Project 2

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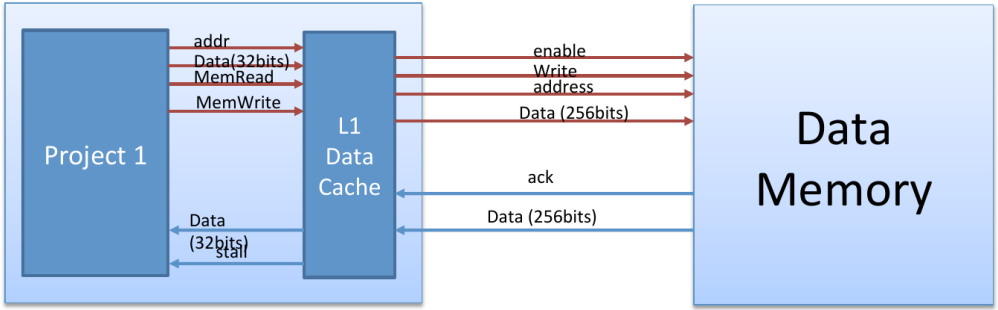
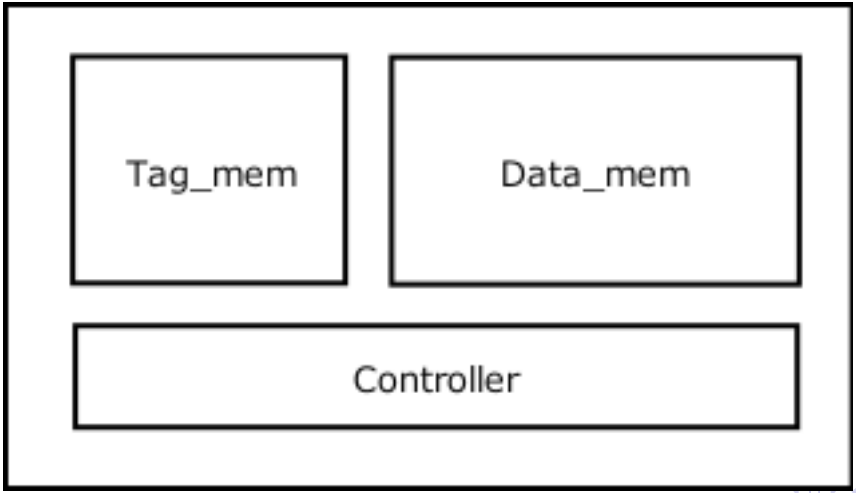
System Block Diagram

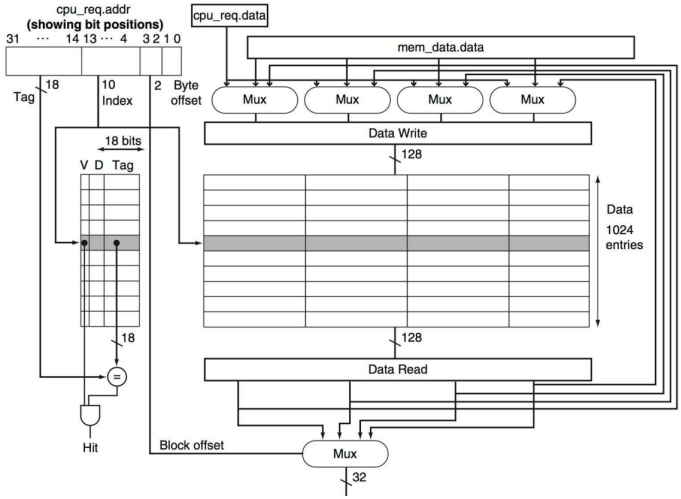


From TA

L1 Cache Structure



Example of Read and Write Structure



Difference

- 8 Mux instead of 4 Mux when write (8 words in a cache line)
- 31:10 tag bit, 9:5 index bit, 4:0 offset bit (spec)

Deciding the Source of Data

Table: Deciding the Source of Data

	Load Word (Read)	Store Word (Write)
Cache Hit	Every word from SRAM	One word from CPU, other from SRAM
Cache Miss	Every word from DRAM	One word from CPU, other from DRAM

Finite State Machine