Nilufar Ferdous

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PhD Student, Computer Engineering, UCSC

Diverse work experience, including programming, software development, research and teaching assistant.

EXPERIENCE

University of Texas at San Antonio
Teaching Assistant, 2013

EE 3223 :C++ and Data Structures

Responsibilities:

- Grading Homework
- Teaching in classroom

University of Texas at San Antonio
Teaching Assistant, 2013

EE 3563. Digital Systems Design

Responsibilities:

- Lab Sessions in verilog

University of Texas at San Antonio
Research Assistant, 2012-2013

Samsung Austin Research And Development
Performance Intern, 2014-2015

Responsibilities:

Fingerprinting Traces Using Non-Micro Architectural Components: designed and developed a Register Traffic Characterization Engine called RTE by utilizing several advanced libraries of C++ including Boost, Regex, etc. RTE is capable to extract various information including Register Dependency Distance, Register Reuse Degree, etc. from the fingerprint of traces. I performed various types of unit testing and debugging in RTE with a large variety of benchmarks as Hadoop, SPEC, etc. I also developed a Pattern Recognition Engine to recognize and parse the ARMv8 instructions based on the mnemonics available in ARMv8 instruction set.

EDUCATION

University Of Texas at San Antonio
Master in Computer Engineering 2012 - 2014, San Antonio, Texas

Rajshahi University Of Science and Technology
Bachelor in Computer Science and Engineering , 2007, Bangladesh

SKILLS

C/C++ Programming
Verilog
Python
Unix Shell Scripting

TEACHING EXPERIENCES

Teaching Assistant

GRADUATE COURSES COMPLETED

VLSI System Design
VLSI System-on-a-Chip
Computer Architecture and Design
Computer and Network Security
SuperScalar MicroProcessor Architecture

UNDER-GRADUATE COURSES COMPLETED

VLSI System Design
Computer Architecture and Design
Computer and Network Security
C++ and Data Structure
Digital System design

PROJECTS

- Analysis of GSHARE And YAGS Branch Predictor in a Chip Multiprocessor exploiting MOESI Cache Coherence Protocol: The project was done using OPAL, GEMS, RUBY, GARNET and SIMICS simulator.
- Design and Synthesis of a 64-bit RISC Stored-Program Machine using Xilinx and Verilog.
- Design, implementation and synthes of a 64-bit pipelined architecture to support a subset of MIPS ISA using Xilinx, Verilog and Credence Encounter.
- Performance Evaluation of Non Uniform Cache Architecture(NUCA) in Chip Multi Processor.
  The Parsec Benchmark was used for the performance evaluation using GEMS, GARNET, SIMICS simulator.

PUBLICATIONS

- Performance Enhancement in Shared-Memory Multiprocessors using Dynamically Classified Sharing Information.33rd IEEE International Performance Computing and Communication Conference IPCCC 2014,December 1, 2014.