

make

Adapted from materials by Dr. Carrier



Compiling

How do we compile this program?

Contents of main.c:

```
#include <stdio.h>

#include "vector.h"
#include "cool_math.h"

int main(){
    // ...
}
```

Result of ls:

```
class/c/make_files/example_project$ ls
cool_math.c  cool_math.h  main.c  vector.c  vector.h
```

```
gcc main.c cool_math.c vector.c
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gcc main.c cool_math.c vector.c
```

Or

```
gcc -c vector.c -o vector.o
```

```
gcc -c cool_math.c -o cool_math.o
```

```
gcc main.c vector.o cool_math.o
```

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We are using GNU make

Running make

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2. Run `make` (just that one word)
 - a. Alternatively you can run `make rule` to run that specific rule

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Note, recipes line start with a tab, not spaces!

[Ctrl + V then Tab in Vim \(if you use spaces via expandtab\)](#)

Example (simple)

To compile our example from earlier

```
default: main.c vector.c cool_math.c
```

```
gcc -o program main.c vector.c cool_math.c
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Note that running make will run the “default” rule, or the first in the file if default doesn’t exist

Example (advanced)

To compile our example from earlier

```
default: program
```

```
program: main.c vector.o cool_math.o
```

```
    gcc -o program main.c vector.o cool_math.o
```

```
vector.o: vector.c
```

```
    gcc -o vector.o -c vector.c
```

```
cool_math.o: cool_math.c
```

```
    gcc -o cool_math.o -c cool_math.c
```

Future compilation will only recompile what's needed! (uses file modified dates/times)

Making changes easier

What if we want to change compilers later?

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```
CC = gcc
```

```
CFLAGS = -Wall
```

```
program: main.c vector.o
```

```
    $(CC) $(CFLAGS) -o program main.c vector.o
```

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We can use variables!

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CC = gcc
```

```
CFLAGS = -Wall
```

```
program: main.c vector.o
```

```
    $(CC) $(CFLAGS) -o program main.c vector.o
```

Note we access variables with \$(var)

This is different from bash scripts!

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```
%.o : %.c
```

```
    gcc -o $@ -c $<
```

This generalizes our `vector.o` and `cool_math.o` from our example!

Comments

Comments start with `#`, just like in bash!

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clean:
```

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```

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Another common example is the `install` rule

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Why use make over a bash script?

- The recursive prereq lookup
- The date-checking to prevent us from recompiling files that haven't changed