CS 223 Digital Design

Section 01

Lab 03

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**b-) Behavioral System Verilog**

module twoToFourDecoder(input logic a, b, output logic y0, y1,y2, y3);

assign y0 = ~a & ~ b;

assign y1 = ~a & b;

assign y2 = a & ~b;

assign y3 = a & b;

endmodule

**Testbench**

module testbenchForTwoToOneDecoder();

logic a,b, y0, y1, y2, y3;

twoToFourDecoder(a, b, y0, y1, y2, y3);

initial begin

a = 0; b = 0;#10;

a = 0; b = 1;#10;

a = 1; b = 0;#10;

a = 1; b = 1;#10;

end

endmodule

**c-)**

**Behavioral System Verilog**

module fourToOneMux(input logic a, b, c, d, s0, s1, output logic y);

assign y = s1 ? ( s0 ? d : c) : ( s0 ? b: a);

endmodule

**Testbench**

module testbenchForFourToOneMux();

logic a,b,c,d,s0,s1,y;

fourToOneMux test(a,b,c,d,s0,s1,y);

initial begin

a = 0; b = 0; c = 0; d = 0; s0 = 0; s1 = 0;#10;

a = 0; b = 0; c = 0; d = 0; s0 = 0; s1 = 1;#10;

a = 0; b = 0; c = 0; d = 0; s0 = 1; s1 = 0;#10;

a = 0; b = 0; c = 0; d = 0; s0 = 1; s1 = 1;#10;

a = 0; b = 0; c = 0; d = 1; s0 = 0; s1 = 0;#10;

a = 0; b = 0; c = 0; d = 1; s0 = 0; s1 = 1;#10;

a = 0; b = 0; c = 0; d = 1; s0 = 1; s1 = 0;#10;

a = 0; b = 0; c = 0; d = 1; s0 = 1; s1 = 1;#10;

a = 0; b = 0; c = 1; d = 0; s0 = 0; s1 = 0;#10;

a = 0; b = 0; c = 1; d = 0; s0 = 0; s1 = 1;#10;

a = 0; b = 0; c = 1; d = 0; s0 = 1; s1 = 0;#10;

a = 0; b = 0; c = 1; d = 0; s0 = 1; s1 = 1;#10;

a = 0; b = 0; c = 1; d = 1; s0 = 0; s1 = 0;#10;

a = 0; b = 0; c = 1; d = 1; s0 = 0; s1 = 1;#10;

a = 0; b = 0; c = 1; d = 1; s0 = 1; s1 = 0;#10;

a = 0; b = 0; c = 1; d = 1; s0 = 1; s1 = 1;#10;

a = 0; b = 1; c = 0; d = 0; s0 = 0; s1 = 0;#10;

a = 0; b = 1; c = 0; d = 0; s0 = 0; s1 = 1;#10;

a = 0; b = 1; c = 0; d = 0; s0 = 1; s1 = 0;#10;

a = 0; b = 1; c = 0; d = 0; s0 = 1; s1 = 1;#10;

a = 0; b = 1; c = 0; d = 1; s0 = 0; s1 = 0;#10;

a = 0; b = 1; c = 0; d = 1; s0 = 0; s1 = 1;#10;

a = 0; b = 1; c = 0; d = 1; s0 = 1; s1 = 0;#10;

a = 0; b = 1; c = 0; d = 1; s0 = 1; s1 = 1;#10;

a = 0; b = 1; c = 1; d = 0; s0 = 0; s1 = 0;#10;

a = 0; b = 1; c = 1; d = 0; s0 = 0; s1 = 1;#10;

a = 0; b = 1; c = 1; d = 0; s0 = 1; s1 = 0;#10;

a = 0; b = 1; c = 1; d = 0; s0 = 1; s1 = 1;#10;

a = 0; b = 1; c = 1; d = 1; s0 = 0; s1 = 0;#10;

a = 0; b = 1; c = 1; d = 1; s0 = 0; s1 = 1;#10;

a = 0; b = 1; c = 1; d = 1; s0 = 1; s1 = 0;#10;

a = 0; b = 1; c = 1; d = 1; s0 = 1; s1 = 1;#10;

a = 1; b = 0; c = 0; d = 0; s0 = 0; s1 = 0;#10;

a = 1; b = 0; c = 0; d = 0; s0 = 0; s1 = 1;#10;

a = 1; b = 0; c = 0; d = 0; s0 = 1; s1 = 0;#10;

a = 1; b = 0; c = 0; d = 0; s0 = 1; s1 = 1;#10;

a = 1; b = 0; c = 0; d = 1; s0 = 0; s1 = 0;#10;

a = 1; b = 0; c = 0; d = 1; s0 = 0; s1 = 1;#10;

a = 1; b = 0; c = 0; d = 1; s0 = 1; s1 = 0;#10;

a = 1; b = 0; c = 0; d = 1; s0 = 1; s1 = 1;#10;

a = 1; b = 0; c = 1; d = 0; s0 = 0; s1 = 0;#10;

a = 1; b = 0; c = 1; d = 0; s0 = 0; s1 = 1;#10;

a = 1; b = 0; c = 1; d = 0; s0 = 1; s1 = 0;#10;

a = 1; b = 0; c = 1; d = 0; s0 = 1; s1 = 1;#10;

a = 1; b = 0; c = 1; d = 1; s0 = 0; s1 = 0;#10;

a = 1; b = 0; c = 1; d = 1; s0 = 0; s1 = 1;#10;

a = 1; b = 0; c = 1; d = 1; s0 = 1; s1 = 0;#10;

a = 1; b = 0; c = 1; d = 1; s0 = 1; s1 = 1;#10;

a = 1; b = 1; c = 0; d = 0; s0 = 0; s1 = 0;#10;

a = 1; b = 1; c = 0; d = 0; s0 = 0; s1 = 1;#10;

a = 1; b = 1; c = 0; d = 0; s0 = 1; s1 = 0;#10;

a = 1; b = 1; c = 0; d = 0; s0 = 1; s1 = 1;#10;

a = 1; b = 1; c = 0; d = 1; s0 = 0; s1 = 0;#10;

a = 1; b = 1; c = 0; d = 1; s0 = 0; s1 = 1;#10;

a = 1; b = 1; c = 0; d = 1; s0 = 1; s1 = 0;#10;

a = 1; b = 1; c = 0; d = 1; s0 = 1; s1 = 1;#10;

a = 1; b = 1; c = 1; d = 0; s0 = 0; s1 = 0;#10;

a = 1; b = 1; c = 1; d = 0; s0 = 0; s1 = 1;#10;

a = 1; b = 1; c = 1; d = 0; s0 = 1; s1 = 0;#10;

a = 1; b = 1; c = 1; d = 0; s0 = 1; s1 = 1;#10;

a = 1; b = 1; c = 1; d = 1; s0 = 0; s1 = 0;#10;

a = 1; b = 1; c = 1; d = 1; s0 = 0; s1 = 1;#10;

a = 1; b = 1; c = 1; d = 1; s0 = 1; s1 = 0;#10;

a = 1; b = 1; c = 1; d = 1; s0 = 1; s1 = 1;#10;

end

endmodule

**d-) Schematic**

D0

D1

D2

D3

D4

D5

D6

D7

S2

S0 S1

S0 S1



Y

**Structural System Verilog**

module eightToOneMux(input logic d0, d1, d2, d3, d4, d5, d6, d7, s0, s1, s2, output logic y);

logic a, b, c, d, e;

fourToOneMux mux1 (d0, d1, d2, d3, s0, s1, a);

fourToOneMux mux2(d4, d5, d6, d7, s0, s1, b);

and(d, b, s2);

not(e, s2);

and(c, a, e);

or(y, c, d);

endmodule

**Testbench**

module testbenchForEightToOneMux();

logic d0, d1, d2, d3, d4, d5, d6, d7, s0, s1, s2, y;

eightToOneMux mux(d0, d1, d2, d3, d4 ,d5, d6, d7, s0, s1, s2, y);

initial begin

d0 = 0; d1 = 0; d2 = 1; d3 = 1; d4 = 0; d5 = 0; d6 = 1; d7 = 1; s0 = 0; s1 = 0; s2 = 0; #10;

d0 = 0; d1 = 0; d2 = 1; d3 = 1; d4 = 0; d5 = 0; d6 = 1; d7 = 1; s0 = 0; s1 = 0; s2 = 1; #10;

d0 = 0; d1 = 0; d2 = 1; d3 = 1; d4 = 0; d5 = 0; d6 = 1; d7 = 1; s0 = 0; s1 = 1; s2 = 0; #10;

d0 = 0; d1 = 0; d2 = 1; d3 = 1; d4 = 0; d5 = 0; d6 = 1; d7 = 1; s0 = 0; s1 = 1; s2 = 1; #10;

d0 = 0; d1 = 0; d2 = 1; d3 = 1; d4 = 0; d5 = 0; d6 = 1; d7 = 1; s0 = 1; s1 = 0; s2 = 0; #10;

d0 = 0; d1 = 0; d2 = 1; d3 = 1; d4 = 0; d5 = 0; d6 = 1; d7 = 1; s0 = 1; s1 = 0; s2 = 1; #10;

d0 = 0; d1 = 0; d2 = 1; d3 = 1; d4 = 0; d5 = 0; d6 = 1; d7 = 1; s0 = 1; s1 = 1; s2 = 0; #10;

d0 = 0; d1 = 0; d2 = 1; d3 = 1; d4 = 0; d5 = 0; d6 = 1; d7 = 1; s0 = 1; s1 = 1; s2 = 1; #10;

end

endmodule

**e-)**

S3 S2 S1

000

001

010

011

100

101

110

111

S0

VDD

Y

**System Verilog Module**

module eightToOneMuxForF(input logic s0, s1, s2, s3, output logic y);

eightToOneMux forF(s0, ~s0, s0, s0, 1, ~s0, ~s0, s0, s1, s2, s3, y);

endmodule

**TESTBENCH**

module testbenchForEightToOneMuxForF();

logic s0,s1,s2,s3,y;

eightToOneMuxForF test(s0 ,s1 ,s2 , s3, y);

initial begin

s0 = 0; s1 = 0; s2 = 0; s3 = 0;#10;

s0 = 0; s1 = 0; s2 = 0; s3 = 1;#10;

s0 = 0; s1 = 0; s2 = 1; s3 = 0;#10;

s0 = 0; s1 = 0; s2 = 1; s3 = 1;#10;

s0 = 0; s1 = 1; s2 = 0; s3 = 0;#10;

s0 = 0; s1 = 1; s2 = 0; s3 = 1;#10;

s0 = 0; s1 = 1; s2 = 1; s3 = 0;#10;

s0 = 0; s1 = 1; s2 = 1; s3 = 1;#10;

s0 = 1; s1 = 0; s2 = 0; s3 = 0;#10;

s0 = 1; s1 = 0; s2 = 0; s3 = 1;#10;

s0 = 1; s1 = 0; s2 = 1; s3 = 0;#10;

s0 = 1; s1 = 0; s2 = 1; s3 = 1;#10;

s0 = 1; s1 = 1; s2 = 0; s3 = 0;#10;

s0 = 1; s1 = 1; s2 = 0; s3 = 1;#10;

s0 = 1; s1 = 1; s2 = 1; s3 = 0;#10;

s0 = 1; s1 = 1; s2 = 1; s3 = 1;#10;

end

endmodule