DIGITAL INTEGRATED CIRCUITS
PROJECT

1011 Non-Overlapping Moore Sequence Detector

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1) INTRODUCTION

Sequence detector is designed and its CMOS layout is drawed using Magic layout tool. When detector receives a sequence 1011, its output will be high at the end of the sequence. For any other sequence, output will be low. Circuit is non-overlapping thus, an overlapping sequence like 1011011 will output low at the end of sequence, but since first part of the sequence 1011, it will make output high at that position. Circuit is designed as a Moore machine, so it will change its output, only if its state is changed. Input does not affect the output directly.

Positive edge triggered D flip flop is used in the project. Input is only considered during the positive edge of the clock signal. During the other part of clock signal, input does not affect the state of flip flop.

Circuit is drawed at TSMC 0.25 µm technology using Magic layout tool. Lambda in this technology is λ =0.12 µm. Gate length of the mosfets is 2λ. The width of mosfet is chosen as 5λ for nMOS and 10λ for pMOS to approximate high to low delay and low to high delay time.

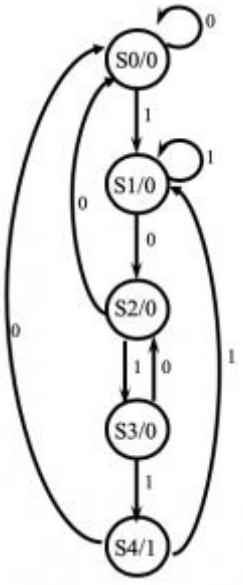

FIGURE 1.1 : State Diagram of Circuit

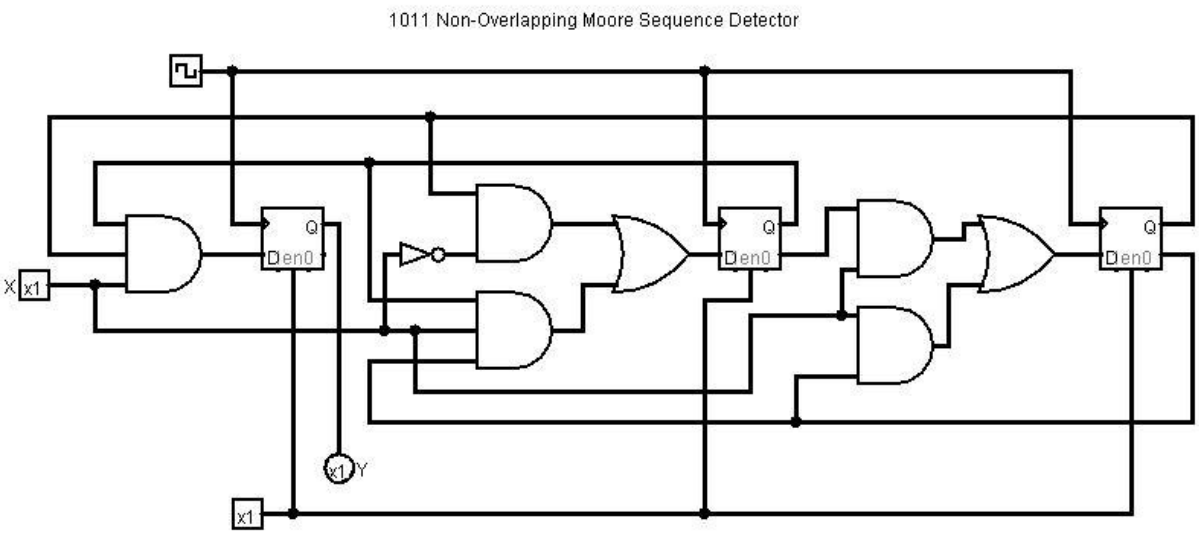

FIGURE 1.2 : Circuit Diagram

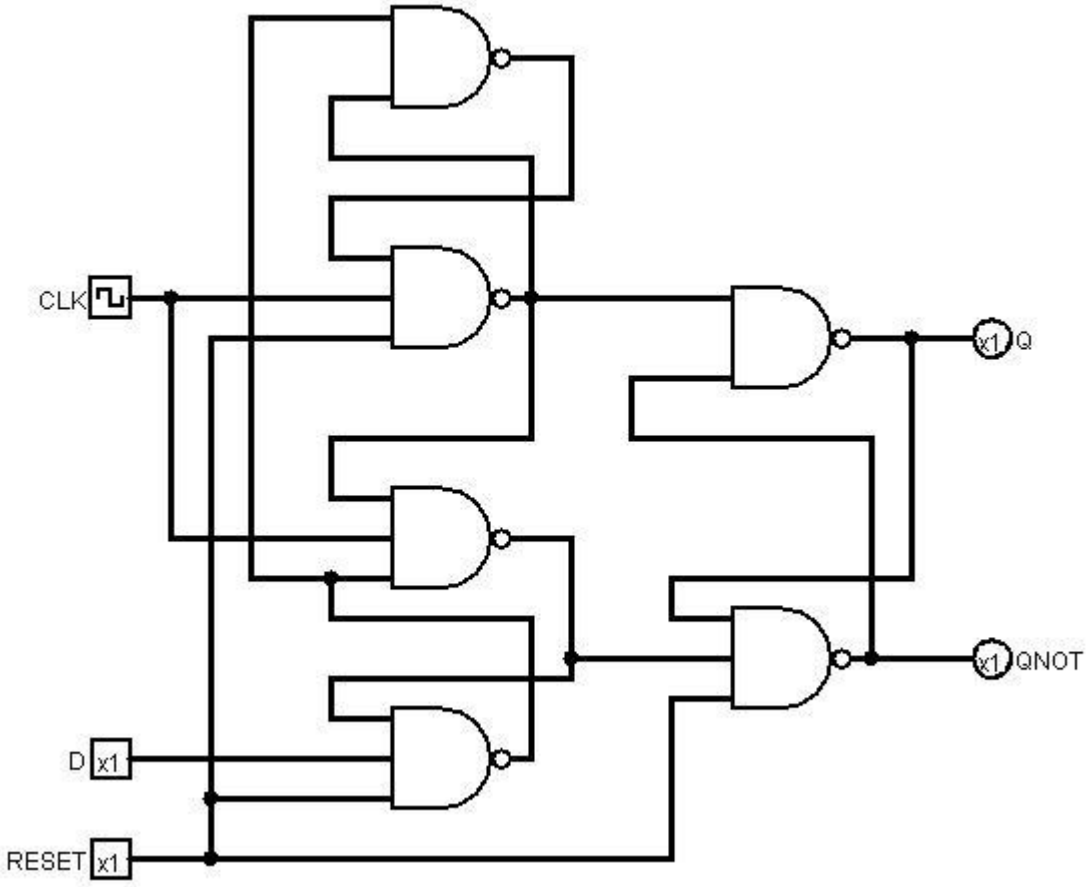

FIGURE 1.3 : D Flip Flop Diagram

2) Circuits and Delays

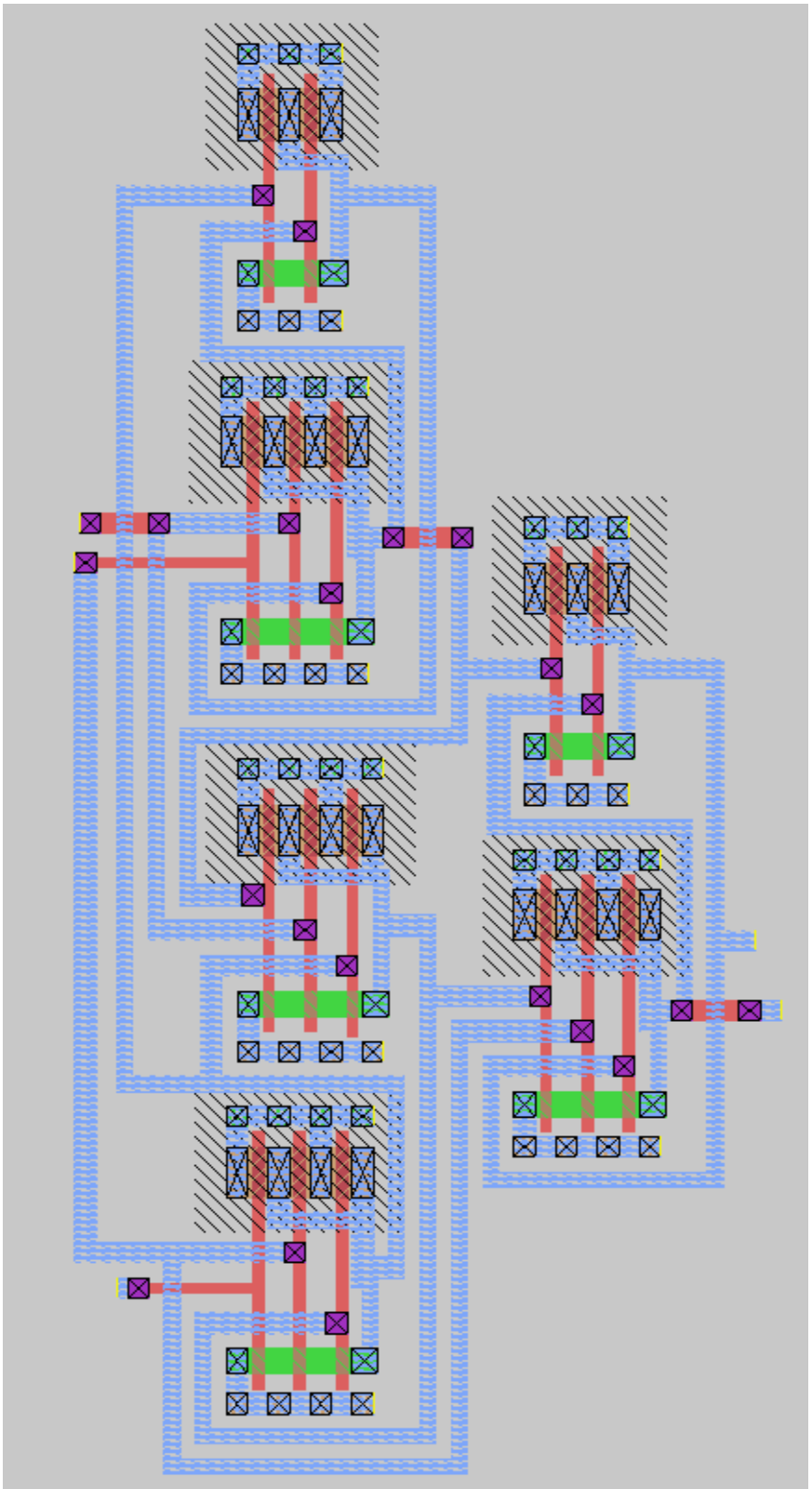

FIGURE : 1.4 : D Flip Flop CMOS Layout

Total area used for D flip flop 140λ x 288λ

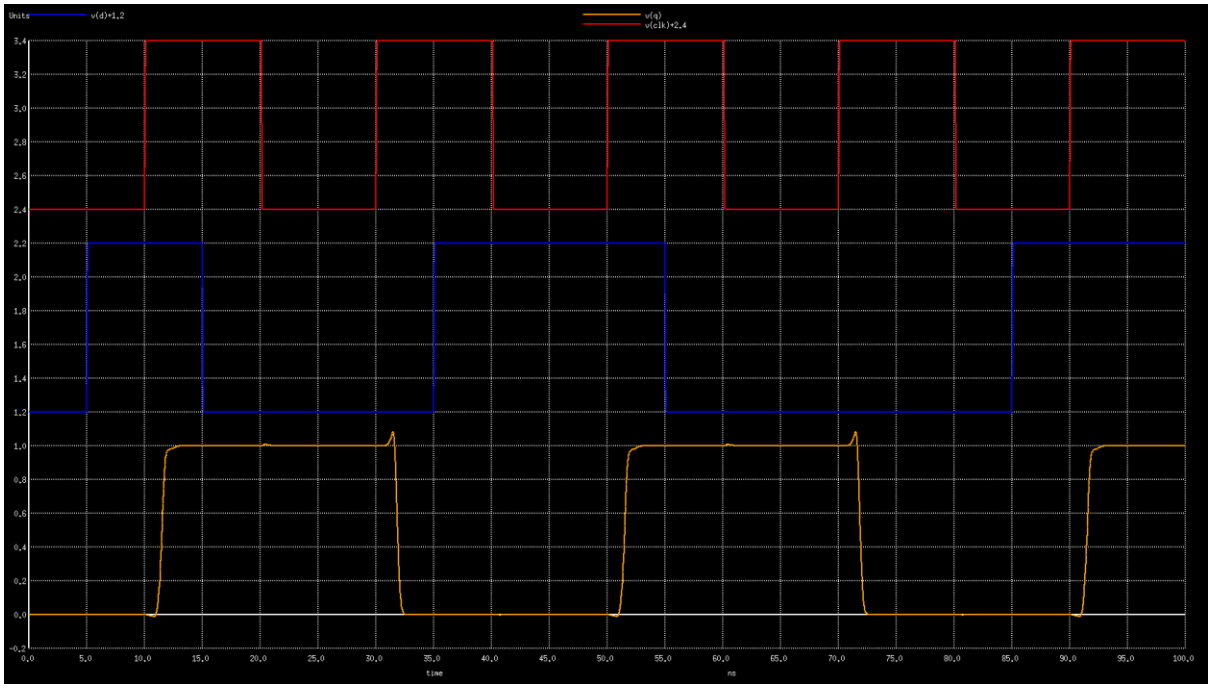

FIGURE 1.5 : D Flip Flop Test

DELAYS	T
Rising Delay	2.8ns
Falling Delay	2.4ns

TABLE 1.1 : D Flip Flop Delay

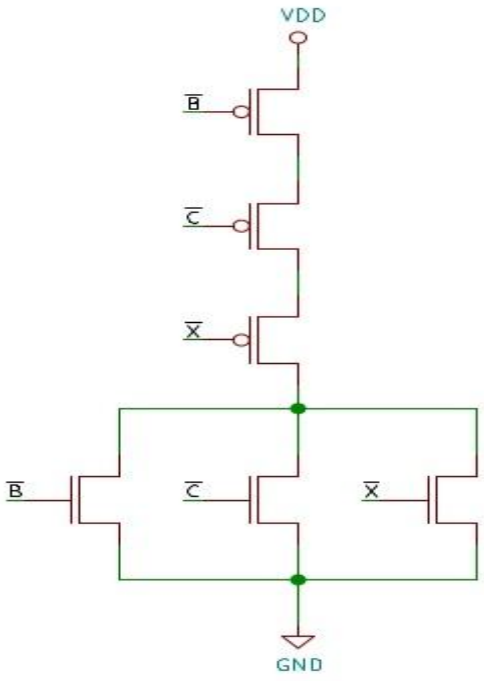

FIGURE 1.6 : Input Gate For A Flip Flop

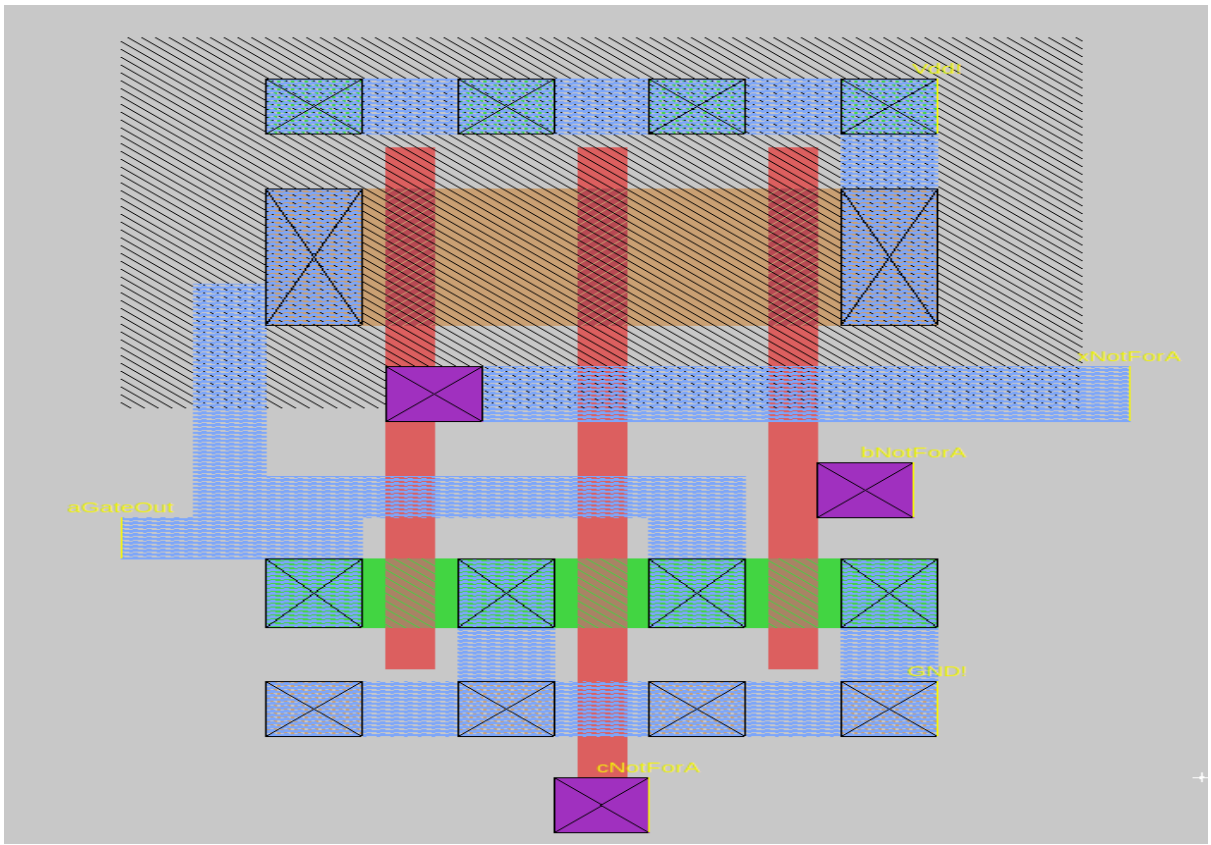

FIGURE 1.7 : Input Gate CMOS Layout For A Flip Flop

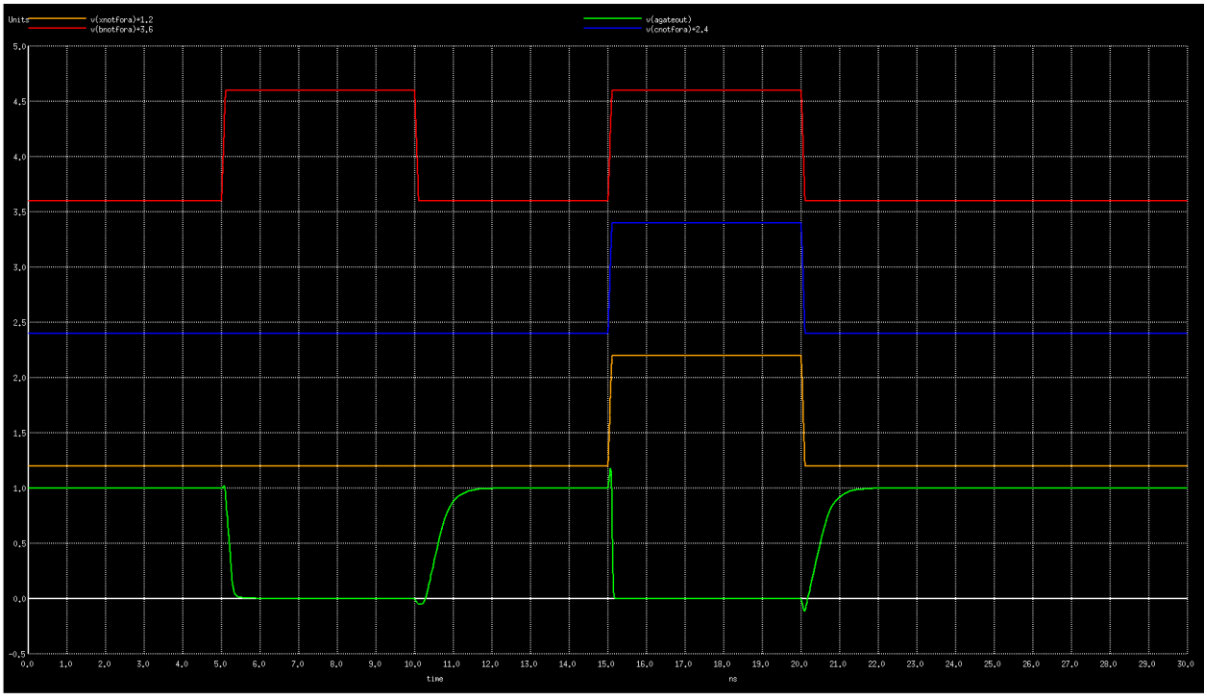

FIGURE 1.8 : Input Gate For A FF Delays

DELAYS	~B	~C	~X	T
Worst Falling Delay	0	0	0	0.4ns
	1	0	0	
Best Falling Delay	0	0	0	0.15ns
	1	1	1	
Worst Rising Delay	1	1	1	1.6ns
	0	0	0	
Best Rising Delay	0	0	1	1.2ns
	0	0	0	

TABLE 1.2 : Delays For Input Gate A

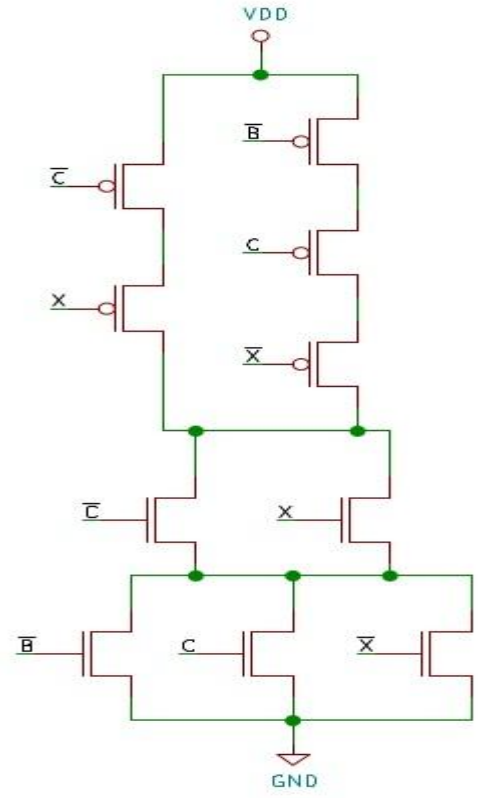

FIGURE 1.9 : Input Gate For B Flip Flop

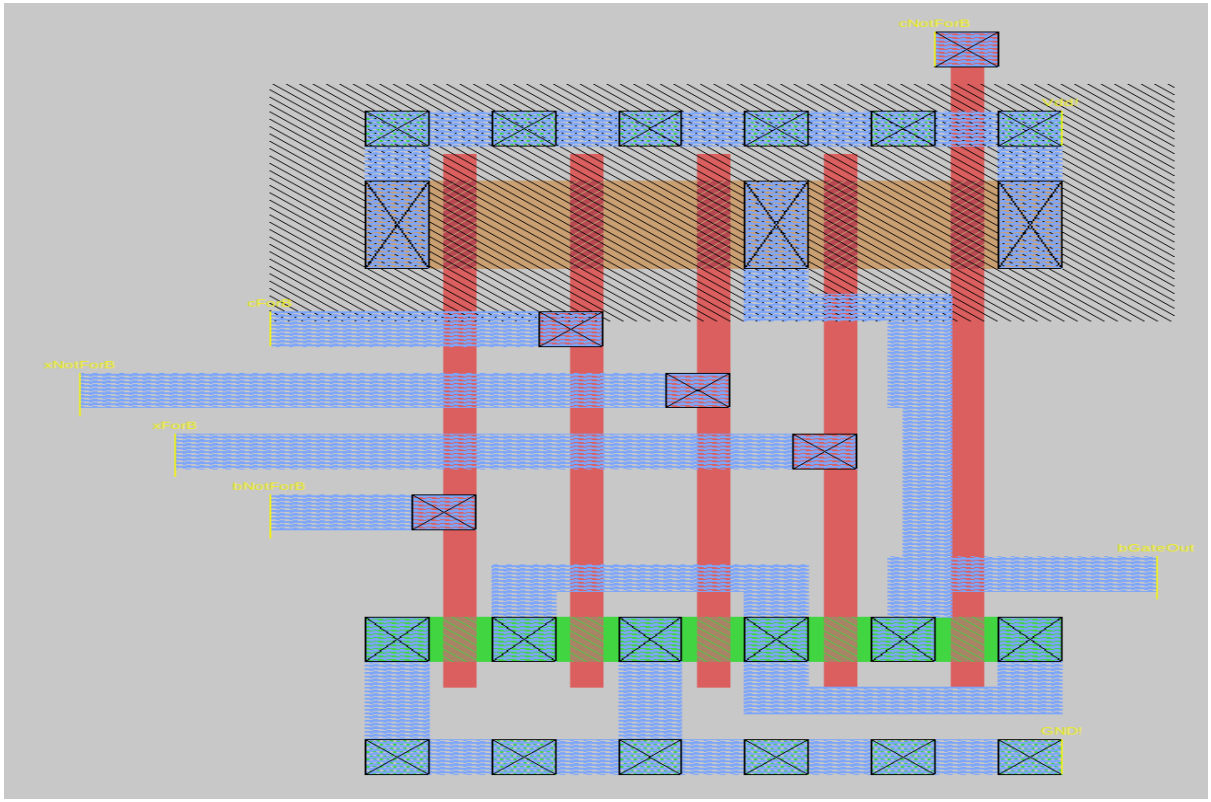

FIGURE 1.10 : Input Gate CMOS Layout For B Flip Flop

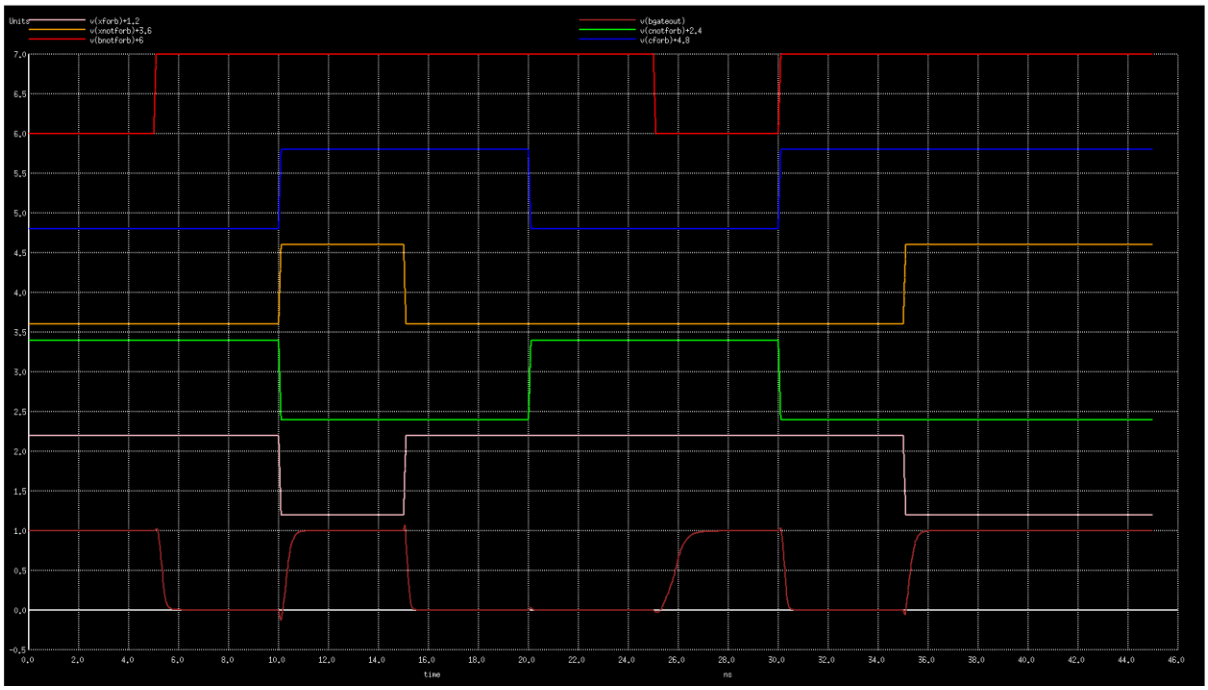

FIGURE 1.11 : Input Gate For B FF Delays

DELAYS	~B	C	~X	~C	X	T
Worst Falling Delay	0	0	0	1	1	0.7ns
	1	0	0	1	1	
Best Falling Delay	1	1	1	0	0	0.4ns
	1	1	0	0	1	
Worst Rising Delay	1	0	0	1	1	1.8ns
	0	0	0	1	1	
Best Rising Delay	1	1	0	0	1	0.8ns
	1	1	1	0	0	

TABLE 1.3 : Delays For Input Gate B

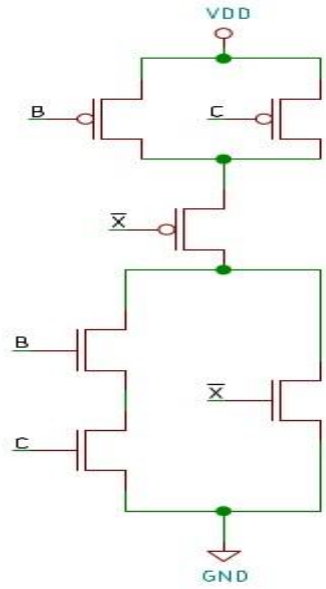

FIGURE 1.12 : Input Gate For C Flip Flop

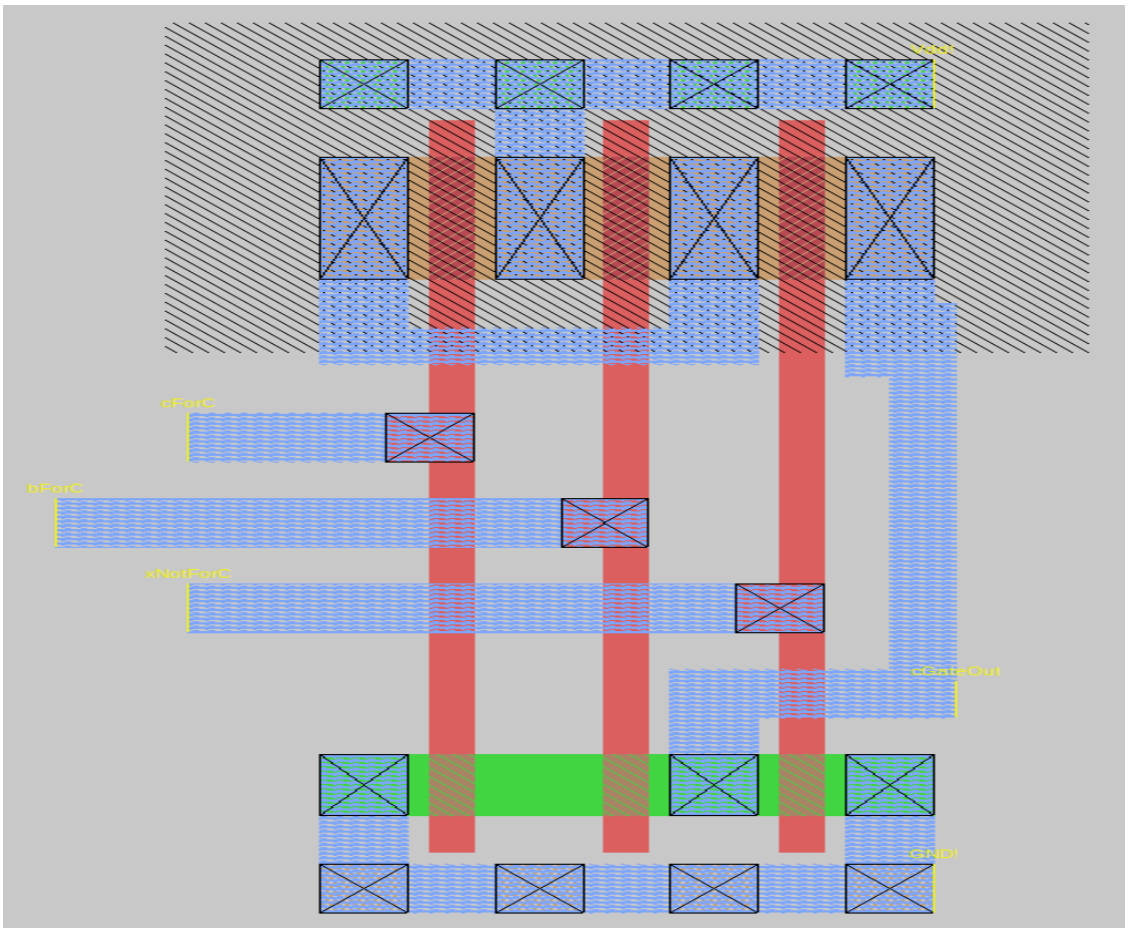

FIGURE 1.13 : Input Gate CMOS Layout For C Flip Flop

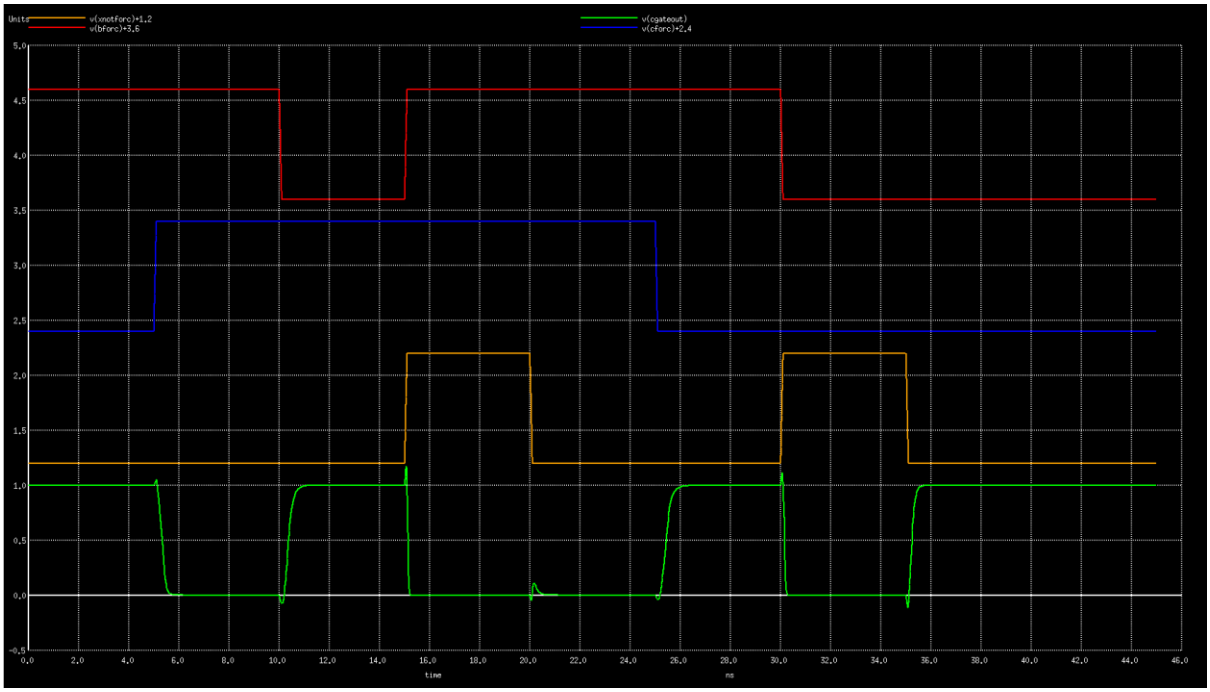

FIGURE 1.14 : Input Gate For C FF Delays

DELAYS	B	C	~X	T
Worst Falling Delay	1	0	0	0.7ns
	1	1	0	
Best Falling Delay	0	1	0	0.2ns
	1	1	1	
Worst Rising Delay	1	1	0	1ns
	1	0	0	
Best Rising Delay	0	0	1	0.6ns
	0	0	0	

TABLE : 1.4 : Delays For Input Gate C

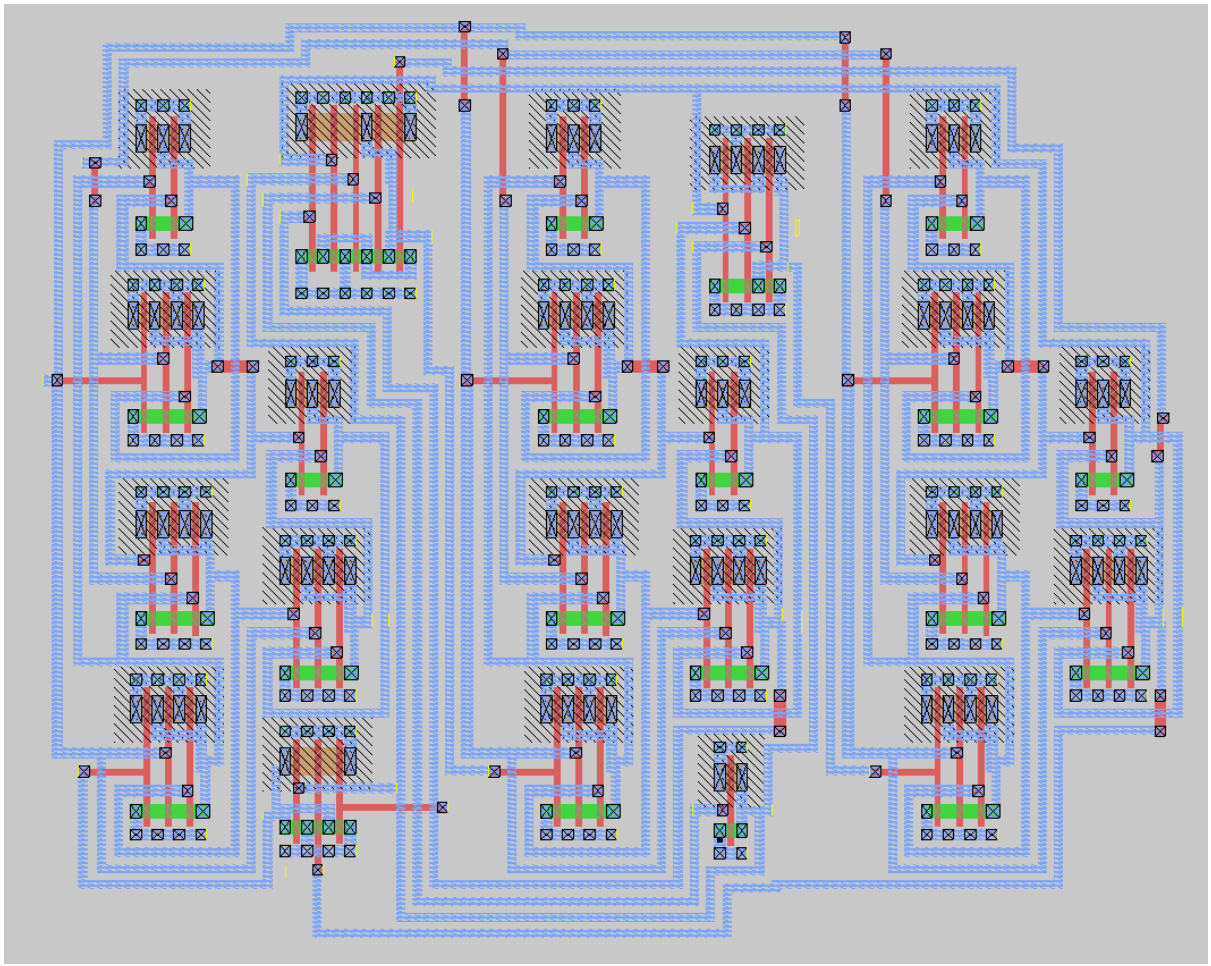

FIGURE 1.15 : 1011 Sequence Detector CMOS Layout

Total area used for the project -> 426λ x 340λ

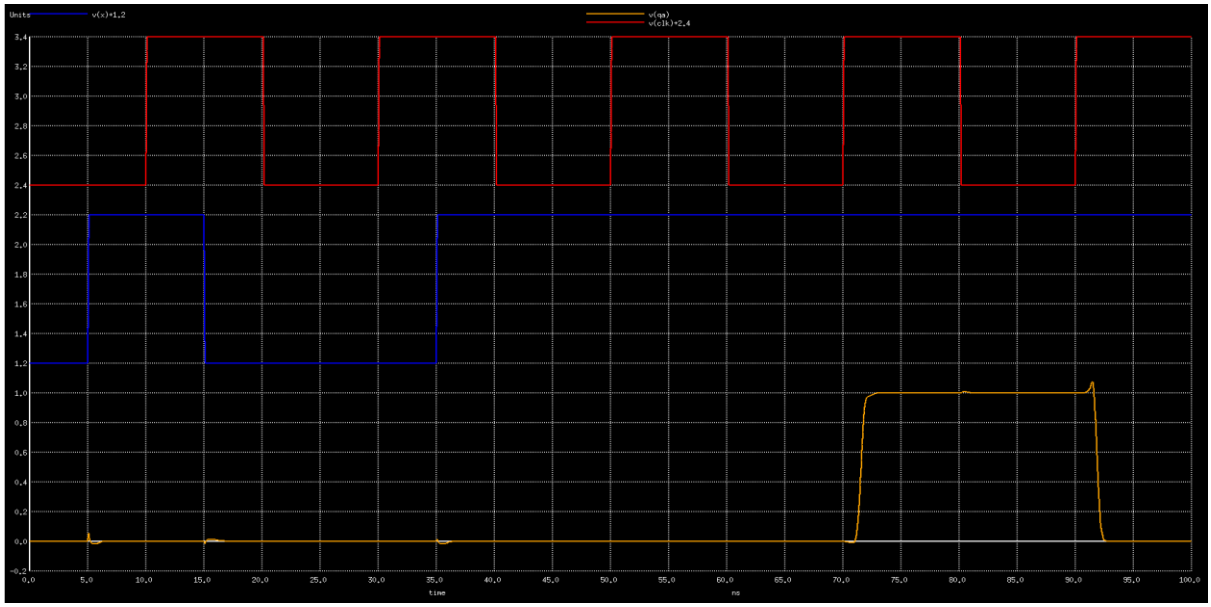

FIGURE 1.16 : Test For Sequence 1011

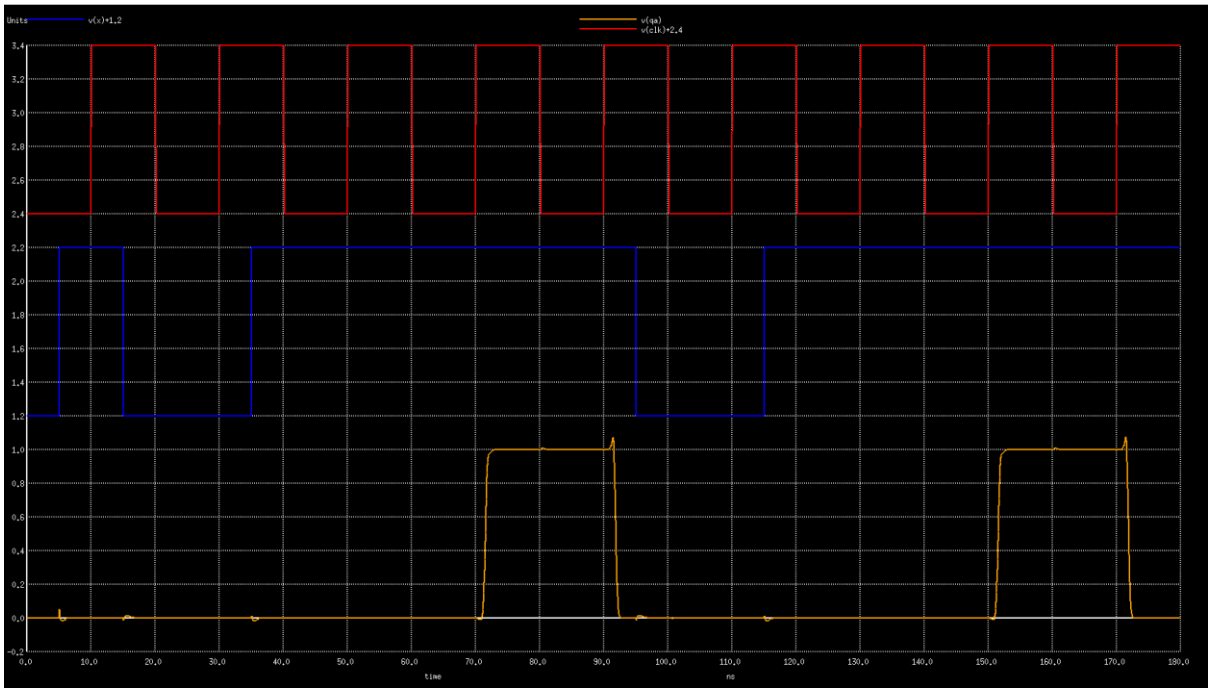

FIGURE 1.17 : Test For Non-Overlapping Sequence 10111011

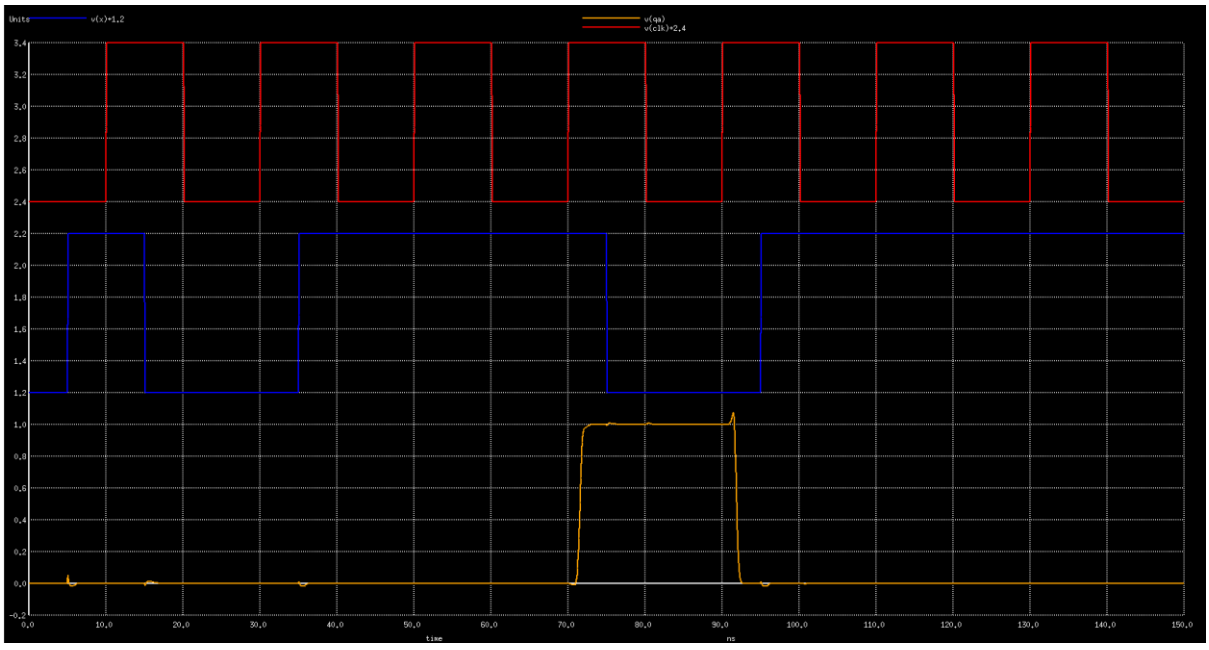

FIGURE 1.18 : Test For Over-Lapping Sequence 1011011

DELAYS	T
Rising Delay	2.8ns
Falling Delay	2.4ns

TABLE 1.5 : Delays When Sequence Detected

3) Enhancement

Size of mosfets could be adjusted to achieve equal rise and fall resistance. So that worst case delays are approximated.

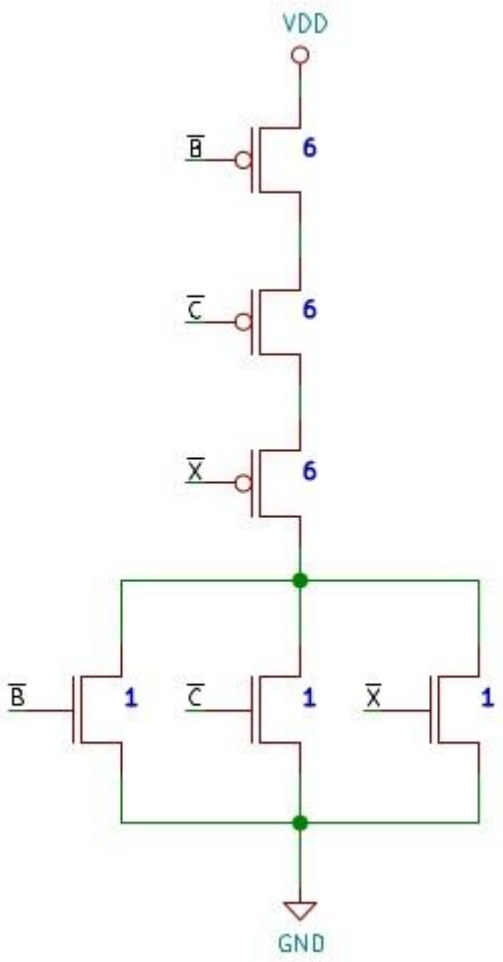

FIGURE 1.15 : Input Gate for A FF

If width of nMos is 10λ, pMos width should be 60λ.

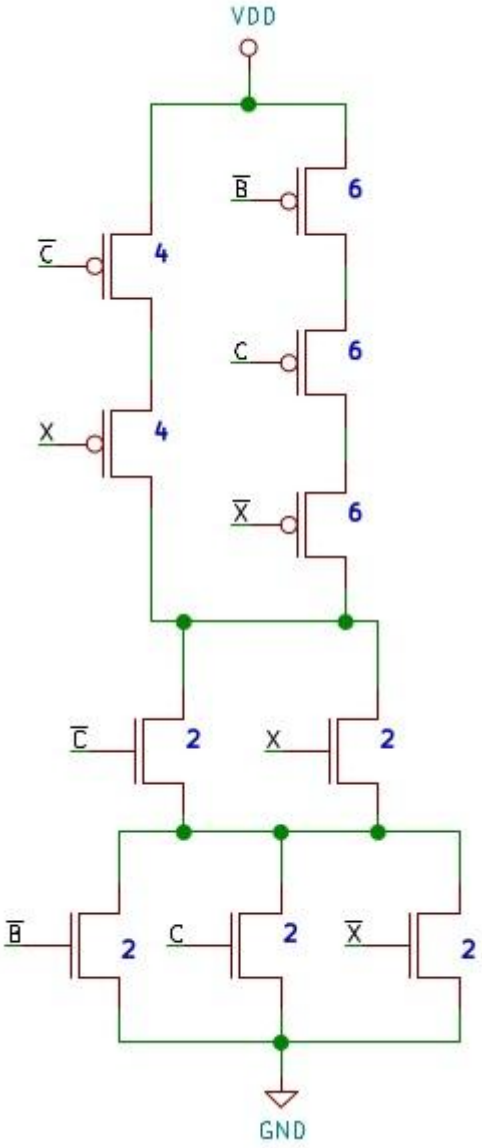

FIGURE 1.16 : Input Gate For B FF

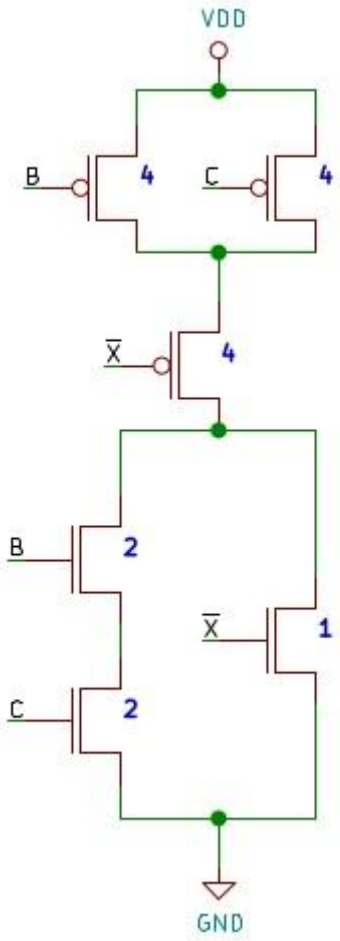

FIGURE 1.16 : Input Gate For C FF