1. Implement the following Boolean functions using only NAND gates. Implement them in Verilog.
   a. $f_1=\sum(0,2,3,4,5,7)$
   b. $f_2=\sum(1,5,7,8,9,10,11,13,15)$
   c. $f_3=\sum(0,4,5,15)+\sum_d(2,7,8,10,12,13)$
   d. $f_4=\sum(1,4,5,13,14,15)+\sum_d(7,8,9,12)$
   e. $f_5=\sum(1,3,4,5,11,12,14)+\sum_d(6,7,9)$
2. Design a module having one input *i*, as an unsigned on 3 bits and one output *o*, on 1 bit. The output *o* is generated as bellow. Implement the unit in Verilog.

$$o=\begin{cases}1, & if\ \ i=4k-3, k\in\mathbb{N}\\ 0, & otherwise\end{cases}$$

3. Implement the Binary Coded Decimal converter given by the truth table below. Implement it in Verilog.

Inputs				Outputs			
i_3	i_2	i_1	i_0	o_3	o_2	o_1	o_0
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	1
0	1	0	0	0	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	1	1	1

4. Build a Verilog module, receiving on the 6-bit input *i* non-negative integer numbers. Module's output, on 1 bit is called *is6* and will be active if the decimal's figure of the input number's decimal representation is 6 (Example: i=32 -> is6=0; i=60 -> is6=1; i=63 -> is6=1)