Materia:

Diseño de Circuitos Integrados Digitales CMOS I

Nombre de la Tarea:

Práctica 19 - Detección de presencia con sensor piroeléctrico y un foco de actuador

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Introduction.

Our teacher proposes us to do an exercise or practice of a Controlled Environment as a sensored light with pyroelectric sensor. Explaining us how to use this system in the program: "Quartus Prime" with the objective to performing it in the chipset FPGA and visualize how the light activates with the presence of someone

Theoretical Framework.

- Background: Be able to program a FPGA chipset (more specifically, the Terasic DE10-Lite board) to ensure that in the future, we can do a bigger project with this board along. In this case, the exercise is to do a Controlled Environment as a pyroelectric sensor. For see how to apply this system to the board and learn how to use the vectors and all the parameters this project needs.
- Theoretical basis: After having consulted and read in its entirety the theory of this circuit, we can establish:
    - Apply the knowledge acquired in the past projects of Quartus Prime we do it.
    - How to create code in this program in an advanced way with the vectors.
    - Have the possibility to make a practice without help
    - Manipulate the modules of the board efficiently for the optimal functioning in the exercise, in this case, the ports of the FPGA.
    - Know how to use the clock signals of the board.

Development.

In this practice we have the demonstration of a clock signal represented in the lights, having a reaction with the reaction of someone in front of the person.

With the passed knowledge of how use the clocks, represent the pins and use the ports and the address of the components, we can have an idea on how it can work all and how the inputs can be processed on this new practice with a clock and the response of the lights in determinate moments of the time

But, what is a Clock Signal and how works on this project? Or, how works an pyroelectric sensor? Because we already mentioned a bit about how this would work, but not so clear.

Clock Signal.

A clock signal in electronics and synchronous digital circuits is an essential element that synchronizes the actions of various digital components. It functions like a metronome, oscillating between high and low states at a constant frequency. This signal is produced by a clock generator, typically in the form of a square wave with a 50% duty cycle.

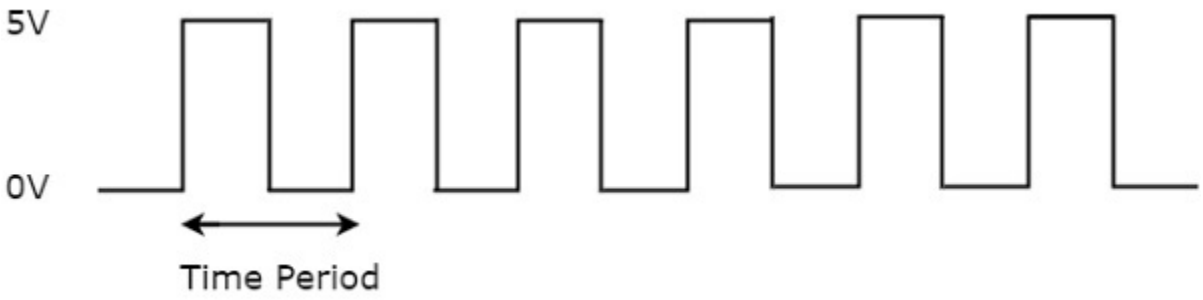
The clock signal serves as a reference for storage devices, flip-flops, and latches, ensuring that they all change state simultaneously to prevent race conditions. It can trigger circuit activity at the rising edge, falling edge, or both edges of the clock cycle in the case of double data rate synchronization.

Clock signals can be represented in different ways. When the ON and OFF times are equal, the signal appears as a square wave with a consistent high and low voltage level. However, the ON and OFF times can also vary, resulting in a train of pulses with different durations for the high and low states.

The time period of the clock signal can be calculated as twice the ON time or twice the OFF time for a square wave, or as the sum of the ON and OFF times for a train of pulses.

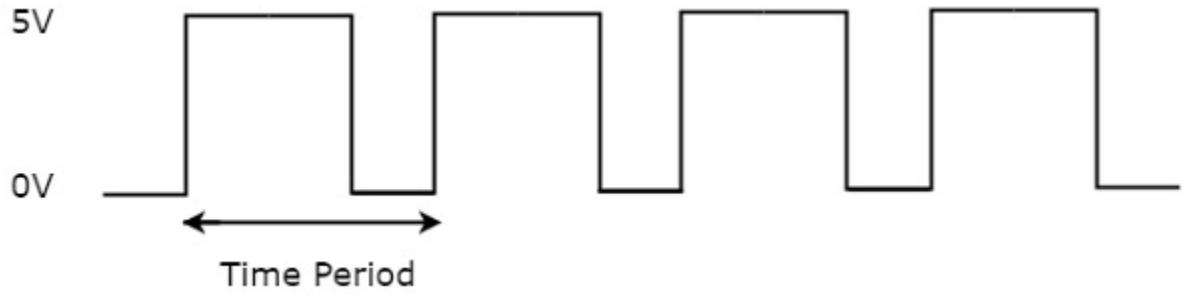
The frequency of the clock signal, which is the reciprocal of its time period, determines the operating frequency of sequential circuits. Sequential circuits rely on clock signals to dictate their timing and enable proper execution of programmed functions.

A square wave is considered as clock signal. This signal stays at logic High (5V) for some time and stays at logic Low (0V) for equal amount of time. This pattern repeats with some time period. In this case, the time period will be equal to either twice of ON time or twice of OFF time.



In that case, train of pulses is considered as clock signal. This signal stays at logic High (5V) for some time and stays at logic Low (0V) for some other time. This pattern repeats with some time period. In this case, the time period will be equal to sum of ON time and OFF time.

The reciprocal of the time period of clock signal is known as the frequency of the clock signal. All sequential circuits are operated with clock signal. So, the frequency at which the sequential circuits can be operated accordingly the clock signal frequency has to be chosen.



Types of triggering

Following are the two possible types of triggering that are used in sequential circuits.

- Level triggering
- Edge triggering

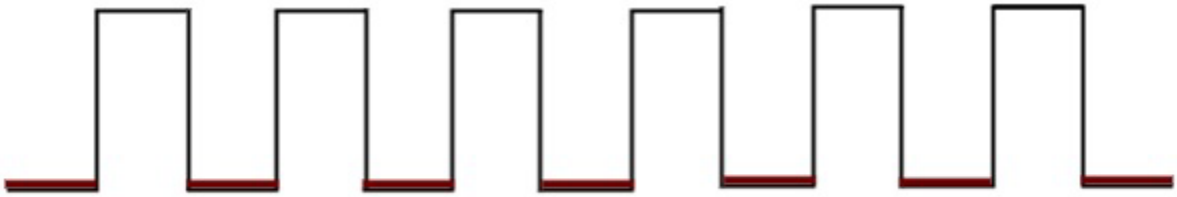
Level triggering

There are two levels, namely logic High and logic Low in clock signal. Following are the two types of level triggering.

- Positive level triggering
- Negative level triggering

If the sequential circuit is operated with the clock signal when it is in Logic High, then that type of triggering is known as Positive level triggering.

If the sequential circuit is operated with the clock signal when it is in Logic Low, then that type of triggering is known as Negative level triggering.



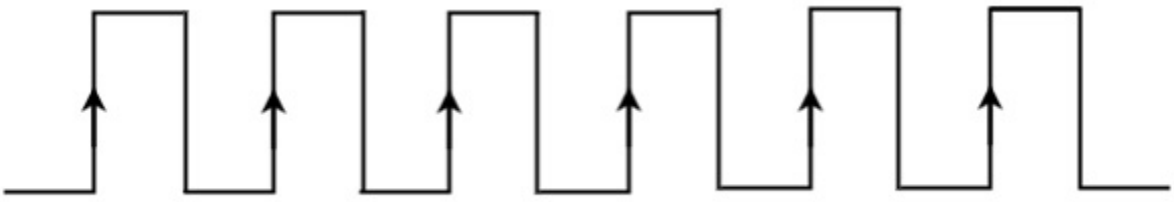
Edge triggering

There are two types of transitions that occur in clock signal. That means, the clock signal transitions either from Logic Low to Logic High or Logic High to Logic Low.

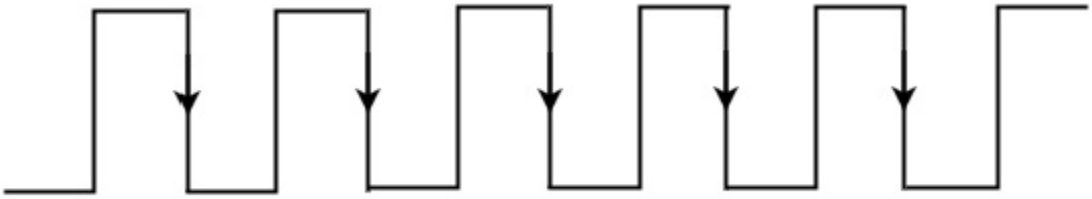
Following are the two types of edge triggering based on the transitions of clock signal.

- Positive edge triggering
- Negative edge triggering

If the sequential circuit is operated with the clock signal that is transitioning from Logic Low to Logic High, then that type of triggering is known as Positive edge triggering. It is also called as rising edge triggering.



If the sequential circuit is operated with the clock signal that is transitioning from Logic High to Logic Low, then that type of triggering is known as Negative edge triggering. It is also called as falling edge triggering.



Pyroelectric sensor

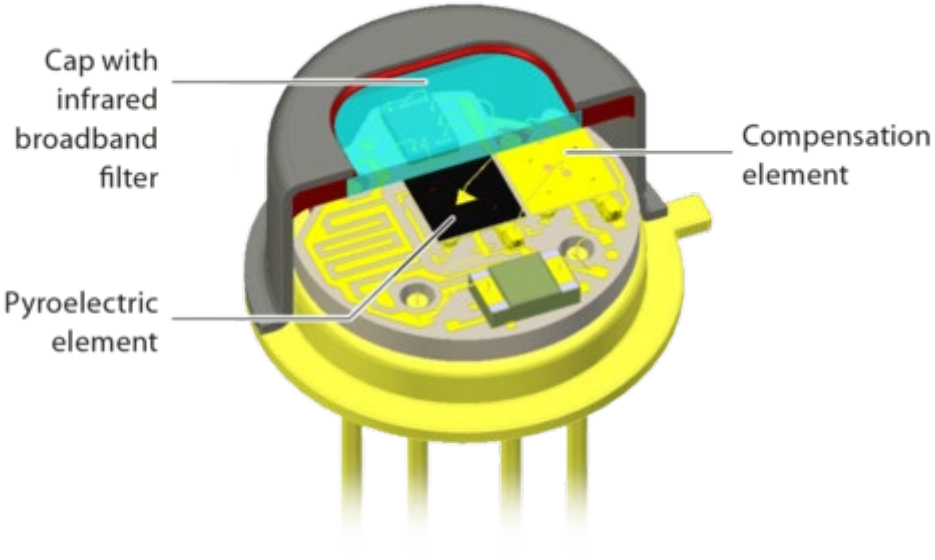
A Pyroelectric detector is an infrared sensitive optoelectronic component which are specifically used for detecting electromagnetic radiation in a wavelength range from 2 to 14 µm.

A receiver chip of a pyroelectric infrared detector manufactured by the sensor division of InfraTec consists of single-crystalline lithium tantalate. Because of its very high curie temperature of 620 °C lithium tantalate guarantees an extremely low temperature coefficient with an excellent long-term stability of the signal voltage.

How Does a Pyroelectric Detector Work?

Pyroelectric crystals have a rare asymmetry due to their single polar axis. This causes their polarisation to change with temperature. This so-called pyroelectric effect is used in sensor technology. For this, a thin pyroelectric crystal is coated perpendicular to the polar axis with electrodes. On the upper electrode of the crystal, an absorbing layer (black layer) is applied. When this layer interacts with infrared radiation, the pyroelectric layer heats up and surface charge arises. If the radiation is switched off, a charge of the opposite polarity originates. However, the charge is very low. Before the finite internal resistance of the crystal can equalise the charges, extremely low-noise and low leakage current field-effect transistors (JFET) or operational amplifier (OpAmp) convert the charges into a signal voltage. Thermopiles, too, belong to the group of thermal detectors, however, the measuring effect is less significant. While pyroelectric infrared detectors show a good

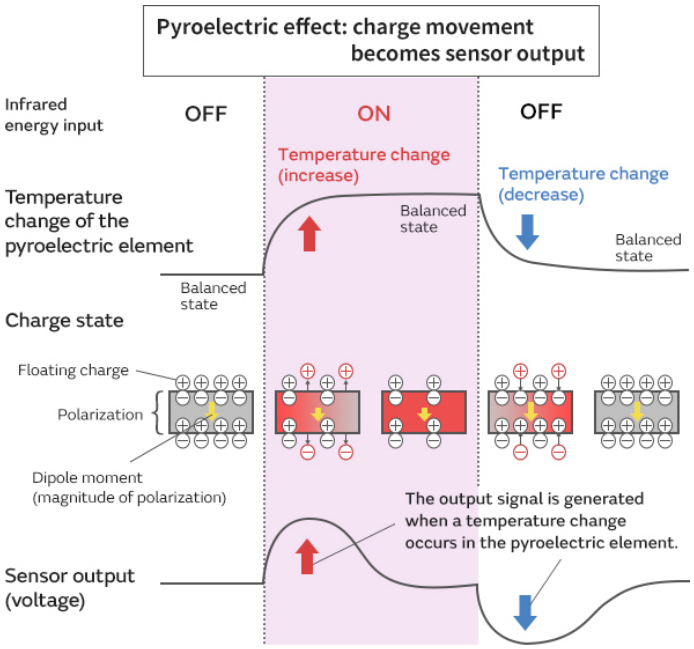
signal/noise ratio up to modulation frequencies of 4 kHz, e.g. in FTIR spectrometers, thermopiles produce good results up to modulation frequencies of specific Hertz only.



A temperature change occurs when the infrared rays enter the sensor, so the surface temperature of the pyroelectric element (ceramic) rises, and a surface charge is generated by the pyroelectric effect.
Therefore, the neutral state of the charge collapses during stability, the sensing element surface charge and the adsorption floating ion charge become unbalanced due to different relaxation times, and an unpaired charge is generated.

This generated surface charge is extracted as an electrical signal by the components inside the sensor and used as an output signal.

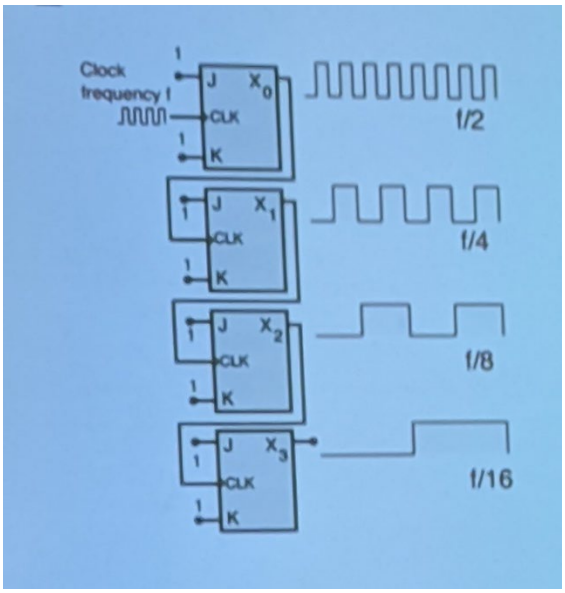
Detection is only possible at the moment when there is a temperature change. Detection cannot be performed when there is no temperature change = no movement.



In our case, we start with twenty nanoseconds on our project having a response in the frequency of 50 Mhz. Our goal is to reach to one second and know how many frequency is required for do this possible, and for know that we can do use of the program “Excel” for evade the situation of use too much time to calculate that thing.

14	655.36E-06	1.526E+03
15	1.311E-03	762.939E+00
16	2.621E-03	381.47E+00
17	5.243E-03	190.735E+00
18	10.486E-03	95.367E+00
19	20.972E-03	47.684E+00
20	41.943E-03	23.842E+00
21	83.886E-03	11.921E+00
22	167.772E-03	5.96E+00
23	335.544E-03	2.98E+00
24	671.089E-03	1.49E+00
25	1.34[illegible]E+00	745.058E-03

By understanding the limitations and possibilities of clock signals in FPGAs, electronic engineers can design efficient and reliable systems that meet the needs of a wide range of applications.



The input is a clock signal of 50 MHz and the output having the result of this.

Like we mention back, the function of this clocks is with flipflops, passing by the signal among them, creating a delay of that and make a visual result more notable for our eyes.

Starting developing our system, we need to describe on our code as always first in the vhd:

```vhdl
--Fermin Covarrubias Ramos
--Ariel Gonzales Diaz

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;


ENTITY PYROSENSOR IS
    PORT(
        clk_50MHz : IN STD_LOGIC;
        clk : OUT STD_LOGIC;
        pyro : IN STD_LOGIC;
        light : OUT STD_LOGIC
        );
    END PYROSENSOR;

ARCHITECTURE Behavioral OF PYROSENSOR IS

        CONSTANT max_count : INTEGER := 24999999;
        SIGNAL counter : INTEGER RANGE 0 TO max_count;
        SIGNAL clk_state : std_logic := '0';

        CONSTANT timeMAX : INTEGER := 15;
        CONSTANT timelight : INTEGER := 5;
        CONSTANT timesb : INTEGER := 10;
        CONSTANT timesi : INTEGER := 1;
        TYPE state IS (reading);
        SIGNAL pr_state, nx_state : state;
        SIGNAL time : INTEGER RANGE 0 TO timeMAX;


BEGIN

    CLOCK_GENERATOR: PROCESS(clk_50MHz, clk_state, counter)
    BEGIN
        IF RISING_EDGE(clk_50MHz) THEN
            IF counter < max_count THEN
                counter <= counter + 1;
            ELSE
                clk_state <= NOT clk_state;
                counter <= 0;
            END IF;
        END IF;
    END PROCESS CLOCK_GENERATOR;

    SECOND_OUT : PROCESS (clk_state)
    BEGIN
        clk <= clk_state;
    END PROCESS SECOND_OUT;

    PROCESS (clk_50MHz, clk_state, counter)
    BEGIN
        light <= '0';
        time <= timesi;
        CASE pr_state IS
            WHEN reading =>
                IF (pyro= '1') THEN
                light <='1';
                time <= timesb;
                nx_state <= reading;
                END IF;
                IF (pyro= '0') THEN
                light <='0';
                nx_state <= reading;
                END IF;


        END CASE;
    END PROCESS;
    END Behavioral;
```

Our code on an .vhd format

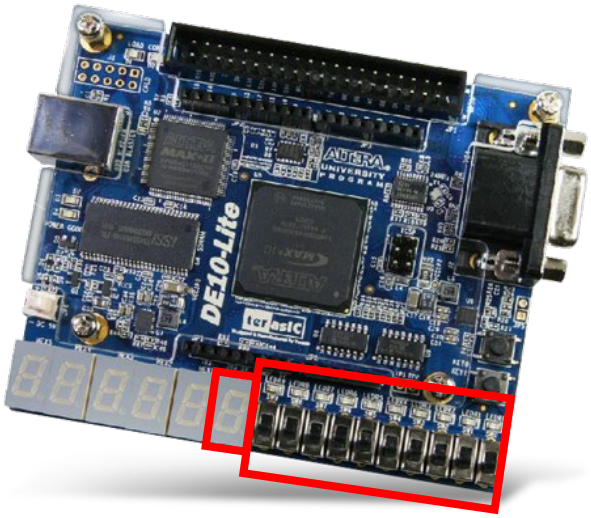
Notable features of this code could be:

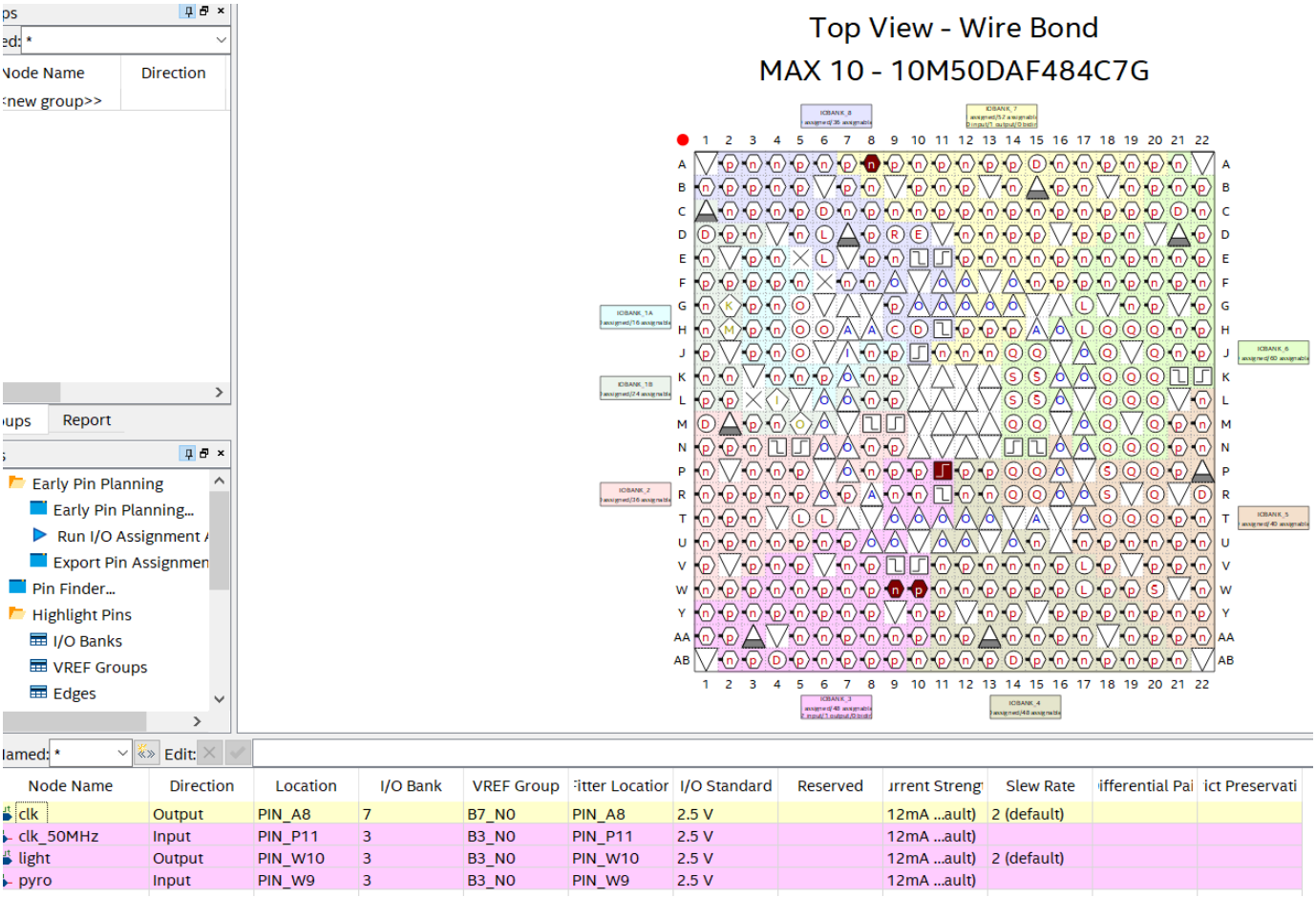
- Declaring of our timer, with the 50 Mhz
- Having diverse entries like for the light and the Pyroelectric Detector
- A counter managing the time of stay in a state of the light

Next to, for having free of errors in our program, after a successfully compilation, we need to generate the test bench for write the possible instances of the code for the FPGA

```
        Command: quartus_eda --read_settings_files=off --write_settings_files=off mux_2to1_bit -c mux_2to1_bit
 18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PAR
204019 Generated file mux_2to1_bit.vho in folder "C:/CMOS_I_DIGITALES/mux_2to1_bit/simulation/modelsim/" for EDA simulation tool
        Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
        ******************************************************************
        Running Quartus Prime EDA Netlist Writer
        Command: quartus_eda --read_settings_files=on --write_settings_files=off mux_2to1_bit -c mux_2to1_bit --gen_testbench
 18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment N
201002 Generated VHDL Test Bench File C:/CMOS_I_DIGITALES/mux_2to1_bit/simulation/modelsim/mux_2to1_bit.vht for simulation
        Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
```

In the final steps we need to declare our ports for see in the board, using the switches for the inputs and now one display to show the value:





This are ports of the expansion header, now using the clock ports for use this feature in our project.

Conclusions.

By combining the Pyroelectric Detector, clock model, and state machine on an FPGA, this project offers an effective solution for human presence detection and response. It showcases the integration of different electronic components and demonstrates the power of programmable logic for implementing complex systems. Additionally, it provides practical applications in areas such as security, automation, and energy management.

Overall, this project highlights the capabilities of the Pyroelectric Detector and FPGA technology, showcasing how they can be leveraged to create an intelligent system that detects human presence and responds with a lighting mechanism.

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