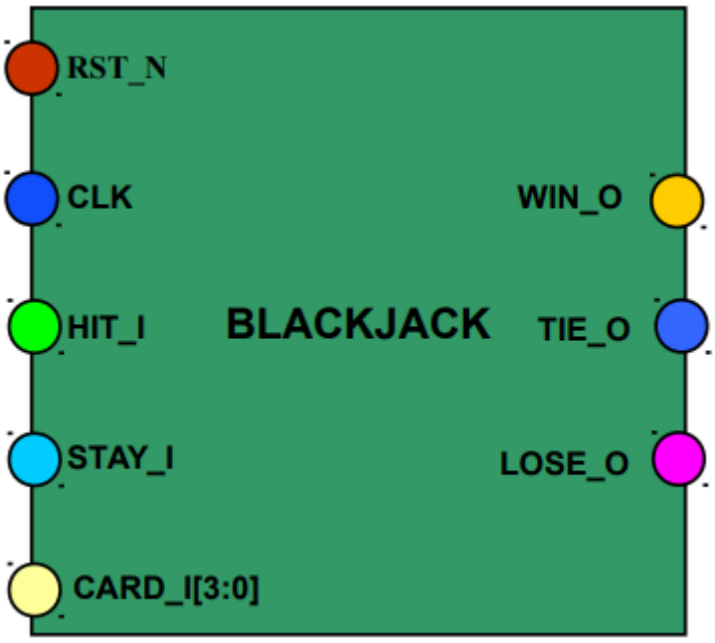
A Verilog block containing the following input and output signals should be developed:



RST_N: When at '0' the block will be reset.
CLK: Block clock.
HIT_I: Sign that will be used when the Player wants to pick up one more card.
STAY_I: Sign that will be used to inform you that the Player no longer wants to pick up cards. Activation of this signal also moves the Dealer.
CARD_I [3: 0]: Bus for the cards considering the following values:
• 1 = A2-2-9 = 2-9
• 10 = 10 • 11 = Jack
• 12 = Lady • 13 = King
• When considering the play (the sum of the cards, the Ace may be worth 1 or 11)
WIN_O: Player won
TIE_O: Draw
LOSE_O: Player lost