Código ejercicios 1 y 2 Lab 04

```verilog
module tabla1(input wire A, B, C, output wire Y);
    assign Y = (~A & ~C) | (A & ~B) | (A & C);
endmodule

module tabla2(input wire A, B, C, output wire Y);
    not (Y, B);
endmodule

module tabla3(input wire A, B, C, D, output wire Y);
    assign Y = (~A & ~B & ~C & ~D) | (~A & ~B & C & D) | (~A & B & ~C & ~D) | (~A & B & ~C & D) | (A & B & ~C & ~D) | (A & B & C & ~D) | (A & ~B & C & D) | (A & ~B & C & ~D);
endmodule

module tabla4(input wire A, B, C, D, output wire Y);
    assign Y = (A & B) | (A & C) | (A & ~D);
endmodule
```

```verilog
module tabla5(input wire A, B, C, D, output wire Y);

  assign Y = (A & ~B) | (A & ~C) | (A & ~D) | (~B & ~C & ~D);

endmodule

module tabla6(input wire A, B, C, output wire Y);

  not(n1, B);
  or (Y, n1, C);

endmodule

module tabla7(input wire A, B, C, D, output wire Y);

  not (n2, C);
  and (n3, n1, D);
  and (n4, A, D);
  or  (Y, B, n3, n4);

endmodule

module tabla8(input wire A, B, C, output wire Y);

  not (n5, A);
  not (n6, C);
  and (n7, n5, n6);
  or  (Y, n7, B);

endmodule
```

Testbench Ejercicio 1 y 2

```verilog
module testbench();

reg p1, p2, p3, p4, p5, p6, p7, p8, p9, p10, p11, p12, p13, p14, p15, p16, p17, p18, p19, p20, p21, p22, p23, p24, p25, p26, p27, p28;
wire s1, s2, s3, s4, s5, s6, s7, s8;

tabla1 t1(p1, p2, p3, s1);
tabla2 t2(p4, p5, p6, s2);
tabla3 t3(p7, p8, p9, p10, s3);
tabla4 t4(p11, p12, p13, p14, s4);
tabla5 t5(p15, p16, p17, p18, s5);
tabla6 t6(p19, p20, p21, s6);
tabla7 t7(p22, p23, p24, p25, s7);
tabla8 t8(p26, p27, p28, s8);
```

```verilog
initial begin

  $display("Ejercicio 1, Tabla 1");
  $display("A B C | Y");
  $monitor("%b %b %b | %b", p1, p2, p3, s1);

     p1 = 0; p2 = 0; p3 = 0;
  #1 p1 = 0; p2 = 0; p3 = 1;
  #1 p1 = 0; p2 = 1; p3 = 0;
  #1 p1 = 0; p2 = 1; p3 = 1;
  #1 p1 = 1; p2 = 0; p3 = 0;
  #1 p1 = 1; p2 = 0; p3 = 1;
  #1 p1 = 1; p2 = 1; p3 = 0;
  #1 p1 = 1; p2 = 1; p3 = 1;

end
```

```verilog
initial begin

  #9

  $display("\n");
  $display("Ejercicio 1, Tabla 2");
  $display("A B C | Y");
  $monitor("%b %b %b | %b", p4, p5, p6, s2);


     p4 = 0; p5 = 0; p6 = 0;
  #1 p4 = 0; p5 = 0; p6 = 1;
  #1 p4 = 0; p5 = 1; p6 = 0;
  #1 p4 = 0; p5 = 1; p6 = 1;
  #1 p4 = 1; p5 = 0; p6 = 0;
  #1 p4 = 1; p5 = 0; p6 = 1;
  #1 p4 = 1; p5 = 1; p6 = 0;
  #1 p4 = 1; p5 = 1; p6 = 1;

end
```

```verilog
initial begin

  #35

  $display("\n");
  $display("Ejercicio 1, Tabla 4");
  $display("A B C D | Y");
  $monitor("%b %b %b %b | %b", p11, p12, p13, p14, s4);


     p11 = 0; p12 = 0; p13 = 0; p14 = 0;
  #1 p11 = 0; p12 = 0; p13 = 0; p14 = 1;
  #1 p11 = 0; p12 = 0; p13 = 1; p14 = 0;
  #1 p11 = 0; p12 = 0; p13 = 1; p14 = 1;
  #1 p11 = 0; p12 = 1; p13 = 0; p14 = 0;
  #1 p11 = 0; p12 = 1; p13 = 0; p14 = 1;
  #1 p11 = 0; p12 = 1; p13 = 1; p14 = 0;
  #1 p11 = 0; p12 = 1; p13 = 1; p14 = 1;
  #1 p11 = 1; p12 = 0; p13 = 0; p14 = 0;
  #1 p11 = 1; p12 = 0; p13 = 0; p14 = 1;
  #1 p11 = 1; p12 = 0; p13 = 1; p14 = 0;
  #1 p11 = 1; p12 = 0; p13 = 1; p14 = 1;
  #1 p11 = 1; p12 = 1; p13 = 0; p14 = 0;
  #1 p11 = 1; p12 = 1; p13 = 0; p14 = 1;
  #1 p11 = 1; p12 = 1; p13 = 1; p14 = 0;
  #1 p11 = 1; p12 = 1; p13 = 1; p14 = 1;

end
```

```verilog
initial begin

  #18

  $display("\n");
  $display("Ejercicio 1, Tabla 3");
  $display("A B C D | Y");
  $monitor("%b %b %b %b | %b", p7, p8, p9, p10, s3);


     p7 = 0; p8 = 0; p9 = 0; p10 = 0;
  #1 p7 = 0; p8 = 0; p9 = 0; p10 = 1;
  #1 p7 = 0; p8 = 0; p9 = 1; p10 = 0;
  #1 p7 = 0; p8 = 0; p9 = 1; p10 = 1;
  #1 p7 = 0; p8 = 1; p9 = 0; p10 = 0;
  #1 p7 = 0; p8 = 1; p9 = 0; p10 = 1;
  #1 p7 = 0; p8 = 1; p9 = 1; p10 = 0;
  #1 p7 = 0; p8 = 1; p9 = 1; p10 = 1;
  #1 p7 = 1; p8 = 0; p9 = 0; p10 = 0;
  #1 p7 = 1; p8 = 0; p9 = 0; p10 = 1;
  #1 p7 = 1; p8 = 0; p9 = 1; p10 = 0;
  #1 p7 = 1; p8 = 0; p9 = 1; p10 = 1;
  #1 p7 = 1; p8 = 1; p9 = 0; p10 = 0;
  #1 p7 = 1; p8 = 1; p9 = 0; p10 = 1;
  #1 p7 = 1; p8 = 1; p9 = 1; p10 = 0;
  #1 p7 = 1; p8 = 1; p9 = 1; p10 = 1;

end
```

```verilog
initial begin

  #52

  $display("\n");
  $display("Ejercicio 2, Tabla 1");
  $display("A B C D | Y");
  $monitor("%b %b %b %b | %b", p15, p16, p17, p18, s5);


     p15 = 0; p16 = 0; p17 = 0; p18 = 0;
  #1 p15 = 0; p16 = 0; p17 = 0; p18 = 1;
  #1 p15 = 0; p16 = 0; p17 = 1; p18 = 0;
  #1 p15 = 0; p16 = 0; p17 = 1; p18 = 1;
  #1 p15 = 0; p16 = 1; p17 = 0; p18 = 0;
  #1 p15 = 0; p16 = 1; p17 = 0; p18 = 1;
  #1 p15 = 0; p16 = 1; p17 = 1; p18 = 0;
  #1 p15 = 0; p16 = 1; p17 = 1; p18 = 1;
  #1 p15 = 1; p16 = 0; p17 = 0; p18 = 0;
  #1 p15 = 1; p16 = 0; p17 = 0; p18 = 1;
  #1 p15 = 1; p16 = 0; p17 = 1; p18 = 0;
  #1 p15 = 1; p16 = 0; p17 = 1; p18 = 1;
  #1 p15 = 1; p16 = 1; p17 = 0; p18 = 0;
  #1 p15 = 1; p16 = 1; p17 = 0; p18 = 1;
  #1 p15 = 1; p16 = 1; p17 = 1; p18 = 0;
  #1 p15 = 1; p16 = 1; p17 = 1; p18 = 1;

end
```

```
initial begin

  #69

  $display("\n");
  $display("Ejercicio 2, Tabla 2");
  $display("A B C | Y");
  $monitor("%b %b %b | %b", p19, p20, p21, s6);


     p19 = 0; p20 = 0; p21 = 0;
  #1 p19 = 0; p20 = 0; p21 = 1;
  #1 p19 = 0; p20 = 1; p21 = 0;
  #1 p19 = 0; p20 = 1; p21 = 1;
  #1 p19 = 1; p20 = 0; p21 = 0;
  #1 p19 = 1; p20 = 0; p21 = 1;
  #1 p19 = 1; p20 = 1; p21 = 0;
  #1 p19 = 1; p20 = 1; p21 = 1;

end
```

```verilog
initial begin

  #78

  $display("\n");
  $display("Ejercicio 2, Tabla 3");
  $display("A B C D | Y");
  $monitor("%b %b %b %b | %b", p22, p23, p24, p25, s7);

     p22 = 0; p23 = 0; p24 = 0; p25 = 0;
  #1 p22 = 0; p23 = 0; p24 = 0; p25 = 1;
  #1 p22 = 0; p23 = 0; p24 = 1; p25 = 0;
  #1 p22 = 0; p23 = 0; p24 = 1; p25 = 1;
  #1 p22 = 0; p23 = 1; p24 = 0; p25 = 0;
  #1 p22 = 0; p23 = 1; p24 = 0; p25 = 1;
  #1 p22 = 0; p23 = 1; p24 = 1; p25 = 0;
  #1 p22 = 0; p23 = 1; p24 = 1; p25 = 1;
  #1 p22 = 1; p23 = 0; p24 = 0; p25 = 0;
  #1 p22 = 1; p23 = 0; p24 = 0; p25 = 1;
  #1 p22 = 1; p23 = 0; p24 = 1; p25 = 0;
  #1 p22 = 1; p23 = 0; p24 = 1; p25 = 1;
  #1 p22 = 1; p23 = 1; p24 = 0; p25 = 0;
  #1 p22 = 1; p23 = 1; p24 = 0; p25 = 1;
  #1 p22 = 1; p23 = 1; p24 = 1; p25 = 0;
  #1 p22 = 1; p23 = 1; p24 = 1; p25 = 1;

end
```

```verilog
  initial begin

    #95

    $display("\n");
    $display("Ejercicio 2, Tabla 4");
    $display("A B C | Y");
    $monitor("%b %b %b | %b", p26, p27, p28, s8);

       p26 = 0; p27 = 0; p28 = 0;
    #1 p26 = 0; p27 = 0; p28 = 1;
    #1 p26 = 0; p27 = 1; p28 = 0;
    #1 p26 = 0; p27 = 1; p28 = 1;
    #1 p26 = 1; p27 = 0; p28 = 0;
    #1 p26 = 1; p27 = 0; p28 = 1;
    #1 p26 = 1; p27 = 1; p28 = 0;
    #1 p26 = 1; p27 = 1; p28 = 1;

  end

  initial
  #105 $finish;

  initial begin

    $dumpfile("Lab4_tb.vcd");
    $dumpvars(0, testbench);

  end

endmodule
```

Código Ejercicio 5

```verilog
module alarmakarnough(input wire A, B, C, output wire Y);

  not (n1, A);
  and (n2, n1, C);
  and (n3, B, C);
  or  (Y, n2, n3);

endmodule

module alarmaPOS(input wire A, B, C, output wire Y);

  assign Y = (A | B | C) & (A | ~B | C) & (~A | B | C) & (~A | B | ~C) & (~A | ~B | C);

endmodule

module alarmaSOP(input wire A, B, C, output wire Y);

  assign Y = (~A & ~B & C) | (~A & B & C) | (A & B & C);

endmodule
```

Testbench ejercicio 5

```verilog
module testbench();

  reg p1, p2, p3, p4, p5, p6, p7, p8, p9;
  wire s1, s2, s3;

  alarmakarnough a1(p1, p2, p3, s1);
  alarmaPOS a2(p4, p5, p6, s2);
  alarmaSOP a3(p7, p8, p9, s3);


  initial begin

    $display("Ejercicio 5 Mapa de Karnough");
    $display("A B C | Y");
    $monitor("%b %b %b  | %b", p1, p2, p3, s1);


        p1 = 0; p2 = 0; p3 = 0;
    #1 p1 = 0; p2 = 0; p3 = 1;
    #1 p1 = 0; p2 = 1; p3 = 0;
    #1 p1 = 0; p2 = 1; p3 = 1;
    #1 p1 = 1; p2 = 0; p3 = 0;
    #1 p1 = 1; p2 = 0; p3 = 1;
    #1 p1 = 1; p2 = 1; p3 = 0;
    #1 p1 = 1; p2 = 1; p3 = 1;

  end
```

```verilog
initial begin

  #9

  $display("\n");
  $display("Ejercicio 5 POS");
  $display("A B C | Y");
  $monitor("%b %b %b  | %b", p4, p5, p6, s2);


     p4 = 0; p5 = 0; p6 = 0;
  #1 p4 = 0; p5 = 0; p6 = 1;
  #1 p4 = 0; p5 = 1; p6 = 0;
  #1 p4 = 0; p5 = 1; p6 = 1;
  #1 p4 = 1; p5 = 0; p6 = 0;
  #1 p4 = 1; p5 = 0; p6 = 1;
  #1 p4 = 1; p5 = 1; p6 = 0;
  #1 p4 = 1; p5 = 1; p6 = 1;

end
```

```verilog
    initial begin

      #18

      $display("\n");
      $display("Ejercicio 5 SOP");
      $display("A B C | Y");
      $monitor("%b %b %b   | %b", p7, p8, p9, s3);

         p7 = 0; p8 = 0; p9 = 0;
      #1 p7 = 0; p8 = 0; p9 = 1;
      #1 p7 = 0; p8 = 1; p9 = 0;
      #1 p7 = 0; p8 = 1; p9 = 1;
      #1 p7 = 1; p8 = 0; p9 = 0;
      #1 p7 = 1; p8 = 0; p9 = 1;
      #1 p7 = 1; p8 = 1; p9 = 0;
      #1 p7 = 1; p8 = 1; p9 = 1;

    end

    initial

      #27 $finish;

    initial begin

      $dumpfile("Alarma_tb.vcd");
      $dumpvars(0, testbench);

    end

endmodule
```