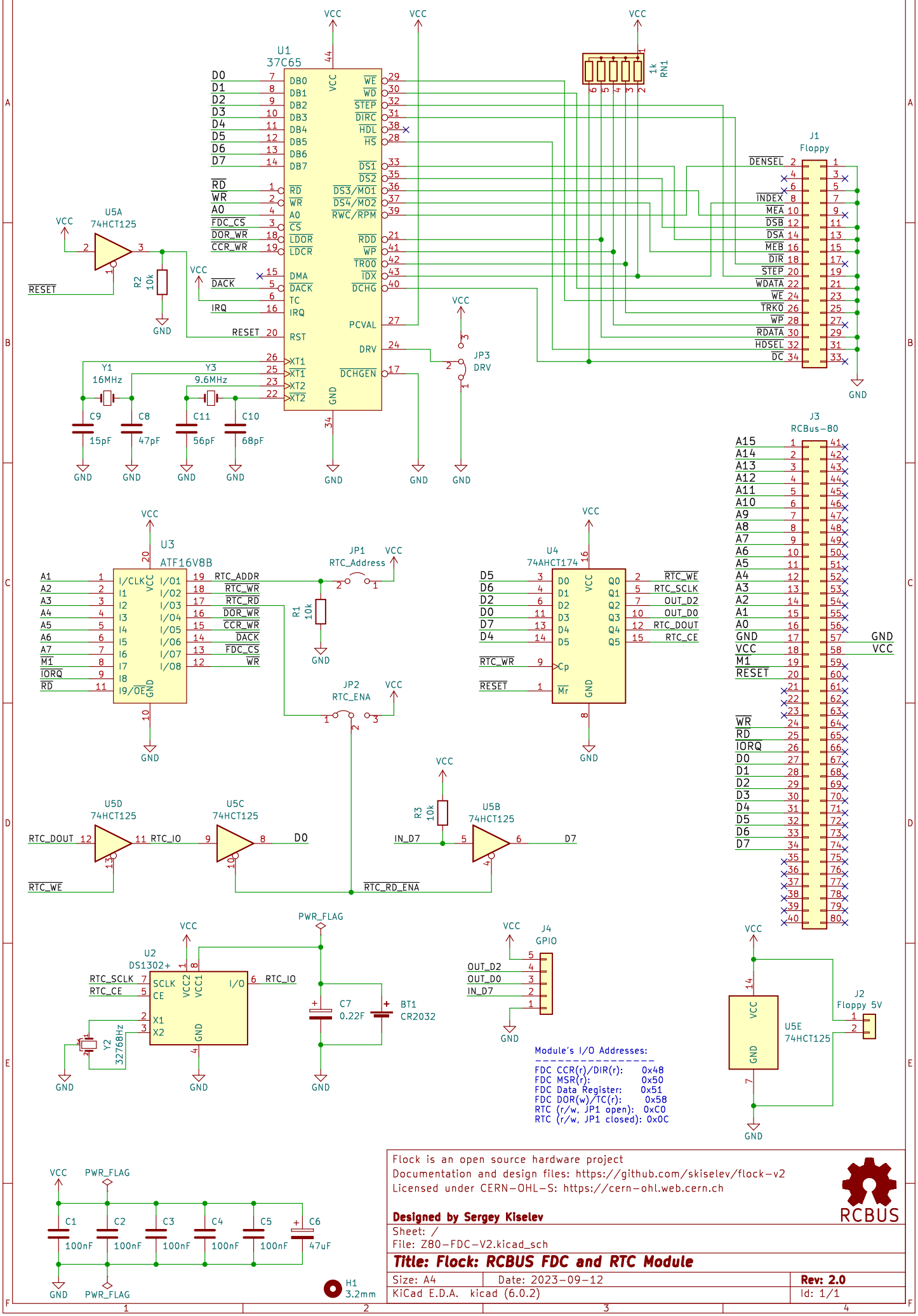
U1
37C65
U5A
74HCT125
RESET
R2
10k
Y1
16MHz
Y3
9.6MHz
C9
15pF
C8
47pF
C11
56pF
C10
68pF
JP3
DRV
1k
RN1
J1
Floppy
J3
RCBus-80
U3
ATF16V8B
JP1
RTC_Address
R1
10k
JP2
RTC_ENA
U4
74AHCT174
U5D
74HCT125
U5C
74HCT125
R3
10k
U5B
74HCT125
U2
DS1302+
Y2
32768Hz
C7
0.22F
BT1
CR2032
J4
GPIO
U5E
74HCT125
J2
Floppy 5V
Module's I/O Addresses:
FDC CCR(r)/DIR(r): 0x48
FDC MSR(r): 0x50
FDC Data Register: 0x51
FDC DOR(w)/TC(r): 0x58
RTC (r/w, JP1 open): 0xC0
RTC (r/w, JP1 closed): 0x0C
C1
100nF
C2
100nF
C3
100nF
C4
100nF
C5
100nF
C6
47uF
H1
3.2mm
Flock is an open source hardware project
Documentation and design files: https://github.com/skiselev/flock-v2
Licensed under CERN-OHL-S: https://cern-ohl.web.cern.ch
Designed by Sergey Kiselev
RCBUS
Sheet: /
File: Z80-FDC-V2.kicad_sch
Title: Flock: RCBUS FDC and RTC Module
Size: A4
Date: 2023-09-12
Rev: 2.0
KiCad E.D.A. kicad (6.0.2)
Id: 1/1