

**DEPARTMENT OF COMPUTER  
SCIENCE & ENGINEERING**  
College of Engineering



# **Remote Embedded Systems Lab (RESL)**



**Discovery Park**

3940 N. Elm, Room F201  
Denton, TX 76207-7102



## Introduction

Most of the computer engineering classes have a lab component attached to the class. These labs provide hands-on exposure on how to design a system for an application or to solve a problem. These labs are mostly done on general purpose embedded system based boards (Example: Tiva C Launch Pad and MKII Booster Pack). Since these classes have a hands-on component, many students from Electrical Engineering (EE), Computer Science (CS), and Computer Engineering (CE) fields are interested to learn more about embedded system design. As a result there is a 20% increase in class enrollments every time the class is offered at UNT. This increase in enrollment requires more resources (computers and boards) to teach these classes. In order to meet the demands of growing classes, buying more computers and boards is not a great way to scale.

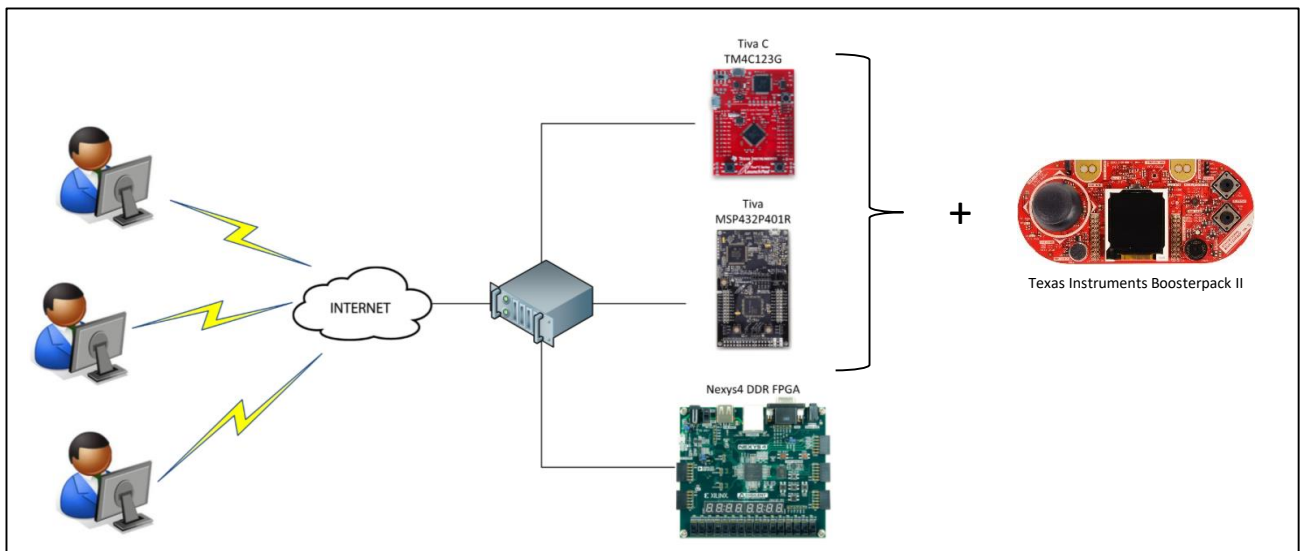


Figure 1: Overall Diagram of the Remote Embedded Systems Lab

The Remote Embedded Systems Lab (RESL) is a development environment for embedded systems. This lab is remotely accessible through a web browser, and allows users to upload compiled code to an embedded systems board, and to monitor the board's outputs by camera, microphone, and serial port. The user is capable of interacting with the target board, to activate sensors and buttons, through the web interface. The Remote Embedded Systems Lab also features an extensive database, permitting the management of boards, users, permissions, and statistics of usage. This lab also provides a web-based method of developing application using embedded systems, which opens paths to distance education as well as helping to reduce the required number of workstations and boards in traditional Labs.

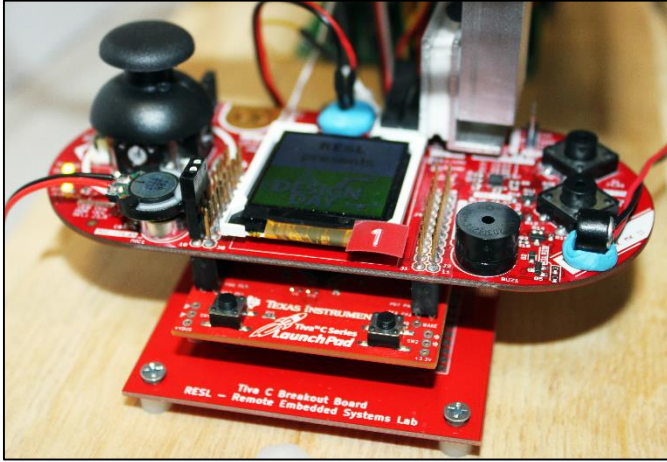


Figure 2: Tiva C with BoosterPack

## Main Characteristics

- Multi-board
- Multi-user
- Responsive in **real-time**
- Ideal for long distance education
- Allows the sharing of expensive boards in traditional labs or large organizations

## User Interaction

- Watch the LCD screen and LED of Booster Pack II through the video streaming in **real time**.
- Listen the Booster Pack II's Buzzer through the audio streaming.
- Press 2 buttons, and reset button.
- Set the external LED's brightness connected to the board's ambient light sensor.
- Set temperature to board's temperature sensor.
- Set voltage to board's ADC.
- Upload and flash the board with examples or the user's own binary code.
- Generate a sine tone and play it to the board's microphone.
- Select mp3 sound examples or send a user's mp3 sound file, for playback to the board's microphone.
- Record sound with the user's microphone and play it to the board's microphone.

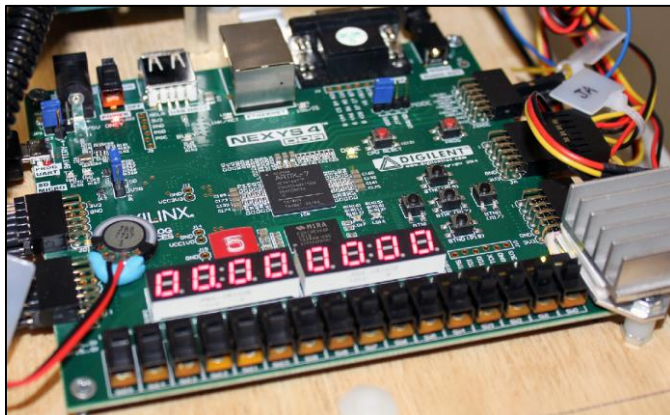


Figure 3: Nexys 4 DDR FPGA Board



Figure 4: MSP432 with BoosterPack II

## Menu Board Options

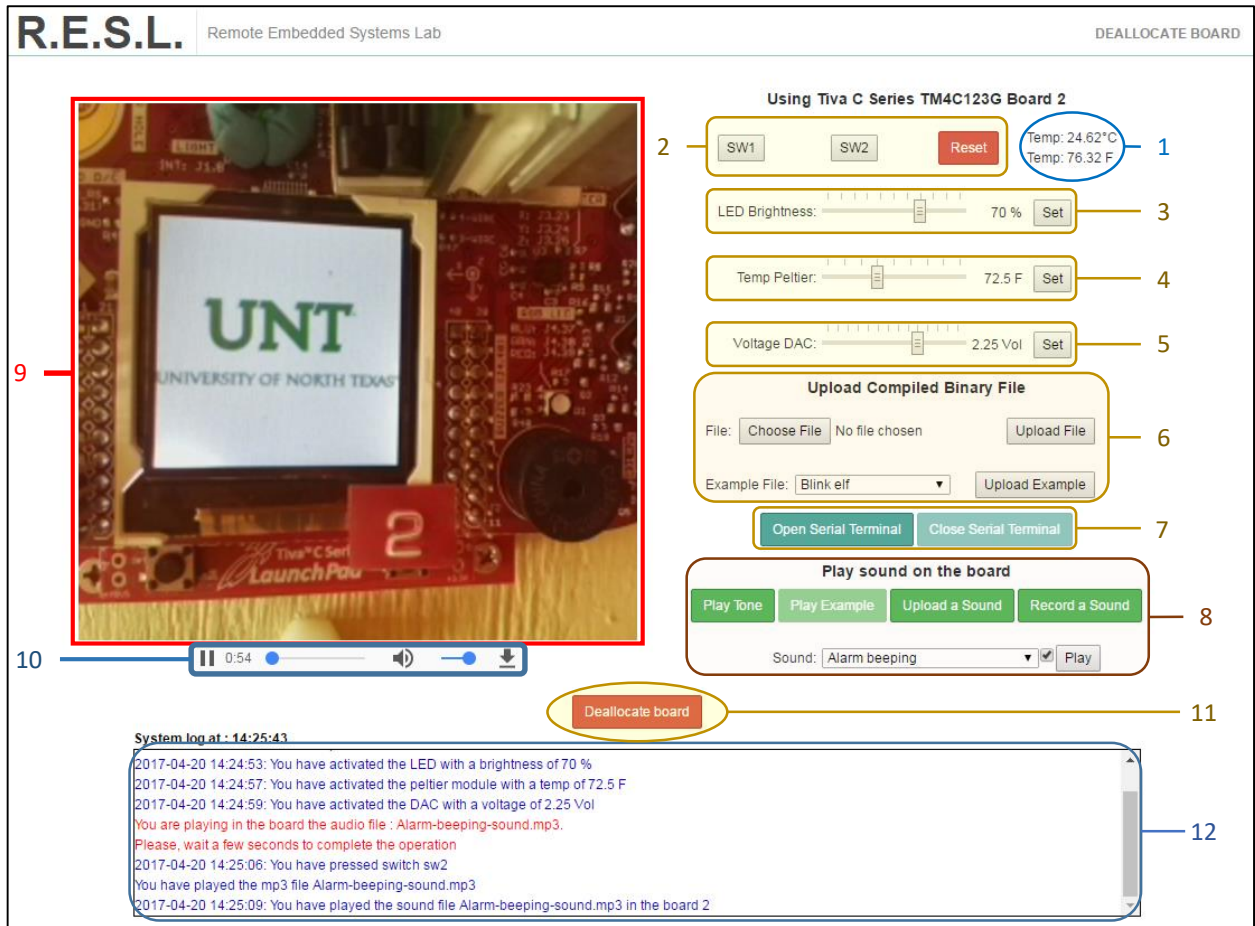


Figure 5: Menu Board Options

1. Show the temperature of the temperature sensor
2. Switches buttons and Reset button
3. Set the LED brightness (0 to 100%)
4. Set the temperature (65-85 F)
5. Set the voltage of the DAC (0 to 3 V)
6. Upload binary code (user and example code)
7. Open - close serial terminal windows
8. Play sound on the board options
9. Show video streaming
10. Control volume of audio Streaming
11. Deallocate board button
12. System log to show every action



## Menu Board Options

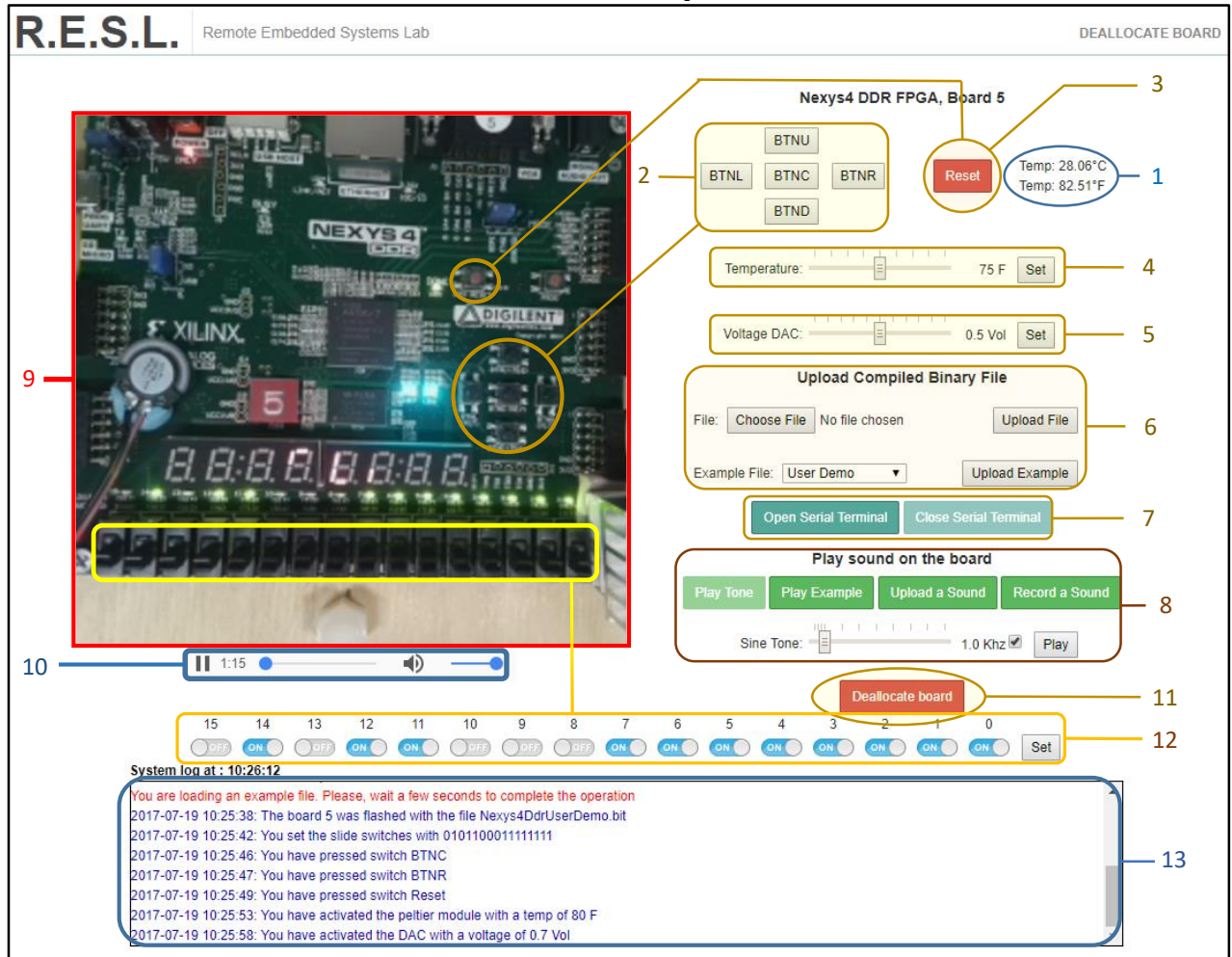


Figure 6: Menu Board Options

1. Show the temperature of the temperature sensor
2. 5 Switches buttons
3. Reset button
4. Set the temperature (65-85 F)
5. Set the voltage of the DAC (0 to 1 V)
6. Upload bitstream code (user and example code)
7. Open - close serial terminal windows
8. Play sound on the board options
9. Show video streaming
10. Control volume of audio Streaming
11. Deallocate board button
12. 16 slides switches
13. System log to show every action

### Friendly Interface

- Boards Reservation selection
- Connection list (by board, time interval, EUID)
- Boards Monitor in **real time**
- User list
- Course List
- Server Settings

### Board Reservation

This page is automatically updated every 10 seconds

Please, select one of the available boards.

Board ID	Board Model	Select
1	Tiva C Series TM4C123G	1
2	Tiva C Series TM4C123G	2
3	Tiva C Series TM4C123G	3
4	MSP432P401R	4
5	Nexys4 DDR FPGA	5

Boards available : 5

Figure 7: Board Reservation

### Connection list

Board: All Boards Initial Date: 01/01/2017 Final date: 05/26/2017

Course: All Courses EUID: All EUID Submit

Number of connections found: 4110  
Showing page 1 of 17 registers by page  
Showing 1 of 242

Total Connections : 4110  
Total Time : 129:53:54  
Total Up Files : 1652

Connection ID	Board ID	Course	EUID	Initial Time	Final Time	Total Time	Uploaded Files	IP
4672	4	CSCE3730.001	fm0105	2017-05-26 08:38:34	2017-05-26 08:39:13	00:00:39	0	129.120.59.87
4671	2	CSCE3612.001	fm0000	2017-05-26 08:37:59	2017-05-26 08:39:03	00:01:04	0	129.120.59.87
4670	5	CSCE3730.001	fm0105	2017-05-25 12:23:24	2017-05-25 12:24:19	00:00:55	0	129.120.59.87
4669	4	CSCE3730.001	fm0105	2017-05-25 12:23:19	2017-05-25 12:23:22	00:00:03	0	129.120.59.87
4668	2	CSCE3730.001	fm0105	2017-05-25 12:23:14	2017-05-25 12:23:16	00:00:02	0	129.120.59.87
4667	1	CSCE3730.001	fm0105	2017-05-25 12:23:08	2017-05-25 12:23:10	00:00:02	0	129.120.59.87
4666	3	CSCE3730.001	fm0105	2017-05-25 12:23:02	2017-05-25 12:23:05	00:00:03	0	129.120.59.87
4665	3	CSCE3730.001	fm0105	2017-05-24 11:06:19	2017-05-24 11:08:42	00:02:23	4	129.120.59.87
4664	2	CSCE3730.001	fm0105	2017-05-24 11:04:48	2017-05-24 11:06:11	00:01:23	0	129.120.59.87
4663	5	CSCE3730.001	fm0105	2017-05-23 12:43:52	2017-05-23 12:44:06	00:00:14	0	129.120.59.87
4662	4	CSCE3730.001	fm0105	2017-05-23 10:32:55	2017-05-23 10:34:05	00:01:10	0	129.120.59.87
4661	2	CSCE3730.001	fm0105	2017-05-23 09:41:47	2017-05-23 09:41:50	00:00:03	0	129.120.59.87
4660	1	CSCE3730.001	fm0105	2017-05-23 09:41:13	2017-05-23 09:41:44	00:00:31	2	129.120.59.87
4659	5	CSCE3730.001	fm0105	2017-05-22 17:45:35	2017-05-22 17:47:11	00:01:36	0	172.20.4.108
4658	4	CSCE3730.001	fm0105	2017-05-22 17:43:27	2017-05-22 17:45:30	00:02:03	0	172.20.4.108
4657	1	CSCE3730.001	fm0105	2017-05-22 14:05:05	2017-05-22 14:05:16	00:00:11	0	172.20.4.53
4656	1	CSCE3730.001	fm0105	2017-05-20 22:07:49	2017-05-20 22:08:10	00:00:21	0	172.20.3.63

Download CSV File  
Go to Main Page

Figure 8: Connection list

### Board list configuration and Monitorization

This page is automatically updated every 5 seconds

Board ID	Video port	Audio port	Active	Board Model	EUID	Con. ID	Start time	In use time
1	8085	8095	<input checked="" type="checkbox"/>	Tiva C Series TM4C123G				
2	8081	8091	<input checked="" type="checkbox"/>	Tiva C Series TM4C123G	fm0000	4671	2017-05-26 08:37:59	00:00:40
3	8082	8092	<input checked="" type="checkbox"/>	Tiva C Series TM4C123G				
4	8083	8093	<input checked="" type="checkbox"/>	MSP432P401R	fm0105	4672	2017-05-26 08:38:34	00:00:11
5	8084	8094	<input checked="" type="checkbox"/>	Nexys4 DDR FPGA				

Active Boards: 5

Figure 9: Board list and Monitor

### General Settings

Configuration

Server IP Address:

Update Ping Value:  seconds

Logout time:  minutes

Max time of use:  minutes

Refresh Reservation Page:  seconds

Refresh Monitorization Page:  seconds

Automatic Free Boards:  seconds

User List Pagination Size:

Course List Pagination Size:

File List Pagination Size:

Connection List Pagination Size:

Max. Upload Files:

Tiva C Initial File:

MSP432 Initial File:

Nexys4 Initial File:

Update Values

Figure 10: General Settings

### Course list

Search course:  Search

Number of courses found: 4

Course ID	Name	Description	Active	Tiva C	MSP432	FPGA	Enrolled	Connections	Time	Uploaded Files
1	CSCE3612.001	Embedded Systems Design	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	4	1012	37:48:20	474
2	CSCE3730.001	Reconfigurable Logic	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	2	3066	89:46:40	1361
11	TEST01.001	This is a test course	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	2	25	01:29:29	11
12	ADMIN	Course for admin	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	1	8	00:49:25	6

Go to Main Page

Figure 11: Course list

### User list

Course: CSCE3612.001  Send

Search user:  Search

Number of users found: 4

User ID	EUID	Active	Role	Last Name	First Name	Course	Last Connection	Total Connections	Total Time	Uploaded Files
9	fm0000	<input checked="" type="checkbox"/>	Instructor	Mosquera	Fernando	CSCE3612.001	2017-05-26 08:37:59	61	01:07:10	19
12	plm0002	<input checked="" type="checkbox"/>	Administrator	Ogunrinde	Peter	CSCE3612.001	2017-05-05 15:20:45	206	08:16:07	106
13	jma0315	<input checked="" type="checkbox"/>	Administrator	Auringer	Johnathan	CSCE3612.001	2017-05-18 23:30:51	745	28:25:03	349
14	gpo109	<input checked="" type="checkbox"/>	Administrator	Poththuparambil	Rubin	CSCE3612.001	0000-00-00 00:00:00	0	00:00:00	0

Go to Main Page

Figure 12: User list

## Complete Connections Statistics Information

- Boards Statistics
- Overall course/student statistics
- Daily reservation counts by moth
- Hourly reservation counts for each day of the week.
- Bar chart daily counts
- Bar chart hourly counts

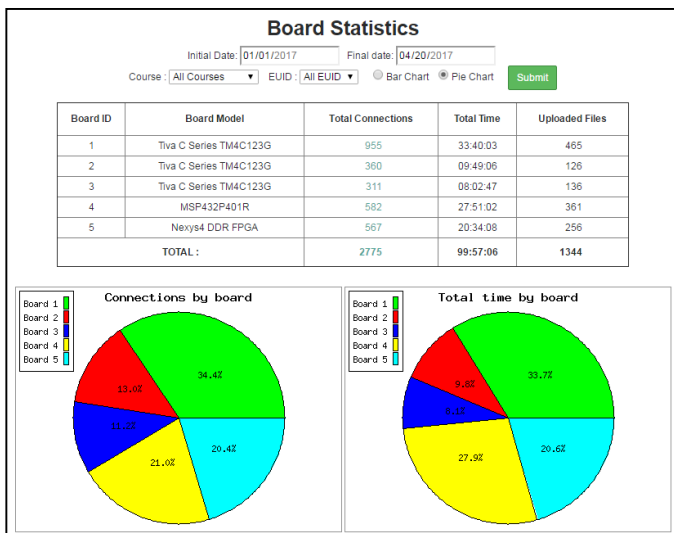


Figure 13: Board Statistics

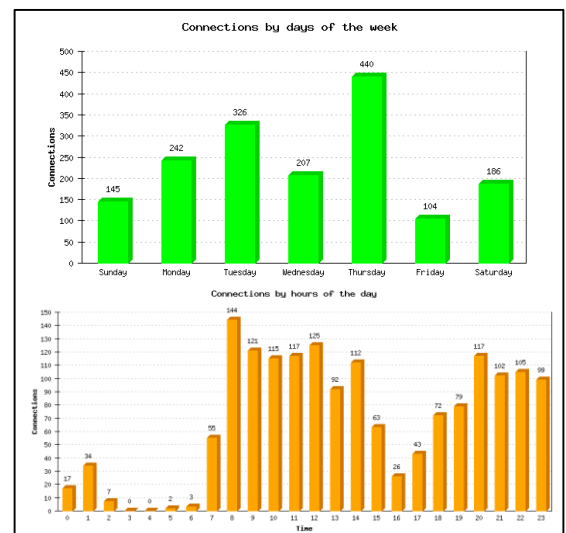


Figure 14: Bar Chart Statistics

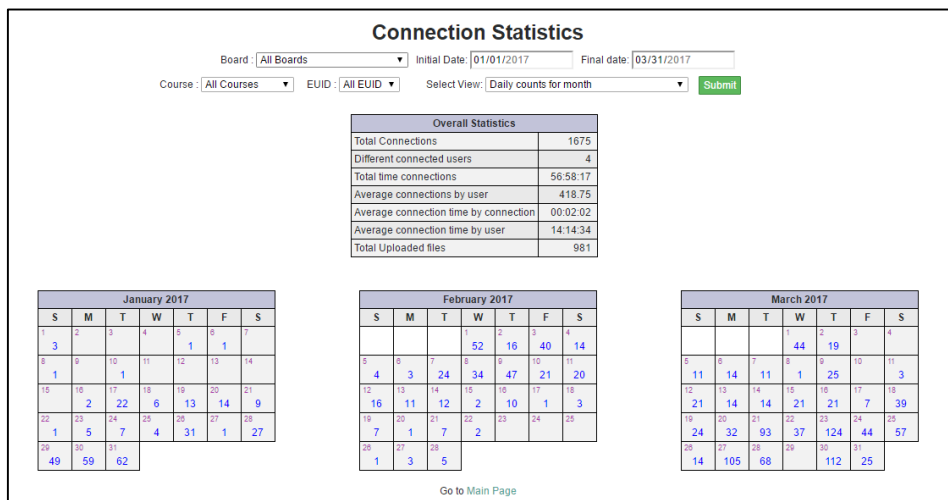


Figure 15: Connection Statistics



## Remote Embedded Systems Lab

### Team: Embedded Systems Online



Fernando Mosquera  
Software and Back-End



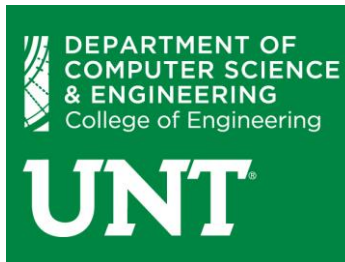
Johnathan Auringer  
Hardware and Firmware



Peter Ogunrinde  
Hardware and Front-End

Advisor: Dr. Robin J. Pottathuparambil

### Senior Design Project



#### Discovery Park

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