UNT UNIVERSITY OF NORTH TEXAS®

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
College of Engineering

E-Learn 2018
World Conference on E-Learning

10/16/2018

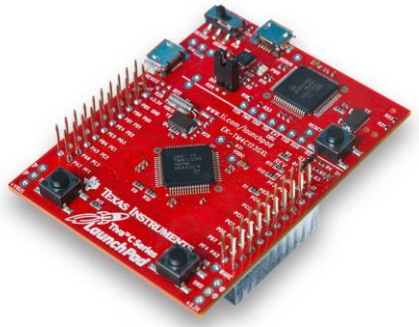
RESL: A Web Browser Based Remote Embedded System Laboratory

Fernando Mosquera
FernandoMosquera@my.unt.edu

Dr. Robin J. Pottathuparambil
robin.pottathuparambil@unt.edu

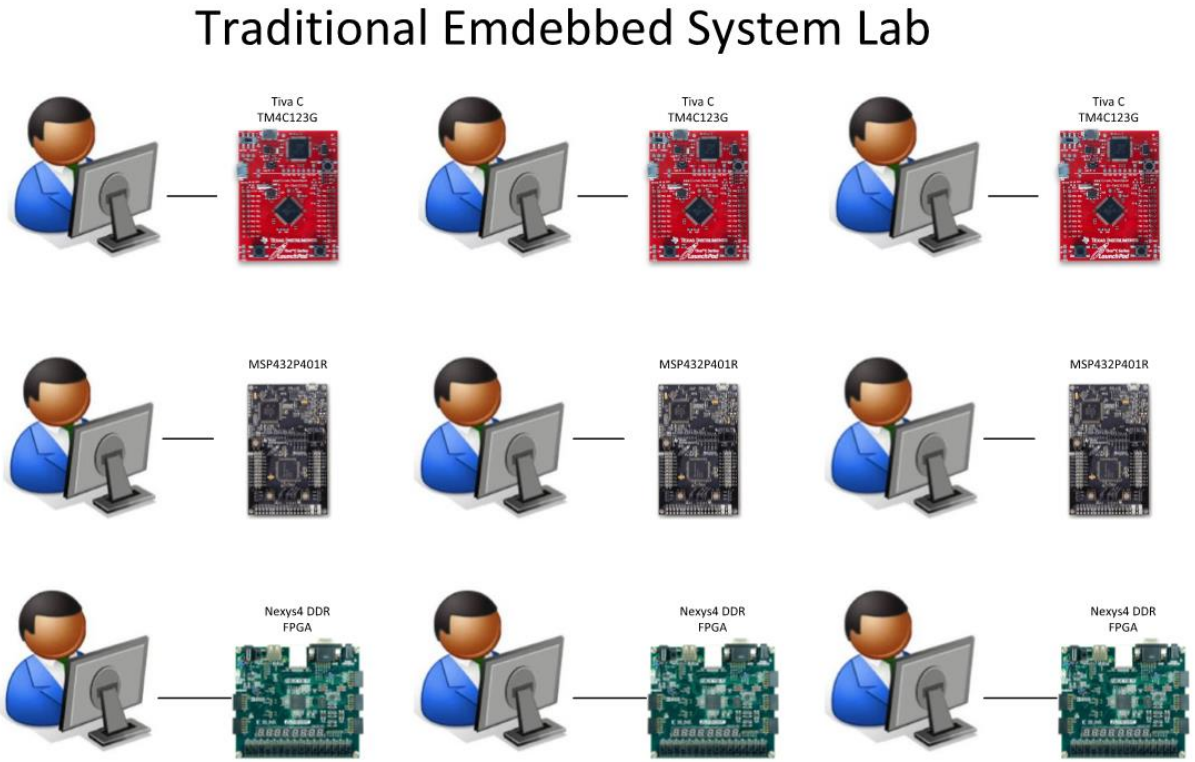
Introduction

- Increasing enrollment of students requires more resources.
- The computer engineering labs are becoming more crowded.
- Labs typically include:
  - Workstation
  - Desk and chair
  - Embedded system board
- How can we expand the labs?
- Adding more workstations is not the best solution!

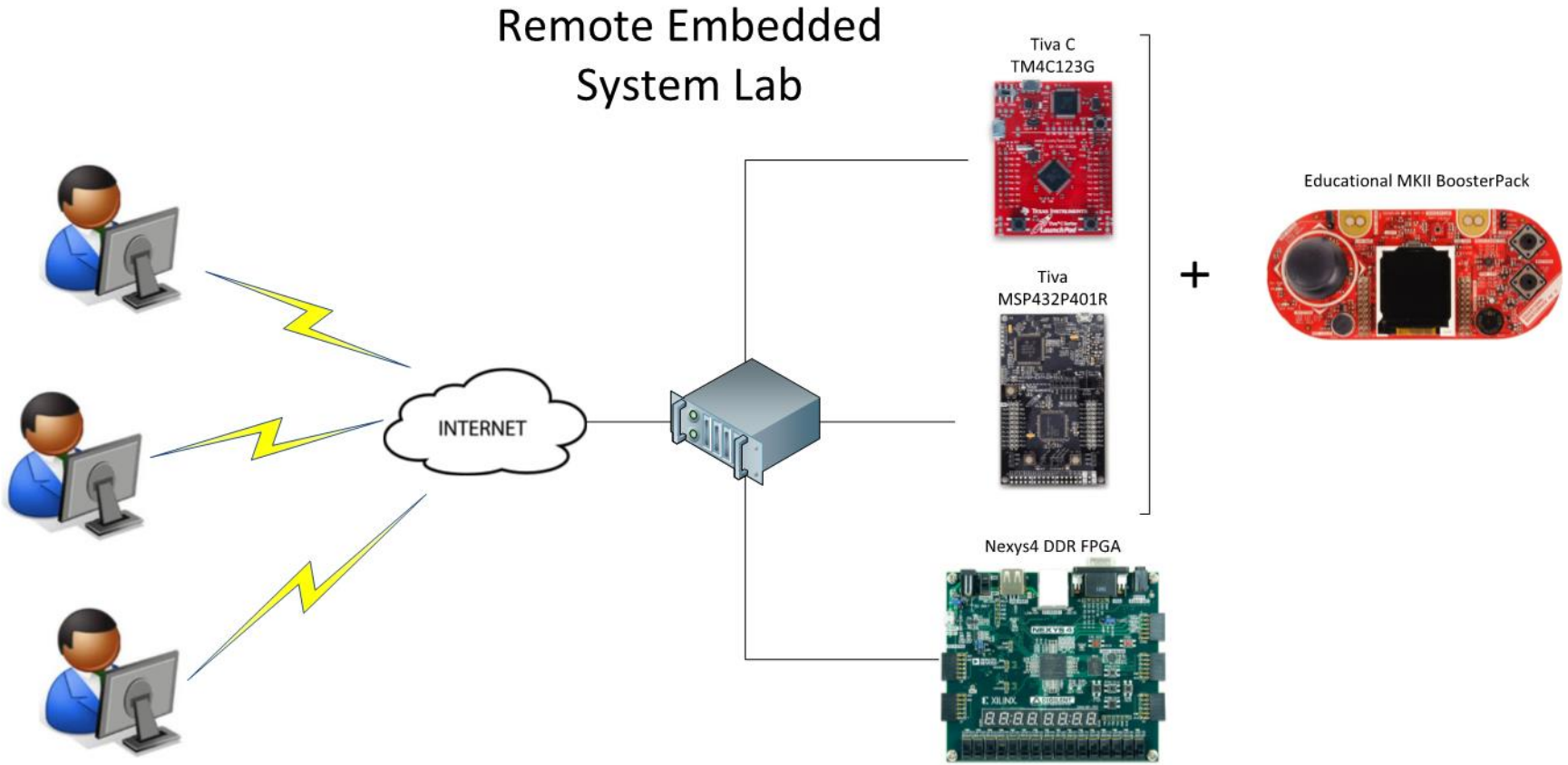


Tiva C

Introduction



Our solution



Our solution

- A remote lab, accessible through web interface.
- All boards connected to the central server.
- The boards can be used, like one is there in person.
  - User can program the boards, control inputs, and monitor outputs.
- Available 24/7.

How to program the boards

C
C++

Code Composer Studio

Energia

Texas Instruments

Verilog

VHDL
Very High Speed Integrated Circuit Hardware Description Language

VIVADO

XILINX

QUARTUS II

*

intel ALTERA

LATTICE DIAMOND DESIGN SOFTWARE

icestudio

*

LATTICE SEMICONDUCTOR

* Boards that will be included in RESL

Board introduction: Arduino

Arduino Uno R3

ATmega328P

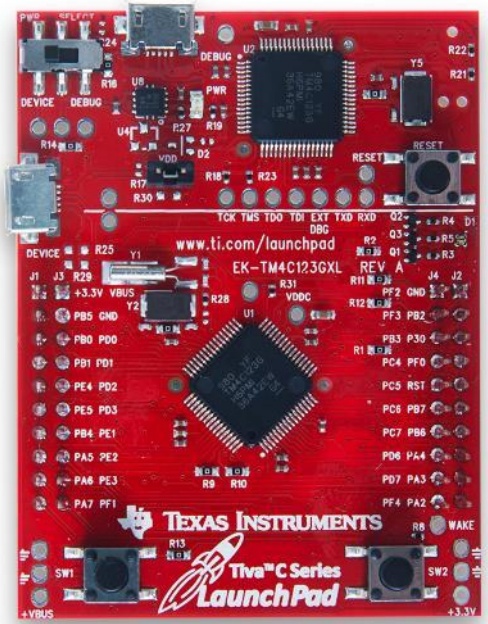
ARDUINO

It is a reference board

NOT included in RESL

Tiva C & MSP432

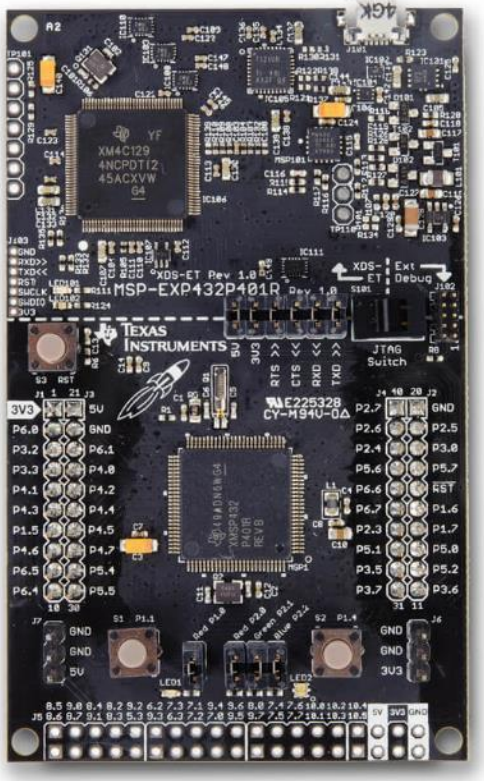
TEXAS INSTRUMENTS



Tiva C

ARM Cortex-M4F

Code Composer Studio

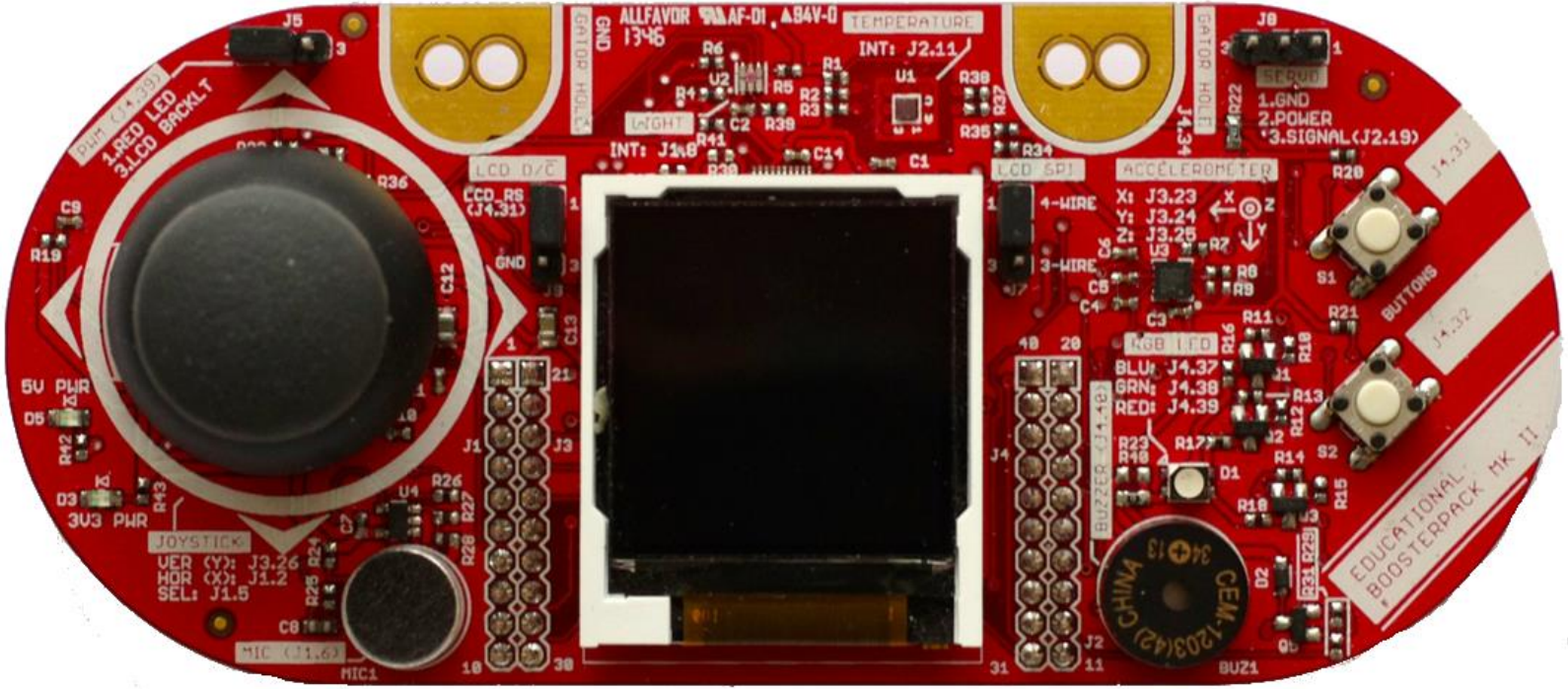


MSP432

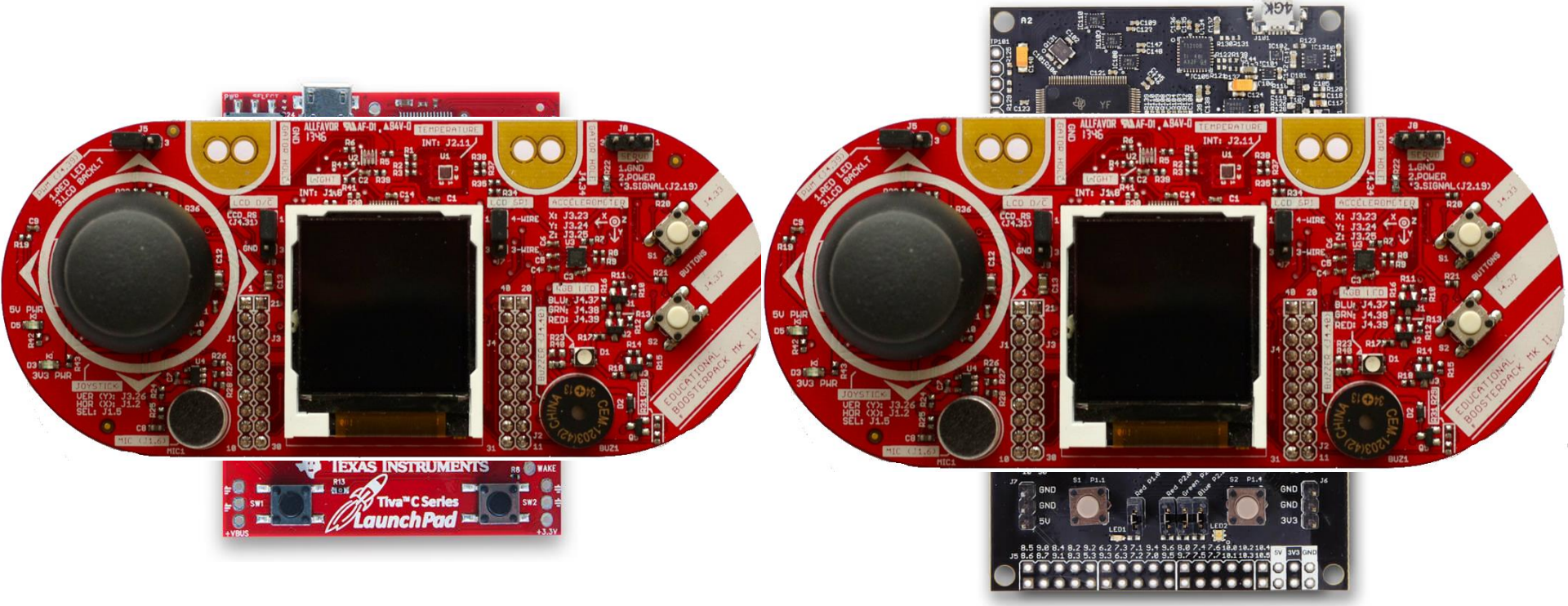
ARM Cortex-M4F

Energīa

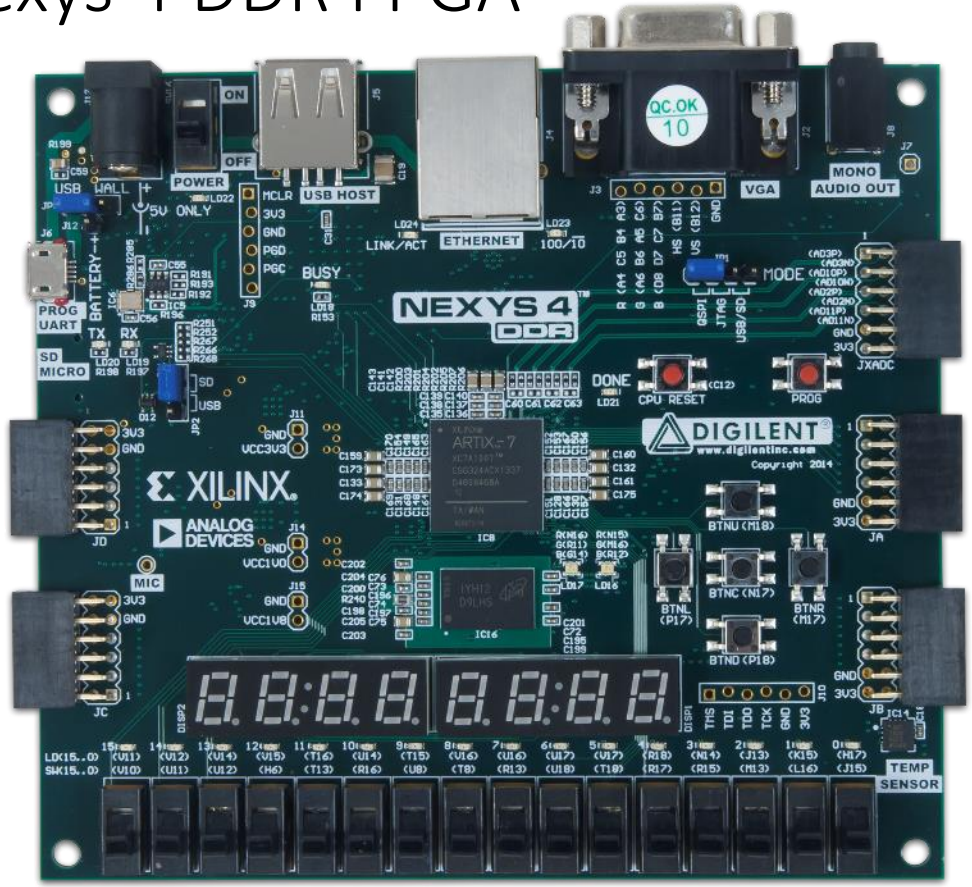
Educational BoosterPack MKII



Boards + BoosterPack MKII



Nexys 4 DDR FPGA



Nexys 4 DDR FPGA

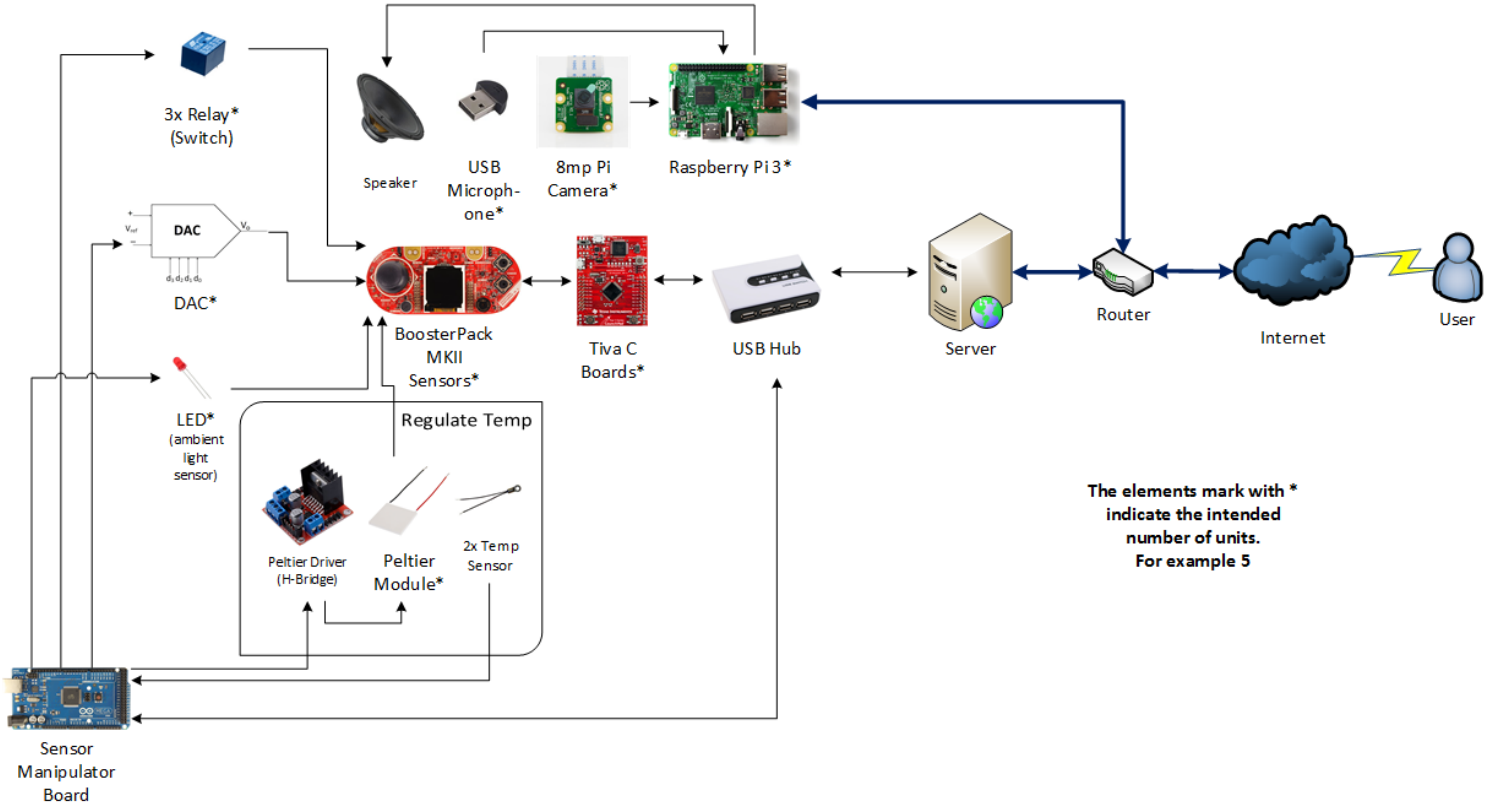
XC7A100T-1CSG324C of Xilinx

XILINX®

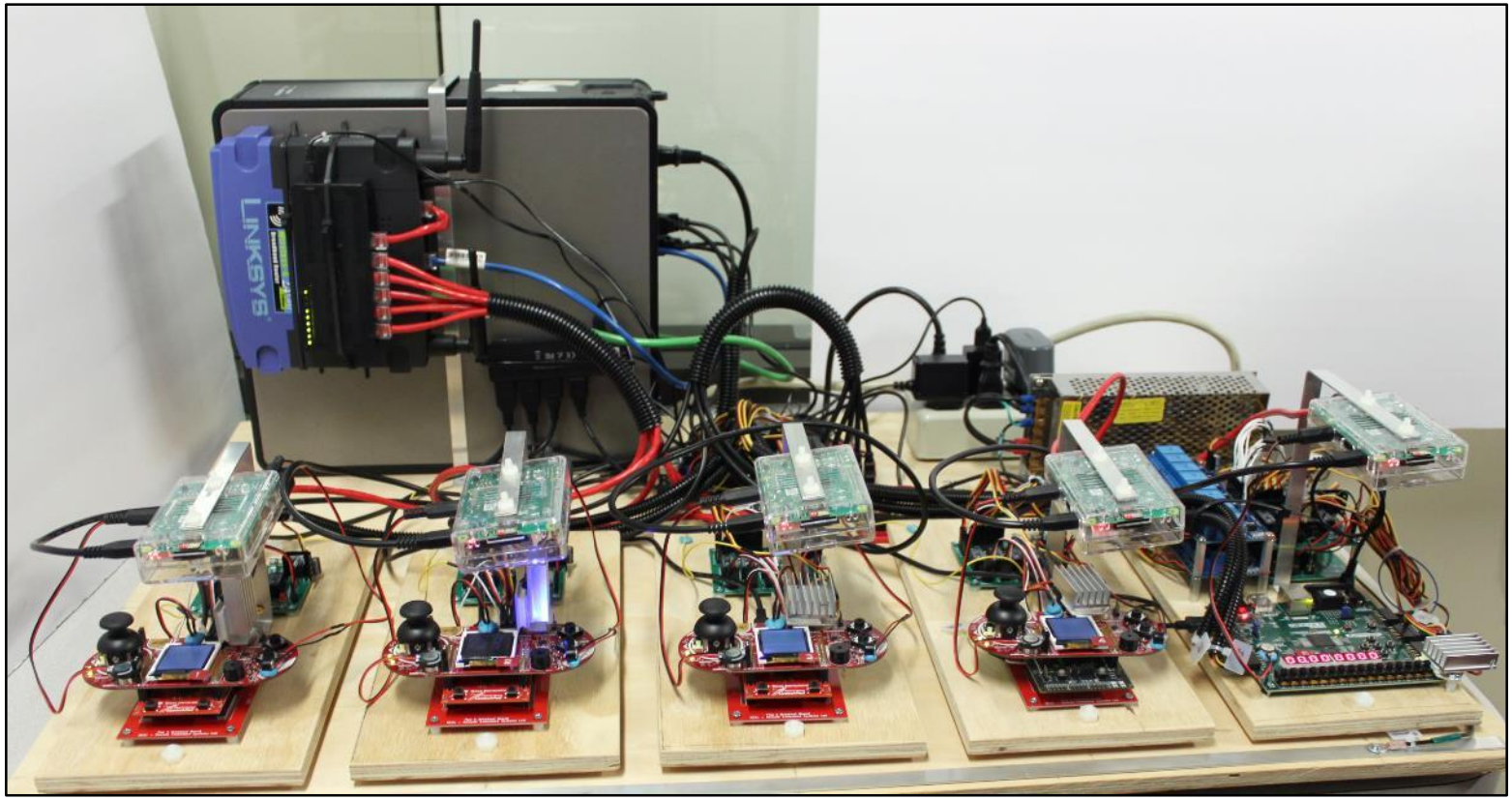
DIGILENT®
A National Instruments Company

VIVADO™

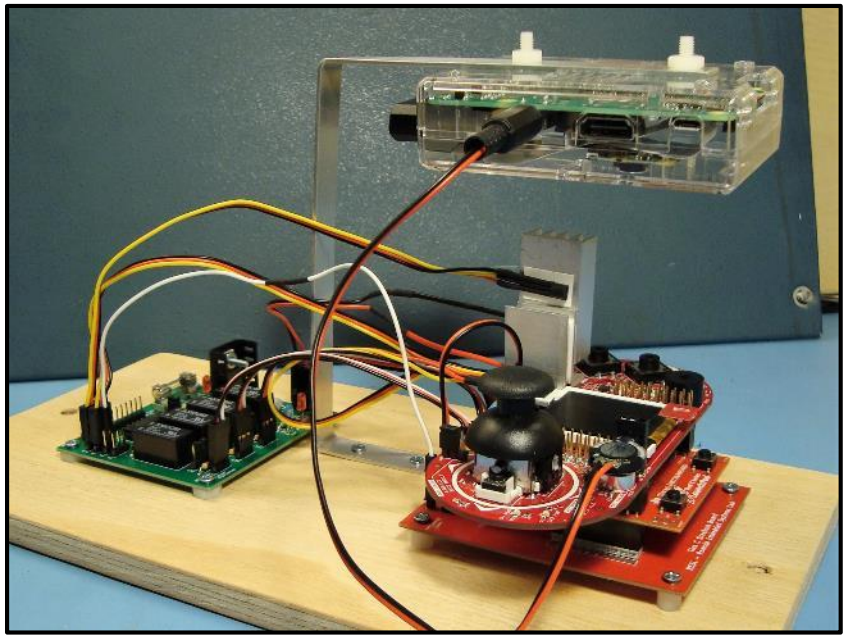
Design


3x Relay*
(Switch)
Speaker
USB
Microph-
one*
8mp Pi
Camera*
Raspberry Pi 3*
DAC
DAC*
BoosterPack
MKII
Sensors*
Tiva C
Boards*
USB Hub
Server
Router
Internet
User
LED*
(ambient
light
sensor)
Regulate Temp
Peltier Driver
(H-Bridge)
Peltier
Module*
2x Temp
Sensor
Sensor
Manipulator
Board
The elements mark with *
indicate the intended
number of units.
For example 5

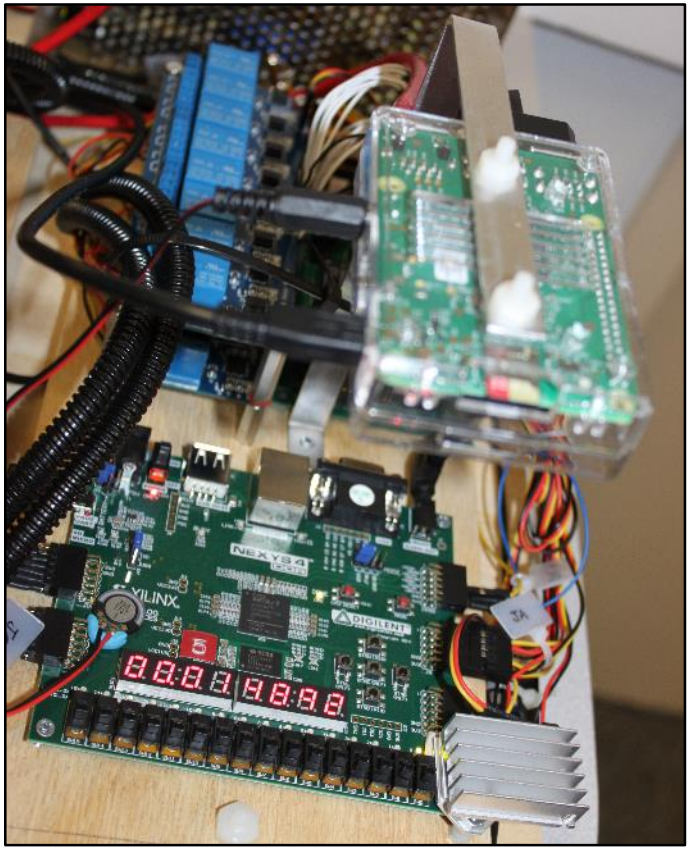
Implementation

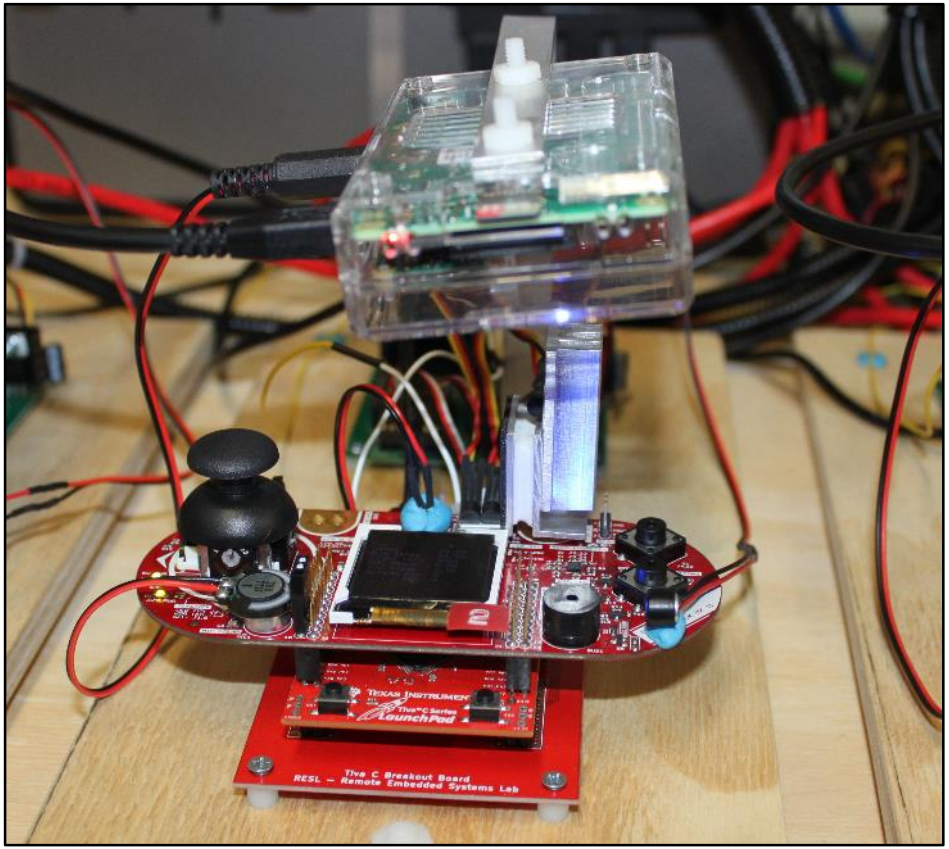


Implementation

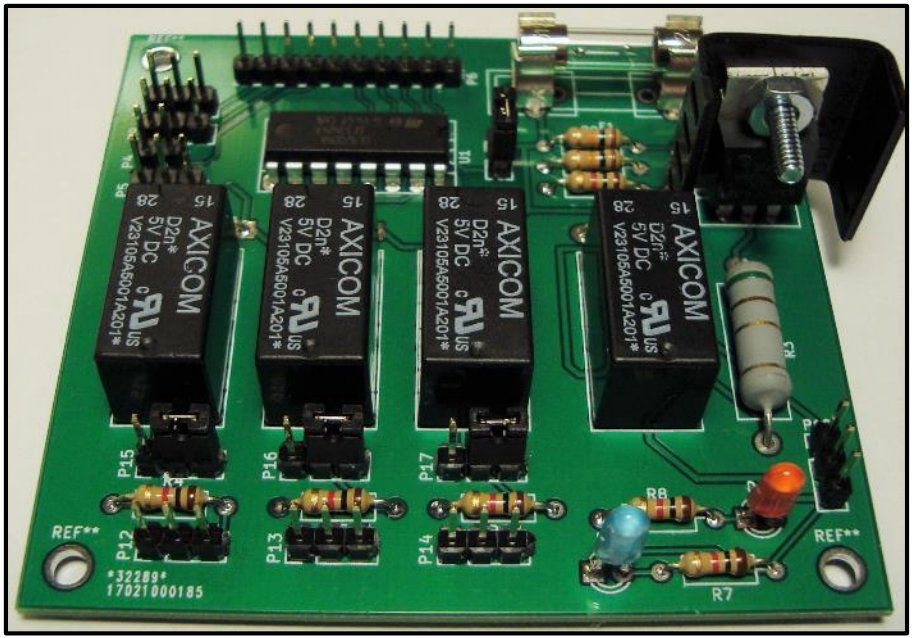


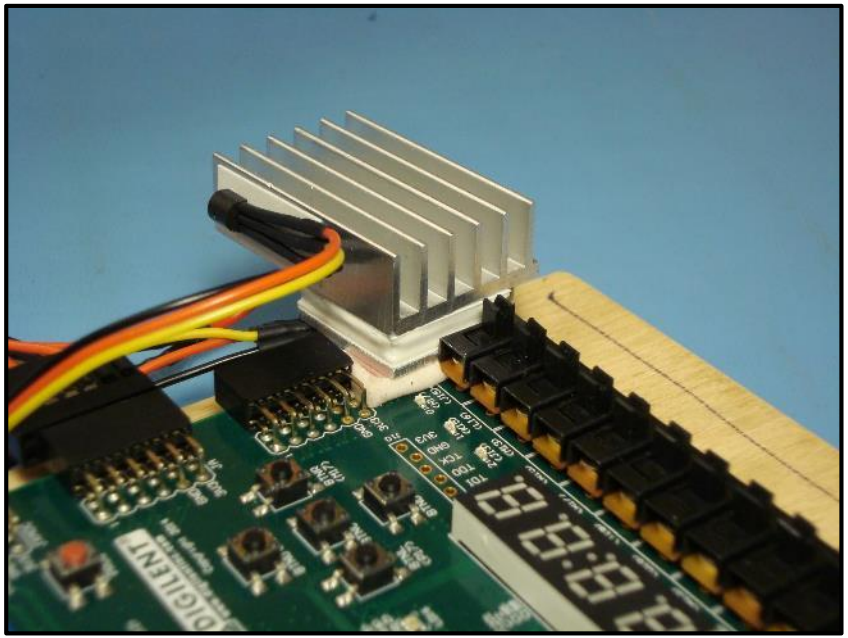
Implementation





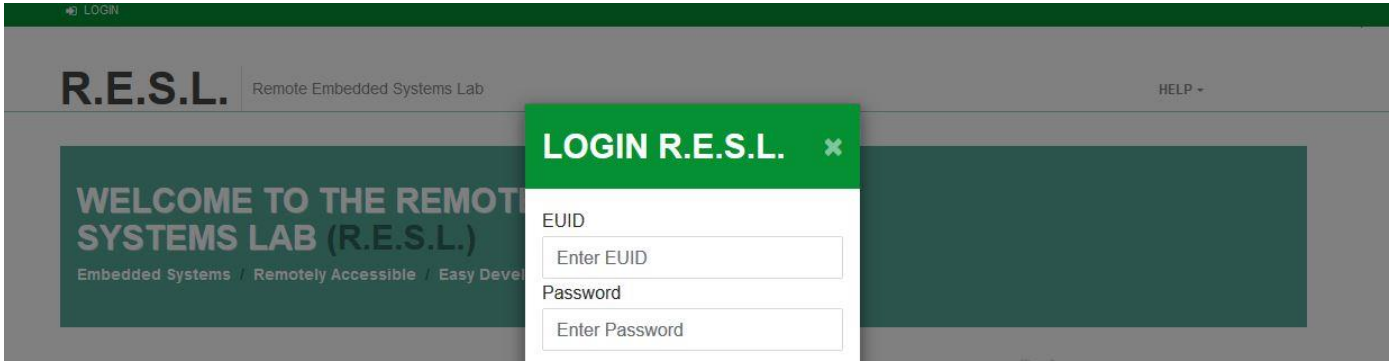
Implementation



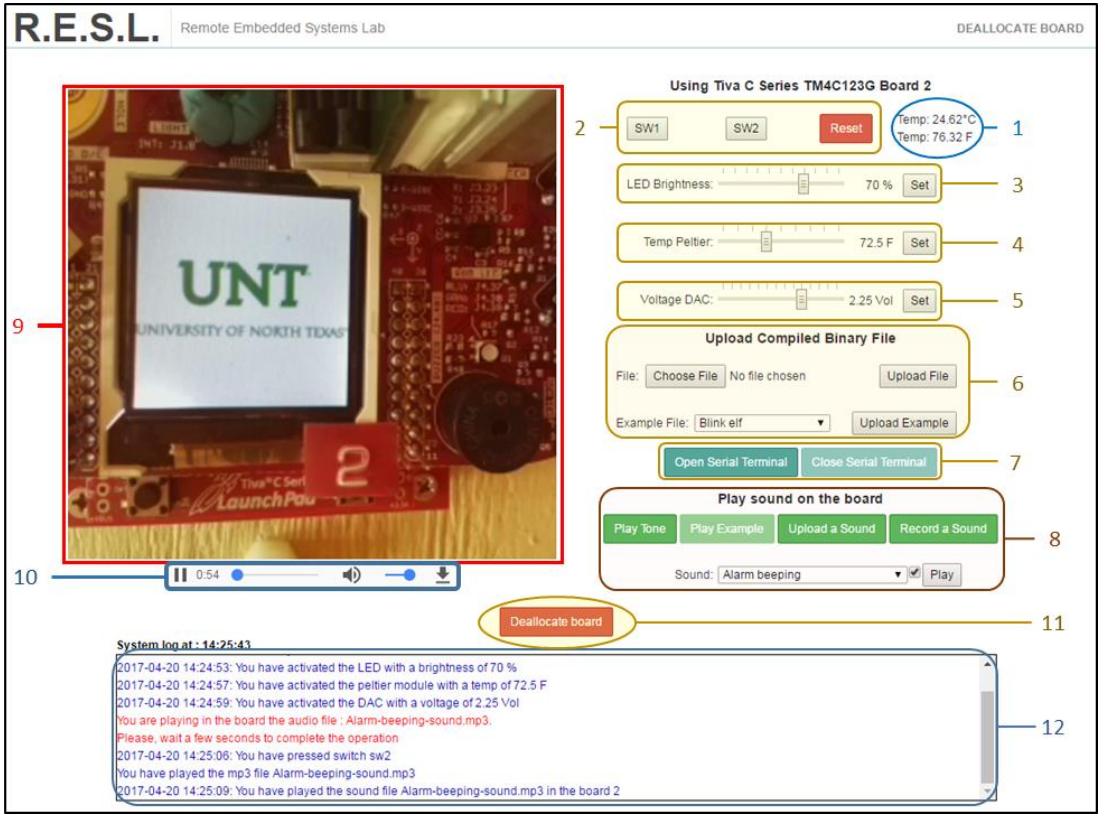


Implementation

- Linux Ubuntu 16.04.1 LTS 64 bits
- Web server Nginx + PHP 7.0 + MariaDB
- Web programed in AJAX
- Bootstrap with Jquery
- Apache2 + php in Raspberry Pi
- FFmpeg server + uv4l in Raspberry Pi

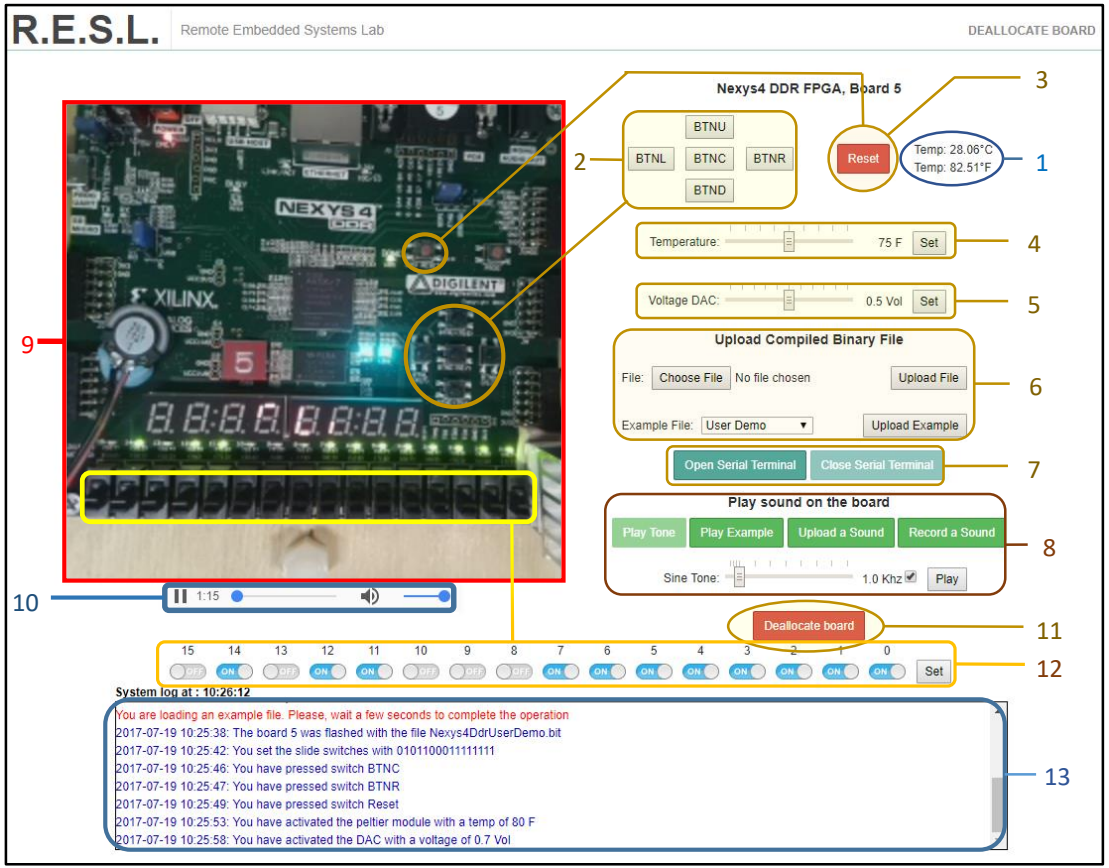


Results



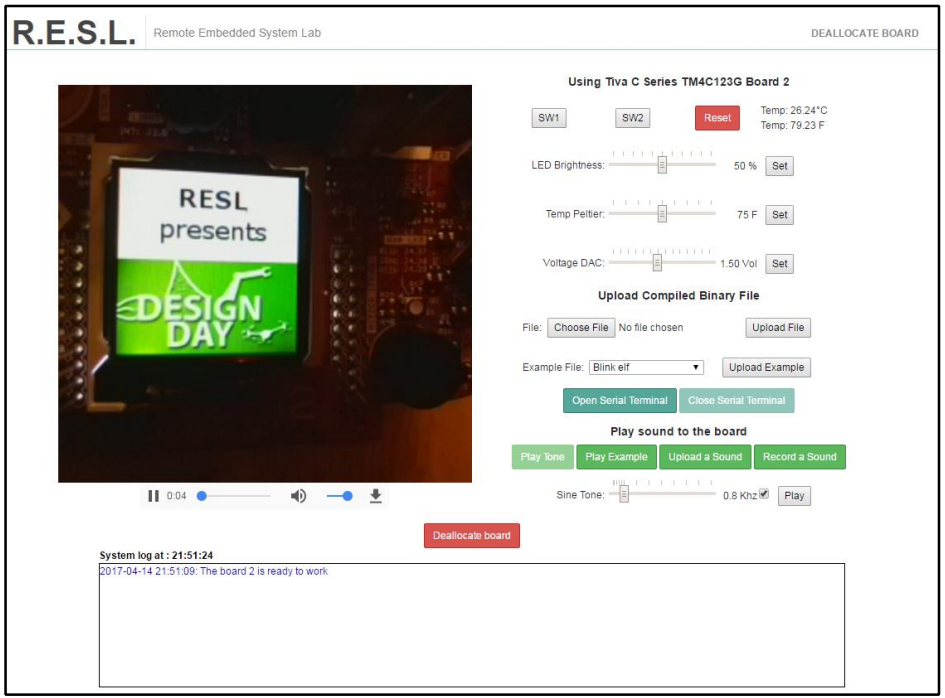
1. Show the temperature of the temperature sensor
2. Switches buttons and Reset button
3. Set the LED brightness (0 to 100%)
4. Set the temperature (65-85 F)
5. Set the voltage of the DAC (0 to 3 V)
6. Upload binary code (user and example code)
7. Open - close serial terminal windows
8. Play sound on the board options
9. Show video streaming
10. Control volume of audio Streaming
11. Deallocate board button
12. System log to show every action

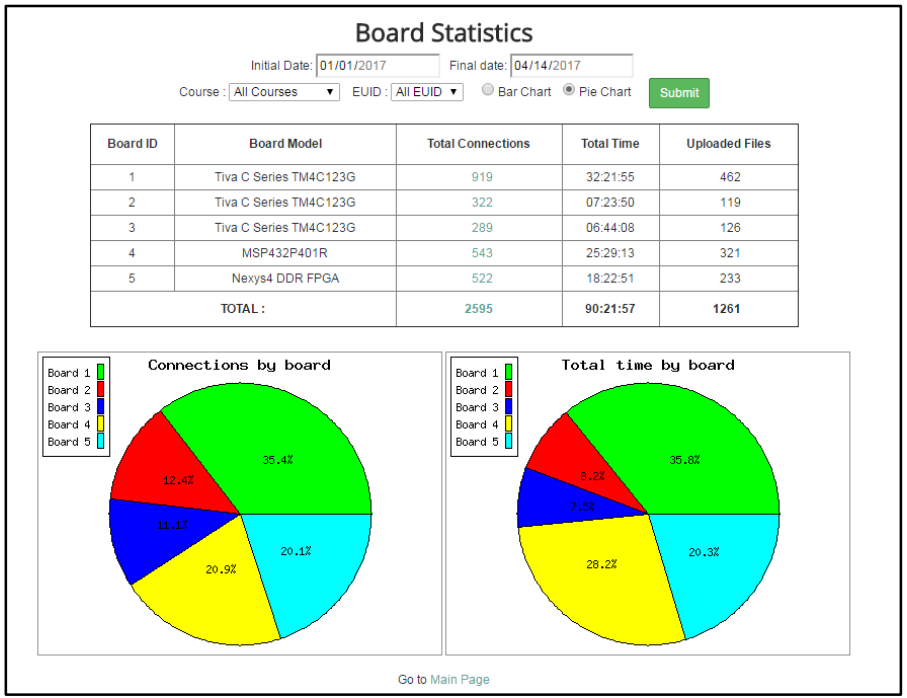
Results



1. Show the temperature of the temperature sensor
2. 5 Switches buttons
3. Reset button
4. Set the temperature (65-85 F)
5. Set the voltage of the DAC (0 to 1 V)
6. Upload bitstream code (user and example code)
7. Open - close serial terminal windows
8. Play sound on the board options
9. Show video streaming
10. Control volume of audio Streaming
11. Deallocate board button
12. 16 slides switches
13. System log to show every action

Results


R.E.S.L.
Remote Embedded System Lab
DEALLOCATE BOARD
RESL
presents
DESIGN DAY
Using Tiva C Series TM4C123G Board 2
SW1
SW2
Reset
Temp: 26.24°C
Temp: 79.23 F
LED Brightness:
50 %
Set
Temp Peltier:
75 F
Set
Voltage DAC:
1.50 Vol
Set
Upload Compiled Binary File
File:
Choose File
No file chosen
Upload File
Example File:
Blink elf
Upload Example
Open Serial Terminal
Close Serial Terminal
Play sound to the board
Play Tone
Play Example
Upload a Sound
Record a Sound
Sine Tone:
0.8 Khz
Play
Deallocate board
System log at : 21:51:24
2017-04-14 21:51:09: The board 2 is ready to work


Board Statistics
Initial Date: 01/01/2017
Final date: 04/14/2017
Course : All Courses
EUID : All EUID
Bar Chart
Pie Chart
Submit
Board ID | Board Model | Total Connections | Total Time | Uploaded Files
1 | Tiva C Series TM4C123G | 919 | 32:21:55 | 462
2 | Tiva C Series TM4C123G | 322 | 07:23:50 | 119
3 | Tiva C Series TM4C123G | 289 | 06:44:08 | 126
4 | MSP432P401R | 543 | 25:29:13 | 321
5 | Nexys4 DDR FPGA | 522 | 18:22:51 | 233
TOTAL : | 2595 | 90:21:57 | 1261
Connections by board
Board 1
Board 2
Board 3
Board 4
Board 5
35.4%
12.4%
11.1%
20.9%
20.1%
Total time by board
Board 1
Board 2
Board 3
Board 4
Board 5
35.8%
8.2%
7.5%
28.2%
20.3%
Go to Main Page

Results

Connection Statistics

Board : All Boards | Initial Date: 01/01/2017 | Final date: 04/14/2017

Course : All Courses | EUID : All EUID | Select View: Daily counts for month | Submit

Overall Statistics	
Total Connections	2595
Different connected users	6
Total time connections	90:21:57
Average connections by user	432.50
Average connection time by connection	00:02:05
Average connection time by user	15:03:39
Total Uploaded files	1261

January 2017

S	M	T	W	T	F	S
1 3	2	3	4	5 1	6 1	7
8 1	9	10 1	11	12	13	14
15	16 2	17 22	18 6	19 13	20 14	21 9
22 1	23 5	24 7	25 4	26 31	27 1	28 27
29 49	30 59	31 62				

February 2017

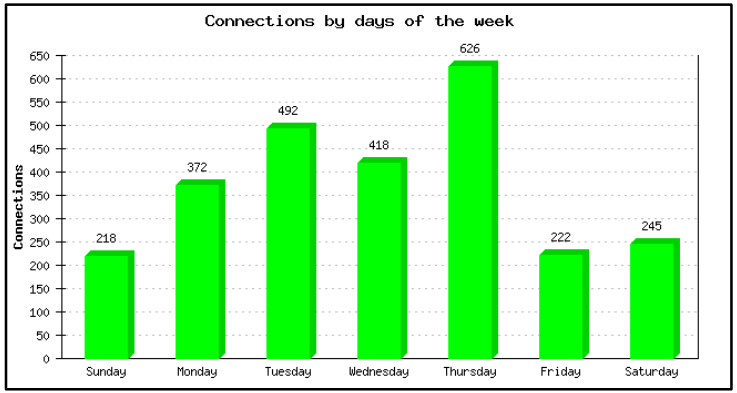
S	M	T	W	T	F	S
			1 52	2 16	3 40	4 14
5 4	6 3	7 24	8 34	9 47	10 21	11 20
12 16	13 11	14 12	15 2	16 10	17 1	18 3
19 7	20 1	21 7	22 2	23	24	25
26 1	27 3	28 5				

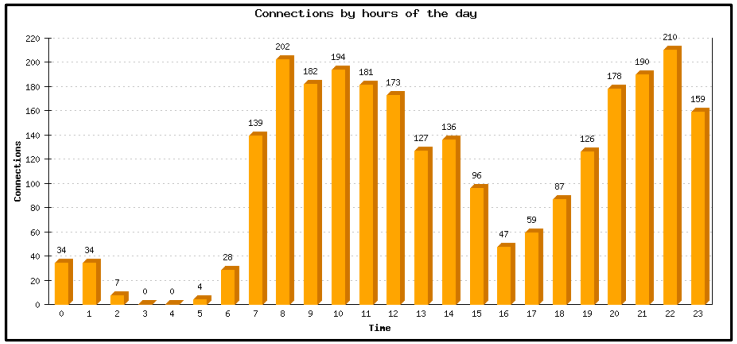
March 2017

S	M	T	W	T	F	S
			1 44	2 19	3	4
5 11	6 14	7 11	8 1	9 25	10	11 3
12 21	13 14	14 14	15 21	16 21	17 7	18 39
19 24	20 32	21 93	22 37	23 124	24 44	25 57
26 14	27 105	28 68	29	30 112	31 25	

April 2017

S	M	T	W	T	F	S
						1 3
2 66	3 70	4 32	5 114	6 115	7 61	8 89
9 7	10 52	11 137	12 89	13 83	14 2	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29
30						





Results

Connection list

Board : All Boards | Initial Date: 01/01/2017 | Final date: 04/14/2017
Course : All Courses | EUID : All EUID | Submit

Number of connections founded: 2595
Showing page 1 of 17 registers by page
Showing 1 de 153

Total Connections : 2595
Total Time : 90:21:57
Total Up Files : 1261

Connection ID	Board ID	Course	EUID	Initial Time	Final Time	Total Time	Uploaded Files	IP
3157	3	CSCE3730.001	fm0105	2017-04-14 19:23:11	2017-04-14 19:24:12	00:01:01	0	66.190.68.255
3156	1	TEST01.001	test123	2017-04-14 12:15:49	2017-04-14 12:16:01	00:00:12	0	129.120.178.55
3155	4	CSCE3730.001	fm0105	2017-04-13 20:58:06	2017-04-13 21:18:58	00:20:52	3	66.190.68.255
3154	4	CSCE3730.001	fm0105	2017-04-13 20:53:43	2017-04-13 20:55:52	00:02:09	1	66.190.68.255
3153	4	CSCE3730.001	fm0105	2017-04-13 20:27:46	2017-04-13 20:38:26	00:10:40	0	66.190.68.255
3152	4	CSCE3730.001	fm0105	2017-04-13 20:24:05	2017-04-13 20:26:58	00:02:53	1	66.190.68.255
3151	5	CSCE3730.001	fm0105	2017-04-13 19:25:41	2017-04-13 19:30:32	00:04:51	3	66.190.68.255
3150	5	CSCE3730.001	fm0105	2017-04-13 19:22:28	2017-04-13 19:25:35	00:03:07	0	66.190.68.255
3149	5	CSCE3730.001	fm0105	2017-04-13 19:20:42	2017-04-13 19:22:16	00:01:34	0	66.190.68.255
3148	5	CSCE3730.001	fm0105	2017-04-13 18:00:52	2017-04-13 18:01:58	00:01:06	0	129.120.178.60
3147	5	CSCE3730.001	fm0105	2017-04-13 17:59:32	2017-04-13 18:00:48	00:01:16	1	129.120.178.60
3146	5	CSCE3730.001	fm0105	2017-04-13 16:25:50	2017-04-13 16:37:06	00:11:16	3	129.120.178.60
3145	5	CSCE3730.001	fm0105	2017-04-13 16:21:56	2017-04-13 16:25:21	00:03:25	2	129.120.178.60
3144	5	CSCE3730.001	fm0105	2017-04-13 15:55:04	2017-04-13 16:12:45	00:17:41	1	129.120.178.60
3143	5	CSCE3730.001	fm0105	2017-04-13 15:20:47	2017-04-13 15:21:52	00:01:05	1	129.120.178.60
3142	4	CSCE3730.001	fm0105	2017-04-13 15:20:39	2017-04-13 15:20:44	00:00:05	0	129.120.178.60
3141	2	CSCE3730.001	fm0105	2017-04-13 15:20:30	2017-04-13 15:20:36	00:00:06	0	129.120.178.60

1 2 3 4 5 6 7 8 9 10 » |>

Save CSV File

Go to Main Page

Deallocate Board (RESL)

fm0105. You have deallocated the Board: 2.

You have been 00:07:10 connected.

View and download your registered log

Go to Main Page

Log List (RESL)

2017-04-13 20:58:07: The board 4 is ready to work
2017-04-13 20:58:45: The board 4 was flashed with the file MicrophoneFFT_MSP432P401R.out
2017-04-13 21:05:06: A 1000 Hz Sine Signal was sent to the microphone of the board 4
2017-04-13 21:05:18: The board 4 was flashed with the file Blink.GREEN.elf
2017-04-13 21:09:26: The board 4 was flashed with the file MicrophoneFFT_MSP432P401R.out
2017-04-13 21:18:58: You have deallocated the Board: 4. You have been 00:20:52 connected.

Download a register log file.

Return to previous page

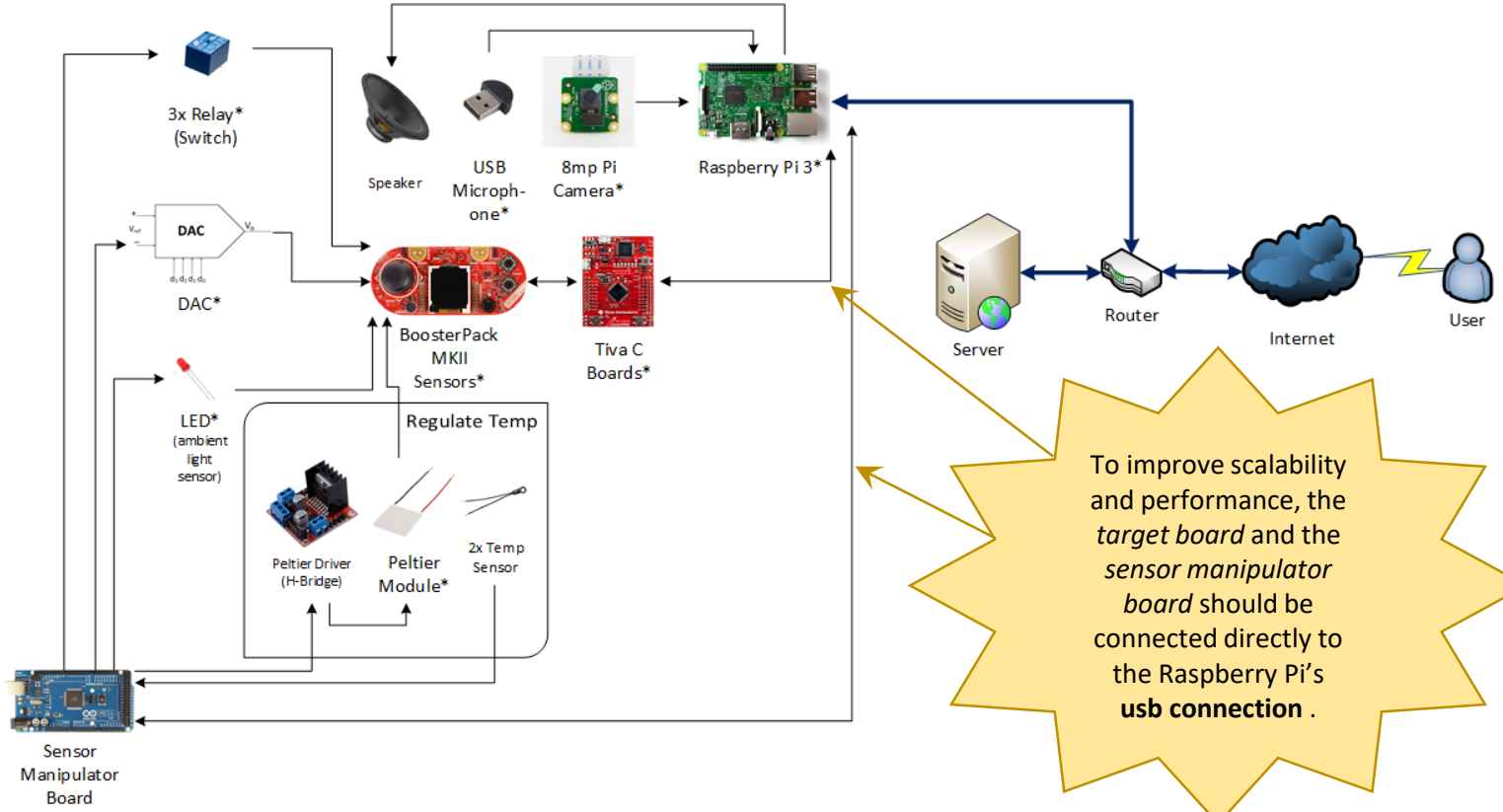
Conclusion

This lab is fully capable of controlling buttons and sensors for all boards

Overall the lab permits the following:

- Multi-user, multi-board
- Responsive in real-time
- Ideal for long distance education
- Sharing expensive boards in traditional labs.

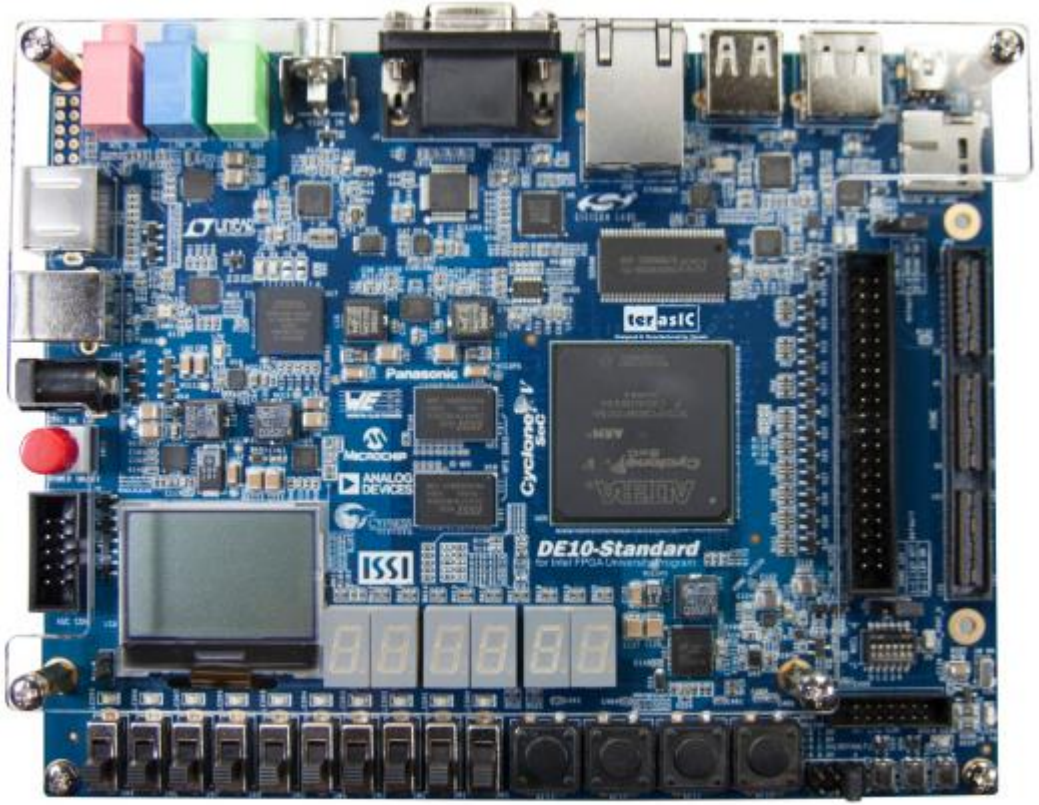
Improvement: Tested, but not implemented



Improvement: Tested, but not implemented yet

- Boards and Arduino connected to Raspberry PI ✓
- Server only will be used for user access, board allocation management, connection logs, and statistics ✓
- Addition of different FPGA boards:
  - Altera DE10-Standard ✓
  - IceZum Alhambra ✓
- Relays to control power of the target boards ✓
- Relays to power on a LED for external board illumination ✓

In Progress



DE-10 Standard Board

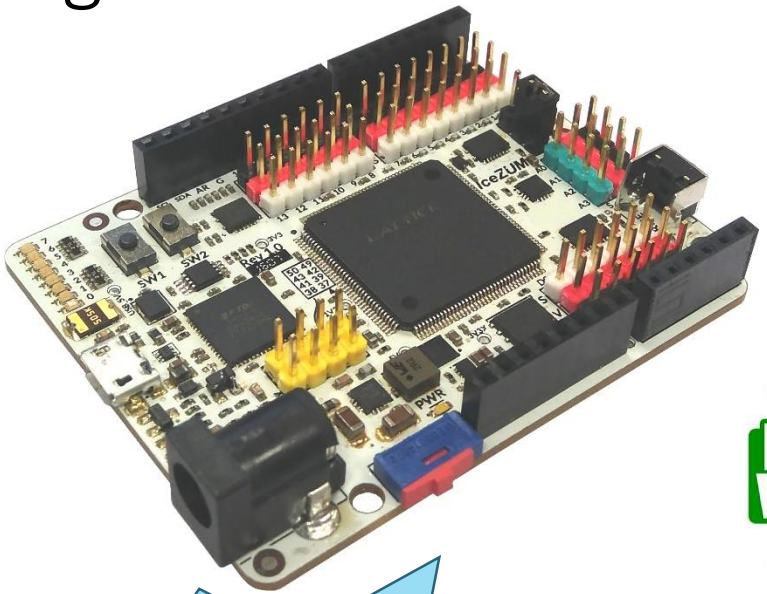
Cyclone V SX SoC

intel
ALTERA

terasIC
www.terasic.com

QUARTUS II

In Progress



IceZum Alhambra

iCE40HX1K from Lattice

OpenFPGA development

Acknowledgements

- UNT Computer Science and Engineering Department
- Dr. Robin Pottathuparambil

Thanks

Questions?