BURR-BROWN®

ADS1286

12-Bit Micro Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SERIAL INTERFACE
- GUARANTEED NO MISSING CODES
- 20kHz SAMPLING RATE
- LOW SUPPLY CURRENT: 250µA

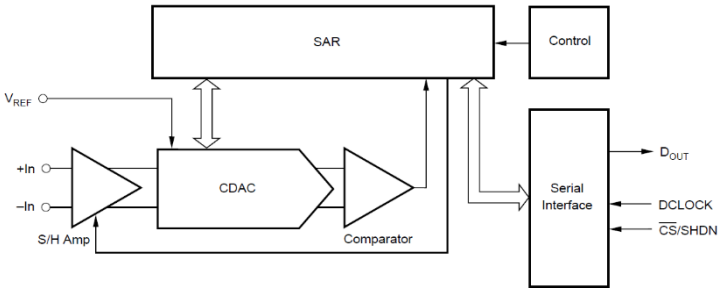
APPLICATIONS

- REMOTE DATA ACQUISITION
- ISOLATED DATA ACQUISITION
- TRANSDUCER INTERFACE
- BATTERY OPERATED SYSTEMS

DESCRIPTION

The ADS1286 is a 12-bit, 20kHz analog-to-digital converter with a differential input and sample and hold amplifier and consumes only 250µA of supply current. The ADS1286 offers an SPI and SSI compatible serial interface for communications over a two or three wire interface. The combination of a serial two wire interface and micropower consumption makes the ADS1286 ideal for remote applications and for those requiring isolation.

The ADS1286 is available in a 8-pin plastic mini DIP and a 8-lead SOIC.



SPECIFICATIONS

At $T_A = T_{MIN}$ to T_{MAX}, $+V_{CC} = +5V$, $V_{REF} = +5V$, $f_{SAMPLE} = 12.5kHz$, , $f_{CLK} = 16 \cdot f_{SAMPLE}$, unless otherwise specified.

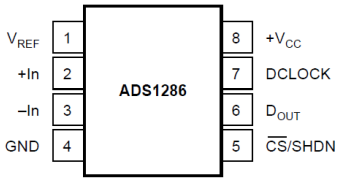
PARAMETER	CONDITIONS	ADS1286, ADS1286A			ADS1286K, ADS1286B			ADS1286C, ADS1286L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT											
Full-Scale Input Range	+In – (–In)	0		V_{REF}	*		*	*		*	V
Absolute Input Voltage	+In	–0.2		V_{CC} +0.2	*		*	*		*	V
	–In	–0.2		+0.2	*		*	*		*	V
SYSTEM PERFORMANCE											
Resolution			12			*			*		Bits
No Missing Codes		12			*			*			Bits
Integral Linearity			±1	±2		*	*		±0.5	±1	LSB
Differential Linearity			±0.5	±1.0		*	±0.75		±0.25	±0.75	LSB
Offset Error			0.75	±3		*	*		*	*	LSB
Gain Error			±2	±8		*	*		*	*	LSB
Noise			50			*			*		µVrms
Power Supply Rejection			82			*			*		dB
SAMPLING DYNAMICS											
Conversion Time				12			*			*	Clk Cycles
Acquisition Time		1.5			*			*			Clk Cycles
Small Signal Bandwidth			500			*			*		kHz
REFERENCE INPUT											
REF Input Range		1.25	2.5	V_{CC}+0.05V	*	*	*	*	*	*	V
Input Resistance	$\overline{CS}$ = V_{CC}		5000			*			*		MΩ
	$\overline{CS}$ = GND, f_{CLK} = 0Hz		5000			*			*		MΩ
Current Drain	$\overline{CS}$ = V_{CC}		0.01	2.5		*	*		*	*	µA
	$t_{CYC} \geq 640\mu s$, $f_{CLK} \leq 25kHz$		2.4	20		*	*		*	*	µA
	$t_{CYC} = 80\mu s$, $f_{CLK} = 200kHz$		2.4	20		*	*		*	*	µA
DIGITAL INPUT/OUTPUT											
Logic Family			CMOS			*			*		
Logic Levels:											
V_{IH}	I_{IH} = +5µA	3		+V_{CC}	*		*	*		*	V
V_{IL}	I_{IL} = +5µA	0.0		0.8	*		*	*		*	V
V_{OH}	I_{OH} = 250µA	3		+V_{CC}	*		*	*		*	V
V_{OL}	I_{OL} = 250µA	0.0		0.4	*		*	*		*	V
Data Format			Straight Binary			*			*		
POWER SUPPLY REQUIREMENTS											
Power Supply Voltage											
V_{CC}		+4.50	5	5.25	*	*	*	*	*	*	V
Quiescent Current, V_{ANA}	$t_{CYC} \geq 640\mu S$, $f_{CLK} \leq 25kHz$		200	400		*	*		*	*	µA
	$t_{CYC} = 90\mu S$, $f_{CLK} = 200kHz$		250	500		*	*		*	*	µA
Power Down	$\overline{CS}$ = V_{CC}			3			*			*	µA

TIMING CHARACTERISTICS

f_{CLK} = 200kHz, $T_A = T_{MIN}$ to T_{MAX}.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence	1.5		2.0	Clk Cycles
$t_{SMPL\ (MAX)}$	Maximum Sampling Frequency	ADS1286			20	kHz
t_{CONV}	Conversion Time	See Operating Sequence		12		Clk Cycles
t_{dDO}	Delay TIme, DCLOCK↓ to D_{OUT} Data Valid	See Test Circuits		85	150	ns
t_{dis}	Delay TIme, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits		25	50	ns
t_{en}	Delay TIme, DCLOCK↓ to D_{OUT} Enable	See Test Circuits		50	100	ns
t_{hDO}	Output Data Remains Valid After DCLOCK↓	C_{LOAD} = 100pF	15	30		ns
t_f	D_{OUT} Fall Time	See Test Circuits		70	100	ns
t_r	D_{OUT} Rise Time	See Test Circuits		60	100	ns
t_{CSD}	Delay Time, $\overline{CS}$↓ to DCLOCK↓	See Operating Sequence			0	ns
t_{SUCS}	Delay Time, $\overline{CS}$↓ to DCLOCK↑	See Operating Sequence	30			ns

PIN CONFIGURATION



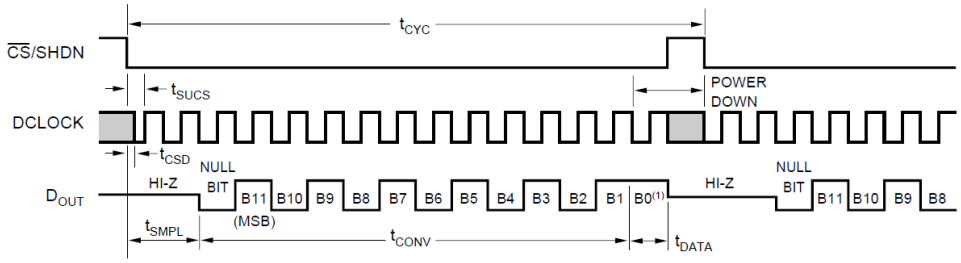
8-Pin Mini PDIP
8-Lead SOIC

SERIAL INTERFACE

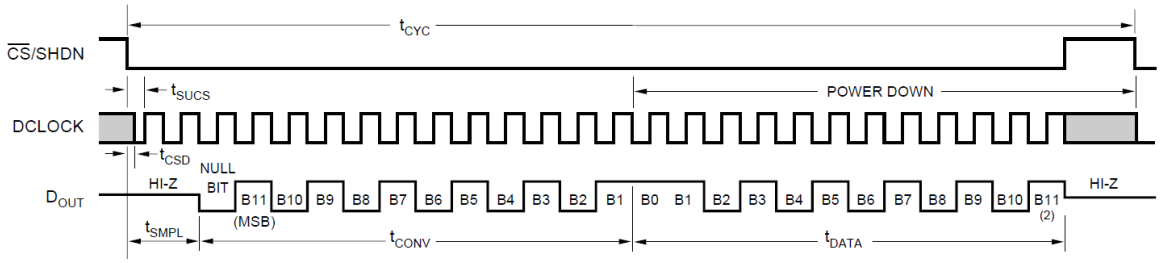
The ADS1286 communicates with microprocessors and other external digital systems via a synchronous 3-wire serial interface. DCLOCK synchronizes the data transfer with each bit being transmitted on the falling DCLOCK edge and captured on the rising DCLOCK edge in the receiving system. A falling $\overline{CS}$ initiates data transfer as shown in Figure 1. After $\overline{CS}$ falls, the second DCLOCK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the ADS1286 for the next data exchange.

PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V_{REF}	Reference Input.
2	+In	Non Inverting Input.
3	–In	Inverting Input. Connect to ground or remote ground sense point.
4	GND	Ground.
5	$\overline{CS}$/SHDN	Chip Select when low, Shutdown Mode when high.
6	D_{OUT}	The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges.
7	DCLOCK	Data Clock synchronizes the serial data transfer and determines conversion speed.
8	$+V_{CC}$	Power Supply.



Note: (1) After completing the data transfer, if further clocks are applied with $\overline{CS}$ LOW, the ADC will output LSB-First data then followed with zeroes indefinitely.



Note: (2) After completing the data transfer, if further clocks are applied with $\overline{CS}$ LOW, the ADC will output zeroes indefinitely.

t_{DATA}: During this time, the bias current and the comparator power down and the reference input becomes a high impedance node, leaving the CLK running to clock out LSB-First data or zeroes.