

# **OptiMOS®-P2 Power-Transistor**

# AEC<sup>0</sup> Qualified

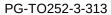


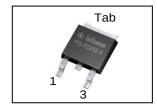
#### **Features**

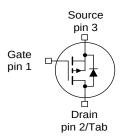
- P-channel Logic Level Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested

#### **Product Summary**

$V_{ m DS}$	-40	٧
R <sub>DS(on)</sub>	7.8	mΩ
$I_{D}$	-70	Α







Туре	Package	Marking
IPD70P04P4L-08	PG-TO252-3-313	4P04L08

## **Maximum ratings,** at $T_j$ =25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I <sub>D</sub>	T <sub>C</sub> =25°C, V <sub>GS</sub> =-10V	-70	А
		T <sub>C</sub> =100°C, V <sub>GS</sub> =-10V <sup>1)</sup>	-55	
Pulsed drain current <sup>1)</sup>	I <sub>D,pulse</sub>	Т <sub>С</sub> =25°С	-280	
Avalanche energy, single pulse <sup>1)</sup>	E <sub>AS</sub>	I <sub>D</sub> =-35A	24	mJ
Avalanche current, single pulse	I <sub>AS</sub>	-	-70	А
Gate source voltage	V <sub>GS</sub>	-	+5/-16	V
Power dissipation	P <sub>tot</sub>	T <sub>C</sub> =25 °C	75	W
Operating and storage temperature	$T_{\rm j}$ , $T_{\rm stg}$	-	-55 +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	



Parameter	Symbol	Conditions	Values		Unit	
			min.	typ.	max.	
Thermal characteristics <sup>1)</sup>						
Thermal resistance, junction - case	R <sub>thJC</sub>	-	-	-	2.0	K/W
SMD version, device on PCB	R <sub>thJA</sub>	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	40	

# **Electrical characteristics,** at $T_j$ =25 °C, unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	$V_{\rm GS}$ =0V, $I_{\rm D}$ = -1mA	-40	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS}=V_{GS}$ , $I_{D}=-120\mu A$	-1.2	-1.7	-2.2	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V, T <sub>j</sub> =25°C	-	-0.05	-1	μΑ
		$V_{DS}$ =-32V, $V_{GS}$ =0V, $T_j$ =125°C <sup>1)</sup>	-	-20	-200	
Gate-source leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =-16V, V <sub>DS</sub> =0V	-	-	-100	nA
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-40A	,	9.5	12.9	mΩ
		V <sub>GS</sub> =-10V, I <sub>D</sub> =-70A	-	6.4	7.8	



Parameter	Symbol Conditions		Values			Unit
			min.	typ.	max.	
Dynamic characteristics <sup>1)</sup>						
Input capacitance	C iss		-	4177	5430	pF
Output capacitance	C <sub>oss</sub>	$V_{\rm GS}$ =0V, $V_{\rm DS}$ =-25V, $f$ =1MHz	-	1185	1778	
Reverse transfer capacitance	C <sub>rss</sub>		-	45	90	
Turn-on delay time	t d(on)		-	12	-	ns
Rise time	t <sub>r</sub>	V <sub>DD</sub> =-20V, V <sub>GS</sub> =-10V, I <sub>D</sub> =-70A,	-	10	-	
Turn-off delay time	t d(off)	$R_{\text{G,ext}}$ =3.5 $\Omega$	-	50	-	
Fall time	t <sub>f</sub>		-	41	-	
Gate Charge Characteristics <sup>1)</sup>			T	1	ı	
Gate to source charge	Q <sub>gs</sub>		-	14	18	nC
Gate to drain charge	$Q_{ m gd}$	V <sub>DD</sub> =-32V, I <sub>D</sub> =-70A,	-	10	20	
Gate charge total	$Q_{\rm g}$	V <sub>GS</sub> =0 to -10V	-	71	92	
Gate plateau voltage	V <sub>plateau</sub>		-	-3.5	-	V
Reverse Diode						
Diode continous forward current <sup>1)</sup>	Is	T -25°C	-	-	-70	А
Diode pulse current <sup>1)</sup>	I <sub>S,pulse</sub>	- <i>T</i> <sub>C</sub> =25°C	-	-	-280	
Diode forward voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>F</sub> =-70A, T <sub>j</sub> =25°C	-	-1	-1.3	V
Reverse recovery time <sup>1)</sup>	t rr	V <sub>R</sub> =-20V, I <sub>F</sub> =-50A,	-	46	-	ns
Reverse recovery charge <sup>1)</sup>	Q <sub>rr</sub>	d <i>i</i> <sub>F</sub> /d <i>t</i> =-100A/μs	-	43	-	nC

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>&</sup>lt;sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

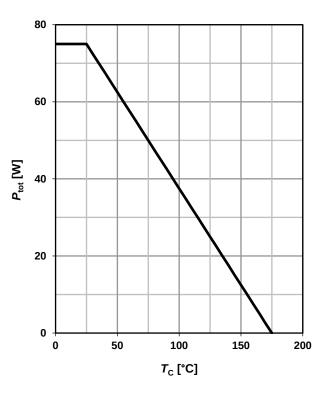


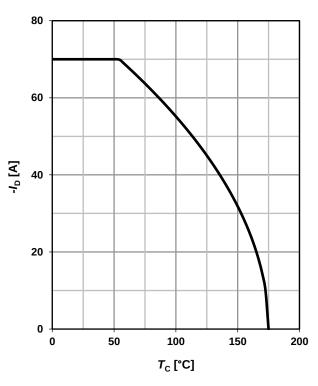
#### 1 Power dissipation

$$P_{tot} = f(T_C); V_{GS} \le -6V$$

#### 2 Drain current

$$I_{\rm D} = f(T_{\rm C}); V_{\rm GS} = -10V$$





#### 3 Safe operating area

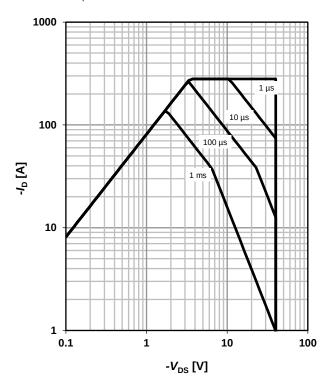
$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

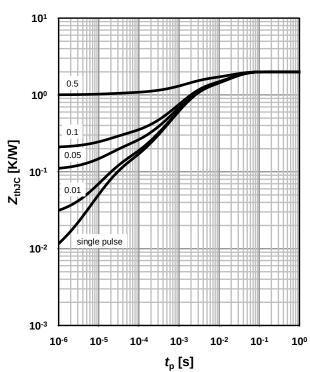
parameter:  $t_p$ 

#### 4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

parameter:  $D = t_p/T$ 



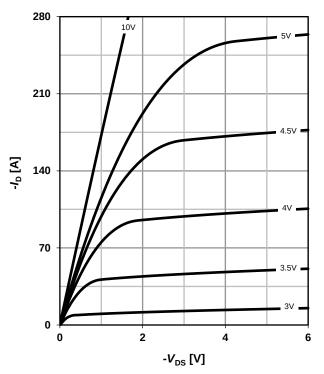




#### 5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25 °C$ 

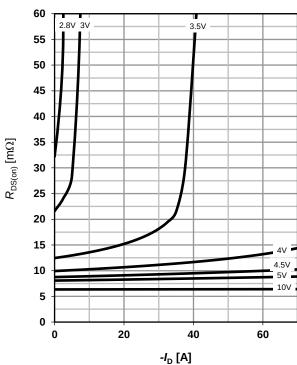
parameter:  $-V_{GS}$ 



#### 6 Typ. drain-source on-state resistance

 $R_{DS(on)} = (I_D); T_j = 25 \, ^{\circ}C$ 

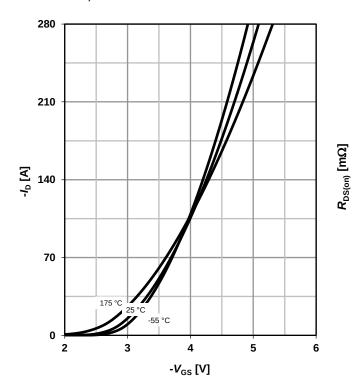
parameter: -V<sub>GS</sub>



#### 7 Typ. transfer characteristics

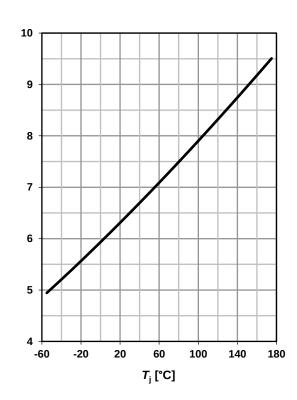
 $I_{D} = f(V_{GS}); V_{DS} = -6V$ 

parameter:  $T_j$ 



#### 8 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = -70 A; V_{GS} = -10 V$$





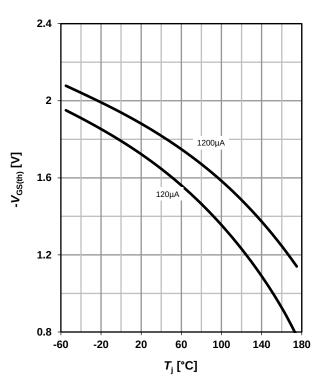
#### 9 Typ. gate threshold voltage

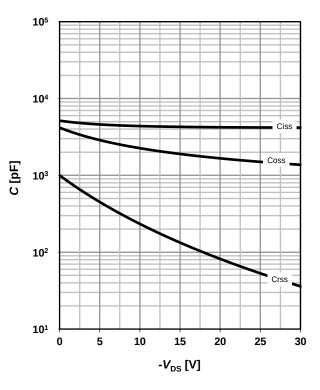
 $V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$ 

parameter: -I D

#### 10 Typ. capacitances

 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$ 





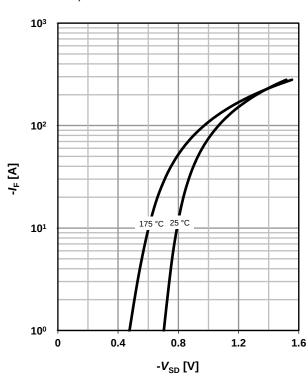
#### 11 Typical forward diode characteristicis

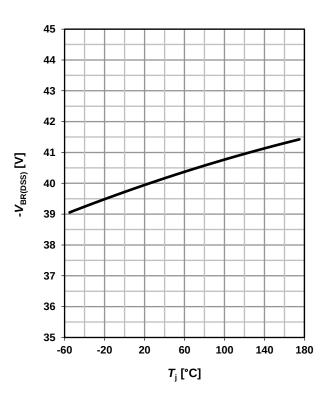
 $IF = f(V_{SD})$ 

parameter:  $T_j$ 

#### 12 Drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_j); I_D = -1 \text{ mA}$$





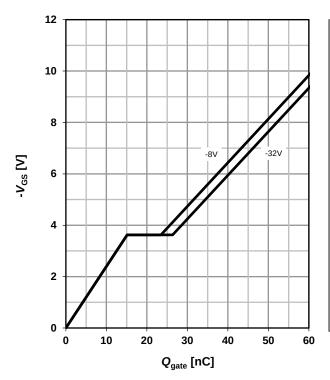


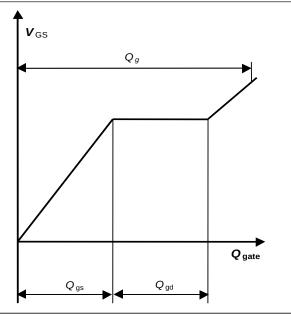
## 13 Typ. gate charge

#### 14 Gate charge waveforms

 $V_{\rm GS}$  = f( $Q_{\rm gate}$ );  $I_{\rm D}$  = -70 A pulsed

parameter:  $V_{\mathrm{DD}}$ 







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**Revision History** 

Version		Date	Changes
	1.0	14.03.2011	Final Data Sheet
	1.1	21.12.2012	Update of typical Rdson
	1.2	04.07.2019	V <sub>GS</sub> changed
	1.21	19.08.2021	Editorial changes

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