

Laboratory Work 4 - Pipelined Processor Design

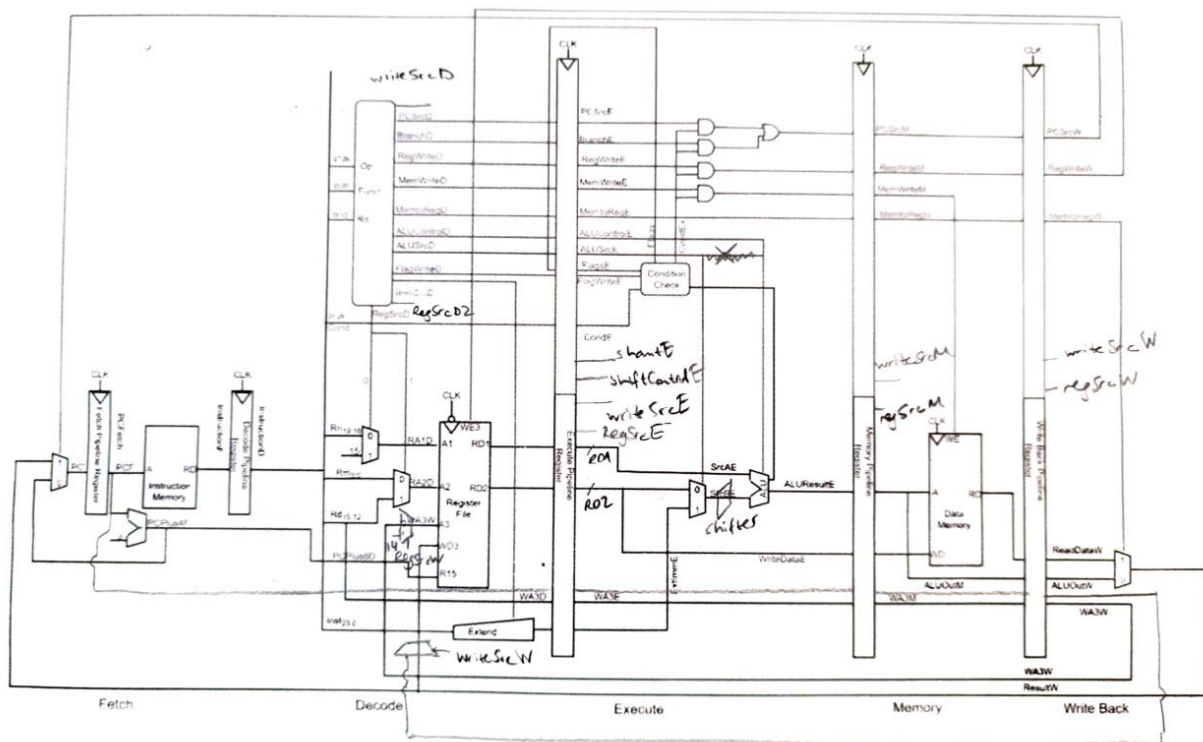
1 Preliminary Work

1.1 Reading Assignment

1.2 Pipelined Processor Design with Verilog HDL

1.2.1 Datapath Design

For datapath design, pipelined processor discussed in the lectures is modified. Modifications can be seen below.



Shifter is added to the datapath immediately before B port of ALU module. To be used in the execute stage, sampled in the execute pipeline register.

To satisfy BL instruction, write address of Register File is selected with an multiplexer between 14 and Rd using select signal RegSrcW. Moreover, for BX instruction, WriteSrc signal is added to select between ResultW or PCPlus4W signal. Since these signals are used in the writeback stage, RegSrcW, PCPlus4W and WriteSrc are sampled in the decode stage and carried through pipeline.

To be able to multiply imm24 by 4, extender is modified.

Register File is written at the negative edge of clock.

For data processing instructions, Rd and Rm selected for A1 and A2, respectively and Rd is forwarded to be used as write address. Then, RD1, RD2, WA3D and ExtImm signals are stored to be used in the next cycle. Then, shifter, ALUSrc and ALU signals are determined according to instruction. RD2, ALUResult and write address for Register File are stored. In the next cycle, memory stage, ReadData and

ALUOut is sampled but read data don't be selected in the next cycle. In the writeback stage, RegWrite signal is high, write address carried is connected to A3. Falling edge of the cycle, ALUOut value is written to the register.

For memory instructions, Rn is selected for A1 and for STR, Rd is selected for A2. RD1, RD2 and ExtImm signals are sampled at the rising edge of clock. Then, ExtImm signal is selected and added with RD1 value. No shift operation for memory instruction. ALUResult and RD2 values are sampled. In the next cycle, data at the address of the ALUResult is read and sampled for LDR. For STR, MemWrite signal is high to write RD2 value to the given position and STR operation is completed. Then, in the next stage, readData is written to Rd register for LDR operation.

For B and BL instructions, R15 is selected and imm24 value is multiplied by 4. Then, in the next cycle, RD1 and ExtImm values are added and result is stored. In the memory stage, memory is read but obtained data won't be used. Then, in the writeback stage, PCSrc is high and PC value will be ResultW in the next cycle. For BL instruction, RegWrite is 1 and PC+4 value will be written to the R14 register. PC+4 value is the value forwarded while decoding the instruction. For BX, Rm value is selected for A2 and RD2 value is stored. In the next cycle, RD2 value directly moved to ALUResult and stored. Then, similar to data processing instructions, memory will be read but its value won't be used. Then, in the writeback stage, ALUResult is written to PC register.

1.2.2 Controller Design

PCSrc is 0 unless it is an write instruction to register 15 and carried through pipeline. Similarly, Branch signal is 0 unless it is an branch instruction and carried through pipeline. During execute stage, (PCSrc | Branch) & CondEx is computed and transferred to the next stage.

During execution stage, RegWriteD and MemWriteD signals are ANDed with CondEx. Flags are updated according to FlagW signal determined in the decode stage.

For all instructions, since RegSrc[2], WriteSrc, RegW and MemtoReg signals are necessary in the writeback stage, they are carried through pipeline.

FlagW signal is the same as previous processors.

For dataprocessing instructions, RegSrc[0] and RegSrc[1] are 0 and RegSrc[2] signal is 0. WriteSrc and MemtoReg signals are 0. Unless it is an compare instruction, RegW is 1. ALUSrc and ImmSrc change depending on whether or not it is an immediate instruction.

For memory instructions, ImmSrc = 01 and ALUSrc = 1 to select imm12. ShiftControl and shamt signals are 0 not to change ExtImm value. RegSrc[0] = 0 select Rn. If it is an LDR instruction, RegSrc[2] = 0 to choose Rd as write address. For STR operation, RegSrc[1] = 1 to make A2 Rd. WriteSrc equals to 0 to choose ResultW. ALU operation is addition.

For branch instructions, ShiftControl and shamt signals are 0 not to change value. RegSrc[0] = 1 to select R15. MemtoReg = 0 to choose ALUResult. For B and BL instructions, ImmSrc = 10 and ALUSrc = 1 to choose imm24. For BL instruction, to be able to write R14, RegSrc[2] = 1 and RegW = 1. While ALU operation is addition for B and BL, for BX ALU operation is moveB. For BX, RegSrc[1] = 0 and ALUSrc = 0 in order to choose Rm for A2 and ALU.

Feyza Nur Takıl 2375780

1.2.3 Testbench

Testbenches can be found inside the code submission.