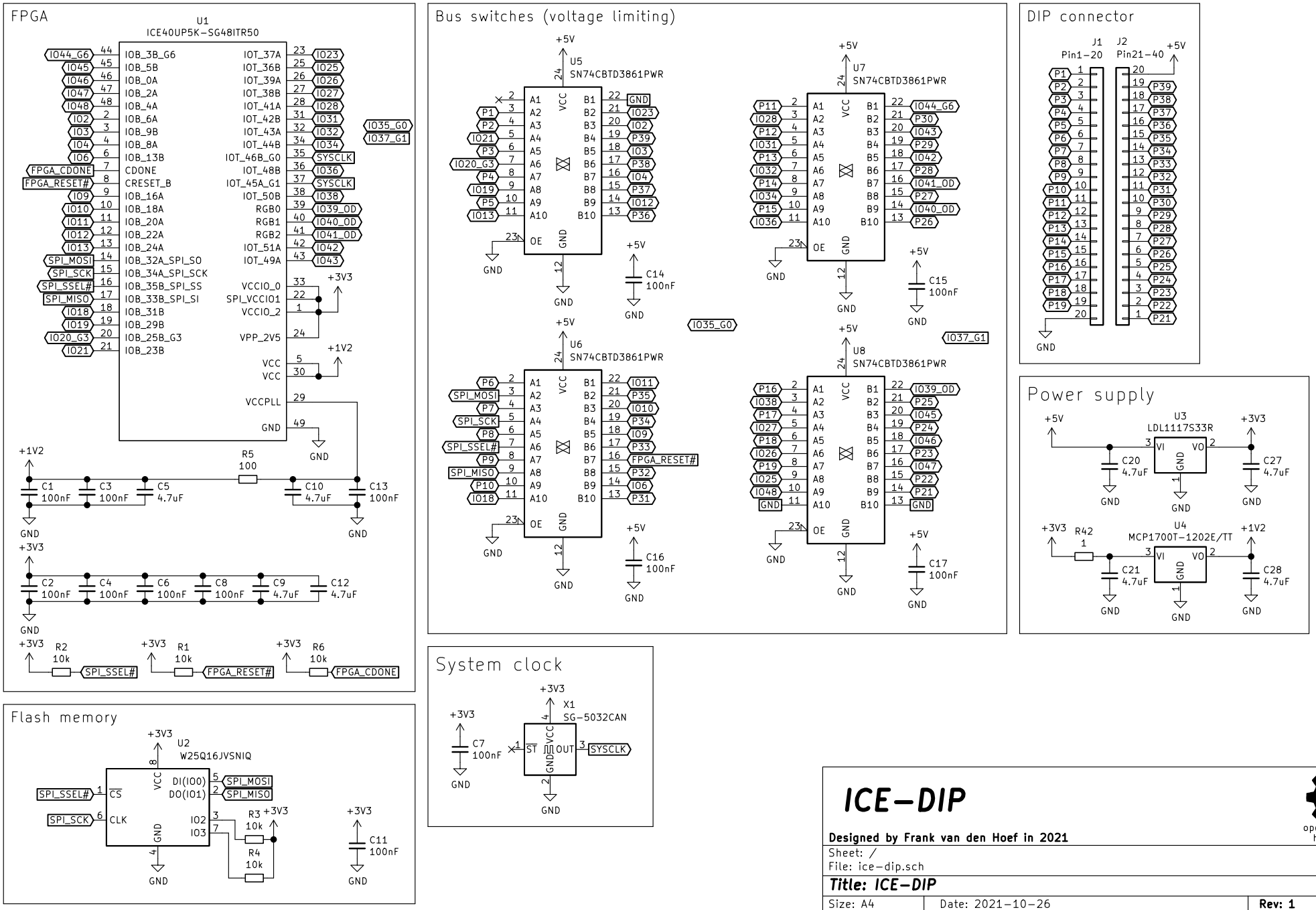
FPGA
U1
ICE40UP5K-SG48ITR50
Bus switches (voltage limiting)
U5
SN74CBTD3861PWR
U6
SN74CBTD3861PWR
U7
SN74CBTD3861PWR
U8
SN74CBTD3861PWR
DIP connector
J1
Pin1-20
J2
Pin21-40
Power supply
U3
LDL1117S33R
U4
MCP1700T-1202E/TT
System clock
X1
SG-5032CAN
Flash memory
U2
W25Q16JVSNIQ
ICE-DIP
Designed by Frank van den Hoef in 2021
open source hardware
Sheet: /
File: ice-dip.sch
Title: ICE-DIP
Size: A4
Date: 2021-10-26
Rev: 1
KiCad E.D.A. kicad (5.1.10-1-10_14)
Id: 1/1