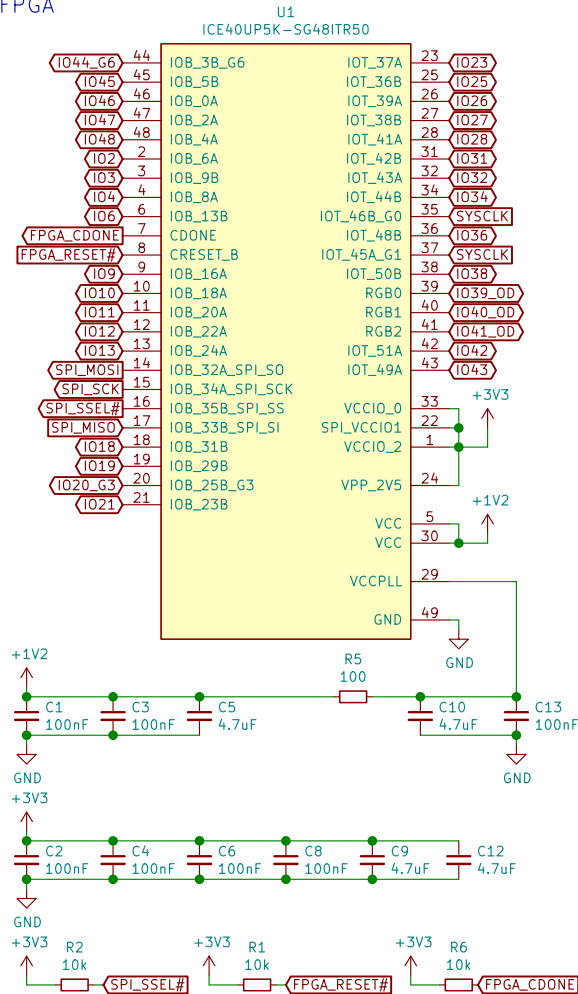
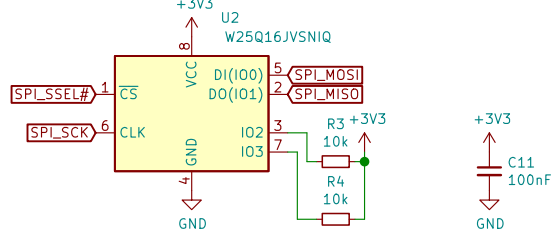


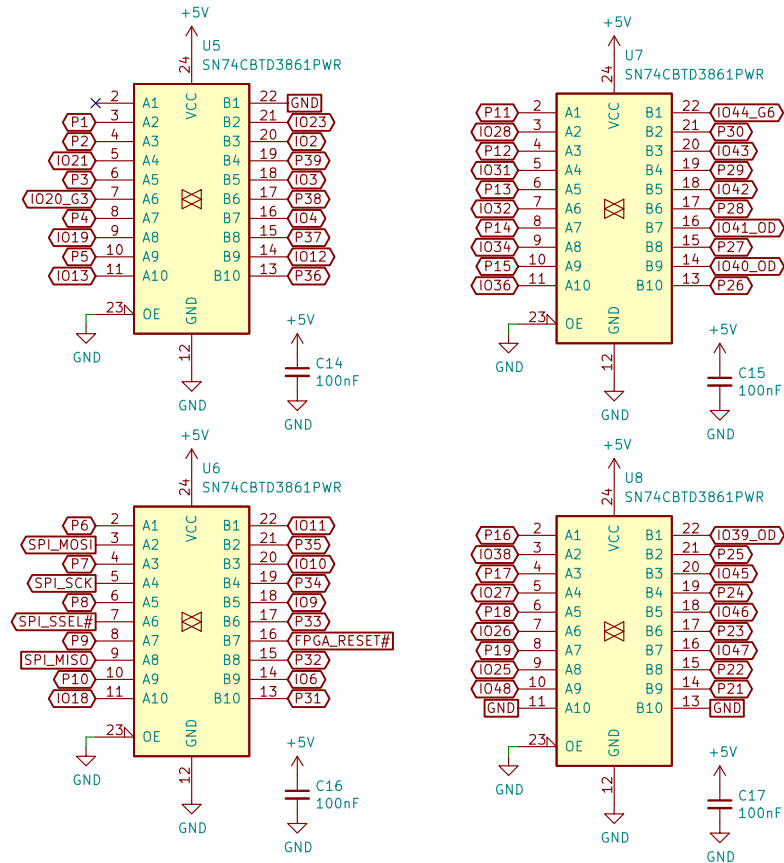
FPGA



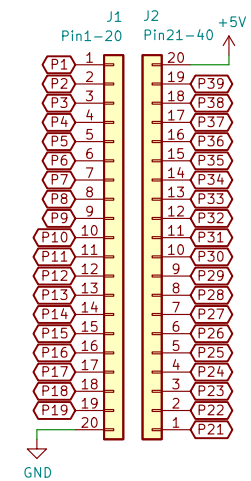
Flash memory



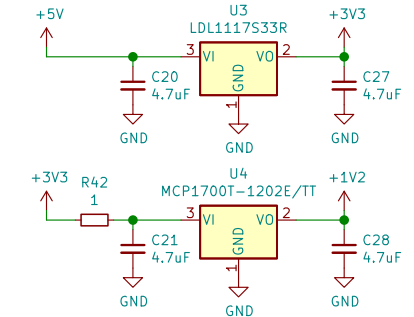
Bus switches (voltage limiting)



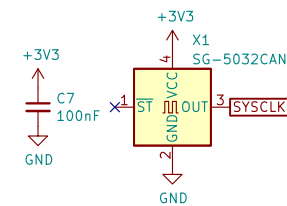
DIP connector



Power supply



System clock



ICE-DIP

Designed by Frank van den Hoef in 2021

Sheet: /
File: ice-dip.sch

Title: ICE-DIP

Size: A4 Date: 2021-10-26
KiCad E.D.A. kicad (5.1.10-1-10_14)

Rev: 1
Id: 1/1

