2022 T4 CSD 2D Group 17

Structure of Adder

We used the 32-bit Kogge Stone Adder (KSA) architecture with some amendments. We added an additional lane for the carry-in (ALUFN0) to allow for the addition of signed integers. We also buffered the ALUFN0 signal via a tree format to optimise the delay and chip area both within the KSA and for the 1's complement of input B aiming to maintain at most 1:4 connection. The KSA design minimises the fan-out for each level of output, creating a minimised dependency on a singular output gate. This will increase the processing speed through the use of parallel processing of inputs to minimise the propagation delay.

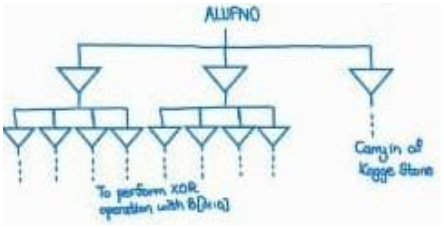

Fig. 1 Diagram of Buffer Tree for ALUFN0

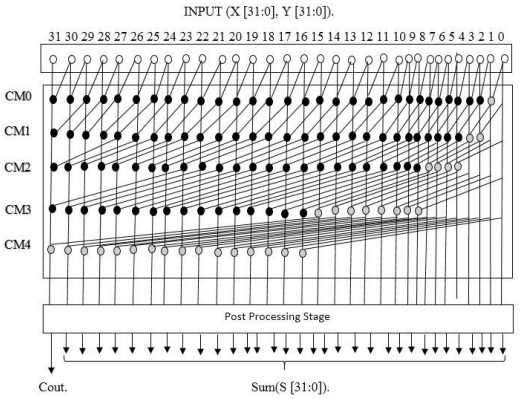

Fig. 2 Abstraction of the 32-bit Kogge Stone adder[1]

The fastest timing the adder can pass is 3ns. (The propagation delay of the 32-bit adder is 2.1531ns)

CNF Proof

The chosen bit output for the CNF between the Ripple Carry Adder (RCA) and KSA is S31

References:

1. Source: Naik V, Manjunatha. (2015). Performance Analysis Of Parallel Prefix Adder. International Journal of Electrical Electronics and Data Communication. 3. 10.18479/ijeedc/2015/v3i7/48267.