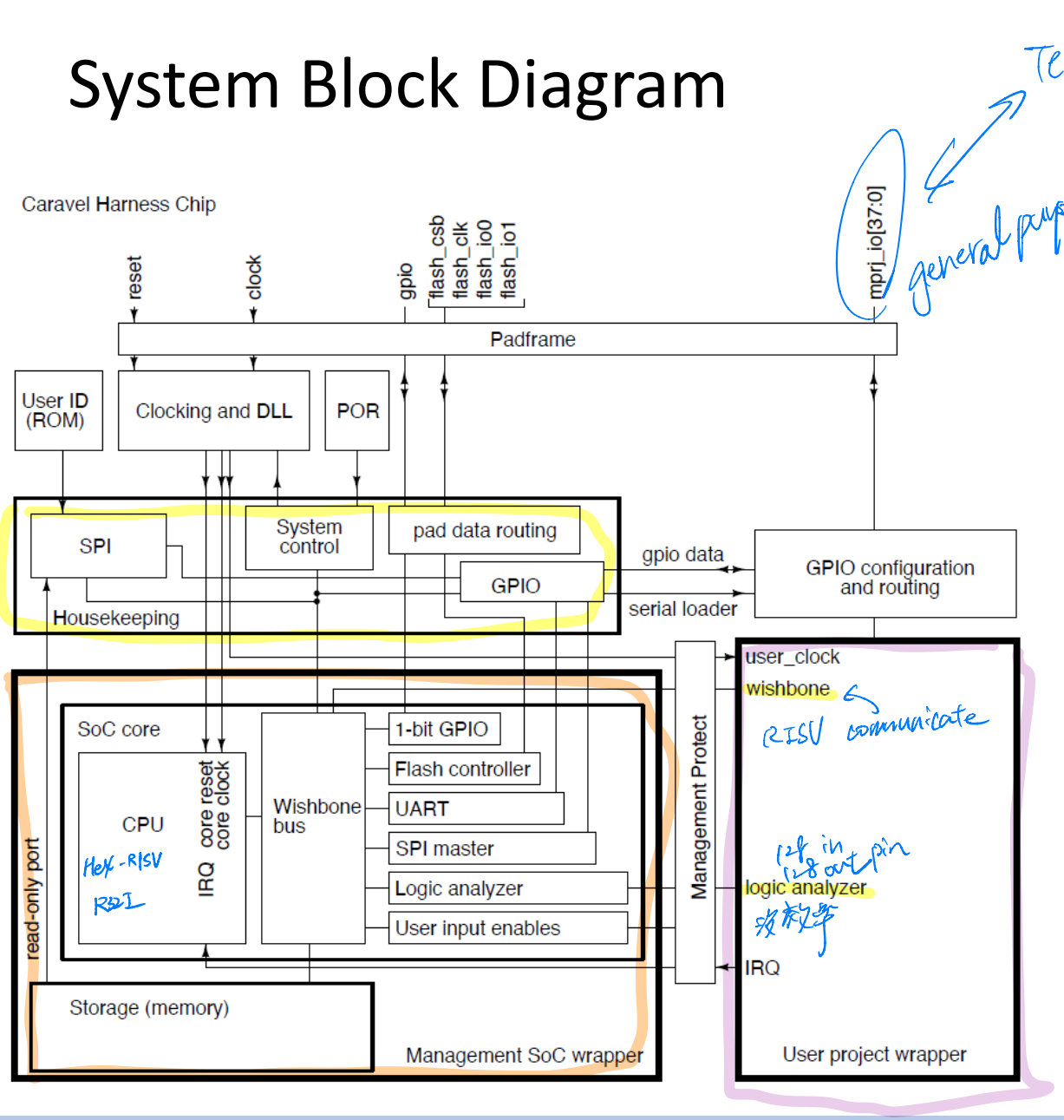
Bridge of Life Education

Caravel SOC Introduction

Jiin Lai

System Block Diagram

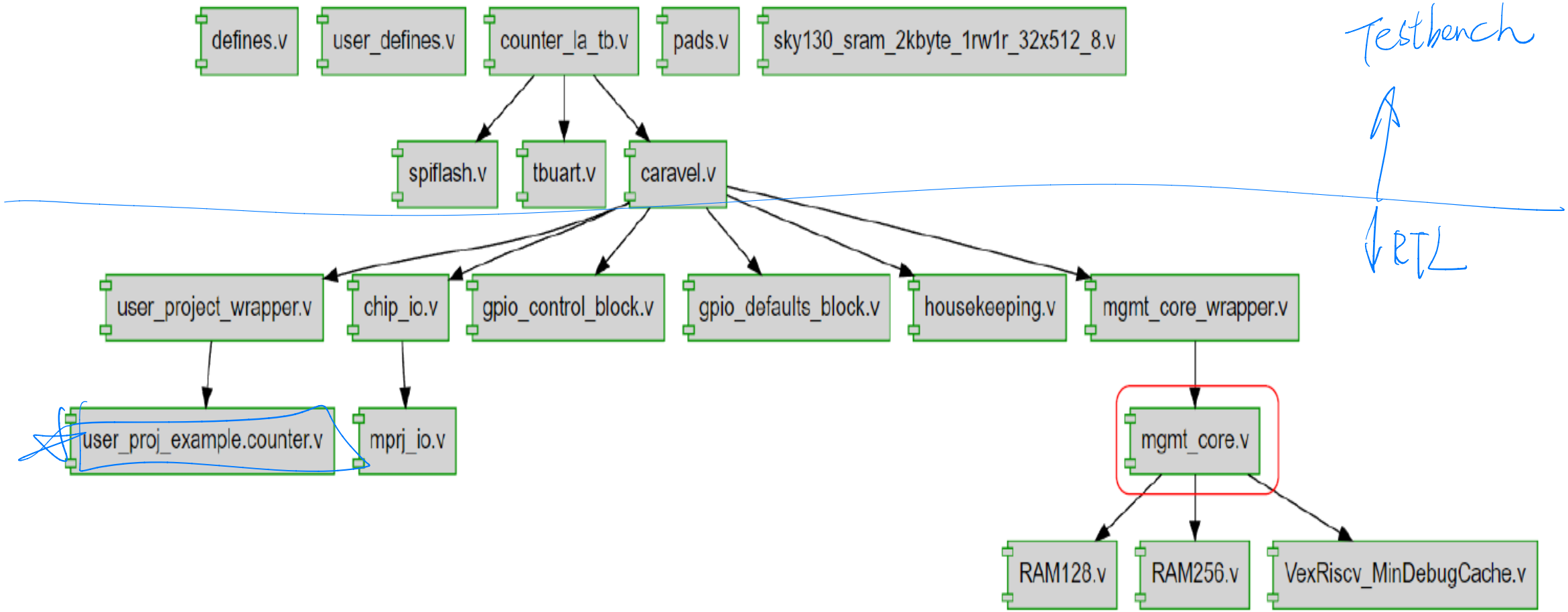


Caravel Architecture

- Top Level : Clocking (DLL)， userID, POR, GPIO
- HouseKeeping - exchange data with management SoC via byte-wide SPI
- Management Area – Peripherals: timer, UART, GPIO, SPI, RISC-V
  - Configure User Project I/O pad
  - Observe and control User Project signals (on-chip logic analyzer)
  - Control the User Project power supply
- User Project Area
  - 38 MPRJ
  - 128 logic analyzer probes
  - Wishbone port to interface with management SoC
- Power-up, SPI automatically configures the GPIO

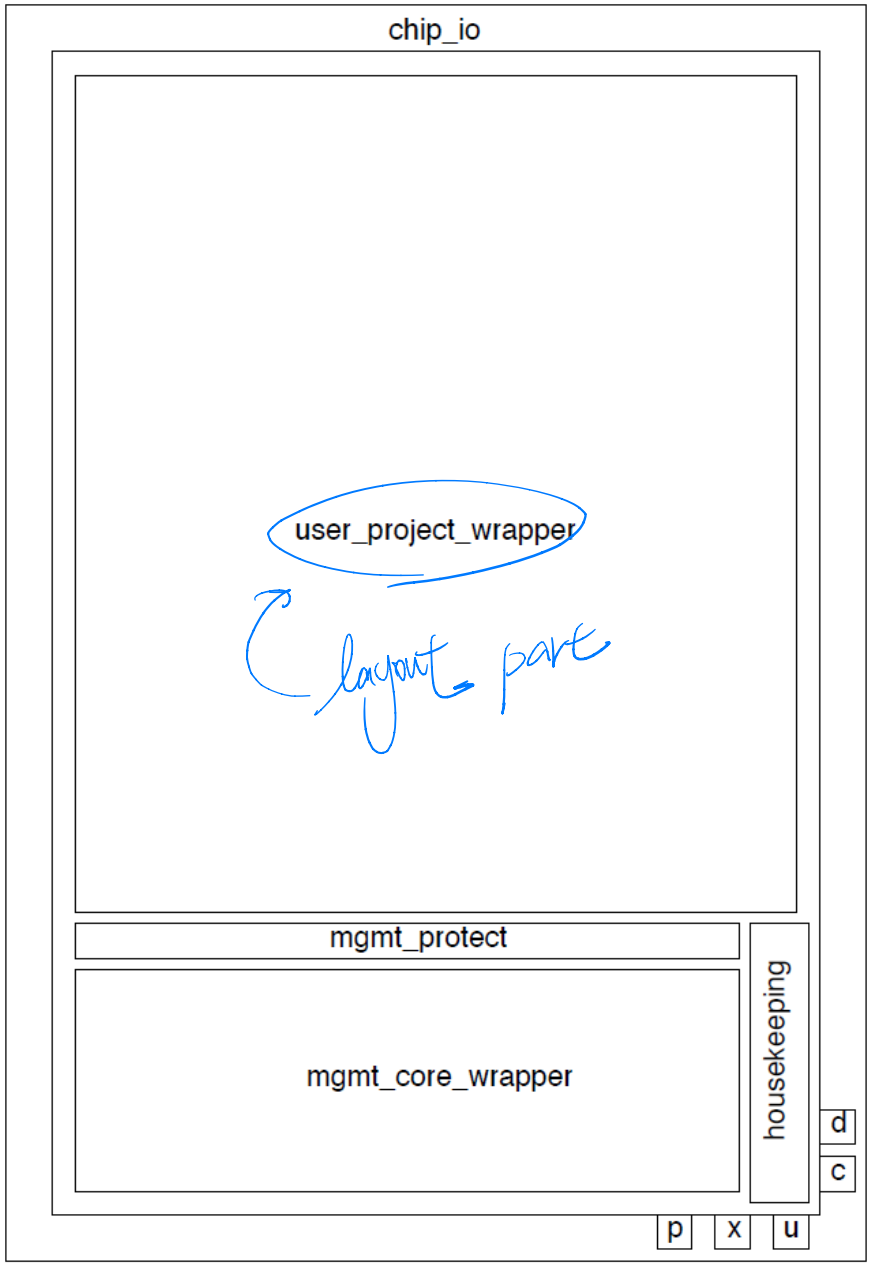
Caravel Github – Design Hierarchy

open source



Caravel Floorplan

Tape out



padframe:
each GPIO pad
has an associated
gpio_control_block
and
gpio_defaults_block

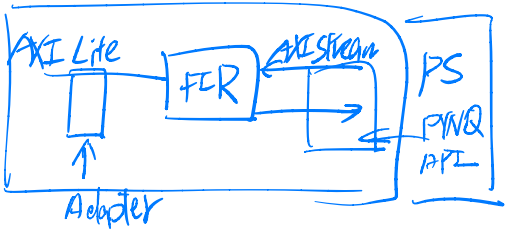
c= caravel_clocking
d= digital_pll
u= user_id_programming
p= simple_por
x= xres_buf

Video

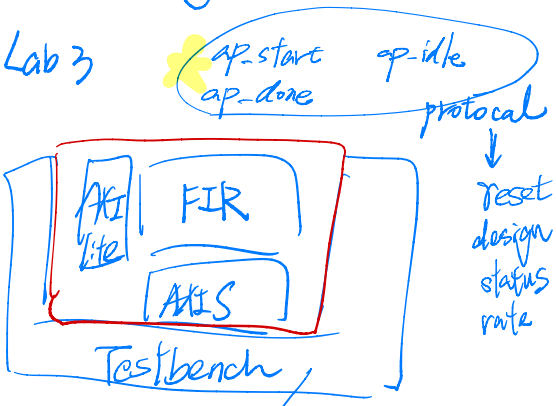
Topics	Author	Video
System Block Diagram		
Reset POR	Tony	https://youtu.be/hbISphnvVYg
Management Project Area	Tony	
DLL, Configuration SPI	Tony	
Housekeep SPI	Willy	https://youtu.be/Vw3TGc-YV8E
GPIO	Willy	
SPI	Willy	
Memory-mapped IO	Willy	
Counter/Timer/UART	Hurry	https://youtu.be/-o87eNkqmPo
Wishbone	Josh	https://youtu.be/Xvk4jCB9l7U
IRQ	Josh	https://youtu.be/G3oT0DJfZMk
SRM	Josh	https://youtu.be/X8sMMfrXKac
User Project Interface	Josh	
Testbench	Josh	https://youtu.be/0neIx5DOK1g
Firmware	Josh	

Verilog FIR

Lab 2 : HLS FIR



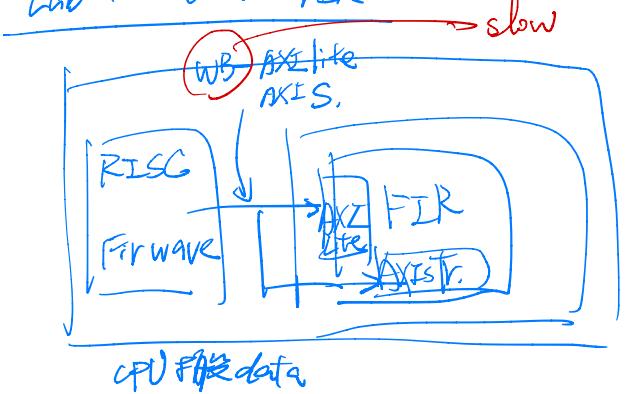
Lab 3



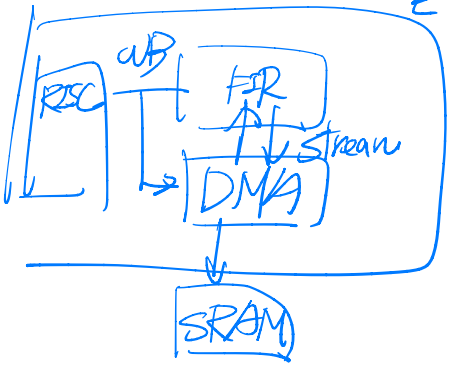
reset?
design
status
rate

① FIR design + State machine
② lite, Stream interface
③ Testbench

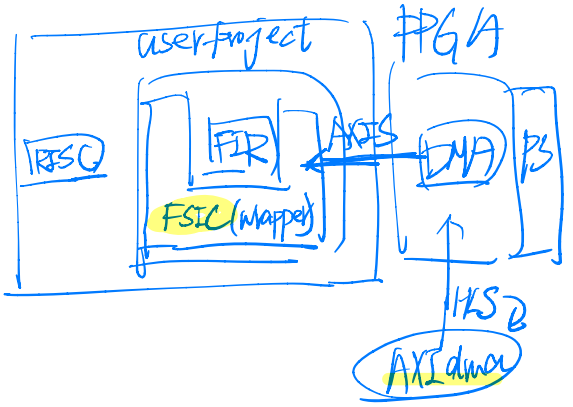
Lab 4-1 Caravel FIR



Final project DMA-FIR



下學期 Caravel



lab 4-2 engine wait

DATA flow ⇒ AXI stream

Reference

- Caravel document
  - https://github.com/efabless/caravel/tree/main/docs

- Management SOC firmware examples (refer to class lecture) – based on mpw-8c branch
  - https://github.com/efabless/caravel/tree/b5010be8a7b89dd52e6da2c6f75f1ab05de43963/verilog/dv/caravel/mgmt_soc