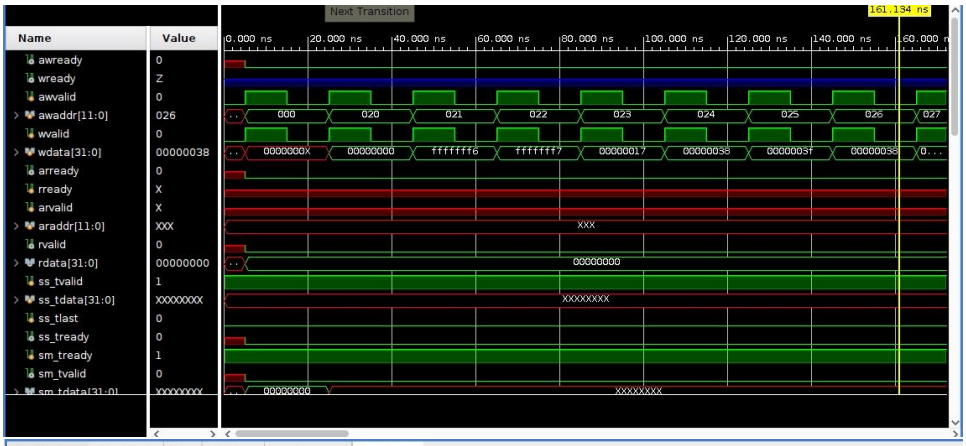
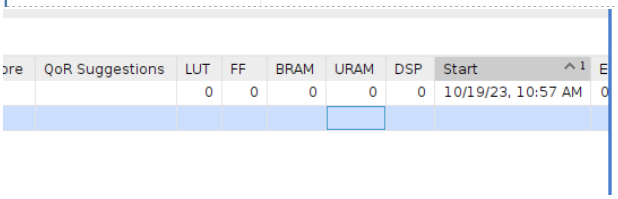

Next Transition
161.134 ns
Name
Value
awready 0
wready Z
awvalid 0
awaddr[11:0] 026
wvalid 0
wdata[31:0] 00000038
arready 0
rready X
arvalid X
araddr[11:0] XXX
rvalid 0
rdata[31:0] 00000000
ss_tvalid 1
ss_tdata[31:0] XXXXXXXX
ss_tlast 0
ss_tready 0
sm_tready 1
sm_tvalid 0
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
000
020
021
022
023
024
025
026
027
00000000
ffffffff6
ffffffff7
00000017
00000038
00000039
00000000
XXXXXXXX

Tcl Console
Messages
Log
Reports
Design Runs
Timing
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Methodology Summary
Check Timing (0)
User Ignored Paths
Unconstrained Paths
Design Timing Summary
Setup
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Hold
Worst Hold Slack (WHS): NA
Total Hold Slack (THS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Pulse Width
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
All user specified timing constraints are met.


QoR Suggestions
LUT
FF
BRAM
URAM
DSP
Start
0
0
0
0
0
10/19/23, 10:57 AM