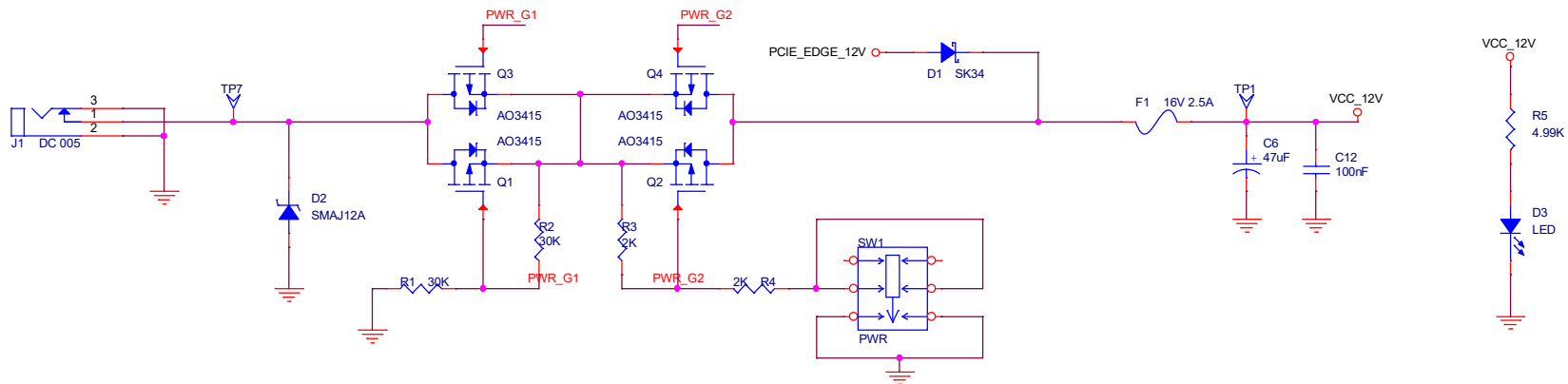


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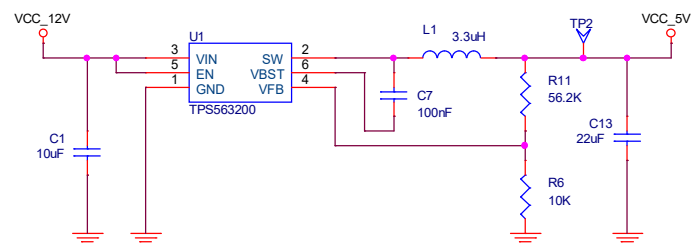
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1	Title, Block Diagram
2	Power 5V & 3V3 & 2V5
3	Power 1.8V & 1.2V & DDR2,DIO,429
4	FPGA Power
5	FPGA Configuration
6	FPGA Bank 3&4
7	FPGA Bank 5&6
8	FPGA Bank 7&8
9	FPGA GXB
10	PCI Express Edge X4
11	DDR2 64M*16bits*2
12	User LEDs and Keys
13	ARINC429 Modules
14	DIO IO Assign
15	Digit Isolate Input 0-15
16	Digit Isolate Input 16-31
17	Digit Isolate Output 0-15
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19	Out Connector
20	
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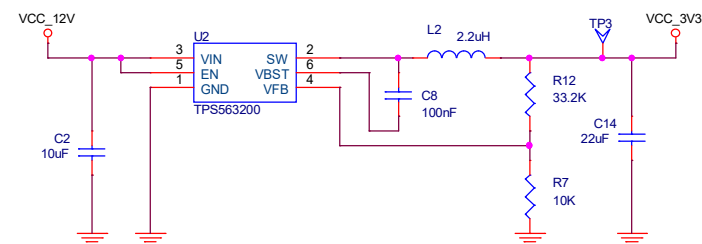
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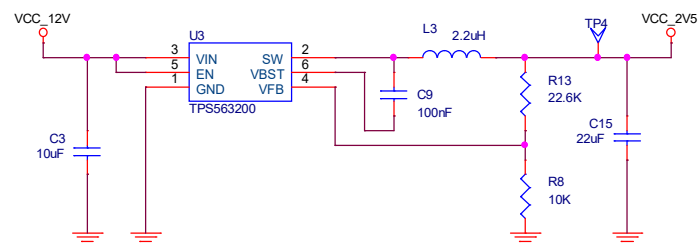
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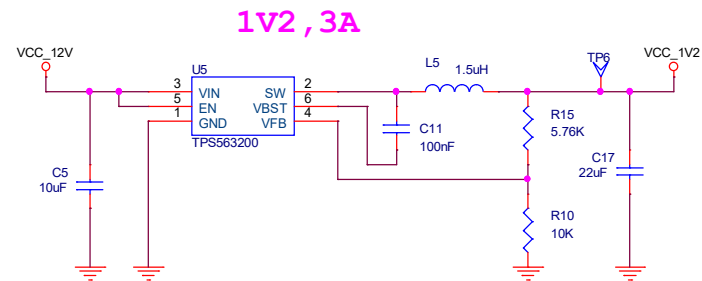
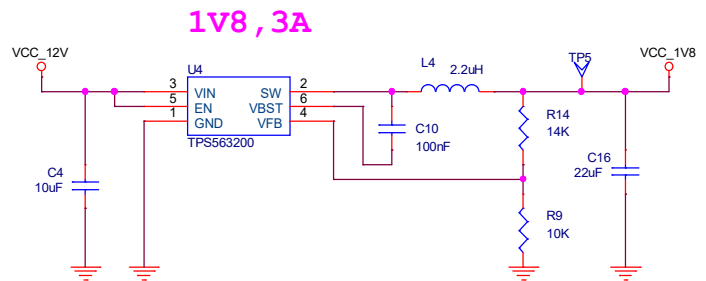
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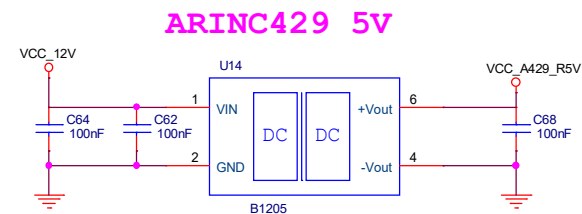
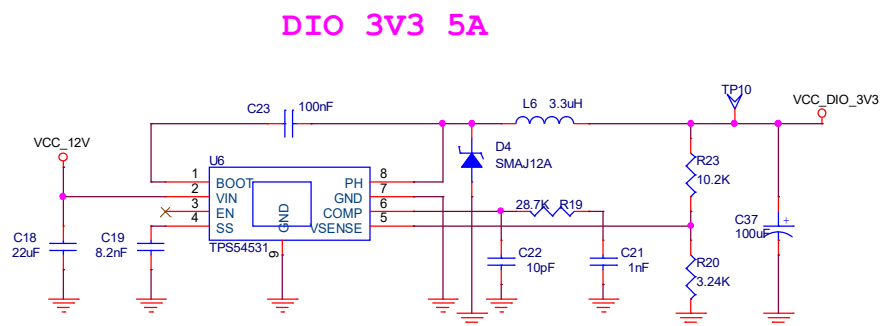
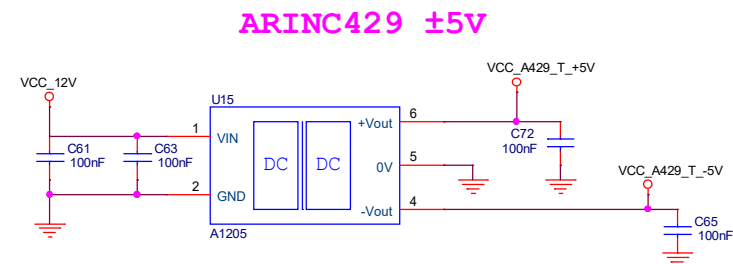
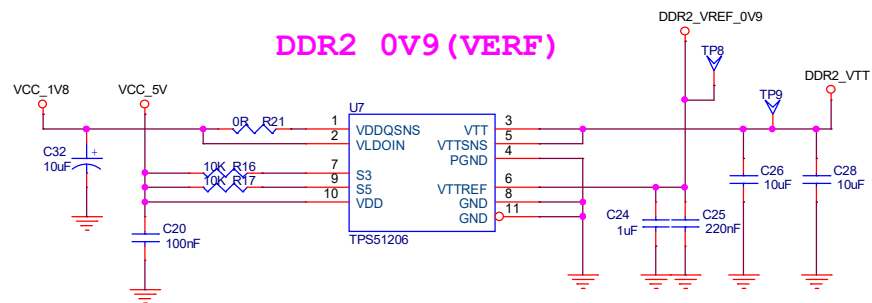
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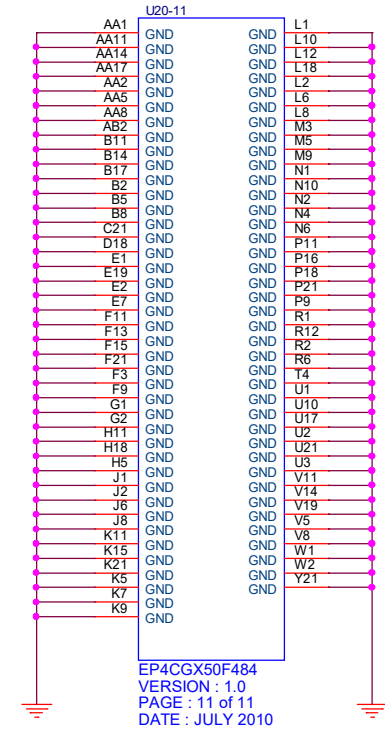
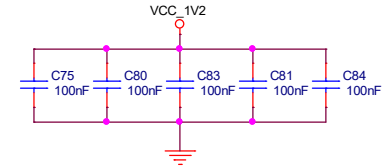
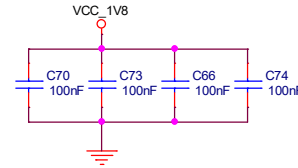
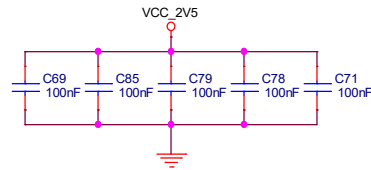
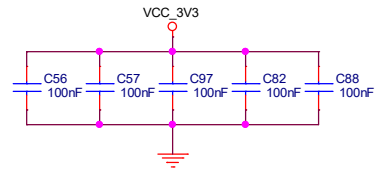
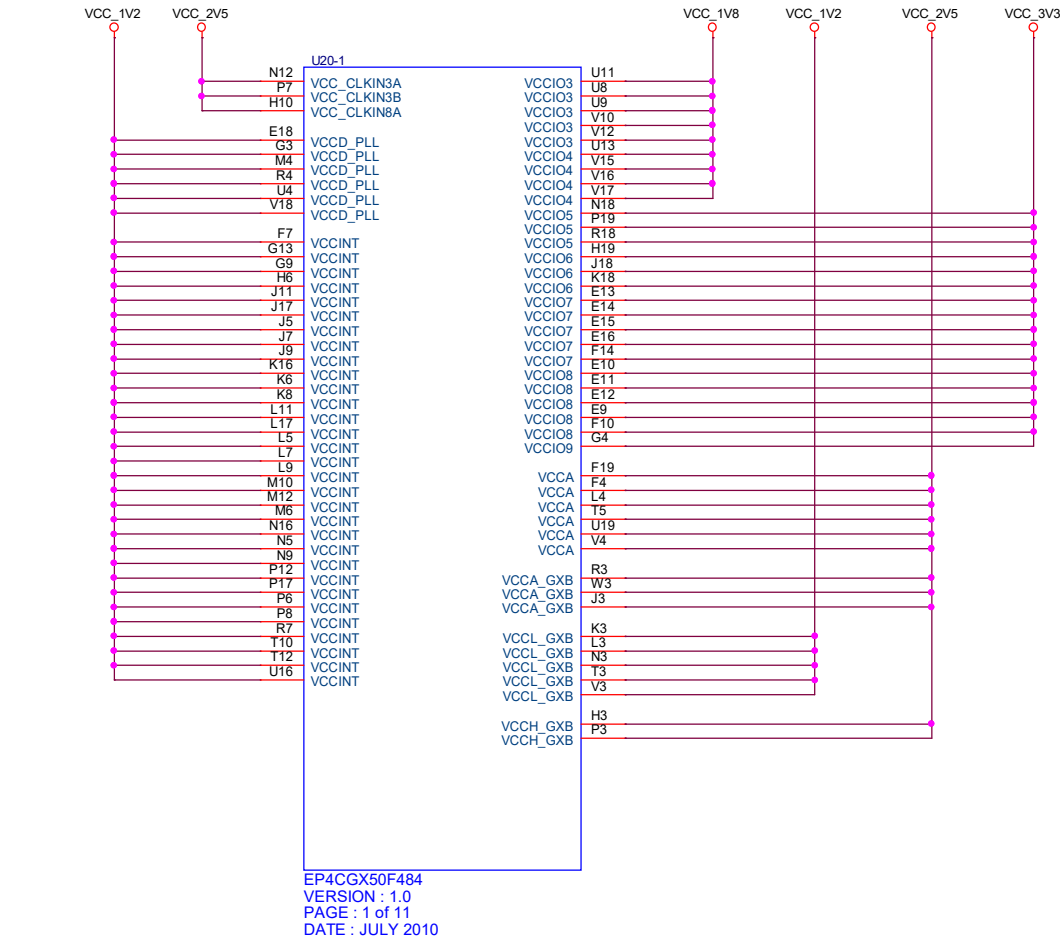


Power 1.8V & 1.2V & DDR2,DIO,429



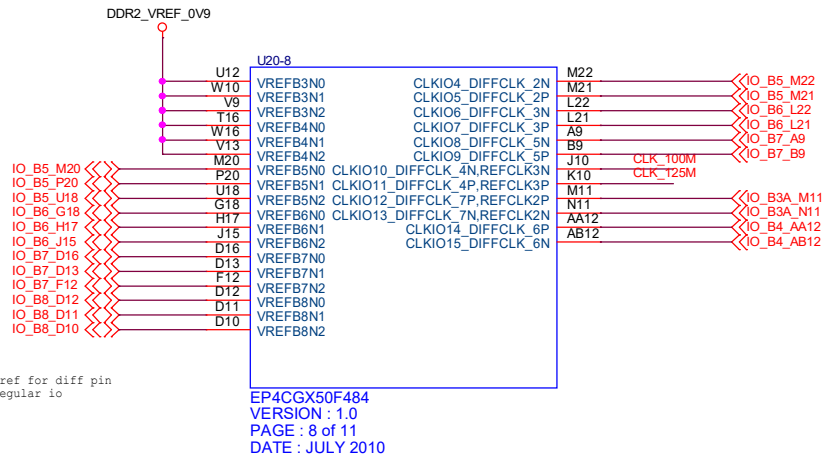
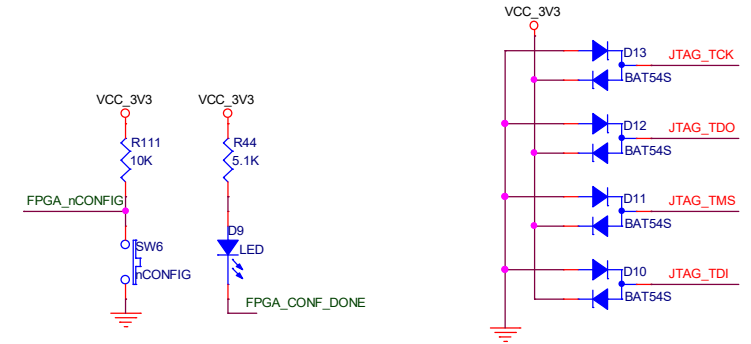
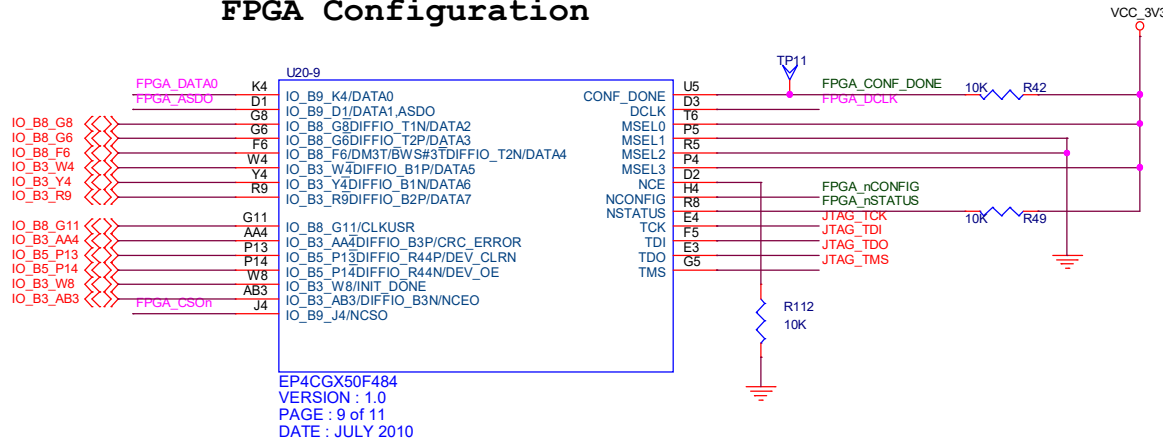
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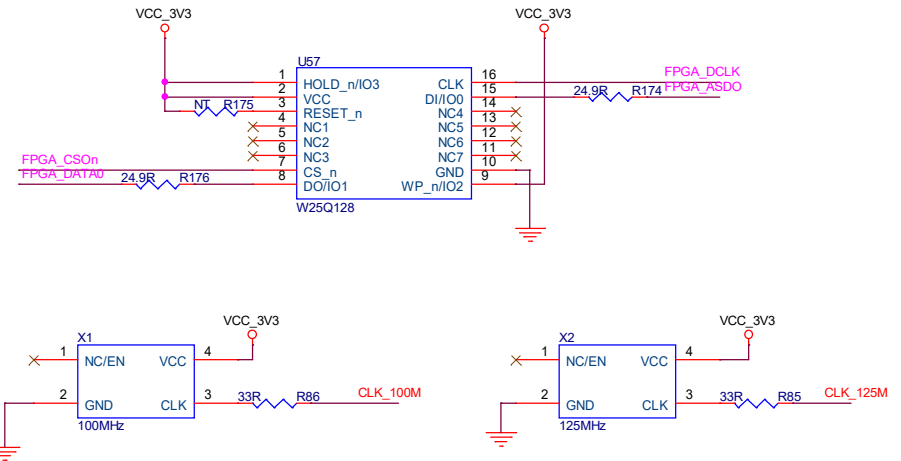
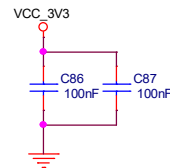
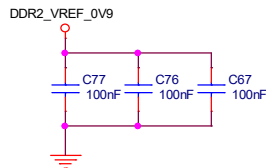


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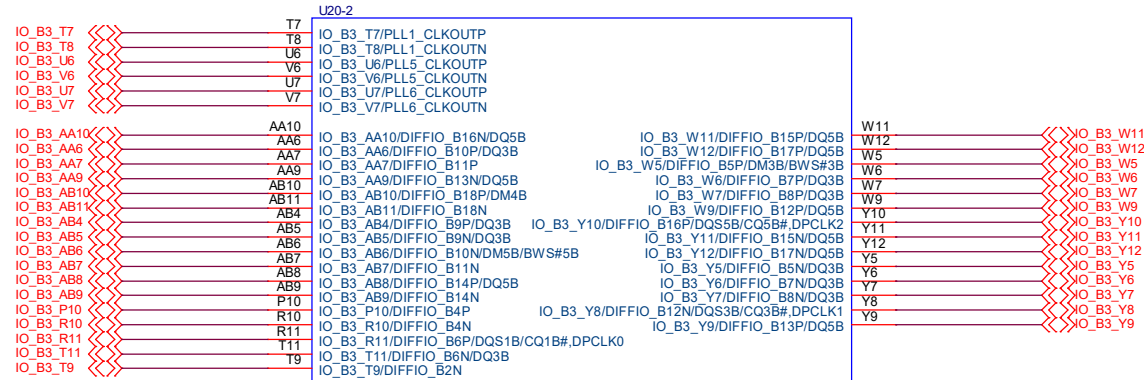


not need Vref for diff pin
used as regular io

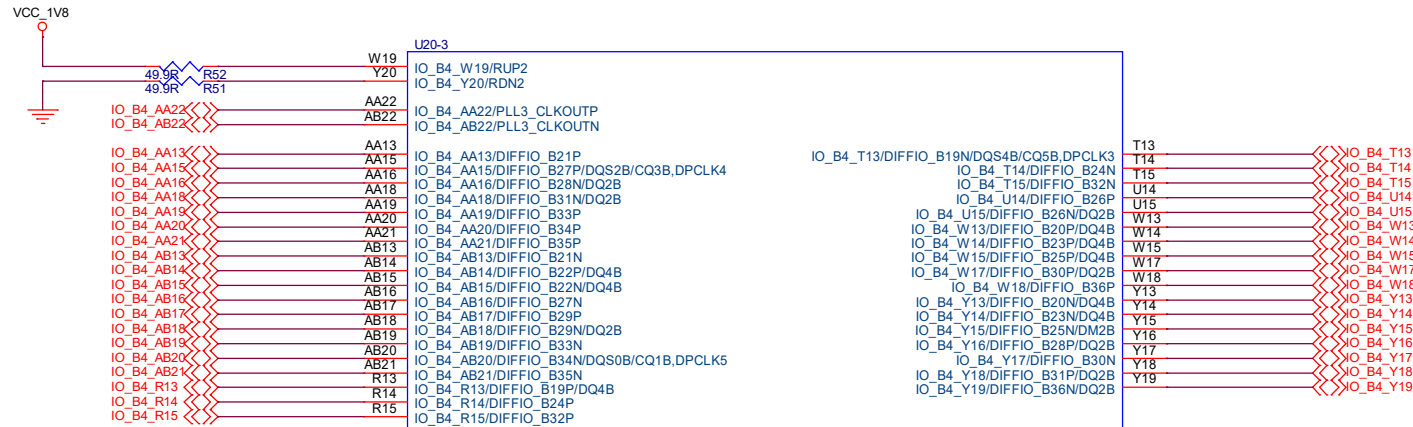


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FPGA Bank 3&4



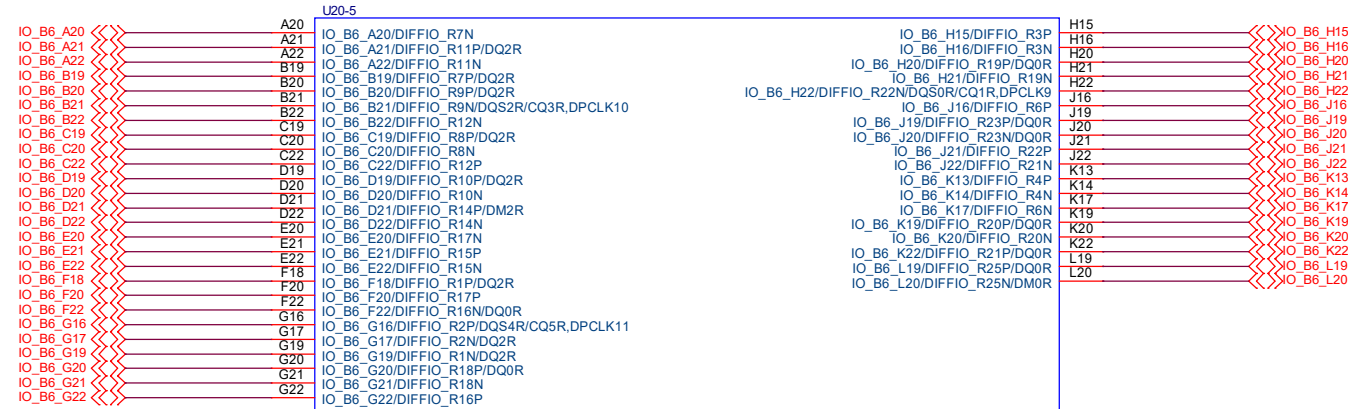
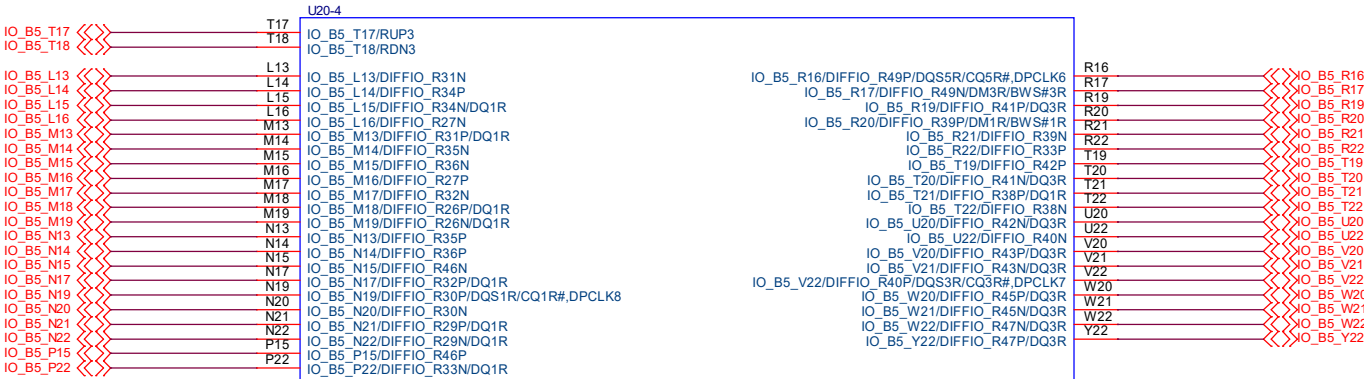
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PAGE : 2 of 11
DATE : JULY 2010



EP4CGX50F484
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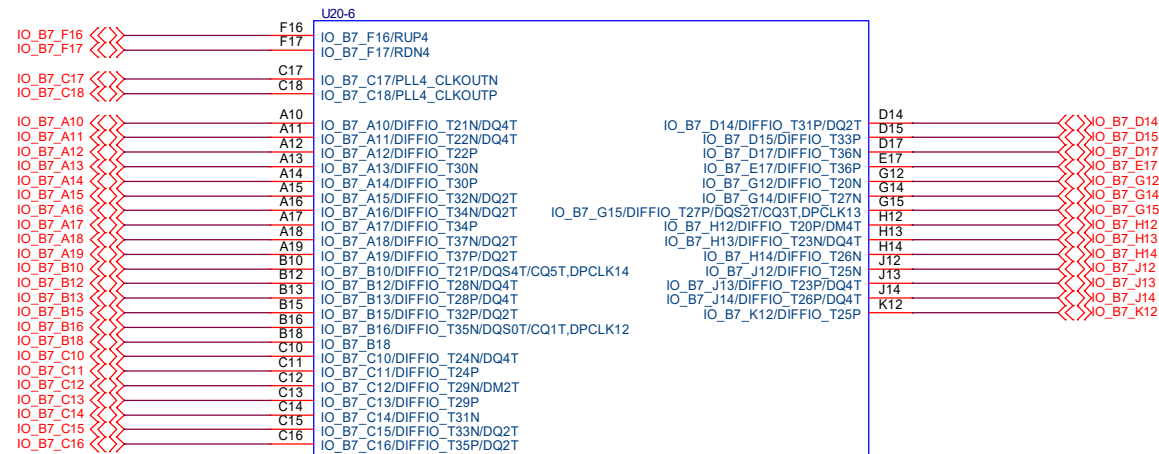
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FPGA Bank 5&6

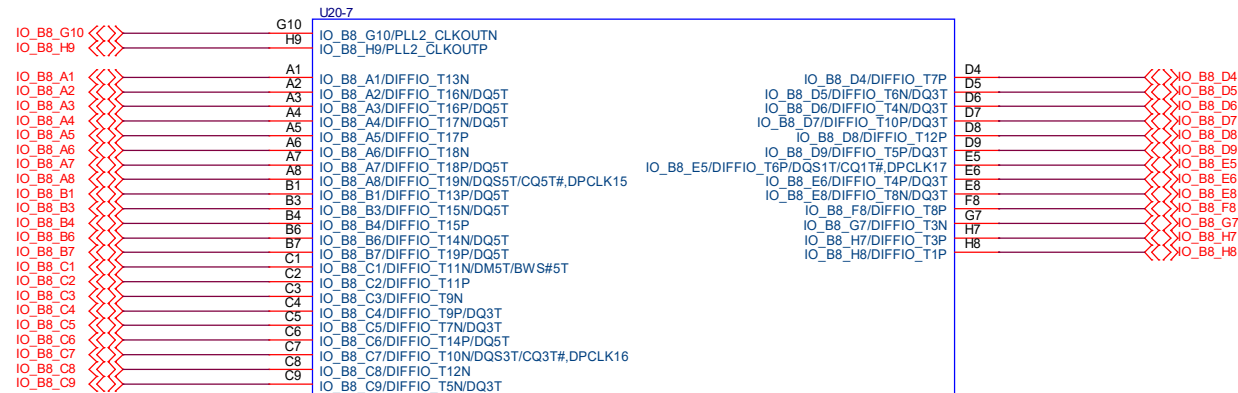


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FPGA Bank 7&8



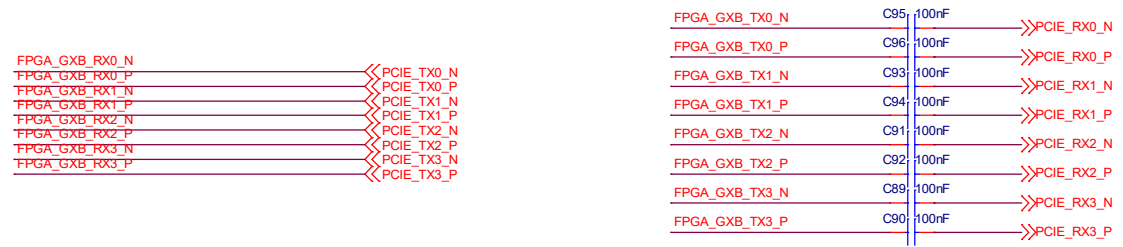
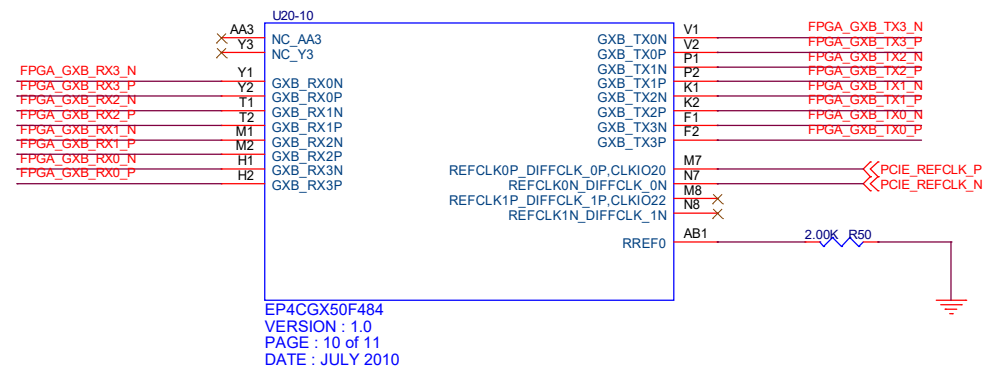
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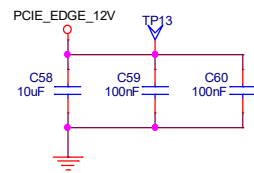
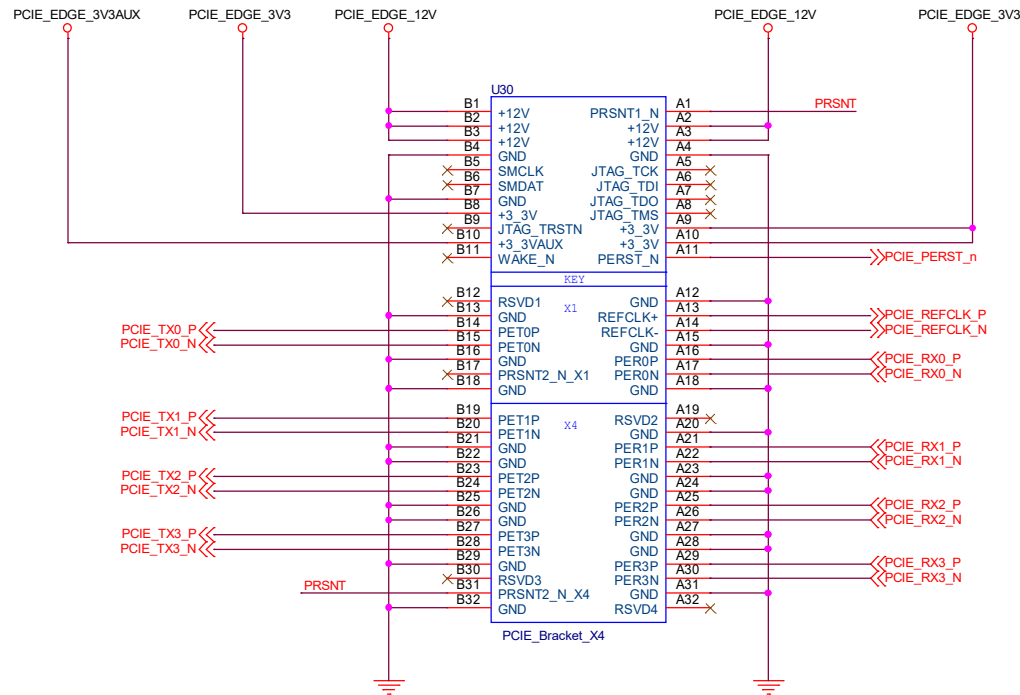
FPGA GXB



FPGA to PCIe interface

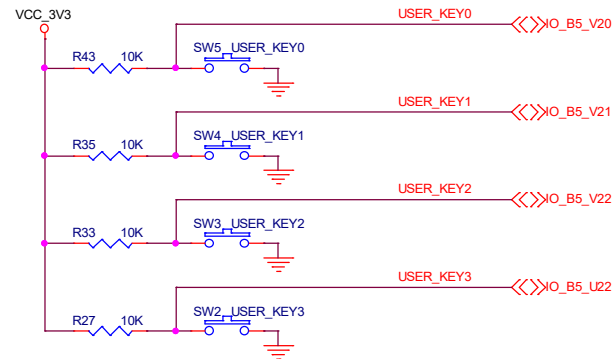
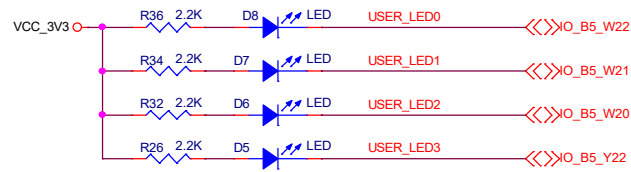
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PCI Express Edge X4



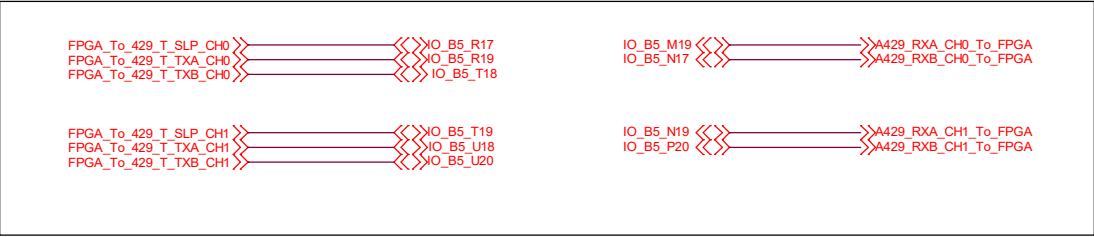
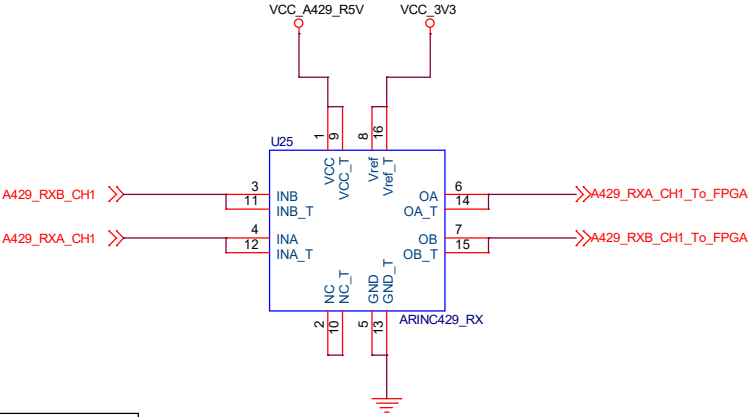
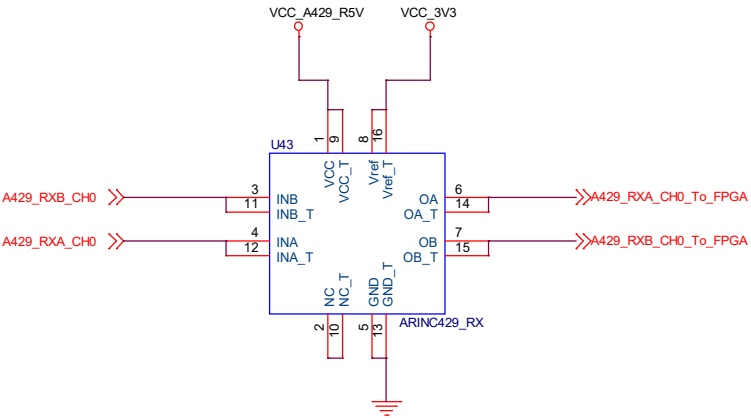
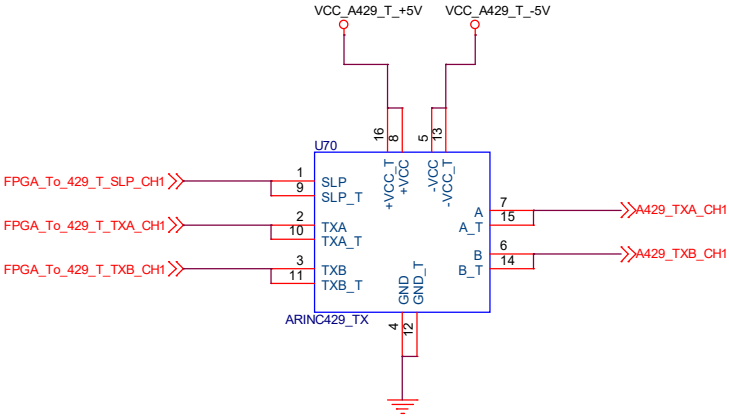
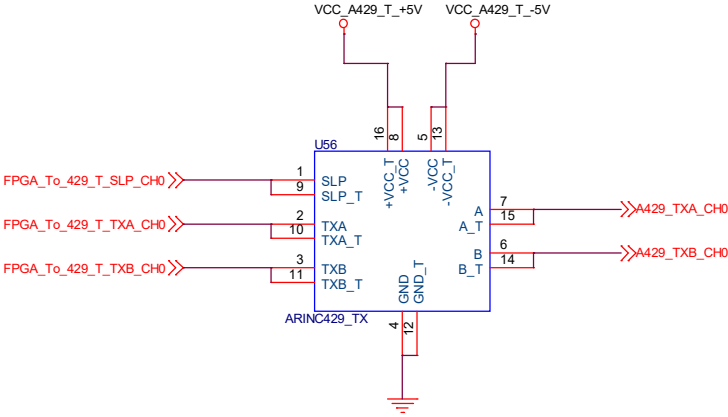
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User LEDs and Keys



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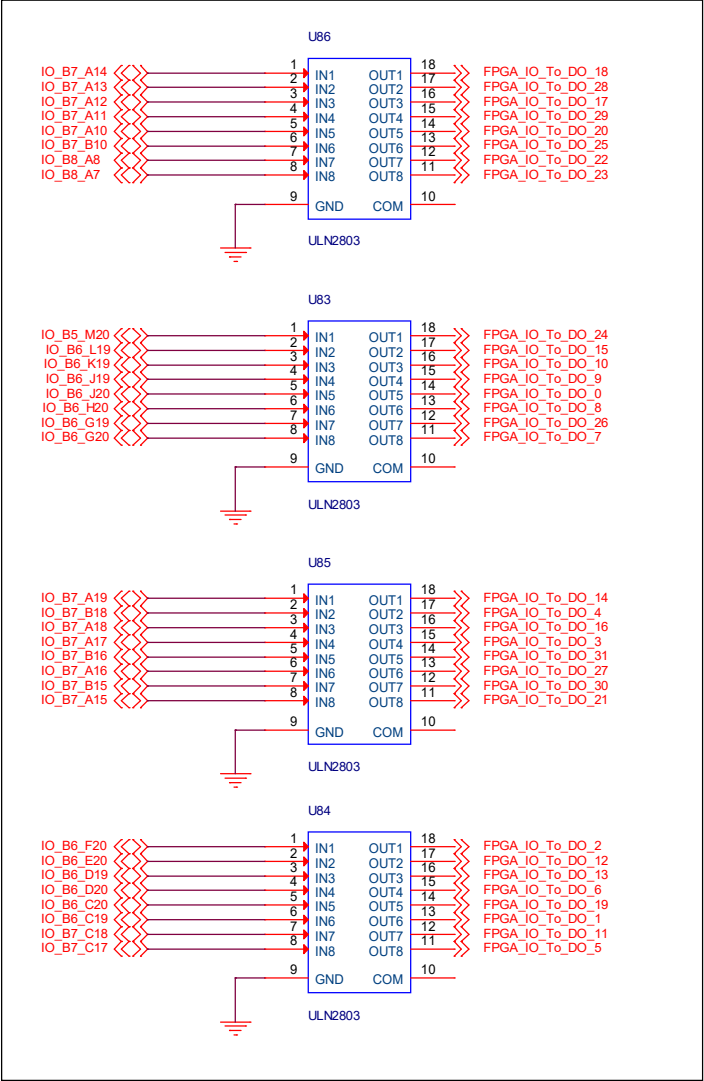
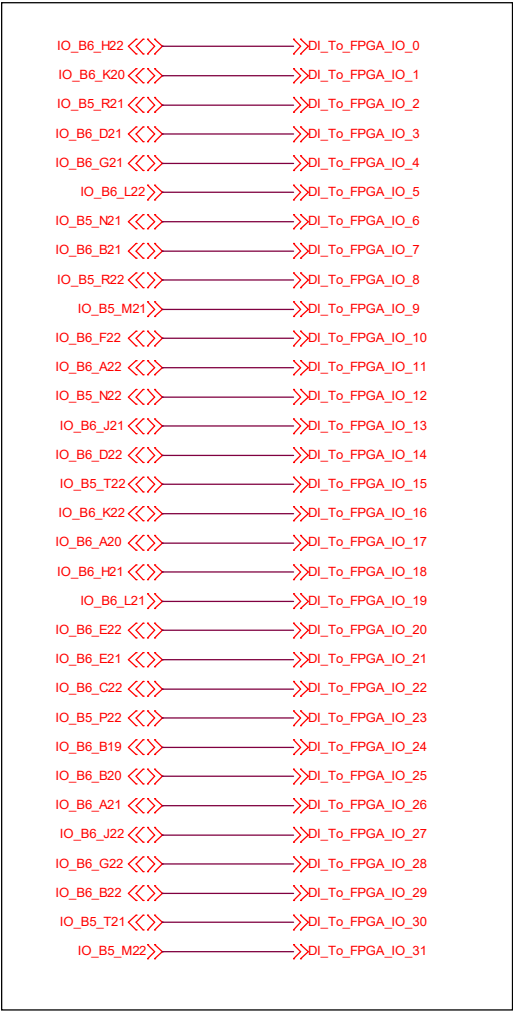
ARINC429 Modules



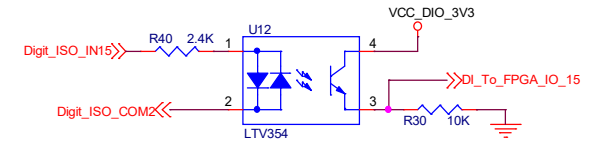
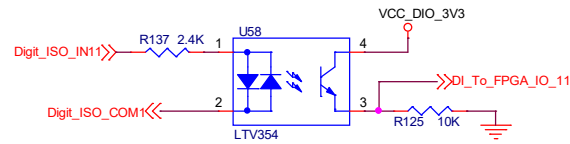
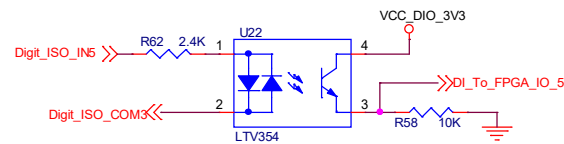
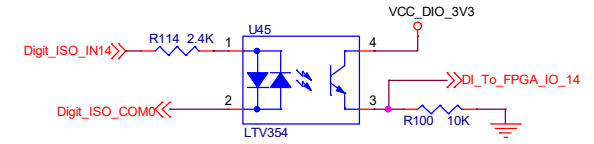
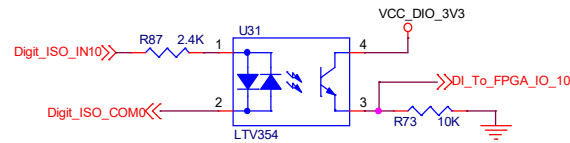
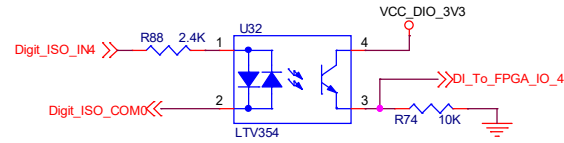
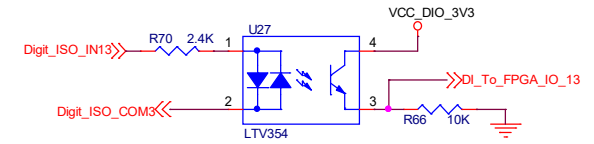
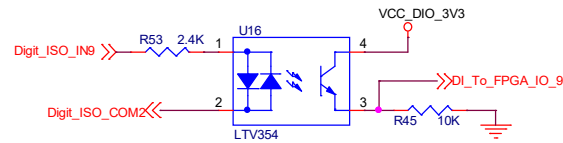
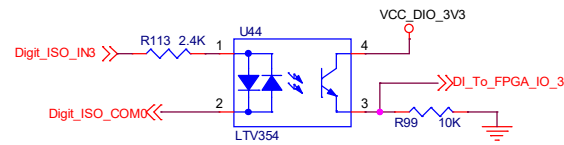
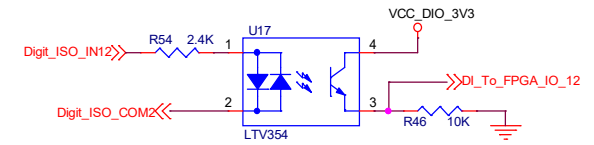
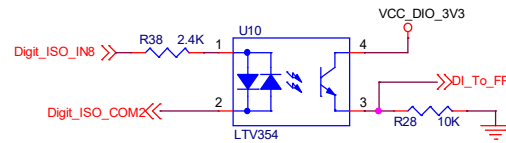
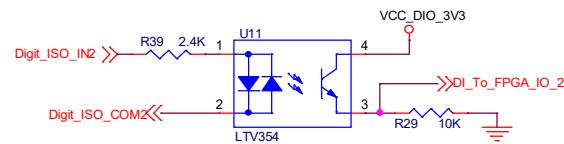
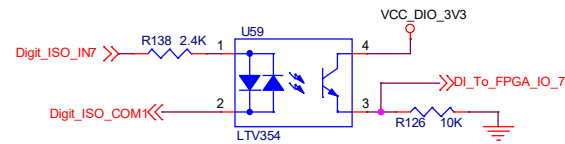
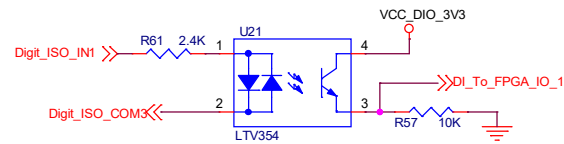
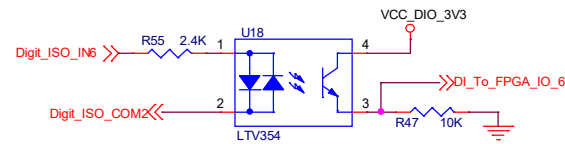
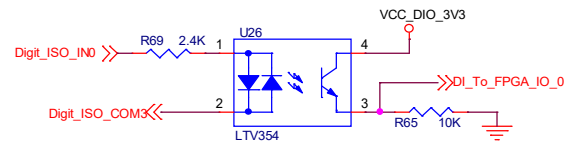
It can used module which make byself
and can used a sop-8 IC such as hi8585,hi8588

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DIO IO Assign

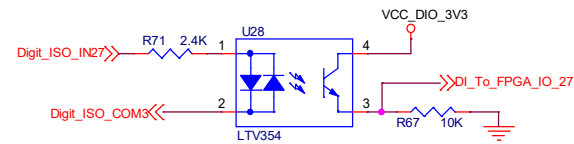
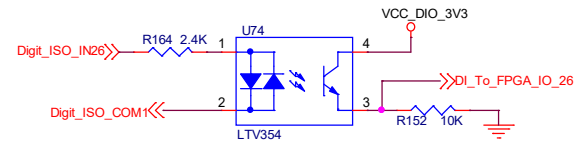
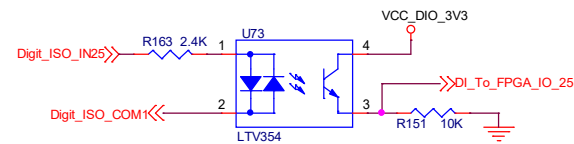
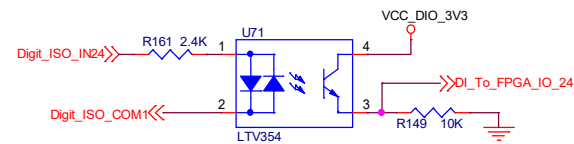
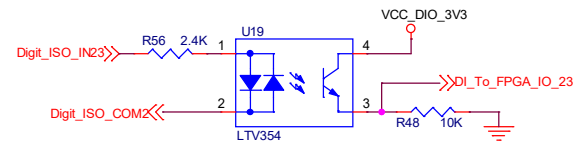
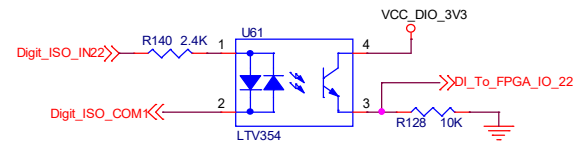
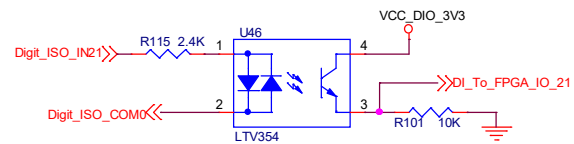
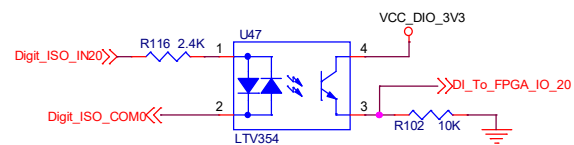
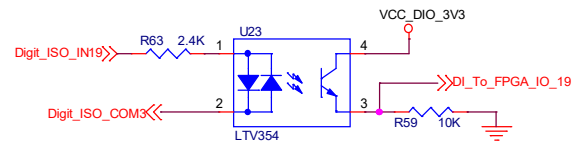
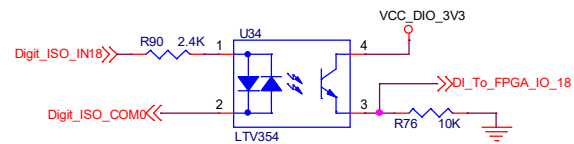
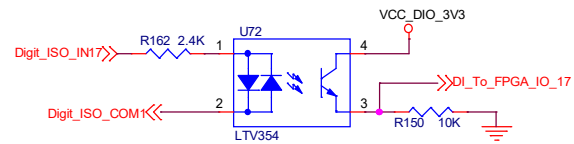
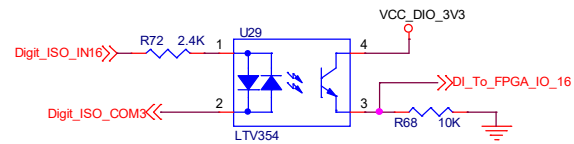


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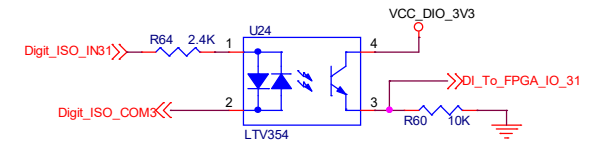
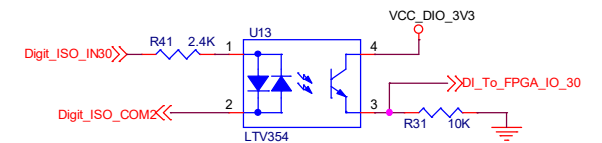
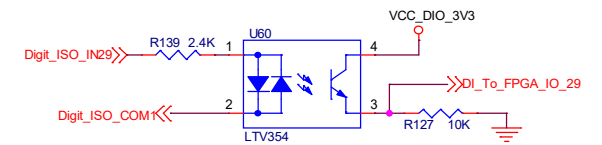
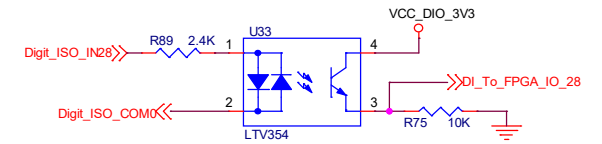


Digit Isolate Input 0-15

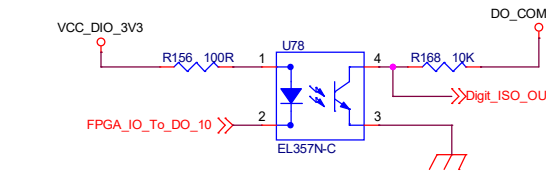
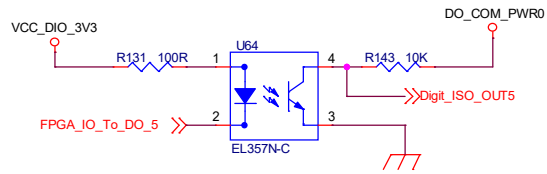
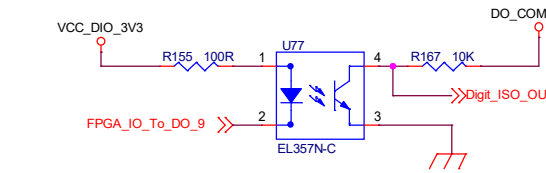
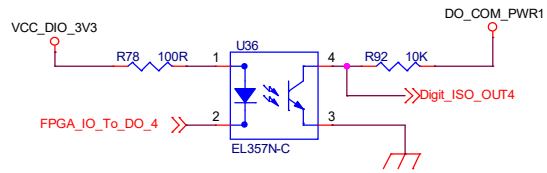
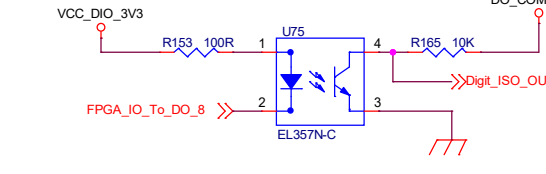
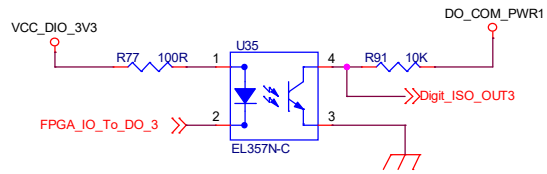
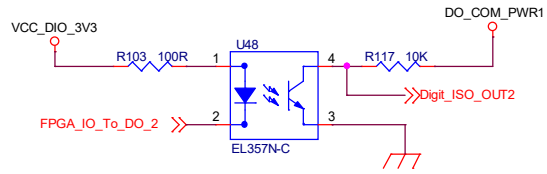
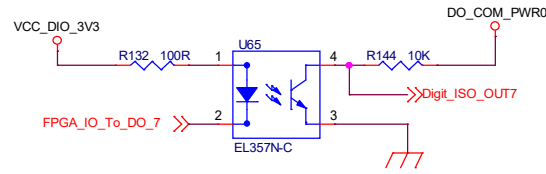
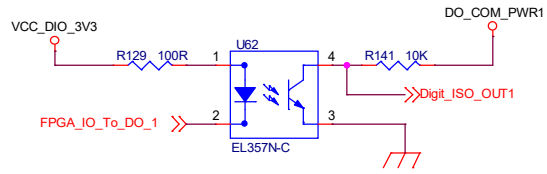
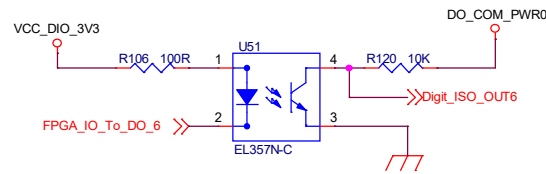
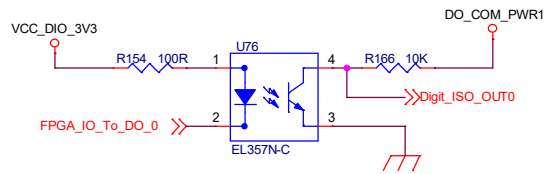
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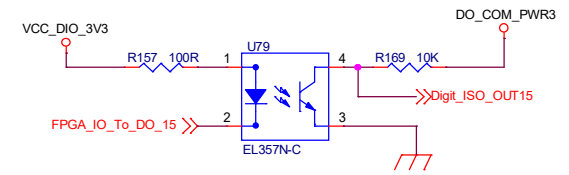
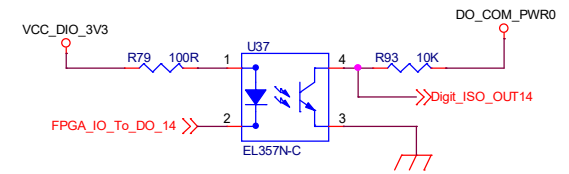
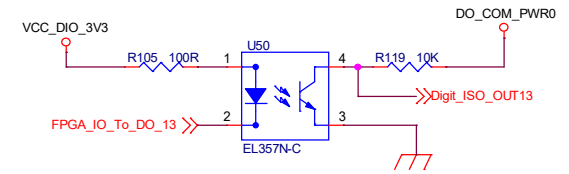
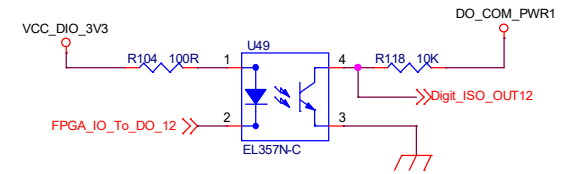
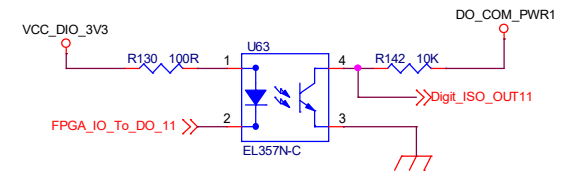
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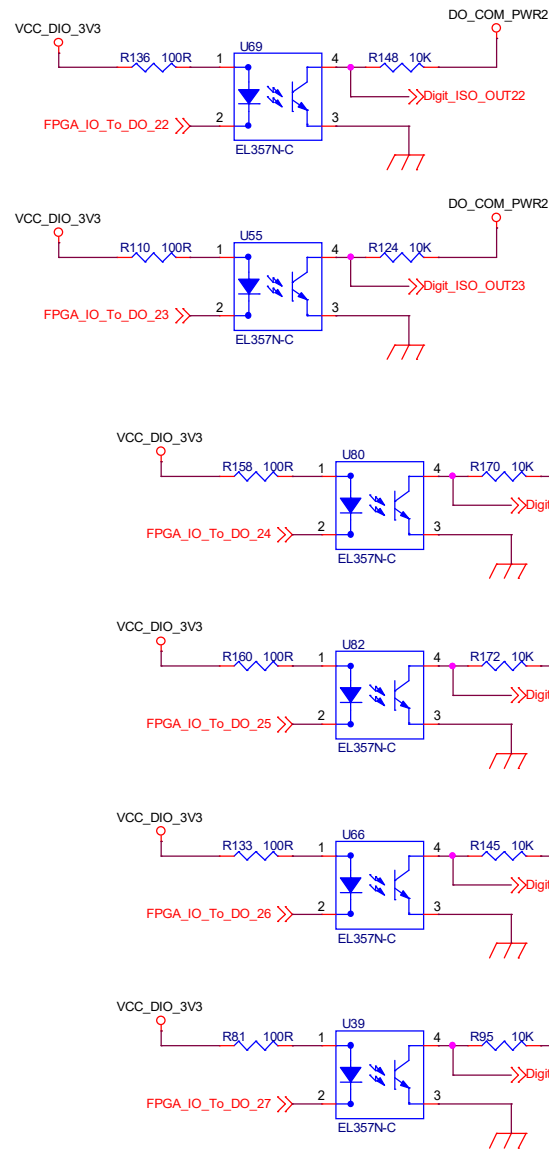
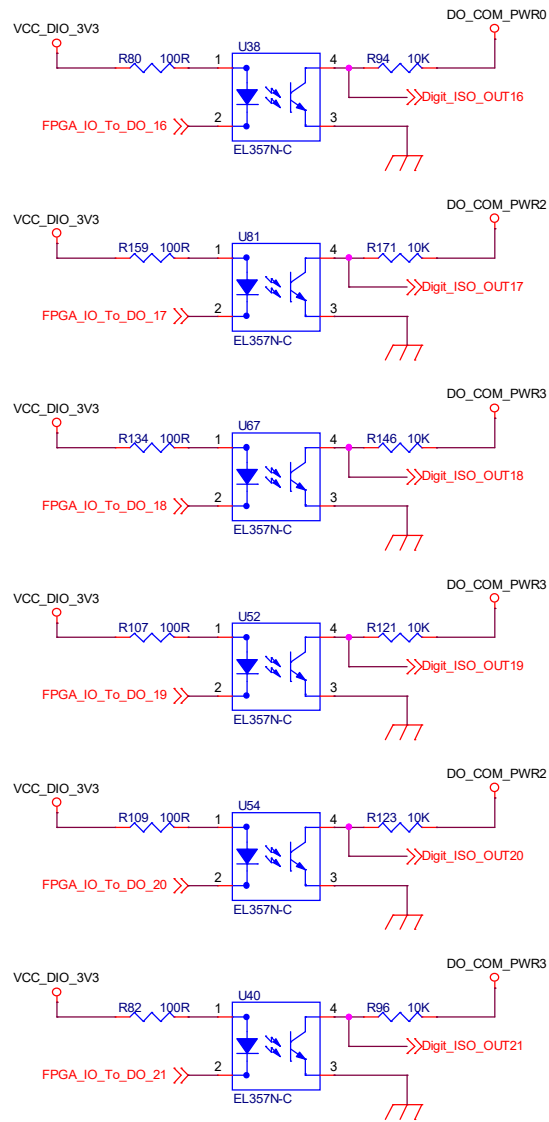
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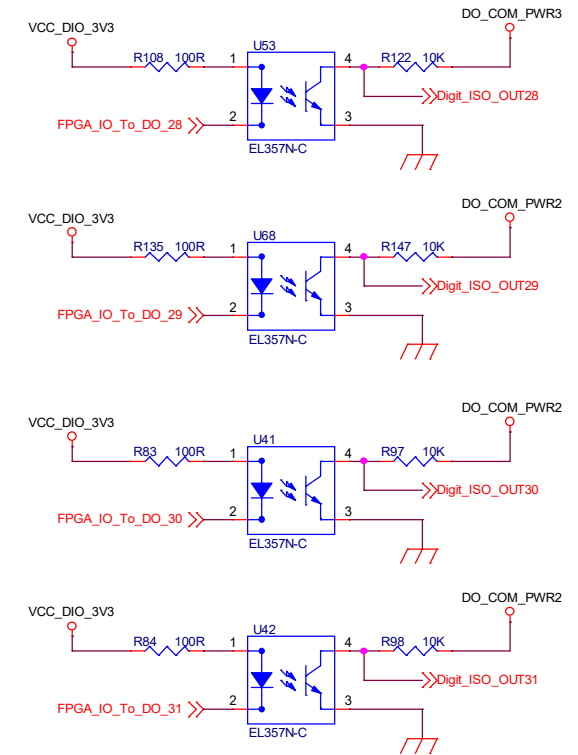
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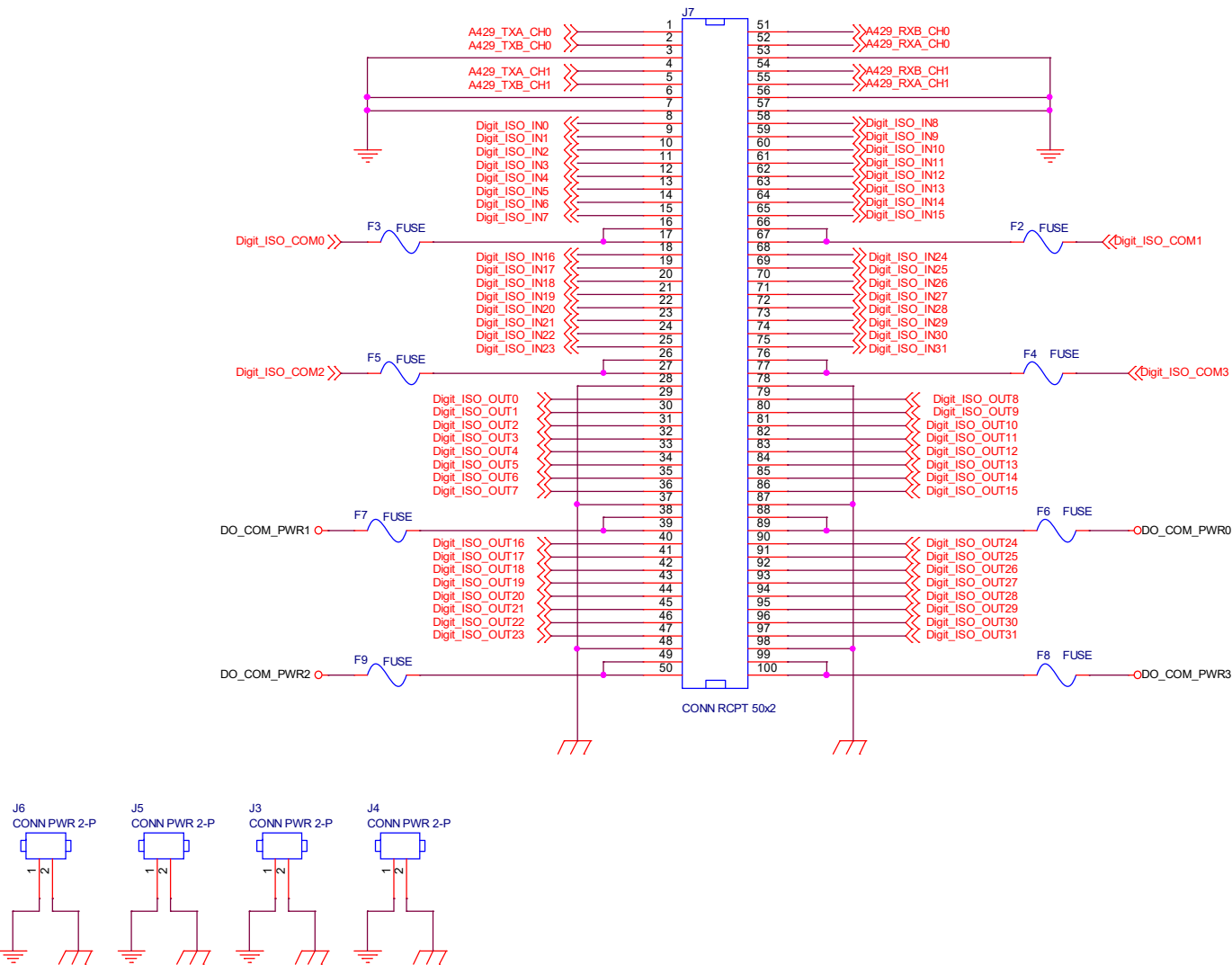


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Out Connector



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