Descripción

Documentación de la placa Alhambra II.

Alhambra II

Open FPGA Board

V1.0A

Clock 12Mhz

USB

FTDI — Serial — FPGA iCE40HX4K — I2C — ADC ADS7924

SPI

FLASH 32Mb

- ⚠ Maximum Supply Voltage: 5.5V
- 👁 Operating Supply Voltage: 3.5 - 5.5V
- ✓ 3.3V GPIO, 5V Compatible
- 👁 Each GPIO Includes a 200 ohm Serial Resistor
- ✓ ADC Internal to External Ref. Automatic Switching

Legend

- Power (red)
- GND (black)
- Serial Pin (light blue)
- Analog Pin (green)
- Control (yellow)
- Bitstream Select (lime)
- Physical Pin (dark gray)
- Icestudio name (cyan)
- Pin name (tan)

Data + Power (1.8A max)

Power Only (3A max)

45	2_73	LED0
44	2_72	LED1
43	2_71	LED2
42	2_64	LED3
41	2_63	LED4
39	2_61	LED5
38	2_57	LED6
37	2_56	LED7

User Switches

| 34 | 3_25B | SW1 |
| 33 | 3_25A | SW2 |

⚠ External Analog Reference: AREF = 3.3V - 5.5V

PERIPHERALS PWR

ON · I/O PWR · OFF

		AREF
		GND
64	2_104	D13	CBSEL_1
63	2_103	D12	CBSEL_0
21	3_14A	D11
22	3_14B	D10
19	3_13A	D9
20	3_13B	D8
9	3_5A	D7
10	3_5B	D6
7	3_4A	D5
8	3_4B	D4
3	3_3A	D3
4	3_3B	D2
1	3_2A	D1
2	3_2B	D0

Voltage Outputs

- RESET
- 3V3
- 5V_P
- GND
- GND
- NC

A0	CH0	A0	0_171	114
A1	CH1	A1	0_172	115
A2	CH2	A2	0_173	116
A3	CH3	A3	0_174	117
SDA	DD4	0_177	118
SCL	DD5	0_178	119

RESET

iCE40 XH 4K (8K)

Alhambra II V1.0A

RESET BUTTON

FTDI

SCK	70	2_107	SCK
SDI	68	2_106	MISO
SDO	67	2_105	MOSI
SS	71	2_108	SS
DONE	65	CDONE	DONE
REST	66	CREST	RES

FTDI

RX	61	2_96	RX
TX	62	2_102	TX
RTS	60	2_95	RTS
CTS	56	2_94	CTS
DTR	52	2_82	DTR
DSR	48	2_80	DSR
DCD	47	2_79	DCD

SIGN — 5V_P — GND

SIGN — 5V_P — GND

👁 Max 4.8A for all 5V_P Pins

| CLK | Clock 12Mhz | 29 | 2_81 |

ADC I²C

Interrupt	90	1_138	ADC_INT
SDA	83	1_119	ADC_SDA
SCL	84	1_120	ADC_SCL

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Made with Inkscape

FPGA wars

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Jedi Knight by University of Hardware

Basado en: Tutorial de Electrónica Digital con FPGAs libres de @Obijuan