EEL 6764 001: Graduate Computer Architecture

Spring 2025

Instructor: Dr. Srinivas Katkoori

**Homework 4**

**Instruction-Level, Data-Level, and Thread-Level Parallelism**

Assigned on Wednesday, 16th April

DUE: 11:59:59PM, Friday, 25th April via Canvas

Upload your solutions in PDF format.

No late work will be accepted.

For some questions, we refer to the exercise problems in the H&P textbook (6th edition). If certain information is not provided, make reasonable assumptions of your own, and use those assumptions to approach the solutions. Make sure that in your solutions, state your assumptions clearly.

1. (15 pts) **Vector Processing** What is the basic idea of a vector processor?
2. (20 pts) **Vector Processing** Draw the block diagram of RISC-V Vector architecture. Briefly explain the various blocks in the architecture.
3. (20 pts) **Vector Processing** With an example, explain the basic idea of the following techniques:
   1. Vector chaining
   2. Strip Mining
   3. Vector Stride
   4. Gather and Scatter
4. (20 pts) **Snooping Protocol** Problem 5.1 parts (a), (b), (c) (Pages 446-447)
5. (15 pts) **Coherence Protocols** Explain how the following protocols work:
   1. Snooping coherence protocol
   2. Directory based coherence protocol.
6. (10 pts) **Directory Protocol** 
   1. Using a state-diagram like figure, show how a **read miss** from local node is handled by the home node and remote node. Briefly explain how it works.
   2. Using a state-diagram like figure, show how a **write miss** from local node is handled by the home node and remote node. Briefly explain how it works.

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