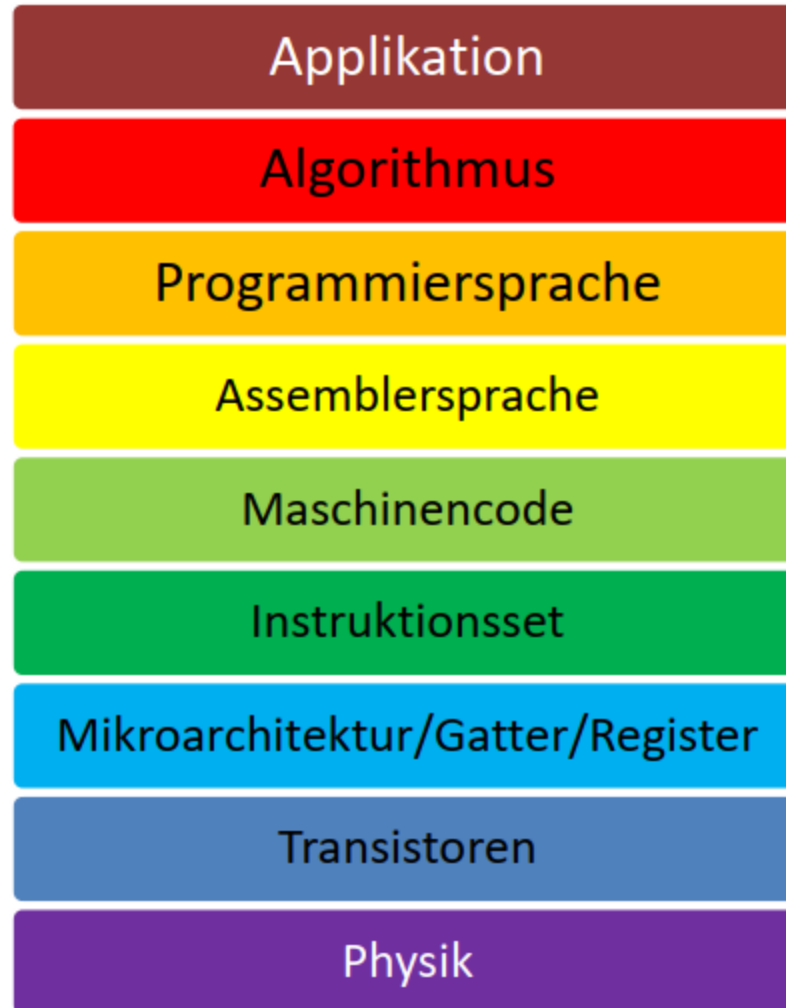


Microcomputertechnik

Überblick



Software

TIOBE Programming Community Index

Source: www.tiobe.com





Ken Thompson, Dennis Ritchie

C Keywords (Auswahl)

bool (C23)	extern	sizeof	default	return
false (C23)	float	static	do	volatile
break	for	struct	double	short
case	goto	switch	else	signed
char	if	true (C23)	unsigned	register
const	int	typedef	void	union
continue	long			

Python Keywords

False	await	else	import	pass
None	break	except	in	raise
True	class	finally	is	return
and	continue	for	lambda	try
as	def	from	nonlocal	while
assert	del	global	not	with
async	elif	if	or	yield

Go Keywords

break	default	func	interface	select
case	defer	go	map	struct
chan	else	goto	package	switch
const	fallthrough	if	range	type
continue	for	import	return	var

<https://go.dev/ref/spec#Keywords>

Hochsprache zu Maschinencode

Rust

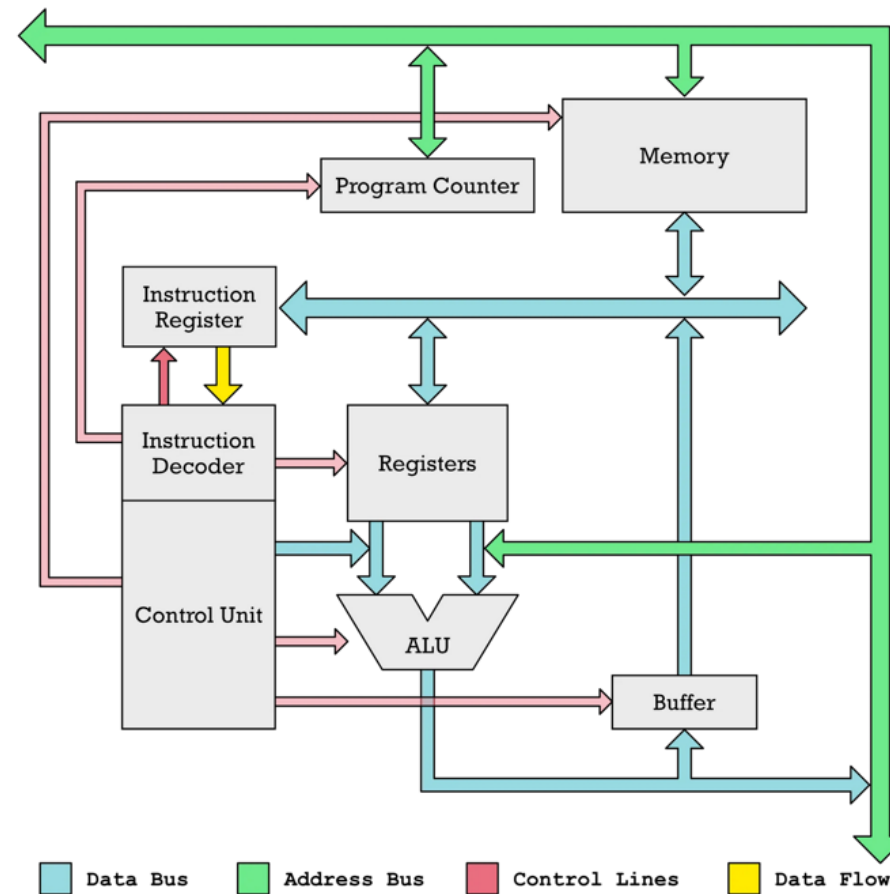
```
pub fn square(num: i32) -> i32 {  
    num * num  
}
```

Assembler

```
square:
    push    {r7, lr}
    sub     sp, #8
    smull   r1, r0, r0, r0
    mov     r2, r1
    str     r2, [sp, #4]
    cmp.w   r0, r1, asr #31
    bne     .LBB0_2
    b       .LBB0_1
.LBB0_1:
    ldr     r0, [sp, #4]
    add     sp, #8
    pop     {r7, pc}
.LBB0_2:
    ldr     r0, .LCPI0_0
.LPC0_0:
    add     r0, pc
    ldr     r2, .LCPI0_1
.LPC0_1:
    add     r2, pc
    movs    r1, #33
    bl      core::panicking::panic
    .inst.n 0xdefe
.LCPI0_0:
    .long   str.0-(.LPC0_0+4)
.LCPI0_1:
    .long   .L__unnamed_1-(.LPC0_1+4)
.L__unnamed_2:
    .ascii  "/app/example.rs"
.L__unnamed_1:
    .long   .L__unnamed_2
    .asciz  "\017\000\000\000\013\000\000\000\005\000\000"

str.0:
    .ascii  "attempt to multiply with overflow"
```

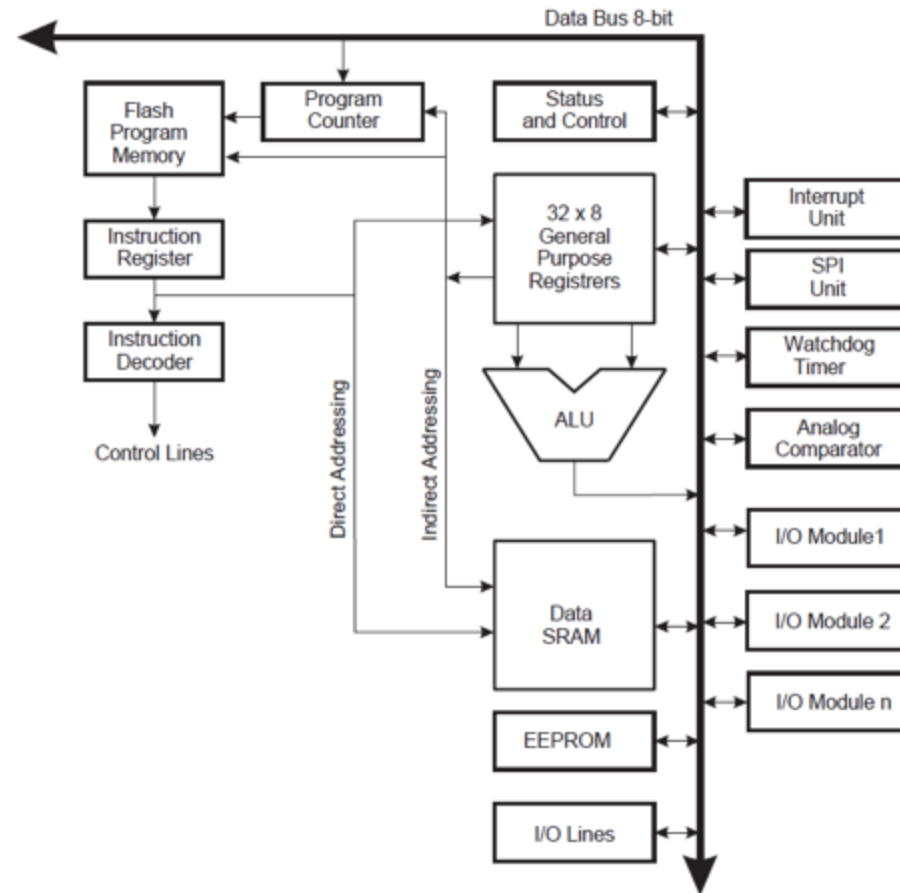
Aufbau und Funktion eines Microprozessors



Decoding instruction located in instruction register.

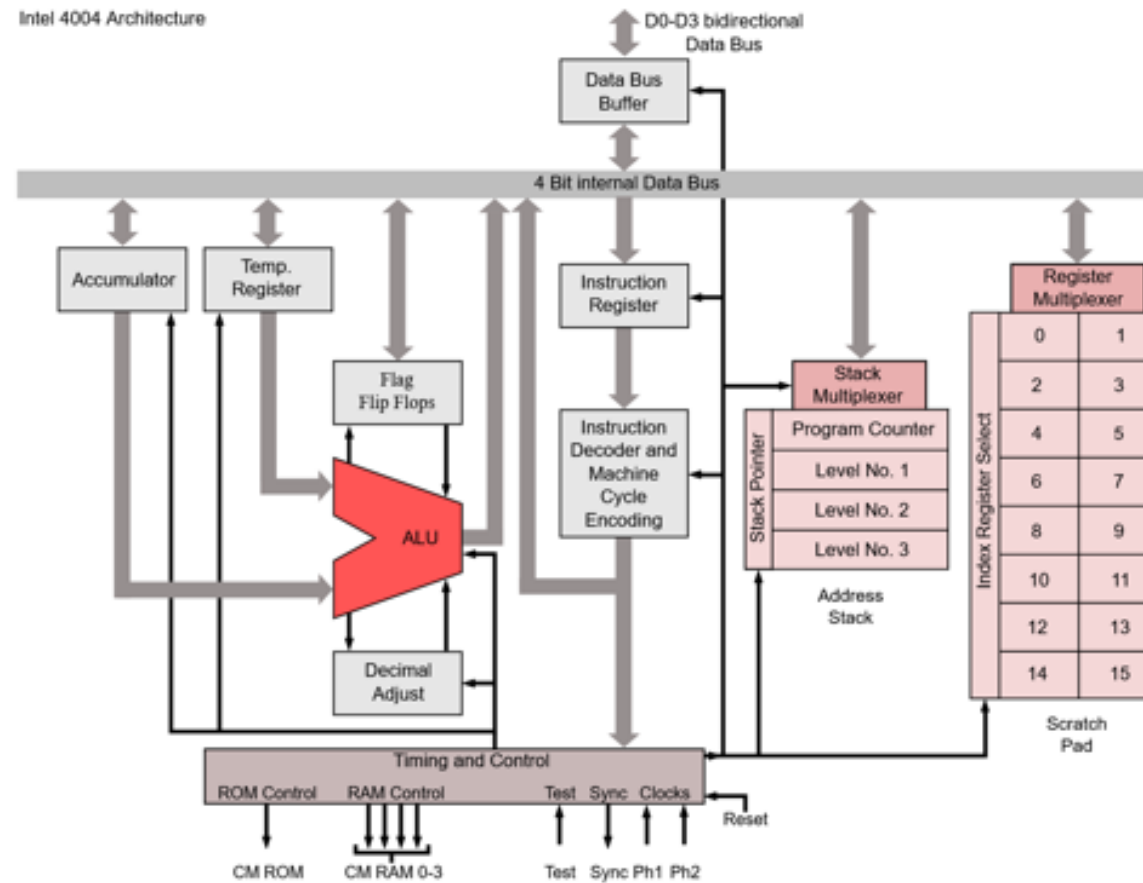
<https://erik-engheim.medium.com/how-does-a-microprocessor-run-a-program-11744ab47d04>

AVR Architektur Blockschaltbild

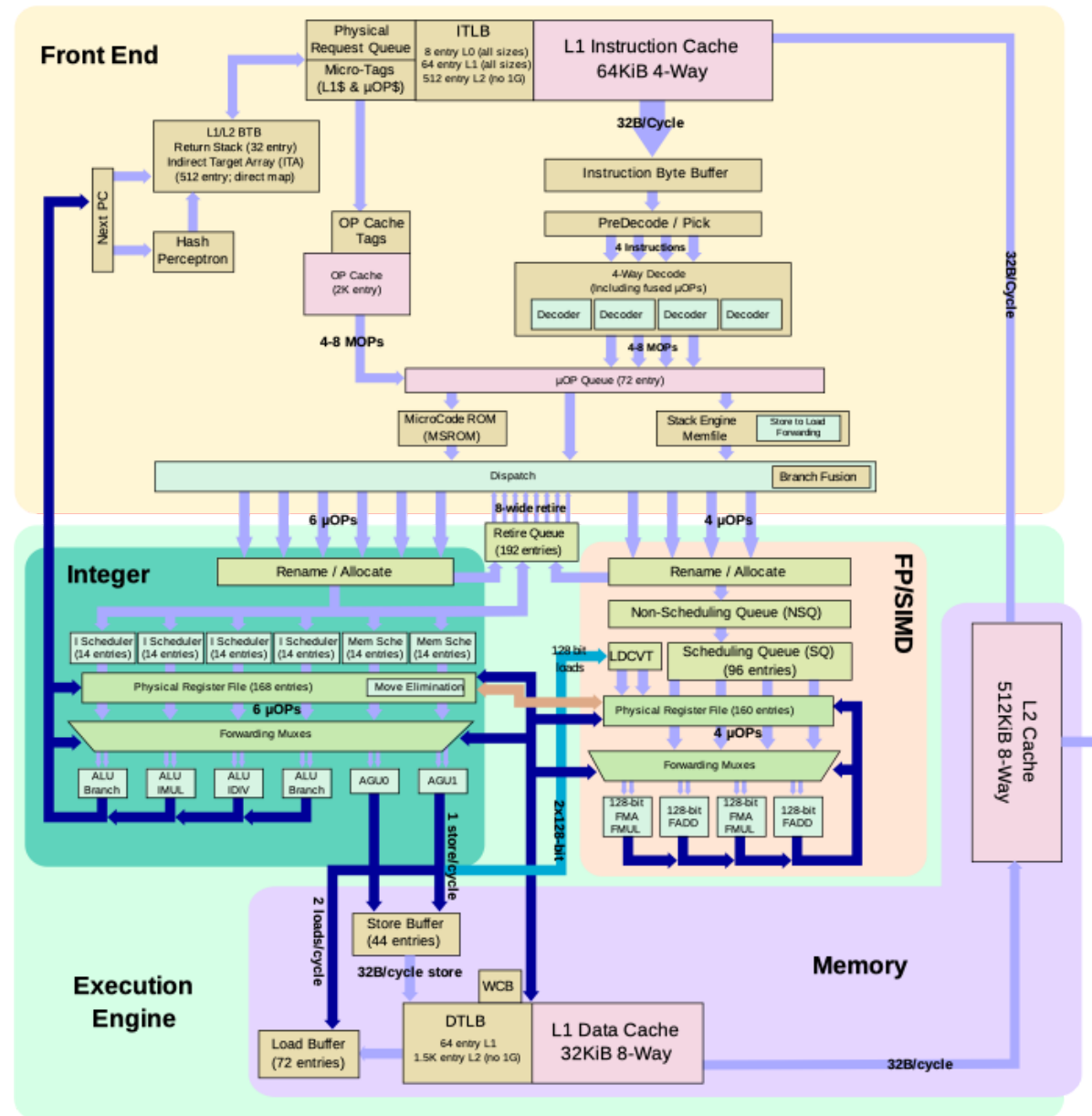


1971: Intel 4004

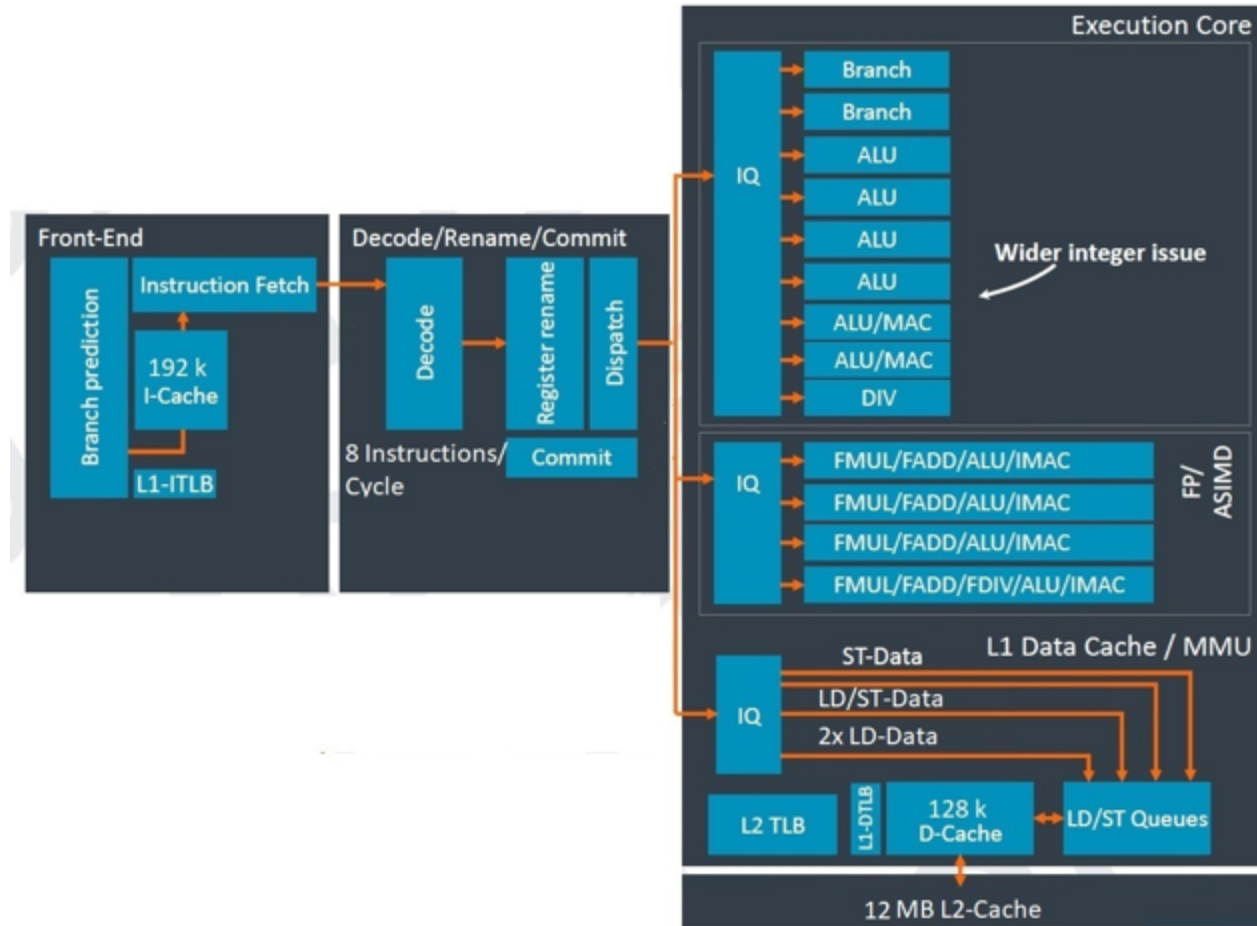
Intel 4004 Architecture



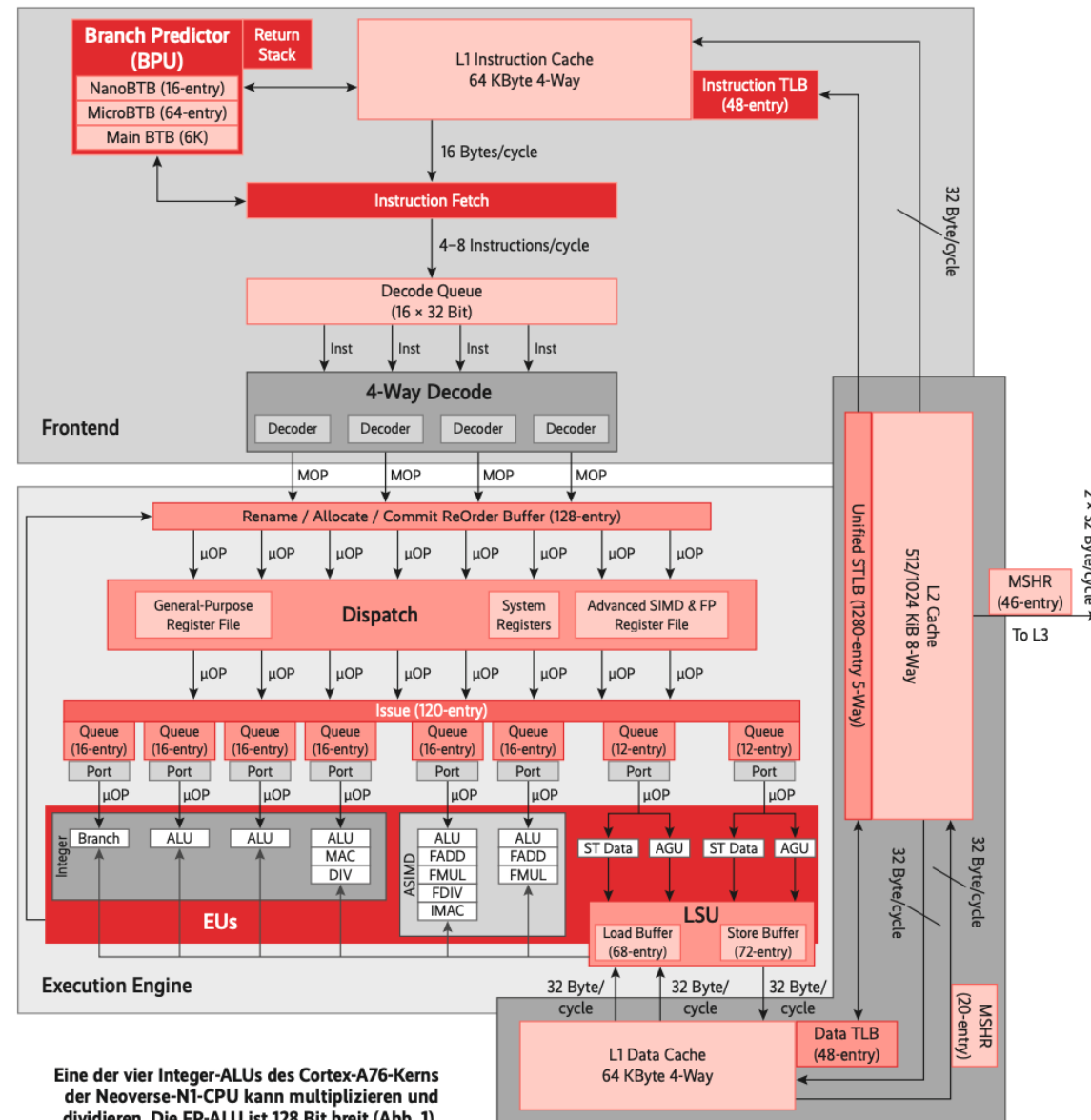
AMD Threadripper



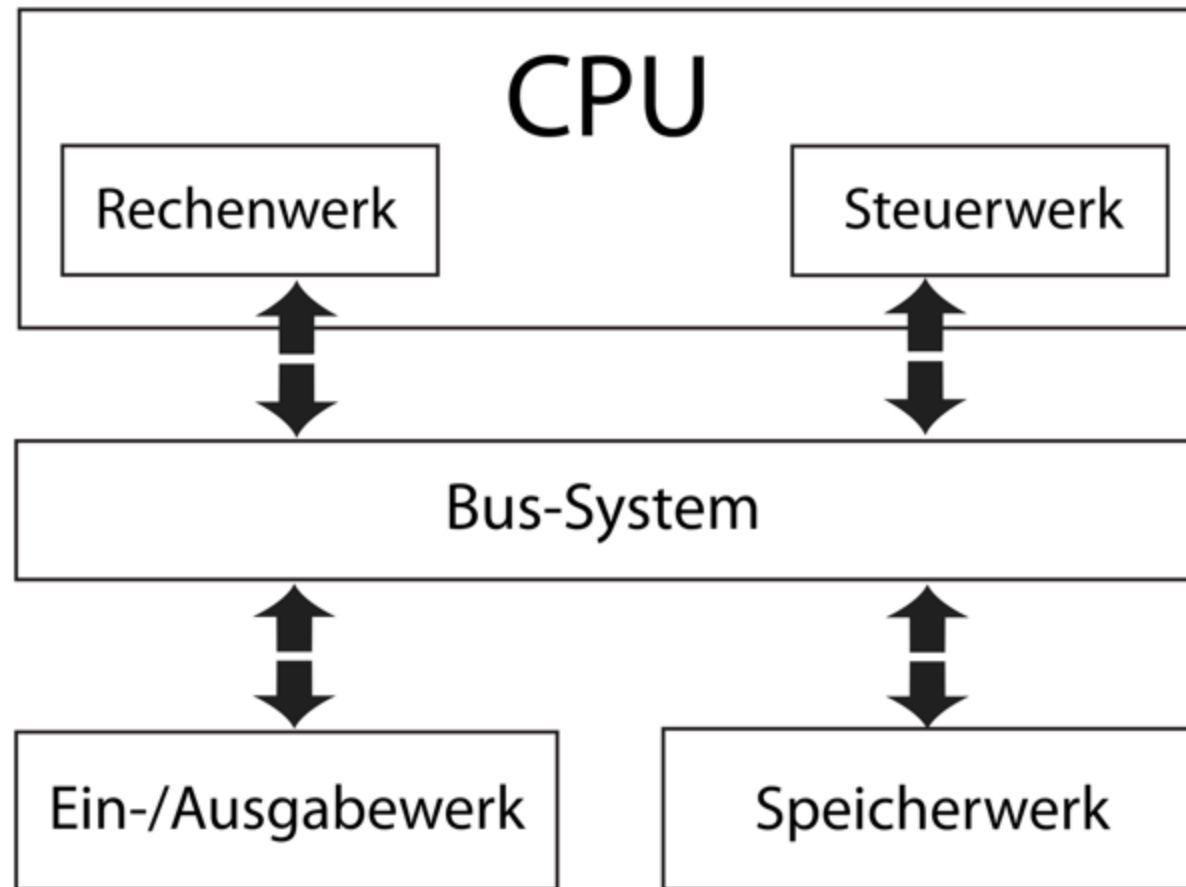
Apple M1



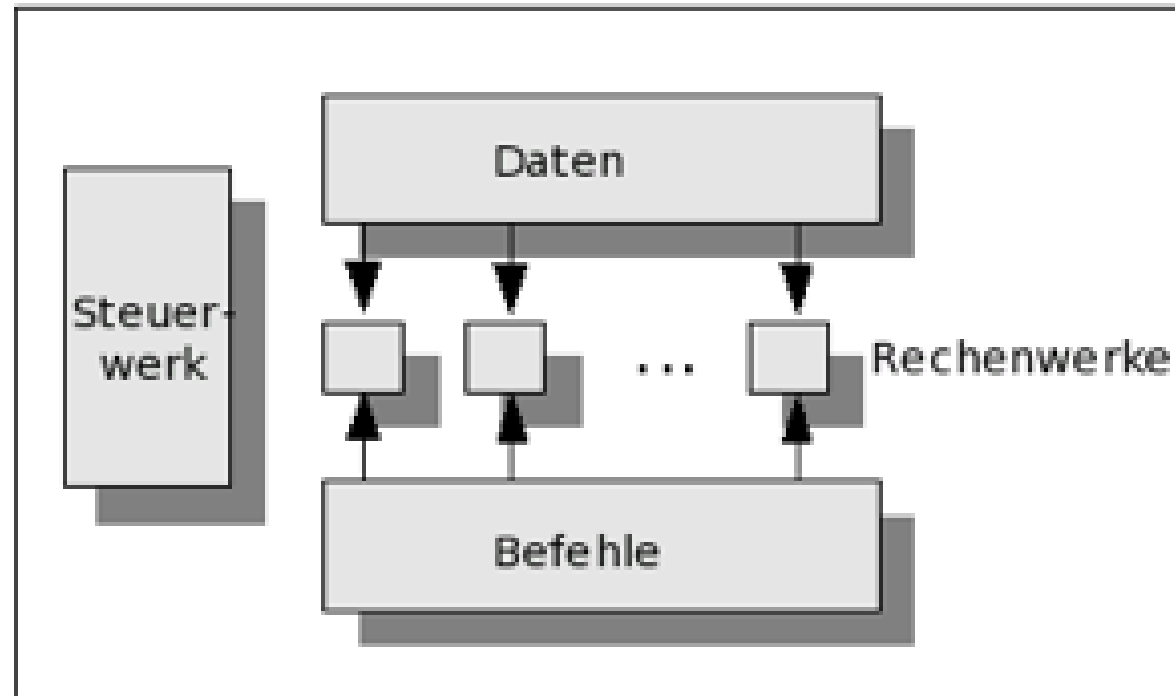
ARM Cortex A67



von Neumann Architektur

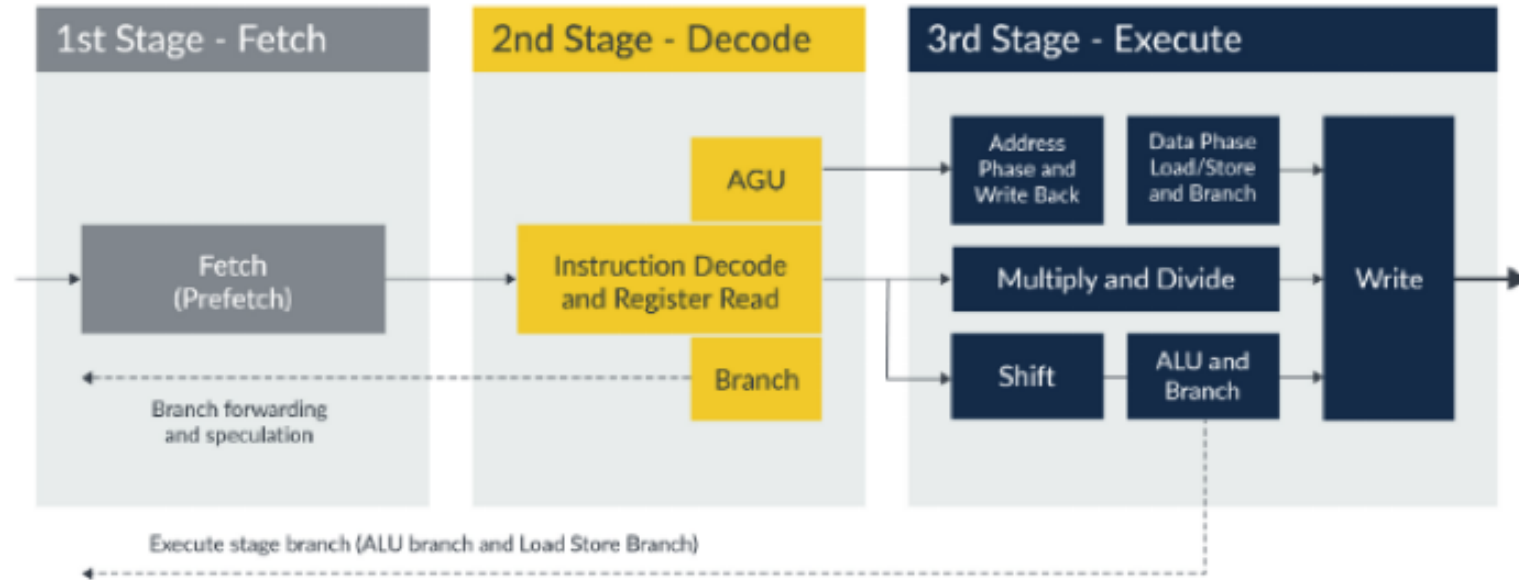


Harvard Architektur

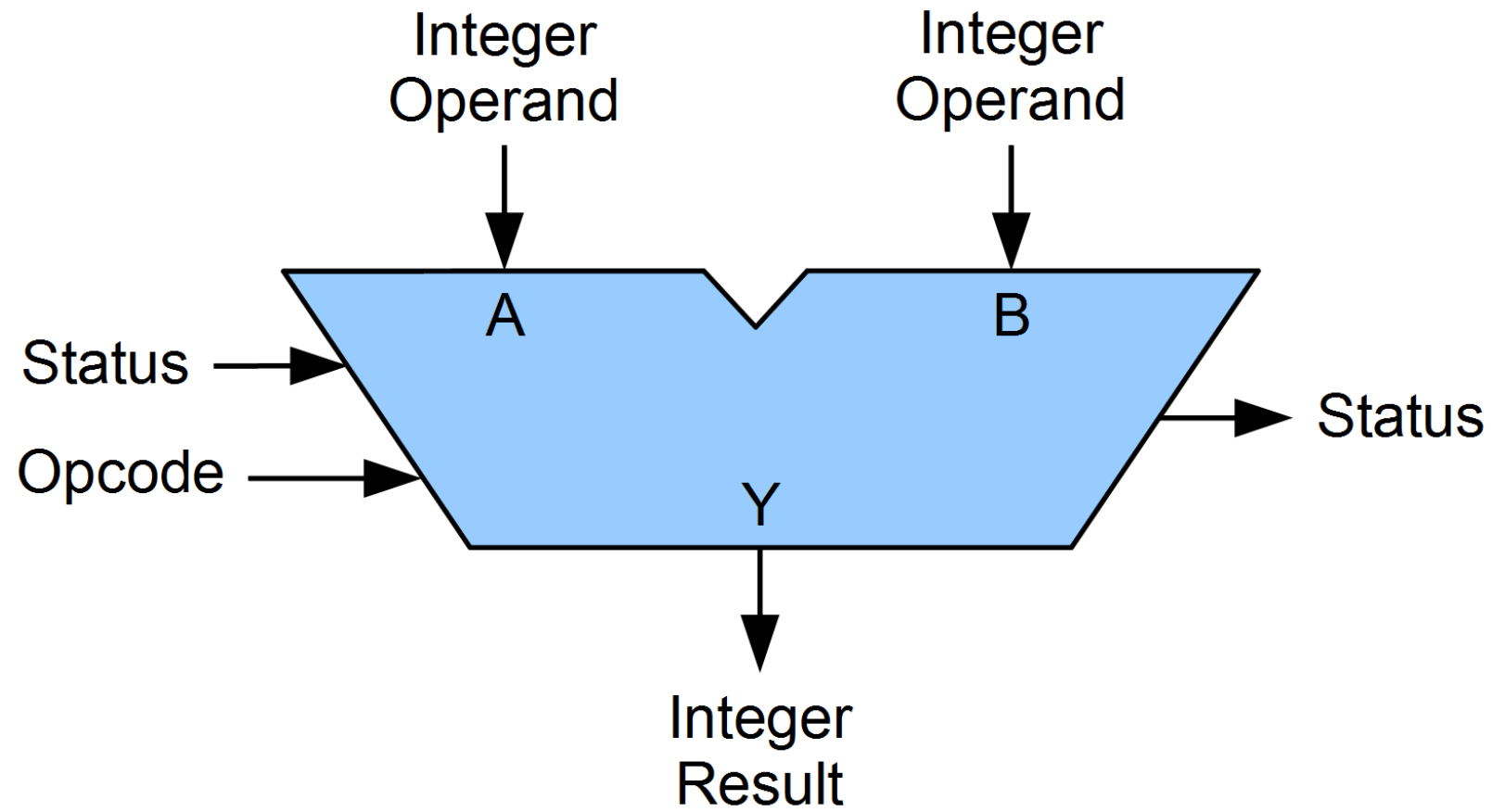


Fetch - Decode - Execute

Cortex-M4 Pipeline



Arithmetic Logic Unit (ALU)



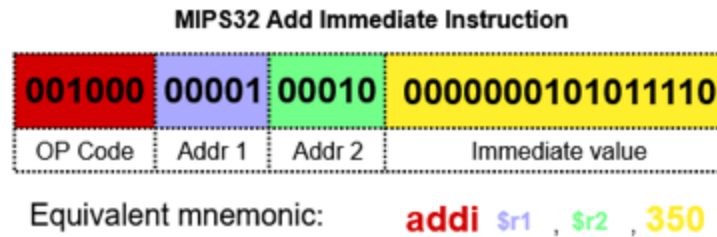
Mindestens:

- Addition (ADD)
- Negation (NOT)
- Konjunktion (AND)

Zusätzlich (Auswahl):

- Subtraktion
- Vergleich
- Multiplikationen / Division
- Oder
- Shift / Rotation

Instruction Set



<http://lyons42.com/AVR/Opcodes/AVRAAllOpcodes.html>

A64 Instruction Set

C4.1 A64 instruction set encoding

The A64 instruction encoding is:



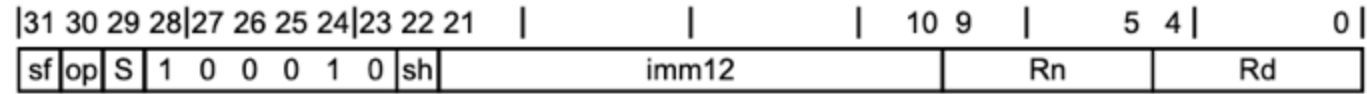
Table C4-1 Main encoding table for the A64 instruction set

Decode fields	Decode group or instruction page
op0	
0000	<i>Reserved on page C4-284.</i>
0001	Unallocated.
0010	SVE instructions. See <i>The Scalable Vector Extension (SVE)</i> on page A2-110.
0011	Unallocated.
100x	<i>Data Processing -- Immediate on page C4-284.</i>
101x	<i>Branches, Exception Generating and System instructions on page C4-289.</i>
x1x0	<i>Loads and Stores on page C4-298.</i>
x101	<i>Data Processing -- Register on page C4-332.</i>
x111	<i>Data Processing -- Scalar Floating-Point and Advanced SIMD on page C4-342.</i>



Table C4-3 Encoding table for the Data Processing -- Immediate group

Decode fields	Decode group or instruction page
op0	
00x	<i>PC-rel. addressing on page C4-285</i>
010	<i>Add/subtract (immediate) on page C4-285</i>
011	<i>Add/subtract (immediate, with tags) on page C4-286</i>
100	<i>Logical (immediate) on page C4-286</i>
101	<i>Move wide (immediate) on page C4-287</i>
110	<i>Bitfield on page C4-288</i>
111	<i>Extract on page C4-288</i>



Decode fields

Instruction page

sf	op	S	
0	0	0	ADD (immediate) - 32-bit variant
0	0	1	ADDS (immediate) - 32-bit variant
0	1	0	SUB (immediate) - 32-bit variant
0	1	1	SUBS (immediate) - 32-bit variant
1	0	0	ADD (immediate) - 64-bit variant
1	0	1	ADDS (immediate) - 64-bit variant
1	1	0	SUB (immediate) - 64-bit variant
1	1	1	SUBS (immediate) - 64-bit variant

Instruction Set

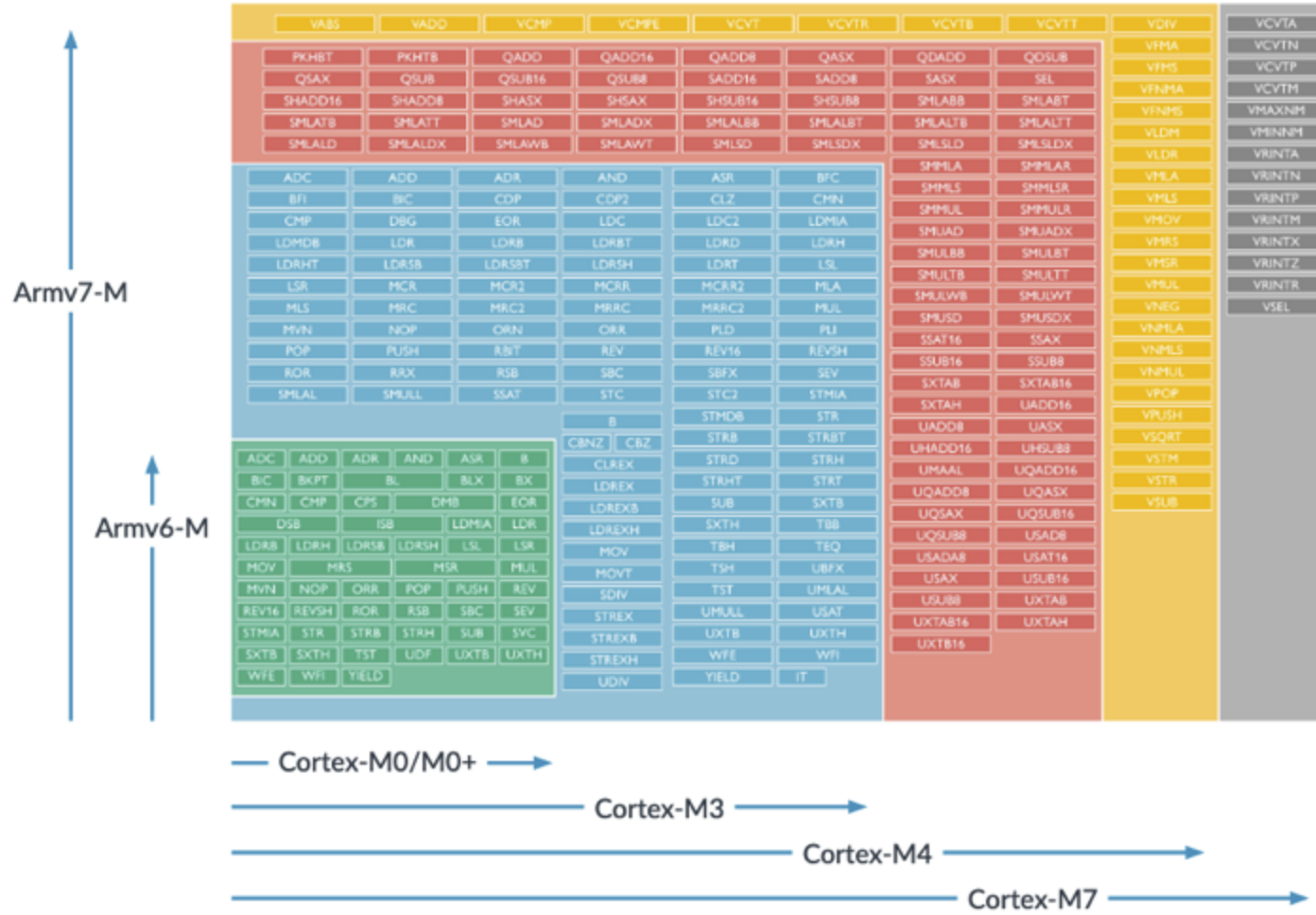


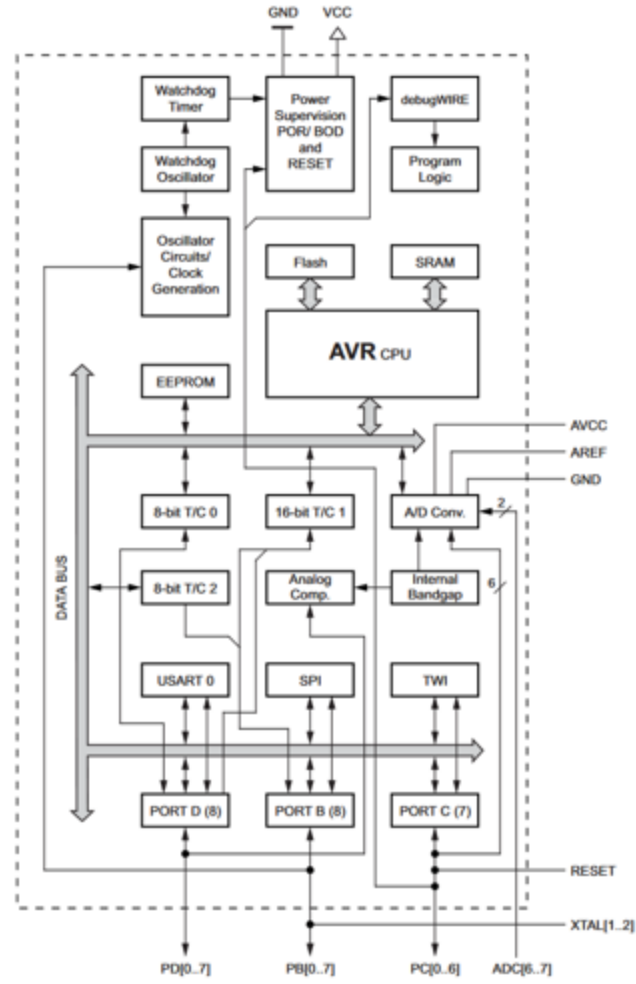
Figure 5: Instruction set

Reduced Instruction Set Computer (RISC)

- Opcode hat eine feste Länge
- Meistens 1 Takt pro Operation
- Load/Store Architektur: Separate Lade und Speicher-Befehle
- Hohe Anzahl an Registern für Zwischenresultate
- Oft Harvard-Architektur
- Grundsätzlich: Einfachere Architektur, einfacher für Compiler
- Alles andere: **CISC**

SoC vs Microprocessor vs Microcontroller

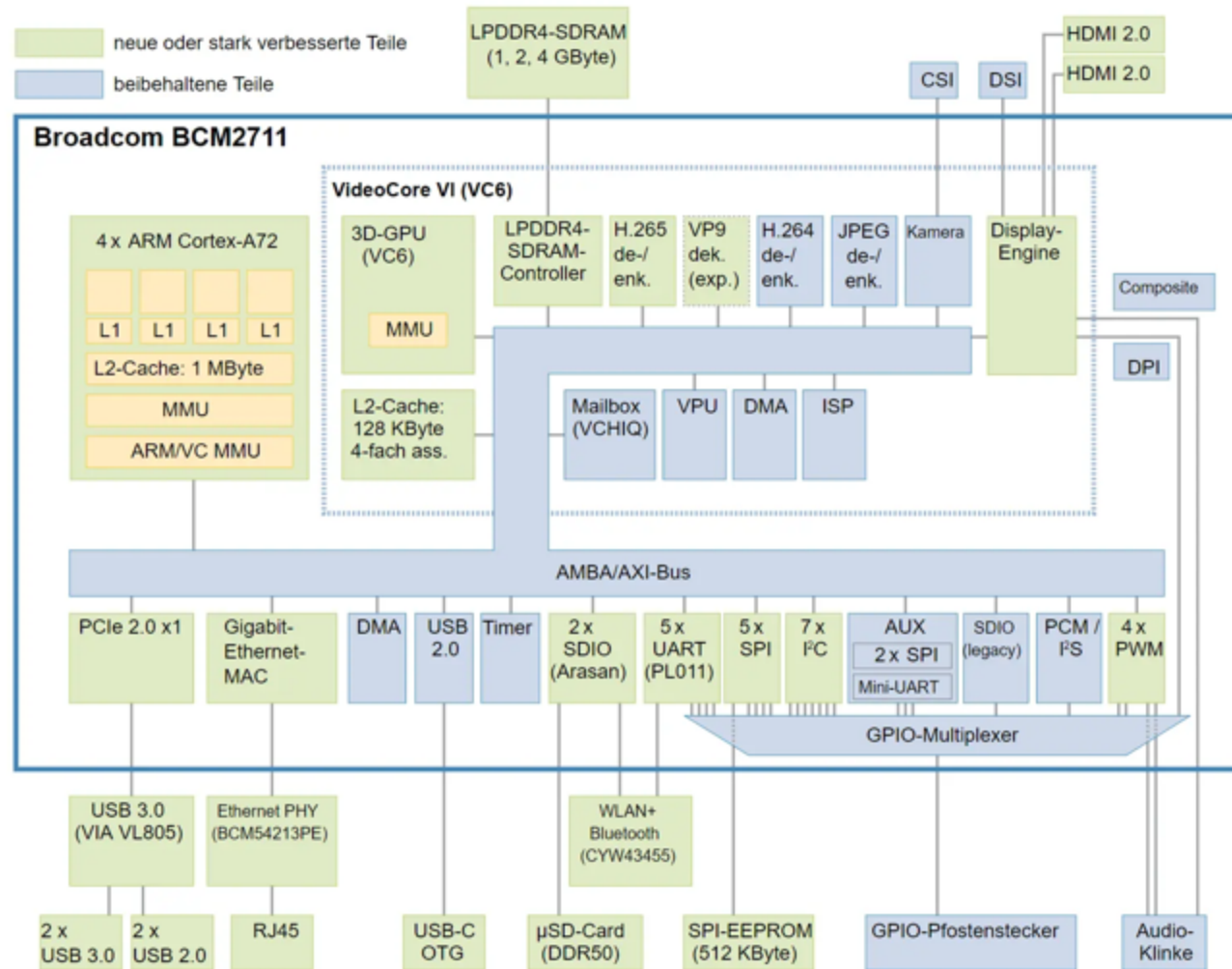
Microcontroller: ATmega328P

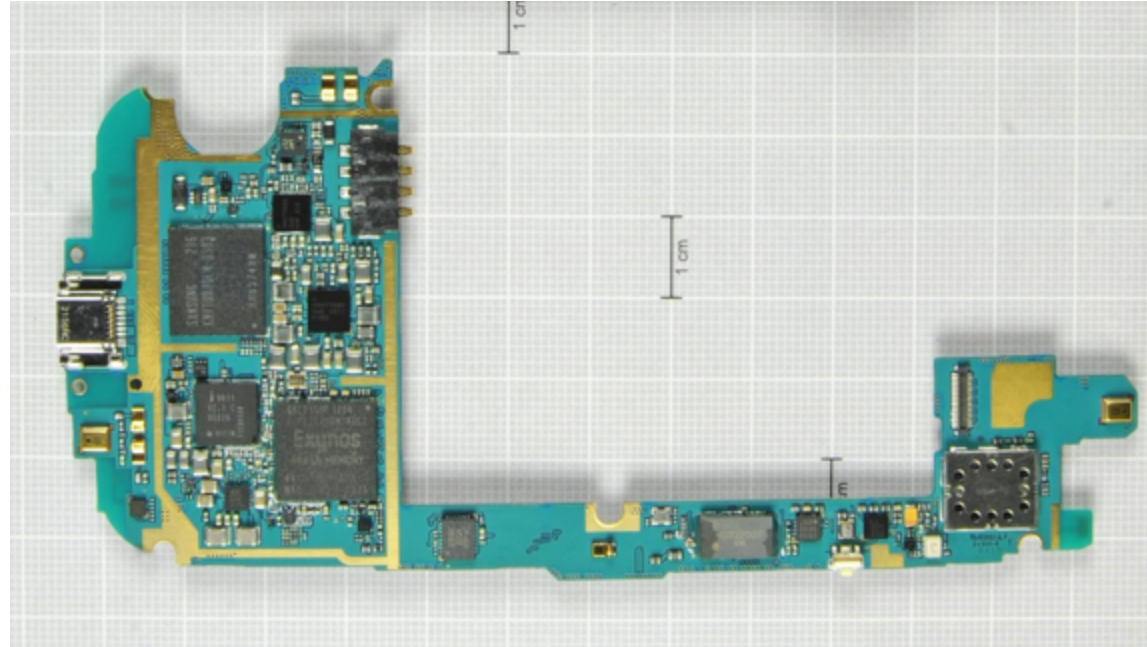


System on Chip (SoC)

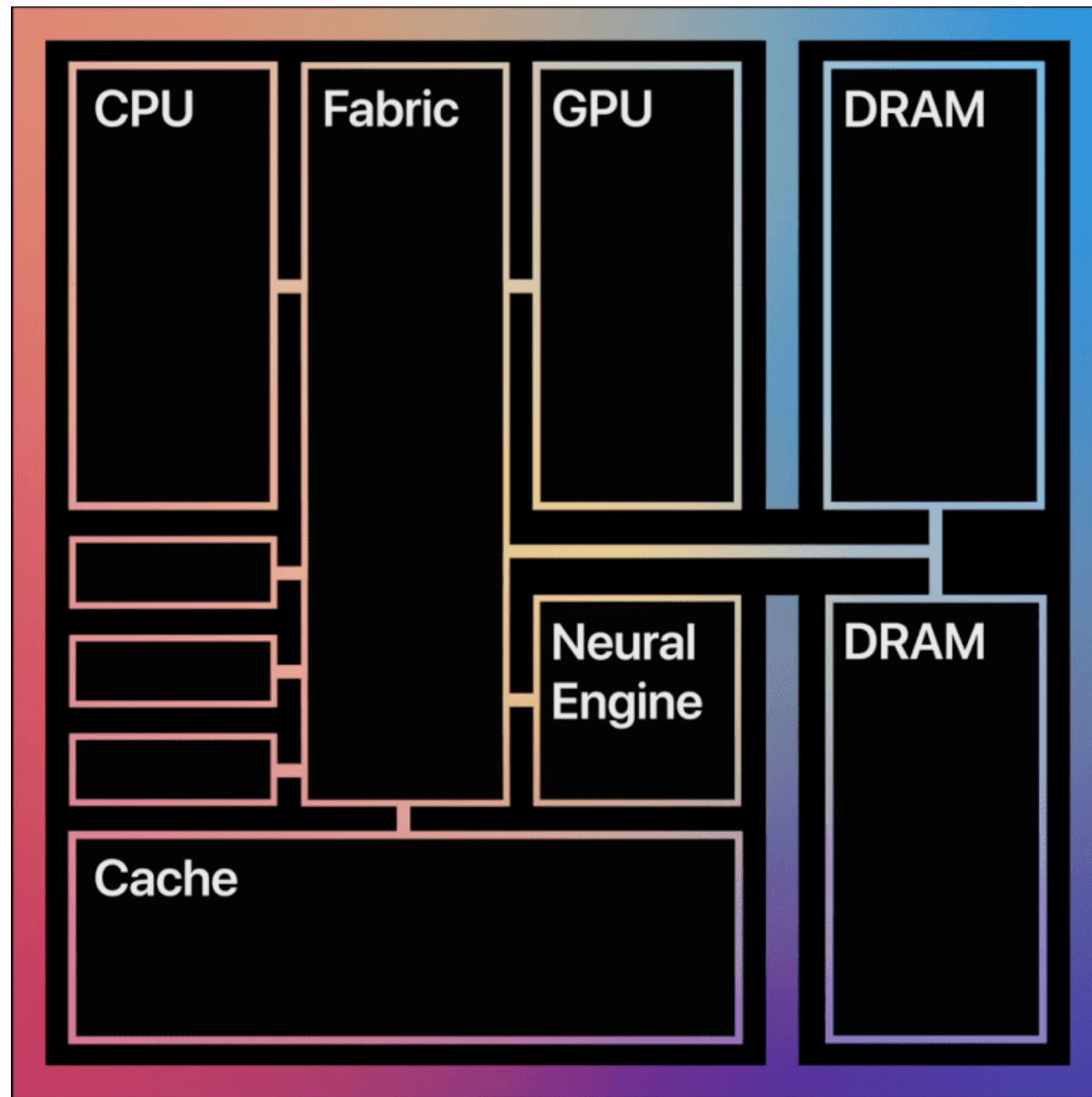
Herz des Raspberry Pi 4: Broadcom BCM2711

Das System-on-Chip (SoC) BCM2711 vereint nicht nur vier CPU-Kerne mit einer GPU, sondern enthält auch Controller für viele Schnittstellen.



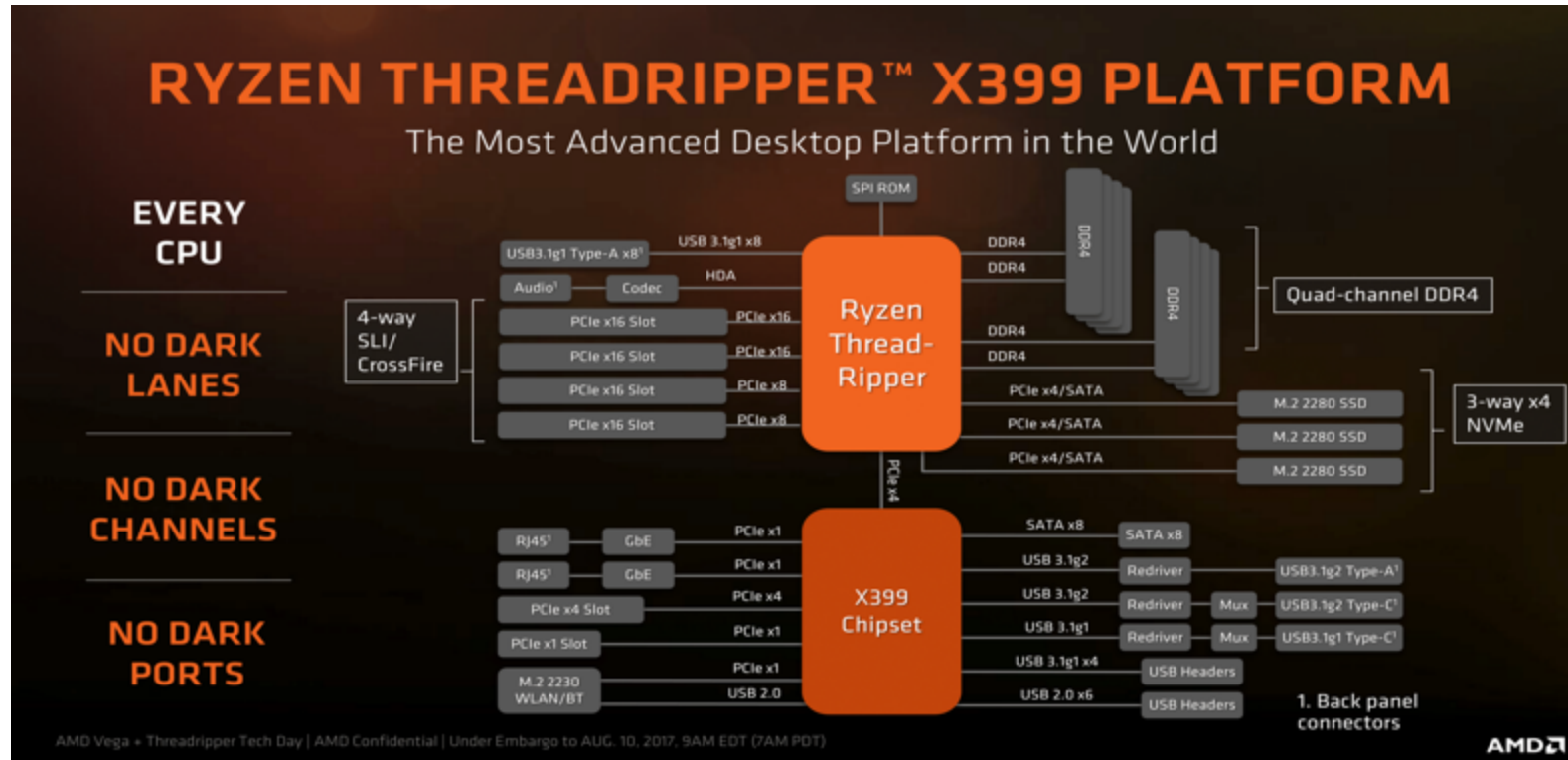


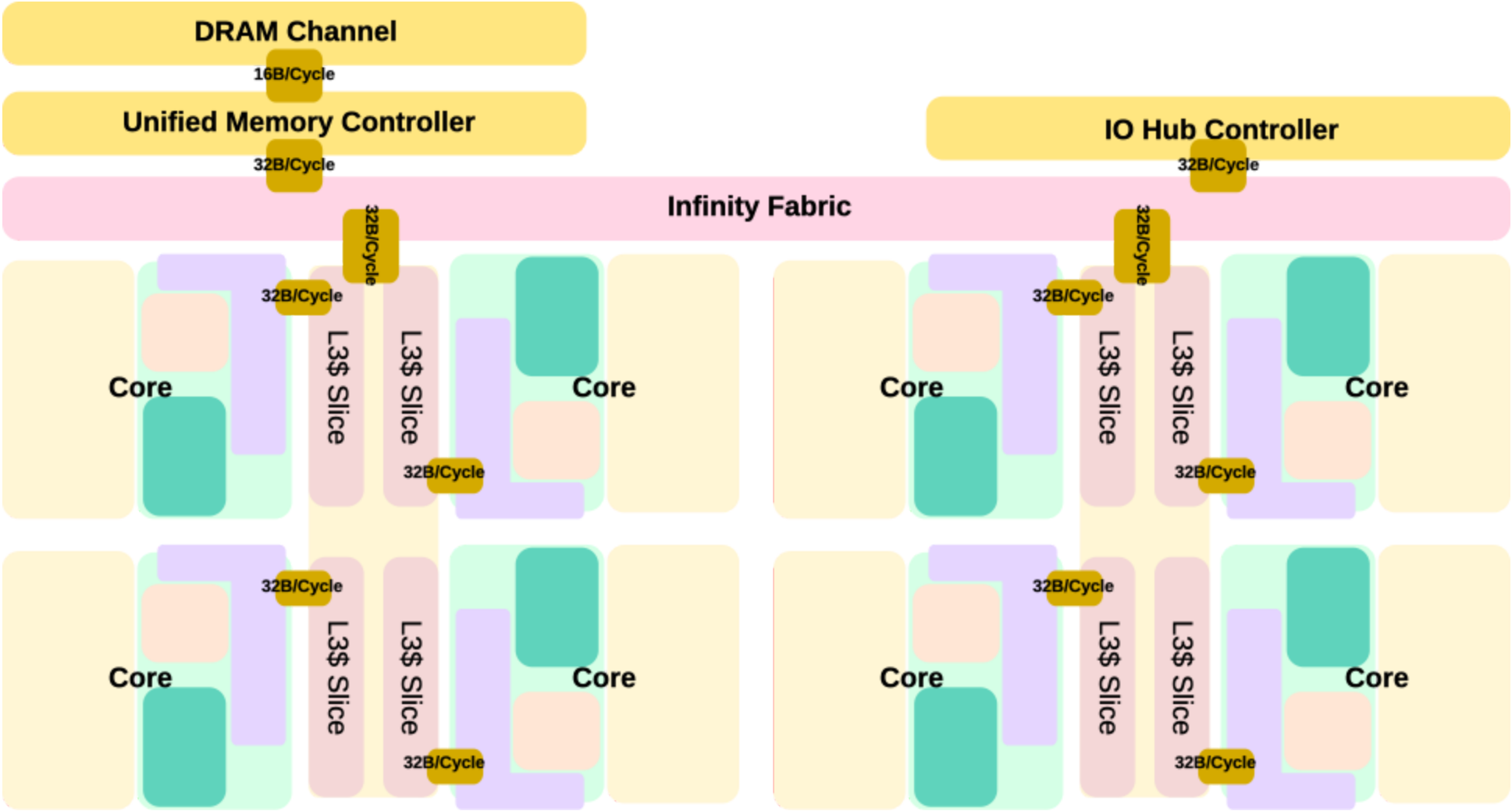
Samsung Galaxy S3



Apple M1

Microprocessor: AMD Ryzen Threadripper





Advanced RISC Machine (ARM)

"Arm licenses processor designs to semiconductor companies that incorporate the technology into their computer chips.

Licensees pay an up-front fee to gain access to our technology, and a royalty on every chip that uses one of our technology designs.

Typically, the royalty is based on the selling price of the chip."

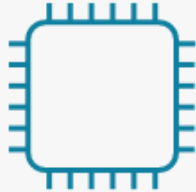
(https://group.softbank/en/ir/financials/annual_reports/2021/message/segars,
08.01.2024)

Company Highlights



70%

of the world's population
uses Arm-based
products



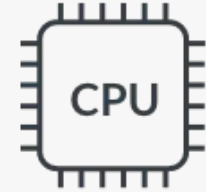
270Bn+

Arm-based chips shipped
to date



99%

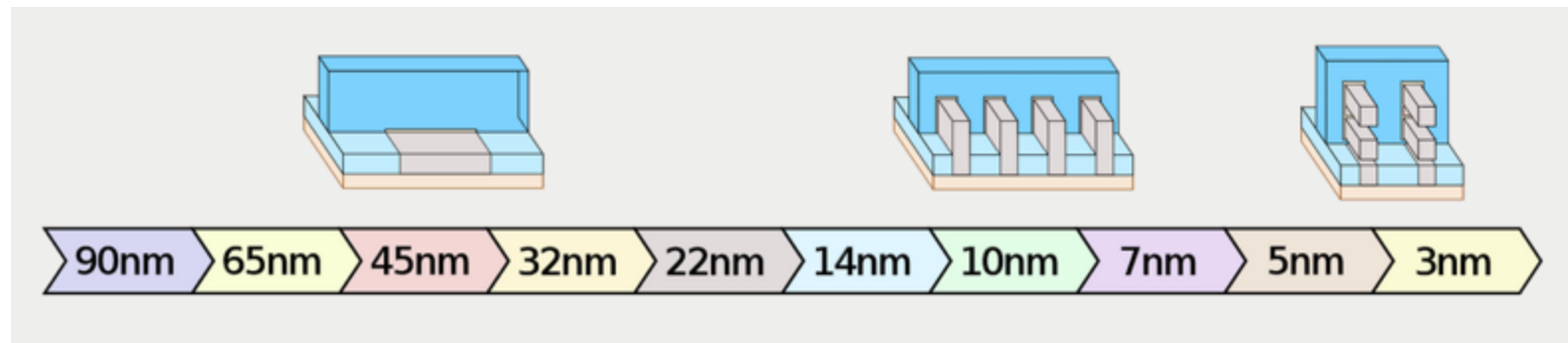
of smartphones run on
Arm-based processors



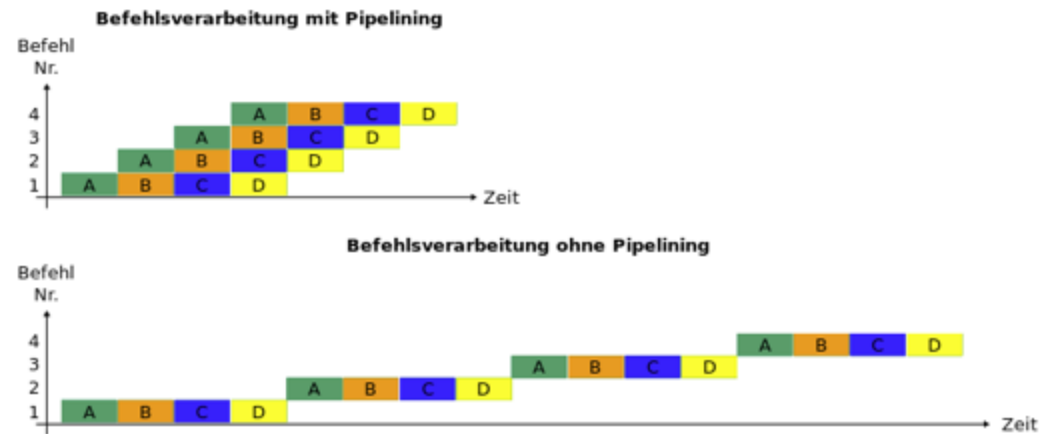
50%

of all chips with
processors are Arm-
based

Strukturgrösse



Pipelining



A – Befehlscode laden (IF, Instruction Fetch)

In der Befehlsbereitstellungsphase wird der Befehl, der durch den Befehlszähler adressiert ist, aus dem Arbeitsspeicher geladen. Der Befehlszähler wird anschließend hochgezählt.

B – Instruktion dekodieren und Laden der Daten (ID, Instruction Decoding)

In der Dekodier- und Ladephase wird der geladene Befehl dekodiert (1. Takthälfte) und die notwendigen Daten aus dem Arbeitsspeicher und dem Registersatz geladen (2. Takthälfte).

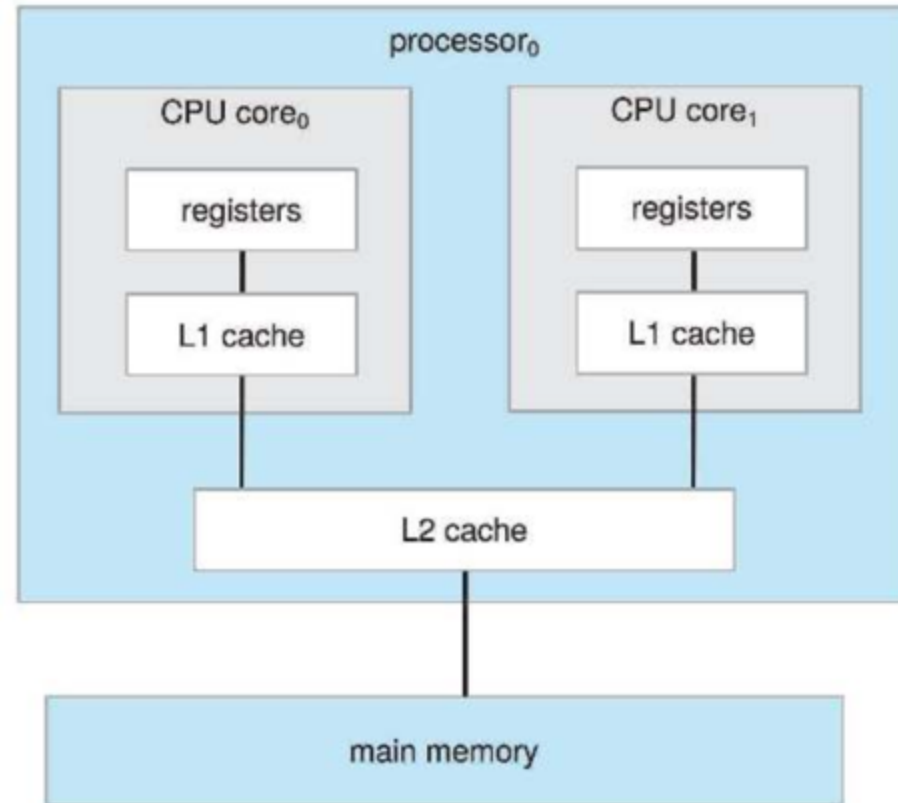
C – Befehl ausführen (EX, Execution)

In der Ausführungsphase wird der dekodierte Befehl ausgeführt. Das Ergebnis wird durch den [Pipeline-latch](#) gepuffert.

D – Ergebnisse zurückgeben (WB, Write Back)

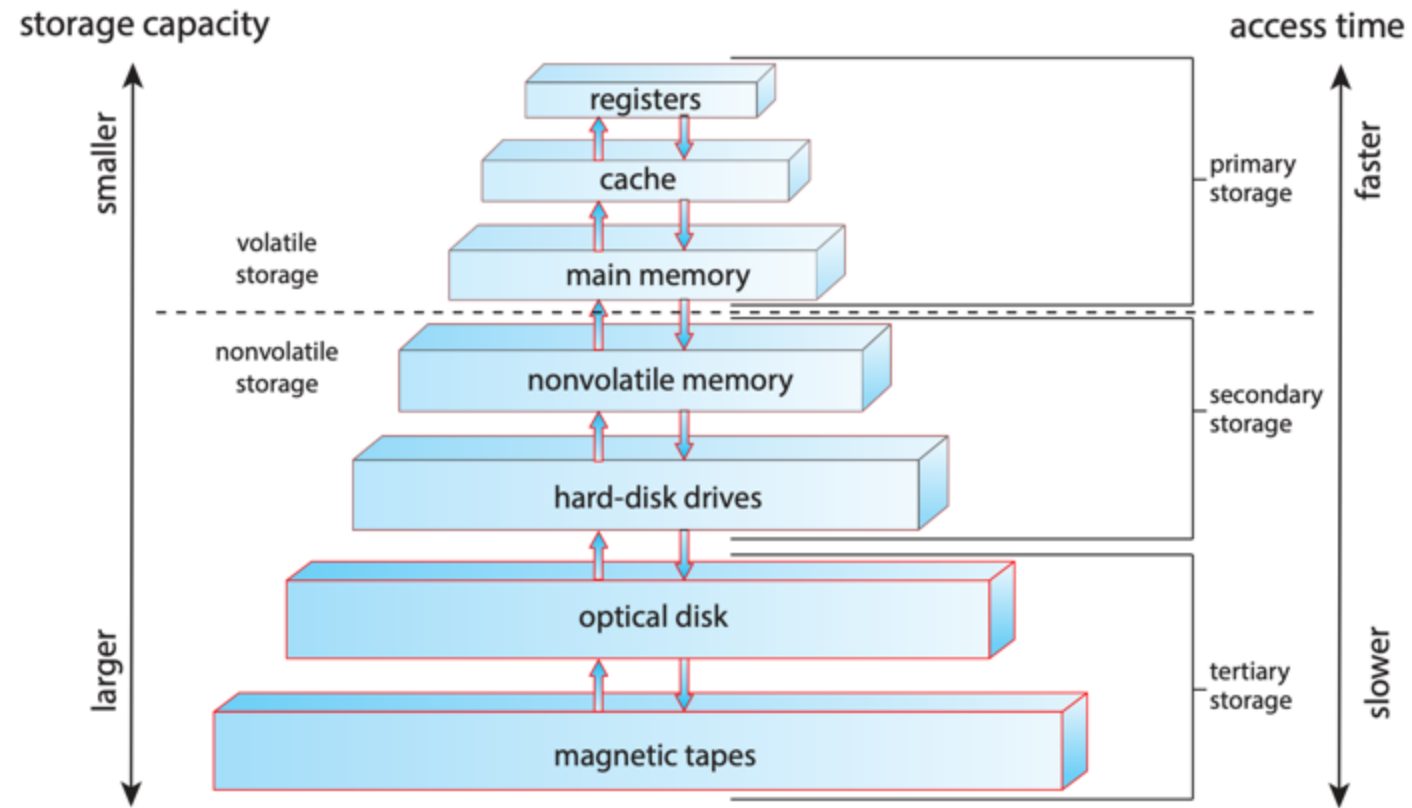
In der Resultatspeicherphase wird das Ergebnis in den Arbeitsspeicher oder in den Registersatz zurückgeschrieben.

Cache



(Silberschatz, 2019)

Speicher



(Silberschatz, 2019)

Level	1	2	3	4	5
Name	registers	cache	main memory	solid-state disk	magnetic disk
Typical size	< 1 KB	< 16MB	< 64GB	< 1 TB	< 10 TB
Implementation technology	custom memory with multiple ports CMOS	on-chip or off-chip CMOS SRAM	CMOS SRAM	flash memory	magnetic disk
Access time (ns)	0.25-0.5	0.5-25	80-250	25,000-50,000	5,000,000
Bandwidth (MB/sec)	20,000-100,000	5,000-10,000	1,000-5,000	500	20-150
Managed by	compiler	hardware	operating system	operating system	operating system
Backed by	cache	main memory	disk	disk	disk or tape

Figure 1.14 Characteristics of various types of storage.

(Silberschatz, 2019)

Quellen

Silberschatz, 2019

: A.Silberschatz, P.B.Galvin, G. Gagne (2019): Operating System Concepts, Global Edition,
Wiley