UNSW Course Outline

COMP4601 Design Project B - 2024

Published on the 29 May 2024

General Course Information

Course Code : COMP4601
Year : 2024
Term : Term 2
Teaching Period : T2
Is a multi-term course? : No
Faculty : Faculty of Engineering
Academic Unit : School of Computer Science and Engineering
Delivery Mode : In Person
Delivery Format : Standard
Delivery Location : Kensington
Campus : Sydney
Study Level : Undergraduate
Units of Credit : 6

Useful Links

Handbook Class Timetable

Course Details & Outcomes

Course Description

COMP4601 is a team-based project development course involving the analysis, design and implementation of embedded, high performance or low power FPGA-based accelerators using high-level synthesis.

Students study concepts through lectures and guided lab exercises during the first half of the

course, when project teams are also formed and the project goals are developed. During the second half of the course, students are involved in presenting group seminars and working on their projects. The course finishes with final project presentations.

Course Aims

Apart from teaching the elements of how to design hardware using high-level synthesis and gaining an understanding of accelerator design, this course enhances research skills, sharpens design, implementation and presentation skills, allow students to explore solutions to open-ended problems, and provides opportunities to practice the rapid acquisition of new technical skills with state-of-the-art technology.

Course Learning Outcomes

Course Learning Outcomes
CLO1 : Rapidly design and implement digital systems that incorporate programable logic as accelerators
CLO2 : Explain and put into practice techniques for accelerating computation in hardware
CLO3 : Independently, and collectively study advanced techniques in digital design and implementation
CLO4 : Document and present the work of their team in a professional manner

Course Learning Outcomes	Assessment Item
CLO1 : Rapidly design and implement digital systems that incorporate programable logic as accelerators	• Lab Component • Individual Project Score • Group Project Score
CLO2 : Explain and put into practice techniques for accelerating computation in hardware	• Lab Component • Individual Project Score • Group Project Score
CLO3 : Independently, and collectively study advanced techniques in digital design and implementation	• Seminar Component • Individual Project Score • Group Project Score
CLO4 : Document and present the work of their team in a professional manner	• Seminar Component • Individual Project Score • Group Project Score

Learning and Teaching Technologies

Moodle - Learning Management System | WebCMS3

Learning and Teaching in this course

Hardware design and systems prototyping using field-programmable gate arrays is increasingly important and supports a booming embedded systems and hardware accelerator industry. In order to develop essential skills and to be industrially relevant, computer engineering students need to gain experience designing and prototyping systems and components using programmable logic devices. Increasingly, these devices include hard processors, and therefore require designers to consider the appropriate mix of hardware and software approaches. In recent years much attention has also been given to using high-level synthesis tools that can enhance the productivity of designers prototyping hardware solutions to computational problems. We therefore endeavour to introduce our students to this important approach to hardware design. The background necessary to understand the design problem, processors and programmable logic technology will be outlined in classes. Students will work in teams to study and develop solutions using current methodologies to a computationally demanding and relevant problem.

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates
Lab Component Assessment Format: Individual	40%	Due Date: Weeks 3, 4, 5 & 6
Seminar Component Assessment Format: Individual	20%	Due Date: Weeks 7-10
Individual Project Score Assessment Format: Individual	10%	Due Date: Weeks 7-10
Group Project Score Assessment Format: Group	30%	Due Date: Week 5 & Week 10

Assessment Details

Lab Component

Assessment Overview

Four lab reports that are individually marked with written feedback being provided. Expected effort is 30 - 40 hours.

Course Learning Outcomes

- CLO1 : Rapidly design and implement digital systems that incorporate programable logic as accelerators

- CLO2 : Explain and put into practice techniques for accelerating computation in hardware

Seminar Component

Assessment Overview

Students present a seminar on a selected topic in groups of three. Seminar groups are provided with academic papers to form the basis of a coherent and interesting seminar. Seminar groups and their members are assessed by their peers with scores moderated by the convenor. Seminar groups are assessed on the coherence of their presentations and the interest engendered in their presentations. Individual seminar group members are assessed on their preparation, delivery and topic knowledge. Students spend 20 hours preparing their seminars.

Students are provided with an individual score for the quality of their contributions to seminar discussions and the quality of the assessments they have made of other seminar groups and seminar group members.

Course Learning Outcomes

- CLO3 : Independently, and collectively study advanced techniques in digital design and implementation
- CLO4 : Document and present the work of their team in a professional manner

Individual Project Score

Assessment Overview

Individual contribution to the quality of project outcomes is assessed based on discussions between individual team members and course staff over the period of the project work. The score is informed by the successes achieved relative to the challenges presented.

Course Learning Outcomes

- CLO1 : Rapidly design and implement digital systems that incorporate programable logic as accelerators
- CLO2 : Explain and put into practice techniques for accelerating computation in hardware
- CLO3 : Independently, and collectively study advanced techniques in digital design and implementation
- CLO4 : Document and present the work of their team in a professional manner

Group Project Score

Assessment Overview

Students team up into groups of three or four students to undertake a design project of their choice involving the acceleration in hardware of an algorithm studied in software. Students

spend 40 - 80 hours on their projects depending upon motivation and complexity.

Assessment is based on project planning (presentation and report) and final project reporting (presentation, report and demonstration). Oral feedback is provided at the planning stage. Students are able to consult course staff during the development phase. Some oral feedback is provided at the final reporting stage.

Course Learning Outcomes

- CLO1 : Rapidly design and implement digital systems that incorporate programable logic as accelerators
- CLO2 : Explain and put into practice techniques for accelerating computation in hardware
- CLO3 : Independently, and collectively study advanced techniques in digital design and implementation
- CLO4 : Document and present the work of their team in a professional manner

General Assessment Information

Grading Basis

Standard

Course Schedule

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

General Schedule Information

Course Schedule

This section explains the weekly schedule of activities, organisational deadlines and due dates for the course.

Weekly Schedule

Week	Weekday	Time	Activity
1 - 5	Mondays	11:00 - 13:00	In person lecture - Lawrence East M032
	Mondays	15:00 - 16:00	Lab/project support session - Brass ME305
	Tuesdays	9:00 - 10:00	Lab/project support session - Brass ME305

	Wednesdays	11:00 - 13:00	In person lecture - Lawrence Theatre G001
6	Wednesday	14:00 - 16:00	Online lab/project help (tentative)
7 - 10	Mondays	11:00 - 13:00	Seminars - Lawrence East M032
	Mondays	15:00 - 16:00	Project support session - Brass ME305
	Tuesdays	9:00 - 10:00	Project support session - Brass ME305
	Wednesdays	11:00 - 13:00	Seminars - Lawrence Theatre G001

Course Resources

Prescribed Resources

The formal pre-requisites for this course are COMP3211 and COMP3601.

It is assumed that, prior to taking this course, students:

- know a hardware description language, such as VHDL or Verilog,
- have experience designing, implementing and testing FPGA solutions,
- have the background to architect solutions to computational problems,
- know C/C++, and
- understand the structure of computer and operating systems.

Recommended Resources

During the first 5 weeks of lectures, we will be discussing the content of the electronic book Parallel Programming for FPGAs by Ryan Kastner, Janarbek Matai and Stephen Neuendorfer . Lab exercises will be also be based on exercises suggested in this text. We will use the 2020.1 version of Vivado HLS and 2021.2 Vitis tools from Xilinx and target the KV260 Kria boards. Students will be guided in their uptake of the tools via Xilinx tutorials and guides prepared by the teaching staff.

Students will need to refer to a wide range of technical information, such as research papers, product data sheets, application notes, standards, system documentation and reference books to gain the background needed to design and implement the project systems. Some of these references will be identified during the course. Please ask the lecturer and/or demonstrators for assistance if you are lost.

Course Evaluation and Development

Student feedback on this course will be obtained via electronic survey (myExperience) at the end of session and will be used to make improvements to the course. **Students are encouraged to provide informal feedback during the session and to let the lecturer in charge know of any problems as soon as they arise** . Every reasonable effort to address concerns will be made.

myExperience responses for 2023 were overwhelmingly positive. Suggested improvements centred on a heavy workload - 3 presentations too many - reducing number of deliverables - and a desire for even more guidance on what was expected than what was added during 2023. This year I have decided to reduce the number of presentations to two per student and to ease the deliverable burden by eliminating project plan presentations - a brief report on your plans should still needs to be prepared for comment/feedback. I will re-examine the labs to streamline them. I will also try to be more expansive about what I'm looking for in the lab and project reports. One student commented: " *I think the course should emphasize more the importance of understanding the tutorials before each lab. Also, I think reading the [relevant] chapter in the textbook before lectures is more helpful for understanding the concepts than reading it afterwards.* " - I couldn't agree more.

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Convenor	Oliver Diessel					Yes	Yes
Lecturer	Hammond Pea rce					No	No

Other Useful Information

Academic Information

I. Special consideration and supplementary assessment

If you have experienced an illness or misadventure beyond your control that will interfere with your assessment performance, you are eligible to apply for Special Consideration prior to, or within 3 working days of, submitting an assessment or sitting an exam.

Please note that UNSW has a Fit to Sit rule, which means that if you sit an exam, you are declaring yourself fit enough to do so and cannot later apply for Special Consideration.

For details of applying for Special Consideration and conditions for the award of supplementary assessment, please see the information on UNSW's Special Consideration page.

II. Administrative matters and links

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Attendance
- UNSW Email Address
- Special Consideration
- Exams
- Approved Calculators
- Academic Honesty and Plagiarism
- Equitable Learning Services

III. Equity and diversity

Those students who have a disability that requires some adjustment in their teaching or learning environment are encouraged to discuss their study needs with the course convener prior to, or at the commencement of, their course, or with the Equity Officer (Disability) in the Equitable Learning Services. Issues to be discussed may include access to materials, signers or note-takers, the provision of services and additional exam and assessment arrangements. Early notification is essential to enable any necessary adjustments to be made.

IV. Professional Outcomes and Program Design

Students are able to review the relevant professional outcomes and program designs for their streams by going to the following link: https://www.unsw.edu.au/engineering/student-life/student-resources/program-design.

Note: This course outline sets out the description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle or your primary learning management system (LMS) should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline/Moodle/LMS, the description in the Course Outline/Moodle/LMS applies.

Academic Honesty and Plagarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. *Plagiarism at UNSW is defined as using the words or ideas of others and passing them off as your own.*

Plagiarism is a type of intellectual theft. It can take many forms, from deliberate cheating to accidentally copying from a source without acknowledgement. UNSW has produced a website with a wealth of resources to support students to understand and avoid plagiarism, visit: student.unsw.edu.au/plagiarism. The Learning Centre assists students with understanding academic integrity and how not to plagiarise. They also hold workshops and can help students one-on-one.

You are also reminded that careful time management is an important part of study and one of the identified causes of plagiarism is poor time management. Students should allow sufficient time for research, drafting and the proper referencing of sources in preparing all assessment tasks.

Repeated plagiarism (even in first year), plagiarism after first year, or serious instances, may also be investigated under the Student Misconduct Procedures. The penalties under the procedures can include a reduction in marks, failing a course or for the most serious matters (like plagiarism in an honours thesis or contract cheating) even suspension from the university. The Student Misconduct Procedures are available here:

www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf

Submission of Assessment Tasks

Work submitted late without an approved extension by the course coordinator or delegated authority is subject to a late penalty of five percent (5%) of the maximum mark possible for that assessment item, per calendar day.

The late penalty is applied per calendar day (including weekends and public holidays) that the assessment is overdue. There is no pro-rata of the late penalty for submissions made part way through a day. This is for all assessments where a penalty applies.

Work submitted after five days (120 hours) will not be accepted and a mark of zero will be

awarded for that assessment item.

For some assessment items, a late penalty may not be appropriate. These will be clearly indicated in the course outline, and such assessments will receive a mark of zero if not completed by the specified date. Examples include:

- Weekly online tests or laboratory work worth a small proportion of the subject mark;
- Exams, peer feedback and team evaluation surveys;
- Online quizzes where answers are released to students on completion;
- Professional assessment tasks, where the intention is to create an authentic assessment that has an absolute submission date; and,
- Pass/Fail assessment tasks.

Faculty-specific Information

Engineering Student Support Services – The Nucleus - enrolment, progression checks, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries e.g. admissions, fees, programs, credit transfer

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

School Contact Information

CSE Help! - on the Ground Floor of K17

- For assistance with coursework assessments.

The Nucleus Student Hub - https://nucleus.unsw.edu.au/en/contact-us

- Course enrolment queries.

Grievance Officer - grievance-officer@cse.unsw.edu.au

- If the course convenor gives an inadequate response to a query or when the courses convenor does not respond to a query about assessment.

Student Reps - stureps@cse.unsw.edu.au

- If some aspect of a course needs urgent improvement. (e.g. Nobody responding to forum queries, cannot understand the lecturer)

You should **never** contact any of the following people directly:

- Vice Chancellor

- Pro-vice Chancellor Education (PVCE)

- Head of School

- CSE administrative staff

- CSE teaching support staff

They will simply bounce the email to one of the above, thereby creating an unnecessary level of indirection and a delay in the response.