



UNSW Course Outline

ZEIT2209 Electrical Engineering Design Project 1 - 2024

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General Course Information

Course Code : ZEIT2209

Year : 2024

Term : Semester 2

Teaching Period : Z2

Is a multi-term course? : No

Faculty : UNSW Canberra

Academic Unit : School of Engineering and Technology

Delivery Mode : In Person

Delivery Format : Standard

Delivery Location : UNSW Canberra at ADFA

Campus : UNSW Canberra

Study Level : Undergraduate

Units of Credit : 6

Useful Links

[Handbook Class Timetable](#)

Course Details & Outcomes

Course Description

This 6 unit of credit course is the capstone for the first two years of the program, where students will apply their learning from earlier electrical engineering courses to a design project. Working in small groups, students will develop their own prototype electronic circuits, and integrate them to

create a functional system which meets specified requirements. The project requires students to be self-directed in finding solutions to open-ended design problems, and to work effectively in a team environment. The course centres around lab-based project activities, which are supported by lessons on the practical aspects of creating an electrical system, techniques to ensure system quality, and effective communication of engineering information. Students are expected to communicate their results using appropriate language, mathematics, and figures of the electrical engineering profession.

Course Aims

This course provides a foundation in understanding the fundamental concepts in electrical engineering and leads to the solution of practical problems in electrical engineering. This course will enable students to design and implement effective electrical engineering project using a broad range of electrical engineering fundamentals and tools including analog/digital conversion, spectrum of a signal, sampling theorem, modulation, microcontroller programming, feedback control systems, DC motors and motor drive systems. This course will enable students to study practical electrical circuits and control systems involving modulator and amplifier, and understand how fundamental concepts in electrical engineering are linked with mathematical tools such as Fourier Transform, convolution and Laplace transform. This course aims to show engineering applications of Mathematics courses, and to bridge them with third year Electrical Engineering courses.

Relationship to Other Courses

Prerequisites: ZEIT2207 and ZEIT2208

Course Learning Outcomes

Course Learning Outcomes	Engineers Australia - Professional Engineer (Stage 1)
CLO1 : Create an authentic prototype of an electronic circuit.	<ul style="list-style-type: none"> • PEE1.5 : Knowledge of engineering design practice and contextual factors impacting the engineering discipline • PEE1.6 : Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline
CLO2 : Combine knowledge from multiple sub-disciplines of electrical engineering to the design of an electronic circuit.	<ul style="list-style-type: none"> • PEE1.6 : Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline • PEE2.1 : Application of established engineering methods to complex engineering problem solving • PEE2.2 : Fluent application of engineering techniques, tools and resources
CLO3 : Work effectively in a team environment to integrate electronic circuits into a solution that meets specified requirements.	<ul style="list-style-type: none"> • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE3.3 : Creative, innovative and pro-active demeanour • PEE3.6 : Effective team membership and team leadership
CLO4 : Communicate appropriate design information verbally and through documents, using the language of the discipline, mathematics and drawings.	<ul style="list-style-type: none"> • PEE3.2 : Effective oral and written communication in professional and lay domains • PEE3.4 : Professional use and management of information

Course Learning Outcomes	Assessment Item
CLO1 : Create an authentic prototype of an electronic circuit.	<ul style="list-style-type: none"> • Schematic and PCB Layout • Soldering • Hardware Testing
CLO2 : Combine knowledge from multiple sub-disciplines of electrical engineering to the design of an electronic circuit.	<ul style="list-style-type: none"> • Subsystem Design • Final Report • Hardware Testing
CLO3 : Work effectively in a team environment to integrate electronic circuits into a solution that meets specified requirements.	<ul style="list-style-type: none"> • System Demonstration • Final Report
CLO4 : Communicate appropriate design information verbally and through documents, using the language of the discipline, mathematics and drawings.	<ul style="list-style-type: none"> • Subsystem Design • Final Report

Learning and Teaching Technologies

Moodle - Learning Management System

Learning and Teaching in this course

The Learning Management System

Moodle is the Learning Management System used at UNSW Canberra. All courses have a Moodle site which will become available to students at least one week before the start of semester.

Please find all help and documentation (including Blackboard Collaborate) at the [Moodle Support page](#).

UNSW Moodle supports the following web browsers:

» Google Chrome 50+

» Safari 10+

** Internet Explorer is not recommended

** Addons and Toolbars can affect any browser's performance.

Operating systems recommended are:

Windows 7, 10, Mac OSX Sierra, iPad IOS10

For further details about system requirements click [here](#).

Log in to Moodle [here](#).

If you need further assistance with Moodle:

For enrolment and login issues please contact:

IT Service Centre

Email: itservicecentre@unsw.edu.au

Phone: (02) 9385-1333

International: +61 2 9385 1333

For all other Moodle issues please contact:

External TELT Support

Email: externalteltsupport@unsw.edu.au

Phone: (02) 9385-3331

International: +61 2 938 53331

Opening hours:

Monday – Friday 7:30am – 9:30 pm

Saturday & Sunday 8:30 am – 4:30pm

Additional Course Information

Academic Integrity and Plagiarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW staff and students have a responsibility to adhere to this principle of academic integrity. All students are expected to adhere to UNSW's Student Code of Conduct

<https://www.gs.unsw.edu.au/policy/documents/studentcodepolicy.pdf>

Plagiarism undermines academic integrity and is not tolerated at UNSW. *It is defined as using the words or ideas of others and passing them off as your own, and can take many forms, from deliberate cheating to accidental copying from a source without acknowledgement.*

For more information, please refer to the following:

<https://student.unsw.edu.au/plagiarism>

Referencing

In this course, students are required to reference following the APA 7 / Chicago NB referencing style. Information about referencing styles is available at: <https://guides.lib.unsw.adfa.edu.au/c.php?g=472948&p=3246720>

Study at UNSW Canberra

<https://www.unsw.adfa.edu.au/study>

Study at UNSW Canberra has lots of useful information regarding:

- Where to get help
- Administrative matters
- Getting your passwords set up
- How to log on to Moodle
- Accessing the Library and other areas.

Additional Information as required

CRICOS Provider no. 00098G

The University of New South Wales Canberra.

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates
Schematic and PCB Layout Assessment Format: Individual	0%	Due Date: Week 4: 05 August - 09 August
Subsystem Design Assessment Format: Individual	20%	Due Date: 23/08/2024 11:59 PM
Soldering Assessment Format: Individual	0%	Due Date: Week 7: 09 September - 13 September
Hardware Testing Assessment Format: Individual	0%	Due Date: Week 9: 23 September - 27 September
System Demonstration Assessment Format: Group	0%	Due Date: Week 13: 21 October - 25 October
Meet all Individual Competency Items Assessment Format: Individual	50%	
Final Report Assessment Format: Group	30%	Due Date: 04/11/2024 11:59 PM

Assessment Details

Schematic and PCB Layout

Assessment Overview

Competency assessment

Course Learning Outcomes

- CLO1 : Create an authentic prototype of an electronic circuit.

Hurdle rules

Completing this task is a requirement to achieve the 50% competency grade for the course.

Subsystem Design

Assessment Overview

n/a

Course Learning Outcomes

- CLO2 : Combine knowledge from multiple sub-disciplines of electrical engineering to the design of an electronic circuit.
- CLO4 : Communicate appropriate design information verbally and through documents, using the language of the discipline, mathematics and drawings.

Assignment submission Turnitin type

This assignment is submitted through Turnitin and students do not see Turnitin similarity reports.

Hurdle rules

This assessment item must be completed to a basic pass level to achieve the 50% competency grades. The 20% grades for this assessment item represent excellence - i.e. performance above a pass level.

Soldering

Assessment Overview

Competency Assessment

Course Learning Outcomes

- CLO1 : Create an authentic prototype of an electronic circuit.

Hurdle rules

This assessment item must be completed in order to achieve the 50% competency grades.

Hardware Testing

Assessment Overview

Competency Assessment

Course Learning Outcomes

- CLO1 : Create an authentic prototype of an electronic circuit.
- CLO2 : Combine knowledge from multiple sub-disciplines of electrical engineering to the design of an electronic circuit.

Hurdle rules

This assessment must be completed in order to achieve the 50% competency grade

System Demonstration

Assessment Overview

Competency Assessment

Course Learning Outcomes

- CLO3 : Work effectively in a team environment to integrate electronic circuits into a solution that meets specified requirements.

Hurdle rules

This assessment item must be completed successfully in order to achieve the 50% competency grade for the course.

Meet all Individual Competency Items

Assessment Overview

Awarded on successful competency checks throughout the course.

Final Report

Assessment Overview

n/a

Course Learning Outcomes

- CLO2 : Combine knowledge from multiple sub-disciplines of electrical engineering to the design of an electronic circuit.
- CLO3 : Work effectively in a team environment to integrate electronic circuits into a solution that meets specified requirements.
- CLO4 : Communicate appropriate design information verbally and through documents, using the language of the discipline, mathematics and drawings.

Detailed Assessment Description

This is a group submission where all members of the group receive the same grade.

Hurdle rules

This report must be completed to a pass level in order to achieve the 50% competency grade.

The 30% for this assessment item are the excellence grades, representing performance above a minimum pass level.

General Assessment Information

Late Submission of Assessment

Unless prior arrangement is made with the lecturer or a formal application for special consideration is submitted, a penalty of 5% of the total available mark for the assessment will apply for each day that an assessment item is late up to a maximum of 5 days (120 hours) after which an assessment can no longer be submitted and a grade of 0 will be applied.

Use of Generative AI in Assessments

Unless stated otherwise, for assessment items in this course the following policy applies:

PLANNING ASSISTANCE

As this assessment task involves some planning or creative processes, you are permitted to use software to generate initial ideas. However, you must develop or edit those ideas to such a significant extent that what is submitted is your own work, i.e. only occasional AI generated words or phrases may form part of your final submission. It is a good idea to keep copies of the initial prompts to show your lecturer if there is any uncertainty about the originality of your work. If the outputs of generative AI such as ChatGPT form a part of your submission, it will be regarded as serious academic misconduct and subject to the standard penalties, which may include 00FL, suspension and exclusion.

Grading Basis

Standard

Requirements to pass course

This course will be graded according to a competency/excellence model.

Competency must be demonstrated in all assessment items to pass the course. 50% of the course grade will be automatically awarded if all competencies are demonstrated. The assessment for items labelled as "Competency" in the above table will be graded as either "competent" or "not competent", and no numerical grades will be given.

To achieve the remaining 50% of the course grade, students must demonstrate excellence in their individual design submission, and group final report. The numerical grades for these items will reflect the level of achievement beyond basic competency - so a bare minimum pass will result in 0 additional grades for excellence. Note that students must demonstrate competency in these two assessment items to pass the course.

Where students fail to demonstrate competency on the first attempt, there will be opportunities for supplementary assessment.

Course Schedule

Teaching Week/Module	Activity Type	Content
Week 1 : 15 July - 19 July	Lecture	Introduction to Project
	Tutorial	Data Sheets and Application Notes Exercise
	Laboratory	Introductory Project Exercise
Week 2 : 22 July - 26 July	Lecture	Introduction to Schematic Layout
	Tutorial	Schematic Layout Exercise
	Laboratory	Prototype Subsystem on Breadboard
Week 3 : 29 July - 2 August	Lecture	Introduction to PCB Layout
	Tutorial	PCB Layout Exercise
	Laboratory	Prototype Subsystem on Breadboard
Week 4 : 5 August - 9 August	Lecture	Component Selection and Custom Parts
	Tutorial	Schematic and PCB Layout Competency Assessment
	Laboratory	Prototype Subsystem on Breadboard
Week 5 : 12 August - 16 August	Lecture	Design and Schematic Quality
	Tutorial	Custom Part Creation
	Laboratory	Schematic and PCB Layout of Subsystem
Week 6 : 19 August - 23 August	Lecture	PCB Quality and Design Submission
	Tutorial	Peer Review of Schematic and PCB
	Laboratory	Schematic and PCB Layout of Subsystem
Week 7 : 9 September - 13 September	Lecture	Soldering Demonstration
	Laboratory	Soldering Competency Assessment
Week 8 : 16 September - 20 September	Lecture	Requirements and Testing
	Laboratory	Subsystem Assembly and Testing
Week 9 : 23 September - 27 September	Lecture	Code Quality
	Tutorial	Requirements Exercise
	Laboratory	Hardware Testing Competency Assessment
Week 10 : 30 September - 4 October	Tutorial	Code Quality Exercise
	Laboratory	System Integration
Week 11 : 7 October - 11 October	Tutorial	Drop-in session for project assistance
Week 12 : 14 October - 18 October	Lecture	Report Writing
	Tutorial	Peer Review of Code
	Laboratory	System Integration
Week 13 : 21 October - 25 October	Laboratory	System Demonstration Competency Assessment

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

Course Resources

Prescribed Resources

Students will be required to bring to all lectures, labs and tutorials a laptop capable of running electronic CAD software for schematic and PCB design.

For the lab sessions, students are expected to have a multimeter and breadboard.

Course Evaluation and Development

One of the key priorities in the 2025 Strategy for UNSW is a drive for academic excellence in education. One of the ways of determining how well UNSW is progressing towards this goal is by listening to our own students. Students will be asked to complete the myExperience survey towards the end of this course.

Students can also provide feedback during the semester via: direct contact with the lecturer, the “On-going Student Feedback” link in Moodle, Student-Staff Liaison Committee meetings in schools, informal feedback conducted by staff, and focus groups. Student opinions really do make a difference. Refer to the Moodle site for this course to see how the feedback from previous students has contributed to the course development.

Important note: Students are reminded that any feedback provided should be constructive and professional and that they are bound by the Student Code of Conduct Policy

<https://www.gs.unsw.edu.au/policy/documents/studentcodepolicy.pdf>

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Convenor	David Powell		B32 SR102(A)		By Appointment	Yes	Yes
Lecturer	Toby Boyson				By appointment	No	No