UNSW Course Outline

ZEIT2208 Digital Electronics and Microcontrollers - 2024

Published on the 11 Feb 2024

General Course Information

Course Code : ZEIT2208
Year : 2024
Term : Semester 1
Teaching Period : Z1
Is a multi-term course? : No
Faculty : UNSW Canberra
Academic Unit : School of Engineering and Technology
Delivery Mode : In Person
Delivery Format : Standard
Delivery Location : UNSW Canberra at ADFA
Campus : UNSW Canberra
Study Level : Undergraduate
Units of Credit : 6

Useful Links

Handbook Class Timetable

Course Details & Outcomes

Course Description

This course provides a thorough examination of modern digital systems. Fundamental concepts of numbering systems, logic gates, boolean algebra and logic simplification pave the way towards eventual implementations with flip-flops, registers, as well as analog-to-digital and

digital-to-analog conversions. With the focus on practical use cases for microcontrollers, C programming language is leveraged to arrive at successful integrations of microcontrollers with additional peripherals. Finally, standardised communication buses are discussed to introduce how a microcontroller may function within the greater realm of all digital systems.

Course Aims

This course aims to provide a thorough examination of modern digital systems.

Relationship to Other Courses

Prerequisite courses: ZEIT1208, ZEIT1102

Digital Electronics and Microcontrollers relies on circuit knowledge developed in first year of EE program.

The class enables students to successfully implement electronic functionality via micronocontroller in future design courses, namely, ZEIT2209 and ZEIT4230

Course Learning Outcomes

Course Learning Outcomes	Engineers Australia - Professional Engineer (Stage 1)
CLO1 : Describe the fundamental building blocks of a digital system and combine their operations to help implement complex digital systems. Apply different techniques such as K-map to minimise logic expressions and implement them using logical gates.	• PEE1.2 : Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline • PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering discipline • PEE2.2 : Fluent application of engineering techniques, tools and resources • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE3.2 : Effective oral and written communication in professional and lay domains
CLO2 : Analyse, design and implement digital circuits within practical programming languages, such as C.	• PEE1.2 : Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline • PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering discipline • PEE2.2 : Fluent application of engineering techniques, tools and resources • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE3.2 : Effective oral and written communication in professional and lay domains
CLO3 : Generate and organize digital circuits to manipulate peripherals attached to a microcontroller.	• PEE1.2 : Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline • PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering discipline • PEE2.2 : Fluent application of engineering techniques, tools and resources • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE3.2 : Effective oral and written communication in professional and lay domains
CLO4 : Recognise the limitations of digital circuit implementations; and specify solutions that fits within the modern communications frameworks.	• PEE1.2 : Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline • PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering

	discipline • PEE2.2 : Fluent application of engineering techniques, tools and resources • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE3.2 : Effective oral and written communication in professional and lay domains

Course Learning Outcomes	Assessment Item
CLO1 : Describe the fundamental building blocks of a digital system and combine their operations to help implement complex digital systems. Apply different techniques such as K-map to minimise logic expressions and implement them using logical gates.	
CLO2 : Analyse, design and implement digital circuits within practical programming languages, such as C.	
CLO3 : Generate and organize digital circuits to manipulate peripherals attached to a microcontroller.	
CLO4 : Recognise the limitations of digital circuit implementations; and specify solutions that fits within the modern communications frameworks.	

Learning and Teaching Technologies

Moodle - Learning Management System

Learning and Teaching in this course

The Learning Management System

Moodle is the Learning Management System used at UNSW Canberra. All courses have a Moodle site which will become available to students at least one week before the start of semester. Please find all help and documentation (including Blackboard Collaborate) at the Moodle Support page.

UNSW Moodle supports the following web browsers:

» Google Chrome 50+

» Safari 10+

** Internet Explorer is not recommended

** Addons and Toolbars can affect any browser's performance.

Operating systems recommended are:

Windows 7, 10, Mac OSX Sierra, iPad IOS10

For further details about system requirements click here.

Log in to Moodle here.

If you need further assistance with Moodle:

For enrolment and login issues please contact:
IT Service Centre
Email: itservicecentre@unsw.edu.au
Phone: (02) 9385-1333
International: +61 2 9385 1333

For all other Moodle issues please contact:
External TELT Support
Email: externalteltsupport@unsw.edu.au
Phone: (02) 9385-3331
International: +61 2 938 53331

Opening hours:
Monday – Friday 7:30am – 9:30 pm
Saturday & Sunday 8:30 am – 4:30pm

Additional Course Information

Referencing

In this course, students are required to reference following the APA 7 / Chicago NB referencing style. Information about referencing styles is available at: https://guides.lib.unsw.adfa.edu.au/c.php?g=472948&p=3246720

Study at UNSW Canberra

https://www.unsw.adfa.edu.au/study

Study at UNSW Canberra has lots of useful information regarding:

- Where to get help
- Administrative matters
- Getting your passwords set up
- How to log on to Moodle
- Accessing the Library and other areas.

Additional Information as required

CRICOS Provider no. 00098G

The University of New South Wales Canberra.

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates	Engineers Australia - Professional Engineer (Stage 1)
Laboratory Report Assessment Format: Individual	36%	Start Date: Not Applicable Due Date: Not Applicable	• PEE1.2 : Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline • PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering discipline • PEE2.2 : Fluent application of engineering techniques, tools and resources • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE3.2 : Effective oral and written communication in professional and lay domains
Final Examination Assessment Format: Individual	40%	Start Date: Not Applicable Due Date: Not Applicable	• PEE1.2 : Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline • PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering discipline • PEE2.2 : Fluent application of engineering techniques, tools and resources • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE3.2 : Effective oral and written communication in professional and lay domains
Take Home Tests Assessment Format: Individual	24%	Start Date: Not Applicable Due Date: Not Applicable	• PEE1.2 : Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information

			sciences which underpin the engineering discipline • PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering discipline • PEE2.2 : Fluent application of engineering techniques, tools and resources • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE3.2 : Effective oral and written communication in professional and lay domains

Assessment Details

Laboratory Report

Assessment Overview

Three lab reports (worth 12% each)

Detailed Assessment Description

Three laboratory exercises will be conducted during the course. These are:

- Lab 1: Introduction to C
- Lab 2: Successive Approximation Converter
- Lab 3: UART + LCD Displays

Each of these laboratory exercises run over a number of weeks, and will be conducted during the weekly 2-hour lab period in the Electrical Engineering Teaching Laboratories (Rooms 114/116, Building 16). You are required to submit Lab Reports at the completion of Lab #1, Lab #2 and Lab #3 activities. These reports provide you with the opportunity to demonstrate your understanding of the material, and draw on various concepts and techniques covered in this and other courses in the program.

The Lab Report submission due dates are:

- Lab 1 (12%) - Friday, 29 March, 2024 at 23:59
- Lab 2 (12%) - Friday, 10 May, 2024 at 23:59
- Lab 3 (12%) - Friday, 7 June, 2024 at 23:59

Each laboratory report will have marks reserved for interesting and successfully implemented extensions.

Mapping to course learning outcomes: LO1, LO2, LO3, LO4

Assessment Length

No longer than 6 pages

Assignment submission Turnitin type

This assignment is submitted through Turnitin and students do not see Turnitin similarity reports.

Final Examination

Assessment Overview

Covers all class material (2hrs)

Detailed Assessment Description

Mapping to course learning outcomes: LO1, LO2, LO3, LO4

Assessment Length

2 hours

Assignment submission Turnitin type

Not Applicable

Take Home Tests

Assessment Overview

Three take home tests (worth 8% each)

Detailed Assessment Description

Three take home tests will be run, linked to units 1, 2 and 3 respectively.

The THT submission due dates are:

- THT1 (8%) - Thursday, 21 March, 2024 at 23:59
- THT2 (8%) - Thursday, 2 May, 2024 at 23:59
- THT3 (8%) - Thursday, 30 May, 2024 at 23:59

Mapping to course learning outcomes: LO1, LO2, LO3

Assessment Length

Each Take Home Test will be given 60hrs to complete.

Assignment submission Turnitin type

This is not a Turnitin assignment

General Assessment Information

THT1 will be due in week 4, feedback and grades will be given to students during week 4.

Standard UNSW late assessment policy applies in this class:

- Unless prior arrangement is made with the lecturer or a formal application for special consideration is submitted, a penalty of 5% of the total available mark for the assessment will apply for each day that an assessment item is late up to a maximum of 5 days (120 hours) after which an assessment can no longer be submitted and a grade of 0 will be applied.
- no permitted variation.

Generative AI is a tool that should be used with utmost care. It can often get confused and hallucinate information that ends up providing the user with incorrect and/or irrelevant information given the specified context. Irrelevant (but correct) information is likely to be ignored in marking; non-citability of AI-generated information is a further likely detriment against evaluation of understanding. THT questions are regularly checked against generative AI tools.

Grading Basis

Standard

Requirements to pass course

In order to satisfactorily complete this course students must achieve an overall mark of 50% or greater in the overall course assessment.

Course Schedule

Teaching Week/Module	Activity Type	Content
Week 1 : 26 February - 1 March	Lecture	U1 L1 Number Systems U1 L2 Basic Logic Gates
	Laboratory	LAB 1 - Introduction to C
Week 2 : 4 March - 8 March	Lecture	U1 L3 Combinational Logic and Boolean Algebra U1 L4 Semiconductors and Logic Families
	Laboratory	LAB 1 - Introduction to C
Week 3 : 11 March - 15 March	Lecture	U1 L5 Multilevel Logic and Karnaugh Maps
	Laboratory	LAB 1 - Introduction to C (Friday session only)
Week 4 : 18 March - 22 March	Lecture	U1 Review U2 L1 Flip-Flops
	Laboratory	LAB 1 - Introduction to C (Monday session only)
	Assessment	THT1
Week 5 : 25 March - 29 March	Lecture	U2 L2 Registers
	Laboratory	LAB 2 - Successive Approximation Converter (Monday session only)
	Assessment	Lab 1 Report
Week 6 : 1 April - 5 April	Lecture	U2 L3 Adders, Subtractors and ALUs
	Laboratory	LAB 2 - Successive Approximation Converter (Friday session only)
Week 7 : 22 April - 26 April	Lecture	U2 L4 ALUs + Other Operations U2 L5 DAC, ADC and Quantisation
	Laboratory	LAB 2 - Successive Approximation Converter
Week 8 : 29 April - 3 May	Lecture	U2 Review U3 L1 Microcontrollers and Interrupts
	Laboratory	LAB 2 - Successive Approximation Converter
	Assessment	THT2
Week 9 : 6 May - 10 May	Lecture	U3 L2 555 Timer
	Laboratory	No lab sessions due to days missed
	Assessment	Lab 2 Report
Week 10 : 13 May - 17 May	Lecture	U3 L3 LCD Displays U3 L4 Sensors
	Laboratory	LAB 3 - UART + LCD displays
Week 11 : 20 May - 24 May	Lecture	U3 L5 DC, Servo, and Stepper Motors U3 Review
	Laboratory	LAB 3 - UART + LCD displays
Week 12 : 27 May - 31 May	Lecture	U4 L1 UART U4 L2 SPI and I2C
	Laboratory	LAB 3 - UART + LCD displays
	Assessment	THT3
Week 13 : 3 June - 7 June	Lecture	U4 L3 Modulation and Multiplexing U4 L4 Other Interfaces
	Laboratory	Lab slot may be used for catch-up
	Assessment	Lab 3 Report

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

General Schedule Information

The following days are missed:

Canberra Day - Monday, 11 March, lost

Good Friday - Friday, 29 March, lost

Easter Monday - Monday, 1 April, lost

Military Training Day - Friday, 10 May, lost

Reconciliation Day - Monday, 27 May - delivered on Tuesday, 28 May

Course Resources

Prescribed Resources

Sarah Harris and David Harris. 2015. Digital Design and Computer Architecture: ARM Edition (1st. ed.). Morgan Kaufmann Publishers Inc., San Francisco, CA, USA

Recommended Resources

Neal Widmer, Greg Moss and Ronald Tocci. 2017. Digital Systems: Principles and Applications, Global Edition, (12th ed.). Pearson Higher Ed, USA

Additional Costs

N/A

Course Evaluation and Development

Following past feedback, the number of laboratories is reduced from four to three. This will give a little more time for laboratories 1 and 2, while combining the learning outcomes of 3 and 4 into the new lab 3.

One of the key priorities in the 2025 Strategy for UNSW is a drive for academic excellence in education. One of the ways of determining how well UNSW is progressing towards this goal is by listening to our own students. Students will be asked to complete the myExperience survey towards the end of this course.

Students can also provide feedback during the semester via: direct contact with the lecturer, the “On-going Student Feedback” link in Moodle, Student-Staff Liaison Committee meetings in schools, informal feedback conducted by staff, and focus groups. Student opinions really do make a difference. Refer to the Moodle site for this course to see how the feedback from previous students has contributed to the course development.

Important note: Students are reminded that any feedback provided should be constructive and professional and that they are bound by the Student Code of Conduct Policy

https://www.gs.unsw.edu.au/policy/documents/studentcodepolicy.pdf

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Convenor	Andrey Alenin		Bldg 16 Room 206	02 5114 5114	On Request	Yes	Yes
Lecturer	Edwin Peters		Bldg 16 Room 220		On request	No	No
Demonstrator	Khalil As'Ham				On request	No	No

Other Useful Information

Academic Information

Course Evaluation and Development

One of the key priorities in the 2025 Strategy for UNSW is a drive for academic excellence in education. One of the ways of determining how well UNSW is progressing towards this goal is by listening to our own students. Students will be asked to complete the myExperience survey towards the end of each course.

Students can also provide feedback during the semester via: direct contact with the lecturer, the “On-going Student Feedback” link in Moodle, Student-Staff Liaison Committee meetings in schools, informal feedback conducted by staff, and focus groups (where applicable). Student opinions really do make a difference. Refer to the Moodle site for your course to see how the feedback from previous students has contributed to the course development.

Important note: Students are reminded that any feedback provided should be constructive and professional and that they are bound by the Student Code of Conduct.

https://www.gs.unsw.edu.au/policy/documents/studentcodepolicy.pdf

Equitable Learning Services (ELS)

Students living with neurodivergent, physical and/or mental health conditions or caring for someone with these conditions may be eligible for support through the Equitible Learning Services team. Equitable Learning Services is a free and confidential service that provides practical support to ensure your mental or physical health conditions do not adversely affect your studies.

Our team of dedicated **Equitable Learning Facilitators** (ELFs) are here to assist you through this process. We offer a number of services to make your education at UNSW easier and more equitable.

Further information about ELS for currently enrolled students can be found at: https://www.student.unsw.edu.au/equitable-learning

Academic Honesty and Plagarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW staff and students have a responsibility to adhere to this principle of academic integrity. All students are expected to adhere to UNSW's Student Code of Conduct. Find relevant information at: Student Code of Conduct (unsw.edu.au)

Plagiarism undermines academic integrity and is not tolerated at UNSW. It is defined as using the words or ideas of others and passing them off as your own, and can take many forms, from deliberate cheating to accidental copying from a source without acknowledgement.

For more information, please refer to the following:

https://student.unsw.edu.au/plagiarism

Submission of Assessment Tasks

Special Consideration

Special Consideration is the process for assessing and addressing the impact on students of short-term events, that are beyond the control of the student, and that affect performance in a specific assessment task or tasks.

Applications for Special Consideration will be accepted in the following circumstances only:

- Where academic work has been hampered to a substantial degree by illness or other cause;
- The circumstances are unexpected and beyond the student's control;
- The circumstances could not have reasonably been anticipated, avoided or guarded against by the student; and either:

(i) they occurred during a critical study period and was 3 consecutive days or more duration, or a total of 5 days within the critical study period; or

(ii) they prevented the ability to complete, attend or submit an assessment task for a specific date (e.g. final exam, in class test/quiz, in class presentation)

Applications for Special Consideration must be made as soon as practicable after the problem occurs and at the latest within three working days of the assessment or the period covered by the supporting documentation.

By sitting or submitting the assessment task the student is declaring that they are fit to do so and cannot later apply for Special Consideration (UNSW 'fit to sit or submit' requirement).

Sitting, accessing or submitting an assessment task on the scheduled assessment date, after applying for special consideration, renders the special consideration application void.

Find more information about special consideration at: https://www.student.unsw.edu.au/special/consideration/guide

Or apply for special consideration through your MyUNSW portal.

Late Submission of assessment tasks (other than examinations)

UNSW has a standard late submission penalty of:

- 5% per day,
- capped at five days (120 hours) from the assessment deadline, after which a student cannot submit an assessment, and
- no permitted variation.

Students are expected to manage their time to meet deadlines and to request extensions as early as possible before the deadline.

Electronic submission of assessment

Except where the nature of an assessment task precludes its electronic submission, all assessments must be submitted to an electronic repository, approved by UNSW or the Faculty, for archiving and subsequent marking and analysis.

Release of final mark

All marks obtained for assessment items during the session are provisional. The final mark as published by the university following the assessment review group meeting is the only official

mark.