UNSW Course Outline

COMP3222 Digital Circuits and Systems - 2024

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General Course Information

Course Code : COMP3222
Year : 2024
Term : Term 3
Teaching Period : T3
Is a multi-term course? : No
Faculty : Faculty of Engineering
Academic Unit : School of Computer Science and Engineering
Delivery Mode : In Person
Delivery Format : Standard
Delivery Location : Kensington
Campus : Sydney
Study Level : Undergraduate
Units of Credit : 6

Useful Links

Handbook Class Timetable

Course Details & Outcomes

Course Description

This course teaches students the fundamentals of digital design.

The course introduces the components of digital systems, explains how these are described in

the VHDL hardware description language and familiarizes the student with the implementation of digital circuits using FPGA prototyping boards.

Course Aims

This course aims to provide students with a knowledge of designing and implementing simple digital logic circuits & systems. The basic building blocks of combinational and sequential circuits are introduced to enable students to develop circuit solutions to problems and to understand the design and operation of hardware models of digital systems. Students are introduced to the VHDL hardware description language as a means of describing circuits. Computer-aided design tools are used to specify, simulate and implement a variety of simple digital systems. Students learn how to implement and test their designs using Field-Programmmable Gate Arrays.

As an introductory course, a principal aim is to prepare students for more advanced study in follow-on courses.

Relationship to Other Courses

Along with microprocessor design and assembly language programming, the study and design of digital circuits using CAD tools and targeting FPGAs are fundamental computer engineering skills. COMP3222 leads on to studies in computer architecture and embedded systems design in 3rd and 4th years of the computer engineering program. We build on your understanding of physical, electrical and computational principles acquired in your 1st year of studies.

Course Learning Outcomes

Course Learning Outcomes
CLO1 : Design and implement combinational and synchronous sequential logic circuits
CLO2 : Analyse combinational and sequential digital logic circuits
CLO3 : Describe hardware functions using a hardware description language
CLO4 : Make use of CAD tools to specify, simulate and synthesize circuit designs
CLO5 : Perform the steps involved in digital circuit implementation using Field-Programmable Gate Arrays

Course Learning Outcomes	Assessment Item
CLO1 : Design and implement combinational and synchronous sequential logic circuits	• Final Practical Test • Final Theory Test • Labs • Fortnightly quizzes
CLO2 : Analyse combinational and sequential digital logic circuits	• Final Practical Test • Final Theory Test • Labs • Fortnightly quizzes
CLO3 : Describe hardware functions using a hardware description language	• Final Practical Test • Final Theory Test • Labs • Fortnightly quizzes
CLO4 : Make use of CAD tools to specify, simulate and synthesize circuit designs	• Final Practical Test • Labs
CLO5 : Perform the steps involved in digital circuit implementation using Field-Programmable Gate Arrays	• Final Practical Test • Labs

Learning and Teaching Technologies

Moodle - Learning Management System | Echo 360 | EdStem | WebCMS3

Learning and Teaching in this course

An in-depth understanding of digital circuits and systems is fundamental to your ability to become a successful digital designer and computer engineer.

This course founds studies in computer architecture, embedded systems and configurable logic design, and also forms the basis for a deeper understanding of the hardware underpinnings of operating systems, compilers, networks, graphics systems, etc.

In this course we attempt to provide you with a rigorous and thorough grounding in the essential skills you will need to carry out digital design activities in the follow-on courses of Computer Architecture, Embedded Systems Design (Design Project A) and Configurable Systems Design (Design Project B).

To that end, we aim to provide a systematic, bottom-up coverage of the essential skills and theory, and to provide a top-down view of the broader area to motivate and highlight the interrelationship of the topics.

In order to learn, students are expected to play an active role in participating by continuously thinking about *HOW* what is said in lectures or read in texts or on the web relates to what you already know from this course and related studies. You are encouraged and expected to ask questions to clarify contradictions or uncertainties in your understanding as we proceed.

In this course, we also place considerable value on putting theory into practice through guided laboratory and virtual classroom exercises. Staying up-to-date with these will help enormously in picking up the skills we expect you to have acquired by the end of the course.

This course will involve:

- Lecture recordings, to introduce concepts, show examples
- F2F and on-line discussions of the lecture material and tutorial exercises
- Self-directed lab work, to introduce technology and put theory into practice
- Recordings, F2F, and on-line drop-in sessions, to assist with the completion of lab work.

The course will also involve:

- Practical Test, to encourage active participation in laboratory work and to determine whether acquired skill levels are sufficient to pass the course, and
- Fortnightly quizzes as well as a Theory Test, to encourage study and more formally gauge uptake of theory.

Students are encouraged to discuss their work with fellow students as well as the demonstrators and lecturer. However, each student is expected to write their own code and to submit solutions they can confidently claim as their own. Sharing lab files is not considered fair practice.

Quizzes are primarily intended to encourage you to study and stay up to date with the theory, rather than to provide confirmation of what you have understood or still need to work on. Given the reasonably straightforward nature of the theory covered, if you don't know how to approach the solution to a problem, that's potentially a sign that you need to work on your understanding

and/or seek help with that aspect of the theory. So please ask.

A forum is provided on the course website. We encourage you to ask questions on the forum, particularly if you think you won't be the only one curious to have an answer. The forum is monitored on weekdays by the lecturer and lab demonstrators for them to respond in a reasonable timeframe. If you need help, please allow enough time for them to be able to respond. Feel free to email the lecturer or lab demonstrators if you feel they may have missed your question on the forum.

Other Professional Outcomes

Relevant professional framework

https://www.acm.org/binaries/content/assets/education/ce2016-final-report.pdf

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates
Final Practical Test Assessment Format: Individual	30%	Start Date: End of term exam period Due Date: Not Applicable
Final Theory Test Assessment Format: Individual	15%	Start Date: End of term exam period Due Date: Not Applicable
Labs Assessment Format: Individual	40%	Start Date: See Course Schedule Due Date: Midnight Monday, the week after the lab is scheduled.
Fortnightly quizzes Assessment Format: Individual	15%	Start Date: Weeks 3, 5, 7 & 9 Due Date: Not Applicable

Assessment Details

Final Practical Test

Assessment Overview

The invigilated Final Practical Test assesses the acquisition of theoretical and practical skills needed to implement digital circuits using FPGAs.

Course Learning Outcomes

- CLO1 : Design and implement combinational and synchronous sequential logic circuits
- CLO2 : Analyse combinational and sequential digital logic circuits
- CLO3 : Describe hardware functions using a hardware description language
- CLO4 : Make use of CAD tools to specify, simulate and synthesize circuit designs

- CLO5 : Perform the steps involved in digital circuit implementation using Field-Programmable Gate Arrays

Detailed Assessment Description

A two-hour open book exam involving the design, implementation and testing of a small digital system.

Offline aids are permitted. Online aids are not permitted.

You must score 40% of the available marks for this component to pass the course.

Assessment Length

2 hours

Assessment information

Open book; no Internet access

Assignment submission Turnitin type

Not Applicable

Hurdle rules

Students must achieve 40% of the available marks in this component and achieve at least 50% over all assessments in order to pass the course

Generative AI Permission Level

No Assistance

This assessment is designed for you to complete without the use of any generative AI. You are not permitted to use any generative AI tools, software or service to search for or generate information or answers.
For more information on Generative AI and permitted use please see here.

Final Theory Test

Assessment Overview

The Final Theory Test is a written paper that provides an invigilated individual assessment of theory learning in the course.

Course Learning Outcomes

- CLO1 : Design and implement combinational and synchronous sequential logic circuits
- CLO2 : Analyse combinational and sequential digital logic circuits

- CLO3 : Describe hardware functions using a hardware description language

Detailed Assessment Description

A one-hour open book short and long answer paper.

Offline aids permitted. Online aids not permitted.

Assessment Length

1 hour

Assessment information

Open book; no Internet access

Assignment submission Turnitin type

Not Applicable

Generative AI Permission Level

No Assistance

This assessment is designed for you to complete without the use of any generative AI. You are not permitted to use any generative AI tools, software or service to search for or generate information or answers.
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Labs

Assessment Overview

Weekly lab exercises aligned with theory provided in lectures. Labs increase in complexity from simple components to complete processors.

Students need to plan, design, implement and test the required circuits.

Demonstrators mark submitted labs and provide individual written feedback.

Course Learning Outcomes

- CLO1 : Design and implement combinational and synchronous sequential logic circuits
- CLO2 : Analyse combinational and sequential digital logic circuits
- CLO3 : Describe hardware functions using a hardware description language
- CLO4 : Make use of CAD tools to specify, simulate and synthesize circuit designs
- CLO5 : Perform the steps involved in digital circuit implementation using Field-Programmable Gate Arrays

Detailed Assessment Description

Completed designs, code and simulation testbenches are submitted at midnight on the Monday after the week in which the lab is completed.

Submission notes

Use WebCMS3 to submit labs

Assignment submission Turnitin type

This is not a Turnitin assignment

Generative AI Permission Level

No Assistance

This assessment is designed for you to complete without the use of any generative AI. You are not permitted to use any generative AI tools, software or service to search for or generate information or answers.
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Fortnightly quizzes

Assessment Overview

Fortnightly multiple-choice quizzes are held using Moodle to encourage learning and practice.

Scores are provided as feedback.

Course Learning Outcomes

- CLO1 : Design and implement combinational and synchronous sequential logic circuits
- CLO2 : Analyse combinational and sequential digital logic circuits
- CLO3 : Describe hardware functions using a hardware description language

Detailed Assessment Description

These quizes are intended to encourage students to keep up with the material being presented in class.

Assessment Length

15 minutes each quiz

Submission notes

Complete online, using Moodle

Assessment information

Each quiz comprises 5 multiple choice questions covering the lecture material up to and including the previous week.

This is an online quiz in which you are unable to review your answers to prior questions (go back). Answers are not provided. You will be provided with your score, which is a gauge of your understanding, in the day or two following the quiz.

Assignment submission Turnitin type

Not Applicable

Generative AI Permission Level

No Assistance

This assessment is designed for you to complete without the use of any generative AI. You are not permitted to use any generative AI tools, software or service to search for or generate information or answers.
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General Assessment Information

Assessment details will be discussed during the first lecture.

Grading Basis

Standard

Requirements to pass course

Gain a **minimum of 40% in the final practical test** and a combined minimum of 50% over all of the assessments in the course.

Course Schedule

Teaching Week/Module	Activity Type	Content
Week 1 : 9 September - 15 September	Lecture	Introduction & simplifying circuits; Ch 1 & 2 Optimizing logic functions; Ch 4.1-4.7 & 4.12
	Laboratory	Introduction to Vivado and digital circuit implementation
Week 2 : 16 September - 22 September	Lecture	Number representation & arithmetic circuits; Ch 5.1-5.5
	Laboratory	Switches, Lights, and Multiplexers
Week 3 : 23 September - 29 September	Lecture	Combinational circuit blocks; Ch 6
	Laboratory	Numbers and Displays
	Online Activity	Fortnightly quiz on material of Weeks 1 & 2
Week 4 : 30 September - 6 October	Lecture	Flip-flops, Registers & Counters; Ch 7.1-7.16
	Laboratory	Latches, Flip-flops, and Registers
Week 5 : 7 October - 13 October	Lecture	Synchronous sequential circuits; Ch 8.1-8.9
	Laboratory	Counters
	Online Activity	Fortnightly quiz on material of Weeks 1 - 4
Week 6 : 14 October - 20 October	Other	Flexibility week
	Laboratory	Finite State Machines
Week 7 : 21 October - 27 October	Lecture	Digital system design; Ch 10
	Laboratory	Finite State Machines (continued)
	Online Activity	Fortnightly quiz on material of Weeks 1 - 5
Week 8 : 28 October - 3 November	Lecture	Digital system design (continued); Ch 10
	Laboratory	Simple Processor
Week 9 : 4 November - 10 November	Lecture	Blackjack player Implementation technology; Ch 3
	Laboratory	Implementing Algorithms in Hardware
	Online Activity	Fortnightly quiz on material of Weeks 1 - 8
Week 10 : 11 November - 17 November	Lecture	Course wrap-up
	Laboratory	Implementing Algorithms in Hardware (continued)

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

General Schedule Information

Students are encouraged to attend lectures and expected to attend labs each week to seek assistance with their lab work.

Like most courses at UNSW, your results in the course will reflect the amount of effort you invest in your learning. As a guide, an allocation of 15 total hours of attendance and private study per week for a 6 UoC course such as COMP3222 should see you doing well. You will need to adjust this general advice to meet your own objectives and needs.

Please consult the lecturer or the lab demonstrators if you would like advice on the course.

Course Resources

Prescribed Resources

Lab Kits

Lab kits will be handed out to students during Weeks 1 & 2. These kits are delicate and expensive to replace. We therefore ask that you take care of your kit until the final practical exam. Further information will be provided at that time for how to return your lab kit.

Should you discontinue the course, please return your kit as soon as practical to avoid inconvenience to yourself and the School. ***We may seek to recover from you the replacement cost of lost or unreturned kits (currently AUD 250). In addition, you may have a financial block placed on your ZID and be thereby prevented from further enrolment at UNSW until the kit is returned.***

Course textbook:

- Stephen Brown & Zvonko Vranesic, Fundamentals of Digital Logic with VHDL Design, 3ed, McGraw-Hill, 2009

Useful references:

- Katz and Borriello, Contemporary Logic Design (2nd edition)
- Mano and Kime, Logic and Computer Design Fundamentals (3rd Edition)

Other resources:

- AMD Xilinx on-line User Guides and Data Sheets

Course Evaluation and Development

This course is evaluated each session using myExperience. Your feedback is highly appreciated. Students are encouraged to provide feedback or discuss the course at any time either in person or by emailing the lecturer.

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Lecturer	Oliver Diessel		K17-501B	93857384	Office hours	Yes	Yes

Other Useful Information

Academic Information

I. Special consideration and supplementary assessment

If you have experienced an illness or misadventure beyond your control that will interfere with your assessment performance, you are eligible to apply for Special Consideration prior to, or within 3 working days of, submitting an assessment or sitting an exam.

Please note that UNSW has a Fit to Sit rule, which means that if you sit an exam, you are declaring yourself fit enough to do so and cannot later apply for Special Consideration.

For details of applying for Special Consideration and conditions for the award of supplementary assessment, please see the information on UNSW's Special Consideration page.

II. Administrative matters and links

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Attendance
- UNSW Email Address
- Special Consideration
- Exams
- Approved Calculators
- Academic Honesty and Plagiarism
- Equitable Learning Services

III. Equity and diversity

Those students who have a disability that requires some adjustment in their teaching or learning environment are encouraged to discuss their study needs with the course convener prior to, or at the commencement of, their course, or with the Equity Officer (Disability) in the Equitable Learning Services. Issues to be discussed may include access to materials, signers or note-takers, the provision of services and additional exam and assessment arrangements. Early notification is essential to enable any necessary adjustments to be made.

IV. Professional Outcomes and Program Design

Students are able to review the relevant professional outcomes and program designs for their streams by going to the following link: https://www.unsw.edu.au/engineering/student-life/student-resources/program-design.

Note: This course outline sets out the description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle or your primary learning management system (LMS) should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline/Moodle/LMS, the description in the Course Outline/Moodle/LMS applies.

Academic Honesty and Plagarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. *Plagiarism at UNSW is defined as using the words or ideas of others and passing them off as your own.*

Plagiarism is a type of intellectual theft. It can take many forms, from deliberate cheating to accidentally copying from a source without acknowledgement. UNSW has produced a website with a wealth of resources to support students to understand and avoid plagiarism, visit: student.unsw.edu.au/plagiarism. The Learning Centre assists students with understanding academic integrity and how not to plagiarise. They also hold workshops and can help students one-on-one.

You are also reminded that careful time management is an important part of study and one of the identified causes of plagiarism is poor time management. Students should allow sufficient time for research, drafting and the proper referencing of sources in preparing all assessment tasks.

Repeated plagiarism (even in first year), plagiarism after first year, or serious instances, may also be investigated under the Student Misconduct Procedures. The penalties under the procedures can include a reduction in marks, failing a course or for the most serious matters (like plagiarism in an honours thesis or contract cheating) even suspension from the university. The Student Misconduct Procedures are available here:

www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf

Submission of Assessment Tasks

Work submitted late without an approved extension by the course coordinator or delegated authority is subject to a late penalty of five percent (5%) of the maximum mark possible for that assessment item, per calendar day.

The late penalty is applied per calendar day (including weekends and public holidays) that the assessment is overdue. There is no pro-rata of the late penalty for submissions made part way through a day. This is for all assessments where a penalty applies.

Work submitted after five days (120 hours) will not be accepted and a mark of zero will be awarded for that assessment item.

For some assessment items, a late penalty may not be appropriate. These will be clearly indicated in the course outline, and such assessments will receive a mark of zero if not completed by the specified date. Examples include:

- Weekly online tests or laboratory work worth a small proportion of the subject mark;
- Exams, peer feedback and team evaluation surveys;
- Online quizzes where answers are released to students on completion;
- Professional assessment tasks, where the intention is to create an authentic assessment that has an absolute submission date; and,
- Pass/Fail assessment tasks.

Faculty-specific Information

Engineering Student Support Services – The Nucleus - enrolment, progression checks, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries e.g. admissions, fees, programs, credit transfer

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

School Contact Information

CSE Help! - on the Ground Floor of K17

- For assistance with coursework assessments.

The Nucleus Student Hub - https://nucleus.unsw.edu.au/en/contact-us

- Course enrolment queries.

Grievance Officer - grievance-officer@cse.unsw.edu.au

- If the course convenor gives an inadequate response to a query or when the courses convenor does not respond to a query about assessment.

Student Reps - stureps@cse.unsw.edu.au

- If some aspect of a course needs urgent improvement. (e.g. Nobody responding to forum queries, cannot understand the lecturer)

You should **never** contact any of the following people directly:

- Vice Chancellor

- Pro-vice Chancellor Education (PVCE)

- Head of School

- CSE administrative staff

- CSE teaching support staff

They will simply bounce the email to one of the above, thereby creating an unnecessary level of indirection and a delay in the response.