**UNSW Course Outline**

# ELEC4602 Microelectronic Design and Technology - 2024

Published on the  30 Aug 2024

## General Course Information

**Course Code :**  ELEC4602
**Year :**  2024
**Term :**  Term 3
**Teaching Period :**  T3
**Is a multi-term course? :**  No
**Faculty :**  Faculty of Engineering
**Academic Unit :**  School of Electrical Engineering & Telecommunications
**Delivery Mode :**  In Person
**Delivery Format :**  Standard
**Delivery Location :**  Kensington
**Campus :**  Sydney
**Study Level :**  Postgraduate, Undergraduate
**Units of Credit :**  6

<u>Useful Links</u>

<u>Handbook</u> <u>Class Timetable</u>

## Course Details & Outcomes

### Course Description

Microelectronics or integrated electronics is the miniaturised electronic circuits that make up
Integrated Circuits (ICs) such as microprocessors, Field-Programmable Gate Arrays, Flash-
memories, operational amplifier, analogue-to-digital converters, SoCs, ASICs and many other

devices. Most ICs today are implemented in various flavours of CMOS technology which is the focus of this course. The ability to use a large number of components at a relatively low cost and the ability to match components accurately on-chip makes the design of integrated circuits and systems different from a similar design using discrete components. Microelectronics Design and Technology is a broad-based, introductory IC design course, which takes the student through all the necessary steps in order to complete (ready-to-manufacture) a basic mixed-signal front-end in a typical integrated system.

Course content includes: basic IC processing technology: lithography, oxidation, diffusion, implantation, film deposition, etching, metalisation. CMOS IC technologies. MOS device models. On-chip components: transistors, capacitors, inductors, resistors, diodes. CMOS design rules, scaling. Tapeout and MPW, floor planning, cell layout and routing. CAD tools. Corner and Monte Carlo simulations. CMOS analogue building blocks: amplifier stages, current mirrors, active loads. Noise sources and analysis. CMOS operational amplifiers, samplers and comparators. D/A converters and A/D converters. Static CMOS gates. Device sizing. Flip-flops. CMOS digital building blocks: level shifters, decoders, multiplexers, tri-states, buffers and adders. Memories: ROM, SRAM and DRAM cell design; sense amplifiers.

## Course Aims

The course builds on the knowledge gained in the first three years of studying electrical engineering and provides students with more advanced electronic circuit design skills.

The course aims to make students familiar with CMOS microelectronics technologies and enable them to analyse and design circuits implemented using these technologies.

## Relationship to Other Courses

This is a 4th year course in the School of Electrical Engineering and Telecommunications. It is a professional elective course for students following a BE (Electrical) or (Telecommunications) program and other combined degree programs.

**Pre-requisites and Assumed Knowledge**

The pre-requisite for this course is ELEC3106, Electronics. It is essential that you have good working knowledge of circuit theory, basic analogue and digital electronics, and basic signal analysis as covered in the courses ELEC1112, Electrical Circuits, ELEC2133, Analogue Electronics, ELEC2141, Digital Circuit Design, and ELEC2134, Circuits and Signals. It is finally assumed that you are proficient in the use of personal computers.

**Following Courses**

The course is a co-requisite for the post-graduate course ELEC9701, Mixed Signal Microelectronics Design. The course is also a co-requisite for thesis work in the area of integrated circuit design.

# Course Learning Outcomes

| Course Learning Outcomes |
|---|
| CLO1 : Recognise capabilities and limitations of current microelectronic (or IC) technologies |
| CLO2 : Apply modern CAD design tools to design ICs |
| CLO3 : Create IC layouts |
| CLO4 : Apply circuit models of IC components |
| CLO5 : Analyse analogue and digital microelectronic circuits |
| CLO6 : Design basic analogue, digital and mixed microelectronic circuits |

| Course Learning Outcomes | Assessment Item |
|---|---|
| CLO1 : Recognise capabilities and limitations of current microelectronic (or IC) technologies | • Laboratory work<br>• Design task<br>• Final examination |
| CLO2 : Apply modern CAD design tools to design ICs | • Laboratory work<br>• Design task |
| CLO3 : Create IC layouts | • Final examination<br>• Laboratory work |
| CLO4 : Apply circuit models of IC components | • Quizzes<br>• Design task<br>• Final examination |
| CLO5 : Analyse analogue and digital microelectronic circuits | • Quizzes<br>• Final examination |
| CLO6 : Design basic analogue, digital and mixed microelectronic circuits | • Design task<br>• Final examination |

# Learning and Teaching Technologies

Moodle - Learning Management System | Course website | Echo 360

# Learning and Teaching in this course

**Delivery mode**

- Lecture recordings and following Q&A sessions, which provide students with a focus on the core analytical material in the course, together with qualitative, alternative explanations and individually targeted illustrations to aid student understanding.
- Self-guided tutorials, which allow for exercises in problem solving and allow time for students to resolve in-depth problems for quantitative understanding of the lecture material.
- Computer laboratory sessions, which support, via detailed simulations using state-of-the art CAD tools, the formal lecture material and also provide students with practical design, and debugging skills.
- A design task, which draws together theoretical and practical design aspects in an open-ended realistic design problem, reinforcing the course material.

## Learning in this course

You are expected to watch all lecture recordings and attend all Q&A sessions, labs, tutorials and quizzes in order to maximise your learning. You must prepare well for your laboratory classes and your lab work will be assessed. You should read relevant sections of the recommended texts. For most topics, lecture notes will not be given: reading and reflecting on the recommended texts and identify critical parts with the aid of the lectures is an essential component of this course. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW assumes that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

## Lecture recordings and Q&A sessions

During the lecture recordings technology capabilities and design issues are discussed and theoretical aspects of IC design and technology are presented. Numerous examples of analogue and digital integrated circuit functions are discussed in order to convey a qualitative understanding of circuit operations. You are encouraged to actively engage in the Q&A sessions to facilitate two-way communication and enhance learning. The lecture recordings and Q&A sessions aim to support you in analysing and designing integrated circuits, and to help you appreciate the capabilities of IC technologies.

## Self-guided tutorials

You should attempt all of your problem sheet questions as indicated in the tutorial schedule. Group learning is encouraged. Answers for these questions will be discussed during the Q&A sessions or during the consultation time.

## Laboratory Program

The laboratory work provides you with hands-on design experience and exposure to state-of-the-art CAD tools. The laboratory thus enables you to use these tools for IC circuit design, analysis and lay-out, and re-enforces the central topics in the course. Verifying circuit functions by simulations also train you in best-practice IC verification and exercises your ability to locate circuit errors.

**Design Task**

The design task aims to draw together theoretical and practical design aspects in an open-ended realistic design problem. You will design an integrated circuit meeting given specifications, use the CAD tools to verify the circuit operation and write a report documenting your design. The design task provide and test engineering creativity, open-ended problem solving skills, communication skills and general understanding of the course content. You may use the CAD tools in rooms G17-202/G17-209/G17-217 for this task. You may also use up to 1 h/week of the scheduled laboratory time for the design task where demonstrators can assist you.

# Other Professional Outcomes

**Relationship to Engineers Australia Stage 1 competencies:**

The Course Learning Outcomes (LOs) contribute to the Engineers Australia (National Accreditation Body) Stage I competencies as outlined below

**Engineers Australia (EA), Professional Engineer Stage 1 Competencies**

*PE1: Knowledge and Skill Base:*

PE1.1 Comprehensive, theory-based **understanding of underpinning fundamentals**: LO 5

PE1.2 Conceptual understanding of underpinning maths, **analysis**, statistics, **computing**: LO 4, 5

PE1.3 In-depth understanding of specialist bodies of **knowledge**: LO 1, 2, 3, 4, 5, 6

PE1.4 Discernment of knowledge development and research directions: LO 1

PE1.5 Knowledge of **engineering design** practice: LO 2, 3, 4, 5, 6

PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice: NA

*PE2: Engineering Application Ability:*

PE2.1 Application of established engineering methods to **complex problem solving**: LO 3, 5, 6

PE2.2 Fluent **application of engineering techniques**, tools and resources: LO 2, 3, 5, 6

PE2.3 Application of systematic engineering synthesis and design processes: LO 3, 5, 6

PE2.4 Application of systematic approaches to the conduct and management of engineering projects: NA

*PE3: Professional and Personal Attributes:*

PE3.1 Ethical conduct and professional accountability: NA

PE3.2 Effective **oral and written communication** (professional and lay domains): LO 2, 3, 6

PE3.3 **Creative, innovative** and pro-active demeanour: LO 6

PE3.4 Professional use and management of information: LO 6

PE3.5 Orderly management of **self, and professional conduct**: LO 6

PE3.6 Effective team membership and team leadership: NA

This course is also designed to provide the course learning outcomes which arise from targeted graduate capabilities. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (also listed below).

## Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

## UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of

core UNSW graduate capabilities, as follows:

- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems, through laboratory experiments and tutorial exercises.
- Developing capable independent and collaborative enquiry, through tutorials exercises.
- Developing digital and information literacy and lifelong learning skills, through lectures, class preparations and  report writing.
- Developing the capability of effective communication, through report writing.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through the design task.

https://www.unsw.edu.au/engineering/student-life/student-resources/program-design

# Assessments

## Assessment Structure

| Assessment Item | Weight | Relevant Dates |
|---|---|---|
| Laboratory work<br>Assessment Format: Group | 15% | Start Date: Not Applicable |
| Quizzes<br>Assessment Format: Individual | 10% | Start Date: Not Applicable |
| Design task<br>Assessment Format: Group | 15% | Start Date: Not Applicable |
| Final examination<br>Assessment Format: Individual | 60% | Start Date: Not Applicable |

## Assessment Details
### Laboratory work

Assessment Overview

For each of the five laboratory exercises, the student's work will be assessed in class and on a short report.  A rubric will be used for marking and feedback given to each group online.

Course Learning Outcomes

- CLO1 : Recognise capabilities and limitations of current microelectronic (or IC) technologies
- CLO2 : Apply modern CAD design tools to design ICs
- CLO3 : Create IC layouts

Detailed Assessment Description

While laboratory work is primarily about learning, it is assessed to ensure that you understand the material in this essential course component. This assessment test that you can use the CAD tools, create IC layouts, understand circuit models and functions, carry out appropriate

simulations, and can design simple circuits.

You are required to maintain a lab book for recording your observations and you must bring a USB stick to capture screen shots or print-outs of your work for documentation. After completing each key lab component, your work will be assessed by the laboratory demonstrator, so make sure that your demonstrator notice your work. Laboratory work must be documented in brief reports which are due Monday the week after the laboratory session ending each exercise. Each report must be uploaded as a .pdf file (no other format accepted) on the course Moodle site.

<u>Submission notes</u>

See Moodle for laboratory report submission dates.

<u>Assessment information</u>

See Moodle for submission dates.

<u>Assignment submission Turnitin type</u>

Not Applicable

<u>Generative AI Permission Level</u>

**Simple Editing Assistance**

In completing this assessment, you are permitted to use standard editing and referencing functions in the software you use to complete your assessment. These functions are described below. You must not use any functions that generate or paraphrase passages of text or other media, whether based on your own work or not.

If your Convenor has concerns that your submission contains passages of AI-generated text or media, you may be asked to account for your work. If you are unable to satisfactorily demonstrate your understanding of your submission you may be referred to UNSW Conduct & Integrity Office for investigation for academic misconduct and possible penalties.

For more information on Generative AI and permitted use please see here.

## Quizzes

<u>Assessment Overview</u>

Two in-class quizzes will be held during lecture time. Marks will be assigned according to the correct fraction of the response. Verbal class-wide feedback will be given during lectures.

<u>Course Learning Outcomes</u>

- CLO4 : Apply circuit models of IC components

- CLO5 : Analyse analogue and digital microelectronic circuits

<u>Detailed Assessment Description</u>

There are two quizzes held during the lecture time through the term. These are designed to give early feedback on your progress through the theoretical components of the course and test your general understanding of the course material. Questions will be drawn from course material covered in the three-four weeks prior to each quiz.

<u>Submission notes</u>

See Moode for quiz dates and times.

<u>Assessment information</u>

See Moodle for assessment dates.

<u>Assignment submission Turnitin type</u>

Not Applicable

<u>Generative AI Permission Level</u>

**Simple Editing Assistance**

In completing this assessment, you are permitted to use standard editing and referencing functions in the software you use to complete your assessment. These functions are described below. You must not use any functions that generate or paraphrase passages of text or other media, whether based on your own work or not.

If your Convenor has concerns that your submission contains passages of AI-generated text or media, you may be asked to account for your work. If you are unable to satisfactorily demonstrate your understanding of your submission you may be referred to UNSW Conduct & Integrity Office for investigation for academic misconduct and possible penalties.

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## Design task

<u>Assessment Overview</u>

The design task will be carried out in open computer labs in addition to the scheduled laboratories. The work will be assessed on a submitted report. A rubric will be used for marking and feedback given to each group online.

<u>Course Learning Outcomes</u>

- CLO1 : Recognise capabilities and limitations of current microelectronic (or IC) technologies
- CLO2 : Apply modern CAD design tools to design ICs

- CLO4 : Apply circuit models of IC components
- CLO6 : Design basic analogue, digital and mixed microelectronic circuits

<u>Detailed Assessment Description</u>

The design task is assessed to test your ability to design a simple integrated circuit, thus also demonstrating your appreciation of the technology, your ability to use appropriate models and simulations, and your ability to conduct suitable analysis to aid in the design.

As for the other laboratory work, you should maintain a lab book and must record suitable screen shots or print-outs as documentation for your work. The design and verification work must be documented in a brief report which is due Monday the due week listed in the laboratory schedule. Each report must be uploaded as a .pdf file (no other format accepted) on the course Moodle site.

<u>Submission notes</u>

See Moodle for design report submission date.

<u>Assessment information</u>

See Moodle for submission date.

<u>Assignment submission Turnitin type</u>

Not Applicable

<u>Generative AI Permission Level</u>

**Simple Editing Assistance**

In completing this assessment, you are permitted to use standard editing and referencing functions in the software you use to complete your assessment. These functions are described below. You must not use any functions that generate or paraphrase passages of text or other media, whether based on your own work or not.

If your Convenor has concerns that your submission contains passages of AI-generated text or media, you may be asked to account for your work. If you are unable to satisfactorily demonstrate your understanding of your submission you may be referred to UNSW Conduct & Integrity Office for investigation for academic misconduct and possible penalties.

For more information on Generative AI and permitted use please see here.

# Final examination

<u>Assessment Overview</u>

The examination is a 2-hour open-book examination. Marks will be assigned according to the

correct fraction of the response.

## Course Learning Outcomes

- CLO1 : Recognise capabilities and limitations of current microelectronic (or IC) technologies
- CLO3 : Create IC layouts
- CLO4 : Apply circuit models of IC components
- CLO5 : Analyse analogue and digital microelectronic circuits
- CLO6 : Design basic analogue, digital and mixed microelectronic circuits

## Detailed Assessment Description

The exam in this course is an open-book 2 hour (nominal) written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including laboratories and design task), unless specifically indicated otherwise by the lecturer.

## Assessment information

Face-to-face during exam period.

## Assignment submission Turnitin type

Not Applicable

## Hurdle rules

An examination mark of at least 45% is required to pass the course.

## Generative AI Permission Level

No Assistance

This assessment is designed for you to complete without the use of any generative AI. You are not permitted to use any generative AI tools, software or service to search for or generate information or answers.

For more information on Generative AI and permitted use please see here.

# General Assessment Information

## Grading Basis

Standard

# Course Schedule

| Teaching Week/Module | Activity Type | Content |
|---|---|---|
| Week 1 : 9 September - 15 September | Lecture | CMOS processing technologies and components. Layout layers. IC layout and design rules. |
| | Reading | JB ch. 7, web, JB ch. 3, 4, 5. |
| | Laboratory | Lab 1: layout. |
| | Tutorial | Tute 1: layout. |
| Week 2 : 16 September - 22 September | Lecture | Design Synthesis and verification tools. Analogue MOS models. |
| | Reading | Web. JB ch. 9. |
| | Laboratory | Lab 1: continued. |
| | Tutorial | Tute 2: transistor models. |
| Week 3 : 23 September - 29 September | Lecture | Digital MOS models and device noise. Current mirrors. |
| | Reading | JB ch. 10, JB ch. 8, JB ch. 20. |
| | Laboratory | Lab 2: circuit simulation. |
| | Tutorial | Tute 3: single-stage amplifiers. |
| | Assessment | Lab 1 report due. |
| Week 4 : 30 September - 6 October | Lecture | Single-stage amplifiers. Operational amplifier design I. |
| | Reading | JB ch. 21, 22. |
| | Laboratory | Lab 3: op-amp design. |
| | Tutorial | Tute 4: op-amps. |
| | Assessment | Quiz 1. |
| Week 5 : 7 October - 13 October | Lecture | Operational amplifier design II. Comparators. Charge Injection. |
| | Reading | JB ch. 24, 27, JB ch. 25. |
| | Laboratory | Lab 3: continued. |
| | Tutorial | Tute 5: sampling and comparators. |
| | Assessment | Lab 2 report due. |
| | Project | Design task. |
| Week 6 : 14 October - 20 October | Project | Flexibility Week.  Design task. |
| Week 7 : 21 October - 27 October | Lecture | Samplers, data converter metrics, D/A and A/D converter design. |
| | Reading | JB ch. 25, 28, 29. |
| | Laboratory | Lab 4: combinational logic. |
| | Tutorial | Tute 6: A/D converters. |
| | Assessment | Lab 3 report due. |
| | Project | Design task. |
| Week 8 : 28 October - 3 November | Lecture | CMOS inverters and logic. Buffers and sizing. |
| | Reading | JB ch. 11. |
| | Laboratory | Lab 4 continued. |
| | Tutorial | Tute 7: CMOS inverters. |
| | Assessment | Quiz 2. |
| | Project | Design task. |
| Week 9 : 4 November - 10 November | Lecture | Static CMOS logic design. Sequential CMOS logic. |
| | Reading | JB ch. 12, 13. |
| | Laboratory | Lab 5: sequential logic. |
| | Tutorial | Tute 8: CMOS logic. |
| | Assessment | Lab 4 report due. |
| | Project | Design task. |
| Week 10 : 11 November - 17 November | Lecture | Dynamic CMOS logic. Memory design and topologies. |
| | Reading | JB ch. 14, 16. |
| | Laboratory | Lab 5 continued. |
| | Tutorial | Tute 9: sequential logic. |

| | Assessment | Design task report due. |
|---|---|---|
| Week 11 : 18 November - 24 November | Assessment | Lab 5 report due. |

# Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

# Course Resources

## Prescribed Resources

Textbook

- R. J. Baker, CMOS Circuit Design, Layout, and Simulation. Wiley Interscience, 3rd/4th ed., 2010/2019.

On-line resources

**Moodle**: As a part of the teaching component, Moodle will be used to upload lab reports and host forums. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

**Course webpage**: The course webpage is used to disseminate course material, including laboratory notes and design brief, past assessment and examination papers, and some lecture notes: https://subjects.ee.unsw.edu.au/elec4602.

CAD resources

Students will use the PCs in the Signal Processing Laboratory G17-108 for all in-class laboratory work. The CAD tools used in this course is the industry standard Cadence design suite which run under the Linux system Virtual Machine on the lab PCs. For specific details on how to log on, see the course web page. Students can access the CAD tools on the PCs in the school located in rooms G17-202 and G17-217 as well as the open space area G17-209.

Remote computer access

Computers in rooms G17-202 and G17-217 can be accessed remotely via https://myaccessunsw.cloud.com/Citrix/StoreWeb/#/desktops/all. Click on DESKTOPS and subsequenty ELECENG-LABPC-G17-Rm202 or ELECENG-LABPC-G17-Rm217 to start a Citrix remote session on a  computer in one of those rooms. Students must have the Citrix Workspace

player (download from [https://www.citrix.com/en-au/downloads/workspace-app/](https://www.citrix.com/en-au/downloads/workspace-app/)) installed on their own computer.

# Recommended Resources

**Reference books**

- T. C. Carusone, D. A. Johns and K. W. Martin, Analog Integrated Circuit Design. Wiley and Sons Inc., 2nd ed., 2012.
- T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press, 1998.
- N. Weste and D. Harris, CMOS VLSI Design: a Circuits and Systems Perspective. Addison-Wesley, 3rd ed., 2005

# Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course, and in our efforts to provide a rich and meaningful learning experience, we have changed the weighting of in-term assessments, introduced formal tutorial classes, and released summary slides.

# Staff Details

| Position | Name | Email | Location | Phone | Availability | Equitable Learning Services Contact | Primary Contact |
|----------|------|-------|----------|-------|--------------|-------------------------------------|-----------------|
| Convenor | Torsten Lehmann | | G17-343 | 93855374 | Wednesdays 4-5pm | Yes | Yes |

# Other Useful Information

Academic Information

### I. Special consideration and supplementary assessment

If you have experienced an illness or misadventure beyond your control that will interfere with your assessment performance, you are eligible to apply for Special Consideration prior to, or within 3 working days of, submitting an assessment or sitting an exam.

Please note that UNSW has a Fit to Sit rule, which means that if you sit an exam, you are declaring yourself fit enough to do so and cannot later apply for Special Consideration.

For details of applying for Special Consideration and conditions for the award of supplementary assessment, please see the information on UNSW's Special Consideration page.

## II. Administrative matters and links

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Attendance
- UNSW Email Address
- Special Consideration
- Exams
- Approved Calculators
- Academic Honesty and Plagiarism
- Equitable Learning Services

## III. Equity and diversity

Those students who have a disability that requires some adjustment in their teaching or learning environment are encouraged to discuss their study needs with the course convener prior to, or at the commencement of, their course, or with the Equity Officer (Disability) in the Equitable Learning Services. Issues to be discussed may include access to materials, signers or note-takers, the provision of services and additional exam and assessment arrangements. Early notification is essential to enable any necessary adjustments to be made.

## IV. Professional Outcomes and Program Design

Students are able to review the relevant professional outcomes and program designs for their streams by going to the following link: https://www.unsw.edu.au/engineering/student-life/student-resources/program-design.

*Note: This course outline sets out the description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle or your primary learning management system (LMS) should be consulted for the up-to-date class descriptions.  If there is any inconsistency in the description of activities between the University timetable and the Course Outline/Moodle/LMS, the description in the Course Outline/Moodle/LMS applies.*

## Academic Honesty and Plagarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. *Plagiarism at UNSW is defined as using the words or ideas of others and passing them off as your own.*

Plagiarism is a type of intellectual theft. It can take many forms, from deliberate cheating to accidentally copying from a source without acknowledgement. UNSW has produced a website with a wealth of resources to support students to understand and avoid plagiarism, visit: student.unsw.edu.au/plagiarism. The Learning Centre assists students with understanding academic integrity and how not to plagiarise. They also hold workshops and can help students one-on-one.

You are also reminded that careful time management is an important part of study and one of the identified causes of plagiarism is poor time management. Students should allow sufficient time for research, drafting and the proper referencing of sources in preparing all assessment tasks.

Repeated plagiarism (even in first year), plagiarism after first year, or serious instances, may also be investigated under the Student Misconduct Procedures. The penalties under the procedures can include a reduction in marks, failing a course or for the most serious matters (like plagiarism in an honours thesis or contract cheating) even suspension from the university. The Student Misconduct Procedures are available here:

www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf

## Submission of Assessment Tasks

Work submitted late without an approved extension by the course coordinator or delegated authority is subject to a late penalty of five percent (5%) of the maximum mark possible for that assessment item, per calendar day.

The late penalty is applied per calendar day (including weekends and public holidays) that the assessment is overdue. There is no pro-rata of the late penalty for submissions made part way through a day. This is for all assessments where a penalty applies.

Work submitted after five days (120 hours) will not be accepted and a mark of zero will be

awarded for that assessment item.

For some assessment items, a late penalty may not be appropriate. These will be clearly indicated in the course outline, and such assessments will receive a mark of zero if not completed by the specified date. Examples include:

- Weekly online tests or laboratory work worth a small proportion of the subject mark;
- Exams, peer feedback and team evaluation surveys;
- Online quizzes where answers are released to students on completion;
- Professional assessment tasks, where the intention is to create an authentic assessment that has an absolute submission date; and,
- Pass/Fail assessment tasks.

## Faculty-specific Information

Engineering Student Support Services – The Nucleus - enrolment, progression checks, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries e.g. admissions, fees, programs, credit transfer

**Phone**

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

## School-specific Information

**General Conduct and Behaviour**

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and

students may be asked to leave the class.

### Use of AI for assessments

Your work must be your own. If you use AI in the writing of your assessment, you must acknowledge this and your submission must be substantially your own work. More information can be found on this website.

### Workplace Health & Safety (WHS)

WHS for students and staff is of utmost priority. Most courses involve laboratory work. You must follow the rules about conduct in the laboratory. About COVID-19, advice can be found on this website.

## School Contact Information

**Consultations:** Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

**Keeping Informed:** Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

### Student Support Enquiries

For enrolment and progression enquiries please contact Student Services

### Web

Electrical Engineering Homepage