UNSW Course Outline

ZEIT3223 Embedded Systems - 2024

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General Course Information

Course Code : ZEIT3223
Year : 2024
Term : Semester 2
Teaching Period : Z2
Is a multi-term course? : No
Faculty : UNSW Canberra
Academic Unit : School of Engineering and Technology
Delivery Mode : In Person
Delivery Format : Standard
Delivery Location : UNSW Canberra at ADFA
Campus : UNSW Canberra
Study Level : Undergraduate
Units of Credit : 6

Useful Links

Handbook Class Timetable

Course Details & Outcomes

Course Description

The focus of this course will be on developing the theory and practice of modern embedded systems technology, with a focus on the platforms of FPGAs (field-programmable gate arrays) and single-board computers. This course will build on the prerequisite course Digital Electronics

and Microcontrollers, in which the analysis and design of digital systems composed of discrete digital components and microcontrollers has been developed. This course will cover digital logic families, hardware description languages for combinational circuits, sequential circuits, and finite state machines; programming, including assembly, machine language and C; architectures (including ARM and x86), micro architecture; memory systems, including caches and virtual memory; input/output systems, and embedded Linux. The course will include a laboratory sequence focused on the development of digital solutions based on FPGA-based system-on-a-chip (SoC) boards.

Course Aims

A key part of the faculty's mission is to educate Australia's future technology decision makers. In order to remain relevant it is necessary to keep pace with modern technology. This course will provide the second course on modern digital systems technology in the core of the Electrical Engineering (Honours) program.

Relationship to Other Courses

Prerequisite: ZEIT2208 and ZEIT2209

This course extends concepts covered in ZEIT2208 "Digital Electronics and Microcontrollers".

Course Learning Outcomes

Course Learning Outcomes	Engineers Australia - Professional Engineer (Stage 1)
CLO1 : Design digital systems in a hardware description language and implement in programmable logic.	• PEE2.1 : Application of established engineering methods to complex engineering problem solving • PEE2.2 : Fluent application of engineering techniques, tools and resources • PEE2.3 : Application of systematic engineering synthesis and design processes
CLO2 : Summarize, evaluate, and compare features of modern computer architectures, including processing and storage.	• PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering discipline • PEE1.5 : Knowledge of engineering design practice and contextual factors impacting the engineering discipline • PEE3.4 : Professional use and management of information
CLO3 : Implement computer interfaces to the physical world via inputs and outputs, and communicate with other digital systems.	• PEE1.2 : Conceptual understanding of the mathematics, numerical analysis, statistics, and computer and information sciences which underpin the engineering discipline • PEE1.5 : Knowledge of engineering design practice and contextual factors impacting the engineering discipline • PEE2.1 : Application of established engineering methods to complex engineering problem solving • PEE2.3 : Application of systematic engineering synthesis and design processes • PEE2.4 : Application of systematic approaches to the conduct and management of projects within the technology domain
CLO4 : Analyse and deploy digital systems based around embedded operating systems.	• PEE1.3 : In-depth understanding of specialist bodies of knowledge within the engineering discipline • PEE1.5 : Knowledge of engineering design practice and contextual factors impacting the engineering discipline • PEE1.6 : Understanding of the scope, principles, norms, accountabilities and bounds of sustainable engineering practice in the specific discipline

Course Learning Outcomes	Assessment Item
CLO1 : Design digital systems in a hardware description language and implement in programmable logic.	• Laboratory • Class Tests • Final Exam
CLO2 : Summarize, evaluate, and compare features of modern computer architectures, including processing and storage.	• Class Tests • Final Exam
CLO3 : Implement computer interfaces to the physical world via inputs and outputs, and communicate with other digital systems.	• Laboratory • Class Tests • Final Exam
CLO4 : Analyse and deploy digital systems based around embedded operating systems.	• Laboratory • Final Exam

Learning and Teaching Technologies

Moodle - Learning Management System

Learning and Teaching in this course

This course presents concepts through lectures. Tutorial and laboratory exercises are used to reinforce the content presented during the lectures. A large part of the learning is done through the laboratory exercises.

The Learning Management System

Moodle is the Learning Management System used at UNSW Canberra. All courses have a Moodle site which will become available to students at least one week before the start of semester. Please find all help and documentation (including Blackboard Collaborate) at the Moodle Support page.

UNSW Moodle supports the following web browsers:

» Google Chrome 50+
» Safari 10+
** Internet Explorer is not recommended

** Addons and Toolbars can affect any browser's performance.

Operating systems recommended are:

Windows 7, 10, Mac OSX Sierra, iPad IOS10

For further details about system requirements click here.

Log in to Moodle here.

If you need further assistance with Moodle:

For enrolment and login issues please contact:
IT Service Centre
Email: itservicecentre@unsw.edu.au
Phone: (02) 9385-1333
International: +61 2 9385 1333

For all other Moodle issues please contact:
External TELT Support
Email: externalteltsupport@unsw.edu.au
Phone: (02) 9385-3331
International: +61 2 938 53331

Opening hours:
Monday – Friday 7:30am – 9:30 pm
Saturday & Sunday 8:30 am – 4:30pm

Additional Course Information

Academic Integrity and Plagiarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW staff and students have a responsibility to adhere to this principle of academic integrity. All students are expected to adhere to UNSW's Student Code of Conduct https://www.gs.unsw.edu.au/policy/documents/studentcodepolicy.pdf

Plagiarism undermines academic integrity and is not tolerated at UNSW. *It is defined as using the words or ideas of others and passing them off as your own, and* can take many forms, from deliberate cheating to accidental copying from a source without acknowledgement.

For more information, please refer to the following:

https://student.unsw.edu.au/plagiarism

Referencing

In this course, students are required to reference following the APA 7 / Chicago NB referencing style. Information about referencing styles is available at: https://guides.lib.unsw.adfa.edu.au/c.php?g=472948&p=3246720

Study at UNSW Canberra

https://www.unsw.adfa.edu.au/study

Study at UNSW Canberra has lots of useful information regarding:

- Where to get help
- Administrative matters
- Getting your passwords set up
- How to log on to Moodle
- Accessing the Library and other areas.

Additional Information as required

CRICOS Provider no. 00098G

The University of New South Wales Canberra.

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates
Laboratory Assessment Format: Individual	36%	Start Date: Not Applicable Due Date: Week 5: 12 August - 16 August, Week 10: 30 September - 04 October, Week 12: 14 October - 18 October
Class Tests Assessment Format: Individual	24%	Start Date: Not Applicable Due Date: Week 3: 29 July - 02 August, Week 6: 19 August - 23 August, Week 9: 23 September - 27 September
Final Exam Assessment Format: Individual	40%	Start Date: Not Applicable Due Date: Not Applicable

Assessment Details

Laboratory

Assessment Overview

Three laboratory assessments; worth 12% each.

Course Learning Outcomes

- CLO1 : Design digital systems in a hardware description language and implement in programmable logic.
- CLO3 : Implement computer interfaces to the physical world via inputs and outputs, and communicate with other digital systems.
- CLO4 : Analyse and deploy digital systems based around embedded operating systems.

Detailed Assessment Description

This course will contain three laboratory assessments. Each of these laboratory exercises run over the course of multiple weeks, and will be conducted during the 3 hour lab sessions scheduled during the semester. The assessments are individual, and you will be graded on your understanding of the concepts and the quality of the source code, design and presentation.

- Laboratory 1 (12%) will cover hardware description languages and FPGAs. Due on Wednesday week 5, and will consists of a short in-lab demonstration with a submission
- Laboratory 2 (12%) will cover programmable logic and microprocessor subsystems, logic design and C programming. Due on Wednesday week 10, and will consists of a short in-lab demonstration with a submission
- Laboratory 3 (12%) will cover embedded operating systems. Due in week 12, and will consits of a lab report and source code.

Each laboratory assessment has marks reserved for interesting and successfully implemented extensions.

Mapping to course learning outcomes: LO1, LO2, LO3 and LO4.

Assignment submission Turnitin type

This assignment is submitted through Turnitin and students can see Turnitin similarity reports.

Class Tests

Assessment Overview

Three class tests; worth 8% each

Course Learning Outcomes

- CLO1 : Design digital systems in a hardware description language and implement in programmable logic.
- CLO2 : Summarize, evaluate, and compare features of modern computer architectures, including processing and storage.
- CLO3 : Implement computer interfaces to the physical world via inputs and outputs, and communicate with other digital systems.

Detailed Assessment Description

The contents covered in Units 1, 2 and 3 will be assesed by a class test after each unit. The class tests are individual and will be held either during a lecture slot or a tutorial slot.

- Class test 1: Week 3 and will cover the content covered in Unit 1
- Class test 2: Week 6 and will cover the content covered in Unit 2
- Class test 3: Week 9 and will covere the content covered in Unit 3

Mapping to course learning outcomes: LO1, LO2 and LO3.

Assessment Length

45 min

Assignment submission Turnitin type

This is not a Turnitin assignment

Final Exam

Assessment Overview

n/a

Course Learning Outcomes

- CLO1 : Design digital systems in a hardware description language and implement in programmable logic.
- CLO2 : Summarize, evaluate, and compare features of modern computer architectures, including processing and storage.
- CLO3 : Implement computer interfaces to the physical world via inputs and outputs, and communicate with other digital systems.
- CLO4 : Analyse and deploy digital systems based around embedded operating systems.

Detailed Assessment Description

The exam covers all contents presented in this course during lectures, tutorials and laboratory exercises.

Mapping to course learning outcomes: LO1, LO2, LO3 and LO4.

Assessment Length

2 hr

Assignment submission Turnitin type

Not Applicable

General Assessment Information

Class test 1 will be held during week 3. Grades and feedback will be provided during week 4.

Late Submission of Assessment

Unless prior arrangement is made with the lecturer or a formal application for special consideration is submitted, a penalty of 5% of the total available mark for the assessment will apply for each day that an assessment item is late up to a maximum of 5 days (120 hours) after which an assessment can no longer be submitted and a grade of 0 will be applied.

Use of Generative AI in Assessments

You can use generative AI software in this assessment to the extent specified in the assessment instructions. Any output of generative software within your assessment must be attributed with full referencing.

If the outputs of generative AI such as ChatGPT form part of your submission and is not appropriately attributed, it will be regarded as serious academic misconduct and subject to the standard penalties, which may include 00FL, suspension and exclusion.

* To cite: OpenAI (Year Accessed). ChatGPT. OpenAI. https://openai.com/models/chatgpt/

* Please note that the outputs from these tools are not always accurate, appropriate, nor properly referenced. You should ensure that you have moderated and critically evaluated the outputs from generative AI tools such as ChatGPT before submission.

Grading Basis

Standard

Requirements to pass course

The overal passing mark is set to 50%

Course Schedule

Teaching Week/Module	Activity Type	Content
Week 1 : 15 July - 19 July	Lecture	• U1L1: Intro to FPGA and logic in VHDL • U2L2: Logic in VHDL
	Laboratory	Getting started with development using the Pynq-Z2 dev board and combinatorial logic
	Tutorial	Covering concepts from U1L1 and U1L2
Week 2 : 22 July - 26 July	Lecture	• U1L3: Scopes and structures in VHDL • U1L4: Finite state machines
	Laboratory	Working on lab assesment 1
	Tutorial	Content from U1L3 and U1L4
Week 3 : 29 July - 2 August	Lecture	• U1L5: Parametric VHDL design and signalling • Class test 1
	Laboratory	Working on lab assessment 1
	Tutorial	Run through class test 1
Week 4 : 5 August - 9 August	Lecture	• U2L1: Computer architectures • U2L2: Register and bit manipulation
	Laboratory	Working on lab assessment 1
	Tutorial	Content from U2L1 and U2L2
Week 5 : 12 August - 16 August	Lecture	• U2L3: Interfacing PS and PL • Friday timetable
	Laboratory	Wednesday: Lab demonstration.
	Tutorial	Content from U2L2 and U2L3
Week 6 : 19 August - 23 August	Lecture	• U2L4: Program counter and the stack • U2L5: Memory
	Laboratory	Introduction to the microprocessor IDE and PS and PL integration workflow
	Tutorial	Class test 2
Week 7 : 9 September - 13 September	Lecture	• U3L1: Multi-core architectures • U3L2: Parallel algorithm design
	Laboratory	Working on lab assessment 2
	Tutorial	Content from U3L1 and U3L2
Week 8 : 16 September - 20 September	Lecture	• U3L3: Scheduling and real-time computing • U3L4: Data path and memory
	Laboratory	Working on lab assessment 2
	Tutorial	Content from U3L3 and U3L4
Week 9 : 23 September - 27 September	Lecture	• U3L5: Integer math and memory • Class test 3
	Laboratory	Working on lab assessment 1
	Tutorial	Run through class test 3
Week 10 : 30 September - 4 October	Lecture	• U4L1: Operating systems • U4L2: Tasking and threading
	Laboratory	Lab 2 demonstration
	Tutorial	Run through class test 1
Week 11 : 7 October - 11 October	Lecture	• Monday: Public holiday • U4L3: Real time programming on operating systems
	Laboratory	Working on lab assessment 3
	Tutorial	Military training day
Week 12 : 14 October - 18 October	Lecture	• U4L4: Interfacing hardare and device drivers • U4L5: Further concepts on embedded systems
	Laboratory	Working on lab assessment 3
	Tutorial	Content from U4L3 and revisiting topics

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

General Schedule Information

This schedule is tentative and minor changes might occur during the teaching period.

Course Resources

Prescribed Resources

Title: Digital systems: principles and applications

12th edition, Global edition.

Author: Tocci, Ronald,

ISBN: 1292162007; 9781292162003

Recommended Resources

Title: The VHDL Handbook

Author: David R. Coelho

Published: 22nd January 2012

ISBN: 9781461289029

Title: Structured Computer Organization

Author: Andrew Tanenbaum and Todd Austin

Edition: 6

Publisher: Pearson

Published: 15 October 2012

ISBN: 978-0132916523

Title: Modern Operating Systems 4th edition

Author: Andrew Tanenbaum, Herbert Bos

Publisher: Pearson

Published 18 September 2014

ISBN: 978-0133591620

Course Evaluation and Development

One of the key priorities in the 2025 Strategy for UNSW is a drive for academic excellence in education. One of the ways of determining how well UNSW is progressing towards this goal is by listening to our own students. Students will be asked to complete the myExperience survey towards the end of this course.

Students can also provide feedback during the semester via: direct contact with the lecturer, the "On-going Student Feedback" link in Moodle, Student-Staff Liaison Committee meetings in schools, informal feedback conducted by staff, and focus groups. Student opinions really do make a difference. Refer to the Moodle site for this course to see how the feedback from previous students has contributed to the course development.

Important note: Students are reminded that any feedback provided should be constructive and professional and that they are bound by the Student Code of Conduct Policy

https://www.gs.unsw.edu.au/policy/documents/studentcodepolicy.pdf

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Convenor	Edwin Peters		B16R217		Send an email or pop by my office	No	Yes