UNSW Course Outline

ELEC3106 Electronics - 2024

Published on the 08 Feb 2024

General Course Information

Course Code : ELEC3106
Year : 2024
Term : Term 1
Teaching Period : T1
Is a multi-term course? : No
Faculty : Faculty of Engineering
Academic Unit : School of Electrical Engineering & Telecommunications
Delivery Mode : In Person
Delivery Format : Standard
Delivery Location : Kensington
Campus : Sydney
Study Level : Undergraduate
Units of Credit : 6

Useful Links

Handbook Class Timetable

Course Details & Outcomes

Course Description

Physical electronic circuits and systems are plagued by a number of undesired effects that the designer need be aware of in order to implement operational electronics. Electrical noise and non-linearity, for instance, limit signal dynamic range; dynamic power supply currents can lead to corruption of digital data; electromagnetic interference (EMI) can cause system malfunction;

parasitic components limit the operating frequencies of all circuits. Modern electronic systems, such as laptops and mobile phones, are actually extraordinarily difficult to implement. The Electronics course introduces you to a number of important undesired effects of electronic systems and ways to deal with these; also, it introduces some more advanced circuit functions.

Course content includes: Non-ideal effects in electronic circuits and systems: noise; device noise, external noise, CMRR, PSRR, mixed A/D. Distortion; non-linearity, dynamic range, saturation. Stability and performance sensitivity to parameter variations. Some simple design for stability and performance. Design optimisation. Power-supply distribution and decoupling. Mixed analogue/digital system design, including grounding, shielding and interfacing. Circuit modelling with SPICE. Data sheet interpretation. Design of analogue and digital circuits and system components: non-linear circuits; oscillators, PLLs, multipliers, AGCs, Schmitt triggers. Introduction to filter design; active filters; op-amp. Sensors and actuators, PTAT; instrumentation amplifiers and signal conditioning. Gate delay, power dissipation, noise margins, fan-out. Thermal consideration, power supplies and power sources, reliability, uC watchdogs. ESD. Transmission lines.

Course Aims

The course builds on the knowledge gained in the first two years of studying electrical engineering and provides the students with practical electronic circuit design skills.

The course aims to make the student familiar with critical non-ideal effects in electronic devices and systems, thus enabling the student to design and construct physical electronic circuits that operate as desired.

Relationship to Other Courses

This is a 3rd year course in the School of Electrical Engineering and Telecommunications. It is a core course for students following a BE (Electrical) or (Telecommunications) or (Quantum) program and other combined degree programs, and an elective for Computer Engineering students.

Pre-requisites and Assumed Knowledge

The pre-requisites for this course are ELEC2133, Analogue Electronics, and ELEC2141, Digital Circuit Design. ELEC2133 may be taken as a co-requisite. It is also required that you have good working knowledge of circuit theory and some basic signal analysis as covered in the courses ELEC1111, Electrical Circuit Fundamentals, and ELEC2134 Circuits and Signals. It is finally

assumed that you are proficient in the use of personal computers, and are able to operate electronics laboratory equipment independently.

Following Courses

The course is a pre-requisite for the fourth-year professional elective courses in the electronics area: ELEC4601, Digital and Embedded Systems Design, ELEC4602, Microelectronics Design and Technology, and ELEC4604, RF Electronics. These courses are again pre-requisites for post-graduate level courses in electronics.

Course Learning Outcomes

Course Learning Outcomes
CLO1 : Identify critical non-ideal effects in analogue and digital electronic circuits
CLO2 : Design electronics that work in practice including design for EMC
CLO3 : Design simple power supplies and circuits
CLO4 : Interface analogue circuits and digital circuits
CLO5 : Design reliable systems, including failure protection in firmware and hardware
CLO6 : Integrate and utilise previously acquired engineering skills to the design and analysis of electronics

Course Learning Outcomes	Assessment Item
CLO1 : Identify critical non-ideal effects in analogue and digital electronic circuits	• Laboratory Work and Reporting • Quizzes • Final Examination
CLO2 : Design electronics that work in practice including design for EMC	• Project design task and report • Quizzes • Final Examination
CLO3 : Design simple power supplies and circuits	• Project design task and report • Quizzes • Final Examination
CLO4 : Interface analogue circuits and digital circuits	• Laboratory Work and Reporting • Project design task and report • Final Examination
CLO5 : Design reliable systems, including failure protection in firmware and hardware	• Quizzes • Final Examination
CLO6 : Integrate and utilise previously acquired engineering skills to the design and analysis of electronics	• Laboratory Work and Reporting • Project design task and report • Final Examination

Learning and Teaching Technologies

Moodle - Learning Management System | Microsoft Teams | Course website

Learning and Teaching in this course

Delivery mode

- Formal face-to-face lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations and individually targeted illustrations to aid your understanding.
- Tutorials, which allow for exercises in problem solving and allow time for you to resolve in-depth problems for quantitative understanding of the lecture material and applying your engineering skills in electronics context.
- Laboratory sessions, which experimentally support the formal lecture material and also provide you with practical design, construction, measurement and debugging skills.
- Design labs, which support creativity set in the course context solving an open-ended design problem with experimental verification.

Learning in this course

You are expected to attend all lectures, tutorials, labs, and quizzes in order to maximise learning. You must prepare well for your laboratory classes and your lab work will be assessed. You should read relevant sections of the recommended texts. For most topics, lecture notes will not be given: reading and reflecting on the recommended texts and identify critical parts with the aid of the lectures is an essential component of this course. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW assumes that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Lectures

During the lectures technology capabilities and design issues are discussed and theoretical aspects of electronics design and technology are presented. Numerous examples of analogue and digital electronic circuit functions are discussed in order to convey a qualitative understanding of circuit operations, non-idealities, and EMI. You are encouraged to actively engage in the lectures to facilitate two-way communication and enhance learning. The lectures aim to support you in identifying and analysing non-ideal effects in circuits, to aid in learning how to mitigate such effects, and finally to help you appreciate the capabilities and limitations of the technology.

Tutorial Classes

You should attempt all of your problem sheet questions in advance of attending the tutorial classes. The importance of adequate preparation prior to each tutorial cannot be overemphasised, as the effectiveness and usefulness of the tutorial depends to a large extent on this preparation. Group learning is encouraged. Answers for these questions will be discussed during the tutorial class and the tutor will cover the more complex questions in the tutorial class.

Laboratory Program

The laboratory work provides you with hands-on experience in measuring non-ideal effects and EMI in electronic circuits, and thus helps to re-enforce the central topics in the course. Most of the laboratory work being carried out on bread boards constructed by you, also exercises your ability to set up measurements and locating circuit errors. The laboratory work will be carried out in groups of two students.

Laboratory Design Task

The design laboratory exercise is a small design task which aims to draw together theoretical and practical design aspects in a small open-ended design problem. You will design a circuit meeting given specifications during ther term and debug and characterise the circuit during the design laboratory sessions. The design task provide and test engineering creativity, open-ended problem solving skills, communication skills and general understanding of the course content.

Other Professional Outcomes

Engineers Australia (EA), Professional Engineer Stage 1 Competencies

The Course Learning Outcomes (CLOs) contribute to your development of the following EA competencies:

PE1: Knowledge and Skill Base:
PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals: CLO 1, 2, 3, 4, 5
PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing: CLO 5
PE1.3 In-depth understanding of specialist bodies of knowledge: CLO 1, 2, 3, 4, 5, 6
PE1.4 Discernment of knowledge development and research directions: n/a
PE1.5 Knowledge of engineering design practice: CLO 2, 3, 4, 5, 6
PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering

practice: n/a

PE2: Engineering Application Ability:
PE2.1 Application of established engineering methods to complex problem solving: CLO 6
PE2.2 Fluent application of engineering techniques, tools and resources: CLO 2, 4, 6
PE2.3 Application of systematic engineering synthesis and design processes: n/a
PE2.4 Application of systematic approaches to the conduct and management of engineering projects: n/a

PE3: Professional and Personal Attributes:
PE3.1 Ethical conduct and professional accountability: n/a
PE3.2 Effective oral and written communication (professional and lay domains): CLO 2, 4, 6
PE3.3 Creative, innovative and pro-active demeanour: CLO 6
PE3.4 Professional use and management of information: CLO 6
PE3.5 Orderly management of self, and professional conduct: CLO 6
PE3.6 Effective team membership and team leadership: n/a

Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems, through laboratory experiments and tutorial exercises.
- Developing capable independent and collaborative enquiry, through tutorials exercises.
- Developing digital and information literacy and lifelong learning skills, through lectures, class preparations and report writing.
- Developing the capability of effective communication, through report writing.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through the design task.

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates
Laboratory Work and Reporting Assessment Format: Group	15%	
Quizzes Assessment Format: Individual	10%	
Project design task and report Assessment Format: Group	15%	
Final Examination Assessment Format: Individual	60%	

Assessment Details

Laboratory Work and Reporting

Assessment Overview

For each of the four laboratory exercises, the student's work will be assessed in class and on a short report. A rubric will be used for marking and feedback given to each group online.

Course Learning Outcomes

- CLO1 : Identify critical non-ideal effects in analogue and digital electronic circuits
- CLO4 : Interface analogue circuits and digital circuits
- CLO6 : Integrate and utilise previously acquired engineering skills to the design and analysis of electronics

Detailed Assessment Description

While laboratory work is primarily about learning, it is assessed to ensure that you understand the material in this essential course component. This assessment test that you can use the lab equipment, understand circuit models and non-idealities, carry out measurements, and can

design simple circuits.

You are required to maintain a lab book for recording your observations and you must bring a camera or USB stick to capture CRO images of your observations for documentation. After completing each lab component, your work will be assessed by the laboratory demonstrator, so make sure that your demonstrator notice your work. Laboratory work must be documented in brief reports which are due Monday the week after the laboratory session ending each exercise. Each report must be uploaded as a .pdf file (no other format accepted) on the course Moodle site.

Submission notes

See Moodle for laboratory submission dates.

Quizzes

Assessment Overview

Two in-class quizzes will be held during lecture time. Marks will be assigned according to the correct fraction of the response. Verbal class-wide feedback will be given during lectures.

Course Learning Outcomes

- CLO1 : Identify critical non-ideal effects in analogue and digital electronic circuits
- CLO2 : Design electronics that work in practice including design for EMC
- CLO3 : Design simple power supplies and circuits
- CLO5 : Design reliable systems, including failure protection in firmware and hardware

Detailed Assessment Description

The two quizzes will be held during the lecture time in the term. These are designed to give early feed-back on your progress through the theoretical components of the course and test your general understanding of the course material. Questions will be drawn from course material covered in the four weeks prior to each quiz.

Submission notes

See Moodle for quiz dates and times.

Project design task and report

Assessment Overview

The design task will be carried out in open labs and in the scheduled laboratories. The work will be assessed on a demonstration in the last lab class an on a submitted report. A rubric will be used for marking and feedback given to each group online.

Course Learning Outcomes

- CLO2 : Design electronics that work in practice including design for EMC
- CLO3 : Design simple power supplies and circuits
- CLO4 : Interface analogue circuits and digital circuits
- CLO6 : Integrate and utilise previously acquired engineering skills to the design and analysis of electronics

Detailed Assessment Description

The design task is assessed to test your ability to design a simple electronic circuit, thus also demonstrating the your appreciation of the technology, and ability to use appropriate components and conduct suitable analysis to aid the design.

As for the other laboratory work, you are required to maintain a lab book and bring a camera or USB stick for recording your observations. Again, your work will be assessed by the laboratory demonstrator, so make sure that your demonstrator notice your work. The design and experimentation work must be documented in a brief report which is due Monday the due week listed in the laboratory schedule. Each report must be uploaded as a .pdf file (no other format accepted) on the course Moodle site.

Submission notes

See Moodle for design report submission date.

Final Examination

Assessment Overview

The examination is a 2-hour open-book examination. Marks will be assigned according to the correct fraction of the response.

Course Learning Outcomes

- CLO1 : Identify critical non-ideal effects in analogue and digital electronic circuits
- CLO2 : Design electronics that work in practice including design for EMC
- CLO3 : Design simple power supplies and circuits
- CLO4 : Interface analogue circuits and digital circuits
- CLO5 : Design reliable systems, including failure protection in firmware and hardware
- CLO6 : Integrate and utilise previously acquired engineering skills to the design and analysis of electronics

Detailed Assessment Description

The exam in this course is a standard open-book 2-hour (nominal) written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may

be drawn from any aspect of the course (including tutorials, laboratories and design task), unless specifically indicated otherwise by the lecturer.

Hurdle rules

An examination mark of at least 45% is required to pass the course.

General Assessment Information

Grading Basis

Standard

Course Schedule

Teaching Week/Module	Activity Type	Content
Week 1 : 12 February - 18 February	Lecture	Op-amp voltage/current limitations, offsets, biasing. CMRR, PSRR, parameter variation. Slew-rate, bandwidth, compensation. Distortion, saturation.
	Reading	PW ch. 5, notes, datasheets.
	Laboratory	Lab 1: op-amp measurements.
	Tutorial	Tute 1: op-amps.
Week 2 : 19 February - 25 February	Lecture	Electrical noise. Dynamic range. Digital fan-out, noise margins.Logic families, VTC, I/O characteristics.
	Reading	SS Ch. 15, PW ch. 6, notes, datasheets.
	Laboratory	Lab 1 cont.
	Tutorial	Tute: Ex-2016-Q1.
Week 3 : 26 February - 3 March	Lecture	Gate delays, timing. Logic families. Interfacing to logic, opto-coupling. Level-shifting, ESD. Driving transmission lines, human interfaces.
	Reading	SS ch. 15, PW ch. 6+9, videos, datasheets.
	Laboratory	Lab 2: logic gate measurements.
	Tutorial	Tute 2: logic.
	Assessment	Lab 1 report due.
Week 4 : 4 March - 10 March	Lecture	Grounding, decoupling. Noise coupling, shielding. EMC, mixed A/D.
	Reading	PW ch. 1+8.
	Laboratory	Lab 2 cont.
	Tutorial	Tute: Ex-2016-Q2.
	Assessment	Quiz 1.
Week 5 : 11 March - 17 March	Lecture	Power supplies, linear regulators, rectification. Switch-mode supplies, start-up. Batteries, solar cells. Thermal modelling.
	Reading	PW ch. 7, ch. 9.
	Laboratory	Lab 3: PCB EMI measurements.
	Tutorial	Tute 3: power supplies.
	Assessment	Lab 2 report due.
Week 6 : 18 March - 24 March	Workshop	Surface-mount soldering practice or PCB layout.
	Laboratory	Design task.
Week 7 : 25 March - 31 March	Lecture	SPICE simulations, models, functions. Simulation types and limitations. Power stages (A, B, AB, D). Protection, biasing.
	Reading	Notes, SS ch. 11.
	Laboratory	Lab 4: EMI simulations with SPICE.
	Tutorial	Tute: Ex-2016-Q3.
	Assessment	Lab 3 report due.
Week 8 : 1 April - 7 April	Lecture	Filtering. Passive and active filters. Filter design, sensitivity.
	Reading	SS ch. 13.
	Laboratory	Design task.
	Tutorial	Tute 4: power amps.
	Assessment	Quiz 2.
Week 9 : 8 April - 14 April	Lecture	Oscillators. Multipliers, Schmitt triggers, PLL. AGC, sensors, interfaces.
	Reading	SS ch. 2+14.
	Laboratory	Design task.
	Tutorial	Tute 5: filters & non-lin.
	Assessment	Lab 4 report due.
Week 10 : 15 April - 21 April	Lecture	Electronic failure mechanisms. Reliability. FMEA, watchdogs, defensive programming.
	Reading	PW ch. 6+9, notes.
	Laboratory	Design demonstration.
	Tutorial	Tute Ex-2016-Q4.

Week 11 : 22 April - 28 April	Assessment	Design task report due.

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

Course Resources

Prescribed Resources

Textbooks

- A. S. Sedra & K. C. Smith, Microelectronic Circuits. Oxford University Press, 7th ed., 2016.
- P. Wilson, The Circuit Designer's Companion. Elsevier, 4th ed. 2017.

Note, if you use the 6th edition of SS, subtract 1 from the chapter references in the lecture schedule (except for chapter 2).

On-line resources

Moodle: As a part of the teaching component, Moodle will be used to upload lab reports and host forums. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

Course webpage: The course webpage is used to disseminate course material, including laboratory notes and design brief, past assessment and examination papers, and some lecture notes: https://subjects.ee.unsw.edu.au/elec3106.

Teams: MS Teams (accessed using your University zpass credentials) will be used for on-line real-time communications: https://teams.microsoft.com/.

Recommended Resources

Reference books

- P. Horowitz & W. Hill, The Art of Electronics. Cambridge University Press, 3rd ed., 2015.
- E. Bogatin, Signal and Power Integrity — Simplified. Pearson, 2nd ed., 2009.

Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via

the myExperience process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course, and in our efforts to provide a rich and meaningful learning experience, we have changed the weighting of in-semester assessments, increased the number of tutorial exercises, commenced use of the LTSpice simulator program, provided supplementary lecture notes on selected topics, released lecture summary slides, and provided lecture video recordings.

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Convenor	Torsten Lehmann		G17-343	93855374	Tuesdays 3-4pm, Fridays 11am-12pm.	No	Yes
Demonstrator	Julian Keledjian					No	No

Other Useful Information

Academic Information

I. Special consideration and supplementary assessment

If you have experienced an illness or misadventure beyond your control that will interfere with your assessment performance, you are eligible to apply for Special Consideration prior to, or within 3 working days of, submitting an assessment or sitting an exam.

Please note that UNSW has a Fit to Sit rule, which means that if you sit an exam, you are declaring yourself fit enough to do so and cannot later apply for Special Consideration.

For details of applying for Special Consideration and conditions for the award of supplementary assessment, please see the information on UNSW's Special Consideration page.

II. Administrative matters and links

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Attendance
- UNSW Email Address
- Special Consideration
- Exams

- Approved Calculators
- Academic Honesty and Plagiarism
- Equitable Learning Services

III. Equity and diversity

Those students who have a disability that requires some adjustment in their teaching or learning environment are encouraged to discuss their study needs with the course convener prior to, or at the commencement of, their course, or with the Equity Officer (Disability) in the Equitable Learning Services. Issues to be discussed may include access to materials, signers or note-takers, the provision of services and additional exam and assessment arrangements. Early notification is essential to enable any necessary adjustments to be made.

IV. Professional Outcomes and Program Design

Students are able to review the relevant professional outcomes and program designs for their streams by going to the following link: https://www.unsw.edu.au/engineering/student-life/student-resources/program-design.

Note: This course outline sets out the description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle or your primary learning management system (LMS) should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline/Moodle/LMS, the description in the Course Outline/Moodle/LMS applies.

Academic Honesty and Plagarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. *Plagiarism at UNSW is defined as using the words or ideas of others and passing them off as your own.*

Plagiarism is a type of intellectual theft. It can take many forms, from deliberate cheating to accidentally copying from a source without acknowledgement. UNSW has produced a website with a wealth of resources to support students to understand and avoid plagiarism, visit: student.unsw.edu.au/plagiarism. The Learning Centre assists students with understanding academic integrity and how not to plagiarise. They also hold workshops and can help students one-on-one.

You are also reminded that careful time management is an important part of study and one of the identified causes of plagiarism is poor time management. Students should allow sufficient time for research, drafting and the proper referencing of sources in preparing all assessment tasks.

Repeated plagiarism (even in first year), plagiarism after first year, or serious instances, may also be investigated under the Student Misconduct Procedures. The penalties under the procedures can include a reduction in marks, failing a course or for the most serious matters (like plagiarism in an honours thesis or contract cheating) even suspension from the university. The Student Misconduct Procedures are available here:

www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf

Submission of Assessment Tasks

Work submitted late without an approved extension by the course coordinator or delegated authority is subject to a late penalty of five percent (5%) of the maximum mark possible for that assessment item, per calendar day.

The late penalty is applied per calendar day (including weekends and public holidays) that the assessment is overdue. There is no pro-rata of the late penalty for submissions made part way through a day. This is for all assessments where a penalty applies.

Work submitted after five days (120 hours) will not be accepted and a mark of zero will be awarded for that assessment item.

For some assessment items, a late penalty may not be appropriate. These will be clearly indicated in the course outline, and such assessments will receive a mark of zero if not completed by the specified date. Examples include:

- Weekly online tests or laboratory work worth a small proportion of the subject mark;
- Exams, peer feedback and team evaluation surveys;
- Online quizzes where answers are released to students on completion;
- Professional assessment tasks, where the intention is to create an authentic assessment that has an absolute submission date; and,
- Pass/Fail assessment tasks.

Faculty-specific Information

Engineering Student Support Services – The Nucleus - enrolment, progression checks, clash

requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries e.g. admissions, fees, programs, credit transfer

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

School-specific Information

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Use of AI for assessments

Your work must be your own. If you use AI in the writing of your assessment, you must acknowledge this and your submission must be substantially your own work. More information can be found on this website.

Workplace Health & Safety (WHS)

WHS for students and staff is of utmost priority. Most courses involve laboratory work. You must follow the rules about conduct in the laboratory. About COVID-19, advice can be found on this website.

School Contact Information

Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Student Support Enquiries

For enrolment and progression enquiries please contact Student Services

Web

Electrical Engineering Homepage