UNSW Course Outline

ELEC2141 Digital Circuit Design - 2024

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General Course Information

Course Code : ELEC2141
Year : 2024
Term : Term 1
Teaching Period : T1
Is a multi-term course? : No
Faculty : Faculty of Engineering
Academic Unit : School of Electrical Engineering & Telecommunications
Delivery Mode : In Person
Delivery Format : Standard
Delivery Location : Kensington
Campus : Sydney
Study Level : Undergraduate
Units of Credit : 6

Useful Links

Handbook Class Timetable

Course Details & Outcomes

Course Description

Digital systems store, move and process information. Digital systems consist of logic circuits and are a key component of computers and other products such as smartphones, digital watches, household appliances and electronic games. Digital systems are integral to different

areas in electrical engineering such as digital signal processing, telecommunications, speech analysis and recognition, power electronics and control systems. Knowledge of digital systems is thus a core capability for all electrical engineers.

This course will provide an introduction to modern digital logic design. It will cover the analysis and design of combinational and sequential logic circuits, computer design fundamentals as well as the digital switches used to build digital systems. The course will start by covering basic logic gates, Boolean algebra, two-level logic and then build to the analysis and design of combinational logic circuits, regular logic structures, multi-level networks, combination circuit building blocks and implementation of combinational circuits. It will also cover topics in sequential logic, which will include basic latches and flip-flops, timing methodologies, analysis and design of Finite state machines (FSMs), state minimization, state encoding, counters, registers and implementation of FSMs. Elements of computers will be introduced, specifically arithmetic circuits, arithmetic and logic units, register and bus structures, controllers/ sequencers, programmable logic devices and microprogramming. CMOS and TTL digital switch technologies, the building blocks of digital systems, will be also covered. The course will provide hands-on experience with computer-aided design tools for logic design, schematic entry, state diagram entry, hardware description language entry, compilation to logic networks, simulation and mapping to programmable logic devices.

Course Aims

Digital circuits are integral parts of many areas of engineering and technology such as personal computers, digital signal processing, telecommunications, speech analysis and recognition, and control systems. The objective of this course is to equip students with the necessary fundamental knowledge and skill that enable them to understand, analyze and design digital circuits in the real world. At the completion of the course, students should be in a position to be able to design and build reliable and cost effective digital circuits. The course aims to provide students with fundamental knowledge of digital systems with respect to several different levels of abstraction that they will need in their program – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.

Relationship to Other Courses

This is a 2nd year course in the School of Electrical Engineering & Telecommunications. It is a core course for students in a BE (Electrical) or (Telecommunications) or (Quantum) program.

Pre-requisites and Assumed Knowledge

The co-requisite for this course is ELEC1111: Electrical Circuit Fundamentals, which introduced basic concepts of electrical circuits. It is assumed that you have a good computer literacy.

Following Courses

The course is a pre-requisite for DESN2000: Engineering Design and Professional Practice, in which the digital system design concepts introduced in ELEC2141 will be applied extensively. It is also a pre-requisite for ELEC3106: Electronics in which low level analysis and implementation of various logic gates are undertaken.

Course Learning Outcomes

Course Learning Outcomes
CLO1 : Analyse and design combinational circuits
CLO2 : Implement combinational circuits using standard digital circuit elements such as multiplexers, decoders, etc
CLO3 : Design and optimize simple synchronous sequential circuits
CLO4 : Examine the fundamental components of the central processing unit (CPU) in a computer and their workings
CLO5 : Implement simple designs at various levels employing knowledge of practical aspects of digital circuits and systems and their use in more complex systems
CLO6 : Demonstrate understanding of the various hardware realizations of the basic digital circuit elements
CLO7 : Apply basic skills in computer-aided design tools, including a hardware description language (Verilog) in the analysis and design of digital circuits

Course Learning Outcomes	Assessment Item
CLO1 : Analyse and design combinational circuits	• Assignments • Mid-Term Assessment • Final Examination • Laboratory practical experiments
CLO2 : Implement combinational circuits using standard digital circuit elements such as multiplexers, decoders, etc	• Assignments • Mid-Term Assessment • Final Examination • Laboratory practical experiments
CLO3 : Design and optimize simple synchronous sequential circuits	• Assignments • Mid-Term Assessment • Final Examination • Laboratory practical experiments
CLO4 : Examine the fundamental components of the central processing unit (CPU) in a computer and their workings	• Mid-Term Assessment • Final Examination
CLO5 : Implement simple designs at various levels employing knowledge of practical aspects of digital circuits and systems and their use in more complex systems	• Assignments • Laboratory practical experiments
CLO6 : Demonstrate understanding of the various hardware realizations of the basic digital circuit elements	• Assignments • Mid-Term Assessment • Final Examination • Laboratory practical experiments
CLO7 : Apply basic skills in computer-aided design tools, including a hardware description language (Verilog) in the analysis and design of digital circuits	• Assignments • Mid-Term Assessment • Final Examination • Laboratory practical experiments

Learning and Teaching Technologies

Moodle - Learning Management System | Microsoft Teams

Learning and Teaching in this course

Course program

The course consists of pre-recorded videos lectures available online, one 2-hour discussion sessions, one 2-hour workshop, and one 2-hour laboratory session each week.

Lecture program

Pre-recorded video lectures explaining the course content will be available on Moodle in the corresponding weekly section. Each video explains the content for a specific topic and examples to help understand the material. Students are expected to watch all the videos assigned for each week prior to the discussion session on Mondays. In the discussion session, the material in the videos will be revised and examples solved in more detail. Addtional problems will also be solved in a group setting. The discussion session will be offered in-person only. Recordings will not be avialable for the discussion sessions.

Workshop program

Workshops will be held in Weeks 2-10. You should attempt all of the questions in the workshop sheet posted on Moodle in advance of attending the workshops. The importance of adequate preparation prior to each workshop cannot be overemphasized, as the effectiveness and usefulness of the workshop depends to a large extent on this preparation. Group learning is encouraged. Answers for these questions will be discussed during the workshop and the tutor will cover the more complex questions in the workshop. In addition, during the workshop, you will be quizzed individually on similar but new questions which will be marked and count towards your final mark. Solutions to the workshop questions and videos explaining the solutions will be posted on Moodle at the end of the week.

Laboratory program

Laboratories will be held in Weeks 2-10. The laboratory schedule is deliberately designed to provide practical, hands-on exposure to the concepts conveyed in lectures. Each week a new design problem is presented. Students will be required to step through the problem to a

complete solution using the guidelines given as per lab exercise. The laboratory exercises cover a wide scope ranging from using breadboards and discrete IC components to using industry-standard design software and FPGA implementation. The exercise will follow similar (although simplified) design procedures used in industry.

The laboratory manual will be uploaded on Moodle. Every student will need to bring a lab pack with them to the lab, that can be ordered online from https://recharge.it.unsw.edu.au, prior to attending the first laboratory class. The lab pack will contain all hardware components you will need for the entire lab. Without the hardware components in the lab pack, you will not be able to do some of the laboratory activities and therefore it is important you bring you lab pack to the laboratory class. You will also need to bring the breadboards previously used in ELEC1111 to the laboratory. Breadboards will also be offered for sale through the school office.

Laboratory attendance WILL be kept, and you MUST attend at least 80% of the labs. Prior to attending each lab, you must read over each lab in the lab manual and complete the pre-lab quiz on Moodle before each session. You will not be allowed to start the lab unless you have answered all the questions in the pre-lab quiz.

A broad understanding of the tools utilized in these exercises is highly encouraged and a bonus lab task will be available to students after the successful completion of all other exercises. The bonus task will carry on from the last lab exercise and will be accompanied by minimal guidelines, allowing students to further demonstrate their ability to analyse and resolve issues independently. The optional labs should be done under minimal supervision and only considered or marked after the student has finished all mandatory labs.

Other Professional Outcomes

Engineers Australia, Professional Engineer Stage 1 Competencies

The learning outcomes of this course contribute to your development of the following EA competencies:

	EA Stage 1 Competencies	Course Learning Outcomes (CLOs)
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	1, 2, 3, 4, 5, 6, 7
PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing		1, 2, 3, 4, 5, 6, 7
PE1.3 In-depth understanding of specialist bodies of knowledge		1, 2, 3, 4, 5, 6, 7
PE1.4 Discernment of knowledge development and research directions		
PE1.5 Knowledge of engineering design practice		1, 2, 3, 4, 5, 6, 7
PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice		
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	1, 2, 3, 4, 5, 6, 7
PE2.2 Fluent application of engineering techniques, tools and resources		1, 2, 3, 4, 5, 6, 7
PE2.3 Application of systematic engineering synthesis and design processes		
PE2.4 Application of systematic approaches to the conduct and management of engineering projects		
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability	
PE3.2 Effective oral and written communication (professional and lay domains)		5, 6
PE3.3 Creative, innovative and pro-active demeanour		5, 6
PE3.4 Professional use and management of information		5, 6
PE3.5 Orderly management of self, and professional conduct		
PE3.6 Effective team membership and team leadership		5, 6

Additional Course Information

Workload

The expected workload is 15 hours per week throughout the 10-week term.

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates
Assignments Assessment Format: Individual	20%	Start Date: Not Applicable Due Date: Not Applicable
Mid-Term Assessment Assessment Format: Individual	25%	Start Date: Not Applicable Due Date: Not Applicable
Final Examination Assessment Format: Individual	35%	Start Date: Not Applicable Due Date: Not Applicable
Laboratory practical experiments Assessment Format: Group	20%	Start Date: Not Applicable Due Date: Not Applicable

Assessment Details

Assignments

Assessment Overview

The assignments will consist of two design challenges, each worth 10% of the overall course marks,. Students are required to provide a complete design solution with verified implementations.

Though generic guidelines will be provided, there will be no one “correct” solution to the assignments. Students will be expected to work independently on their implementation and to be able to justify the unique design choices along the way.

Course Learning Outcomes

- CLO1 : Analyse and design combinational circuits
- CLO2 : Implement combinational circuits using standard digital circuit elements such as multiplexers, decoders, etc
- CLO3 : Design and optimize simple synchronous sequential circuits
- CLO5 : Implement simple designs at various levels employing knowledge of practical aspects of digital circuits and systems and their use in more complex systems
- CLO6 : Demonstrate understanding of the various hardware realizations of the basic digital circuit elements
- CLO7 : Apply basic skills in computer-aided design tools, including a hardware description language (Verilog) in the analysis and design of digital circuits

Detailed Assessment Description

There will be two assignments for this subject due at the end of week 6 and 9. The assignments will be released at the end of week 2 and week 6, respectively, on Moodle. The assignments will consist of one or more design problems. The complete designs as well as their verified

implementations including relevant workings, schematic diagrams, HDL codes, and simulations results must be attached to the submissions. All submissions must be made electronically via Moodle. **Assignment 1 is due on March 25, 23:55 (Monday, Week 7). Assignment 2 is due on April 22, 23:55 (Monday, Week 11). No late submission will be possible after the due time.**

Assignment submission Turnitin type

This is not a Turnitin assignment

Mid-Term Assessment

Assessment Overview

The midterm assessment has two parts:

1. Regular quizzes throughout the term, worth 10% of the overall course marks. The purpose of the quizzes is to keep students up to date with the lecture material and to test understanding of the course concepts.
2. A midterm exam, worth 15% of the overall course marks, that tests analytical and critical thinking and general understanding of the course material presented prior to the exam in a controlled fashion.

Course Learning Outcomes

- CLO1 : Analyse and design combinational circuits
- CLO2 : Implement combinational circuits using standard digital circuit elements such as multiplexers, decoders, etc
- CLO3 : Design and optimize simple synchronous sequential circuits
- CLO4 : Examine the fundamental components of the central processing unit (CPU) in a computer and their workings
- CLO6 : Demonstrate understanding of the various hardware realizations of the basic digital circuit elements
- CLO7 : Apply basic skills in computer-aided design tools, including a hardware description language (Verilog) in the analysis and design of digital circuits

Detailed Assessment Description

Weekly Workshop Quizzes

There will be weekly quizzes in each of the workshops throughout the term. The purpose of the quizzes is to keep students up to date with the lecture material and to test understanding of the course concepts. These quizzes will make up 10% of the overall mark. Each quiz will consist of a number of randomly selected questions from a pool of questions so that students may not have exactly the same set of questions. The quiz will be marked according to the number of correct answers. The quizzes are a mandatory component of the overall assessment and failure to

attempt a quiz will result in no marks being given for the quiz. Each quiz will only be available during the workshop. No late attempts will be permitted. **Quizzes should be attempted genuinely and independently. If Moodle suspects dependent and insincere practices, it will alert the course convener.**

Mid-Term Exam

The midterm exam in this course is a 1-hour examination, comprising two compulsory questions. It accounts for 15% of the overall mark. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions will be drawn from the topics covered in the first four weeks of the course, unless specifically indicated otherwise by the lecturer. Marks will be assigned according to the correctness of the responses. The exam will be held in week 5.

Assessment Length

1 hour

Assignment submission Turnitin type

Not Applicable

Final Examination

Assessment Overview

The final exam in this course is a cumulative written examination that tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including laboratory), unless specifically indicated otherwise by the lecturer.

Course Learning Outcomes

- CLO1 : Analyse and design combinational circuits
- CLO2 : Implement combinational circuits using standard digital circuit elements such as multiplexers, decoders, etc
- CLO3 : Design and optimize simple synchronous sequential circuits
- CLO4 : Examine the fundamental components of the central processing unit (CPU) in a computer and their workings
- CLO6 : Demonstrate understanding of the various hardware realizations of the basic digital circuit elements
- CLO7 : Apply basic skills in computer-aided design tools, including a hardware description language (Verilog) in the analysis and design of digital circuits

Detailed Assessment Description

The exam in this course is a two-hour cumulative written examination, comprising four compulsory questions. It accounts for 35% of the overall mark. University approved calculators are allowed. Marks will be assigned according to the correctness of the responses.

Assessment Length

2 hours

Assignment submission Turnitin type

Not Applicable

Laboratory practical experiments

Assessment Overview

The laboratory component of the course consists of two parts:

1. Weekly laboratory assessments, worth 15% of the overall course marks, in which students will work on weekly practical design task. Students will work in pairs but be marked individually. There will also be a mark for the group based on demonstrating the required lab tasks.
2. Final lab exam at the end of term, worth 5% of the overall course marks, to check students have achieved the practical learning outcomes for the course. This is a closed book practical exam that will assess students' technical understanding on design software tools used throughout the labs in simulating, verifying, and implementing digital circuits on the FPGA board.

Course Learning Outcomes

- CLO1 : Analyse and design combinational circuits
- CLO2 : Implement combinational circuits using standard digital circuit elements such as multiplexers, decoders, etc
- CLO3 : Design and optimize simple synchronous sequential circuits
- CLO5 : Implement simple designs at various levels employing knowledge of practical aspects of digital circuits and systems and their use in more complex systems
- CLO6 : Demonstrate understanding of the various hardware realizations of the basic digital circuit elements
- CLO7 : Apply basic skills in computer-aided design tools, including a hardware description language (Verilog) in the analysis and design of digital circuits

Detailed Assessment Description

Laboratory Assessment

Laboratories are primarily about learning, and the laboratory assessment is designed mainly to check your knowledge as you progress through each stage of the laboratory tasks. It is essential

that you complete the laboratory preparation before coming to the lab. **This includes reading over each lab in the lab manual and completing the pre-lab quiz on Moodle before each session. Students will not be allowed to start the lab unless they have answered all the questions in the pre-lab quiz. Students will have unlimited attempts to complete the pre-lab quiz.** Each lab exercise will have one check point that will be marked by the laboratory demonstrators. Although there is only one check point for each lab, there are several results that students are required to demonstrate when marked for the check point. Therefore, you are strongly advised to (i) record results on the lab manual; (ii) save the accomplished tasks or results on working directory in the lab PC; (iii) keep the working circuit on the breadboard for the laboratory demonstrators to check. Laboratory demonstrators will be available to help students with any questions or difficulties.

Upon completion of a checkpoint, students will be required to write down their student and bench numbers on the Laboratory Queue Sheet and wait for the laboratory assessor to mark their work. Students may continue working on subsequent lab tasks while waiting to be assessed. Students will be required to show the working of their task for each checkpoint and answer questions asked by the laboratory assessor to demonstrate their understanding of the ideas addressed within each task.

Students will work in pairs but be marked individually. Each student will be asked a few questions. There will also be a mark for the group based on demonstrating the required lab tasks. Refer to the laboratory manual for the marking guideline.

Assessment marks will be awarded according to your preparation (completing set preparation exercises and correctness of these or readiness for the lab in terms of pre-reading), how much of the lab you were able to complete, your understanding of the experiments conducted during the lab, the quality of the code you write during your lab work (according to the guidelines given in lectures), and your understanding of the topic covered by the lab.

After completing each experiment, your work will be assessed by the laboratory demonstrator. Both the results sheet and your lab book will be assessed by the laboratory demonstrator.

Laboratory Exam

To check that you have achieved the practical learning outcomes for the course, you will be examined in the laboratory. Laboratory Exams are closed book practical exams that will assess your technical understanding of using design software tools used throughout the labs in simulating, verifying, and implementing digital circuits on the FPGA board. You will be given two

design problems, asked to implement and verify the design on the FPGA board. Marks will be awarded for the correct understanding of practical and relevant theoretical concepts, correct operation of laboratory equipment, and correct interpretation of measured results.

Assignment submission Turnitin type

Not Applicable

General Assessment Information

The assessment scheme in this course reflects the intention to assess your learning progress through the term. Ongoing assessment occurs through the lab checkpoints (see lab manual), lab exam, mid-term assessments and two assignments. There will be a final cumulative exam at the end of term.

Grading Basis

Standard

Course Schedule

Teaching Week/Module	Activity Type	Content
Week 1 : 12 February - 18 February	Topic	Introduction to digital systems, number systems & combinational logic circuits
Week 2 : 19 February - 25 February	Topic	Combinational logic circuit analysis
	Laboratory	Introduction to digital circuits
Week 3 : 26 February - 3 March	Topic	Combinational logic circuit design
	Laboratory	Xilinx ISE and Digilent Nexys 3
Week 4 : 4 March - 10 March	Topic	Combinational circuit blocks & arithmetic circuits
	Laboratory	Comprehensive Guide to FPGA Programming
Week 5 : 11 March - 17 March	Assessment	Midterm exam
	Laboratory	Combinational circuit design
Week 7 : 25 March - 31 March	Topic	Sequential circuit elements and analysis
	Laboratory	Flip-Flop basics
	Assessment	Assignment 1 due
Week 8 : 1 April - 7 April	Topic	Sequential circuit design
	Laboratory	Sequential circuit design
Week 9 : 8 April - 14 April	Topic	Registers and computer design fundamentals
	Laboratory	Addressable RGB LED Controller Design
Week 10 : 15 April - 21 April	Topic	Digital logic families and CMOS technology
	Laboratory	Lab exam
	Assessment	Assignment 2 due

Attendance Requirements

Please note that lecture recordings are not available for this course. Students are strongly

encouraged to attend all classes and contact the Course Authority to make alternative arrangements for classes missed.

Course Resources

Prescribed Resources

M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016.

Recommended Resources

M. Mano, C. R. Kime, Logic and Computer Design Fundamentals, 4th Edition, Prentice Hall, 2008

R. H. Katz & G. Borriello, Contemporary Logic Design, 2nd Edition, Prentice Hall, 2005

M. Mano & M. D. Cilietti, Digital Design, 4th Edition, Prentice Hall, 2007

J. F. Wakerly, Digital Design: Principles and Practices, 4th Edition, Prentice Hall, 2006

Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods.

The students use the online lecture recordings extensively so more detailed recordings will be created to better support their learning. Additional problem solving videos have been created and will be provided to the students. Qujizzes have been added to the workshops to provide problem solving practice.

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Convenor	Beena Ahmed		EE&T 444		Wed 3-5 pm	No	Yes
Lab staff	Riley Dean					No	No
Tutor	Waheeda Jab bar					No	No

Other Useful Information

Academic Information

I. Special consideration and supplementary assessment

If you have experienced an illness or misadventure beyond your control that will interfere with your assessment performance, you are eligible to apply for Special Consideration prior to, or within 3 working days of, submitting an assessment or sitting an exam.

Please note that UNSW has a Fit to Sit rule, which means that if you sit an exam, you are declaring yourself fit enough to do so and cannot later apply for Special Consideration.

For details of applying for Special Consideration and conditions for the award of supplementary assessment, please see the information on UNSW's Special Consideration page.

II. Administrative matters and links

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Attendance
- UNSW Email Address
- Special Consideration
- Exams
- Approved Calculators
- Academic Honesty and Plagiarism
- Equitable Learning Services

III. Equity and diversity

Those students who have a disability that requires some adjustment in their teaching or learning environment are encouraged to discuss their study needs with the course convener prior to, or at the commencement of, their course, or with the Equity Officer (Disability) in the Equitable Learning Services. Issues to be discussed may include access to materials, signers or note-takers, the provision of services and additional exam and assessment arrangements. Early notification is essential to enable any necessary adjustments to be made.

IV. Professional Outcomes and Program Design

Students are able to review the relevant professional outcomes and program designs for their streams by going to the following link: https://www.unsw.edu.au/engineering/student-life/student-resources/program-design.

Note: This course outline sets out the description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle or your primary learning management system (LMS) should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline/Moodle/LMS, the description in the Course Outline/Moodle/LMS applies.

Academic Honesty and Plagarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. *Plagiarism at UNSW is defined as using the words or ideas of others and passing them off as your own.*

Plagiarism is a type of intellectual theft. It can take many forms, from deliberate cheating to accidentally copying from a source without acknowledgement. UNSW has produced a website with a wealth of resources to support students to understand and avoid plagiarism, visit: student.unsw.edu.au/plagiarism. The Learning Centre assists students with understanding academic integrity and how not to plagiarise. They also hold workshops and can help students one-on-one.

You are also reminded that careful time management is an important part of study and one of the identified causes of plagiarism is poor time management. Students should allow sufficient time for research, drafting and the proper referencing of sources in preparing all assessment tasks.

Repeated plagiarism (even in first year), plagiarism after first year, or serious instances, may also be investigated under the Student Misconduct Procedures. The penalties under the procedures can include a reduction in marks, failing a course or for the most serious matters (like plagiarism in an honours thesis or contract cheating) even suspension from the university. The Student Misconduct Procedures are available here:

www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf

Submission of Assessment Tasks

Work submitted late without an approved extension by the course coordinator or delegated authority is subject to a late penalty of five percent (5%) of the maximum mark possible for that assessment item, per calendar day.

The late penalty is applied per calendar day (including weekends and public holidays) that the assessment is overdue. There is no pro-rata of the late penalty for submissions made part way through a day. This is for all assessments where a penalty applies.

Work submitted after five days (120 hours) will not be accepted and a mark of zero will be awarded for that assessment item.

For some assessment items, a late penalty may not be appropriate. These will be clearly indicated in the course outline, and such assessments will receive a mark of zero if not completed by the specified date. Examples include:

- Weekly online tests or laboratory work worth a small proportion of the subject mark;
- Exams, peer feedback and team evaluation surveys;
- Online quizzes where answers are released to students on completion;
- Professional assessment tasks, where the intention is to create an authentic assessment that has an absolute submission date; and,
- Pass/Fail assessment tasks.

Faculty-specific Information

Engineering Student Support Services – The Nucleus - enrolment, progression checks, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries e.g. admissions, fees, programs, credit transfer

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

School-specific Information

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Use of AI for assessments

Your work must be your own. If you use AI in the writing of your assessment, you must acknowledge this and your submission must be substantially your own work. More information can be found on this website.

Workplace Health & Safety (WHS)

WHS for students and staff is of utmost priority. Most courses involve laboratory work. You must follow the rules about conduct in the laboratory. About COVID-19, advice can be found on this website.

School Contact Information

Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Student Support Enquiries

For enrolment and progression enquiries please contact Student Services

Web

Electrical Engineering Homepage