UNSW Course Outline

ELEC4603 Solid State Electronics - 2024

Published on the 26 Aug 2024

General Course Information

Course Code : ELEC4603
Year : 2024
Term : Term 3
Teaching Period : T3
Is a multi-term course? : No
Faculty : Faculty of Engineering
Academic Unit : School of Electrical Engineering & Telecommunications
Delivery Mode : In Person
Delivery Format : Standard
Delivery Location : Kensington
Campus : Sydney
Study Level : Postgraduate, Undergraduate
Units of Credit : 6

Useful Links

Handbook Class Timetable

Course Details & Outcomes

Course Description

Solid state electronics has been the number one tool that engineers choose to create novel technologies, from mobile phones to solar cells. By taking this course you will learn how to stay on top of the new inventions of the future.

- What are the challenges in making better CPUs? Does it need to be made out of silicon at all?
- How can we produce more colourful monitor screens? What limits photonic communication? When will detectors enable my car to self-drive?
- What if the devices get so small that you only have a few atoms and electrons? And what is the big deal with nanotechnology?

This is an elective course for computer, telecommunications, and electrical engineering students. It provides a detailed understanding of the physics, design, operation, and limitations of important solid-state electronic and optoelectronic devices used by electrical and telecommunications engineers. It is highly relevant for electrical engineers who intend to pursue further studies of integrated circuit design and/or microfabrication. The topics to be covered include the following:

- Band-structure and doping of semiconductors.
- Drift-Diffusion Equations; Density of states; Fermi function; Law of Mass Action.
- PN Junctions: Derivation of I-V characteristics; Capacitance; Breakdown; Non-idealities.
- Bipolar Junction Transistor (BJT): Operation principles; Derivation of I-V characteristics; Ebers-Moll model; Non-idealities.
- MOSFET: Derivation of I-V characteristics; Structure; Threshold Voltage; Operating modes. CMOS devices.
- Microfabrication of: BJTs; MOSFETs; CMOS; Integrated circuits.
- Quantum effects: Tunnelling effects in diodes; Tunnel FETs; Quantization of transport; Energy levels in ultra-scaled transistors.
- Optoelectronic & Photonic Devices: Direct vs Indirect Band-gap devices.
- LEDs; Semiconductor Lasers; Photovoltaic Cells.

Course Aims

This course expands significantly on the simple models of electronic devices studied in ELEC2133 (Analogue Electronics) and uses concepts of solid-state physics learned in PHYS1231 (Physics 1B). At the end of the course, you should:

1. understand the underlying operating principles of important microelectronic and photonic devices, such as MOSFETs, BJTs, and semiconductor lasers;
2. understand the limits of ideal "black box" models of devices, and predict the effect of these nonidealities on real circuits and systems;
3. have an appreciation of the principles of microfabrication relevant to integrated circuit manufacture, and how these affect device performance.
4. have a vision for the future of technology and the independence to self-teach the necessary science to understand it.

Relationship to Other Courses

This is a 4th year course in the School of Electrical Engineering and Telecommunications. It is an elective course for computer, telecommunications, and electrical engineering students (including combined degrees).

Pre-requisites and Assumed Knowledge

The prerequisite for this course is ELEC2133 Analogue Electronics. It will be assumed that students have mastered this subject. Students are strongly advised to revise any unfamiliar topics in their own time.

Following Courses

There are no following courses for this course, but it suits for students aiming for postgraduate level course ELEC9704 VLSI Technology.

Course Learning Outcomes

Course Learning Outcomes
CLO1 : Explain the key concepts involved in semiconductor device operation and their characteristics
CLO2 : Perform calculation and analysis of semiconductor devices through applying fundamental equations and constants
CLO3 : Validate the performance of diodes, transistors and optoelectronics through experiments and simulations
CLO4 : Illustrate CMOS fabrication processes, pinpointing future opportunities and challenges of massive integration
CLO5 : Recognise the onset of quantum effects and its importance for aggressively miniaturized devices
CLO6 : Collaborate in teams to create shared content with diverse pedagogy on solid state electronics and relevant background knowledges

Course Learning Outcomes	Assessment Item
CLO1 : Explain the key concepts involved in semiconductor device operation and their characteristics	• Quizzes • Laboratory • Wiki Project • Final Examination
CLO2 : Perform calculation and analysis of semiconductor devices through applying fundamental equations and constants	• Quizzes • Laboratory • Final Examination
CLO3 : Validate the performance of diodes, transistors and optoelectronics through experiments and simulations	• Laboratory
CLO4 : Illustrate CMOS fabrication processes, pinpointing future opportunities and challenges of massive integration	• Wiki Project • Final Examination
CLO5 : Recognise the onset of quantum effects and its importance for aggressively miniaturized devices	• Quizzes • Wiki Project • Final Examination
CLO6 : Collaborate in teams to create shared content with diverse pedagogy on solid state electronics and relevant background knowledges	• Wiki Project

Learning and Teaching Technologies

Moodle - Learning Management System | Microsoft Teams

Other Professional Outcomes

Relationship to Engineers Australia Stage 1 competencies:

The Course Learning Outcomes (CLOs) contribute to the Engineers Australia (National Accreditation Body) Stage I competencies as outlined below

Engineers Australia (EA), Professional Engineer Stage 1 Competencies

PE1: Knowledge and Skill Base:
PE1.1 Comprehensive, theory-based **understanding of underpinning fundamentals**: CLO 1, 2
PE1.2 Conceptual understanding of underpinning maths, **analysis**, statistics, **computing**: CLO 1, 2
PE1.3 In-depth understanding of specialist bodies of **knowledge**: CLO 2, 3, 4
PE1.4 Discernment of knowledge development and research directions: NA
PE1.5 Knowledge of **engineering design** practice: CLO 3, 4
PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice: NA

PE2: Engineering Application Ability:
PE2.1 Application of established engineering methods to **complex problem solving**: CLO 2, 3, 4
PE2.2 Fluent **application of engineering techniques**, tools and resources: CLO 1, 2, 3, 4
PE2.3 Application of systematic engineering synthesis and design processes: NA
PE2.4 Application of systematic approaches to the conduct and management of engineering projects: NA

PE3: *Professional and Personal Attributes:*
PE3.1 Ethical conduct and professional accountability: CLO 4
PE3.2 Effective **oral and written communication** (professional and lay domains): CLO 4
PE3.3 **Creative, innovative** and pro-active demeanour: CLO 3, 4
PE3.4 Professional use and management of information: NA
PE3.5 Orderly management of **self, and professional conduct**: CLO 4
PE3.6 Effective team membership and team leadership: NA

This course is also designed to provide the course learning outcomes which arise from targeted graduate capabilities. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (also listed below).

Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning

UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing scholars who have a deep understanding of their discipline, through lectures and solution of analytical problems in tutorials and assessed by assignments and written examinations.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved by the laboratory experiments and interactive checkpoint assessments and lab exams during the labs.
- Developing capable independent and collaborative enquiry, through a series of tutorials spanning the duration of the course.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through challenging design and project tasks.
- Developing citizens who can apply their discipline in other contexts, are culturally aware and environmentally responsible, through interdisciplinary tasks, seminars and group activities

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates
Quizzes Assessment Format: Individual	20%	
Laboratory Assessment Format: Individual	20%	
Wiki Project Assessment Format: Group	30%	
Final Examination Assessment Format: Individual	30%	

Assessment Details

Quizzes

Assessment Overview

After the previous week's tutorial and watching the weekly pre-lecture recordings, you are required to answer simple questions on Moodle. Due before the next lecture. Marks are assigned according to correct or closest answers and verbal class-wide feedback will be given during lectures.

Course Learning Outcomes

- CLO1 : Explain the key concepts involved in semiconductor device operation and their characteristics
- CLO2 : Perform calculation and analysis of semiconductor devices through applying fundamental equations and constants
- CLO5 : Recognise the onset of quantum effects and its importance for aggressively miniaturized devices

Detailed Assessment Description

1. The bulk of the content is delivered by Pre-Recorded Videos of 7 to 16 min duration, which can be watched on your time. There is a total of 20 to 25 videos. You are supposed to watch a average of 3 videos per week. (Estimated time: 45min/week)
2. You will answer simple questions about the videos for that week. These questions are simple enough that you can answer them by simply watching the videos with attention. Correctly answering this Quiz will account for 10% of your marks. (Estimated time: 15min/week)
3. In the Tutorial, you will discuss problems that follows the lecture, as well as further applications of the content in real-life engineering problems. We will have 9 tutorials in 2024. (Estimated time: 60 min/week)
4. You will then get a more challenging, math-based question to answer. This part of the Quiz will account for another 10% of your total marks, which adds up to 20% with the Pre-Recorded

videos questions. You will have until the follwing week's Lecture to answer that question. (Estimated time: 30 min/week)

Generative AI Permission Level

No Assistance

This assessment is designed for you to complete without the use of any generative AI. You are not permitted to use any generative AI tools, software or service to search for or generate information or answers.
For more information on Generative AI and permitted use please see here.

Laboratory

Assessment Overview

Students work in groups but will be assessed individually. Marks are given based on the report you have prepared during each laboratory session. The report will contain short paragraphs of the findings of the experiment/simulation and include screenshots or any other output formats from the software. You will be asked random questions from the demonstrators and received verbal feedback; satisfactory answers are expected in order to receive the marks.

Course Learning Outcomes

- CLO1 : Explain the key concepts involved in semiconductor device operation and their characteristics
- CLO2 : Perform calculation and analysis of semiconductor devices through applying fundamental equations and constants
- CLO3 : Validate the performance of diodes, transistors and optoelectronics through experiments and simulations

Detailed Assessment Description

There are 6 laboratory sessions with one preparation Lab-0 to install softwares and registering online accounts for simulation.

Lab-0 contributres 1% and Lab-1 3% to the course total marks. From Lab-2 to Lab-5 each contributes 4% to the total marks.

Your performance on labs will amount to 20% of your final marks. (Estimated time: (180 min x 5 main sessions)= 90min/week)

Demonstrators will strictly follow the guideline below during the assessment:

1. All preliminary preparation, results of experimental measurements and discussion of results must be **neatly recorded** in a laboratory book or electronic document.
2. Marking will only be done during the laboratory period by the demonstrator's present through **oral assessment**. It is the responsibility of the students to make sure that his/her mark is recorded by the demonstrator.
3. Experiments will **only** be marked during a student's assigned lab time. Do not attend another lab group to get marked unless permission has been given by a demonstrator

Hurdle rules

A pass grade in laboratory component is required to pass this course overall.

Generative AI Permission Level

Simple Editing Assistance

In completing this assessment, you are permitted to use standard editing and referencing functions in the software you use to complete your assessment. These functions are described below. You must not use any functions that generate or paraphrase passages of text or other media, whether based on your own work or not.
If your Convenor has concerns that your submission contains passages of AI-generated text or media, you may be asked to account for your work. If you are unable to satisfactorily demonstrate your understanding of your submission you may be referred to UNSW Conduct & Integrity Office for investigation for academic misconduct and possible penalties.
For more information on Generative AI and permitted use please see here.

Wiki Project

Assessment Overview

Details of the Wiki project will be handed out in a separate project description document. You will be given topics that are covered in the course, and build wiki notes around them. You will be creating summarised lecture notes, questions and their worked-out example, a review of relevant backgrounds, and any supporting multimedia materials. You are strongly encouraged to build up each Wiki topic before its corresponding lecture in order to receive feedback during the lecture. The total course mark will be given as group marks, unless under special circumstances where the marks will be modified for each individual. Details of the marking rubrics will be given in the projection description. Written comments are provided on the report where appropriate.

Course Learning Outcomes

- CLO1 : Explain the key concepts involved in semiconductor device operation and their characteristics

- CLO4 : Illustrate CMOS fabrication processes, pinpointing future opportunities and challenges of massive integration
- CLO5 : Recognise the onset of quantum effects and its importance for aggressively miniaturized devices
- CLO6 : Collaborate in teams to create shared content with diverse pedagogy on solid state electronics and relevant background knowledges

Detailed Assessment Description

You and your team will work together in writing some Wiki-Style lecture notes. The topics for these notes are assigned to each team, and typically a team will have one topic to write about every two weeks. The whole class can see your notes and use them for their own learning. They can also help you by providing constructive criticism. You will get marks for these notes, so the more input you get from your colleagues before we mark them, the better for you. These notes have a well-defined structure and marking rubrics, and will amount to 30% of your final marks. (Estimated time: 240 min every 2 weeks = 120min/week)

The Wiki will be marked at two check points: end of **Week 5 (10%)** and end of **Week 10 (20%)**.

Generative AI Permission Level

Assistance with Attribution

This assessment requires you to write/create a first iteration of your submission yourself. You are then permitted to use generative AI tools, software or services to improve your submission in the ways set out below.
Any output of generative AI tools, software or services that is used within your assessment must be attributed with full referencing.
If outputs of generative AI tools, software or services form part of your submission and are not appropriately attributed, your Convenor will determine whether the omission is significant. If so, you may be asked to explain your submission. If you are unable to satisfactorily demonstrate your understanding of your submission you may be referred to UNSW Conduct & Integrity Office for investigation for academic misconduct and possible penalties.
For more information on Generative AI and permitted use please see here.

Final Examination

Assessment Overview

This two-hour written exam aims to assess students' competency. Questions may be drawn from any aspect of the course. Marks will be assigned according to the correctness of the responses.

Course Learning Outcomes

- CLO1 : Explain the key concepts involved in semiconductor device operation and their characteristics
- CLO2 : Perform calculation and analysis of semiconductor devices through applying fundamental equations and constants
- CLO4 : Illustrate CMOS fabrication processes, pinpointing future opportunities and challenges of massive integration
- CLO5 : Recognise the onset of quantum effects and its importance for aggressively miniaturized devices

Detailed Assessment Description

Final Exam, worth 30% of your final marks. This is a more traditional, summative assessment, but we will base it strongly on the quizzes and content generated by the students in the Wiki-Style Lecture Notes. (Estimated time: 120 min)

Assignment submission Turnitin type

Not Applicable

Generative AI Permission Level

No Assistance

This assessment is designed for you to complete without the use of any generative AI. You are not permitted to use any generative AI tools, software or service to search for or generate information or answers.
For more information on Generative AI and permitted use please see here.

General Assessment Information

Grading Basis

Standard

Requirements to pass course

You must pass both the laboratory component (50%) and achieve an overall grade of at least 50% to pass the course.

Course Schedule

Teaching Week/Module	Activity Type	Content
Week 1 : 9 September - 15 September	Lecture	Introduction to course Band-structure and doping profile of semiconductors
	Workshop	Introduction to Wiki project.
	Tutorial	Tute 1
	Homework	Pre-lecture recording and Quiz
Week 2 : 16 September - 22 September	Lecture	Carrier motion and continuity
	Workshop	Group assignment for Wiki project
	Laboratory	Lab 0
	Tutorial	Tute 2
	Homework	Pre-lecture recording and Quiz
Week 3 : 23 September - 29 September	Lecture	p-n junction
	Workshop	Lecture extra hour
	Laboratory	Lab 1
	Tutorial	Tute 3/4
	Homework	Pre-lecture recording and Quiz
Week 4 : 30 September - 6 October	Lecture	BJT
	Workshop	Wiki catch up
	Laboratory	Lab 2
	Tutorial	Tute 4/5
	Homework	Pre-lecture recording and Quiz
Week 5 : 7 October - 13 October	Laboratory	Lab 3
	Tutorial	Tute 6
	Homework	Pre-lecture recording and Quiz
	Assessment	Wiki project check point 1
Week 6 : 14 October - 20 October	Lecture	Flexible week Revision
	Workshop	Flexible week Revision
Week 7 : 21 October - 27 October	Lecture	MOSFET
	Workshop	Lecture extra hour
	Laboratory	Lab 4
	Tutorial	Tute 7
	Homework	Pre-lecture recording and Quiz
Week 8 : 28 October - 3 November	Lecture	Quantum effects
	Workshop	Wiki catch up
	Laboratory	Lab 5
	Tutorial	Tute 9
	Homework	Pre-lecture recording and Quiz
Week 9 : 4 November - 10 November	Lecture	Guest Lecturer, microfabrication
	Homework	Pre-lecture recording and Quiz
	Tutorial	Tute 8
	Homework	Pre-lecture recording and Quiz
Week 10 : 11 November - 17 November	Lecture	Optoelectronics
	Workshop	Revision
	Laboratory	Catch-up lab
	Tutorial	Tute 10
	Homework	Pre-lecture recording and Quiz
	Assessment	Wiki project check point 2

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

General Schedule Information

Lectures run weekly on Monday 1pm to 3pm, in Electrical Engineering G23 (K-G17-G23).

Workshop sessions will run after the lectures on Monday 3pm to 4pm, in Mathews 310 (K-F23-310) (Monday 5pm to 6pm, in Law Building 203 (K-F8-203)).

Tutorials run weekly on Thursday 9am to 10am (10am to 11am), in Mathews 214 (K-F23-214).

You are required to take quizzes weekly. Quiz due at beginning of each lecture, where you are required to watch pre-recorded videos in order to answer.

You are required to attend ALL laboratories. Laboratory sessions are scheduled in Week 2,3,4,5,7,8. (Monday session will extend to Week 10)

There will be two check points of the Collaborative Wiki project, where marks will be awarded based on the content at the check points.

Schedule is subject to change.

Course Resources

Prescribed Resources

Textbooks

The prescribed textbook (free library access) set for this course is:

- Christo Papadopoulos, Solid-State Electronic Devices: An Introduction (Springer, 2014). https://primoa.library.unsw.edu.au/permalink/f/238ui7/UNSWALMA51227971010001731

An alternative textbook, which covers much of the same material, but with greater emphasis on semiconductor fabrication, is:

- S. M. Sze & M. K. Lee, Semiconductor Devices, Physics and Technology (Wiley, 3rd ed., 2012). https://primoa.library.unsw.edu.au/permalink/f/1gq3lal/UNSWALMA21173723460001731

Muller & Kamins was formerly the textbook for this course:

- R. S. Muller, T. I. Kamins & M. Chan, Device Electronics for Integrated Circuits (Wiley, 3rd ed.,

2003). https://primoa.library.unsw.edu.au/permalink/f/1gq3lal/UNSWALMA21171428390001731

On-line resources

Microsoft Teams

- As a part of the teaching component, Microsoft Teams will be used to disseminate teaching materials, host channels and occasionally. Assessment marks will also be made available via Microsoft Teams: https://student.unsw.edu.au/teams-students

Moodle

- Moodle will be used to host quizzes. https://moodle.telt.unsw.edu.au/

Mailing list

- Announcements concerning course information will be given in the lectures and/or on Microsoft Teams and/or via email (which will be sent to your student email address).

Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods.

Starting 2020, this course has been refreshed with content that fits better with modern solid-state technologies, with additional delivery methods such as quizzes. Changes in content included dropping the section on legacy digital circuits, and inclusion of quantum effect of nano-scale transistors.

In 2021, with collective feedbacks from the students, further changes to the course has been made.

- The lecturer/tutorial hours has been readjusted. More turotial sessions have been introduced to ensure students have more problem solving chances.
- The new colloborative Wiki project encourages students to engage with each other online, and perform a literature review style group-learning platform.
- Laboratory transformations are in the progress, dropping what students find as "irrelavant contents" to the course. However, new 2021 laboratory activities will be online simulation only

due to lockdown restrictions.

In 2024, to further enhance the quality of teaching and to accommodate the increasing class size, an extra workshop was introduced. This workshop aims to provide additional support for students, offering opportunities for catch-up sessions and reinforcing key concepts. Additionally, it plays a crucial role in aiding the collaborative Wiki project, helping to support group learning and engagement. This change reflects our ongoing commitment to adapting the course structure to better meet the needs of our students.

The overall change is to move towards a more formative learning environment, providing more progressive feedback rather than focusing on summative assessments.

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Convenor	Henry Yang		315 Newton Building	+61 2 9065 9874	Through Microsoft Teams	Yes	Yes
	Tuomo Tanttu		315 Newton Building	+61 401 517972	Through Microsoft Teams	Yes	No
Tutor	Mengke Feng				Contact via email	No	No

Other Useful Information

Academic Information

I. Special consideration and supplementary assessment

If you have experienced an illness or misadventure beyond your control that will interfere with your assessment performance, you are eligible to apply for Special Consideration prior to, or within 3 working days of, submitting an assessment or sitting an exam.

Please note that UNSW has a Fit to Sit rule, which means that if you sit an exam, you are declaring yourself fit enough to do so and cannot later apply for Special Consideration.

For details of applying for Special Consideration and conditions for the award of supplementary assessment, please see the information on UNSW's Special Consideration page.

II. Administrative matters and links

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Attendance
- UNSW Email Address
- Special Consideration
- Exams
- Approved Calculators
- Academic Honesty and Plagiarism
- Equitable Learning Services

III. Equity and diversity

Those students who have a disability that requires some adjustment in their teaching or learning environment are encouraged to discuss their study needs with the course convener prior to, or at the commencement of, their course, or with the Equity Officer (Disability) in the Equitable Learning Services. Issues to be discussed may include access to materials, signers or note-takers, the provision of services and additional exam and assessment arrangements. Early notification is essential to enable any necessary adjustments to be made.

IV. Professional Outcomes and Program Design

Students are able to review the relevant professional outcomes and program designs for their streams by going to the following link: https://www.unsw.edu.au/engineering/student-life/student-resources/program-design.

Note: This course outline sets out the description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle or your primary learning management system (LMS) should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline/Moodle/LMS, the description in the Course Outline/Moodle/LMS applies.

Academic Honesty and Plagarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. *Plagiarism at UNSW is defined as using the words or ideas of others and passing them off as your own.*

Plagiarism is a type of intellectual theft. It can take many forms, from deliberate cheating to accidentally copying from a source without acknowledgement. UNSW has produced a website with a wealth of resources to support students to understand and avoid plagiarism, visit: student.unsw.edu.au/plagiarism. The Learning Centre assists students with understanding academic integrity and how not to plagiarise. They also hold workshops and can help students one-on-one.

You are also reminded that careful time management is an important part of study and one of the identified causes of plagiarism is poor time management. Students should allow sufficient time for research, drafting and the proper referencing of sources in preparing all assessment tasks.

Repeated plagiarism (even in first year), plagiarism after first year, or serious instances, may also be investigated under the Student Misconduct Procedures. The penalties under the procedures can include a reduction in marks, failing a course or for the most serious matters (like plagiarism in an honours thesis or contract cheating) even suspension from the university. The Student Misconduct Procedures are available here:

www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf

Submission of Assessment Tasks

Work submitted late without an approved extension by the course coordinator or delegated authority is subject to a late penalty of five percent (5%) of the maximum mark possible for that assessment item, per calendar day.

The late penalty is applied per calendar day (including weekends and public holidays) that the assessment is overdue. There is no pro-rata of the late penalty for submissions made part way through a day. This is for all assessments where a penalty applies.

Work submitted after five days (120 hours) will not be accepted and a mark of zero will be awarded for that assessment item.

For some assessment items, a late penalty may not be appropriate. These will be clearly indicated in the course outline, and such assessments will receive a mark of zero if not completed by the specified date. Examples include:

- Weekly online tests or laboratory work worth a small proportion of the subject mark;
- Exams, peer feedback and team evaluation surveys;

- Online quizzes where answers are released to students on completion;
- Professional assessment tasks, where the intention is to create an authentic assessment that has an absolute submission date; and,
- Pass/Fail assessment tasks.

Faculty-specific Information

Engineering Student Support Services – The Nucleus - enrolment, progression checks, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries e.g. admissions, fees, programs, credit transfer

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

School-specific Information

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Use of AI for assessments

Your work must be your own. If you use AI in the writing of your assessment, you must acknowledge this and your submission must be substantially your own work. More information can be found on this website.

Workplace Health & Safety (WHS)

WHS for students and staff is of utmost priority. Most courses involve laboratory work. You must follow the rules about conduct in the laboratory. About COVID-19, advice can be found on this website.

School Contact Information

Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Student Support Enquiries

For enrolment and progression enquiries please contact Student Services

Web

Electrical Engineering Homepage