UNSW Course Outline

ELEC9701 Mixed Signal Microelectronic Design - 2024

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General Course Information

Course Code : ELEC9701
Year : 2024
Term : Term 3
Teaching Period : T3
Is a multi-term course? : No
Faculty : Faculty of Engineering
Academic Unit : School of Electrical Engineering & Telecommunications
Delivery Mode : In Person
Delivery Format : Standard
Delivery Location : Kensington
Campus : Sydney
Study Level : Postgraduate
Units of Credit : 6

Useful Links

Handbook Class Timetable

Course Details & Outcomes

Course Description

Microelectronics or integrated electronics are the miniaturised electronic circuits that make up Integrated Circuits (ICs) such as microprocessors, Field-Programmable Gate Arrays, Flash-memories, operational amplifiers, analogue-to-digital converters, SoCs, ASICs and many other

devices. Most ICs today are implemented in various flavours of CMOS technology which is the focus of this course. The ability to use a large number of components at a relatively low cost and the ability to match components accurately on-chip makes the design of integrated circuits and systems different from a similar design using discrete components. Mixed Signal Microelectronics Design is a broad-based, more advanced IC design course, which provides the students with analogue and digital circuits and design techniques required to implement mixed-signal integrated circuits with good performance and enables them to keep up to date with contemporary design methods.

Course content includes: Advanced fabrication and special IC processes (high-voltage, silicon-on-insulator, nano-scale CMOS); Technology scaling, process variation, device matching, layout for matching; Parasitics, gate leakage and wire models; Advanced transistor modelling, velocity saturation, sub-threshold operation; High-frequency analysis; Advanced cascodes and amplifier design, fully-differential circuits, common-mode feedback, rail-to-rail circuits, power outputs, biasing and references; Trimming; Active filters, switched capacitor circuits, transconductors and Gm-C filters; Non-linear circuits; Schmitt triggers and charge pumps; Sigma-delta converters and ADC calibration; Logic effort; Advanced logic families, rationed logic, special functions, oscillators, PLLs, TDCs; Dynamic logic and registers, TSP registers, timing, clock distribution, self-timed systems; Assembly techniques and packaging, latch-up, I/O design, ESD, shielding, interference and mixed analogue-digital design; Current research and reading research papers.

Course Aims

The course builds on knowledge gained in the undergraduate electronics curriculum in general and the microelectronics design and technology course in particular, providing students with advanced electronic circuit design skills.

The course aims to enable the student to do analysis and design of integrated circuits of good performance, and to equip the student to do self-guided, continuing learning in the advancing field of microelectronics.

Relationship to Other Courses

This is a graduate level course in the School of Electrical Engineering and Telecommunications. It is offered to students following a post-graduate program at the university and is a requirement for students doing research in the area of integrated circuit design.

Pre-requisites and Assumed Knowledge

The course builds on the integrated circuit design foundations given in the undergraduate course ELEC4602, Microelectronics Design and Technology. ELEC4602 is a pre-requisite for this course, but the two courses can be followed concurrently. It is essential that you have good working knowledge of circuit theory, basic analogue and digital electronics, and basic signal analysis as covered in the courses ELEC1112, Electrical Circuits, ELEC2133, Analogue Electronics, ELEC2141, Digital Circuit Design, ELEC2134, Circuits and Signals, and ELEC3106, Electronics which is the pre-requisite course for ELEC4602. It is finally assumed that you are proficient in the use of personal computers and are familiar with SPICE-type circuit simulation.

Course Learning Outcomes

Course Learning Outcomes
CLO1 : Recognise capabilities and limitations of advanced microelectronic (or IC) technologies
CLO2 : Apply advanced circuit models of IC components
CLO3 : Analyse advanced analogue and digital microelectronic circuits
CLO4 : Design analogue, digital and mixed microelectronic circuits
CLO5 : Critically read and present technical research papers
CLO6 : Keep up-to-date with future technological development in the field

Course Learning Outcomes	Assessment Item
CLO1 : Recognise capabilities and limitations of advanced microelectronic (or IC) technologies	• Discussion classes • Quizzes
CLO2 : Apply advanced circuit models of IC components	• Final Examination • Quizzes
CLO3 : Analyse advanced analogue and digital microelectronic circuits	• Design Task • Final Examination • Quizzes
CLO4 : Design analogue, digital and mixed microelectronic circuits	• Design Task • Final Examination
CLO5 : Critically read and present technical research papers	• Discussion classes
CLO6 : Keep up-to-date with future technological development in the field	• Discussion classes • Final Examination

Learning and Teaching Technologies

Moodle - Learning Management System | Course website | Echo 360

Learning and Teaching in this course

Delivery Mode

- Formal lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations and individually targeted illustrations to aid your understanding.
- Self-guided tutorials, which allow for exercises in problem solving and allow time for you to resolve in-depth problems for quantitative understanding of the lecture material.
- Discussion classes, which practice critical analysis and detailed discussion of design engineer's primary source of knowledge for keeping abreast a rapidly developing field: research papers.
- A design task, which draws together theoretical and practical design aspects in an open-ended realistic design problem, reinforcing the course material.

Learning in this Course

You are expected to attend all lectures, discussion classes, and quizzes, in order to maximise your learning. You must prepare well for discussion classes and your participation will be assessed. You should read relevant sections of the recommended texts. Lecture notes will not be given: reading and reflecting on the recommended texts and identify critical parts with the aid of the lectures is an essential component of this course. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW assumes that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Lectures

During the lectures technology capabilities and design issues are discussed and theoretical aspects of IC design and technology are presented. Numerous examples of analogue and digital integrated circuit functions are discussed in order to convey a qualitative understanding of circuit operations. You are encouraged to actively engage in the lectures to facilitate two-way communication and enhance learning. The lectures aim to support you in analysing and designing integrated circuits, and to help you appreciate the capabilities of IC technologies.

Self-guided Tutorials

You should attempt all of the problem sheet questions provided. Group learning is encouraged. Answers to these questions may be discussed during the consultation time.

Discussion Classes

Technical papers are the researcher's and practicing design engineer's primary source of knowledge for keeping abreast a rapidly developing field. During the discussion classes, and on-line prior to classes, students and lecturer will discuss papers from technical journals; from week 2 onwards, students will take turns to lead these discussions. The discussion classes thus provide you with exercises in critically analysing and reflective learning from technical papers; they also provide you with exercise in oral communication and with advanced, contemporary discipline knowledge. The discussion classes aim to prepare you for future self-guided learning. You are required to participate in the discussion classes.

Design Task

The design task aims to draw together theoretical and practical design aspects in an open-ended realistic design problem. You will design an integrated circuit meeting given specifications, use the CAD tools to verify the circuit operation and write a report in the form of a technical paper documenting your design. The design task provide and test engineering creativity, open-ended problem solving skills, communication skills and general understanding of the course content. You may use the CAD tools in room G17-202/G17-217 for this task.

Other Professional Outcomes

Relationship to Engineers Australia Stage 1 competencies:

The Course Learning Outcomes (LOs) contribute to the Engineers Australia (National Accreditation Body) Stage I competencies as outlined below

Engineers Australia (EA), Professional Engineer Stage 1 Competencies

PE1: Knowledge and Skill Base:
PE1.1 Comprehensive, theory-based **understanding of underpinning fundamentals**: LO 3
PE1.2 Conceptual understanding of underpinning maths, **analysis**, statistics, **computing**: LO 2, 3
PE1.3 In-depth understanding of specialist bodies of **knowledge**: LO 1, 2, 3, 4, 5, 6
PE1.4 Discernment of knowledge development and research directions: LO 1, 5, 6
PE1.5 Knowledge of **engineering design** practice: LO 3, 4
PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice: NA

PE2: Engineering Application Ability:
PE2.1 Application of established engineering methods to **complex problem solving**: LO 3, 4

PE2.2 Fluent **application of engineering techniques**, tools and resources: LO 3, 4, 5, 6
PE2.3 Application of systematic engineering synthesis and design processes: LO 3, 4
PE2.4 Application of systematic approaches to the conduct and management of engineering projects: NA

PE3: Professional and Personal Attributes:
PE3.1 Ethical conduct and professional accountability: NA
PE3.2 Effective **oral and written communication** (professional and lay domains): LO 4, 5
PE3.3 **Creative, innovative** and pro-active demeanour: LO 4, 5
PE3.4 Professional use and management of information: LO 4, 5
PE3.5 Orderly management of **self, and professional conduct**: LO 4, 5
PE3.6 Effective team membership and team leadership: NA

This course is also designed to provide the course learning outcomes which arise from targeted graduate capabilities. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (also listed below).

Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing scholars who have a deep understanding of their discipline, through discussion classes and design task.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems, through tutorial exercises and design task.
- Developing capable independent and collaborative enquiry, through discussion classes.
- Developing digital and information literacy and lifelong learning skills, through lectures, class preparations and report writing.
- Developing the capability of effective communication, through report writing.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through the design task.

https://www.unsw.edu.au/engineering/student-life/student-resources/program-design

Assessments

Assessment Structure

Assessment Item	Weight	Relevant Dates
Discussion classes Assessment Format: Individual	15%	
Quizzes Assessment Format: Individual	10%	
Final Examination Assessment Format: Individual	60%	
Design Task Assessment Format: Group	15%	

Assessment Details

Discussion classes

Assessment Overview

Students' involvement and engagement in the discussion classes throughout the term will be marked. A rubric will be used for marking and feedback given to students online.

Course Learning Outcomes

- CLO1 : Recognise capabilities and limitations of advanced microelectronic (or IC) technologies
- CLO5 : Critically read and present technical research papers
- CLO6 : Keep up-to-date with future technological development in the field

Detailed Assessment Description

Participation and engagement in the discussion classes are assessed in order to ensure that the students are able to critically read and learn from technical papers, and communicate their findings to the class. Students must post discussion items (questions, answers, observations, etc) related to each weeks discussion paper on Moodle prior to each discussion class.

Assignment submission Turnitin type

Not Applicable

Generative AI Permission Level

Simple Editing Assistance

In completing this assessment, you are permitted to use standard editing and referencing functions in the software you use to complete your assessment. These functions are described below. You must not use any functions that generate or paraphrase passages of text or other media, whether based on your own work or not.
If your Convenor has concerns that your submission contains passages of AI-generated text or media, you may be asked to account for your work. If you are unable to satisfactorily demonstrate your understanding of your submission you may be referred to UNSW Conduct & Integrity Office for investigation for academic misconduct and possible penalties.
For more information on Generative AI and permitted use please see here.

Quizzes

Assessment Overview

Two in-class quizzes will be held during lecture time. Marks will be assigned according to the correct fraction of the response. Verbal class-wide feedback will be given during lectures.

Course Learning Outcomes

- CLO1 : Recognise capabilities and limitations of advanced microelectronic (or IC) technologies
- CLO2 : Apply advanced circuit models of IC components
- CLO3 : Analyse advanced analogue and digital microelectronic circuits

Detailed Assessment Description

There are two quizzes held during the lecture time through the term. These are designed to give early feedback on your progress through the theoretical components of the course and test your general understanding of the course material. Questions will be drawn from course material covered in the three-four weeks prior to each quiz.

Assignment submission Turnitin type

Not Applicable

Generative AI Permission Level

Simple Editing Assistance

In completing this assessment, you are permitted to use standard editing and referencing functions in the software you use to complete your assessment. These functions are described below. You must not use any functions that generate or paraphrase passages of text or other media, whether based on your own work or not.
If your Convenor has concerns that your submission contains passages of AI-generated text or media, you may be asked to account for your work. If you are unable to satisfactorily demonstrate your understanding of your submission you may be referred to UNSW Conduct & Integrity Office for investigation for academic misconduct and possible penalties.
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Final Examination

Assessment Overview

The examination is a 2-hour open-book examination. Marks will be assigned according to the correct fraction of the response.

Course Learning Outcomes

- CLO2 : Apply advanced circuit models of IC components
- CLO3 : Analyse advanced analogue and digital microelectronic circuits
- CLO4 : Design analogue, digital and mixed microelectronic circuits
- CLO6 : Keep up-to-date with future technological development in the field

Detailed Assessment Description

The exam in this course is an open-book 2 hour (nominal) written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including discussion classes), unless specifically indicated otherwise by the lecturer.

Hurdle rules

An examination mark of at least 45% is required to pass the course.

Generative AI Permission Level

No Assistance

This assessment is designed for you to complete without the use of any generative AI. You are not permitted to use any generative AI tools, software or service to search for or generate information or answers.
For more information on Generative AI and permitted use please see here.

Design Task

Assessment Overview

The design task will be carried out in open computer labs using a specified process design kit. The work will be assessed on a submitted paper-style report. A rubric will be used for marking and feedback given to each group online.

Course Learning Outcomes

- CLO3 : Analyse advanced analogue and digital microelectronic circuits
- CLO4 : Design analogue, digital and mixed microelectronic circuits

Detailed Assessment Description

The design task is assessed to test your ability to design an integrated circuit and communicate its key features in a professional manner, thus also demonstrating your appreciation of the technology, your ability to use appropriate models and simulations, and your ability to conduct suitable analysis to aid in the design.

You should maintain a lab book and must record suitable screen shots or print-outs as documentation for your work. The design and verification work must be documented in a report which is due Monday the due week listed in the course schedule. The report must take the form of a four-page technical paper (IEEE format). Each report must be uploaded as a .pdf file (no other format accepted) on the course Moodle site.

Assignment submission Turnitin type

Not Applicable

Generative AI Permission Level

Simple Editing Assistance

In completing this assessment, you are permitted to use standard editing and referencing functions in the software you use to complete your assessment. These functions are described below. You must not use any functions that generate or paraphrase passages of text or other media, whether based on your own work or not.
If your Convenor has concerns that your submission contains passages of AI-generated text or

media, you may be asked to account for your work. If you are unable to satisfactorily demonstrate your understanding of your submission you may be referred to UNSW Conduct & Integrity Office for investigation for academic misconduct and possible penalties.
For more information on Generative AI and permitted use please see here.

General Assessment Information

Grading Basis

Standard

Course Schedule

Teaching Week/Module	Activity Type	Content
Week 1 : 9 September - 15 September	Lecture	Advanced CMOS technologies and components.
	Reading	Notes.
	Other	Self-directed: technology scaling. JB ch. 6, Notes.
	Seminar	Discussion topic 0: integrated technology/devices.
Week 2 : 16 September - 22 September	Lecture	Process variations, parasitics, wire models, non-linear capacitances.
	Reading	JB ch. 3, 4, 5, Notes.
	Other	Self-directed: layout matching. JB ch. 5, 20.
	Seminar	Discussion topic 1: integrated technology/devices.
Week 3 : 23 September - 29 September	Lecture	Advanced MOS models and matching models.
	Reading	JB ch. 9, 10, Notes.
	Seminar	Discussion topic 2: integrated technology/devices.
Week 4 : 30 September - 6 October	Lecture	Advanced cascodes and HF analysis.
	Reading	JB ch. 20, 21, 22.
	Seminar	Discussion topic 3: integrated analogue circuits.
	Assessment	Quiz 1.
Week 5 : 7 October - 13 October	Lecture	Advanced operational amplifier design.
	Reading	JB ch. 24, 26, 23.
	Seminar	Discussion topic 4: integrated analogue circuits.
Week 6 : 14 October - 20 October	Lecture	Active filters and non-linear circuits.
	Reading	JB ch. 25, 27, Notes.
	Seminar	Discussion topic 5: integrated analogue circuits.
Week 7 : 21 October - 27 October	Lecture	Advanced A/D converter design.
	Reading	JB ch. 29, Notes.
	Seminar	Discussion topic 6: integrated analogue circuits.
Week 8 : 28 October - 3 November	Lecture	Advanced logic, sizing, special functions, PLLs.
	Reading	JB ch. 11, 12, 18, 19, Notes.
	Other	Self-directed: logic effort. Notes.
	Seminar	Discussion topic 7: integrated digital circuits.
	Assessment	Quiz 2.
Week 9 : 4 November - 10 November	Lecture	Dynamic logic, registers and timing.
	Reading	JB ch. 13, 14, Notes.
	Seminar	Discussion topic 8: integrated digital circuits.
Week 10 : 11 November - 17 November	Lecture	Packaging, I/O and mixed-signal design.
	Reading	JB ch. 1, 3, 4, Notes.
	Seminar	Discussion topic 9: integrated digital circuits.
	Assessment	Project Report due.

Attendance Requirements

Students are strongly encouraged to attend all classes and review lecture recordings.

Course Resources

Prescribed Resources

Textbook

- R. J. Baker, CMOS Circuit Design, Layout, and Simulation. Wiley Interscience, 3rd/4th ed., 2010/2019.

On-line resources

Moodle: As a part of the teaching component, Moodle will be used to upload project reports and host forums, including a discussion classes forum. Moodle will also be used to dissiminate discussion papers. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

Course webpage: The course webpage is used to disseminate course material, including design brief, past assessment and examination papers, and some lecture notes: https://subjects.ee.unsw.edu.au/elec9701.

CAD resources

Students can access the industry standard Cadence design suite for the work in this course. The CAD tools are located in the computer laboratories G17-202 and G17-217. Students must remember to copy their work on to their own storage device before they logout as all data will otherwise be lost. For specific details on how to log on, see the course web page. Students who have not followed ELEC4602 are encouraged to go through the ELEC4602 laboratory exercises in order to familiarise themselves with the CAD tools.

Remote computer access

Computers in rooms G17-202 and G17-217 can be accessed remotely via https://myaccessunsw.cloud.com/Citrix/StoreWeb/#/desktops/all. Click on DESKTOPS and subsequenty ELECENG-LABPC-G17-Rm202 or ELECENG-LABPC-G17-Rm217 to start a Citrix remote session on a computer in one of those rooms. Students must have the Citrix Workspace player (download from https://www.citrix.com/en-au/downloads/workspace-app/) installed on

their own computer.

Recommended Resources

Reference books

- T. C. Carusone, D. A. Johns and K. W. Martin, Analog Integrated Circuit Design. Wiley and Sons Inc., 2nd ed., 2012.
- T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press, 1998.
- N. Weste and D. Harris, CMOS VLSI Design: a Circuits and Systems Perspective. Addison-Wesley, 3rd ed., 2005.

Course Evaluation and Development

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course, and in our efforts to provide a rich and meaningful learning experience, we have changed the weighting of in-term assessments, increased the number of tutorial exercises, released summary slides, and commenced the use of on-line discussion tools.

Staff Details

Position	Name	Email	Location	Phone	Availability	Equitable Learning Services Contact	Primary Contact
Convenor	Torsten Lehmann		G17-343	93855374	Wednesdays 4-5pm	Yes	Yes

Other Useful Information

Academic Information

I. Special consideration and supplementary assessment

If you have experienced an illness or misadventure beyond your control that will interfere with your assessment performance, you are eligible to apply for Special Consideration prior to, or within 3 working days of, submitting an assessment or sitting an exam.

Please note that UNSW has a Fit to Sit rule, which means that if you sit an exam, you are

declaring yourself fit enough to do so and cannot later apply for Special Consideration.

For details of applying for Special Consideration and conditions for the award of supplementary assessment, please see the information on UNSW's Special Consideration page.

II. Administrative matters and links

All students are expected to read and be familiar with UNSW guidelines and polices. In particular, students should be familiar with the following:

- Attendance
- UNSW Email Address
- Special Consideration
- Exams
- Approved Calculators
- Academic Honesty and Plagiarism
- Equitable Learning Services

III. Equity and diversity

Those students who have a disability that requires some adjustment in their teaching or learning environment are encouraged to discuss their study needs with the course convener prior to, or at the commencement of, their course, or with the Equity Officer (Disability) in the Equitable Learning Services. Issues to be discussed may include access to materials, signers or note-takers, the provision of services and additional exam and assessment arrangements. Early notification is essential to enable any necessary adjustments to be made.

IV. Professional Outcomes and Program Design

Students are able to review the relevant professional outcomes and program designs for their streams by going to the following link: https://www.unsw.edu.au/engineering/student-life/student-resources/program-design.

Note: This course outline sets out the description of classes at the date the Course Outline is published. The nature of classes may change during the Term after the Course Outline is published. Moodle or your primary learning management system (LMS) should be consulted for the up-to-date class descriptions. If there is any inconsistency in the description of activities between the University timetable and the Course Outline/Moodle/LMS, the description in the Course Outline/Moodle/LMS applies.

Academic Honesty and Plagarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. *Plagiarism at UNSW is defined as using the words or ideas of others and passing them off as your own.*

Plagiarism is a type of intellectual theft. It can take many forms, from deliberate cheating to accidentally copying from a source without acknowledgement. UNSW has produced a website with a wealth of resources to support students to understand and avoid plagiarism, visit: student.unsw.edu.au/plagiarism. The Learning Centre assists students with understanding academic integrity and how not to plagiarise. They also hold workshops and can help students one-on-one.

You are also reminded that careful time management is an important part of study and one of the identified causes of plagiarism is poor time management. Students should allow sufficient time for research, drafting and the proper referencing of sources in preparing all assessment tasks.

Repeated plagiarism (even in first year), plagiarism after first year, or serious instances, may also be investigated under the Student Misconduct Procedures. The penalties under the procedures can include a reduction in marks, failing a course or for the most serious matters (like plagiarism in an honours thesis or contract cheating) even suspension from the university. The Student Misconduct Procedures are available here:

www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf

Submission of Assessment Tasks

Work submitted late without an approved extension by the course coordinator or delegated authority is subject to a late penalty of five percent (5%) of the maximum mark possible for that assessment item, per calendar day.

The late penalty is applied per calendar day (including weekends and public holidays) that the assessment is overdue. There is no pro-rata of the late penalty for submissions made part way through a day. This is for all assessments where a penalty applies.

Work submitted after five days (120 hours) will not be accepted and a mark of zero will be

awarded for that assessment item.

For some assessment items, a late penalty may not be appropriate. These will be clearly indicated in the course outline, and such assessments will receive a mark of zero if not completed by the specified date. Examples include:

- Weekly online tests or laboratory work worth a small proportion of the subject mark;
- Exams, peer feedback and team evaluation surveys;
- Online quizzes where answers are released to students on completion;
- Professional assessment tasks, where the intention is to create an authentic assessment that has an absolute submission date; and,
- Pass/Fail assessment tasks.

Faculty-specific Information

Engineering Student Support Services – The Nucleus - enrolment, progression checks, clash requests, course issues or program-related queries

Engineering Industrial Training – Industrial training questions

UNSW Study Abroad – study abroad student enquiries (for inbound students)

UNSW Exchange – student exchange enquiries (for inbound students)

UNSW Future Students – potential student enquiries e.g. admissions, fees, programs, credit transfer

Phone

(+61 2) 9385 8500 – Nucleus Student Hub

(+61 2) 9385 7661 – Engineering Industrial Training

(+61 2) 9385 3179 – UNSW Study Abroad and UNSW Exchange (for inbound students)

School-specific Information

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and

students may be asked to leave the class.

Use of AI for assessments

Your work must be your own. If you use AI in the writing of your assessment, you must acknowledge this and your submission must be substantially your own work. More information can be found on this website.

Workplace Health & Safety (WHS)

WHS for students and staff is of utmost priority. Most courses involve laboratory work. You must follow the rules about conduct in the laboratory. About COVID-19, advice can be found on this website.

School Contact Information

Consultations: Lecturer consultation times will be advised during the first lecture. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC/TELExxxx in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Student Support Enquiries

For enrolment and progression enquiries please contact Student Services

Web

Electrical Engineering Homepage