LAB 11: AC-DC Power Supply Design

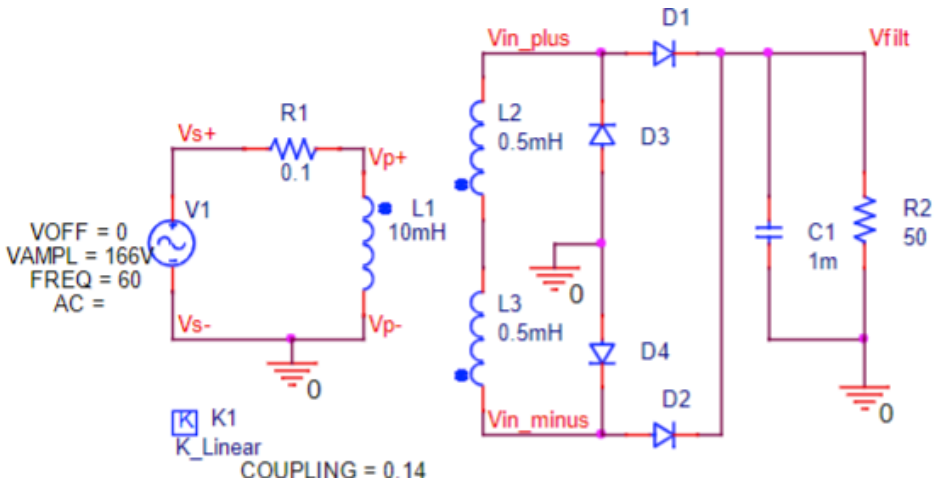
Contents

Executive Summary: The output plots of the AC to DC power supply circuit configurations were analyzed, with the value of the ripple voltage decreasing steadily with each circuit configuration. In the lab portion, transformer only configuration had the greatest peak to peak value at 19Vpp, resembling that of the input AC wave, while the filter, Zener, and BJT configuration was able to successfully reduce the Vripple down the most, to 4.9mV, with simulations of the same circuits providing similar results.

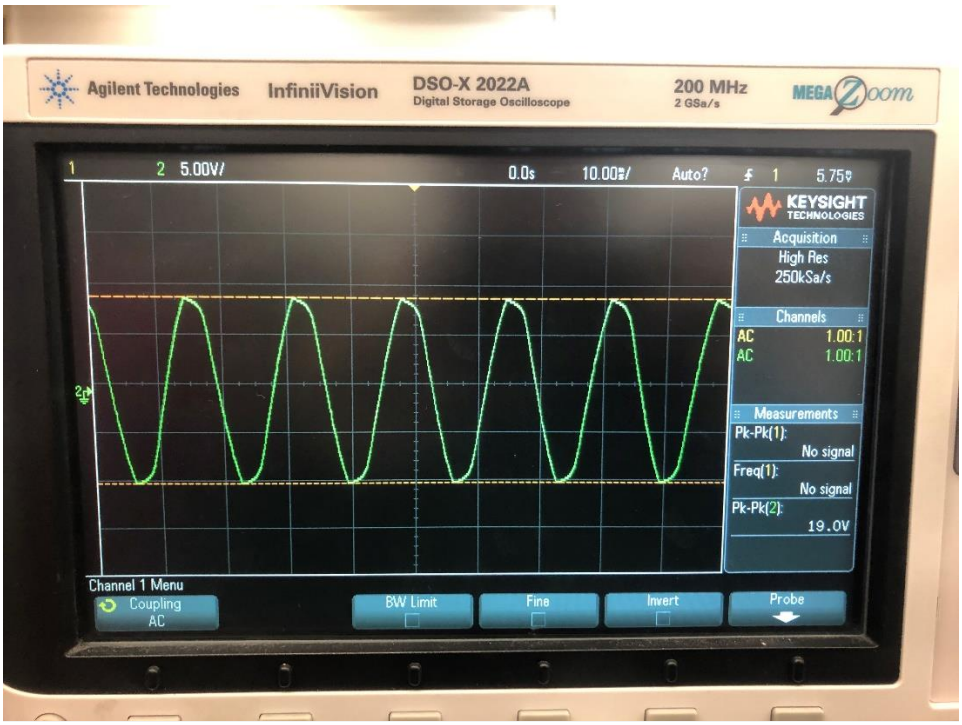
Objective: To design a simple regulated AC-DC Zener diode based power supply that minimizes the output ripple voltage. The goal in this experiment is to have the AC Vripple < 10 mV, providing 100mA into the load.

AC-DC Stage 1, Filter (LAB)

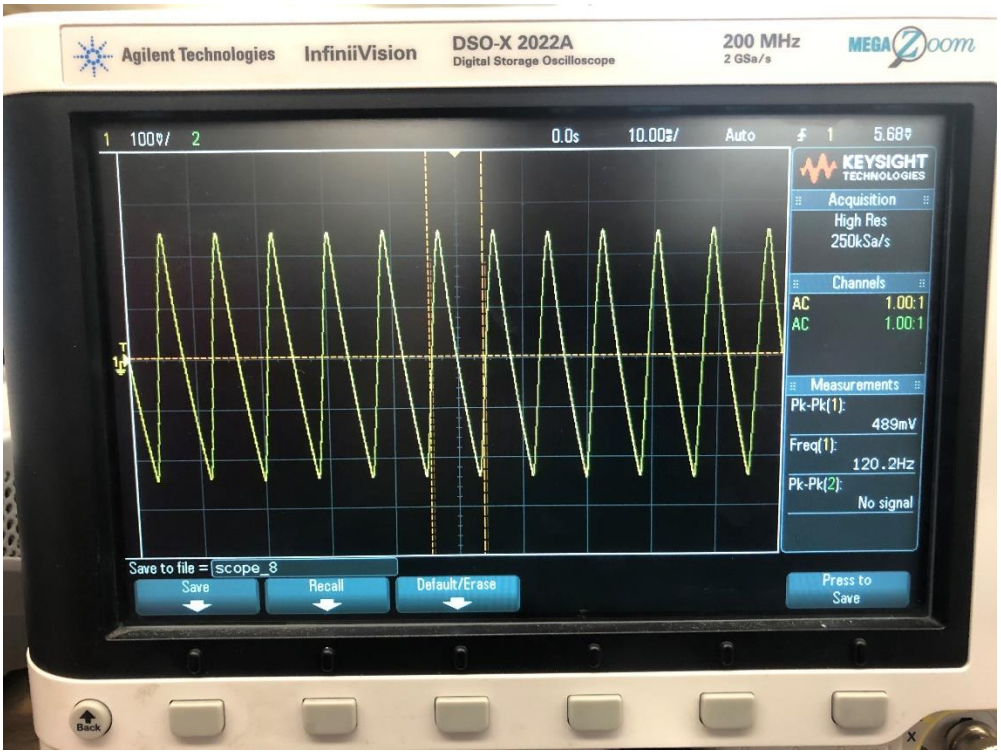
Schematic



PSpice Generated Plots



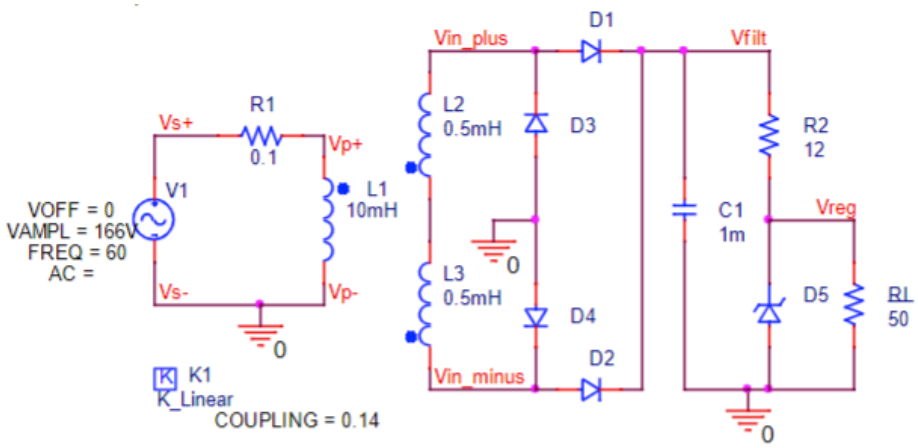
Picture of Vinplus/Vinminus = 19Vpp , the voltage after the center tap transformer has been applied.



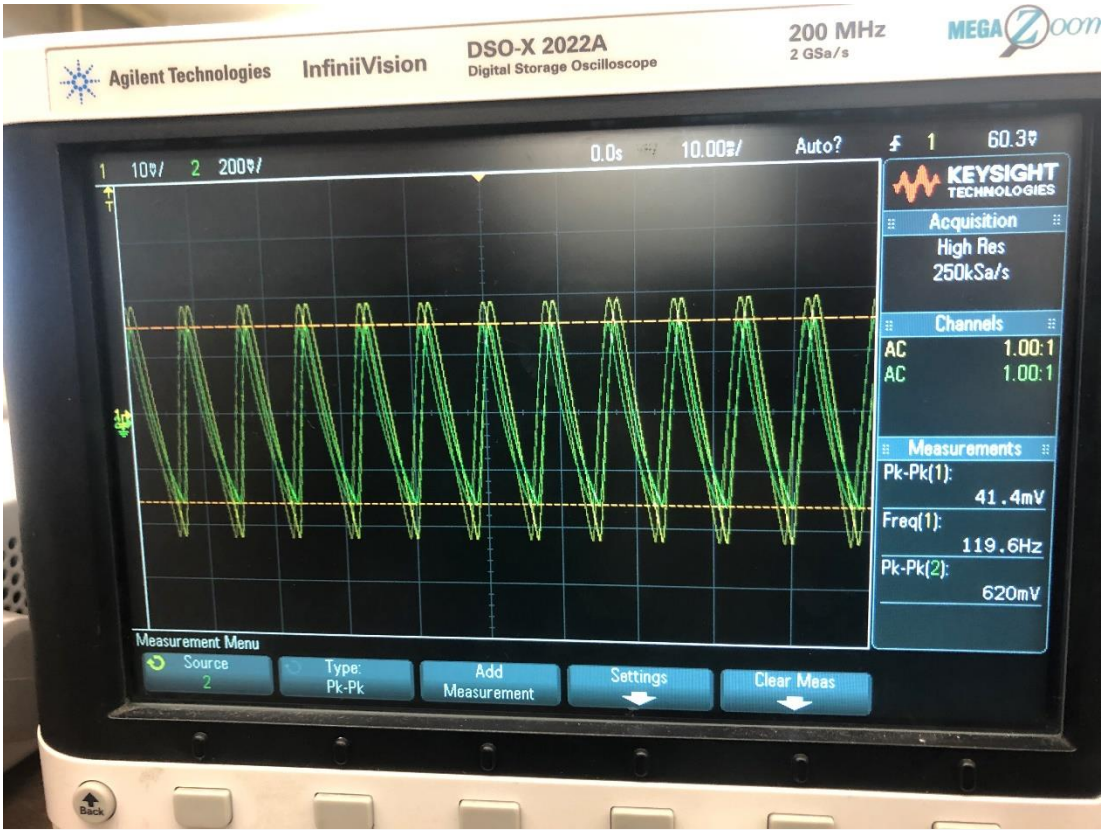
Vfilt=489mVpp, the waveform is currently unregulated, but the capacitor's discharge and charge behavior allow the input voltage (19Vpp) to constantly refresh to its peak as determined by the time constant T=RC. For this simulation we used C=1mF, R =50ohm, T=50*1(10^-3)=0.05s or 50ms. Period is T=1/f=1/120=0.0083=~10ms. So, whereas the voltage would decay to 0 in about 4 time constants time (200ms), it is instead refreshed every 10ms. The capacitor decay rate is V(t)=Vi(e^(-t/RC)).

AC-DC Stage 2, Filter, Zener (LAB)

Schematic



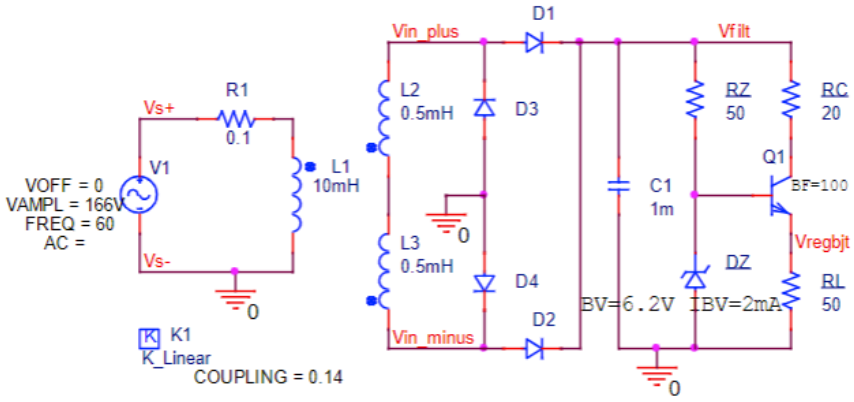
PSpice Generated Plots



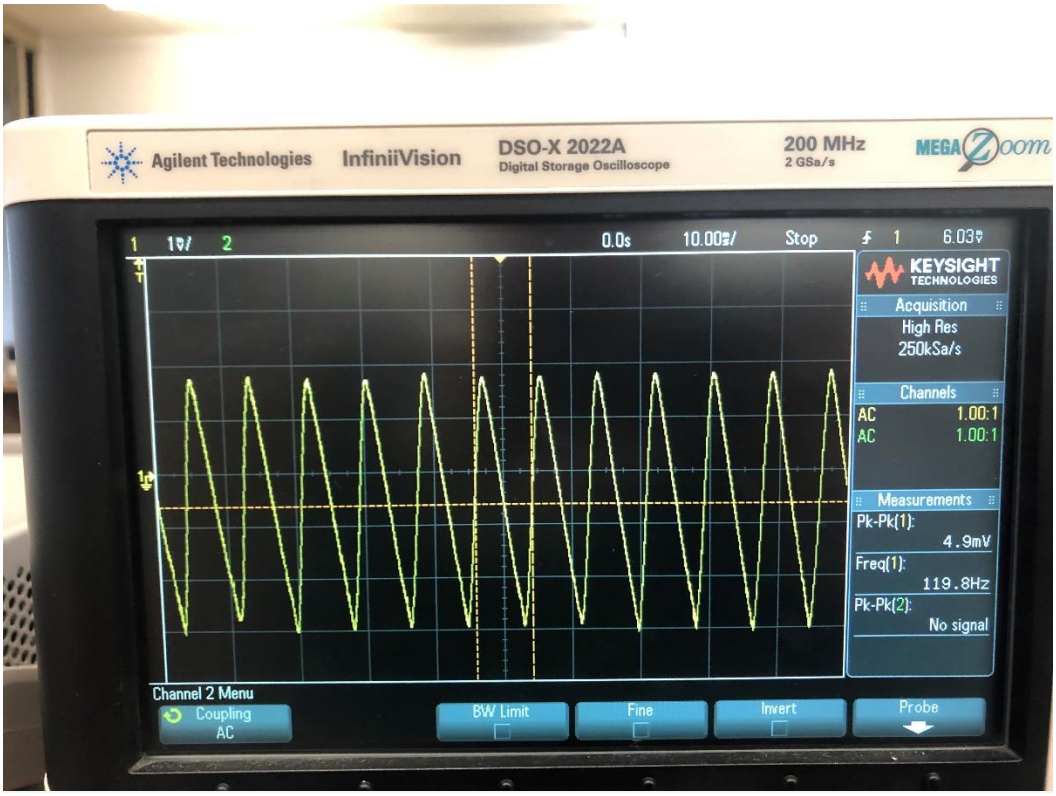
Note that the picture is a bit blurry, but the correct waveform is shown. The 120Hz frequency and 620mVpp of the Vreg is shown alongside the 41.4mVpp of Vfilt, the voltage before Zener regulation.

AC-DC Stage 3, Filter, Zener, BJT (LAB)

Schematic



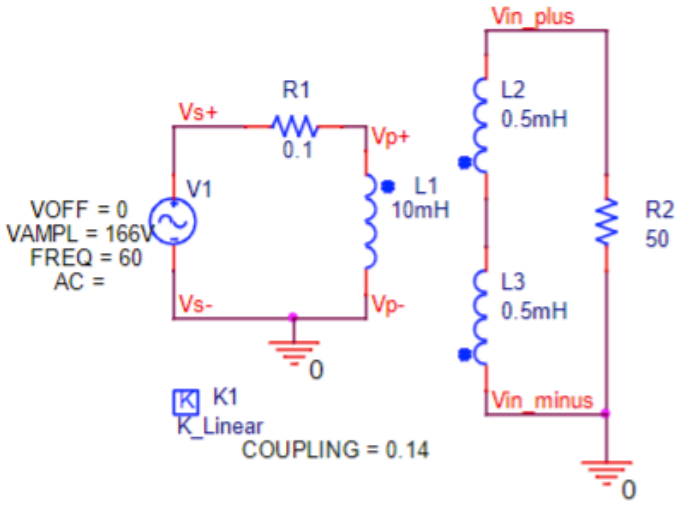
PSpice Generated Plots



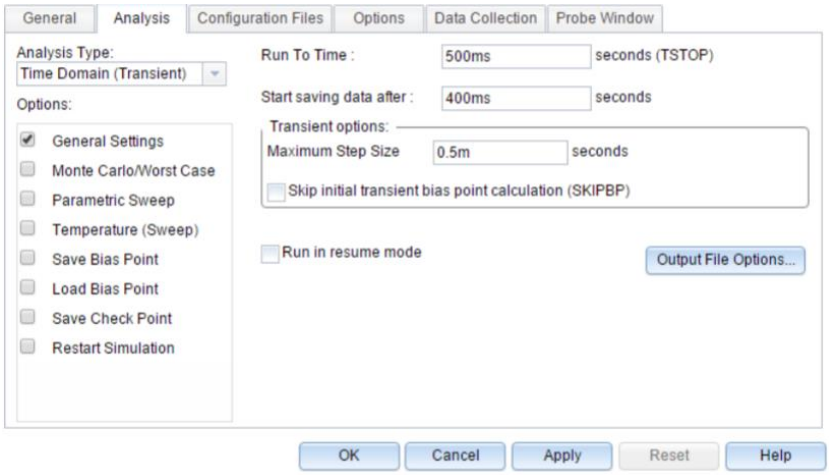
Fully regulated voltage Vregbjt is much lower than the Vreg of the filter & zener only (Stage 2) configuration. The 50 ohm resistor ensures that Ib is small compared to Ic, which has a 20 ohm resistor. The small Ib is also Iz flowing into the Zener diode, and because of the V regulation of the Zener, we are placed further UP the Zener breakdown voltage line in the negative x axis. Therefore, there is less variance or ripple in our Vz when compared to the stage 2 configuration.

AC-DC Stage 1, Transformer (SIM)

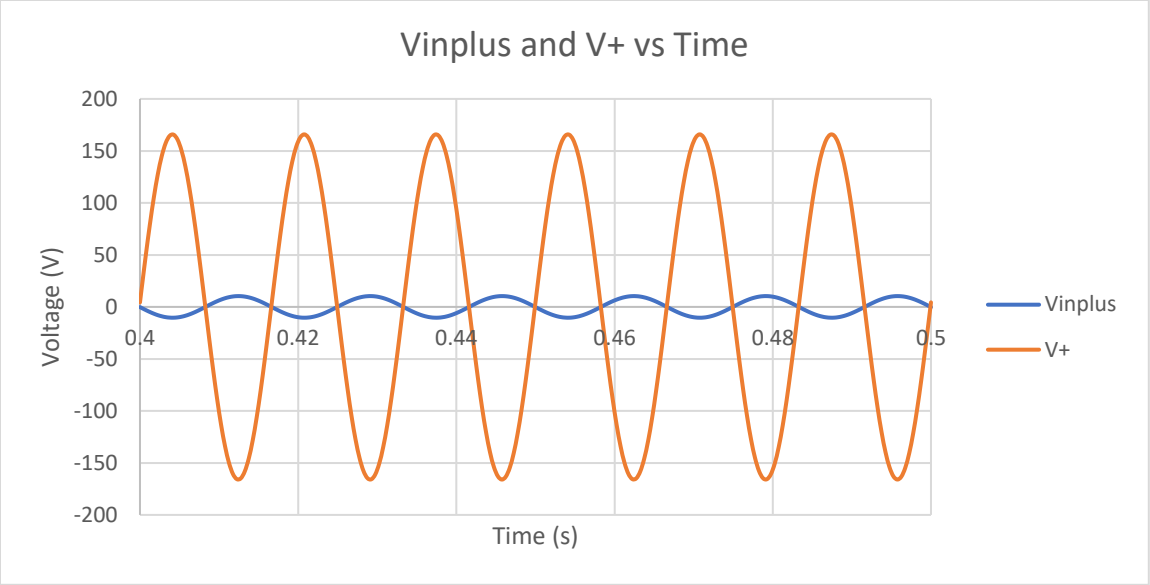
Schematic



Simulation Profile



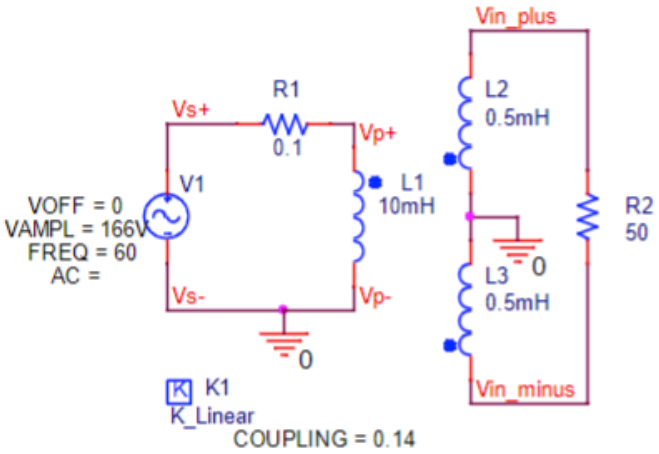
Excel Generated Plots



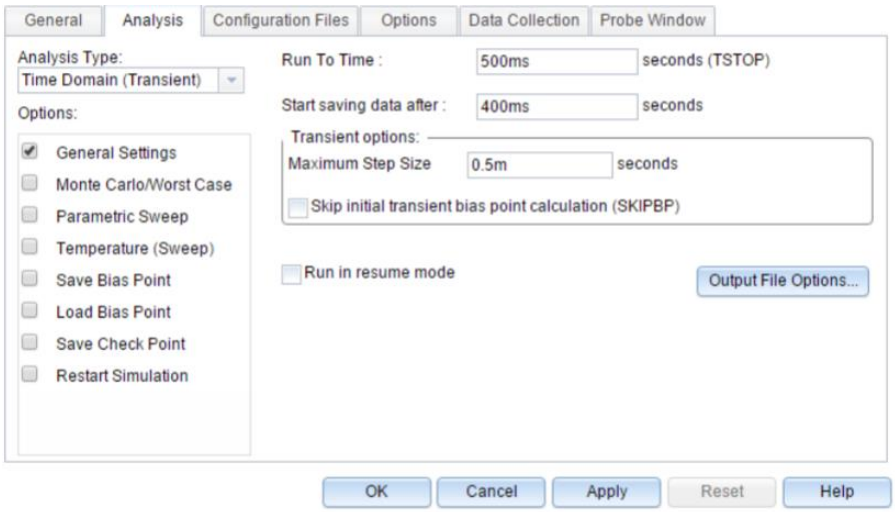
The transformer successfully converts the large 166Vp AC input voltage to ~6Vp.

AC-DC Stage 1.5, Transformer/GND (SIM)

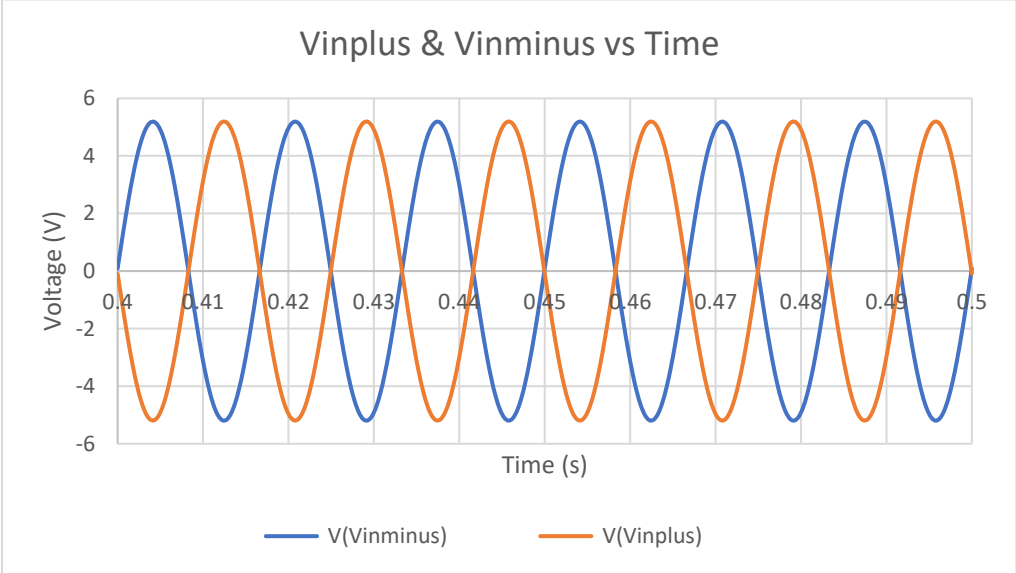
Schematic



Simulation Profile



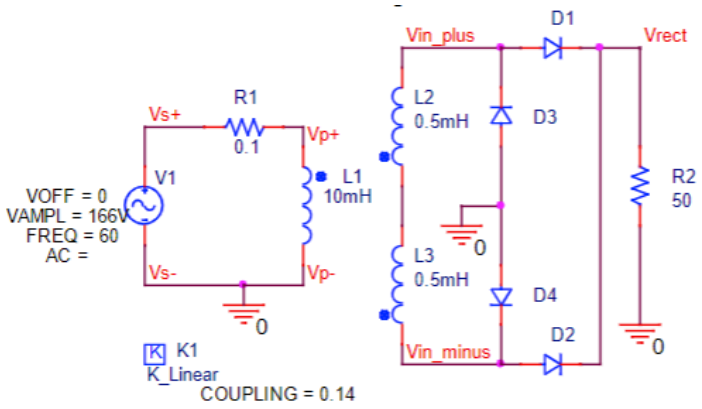
Excel Generated Plots



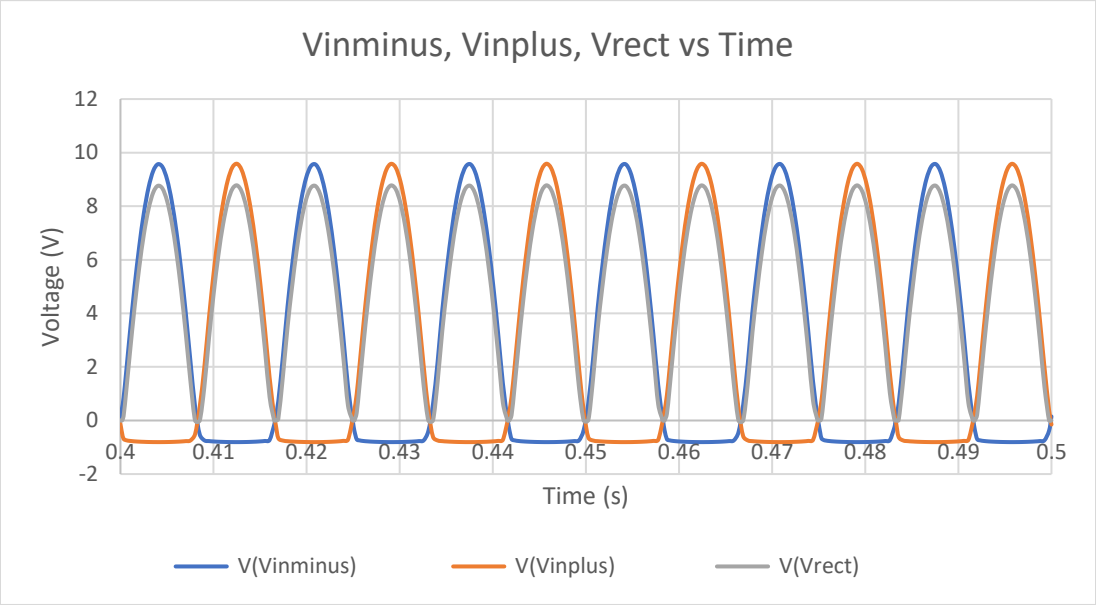
Vinplus and Vinminus swings between the max and min values of the rectified output voltage, 180 degrees out of phase.

AC-DC Stage 2, Bridge Rectifier (SIM)

Schematic



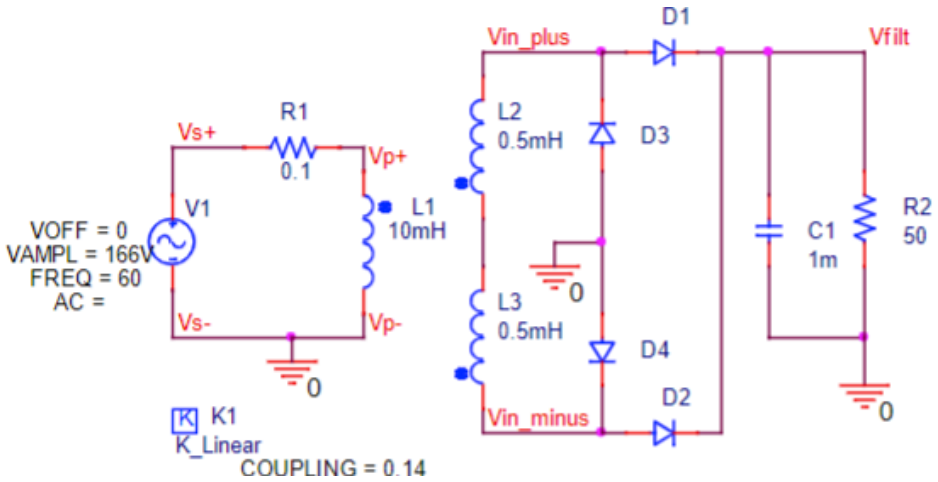
Excel Generated Plots



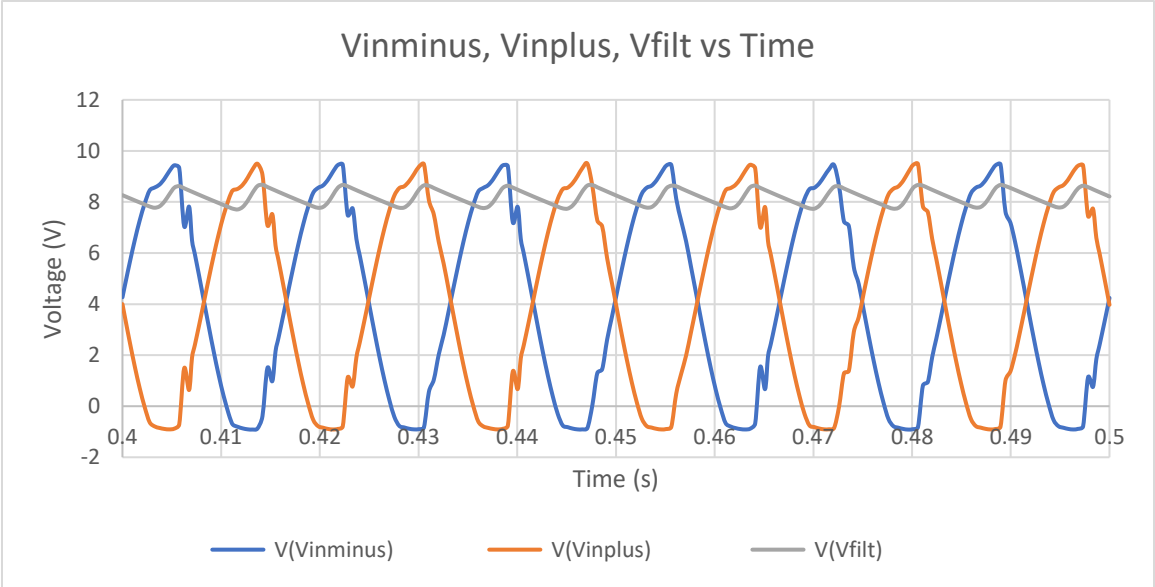
With the rectifier in place, the Vinminus portion of the input voltage at the transformer is flipped to positive, meaning that the frequency has now been doubled from 60Hz to 120Hz. Vrect at the resistor is slightly lower because of the diode activation voltages.

AC-DC Stage 3, Filter (SIM)

Schematic



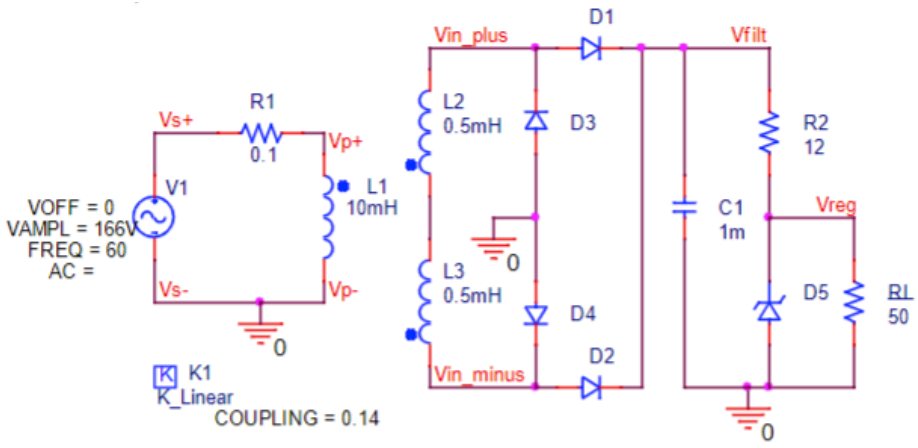
Excel Generated Plots



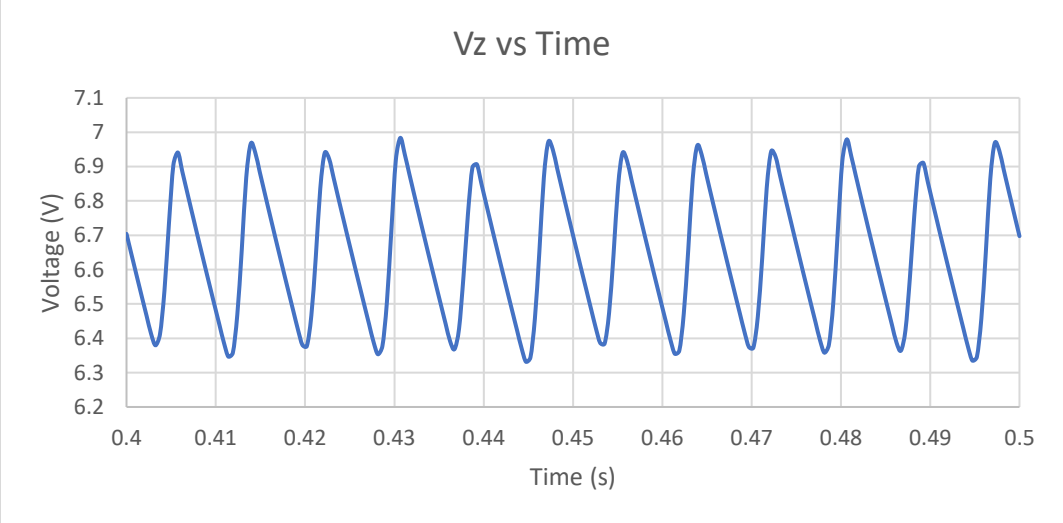
Comparing this plot to the load resistor configuration plot, we notice that the top of the Vrect waveform has been isolated and the new Vfilt signal is now slightly out of phase to the input signal due to the capacitor's discharge time. There are voltage fluctuations @ the input Vinplus and Vinminus around the time when the capacitor discharges and refreshes the voltage @ Vrect. This likely occurs at the input voltage before the capacitor in the circuit because some voltage is being drained by the capacitor for charging. Note the ripple voltage is ~0.4Vp. RRR is about 20log10(8.63/9.33)=-0.677.

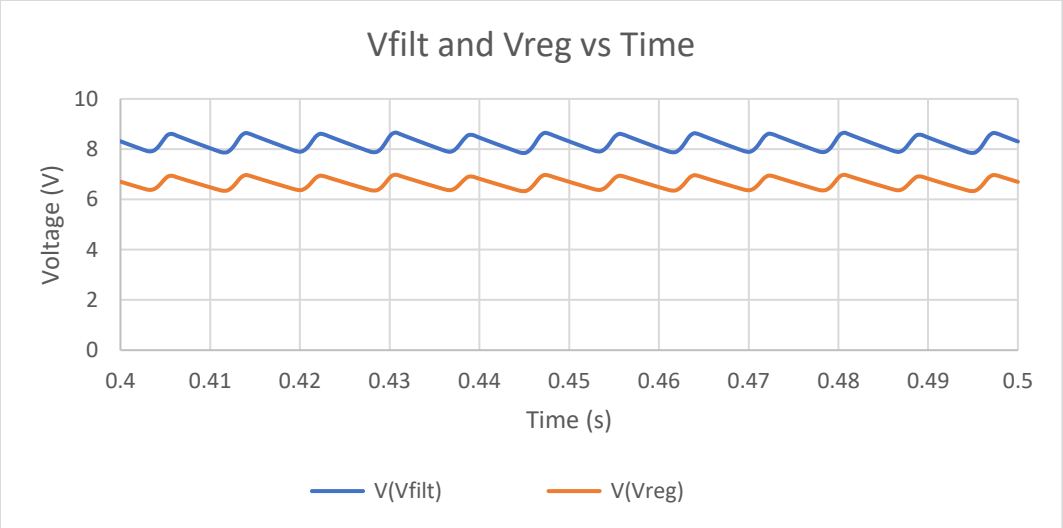
AC-DC Stage 4, Filter, Zener (SIM)

Schematic



Excel Generated Plots



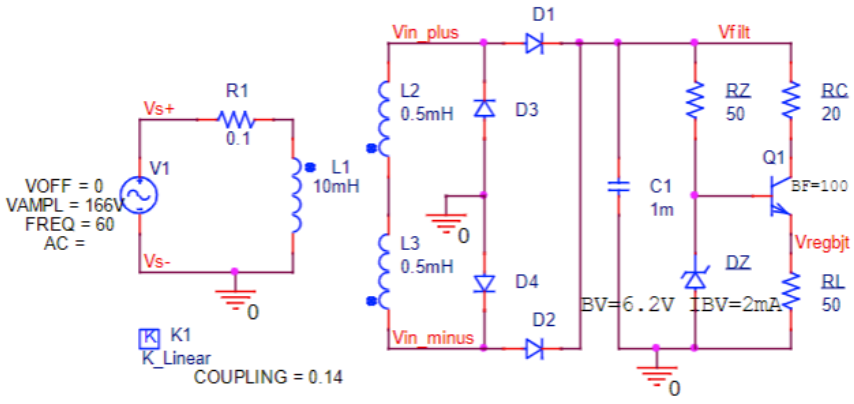


For plot 1, the Zener diode's breakdown voltage fluctuates from ~6.7V with fluctuations of ~0.2V. These fluctuations should be lessened by adding the BJT in the next stage.

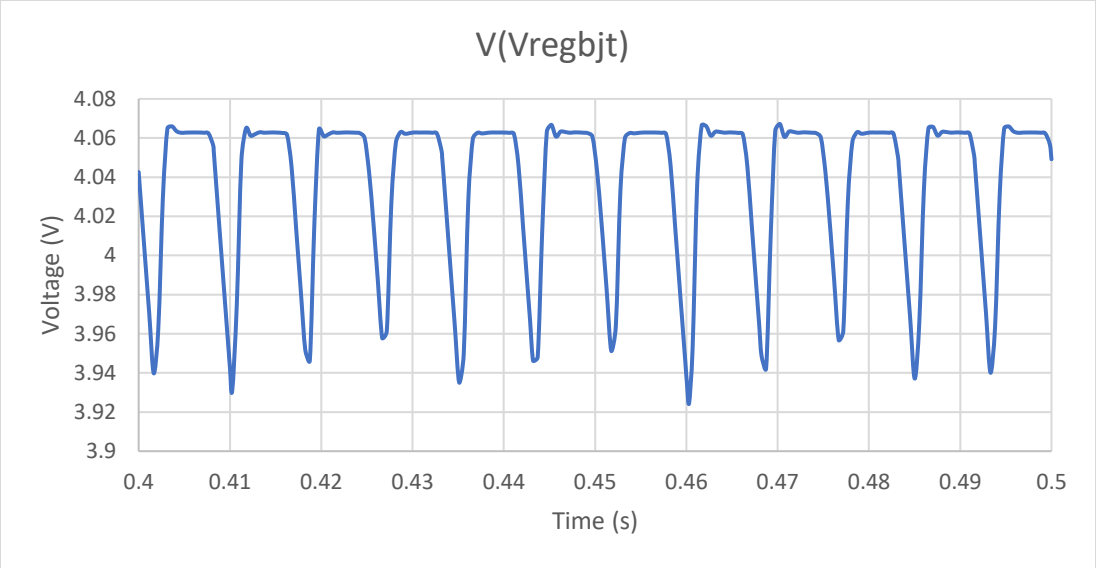
For plot 2, the Zener diode regulates the previously 8V Vfilt we see from stage 3, to ~6.2V with a ripple of ~0.1Vp. RRR is about 20log10(6.7/8.2)=-1.75.

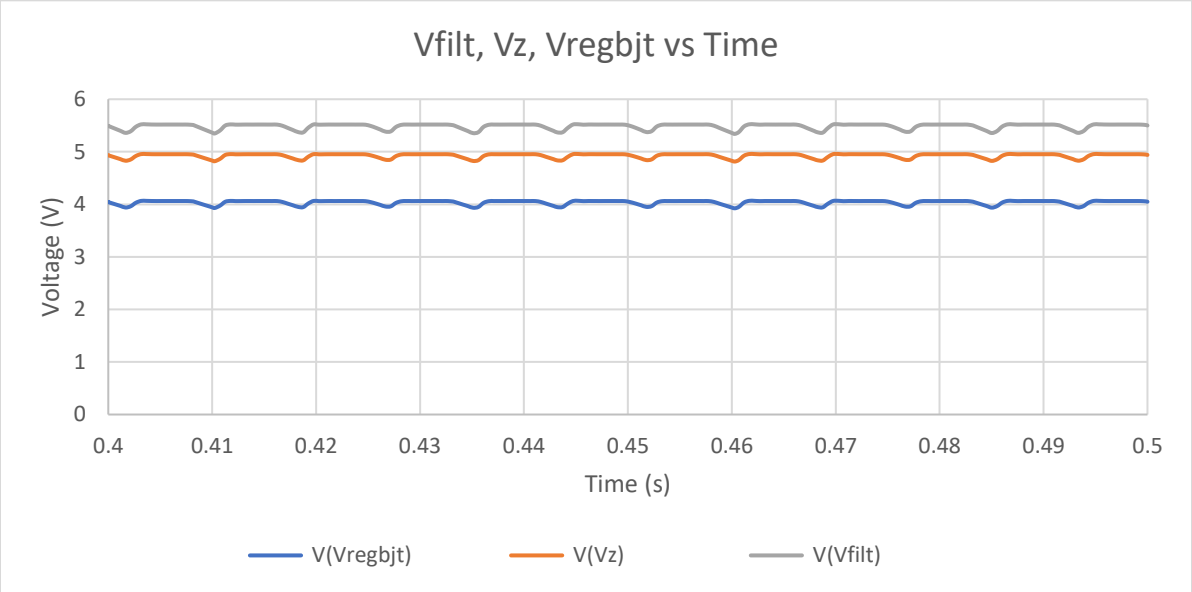
AC-DC Stage 5, Filter, Zener, BJT (SIM)

Schematic



Excel Generated Plots





For plot 1, the BJT has effectively reduced the voltage ripple to ~0.06Vp, much less than the 0.2Vp found in the Zener only circuit. Again, this is a result of the resistor configurations lowering the Iz (Ib). On the Zener characteristic curve, lowering the current will create a lower Vz in the breakdown region.

For plot 2, we see that Vfilt is now 6V as opposed to 8V as a portion of the current as been drawn away from the collector line (where Vfilt is) into the base line of the transistor. Then the

Zener diode regulates it down to 5V and it is reduced even further at the load by the 50 ohm resistor. (Ic=Ie, but Rc < RL). RRR is about 20log10(4.306/5.517)=-2.15.

Analysis

Analyzing the final circuit we can trace the behavior of the ripple voltage as each component is applied. First the transformer is used to step down the input 120Vrms AC voltage to an ~20Vpp AC voltage. The rectifier converts the negative portion of the sine wave to positive, doubling the frequency to 120Hz and creating a Vrect that somewhat resembles DC. The capacitor filter prevents the decay of the ripple voltage by discharging during decay and recharging the Vfilt output voltage. The rate of discharge can be manipulated via capacitance and resistor; it is controlled by the time constant T=RC and dictated by V(t)=Vi(e^(-t/RC)). We can now measure the ripple voltage @Vfilt to be ~0.4Vp. The Zener diode acts as the voltage regulator, but drops the output voltage due to its diode activation voltage. Yet it is still not optimized because the higher current Iz results in a higher Vz, which is our Vreg. We must use a BJT and a separate resistor to control the current coming into the Zener, splitting it along the base and collector lines so that we are placed further up the Zener breakdown voltage line in the Zener characteristic, reducing out output voltage's ripple even further. Note the RRR differences are from -0.677 w/ the filter only to -2.15 with the filter, Zener, BJT configuration. The values are small because it is a simulation environment, but greater negative values corresponds to a better rejection of the input's ripple at the output (aka less ripple at the output), which corresponds to our findings.

Addendum or Reference

Excel Generated Data (some datasets may be linked if too large)

Simulation Data (Stages 1 to 5)

2200L-L11sim1.xlsx

L11sim1.5.xlsx

L11sim2.xlsx

L11sim3.xlsx

L11sim4.xlsx

L11sim5.xlsx