JFET IV Characteristics

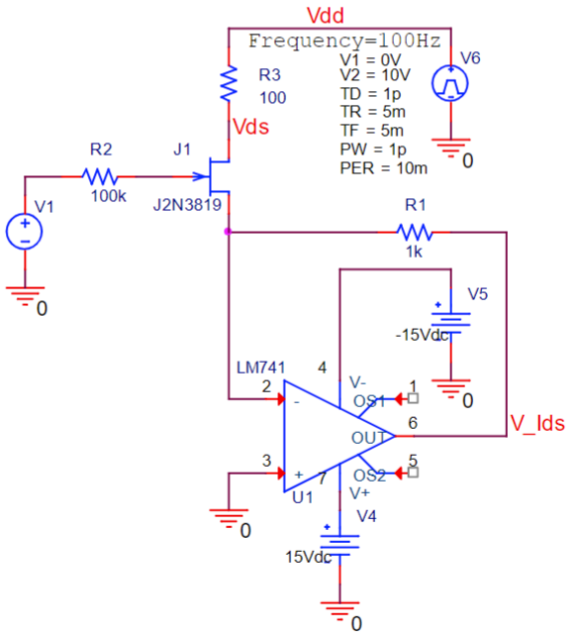
Contents

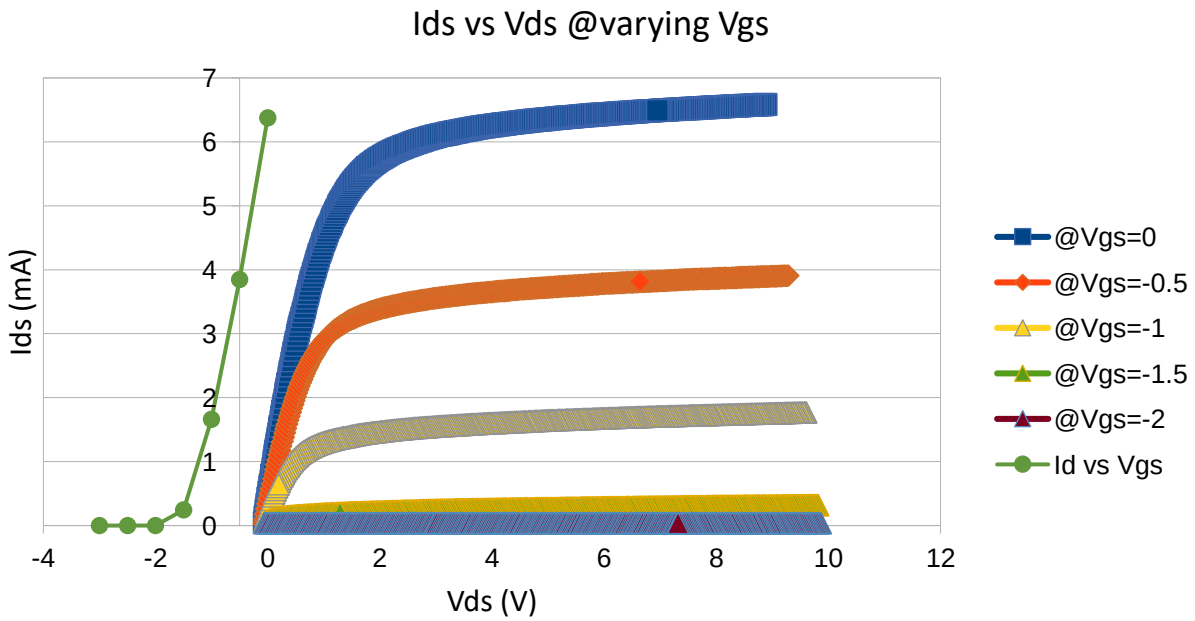
Executive Summary: The current voltage relationship in the JFET acts in an almost identical way to the FET, with the exception of varying Vgs at a negative voltage instead of a positive one to achieve the characteristic curves due to the natural ON state of the transistor allowing uninhibited electron flow. The input side Ids and sqrt(Id) vs Vgs relationship also match expected theory, with a exponential and linear relationship respectively. The output side Ids vs Vds also demonstrates characteristics curves that match the FET's.

Objective: To study the relationships between the terminal currents and terminal voltages in the Junction Field Effect Transistor (JFET).

JFET Op-Amp Circuit (LAB)

Schematic





JFET I-V characteristic curve on the right with the Id vs Vgs curve @Vgs=0 on the right.

Vgs (V)	Id (mA)	sqrt(Id)
0	6.376	2.525074
-0.5	3.848	1.961632
-1	1.66	1.28841
-1.5	0.245	0.494975
-2	3.00E-05	0.005477
-2.5	0.00E+00	0
-3	0	0
Vdd =5.63V		

Vdd= 5.63V is chosen, being in the saturation region for the Ids vs Vds curve @Vgs=0.

Vp = 2V // Vgs when Id=0, the x intercept.

Idss=6.376mA // Id @ Vgs=0, the y intercept.

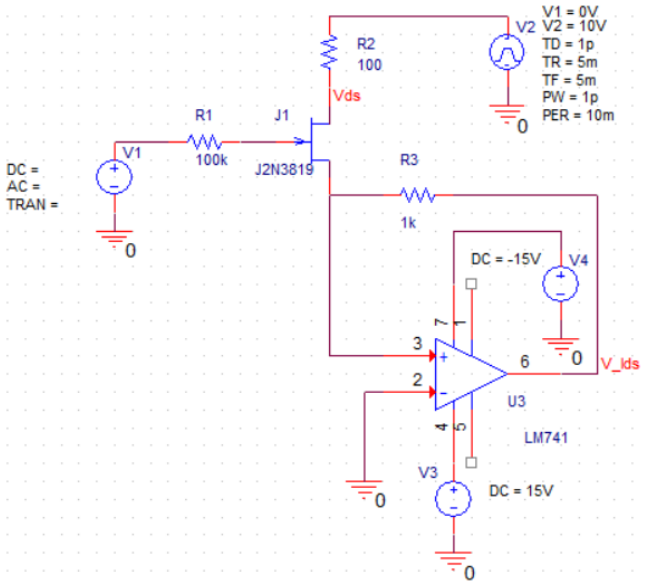
Using the oscilloscope's Ids vs Vds plot @ varying Vgs, we found Idss = 6.589mA and Vp=2V.

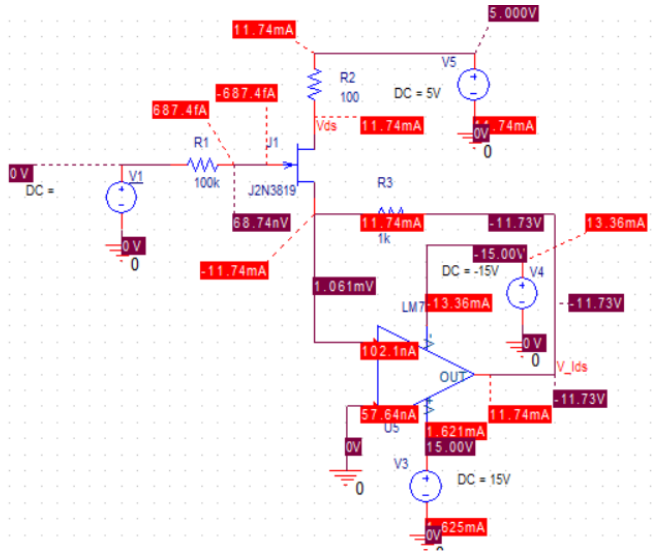
Comparing 1 operating point of the circuit in saturation mode (Vdd=5.63V, Vgs=0) (1) and vs the function's IV curve @ Vgs=0 (2), we see the values of Idss and Vp match. We can see this

graphically too, Idss is the same (y intercept in (1) and stable y value @ Vgs in (2)) and Vp is the same (x intercept in (1) and x value at transition point of linear and saturation modes in (2)). These similarities, as well as the similarities between the JFET and MOSFET curves demonstrate that the former can function the same as the latter.

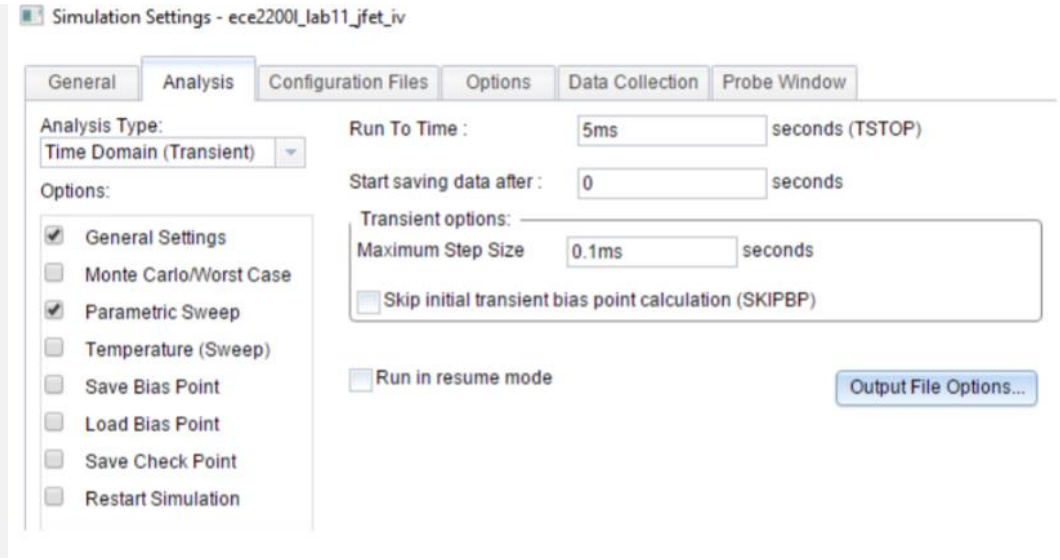
JFET Op-Amp Circuit (SIM)

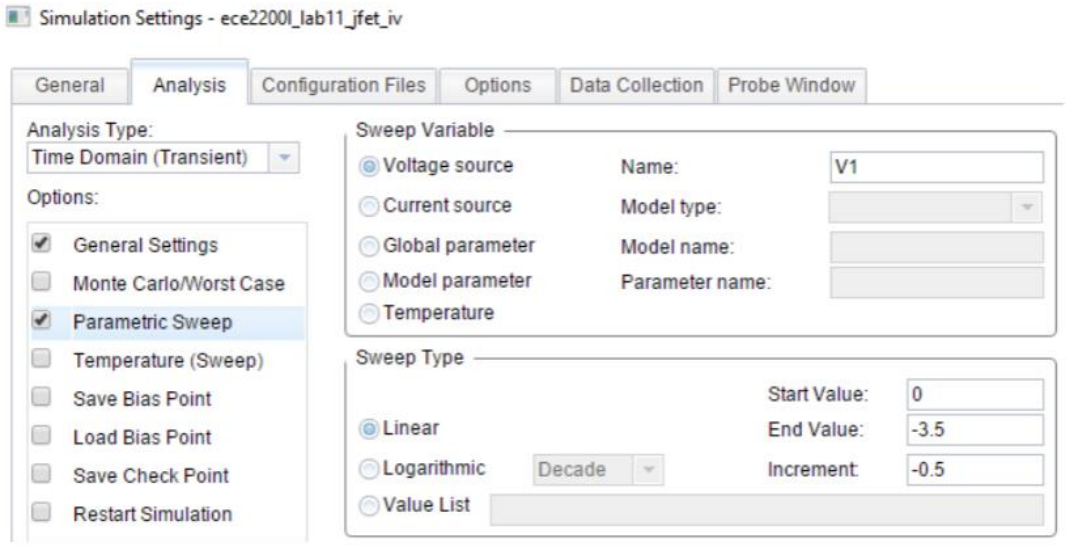
Schematic (note that -input pin of the opamp acts as virtual ground)



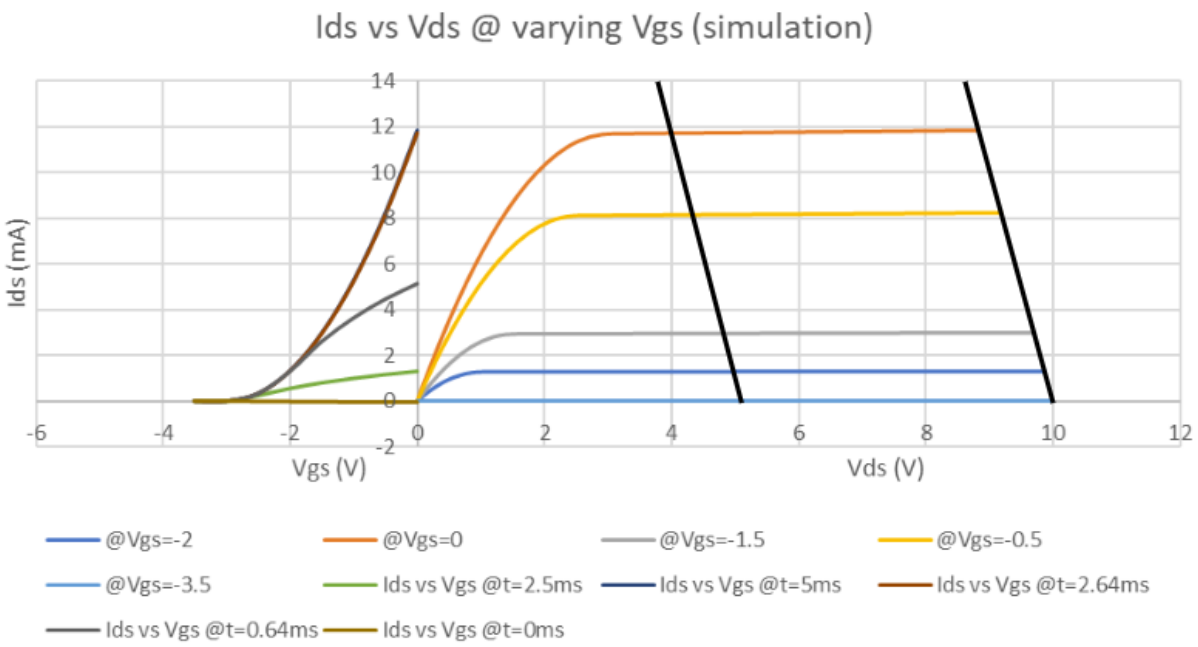


Simulation Profile



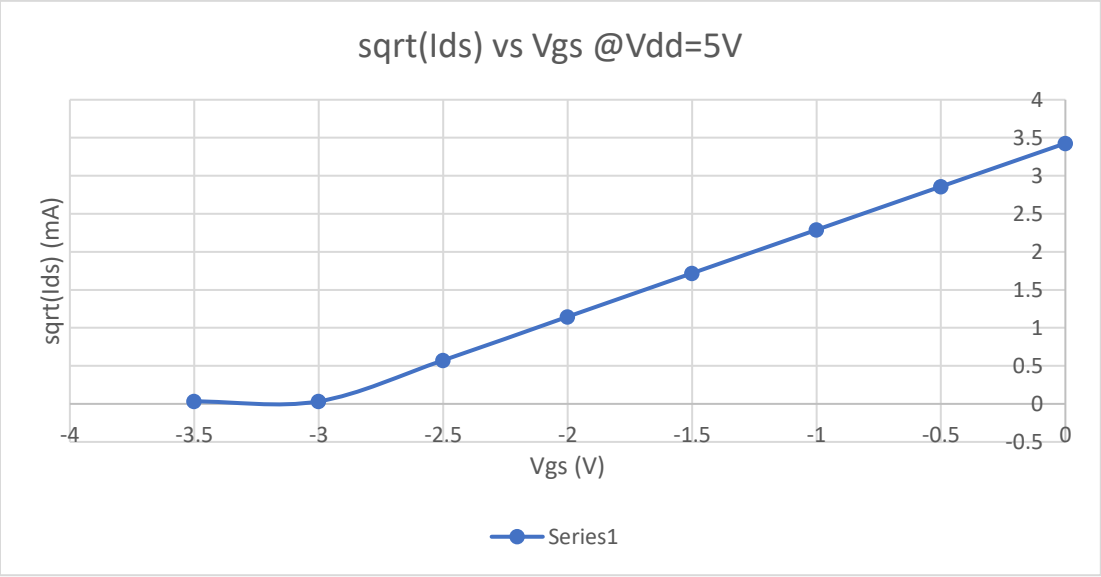


Excel Generated Plots



For the Ids vs Vgs graph, we are incrementing Vdd from 0 to 10V in 0 to 5ms so the larger the time the larger the Vdd.

Note that Ids=Id. We choose a Vdd=5V in saturation for the load line. Doing KVL around the circuit we receive Id=-Vds/Rd+Vdd/Rd where the y intercept is Vdd/Rd and the x intercept is Vds=Vdd=5V. Vdd/Rd = 5V/100ohm = 50mA. Similarly, for Vdd=10V, we receive a y intercept of 100mA and an x intercept of 10V.



A linear relationship line exists between sqrt(Ids) and Vgs, which is expect, since we know from theory (Idssmax=Idss*(Vgs/Vp -1)^2) that Ids increases exponentially with linear Vgs increase and we are removing the exponential behavior with the sqrt().

Graphically from the Ids vs Vds graph, we see Idds=~11.7 mA and Vp=~3.3V.

Graphically from the sqrt(Id) vs Vgs graph we see Idss= ~11.73mA (we do sqrt(Ids)^2) and Vp= ~3V.

Specifically we are analyzing the Idss and Vp @ the transition point between linear and saturation (but it could be anywhere along the horizontal of the Vdd=10V line, since that is also in the saturation) in the Ids vs Vds plot (output side) as well as the Idss and Vp from a chosen Ids and Vgs point (input side) in the saturation region where Vdd=5V. Since both match, the saturation behavior of the JFET is verified and is very similar to the FET.

Analysis

One difference between the JFET and MOSFET is the requirement for a -Vgs at the input side instead of +Vgs like in the FET. This is because of the JFET's makeup, which consists of the N, negatively charged, regions connecting the drain and source in the transistor's natural state. The gate voltage are P, positively charged, regions that, when a negative voltage Vg is applied, will gather electrons around inside. This electron-electron gradient between the N and now increasingly negative P regions will repel electrons and create a depletion layer, closing the channel between the two P regions and no allowing current to pass from drain to source. This operates different to FETs, which have two N regions (drain and source) separated by a P region that can be controlled by a gate voltage which contributes no current due to the metal oxide layer. When a positive voltage is applied at the gate (Vgs >Vth) negative charge carriers begin to attract towards the positive Vg and because the gate is in between the N regions, a current is established between the two N regions. In this way, we can see that both the JFET and the MOSFET can work in the same ways in the saturation region, and have applications like

amplification and switching. One works by the gate voltage restricting naturally established current flow and the other works by the gate voltage establishing current flow where there was none.

Addendum or Reference

Excel Generated Data (some datasets may be linked if too large)

Laboratory Data

Ids vs Vds @ varying Vgs Plot Data: ECE2200L-L9pt1.xlsx

Sqrt(Id) vs Vgs Plot Data: 2200-L9lab.xlsx

Simulation Data
Ids vs Vds @ varying Vgs and Ids vs Vgs Plots: 2200L-L9sim1.xlsx

Sqrt(Ids) vs Vgs Plot Data: 2200L-L9sim2.xlsx