MOSFET IV Characteristics

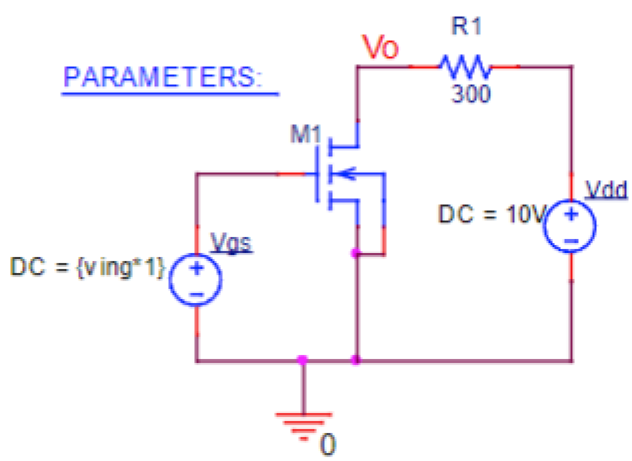
Contents

Executive Summary: The analysis of the output vs input (transfer) relationships of the MOSFET shows a nonproportional relationship between input voltage Vgs and output voltage Ids. When the former is increased, the latter increases exponentially, which confirms the saturation mode equation Id = (Kn/2)(Vgs-Vtn)^2 from theory. The relationship between Vds and Id is variable, MOSFET behavior changes depending on the mode. In cutoff, Id and Vds are 0 because Vgs has not overcome Vtn. In saturation, when Vds increases are large, Id increases are small, assuming real conditions, and approaching none assuming ideal conditions. In linear, as Vds increases, Ids has larger increases, and the two form a sloped line indicating a constant resistance.

Objective: To study the transfer characteristics of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) through laboratory experiments and PSpice simulation.

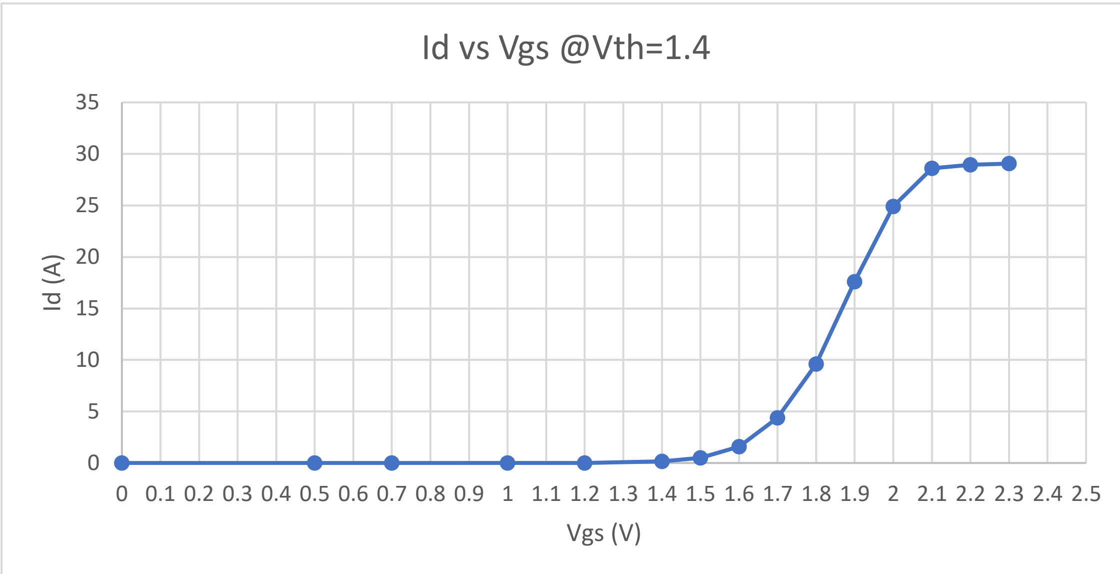
Figure 1 (LAB)

Schematic

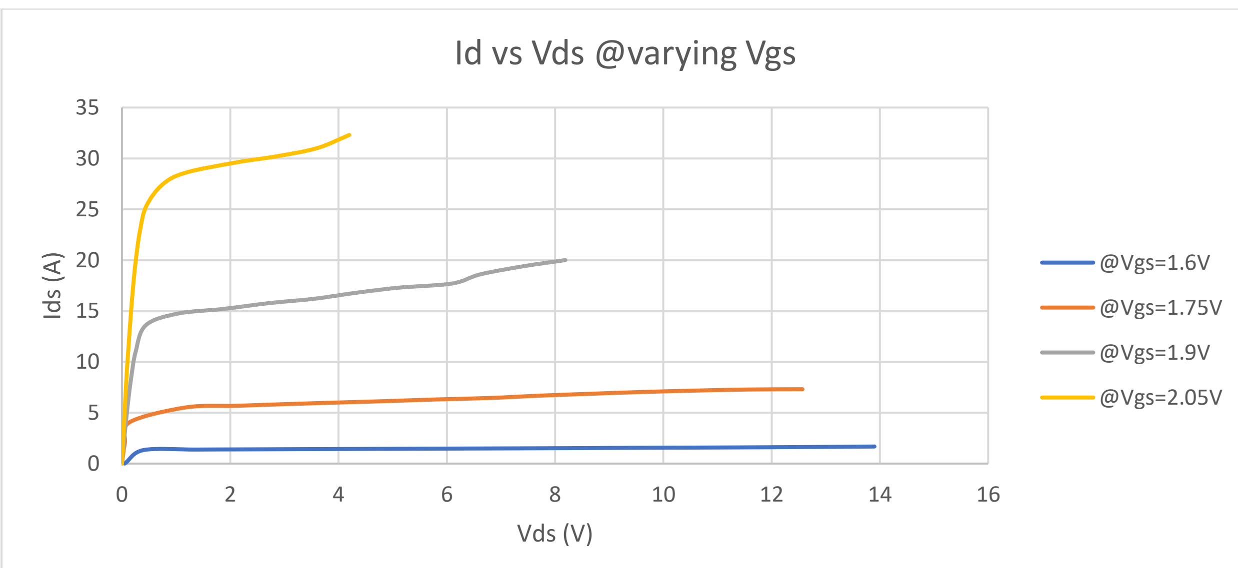


Excel Generated Plots

Plot Id vs Vgs, identify Vth. Graphically, Vth=1.4V, the point that indicates that the MOSFET is entering saturation and Id is beginning to increase exponentially.



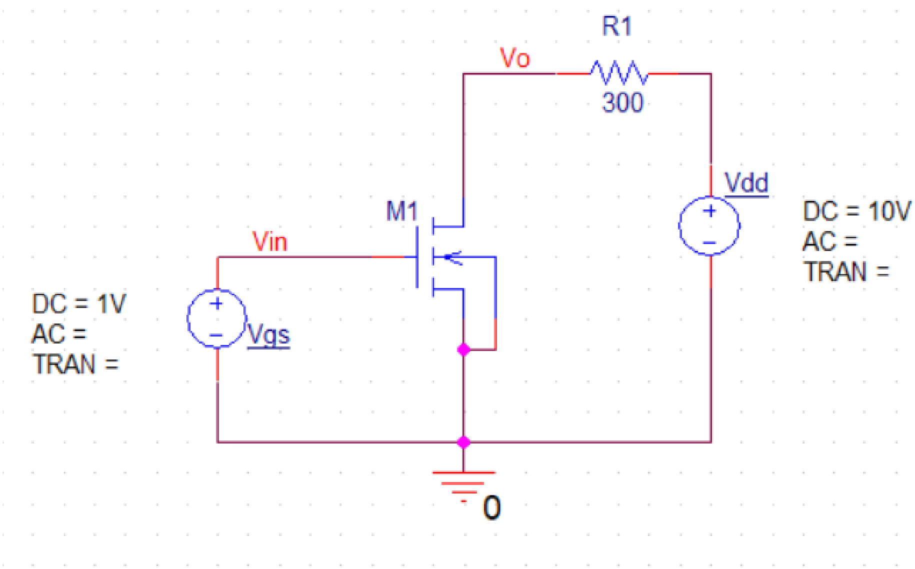
Plot Id vs Vds @ the chosen 4 Vgs points.



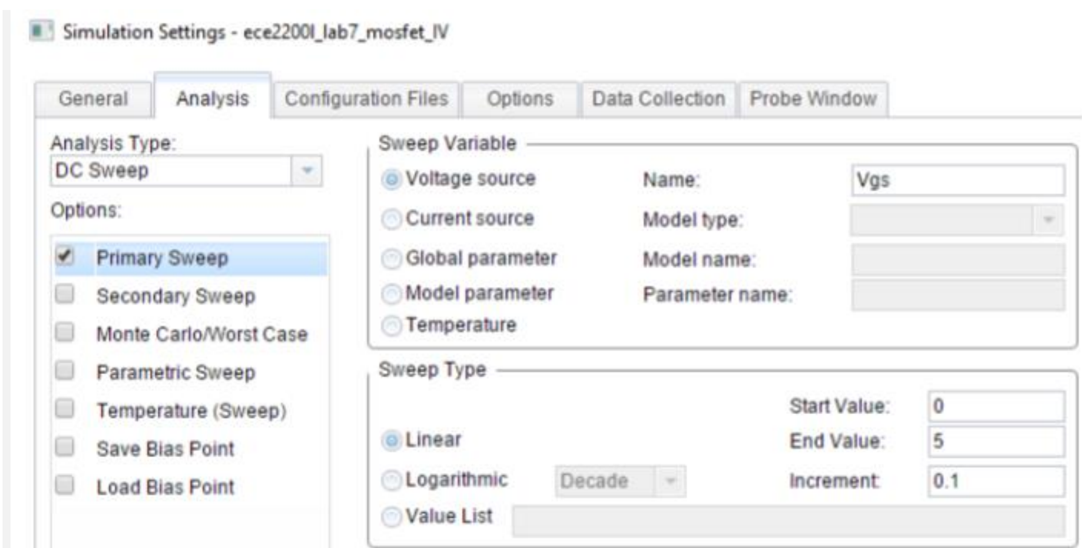
Not straight lines due to channel modulation (more on this in analysis), the resistor acts as an imperfect current source under real conditions. Compared with the simulation plot, where the current source is a much more ideal, straight line.

Id vs Vgs (SIM)

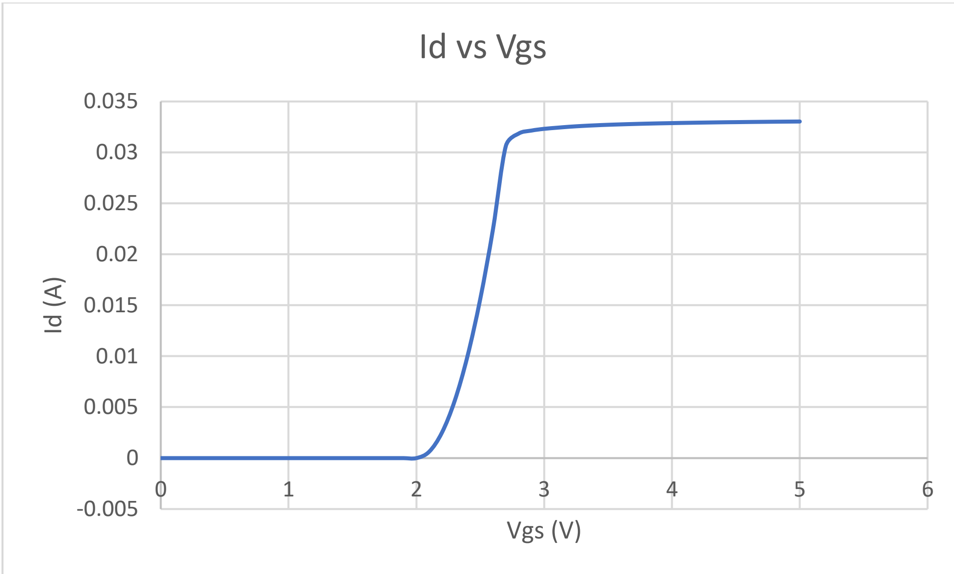
Schematic



Simulation Profile



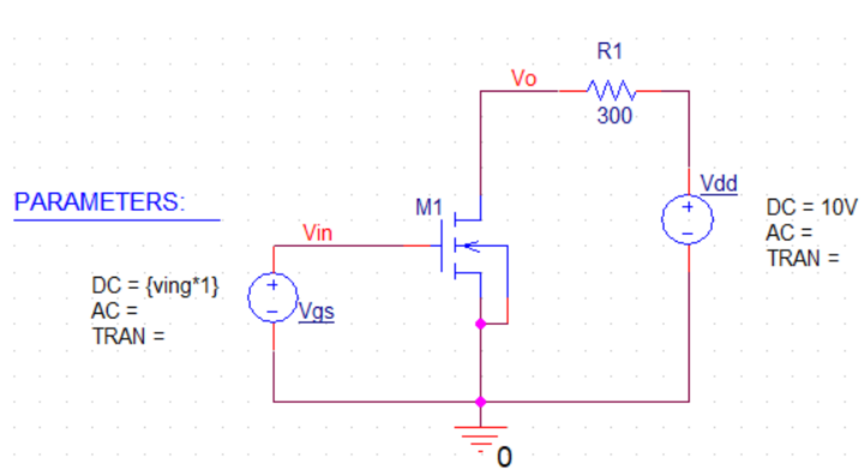
Excel Generated Plots



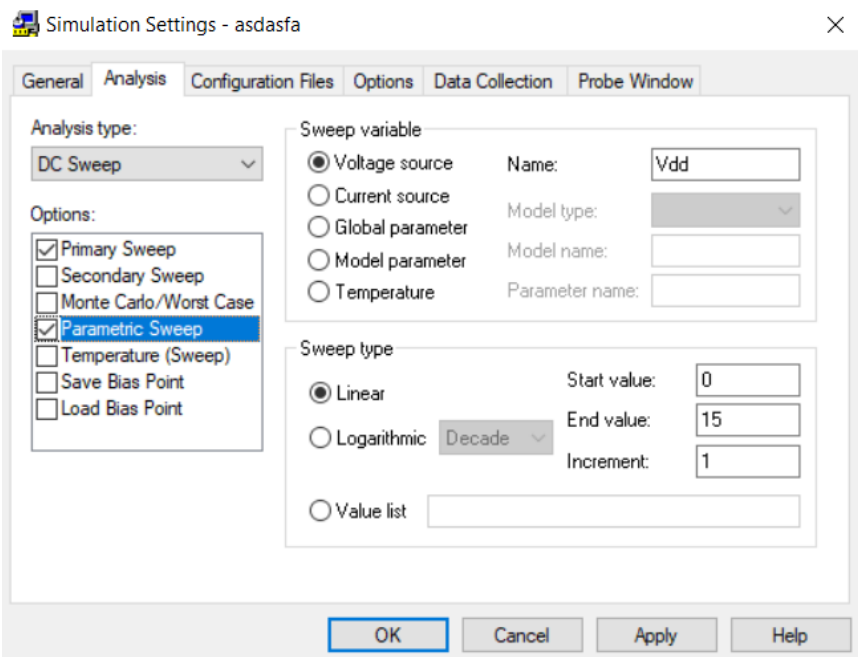
Vgs increase doesn't affect Id until the Vtn (or Vth) threshold voltage is overcome, this is cutoff mode. Once Vgs > Vth, the MOSFET enters saturation mode and Id rapidly begins to rise (the "wall" is overcome") until the linear region is reached and the MOSFET's resistance becomes constant.

Id vs Vds (SIM)

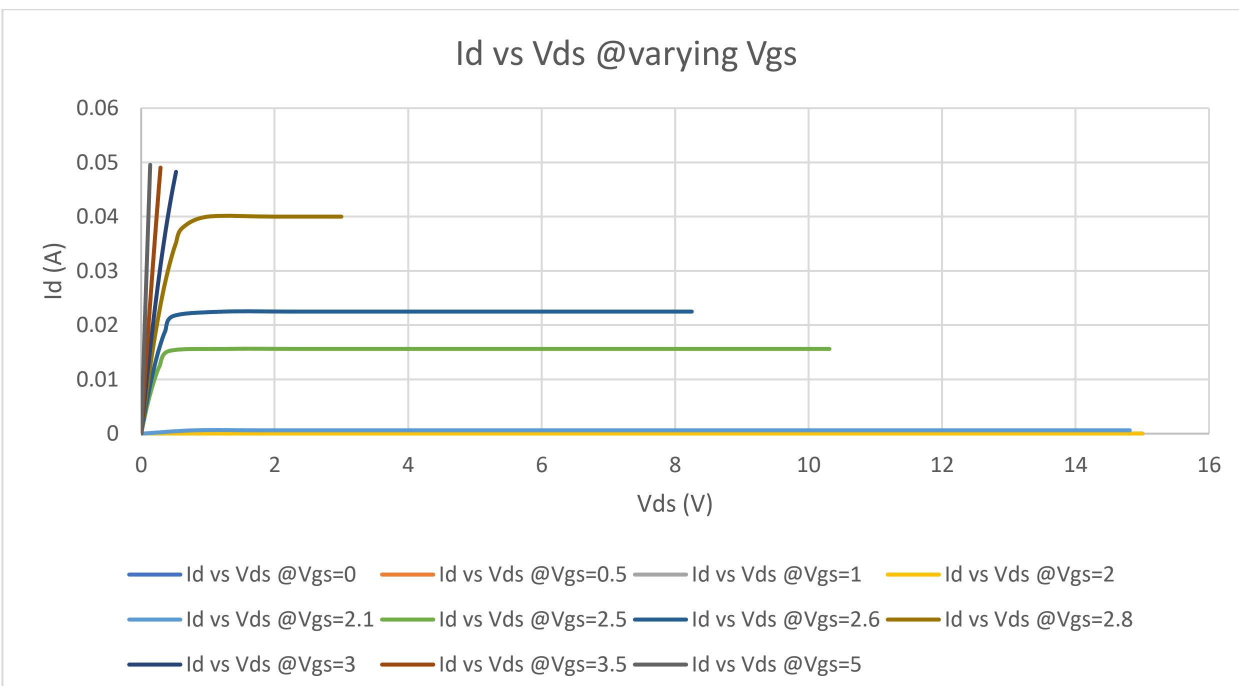
Schematic



Simulation Profile



Excel Generated Plots

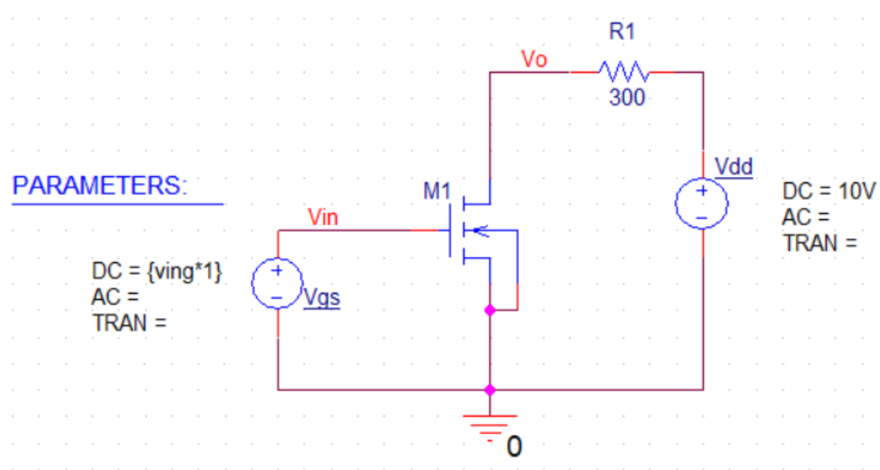


Before Vgs=2.1 there is no Id vs Vds change at all. @Vgs=2.1, there begins a change in Id vs Vds plot, a small Ids difference creates an exponential curve leveling off into a straight line.

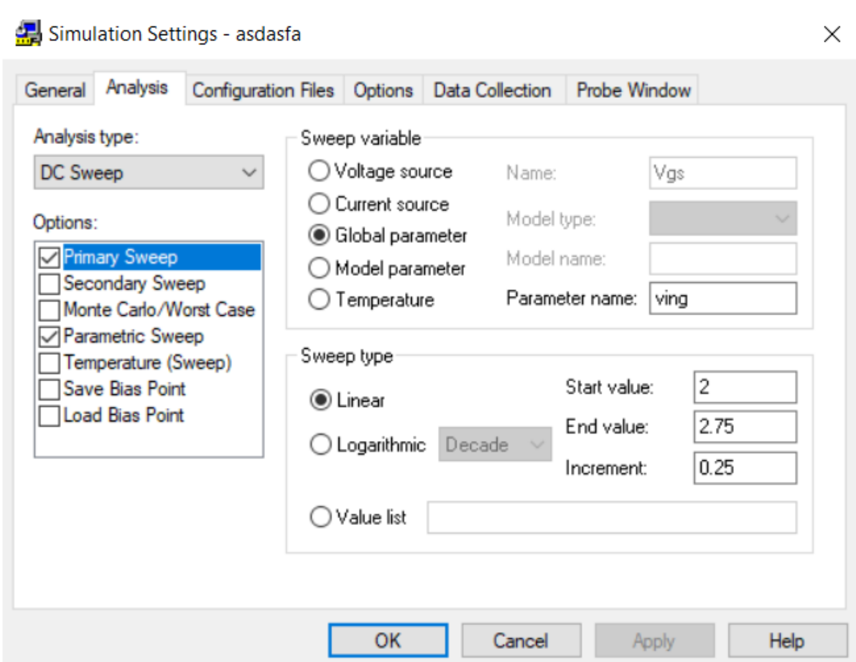
@Vgs=2.5 this increase is more noticeable. This shows that Id is increasing exponentially when Vgs increases linearly.

Figure 3 (SIM)

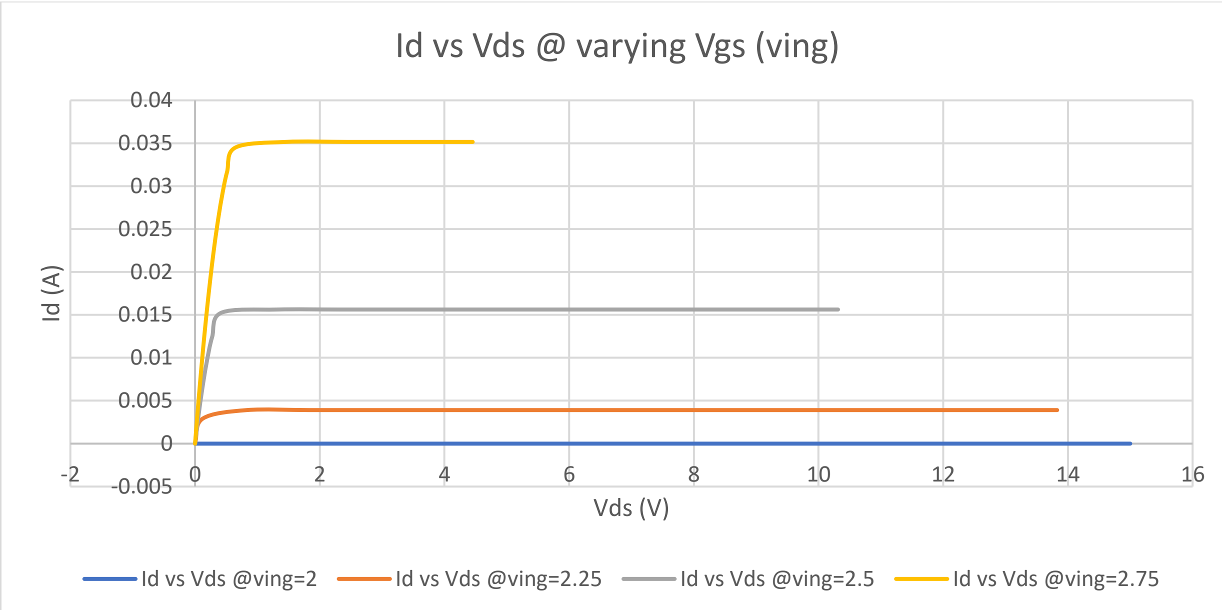
Schematic



Simulation Profile



Excel Generated Plots



At higher input voltage Vgs (incrementing linearly), MOSFET acts as an exponentially larger Ids current source, which is perfect (straight horizontal line) under simulation. This is also shown by the earlier Id vs Vgs plot.

Analysis

Firstly, regarding the Id vs Vgs plot, the saturation region mode is perfect for amplification uses because as Vgs increases and Vth is overcome, the MOSFET becomes like a resistor (looks like an imperfect pure voltage source), amplifying the input Vgs voltage into a high output Vds (through a high Ids). Ideally, in this region Id is completely dependent on Vgs only, not Vds as shown in the saturation equation. After pushing Vgs too high, linear mode is reached. Vgs (or Vdsat which is Vgs-Vth) becomes greater than Vds, and Id stops increasing exponentially. This behavior in the linear region is like a voltage-controlled resistor controlled by Vgs, where the resistance is maintained as constant no matter how large Vgs becomes. As mentioned in the relevant section, the relationship between Vgs and Id is nonproportional, Id increases are exponential when Vgs increases are linear. This can be seen in the second simulation plot, where the Id difference between Vgs@3 and @3.5 is ~0.022 A and ~0.04 A, Id almost doubles, while Vgs increases by ~17%. For the Id vs Vds plots, the difference between real and simulated conditions are most noticeable in the linear region where the MOSFET's Id vs Vds relationship begins to look like a current source: as expected, the lab data yields an imperfect sloped line as opposed to the perfect horizontal line of the simulation data, which is a result of the channel modulation between the source and drain N regions. That is, the increase of Vds controls the width of channel between the source and drain, which results in a small increase in the Id as Vds increases only under real conditions. Note that the transition region between linear and saturation modes is parabolic, governed by the linear equation: $I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS})$ (the saturation equation is also valid), which shows the initial exponential relationship between Vds and Ids.

Addendum or Reference

Excel Generated Data (some datasets may be linked if too large)

Lab Data: 2200L-L7lab.xlsx

^(includes Id vs Vgs Plot & Id vs Vds @varying Vgs Plot)

Simulation 1: 2200-L7model1.1.xlsx

Simulation 2: 2200L-L7model2.1.xlsx

Simulation 3: 2200-L7model3.xlsx