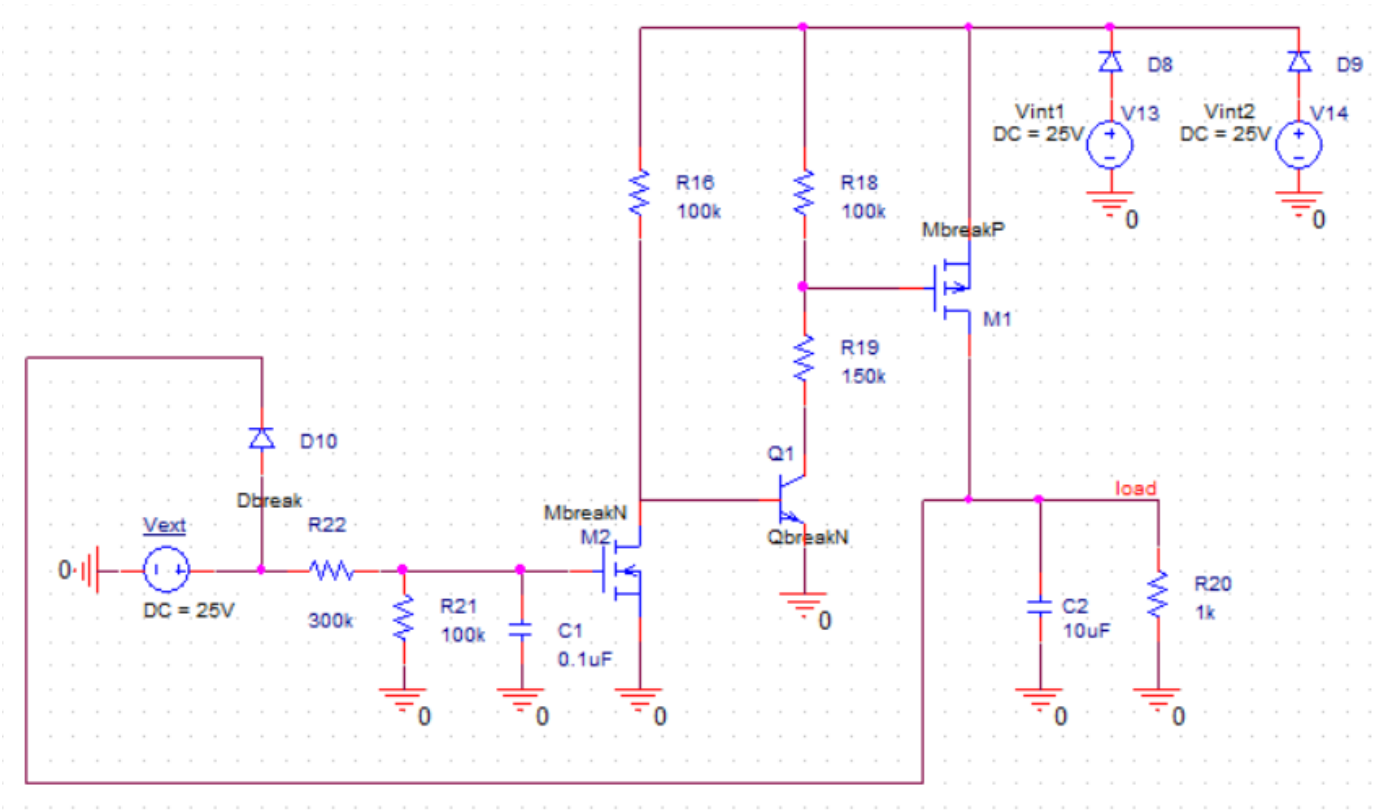
Power Switching Circuit Overview

Designed and written by Michael Huang

Circuit Requirements: Circuit must supply uninterrupted power to the load resistor at all times. It must detect the voltage from each internal battery and send an ON (1) or OFF (0) signal to the GPIO input of a Raspberry Pi to indicate when the battery is low charge or dead.

- Battery Voltage Range: 21-29.4V (~22V chosen as LOW, ~20V chosen as OFF)
- Max Load Current: 3A (5A chosen for most components)

Main Circuit



Summary:

When Vext is disconnected: Vint1 and Vint2 power the PMOS source (top), the PMOS gate, and the NMOS drain. The NMOS gate will be 0V, so the current will flow to the BJT base and allow the collector current to flow to GND, establishing the voltage divider (establishes low reference voltage potential of GND). The current will still flow to the PMOS gate and be subject to the voltage divider, so the Vgs is LOW relative to the high voltage at the source. With the voltages shown above, the Vg=14.6V, Vs=24.3V, so Vgs=-9.7V. This LOW Vgs allows the Vint1 and Vint2 current to flow down to the load.

When Vext is connected: Vext powers the NMOS gate and drains the current previously at the BJT base to GND. With the base not powered, current will still flow to the PMOS gate but NOT be subject to the voltage divider, so the gate voltage will be HIGH (less LOW) relative to the source. With the voltages shown above, the Vg=24.3V, Vs=24.3V, so Vgs=~0V. This HIGH (less LOW) Vgs prevents the flow of current at the PMOS source to drain and so only the Vext current flows to the load.

Reminder for Transistors:

- NMOS conducts current from drain to source when Vgs (gate voltage relative to source) is HIGH.
- PMOS conducts current from source to drain when Vgs is LOW. Source & drain are inverted from standard configuration (S on top, D on bottom).

Resistors: High valued resistors are chosen to prevent power loss at the expense of capacitor charging speed.

- The resistors at the NMOS are a voltage divider used to supply the NMOS's gate voltage. It must be within the Vgs(on) range specified by the transistor datasheet for Vext's entire voltage range, 21-29.4V. The resistors at the PMOS gate serve the same purpose and send the PMOS's approximate Vgs(on) to the gate.

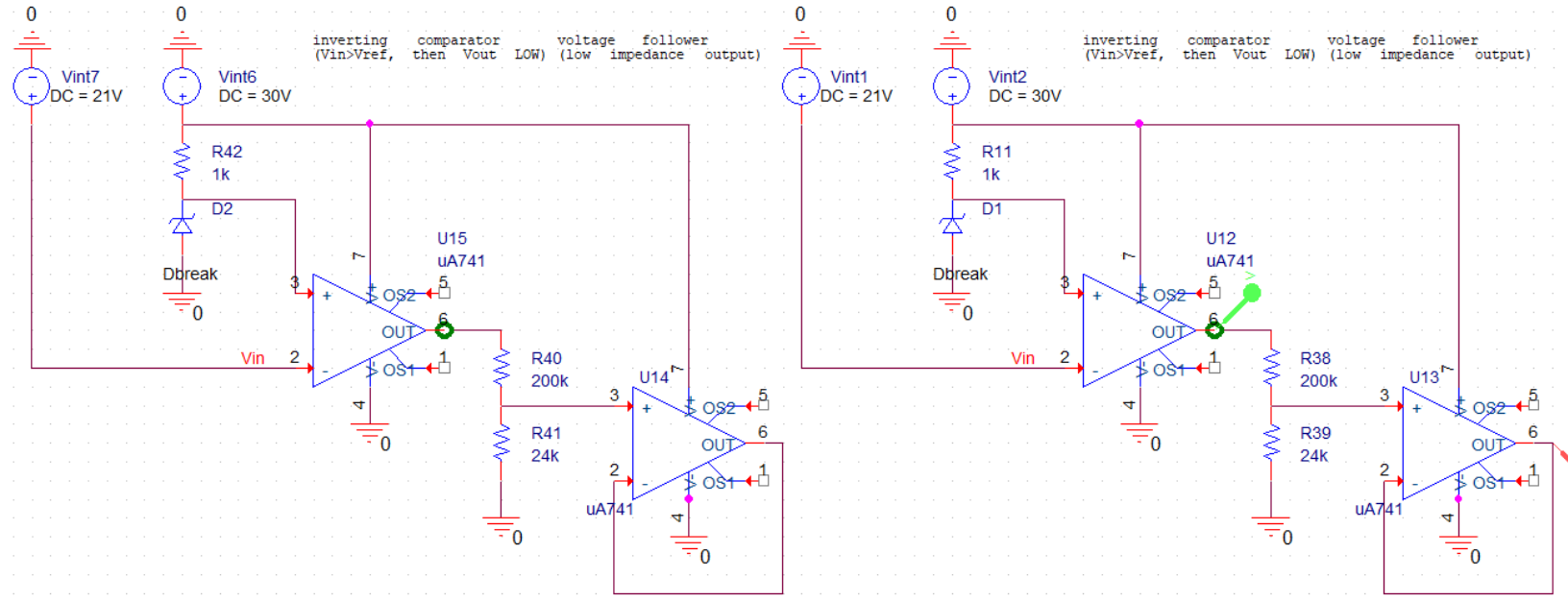
Schottky Diodes: One used for each battery. Used to prevent reverse currents from external sources or from the other batteries.

- Schottky diodes are specifically chosen for their lower voltage drop vs standard diodes and simplicity. The drop can be further lowered to the mV range with MOSFET (nmos, pmos) switching.

Capacitors: A 0.1uF capacitor is used at the NMOS gate to prevent voltage spikes/fluctuation from Vext. A 100uF capacitor is used at the load resistor to ensure that the voltage is maintained at the load while the circuit switches between Vint1 and Vint2, and Vext.

- 100uF Capacitor Calculation: Assuming max voltage and current, E=29.4Vx5A = 150W. Power needed during the switching time is 150Wx50ns (switching time) = 0.0000075W. By E=0.5CV^2 (cap charge stored eqn), with E=0.0000075W, V=0.5V (permissible voltage drop), I get C=0.00006F or 60uF, we use 100uF.

Voltage Sensing Circuit



Notes

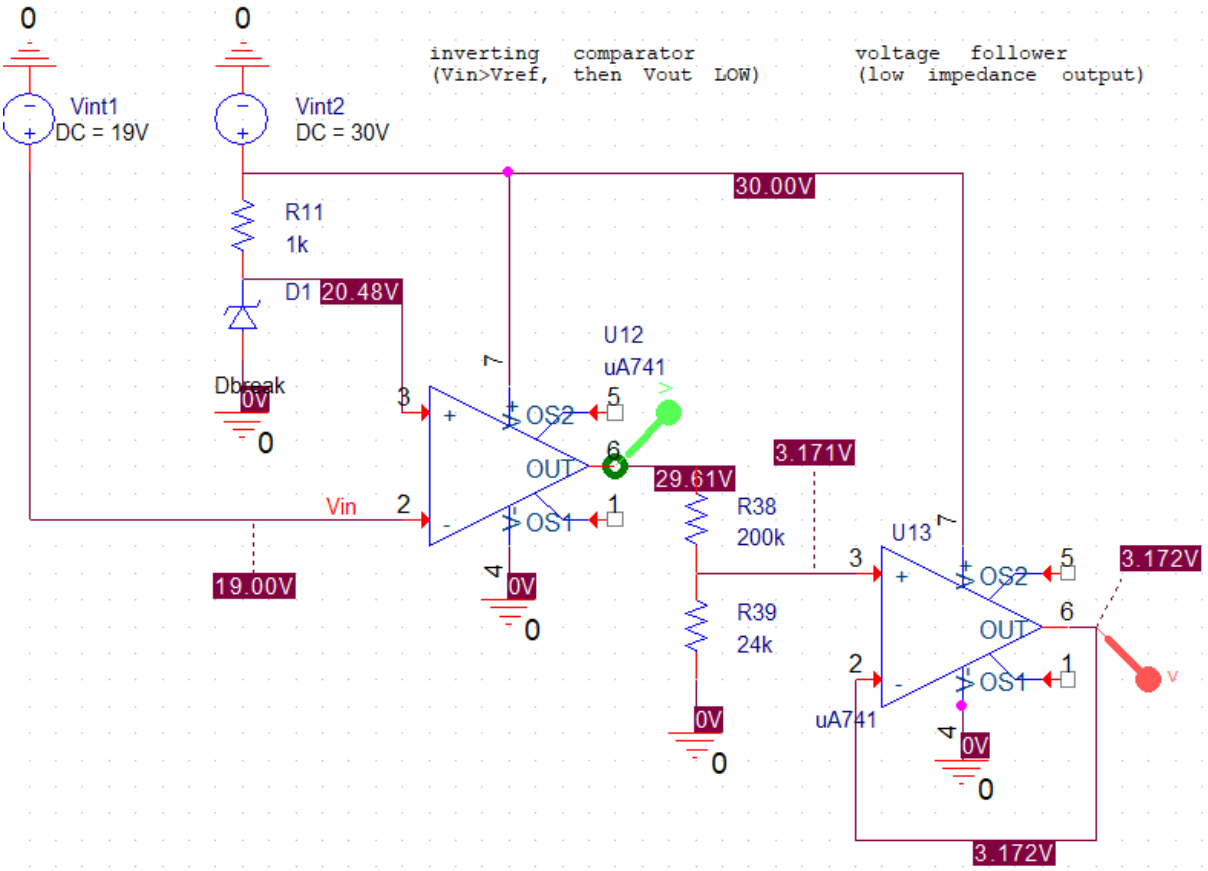
- Per the requirements, Vint1 and Vint2 are connected to 2 pairs of opamps instead of the 1 pair shown. The pair shown here are for the OFF (20Vz) signals. There is another pair for the LOW (22Vz) signals with different Zener diodes.
- At stage 2, Vdivider values are 200k and 24k, tuned to give a 2.1-3.3V output for a 20-30V input. Pi GPIO 4 reads HIGH at 2V-3.3V. So it will produce at HIGH output for the entire range of 20-30V (though of course when input battery is below 22V and 20V, it will trigger a 0V output)
- Since Vint2 fluctuates (less voltage as it drains), the current going into the Zener will fluctuate away from the rated Izt, so there exists reference voltage fluctuations as well.

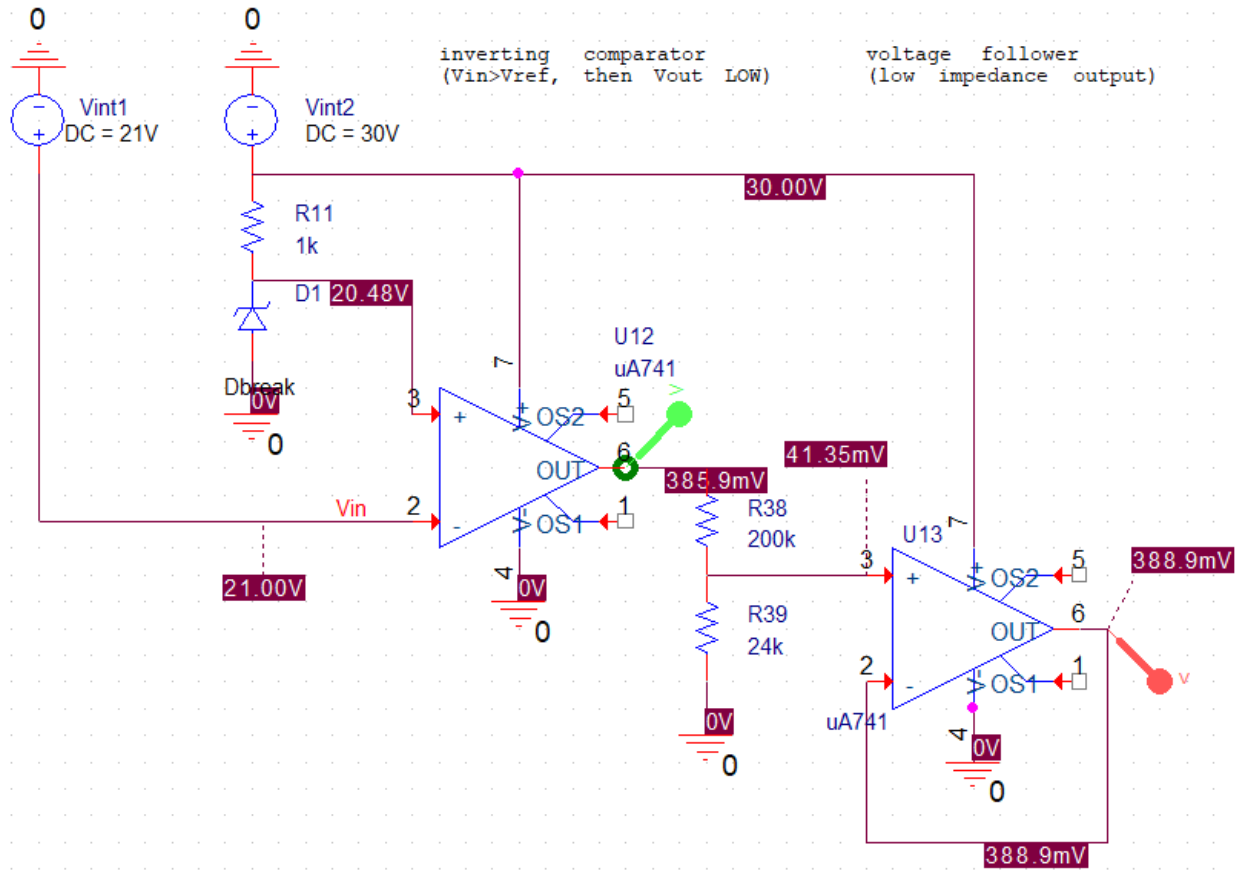
Summary: There are two stages in the design. The first uses an opamp as an inverting comparator which follows these rules: (If Vin>Vref, then Vout LOW), (If Vin<Vref, then Vout HIGH). Stage 1's output range is ideally 0V-30V. Too high a raspberry pi GPIO pins, which registers HIGH at 2-3.3V. The voltage follower opamp at stage 2 will create a LOW impedance output, allowing it's 3V output to sink enough current (nA to uA range) to the raspberry pi 50k GPIO pulldown resistor. It will be below the 0.5mA input current limit.

Current Limiting Resistor Calculation: For example, given a 20Vz, 5mA Iz Zener diode, we will need R=800-2k for the Vint2 voltage range. The equation is R = (Vin-Vz)/Iz, so w/ the average value of Vint2, R=(25.2-20)/0.005=1.04k→1k. For a 22Vz, 5mA Zener diode, R = 650→700. Ploss = ((Vin-Vz)^2)/R = 0.13W, so 1/4W resistors are used.

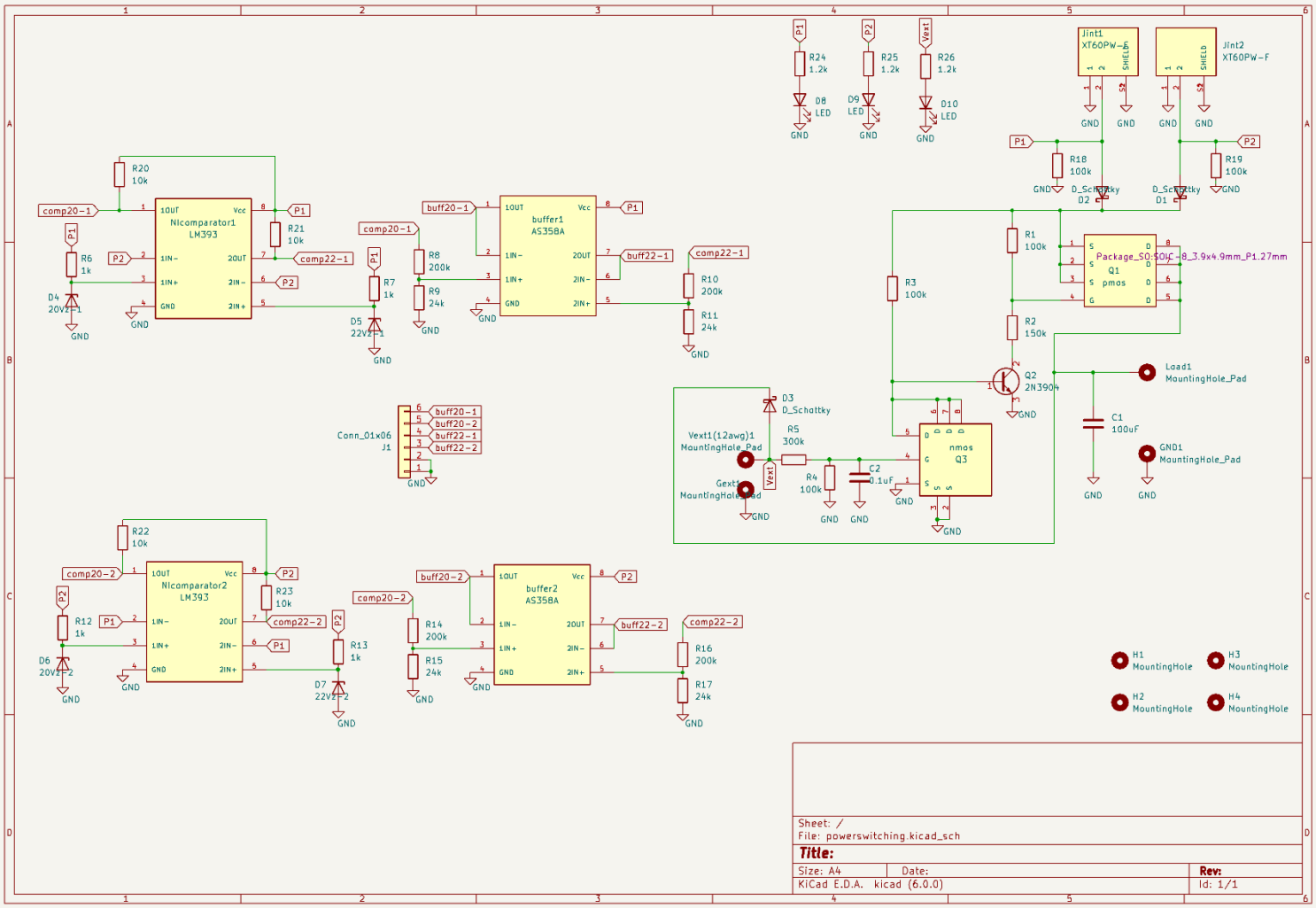
Pullup Resistor Considerations: A 10k pullup resistor is used to connect the stage 1 output's to Vsupply. It limits stage 1's sourced current to 30V/10k = 3mA. Since stage 1 output has high impedance (~infinity), then the pullup resistor creates a Vdivider: Vout (when HIGH) = (infinity/(10k+infinity))Vcc = Vcc.

Simulation Results

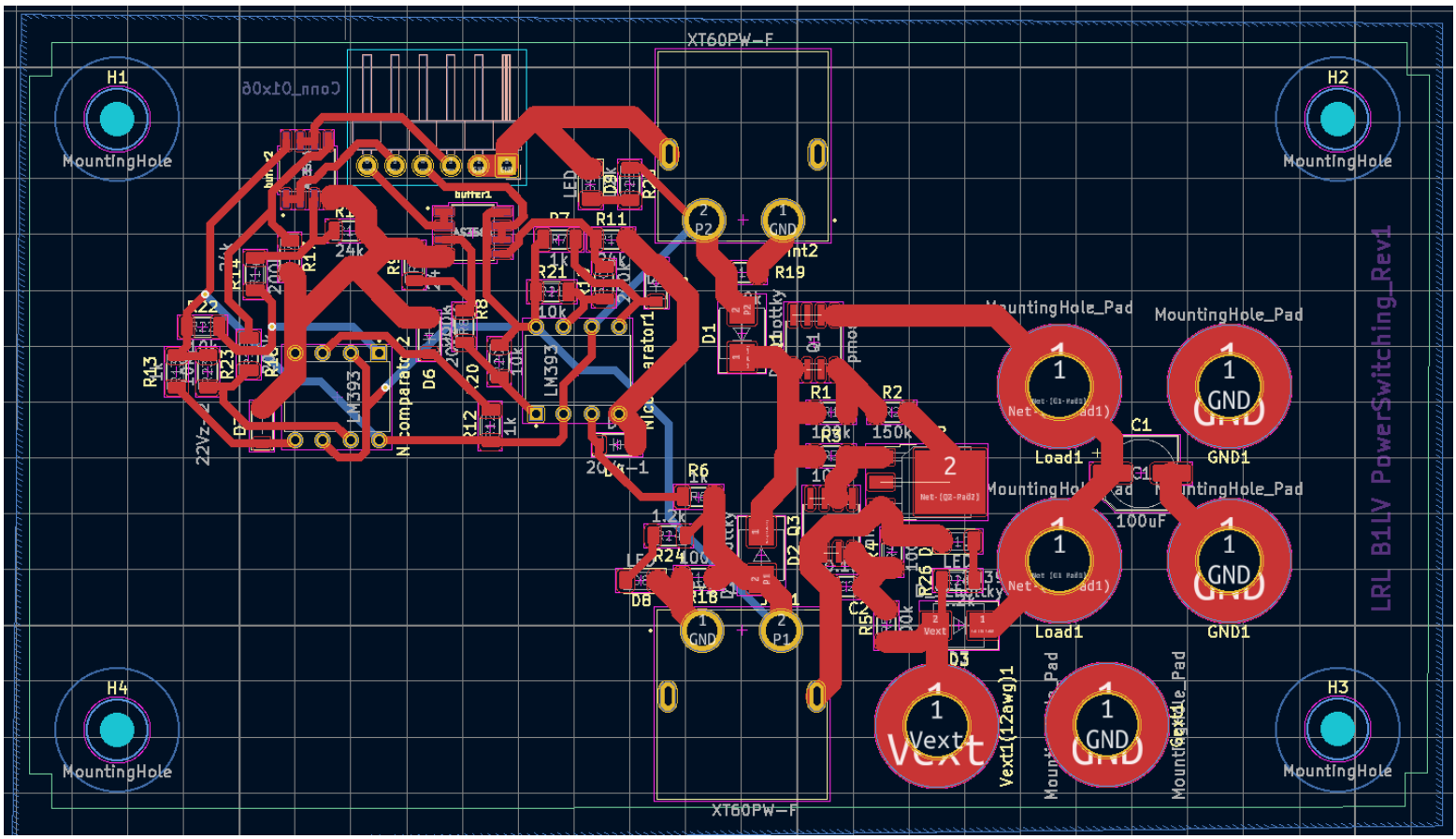




PCB Schematic



PCB Routing



PCB Model