

Batch Wafer Quality Summary Report

Report Generated: 2025-12-27 12:32:13

Simulation Date: All Dates

Report Type: Summary Only (Per-Wafer Details Excluded)

Batch Summary

Total wafers: 758

Date Range: 2025-12-21 to 2025-12-27 (3 days)

PASS: 523 | **FAIL:** 235

PASS rate: 69.0%

Top 5 Highest Defect Percentages

- Electrical_ELEC_02_W0018 (Electrical): 98.04% [Near-Full]
- Electrical_ELEC_02_W0035 (Electrical): 98.03% [Near-Full]
- Mechanical_MECH_02_W0041 (Mechanical): 96.48% [Near-Full]
- Thermal_THERM_01_W0032 (Thermal): 95.53% [Near-Full]
- Thermal_THERM_01_W0022 (Thermal): 94.31% [Near-Full]

Distribution by Machine Type

- Electrical: 302 wafers
- Mechanical: 261 wafers
- Thermal: 195 wafers

Distribution by Defect Class

- Normal: 519 wafers
- Donut: 37 wafers
- Edge-Ring: 35 wafers
- Local: 34 wafers
- Edge-Loc: 33 wafers
- Random: 31 wafers
- Near-Full: 25 wafers
- Scratch: 25 wafers
- Center: 19 wafers

AI-Enhanced Engineering Summary

The batch yield is currently at 69%, with a total of 758 wafers processed and 235 failing. The predominant defect class impacting yield is 'Near-Full', which accounts for significant failures across all machine types, especially Electrical and Thermal. The top five worst wafers exhibit defect percentages above 94%, indicating severe contamination or process issues. Mechanical, Electrical, and Thermal machines all contribute to the defect distribution, but Electrical machines show the highest number of critical failures.

Estimated batch yield impact: High

Key Risks

- High incidence of Near-Full defects across multiple machine types
- Severe wafer contamination leading to very high defect percentages
- Potential process instability in Electrical and Thermal machines
- Cross-machine type defect propagation risk

Recommended Actions

- Perform root cause analysis focusing on Near-Full defect sources
- Inspect and recalibrate Electrical and Thermal machines urgently
- Implement enhanced cleaning and contamination control protocols
- Review process parameters and maintenance schedules for all machines