



# USER'S MANUAL

**AVME**  
**SERIES**

68040 MPU MODULE

## AVME-148



Before using this product, be sure to read the instruction manual carefully and use it correctly.

Keep the instruction manual so that you can refer to it at any time.

Please also reread it so that you can always perform the correct operation.

**Important points to note when exporting**

This product is designed for use in Japan. We take no responsibility if this product is used outside of Japan.

vinegar.

In addition, we do not provide maintenance services or technical support for this product overseas.

**Note**

1. Reproduction of any part or all of the contents of this book without permission is prohibited.
2. The contents of this document may be changed without notice in the future.
3. We have taken every precaution to ensure the accuracy of the contents of this document, but if you find any suspicious points, errors, or omissions, If you have any concerns, please contact the store where you purchased the product.
4. Please note that we cannot be held responsible for any consequences resulting from operation, regardless of paragraph 3.

Copyright                  2004 AVALDATA CORPORATION

All company names and product names used in this document are trademarks or registered trademarks of their respective companies.

## Before reading this manual

This manual describes how to use the product safely and prevent injury to yourself and damage to property.

The following pictorial symbols are used to prevent accidents. Please read the text after you have fully understood the meaning of the pictorial symbols.

Please take a look.



### caveat:

If you ignore this warning and handle the product incorrectly, it may result in death or serious injury.

This is an issue that is expected to be addressed.



### Note:

If you ignore this warning and handle the product incorrectly, it is possible that you may be injured.

These are matters for which the actual operation of the equipment may be seriously affected, and matters for which only physical damage is expected to occur.

	This indicates that improper handling may result in electric shock.
	This indicates that improper handling may result in injury.
	This indicates that improper handling may result in damage due to high temperatures.
	For safety reasons, this instructs you to always unplug the power cable.
	This indicates that improper handling may result in smoke or fire.



## caveat:

Do not put the sub-battery built into this product into your mouth.

The contents of this product contain substances that are harmful to the human body.

If this occurs, spit it out immediately, rinse your mouth, and consult a doctor.



## Note:

•Please use AC100V (50/60Hz) as the power source for this product. If you use it with a different voltage, it may cause damage.

This may cause electricity, smoke, or fire.

•Do not use this product in places with a lot of water or moisture, as this may result in electric shock.

•Do not plug the device's power cord into an AC outlet with wet hands.

This can cause the following problems.

When the power cord is connected to an AC outlet, do not touch the unit with wet hands.

Doing so may result in electric shock.

• When installing or removing peripheral devices, unplug the power cord from the AC outlet.

Do not install or remove any peripheral devices with the power cord still connected to the AC outlet.

Doing so may result in electric shock.

• Connect the power cord plug of the device to an independent AC outlet that has a ground terminal.

An unconnected or improperly connected earth may cause electric shock or malfunction.

Also, excessive use of electrical outlets can cause the outlets to overheat and lead to a fire.

If a malfunction or abnormality occurs, immediately stop using the product and notify the designated contact.

stomach.

•Customers are prohibited from repairing or modifying the product.

**Chapter 1. Precautions for Use**

- 1.1 Handling the VMEbus module (board) 1-1
- 1.2 Aftercare 1-5
- 1.3 Module disposal method 1-7
- 1.4 Handling of lithium batteries 1-7

**Chapter 2 Overview**

<b>2.1 Overview .....</b>	<b>2-1</b>	<b>2.2 Features</b>
of AVME-148 .....	2-2	2.3
Specifications .....	2-3	2.4 Cooling
Conditions .....	2-5	2.5
Configuration .....	2-6	2.6 Memory
Map .....	2-7	2.7 Parts Layout
Diagram .....	2-8	2.8 EPROM Layout
Diagram .....	2-10	2.9 Related
Documents .....	2-11	

**Chapter 3 Memory Map**

<b>3.1 AVME-148 Memory Map .....</b>	<b>3-1</b>	<b>3.2</b>
System ROM Memory Map .....	3-3	3.3 Local I/O Memory
Map .....	3-4	3.4 VMEbus Memory
Map .....	3-5	3.5 VMEbus Short I/O Memory
Map .....	3-6	

**Chapter 4. Front Panel**

<b>4.1 Front Panel, Switches, and Indicators 4-1</b>	<b>4.1.1 Front Panel DIP Switches 4-1</b>	<b>4.1.2 Front Panel Appearance 4-2 (SW1)</b>	<b>4-3</b>	<b>4.1.3 RESET Switch</b>
--	---	---	------------	---------------------------

(SW2) 4-3 4.1.4 ABORT switch

4.1.5 RUN indicator (DS1) 4-3	4.1.6 HALT indicator (DS2) 4-3	4.1.7 FAIL indicator (DS3) 4-3
4.1.8 SCON indicator (DS4) 4-4	(DSW1) 4-5	

<b>4.2 Front DIP Switch Settings</b>
--------------------------------------

## Chapter 5

Functions	5.1 Function Operation	5-1
5.1.1	MPU	5-1
5.1.2	Multiport Arbiter	5-1
	5.1.3 Dual Port Memory (DPRAM)	5-1
5.1.3.1	Access to DPRAM from MPU	5-1
5.1.3.2	Access to DPRAM via VMEbus	5-3
5.1.3.3	5.1.3.4 Access to DPRAM via LAN and FDC	5-3
5.1.3.4	5.1.4 Local SRAM	5-3
5.1.5	Flash	5-3
5.1.6	Bus	Memory
Error		5-4
Monitoring		5-4
Battery		5-4
(WDT)		5-5
Function		5-5
Controller		5.2 VMEbus System
	5.2.1	VMEbus
Supervisor		5-6
Driver		5-6
Arbiter		5-6
Driver		5-8
Reset		5-8
Interface		5-8
Requester		5-8
Interface		5-9
Interface		5-10
Handler		5.3 Interrupts
	5.3.1	VMEbus Interrupter/
	5.3.2	VMEbus Interrupt
Acknowledge		5-11
Sources		5-11
O		5-13
(SCC)		5.4 Programmable
Timer		5-13
Clock		5-13
Interface		5-14
Interface		5-14
5-14	5.4.8 Interrupt Handler (IHAN)	5-15
5.4.8	Reset	5-16

## Chapter 6. Settings

6.1 Jumper Locations 6-1 6.2 Jumper Functions  
 6-3 (W1) 6-3

6.2.1 Setting the Bus Grant Signal 6.2.2

Setting the Bus Request Signal 6.2.3

Setting the Bus Monitoring Time

6.2.4 Setting the Watch Dog Timer 6.2.5 Setting

the Bus Arbitration 6.2.6 Whether to Use the

IDE Bus (P2) 6.2.7 Selecting the

Battery 6.2.8 Setting the

SRAM Battery Backup

(W2) 6-4 (W3) 6-5

(W4) 6-5 (W5) 6-6 (W6,W9) 6-6 (W7) 6-7 (W8) 6-7 6.3 DIP Switches

6-8 6.3.1 Front DIP Switch Settings (DSW1) 6-8 6.3.2 Sta

7.1 Control Registers ..... 7-1 7.1.1 CNT1

Register ..... 7-2 7.1.2 CNT2

Register ..... 7-4 7.1.3 CNT3

Register ..... 7-5 7.1.4 CNT5

Register ..... 7-6 7.1.5 CNT6

Register ..... 7-7 7.1.6 CNT7

Register ..... 7-8 7.1.7 CNT9

Register ..... 7-8 7.1.8 CNT10

Register ..... 7-9 7.1.9 CNT11

Register ..... 7-9 7.1.10 CNT13

Register ..... 7-10 7.1.11 CNT14

register ..... 7-11 7.1.12 CNT15

register ..... 7-11 7.1.13 CNT17

register ..... 7-12 7.1.14 CNT19

register ..... 7-12 7.2 Status

Registers ..... 7-13 7.2.1 STAT0

register ..... 7-14 7.2.2 STAT1

register ..... 7-14 7.2.3 STAT2

register ..... 7-14 7.2.4 STAT3

register ..... 7-15 7.2.5 STAT4

register ..... 7-16 7.2.6 STAT5

register ..... 7-16 7.2.7 STAT6

register ..... 7-16

Chapter 8 Connector Pin Assignment 8.1

Connector Assignment yyyy-yy8-1

8.2.1 VMEbus Connector (P1, P2) yyyy-yyyyyyyyyyyy8-1

8.2.2 RS-232C Connector (CN1,CN2,CN3,CN4) yyyy-yyyy8-3

8.2.3 Ethernet Connector (LAN) yyyy-yyyyyyyyyy8-5

## Chapter 1 Precautions for Use

### 1.1 Handling of VMEbus modules (boards)

#### Where to Use or Store VMEbus Modules

Do not use this module in a location where it may come into contact with chemicals.

If objects are placed on the product, it may cause a short circuit, resulting in a fire or damage to the product or its structure.

Do not use this module in locations where it may be exposed to liquids such as water or oil, steam, or high humidity.

Do not use or store the product in this manner as it may cause malfunction.

Use and store this module on a flat and sturdy surface. Also, avoid vibration and shock.

Please do not add it.

Do not use or store this module in direct sunlight or near heating appliances such as fire or stoves, as this may cause malfunction or deformation.

Do not use or store this module in dusty locations.

Do not use this module near a television, radio, cordless telephone, etc. Noise may be introduced into the television, radio, or cordless telephone.

Do not use or store this module near devices that generate magnetic or radio waves.

This may cause the problem.

Do not place heavy objects on this module as this may cause it to break down.

Do not insert metal objects or other foreign objects into this module. If a foreign object gets into the module, the circuit may be damaged.

This may cause a short circuit and lead to a fire.

Do not allow water or other liquids to enter the module as this may result in electric shock.

Do not disassemble the battery pack or sub-battery. Disassembly may result in leakage of battery fluid.

Do not put the battery pack or sub-battery into a fire. It may explode or burst.

There are times when this happens.

Static electricity may cause the module to malfunction. When handling this module,

Please take sufficient anti-static measures, such as removing static electricity from your body.

## Chapter 1 Precautions for Use

When replacing the ROM on this module, please use the special tool. If you try to remove it by force,

Doing so may damage the module, corrupt the ROM, or even cause injury.

When inserting or removing the jumpers/shunts on this module, use tools such as tweezers to avoid injury. Also,

make sure to set the jumpers/shunts correctly as shown in this manual.

When handling this module, you may cut your hands or other parts of your body on the front or back of the module.

So please be careful.

If a module with a battery is placed on a metal surface, it may discharge or generate heat.

Keep it in a protective bag to avoid direct contact with metal surfaces.

## Precautions when using VMEbus modules in a rack

When installing or removing this module from the system rack, be sure to unplug the power cable from the system rack beforehand, as this may cause electric shock.

When installing this module in our VMEbus system rack (installing the module in the second or subsequent slots from the left of the VMEbus backplane), be sure to remove the corresponding jumpers and shunts on the VMEbus backplane. This can cause a malfunction.

Module installation procedure precautions

a) Check that the jumpers on this module are set correctly. b) Turn off the power to the VME system (rack side) and remove all jumpers (BG0, BG1, BG3, IACK jumpers) on the VME backplane that corresponds to the VME slot where you plan to install this module. (When using a backplane manufactured by our company, the relationship between the slots and jumpers is as shown in Figure 1-2.) c) Insert this module into the slot you will be using

(Figure 1-1). At this time, insert it straight along the rails to avoid damaging the parts on the module. Also, push it in firmly so that the connector of the inserted module and the connector of the backplane in the rack are properly connected. (After inserting the module, securely fix it with the screws shown in Figure 1-3.)

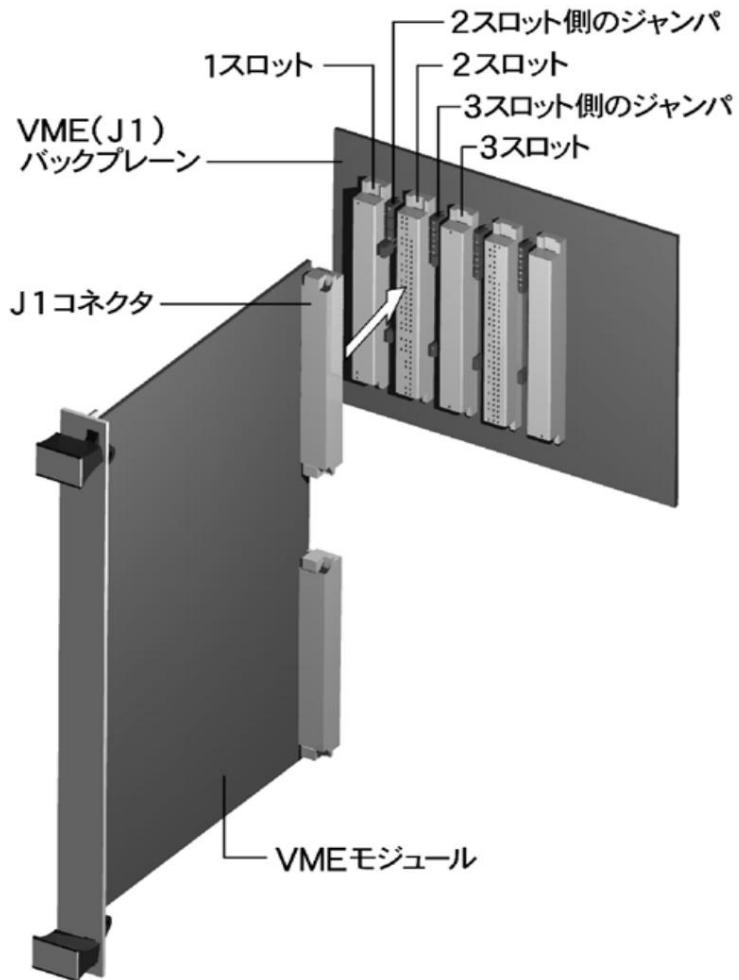


Figure 1-1

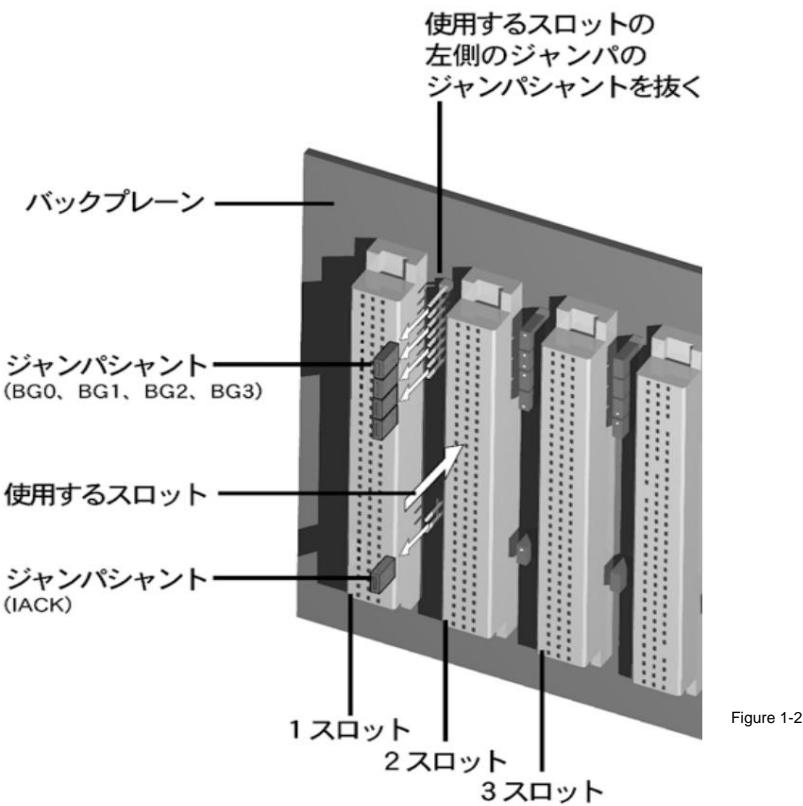


Figure 1-2

## Chapter 1 Precautions for Use

- d) After confirming that the modules are installed in the rack as described above, turn on the system power and check that it is working properly.

ŷ Precautions when removing modules

- a) Be sure to turn off the power to the VME system rack before removing the module. Otherwise, it may cause a malfunction.
- b) Remove the screws shown in Figure 1-3 and insert the ejector as shown in Figure 1-4.
- Pushing the connector handles up and down will release the module from the connector and allow you to remove it from the slot without forcing it out. Forcing the module out can damage the module and/or the rack.

ŷ If the system does not operate even after the VME module is installed in the system rack, this may be because the specified jumper/shunt on the VME backplane on the rack side is not removed (or a jumper/shunt other than the specified one is removed), or the module side is not set correctly. If these settings are not made correctly, it may cause damage to the module.

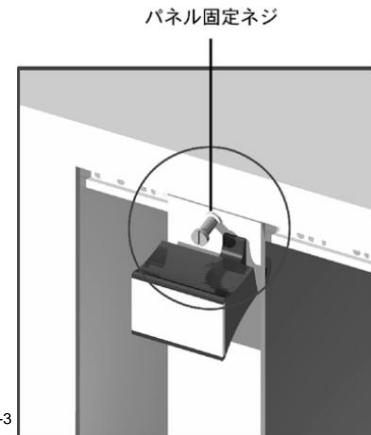


Figure 1-3

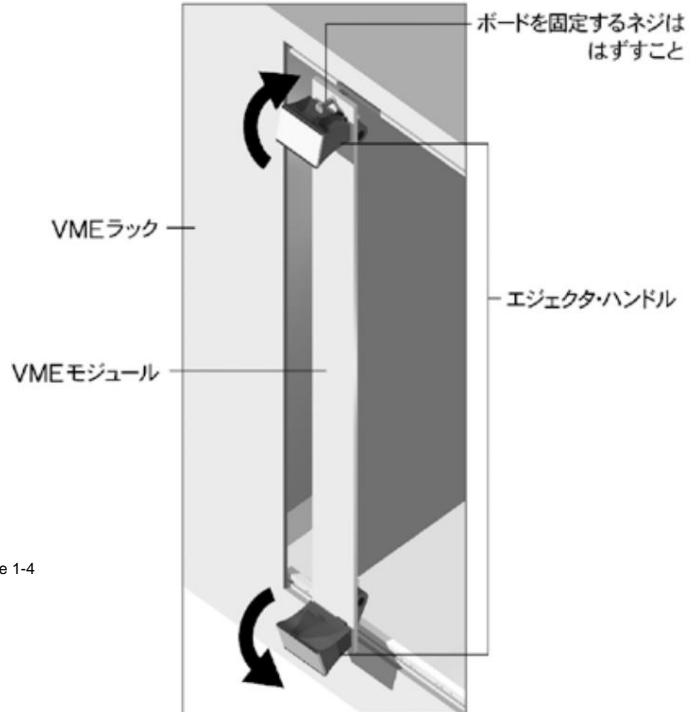


Figure 1-4

## VMEbus System Rack Handling Precautions

- ŷ When connecting cables, organize them carefully to avoid tripping over them.  
Tripping over loose cables can cause damage or malfunction to the VMEbus system rack or modules.

- ŷ Do not step on or bend cables. This can cause the cables to break and lead to malfunctions.

There are times when this happens.

ÿIf you will not be using the device for a long period of time, for safety reasons, unplug the power cord from the AC outlet.

stomach.

ÿPlease connect the power cord of the device to a different AC outlet from that of the TV, radio, etc.

Using a C-type outlet may result in noise being produced to televisions, radios, etc.

ÿDo not leave rubber or vinyl products in contact with the VMEbus System Rack for long periods of time, as this may cause the surface of the unit to deteriorate or the paint to peel off.

ÿ Never place heavy objects on the power cord. Placing heavy objects on the power cord may damage the cord.

Doing so may result in electric shock or cause a fire.

ÿ When unplugging the power cord from the AC outlet, always pull on the plug.

Doing so may result in a broken wire and cause a fire.

ÿTo prevent any danger, please make sure that children do not touch the cables.

## 1.2 Aftercare

Please send us your user registration card. Please fill  
in the required information on the user registration card and be sure to mail it to us.

### What to do if a malfunction or abnormality occurs

If the module experiences any of the following malfunctions or abnormalities, immediately turn off the power to the device and unplug the power cord from the AC outlet.

- A) If smoke or an unusual odor comes from the device
- B) If the device becomes too hot to touch
- C) If the device makes an abnormal noise
- D) If the application you are using malfunctions

If you experience a malfunction or abnormality, please contact your retailer or our service center.

Before you contact us If you

are consulting about a module failure or abnormality, please check the following in advance.

- A) Please check the model name and serial number.
  - B) Please prepare the module warranty card.
  - C) Make a brief note of the malfunction or abnormality.
  - D) Note the environment in which the module is used (both hardware and software)
- Please do.
- E) Please prepare the module manual.

## Chapter 1 Precautions for Use

Contact (service window) Aval

Data Co., Ltd. Sales Division 2 1-25-10 Asahi-cho,

Machida-shi, Tokyo TEL: 042-732-1030 (Hours:

Monday to Friday, 9:00am to 5:00pm) FAX: 042-732-1032 (Fax is also accepted outside of the above

hours. Please fill out the form with your questions and inquiries and contact us.

Please send it.)

## Repurchasing the manual

If you have lost this manual, you can purchase it again from your place of purchase or from our company. Please make a note of the product name and model number in case you lose the manual.

About repair and maintenance service •About

warranty card If the product

breaks down during the warranty period, we will repair it according to the warranty card. For details, please refer to the warranty card.

Please see the book.

### • Regarding repair parts

Replacement parts for this product will be available for a minimum of five years after production is discontinued.

## When transferring this product to a third party

### A. To the Transferring User

If this product is transferred to a third party, the following conditions must be met:

a) Transfer all items attached to the module (instruction manual, warranty, accessories, etc.)

Not to retain any copies

a) You agree to comply with the conditions regarding the transfer or assignment of the software's terms of use that accompany each software.

What we do

C) Software that is not permitted to be transferred or assigned must be deleted before being assigned or assigned.

### B. To the User Receiving the Transfer

We may send you notifications from us, so please be sure to inform us of any items required to change your user registration information.

Items required for

registration: a) Warranty number and product name, model number, and serial

number b) Name, company name, address, and phone number of the previous user, or name, address, and phone number of the store

where you purchased the second-hand item

Registration address

〒194-0023

1-25-10 Asahi-cho, Machida-shi, Tokyo  
Aval Data Co., Ltd. Head Office/Machida  
Office Sales Department 2

### 1.3 How to dispose of the module

When disposing of the module, please dispose of it in accordance with the local government regulations.

Please contact the local government.

### 1.4 Handling of lithium batteries

Please take note of the following points when handling the lithium battery used in this module.

#### Precautions when disposing

A) Insulate the battery by applying insulating tape to both the positive and negative terminals, then dispose of it as "general non-burnable waste."

Please dispose of them in units of a few pieces.

B) Do not throw batteries into a fire or incinerate them in an incinerator, as they may explode or catch fire. c) Do not dispose of batteries carelessly mixed with general waste or together with conductive objects such as metal pieces.

Doing so may result in fire or explosion.

d) If you are disposing of a large amount of batteries, we recommend that you entrust it to a specialized waste disposal company. e) If you are unsure of the disposal method, please contact the battery manufacturer.

#### Other notes

To prevent batteries from being swallowed accidentally, keep them out of the reach of small children.

If swallowed, consult a doctor immediately.

Chapter 1 Precautions for Use

<memo>

### ŷ Description

This section explains how to use the AVME-148 module. The numerical notation is defined as follows:  
I will.

\$: Displays hexadecimal numbers.

%: Displays binary numbers. No

mark: Displays decimal numbers. \* in

a signal name means that the signal is active LOW and true or enabled. The terms "assert" and  
"negate" are used to describe the state of a signal. This refers to the voltage level of the signal .

Regardless of whether the signal is High or Low, it is asserted when the signal is active (true) and asserted when it is not active (false).  
(meaning "negate")

## Chapter 2 Overview

### 2.1 Overview

The AVME-148 is equipped with a 32-bit microprocessor 68040MPU and is connected to both the local bus and VMEbus ports.  
A large-capacity dual-port access memory that can be accessed from any  
This MPU module is compatible with our AVME-140 series and prioritizes performance.

This

module is equipped with 32MByte of dual port memory.

There is a 512KByte system ROM area using SRAM and Flash Memory, and a 4MByte extended ROM area.

The interface includes 4 channels of RS232C (using 8-pole modular connectors), 10BaseT Ethernet,  
Equipped with an IDE and FDD interface, a system can be constructed using just this module.

Multi-MPU systems can use round-robin or priority-based bus arbitration.

It is possible to set one level of interrupt request.

In addition, the system bus can access the VMEbus (A32/D32, A24/D16), allowing users to use a variety of systems.

This MPU module is designed with a focus on maximum speed and multiple functions while taking into consideration the system configuration.

## 2.2 Features of AVME-148

Features of the AVME-148 include:

a) The MPU is 68040/25MHz.

b) The dual-port memory is 32MB. c)

The MPU access cycle for the dual-port memory is 4 clocks.

Supports burst transfer (4:2:2:2) d)

Equipped with one 32-pin Flash Memory IC socket

e) Built-in 512KByte SRAM with battery backup f) Built-in

4MByte expansion Flash Memory g)

Battery-backed real-time clock h) 4-channel RS232C serial

port (asynchronous/8-pole modular) i) Built-in CompactFlash interface j)

Built-in Ethernet interface (10BaseT) k) Built-in IDE

and FDD interfaces l) Built-in VMEbus system

controller function m) VMEbus

interrupter n) VMEbus requester o) Supports

VMEbus master interface

(A32/D32, A24/D16,

A16/D16) p) Supports VMEbus slave interface (A32/D32/D16/D8) q) Built-

in watchdog timer r) RESET on front panel and ABORT switches

s) RUN, HALT, FAIL, and SCON

LEDs on the front panel t) Built-in 16-bit programmable

timer u) Low battery voltage detection function v) Upward

hardware compatibility with the AVME-140

series and AVME-130.

## 2.3 Specifications

The specifications of AVME-148 are shown in Table 2-1.

Table 2-1 AVME-148 Specifications

Term	eye	specification
MPU		MC68040/25MHz
Dual Port Memory		32MB (EDODRAM, 60ns product) Accessible via MPU/VMEbus
Access from MPU to EDODRAM 1 cycle 4 clocks		Burst mode support (4:2:2:2) Implemented only
Snooping Function		with on-board dual port memory
Local Memory System		
ROM		MBM29F040C-90PD (Fujitsu) equivalent ... 1 x 32-pin IC socket (D8) (512KByte: when using 4Mbit Flash Memory)
Flash Memory		4Mbyte...MBM29F080A-90PFTN equivalent 4 pieces (D32)
SRAM		512KByte - Battery backup possible (D8) 16-bit programmable
Programmable Timer		timer MSM82C54 (Oki Electric) Clock: 4MHz Time:
Watchdog Timer		500mS and 1S
Real Time Clock Serial Port		FDC37C935 (SMSC) - Battery backup RS232C 4 channels
		(asynchronous/8-pole modular) FDC37C935 (SMSC) Clock: 14.318MHz MAX 19.2KBPS PC16552DV (NS) Clock: 1.8432MHz MAX 19.2KBPS FDC37C935 (SMSC) Clock: 14.318MHz FDC37C935 (SMSC)
FDC		Clock: 14.318MHz 10/100 Base Tx Interface
IDE		AX88796L (ASIX) Clock: 25MHz VMEbus REV.C.1
Ethernet		compliant A32/A24/A16 D32/D16/D8 RMW possible, UAT bus request signals BR0* to 3*
VMEbus		available Two types of signals: Release on request (ROR) and Release when down
VMEbus Requester		(RWD) Mode selectable
VMEbus Release		
VMEbus Interrupter		Vectored interrupts available for VMEbus (IRQ1* to IRQ7* )

Table 2-1 AVME-148 Specifications (continued)

Interrupt Handler	VMEbus interrupts IRQ1* to IRQ7* (specially vectored) Local interrupts LRQ1* to LRQ7* (specially vectored) (specially vectored) ACFAIL*, SYSFAIL*
VMEbus System Controller VMEbus Arbiter	Round-robin/Priority  IACK Daisy Chain Driver System Clock Driver (SYSCLK)  VMEbus Watchdog Timer  System Reset (SYSRESET*)
Panel Switches	RESET switch, ABORT switch, DIP switch (DSW1)
LED display	RUN (green), HALT (red), FAIL (red), SCON (green)
Power supply	+5Vdc +0.25V/-0.125V 2.2A(typ)  +5Vdc Standby +0.25V/-0.125V Operating
Environmental conditions	temperature 0 to 45°C (under forced air cooling)  Storage temperature 0 to 55°C Humidity 35% to 85% (non-condensing)
Board Size	233.4mm(W), 160mm(D)
Panel Width	20mm
weight	380g

#### 2.4 Cooling conditions

The AVME-148 is a standard enclosure for our company, with the board under test and a 30W load board inserted in the adjacent slot, forcing it has been confirmed that the device operates normally in an ambient temperature range of 0 to 45°C with air cooling. The required airflow for cooling is 10CFM and 200LFM or more per slot. You can do this.

The amount of air flowing over the module varies depending on the chassis structure, board shape, and location.

For conversion of air volume and wind speed, please refer to the following:

$$10\text{CFM} = 0.2831 \text{ m}^3/\text{min} \text{ per slot (ft}^3/\text{min)}$$

$$200\text{LFM} = 1.018 \text{ meter/S}$$

CFM = Cubic Feet per Minute

LFM = Linear Feet per Minute

## 2.5 Configuration

A simplified block diagram of the AVME-148 is shown in Figure 2-1.

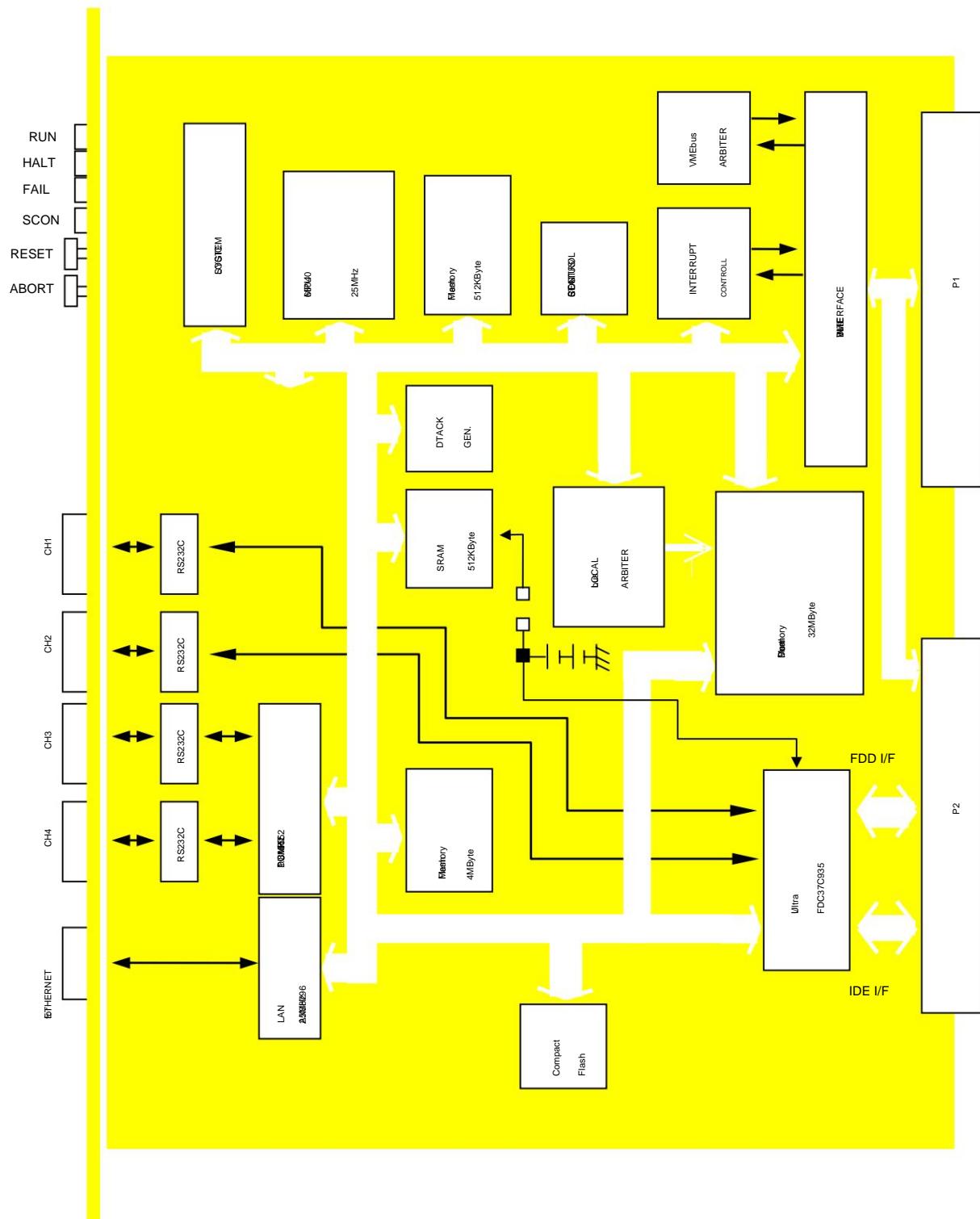


Figure 2-1 AVME-148 block diagram

## 2.6 Summary memory map

A simplified memory map of the AVME-148 is shown in Figure 2-2.

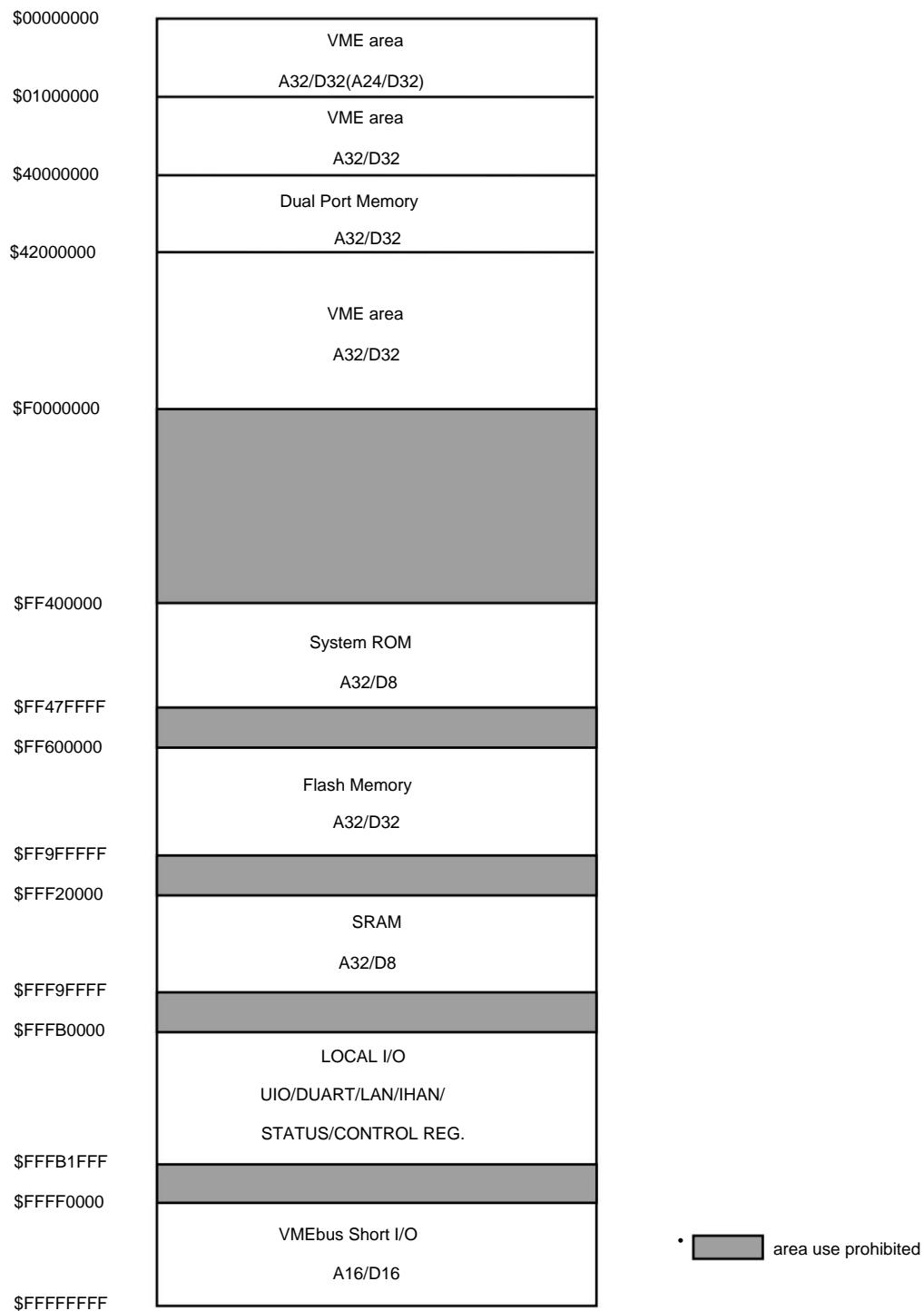


Figure 2-2. AVME-148 Simplified Memory Map

## Chapter 2 Overview

## 2.7 Component Layout

The parts layout of the AVME-148 is shown in Figure 2-3 and Figure 2-4.

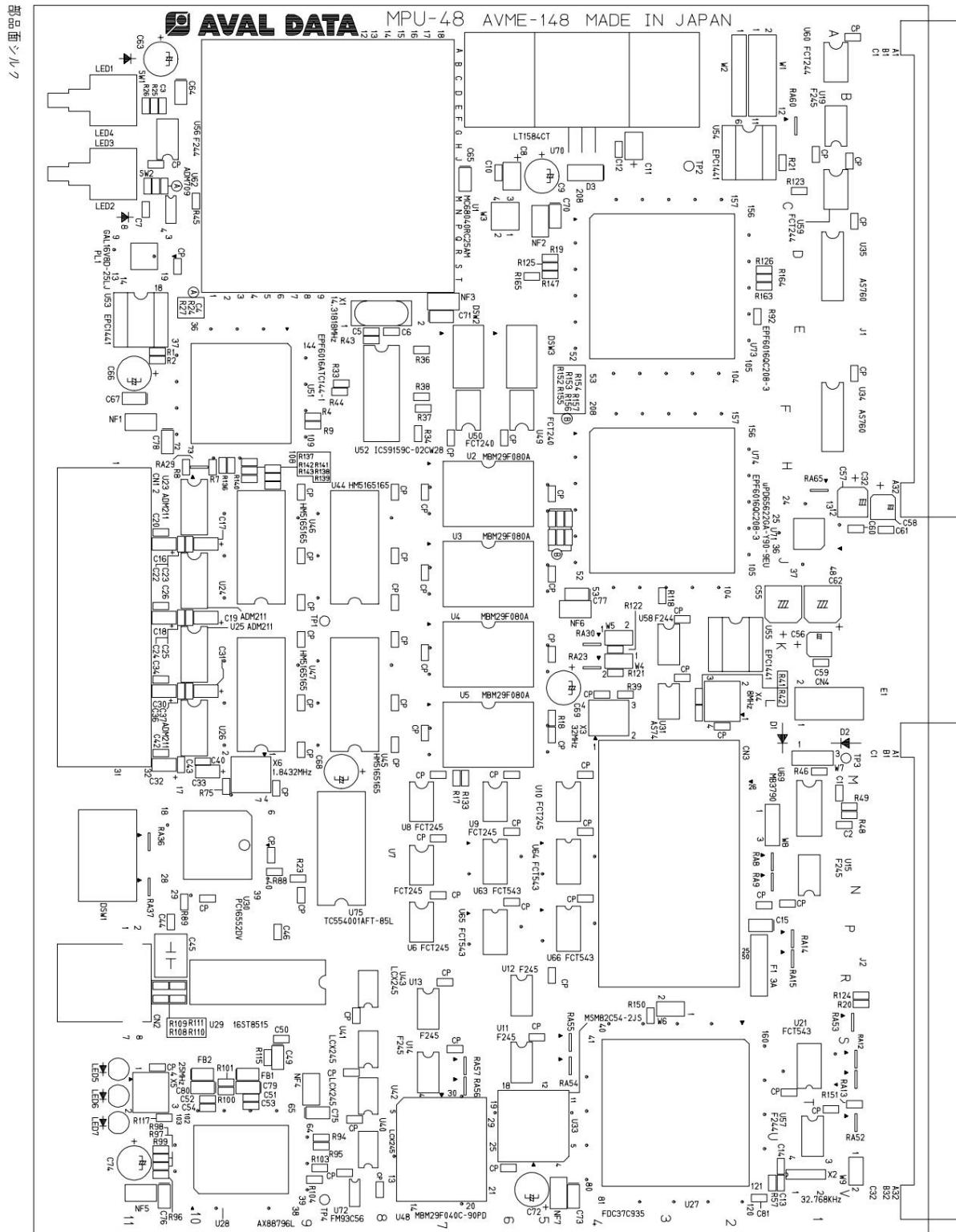


Figure 2-3 AVME-148 component layout diagram

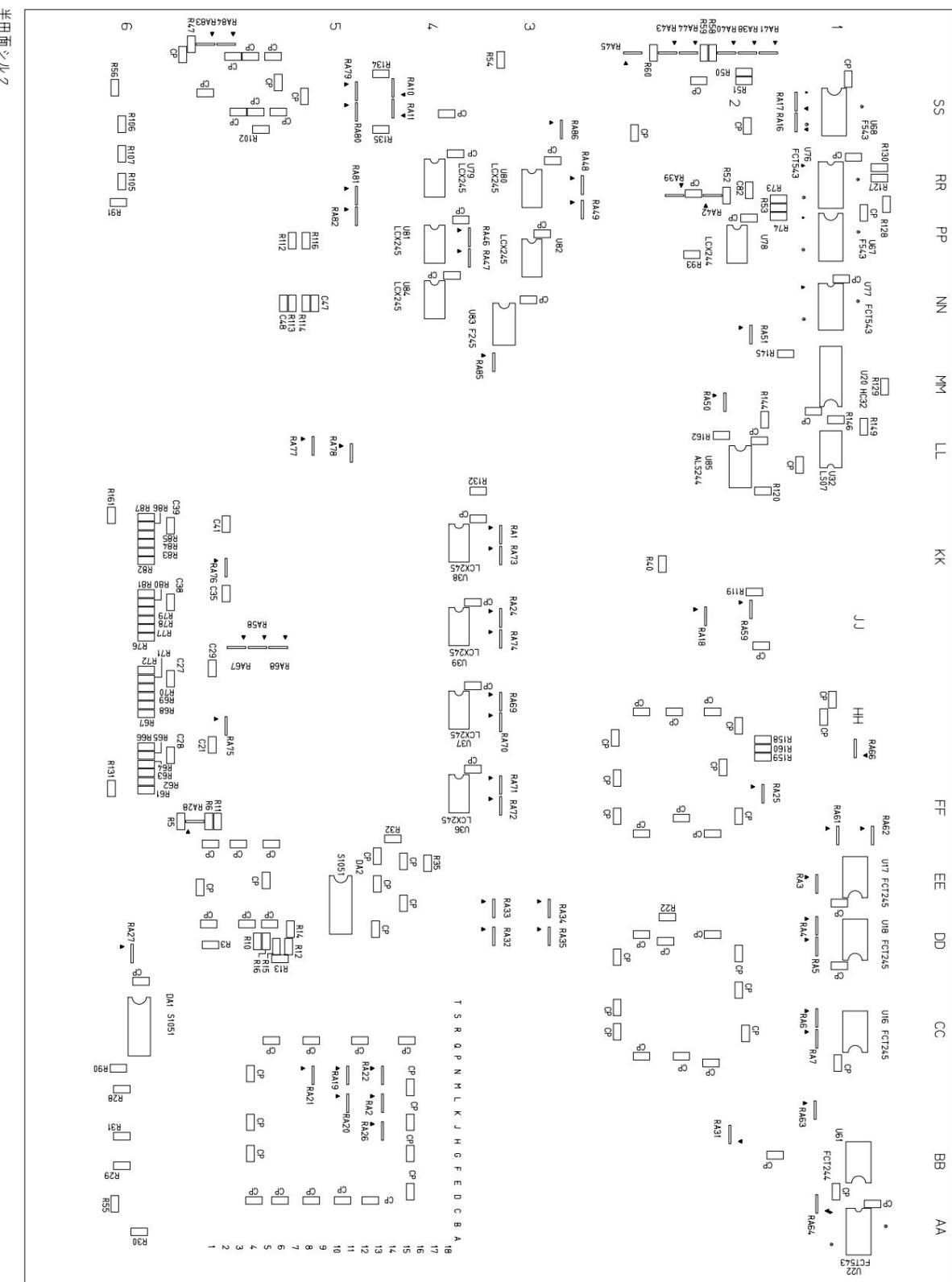


Figure 2-4 AVME-148 Solder Side Component Layout

## 2.8 System ROM layout

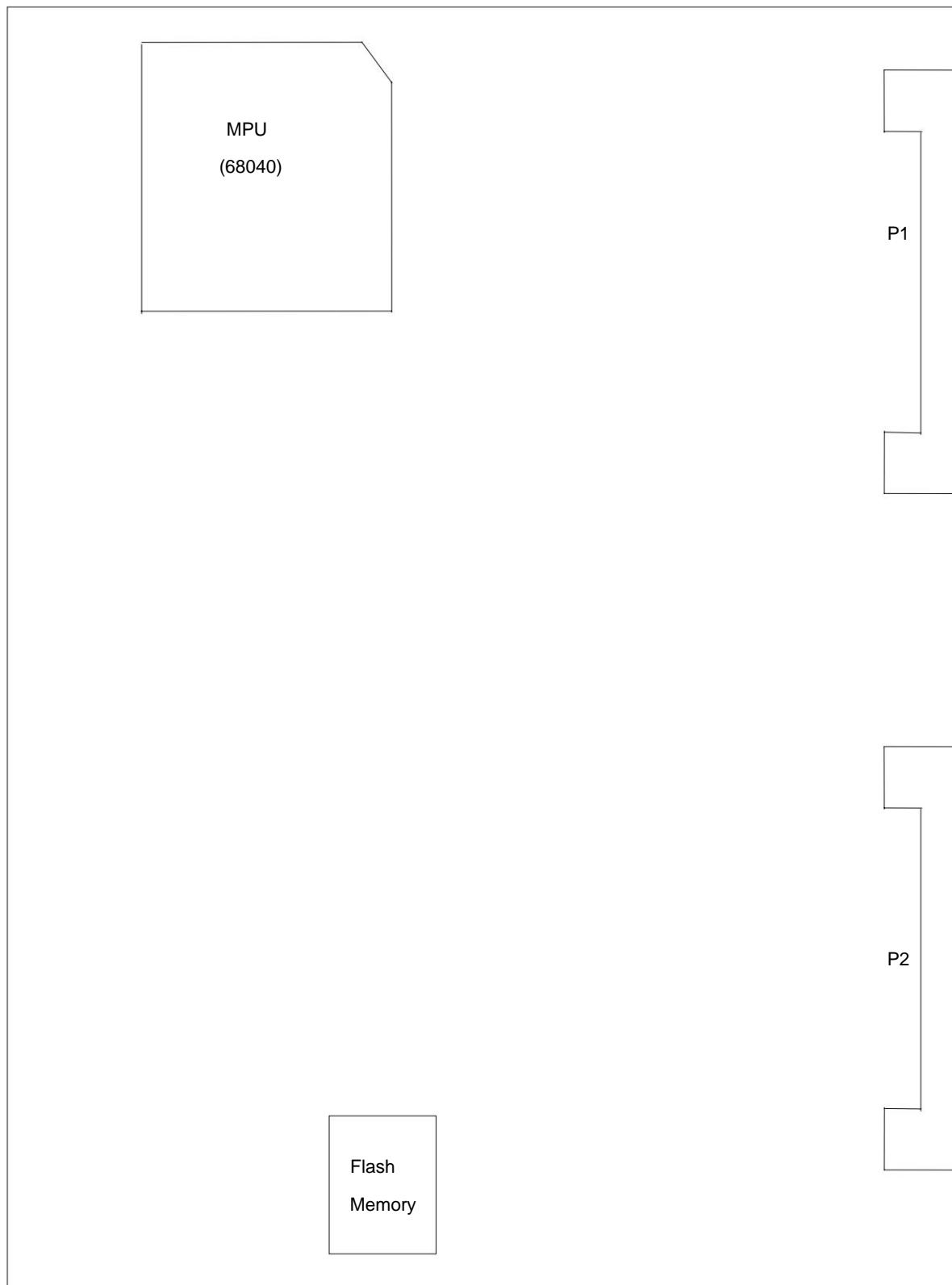


Figure 2-5 System ROM layout

## 2.9 Related Documents

For technical documents other than the user's manual for this module and detailed manuals for each device, Table 2-2 lists related documents.

Table 2-2 Related

Documents	Document Name	Manufacturer	VMEbus Architecture
Manual REVISION C.1	Motorola MC68040 32-bit Microprocessor User's Manual	Motorola	Ultra I/O
(FDC37C93X) Data Sheet	PC16552DV Data Sheet	AX88796L Data Sheet	PD65622GA-Y90-9EV
IHAN Data Sheet		SMSC	
		NS Company	
		ASIX	
		Aval Data	

<memo>

## Chapter 3 Memory Map

This section describes the memory map of the AVME-148.

### 3.1 AVME-148 Memory Map

The memory map seen by the 68040MPU ranges from \$00000000 to \$FFFFFF, with each space being finely defined. The memory map seen from the MPU is shown in Table 3-1.

Table 3-1 AVME-148 Memory Map

Address range	Access area	Address size	Data port Size	Hardware cache Inhibit	Burst Transfer	
\$00000000 ~\$00FFFFFF	VMEbus	A32/A24	D32/D16	Yes	No. Caution 1)	
\$01000000 ~\$3FFFFFFF	VMEbus	A32	D32	Yes	No	
\$40000000 ~\$41FFFFFF	On Board	A32	D32	No	Yes	
\$42000000 ~\$EFFFFFFF	VMEbus	A32	D32	Yes	No	
\$F0000000 - \$FF3FFFFF	Reserve	-	-	-	-	
\$FF400000 - \$FF47FFFF	System ROM	A32	D8	Yes	No Note 2)	
\$FF480000 - \$FF5FFFFFF	Reserve	-	-	-	-	
\$FF600000 - \$FF9FFFFFF	Flash Memory	A32	D32	Yes	No	
\$FFA00000 - \$FFF1FFFF	Reserve	-	-	-	-	
\$FFF20000 - \$FFF9FFFF	SRAM	A32	D8	No	No	
\$FFFA0000 - \$FFF9FFFF	Reserve	-	-	-	-	
\$FFFFB0000 - \$FFFFB1FFF	Local I/O	A32	D32/D16/D8	Yes	No. Caution 3)	
\$FFFFB2000 - \$FFFFEFFFF	Reserve	-	-	-	-	
\$FFFF0000 - \$FFFFFFFFF	VMEbus Short I/O	A16	D16	Yes	No	

Chapter 3 Memory Map

Note:

- 1) A24/D16 address and data port size change the control register of AVME-148

This is possible by doing the following. At reset, the size is set to A32/D32.

If the VMEbus slave board can only be accessed by A24 or D16, it can be used by placing it in this space and setting it to A24/D16. It can also be used by A24/D32.

- 2) In the first two cycles after reset, 8 bytes are forcibly read from address 0 of the system ROM, and subsequent addresses are accessed according to the MPU memory map.

The 8 bytes from address 0 of the EPROM are always used as the initial interrupt stack pointer (ISP) and the

It is necessary to store the logical program counter (PC) information in the

- 3) Data port size varies depending on local I/O. 4) Cache inhibited space by hardware is enabled by software.

Please do not do so.

- 5) Make sure that the MOVE16 command to the VMEbus is executed from the boundary address of '\$0, \$10...'.

### 3.2 System ROM Memory Map

The system ROM uses Flash Memory with a data width of 8 bits.

The range is secured from \$FF400000 to \$FF47FFFF.

The address map of the system ROM is shown in Table 3-2.

The system ROM is hard-forced for the first two cycles at power-on or system reset.

The data is read from the top of the MPU and the interrupt stack pointer (ISP) and program counter are set.

The program is then executed from the address indicated by the program counter.

Therefore, the first 8 bytes of the system ROM contain the initial interrupt stack pointer and the

You must store the value of the global program counter.

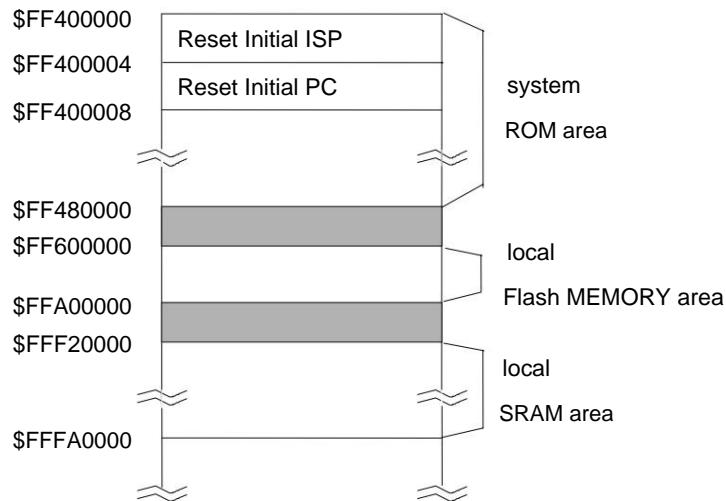


Table 3-2 System ROM Address Map

### 3.3 Local I/O Memory Map

A detailed map of the local I/O portion of the AVME-148 memory map (Table 3-1) is shown in Table 3-3.

Table 3-3 Local I/O Memory Map

Start address	End address	Name	Explanation	Size	Device
\$FFFB0000	\$FFFB0003	Timer	Programmable Timer	D8	MSM82C54
\$FFFB0020	\$FFFB0043	Status/Control	Board Status/Control	D32, D16, D8	FPGAs, DSW1, DSW2
\$FFFB0080	\$FFFB008F	IHAN	Interrupt Handler	D8	UPD65622GA-Y90-9EV
\$FFFB0100	\$FFFB0107	DUART	DUART COM2	D8	PC16552
\$FFFB0108	\$FFFB010F	DUART	DUART COM1	D8	PC16552
\$FFFB0600	\$FFFB061F	LAN	Ethernet	D16	AX88796
\$FFFB1070	\$FFFB1071	RTC	Real Time Clock	D8	FDC37C935
\$FFFB1300	\$FFFB1307	FDC	Floppy Disk Controller	D8	FDC37C935
\$FFFB1320	\$FFFB1327	UART1	Serial Port COM1	D8	FDC37C935
\$FFFB1330	\$FFFB1337	UART2	Serial Port COM2	D8	FDC37C935
\$FFFB1340	\$FFFB1347	IDE1	IDE1 Task File Register	D8, D16	
\$FFFB134E		IDE1	IDE1 Misc AT Register	D8	
\$FFFB1350	\$FFFB1357	IDE2	IDE2 Task File Register	D8, D16	
\$FFFB135E		IDE2	IDE2 Misc AT Register	D8	
\$FFFB13F0		Ultra I/O	Config Port	D8	FDC37C935
\$FFFB13F1		Ultra I/O	Data Port	D8	FDC37C935

Note:

1) I/O access is guaranteed only at the data port size of the specified address. 2) For detailed explanations of each register bit, refer to the data sheet of each chip.

### 3.4 VMEbus Memory Map

This section describes the AVME-148 dual-port memory map as seen by the VMEbus master.

The dual-port memory of the AVME-148 is located in the extended space.

The dual port memory address is determined by DSW1 bits 5 and 6 as seen from the VMEbus.

You can change the start address of the map. When you install the VMEbus address in the system,

If it overlaps with the Reve, you will need to place it in a separate space by setting the dip switch.

The AVME-148 also allows the on-board dual-port memory to be accessed from the VMEbus address space.

It is not possible to do so.

The memory map as seen from the VMEbus is shown in Table 3-4.

Table 3-4 Memory map as seen from the VMEbus

DSW1 Address Range	Address Size	Data Port Size
No. 5 No. 6 A VME-148		
OFF OFF	\$40000000 ~\$41FFFFFF	
OFF ON	\$42000000 ~\$43FFFFFF	A32
ON OFF	\$44000000 ~\$45FFFFFF	D32
ON ON	\$46000000 ~\$47FFFFFF	

Notes:

- 1) Dual port memory can only be accessed with A32 extended addresses.

In this case, the VMEbus address modifier lines (AM0 to AM5) must be the extended address AM codes \$0E, \$0D, \$0A, or \$09.

- 2) Data port sizes that can be accessed are D32, D16, and D8.

### 3.5 VMEbus Short I/O Memory Map

This section explains the VMEbus short I/O memory space of the AVME-148. This space is 64KByte.

The addresses on the VMEbus side are A1 to A15. The data width can be accessed in 16/8 bits.

It's Noh.

The VMEbus short I/O memory map is shown in Table 3-5.

Table 3-5 VMEbus Short I/O Memory Map

Address Access area	AM code	Address size	Data port size	
\$FFFF0000 - \$FFFFFF	VMEbus Short I/O	\$2D or \$29	A16	D16

Note:

If 32-bit access is performed to the short I/O space, it will be changed to 16-bit access by the hardware.

## Chapter 4 Front Panel

### 4.1 Front Panel, Switches and Indicators

This section describes the switches and indicators on the front panel of the AVME-148.

#### 4.1.1 Front Panel DIP Switches

The 6-pole DIP switch on the front panel controls the system controller selection and the RESET/ABORT Switches, enable/disable VMEbus timer and local bus timer, and read/write memory addresses from the VMEbus. There is a selection feature.

The RESET switch resets all on-board devices while it is pressed, and the module is ready to use.

If the system controller is a SYSRESET\* signal, it also drives SYSRESET\*.

When the ABORT switch is pressed, it generates a local interrupt to the MPU with level

7. There are four LED indicators: RUN, HALT, FAIL, and SCON.

RUN is lit when a local bus cycle is being performed by the local MPU, LAN, DMA, or VMEbus.

HALT is lit when the 68040MPU is in halt status, and FAIL is BDFAIL\* in the control register (CNT1).

When the bit is LOW, the LED is lit. When the SCON LED is LOW, the LED is lit.

It lights up.

For the DIP switch settings, see 4.2 Front DIP Switch Settings.

#### 4.1.2 Front panel appearance

The front panel of the AVME-148 is shown in Figure 4-1.

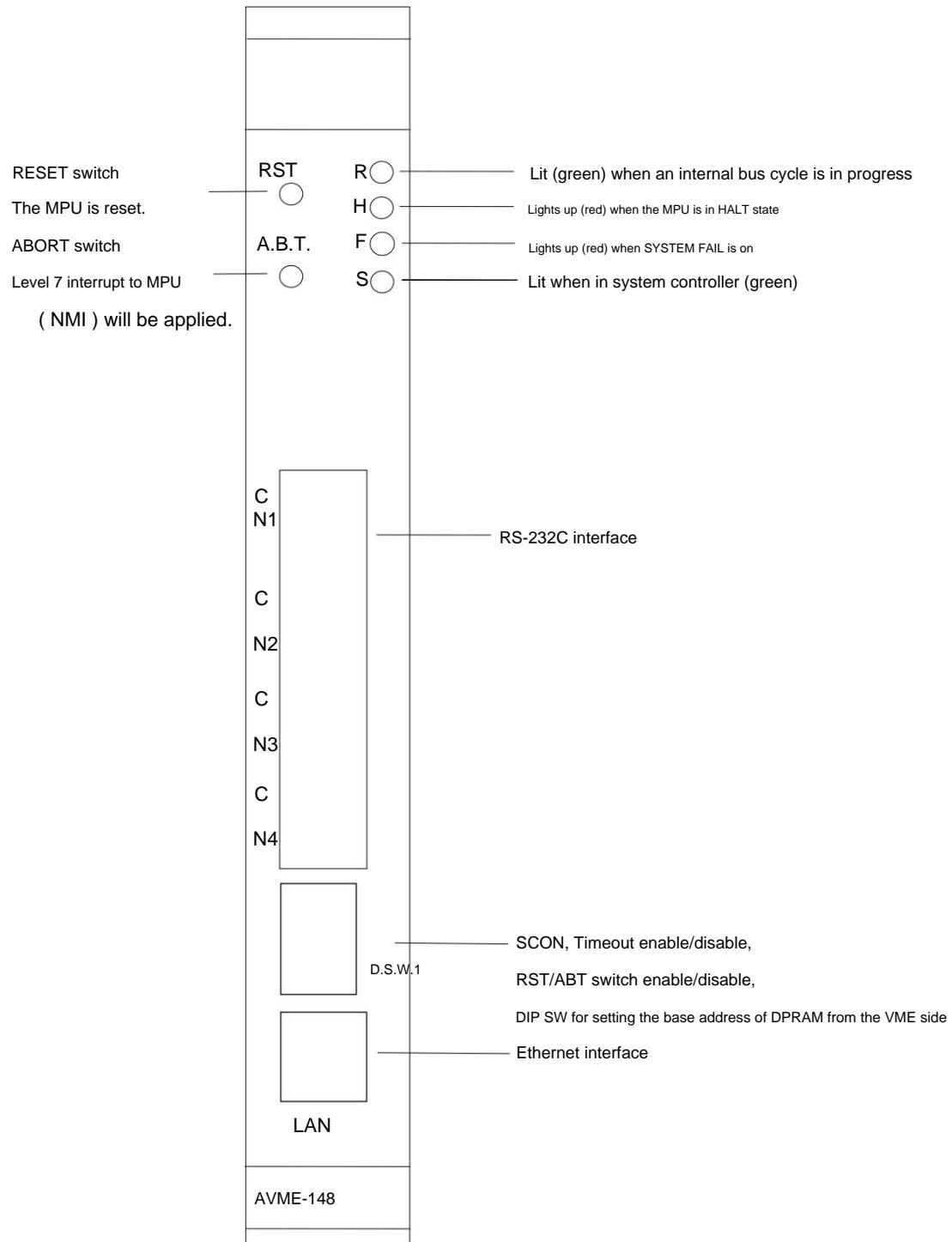


Figure 4-1 Front panel overview

#### 4.1.3 RESET switch (SW1)

The RESET switch (SW1) on the front panel is enabled when DSW1-2 is ON and resets the local bus. Run the set.

In addition, if the system controller is specified (DSW1-1 is ON), the SYSRES\* signal of the VMEbus is also driven. The reset signal is asserted while the switch is pressed down.

#### 4.1.4 ABORT switch (SW2)

The ABORT switch (SW2) on the front panel is enabled when DSW1-2 is ON, is connected to the NMI\* terminal of the interrupt handler (IHAN), and generates a local interrupt of level 7 to the MPU through IHAN. At this time, it is necessary to program the device to obtain the interrupt status ID information from IHAN.

It is also possible to mask IHAN interrupts by program. The switch is a push type that asserts the NMI\* input signal when pressed .

#### 4.1.5 RUN indicator (DS1)

The green LED (DS1) marked with "R" is connected to the local address strobe signal and indicates the execution status of each bus cycle of the local bus, LAN (AX88796), and DMA, as well as the access status from the VMEbus side. Display.

#### 4.1.6 HALT indicator (DS2)

The red LED (DS2) showing "H" decodes the PSTn signal of the MPU and indicates the HALT status. Sometimes it lights up.

#### 4.1.7 FAIL Indicator (DS3)

The red LED (DS3) marked with an "F" is connected to the BDFAIL\* bit in the control register and indicates its status. This bit is controlled by the program. This signal is also asserted during a reset, so the LED is lit. When lit, the SYSFAIL\* bit on the VMEbus is The signal is also driven.

Chapter 4 Front Panel

#### 4.1.8 SCON indicator (DS4)

The green LED marked "S" (DS4) indicates that the module is selected as the system controller.

Indicates that you are

Notes:

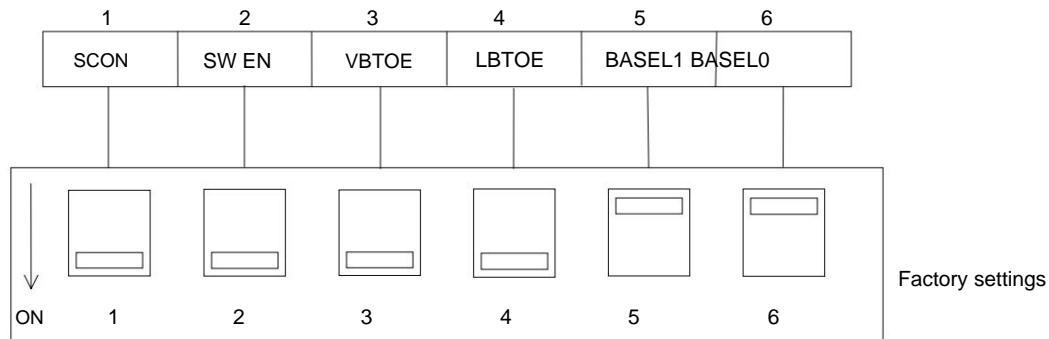
- 1) When used as a system controller, it must be installed in the first slot of the system.  
It must be.
- 2) When using two or more of these modules in one system, the SCON LEDs of all slots other than the first slot will light up.  
I will try not to do so.

## 4.2 Front DIP Switch Settings (DSW1)

The DIP switch DSW1 is used to set the functions of this module and is set when the module is installed in the system.

There are DIP switches on the front panel to allow this to be changed.

The configuration of DSW1 is as follows:



### 1) SCON (System Controller)

This bit makes this module a system controller.

ON : valid

OFF: Disabled

### 2) SW EN (Switch Enable)

This bit enables/disables the RESET and ABORT switches on the front panel.

ON : valid

OFF: Disabled

### 3) VBTOE (VMEbus Time Out Enable)

This bit enables/disables the VMEbus watchdog timer of this module. However, if SCON is not ON, the setting is invalid.

ON : valid

OFF: Disabled

## Chapter 4 Front Panel

## 4) LBTOE (Local Bus Timeout Enable)

This bit enables/disables the local bus watchdog timer in this module.

ON : valid

OFF: Disabled

## 5) BASEL1, BASEL0 (Base Address Select 1,0)

This bit changes the base address of the dual port memory as seen from the VMEbus side.

BASEL 1	BASEL 0 starting address	
OFF	OFF	\$40000000
OFF	ON	\$42000000
ON	OFF	\$44000000
ON	ON	\$46000000

\$ displays hexadecimal

Notes:

- 1) Dual port memory can only be accessed from the VMEbus using extended addresses. 2) An address space equal to the size of the installed memory capacity is allocated from the selected start address.

## Chapter 5 Functions

## 5.1 Functionality

## 5.1.1 MPU

The 68040MPU has 4KByte independent instruction and data caches, a memory management unit (MMU), It integrates a floating-point unit (FPU) on a single chip. It also supports snooping function. This allows for better caching functionality.

For details, refer to the MC68040 32-bit Microprocessor User's Manual. Note that the user page attribute (UPA1, UPA0) pins are not used in this module.

## 5.1.2 Multiport Arbiter

To access the DPRAM, the LAN, FDC, VMEbus, and MPU must request and be granted the right to use the local bus. Those who get the pass will have access to the memory.

Once the MPU has been granted the bus, it will not release it until another bus request is made. The DPRAM refresh operation has priority over any other master.

## 5.1.3 Dual Port Memory (DPRAM)

The access to the dual-port memory from the 68040MPU, VMEbus master, LAN, and FDC is as follows: It can be implemented with bit widths of D32/D16/D8, D32/D16/D8, D16, and D8. In addition, it uses EDODRAM as the memory element. If these requests occur simultaneously, the following priority order is given:

The DPRAM is accessed in the

If a request occurs from a higher priority during a DPRAM access, the bus

The usage right of the higher priority node is transferred to the higher priority node.

Only access from the 68040MPU to the DPRAM supports burst transfers, allowing very fast data transfer.

Data transfer is now possible.

Table 5-1 DPRAM access priority

Priority DPRAM	Access Refresh
1	Request
2	LAN (AX88796)
3	FDC (FDC37C935)
4	VMEbus Master
5	68040 MPU

### 5.1.3.1 Access to DPRAM from the MPU

The local bus usage requested by the 68040MPU to the multiport arbiter to access the DPRAM.

If permission is granted, a read or write cycle is performed.

If another DPRAM access occurs during this cycle, the request is not processed until the cycle is completed.

I'll keep you waiting.

However, the MPU does not receive requests from other sources during read-modify-write cycles or burst transfer cycles.

If a request occurs, it will wait until the cycle is complete.

For memory access times, see the table below.

Table 5-2 Memory access times

item	AVME-148(25MHz)		remarks
	When reading	When writing	
MPU to local EEPROM	19 Clock -		1 Cycle Note 1)
MPU to local SRAM	4 clocks	4 clocks 1 cycle	
MPU to local FlashMemory	6 Clock -		1 Cycle Note 5)
MPU to Normal Mode	4 clocks	4 clocks 1 cycle	
Onboard DRAM	Burst Mode	4 $\ddot{\wedge}$ 2 $\ddot{\wedge}$ 2 $\ddot{\wedge}$ 2 Clock 5	4 $\ddot{\wedge}$ 2 $\ddot{\wedge}$ 2 $\ddot{\wedge}$ 2 Clock 6 1. Burst Note 2)
MPU to VMEbus	Clock +T	Clock +T	1 Cycle Note 4)
VMEbus to on-board DPRAM	430ns	430ns	Access Time Note 3)

Note:

- 1) This is the case when an EEPROM with an access time of 90nS is used. Note that the EEPROM is accessed by latching 8-bit data four times to make it 32-bit data, which is then read by the MPU. I am.
- 2) When the local SRAM access time is 80 nS. 3) This is the typical value from assertion of DS0\* /DS1\* on the VMEbus to returning DTACK\* when the local MPU is executing a STOP command. However, this is not the case if there is a refresh conflict.
- 4) Assuming that the AVME-148 is the VMEbus master, let T be the integer obtained by dividing the response time from DS0\* /DS1\* assertion to DTACK\* by one MPU clock time (40 nS). 5) The cycle time during a read is 6 clocks, but the cycle time during a write is a minimum of 8  $\mu$ s. It will be.

### 5.1.3.2 Accessing DPRAM via VMEbus

The local bus is acquired from the VMEbus once per cycle to access the DPRAM.

If the MPU attempts to access the VMEbus and the VMEbus receives an access, a deadlock condition occurs.

To release this state, the MPU is instructed to retry and the cycle is aborted.

This causes the local bus to be relinquished and the VMEbus to be given bus mastership.

After the VMEbus side completes one cycle of access to the DPRAM, the MPU acquires the local bus again and aborts.

If the VMEbus is accessed by block transfer, it does not respond.

Termination due to VMEbus timeout.

When a read-modify-write cycle is executed from the VMEbus side to the DPRAM, the read and write

Note that MPU cycles may be inserted between the cycles of the other programs.

### 5.1.3.3 Refresh

The DPRAM is refreshed approximately once every 15 µs and is executed between DPRAM access cycles.

In this case, the local bus is not acquired.

### 5.1.3.4 Accessing DPRAM from LAN and FDC

LAN and FDC use the local DMAC (built into FPGA) to access DPRAM. LAN and FDC

When a transfer request is received from the local DMAC, the local bus right is given to the multi-port arbiter.

A request is made for each access. If the request is granted, the local DMAC reads from or writes to the DPRAM.

Perform a write cycle.

The local DMAC can only access the DPRAM and cannot access the VMEbus.

### 5.1.4 Local SRAM

The MPU has a dedicated local memory, a 512K x 8-bit SRAM.

Backup is possible from an on-board battery or the +5V STDBY power supply from the VMEbus.

### 5.1.5 Flash Memory

Four 1M x 8-bit flash memories are installed as local memory for the MPU, making the memory width 32 bits.  
I am.

### 5.1.6 Bus Errors

If the local MPU, LAN, or FDC encounters a fault or abnormality while executing a bus cycle, a bus error is input. This module can check the cause of a bus error by referencing the status register (STAT2). This error status is write clear.

The error source is an error from the local bus timer or VMEbus. Local bus timer  
For errors caused by this, see the next section: Local Bus Monitoring.

Errors from the VMEbus are reported by the slave module either by driving the bus error signal (BERR\*) or by the VMEbus  
This is an error caused by a timer time-out.

The VMEbus error signal is asserted when the local MPU executes a VMEbus cycle.

### 5.1.7 Local Bus Monitoring

This module has a local bus timer monitoring function, and two types of time settings are available.  
This can also be disabled by using the DIP switch on the front panel.  
This timer is enabled when the 68040MPU becomes the local bus master.  
It does not work when accessed from the VMEbus. The following factors can cause a timeout:

- 1) When an undefined memory map is accessed. 2) When  
an on-board device such as local I/O is accessed, a response signal (TA\* or TEA\* ) is not returned.  
When it didn't come
- 3) When accessing the VMEbus, if the VMEbus cannot be acquired (after the VMEbus is acquired, this timer stops).

All of these errors are reported as a local bus time-out, set to LBTO in the status register.  
Set the following.

### 5.1.8 Battery

An on-board lithium battery backs up the RTC and local SRAM.  
The local SRAM can also be backed up from +5VSTDBY on the VMEbus.  
The backup continues until the system power voltage exceeds 4.3V (typ.). The RTC is always on.  
Backed up by the on-board lithium battery.

This module has a function to detect low battery voltage. When the battery voltage falls below 2.65V (typ.),  
Bit 12 (BATF) of the status register (STAT2) is set. On-board lithium battery

The lifespan of the is approximately 8 years under the following conditions.

- a) RTC = 2 $\mu$ A (typ)
- b) SRAM = 5 $\mu$ A (typ)
- c) Backup IC 2 $\mu$ A (typ)
- d) Leakage current of capacitors, etc. is 2 $\mu$ A
- e) Operating temperature is 25°C

### 5.1.9 Watchdog Timer (WDT)

The watchdog timer is built into the FPGA. The time-out period is set in the CNT2 register.

By setting the WDTIME bit, you can choose between two times: 500mS ("0") and 1S ("1").

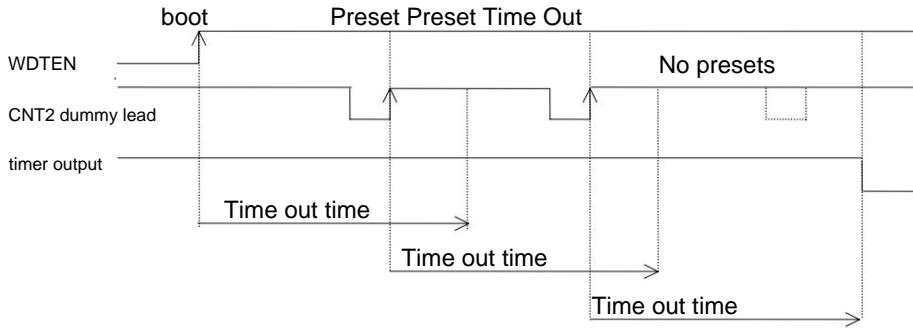
The master is started by setting the WDTEN bit of the CNT2 register to "1".

Preset the watchdog timer within the time set in the CNT2 register (dummy read of CNT2)

If there is no W5, a timeout occurs. If W5 is open at this time, the LRQ6 interrupt is asserted.

If shorted, a system reset is performed.

The watchdog timer must be preset well in advance of the set time.



### 5.1.10 Snooping function

When another master starts accessing the DPRAM, the MC68040MPU data cache entry

If the address is in the slave and the line is dirty, the MPU inhibits the memory and

The device responds to other masters as if it were the memory.

Snoop control is performed with the settings SC1="0" and SC0="1".

## 5.2 VMEbus System Controller

This module has the necessary functions as a VMEbus system controller. The internal configuration is as follows: These include a VMEbus watchdog timer, a system clock driver (SYSCLK\*), an arbiter, and an IACK daisy chain driver. In addition, a system reset is also provided. The system controller function can be enabled/disabled using the dip switches on the front panel, and the SCON (S) LED (green) lights up when the system controller is configured.

### 5.2.1 VMEbus Monitoring

The VMEbus timer starts after the data strobe signal (DS0\* or DS1\*) on the VMEbus is asserted. When both are negated, the timer stops. Two time settings, 128  $\mu$ s and 256  $\mu$ s, can be set, and they can be individually disabled by the system controller using the dip switches on the front panel. When a time-out occurs, the bus error signal (BERR\*) is driven on the VMEbus.

### 5.2.2 System Clock Driver

It supplies a 16MHz clock with a 50% duty cycle as the VMEbus system clock (SYSCLK).

### 5.2.3 Arbitrator

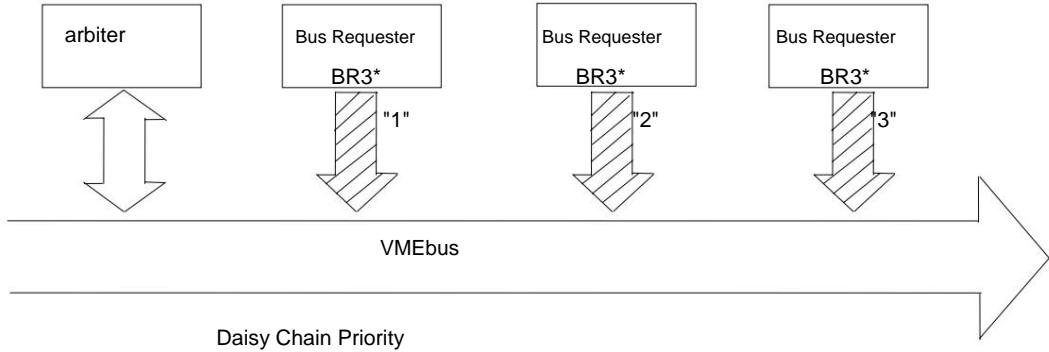
The VMEbus arbiter on this module supports both priority (PRI) and round robin (RRS) can be selected by jumper settings.

#### 1) Priority Method (PRI)

The priority method assigns priorities to the VMEbus bus request signals (BR3\* to BR0\*), with BR3\* being the highest and BR0\* being the lowest. The bus requester outputs a level of 1 for these BR3\* to BR0\* request signals. If the arbiter determines that access is possible for this request, it asserts a bus grant signal (BG3IN\* to BG0IN\*) of the same level as the highest-ranked request signal being requested.

When there are request signals of the same level from other bus requesters, the priority is determined by a daisy chain. In the daisy chain, the requester closest to the arbiter has the highest priority, and the further away from the chain the lower the priority is. Also, when the PRI arbiter receives a bus request signal

with a higher level than the master currently holding the bus, it outputs a bus clear signal (BCLR\*) to notify the current master that a higher priority request is waiting. The PRI arbiter is used when priority is required for bus use.

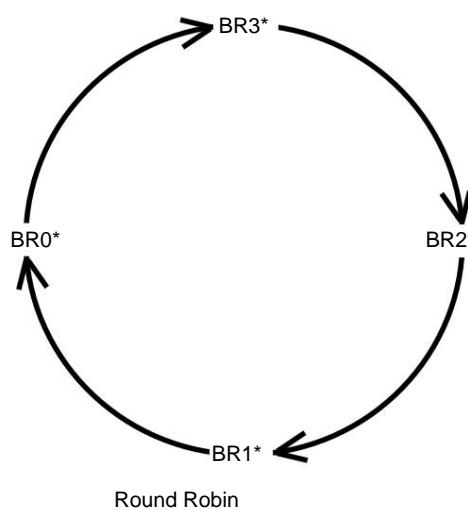


## 2) Round Robin Method (RRS)

The round robin method cyclically changes the priority level of the bus request signals (BR<sub>3\*</sub> to BR<sub>0\*</sub>) as shown in the figure below. Assign to.

In response to a request signal (BR<sub>n\*</sub>: n = 0 to 3) from the bus requester , if the arbiter is able to access the bus, The bus grant signal (BG<sub>nIN\*</sub> ) is driven at the same level as the request signal. The highest priority level of vitiation is assigned to BR<sub>(n-1)\*</sub>. Also, no other requester with the same level can When a bell request signal is received, priority is determined by daisy chain.

The priority of the daisy chain is decided by the requester closest to the arbiter being given the highest priority. The further along the line the bus has lower priority. The RRS arbiter in this module does not support the bus clear signal (BCLR\*). The bit is used when you want to give bus use rights to each bus master evenly.



### 5.2.4 IACK daisy chain driver

The IACK daisy chain driver allows interrupt handlers to acknowledge VMEbus interrupts (IRQ1\* to IRQ7\* ).

The read cycle starts when the acknowledge cycle is executed.

We are also checking whether it is a cyclical downtime.

### 5.2.5 System Reset

The VMEbus system reset signal (SYSRESET\* ) is supported, allowing this module to

This signal is output when a reset operation occurs internally in the controller.

However, it will not be output by a software reset command.

### 5.2.6 VMEbus Interface

This module provides the VMEbus interface including the bus requester, interrupter/handler,

It has a built-in master/slave interface and AC FAIL\* /SYSFAIL\* monitor function.

### 5.2.7 VMEbus Requestor

The VMEbus requester outputs a level 1 request signal (BR3\* to BR0\* ) to the bus arbiter.

In response to this request, the bus arbiter issues a bus grant signal of the same level.

When it receives a bus signal (BG3IN\* to BG0IN\* ), it outputs a bus busy signal (BBSY\*) and acquires the bus.

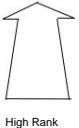
After the bus is acquired, there are two bus release conditions, which are specified by the control register (CNT1).

The bus release conditions are ROR and RWD, and they determine the execution efficiency from the viewpoint of the MPU module and the VMEbus.

The rates are shown in Table 9-1.

If you change the mode from ROR to RWD while the bus is acquired, the bus will be released immediately and the mode will switch to RWD.

Table 9-1 Execution efficiency by release conditions

Bus release MPU module VME bus conditions		Execution	Execution Efficiency
ROR		efficiency: High 	Low
RWD			 High Rank

## 5.2.8 VMEbus Master Interface

This module is equipped with VMEbus master function and supports address sizes A32/A24/A16 by MPU memory map. and data port sizes D32/D16/D8.

The AM code signal (AM5 to AM0) is AM5 to AM3 for standard access, extended access, and short I/O access. AM2 to AM0 are connected to the transfer modifier signals TM2 to TM0 of the MC68040MPU.

Data access to the VMEbus can be by byte, word or longword.

The VMEbus long word signals (LWORD\* signals) are used to communicate with the VMEbus's extended address space. This signal is asserted when a 4-byte access is performed on a word boundary.

Transfer is not possible.

Also, in the VMEbus standard, during a read-modify-write cycle, the master must assert DTACK\* or The address must be held valid until the second falling edge of BERR\* is detected.

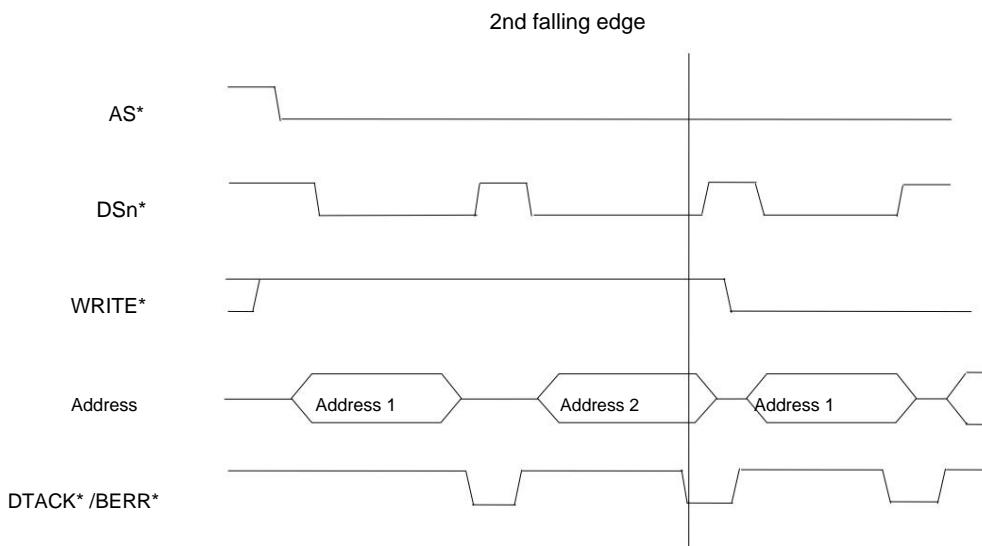
However, the MPU of this module has a read modifier that changes the address in the second cycle.

There is a phi instruction (CAS2 instruction and CAS instruction executed in word/longword from odd address).

If the above VMEbus standard is satisfied, the read-modify data that changes the address in the second cycle is

The instruction cannot be executed. Therefore, the read-modify-write cycle to the VMEbus of this module is

The timing is as follows:



Therefore, the module sends a read-modify command to the VMEbus that changes the address in the second cycle. When executing an instruction, the slave should obtain address information at the falling edge of DSn\*.

## 5.2.9 VMEbus Slave Interface

The slave function of this module allows other VMEbus masters to access the dual port memory.

This memory is located in the extended address space of the VMEbus and can be accessed by a front panel

The flip switch allows you to select from four different memory addresses.

There are 32 addresses and the AM codes are \$0E, \$0D, \$0A, and \$09.

Supports D32/D16/D8 and supports byte, word, longword, unaligned and read-modify.

Write (RMW) transfers are possible.

However, during a RMW cycle from the VMEbus, the local

It may be interrupted by cycles from the MPU, LAN, or FDC.

Access to I/O devices other than dual port memory from the VMEbus and when this module is connected to the VMEbus

It is not possible to access the on-board dual-port memory via

## 5.3 Interrupts

### 5.3.1 VMEbus Interrupters/Handlers

The VMEbus interrupter generates an interrupt to the VMEbus, the handler accepts the interrupt and enters an acknowledge cycle. If the cycle is an acknowledgement of the requested interrupt level, it sends out 8 bits of status ID information, otherwise it sends out the IACK out signal (IACKOUT\*).

This module can be programmed to send interrupts to any of the seven interrupt levels (IRQ7\* - IRQ1\*) and can also display status. The ID information can also be set programmably.

If acknowledged, the interrupt source to the VMEbus is cleared and the VME INTERRUPT STATUS is returned locally.

The cause of the interrupt is cleared by the program.

When an interrupt occurs from this module to the VMEbus, the same level of the on-board VMEbus interrupt handler must be masked and the status ID information must be set. For details about the handler, see 8.12

Interrupt Handler.

### 5.3.2 VMEbus Interrupt Acknowledge

The VMEbus interrupt acknowledge activates the IACK\* signal and outputs the interrupt acknowledge level to A01 to A03. These signals are monitored, and if an interrupt is not generated at the level when the IACKIN\* signal was asserted, the IACKOUT\* signal is asserted. If they match, the status ID data is output to D00 to D07 and the response signal (DTACK\*) is driven.

### 5.3.3 Interrupt Sources

#### 1) ACFAIL\*

Occurs when the ACFAIL\* signal on the VMEbus is asserted low.

#### 2) ABORT

This occurs when the front panel DIP switch (DSW1) 2 is set to "ON" and the ABORT switch is pressed.

#### 3) SYSFAIL\*

When the "SYSFIEN" bit in the control register (CNT1) is set to "1", the SYSFAIL\* signal on the VMEbus is assigned to "L".

This occurs when the

4) WDT

When the "WDTEN" bit of the control register (CNT2) is "1", the watchdog timer times out.  
However, if jumper W5 is shorted, a forced reset is performed.

vinegar.

5) Timer

This occurs when the falling edge of the OUT output of the MSM82C54-2 (Timer) is detected.

6) Serial

INTR1(CN3), INTR2(CN4) of PC15662 and IRQ3\*(CN1), IRQ4\*(CN2) of FDC37C935 are asserted.  
This occurs when

7) SRQ3\*

This occurs when IRQ7\*(FDC), IRQ14\*(IDE1), or IRQ15\*(IDE2) of FDC37C935 is asserted.

8) VME INTERRUPT STATUS

When an interrupt is generated by the VME interrupt requester of this module,  
The interrupt occurs when the handler acknowledges the interrupt.

9) LAN

This occurs when AX88796's IRQ\* is asserted.

10) RTC

This occurs when IRQ1\* of FDC37C935 is asserted.

11) IRQ1\* - IRQ7\*

It is assigned to the VMEbus interrupt signal and occurs when the corresponding signal is "L".

## 5.4 Local I/O

### 5.4.1 Serial interface

This module uses one PC16552 as a serial communication controller and one FDC37C935 (Ultra I/O) is used to provide a total of 4 channels of serial interface (8-pin modular connector). Both are designed to communicate in asynchronous mode only.

The baud rate of this module is a maximum of 19.2 kbps and can be set for each channel.

For details, please refer to the user's manuals for PC16552 (NS) and FDC37C935 (SMSC).

### 5.4.2 Programmable Timers

The timer MSM82C54-2 (PIT) has three 16-bit programmable counters.

The source clock will be 4MHz.

The timer interrupt acknowledge status ID is given by IHAN. For details on the device, refer to the user's manual.

### 5.4.3 Real-time Clock (RTC)

The real-time clock uses the RTC (MC146818, DS1287 Compatible) built into the FDC37C935.

Built-in counters for hours, minutes, and seconds, as well as calendars for year, month, day, and day of the week, and can switch between 24H/12H, leap days, etc.

The FDC37C935 has an automatic year setting

function and a timer function. The RTC built in the FDC37C935 is backed up by a battery, and the backup power source is the on-board

It is a lithium battery.

In addition, the timer function generates a local interrupt of level 1 (LRQ1\*).

The status ID is provided by IHAN.

For more information about the device, see the user's manual.

#### 5.4.4 FDD interface

The controller uses the FDC37C935 built-in FDC, and uses the local DMAC (built-in FPGA) to read and write data from the DPRAM. Direct DMA transfer is performed.

The FDC37C935's built-in FDC has a 16-byte FIFO on the host interface.

The interface is assigned to row C of the P2 connector on the VMEbus.

If you use the FDD interface, a separate dedicated backplane (AVME-975A) is required.

For details

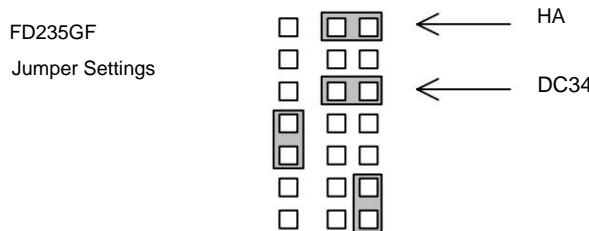
on the device, refer to the user's manual.

\*The recommended FDD for use with this module is the FD235GF made by TEAC. Do not use an FDD other than the recommended one.

Please contact us if you wish to

use the recommended product in an OS-9 environment.

Use the RY34/DC34 signal with the DC34 (DISK CHANGE signal).



#### 5.4.5 IDE Interface

The controller uses the IDE interface built into the FDC37C935, and data transfer is performed by the MPU.

The IDE interface has two channels. One channel (IDE1) is connected to P2 of the VME bus.

The other channel (IDE2) is assigned to the internal CompactFlash

It is assigned to the interface connector (CN3).

For more information about the device, see the user's manual.

\*The IDE interface of this module supports PIO mode 2 and later.

If you are using an IDE device with an IDE interface in the previous mode (PIO mode 0, 1), it may not work.

Please note that we cannot guarantee the product. Please check with our sales department for recommended equipment.

Sai.

#### 5.4.6 Ethernet Interface (LAN)

The AX88796 (manufactured by ASIX) is used as the controller to configure the 10BaseT interface.

DMA transfer is performed directly to DPRAM using the local DMAC (built into FPGA).

The highest addresses (PA31 to PA24) are fixed, so DMA transfers are performed only via the on-board DPRAM and the VMEbus.

DMA transfers to the above memory are not possible.

For more information about the device, see the user's manual.

### 5.4.7 Interrupt Handler (IHAN)

This module uses the uPD65622GA-Y90-9EV as an interrupt handler (IHAN) and handles VMEbus interrupts (IRQ1\*

Seven levels of priority are assigned to 14 interrupt sources, including interrupts (IRQ1\* to IRQ7\*) and local interrupts (LRQ1\* to LRQ7\*), and are reported to the MPU.

The interrupts can be masked and the detection conditions can be set individually. During

the acknowledge cycle of a local interrupt, a vector is sent from IHAN.

During an acknowledge cycle, if there is no local interrupt of the appropriate level, the VMEbus

An acknowledge cycle is performed.

In other words, interrupt priority at the same level is on the local side, and is overridden by the ACFAIL\* and SYSFAIL\* signals of the VMEbus.

The interrupts that occur due to these two factors are assigned to local interrupts, and only the interrupt detection for these two factors is set to the falling edge.

It is recommended to use the others under low-level conditions (LRQ7\* is fixed to detect the falling edge).

The interrupt level assignment and priority are shown in Table 8-1 and Table 8-2.

The SRQ3\* interrupt is an OR condition of the FDC, IDE1, and IDE2 interrupts. The vector values are FDC (\$F8),

The interrupts are IDE1 (\$F9) and IDE2 (\$FA), so you can tell which one is causing the interrupt.

The SRQ4\* interrupt is the OR condition of the UART (FDC37C935) 2ch and DUART (PC16552D) 2ch interrupt.

The vector values are UART1 (\$FC), UART2 (\$FD), DUART1 (\$FE), and DUART2 (\$FF), and each channel is

This allows you to tell which interrupt is which.

The SRQ5\* interrupt is an OR condition of the 3ch interrupt of the Timer (82C54), and each vector value is

The channels are Timer1 (\$F0), Timer2 (\$F1), and Timer3 (\$F2), and it is now possible to tell which channel the interrupt is coming from.

I am.

Table 8-1 Interrupt level allocation

interrupt level	interrupt factor	Local Interrupt Level	Interrupt Cause	Bus Interrupt Level	Interruption fortunes
7		LRQ7*	ACFAIL/ABORT	IRQ7*	IRQ7* on the VMEbus
6		LRQ6*	SYSFAIL/WDT	IRQ6*	IRQ6* on the VMEbus
5	SRQ5*	-	-	IRQ5*	IRQ5* on the VMEbus
4	SRQ4*	-	-	IRQ4*	IRQ4* on the VMEbus
3	SRQ3*	LRQ3*	VME INTERRUPT STATUS	IRQ3*	IRQ3* on the VMEbus
2		LRQ2*	LAN (AX88796)	IRQ2*	IRQ2* on the VMEbus
1		LRQ1*	RTC (FDC37C935)	IRQ1*	IRQ1* on the VMEbus

Table 8-2 Interrupt Priority

interrupt level	priority Rank	High ←													
		LRQ7*   IRQ7*													
7	High ↑		LRQ6*   RQ6*												
6				SRQ5*   RQ5*											
5					SRQ4*   RQ4*										
4						SRQ3*   RQ3*									
3							LRQ2*   RQ2*								
2								LRQ1*   RQ1*							
1															

## 5.4.8 Reset

This module has five reset sources and performs on-board initialization. The way the SYSRESET\* signal on the VMEbus is driven varies depending on whether this module has a system controller function or not.

a) Reset by SYSRESET\* signal

Resets all devices in this module.

b) Power-on Reset

When the power is turned on and the voltage exceeds 4.6V to 4.8V, a reset signal is generated for about 550mS to reset all on-board devices. If this module is a system controller, it also drives the SYSRESET\* signal.

c) Resetting via the front panel RST switch

Resets all devices in this module. The reset signal is asserted while the switch is pressed. If this module is a system controller, it also drives the SYSRESET\* signal.

d) Watchdog Timer Reset

At the timeout, the reset signal is asserted for about 300mS to set all devices in this module, and if this module is a system controller, it also drives the SYSRESET\* signal.

e) Reset by MPU reset command

It only resets the on-board I/O devices, but not the control/status registers.  
It is not reset and does not drive the SYSRESET\* signal.

## Chapter 6: Setting

This section explains jumper and switch settings for the AVME-148.

### 6.1 Jumper Location

The jumper locations for the AVME-148 are shown in Figure

6-1. The jumper and switch information that can be read is short and switched on for a logic "1", open and A switch on and a switch off represent a logical "0."

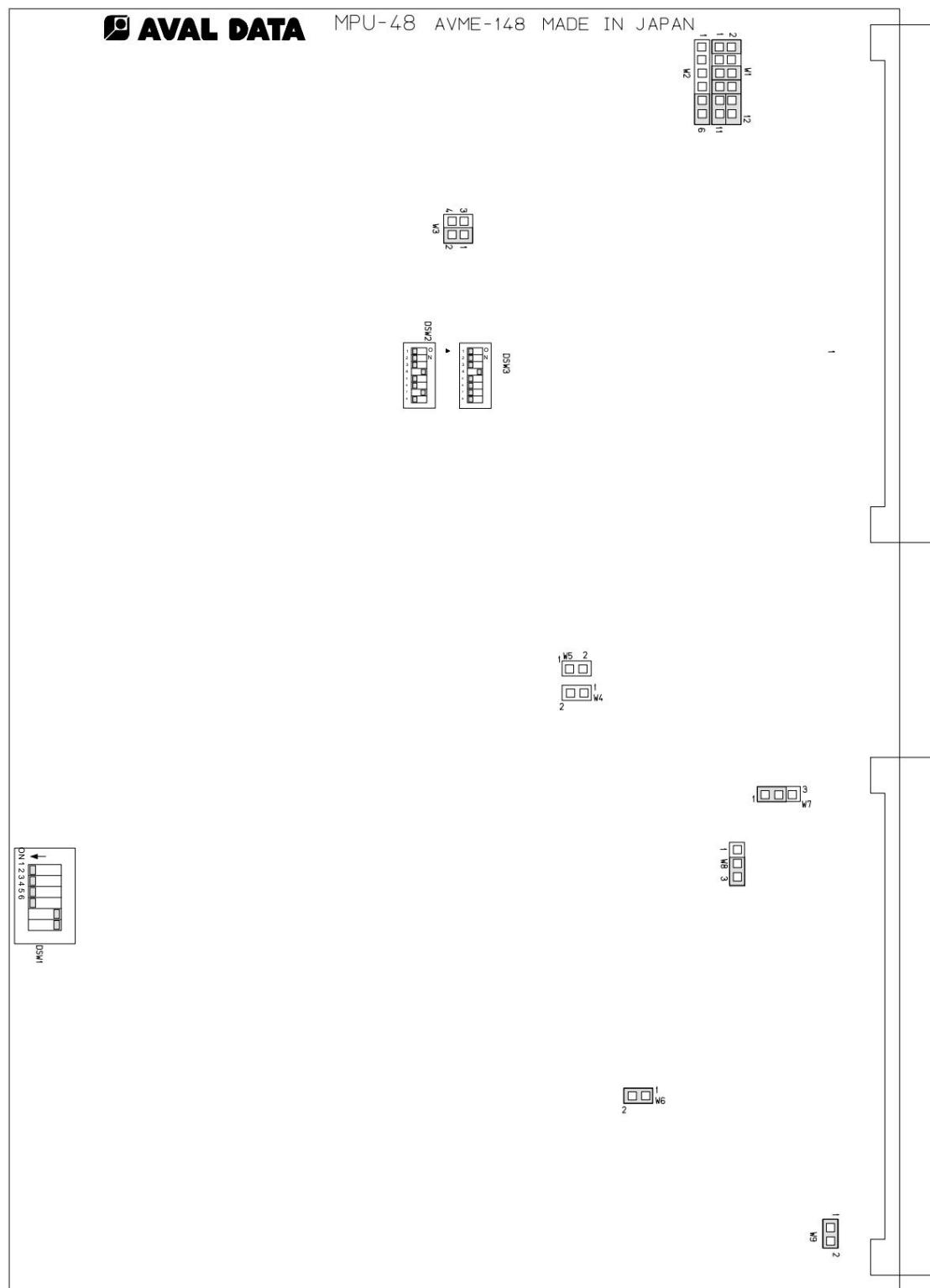


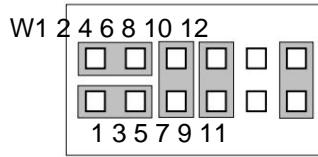
Figure 6-1 AVME-148 Jumper Locations

## 6.2 Jumper Functions

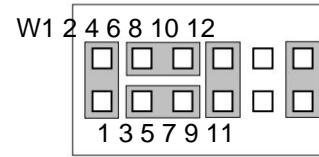
### 6.2.1 Bus grant signal setting (W1)

Jumper W1 sets the level of one of the bus grant signals BG0IN\* to BG3IN\*. Set the bus grant signal to the same level as that set for the bus request signal (W2). The factory setting is d).

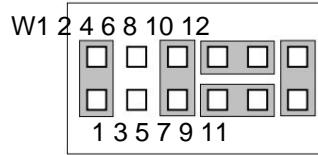
- a) When BR0\* is used,  
the bus grant signal is  
Select BG0IN\*



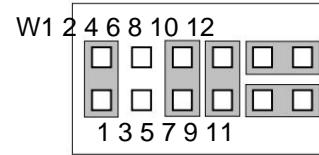
- b) When using BR1\*, the bus grant signal is Select BG1IN\*



- c) When using BR2\*, the bus grant signal is Select BG2IN\*



- d) When using BR3\*, the bus grant signal is Select BG3IN\*



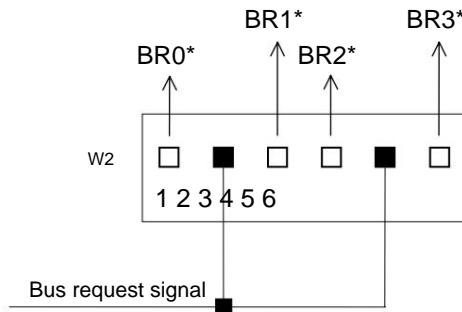
#### Notes:

- 1) The bus requester consists of W1 and W2, so please set them according to the usage level of this module.
  - 2) When installing this module in a system, make sure to open the BGnIN\* /BGnOUT\* daisy chain jumpers for the insertion slot of the VME:J1 backplane .
  - 3) When using a single-level arbiter, use the BR3\* level. 4) There are four possible settings for jumper W1: a) to d). Do not use any other combinations.
- Please come.

### 6.2.2 Setting the Bus Request Signal (W2)

Jumper W2 selects one of the bus request signals BR0\* to BR3\* to be output when acquiring the VMEbus.

Set the following:



W2 jumper setting 1 2 3 4 5 6	Bus Request Usage Level Factory Default
<input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/>	Bus request level 0: BR0*
<input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input checked="" type="checkbox"/>	Bus request level 1: BR1*
<input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	Bus request level 2: BR2*
<input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>	Bus request level 3: BR3* •

Note:

Be sure to pair with W1.

### 6.2.3 Time Settings for Bus Monitoring (W3)

Jumper W3 sets the bus watchdog timer for the local bus and VMEbus.

#### a) Local Bus Watchdog Timer

W3 jumper setting	Local bus timeout time	Factory setting
4 <input type="checkbox"/> <input type="checkbox"/> 3	128µS	●
4 <input checked="" type="checkbox"/> <input type="checkbox"/> 3	256µS	

This timer is enabled when DSW1 4 on the front panel is turned on. A time-out occurs within the above period if the local bus cycle does not end. However, if the VMEbus side is accessed, the timer is reset when access to the VMEbus becomes valid.

#### b) VMEbus Watchdog Timer

W3 jumper setting	Local bus timeout time	Factory setting
2 <input type="checkbox"/> <input type="checkbox"/> 1	128µS	
2 <input checked="" type="checkbox"/> <input type="checkbox"/> 1	256µS	●

This timer is enabled when DSW1 1 (system controller) and 3 are on.

A timer out occurs when a VMEbus bus cycle does not finish within the above time period.

Note:

The bus timer must have a shorter local bus watch time than the VMEbus watch time.

### 6.2.4 Watchdog Timer Settings (W4)

Jumper W4 is set when using the watchdog timer. The watchdog timer is controlled by the WDTEN bit of the control register (CNT2).

Setting this bit to "1" starts the timer and sets the control register (CNT2)

The timer is preset by a dummy read of this bit. The time-out

period is set by the WDTIME bit in the control register (CNT2).

A "0" bit is approximately 500mS and a "1" bit is approximately 1S.

#### a) Jumper settings

W4 Jumper Settings	Machine	Noh	Factory
2 <input type="checkbox"/> <input type="checkbox"/> 1	reset by watchdog timer is disabled	•	
2 <input checked="" type="checkbox"/> <input type="checkbox"/> 1	Enable reset by watchdog timer		

### 6.2.5 Bus arbitration settings (W5)

Jumper W5 selects the arbitration method for the VMEbus arbiter. This setting is valid when the controller is a system controller.

W5 Jumper Settings	Machine	At time of shipment *
1 <input type="checkbox"/> <input type="checkbox"/> 2	Round Robin System (RRS)	
1 <input checked="" type="checkbox"/> <input type="checkbox"/> 2	Priority Method (PRI)	

### 6.2.6 Use of IDE bus (P2) (W6, W9)

Jumpers W6 and W9 select the use of the IDE bus assigned to P2.

W6 Jumper Setting Function	At the time of shipment
1 <input type="checkbox"/> <input type="checkbox"/> 2	Do not use the IDE bus (P2)
1 <input checked="" type="checkbox"/> <input type="checkbox"/> 2	Use IDE bus (P2 )

W9 Jumper Setting Function	At the time of shipment
1 <input type="checkbox"/> <input type="checkbox"/> 2	Do not use the IDE bus (P2)
1 <input checked="" type="checkbox"/> <input type="checkbox"/> 2	Use IDE bus (P2 )

### 6.2.7 Battery Selection (W7)

Jumper W7 selects the source of the backup power for the local SRAM: VMEbus (+5V STDBY) and on-board battery options.

W7 Jumper Settings	Battery power	At the time of shipment
 1 2 3	Use the on-board battery	<input checked="" type="radio"/>
 1 2 3	Supplied from VMEbus (+5V STDBY)	

Note:

- 1) When using with 2-3 shorted, +5V standby power must always be supplied to the VMEbus (+5V STDBY) side.  
only on systems where
- 2) If there is no battery voltage or all jumpers on W7 are open, the  
may not function properly.

### 6.2.8 SRAM Battery Backup Setting (W8)

Jumper W8 sets the local SRAM with or without battery backup.

W8 Jumper Settings	Machine Noh	At the time of shipment
 1 2 3	SRAM battery backup available	
 1 2 3	No SRAM battery backup	

Note:

If you do not need to back up the SRAM, use 2-3 shorted.

## 6.3 DIP Switches

The AVME-148 has three dip switches. DSW1 controls the hardware of this module.

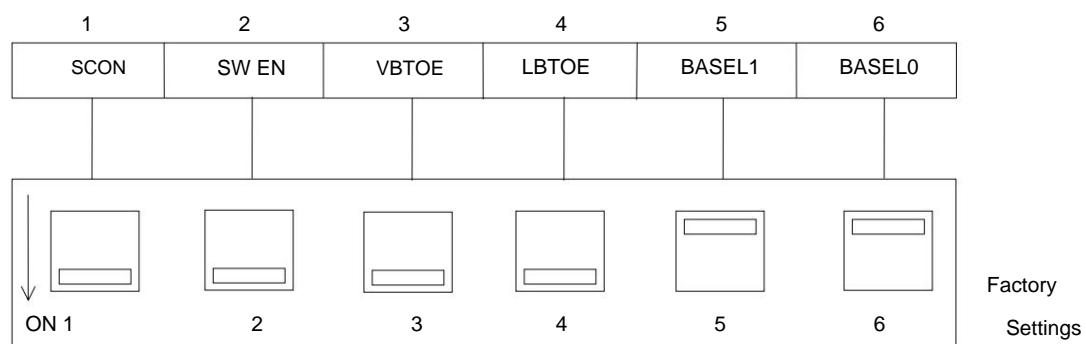
DSW2 and 3 are provided for software purposes.

### 6.3.1 Front DIP Switch Settings (DSW1)

The DIP switch DSW1 is used to set the functions of this module and is set when the module is installed in the system.

There are DIP switches on the front panel to allow this to be changed.

The configuration of DSW1 is as follows:



#### 1) SCON (System Controller)

This bit makes this module a system controller.

ON : valid

OFF: Disabled

#### 2) SW EN (Switch Enable)

This bit enables/disables the RESET and ABORT switches on the front panel.

ON : valid

OFF: Disabled

#### 3) VBTOE (VMEbus Time Out Enable)

This bit enables/disables the VMEbus watchdog timer of this module. However, if SCON is not ON, the setting is invalid.

ON : valid

OFF: Disabled

## 4) LBTOE (Local Bus Timeout Enable)

This bit enables/disables the local bus watchdog timer in this module.

ON : valid

OFF: Disabled

## 5) BASEL1, BASEL0 (Base Address Select 1,0)

This bit changes the base address of the dual port memory as seen from the VMEbus side.

BASEL 1	BASEL 0	starting address
OFF	OFF	\$40000000
OFF	ON	\$42000000
ON	OFF	\$44000000
ON	ON	\$46000000

\$ displays hexadecimal

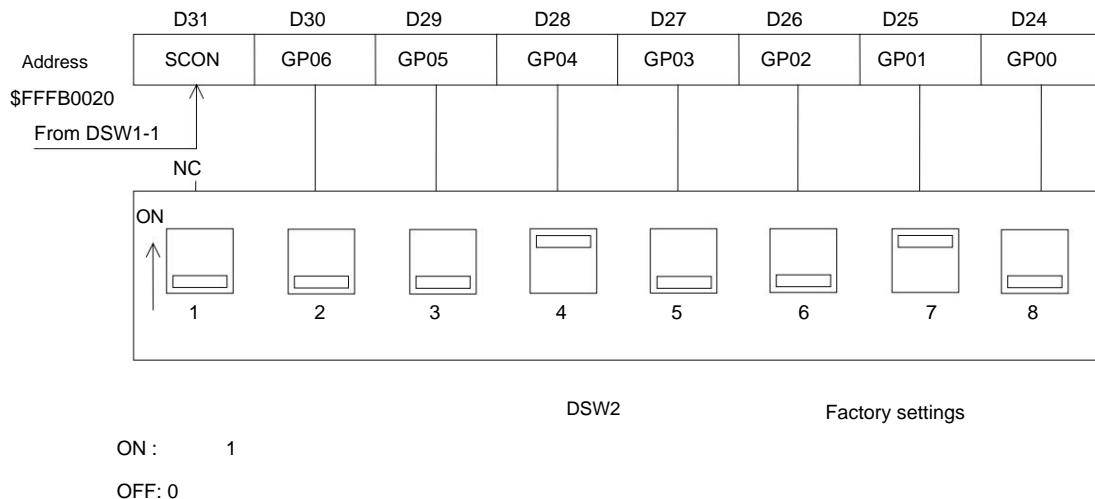
Notes:

- 1) Dual port memory can only be accessed from the VMEbus using extended addresses. 2) An address space equal to the size of the installed memory capacity is allocated from the selected start address.

### 6.3.2 Status 0 Setting (DSW2)

DIP switch DSW2 sets the information in status register 0 (STAT0). STAT0 is \$FFFFB0020

The user can use DSW2 as desired.



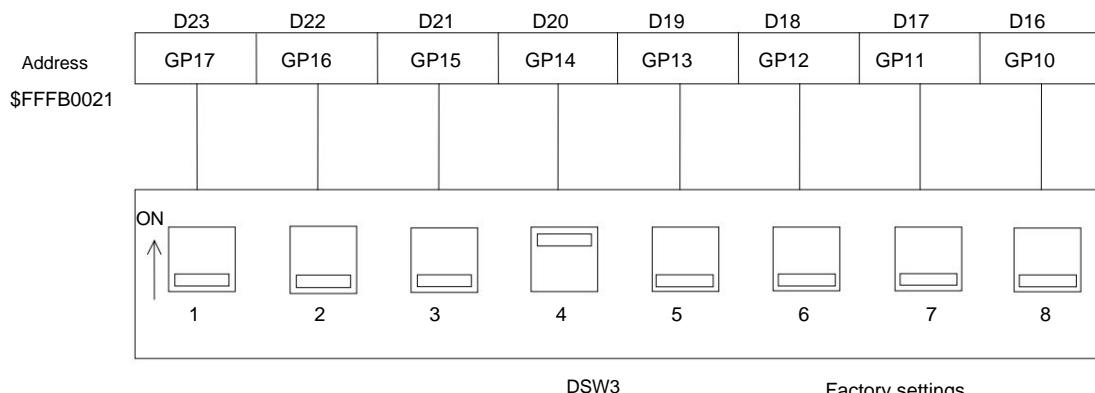
Note:

- 1) DSW2 No. 1 is not connected.
- 2) DSW1-1 information is input to SCON of D31.

### 6.3.3 Status 1 Setting (DSW3)

DIP switch DSW3 sets the information in status register 1 (STAT1). STAT1 is \$FFFFB0021

The user can use DSW3 at will.



ON :        1  
OFF: 0

## Chapter 7 Module Registers

This section describes the module control/status registers of the AVME-148. The module has a read/write control register and a read-only status register.

The control registers are VMEbus interrupt, watchdog, and

It controls the timing timer, VMEbus release mode, SYSFAIL\* signal control, and standard space usage.

The status register is used to store information about the system controller, user information, bus error conditions, and interrupt requests.

The device recognizes conditions such as low battery voltage and power failure.

### 7.1 Control Registers

These registers are control registers for this module.

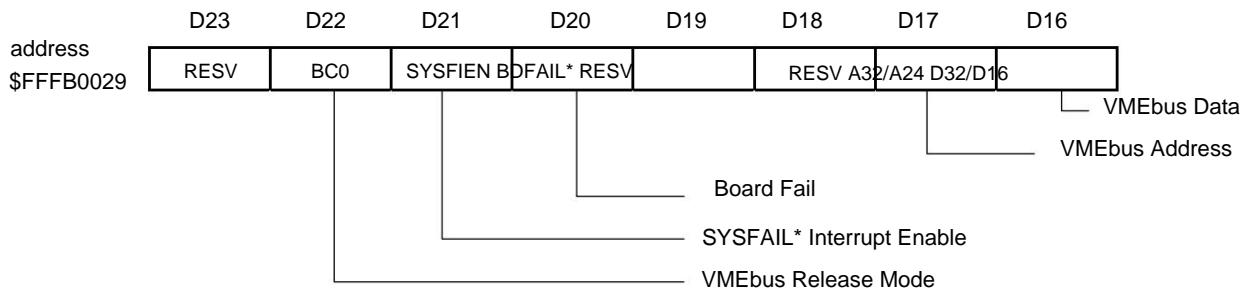
	D31	D24 D23	D16 D15	D8 D7	D0
address \$FFFFB0028		CNT0	CNT1	CNT2	CNT3
address \$FFFFB002C		CNT4	CNT5	CNT6	CNT7
address \$FFFFB0030		CNT8	CNT9	CNT10	
address \$FFFFB0034	D31	CNT11H		CNT11L	D0
address \$FFFFB0038	D31	CNT12	CNT13	CNT14	D0
address \$FFFFB003C	D31	CNT15H		CNT15L	D0
address \$FFFFB0040	D31	D24 D23	D16 D15	D8 D7	D0
		CNT16	CNT17	CNT18	CNT19

Note:

CNT0, 4, 5, 8, 12, 16, and 18 are reserved and the data is undefined when read.

### 7.1.1 CNT1 Register (Byte)

This register has the following structure:



At reset, all bits except the RESV bit are cleared to "0".

#### a) VMEbus ADDRESS/DATA (A32/A24, D32/D16)

This bit specifies the address range for the AVME-148 memory map address space from \$00000000 to \$00FFFFFF.

Specifies the size of the data bus and the address space. When this space is accessed by specifying A32, the AM command of the VMEbus is output. The extended address modifier code is output, and if it is A24, it is the standard address modifier code.

A code will be output.

For D32/D16, specify the data port size of the slave board, which allows standard adapters to be used.

VME module or 16-bit data port module decoded by address modifier code

It is possible to place and use slave modules of various sizes in this space. At reset, A32 and D32 are set.

A32/A24	D32/D16	Address	Data	AM	Code	
0	0	A24	D16		Standard	
0	1	A24	D32		Standard	
1	0	A32	D16		Extended	
1	1	A32	D32		Extended	

#### b) RESV (RESERVED)

Reserved. Data is undefined when read.

## c) BDFAIL\* (BOARD FAIL OUT)

BDFAIL\* is a bit that drives the SYSFAIL\* signal on the VMEbus from this module to "L". When this bit is set to "0", the FAIL LED (red) on the front panel lights up and the SYSFAIL\* signal on the VMEbus Drives to "L".

BDFAIL*	explanation
0	Drive the SYSFAIL* signal to "L"
1	Drive the SYSFAIL* signal to "H"

## d) SYSFIEN (SYSFAIL\* Interrupt Enable)

This bit enables an interrupt to be generated by the SYSFAIL\* signal from the VMEbus .

When the above SYSFAIL\* signal is active, a local interrupt level 6 (LRQ6\* ) is generated in this module.

However, this is only effective if this module is set as the system controller.

In addition, IHAN also has a mask function.

SYSFIEN	explanation
0	Mask the SYSFAIL* signal interrupt
1	Does not mask the SYSFAIL* signal interrupt

## e) BC0 (Bass Release Control 0)

Sets the bus release condition as a VMEbus master.

BC0 Release Conditions	function
0	ROR Release if requested by other bus master
1	Release after each RWD bus access

## •ROR (Release On Request)

Even if the bus mastership is granted once, if another bus master requests to use the bus, the bus is released. This mode is selected at reset.

## •RWD (Release When Done)

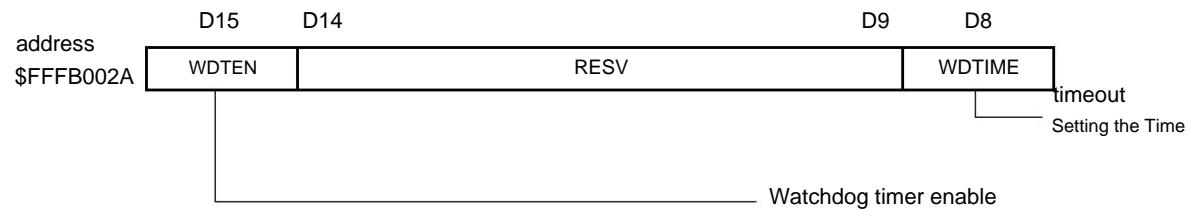
Once bus mastership is granted, it is released after the bus cycle ends.

The mode switch occurs after the current bus cycle ends. This mode is used by all VMEbus

This is effective when you want to encourage other bus masters that use the bus more frequently to use the bus more frequently.

### 7.1.2 CNT2 Register (Byte)

This register sets the timeout period for the timer in the watchdog timer circuit and also sets the timer. This register is used to preset the timer. A dummy read of this register initializes the timer. It is possible to make it.



a) WDTIME (watchdog timer timeout setting)

WDTIME	Function 0
Timeout	time is approximately 500mS. 1
Timeout	time is approximately 1S.

b) RESV (RESERVED)

Reserved. Data is undefined when read.

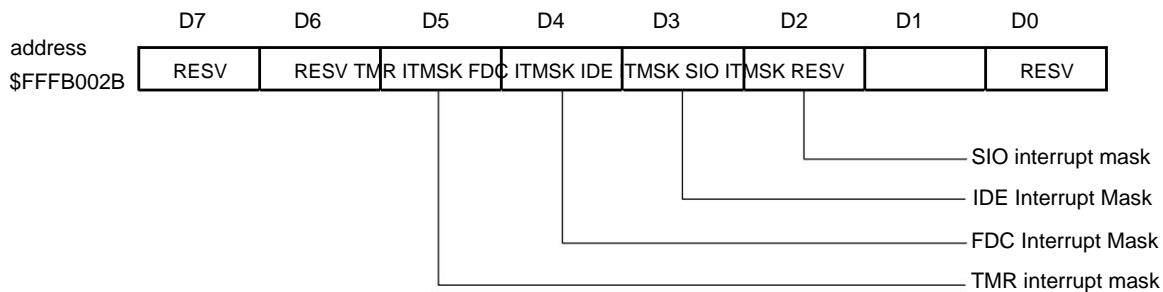
c) WDTEN (Watchdog Timer Enable)

Setting this bit to "1" enables the watchdog timer and starts it at the same time.  
It takes time.

WDTEN	Function 0
Disables	the watchdog timer. 1 Enables and starts
	the watchdog timer.

### 7.1.3 CNT3 Register (Byte)

This register has the following structure:



At reset, all bits are set to "1".

#### a) RESV (RESERVED)

Reserved. Data is undefined when read.

#### b) SIO IT MSK (SIO Interrupt Mask)

SIO IT MSK is a function that masks the interrupt signal (IRQ) from the SIO (FDC37C935) chip.

SIO IT MSK	explanation
0	Does not mask the interrupt signal from the SIO chip.
1	Masks the interrupt signal from the SIO chip

#### c) IDE IT MSK (IDE Interrupt Mask)

IDE IT MSK is a function that masks the interrupt signal (IRQ) from the IDE (FDC37C935) chip.

IDE IT MSK	explanation
0	Do not mask the interrupt signal from the IDE chip.
1	Masks the interrupt signal from the IDE chip

#### d) FDC IT MSK (FDC Interrupt Mask)

FDC IT MSK is a function that masks the interrupt signal (IRQ) from the FDC (FDC37C935) chip.

FDC IT MSK	explanation
0	Does not mask the interrupt signal from the FDC chip.
1	Masks the interrupt signal from the FDC chip.

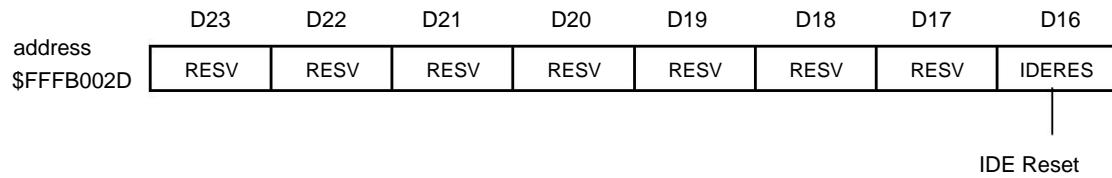
## d) TMR IT MSK (TMR Interrupt Mask)

TMR IT MSK is a function that masks the interrupt signal (IRQ) from the Timer (MSM82C54) chip.

FDC IT MSK	explanation
0	Does not mask the interrupt signal from the Timer chip.
1	Masks the interrupt signal from the Timer chip

## 7.1.4 CNT5 Register (Byte)

This register has the following structure:



At reset, all bits except the RESV bit are set to "1".

## a) RESV (RESERVED)

Reserved. Data is undefined when read.

## b) IDERES (IDE bus RESET)

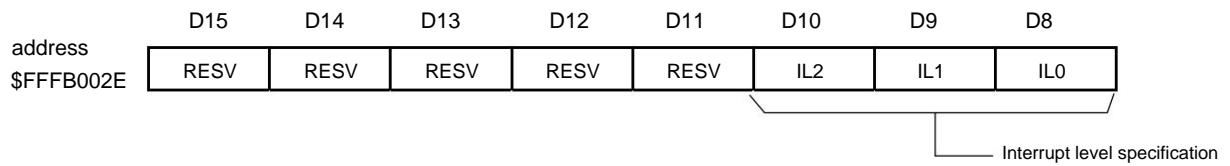
This bit is used to reset the devices on the IDE bus. Setting this bit to "0"

The RESET signal on the IDE bus is asserted for approximately 28 µS.

This bit remains at "0" and is set to "1" when the RESET signal is negated.

### 7.1.5 CNT6 Register (Byte)

This register has the following structure:



At reset, all bits except the RESV bit are cleared to "0".

#### a) Interrupt level specification (IL2, IL1, IL0)

The ILx bits are used to output vectored interrupts (IRQ1\* to IRQ7\*) to the VMEbus.

The interrupt signal output by the interrupt handler is received by the interrupt handler and the interrupt response cycle begins.

If the output level matches the interrupt response level, the ILx bit is cleared (%000) and the response cycle

When the module is executed, an interrupt with local interrupt level 3 (LRQ3\*) is generated for the interrupt handler of this module.

This notifies the MPU that a response cycle has been executed.

The signal can be cleared by doing a dummy read on this port.

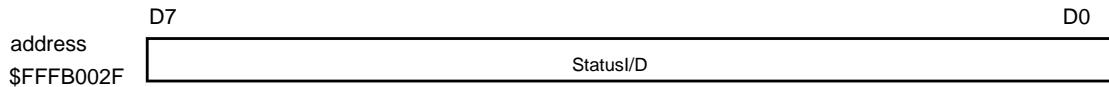
IL2	IL1	IL0	VMEbus	Vector Interrupt
0	0	0		No output
0	0	1		IRQ1*
0	1	0		IRQ2*
0	1	1		IRQ3*
1	0	0		IRQ4*
1	0	1		IRQ5*
1	1	0		IRQ6*
1	1	1		IRQ7*

#### b) RESV (RESERVED)

Reserved. Data is undefined when read.

### 7.1.6 CNT7 Register (Byte)

This register has the following structure:



#### a) StatusI/D

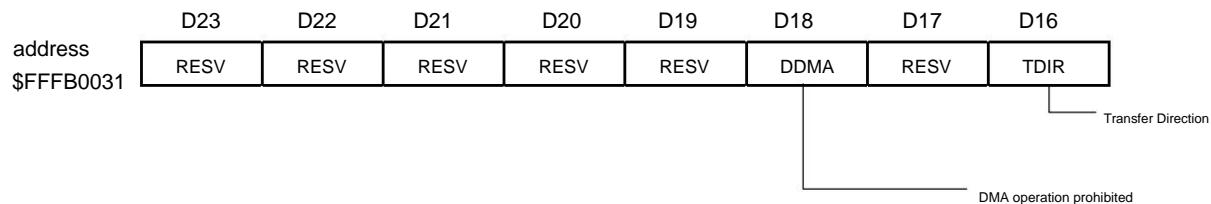
This register is for the status I/D when this module functions as an interrupter.

The value set in this register is output on the VMEbus as the response status I/D during an interrupt cycle.

vinegar.

### 7.1.7 CNT9 Register (Byte)

This register selects the mode for DMA transfer of FDC. The configuration is as follows:



#### a) TDIR (Transfer Direction)

This bit determines the direction of DMA transfers between memory and I/O.

TDIR	Transfer direction
0	I/O → Memory
1	Memory → I/O

#### b) RESV (RESERVED)

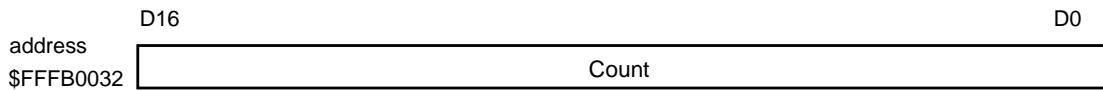
Reserved, ignored on write.

#### c) DDMA (DMA operation disabled)

Setting this bit inhibits DMA operations. While this bit is set, the bus It will no longer output quest signals.

### 7.1.8 CNT10 Register (Word)

This register is a count register for DMA transfer of FDC. It has the following structure:

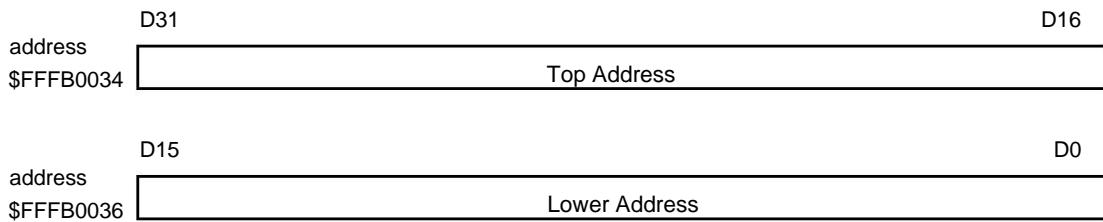


This register is a count register for DMA transfers of the FDC and counts up to 1 for each DMA transfer.

It will be down. Set the number of transfers as it is.

### 7.1.9 CNT11 Register (Word)

This register is the address register for DMA transfer of FDC. It has the following structure:

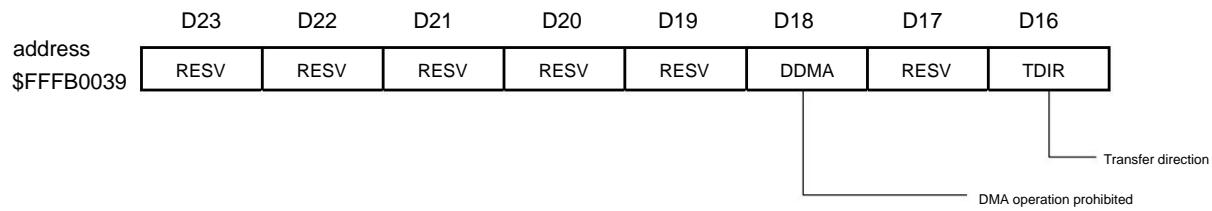


This register is the address register for DMA transfers of the FDC and is incremented by one for each DMA transfer.

I will upload it.

### 7.1.10 CNT13 Register (Byte)

This register selects the mode for DMA transfer over LAN. It has the following configuration:



#### a) TDIR (Transfer Direction)

This bit determines the direction of DMA transfers between memory and I/O.

TDIR	Transfer direction
0	I/O → Memory
1	Memory → I/O

#### b) RESV (RESERVED)

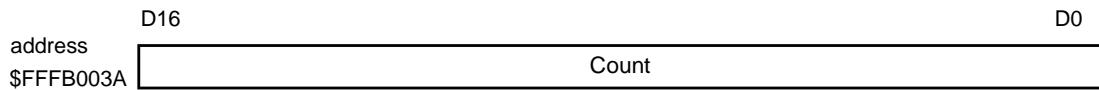
Reserved, ignored on write.

#### c) DDMA (DMA operation disabled)

Setting this bit inhibits DMA operations. While this bit is set, the bus It will no longer output quest signals.

### 7.1.11 CNT14 Register (Word)

This register is a count register for DMA transfers over LAN. Its configuration is as follows:

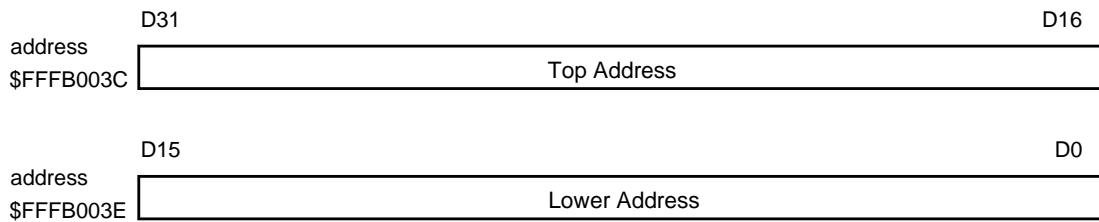


This register is a count register for LAN DMA transfers and counts up to 1 for each DMA transfer.

It will be down. Set the number of transfers as it is.

### 7.1.12 CNT15 Register (Word)

This register is the address register for DMA transfer over LAN. Its configuration is as follows:



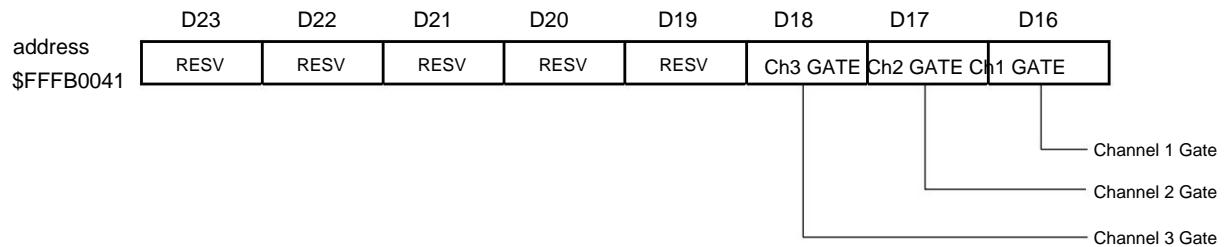
This register is the address register for LAN DMA transfers and is incremented by 2 for each DMA transfer.

I will upload it.

## Chapter 7 Module Registers

**7.1.13 CNT17 Register (Byte)**

This register has the following structure:

**a) Ch1 GATE (Ch0 GATE)**

Setting this bit controls the count of Ch1 of the timer (MSM82C54).

You can use the following functions to start, pause, restart, etc.

**b) Ch2 GATE (Ch1 GATE)**

Setting this bit controls the count of Ch2 of the timer (MSM82C54).

You can use the following functions to start, pause, restart, etc.

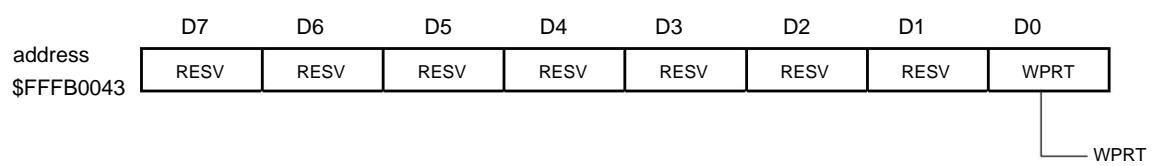
**c) Ch3 GATE (Ch2 Gate)**

Setting this bit controls the count of Ch3 of the timer (MSM82C54).

You can use the following functions to start, pause, restart, etc.

**7.1.14 CNT19 Register (Byte)**

This register has the following structure:

**a) WPRT (Write Protect)**

Setting this bit enables writing to the system ROM (Flash Memory).

## 7.2 Status Registers

This register is a register for identifying the status of this module that can be read in byte, word, or longword units.

It is a 32-bit data.

address	D31	D24 D23	D16 D15	D8 D7	D0
\$FFFFB0020		STAT0	STAT1	STAT2	STAT3

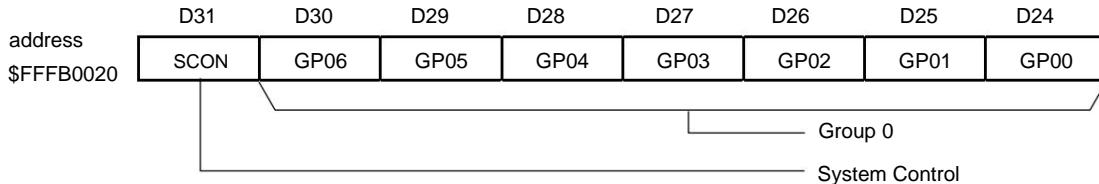
address	D31	D24 D23	D16 D15	D0
\$FFFFB0024		STAT4	STAT5	STAT6

Note: STAT3, 4, and 5 are reserved and the data is undefined when read.

### 7.2.1 STAT0 Register

This register has the following structure: See section 6.3.1: Status

0 Settings.



a) Group 0

Recognizes the switch (DSW2) information that is open to the user. The state is "1" when the switch is ON, and "0" when the switch is OFF. It will be read as "0".

b) SCON

When this bit is "1", this module is the system controller.

When the switch (DSW1-1) is ON, it is read as "1" and when it is OFF, it is read as "0."

## 7.2.2 STAT1 Register

This register has the following structure:

See section 6.3.2: Status 1 Settings.



a) Group 1

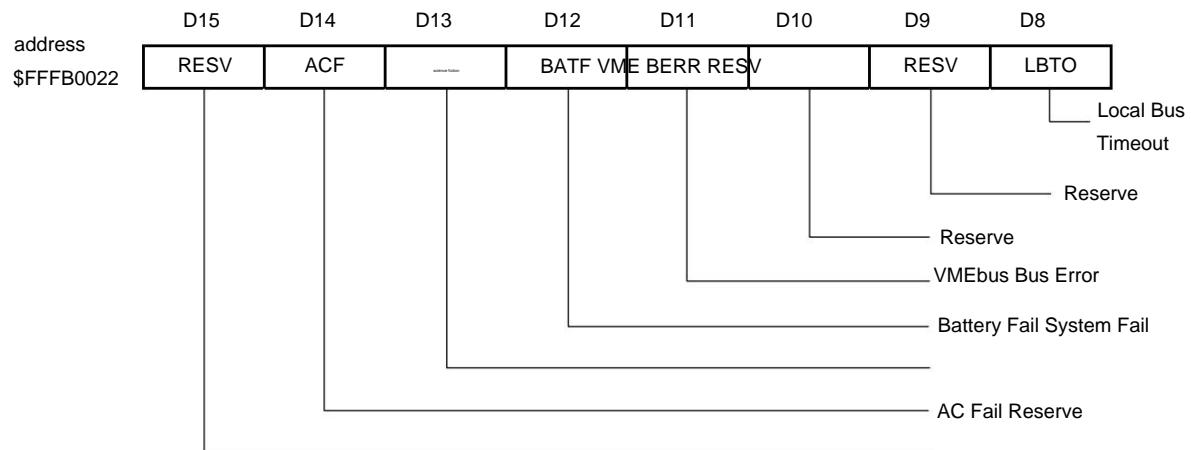
This recognizes the switch (DSW3) information that has been released by the user. The status is read as "1" when the switch is ON and "0" when it is OFF.

## 7.2.3 STAT2 Register

This register holds state changes. A set bit can be cleared by writing a "1" to it.

It is possible to do so.

However, if the set condition for each bit continues, it will be set again.



## a) LBTO (Local Bus Timeout)

LBTO monitors the local bus and if no response is received within the time set by W3, a timeout occurs.  
This bit becomes "1".

## b) RESV (RESERVED)

Reserved. Data is undefined when read.

## d) VMEBERR (VMEbus Bus Error)

When this module executes a VMEbus cycle, this bit is set to "1" when the VMEbus BERR\* signal is asserted.  
Set it to.

## e) BATF (Battery Fail)

This bit is set when the battery voltage of this module falls below approximately 2.65V.

## f) SF (System Fail)

When the SYSFAIL\* signal on the VMEbus is "L", this bit is set to "1". However,  
this is only valid when this module is the system controller.

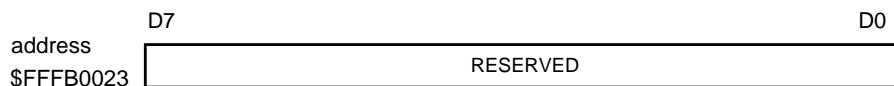
## g) ACF (AC FAIL)

When the ACFAIL\* signal on the VMEbus is "L", this bit is set to "1". This allows the system power supply to recognize an abnormality.  
It is also used to recognize the interrupt cause when a local interrupt LRQ7\* occurs.

If it exists, it is determined that the interrupt was caused by the ACFAIL\* signal; if it is "0", it is determined that the interrupt was caused by the ABORT switch.

### 7.2.4 STAT3 Register

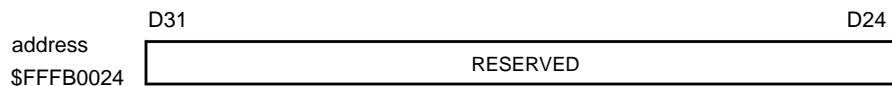
This register is reserved and the data is undefined when read.



## Chapter 7 Module Registers

**7.2.5 STAT4 Register**

This register is reserved and the data is undefined when read.

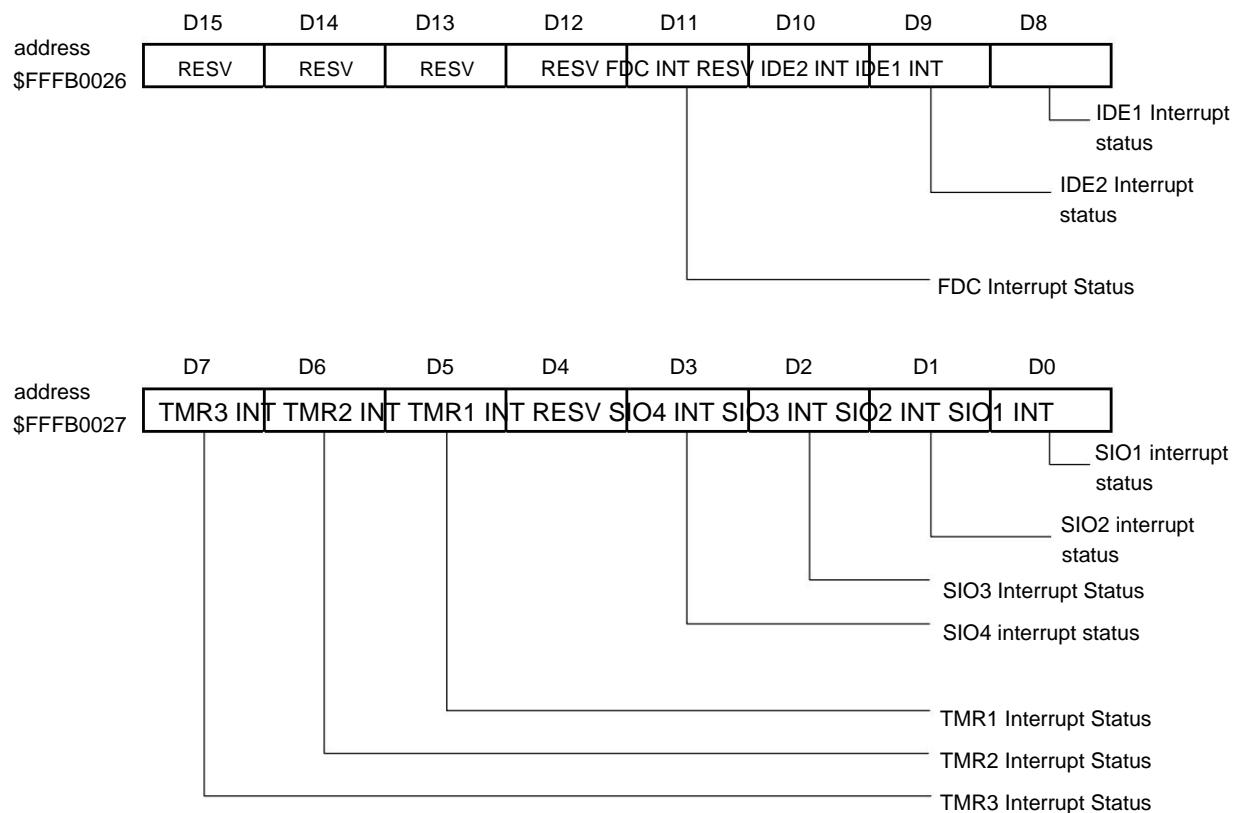
**7.2.6 STAT5 Register**

This register is reserved and the data is undefined when read.

**7.2.7 STAT6 Register**

This register is for interrupt status. FDC, IDE, serial, and timer interrupt information

You can know the information that has been set. You can clear the information by writing "1".



**a) SIO1 INT (SIO1 interrupt status)**

This bit recognizes the interrupt information from ch1 of UART (FDC37C935). If an interrupt occurs, will be set.

**b) SIO2 INT (SIO2 Interrupt Status)**

This bit recognizes the interrupt information from ch2 of UART (FDC37C935). If an interrupt occurs, will be set.

**c) SIO3 INT (SIO3 Interrupt Status)**

This bit recognizes the interrupt information from ch1 of DUART (PC15662). If an interrupt occurs, will be set.

**d) SIO4 INT (SIO4 Interrupt Status)**

This bit recognizes interrupt information from ch2 of DUART (PC15662). If an interrupt occurs, will be set.

**e) RESV (Reserved)**

Reserved. Data is undefined when read.

**f) TMR1 INT (TMR1 Interrupt Status)**

This bit recognizes the interrupt information from ch1 of the timer (MSM82C54). If an interrupt occurs, will be set.

**g) TMR2 INT (TMR2 Interrupt Status)**

This bit recognizes the interrupt information from ch2 of the timer (MSM82C54). If an interrupt occurs, will be set.

**h) TMR3 INT (TMR3 Interrupt Status)**

This bit recognizes the interrupt information from ch3 of the timer (MSM82C54). If an interrupt occurs, will be set.

## Chapter 7 Module Registers

### i) IDE1 INT (IDE1 Interrupt Status)

This bit recognizes the interrupt information from ch1 of IDE1 (FDC37C935). If an interrupt occurs, will be set.

### j) IDE2 INT (IDE2 Interrupt Status)

This bit recognizes the interrupt information from ch2 of IDE2 (FDC37C935). If an interrupt occurs, will be set.

### k) FDC INT (FDC Interrupt Status)

This bit recognizes the interrupt information from the FDC (FDC37C935). When an interrupt occurs, this bit is set. will be displayed.

## Chapter 8 Connector Pin Assignments

### 8.1 Connector assignment

The VMEbus, RS-232C, and Ethernet connector assignments for the AVME-148 module are shown below.

#### 8.1.1 VMEbus Connectors (P1, P2)

There are two connectors, P1 and P2, and the pin assignments of each connector are shown in Table 8-1 and Table 8-2.

Please be careful when using the A and C columns of the P2 connector, as they are assigned to IDE and FDD signals.

Sai.

Table 8-1 P1 connector PIN

No.	A row signal name	B row signal name	C row signal name
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
twenty one	IACKIN*	SERCLK(1)̄	A17
twenty two	IACKOUT*	SERDAT* (1)̄	A16
twenty three	AM4	GND	A15
twenty four	A07	IRQ7*	A14
twenty five	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

\* indicates not connected

Table 8-2 P2 connector PIN

No. A column	signal name B column	signal name C column	signal name
1	HRST*	+5V	PPM
2	HD0	GND	Reserved
3	HD1	Reserved	DRATE0*
4	HD2	A24	INDEX*
5	HD3	A25	DRV_SEL0*
6	HD4	A26	DRV_SEL1*
7	HD5	A27	DRV_SEL2*
8	HD6	A28	MO_ON*
9	HD7	A29	DIR
10	HD8	A30	STEP*
11	HD9	A31	WDATA*
12	HD10	GND	WGATE*
13	HD11	+5V	TRK0*
14	HD12	D16	WPT*
15	HD13	D17	RDATA*
16	HD14	D18	SIDE1*
17	HD15	D19	DSKCHG
18	HDRQ0/1	D20	Reserved
19	HDIOW*	D21	Reserved
20	HDIOR*	D22	GND
twenty one	HDIORDY	D23	GND
twenty two	HDAK0/1	GND	GND
twenty three	IRQ	D24	GND
twenty four	HDIO16*	D25	GND
twenty five	HDA2	D26	GND
26	HDA1	D27	GND
27	HDA0	D28	GND
28	HDCSO* /2*	D29	GND
29	HDCS1* /3*	D30	GND
30	GND	D31	GND
31	GND	GND	GND
32	GND	+5V	GND

### 8.1.2 RS-232C connectors (CN1, CN2, CN3, CN4)

One 8-pole modular jack with 4 sockets is used. CN1 is the serial port of FDC37C935 (Ultra I/O).

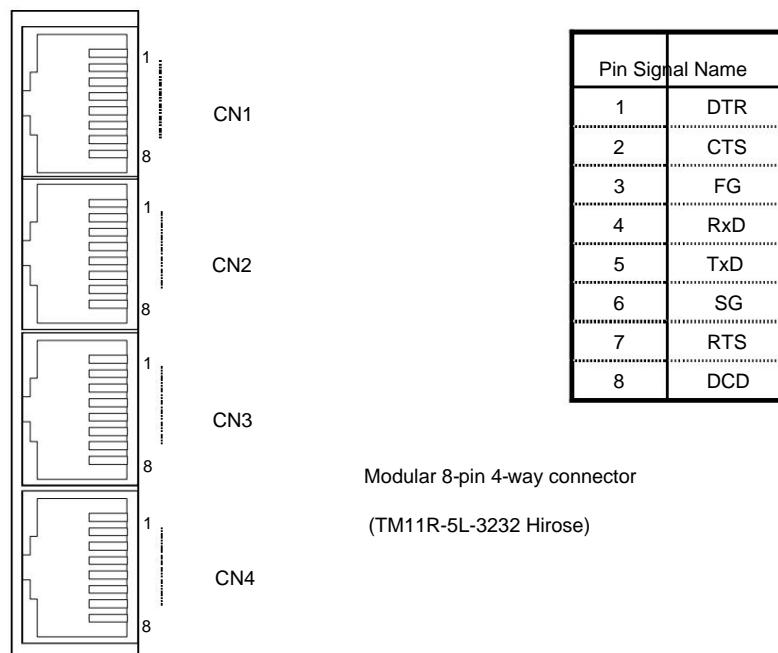
CN1 to serial port 1, CN2 to serial port 2, CN3 to serial port 1 of the PC15662 (DUART), CN4 to serial port 5 of the PC15662 (DUART), is connected to serial port 2.

The pin assignments for CN1 to CN4 are shown in Table 8-3. Also, the conversion connector to a 25-pin DSUB connector is

The sequence is shown in Figure 8-1.

Table 8-3 CN1, CN2, CN3, CN4 pin assignments

Pin number	Signal name	Signal direction	Function	Output
1	DTR	Input	Outputs data terminal ready state to external device.	
2	CTS	-	Inputs transmit enable from external device.	
3	FG	-		
4	RxD	Input	Frame ground. Inputs serial data from external device.	
5	TxD	Output	Outputs serial data to external device.	
6	SG	-	Signal	
7	RTS	Output	ground. Outputs request to send to external device.	
8	DCD	Input	Inputs carrier detect signal from external device.	



## Chapter 8 Connector Pin Assignments

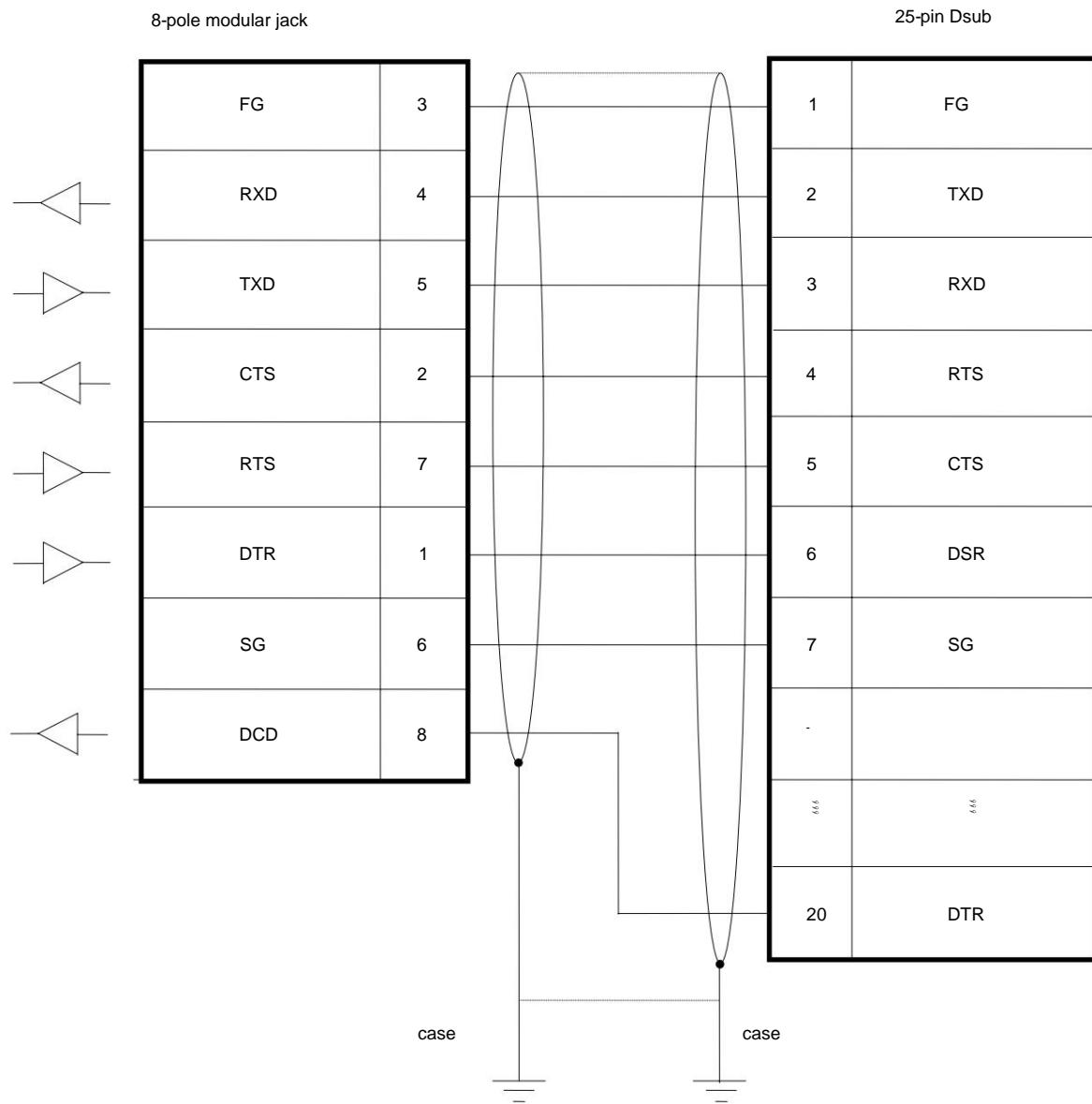


Figure 8-1 8-pole modular connector conversion cable connection diagram

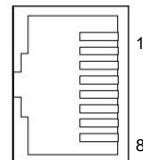
### 8.1.3 Ethernet Connector (LAN)

The LAN connector is equipped with a 10BaseT 8-pin modular connector as standard.

As shown in Table 8-4.

Table 8-4 LAN connector pin assignments

Pin Number	Signal Name	Signal direction
1	TD+	Function Output + Transmit
2	TD-	data +
3	RD+	Transmit data - Output - Input
4	SG	-
5	SG	+ Receive data +
6	RD-	Signal ground Signal input-
7	SG	ground
8	SG	Receive data - Signal ground Signal ground



Modular 8pin

(TM11R-5L-88 Hirose)

Pin	Signal Name
1	TD+
2	TD-
3	RD+
4	-
5	-
6	RD-
7	-
8	-

Chapter 8 Connector Pin Assignments

<memo>

Please contact us at the address below.

Aval Data Co., Ltd.

1-25-10 Asahimachi, Machida City, Tokyo 194-0023

TEL 042-732-1030      FAX: 042-732-1032

Homepage <http://www.avaldata.co.jp/>

Inquiry reception hours: Monday to Friday 9:00 to 17:00

## 68040 MPU module

## AVME-148

## User's Manual

January 31, 2002 First edition, 1st printing

September 24, 2004 First edition, 2nd printing

OM020000006B

Edited by Aval Data Co., Ltd. Published

by Aval Data Co., Ltd.

© 2004 AVALDATA CORPORATION



Head Office/Machida Office

1-25-10 Asahi-cho, Machida-shi, Tokyo 194-0023 TEL 0427-32-1030 FAX 0427-32-1032