μPD8251A/AF
PROGRAMMABLE COMMUNICATIONS INTERFACE (USART)

Description

The μPD8251A and μPD8251AF Universal Synchronous/Asynchronous Receiver/Transmitter (USART) are designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the 8085A or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format, and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

Features

- ☐ Asynchronous or synchronous operation
  - — Asynchronous:
    - -Five 8-bit characters
    - -Clock rate — 1, 16, or 64 x baud rate
    - -Break character generation
    - -Select 1, 1½, or 2 stop bits
    - -False start bit detector
    - -Automatic break detect and handling
  - — Synchronous:
    - -Five 8-bit characters
    - -Internal or external character synchronization
    - -Automatic sync insertion
    - -Single or double sync characters
- ☐ Baud rate (1x mode) — DC to 64K baud
- ☐ Full-duplex, double buffered transmitter and receiver
- ☐ Parity, overrun and framing flags
- ☐ Fully compatible with 8085A/μPD780 (Z80®), etc.
- ☐ All inputs and outputs are TTL-compatible
- ☐ Single +5 V supply, ±10%
- ☐ Separate device receive and transmit TTL clocks
- ☐ NMOS technology

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8251AC	28-Pin plastic DIP	3/5 MHz
μPD8251AFC	28-Pin plastic DIP	3/5 MHz

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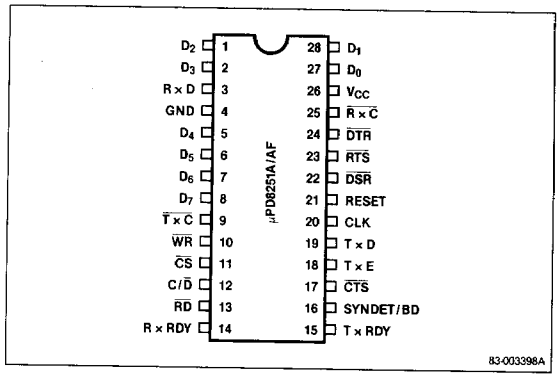
Pin Configuration



Pin Identification

No.	Symbol	Function
1, 2, 27, 28, 5–8	D_7–D_0	Data bus buffer
26	V_{DD}	V_{DD} supply voltage
4	GND	Ground
21	RESET	Reset
20	CLK	Clock pulse
10	$\overline{WR}$	Write data
13	$\overline{RD}$	Read data
12	C/$\overline{D}$	Control / data
11	$\overline{CS}$	Chip select
22	$\overline{DSR}$	Data set ready
24	$\overline{DTR}$	Data terminal ready
23	$\overline{RTS}$	Request to send
17	$\overline{CTS}$	Clear to send
15	TxRDY	Transmitter ready
18	TxE	Transmitter empty
9	$\overline{TxC}$	Transmitter clock
19	TxD	Transmitter data
14	RxRDY	Receiver ready
25	$\overline{RxC}$	Receiver clock
3	RxD	Receiver data
16	SYNDET / BD	Sync detect / break detect

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Pin Functions

Data Bus Buffer

An 8-bit, 3-state bi-directional buffer used to interface the USART to the processor data bus. Data is transmitted or received by the buffer in response to input/output or read/write instructions from the processor. The data bus buffer also transfers control words, command words, and status.

V_{DD} Supply Voltage

+5 V supply

Ground

Ground

Read/Write Control Logic

This logic block accepts inputs from the processor control bus and generates control signals for overall USART operation. The mode instruction and command instruction registers that store the control formats for device functional definition are located in the read/write control logic.

Reset

A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is $6\,t_{CY}$.

Clock Pulse

The CLK input provides for internal device timing and is usually connected to the phase 2 (TTL) output of the μPB8224 clock generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be at least 30 times the receiver or transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.

Write Data

A "zero" on this input instructs the USART to accept the data or control word which the processor is writing out on the data bus.

Read Data

A "zero" on this input instructs the USART to place the data or status information onto the data bus for the processor to read.

Control/Data

The control/data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word, or status information via the data bus. 0 = Data; 1 = Control.

Chip Select

A "zero" on this input enables the USART to read from or write to the processor.

Modem Control

The μPD8251A/51AF have a set of control inputs and outputs which may be used to simplify the interface to a modem.

Data Set Ready

The data set ready input can be tested by the processor via status information. The $\overline{DSR}$ input is normally used to test the modem data set ready condition.

Data Terminal Ready

The data terminal ready output can be controlled via the command word. The $\overline{DTR}$ output is normally used to drive modem data terminal ready or rate select lines.

Request to Send

The request to send output can be controlled via the command word. The $\overline{RTS}$ output is normally used to drive the modem request to send line.

Clear to Send

A "zero" on the clear to send input enables the USART to transmit serial data if the TxEN bit in the command instruction register is enabled (one).

Transmit Control Logic

The transmit control logic accepts and outputs all external and internal signals necessary for serial data transmission.

Transmitter Ready

Transmitter ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the status information for polled operation. Loading a character from the processor automatically resets TxRDY, on the leading edge.

Transmitter Empty

The transmitter empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal the end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE.

In the synchronous mode, a "one" on this output indicates that a sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.

Transmitter Clock

The transmitter clock controls the serial character transmission rate. In the asynchronous mode, the $\overline{\text{TxC}}$ frequency is a multiple of the actual baud rate. Two bits of the mode instruction select the multiple to be 1x, 16x, or 64x the baud rate. In the synchronous mode, the $\overline{\text{TxC}}$ frequency is automatically selected to equal the actual baud rate.

Note that for both synchronous and asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{\text{TxC}}$.

Transmitter Data

The transmit control logic outputs the composite serial data stream on this pin.

Receiver Control Logic

This block manages all activities related to incoming data.

Receiver Ready

The receiver ready output indicates that the receiver buffer is ready with an "assembled" character for input to the processor. For polled operation, the processor can check RxRDY using a status read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.

Receiver Clock

The receiver clock determines the rate at which the incoming character is received. In the asynchronous mode, the $\overline{\text{RxC}}$ frequency may be 1, 16 or 64 times the actual baud rate, but in the synchronous mode the $\overline{\text{RxC}}$ frequency must equal the baud rate. Two bits in the mode instruction select asynchronous at 1x, 16x, or 64x or synchronous operation at 1x the baud rate.

Unlike $\overline{\text{TxC}}$, data is sampled by the μPD8251A/51AF on the rising edge of $\overline{\text{RxC}}$. (Note 1)

Receiver Data

A composite serial data stream is received by the receiver control logic on this pin.

Sync Detect/Break Detect

The μPD8251A/51AF may be programmed through the mode instruction to operate in either the internal or external sync mode; the SYNDET/BD pin then functions as an output or input respectively. In the internal sync mode, the SYNDET output will go to a "one" when the μPD8251A/51AF has located the SYNC character in the receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a status read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251A/51AF to start assembling data character on the next falling edge of $\overline{\text{RxC}}$. The length of the SYNDET input should be at least one $\overline{\text{RxC}}$ period, but may be removed once the μPD8251A/51AF is in SYNC.

In the asynchronous mode, the SYNDET/BD pin functions as a break detect. The BD output will go high when a word of all zeros is received. This word consists of: start bit, data bits, parity bit, and one stop bit. Reset only occurs when Rx data returns to a logic one state or upon chip reset. The state of break detect can be read as a status bit.

Note:

(1) Since the μPD8251A/51AF will frequently be handling both the reception and transmission for a given link, the receive and transmit baud rates will be the same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or baud rate generator.
Examples:
If the baud rate equals 110 (Async):
$\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
$\overline{RxC}$ or $\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{RxC}$ or $\overline{TxC}$ equals 7.04 kHz (64x)
If the baud rate equals 300:
$\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
$\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
$\overline{RxC}$ or $\overline{TxC}$ equals 19.2 kHz (64x) A only

Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.5 V to +7 V
Input voltage, V_I	−0.5 V to +7 V
Output voltage, V_O	−0.5 V to +7 V
Operating temperature, T_{OPT}	−0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

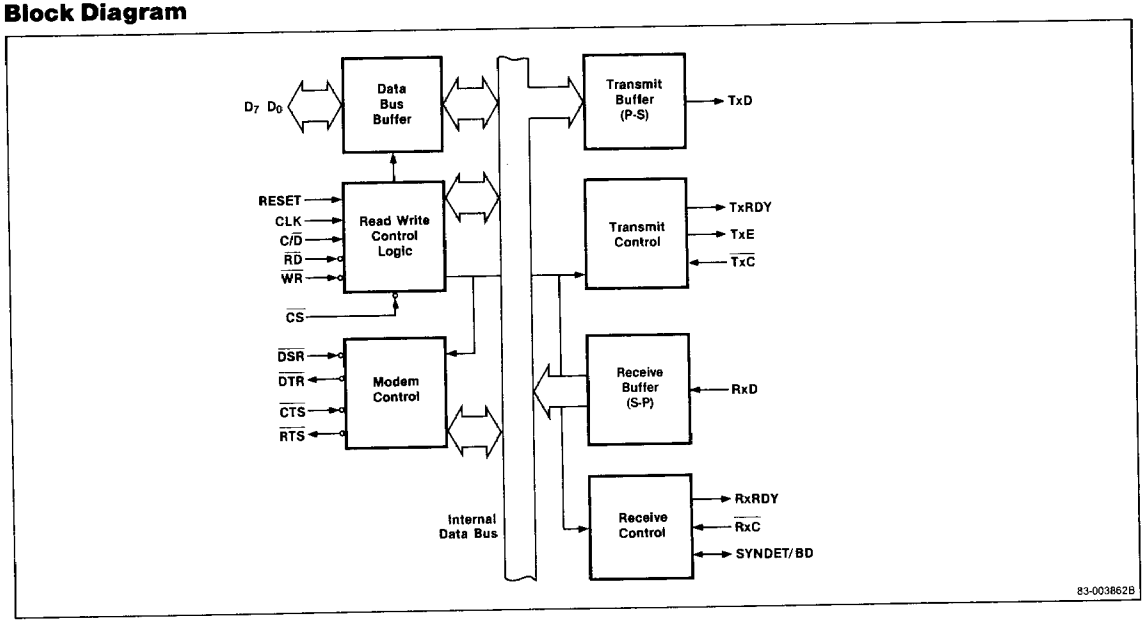
$T_A = 25°C$, $V_{CC} = GND = 0\ V$, $f_c = 1.0\ MHz$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			10	pF	(Note 1)
I/O capacitance	C_{IO}			20	pF	(Note 1)

Note:

(1) All unmeasured pins returned to GND.

Block Diagram



DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, GND = 0 V

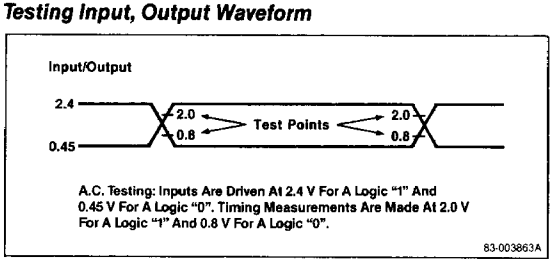
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.5		+0.8	V	
Input voltage high	V_{IH}	2		V_{CC}	V	
Output voltage low	V_{OL}			+0.45	V	μPD8251: $I_{OL} = 1.7$ mA μPD8251A: $I_{OL} = 2.2$ mA
Output voltage high	V_{OH}	2.4			V	μPD8251: $I_{OH} = -100\ \mu A$ μPD8251A: $I_{OH} = -400$ mA
Output float leakage current	I_{OFL}			±10	μA	$V_{OUT} = 0.45$ V
				10	μA	$0.45\ V \leq V_{OUT} \leq V_{CC}$
Input load current	I_{IL}			10	μA	$0.45\ V \leq V_{IN} \leq V_{CC}$
Power supply current	I_{CC}			100	mA	All outputs = logic 1

AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$; GND = 0 V

Parameter	Symbol	Limits μPD8251A Min	Max	μPD8251AF Min	Max	Unit	Test Conditions
Read							
Address stable before $\overline{RD}$, ($\overline{CS}$, $\overline{CD}$)	t_{AR}	50		0		ns	(Note 7)
Address hold time for $\overline{RD}$, ($\overline{CS}$, $\overline{CD}$)	t_{RA}	50		0		ns	(Note 7)
$\overline{RD}$ pulse width	t_{RR}	250		200		ns	
Data delay from $\overline{RD}$	t_{RD}		250		140	ns	μPD8251A; $C_L = 150$ pF, (Note 8)
$\overline{RD}$ to data floating	t_{DF}	10	100	10	80	ns	
Write							
Address stable before $\overline{WR}$	t_{AW}	50		0		ns	
Address hold time for $\overline{WR}$	t_{WA}	50		0		ns	
$\overline{WR}$ pulse width	t_{WW}	250		200		ns	
Data set-up time for $\overline{WR}$	t_{DW}	150		100		ns	
Data hold time for $\overline{WR}$	t_{WD}	30		0		ns	
Recovery time between $\overline{WR}$'s	t_{RV}	6		6		t_{CY}	(Note 2)
Other Timing							
Clock period	t_{CY}	0.32	1.35	0.20	1.35	μs	(Note 3)
Clock pulse width high	$t_{\phi W}$	140	$t_{CY} - 90$	70	$t_{CY} - 40$	ns	
Clock pulse width low	$t_{\phi W}$	90		40		ns	
Clock rise and fall time	t_R, t_F	5	20	5	20	ns	
TxD delay from falling edge of TxC	t_{DTx}		1		1	μs	
Rx data set-up time to sampling pulse	t_{SRx}	2				μs	
Rx data hold time to sampling pulse	t_{HRx}	2				μs	
Transmitter input clock frequency	f_{Tx}		64	DC	64	kHz	1x baud rate
			310	DC	310	kHz	16x baud rate
			615	DC	615	kHz	64x baud rate
Transmitter input clock pulse width	t_{TPW}	12		12		t_{CY}	1x baud rate
		1		1		t_{CY}	16x and 64x baud rate
Transmitter input clock pulse delay	t_{TPD}	15		15		t_{CY}	1x baud rate
		3		3		t_{CY}	16x and 64x baud rate

Testing Input, Output Waveform



A.C. Testing: Inputs Are Driven At 2.4 V For A Logic "1" And 0.45 V For A Logic "0". Timing Measurements Are Made At 2.0 V For A Logic "1" And 0.8 V For A Logic "0".

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AC Characteristics (cont)

Parameter	Symbol	Limits μPD8251A Min	Limits μPD8251A Max	Limits μPD8251AF Min	Limits μPD8251AF Max	Unit	Test Conditions
Other Timing (cont)							
Receiver input clock frequency	f_{Rx}		64	DC	64	kHz	1x baud rate
			310	DC	310	kHz	16x baud rate
			615	DC	615	kHz	64x baud rate
Receiver input clock pulse width	t_{RPW}	12		12		t_{CY}	1x baud rate
		1		1		t_{CY}	16x and 64x baud rate
Receiver input clock pulse delay	t_{RPD}	15		15		t_{CY}	1x baud rate
		3		3		t_{CY}	16x and 64x baud rate
TxRDY delay from center of data bit	t_{Tx}		8		8	t_{CY}	(Note 9)
TxRDY ↓ from leading edge of $\overline{WR}$	$t_{TxRDY\ CLEAR}$				300	ns	(Note 9)
RxRDY delay from center of data bit	t_{RX}		24		20	t_{CY}	
Internal SYNDET delay from center of data bit	t_{IS}		24			t_{CY}	(Note 9)
RxRDY ↓ from leading edge of $\overline{RD}$	$t_{RxRDY\ CLEAR}$				300	ns	(Note 9)
External SYNDET set-up time before falling edge of $\overline{RxC}$	t_{ES}	16		18		t_{CY}	(Note 9)
TxEMPTY delay from center of data bit	t_{TxE}		20		20	t_{CY}	(Note 9)
Control delay from rising edge of $\overline{WR}$ ($\overline{TxE}$, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}		8		8	t_{CY}	(Note 9)
Control to $\overline{RD}$ set-up time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	20		20		t_{CY}	(Note 9)

Note:

(1) AC timing measured at $V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V, and with test load circuit below.

(2) This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

(3) The TxC and RxC frequencies have the following limitations with respect to CLK:
For 1x baud rate, f_{Tx} or $f_{Rx} \leq \frac{1}{(30\ t_{CY})}$
For 16x and 64x baud rate, f_{Tx} or $f_{Rx} \leq \frac{1}{(4.5\ t_{CY})}$

(4) Reset pulse width = $6\ t_{CY}$ minimum.

(5) $t_{TxRDYCCR} - 2\ t_{CY} + t_{\phi} + t_R + 200$ ns

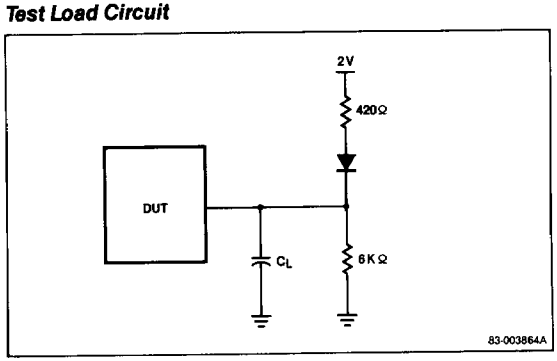
(6) $t_{RxRDYCCR} - 2\ t_{CY} + t_{\phi} + t_R + 170$ ns

(7) Chip Select (CS) and Command/Data (C/D) are considered as addresses.

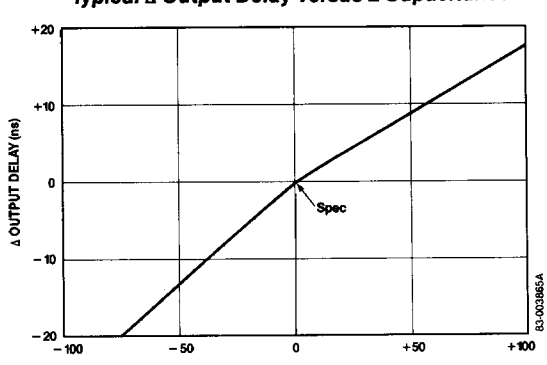
(8) Assumes that address is valid before R_O ↓.

(9) Status update can have a miximum delay of 28 clock periods from the event affecting the status.

Test Load Circuit

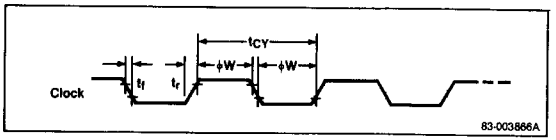


Typical Δ Output Delay Versus Δ Capacitance

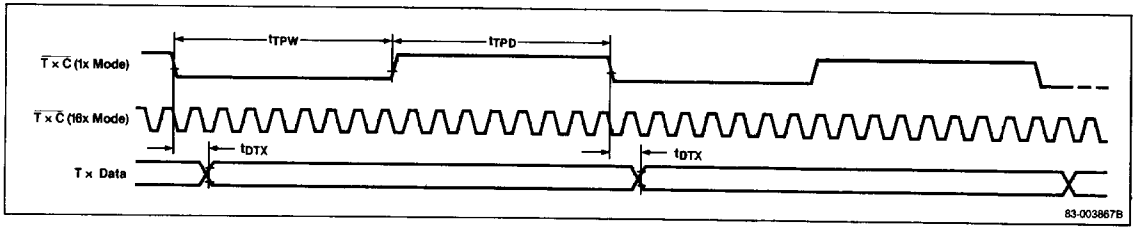


Timing Waveforms

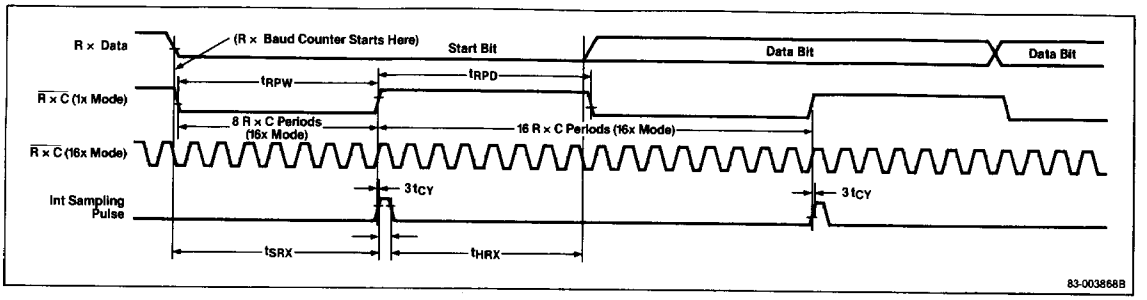
System Clock Input



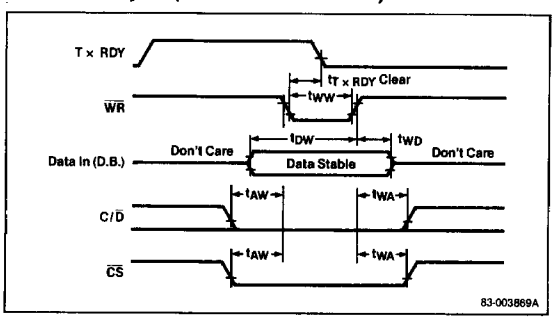
Transmitter Clock and Data



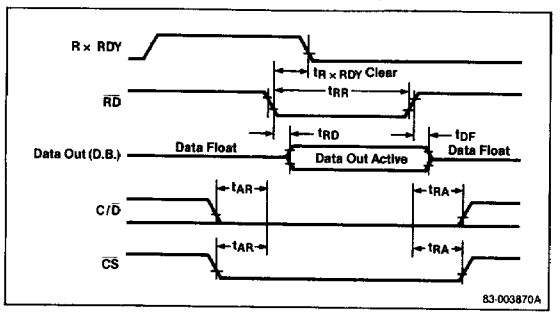
Receiver Clock and Data



Write Data Cycle (Processor → USART)



Read Data Cycle (Processor ← USART)



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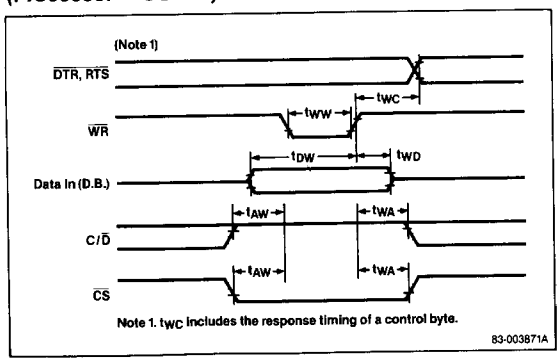
Timing Waveforms (cont)

Write Control or Output Port Cycle (Processor → USART)



Note 1. t_{WC} includes the response timing of a control byte.

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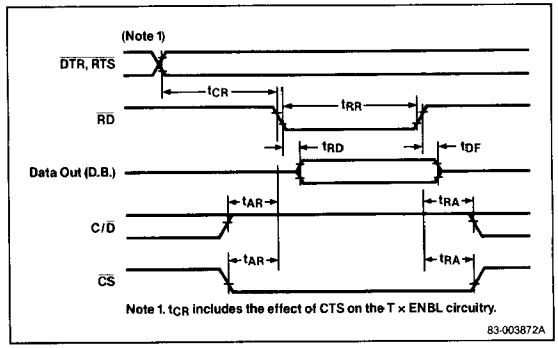
Read Control or Input Port Cycle (Processor ← USART)



Note 1. t_{CR} includes the effect of CTS on the T x ENBL circuitry.

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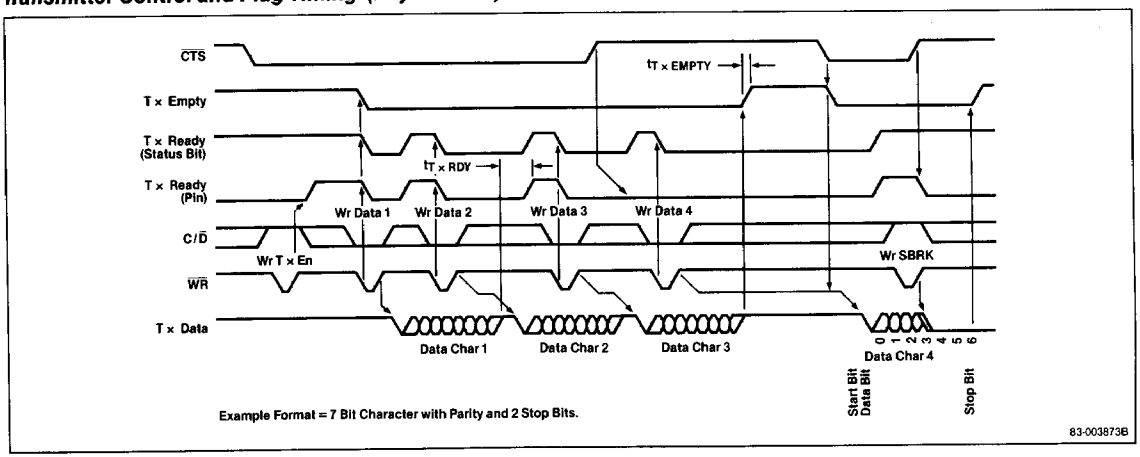
Transmitter Control and Flag Timing (Async Mode)



Example Format = 7 Bit Character with Parity and 2 Stop Bits.

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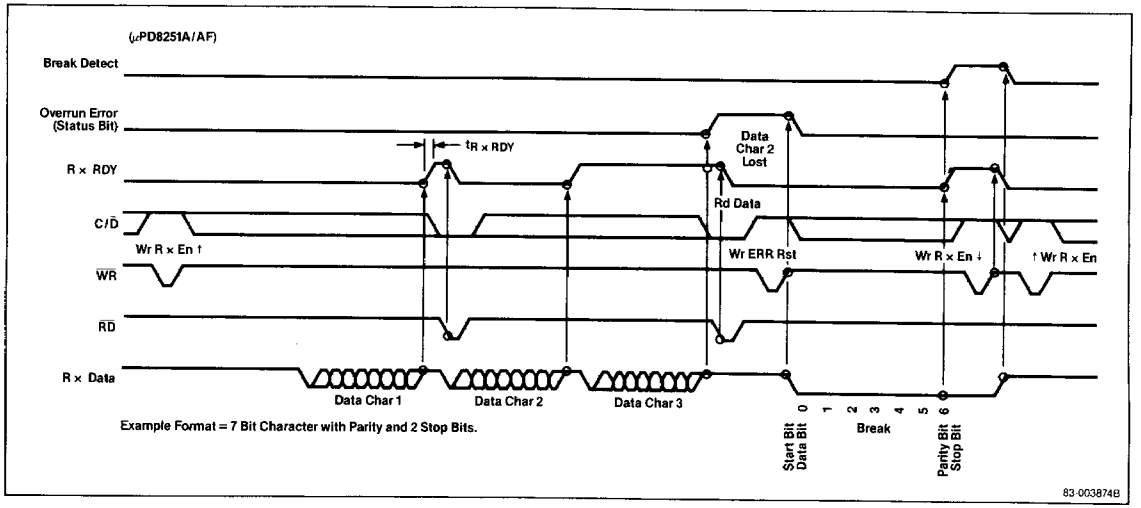
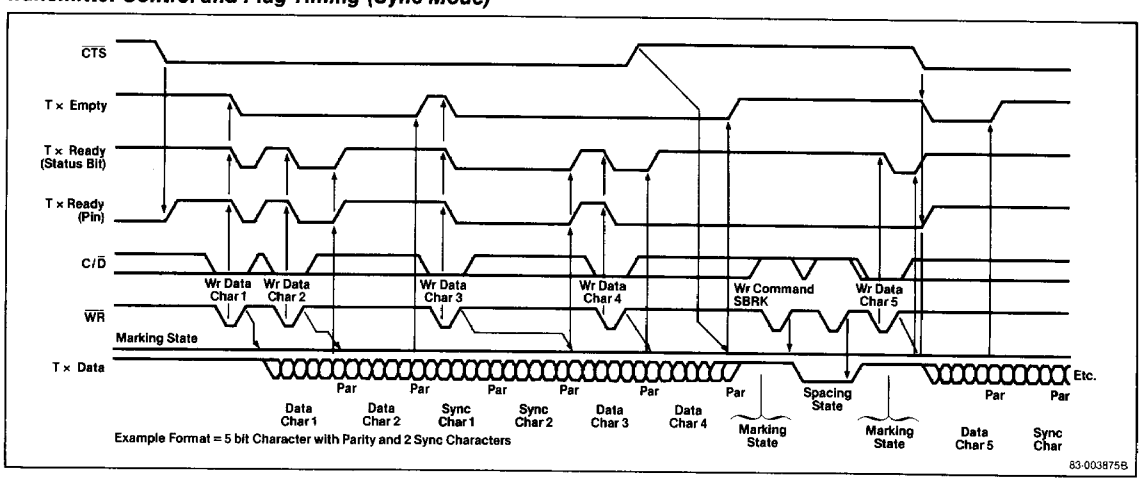
Timing Waveforms (cont)

Receiver Control and Flag Timing (Async Mode)



Transmitter Control and Flag Timing (Sync Mode)



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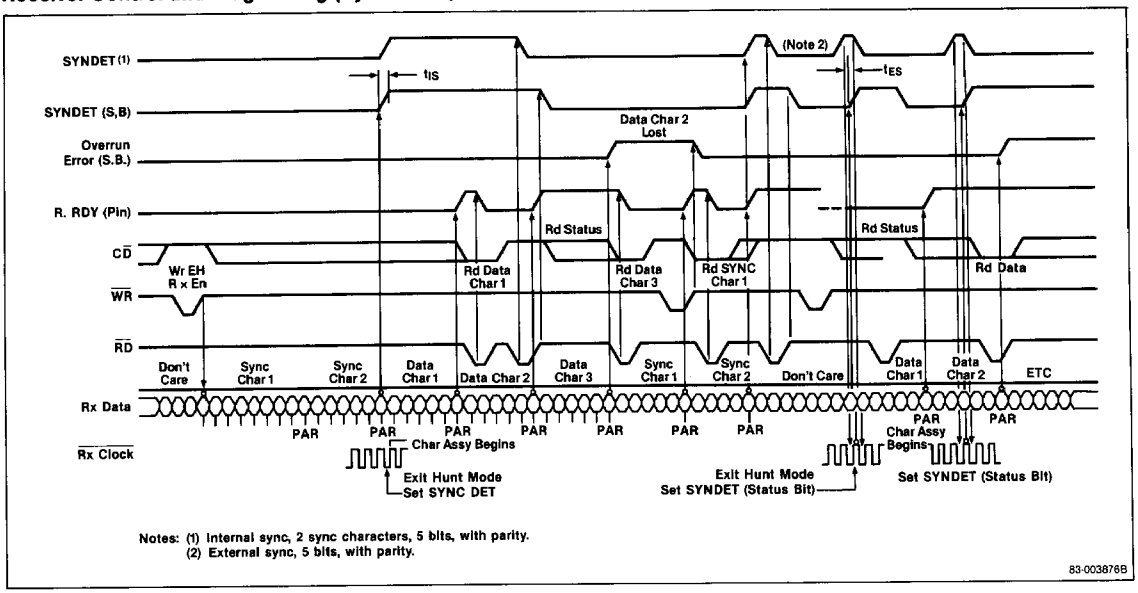
Timing Waveforms (cont)

Receiver Control and Flag Timing (Sync Mode)



Notes: (1) Internal sync, 2 sync characters, 5 bits, with parity.
(2) External sync, 5 bits, with parity.

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μPD8251AF Enhancements

μPD8251A	μPD8251AF
A previously loaded data character will be retransmitted if Tx was disabled before TxEMPTY by TxEnable ↓ or $\overline{CTS}$ ↑, and is re-enabled by TxEnable ↑ or $\overline{CTS}$ ↓ before a new data character is sent to μPD8251A by the CPU.	A previously loaded character will be flushed out and not transmitted on $\overline{CTS}$ ↓ or TxEnable ↑.
Break detect does not always reset upon RxData returning to a '1' during the last bit of the character following the break. Break detect will latch up, and the device must be cleared by device reset.	Break detect will reset on RxData going to '1'.
On TxEnable ↓ or $\overline{CTS}$ ↑ during the first character of a double-character sync output, the second sync character will not be output.	Will output both sync characters on TxEnable ↓ or $\overline{CTS}$ ↑.
If the status register is read during a status update, an erroneous status read may result.	Some valid status (either new or old) will always be available.
In Rx mode, a hardware or software reset does not force asynchronous mode, clear hunt condition, or require a proper line initialization (1 to 0 transition) before receiving. This may cause reception of garbage characters.	Reset will clear Rx hunt condition, force asynchronous operation (64x clock), and require a proper line initialization before receiving anything.
Break detect will occur on the first complete (start bit to stop bit) break. This situation could be confused with a null frame (all zeros) that also has a framing error.	Will give a framing error at the end of the first complete or partial break and will give a break detect at the stop bit position of the second contiguous break character.
Sync detect does not reset on status read.	Sync detect will reset on status read.
RxRDY clears within 2 t_{CY}'s of $\overline{RD}$ leading edge.	RxRDY will clear on $\overline{RD}$ leading edge.
TxEMPTY oscillates with internal clock when TxEnable ↓ or $\overline{CTS}$ ↑.	TxEMPTY will not oscillate this way.
TxRDY and TxEMPTY clear on $\overline{WR}$ trailing edge (data).	TxRDY, TxEMPTY will clear on $\overline{WR}$ leading edge.
Enter hunt command affects asynchronous Rx by loss of data characters.	Enter hunt will not affect asynchronous operation.
Writing a command will sometimes clear TxRDY or TxEMPTY if C / $\overline{D}$ set up or hold is marginal. Reading status will sometimes clear RxRDY if C / $\overline{D}$ set up or hold is marginal.	C / $\overline{D}$ set up and hold margin will be improved.

μPD8251AF Enhancements (cont)

μPD8251A	μPD8251AF
Rx data overrun error will not occur and garbage data may result if $\overline{RD}$ and $\overline{CS}$ are active during an internal data update.	Will indicate an overrun error properly.
In asynchronous mode, after a reset, the first TxD bit may be shifted out on either the first or second $\overline{TxC}$ ↓ edge.	The first TxD bit will be shifted out on the first $\overline{TxC}$ ↓ edge.
RxRDY can glitch when CLK does not have a fixed phase relationship to $\overline{RxC}$.	RxRDY will not glitch.
The receiver occasionally gives an extra character following the end of break condition.	No extra characters will occur.

Functional Description

The μPD8251A/51AF Universal Synchronous/Asynchronous Receiver/Transmitters are designed specifically for 8085A microcomputer systems but work with most 8-bit processors. Operations of the μPD8251A/51AF, like other I/O devices in the 8085A family, are programmed by system software for maximum flexibility.

In the receive mode, the μPD8251A/51AF converts incoming serial format data into parallel data and makes certain format checks. In the transmit mode, it formats parallel data into serial form. The device also supplies or removes characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

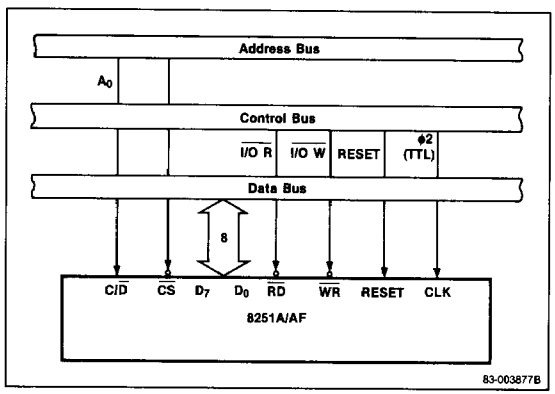
Truth Table

$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	MODE
0	0	1	0	μPD8251A/51AF → Data bus
0	1	0	0	Data bus → μPD8251A/51AF
1	0	1	0	Status → Data bus
1	1	0	0	Data bus → Control
X	X	X	1	Data bus → 3-state
X	1	1	0	Data bus → 3-state

Transmit Buffer

The transmit buffer receives parallel data from the data bus buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD pin.

μPD8251A/51AF Interface to 8085A Standard System Bus



Receive Buffer

The receive buffer accepts serial data input at the RxD pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require fewer than eight bits, the μPD8251A/51AF set the extra bits to "zero".

Operation

A set of control words must be sent to the μPD8251A/51AF to define the desired mode and communications format. The control words will specifiy the baud rate factor (1x, 16x, 64x), character length (5 to 8), number of STOP bits (1, 1½, 2) asynchronous or synchronous mode, SYNDET (IN or OUT), parity, etc.

After receiving the control words, the μPD8251A/51AF are ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251A/51AF may receive serial data; and after receiving an entire character, the RxRDY

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output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note:

The μPD8251A/51AF may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251A/51AF cannot transmit until the TxEN (transmitter enable) bit has been set by a command instruction and until the $\overline{CTS}$ (clear to send) input is a "zero". TxD is held in the "marking" state after reset awaiting new control words.

USART Programming

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A RESET (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D} = 1$) followed by a software reset command instruction (40 Hex) can be used to initialize the μPD8251A/51AF.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

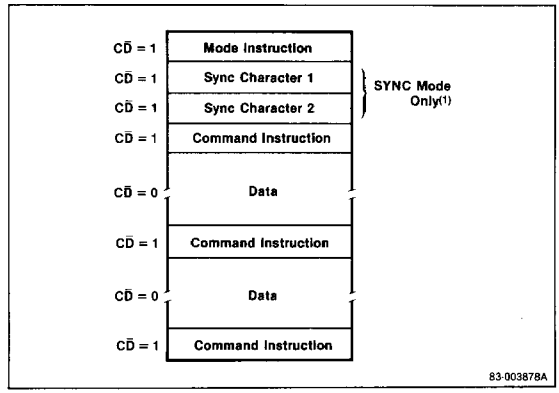
Mode Instruction

This control word specifies the general characteristics of the interface regarding the synchronous or asynchronous mode, baud rate factor, character length, parity, and number of stop bits. Once the mode instruction has been received, SYNC characters or command instructions may be inserted depending on the mode instruction content.

Command Instruction

This control word will be interpreted as a SYNC character definition if immediately preceded by a mode instruction which specified a synchronous format. After the SYNC character(s) are specified or after an asynchronous mode instruction, all subsequent control words will be interpreted as an update to the command instruction. Command instruction updates may occur at any time during the data block. To modify the mode instruction, a bit may be set in the command instruction which causes an internal reset which allows a new mode instruction to be accepted.

Typical Data Block



Mode Instruction Definition

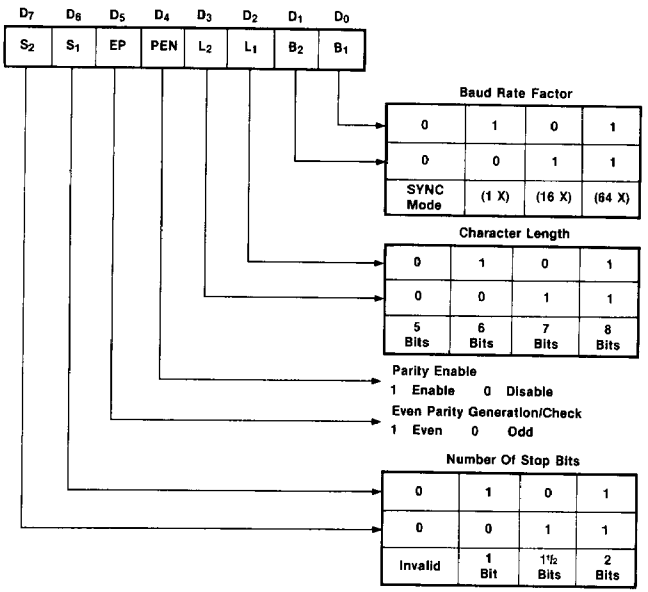
The μPD8251A/51AF can operate in either asynchronous or synchronous communication modes. Understanding how the mode instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components (one asynchronous and the other synchronous) which share the same support circuits and package. Although the format definition can be changed at will or "on the fly," the two modes will be explained separately for clarity.

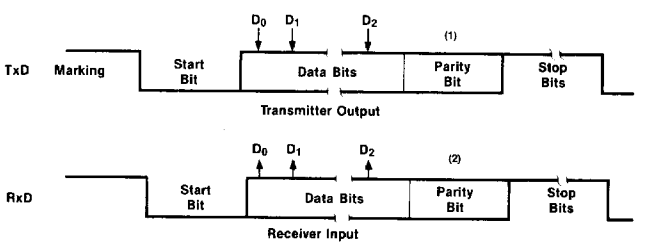
Asynchronous Transmission

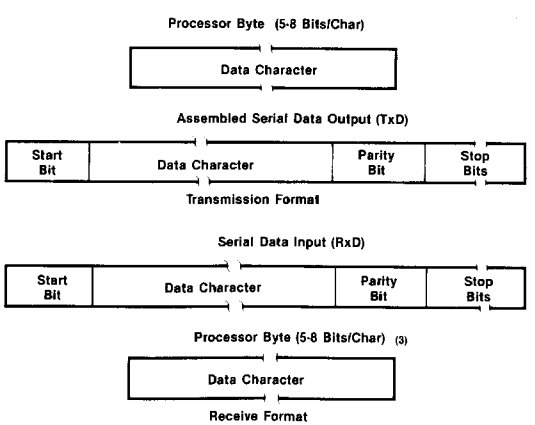
When a data character is written into μPD8251A/51AF, the USART automatically adds a start bit (low level or "space") and the number of stop bits (high level or "mark") specified by the mode instruction. If parity has been enabled, an odd or even parity bit is inserted just before the stop bit(s), as specified by the mode instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the mode instruction.

If no data characters have been loaded into the μPD8251A/51AF, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the start bit of the next character provided by the processor. TxD may be forced to send a break (continuously low) by setting the correct bit in the command instruction.

Mode Instruction Format for Asynchronous Mode







Notes:

(1) Generated by μPD8251A/AF

(2) Does not appear on the Data Bus.

(3) If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero."

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Asynchronous Receive

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a start bit and a new character. The start bit is checked by testing for a "low" at its nominal center as specified by the baud rate. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and stop bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the stop bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid stop bit, the input character is loaded into the parallel data bus buffer of the μPD8251A/51AF and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the command instruction. Error flag conditions will not stop subsequent USART operation.

Synchronous Transmission

As in asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251A/51AF receive the first character (usually a SYNC character) from the processor. After a command instruction has set TxEN and after clear to send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

Once transmission has started, synchronous mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251A/51AF transmit buffer becomes empty, the SYNC character(s) loaded directly following the mode instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251A/51AF become empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the transmitter buffer is empty and SYNC characters are begin transmitted. TxEMPTY is automatically reset by the next character from the processor.

Synchronous Receive

In synchronous receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the enter hunt (EH) bit has been set by a command instruction, the receiver goes into the HUNT mode.

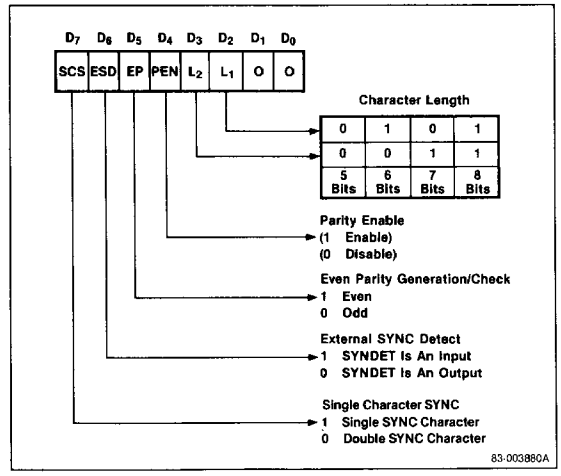
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the receive buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251A/51AF leave the HUNT mode and are in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a status read.

If external SYNC has been specified in the mode instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

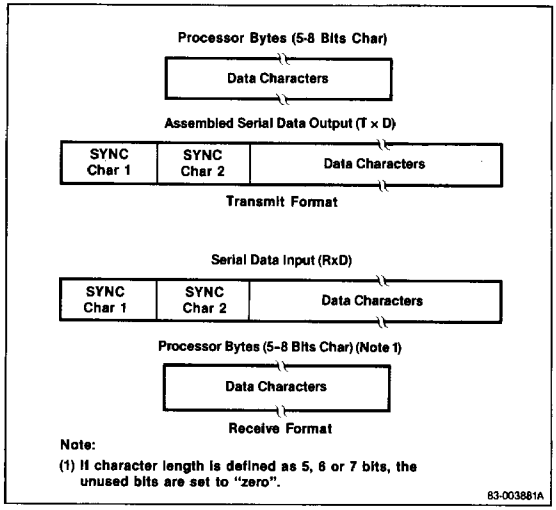
Parity and overrun errors are treated the same in the synchronous as in the asynchronous mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the synchronous format.

The processor may command the receiver to enter the HUNT mode with a command instruction which sets enter hunt (EH) if synchronization is lost.

Mode Instruction Format for Synchronous Mode



Transmit/Receive Format Synchronous Mode



Command Instruction Format

After the functional definition of the μPD8251A/51AF has been specified by the mode instruction and the SYNC character(s) have been entered (if in SYNC mode), the USART is ready to receive command instructions and begin communication. A command instruction is used to control the specific operation of the format selected by the mode instruction. Enable transmit, enable receive, error reset and modem controls are controlled by the command instruction.

After the mode instruction and the SYNC character(s) (as needed) are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the command instruction register. A reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251A/51AF to interpret the next "control write", which must immediately follow the reset, as a mode instruction.

Status Read Format

It is frequently necessary for the processor to examine the status of an active interface device to determine if errors have occurred or if there are other conditions which require a response from the processor. The μPD8251A/51AF have features which allow the processor to read the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device status information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251A/51AF to be used in both polled and interrupt driven environments. Status update can have a maximum delay of 28 clock periods in the μPD8251A/51AF.

Parity Error

When a parity error is detected, the PE flag is set. It is cleared by setting the ER bit in a subsequent command instruction. PE begin set does not inhibit USART operation.

Overrun Error

If the processor fails to read a data character before the one following is available, the OE flag is set. It is cleared by setting the ER bit in a subsequent command instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

Framing Error

If a valid STOP bit is not detected at the end of a character, the FE flag is set (ASYUNC mode only). It is cleared by setting the ER bit in a subsequent command instruction. FE being set does not inhibit USART operation.

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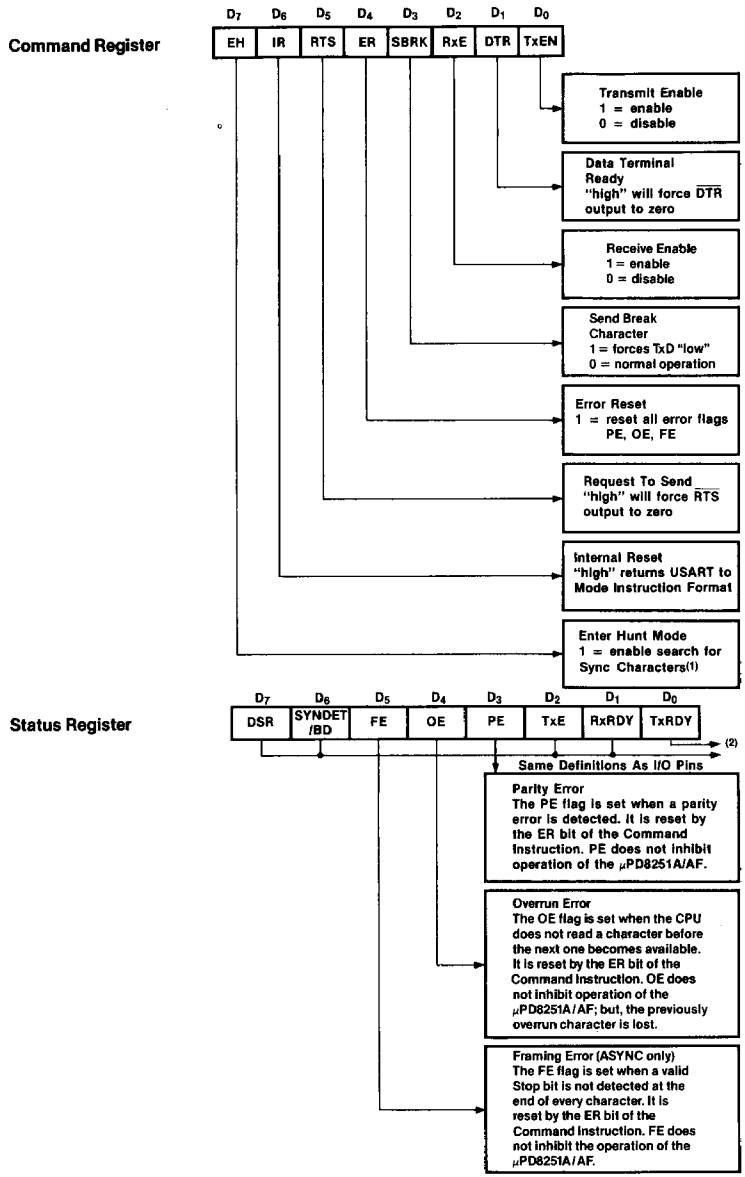
Command and Status Register Formats



Notes:

(1) **NO effect in ASYNC mode.**

(2) **TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:**

$$\text{TxRDY status bit} = \text{DB Buffer Empty}$$

$$\text{TxRDY (pin 15)} = \text{DB Buffer Empty} \cdot \overline{\text{CTS}} \cdot \text{TxE}_n$$

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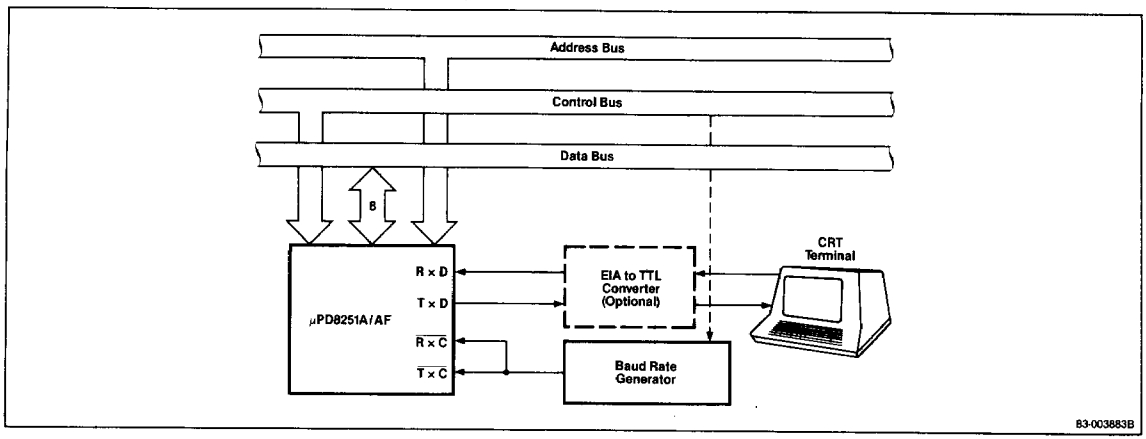
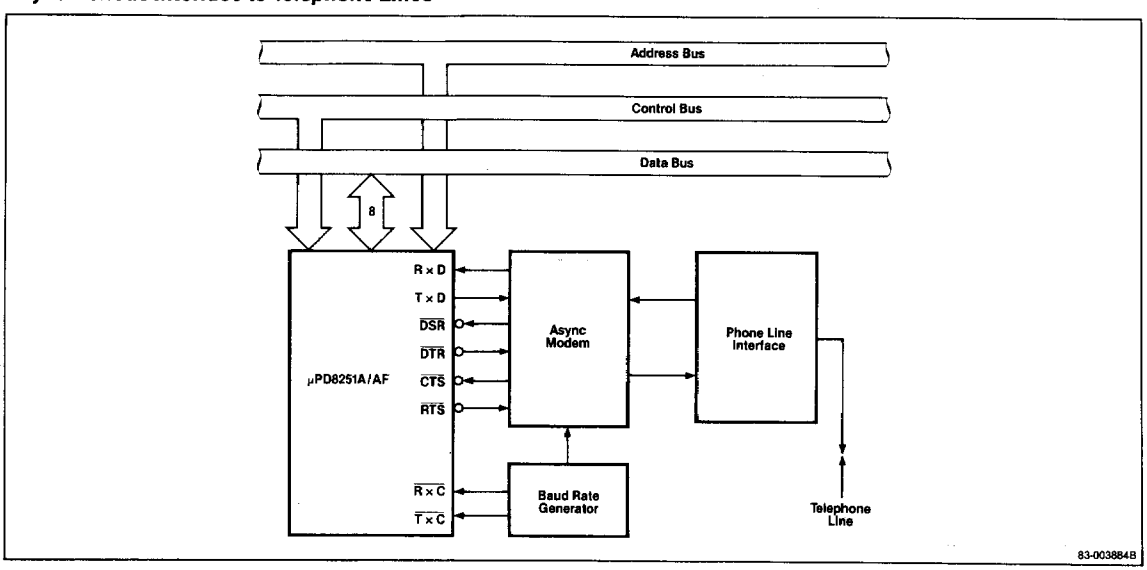
Asynchronous Serial Interface to CRT Terminal, DC to 9600 Baud



Asynchronous Interface to Telephone Lines



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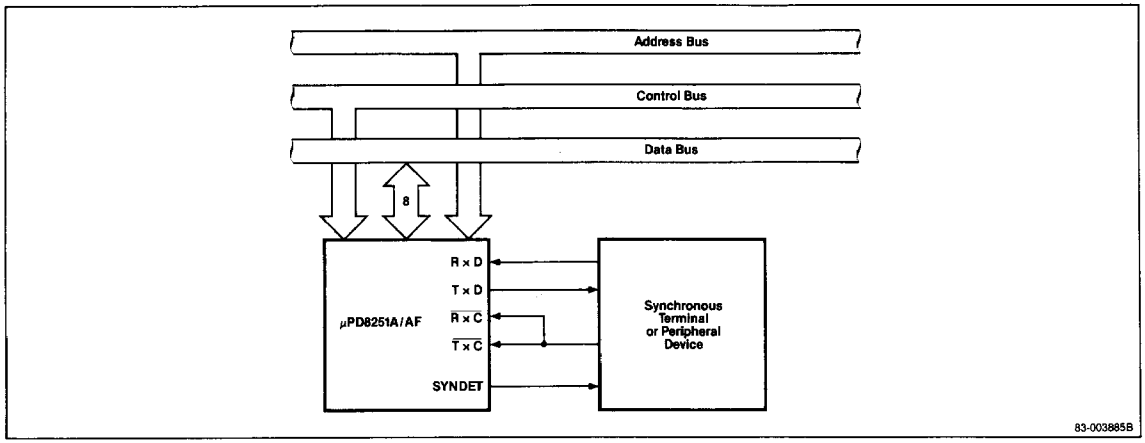
Synchronous Interface to Terminal or Peripheral Device



Synchronous Interface to Telephone Lines