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DSP Division

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1. Introduction

1.1 Scope

This document describes the power modes available in the CEVA-XM4™ DSP core, as well as the hardware and software considerations involved in its power implementation.

1.2 Related Documents

The following documents are related to the information in this document:

1. *CEVA-XM4 Database Reference Guide*
2. *CEVA-XM4 Backend Flow Reference Guide*
3. *CEVA-XM4 Integration Reference Guide*
4. *CEVA-XM4 Architecture Specification*

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2. Power Saving Modes

The following sections describe the power management modes available in the CEVA-XM4 DSP core. The core supports the following power modes:

- Standard Operation mode (which includes the Free Run, Dynamic Power Saving (DPS), and Light Sleep modes)
- Deep Sleep mode
- Shutdown mode

2.1 Standard Operation Mode

In this mode, several clock activation policies can be used to enable or disable different clock-gating approaches. For more details, see the *CEVA-XM4 Architecture Specification.*

2.2 Deep Sleep Mode

This mode is intended for use when the core is not active and a long recovery time is acceptable. In this mode, the power to the core and MSS is shut down, while the memories' power is kept for data retention.

Important: *Retention and shutdown to memory are dependent on the memory vendor supplier and not on CEVA. The PSU provides only the required retention/shutdown indications.*

For more details, see Section 3.2.

2.3 Shutdown Mode

This mode is intended for use when the core has no active tasks and there is no need for data transfer to or from the MSS for a long period of time. In this mode, the entire DSP, MSS, debug block, and memories are in power off. This means that no data is saved in the memories or in the CEVA-XM4 registers.

For more details, see Section 3.3.

Note: *The power shutdown implementation is done independently by the PSU but requires backend implementation provided by CEVA. For more details, see the CEVA-XM4 Backend Flow Reference Guide.*

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2.4 Debug Block Configuration Mode Bit

The Debug Block Configuration (DBC) mode bit enables and disables the debug module (Emulation unit). The following power modes are supported:

- **Operational Production**: Debug is disabled, and no power or clock is provided to the OCEM and RTT.
- **Debug**: The Emulation unit (that is, the OCEM and RTT) is fully functional and always toggling.

For more details, see Section 3.4.

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3. Design Considerations

3.1 Memory ON/OFF/Retention States

Each memory block can be separately defined as ON, OFF, or Retention while the core/MSS are ON. The following sections describe only the PSU/memory blocks interface.

The PSU launches the following internal CEVA-XM4 control signals for each memory block:

- *psu_block_deep_sleep_switch_r*: For memory retention (in some vendor specifications, this is called **Deep Sleep**)
- *psu_domain_shut_down_switch_r*: For memory shutdown

The PSU also generates the following CEVA-XM4 output indications:

- *cevaxm4_psu_sys_pshtdwn_r*: Retention indication bus
- *cevaxm4_psu_pshtdwn_r*: Shutdown indication bus

3.1.1 Special Considerations

- Memory OFF/Retention states are dependent on the memory modules provided by the vendor. These abilities should be integrated as part of the vendor's memory solution.
- Turning the memory block ON/OFF is done only via a *psu* instruction.
- When the memory blocks are switched OFF/Retention, the user is responsible for ensuring that there are no transactions to the relevant block.
- The signals' polarity should be considered carefully when embedding the CEVA-XM4 CPF/UPF file into the entire chip CPF/UPF.
- The PSU sets the internal *psu_block_deep_sleep_switch_r*/ *psu_domain_shut_down_switch_r* signals to low under the OFF/Retention states respectively.

  When set to ON, these signals are set to high.

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3.1.2 Enter/Exit Retention State Sequence

The following is the sequence for entering the Retention state:

- Bits [9:4] of the PSVM register (CPM address 0x0E50) are written with the value 6'b010100 by using the *PCU.psu{deepsleep} #0x14* instruction.

  This means that the PMSS TCM, PMSS cache, data TCM block 1, and data TCM block 3 are going into the Retention state (their relevant bits in the *psu* instruction are **0**).

The following is the sequence for exiting the Retention state:

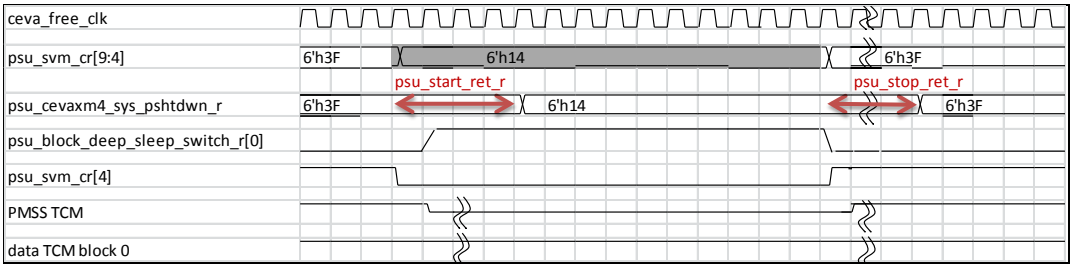
- The relevant bits in the PSVM register are written by ones with the same *psu* instruction.

  The user can access the relevant block only after the relevant *cevaxm4_psu_sys_pshtdwn_r* bus bits are asserted (*cevaxm4_psu_sys_pshtdwn_r* indicates the blocks' retention status).

When the polarity is high, the block is in regular mode; when low, it is in Retention state.

Example 3-1 shows entering/exiting the Retention state.

Example 3-1: Entering/Exiting Retention State



3.2 Deep Sleep Mode

This mode is executed by the *psu* instruction that writes zeros to all retention bits and to the core/MSS Shutdown bit.

The usage is:

```
psu {deepsleep} #0x0 -> All memories are in retention
psu {shutdown} #0x7E -> Core is in shutdown
```

To exit this mode, *stop_sd* (a cevaxm4 input) should be asserted for at least two cycles.

After the core exits Shutdown mode, memories are enabled via a *psu* instruction.

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3.2.1 Special Considerations

- The user can choose to stop the root clock to the CEVA-XM4 DSP core only after *cevaxm4_psu_dsp_idle_r* rises.
- If the root clock was stopped, the user must restore the root clock before *stop_sd* rises. The PSU cannot start the recover sequence without a clock.
- There is no need for *ceva_global_rst_n* upon recovery. The PSU resets the core/MSS internally (*stop_sd* triggers this chain of events).
- To enable the PSU to synchronize the *stop_sd* pulse, it should be active longer than one core clock.
- Because the core is reset by the PSU ("beginning of time" situation), the user must also assert *boot* and *vector* inputs with *stop_sd*. The *vector* value must point to the external memory to start loading the new program.
- Program TCM and Program Cache are enabled automatically after the core is reset. Data memories remain in retention state.
- If both the Retention and Shutdown indications of the same block are cleared, the block will be shut down (Shutdown mode has priority).
- It is recommended to disable interrupts before going into Deep Sleep mode. If an interrupt is received while going into Deep Sleep mode, the interrupt will be partially executed. However, the core will be shut off eventually.
- In addition, the EMULATION domain is turned OFF when core is OFF, regardless of the DBC MMIO register bit.

3.3 Shutdown Mode

The special considerations for Shutdown mode are the same as those for Deep Sleep mode, as described in Section 3.2.1.

3.3.1 Enter/Exit Shutdown Mode Sequence

The following is the sequence for entering Shutdown mode:

1. PSVM Shutdown indications are cleared by the *PCU.psu{shutdown} #0x0* instruction.
2. The isolation register de-asserts one cycle after the PSVM[10] bit is cleared.
3. After <STSD value> cycles (CPM address 0x0E60), the *cevaxm4_psu_pshtdwn_r* is zeroed, which means that there is no power to any of the domains.
4. The user disables the root clock.

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The following is the sequence for exiting Shutdown mode:

1. The user enables the root clock.
2. The user gives *stop_sd* at least a two-cycle pulse.
3. *psu_domain_shut_down_switch_r[0]* restarts power to the core and the PSU starts to give resets to the core/MSS and Emulation unit.
4. After <SPSD value> cycles (CPM Address 0x0E64), the power is ON and the *cevaxm4_psu_pshtdwn_r[0]* bus is asserted.
5. The memories are back to ON by writing to the PSVM relevant memory bits (for more details, see Section 3.1).

Example 3-2 shows entering/exiting Shutdown mode.

Example 3-2: Entering/Exiting Shutdown Mode

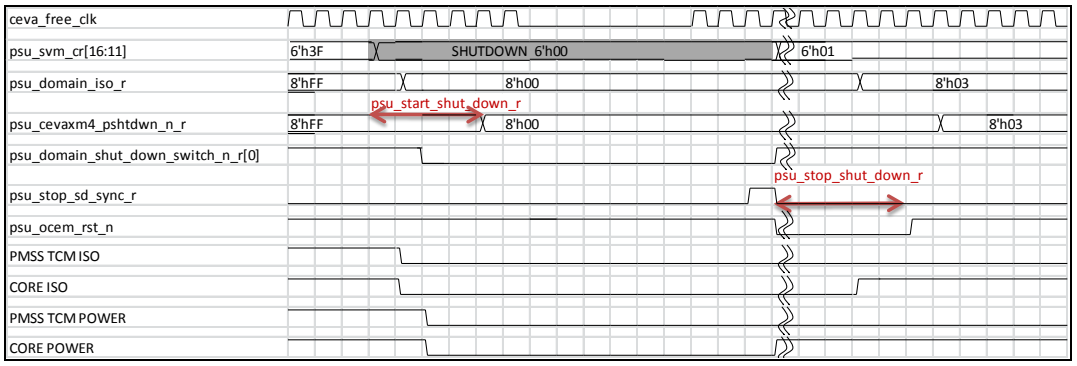

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Figure 3-1 shows the connectivity between the different power domains.

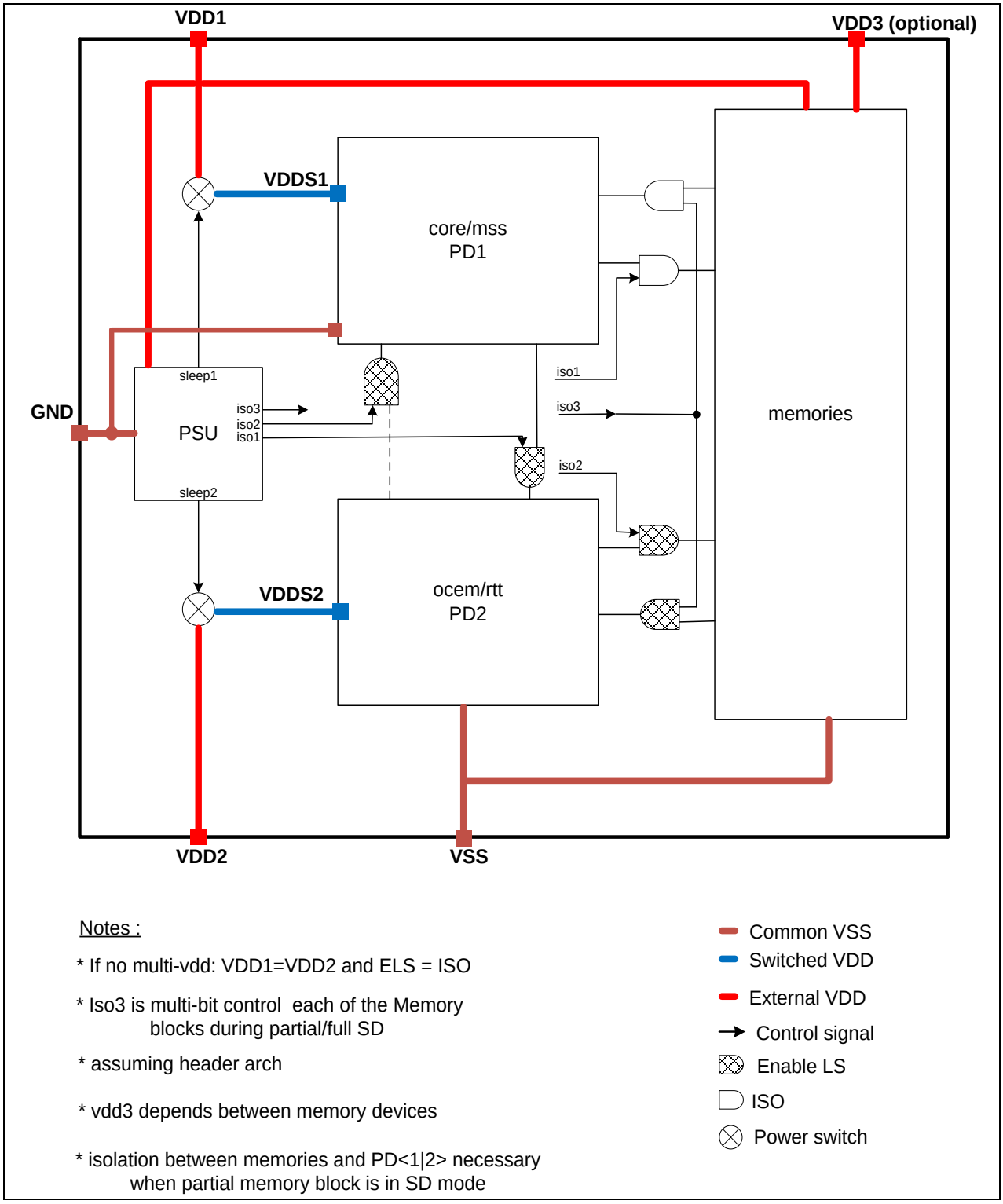

Figure 3-1: CEVA-XM4 Power Domains

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In Figure 3-1:

- PD1: The first power domain, includes the core and MSS
- PD2: The second power domain, includes OCEM and RTT
- The PSU stays ON all of the time.
- The memory domain is controlled by PSU indications.

Note: *Backend implementation is not provided by CEVA and depends on the memory vendor supplier.*

3.4 Emulation Unit Power Modes

As described in Section 2.4, two power modes are supported: Operational Production and Debug. In Debug mode, the Emulation unit (that is, the OCEM and RTT) is fully functional; in Operational Production mode, it is off and no power or clock is provided to the OCEM and RTT.

Note: *If RTT is active and the DBC bit is cleared, then all traces that are stored in the RTT are lost.*

3.4.1 Special Considerations

- The default value of the DBC bit is 1'b1. This means that the core wakes with the OCEM/RTT domain ON. Any application that does not need the debugger must zero the DBC bit to save power.
- If the EMULATION domain is OFF, neither interrupts nor any kind of JTAG access will wake the OCEM in any way.
- After shutdown, the core/MSS power state is resumed as it was before the shutdown. If the EMULATION domain was ON before, it is reset as the core.
- During debug action, writing to the PSU mode register and changing the mode is restricted.

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3.4.2 Enter/Exit Debug Mode Sequence

The following is the sequence for entering Debug mode:

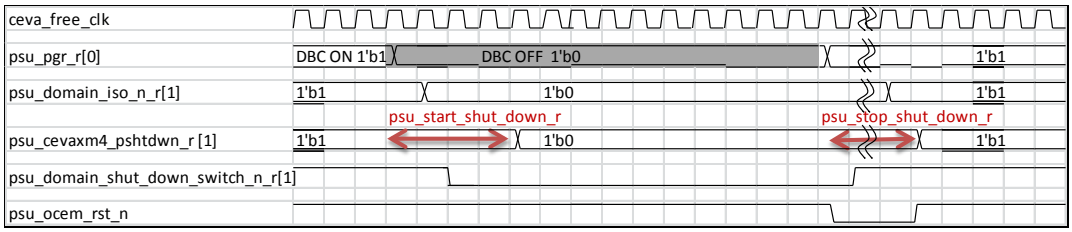
1. Configure the STSD MMIO register.
2. Write to the DBC 1'b1 (Debug mode) bit using an *out* instruction.
3. The PSU resets the OCEM using *psu_ocem_rst_n*.
4. After <SPSD MMIO value> cycles, the PSU asserts the *cevaxm4_psu_pshtdwn_r[1]* output indication for the OCEM/RTT ON domain.
5. The user can start working with the Emulation unit.

The following is the sequence for exiting Debug mode:

1. Configure the STSD MMIO register.
2. Write to the DBC 1'b0 (production mode) bit using an *out* instruction.
3. The PSU de-asserts the *cevaxm4_psu_pshtdwn_r[1]* signal.
4. If the core enters Shutdown/Deep Sleep, the OCEM turns off regardless of the DBC field (for more details, see Section 3.3).
5. After shutdown, the core/MSS power is resumed (but **not** necessarily OCEM/RTT).
6. Debug mode remains as it was before shutdown.

Example 3-3 shows entering/exiting OCEM/RTT Shutdown mode.

Example 3-3: Entering/Exiting OCEM/RTT Shutdown Mode



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3.5 CPF/UPF Definitions

This CEVA-XM4 release includes a generic CPF file and a generic UPF file. For more details about power simulation, see the *CEVA-XM4 Simulation Reference Guide*.

The following must be taken into consideration when working with CPF/UPF:

- The following power domains are defined:
  - PD1: Core/MSS
  - PD2: Emulation
  - Always on domain (top)
- If Retention/OFF states are used on the data/program memories, then real memory switches must be used (for more details, see the *CEVA-XM4 Simulation Reference Guide).*
- To determine the isolation values under Power OFF mode, the following lists are defined in the CPF for each domain:
  - **isolation_pd1_high_list**: All outputs from PD1 whose values are 1'b1 under Power OFF
  - **isolation_pd1_low_list**: All outputs from PD1 whose values are 1'b0 under Power OFF
  - **isolation_pd2_high_list**: All outputs from PD1 whose values are 1'b1 under Power OFF
  - **isolation_pd2_low_list**: All outputs from PD2 whose values are 1'b0 under Power OFF
- Each domain has its own switch, as follows:
  - For PD1: *cevaXM4_sim_top.cevaxm4.cevaxm4_psu.psu_domain_shut_down_switch_n_r[0]*
  - For PD2: *cevaXM4_sim_top.cevaxm4.cevaxm4_psu.psu_domain_shut_down_switch_n_r[1]*
- *psu_domain_shut_down_switch_r* is the bus to the domains and memories to start shutting down the power, as shown in Example 3-3.

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4. Backend Considerations

Entering and exiting the Deep Sleep/Shutdown modes might be a slow, time-consuming process.

4.1 Restrictions and Limitations

- Shutdown/Retention/Isolation signals are considered to be multi-cycles by synthesis constraints. For that reason, toggling these signals in intervals smaller than two (that is, write to “core shutdown”, SVM MMIO field, and change in the *stop_sd* signal) is restricted.
- Turning Power OFF/Retention is done gradually in the logic and memory domains). Writing to the PSU programming model only starts the Shutdown and Deep-Sleep sequences. Due to physical implementation issues, serial switches are inserted, and each part of the relevant domain power is turned OFF serially.
- Because there is a strong link between the physical implementation of the power switches and the functional behavior, the STRET/SPRET/STSD/SPSD MMIO registers **must** be configured based on real values extrapolated from the STA result. These registers define the period of time that it takes to get in/out of the Retention/OFF states.
- *cevaxm4_psu_pshtdwn_r* and *cevaxm4_psu_sys_pshtdwn_r* are the output indications from the CEVA-XM4.

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5. Simulation Considerations

PSU tests are part of the assembly test suite provided in the CEVA-XM4 release. Table 5-1 summarizes the parameters that need to be defined in simulation based on backend parameters.

Table 5-1: Label Values

Label	Value
#START_SHUT_DOWN	Period (in cycles) to complete entering Shutdown mode. Defined by backend.
#STOP_SHUT_DOWN	Period (in cycles) to complete exiting Shutdown mode. Defined by backend.
#START_RET	Period (in cycles) to complete entering Shutdown mode. Defined by backend.
#STOP_RET	Period (in cycles) to complete exiting Shutdown mode. Defined by backend.
Relative PSU Addresses	
@PSVM	0x50
@PGR	0x54
@STRET	0x58
@SPRET	0x5C
@SPSD	0x60
@STSD	0x64

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6. Software Considerations

The CEVA-XM4 power modes are software configurable. Depending on the application, various routines can be introduced into the application to change the PSU programming model and power modes. The following examples demonstrate these small routines; they can be modified to fit the real application needs.

Example 6-1: DMSS Block #1 Entering Retention Routine

```
Retention:
    SC0.lbf #0xE , iopage          // page number = 0xE
    PCU.eint                       // enable IE bit
    # no transaction to the relevant block
    mov #START_RET, r0.ui;         // start retention period
    out {offset, cpm} r0.ui, (#STRET).ui;   // write to MMIO
start retention
    mov #STOP_RET, r0.ui;          // stop retention period
    out {offset, cpm} r0.ui, (#SPRET).ui;  // write to MMIO stop
retention
    psu{deepsleep} #0x37           // enter the mode to PSVM_LO
```

Example 6-2: Enter Deep Sleep Routine

```
Deep Sleep:
    SC0.mov #0xE , iopage          // page number = 0x2
    PCU.eint                       // enable IE bit
    mov,#START_SHUT_DOWN, r0.ui ;  // start Shutdown period (for
core)
    out{offset,cpm} r0.ui, (#STSD).ui ;
    mov,#STOP_SHUT_DOWN, r0.ui ;   // stop Shutdown period (for
core)
    out{dw,cpm} r0.ui, (#SPSD).ui ;
    mov,#START_RETENTION, r0.ui ;  // start Retention period (for
memories)
    out{dw,cpm} r0.ui, (#STRET).ui ;
    mov,#STOP_RETENTION, r0.ui ;   // stop Retention period (for
memories)
    out{dw,cpm} r0.ui, (#SPRET).ui ;
    psu{deepsleep} 0x0             // enter Deep Sleep mode to
the PSVM_LO 9:4
```

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Example 6-3: Enter Shutdown Routine

```
Shutdown:
    SC0.mov #0xE , iopage          // page number = 0xE
    PCU.eint                       // enable IE bit
    mov #START_SHUT_DOWN, r0.ui ;  // start Shutdown period
    out{offset,cpm} r0.ui, (#STSD).ui ;
    mov #STOP_SHUT_DOWN, r0.ui ;   // stop Shutdown period
    out{offset,cpm} r0.ui, #(SPSD).ui ;
    psu{shutdown} 0x0 ;            // enter Shutdown mode to the
PSVM 16:10
```


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7. Glossary

Table 7-1 defines the acronyms used in this document.

Table 7-1: Acronyms

Term	Definition
CPF	Common Power Format
CPM	Configuration Programming Model
DBC	Debug Block Configuration
DMSS	Data Memory Sub System
DPS	Dynamic Power Save mode
DSP	Digital Signal Processor
MIMO	Multiple input Multiple Output
MMIO	Memory Mapped I/O
MSS	Memory Sub System
OCEM	On-Chip Emulation
PCU	Program Control Unit
PMSS	Program Memory Sub-System
PSU	Power Scaling Unit
RTT	Real-Time Trace
SDT	Software Development Tools
STA	Static Timing Analysis
UPF	Unified Power Format

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