CEVA-XM4™

RTL V1.1.3.F Release Notes

Rev. 1.1.3.F

June 2016

DSP Division

Documentation Control

History Table

Version	Date	Description	Remarks
V1.0.0.A	24 February 2015	Initial release	
V1.0.0.F	12 April 2015	Updated delta from previous release	
V1.1.0.F	12 August 2015	Updated supported tools, documents, delta from previous release and package installation	
V1.1.1.F	18 January 2016	Updated delta + version	
V1.1.2.F	9 March 2016	Updated delta + version	
V1.1.3.F	8 June 2016	Updated delta + version	

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1. Introduction

The CEVA-XM4™ is a reusable Silicon Intellectual Property (SIP), DSP core family with a Memory Subsystem (MSS). The SIP source code is the RTL Verilog code, which is fully synthesizable and technology-process independent. This means that it can be easily implemented in various technologies and reduce time-to-market for development.

This release is compatible with the CEVA-XM4 Architecture Specification V1.1.3.F.

This release contains:

- Verilog RTL source code of the CEVA-XM4
- Reference reports and logs
- Simulation environment
- Full backend (RTL-to-GDSII) flow
- Release documentation

Important: *The ETM/RTT IP module referred to in the documentation is an add-on feature that is separately licensed.*

2. Overview

2.1 CEVA-XM4 Modules

Figure 2-1 shows a block diagram of the CEVA-XM4 DSP.

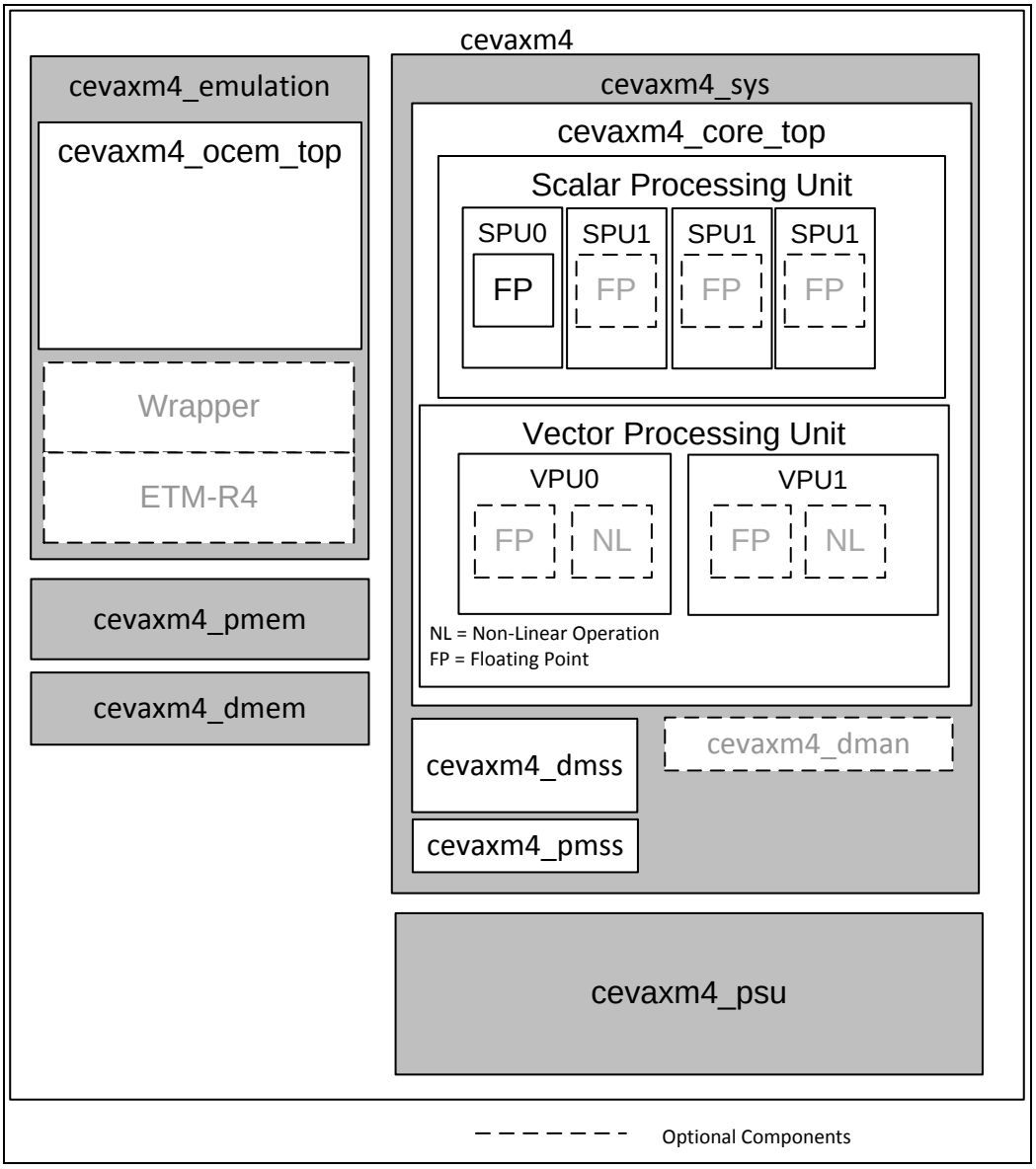

Figure 2-1: CEVA-XM4 Block Diagram

Table 2-1 describes the modules in Figure 2-1.

Table 2-1: CEVA-XM4 Modules

Module Name	Description
cevaxm4	The top-level RTL module. Contains the cevaxm4_sys, the PSU module, the internal memories, and the On-Chip Emulation Module (OCEM).
cevaxm4_pmem	The internal program memory, partitioned into two main blocks: ● block0, which has a configurable size (0KB/32 KB/64 KB/128 KB/256 KB). ● The internal program cache memory, which has a configurable size (32 KB/64 KB/128 KB). When the ECC configuration is installed, each of these blocks has additional redundancy memories. For more details, see the *CEVA-XM4 Integration Reference Guide.*
cevaxm4_dmem	The internal data memory. The size and partition are configurable. The data memory size can be 128 KB/256 KB/512 KB, divided into four blocks. Each memory block is divided into 16 banks. When the ECC configuration is installed, each of these blocks has additional redundancy memories. For more details, see the *CEVA-XM4 Integration Reference Guide*.
cevaxm4_sys	The system top module. Contains the core, DMSS, DMAN, PMSS, and PSU modules
cevaxm4_core_top	The DSP core module
Scalar Processing Unit (SPU)	Handles all scalar computations and bit-manipulation operations that are non-vector DSP operations. The following Scalar Floating Point configurations are supported: ● 1 (floating point unit exists only in SPU0) ● 4 (floating point units exist in SPU0, SPU1, SPU2, and SPU3).
Vector Processing Unit (VPU)	Handles all vector computations. The following Vector Floating Point configurations are supported: ● 0 (no vector floating points) ● 16 (eight floating points per VPU) The following Non-Linear Function Support configurations are supported: ● 0 (no operations per unit) ● 32 (16 operations per VPU)
cevaxm4_emulation	Contains the OCEM, Profiler, and RTT modules
cevaxm4_ocem_top	OCEM top-level module
Profiler	Profiler block (part of the OCEM enhanced configuration)

Module Name	Description
Wrapper	Real-Time Trace (RTT) Wrapper (optional)
ETM-R4	The ETMR4 is licensed separately from ARM. In addition, the ETM-R4 can be configured internally or externally to the CEVA-XM4 top module.
cevaxm4_psu	Power Scaling Unit (PSU)
cevaxm4_pmss	Program MSS
cevaxm4_dmss	Data MSS
cevaxm4_dman	DMA Manager logic

2.2 Internal Program Memory

Table 2-2: Internal Program TCM Hardware Configurations

Program TCM Bank Depth	Size Option				
	0 kB	32 kB	64 kB	128 kB	256 kB
One block	None	1K	2K	4K	8K

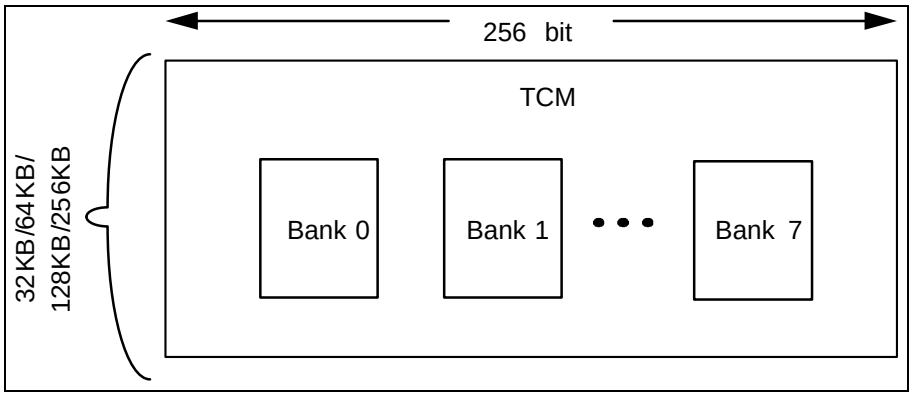

Figure 2-2: Internal TCM Memory Default Configuration

2.2.1 Internal Program Cache Memory

The internal program cache memory consists of Set memory and TAG memory.

2.2.1.1 Internal Program Cache Set Memory

The program cache Set memory consists of four identical blocks for **Way0**, **Way1**, **Way2**, and **Way3**. Each **WayX** block is divided into eight banks of 32 bits. Table 2-3 describes the configurations.

Table 2-3: Internal Program Cache Set Memory Hardware Configurations

Program Cache Set	Size Option		
	32 kB	64 kB	128 kB
Bank depth	0.25K	0.5K	1k

Figure 2-3 shows the internal program cache Set memory partition in the one-block configuration.

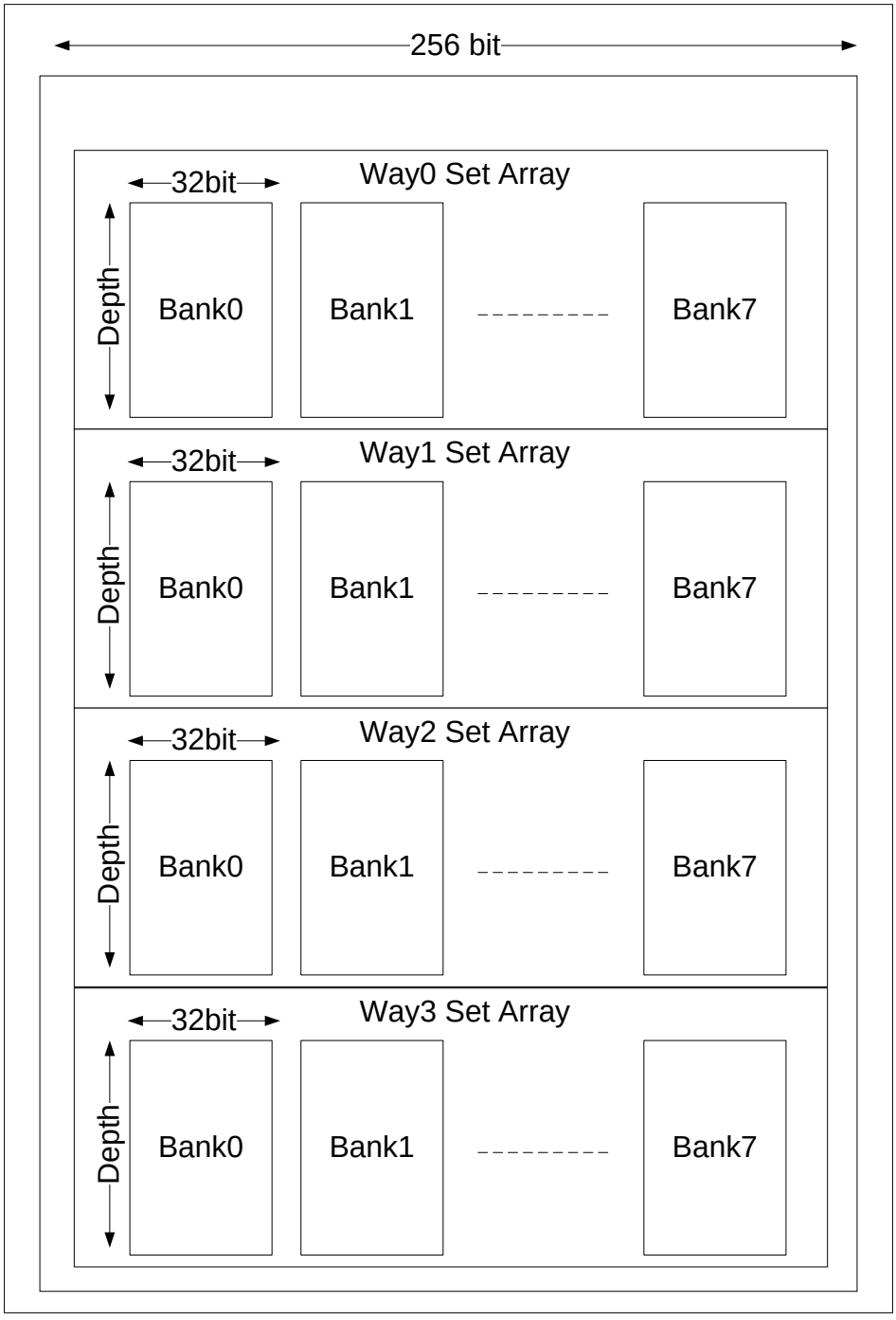

Figure 2-3: Internal Program Cache Set Memory Partition (One-Block Configuration)

2.2.1.2 Internal Program Cache TAG Memory

The program cache TAG memory consists of four identical memory banks for **Way0**, **Way1**, **Way2**, and **Way3**. Table 2-4 describes the configurations.

Table 2-4: Internal Program Cache TAG Memory Hardware Configurations

Program Cache Tag	Size Option		
	32 KB	**64 KB**	**128 KB**
Bank width	21 bits	20 bits	19 bits
Bank depth for 64-byte cache block size	128	256	512

Figure 2-4 shows the internal program cache TAG memory partition.

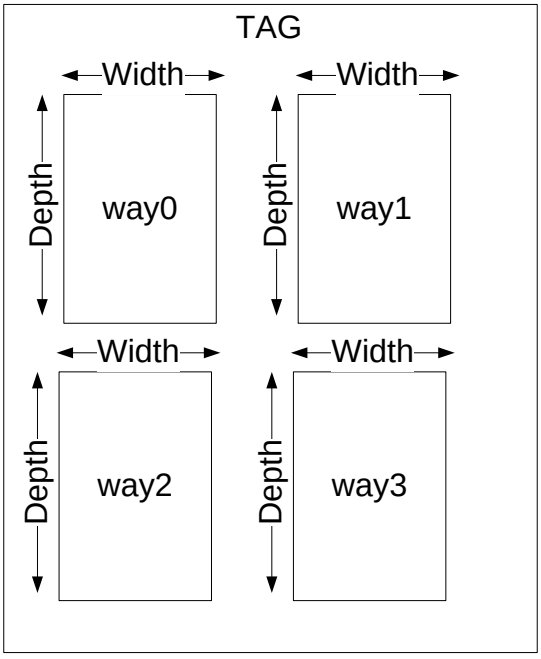

Figure 2-4: Internal Program Cache TAG Memory Partition

The internal program memory is implemented using simulative modules. The IP integrator should replace these memories with its own memories.

Note: *When using the ECC configuration, the internal program memory has additional parity memories for each of the blocks (TCM, cache, and TAG). For more details, see the CEVA-XM4 Integration Reference Guide.*

2.3 Internal Data Memory

Table 2-5: Internal Data TCM Hardware Configurations

Data TCM	Size Option		
	128 KB	256 KB	512 KB
Bank depth for 4 blocks	0.5K	1K	2K

Figure 2-5 shows the internal data memory partition in the four-block configuration.

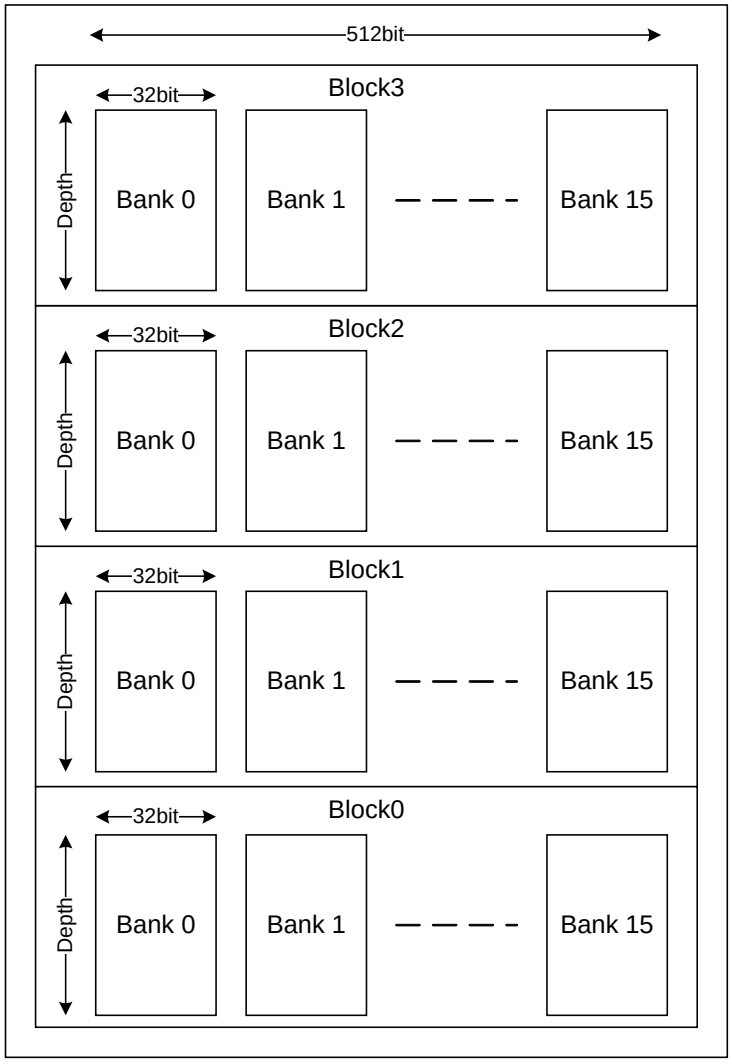

Figure 2-5: Internal Data Memory Partition – Four-Block Configuration (without Memory ECC)

The internal data memory is implemented using simulative modules. The IP integrator should replace these memories with its own memories.

Note: *When using the ECC configuration, the internal data memory has additional parity memories for each of the blocks. For more details, see the CEVA-XM4 Integration Reference Guide.*

3. Database Structure

Figure 3-1 shows a general description of the CEVA-XM4_V1.1.3.F database.

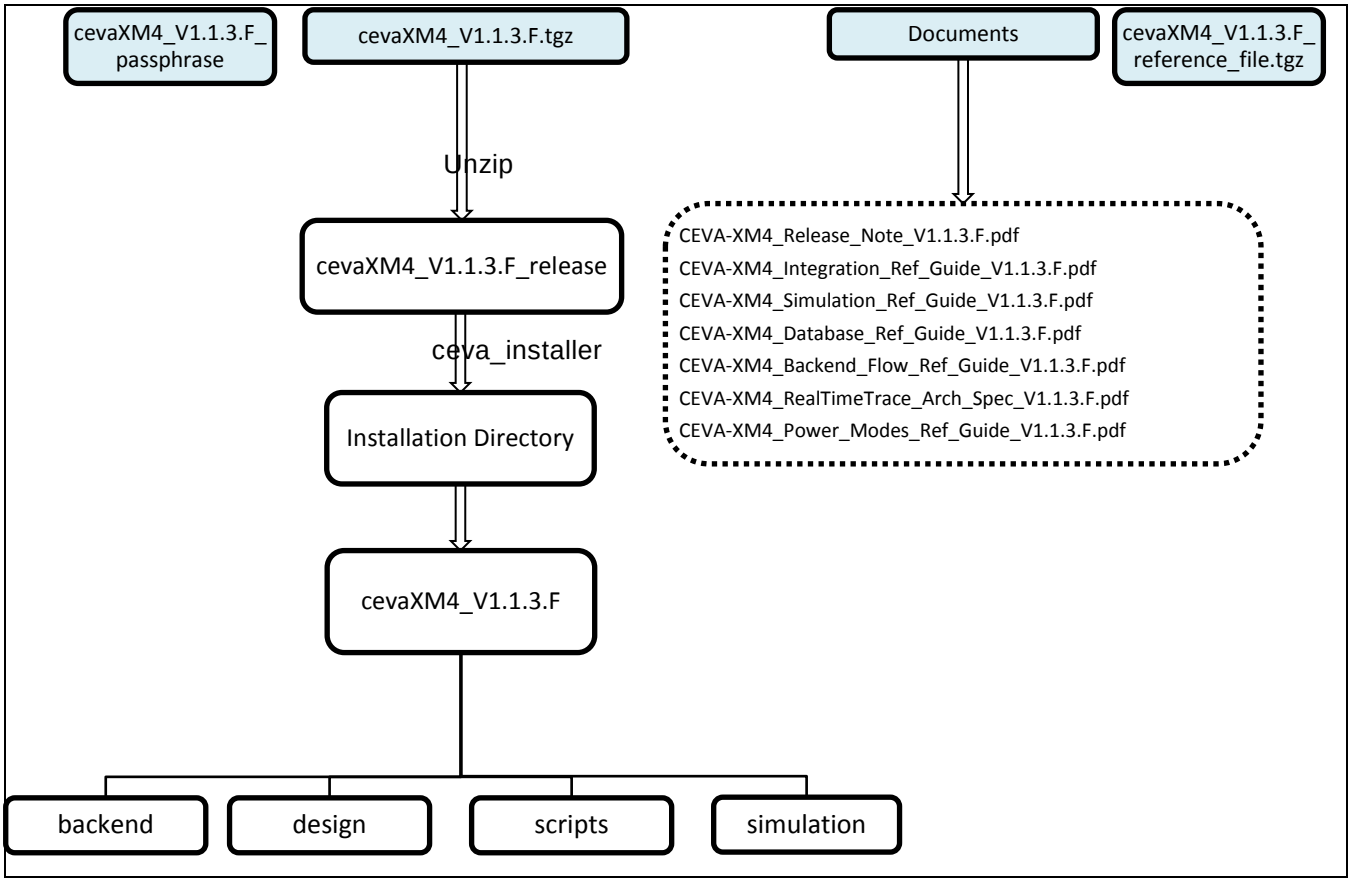

Figure 3-1: CEVA-XM4 V1.1.3.F Database General Structure

Table 3-1: CEVA-XM4 V1.1.3.F Database Description

Directory Name	Description
Documents	Release documentation; delivered separately, outside of the package
cevaXM4_V1.1.3.F	Database root directory
backend	Backend reference flow
design	CEVA-XM4 V1.1.3.F RTL
scripts	Simulation scripts
simulation	Simulation environment and assembly tests

The **cevaXM4_V1.1.3.F_reference_files.tgz** file contains CEVA-XM4 reference reports and EDA tool-related files. It is delivered separately.

For more details, see the *CEVA-XM4 Database Reference Guide*.

4. Supported Tools

Table 4-1 describes the tools that are supported in the simulation and synthesis environments.

Table 4-1: Supported Tools

Tool	Version	Vendor	Description
IES	15.20.002	Cadence	RTL Simulation
VCS	2014.03-2	Synopsys	RTL Simulation
ModelSim	10.2c	Mentor	RTL Simulation
Design Compiler	2015.06	Synopsys	Synthesis
Formality	2015.06	Synopsys	Equivalence checking
IC Compiler	2015.06	Synopsys	Floorplan, Place, CTS, Route
StarRCXT	2015.06	Synopsys	Parasitic Extraction
PrimeTime	2015.06	Synopsys	Static Timing Analysis
TetraMax	2015.06	Synopsys	Test – ATPG+DRC

5. Documentation

The CEVA-XM4 V1.1.3.F documentation is delivered separately from the released package, and contains the following:

- *CEVA-XM4 Backend Flow Reference Guide*
- *CEVA-XM4 Database Reference Guide*
- *CEVA-XM4 Integration Reference Guide*
- *CEVA-XM4 Power Modes Reference Guide*
- *CEVA-XM4 Simulation Reference Guide*
- *CEVA-XM4 Real-Time Trace Specification*

6. Validation for Signoff

To guarantee correct functionality, the IP integrator must ensure that the following signoff stages pass when implementing the CEVA-XM4:

- The entire test suite passes the RTL-level simulation.
- Equivalence checking of the RTL against pre/post-layout netlists succeeded.
- Static Timing Analysis (STA) is clean, with no violation in any corners.
- The entire test suite passes the Gate-level simulation with timing (Dynamic Timing Analysis /SDF).
- The LVS DRC is clean.

For more details about the simulation and verification environment of the CEVA-XM4, see *CEVA-XM4 Simulation Reference Guide.*

7. Delta from Previous Release

7.1 Delta between RTL V1.1.2.F and RTL V1.1.3.F

7.1.1 RTL Changes

- Updated RTL version number. The following file was updated:

  cevaxm4_gendef.v
- Fix for bug #004, as described in Section 7.1.5. The following file was updated:

  cevaxm4_vst.v
- Fix for bug #005, as described in Section 7.1.5. The following file was updated:

  cevaxm4_ddma_q.v
- Fix for bug #006, as described in Section 7.1.5. The following file was updated:

  cevaxm4_qman_task_proc_fsm.v
- Support for architecture enhancement for DMAN shared queue described in Section 7.1.6:
  - **cevaxm4_dman_cpm.v**
  - **cevaxm4_qman.v**
  - **cevaxm4_qman_queue_db.v**
  - **cevaxm4_dman.v**
  - **cevaxm4_dman_cpm_qman.v**
  - **cevaxm4_qman_task_fetch_fsm.v**
- Removal of ***EXT_MEM_WR*** input pin and modification of the related bit in the **OCM_STATUS** register to Reserved:
  - **cevaxm4.v**
  - **cevaxm4_emulation.v**
  - **cevaxm4_ocem_top.v**
  - **cevaxm4_ocem_control.v**

- DFT Improvement; inserted *tst_gatedclock* to a FF in the DACU module:
  - **cevaxm4_dacu.v**
  - **cevaxm4_ddma_q.v**
  - **cevaxm4_dmss.v**
  - **cevaxm4_dman.v**

7.1.2 Simulation Environment Changes

The following simulation files were modified:

- Lists:
  - **cevaxm4_release_without_simulative_switches**
    - **cevaxm4_dman_en_cnt_no_rptr_dec.asm** was added.
    - **cevaxm4_dmss_dma_dman_upload_fixed.asm** was added.
- Includes:
  - **cevaxm4_param.asm**: Updated core version
- Test modifications:
  - **cevaxm4_ocem_apb_gp_out.asm**: Removed ext_pmem_wr use
  - **cevaxm4_ocem_mss_rst_boot.asm**: Fixed typo
  - **cevaxm4_ocem_jtag_single_step.asm**: Removed redundant lines
  - **cevaxm4_dmss_dma_dman_iit_2d_dup2b.asm**: Fixed test
  - **cevaxm4_dmss_dma_q_ext.asm**: Added LSID read check
  - **cevaxm4_boot_lightsleep_edap.asm**: Fixed test
  - **cevaxm4_boot_lightsleep_pdma.asm**: Fixed test
- New tests:
  - **cevaxm4_dmss_dma_dman_upload_fixed.asm**
  - **cevaxm4_dman_en_cnt_no_rptr_dec.asm**
- Simulation top files; the following files were modified to remove the *ext_pmem_wr* input port:
  - **cevaxm4_sim_top.v**
  - **cevaxm4_sim_cntrl.v**

7.1.3 Backend Flow Changes

The following files were modified:

- **fm.tcl**: Added a mechanism to verify the netlist vs. the RTL of **ceva_clock_gater.v** and **gnf_ff.v**
- **constrains.tcl**: Fixed typos and error reporting
- **dc.tcl**: Fixed typos and made some slight flow changes
- **tm.tcl**: Fixed a typo in the coverage goal and pattern generation setup

7.1.4 Documentation Modifications

- The following changes were made to the *CEVA-XM4 Integration Reference Guide*:
  - Updated version
  - Modified ***Table 2-1: CEVA-XM4 Interface***:
    - Removed *ext_pmem_wr* input port
  - Removed Section 22.8, External Program Memory Indication
  - Added Section 21, Access Protection Violation
- The following changes were made to the *CEVA-XM4 Simulation Reference Guide*:
  - Updated version
  - In Section 6.2.1, Tests That Cannot Run with Simulative Switches:
    - **cevaxm4_dmss_dma_dman_upload_fixed.asm** was added.
    - **cevaxm4_dman_en_cnt_no_rptr_dec.asm** was added.
- The following changes were made to the *CEVA-XM4 Backend Flow Reference Guide*:
  - Updated version
  - Modified Section 11.3, Reset

7.1.5 Bug Fixes

The following bugs were fixed:

- Bug #004: Core vector-store saturation
- Bug #005: LSID field in DDRS register
- Bug #006: QMAN download task with burst type FIXED increment DDEA

For more details, see the *CEVA-XM4 Bug List.*

7.1.6 Architecture Changes

The following architecture changes were made in the QMAN to improve the QMAN's operation in shared queue mode:

- New fields (bits) were added in the QMAN programming model for each task counter.
- These bits enable control over the mode in which the enabled task counters in each QMAN are decremented.
- The old mode in which the counter is decremented by the amount of tasks that were "pulled" by another core's QMAN is still supported.
- A new mode in which the counter is decremented by one without relation to the number of tasks that were pulled by another core's QMAN2 is supported.

8. Package Installation

The following sections describe the installation of the CEVA-XM4 environment on the user's system.

The CEVA-XM4 release contains the zipped **cevaXM4_V1.1.3.F.tgz** file and requires the **cevaXM4_V1.1.3.F_passphrase** license file, which is obtainable from CEVA support (ceva-support@ceva-dsp.com).

8.1 Unpacking the Release

In the directory containing the zipped file, unpack the release by typing:

```
tar -zxvf cevaXM4_V1.1.3.F.tgz
```

8.2 Installing in Batch Mode

Do the following:

1. Change directories to the extracted directory by typing:

```
cd cevaXM4_V1.1.3.F_release
```

2. Run the installer in batch mode by typing::

```
./ceva_installer -passphrase_file
../cevaXM4_V1.1.3.F_passphrase -dw_root_dir <dw_path>
```

3. On the command line, type the relevant switches that define the design configuration, as described in Table 8-1.

   For example:

```
./ceva_installer -passphrase_file ../ cevaXM4_V1.1.3.F
_passphrase -dw_root_dir <dw_path> –dtcm_size 128kb    -
memory_ecc 32bit
```

Table 8-1: Design Configuration Switches

Switch Name	Description	Options	Default Value	Restrictions
passphrase_file	Sets the path to the passphrase file	-	-	Mandatory
dw_root_dir	Sets the path to the DesignWare root directory	-	-	Mandatory
amba_ecc	Sets the Bus ECC width configuration	0, 32bit	0	32-bit configuration is restricted when memory_ecc is 0.
memory_ecc	Sets the ECC width configuration	0, 32bit	0	-

Switch Name	Description	Options	Default Value	Restrictions
axi_masters_num	Sets the number of AXI Masters (including EDP)	1, 3	1	-
axi_slaves_num	Sets the number of AXI slaves	0, 1, 3	0	-
axim_width	Sets the AXI Master width configuration	128 bit, 256 bit	256 bit	-
axis_width	Sets the AXI slave width configuration	128 bit, 256 bit	-	Mandatory when running with slaves
nff	Sets the Non-Functional Flip-Flop (NFF) configuration	-	Off	Add the switch to invoke
cevamm3101_compt		-	Off	Add the switch to invoke
design_name	Sets a valid name for the design. ***Note**: The name must not contain any special characters or start with a number.*	-	Conf1	-
dtcm_size	Sets the DMSS configuration	128 kb, 256 kb, 512 kb	256 kb	-
Help | h	Prints the help menu	-	-	-
install_dir	Sets the path to the installation directory	-	Current directory	-
mem_power_gating	Uses memory with power gating	-	Off	Add the switch to invoke
nonlinear_units	Non Linear functions support	0, 32	32	-
pcache_size	I-Cache configuration	32 kb, 64 kb, 128 kb	32 kb	-
ptcm_size	Configures the I-TCM size	0, 32 kb, 64 kb, 128 kb, 256 kb	32 kb	-
qman_num	QMAN configuration	0, 8	0	-
sflp	Includes three additional floating point units in the SPU (which allows four operations in the SPU)	1, 4	1	-
spu_xtend	Installs with SPU XTEND	-	Off	Add the switch to invoke

Switch Name	Description	Options	Default Value	Restrictions
vflp	Includes additional floating point units in the VPU (which allows 16 operations in the VPU)	0, 16	16	-
vpu_xtend	Installs with VPU XTEND	-	Off	Add the switch to invoke
real_time_trace	Includes RTT in the design	no_rtt, internal, external	no_rtt	If RTT is used, the user must add a path to the RTT passphrase file, ETM-R4, and CoreSight root directories.
etm_install_dir	Sets the path to the ETM-R4 root directory	-	-	Mandatory when running with real_time_trace
tpiu_lite_install_dir	Sets the path to the CoreSight root directory	-	-	Mandatory when running with real_time_trace

The installation process was verified in the following operating systems:

- Fedora
- CentOS
- Red Hat 5
- Red Hat 6

Your system must support the following libraries:

- Fedora:
  - **glibc.i686**
  - **libXft**
  - **libsgutilnogui.so**
- CentOS:
  - **zlib.i686**
  - **libXft**
  - **libstdc++.so.6**
  - **libXext.so.6**