CEVA-XM4™

RTL V1.1.1.F Database Reference Guide

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DSP Division

Documentation Control

History Table

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V1.1.0.F	12/6/2015	Added reference chapter and made updates for V1.1.0.F	
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1. Introduction

1.1 Scope

This document describes the structure and contents of the CEVA-XM4™ DSP Core delivery database.

CEVA-XM4 is a complex IP that contains thousands of files and hundreds of directories. The main purpose of this document is to provide easy access for CEVA IP database users and to become familiar with this database.

Important: *The ETM/RTT module referred to in this document is an add-on feature with separate licensing.*

Note: *The Wrapper is SIP, but the ETMR4 is licensed separately from ARM. In addition, the ETMR4 can be configured as either internal or external to the CEVA-XM4™ top module.*

1.2 Audience

This document is intended for ASIC designers who are implementing and embedding the CEVA-XM4 into their design.

1.3 Related Documents

The following documents are related to the information in this document:

1. *CEVA-XM4 Backend Reference Flow Guide*
2. *CEVA-XM4 Simulation Reference Guide*
3. *CEVA-XM4 Integration Reference Guide*
4. *CEVA-XM4 Power Modes Reference Guide*
5. *CEVA-XM4 Real-Time Trace Architecture Specification*
6. *CEVA-XM4 Release Notes*

Note: *All of these documents are delivered separately, and are not contained in the release package.*

2. Database Structure

Figure 2-1 shows the main directory structure of the CEVA-XM4 database.

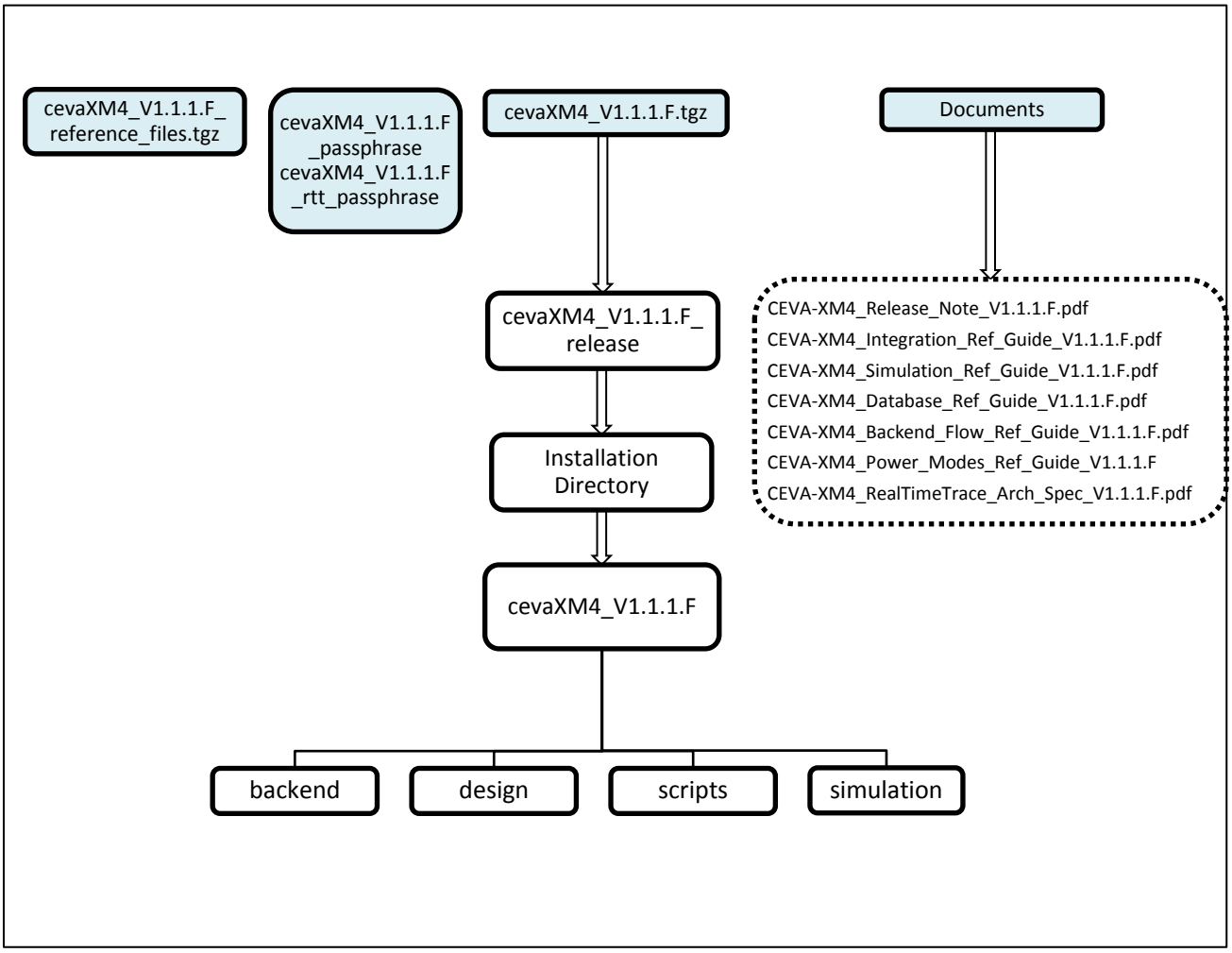

Figure 2-1: CEVA-XM4 Database Structure

Table 2-1 describes the database structure.

Table 2-1: CEVA-XM4 Database Structure

Name	Description
CEVA-XM4_V1.1.1.F	The database root directory. Contains the following subdirectories: • **backend**: CEVA-XM4 backend directory • **design**: CEVA-XM4 RTL • **scripts**: Verification- and simulation-related scripts • **simulation**: CEVA-XM4 RTL simulation environment
Documents	Contains the release documentation
cevaXM4_V1.1.1.F_ reference_files.tgz	Contains the CEVA-XM4 reference reports and EDA tool-related files
• **cevaXM4_V1.1.1.F_ passphrase** • **cevaXM4_V1.1.1.F_ rtt_passphrase**	Passphrase files for the CEVA-XM4 and Real-Time-Trace

A full description of the database is presented in the following sections.

3. Backend Environment Structure

The backend directories contain the CEVA-XM4 full RTL-to-GDSII environment. For a description of this backend environment (that is, the scripts, reports, and other files), see the *CEVA-XM4 Backend Reference Flow* document.

Figure 3-1 shows the backend directory structure.

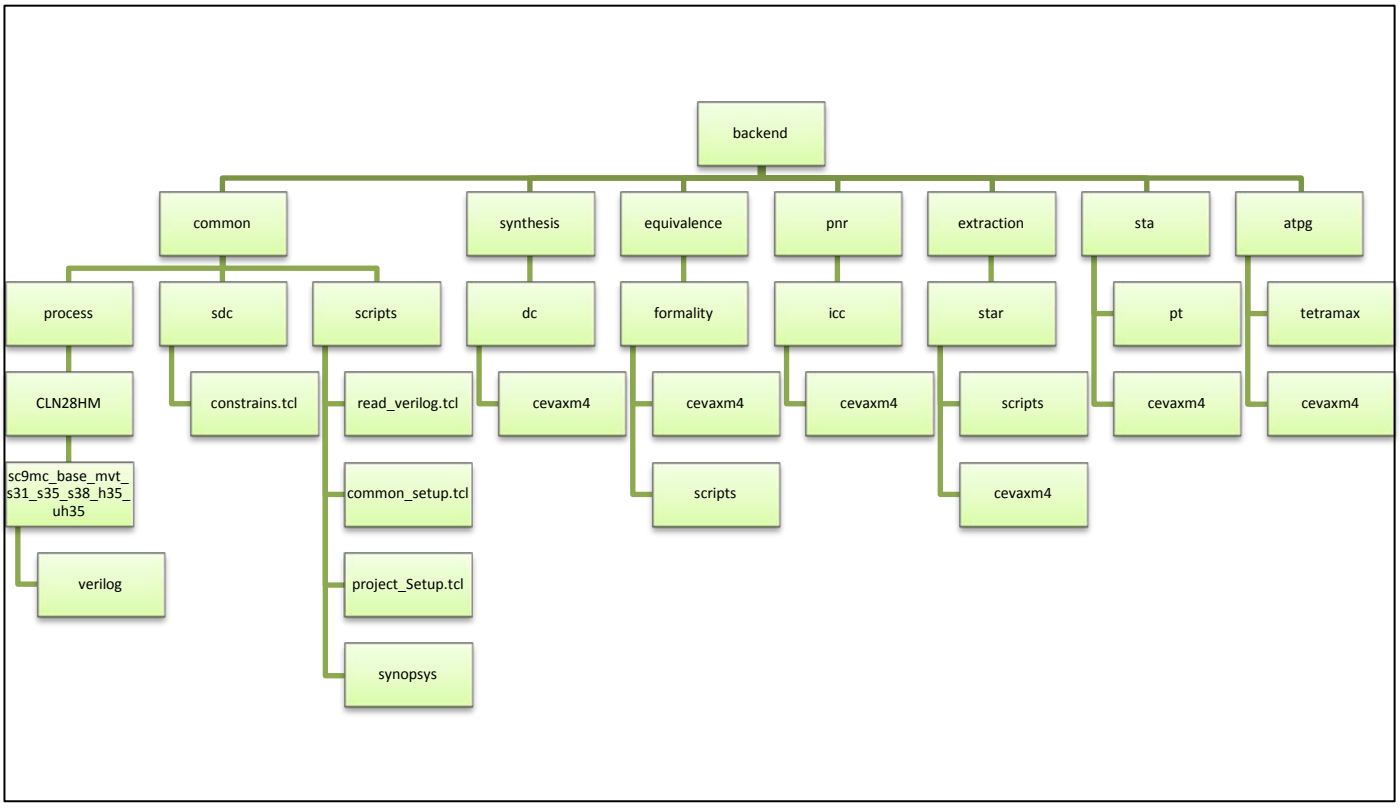

Figure 3-1: backend/ Directory Structure

Table 3-1 describes the top-level **backend/** directories.

Table 3-1: CEVA-XM4 Top-Level backend/ Directories

Directory Name	Description
common	Root directory for common scripts and common data, for example, SDC constraints and Verilog files. Contains the following subdirectories: • **process**: Process-dependent scripts and Verilog files • **sdc**: Constraints scripts • **scripts**: Common scripts that should be sourced by all tools
synthesis	Root directory for synthesis runs. See Table 3-2 for the subdirectories.
equivalence	Root directory for equivalence check runs. See Table 3-2 for the subdirectories.
pnr	Root directory for place/CTS/route runs. See Table 3-2 for the subdirectories.
extraction	Parasitic extraction. See Table 3-2 for the subdirectories.
sta	Root directory for STA runs. See Table 3-2 for the subdirectories.
atpg	Root directory for ATPG runs. See Table 3-2 for the subdirectories.

Table 3-2: CEVA-XM4 Synopsys Tool Directories

Directory Name	Description
synthesis/dc	Root directory for the CEVA-XM4 design compiler synthesis directories
equivalence/formality	Root directory for the Formality tool for checking functional equivalence
pnr/icc	Root directory for the CEVA-XM4 IC Compiler (place and route)
extraction/star	Root directory for the CEVA-XM4 StarRCXT directories
sta/pt	Root directory for the CEVA-XM4 PrimeTime directories
atpg/tetramax	Root directory for the CEVA-XM4 TetraMax directories

4. Verilog Design Structure

Figure 4-1 shows the CEVA-XM4 Verilog RTL directory structure.

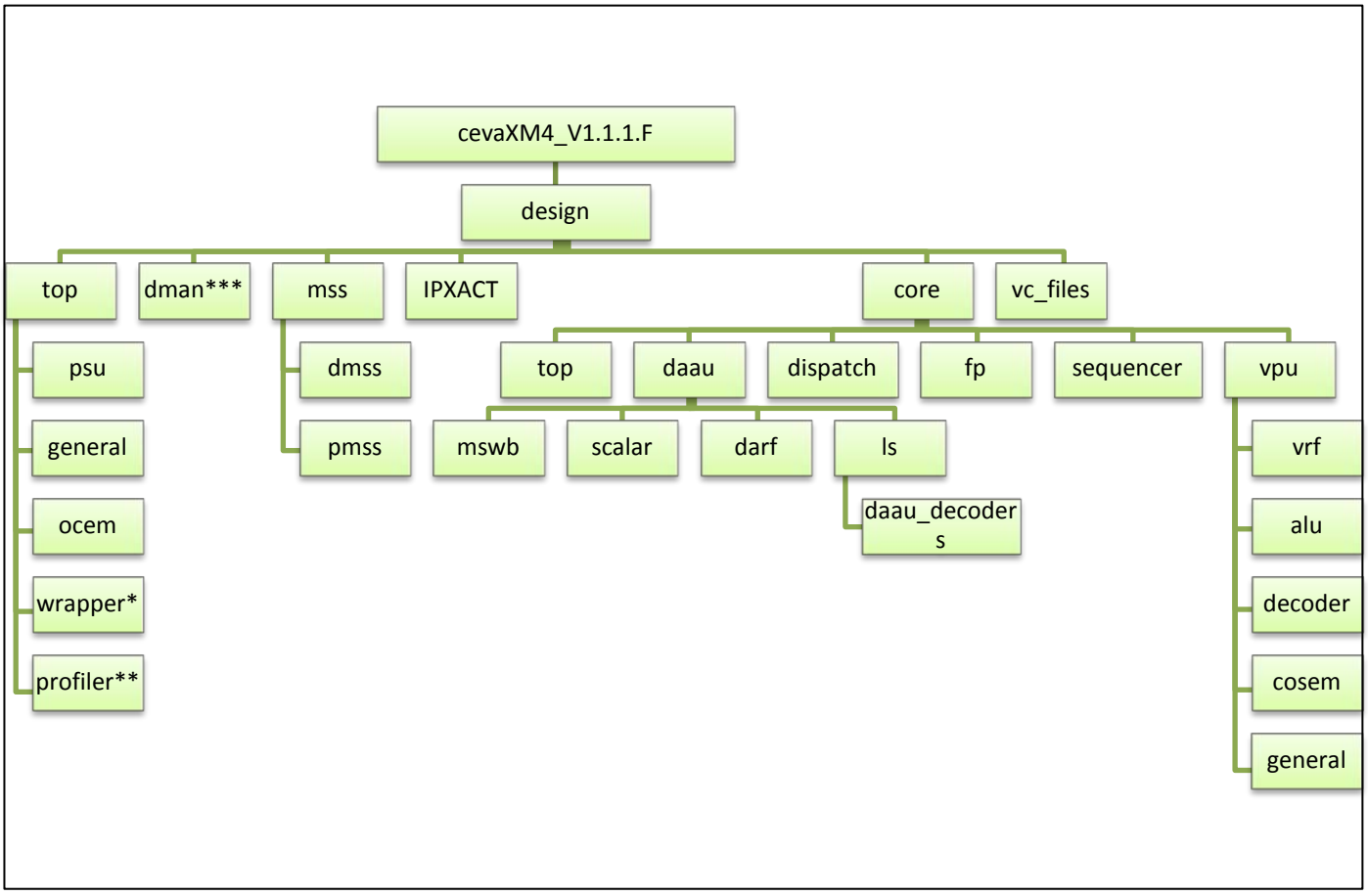

Figure 4-1: CEVA-XM4 design/ Directory Structure

Notes: ** Only if the RTT is installed (an add-on module separately licensed).*

*** Only if the PROFILER (Enhanced OCEM) configuration is installed.*

****Only if the DMA Manager Configuration is installed.*

Table 4-1 describes the CEVA-XM4 Verilog release **design/** directories.

Table 4-1: CEVA-XM4 design/ Directories

Directory Name	Description
design/CEVA-XM4	The source code directory
top	CEVA-XM4 top Verilog source code. Contains the following subdirectories: ● **psu**: The PSU Verilog source code ● **general**: General submodules that are used as building blocks in various modules ● **ocem**: The OCEM Verilog source code ● **wrapper**: The RTT Wrapper Verilog source code ● **profiler**: The PROFILER Verilog source code
dman	Top directory for DMA Manager Verilog source code
mss	Top directory for MSS Verilog source code. Contains the following subdirectories: ● **dmss**: The DMSS Verilog source code ● **pmss**: The PMSS Verilog source code
IPXACT	CEVA-XM4 design data in IPXACT format
core	Top directory for Core Verilog source code. See Table 4-2 for the subdirectories.
vc_files	VC files of all Verilog modules for all configurations

Table 4-2: CEVA-XM4 design/core/ Directories

Directory Name	Description
top	The CEVA-XM4_core top-level module
daau	The Data Address generation Verilog source code. Contains the following subdirectories: ● **mswb**: The Memory Switch Box Verilog source code ● **scalar**: The Scalar Processing Unit Verilog source code ● **darf**: The ARF register Verilog source code ● **ls**: The Load/Store Verilog source code, which has the following subdirectory: ○ **daau_decoders**: The decoder Verilog source code.
dispatch	The dispatcher Verilog source code

Directory Name	Description
fp	The Floating-Point Unit Verilog source code
sequencer	The sequencer Verilog source code
vpu	The VPU Verilog source code. Contains the following subdirectories: • **vrf**: The VRF Verilog source code • **alu**: The Arithmetic Logic Unit Verilog source code • **decoder**: The VPU decoder Verilog source code • **general**: General submodules that are used in the VPU

5. Scripts Directory Structure

Figure 5-1 shows the **<install_dir>/CEVA-XM4_V1.1.1.F/scripts** directory, which contains the Cshell and Perl scripts used for verification and simulation. For more details about the simulation environment (that is, simulation scripts, tests, and other files that are used in the verification environment), see the *CEVA-XM4 Simulation Reference Guide* document.

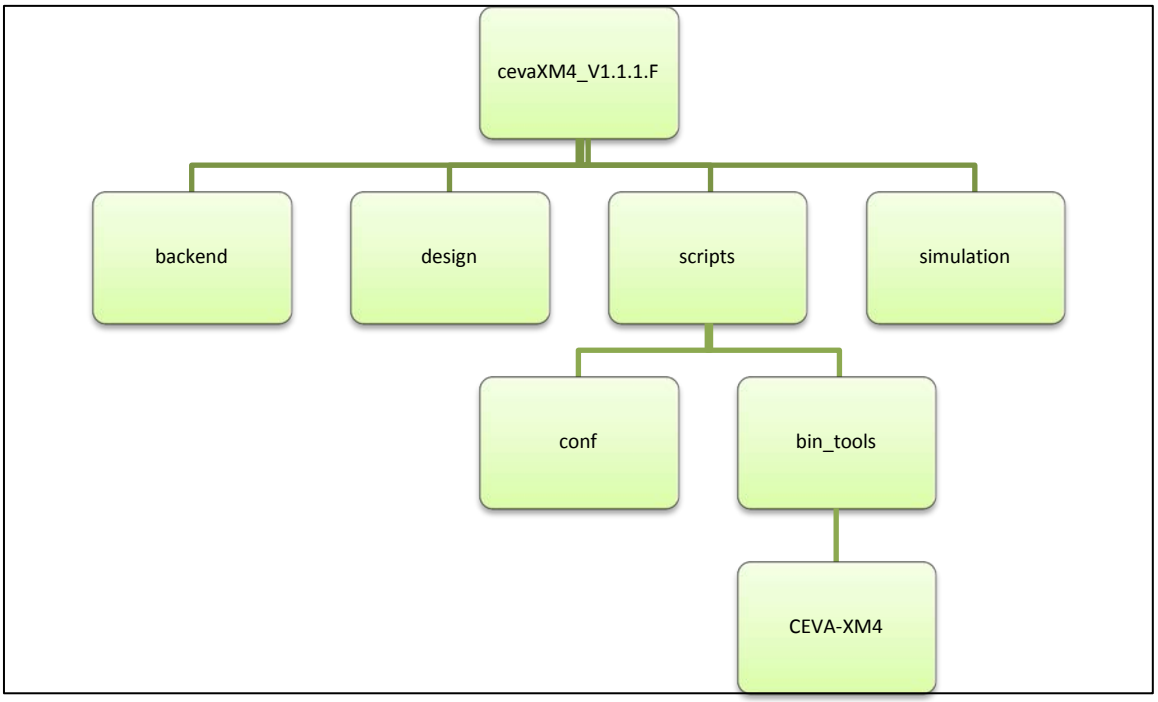

Figure 5-1: CEVA-XM4 scripts/ Directory Structure

Table 5-1 describes the CEVA-XM4 release **scripts/** directories.

Table 5-1: CEVA-XM4 scripts/ Directories

Directory Name	Description
conf	The CEVA-XM4 script configuration
bin_tools	The CEVA-XM4 Software Development Tools (SDT)

6. Simulation Environment Structure

Figure 6-1 shows the CEVA-XM4 simulation directory, which is used for the simulation environment. The simulation environment includes some Verilog modules that are not part of the CEVA-XM4 IP and are used for simulation purposes only.

The release contains a comprehensive verification and simulation environment for the CEVA-XM4 RTL. The environment is based on an assembly self-check test suite, which is executed using the ceva_sim script.

For a description of the CEVA-XM4 verification environment (that is, simulation scripts, tests, and other files that are used in the verification environment), see the *CEVA-XM4 Simulation Reference Guide* document.

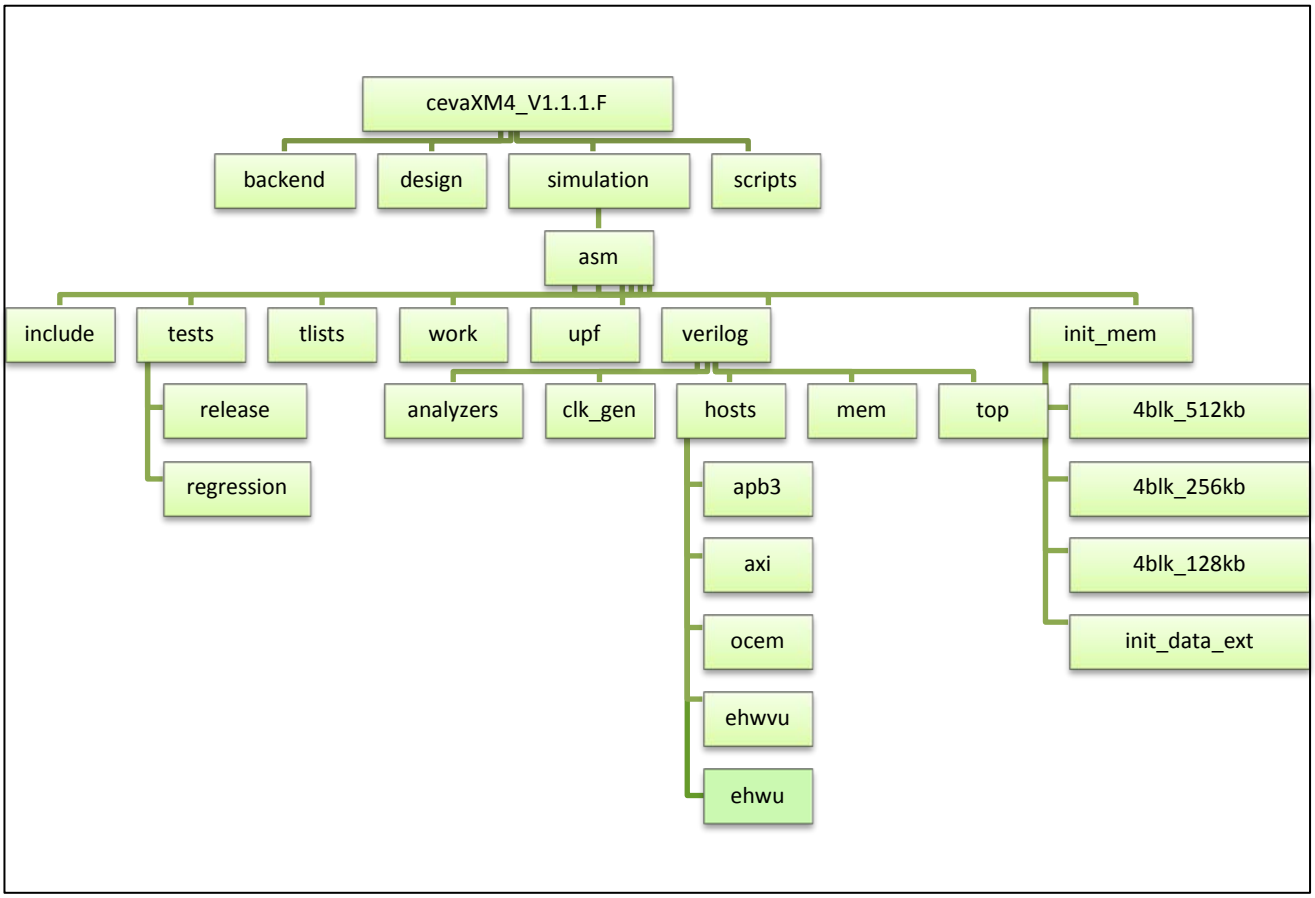

Figure 6-1: CEVA-XM4 simulation/ Directory Structure

Table 6-1 describes the CEVA-XM4 release **simulation/** directories.

Table 6-1: CEVA-XM4 simulation/ Directories

Directory Name	Description
simulation	The simulation-related source code root directory
asm	The ASM-based simulation environment and tests directory
include	The parameters file and assembly macros
tests	The tests directory. Contains the following subdirectories: ● **release**: Assembly tests that are part of the release package ● **regression**: IPXACT tests (installed only if python is supported)
tlists	The test list file(s)
work	The simulation execution directory
cpf	The CPF power file
upf	The UPF power file
verilog	The simulation environment Verilog files directory. See Table 6-2 for the subdirectories.
init_mem	The internal and external data memory initialization files

Table 6-2: CEVA-XM4 simulation/asm/verilog Directories

Directory Name	Description
analyzers	The analyzers (checkers)
clk_gen	The CEVA-XM4 clock generation unit
hosts	The APB, AXI, EHW, and OCEM Host files. Contains the following subdirectories: ● **apb3**: The APB3 Host files ● **axi**: The AXI Host files ● **ocem**: The OCEM Host files ● **ehwvu**: The CEVA-Xtend hardware Host for VPU unit ● **ehwu**: The CEVA-Xtend hardware Host for SCLAR unit
mem	The behavioral memory files
top	All top-level Verilog source code used for simulation

7. Reference Directory Structure

Figure 7-1 shows the CEVA-XM4 **reference/** directory, which is delivered separately from the RTL package. It contains various EDA tool-related setup, log, and report files.

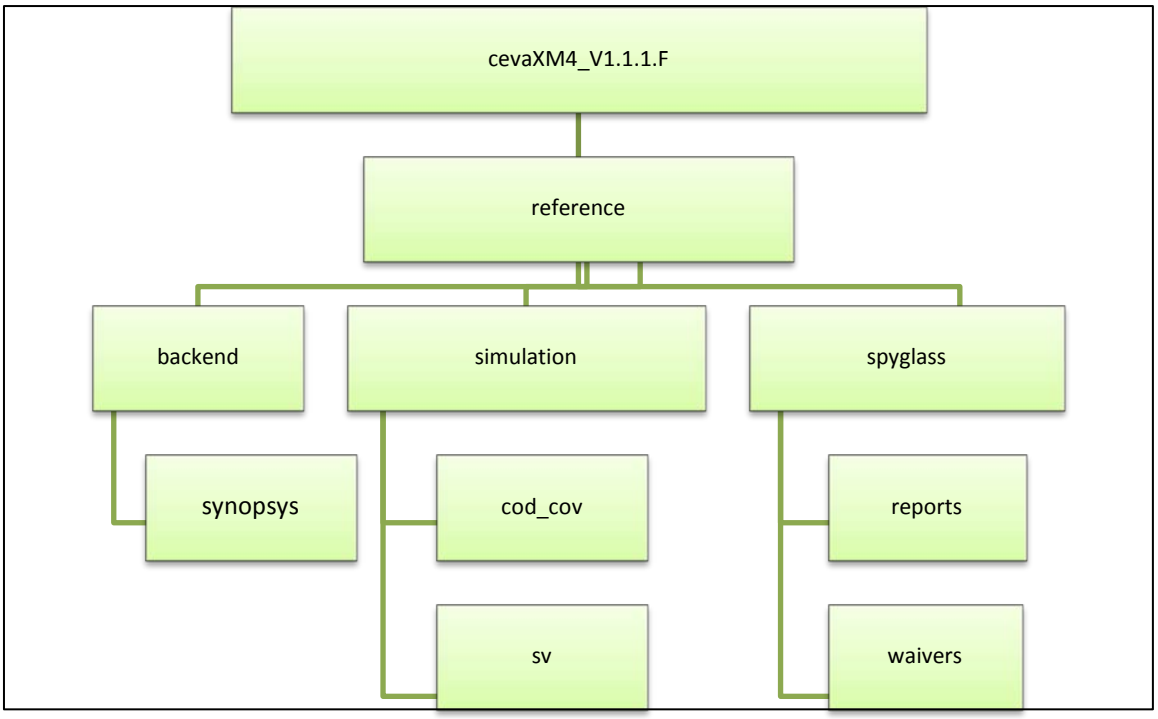

Figure 7-1: CEVA-XM4 reference/ Directory Structure

Table 7-1 describes the CEVA-XM4 release **reference/** directories.

Table 7-1: CEVA-XM4 reference/ Directories

Directory Name	Description
backend	Contains the **synopsys** subdirectory, which has the supporting logs, reports and floorplan files
simulation	The code coverage and waveform viewer files. Contains the following subdirectories: • **cod_cov**: Cadence IMC Code Coverage top-level toggle coverage report and the exclude file • **sv**: Cadence SimVision command script
spyglass	The Atrenta Spyglass files. Contains the following subdirectories: • **reports**: LINT and CDC reports • **waivers**: LINT and CDC waivers

8. Glossary

Table 8-1 defines the acronyms used in this document.

Table 8-1: Acronyms

Term	Definition
ARF	Address Register File
CDC	Clock Domain Cross
CPF	Common Power Format
DMA	Direct Memory Access
DMSS	Data Memory Sub System
DSP	Digital Signal Processor
EDA	Electronic Design Automation
EHW	Extend Hardware
ETM	Embedded Trace Macrocell
MSS	Memory Sub System
OCEM	On-Chip Emulation Module
PMSS	Program Memory Sub-System
PSU	Power Scaling Unit
RTT	Real-Time Trace
SDT	Software Development Tools
SIP	Silicon Intellectual Property
UPF	Unified Power Format
VPU	Vector Processing Unit
VRF	Vector Register File