CEVA-XM4™

Architecture Specification Release Notes

Rev. 1.1.3.F

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DSP Division

Documentation Control

History Table

Version	Date	Description	Remarks
1.1.1.A	19/1/2016	Official release	
1.1.1.F	22/2/2016	Official release, resynching version number	
1.1.2.F	29/3/2016	Official release, resynching version number	
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Table of Contents

1. Introduction

1.1 Scope

This document describes the CEVA-XM4™ DSP Core Architecture Specification 1.1.3.F release.

1.2 Overview

The CEVA-XM4 is high-performance computer-vision and imaging DSP architecture.

1.3 Related Documents

The CEVA-XM4 IP includes the DSP core specified by the core's architecture specification documents (volumes I and II) and the memory subsystem (MSS), as specified by the MSS architecture specification document.

This release includes DSP version 1.1.3.F and MSS version 1.1.3.F as listed below:

1. *CEVA-XM4 Architecture Specification Volume I V1.1.3.F*
2. *CEVA- XM4 Architecture Specification Volume II V1.1.3.F*
3. *CEVA-XM4 MSS Architecture Specification V1.1.3.F*
4. *CEVA-XM4 Xtend Specification V1.1.3.F*
5. *CEVA-XM4 On-Chip Emulation Reference Guide V1.1.3.F*
6. *CEVA-XM4 TCE Integration Guide V1.1.3.F*

2. MSS Differences between CEVA-XM4 V1.1.0.F and V1.1.1.F

The following are the differences in the Memory Subsystem (MSS) between the CEVA-XM4 V1.1.0.F and V1.1.1.F releases. All cross-references are to the *CEVA-XM4 MSS Architecture Specification V1.1.1.F*.

- Table 2-9 was corrected to refer to L1IC.
- Notes were added to Tables 3-30 and 5-81 to clarify the *DMA_SIZE*, *TILE_WIDTH*, and *TILE_HEIGHT* fields.
- The size of the *EXT_STRIDE* field was corrected to 16 bits.
- Section 5.5.4 was clarified to indicate that **QMAN_IDM_CROS** applies to both Direct and 2D transfers.
- The DBC bit (in the **PGR[0]** register) was moved to the **PSVM[2]** register. **PGR[0]** is now reserved.
- The new *VP_LDST_BNK_CF* field was added to Table 5-90 (the **DBG_GEN_2** register).

  The corresponding mask and shadow fields were also added to Table 5-94 (the **DBG_GEN2_MASK** register) and Table 5-112 (the **SHW_DBG_GEN_2** register).

3. Core Differences between CEVA-XM4 V1.1.0.F and V1.1.1.F

The following are the differences in the core between the CEVA-XM4 V1.1.0.F and V1.1.1.F releases. All cross-references are to the *CEVA-XM4 Architecture Specification Vol. II V1.1.1.F*.

3.1.1 MM3K Compatibility

Full support for MM3K compatibility was added.

For more details, see the relevant instruction in the *CEVA-XM4 Architecture Specification Vol. II V1.1.1.F*.

3.1.2 Floating Point Instructions Bug Fix

- **fpextract**: Left shift when extracting mantissa and truncated the LSB
- **fpsub/vfpsub**: Fixed the sub of two identical numbers
- **fpmpy, fpadd, fpsub, vfpadd, vfpsub**: Removed OV indication in case of INF
- **vfpsqrt and vfpsqrti**: Fixed negative detection
- **vfpinv**: Checked if result is INF
- **vfpextract**: Fixed the case of odd to left shift by one

For more details, see the relevant instruction in the *CEVA-XM4 Architecture Specification Vol. II V1.1.1.F*.

3.1.3 New Instructions

To improve the performance of the CEVA-XM4 V1.1.1, the following new instructions were added:

- **rmodw**: Reads/modifies/writes atomic instructions
- **vpst** and **vbcpst**: Add unsigned saturation
- **movselect**: Adds an immediate data type to this instruction, and a debug option switch for the PSU
- **divstep**: Adds a new division instruction to the scalar
- **brar** and **callar**: Add static taken prediction

For more details, see the relevant instructions in the *CEVA-XM4 Architecture Specification Vol. II V1.1.1.F*.

3.1.4 Restriction Table Update

To improve the performance of the CEVA-XM4 V1.1.1, a bypass was added to the core, and the restriction tables in Sections 6 and 7 of the *CEVA-XM4 Architecture Specification Vol. II V1.1.1.F* were updated.

4. Core Differences between CEVA-XM4 V1.1.1.F and V1.1.2.F

The following are the differences in the core between the CEVA-XM4 V1.1.1.F and V1.1.2.F releases. All cross-references are to the *CEVA-XM4 Architecture Specification Vol. II V1.1.2.F*.

4.1.1 MM3K Compatibility

Remark for MM3K compatibility was added to the relevant ISAs.

For more details, see the relevant instruction in the *CEVA-XM4 Architecture Specification Vol. II V1.1.2.F*.

5. Core Differences between CEVA-XM4 V1.1.2.F and V1.1.3.F

The following are the differences in the core between the CEVA-XM4 V1.1.2.F and V1.1.3.F releases. All cross-references are to the *CEVA-XM4 Architecture Specification Vol. II V1.1.3.F*.

5.1.1 vhist Operation Description Bug

For 32-bit increments with the *vhist* instruction, the operation's description was changed to 32-bit increments instead of 16 bits.

For more details, see the relevant instruction in the *CEVA-XM4 Architecture Specification Vol. II V1.1.3.F*.