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HDLs Evolve as they Affect Design Methodology for a Higher Abstraction and a Better Integration

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I. ABSTRACT

The history of hardware description language goes back to 1960's when IBM introduced APL (A Programming Language) for their in-house digital circuit modeling and simulation. The early 1970's witnessed a rise of HDLs like AHPL (originally derived from APL), DDL, CDL, and other primarily register transfer level (RTL) languages. The advent of VHDL in the 1980's formalized RTL languages and gave a new meaning to electronic design automation (EDA). Thanks to today's HDL based electronic design, methodologies and tools for simulation, synthesis, verification, physical modeling, and post-manufacturing test are now well in-place and are essential for digital designers. With the present changes in electronic system design technology, which has defined ESL as the next higher level of design abstraction, and mixed-signal simulation requirements, HDLs are being redefined and evolving to a higher level. At this level, digital design is redefined as putting together digital, analog, and software components, and defining communication between them. This requires new design methodologies based on new HDLs. On the other hand, handling such variety of components requires well integrated tools and easy interfacing between design components. This talk begins with a presentation of history of HDLs in the last half-a-century. Tools as they became available to digital designers at various abstraction levels will be discussed. Environments and methodologies as they evolved and as they changed requirements for hardware description languages will be discussed. We will show how new HDLs are dealing with the issue of integration. The talk concludes by presentation of shortcomings of existing HDLs and areas for research and development in this area.

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