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It's an FPGA!

The birth of the fabless model.

"Real men have fabs" is a remark famous in the semiconductor industry, made in the early 1990s by the CEO of AMD, Jerry Sanders. The statement was clearly a defensive reaction to exploding competition from a flurry of IC start-ups that maneuvered their way into the semiconductor business by embracing what we know today as the fabless chip model, pioneered by Xilinx Inc. and others in the early 1980s. The fabless model smashed the barriers to entry into the semiconductor business and sped up the pace of IC and electronic product innovation. While today the vast majority of chip companies, including AMD, are fabless or partially fabless, establishing the model was a harrowing, revolutionary adventure.

Before the rise of the fabless model, if a company wanted to create its own chips it had to be an integrated device manufacturer (IDM). Not only did it have to design those chips, it also had to assume the responsibility and costs of manufacturing them in a fabrication facility, or "fab." Therefore, in addition to hiring engineers to design, lay out, verify, and test the chip, a company needed to buy or lease proper facilities outfitted with clean rooms; extremely expensive manufacturing, testing, and safety equipment; and expensive materials (a slew of chemicals, wafers, and an endless supply of water) to build them. It also needed to employ a relatively large and highly trained staff of chemical, mechanical, and IC process engineers, as well as electrical engineers and skilled laborers.

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By this time, Moore's law was in full swing. Just to stay in business—let alone remain competitive—IC companies had to double the transistor counts of their chips every 22 months. Every new cycle of Moore's law required companies to buy new equipment, however; in some instances, they had to break ground to build entirely new buildings. This was a daunting task, given that every new generation of capital equipment required at least double the cost outlay of the last one. To offset the costs of building the fab, a company needed to keep it running at full capacity, which meant lulls in demand and recessions were extremely hazardous to the finances of any entity that owned and maintained a semiconductor fab.

Needless to say, all this made for an extremely high barrier to entry into the IC business. To be in the semiconductor game, to build infrastructure and then keep pace with Moore's law, a company had to have copious amounts of cash with which to weather the boom-and-bust cycles. If it was a start-up, it needed an ironclad proposition to secure the vast amounts of funding necessary to build a manufacturing facility as well as employ an IC design group.

In the mid-1980s, armed with a fantastic silicon invention, a small group of real men—and real women—took steps that would change the game forever. At that time, there were dozens, perhaps hundreds, of application-specific IC (ASIC) companies building custom silicon for thousands of customers. An engineer at Zilog named Ross Freeman had conceived of a new logic circuit that was reprogrammable: a single piece of silicon that could meet the needs of all of those ASIC customers. He left Zilog to further develop the concept of this circuit, later named the field-programmable gate array (FPGA); the hardware had not yet been designed. Nevertheless, the invention was impressive enough that Freeman was able to sway a former coworker from Zilog, Jim Barnett, to help him recruit a famous electronics executive named Bernie Vonderschmitt from Zilog to be the CEO of a new start-up. Prior to joining Zilog, Vonderschmitt had headed up RCA's IC development and manufacturing business. As such, he had the star power the team needed to secure investors. The trio officially founded Xilinx in February 1984 (see Figure 1).

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Having management with silicon business experience was critical to securing funding in those days. Vonderschmitt was clearly convinced of the potential of the FPGA, though he had no true intention of getting into the manufacturing game again. Having already experienced the stresses and risks of manufacturing, Vonderschmitt planned to have Xilinx focus on what Xilinx did best—designing innovative programmable ICs—and to partner with others to access skills that were not within its area of expertise.

In pursuit of this vision, Vonderschmitt leveraged his friendship with fellow fab-management executives at Japan's Seiko Corp. to see if Seiko would be willing to manufacture the first FPGAs for Xilinx. While he was at RCA, Vonderschmitt had in fact helped Seiko, an RCA partner, enter the semiconductor business. In pitching the Xilinx proposal, Vonderschmitt convincingly argued that such a partnership would let Seiko keep its fab running at capacity to further offset costs and perhaps even make a profit if the FPGAs were successful. Xilinx would further sweeten the deal by granting Seiko exclusive FPGA reselling rights in Japan. On the basis of friendship and, literally, a handshake (at the outset there was no formal contract), Xilinx's fabless business was launched (see Figure 2). Xilinx became a semiconductor manufacturer—without the semiconductor manufacturing.

FIGURE 1: Seated, left to right: Xilinx founders Freeman, Vonderschmitt, and Barnett. Back row: Early Xilinx executives Frank Myers, Wes Patterson, and Scott Brown, circa 1988 at Xilinx's first headquarters in San Jose, California.

Planning the First Fabless Chip

The task of actually designing the first functional FPGA fell to a

young engineer named Bill Carter, whom Freeman and Barnett had recruited from Zilog in March 1984 (see Figure 3).

It was a brave new world for the young designer. Up until that time, Carter had only worked with bipolar and n-type metal-oxide semiconductor (NMOS) circuits, and this would be his first foray into complementary MOS (CMOS) design. The design constraints were daunting. This was going to be a very large chip. Programmability required many, many transistors, and area was going to be at a premium to keep down the cost of the final product. What's more, Carter also had to figure out a way to implement this new IC and work with a fab on the other side of the Pacific, overcoming barriers of language, business culture, and engineering culture. The task of designing the device was complicated by the fact that Vonderschmitt regularly advised Carter to keep it as simple as possible and not try anything "too clever or exotic." An overly complex design could make it harder to produce a functional device and deliver it to customers on schedule.

Keeping risk to a minimum was very important to Vonderschmitt. He realized that a tiny, start-up company offering a first-of-its-kind chip through a unique fabless business model could scare off customers. In fact, to downplay the risk of doing business with the new company, Vonderschmitt told would-be customers that Xilinx planned to build a fab once it hit a US$50 million run rate and would also secure a second source, as was customary at the time. (It's interesting to note that Xilinx's first second-source partner was Monolithic Memories, later acquired by Sanders's AMD. Thus, AMD for years served as an active second source of Xilinx FPGAs.)

Keeping risk to a minimum in the design and manufacturing of the device certainly added to the design team's pressure to deliver. Carter and his very small team had to meet with Seiko's manufacturing engineers to see what types of circuits and silicon features Seiko could manufacture given the unique specification of the FPGA. Seiko's logic IC fab at the time was using a 2.5-μm process, a relatively mature and low-risk silicon process with which Seiko had been manufacturing gate arrays. Gate arrays employed fairly conservatively spaced structures, but the FPGA design would not. In fact, the XC2064 FPGA would have 85,000 transistors forming 64 configurable logic blocks and 58 input/output (I/O) blocks—larger than most microprocessors at the time and much bigger than anything Seiko's own designers had attempted, at roughly 300 mils per side (see Figure 4).

According to the first press release announcing the XC2064, the device would be a 1,000-ASIC-gate equivalent and run initially at 18 MHz, with a 33-MHz, 1,500-ASIC-gate-equivalent version planned for the future. To design the FPGA to spec, Carter knew he would have to pack its features as close together as possible. He thus had to push Seiko to thoroughly characterize its process and provide minimum feature widths. Carter had the feeling that, at least at first, his counterparts at Seiko were not too thrilled to be given the extra task of having to figure out how to manufacture someone else's IC, especially one with its own set of unique requirements. It also meant that Seiko had to open up the kimono, so to speak, to give outsiders a peek at its proprietary secrets and manufacturing procedures.

By July 1984, Carter and his counterparts at Seiko had developed a

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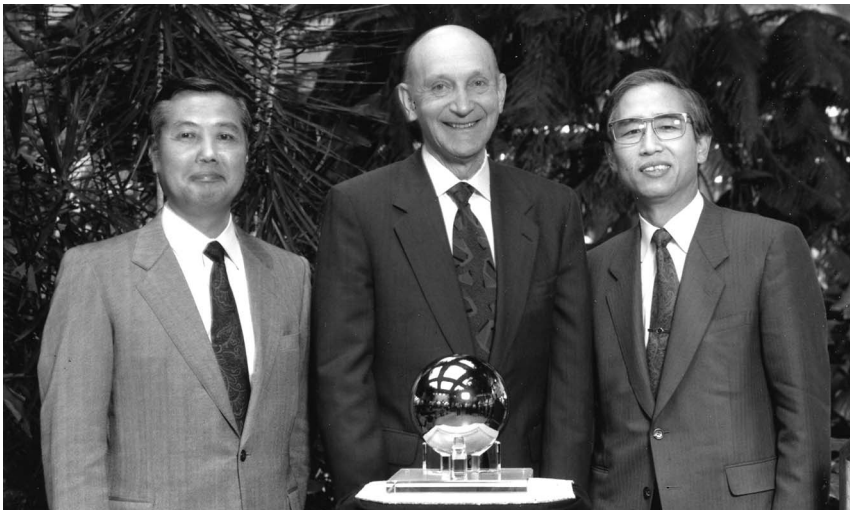

FIGURE 2: Pictured (left to right) circa 1992, at Xilinx's new headquarters in San Jose, California: Keizo Ichikawa, president of Xilinx KK in Japan; Xilinx CEO Bernie Vonderschmitt; and Saburo Kusama, the managing director and general manager of Seiko Epson Semiconductor Operations. In 2001, Kusama became the president of Seiko Epson Corp. He retired in 2005.

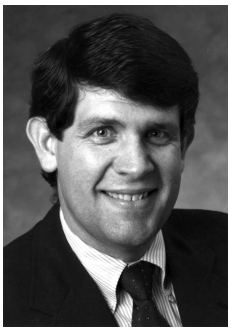

FIGURE 3: Bill Carter, circa 1988. His design team created the first FPGA, which established the fabless model.

good working relationship and were able to put a plan in place. Soon afterward, Carter and another hardware engineer began work on the final design of the first FPGA.

Designing the First Fabless Chip

With so much risk in the business process, Carter put together a particularly risk-averse design process. The architecture was largely based on one modular configurable logic block (CLB) and one modular I/O block repeated many times throughout the design. Some of the CLBs on the corners and edges required slight variations. Still, the repetition and use of modular blocks greatly simplified the design—enough so that logic design and logic verification were done manually. The company didn't use any computer-aided design (CAD) system, because CAD systems of the time were notoriously unreliable and in any case were too expensive for a start-up on a shoestring budget.

Because Carter's team was employing such extensive design reuse, it could concentrate the bulk of its time on circuit-level design and Simulation Program with Integrated Circuit Emphasis (SPICE) verification of the unique and more exotic blocks. Though the majority of the massive design was elegantly simple, some of the design techniques used for the FPGA were unconventional. Where a typical CMOS design of the time always used one p-channel transistor for every n-channel device in a circuit, Carter's design drew on his NMOS design experience and employed fewer p-channel and more n-channel devices to improve performance and save space.

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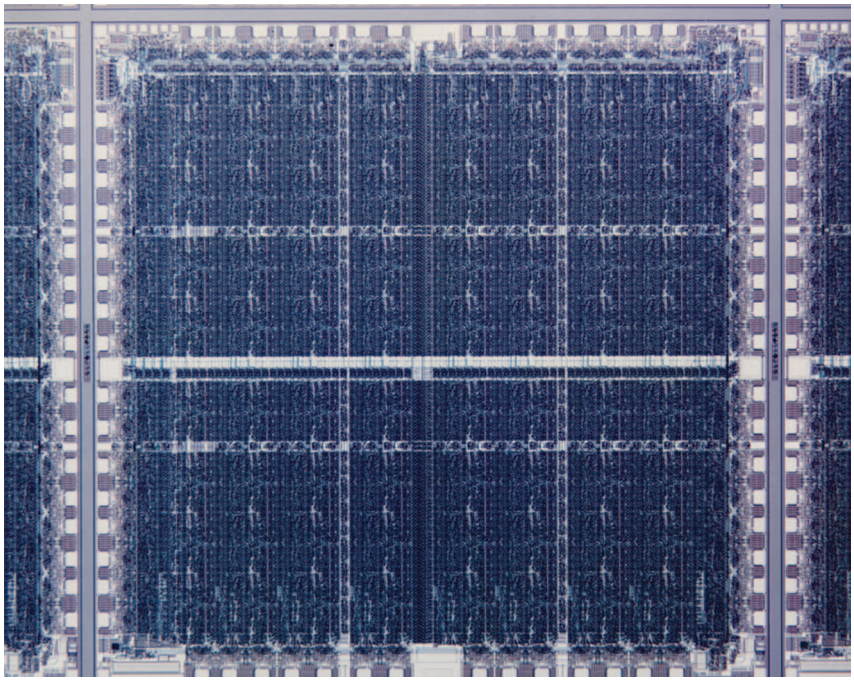

FIGURE 4: The world's first FPGA, the XC2064, was implemented on Seiko's 2.5-μm CMOS process. It featured 85,000 transistors forming 64 CLBs and 58 I/O blocks. This 1,000-ASIC-gate equivalent initially ran at a whopping 18 MHz.

The design budget did, however, allow the team to initially lease SPICE simulation time on a Control Data Corporation (CDC) mainframe, accessed via a dial-up connection. The simulation was extremely slow, and a simple syntactic error or typo could mean many lost hours. Waiting in the queue for the job to run only to have that run fail because of a silly mistake was frustrating in the extreme for a start-up with a critical, looming product delivery deadline. Luckily, right around this time, an inexpensive version of SPICE that ran on a personal computer became available. Carter convinced Vonderschmitt to invest in a few PCs, and he used them to verify that the SPICE deck syntax was correct before submitting the simulation to the mainframe.

The team discovered that although the simulation ran very slowly on the PC, the elapsed time was about the same as waiting for the job to run on the mainframe. It eventually did away with the CDC subscription. The team did all its design rule checks at the end of the process, including electronic CAD (ECAD) electrical rule checks to find simple errors, and then manually typed the final layout's cell coordinates into a Calma digitizer, which allowed it to see the complete design laid out for the first time. After further rounds of checks, the team sent the nine-layer design out to run through a pattern generator in preparation for mask production, which was done by Seiko. The chip taped out in late May 1985.

Powering Up the First Fabless Silicon

After delivering the design to Seiko, Carter's team had to wait until early July to receive first-run silicon: a box of 25 wafers. Powering them up entailed many nervous hours, as the team applied probes, a home-brew debugger, and a curve tracer to the wafers to see if the chips could be powered up, let alone programmed with a bit stream.

The first ten wafers out of the box all produced dead shorts. On the 11th try, the test finally yielded a wafer that showed signs of life, albeit with very high current draw. The next 14 wafers also produced dead shorts. Fortunately, with this one good wafer Carter's team deduced that insufficient etching in the manufacturing process was the cause of at least part of the problem. Aluminum whiskers missed in the etching process had short circuited different metal traces together, creating dead shorts on the 24 defective wafers. On the single relatively healthy wafer, the whiskers were extremely thin and worked in a manner similar to fuses. When enough power was applied, the current would burn out the whiskers, breaking the short.

The chips on that one wafer were robust enough to let Carter's team continue debugging and eventually run a simple bit stream into the device. The team successfully programmed in an inverter, after which Carter called Freeman and Vonderschmitt, who were traveling in Japan, to report that the DONE line had "gone high" and Xilinx had "successfully created the world's most expensive inverter." Much rejoicing ensued, and in short order the designers were able to program a vast array of features into the device, eventually populating an entire FPGA with a broad spectrum of circuits—all on a single, reprogrammable device.

Xilinx and Seiko worked together to solve the whisker issue and a few others, and soon the XC2064, the world's first FPGA, was commercially available. It was the beginning of a fruitful relationship between the two companies. In addition to providing an additional revenue stream to Seiko, running FPGAs with their repetitive structures through the fabs helped Seiko debug subsequent generations of silicon processes and produce greater yields and lower costs for all devices it manufactured. This use of FPGAs as a "process driver" allowed Xilinx access to leading-edge manufacturing technology at Seiko and at other foundries.

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The Rest Is History

Carter's team had made Freeman and Vonderschmitt's dream a reality—and Xilinx's backers very happy (see Figure 5). Indeed, the experience was the beginning of an exciting new chapter in semiconductor and electronics history. Soon, other IDMs started to supplement their fab expenses by manufacturing devices for third parties. In due course, an entire new subindustry of merchant foundries led by TSMC, UMC, and Chartered emerged to change the face of the semiconductor industry altogether and enable even a small company of entrepreneurial designers to realize their innovations in real silicon. Today, there are more than 1,300 fabless companies worldwide, according to the Global Semiconductor Alliance—a true testament

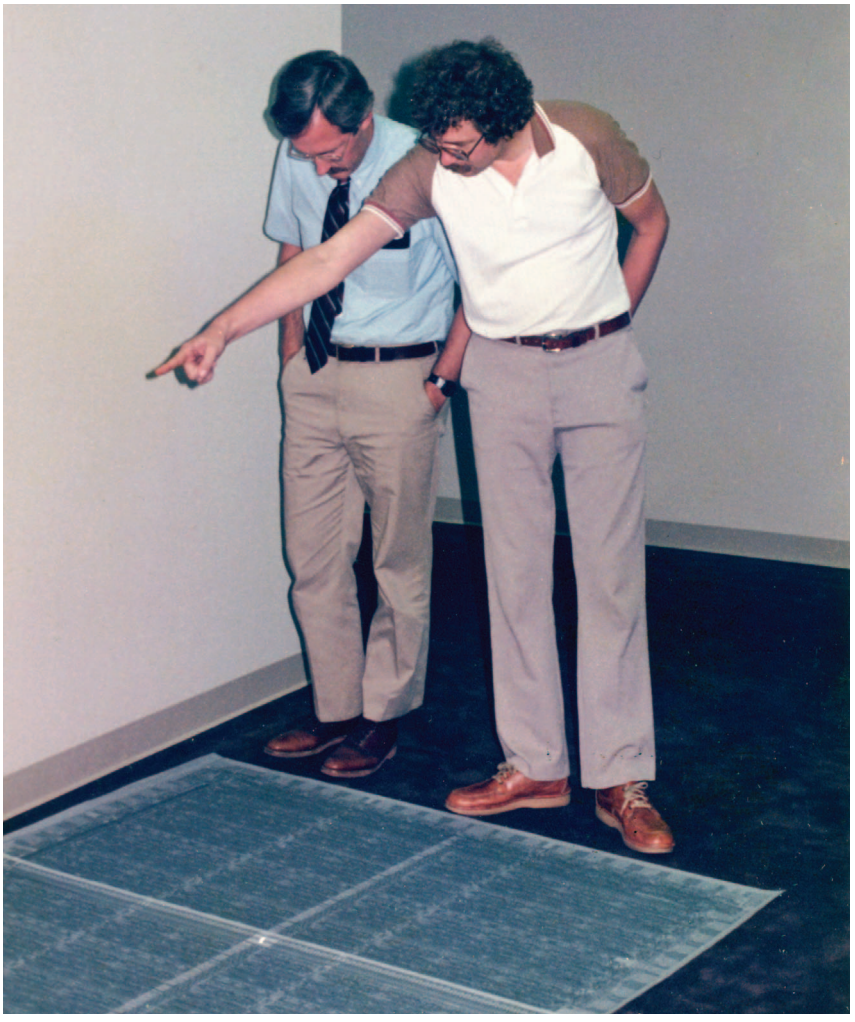

FIGURE 5: Freeman (circa 1985) looks over a plot of the XC2064.

to the charisma and genius of Bernie Vonderschmitt.

Indeed, the relationship between Seiko's executives and Vonderschmitt was so strong that Saburo Kusama, who later became president of Seiko Epson Corp., traveled all the way to the tiny town of Jasper, Indiana, in 2004 to visit Vonderschmitt's grave. Vonderschmitt died in June of that year, two years after retiring from Xilinx. In 2009, Ross Freeman—who died in 1989 at the age of 45—was posthumously inducted into the National Inventor's Hall of Fame for originating the FPGA (see www.uspto.gov/main/homepagenews/2009feb12.htm). Bill Carter and members of the Freeman and Vonderschmitt families were among the many attendees.

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Acknowledgments

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About the Authors

Peter Alfke came to the United States in 1966, with a German M.S.E.E. degree and nine years' experience in digital systems and circuit design at LM Ericsson and Litton Industries in Sweden. He has been a manager and later a director of applications engineering for more than 30 years at Fairchild, Zilog, AMD, and, from 1988, Xilinx. In 1970, he invented a serial architecture that became the basis of the HP-35 scientific calculator. He holds more than 30 patents, has written many application notes, has presented at numerous design conferences, and has given many applications-oriented seminars in the United States and Europe. After 22 years at Xilinx, he retired in September 2009.

Ivo Bolsens is senior vice president and CTO with responsibility for advanced technology development at Xilinx Research Laboratories and Xilinx University Program. He came to Xilinx in June 2001 from the Belgium-based research center IMEC, where he was vice president of information and communication systems. His research included the development of knowledge-based verification for very large scale integration circuits, design of digital signal processing applications, and wireless communication terminals. He also headed the research on design technology for high-level synthesis of DSP hardware, hardware-software codesign, and system-on-chip design. He holds a Ph.D. in applied science and an M.S.E.E. from K.U. Leuven, Belgium.

Bill Carter is the former CTO of Xilinx, where he helped pioneer the development on the first FPGA. Prior to joining Xilinx, he designed and managed the design of NMOS microprocessors and peripherals at Zilog. He was a member of the Custom Integrated Circuit Conference Technical Program Committee from 1987 through 1993. He received his B.S.E.E. and M.S.E.E. degrees from Santa Clara University. He received Santa Clara University's 1996 Distinguished Engineering Alumni Award. In addition to being a member of Santa Clara University's Board of Fellows, he also participates on its Engineering Advisory Board, as well as the Center for Science, Technology, and Society Advisory Board. He has authored and coauthored several technical papers and holds ten U.S. patents.

Mike Santarini is the publisher of Xilinx's award-winning customer magazine, *Xcell Journal*, and senior manager in the Corporate Communications Department at Xilinx, which he joined in 2008. For 14 years prior to joining Xilinx, he was an editor for the trade publications *EDN*, *EE Times*, and *Integrated System Design*.

Steve Trimberger has been employed at Xilinx since 1988. He is currently a Xilinx fellow, heading the Circuits and Architectures group at Xilinx Research Laboratories in San Jose, California. He was the technical leader for the XC4000 design automation software, developed a dynamically reconfigurable multicontext FPGA, led the architecture definition group for the Xilinx XC4000X device families, and designed the Xilinx bit-stream security functions in the Virtex FPGA product families. He has served as design methods chair for the Design Automation Conference, program chair and general chair for the ACM/SIGDA FPGA Symposium, and on the technical programs of numerous workshops and symposia. He has published three books and dozens of papers on design automation and FPGA architectures. He holds more than 180 patents in IC design, FPGA and ASIC architecture, CAE, and cryptography. His innovations appear today in nearly all commercial FPGA devices. He is a fellow of the Association for Computing Machinery.

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