Microprocessors And Microcontrollers

Assignment- Week 0

TYPE OF QUESTION: MCQ

Number of questions: 10 **Total mark: 10 X 1 = 10**

QUESTION 1:

The smaller unit of binary data

a) Nibble
b) Bit
c) Byte
d) word

Correct Answer: b

Detailed Solution: Bit: The smallest unit of binary data is a bit (short for "binary digit"). A bit can have only two possible values: 0 or 1. It is the fundamental building block of binary data in computing.

Nibble: A nibble is a group of 4 bits. For example, 1010 is a nibble.

Byte: A byte consists of 8 bits. It is the standard unit of data storage in most computer systems.

Word: A word refers to a data unit consisting of a fixed number of bits, depending on the computer architecture. For example, in a 32-bit system, a word is 32 bits, and in a 64-bit system, it is 64 bits.

QUESTION 2:

How many possible values for digital signals

a) 4

b) 2

c) 8

d) 1

Correct Answer: b

Detailed Solution:

Digital signals are based on the binary number system, which has only **two possible states**:
0 and **1**.

These two states represent the two voltage levels typically used in digital electronics:

0 (Low or Off)

1 (High or On)

This binary nature of digital signals allows for reliable representation and transmission of data in computers and digital devices

---

QUESTION 3:

Which number system has a base of 16

a) Decimal
b) Octal
c) Hexadecimal
d) Binary

Correct Answer: c

Detailed Solution:

Number systems are categorized based on their **base** (or radix), which indicates the number of unique digits, including zero, used in the system.

Hexadecimal (Base 16):

The **hexadecimal number system** has a base of **16**, meaning it uses 16 unique symbols: **0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F**.

Here, the letters **A** to **F** represent the decimal values **10 to 15**, respectively.

Decimal (Base 10):

The decimal system is the standard number system with a base of **10**. It uses the digits **0–9**.

Octal (Base 8):

The octal system has a base of **8**, using the digits **0–7**.

Binary (Base 2):

The binary system has a base of **2**, using only the digits **0** and **1**.

QUESTION 4:

Single Flip-Flop can store ____ bits of information.

a) 2
b) 32
c) 64
d) 1

Correct Answer: d

Detailed Solution:

A flip-flop is a basic building block in digital electronics, primarily used for storing a single bit of data. A single flip-flop can store only 1 bit of information, which can either be 0 or 1.

Flip-flops are bistable devices, meaning they have two stable states:

Set state (1)

Reset state (0)

Depending on the input signals and the type of flip-flop (e.g., SR, D, JK, T), it can store and maintain the bit value until it is changed by a clock signal or another input.

1 flip-flop = 1 bit of data storage.

To store multiple bits of data, a group of flip-flops (registers) is used:

For example, 8 flip-flops are needed to store 1 byte (8 bits).

QUESTION 5:

A 64 bit word consists of

a) 4 bits
b) 4 bytes
c) 8 bytes
d) 8 bits

Correct Answer: c

Detailed Solution:

8 bits = 1 byte.
64/8= 8 bytes.

QUESTION 6:

What is the high speed memory between the main memory and CPU called?

a) Magnetic Disk
b) Cache memory
c) DRAM
d) Secondary memory

Correct Answer: b

Detailed Solution:

It is called the Cache Memory. The cache memory is the high speed memory between the main memory and the CPU.

QUESTION 7:

Which of the following best describes random-access memory (RAM)?

a) A type of memory in which access time depends on memory location
b) They lose memory when power is removed
c) A type of memory in which access time is the same for any memory location
d) both b & c

Correct Answer: d

Detailed Solution:

b) They lose memory when power is removed:

RAM is a type of volatile memory, meaning it requires power to retain data. When the power is turned off, the data stored in RAM is lost.

c) A type of memory in which access time is the same for any memory location:

RAM is a random-access memory, meaning any memory location can be accessed in the same amount of time, regardless of its position.

d) both b & c:

Correct: Both b and c are true descriptions of RAM.

Volatile memory: Loses data when power is removed. Random access: Any memory cell can be accessed directly and in the same amount of time. Common types include DRAM (Dynamic RAM) and SRAM (Static RAM), with DRAM being slower but more widely used in modern computers.

QUESTION 8:

CPU stands for

a) Common purpose unit
b) Central processing unit
c) Central point unit
d) common processing unit

Correct Answer: b

Detailed Solution:

QUESTION 9:

CD-ROM is known as

a) Floppy Disk
b) Compact Disk Read Only Memory
c) Compressed Disk Read Only Memory
d) Compact Disk Random Access Memory

Correct Answer: b

Detailed Solution: CD-ROM (Compact Disk Read Only Memory) is a type of optical disk that is pre-pressed with data, which means the data is written onto the disk during its manufacturing process and cannot be altered or erased.

QUESTION 10:

What is the primary function of a register in a CPU?

a) To perform arithmetic operations
b) To store frequently accessed data or instructions temporarily
c) To connect the CPU to external devices
d) To hold non-volatile data

Correct Answer: b

Detailed Solution:

**********END*******

Microprocessors And Microcontrollers

Assignment 1- Week 1

QUESTION 1:

Correct Answer: b

Detailed Solution:

Step 1: Convert the numbers to binary

1. **2.625** in binary:
   - 2 = 10210_2102
   - 0.625 = 0.10120.101_20.1012
   - So, 2.625 = 10.101210.101_210.1012
2. **10.25** in binary:
   - 10 = 101021010_210102
   - 0.25 = 0.0120.01_20.012
   - So, 10.25 = 1010.0121010.01_21010.012

Step 2: Convert to 2's complement

To subtract 10.2510.2510.25 from 2.6252.6252.625, we need to represent −10.25-10.25−10.25 in 2's complement form.

1. **Represent 10.25**:
   - 10.25=1010.01210.25 = 1010.01_210.25=1010.012
2. **Invert the bits** for 1010.0121010.01_21010.012:
   - 1010.012→0101.1021010.01_2 \rightarrow 0101.10_21010.012→0101.102
3. **Add 1** to the result:
   - 0101.102+1=0101.1120101.10_2 + 1 = 0101.11_20101.102+1=0101.112

So, the 2's complement representation of −10.25-10.25−10.25 is 0101.1120101.11_20101.112.

Step 3: Perform the subtraction using 2's complement

Now, to subtract 10.2510.2510.25, we add 2.6252.6252.625 to the 2's complement of 10.2510.2510.25:

- 2.625=10.10122.625 = 10.101_22.625=10.1012
- −10.25=0101.112-10.25 = 0101.11_2−10.25=0101.112

Add these two numbers:

10.1012+0101.112 10.101_2 + 0101.11_210.1012+0101.112

Perform the binary addition:

- Add 101101101 and 110110110: this results in 101121011_210112, and carry over the 1.

The result will be 10000.011210000.011_210000.0112, which is the binary representation of the result.

Thus, the correct answer is **(11000.011)2**, which corresponds to option **b**.

QUESTION 2:

Correct Answer: a

Detailed Solution:

Step 1: Convert +1 to binary

In 4-bit binary, $+1$ is represented as:

$$0001_2$$

Step 2: Find the 2's complement to represent -1

To get the 2's complement (which represents negative numbers), perform the following:

1. **Invert the bits** of 0001_2, which gives:

$$1110_2$$

2. **Add 1** to the result:

$$1110_2 + 1 = 1111_2$$

So, -1 in 4-bit 2's complement is 1111_2.

QUESTION 3:

Correct Answer: a

Detailed Solution:

The range of values for n-bit number in 2's complement system is given as -2^{n-1} , $(2^{n-1} - 1)$. Substitute n = 4, we get the range as -8 to+7.

QUESTION 4:

Correct Answer: c

Detailed Solution:

The decimal equivalent would be $(1x2^0)+(1\times0.5^1)+ (1\times0.5^2)$ = ¾

QUESTION 5:

Correct Answer: c

Detailed Solution:

QUESTION 6:

Correct Answer: b

Detailed Solution:

QUESTION 7:

Correct Answer: c

Detailed Solution:

QUESTION 8:

Correct Answer: d

Detailed Solution:

QUESTION 9:

Correct Answer: d

Detailed Solution:

4K RAM need 12 address lines to access particular location, and CPU address width is 16 bit. Address lines A11 to A0 of CPU is connected to address bus of the memory, out of remaining 4 address lines of CPU 3 lines (A15'A14A13) connected to chip select(CS) of the RAM. Address line A12 can be 0 or 1, so the possible address range:

for A12 = 0 : 6000-6FFFH and

for A12 = 1 : 7000-7FFFH

QUESTION 10:

Correct Answer: a

Detailed Solution:

**************END*********

Microprocessors And Microcontrollers

Assignment 2- Week 2

TYPE OF QUESTION: MCQ

Number of questions: 15 **Total mark: 15 X 1 = 15**

QUESTION 1:

Correct Answer: b

Detailed Solution: A microprocessor is the central processing unit (CPU) of a computer system and is responsible for executing instructions. It typically contains:

- ALU (Arithmetic Logic Unit): Performs arithmetic and logical operations.
- Registers: Small, fast storage locations that temporarily hold data and instructions.
- Control Unit: Directs the operation of the processor by interpreting instructions and controlling the flow of data between the CPU and other components.

QUESTION 2:

Correct Answer: c

Detailed Solution: 1 MB (Megabyte) is equivalent to 1024 Kilobytes (KB). Here's the breakdown:

- 1 KB = 1024 bytes
- 1 MB = 1024 KB = 1024 * 1024 bytes = 1,048,576 bytes

QUESTION 3:

Correct Answer: c

Detailed Solution: The **Intel 8085 microprocessor** is a **40-pin** integrated circuit (IC). These pins include connections for data, address, power supply, control signals, and interrupt lines. The 8085 microprocessor is an 8-bit processor that was widely used in early microprocessor-based systems.

QUESTION 4:

Correct Answer: b

Detailed Solution: The **program counter (PC)** in the **8085 microprocessor** is a **16-bit register** because it is used to store the address of the next instruction to be executed. The 8085 microprocessor has **16 address lines**, which means it can access **2^16 = 65,536** memory locations (addresses), and hence the program counter needs to be a 16-bit register to store these addresses.

QUESTION 5:

Correct Answer: d

Detailed Solution: The **ALE (Address Latch Enable)** signal in the **Intel 8085 microprocessor** is used to demarcate the time when the address is being sent from the microprocessor to the memory or I/O device. When ALE is **high**, the **lower 8 bits** of the address are placed on the data bus. This allows the data bus to be used as the **low-order address bus** for accessing memory locations.

QUESTION 6:

Correct Answer: b

Detailed Solution: The **flag register** in the **Intel 8085 microprocessor** contains the status flags, which are used to indicate the result of arithmetic and logical operations. These flags are:

- **S (Sign flag)**: Set if the result of an operation is negative.
- **Z (Zero flag)**: Set if the result of an operation is zero.
- **AC (Auxiliary carry flag)**: Set if there is a carry from the lower nibble (used for BCD arithmetic).
- **P (Parity flag)**: Set if the result has an even number of 1's (indicating even parity).
- **CY (Carry flag)**: Set if there is a carry out of the most significant bit (for addition) or a borrow (for subtraction).

These flags are important for conditionally branching or for checking the results of operations.

QUESTION 7:

Correct Answer: d

Detailed Solution: The **Intel 8085 microprocessor** typically operates with a clock speed of **3.125 MHz**. This clock speed is derived from the clock cycle and is the frequency at which the microprocessor's internal operations, such as fetching instructions and executing them, occur.

QUESTION 8:

Correct Answer: a

Detailed Solution: The **flag register** holds the status flags that indicate the result of arithmetic and logical operations. These flags include the **Sign (S)**, **Zero (Z)**, **Auxiliary Carry (AC)**, **Parity (P)**, and **Carry (CY)** flags. These flags provide information about the nature of the result, such as whether the result is zero, negative, or if there was a carry or borrow during the operation.

QUESTION 9:

Correct Answer: b

Detailed Solution: The **CMA (Complement Accumulator)** instruction in the **8085 microprocessor** performs a **1's complement** of the contents of the accumulator. This means that it flips all the bits of the accumulator (i.e., converts 0s to 1s and 1s to 0s).

QUESTION 10:

Correct Answer: c

Detailed Solution: The **INX BC** instruction in the **8085 microprocessor** increments the **16-bit register pair BC** by one. It treats the contents of **B** and **C** together as a 16-bit value and adds one to it. This operation affects both registers (B and C), where the contents of **C** are incremented first, and if there is a carry, the contents of **B** are also incremented.

QUESTION 11:

Correct Answer: b

Detailed Solution: T The **parity flag** in the **8085 microprocessor** is set based on the number of 1s in the result. If the number of 1s in the result is **even**, the parity flag is **set** (indicating even parity). If the number of 1s is **odd**, the parity flag is **reset** (indicating odd parity).

In your case, the register contains **4EH** (which is **01001110** in binary). Let's count the number of 1s:

- **01001110** has **4 ones** (which is an even number).

Since the number of 1s is even, the **parity flag** is **set** (even parity).

QUESTION 12:

Correct Answer: c

Detailed Solution: A **program that uses mnemonics** refers to a **program written in assembly language**. In assembly language, human-readable mnemonics (such as `MOV`, `ADD`, `SUB`, etc.) are used to represent machine-level instructions. These mnemonics are later translated into machine code by an assembler.

QUESTION 13:

Correct Answer: d

Detailed Solution:

1. **RAL (Rotate Accumulator Left)**:
    - The **RAL** instruction performs a left rotation of the contents of the accumulator. This means that the most significant bit (MSB) is shifted into the carry flag, and the contents of the accumulator are shifted left by one position.
    - For **FFH** (which is `11111111` in binary), rotating it left results in **FEH** (`11111110`), and the **carry flag** will be set to 1.
2. **RLC (Rotate Left through Carry)**:
    - The **RLC** instruction performs a left rotation through the carry flag. The most significant bit (MSB) of the accumulator is shifted into the carry flag, and the contents of the accumulator are shifted left by one position, with the carry flag being inserted into the least significant bit (LSB).
    - After the **RAL** instruction, the **carry flag** is 1 (since the MSB of **FFH** is moved into it). When **RLC** is executed, the carry flag (which is now 1) will be placed into the LSB of the accumulator, and the new accumulator content will be **FFH** (`11111111`).

Summary:

- After **RAL**, the accumulator becomes **FEH** (`11111110`).
- After **RLC**, the accumulator becomes **FFH** (`11111111`).

QUESTION 14:

Correct Answer: c

Detailed Solution:

In the **8085 microprocessor**, the **LDAX** instruction is used to load the accumulator with the contents of memory pointed to by a register pair. However, the **LDAX** instruction only works with the **BC** and **DE** register pairs. It loads the accumulator with the value stored at the memory address specified by these register pairs.

- **LDAX BC**: Loads the accumulator with the 16-bit memory address contained in **BC**.
- **LDAX DE**: Loads the accumulator with the 16-bit memory address contained in **DE**.

The **HL** register pair is used for other operations like **LHLD** and **SHLD**, but it is **not** used in the **LDAX** instruction.

QUESTION 15:

Correct Answer: d

Detailed Solution: The **XRA A** instruction in the **8085 microprocessor** performs an **exclusive OR (XOR)** operation between the contents of the accumulator (**A**) and itself.

- **XOR operation** between any number and itself results in **0**.
  - So, **A XOR A = 00** (since any value XORed with itself gives 0).
- **Zero Flag (Z)**:
  - The **Zero Flag** is set (Z = 1) if the result of the operation is **zero**. Since the result of **XRA A** is **00**, the **Zero Flag** will be set to **1**.
- **Carry Flag (CY)**:
  - The **Carry Flag** is not affected by the **XRA** operation, so it remains unchanged. Since the **Carry Flag** was not set before the instruction and there is no carry in this operation, **CY = 0**.

Summary:

After executing **XRA A**:

- **A = 00** (the contents of the accumulator are zero).
- **CY = 0** (the carry flag is not affected).
- **Z = 1** (the zero flag is set because the result is zero).

Microprocessors And Microcontrollers

Assignment 3- Week 3

TYPE OF QUESTION: MCQ

Number of questions: 15 **Total mark: 15 X 1 = 15**

QUESTION 1:

Correct Answer: b

Detailed Solution:

1. `XRA A`: This instruction XORs register A with itself, effectively clearing register A (set to 0).
2. `MVI C, 05H`: This instruction loads register C with the value 05H (5 in decimal).
3. `LOOP: DCR C`: This instruction decrements the value in register C by 1.
4. `JNZ LOOP`: This instruction jumps back to `LOOP` if the Zero flag is not set (i.e., if C is not zero).

The loop will start with C = 5. Each time through the loop, C is decremented, and the loop continues as long as C is not zero. Therefore:

- First iteration: C = 5 → decremented to 4.
- Second iteration: C = 4 → decremented to 3.
- Third iteration: C = 3 → decremented to 2.
- Fourth iteration: C = 2 → decremented to 1.
- Fifth iteration: C = 1 → decremented to 0.

When C becomes 0, the `JNZ` instruction will fail (because the Zero flag is set), and the loop will exit.

Thus, the loop will be executed **five times**.

QUESTION 2:

Correct Answer: d

Detailed Solution:

In the 8085 microprocessor, the flags (Zero, Carry, Sign, and others) can be affected by various instructions, including conditional branch instructions. However, the specific behavior of conditional branch instructions depends on the flags that they check. Here's a breakdown:

- **Zero flag (Z)**: The Zero flag is checked and affected by instructions like `JZ` (Jump if Zero) or `JNZ` (Jump if Not Zero). These instructions make decisions based on the status of the Zero flag, so it is not unaffected.
- **Carry flag (C)**: The Carry flag is checked and affected by conditional branch instructions like `JC` (Jump if Carry) or `JNC` (Jump if No Carry), meaning it is also not unaffected.
- **Sign flag (S)**: The Sign flag, which indicates the sign of the result in the accumulator, is also checked by conditional branch instructions like `JS` (Jump if Sign) or `JNS` (Jump if No Sign).
- **None of the given options**: This means that all of the listed flags (Zero, Carry, Sign) can be affected by conditional branch instructions. Therefore, none of the flags in the given options is unaffected.

QUESTION 3:

Correct Answer: a

Detailed Solution:

TRAP is non maskable interrupt, but other interrupts can be maskable using interrupt enable(IE).

QUESTION 4:

Correct Answer: d

Detailed Solution:

Whenever a interrupt signal encountered by MP, then MP stops execution of the current instruction and start service the interrupt.

QUESTION 5:

Correct Answer: a

Detailed Solution:

1. **MVI A, 65H**
   This instruction loads the accumulator (register A) with the value **65H** (101 in decimal). So, at this point:
   - **A = 65H**
2. **MVI B, 32H**
   This instruction loads register B with the value **32H** (50 in decimal). So, at this point:
   - **B = 32H**
3. **CMP B**
   The `CMP` instruction compares the contents of the accumulator (A) with the contents of register B. It performs the operation:
   - **A - B**
   - This operation is performed without modifying the accumulator. Instead, it updates the flags based on the result of the subtraction.
   - **65H (A) - 32H (B) = 33H**

   Since the result of the subtraction is **33H**, which is a positive value (non-zero), the **Zero flag** will be **reset** (set to 0) because the result is non-zero. The contents of the accumulator (A) remain **65H**, since `CMP` does not modify the accumulator.

Thus, after the execution:

- **Zero flag = 0** (because A ≠ B)
- **Accumulator contents = 65H** (unchanged after `CMP`)

QUESTION 6:

Correct Answer: c

Detailed Solution:

1. **MVI A, 35H**
   - The `MVI` instruction (Move Immediate) takes 2 bytes: 1 byte for the opcode and 1 byte for the immediate data.
   - This instruction occupies **2 bytes**.
2. **MVI B, 23H**
   - Similar to the previous instruction, `MVI B, 23H` also occupies **2 bytes** (1 byte for the opcode and 1 byte for the immediate data).
3. **ADD B**
   - The `ADD` instruction (Add Register) occupies **1 byte** because it only requires 1 byte for the opcode (since it adds the contents of register B to the accumulator).

Now, let's calculate the total size:

- **MVI A, 35H** = 2 bytes
- **MVI B, 23H** = 2 bytes
- **ADD B** = 1 byte

Total = 2 + 2 + 1 = **5 bytes**

QUESTION 7:

Correct Answer: c

Detailed Solution:

- **a) Stack is a last-in-first-out structure.**
  - This is **true**. The stack in the 8085 microprocessor follows the **LIFO** (Last-In, First-Out) principle, meaning the last item pushed onto the stack is the first one to be popped off.
- **b) Information is saved on the stack by pushing on it.**
  - This is **true**. The **PUSH** instruction is used to save information onto the stack, which involves writing data to the memory location pointed to by the stack pointer (SP).
- **c) Size of the register associated with the stack is 8 bits.**

- This is **false**. The **stack pointer (SP)** is a **16-bit register**, not an 8-bit register. It holds the address of the current top of the stack and allows for 16-bit memory addressing.

- **d) Information is retrieved on the stack by popping it off.**

  - This is **true**. The **POP** instruction is used to retrieve data from the stack by removing the topmost element and adjusting the stack pointer.

QUESTION 8:

Correct Answer: d

Detailed Solution:

- **a) LXI SP, 0FFFH**

  - This instruction loads the stack pointer (SP) with the address **0FFFH**. It is a valid operation, setting the SP to point to a specific memory address.

- **b) PUSH PSW**

  - The `PUSH PSW` instruction is valid. It pushes the contents of the **PSW (Program Status Word)** onto the stack. The PSW contains the accumulator and the flag register, which are stored in memory when this instruction is executed.

- **c) SPHL**

  - The `SPHL` instruction is valid. It copies the contents of the **HL** register pair to the stack pointer (SP), setting the SP to the address in HL. This operation is often used to manipulate the stack pointer.

- **d) POP C**

  - This instruction is **invalid**. The `POP` instruction is used to retrieve data from the stack, but it requires the use of a **16-bit register pair** to store the popped data. Register C is an **8-bit** register, so it cannot be used with the `POP` instruction. For example, valid `POP` instructions would be `POP BC`, `POP DE`, etc., which use 16-bit register pairs.

QUESTION 9:

Correct Answer: d

Detailed Solution:

This is **false**. The first `RET` instruction must always correspond to a previous `CALL` instruction. If a `RET` appears before a `CALL`, there is no return address on the stack, leading to undefined behavior or an error in program execution.

QUESTION 10:

Correct Answer: d

Detailed Solution:

- MVI C, 03H: Load register C with 03H.
- LXI H, 2000H: Load the HL register pair with 2000H. This means H = 20H and L = 00H.
- MOV A, M: Move the contents of the memory location pointed to by HL (2000H) into register A. The value at memory location 2000H is 18H.
  Now, A = 18H.
- DCR C: Decrement register C.
  C = 03H → 02H.

Loop - L1 (First Iteration)

- L1: INX H: Increment the HL register pair. Now HL = 2001H.
- MOV B, M: Move the contents of memory location 2001H into register B. The value at 2001H is 10H.
  Now, B = 10H.
- CMP B: Compare the contents of the accumulator (A = 18H) with B (B = 10H).
  A - B = 18H - 10H = 08H. Since the result is not zero, the Zero flag is not set.
- JNC L2: Since the Zero flag is not set, the jump does not occur, and we proceed to the next instruction.
- MOV A, B: Now, move the contents of register B (which is 10H) into register A.
  A = 10H.
- L2: DCR C: Decrement register C.
  C = 02H → 01H.
- JNZ L1: Since C is not zero, we jump to L1.

Loop - L1 (Second Iteration)

- L1: INX H: Increment the HL register pair. Now HL = 2002H.

- MOV B, M: Move the contents of memory location 2002H into register B. The value at 2002H is 2BH.
  Now, B = 2BH.
- CMP B: Compare the contents of the accumulator (A = 10H) with B (B = 2BH).
  A - B = 10H - 2BH = -1BH. Since the result is not zero, the Zero flag is not set.
- JNC L2: Since the Zero flag is not set, the jump does not occur, and we proceed to the next instruction.
- MOV A, B: Now, move the contents of register B (which is 2BH) into register A.
  A = 2BH.
- L2: DCR C: Decrement register C.
  C = 01H → 00H.
- JNZ L1: Since C is now zero, the loop terminates and we exit to the next instruction.

Post-Loop Operations

- STA 2100H: Store the contents of register A (which is 2BH) into memory location 2100H.
- HLT: Halt the program.

Final Register Contents

- A = 2BH
- B = 2BH
- C = 00H

Thus, the final contents of registers A, B, and C are 2BH, 2BH, and 00H, respectively.

QUESTION 11:

If an 8085 microprocessor works at a frequency of 1 MHz, determine the total delay of the following sequence of instructions (in seconds).

```
        MVI A, 0FH
        MVI B, 0FH
L1:     DCR B
        JNZ L1
```

a) 218 μs

b) 219 μs

c) 220 μs

d) 221 μs

Correct Answer: a

Detailed Solution:

Program Breakdown:

1. `MVI A, 0FH`
   - This instruction moves the immediate value **0FH** (15 in decimal) into register **A**.
   - The instruction takes **1 machine cycle**, which corresponds to **4 T-states**.
2. `MVI B, 0FH`
   - This instruction moves the immediate value **0FH** (15 in decimal) into register **B**.
   - The instruction takes **1 machine cycle**, which corresponds to **4 T-states**.
3. `L1: DCR B`
   - This instruction decrements the contents of register **B**.
   - **DCR** takes **1 machine cycle**, corresponding to **4 T-states**.
4. `JNZ L1`
   - This instruction checks if the **Zero flag** is **not** set and jumps back to **L1** if the condition is true.
   - **JNZ** takes **2 machine cycles** (since it may jump), corresponding to **10 T-states**.

Calculation of Total Delay:

Total Delay for Each Instruction:

1. `MVI A, 0FH` takes **4 T-states**.
2. `MVI B, 0FH` takes **4 T-states**.
3. `DCR B` takes **4 T-states**.
4. `JNZ L1` takes **10 T-states**.

The loop runs until **B** reaches 0. Initially, **B = 0FH** (15 in decimal), and **DCR B** will decrement **B** by 1 each time. The loop will execute 15 times because **B** starts from 15 and is decremented until it reaches 0.

- **Total time for one loop iteration = 4 (DCR B) + 10 (JNZ L1) = 14 T-states**.

Since the loop runs 15 times, the total time for the loop is:

- **Total loop time = 15 iterations × 14 T-states = 210 T-states**.

Total Time for the Program:

- **Total time = Time for `MVI A, 0FH` + Time for `MVI B, 0FH` + Total loop time**.
- **Total time = 4 (MVI A) + 4 (MVI B) + 210 (loop) = 218 T-states**.

Now, let's calculate the delay in seconds.

Calculation of Time in Seconds:

- The 8085 microprocessor works at **1 MHz**, which means the time for each T-state is:

$$\text{Time per T-state} = \frac{1}{\text{Frequency}} = \frac{1}{1,000,000} \text{ seconds} = 1 \ \mu\text{s}.$$

- Therefore, the total delay in microseconds is:

$$\text{Total delay} = 218 \times 1 \ \mu\text{s} = 218 \ \mu\text{s}.$$

QUESTION 12:

Correct Answer: b

Detailed Solution:

- LXI 3FFFH:
  - This instruction loads the stack pointer (SP) with the value 3FFFH.
  - So, after this instruction, SP = 3FFFH.
- PUSH B:
  - The `PUSH` instruction is used to push the contents of the register pair (in this case, the B register pair) onto the stack.
  - The B register pair contains the contents of registers B and C, and PUSH B stores these two 8-bit values onto the stack.

- Each PUSH instruction causes the stack pointer (SP) to be decremented by 2 because it is pushing two 8-bit values (16 bits total).
- So, after executing `PUSH B`, SP is decremented by 2:
  SP = 3FFFH - 2 = 3FFDH.

- HLT:
  - This instruction halts the program and does not affect the SP.

QUESTION 13:

Correct Answer: c

Detailed Solution:

The Program Status Word (PSW) in the 8085 microprocessor is a 16-bit register that contains two parts:

1. Accumulator (8 bits)
2. Flag Register (8 bits)

- The Accumulator holds the result of arithmetic and logical operations.
- The Flag Register contains the flags (Zero, Sign, Parity, Carry, and Auxiliary Carry), which indicate the status of the last operation.

Thus, the PSW is represented as the Accumulator and Flag Register pair.

QUESTION 14:

The total number of memory accesses involved (including opcode fetch), when an 8085 microprocessor executes the instruction **STA 2050H**, is:

a) 1
b) 2
c) 3
d) 4

Correct Answer: d

Detailed Solution:

The **STA 2050H** instruction stores the contents of the accumulator into the memory location 2050H. The execution involves the following steps:

1. **Opcode Fetch**: The microprocessor fetches the opcode for the STA instruction from memory. (1 memory access)
2. **Operand Fetch (Low Byte)**: The lower-order byte of the address (50H) is fetched from memory. (1 memory access)
3. **Operand Fetch (High Byte)**: The higher-order byte of the address (20H) is fetched from memory. (1 memory access)
4. **Memory Write**: The contents of the accumulator are written to the memory location 2050H. (1 memory access)

Total Memory Accesses: 1+1+1+1=41 + 1 + 1 + 1 = 41+1+1+1=4

QUESTION 15:

Correct Answer: d

Detailed Solution:

- **ADD C** directly refers to the **C** register as an operand, meaning the operand is in a register.
- The operation does not involve any memory address or an immediate value but instead directly uses the contents of the **C** register.

This is an example of **register addressing mode**, where the operand is specified by a register.

**************END*********

Microprocessors And Microcontrollers

Assignment 4- Week 4

TYPE OF QUESTION: MCQ

Number of questions: **15** **Total mark: 15 X 1 = 15**

QUESTION 1:

Correct Answer: b

Detailed Solution:

QUESTION 2:

Correct Answer: c

Detailed Solution:

The **Interrupt Vector Table (IVT) of the 8085 microprocessor** is a fixed memory location range where the addresses of the interrupt service routines (ISR) are stored.

Interrupt Vector Table (IVT) Range in 8085

- The **8085 processor** has **vectored interrupts** that jump to predefined memory locations.
- Each vectored interrupt has a **fixed 8-bit address**, meaning it must be within the first **256 bytes** of memory.
- These addresses range from **0000H to 00FFH**.

Breakdown of Interrupt Vector Addresses:

Interrupt	Vector Address
TRAP	0024H
RST 7.5	003CH
RST 6.5	0034H
RST 5.5	002CH

Interrupt	Vector Address
INTR (if vectored externally)	User-defined
RST 0	0000H
RST 1	0008H
RST 2	0010H
RST 3	0018H
RST 4	0020H
RST 5	0028H
RST 6	0030H
RST 7	0038H

QUESTION 3:

Correct Answer: b

Detailed Solution:

When RST 7 instruction encountered corresponding ISR starting at memory location 7*8 = $(56)_{10}$ = $(38)_{16}$ is executed.

QUESTION 4:

Correct Answer: c

Detailed Solution:

QUESTION 5:

INTR must remain active for how many T-states?

A) 16.5 T-states
B)17.5 T-states
C) 18.5 T-states
D) 19.5 T-states

Correct Answer: B

Detailed Solution:

QUESTION 6:

Multiply 03H and B2H (two 8-bit numbers) stored in memory locations 2200H and 2201H by repetitive addition and store the result in memory locations 2300H and 2301H. The output in 2300H and 2301H is

a) 04H and 16H

b) 16H and 02H

c) 03H and 16H

d) 16H and 03H

Correct Answer: b

Detailed Solution: (2200H) = 03H ; (2201H) = B2H

Result = B2H + B2H + B2H = 216H ; (2300H) = 16H ; (2301H) = 02H

QUESTION 7:

Correct Answer: a

Detailed Solution:

QUESTION 8:

Correct Answer: b

Detailed Solution:

QUESTION 9:

Correct Answer: c

Detailed Solution:

QUESTION 10:

Correct Answer: b

Detailed Solution:

QUESTION 11:

Correct Answer: b

Detailed Solution:

QUESTION 12:

Correct Answer: c

Detailed Solution:

QUESTION 13:

Correct Answer: a

Detailed Solution:

Bit 4 of the accumulator in the SIM instruction allows explicitly

resetting the RST 7.5 memory

QUESTION 14:

Correct Answer: b

Detailed Solution:

QUESTION 15:

How many 8-bit characters can be transmitted per second over a 9600 baud serial communication link using asynchronous mode of transmission with one start bit, eight data bits, two stop bits, and one parity bit?

a) 600

b) 800

c) 1000

d) 1200

Correct Answer: b

Detailed Solution: "9600 baud" means that the serial port is capable of transferring a maximum of 9600 bits per second.

Total Data To send = 1 bit(start) + 8 bits (char size) + 1 bit (Parity) + 2 bits (Stop) = 12 bits.

Number of 8-bit characters that can be transmitted per second = 9600/12 = 800.

**************END*********

NPTEL Online Certification Courses

Indian Institute of Technology Kharagpur

Microprocessors And Microcontrollers

Assignment 5- Week 5

TYPE OF QUESTION: MCQ

Number of questions: **15** **Total mark: 15 X 1 = 15**

QUESTION 1:

Correct Answer: C

Detailed Solution:

8051 Microcontroller consists of CPU, RAM, ROM, I/O devices, timers, serial and parallel ports

---

QUESTION 2:

Correct Answer: d

Detailed Solution:

8051 Microcontroller contains 4K bytes of internal ROM memory

---

QUESTION 3:

Correct Answer: c

Detailed Solution:

QUESTION 4:

Correct Answer: a

Detailed Solution:

Port 0 (pins 32-39):P0(P0.0~P0.7)
– 8-bit R/W - General Purpose I/O
– Or acts as a multiplexed low byte address and data bus for external memory design

QUESTION 5:

Correct Answer: b

Detailed Solution:

20MHz/12 = 1.6667 MHz

One machine cycle = 1/1.6667 = 0.6 micro seconds

QUESTION 6:

Correct Answer: d

Detailed Solution:

After RESET content of SP register is 07H

QUESTION 7:

a)

Correct Answer: c

Detailed Solution:

QUESTION 8:

Correct Answer: d

Detailed Solution:

QUESTION 9:

Correct Answer: a

Detailed Solution:

QUESTION 10:

Correct Answer: b

Detailed Solution:

8051 contains two 16 bit registers:PC and DTPR

QUESTION 11:

Correct Answer: c

Detailed Solution:

Bit 3 and bit 4 contains register bank selections bits

Bit 4	Bit3	
0	0	Select Register Bank0
0	1	Select Register Bank1
1	0	Select Register Bank2
1	1	Select Register Bank3

QUESTION 12:

Correct Answer: b

Detailed Solution:

QUESTION 13:

Correct Answer: c

Detailed Solution:

QUESTION 14:

Correct Answer: d

Detailed Solution:

GFO flag stored in PCON register

QUESTION 15:

Correct Answer: a

Detailed Solution:

**************END*********

NPTEL Online Certification Courses

Indian Institute of Technology Kharagpur

Microprocessors And Microcontrollers

Assignment 6- Week 6

TYPE OF QUESTION: MCQ

Number of questions: **15** **Total mark: 15 X 1 = 15**

QUESTION 1:

Correct Answer: c

Detailed Solution:

In register addressing mode one of the source or destination should be CPU register

---

QUESTION 2:

Correct Answer: c

Detailed Solution:

In immediate addressing mode source operand is constant. But the value should be less than FFFFH. So option C is coorect

---

QUESTION 3:

Correct Answer: b

Detailed Solution:

The SFR (Special Function Register) can be accessed by their names or by their addresses

Register A address is 0E0H, so option B is correct

QUESTION 4:

Correct Answer: b

Detailed Solution:

```
CLR A                ;A=0
MOV R1,#60H          ;load pointer. R1=60H
MOV R7,#16           ;load counter, R7=16
AGAIN: MOV @R1,A     ;clear RAM R1 points to
INC R1               ;increment R1 pointer
DJNZ R7,AGAIN        ;loop until counter=zero
```

option b is correct

QUESTION 5:

Correct Answer: a

Detailed Solution:

RAM locations from 20H-2FH are both bit addressable and byte addressable, so option a is correct

---

QUESTION 6:

Correct Answer: C

Detailed Solution:

QUESTION 7:

Correct Answer: d

Detailed Solution:

```
mov a,#54h   ; a = 54H
swap a       ; a = 45H
RL a         ; Rotate left contents of A , so A =  8AH
```

QUESTION 8:

a)

Correct Answer: d

Detailed Solution:

MUL AB → Multiply A by B, put the low-order byte in A , High-order byte in B

Carry flag(CY) is always cleared after this operation.

QUESTION 9:

Correct Answer: b

Detailed Solution:

```
MOV A,#2Fh       ; A = 2fh
MOV 0F0h,#12h    ; B = 12h
DIV AB           ; A = 02h, B = 0Bh
DIV AB           ; A = 00h, B = 02h
```

option b is correct

QUESTION 10:

Correct Answer: a

Detailed Solution:

QUESTION 11:

Correct Answer: b

Detailed Solution:

Timer in mode2 acts as 8-bit auto reload, THx holds a value which is to be reloaded TLx each time it overflows.

QUESTION 12:

Correct Answer: b

Detailed Solution:

The DA instruction is provided to correct the aforementioned problem associated with BCD addition; it will add 6 to the lower nibble or higher nibble if need

---

QUESTION 13:

Correct Answer: c

Detailed Solution:

Decrement of data pointer is not allowed

QUESTION 14:

Correct Answer: C

Detailed Solution:

QUESTION 15:

Correct Answer: a

Detailed Solution:

XCHD: Exchanges bits 0-3 of the Accumulator with bits 0-3 of the Internal RAM address pointed to indirectly by R0. Bits 4-7 of each register are unaffected.

**********END*******