WEEK 1

1. **Perform (2.625-10.25) using 2's complement arithmetic.**
   a) $(00111.101)_2$
   b) $(11000.011)_2$ ✅
   c) $(01100.111)_2$
   d) $(10011.001)_2$
   Score: 1
   Accepted Answer: b

2. **Represent $(-1)_{10}$ using 4-bit 2's complement representation.**
   a) $(1111)_2$ ✅
   b) $(1000)_2$
   c) $(-0001)_2$
   d) $(0001)_2$
   Score: 1
   Accepted Answer: a

3. **In 2's complement number system, the range of values for 4-bit number is given as**
   a) -8 to 7 ✅
   b) -16 to 16
   c) -7 to 8
   d) -7 to 7
   Score: 1
   Accepted Answer: a

4. **The fractional binary number (0.11) has a decimal value of**
   a) (%)10(%)10
   b) (%)10(%)10
   c) (%)10(%)10 ✅
   d) None of the above
   Score: 1
   Accepted Answer: c

5. **Which of the following components present in a computer?**
   a) CPU, Memory
   b) Peripherals
   c) Both a & b ✅
   d) None of the above
   Score: 1
   Accepted Answer: c

6. Program counter(PC) contains?
   a) Address of the current instruction
   b) Address of the next instruction to fetch
   c) Value of the operand ✅
   d) Starting address of the program
   Score: 1
   Accepted Answer: c

7. Instruction decoder
   a) Holds the address of the current instruction
   b) Contains next instruction to be fetch
   c) Decodes the OPCODE and generates control signals ✅
   d) Fetches operands from memory
   Score: 1
   Accepted Answer: c

8. Fastest memory present in a computer?
   a) Flash memory
   b) RAM
   c) ROM
   d) Registers ✅
   Score: 1
   Accepted Answer: d

9. If CS = A15^A14A13 is used as the chip select of a 4K RAM in an 8085 system, then its memory range will be
   a) 3000-3FFFH
   b) 7000-7FFFH
   c) 5000-5FFFH and 6000-6FFFH
   d) 6000-6FFFH and 7000-7FFFH ✅
   Score: 0
   Accepted Answer: d

10. ALU stands for
    a) Arithmetic Logic Unit ✅
    b) Arithmetic Lower unit
    c) Addition Logic Unit
    d) AND Logic Unit
    Score: 1
    Accepted Answer: a

WEEK 2

1. **Which of the following is correct.**
   a) A microprocessor contains ALU, flash memory and control units
   b) A microprocessor contains ALU, registers and control units
   c) A microcontroller contains ALU and control units only
   d) A microprocessor contains ALU only
   Score: 1
   Accepted Answer: a

2. **1 MB memory equivalent to**
   a) 1024 bits
   b) 1024 bytes
   c) 1024 KB
   d) 1024 GB
   Score: 1
   Accepted Answer: a

3. **8085 microprocessor has how many pins**
   a) 20
   b) 60
   c) 40
   d) 30
   Score: 1
   Accepted Answer: a

4. **The program counter in a 8085 micro-processor is a 16-bit register, because**
   a) It counts 16-bits at a time
   b) There are 16 address lines
   c) It can fetch two 8 bit data at a time
   d) none of the above
   Score: 1
   Accepted Answer: a

5. **In Intel 8085 microprocessor ALE signal is made high to**
   a) To fetch the instruction
   b) To increment the program counter
   c) Enable the data bus to be used as higher order address bus
   d) Enable the data bus to be used as low order address bus
   Score: 1
   Accepted Answer: d

6. **8085 microprocessor flag register contains**
   a) Address of the next instruction to be fetch
   b) S.Z.A.C.P.C.Y flags
   c) data required to execute current instruction
   d) starting address of the program
   Score: 1
   Accepted Answer: b

7. **The clock speed of 8085 is**
   a) 10 MHz
   b) 2.5 THz
   c) 8 MHz
   d) 3.12.5 MHz
   Score: 1
   Accepted Answer: d

8. **The register which holds the information about the nature of results of arithmetic and logic operations is called as**
   a) Flag Register
   b) Accumulator
   c) Program Counter
   d) Register B
   Score: 1
   Accepted Answer: a

9. **CMA instruction**
   a) Decrement the contents of the accumulator
   b) Performs 1's complement of the accumulator contents
   c) Performs 2's complement of the accumulator contents
   d) Increment the contents of the accumulator
   Score: 1
   Accepted Answer: a

10. **INX BC instruction**
    a) Increment the contents of register B by one
    b) Increment the contents of register C by one
    c) Increment the contents of register pair BC by one
    d) Contents of C is incremented but contents of B is unchanged
    Score: 1
    Accepted Answer: a

11. **If A register of 8085 contains 4EH, the parity flag is**
    a) Rest
    b) Set
    c) Not decidable
    d) Don't care
    Score: 1
    Accepted Answer: a

12. **A program that uses mnemonics is called**
    a) Object program
    b) Fetch cycle
    c) Assembly language
    d) Micro instruction
    Score: 1
    Accepted Answer: c

13. **In an 8085 processor, suppose the accumulator content is FFH and the carry flag is 0. What will be the content of the accumulator after RAL and RLC instructions?**
    a) Both FFH
    b) Both FEH
    c) RAL - FFH, RLC – FEH
    d) RAL - FEH, RLC – FFH
    Score: 0
    Accepted Answer: c

14. **Which register pair of 8085 is NOT accepted in LDAX instruction?**
    a) BC
    b) DE
    c) HL
    d) All pairs are acceptable
    Score: 0
    Accepted Answer: c

15. **After the execution of the instruction XRA A the contents of A, carry and zero flags are respectively**
    a) A = 00, CY = 1, Z = 1
    b) A = 00, CY = 0, Z = 0
    c) A = FF, CY = 1, Z = 0
    d) A = 00, CY = 0, Z = 1
    Score: 1
    Accepted Answer: c

WEEK 3

1) How many times will the following loop be executed?

```
XRA A
MVI C, 05H
LOOP: DCR C
JNZ LOOP
```

a) Once
b) Five times
c) Infinite times
d) Depends on the initial value of A

Score: 0
Accepted Answer: b

---

2) Which of the following flags is not affected by a conditional branch statement in an 8085 microprocessor?

a) Zero flag
b) Carry flag
c) Sign flag
d) None of the given options

Score: 0
Accepted Answer: d

---

3) The interrupt in an 8085 microprocessor that is not affected by the value of the Interrupt Enable (IE) flip flop is

a) TRAP
b) INTR
c) RST 5.5
d) RST 7.5

Score: 0
Accepted Answer: a

---

4) Which of the following statements regarding 8085 interrupts is FALSE?

a) An interrupt is a process that starts from an I/O device and is asynchronous.
b) An interrupt can either be a maskable or non-maskable.
c) An interrupt can either be a vectored or a non-vectored one.
d) An interrupt is serviced only after the microprocessor completes the execution of its current program.

Score: 0
Accepted Answer: d

---

5) What are the status of the zero flag and the contents of the accumulator after execution of the following 8085 assembly code?

MVI A, 65H
MVI B, 32H
CMP B

a) 0, 65H
b) 1, 65H
c) 0, 33H
d) 1, 00H

Score: 0
Accepted Answer: a

---

6) How many bytes does the following set of instructions occupy?

MVI A, 35H
MVI B, 23H
ADD B

a) Three bytes
b) Six bytes
c) Five bytes
d) Four bytes

Score: 0
Accepted Answer: c

---

7) Which of the following statements about the stack in an 8085 microprocessor is FALSE?

a) Stack is a last-in-first-out structure.
b) Information is saved on the stack by pushing on it.
c) Size of the register associated with the stack is 8 bits.
d) Information is retrieved on the stack by popping it off.

Score: 0
Accepted Answer: c

8) Which of the following operations on stack is an invalid one?

a) LXI SP, 0FFFH
b) PUSH PSW

c) SPHL
d) POP C

Score: 0
Accepted Answer: d

---

9) Which of the following statements regarding CALL and RET instructions is FALSE?

a) An 8085 program may contain multiple CALL instructions
b) An 8085 program may contain multiple RET instructions
c) In an 8085 program, the first CALL instruction may appear before the first RET instruction
d) In an 8085 program, the first RET instruction may appear before the first CALL instruction

Score: 0
Accepted Answer: d

---

10) What will be the contents of the registers A, B, and C, respectively, after the execution of the following 8085 program?

```
MVI C, 03H
LXI H, 2000H
MOV A, M
DCR C

L1: INX H
MOV B, M
CMP B
JNC L2
MOV A, B

L2: DCR C
JNZ L1
STA 2100H
HLT
```

Contents of memory locations:
2000H: 18H
2001H: 10H
2002H: 2BH

a) 2AH, 2BH, and 00H
b) 2BH, 2BH, and 02H
c) 2BH, 2AH, and 00H
d) 2BH, 2BH, and 00H

Score: 0
Accepted Answer: a

---

11) If an 8085 microprocessor works at a frequency of 1 MHz, determine the total delay of the following sequence of instructions (in seconds).

```
MVI A, 0FH
MVI B, 0FH

L1: DCR B
JNZ L1
```

a) 218 µs
b) 219 µs
c) 220 µs
d) 221 µs

Score: 0
Accepted Answer: a

---

12) Contents of the stack pointer (SP) after executing the following instructions?

```
LXI SP, 3FFFH
PUSH B
HLT
```

a) SP = 4001H
b) SP = 3FFDH
c) SP = 4000H
d) SP = 3FFEH

Score: 0
Accepted Answer: d

---

13) The Program Status Word register pair in an 8085 microprocessor is realized as the pair of which of the following registers?

a) Program Counter and Accumulator
b) Program Counter and Stack Pointer
c) Accumulator and Flag Register
d) Program Counter and Flag Register

Score: 0
Accepted Answer: c

14) The total number of memory accesses involved (including opcode fetch), when an 8085 microprocessor executes the instruction STA 2050H, is:

a) 1
b) 2
c) 3
d) 4

Score: 0
Accepted Answer: d

---

15) Identify the addressing mode of the following 8085 instruction.

ADD C

a) Implied addressing mode
b) Immediate addressing mode
c) Direct addressing mode
d) Register addressing mode

Score: 0
Accepted Answer: d

WEEK 4

1) With respect to 8085, match Column X with Column Y.
Column X

1. **INTR**
2. **RST 5.5**
3. **TRAP**
4. **RST 1**

Column Y

1. **Non-maskable**
2. **Maskable**
3. **Software**
4. **Non-vectored**

a) X1-Y2, X2-Y1, X3-Y4, X4-Y3
b) X1-Y4, X2-Y2, X3-Y1, X4-Y3
c) X1-Y3, X2-Y2, X3-Y4, X4-Y1
d) X1-Y1, X2-Y4, X3-Y2, X4-Y3

Score: 1
Accepted Answer: b

---

2) Interrupt vector table of 8085 ranges over
a) 0010H-0100H
b) 0000H-FFFFH
c) 0000H-00FFH
d) 0100H-01FFH

Score: 1
Accepted Answer: c

---

3) The instruction RST 7 is a:
a) Restart instruction that begins the execution of a program.
b) One-byte call to the memory address 0038H.
c) One-byte call to the memory address 0007H.
d) Hardware interrupt.

Score: 1
Accepted Answer: b

---

4) With respect to 8085, match Column X with Column Y.
Column X

1. **RST 5.5**
2. **RST 6**
3. **RST 7.5**
4. **RST 4.5**

Column Y

1. **Edge-triggered**
2. **Level-triggered**
3. **Edge and level triggered**
4. **Software**

a) X1-Y3, X2-Y1, X3-Y4, X4-Y2
b) X1-Y4, X2-Y2, X3-Y1, X4-Y3
c) X1-Y2, X2-Y4, X3-Y1, X4-Y3
d) X1-Y3, X2-Y4, X3-Y2, X4-Y1

Score: 0
Accepted Answer: a

---

5) INTR must remain active for how many T-states?
a) 16.5 T-states
b) 17.5 T-states
c) 18.5 T-states
d) 19.5 T-states

Score: 1
Accepted Answer: b

---

6) Multiply 03H and B2H (two 8-bit numbers) stored in memory locations 2200H and 2201H by repetitive addition and store the result in memory locations 2300H and 2301H. The output in 2300H and 2301H is
a) 04H and 16H
b) 16H and 02H
c) 03H and 16H
d) 16H and 03H

Score: 1
Accepted Answer: b

---

7) Which of the following is the correct ordering of the priority of the interrupts in 8085?
a) TRAP > RST 7.5 > RST 6.5 > RST 5.5
b) RST 7.5 > RST 6.5 > RST 5.5 > TRAP
c) TRAP > RST 5.5 > RST 6.5 > RST 7.5
d) RST 5.5 > RST 6.5 > RST 7.5 > TRAP

Score: 1
Accepted Answer: a

---

8) A direct memory access (DMA) transfer replies
a) Direct transfer of data between memory and accumulator
b) Direct transfer of data between memory and I/O devices without the use of microprocessor
c) Transfer of data exclusively within microprocessor registers
d) A fast transfer of data between microprocessor and I/O devices

Score: 1
Accepted Answer: b

---

9) The INTR interrupt may be masked using the flag
a) Direction flag
b) Overflow flag
c) Interrupt flag
d) Sign flag

Score: 1
Accepted Answer: c

---

10) At the end of ISR, the instruction should be
a) HLT
b) RET
c) END
d) NOP

Score: 1
Accepted Answer: b

---

11) Which of the following statement is TRUE?
a) In half duplex mode data transmission is one way
b) In half duplex mode data transmission is two way
c) In full duplex mode data transmission is one way
d) None of the above

Score: 1
Accepted Answer: b

---

12) The contents of the accumulator is AAH, after execution of SIM instruction
a) Interrupt RST 7.5 is enabled
b) Interrupt RST 6.5 is disabled
c) Interrupt RST 6.5 is enabled
d) Transmission of serial data is enabled

Score: 1
Accepted Answer: c

---

13) The contents of the accumulator is BAH, after execution of SIM instruction.
a) Reset the RST 7.5 flip-flop memory
b) Set the RST 7.5 flip-flop memory
c) Reset the RST 6.5 flip-flop memory
d) Interrupt RST 6.5 is disabled

Score: 0
Accepted Answer: a

---

14) What does the following set of instructions do in an 8085 microprocessor?
EI
MVI A, 08H
SIM

a) Resets the 7.5 interrupt in an 8085 system.
b) Enables all the interrupts in an 8085 system.
c) Enables the 5.5 interrupt and masks all other interrupts in an 8085 system.
d) Enables the 6.5 interrupt and masks all other interrupts in an 8085 system.

Score: 1
Accepted Answer: b

---

15) How many 8-bit characters can be transmitted per second over a 9600 baud serial communication link using asynchronous mode of transmission with one start bit, eight data bits, two stop bits, and one parity bit?
a) 600
b) 800
c) 1000
d) 1200

Score: 1
Accepted Answer: b

WEEK 5

1) A microcontroller at least should consist of:

a) RAM, ROM, I/O devices, serial and parallel ports and timers
b) CPU, RAM, I/O devices, serial and parallel ports and timers
c) CPU, RAM, ROM, I/O devices, serial and parallel ports and timers ✅
d) CPU, ROM, I/O devices and timers

Score: 1
Accepted Answer: c

---

2) What is the size of the internal ROM memory of 8051 Microcontroller?

a) 128 bits
b) 128 bytes
c) 4K bits
d) 4K bytes ✅

Score: 1
Accepted Answer: d

---

3) Number of pins present in 8051 Microcontroller?

a) 20
b) 30
c) 40 ✅
d) 80

Score: 1
Accepted Answer: c

---

4) Which of the following is true in the context of 8051 microcontroller?

a) I/O port 0 is used as 8-bit R/W general purpose input-output operations ✅
b) I/O port 1 is used as an address bus for external memory design
c) I/O port 2 is used for internal timers and external interrupts
d) None of the above

Score: 1
Accepted Answer: a

---

5) What is the time taken by one machine cycle if crystal frequency is 20MHz?

a) 1.085 microseconds
b) 0.60 microseconds ✅
c) 0.75 microseconds
d) 1 microsecond

Score: 1
Accepted Answer: b

---

6) The contents of SP register after RESET?

a) 06H
b) 00H
c) 0AH
d) 07H ✅

Score: 1
Accepted Answer: d

---

7) Which pin of port 3 has an alternative function as a write control signal for external data memory?

a) P3.0
b) P3.3
c) P3.6 ✅
d) P3.7

Score: 1
Accepted Answer: c

---

8) The SP is of ___ wide register. And this may be defined anywhere in the ____.

a) 8 byte, on-chip 128 byte RAM.
b) 8 bit, on-chip 256 byte RAM.
c) 16 bit, on-chip 128 byte ROM.
d) 8 bit, on-chip 128 byte RAM. ✅

Score: 1
Accepted Answer: d

---

9) Match the following:

1) TCON → **ii)** Timer / counter control register.
2) SBUF → **iv)** Serial data buffer for Tx and Rx.
3) TMOD → **iii)** Idle bit, power down bit.
4) PSW → **i)** Contains status information.
5) PCON → **v)** Timer/counter modes of operation.

a) 1-ii, 2-iv, 3-iii, 4-i, 5-v. ✅
b) 1-ii, 2-v, 3-iv, 4-iii, 5-i.
c) 1-v, 2-iii, 3-ii, 4-iv, 5-i.
d) 1-iii, 2-ii, 3-i, 4-v, 5-iv.

Score: 1
Accepted Answer: a

---

10) How many 16-bit registers are present in the 8051 microcontroller?

a) 1
b) 2 ✅
c) 3
d) 4

Score: 0 (Incorrect Attempt)
Accepted Answer: b

---

11) Which of the following is true if the contents of PSW is 16H?

a) Program uses registers from bank3
b) Carry flag set to 1
c) Program uses registers from bank2 ✅
d) Program uses registers from bank0

Score: 1
Accepted Answer: c

---

12) An alternate function of port pin P3.0 in the 8051 is:

a) Timer 0 external input
b) Serial input port
c) External data memory write strobe
d) External data memory read strobe ✅

Score: 0 (Incorrect Attempt)
Accepted Answer: d

---

13) How many 16-bit timers/counters are present in the 8051 microcontroller?

a) 8
b) 4
c) 2 ✅
d) 1

Score: 1
Accepted Answer: c

---

14) Which of the following Flag is not present in PSW?

a) Carry Flag (CY)
b) Parity Flag (P)
c) Overflow Flag (OV)
d) GF0 ✅

Score: 1
Accepted Answer: d

---

15) When the PUSH instruction is executed:

a) The SP is incremented by one
b) The SP is incremented by two ✅
c) The SP is decremented by one
d) The SP is decremented by two

Score: 0 (Incorrect Attempt)
Accepted Answer: b

WEEK 6

1. **Which of the following instructions of 8051 is not permitted?**

- **a) ADD A, R4**
- **b) MOV R0, A**
- **c) MOV R3, R2**
- **d) MOV R5, DPL**
  Correct Answer: c) MOV R3, R2

2. **Which of the following is a valid immediate addressing mode?**

- **a) MOV A, R1**
- **b) MOV 45h, A**
- **c) MOV A, #42h**
- **d) MOV DPTR, #68975h**
  Correct Answer: c) MOV A, #42h

3. **Which of the following instructions is equivalent to MOV A, #55h?**

- **a) MOV 0F0H, #55H**
- **b) MOV 0E0H, #55H**
- **c) MOV 0E0H, 55H**
- **d) MOV 0F0H, 55H**
  Correct Answer: b) MOV 0E0H, #55H

4. **Identify the operation performed by the following program**
   CLR A
   MOV R1, #60H
   MOV R7, #16
   AGAIN: MOV @R1, A
   INC R1
   DJNZ R7, AGAIN

- **a) Clear 16 ROM locations starting at ROM address 60H**
- **b) Clear 16 RAM locations starting at RAM address 60H**
- **c) Increment the contents of memory locations (60H-6FH) by one**
- **d) Increment the contents of memory locations (60H-75H) by one**
  Correct Answer: b) Clear 16 RAM locations starting at RAM address 60H

5. **Which of the following RAM locations are bit addressable?**

- **a) 20H-2FH**
- **b) 00H-0FH**
- **c) 70H-7FH**
- **d) 10H-1FH**
  Correct Answer: a) 20H-2FH

6. **What is the result after execution of SETB P1.5?**

- **a) Bit 5 of Register B is set to 1**
- **b) Bit 5 of port P1 is set to 0**
- **c) Bit 5 of port P1 is set to 1**
- **d) Bit 1 of port P5 is set to 1**
  Correct Answer: c) Bit 5 of port P1 is set to 1

7. **What is the contents of the accumulator after execution of the following instructions?**
   MOV A, #54H
   SWAP A
   RL A

- **a) 6DH**
- **b) A8H**

- **c) ABH**
- **d) 8AH**
  Correct Answer: d) 8AH

8. **Which of the following statement is true after execution of MUL AB?**

- **a) High-order byte of the result stored in B register when overflow flag is set to 1**
- **b) Carry flag is cleared to 0**
- **c) Lower-order byte of the result stored in A**
- **d) All of the above**
  Correct Answer: d) All of the above

9. **Identify the contents of A and B after the following instructions are executed.**
   MOV A, #2FH
   MOV 0F0H, #12H
   DIV AB
   DIV AB

- **a) A = 02H, B = 0BH**
- **b) A = 00H, B = 02H**
- **c) A = 02H, B = 00H**
- **d) A = 0BH, B = 02H**
  Correct Answer: b) A = 00H, B = 02H

10. **Indicate which mode and which timer are selected for the following instruction.**
    MOV TMOD, #20H

- **a) Mode 2 of timer 1 is selected**
- **b) Mode 2 of timer 0 is selected**
- **c) Mode 1 of timer 1 is selected**
- **d) Mode 1 of timer 0 is selected**
  Correct Answer: a) Mode 2 of timer 1 is selected

11. **Which of the following statements is true if a timer operates in mode 2?**

- **a) It is a 16-bit timer**
- **b) When the TL register overflows, TL is reloaded automatically with the original value kept by the TH register**
- **c) It is a 13-bit timer**
- **d) When the TL register overflows, TL register is loaded with 00h**
  Correct Answer: b) When the TL register overflows, TL is reloaded automatically with the original value kept by the TH register

12. **Contents of the register A after execution of the following instructions**
    MOV A, #47H

MOV B, #25H
ADD A, B
DA A

- **a) A = 66H**
- **b) A = 72H**
- **c) A = A8H**
- **d) A = 62H**
  Correct Answer: b) A = 72H

13. **Which of the following is not a valid 8051 instruction?**

- **a) INC DPTR**
- **b) INC A**
- **c) DEC DPTR**
- **d) DEC A**
  Correct Answer: c) DEC DPTR

14. **Which of the following flags are affected by the instruction DIV AB of an 8051 microcontroller?**

- **a) OV, CY, AC**
- **b) OV, AC**
- **c) OV, CY**
- **d) CY, AC**
  Correct Answer: c) OV, CY

15. **What is the content of the memory location specified R0 after the following set of instructions are executed?**
    MOV @R0, #04H
    MOV A, #11H
    XCHD A, @R0

- **a) 01H**
- **b) 10H**
- **c) 04H**
- **d) 40H**
  Correct Answer: a) 01H