| COURSE MATERIAL | |
|---|---|
| SUBJECT | **ELECTRONIC CIRCUIT ANALYSIS (19A04402T)** |
| UNIT | **1** |
| COURSE | **B.TECH** |
| DEPARTMENT | **ELECTRONICS AND COMMUNICATION ENGINEERING** |
| SEMESTER | **II-II** |
| PREPARED BY<br>(Faculty Name/s) | **Dr. DILEEP KUMAR P**<br>**Associate Professor**<br><br>**Mrs. C. PADMA**<br>**Assistant Professor** |

| | |
|---|---|
| Version | **1** |
| PREPARED / REVISED DATE | **01-4-2021** |

TABLE OF CONTENTS – UNIT 5

## 1. Course Objectives

The objectives of this course is to

1. Understand the operation in different regions and determine the operating point of BJT and JFET
2. Analyse the performance of BJT ,JFET and MOSFET in different configurations
3. Design the single stage amplifiers by the requirements of manufacturer

## 2. Prerequisites

Students should have knowledge on

1. Basic operation of BJT, FET and MOSFET

## 3. Syllabus

**UNIT V**

**COMBINATIONAL & SEQUENTIAL CIRCUITS**

**Small Signal Amplifiers Using MOSFETS:** Graphical analysis, Load line and small signal parameters, Small signal equivalent circuit, Small signal analysis of Common source, Common drain, Common gate amplifiers, Comparison of the three basic amplifier configurations, Problem solving.

**JFET Small Signal Amplifiers:** Small signal analysis of common source, common drain, common gate amplifiers, JFET as voltage variable resistor, Problem solving.

**BJT Small Signal Models:** Bipolar linear amplifier, Graphical and ac equivalent circuit, Small signal hybrid-Π equivalent circuit, Hybrid-Π equivalent circuit including the early effect, other small signal parameters and equivalent circuits-h-parameters.

**Small Signal Analysis:** Basic CE amplifier circuit, Circuit with Emitter resistance, ac load line analysis, maximum symmetrical swing, Small signal analysis-input and output impedances, Voltage gain, Current gain of CB, CC amplifiers, Problem solving.

## 4. Course outcomes

1. **Understand** the concepts and equivalent circuit models of small signal amplifiers. (L1)
2. **Analyze** low frequency and high frequency models of BJT and FET. (L3)
3. **Design** BJT and FET amplifier circuits.(L4)
4. **Determine** performance parameters of BJT and FET amplifiers. (L2)

## 5. Co-PO / PSO Mapping

| Machine Tools | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | P10 | PO11 | PO12 | PSO1 | PSO2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 3 | 2 | | | | | | | | | | | 2 | 2 |
| **CO2** | 3 | 2 | 2 | 2 | | | | | | | | | 2 | 2 |
| **CO3** | 3 | 2 | | | | | | | | | | | 2 | 2 |

## 6. Lesson Plan

| Lecture No. | Weeks | Topics to be covered | References |
|---|---|---|---|
| 1 | **1** | Introduction to BJT,JFET and MOSFET | T1, R1 |
| 2 | | Graphical analysis, Load line and small signal parameter | T1, R1 |
| 3 | | Small signal equivalent circuit and Small signal analysis of Common source amplifiers | T1, R1 |
| 4 | | Small signal analysis of Common Drain and Gate amplifiers | T1, R1 |
| 5 | | Comparison of the three basic amplifier configurations, Problem solving. | T1, R1 |
| 6 | **2** | JFET- Small signal analysis of common source amplifiers | T1, R1 |
| 7 | | JFET- Small signal analysis of common Drain and Gate amplifiers | T1, R1 |
| 8 | | JFET as voltage variable resistor, Problem solving | T1, R1 |
| 9 | | **BJT Small Signal Models-** Bipolar linear amplifier, Graphical and ac equivalent circuit | T1, R1 |
| 10 | | Small signal hybrid-Π equivalent circuit | T1, R1 |
| 11 | **3** | Hybrid-Π equivalent circuit including the early effect | T1, R1 |
| 12 | | other small signal parameters and equivalent circuits-h- | T1, R1 |

| | | | |
|---|---|---|---|
| | | parameters | |
| 13 | | **Small Signal Analysis:** Basic CE amplifier circuit | T1, R1 |
| 14 | | **Small Signal Analysis:** CE Circuit with Emitter resistance | T1, R1 |
| 15 | | ac load line analysis and maximum symmetrical swing | T1, R1 |
| 16 | **4** | Small signal analysis-input and output impedances, Voltage gain, Current gain of CB amplifier, Problems | T1, R1 |
| 17 | | Small signal analysis-input and output impedances, Voltage gain, Current gain of CC amplifier, problems | T1, R1 |
| 18 | | Problem solving on unit-I | T1, R1 |

## 7. Activity Based Learning

1. Design single stage amplifiers depending on varying biasing resistors,output coltage,output current

## 8. Lecture Notes

### 1.1 INTRODUCTION

#### DEPLETION-TYPE MOSFETs

The fact that Shockley's equation is also applicable to depletion-type MOSFETs results in the same equation for gm. In fact, the ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs The only difference offered by D-MOSFETs is that VGSQ can be positive for n-channel devices and negative for p-channel units. The result is that gm can be greater than gm0 as demonstrated by the example to follow. The range of rd is very similar to that encountered for JFETs.

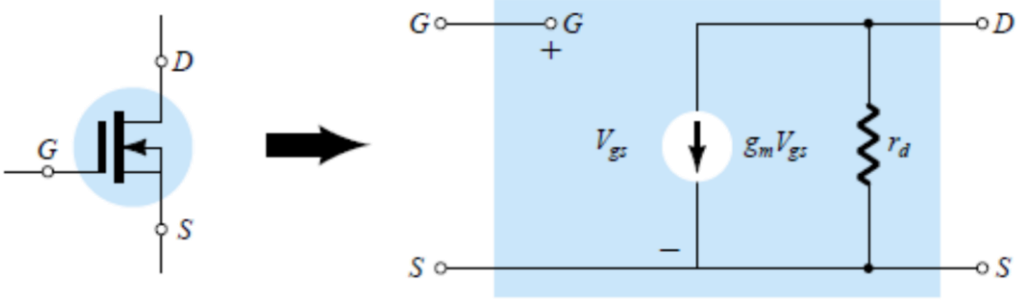


Fig 1.1.: Symbol and small signal model of Depletion MOSFET

**Enhancement MOSFETS**

The enhancement-type MOSFET can be either an n-channel (nMOS) or p-channel (pMOS) device, as shown in Fig.The ac small-signal equivalent circuit of either device is shown in Figure, revealing an open-circuit between gate and drain source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage.

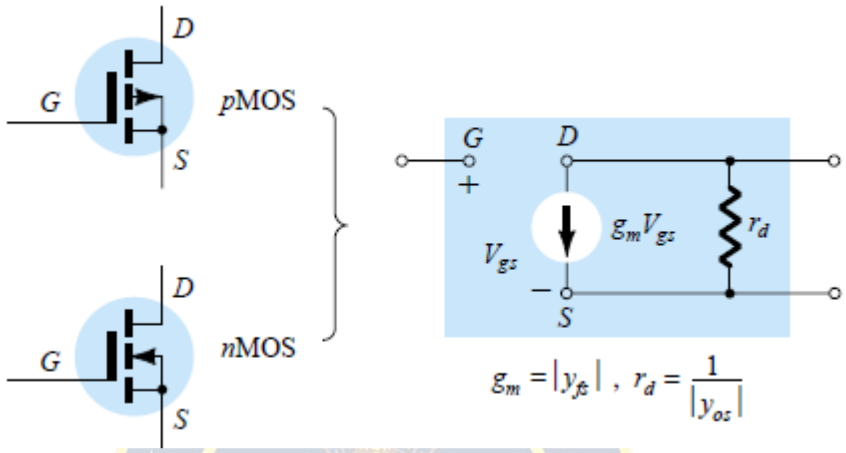
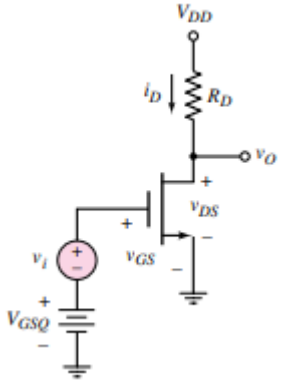



Fig 1.2.: Symbol and small signal model of Depletion MOSFET

**1.2 Graphical analysis, Load line and small signal parameters:**

Figure 1.3 shows an NMOS common-source circuit with a time-varying voltage source in series with the dc source. We assume the time-varying input signal is sinusoidal. Figure 1.4 shows the transistor characteristics, dc load line, and Q-point, where the dc load line and Q-point are functions of VGS, VDD, RD, and the transistor parameters. For the output voltage to be a linear function of the input voltage, the transistor must be biased in the saturation region. (Note that, although we primarily use n-channel, enhancement-mode MOSFETs in our discussions, the same results apply to the other MOSFETs.)



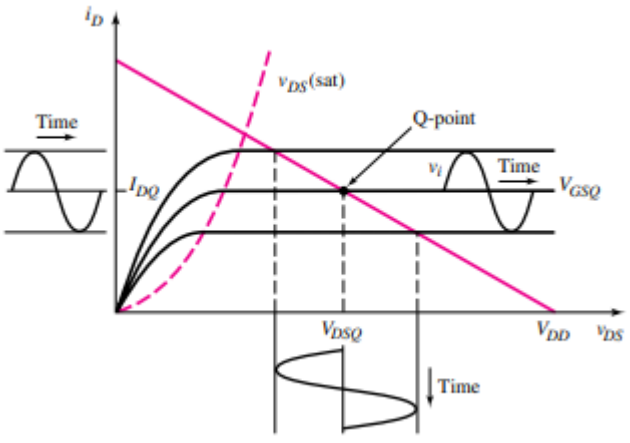



Fig 1.3.: MOSFET with CS Amplifier

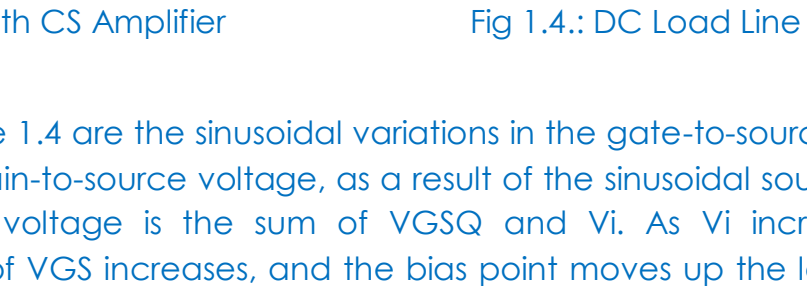


Fig 1.4.: DC Load Line

Also shown in Figure 1.4 are the sinusoidal variations in the gate-to-source voltage, drain current, and drain-to-source voltage, as a result of the sinusoidal source Vi. The total gate-to-source voltage is the sum of VGSQ and Vi. As Vi increases, the instantaneous value of VGS increases, and the bias point moves up the load line. A larger value of rGS means a larger drain current and a smaller value of VDS. For a negative VI (the negative portion of the sine wave), the instantaneous value of VGS decreases below the quiescent value, and the bias point moves down the load line. A smaller VGS value means a smaller drain current and increased value of VDS. Once the Q-point is established, we can develop a mathematical model for the sinusoidal, or small-signal, variations in gate-to-source voltage, drain-to-source voltage, and drain current.

The time-varying signal source ri in Figure 1.3 generates a time- varying component of the gate-to-source voltage. In this case, VGS = Vi, where VGS is the time-varying component of the gate-to-source voltage. For the FET to operate as a linear amplifier the transistor must be biased in the saturation region, and the instantaneous drain current and drain-to-source voltage must also be con- fined to the saturation region

**Transistor Parameters**

The instantaneous gate-to-source voltage is

$$v_{GS} = V_{GSQ} + V_i = V_{GSQ} + V_{gs} \qquad (1.1)$$

Where VGSQ is the dc component and Vgs is the ac component. The instantaneous drain current is

$$i_D = K_n(V_{GS} - V_{TN})^2 \qquad (1.2)$$

Substituting Equation (1.1) into (1.2) produces

$$i_D = K_n[V_{GSQ} + V_{gs} - V_{TN}]^2 = K_n[(V_{GSQ} - V_{TN}) + V_{gs}]^2 \qquad (1.3)$$

**or**

$$i_D = K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})\, V_{gs} + K_n V_{GS}^2 \qquad (1.4)$$

The first term in Equation (1.4) is the dc or quiescent drain current IDQ, the second term is the time-varying drain current component that is linearly related to the signal Vgs, and the third term is proportional to the square of the signal voltage. For a

sinusoidal input signal, the squared term produces undesirable harmonics, or nonlinear distortion, in the output voltage.

To minimize these harmonics, we require

$$\mathbf{Vgs << 2(VGSQ — VTN )} \qquad \mathbf{(1.5)}$$

Which means that the third term in Equation (1.4) will be much smaller than the second term? Equation (1.5) represents the small-signal condition that must be satisfied for linear amplifiers.

Neglecting the term $V_{gs}^2$, we can write Equation (1.4)

$$\mathbf{i_D = I_{DQ} + i_d} \qquad \mathbf{(1.6)}$$

Again, small-signal implies linearity so that the total current can be separated into a dc component and an ac component. The ac component of the drain current is given by

$$\mathbf{id = 2Kn(VGSQ — VTN )Vgs} \qquad \mathbf{(1.7)}$$

The small-signal drain current is related to the small-signal gate-to-source voltage by the trans conductance gm. The relationship is

$$\mathbf{g_m = i_d/V_{gs} = 2K_n(V_{GSQ} — V_{TN} )} \qquad (1.8)$$

The trans conductance is a transfer coefficient relating output current to input voltage and can be thought of as representing the gain of the transistor.

The trans conductance can also be obtained from the derivative

$$\mathbf{g_m = \partial i_D / \partial V_{GS} |\ V_{GS} = V_{GSQ} = const. = 2K_n(V_{GSQ} — V_{TN} )} \qquad (1.9))$$

This can be written

$$gm = 2\sqrt{KnI_{DQ}} \qquad (1.10)$$

The drain current versus gate-to-source voltage for the transistor biased in the saturation region is given in Equation (1.2) and is shown in Figure 1.5. The transconductance gm is the slope of the curve. If the time-varying signal Vgs is sufficiently small, the transconductance gm is a constant. With the Q-point in the saturation region, the transistor operates as a current source that is linearly controlled by Vgs. If the Q-point moves into the non-saturation region, the transistor no longer operates as a linearly controlled current source.

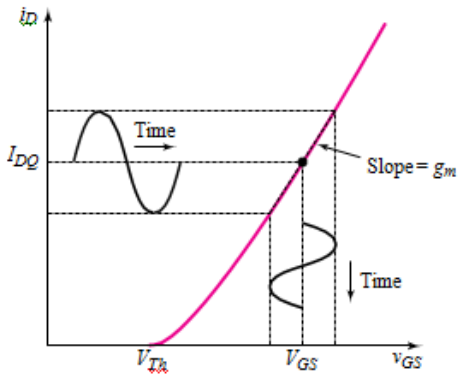



Fig 1.5: Drain current versus gate-to-source voltage characteristics, with superimposed sinusoidal signals

As shown in Equation (1.9), the trans conductance is directly proportional to the conduction parameter Kn, which in turn is a function of the width- to-length ratio. Therefore, increasing the width of the transistor increases the trans conductance, or gain, of the transistor.

**AC Equivalent Circuit of MOSFET:**

From Figure 1.3, we see that the output voltage is

$$V_{DS} = V_O = V_{DD} — i_D R_D \qquad (1.11)$$

Using Equation (1.6), we obtain

$$V_O = V_{DD} — (I_{DQ} + id\ ) R_D = (V_{DD} — I_{DQ}R_D) — id\ R_D \qquad (1.12)$$

The output voltage is also a combination of dc and ac values. The time- varying output signal is the time-varying drain-to-source voltage, or

$$Vo = Vds = —id\ R_D \qquad (1.13)$$

Also, from Equations (6) and (7), we have

$$i_d = g_m V_{gs} \qquad (1.14)$$

In summary, the following relationships exist between the time-varying signals for the circuit. The equations are given in terms of the instantaneous ac values, as well as the phasors. We have

$$Vgs = V_i \quad or \quad Vgs = V_i \qquad (1.15)$$

and

$$id = g_m Vgs \text{ or } I_d = gmVgs \qquad (1.16)$$

Also, $Vds = —id\ RD$ or $Vds = —Id\ RD$ (1.17)

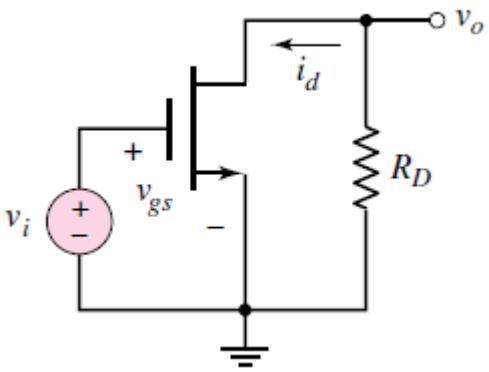



Fig.1.6: AC equivalent circuit of common-source amplifier with NMOS transistor

The ac equivalent circuit in Figure 6.4 is developed by setting the dc sources in Figure 1 equal to zero. The small-signal relationships are given in Equations 1.15,1.16 and 1.17,As shown in Figure 1.3, the drain current, which is composed of ac signals superimposed on the quiescent value, flows through the voltage source VDD. Since the voltage across this source is assumed to be constant, the sinusoidal current produces no sinusoidal voltage component across this element. The equivalent ac impedance is there- fore zero, or a short circuit. Consequently, in the ac equivalent circuit, the dc voltage sources are equal to zero. We say that the node connecting RD and VDD is at signal ground.

### 1.3 Small-Signal Equivalent Circuit of MOSFET:

Now that we have the ac equivalent circuit for the NMOS amplifier circuit, (Figure 4), we must develop a small-signal equivalent circuit for the transistor. Initially, we assume that the signal frequency is sufficiently low so that any capacitance at the gate terminal can be neglected. The input to the gate thus appears as an open circuit, or an infinite resistance. Equation (16) relates the small-signal drain current to the small-signal input voltage, and Equation (1.8) shows that the transconductance $g_m$ is a function of the Q-point. The resulting simplified small-signal equivalent circuit for the NMOS device is shown in Figure 1.7. (The phasor components are in parentheses.)

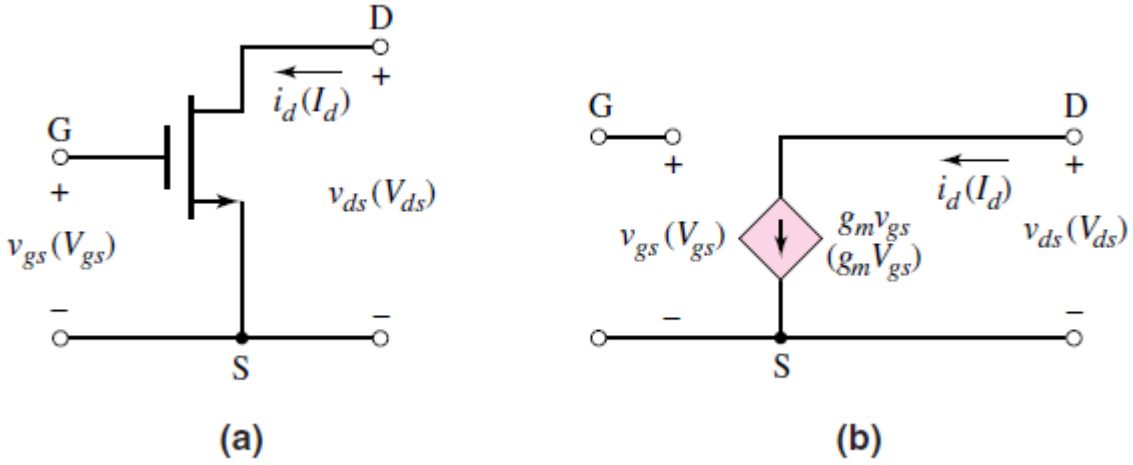



Fig. 1.7 (a) Common-source NMOS transistor with small-signal parameters and

(b) Simplified small-signal equivalent circuit for NMOS transistor

This small-signal equivalent circuit can also be expanded to take into account the finite output resistance of a MOSFET biased in the saturation region.

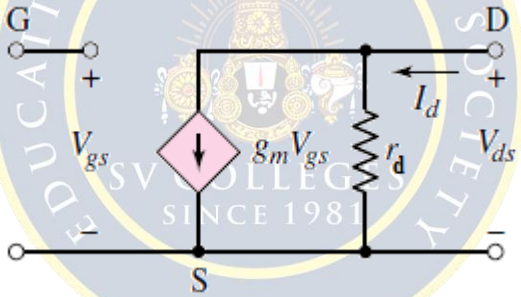



Fig.1.8 Expanded small- signal equivalent circuit, including output resistance, for NMOS transistor

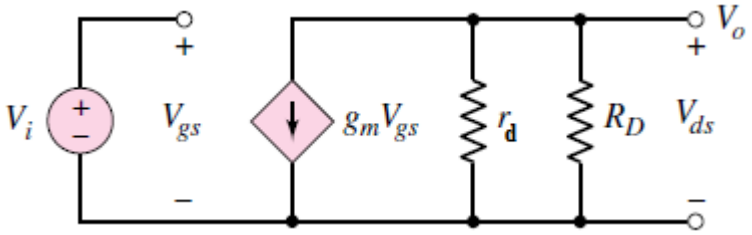



Fig. 1.9 Small-signal equivalent circuit of common source circuit with NMOS transistor model

## 1.4 Common Source Amplifier (CS):

### Small signal analysis of common source amplifier using MOSFET with Fixed bias

Figure 1.10 shows Common Source Amplifier with Fixed Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis.

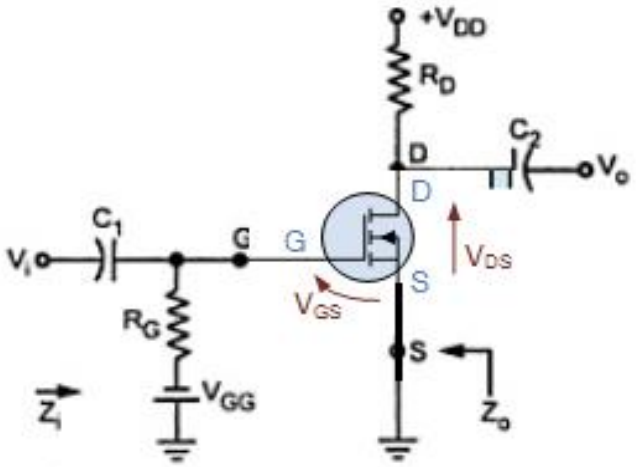



Fig 1.10: CS MOSFET Amplifier with Fixed Bias

The following figure shows the low frequency equivalent model for Common Source Amplifier With Fixed Bias. It is drawn by replacing

- All capacitors and d.c supply voltages with short circuit
- JFET with its low frequency a.c Equivalent circuit

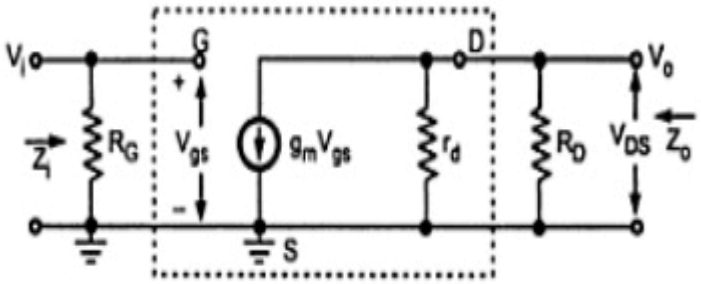



Fig 1.11: Small Signal Model of CS MOSFET Amplifier

### 1. Input impedance ($Z_i$):

Input impedance is the impedance measured at the input terminal. The input impedance can be calculated as

$$Z_i = R_G$$

**2. Output impedance (Zo):**

Output impedance is the impedance measured at the output terminal with input voltage Vi=0. From the figure when Vi=0, Vgs=0 and hence, The output impedance can be calculated as

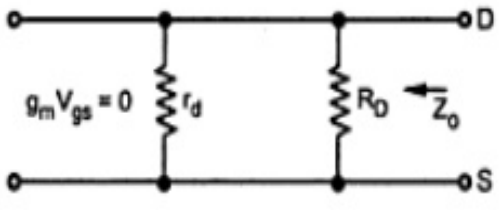



Fig 1.12: Output Equivalent circuit of CS JFET, When Vi=0

$$Z_o = r_d \,||\, R_D$$

Normally rd >> RD [Typical values are rd =35 KΩ and RD=5 KΩ]

Hence $$Z_o = R_D$$

**3. Voltage Gain (AV):** It is defined as the ratio of output voltage to the input voltage.

Where

$$A_V = V_o/V_i = V_{ds}/V_{gs}$$

$$V_o = -I_D (r_d \,||\, R_D),$$

$$\text{Where } I_D = -g_m V_{gs},$$

$$V_o = -g_m V_{gs} (r_d \,||\, R_D),$$

$$V_i = V_{gs}$$

Therefore $$A_V = V_o/V_i$$

$$A_V = -g_m V_{gs} (r_d \,||\, R_D) / V_{gs}$$

$$A_V = -g_m (r_d \,||\, R_D) \quad [\text{Where } r_d >> R_D]$$

$$A_V = -g_m R_D$$

**Table.1.1 Summarize the performance of common source amplifier with fixed bias**

| Parameter | Exact | With rd >> $R_D$ |
|---|---|---|
| $Z_i$ | $Z_i = R_G$ | $Z_i = R_G$ |
| $Z_O$ | $Z_o = rd \| \| R_D$ | $Z_o = R_D$ |
| Av | $-gm (rd \| \| R_D)$ | $-gm R_D$ |

### 1.4.1. Small signal analysis of common source amplifier using MOSFET with voltage divider bias or Bypassed (Rs):

In common source configuration of MOSFET, the inputs is fed to the gate and output is taken at the drain. The resistor R1 and R2 acts as biasing resistors. For AC analysis the source is connected to ground and hence source terminal is connected to both input and output. The circuit diagram of voltage-divider bias for MOSFET is shown in the below figure. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis. The AC equivalent model of the voltage –divider bias circuit of MOSFET can be obtained by shorting the capacitors and grounding the biasing sources as shown in the below figure. Replacing the devices by its small signal model, we get the small signal equivalent circuit is shown below figure.

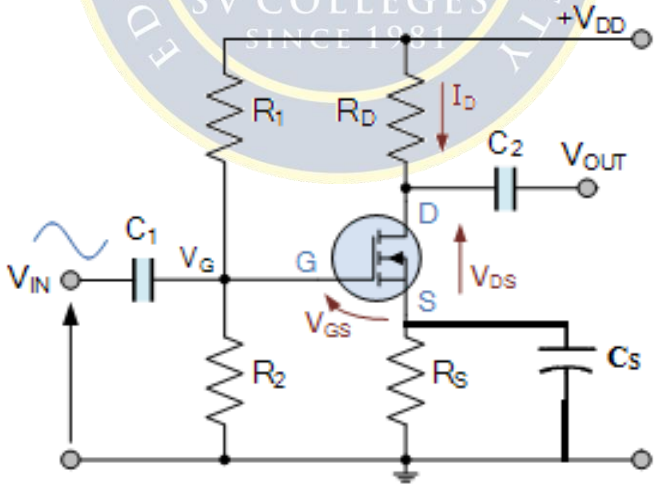



Fig 1.13. Common Source Amplifier using MOSFET

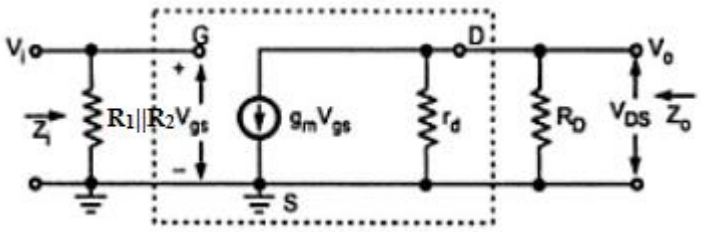



Fig 1.14. Small signal model of Common Source Amplifier with self bias

**1. Input impedance (Zi):**

Input impedance is the impedance measured at the input terminal. The input impedance can be calculated as

$$Z_i = R_G$$

From the small signal model of voltage divider configuration of MOSFET shown in the above figure, where

$$R_G = R_1 \,||\, R_2$$

**2. Output impedance (Zo):**

Output impedance is the impedance measured at the output terminal with input voltage Vi=0. From the figure when Vi=0, Vgs=0 and hence, The output impedance can be calculated as

$$Zo = rd \,||\, RD$$

Normally $r_d >> R_D$ [Typical values are rd =35 KΩ and RD=5 KΩ]

Hence $Zo = RD$

**3. Voltage Gain (AV):** It is defined as the ratio of output voltage to the input voltage. Where

$$A_V = Vo/V_i = V_{ds}/Vgs$$

$$Vo = - I_D (r_d \,||\, R_D),$$

Where $I_D = -g_m Vgs$,

$$Vo = -g_m Vgs, (rd \,||\, RD),$$

$$Vi = Vgs$$

Therefore $A_V = V_o/V_i$

$A_V = -g_m V_{gs} (r_d \| R_D) / V_{gs}$

$A_V = -gm (r_d \| R_D)$ [Where $r_d >> R_D$]

$A_V = - g_m R_D$

**Table.1.2 Summarize the performance of common source amplifier with voltage divider Bias**

| Bypassed RS | | |
|---|---|---|
| Parameter | Exact | With rd >> RD |
| $Z_i$ | $Z_i = R_1 \| \| R_2$ | $Z_i = R_1 \| \| R_2$ |
| $Z_O$ | $Z_o = r_d \| \| R_D$ | $Z_o = R_D$ |
| Av | $-g_m (r_d \| \| R_D)$ | $- g_m R_D$ |

### 1.4.2 Small signal analysis of common source amplifier using MOSFET with voltage divider bias or Un Bypassed (Rs):

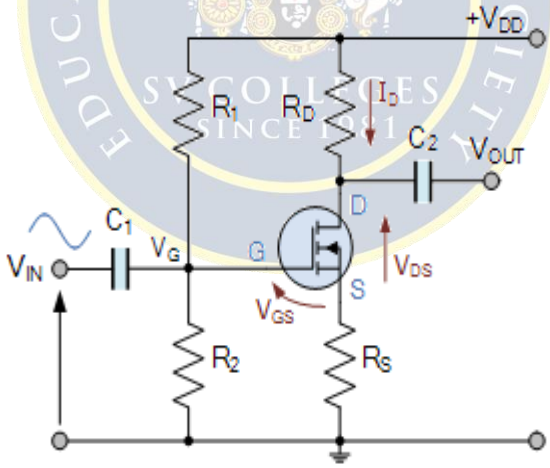



Fig 1.15. MOSFET CS Amplifier with Source Resistor

Now Rs will be the part of low frequency equivalent model as shown in figure 1.16.

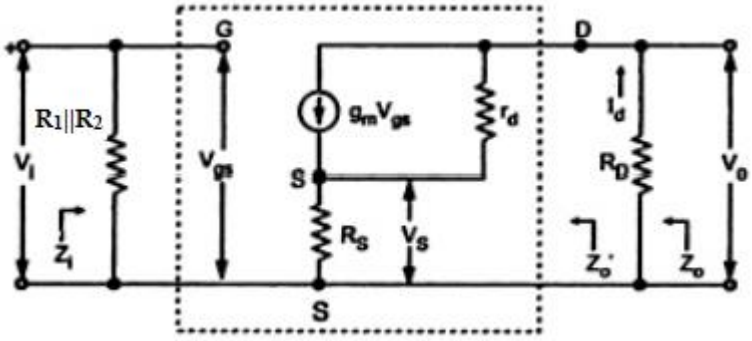



Fig 1.16. Small signal model of Common Source Amplifier with source resistor

**1. Input impedance (Zi):**

Input impedance is the impedance measured at the input terminal. From the small signal model of voltage divider configuration of MOSFET shown in the above figure, where $Z_i = R_G$,

$R_G = R_1 \,||\, R_2$

**2. Output impedance (Zo):**

Output impedance is the impedance measured at the output terminal with input voltage $V_i=0$. From the figure when $V_i=0$, Vgs=0 and hence, The output impedance can be calculated as

$$Zo = Zo' \,||\, R_D$$

$$\text{Where} \quad Zo' = V_O/I_d \text{ at } V_i=0$$

$$Zo = [rd + Rs\,(g_m\, r_d + 1)] \,||\, R_D$$

**3. Voltage Gain ($A_V$):** It is defined as the ratio of output voltage to the input voltage. Where

$$A_V = Vo/V_i = V_{ds}/V_{gs}$$

We Know that $Vo = -I_D R_D$

$$= -g_m (r_d R_D)$$

Therefore $A_V = Vo/V_i$

$$A_V = -[g_m (r_d R_D)] / [\, rd + Rs + R_D + g_m R_s r_d \,]$$

Dividing the numerator and denominator with respect to $r_d$, we get

$$AV = Vo/Vi = - [g_m R_D] / [1 + g_m R_s + (R_s + R_D/ r_d)]$$

If $rd >> Rs + R_D$ We get

$$AV = - g_m R_D/1+ g_m R_s$$

Table.1.3 Summarize the performance of common source amplifier with voltage divider Bias

| Un Bypassed $R_S$ | | |
|---|---|---|
| Parameter | Exact | With rd >> RD |
| $Z_i$ | Zi= R1 \| \|R2 | Zi= $R_1$ \| \|$R_2$ |
| $Z_O$ | [rd + Rs (gm rd + 1)] \| \| RD (or) [rd + Rs (μ+ 1)] \| \| RD | [rd + Rs ($g_m r_d$ + 1)] \| \| $R_D$ (or) [rd + Rs (μ+ 1)] \| \| RD |
| Av | - [$g_m R_D$] / [1 + $g_m$ $R_s$+ (Rs + RD/ rd)] | - $g_m R_D/1+ g_m R_s$ |

## 1.5. Common Drain Amplifier (CD):

### 1.5.1. Small signal analysis of common drain amplifier using MOSFET with self bias:

In this circuit, input is applied between gate and source and output is taken between source and drain.

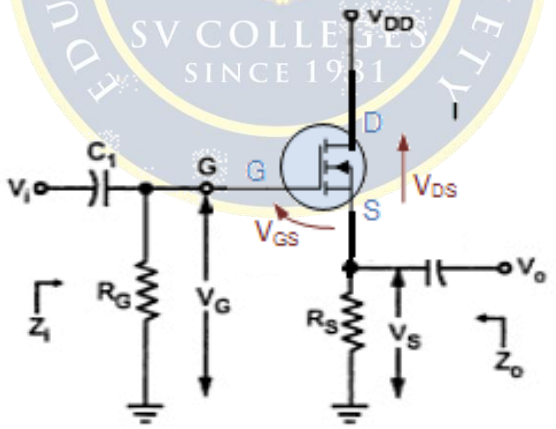



Fig 1.17: Circuit diagram of Common Drain Amplifier with self bias

In this circuit, the source voltage is

$$V_s = V_G + V_{GS}$$

When a signal is applied to the MOSFET gate via $C_1$, $V_G$ varies with the signal. As $V_{GS}$ is fairly constant and $V_s = V_G + V_{GS}$, $V_s$ varies with $V_i$.

The following figure shows the low frequency equivalent model for common drain circuit.

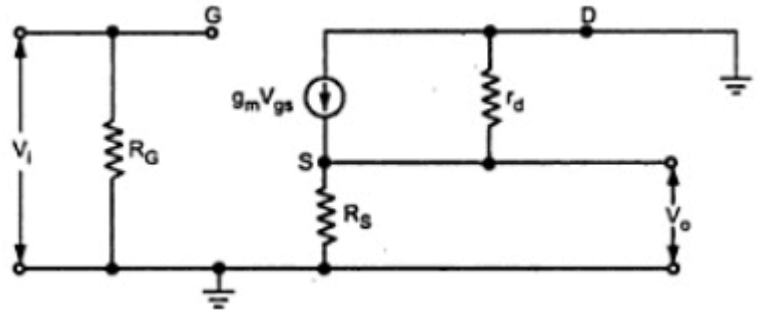



Fig 1.18. Small Signal Model of Common Drain Amplifier

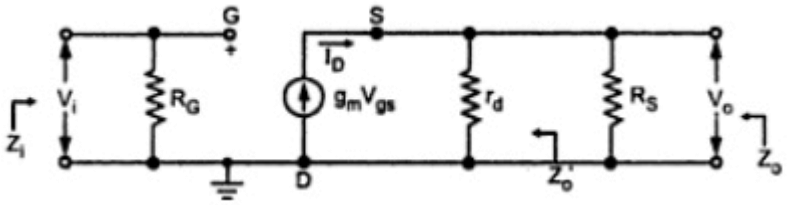



Fig 1.19. Equivalent Circuit of Common Drain Amplifier

**1. Input impedance (Zi):**

Input impedance is the impedance measured at the input terminal. From the small signal model of voltage divider configuration of MOSFET shown in the above figure, where

$$Z_i = R_G , \qquad R_G = R_1 \| R_2$$

**2. Output impedance (Zo):**

Output impedance is the impedance measured at the output terminal with input voltage Vi=0. From the figure when Vi=0, Vgs=0 and hence, The output impedance can be calculated as

$$Zo = Zo' \| R_S$$

**Where** $Zo' = V_O/I_d$ **at** $V_i = 0$

Apply KVL to the outer Loop, we get

$$V_i + Vgs - V_O = 0$$

As $V_i = 0$, $V_{gs} = V_O$

From the equivalent circuit, We can write that

$g_m V_{gs} = I_d$

But $V_{gs} = V_O$ , So

$g_m V_O = I_d$

$Zo' = V_O / g_m V_O$

$Zo' = 1/ gm$

Therefore $Zo = Zo' \,||\, R_S$

$Zo = 1/ g_m \,||\, R_S$

**3. Voltage Gain (AV):** It is defined as the ratio of output voltage to the input voltage.

Where

$A_V = Vo/V_i$

From the equivalent circuit, We can write that

$Vo = -I_D (r_d \,||\, R_S)$ and $I_D = g_m V_{gs}$

Therefore $Vo = - gm\ Vgs\ (rd \,||\, RS)$

But $v_i = -Vgs + V_O$

$= -Vgs + [-gmVgs\ (rd \,||\, Rs)]$

Substitute the value Vi

$A_V = - [gm\ Vgs\ (rd \,||\, Rs)] / [-Vgs( 1 + gm\ (rd \,||\, Rs)]$

$= [gm\ (rd \,||\, Rs)] / [(1 + gm\ (rd \,||\, Rs)]$

If $rd >> Rs$

$A_V = g_m Rs/1+g_m R_S$

If $g_m R_S >> 1$

$A_V = 1$, But always less than one.

Common drain circuit does not provide voltage gain and there is no phase shift between input and output voltages.

Table 1.4 summarizes the performance of common drain amplifier

| Parameter | Exact | rd >> RD |
|---|---|---|
| ZI | RG | RG |
| ZO | (1/gm)\|\|RS | (1/gm)\|\|RS |
| AV | gm(rd\|\|RS)/(1+gm(rd\|\|RS) | gmRS/1+gmRS |

## 1.6. Common Gate Amplifier (CG):

**Small signal analysis of common gate amplifier using MOSFET :**

In this circuit, input is applied between source and gate and output is taken between drain and gate.

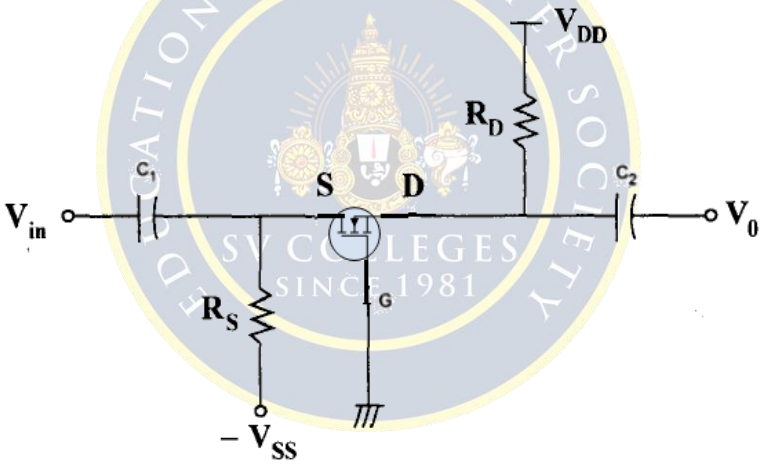



Fig 1.20. Circuit diagram of Common Gate Amplifier

In CG Configuration, gate potential is at constant potential. so, increase in input voltage Vi in positive direction increase the negative gate source voltage. Due to ID reduces, reducing the drop IDRD. Since VD= VDD-IDRD, the reduction in ID results in an increase in output voltage.

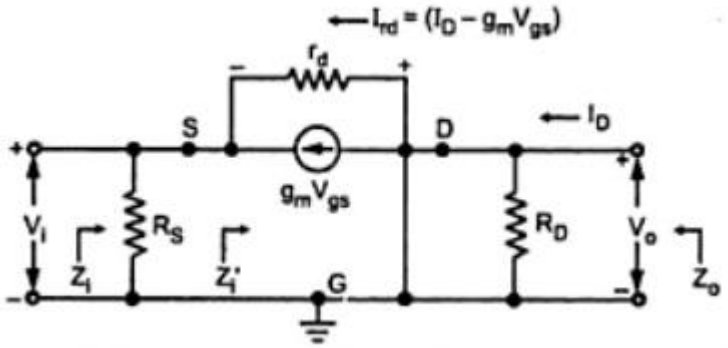



Fig 1.21: Small Signal Model of Common Gate Amplifier

**1. Input impedance (Zi):**

Input impedance is the impedance measured at the input terminal.

$$Z_i = R_S \,||\, Z_i'$$

and $Z_i' = V_i/I$

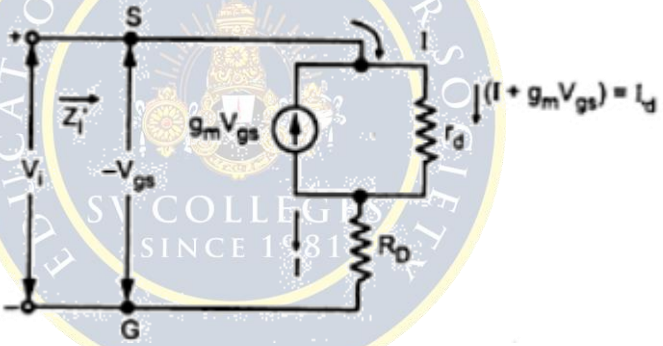



Fig 1.22: Small Signal Model of Common Gate Amplifier for calculating input impedance

$$I_d = I + g_m V_{gs}$$

Therefore $I = I_d\, g_m V_{gs}$

Where $I_d = (V_i - IR_D) / r_d$

After substituting and simplification

$$V_i/I = 1+(R_D/r_d)/[(1/r_d)+g_m)]$$

$$= (r_d+R_D) /(1+ g_m r_d)$$

and $Z_i = Rs \,||\, Z_i' = Rs \,||\, (r_d+R_D)/ (1+ g_m r_d)$

If rd >> $R_D$ and $g_m r_d$ >> 1 than we can write,

$$Z_i = R_S \,||\, (r_d / g_m r_d) = R_S \,||\, (1/g_m)$$

**2. Output impedance (Zo):**

Output impedance is the impedance measured at the output terminal with input voltage $V_i$=0. From the figure when $V_i$=0, $V_{gs}$=0 and hence, The output impedance can be calculated as

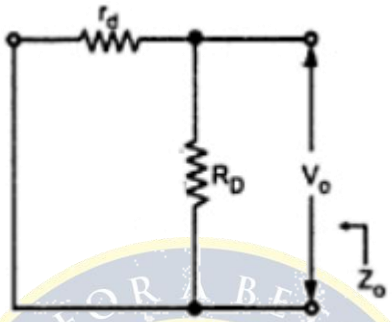



Fig 1.23: Small signal model of common Gate Amplifier for calculating output impedance

It is given by

$$Zo = r_d \,||\, R_D$$

If $r_d >> R_D$

$$Zo = R_D$$

**3. Voltage Gain ($A_V$):** It is defined as the ratio of output voltage to the input voltage. Where

$$A_V = V_o / V_i$$

$$Vo = -I_D R_D$$

$$V_i = -Vgs$$

Using KVL to the Outer Loop, after simplification

$$A_V = Vo/V_i = [(-I_d + R_D)] \,/\, [(-I_d(r_d + R_D)/(1 + g_m r_d)]$$

$$= RD\ (1+gmrd)/(rd + RD)$$

If rd >> RD and gm rd >> 1

$$AV = RD(gmrd)/(rd) = RD\ gm$$

Table 1.5 : summarizes the performance of common gate amplifier

| Parameter | Exact | rd >> RD |
|---|---|---|
| ZI | RS \|\| (rd/gm rd) | RS \|\| (1/gm) |
| ZO | rd \|\| RD | RD |
| AV | RD(gmrd)/(rd) | RD gm |

## 1.7. MOSFET- Comparison of the three basic amplifier configurations,

Table 1.6 : Comparison of Three Basic Amplifier Configurations:

| Parameters | CS (By Passed RS) | CS ( Un bypassed RS) | CD | CG |
|---|---|---|---|---|
| Zi | $Z_i=R_1 \| \| R_2$ | $Z_i=R_1 \| \| R_2$ | $R_G$ | $R_S \| \| (1/g_m)$ |
| $Z_O$ | $Zo= R_D$ | $[rd + Rs (g_m r_d + 1)] \| \| R_D$ (or) $[rd + Rs (\mu + 1)] \| \| R_D$ | $(1/gm) \| \| R_S$ | $R_D$ |
| AV | $-g_m R_D$ | $- g_m R_D/1+ g_m R_S$ | $g_m R_S/1+g_m R_S$ | $R_D\ g_m$ |

## 1.8. JFET-Common Source Amplifier (CD):

### 1.8.1. Small signal analysis of common Source amplifier using JFET with self bias:

In this circuit, input is applied between gate and source and output is taken between source and drain.

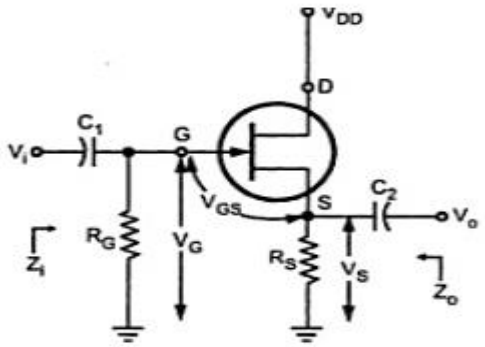



Fig 1.24. Circuit diagram of Common Drain Amplifier with self bias

Now Rs will be the part of low frequency equivalent model as shown in figure 1.16.

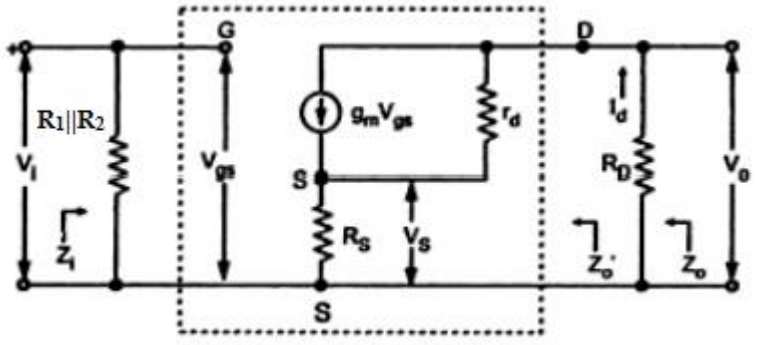



Fig 1.16. Small signal model of Common Source Amplifier with source resistor

**1. Input impedance (Zi):**

Input impedance is the impedance measured at the input terminal. From the small signal model of voltage divider configuration of BJT shown in the above figure, where

$$Z_i = R_G,$$

$$R_G = R_1 \,||\, R_2$$

**2. Output impedance (Zo):**

Output impedance is the impedance measured at the output terminal with input voltage $V_i$=0. From the figure when $V_i$=0, Vgs=0 and hence, The output impedance can be calculated as

$$Zo = Zo' \,||\, R_D$$

$$\text{Where} \quad Zo' = V_O/I_d \text{ at } V_i=0$$

$$Zo = [rd + Rs\,(g_m\, r_d + 1)] \,||\, R_D$$

**3. Voltage Gain ($A_V$):** It is defined as the ratio of output voltage to the input voltage. Where

$$A_V = Vo/V_i = V_{ds}/V_{gs}$$

We Know that $Vo = -I_D\, R_D$

$$= -g_m\,(r_d\, R_D)$$

Therefore $A_V = Vo/V_i$

$$A_V = -[g_m\,(r_d\, R_D)] \,/\, [\, rd + Rs + R_D + g_m\, R_s\, r_d\,]$$

Dividing the numerator and denominator with respect to $r_d$, we get

$$AV = Vo/Vi = - [g_m R_D] / [1 + g_m R_s + (R_s + R_D/ r_d)]$$

If $rd >> Rs + R_D$ We get

$$AV = - g_m R_D/1+ g_m R_s$$

Table.1.3 Summarize the performance of common source amplifier with voltage divider Bias

| Un Bypassed $R_S$ | | |
|---|---|---|
| Parameter | Exact | With rd >> RD |
| $Z_i$ | Zi= R1 \| \|R2 | Zi= $R_1$ \| \|$R_2$ |
| $Z_O$ | [rd + Rs (gm rd + 1)] \| \| RD<br>(or) [rd + Rs (μ+ 1)] \| \| RD | [rd + Rs ($g_m r_d$ + 1)] \| \| $R_D$<br>(or) [rd + Rs (μ+ 1)] \| \| RD |
| Av | - [$g_m R_D$] / [1 + $g_m R_s$+ (Rs + RD/ rd)] | - $g_m R_D$/1+ $g_m R_s$ |

## 1.9. Common Gate Amplifier (CG):

### Small signal analysis of common gate amplifier using JFET :

In this circuit, input is applied between source and gate and output is taken between drain and gate.

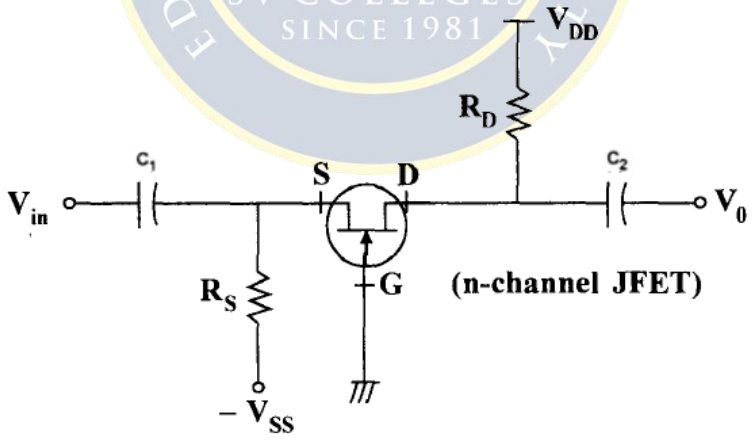



Fig 1.27. Circuit diagram of Common Gate Amplifier

In CG Configuration, gate potential is at constant potential. so, increase in input voltage Vi in positive direction increase the negative gate source voltage. Due to ID reduces, reducing the drop IDRD. Since VD= VDD-IDRD, the reduction in ID results in an increase in output voltage.

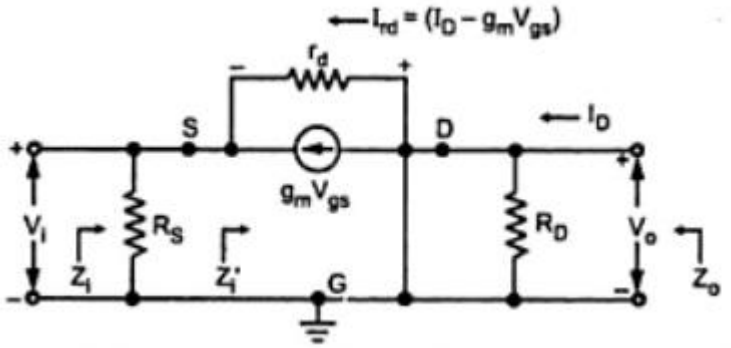



Fig 1.28. Small Signal Model of Common Gate Amplifier

**1. Input impedance (Zi):**

Input impedance is the impedance measured at the input terminal.

$$Z_i = R_S \| Z_i'$$

and $Z_i' = V_i/I$

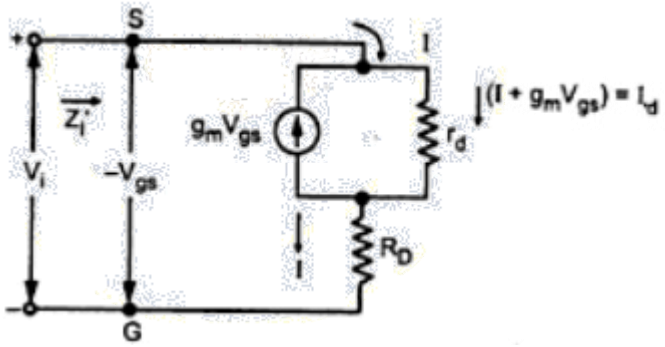



Fig 1.28. Small Signal Model of Common Gate Amplifier for input impedance

$$Id = I + g_m V_{gs}$$

$$\text{Therefore } I = I_d\, g_m V_{gs}$$

Where $Id = (V_i - IR_D) / r_d$

After substituting and simplification

$V_i/I = 1+(R_D/r_d)/[(1/r_d)+g_m)]$

$= (r_d+R_D) /(1+g_m r_d)$

and $Z_i = R_S \,||\, Z_i' = R_s \,||\, (r_d + R_D)/(1 + g_m r_d)$

If rd >> RD and gm rd >> 1 than we can write,

$$Z_i = R_S \,||\, (r_d / g_m r_d) = R_S \,||\, (1/g_m)$$

**2. Output impedance (Zo):**

Output impedance is the impedance measured at the output terminal with input voltage $V_i$=0. From the figure when $V_i$=0, $V_{gs}$=0 and hence, The output impedance can be calculated as

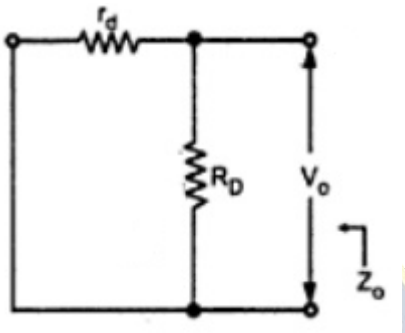



Fig 1.29. Small Signal Model of Common Gate Amplifier for output impedance

It is given by

$$Zo = r_d \,||\, R_D$$

If $r_d >> R_D$

$$Zo = R_D$$

**3. Voltage Gain ($A_V$):** It is defined as the ratio of output voltage to the input voltage. Where

$$A_V = V_o/V_i$$

$$V_o = -I_D R_D$$

$$Vi = -Vgs$$

Using KVL to the Outer Loop, after simplification

$$A_V = V_o/V_i = [(-I_d + R_D)] / [(-I_d(r_d + R_D)/(1+g_m r_d)]$$

$$= R_D (1+g_m r_d)/(r_d + R_D)$$

If $r_d >> R_D$ and $g_m r_d >> 1$

$$A_V = R_D(g_m r_d)/(r_d) = R_D g_m$$

Table 1.8: summarizes the performance of common gate amplifier

| Parameter | Exact | $r_d >> R_D$ |
|---|---|---|
| $Z_I$ | $R_S \mid\mid (rd/gm\ rd)$ | $R_S \mid\mid (1/gm)$ |
| $Z_O$ | $rd \mid\mid R_D$ | $R_D$ |
| $A_V$ | $R_D(g_m r_d)/(rd)$ | $R_D\ gm$ |

## 1.10. Common Drain Amplifier (CD):

### Small signal analysis of common drain amplifier using JFET with self bias

In this circuit, input is applied between gate and source and output is taken between source and drain.

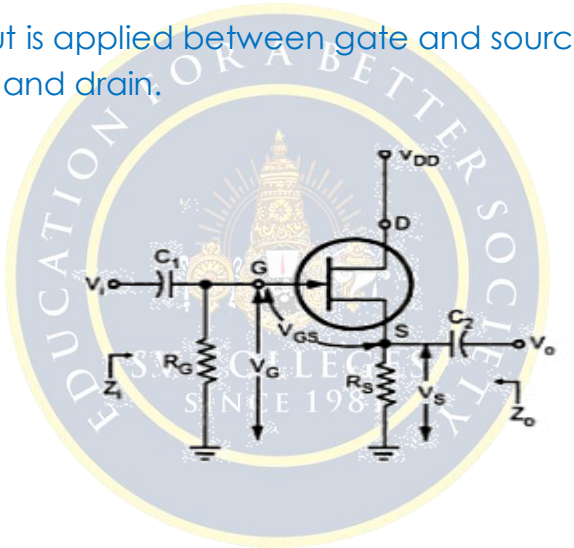



Fig 1.30. Circuit diagram of Common Drain Amplifier with self bias

In this circuit, the source voltage is

$$V_s = V_G + V_{GS}$$

When a signal is applied to the JFET gate via $C_1$, $V_G$ varies with the signal. As $V_{GS}$ is fairly constant and $Vs = V_G + V_{GS}$, Vs varies with $V_i$.

The following figure shows the low frequency equivalent model for common drain circuit.

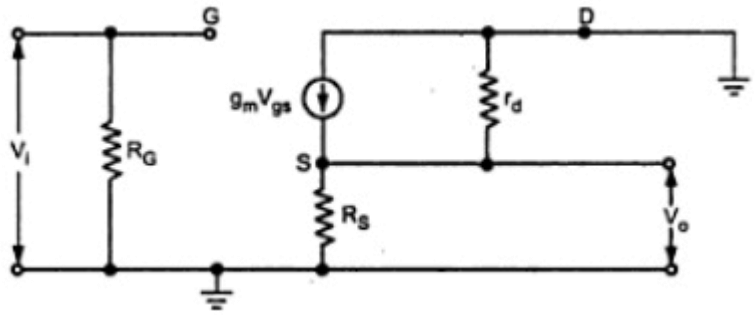



Fig 1.31. Small Signal Model of Common Drain Amplifier

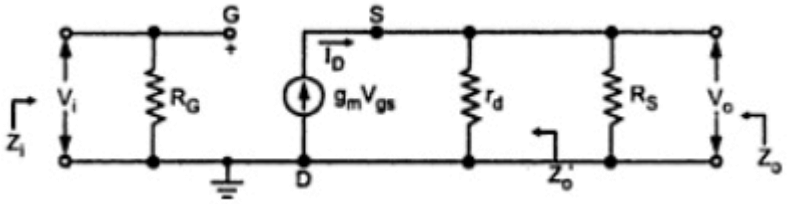



Fig 1.32. Equivalent Circuit of Common Drain Amplifier

**1. Input impedance (Zi):**

Input impedance is the impedance measured at the input terminal. From the small signal model of voltage divider configuration of MOSFET shown in the above figure, where

$$Z_i = R_G \text{ , } \quad R_G = R_1 \| R_2$$

**2. Output impedance (Zo):**

Output impedance is the impedance measured at the output terminal with input voltage Vi=0. From the figure when Vi=0, Vgs=0 and hence, The output impedance can be calculated as

$$Z_o = Z_o' \| R_S$$

**Where** $Z_o' = V_O/I_d$ **at** $V_i = 0$

Apply KVL to the outer Loop, we get

$$V_i + V_{gs} - V_O = 0$$

As $V_i = 0$, $V_{gs} = V_O$

From the equivalent circuit, We can write that

$g_m V_{gs} = I_d$

But $V_{gs} = V_O$ , So

$g_m V_O = I_d$

$Zo' = V_O / g_m V_O$

$Zo' = 1 / gm$

Therefore $Zo = Zo' \,||\, R_S$

$Zo = 1 / g_m \,||\, R_S$

**3. Voltage Gain (AV):** It is defined as the ratio of output voltage to the input voltage.

Where

$A_V = Vo/V_i$

From the equivalent circuit, We can write that

$Vo = -I_D (r_d \,||\, R_S)$ and $I_D = g_m V_{gs}$

Therefore $Vo = - gm\ Vgs\ (rd \,||\, RS)$

But $v_i = -Vgs + V_O$

$= -Vgs + [-gmVgs\ (rd \,||\, Rs)]$

Substitute the value Vi

$A_V = - [gm\ Vgs\ (rd \,||\, Rs)] / [-Vgs(\ 1 + gm\ (rd \,||\, Rs)]$

$= [gm\ (rd \,||\, Rs)] / [(1 + gm\ (rd \,||\, Rs)]$

If $rd >> Rs$

$A_V = g_m Rs / 1 + g_m R_S$

If $g_m R_S >> 1$

$A_V = 1$, But always less than one.

Common drain circuit does not provide voltage gain and there is no phase shift between input and output voltages.

Table 1.4 summarizes the performance of common drain amplifier

| Parameter | Exact | rd >> RD |
|---|---|---|
| ZI | RG | RG |
| ZO | $(1/g_m)\|\|R_S$ | (1/gm)\|\|RS |
| AV | gm(rd\|\|RS)/(1+gm(rd\|\|RS) | $g_mR_S/1+gmR_S$ |

## 1.11. **JFET as a Voltage Variable Resistor (VVR)**

Let us consider the drain characteristics of FET as shown in the fig.

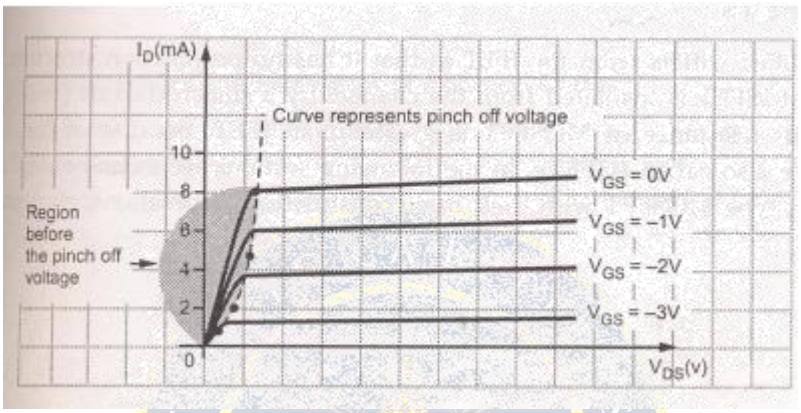



Fig 1.37. Drain Characteristics

In this characteristic we can see that in the region before pinch off voltage, drain characteristics are linear, i.e. FET operation is linear. In this region the FET is useful as a voltage controlled resistor, i.e. the drain to source resistance is controlled by the bias voltage VGS.( In this region only FET behaves like an ordinary resistor This resistances can be varied by VGS ) .The operation of FET in the region is useful in most linear applications of FET. In such an application the FET is also referred to as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

The drain to source conductance (rd)

gd= for small values of VDS which may also be expressed as $g_d=g_{d0}$(1- ) 1/2) Where gd0 is the value of drain conductance When the variation of the rd with VGS can be closely approximated by the expression rd= ) Where ro = drain resistance at zero gate bias. K = a constant, dependent upon FET type.

FET is a device that is usually operated in the constant-current portion of its output characteristics. But if it is operated on the region prior to pinch-off (that is where VDS is small, say below 100 mV), it will behave as a voltage-variable resistor (WE). It is due to the fact that in this region drain-to-source resistance RDS can be controlled by varying the bias voltage VGS. In such applications the FET is also

referred to as a voltage-variable resistor or volatile dependent resistor. It finds applications in many areas where this property is useful.
Figure shows the drain characteristic curves for a 2N 5951 in the ohmic region (i.e. for low VDS). From the characteristic curve it can be seen that RDS varies with VGS. For example, when VGS = 0, RDS = 133 ohm and when VGS = – 2 V, RDS = 250 ohm. Because of this a JFET operating in the ohmic region with small ac signals acts as a voltage-controlled resistance.
Note that the drain curves shown in figure extend on both sides of the origin. This means that a JFET can be employed as a voltage-variable resistor for small ac signals, typically those less than 100 mV. When it is employed in this way, it does not require a dc drain voltage from the supply. All that is required is an ac input signal.

## 1.12. SINGLE STAGE AMPLIFIERS- BJT

### Introduction

V-I characteristics of an active device such as BJT are non-linear. The analysis of a non- linear device is complex. Thus to simplify the analysis of the BJT, its operation is restricted to the linear V-I characteristics around the Q-point i.e. in the active region. This approximation is possible only with small input signals. With small input signals transistor can be replaced with small signal linear model. This model is also called small signal equivalent circuit.

Two –Port Devices and Network Parameters

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in fig. 1.

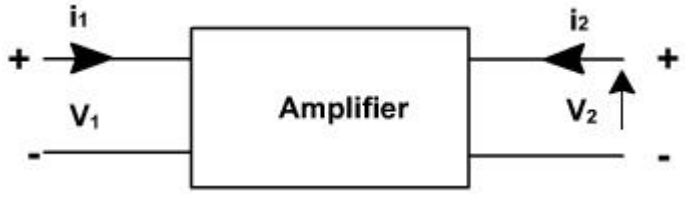



Fig. 1.38 Two port Network

A two-port network is represented by four external variables: voltage V1 and current I1 at the input port, and voltage V2 and current I2 at the output port, so that the

two-port network can be treated as a black box modeled by the relationships between the four variables,V1,V2, I1,I2 . Out of four variables two can be selected as are independent variables and two are dependent variables.The dependent variables can be expressed interns of independent variables. This leads to various two port parameters out of which the following three are important:

1. Impedance parameters (z-parameters)
2. Admittance parameters (y-parameters)
3. Hybrid parameters (h-parameters)
4. z-parameters

**Y-parameters**

A two-port network can be described by Y-parameters as

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

Input admittance with output port short circuited

$$y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0}$$

Reverse transfer admittance with input port short circuited

$$y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0}$$

Forward transfer admittance with output port short circuited

$$y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0}$$

Output admittance with input port short circuited

$$y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0}$$

**Hybrid parameters (h-parameters)**

If the input current I1 and output voltage V2 are taken as independent variables, the dependent variables V1 and I2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Where $h_{11}$, $h_{12}$, $h_{21}$, $h_{22}$ are called as hybrid parameters.

Input impedence with o/p port short circuited

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0}$$

Forward voltage transfer ratio with o/p port short circuited

$$h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0}$$

output impedence with i/p port open circuited

$$h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$$

## 1.13. THE HYBRID MODEL FOR TWO PORT NETWORK:

Based on the definition of hybrid parameters the mathematical model for two pert networks known as h-parameter model can be developed. The hybrid equations can be written as:

$$V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

(The following convenient alternative subscript notation is recommended by the IEEE Standards:

i=11= input o = 22 = output

f =21 = forward transfer r = 12 = reverse transfer)

We may now use the four h parameters to construct a mathematical model of the device of Fig.(1). The hybrid circuit for any device indicated in Fig.(2). We can verify that the model of Fig.(2) satisfies above equations by writing Kirchhoff's voltage and current laws for input and output ports.

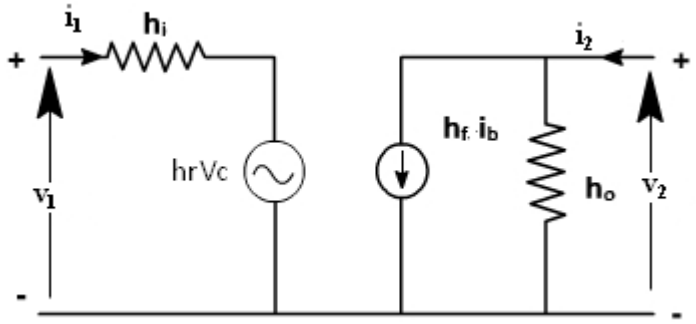



Fig 1.39 H-Parameter model

If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. $h_{fe}$ ,$h_{ib}$ are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in Figure 1.40.

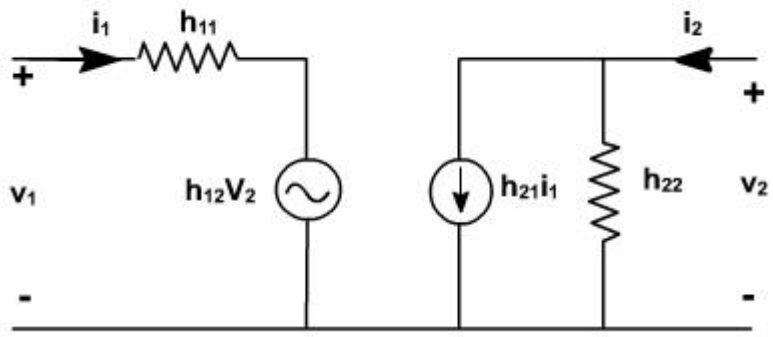



Fig 1.40 Equivalent Representation of H-Parameter model

**TRANSISTOR HYBRID MODEL:**

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in **41**. The variables, iB, iC ,vC, and vB represent total instantaneous currents and voltages iB and vC can be taken as independent variables and vB, IC as dependent variables.

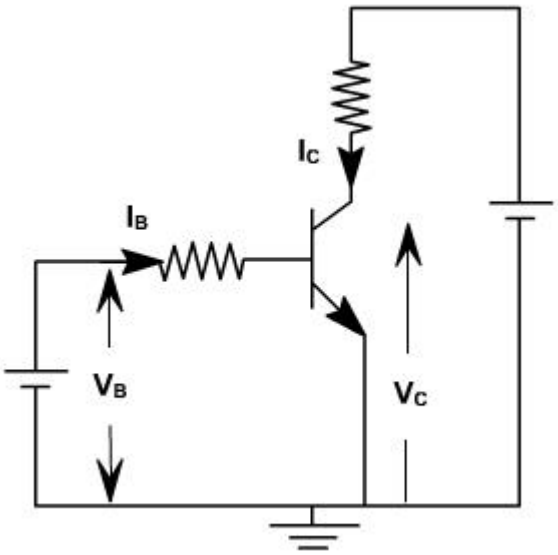



Fig. 1.41 CE Configuartion

VB = f1 (iB ,vC )

IC = f2 (iB ,vC).

Using Taylor 's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} \Delta v_C$$

$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The Δ vB, Δ vC, Δ iB, Δ iC represent the small signal (incremental) base and collector current and voltage and can be represented as vB, iC, iB ,vC

$$\therefore v_b = h_{ie}\, i_B + h_{re}\, v_C$$
$$i_C = h_{fe}\, i_B + h_{oe}\, v_b$$

where

$$h_{ie} = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_c} = \left.\frac{\partial v_B}{\partial i_B}\right|_{v_c}; \qquad h_{re} = \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$
$$h_{fe} = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_c} = \left.\frac{\partial i_C}{\partial i_B}\right|_{v_c}; \qquad h_{oe} = \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

**The model for CE configuration is shown in** fig. 4

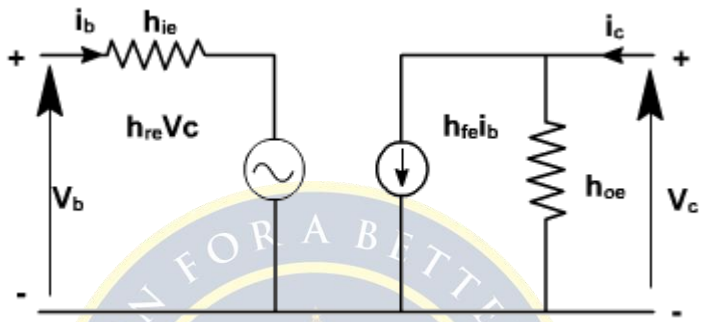



Fig. 1.42 H-parameter model of CE Configuration

To determine the four h-parameters of transistor amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. Fig. 5, shows the output characteristics of CE amplifier.

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{b2} - i_{b1}}$$

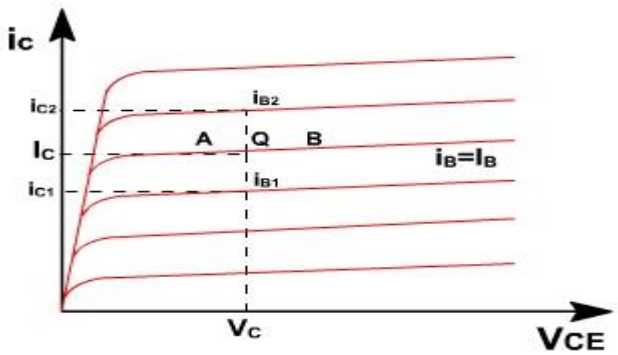



Fig. 1.43 output characteristics of CE Configuration

The current increments are taken around the quiescent point Q which corresponds to iB = IB and to the collector voltage VCE = VC

$$h_{oe} = \frac{\partial i_C}{\partial V_C}\bigg|_{i_B}$$

The value of hoe at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \frac{\Delta V_B}{\Delta i_B}\bigg|_{V_C}$$

hie is the slope of the appropriate input on Fi, at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \frac{\Delta V_B}{\Delta V_C}\bigg|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

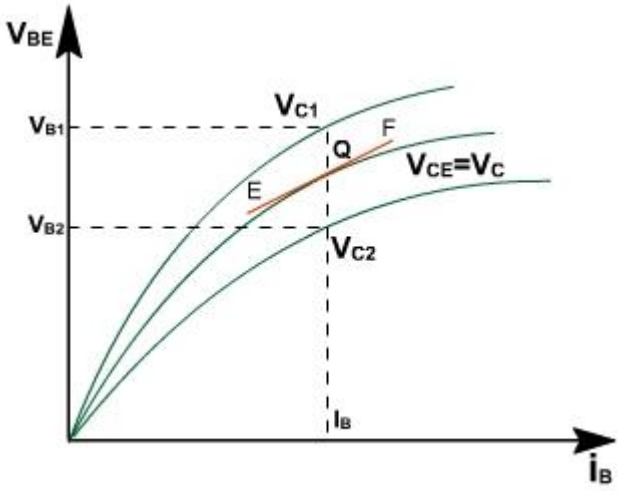



Fig. 1.44 Determination of operating point for CE Configuration

A vertical line on the input characteristic represents constant base current. The parameter hre can be obtained from the ratio (VB2– V B1 ) and ($V_{C2}$– $V_{C1}$ ) for at Q.

Typical CE h-parameters of transistor 2N1573 are given below:

hie = 1000 ohm.
hre = 2.5 * 10 –4
hfe = 50
hoe = 25 □□A / V

## 1.14. ANALYSIS OF A TRANSISTOR AMPLIFIER USING H-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in fig. 1.45 and to bias the transistor properly.

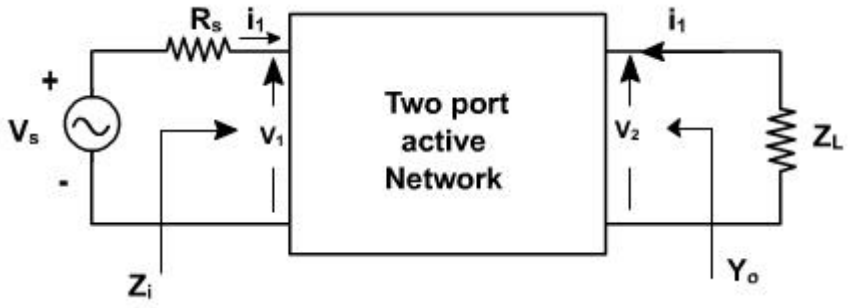



Fig. 1.45 Transistor Two port Representation

Consider the two-port network of CE amplifier. RS is the source resistance and ZL is the load impedence h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in 1.46. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedence, voltage gain, and output impedence.

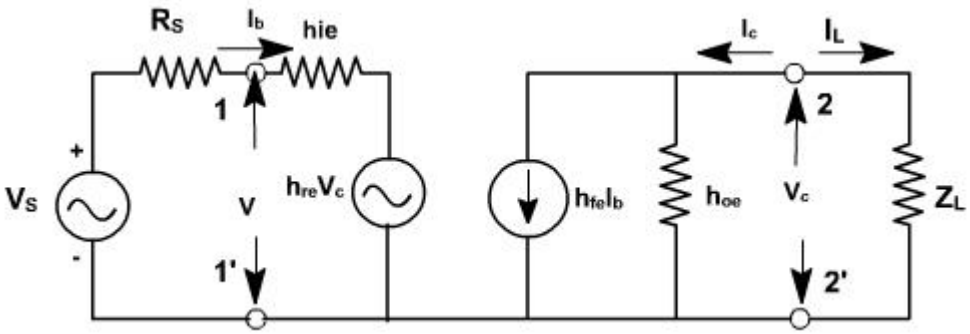



Fig. 1.46 Transistor h-parameter equivalent circuit

### Current gain:

For the transistor amplifier stage, Ai is defined as the ratio of output to input currents.

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

For transistor amplifier the current gain Ai is defined as the ratio of output current to input current, i.e,

From the circuit of Fig

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$

$$I_2 = h_f I_1 - I_2 Z_L \, ho$$

$$I_2 + I_2 Z_L \, h_o = h_f I_1$$

$$I_2 ( 1 + Z_L \, h_o) = h_f I_1$$

$$A_I = -I_2 / I_1 = - h_f / ( 1 + Z_L \, h_o)$$

Therefore,

$$A_i = - h_f / ( 1 + Z_L \, h_o)$$

**Input impedence:**

The impedence looking into the amplifier input terminals ( 1,1' ) is the input impedance $Z_I$

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

**Voltage gain:**

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_C}{V_b} = -\frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

**Output Admittance:**

It is defined as the ratio of output current to output voltage by considering source voltage is equal to zero volts.

$$Y_0 = \left.\frac{I_c}{V_c}\right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe}\frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $\quad R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0.$

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re}\, h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance ($R_S$) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i\right)$$

$$= A_V \cdot \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_i Z_L}{Z_i + R_s}$$

$A_v$ is the voltage gain for an ideal voltage source ($R_S = 0$).

**Voltage Amplification Factor(Avs) taking into account the resistance (Rs) of the source**

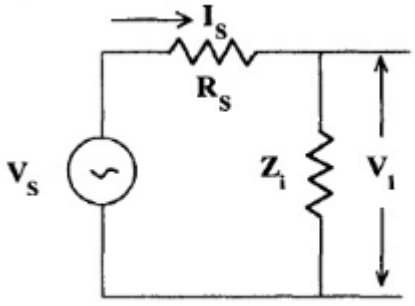



Fig. 1.47 Thevenin's Equivalent Input Circuit

This overall voltage gain Avs is given by

$$Avs = V_2 / V_S = V_2V_1 / V_1V_S = Av\ V_1/ V_S$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 1.47

$$V_1 = V_S\ Z_i / (Z_i + R_S)$$

$$V_1 / V_S = Z_i / (Z_i + R_S)$$

Then, $Avs = Av\ Z_i / (Z_i + R_S)$

Substituting $Av = A_iZ_L / Z_i$

$$Avs = A_i\ Z_L / (Z_i + R_S)$$

$$Avs = A_i\ Z_L\ R_S / (Z_i + R_S)\ RS$$

**$Avs = A_i\ Z_L / (Z_i + R_S)$**

**Current Amplification (Ais) taking into account the sourse Resistance(RS)**

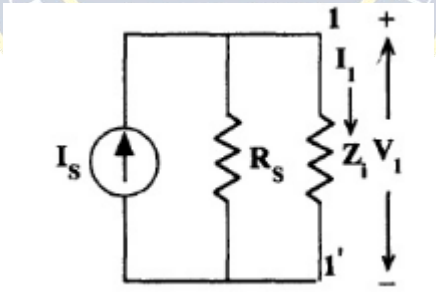



Fig. 1.48 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of Ais is shown in Fig. 1.48

**Overall Current Gain,** $Ais = -I_2 / I_S = - I_2I_1 /I_1\ I_S = Ai\ I_1/I_S$

From Fig. 1.7 $I_1= I_S\ R_S / (R_S + Z_i)$

$$I_1 / I_S = R_S / (R_S + Z_i)$$

and hence,

$$A_{is} = A_i R_S / (R_S + Z_i)$$

### Operating Power Gain (AP)

The operating power gain AP of the transistor is defined as

$A_P = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = Ai\ A_i Z_L / Z_i$

$$A_P = A_i^2 (ZL / Zi)$$

### H-parameters

To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture data sheet. The manufacture data sheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example fig. 4 hrc in terms of CE parameter can be obtained as follows.

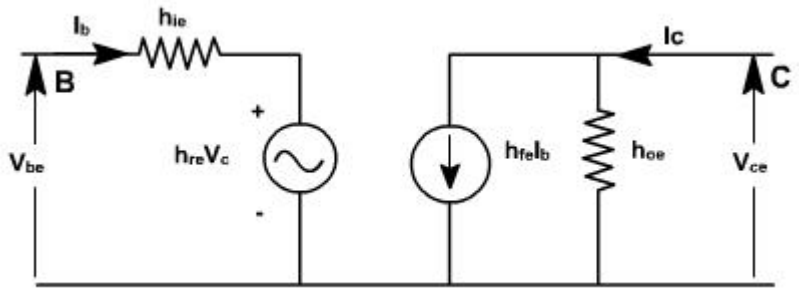



**Fig. 1.49 H-parameter Equivalent Circuit**

For CE transistor configuaration

Vbe = hie Ib + hre Vce

Ic = h fe Ib + hoe Vce

The circuit can be redrawn like CC transistor configuration as shown in fig. 5.

Vbc = hie Ib + hrc Vec

Ic = hfe Ib + hoe Vec

## Hybrid model for transistor in three different configurations

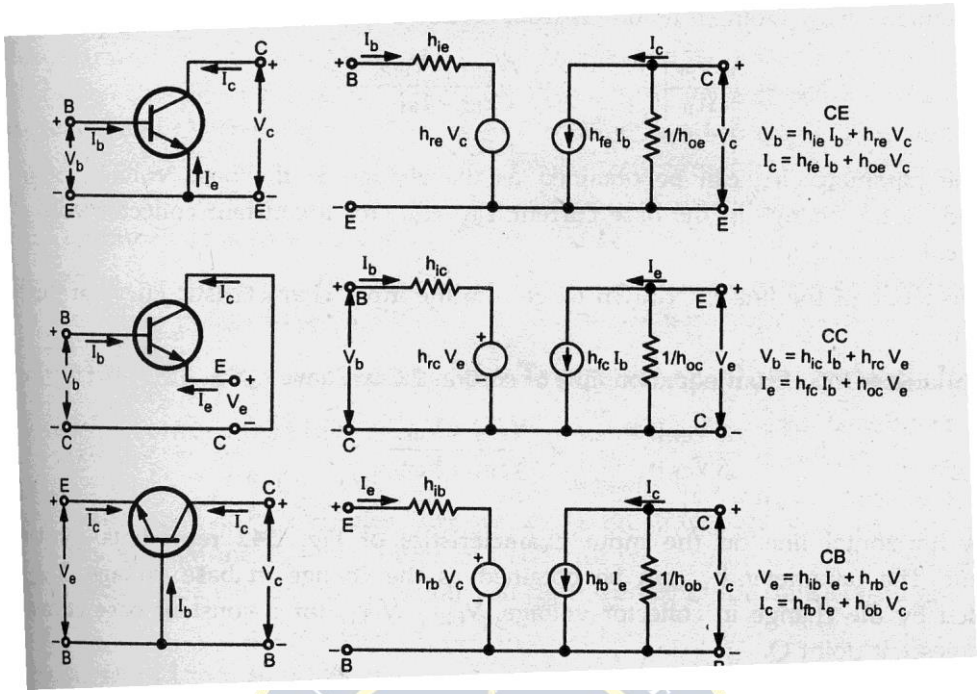



**Fig. 1.50- H-parameter model for all configurations**

Table 1.6: Typical h-parameter values for a transistor

| Parameter | CE | CC | CB |
|---|---|---|---|
| hi | 1100 Ω | 1100 Ω | 22 Ω |
| hr | 2.5 × 10-4 | 1 | 3 × 10-4 |
| hf | 50 | -51 | -0.98 |
| ho | 25 μA/V | 25 μA/V | 0.49 μA/V |

Table 1.7: Small Signal analysis of a transistor amplifier

| $A_i = - h_f / ( 1+ Z_L h_o)$ | $Av = A_i Z_L / Z_i$ |
|---|---|
| $Zi = h_i + h_r A_I Z_L = h_i - h_f h_r / (YL + ho)$ | **$Avs = A_i Z_L / ( Z_i + R_S)$** |

| | |
|---|---|
| $Y_o = h_o - h_f h_r/(R_S + h_i) = 1/Z_o$ | $\mathbf{A_{is} = A_i R_S / (R_S + Z_i)}$ |

### Comparison of Transistor Amplifier Configuration

The characteristics of three configurations are summarized in Table .Here the quantities $A_i$,Av,Ri,Ro and AP are calculated for a typical transistor whose h-parameters are given in table .The values of RL and Rs are taken as 3KΩ.

Table 1.8: Performance schedule of three transistor configurations

| Quantity | CB | CC | CE |
|---|---|---|---|
| $A_I$ | 0.98 | 47.5 | -46.5 |
| $A_V$ | 131 | 0.989 | -131 |
| $A_P$ | 128.38 | 46.98 | 6091.5 |
| $R_i$ | 22.6 Ω | 144 kΩ | 1065 Ω |
| $R_o$ | 1.72 MΩ | 80.5 Ω | 45.5 kΩ |

The values of current gain, voltage gain, input impedance and output impedance calculated as a function of load and source impedances

### Characteristics of Common Base Amplifier

(i) Current gain is less than unity and its magnitude decreases with the increase of load resistance RL,

(ii) Voltage gain AV is high for normal values of RL,

(iii) The input resistance Ri is the lowest of all the three configurations, and

(iv) The output resistance Ro is the highest of all the three configurations.

Applications The CB amplifier is not commonly used for amplification purpose.

It is used for

(i) Matching a very low impedance source

(ii) As a non inverting amplifier to voltage gain exceeding unity.

(iii) For driving a high impedance load.

(iv) As a constant current source.

**Characteristics of Common Collector Amplifier**

(i) For low RL (< 10 kΩ), the current gain Ai is high and almost equal to that of a CE amplifier.

(ii) The voltage gain AV is less than unity.

(iii) The input resistance is the highest of all the three configurations.

(iv) The output resistance is the lowest of all the three configurations.

Applications The CC amplifier is widely used as a buffer stage between a high impedance source and a low impedance load.

**Characteristics of Common Emitter Amplifier**

(i) The current gain Ai is high for RL < 10 kΩ.

(ii) The voltage gain is high for normal values of load resistance RL.

(iii) The input resistance Ri is medium.

(iv) The output resistance Ro is moderately high.

Applications: CE amplifier is widely used for amplification

**Simplified common emitter hybrid model:**

In most practical cases it is appropriate to obtain approximate values of A V , A i etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. Fig. 4 shows the CE amplifier equivalent circuit in terms of h-parameters Since 1 / hoe in parallel with RL is approximately equal to RL if 1 / hoe >> RL then hoe may be neglected. Under these conditions.

$$Ic = hfe\ IB\ .$$

$$hre\ vc = hre\ Ic\ RL = hre\ hfe\ Ib\ RL\ .$$

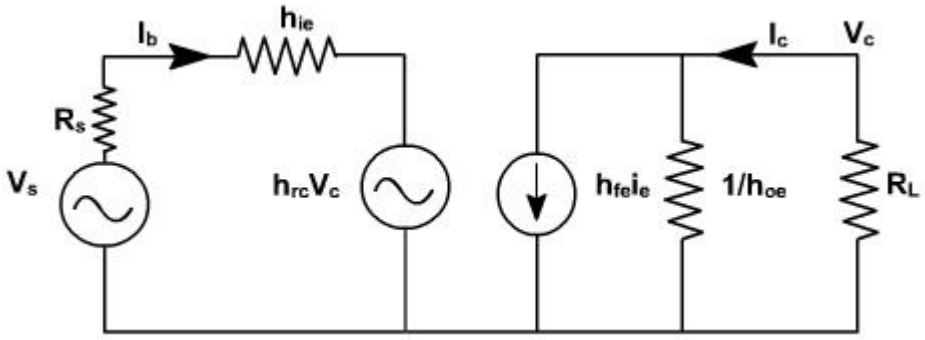



**Fig. 1.51.Simplified CE Hybrid Model**

Since $h_{fe}$.hre = 0.01(approximately), this voltage may be neglected in comparison with h ic $I_b$ drop across $h_{ie}$ provided $R_L$ is not very large. If load resistance $R_L$ is small than $h_{oe}$ and $h_{re}$ can be neglected.

$$A_I = -\frac{h_{fe}}{1+h_{oe}R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_V = \frac{A_I R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie}}$$

Output impedance seems to be infinite. When Vs = 0, and an external voltage is applied at the output we fined $I_b = 0$, $I_C = 0$. True value depends upon $R_S$ and lies between 40 K and 80K.

On the same lines, the calculations for CC and CB can be done.

**CE amplifier with an emitter resistor:**

The voltage gain of a CE stage depends upon hfe. This transistor parameter depends upon temperature, aging and the operating point. Moreover, hfe may vary widely from device to device, even for same type of transistor. To stabilize voltage gain A V of each stage, it should be independent of hfe. A simple and effective way is to connect an emitter resistor Re as shown in fig. 5. The resistor provides negative feedback and provide stabilization.

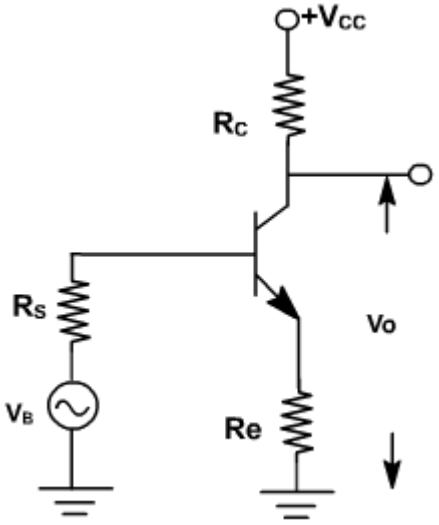



**Fig. 52 CE Amplifier with Emitter Resistor**

An approximate analysis of the circuit can be made using the simplified model.

$$\text{Current gain } A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe}\, I_b}{I_b}$$

$$= -h_{fe}$$

It is unaffected by the addition of $R_C$.

Input resistance is given by

$$R_i = \frac{V_i}{I_b}$$

$$= \frac{h_{ie}\, I_b + (1+h_{fe})\, I_b\, R_e}{I_b}$$

$$= h_{ie} = (1+h_{fe})\, R_e$$

The input resistance increases by $(1+h_{fe})R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe}\, R_L}{h_{ie} + (1+h_{fe})R_e}$$

Clearly, the addition of $R_e$ reduces the voltage gain.

If $(1+h_{fe})R_e >> h_{ie}$ and $h_{fe} >> 1$

then

$$A_v = \frac{-h_{fe}\, R_L}{(1+h_{fe})R_e} \approx -\frac{R_L}{R_e}$$

Subject to above approximation A V is completely stable. The output resistance is infinite for the approximate model.

## 1.15. Common Base Amplifier:

The common base amplifier circuit is shown in Fig. 1. The VEE source forward biases the emitter diode and VCC source reverse biased collector diode. The ac source vin is connected to emitter through a coupling capacitor so that it blocks dc. This ac voltage produces small fluctuation in currents and voltages. The load resistance RL is also connected to collector through coupling capacitor so the fluctuation in collector base voltage will be observed across RL.The dc equivalent circuit is obtained by reducing all ac sources to zero and opening all capacitors. The dc collector current is same as IE and VCB is given by

$$V_{CB} = V_{CC} - I_C R_C.$$

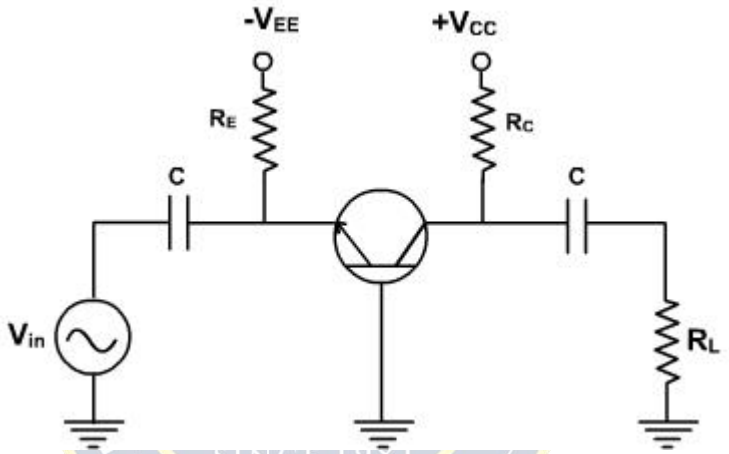



Fig. 53: Common Base Amplifier with Emitter Resistance

These current and voltage fix the Q point. The ac equivalent circuit is obtained by reducing all dc sources to zero and shorting all coupling capacitors. r'e represents the ac resistance of the diode as shown in Figure 1.54.

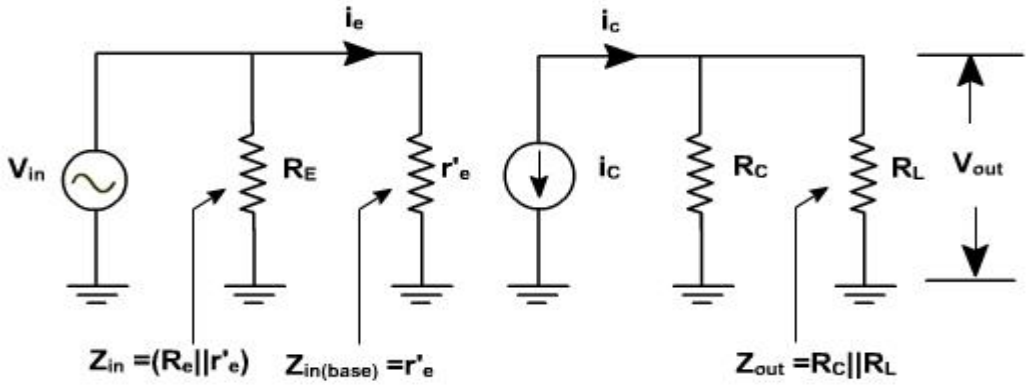



Fig. 1.54. CB Amplifier with Emitter Resistance

Figure 1.55, shows the diode curve relating $I_E$ and $V_{BE}$. In the absence of ac signal, the transistor operates at Q point (point of intersection of load line and input characteristic). When the ac signal is applied, the emitter current and voltage also change. If the signal is small, the operating point swings sinusoidally about Q point (A to B).

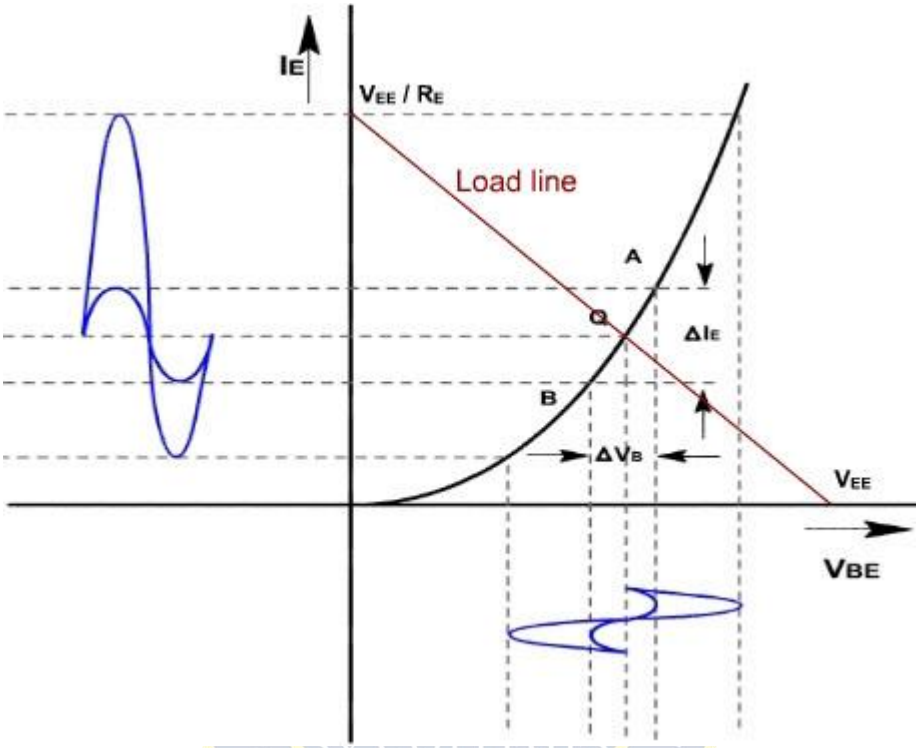



Fig .1.55.DC load line

If the ac signal is small, the points A and B are close to Q, and arc A B can be approximated by a straight line and diode appears to be a resistance given by

$$r'_e = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{\text{small change}}$$

$$= \frac{V_{be}}{i_e} = \frac{\text{ac voltage across base and emitter}}{\text{ac current through emitter}}$$

If the input signal is small, input voltage and current will be sinusoidal but if the input voltage is large then current will no longer be sinusoidal because of the non linearity of diode curve. The emitter current is elongated on the positive half cycle and compressed on negative half cycle. Therefore the output will also be distorted.

r'e is the ratio of ΔVBE and Δ IE and its value depends upon the location of Q. Higher up the Q point small will be the value of r' e because the same change in VBE

produces large change in IE. The slope of the curve at Q determines the value of r'e. From calculation it can be proved that.

$$r'e = 25mV / IE$$

**Small Signal CE Amplifiers:**

CE amplifiers are very popular to amplify the small signal ac. After a transistor has been biased with a Q point near the middle of a dc load line, ac source can be coupled to the base. This produces fluctuations in the base current and hence in the collector current of the same shape and frequency. The output will be enlarged sine wave of same frequency.

The amplifier is called linear if it does not change the wave shape of the signal. As long as the input signal is small, the transistor will use only a small part of the load line and the operation will be linear.

On the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut off. This clips the peaks of the input and the amplifier is no longer linear.

The CE amplifier configuration is shown in fig. 1.

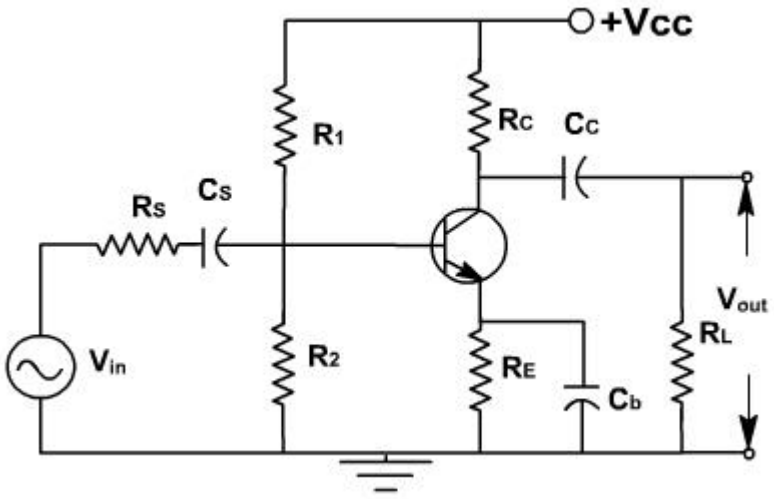



Fig. 1.56.Single Stage CE Amplifier

The coupling capacitor (CC ) passes an ac signal from one point to another. At the same time it does not allow the dc to pass through it. Hence it is also called blocking capacitor.

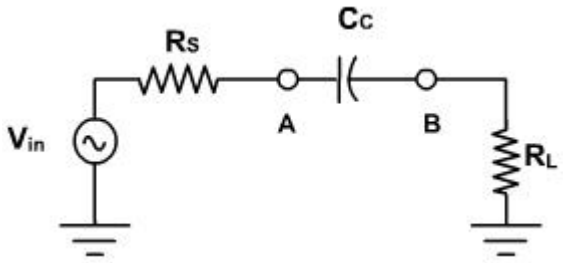



Fig. 1.57. Coupling Capacitor with source Resistance

For example in fig. 2, the ac voltage at point A is transmitted to point B. For this series reactance XC should be very small compared to series resistance RS. The circuit to the left of A may be a source and a series resistor or may be the Thevenin equivalent of a complex circuit. Similarly RL may be the load resistance or equivalent resistance of a complex network. The current in the loop is given by

$$i = \frac{v_{in}}{\sqrt{(R_S + R_L)^2 + X_C^2}} = \frac{v_{in}}{\sqrt{R^2 + X^2}}$$

$$X_C \left( = \frac{1}{2\pi fc} \right)$$

As frequency increases, $X_C$ decreases, and current increases until it reaches to its maximum value vin / R. Therefore the capacitor couples the signal properly from A to B when XC<< R. The size of the coupling capacitor depends upon the lowest frequency to be coupled. Normally, for lowest frequency XC □□0.1R is taken as design rule.

The coupling capacitor acts like a switch, which is open to dc and shorted for ac.

The bypass capacitor Cb is similar to a coupling capacitor, except that it couples an ungrounded point to a grounded point. The Cb capacitor looks like a short to an ac signal and therefore emitter is said ac grounded. A bypass capacitor does not disturb the dc voltage at emitter because it looks open to dc current. As a design rule XCb □ 0.1RE at Analysis of CE amplifier:

In a transistor amplifier, the dc source sets up quiescent current and voltages. The ac source then produces fluctuations in these current and voltages. The simplest way to analyze this circuit is to split the analysis in two parts: dc analysis and ac analysis. One can use superposition theorem for analysis .

**AC & DC Equivalent Circuits:**

For dc equivalent circuit, reduce all ac voltage sources to zero and open all ac current sources and open all capacitors. With this reduced circuit shown in fig. 3 dc current and voltages can be calculated.

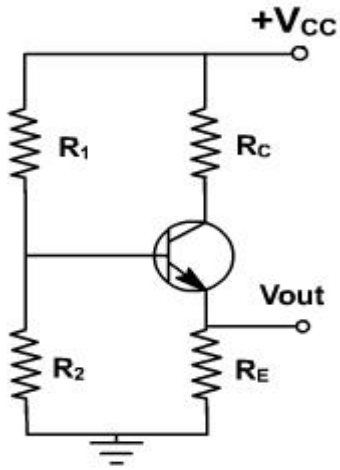



**Fig. 58. DC Equivalent Circuit**

For ac equivalent circuits reduce dc voltage sources to zero and open current sources and short all capacitors. This circuit is used to calculate ac currents and voltage as shown in fig. 4.

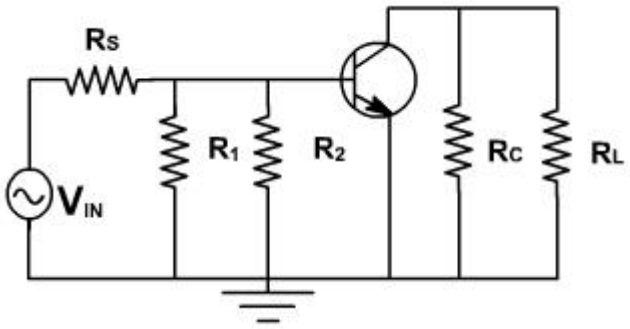



**Fig. 59. AC Equivalent Circuit**

The total current in any branch is the sum of dc and ac currents through that branch. The total voltage across any branch is the sum of the dc voltage and ac voltage across that branch.

**Phase Inversion:**

Because of the fluctuation is base current; collector current and collector voltage also swings above and below the quiescent voltage. The ac output voltage is

inverted with respect to the ac input voltage, meaning it is 180o out of phase with input.

During the positive half cycle base current increase, causing the collector current to increase. This produces a large voltage drop across the collector resistor; therefore, the voltage output decreases and negative half cycle of output voltage is obtained. Conversely, on the negative half cycle of input voltage less collector current flows and increases the voltage drop across the collector resistor decreases, and hence collector voltage we get the positive half cycle of output voltage as shown in 60.

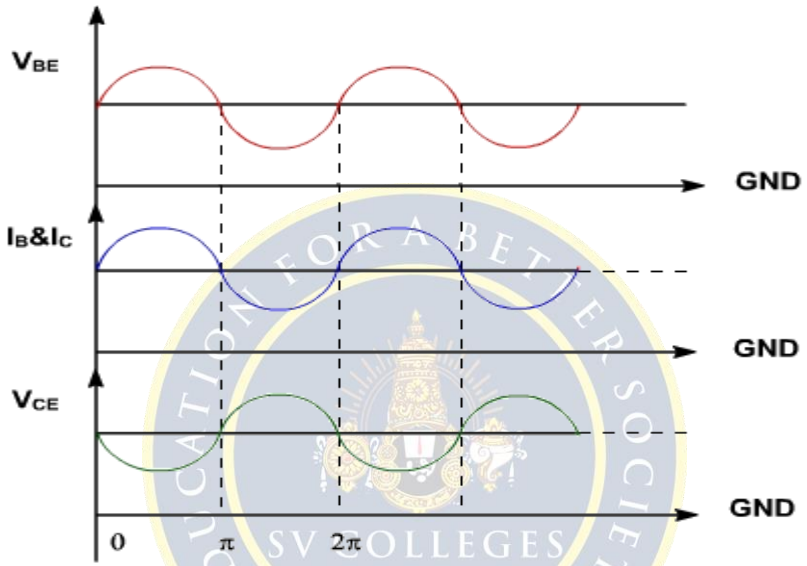



**Fig.60. Input and output waveforms of CE Amplifier**

**AC Load line:**

Consider the dc equivalent circuit shown in Figure 61.

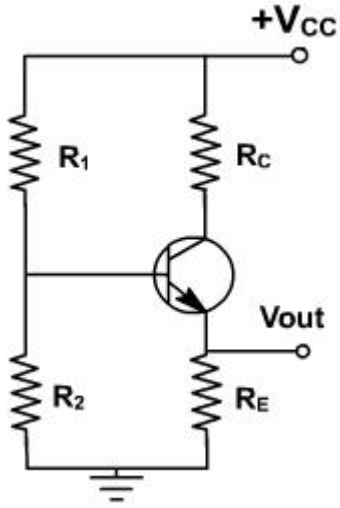



**Fig. 61 DC Equivalent Circuit**

Assuming $I_C = I_C(approx)$, the output circuit voltage equation can be written as

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

and $$I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E}$$

and $$I_C = 0, \quad V_{CE} = V_{CC}$$

The slope of the d.c load line is. $-\frac{1}{R_C + R_E}$

When considering the ac equivalent circuit, the output impedance becomes RC || RL which is less than (RC +RE).

In the absence of ac signal, this load line passes through Q point. Therefore ac load line is a line of slope (-1 / ( RC || RL) ) passing through Q point. Therefore, the output voltage fluctuations will now be corresponding to ac load line as shown in fig. 2. Under this condition, Q-point is not in the middle of load line, therefore Q-point is selected slightly upward, means slightly shifted to saturation side.

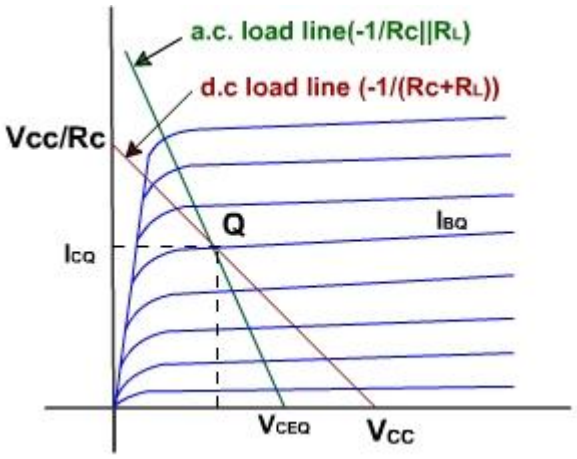



**Fig. 62 Determination of operating point**

## 9. Practice Quiz

**1. H-Parameters are preferred over other parameters due to**

a) They are easy to measure

b) They can convert from one configuration to other configuration easily

c) Readily supplied by manufacturers

**d) All of the above**

**2. Which amplifier has high Voltage gain**

**a) Common Base Amplifier**

b) Common Collector Amplifier

c) Common Emitter Amplifier

d) None of the above

**3. Which amplifier has high Current gain**

**a) Common Collector Amplifier**

b) Common Emitter Amplifier

c) Common Base Amplifier

d) None of the above

**4 Which amplifier is suitable for power amplification**

a) Common Collector Amplifier

**b) Common Emitter Amplifier**

c) Common Base Amplifier

d) None of the above

**5. Which device is used as a voltage variable resistor**

a) BJT

b) **JFET**

c) P N Diode

d) Zener Diode

**6. The output impedance of common source amplifier $Z_0$ is approximately equal to**

a) Source Resistance ($R_S$)

**b) Drain Resistance ($R_D$)**

c) Gate Resistance ($R_G$)

d) None of the above

**7. The relation between μ, $g_m$ and $r_d$ is**

a) $\mu=g_m+r_d$

b) **$\mu=g_m*r_d$**

c) $\mu=g_m/r_d$

d) $\mu=g_m-r_d$

**8. FET is preferred over BJT due to**

a) FET is a voltage controlled device
b) FET is temperature independent compared to BJT
c) FET has High Input Impedance
**d) All of the Above**

**9. The current gain for BJT in small signal model is**

**a)** $A_I = \frac{-h_f}{1+h_0 Z_L}$

b) $A_I = \frac{-h_f}{1+h_0 Z_I}$

c) $A_I = \frac{h_f}{1+h_0 Z_L}$

d) $A_I = \frac{h_f}{1+h_r Z_L}$

**10. The input impedance of BJT in small signal model is**

**a)** $Z_i = h_i + h_r A_I Z_L$

b) $Z_i = h_i - h_r A_I Z_L$

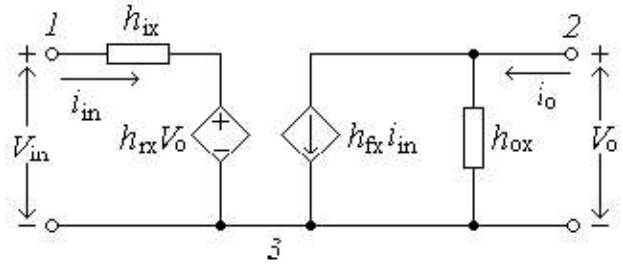
c) $Z_i = h_i + h_f A_I Z_L$

d) $Z_i = h_i - h_f A_I Z_L$

**10.Assignments**

| S.No | Question | BL | CO |
|---|---|---|---|
| 1 | Derive the voltage gain, current gain , input impedance and output impedance of Common collector amplifier using h-parameter small signal model | **2** | **1** |
| 2 | Derive the voltage gain, current gain , input impedance and output impedance of FET Common Drain Amplifier | **2** | **1** |
| 3 | Derive the voltage gain, current gain , input impedance and output impedance of Common base amplifier using simplified hybrid model | **2** | **1** |
| 4 | Determine the operating point of BJT using dc load line and ac load line analysis | **2** | **1** |
| 5 | Derive the voltage gain, current gain , input impedance and output impedance of MOSFET Common Source Amplifier | **3** | **1** |

## 11. Part A- Question & Answers

| S.No | Question & Answers | BL | CO |
|---|---|---|---|
| 1 | **What is meant by biasing a transistor?**<br>**Ans.** Process of maintaining proper flow of zero signal collector current and collector emitter voltage during the passage of signal. Biasing keeps emitter base junction forward biased and collector base junction reverse biased during the passage of signal. | **1** | **1** |
| 2 | **What is an amplifier?**<br>**Ans.** Amplifier raises the level of a weak signal.<br>No change in the wave shape.<br>No change in the frequency of the input signal | **1** | **1** |
| 3 | **What is a D.C. Load Line?**<br>**Ans.** It is a graph drawn between collector current $I_C$ and collector to emitter voltage VCE for a given $V_{CC}$ and $R_C$. | **1** | **1** |
| 4 | **What is operating point?**<br>**Ans.** It is a point on the DC load line which specifies collector current IC and collector emitter voltage VCE that exist when no signal is applied. | **1** | **1** |
| 5 | **Draw the h-parameter circuit and its equivalent circuit in CE configuration**<br>**Ans.**<br>  | **1** | **1** |
| 6 | **List out the advantages of h-parameters.**<br>**Ans.** H-parameters are real numbers at audio frequencies.<br>These are easy to measure.<br>H-parameter can also be obtained from the transistor static characteristic curves.<br>H-parameters are convenient to use in circuit analysis and design.<br>A set of h-parameters is specified for many transistors by the manufacturers | **1** | **1** |

| | | | |
|---|---|---|---|
| 7 | **Define small signal amplifier?**<br>**Ans.** When the input signal of an amplifier is relatively weak and generates amplified output signal, the amplifier is called small signal amplifier or voltage amplifier. | **2** | **1** |
| 8 | **How to obtain ac equivalent of a network?**<br>**Ans. 1.** Setting all dc sources to zero and replacing them by a short-circuit equivalent<br>2. Replacing all capacitors by a short-circuit equivalent<br>3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2<br>4.Redrawing the network in a more convenient and logical form | **2** | **1** |
| 9 | **Which configurations having very low input impedance?**<br>Ans. The common base configuration has very low input impedance, but it can have a significant voltage gain. The current gain is just less than one, and the output impedance is simply RC. | **2** | **1** |
| 10 | **Which parameters determine the operating conditions of a transistor?**<br>**Ans** The operating conditions of a transistor are determined by<br>• VCE collector to emitter voltage<br>• IC collector current<br>• The value of IC for a given VCE can be known from output characteristics of a transistor and From D.C. Load Line | **2** | **1** |
| 11 | **Why C.E. Configuration is commonly used?**<br>**Ans.** Its input and output impedances are suitable in many applications. It offers current gain, voltage gain, power gain | **2** | **1** |

## 12. Part B- Questions

| S.No | Question | BL | CO |
|---|---|---|---|
| 1 | Derive the input impedance, output impedance ,voltage gain and current gain for small signal CE amplifier | **1** | **1** |
| 2 | Derive the input impedance, output impedance ,voltage gain and current gain for small signal common source FET amplifier | **2** | **1** |
| 3 | Draw the simplified CC Hybrid model and derive the expressions for input impedance, output impedance ,voltage gain and | **2** | **1** |

| | | | |
|---|---|---|---|
| | current gain | | |
| 4 | Derive the input impedance, output impedance ,voltage gain and current gain for small signal common Drain MOSFET amplifier | **3** | **1** |
| 5 | Determine the operating point and draw the dc load line and ac load line analysis of BJT and FET. | **3** | **1** |

## 13. Supportive Online Certification Courses

1. Analog Electronic Circuits By Prof. Pradip Mandil, conducted by IIT Kharagpur – 12 weeks
2. Analog Electronic Circuits By Prof. Dr. Shouribrata Chatterjee, conducted by IIT Kharagpur – 12 weeks.

## 14. Real Time Applications

| S.No | Application | CO |
|---|---|---|
| 1 | **Determine the frequency response of single stage amplifier**<br>By keeping the input signal voltage constant and by changing the input frequencies ,the change in the output voltage is noted and by drawing the plot between output voltage for different frequencies. we can obtain th frequency response of amplifier | **1** |
| 2 | **Determine the frequency response of Common source amplifier**<br>By keeping the input signal voltage constant and by changing the input frequencies ,the change in the output voltage is noted and by drawing the plot between output voltage for different frequencies. we can obtain th frequency response of amplifier | **1** |
| 3 | **Calculating input impedance, output impedance ,voltage gain and current gain for BJT, FET and MOSFET amplifiers**<br>From the h-parameter model of BJT and small signal model of FET, the input impedance, output impedance ,voltage gain and current gain for BJT, FET and MOSFET amplifiers | **1** |

## 15. Contents Beyond the Syllabus

1. **The $r_e$ model of Transistor**

   The advantages of using this model compared to h-parameters are are (i) required parameters are easily available (ii) simple and easy procedure (iii) results obtained have a fairly good accuracy for the study of amplifier circuits.

2. **Millers Theorem and its Dual**

To know the exact value of input impedance and output impedance when a resistor, capacitor or inductor connected directly from input to output.

## 16. Prescribed Text Books & Reference Books

### Text Book

1. Donald A Neaman- "Electronic Circuits – Analysis and Design," 3rdEdition, McGraw Hill (India), 2019.
2. J. Millman, C Chalkias, "Integrated Electronics", 4th Edition, McGraw Hill Education (India) Private Ltd., 2015.

### References:

1. Robert L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuits Theory", 9th Edition, Pearson/Prentice Hall, 2006.

## 17. Mini Project Suggestion

### 1. Water Pump Controller circuit

A water pump controller senses the level of water in a tank and drives the water pump. The circuit described here is built around timer IC1 (555). When the water level of tank goes below the low level marked by 'L' the voltage at pin 2 of IC1 becomes low. As a result, internal SR-flip-flop of IC1 resets and its output goes high. This high output pin 3 of IC1 drives relay driver transistor T1 (BC547) and energises relay RL1. Water pump gets mains power supply through n/o contacts of the relay and is powered on. It starts filling water in the tank.

### 2. Farmhouse Lantern-Cum-Flasher

This circuit uses a dual op-amp IC LM358 and two transistors. It can be powered by a 6V maintenance free rechargeable battery or a lead-acid accumulator type battery. It has two modes of operation: flasher mode and dimmer mode. The dimmer mode helps conserve the battery power, while in flasher mode the lantern can be used as a beacon

### 3. Sound-Operated Switch for Lamps

This inexpensive, fully transistorised switch is very sensitive to sound signals and turns on a lamp when you clap within 1.5 metres of the switch. One of its interesting applications is in discotheques, where lights could be turned on or off in sync with the music beats or clapping