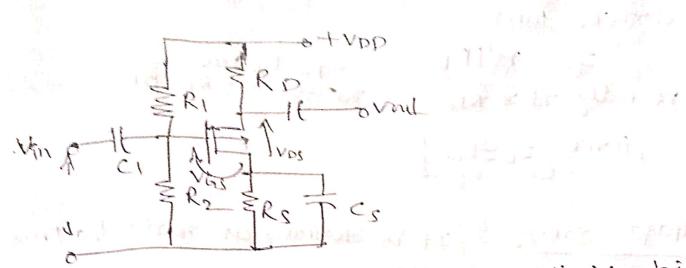
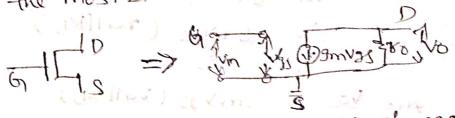
small signal Analysis of common source amplifies

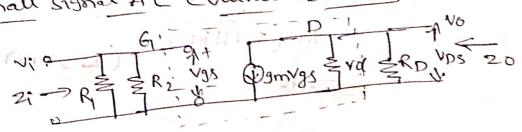


The Ac avuivalent model of voltage devider bias. circuit of MOSPET can be obtained by all capacitors and biasing sources work shorting.

Reface the mosfer with small signal contivalent mosal



small signal AC exuivalent model of MOSFET:



Input impedance is measured at the sengut torninal. Then Input impedance:(zi) zi= RillR2 = RG

output impedance (20) :- output impedance is measured at the output terminal with input voltage Vi=0're Short ext-mat is all independent sources are becomes zero

From the tigb. when Vp-0, Vgs=0 tuen dependent source 9 mvg is open ckt turn Typical valus (8d=35km & RD=5km) Zo= YdllRD normally od >>RD. Honce / Zo=RD Voltage gain: _ It is defined as natio of outry voltage to the input voltage. restances We the top of the value of the said of the s VAS = VO = - Id (Valled) ---And som of some of some of some Vo= -9mvgs (rallRD)

Vi= V85 137 com de Vo = -9m vgs (8dIIRD) =-9m (2011RD) (2017RD) (2017RD) (is): emphanisty topo partitioning of James at Jacks about 81 Dackston; began 24 = 1/4/1 = 1/4 anguation Lakes - I (at) the street has the

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small signal Analysis of Common Source amplifier Dsing cionby Passed Rs: ather till in GI O Domings Fra & RDVO

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RS LVS FT FT Input impedance: -Input impedance is measured at input towning Z9= R1/1R2 1/11/4 III CHEMBI I), or will output impedance:output impedance is measured at output terminal cohen inpledependent sources be comes zero il Vizo. when Vi=0 R, & R2 are also short ckted. Then 20= 20 11RD (151111) 2017 Wout -vaat Vi=0 Raut = V2 Incluingo Warth visite at input side kyl vgs + id Rs = D consent flows from Vg8 = - Pars 1) write KVL at Drain to Source voltage dropacooss RDidvix = valid - 9mvgs) + idres =80 (id+9midRs)+idRs

$$V_1 = id (x_0 + 9m \text{ YORs}) + idRs$$

$$\frac{1}{26} Rout \frac{V_M}{Aa} = 30 + Rs + 9m \text{ YORs} = 7d + Rs (1+9m \text{ YO})$$

$$\frac{1}{12} = 4id + 4v$$

$$\frac{1}{12} = 4id + 4v$$

$$\frac{1}{12} = \frac{1}{12} \frac{1}$$

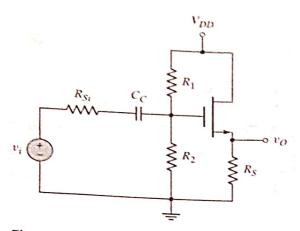
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4.4

THE COMMON-DRAIN (SOURCE-FOLLOWER) AMPLIFIER

Objective: • Analyze the common-drain (source-follower) amplifier and become familiar

The second type of MOSFET amplifier to be considered is the common-drain circuit. An example of this circuit configuration is shown in Figure 4.30. As seen in the figure, the output signal is taken off the source



Flgure 4.30 NMOS source-follower or common-drain amplifier

with respect to ground and the drain is connected directly to V_{DD} . Since V_{DD} becomes signal ground in the ac equivalent circuit, we have the name common drain. The more common name is **source follower**. The reason for this name will become apparent as we proceed through the analysis.

4.4.1 Small-Signal Voltage Gain

The dc analysis of the circuit is exactly the same as we have already seen, so we will concentrate on the small-signal analysis. The small-signal equivalent circuit, assuming the coupling capacitor acts as a short circuit, is shown in Figure 4.31(a). The drain is at signal ground, and the small-signal resistance r_o of the transistor is in parallel with the dependent current source. Figure 4.31(b) is the same equivalent circuit, but with all signal grounds at a common point. We are again neglecting the body effect. The output voltage is

$$V_o = (g_m V_{gs})(R_S || r_o) (4.30)$$

Writing a KVL equation from input to output results in the following:

$$V_{\rm in} = V_{gs} + V_o = V_{gs} + g_m V_{gs} (R_S || r_o)$$
 (4.31(a))

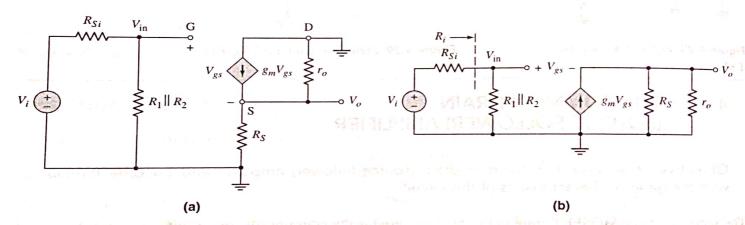


Figure 4.31 (a) Small-signal equivalent circuit of NMOS source follower and (b) small-signal equivalent circuit of NMOS source follower with all signal grounds at a common point

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$$V_{in} = \frac{V_{in}}{1 + g_m(R_S \parallel r_o)} = \left[\frac{\frac{1}{g_m}}{\frac{1}{g_m} + (R_S \parallel r_o)}\right] \cdot V_{in}$$
(4.31(b))

Equation (4.31(b)) is written in the form of a voltage-divider equation, in which the gate-to-source of the Equation (in which the gate-to-source of the wilder equation) looks like a resistance with a value of $1/g_m$. More accurately, the effective resistance looking source terminal (ignoring r_o) is $1/g_m$. The voltage V_{in} is related to the 1/0S device terminal (ignoring r_o) is $1/g_m$. More accurately, the effective resistance look to the source terminal (ignoring r_o) is $1/g_m$. The voltage V_{in} is related to the source input voltage V_i by

$$V_{ii} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i \tag{4.32}$$

 $R_1 = R_1 || R_2$ is the input resistance to the amplifier. $R_i = \frac{1}{100}$ Equations (4.31(b)) and (4.32) into (4.30), we have the small-signal voltage gain:

$$\frac{g_{u} g_{m}(R_{S} \| r_{o})}{A_{v}} = \frac{g_{m}(R_{S} \| r_{o})}{1 + g_{m}(R_{S} \| r_{o})} \cdot \left(\frac{R_{i}}{R_{i} + R_{Si}}\right)$$
(4.33(a))

$$A_{i} = \frac{R_{S} \| r_{o}}{\frac{1}{g_{m}} + R_{S} \| r_{o}} \cdot \left(\frac{R_{i}}{R_{i} + R_{Si}} \right)$$
(4.33(b))

which again is written in the form of a voltage-divider equation. An inspection of Equation 4.33(b) shows that the magnitude of the voltage gain is always less than unity.

EXAMPLE 4.8

Objective: Calculate the small-signal voltage gain of the source-follower circuit in Figure 4.30. Assume the circuit parameters are $V_{DD}=12$ V, $R_1=162$ k Ω , $R_2=463$ k Ω , and $R_S=0.75$ k Ω , and the transistor parameters are $V_{TN}=1.5$ V, $K_n=4$ mA/V², and $\lambda=0.01$ V⁻¹. Also assume $R_{Si}=4$ k Ω .

Solution: The dc analysis results are $I_{DQ} = 7.97$ mA and $V_{GSQ} = 2.91$ V. The small-signal transconductance is therefore

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(4)(2.91 - 1.5) = 11.3 \text{ mA/V}$$

and the small-signal transistor resistance is

$$r_o \cong [\lambda I_{DQ}]^{-1} = [(0.01)(7.97)]^{-1} = 12.5 \,\mathrm{k}\Omega$$

The amplifier input resistance is

$$R_i = R_1 \| R_2 = 162 \| 463 = 120 \,\mathrm{k}\Omega$$

The small-signal voltage gain then becomes

$$A_v = \frac{g_m(R_S \parallel r_o)}{1 + g_m(R_S \parallel r_o)} \cdot \frac{R_i}{R_i + R_{Si}}$$

$$= \frac{(11.3)(0.75 \parallel 12.5)}{1 + (11.3)(0.75 \parallel 12.5)} \cdot \frac{120}{120 + 4} = +0.860$$

Small-Signal Voltage and Current Gains

In the common-gate configuration, the input signal is applied to the source terminal and the gate is at signal in the common-gate configuration shown in Figure 4.36 is biased with a constant-current source charge on the gate terminal, and the capacitos source is at signal charge on the gate terminal. In the common-gate configuration, the input signal is applied to one and the gate is at signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. The common-gate configuration shown in Figure 4.36 is biased with a constant-current sat signal ground. In the common-gate configuration, the rope ground. The common-gate configuration shown in Figure 4.50 is charge on the gate terminal, and the capacitor $c_{\text{urrent}} = c_{\text{urrent}} = c_{\text$ ground. The common-gate configuration. The gate resistor R_G prevents the buildup of static charge on the g_{abc} couples the signal to the source, and g_{abc} that the gate is at signal ground. The coupling capacitor C_{C1} couples the signal to the source, and g_{abc} coupling g_{abc

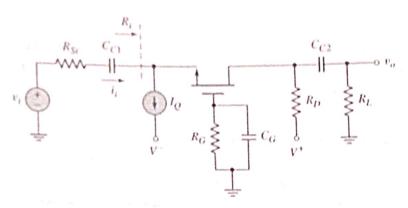


Figure 4.36 Common-gate circuit

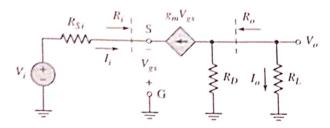


Figure 4.37 Small-signal equivalent circuit of common-gate amplifier

The small-signal equivalent circuit is shown in Figure 4.37. The small-signal transistor resistance assumed to be infinite. Since the source is the input terminal, the small-signal equivalent circuit shown i ure 4.37 may appear to be different from those considered previously. However, to sketch the equi circuit, we can use the same technique as used previously. Sketch in the three terminals of the transisto the source at the input for this case. Then draw in the transistor equivalent circuit between the three ter and then sketch in the remaining circuit elements around the transistor.

The output voltage is

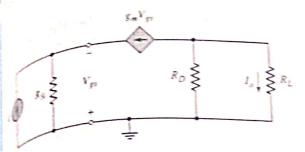
$$V_o = -(g_m V_{gs})(R_D || R_L)$$

Writing the KVL equation around the input, we find

$$V_i = I_i R_{Si} - V_{gs}$$

where $I_i = -g_m V_{gs}$. The gate-to-source voltage can then be written as

$$V_{gs} = \frac{-V_i}{1 + g_m R_{Si}}$$



55 Small-signal equivalent circuit of common-gate amplifier with a Norton equivalent signal source

$$\int_{A}^{\infty} \frac{g_{mh} || \operatorname{signal}}{V_{i}} = \frac{g_{m}(R_{D} || R_{L})}{1 + g_{m} R_{Si}}$$
(4.41)

the voltage gain is positive, the output and input signals are in phase. to many cases, the signal input to a common-gate circuit is a current. Figure 4.38 shows the small-signal In many I_0 common-gate circuit with a Norton equivalent circuit as the signal source. We can calculate a curagain the output current I_0 can be written The output current I_o can be written

$$I_{s} = \left(\frac{R_{D}}{R_{D} + R_{L}}\right) \left(-g_{m} V_{gs}\right) \tag{4.42}$$

ute input we have

$$\frac{1}{l_1 + g_m V_{gs}} + \frac{V_{gs}}{R_{Si}} = 0 {4.43}$$

$$V_{ps} = -I_i \left(\frac{R_{Si}}{1 + g_m R_{Si}} \right) \tag{4.44}$$

The small-signal current gain is then

$$A_{i} = \frac{I_{o}}{I_{i}} = \left(\frac{R_{D}}{R_{D} + R_{L}}\right) \cdot \left(\frac{g_{m}R_{Si}}{1 + g_{m}R_{Si}}\right) \tag{4.45}$$

We may note that if $R_D \gg R_L$ and $g_m R_{Si} \gg 1$, then the current gain is essentially unity.

Input and Output Impedance

is contrast to the common-source and source-follower amplifiers, the common-gate circuit has a low input assistance because of the transistor. However, if the input signal is a current, a low input resistance is an adunage. The input resistance is defined as

$$R_i = \frac{-V_{gs}}{l_i} \qquad \text{the presentation of the latter of the state of the stat$$

Since $l_i = -g_m V_{gs}$, the input resistance is

$$R = \frac{1}{g_m} \tag{4.47}$$

This result has been obtained previously.

Part 1 Semiconducts.

We can find the output resistance by setting the input signal voltage equal to zero. From Figure 4.37, we which means that $V_{gs} = 0$. Consequently, $g_m V_{gs} = 0$. The output resistance $V_{gs} = 0$. We can find the output resistance by setting the input significance $g_m V_{gs} = 0$. The output $g_s V_{gs} = 0$. The load resistance, is therefore looking back from the load resistance, is therefore

$$R_o = R_D \tag{4.48}$$

EXAMPLE 4.11

Objective: For the common-gate circuit, determine the output voltage for a given input current. For the circuits shown in Figures 4.36 and 4.38, the circuit parameters are: $I_Q = 1$ mA, $V^+ = 5V$. For the circuits shown in Figures 4.30 and $R_L = 10 \text{ k}\Omega$. The transistor parameters are: $V_{TN} = 5 \text{ V}$, $V^- = -5 \text{ V}$, $R_G = 100 \text{ k}\Omega$, $R_D = 4 \text{ k}\Omega$, and $R_L = 10 \text{ k}\Omega$. The transistor parameters are: $V_{TN} = 1 \text{ V}$, $V^- = -5 \text{ V}$, $R_G = 100 \text{ k}\Omega$, $R_D = 4 \text{ k}\Omega$, and $R_L = 10 \text{ k}\Omega$. The transistor parameters are: $V_{TN} = 1 \text{ V}$, $V^- = 100 \text{ k}\Omega$, and $V^- = 100 \text{ k}\Omega$. The transistor parameters are: $V_{TN} = 100 \text{ k}\Omega$, $V^- = 100 \text{ k}\Omega$, $V^- = 100 \text{ k}\Omega$, and $V^- = 100 \text{ k}\Omega$. $V^- = -5$ V, $R_G = 100$ k Ω , $R_D = 4$ K Ω , and $R_L = 1$ V, $R_S = 1$ V, $R_S = 1$ V, $R_S = 1$ M Ω and $R_S = 1$ V, $R_S = 1$ M Ω and $R_S = 1$ V, $R_S = 1$ V, $R_S = 1$ M Ω and $R_S = 1$ M Ω and $R_S = 1$ V, $R_S = 1$ M Ω and $R_S = 1$ V, $R_S = 1$ M Ω and $R_S = 1$

Solution: The quiescent gate-to-source voltage is determined from

$$I_Q = I_{DQ} = K_n (V_{GSQ} - V_{TN})^2$$

OL

$$1 = 1(V_{GSQ} - 1)^2$$

which yields

$$V_{GSO} = 2 \text{ V}$$

The small-signal transconductance is

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(1)(2 - 1) = 2 \text{ mA/V}$$

From Equation (4.45), we can write the output current as

$$I_o = I_i \left(\frac{R_D}{R_D + R_L} \right) \cdot \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}} \right)$$

The output voltage is $V_o = I_o R_L$, so we find

$$V_{o} = I_{i} \left(\frac{R_{L} R_{D}}{R_{D} + R_{L}} \right) \cdot \left(\frac{g_{m} R_{Si}}{1 + g_{m} R_{Si}} \right)$$
$$= \left[\frac{(10)(4)}{4 + 10} \right] \cdot \left[\frac{(2)(50)}{1 + (2)(50)} \right] \cdot (0.1) \sin \omega t$$

or

$$V_o = 0.283 \sin \omega t \,\mathrm{V}$$

Comment: As with the BJT common-base circuit, the MOSFET common-gate amplifier is useful if the input signal is a current.