ESPECIFICAÇÃO DO PROJETO (Segunda Unidade)

Projeto da CPU

O projeto da CPU precisa ser acoplado a um decodificador para display de sete segmentos que também será desenvolvido. Neste projeto da segunda unidade, a **ULA** e os registradores da CPU devem ser desenvolvidos usando Portas Lógicas ou em verilog, já a **Unidade de Controle** da CPU em Verilog.

O projeto deve estar pronto para baixar na placa de prototipação DE2-70, inclusive com as pinagens configuradas. As respectivas pinagens (associação de um sinal entrada/saída com um pino do FPGA) estão especificadas em anexo.

Deverá ser entregue um relatório impresso ao professor juntamente com o código fonte (pasta completa do projeto compactada), detalhando cada fase desenvolvida, que deve conter:

- a) Capa com identificação dos alunos
- b) Visão Geral do Projeto (figura ilustrando o sistema completo em blocos). Explicar sucintamente nesta etapa cada módulo desenvolvido.
- c) Circuito ou Verilog projetado de cada módulo e simulação (waveform)
- d) Circuito / Verilog com todo sistema conectado e simulação (waveform)
- e) Conclusão

CPU

A CPU é composta da Unidade de Controle, Unidade Lógica e Aritmética e Registradores.

Registradores

Os registradores armazenam temporariamente um dado, que nunca estará no formato de complemento a dois. O registrador pode receber 3 comandos: (00, 01, 10), oriundos de Tx, Ty e Tz. Os registradores X, Y e Z possuem 6 bits cada um (um bit de sinal e cinco de módulo). A entrada para o registrador X está conectada a 5 switches, sendo um switch para o bit de sinal e os outros quatro para o módulo do registrador X. Percebese que tem um bit a mais internamente no registrador para tratar casos em que a soma de X + Y ultrapasse o máximo para 4 bits.

Unidade de Controle

A unidade de controle é responsável pela sequência de execução das instruções na CPU. Caso o "new_instruction = 1", então indica que chegou uma nova instrução. Em seguida, o comando contido em "instruction"(oriundo do switch) é decodificado seguindo a Tabela1 abaixo. Exemplo: Caso "instruction=001", então foi o comando de CLEAR, com isso, deve-se colocar nos sinais Tx, Ty, Tz e Tula os valores indicados na tabela2. OBS.: Na tabela 2, os valores iguais a X na coluna correspondente a Tula significam don'tcare, ficando a cargo da equipe tratar este caso.

Tabela 1:

Instruction	Ação
001	CLEAR
010	ADD
011	SUB
100	DISP
101	LOAD_X

Tabela 2:

Ação	Tula	Тх	Ту	Tz
CLEAR	Х	00	00	00
ADD	00	10	01	10
SUB	01	10	01	10
DISP	Х	00	00	01
LOAD_X	Х	01	10	10

Tula

[00]: ADD (+) [01]: SUB (-)

ULA

A unidade lógica e aritmética é responsável pelas operações aritméticas de adição e subtração.

Entradas:

- 1. Dois vetores de 6 bits (1 para o sinal e 5 para o módulo) oriundos dos registradores X e Y, representando os operandos. Esses números são binários positivos ou negativos (não estarão complementados a 2).OBS.: O vetor do registrador X pode ter como valores números de -16 até 15, sendo limitado ao numero de switches. O vetor do registrador Y, por sua vez, possui números de -32 até 31.
- 2. O sinal Tula de 2 bits que representa o tipo de operação.

Saídas:

- 1. Um vetor F de 6 bits, que não deve estar complementado a dois, representando o resultado da operação. OBS.: O vetor F pode ter como valores números de -32 (100000) até 31 (011111).
- 2. Um sinal (LED) representando overflow (para as operações que podem gerar overflow).
- 3. Um sinal (LED) para indicar que o resultado é negativo (aceso quando negativo e apagado quando positivo).

Decodificador BCD para display de 7 segmentos

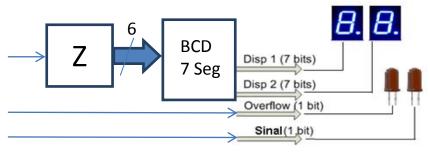
Para que seja possível exibir os números no display da placa DE2-70, o projeto da ULA deve estar acoplado a um decodificador. Os leds de cada display acendem quando colocado nível lógico 0.

Entradas:

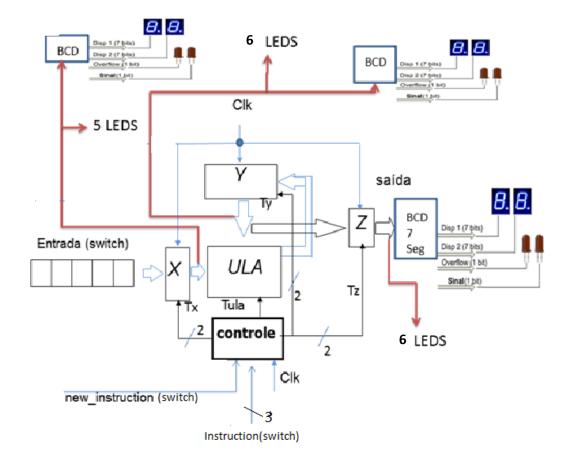
1. Vetor de 6 bits (F) vindo da ULA, representando um número binário positivo ou negativo (sem estar no complemento a 2).

Saídas:

1. Dois vetores de 7 bits representando os 2 displays, segundo a tabela abaixo.



Sistema Completo



Observação: Além de ser conectado a dois displays de 7 segmentos, cada registrador também deve estar conectado a 6 LEDS (cada bit ligado a um LED) vermelhos.

Observação: Os valores a serem processados virão de 5 switches, com 1 bit sendo de sinal e 4 para o módulo (ou seja, não virão complementados a dois).

Observação: Quando acontecer um overflow deverá ser mostrado no display de Z



Exemplo1:

SEQUÊNCIA: 7 + 2 - 3 - 1 = 5

Execução:

new instruction (Switch): 1

instruction (Switches): CLEAR (Zera Y, Z e X)

new_instruction (Switch): 1

Entrada (Switches): 00111

instruction (Switches): LOAD_X [101] (carregaem X o valor 7)

new_instruction (Switch): 1

instruction (Switches): ADD [010] (Adiciona Y = 0 com X = 7e carrega este valor em Y)

new_instruction (Switch): 1

Entrada (Switches): 00010

instruction (Switches): LOAD_X [101] (carregaem X o valor 2)

new instruction (Switch): 1

instruction (Switches): ADD [010] (Adiciona Y = 7 com X = 2 e carrega este valor em Y)

new_instruction (Switch): 1

Entrada (Switches): 00011

instruction (Switches): LOAD_X [101] (carregaem X o valor 3)

new_instruction (Switch): 1

instruction (Switches): SUB [011] (Subtrai Y = 9 de X = 3 e carrega este valor em Y)

new_instruction (Switch): 1

Entrada (Switches): 00001

instruction (Switches): LOAD_X [101] (carregaem X o valor 1)

new_instruction (Switch): 1

instruction (Switches): SUB [011] (Subtrai Y = 6 de X = 1)

new_instruction (Switch): 1

instruction (Switches): DISP [100] (Carrega o resultado em Z e zera X e Y)

Exemplo2:

SEQUÊNCIA: 7 + 14-12 -5= 4

Execução:

new instruction (Switch): 1

instruction (Switches): CLEAR (Zera Y, Z e X)

new_instruction (Switch): 1

Entrada (Switches): 00111

instruction (Switches): LOAD X [101] (carregaem X o valor 7)

new_instruction (Switch): 1

instruction (Switches): ADD [010] (Adiciona Y = 0 com X = 7 e carrega este valor em Y)

new_instruction (Switch): 1

Entrada (Switches): 01110

instruction (Switches): LOAD_X [101] (carregaem X o valor 14)

new_instruction (Switch): 1

instruction (Switches): ADD [010] (Adiciona Y = 7 com X = 14)

Overflow ocorre!

new_instruction (Switch): 1

ready (habilita o instruction): 1

instruction (Switches): DISP [100] (Carrega em Z OU e zera X e Y)

Informações sobre clock

Signal Name	FPGA Pin No.	Description
CLK_28	PIN_E16	28 MHz clock input
CLK_50	PIN_AD15	50 MHz clock input
CLK_50_2	PIN_D16	50 MHz clock input
CLK_50_3	PIN_R28	50 MHz clock input
CLK_50_4	PIN_R3	50 MHz clock input
EXT_CLOCK	PIN_R29	External (SMA) clock input

Table 5.5. Pin assignments for the clock inputs.

Pinagem:

O FPGA Cyclone II para o qual o projeto será baixado é o EP2C70F896C6.

Signal Name			Signal Name	FPGA Pin No.	Description			
ngilai italiic	FPGA Pin No.	Description	KEY[0]	PIN_T29	Pushbutton[0]	Signal Name	FPGA Pin No.	Description
LEDR[0]	PIN_AJ6	LED Red[0]	-	_		LEDG[0]	PIN_W27	LED Green[0]
LEDR[1]	PIN_ AK5	LED Red[1]	KEY[1]	PIN_T28	Pushbutton[1]	LEDG[1]	PIN_ W25	LED Green[1]
LEDR[2]	PIN_AJ5	LED Red[2]	KEY[2]	PIN_U30	Pushbutton[2]	LEDG[2]	PIN_ W23	LED Green[2]
LEDR[3]	PIN_AJ4	LED Red[3]	KEY[3]	PIN_U29	Pushbutton[3]	LEDG[3]	PIN_Y27	LED Green[3]
LEDR[4]	PIN_AK3	LED Red[4]	T.11			LEDG[4]	PIN_Y24	LED Green[4]
LEDR[5]	PIN_AH4	LED Red[5]	lable	5.2. Pin assignmen	ts for the pushbutton switches.	LEDG[5]	PIN_Y23	LED Green[5]
LEDR[6]	PIN_AJ3	LED Red[6]				LEDG[6]	PIN_ AA27	LED Green[6]
LEDR[7]	PIN_AJ2	LED Red[7]				LEDG[7]	PIN_ AA24	LED Green[7]
LEDR[8]	PIN_AH3	LED Red[8]				LEDG[8]	PIN_AC14	LED Green[8]
LEDR[9]	PIN_AD14	LED Red[9]						
LEDR[10]	PIN_AC13	LED Red[10]				1		
LEDR[11]	PIN_AB13	LED Red[11]				1		
LEDR[12]	PIN_AC12	LED Red[12]		201		_	Ethernet 10/100M Po	
LEDR[13]	PIN_AB12	LED Red[13]					A Out	RS-232 Port
LEDR[14]	PIN_AC11	LED Red[14]			USB Blaster Port USB Host Port	Video In 1 deo In 2		-
LEDR[15]	PIN_AD9	LED Red[15]				I THE LOW	POU U	
LEDR[16]	PIN_AD8	LED Red[16]				1-31-4 A	Y.	TV Dec ber (NTSC
LEDR[17]	PIN_AJ7	LED Red[17]		12V DC Power Supply = Connector		101		PS Port VG Point DAC
				Power ON/OFF Switch				Et met 10/100M
			,	Controller Audio CODEC —	CTUEVE -			
HEX0_D[06]				Altera USB Blaster — Controller chipset		E An man		50Mrz Oscillator
	RN171K	HEX0		Altera EPCS16 -		DE2-70		Expansion Header
HEX0_D0	1 8 A0 7 B0	10 a VCC33		Configuration Device		O DEGIO	CENEA. VV	Expansion Header
HEX0_D2	3 00	**************************************		200	Welcone to the	S. F.	Table of the last	
HEXU_D3	4 W 5 W	5 d 0 0 0 6		RUNIPROS Sten for — JTAGIAS : 164	Altera DE2-78	P	*	tere (c)
	RN181K	2 1 4 6		2247244				SD Card Slot SD Card Store SD
HEX0_D4 HEX0_D5	1 8 E0 2 7 F0			15x2 LCD Module -		Name and Address of the Owner, where		
HEX0_D6			1 1		A CONTRACTOR OF THE PARTY OF TH			FPGA with 70K
HEX0 DP	3 6 G0 4 DP0	7Segment Display		7-Segment Displays —			IA TA	FPGA with 70K IrDA Transceiver
HEX0_DP	3 6 GU 5 DP0	7Segment Display				and a second		FPGA with 70K I/DA Transceiver SMbyte Flash Mem
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gnal Name EXO_D[0] EXO_D[1] EXO_D[2] EXO_D[3] EXO_D[6] EXO_D[6] EXO_D[6] EXO_D[6] EXO_D[7] EXO_D[7]	PPGA PIN NO. PIN_AE8 PIN_AF9 PIN_AH9 PIN_AD10 PIN_AF10 PIN_AF10 PIN_AF11 PIN_AD12 PIN_AF12 PIN_AF12	Description Seven Segment Digit 0[0] Seven Segment Digit 0[0] Seven Segment Digit 0[1] Seven Segment Digit 0[2] Seven Segment Digit 0[3] Seven Segment Digit 0[4] Seven Segment Digit 0[5] Seven Segment Digit 0[6] Seven Segment Decimal Point 0 Description Seven Segment Digit 1[0] Seven Segment Digit 1[1] Seven Segment Digit 1[2] Seven Segment Digit 1[4] Seven Segment Digit 1[5]		18 Red LEDs —	Signal Swy	Name	No. 33 3 5 5 7 6 6 4 4 3 3 5 5 4 4 7 7	Description Toggle Switch[0] Toggle Switch[1] Toggle Switch[6] Toggle Switch[7] Toggle Switch[8] Toggle Switch[9] Toggle Switch[10]

Table 5.1. Pin assignments for the toggle switches.