Filip Księżyc **nr. 303359**

VDIC

ALU test specification

Number of input data words used in simulation can be setted by changing parameter „numberOfInputWords” in „Parameters” section specified at the top of the testbench.

This testbench perfoms 4 series of testing to cover all implemented ALU operations (ADD, AND, UNKNOWN_OPCODE). For each test input data words are generated randomly.

Data corners simulated via this testbench are:

1. Test all operations
2. Execute all operations after reset
3. Execute reset after all operations
4. Simulate all operations twice a row.

If any of tests fails then testbench will print „FAILED” in terminal, other way there will be printed „PASSED”.