

# Mobile Intel® 4 Series Express Chipset Family

**Datasheet**

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*June 2009*

Document Number: 320122-006



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## Revision History

Document Number	Revision Number	Description	Date
320122	001	<ul style="list-style-type: none"><li>Initial Release</li></ul>	July 2008
320122	002	<ul style="list-style-type: none"><li><a href="#">Chapter 1</a><ul style="list-style-type: none"><li>Added <a href="#">Section 1.3</a>: GS45 Feature Support</li><li>Added <a href="#">Section 1.4</a>: GL40 Feature Support</li></ul></li><li><a href="#">Chapter 10</a><ul style="list-style-type: none"><li>Added GS45 and GL40 power characteristic data to <a href="#">Table 24</a></li><li>Added GS45 and GL40 current data to <a href="#">Table 24</a></li><li>Added GS45 current data to <a href="#">Table 27</a></li></ul></li><li><a href="#">Section 13.3</a>: Added clocking information for GS45 and GL40</li><li><a href="#">Section 16.4</a> and <a href="#">Section 16.5</a>: Added Ballout and Signal Names for GS45</li><li><a href="#">Section 19.1.36</a>: Added Configuration Register Description for GS45 and GL40</li></ul>	August 2008
320122	003	<ul style="list-style-type: none"><li>Chapter 1<ul style="list-style-type: none"><li><a href="#">Section 1.3</a>: Added GM47 Feature Support</li><li><a href="#">Section 1.3.3</a>: Updated GS45 Graphics Core Render Clock</li><li><a href="#">Section 1.4.3</a>: Updated GL40 Graphics Core Render Clock</li></ul></li><li>Chapter 5<ul style="list-style-type: none"><li><a href="#">Section 5.1</a>: Added GS45 memory-down support on two channels</li></ul></li><li>Chapter 10<ul style="list-style-type: none"><li><a href="#">Section 10.1</a>: Added GM47, updated GS45 and GL40 TDP numbers in <a href="#">Table 23</a></li><li><a href="#">Section 10.1</a>: Added GM47, GS45 <math>I_{VCC}</math> and updated GL40 <math>I_{VCC\_AXG}</math> specification in <a href="#">Table 24</a></li><li><a href="#">Section 10.1</a>: Added GM47 and GL40 <math>I_{VCC\_AXF}</math> specification in <a href="#">Table 27</a></li></ul></li><li>Chapter 13<ul style="list-style-type: none"><li><a href="#">Section 13.3</a>: Added GM47 GMCH Clock Frequency Support</li><li><a href="#">Section 13.3</a>: Added GL40 conversion stepping updates to Clock Frequency Support</li></ul></li><li>Chapter 16<ul style="list-style-type: none"><li><a href="#">Section 16.3</a>: Updated Intel 4 Series Express Chipset package drawing in <a href="#">Figure 25</a></li></ul></li><li>Chapter 19<ul style="list-style-type: none"><li><a href="#">Section 19.1.36</a>: Added GM47 GFX Software and DDR2 Capability and updated DDR3 and FSB Capability in CAPID Register</li></ul></li><li>Chapter 20<ul style="list-style-type: none"><li><a href="#">Section 20.4.4</a>: Updated RST_EVNT definition in SLFRCS Register</li></ul></li><li>Chapter 21<ul style="list-style-type: none"><li><a href="#">Section 21.1.5</a>: Added conversion A-1 stepping revision ID in RID Register</li></ul></li><li>Chapter 23<ul style="list-style-type: none"><li><a href="#">Section 23.1.1</a>: Corrected Intel ME Identifier Register default value</li></ul></li></ul>	December 2008



Document Number	Revision Number	Description	Date
320122	004	<ul style="list-style-type: none"><li>• Chapter 1<ul style="list-style-type: none"><li>— Removed Section 1.3 GM47 Feature Support</li></ul></li><li>• Chapter 10<ul style="list-style-type: none"><li>— <a href="#">Section 10.1</a>: Removed GM47 in <a href="#">Table 23</a></li><li>— <a href="#">Section 10.1</a>: Removed GM47 <math>I_{VCC}</math> in <a href="#">Table 24</a></li><li>— <a href="#">Section 10.1</a>: Removed GM47 <math>I_{VCC\_AXF}</math> specification in <a href="#">Table 27</a></li></ul></li><li>• Chapter 13<ul style="list-style-type: none"><li>— <a href="#">Section 13.3</a>: Removed GM47 GMCH Clock Frequency Support</li></ul></li><li>• Chapter 19<ul style="list-style-type: none"><li>— <a href="#">Section 19.1.36</a>: Removed GM47 GFX Software and DDR2 Capability</li></ul></li></ul>	January 2009
320122	005	<ul style="list-style-type: none"><li>• Chapter 1<ul style="list-style-type: none"><li>— <a href="#">Section 1.1.1</a>: Updated processor list for PM45</li><li>— <a href="#">Section 1.2.1</a>: Updated processor list for GM45</li><li>— <a href="#">Section 1.2.2</a>: Added DDR3 667 MHz support at FSB 667 MHz only for GM45</li><li>— <a href="#">Section 1.3.1</a>: Updated processor list for GS45</li><li>— <a href="#">Section 1.3.4</a>: Added ICH9 Support for GS45</li><li>— <a href="#">Section 1.4.1</a>: Updated processor list for GL40</li><li>— <a href="#">Section 1.4.2</a>: Added 800MHz support for DDR2/DDR3 and DDR3 667 MHz support at FSB 667 MHz only for GL40</li><li>— <a href="#">Section 1.4.5</a>: Updated list of features not supported</li></ul></li><li>• Chapter 5<ul style="list-style-type: none"><li>— <a href="#">Section 5.1</a>: Rearranged the contents and added a note that mixed CAS latency memory combination is not supported</li><li>— <a href="#">Section 5.1</a>: Added DDR2 2 Gb memory support in <a href="#">Table 8</a></li><li>— <a href="#">Section 5.1</a>: Added DDR3 2 Gb memory support in <a href="#">Table 9</a></li></ul></li><li>• Chapter 6<ul style="list-style-type: none"><li>— <a href="#">Section 6.2</a>: Updated configuration strap controls in <a href="#">Table 15</a></li></ul></li><li>• Chapter 8<ul style="list-style-type: none"><li>— <a href="#">Section 8.4</a>: Removed Embedded DP support in <a href="#">Table 17</a></li></ul></li><li>• Chapter 9<ul style="list-style-type: none"><li>— Removed Section 9.10 PWROK Timing Requirements for Power-Up, Resume from S3</li><li>— Removed Section 9.11 GFX VR Timing Requirements for Power-Up, Resume from Sx</li></ul></li><li>• Chapter 10<ul style="list-style-type: none"><li>— <a href="#">Section 10.1</a>: Updated GM45 <math>I_{VCC\_AXG}</math> specification in <a href="#">Table 24</a></li></ul></li><li>• Chapter 13<ul style="list-style-type: none"><li>— <a href="#">Section 13.3</a>: Removed GM47 GMCH Clock Frequency Support, updated GM45 and GL40 Memory Clock Frequency Support and added note</li></ul></li><li>• Chapter 19<ul style="list-style-type: none"><li>— <a href="#">Section 19.1.36</a>: Removed 667 MHz Render Clock definition from CAPID Register</li></ul></li></ul>	February 2009



Document Number	Revision Number	Description	Date
320122	006	<ul style="list-style-type: none"><li>• Chapter 1<ul style="list-style-type: none"><li>— <a href="#">Section 1.3.1</a>: Updated FSB Support for GS45</li><li>— <a href="#">Section 1.5</a>: Added GS40 Feature Support</li></ul></li><li>• Chapter 5<ul style="list-style-type: none"><li>— <a href="#">Section 5.1</a>: Added GS40 memory support note</li></ul></li><li>• Chapter 10<ul style="list-style-type: none"><li>— <a href="#">Section 10</a>: Added GS40 storage temperature and updated notes in <a href="#">Table 22</a></li><li>— <a href="#">Section 10.1</a>: Added GS40 TDP numbers in <a href="#">Table 23</a></li><li>— <a href="#">Section 10.1</a>: Updated notes for GS40 Power Characteristics in <a href="#">Table 24</a></li><li>— <a href="#">Section 10.1</a>: Updated notes for GS40 Vcc Auxiliary Power Characteristics in <a href="#">Table 27</a></li></ul></li><li>• Chapter 12<ul style="list-style-type: none"><li>— <a href="#">Section 12</a>: Updated signal groups for DC RSTIN#, PWROK, and CL_PWROK in <a href="#">Table 28</a></li><li>— <a href="#">Section 12.1</a>: Added V<sub>IL</sub> and V<sub>IH</sub> and updated DC Characteristics for CL_VREF, SM_PWROK, HDA interface in <a href="#">Table 29</a></li></ul></li><li>• Chapter 13<ul style="list-style-type: none"><li>— <a href="#">Section 13.3</a>: Added GS40 to GMCH Host/Memory/Graphics Core Clock Frequency Support matrix</li></ul></li><li>• Chapter 19<ul style="list-style-type: none"><li>— <a href="#">Section 19.1.36</a>: Added GS40 GFX Software Capability ID in CAPID Register</li></ul></li></ul>	June 2009

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# 1 Introduction

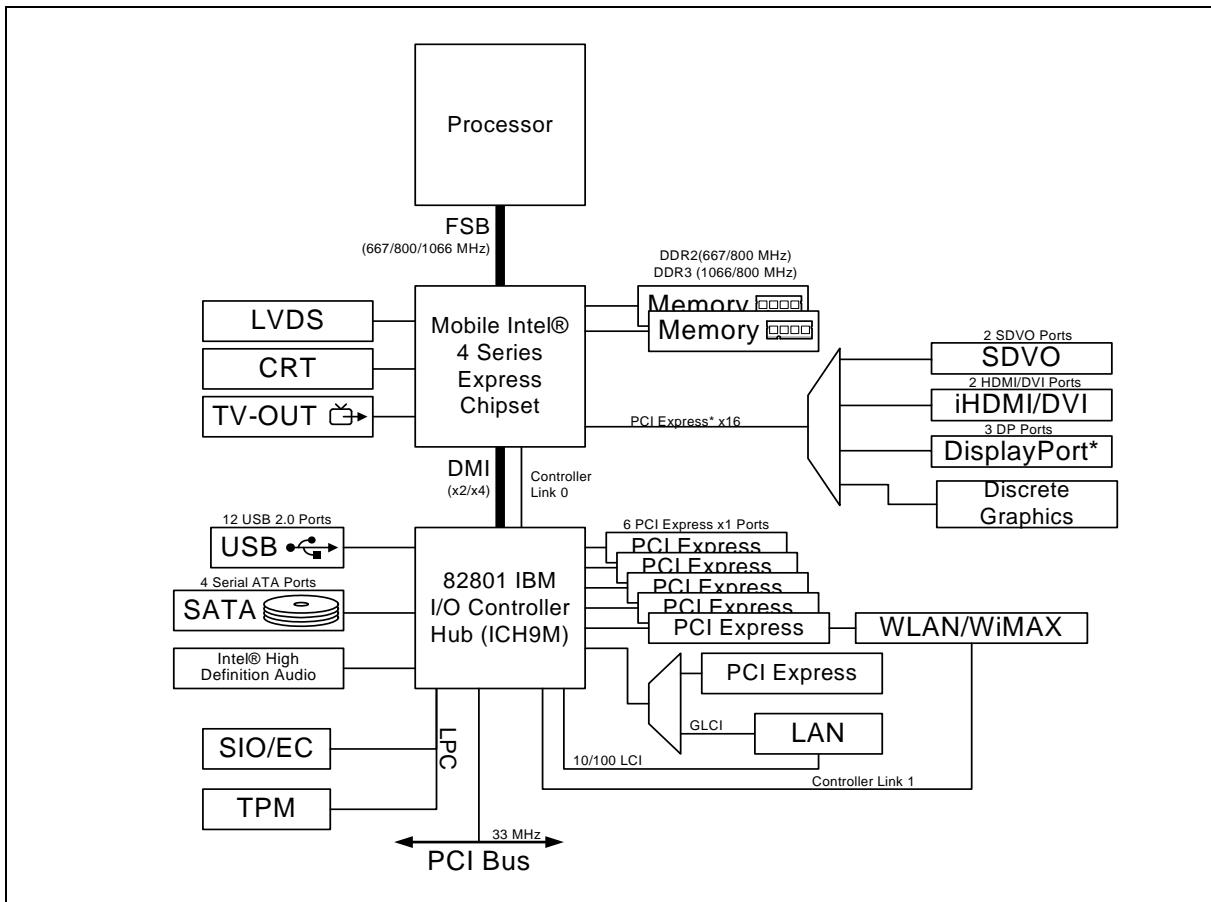
This document provides specifications for the Mobile Intel® 4 Series Express Chipset Family. In this document, the Mobile Intel 4 Series Express Chipset Family is referred to as the GMCH.

The GMCH manages the flow of information between various components through four main interfaces:

- Front Side Bus (FSB)
- System Memory Interface (DDR2/DDR3)
- Graphics Interfaces (CRT, TV-Out, LVDS, SDVO, DisplayPort\*, iHDMI\* (DVI also) and PCI Express Graphics)
- Direct Management Interface (DMI)

Figure 1 provides a block diagram of the GMCH.

**Figure 1. Block Diagram**





## 1.1 Intel® PM45 Express Chipset Feature Support

### 1.1.1 Processor

- Intel® Core™2 Extreme, Intel® Core™2 Quad, and Intel® Core™2 Duo mobile processors based on the 45-nm process
- 667-MHz, 800-MHz and 1066-MHz FSB
- Source synchronous double-pumped (2x) address
- Source synchronous quad-pumped (4x) data
- Support for Dynamic FSB Frequency Switching
- Other key features are:
  - Support for Intel® Trusted Execution Technology (Intel® TXT) commands and signaling
  - Support for Data Bus Inversion (DBI)
  - Support for Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) (DMA)
  - Support for Message Signaled Interrupt (MSI)
  - 36-bit interface to addressing, allowing the CPU to access the entire 64 GB of the GMCH's memory address space
  - 12-deep, in-order queue to pipeline FSB commands
  - AGTL+ bus driver with integrated AGTL termination resistors

### 1.1.2 System Memory

- Supports DDR2 and DDR3 SDRAM
- Support for DDR2 at 667 MHz and 800 MHz
- Support for DDR3 at 667, 800 and 1066 MHz
- One SO-DIMM connector (or memory module) per channel
- Two Memory Channel Configurations supported
  - Dual-channel Symmetric (with Interleaved access)
  - Dual-channel Asymmetric (with or without Intel® Flex Memory Technology)
- 8-GB maximum memory support
- 64-bit wide per channel
- 256-Mb, 512-Mb, 1-Gb, and 2-Gb memory technologies supported
- Support for x8 and x16 DDR2 and DDR3 devices
- Support for DDR2/DDR3 On-Die Termination (ODT)
- Supports partial writes to memory using data mask signals (DM)
- No support for Fast Chip Select mode
- No support for ECC
- No support for 1N operation

### 1.1.3 Discrete Graphics Using PCI Express\* Graphics Attach Port

- One, 16-lane (x16) PCI Express port for external PCI Express-based graphics card



#### **1.1.4 Direct Management Interface (DMI)**

- Chip-to-chip interface between GMCH and ICH
- Configurable as x2 or x4 DMI lanes
- x2 and x4 lane-reversal support
- DMI Polarity inversion support
- 2-GB/s (1 GB/s each direction), point-to-point interface to ICH
- 32-bit downstream address
- DMI asynchronously coupled to core
- APIC and MSI interrupt messaging support
- Supports SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters

#### **1.1.5 Power Management**

- Supports ACPI 3.0
- S-States: S0, S3, S4, S5
- C-States: C0, C1/C1E, C2/C2E, C3, C4/C4E, Intel® Enhanced Deeper Sleep and Deep Power Down technology (code named C6) states
- M-States: M0, M1, M-off
- PCI Express Link States: L0, L0s, L1, L2/L3 ready, L3
- H\_CPLUSLP# output
- H\_DPWR# support
- Intel® Rapid Memory Power Management (Intel® RMPM)
- Dynamic Memory Rank power-down

#### **1.1.6 Thermal Management**

- Programmable Aux Trip point notification (via HW pin) support
- Support for External Thermal Sensor

#### **1.1.7 Intel® Trusted Execution Technology (Intel® TxT)**

- Memory protection from bus masters via No-DMA support (in a secure environment)

#### **1.1.8 Intel® Virtualization Technology (Intel® VT) DMA**

- DMA remapping support via a GMCH Remapping engine
- Chipset support for hardware address translation GPA (Guest Physical Address) to HPA (Host Physical Address)
- Accelerated DMA translation performance via GMCH cache support
- Protected Low-Memory Region (<4 GB) and High-Memory Region (>4 GB) to securely store VMM data



### 1.1.9 Intel® Active Management Technology (Intel® AMT) 4.0

The GMCH supports Intel® Active Management Technology 4.0 (Intel® AMT) with both wired and wireless LAN support via a Controller Link interface to ICH for extended manageability functionality.

An Intel AMT engine integrated within the GMCH combines hardware and software solutions to provide:

- Remote Asset Management
- Remote Diagnosis and Repair
- Remote Agent Presence
- Wireless OOB Management
- Circuit Breaker Network Isolation
- Mobile Power Management Policies
- 3rd Party Non-Volatile Storage

Controller link is the Intel® Management Engine (ME) link between the GMCH and ICH.

### 1.1.10 Integrated Trusted Platform Module (ITPM)

The GMCH supports an Integrated Trusted Platform Module (ITPM) 1.2 unit within the Intel Management Engine subsystem of the platform. ITPM support can be enabled/disabled via a strapping option.

The GMCH executes validated TPM firmware out of a portion of hardware isolated DDR DRAM.

### 1.1.11 Package

- 1329-ball FCBGA
- Package Size: 34 mm x 34 mm
- Ball pitch: 0.7 mm

## 1.2 Intel® GM45 Express Chipset Feature Support

All features supported by Intel® PM45 Express Chipset are supported by Intel GM45 Express Chipset unless otherwise noted below. Additional features are listed below.

The GM variant can be enabled to support either integrated graphics or external graphics. When external graphics is enabled, the x16 PCI Express Graphics attach port is utilized, and the internal graphics ports are disabled.

### 1.2.1 Processor

- Intel® Pentium® and Intel® Celeron® mobile processors on 45nm technology
- Intel® Celeron® T1700, T1600, 585 and 575 processors on 65nm technology

### 1.2.2 System Memory

- Support for DDR3 at 667MHz when FSB at 667MHz only



### 1.2.3 PCI Express Graphics Attach Port

- One 16-lane (x16) PCI Express port for external PCI Express-based graphics card
  - May also be configured as a PCI Express x1 port for video capture

### 1.2.4 Internal Graphics

- Intel Gen 5.0 integrated graphics engine with ten, fully-programmable cores
- 533-MHz core render clock @ 1.05-V core voltage
- Supports iHDMI/DVI, DP, TV-Out, LVDS, CRT and SDVO
- Intel® Dynamic Video Memory Technology (Intel® DVMT 5.0)
- Video Capture via x1 concurrent PCI Express port
- PAVP (Protected Audio-Video Path) support for Protected Intel® HD Audio (Video and Audio) Playback
- High performance MPEG-2 decoding
- WMV9 (VC-1) and H.264 (AVC) support
- Hardware acceleration for MPEG2 VLD/iDCT
- Microsoft DirectX\*10 support
- Blu-ray\* support @ 40 Mb/s
- Hardware motion compensation
- Intermediate Z in classic rendering

#### 1.2.4.1 Dual-Channel LVDS

- 25-112-MHz single/dual-channel
  - Single channel LVDS interface support: 1 x 18 bpp OR 1 x 24 bpp (Type 1 only, compatible with VESA LVDS color mapping)
  - Dual-channel LVDS interface support: 2 x 18 bpp OR 2 x 24 bpp panel support
    - TFT panel type supported
- Pixel dithering for 18-bit TFT panel to emulate 24-bpp true color displays
- Panel Fitting, Panning and Center mode supported
- Standard Panel Working Group (SPWG) v.3.5 specification compliant
- Spread spectrum clocking support
- Panel power sequencing support
- Integrated PWM interface for LCD backlight inverter control

#### 1.2.4.2 DisplayPort\* (DP)

The GMCH supports three DP ports muxed on the PCI Express interface

- 1.62 Gb/s and 2.7 Gb/s
- 1, 2 or 4 data lanes
- 8b 10b coding
- Hot-Plug detect support
- HDCP support



#### 1.2.4.3 Integrated HDMI (iHDMI)\*

- DVI also supported on same interface
- Single TMDS Link
- 8 bpc only supporting RGB - no YCrCb4:4:4 and YCrCb4:2:2 support
- Data Island Packets including null, AVI Infoframe, audio samples and more
- Video support for CEA modes 480i/p, 576i/p, 720p, 1080i/p and PC modes through dot clock
- HDMI Source only – not a receiver device
- HDCP support
- Support for HDMI repeaters
- Intel HD Audio support
  - Integrated Intel HD Audio codec
  - Dolby\* AC3 compress, Dolby\* Digital, Dolby\* DTS (full support)
  - PCM audio support

#### 1.2.4.4 SDVO Ports

- Two SDVO ports supported
  - SDVO pins are muxed onto the PCI Express Graphics-attach port pins
  - DVI 1.0 support for External Digital Monitor
  - Downstream HDCP Support but no upstream HDCP support
  - Display Hot-Plug support
- Supports appropriate external SDVO components (HDMI, DVI, LVDS, TV-Out)
- I<sup>2</sup>C channel provided for control

#### 1.2.4.5 Analog CRT

- Integrated 300-MHz DAC
- Analog monitor support up to QXGA
- Support for CRT Hot-Plug

#### 1.2.4.6 TV-Out

- Macrovision\* not supported
- Overscaling
- NTSC/PAL
- Component, S-Video and Composite Output Interfaces
- HDTV graphics mode support



## 1.2.5 Power Management

- Graphics Display Adapter States: D0, D3
- Intel® Display Power Saving Technology (Intel® DPST) 4.0
- Graphics Render Standby Mode
  - Render Standby Voltages: RS2 (0.55 V)
- Graphics Render Thermal Throttling
- Support for Frame Buffer Compression 2 (FBC2)

## 1.3 Intel® GS45 Express Chipset Feature Support

All features supported by the Intel GM45 Express chipset are supported by Intel GS45 Express chipset unless otherwise noted below. Additional features are listed below.

### 1.3.1 Processor

- Intel® Core™2 Duo, Intel® Core™2 Solo and Intel® Celeron® mobile processors based on the 45-nm process
- Low power configuration: 800 MHz FSB support
- High performance configuration: 800- and 1066- MHz FSB Support

### 1.3.2 Memory

- Low-power configuration
  - Support for DDR2 at 667 MHz
  - Support for DDR3 at 667 MHz and 800 MHz
- High performance configuration
  - Support for DDR2 at 667 MHz and 800 MHz
  - Support for DDR3 at 667 MHz, 800 MHz and 1066 MHz

### 1.3.3 Internal Graphics

- Low-power configuration: 320-MHz core render clock at 1.05-V core voltage
- High performance configuration: Same as Intel GM45 Express chipset

### 1.3.4 ICH Support

- Support for ICH9M-SFF-Enhanced only

### 1.3.5 Package

- 1363 Ball FCBGA
- Package Size: 27 mm x 25 mm
- 0.593-mm minimum ball pitch



## 1.4 Intel® GL40 Express Chipset Feature Support

All features supported by the Intel GM45 Express chipset are supported by Intel GL40 Express chipset unless otherwise noted below. Additional features are also listed below.

### 1.4.1 Processor

- Intel® Pentium® and Intel® Celeron® mobile processors based on the 45-nm process
- Intel® Celeron® Processors T1700, T1600, 585 and 575
- 667 MHz and 800 MHz<sup>1</sup> FSB support

### 1.4.2 System Memory

- Support for DDR2 at 667 MHz and 800 MHz
- Support for DDR3 at 667 MHz when FSB at 667 MHz only
- Support for DDR3 at 800 MHz
- Maximum memory supported: 4 GB

### 1.4.3 Internal Graphics

- 400-MHz core render clock at 1.05-V core voltage

### 1.4.4 ICH Support

- Support for ICH9M (base) only

### 1.4.5 Power Management

- No support for
  - Intel DPST 4.0
  - Graphics Render Standby Modes
  - Intel® Display Refresh Rate Switching
  - FSB Dynamic Frequency Switching

### 1.4.6 Unsupported Features

- Discrete Graphics using PCI Express Graphics Attach Port
- ITPM
- Intel VT DMA
- Intel TxT
- Intel AMT

## 1.5 Intel® GS40 Express Chipset Feature Support

All features supported by the Intel GM45 Express chipset are supported by Intel GS40 Express chipset unless otherwise noted below. Additional features are also listed below.



### **1.5.1 Processor**

- Intel® Celeron® mobile processor 723
- 800 MHz FSB support

### **1.5.2 System Memory**

- Support for DDR2 at 667 MHz and 800 MHz
- Support for DDR3 at 667 MHz when FSB at 667 MHz only
- Support for DDR3 at 800 MHz
- Maximum memory supported: 4 GB

### **1.5.3 Internal Graphics**

- 400-MHz core render clock at 1.05-V core voltage

### **1.5.4 ICH Support**

- Support for ICH9M SFF Enhanced only

### **1.5.5 Power Management**

- No support for
  - Intel DPST 4.0
  - Graphics Render Standby Modes
  - Intel® Display Refresh Rate Switching
  - FSB Dynamic Frequency Switching

### **1.5.6 Unsupported Features**

- Discrete Graphics using PCI Express Graphics Attach Port
- ITPM
- Intel VT DMA
- Intel TxT
- Intel AMT



## 1.6 Reference Documents

Document	Document No./Location
<i>Mobile Intel® 4 Series Express Chipset Family Specification Update</i>	<a href="http://www.intel.com/design/mobile/specupdt/32012301.pdf">http://www.intel.com/design/mobile/specupdt/32012301.pdf</a>
<i>Intel® Core™2 Duo Mobile Processor and Intel® Core™2 Extreme Mobile Processor on 45nm Technology Datasheet</i>	<a href="http://download.intel.com/design/mobile/datashts/32012001.pdf">http://download.intel.com/design/mobile/datashts/32012001.pdf</a>
<i>Intel® Core™2 Duo Mobile Processor and Intel® Core™2 Extreme Mobile Processor on 45nm Technology Specification Update</i>	<a href="http://download.intel.com/design/mobile/specupdt/32012101.pdf">http://download.intel.com/design/mobile/specupdt/32012101.pdf</a>
<i>Intel® I/O Controller Hub 9 (ICH9) Family Datasheet</i>	<a href="http://www.intel.com/Assets/PDF/datasheet/316972.pdf">http://www.intel.com/Assets/PDF/datasheet/316972.pdf</a>
<i>Intel® I/O Controller Hub 9 (ICH9) Family Specification Update</i>	<a href="http://www.intel.com/Assets/PDF/specupdate/316973.pdf">http://www.intel.com/Assets/PDF/specupdate/316973.pdf</a>
<i>Advanced Configuration and Power Interface Specification 3.0</i>	<a href="http://www.acpi.info/">http://www.acpi.info/</a>
<i>PCI Local Bus Specification 3.0</i>	<a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>
<i>PCI Express Specification 1.1</i>	<a href="http://www.pcisig.com">http://www.pcisig.com</a>
<i>Standard Panel Working Group (SPWG) v.3.5 Specification</i>	<a href="http://www.spwg.org/">http://www.spwg.org/</a>
<i>JEDEC Double Data Rate 2 (DDR2) SDRAM Specification</i>	<a href="http://www.jedec.com">http://www.jedec.com</a>
<i>JEDEC Double Data Rate 3 (DDR3) SDRAM Specification</i>	<a href="http://www.jedec.com">http://www.jedec.com</a>
<i>PCI Express Specification 1.0a Mobile Graphics Low Power Addendum to the PCI Express Base Specification Revision 1.0</i>	<a href="http://www.pcisig.org">http://www.pcisig.org</a>
<i>VESA Specification</i>	<a href="http://www.vesa.org">http://www.vesa.org</a>
<i>TIA/EIA-644 Standard</i>	<a href="http://www.tiaonline.org">http://www.tiaonline.org</a>

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## 2 Signal Description

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This section describes the GMCH signals. These signals are arranged in functional groups according to their associated interface. The following notations are used to describe the signal type:

Notations	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

Signal	Description
AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The GMCH integrates AGTL+ termination resistors, and supports $V_{TT} = 1.05$ V.
PCI Express	PCI Express interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
CMOS	CMOS buffers. 1.5-V tolerant.
HVCMOS	High-voltage CMOS buffers. 3.3-V tolerant.
LVCMOS	Low-voltage CMOS buffers. $V_{TT}$ tolerant.
COD	CMOS Open Drain buffers. 3.3-V tolerant.
SSTL-1.8	Stub Series Termination Logic: These are 1.8-V capable buffers.
SSTL-1.5	Stub Series Termination Logic: These are 1.5-V capable buffers.
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.
LVDS	Low-Voltage Differential Signal Interface.
Ref	Voltage reference signal.

**Note:** System Address and Data Bus signals are logically inverted signals. The actual values are inverted of what appears on the system bus. This must be considered and the addresses and data bus signals must be inverted inside the GMCH. All processor control signals follow normal convention: A 0 indicates an active level (low-voltage), and a 1 indicates an active level (high-voltage).

**Note:** All pins marked RESERVED should be left NC, unless otherwise specified.

### 2.1 Host Interface

Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the host bus ( $V_{TT}$ ).



## 2.1.1 Host Interface Signals

(Sheet 1 of 4)

Signal Name	Type	Description						
H_A# [35:3]	I/O AGTL+ 2X	<b>Host Address Bus:</b> HA# [35:3] connects to the processor address bus. During processor cycles the HA# [35:3] are inputs. The GMCH drives HA# [35:3] during snoop cycles on behalf of PCI Express/Internal Graphics or ICH. HA# [35:3] are transferred at 2x rate. Note that the address is inverted on the processor bus.						
H_ADS#	I/O AGTL+	<b>Host Address Strobe:</b> The system bus owner asserts H_ADS# to indicate the first of two cycles of a request phase. The GMCH can also assert this signal for snoop cycles and interrupt messages.						
H_ADSTB# [1:0]	I/O AGTL+ 2X	<b>Host Address Strobe:</b> HA# [31:3] connects to the processor address bus. During processor cycles, the source synchronous strobes are used to transfer HA# [35:3] and HREQ# [4:0] at the 2x transfer rate. <table border="1"><thead><tr><th>Strobe</th><th>Address Bits</th></tr></thead><tbody><tr><td>HADSTB#0</td><td>HA# [15:3], HREQ# [4:0]</td></tr><tr><td>HADSTB#1</td><td>HA# [35:16]</td></tr></tbody></table>	Strobe	Address Bits	HADSTB#0	HA# [15:3], HREQ# [4:0]	HADSTB#1	HA# [35:16]
Strobe	Address Bits							
HADSTB#0	HA# [15:3], HREQ# [4:0]							
HADSTB#1	HA# [35:16]							
H_AVREF H_DVREF	I A	<b>Host Reference Voltage:</b> Reference voltage input for the Data, Address, and Common clock signals of the Host AGTL+ interface						
H_BNR#	I/O AGTL+	<b>Host Block Next Request:</b> Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the processor bus pipeline depth.						
H_BPRI#	O AGTL+	<b>Host Bus Priority Request:</b> The GMCH is the only Priority Agent on the system bus. It asserts this signal to get the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the H_LOCK# signal was asserted.						
H_BREQ#	I/O AGTL+	<b>Host Bus Request:</b> The GMCH pulls the processor bus H_BREQ# signal low during H_CPURST#. The signal is sampled by the processor on the active-to-inactive transition of H_CPURST#. H_BREQ# should be tri-stated after the hold time requirement has been satisfied.						
H_CPURST#	O AGTL+	<b>Host CPU Reset:</b> The H_CPURST# pin is an output from the GMCH. The GMCH asserts H_CPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. H_CPURST# allows the processor to begin execution in a known state.						



(Sheet 2 of 4)

Signal Name	Type	Description										
H_CPUSLP#	O LVCMOS	<b>Host CPU Sleep:</b> When asserted in the Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. (This is a CMOS type buffer with V <sub>TT</sub> - <b>not</b> 3.3 V.)										
H_D# [63:0]	I/O AGTL+ 4X	<b>Host Data:</b> These signals are connected to the processor data bus. HD [63:0]# are transferred at 4x rate. Note that the data signals are inverted on the processor bus depending on the HDINV# [3:0] signals.										
H_DBSY#	I/O AGTL+	<b>Host Data Bus Busy:</b> Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.										
H_DEFER#	O AGTL+	<b>Host Defer:</b> Signals that the GMCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.										
H_DINV# [3:0]	I/O AGTL+	<b>Host Dynamic Bus Inversion:</b> Driven along with the HD [63:0]# signals. Indicates if the associated signals are inverted or not. HDINV [3:0]# are asserted such that the number of data bits driven electrically low (low-voltage) within the corresponding 16-bit group never exceeds 8. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>H_DINV#</th> <th>Data Bits</th> </tr> </thead> <tbody> <tr> <td>H_DINV#3</td> <td>H_D# [63:48]</td> </tr> <tr> <td>H_DINV#2</td> <td>H_D# [47:32]</td> </tr> <tr> <td>H_DINV#1</td> <td>H_D# [31:16]</td> </tr> <tr> <td>H_DINV#0</td> <td>H_D# [15:0]</td> </tr> </tbody> </table>	H_DINV#	Data Bits	H_DINV#3	H_D# [63:48]	H_DINV#2	H_D# [47:32]	H_DINV#1	H_D# [31:16]	H_DINV#0	H_D# [15:0]
H_DINV#	Data Bits											
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H_DINV#2	H_D# [47:32]											
H_DINV#1	H_D# [31:16]											
H_DINV#0	H_D# [15:0]											
H_DPWR#	I/O AGTL+	<b>Host Data Power:</b> Used by GMCH to indicate that a data return cycle is pending within 2 H_CLK cycles or more. Processor uses this signal during a read-cycle to activate the data input buffers in preparation for H_DRDY# and the related data.										
H_DRDY#	I/O AGTL+	<b>Host Data Ready:</b> Asserted for each cycle that data is transferred.										
H_DSTBP# [3:0] H_DSTBN# [3:0]	I/O AGTL+ 4X	<b>Host Differential Host Data Strobes:</b> The differential source synchronous strobes are used to transfer HD [63:0]# and HDINV# [3:0] at the 4x transfer rate. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Strobe</th> <th>Data Bits</th> </tr> </thead> <tbody> <tr> <td>H_DSTBP#3, H_DSTBN#3</td> <td>H_D# [63:48], H_DINV# [3]</td> </tr> <tr> <td>H_DSTBP#2, H_DSTBN#2</td> <td>H_D# [47:32], H_DINV# [2]</td> </tr> <tr> <td>H_DSTBP#1, H_DSTBN#1</td> <td>H_D# [31:16], H_DINV# [1]</td> </tr> <tr> <td>H_DSTBP#0, H_DSTBN#9</td> <td>H_D# [15:0], H_DINV# [0]</td> </tr> </tbody> </table>	Strobe	Data Bits	H_DSTBP#3, H_DSTBN#3	H_D# [63:48], H_DINV# [3]	H_DSTBP#2, H_DSTBN#2	H_D# [47:32], H_DINV# [2]	H_DSTBP#1, H_DSTBN#1	H_D# [31:16], H_DINV# [1]	H_DSTBP#0, H_DSTBN#9	H_D# [15:0], H_DINV# [0]
Strobe	Data Bits											
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H_DSTBP#2, H_DSTBN#2	H_D# [47:32], H_DINV# [2]											
H_DSTBP#1, H_DSTBN#1	H_D# [31:16], H_DINV# [1]											
H_DSTBP#0, H_DSTBN#9	H_D# [15:0], H_DINV# [0]											



(Sheet 3 of 4)

Signal Name	Type	Description																		
H_HIT#	I/O AGTL+	<b>Host Hit:</b> Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with H_HITM# by the target to extend the snoop window.																		
H_HITM#	I/O AGTL+	<b>Host Hit Modified:</b> Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with H_HIT# to extend the snoop window.																		
H_LOCK#	I AGTL+	<b>Host Lock:</b> All processor bus cycles sampled with the assertion of H_LOCK# and H_ADS#, until the negation of H_LOCK# must be atomic.																		
H_RCOMP	I/O A	<b>Host RCOMP:</b> Used to calibrate the Host AGTL+ I/O buffers.																		
H_REQ# [4:0]	I/O AGTL+ 2X	<b>Host Request Command:</b> Defines the attributes of the request. H_REQ# [4:0] are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.																		
H_RS# [2:0]	O AGTL+	<b>Host Response Status:</b> Indicates the type of response according to the following the table:  <table border="1"><thead><tr><th>HRS [2:0]#</th><th>Response type</th></tr></thead><tbody><tr><td>000</td><td>Idle state</td></tr><tr><td>001</td><td>Retry response</td></tr><tr><td>010</td><td>Deferred response</td></tr><tr><td>011</td><td>Reserved (not driven by GMCH)</td></tr><tr><td>100</td><td>Hard Failure (not driven by GMCH)</td></tr><tr><td>101</td><td>No data response</td></tr><tr><td>110</td><td>Implicit write back</td></tr><tr><td>111</td><td>Normal data response</td></tr></tbody></table>	HRS [2:0]#	Response type	000	Idle state	001	Retry response	010	Deferred response	011	Reserved (not driven by GMCH)	100	Hard Failure (not driven by GMCH)	101	No data response	110	Implicit write back	111	Normal data response
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111	Normal data response																			
H_SWING	I A	<b>Host Voltage Swing:</b> These signals provide reference voltages used by the H_RCOMP circuits.																		
H_TRDY#	O AGTL+	<b>Host Target Ready:</b> Indicates that the target of the processor transaction can enter the data transfer phase.																		



(Sheet 4 of 4)

Signal Name	Type	Description
THERMTRIP#	O AGTL+	<b>Connects between the Processor, GMCH and the ICH:</b> Assertion of THERMTRIP# (Thermal Trip) indicates the GMCH junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the GMCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the GMCH core junction temperature. To protect the GMCH, its core voltage ( $V_{CC}$ ) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RSTIN# is asserted. While the assertion of the RSTIN# signal will deassert THERMTRIP#, if the GMCH's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted.

## 2.2 Memory Interface

### 2.2.1 Memory Channel A Interface

(Sheet 1 of 2)

Signal Name	Type	Description
SA_BS [2:0]	O SSTL-1.8/1.5	<b>Bank Select:</b> These signals define which banks are selected within each SDRAM rank.
SA_WE#	O SSTL-1.8/1.5	<b>Write Enable Control Signal:</b> Used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM commands.
SA_RAS#	O SSTL-1.8/1.5	<b>RAS Control Signal:</b> Used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SDRAM commands.
SA_CAS#	O SSTL-1.8/1.5	<b>CAS Control Signal:</b> Used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SDRAM commands.
SA_DM [7:0]	O SSTL-1.8/1.5 2x	<b>Data Mask:</b> These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM [7:0] for every data byte lane.
SA_DQS [7:0]	I/O SSTL-1.8/1.5 2x	<b>Data Strobes:</b> SA_DQS [7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS [7:0] and its SA_DQS [7:0]# during read and write transactions.
SA_DQS# [7:0]	I/O SSTL-1.8/1.5 2x	<b>Data Strobe Complements:</b> These are the complementary strobe signals.
SA_DQ [63:0]	I/O SSTL-1.8/1.5 2x	<b>Data Bus:</b> Channel A data signal interface to the SDRAM data bus.
SA_MA [14:0]	O SSTL-1.8/1.5	<b>Memory Address:</b> These signals are used to provide the multiplexed row and column address to the SDRAM.



(Sheet 2 of 2)

Signal Name	Type	Description
SA_CK [1:0]	O SSTL-1.8/1.5	<b>SDRAM Differential Clock:</b> Channel A SDRAM Differential Clock signal-pair. The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM.
SA_CK# [1:0]	O SSTL-1.8/1.5	<b>SDRAM Inverted Differential Clock:</b> Channel A SDRAM Differential Clock signal-pair complement.
SA_CKE [1:0]	O SSTL-1.8/1.5	<b>Clock Enable:</b> (1 per Rank) used to: <ul style="list-style-type: none"><li>Initialize the SDRAMs during power-up</li><li>Power-down SDRAM ranks</li><li>Place all SDRAM ranks into and out of self-refresh during STR.</li></ul>
SA_CS# [1:0]	O SSTL-1.8/1.5	<b>Chip Select:</b> (1 per Rank): Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
SA_ODT [1:0]	O SSTL-1.8/1.5	<b>On Die Termination:</b> Active Termination Control.

## 2.2.2 Memory Channel B Interface

(Sheet 1 of 2)

Signal Name	Type	Description
SB_BS [2:0]	O SSTL-1.8/1.5	<b>Bank Select:</b> These signals define which banks are selected within each SDRAM rank.
SB_WE#	O SSTL-1.8/1.5	<b>Write Enable Control Signal:</b> Used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM commands.
SB_RAS#	O SSTL-1.8/1.5	<b>RAS Control Signal:</b> Used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SDRAM commands.
SB_CAS#	O SSTL-1.8/1.5	<b>CAS Control Signal:</b> Used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SDRAM commands.
SB_DM [7:0]	O SSTL-1.8/1.5 2x	<b>Data Mask:</b> These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM [7:0] for every data byte lane.
SB_DQS# [7:0]	I/O SSTL-1.8/1.5 2x	<b>Data Strobe Complements:</b> These are the complementary strobe signals.
SB_DQS [7:0]	I/O SSTL-1.8/1.5 2x	<b>Data Strobes:</b> SB_DQS [7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS [7:0] and its SB_DQS [7:0]# during read and write transactions.



(Sheet 2 of 2)

Signal Name	Type	Description
SB_MA [14:0]	O SSTL-1.8/1.5	<b>Memory Address:</b> These signals are used to provide the multiplexed row and column address to the SDRAM.
SB_DQ [63:0]	I/O SSTL-1.8/1.5 2x	<b>Data Bus:</b> Channel B data signal interface to the SDRAM data bus.
SB_CK [1:0]	O SSTL-1.8/1.5	<b>SDRAM Differential Clock:</b> Channel B SDRAM Differential Clock signal-pair. The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM.
SB_CK# [1:0]	O SSTL-1.8/1.5	<b>SDRAM Inverted Differential Clock:</b> Channel B SDRAM Differential Clock signal-pair complement.
SB_CKE [1:0]	O SSTL-1.8/1.5	<b>Clock Enable</b> (1 per Rank): Used to initialize the SDRAMs during power-up, power-down SDRAM ranks, place all SDRAM ranks into and out of self-refresh during STR.
SB_CS# [1:0]	O SSTL-1.8/1.5	<b>Chip Select</b> (1 per Rank): Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
SB_ODT [1:0]	O SSTL-1.8/1.5	<b>On Die Termination:</b> Active Termination Control

### 2.2.3 Memory Reference and Compensation

Signal Name	Type	Description
SM_RCOMP	I A	System Memory Impedance Compensation
SM_RCOMP#	I A	System Memory Impedance Compensation
SM_RCOMP_VO_H	I A	System Memory Pull-up Impedance Compensation
SM_RCOMP_VOL	I A	System Memory Pull-down Impedance Compensation
SM_VREF	I A	<b>System Memory Reference Voltage:</b> For all data and data strobe signals.
SM_REXT	IO A	Constant Circuit Reference for Clocks



## 2.3 PCI Express-Based Graphics Interface Signals

Unless otherwise specified, these signals are AC coupled.

Signal Name	Type	Description
PEG_COMPI	I A	PCI Express Graphics Input Current Compensation
PEG_COMPO	I A	PCI Express Graphics Output Current and Resistance Compensation
PEG_RX [15:0] PEG_RX# [15:0]	I PCI Express*	PCI Express Graphics Receive Differential Pair
PEG_TX [15:0] PEG_TX# [15:0]	O PCI Express	PCI Express Graphics Transmit Differential Pair

### 2.3.1 DisplayPort (DP), iHDMI and SDVO on PCI Express Based Graphics

The DP, iHDMI and SDVO interfaces are multiplexed on to the GMCH PCI Express Interface. See [Chapter 6](#) for more details.

## 2.4 DMI – GMCH to ICH Serial Interface

Signal Name	Type	Description
DMI_RXN [3:0] DMI_RXP [3:0]	I PCI Express*	<b>DMI Input from ICH:</b> Direct Media Interface receive differential pair.
DMI_TXN [3:0] DMI_TXP [3:0]	O PCI Express	<b>DMI Output to ICH:</b> Direct Media Interface transmit differential pair.



## 2.5 Integrated Graphics Interface Signals

### 2.5.1 CRT DAC Signals

Signal Name	Type	Description
CRT_RED	O A	<b>RED Analog Video Output:</b> This signal is a CRT analog video output from the internal color palette DAC.
CRT_GREEN	O A	<b>GREEN Analog Video Output:</b> This signal is a CRT analog video output from the internal color palette DAC.
CRT_BLUE	O A	<b>BLUE Analog Video Output:</b> This signal is a CRT analog video output from the internal color palette DAC.
CRT_TVO_IREF	O A	<b>Resistor Set and TV Reference Current:</b> Set point resistor for the internal color palette DAC and TV reference current.
CRT_VSYNC	O HVCMOS	<b>CRT Vertical Synchronization:</b> This signal is used as the vertical sync (polarity is programmable).
CRT_HSYNC	O HVCMOS	<b>CRT Horizontal Synchronization:</b> This signal is used as the horizontal sync (polarity is programmable) or "sync interval."
CRT_IRTN	O A	<b>Resistor Set:</b> Set point resistor for the internal color palette DAC.

### 2.5.2 Analog TV-out Signals

Signal Name	Type	Description
TV_DCONSEL [1:0]	O COD	<b>TV D-connector Select:</b> Selects appropriate full-voltage discernment signals for TV-out D-connector.
TVA_DAC	O A	<b>TVDAC Channel A Output:</b> Can map to any one of the following: <ul style="list-style-type: none"> <li>• Composite Video, Blank, and Sync (CVBS)</li> <li>• Component Pb</li> </ul>
TVB_DAC	O A	<b>TVDAC Channel B Output:</b> Can map to any one of the following: <ul style="list-style-type: none"> <li>• Svideo - Y</li> <li>• Component Y</li> </ul>
TVC_DAC	O A	<b>TVDAC Channel C Output:</b> Can map to any one of the following: <ul style="list-style-type: none"> <li>• Svideo - C</li> <li>• Component Pr</li> </ul>
TV_RTN	O A	<b>Current Return for TV DAC Channel A/B/C:</b> Connect to ground on board



## 2.5.3 LVDS Signals

Signal Name	Type	Description
<b>LVDS Channel A</b>		
LVDSA_CLK	O LVDS	LVDS Channel A differential clock output – positive
LVDSA_CLK#	O LVDS	LVDS Channel A differential clock output – negative
LVDSA_DATA# [3:0]	O LVDS	LVDS Channel A differential data output – negative
LVDSA_DATA [3:0]	O LVDS	LVDS Channel A differential data output – positive
<b>LVDS Channel B</b>		
LVDSB_CLK	O LVDS	LVDS Channel B differential clock output – positive
LVDSB_CLK#	O LVDS	LVDS Channel B differential clock output – negative
LVDSB_DATA# [3:0]	O LVDS	LVDS Channel B differential data output – negative
LVDSB_DATA [3:0]	O LVDS	LVDS Channel B differential data output – positive
<b>Panel Power and Backlight Control</b>		
L_BKLT_CTRL	O HVCMOS	<b>Panel Backlight Brightness Control:</b> Panel brightness control. This signal is also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal.
L_BKLT_EN	O HVCMOS	<b>LVDS Backlight Enable:</b> Panel backlight enable control. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry.
L_VDD_EN	O HVCMOS	<b>LVDS Panel Power Enable:</b> Panel power control enable control. This signal is also called VDD_DB in the CPIS specification and is used to control the VDC source to the panel logic.
<b>LVDS Reference Signals</b>		
LVDS_IBG	I/O Ref	LVDS Reference Current
LVDS_VBG	O A	Leave as NC
LVDS_VREFH	I Ref	Must Be Connected to Ground
LVDS_VREFL	I Ref	Must Be Connected to Ground



## 2.5.4 Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	Description
CRT_DDC_CLK	I/O COD	CRT DDC Clock Monitor Control Support
CRT_DDC_DATA	I/O COD	CRT DDC Data Monitor Control Support
L_CTRL_CLK	I/O COD	Control Signal (Clock) for External SSC clock chip control – optional
L_CTRL_DATA	I/O COD	Control signal (data) for External SSC clock chip control – optional
L_DDC_CLK	I/O COD	EDID support for flat panel display
L_DDC_DATA	I/O COD	EDID support for flat panel display
SDVO_CTRLCLK	I/O COD	HDMI Port B Control Clock (This pin is shared with SDVO)
SDVO_CTRLDATA	I/O COD	HDMI Port B Control Data (This pin is shared with SDVO)
DDPC_CTRLCLK	I/O COD	HDMI Port C Control Clock
DDPC_CTRLDATA	I/O COD	HDMI Port C Control Data

## 2.6 Intel® High Definition Audio (Intel® HD Audio) Signals

Signal Name	Type	Description
HDA_SDO	I CMOS	<b>Intel® HD Audio Serial Data Input to GMCH Audio HW:</b> Driven by Intel HD Audio controller.
HDA_SDI	I/O CMOS	Point-to-Point ICH Intel HD Audio Serial Response Output
HDA_RST#	I CMOS	Global Intel HD Audio Link Reset
HDA_BCLK	I CMOS	Global Intel HD Audio 24.00-MHz clk
HDA_SYNC	I CMOS	<b>Global 48-kHz Frame Sync and Inbound Tag Signal:</b> SYNC is sourced from the Intel HD Audio controller and input to GMCH Audio HW.



## 2.7 Intel® Management Engine Interface (Intel® MEI) Signals

**Note:** The signals below are used as the Intel® Management Engine Interface (Intel® MEI) between the GMCH and the ICH. For details on implementing Intel Management Engine on the platform, please see the *Platform Intel ME-EC Interaction Specification* document.

Signal Name	Type	Description
CL_CLK	I/O GTL	Controller Link Bi-Directional Clock
CL_DATA	I/O GTL	Controller Link Bi-Directional Data
CL_RST#	I GTL	Controller Link Reset
CL_VREF	I A	External Reference Voltage for Controller Link Input Buffers
CL_PWROK	I HVCMOS	Intel® Management Engine/Controller Link Power OK

## 2.8 PLL Signals

(Sheet 1 of 2)

Signal Name	Type	Description
DPLL_REF_CLK	I Diff Clk	<b>Display PLLA Differential Clock In:</b> 96 MHz Display PLL Differential Clock In, no SSC support –
DPLL_REF_CLK#	I Diff Clk	<b>Display PLLA Differential Clock In Complement:</b> Display PLL Differential Clock In Complement - no SSC support.
DPLL_REF_SSCLK	I Diff Clk	<b>Display PLLB Differential Clock In:</b> 100 MHz Optional Display PLL Differential Clock In for SSC support <b>NOTE:</b> Differential Clock input for optional SSC support for LVDS display.
DPLL_REF_SSCLK#	I Diff Clk	<b>Display PLLB Differential Clock In Complement:</b> Optional Display PLL Differential Clock In Complement for SSC support. <b>NOTE:</b> Differential Clock input for optional SSC support for LVDS display.
HPLL_CLK	I Diff Clk	<b>Differential Host Clock In:</b> Differential clock input for the Host PLL. Used for phase cancellation for FSB transactions. This clock is used by all of the GMCH logic that is in the Host clock domain. Also used to generate core and system memory internal clocks. This is a low-voltage differential signal and runs at ¼ the FSB data rate.



(Sheet 2 of 2)

Signal Name	Type	Description
HPLL_CLK#	I Diff Clk	Differential Host Clock Input Complement
PEG_CLK	I Diff Clk	<b>Differential PCI Express Based Graphics/DMI Clock In:</b> These pins receive a differential 100-MHZ Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
PEG_CLK#	I Diff Clk	Differential PCI Express Based Graphics/DMI Clock In Complement

## 2.9 Reset and Miscellaneous Signals

(Sheet 1 of 2)

Signal Name	Type	Description
CLKREQ#	O COD	<b>External Clock Request:</b> GMCH drives CLKREQ# to control the PCI Express differential clock input to itself.
GFX_VID [4:0]	O HVC MOS	<b>Voltage ID to Support Graphics Render Standby Mode</b>
GFX_VR_EN	O HVC MOS	<b>VR Enable Signal to Support Graphics Render Standby Mode</b>
ICH_SYNC#	O HVC MOS	<b>ICH Synchronization:</b> Asserted to synchronize with ICH on faults. ICH_SYNC# must be connected to ICH's MCH_SYNC# signal.
PM_SYNC#	I HVC MOS	<b>Power Management Sync:</b> Used to indicate a Cx state transition between ICH and GMCH.
DPRSLPVR	I HVC MOS	<b>Deeper Sleep - Voltage Regulator:</b> Deeper Sleep Voltage signal from ICH.
PM_DPRSTP#	I LVC MOS	<b>Deeper Sleep State:</b> Deeper Sleep State signal coming from the ICH.
PM_EXT_TS# [1:0]	I HVC MOS	<b>External Thermal Sensor Input:</b> If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling.
SM_PWROK	I CMOS	<b>DDR3 Power Good Monitor:</b> Connected to V <sub>SS</sub> in DDR2. Driven by platform logic for DDR3.
SM_DRAMRST#	O SSTL-1.5	<b>DDR3 DRAM Reset:</b> Reset signal from GMCH to DRAM devices. One for all channels or SO-DIMMs. Used only in DDR3 mode.
PWROK	I HVC MOS	<b>Power OK:</b> Indication to the GMCH that core power is stable. This input buffer is 3.3-V tolerant.
RSTIN#	I HVC MOS	<b>Reset In:</b> When asserted this signal will asynchronously reset the GMCH logic. This signal is connected to the PLTRST# output of the ICH. This input has a Schmitt trigger to avoid spurious resets. This input buffer is 3.3-V tolerant.



(Sheet 2 of 2)

Signal Name	Type	Description
TSATN#	O AGTL+	<b>Thermal Sensor Aux Trip Notification:</b> Output from the GMCH to the EC indicating the Aux2 trip point (SW programmable) has been crossed.
JTAG_TDI	I CMOS	Intel Management Engine JTAG Test Data Input
JTAG_TDO	I/O CMOS	Intel Management Engine JTAG Test Data Output
JTAG_TCK	I CMOS	Intel Management Engine JTAG Test Clock
JTAG_TMS	I CMOS	Intel Management Engine JTAG Test Mode Select
NC	NC	<b>No Connects:</b> This signals should be left as no connects.

## 2.10 Non-Critical to Function (NCTF)

Non-Critical To Function (NCTF) solder balls on packages can improve the overall package-to-board solder joint strength and reliability.

Ball locations/signal ID's followed with the suffix of NCTF have been designed into the package footprint to enhance the package to board solder joint strength/reliability of this product by absorbing some of the stress introduced by the Characteristic Thermal Expansion (CTE) mismatch of the die to package interface.

**Caution:** Where board stresses are excessive, the NCTF balls may crack partially or completely. However, cracks in the NCTF balls will have no impact to our product performance or reliability. These balls have been added primarily to serve as stress absorbers.

## 2.11 Power and Ground

(Sheet 1 of 3)

Voltage	Ball Name	Description
<b>Host</b>		
1.05	VTT	Host Interface I/O Voltage
1.05	VTTLF	These balls are internally connected to power and require decoupling capacitors.
1.05	VCC_AXF	Host Interface I/O and HSIO Voltage
<b>System Memory</b>		
1.5/1.8	VCC_SM	I/O Voltage
1.5/1.8	VCC_SM/NC	I/O Voltage - May be left NC on DDR2 motherboards
1.5/1.8	VCC_SM_LF	These balls are internally connected to power and require a decoupling capacitor.
1.5/1.8	VCC_SM_CK	Clock I/O Voltage
1.05	VCCA_SM	I/O Logic and DLL Voltage



(Sheet 2 of 3)

Voltage	Ball Name	Description
1.05	VCCA_SM_CK	Clock Logic Voltage
<b>PCI Express* Based Graphics/DMI</b>		
1.05	VCC_PEG	Analog, I/O Logic, and Term Voltage for PCI Express* Based Graphics
1.5	VCCA_PEG_BG	Band Gap Voltage for PCI Express Based Graphics
Ground	VSSA_PEG_BG	Band Gap Ground for PCI Express Based Graphics
1.05	VCC_DMI	TX Analog and Termination Voltage for DMI
<b>PLL</b>		
1.05	VCCA_HPLL	Host PLL Analog Supply
1.05	VCCD_HPLL	Host PLL Digital Supply
1.05	VCCA_MPLL	MPLL Analog Circuits
1.05	VCCA_DPLLA	Display A PLL Power Supply
1.05	VCCA_DPLLB	Display B PLL Power Supply
1.05	VCCA_PEG_PLL	Analog PLL Voltage for PCI Express Based Graphics
1.05	VCCD_PEG_PLL	Digital PLL Voltage for PCI Express Based Graphics
<b>High-voltage</b>		
3.3	VCC_HV	HV buffer Power Supply
<b>CRT</b>		
3.3	VCCA_CRT_DAC	Analog Power Supply
1.5	VCCD_QDAC	Quiet Digital Power Supply (same as VCCD_QDAC for TV)
<b>LVDS</b>		
1.8	VCCD_LVDS	Digital Power Supply
1.8	VCC_TX_LVDS	I/O Power Supply
1.8	VCCA_LVDS	Analog Power Supply
Ground	VSSA_LVDS	Analog Ground
<b>TV</b>		
1.5	VCCD_TVDAC	TV DAC Power Supply
3.3	VCCA_TV_DAC	TVDAC IO Voltage
1.5	VCCD_QDAC	Quiet Digital TV DAC Power Supply (Shared with CRTDAC)
3.3	VCCA_DAC_BG	TV DAC Band Gap Power
Ground	VSSA_DAC_BG	TV DAC Band Gap Ground
<b>Intel® HD Audio</b>		
1.5	VCC_HDA	Intel HD Audio Power Supply
<b>Intel® Management Engine</b>		
1.05	VCC	Intel Management Engine voltage is tied to V <sub>cc</sub>



(Sheet 3 of 3)

Voltage	Ball Name	Description
<b>Core</b>		
1.05	VCC	Core Chipset Voltage Supply
1.05 (Nominal)	VCC_AXG	Graphics Voltage Supply
1.05	VCC_AXG_SENSE	GFX Voltage Supply Sense Signal
Ground	VSS_AXG_SENSE	V <sub>SS</sub> Sense Signal
Ground	VSS	Ground
Ground	VSS_SCB	Sacrificial Corner Balls for Improved Package Reliability

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## 3 Host Interface

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### 3.1 FSB Source Synchronous Transfers

The GMCH supports the Intel Core 2 Duo mobile processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At bus clock speeds of 166 MHz, 200 MHz and 266 MHz, address signals run at 667 MT/s, 800 MT/s and 1066 MT/s, which amounts to a maximum address queue rate of 83, 100 and 133 Mega-addresses/sec, respectively. Data signals are quad pumped and an entire 64-B cache line can be transferred in two bus clocks.

At 166-MHz, 200-MHz and 266-MHz bus clocks, data signals run at 667 MT/s, 800 MT/s and 1066 MT/s for a maximum bandwidth of 5.3 GB/s, 6.4 GB/s and 8.5 GB/s, respectively.

### 3.2 FSB IOQ Depth

The Scalable Bus supports up to 12 simultaneous outstanding transactions. The GMCH has a 12 deep IOQ.

### 3.3 FSB OOQ Depth

The GMCH supports only one outstanding deferred transaction on the FSB.

### 3.4 FSB AGTL+ Termination

The GMCH integrates AGTL+ termination resistors on die.

### 3.5 FSB Dynamic Bus Inversion

The GMCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low-voltage on each quad pumped data phase. This decreases the worst-case power consumption of the GMCH. H\_DINV [3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

H_DINV# [3:0]	Data Bits
H_DINV#0	H_D# [15:0]
H_DINV#1	H_D# [31:16]
H_DINV#2	H_D# [47:32]
H_DINV#3	H_D# [63:48]

Whenever the processor or the GMCH drives data, each 16-bit segment is analyzed. If there are more than eight (out of sixteen) signals driven low on the H\_D# bus, a corresponding H\_DINV# signal is asserted. As a result, the data is inverted prior to



being driven on the bus. Whenever the processor or the GMCH receives data, it monitors H\_DINV# [3:0] to determine if the corresponding data segment should be inverted.

### 3.6 FSB Interrupt Overview

The Intel Core 2 Duo mobile processor and Intel Core 2 Extreme mobile processor support FSB interrupt delivery, but **do not** support the APIC serial bus interrupt delivery mechanism. Interrupt related messages are encoded on the FSB as Interrupt Message Transactions. FSB interrupts may originate from the CPU(s) on the FSB, or from a downstream device on the DMI or PCI Express Graphics Attach. In the latter case, the GMCH drives the Interrupt Message Transaction on the FSB.

In the IOxAPIC environment, an interrupt is generated from the IOxAPIC to a processor in the form of an upstream Memory Write. The ICH contains IOxAPICs, and its interrupts are generated as upstream DMI Memory Writes. A PCI device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC. The IOxAPIC in turn generates an interrupt as an upstream DMI Memory Write. Alternatively, the MSI may directly route to the FSB. The target of an MSI depends on the address of the interrupt Memory Write. The GMCH forwards upstream DMI and PCI Express Graphics Attach low-priority Memory Writes to address OFEEx\_xxxxh to the FSB as Interrupt Message Transactions.

The GMCH also broadcasts EOI cycles generated by a processor downstream to the PCI Express Port and DMI interfaces.

### 3.7 APIC Cluster Mode Support

APIC Cluster Mode support is required for backwards compatibility with existing software, including various operating systems. For example, beginning with Microsoft Windows\* 2000 operating system, there is a mode (boot.ini) that allows an end-user to enable the use of cluster addressing support of the APIC.

### 3.8 FSB Dynamic Frequency Switching

Dynamic FSB frequency switching effectively reduces the internal bus clock frequency in half to further decrease the minimum processor operating frequency. This feature does not entail a change in the external bus signal (BCLK) frequency. Instead, both the processor and GMCH internally lower their BCLK reference frequency to 50% of the externally visible frequency. The down-shift and up-shift transitions are done following a handshake between the processor and chipset.

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## 4 System Address Map

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The GMCH supports up to 64 GB of addressable memory space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1-MB region, which is divided into regions that can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only.

This section specifies how the memory space is partitioned and what the separate memory regions are used for I/O address space has simpler mapping and is explained in [Section 4.10](#).

**Note:** In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI. The exception to this rule is VGA ranges, which may be mapped to PCI Express, DMI, or to the internal graphics device (IGD).

In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the internal graphics device respectively. The GMCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS.

The Address Map includes a number of programmable ranges:

- Device0
  - EPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4-KB window)
  - MCHBAR – Memory mapped range for internal GMCH registers.
  - PCIEXBAR – Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0-FFh) and extended configuration space (100h-FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (64-MB, 128-MB, or 256-MB window)
  - DMIBAR –This window is used to access registers associated with the Direct Media Interface (DMI) register memory range. (4-KB window)
  - GGC – GMCH graphics control register. Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes. (0 to 64-MB options)
- Device 1, Function 0:
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window
  - PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window (PMUBASE/PMULIMIT) - are applicable for 36-bit SKUs
  - IOBASE1/IOLIMIT1 – PCI Express port IO access window
- Device 2, Function 0:
  - MMADR – IGD registers and internal graphics instruction port. (512-KB window)
  - IOBAR – I/O access window for internal graphics. Through this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed.

**Note:** This allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTADR table.



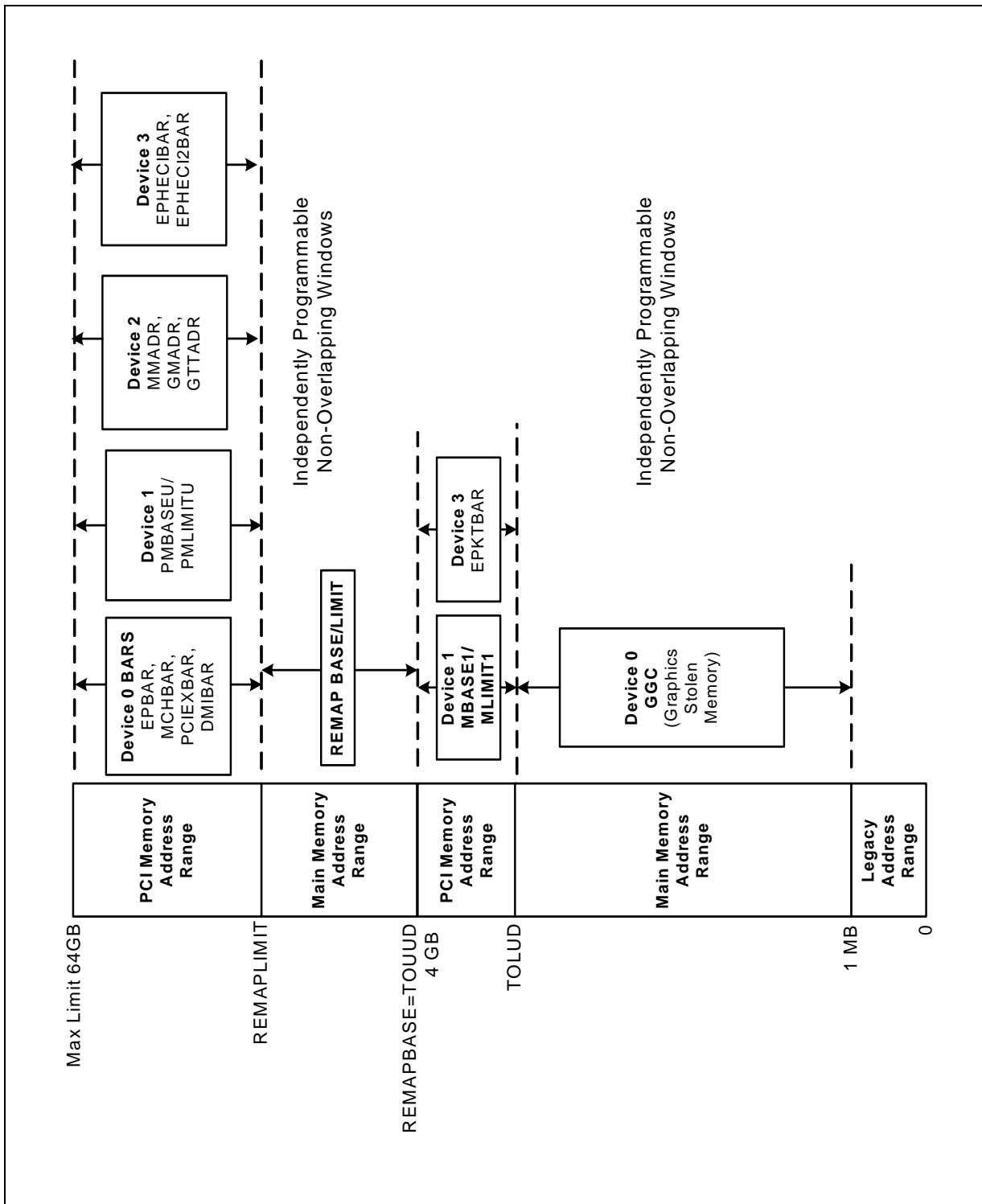
- GMADR – Internal graphics translation window. (256-MB window)
- GTTADR – Internal graphics translation table location. (256-KB window)
- Device 2, Function 1:
  - MMADR – Function 1 IGD registers and internal graphics instruction port. (512-KB window)
- Device 3, Function 0:
  - EPHECIBAR - Function 0 HECI memory mapped registers (16-B window)
- Device 3, Function 1:
  - EPHECI2BAR - Function 0 HECI memory mapped registers (16-B window)
- Device 3, Function 3:
  - EPKTBAR - Function 3 Keyboard and Text IO space (8-B window)

The rules for the above programmable ranges are:

1. ALL of these ranges MUST be unique and NON-OVERLAPPING. **It is the BIOS or system designers responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.**
2. In the case of overlapping ranges with memory, the memory decode will be given priority.
3. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
4. Accesses to overlapped ranges may produce indeterminate results.
5. The only peer-to-peer cycles allowed below the top of memory (register TOLUD) are DMI to PCI Express VGA range writes. Note that peer to peer cycles to the Internal Graphics VGA range are not supported.

Figure 2 represents system memory address map in a simplified form.

Figure 2. System Address Ranges



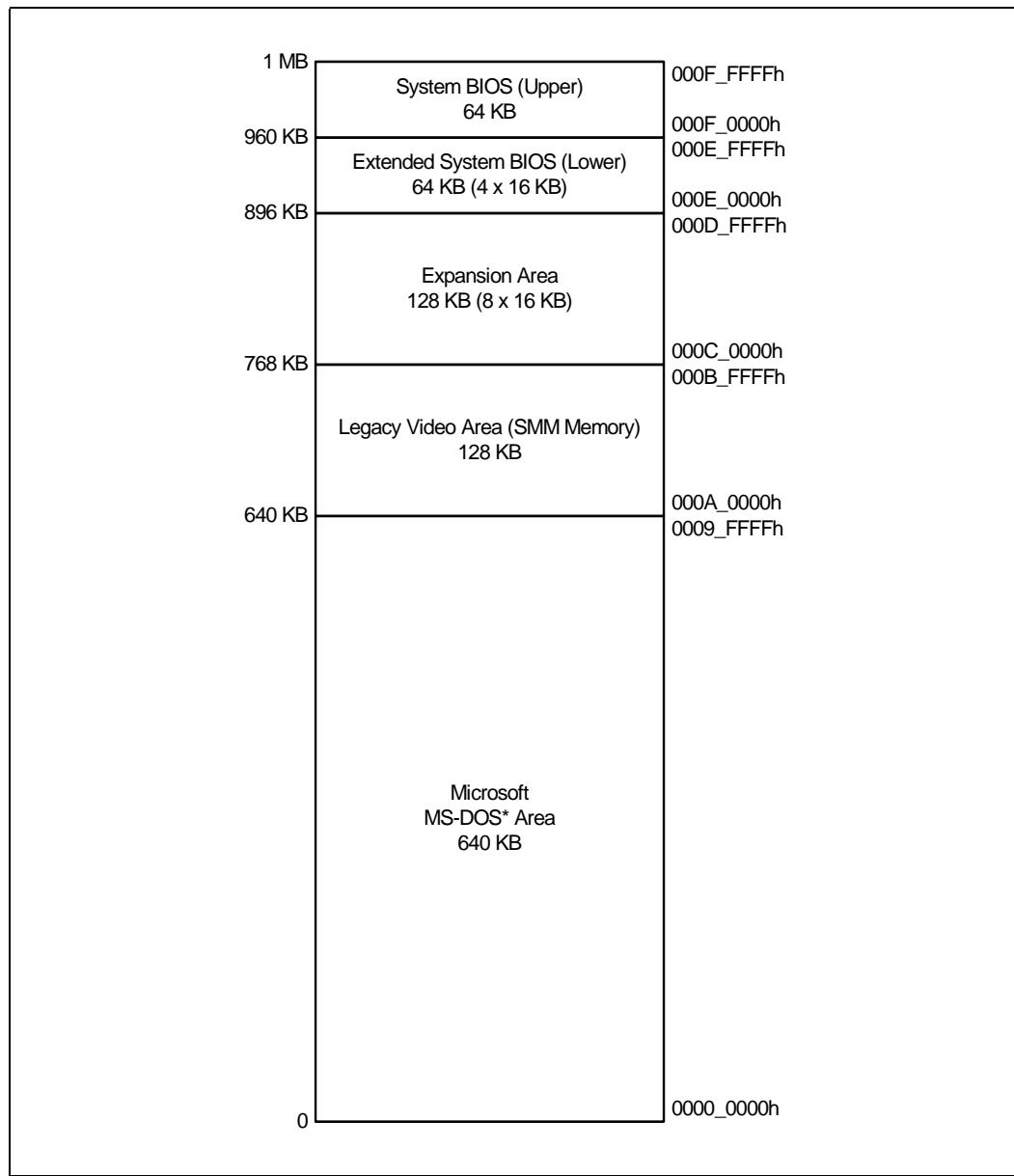
**NOTE:** BARs mapped to the REMAPLIMIT-64 GB space can also be mapped to the TOLUD-4 GB space. GMCH variants not supporting 36-bit addressing will require these BARs to be mapped to the TOLUD-4 GB space.

## 4.1 Legacy Address Range

This area is divided into the following address regions:

- 0 - 640 KB – MS-DOS\* Area
- 640 - 768 KB – Legacy Video Buffer Area
- 768 - 896 KB in 16-KB sections (total of eight sections) – Expansion Area
- 896 - 960 KB in 16-KB sections (total of four sections) – Extended System BIOS Area
- 960 KB - 1 MB - Memory – System BIOS Area

**Figure 3.** Microsoft MS-DOS\* Legacy Address Range





#### **4.1.1 MS-DOS Range (0000\_0000h – 0009\_FFFFh)**

The MS-DOS area is 640 KB (0000\_0000h to 0009\_FFFFh) in size and is always mapped to the main memory controlled by the GMCH.

#### **4.1.2 Legacy Video Area (000A\_0000h to 000B\_FFFFh)**

The legacy 128-KB VGA memory range, frame buffer, (000A\_0000h to 000B\_FFFFh) can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The GMCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configuration bits (VGA Enable and MDAP). This region is also the default for SMM space.

#### **4.1.2.1 Compatible SMRAM Address Range (000A\_0000h to 000B\_FFFFh)**

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at 000A\_0000h to 000B\_FFFFh. Non-SMM-mode processor accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area if IGD is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as peer cycles, and will master abort on PCI if no external VGA device claims them.

#### **4.1.2.2 Monochrome Adapter (MDA) Range (000B\_0000h to 000B\_7FFFh)**

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI (depending on configuration bits). Since the monochrome adapter may be mapped to any one of these devices, the GMCH must decode cycles in the MDA range (000B\_0000h to 000B\_7FFFh) and forward either to IGD, PCI Express, or the DMI. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the GMCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI Express, and/or the DMI.

#### **4.1.3 Expansion Area (000C\_0000h to 000D\_FFFFh)**

This 128-KB ISA Expansion region (000C\_0000h – 000D\_FFFFh) is divided into eight, 16-KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through GMCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

**Table 1.** Expansion Area Memory Segments

Memory Segments	Attributes	Comments
000C_0000h to 000C_3FFFh	W/R	Add-on BIOS
000C_4000h to 000C_7FFFh	W/R	Add-on BIOS
000C_8000h to 000C_BFFFh	W/R	Add-on BIOS
000C_C000h to 000C_FFFFh	W/R	Add-on BIOS
000D_0000h to 000D_3FFFh	W/R	Add-on BIOS
000D_4000h to 000D_7FFFh	W/R	Add-on BIOS
000D_8000h to 000D_BFFFh	W/R	Add-on BIOS
000D_C000h to 000D_FFFFh	W/R	Add-on BIOS

#### 4.1.4 Extended System BIOS Area (000E\_0000h to 000E\_FFFFh)

This 64-KB area (000E\_0000h to 000E\_FFFFh) is divided into four, 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

**Table 2.** Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
000E_0000h to 000E_3FFFh	W/R	BIOS Extension
000E_4000h to 000E_7FFFh	W/R	BIOS Extension
000E_8000h to 000E_BFFFh	W/R	BIOS Extension
000E_C000h to 000E_FFFFh	W/R	BIOS Extension

#### 4.1.5 System BIOS Area (000F\_0000h to 000F\_FFFFh)

This area is a single 64-KB segment (000F\_0000h – 000F\_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to DMI. By manipulating the Read/Write attributes, the GMCH can shadow the BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

**Table 3.** System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
000F_0000h to 000F_FFFFh	WE RE	BIOS Area

#### 4.1.6 Programmable Attribute Map (PAM) Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM Memory Area.

The GMCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there normally will not be IWB cycles targeting DMI.

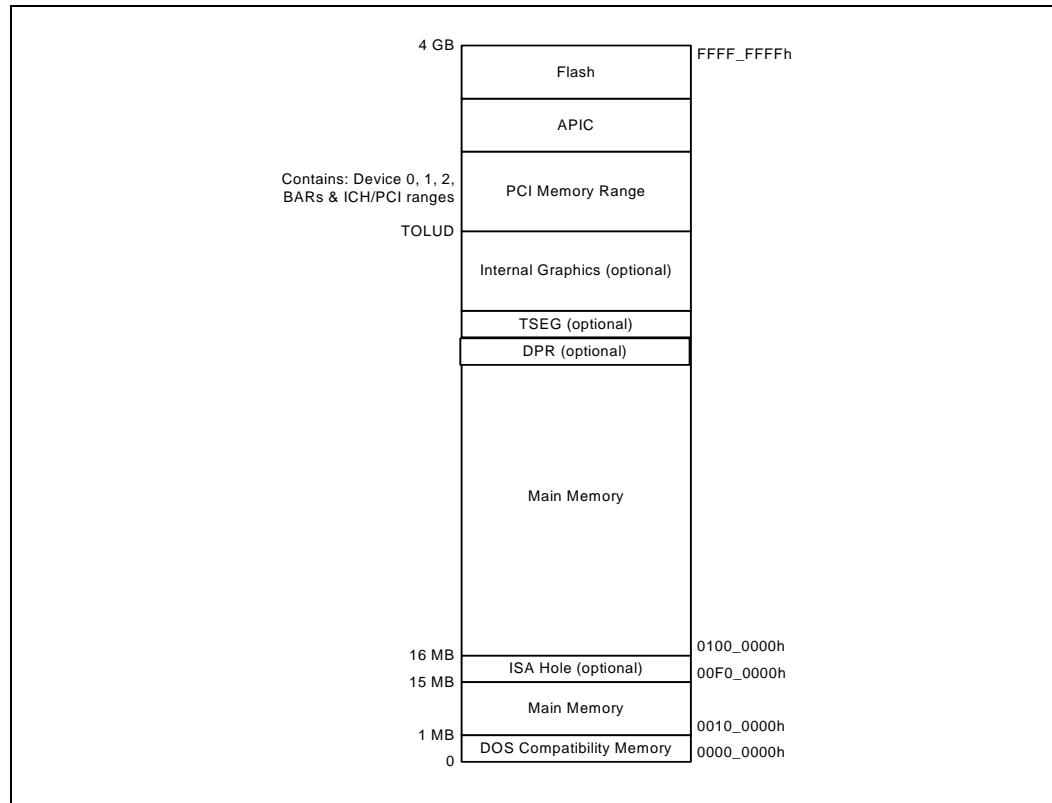
However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RD it is possible to get IWB cycles targeting DMI. This may occur for DMI originated cycles to disabled PAM regions.

In an example scenario, a particular PAM region is set for Read Disabled and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is Read Disabled the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the GMCH to hang.

### 4.2 Main Memory Address Range (1 MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the GMCH (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the GMCH to the DRAM unless they fall into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

**Figure 4. Main Memory Address Range (1 MB to TOLUD)**





#### 4.2.1 ISA Hole (15 MB to 16 MB)

A hole can be created at 15 MB to 16 MB as controlled by the fixed hole enable in Device0 space. Accesses within this hole are forwarded to the DMI. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15-MB to 16-MB hole is an optionally enabled ISA hole.

Video accelerators originally used this hole. It is also used for validation by customer teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15-MB to 16-MB window.

#### 4.2.2 TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of physical memory. System management software may partition this region of memory so it is accessible only by system management software. SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI Express, DMI, and Internal Graphics originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses (see [Table 5](#)). Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB or 8 MB.

#### 4.2.3 DPR (DMA Protected Range)

DMA protected memory only applies to DMAs and GMADR translations. This memory range will be protected from all DMA accesses, including translated CPU accesses and Graphics. The maximum amount of memory supported by DPR is 255 MB. The top of the protected range is the BASE of TSEG -1. If TSEG is not enabled, then the top of this range becomes the base location of the space TSEG (if enabled) would have occupied.

#### 4.2.4 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions.** [Table 4](#) details the location and attributes of the regions. How to enable and disable these ranges are described in the GMCH Control Register Device0 (GGC).

**Table 4. Pre-allocated Memory Example for 512-MB DRAM, 64-MB VGA, and 1-MB TSEG**

Memory Segments	Attributes	Comments
0000_0000h to 1BEF_FFFFh	R/W	Available System Memory 447 MB
1BF0_0000h to 1BFF_FFFFh	SMM Mode Only - Processor Reads	TSEG Address Range & Pre-allocated Memory
1C00_0000h to 1FFF_FFFFh	R/W	Pre-allocated Graphics VGA memory. 64 MB when IGD is enabled.



## 4.3 PCI Memory Address Range (TOLUD to 4 GB)

This address range, from the top of physical memory to 4 GB, is normally mapped to the DMI Interface.

Exceptions to this mapping include the BAR memory mapped regions, which include: EPBAR, MCHBAR, and DMIBAR.

In the PCI Express port, there are two exceptions to this rule:

1. Addresses decoded to the PCI Express Memory Window defined by the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers are mapped to PCI Express
2. Addresses decoded to PCI Express Configuration Space are mapped based on Bus, Device, and Function number (PCIEXBAR range)

**Note:** AGP Aperture no longer exists with PCI Express.

In an internal graphics configuration, there are three exceptions to this rule:

1. Addresses decoded to the Graphics Memory Range. (GMADR range)
2. Addresses decoded to the Graphics Translation table range (GTTADR range)
3. Addresses decoded to the Memory Mapped Range of the Internal Graphics Device (MMADR range). There is a MMADR range for Device2 function 0 and a MMADR range for Device2 function 1. Both ranges are forwarded to the internal graphics device.

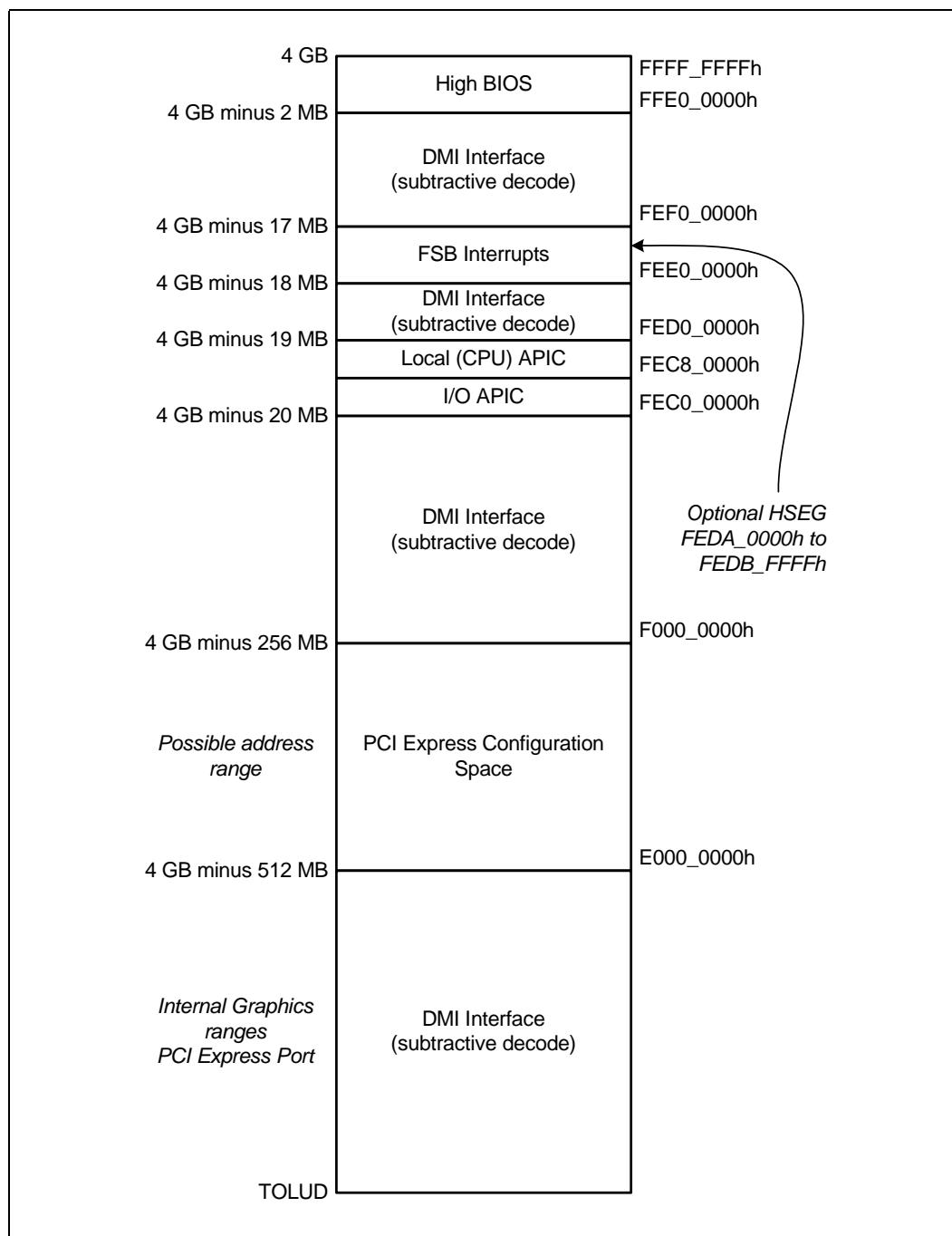
In Intel Management Engine configuration, there are exceptions to this rule:

1. Addresses decoded to the Intel Management Engine keyboard and Text MMIO range (EPKTBAR)

The exceptions listed above for internal graphics and the PCI Express ports **MUST NOT overlap with APIC Configuration Space, FSB Interrupt Space and High BIOS Address Range.**

**Note:** With the exception of certain BARs, all the above mentioned BARs can be mapped in the TOUUD to 64-GB range in the case of chipset variants supporting 36-bit addressing. See [Figure 2](#) for details.

**Figure 5. PCI Memory Address Range (TOLUD to 4 GB)**





### 4.3.1 APIC Configuration Space (FEC0\_0000h to FECF\_FFFFh)

This range is reserved for APIC configuration space which includes the default I/O APIC configuration space from FEC0\_0000h to FEC7\_0FFFh. The default Local (processor) APIC configuration space goes from FEC8\_0000h to FECF\_FFFFh.

Processor accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the processor. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each processor should be relocated to the FEC0\_0000h (4 GB minus 20 MB) to FECF\_FFFFh range so that one MTRR can be programmed to 64 KB for the Local and I/O APICs. The I/O APIC(s) usually reside in the ICH portion of the chip set or as a stand-alone component(s).

I/O APIC units will be located beginning at the default address FEC0\_0000h. The first I/O APIC will be located at FEC0\_0000h. Each I/O APIC unit is located at FEC0\_x000h where x is I/O APIC unit number 0 through F (hex). This address range will normally be mapped to DMI.

**Note:** There is no provision to support an I/O APIC device on PCI Express.

### 4.3.2 HSEG (FEDA\_0000h to FEDB\_FFFFh)

This optional segment from FEDA\_0000h to FEDB\_FFFFh provides a remapping window to SMM memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A\_0000h to 000B\_FFFFh. Non-SMM mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All Cacheline writes with WB attribute or implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

### 4.3.3 FSB Interrupt Memory Space (FEE0\_0000 to FEEF\_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express, internal graphics, or DMI may issue a Memory Write to OFEEx\_xxxxh. The GMCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The GMCH terminates the FSB transaction by providing the response and asserting H\_TRDY#. This Memory Write cycle does not go to DRAM.

### 4.3.4 High BIOS Area

The top 2 MB (FFE0\_0000h to FFFF\_FFFFh) of the PCI Memory Address Range is reserved for system BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to DMI so that the upper subset of this region aliases to the 16-MB minus 256-KB range. The actual address space required for the BIOS is less than 2 MB, but the minimum processor MTRR range for this region is 2 MB so a full 2 MB must be considered.



## 4.4 Main Memory Address Space (4 GB to TOUUD)

Earlier chipsets supported a maximum main memory size of 4-GB total memory. This would result in a hole between TOLUD (Top of Low Usable DRAM) and 4 GB when main memory size approached 4 GB, resulting in a certain amount of physical memory being inaccessible to the system.

The new reclaim configuration registers (TOUUD, REMAPBASE, REMAPLIMIT) exist to reclaim lost main memory space. The greater than 32-bit reclaim handling will be handled similar to other MCHs.

Upstream read and write accesses above 36-bit addressing will be treated as invalid cycles by PCI Express Graphics and DMI.

The Top of Memory (TOM) register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO above TOM).

The Intel ME stolen memory is located at the top of physical memory. TOM is used to allocate the Intel ME's stolen memory; the Intel ME stolen memory base is calculated by subtracting the amount of memory stolen by the Intel ME from TOM. The Intel ME stolen size register reflects the total amount of physical memory stolen by the Intel ME.

The Top of Upper Usable DRAM (TOUUD) register reflects the total amount of addressable memory. If reclaim is disabled, TOUUD will reflect TOM minus Intel ME's stolen size. If reclaim is enabled, then it will reflect the reclaim limit. Also, the reclaim base will be the same as TOM minus Intel Management Engine stolen memory size to the nearest 64-MB alignment.

### 4.4.1 Memory Remap Background

The following examples of Memory Mapped I/O devices are typically located below 4 GB:

- High BIOS
- H-Seg
- T-Seg
- Graphics Stolen Memory
- Local APIC
- FSB Interrupts
- Mbase/Mlimit
- Memory Mapped I/O space that supports only 32-bit addressing

The GMCH provides the capability to remap or reclaim the physical memory overlapped by the Memory Mapped I/O logical address space. The GMCH re-maps physical memory from the Top of Low Usable DRAM (TOLUD) boundary up to the 4-GB boundary to an equivalent sized logical address range located just below the Intel ME's stolen memory.



#### 4.4.2 Memory Remapping (or Reclaiming)

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the REMAPBASE register. The top of the re-map window is defined by the value in the REMAPLIMIT register. An address that falls within this window is remapped to the physical memory starting at the address defined by the TOLUD register. The TOLUD register must be 64-MB aligned when remapping is enabled, but can be 1-MB aligned when remapping is disabled.

### 4.5 PCI Express Configuration Address Space

The Device0 register (PCIEXBAR), defines the base address for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. This is a 256-MB block of addresses below top of addressable memory (currently 4 GB) and is aligned to a 256-MB boundary. BIOS must assign this address range such that it will not conflict with any other address ranges.

#### 4.5.1 PCI Express Graphics Attach

The GMCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in GMCH's Device1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Prefetchable Memory Base (PMBASE/PMBASEU) and Prefetchable Memory Limit (PMLIMIT/PMLIMITU) registers.

The GMCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

$$\text{Memory\_Base\_Address} \leq \text{Address} \leq \text{Memory\_Limit\_Address}$$

$$\text{Prefetchable\_Memory\_Base\_Address} \leq \text{Address} \leq \text{Prefetchable\_Memory\_Limit\_Address}$$

It is essential to support a separate Prefetchable range to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the GMCH Device1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the Device1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

#### 4.5.2 Graphics Aperture

Unlike AGP, PCI Express has no concept of aperture for PCI Express devices. As a result, there is no need to translate addresses from PCI Express. Therefore, the GMCH has no APBASE and APSIZE registers.



## 4.6 Graphics Memory Address Ranges

The GMCH can be programmed to direct memory accesses to IGD when addresses are within any of three ranges specified via registers in GMCH's Device2 configuration space.

- The Memory Map Base Register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base Register (GTTADR) is used to access the translation table.

Normally these ranges will reside above the Top-of-Main-DRAM and below high BIOS and APIC address ranges. They normally reside above the top of memory (TOLUD) so they do not steal any physical DRAM memory space. GMADR is a Prefetchable range to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

### 4.6.1 Graphics Register Ranges

This section provides a high-level register map (register groupings per function) for the integrated graphics. The memory and I/O maps for the graphics registers are shown in [Figure 6](#), except PCI Configuration registers, which are described in Volume 2 of this document. The VGA and Extended VGA registers can be accessed via standard VGA I/O locations as well as via memory-mapped locations. In addition, the memory map contains allocation ranges for various functions. The memory space address listed for each register is an offset from the base memory address programmed into the MMADR register (PCI configuration offset 14h). The same memory space can be accessed via dword accesses to I/OBAR. Through the IOBAR, I/O registers MMIO\_index and MMIO\_data are written.

#### 4.6.1.1 VGA and Extended VGA Control Registers (0000\_0000h to 0000\_0FFFh)

These registers are located in both I/O space and memory space. The VGA and Extended VGA registers contain the following register sets: General Control/Status, Sequencer (SRxx), Graphics Controller (GRxx), Attribute Controller (ARxx), VGA Color Palette, and CRT Controller (CRxx) registers.

#### 4.6.1.2 Instruction, Memory, and Interrupt Control Registers (0000\_1000h to 0000\_2FFFh)

The Instruction and Interrupt Control registers are located in this space and contain the types of registers listed in the following sections.

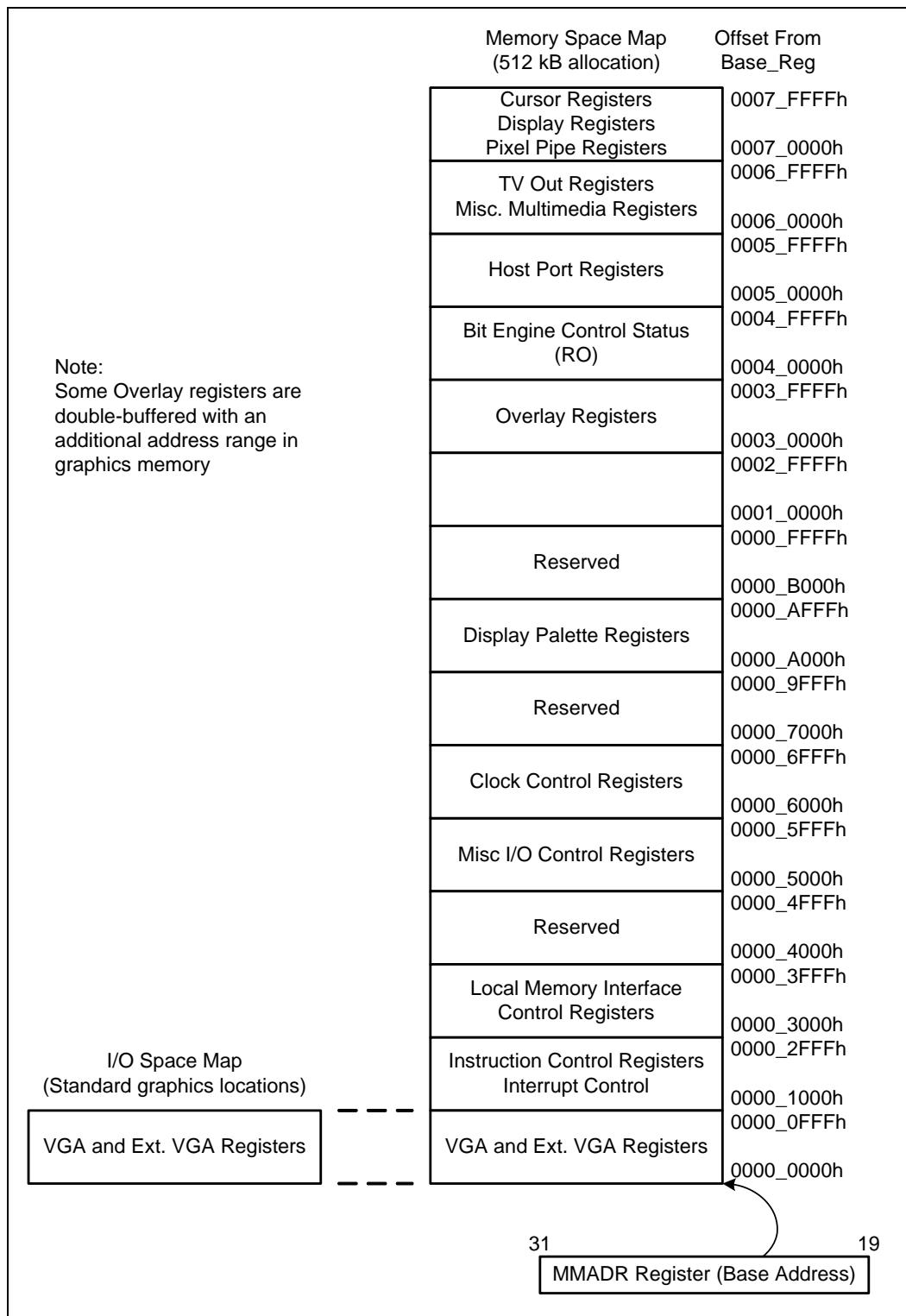
### 4.6.2 I/O Mapped Access to Device 2 MMIO Space

If Device 2 is enabled, and Function 0 within Device 2 is enabled, then IGD registers can be accessed using the IOBAR.

**MMIO\_Index:** MMIO\_INDEX is a 32-bit register. An I/O write to this port loads the address of the MMIO register that needs to be accessed. I/O Reads returns the current value of this register.

**MMIO\_Data:** MMIO\_DATA is a 32-bit register. An I/O write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. An I/O read to this port is re-directed to the MMIO register pointed to by the MMIO-index register.

Figure 6. Graphics Register Memory and I/O Map





## 4.7 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SM RAM). The GMCH supports: Compatible SMRAM (C\_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. GMCH provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.
- Above 1-MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. The TSEG area lies below IGD stolen memory.

The above 1-MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

**Note:**

DMI and PCI Express masters are not allowed to access the SMM space.

### 4.7.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space are different address ranges. Note that the High DRAM space is the same as the Compatible Transaction Address space. [Table 5](#) describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

**Table 5.** SMM Space Definition Summary

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (Adr C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (Adr H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (Adr T)	(TOLUD minus STOLEN minus TSEG) to (TOLUD minus STOLEN)	(TOLUD minus STOLEN minus TSEG) to (TOLUD minus STOLEN)



## 4.8 SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any PCI devices (including DMI, PCI Express, and graphics devices). This is a BIOS responsibility.
- Both D\_OPEN and D\_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
- Any address translated through the GMADR must not target DRAM from A\_0000-F\_FFFF.

### 4.8.1 SMM Space Combinations

When High SMM is enabled (G\_SMRAME=1 and H\_SMRAM\_EN=1) the Compatible SMM space is effectively disabled. Processor originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP), otherwise they are forwarded to the DMI. PCI Express and DMI originated accesses are **never** allowed to access SMM space.

**Table 6.** SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Adr C Range	Adr H Range	Adr T Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

### 4.8.2 SMM Control Combinations

The G\_SMRAME bit provides a global enable for all SMM memory. The D\_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at power up. The D\_LCK bit limits the SMM range access to only SMM mode accesses. The D\_CLS bit causes SMM data accesses to be forwarded to the DMI or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

**Table 7. SMM Control Table**

G_SMRAWE	D_LCK	D_CLS	D_OPEN	Processor in SMM Mode	SMM Code Access	SMM Data Access
0	X	X	X	X	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	X	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	X	Invalid	Invalid
1	1	X	X	0	Disable	Disable
1	1	0	X	1	Enable	Enable
1	1	1	X	1	Enable	Disable

#### 4.8.3 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI originated transactions are not allowed to SMM space.

#### 4.8.4 Processor WB Transaction to an Enabled SMM Address Space

Processor Writeback transactions (REQ [1]# = 0) to enabled SMM address space must be written to the associated SMM DRAM even though D\_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

### 4.9 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be shadowed into GMCH DRAM memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. Processor bus transactions are routed accordingly.

### 4.10 I/O Address Space

The GMCH does not support the existence of any other I/O devices beside itself on the processor bus. The GMCH generates either DMI or PCI Express bus cycles for all processor I/O accesses that it does not claim. Within the host bridge the GMCH contains two internal registers in the processor I/O space, Configuration Address Register (CONFIG\_ADDRESS) and the Configuration Data Register (CONFIG\_DATA). These locations are used to implement a configuration space access mechanism.

The processor allows 64 KB plus 3 B to be addressed within the I/O space. The GMCH propagates the processor I/O address without any translation on to the destination bus and therefore provides addressability for 64-KB plus 3-B locations.



**Note:** The upper three locations can be accessed only during I/O address wrap-around when processor bus H\_A#16 address signal is asserted. H\_A#16 is asserted on the processor bus whenever an I/O access is made to four bytes from address 0000\_FFFDh, 0000\_FFFEh, or 0000\_FFFFh. H\_A#16 is also asserted when an I/O access is made to 2 bytes from address 0000\_FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to ICH or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to PCI Express.

The GMCH responds to I/O cycles initiated on PCI Express or DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The GMCH will break this into two separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into two transactions by the processor.

#### 4.10.1 PCI Express I/O Address Mapping

The GMCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in GMCH Device1 configuration space.

The GMCH positively decodes I/O accesses to PCI Express I/O address space as defined by the following relation:

$$\text{I/O\_Base\_Address} \leq \text{Processor I/O Cycle Address} \leq \text{I/O\_Limit\_Address}$$

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

The GMCH also forwards accesses to the Legacy VGA I/O ranges according to the settings in the Device1 configuration registers BCTRL (VGA Enable) and PCICMD1 (IOAE1), unless a second adapter (monochrome) is present on the DMI Interface/PCI. The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set, the GMCH will decode legacy monochrome IO ranges and forward them to the DMI Interface. The IO ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3Bah and 3BFh.

**Note:** The GMCH Device 1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI Express.

## 4.11 GMCH Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A\_0000 to 000A\_FFFF

MDA = 000B\_0000 to 000B\_7FFF

VGAB = 000B\_8000 to 000B\_FFFF

MAINMEM = 0100\_0000 to TOLUD

### 4.11.1 Legacy VGA and I/O Range Decode Rules

The legacy 128-KB VGA memory range 000A\_0000h to 000B\_FFFFh can be mapped to IGD (Device 2), to PCI Express (Device1), and/or to the DMI depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the GMCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

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## 5 System Memory Controller

### 5.1 Functional Overview

The Mobile Intel 4 Series Express Chipset Family system memory controller supports DDR2 and DDR3 SDRAMs.

Two memory channel organizations are supported:

- Dual-channel interleaved (single SO-DIMM per channel)
- Dual-channel asymmetric (single SO-DIMM per channel)

Each channel has a 64-bit data interface and the frequencies supported are:

- 667 MHz and 800 MHz for DDR2
- 800 MHz and 1066 MHz for DDR3

Each channel can have one or two ranks populated. There can be a maximum of four ranks (two, double-sided SO-DIMMs) populated.

- Note:** The Mobile Intel GS45 and GS40 Express Chipsets can support memory-down on one channel and SO-DIMM on the other channel. The Mobile Intel GS45 and GS40 Express Chipsets can support memory-down on two channels, but not validated.
- Note:** The Mobile Intel 4 Series Express Chipset Family supports only one SO-DIMM connector per channel.
- Note:** The Mobile Intel 4 Series Express Chipset Family supports Channel A only for single channel configuration.
- Note:** The Mobile Intel 4 Series Express Chipset Family does not support mixed CAS Latency memory combination.

**Table 8. System Memory Organization Support for DDR2**

DDR2							
Tech	Config	Page Size (Device/Module)	Banks	Smallest Increments	Largest Increments	Maximum Capacity (2 SO-DIMMs)	Note
256 Mb	32 Mb x 8	1 k/8 k	4	256 MB	512 MB	1 GB	1
256 Mb	16 Mb x 16	1 k/4 k	4	128 MB	256 MB	512 MB	1
512 Mb	64 Mb x 8	1 k/8 k	4	512 MB	1 GB	2 GB	
512 Mb	32 Mb x 16	2 k/8 k	4	256 MB	512 MB	1 GB	
1 Gb	128 Mb x 8	1 k/8 k	8	1 GB	2 GB	4 GB	
1 Gb	64 Mb x 16	2 k/8 k	8	512 MB	1 GB	2 GB	
2 Gb	256 Mb x 8	1 k/8 k	8	2 GB	4 GB	8 GB	
2 Gb	128 Mb x 16	2 k/8 k	8	1 GB	2 GB	4 GB	

**NOTES:**

1. Not validated.

**Table 9. System Memory Organization Support for DDR3**

DDR3							
Tech	Config	Page Size (Device/Module)	Banks	Smallest Increments	Largest Increments	Maximum Capacity (2 SO-DIMMs)	Note
512 Mb	64 Mb x 8	1 k/8 k	8	512 MB	1 GB	2 GB	1
512 Mb	32 Mb x 16	2 k/8 k	8	256 MB	512 MB	1 GB	1
1 Gb	128 Mb x 8	1 k/8 k	8	1 GB	2 GB	4 GB	
1 Gb	64 Mb x 16	2 k/8 k	8	512 MB	1 GB	2 GB	
2 Gb	256 Mb x 8	1 k/8 k	8	2 GB	4 GB	8 GB	
2 Gb	128 Mb x 16	2 k/8 k	8	1 GB	2 GB	4 GB	

**NOTES:**

1. Not validated, memory product is currently not available.

## 5.2 Memory Channel Access Modes

The system memory controller supports two styles of memory access: dual-channel Interleaved and dual-channel Asymmetric. Rules for populating SO-DIMM slots are included in this chapter.

### 5.2.1 Dual-Channel Interleaved Mode

This mode provides maximum performance on real applications. Addresses alternate between the channels after each cache line (64-byte boundary). The channel selection address bit is controlled by DCC [10:9]. If a second request sits behind the first, and that request is to an address on the second channel, that request can be sent before data from the first request has returned. Due to this feature, some progress is made even during page conflict scenarios. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels. The drawback of conventional Interleaved mode is that the system designer must populate both channels of memory so that they have equal capacity, however the technology and device width may vary from one channel to the other.

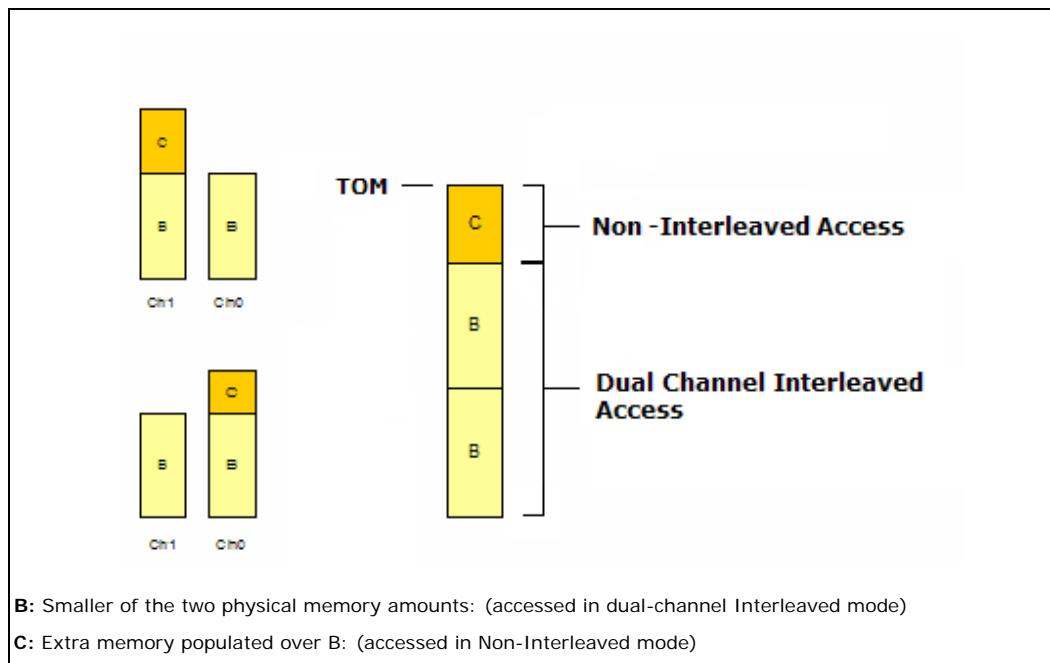
#### 5.2.1.1 Intel Flex Memory Technology (Dual-Channel Interleaved Mode with Unequal Memory Population)

The GMCH supports Interleaved addressing in dual-channel memory configurations even when the two channels have unequal amounts of memory populated. This is called Intel Flex Memory Technology.

Intel Flex Memory Technology provides higher performance with different sized channel populations than Asymmetric mode (where no interleaving is used) by allowing some interleaving.

The memory addresses up to the twice the size of the smaller SO-DIMM are Interleaved on a 64-B boundary using address Bit 6 (including any XOR-ing already used in Interleaved mode). Above this, the rest of the address space is assigned to the remaining memory in the larger channel. [Figure 7](#) shows various configurations of memory populations.

**Figure 7. Intel Flex Memory Technology Operation**



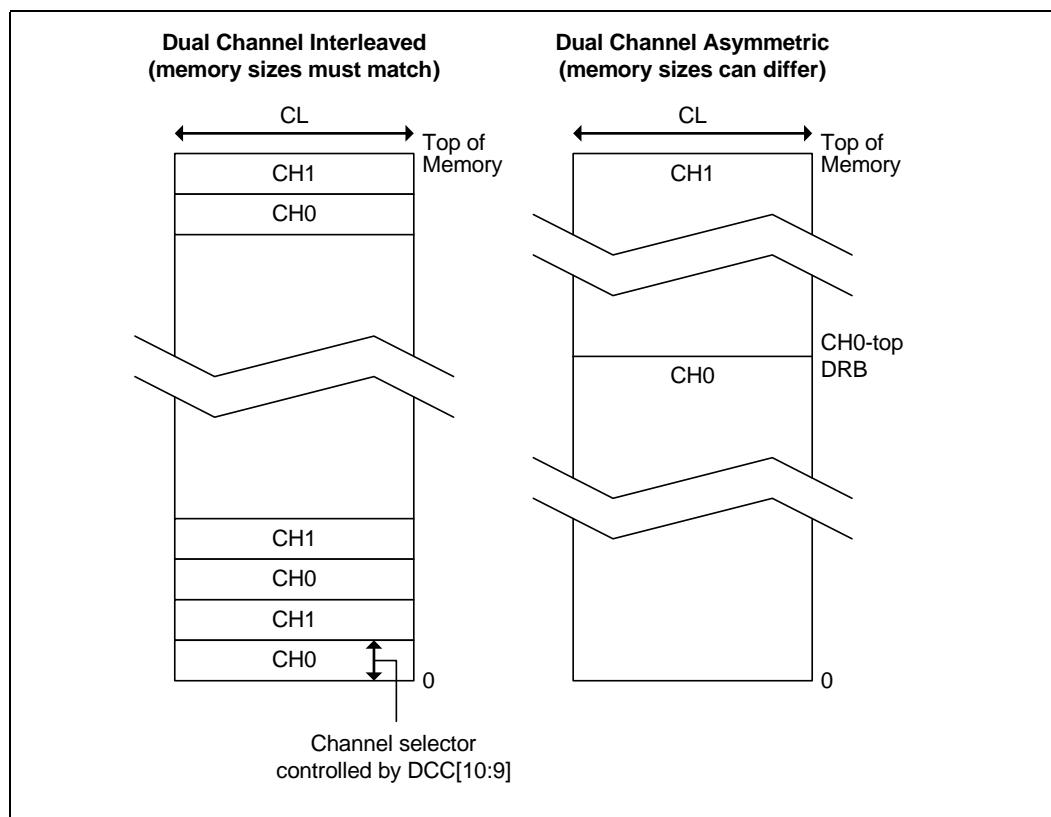
**NOTES:**

1. To enable Intel Flex Memory Technology, BIOS should program both channels' DRBs (DRAM Rank Boundaries) to the size of memory in that channel, as if for fully interleaved memory (should not add the top of one channel to the other as in Asymmetric mode). Interleaved mode operation should also be enabled.
2. To disable Intel Flex Memory Technology, BIOS should program as usual for the Asymmetric mode.

### 5.2.2 Dual-Channel Asymmetric Mode

This mode trades performance for system design flexibility, by allowing unequal amounts of memory to be populated in the two channels. Unlike the previous mode, addresses start in Channel A and stay there until the end of the highest rank in Channel A, then addresses continue from the bottom of Channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization. Therefore, in most cases bandwidth will be limited. The system designer is free to populate or not to populate any rank on either channel, including either degenerate single channel case. Because Channel A is addressed first when using only one channel, Channel A should be the channel used.

**Figure 8. System Memory Styles**



### 5.3

### DRAM Technologies and Organization

All standard 256-Mb, 512-Mb, 1-Gb, and 2-Gb technologies and addressing are supported for x16 and x8 devices.

The GMCH supports various page sizes. Page size is individually selected for every rank; 4 k and 8 k for Interleaved and Asymmetric dual-channel modes.

The DRAM sub-system supports only dual-channel with 64-bit width per channel.

The number of ranks each channel can have populated is one or two.

Mixed mode double-sided SO-DIMMs (x8 and x16 on the same SO-DIMM) are not supported.



### 5.3.1 Rules for Populating SO-DIMM Slots

In all modes, the frequency of system memory will be the lowest frequency of all SO-DIMMs in the system, as determined through the SPD registers on the SO-DIMMs. The GMCH supports only one SO-DIMM connector per channel.

- In dual-channel Interleaved mode, both SO-DIMM slots must be populated and the total amount of memory in each channel must be the same. The device technologies may differ.
- In dual-channel Asymmetric mode, the total memory in the two channels need not be equal (one slot could even be unpopulated).

#### 5.3.1.1 Single-Channel Population Rules for Systems with Intel Management Engine Enabled

Channel 0 should always be populated in either of the below cases, as it will be required for Intel Management Engine operation.

- Intel AMT enabled
- iTPM enabled

In case of Non-AMT AND non-iTPM systems, either Channel 0 or Channel 1 may be populated.

### 5.3.2 Pin Connectivity for Dual-Channel Modes

**Table 10. DDR2/DDR3 Dual-Channel Pin Connectivity**

JEDEC Signal Name	Channel A	Channel B
CK [1:0]	SA_CK [1:0]	SB_CK [1:0]
CKB [1:0]	SA_CK# [1:0]	SB_CK# [1:0]
CSB [1:0]	SA_CS# [1:0]	SB_CS# [1:0]
CKE [1:0]	SA_CKE [1:0]	SB_CKE [1:0]
ODT [1:0]	SA_ODT [1:0]	SB_ODT [1:0]
BS [2:0]	SA_BS [2:0]	SB_BS [2:0]
MA [14:0]	SA_MA [14:0]	SB_MA [14:0]
RAS#	SA_RAS#	SB_RAS#
CAS#	SA_CAS#	SB_CAS#
WE#	SA_WE#	SB_WE#
DQ [63:0]	SA_DQ [63:0]	SB_DQ [63:0]
DQS [7:0]	SA_DQS [7:0]	SB_DQS [7:0]
DM [7:0]	SA_DM [7:0]	SB_DM [7:0]
RESETB <sup>1</sup>		SM_DRAMRST#

**NOTES:**

1. Applicable only in DDR3 mode.



## 5.4 DRAM Clock Generation

The GMCH generates two differential clock pairs for every supported SO-DIMM. There are total of four clock pairs driven directly by the GMCH to two SO-DIMMs.

## 5.5 DDR2/DDR3 On Die Termination

On die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each DQ, DQS/DQS# and DM signal for x8 configurations via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the termination resistance for the DQ, DM, DQS, and DQS# signals to be located inside the DRAM devices themselves instead of on the motherboard. The GMCH drives out the required ODT signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted SO-DIMM rank to enable or disable their termination resistance.

ODT operation follows these general rules:

### WRITE

- Chipset: ODT off
- DRAM:
  - If one slot is populated but has two ranks, turn on termination in the written rank.
  - If one slot/one rank, turn on that rank's termination.

### READ

- Chipset: ODT on
- DRAM: ODT off

## 5.6 DRAM Power Management

The GMCH implements extensive support for power management on the SDRAM interface.

### 5.6.1 Self Refresh Entry and Exit Operation

When entering the Suspend-To-RAM (STR) state, GMCH will flush pending cycles and then enter all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices will perform self-refresh.

## 5.6.2 Dynamic-Power-Down Operation

The GMCH implements aggressive CKE control to dynamically put the DRAM devices in a power down state. The GMCH controller can be configured to put the devices in *active power down* (CKE deassertion with open pages) or *precharge power down* (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages are needed to be closed before putting the devices in power down mode.

If dynamic-power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

## 5.6.3 DRAM I/O Power Management

GMCH implements several power saving features where different groups of IO buffers are disabled when safe to do so in a dynamic fashion thereby saving IO power. These features are listed below.

- SO-DIMM clock disable – The GMCH has two clock pairs per SO-DIMM. If only one SO-DIMM is populated, it allows the other 2 clock pairs to be disabled.
- Unused CKE pins can be tri-stated.
- Address and control tri-state enable – If CKE for any given rank is deasserted, the CS# to that rank is disabled. If all CKEs are deasserted (such as in S3), All address and control buffers (excluding CKEs) are disabled.
- Self refresh master/slave DLL disable - When all the SDRAMs ranks have been put in a self refresh state, all DLLs are disabled.
- Data sense amp disable (self refresh, dynamic) - When all the SDRAM ranks have been put in a self refresh state, or during normal operation, if no memory accesses are pending, the sense amplifiers for all data buffers are turned off.
- Output only sense amp disable – Sense amplifiers of all IO buffers which are functionally outputs only (everything except DQ and DQS) are turned off.

## 5.7 System Memory Throttling

The GMCH has two, independent mechanisms – GMCH Thermal Management and DRAM Thermal Management – that cause system memory bandwidth throttling. For more information on system memory throttling, see [Section 11.3](#).

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## 6 PCI Express-Based External Graphics

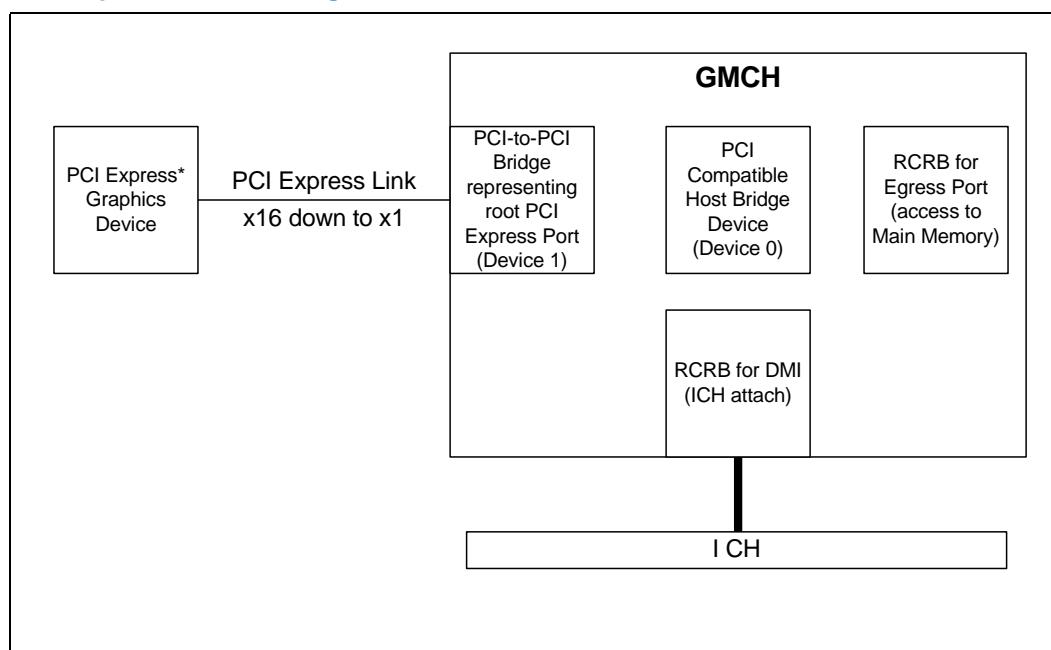
This chapter details the PCI Express interface capabilities of the GMCH and also the digital display ports that can be multiplexed on it. See the PCI Express Specification for details of PCI Express.

This GMCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express Hierarchy. The control registers for this functionality are located in Device1 configuration space and two Root Complex Register Blocks (RCRBs).

### 6.1 PCI Express Configuration Mechanism

The PCI Express (external graphics) link is mapped through a PCI-to-PCI bridge structure.

**Figure 9.** PCI Express Related Register Structures in GMCH



**NOTE:** Details of both the PCI compatible and PCI Express Enhanced configuration mechanisms and transaction rules are provided in the PCI Express Specification.

**Note:** DMA transfers on some latency-sensitive devices may incur completion delays during heavy external PCI Express Graphics traffic to cacheable memory regions. These latency sensitive devices have been typically used in AC mode. The completion delays do not violate platform or industry specifications. If such completion delays are encountered, a system BIOS configuration change to disable C3 allows a device to be serviced during heavy external PCI Express Graphics traffic.



## 6.2 Concurrent Operation of Digital DisplayPorts Multiplexed with the GMCH PCI Express Interface

The GMCH supports concurrent operation of the multiplexed Digital display ports with a x1 PCI Express interface. In addition to supporting video capture, this port may be configured as an additional general-purpose PCIe port, thus bringing the total number of PCIe ports on the Intel Centrino 2 platform to 7.

### 6.2.1 SDVO Multiplexed on the PCI Express Interface

The SDVO interface is muxed onto the PCI Express x16 port pins. The AC/DC specifications are identical to the PCI Express Graphics interface.

SDVO slot reversal is also supported on the GMCH. The GMCH allows SDVO and x1 PCI Express to operate concurrently on the PCI Express-based graphics link.

The PCI Express lanes comprise a standard PCI Express link and must always originate with Lane 0 on the PCI Express connector. The only supported PCI Express width when SDVO is present is x1.

This concurrency is supported in reversed and non-reversed configurations. Mirroring/Reversing are always about the axis between Lane 7 and Lane 8. When SDVO is reversed, SDVO Lane 0 corresponds to what would be PCI Express pin/connector Lane15 (mirrored to higher lane numbers).

Hardware reset straps are used to determine which of the six configurations in Table 11 is desired.

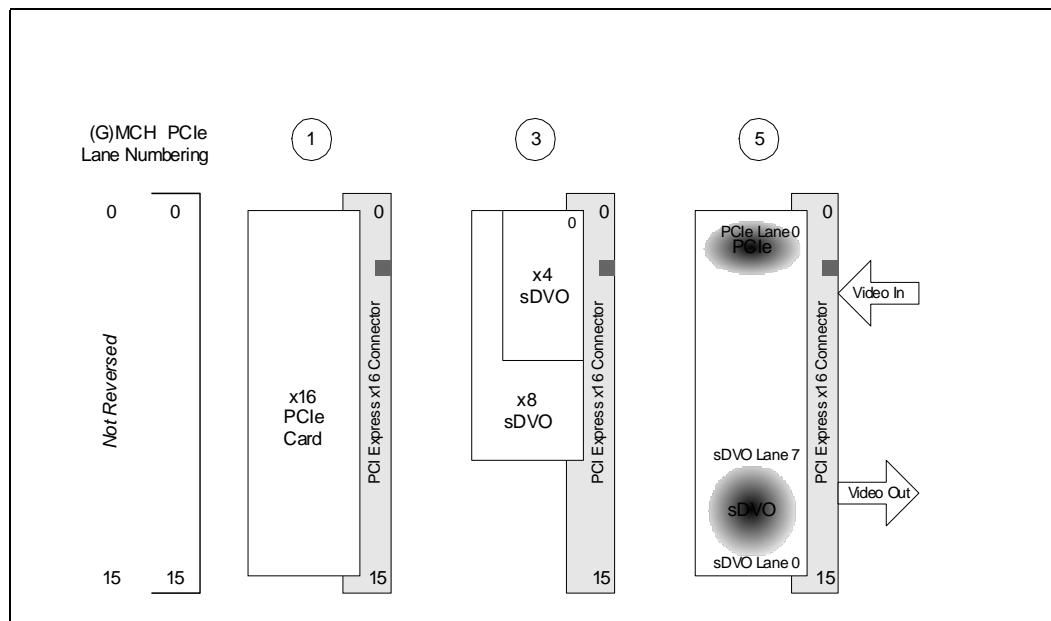
**Table 11. Concurrent SDVO/PCI Express Configuration Strap Controls**

Configuration Number	Description	Slot Reversed Strap (CFG9)	SDVO Present Strap (SDVO_CTRLDATA)	Digital Display Port/PCI Express Concurrent Strap (CFG20)
1	PCI Express*-only not reversed	High	Low	Low
2	PCI Express-only Reversed	Low	Low	Low
3	SDVO-only not reversed	High	High	Low
4	SDVO-only Reversed	Low	High	Low
5	SDVO and PCI Express not reversed	High	High	High
6	SDVO and PCI Express Reversed	Low	High	High

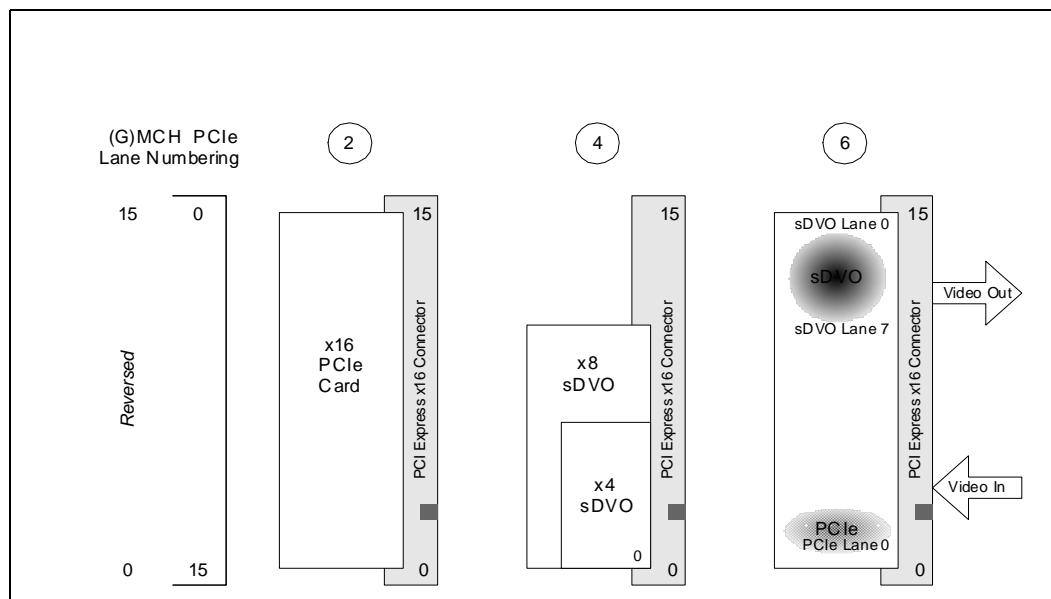
**NOTES:**

1. Details of the implementations corresponding to the configuration number are shown in [Figure 10](#) and [Figure 11](#).
2. SDVO\_CTRLCLK should be pulled up if SDVO\_CTRLDATA is HIGH.

**Figure 10. SDVO/PCI Express Non-Reversed Configurations**



**Figure 11. SDVO/PCI Express Reversed Configurations**





### 6.2.1.1 SDVO Signal Mapping

Table 12 shows the mapping of SDVO signals to the PCI Express lanes in the various possible configurations as determined by the strapping configuration.

**Note:** Slot-reversed configurations do not apply to the integrated graphics only variants.

**Table 12. Configuration Mapping of SDVO Signals on the PCI Express Interface**

SDVO Signal	Configuration-wise Mapping			
	SDVO Only – Normal (3)	SDVO Only – Reversed (4)	Concurrent SDVO and PCI Express – Normal (5)	Concurrent SDVO and PCI Express – Reversed (6)
SDVOB_RED#	PEG_TXN0	PEG_TXN15	PEG_TXN15	PEG_TXN0
SDVOB_RED	PEG_TXP0	PEG_TXP15	PEG_TXP15	PEG_TXP0
SDVOB_GREEN#	PEG_TXN1	PEG_TXN14	PEG_TXN14	PEG_TXN1
SDVOB_GREEN	PEG_TXP1	PEG_TXP14	PEG_TXP14	PEG_TXP1
SDVOB_BLUE#	PEG_TXN2	PEG_TXN13	PEG_TXN13	PEG_TXN2
SDVOB_BLUE	PEG_TXP2	PEG_TXP13	PEG_TXP13	PEG_TXP2
SDVOB_CLK#	PEG_TXN3	PEG_TXN12	PEG_TXN12	PEG_TXN3
SDVOB_CLK	PEG_TXP3	PEG_TXP12	PEG_TXP12	PEG_TXP3
SDVOC_RED#	PEG_TXN4	PEG_TXN11	PEG_TXN11	PEG_TXN4
SDVOC_RED	PEG_TXP4	PEG_TXP11	PEG_TXP11	PEG_TXP4
SDVOC_GREEN#	PEG_TXN5	PEG_TXN10	PEG_TXN10	PEG_TXN5
SDVOC_GREEN	PEG_TXP5	PEG_TXP10	PEG_TXP10	PEG_TXP5
SDVOC_BLUE#	PEG_TXN6	PEG_TXN9	PEG_TXN9	PEG_TXN6
SDVOC_BLUE	PEG_TXP6	PEG_TXP9	PEG_TXP9	PEG_TXP6
SDVOC_CLK#	PEG_TXN7	PEG_TXN8	PEG_TXN8	PEG_TXN7
SDVOC_CLK	PEG_TXP7	PEG_TXP8	PEG_TXP8	PEG_TXP7
SDVO_TVCLKIN#	PEG_RXN0	PEG_RXN15	PEG_RXN15	PEG_RXN0
SDVO_TVCLKIN	PEG_RXP0	PEG_RXP15	PEG_RXP15	PEG_RXP0
SDVOB_INT#	PEG_RXN1	PEG_RXN14	PEG_RXN14	PEG_RXN1
SDVOB_INT	PEG_RXP1	PEG_RXP14	PEG_RXP14	PEG_RXP1
SDVO_FLDSTALL#	PEG_RXN2	PEG_RXN13	PEG_RXN13	PEG_RXN2
SDVO_FLDSTALL	PEG_RXP2	PEG_RXP13	PEG_RXP13	PEG_RXP2
SDVOC_INT#	PEG_RXN5	PEG_RXN10	PEG_RXN10	PEG_RXN5
SDVOC_INT	PEG_RXP5	PEG_RXP10	PEG_RXP10	PEG_RXP5



## 6.2.2 Integrated HDMI/DVI (iHDMI) Multiplexed on the PCI Express Interface

Table 13 shows the mapping of the Integrated HDMI/DVI pins on to the GMCH PCI Express interface.

**Table 13. Configuration Mapping of iHDMI Signals on the PCI Express Interface**

iHDMI Signal Name	Description	Multiplexed with	
		PCIe Normal Operation	PCIe Lane-Reversed
TMDS_B_CLK	HDMI port B Clock	PEG_TXP_3	PEG_TXP_12
TMDS_B_CLK#	HDMI port B Clock complement	PEG_TXN_3	PEG_TXN_12
TMDS_B_DATA0	HDMI port B Data0	PEG_TXP_2	PEG_TXP_13
TMDS_B_DATA0#	HDMI port B Data0 Complement	PEG_TXN_2	PEG_TXN_13
TMDS_B_DATA1	HDMI port B Data1	PEG_TXP_1	PEG_TXP_14
TMDS_B_DATA1#	HDMI port B Data1 Complement	PEG_TXN_1	PEG_TXN_14
TMDS_B_DATA2	HDMI port B Data2	PEG_TXP_0	PEG_TXP_15
TMDS_B_DATA2#	HDMI port B Data2 Complement	PEG_TXN_0	PEG_TXN_15
TMDS_B_HPD#	HDMI port B Hot-plug detect	PEG_RXP_3	PEG_RXP_12
TMDS_C_CLK	HDMI port C Clock	PEG_TXP_7	PEG_TXP_8
TMDS_C_CLK#	HDMI port C Clock complement	PEG_TXN_7	PEG_TXN_8
TMDS_C_DATA0	HDMI port C Data0	PEG_TXP_6	PEG_TXP_9
TMDS_C_DATA0#	HDMI port C Data0 Complement	PEG_TXN_6	PEG_TXN_9
TMDS_C_DATA1	HDMI port C Data1	PEG_TXP_5	PEG_TXP_10
TMDS_C_DATA1#	HDMI port C Data1 Complement	PEG_TXN_5	PEG_TXN_10
TMDS_C_DATA2	HDMI port C Data2	PEG_TXP_4	PEG_TXP_11
TMDS_C_DATA2#	HDMI port C Data2 Complement	PEG_TXN_4	PEG_TXN_11
TMDS_C_HPD#	HDMI port C Hot-plug detect	PEG_RXP_7	PEG_RXP_8

**NOTE:** DisplayPort multiplexed on the PCI Express Interface.

Table 14 shows the mapping of the DisplayPort pins on to the GMCH PCI Express interface.

**Table 14. Configuration Mapping of DisplayPort Signals on the PCI Express Interface**

DisplayPort Signal Name	Description	Multiplexed with	
		PCIE Normal Operation	PCIE Lane-Reversed
DPB_LANE3	DisplayPort B Lane3	PEG_TXP_3	PEG_TXP_12
DPB_LANE3#	DisplayPort B Lane3 Complement	PEG_TXN_3	PEG_TXN_12
DPB_LANE2	DisplayPort B Lane2	PEG_TXP_2	PEG_TXP_13
DPB_LANE2#	DisplayPort B Lane2 Complement	PEG_TXN_2	PEG_TXN_13
DPB_LANE1	DisplayPort B Lane1	PEG_TXP_1	PEG_TXP_14
DPB_LANE1#	DisplayPort B Lane1 Complement	PEG_TXN_1	PEG_TXN_14
DPB_LANE0	DisplayPort B Lane0	PEG_TXP_0	PEG_TXP_15
DPB_LANE0#	DisplayPort B Lane0 Complement	PEG_TXN_0	PEG_TXN_15
DPB_HPD#	DisplayPort B Hot-plug detect	PEG_RXP_3	PEG_RXP_12
DPB_AUX	DisplayPort B Aux	PEG_RXP_2	PEG_RXP_13
DPB_AUX#	DisplayPort B Aux Complement	PEG_RXN_2	PEG_RXN_13
DPC_LANE3	DisplayPort C Lane3	PEG_TXP_7	PEG_TXP_8
DPC_LANE3#	DisplayPort C Lane3 Complement	PEG_TXN_7	PEG_TXN_8
DPC_LANE2	DisplayPort C Lane2	PEG_TXP_6	PEG_TXP_9
DPC_LANE2#	DisplayPort C Lane2 Complement	PEG_TXN_6	PEG_TXN_9
DPC_LANE1	DisplayPort C Lane1	PEG_TXP_5	PEG_TXP_10
DPC_LANE1#	DisplayPort C Lane1 Complement	PEG_TXN_5	PEG_TXN_10
DPC_LANE0	DisplayPort C Lane0	PEG_TXP_4	PEG_TXP_11
DPC_LANE0#	DisplayPort C Lane0 Complement	PEG_TXN_4	PEG_RXN_11
DPC_HPD#	DisplayPort C Hot-plug detect	PEG_RXP_7	PEG_RXP_8
DPC_AUX	DisplayPort C Aux	PEG_RXP_6	PEG_RXP_9
DPC_AUX#	DisplayPort C Aux Complement	PEG_RXN_6	PEG_RXN_9
DPD_LANE3	DisplayPort D Lane3	PEG_TXP_11	PEG_TXP_4
DPD_LANE3#	DisplayPort D Lane3 Complement	PEG_TXN_11	PEG_TXN_4
DPD_LANE2	DisplayPort D Lane2	PEG_TXP_10	PEG_TXP_5
DPD_LANE2#	DisplayPort D Lane2 Complement	PEG_TXN_10	PEG_TXN_5
DPD_LANE1	DisplayPort D Lane1	PEG_TXP_9	PEG_TXP_6
DPD_LANE1#	DisplayPort D Lane1 Complement	PEG_TXN_9	PEG_TXN_6
DPD_LANE0	DisplayPort D Lane0	PEG_TXP_8	PEG_TXP_7
DPD_LANE0#	DisplayPort D Lane0 Complement	PEG_TXN_8	PEG_TXN_7
DPD_HPD#	DisplayPort D Hot-plug detect	PEG_RXP_11	PEG_RXP_4
DPD_AUX	DisplayPort D Aux	PEG_RXP_10	PEG_RXP_5
DPD_AUX#	DisplayPort D Aux Complement	PEG_RXN_10	PEG_RXN_5

**Table 15. Concurrent DisplayPort (HDMI)/PCI Express Configuration Strap Controls**

Configuration Number	Description	Local Flat Panel (LFP) Present Strap (L_DDC_DATA)	DP/HDMI Present Strap (DDPC_CTRLDATA)	SDVO Present Strap (SDVO_CTRLDATA)	Digital Display Port/PCI Express Concurrent Strap (CFG20)
1	DP/HDMI Port-B enabled	X	X	High	Low
2	DP/HDMI Port-C enabled	X	High	High	Low
3	DP Port-D enabled	High	X	High	Low
4	DP/HDMI Port-B and PCI Express*	X	X	High	High
5	DP/HDMI Port-C and PCI Express	X	High	High	High
6	DP Port-D and PCI Express	High	X	High	High

**NOTES:**

1. SDVO\_CTRLCLK should be pulled up if SDVO\_CTRLDATA is HIGH.
2. DDPC\_CTRLCLK should be pulled up if DDPC\_CTRLDATA is HIGH.
3. L\_DDC\_CLK should be pulled up if L\_DDC\_DATA is HIGH.

### 6.3 Co-Existence of DisplayPorts

In Integrated Graphics mode, a maximum of two DisplayPorts can simultaneously operate on the GMCH. See [Section 8.4](#) for a matrix detailing the possible combinations.

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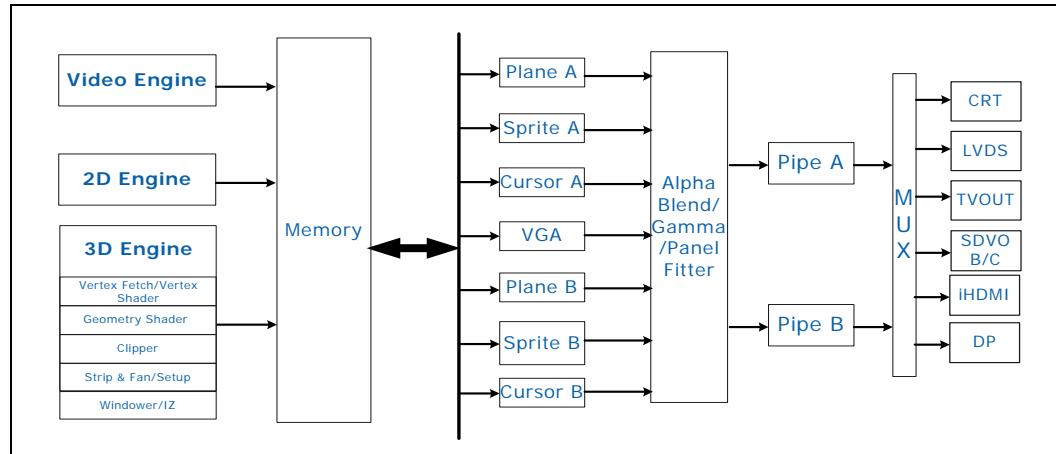
## 7 Integrated Graphics Controller

This chapter details the chipset integrated graphics engines (3D, 2D and Video), 3D pipeline and their respective capabilities.

The GMCH graphics is powered by the Gen-5.0 Graphics Architecture and supports ten fully programmable execution cores, enabling greater performance than previous generation chipsets. GMCH graphics supports full-precision, floating-point operations to enhance the visual experience of compute-intensive applications.

The GMCH internal graphics devices (IGD) contain several types of components. The major components in the IGD are the engines, planes, pipes and ports. The GMCH has a 3D/2D Instruction Processing unit to control the 3D and 2D engines respectively. The IGD's 3D and 2D engines are fed with data through the memory controller. The outputs of the engines are surfaces sent to memory, which are then retrieved and processed by GMCH planes.

**Figure 12. GMCH Graphics Controller Block Diagram**



### 7.1 Gen 5.0 3D and Video Engines for Graphics Processing

The 3D graphics pipeline for the chipset has a deep pipelined architecture in which each stage can simultaneously operate on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine.

The Gen 5.0 3D engine also has a number of performance and power-management enhancements, providing improved power/performance ratios over the Gen 4.0 IGD. These include:

- Execution Units increased to 10 from 8 EU's
- Support for full decoding of VC-1 and AVC in hardware
- Graphics support for Intel Virtualization Technology DMA
- Improved Anti-aliasing support in hardware



## 7.1.1 3D Engine Execution Units (EUs)

The 3D processing hardware includes support for two more EUs over the previous generation. The EUs perform 128-bit wide execution per clock and are support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing.

## 7.1.2 3D Pipeline

### 7.1.2.1 Vertex Fetch (VF) Stage

The VF stage performs one major function: executing 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as OpenGL.

### 7.1.2.2 Vertex Shader (VS) Stage

The VS stage of the Gen 5.0 3D pipeline is used to perform shading of vertices output by the VF function. The VS unit will thus produce an output vertex reference for every input vertex reference received from the VF unit, in the order received.

### 7.1.2.3 Geometry Shader Stage

As a stage of the Gen 5.0 3D pipeline, the GS stage receives inputs from the previous (VS) stage. Compiled application-provided GS shader programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from those edges.

### 7.1.2.4 Clip Stage

The CLIP stage can be used to perform general processing on incoming 3D objects. However, it also includes specialized logic to perform a ClipTest function on incoming object. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

### 7.1.2.5 Strips and Fans Stage

The Strips and Fans (SF) stage of the Gen 5.0 3D pipeline is responsible for performing setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage comprise of implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

### 7.1.2.6 Windower/IZ (WIZ) Stage

The WIZ unit performs an early depth test, a major performance-optimization feature where failing pixels are removed, thus eliminating unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels.

The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering tends to diffuse the sharp color bands seen on smooth-shaded objects.



## 7.2 Video Engine

The Video Engine handles the non-3D (media/video) applications. It includes support for full MPEG2, VC-1 and AVC decode in hardware to support high-definition content, including next generation optical media (Blu-Ray Disc). The Gen 5.0 chipset engine includes a number of encompassments over the previous generation capabilities, which have been listed above. More details will be provided in a future revision of this document.

## 7.3 2D Engine

The GMCH contains BLT (Block Level Transfer) functionality and an extensive set of 2D instructions. To take advantage of the 3D drawing engine's functionality, some BLT functions make use of the 3D renderer.

### 7.3.1 Chipset VGA Registers

The 2D registers are a combination of registers for the original Video Graphics Array (VGA) and others to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

### 7.3.2 Logical 128-Bit Fixed BLT and 256 Fill Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows\* operating systems. The 128-bit GMCH BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8 x 8 pixels wide and may be 8, 16, or 32 bits per pixel.

The BLT engine has the ability to expand monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the GMCH can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

The GMCH has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The GMCH can perform hardware clipping during BLTs.

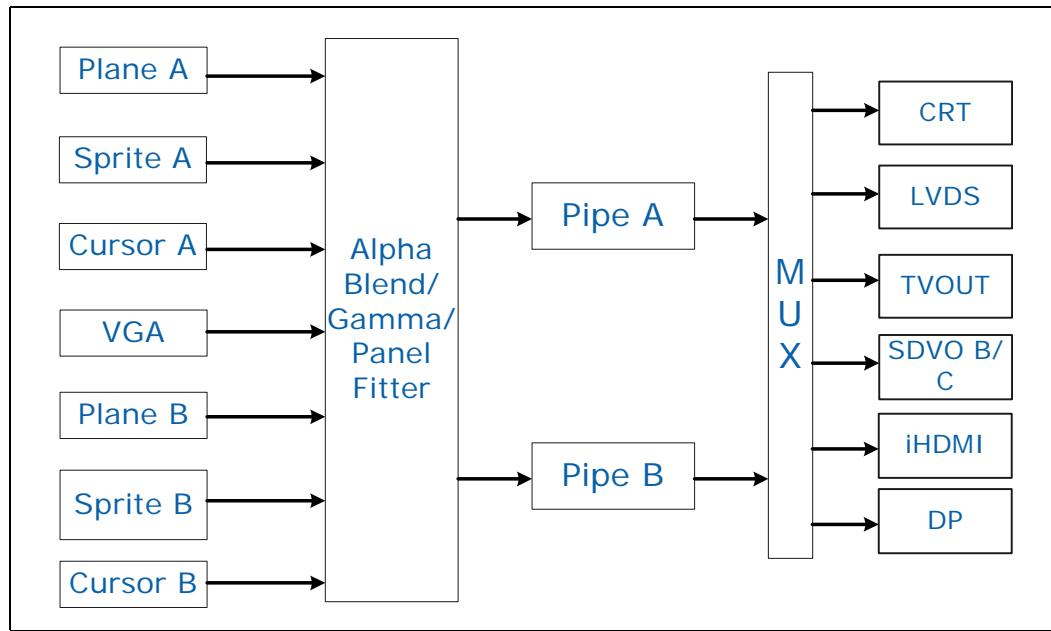
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## 8 *Display Interfaces*

The display converts a set of source images or surfaces, combines them and sends them out at the proper timing to an output interface connected to a display device. Along the way, the data can be converted from one format to another, stretched or shrunk, and color corrected or gamma converted.

This chapter details the units of the GMCH that perform the action of formatting and displaying the images generated by the IGD's graphics engines.

**Figure 13. Mobile Intel 4 Series Express Chipset Family Display Block Diagram**



### 8.1 GMCH Display Overview

Integrated Graphics Display on the GMCH can be broken down into three components:

- Display Planes
- Display Pipes
- DisplayPorts

#### 8.1.1 Display Planes

A Display Plane is a single displayed surface in memory, usually containing one image (desktop, cursor, overlay). It is the portion of the display HW logic which defines the format and location of a rectangular region of memory that can be displayed on display output device and delivers that data to a display pipe. This is clocked by the Core Display Clock.



### 8.1.1.1 Planes A and B

Planes A and B are the main display Planes and are associated with Pipes A and B respectively. The two display pipes are independent, allowing for support of two independent display streams. They are both double-buffered, thus minimizing latency and improving visual quality.

### 8.1.1.2 Sprite A and B

Sprite A and Sprite B are planes optimized for video decode, and are associated with Planes A and B respectively. Sprite A and B are also double-buffered. Overlay is supported through Sprite.

**Note:**

1. Overlay color control feature (brightness, contrast and saturation) is not supported
2. Overlay does not support planar YUV format (IMC3 and YUV12)

### 8.1.1.3 Cursors A and B

Cursors A and B are small, fixed-sized planes dedicated for mouse cursor acceleration, and are associated with Planes A and B, respectively. These planes support resolutions up to 256 x 256 each.

### 8.1.1.4 VGA

Used for boot, safe mode, legacy games etc. Can be changed by an application without OS/driver notification, due to legacy requirements.

## 8.1.2 Display Pipes

The display pipe blends and synchronizes pixel data received from one or more display planes and adds the timing of the display output device upon which the image is to be displayed. This is clocked by the Display Reference clock inputs to the GMCH.

The display pipes A and B operate independently of each other at the rate of 1 pixel per clock. They can attach to any of the display ports.

## 8.1.3 DisplayPorts

The DisplayPorts comprise output logic and pins that transmit the data to a display device (CRT, panel, TV etc.) and the associated encoding logic. These are clocked by GMCH clock outputs corresponding to the particular display device in use. This chapter shall primarily discuss DisplayPorts. The GMCH supports the following DisplayPorts:

- Analog
  - CRT
  - TV out
- Digital
  - LVDS
  - SDVOB & SDVOC
  - iHDMI
  - DisplayPort (DP)

The next sections detail the capabilities of the analog and digital DisplayPorts.

## 8.2 Analog DisplayPorts

### 8.2.1 CRT

The analog DisplayPort provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality has been added to the signals to enhance that capability.

**Table 16. Analog Port Characteristics**

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	3.3 V
	Enable/Disable	Port control
	Polarity Adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5 V
	Control	Through GPIO interface

#### 8.2.1.1 Integrated DAC

The display function contains a Digital-to-Analog Converter (DAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor, capable of supporting resolutions up to QXGA.

#### 8.2.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support is included.

### 8.2.2 TV

The GMCH converts RGB data into various analog television standards (NTSC, PAL) and formats (composite, S-Video) and provides it via the TV port. The data can be either interlaced or progressive format. The TVout port has one 10-bit DAC for each of the three analog outputs.

## 8.3 Digital DisplayPorts

### 8.3.1 LVDS

LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics.

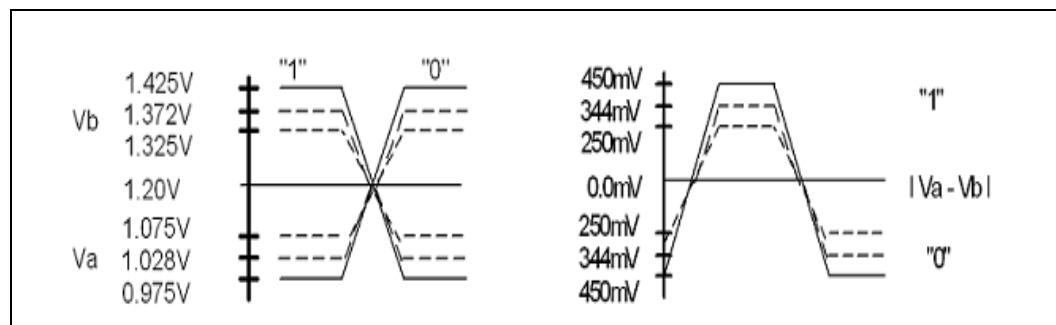
Each channel supports transmit clock frequency ranges from 25 MHz to 112 MHz, which provides a throughput of up to 784 Mbps on each data output and up to 112 MP/s on the input. When using both channels, each carry a portion of the data, thus doubling the throughput to a maximum theoretical pixel rate of 224 MP/s.

There are two LVDS transmitter channels (Channel A and Channel B) in the LVDS interface. Channel A and Channel B consist of 4-data pairs and a clock pair each.

The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals.

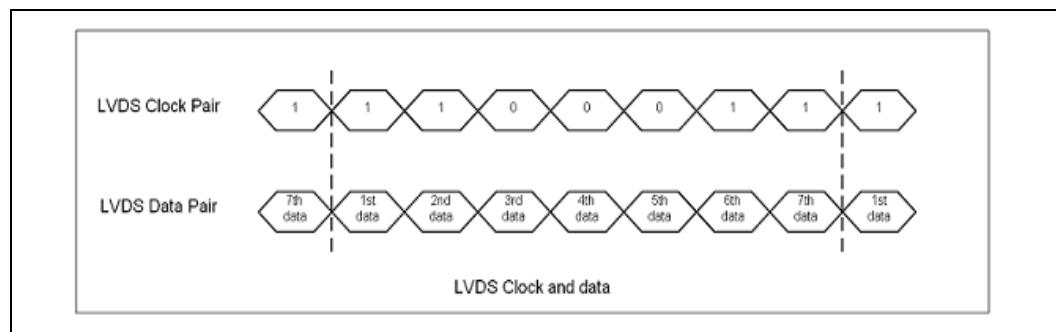
Figure 14 shows a pair of LVDS signals and swing voltage.

**Figure 14. LVDS Signals and Swing Voltage**



1's and 0's are represented the differential voltage between the pair of signals. As shown in the Figure 15 a serial pattern of 1100011 represents one cycle of the clock.

**Figure 15. LVDS Clock and Data Relationship**





### 8.3.1.1 LVDS Pair States

The LVDS pairs can be put into one of five states:

- Active
- Powered down tri-state
- Powered down 0 V
- Common mode
- Send zeros

When in the active state, several data formats are supported. When in powered down state, the circuit enters a low-power state and drives out OV or tri-states on both the output pins for the entire channel. The common mode tri-state is both pins of the pair set to the common mode voltage. When in the send zeros state, the circuit is powered up but sends only zero for the pixel color data regardless what the actual data is with the clock lines and timing signals sending the normal clock and timing data.

The LVDS Port can be enabled/disabled via Software. A disabled port enters a low-power state. Once the port is enabled, individual driver pairs may be disabled based on the operating mode. Disabled drivers can be powered down for reduced power consumption or optionally fixed to forced 0's output.

Individual pairs or sets of LVDS pairs can be selectively powered down when not being used. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

### 8.3.1.2 Single-Channel versus Dual-Channel Mode

In the single channel mode, only Channel-A is used. Channel-B cannot be used for single channel mode. In the dual-channel mode, both Channel-A and Channel-B pins are used concurrently to drive one LVDS display.

In Single-channel mode, Channel A can take 18 bits of RGB pixel data, plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on three differential data pair outputs; or 24 bits of RGB (plus 4 bits of timing control) output on four differential data pair outputs. A dual-channel interface converts 36 or 48 bits of color information plus the 3 or 4 bits of timing control respectively and outputs it on six or eight sets of differential data outputs respectively.

Dual-channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single channel. In general, one channel will be used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel will be sent out Channel-A. All horizontal timings for active, sync, and blank will be limited to be on two pixel boundaries in the two channel modes.

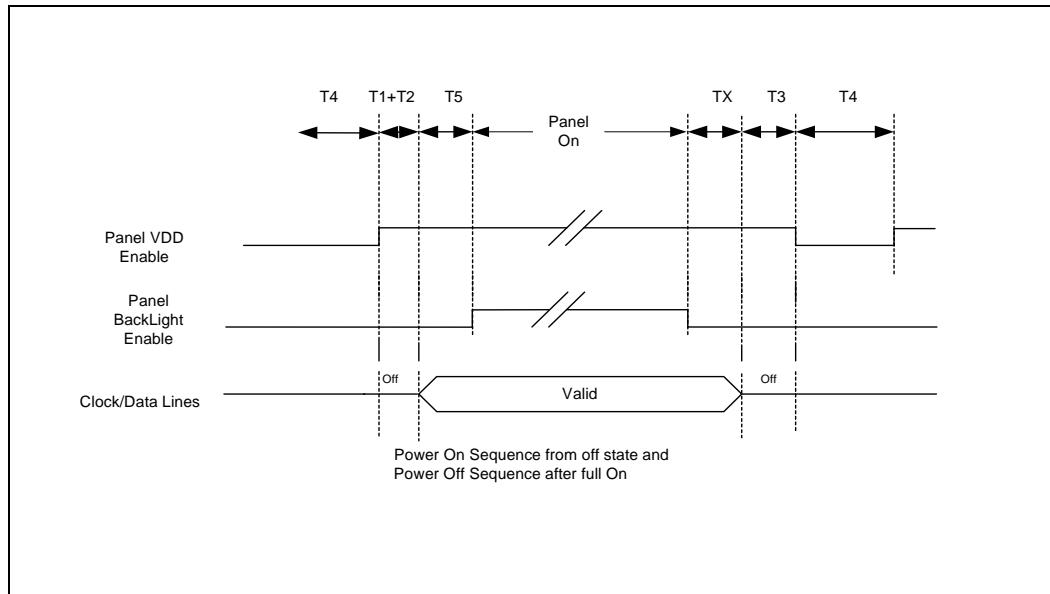
**Note:** The GMCH supports 2- bpp display panels of Type 1 only (compatible with VESA LVDS color mapping).

### 8.3.1.3 Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. To meet the panel power timing specification requirements two signals, LFP\_VDD\_EN and LFP\_BKLT\_EN, are provided to control the timing sequencing function of the panel and the backlight power supplies.

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

**Figure 16. Panel Power Sequencing**



**NOTE:** Support for programming parameters TX and T1 through T5 via SW is provided.

#### 8.3.1.4 LVDS DDC

The display pipe selected by the LVDS display port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then "locked" into the registers to prevent unwanted corruption of the values. From that point on, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA.

#### 8.3.2 iHDMI

The GMCH supports integrated HDMI multiplexed onto the PCI Express interface. For details on the pin-mapping, see [Chapter 6](#). As the PCI Express interface is AC coupled, a level-shifter is required to translate the signals to the HDMI logic levels. The integrated solution saves BOM cost compared to HDMI over SDVO.

The GMCH provides two ports capable of supporting HDMI. However, Intel HD Audio can be supported on any one of the iHDMI ports at any given point. A separate audio path shall be required for the other port.

For Integrated HDMI, the integrated HDMI transmitter receives both the digital video and audio data which it synchronizes before it transmits the data across a single cable connection to the HDMI receiver on the HDMI sink.

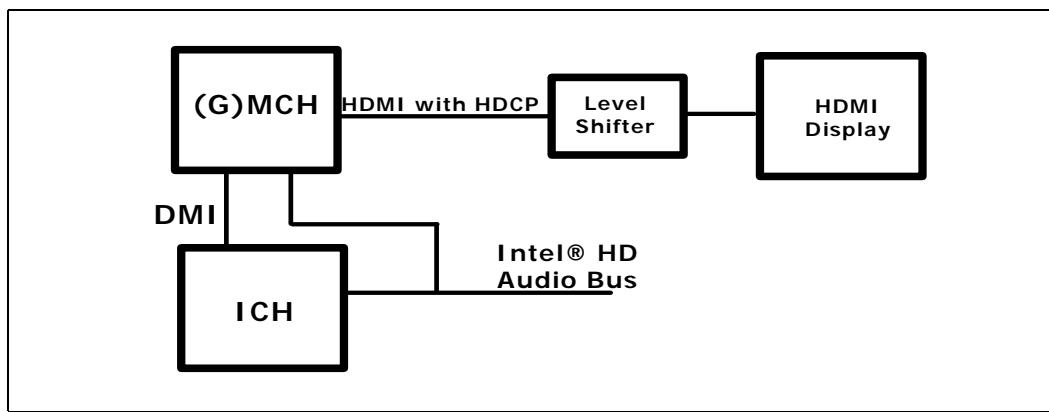
**Note:**

1. Even V-Total Interlaced mode is not supported.
2. Integrated Intel High Definition Audio can be used only with iHDMI.
3. OEMs need to ensure that when using integrated Intel High Definition Audio, the Intel High Definition Audio power supply on the ICH side also needs to be 1.5 V. If not, damage to the GMCH may result.

### 8.3.2.1    **HDCP**

The GMCH supports HDCP via the iHDMI interface on any one iHDMI port at a given point. A high-level block diagram of integrated HDMI/HDCP on the Intel Centrino 2 platform is in [Figure 17](#).

**Figure 17.    Integrated HDMI w/HDCP on Intel Centrino 2**



### 8.3.3    **DisplayPort (DP)**

The DisplayPort abbreviated as DP (different than the generic term display port) specification is a VESA standard aimed at consolidating internal and external connection methods to reduce device complexity, supporting key cross industry applications, and providing performance scalability to enable the next generation of displays. The GMCH supports HDCP on the DP interface also.

The DP is multiplexed onto the PCI Express interface. For details on the pin-mapping, see [Chapter 6](#).

The GMCH has 3 DP ports, each capable of supporting link-speeds of 1.62 Gbps and 2.7 Gbps on 1, 2 or 4 data lanes.

**Note:**

1. Even V-Total Interlaced mode is not supported.
2. The GMCH can support a maximum of 2 DP ports simultaneously. See [Section 8.4](#) for details.
3. The “Embedded DisplayPort (eDP)” is a dedicated DP port for the embedded display (e.g., Local Flat Panel) and is supported via port D of the DP interface. Ports B and C of the DP interface are also occasionally referred to as the “Integrated DisplayPort”.

### 8.3.3.1 DP Aux Channel

A bi-directional AC coupled AUX channel interface replaces the I<sup>2</sup>C on the DP. These pins are also muxed onto the PCI Express interface. I<sup>2</sup>C-to-Aux bridges shall be required to connect legacy EDID DP devices.

### 8.3.3.2 DP Hot-Plug Detect (HPD)

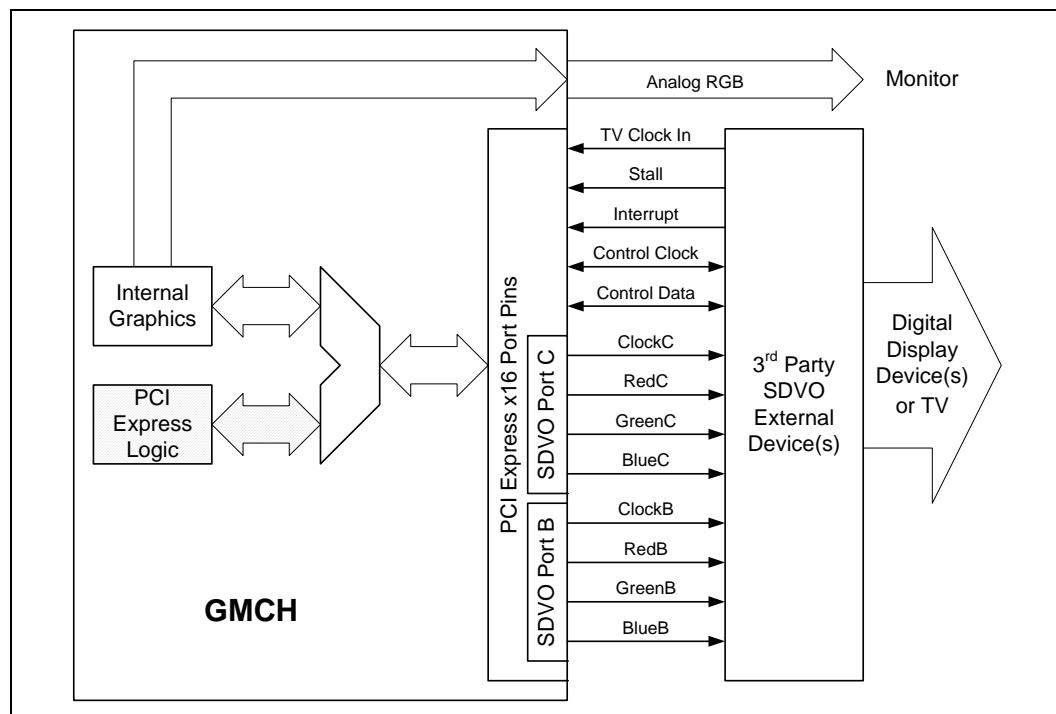
The GMCH supports HPD for Hot-Plug and sink events on the DP interface.

## 8.3.4 SDVO

SDVO supports a variety of display types – LVDS, DVI, TV-Out, HDMI, and external CE type devices. Though the SDVO electrical interface is based on the PCI Express interface, the protocol and timings are completely unique. The GMCH utilizes an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings.

The internal graphics controller can have one or two SDVO ports multiplexed on the x16 PCI Express interface.

**Figure 18. SDVO Conceptual Block Diagram**



The ports can be dynamically configured in the following modes:

- Standard – Baseline SDVO functionality. Supports Pixel Rates between 25 and 225 MP/s. Utilizes three data pairs to transfer RGB data.
- Dual Standard – Utilizes two standard data streams across both SDVO B and SDVO C. There are two types of dual standard modes:
  - Dual Independent Standard - Each SDVO channel will see a different pixel stream. The data stream across SDVO B will not be the same as the data stream across SDVO C.



- Dual Simultaneous Standard - Both SDVO channels will see the same pixel stream from a single pixel pipeline. The display timings will be identical, but the transfer timings may not, for example the timing between the two channels as seen at the SDVO device(s) may not be perfectly aligned.

#### 8.3.4.1 SDVO Control Bus

The SDVO Control clock (SDVO\_CTRLCLK) and data (SDVO\_CTRLDATA) provide similar functionality to I<sup>2</sup>C. Traffic destined for the PROM or DDC will travel across the control bus, and will then require the SDVO device to act as a switch and direct traffic from the control bus to the appropriate receiver. Additionally, the control bus can operate at up to 1 MHz.

## 8.4 Co-Existence of DisplayPorts

The Table 17 describes the valid interoperability between display technologies.

- **Single Pipe Single Display** is a mode with one display port activated to display the output to one display device.
- **Intel® Dual Display Clone** is a mode with both display ports activated to display the same output to two different display devices with the same color depth setting, but different refresh rate and resolution settings.
- **Intel® Dual Display Twin** is a mode with one display port activated to display the same output to two different display devices with the same color depth, refresh rate, and resolution settings.
- **Extended Desktop** is a mode with both display ports activated used to display two different outputs to two different display devices with different color depth, refresh rate, and resolution settings.

Table 17. DisplayPort Co-Existence Table (Sheet 1 of 2)

Display		Not Attached	DAC	Integrated LVDS	TV Out	Integrated DP	HDMI
			CRT		TV		
Not Attached		X	S	S	S	S	S
DAC	CRT	S	X	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E	A	A
Integrated LVDS		S	S <sup>1</sup> , C, E, T	X	S <sup>1</sup> , C, E	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E, T
TV Out	TV	S	S <sup>1</sup> , C, E	S <sup>1</sup> , C, E	X	S <sup>1</sup> , C, E	S <sup>1</sup> , C, E
Integrated DP		S	A	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E	A	A
HDMI		S	A	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E	A	X
SDVO CRT		S	A	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E	A	A
SDVO DVI		S	A	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E	A	A
SDVO HDMI		S	A	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E	A	X

**Table 17. DisplayPort Co-Existence Table (Sheet 2 of 2)**

Display	Not Attached	DAC	Integrated LVDS	TV Out	Integrated DP	HDMI
		CRT		TV		
<b>SDVO LVDS</b>	S	S <sup>1</sup> , C, E, T	X	S <sup>1</sup> , C, E	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E, T
<b>SDVO TV</b>	S	S <sup>1</sup> , C, E	S <sup>1</sup> , C, E	X	S <sup>1</sup> , C, E	S <sup>1</sup> , C, E
<ul style="list-style-type: none"> <li>• A = Single Pipe Single Display, Dual Display Clone/Twin Mode (Only 24 bpp), or Extended Desktop Mode</li> <li>• C = Clone Mode</li> <li>• E = Extended Desktop Mode</li> <li>• S = Single Pipe Single Display</li> <li>• S<sup>1</sup> = Single Pipe Single Display With One Display Device Disabled</li> <li>• T = Twin Mode (Only 24 bpp) Supported By Displaying SSC Clock</li> <li>• X = Unsupported</li> </ul>						

**Table 18. Display Port Co-Existence Table**

Display		SDVO CRT	SDVO DVI	SDVO HDMI	SDVO LVDS	SDVO TV
Not Attached		S	S	S	S	S
DAC	CRT	A	A	A	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E
<b>Embedded DP</b>		S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E, T	X	S <sup>1</sup> , C, E
<b>Integrated LVDS</b>		S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E, T	X	S <sup>1</sup> , C, E
<b>TV Out</b>	<b>TV</b>	S <sup>1</sup> , C, E	X			
<b>Integrated DP</b>		A	A	A	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E
<b>HDMI</b>		A	A	X	S <sup>1</sup> , C, E, T	S <sup>1</sup> , C, E
<b>SDVO CRT</b>		A	A	A	A	A
<b>SDVO DVI</b>		A	A	A	A	A
<b>SDVO HDMI</b>		A	A	X	A	A
<b>SDVO LVDS</b>		A	A	A	X	A
<b>SDVO TV</b>		A	A	A	A	A
<ul style="list-style-type: none"> <li>• A = Single Pipe Single Display, Dual Display Clone/Twin Mode (Only 24 bpp), or Extended Desktop Mode</li> <li>• C = Clone Mode</li> <li>• E = Extended Desktop Mode</li> <li>• S = Single Pipe Single Display</li> <li>• S<sup>1</sup> = Single Pipe Single Display With One Display Device Disabled</li> <li>• T = Twin Mode (Only 24 bpp) Supported By Displaying SSC Clock</li> <li>• X = Unsupported</li> </ul>						

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## 9 Power Management and Sequencing

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This chapter details the various power management capabilities of the GMCH.

### 9.1 Power Management Features

Refer to the *ACPI Specification Revision 3.0* for an overview of the system power states mentioned in this chapter.

#### 9.1.1 Dynamic Power Management on I/O

The GMCH provides several features to reduce I/O power dynamically.

##### 9.1.1.1 Host

- H\_DPWR# signal disables processor sense amps when no read return data is pending.

##### 9.1.1.2 System Memory

- Dynamic-power-down of unused ranks of memory.
- Intel Rapid Memory Power Management conditionally places memory into self-refresh based on C state, PCI Express link states, and graphics/display activity.

##### 9.1.1.3 PCI Express

- Active power management support using L0s, and L1 states.
- All inputs and outputs disabled in L2/L3 Ready state.

##### 9.1.1.4 DMI

- Active power management support using L0s/L1 state.
- All inputs and outputs disabled in L2/L3 Ready state.

##### 9.1.1.5 Intel Management Engine

- Active power management support for Intel AMT capable systems via M0, M1 and M-off states.

## 9.1.2 System Memory Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

### 9.1.2.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a SO-DIMM connector in which it is not connected to any actual memory devices (such as SO-DIMM connector is unpopulated, or is single-sided) will be tri-stated.

The benefits of disabling unused SM signals are:

- Reduce power consumption
- Reduce possible overshoot/undershoot signal quality issues seen by the GMCH I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated (as determined by the DRAM Rank Boundary register values) then the corresponding chip select and SCKE signals will not be driven.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

### 9.1.2.2 Dynamic Power Management of Memory

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. If the pages for a rank have all been closed at the time of power down, then the device will enter the precharge power-down state. If pages remain open at the time of power-down the devices will enter the active power-down state.

### 9.1.2.3 Conditional Self-Refresh

The GMCH supports Intel Rapid Memory Power Management which conditionally places memory into self-refresh in the C3, C4, C5 and Deep Power-Down Technology (code named C6) state, based on the graphics/display (if internal graphics is being used) and on the state of the PCI Express links.

The target behavior is to enter self-refresh for C3/C4/C5/Deep Power-Down Technology (code named C6) state as long as there is no memory requests to service. The target usage is shown in the [Table 19](#).

**Table 19. Targeted Memory State Conditions**

Mode	Memory State with Internal Graphics	Memory State with External Graphics
C0, C1, C2	Dynamic memory rank power-down based on idle conditions.	Dynamic memory rank power-down based on idle conditions.
C3, C4, C5, Deep Power Down Technology (code named C6)	Dynamic memory rank power-down based on idle conditions. If graphics engine is idle, no display requests, and permitted display configuration, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.	Dynamic memory rank power-down based on idle conditions. If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power down based on idle conditions.
S3	Self Refresh Mode	Self Refresh Mode
S4	Memory power-down (contents lost)	Memory power-down (contents lost)



## 9.2 ACPI States Supported

This section details the support provided by the GMCH corresponding to the various CPU/Display/System ACPI states. Descriptions provided in this section shall be used in [Section 9.4](#).

### 9.2.1 System

State	Description
G0/S0	Full On
G1/S1	Not supported
G1/S2	Not supported
G1/S3-Cold	Suspend to RAM (STR). Context saved to memory (S3-Hot is not supported by the GMCH)
G1/S4	Suspend to Disk (STD). All power lost (except wakeup on ICH)
G2/S5	Soft off. All power lost (except wakeup on ICH). Total reboot
G3	Mechanical off. All power (AC and battery) removed from system

### 9.2.2 Processor

State	Description
C0	Full On
C1/C1E	Auto Halt
C2/C2E	Stop Grant. Clock stopped to processor core.
C3	Deep Sleep. Clock to processor stopped.
C4/C4E	Deeper Sleep. Same as C3 with reduced voltage on the processor.
C5	Enhanced Deeper Sleep. Lower core voltage than C4 and L2 cache flushed.
Deep Power Down Technology (code named C6)	Deep Power Down Technology state. Core power below VCC_min, with L2 cache invalidated.

### 9.2.3 Internal Graphics Display Device Control

State	Description
D0	Display Active
D1	Low-power state, low latency recovery, Standby display
D2	Suspend display
D3	power-off display

## 9.2.4 Internal Graphics Adapter

State	Description
D0	Full on, display active
D3 Cold	power-off

## 9.3 Interface Power States Supported

### 9.3.1 PCI Express Link States

State	Description
L0	Full on – Active transfer state
L0s	First Active Power Management low-power state – Low exit latency
L1	Lowest Active Power Management - Longer exit latency
L2/L3 Ready	Lower link state with power applied – Long exit latency
L3	Lowest power state (power-off) – Longest exit latency

### 9.3.2 Main Memory States

State	Description
Power up	CKE asserted. Active mode
Pre-charge Power down	CKE deasserted (not self-refresh) with all banks closed
Active Power down	CKE deasserted (not self-refresh) with min. one bank active
Self-Refresh	CKE deasserted using device self-refresh



## 9.4 Chipset State Combinations

GMCH supports the state combinations listed in the [Table 20](#) and [Table 21](#).

**Table 20.** G-, S- and C-State Combinations

Global (G) State	Sleep (S) State	CPU (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1	Auto-Halt	On	Auto Halt
G0	S0	C2	Stop Grant	On	Stop Grant
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C4	Deeper Sleep	On	Deep Sleep with processor voltage lowered.
G0	S0	IC5/Deep Power Down Technology (code named C6)		On	Deep Sleep with processor voltage lowered.
G1	S3	power-off	-	Off, except RTC	Suspend to RAM
G1	S4	power-off	-	Off, except RTC	Suspend to Disk
G2	S5	power-off	-	Off, except RTC	Soft Off
G3	NA	power-off	-	power-off	Hard Off

**Table 21.** D-, S-, and C-State Combinations

Graphics Adapter (D) State	Sleep (S) State	CPU (C) State	Display Device State
D0	S0	C0	Displaying
D0	S0	C1	Displaying
D0	S0	C2	Displaying
D0	S0	C3	Displaying
D0	S0	C4	Displaying
D0	S0	C5/Deep Power Down Technology (code named C6)	Displaying
D3	S0	C0-2/ C3/C4/C5/Deep Power Down Technology (code named C6)	Not Displaying
D3	S3	-	Not Displaying GMCH may power-off
D3	S4	-	Not Displaying Suspend to disk



#### 9.4.1 CPU Sleep (H\_CPUSLP#) Signal Definition

The processor's sleep signal (SLP#) reduces power in the processor by gating off unused clocks in the C2-popup states or lower. This signal can be driven only by the GMCH's H\_CPUSLP# signal.

The GMCH host interface controller will ensure that no transactions will be initiated on the FSB without having first met the required timing from the SLP# deassertion to the assertion of BPRI#.

GMCH will control H\_CPUSLP# and enforce the associated configured timing rules associated.

### 9.5 CLKREQ# - Mode of Operation

The CLKREQ# signal is driven by the GMCH to control the PCI Express clock to the external graphics and the DMI clock. When both the DMI and PCI Express links (if supported) are in L1, with CPU in C4 (and lower states), the GMCH deasserts CLKREQ# to the clock chip, allowing it to gate the GCLK differential clock pair to the GMCH, in turn disabling the PCI Express and DMI clocks inside the GMCH. For the GMCH to support CLKREQ# functionality, ASPM must be enabled on the platform.

### 9.6 Intel® Display Power Saving Technology (Intel® DPST) 4.0

Intel DPST maintains apparent visual experience by managing display image brightness and contrast while adaptively dimming the backlight. As a result, the display backlight power can be reduced by up to 25% with minimal visual impact depending on Intel DPST settings and system use.

Intel DPST 4.0 provides enhanced image quality over the previous version of Intel DPST.

### 9.7 FSB Dynamic Frequency Switching

See Section 3.8 for details on FSB Dynamic Frequency Switching.

### 9.8 Render Standby States

Graphics Render Standby is a technique designed to optimize the average power to the GMCH. (This technique requires a separate Graphics VRM.) GMCH will put the Graphics Render engine to Render Standby (RS) state, during times of inactivity or basic video modes. While in Render Standby state, the GMCH will place the VR into a low voltage state through VID signals. To indicate a condition where GMCH Render core is in a very low-power state, the GMCH will place the render engine into a RS-state and will change the VID code to the Render core VR to a lower voltage state.

Below is the Render Core Standby-states supported and corresponding voltages on the GMCH. The Render Core clock is gated in all the below states.

RSx	Core Voltage (V)
RS2	0.55 V



## 9.9 Render Thermal Throttling

Render Thermal Throttling of the graphics core allows for the reduction of frequency of the render core engine, thus reducing graphics power and chipset thermals. Performance is degraded, but the platform's thermal burden is relieved.

Render Thermal Throttling uses several P-states that can be used to throttle the render core. Each P-state has a frequency assigned to it. As the temperature of chipset thermal sensor exceeds the Hot-trip point, the graphics engine begins to reduce frequency, dropping to the first p-state. After a timeout, the DTS is rechecked, and if the DTS temperature is still greater than the designed hysteresis, frequency is again reduced. Render frequency will not increase in frequency unless the DTS temperature falls below the hysteresis. Once this point occurs, P-states immediately step back up to the previous highest frequency (one before trip point).



## 10 Absolute Maximum Ratings

**Table 22** specifies the GMCH's absolute maximum and minimum ratings. Within functional operation limits (specified in [Chapter 12](#) and [13](#)), functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the GMCH contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

**Table 22. Absolute Maximum Ratings (Sheet 1 of 2)**

Symbol	Parameter	Min	Max	Unit	Notes
T <sub>die</sub>	Die Temperature under Bias	0	100	°C	1
T <sub>storage</sub>	Storage Temperature	-55	150	°C	2, 3, 4
		-25	150	°C	2, 3, 5
<b>GMCH</b>					
V <sub>CC</sub>	1.05-V Core Supply Voltage with respect to V <sub>SS</sub>	-0.3	1.155	V	
V <sub>CC_AXG</sub>	1.05-V Graphics Voltage with respect to V <sub>SS</sub>	-0.3	1.155	V	
<b>M LINK</b>					
V <sub>CC</sub>	1.05-V Controller link voltage with respect to V <sub>SS</sub>	-0.3	1.115	V	
<b>Host Interface</b>					
V <sub>TT</sub> (FSB V <sub>CCP</sub> )	1.05-V AGTL+ buffer DC Input Voltage with respect to V <sub>SS</sub>	-0.3	1.32	V	
V <sub>CC_AXF</sub>	1.05-V DC Input Voltage for AGTL+ buffer logic with respect to V <sub>SS</sub>	-0.3	1.155	V	
<b>DDR2 (667-MTs/800-MTs) / DDR3 (800-MTs/1066-MTs) Interfaces</b>					
V <sub>CC_SM</sub>	1.5/1.8-V DDR3/DDR2 Supply Voltage with Respect to V <sub>SS</sub> .	-0.3	2.1	V	
V <sub>CC_SM_CK</sub>	1.5/1.8-V DDR3/DDR2 Clock IO Voltage with Respect to V <sub>SS</sub> .	-0.3	2.1	V	
V <sub>CCA_SM</sub>	1.05-V DDR3/DDR2 Voltage connects to IO logic and DLLs with Respect to V <sub>SS</sub> .	-0.3	1.155	V	6



Table 22. Absolute Maximum Ratings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes
V <sub>CCA_SM_CK</sub>	1.05-V DDR2/DDR3 Voltage for clock module to avoid noise with Respect to V <sub>SS</sub> .	-0.3	1.155	V	6
<b>DMI /PCI Express Graphics/SDVO Interface/HDMI /DP</b>					
Symbol	Parameter	Min	Max	Unit	Notes
V <sub>CC_PEG</sub>	1.05-V PCI-Express Supply Voltage with respect to V <sub>SS</sub>	-0.3	1.155	V	
V <sub>CC_DMI</sub>	1.05-V DMI Terminal Supply Voltage with respect to V <sub>SS</sub>	-0.3	1.155	V	
V <sub>CCA_PEG_BG</sub>	3.3-V Analog Band Gap Voltage with respect to V <sub>SSA_PEG_BG</sub>	-0.3	3.63	V	
V <sub>CCA_PEG_PLL</sub>	Analog PLL Voltage for PCI Express-Based Graphics	-0.3	1.155	V	
V <sub>CCD_PEG_PLL</sub>	Digital PLL Voltage for PCI Express-Based Graphics	-0.3	1.155	V	
<b>CRT DAC Interface (8 bit DAC)</b>					
V <sub>CCA_CRT_DAC</sub>	3.3-V DAC IO Supply Voltage	-0.3	3.63	V	
V <sub>CCD_QDAC</sub>	1.5-V CRT Quiet Digital Voltage	-0.3	1.65	V	
<b>HV CMOS Interface</b>					
V <sub>CC_HV</sub>	3.3-V Supply Voltage with respect to V <sub>SS</sub>	-0.3	3.63	V	
<b>TV OUT Interface (10 bit DAC)</b>					
V <sub>CCD_TVDAC</sub>	1.5-V TV Supply	-0.3	1.65	V	
V <sub>CCA_TV_DAC</sub>	3.3-V TV Analog Supply	-0.3	3.63	V	
V <sub>CCA_DAC_BG</sub>	3.3-V TV DAC Band Gap voltage	-0.3	3.63	V	
V <sub>CCD_QDAC</sub>	1.5-V Quiet Supply	-0.3	1.65	V	
<b>LVDS Interface</b>					
V <sub>CCD_LVDS</sub>	1.8-V LVDS Digital Power Supply	-0.3	1.98	V	
V <sub>CC_TX_LVDS</sub>	1.8-V LVDS Data/Clock Transmitter Supply Voltage with respect to V <sub>SS</sub>	-0.3	1.98	V	
V <sub>CCA_LVDS</sub>	1.8-V LVDS Analog Supply voltage with respect to V <sub>SS</sub>	-0.3	1.98	V	
<b>PLL Analog Power Supplies</b>					
V <sub>CCA_HPLL</sub> V <sub>CCD_HPLL</sub> V <sub>CCA_MPLL</sub> V <sub>CCA_DPLLA</sub> V <sub>CCA_DPLLB</sub>	1.05-V Power Supply for various PLL	-0.3	1.155	V	
<b>Intel® High Definition Audio</b>					
V <sub>CC_HDA</sub>	1.5 V	-0.3	1.65	V	

**NOTES:** See next page.

1. Functionality is not guaranteed for parts that exceed Tdie temperature above 100 °C. Tdie is measured using the integrated digital thermal sensor (DTS). Performance may be affected if the on-die thermal sensor is enabled and the die temperature spec is exceeded.
2. Possible damage to the GMCH may occur if the GMCH storage temperature exceeds 150 °C. Intel does not guarantee functionality for parts that have exceeded temperatures above 150 °C due to spec violation.
3. Storage temperature is applicable to storage conditions only. In this scenario, the device must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. This rating applies to the silicon and does not include any tray or packaging.
4. This storage temperature data is for all Mobile Intel 4 Series Express Chipset Family except Mobile Intel GS45 and GS40 Express Chipsets.
5. This storage temperature data is for the Mobile Intel GS45 and GS40 Express Chipsets.
6. These values assume that MPPLL is turned ON.

## 10.1 Power Characteristics

**Table 23. Thermal Design Power Number**

SKU	GFX/GMCH Core voltage (V)	Max GFX Core Frequency (MHz)	TDP (W)	Notes
Intel® GM45	1.05/1.05	533	12	1
Intel® GS45 (Low-power)	1.00/1.05	320	7	1,2
	1.05/1.05	533 (for playback)	8	1,2
Intel® GS45 (High-Performance)	1.05/1.05	533	12	1
Intel® GL40	1.05/1.05	400	12	1
Intel® GS40	1.05/1.05	400	12	1
Intel® PM45	0/1.05	NA	7	1

**NOTES:**

1. Thermal design power (TDP) does not represent the worst case possible power of the product and is not intended for power delivery or  $I_{cc,max}$  specifications. TDP is an Intel characterized value intended to represent the maximum measured 5 second moving average power of the product while running typical application workloads and is useful for the product thermal design requirements. This characterized value is valid with the product  $T_j$  operation range and nominal  $V_{cc}$ .
2. FSB/DDR2 667 MHz/667 MHz and FSB/DDR3 800 MHz/800 MHz with no-ODT.



Table 24. Power Characteristics (Sheet 1 of 2)

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
<b>GMCH</b>							
$I_{VCC}$ (totalw/E GFX)	Core + IMEL + HSIO				3060	mA	8
$I_{VCC}$ (totalw/I GFX)	Core + IMEL + HSIO				2400	mA	8, 11
					2200	mA	8, 10
					1900	mA	8, 12
					1800	mA	8, 9
					9600	mA	1
$I_{VCC\_AXG}$	Graphics Core Supply Current				7700	mA	1, 10
					8000	mA	1, 11
					6387	mA	1, 12
					4700	mA	1, 9
<b>Host Interface</b>							
$I_{VTT}$ FSB at 1066 MHz	V <sub>TT</sub> Supply Current (1.05 V)				852	mA	
<b>DMI /PCI Express Graphics/SDVO Interface</b>							
$I_{VCC\_PEG}$	1.05 V PCI-Express Supply Current				1782	mA	1, 2, 5
$I_{VCC\_DMI}$	1.05 V DMI termination Supply current				456	mA	1
$I_{VCCA\_PEG\_BG}$	Band Gap Current				414	µA	1
<b>CRT DAC Interface (8 bit DAC)</b>							
$I_{VCCA\_CRT\_DAC}$	3.3-V DAC IO Supply Current				73	mA	1, 5
$I_{VCCD\_QDAC}$	1.5-V CRT Quiet Digital Current				500	µA	
<b>HV CMOS Interface</b>							
$I_{VCC\_HV}$	3.3-V Supply Current				105.3	mA	1
<b>TV OUT Interface (10 bit DAC)</b>							
$I_{VCCD\_TVDAC}$	1.5-V TV Supply				35	mA	1, 5
$I_{VCCA\_TV\_DAC}$	3.3-V TV Analog Supply				79	mA	1, 5
$I_{VCCA\_DAC\_BG}$	3.3-V TV Analog Supply				5	mA	1
$I_{VCCD\_QDAC}$	1.5-V Quiet Supply				500	µA	1
<b>Thermal Sensor</b>							
$I_{VCCD\_QDAC}$	1.5-V Thermal Sensor Current				1700	µA	

**Table 24. Power Characteristics (Sheet 2 of 2)**

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
<b>LVDS Interface</b>							
I <sub>VCCD_LVDS</sub>	1.8-V LVDS Digital Power Supply				30	mA	1
I <sub>VCC_TX_LVDS</sub>	1.8-V LVDS Data/Clock Transmitter Supply Voltage with respect to V <sub>SS</sub>				80	mA	1
I <sub>VCCA_LVDS</sub>	1.8-V LVDS Analog Supply voltage with respect to V <sub>SS</sub>				10	mA	1
<b>PLL Analog Power Supplies</b>							
I <sub>VCCA_HPLL</sub>	Host PLL Supply Current	V <sub>CCA_HPLL</sub>			24	mA	1
I <sub>VCCD_HPLL</sub>	HPLL Supply Current for Digital Interface	V <sub>CCD_HPLL</sub>			157.2	mA	1
I <sub>VCCA_DPLLA</sub> I <sub>VCCA_DPLLB</sub>	Display PLLA Supply Current Display PLLB Supply Current	V <sub>CCA_DPLLA</sub> V <sub>CCA_DPLLB</sub>			64.8	mA	1
I <sub>VCCA_MPLL</sub>	Memory PLL Supply Current	V <sub>CCA_MPLL</sub>			139.2	mA	1
I <sub>VCCA_PEG_PLL</sub>	Analog PLL Supply current	V <sub>CCA_PEG_PLL</sub>			50	mA	1
I <sub>VCCD_PEG_PLL</sub>	Digital PLL Supply current	V <sub>CCD_PEG_PLL</sub>			50	mA	1
<b>Intel High Definition Audio</b>							
I <sub>VCC_HDA</sub>	1.5-V Intel HD Audio Supply Current				50	mA	1

**NOTES:**

1. Estimate is only for max current coming through the chipset's supply balls.
2. Rail includes PLL current.
3. Includes worst case Leakage.
4. Calculated for highest stretch goal frequencies.
5. I<sub>CCMAX</sub> is determined on a per-interface basis, and all can not happen simultaneously.
6. I<sub>CCMAX</sub> number includes max current for all signal names listed in this table.
7. CLink power consumption is only for the Intel ME core logic.
8. Intel ME Link and DDR HSIO are on the V<sub>CC\_CORE</sub> rail.
9. This current data is for Mobile Intel GS45 Express Chipset in low-power mode.
10. This current data is for Mobile Intel GS45 Express Chipset in high-performance mode.
11. This current data is for Mobile Intel GM45 Express Chipset.
12. This current data is for Mobile Intel GL40 and GS40 Express Chipsets.



Table 25. DDR2 (667/800 MTs) Power Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I <sub>VCC_SM</sub>	DDR2 System Memory Interface (1.8 V, 667 MTs) Supply Current			2600	mA	
I <sub>VCC_SM</sub>	DDR2 System Memory Interface (1.8 V, 800 MTs) Supply Current			3000	mA	
I <sub>VCC_SM_CK</sub>	DDR2 System Memory Interface Clock Supply Current (667 MTs)			119.85	mA	
I <sub>VCC_SM_CK</sub>	DDR2 System Memory Interface Clock Supply Current (800 MTs)			124	mA	
I <sub>VCCA_SM</sub>	IO Logic and DLL Current(1.05 V, 667 MTs)			480	mA	
I <sub>VCCA_SM</sub>	IO Logic and DLL Current(1.05 V, 800 MTs)			720	mA	
I <sub>VCCA_SM_CK</sub>	Clock Logic Current (1.05 V, 667 MTs)			24	mA	
I <sub>VCCA_SM_CK</sub>	Clock Logic Current (1.05 V, 800 MTs)			26	mA	
I <sub>SUS_VCCSM</sub>	DDR2 System Memory Interface (1.8 V) Standby Supply Current			1	mA	See Note
I <sub>SMVREF</sub>	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current			50	μA	
I <sub>SUS_SMVREF</sub>	DDR2 System Memory Interface Reference Voltage (0.90 V) Standby Supply Current			200	μA	See Note
I <sub>TTRC</sub>	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current			2	mA	
I <sub>SUS_TTRC</sub>	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Standby Supply Current			2	mA	

**NOTE:** CLink power consumption is only for the Intel Management Engine core logic. Standby in Table 25 refers to system memory in Self Refresh during S3 (STR).

**Table 26.** DDR3 (800 /1066 MTs) Power Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I <sub>VCC_SM</sub>	DDR3 Supply Current (1.5 V, 1066 MTs)			4140	mA	
I <sub>VCC_SM</sub>	DDR3 Supply Current (1.5 V, 800 MTs)			3162.5	mA	
I <sub>VCC_SM_CK</sub>	DDR3 Clock Supply Current (1.5 V, 1066 MTs)			149.5	mA	
I <sub>VCC_SM_CK</sub>	DDR3 Clock Supply Current (1.5 V, 800 MTs)			143.75	mA	
I <sub>VCCA_SM</sub>	IO Logic and DLL Current (1.05 V, 1066 MTs)			747.5	mA	
I <sub>VCCA_SM</sub>	IO Logic and DLL Current (1.05 V, 800 MTs)			575	mA	
I <sub>VCCA_SM_CK</sub>	Clock Logic Current (1.05 V, 1066 MTs)			37.95	mA	
I <sub>VCCA_SM_CK</sub>	Clock Logic Current (1.05 V, 800 MTs)			28.75	mA	
I <sub>SUS_VCCSM</sub>	DDR3 System Memory Interface (1.5-V) Standby Supply Current			1	mA	See Note
I <sub>SMVREF</sub>	DDR3 System Memory Interface Reference Voltage Supply Current			50	µA	
I <sub>SUS_SMVREF</sub>	DDR3 System Memory Interface Reference Voltage Standby Supply Current			200	µA	See Note
I <sub>TTRC</sub>	DDR3 System Memory Interface Resister Compensation Voltage (1.5-V) Supply Current			2	mA	
I <sub>SUS_TTRC</sub>	DDR3 System Memory Interface Resister Compensation Voltage (1.5-V) Standby Supply Current			2	mA	

**NOTE:** Standby in [Table 4](#) refers to system memory in Self Refresh during S3(STR).

**Table 27.** V<sub>cc</sub> Auxiliary Power Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I <sub>VCC_AXF</sub>	Supply current FSB IO and HSIO			440	mA	1
				324	mA	2
				330	mA	3

#### NOTES:

1. This current data is for Mobile Intel GM45 Express Chipset and Mobile Intel GS45 Express Chipset in high-performance mode.
2. This current data is for Mobile Intel GS45 Express Chipset in low-power mode.
3. This current data is for Mobile Intel GL40 and GS40 Express Chipsets.

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# 11 Thermal Management

System level thermal management requires comprehending thermal solutions for two domains of operation:

1. Robust Thermal Solution Design: The system's thermal solution should be capable of dissipating the platform's TDP power while keeping all components below the relevant Tdie\_max under the intended usage conditions. Such conditions include ambient air temperature and available airflow inside the laptop.
2. Thermal Failsafe Protection Assistance: As a backup to the implemented thermal solution, the system design should provide a method to provide additional thermal protection for the components of concern. The failsafe assistance mechanism is to help manage components from being damaged by excessive thermal stress under situations in which the implemented thermal solution is inadequate or has failed.

The GMCH provides two internal thermal sensors, plus hooks for an external thermal sensor mechanism. These can be used for detecting the component temperature and for triggering thermal control within the GMCH. The GMCH has implemented several silicon level thermal management features that can lower both GMCH and DDR power during periods of high activity. These features can help control temperature of the GMCH and DDR and thus help prevent thermally induced component failures. These features include:

- Memory throttling triggered by memory heating
- Memory throttling triggered by GMCH heating
- THRMTRIP# support

## 11.1 Internal Thermal Sensor

The GMCH incorporates two on-die thermal sensors for thermal management.

The thermal sensors may be programmed to cause hardware throttling and/or software interrupts. Hardware throttling includes render and main memory programmable throttling thresholds. Sensor trip points may also be programmed to generate various interrupts including SCI, SMI, SERR, or an internal graphics interrupt.

### 11.1.1 Internal Thermal Sensor Operation

The internal thermal sensor reports six trip points: Aux0, Aux1, Aux2, Aux3, Hot and Catastrophic trip points in the order of increasing temperature.

#### Aux0, 1, 2, 3 Temperature Trip Points

These trip points may be set dynamically if desired and provides an interrupt to ACPI (or other software) when it is crossed in either direction. These auxiliary temperature trip points do not automatically cause any hardware throttling but may be used by software to trigger interrupts. Additionally, the Aux2 trip point supports an output pin - TSATN#. This pin can be used to notify platform logic when GMCH temperature crosses the Aux2 setting. See [Section 11.5](#) for more details.



### Hot Temperature Trip Point

This trip point is set at the temperature at which the GMCH must start throttling. It may optionally enable GMCH throttling when the temperature is exceeded. This trip point may provide an interrupt to ACPI (or other software) when it is crossed in either direction. Software could optionally set this as an *Interrupt when the temperature exceeds this level* setting.

### Catastrophic Trip Point

This trip point is set at the temperature at which the GMCH must be shut down immediately without any software support. This trip point may be programmed to generate an interrupt, enable throttling, or immediately shut down the system (via Halt, or via THERMTRIP# assertion).

Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register to select what type of interrupt is generated. Crossing a trip point is implemented as edge detection, used to trigger the interrupts. Either edge (i.e., crossing the trip point in either direction) generates the interrupt.

#### 11.1.1.1 Recommended Programming for Available Trip Points

Thermal Sensors are not located in hotspot of GMCH. Thermal Sensors may be up to 3°C lower than maximum  $T_j$  of GMCH. Trip points should be set to account for temperature offset between thermal sensors and maximum  $T_j$  hotspot and thermal sensor accuracy.

**Aux Trip Points (0, 1, 2, 3)** should be programmed for software and firmware control via interrupts.  $T_{jmax}$  is 100 °C. Intel suggests that Hot Trip Point should be set to throttle at 102 °C due to DTS trim accuracy adjustments. Intel guarantees functionality up until 102 °C. **Catastrophic Trip Point** should be set to halt operation to avoid maximum  $T_j$  of 130 °C.

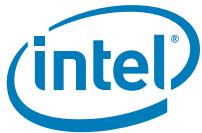
**Note:**

Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register that can be programmed to select the type of interrupt to be generated. Crossing a trip point is implemented as edge detection on each trip point to generate the interrupts.

#### 11.1.1.2 Thermal Sensor Accuracy ( $T_{accuracy}$ )

$T_{accuracy}$  for GMCH is  $\pm 5$  °C for temperature range 80 °C to 110 °C. Temperature reading accuracy from Thermal sensor will degrade further with junction temperatures below +80 °C. Temperature readings from Thermal Sensor may not be available below +40 °C. GMCH may not operate above +102 °C. This value is based on product characterization and is not guaranteed by manufacturing test.

Software has the ability to program the  $T_{cat}$ ,  $T_{hot}$ , and  $T_{aux}$  trip points, but these trip points should be selected with consideration for the thermal sensor accuracy and the quality of the platform thermal solution. Overly conservative (unnecessarily low) temperature settings may unnecessarily degrade performance due to frequent throttling, while overly aggressive (dangerously high) temperature settings may fail to protect the part against permanent thermal damage.



### 11.1.2 Hysteresis Operation

Hysteresis provides a small amount of positive feedback to the thermal sensor circuit to prevent a trip point from flipping back and forth rapidly when the temperature is right at the trip point.

The digital hysteresis offset is programmable to be 0, 1, 2...15, which corresponds to an offset in the range of approximately 0 to 7 °C.

## 11.2 Memory Thermal Throttling Options

The GMCH has two independent mechanisms that cause system memory throttling.

- GMCH Thermal Management: Ensures that the chipset is operating within thermal limits. The mechanism can be initiated by a thermal sensor (internal) trip or by virtual thermal sensor bandwidth measurement exceeding a programmed threshold via a weighted input averaging filter.
- DRAM Thermal Management: Ensures that the DRAM chips are operating within thermal limits. The GMCH can control the amount of GMCH - initiated bandwidth per rank to a programmable limit via a weighted input averaging filter.

## 11.3 External Thermal Sensor Interface Overview

The GMCH supports two inputs for external thermal sensor notifications, based on which it can regulate memory accesses.

**Note:**

The thermal sensors should be capable of measuring the ambient temperature only and should be able to assert PM\_EXT\_TS# [1:0] if the pre-programmed thermal limits/ conditions are met or exceeded.

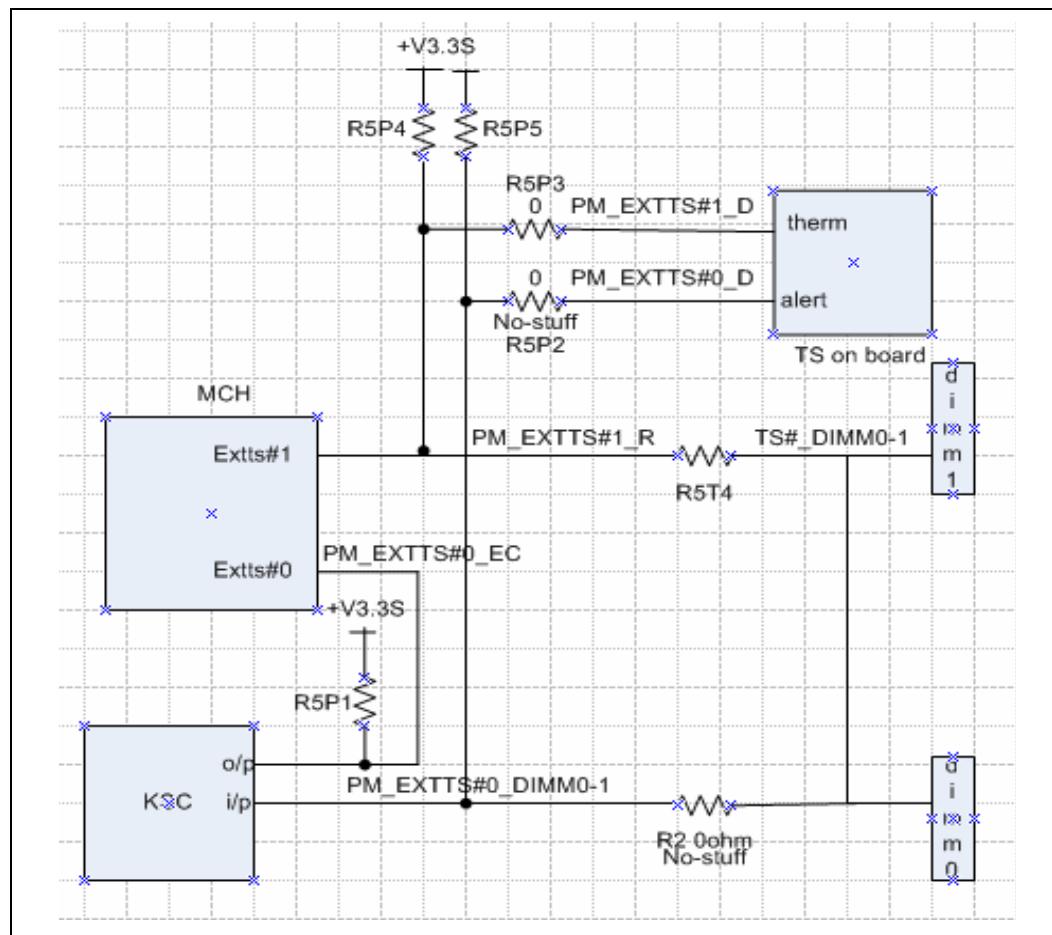
An external thermal sensor with a serial interface may be placed next to a SO-DIMM (or any other appropriate platform location), or a remote Thermal Diode may be placed next to the SO-DIMM (or any other appropriate platform location) and connected to the external Thermal Sensor.

The external sensor can be connected to the ICH via the SMBus Interface to allow programming and setup by BIOS software over the serial interface.

Additional external thermal sensor's outputs, for multiple sensors, can be wire-OR'd together allow signaling from multiple sensors that are physically located separately. Software can, if necessary, distinguish which SO-DIMM(s) is the source of the over-temp through the serial interface. However, since the SO-DIMM's is located on the same Memory Bus Data lines, any GMCH-based Read throttle will apply equally.

Thermal sensor can either directly routing to the GMCH pins or indirectly routing to GMCH by invoking an Embedded Controller (EC) or KSC connected in between the thermal sensor and GMCH pins. Both routing methods are applicable for both thermal sensors placed on the motherboard (TS on board) and/or thermal sensors located on the memory modules (TS-on-DIMM).

**Figure 19. Platform External Sensor**



## 11.4 THERMTRIP# Operation

Assertion of the GMCH's THERMTRIP# (Thermal Trip) indicates that its junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the GMCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the core junction temperature. Once activated, THERMTRIP# remains latched until RSTIN# is asserted.

## 11.5 TSATN# Operation

TSATN# is an AGTL+ output pin of the GMCH which indicates when the AUX2 temperature trip point of the internal thermal sensor has been crossed. This may be connected to platform logic (a level-shifter may be required), optionally. This input can then trigger the GMCH fan to a higher setting to increase GMCH cooling.

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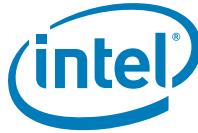
## 12 DC Characteristics

The following notations are used to describe the signal types

Notations	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description includes the type of buffer used for the particular signal

Signal	Description
AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The GMCH integrates AGTL+ termination resistors, and supports $V_{TT} = 1.05$ V.
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express 1.0. Signaling Environment AC Specifications. The buffers are not 3.3-V tolerant. Refer to the PCIE specification.
CMOS	CMOS buffers. 1.5-V tolerant.
HVCmos	High-voltage CMOS buffers. 3.3-V tolerant.
LVCMOS	Low-voltage CMOS buffers. $V_{TT}$ tolerant
COD	CMOS Open Drain buffers. 3.3-V tolerant
SSTL-1.8	Stub Series Termination Logic: These are 1.8-V capable buffers.
SSTL-1.5	Stub Series Termination Logic: These are 1.5-V capable buffers.
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
LVDS	Low-voltage Differential signal interface
Ref	Voltage reference signal

**Table 28. Signal Groups (Sheet 1 of 4)**

Signal Group	Signal Type	Signals	Notes
<b>Host Interface Signal Groups</b>			
(a)	I/O AGTL+	H_ADS#, H_BNR#, H_BREQ#, H_DBSY#, H_DRDY#, H_DINV# [3:0], H_A# [35:3], H_ADSTB# [1:0], H_D# [63:0], H_DSTBP# [3:0], H_DPWR#, H_DSTBN# [3:0], H_HIT#, H_HITM#, H_REQ# [4:0], H_DINV# [3:0],	
(b)	O AGTL+	H_BPRI#, H_CPURST#, H_DEFER#, H_TRDY#, H_RS# [2:0], THERMTRIP#,	
(c)	O LVCMOS	H_CPUSLP#	
(d)	I AGTL+	H_LOCK#	
(e)	I A	H_AVREF, H_DVREF, H_SWING	
(f)	I/O A	H_RCOMP	
<b>Serial DVO/PCI-Express* Graphics/iHDMI/DP Interface Signal Groups</b>			
(g)	I PCI Express	<b>PCI-E GFX Interface:</b> PEG_RX [15:0], PEG_RX# [15:0] <b>SDVO Interface:</b> SDVO_TVCLKIN#, SDVO_TVCLKIN, SDVOB_INT, SDVOB_INT#, SDVOC_INT, SDVOC_INT#, SDVO_FLDSTALL#, SDVO_FLDSTALL <b>iHDMI:</b> TMDSB_HPD#, TMDSC_HDP# <b>DP Interface:</b> DPB_HPD#, DPB_AUX, DPB_AUX#, DPC_HPD#, DPC_AUX, DPC_AUX#, DPD_HPD#, DPD_AUX, DPD_AUX#	See <a href="#">Section 6.2</a> for SDVO/DP/HDMI & PCI Express GFX Pin Mapping
(h)	O PCI Express	<b>PCI Express GFX Interface:</b> PEG_TX [15:0], PEG_TX# [15:0] <b>SDVO Interface:</b> SDVOB_RED#, SDVOB_RED, SDVOB_GREEN#, SDVOB_GREEN, SDVOB_BLUE#, SDVOB_BLUE, SDVOB_CLK, SDVOB_CLK#, SDVOC_RED#, SDVOC_RED, SDVOC_GREEN#, SDVOC_GREEN, SDVOC_BLUE#, SDVOC_BLUE, SDVOC_CLK, SDVOC_CLK# <b>iHDMI:</b> TMDS_B_CLK, TMDS_B_CLK#, TMDS_B_DATA0, TMDS_B_DATA0#, TMDS_B_DATA1, TMDS_B_DATA1#, TMDS_B_DATA2, TMDC_B_DATA2#, TMDS_C_CLK, TMDS_C_CLK#, TMDS_C_DATA0, TMDS_C_DATA0#, TMDS_C_DATA1, TMDS_C_DATA1#, TMDS_C_DATA2, TMDS_C_DATA2# <b>DP Interface:</b> DPB_LANE3, DPB_LANE3#, DPB_LANE2, DPB_LANE2#, DPB_LANE1, DPB_LANE1#, DPB_LANE0, DPB_LANE0#, DPC_LANE3, DPC_LANE3#, DPC_LANE2, DPC_LANE2#, DPC_LANE1, DPC_LANE1#, DPC_LANE0, DPC_LANE0#, DPD_LANE3, DPD_LANE3#, DPD_LANE2, DPD_LANE2#, DPD_LANE1, DPD_LANE1#, DPD_LANE0, DPD_LANE0#	See <a href="#">Section 6.2</a> for SDVO/DP/HDMI & PCI Express GFX Pins Mapping



Table 28. Signal Groups (Sheet 2 of 4)

Signal Group	Signal Type	Signals	Notes
(i)	I COD	<b>iHDMI:</b> SDVO_CTRLCLK, SDVO_CTRLDATA, DDPC_CTRLCLK, DDPC_CTRLDATA	
(j)	I A	PEG_COMPO PEG_COMPI	Analog PCI Express GFX/ SDVO I/F Compensation Signals
<b>DDR Interface Signal Groups</b>			
(k)	I/O SSTL-1.8/1.5	SA_DQ [63:0], SB_DQ [63:0] SA_DQS [7:0], SB_DQS [7:0], SA_DQS# [7:0], SB_DQS# [7:0]	
(l)	O SSTL-1.8/1.5	SA_DM [7:0], SB_DM [7:0], SA_MA [14:0], SB_MA [14:0], SA_BS [2:0], SB_BS [2:0], SA_RAS#, SB_RAS#, SA_CAS#, SB_CAS#, SA_WE#, SB_WE#, SA_CK# [1:0], SA_CK [1:0], SA_CKE [1:0], SA_CS# [1:0], SA_ODT [1:0], SB_CK [1:0], SB_CK# [1:0], SB_CKE [1:0], SB_CS# [1:0], SB_ODT [1:0]	
(m)	I CMOS	SM_PWROK	
(n)	I/O A	SM_REXT	
(o)	I A	SM_RCOMP, SM_RCOMP#, SM_VREF, SM_RCOMP_VOL, SM_RCOMP_VOH	
<b>LVDS Signal Groups</b>			
(p)	O LVDS	LVDSA_DATA [3:0], LVDSA_DATA# [3:0], LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0], LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#	
(q)	I/O Ref	LVDS_IBG	
(r)	I Ref	LVDS_VREFH, LVDS_VREFL	Must be connected to Ground
(s)	O HVCMOS	L_BKLT_CTRL, L_BKLT_EN, L_VDD_EN	
(t)	O A	LVDS_VBG	Leave as NC
<b>CRT DAC Signal Groups</b>			
(u)	O A	CRT_RED, CRT_GREEN, CRT_BLUE, CRT_IRTN, CRT_TVO_IREF	Refer to CRT/ Analog VESA spec
(v)	O HVCMOS	CRT_HSYNC, CRT_VSYNC	Refer to CRT/ Analog VESA spec

**Table 28. Signal Groups (Sheet 3 of 4)**

Signal Group	Signal Type	Signals	Notes
<b>TV DAC Signal Groups</b>			
(w)	O A	TVA_DAC, TVB_DAC, TVC_DAC, TV_RTN	
(x)	O COD	TV_DCONSEL [1:0]	
<b>Clocks, Reset, and Miscellaneous Signal Groups</b>			
(y)	O HVCMOS	ICH_SYNC#, GFX_VID [4:0], GFX_VR_EN	
(z)	I Diff Clk	DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#, HPLL_CLK, HPLL_CLK#, PEG_CLK, PEG_CLK#	PLL Signals
(aa)	O AGTL+	TSATN#	
(ab)	I LVCMOS	PM_DPRSTP#	
(ac)	I HVCMOS	PM_EXT_TS [1:0]#, DPRSLPVR, PM_SYNC#	
(ad)	I HVCMOS	RSTIN#, PWROK, CL_PWROK	
(ae)	O SSTL-1.5	SM_DRAMRST#	
<b>I/O Buffer Supply Voltages</b>			
(af)	AGTL+ Termination Voltage	VTT (Vccp)	
(ag)	SDVO, HDMI, DP, PCI Express GFX Voltages	VCC_DMI, VCCA_PEG_BG, VSSA_PEG_BG, VCCD_PEG_PLL, VCCA_PEG_PLL	
(ah)	1.8-V DDR2/ 1.5-V DDR3 Supply Voltage	VCC_SM, VCC_SM_CK, VCCA_SM, VCCA_SM_CK	
(ai)	GMCH Core	VCC, VCC_AXG, VCC_AXF, VCC_AXG_SENSE	
(aj)	HV Supply Voltage	VCC_HV	
(ak)	TV DAC Supply Voltage	VCCD_TVDAC, VCCA_TV_DAC, VCCD_QDAC,	
(al)	TV DAC Band Gap and Channel Supply	VCCA_DAC_BG, VSSA_DAC_BG	
(am)	CRT DAC Supply Voltage	VCCA_CRT_DAC, VCCD_QDAC	
(an)	PLL Supply Voltages	VCCA_HPLL, VCCA_MPLL, VCCD_HPLL, VCCA_DPLLA, VCCA_DPLLB	
(ao)	1.8-V LVDS Digital Supply	VCCD_LVDS, VCC_TX_LVDS, VCCA_LVDS	

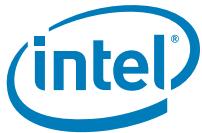


Table 28. Signal Groups (Sheet 4 of 4)

Signal Group	Signal Type	Signals	Notes
(ap)	1.5-V Intel HD Audio Power Supply	VCC_HDA	
<b>Intel® Management Engine Interface</b>			
(aq)	I/O GTL	CL_DATA, CL_CLK	
(ar)	I GTL	CL_RST#	
(as)	I A	CL_VREF	
<b>Intel® High Definition Audio (Intel HD Audio)</b>			
(at)	I CMOS	HDA_BCLK, HDA_SYNC, HDA_SDO, HDA_RST#	
(au)	I/O CMOS	HDA_SDI	
<b>GMCH ICH Serial Interface</b>			
(av)	I PCIE	DMI_RXP [3:0], DMI_RXN [3:0]	
(aw)	O PCIE	DMI_TXP [3:0], DMI_TXN [3:0]	
<b>Display Data Channel (DDC) and GMBUS Support</b>			
(ax)	I/O COD	CRT_DDC_CLK, CRT_DDC_DATA, L_CTRL_CLK, L_CTRL_DATA, L_DDC_CLK, L_DDC_DATA, SDVO_CTRLCLK, SDVO_CTRLDATA, DDPC_CTRLCLK, DDPC_CTRLDATA	

## 12.1 I/O Buffer Supply Voltages

The I/O buffer supply voltage is measured at the GMCH package pins. The tolerances shown in Table 29 are inclusive of all noise from DC up to 20 MHz. In the lab, the voltage rails should be measured with a bandwidth limited oscilloscope with a roll off of 3 dB/decade above 20 MHz under all operating conditions. Table 29 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail.

For voltages that are connected to a filter, they should be measured at the input of the filter. If the recommended platform decoupling guidelines cannot be met, the system designer will have to make tradeoffs between the voltage regulator output DC tolerance and the decoupling performance of the capacitor network to stay within the voltage tolerances listed below.



## 12.2 General DC Characteristics

**Table 29. DC Characteristics (Sheet 1 of 6)**

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
<b>I/O Buffer Supply Voltage</b>							
V <sub>TT</sub>	(af)	1.05-V Host AGTL+ Termination Voltage	0.9975	1.05	1.1025	V	
V <sub>CC_AXF</sub>	(ai)	1.05-V DC Input Voltage for IO	0.9975	1.05	1.1025	V	
V <sub>CC</sub>	(ai)	1.05-V GMCH Core Supply Voltage	0.9975	1.05	1.1025	V	
V <sub>CC_AXG</sub>	(ai)	1.05-V Graphics Voltage	0.9975	1.05	1.1025	V	
V <sub>CC_SM</sub>	(ah)	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	
V <sub>CC_SM</sub>	(ah)	DDR3 I/O Supply Voltage		1.5		V	
V <sub>CC_SM_CK</sub>	(ah)	1.8-V DDR2 Clock IO Voltage	1.7	1.8	1.9	V	1
V <sub>CC_SM_CK</sub>	(ah)	1.5-V DDR3 Clock IO Voltage	1.425	1.5	1.575	V	
V <sub>CCA_SM</sub>	(ah)	1.05-V DDR2 Voltage Connects to IO Logic and DLLs	0.9975	1.05	1.1025	V	
<b>I/O Buffer Supply Voltage</b>							
V <sub>CCA_SM_CK</sub>	(ah)	1.05-V DDR2 Voltage for Clock Module to Avoid Noise	0.9975	1.05	1.1025	V	
V <sub>CC_PEG</sub>	(ag)	1.05-V PCI Express Supply Voltage	0.9975	1.05	1.1025	V	
V <sub>CC_DMI</sub>	(ag)	1.05-V DMI Supply Voltage	0.9975	1.05	1.1025	V	
V <sub>CCA_PEG_BG</sub>	(ag)	Analog Band Gap Voltage	1.425	1.5	1.575	V	1
V <sub>CC_HV</sub>	(aj)	HV CMOS Supply Voltage	3.135	3.3	3.465	V	
V <sub>CCD_TVDAC</sub>	(ak)	TV DAC Supply Voltage	1.425	1.5	1.575	V	
V <sub>CCD_QDAC</sub>	(ak)	TV/CRT DAC Quiet Supply Voltage	1.425	1.5	1.575	V	1
V <sub>CCA_TV_DAC</sub> V <sub>CCA_DAC_BG</sub>	(al)	TV DAC Analog & Band Gap Supply Voltage	3.135	3.3	3.465	V	1
V <sub>CCA_CRT_DAC</sub>	(am)	CRT DAC Supply Voltage	3.135	3.3	3.465	V	1
V <sub>CCA_HPLL</sub> V <sub>CCA_MPLL</sub> V <sub>CCD_HPLL</sub> V <sub>CCA_PEG_PLL</sub> V <sub>CCD_PEG_PLL</sub> V <sub>CCA_DPLLA</sub> V <sub>CCA_DPLLB</sub>	(an)	Various PLLS Analog Supply Voltages	0.9975	1.05	1.1025	V	1



Table 29. DC Characteristics (Sheet 2 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V <sub>CCD_LVDS</sub>	(ao)	Digital LVDS Supply Voltage	1.71	1.8	1.89	V	
V <sub>CC_TX_LVDS</sub>	(ao)	Data/Clock Transmitter LVDS Supply Voltage	1.71	1.8	1.89	V	1
V <sub>CCA_LVDS</sub>	(ao)	Analog LVDS Supply Voltage	1.71	1.8	1.89	V	1
V <sub>CC_HDA</sub>	(ap)	1.5-V Intel HD Audio Power Supply	1.425	1.5	1.575	V	
<b>Reference Voltages</b>							
H_VREF	(e)	Host Address and Data Reference Voltage	2/3 x V <sub>TT</sub> - 2%	2/3 x V <sub>TT</sub>	2/3 x V <sub>TT</sub> + 2%	V	
H_SWING	(e)	Host Compensation Reference Voltage	0.3125x V <sub>TT</sub> - 2%	0.3125 x V <sub>TT</sub>	0.3125x V <sub>TT</sub> + 2%	V	
SM_VREF	(o)	DDR2/3 Reference Voltage	0.49 x V <sub>CC_SM</sub>	0.50 x V <sub>CC_SM</sub>	0.51 x V <sub>CC_SM</sub>	V	16
<b>Host Interface</b>							
V <sub>IL_H</sub>	(a, d)	Host AGTL+ Input Low-voltage	-0.10	0	(2/3 x V <sub>TT</sub> ) - 0.1	V	
V <sub>IH_H</sub>	(a, d)	Host AGTL+ Input High-voltage	(2/3 x V <sub>TT</sub> ) + 0.1	V <sub>TT</sub> (1.05)	V <sub>TT</sub> + 0.1	V	
V <sub>OL_H</sub>	(a, b, aa)	Host AGTL+ Output Low-voltage			0.3125 x V <sub>TT</sub> ) + 0.1	V	
V <sub>OH_H</sub>	(a, b, aa)	Host AGTL+ Output High-voltage	V <sub>TT</sub> - 0.1		V <sub>TT</sub>	V	
I <sub>OL_H</sub>	(a, b, aa)	Host AGTL+ Output Low Current			13.2	mA	
I <sub>LEAK_H</sub>	(a, d)	Host AGTL+ Input Leakage Current			11	µA	
C <sub>PAD</sub>	(a, d)	Host AGTL+ Input Capacitance	1.5	2.0	2.5	pF	
V <sub>OL_H</sub>	(c)	CMOS Output Low-voltage			0.1 V <sub>TT</sub>	V	I <sub>OL</sub> = 1 mA
V <sub>OH_H</sub>	(c)	CMOS Output High-voltage	0.9 V <sub>TT</sub>		V <sub>TT</sub>	V	I <sub>OH</sub> = 1 mA



Table 29. DC Characteristics (Sheet 3 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
<b>DDR2 Interface</b>							
$V_{IL(DC)}$	(k)	DDR2 Input Low-voltage			$SM\_VREF - 0.075$	V	
$V_{IH(DC)}$	(k)	DDR2 Input High-voltage	$SM\_VREF + 0.075$			V	
$V_{IL(AC)}$	(k)	DDR2 Input Low-voltage			$SM\_VREF - 0.100$	V	
$V_{IH(AC)}$	(k)	DDR2 Input High-voltage	$SM\_VREF + 0.100$			V	
$V_{OL}$	(k, l)	DDR2 Output Low-voltage			0.102	V	2
$V_{OH}$	(k, l)	DDR2 Output High-voltage	1.698			V	2
$I_{Leak}$	(k)	Input Leakage Current			$\pm 10$	$\mu A$	
$C_{I/O}$	(k, l)	DDR2 Input/Output Pin Capacitance			2.3	pF	
<b>DDR3 Interface</b>							
$V_{IL(DC)}$	(k)	DDR3 Input Low-voltage			$SM\_VREF - 0.075$	V	5
$V_{IH(DC)}$	(k)	DDR3 Input High-voltage	$SM\_VREF + 0.075$			V	5
$V_{IL(AC)}$	(k)	DDR3 Input Low-voltage			$SM\_VREF - 0.100$	V	
$V_{IH(AC)}$	(k)	DDR3 Input High-voltage	$SM\_VREF + 0.100$			V	
$V_{OL}$	(k, l)	DDR3 Output Low-voltage			0.159	V	5
$V_{OH}$	(k, l)	DDR3 Output High-voltage		1.34		V	5
$I_{Leak}$	(k)	Input Leakage Current			$\pm 10$	$\mu A$	5
$C_{I/O}$	(k, l)	DDR3 Input/Output Pin Capacitance			2.3	pF	5
<b>1.05 V PCI Express Interface (includes PCI Express GFX/SDVO/HDMI/DP)</b>							
$V_{TX-DIFF\ P-P}$	(g, h)	Differential Peak to Peak Output Voltage	0.400		0.600	V	3, 4
$V_{TX\_CM-ACP}$	(g, h)	AC Peak Common Mode Output Voltage			20	mV	3
$Z_{TX-DIFF-DC}$	(g, h)	DC Differential TX Impedance	80	100	120	$\Omega$	
$V_{RX-DIFF\ p-p}$	(g, h)	Differential Input Peak to Peak Voltage	0.175		1.2	V	3, 4
$V_{RX\_CM-ACP}$	(g, h)	AC peak Common Mode Input Voltage			150	mV	



Table 29. DC Characteristics (Sheet 4 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
<b>Clocks, Reset, and Miscellaneous Signals</b>							
V <sub>IL</sub>	(ac)	Input Low-voltage			0.8	V	
V <sub>IH</sub>	(ac)	Input High-voltage	2.0			V	
V <sub>IL</sub>	(ad)	Input Low-voltage			0.4	V	
V <sub>IH</sub>	(ad)	Input High-voltage	3.0			V	
I <sub>LEAK</sub>	(ac)	Input Leakage Current			±10	µA	
C <sub>IN</sub>	(ac)	Input Capacitance	3.0		6.0	pF	
V <sub>IL</sub>	(z)	Input Low-voltage	-0.150	0		V	6, 13, 14
V <sub>IH</sub>	(z)	Input High-voltage	0.660	0.710	1.150	V	6, 13
V <sub>CROSS</sub>	(z)	Crossing Voltage	0.300		0.550	V	7, 12, 15
ΔVCROSS(REL)		Range of Crossing Points			0.140	V	7, 12, 10
V <sub>SWING</sub>	(z)	Differential Output Swing	0.300			V	6, 11
I <sub>LEAK</sub>	(z)	Input Leakage Current	-0.5		+5	µA	6, 8
C <sub>IN</sub>	(z)	Pad Capacitance	1.0		3.0	pF	6, 9
V <sub>OL</sub>	(y)	Output Low-voltage (CMOS Outputs)			0.4	V	
V <sub>OH</sub>	(y)	Output High-voltage (CMOS Outputs)	2.8			V	
I <sub>OL</sub>	(y)	Output Low Current (CMOS Outputs)			1	mA	@V <sub>OL</sub> _ HI max
I <sub>OH</sub>	(y)	Output High Current (CMOS Outputs)	-1			mA	@V <sub>OH</sub> _HI min
V <sub>IL</sub>	(ab)	Input Low-voltage (DC)			2/3 * V <sub>TT</sub> - 0.2V	V	
V <sub>IH</sub>	(ab)	Input High-voltage (DC)	2/3 * V <sub>TT</sub> + 0.2V			V	
I <sub>LEAK</sub>	(ab)	Input Leakage Current			±10	µA	
C <sub>IN</sub>	(ab)	Input Capacitance			10	pF	
V <sub>IL</sub>	(ac)	Input Low-voltage			0.8	V	
V <sub>IH</sub>	(ac)	Input High-voltage	2.0			V	
I <sub>LEAK</sub>	(ac)	Input Leakage Current			±10	µA	
C <sub>IN</sub>	(ac)	Input Capacitance			10	pF	



Table 29. DC Characteristics (Sheet 5 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
<b>LVDS Interface: Functional Operating Range (<math>V_{CC}=1.8\text{ V} \pm 5\%</math>)</b>							
$V_{OD}$	(p)	Differential Output Voltage	250	350	450	mV	
$\Delta V_{OD}$	(p)	Change in $V_{OD}$ between Complementary Output States			50	mV	
$V_{OS}$	(p)	Offset Voltage	1.125	1.25	1.375	V	
$\Delta V_{OS}$	(p)	Change in $V_{OS}$ between Complementary Output States			50	mV	
$I_{OS}$	(p)	Output Short Circuit Current		-3.5	-10	mA	
$I_{OZ}$	(p)	Output TRI-STATE Current		$\pm 1$	$\pm 10$	$\mu\text{A}$	
<b>Intel® Management Engine Interface</b>							
$V_{IL}$	(aq, ar)	Input Low-voltage	$V_{SS}$		$CL\_VREF -80\text{ mV}$	V	
$V_{IH}$	(aq, ar)	Input High-voltage	$CL\_VREF +80\text{ mV}$		$V_{CC}$	V	
$I_{LEAK}$	(aq, ar)	Input Leakage Current			$\pm 20$	$\mu\text{A}$	
$C_{IN}$	(aq, ar)	Input Capacitance			2.0	pF	
$I_{OL}$	(aq)	Output Low Current (CMOS Outputs)			1.0	mA	$@V_{OL\_HI} \text{ max}$
$I_{OH}$	(aq)	Output High Current (CMOS Outputs)	6			mA	$@V_{OH\_HI} \text{ min}$
$V_{OL}$	(aq)	Output Low-voltage (CMOS Outputs)			0.06	V	
$V_{OH}$	(aq)	Output High-voltage (CMOS Outputs)	0.61	0.8	0.98	V	
$CL\_VREF$	(as)	Intel Management Engine (ME) reference voltage	343	350	357	mV	
<b>SDVO_CTRLDATA, SDVO_CTRLCLK</b>							
$V_{IL}$	(i)	Input Low-voltage			$0.3 \times V_{CCP}$	V	
$V_{IH}$	(i)	Input High-voltage	$0.6 \times V_{CCP}$			V	
$I_{LEAK}$	(i)	Input Leakage Current			$\pm 10$	$\mu\text{A}$	
$C_{IN}$	(i)	Input Capacitance			10.0	pF	
$V_{OL}$	(i)	Output Low-voltage			0.4 @ 3 mA	V	
<b>SM_PWROK</b>							
$V_{IL}$	(m)	Input Low-voltage			0.2	V	
$V_{IH}$	(m)	Input High-voltage	1.4			V	

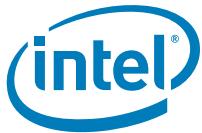


Table 29. DC Characteristics (Sheet 6 of 6)

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
<b>CRT_DDC_DATA, CRT_DDC_CLK, L_DDC_CLK, L_DDC_DATA, L_CTRL_CLK, L_CTRL_DATA, TV_DCONSEL_0, TV_DCONSEL_1, CLKREQ#</b>							
V <sub>IL</sub>		Input Low-voltage			0.3 * V <sub>CCP</sub>	V	
V <sub>IH</sub>		Input High-voltage	0.7 * V <sub>CCP</sub>			V	
I <sub>LEAK</sub>		Input Leakage Current			±150	µA	
C <sub>IN</sub>		Input Capacitance			10.0	pF	
V <sub>OL</sub>		Output Low-voltage			0.4 @ 3 mA	V	
<b>CRT_HSYNC, CRT_VSYNC</b>							
V <sub>OL</sub>		Output Low-voltage			0.5 @ 8 mA	V	
V <sub>OH</sub>		Output High-voltage	2.4 @ 8 mA			V	
<b>ICH_SYNC#, VDD_EN, BKLT_EN, BKLT_CTRL, GFX_VID [4:0], GFX_VR_EN</b>							
V <sub>IL</sub>		Input Low-voltage			0.8	V	
V <sub>IH</sub>		Input High-voltage	2.0			V	
I <sub>LEAK</sub>		Input Leakage Current			±150	µA	
C <sub>IN</sub>		Input Capacitance			10.0	pF	
V <sub>OL</sub>		Output Low-voltage (CMOS Outputs)			0.4 @ 6 mA	V	
V <sub>OH</sub>		Output High-voltage (CMOS Outputs)	V <sub>CCP</sub> -0.5 @ 2 mA			V	
<b>DPB_HPD#, DPC_HPD#, TMDS_B_HPD#, TMDS_C_HPD#</b>							
V <sub>IL</sub>		Input Low-voltage	-0.3		0.3	V	
V <sub>IH</sub>		Input High-voltage	0.6		1.155	V	
I <sub>LEAK</sub>		Input Leakage Current					
C <sub>IN</sub>		Input Capacitance					
<b>Intel® High Definition Audio</b>							
V <sub>IL_HDA</sub>	(at, au)	Input Low-voltage	—		0.2 (V <sub>CC_HDA</sub> )	V	
V <sub>IH_HDA</sub>	(at, au)	Input High-voltage	0.8 (V <sub>CC_HDA</sub> )		—	V	
V <sub>OL_HDA</sub>	(au)	Output Low-voltage	—		0.1 (V <sub>CC_HDA</sub> ) @ 1.5 mA	V	
V <sub>OH_HDA</sub>	(au)	Output High-voltage	0.9 (V <sub>CC_HDA</sub> ) @ -0.5 mA		—	V	

**NOTES:**

1. Refer to the design guidelines for filter recommendations for these rails.
2. Determined with 2x GMCH DDR2 buffer strength settings into a 50 Ω to 0.5xVCC\_SM (DDR2) test load.
3. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express specification and measured over any 250 consecutive TX UI's. Specified at the measurement point and measured over any 250 consecutive ULS. The test load shown in receiver compliance eye diagram of PCI Express specification. Should be used as the RX device when taking measurements.
4. Low-voltage PCI Express (PCI Express Graphics/SDVO) interface.



5. DDR3

Symbol	Parameter	Min	Typ	Max	Unit
R <sub>TT</sub>	Termination Resistance	50	55	61	Ω
R <sub>CN</sub>	Buffer On Resistance	22	25	28	Ω

- 6. Unless otherwise noted all specifications in this table apply to all FSB frequencies.
- 7. Crossing Voltage is defined as absolute voltage where rising edge of H<sub>PLL\_CLK</sub> is equal to the falling edge of H<sub>PLL\_CLK#</sub>.
- 8. For V<sub>IN</sub> between 0 V and VH.
- 9. CPAD includes die capacitance only. No package parasitics are included.
- 10. V<sub>CROSS</sub> is defined as the total variation of all crossing voltages as defined in Note 6.
- 11. Measurement taken from Differential Waveform.
- 12. Measurement taken from Single Ended waveform.
- 13. The max voltage including overshoot.
- 14. The min voltage including undershoot.
- 15. Only applies to the differential rising edge. (Clock rising and Clock # falling).
- 16. V<sub>CC\_SM</sub> may be 1.5-V (DDR3) or 1.8-V (DDR2).

## 12.3 CRT DAC DC Characteristics

**Table 30. CRT DAC DC Characteristics: Functional Operating Range  
(V<sub>CCA\_CRT\_DAC</sub> = 3.3 V ±5%)**

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution		8		Bits	(1)
Max Luminance (full-scale)	0.665	0.700	0.770	V	(1, 2, 4) white video level voltage
Min Luminance		0.000		V	(1, 3, 4) black video level voltage
LSB Current		73.2		µA	(4, 5)
Integral Linearity (INL)	-1.0		+1.0	LSB	(1, 6)
Differential Linearity (DNL)	-1.0		+1.0	LSB	(1, 6)
Video channel-channel voltage amplitude mismatch			6	%	(7)
Monotonicity	Guaranteed				

**NOTES:**

1. Measured at each R, G, B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude
4. Defined for a double 75-Ω termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA video signal standards.
7. Max full-scale voltage difference among R,G,B outputs (percentage of steady-state full-scale voltage).



## 12.4 TV DAC DC Characteristics

**Table 31. TV DAC DC Characteristics: Functional Operating Range  
( $V_{CCA\_TV\_DAC}$  [A,B,C]=3.3 V  $\pm$ 5%)**

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution		10		Bits	Measured at low-frequency
ENOB (Effective Number of Bits)	7.5			Bits	@ NTSC/PAL Video BW
Max Luminance (full-scale)	1.235	1.3	1.365	V	For composite video signal Note: 1,3,4
Max Luminance (full-scale)	1.045	1.1	1.155	V	For S-Video signal Note: 1,3,4
Max Luminance (full-scale)	0.665	0.7	0.735	V	For component video signal Note: 1,3,4
Min Luminance	-0.1	0	+0.1	mV	Measured at DC, Note: 2
Integral Linearity (INL)	-1		+3.5	LSB	Note: 5
Differential Linearity (DNL)	-0.5		+0.5	LSB	Note: 5
SNR	48			dB	RMS @ NTSC/PAL Video BW
Video channel-channel voltage amplitude mismatch	-3		+3	%	Note: 6
Monotonicity	Guaranteed				

**NOTES:**

1. Max steady-state amplitude.
2. Min steady-state amplitude.
3. Defined for a double 75- $\Omega$  termination.
4. Set by external reference resistor value.
5. INL and DNL measured and calculated based on the method given in VESA video signal standards.
6. Max full-scale voltage difference among the outputs (percentage of steady-state full-scale voltage).

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# 13 Clocking

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## 13.1 Overview

The GMCH has a total of four main PLLs that are used for many internal clocks. Each PLL requires one reference clock from the platform clock generator. The PLLs are:

- Host/Memory/Graphics Core PLL – Generates the main core clocks in the host clock domain. Also used to generate memory and internal graphics core clocks. Uses the Host clock (HPLL\_CLK /HPLL\_CLK#) as a reference.
- PCI Express PLL – Generates all PCI Express related clocks, including the DMI that connects to the ICH. This PLL uses the 100 MHz (PEG\_CLK/PEG\_CLK#) as a reference.
- Display PLL A – Generates the internal clocks for Display A or Display B. Uses the low-voltage 96-MHz differential clock, DPLL\_REF\_CLK/DPLL\_REF\_CLK#, as a reference.
- Display PLL B – 100-MHz differential clock, DPLL\_REF\_CLK/DPLL\_REF\_CLK#, as a reference. Also may optionally use DPLL\_REF\_SSCLK/DPLL\_REF\_SSCLK#as a reference for SSC support for LVDS display.

## 13.2 GMCH Reference Clocks

Reference Input Clocks	Input Frequency	Associated PLL
HPLL_CLK/HPLL_CLK#	166, 200, 266	Host/Memory/Graphics Core
PEG_CLK/PEG_CLK#	100 MHz	PCI Express/DMI PLL
DPLL_REF_CLK/DPLL_REF_CLK#	96 MHz	Display PLL A or B
DPLL_REF_SSCLK/DPLL_REF_SSCLK#	96 MHz (Non-SSC) 100 MHz (SSC)	Display PLL A or B



### 13.3 GMCH Host/Memory/Graphics Core Clock Frequency Support

Chipset Variant	Host Clock (MHz)	Memory Clock (MHz)	Render Clock @ Core-voltage (MHz@V)	Display Clock (MHz)
Mobile Intel GM45 Express Chipset	667/800/1066	667/800(DDR2); 667 <sup>1</sup> /800/ 1066(DDR3)	533/500 @1.05	320/333
Mobile Intel PM45 Express Chipset	667/800/1066	667/800(DDR2); 800/1066(DDR3)	NA	NA
Mobile Intel GS45 Express Chipset (Low-power)	800	667(DDR2); 667/800(DDR3)	320 @1.05 533/500 @1.05 (Turbo mode)	222/228
Mobile Intel GS45 Express Chipset (High-performance)	800/1066	667/800(DDR2); 667/800/ 1066(DDR3)	533/500 @1.05	320/333
Mobile Intel GL40 Express Chipset	800/667	800/667(DDR2) 800/667 <sup>1</sup> (DDR3)	400/380 @1.05	320/333
Mobile Intel GS40 Express Chipset	800	800/667(DDR2) 800/667(DDR3)	400 @1.05	320/333

Host Clock (MHz)	Memory Clock (MHz)	Render Clock/Display Clock (MHz)				
		Mobile Intel® GM45 Express Chipset	Mobile Intel® GS45 Express Chipset (High-performance)	Mobile Intel® GS45 Express Chipset (Low-power)	Mobile Intel® GL40 Express Chipset	Mobile Intel® GS40 Express Chipset
667	667	533/333			380/333	
800	667	500/333	500/333	333/222	400/333	400/333
800	800	533/320	533/320	320/228	400/320	400/320
1066	667	533/333	533/333			
1066	800	533/320	533/320			
1066	1066	533/320	533/320			

**Note:**

- Support for DDR3 at 667 MHz when FSB at 667 MHz only



# 14 Intel Virtualization Technology (Intel VT) for Directed I/O (Intel VT-d) Technology

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Intel Virtualization Technology (Intel VT) comprises technology components to support virtualization of platforms based on Intel architecture microprocessors. This section describes the chipset hardware components supporting IO virtualization that are architected for implementation in the GMCH.

For the GMCH, the key Intel VT-d functions are domain based isolation and virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Virtualization allows for the creation of one or more partitions on a single system. This could be multiple partitions in the same OS or there can be multiple operating system instances running on the same system offering benefits such as system consolidation, legacy migration, activity partitioning or security.

## 14.1 Intel VT-d Terminology

Term	Description
Chipset /Root-Complex	Refers to one or more hardware components that connect processor complexes to the I/O and memory subsystems. The chipset may include a variety of integrated devices.
Context	A hardware representation of state that identifies a device and the domain to which the device is assigned.
Context Cache	Remapping hardware cache that stores device to domain mappings
DMA Remapping	The act of translating the address in a DMA request to a host physical address (HPA).
Domain	A collection of physical, logical, or virtual resources that are allocated to work together. Used as a generic term for virtual machines, partitions, etc.
DVA	DMA Virtual Address: a virtual address in a DMA request. For certain virtualization usages of remapping, DVA can be the Guest Physical Address (GPA).
GAW	Guest Address Width: the DMA virtual addressability limit for a Guest partition.
GPA	Guest Physical Address: the view of physical memory from software running in a partition. GPA is used in this document as an example of DVA.
Guest	Software running within a virtual machine environment (partition).
HAW	Host Address Width: the DMA physical addressability limit for a platform.
HPA	Host Physical Address.
IEC	Interrupt Entry Cache: A translation cache in remapping hardware unit that caches frequently used interrupt-remapping table entries.



Term	Description
IOTLB	I/O Translation Lookaside Buffer: an address translation cache in remapping hardware unit that caches effective translations from DVA (GPA) to HPA.
I/OxAPIC	I/O Advanced Programmable Interrupt Controller
Interrupt Remapping	The act of translating an interrupt request before it is delivered to the CPU complex.
MGAW	Maximum Guest Address Width: the maximum DMA virtual addressability supported by a remapping hardware implementation.
MSI	Message Signalled Interrupts.
PDE Cache	Page Directory Entry cache: address translation caches in a remapping hardware unit that caches page directory entries at the various page-directory levels. Also referred to as non-leaf caches in this document.
Source ID	A 16-bit identification number to identify the source of a DMA or interrupt request. For PCI family devices this is the 'Requester ID' which consists of PCI Bus number, Device number, and Function number.
VMM	Virtual Machine Monitor: a software layer that controls virtualization. Also referred to as hypervisor in this document.

### 14.1.1 GCH/Intel VT-d Chipset Components

The GMCH supports four DMAr (DMA-remapping) engines. Three of these are contained in a central Intel VT-d block. This block also serves as the dispatcher for arbitration and forwarding the DMAr requests to memory for the Intel ME DMAr engine.

- PEG and DMI (non-HDA) DMAr Engine
  - The PEG and DMI bus hierarchies share a single remap engine, but have dedicated caching structures. The dedicated cache elements ensure that a given bus hierarchy cannot dominate a shared cache resource at the expense of the other bus.
- HDA-DMI DMAr Engine
  - Used for only the Intel HD Audio engine to provide maximum isolation for the isochronous nature of the engine.
- Intel Management Engine DMAr Engine
  - Intel Management Engine in the GMCH is implemented as a stand-alone DMAr engine, and has a dedicated interface to the Intel VT dispatcher.
- Integrated Gfx DMAr Engine
  - This DMAr engine supports a prefetch mechanism which reduces the maximum fetches from Intel VT lookup tables to 2, thus improving performance.

Translation logic is implemented within the GMCH in order to minimize latency. The DMA-remapping engines support logging of Translation Faults, and Enable/Disable of Translation (TE). Protected memory regions for secure operations are supported.

### 14.1.2 DMA Address Remapping

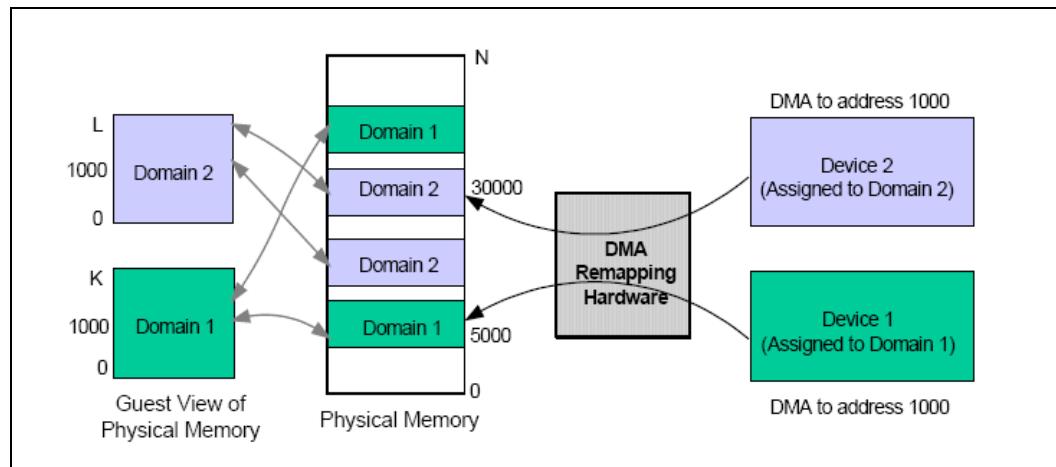
Address translation functionality for I/O device DMA requests shall be referred to as DMA remapping in this chapter.



This section describes the hardware architecture concepts of DMA remapping. The DMA-remapping architecture facilitates flexible assignment of I/O devices to multiple domains. Each domain has a view of physical address space that may be different than the host physical address space. DMA-remapping treats the address specified in DMA requests as DMA virtual addresses (DVA). DMA-remapping provides the transformation of address in a DMA request issued by an I/O device to its corresponding host-physical address (HPA).

For simplicity, the rest of the document describes the input address to the DMA-remapping hardware as GPA. [Figure 20](#) illustrates the I/O physical address translation. I/O Devices 1 and 2 are assigned to Domains 1 and 2, respectively. The software responsible for creating and managing the domains allocates system physical memory for both domains and sets up the DMA address translation function. GPA in DMA requests initiated by Devices 1 and 2 are translated to appropriate HPAs by the DMA remapping hardware.

**Figure 20. DMA Address Translation**



### 14.1.3 Capabilities of GMCH DMAr hardware

The GMCH supports the following Intel VT-d capabilities in Hardware:

- Address translation and Address protection functions are provided. This is required to support the OS robustness, virtualization and security usages.
- Multiple devices can be assigned to the same domain, and hence may share the same view of physical memory.
- Legacy and virtualization-aware guest operating systems may be run on the hardware. Direct device assignment without device driver modifications is allowed.
- DMA virtual address space sizes up to the addressing (HPA) capacity of the underlying host platform are supported.
  - The DMI non-HDA DMAr engine can support DVA's up to 48 bits.
- Allocation of physical memory to domains at a CPU page-size granularity (minimum 4 KB) is supported.
- Hardware-caching of translation structures for performance is supported.
- Remapping of translation structures at runtime under software control is supported.
- A notification mechanism to inform software about translation faults is provided. It also supports recording of translation faults (error-logging) which may be used by software to isolate faulty devices/drivers.



- To support security usages, memory protection required for secure launch, operation and tear-down of an MVMM is provided.

#### **14.1.4 Handling Interrupt Messages**

On Intel platforms, interrupt requests from IOAPICs and MSI-capable devices appear to the root-complex as upstream memory write requests to the address range 0xFEE0\_0000h to 0xFEEF\_FFFFh. Since this interrupt message address range is architectural and identical between the guest and the host, upstream DMA requests to addresses in the MSI address range are not subject to DMA-remapping.

Hardware decodes the address in DMA requests to check if it falls in the interrupt address range and bypass DMA-remapping for such transactions. DMA write requests to this range are validated and interpreted as interrupt messages, and DMA read requests to this range are treated as error.

Software must ensure that the DMA-remapping page tables are programmed to not remap regular DMA requests to the above interrupt address range. Hardware behavior is undefined for DMA requests remapped to the interrupt address range through the DMA-remapping structures.

### **14.2 Intel Trusted Execution Technology (Intel TXT)**

Intel Trusted Execution Technology is a platform initiative to address system security issues. It provides protection against software attacks or viruses, and also some level of protection against hardware attacks. The chipset will provide new features that 'fence off' DMA and other I/O from those pages the OS has marked as secure.

The GMCH leverages its Intel VT-d capabilities to isolate and secure trusted and privileged operations.

When used in conjunction with Intel VT, Intel TXT provides hardware-rooted trust for virtual applications.

The chipset protects confidential information mainly through preventing I/O DMA from accessing certain physical pages in memory. This mechanism is facilitated by the Intel VT-d table.

§



## 15 GMCH Strapping Configuration

**Table 32. GMCH Strapping Signals and Configuration**

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Others = Reserved
CFG4:3		Reserved
CFG5	DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
CFG[8:6]		Reserved
CFG9	PCIE Graphics Lane	Low = Reverse Lanes, 15->0, 14->1 etc High = Normal operation (default): Lane Numbered in Order
CFG[11:10]		Reserved
CFG12	ALLZ	Low = ALLZ mode enabled <sup>3</sup> High = Disabled (default)
CFG13	XOR	Low = XOR mode enabled <sup>3</sup> High = Disabled (default)
CFG14		Reserved
CFG15		Reserved
CFG16	FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
CFG17		Reserved
CFG18		Reserved
CFG19	DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [GMCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [GMCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE <sup>4</sup>	Low = Only digital display port (SDVO/DP/iHDMI) or PCIE is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO/iHDMI */DP Interface enabled <sup>4</sup>	Low = SDVO/iHDMI/DP interface disabled (default) High = SDVO/HDMI/DP interface enabled
L_DDC_DATA	Local Flat Panel (LFP) Present	Low = LFP Disabled (default) High = LFP Card Present; PCIe disabled
DDPC_CTRLDATA	Digital Display (iHDMI/DP) interface enabled <sup>4</sup>	Low = Digital display (iHDMI/DP) interface disabled (default) High = Digital display (iHDMI/DP) interface enabled

**NOTES:**

1. All strap signals are sampled with respect to the leading edge of the GMCH Power OK (PWROK) signal.
2. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
3. Refer to [Table 15](#) for Concurrent DP(HDMI)/PCIE configuration strap controls. §



# 16 Ballout and Package Information

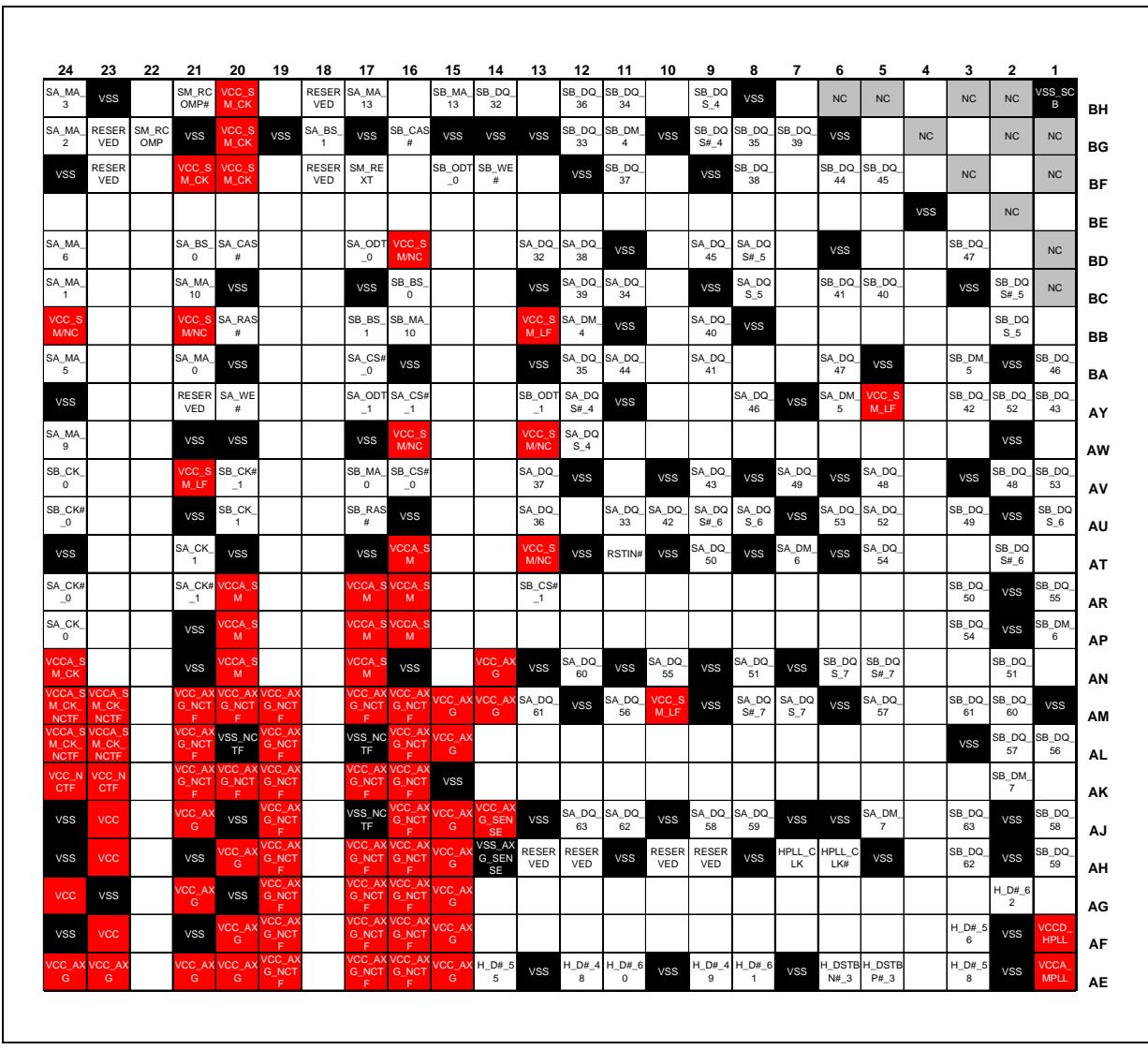
## 16.1 Mobile Intel 4 Series Express Chipset Ballout Diagrams

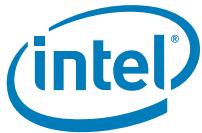
Figure 21. Ballout Diagram (Top View) Upper Left Quadrant

	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	
BH	VSS_SC_B	NC	NC		NC	NC		SB_DQ_S#_2	SB_DQ_28	VSS	SB_DQ_S#_3		SB_DQ_26	SB_DQ_31		VCC_S_M	VCC_S_M		VCC_S_M	SM_RC_OMP_VOL	SA_MA_12	VSS			
BG	NC	NC		NC		SB_DQ_18	VSS	SB_DQ_S_2	VSS	SB_DQ_29	SB_DQ_24	SB_DQ_S_3	VSS	SB_DQ_27	SB_DQ_30	VSS	VCC_S_M	VCC_S_M	VCC_S_M	VCC_S_M	VSS	SA_MA_7	SA_MA_11	SA_MA_4	
BF	NC		NC		VSS	SB_DQ_19		SB_DQ_23	SB_DQ_22		SB_DQ_25	VSS		SB_DM_3	VSS		VCC_S_M	VCC_S_M		VCC_S_M	SM_RC_OMP_VOL		VSS	SA_MA_8	
BE		NC		SB_DQ_20																					
BD	NC		VSS			SA_DQ_19		VSS	SB_DM_2	SA_DQ_S#_3	SA_DQ_25	SA_DQ_S_3	VSS			SB_MA_9	VCC_S_M			VCC_S_M	VSS			VSS	
BC	NC	SB_DQ_15	SB_DQ_16		SB_DQ_17	VSS		SB_DQ_21	SA_DQ_23		VSS	SA_DQ_S_3	SM_DR_AMRST_#			VSS	VCC_S_M			VCC_S_M	SA_CKE_0		SB_MA_2		
BB		VSS						SA_DQ_22	VSS		SA_DQ_29	VSS	SB_CKE_1			SB_BS_2	VCC_S_M			VCC_S_M	SB_MA_5			VSS	
BA	SB_DQ_10	SB_DQ_14	VSS		SA_DQ_S#_2	SA_DQ_S_2			SA_DQ_18	VSS	VCC_S_M_LF	VCC_S_M_NC				VSS	VCC_S_M			VCC_S_M	VSS			SB_MA_1	
AY	SB_DQ_11	SB_DM_1	VSS		SA_DQ_17	SA_DQ_21	VSS	SA_DM_2			SA_DQ_28	SA_DQ_24	SB_CKE_0			SB_MA_12	VCC_S_M			VCC_S_M	SA_CKE_1		SA_MA_14		
AW		VSS									VSS	SA_DQ_31				SB_MA_11	VCC_S_M			VCC_S_M	SB_MA_7			SB_MA_4	
AV	SB_DQ_S_1	SB_DQ_S#_1	VSS		VCC_S_M_LF	VSS	SM_VREF	SA_DQ_20	VSS	SA_DQ_16		SA_DQ_26	SA_DQ_30			VSS	VCC_S_M			VCC_S_M	VSS			VSS	
AU	VSS	SB_DQ_8	SB_DQ_9		SA_DQ_14	VSS	SA_DQ_15	VSS	SA_DQ_10	SA_DM_3	VSS					SB_MA_14	VCC_S_M			VCC_S_M	SB_MA_6			SB_MA_3	
AT		SB_DQ_12			SA_DQ_S_1	SA_DQ_S#_1	VSS	SA_DM_1	PWROK	VSS	SA_DQ_11	VSS	SA_DQ_27			SB_MA_8	VCC_S_M			VCC_S_M	VSS			SA_BS_2	
AR	VSS	SB_DQ_13	VSS											SM_PWORD			VSS	VCC_S_M			VCC_S_M	VSS			VSS
AP	SB_DQ_7	SB_DQ_2	SB_DQ_3														VCC_S_M	VCC_S_M			VCC_S_M	VCCA_S_M_CK			VCCA_S_M_CK
AN		VSS			SA_DQ_9	SA_DQ_8	VSS	SA_DQ_12	VSS	SA_DQ_13	SA_DQ_2	VSS	CL_PW_ROK	ME_JTAG_TDO			VCC_S_M	VCC_S_M			VSS	VCCA_S_M_CK			VCCA_S_M_CK
AM	SB_DQ_6	SB_DM_0	VSS		SA_DQ_6	VSS	SA_DQ_7	VSS	VCC_S_M_LF	VSS	SA_DQ_3	SA_DM_0	VSS	ME_JTAG_TMS	VSS	VCC	VCC_N_CTF			VCC_N_CTF	VSS_NC_CTF			VCCA_S_M_CK_NCTF	
AL	VSS	SB_DQ_S_0	SB_DQ_S#_0													ME_JTAG_G_TCK	VSS	VCC_N_CTF			VCC_N_CTF	VCC_N_CTF			VCCA_S_M_CK_NCTF
AK		SB_DQ_0														ME_JTAG_G_TDI	VCC	VCC_N_CTF			VCC_N_CTF	VCC_N_CTF			VCCA_S_M_CK_NCTF
AJ	SB_DQ_5	VSS	SB_DQ_4		SA_DQ_S_0	SA_DQ_S#_0	VSS	SA_DQ_1	SA_DQ_5	VSS	SA_DQ_0	VSS	SA_DQ_4	CL_RST_#	VSS	VCC	VCC_N_CTF			VSS_NC_CTF	VCC_N_CTF	VSS		VCC	
AH	VCC_D_MI	VCC_D_MI	SB_DQ_1		VSS	DML_TX_P_3	DML_TX_N_3	VSS	DML_RX_P_3	DML_RX_N_3	VSS	CL_CLK	CL_DAT_A	VSS	CL_VREF_F	VSS	VCC_N_CTF			VCC_N_CTF	VCC_N_CTF	VCC		VSS	
AG		VCC_D_MI														VCC	VCC	VCC_N_CTF			VCC_N_CTF	VCC_N_CTF	VSS		VCC
AF	VCC_D_MI	VSS	DML_TX_P_2													VSS	VCC	VSS_NC_CTF			VCC_N_CTF	VSS_NC_CTF	VCC		VSS
AE	DML_RX_P_2	DML_RX_N_2	DML_TX_P_1	DML_TX_N_1	VSS	DML_RX_N_0	DML_RX_P_0	VSS	DML_RX_P_1	DML_RX_N_1	VSS	DML_RX_N_0	VSS	DML_RX_N_0	VSS	VCC	VCC_N_CTF			VCC_N_CTF	VCC_N_CTF	VSS		VCC_VCC_AX_G	



Figure 22. Ballout Diagram (Top View) Upper Right Quadrant





**Figure 23. Ballout Diagram (Top View) Lower Left Quadrant**

AD	VCCA_P EG_BG	VSS	PEG_TX _15		VSS	PEG_TX #_14	PEG_TX _14	VSS	PEG_R X_15	PEG_R X#_15	VSS	PEG_R X#_13	PEG_R X_13	DMI_TX P_0													
AC	PEG_R X_14	PEG_R #_14	PEG_TX _15												VCC	VCC	VCC_N CTF	VCC_N CTF	VCC	VCC	VCC	VCC	VCC	VSS			
AB		VSS													VCC	VSS	VSS_NC TF	VCC_N CTF	VSS_NC TF	VSS	VSS	VSS	VCC_AX G	VCC_AX G			
AA	VCCA_P EG_PL	VCCD PEG_PL L	PEG_TX #_11		VSS	PEG_R X#_12	PEG_R X_12	VSS	PEG_TX #_13	PEG_TX _13	VSS	PEG_TX #_12	PEG_TX _12	VSS	VCC	VCC	VCC_N CTF	VCC_N CTF	VCC	VCC	VCC	VCC	VCC_AX G	VCC_AX G			
Y	PEG_R X#_10	VSS	PEG_TX _11		VSS	PEG_R X#_9	PEG_R X_9	VSS	PEG_TX #_10	PEG_TX _10	VSS	PEG_R X_11	PEG_R X#_11	VSS	VCC	VCC	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_AX G	VCC_AX G	VSS		
W		PEG_R X_10													VSS	VCC	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_AX G_NCT F	VCC_AX G_NCT F			
V	VCC_PE VCC_PE G	VCC_PE G	VSS												VCC	VCC	VSS_NC TF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_N CTF	VCC_AX G_NCT F	VCC_AX G_NCT F			
U	VCC_PE VCC_PE G	VCC_PE G	VSS	PEG_R X#_8	PEG_R X_8	VSS	PEG_TX #_9	PEG_TX _9	VSS	PEG_TX #_8	PEG_TX _8	VSS	VCC	VCC	VCC_N CTF	VCC_N CTF	VSS	VSS	VSS	VSS	VSS	VSS	VSS_NC TF	VSS			
T		VSS			VSS	PEG_R X#_7	PEG_R X_7	VSS	PEG_TX #_7	PEG_TX _7	VSS	PEG_C OMPI	PEG_C OMPO	VSS	RESER VED	VCC				VSS	CFG_20			CFG_0			
R	PEG_TX #_5	PEG_TX _5	VSS													RESER VED	DPRSLP VR			PM_SY NC#	CFG_19				CFG_1		
P	PEG_R X#_5	PEG_R X_5	VSS												VSS	PM_EXT _TS#_1			CFG_18	VSS				CFG_2			
N		VSS		PEG_R X#_6	PEG_R X_6	VSS	PEG_R X#_4	PEG_R X_4	VSS	PEG_TX #_6	PEG_TX _6	RESER VED			PM_EXT _TS#_0	VSS			VSS	DDPC CTRLCK				VSS			
M	PEG_TX _2	PEG_TX #_2	PEG_TX _1	VSS	PEG_TX _4	PEG_TX #_4	VSS	PEG_TX #_3	PEG_TX _3	VSS	VCCD_L VDS		RESER VED			L_CTRL _DATA	L_CTRL _CLK			L_VDD EN	DDPC CTRLRD ATA			VCCD TVDAC			
L	VCCA_DPLB	VSS	PEG_TX _1	PEG_R X#_2	PEG_R X_2	VSS	PEG_R X_3	PEG_R X#_3	VSS	VCCD_L VDS	VSS				VSS	L_BKLT _CTRL			CRT_VS YNC	VCCD ODAC			VSS				
K		VCC_TX _LVDS										LVDSB DATA#_3	CLKRE Q#			L_DDC _CLK	VSS			VSS	VSS			TVC_DA C			
J	VCCA_L VDS	VSSA_L VDS	PEG_R X#_1	PEG_R X_1	VSS	PEG_TX _0	PEG_TX #_0				VSS	LVDSB DATA#_3	SDVO CTRLD ATA	VSS		L_DDC _DATA	CRT_D DC_DA TA			CRT_H SYNC	CRT_R ED			VSS			
H	LVDSA_D DATA#_0	LVDSA_D DATA#_0	VSS	PEG_R X#_0	PEG_R X_0			VSS	LVDSA DATA#_2	LVDSA DATA#_2	VSS	LVDSB DATA#_1	SDVO CTRLRCL K	VSS		GFX_VI _EN	CRT_D DC_CLK			VSS	VSS			TVB_DA C			
G		VSS						VSS	LVDSA DATA#_1	LVDSA DATA#_1	VSS	LVDSB DATA#_2	SDVO CTRLRCL K	VSS		GFX_VI _D_2	L_BKLT _EN			CRT_IR TN	CRT_G REEN			VSS			
F	NC	VCCA DPLLA	VSS		PEG_CL K	DPLL_R EF_SSC LK#	LVDSA DATA_2	VSS			VSS	LVDSB DATA_2	SDVO CTRLRCL ATA	VSS		GFX_VI _D_3	VSS			VSS	VSS			TVA_DA C			
E	NC		LVDSA DATA#_1		PEG_CL K#	DPLL_R EF_SSC LK	VSS		LVDS_V REFL	LVDS_V REFH	VSS		LVDS_V REFL	SDVO CTRLRCL ATA	VSS		GFX_VI _D_4	TV_DC ONSEL_1			CRT_TV O_IREF	CRT_BL UE			VSS		
D		NC	LVDSA DATA_1																								
C	NC	NC	NC	LVDSA DATA_1	LVDS_J BG	VSS	LVDSA CLK#	LVDSA CLK	VSS	VSS	VSS		VCC_H V	GFX_VR _EN	VSS		TV_DC ONSEL_0	HDA_S DO	VSS		VSS	CFG_5			VSS	VSSA_D AC_BG	
B	NC	NC	NC	NC	NC	NC	LVDS_V BG	LVDSB DATA_0	VSS	LVDSA DATA_3	VSS	DPLL_R EF_CLK	LVDSB CLK#	VSS	VCC_H V	VSS	GFX_VI _D_0	GFX_VI _D_1	RESER VED	HDA_R ST#	HDA_S DI	HDA_B CLK	VSS	VSSA_D AC_BG	VCCA_CRT_D AC	VSSA_D AC_BG	
A	VSS_S C	NC	NC	NC	NC	NC	LVDSB DATA#_0	LVDSB DATA#_3	VSS	DPLL_R EF_CLK	LVDSB CLK#	VSS	VCC_H V	VSS	VCC_H V	VSS	VCC_H DA	VSS		VSS	HDA_S NC	VSS	HDA_S NC	VSSA_D AC_BG	VCCA_CRT_D AC	VSSA_D AC_BG	

Figure 24. Ballout Diagram (Top View) Lower Right Quadrant

								H_D#_3	H_D#_4	VSS	H_D#_4	VSS	H_D#_5	H_D#_4	H_D#_6	VSS	H_D#_5	VSS	VCCA_HPLL	
VCC_AX_G	VCC_AX_G	VCC_AX_G	VCC_AX_G	VSS_NC_TF	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VSS											H_D#_5	VSS	H_D#_5
VSS	VCC_AX_G	VSS	VCC_AX_G	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VSS											VTTLF		
VCC_AX_G	VCC_AX_G	VCC_AX_G	VCC_AX_G	VCC_AX_G_NCT_F	VSS_NC_TF	VCC_AX_G_NCT_F	VSS	H_D#_4	H_D#_4	VSS	H_D#_4	VSS	H_D#_5	H_D#_4	H_D#_6	VSS	H_D#_5	VSS	H_D#_5	
VCC_AX_G	VSS	VCC_AX_G	VSS	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VSS	H_D#_3	H_D#_3	VSS	H_D#_3	VSS	H_D#_3	H_D#_4	H_D#_4	VSS	H_D#_3	VSS	H_D#_3	
VCC_AX_G_NCT_F	VSS												H_D#_3							
VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VSS_NC_TF	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VSS											VTT	VTT	VTT
VSS	VSS_NC_TF	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VCC_AX_G_NCT_F	VSS_NC_TF	VCC_AX_G_NCT_F	VCC_AX_G	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	
RESER_VED		CFG_13	THERM_TRIP#		VCC_AX_G	VCC_AX_G	VCC_AX_G	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT			
VSS		VSS	CFG_14		VSS	H_A#_1												VSS	H_D#_1	H_D#_2
CFG_4		CFG_12	CFG_3		H_A#_1	H_A#_1		H_D#_2										VSS	H_D#_1	VSS
CFG_6		CFG_11	VSS		H_A#_1	VSS		VSS	H_D#_1	VSS	H_D#_3	H_D#_2	H_D#_2	VSS	H_D#_2	H_D#_2			H_D#_2	
CFG_7		VSS	CFG_15		VSS	H_A#_8		H_A#_1	H_D#_1	VSS	H_D#_1	VSS	H_D#_2	H_D#_2	H_D#_2	VSS	H_D#_3	VSS	RESER_VED	
VSS		CFG_16	H_A#_3		H_A#_2	H_A#_2		VSS	VSS		H_DSTB_N#_0	H_DSTB_P#_0	VSS	H_D#_2	H_D#_2	VSS	H_D#_1	H_D#_1	VTTLF	
VSS		H_A#_3	VSS		H_A#_1	VSS		H_A#_1	RESER_VED									VSS		
VSS		VSS	H_A#_2		H_A#_2	H_A#_1		H_A#_9	VSS	H_DPW_R#		H_DINV_#_0	VSS	H_D#_1	H_D#_1	VSS	H_D#_2	H_D#_3	H_D#_1	
TV_RTN		CFG_17	H_A#_2		VSS	H_A#_2		H_A#_6	H_ADS#	H_LOC_K#	H_HIT#		H_D#_5	VSS		H_D#_9	H_D#_6	VSS	H_D#_9	
VSS		VSS	H_A#_1		H_ADS_B#_1	VSS		VSS	H_BRE_Q#	VSS	VSS	H_D#_1						H_D#_4		
VSS		H_A#_3	VSS		H_A#_1	H_A#_5		H_REQ_#_2	H_RS#_1	H_BPRI_#	H_DRD_Y#	H_D#_2	H_D#_7	VSS		VSS	H_D#_0	NC		
VSS		CFG_8	H_A#_2		H_A#_1	VSS		VSS	H_HITM_SLP#	H_CPU_SLP#	H_DEF_E_R#	VSS	H_D#_3			H_D#_8	NC		NC	
CFG_10	CFG_9	H_A#_2	VSS		H_A#_7	VSS		H_A#_4	VSS	H_CPU_RST#	VSS	H_TRD_Y#	H_RS#_2	VSS	H_SWING		NC	VSS_SC_B		
VCCA_T_V_DAC	VSS	VCC_AX_F	VCC_AX_F	H_A#_3	H_A#_1	H_A#_3	H_A#_2	H_ADS_B#_0	H_REQ_#_0	H_REQ_#_4	H_REQ_#_3	TSATN#	H_DVRF_EF	H_DBSY_#	VSS	VSS	PM_DP_RSTP#	H_RS#_0	NC	RESER_VED
VCCA_T_V_DAC	VSS	VCC_AX_F	VSS		VSS	H_A#_2		VSS	H_A#_3	VSS	H_AVREF		H_BNR#	VTTLF			NC	NC	VSS_SC_B	

24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1



## 16.2 GMCH Signal List by Ball

Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 1 of 12)

Ball	Signal
A11	H_AVREF
A12	VSS
A14	H_A#_3
A15	VSS
A17	H_A#_24
A18	VSS
A20	VSS
A21	VCC_AXF
A23	VSS
A24	VCCA_TV_DAC
A25	VCCA_DAC_BG
A26	VCCA_CRT_DAC
A28	HDA_SYNC
A29	VSS
A3	VSS_SCB
A31	VSS
A32	VCC_HDA
A34	VSS
A35	VCC_HV
A37	LVDSB_CLK
A38	DPLL_REF_CLK#
A40	LVDSA_DATA#_3
A41	LVDSB_DATA#_0
A43	NC
A44	NC
A46	NC
A47	NC
A48	VSS_SCB
A5	NC
A6	NC
A8	VTTLF
A9	H_BNR#
AA1	VSS
AA10	VSS
AA11	H_D#_44

Ball	Signal
AR21	SA_CK#_1
AR24	SA_CK#_0
AR25	VSS
AR28	VSS
AR29	VCC_SM
AR3	SB_DQ_50
AR32	VCC_SM
AR33	VSS
AR36	SM_PWROK
AR46	VSS
AR47	SB_DQ_13
AR48	VSS
AT10	VSS
AT11	RSTIN#
AT12	VSS
AT13	VCC_SM/NC
AT16	VCCA_SM
AT17	VSS
AT2	SB_DQS#_6
AT20	VSS
AT21	SA_CK_1
AT24	VSS
AT25	SA_BS_2
AT28	VSS
AT29	VCC_SM
AT32	VCC_SM
AT33	SB_MA_8
AT36	SA_DQ_27
AT37	VSS
AT38	SA_DQ_11
AT39	VSS
AT40	PWROK
AT41	SA_DM_1
AT42	VSS
AT43	SA_DQS#_1

Ball	Signal
C48	NC
C5	H_SWING
C6	VSS
C8	H_RS#_2
C9	H_TRDY#
D2	NC
D4	H_D#_8
D45	LVDSA_DATA_1
D47	NC
E1	NC
E11	H_CPUSLP#
E12	H_HITM#
E13	VSS
E16	VSS
E17	H_A#_14
E20	H_A#_20
E21	CFG_8
E24	VSS
E25	VSS
E28	CRT_BLUE
E29	CRT_TVO_IREF
E3	H_RCOMP
E32	TV_DCONSEL_1
E33	GFX_VID_4
E36	SDVO_CTRLDATA
E37	LVDS_VREFH
E38	LVDS_VREFL
E40	VSS
E41	DPLL_REF_SSCLK
E43	PEG_CLK#
E46	LVDSA_DATA#_1
E48	NC
E6	H_D#_3
E8	VSS
E9	H_DEFER#

**Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 2 of 12)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AA12	VSS	AT44	SA_DQS_1	F1	NC
AA13	H_D#_42	AT47	SB_DQ_12	F11	H_BPRI#
AA14	VSS	AT5	SA_DQ_54	F12	H_RS#_1
AA15	VCC_AXG	AT6	VSS	F13	H_REQ#_2
AA16	VCC_AXG_NCTF	AT7	SA_DM_6	F16	H_A#_5
AA17	VSS_NCTF	AT8	VSS	F17	H_A#_16
AA19	VCC_AXG_NCTF	AT9	SA_DQ_50	F2	H_D#_0
AA2	H_D#_50	AU1	SB_DQS_6	F20	VSS
AA20	VCC_AXG	AU10	SA_DQ_42	F21	H_A#_33
AA21	VCC_AXG	AU11	SA_DQ_33	F24	VSS
AA23	VCC_AXG	AU13	SA_DQ_36	F25	TVA_DAC
AA24	VCC_AXG	AU16	VSS	F28	VSS
AA25	VCC_AXG	AU17	SB_RAS#	F29	VSS
AA26	VSS	AU2	VSS	F3	VSS
AA28	VCC	AU20	SB_CK_1	F32	VSS
AA29	VCC_NCTF	AU21	VSS	F33	GFX_VID_3
AA3	H_D#_52	AU24	SB_CK#_0	F36	VSS
AA30	VCC_NCTF	AU25	SB_MA_3	F37	LVDSB_DATA_2
AA32	VCC_NCTF	AU28	SB_MA_6	F38	VSS
AA33	VCC	AU29	VCC_SM	F40	LVDSA_DATA_2
AA34	VCC	AU3	SB_DQ_49	F41	DPLL_REF_SSCLK#
AA35	VSS	AU32	VCC_SM	F43	PEG_CLK
AA36	PEG_TX_12	AU33	SB_MA_14	F44	VSS
AA37	PEG_TX#_12	AU36	VSS	F46	VSS
AA38	VSS	AU38	VSS	F47	VCCA_DPLLA
AA39	PEG_TX_13	AU39	SA_DM_3	F48	NC
AA40	PEG_TX#_13	AU40	SA_DQ_10	F5	VSS
AA41	VSS	AU41	VSS	F6	H_D#_7
AA42	PEG_RX_12	AU42	SA_DQ_15	F8	H_D#_2
AA43	PEG_RX#_12	AU43	VSS	F9	H_DRDY#
AA44	VSS	AU44	SA_DQ_14	G11	VSS
AA46	PEG_TX#_11	AU46	SB_DQ_9	G12	H_BREQ#
AA47	VCCD_PEG_PLL	AU47	SB_DQ_8	G13	VSS
AA48	VCCA_PEG_PLL	AU48	VSS	G16	VSS
AA5	H_DSTBN#_2	AU5	SA_DQ_52	G17	H_ADSTB#_1
AA6	H_DSTBP#_2	AU6	SA_DQ_53	G2	H_D#_4
AA7	VSS	AU7	VSS	G20	H_A#_17
AA8	H_D#_40	AU8	SA_DQS_6	G21	VSS



Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 3 of 12)

Ball	Signal
AA9	H_D#_43
AB15	VCC_AXG
AB16	VCC_AXG_NCTF
AB17	VCC_AXG_NCTF
AB19	VCC_AXG_NCTF
AB2	VTTLF
AB20	VCC_AXG
AB21	VSS
AB23	VCC_AXG
AB24	VSS
AB25	VCC_AXG
AB26	VSS
AB28	VSS
AB29	VSS_NCTF
AB30	VCC_NCTF
AB32	VSS_NCTF
AB33	VSS
AB34	VCC
AB47	VSS
AC1	H_D#_57
AC15	VSS
AC16	VCC_AXG_NCTF
AC17	VCC_AXG_NCTF
AC19	VSS_NCTF
AC2	VSS
AC20	VCC_AXG
AC21	VCC_AXG
AC23	VCC_AXG
AC24	VCC_AXG
AC25	VSS
AC26	VCC
AC28	VCC
AC29	VCC_NCTF
AC3	H_D#_59
AC30	VCC_NCTF
AC32	VCC_NCTF
AC33	VCC
AC34	VCC

Ball	Signal
AU9	SA_DQS#_6
AV1	SB_DQ_53
AV10	VSS
AV12	VSS
AV13	SA_DQ_37
AV16	SB_CS#_0
AV17	SB_MA_0
AV2	SB_DQ_48
AV20	SB_CK#_1
AV21	VCC_SM_LF
AV24	SB_CK_0
AV25	VSS
AV28	VSS
AV29	VCC_SM
AV3	VSS
AV32	VCC_SM
AV33	VSS
AV36	SA_DQ_30
AV37	SA_DQ_26
AV39	SA_DQ_16
AV40	VSS
AV41	SA_DQ_20
AV42	SM_VREF
AV43	VSS
AV44	VCC_SM_LF
AV46	VSS
AV47	SB_DQS#_1
AV48	SB_DQS_1
AV5	SA_DQ_48
AV6	VSS
AV7	SA_DQ_49
AV8	VSS
AV9	SA_DQ_43
AW12	SA_DQS_4
AW13	VCC_SM/NC
AW16	VCC_SM/NC
AW17	VSS
AW2	VSS

Ball	Signal
G24	VSS
G25	VSS
G28	CRT_GREEN
G29	CRT_IRTN
G32	L_BKLT_EN
G33	GFX_VID_2
G36	SDVO_CTRLCLK
G37	LVDSB_DATA#_2
G38	LVDSB_DATA_1
G40	LVDSA_DATA#_2
G41	VSS
G47	VSS
G8	H_D#_1
G9	VSS
H1	VSS
H11	H_LOCK#
H12	H_ADS#
H13	H_A#_6
H16	H_A#_21
H17	VSS
H2	H_D#_6
H20	H_A#_29
H21	CFG_17
H24	TV_RTN
H25	TVB_DAC
H28	VSS
H29	VSS
H3	H_D#_9
H32	CRT_DDC_CLK
H33	VSS
H36	ICH_SYNC#
H37	VSS
H38	LVDSB_DATA#_1
H40	VSS
H43	PEG_RX_0
H44	PEG_RX#_0
H46	VSS
H47	LVDSA_DATA#_0

**Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 4 of 12)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AC46	PEG_TX#_15	AW20	VSS	H48	LVDSA_DATA_0
AC47	PEG_RX#_14	AW21	VSS	H5	VSS
AC48	PEG_RX_14	AW24	SA_MA_9	H6	H_D#_5
AD1	VCCA_HPLL	AW25	SB_MA_4	H9	H_HIT#
AD10	H_D#_46	AW28	SB_MA_7	J1	H_D#_12
AD11	H_D#_45	AW29	VCC_SM	J11	H_DPWR#
AD12	VSS	AW32	VCC_SM	J12	VSS
AD13	H_D#_47	AW33	SB_MA_11	J13	H_A#_9
AD14	H_D#_33	AW36	SA_DQ_31	J16	H_A#_19
AD2	VSS	AW37	VSS	J17	H_A#_28
AD3	H_D#_53	AW47	VSS	J2	H_D#_13
AD35	DMI_TXP_0	AY1	SB_DQ_43	J20	H_A#_22
AD36	PEG_RX_13	AY11	VSS	J21	VSS
AD37	PEG_RX#_13	AY12	SA_DQS#_4	J24	VSS
AD38	VSS	AY13	SB_ODT_1	J25	VSS
AD39	PEG_RX#_15	AY16	SA_CS#_1	J28	CRT_RED
AD40	PEG_RX_15	AY17	SA_ODT_1	J29	CRT_HSYNC
AD41	VSS	AY2	SB_DQ_52	J3	H_D#_22
AD42	PEG_TX_14	AY20	SA_WE#	J32	CRT_DDC_DATA
AD43	PEG_TX#_14	AY21	RESERVED	J33	L_DDC_DATA
AD44	VSS	AY24	VSS	J36	VSS
AD46	PEG_TX_15	AY25	SA_MA_14	J37	LVDSB_DATA#_3
AD47	VSS	AY28	SA_CKE_1	J38	VSS
AD48	VCCA_PEG_BG	AY29	VCC_SM	J41	PEG_TX#_0
AD5	VSS	AY3	SB_DQ_42	J42	PEG_TX_0
AD6	H_D#_63	AY32	VCC_SM	J43	VSS
AD7	H_D#_54	AY33	SB_MA_12	J44	PEG_RX_1
AD8	H_D#_51	AY36	SB_CKE_0	J46	PEG_RX#_1
AD9	VSS	AY37	SA_DQ_24	J47	VSSA_LVDS
AE1	VCCA_MPLL	AY38	SA_DQ_28	J48	VCCA_LVDS
AE10	VSS	AY41	SA_DM_2	J5	VSS
AE11	H_D#_60	AY42	VSS	J6	H_D#_15
AE12	H_D#_48	AY43	SA_DQ_21	J7	VSS
AE13	VSS	AY44	SA_DQ_17	J8	H_DINV#_0
AE14	H_D#_55	AY46	VSS	K12	RESERVED
AE15	VCC_AXG	AY47	SB_DM_1	K13	H_REQ#_1
AE16	VCC_AXG_NCTF	AY48	SB_DQ_11	K16	VSS
AE17	VCC_AXG_NCTF	AY5	VCC_SM_LF	K17	H_A#_31



Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 5 of 12)

Ball	Signal
AE19	VCC_AXG_NCTF
AE2	VSS
AE20	VCC_AXG
AE21	VCC_AXG
AE23	VCC_AXG
AE24	VCC_AXG
AE25	VCC_AXG
AE26	VCC
AE28	VSS
AE29	VCC_NCTF
AE3	H_D#_58
AE30	VCC_NCTF
AE32	VCC_NCTF
AE33	VCC
AE34	VSS
AE35	DMI_TXN_0
AE36	VSS
AE37	DMI_RXN_1
AE38	DMI_RXP_1
AE39	VSS
AE40	DMI_RXP_0
AE41	DMI_RXN_0
AE42	VSS
AE43	DMI_TXN_1
AE44	DMI_TXP_1
AE46	DMI_TXN_2
AE47	DMI_RXN_2
AE48	DMI_RXP_2
AE5	H_DSTBP#_3
AE6	H_DSTBN#_3
AE7	VSS
AE8	H_D#_61
AE9	H_D#_49
AF1	VCCD_HPLL
AF15	VCC_AXG
AF16	VCC_AXG_NCTF
AF17	VCC_AXG_NCTF
AF19	VCC_AXG_NCTF
Ball	Signal
AY6	SA_DM_5
AY7	VSS
AY8	SA_DQ_46
B10	H_DBSY#
B11	H_DVREF
B12	TSATN#
B13	H_REQ#_3
B14	H_REQ#_4
B15	H_REQ#_0
B16	H_ADSTB#_0
B17	H_A#_25
B18	H_A#_30
B19	H_A#_18
B2	RESERVED
B20	H_A#_32
B21	VCC_AXF
B22	VCC_AXF
B23	VSS
B24	VCCA_TV_DAC
B25	VSSA_DAC_BG
B26	VSS
B27	VCCA_CRT_DAC
B28	HDA_BCLK
B29	HDA_SDI
B30	HDA_RST#
B31	RESERVED
B32	GFX_VID_1
B33	GFX_VID_0
B34	VSS
B35	VCC_HV
B36	VSS
B37	LVDSB_CLK#
B38	DPLL_REF_CLK
B39	VSS
B4	NC
B40	LVDSA_DATA_3
B41	VSS
B42	LVDSB_DATA_0
Ball	Signal
K2	VSS
K20	VSS
K21	H_A#_34
K24	VSS
K25	TVC_DAC
K28	VSS
K29	VSS
K32	VSS
K33	L_DDC_CLK
K36	CLKREQ#
K37	LVDSB_DATA_3
K47	VCC_TX_LVDS
L1	VTTLF
L10	H_DSTBN#_0
L12	VSS
L13	VSS
L16	H_A#_26
L17	H_A#_23
L2	H_D#_17
L20	H_A#_35
L21	CFG_16
L24	VSS
L25	VSS
L28	VCCD_QDAC
L29	CRT_VSYNC
L3	H_DINV#_1
L32	L_BKLT_CTRL
L33	VSS
L36	VSS
L37	VCCD_LVDS
L39	VSS
L40	PEG_RX#_3
L41	PEG_RX_3
L42	VSS
L43	PEG_RX_2
L44	PEG_RX#_2
L46	PEG_TX_1
L47	VSS

**Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 6 of 12)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AF2	VSS	B43	LVDS_VBG	L48	VCCA_DPLL_B
AF20	VCC_AXG	B45	NC	L5	VSS
AF21	VSS	B47	NC	L6	H_D#_20
AF23	VCC	B48	NC	L7	H_D#_29
AF24	VSS	B6	H_RS#_0	L8	VSS
AF25	VCC	B7	PM_DPRSTP#	L9	H_DSTBP#_0
AF26	VSS	B8	VSS	M1	RESERVED
AF28	VCC	B9	VSS	M10	VSS
AF29	VSS_NCTF	BA1	SB_DQ_46	M11	H_D#_11
AF3	H_D#_56	BA11	SA_DQ_44	M13	H_A#_13
AF30	VCC_NCTF	BA12	SA_DQ_35	M16	H_A#_8
AF32	VSS_NCTF	BA13	VSS	M17	VSS
AF33	VCC	BA16	VSS	M2	VSS
AF34	VSS	BA17	SA_CS#_0	M20	CFG_15
AF46	DMI_TXP_2	BA2	VSS	M21	VSS
AF47	VSS	BA20	VSS	M24	CFG_7
AF48	VCC_DMI	BA21	SA_MA_0	M25	VCCD_TVDAC
AG15	VCC_AXG	BA24	SA_MA_5	M28	DDPC_CTRLDATA
AG16	VCC_AXG_NCTF	BA25	SB_MA_1	M29	L_VDD_EN
AG17	VCC_AXG_NCTF	BA28	VSS	M3	H_D#_31
AG19	VCC_AXG_NCTF	BA29	VCC_SM	M32	L_CTRL_CLK
AG2	H_D#_62	BA3	SB_DM_5	M33	L_CTRL_DATA
AG20	VSS	BA32	VCC_SM	M36	RESERVED
AG21	VCC_AXG	BA33	VSS	M38	VCCD_LVDS
AG23	VSS	BA36	VCC_SM/NC	M39	PEG_TX_3
AG24	VCC	BA37	VCC_SM_LF	M40	PEG_TX#_3
AG25	VCC	BA38	VSS	M41	VSS
AG26	VCC	BA40	SA_DQ_18	M42	PEG_TX#_4
AG28	VSS	BA43	SA_DQS_2	M43	PEG_TX_4
AG29	VCC_NCTF	BA44	SA_DQS#_2	M44	VSS
AG30	VCC_NCTF	BA46	VSS	M46	PEG_TX#_1
AG32	VCC_NCTF	BA47	SB_DQ_14	M47	PEG_TX#_2
AG33	VCC	BA48	SB_DQ_10	M48	PEG_TX_2
AG34	VCC	BA5	VSS	M5	H_D#_21
AG47	VCC_DMI	BA6	SA_DQ_47	M6	VSS
AH1	SB_DQ_59	BA9	SA_DQ_41	M7	H_DSTBN#_1
AH10	RESERVED	BB11	VSS	M8	H_DSTBP#_1
AH11	VSS	BB12	SA_DM_4	M9	H_D#_10



Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 7 of 12)

Ball	Signal
AH12	RESERVED
AH13	RESERVED
AH14	VSS_AXG_SENSE
AH15	VCC_AXG
AH16	VCC_AXG_NCTF
AH17	VCC_AXG_NCTF
AH19	VCC_AXG_NCTF
AH2	VSS
AH20	VCC_AXG
AH21	VSS
AH23	VCC
AH24	VSS
AH25	VCC
AH26	VSS
AH28	VCC
AH29	VCC_NCTF
AH3	SB_DQ_62
AH30	VCC_NCTF
AH32	VCC_NCTF
AH33	VSS
AH34	CL_VREF
AH35	VSS
AH36	CL_DATA
AH37	CL_CLK
AH38	VSS
AH39	DMI_RXN_3
AH40	DMI_RXP_3
AH41	VSS
AH42	DMI_TXN_3
AH43	DMI_TXP_3
AH44	VSS
AH46	SB_DQ_1
AH47	VCC_DMI
AH48	VCC_DMI
AH5	VSS
AH6	HPLL_CLK#
AH7	HPLL_CLK
AH8	VSS
BB13	VCC_SM_LF
BB16	SB_MA_10
BB17	SB_BS_1
BB2	SB_DQS_5
BB20	SA_RAS#
BB21	VCC_SM/NC
BB24	VCC_SM/NC
BB25	VSS
BB28	SB_MA_5
BB29	VCC_SM
BB32	VCC_SM
BB33	SB_BS_2
BB36	SB_CKE_1
BB37	VSS
BB38	SA_DQ_29
BB40	VSS
BB41	SA_DQ_22
BB47	VSS
BB8	VSS
BB9	SA_DQ_40
BC1	NC
BC11	SA_DQ_34
BC12	SA_DQ_39
BC13	VSS
BC16	SB_BS_0
BC17	VSS
BC2	SB_DQS#_5
BC20	VSS
BC21	SA_MA_10
BC24	SA_MA_1
BC25	SB_MA_2
BC28	SA_CKE_0
BC29	VCC_SM
BC3	VSS
BC32	VCC_SM
BC33	VSS
BC36	SM_DRAMRST#
BC37	SA_DQS_3
N10	H_D#_30
N11	VSS
N12	H_D#_14
N13	VSS
N16	VSS
N17	H_A#_12
N2	H_D#_23
N20	VSS
N21	CFG_11
N24	CFG_6
N25	VSS
N28	DDPC_CTRLCLK
N29	VSS
N32	VSS
N33	PM_EXT_TS#_0
N36	RESERVED
N37	PEG_TX_6
N38	PEG_TX#_6
N39	VSS
N40	PEG_RX_4
N41	PEG_RX#_4
N42	VSS
N43	PEG_RX_6
N44	PEG_RX#_6
N47	VSS
N5	H_D#_25
N6	H_D#_26
N7	VSS
N8	H_D#_28
N9	H_D#_19
P1	VSS
P13	H_D#_27
P16	H_A#_10
P17	H_A#_15
P2	H_D#_16
P20	CFG_3
P21	CFG_12
P24	CFG_4

**Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 8 of 12)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AH9	RESERVED	BC38	VSS	P25	CFG_2
AJ1	SB_DQ_58	BC40	SA_DQ_23	P28	VSS
AJ10	VSS	BC41	SB_DQ_21	P29	CFG_18
AJ11	SA_DQ_62	BC43	VSS	P3	VSS
AJ12	SA_DQ_63	BC44	SB_DQ_17	P32	PM_EXT_TS#_1
AJ13	VSS	BC46	SB_DQ_16	P33	VSS
AJ14	VCC_AXG_SENSE	BC47	SB_DQ_15	P36	VSS
AJ15	VCC_AXG	BC48	NC	P46	VSS
AJ16	VCC_AXG_NCTF	BC5	SB_DQ_40	P47	PEG_RX_5
AJ17	VSS_NCTF	BC6	SB_DQ_41	P48	PEG_RX#_5
AJ19	VCC_AXG_NCTF	BC8	SA_DQS_5	R1	H_D#_24
AJ2	VSS	BC9	VSS	R16	H_A#_11
AJ20	VSS	BD1	NC	R17	VSS
AJ21	VCC_AXG	BD11	VSS	R2	H_D#_18
AJ23	VCC	BD12	SA_DQ_38	R20	CFG_14
AJ24	VSS	BD13	SA_DQ_32	R21	VSS
AJ25	VSS	BD16	VCC_SM/NC	R24	VSS
AJ26	VCC	BD17	SA_ODT_0	R25	CFG_1
AJ28	VSS	BD20	SA_CAS#	R28	CFG_19
AJ29	VCC_NCTF	BD21	SA_BS_0	R29	PM_SYNC#
AJ3	SB_DQ_63	BD24	SA_MA_6	R3	VSS
AJ30	VSS_NCTF	BD25	VSS	R32	DPRSLPVR
AJ32	VCC_NCTF	BD28	VSS	R33	RESERVED
AJ33	VCC	BD29	VCC_SM	R46	VSS
AJ34	VSS	BD3	SB_DQ_47	R47	PEG_TX_5
AJ35	CL_RST#	BD32	VCC_SM	R48	PEG_TX#_5
AJ36	SA_DQ_4	BD33	SB_MA_9	T10	VTT
AJ37	VSS	BD36	VSS	T11	VTT
AJ38	SA_DQ_0	BD37	SA_DQS#_3	T12	VTT
AJ39	VSS	BD38	SA_DQ_25	T13	VTT
AJ40	SA_DQ_5	BD40	SB_DM_2	T14	VCC_AXG
AJ41	SA_DQ_1	BD41	VSS	T16	VCC_AXG
AJ42	VSS	BD43	SA_DQ_19	T17	VCC_AXG
AJ43	SA_DQS#_0	BD46	VSS	T2	VTT
AJ44	SA_DQS_0	BD48	NC	T20	THERMTRIP#
AJ46	SB_DQ_4	BD6	VSS	T21	CFG_13
AJ47	VSS	BD8	SA_DQS#_5	T24	RESERVED
AJ48	SB_DQ_5	BD9	SA_DQ_45	T25	CFG_0



Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 9 of 12)

Ball	Signal
AJ5	SA_DM_7
AJ6	VSS
AJ7	VSS
AJ8	SA_DQ_59
AJ9	SA_DQ_58
AK15	VSS
AK16	VCC_AXG_NCTF
AK17	VCC_AXG_NCTF
AK19	VCC_AXG_NCTF
AK2	SB_DM_7
AK20	VCC_AXG_NCTF
AK21	VCC_AXG_NCTF
AK23	VCC_NCTF
AK24	VCC_NCTF
AK25	VCC_NCTF
AK26	VCC_NCTF
AK28	VCC_NCTF
AK29	VCC_NCTF
AK30	VCC_NCTF
AK32	VCC_NCTF
AK33	VCC
AK34	ME_JTAG_TDI
AK47	SB_DQ_0
AL1	SB_DQ_56
AL15	VCC_AXG
AL16	VCC_AXG_NCTF
AL17	VSS_NCTF
AL19	VCC_AXG_NCTF
AL2	SB_DQ_57
AL20	VSS_NCTF
AL21	VCC_AXG_NCTF
AL23	VCCA_SM_CK_NCTF
AL24	VCCA_SM_CK_NCTF
AL25	VCCA_SM_CK_NCTF
AL26	VCC_NCTF
AL28	VCC_NCTF
AL29	VCC_NCTF
AL3	VSS

Ball	Signal
BE2	NC
BE4	VSS
BE45	SB_DQ_20
BE47	NC
BF1	NC
BF11	SB_DQ_37
BF12	VSS
BF14	SB_WE#
BF15	SB_ODT_0
BF17	SM_REXT
BF18	RESERVED
BF20	VCC_SM_CK
BF21	VCC_SM_CK
BF23	RESERVED
BF24	VSS
BF25	SA_MA_8
BF26	VSS
BF28	SM_RCOMP_VOH
BF29	VCC_SM
BF3	NC
BF31	VCC_SM
BF32	VCC_SM
BF34	VSS
BF35	SB_DM_3
BF37	VSS
BF38	SB_DQ_25
BF40	SB_DQ_22
BF41	SB_DQ_23
BF43	SB_DQ_19
BF44	VSS
BF46	NC
BF48	NC
BF5	SB_DQ_45
BF6	SB_DQ_44
BF8	SB_DQ_38
BF9	VSS
BG1	NC
BG10	VSS

Ball	Signal
T28	CFG_20
T29	VSS
T32	VCC
T33	RESERVED
T35	VSS
T36	PEG_COMPO
T37	PEG_COMPI
T38	VSS
T39	PEG_TX_7
T40	PEG_TX#_7
T41	VSS
T42	PEG_RX_7
T43	PEG_RX#_7
T44	VSS
T47	VSS
T5	VTT
T6	VTT
T7	VTT
T8	VTT
T9	VTT
U1	VTT
U10	VTT
U11	VTT
U12	VTT
U13	VTT
U14	VCC_AXG
U15	VCC_AXG
U16	VCC_AXG_NCTF
U17	VSS_NCTF
U19	VCC_AXG_NCTF
U2	VTT
U20	VCC_AXG_NCTF
U21	VCC_AXG_NCTF
U23	VSS_NCTF
U24	VSS
U25	VSS
U26	VSS_NCTF
U28	VSS

**Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 10 of 12)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AL30	VCC_NCTF	BG11	SB_DM_4	U29	VSS
AL32	VCC_NCTF	BG12	SB_DQ_33	U3	VTT
AL33	VSS	BG13	VSS	U30	VCC_NCTF
AL34	ME_JTAG_TCK	BG14	VSS	U32	VCC_NCTF
AL46	SB_DQS#_0	BG15	VSS	U33	VCC
AL47	SB_DQS_0	BG16	SB_CAS#	U34	VCC
AL48	VSS	BG17	VSS	U35	VSS
AM1	VSS	BG18	SA_BS_1	U36	PEG_TX_8
AM10	VCC_SM_LF	BG19	VSS	U37	PEG_TX#_8
AM11	SA_DQ_56	BG2	NC	U38	VSS
AM12	VSS	BG20	VCC_SM_CK	U39	PEG_TX_9
AM13	SA_DQ_61	BG21	VSS	U40	PEG_TX#_9
AM14	VCC_AXG	BG22	SM_RCOMP	U41	VSS
AM15	VCC_AXG	BG23	RESERVED	U42	PEG_RX_8
AM16	VCC_AXG_NCTF	BG24	SA_MA_2	U43	PEG_RX#_8
AM17	VCC_AXG_NCTF	BG25	SA_MA_4	U44	VSS
AM19	VCC_AXG_NCTF	BG26	SA_MA_11	U46	VCC_PEG
AM2	SB_DQ_60	BG27	SA_MA_7	U47	VCC_PEG
AM20	VCC_AXG_NCTF	BG28	VSS	U48	VCC_PEG
AM21	VCC_AXG_NCTF	BG29	VCC_SM	U5	VTT
AM23	VCCA_SM_CK_NCTF	BG30	VCC_SM	U6	VTT
AM24	VCCA_SM_CK_NCTF	BG31	VCC_SM	U7	VTT
AM25	VCCA_SM_CK_NCTF	BG32	VCC_SM	U8	VTT
AM26	VCCA_SM_CK_NCTF	BG33	VSS	U9	VTT
AM28	VCCA_SM_CK_NCTF	BG34	SB_DQ_30	V1	VTT
AM29	VSS_NCTF	BG35	SB_DQ_27	V15	VCC_AXG
AM3	SB_DQ_61	BG36	VSS	V16	VCC_AXG_NCTF
AM30	VCC_NCTF	BG37	SB_DQS_3	V17	VCC_AXG_NCTF
AM32	VCC_NCTF	BG38	SB_DQ_24	V19	VCC_AXG_NCTF
AM33	VCC	BG39	SB_DQ_29	V2	VTT
AM34	VSS	BG4	NC	V20	VSS_NCTF
AM35	ME_JTAG_TMS	BG40	VSS	V21	VCC_AXG_NCTF
AM36	VSS	BG41	SB_DQS_2	V23	VCC_AXG_NCTF
AM37	SA_DM_0	BG42	VSS	V24	VCC_AXG_NCTF
AM38	SA_DQ_3	BG43	SB_DQ_18	V25	VCC_AXG_NCTF
AM39	VSS	BG45	NC	V26	VCC_AXG_NCTF
AM40	VCC_SM_LF	BG47	NC	V28	VCC_AXG_NCTF
AM41	VSS	BG48	NC	V29	VCC_NCTF



Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 11 of 12)

Ball	Signal
AM42	SA_DO_7
AM43	VSS
AM44	SA_DO_6
AM46	VSS
AM47	SB_DM_0
AM48	SB_DQ_6
AM5	SA_DQ_57
AM6	VSS
AM7	SA_DQS_7
AM8	SA_DQS#_7
AM9	VSS
AN10	SA_DQ_55
AN11	VSS
AN12	SA_DO_60
AN13	VSS
AN14	VCC_AXG
AN16	VSS
AN17	VCCA_SM
AN2	SB_DQ_51
AN20	VCCA_SM
AN21	VSS
AN24	VCCA_SM_CK
AN25	VCCA_SM_CK
AN28	VCCA_SM_CK
AN29	VSS
AN32	VCC_SM
AN33	VCC_SM
AN35	ME_JTAG_TDO
AN36	CL_PWROK
AN37	VSS
AN38	SA_DQ_2
AN39	SA_DQ_13
AN40	VSS
AN41	SA_DQ_12
AN42	VSS
AN43	SA_DQ_8
AN44	SA_DQ_9
AN47	VSS
BG6	VSS
BG7	SB_DQ_39
BG8	SB_DQ_35
BG9	SB_DQS#_4
BH1	VSS_SCB
BH11	SB_DQ_34
BH12	SB_DQ_36
BH14	SB_DQ_32
BH15	SB_MA_13
BH17	SA_MA_13
BH18	RESERVED
BH2	NC
BH20	VCC_SM_CK
BH21	SM_RCOMP#
BH23	VSS
BH24	SA_MA_3
BH25	VSS
BH26	SA_MA_12
BH28	SM_RCOMP_VOL
BH29	VCC_SM
BH3	NC
BH31	VCC_SM
BH32	VCC_SM
BH34	SB_DQ_31
BH35	SB_DQ_26
BH37	SB_DQS#_3
BH38	VSS
BH40	SB_DQ_28
BH41	SB_DQS#_2
BH43	NC
BH44	NC
BH46	NC
BH47	NC
BH48	VSS_SCB
BH5	NC
BH6	NC
BH8	VSS
BH9	SB_DQS_4
V3	VTT
V30	VCC_NCTF
V32	VSS_NCTF
V33	VCC
V34	VCC
V46	VSS
V47	VCC_PEG
V48	VCC_PEG
W15	VSS
W16	VCC_AXG_NCTF
W17	VCC_AXG_NCTF
W19	VCC_AXG_NCTF
W2	H_D#_39
W20	VCC_AXG_NCTF
W21	VCC_AXG_NCTF
W23	VCC_AXG_NCTF
W24	VCC_AXG_NCTF
W25	VCC_AXG_NCTF
W26	VCC_AXG_NCTF
W28	VCC_AXG_NCTF
W29	VCC_NCTF
W30	VCC_NCTF
W32	VCC_NCTF
W33	VCC
W34	VSS
W47	PEG_RX_10
Y1	H_DINV#_3
Y10	H_D#_35
Y11	VSS
Y12	H_D#_36
Y13	H_DINV#_2
Y14	H_D#_37
Y15	VCC_AXG
Y16	VCC_AXG_NCTF
Y17	VCC_AXG_NCTF
Y19	VCC_AXG_NCTF
Y2	VSS
Y20	VSS



**Table 33. Mobile Intel 4 Series Express Chipset Ball List (Sheet 12 of 12)**

Ball	Signal	Ball	Signal	Ball	Signal
AN5	SB_DQS#_7	C1	VSS_SCB	Y21	VCC_AXG
AN6	SB_DQS_7	C11	VSS	Y23	VSS
AN7	VSS	C12	H_CPURST#	Y24	VCC_AXG
AN8	SA_DQ_51	C14	VSS	Y25	VSS
AN9	VSS	C15	H_A#_4	Y26	VCC_AXG
AP1	SB_DM_6	C17	VSS	Y28	VSS
AP16	VCCA_SM	C18	H_A#_7	Y29	VCC_NCTF
AP17	VCCA_SM	C20	VSS	Y3	H_D#_32
AP2	VSS	C21	H_A#_27	Y30	VCC_NCTF
AP20	VCCA_SM	C23	CFG_9	Y32	VCC_NCTF
AP21	VSS	C24	CFG_10	Y33	VCC
AP24	SA_CK_0	C25	CFG_5	Y34	VCC
AP25	VCCA_SM_CK	C26	VSS	Y35	VSS
AP28	VCCA_SM_CK	C28	VSS	Y36	PEG_RX#_11
AP29	VCC_SM	C29	HDA_SDO	Y37	PEG_RX_11
AP3	SB_DQ_54	C3	NC	Y38	VSS
AP32	VCC_SM	C31	TV_DCONSEL_0	Y39	PEG_TX_10
AP33	VCC_SM	C32	VSS	Y40	PEG_TX#_10
AP46	SB_DQ_3	C34	GFX_VR_EN	Y41	VSS
AP47	SB_DQ_2	C35	VCC_HV	Y42	PEG_RX_9
AP48	SB_DQ_7	C37	VSS	Y43	PEG_RX#_9
AR1	SB_DQ_55	C38	VSS	Y44	VSS
AR13	SB_CS#_1	C40	LVDSA_CLK	Y46	PEG_TX_11
AR16	VCCA_SM	C41	LVDSA_CLK#	Y47	VSS
AR17	VCCA_SM	C43	VSS	Y48	PEG_RX#_10
AR2	VSS	C44	LVDS_IBG	Y5	VSS
AR20	VCCA_SM	C46	NC	Y6	H_D#_34
				Y7	H_D#_38
				Y8	VSS
				Y9	H_D#_41

**NOTE:** VCC\_SM/NC Pins may be left NC in DDR2 designs for ease of routing.



## 16.3 Standard GMCH Package Information

The GMCH comes in an FCBGA package, which consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die.

**Caution:** Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

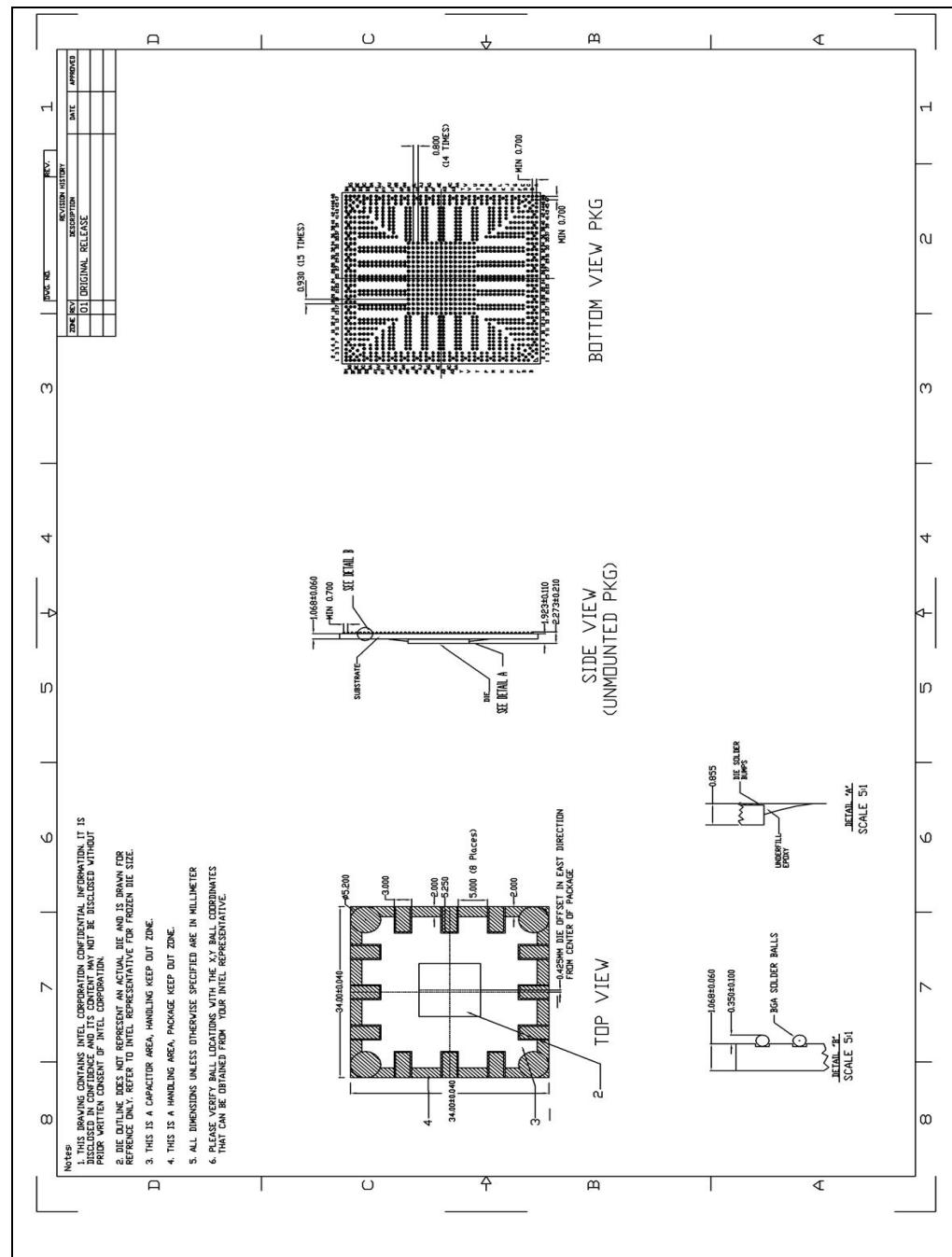
Dimensions are in millimeters. Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994.

- Tolerances:
  - X:  $\pm 0.1$
  - XX:  $\pm 0.05$
- Angles:  $\pm 1.0$  degrees
- Package parameters: 34 mm x 34 mm, 0.7-mm ball pitch
- Solder resist opening: 430 microns

Package thickness changed to  $2.273 \pm 0.210$  and ball diameter changed to  $0.350 \pm 0.100$ . These dimensions have been updated in [Figure 25](#).

**Note:** This change to mechanical specification does not impact any mechanical/ thermal/ manufacture design of the customer.

**Figure 25. Mobile Intel 4 Series Express Chipset Drawing**



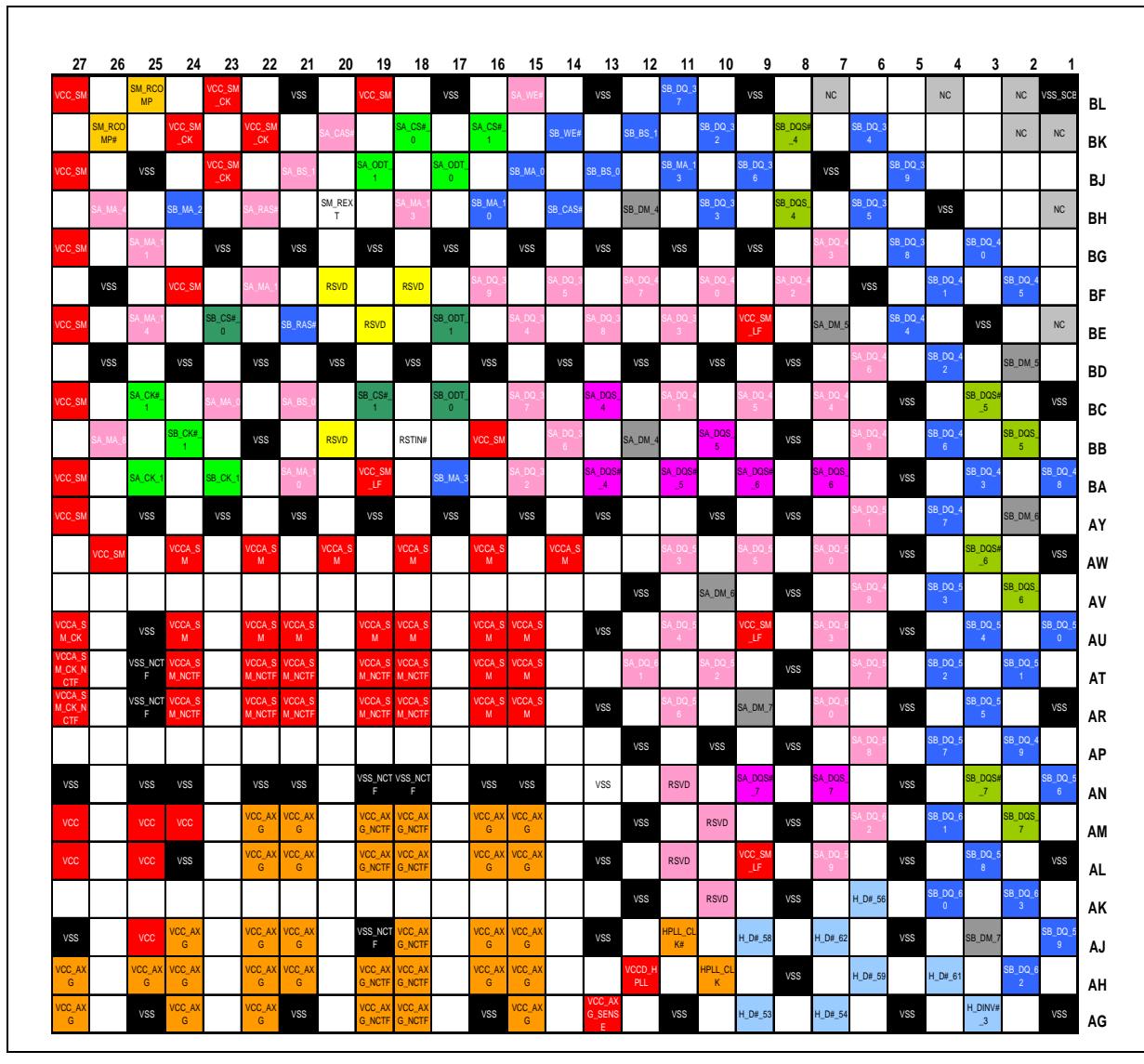
## 16.4 Intel® GS45 Express Chipset Ballout Diagrams

Figure 26. Ballout Diagram (Top View) Upper Left Quadrant

	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28
BL	VSS_SCB	NC		NC		NC		VSS	SB_DQ_2_4		VSS	SB_DQ_2_6		VSS	SB_MA_1_4		VSS		VSS		VSS		SM_RCO_MP_VOL		VCC_SM		VCC_SM	
BK	NC	NC			VSS	SB_DQ_1_9	SB_DQ_2_2	SB_DQ_2_9	SB_DQ_2_3	SB_DQ_2_5	SB_DQ_2_8	SB_DQ_2_7	SB_DQ_2_3	SB_DQ_1_1	SB_MA_1_1	SB_MA_1_2	SB_MA_1_0	SB_MA_2_1	SB_MA_2_2	SB_MA_5_1	SB_MA_5_2	SA_MA_1	SA_MA_2	SB_MA_1	SB_MA_2	SM_RCO_MP_VOL	VCC_SM	VCC_SM
BJ			SB_DQ_2_2		SB_DM_2	SB_DQ_2_3	SB_DQ_2_5	SB_DM_3			SB_DQ_2_8	SB_DQ_2_7	SB_DQ_2_3		SB_MA_5	SB_MA_1_2	SB_MA_1_1	SB_MA_5_2	SA_MA_1	SA_MA_2	SB_MA_1	SA_MA_1			VSS	VCC_SM	VCC_SM	
BH	NC		SB_DQ_2_1	SB_DQ_2_2	SB_DQ_2_3	SB_DQ_2_8	SB_DQ_2_7	SB_DQ_2_3	SB_DQ_2_8	SB_DQ_2_5	SB_DQ_2_7	SB_DQ_2_3	SB_DQ_2_8	SB_DQ_2_1	SB_MA_5	SB_MA_1_2	SB_MA_1_1	SB_MA_5_2	SA_MA_1	SA_MA_2	SA_MA_1	SA_MA_2	SB_MA_1	SA_MA_1	VCC_SM	VCC_SM	VCC_SM	
BG		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VCC_SM		VCC_SM
BF		SB_DQ_1_6	VCC_SM_LF	SA_DQ_8	SA_DQ_9	SA_DQ_8	SA_DQ_6	SA_DQ_7	SA_DQ_6	SA_DQ_4	SA_DQ_5	SA_DQ_7	SA_DQ_6	SA_DQ_4	SA_DQ_1	SA_DM_3	SB_CKE_0	VCC_SM	SA_CKE_1	SA_MA_1	SA_MA_2	SB_MA_4	SB_MA_6	SA_MA_1	VCC_SM	VCC_SM		
BE	NC	SB_DQ_2_0	SB_DQ_2_7	SA_DQ_1	SA_DQ_3	SA_DQ_2	SA_DQ_3	SA_DQ_2	SA_DQ_3	SA_DQ_4	SA_DQ_5	SA_DQ_6	SA_DQ_7	SA_DQ_8	SA_DQ_1	SA_DM_3	SB_CKE_0	VCC_SM	SA_CKE_1	SA_MA_1	SA_MA_2	SB_CKE_0	SA_CKE_1	SA_MA_1	VCC_SM	VCC_SM		
BD	VSS	SB_DQ_1_4	SA_DQ_4	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC_SM	VCC_SM		
BC	SB_DQ_5	SB_DQ_1_1	SM_VRE_F	SA_DQ_2	SA_DQ_7	SA_DQ_2	SA_DQ_7	SA_DQ_2	SA_DQ_3	SA_DQ_2	SA_DQ_3	SA_DQ_2	SA_DQ_3	SA_DQ_4	SA_DQ_5	SB_CKE_1	SA_CKE_0	SB_CKE_0	SA_CKE_0	SA_CKE_0	SA_CKE_0	SA_CKE_0	SA_CKE_0	SA_CKE_0	SA_CKE_0	VCC_SM		
BB	SB_DQ_3_1	SB_DQ_3_0	SA_DM_1	VSS	SA_DM_2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC_SM_LF	VCC_SM	VCC_SM	SA_MA_1	SA_MA_2	SA_MA_1	SA_MA_2	SA_MA_1	SA_MA_2	SA_MA_1	SA_MA_2	VCC_SM	
BA	VSS	SB_DQ_1_1	VSS	SA_DQ_1	SA_DQ_4	SA_DQ_1	SA_DQ_4	SA_DQ_1	SA_DQ_2	SA_DQ_1	SA_DQ_2	SA_DQ_1	SA_DQ_2	SA_DQ_3	VSS	PWROK	SM_DRA_MRST#	SM_PWR_OK	VSS	SB_OK_0	SA_CK_0	SA_CK_0	SB_OK_0	SA_CK_0	SA_CK_0	SA_CK_0	VCC_SM	
AY	SB_DM_1	SB_DQ_3	SA_DQ_5	SA_DQ_0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PWROK	CL_PWR_OK	VSS	VSS	VCC_SM	VCC_SM	VCC_SM	VCC_SM	VCC_SM	VCC_SM	VSS		
AW	SB_DQ_3	SB_DQ_1_2	SA_DQ_1	VSS	SA_DQ_3	VSS	SA_DQ_1	VSS	VSS	VSS	VSS	VSS	VSS	RVID	CL_PWR_OK	VSS	VSS	VSS	VSS	VCC_SM	VCC_SM	VCC_SM	VCC_SM	VCC_SM	VSS			
AV	SB_DQ_3	SB_DQ_1_2	SA_DQ_1	VSS	SA_DQ_3	VSS	SA_DQ_1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC_S_MCK	VCC_S_MCK	VCC_S_MCK	VCC_S_MCK	VCC_S_MCK	VCC_S_MCK			
AU	VSS	SB_DQ_7	VSS	SA_DQ_0	SA_DQ_1	SA_DQ_1	VCC_SM_LF	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC_S_MCK_N	VCC_S_MCK_N	VCC_S_MCK_N	VCC_S_MCK_N	VCC_S_MCK_N	VCC_S_MCK_N			
AT	SB_DQ_0	SB_DQ_4	SA_DM_0	VSS	SA_DQ_0	SA_DQ_1	SA_DQ_0	ME_JTAG_TDO	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		
AR	SB_DQ_3	SB_DQ_0	VSS	SA_DQ_0	SA_DQ_0	SA_DQ_0	VSS	SA_DQ_0	VSS	VCC	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		
AP	SB_DQ_0	SB_DM_0	SA_DQ_0	VSS	SA_DQ_0	VSS	SA_DQ_0	ME_JTAG_TDI	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		
AN	VSS	SB_DQ_5	VSS	SA_DQ_0	ME_JTAG_TMS	ME_JTAG_TCK	VCC_DM	VCC_DM	VCC	VSS	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VSS	VSS	VSS	VSS	VSS	VSS		
AM	SB_DQ_4	SB_DQ_3	VSS	VSS	VSS	VSS	VSS	VCC_DM	VCC_DM	VSS	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		
AL	CL_VREF	CL_RST#	VSS	DML_RXN_1	DML_RXN_2	DML_RXN_3	DML_RXP_2	DML_RXP_3	VCC_DM	VCC_DM	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		
AK	CL_DATA	CL_CLK	DML_RXP_1	VSS	DML_TXN_1	DML_TXN_2	DML_TXP_1	DML_TXP_2	VCCA_P_EG_B6	VCCA_P_EG_PLI	VSS	VCC	VCC	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		
AJ	VSS	VSS	VSS	DML_RXN_1	DML_RXN_2	DML_RXP_1	VSS	VSS	VSS	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		
AH	DML_RXN_2	DML_RXP_2	VSS	DML_RXN_0	DML_RXN_3	DML_RXP_3	VCCA_P_EG_PLI	VCCA_P_EG_PLI	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC_AX_G	VCC_AX_G	VCC_AX_G			
AG	DML_RXN_0	DML_RXP_0	VSS	DML_RXN_0	DML_RXN_3	DML_RXP_3	VCCA_P_EG_PLI	VCCA_P_EG_PLI	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VCC_AX_G	VCC_AX_G	VCC_AX_G	VCC_AX_G	VCC_AX_G			

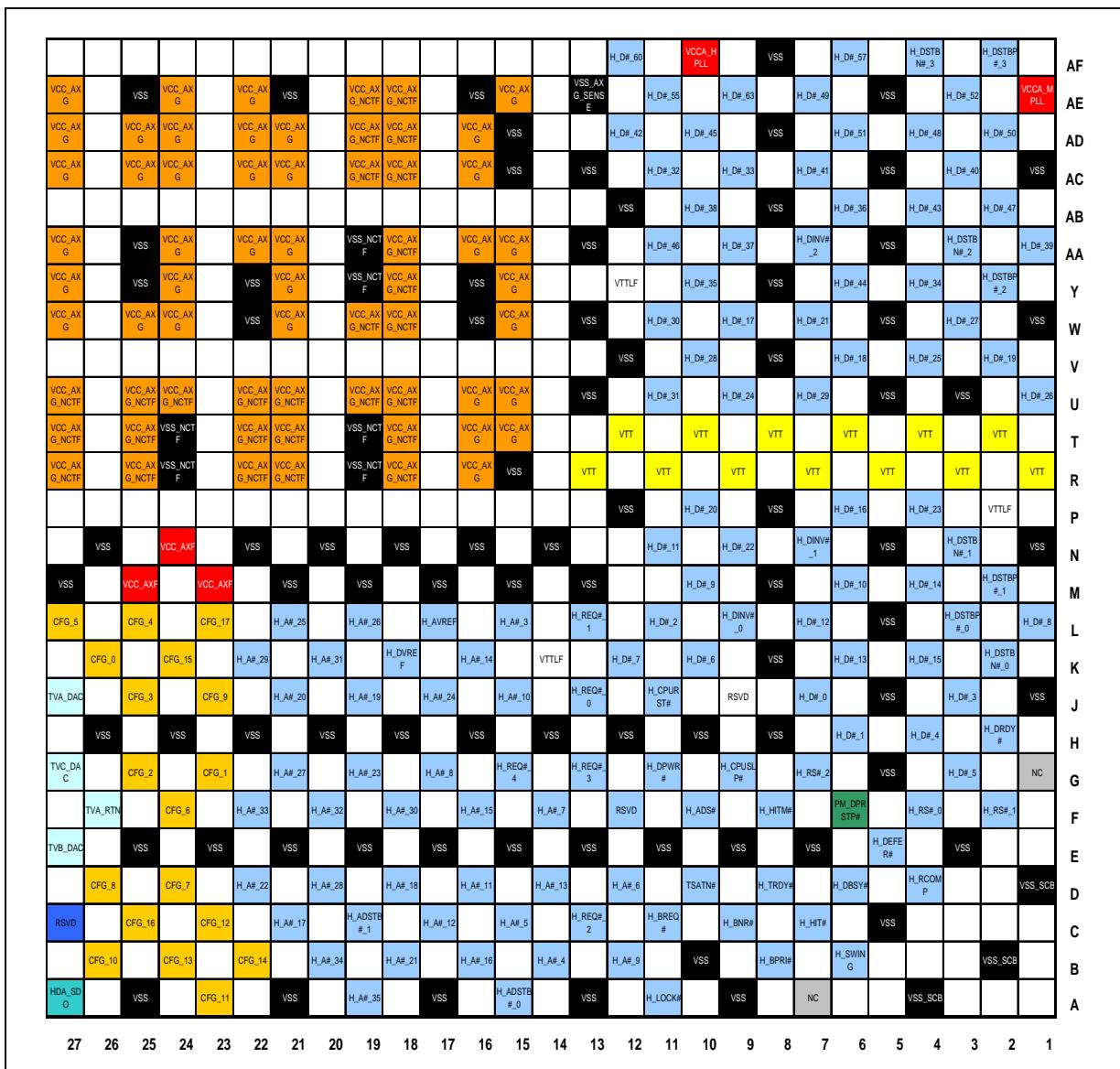


Figure 27. Ballout Diagram (Top View) Upper Right Quadrant

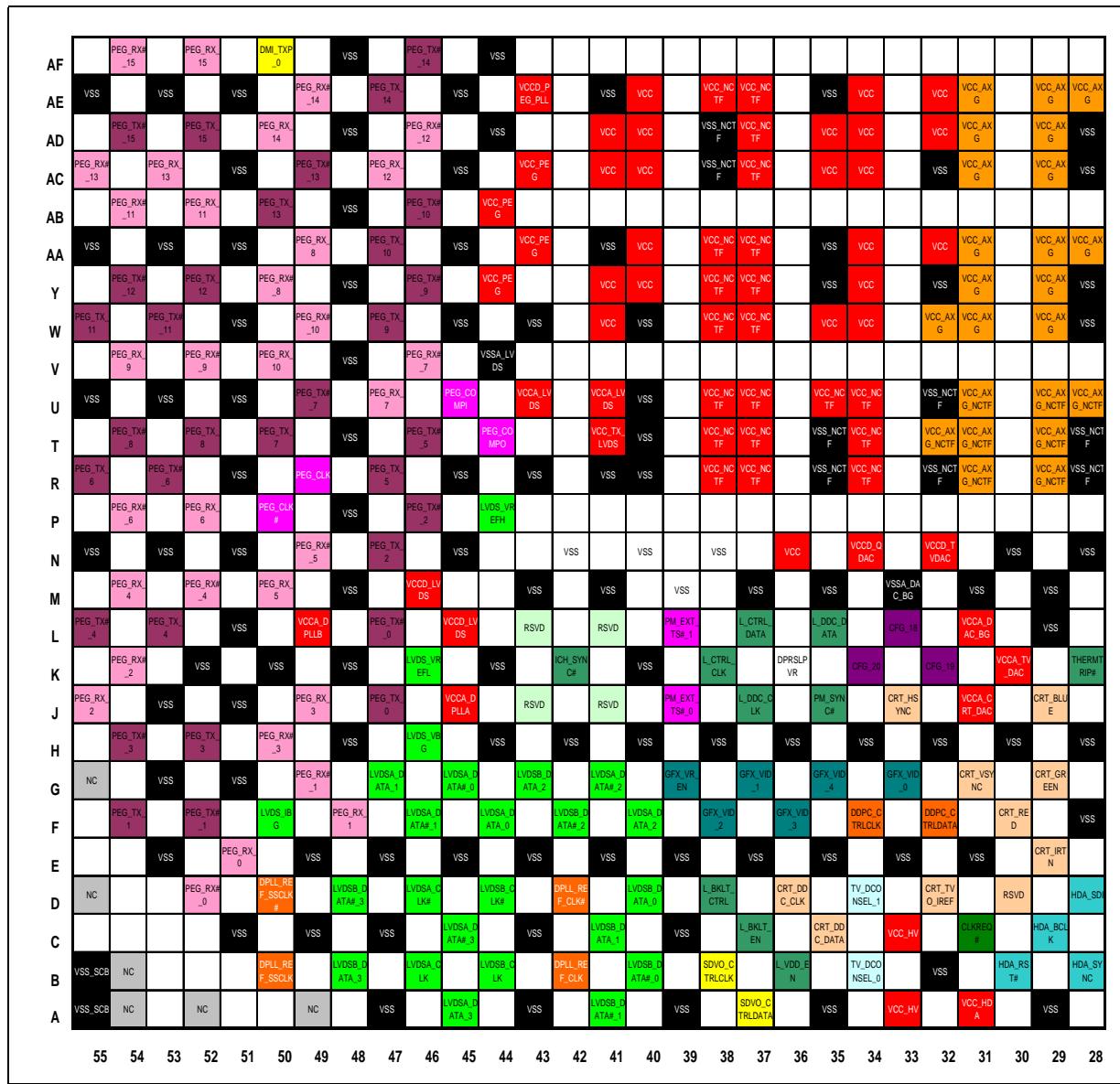




**Figure 28. Ballout Diagram (Top View) Lower Right Quadrant**



**Figure 29. Ballout Diagram (Top View) Lower Left Quadrant**





## 16.5 Intel GS45 Express Chipset Package Information

The Intel GS45 Express Chipset (SFF GMCH) comes in an FCBGA package, which consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die.

**Caution:** Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

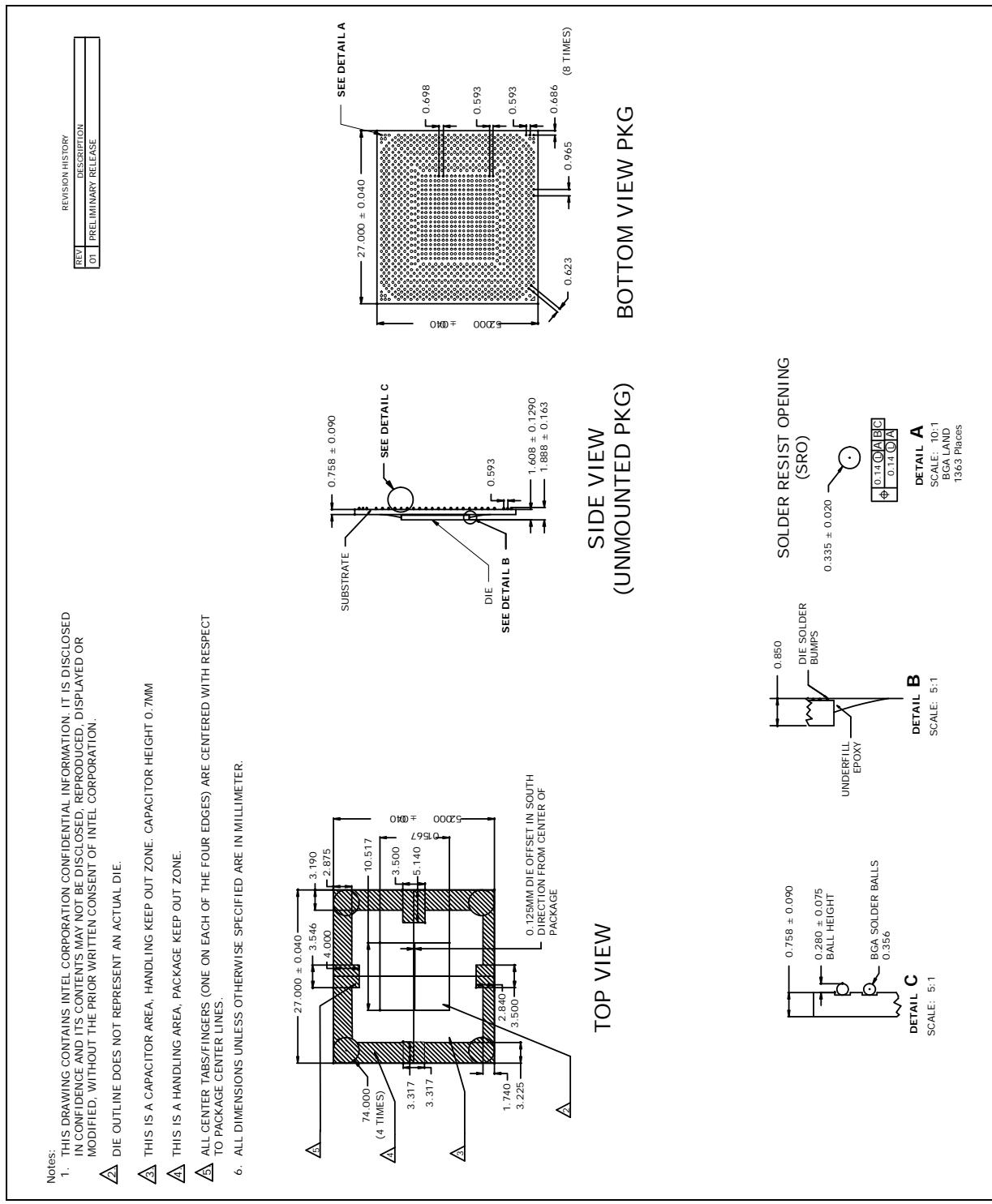
The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Dimensions are in millimeters. Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994.

- Tolerances:
  - X:  $\pm 0.1$
  - XX:  $\pm 0.05$
- Angles:  $\pm 1.0$  degrees
- Package parameters: 1363 FCBGA, 27 mm x 25 mm, 0.593-mm minimum ball pitch
- Solder resist opening: 335 microns
- Outgoing coplanarity (max): 0.2 mm (8 mils)



Figure 30. Intel GS45 Express Chipset Drawing



**Table 34. Intel GS45 Chipset Pinlist (Sheet 1 of 13)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
A11	H_LOCK#	AT46	SA_DQ_2	D14	H_A#_13
A13	VSS	AT48	VSS	D16	H_A#_11
A15	H_ADSTB#_0	AT50	SA_DM_0	D18	H_A#_18
A17	VSS	AT52	SB_DQ_6	D20	H_A#_28
A19	H_A#_35	AT54	SB_DQS#_0	D22	H_A#_22
A21	VSS	AT6	SA_DQ_57	D24	CFG_7
A23	CFG_11	AT8	VSS	D26	CFG_8
A25	VSS	AU1	SB_DQ_50	D28	HDA_SDI
A27	HDA_SDO	AU11	SA_DQ_54	D30	RSVD
A29	VSS	AU13	VSS	D32	CRT_TVO_IREF
A31	VCC_HDA	AU15	VCCA_SM	D34	TV_DCONSEL_1
A33	VCC_HV	AU16	VCCA_SM	D36	CRT_DDC_CLK
A35	VSS	AU18	VCCA_SM	D38	L_BKLT_CTRL
A37	SDVO_CTRLDATA	AU19	VCCA_SM	D4	H_RCOMP
A39	VSS	AU21	VCCA_SM	D40	LVDSB_DATA_0
A4	VSS_SCB	AU22	VCCA_SM	D42	DPLL_REF_CLK#
A41	LVDSB_DATA#_1	AU24	VCCA_SM	D44	LVDSB_CLK#
A43	VSS	AU25	VSS	D46	LVDSA_CLK#
A45	LVDSA_DATA_3	AU27	VCCA_SM_CK	D48	LVDSB_DATA#_3
A47	VSS	AU28	VCCA_SM_CK	D50	DPLL_REF_SSCLK#
A49	NC	AU29	VCCA_SM_CK	D52	PEG_RX#_0
A52	NC	AU3	SB_DQ_54	D55	NC
A54	NC	AU31	VCCA_SM_CK	D6	H_DBSY#
A55	VSS_SCB	AU32	VSS	D8	H_TRDY#
A7	NC	AU34	VSS	E11	VSS
A9	VSS	AU35	VSS	E13	VSS
AA1	H_D#_39	AU37	VSS	E15	VSS
AA11	H_D#_46	AU38	VSS	E17	VSS
AA13	VSS	AU40	VSS	E19	VSS
AA15	VCC_AXG	AU41	VSS	E21	VSS
AA16	VCC_AXG	AU43	VSS	E23	VSS
AA18	VCC_AXG_NCTF	AU45	VCC_SM_LF	E25	VSS
AA19	VSS_NCTF	AU47	SA_DQ_1	E27	TVB_DAC
AA21	VCC_AXG	AU49	SA_DQ_3	E29	CRT_IRTN
AA22	VCC_AXG	AU5	VSS	E3	VSS
AA24	VCC_AXG	AU51	VSS	E31	VSS
AA25	VSS	AU53	SB_DQ_7	E33	VSS

**Table 34. Intel GS45 Chipset Pinlist (Sheet 2 of 13)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AA27	VCC_AXG	AU55	VSS	E35	VSS
AA28	VCC_AXG	AU7	SA_DQ_63	E37	VSS
AA29	VCC_AXG	AU9	VCC_SM_LF	E39	VSS
AA3	H_DSTBN#_2	AV10	SA_DM_6	E41	VSS
AA31	VCC_AXG	AV12	VSS	E43	VSS
AA32	VCC	AV2	SB_DQS_6	E45	VSS
AA34	VCC	AV4	SB_DQ_53	E47	VSS
AA35	VSS	AV44	VSS	E49	VSS
AA37	VCC_NCTF	AV46	SA_DQ_13	E5	H_DEFER#
AA38	VCC_NCTF	AV48	VSS	E51	PEG_RX_0
AA40	VCC	AV50	SA_DQ_6	E53	VSS
AA41	VSS	AV52	SB_DQ_12	E7	VSS
AA43	VCC_PEG	AV54	SB_DQ_3	E9	VSS
AA45	VSS	AV6	SA_DQ_48	F10	H_ADS#
AA47	PEG_TX_10	AV8	VSS	F12	RSVD
AA49	PEG_RX_8	AW1	VSS	F14	H_A#_7
AA5	VSS	AW11	SA_DQ_53	F16	H_A#_15
AA51	VSS	AW14	VCCA_SM	F18	H_A#_30
AA53	VSS	AW16	VCCA_SM	F2	H_RS#_1
AA55	VSS	AW18	VCCA_SM	F20	H_A#_32
AA7	H_DINV#_2	AW20	VCCA_SM	F22	H_A#_33
AA9	H_D#_37	AW22	VCCA_SM	F24	CFG_6
AB10	H_D#_38	AW24	VCCA_SM	F26	TVA_RTN
AB12	VSS	AW26	VCC_SM	F28	VSS
AB2	H_D#_47	AW28	VSS	F30	CRT_RED
AB4	H_D#_43	AW3	SB_DQS#_6	F32	DDPC_CTRLDATA
AB44	VCC_PEG	AW30	VCC_SM	F34	DDPC_CTRLCLK
AB46	PEG_TX#_10	AW32	VCC_SM	F36	GFX_VID_3
AB48	VSS	AW34	VCC_SM	F38	GFX_VID_2
AB50	PEG_TX_13	AW36	VSS	F4	H_RS#_0
AB52	PEG_RX_11	AW38	VSS	F40	LVDSA_DATA_2
AB54	PEG_RX#_11	AW40	CL_PWROK	F42	LVDSB_DATA#_2
AB6	H_D#_36	AW42	RSVD	F44	LVDSA_DATA_0
AB8	VSS	AW45	SA_DQS#_1	F46	LVDSA_DATA#_1
AC1	VSS	AW47	SA_DQ_8	F48	PEG_RX_1
AC11	H_D#_32	AW49	SA_DQ_10	F50	LVDS_IBG
AC13	VSS	AW5	VSS	F52	PEG_TX#_1
AC15	VSS	AW51	VSS	F54	PEG_TX_1



Table 34. Intel GS45 Chipset Pinlist (Sheet 3 of 13)

Ball	Signal	Ball	Signal	Ball	Signal
AC16	VCC_AXG	AW53	SB_DQ_8	F6	PM_DPRSTP#
AC18	VCC_AXG_NCTF	AW55	SB_DQ_13	F8	H_HITM#
AC19	VCC_AXG_NCTF	AW7	SA_DQ_50	G1	NC
AC21	VCC_AXG	AW9	SA_DQ_55	G11	H_DPWR#
AC22	VCC_AXG	AY10	VSS	G13	H_REQ#_3
AC24	VCC_AXG	AY13	VSS	G15	H_REQ#_4
AC25	VCC_AXG	AY15	VSS	G17	H_A#_8
AC27	VCC_AXG	AY17	VSS	G19	H_A#_23
AC28	VSS	AY19	VSS	G21	H_A#_27
AC29	VCC_AXG	AY2	SB_DM_6	G23	CFG_1
AC3	H_D#_40	AY21	VSS	G25	CFG_2
AC31	VCC_AXG	AY23	VSS	G27	TVC_DAC
AC32	VSS	AY25	VSS	G29	CRT_GREEN
AC34	VCC	AY27	VCC_SM	G3	H_D#_5
AC35	VCC	AY29	VCC_SM	G31	CRT_VSYNC
AC37	VCC_NCTF	AY31	VSS	G33	GFX_VID_0
AC38	VSS_NCTF	AY33	VSS	G35	GFX_VID_4
AC40	VCC	AY35	VSS	G37	GFX_VID_1
AC41	VCC	AY37	SM_PWROK	G39	GFX_VR_EN
AC43	VCC_PEG	AY39	PWROK	G41	LVDSA_DATA#_2
AC45	VSS	AY4	SB_DQ_47	G43	LVDSB_DATA_2
AC47	PEG_RX_12	AY41	VSS	G45	LVDSA_DATA#_0
AC49	PEG_TX#_13	AY43	VSS	G47	LVDSA_DATA_1
AC5	VSS	AY46	VSS	G49	PEG_RX#_1
AC51	VSS	AY48	VSS	G5	VSS
AC53	PEG_RX_13	AY50	SA_DQ_15	G51	VSS
AC55	PEG_RX#_13	AY52	SB_DQ_9	G53	VSS
AC7	H_D#_41	AY54	SB_DM_1	G55	NC
AC9	H_D#_33	AY6	SA_DQ_51	G7	H_RS#_2
AD10	H_D#_45	AY8	VSS	G9	H_CPUSLP#
AD12	H_D#_42	B10	VSS	H10	VSS
AD15	VSS	B12	H_A#_9	H12	VSS
AD16	VCC_AXG	B14	H_A#_4	H14	VSS
AD18	VCC_AXG_NCTF	B16	H_A#_16	H16	VSS
AD19	VCC_AXG_NCTF	B18	H_A#_21	H18	VSS
AD2	H_D#_50	B2	VSS_SCB	H2	H_DRDY#
AD21	VCC_AXG	B20	H_A#_34	H20	VSS
AD22	VCC_AXG	B22	CFG_14	H22	VSS

**Table 34. Intel GS45 Chipset Pinlist (Sheet 4 of 13)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AD24	VCC_AXG	B24	CFG_13	H24	VSS
AD25	VCC_AXG	B26	CFG_10	H26	VSS
AD27	VCC_AXG	B28	HDA_SYNC	H28	VSS
AD28	VSS	B30	HDA_RST#	H30	VSS
AD29	VCC_AXG	B32	VSS	H32	VSS
AD31	VCC_AXG	B34	TV_DCONSEL_0	H34	VSS
AD32	VCC	B36	L_VDD_EN	H36	VSS
AD34	VCC	B38	SDVO_CTRLCLK	H38	VSS
AD35	VCC	B40	LVDSB_DATA#_0	H4	H_D#_4
AD37	VCC_NCTF	B42	DPLL_REF_CLK	H40	VSS
AD38	VSS_NCTF	B44	LVDSB_CLK	H42	VSS
AD4	H_D#_48	B46	LVDSA_CLK	H44	VSS
AD40	VCC	B48	LVDSB_DATA_3	H46	LVDS_VBG
AD41	VCC	B50	DPLL_REF_SSCLK	H48	VSS
AD44	VSS	B54	NC	H50	PEG_RX#_3
AD46	PEG_RX#_12	B55	VSS_SCB	H52	PEG_TX_3
AD48	VSS	B6	H_SWING	H54	PEG_TX#_3
AD50	PEG_RX_14	B8	H_BPRI#	H6	H_D#_1
AD52	PEG_TX_15	BA1	SB_DO_48	H8	VSS
AD54	PEG_TX#_15	BA11	SA_DQS#_5	J1	VSS
AD6	H_D#_51	BA13	SA_DQS#_4	J11	H_CPURST#
AD8	VSS	BA15	SA_DO_32	J13	H_REQ#_0
AE1	VCCA_MPPLL	BA17	SB_MA_3	J15	H_A#_10
AE11	H_D#_55	BA19	VCC_SM_LF	J17	H_A#_24
AE13	VSS_AXG_SENSE	BA21	SA_MA_10	J19	H_A#_19
AE15	VCC_AXG	BA23	SB_CK_1	J21	H_A#_20
AE16	VSS	BA25	SA_CK_1	J23	CFG_9
AE18	VCC_AXG_NCTF	BA27	VCC_SM	J25	CFG_3
AE19	VCC_AXG_NCTF	BA29	VCC_SM	J27	TVA_DAC
AE21	VSS	BA3	SB_DO_43	J29	CRT_BLUE
AE22	VCC_AXG	BA31	SA_CK#_0	J3	H_D#_3
AE24	VCC_AXG	BA33	SB_CK_0	J31	VCCA_CRT_DAC
AE25	VSS	BA35	VSS	J33	CRT_HSYNC
AE27	VCC_AXG	BA37	SM_DRAMRST#	J35	PM_SYNC#
AE28	VCC_AXG	BA39	VSS	J37	L_DDC_CLK
AE29	VCC_AXG	BA41	SA_DQS#_3	J39	PM_EXT_TS#_0
AE3	H_D#_52	BA43	SA_DO_22	J41	RSVD
AE31	VCC_AXG	BA45	SA_DQS_1	J43	RSVD



Table 34. Intel GS45 Chipset Pinlist (Sheet 5 of 13)

Ball	Signal	Ball	Signal	Ball	Signal
AE32	VCC	BA47	SA_DQ_14	J45	VCCA_DPLLA
AE34	VCC	BA49	SA_DQ_11	J47	PEG_TX_0
AE35	VSS	BA5	VSS	J49	PEG_RX_3
AE37	VCC_NCTF	BA51	VSS	J5	VSS
AE38	VCC_NCTF	BA53	SB_DQS_1	J51	VSS
AE40	VCC	BA55	VSS	J53	VSS
AE41	VSS	BA7	SA_DQS_6	J55	PEG_RX_2
AE43	VCCD_PEG_PLL	BA9	SA_DQS#_6	J7	H_D#_0
AE45	VSS	BB10	SA_DQS_5	J9	RSVD
AE47	PEG_TX_14	BB12	SA_DM_4	K10	H_D#_6
AE49	PEG_RX#_14	BB14	SA_DQ_36	K12	H_D#_7
AE5	VSS	BB16	VCC_SM	K14	VTTLF
AE51	VSS	BB18	RSTIN#	K16	H_A#_14
AE53	VSS	BB2	SB_DQS_5	K18	H_DVREF
AE55	VSS	BB20	RSVD	K2	H_DSTBN#_0
AE7	H_D#_49	BB22	VSS	K20	H_A#_31
AE9	H_D#_63	BB24	SB_CK#_1	K22	H_A#_29
AF10	VCCA_HPLL	BB26	SA_MA_8	K24	CFG_15
AF12	H_D#_60	BB28	VCC_SM	K26	CFG_0
AF2	H_DSTBP#_3	BB30	VCC_SM	K28	THERMTRIP#
AF4	H_DSTBN#_3	BB32	SA_CK_0	K30	VCCA_TV_DAC
AF44	VSS	BB34	SA_MA_6	K32	CFG_19
AF46	PEG_TX#_14	BB36	VCC_SM	K34	CFG_20
AF48	VSS	BB38	VCC_SM_LF	K36	DPRSLPVR
AF50	DMI_TXP_0	BB4	SB_DQ_46	K38	L_CTRL_CLK
AF52	PEG_RX_15	BB40	SA_DQ_28	K4	H_D#_15
AF54	PEG_RX#_15	BB42	VSS	K40	VSS
AF6	H_D#_57	BB44	VSS	K42	ICH_SYNC#
AF8	VSS	BB46	SA_DM_2	K44	VSS
AG1	VSS	BB48	VSS	K46	LVDS_VREFL
AG11	VSS	BB50	SA_DM_1	K48	VSS
AG13	VCC_AXG_SENSE	BB52	SB_DQ_10	K50	VSS
AG15	VCC_AXG	BB54	SB_DQS#_1	K52	VSS
AG16	VSS	BB6	SA_DQ_49	K54	PEG_RX#_2
AG18	VCC_AXG_NCTF	BB8	VSS	K6	H_D#_13
AG19	VCC_AXG_NCTF	BC1	VSS	K8	VSS
AG21	VSS	BC11	SA_DQ_41	L1	H_D#_8
AG22	VCC_AXG	BC13	SA_DQS_4	L11	H_D#_2

**Table 34. Intel GS45 Chipset Pinlist (Sheet 6 of 13)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AG24	VCC_AXG	BC15	SA_DQ_37	L13	H_REQ#_1
AG25	VSS	BC17	SB_ODT_0	L15	H_A#_3
AG27	VCC_AXG	BC19	SB_CS#_1	L17	H_AVREF
AG28	VCC_AXG	BC21	SA_BS_0	L19	H_A#_26
AG29	VCC_AXG	BC23	SA_MA_0	L21	H_A#_25
AG3	H_DINV#_3	BC25	SA_CK#_1	L23	CFG_17
AG31	VCC_AXG	BC27	VCC_SM	L25	CFG_4
AG32	VSS	BC29	VCC_SM	L27	CFG_5
AG34	VCC	BC3	SB_DQS#_5	L29	VSS
AG35	VSS	BC31	SA_MA_3	L3	H_DSTBP#_0
AG37	VCC_NCTF	BC33	SB_CK#_0	L31	VCCA_DAC_BG
AG38	VCC_NCTF	BC35	SA_CKE_0	L33	CFG_18
AG40	VCC	BC37	SB_CKE_1	L35	L_DDC_DATA
AG41	VSS	BC39	SA_DQ_25	L37	L_CTRL_DATA
AG43	VCCA_PEG_PLL	BC41	SA_DQS_3	L39	PM_EXT_TS#_1
AG45	DMI_TXP_3	BC43	SA_DQ_20	L41	RSVD
AG47	DMI_TXN_3	BC45	SA_DQS#_2	L43	RSVD
AG49	DMI_TXN_0	BC47	SA_DQ_17	L45	VCCD_LVDS
AG5	VSS	BC49	SA_DQ_12	L47	PEG_TX#_0
AG51	VSS	BC5	VSS	L49	VCCA_DPPLL_B
AG53	DMI_RXP_0	BC51	SM_VREF	L5	VSS
AG55	DMI_RXN_0	BC53	SB_DQ_11	L51	VSS
AG7	H_D#_54	BC55	SB_DQ_15	L53	PEG_TX_4
AG9	H_D#_53	BC7	SA_DQ_44	L55	PEG_TX#_4
AH10	HPLL_CLK	BC9	SA_DQ_45	L7	H_D#_12
AH12	VCCD_HPLL	BD10	VSS	L9	H_DINV#_0
AH15	VCC_AXG	BD12	VSS	M10	H_D#_9
AH16	VCC_AXG	BD14	VSS	M13	VSS
AH18	VCC_AXG_NCTF	BD16	VSS	M15	VSS
AH19	VCC_AXG_NCTF	BD18	VSS	M17	VSS
AH2	SB_DQ_62	BD2	SB_DM_5	M19	VSS
AH21	VCC_AXG	BD20	VSS	M2	H_DSTBP#_1
AH22	VCC_AXG	BD22	VSS	M21	VSS
AH24	VCC_AXG	BD24	VSS	M23	VCC_AXF
AH25	VCC_AXG	BD26	VSS	M25	VCC_AXF
AH27	VCC_AXG	BD28	VCC_SM	M27	VSS
AH28	VCC_AXG	BD30	VCC_SM	M29	VSS
AH29	VCC_AXG	BD32	VSS	M31	VSS



Table 34. Intel GS45 Chipset Pinlist (Sheet 7 of 13)

Ball	Signal	Ball	Signal	Ball	Signal
AH31	VCC	BD34	VSS	M33	VSSA_DAC_BG
AH32	VCC	BD36	VSS	M35	VSS
AH34	VCC	BD38	VSS	M37	VSS
AH35	VCC	BD4	SB_DQ_42	M39	VSS
AH37	VCC_NCTF	BD40	VSS	M4	H_D#_14
AH38	VSS_NCTF	BD42	VSS	M41	VSS
AH4	H_D#_61	BD44	VSS	M43	VSS
AH40	VCC	BD46	VSS	M46	VCCD_LVDS
AH41	VCC	BD48	VSS	M48	VSS
AH44	VSS	BD50	SA_DQ_9	M50	PEG_RX_5
AH46	VSS	BD52	SB_DQ_14	M52	PEG_RX#_4
AH48	VSS	BD54	VSS	M54	PEG_RX_4
AH50	DMI_TXP_1	BD6	SA_DQ_46	M6	H_D#_10
AH52	DMI_RXP_2	BD8	VSS	M8	VSS
AH54	DMI_RXN_2	BE1	NC	N1	VSS
AH6	H_D#_59	BE11	SA_DQ_33	N11	H_D#_11
AH8	VSS	BE13	SA_DQ_38	N14	VSS
AJ1	SB_DQ_59	BE15	SA_DQ_34	N16	VSS
AJ11	HPLL_CLK#	BE17	SB_ODT_1	N18	VSS
AJ13	VSS	BE19	RSVD	N20	VSS
AJ15	VCC_AXG	BE21	SB_RAS#	N22	VSS
AJ16	VCC_AXG	BE23	SB_CS#_0	N24	VCC_AXF
AJ18	VCC_AXG_NCTF	BE25	SA_MA_14	N26	VSS
AJ19	VSS_NCTF	BE27	VCC_SM	N28	VSS
AJ21	VCC_AXG	BE29	VCC_SM	N3	H_DSTBN#_1
AJ22	VCC_AXG	BE3	VSS	N30	VSS
AJ24	VCC_AXG	BE31	SA_MA_2	N32	VCCD_TVDAC
AJ25	VCC	BE33	SA_CKE_1	N34	VCCD_QDAC
AJ27	VSS	BE35	VCC_SM	N36	VCC
AJ28	VCC	BE37	SB_CKE_0	N38	VSS
AJ29	VSS	BE39	SA_DM_3	N40	VSS
AJ3	SB_DM_7	BE41	SA_DQ_31	N42	VSS
AJ31	VCC	BE43	SA_DQ_29	N45	VSS
AJ32	VCC	BE45	SA_DQS_2	N47	PEG_TX_2
AJ34	VCC	BE47	SA_DQ_23	N49	PEG_RX#_5
AJ35	VCC	BE49	SA_DQ_21	N5	VSS
AJ37	VCC_NCTF	BE5	SB_DQ_44	N51	VSS
AJ38	VSS_NCTF	BE51	SB_DQ_17	N53	VSS

**Table 34. Intel GS45 Chipset Pinlist (Sheet 8 of 13)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AJ40	VCC	BE53	SB_DQ_20	N55	VSS
AJ41	VCC	BE55	NC	N7	H_DINV#_1
AJ43	VCCA_PEG_BG	BE7	SA_DM_5	N9	H_D#_22
AJ45	DMI_TXP_2	BE9	VCC_SM_LF	P10	H_D#_20
AJ47	DMI_TXN_2	BF10	SA_DO_40	P12	VSS
AJ49	DMI_TXN_1	BF12	SA_DO_47	P2	VTTLF
AJ5	VSS	BF14	SA_DO_35	P4	H_D#_23
AJ51	VSS	BF16	SA_DO_39	P44	LVDS_VREFH
AJ53	VSS	BF18	RSVD	P46	PEG_RX#_2
AJ55	VSS	BF2	SB_DQ_45	P48	VSS
AJ7	H_D#_62	BF20	RSVD	P50	PEG_CLK#
AJ9	H_D#_58	BF22	SA_MA_1	P52	PEG_RX_6
AK10	RSVD	BF24	VCC_SM	P54	PEG_RX#_6
AK12	VSS	BF26	VSS	P6	H_D#_16
AK2	SB_DQ_63	BF28	VCC_SM	P8	VSS
AK4	SB_DQ_60	BF30	VCC_SM	R1	VTT
AK44	VSS	BF32	SA_MA_9	R11	VTT
AK46	VSS	BF34	SB_MA_6	R13	VTT
AK48	VSS	BF36	SB_MA_4	R15	VSS
AK50	DMI_RXP_1	BF38	SA_DO_30	R16	VCC_AXG
AK52	CL_CLK	BF4	SB_DQ_41	R18	VCC_AXG_NCTF
AK54	CL_DATA	BF40	SA_DO_27	R19	VSS_NCTF
AK6	H_D#_56	BF42	SA_DO_24	R21	VCC_AXG_NCTF
AK8	VSS	BF44	SA_DO_26	R22	VCC_AXG_NCTF
AL1	VSS	BF46	SA_DO_16	R24	VSS_NCTF
AL11	RSVD	BF48	SA_DO_19	R25	VCC_AXG_NCTF
AL13	VSS	BF50	SA_DO_18	R27	VCC_AXG_NCTF
AL15	VCC_AXG	BF52	VCC_SM_LF	R28	VSS_NCTF
AL16	VCC_AXG	BF54	SB_DQ_16	R29	VCC_AXG_NCTF
AL18	VCC_AXG_NCTF	BF6	VSS	R3	VTT
AL19	VCC_AXG_NCTF	BF8	SA_DO_42	R31	VCC_AXG_NCTF
AL21	VCC_AXG	BG11	VSS	R32	VSS_NCTF
AL22	VCC_AXG	BG13	VSS	R34	VCC_NCTF
AL24	VSS	BG15	VSS	R35	VSS_NCTF
AL25	VCC	BG17	VSS	R37	VCC_NCTF
AL27	VCC	BG19	VSS	R38	VCC_NCTF
AL28	VCC	BG21	VSS	R40	VSS
AL29	VCC	BG23	VSS	R41	VSS



Table 34. Intel GS45 Chipset Pinlist (Sheet 9 of 13)

Ball	Signal	Ball	Signal	Ball	Signal
AL3	SB_DQ_58	BG25	SA_MA_11	R43	VSS
AL31	VCC	BG27	VCC_SM	R45	VSS
AL32	VCC	BG29	VCC_SM	R47	PEG_TX_5
AL34	VCC	BG3	SB_DQ_40	R49	PEG_CLK
AL35	VSS	BG31	VSS	R5	VTT
AL37	VCC_NCTF	BG33	VSS	R51	VSS
AL38	VCC_NCTF	BG35	VSS	R53	PEG_TX#_6
AL40	VCC	BG37	VSS	R55	PEG_TX_6
AL41	VSS	BG39	VSS	R7	VTT
AL43	VCC_DMI	BG41	VSS	R9	VTT
AL45	DMI_RXP_3	BG43	VSS	T10	VTT
AL47	DMI_RXN_3	BG45	VSS	T12	VTT
AL49	DMI_RXN_1	BG47	VSS	T15	VCC_AXG
AL5	VSS	BG49	VSS	T16	VCC_AXG
AL51	VSS	BG5	SB_DQ_38	T18	VCC_AXG_NCTF
AL53	CL_RST#	BG51	VSS	T19	VSS_NCTF
AL55	CL_VREF	BG53	VSS	T2	VTT
AL7	SA_DQ_59	BG7	SA_DQ_43	T21	VCC_AXG_NCTF
AL9	VCC_SM_LF	BG9	VSS	T22	VCC_AXG_NCTF
AM10	RSVD	BH1	NC	T24	VSS_NCTF
AM12	VSS	BH10	SB_DQ_33	T25	VCC_AXG_NCTF
AM15	VCC_AXG	BH12	SB_DM_4	T27	VCC_AXG_NCTF
AM16	VCC_AXG	BH14	SB_CAS#	T28	VSS_NCTF
AM18	VCC_AXG_NCTF	BH16	SB_MA_10	T29	VCC_AXG_NCTF
AM19	VCC_AXG_NCTF	BH18	SA_MA_13	T31	VCC_AXG_NCTF
AM2	SB_DQS_7	BH20	SM_REXT	T32	VCC_AXG_NCTF
AM21	VCC_AXG	BH22	SA_RAS#	T34	VCC_NCTF
AM22	VCC_AXG	BH24	SB_MA_2	T35	VSS_NCTF
AM24	VCC	BH26	SA_MA_4	T37	VCC_NCTF
AM25	VCC	BH28	VCC_SM	T38	VCC_NCTF
AM27	VCC	BH30	VCC_SM	T4	VTT
AM28	VCC	BH32	SA_MA_7	T40	VSS
AM29	VCC	BH34	SA_MA_12	T41	VCC_TX_LVDS
AM31	VCC	BH36	SB_MA_5	T44	PEG_COMPO
AM32	VCC	BH38	SB_MA_12	T46	PEG_TX#_5
AM34	VCC	BH4	VSS	T48	VSS
AM35	VCC	BH40	SB_MA_9	T50	PEG_TX_7
AM37	VCC_NCTF	BH42	SB_DQS#_3	T52	PEG_TX_8

**Table 34. Intel GS45 Chipset Pinlist (Sheet 10 of 13)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AM38	VCC_NCTF	BH44	SB_DQ_27	T54	PEG_TX#_8
AM4	SB_DQ_61	BH46	SB_DQ_28	T6	VTT
AM40	VCC	BH48	SB_DQ_18	T8	VTT
AM41	VSS	BH50	SB_DQS_2	U1	H_D#_26
AM44	VCC_DMI	BH52	SB_DQ_21	U11	H_D#_31
AM46	VSS	BH55	NC	U13	VSS
AM48	VSS	BH6	SB_DQ_35	U15	VCC_AXG
AM50	VSS	BH8	SB_DQS_4	U16	VCC_AXG
AM52	SB_DQ_1	BJ11	SB_MA_13	U18	VCC_AXG_NCTF
AM54	SB_DQ_4	BJ13	SB_BS_0	U19	VCC_AXG_NCTF
AM6	SA_DQ_62	BJ15	SB_MA_0	U21	VCC_AXG_NCTF
AM8	VSS	BJ17	SA_ODT_0	U22	VCC_AXG_NCTF
AN1	SB_DQ_56	BJ19	SA_ODT_1	U24	VCC_AXG_NCTF
AN11	RSVD	BJ21	SA_BS_1	U25	VCC_AXG_NCTF
AN13	VSS	BJ23	VCC_SM_CK	U27	VCC_AXG_NCTF
AN15	VSS	BJ25	VSS	U28	VCC_AXG_NCTF
AN16	VSS	BJ27	VCC_SM	U29	VCC_AXG_NCTF
AN18	VSS_NCTF	BJ29	VCC_SM	U3	VSS
AN19	VSS_NCTF	BJ31	VSS	U31	VCC_AXG_NCTF
AN21	VSS	BJ33	SB_MA_1	U32	VSS_NCTF
AN22	VSS	BJ35	SA_MA_5	U34	VCC_NCTF
AN24	VSS	BJ37	SB_MA_8	U35	VCC_NCTF
AN25	VSS	BJ39	SB_DQ_31	U37	VCC_NCTF
AN27	VSS	BJ41	SA_BS_2	U38	VCC_NCTF
AN28	VSS	BJ43	SB_DM_3	U40	VSS
AN29	VSS	BJ45	SB_DQ_25	U41	VCCA_LVDS
AN3	SB_DQS#_7	BJ47	SB_DQ_23	U43	VCCA_LVDS
AN31	VSS	BJ49	SB_DM_2	U45	PEG_COMPI
AN32	VSS	BJ5	SB_DQ_39	U47	PEG_RX_7
AN34	VSS	BJ51	SB_DQS#_2	U49	PEG_TX#_7
AN35	VCC	BJ7	VSS	U5	VSS
AN37	VCC_NCTF	BJ9	SB_DQ_36	U51	VSS
AN38	VCC_NCTF	BK1	NC	U53	VSS
AN40	VSS	BK10	SB_DQ_32	U55	VSS
AN41	VCC	BK12	SB_BS_1	U7	H_D#_29
AN43	VCC_DMI	BK14	SB_WE#	U9	H_D#_24
AN45	ME_JTAG_TCK	BK16	SA_CS#_1	V10	H_D#_28
AN47	ME_JTAG_TMS	BK18	SA_CS#_0	V12	VSS



Table 34. Intel GS45 Chipset Pinlist (Sheet 11 of 13)

Ball	Signal	Ball	Signal	Ball	Signal
AN49	SA_DQ_5	BK2	NC	V2	H_D#_19
AN5	VSS	BK20	SA_CAS#	V4	H_D#_25
AN51	VSS	BK22	VCC_SM_CK	V44	VSSA_LVDS
AN53	SB_DQ_5	BK24	VCC_SM_CK	V46	PEG_RX#_7
AN55	VSS	BK26	SM_RCOMP#	V48	VSS
AN7	SA_DQS_7	BK28	VCC_SM	V50	PEG_RX_10
AN9	SA_DQS#_7	BK30	VCC_SM	V52	PEG_RX#_9
AP10	VSS	BK32	SM_RCOMP_VOH	V54	PEG_RX_9
AP12	VSS	BK34	SB_MA_7	V6	H_D#_18
AP2	SB_DQ_49	BK36	SB_MA_11	V8	VSS
AP4	SB_DQ_57	BK38	SB_BS_2	W1	VSS
AP44	ME_JTAG_TDI	BK40	SB_DQ_30	W11	H_D#_30
AP46	SA_DQ_0	BK42	SB_DQS_3	W13	VSS
AP48	VSS	BK44	SB_DQ_29	W15	VCC_AXG
AP50	SA_DQ_7	BK46	SB_DQ_22	W16	VSS
AP52	SB_DM_0	BK48	SB_DQ_19	W18	VCC_AXG_NCTF
AP54	SB_DQ_0	BK50	VSS	W19	VCC_AXG_NCTF
AP6	SA_DQ_58	BK54	NC	W21	VCC_AXG
AP8	VSS	BK55	NC	W22	VSS
AR1	VSS	BK6	SB_DQ_34	W24	VCC_AXG
AR11	SA_DQ_56	BK8	SB_DQS#_4	W25	VCC_AXG
AR13	VSS	BL1	VSS_SCB	W27	VCC_AXG
AR15	VCCA_SM	BL11	SB_DQ_37	W28	VSS
AR16	VCCA_SM	BL13	VSS	W29	VCC_AXG
AR18	VCCA_SM_NCTF	BL15	SA_WE#	W3	H_D#_27
AR19	VCCA_SM_NCTF	BL17	VSS	W31	VCC_AXG
AR21	VCCA_SM_NCTF	BL19	VCC_SM	W32	VCC_AXG
AR22	VCCA_SM_NCTF	BL2	NC	W34	VCC
AR24	VCCA_SM_NCTF	BL21	VSS	W35	VCC
AR25	VSS_NCTF	BL23	VCC_SM_CK	W37	VCC_NCTF
AR27	VCCA_SM_CK_NCTF	BL25	SM_RCOMP	W38	VCC_NCTF
AR28	VCCA_SM_CK_NCTF	BL27	VCC_SM	W40	VSS
AR29	VCCA_SM_CK_NCTF	BL29	VCC_SM	W41	VCC
AR3	SB_DQ_55	BL31	SM_RCOMP_VOL	W43	VSS
AR31	VCCA_SM_CK_NCTF	BL33	VSS	W45	VSS

**Table 34. Intel GS45 Chipset Pinlist (Sheet 12 of 13)**

<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>	<b>Ball</b>	<b>Signal</b>
AR32	VSS_NCTF	BL35	VSS	W47	PEG_TX_9
AR34	VCC_NCTF	BL37	SB_MA_14	W49	PEG_RX#_10
AR35	VCC_NCTF	BL39	VSS	W5	VSS
AR37	VCC_NCTF	BL4	NC	W51	VSS
AR38	VCC_NCTF	BL41	SB_DQ_26	W53	PEG_TX#_11
AR40	VSS	BL43	VSS	W55	PEG_TX_11
AR41	VCC	BL45	SB_DQ_24	W7	H_D#_21
AR43	VSS	BL47	VSS	W9	H_D#_17
AR45	SA_DQ_4	BL49	NC	Y10	H_D#_35
AR47	SA_DQS_0	BL52	NC	Y12	VTTLF
AR49	SA_DQS#_0	BL54	NC	Y15	VCC_AXG
AR5	VSS	BL55	VSS_SCB	Y16	VSS
AR51	VSS	BL7	NC	Y18	VCC_AXG_NCTF
AR53	SB_DQS_0	BL9	VSS	Y19	VSS_NCTF
AR55	SB_DQ_2	C11	H_BREQ#	Y2	H_DSTBP#_2
AR7	SA_DQ_60	C13	H_REQ#_2	Y21	VCC_AXG
AR9	SA_DM_7	C15	H_A#_5	Y22	VSS
AT10	SA_DQ_52	C17	H_A#_12	Y24	VCC_AXG
AT12	SA_DQ_61	C19	H_ADSTB#_1	Y25	VSS
AT15	VCCA_SM	C21	H_A#_17	Y27	VCC_AXG
AT16	VCCA_SM	C23	CFG_12	Y28	VSS
AT18	VCCA_SM_NCTF	C25	CFG_16	Y29	VCC_AXG
AT19	VCCA_SM_NCTF	C27	RSVD	Y31	VCC_AXG
AT2	SB_DQ_51	C29	HDA_BCLK	Y32	VSS
AT21	VCCA_SM_NCTF	C31	CLKREQ#	Y34	VCC
AT22	VCCA_SM_NCTF	C33	VCC_HV	Y35	VSS
AT24	VCCA_SM_NCTF	C35	CRT_DDC_DATA	Y37	VCC_NCTF
AT25	VSS_NCTF	C37	L_BKLT_EN	Y38	VCC_NCTF
AT27	VCCA_SM_CK_NCTF	C39	VSS	Y4	H_D#_34
AT28	VCCA_SM_CK_NCTF	C41	LVDSB_DATA_1	Y40	VCC
AT29	VCCA_SM_CK_NCTF	C43	VSS	Y41	VCC
AT31	VCCA_SM_CK_NCTF	C45	LVDSA_DATA#_3	Y44	VCC_PEG
AT32	VSS_NCTF	C47	VSS	Y46	PEG_TX#_9
AT34	VCC_NCTF	C49	VSS	Y48	VSS
AT35	VCC_NCTF	C5	VSS	Y50	PEG_RX#_8



Table 34. Intel GS45 Chipset Pinlist (Sheet 13 of 13)

Ball	Signal	Ball	Signal	Ball	Signal
AT37	VCC_NCTF	C51	VSS	Y52	PEG_TX_12
AT38	VCC_NCTF	C7	H_HIT#	Y54	PEG_TX#_12
AT4	SB_DQ_52	C9	H_BNR#	Y6	H_D#_44
AT40	VCC	D1	VSS_SCB	Y8	VSS
AT41	VCC	D10	TSATN#		
AT44	ME_JTAG_TDO	D12	H_A#_6		

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# 17 (G)MCH Register Description

## 17.1 Register Terminology

For general terminology, refer to the Terminology Section in volume 1.

Abbreviation	Definition
RO	<b>Read Only Bit(s).</b> Writes to these bits have no effect. This may be a status bit or a static value.
RS/WC	<b>Read Set/Write Clear Bit(s).</b> The first time the bit is read with an enabled byte, it returns the value 0, but a side-effect of the read is that the value changes to 1. Any subsequent reads with enabled bytes return a 1 until a 1 is written to the bit. When the bit is read, but the byte is not enabled, the state of the bit does not change, and the value returned is irrelevant, but will match the state of the bit. When a 0 is written to the bit, there is no effect. When a 1 is written to the bit, its value becomes 0, until the next byte-enabled read. When the bit is written, but the byte is not enabled, there is no effect.
R/W	<b>Read/Write Bit(s).</b> These bits can be read and written by software. Hardware may only change the state of this bit by reset.
R/WC	<b>Read/Write Clear Bit(s).</b> These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/WC/S	<b>Read/Write Clear/Sticky Bit(s).</b> These bits can be read. Internal events may set this bit. A software write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express* related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).
R/W/B	<b>Read/Write/Blind Bit(s).</b> These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit.
R/W/K	<b>Read/Write/Key Bit(s).</b> These bits can be read and written by software. Additionally this bit, when set, prohibits some other bit field(s) from being writeable (bit fields become Read Only).
R/W/L	<b>Read/Write/Lockable Bit(s).</b> These bits can be read and written by software. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/L/K	<b>Read/Write/Lockable/Key Bit(s).</b> These bits can be read and written by software. Additionally this bit is a Key bit that, when set, prohibits this bit field and/or some other specified bit fields from being writeable (bit fields become Read Only).
R/W/S	<b>Read/Write/Sticky Bit(s).</b> These bits can be read and written by software. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).



Abbreviation	Definition
R/WSC	<b>Read/Write Self Clear Bit(s).</b> These bits can be read and written by software. When the bit is 1, hardware may clear the bit to 0 based upon internal events, possibly sooner than any subsequent software read could retrieve a 1.
R/WSC/L	<b>Read/Write Self Clear/Lockable Bit(s).</b> These bits can be read and written by software. When the bit is 1, hardware may clear the bit to 0 based upon internal events, possibly sooner than any subsequent software read could retrieve a 1. Additionally there is a bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WO	<b>Write Once Bit(s).</b> Once written by software, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	<b>Write Only.</b> These bits may be written by software, but will always return zeros when read. They are used for write side-effects. Any data written to these registers cannot be retrieved.

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# 18 (G)MCH Configuration Process and Registers

## 18.1 Platform Configuration Structure

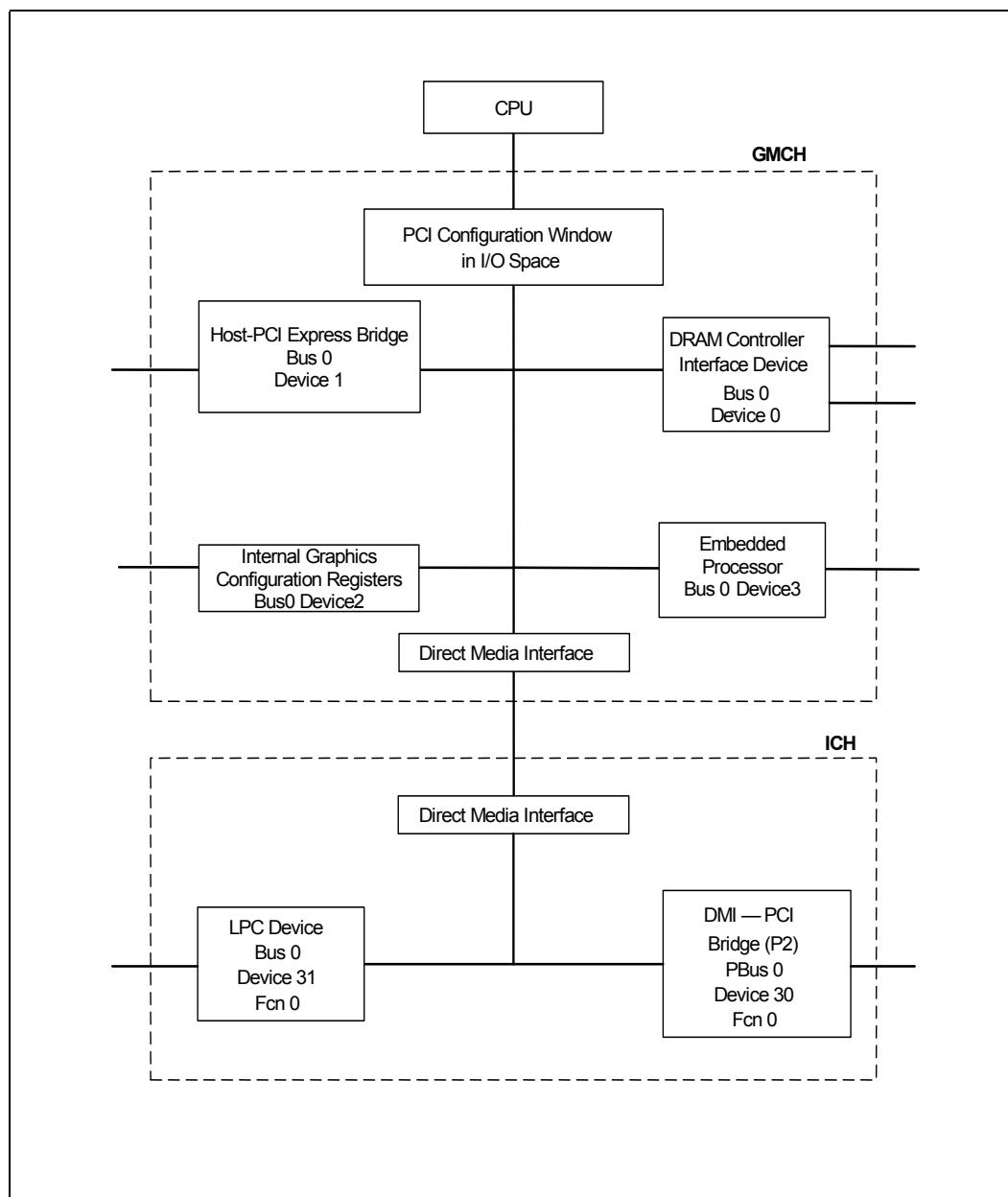
From a configuration standpoint, the DMI is logically PCI Bus 0. As a result, all devices internal to the (G)MCH and the ICH appear to be on PCI Bus 0. The system's primary PCI expansion bus is physically attached to the ICH and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI bus number. The PCI Express X16 graphics attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI Bus 0.

**Note:** A physical PCI Bus 0 does not exist. DMI and the internal devices in the (G)MCH and ICH logically constitute PCI Bus 0 to configuration software. This is shown in [Figure 1](#).

The (G)MCH contains the following PCI devices. The Configuration Registers for these devices are mapped as devices residing on PCI Bus 0.

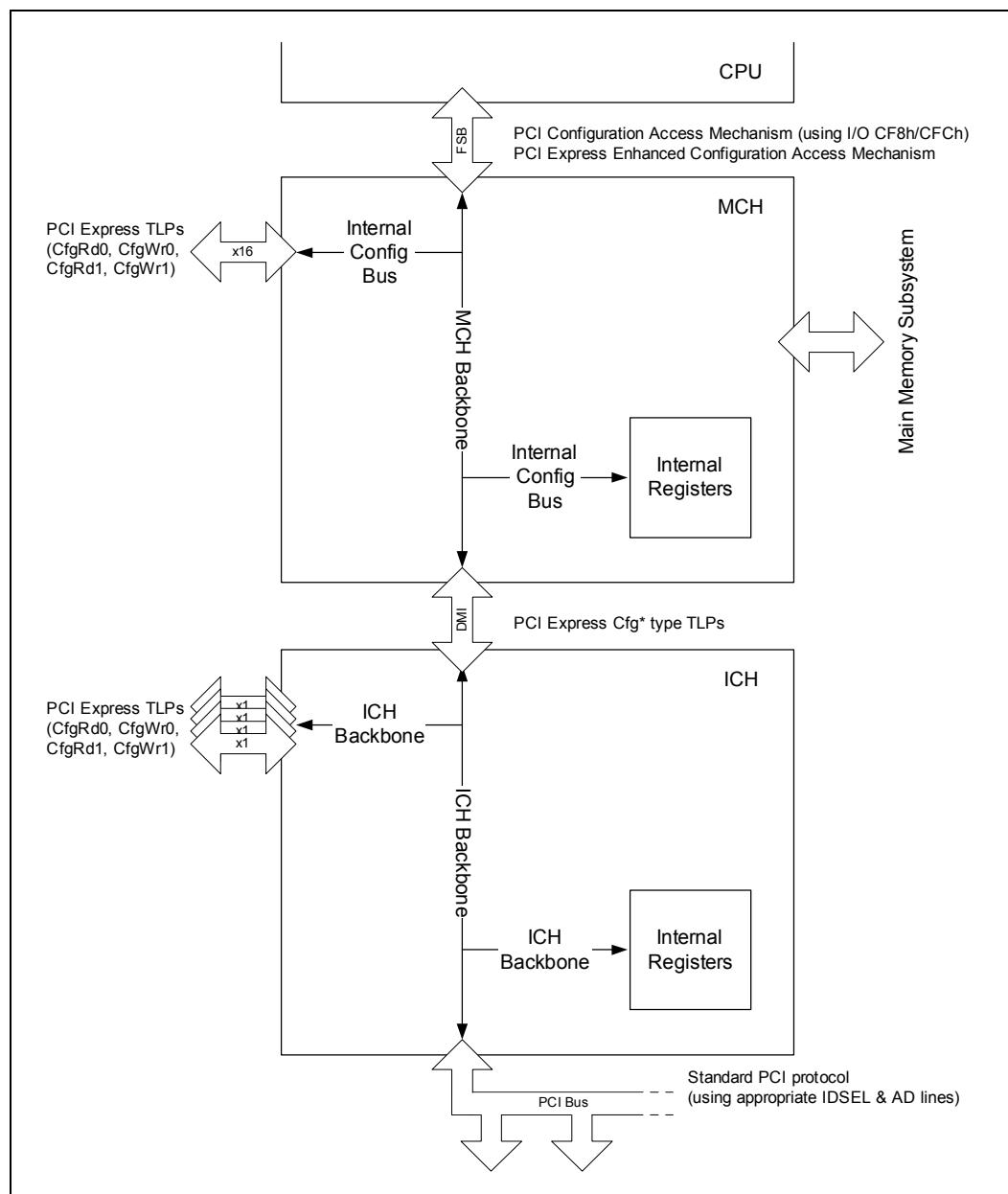
- **Device 0:** Host Bridge/DRAM Controller. Logically this appears as a PCI device residing on PCI Bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), configuration for the DMI, and other (G)MCH-specific registers.
- **Device 1:** Host-PCI Express Bridge. Logically, this appears as a “virtual” PCI-to-PCI bridge residing on PCI Bus 0 and is compliant with *PCI Express Specification*, Rev. 1.0. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 2:** Internal Graphics Control. Logically, this appears as a PCI device residing on PCI Bus 0. Physically, Device 2 contains the configuration registers for 3D, 2D, and display functions.
- **Device 3:** Internal Embedded Processor. This is the management engine built-in to Mobile Intel 4 Series Express Chipsets for supporting embedded function beyond the host system. It will appear on the PCI configuration bus as a new device.

**Figure 1. Conceptual Platform PCI Configuration Diagram**



## 18.2 Configuration Mechanisms

The CPU is the originator of configuration cycles so the FSB is the only interface in the platform where these configuration mechanisms are used. Internal to the (G)MCH transactions received through both configuration mechanisms are translated to the same format.

**Figure 2. Chipset Configuration Paths and Transaction Types**



### 18.2.1 Standard PCI Configuration Mechanism

A detailed description of the mechanism for translating CPU I/O bus cycles to configuration cycles is described below.

The PCI specification defines a slot-based configuration space that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the CPU. Configuration space is supported by a mapping mechanism implemented within the (G)MCH.

The configuration access mechanism makes use of the CONFIG\_ADDRESS Register (at I/O address 0CF8h through 0CFBh) and CONFIG\_DATA Register (at I/O address 0CFCh through 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG\_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of the device function being accessed. CONFIG\_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG\_DATA then becomes a window into the 4 bytes of configuration space specified by the contents of CONFIG\_ADDRESS. Any read or write to CONFIG\_DATA will result in the (G)MCH translating the CONFIG\_ADDRESS into the appropriate configuration cycle.

The (G)MCH is responsible for translating and routing the CPU's I/O accesses to the CONFIG\_ADDRESS and CONFIG\_DATA Registers to internal (G)MCH Configuration Registers, DMI or PCI Express.

### 18.2.2 Logical PCI Bus 0 Configuration Mechanism

The (G)MCH decodes the Bus Number (Bits 23:16) and the Device Number fields of the CONFIG\_ADDRESS Register. If the Bus Number field of CONFIG\_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device. The Host-DMI Bridge entity within the (G)MCH is hardwired as Device 0 on PCI Bus 0. The Host-PCI Express Bridge entity within the (G)MCH is hardwired as Device 1 on PCI Bus 0. Device 2 contains the control registers for the Integrated Graphics Controller. The ICH decodes the Type 0 access and generates a configuration access to the selected internal device.

### 18.2.3 Primary PCI and Downstream Configuration Mechanism

If the bus number in the CONFIG\_ADDRESS is non-zero, and falls outside the range claimed by the Host-PCI Express bridge (not between the upper bound of the bridge device's Subordinate Bus Number Register and the lower bound of the bridge device's Secondary Bus Number Register), the (G)MCH will generate a Type 1 DMI configuration Cycle. A [1:0] of the DMI request packet for the Type 1 configuration cycle will be "01". Bits 31:2 of the CONFIG\_ADDRESS Register will be translated to the A [31:2] field of the DMI request packet of the configuration cycle as shown below. This DMI configuration cycle will be sent over the DMI.

If the cycle is forwarded to the ICH via the DMI, the ICH compares the non-zero bus number with the Secondary Bus Number and Subordinate Bus Number Registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH's devices, the DMI, or a downstream PCI bus.

**Figure 3. DMI Type 0 Configuration Address Translation**

CONFIG_ADDRESS													
3	2 2	2 2	1	1	1 1	1 1	8 7	2 1 0					
1	8 7	4 3	6 5	1 0					x	x			
DMI Type 0 Configuration Address Extension													
3	2 2	2 2	1 1	1 1	8 7	2 1 0							
1	8 7	4 3	6 5	1 0					0	0			
CONFIG_ADDRESS													
3	2 2	2 2	1 1	1 1	8 7	2 1 0							
1	8 7	4 3	6 5	1 0					x	x			
DMI Type 1 Configuration Address Extension													
3	2 2	2 2	1 1	1 1	8 7	2 1 0							
1	8 7	4 3	6 5	1 0					0	1			
Reserved				Bus Number		Device Number		Function		Register Number		0	1

#### 18.2.4 PCI Express\* Enhanced Configuration Mechanism

PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by *PCI Specification Revision 2.3*. PCI Express configuration space is divided into a PCI 2.3-compatible region, which consists of the first 256 bytes of a logical device's configuration space and a PCI Express extended region which consists of the remaining configuration space.

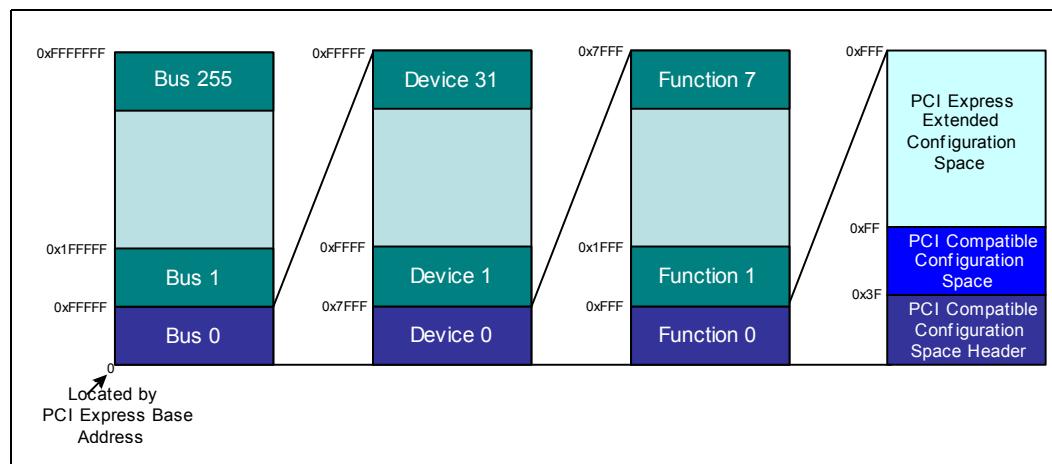
The PCI-compatible region can be accessed using either the mechanism defined in the previous Standard PCI Configuration Mechanism or using the PCI Express Enhanced Configuration Mechanism described in this section. The extended configuration registers may only be accessed using the PCI Express Enhanced Configuration Mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the dword to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The PCI Express enhanced configuration mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. There is a register, PCIEXBAR, which defines the base address for the block of addresses below top 4 GB for the configuration space associated with buses, devices and functions that are potentially a

part of the PCI Express root complex hierarchy. In the PCIEXBAR register there exist controls to limit the size of this reserved memory mapped space. 256 MB is the amount of address space required to reserve space for every bus, device, and function that could possibly exist. Options for 128 MB and 64 MB exist in order to free up those addresses for other uses. In these cases, the number of buses and all of their associated devices and functions are limited to 128 or 64 buses, respectively.

The PCI Express configuration transaction header includes an additional 4 bits (ExtendedRegisterAddress[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all zeros.

**Figure 4. Memory Map to PCI Express Device Configuration Space**



As with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

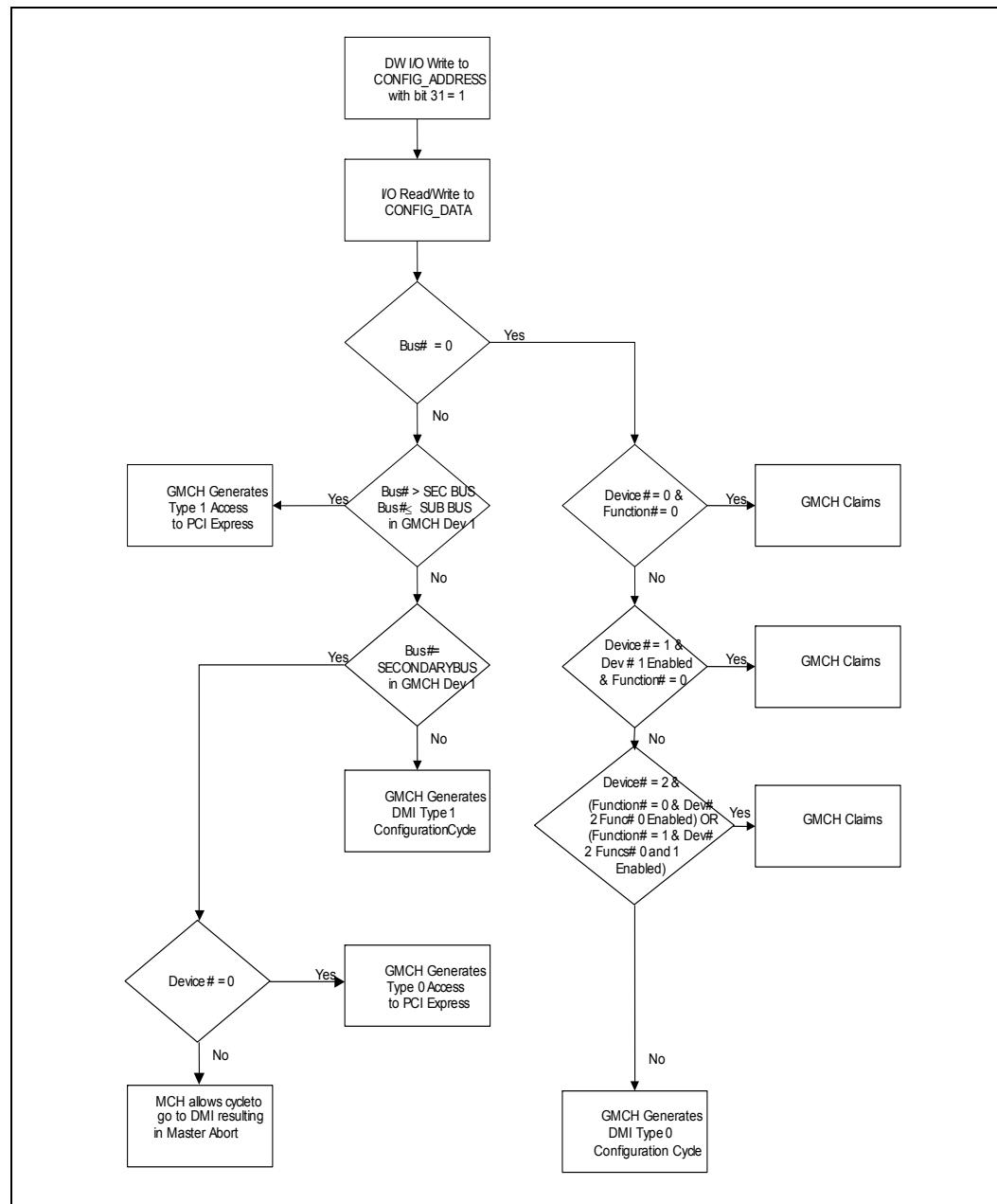
To access this space (steps 1, 2, 3 are done only once by BIOS):

1. Use the PCI-compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to Bit 0 of the PCIEXBAR register.
2. Use the PCI-compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register.
3. Calculate the host address of the register you wish to set using (PCI Express Base + (bus number x 1 MB) + (device number x 32 KB) + (function number x 4 KB) + (1 B x offset within the function) = host address).
4. Use a memory write or memory read cycle to the calculated host address to write or read that register.

## 18.3 Routing Configuration Accesses

The (G)MCH supports two PCI related interfaces: DMI and PCI Express Graphics. The (G)MCH is responsible for routing PCI and PCI Express configuration cycles to the appropriate device that is an integrated part of the (G)MCH or to one of these two interfaces. Configuration cycles to the ICH internal devices and Primary PCI (including downstream devices) are routed to the ICH via DMI. Configuration cycles to both the PCI Express Graphics PCI-compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port device or associated link.

**Figure 5.** (G)MCH Configuration Cycle Flowchart





### 18.3.1 Internal Device Configuration Accesses

The (G)MCH decodes the Bus Number (Bits 23:16) and the Device Number fields of the CONFIG\_ADDRESS register. If the Bus Number field of CONFIG\_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device.

If the targeted PCI Bus 0 device exists in the (G)MCH and is not disabled, the configuration cycle is claimed by the appropriate device.

### 18.3.2 Bridge Related Configuration Accesses

Configuration accesses on PCI Express graphics or DMI are PCI Express Configuration TLPs:

- Bus Number [7:0] is Header Byte 8 [7:0]
- Device Number [4:0] is Header Byte 9 [7:3]
- Function Number [2:0] is Header Byte 9 [2:0]

And special fields for this type of TLP:

- Extended Register Number [3:0] is Header Byte 10 [3:0]
- Register Number [5:0] is Header Byte 11 [7:2]

See the *PCI Express Specification* for more information on both the PCI 2.3-compatible and PCI Express Enhanced Configuration Mechanism and transaction rules.

#### 18.3.2.1 PCI Express Graphics Configuration Accesses

When the bus number of a Type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access matches the Device 1 Secondary Bus Number, a PCI Express Type 0 Configuration TLP is generated on the PCI Express graphics link targeting the device directly on the opposite side of the link. This should be Device 0 on the bus number assigned to the PCI Express graphics link (likely Bus 1).

The device on other side of link must be Device 0. The (G)MCH will Master Abort any Type 0 Configuration access to a non-zero device number. If there is to be more than one device on that side of the link there must be a bridge implemented in the downstream device.

When the bus number of a Type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access is within the claimed range (between the upper bound of the bridge device's Subordinate Bus Number Register and the lower bound of the bridge device's Secondary Bus Number Register) but doesn't match the Device 1 Secondary Bus Number, a PCI Express Type 1 Configuration TLP is generated on the secondary side of the PCI Express graphics link.

PCI Express Configuration Writes:

- Internally the host interface unit will translate writes to PCI Express extended configuration space to configuration writes on the backbone.
- Writes to extended space are posted on the FSB, but non-posted on the PCI Express graphics or DMI (i.e., translated to configuration writes).



### 18.3.2.2 DMI Configuration Accesses

Accesses to disabled (G)MCH internal devices, bus numbers not claimed by the Host-PCI Express graphics bridge, or PCI Bus 0 devices not part of the (G)MCH will subtractively decode to the ICH and consequently be forwarded over the DMI via a PCI Express configuration TLP.

If the bus number is zero, the (G)MCH will generate a Type 0 Configuration Cycle TLP on DMI. If the bus number is non-zero, and falls outside the range claimed by the Host-PCI Express graphics bridge, the (G)MCH will generate a Type 1 Configuration Cycle TLP on DMI.

The ICH routes configurations accesses in a manner similar to the (G)MCH. The ICH decodes the configuration TLP and generates a corresponding configuration access. Accesses targeting a device on PCI Bus 0 may be claimed by an internal device. The ICH compares the non-zero bus number with the Secondary Bus Number and Subordinate Bus Number Registers of its PCI-to-PCI bridges to determine if the configuration access is meant for Primary PCI, or some other downstream PCI bus or PCI Express link.

Configuration accesses that are forwarded to the ICH, but remain unclaimed by any device or bridge will result in a master abort.

### 18.3.2.3 Configuration Retry

For both PCI Express graphics and DMI, any configuration request (read or write) that receives a Configuration Request Retry Completion Status (CRS) will be reissued as a new transaction. The CRS terminates the original request TLP, but the (G)MCH will synthesize a subsequent request. The new configuration TLP which gets "reissued" due to CRS will have a new Sequence Number, but the TLP fields (tag, address, data, attributes, requestor ID, etc.) will be the same as the original TLP.

While this is happening, no completion will be sent to the originator of the configuration cycle (the CPU). A completion will not be sent to the CPU until the (G)MCH receives a successful completion, an Unsupported Request or Completer Abort completion, or the completion times out (if completion timeout is enabled).

This mechanism mimics the behavior on a legacy PCI bus, where any request that is retried will retry indefinitely.

No devices in the ICH ever return CRS. The (G)MCH is the only root complex device that handles CRS. The ICH just forwards to the (G)MCH all completions independent of completion status.

## 18.4 (G)MCH Register Introduction

The (G)MCH internal registers (I/O Mapped, Configuration, and PCI Express Extended Configuration registers) are accessible by the Host CPU. The registers that reside within the lower 256 bytes of each device can be accessed as byte, word (16-bit), or dword (32-bit) quantities, with the exception of CONFIG\_ADDRESS which can only be accessed as a dword. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in dword (32-bit) quantities.

Some of the (G)MCH registers described in this section contain reserved bits. These bits are labeled "Reserved." Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the



values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, or write operation for the configuration address register.

In addition to reserved bits within a register, the (G)MCH contains address locations in the configuration space of the Host Bridge entity that are marked either "Reserved" or "Intel Reserved". The (G)MCH responds to accesses to Reserved address locations by completing the host cycle. When a Reserved register location is read, a zero value is returned. (Reserved registers can be 8, 16, or 32 bits in size). Writes to Reserved registers have no effect on the (G)MCH. Reads to Intel Reserved registers may return a non-zero value.

**Warning:** Registers that are marked as Intel Reserved must not be modified by system software. Writes to Intel Reserved registers may cause system failure.

Upon a Full Reset, the (G)MCH sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the (G)MCH registers accordingly.

## 18.5 I/O Mapped Registers

The (G)MCH contains two registers that reside in the CPU I/O address space – the configuration address (CONFIG\_ADDRESS) register and the configuration data (CONFIG\_DATA) register. The configuration address register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

### 18.5.1 CONFIG\_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a dword  
Size: 32 bits

CONFIG\_ADDRESS is a 32-bit register that can be accessed only as a dword. A byte or word reference will "pass through" the configuration address register and DMI onto the PCI\_A bus as an I/O cycle. The CONFIG\_ADDRESS register contains the bus number, device number, function number, and register number for which a subsequent configuration access is intended.



Bit	Access	Default Value	Description
31	R/W	0b	<b>Configuration Enable (CFGE):</b> When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
30:24	RO	00h	<b>Reserved</b>
23:16	R/W	00h	<p><b>Bus Number:</b> If the bus number is programmed to 00h, the target of the configuration cycle is a PCI Bus 0 agent. If this is the case and the (G)MCH is not the target (i.e., the device number is &gt;=3 and not equal to 7), then a DMI Type 0 configuration cycle is generated.</p> <p>If the bus number is non-zero, and does not fall within the ranges enumerated by Device 1's Secondary Bus Number or Subordinate Bus Number Register, then a DMI Type 1 configuration cycle is generated.</p> <p>If the bus number is non-zero and matches the value programmed into the Secondary Bus Number Register of Device 1, a Type 0 PCI configuration cycle will be generated on PCI Express graphics.</p> <p>If the bus number is non-zero, greater than the value in the Secondary Bus Number Register of Device 1 and less than or equal to the value programmed into the Subordinate Bus Number Register of Device 1 a Type 1 PCI configuration cycle will be generated on PCI Express graphics.</p> <p>This field is mapped to Byte 8 [7:0] of the request header format during PCI Express* configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.</p>
15:11	R/W	00h	<p><b>Device Number:</b> This field selects one agent on the PCI bus selected by the bus number. When the bus number field is 00 the (G)MCH decodes the Device Number field. The (G)MCH is always Device 0 for the Host bridge entity, Device 1 for the Host-PCI Express entity. Therefore, when the bus number equals 0 and the device number equals 0, 1, 2 or 7 the internal (G)MCH devices are selected.</p> <p>This field is mapped to Byte 6 [7:3] of the request header format during PCI Express and DMI configuration cycles.</p>
10:8	R/W	000b	<p><b>Function Number:</b> This field allows the configuration registers of a particular function in a multi-function device to be accessed. The (G)MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1.</p> <p>This field is mapped to Byte 6 [2:0] of the request header format during PCI Express and DMI configuration cycles.</p>
7:2	R/W	00h	<p><b>Register Number:</b> This field selects one register within a particular bus, device, and function as specified by the other fields in the Configuration Address Register.</p> <p>This field is mapped to Byte 7 [7:2] of the request header format during PCI Express and DMI configuration cycles.</p>
1:0	RO	00b	<b>Reserved</b>



## 18.5.2 CONFIG\_DATA—Configuration Data Register

I/O Address: 0CFCh  
Size: 32 bits

CONFIG\_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG\_DATA is determined by the contents of CONFIG\_ADDRESS.

Bit	Access	Default Value	Description
31:0	R/W	0000 0000h	<b>Configuration Data Window (CDW):</b> If Bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

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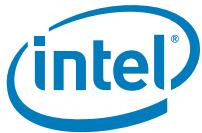
# 19 Host Bridge Device 0 Configuration Registers (D0:F0)

**Caution:** Address locations that are not listed are considered Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

## 19.1 Device 0 Configuration Registers

(Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	0	1	8086h	RO
Device Identification	DID	2	3	2A40h	RO
PCI Command	PCICMD	4	5	0006h	RO; R/W
PCI Status	PCISTS	6	7	0090h	RO; R/WC
Revision Identification	RID	8	8	00h	RO
Class Code	CC	9	B	060000h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HDR	E	E	00h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	E0h	RO
Egress Port Base Address	EPBAR	40	47	000000000 0000000h	RO; R/W/L; R/W
(G)MCH Memory Mapped Register Range Base	MCHBAR	48	4F	000000000 0000000h	RO; R/W/L; R/W
(G)MCH Graphics Control Register (Device 0)	GGC	52	53	0030h	RO; R/W/L
Device Enable	DEVEN	54	57	000043DBh	RO; R/W/L
PCI Express Register Range Base Address	PCIEXBAR	60	67	00000000E 0000000h	RO; R/W/L; R/W
MCH-ICH Serial Interconnect Ingress Root Complex	DMIBAR	68	6F	000000000 0000000h	RO; R/W/L; R/W
Reserved		70	8F		
Programmable Attribute Map 0	PAM0	90	90	00h	RO; R/W/L
Programmable Attribute Map 1	PAM1	91	91	00h	RO; R/W/L
Programmable Attribute Map 2	PAM2	92	92	00h	RO; R/W/L
Programmable Attribute Map 3	PAM3	93	93	00h	RO; R/W/L
Programmable Attribute Map 4	PAM4	94	94	00h	RO; R/W/L



(Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Programmable Attribute Map 5	PAM5	95	95	00h	RO; R/W/L
Programmable Attribute Map 6	PAM6	96	96	00h	RO; R/W/L
Legacy Access Control	LAC	97	97	00h	RO; R/W/L
Remap Base Address Register	REMAPBASE	98	99	03FFh	RO; R/W/L
Remap Limit Address Register	REMAPLIMIT	9A	9B	0000h	RO; R/W/L
System Management RAM Control	SMRAM	9D	9D	02h	RO; R/W/L; R/W
Extended System Management RAM Control	ESMRAMC	9E	9E	38h	RO; R/W/L; R/WC
Top of Memory	TOM	A0	A1	0001h	RO; R/W/L
Top of Upper Usable DRAM	TOUUID	A2	A3	0000h	R/W/L
Top of Low Used DRAM Register	TOLUD	B0	B1	0010h	RO; R/W/L
Error Status	ERRSTS	C8	C9	0000h	RO; R/WC/S
Error Command	ERRCMD	CA	CB	0000h	RO; R/W
Reserved		CC	CF		
Scratchpad Data	SKPD	DC	DF	00000000h	
Capability Identifier	CAPID0	E0	E9	000000000 000010A00 09h	
Reserved		F0	FF		

**NOTES:**

- Since the MCH Device 0 does not physically reside on PCI\_A many of the bits are not implemented.

### 19.1.1 VID - Vendor Identification

B/D/F/Type: 0/0/0/PCI  
Address Offset: 0-1h  
Default Value: 8086h  
Access: RO  
Size: 16 bits

This register combined with the Device Identification Register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	<b>Vendor Identification Number (VID):</b> PCI standard identification for Intel.



## 19.1.2 DID - Device Identification

B/D/F/Type:	0/0/0/PCI
Address Offset:	2-3h
Default Value:	2A40h
Access:	RO
Size:	16 bits

This register combined with the Vendor Identification Register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	2A40h	<b>Device Identification Number (DID):</b> Identifier assigned to the (G)MCH core/primary PCI device.

## 19.1.3 PCICMD - PCI Command

B/D/F/Type:	0/0/0/PCI
Address Offset:	4-5h
Default Value:	0006h
Access:	RO; R/W
Size:	16 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:10	RO	00h	<b>Reserved</b>
9	RO	0b	<b>Fast Back-to-Back Enable (FB2B):</b> Since Device 0 is strictly a target, this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect.
8	R/W	0b	<b>SERR Enable (SERRE):</b> Global enable bit for Device 0 SERR messaging. The MCH does not have an SERR signal. The MCH communicates the SERR condition by sending an SERR message over MCH ICH Serial Interface (DMI) to the ICH. If this bit is set to a 1, the MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. If SERRE is clear, then the SERR message is not generated by the MCH for Device 0. Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring on their respective devices. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO	0b	<b>Address/Data Stepping Enable (ADSTEP):</b> Address/data stepping is not implemented in the MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	RO	0b	<b>Parity Error Enable (PERRE):</b> PERRB is not implemented by the MCH and this bit is hardwired to 0. Writes to this bit position have no effect.



(Sheet 2 of 2)

Bit	Access	Default Value	Description
5	RO	0b	<b>VGA Palette Snoop Enable (VGASNOOP):</b> The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	RO	0b	<b>Memory Write and Invalidate Enable (MWIE):</b> The MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	RO	0b	<b>Special Cycle Enable (SCE):</b> The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	RO	1b	<b>Bus Master Enable (BME):</b> The MCH is always enabled as a master on DMI. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	RO	1b	<b>Memory Access Enable (MAE):</b> The MCH always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	RO	0b	<b>I/O Access Enable (IOAE):</b> This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.

#### 19.1.4 PCISTS - PCI Status

B/D/F/Type: 0/0/0/PCI  
Address Offset: 6-7h  
Default Value: 0090h  
Access: RO; R/WC  
Size: 16 bits

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Bit	Access	Default Value	Description
15	RO	0b	<b>Detected Parity Error (DPE):</b> The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	R/WC	0b	<b>Signaled System Error (SSE):</b> This bit is set to 1 when the MCH Device 0 generates an SERR message over DMI for any enabled Device 0 error condition or Device 0 error conditions are enabled in the PCICMD and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS or ERRSTS registers. Software clears this bit by writing a 1 to it.
13	R/WC	0b	<b>Received Unsupported Request (RURS):</b> This bit is set when the MCH generates a DMI request that receives an unsupported request completion. Software clears this bit by writing a 1 to it.
12	R/WC	0b	<b>Received Completion Abort Status (RCAS):</b> This bit is set when the MCH generates a DMI request that receives a completion abort. Software clears this bit by writing a 1 to it.



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Bit	Access	Default Value	Description
11	RO	0b	<b>Signaled Target Abort Status (STAS):</b> The MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	RO	00b	<b>DEVSEL Timing (DEVT):</b> These bits are hardwired to "00". Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the MCH.
8	RO	0b	<b>Master Data Parity Error Detected (DPD):</b> PERR signaling and messaging are not implemented by the MCH therefore this bit is hardwired to 0. Writes to this bit position have no effect.
7	RO	1b	<b>Fast Back-to-Back (FB2B):</b> This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the MCH.
6:5	RO	00b	<b>Reserved</b>
4	RO	1b	<b>Capability List (CLIST):</b> This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the AGP capability standard register resides.
3:0	RO	0h	<b>Reserved</b>



### 19.1.5 RID - Revision Identification

B/D/F/Type:	0/0/0/PCI
Address Offset:	8h
Default Value:	00h
Access:	RO
Size:	8 bits

RID Definition: This register contains the revision number of the (G)MCH Device 0. Following PCI Reset, the SRID value is selected to be read. When a write occurs to this register, the write data is compared to the hardwired RID Select Key Value, which is 69h. If the data matches this key, a flag is set that enables the CRID value to be read through this register.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the MCH Device 0. 07h: B-3 stepping

### 19.1.6 CC - Class Code

B/D/F/Type:	0/0/0/PCI
Address Offset:	9-Bh
Default Value:	060000h
Access:	RO
Size:	24 bits

Bit	Access	Default Value	Description
23:16	RO	06h	<b>Base Class Code (BCC):</b> This is an 8-bit value that indicates the base class code for the MCH. This code has the value 06h, indicating a bridge device.
15:8	RO	00h	<b>Sub-Class Code (SUBCC):</b> This is an 8-bit value that indicates the category of bridge into which the MCH falls. The code is 00h indicating a host bridge.
7:0	RO	00h	<b>Programming Interface (PI):</b> This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.



### 19.1.7 MLT - Master Latency Timer

B/D/F/Type:	0/0/0/PCI
Address Offset:	Dh
Default Value:	00h
Access:	RO
Size:	8 bits

Device 0 in the MCH is not a PCI master. Therefore this register is not implemented.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Reserved</b>

### 19.1.8 HDR - Header Type

B/D/F/Type:	0/0/0/PCI
Address Offset:	Eh
Default Value:	00h
Access:	RO
Size:	8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

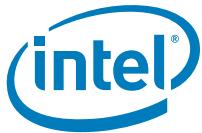
Bit	Access	Default Value	Description
7:0	RO	00h	<b>PCI Header (HDR):</b> This field always returns 0 to indicate that the MCH is a single-function device with standard header layout. Reads and writes to this location have no effect.

### 19.1.9 SVID - Subsystem Vendor Identification

B/D/F/Type:	0/0/0/PCI
Address Offset:	2C-2Dh
Default Value:	0000h
Access:	R/WO
Size:	16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access	Default Value	Description
15:0	R/WO	0000h	<b>Subsystem Vendor ID (SUBVID):</b> This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.



### 19.1.10 SID - Subsystem Identification

B/D/F/Type:	0/0/0/PCI
Address Offset:	2E-2Fh
Default Value:	0000h
Access:	R/WO
Size:	16 bits

This value is used to identify a particular subsystem.

Bit	Access	Default Value	Description
15:0	R/WO	0000h	<b>Subsystem ID (SUBID):</b> This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

### 19.1.11 CAPPTR - Capabilities Pointer

B/D/F/Type:	0/0/0/PCI
Address Offset:	34h
Default Value:	E0h
Access:	RO
Size:	8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access	Default Value	Description
7:0	RO	E0h	<b>Pointer to the Offset of the First Capability ID Register Block:</b> In this case the first capability is the product-specific Capability Identifier (CAPID0).



### 19.1.12 EPBAR - Egress Port Base Address

B/D/F/Type:	0/0/0/PCI
Address Offset:	40-47h
Default Value:	0000000000000000h
Access:	R/W/L; RO; R/W
Size:	64 bits

This is the base address for the Egress Port Root Complex MMIO configuration space. This window of addresses contains the Egress Port Root Complex Register set for the PCI Express Hierarchy associated with the MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 3.0-compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to EPBAREN [Bit 0 of this register].

All the bits in this register are Intel TXT locked. In Intel TXT mode, R/W bits are RO.

Bit	Access	Default Value	Description
63:36	R/W	0000000h	Reserved
35:12	R/W/L	000000h	<b>Egress Port RCRB Base Address:</b> This field corresponds to bits 35 to 12 of the base address Egress port RCRB MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the Egress Port RCRB and associated registers.
11:1	RO	000h	<b>Reserved</b>
0	R/W/L	0b	<b>EPBAR Enable (EPBAREN):</b> 0 = EPBAR is disabled and does not claim memory. 1 = EPBAR memory mapped accesses are claimed and decoded appropriately.



### 19.1.13 MCHBAR - (G)MCH Memory Mapped Register Range Base

B/D/F/Type:	0/0/0/PCI
Address Offset:	48-4Fh
Default Value:	0000000000000000h
Access:	R/W/L; RO; R/W
Size:	64 bits

This is the base address for the MCH MMIO configuration space. There is no physical memory within this 16-KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 3.0 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to MCHBAREN [Dev0, offset 54h, bit 28].

All the bits in this register are Intel TXT locked. In Intel TXT mode, R/W bits are RO.

Bit	Access	Default Value	Description
63:36	R/W	0000000h	<b>Reserved</b>
35:14	R/W/L	000000h	<b>(G)MCH Memory Map Base Address:</b> This field corresponds to Bits 35 to 14 of the base address MCHBAR configuration space. BIOS will program this register resulting in a base address for a 16-KB block of contiguous memory address space. This register ensures that a naturally aligned 16-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the MCH register set.
13:1	RO	0000h	<b>Reserved</b>
0	R/W/L	0b	<b>MCHBAR Enable (MCHBAREN):</b> 0 = MCHBAR is disabled and does not claim any memory. 1 = MCHBAR memory mapped accesses are claimed and decoded appropriately.



### 19.1.14 GGC - (G)MCH Graphics Control Register (Device 0)

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 52-53h  
 Default Value: 0030h  
 Access: RO; R/W/L  
 Size: 16 bits

All the bits in this register are Intel TXT locked. In Intel TXT mode, R/W bits are RO.

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Bit	Access	Default Value	Description
15:12	RO	0h	<b>Reserved</b>
11:8	R/W/L	0h	<p>GSM Memory Size (GGMS): This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will drive the base of GSM from DSM only using the GSM size programmed in the register.</p> <p>0000 = No memory pre-allocated. GTT cycles (Mem and IO) are not decoded.</p> <p>0001 = No Intel® Virtualization Technology (Intel® VT) mode, 1 MB of memory pre-allocated for GTT.</p> <p>0011 = No Intel VT mode, 2 MB of memory pre-allocated for GTT.</p> <p>1001 = Intel VT mode, 2 MB of memory pre-allocated for 1 MB of Global GTT and 1 MB Shadow GTT.</p> <p>1010 = Intel VT mode, 3 MB of memory pre-allocated for 1.5 MB of Global GTT and 1.5 MB Shadow GTT.</p> <p>1011 = Intel VT mode, 4 MB of memory pre-allocated for 2 MB of Global GTT and 2 MB Shadow GTT. If Intel VT for Directed I/O (Intel® VT-d) is disabled, then only "No Intel VT mode" values (0001 &amp; 0011) will take effect and setting this register to "Intel VT mode. values" (1001, 1010 &amp; 1011) will have the same effect as with 0000 value.</p> <p><b>NOTE:</b> All unspecified encodings of this register field are reserved, hardware functionality is not guaranteed if used. This register is locked and becomes Read Only when the D_LCK bit in SMRAM register is set.</p>



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Bit	Access	Default Value	Description
7:4	R/W/L	0011b	<p><b>Graphics Mode Select (GMS):</b> This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>0000: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80.</p> <p>0001 = Reserved.</p> <p>0010 = Reserved.</p> <p>0011 = Reserved.</p> <p>0100 = Reserved.</p> <p>0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer.</p> <p>0110 = Reserved.</p> <p>0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer.</p> <p>1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer.</p> <p>1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer.</p> <p>1010 = DVMT (UMA) mode, 96 MB of memory pre-allocated for frame buffer.</p> <p>1011 = DVMT (UMA) mode, 160 MB of memory pre-allocated for frame buffer.</p> <p>1100 = DVMT (UMA) mode, 224 MB of memory pre-allocated for frame buffer.</p> <p>1101 = DVMT (UMA) mode, 352 MB of memory pre-allocated for frame buffer.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"><li>1. This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. This register is also Intel® TXT lockable.</li><li>2. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.</li><li>3. BIOS Requirement: BIOS must not set this field to 0000 if IVD (Bit 1 of this register) is 0.</li></ol>
3:2	RO	00b	<b>Reserved</b>
1	R/W/L	0b	<p><b>IGD VGA Disable (IVD):</b></p> <p>0 = Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code Register is 00.</p> <p>1 = Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code Register is 80.</p>
0	RO	0b	<b>Reserved</b>



### 19.1.15 DEVEN - Device Enable

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 54-57h  
 Default Value: 000043DBh  
 Access: RO; R/W/L  
 Size: 32 bits

Allows for enabling/disabling of PCI devices and functions that are within the MCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

All the bits in this register are Intel TXT locked. In Intel TXT mode, R/W bits are RO.

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b>
15	R/W/L	0b	<b>Reserved</b>
14	R/W/L	1b	<b>Reserved</b>
13	RO	0b	<b>Reserved</b>
12:11	RO	00b	<b>Reserved</b>
10	RO	0b	<b>Reserved</b>
9:6	R/W/L	1b	<b>Reserved</b>
5	RO	0b	<b>Reserved</b>
4	R/W/L	1b	<b>Internal Graphics Engine Function 1 (D2F1EN):</b> 0 = Bus 0 Device 2 Function 1 is disabled and hidden. 1 = Bus 0 Device 2 Function 1 is enabled and visible. If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden, independent of the state of this bit.
3	R/W/L	1b	<b>Internal Graphics Engine Function 0 (D2F0EN):</b> 0 = Bus 0 Device 2 Function 0 is disabled and hidden. 1 = Bus 0 Device 2 Function 0 is enabled and visible. If this (G)MCH does not have internal graphics capability, then Device 2 Function 0 is disabled and hidden, independent of the state of this bit. If this function is disabled, then memory decoding for the Intel® TXT Trusted Graphics Registers at 0xFED305xx also needs to be disabled.
2	RO	0b	<b>Reserved</b>
1	R/W/L	1b	<b>PCI Express Graphics Port Enable (D1EN):</b> 0 = Bus 0 Device 1 Function 0 is disabled and hidden. 1 = Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by the device capabilities, SDVO presence HW strap and SDVO/PCI Express concurrent HW strap. Device 1 is Disabled on Reset if the SDVO present strap is sampled high and the SDVO/PCI Express concurrent strap is sampled low.
0	RO	1b	<b>Host Bridge:</b> Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.



### 19.1.16 PCIEXBAR - PCI Express Register Range Base Address

B/D/F/Type:	0/0/0/PCI
Address Offset:	60-67h
Default Value:	00000000E0000000h
Access:	R/W/L; RO; R/W
Size:	64 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the (G)MCH. There is not actual physical memory within this 256-MB window that can be addressed. Each PCI Express hierarchies requires a PCI Express BASE Register. The (G)MCH supports one PCI Express hierarchy.

The 256 MB reserved by this register does not alias to any PCI 2.3-compliant memory mapped space. For example MCHBAR reserves a 16-KB space and CHAPADR reserves a 4-KB space both outside of PCIEXBAR space. They cannot be overlayed on the space reserved by PCIEXBAR for Devices 0 and 7, respectively.

On reset, this register is disabled and must be enabled by writing a 1 to PCIXBAREN [Dev0, Offset 54h, Bit 31].

If the PCI Express Base Address [Bits 35:28] were set to Fh, an overlap with the High BIOS area, APIC and Intel TXT ranges would result. Software must guarantee that these ranges do not overlap. The PCI Express Base Address cannot be less than the maximum address written to the top of physical memory register (TOLUD). If a system is populated with more than 3.5 GB, either the PCI Express enhanced access mechanism must be disabled or the value in TOLUD must be reduced to report that only 3.5 GB are present in the system to allow a value of Eh for the PCI Express Base Address (assuming that all PCI 2.3-compatible configuration space fits above 3.75 GB).

All the bits in this register are Intel TXT locked. In Intel TXT mode, R/W bits are RO.



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Bit	Access	Default Value	Description
63:36	R/W	0000000h	<b>Reserved</b>
35:28	R/W/L	00001110b	<p><b>PCI Express* Base Address:</b> This field corresponds to bits 35 to 28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by Bits 3:1 of this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register), above TOLUD and still within total 36-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows:</p> <p>PCI Express Base Address + Bus Number x 1 MB + Device Number x 32 KB + Function Number x4 KB The address used to access the PCI Express configuration space for Device 1 in this component would be PCI Express Base Address + 0 x 1 MB + 1 x 32 KB + 0 x 4 KB = PCI Express Base Address + 32 KB. Remember that this address is the beginning of the 4-KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space. All the bits in this register are locked in Intel® TXT mode.</p>
27	R/W/L	0b	<b>128-MB Address Mask:</b> This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
26	R/W/L	0b	<b>64-MB Base Address Mask:</b> This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of Bits 2:1 in this register.
25:3	RO	000000h	<b>Reserved</b>



## (Sheet 2 of 2)

Bit	Access	Default Value	Description
2:1	R/W/L	00b	<b>Length:</b> This field describes the length of this region - Enhanced Configuration Space Region/Buses Decoded 00 = 256 MB (Buses 0-255). Bits 31:28 are decoded in the PCI Express Base Address field. 01 = 128 MB (Buses 0-127). Bits 31:27 are decoded in the PCI Express Base Address field. 10 = 64 MB (Buses 0-63). Bits 31:26 are decoded in the PCI Express Base Address field. 11 = Reserved
0	R/W/L	0b	<b>PCIEXBAR Enable (PCIEXBAREN):</b> 0 = PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR Register Bits 31:28 are R/W with no functionality behind them. 1 = The PCIEXBAR register is enabled. Memory read and write transactions whose Address Bits 31:28 match PCIEXBAR 31:28 will be translated to configuration reads and writes within the (G)MCH. These translation cycles are routed as shown in the tables above.



### 19.1.17 DMIBAR - MCH-ICH Serial Interconnect Ingress Root Complex

B/D/F/Type:	0/0/0/PCI
Address Offset:	68-6Fh
Default Value:	0000000000000000h
Access:	R/W/L; RO; R/W
Size:	64 bits

This is the base address for the DMI Root Complex MMIO configuration space. This window of addresses contains the DMI Root Complex Register set for the PCI Express Hierarchy associated with the MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 3.0-compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to RCBAREN [Dev0, Offset 54h, Bit 29].

All the bits in this register are Intel TXT locked. In Intel TXT mode, R/W bits are RO.

Bit	Access	Default Value	Description
63:36	R/W	0000000h	<b>Reserved</b>
35:12	R/W/L	000000h	<b>DMI Root Complex MMIO Register Set Base Address:</b> This field corresponds to Bits 35 to 12 of the base address DMI RCRB MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the DMI RCRB registers.
11:1	RO	000h	<b>Reserved</b>
0	R/W/L	0b	<b>DMIBAR Enable (DMIBAREN):</b> 0 = DMIBAR is disabled and does not claim any memory. 1 = DMIBAR memory mapped accesses are claimed and decoded appropriately.



### 19.1.18 TCSBAR - Trusted Configuration Register Range Base Address

B/D/F/Type:	0/0/0/PCI
Address Offset:	80-87h
Default Value:	00000000E0000000h
Access:	R/W/L; RO
Size:	64 bits

This is the base address for the trusted configuration space. This window of addresses contains the 4 KB of configuration space for each device/function that can potentially be part of the PCI hierarchy associated with the (G)MCH. There is not actual physical memory within this 256-MB/128-MB/64-MB window that can be addressed. Each PCI Hierarchies requires a PCI Base register.

All the bits in this register are Intel TXT locked. In Intel TXT mode, R/W bits are RO.

Bit	Access	Default Value	Description
63:36	R/W/L	0000000h	<b>Reserved</b>
35:28	R/W/L	0Eh	<b>Trusted Configuration Base Address:</b> This field corresponds to Bits 63 to 28 of the base address for TCS configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by Bits 2:1 of Dev0 Offsetx60 (PCIEXBAR). This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register), above TOLUD and still within total 36-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows: TCS Base Address + Bus Number x 1 MB + Device Number x 32 KB + Function Number x 4 KB. Example: The address used to access the PCI configuration space for Device 1 in this component would be PCI Express Base Address + 0 x 1 MB + 1 x 32 KB + 0 x 4 KB = PCI Express Base Address + 32 KB. This address is the beginning of the 4-KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space. All the bits in this register are locked in Intel® TXT mode.
27	R/W/L	0b	<b>128-MB Address Mask:</b> This bit is either part of the TCS Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of Bits 2:1 of Dev 0 Offsetx60 (PCIEXBAR).
26	R/W/L	0b	<b>64-MB Address Mask:</b> This bit is either part of the TCS Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of Bits 2:1 of Dev 0 Offsetx60 (PCIEXBAR).
25:0	RO	0000000h	<b>Reserved</b>



### 19.1.19 PAM0 - Programmable Attribute Map 0

B/D/F/Type:	0/0/0/PCI
Address Offset:	90h
Default Value:	00h
Access:	RO; R/W/L
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h-0FFFFh.

The MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 640-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

- RE - Read Enable. When RE = 1, the CPU read accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI\_A.
- WE - Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI\_A.

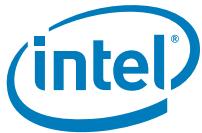
The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size. Accesses to the entire PAM region (000C\_0000h to 000F\_FFFFh) from DMI and PCI Express Graphics Attach Low Priority will be forwarded to main memory. The PAM read enable and write enable bits are not functional for these accesses. A full set of PAM decode/attribute logic is not being implemented. The MCH may hang if a PCI Express Graphics Attach or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM).

For these reasons the following critical restriction is placed on the programming of the PAM regions. At the time that a DMI or PCI Express Graphics Attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

All the bits in this register are Intel TXT locked. In Intel TXT mode, R/W bits are RO.

Bit	Access	Default Value	Description
7:6	RO	00b	<b>Reserved</b>
5:4	R/W/L	00b	<b>0F0000-0FFFF Attribute (HENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0F0000 to 0FFFF. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked in Intel® TXT mode. (RO in Intel TXT mode)
3:0	RO	0h	<b>Reserved</b>



### 19.1.20 PAM1 - Programmable Attribute Map 1

B/D/F/Type: 0/0/0/PCI  
Address Offset: 91h  
Default Value: 00h  
Access: RO; R/W/L  
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h-0C7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	<b>Reserved</b>
5:4	R/W/L	00b	<b>OC4000-0C7FFF Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0C4000 to 0C7FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.  This register is locked in Intel® TXT mode. (RO in Intel TXT mode)
3:2	RO	00b	<b>Reserved</b>
1:0	R/W/L	00b	<b>OC0000-0C3FFF Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0C0000 to 0C3FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.  This register is locked in Intel TXT mode. (RO in Intel TXT mode)



### 19.1.21 PAM2 - Programmable Attribute Map 2

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 92h  
 Default Value: 00h  
 Access: RO; R/W/L  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h-0CFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	<b>Reserved</b>
5:4	R/W/L	00b	<b>OCC000-0CFFFF Attribute (HIENABLE):</b> Reserved 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked in Intel® TXT mode. (RO in Intel TXT mode.)
3:2	RO	00b	<b>Reserved</b>
1:0	R/W/L	00b	<b>OC8000-0CBFFF Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0C8000 to 0CBFFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked in Intel TXT mode. (RO in Intel TXT mode.)



### 19.1.22 PAM3 - Programmable Attribute Map 3

B/D/F/Type: 0/0/0/PCI  
Address Offset: 93h  
Default Value: 00h  
Access: RO; R/W/L  
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h-0D7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	<b>Reserved</b>
5:4	R/W/L	00b	<b>OD4000-0D7FFF Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0D4000 to 0D7FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked in Intel® TXT mode. (RO in Intel TXT mode.)
3:2	RO	00b	<b>Reserved</b>
1:0	R/W/L	00b	<b>OD0000-0D3FFF Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0D0000 to 0D3FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked in Intel TXT mode. (RO in Intel TXT mode.)



### 19.1.23 PAM4 - Programmable Attribute Map 4

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 94h  
 Default Value: 00h  
 Access: RO; R/W/L  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h-0DFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	<b>Reserved</b>
5:4	R/W/L	00b	<p><b>0DC000-0DFFFF Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0DC000 to 0DFFFF.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.    01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.    10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.    11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> <p>This register is locked in Intel® TXT mode. (RO in Intel TXT mode.)</p>
3:2	RO	00b	<b>Reserved</b>
1:0	R/W/L	00b	<p><b>0D8000-0DBFFF Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0D8000 to 0DBFFF.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.    01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.    10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.    11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> <p>This register is locked in Intel TXT mode. (RO in Intel TXT mode.)</p>



### 19.1.24 PAM5 - Programmable Attribute Map 5

B/D/F/Type: 0/0/0/PCI  
Address Offset: 95h  
Default Value: 00h  
Access: RO; R/W/L  
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h-0E7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	<b>Reserved</b>
5:4	R/W/L	00b	<b>OE4000-0E7FFF Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.  This register is locked in Intel® TXT mode. (RO in Intel TXT mode.)
3:2	RO	00b	<b>Reserved</b>
1:0	R/W/L	00b	<b>OE0000-0E3FFF Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.  This register is locked in Intel TXT mode. (RO in Intel TXT mode.)



### 19.1.25 PAM6 - Programmable Attribute Map 6

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 96h  
 Default Value: 00h  
 Access: RO; R/W/L  
 Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h-0EFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	<b>Reserved</b>
5:4	R/W/L	00b	<p><b>0EC000-0EFFFF Attribute (HIENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0EC000 to 0EFFFF.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.    01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.    10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.    11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> <p>This register is locked in Intel® TXT mode. (RO in Intel TXT mode.)</p>
3:2	RO	00b	<b>Reserved</b>
1:0	R/W/L	00b	<p><b>0E8000-0EBFFF Attribute (LOENABLE):</b> This field controls the steering of read and write cycles that address the BIOS area from 0E8000 to 0EBFFF.</p> <p>00 = DRAM Disabled: Accesses are directed to DMI.    01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI.    10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI.    11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.</p> <p>This register is locked in Intel TXT mode. (RO in Intel TXT mode.)</p>



### 19.1.26 LAC - Legacy Access Control

B/D/F/Type: 0/0/0/PCI  
Address Offset: 97h  
Default Value: 00h  
Access: R/W/L; RO  
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15-16 MB.

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Bit	Access	Default Value	Description
7	R/W/L	0b	<b>Hole Enable (HEN):</b> This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0 = No memory hole. 1 = Memory hole from 15 MB to 16 MB. This register is locked in Intel® TXT mode. (RO in Intel TXT mode.)
6:1	RO	00h	<b>Reserved</b>



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Bit	Access	Default Value	Description															
0	R/W/L	0b	<p><b>MDA Present (MDAP):</b> This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if Device 1's VGA enable bit is not set. If Device 1's VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh are forwarded to DMI. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express graphics if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to DMI.</p> <p>MDA resources are defined as the following:</p> <p>Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh (Including ISA addresses aliases, A[15:10] are not used in decode).</p> <p>Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to DMI even if the reference includes I/O locations not listed above.</p> <p>The following table shows the behavior for all combinations of MDA and VGA:</p> <table border="1"> <thead> <tr> <th>VGAEN</th> <th>MDAP</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>All references to MDA and VGA space are routed to HI.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Illegal Combination</td> </tr> <tr> <td>1</td> <td>0</td> <td>All VGA and MDA references are routed to PCI Express Graphics Attach.</td> </tr> <tr> <td>1</td> <td>1</td> <td>All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to the HI. This register is locked in Intel® TXT mode. (RO in Intel TXT mode).</td> </tr> </tbody> </table>	VGAEN	MDAP	Description	0	0	All references to MDA and VGA space are routed to HI.	0	1	Illegal Combination	1	0	All VGA and MDA references are routed to PCI Express Graphics Attach.	1	1	All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to the HI. This register is locked in Intel® TXT mode. (RO in Intel TXT mode).
VGAEN	MDAP	Description																
0	0	All references to MDA and VGA space are routed to HI.																
0	1	Illegal Combination																
1	0	All VGA and MDA references are routed to PCI Express Graphics Attach.																
1	1	All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to the HI. This register is locked in Intel® TXT mode. (RO in Intel TXT mode).																



### 19.1.27 REMAPBASE - Remap Base Address Register

B/D/F/Type: 0/0/0/PCI  
Address Offset: 98-99h  
Default Value: 03FFh  
Access: RO; R/W/L  
Size: 16 bits

Bit	Access	Default Value	Description
15:10	RO	00h	<b>Reserved</b>
9:0	R/W/L	3FFh	<b>Remap Base Address[35:26]:</b> The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Base Address are assumed to be 0's. Thus the bottom of the defined memory range will be aligned to a 64-MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled. This field defaults to 3FFh. These bits are locked in Intel® TXT mode. They are also locked in Intel® Management Engine mode.

### 19.1.28 REMAPLIMIT - Remap Limit Address Register

B/D/F/Type: 0/0/0/PCI  
Address Offset: 9A-9Bh  
Default Value: 0000h  
Access: RO; R/W/L  
Size: 16 bits

Bit	Access	Default Value	Description
15:10	RO	00h	<b>Reserved</b>
9:0	R/W/L	000h	<b>Remap Limit Address [35:26]:</b> The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Limit Address are assumed to be F's. Thus the top of the defined range will be one less than a 64-MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled. This field defaults to 00h. These bits are locked in Intel® TXT mode. They are also locked in Intel® Management Engine mode.



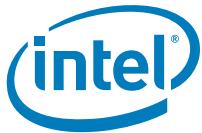
### 19.1.29 SMRAM - System Management RAM Control

B/D/F/Type: 0/0/0/PCI  
 Address Offset: 9Dh  
 Default Value: 02h  
 Access: RO; R/W/L; R/W  
 Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G\_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

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Bit	Access	Default Value	Description
7	RO	0b	<b>Reserved</b>
6	R/W/L	0b	<b>SMM Space Open (D_OPEN):</b> (When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. This register is locked in Intel® TXT mode (RO in Intel TXT mode). It also locks when D_LCK bit is set.)
5	R/W	0b	<b>SMM Space Closed (D_CLS):</b> When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. This register is locked in Intel TXT mode (RO in Intel TXT mode).
4	R/W/L	0b	<b>SMM Space Locked (D_LCK):</b> When D_LCK is set to a 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, G_SMRARE, C_BASE_SEG, H_SMRAM_EN, GMS, TOLUD, TOM, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.  This bit when set locks itself.
3	R/W/L	0b	<b>Global SMRAM Enable (G_SMRARE):</b> If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details.  This register is locked in Intel TXT mode (RO in Intel TXT mode). It also locks when D_LCK bit is set.



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Bit	Access	Default Value	Description
2:0	RO	010b	<b>Compatible SMM Space Base Segment (C_BASE_SEG):</b> This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the MCH supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.

### 19.1.30 ESMRAMC - Extended System Management RAM Control

B/D/F/Type: 0/0/0/PCI  
Address Offset: 9Eh  
Default Value: 38h  
Access: R/W/L; R/WC; RO  
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E\_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

**Note:** When Extended SMRAM is used, the maximum amount of DRAM accessible is limited to 256 MB.

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Bit	Access	Default Value	Description
7	R/W/L	0b	<b>Enable High SMRAM (H_SMRAME):</b> Controls the SMM memory space location (i.e., above 1 MB or below 1 MB). When G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range OFEDA0000h to OFEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh.  This register is locked in Intel® TXT mode (RO in Intel TXT mode). It also locks when D_LCK bit is set.
6	R/WC	0b	<b>Invalid SMRAM Access (E_SMERR):</b> This bit is set when CPU has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO	1b	<b>SMRAM Cacheable (SM_CACHE):</b> This bit is forced to 1 by the MCH.
4	RO	1b	<b>L1 Cache Enable for SMRAM (SM_L1):</b> This bit is forced to 1 by the MCH.
3	RO	1b	<b>L2 Cache Enable for SMRAM (SM_L2):</b> This bit is forced to 1 by the MCH.



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Bit	Access	Default Value	Description
2:1	R/W/L	00b	<p><b>TSEG Size (TSEG_SZ):</b> Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled.</p> <p>00 = 1 MB Tseg. (TOLUD:Graphics Stolen Memory Size - 1M) to (TOLUD - Graphics Stolen Memory Size).</p> <p>01 = 2 MB Tseg (TOLUD:Graphics Stolen Memory Size - 2M) to (TOLUD - Graphics Stolen Memory Size).</p> <p>10 = 8 MB Tseg (TOLUD:Graphics Stolen Memory Size - 8M) to (TOLUD - Graphics Stolen Memory Size).</p> <p>11 = Reserved.</p> <p>This register is locked in Intel TXT mode (RO in Intel TXT mode). It also locks when D_LCK bit is set.</p>
0	R/W/L	0b	<p><b>TSEG Enable (T_EN):</b> Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAWE =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space.</p> <p>This register is locked in Intel TXT mode (RO in Intel TXT mode). It also locks when D_LCK bit is set.</p>



### 19.1.31 TOM - Top of Memory

B/D/F/Type:	0/0/0/PCI
Address Offset:	A0-A1h
Default Value:	0001h
Access:	RO; R/W/L
Size:	16 bits

This register contains the size of physical memory. BIOS determines the memory size reported to the OS using this register.

All the bits in this register are locked in Intel TXT mode. They are also locked in Intel Management Engine mode.

Bit	Access	Default Value	Description
15:9	RO	00h	<b>Reserved</b>
8:0	R/W/L	001h	<b>Top of Memory:</b> This register reflects the total amount of populated physical memory. This is also the amount of addressable physical memory when remapping is used appropriate to ensure that no physical memory is wasted. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO). These bits correspond to address Bits 35:27 (128 MB granularity). Bits 26:0 are assumed to be 0. All the bits in this register are locked in Intel® TXT mode. They are also locked in Intel® Management Engine mode and when D_LCK bit is set in SMRAM register.



### 19.1.32 TOUUID - Top of Upper Usable DRAM

B/D/F/Type:	0/0/0/PCI
Address Offset:	A2-A3h
Default Value:	0000h
Access:	R/W/L
Size:	16 bits

Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 64-MB aligned since reclaim limit is 64-MB aligned. Address Bits 19:0 are assumed to be 0\_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4 GB. All the bits in this register are locked in Intel Management Engine mode and when D\_LCK bit is set in SMRAM register.

Bit	Access	Default Value	Description
15:0	R/W/L	0000h	<p><b>Top of Upper Usable DRAM (TOUUID):</b> This register contains Bits 35 to 20 of an address one byte above the maximum DRAM memory above 4 G that is usable by the operating system. Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 64-MB aligned since reclaim limit is 64-MB aligned. Address Bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4 GB.</p> <p>All the bits in this register are locked in Intel® TXT mode. They are also locked in Intel® Management Engine mode and when D_LCK bit is set in SMRAM register.</p>



### 19.1.33 TOLUD - Top of Low Used DRAM Register

B/D/F/Type:	0/0/0/PCI
Address Offset:	B0-B1h
Default Value:	0010h
Access:	R/W/L; RO
Size:	16 bits

This 16-bit register defines the Top of Low Usable DRAM. Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the Top of Low Usable DRAM, (G)MCH claims 1 to 64 MB of DRAM for internal graphics if enabled and 1, 2 or 8 MB of DRAM for TSEG if enabled. All the bits in this register are locked in Intel TXT mode. They are also locked in Intel Management Engine mode, or when D\_LCK bit is set in SMRAM register.

**Note:** Even if the OS does not need any PCI space, TOLUD can only be programmed to **FFh**. This ensures that addresses within 128 MB below 4 GB that are reserved for APIC and Intel TXT will not become accessible to applications.

Bit	Access	Default Value	Description
15:4	R/W/L	001h	<b>Top of Low Usable DRAM (TOLUD):</b> This register contains Bits 31 to 20 of an address one byte above the maximum DRAM memory below 4 GB that is usable by the operating system. Address Bits 31 down to 20 programmed to a "001h" implies a minimum memory size of 1 MB. Configuration software must set this value to the smaller of the following 2 choices: <ol style="list-style-type: none"><li>1. Maximum amount memory in the system minus Intel® Management Engine stolen memory plus 1 byte or</li><li>2. The minimum address allocated for PCI memory.</li></ol> Address Bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than that value programmed in this register. This register must not be set to 0000 0 b.  <b>NOTE:</b> The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and TSEG. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by TSEG size to determine the base of TSEG. All the bits in this register are locked in Intel® TXT mode. They are also locked in Intel Management Engine mode and when D_LCK bit is set in SMRAM register.  <b>NOTE:</b> This register MUST be 64-MB aligned when reclaim is enabled.
3:0	RO	0h	<b>Reserved</b>



### 19.1.34 ERRSTS - Error Status

B/D/F/Type:	0/0/0/PCI
Address Offset:	C8-C9h
Default Value:	0000h
Access:	RO; R/WC/S
Size:	16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. A SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

All the bits in this register are locked in Intel TXT mode. They are also locked in Intel Management Engine mode, or when D\_LCK bit is set in SMRAM register.

Bit	Access	Default Value	Description
15	RO	0b	<b>Reserved</b>
14	R/WC/S	0b	<b>Reserved</b>
13	R/WC/S	0b	<b>Reserved</b>
12	R/WC/S	0b	<b>(G)MCH Software Generated Event for SMI:</b> This indicates the source of the SMI was a Device 2 Software Event.
11	R/WC/S	0b	<b>(G)MCH Thermal Sensor Event for SMI/SCI/SERR:</b> Indicates that a (G)MCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.
10	RO	0b	<b>Reserved</b>
9	R/WC/S	0b	<b>LOCK to non-DRAM Memory Flag (LCKF):</b> When this bit is set to 1, the MCH has detected a lock operation to memory space that did not map into DRAM.
8	R/WC/S	0b	<b>Received Refresh Timeout Flag (RRTOF):</b> This bit is set when 1024 memory core refreshes are enqueued.
7	R/WC/S	0b	<b>DRAM Throttle Flag (DTF):</b> 0 = Software has cleared this flag since the most recent throttling event. 1 = Indicates that a DRAM Throttling condition occurred.
6:0	RO	00h	<b>Reserved</b>



### 19.1.35 ERRCMD - Error Command

B/D/F/Type: 0/0/0/PCI  
Address Offset: CA-CBh  
Default Value: 0000h  
Access: RO; R/W  
Size: 16 bits

This register controls the MCH responses to various system errors. Since the MCH does not have an SERRB signal, SERR messages are passed from the MCH to the ICH over DMI. When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Access	Default Value	Description
15:13	RO	000b	<b>Reserved</b>
12	RO	0b	<b>Reserved</b>
11	R/W	0b	<b>SERR on (G)MCH Thermal Sensor Event (TSESERR):</b> 0 = Reporting of this condition via SERR messaging is disabled. 1 = The MCH generates a SERR DMI special cycle when Bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event.
10	RO	0b	<b>Reserved</b>
9	R/W	0b	<b>SERR on LOCK to non-DRAM Memory (LCKERR):</b> 0 = Reporting of this condition via SERR messaging is disabled. 1 = The MCH will generate a DMI SERR special cycle whenever a CPU lock cycle is detected that does not hit DRAM.
8	R/W	0b	<b>SERR on DRAM Refresh Timeout (DRTOERR):</b> 0 = Reporting of this condition via SERR messaging is disabled. 1 = The (G)MCH generates an SERR DMI special cycle when a DRAM Refresh timeout occurs.
7	R/W	0b	<b>SERR on DRAM Throttle Condition (DTCERR):</b> 0 = Reporting of this condition via SERR messaging is disabled. 1 = The (G)MCH generates an SERR DMI special cycle when a DRAM Read or Write Throttle condition occurs.
6:0	RO	00h	<b>Reserved</b>



### 19.1.36 CAPID0 - Capability Identifier

B/D/F/Type: 0/0/0/PCI  
 Address Offset: E0-E9h  
 Default Value: 00000000000010A0009h  
 Access: RO  
 Size: 80 bits

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Bit	Access	Default Value	Description
79	RO	0b	<b>Integrated TPM Disable (ITPMDIS):</b> 0 = iTPM is enabled 1 = iTPM is disabled (delivered through Intel® Management Engine)
78	RO	0b	<b>Reserved</b>
77	RO	0b	<b>Reserved</b>
76	RO	0b	<b>Reserved</b>
75:73	RO	000b	<b>Reserved</b>
72	RO	0b	<b>Reserved</b>
71	RO	0b	<b>Reserved</b>
70	RO	0b	<b>Reserved</b>
69	RO	0b	<b>Reserved</b>
68	RO	0b	<b>Reserved</b>
67	RO	0b	<b>Reserved</b>
66	RO	0b	<b>Reserved</b>
65:62	RO	0000b	<b>Compatibility Device ID:</b> Identifier assigned to the (G)MCH core/primary PCI device.
61:58	RO	0111b	<b>Compatibility Revision ID:</b> This is a 4-bit value that indicates the revision identification number for the (G)MCH Device 0.
57	RO	0b	<b>Intel Management Engine / EP Disable:</b> 0 = Intel Management Engine Feature is enabled. 1 = Intel Management Engine Feature is disabled.
56	RO	0b	<b>All Intel® Active Management Technology (Intel® AMT) Disable:</b> 0 = Intel AMT Feature is enabled. 1 = Intel AMT Feature is disabled.
55	RO	0b	<b>Reserved</b>
54	RO	0b	<b>Reserved</b>
53	RO	0b	<b>Audio Disable:</b> 0 = (G)MCH is capable of audio. 1 = (G)MCH is not capable of audio.
52	RO	0b	<b>Reserved</b>
51	RO	0b	<b>Reserved</b>
50	RO	0b	<b>Reserved</b>



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Bit	Access	Default Value	Description
49	RO	0b	<b>DDR2 Capability:</b> 0 = (G)MCH is capable of supporting DDR2 SDRAM with 800 MHz and lower. 1 = (G)MCH is capable of supporting DDR2 SDRAM with 667 MHz and lower.
48	RO	0b	<b>Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Disable (VTDDIS):</b> Controls Intel VT-d capability. 0 = Intel VT-d is enabled 1 = Intel VT-d is disabled
47	RO	0b	<b>Reserved</b>
46	RO	0b	<b>Reserved</b>
45	RO	0b	<b>Reserved</b>
44:42	RO	000b	<b>GFX Software Capability ID:</b> Used to communicate (G)MCH variant information to the Graphics Driver software 111 = PM45 001 = GM45 011 = GL40 100 = GS45, GS40 Others = Reserved
41	RO	0b	<b>Reserved</b>
40	RO	0b	<b>Reserved</b>
39	RO	0b	<b>Reserved</b>
38	RO	0b	<b>Reserved</b>
37	RO	0b	<b>Chipset Intel® TXT Disable:</b> The purpose of Intel TXT Disable is to mask all Intel TXT functionality in the chipset. With Intel TXT disabled, the chipset will decode all cycles as in previous chipsets. 0 = Intel TXT behaviors are allowed. Graphics Intel TXT capability depends on separate Graphics Intel TXT Disable field. 1 = Intel TXT behaviors are not allowed, including graphics are not allowed. (Delivered through Intel Management Engine)
36:35	RO	00b	<b>Render Core Frequency Capability:</b> 01 = Capable of 533-MHz Core or lower 10 = Capable of 400-MHz Core or lower 11 = Capable of 333-MHz Core or lower 00 = Reserved
34	RO	0b	<b>Reserved</b>



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Bit	Access	Default Value	Description
33	RO	0b	<p><b>Internal Graphics Disable:</b></p> <p>0 = There is a graphics engine within this (G)MCH. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the (G)MCH. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Device 1 (if PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the (G)MCH Control Register). Graphics Memory is pre-allocated above TSEG Memory.</p> <p>1 = There is no graphics engine within this (G)MCH. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, All clocks to internal graphics logic are turned off. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Device 1. DEVEN [4:3] (Device 0, offset 54h) are forced to 00 have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.</p>
32	RO	0b	<p><b>PCI Express Port Disable:</b></p> <p>0 = There is a PCI Express GFX Attach on this (G)MCH. Device 1 and associated memory spaces are accessible. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Device 1 and VGA settings controlling internal graphics VGA if internal graphics is enabled.</p> <p>1 = There is no PCI Express GFX Attach on this (G)MCH. Device 1 and associated memory and IO spaces are disabled. In addition, Next_Pointer = 00h, VGA memory and IO cannot decode to the PCI Express interface. VGA memory and IO cannot decode to the PCI Express interface. From a Physical Layer perspective, all 16 lanes are powered down and the link does not attempt to train.</p>
31:30	RO	00b	<p><b>DDR3 Capability:</b></p> <p>00 = (G)MCH is capable of supporting DDR3 SDRAM with 1066 MHz and lower.</p> <p>01 = (G)MCH is capable of supporting DDR3 SDRAM with 800 MHz and lower.</p> <p>1x: (G)MCH is not capable of supporting DDR3 SDRAM.</p>



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Bit	Access	Default Value	Description
29:28	RO	00b	<b>FSB Capability:</b> This field controls which values are allowed in the FSB Frequency Select Field of the Clocking Configuration Register (MCHBAR Offset C00h). These values are determined by the BSEL[2:0] frequency straps. Any unsupported straps will render the (G)MCH host interface inoperable. <b>00 = Reserved</b> 01 = (G)MCH capable of up to FSB 1066 MHz 10 = (G)MCH capable of up to FSB 800 MHz 11 = (G)MCH capable of up to FSB 667 MHz
27:24	RO	1h	<b>CAPID Version:</b> This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO	0Ah	<b>CAPID Length:</b> This field has the value 0Ah to indicate the structure length (10 bytes).
15:8	RO	00h	<b>Next Capability Pointer:</b> This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO	09h	<b>CAP_ID:</b> This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

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# 20 Device 0 Memory Mapped I/O Register

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**Note:** All accesses to the Memory Mapped registers must be made as a single dword (4 bytes) or less. Access must be aligned on a natural boundary.

## 20.1 Device 0 Memory Mapped I/O Registers

A variety of timing and control registers have been moved to MMR space of Device 0 due to space constraints.

To simplify the read/write logic to the SRAM, BIOS is required to write and read 32-bit aligned dword. The SRAM includes a separate Write Enable for every dword.

The BIOS read/write cycles are performed in a memory mapped IO range that is setup for this purpose in the PCI configuration space, via standard PCI range scheme.

### 20.1.1 Device 0 MCHBAR Chipset Control Registers

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
MEREMAPBAR Memory Intel® Management Engine ReMap Memory Register Range Base Address	MEREMAPBAR	10	17	0000000000000000h	RO; R/W
GFXREMAPBAR Memory GFX ReMap Memory Register Range Base Address	GFXREMAPBAR	18	1F	0000000000000000h	RO; R/W
VC0REMAPBAR Memory VC0 ReMap Memory Register Range Base Address	VC0REMAPBAR	20	27	0000000000000000h	RO; R/W
VC1REMAPBAR Memory VC1 ReMap Memory Register Range Base Address	VC1REMAPBAR	28	2F	0000000000000000h	RO; R/W
Reserved		30	33		
PAVPC GMCH Graphics Protected Audio Video Path Control Register (Device 0)	PAVPC	34	37	00000000h	RO; R/W
Reserved		38	FA		



## 20.1.2 MEREMAPBAR - MEREMAPBAR Memory Intel® Management Engine REMAP Memory Register Range Base Address

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	10-17h
Default Value:	0000000000000000h
Access:	RO; R/W
Size:	64 bits

This is the base address for Intel Management Engine REMAP MMIO configuration space. This window of addresses contains the Intel Management Engine ReMap Register set. There is no physical memory within this 4-KB window that can be addressed. The 4-KB reserved by this register does not alias to any PCI 2.2-compliant memory mapped space.

The following BAR register will naturally get locked when MCHBAR gets locked. The access to this BAR registers is not allowed when Intel Management Engine is disabled or when Intel VT-d is disabled.

Bit	Access	Default Value	Description
63:12	R/W	0000000 000000h	<b>Intel® Management Engine REMAP MMIO Register Set Base Address:</b> This field corresponds to Bits 63 to 12 of the base address Intel Management Engine REMAP configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the DMA REMAP registers for Intel Management Engine. This register is locked based on Intel® VT-d capability (i.e., it becomes RO when Intel VT-d is disabled) or when Intel Management Engine is disabled.
11:1	RO	000h	<b>Reserved</b>
0	R/W	0b	<b>Intel Management Engine REMAP MMIO Space Enable (MEREMAPBAREN) (MEREMAPBAREN):</b> 0 = MEREMAPBAR is disabled and does not claim any memory. 1 = MEREMAPBAR memory mapped accesses are claimed and decoded appropriately. This register is locked based on Intel VT-d capability (i.e., it becomes RO when Intel VT-d is disabled) or when Intel Management Engine is disabled.



### 20.1.3 GFXREMAPBAR - GFXREMAPBAR Memory GFX ReMap Memory Register Range Base Address

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	18-1Fh
Default Value:	0000000000000000h
Access:	RO; R/W
Size:	64 bits

This is the base address for GFX ReMAP MMIO configuration space. This window of addresses contains the GFX ReMap Register set. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space.

The following BAR register will naturally lock when MCHBAR locks.

The accesses to this BAR registers are not allowed when IGD is disabled or when Intel VT-d is disabled.

Bit	Access	Default Value	Description
63:12	R/W	0000000 000000h	<p><b>GFX REMAP MMIO register set Base Address:</b> This field corresponds to Bits 63 to 12 of the base address GFX REMAP configuration space.</p> <p>BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB.</p> <p>System Software uses this base address to program the DMA REMAP registers for GFX.</p> <p>This register is locked based on Intel® VT-d capability (i.e., it becomes RO when Intel VT-d is disabled) or when IntGFX is disabled</p>
11:1	RO	000h	<b>Reserved</b>
0	R/W	0b	<p><b>GFX REMAP MMIO Space Enable (GFXREMAPBAREN):</b></p> <p>0 = GFXREMAPBAR is disabled and does not claim any memory.</p> <p>1 = GFXREMAPBAR memory mapped accesses are claimed and decoded appropriately.</p> <p>This register is locked based on Intel VT-d capability (i.e., it becomes RO when Intel VT-d is disabled) or when IntGFX is disabled.</p>



## 20.1.4 VC0REMAPBAR - VC0REMAPBAR Memory VC0 ReMap Memory Register Range Base Address

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	20-27h
Default Value:	0000000000000000h
Access:	RO; R/W
Size:	64 bits

This is the base address for PCI Express graphics and DMI VC0 ReMAP MMIO configuration space. This window of addresses contains the VC0 ReMap Register set. There is no physical memory within this 4-KB window that can be addressed. The 4-KB reserved by this register does not alias to any PCI 2.2-compliant memory mapped space.

This BAR's registers will naturally lock when MCHBAR gets locks.

Bit	Access	Default Value	Description
63:12	R/W	0000000 000000h	<b>VC0 REMAP MMIO register set Base Address:</b> This field corresponds to Bits 63 to 12 of the base address VC0 REMAP configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the DMA REMAP registers for VC0. This register is locked based on Intel® VT-d capability (i.e., it becomes RO when Intel VT-d is disabled).
11:1	RO	000h	<b>Reserved</b>
0	R/W	0b	<b>VC0 REMAP MMIO Space Enable (VCOREMAPBAREN):</b> 0 = VCOREMAPBAR is disabled and does not claim any memory. 1 = VCOREMAPBAR memory mapped accesses are claimed and decoded appropriately. This register is locked based on Intel VT-d capability (i.e., it becomes RO when Intel VT-d is disabled).



## 20.1.5 VC1REMAPBAR - VC1REMAPBAR Memory VC1 ReMap Memory Register Range Base Address

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 28-2Fh  
 Default Value: 0000000000000000h  
 Access: RO; R/W  
 Size: 64 bits

This is the base address for DMI VC1 ReMAP MMIO configuration space. This window of addresses contains the VC1 ReMap Register set. There is no physical memory within this 4-KB window that can be addressed. The 4-KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space.

This BAR's registers will naturally get locked when MCHBAR gets locked.

Bit	Access	Default Value	Description
63:12	R/W	0000000 000000h	<b>VC1 REMAP MMIO Register Set Base Address:</b> This field corresponds to Bits 63 to 12 of the base address VC1 REMAP configuration space.  BIOS will program this register resulting in a base address for a 4-B block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the DMA REMAP registers for VC1.  This register is locked based on Intel® VT-d capability (i.e., it becomes RO when Intel VT-d is disabled).
11:1	RO	000h	<b>Reserved</b>
0	R/W	0b	<b>VC1 REMAP MMIO Space Enable (VC1REMAPBAREN):</b> 0 = VC1REMAPBAR is disabled and does not claim any memory. 1 = VC1REMAPBAR memory mapped accesses are claimed and decoded appropriately.  This register is locked based on Intel VT-d capability (i.e., it becomes RO when Intel VT-d is disabled).



## 20.1.6 PAVPC - GMCH Graphics Protected Audio Video Path Control Register (Device 0)

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 34-37h  
Default Value: 00000000h  
Access: RO; R/W/L;  
Size: 32 bits

All the Bits in this register are LT locked. In LT mode R/W bits are RO.

Bit	Access	Default Value	Description
31:16	R/W/L	0000h	<b>Protected Content Memory Write Once Base (PCMWOBASE):</b> This field is used to set the base of the Write-Once Protected Content Memory space. This corresponds to bits 31:16 of the system memory address range, giving a 64-KB granularity. This value MUST be above PCMBASE and below the top of stolen memory. This register is locked (becomes read-only) when PAVPE = 1b.
15:4	R/W/L	000h	<b>Protected Content Memory Base (PCMBASE):</b> This field is used to set the base of Protected Content.Memory. This corresponds to bits 31:20 of the system memory address range, giving a 1-MB granularity. This value MUST be at least 8 MB above the base and below the top of stolen memory (unprotected VGA cycles can access 0-8 MB of stolen memory). This register is locked (becomes read-only) when PAVPE = 1b.
3	RO	0b	<b>Reserved</b>
2	RO	0b	<b>Protected Content Memory Write Once Status (PCMWOOST):</b> This field reflects the status of the Write Once PCM lock. It is set when the cyg_ci_wopcm internal signal is pulsed, and reset on a system reset.
1	R/W/L	0b	<b>Protected Audio Video Path Enable (PAVPE):</b> This field locks all of the bits in this register. 0 = PAVP path is disabled, and All PCM registers are R/W (except PCME, which may be held to 0b by a fuse). 1 = PAVP path is enabled, and All PCM registers are read-only (including PAVPE itself). This register is locked (becomes read-only) when PAVPE = 1b (i.e., it locks itself). This register is read-only (stays at 0b) when the PAVP fuse is set to "disabled".
0	R/W/L	0b	<b>Protected Content Memory Enable (PCME):</b> This field enables a Protected Content Memory within Graphics Stolen Memory. This register is locked (becomes read-only) when PAVPE = 1b. This register is read-only (stays at 0b) when the PAVP fuse is set to "disabled".



## 20.2 MCHBAR Arbitration

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
DRAM Channel Control	DCC	200	203	00000000h	RO; R/W; R/W/L
Reserved		204	243		

### 20.2.1 DCC - DRAM Channel Control

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 200-203h  
 Default Value: 00000000h  
 Access: RO; R/W; R/W/L  
 Size: 32 bits

This register controls how the DRAM channels work together. It affects how the CxDRB registers are interpreted and allows them to steer transactions to the correct channel.

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Bit	Access	Default Value	Description
31:29	RO	000b	<b>Reserved</b>
28:24	R/W	00h	<b>Reserved</b>
23	RO	0b	<b>Reserved</b>
22:21	R/W	00b	<b>Bank Select for EMRS Commands:</b> This field applies only when the Mode Select (SMS) bits = 100, implying an EMRS command. 00 = Bank 1 (BS[2:0] = 001), EMRS(1) 01 = Bank 2 (BS[2:0] = 010), EMRS(2) 10 = Bank 3 (BS[2:0] = 011), EMRS(3) 11 = Reserved
20	R/W	0b	<b>Independent Dual Channel IC/SMS Enable:</b> 0 = IC and SMS controls in DCC register control both system memory channels. 1 = IC and SMS bits in C0/1DRC0 register control each system memory channel independently.
19	R/W	0b	<b>Reserved</b>



## (Sheet 2 of 2)

Bit	Access	Default Value	Description
18:16	R/W	000b	<b>Mode Select (SMS):</b> These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. 000 = Post Reset state. When the MCH exits reset, the mode select field is cleared to "000". 001 = NOP Command Enable - All CPU cycles to DRAM result in a NOP command on the DRAM interface. 010 = All Banks Pre-charge Enable - All CPU cycles to DRAM result in an "all banks precharge" command on the DRAM interface. 011 = Mode Register Set Enable - All CPU cycles to DRAM result in a "mode register" set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. 100 = Extended Mode register set (EMRS) 101 = Initial ZQ calibration for DDR3 only 110 = CBR Refresh Enable: In this mode all CPU cycles to DRAM result in a CBR cycle on the DRAM interface 111 = Normal operation
15	R/W	0b	<b>SMS Exit Sequence Initiator:</b> SMS Exit Sequence Initiator 0 = SMS exit sequence handled by EP? 1 = BIOS initiates SMS exit sequence.
14:11	RO	0000b	<b>Reserved</b>
10	R/W/L	0b	<b>Channel XOR Randomization Disable (CXRDIS):</b> When enabled, the DRAM Controller will try to spread page accesses evenly among the channels by including more address bits in the choice for which channel holds the requested address. 0 = Channel XOR Randomization is enabled. 1 = Channel XOR Randomization is disabled
9	R/W/L	0b	<b>Reserved</b>
8:2	RO	0000000b	<b>Reserved</b>
1	R/W/L	0b	<b>DRAM Addressing Mode Control (DAMC):</b> 0 = Single-Channel/Dual-Channel Asymmetric 1 = Dual-Channel Interleaved
0	RO	0b	<b>Reserved</b>



## 20.3 Device 0 MCHBAR Clock Controls

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Clocking Configuration	CLKCFG	C00	C03	00040208h	RO; R/W
Reserved		C04	C17		
Sticky Scratchpad Data	SSKPD	C1C	C1D	0000h	R/W/S
Reserved		C20	C67		

### 20.3.1 CLKCFG - Clocking Configuration

B/D/F/Type: 0/0/0/MCHBAR CLK  
 Address Offset: C00-C03h  
 Default Value: 00040208h  
 Access: RO; R/W  
 Size: 32 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31	R/W	0b	<b>Reserved</b>
30	RO	0b	<b>Reserved</b>
29	RO	0b	<b>Reserved</b>
28	RO	0b	<b>Reserved</b>
27	R/W	0b	<b>Reserved</b>
26	RO	0b	<b>Reserved</b>
25:23	R/W	000b	<b>Reserved</b>
22	R/W	0b	<b>Reserved</b>
21	R/W	0b	<b>Reserved</b>
20:19	R/W	00b	<b>Reserved</b>
18	R/W	1b	<b>Reserved</b>
17	R/W	0b	<b>Reserved</b>
16:15	R/W	00b	<b>Reserved</b>
14	R/W	0b	<b>Reserved</b>
13	RO	0b	<b>Reserved</b>
12	R/W	0b	<b>Reserved</b>
11	R/W	0b	<b>Reserved</b>
10	R/W	0b	<b>Reserved</b>
9:8	R/W	10b	<b>Reserved</b>
7	R/W	0h	<b>Reserved</b>



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Bit	Access	Default Value	Description
6:4	R/W	000b	<b>Memory Frequency Select. (MEMFREQSEL):</b> The values here refer to DDR frequencies. 100 = 667 101 = 800 110 = 1066 Others: Reserved.
3	R/W	1b	<b>Reserved</b>
2:0	RO	000b	<b>PSB Frequency Select. (PSBFREQSEL):</b> 011 = FSB667 010 = FSB800 110 = FSB1066 Others = Reserved Attempts to strap values beyond the configurable limit will shut down the host PLL.

### 20.3.2 SSKPD - Sticky Scratchpad Data

B/D/F/Type: 0/0/0/MCHBAR CLK  
Address Offset: C1C-C1Dh  
Default Value: 0000h  
Access: R/W/S  
Size: 16 bits

This register holds 16 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers. This Register is reset on PWROK.

Bit	Access	Default Value	Description
15:0	R/W/S	0000h	<b>Scratchpad Data (SCRATCHPAD):</b> 1 WORD of data storage.



## 20.4 Device 0 MCHBAR ACPI Power Management Controls

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
C2 to C3 Transition Timer	C2C3TT	F00	F03	00000000h	RO; R/W
C3 to C4 Transition Timer	C3C4TT	F04	F07	00000000h	RO; R/W
Reserved		F08	F0E		
Power Management Configuration	PMCFG	F10	F10	02h	R/W
Self-Refresh Channel Status	SLFRCS	F14	F17	00000000h	RO; R/WC
Reserved		F20	FFF		

### 20.4.1 C2C3TT - C2 to C3 Transition Timer

B/D/F/Type: 0/0/0/MCHBAR PM  
 Address Offset: F00-F03h  
 Default Value: 00000000h  
 Access: RO; R/W  
 Size: 32 bits

Bit	Access	Default Value	Description
31:19	RO	0000h	<b>Reserved</b>
18:7	R/W	000h	<b>C2 to C3 Transition Timer (C2C3TT):</b> Dual purpose timer in 128-core clock granularity. Number of core clocks to wait between last snoop from PCI Express graphics or DMI to a Req_C3 DMI message being issued. Timer is activated only when the WAIT_C3 message from DMI has been received when in C2. 000 = 128 host clocks FFF = 524288 host clocks
6:0	RO	00h	<b>Reserved</b>



## 20.4.2 C3C4TT - C3 to C4 Transition Timer

B/D/F/Type: 0/0/0/MCHBAR PM  
Address Offset: F04-F07h  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

Bit	Access	Default Value	Description
31:19	RO	0000h	<b>Reserved</b>
18:7	R/W	000h	<b>C3 to C4 Transition Timer (C34TT):</b> 128 core clock granularity. Number of core clocks to wait between last snoop from PCI Express graphics or DMI to a Req_C4 DMI message being issued. Timer is activated only when the WAIT_C4 message from DMI has been received when in C3. 000 = 128 host clocks FFF = 524288 host clocks
6:0	RO	00h	<b>Reserved</b>

## 20.4.3 PMCFG - Power Management Configuration

B/D/F/Type: 0/0/0/MCHBAR PM  
Address Offset: F10h  
Default Value: 02h  
Access: R/W  
Size: 8 bits  
BIOS Optimal Default 0h

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.



#### 20.4.4 SLFRCS - Self-Refresh Channel Status

B/D/F/Type: 0/0/0/MCHBAR PM  
 Address Offset: F14-F17h  
 Default Value: 00000000h  
 Access: RO; R/WC  
 Size: 32 bits

This register is reset by PWROK only.

Bit	Access	Default Value	Description
31:2	RO	00000000h	<b>Reserved</b>
1	R/WC	0b	<p><b>Warm Reset Event Occurred (RST_EVNT):</b>  Set by power management hardware when a "RESET_WARN" message has been received on the DMI link.  Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence.  <b>Note:</b> In a non-Intel ME system, this bit will get cleared in a cold reset. In an Intel ME system, this bit will always retain its value.</p>
0	R/WC	0b	<p><b>Channels in Self-refresh:</b>  Set by power management hardware after both memory channels are placed in self refresh as a result of a Power State or a Reset Warn sequence,  Cleared by Power management hardware before starting self refresh exit sequence initiated by a power management exit.  Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence.  0 = Both Channels are not guaranteed to be in Self Refresh.  1 = Both Channels are in Self Refresh.</p>

### 20.5 Device 0 MCHBAR Thermal Management Controls

(Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		1000	1000		
Thermal Sensor Control 1	TSC1	1001	1002	0000h	R/W; R/W/L; R/WC
Thermal Sensor Status 1	TSS1	1004	1005	0000h	RO
Thermometer Read 1	TR1	1006	1006	FFh	RO
Thermometer Offset 1	TOF1	1007	1007	00h	R/W
Relative Thermometer Read 1	RTR1	1008	1008	00h	RO



## (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		100B	100E		
Thermal Sensor Temperature Trip Point A1	TSTTPA1	1010	1013	00000000h	RO; R/W/L; R/WO
Thermal Sensor Temperature Trip Point B1	TSTTPB1	1014	1017	00000000h	R/W/L
Thermal Calibration Offset 1	TCO1	1018	1018	00h	R/W/L
Reserved		101A	101B		
Hardware Throttle Control 1	HWTHROT CTRL1	101C	101C	00h	RO; R/W/L; R/WO
Reserved		101D	101D		
Thermal Interrupt Status 1	TIS1	101E	101F	0000h	R/WC
Reserved		1040	1040		
Thermal Sensor Control 2	TSC2	1041	1042	0000h	R/W; R/W/L; R/WC
Thermal Sensor Status 2	TSS2	1044	1045	0000h	RO
Thermometer Read 2	TR2	1046	1046	FFh	RO
Thermometer Offset 2	TOF2	1047	1047	00h	R/W
Relative Thermometer Read 2	RTR2	1048	1048	00h	RO
Reserved		104B	104E		
Thermal Sensor Temperature Trip Point A2	TSTTPA2	1050	1053	00000000h	RO; R/W/L; R/WO
Thermal Sensor Temperature Trip Point B2	TSTTPB2	1054	1057	00000000h	R/W/L
Thermal Calibration Offset 2	TCO2	1058	1058	00h	R/W/L
Reserved		105A	105B		
Hardware Throttle Control 2	HWTHROT CTRL2	105C	105C	00h	RO; R/W/L; R/WO
Reserved		105D	105D		
Thermal Interrupt Status 2	TIS2	105E	105F	0000h	R/WC
Thermometer Mode Enable and Rate	TERATE	1070	1070	00h	R/W
Thermal Sensor Rate Control	TSRCTRL	1080	1080	06h	R/W
In Use Bits	IUB	10E0	10E3	00000000h	RO; R/WC
Thermal Error Command	TERRCMD	10E4	10E4	00h	R/W
Thermal SMI Command	TSMICMD	10E5	10E5	00h	R/W
Thermal SCI Command	TSCICMD	10E6	10E6	00h	R/W
Thermal INTR Command	TINTRCMD	10E7	10E7	00h	R/W
External Thermal Sensor Control and Status	EXTTSCS	10EF	10EF	00h	RO; R/W/L; R/WO



## 20.5.1 TSC1 - Thermal Sensor Control 1

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1001-1002h
Default Value:	0000h
Access:	R/W; R/W/L; R/WC
Size:	16 bits
BIOS Optimal Default	00h

This register controls the operation of the internal thermal sensor located in the hot spot of graphics region.

Bit	Access	Default Value	Description
15	R/W/L	0b	<b>ThermalSensorenable (TSE):</b> This bit enables power to the thermal sensor. Lockable via TCO Bit 7. 0 = Disabled 1 = Enabled
14	R/W	0b	<b>Reserved</b>
13:10	R/W	0000b	<b>Digital Hysteresis Amount (DHA):</b> This bit determines whether no offset, 1 LSB, 2... 15 is used for hysteresis for the trip points. 0001 = 1 TR value added to each trip temperature when tripped 0010 = 2 TR values added to each trip temperature when tripped: 0110 = ~3.0 °C (Recommended setting) 1110 = 14 TR value added to each trip temperature when tripped 1111 = 15 TR values added to each trip temperature when tripped <b>NOTE:</b> TR = Temperature Read
9	R/W/L	0b	<b>Reserved</b>
8	R/WC	0b	<b>InUse (IU):</b> Software semaphore bit. After a full MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor. Software that reads this register but does not intend to claim exclusive access of the thermal sensor must write a one to this bit if it reads a 0, in order to allow other software threads to claim it. See also THERM Bit 15, which is an independent additional semaphore bit.
7:0	RO	0h	<b>Reserved</b>



## 20.5.2 TSS1 - Thermal Sensor Status 1

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1004-1005h
Default Value:	0000h
Access:	RO
Size:	16 bits
BIOS Optimal Default	00h

This read only register provides trip point and other status of the thermal sensor.

Bit	Access	Default Value	Description
15:11	RO	0h	<b>Reserved</b>
10	RO	0b	<b>ThermometerModeOutputValid:</b> A 1 indicates the Thermometer mode is able to converge to a temperature and that the TR register is reporting a reasonable estimate of the thermal sensor temperature. A 0 indicates the Thermometer mode is off, or that temperature is out of range, or that the TR register is being looked at before a temperature conversion has had time to complete.
9	RO	0b	<b>Reserved</b>
8	RO	0b	<b>Reserved</b>
7:6	RO	0h	<b>Reserved</b>
5	RO	0b	<b>CatastrophicTripIndicator (CTI):</b> A 1 indicates that the internal thermal sensor temperature is above the catastrophic setting.
4	RO	0b	<b>HotTripIndicator (HTI):</b> A 1 indicates that the internal thermal sensor temperature is above the Hot setting.
3	RO	0b	<b>Aux3TripIndicator (A3TI):</b> A 1 indicates that the internal thermal sensor temperature is above the Aux3 setting.
2	RO	0b	<b>Aux2TripIndicator (A2TI):</b> A 1 indicates that the internal thermal sensor temperature is above the Aux2 setting.
1	RO	0b	<b>Aux1TripIndicator (A1TI):</b> A 1 indicates that the internal thermal sensor temperature is above the Aux1 setting.
0	RO	0b	<b>Aux0TripIndicator (A0TI):</b> A 1 indicates that the internal thermal sensor temperature is above the Aux0 setting.



### 20.5.3 TR1 - Thermometer Read 1

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1006h
Default Value:	FFh
Access:	RO
Size:	8 bits

This register generally provides the calibrated current temperature from the thermometer circuit when the Thermometer mode is enabled. See the temperature tables for the temperature calculations.

Bit	Access	Default Value	Description
7:0	RO	FFh	<b>ThermometerReading (TR):</b> Provides the current counter value. The current counter value corresponds to thermal sensor temperature if TSS[Thermometer mode Output Valid] = 1. This register has a straight binary encoding that will range from 0 to FFh.

### 20.5.4 TOF1 - Thermometer Offset 1

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1007h
Default Value:	00h
Access:	R/W
Size:	8 bits

This register is used for programming the thermometer offset.

Bit	Access	Default Value	Description
7:0	R/W	00h	<b>Thermometeroffset (TOF):</b> This value is used to adjust the current thermometer reading so that the TR value is not relative to a specific trip or calibration point, and is positive going for positive increases in temperature. The initial default value is 00h and software must determine the correct temperature adjustment that corresponds to a zero reading by reading the fuses and referring to the temperature tables, and then programming the computed offset into this register.



## 20.5.5 RTR1 - Relative Thermometer Read 1

B/D/F/Type: 0/0/0/MCHBAR Thermal  
Address Offset: 1008h  
Default Value: 00h  
Access: RO  
Size: 8 bits

This register contains the relative temperature.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Relativethermometerreading (RTR1):</b> In Thermometer mode, this register reports the relative temperature of the thermal sensor. Provides a two's complement value of the thermal sensor relative to TOF. TR and HTPS can both vary between 0 and 255. But RTR will be clipped between 127 to keep it an 8-bit number. See also TSS[Thermometer mode Output Valid]. In the Analog mode, the RTR field reports HTPS value.

## 20.5.6 TSTTPA1 - Thermal Sensor Temperature Trip Point A1

B/D/F/Type: 0/0/0/MCHBAR Thermal  
Address Offset: 1010-1013h  
Default Value: 00000000h  
Access: RO; R/W/L; R/WO  
Size: 32 bits  
BIOS Optimal Default 00h

This register:

1. Sets the target values for some of the trip points in thermometer mode.
2. Reports the relative thermal sensor temperature. See also TSTTPB.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31	R/WO	0b	<b>Lock Bit forAux0, Aux1, Aux2 and Aux3 Trip Points (AUXLOCK):</b> This bit, when written to a 1, locks the Aux x Trip point settings. This lock is reversible. The reversing procedure is: following sequence must be done in order without any other configuration cycles in-between write tsttpa1 04C1C202 write tsttpa2 04C1C202 write tsttpa1 04C1C202 It is expected that the Aux x Trip point settings can be changed dynamically when this lock is not set.
30:24	RO	0h	<b>Reserved</b>



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Bit	Access	Default Value	Description
23:16	RO	00h	<b>Reserved</b>
15:8	R/W/L	00h	<b>Hot Trip Point Setting (HTPS):</b> Sets the target value for the Hot trip point. Lockable via TCO Bit 7.
7:0	R/W/L	00h	<b>Catastrophic Trip Point Setting (CTPS):</b> Sets the target for the Catastrophic trip point.

## 20.5.7 TSTTPB1 - Thermal Sensor Temperature Trip Point B1

B/D/F/Type: 0/0/0/MCHBAR Thermal  
 Address Offset: 1014-1017h  
 Default Value: 00000000h  
 Access: R/W/L  
 Size: 32 bits

This register sets the target values for some of the trip points in the Thermometer mode. See also TSTTPA1.

Bit	Access	Default Value	Description
31:24	R/W/L	00h	<b>Aux3Trippointsetting (A3TPS):</b> Sets the target value for the Aux3 trip point Lockable by TSTTPA1[31].
23:16	R/W/L	00h	<b>Aux2Trippointsetting (A2TPS):</b> Sets the target value for the Aux2 trip point Lockable by TSTTPA1[31].
15:8	R/W/L	00h	<b>Aux1Trippointsetting (A1TPS):</b> Sets the target value for the Aux1 trip point Lockable by TSTTPA1[31].
7:0	R/W/L	00h	<b>Aux0Trippointsetting (A0TPS):</b> Sets the target value for the Aux0 trip point Lockable by TSTTPA1[31].



## 20.5.8 TCO1 - Thermal Calibration Offset 1

B/D/F/Type: 0/0/0/MCHBAR Thermal  
Address Offset: 1018h  
Default Value: 00h  
Access: R/W/L  
Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	<b>LockbitforCatastrophic (LBC):</b> This bit, when written to a 1, locks the Catastrophic programming interface, including Bits 7:0 of TSTTPA[15-0], Bits 15 and 9 of TSC, and Bits 10 and 8 of TST1. This bit may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.
6:0	R/W/L	00h	<b>CalibrationOffset (CO):</b> This field contains the current calibration offset for the Thermal Sensor DAC inputs. The calibration offset is a two's complement signed number which is added to the temperature counter value to help generate the final value going to the thermal sensor DAC. This field is Read/Write and can be modified by Software unless locked by setting Bit 7 of this register. The fuses cannot be programmed via this register. Once this register has been overwritten by software, the values of the TCO fuses can be read using the Therm3 register. Note for TCO operation: While this is a 7-bit field, the 7th bit is sign extended to 9 bits for TCO operation. The range of 00h to 3fh corresponds to 0 0000 0000 to 0 0011 1111. The range of 41h to 7fh corresponds to 1 1100 001 (i.e., negative 3fh) to 1 1111 1111 (i.e., negative 1), respectively. If TST[Direct DAC Test Enable] = 1, the values in this field are sent directly to Bank B.



## 20.5.9 HWTHROTCTRL1 - Hardware Throttle Control 1

B/D/F/Type: 0/0/0/MCHBAR Thermal  
 Address Offset: 101Ch  
 Default Value: 00h  
 Access: RO; R/W/L; R/WO  
 Size: 8 bits

Bit	Access	Default Value	Description
7	R/W/L	0b	<b>Internal Thermal Hardware Throttling Enable bit (ITHTE):</b> This bit is a master enable for internal thermal sensor-based hardware throttling. 0 = Hardware actions via the internal thermal sensor are disabled. 1 = Hardware actions via the internal thermal sensor are enabled.
6:5	RO	00b	<b>Reserved:</b>
4	R/W/L	0b	<b>Throttling Zone Selection (Tzs):</b> This bit determines what temperature zones will enable autothrottling. This register applies to internal thermal sensor throttling. Lockable by Bit 0 of this register. See also the throttling registers in PCI config space Device 0 which is used to enable or disable throttling. 0 = Hot, Aux2, and Catastrophic. 1 = Hot and Catastrophic.
3	R/W/L	0b	<b>HaltonCatastrophic (HOC):</b> When this bit is set, THRMTripB is asserted on catastrophic trip to bring the platform down. A system reboot is required to bring the system out of a halt from the thermal sensor. Once the catastrophic trip point is reached, THRMTripB will stay asserted even if the catastrophic trip deasserts before the platform is shut down.
2	R/W/L	0b	<b>Reserved</b>
1	R/W/L	0b	<b>Reserved</b>
0	R/WO	0b	<b>Hardware Throttling Lock Bit (HTL):</b> This bit locks Bits 7:1 of this register. When this bit is set to a one, the register bits are locked. It may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.



## 20.5.10 TIS1 - Thermal Interrupt Status 1

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	101E-101Fh
Default Value:	0000h
Access:	R/WC
Size:	16 bits
BIOS Optimal Default	0h

This register is used to report which specific error condition resulted in the D2F0 or D2F1 ERRSTS[Thermal Sensor event for SMI/SCI/SERR] or memory mapped IIR Thermal Event. SW can examine the current state of the thermal zones by examining the TSS. Software can distinguish internal or external Trip Event by examining TSS.

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Bit	Access	Default Value	Description
15:14	RO	0h	<b>Reserved</b>
13	R/WC	0b	<b>WasCatastrophicThermalSensorInterruptEvent:</b> 0 = No trip for this event 1 = Indicates that a Catastrophic Thermal Sensor trip based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.
12	R/WC	0b	<b>WasHotThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that a Hot Thermal Sensor trip based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.
11	R/WC	0b	<b>WasAux3ThermalSensorInterruptEvent (A3TSIE):</b> 0 = No trip for this event. 1 = Indicates that an Aux3 Thermal Sensor trip based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.
10	R/WC	0b	<b>WasAux2ThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that an Aux2 Thermal Sensor trip based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.
9	R/WC	0b	<b>WasAux1ThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that an Aux1 Thermal Sensor trip based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.



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Bit	Access	Default Value	Description
8	R/WC	0b	<b>WasAux0ThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that an Aux0 Thermal Sensor trip based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.
7:6	RO	0h	<b>Reserved</b>
5	R/WC	0b	<b>CatastrophicThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that a Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit.
4	R/WC	0b	<b>HotThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point Software must write a 1 to clear this status bit.
3	R/WC	0b	<b>Aux3ThermalSensorInterruptEvent (A3TSIE):</b> 0 = No trip for this event. 1 = Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit.
2	R/WC	0b	<b>Aux2ThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit.
1	R/WC	0b	<b>Aux1ThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that an Aux1 Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit.



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Bit	Access	Default Value	Description
0	R/WC	0b	<b>Aux0ThermalSensorInterruptEvent:</b> 0 = No trip for this event. 1 = Indicates that an Aux0 Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit. The following scenario is possible: An interrupt is initiated on a rising temperature trip, the appropriate DMI cycles are generated, and eventually the software services the interrupt and sees a rising temperature trip as the cause in the status bits for the interrupts. Assume that the software then goes and clears the local interrupt status bit in the TIS register for that trip event. It is possible at this point that a falling temperature trip event occurs before the software has had the time to clear the global interrupts status bit. But since software has already looked at the status register before this event happened, software may not clear the local status flag for this event. Therefore, after the global interrupt is cleared by S/W, S/W must look at the instantaneous status in the TSS register.

### 20.5.11 TSC2 - Thermal Sensor Control 2

B/D/F/Type: 0/0/0/MCHBAR Thermal  
Address Offset: 1041-1042h  
Default Value: 0000h  
Access: R/W; R/W/L; R/WC  
Size: 16 bits  
BIOS Optimal Default 00h

This register controls the operation of the internal thermal sensor located in the memory hot spot.

Bit settings for this register are identical to TSC1.

### 20.5.12 TSS2 - Thermal Sensor Status 2

B/D/F/Type: 0/0/0/MCHBAR Thermal  
Address Offset: 1044-1045h  
Default Value: 0000h  
Access: RO  
Size: 16 bits  
BIOS Optimal Default 00h

This read only register provides trip point and other status of the thermal sensor.

Bit settings for this register are identical to TSS1.



### 20.5.13 TOF2 - Thermometer Offset 2

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1047h
Default Value:	00h
Access:	R/W
Size:	8 bits

This register is used to program the thermometer offset.

Bit settings for this register are identical to TOF1.

### 20.5.14 RTR2 - Relative Thermometer Read 2

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1048h
Default Value:	00h
Access:	RO
Size:	8 bits

This register contains the relative temperature.

Bit settings for this register are identical to RTR1.

### 20.5.15 TR2 - Thermometer Read 2

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1046h
Default Value:	FFh
Access:	RO
Size:	8 bits

This register generally provides the calibrated current temperature from the thermometer circuit when the Thermometer mode is enabled. See the temperature tables for the temperature calculations.

Bit settings for this register are identical to TR1.

### 20.5.16 TSTTPA2 - Thermal Sensor Temperature Trip Point A2

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1050-1053h
Default Value:	00000000h
Access:	RO; R/W/L; R/WO
Size:	32 bits
BIOS Optimal Default	00h
This register:	

1. Sets the target values for some of the trip points in thermometer mode.
2. Reports the relative thermal sensor temperature See also TSTTPB. Bit settings for this register are identical to TSTTPA1.



### 20.5.17 TSTTPB2 - Thermal Sensor Temperature Trip Point B2

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1054-1057h
Default Value:	00000000h
Access:	R/W/L
Size:	32 bits

This register sets the target values for some of the trip points in the Thermometer mode. See also TSTTPA.

Bit settings for this register are identical to TSTTPB1.

### 20.5.18 TCO2 - Thermal Calibration Offset 2

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1058h
Default Value:	00h
Access:	R/W/L
Size:	8 bits

Bit settings for this register are identical to TCO1.

### 20.5.19 HWTHROTCTRL2 - Hardware Throttle Control 2

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	105Ch
Default Value:	00h
Access:	RO; R/W/L; R/WO
Size:	8 bits

Bit settings for this register are identical to HWTHROTCTRL1.

### 20.5.20 TIS2 - Thermal Interrupt Status 2

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	105E-105Fh
Default Value:	0000h
Access:	R/WC
Size:	16 bits
BIOS Optimal Default	0h

This register is used to report which specific error condition resulted in the D2F0 or D2F1 ERRSTS[Thermal Sensor event for SMI/SCI/SERR] or memory mapped IIR Thermal Event. SW can examine the current state of the thermal zones by examining the TSS. Software can distinguish internal or external Trip Event by examining TSS.

Bit settings for this register are identical to TIS1.



### 20.5.21 TERATE - Thermometer Mode Enable and Rate

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1070h
Default Value:	00h
Access:	R/W
Size:	8 bits
BIOS Optimal Default	0h

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

### 20.5.22 TSRCTRL - Thermal Sensor Rate Control

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	1080h
Default Value:	06h
Access:	R/W
Size:	8 bits
BIOS Optimal Default	0h

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.

### 20.5.23 IUB - In Use Bits

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	10E0-10E3h
Default Value:	00000000h
Access:	RO; R/WC
Size:	32 bits

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Bit	Access	Default Value	Description
31:25	RO	00h	<b>Reserved</b>
24	R/WC	0b	<b>InUseBit3 (IU3):</b> Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the resource. When finished with the resource, software must write a 1 to this bit to clear the semaphore.
23:17	RO	00h	<b>Reserved</b>



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Bit	Access	Default Value	Description
16	R/WC	0b	<b>InUseBit2 (IU2):</b> Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. <ul style="list-style-type: none"><li>• A write of a 1 to this bit will reset the next read value to 0.</li><li>• Writing a 0 to this bit has no effect.</li></ul> Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the resource. When finished with the resource, software must write a 1 to this bit to clear the semaphore.
15:9	RO	00h	<b>Reserved</b>
8	R/WC	0b	<b>InUseBit1 (IU1):</b> Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. <ul style="list-style-type: none"><li>• A write of a 1 to this bit will reset the next read value to 0.</li><li>• Writing a 0 to this bit has no effect.</li></ul> Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the resource. When finished with the resource, software must write a 1 to this bit to clear the semaphore.
7:1	RO	00h	<b>Reserved</b>
0	R/WC	0b	<b>InUseBit0 (IU0):</b> Software semaphore bit. After a full (G)MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. <ul style="list-style-type: none"><li>• A write of a 1 to this bit will reset the next read value to 0.</li><li>• Writing a 0 to this bit has no effect.</li></ul> Software can poll this bit until it reads a 0, and will then own the usage of the resource with which software associates it. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the resource. When finished with the resource, software must write a 1 to this bit to clear the semaphore.



## 20.5.24 TERRCMD - Thermal Error Command

B/D/F/Type:	0/0/0/MCHBAR Thermal
Address Offset:	10E4h
Default Value:	00h
Access:	R/W
Size:	8 bits
BIOS Optimal Default	0h

This register select which errors are generate a SERR DMI interface special cycle, as enabled by ERRCMD [SERR Thermal Sensor event].The SERR and SCI must not be enabled at the same time for the thermal sensor event.

Bit	Access	Default Value	Description
7:6	RO	0h	<b>Reserved</b>
5	R/W	0b	<b>SERRonCatastrophicThermalSensorEvent:</b> 0 = Disable. Reporting of this condition via SERR messaging is disabled. 1 = Does not mask the generation of a SERR DMI cycle on a catastrophic thermal sensor trip.
4	R/W	0b	<b>SERRonHotThermalSensorEvent:</b> 0 = Disable. Reporting of this condition via SERR messaging is disabled. 1 = Does not mask the generation of a SERR DMI cycle on a Hot thermal sensor trip.
3	R/W	0b	<b>SERRonAux3ThermalSensorEvent (AUX3SERR):</b> 0 = Disable. Reporting of this condition via SERR messaging is disabled. 1 = Does not mask the generation of a SERR DMI cycle on a Aux3 thermal sensor trip.
2	R/W	0b	<b>SERRonAux2ThermalSensorEvent:</b> 0 = Disable. Reporting of this condition via SERR messaging is disabled. 1 = Does not mask the generation of a SERR DMI cycle on a Aux2 thermal sensor trip.
1	R/W	0b	<b>SERRonAux1ThermalSensorEvent:</b> 0 = Disable. Reporting of this condition via SERR messaging is disabled. 1 = Does not mask the generation of a SERR DMI cycle on a Aux1 thermal sensor trip.
0	R/W	0b	<b>SERRonAux0ThermalSensorEvent:</b> 0 = Disable. Reporting of this condition via SERR messaging is disabled. 1 = Does not mask the generation of a SERR DMI cycle on a Aux0 thermal sensor trip.



## 20.5.25 TSMICMD - Thermal SMI Command

B/D/F/Type: 0/0/0/MCHBAR Thermal  
Address Offset: 10E5h  
Default Value: 00h  
Access: R/W  
Size: 8 bits  
BIOS Optimal Default 0h

This register selects specific errors to generate a SMI DMI cycle, as enabled by the SMI Error Command Register[SMI on Thermal Sensor Trip].

Bit	Access	Default Value	Description
7:6	RO	0h	<b>Reserved</b>
5	R/W	0b	<b>SMIonCatastrophicThermalSensorTrip:</b> 0 = Disable reporting of this condition via SMI messaging. 1 = Does not mask the generation of an SMI DMI cycle on a catastrophic thermal sensor trip.
4	R/W	0b	<b>SMIonHotThermalSensorTrip:</b> 0 = Disable reporting of this condition via SMI messaging. 1 = Does not mask the generation of an SMI DMI cycle on a Hot thermal sensor trip.
3	R/W	0b	<b>SMIonAux3ThermalSensorTrip (AUX3SMI):</b> 0 = Disable reporting of this condition via SMI messaging. 1 = Does not mask the generation of an SMI DMI cycle on an Aux3 thermal sensor trip.
2	R/W	0b	<b>SMIonAux2ThermalSensorTrip:</b> 0 = Disable reporting of this condition via SMI messaging. 1 = Does not mask the generation of an SMI DMI cycle on an Aux2 thermal sensor trip.
1	R/W	0b	<b>SMIonAux1ThermalSensorTrip:</b> 0 = Disable reporting of this condition via SMI messaging. 1 = Does not mask the generation of an SMI DMI cycle on an Aux1 thermal sensor trip.
0	R/W	0b	<b>SMIonAux0ThermalSensorTrip:</b> 0 = Disable reporting of this condition via SMI messaging. 1 = Does not mask the generation of an SMI DMI cycle on an Aux0 thermal sensor trip.



## 20.5.26 TSCICMD - Thermal SCI Command

B/D/F/Type: 0/0/0/MCHBAR Thermal  
 Address Offset: 10E6h  
 Default Value: 00h  
 Access: R/W  
 Size: 8 bits  
 BIOS Optimal Default: 0h

This register selects specific errors to generate a SCI DMI cycle, as enabled by the SCI Error Command Register[SCI on Thermal Sensor Trip].The SCI and SERR must not be enabled at the same time for the thermal sensor event.

Bit	Access	Default Value	Description
7:6	RO	0h	<b>Reserved</b>
5	R/W	0b	<b>SCIonCatastrophicThermalSensorTrip:</b> 0 = Disable. Reporting of this condition via SCI messaging is disabled. 1 = Does not mask the generation of an SCI DMI cycle on a catastrophic thermal sensor trip.
4	R/W	0b	<b>SCIonHotThermalSensorTrip:</b> 0 = Disable. Reporting of this condition via SCI messaging is disabled. 1 = Does not mask the generation of an SCI DMI cycle on a Hot thermal sensor trip.
3	R/W	0b	<b>SCIonAux3ThermalSensorTrip (AUX3SCI):</b> 0 = Disable. Reporting of this condition via SCI messaging is disabled. 1 = Does not mask the generation of an SCI DMI cycle on a Aux3 thermal sensor trip.
2	R/W	0b	<b>SCIonAux2ThermalSensorTrip:</b> 0 = Disable. Reporting of this condition via SCI messaging is disabled. 1 = Does not mask the generation of an SCI DMI cycle on a Aux2 thermal sensor trip.
1	R/W	0b	<b>SCIonAux1ThermalSensorTrip:</b> 0 = Disable. Reporting of this condition via SCI messaging is disabled. 1 = Does not mask the generation of an SCI DMI cycle on a Aux1 thermal sensor trip.
0	R/W	0b	<b>SCIonAux0ThermalSensorTrip:</b> 0 = Disable. Reporting of this condition via SCI messaging is disabled. 1 = Does not mask the generation of an SCI DMI cycle on a Aux0 thermal sensor trip.



## 20.5.27 TINTRCMD - Thermal INTR Command

B/D/F/Type: 0/0/0/MCHBAR Thermal  
Address Offset: 10E7h  
Default Value: 00h  
Access: R/W  
Size: 8 bits  
BIOS Optimal Default 0h  
This register selects specific errors to generate an INT DMI cycle

Bit	Access	Default Value	Description
7:6	RO	0h	<b>Reserved</b>
5	R/W	0b	<b>INTRonCatastrophicThermalSensorTrip:</b> 1 = A INTR DMI cycle is generated by (G)MCH
4	R/W	0b	<b>INTRonHotThermalSensorTrip:</b> 1 = A INTR DMI cycle is generated by (G)MCH
3	R/W	0b	<b>INTRonAux3ThermalSensorTrip (AUX3INTR):</b> 1 = A INTR DMI cycle is generated by (G)MCH
2	R/W	0b	<b>INTRonAux2ThermalSensorTrip:</b> 1 = A INTR DMI cycle is generated by (G)MCH
1	R/W	0b	<b>INTRonAux1ThermalSensorTrip:</b> 1 = A INTR DMI cycle is generated by (G)MCH
0	R/W	0b	<b>INTRonAux0ThermalSensorTrip:</b> 1 = A INTR DMI cycle is generated by (G)MCH



## 20.5.28 EXTTSCS - External Thermal Sensor Control and Status

B/D/F/Type: 0/0/0/MCHBAR Thermal  
 Address Offset: 10EFh  
 Default Value: 00h  
 Access: RO; R/W/L; R/WO  
 Size: 8 bits  
 BIOS Optimal Default: 0h

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Bit	Access	Default Value	Description
7	R/WO	0b	<p><b>ExternalSensorEnable:</b> Setting this bit to 1 locks the lockable bits in this register. This bit may only be set to a zero by a hardware reset. Once locked, writing a 0 to bit has no effect.</p> <p>EXTTS0 and EXTTS1 input signal pins are dedicated external thermal sensor use. An asserted External Thermal Sensor Trip signal can also cause a SCI, SMI, SERR or INTR interrupt as well as the Internal Sensor. A 0 on the pins can be used to trigger throttling.</p> <p>If both internal sensor throttling and external write sensor throttling are enabled, either can initiate throttling.</p> <p>The AS0 and AS1 bits of this register allow control of what action is triggered by external sensor trips. The (G)MCH Throttling select bit controls the type of throttling action that will happen, and the {AS0, AS1} bits control what trip actions will result.</p> <p>0 = External Sensor input is disabled.    1 = External Sensor input is enabled.</p>
6	R/W/L	0b	<p><b>ThrottlingTypeSelect (TTS):</b> Lockable by EXTTSCS [External Sensor Enable].</p> <p>If External Thermal Sensor Enable = 1, then:</p> <p>0 = DRAM throttling based on the settings in the Device 0 MCHBAR DRAM Throttling Control register.</p> <p>1 = (G)MCH throttling, based on the settings in the Device 0 MCHBAR (G)MCH Throttling Control Register and the Device 2 Graphics Render Throttle Control Register [Catastrophic and Hot Hardware controlled Thermal Throttle Duty Cycle] else.</p>
5	R/W/L	0b	<p><b>EXTTS1ActionSelect (AS1):</b> Lockable by EXTTSCS [External Sensor Enable]. If External Thermal Sensor Enable = 1, then:</p> <p>0 = The external sensor trip functions same as a Thermometer mode hot trip.</p> <p>1 = The external sensor trip functions as a Thermometer mode aux0 trip.</p>
4	R/W/L	0b	<p><b>EXTTS0ActionSelect (AS0):</b> Lockable by EXTTSCS [External Sensor Enable].</p> <p>If External Thermal Sensor Enable = 1, then:</p> <p>0 = The external sensor trip functions same as a Thermometer mode catastrophic trip.</p> <p>1 = The external sensor trip functions same as a Thermometer mode hot trip.</p>



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Bit	Access	Default Value	Description
3	RO	0b	<b>EXTTSOTripIndicator (S0TI):</b> A 1 indicates that an externally monitored temperature is exceeding the programmed setting of an external thermal sensor.
2	RO	0b	<b>EXTTS1TripIndicator (S1TI):</b> A 1 indicates that an externally monitored temperature is exceeding the programmed setting of an external thermal sensor.
1:1	RO	0h	<b>Reserved</b>
0	R/W/L	0b	<b>External Thermal Sensor Signals Routing Control:</b> 0 = Route all external sensor signals to affect internal thermal sensor 1 registers, as appropriate. 1 = Route all external sensor signals to affect internal thermal sensor 2 registers, as appropriate.

## 20.6 MCHBAR Render Thermal Throttling

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		1100	1101	0000h	R/W
VID and Frequency Relationship Table 1	VIDFREQ1	1110	1113	00000000h	R/W
Reserved		1114	111F		
Internal to External VID Mapping Table 1	INTTOEXT1	1120	1123	00000000h	RO; R/W
Internal to External VID Mapping Table 2	INTTOEXT2	1124	1127	00000000h	RO; R/W
Internal to External VID Mapping Table 3	INTTOEXT3	1128	112B	00000000h	RO; R/W
Reserved		112C	11AF		
Thermal State Control	THERMSTCTL	11B0	11B3	00000000h	R/W
Render Standby State Control	RSTDBYCTL	11B8	11BB	00000000h	R/W
Reserved		11BC	11BF		
VID Control	VIDCTL	11C0	11C3	00000000h	R/W
VID Control 1	VIDCTL1	11C4	11C7	00000000h	R/W
Reserved		11C8	11E9		



### 20.6.1 CRSTANDVID - Render Standby VID

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1100-1101h
Default Value:	0000h
Access:	R/W
Size:	16 bits
BIOS Optimal Default	00h

This register contains the VIDs for Render Standby.

Bit	Access	Default Value	Description
15:12	RO	0h	<b>Reserved</b>
11:8	R/W	0000b	<b>Render Standby without Context Restore Voltage VID (a.k.a. standby VCCMIN) (R2VID):</b> The value in this register corresponds to the internal VID mapping
7:4	RO	0h	<b>Reserved</b>
3:0	R/W	0000b	<b>Reserved</b>

### 20.6.2 VIDFREQ1 - VID and Frequency Relationship Table 1

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	1110-1113h
Default Value:	00000000h
Access:	R/W
Size:	32 bits
BIOS Optimal Default	0000h

Bit	Access	Default Value	Description
31:28	RO	0h	<b>Reserved</b>
27:24	R/W	0000b	<b>VID Point -- P0 (VIDP0)</b>
23:20	RO	0h	<b>Reserved</b>
19:16	R/W	0000b	<b>P0 Frequency (P0FREQ)</b>
15:12	RO	0h	<b>Reserved</b>
11:8	R/W	0000b	<b>VID Point -- P1 (VIDP1)</b>
7:4	RO	0h	<b>Reserved</b>
3:0	R/W	0000b	<b>Reserved</b>



### 20.6.3 INTTOEXT1 - Internal to External VID Mapping Table 1

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 1120-1123h  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

Bit	Access	Default Value	Description
31:28	RO	0h	<b>Reserved</b>
27:24	R/W	0000b	<b>External Mapping for Internal Mapping 15 (MAP15):</b> External mapping for internal mapping 15
23:20	RO	0h	<b>Reserved</b>
19:16	R/W	0000b	<b>External Mapping for Internal Mapping 14 (MAP14)</b>
15:12	RO	0h	<b>Reserved</b>
11:8	R/W	0000b	<b>External Mapping for Internal Mapping 13 (MAP13)</b>
7:4	RO	0h	<b>Reserved</b>
3:0	R/W	0000b	<b>External Mapping for Internal Mapping 12 (MAP12)</b>

### 20.6.4 INTTOEXT2 - Internal to External VID Mapping Table 2

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 1124-1127h  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

Bit	Access	Default Value	Description
31:28	RO	0h	<b>Reserved</b>
27:24	R/W	0000h	<b>External Mapping for Internal Mapping 11 (MAP11)</b>
23:20	RO	0h	<b>Reserved</b>
19:16	R/W	0000b	<b>External Mapping for Internal Mapping 10 (MAP10)</b>
15:12	RO	0h	<b>Reserved</b>
11:8	R/W	0000b	<b>External Mapping for Internal Mapping 9 (MAP9)</b>
7:4	RO	0h	<b>Reserved</b>
3:0	R/W	0000b	<b>External Mapping for Internal Mapping 8 (MAP8)</b>



## 20.6.5 INTTOEXT3 - Internal to External VID Mapping Table 3

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 1128-112Bh  
 Default Value: 00000000h  
 Access: RO; R/W  
 Size: 32 bits

Bit	Access	Default Value	Description
31:28	RO	0h	<b>Reserved</b>
27:24	R/W	0h	<b>External Mapping for Internal Mapping 7 (MAP7)</b>
23:20	RO	0h	<b>Reserved</b>
19:16	R/W	0000b	<b>External Mapping for Internal Mapping 6 (MAP6)</b>
15:12	RO	0h	<b>Reserved</b>
11:8	R/W	0000b	<b>External Mapping for Internal Mapping 5 (MAP5)</b>
7:4	RO	0h	<b>Reserved:</b>
3:0	R/W	0000b	<b>External Mapping for Internal Mapping 4 (MAP4)</b>

## 20.6.6 THERMSTCTL - Thermal State Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 11B0-11B3h  
 Default Value: 00000000h  
 Access: R/W  
 Size: 32 bits  
 BIOS Optimal Default 00000h

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification

## 20.6.7 RSTDBYCTL - Render Standby State Control

B/D/F/Type: 0/0/0/MCHBAR  
 Address Offset: 11B8-11BBh  
 Default Value: 00000000h  
 Access: R/W  
 Size: 32 bits  
 BIOS Optimal Default 000h

Bit	Access	Default Value	Description
31	R/W	0b	<b>Reserved</b>
30	R/W	0b	<b>RS2 Enable (RS2EN):</b> 0 = RS2 not enabled 1 = RS2 enabled
29:0	R/W	0000000b	<b>Reserved</b>



## 20.6.8 VIDCTL - VID Control

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 11C0-11C3h  
Default Value: 00000000h  
Access: R/W  
Size: 32 bits

Bit	Access	Default Value	Description
31:24	R/W	00h	<b>VID Up Time (VIDUPTIME):</b> 0 = 255 µs 1 = 1 µs 255 = 255 µs
23:16	R/W	00h	<b>VID Down Time (VIDDNTIME):</b> 0 = 255 µs 1 = 1 µs 255 = 255 µs
15:0	R/W	0000h	<b>Reserved</b>

## 20.6.9 VIDCTL1 - VID Control 1

B/D/F/Type: 0/0/0/MCHBAR  
Address Offset: 11C4-11C7h  
Default Value: 00000000h  
Access: R/W  
Size: 32 bits

This register bit field shall contain the default value unless otherwise indicated in the BIOS Specification.



## 20.7 Device 0 MCHBAR DRAM Controls

(Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Channel 0 DRAM Rank Boundary 0/1	C0DRB01	1200	1203	00000000h	RO; R/W
Reserved		1204	1207		
Channel 0 DRAM Rank 0,1,2,3 Attribute	C0DRA	1208	120B	00000000h	RO; R/W
Channel 0 DRAM Clock Disable	C0DCLKDIS	120C	120F	00000000h	RO; R/W
Reserved		1210	1213		
Channel 0 DRAM Timing Register 0	C0DRT0	1210	1213	34B10461h	RO; R/W
Channel 0 DRAM Timing Register 1	C0DRT1	1214	1217	11E08463h	RO; R/W
Channel 0 DRAM Timing Register 2	C0DRT2	1218	121B	2200105Fh	RO; R/W
Channel 0 DRAM Timing Register 3	C0DRT3	121C	121F	01056102h	RO; R/W
Channel 0 DRAM Timing Register 4	C0DRT4	1220	1223	28643C32h	RO; R/W
Reserved		1224	122F		
Channel 0 DRAM Controller Mode 0	C0DRC0	1230	1233	4F000008h	RO; R/W
Channel 0 DRAM Controller Mode 1	C0DRC1	1234	1237	00000000h	RO; R/W
Reserved		1238	123B		
Channel 0 ODT Control.	C0ODT	1248	124F	00828787200 02020h	RO; R/W
Reserved		1250	126F		
Channel 0 GMCH Throttling Event Weights	C0GTEW	1270	1273	00000000h	R/W/L
Channel 0 GMCH Throttling Event Control	C0GTC	1274	1277	00000000h	RO; R/W/L
Channel 0 DRAM Rank Throttling Passive Event	C0DTPEW	1278	127F	000000000000 00000h	RO; R/W/L
Channel 0 DRAM Rank Throttling Active Event	C0DTAEW	1280	1287	000000000000 00000h	RO; R/W/L
Channel 0 DRAM Throttling Control	C0DTC	1288	128B	00000000h	RO; R/W/L
Reserved		128C	12B3		
Channel 0 DRAM Thermal Sensor Watch Dog Timer	C0DTWDT	12B4	12B7	00000000h	RO; R/W/L



## (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Channel 1 DRAM Rank Boundary 0/1	C1DRB01	1300	1303	00000000h	RO; R/W
Reserved		1304	1307		
Channel 1 DRAM Rank 0,1,2,3 Attribute	C1DRA	1308	130B	00000000h	RO; R/W
Channel 1 DRAM Clock Disable	C1DCLKDIS	130C	130F	00000000h	RO; R/W
Channel 1 DRAM Timing Register 0	C1DRT0	1310	1313	34B10461h	RO; R/W
Channel 1 DRAM Timing Register 1	C1DRT1	1314	1317	11E08463h	RO; R/W
Channel 1 DRAM Timing Register 2	C1DRT2	1318	131B	2200105Fh	RO; R/W
Channel 1 DRAM Timing Register 3	C1DRT3	131C	131F	01056102h	RO; R/W
Reserved		1320	132F		
Channel 1 DRAM Controller Mode 0	C1DRC0	1330	1333	4F000008h	RO; R/W
Channel 1 DRAM Controller Mode 1	C1DRC1	1334	1337	00000000h	RO; R/W
Channel 1 DRAM Controller Mode 2	C1DRC2	1338	133B	00000000h	RO; R/W
Reserved		1348	136F		
Channel 1 GMCH Throttling Event Weights	C1GTEW	1370	1373	00000000h	R/W/L
Channel 1 GMCH Throttling Event Control	C1GTC	1374	1377	00000000h	RO; R/W/L
Channel 1 DRAM Rank Throttling Passive Event	C1DTPEW	1378	137F	000000000000 00000h	RO; R/W/L
Channel 1 DRAM Rank Throttling Active Event	C1DTAEW	1380	1387	000000000000 00000h	RO; R/W/L
Channel 1 DRAM Throttling Control	C1DTC	1388	138B	00000000h	RO; R/W/L
Reserved		138C	13B3		
Channel 1 DRAM Thermal Sensor Watch Dog Timer	C1DTWDT	13B4	13B7	00000000h	RO; R/W/L



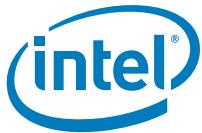
## 20.7.1 C0DRB01 - Channel 0 DRAM Rank Boundary 0/1

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1200-1203h
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

The DRAM Rank Boundary Register defines the upper boundary address of each DRAM rank with a granularity of 32. These registers are used to determine which chip select will be active for a given address.

In all modes, if a SO-DIMM is single-sided, it appears as a populated rank and an empty rank. A DRB must be programmed appropriately for each.

Bit	Access	Default Value	Description
31:25	RO	00h	<b>Reserved</b>
24:16	R/W	000h	<b>Channel 0 DRAM Rank 1 Boundary Address (DRB1):</b> This 9-bit value defines the upper and lower addresses for each DRAM rank. Bits 7:2 are compared against Address 32:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0's. Bit 8 may be programmed to a 1 in the highest DRB (DRB3) if 8 GB of memory are present.
15:9	RO	00h	<b>Reserved</b>
8:0	R/W	000h	<b>Channel 0 DRAM Rank 0 Boundary Address (DRB0):</b> This 9-bit value defines the upper and lower addresses for each DRAM rank. Bits 7:2 are compared against Address 32:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0's. Bit 8 may be programmed to a 1 in the highest DRB (DRB3) if 8 GB of memory are present.



## 20.7.2 C0DRA - Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR Chipset  
Address Offset: 1208-120Bh  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

The **DRAM Rank Attribute Registers** define the page sizes to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31:27	RO	00h	<b>Reserved</b>
26:25	R/W	00b	<b>Reserved</b>
24	RO	0b	<b>Reserved</b>
23:22	R/W	00b	<b>Reserved</b>
21	RO	0b	<b>Reserved</b>
20:19	R/W	00b	<b>Rank 1 Bank Architecture:</b> 00 = 4 Bank 01 = 8 Bank 10 = 16 Bank - Reserved 11 = Reserved
18	RO	0b	<b>Reserved</b>
17:16	R/W	00b	<b>Rank 0 Bank Architecture:</b> 00 = 4 Bank 01 = 8 Bank 10 = 16 Bank - Reserved 11 = Reserved
15	RO	0b	<b>Reserved</b>
14:12	R/W	000b	<b>Reserved</b>
11	RO	0b	<b>Reserved</b>
10:8	R/W	000b	<b>Reserved</b>
7	RO	0b	<b>Reserved</b>
6:4	R/W	000b	<b>Channel 0 DRAM odd Rank 1 Attribute (DRA1):</b> This 3-bit field defines the page size of the corresponding rank. 000 = Unpopulated 001 = Reserved 010 = 4 KB 011 = 8 KB 100 = 16 KB - Reserved Others = Reserved
3	RO	0b	<b>Reserved</b>



(Sheet 2 of 2)

Bit	Access	Default Value	Description
2:0	R/W	000b	<p><b>Channel 0 DRAM even Rank 0 Attribute (DRA0):</b> This 3-bit field defines the page size of the corresponding rank.</p> <p>000 = Unpopulated 001 = Reserved 010 = 4 KB 011 = 8 KB 100 = 16 KB - Reserved Others = Reserved</p>

### 20.7.3 CODCLKDIS - Channel 0 DRAM Clock Disable

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 120C-120Fh  
 Default Value: 00000000h  
 Access: RO; R/W  
 Size: 32 bits

This register can be used to disable the System Memory Clock signals to each SO-DIMM slot, which can significantly reduce EMI and Power concerns for clocks that go to unpopulated SO-DIMMs. Clocks can be enabled based on whether a slot is populated.

Since there are multiple clock signals assigned to each rank of a SO-DIMM, it is important to clarify exactly which rank width field affects which clock signal.

Bit	Access	Default Value	Description
31:3	RO	00000000h	<b>Reserved</b>
2	R/W	0b	<b>Reserved</b>
1	R/W	0b	<b>SO-DIMM Clock Gate Enable Pair 1:</b> 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
0	R/W	0b	<b>SO-DIMM Clock Gate Enable Pair 0:</b> 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.



## 20.7.4 C0DRT0 - Channel 0 DRAM Timing Register 0

B/D/F/Type: 0/0/0/MCHBAR Chipset  
Address Offset: 1210-1213h  
Default Value: 34B10461h  
Access: RO; R/W  
Size: 32 bits

This 32-bit register defines the timing parameters for all devices in this channel. The BIOS programs this register with the "least common denominator" values for each channel after reading configuration registers of each device in each channel.

(Sheet 1 of 5)

Bit	Access	Default Value	Description
31	RO	0b	<b>Reserved</b>
30:26	R/W	0dh	<b>Back-to-Back Write to Precharge Command Spacing (Same Rank) (B2BWR2PCSB):</b> This field determines the number of clocks between write command and a subsequent precharge command to the same bank. The minimum number of clocks is calculated based on this formula: DDR2 / DDR3: WL+ BL/2 + t WR 0h to 9h: Reserved Ah to 13h: Allowed
25	RO	0b	<b>Reserved</b>
24:20	R/W	0Bh	<b>Back-to-Back Write to Read Command Spacing (Same Rank):</b> This field determines the number of clocks between write command and a subsequent read command to the same rank. The minimum number of clocks is calculated based on this formula: DDR2 / DDR3: WL + BL/2 + t WTR 0h - 7h: Reserved 8h - Fh: Allowed <b>NOTE:</b> Write to Read Command delay (tWTR). The tWTR is a standard DDR timing parameter and is used to time a RD command after a WR command to the same row.
19:18	RO	00b	<b>Reserved</b>



(Sheet 2 of 5)

Bit	Access	Default Value	Description																
17:15	R/W	010b	<p><b>Back-to-Back Write-Read Command Spacing (Different Rank):</b></p> <p>This field determines the number of turnaround clocks on the data bus that needs to be inserted between write command and a subsequent read command.</p> <p>The minimum spacing of commands is calculated based on the formula:</p> $\text{Spacing} = \text{BL}/2 + \text{TA (wr-rd)} + \text{WL} - \text{CL}$ <p>BL is the burst length and can be set to either 4 or 8      TA is the required write to read DQ turnaround on the bus. Can be set to 1,2, or 3 CK using this register      CL is CAS Latency      WL is Write Latency</p> <table border="1"> <thead> <tr> <th>Encoding</th><th>BL8 CMD Spacing</th></tr> </thead> <tbody> <tr><td>110</td><td>9</td></tr> <tr><td>101</td><td>8</td></tr> <tr><td>100</td><td>7</td></tr> <tr><td>011</td><td>6</td></tr> <tr><td>010</td><td>5</td></tr> <tr><td>001</td><td>4</td></tr> <tr><td>000</td><td>3</td></tr> </tbody> </table>	Encoding	BL8 CMD Spacing	110	9	101	8	100	7	011	6	010	5	001	4	000	3
Encoding	BL8 CMD Spacing																		
110	9																		
101	8																		
100	7																		
011	6																		
010	5																		
001	4																		
000	3																		
14	RO	0b	<b>Reserved</b>																



(Sheet 3 of 5)

Bit	Access	Default Value	Description																		
13:10	R/W	1h	<p><b>Back-to-Back Read-Write Command Spacing:</b> This field determines the number of turnaround clocks between the read command and a subsequent write command. Same and different rank.</p> <p>The minimum spacing of commands is calculated based on the formula:</p> $\text{Spacing} = \text{CL} + \text{BL}/2 + \text{TA} (\text{wr-rd}) - \text{WL}$ <p>BL is the burst length and can be set to either 4 or 8 TA is the required read to write DQ turnaround on the bus. Can be set to 1,2,3, 4 CK for DDR2 CL is CAS Latency WL is Write Latency</p> <table border="1"><thead><tr><th>Encoding</th><th>BL8 CMD Spacing</th></tr></thead><tbody><tr><td>0111</td><td>12</td></tr><tr><td>0110</td><td>11</td></tr><tr><td>0101</td><td>10</td></tr><tr><td>0100</td><td>9</td></tr><tr><td>0011</td><td>8</td></tr><tr><td>0010</td><td>7</td></tr><tr><td>0001</td><td>6</td></tr><tr><td>0000</td><td>5</td></tr></tbody></table> <p>The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest SO-DIMM is large.</p>	Encoding	BL8 CMD Spacing	0111	12	0110	11	0101	10	0100	9	0011	8	0010	7	0001	6	0000	5
Encoding	BL8 CMD Spacing																				
0111	12																				
0110	11																				
0101	10																				
0100	9																				
0011	8																				
0010	7																				
0001	6																				
0000	5																				
9:8	RO	00b	<b>Reserved</b>																		



(Sheet 4 of 5)

Bit	Access	Default Value	Description																		
7:5	R/W	011b	<p><b>Back-to-Back Write Command Spacing (Different Rank):</b>  This field controls the turnaround time on the DQ bus for WR-WR sequence to different ranks in one channel.  The minimum spacing of commands is calculated based on the formula:  <b>DDR2 and DDR3= BL/2 + TA</b></p> <table border="1"> <thead> <tr> <th>Encoding</th><th>Turnaround</th><th>BL8 CMD Spacing</th></tr> </thead> <tbody> <tr> <td>100</td><td>4 turnaround clocks on DQ</td><td>8</td></tr> <tr> <td>011</td><td>3 turnaround clocks on DQ</td><td>7</td></tr> <tr> <td>010</td><td>2 turnaround clocks on DQ</td><td>6</td></tr> <tr> <td>001</td><td>1 turnaround clocks on DQ</td><td>5</td></tr> <tr> <td>000</td><td>0 turnaround clocks on DQ</td><td>4</td></tr> </tbody> </table> <p>The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest SO-DIMM is large.</p>	Encoding	Turnaround	BL8 CMD Spacing	100	4 turnaround clocks on DQ	8	011	3 turnaround clocks on DQ	7	010	2 turnaround clocks on DQ	6	001	1 turnaround clocks on DQ	5	000	0 turnaround clocks on DQ	4
Encoding	Turnaround	BL8 CMD Spacing																			
100	4 turnaround clocks on DQ	8																			
011	3 turnaround clocks on DQ	7																			
010	2 turnaround clocks on DQ	6																			
001	1 turnaround clocks on DQ	5																			
000	0 turnaround clocks on DQ	4																			
4:3	RO	00b	<b>Reserved</b>																		



(Sheet 5 of 5)

Bit	Access	Default Value	Description																					
2:0	R/W	001b	<p><b>Back-to-Back Read Command Spacing (Different Rank):</b> This field controls the turnaround time on the DQ bus for Rd-RD sequence to different ranks in one channel. The minimum spacing of commands is calculated based on the formula <b>DDR2 and DDR3= BL/2 + TA</b></p> <table border="1"><thead><tr><th>Encoding</th><th>Turnaround</th><th>BL8 CMD Spacing</th></tr></thead><tbody><tr><td>101</td><td>6 turnaround clocks on DQ</td><td>10</td></tr><tr><td>100</td><td>5 turnaround clocks on DQ</td><td>9</td></tr><tr><td>011</td><td>4 turnaround clocks on DQ</td><td>8</td></tr><tr><td>010</td><td>3 turnaround clocks on DQ</td><td>7</td></tr><tr><td>001</td><td>2 turnaround clocks on DQ</td><td>6</td></tr><tr><td>000</td><td>1 turnaround clocks on DQ</td><td>5</td></tr></tbody></table> <p>The bigger turnarounds are used in large configurations, where the difference in total channel delay between the fastest and slowest SO-DIMM is large.</p>	Encoding	Turnaround	BL8 CMD Spacing	101	6 turnaround clocks on DQ	10	100	5 turnaround clocks on DQ	9	011	4 turnaround clocks on DQ	8	010	3 turnaround clocks on DQ	7	001	2 turnaround clocks on DQ	6	000	1 turnaround clocks on DQ	5
Encoding	Turnaround	BL8 CMD Spacing																						
101	6 turnaround clocks on DQ	10																						
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011	4 turnaround clocks on DQ	8																						
010	3 turnaround clocks on DQ	7																						
001	2 turnaround clocks on DQ	6																						
000	1 turnaround clocks on DQ	5																						



## 20.7.5 CODRT1 - Channel 0 DRAM Timing Register 1

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 1214-1217h  
 Default Value: 11E08463h  
 Access: RO; R/W  
 Size: 32 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31:30	RO	00b	<b>Reserved</b>
29:28	R/W	01b	<b>Read to Precharge (tRTP):</b> These bits control the number of clocks that are inserted between a read command to a row precharge command to the same rank.
27:26	RO	00b	<b>Reserved</b>
25:21	R/W	0Fh	<b>Activate to Precharge delay (tRAS):</b> This bit controls the number of DRAM clocks for tRAS. Minimum recommendations are beside their corresponding encodings.
20:19	RO	00b	<b>Reserved</b>
18	R/W	0b	<b>Precharge to Precharge Delay:</b> Control Pre to Pre delay between the different banks of the same rank. 0 = 1 Clock 1 = 2 Clocks
17:16	RO	00b	<b>Reserved</b>
15	R/W	1b	<b>Pre-All to Activate Delay (tRPALL):</b> This is applicable only to 8-bank architectures. Must be set to 1 if any Rank is populated with 8-bank device technology. 0 = tRPALL = tRP 1 = tRPALL = tRP + 1
14:13	RO	00b	<b>Reserved</b>
12:10	R/W	001b	<b>Activate to Activate Delay (tRRD):</b> Control Act to Act delay between the different banks of the same rank. Tr is specified in "ns". 10 ns for 2-KB page size and 7.5 ns for 1-KB page size. BIOS should round up to the nearest number of clocks and use the maximum applicable value. 000 = 2 Clocks 001 = 3 Clocks 010 = 4 Clocks 011 = 5 Clocks 100 = 6 Clocks
9:8	RO	00b	<b>Reserved</b>



(Sheet 2 of 2)

Bit	Access	Default Value	Description																		
7:5	R/W	011b	<b>DRAM RASB to CASB Delay (tRCD):</b> This bit controls the number of clocks inserted between a row activate command and a read or write command to that row.  <table border="1"><thead><tr><th>Encoding</th><th>tRCD</th></tr></thead><tbody><tr><td>000</td><td>2 DRAM Clocks</td></tr><tr><td>001</td><td>3 DRAM Clocks</td></tr><tr><td>010</td><td>4 DRAM Clocks</td></tr><tr><td>011</td><td>5 DRAM Clocks</td></tr><tr><td>100</td><td>6 DRAM Clocks</td></tr><tr><td>101</td><td>7 DRAM Clocks</td></tr><tr><td>110</td><td>8 DRAM Clocks</td></tr><tr><td>111</td><td>Reserved.</td></tr></tbody></table>	Encoding	tRCD	000	2 DRAM Clocks	001	3 DRAM Clocks	010	4 DRAM Clocks	011	5 DRAM Clocks	100	6 DRAM Clocks	101	7 DRAM Clocks	110	8 DRAM Clocks	111	Reserved.
Encoding	tRCD																				
000	2 DRAM Clocks																				
001	3 DRAM Clocks																				
010	4 DRAM Clocks																				
011	5 DRAM Clocks																				
100	6 DRAM Clocks																				
101	7 DRAM Clocks																				
110	8 DRAM Clocks																				
111	Reserved.																				
4:3	RO	00b	<b>Reserved</b>																		
2:0	R/W	011b	<b>DRAM RASB Precharge (tRP):</b> This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank.  <table border="1"><thead><tr><th>Encoding</th><th>tRP</th></tr></thead><tbody><tr><td>000</td><td>2 DRAM Clocks</td></tr><tr><td>001</td><td>3 DRAM Clocks</td></tr><tr><td>010</td><td>4 DRAM Clocks</td></tr><tr><td>011</td><td>5 DRAM Clocks</td></tr><tr><td>100</td><td>6 DRAM clocks</td></tr><tr><td>101</td><td>7 DRAM clocks</td></tr><tr><td>110</td><td>8 DRAM clocks</td></tr><tr><td>111</td><td>Reserved</td></tr></tbody></table>	Encoding	tRP	000	2 DRAM Clocks	001	3 DRAM Clocks	010	4 DRAM Clocks	011	5 DRAM Clocks	100	6 DRAM clocks	101	7 DRAM clocks	110	8 DRAM clocks	111	Reserved
Encoding	tRP																				
000	2 DRAM Clocks																				
001	3 DRAM Clocks																				
010	4 DRAM Clocks																				
011	5 DRAM Clocks																				
100	6 DRAM clocks																				
101	7 DRAM clocks																				
110	8 DRAM clocks																				
111	Reserved																				



## 20.7.6 CODRT2 - Channel 0 DRAM Timing Register 2

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 1218-121Bh  
 Default Value: 2200105Fh  
 Access: RO; R/W  
 Size: 32 bits  
 This register shall retain its default values or be programmed as per the (G)MCH BIOS specification.

## 20.7.7 CODRT3 - Channel 0 DRAM Timing Register 3

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 121C-121Fh  
 Default Value: 01056102h  
 Access: RO; R/W  
 Size: 32 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description																					
31:30	RO	00b	<b>Reserved</b>																					
29:28	R/W	00b	<b>Reserved</b>																					
27:26	R/W	00b	<b>Reserved</b>																					
25:23	R/W	010b	<p><b>CASB Latency (tCL):</b> This value is programmable on SO-DIMMs. The value programmed here must match the CAS Latency of every SO-DIMM in the system.</p> <table border="1"> <thead> <tr> <th>Encoding</th><th>DDR2 CL</th><th>DDR3 CL</th></tr> </thead> <tbody> <tr> <td>000</td><td>3</td><td>3</td></tr> <tr> <td>001</td><td>4</td><td>4</td></tr> <tr> <td>010</td><td>5</td><td>5</td></tr> <tr> <td>011</td><td>6</td><td>6</td></tr> <tr> <td>100</td><td>7</td><td>7</td></tr> <tr> <td>101</td><td>Reserved</td><td>8</td></tr> </tbody> </table>	Encoding	DDR2 CL	DDR3 CL	000	3	3	001	4	4	010	5	5	011	6	6	100	7	7	101	Reserved	8
Encoding	DDR2 CL	DDR3 CL																						
000	3	3																						
001	4	4																						
010	5	5																						
011	6	6																						
100	7	7																						
101	Reserved	8																						
22:21	RO	00b	<b>Reserved</b>																					
20:13	R/W	2Bh	<b>Refresh Cycle Time (tRFC):</b> Refresh cycle time is measured from a Refresh command (REF) until the first Activate command (ACT) to the same rank, required to perform a read or write.																					
12:11	RO	00b	<b>Reserved</b>																					
10:7	R/W	2h	<b>Reserved</b>																					
6:3	RO	0h	<b>Reserved</b>																					



(Sheet 2 of 2)

Bit	Access	Default Value	Description
2:0	R/W	010b	<b>Write Latency (tWL):</b> For DDR2 this register is programmed to CL -1 For DDR3 WL is based on DDR freq. 000 - 2 - DDR2 - CL3 001 - 3 - DDR2 - CL4 010 - 4 - DDR2 - CL5 011 - 5 - DDR2 - CL6 or DDR3 - 800 100 - 6 - DDR2 - CL7 101 - 7 - DDR2 - CL8 Others - Reserved

## 20.7.8 C0DRC0 - Channel 0 DRAM Controller Mode 0

B/D/F/Type: 0/0/0/MCHBAR Chipset  
Address Offset: 1230-1233h  
Default Value: 4F000008h  
Access: RO; R/W  
Size: 32 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31:30	RO	01b	<b>Revision Number (REV):</b> Reflects the revision number of the format used for SDRAM DDR register definition.
29	RO	0b	<b>Reserved</b>
28	RO	0b	<b>Reserved</b>
27:24	R/W	Fh	<b>Rank Enable Bits (RANKEN):</b> These bits should be set to 1 to enable the corresponding rank to come out of Self refresh. The setting of the bit is either done by the Firmware or BIOS. Only those ranks that are populated will be woken up. Writing a 1 to a non-populated rank will not have any effect. [25] = Rank 1 [24] = Rank 0
23:22	RO	0h	<b>Reserved</b>
21:20	RO	00b	<b>Reserved</b>
19:18	RO	00b	<b>DRB Granularity (DRBG):</b> The value in the DRBG field sets the meaning given to the values in the set of DRB registers. 00: Numbers in DRB registers represent 32-MB quantities Other: Reserved
17	RO	0h	<b>Reserved</b>
16	R/W	0h	<b>Reserved</b>
15	RO	0h	<b>Reserved</b>
14	RO	0b	<b>Reserved</b>
13:11	RO	0h	<b>Reserved</b>



(Sheet 2 of 2)

Bit	Access	Default Value	Description
10:8	R/W	000b	<b>Refresh Mode Select (RMS):</b> This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000 = Refresh disabled 010 = Refresh enabled. Refresh interval 7.8 $\mu$ sec 011 = Refresh enabled. Refresh interval 3.9 $\mu$ sec Other = Reserved.
7:4	RO	0h	<b>Reserved</b>
3	R/W	1b	<b>Burst Length (BL):</b> The burst length is the number of QWORDS returned by a SO-DIMM per read command, when not interrupted. This bit is used to select the DRAM controller's Burst Length operation mode. It must be set to match to the behavior of the SO-DIMM. 1 = Burst Length of 8
2:0	RO	000b	<b>Reserved</b>

### 20.7.9 C0DRC1 - Channel 0 DRAM Controller Mode 1

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 1234-1237h  
 Default Value: 00000000h  
 Access: RO; R/W  
 Size: 32 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31	R/W	0b	<b>Address Swap/XOR Enable:</b> 0 = Swap and XOR modes disabled. 1 = Swap or XOR mode enabled.
30	R/W	0b	<b>Reserved</b>
29:28	R/W	00b	<b>Address Swap/XOR Mode:</b> 00 = Swap Enabled for Bank Selects and Rank Selects 01 = XOR Enabled for Bank Selects and Rank Selects 10 = Swap Enabled for Bank Selects only 11 = XOR Enabled for Bank Select only
27	RO	0b	<b>Reserved</b>
26:24	R/W	000b	<b>Reserved</b>
23:20	RO	0h	<b>Reserved</b>
19:16	R/W	0h	<b>CKE Tristate Enable Per Rank:</b> Bit 16 corresponds to Rank 0 and Bit 19 corresponds to rank3 0 = CKE is not tri-stated. 1 = CKE is tri-stated. This is set only if the rank is physically not populated.
15	RO	0b	<b>Reserved</b>
14	RO	0b	<b>Reserved</b>



(Sheet 2 of 2)

Bit	Access	Default Value	Description
13	RO	0b	<b>Reserved</b>
12	R/W	0b	<b>Reserved</b>
11	R/W	0b	<b>Reserved</b>
10	RO	0b	<b>Reserved</b>
9	R/W	0b	<b>Reserved</b>
8	RO	0b	<b>Reserved</b>
7	RO	0b	<b>Reserved</b>
6	R/W	0b	<b>Reserved</b>
5:4	RO	00b	<b>Reserved</b>
3	R/W	0b	<b>Reserved</b>
2:0	RO	000b	<b>Reserved</b>

### 20.7.10 COGTEW - Channel 0 GMCH Throttling Event Weights

B/D/F/Type: 0/0/0/MCHBAR Chipset  
Address Offset: 1270-1273h  
Default Value: 00000000h  
Access: R/W/L  
Size: 32 bits

Bit	Access	Default Value	Bit
31:24	R/W/L	00h	<b>Read Weight ():</b> This value is input to the filter if in a given clock there is a valid read command being issued on the memory bus.
23:16	R/W/L	00h	<b>Write Weight ():</b> This value is input to the filter if in a given clock there is a valid write command being issued on the memory bus.
15:8	R/W/L	00h	<b>Command Weight ():</b> This value is input to the filter if in a given clock there is a valid command other than a read or a write being issued on the memory bus.
7:0	R/W/L	00h	<b>Idle Weight ():</b> This value is input to the filter if in a given clock there is no command being issued on the memory bus. If command and address are tri-stated a value of 0 is input to the filter. If command and address are under reduced drive strength this value is divided by 2 and input to the filter.



### 20.7.11 C0GTC - Channel 0 GMCH Throttling Control

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 1274-1277h  
 Default Value: 00000000h  
 Access: RO; R/W/L  
 Size: 32 bits

Bit	Access	Default Value	Bit
31:22	RO	00h	<b>Reserved</b>
21	R/W/L	0b	<b>GMCH Bandwidth based throttling enable (GBTE):</b> 0 = Bandwidth Threshold (WAB) is not used for throttling. 1 = Bandwidth Threshold (WAB) is used for throttling. If both Bandwidth based and thermal sensor based throttling modes are on and the thermal sensor trips, the WAT Thermal threshold are used for throttling.
20	R/W/L	0b	<b>GMCH Thermal Sensor trip enable ():</b> 0 = GMCH throttling is not initiated when the GMCH thermal sensor trips. 1 = GMCH throttling is initiated when the GMCH thermal sensor trips and the Filter output is equal to or exceeds thermal threshold WAT.
19:16	RO	0000b	<b>Reserved</b>
15:8	R/W/L	00h	<b>WAB ():</b> Threshold allowed per clock for bandwidth based throttling. GMCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.
7:0	R/W/L	00h	<b>WAT ():</b> Threshold allowed per clock during thermal sensor enabled throttling. GMCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.



## 20.7.12 C0DTPEW - Channel 0 DRAM Rank Throttling Passive Event

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1278-127Fh
Default Value:	0000000000000000h
Access:	RO; R/W/L
Size:	64 bits

Programmable Event weights that are entered into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length and 2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks. (G)MCH implements four, independent filters, one per rank. All bits in this register can be locked by the DTLOCK bit in the C0DTC register.

Bit	Access	Default Value	Description
63:48	RO	0000h	<b>Reserved</b>
47:40	R/W/L	00h	<b>Additive Weight for ODT:</b> This value is added to the total weight of a Rank if ODT on that rank is asserted. Note that this value should reflect whether the DRAMs have been programmed for 75 or 150- $\Omega$ termination.
39:32	R/W/L	00h	<b>Weight for Any Open Page during Active (WAOPDA):</b> This value is input to the filter if, during the present clock, the corresponding rank has any pages open and is not in power down. The value programmed here is IDD3N from the JEDEC.
31:24	R/W/L	00h	<b>All Banks Precharge Active (ABPA):</b> This value is input to the filter if, during the present clock, the corresponding rank has all banks precharged but is not in power down. The value programmed here is IDD2N from the JEDEC spec.
23:16	R/W/L	00h	<b>Weight for Any Open Page during Power Down (WAOPDPD):</b> This value is input to the filter if, during the present clock, the corresponding rank is in power down with pages open. The value programmed here is IDD3P from the JEDEC.
15:8	R/W/L	00h	<b>All Banks Precharge Power Down (ABPPD):</b> This value is input to the filter if, during the present clock, the corresponding rank has all banks percharged and is powered down. The value programmed here is IDD2P from the JEDEC spec.
7:0	R/W/L	00h	<b>Self Refresh:</b> This value is input to the filter if in a clock the corresponding rank is in self refresh.



## 20.7.13 C0DTAEW - Channel 0 DRAM Rank Throttling Active Event

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 1280-1287h  
 Default Value: 0000000000000000h  
 Access: RO; R/W/L  
 Size: 64 bits

Programmable Event weights that are input into the averaging filter. Each event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length and 2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks. (G)MCH implements four, independent filters, one per rank. In the clock (G)MCH asserts a command to the DRAM (via CS# assertion) based on the command type the one of the weights specified in this register is added to the weight specified in the previous register and input to the filter.

Bit	Access	Default Value	Description
63:56	RO	00h	<b>Read with AP</b>
55:48	RO	00h	<b>Write with AP</b>
47:40	R/W/L	00h	<b>Read</b>
39:32	R/W/L	00h	<b>Write</b>
31:24	R/W/L	00h	<b>Precharge – All</b>
23:16	R/W/L	00h	<b>Precharge</b>
15:8	R/W/L	00h	<b>Activate</b>
7:0	R/W/L	00h	<b>Refresh</b>



## 20.7.14 C0DTC - Channel 0 DRAM Throttling Control

B/D/F/Type: 0/0/0/MCHBAR Chipset  
Address Offset: 1288-128Bh  
Default Value: 00000000h  
Access: RO; R/W/L  
Size: 32 bits

Programmable Event weights are input into the averaging filter. Each Event weight is a normalized 8-bit value that the BIOS must program. The BIOS must account for burst length and 2N rule considerations. It is also possible for BIOS to take into account type loading variations of memory caused as a function of memory types and population of ranks.

Bit	Access	Default Value	Description
31	R/W/L	0b	<b>Reserved</b>
30	R/W/L	0b	<b>Reserved</b>
29	R/W/L	0b	<b>Reserved</b>
28:25	RO	0h	<b>Reserved</b>
24:22	R/W/L	000b	<b>Reserved</b>
21	R/W/L	0b	<b>(G)MCH Bandwidth-Based Throttling Enable:</b> 0 = Bandwidth Threshold WAB (Weighted Avg. Bandwidth) is not used for throttling. 1 = Bandwidth Threshold (WAB) is used for throttling. If both Bandwidth-based and thermal sensor-based throttling modes are on and the thermal sensor trips, the WAT (Weighted Avg. Threshold) Thermal threshold are used for throttling.
20	R/W/L	0b	<b>(G)MCH Thermal Sensor Trip Enable:</b> 0 = (G)MCH throttling is not initiated when the (G)MCH thermal sensor trips. 1 = (G)MCH throttling is initiated when the (G)MCH thermal sensor trips and the Filter output is equal to or exceeds thermal threshold WAT.
19	RO	0b	<b>Reserved</b>
18:16	R/W/L	000b	<b>Reserved</b>
15:8	R/W/L	00h	<b>WAB:</b> Threshold allowed per clock for bandwidth based throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.
7:0	R/W/L	00h	<b>WAT:</b> Threshold allowed per clock during for thermal sensor enabled throttling. (G)MCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.



## 20.7.15 TSWDT0 - GMCH Thermal Sensor Watch Dog Timer 0

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1290-1293h
Default Value:	00000000h
Access:	RO; R/W/L
Size:	32 bits

When thermal sensor is indicating thermally hot tripped and GMCH throttling is enabled, this register allows the value in the TSWDT0 [Delta] field to affect the impact of the C0GTC [WAT] throttling threshold whenever the TSWDT0 WDT times out.

The thermal sensor lock bit locks the following register bits.

Bit	Access	Default Value	RST/PWR	Description
31:29	R/W/L	000b	Core	<b>Reserved</b>
28:21	R/W/L	00h	Core	<b>Clamp ()</b> : This register contains the lowest value that WATeff is allowed to reach. Clamp must be a value no greater than WAT.
20:16	R/W/L	0000b	Core	<b>Reserved</b>
15:3	RO	00h	Core	<b>Reserved</b>
2:0	R/W/L	0h	Core	<b>Reserved</b>



### 20.7.16 C0DTWDT - Channel 0 DRAM Thermal Sensor Watch Dog Timer

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	12B4-12B7h
Default Value:	00000000h
Access:	RO; R/W/L
Size:	32 bits

When external thermal sensor is indicating thermally hot tripped and DRAM throttling is enabled, this register allows the value in the [Delta] field to affect the impact of the CxDTC [WAT] throttling threshold whenever the WDT times out. If the actual average memory traffic is at a level less than the clamp value during the thermal trip, memory traffic will not be affected.

The Thermal Sensor Lock bit locks the following register bits.

Bit	Access	Default Value	Description
31:29	R/W/L	000b	<b>Reserved</b>
28:21	R/W/L	00h	<b>Clamp (Clamp):</b> This register contains the lowest value that WATeff is allowed to reach. Clamp must be a value no greater than WAT.
20:16	R/W/L	00000b	<b>Reserved</b>
15:8	RO	00h	<b>Reserved</b>
7:3	RO	00h	<b>Reserved</b>
2:0	R/W/L	000b	<b>Reserved</b>

### 20.7.17 C1DRB01 - Channel 1 DRAM Rank Boundary 0/1

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1300-1303h
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DRB01.

### 20.7.18 C1DRA - Channel 1 DRAM Rank 0,1 Attribute

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1308-130Bh
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DRA.



### 20.7.19 C1DCLKDIS - Channel 1 DRAM Clock Disable

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	130C-130Fh
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DCLKDIS.

### 20.7.20 C1DRT0 - Channel 1 DRAM Timing Register 0

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1310-1313h
Default Value:	34B10461h
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DRT0.

### 20.7.21 C1DRT1 - Channel 1 DRAM Timing Register 1

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1314-1317h
Default Value:	11E08463h
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DRT1.

### 20.7.22 C1DRT2 - Channel 1 DRAM Timing Register 2

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1318-131Bh
Default Value:	2200105Fh
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DRT2.

### 20.7.23 C1DRT3 - Channel 1 DRAM Timing Register 3

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	131C-131Fh
Default Value:	01056102h
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DRT3.



#### 20.7.24 C1DRC0 - Channel 1 DRAM Controller Mode 0

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1330-1333h
Default Value:	4F000008h
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DRC0.

#### 20.7.25 C1DRC1 - Channel 1 DRAM Controller Mode 1

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1334-1337h
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

Bit settings for this register are identical to C0DRC1.

#### 20.7.26 C1DRC2 - Channel 1 DRAM Controller Mode 2

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1338-133Bh
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

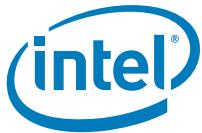
Bit settings for this register are identical to C0DRC2.



## 20.7.27 C1GTEW - Channel 1 GMCH Throttling Event Weights.

B/D/F/Type: 0/0/0/MCHBAR Chipset  
 Address Offset: 1370-1373h  
 Default Value: 00000000h  
 Access: R/W/L  
 Size: 32 bits

Bit	Access	Default Value	Bit
31:24	R/W/L	00h	<b>Read Weight ()</b> : This value is input to the filter if in a given clock there is a valid read command being issued on the memory bus.
23:16	R/W/L	00h	<b>Write Weight ()</b> : This value is input to the filter if in a given clock there is a valid write command being issued on the memory bus.
15:8	R/W/L	00h	<b>Command Weight ()</b> : This value is input to the filter if in a given clock there is a valid command other than a read or a write being issued on the memory bus.
7:0	R/W/L	00h	<b>Idle Weight ()</b> : This value is input to the filter if in a given clock there is no command being issued on the memory bus. If command and address are tri-stated a value of "0" is input to the filter. If command and address are under reduced drive strength this value is divided by 2 and input to the filter.



### 20.7.28 C1GTC - Channel 1 GMCH Throttling Control

B/D/F/Type: 0/0/0/MCHBAR Chipset  
Address Offset: 1374-1377h  
Default Value: 00000000h  
Access: RO; R/W/L  
Size: 32 bits

Bit	Access	Default Value	Bit
31:22	RO	0h	<b>Reserved</b>
21	R/W/L	0b	<b>GMCH Bandwidth-Based Throttling Enable (GBTE):</b> 0 = Bandwidth Threshold (WAB) is not used for throttling. 1 = Bandwidth Threshold (WAB) is used for throttling. If both bandwidth-based and thermal sensor based throttling modes are on and the thermal sensor trips, the WAT Thermal threshold are used for throttling.
20	R/W/L	0b	<b>GMCH Thermal Sensor Trip Enable ():</b> 0 = GMCH throttling is not initiated when the GMCH thermal sensor trips. 1 = GMCH throttling is initiated when the GMCH thermal sensor trips and the Filter output is equal to or exceeds thermal threshold WAT.
19:16	RO	0000b	<b>Reserved</b>
15:8	R/W/L	00h	<b>WAB ():</b> Threshold allowed per clock for bandwidth based throttling. GMCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.
7:0	R/W/L	00h	<b>WAT ():</b> Threshold allowed per clock during thermal sensor enabled throttling. GMCH does not allow transactions to proceed on the DDR bus if the output of the filter equals or exceeds this value.

### 20.7.29 C1DTPEW - Channel 1 DRAM Rank Throttling Passive Event

B/D/F/Type: 0/0/0/MCHBAR Chipset  
Address Offset: 1378-137Fh  
Default Value: 0000000000000000h  
Access: RO; R/W/L  
Size: 64 bits

Bit settings for this register are identical to C0DTPEW.

### 20.7.30 C1DTAEW - Channel 1 DRAM Rank Throttling Active Event

B/D/F/Type: 0/0/0/MCHBAR Chipset  
Address Offset: 1380-1387h  
Default Value: 0000000000000000h  
Access: RO; R/W/L  
Size: 64 bits

Bit settings for this register are identical to C0DTAEW.



### 20.7.31 C1DTC - Channel 1 DRAM Throttling Control

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1388-138Bh
Default Value:	00000000h
Access:	RO; R/W/L
Size:	32 bits

Bit settings for this register are identical to C0DTC.

### 20.7.32 TSWDT1 - GMCH Thermal Sensor Watch Dog Timer 1

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	1390-1393h
Default Value:	00000000h
Access:	RO; R/W/L
Size:	32 bits

Bit settings for this register are identical to TSWDT0.

### 20.7.33 C1DTWDT - Channel 1 DRAM Thermal Sensor Watch Dog Timer

B/D/F/Type:	0/0/0/MCHBAR Chipset
Address Offset:	13B4-13B7h
Default Value:	00000000h
Access:	RO; R/W/L
Size:	32 bits

Bit settings for this register are identical to C0DTWDT.



## 20.8 DMI RCRB

This section describes the mapped register for DMI. The DMIBAR register provides the base address or these registers.

This Root Complex Register Block (RCRB) controls (G)MCH -ICH9M serial interconnect. An RCRB is required for configuration and control of element that are located internal to root complex that are not directly associated with a PCI Express device. The base address of this space is programmed in DMIBAR in Device 0 config space.

All RCRB register spaces needs to remain organized as they are here. The Virtual Channel capabilities (or at least the first PCI Express Extended Capability) must begin at the 0h offset of the 4-K area pointed to by the associated BAR. This is a *PCI Express Specification 1.1* requirement.

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
DMI Virtual Channel Enhanced Capability	DMIVCECH	0	3	04010002h	RO
DMI Port VC Capability Register 1	DMIPVCCAP1	4	7	00000001h	RO; R/W
DMI Port VC Capability Register 2	DMIPVCCAP2	8	B	00000001h	RO
DMI Port VC Control	DMIPVCCTL	C	D	0000h	RO; R/W
DMI VC0 Resource Capability	DMIVC0RCAP	10	13	00000001h	RO
DMI VC0 Resource Control	DMIVC0RCTL0	14	17	80000FFh	RO; R/W
DMI VC0 Resource Status	DMIVC0RSTS	1A	1B	0002h	RO
DMI VC1 Resource Capability	DMIVC1RCAP	1C	1F	00008001h	RO
DMI VC1 Resource Control	DMIVC1RCTL1	20	23	01000000h	RO; R/W
DMI VC1 Resource Status	DMIVC1RSTS	26	27	0002h	RO
Reserved		28	33		
DMI Root Complex Link Declaration	DMIRCLDECH	40	43	08010005h	RO
DMI Element Self Description	DMIESD	44	47	01000202h	RO; R/W
DMI Link Entry 1 Description	DMILE1D	50	53	00000000h	RO; R/W
DMI Link Entry 1 Address	DMILE1A	58	5F	0000000000 000000h	RO; R/W
DMI Link Entry 2 Description	DMILE2D	60	63	00000000h	RO; R/W
DMI Link Entry 2 Address	DMILE2A	68	6F	0000000000 000000h	RO; R/W
DMI Root Complex Internal Link Control	DMIRCILCECH	80	83	00010006h	RO
DMI Link Capabilities	DMILCAP	84	87	00012C41h	RO; R/W
DMI Link Control	DMILCTL	88	89	0000h	RO; R/W
DMI Link Status	DMILSTS	8A	8B	0001h	RO
Reserved		F0	33B		



## 20.8.1 DMIVCECH - DMI Virtual Channel Enhanced Capability

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	0-3h
Default Value:	04010002h
Access:	RO
Size:	32 bits

Indicates DMI Virtual Channel capabilities.

Bit	Access	Default Value	Description
31:20	RO	040h	<b>PointertoNextCapability (PNC):</b> This field contains the offset to the next PCI Express* capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	RO	1h	<b>PCIExpressVirtualChannelCapabilityVersion (PCIEVCCV):</b> Hardwired to 1 to indicate compliances with the 1.0 version of the <i>PCI Express Specification</i> .
15:0	RO	0002h	<b>ExtendedCapabilityID (ECID):</b> Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

## 20.8.2 DMIPVCCAP1 - DMI Port VC Capability Register 1

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	4-7h
Default Value:	00000001h
Access:	RO; R/WO
Size:	32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	0000000h	<b>Reserved</b>
6:4	RO	000b	<b>LowPriorityExtendedVCCount (LPEVCC):</b> Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	<b>Reserved</b>
2:0	R/WO	001b	<b>ExtendedVCCount (EVCC):</b> Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel is not included in this count.



### 20.8.3 DMIPVCCAP2 - DMI Port VC Capability Register 2

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	8-Bh
Default Value:	00000001h
Access:	RO
Size:	32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	<b>Reserved</b>
23:8	RO	0000h	<b>Reserved</b>
7:0	RO	01h	<b>VCArbitrationCapability (VCAC):</b> Indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority and VC0 is the lowest priority.

### 20.8.4 DMIPVCCTL - DMI Port VC Control

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	C-Dh
Default Value:	0000h
Access:	RO; R/W
Size:	16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	<b>Reserved</b>
3:1	R/W	000b	<b>VCArbitrationSelect (VCAS):</b> This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled. 000 = Hardware fixed arbitration scheme, e.g., Round Robin Others = Reserved. See the <i>PCI Express Specification</i> for more details
0	RO	0b	<b>ReservedforLoadVCArbitrationTable</b>



## 20.8.5 DMIVC0RCAP - DMI VC0 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 10-13h  
 Default Value: 00000001h  
 Access: RO  
 Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	00h	<b>ReservedforPortArbitrationTableOffset:</b>
23	RO	0b	<b>Reserved</b>
22:16	RO	00h	<b>ReservedforMaximumTimeSlots:</b>
15	RO	0b	<b>RejectSnoopTransactions (REJSNPT):</b> 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	<b>Reserved</b>
7:0	RO	01h	<b>PortArbitrationCapability (PAC):</b> Having only Bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

## 20.8.6 DMIVC0RCTL0 - DMI VC0 Resource Control

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 14-17h  
 Default Value: 800000FFh  
 Access: RO; R/W  
 Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

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Bit	Access	Default Value	Description
31	RO	1b	<b>VirtualChannel0Enable (VC0E):</b> For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	<b>Reserved</b>
26:24	RO	000b	<b>VirtualChannel0ID (VC0ID):</b> Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	RO	0h	<b>Reserved</b>
19:17	R/W	000b	<b>PortArbitrationSelect (PAS):</b> Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only Bit 0 of that field is asserted. This field will always be programmed to 1.



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Bit	Access	Default Value	Description
16:8	RO	000h	<b>Reserved</b>
7:1	R/W	7Fh	<b>TrafficClass/VirtualChannel0Map (TCVC0M):</b> Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when Bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	<b>TrafficClass0/VirtualChannel0Map (TC0VC0M):</b> Traffic Class 0 is always routed to VC0.

### 20.8.7 DMIVC0RSTS - DMI VC0 Resource Status

B/D/F/Type: 0/0/0/DMIBAR  
Address Offset: 1A-1Bh  
Default Value: 0002h  
Access: RO  
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	<b>Reserved</b>
1	RO	1b	<b>VirtualChannel0NegotiationPending (VC0NP):</b> 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. BIOS Requirement: Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	<b>Reserved</b>



## 20.8.8 DMIVC1RCAP - DMI VC1 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 1C-1Fh  
 Default Value: 00008001h  
 Access: RO  
 Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	00h	<b>Reserved</b>
23	RO	0b	<b>Reserved</b>
22:16	RO	00h	<b>Reserved</b>
15	RO	1b	<b>RejectSnoopTransactions (REJSNPT):</b> 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	<b>Reserved</b>
7:0	RO	01h	<b>PortArbitrationCapability (PAC):</b> Having only Bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

## 20.8.9 DMIVC1RCTL1 - DMI VC1 Resource Control

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 20-23h  
 Default Value: 01000000h  
 Access: RO; R/W  
 Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.



Bit	Access	Default Value	Description
31	R/W	0b	<b>VirtualChannel1Enable (VC1E):</b> 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. <b>BIOS Requirement:</b> <ol style="list-style-type: none"><li>1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link.</li><li>2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link.</li><li>3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled.</li><li>4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.</li></ol>
30:27	RO	0h	<b>Reserved</b>
26:24	R/W	001b	<b>VirtualChannel1ID (VC1ID):</b> Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20	RO	0h	<b>Reserved</b>
19:17	R/W	000b	<b>PortArbitrationSelect (PAS):</b> Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16:8	RO	000h	<b>Reserved</b>
7:1	R/W	00h	<b>TrafficClass/VirtualChannel1Map (TCVC1M):</b> Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when Bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	0b	<b>TrafficClass0/VirtualChannel1Map (TC0VC1M):</b> Traffic Class 0 is always routed to VC0.



## 20.8.10 DMIVC1RSTS - DMI VC1 Resource Status

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 26-27h  
 Default Value: 0002h  
 Access: RO  
 Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	<b>Reserved:</b> Reserved and Zero for future implementations. Software must use 0 for writes to these bits.
1	RO	1b	<b>VirtualChannel1NegotiationPending (VC1NP):</b> 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	<b>Reserved</b>



### 20.8.11 DMIRCLDECH - DMI Root Complex Link Declaration

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	40-43h
Default Value:	08010005h
Access:	RO
Size:	32 bits

This capability declares links from the respective element to other elements of the root complex component to which it belongs and to an element in another root complex component. See the *PCI Express Specification* for link/topology declaration requirements.

Bit	Access	Default Value	Description
31:20	RO	080h	<b>PointertoNextCapability (PNC):</b> This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Internal Link Control Capability).
19:16	RO	1h	<b>LinkDeclarationCapabilityVersion (LDCV):</b> Hardwired to 1 to indicate compliances with the 1.0 version of the <i>PCI Express Specification</i> .
15:0	RO	0005h	<b>ExtendedCapabilityID (ECID):</b> Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.



## 20.8.12 DMIESD - DMI Element Self Description

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 44-47h  
 Default Value: 01000202h  
 Access: RO; R/WO  
 Size: 32 bits

Provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
31:24	RO	01h	<b>PortNumber (PORTNUM):</b> Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	R/WO	00h	<b>ComponentID (CID):</b> Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the <i>PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> .
15:8	RO	02h	<b>NumberOfLinkEntries (NLE):</b> Indicates the number of link entries following the Element Self Description. This field reports 2 (one for MCH egress port to main memory and one to egress port belonging to ICH on other side of internal link).
7:4	RO	0h	<b>Reserved</b>
3:0	RO	2h	<b>ElementType (ETYP):</b> Indicates the type of the Root Complex Element. Value of 2 h represents an Internal Root Complex Link (DMI).



### 20.8.13 DMILE1D - DMI Link Entry 1 Description

B/D/F/Type: 0/0/0/DMIBAR  
Address Offset: 50-53h  
Default Value: 00000000h  
Access: R/WO; RO  
Size: 32 bits

The first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	R/WO	00h	<b>TargetPortNumber (TPN):</b> Specifies the port number associated with the element targeted by this link entry (egress port of ICH). The target port number is with respect to the component that contains this element as specified by the target component ID. This can be programmed by BIOS, but the default value will likely be correct because the DMI RCRB in the ICH will likely be associated with the default egress port for the ICH meaning it will be assigned port number 0.
23:16	R/WO	00h	<b>TargetComponentID (TCID):</b> Identifies the physical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the <i>PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> .
15:2	RO	0000h	<b>Reserved</b>
1	RO	0b	<b>LinkType (LTYP):</b> Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	<b>LinkValid (LV):</b> 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.



## 20.8.14 DMILE1A - DMI Link Entry 1 Address

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 58-5Fh  
 Default Value: 0000000000000000h  
 Access: RO; R/WO  
 Size: 64 bits  
 Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	<b>Reserved:</b> Reserved for Link Address high order 32 bits.
31:12	R/WO	00000h	<b>LinkAddress (LA):</b> Memory mapped base address of the RCRB that is the target element (egress port of ICH) for this link entry.
11:0	RO	000h	<b>Reserved</b>

## 20.8.15 DMILE2D - DMI Link Entry 2 Description

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 60-63h  
 Default Value: 00000000h  
 Access: RO; R/WO  
 Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	00h	<b>TargetPortNumber (TPN):</b> Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	<b>TargetComponentID (TCID):</b> Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the <i>PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> .
15:2	RO	0000h	<b>Reserved</b>
1	RO	0b	<b>LinkType (LTYP):</b> Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	<b>LinkValid (LV):</b> 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.



### 20.8.16 DMILE2A - DMI Link Entry 2 Address

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	68-6Fh
Default Value:	0000000000000000h
Access:	RO; R/WO
Size:	64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	<b>Reserved:</b> Reserved for Link Address high order 32 bits.
31:12	R/WO	00000h	<b>LinkAddress (LA):</b> Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	000h	<b>Reserved</b>

### 20.8.17 DMIRCILCECH - DMI Root Complex Internal Link Control

B/D/F/Type:	0/0/0/DMIBAR
Address Offset:	80-83h
Default Value:	00010006h
Access:	RO
Size:	32 bits

This capability contains controls for the Root Complex Internal Link known as DMI.

Bit	Access	Default Value	Description
31:20	RO	000h	<b>PointertoNextCapability (PNC):</b> This value terminates the PCI Express extended capabilities list associated with this RCRB.
19:16	RO	1h	<b>LinkDeclarationCapabilityVersion (LDCV):</b> Hardwired to 1 to indicate compliances with the 1.0 version of the <i>PCI Express Specification</i> .
15:0	RO	0006h	<b>ExtendedCapabilityID (ECID):</b> Value of 0006 h identifies this linked list item (capability structure) as being for PCI Express Internal Link Control Capability.



## 20.8.18 DMILCAP - DMI Link Capabilities

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 84-87h  
 Default Value: 00012C41h  
 Access: RO; R/WO  
 Size: 32 bits

Indicates DMI specific capabilities.

Bit	Access	Default Value	Description
31:18	RO	0000h	<b>Reserved</b>
17:15	R/WO	010b	<b>Reserved</b>
14:12	R/WO	010b	<b>Reserved</b>
11:10	RO	11b	<b>ActiveStateLinkPMSupport (ASLPMS):</b> 11 = L0s & L1 entry supported.
9:4	RO	04h	<b>MaxLinkWidth (MLW):</b> Indicates the maximum number of lanes supported for this link
3:0	RO	1h	<b>MaxLinkSpeed (MLS):</b> Hardwired to indicate 2.5 Gb/s.

## 20.8.19 DMILCTL - DMI Link Control

B/D/F/Type: 0/0/0/DMIBAR  
 Address Offset: 88-89h  
 Default Value: 0000h  
 Access: RO; R/W  
 Size: 16 bits

Allows control of DMI.

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Bit	Access	Default Value	Description
15:8	RO	00h	<b>Reserved</b>
7	R/W	0b	<b>ExtendedSynch (EXTSYNC):</b> 0 = Standard Fast Training Sequence (FTS). 1 = Forces extended transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP Ordered Set prior to entering L0, and the transmission of 1024 TS1 ordered sets in the RecoveryRcvrLock state prior to entering the RecoveryRcvrCfg state. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.



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Bit	Access	Default Value	Description
6:3	RO	0000b	<b>Reserved</b>
2	R/W	0b	<b>Reserved</b>
1:0	R/W	00b	<b>ActiveStatePowerManagementSupport (ASPMs):</b> Controls the level of active state power management supported on the given link. 00 = Disabled 01 = L0s Entry Supported 10 = Reserved 11 = L0s and L1 Entry Supported

## 20.8.20 DMILSTS - DMI Link Status

B/D/F/Type: 0/0/0/DMIBAR  
Address Offset: 8A-8Bh  
Default Value: 0001h  
Access: RO  
Size: 16 bits

Indicates DMI status.

Bit	Access	Default Value	Description								
15:10	RO	00h	<b>Reserved</b>								
9:4	RO	00h	<b>Negotiated Width (NWID):</b> Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed).  <table border="1"><tr><td>0h:</td><td>Reserved</td></tr><tr><td>1h:</td><td>X1</td></tr><tr><td>2h:</td><td>X2</td></tr><tr><td>4h:</td><td>X4</td></tr></table> All other encodings are reserved.	0h:	Reserved	1h:	X1	2h:	X2	4h:	X4
0h:	Reserved										
1h:	X1										
2h:	X2										
4h:	X4										
3:0	RO	1h	<b>Negotiated Speed (NSPD):</b> Indicates negotiated link speed. <ul style="list-style-type: none"><li>1h: 2.5 Gb/s</li></ul> All other encodings are reserved.								



## 20.9 Egress Port (EP) RCRB

This Root Complex Register Block (RCRB) controls the port arbitration that is based on the *PCI Express Specification*. Port arbitration is done for all PCI Express-based isochronous requests (always on Virtual Channel 1) before being submitted to the main memory arbiter. The base address of this space is programmed in the EPBAR in Device-0 config space.

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
EP Virtual Channel Enhanced Capability	EPVCECH	0	3	04010002h	RO
EP Port VC Capability Register 1	EPPVCCAP1	4	7	00000401h	RO; R/WO
EP Port VC Capability Register 2	EPPVCCAP2	8	B	00000001h	RO
EP Port VC Control	EPPVCCTL	C	D	0000h	RO; R/W
EP VC 0 Resource Capability	EPVC0RCAP	10	13	00000001h	RO
EP VC 0 Resource Control	EPVC0RCTL	14	17	800000FFh	RO; R/W
EP VC 0 Resource Status	EPVC0RSTS	1A	1B	0000h	RO
EP VC 1 Resource Capability	EPVC1RCAP	1C	1F	10008010h	RO; R/WO
EP VC 1 Resource Control	EPVC1RCTL	20	23	01080000h	RO; R/W; R/W/S
EP VC 1 Resource Status	EPVC1RSTS	26	27	0000h	RO
EP VC 1 Maximum Number of Time Slots	EPVC1MTS	28	2B	04050609h	R/W
EP VC 1 Isoch Timing Control	EPVC1ITC	2C	2F	00000000h	RO; R/W
EP VC 1 Isoch Slot Time	EPVC1IST	38	3F	000000000000000000h	R/W
EP Root Complex Link Declaration	EPRCLDECH	40	43	00010005h	RO
EP Element Self Description	EPESD	44	47	00000201h	RO; R/WO
EP Link Entry 1 Description	EPLIE1D	50	53	01000000h	RO; R/WO
EP Link Entry 1 Address	EPLIE1A	58	5F	000000000000000000h	RO; R/WO
EP Link Entry 2 Description	EPLIE2D	60	63	02000002h	RO; R/WO
EP Link Entry 2 Address	EPLIE2A	68	6F	000000000000008000h	RO
Port Arbitration Table	PORTARB	100	11F	0000000000000000 0000000000000000 0000000000000000 0000000000000000 00000000h	R/W



### 20.9.1 EPVCECH - EP Virtual Channel Enhanced Capability

B/D/F/Type:	0/0/0/EPBAR
Address Offset:	0-3h
Default Value:	04010002h
Access:	RO
Size:	32 bits

Indicates Egress Port Virtual Channel capabilities.

Bit	Access	Default Value	Description
31:20	RO	040h	<b>Pointer to Next Capability (PNC):</b> This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability). Bits [21:20] are reserved and software must mask them to allow for future uses of these bits.
19:16	RO	1h	<b>PCI Express Virtual Channel Capability Version (PCIEVCCV):</b> Hardwired to 1 to indicate compliances with the <i>PCI Express Specification</i> .
15:0	RO	0002h	<b>Extended Capability ID (ECID):</b> Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

### 20.9.2 EPPVCCAP1 - EP Port VC Capability Register 1

B/D/F/Type:	0/0/0/EPBAR
Address Offset:	4-7h
Default Value:	00000401h
Access:	RO; R/WO
Size:	32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

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Bit	Access	Default Value	Description
31:12	RO	00000h	<b>Reserved</b>
11:10	RO	01b	<b>Port Arbitration Table Entry Size (PATES):</b> Indicates that the size of the Port Arbitration table entry is 2 bits.
9:8	RO	00b	<b>Reference Clock (RC):</b> Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. 00 = 100 ns
7	RO	0b	<b>Reserved</b>



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Bit	Access	Default Value	Description
6:4	RO	000b	<b>Low Priority Extended VC Count (LPEVCC):</b> Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	<b>Reserved</b>
2:0	R/WO	001b	<b>Extended VC Count (EVCC):</b> Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

### 20.9.3 EPPVCCAP2 - EP Port VC Capability Register 2

B/D/F/Type: 0/0/0/EPBAR  
 Address Offset: 8-Bh  
 Default Value: 00000001h  
 Access: RO  
 Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	<b>Reserved</b>
23:8	RO	0000h	<b>Reserved</b>
7:0	RO	01h	<b>VC Arbitration Capability (VCAC):</b> Indicates the VC arbitration is fixed in the root complex. VC1 is the highest priority, VCp (private VC) is next in priority, and VC0 is the lowest priority.



#### 20.9.4 EPPVCCTL - EP Port VC Control

B/D/F/Type: 0/0/0/EPBAR  
Address Offset: C-Dh  
Default Value: 0000h  
Access: RO; R/W  
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	<b>Reserved</b>
3:1	R/W	000b	<b>VC Arbitration Select (VCAS):</b> This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled.
0	RO	0b	<b>Reserved for Load VC Arbitration Table</b>

#### 20.9.5 EPVC0RCAP - EP VC 0 Resource Capability

B/D/F/Type: 0/0/0/EPBAR  
Address Offset: 10-13h  
Default Value: 00000001h  
Access: RO  
Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	00h	<b>Reserved</b>
23	RO	0b	<b>Reserved</b>
22:16	RO	00h	<b>Reserved</b>
15	RO	0b	<b>Reject Snoop Transactions (RSNPT):</b> 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	<b>Reserved</b>
7:0	RO	01h	<b>Port Arbitration Capability (PAC):</b> Indicates types of Port Arbitration supported by this VC0 resource. The default value of 01h indicates that the only port arbitration capability for VC0 is non-configurable, hardware-fixed arbitration scheme.



## 20.9.6 EPVC0RCTL - EP VC 0 Resource Control

B/D/F/Type: 0/0/0/EPBAR  
 Address Offset: 14-17h  
 Default Value: 800000FFh  
 Access: RO; R/W  
 Size: 32 bits

Controls the resources associated with Egress Port Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	<b>VC0 Enable (VC0E):</b> For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	<b>Reserved</b>
26:24	RO	000b	<b>VC0 ID (VC0ID):</b> Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	RO	0h	<b>Reserved</b>
19:17	RO	000b	<b>Port Arbitration Select (PAS):</b> This field configures the VC resource to provide a particular Port Arbitration service. The value of 0h corresponds to the bit position of the only asserted bit in the Port Arbitration Capability field.
16:8	RO	000h	<b>Reserved</b>
7:1	R/W	7Fh	<b>TC/VC0 Map (TCVCOM):</b> Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when Bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	<b>TC0/VC0 Map (TC0VC0M):</b> Traffic Class 0 is always routed to VC0.



### 20.9.7 EPVC0RSTS - EP VC 0 Resource Status

B/D/F/Type: 0/0/0/EPBAR  
Address Offset: 1A-1Bh  
Default Value: 0000h  
Access: RO  
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	<b>Reserved</b>
1	RO	0b	<b>VC0 Negotiation Pending (VC0NP):</b> 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). For this default VC, this bit indicates the status of the process of Flow Control initialization. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	<b>Reserved</b>



## 20.9.8 EPVC1RCAP - EP VC 1 Resource Capability

B/D/F/Type: 0/0/0/EPBAR  
 Address Offset: 1C-1Fh  
 Default Value: 10008010h  
 Access: RO; R/WO  
 Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	10h	<b>Port Arbitration Table Offset (PATO):</b> Indicates the location of the Port Arbitration Table associated with the Egress Port VC1. This field contains the zero-based offset of the table in DQWORDs (16 bytes) from the base address of the Virtual Channel Capability Structure. The default value of 10h translates to the Port Arbitration Table beginning at offset 100h.
23	RO	0b	<b>Reserved</b>
22:16	R/WO	00h	<b>Maximum Time Slots (MTS):</b> Indicates the maximum number of timeslots (minus one) that the VC resource is capable of supporting when it is configured for time-based WRR Port Arbitration. See the EP VC 1 Maximum Number of Time Slots register from which system initialization software will select the appropriate value for this field.
15	RO	1b	<b>Reject Snoop Transactions (RSNPT):</b> 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO	00h	<b>Reserved</b>
7:0	RO	10h	<b>Port Arbitration Capability (PAC):</b> Indicates types of Port Arbitration supported by this VC1 resource. The default value of 10h indicates that only Bit 4 is set, reporting as our only port arbitration capability Time-Based Weighted Round Robin (WRR) arbitration with 128 phases.



## 20.9.9 EPVC1RCTL - EP VC 1 Resource Control

B/D/F/Type: 0/0/0/EPBAR  
Address Offset: 20-23h  
Default Value: 01080000h  
Access: RO; R/W; R/W/S  
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

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Bit	Access	Default Value	Description
31	R/W	0b	<b>VC1 Enable (VC1E):</b> This bit will be ignored by the hardware. The bit is R/W for specification compliance, but writing to it will result in no behavior change in the hardware (other than the bit value reflecting the written value). 0 = Virtual Channel is disabled. 1 = Virtual Channel is enabled. See exceptions in note below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. <b>NOTES:</b> <ol style="list-style-type: none"><li>1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link.</li><li>2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link.</li><li>3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled.</li><li>4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.</li></ol>
30:27	RO	0h	<b>Reserved</b>
26:24	R/W	001b	<b>VC1 ID (VC1ID):</b> Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field cannot be modified when the VC is already enabled.
23:20	RO	0h	<b>Reserved</b>
19:17	R/W	100b	<b>Port Arbitration Select (PAS):</b> This field configures the VC resource to provide a particular Port Arbitration service. The default value of 4h corresponds to bit position of the only asserted bit in the Port Arbitration Capability field.



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Bit	Access	Default Value	Description
16	R/W/S	0b	<b>Load Port Arbitration Table (LPAT):</b> Software sets this bit (writes a 1) to signal hardware to update the Port Arbitration logic with new values stored in the Port Arbitration Table. Software uses the Port Arbitration Table Status bit to confirm whether the new values of Port Arbitration Table are completely latched by the arbitration logic. Clearing this bit has no effect. This bit always returns 0 when read.
15:8	RO	00h	<b>Reserved</b>
7:1	R/W	00h	<b>TC/VC1 Map (TCVC1M):</b> Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when Bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given link.
0	RO	0b	<b>TC0/VC1 Map (TC0VC1M):</b> Traffic Class 0 is always routed to VC0.

### 20.9.10 EPVC1RSTS - EP VC 1 Resource Status

B/D/F/Type: 0/0/0/EPBAR  
 Address Offset: 26-27h  
 Default Value: 0000h  
 Access: RO  
 Size: 16 bits

Reports the Virtual Channel specific status.

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Bit	Access	Default Value	Description
15:2	RO	0000h	<b>Reserved</b>
1	RO	0b	<b>VC1 Negotiation Pending (VC1NP):</b> 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). For this non-default Virtual Channel, software may use this bit when enabling or disabling the VC. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.



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Bit	Access	Default Value	Description
0	RO	0b	<b>Port Arbitration Table Status (PATS):</b> Indicates the coherency status of the Port Arbitration Table associated with EP VC1. 0 = Hardware has finished loading values stored in the Port Arbitration Table after software set the Load Port Arbitration Table field. 1 = An entry in the Port Arbitration Table is being written to by software. Note that this bit will never be set to the value of 1 because loading the Port Arbitration Table is Non-posted. It will not complete on the FSB until the table loading is finished.

### 20.9.11 EPVC1MTS - EP VC 1 Maximum Number of Time Slots

B/D/F/Type: 0/0/0/EPBAR  
Address Offset: 28-2Bh  
Default Value: 04050609h  
Access: R/W  
Size: 32 bits

The fields in this register reflect the maximum number of time slots supported by the (G)MCH for time based arbitration in various configurations.

### 20.9.12 EPVC1ITC - EP VC 1 Isoch Timing Control

B/D/F/Type: 0/0/0/EPBAR  
Address Offset: 2C-2Fh  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

This register reflects the number of common host clocks (Hclk) per Port Arbitration Table phase.

### 20.9.13 EPVC1IST - EP VC 1 Isoch Slot Time

B/D/F/Type: 0/0/0/EPBAR  
Address Offset: 38-3Fh  
Default Value: 0000000000000000h  
Access: R/W  
Size: 64 bits

This register reflects the number of common host clocks per time slot.

## 20.9.14 EPRCLDECH - EP Root Complex Link Declaration

B/D/F/Type: 0/0/0/EPBAR  
 Address Offset: 40-43h  
 Default Value: 00010005h  
 Access: RO  
 Size: 32 bits

This capability declares links from the respective element to other elements of the root complex component to which it belongs. See the *PCI Express Specification* for link/topology declaration requirements.

Bit	Access	Default Value	Description
31:20	RO	000h	<b>Pointer to Next Capability (PNC):</b> This value terminates the PCI Express extended capabilities list associated with this RCRB.
19:16	RO	1h	<b>Link Declaration Capability Version (LDCV):</b> Hardwired to 1 to indicate compliances with the 1.0 version of the <i>PCI Express Specification</i> .
15:0	RO	0005h	<b>Extended Capability ID (ECID):</b> Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.



## 20.9.15 EPESD - EP Element Self Description

B/D/F/Type: 0/0/0/EPBAR  
Address Offset: 44-47h  
Default Value: 00000201h  
Access: RO; R/WO  
Size: 32 bits

Provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
31:24	RO	00h	<b>Port Number (PN):</b> This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00 h indicates to configuration software that this is the default egress port.
23:16	R/WO	00h	<b>Component ID (CID):</b> Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the <i>PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> .
15:8	RO	02h	<b>Number of Link Entries (NLE):</b> Indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PCI Express graphics and DMI).
7:4	RO	0h	<b>Reserved</b>
3:0	RO	1h	<b>Element Type (ET):</b> Indicates the type of the Root Complex Element. Value of 1 h represents a port to system memory.



## 20.9.16 EPLE1D - EP Link Entry 1 Description

B/D/F/Type: 0/0/0/EPBAR  
 Address Offset: 50-53h  
 Default Value: 01000000h  
 Access: RO; R/WO  
 Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	01h	<b>Target Port Number (TPN):</b> Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	<b>Target Component ID (TCID):</b> Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the <i>PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> .
15:2	RO	0000h	<b>Reserved</b>
1	RO	0b	<b>Link Type (LTYP):</b> Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	<b>Link Valid (LV):</b> 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.



### 20.9.17 EPLE1A - EP Link Entry 1 Address

B/D/F/Type:	0/0/0/EPBAR
Address Offset:	58-5Fh
Default Value:	0000000000000000h
Access:	RO; R/WO
Size:	64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	<b>Reserved for Link Address High Order 32 Bits</b>
31:12	R/WO	00000h	<b>Link Address (LA):</b> Memory mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0	RO	000h	<b>Reserved</b>

### 20.9.18 EPLE2D - EP Link Entry 2 Description

B/D/F/Type:	0/0/0/EPBAR
Address Offset:	60-63h
Default Value:	02000002h
Access:	RO; R/WO
Size:	32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31:24	RO	02h	<b>Target Port Number (TPN):</b> Specifies the port number associated with the element targeted by this link entry (PCI Express graphics). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	<b>Target Component ID (TCID):</b> Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. BIOS Requirement: Must be initialized according to guidelines in the <i>PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> .
15:2	RO	0000h	<b>Reserved</b>
1	RO	1b	<b>Link Type (LTYP):</b> Indicates that the link points to configuration space of the integrated device which controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.



(Sheet 2 of 2)

<b>Bit</b>	<b>Access</b>	<b>Default Value</b>	<b>Description</b>
0	R/WO	0b	<p><b>Link Valid (LV):</b></p> <p>0 = Link Entry is not valid and will be ignored.</p> <p>1 = Link Entry specifies a valid link.</p>

## 20.9.19 EPLE2A - EP Link Entry 2 Address

B/D/F/Type:	0/0/0/EPBAR
Address Offset:	68-6Fh
Default Value:	0000000000008000h
Access:	RO
Size:	64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

<b>Bit</b>	<b>Access</b>	<b>Default Value</b>	<b>Description</b>
63:28	RO	00000000h	<b>Reserved for Configuration Space Base Address:</b> Not required if root complex has only one config space.
27:20	RO	00h	<b>Bus Number (BUSN)</b>
19:15	RO	00001b	<b>Device Number (DEVN):</b> Target for this link is PCI Express x16 port (Device 1).
14:12	RO	000b	<b>Function Number (FUNN)</b>
11:0	RO	000h	<b>Reserved</b>

## **20.9.20 PORTARB - Port Arbitration Table**

The Port Arbitration Table register is a read-write register array that is used to store the arbitration table for Port Arbitration of the Egress Port VC resource.

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***Device 0 Memory Mapped I/O Register***



## 21 PCI Express Graphics Device 1 Configuration Registers (D1:F0)

Device 1 contains the controls associated with the x16 root port that is the intended attach point for external graphics. It is typically referred to as PCI Express graphics port. It also functions as the virtual PCI-to-PCI bridge that was previously associated with AGP.

When reading the PCI Express “conceptual” registers such as these, you may not get a valid value unless the register value is stable.

The *PCI Express Specification* defines two types of reserved bits:

- Reserved and Preserved: Reserved for future R/W implementations; software must preserve value read for writes to these bits.
- Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to these bits.

**Note:** Unless explicitly documented as Reserved and Zero, all bits marked as Reserved are part of the Reserved and Preserved type which has historically been the typical definition for Reserved.

Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first disable the link, then program the registers, then re-enable the link (which will cause a full-retrain with the new settings).

### 21.1 PCI Express Graphics Device 1 Function 0 Configuration Registers

(Sheet 1 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID1	0	1	8086h	RO
Device Identification	DID1	2	3	2A41h	RO
PCI Command	PCICMD1	4	5	0000h	RO; R/W
PCI Status	PCISTS1	6	7	0010h	RO; R/WC
Revision Identification	RID1	8	8	00h	RO
Class Code	CC1	9	B	060400h	RO
Cache Line Size	CL1	C	C	00h	R/W
Header Type	HDR1	E	E	01h	RO
Primary Bus Number	PBUSN1	18	18	00h	RO
Secondary Bus Number	SBUSN1	19	19	00h	R/W
Subordinate Bus Number	SUBUSN1	1A	1A	00h	R/W
I/O Base Address	IOBASE1	1C	1C	F0h	RO; R/W
I/O Limit Address	IOLIMIT1	1D	1D	00h	RO; R/W



## (Sheet 2 of 3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Secondary Status	SSTS1	1E	1F	0000h	R/WC; RO
Memory Base Address	MBASE1	20	21	FFF0h	RO; R/W
Memory Limit Address	MLIMIT1	22	23	0000h	RO; R/W
Prefetchable Memory Base Address	PMBASE1	24	25	FFF1h	RO; R/W
Prefetchable Memory Limit Address	PMLIMIT1	26	27	0001h	RO; R/W
Prefetchable Memory Base Address	PMBASEU1	28	2B	0000000Fh	R/W
Prefetchable Memory Limit Address	PMLIMITU1	2C	2F	00000000h	R/W
Capabilities Pointer	CAPPTR1	34	34	88h	RO
Interrupt Line	INTRLINE1	3C	3C	00h	R/W
Interrupt Pin	INTRPIN1	3D	3D	01h	RO
Bridge Control	BCTRL1	3E	3F	0000h	RO; R/W
Capabilities List Control	CAPL	7F	7F	02h	RO; R/W
Power Management Capabilities	PM_CAPID1	80	83	C8039001h	RO
Power Management Control/ Status	PM_CS1	84	87	00000000h	RO; R/W/S; R/W
Subsystem ID and Vendor ID Capabilities	SS_CAPID	88	8B	0000800Dh	RO
Subsystem ID and Subsystem Vendor ID	SS	8C	8F	00008086h	R/WO
Message Signaled Interrupts Capability ID	MSI_CAPID	90	91	A005h	RO
Message Control	MC	92	93	0000h	RO; R/W
Message Address	MA	94	97	00000000h	RO; R/W
Message Data	MD	98	99	0000h	R/W
PCI Express Graphics Capability List	PEG_CAPL	A0	A1	0010h	RO
PCI Express Graphics Capabilities	PEG_CAP	A2	A3	0141h	RO; R/WO
Device Capabilities	DCAP	A4	A7	00008000h	RO
Device Control	DCTL	A8	A9	0000h	RO; R/W
Device Status	DSTS	AA	AB	0000h	RO; R/WC
Link Capabilities	LCAP	AC	AF	02012D01h	RO; R/WO
Link Control	LCTL	B0	B1	0040h	RO; R/W
Link Status	LSTS	B2	B3	1001h	RO
Slot Capabilities	SLOTCAP	B4	B7	00040040h	R/WO; RO
Slot Control	SLOTCTL	B8	B9	01C0h	RO; R/W



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Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Slot Status	SLOTSTS	BA	BB	0000h	RO; R/WC
Root Control	RCTL	BC	BD	0000h	RO; R/W
Root Status	RSTS	C0	C3	00000000h	RO; R/WC
PCI Express Graphics Legacy Control	PEGLC	EC	EF	00000000h	RO; R/W
PCI Express Graphics CFG1		F0	F3	00010000h	
Reserved		F3	FB		
PCI Express Graphics CFG2		FC	FF	00000000h	

### 21.1.1 VID1 - Vendor Identification

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 0-1h  
 Default Value: 8086h  
 Access: RO  
 Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	<b>Vendor Identification (VID1):</b> PCI standard identification for Intel.

### 21.1.2 DID1 - Device Identification

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 2-3h  
 Default Value: 2A41h  
 Access: RO  
 Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	2A41h	<b>Device Identification Number (DID1):</b> Identifier assigned to the (G)MCH Device 1.



### 21.1.3 PCICMD1 - PCI Command

B/D/F/Type: 0/1/0/PCI  
Address Offset: 4-5h  
Default Value: 0000h  
Access: RO; R/W  
Size: 16 bits

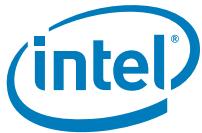
(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:11	RO	00h	<b>Reserved:</b>
10	R/W	0b	<b>INTA Assertion Disable (INTAAD):</b> 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be deasserted when this bit is set. Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD assert and deassert messages.
9	RO	0b	<b>Fast Back-to-Back Enable (FB2B):</b> Not Applicable or Implemented. Hardwired to 0.
8	R/W	0b	<b>SERR Message Enable (SERRE1):</b> Controls Device 1 SERR messaging. The (G)MCH communicates the SERRB condition by sending an SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control Register. 0 = The SERR message is generated by the (G)MCH for Device 1 only under conditions enabled individually through the Device Control Register. 1 = The (G)MCH is enabled to generate SERR messages which will be sent to the ICH for specific Device 1 error conditions generated/detected on the primary side of the virtual PCI to PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS1 register.
7	RO	0b	<b>Reserved:</b> Not Applicable or Implemented. Hardwired to 0.
6	R/W	0b	<b>Parity Error Enable (PERRE):</b> Controls whether or not the Master Data Parity Error bit in the PCI Status register can be set. 0 = Master Data Parity Error bit in PCI Status register <b>cannot</b> be set. 1 = Master Data Parity Error bit in PCI Status register <b>can</b> be set.
5	RO	0b	<b>VGA Palette Snoop (VGAPS):</b> Not Applicable or Implemented. Hardwired to 0.



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Bit	Access	Default Value	Description
4	RO	0b	<b>Memory Write and Invalidate Enable (MWIE):</b> Not Applicable or Implemented. Hardwired to 0.
3	RO	0b	<b>Special Cycle Enable (SCE):</b> Not Applicable or Implemented. Hardwired to 0.
2	R/W	0b	<b>Bus Master Enable (BME):</b> Controls the ability of the PCI Express graphics port to forward Memory and IO Read/Write Requests in the upstream direction. 0 = This device is prevented from making memory or IO requests to its primary bus. Note that according to the <i>PCI Express Specification</i> as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address 0 with byte enables deasserted. Reads will be forwarded to memory address 0 and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available. This bit does not affect forwarding of Completions from the primary interface to the secondary interface.
1	R/W	0b	<b>Memory Access Enable (MAE):</b> 0 = All of Device 1's memory space is disabled. 1 = Enable the Memory and Prefetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W	0b	<b>IO Access Enable (IOAE):</b> 0 = All of Device 1's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.



### 21.1.4 PCISTS1 - PCI Status

B/D/F/Type: 0/1/0/PCI  
Address Offset: 6-7h  
Default Value: 0010h  
Access: RO; R/WC  
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the virtual Host-PCI Express bridge embedded within the (G)MCH.

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Bit	Access	Default Value	Description
15	RO	0b	<b>Detected Parity Error (DPE):</b> Not Applicable or Implemented. Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device (we don't do error forwarding).
14	R/WC	0b	<b>Signaled System Error (SSE):</b> This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is '1'. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO	0b	<b>Received Master Abort Status (RMAS):</b> Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO	0b	<b>Received Target Abort Status (RTAS):</b> Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO	0b	<b>Signaled Target Abort Status (STAS):</b> Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO	00b	<b>DEVSELB Timing (DEVT):</b> This device is not the subtractively decoded device on Bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO	0b	<b>Master Data Parity Error (PMDPE):</b> There is no scenario where this bit will get set. The <i>PCI Express Specification</i> defines it as an R/WC, but for our implementation an RO definition behaves the same way and will meet all testing requirements.
7	RO	0b	<b>Fast Back-to-Back (FB2B):</b> Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	<b>Reserved:</b>
5	RO	0b	<b>66-/60-MHz Capability (CAP66):</b> Not Applicable or Implemented. Hardwired to 0.



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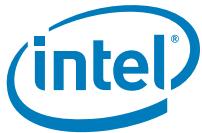
Bit	Access	Default Value	Description
4	RO	1b	<b>Capabilities List (CAPL):</b> Indicates that a capabilities list is present. Hardwired to 1.
3	RO	0b	<b>INTA Status (INTAS):</b> Indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and deassert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit. Note that INTA emulation interrupts received across the link are not reflected in this bit.
2:0	RO	000b	<b>Reserved</b>

### 21.1.5 RID1 - Revision Identification

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 8h  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

RID Definition: This register contains the revision number of the (G)MCH Device 0. Following PCI Reset, the SRID value is selected to be read. When a write occurs to this register, the write data is compared to the hardwired RID Select Key Value, which is 69h. If the data matches this key, a flag is set that enables the CRID value to be read through this register.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Revision Identification Number (RID1):</b> This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. 07h: B-3 stepping 09h: CR A-1 Stepping



### 21.1.6 CC1 - Class Code

B/D/F/Type:	0/1/0/PCI
Address Offset:	9-Bh
Default Value:	060400h
Access:	RO
Size:	24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access	Default Value	Description
23:16	RO	06h	<b>Base Class Code (BCC):</b> Indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO	04h	<b>Sub-Class Code (SUBCC):</b> Indicates the sub-class code for this device. The code is 04h indicating a PCI-to-PCI bridge.
7:0	RO	00h	<b>Programming Interface (PI):</b> Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

### 21.1.7 CL1 - Cache Line Size

B/D/F/Type:	0/1/0/PCI
Address Offset:	Ch
Default Value:	00h
Access:	R/W
Size:	8 bits

Bit	Access	Default Value	Description
7:0	R/W	00h	<b>Cache Line Size (Scratch pad):</b> Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.



### 21.1.8 B/D/F/Type: 0/1/0/PCI

Address Offset: Eh  
 Default Value: 01h  
 Access: RO  
 Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access	Default Value	Description
7:0	RO	01h	<b>Header Type Register (HDR):</b> Returns 01 to indicate that this is a single-function device with bridge header layout.

### 21.1.9 PBUSN1 - Primary Bus Number

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 18h  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

This register identifies that this “virtual” Host-PCI Express bridge is connected to PCI Bus 0.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Primary Bus Number (BUSD):</b> Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since Device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.



### 21.1.10 SBUSN1 - Secondary Bus Number

B/D/F/Type:	0/1/0/PCI
Address Offset:	19h
Default Value:	00h
Access:	R/W
Size:	8 bits

This register identifies the bus number assigned to the second bus side of the “virtual” bridge i.e., to PCI Express Graphics. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express Graphics.

Bit	Access	Default Value	Description
7:0	R/W	00h	<b>Secondary Bus Number (BUSDN):</b> This field is programmed by configuration software with the bus number assigned to PCI Express Graphics.

### 21.1.11 SUBUSN1 - Subordinate Bus Number

B/D/F/Type:	0/1/0/PCI
Address Offset:	1Ah
Default Value:	00h
Access:	R/W
Size:	8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express Graphics. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express Graphics.

Bit	Access	Default Value	Description
7:0	R/W	00h	<b>Subordinate Bus Number (BUSDN):</b> This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the Device 1 bridge. When only a single PCI device resides on the PCI Express Graphics segment, this register will contain the same value as the SBUSN1 register.



### 21.1.12 IOBASE1 - I/O Base Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	1Ch
Default Value:	F0h
Access:	RO; R/W
Size:	8 bits

This register controls the CPU to PCI Express Graphics I/O access routing based on the following formula:  $\text{IO\_BASE} = <\text{address} = <\text{IO\_LIMIT}$

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Access	Default Value	Description
7:4	R/W	Fh	<b>I/O Address Base (IOBASE):</b> Corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express Graphics. BIOS must not set this register to 00h otherwise 0CF8h/0CFCh accesses will be forwarded to the PCI Express hierarchy associated with this device.
3:0	RO	0h	<b>Reserved</b>

### 21.1.13 IOLIMIT1 - I/O Limit Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	1Dh
Default Value:	00h
Access:	RO; R/W
Size:	8 bits

This register controls the CPU to PCI Express Graphics I/O access routing based on the following formula:  $\text{IO\_BASE} = <\text{address} = <\text{IO\_LIMIT}$ .

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Access	Default Value	Description
7:4	R/W	0h	<b>I/O Address Limit (IOLIMIT):</b> Corresponds to A[15:12] of the I/O address limit of Device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0	RO	0h	<b>Reserved</b>



### 21.1.14 SSTS1 - Secondary Status

B/D/F/Type: 0/1/0/PCI  
Address Offset: 1E-1Fh  
Default Value: 0000h  
Access: R/WC; RO  
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express Graphics side) of the "virtual" PCI-PCI bridge embedded within (G)MCH.

Bit	Access	Default Value	Description
15	R/WC	0b	<b>Detected Parity Error (DPE):</b> When set indicates that the MCH received across the link (upstream) a Posted Write Data Poisoned TLP (EP=1).
14	R/WC	0b	<b>Received System Error (RSE):</b> This bit is set when the secondary side receives an ERR_FATAL or ERR_NONFATAL message due to an error detected by the secondary side, and the SERR Enable bit in the Bridge Control register is 1.
13	R/WC	0b	<b>Received Master Abort (RMA):</b> This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	R/WC	0b	<b>Received Target Abort (RTA):</b> This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO	0b	<b>Signaled Target Abort (STA):</b> Not Applicable or Implemented. Hardwired to 0. The (G)MCH does not generate Target Aborts (the (G)MCH will never complete a request using the Completer Abort Completion status).
10:9	RO	00b	<b>DEVSELB Timing (DEVT):</b> Not Applicable or Implemented. Hardwired to 0.
8	R/WC	0b	<b>Master Data Parity Error (SMDPE):</b> When set indicates that the MCH received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO	0b	<b>Fast Back-to-Back (FB2B):</b> Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	Reserved
5	RO	0b	<b>66-/60-MHz Capability (CAP66):</b> Not Applicable or Implemented. Hardwired to 0.
4:0	RO	00h	Reserved



### 21.1.15 MBASE1 - Memory Base Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	20-21h
Default Value:	FFF0h
Access:	RO; R/W
Size:	16 bits

This register controls the CPU to PCI Express Graphics non-prefetchable memory access routing based on the following formula:

$$\text{MEMORY\_BASE} = <\text{address} = <\text{MEMORY\_LIMIT}$$

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access	Default Value	Description
15:4	R/W	FFFh	<b>Memory Address Base (MBASE):</b> Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express Graphics.
3:0	RO	0h	<b>Reserved</b>

### 21.1.16 MLIMIT1 - Memory Limit Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	22-23h
Default Value:	0000h
Access:	RO; R/W
Size:	16 bits

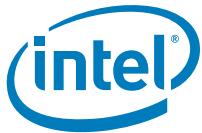
This register controls the CPU to PCI Express Graphics non-prefetchable memory access routing based on the following formula:

$$\text{MEMORY\_BASE} = <\text{address} = <\text{MEMORY\_LIMIT}$$

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

**Note:**

Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express Graphics address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved CPU-PCI Express memory access performance.



**Note:** Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e., prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the (G)MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Access	Default Value	Description
15:4	R/W	000h	<b>Memory Address Limit (MLIMIT):</b> Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express Graphics.
3:0	RO	0h	<b>Reserved</b>

### 21.1.17 PMBASE1 - Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI  
Address Offset: 24-25h  
Default Value: FFF1h  
Access: RO; R/W  
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the CPU to PCI Express Graphics prefetchable memory access routing based on the following formula:

$$\text{PREFETCHABLE\_MEMORY\_BASE} = <\text{address}> - <\text{PREFETCHABLE\_MEMORY\_LIMIT}>$$

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access	Default Value	Description
15:4	R/W	FFFh	<b>Prefetchable Memory Base Address (MBASE):</b> Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express graphics.
3:0	RO	1h	<b>64-Bit Address Support:</b> Indicates that the upper 32 bits of the prefetchable memory region base address are contained in the Prefetchable Memory base Upper Address register at 28h.



## 21.1.18 PMLIMIT1 - Prefetchable Memory Limit Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	26-27h
Default Value:	0001h
Access:	RO; R/W
Size:	16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the CPU to PCI Express Graphics prefetchable memory access routing based on the following formula:

PREFETCHABLE\_MEMORY\_BASE = < address = < PREFETCHABLE\_MEMORY\_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the CPU perspective.

Bit	Access	Default Value	Description
15:4	R/W	000h	<b>Prefetchable Memory Address Limit (PMLIMIT):</b> Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express graphics.
3:0	RO	1h	<b>64-bit Address Support:</b> Indicates that the upper 32 bits of the prefetchable memory region limit address are contained in the Prefetchable Memory Base Limit Address register at 2Ch



### 21.1.19 PMBASEU1 - Prefetchable Memory Base Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	28-2Bh
Default Value:	0000000Fh
Access:	R/W
Size:	32 bits

The functionality associated with this register is present in the PCI Express graphics design implementation.

This register in conjunction with the corresponding Upper Base Address register controls the CPU to PCI Express Graphics prefetchable memory access routing based on the following formula:

PREFETCHABLE\_MEMORY\_BASE =< address =< PREFETCHABLE\_MEMORY\_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access	Default Value	Description
31:4	R/W	0000000h	<b>Reserved (MBASEU1):</b> These registers are R/W for compliance purposes only. They should never be programmed to anything other than zeros.
3:0	R/W	Fh	<b>Prefetchable Memory Base Address (MBASEU):</b> Corresponds to A[35:32] of the lower limit of the prefetchable memory range that will be passed to PCI Express graphics.



## 21.1.20 PMLIMITU1 - Prefetchable Memory Limit Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	2C-2Fh
Default Value:	00000000h
Access:	R/W
Size:	32 bits

The functionality associated with this register is present in the PCI Express graphics design implementation. This register in conjunction with the corresponding Upper Limit Address register controls the CPU to PCI Express Graphics prefetchable memory access routing based on the following formula:

$$\text{PREFETCHABLE\_MEMORY\_BASE} = <\text{address} = <\text{PREFETCHABLE\_MEMORY\_LIMIT}$$

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the CPU perspective.

Bit	Access	Default Value	Description
31:4	R/W	0000000h	<b>Reserved (MLIMITU1):</b> These registers are R/W for compliance purposes only. They should never be programmed to anything other than zeros.
3:0	R/W	0h	<b>Prefetchable Memory Address Limit (MLIMITU):</b> Corresponds to A[35:32] of the upper limit of the prefetchable Memory range that will be passed to PCI Express graphics.



### 21.1.21 CAPPTR1 - Capabilities Pointer

B/D/F/Type:	0/1/0/PCI
Address Offset:	34h
Default Value:	88h
Access:	RO
Size:	8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access	Default Value	Description
7:0	RO	88h	<b>First Capability (CAPPTR1):</b> The first capability in the list is the Subsystem ID and Subsystem Vendor ID capability.

### 21.1.22 INTRLINE1 - Interrupt Line

B/D/F/Type:	0/1/0/PCI
Address Offset:	3Ch
Default Value:	00h
Access:	R/W
Size:	8 bits

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Bit	Access	Default Value	Description
7:0	R/W	00h	<b>Interrupt Connection (INTCON):</b> Used to communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this device's interrupt pin is connected.



### 21.1.23 INTRPIN1 - Interrupt Pin

B/D/F/Type:	0/1/0/PCI
Address Offset:	3Dh
Default Value:	01h
Access:	RO
Size:	8 bits

This register specifies which interrupt pin this device uses.

Bit	Access	Default Value	Description
7:0	RO	01h	<b>Interrupt Pin (INTRPIN1):</b> As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

### 21.1.24 BCTRL1 - Bridge Control

B/D/F/Type:	0/1/0/PCI
Address Offset:	3E-3Fh
Default Value:	0000h
Access:	RO; R/W
Size:	16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express Graphics) as well as some bits that affect the overall behavior of the “virtual” Host-PCI Express bridge embedded within (G)MCH, e.g., VGA-compatible address ranges mapping.

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Bit	Access	Default Value	Description
15:12	RO	0h	<b>Reserved</b>
11	RO	0b	<b>Discard Timer SERR Enable (DTSERRE):</b> Not Applicable or Implemented. Hardwired to 0.
10	RO	0b	<b>Discard Timer Status (DTSTS):</b> Not Applicable or Implemented. Hardwired to 0.
9	RO	0b	<b>Secondary Discard Timer (SDT):</b> Not Applicable or Implemented. Hardwired to 0.
8	RO	0b	<b>Primary Discard Timer (PDT):</b> Not Applicable or Implemented. Hardwired to 0.
7	RO	0b	<b>Fast Back-to-Back Enable (FB2BEN):</b> Not Applicable or Implemented. Hardwired to 0.
6	R/W	0b	<b>Secondary Bus Reset (SRESET):</b> Setting this bit triggers a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0, L0s, or L1 states.



(Sheet 2 of 2)

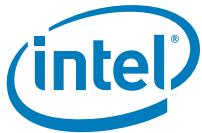
Bit	Access	Default Value	Description
5	RO	0b	<b>Master Abort Mode (MAMODE):</b> When acting as a master, unclaimed reads that experience a master abort returns all 1's and any writes that experience a master abort completes normally and the data is thrown away. Hardwired to 0.
4	R/W	0b	<b>VGA 16-bit Decode (VGA16D):</b> Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if Bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	R/W	0b	<b>VGA Enable (VGAEN):</b> Controls the routing of CPU initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in Device 0, offset 97h[0].
2	R/W	0b	<b>ISA Enable (ISAEN):</b> Needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the (G)MCH to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions will be mapped to PCI Express Graphics. 1 = (G)MCH will not forward to PCI Express Graphics any I/O transactions addressing the last 768 bytes in each 1-KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express Graphics these cycles will be forwarded to DMI where they can be subtractively or positively claimed by the ISA bridge.
1	R/W	0b	<b>SERR Enable (SERREN):</b> 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	R/W	0b	<b>Parity Error Response Enable (PEREN):</b> Controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the MCH receives across the link (upstream) a Read Data Completion Poisoned TLP 0 = Master Data Parity Error bit in Secondary Status register <b>cannot</b> be set. 1 = Master Data Parity Error bit in Secondary Status register <b>can</b> be set.



## 21.1.25 PM\_CAPID1 - Power Management Capabilities

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 80-83h  
 Default Value: C8039001h  
 Access: RO  
 Size: 32 bits

Bit	Access	Default Value	Description
31:27	RO	19h	<b>PME Support (PMES):</b> This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot & D3cold. This device is not required to do anything to support D3hot & D3cold, it simply must report that those states are supported. Refer to the <i>PCI Power Management 1.1 Specification</i> for encoding explanation and other power management details.
26	RO	0b	<b>D2 Power State Support (D2PSS):</b> Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO	0b	<b>D1 Power State Support (D1PSS):</b> Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO	000b	<b>Auxiliary Current (AUXC):</b> Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO	0b	<b>Device Specific Initialization (DSI):</b> Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO	0b	<b>Auxiliary Power Source (APS):</b> Hardwired to 0.
19	RO	0b	<b>PME Clock (PMECLK):</b> Hardwired to 0 to indicate this device does NOT support PMEB generation.
18:16	RO	011b	<b>PCI PM CAP Version (PCIPMCV):</b> Version: - A value of 011b indicates that this function complies with revision 1.2 of the <i>PCI Power Management Interface Specification</i> .
15:8	RO	90h	<b>Pointer to Next Capability (PNC):</b> This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, then the next item in the capabilities list is the PCI Express capability at A0h.
7:0	RO	01h	<b>Capability ID (CID):</b> Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.



### 21.1.26 PM\_CS1 - Power Management Control/Status

B/D/F/Type: 0/1/0/PCI  
Address Offset: 84-87h  
Default Value: 00000000h  
Access: RO; R/W/S; R/W  
Size: 32 bits

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Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b> Not Applicable or Implemented. Hardwired to 0.
15	RO	0b	<b>PME Status (PMESTS):</b> Indicates that this device does not support PMEB generation from D3cold.
14:13	RO	00b	<b>Data Scale (DSCALE):</b> Indicates that this device does not support the power management data register.
12:9	RO	0h	<b>Data Select (DSEL):</b> Indicates that this device does not support the power management data register.
8	R/W/S	0b	<b>PME Enable (PMEE):</b> Indicates that this device does not generate PMEB assertion from any D-state. 0 = PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:4	RO	0000b	<b>Reserved:</b>
3	RO	0b	<b>No Soft Reset (NSR):</b> When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full re-initialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 uninitialized with only PME context preserved if PME is supported and enabled. This bit is hardwired to 0.
2	RO	0b	<b>Reserved</b>



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Bit	Access	Default Value	Description
1:0	R/W	00b	<p><b>Power State (PS):</b> Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs.</p> <p>00 = D0 01 = D1 (Not supported in this device.) 10 = D2 (Not supported in this device.) 11 = D3</p> <p>Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional.</p> <p>When the Power State is other than D0, the bridge will Master Abort (i.e., not claim) any downstream cycles (with exception of Type 0 config cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the MCH logs as Master Aborts in Device 0 PCISTS[13]. There is no additional hardware functionality required to support these power states.</p>

### 21.1.27 SS\_CAPID - Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 88-8Bh  
 Default Value: 0000800Dh  
 Access: RO  
 Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b>
15:8	RO	80h	<b>Pointer to Next Capability (PNC):</b> This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO	0Dh	<b>Capability ID (CID):</b> Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI bridge.



### 21.1.28 SS - Subsystem ID and Subsystem Vendor ID

B/D/F/Type:	0/1/0/PCI
Address Offset:	8C-8Fh
Default Value:	00008086h
Access:	R/WO
Size:	32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and hardware reset.

Bit	Access	Default Value	Description
31:16	R/WO	0000h	<b>Subsystem ID (SSID):</b> Identifies the particular subsystem and is assigned by the vendor.
15:0	R/WO	8086h	<b>Subsystem Vendor ID (SSVID):</b> Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

### 21.1.29 MSI\_CAPID - Message Signaled Interrupts Capability ID

B/D/F/Type:	0/1/0/PCI
Address Offset:	90-91h
Default Value:	A005h
Access:	RO
Size:	16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

The reporting of the existence of this capability can be disabled by setting MSICH (CAPL[0] @ 7Fh). In that case walking this linked list will skip this capability and instead go directly from the PCI PM capability to the PCI Express capability.

Bit	Access	Default Value	Description
15:8	RO	A0h	<b>Pointer to Next Capability (PNC):</b> This contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO	05h	<b>Capability ID (CID):</b> Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

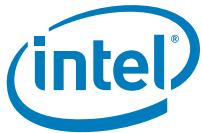


### 21.1.30 MC - Message Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: 92-93h  
 Default Value: 0000h  
 Access: RO; R/W  
 Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Reserved</b>
7	RO	0b	<b>64-bit Address Capable (64AC):</b> Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32 bit-/4-GB limit.
6:4	R/W	000b	<b>Multiple Message Enable (MME):</b> System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO	000b	<b>Multiple Message Capable (MMC):</b> System software reads this field to determine the number of messages being requested by this device. Value: Number of Messages Requested 000 = 1 All of the following are reserved in this implementation: 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110 = Reserved 111 = Reserved
0	R/W	0b	<b>MSI Enable (MSIEN):</b> Controls the ability of this device to generate MSIs. 0 = MSI will not be generated. 1 = MSI will be generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.



### 21.1.31 MA - Message Address

B/D/F/Type: 0/1/0/PCI  
Address Offset: 94-97h  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

Bit	Access	Default Value	Description
31:2	R/W	00000000h	<b>Message Address (MA):</b> Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	<b>Force Dword Align (FDWA):</b> Hardwired to 0 so that addresses assigned by system software are always aligned on a dword address boundary.

### 21.1.32 MD - Message Data

B/D/F/Type: 0/1/0/PCI  
Address Offset: 98-99h  
Default Value: 0000h  
Access: R/W  
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/W	0000h	<b>Message Data (MD):</b> Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.



### 21.1.33 PEG\_CAPL - PCI Express Graphics Capability List

B/D/F/Type:	0/1/0/PCI
Address Offset:	A0-A1h
Default Value:	0010h
Access:	RO
Size:	16 bits

Enumerates the PCI Express capability structure.

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Pointer to Next Capability (PNC):</b> This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express extended configuration space.
7:0	RO	10h	<b>Capability ID (CID):</b> Identifies this linked list item (capability structure) as being for PCI Express registers.

### 21.1.34 PEG\_CAP - PCI Express Graphics Capabilities

B/D/F/Type:	0/1/0/PCI
Address Offset:	A2-A3h
Default Value:	0141h
Access:	RO; R/WO
Size:	16 bits

Indicates PCI Express device capabilities.

Bit	Access	Default Value	Description
15:14	RO	00b	<b>Reserved</b>
13:9	RO	00h	<b>Interrupt Message Number (IMN):</b> Not Applicable or Implemented. Hardwired to 0.
8	R/WO	1b	<b>Slot Implemented (SI):</b> 0 = The PCI Express Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot. BIOS Requirement: This field must be initialized appropriately if a slot connection is not implemented.
7:4	RO	4h	<b>Device/Port Type (DPT):</b> Hardwired to 4h to indicate root port of PCI Express Root Complex.
3:0	RO	1h	<b>PCI Express Capability Version (PCIECV):</b> Hardwired to 1 as it is the first version.



### 21.1.35 DCAP - Device Capabilities

B/D/F/Type: 0/1/0/PCI  
Address Offset: A4-A7h  
Default Value: 00008000h  
Access: RO  
Size: 32 bits

Indicates PCI Express device capabilities

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved:</b> Not Applicable or Implemented. Hardwired to 0.
15	RO	1b	<b>Role-Based Error Reporting (RBER): Role-Based Error Reporting-</b> This bit, when set, indicates that the device implements the functionality originally defined in the Error Reporting ECN for <i>PCI Express Base Specification, Revision 1.0a</i> , and later incorporated into <i>PCI Express Base Specification, Revision 1.1</i> . This bit must be set by all devices conforming to the ECN, <i>PCI Express Base Specification, Revision 1.1</i> , or subsequent <i>PCI Express Base Specification</i> revisions.
14:6	RO	00000000b	<b>Reserved</b>
5	RO	0b	<b>Extended Tag Field Supported (ETFS):</b> Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO	00b	<b>Phantom Functions Supported (PFS):</b> Not Applicable or Implemented. Hardwired to 0.
2:0	RO	000b	<b>Max Payload Size (MPS):</b> Hardwired to indicate 128 B max supported payload for Transaction Layer Packets (TLP).



### 21.1.36 DCTL - Device Control

B/D/F/Type:	0/1/0/PCI
Address Offset:	A8-A9h
Default Value:	0000h
Access:	RO; R/W
Size:	16 bits

Provides control for PCI Express device specific capabilities. The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR\_CORR, ERR\_NONFATAL, ERR\_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access	Default Value	Description
15:12	RO	0h	<b>Reserved</b>
11	RO	0b	<b>Reserved for Enable No Snoop</b>
10:8	RO	000b	<b>Reserved</b>
7:5	R/W	000b	<b>Max Payload Size (MPS):</b> 000 = 128 B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. All other encodings are reserved. Hardware will actually ignore this field. It is writeable only to support compliance testing.
4	RO	0b	<b>Reserved</b>
3	R/W	0b	<b>Unsupported Request Reporting Enable (URRE):</b> When set, Unsupported Requests will be reported. <b>NOTE:</b> Reporting of error messages received by Root Port is controlled exclusively by Root Control register.
2	R/W	0b	<b>Fatal Error Reporting Enable (FERE):</b> When set fatal errors will be reported. For a Root Port, the reporting of fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	R/W	0b	<b>Non-Fatal Error Reporting Enable (NFERE):</b> When set non-fatal errors will be reported. For a Root Port, the reporting of non-fatal errors is internal to the root. No external ERR_NONFATAL message is generated. Uncorrectable errors can result in degraded performance.
0	R/W	0b	<b>Correctable Error Reporting Enable (CERE):</b> When set correctable errors will be reported. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_CORR message is generated.



### 21.1.37 DSTS - Device Status

B/D/F/Type: 0/1/0/PCI  
Address Offset: AA-ABh  
Default Value: 0000h  
Access: RO; R/WC  
Size: 16 bits

Reflects status corresponding to controls in the Device Control register. The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access	Default Value	Description
15:6	RO	000h	<b>Reserved and Zero:</b> For future R/WC/S implementations; software must use 0 for writes to bits.
5	RO	0b	<b>Transactions Pending (TP):</b> 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Indicates that the device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4	RO	0b	<b>Reserved</b>
3	R/WC	0b	<b>Unsupported Request Detected (URD):</b> When set this bit indicates that the Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported.
2	R/WC	0b	<b>Fatal Error Detected (FED):</b> When set this bit indicates that fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
1	R/WC	0b	<b>Non-Fatal Error Detected (NFED):</b> When set this bit indicates that non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
0	R/WC	0b	<b>Correctable Error Detected (CED):</b> When set this bit indicates that correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.



### 21.1.38 LCAP - Link Capabilities

B/D/F/Type: 0/1/0/PCI  
 Address Offset: AC-AFh  
 Default Value: 02012D01h  
 Access: RO; R/WO  
 Size: 32 bits

Indicates PCI Express device specific capabilities.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31:24	RO	02h	<b>Port Number (PN):</b> Indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description[31:24].
23:21	RO	000b	<b>Reserved</b>
20	RO	0b	<b>Data Link Layer Link Active Reporting Capable (DLLLARC):</b> For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable field of the Slot Capabilities register), this bit must be set to 1b. For upstream ports and components that do not support this optional capability, this bit must be hardwired to 0b.
19	RO	0b	<b>Surprise Down Error Reporting Capable (SDERC):</b> For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
18	RO	0b	<b>Clock Power Management (CPM):</b> A value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) when the link is in the L1 and L2/3 Ready link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these link states. This capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multifunction device indicate a 1b in this bit.
17:15	R/WO	010b	<b>L1 Exit Latency (L1ELAT):</b> Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 $\mu$ s to less than 4 $\mu$ s. <b>BIOS Requirement:</b> If this field is required to be any value other than the default, BIOS must initialize it accordingly. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.



## (Sheet 2 of 2)

Bit	Access	Default Value	Description																
14:12	RO	010b	<b>L0s Exit Latency (LOSELAT):</b> Indicates the length of time this Port requires to complete the transition from L0s to L0.  <table border="1"><tr><td>000:</td><td>Less than 64 ns</td></tr><tr><td>001:</td><td>64 ns to less than 128 ns</td></tr><tr><td>010:</td><td>128 ns to less than 256 ns</td></tr><tr><td>011:</td><td>256 ns to less than 512 ns</td></tr><tr><td>100:</td><td>512 ns to less than 1 µs</td></tr><tr><td>101:</td><td>1 µs to less than 2 µs</td></tr><tr><td>110:</td><td>2 µs - 4 µs</td></tr><tr><td>111:</td><td>More than 4 µs</td></tr></table> The actual value of this field depends on the common Clock Configuration bit (LCTL[6]) and the Common and Non-Common clock L0s Exit Latency values in PEGLOSLAT (Offset 22Ch).	000:	Less than 64 ns	001:	64 ns to less than 128 ns	010:	128 ns to less than 256 ns	011:	256 ns to less than 512 ns	100:	512 ns to less than 1 µs	101:	1 µs to less than 2 µs	110:	2 µs - 4 µs	111:	More than 4 µs
000:	Less than 64 ns																		
001:	64 ns to less than 128 ns																		
010:	128 ns to less than 256 ns																		
011:	256 ns to less than 512 ns																		
100:	512 ns to less than 1 µs																		
101:	1 µs to less than 2 µs																		
110:	2 µs - 4 µs																		
111:	More than 4 µs																		
11:10	R/WO	11b	<b>Active State Link PM Support (ASLPMS)</b>																
9:4	RO	10h	<b>Max Link Width (MLW):</b> Indicates the maximum number of lanes supported for this link.																
3:0	RO	1h	<b>Max Link Speed (MLS):</b> Hardwired to indicate 2.5 Gb/s.																



### 21.1.39 LCTL - Link Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: B0-B1h  
 Default Value: 0040h  
 Access: RO; R/W  
 Size: 16 bits

Allows control of PCI Express link.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:9	RO	0000000b	<b>Reserved</b>
8	RO	0b	<p><b>Enable Clock Power Management (ECPM):</b> Applicable only for form factors that support a "Clock Request" (CLKREQ#) mechanism, this enable functions as follows</p> <p>0b – Clock power management is disabled and device must hold CLKREQ# signal low</p> <p>1b – When this bit is set to 1 the device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification.</p> <p>Default value of this field is 0b.</p> <p>Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.</p>
7	R/W	0b	<p><b>Extended Synch (ES):</b></p> <p>0 = Standard Fast Training Sequence (FTS).</p> <p>1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state.</p> <p>This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.</p>
6	R/W	1b	<p><b>Common Clock Configuration (CCC):</b></p> <p>0 = Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock.</p> <p>1 = Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock.</p> <p>The state of this bit affects the L0s Exit Latency reported in LCAP[14:12] and the N_FTS value advertised during link training.</p> <p>See PEGL0SLAT at offset 22Ch.</p>



## (Sheet 2 of 2)

Bit	Access	Default Value	Description								
5	R/W	0b	<b>Retrain Link (RL):</b> 0 = Normal operation. 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).								
4	R/W	0b	<b>Link Disable (LD):</b> 0 = Normal operation 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 1 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.								
3	RO	0b	<b>Read Completion Boundary (RCB):</b> Hardwired to 0 to indicate 64 byte.								
2	R/W	0b	<b>Far-End Digital Loopback (FEDLB):</b>								
1:0	R/W	00b	<b>Active State PM (ASPM):</b> Controls the level of active state power management supported on the given link.  <table border="1"><tr><td>00</td><td>Disabled</td></tr><tr><td>01</td><td>L0s Entry Supported</td></tr><tr><td>10</td><td>Reserved</td></tr><tr><td>11</td><td>L0s and L1 Entry Supported</td></tr></table>	00	Disabled	01	L0s Entry Supported	10	Reserved	11	L0s and L1 Entry Supported
00	Disabled										
01	L0s Entry Supported										
10	Reserved										
11	L0s and L1 Entry Supported										



## 21.1.40 LSTS - Link Status

B/D/F/Type: 0/1/0/PCI  
 Address Offset: B2-B3h  
 Default Value: 1001h  
 Access: RO  
 Size: 16 bits

Indicates PCI Express link status.

Bit	Access	Default Value	Description
15:14	RO	00b	<b>Reserved</b>
13	RO	0b	<b>Data Link Layer Link Active (Optional) (DLLA):</b> This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the corresponding Data Link Layer Active capability bit is implemented. Otherwise, this bit must be hardwired to 0b.
12	RO	1b	<b>Slot Clock Configuration (SCC):</b> 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO	0b	<b>Link Training (LTRN):</b> Indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO	0b	<b>Undefined:</b> The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.
9:4	RO	00h	<b>Negotiated Width (NW):</b> Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). <ul style="list-style-type: none"> <li>• 01h:X1</li> <li>• 10h:X16</li> </ul> All other encodings are reserved.
3:0	RO	1h	<b>Negotiated Speed (NS):</b> Indicates negotiated link speed. <ul style="list-style-type: none"> <li>• 1h:2.5 Gb/s All other encodings are reserved.</li> </ul>



### 21.1.41 SLOTCAP - Slot Capabilities

B/D/F/Type: 0/1/0/PCI  
Address Offset: B4-B7h  
Default Value: 00040040h  
Access: R/WO; RO  
Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access	Default Value	Description								
31:19	R/WO	0000h	<b>Physical Slot Number (PSN):</b> Indicates the physical slot number attached to this Port. BIOS Requirement: This field must be initialized by BIOS to a value that assigns a slot number that is globally unique within the chassis.								
18	R/WO	1b	<b>No Command Completed Support (NCCS):</b> When set to 1b, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set to 1b if the hot-plug capable port is able to accept writes to all fields of the Slot Control register without delay between successive writes.								
17	RO	0b	<b>Reserved</b>								
16:15	R/WO	00b	<b>Slot Power Limit Scale (SPLS):</b> Specifies the scale used for the Slot Power Limit Value. <table border="1"><tr><td>00</td><td>1.0x</td></tr><tr><td>01</td><td>0.1x</td></tr><tr><td>10</td><td>0.01x</td></tr><tr><td>11</td><td>0.001xIf this field is written, the link sends a Set_Slot_Power_Limit message.</td></tr></table>	00	1.0x	01	0.1x	10	0.01x	11	0.001xIf this field is written, the link sends a Set_Slot_Power_Limit message.
00	1.0x										
01	0.1x										
10	0.01x										
11	0.001xIf this field is written, the link sends a Set_Slot_Power_Limit message.										
14:7	R/WO	00h	<b>Slot Power Limit Value (SPLV):</b> In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.								
6	RO	1b	<b>Hot-plug Capable (HPC):</b> When set to 1b, this bit indicates that this slot is capable of supporting hot-plug operations.								
5	RO	0b	<b>Reserved</b>								
4	RO	0b	<b>Reserved</b>								
3	RO	0b	<b>Reserved</b>								
2	RO	0b	<b>Reserved</b>								
1	RO	0b	<b>Reserved</b>								
0	RO	0b	<b>Reserved</b>								



## 21.1.42 SLOTCTL - Slot Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: B8-B9h  
 Default Value: 01C0h  
 Access: RO; R/W  
 Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access	Default Value	Description
15:13	RO	000b	<b>Reserved</b>
12	RO	0b	<b>Reserved</b>
11	RO	0b	<b>Reserved</b>
10	RO	0b	<b>Reserved</b>
9:8	RO	01b	<b>Reserved</b>
7:6	RO	11b	<b>Reserved</b>
5	R/W	0b	<b>Hot-plug Interrupt Enable (HPIE):</b> When set to 1b, this bit enables generation of an interrupt on enabled hot-plug events. Default value of this field is 0b. If the Hot Plug Capable field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.
4	RO	0b	<b>Reserved</b>
3	R/W	0b	<b>Presence Detect Changed Enable (PDCE):</b> When set to 1b, this bit enables software notification on a presence detect changed event.
2	RO	0b	<b>Reserved</b>
1	RO	0b	<b>Reserved</b>
0	RO	0b	<b>Reserved</b>



### 21.1.43 SLOTSTS - Slot Status

B/D/F/Type: 0/1/0/PCI  
Address Offset: BA-BBh  
Default Value: 0000h  
Access: RO; R/WC  
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access	Default Value	Description
15:9	RO	0000000b	<b>Reserved</b>
8	RO	0b	<b>Reserved</b>
7	RO	0b	<b>Reserved</b>
6	RO	0b	<b>Presence Detect State (PDS):</b> This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. Defined encodings are: 0b Slot Empty 1b Card Present in slot  This register must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities Register is 0b), this bit must return 1b.
5	RO	0b	<b>Reserved</b>
4	RO	0b	<b>Reserved</b>
3	R/WC	0b	<b>Presence Detect Changed (PDC):</b> This bit is set when the value reported in Presence Detect State is changed.
2	RO	0b	<b>Reserved</b>
1	RO	0b	<b>Reserved</b>
0	RO	0b	<b>Reserved</b>



## 21.1.44 RCTL - Root Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: BC-BDh  
 Default Value: 0000h  
 Access: RO; R/W  
 Size: 16 bits

Allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access	Default Value	Description
15:4	RO	000h	<b>Reserved</b>
3	R/W	0b	<b>PME Interrupt Enable (PMEIE):</b> 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	R/W	0b	<b>System Error on Fatal Error Enable (SEFEE):</b> Controls the Root Complex's response to fatal errors. 0 = No SERR generated on receipt of fatal error. 1 = Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	R/W	0b	<b>System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE):</b> Controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W	0b	<b>System Error on Correctable Error Enable (SECEE):</b> Controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.



### 21.1.45 RSTS - Root Status

B/D/F/Type: 0/1/0/PCI  
Address Offset: C0-C3h  
Default Value: 00000000h  
Access: RO; R/WC  
Size: 32 bits

Provides information about PCI Express Root Complex specific parameters.

Bit	Access	Default Value	Description
31:18	RO	0000h	<b>Reserved</b>
17	RO	0b	<b>PME Pending (PMEP):</b> Indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	R/WC	0b	<b>PME Status (PMES):</b> Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO	0000h	<b>PME Requestor ID (PMERID):</b> Indicates the PCI requestor ID of the last PME requestor.



## 21.1.46 PEGLC - PCI Express Graphics Legacy Control

B/D/F/Type: 0/1/0/PCI  
 Address Offset: EC-EFh  
 Default Value: 00000000h  
 Access: RO; R/W  
 Size: 32 bits

Controls functionality that is needed by Legacy (non-PCI Express aware) OS's during run time.

Bit	Access	Default Value	Description
31:3	RO	00000000h	<b>Reserved</b>
2	R/W	0b	<b>PME GPE Enable (PMEGPE):</b> 0 = Do not generate GPE PME message when PME is received. 1 = Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the MCH to support PMEs on the PCI Express graphics port under legacy OSs.
1	R/W	0b	<b>Hot-Plug GPE Enable (HPGPE):</b> 0 = Do not generate GPE Hot-Plug message when Hot-Plug event is received. 1 = Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the MCH to support Hot-Plug on the PCI Express graphics port under legacy OSs.
0	R/W	0b	<b>General Message GPE Enable (GENGPE):</b> 0 = Do not forward received GPE assert/deassert messages. 1 = Forward received GPE assert/deassert messages. These general GPE message can be received via the PCI Express graphics port from an external Intel device (i.e., PxH) and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI). For example, PxH might send this message if a PCI Express device is hot plugged into a PxH downstream port.

## 21.1.47 PEGCFG1 - PCI Express Graphics Config 1

B/D/F/Type: 0/1/0/PCI  
 Address Offset: F0-F3h  
 Default Value: 00010000h  
 Access: RO; R/W  
 Size: 32 bits

This register must be left at its default value or programmed as defined by the (G)MCH BIOS Specification.



### 21.1.48 PEGCFG2 - PCI Express Graphics Config 2

B/D/F/Type:	0/1/0/PCI
Address Offset:	FC-FFh
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

This register must be left at its default value or programmed as defined by the (G)MCH BIOS Specification.

## 21.2 PCI Express Graphics Device 1 Function 0 Extended Configuration Registers

Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definition than standard PCI capability structures.

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Virtual Channel Enhanced Capability Header	VCECH	100	103	14010002h	RO
Port VC Capability Register 1	PVCCAP1	104	107	00000000h	RO
Port VC Capability Register 2	PVCCAP2	108	10B	00000001h	RO
Port VC Control	PVCCTL	10C	10D	0000h	RO; R/W
VC0 Resource Capability	VC0RCAP	110	113	00000000h	RO
VC0 Resource Control	VC0RCTL	114	117	800000FFh	RO; R/W
VC0 Resource Status	VC0RSTS	11A	11B	0002h	RO
VC1 Resource Capability	VC1RCAP	11C	11F	00000000h	RO
VC1 Resource Control	VC1RCTL	120	123	00000000h	RO
VC1 Resource Status	VC1RSTS	126	127	0000h	RO
Root Complex Link Declaration Enhanced	RCLDECH	140	143	00010005h	RO
Element Self Description	ESD	144	147	02000100h	RO; R/WO
Link Entry 1 Description	LE1D	150	153	00000000h	RO; R/WO
Link Entry 1 Address	LE1A	158	15F	000000000000000000h	RO; R/WO
PCI Express Graphics Sequence Status	PEGSSTS	218	21F	0000000000000FFh	RO
PCI Express Graphics Error Status	PEGERRSTS	228	22B	00000000h	RO



### 21.2.1 VCECH - Virtual Channel Enhanced Capability Header

B/D/F/Type:	0/1/0/MM
Address Offset:	100-103h
Default Value:	14010002h
Access:	RO
Size:	32 bits

Indicates PCI Express device Virtual Channel capabilities. Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

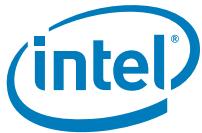
Bit	Access	Default Value	Description
31:20	RO	140h	<b>Pointer to Next Capability (PNC):</b> The Link Declaration capability is the next in the PCI Express extended capabilities list.
19:16	RO	1h	<b>PCI Express Virtual Channel Capability Version (PCIEVCCV):</b> Hardwired to 1 to indicate compliances with the 1.0 version of the <i>PCI Express Specification</i> .
15:0	RO	0002h	<b>Extended Capability ID (ECID):</b> Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

### 21.2.2 PVCCAP1 - Port VC Capability Register 1

B/D/F/Type:	0/1/0/MM
Address Offset:	104-107h
Default Value:	00000000h
Access:	RO
Size:	32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	0000000h	<b>Reserved</b>
6:4	RO	000b	<b>Low Priority Extended VC Count (LPEVCC):</b> Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	<b>Reserved</b>
2:0	RO	000b	<b>Extended VC Count (EVCC):</b> Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. BIOS Requirement: Set this field to 000b for all configurations. VC1 is not a POR feature.



### 21.2.3 PVCCAP2 - Port VC Capability Register 2

B/D/F/Type: 0/1/0/MM  
Address Offset: 108-10Bh  
Default Value: 00000001h  
Access: RO  
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	<b>VC Arbitration Table Offset (VCATO):</b> Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8	RO	0000h	<b>Reserved</b>
7:0	RO	01h	<b>VC Arbitration Capability (VCAC):</b> Indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority. VC0 is the lowest priority.

### 21.2.4 PVCCTL - Port VC Control

B/D/F/Type: 0/1/0/MM  
Address Offset: 10C-10Dh  
Default Value: 0000h  
Access: RO; R/W  
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	<b>Reserved</b>
3:1	R/W	000b	<b>VC Arbitration Select (VCAS):</b> This field will be programmed by software to the only possible value as indicated in the VC Arbitration capability field. The value 001b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field can not be modified when more than one VC in the LPVC group is enabled.
0	RO	0b	<b>Reserved</b>



## 21.2.5 VC0RCAP - VC0 Resource Capability

B/D/F/Type: 0/1/0/MM  
 Address Offset: 110-113h  
 Default Value: 00000000h  
 Access: RO  
 Size: 32 bits

Bit	Access	Default Value	Description
31:24	RO	00h	<b>Reserved</b>
23	RO	0b	<b>Reserved</b>
22:16	RO	00h	<b>Reserved</b>
15	RO	0b	<b>Reject Snoop Transactions (RSNPT):</b> 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0	RO	0000h	<b>Reserved:</b> The Port Arbitration capability is not valid for root ports.

## 21.2.6 VC0RCTL - VC0 Resource Control

B/D/F/Type: 0/1/0/MM  
 Address Offset: 114-117h  
 Default Value: 800000FFh  
 Access: RO; R/W  
 Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	<b>VC0 Enable (VC0E):</b> For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	<b>Reserved</b>
26:24	RO	000b	<b>VC0 ID (VC0ID):</b> Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:8	RO	0000h	<b>Reserved</b>
7:1	R/W	7Fh	<b>TC/VC0 Map (TCVCOM):</b> Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when Bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	<b>TC0/VC0 Map (TC0VC0M):</b> Traffic Class 0 is always routed to VC0.



### 21.2.7 VC0RSTS - VC0 Resource Status

B/D/F/Type: 0/1/0/MM  
Address Offset: 11A-11Bh  
Default Value: 0002h  
Access: RO  
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	<b>Reserved</b>
1	RO	1b	<b>VC0 Negotiation Pending (VC0NP):</b> 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	<b>Reserved</b>

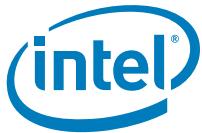


## 21.2.8 RCLDECH - Root Complex Link Declaration Enhanced

B/D/F/Type: 0/1/0/MM  
 Address Offset: 140-143h  
 Default Value: 00010005h  
 Access: RO  
 Size: 32 bits

This capability declares links from this element (PCI Express graphics) to other elements of the root complex component to which it belongs. See the *PCI Express Specification* for link/topology declaration requirements.

Bit	Access	Default Value	Description
31:20	RO	000h	<b>Pointer to Next Capability (PNC):</b> This is the last capability in the PCI Express extended capabilities list unless the partially implemented Advanced Error Reporting capability is exposed. When the AER capability is exposed by clearing the CAPL[1] bit then this field will point to the AER capability at 1CO h which will be the last item in the list.
19:16	RO	1h	<b>Link Declaration Capability Version (LDCV):</b> Hardwired to 1 to indicate compliances with the 1.0 version of the <i>PCI Express Specification</i> .
15:0	RO	0005h	<b>Extended Capability ID (ECID):</b> Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration capability. See corresponding Egress Port Link Declaration capability registers for diagram of Link Declaration Topology.



### 21.2.9 ESD - Element Self Description

B/D/F/Type: 0/1/0/MM  
Address Offset: 144-147h  
Default Value: 02000100h  
Access: RO; R/WO  
Size: 32 bits

Provides information about the root complex element containing this Link Declaration capability.

Bit	Access	Default Value	Description
31:24	RO	02h	<b>Port Number (PN):</b> Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	R/WO	00h	<b>Component ID (CID):</b> Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the <i>PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> .
15:8	RO	01h	<b>Number of Link Entries (NLE):</b> Indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as we don't report any peer-to-peer capabilities in our topology).
7:4	RO	0h	<b>Reserved</b>
3:0	RO	0h	<b>Element Type (ET):</b> Indicates the type of the Root Complex Element. Value of 0 h represents a root port.



## 21.2.10 LE1D - Link Entry 1 Description

B/D/F/Type:	0/1/0/MM
Address Offset:	150-153h
Default Value:	00000000h
Access:	RO; R/WO
Size:	32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	00h	<b>Target Port Number (TPN):</b> Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO	00h	<b>Target Component ID (TCID):</b> Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the <i>PCI Express Isochronous/Virtual Channel Support Hardware Programming Specification (HPS)</i> .
15:2	RO	0000h	<b>Reserved</b>
1	RO	0b	<b>Link Type (LTYP):</b> Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO	0b	<b>Link Valid (LV):</b> 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

## 21.2.11 LE1A - Link Entry 1 Address

B/D/F/Type:	0/1/0/MM
Address Offset:	158-15Fh
Default Value:	0000000000000000h
Access:	RO; R/WO
Size:	64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	<b>Reserved</b>
31:12	R/WO	00000h	<b>Link Address (LA):</b> Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	000h	<b>Reserved</b>



### 21.2.12 PEGSSTS - PCI Express Graphics Sequence Status

B/D/F/Type:	0/1/0/MM
Address Offset:	218-21Fh
Default Value:	0000000000000FFFh
Access:	RO
Size:	64 bits

PCI Express status reporting that is required by the PCI Express specification.

Bit	Access	Default Value	Description
63:60	RO	0h	<b>Reserved</b>
59:48	RO	000h	<b>Next Transmit Sequence Number (NTSN):</b> Value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time.
47:44	RO	0h	<b>Reserved</b>
43:32	RO	000h	<b>Next Packet Sequence Number (NPSN):</b> Packet sequence number to be applied to the next TLP to be transmitted or re-transmitted onto the Link.
31:28	RO	0h	<b>Reserved</b>
27:16	RO	000h	<b>Next Receive Sequence Number (NRSN):</b> This is the sequence number associated with the TLP that is expected to be received next.
15:12	RO	0h	<b>Reserved</b>
11:0	RO	FFFh	<b>Last Acknowledged Sequence Number (LASN):</b> This is the sequence number associated with the last acknowledged TLP.



### 21.2.13 PEGERRSTS - PCI Express Graphics Error Status

B/D/F/Type:	0/1/0/MM
Address Offset:	228-22Bh
Default Value:	00000000h
Access:	RO
Size:	32 bits

This register is used to report various error conditions. A message can be generated on a zero-to-one transition of any of these flags (if enabled by the mask registers). These bits are set regardless of whether or not the message is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Bit	Access	Default Value	Description
31:1	RO	00000000h	<b>Reserved</b>
0	RO	0b	<b>Illegal Isochronous Request Received (IIRR):</b> If set, indicates an illegal TBWRR VC1 Isochronous request was received. This bit is set when a TBWRR VC1 request takes more than 1 time slot to process. This is determined from the address and length information. If this bit is already set, than an interrupt message will not be sent on a new error event.

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## 22 Internal Graphics Device 2 Configuration Register (D2:F0-F1)

Device 2 contains registers for the internal graphics functions. The table below lists the PCI configuration registers in order of ascending offset address.

Function 0 can be VGA compatible or not, this selected through Bit 1 of GGC register (Device 0, offset 52h).

The following sections describe Device 2 PCI configuration registers and are applicable only to (G)MCH variants supporting Integrated Graphics.

### 22.1 Internal Graphics Device 2 Configuration Register Details (D2:F0)

(Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	0	1	8086h	RO
Device Identification	DID2	2	3	2A42h	RO
PCI Command	PCICMD2	4	5	0000h	RO; R/W
PCI Status	PCISTS2	6	7	0090h	RO
Revision Identification	RID2	8	8	00h	RO
Class Code	CC	9	B	030000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT2	D	D	00h	RO
Header Type	HDR2	E	E	80h	RO
Reserved		F	F		
Graphics Translation Table Range Address	GTTMMADR	10	17	0000000000 000004h	RO; R/W
Graphics Memory Range Address	GMADR	18	1F	0000000000 00000Ch	R/W; R/W/L RO
I/O Base Address	IOBAR	20	23	00000001h	RO; R/W
Subsystem Vendor Identification	SVID2	2C	2D	0000h	R/WO
Subsystem Identification	SID2	2E	2F	0000h	R/WO
Video BIOS ROM Base Address	ROMADR	30	33	00000000h	RO
Capabilities Pointer	CAPPOINT	34	34	90h	RO
Interrupt Line	INTRLINE	3C	3C	00h	R/W
Interrupt Pin	INTRPIN	3D	3D	01h	RO
Minimum Grant	MINGNT	3E	3E	00h	RO



## (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Maximum Latency	MAXLAT	3F	3F	00h	RO
Capabilities Pointer (to Mirror of Dev0 CAPID)	MCAPPTR	44	44	48h	RO
Mirror of Dev0 (G)MCH Graphics Control	MGGC	52	53	0030h	RO
Mirror of Dev0 DEVEN	MDEVENdev0F0	54	57	0000001Bh	RO
Software Scratch Read Write	SSRW	58	5B	00000000h	R/W
Base of Stolen Memory	BSM	5C	63	0000000000 000000h	RO
Hardware Scratch Read Write	HSRW	64	65	0000h	R/W
Multi Size Aperture Control	MSAC	66	66	02h	RO; R/W
Message Signaled Interrupts Capability ID	MSI_CAPID	90	91	D005h	RO
Message Control	MC	92	93	0000h	RO; R/W
Message Address	MA	94	97	00000000h	RO; R/W
Message Data	MD	98	99	0000h	R/W
Reserved		9A	CF		
Power Management Capabilities ID	PMCAPID	D0	D1	0001h	RO
Power Management Capabilities	PMCAP	D2	D3	0023h	RO
Power Management Control/ Status	PMCS	D4	D5	0000h	RO; R/W
Reserved		DA	DC		
Software SMI	SWSMI	E0	E1	0000h	R/W
System Display Event Register	ASLE	E4	E7	00000000h	R/W
Software SCI	SWSCI	E8	E9	0000h	R/WO; R/W
Graphics Clock Frequency Control	GCFC	F0	F1	1606h	RO; R/W
Reserved		F2	F3		
Legacy Backlight Brightness	LBB	F4	F7	00000000h	R/W
Reserved		F8	FB		
ASL Storage	ASLS	FC	FF	00000000h	R/W



## 22.1.1 VID2 - Vendor Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	0-1h
Default Value:	8086h
Access:	RO;
Size:	16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

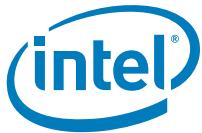
Bit	Access	Default Value	Description
15:0	RO	8086h	<b>Vendor Identification Number (VID):</b> PCI standard identification for Intel.

## 22.1.2 DID2 - Device Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	2-3h
Default Value:	2A42h
Access:	RO;
Size:	16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	2A42h	<b>Device Identification Number (DID2):</b> Identifier assigned to the (G)MCH Device 2 Function 0.



### 22.1.3 PCICMD2 - PCI Command

B/D/F/Type: 0/2/0/PCI  
Address Offset: 4-5h  
Default Value: 0000h  
Access: RO; R/W  
Size: 16 bits

This 16-bit register provides basic control over the IGD ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access	Default Value	Description
15:11	RO	00h	<b>Reserved</b>
10	R/W	0b	<b>Interrupt Disable:</b> This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	RO	0b	<b>Fast Back-to-Back (FB2B):</b> Not Implemented. Hardwired to 0.
8	RO	0b	<b>SERR Enable (SERRE):</b> Not Implemented. Hardwired to 0.
7	RO	0b	<b>Address/Data Stepping Enable (ADSTEP):</b> Not Implemented. Hardwired to 0.
6	RO	0b	<b>Parity Error Enable (PERRE):</b> Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	<b>Video Palette Snooping (VPS):</b> This bit is hardwired to 0 to disable snooping.
4	RO	0b	<b>Memory Write and Invalidate Enable (MWIE):</b> Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	<b>Special Cycle Enable (SCE):</b> This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W	0b	<b>Bus Master Enable (BME):</b> 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	R/W	0b	<b>Memory Access Enable (MAE):</b> This bit controls the IGD response to memory space accesses. 0 = Disable 1 = Enable
0	R/W	0b	<b>I/O Access Enable (IOAE):</b> This bit controls the IGD response to I/O space accesses. 0 = Disable 1 = Enable



## 22.1.4 PCISTS2 - PCI Status

B/D/F/Type:	0/2/0/PCI
Address Offset:	6-7h
Default Value:	0090h
Access:	RO;
Size:	16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	Description
15	RO	0b	<b>Detected Parity Error (DPE):</b> Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO	0b	<b>Signaled System Error (SSE):</b> The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO	0b	<b>Received Master Abort Status (RMAS):</b> The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO	0b	<b>Received Target Abort Status (RTAS):</b> The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO	0b	<b>Signaled Target Abort Status (STAS):</b> Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	<b>DEVSEL Timing (DEVT):</b> N/A. These bits are hardwired to "00".
8	RO	0b	<b>Master Data Parity Error Detected (DPD):</b> Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO	1b	<b>Fast Back-to-Back (FB2B):</b> Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO	0b	<b>User Defined Format (UDF):</b> Hardwired to 0.
5	RO	0b	<b>66-MHz PCI Capable (66C):</b> N/A - Hardwired to 0.
4	RO	1b	<b>Capability List (CLIST):</b> This bit is set to 1 to indicate that the register at 34h provides an offset into the function PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO	0b	<b>Interrupt Status:</b> This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2:0	RO	000b	<b>Reserved</b>



## 22.1.5 RID2 - Revision Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	8h
Default Value:	00h
Access:	RO
Size:	8 bits

RID Definition: This register contains the revision number of the (G)MCH Device 0. Following PCI Reset the SRID value is selected to be read. When a write occurs to this register the write data is compared to the hardwired RID Select Key Value which is 69h. If the data matches this key a flag is set that enables the CRID value to be read through this register.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the (G)MCH. 07h: B-3 stepping

## 22.1.6 CC - Class Code

B/D/F/Type:	0/2/0/PCI
Address Offset:	9-Bh
Default Value:	030000h
Access:	RO;
Size:	24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	Description
23:16	RO	03h	<b>Base Class Code (BCC):</b> This is an 8-bit value that indicates the base class code for the (G)MCH. This code has the value 03h, indicating a Display Controller.
15:8	RO	00h	<b>Sub-Class Code (SUBCC):</b> Based on Device 0 GGC-GMS bits and GGC-IVD bits. 00h = VGA compatible 80h = Non VGA (GMS = "000" or IVD = 1)
7:0	RO	00h	<b>Programming Interface (PI):</b> 00h = Hardwired as a Display controller.



## 22.1.7 CLS - Cache Line Size

B/D/F/Type:	0/2/0/PCI
Address Offset:	Ch
Default Value:	00h
Access:	RO;
Size:	8 bits

The IGD does not support this register as a PCI slave.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Cache Line Size (CLS):</b> This field is hardwired to 0's. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

## 22.1.8 MLT2 - Master Latency Timer

B/D/F/Type:	0/2/0/PCI
Address Offset:	Dh
Default Value:	00h
Access:	RO;
Size:	8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Master Latency Timer Count Value:</b> Hardwired to 0's.

## 22.1.9 HDR2 - Header Type

B/D/F/Type:	0/2/0/PCI
Address Offset:	Eh
Default Value:	80h
Access:	RO;
Size:	8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	Description
7	RO	1b	<b>Multi Function Status (MFunc):</b> Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the Mfunc bit is also set.
6:0	RO	00h	<b>Header Code (H):</b> This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a Type 0 configuration space format.



## 22.1.10 GTTMMADR - Graphics Translation Table Range Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	10-17h
Default Value:	0000000000000004h
Access:	RO; R/W;
Size:	64 bits

This register requests allocation for combined Graphics Translation table and Memory Mapped Range. 4 MB combined for MMIO and Global GTT table aperture (512 KB for MMIO and 2 MB for GTT). GTT base address will be: base address from GTTMMADR + 2 MB, and the MMIO base address will be the same as base address from GTTMMADR.

Bit	Access	Default Value	Description
63:36	R/W	0000000h	<b>Reserved</b>
35:22	R/W	0000h	<b>Memory Base Address:</b> Set by the BIOS, these bits correspond to address signals [35:22]. 4 MB combined for MMIO and Global GTT table aperture (512 KB for MMIO and 2 MB for GTT).
21:4	RO	00000h	<b>Reserved</b>
3	RO	0b	<b>Prefetchable Memory:</b> Hardwired to 0 to prevent prefetching.
2	RO	1b	<b>Memory Type:</b> 0 = To indicate 32-bit base address 1 = To indicate 64-bit base address
1	RO	0b	<b>Reserved</b>
0	RO	0b	<b>Memory/IO Space:</b> Hardwired to 0 to indicate memory space.



## 22.1.11 GMADR - Graphics Memory Range Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	18-1Fh
Default Value:	000000000000000Ch
Access:	R/W; R/W/L; RO;
Size:	64 bits

IGD graphics memory base address is specified in this register.

Bit	Access	Default Value	Description
63:36	R/W	0000000h	<b>Reserved</b>
35:29	R/W	00h	<b>Memory Base Address:</b> Set by the OS, these bits correspond to address signals [35:29].
28	R/W/L	0b	<b>512-MB Address Mask:</b> This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (Dev2, Func0, Offset 66) for details. This bit is locked in Intel® TXT mode (RO in Intel TXT mode).
27	R/W/L	0b	<b>256-MB Address Mask:</b> This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (Dev2, Func0, offset 66h) for details. This bit is locked in Intel TXT mode (RO in Intel TXT mode).
26:4	RO	000000h	<b>Address Mask:</b> Hardwired to 0's to indicate at least 128-MB address range.
3	RO	1b	<b>Prefetchable Memory:</b> Hardwired to 1 to enable prefetching.
2	RO	1b	<b>Memory Type:</b> 0 = To indicate 32-bit base address. 1 = To indicate 64-bit base address.
1	RO	0b	<b>Reserved</b>
0	RO	0b	<b>Memory/IO Space:</b> Hardwired to 0 to indicate memory space.



### 22.1.12 IOBAR - I/O Base Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	20-23h
Default Value:	00000001h
Access:	RO; R/W
Size:	32 bits

This register provides the base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16-bit I/O Address Space. Bits 2:1 are fixed and return zero, Bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded.

Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD Bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device 2 is turned off or if Internal graphics is disabled. Note that access to this IO BAR is independent of VGA functionality within Device 2. Also note that this mechanism is available only through Function 0 of Device 2 and is not duplicated in Function 1.

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b> Read as 0's, these bits correspond to address signals [31:16].
15:3	R/W	0000h	<b>IO Base Address:</b> Set by the OS, these bits correspond to address signals [15:3].
2:1	RO	00b	<b>Memory Type:</b> Hardwired to 0's to indicate 32-bit address.
0	RO	1b	<b>Memory/IO Space:</b> Hardwired to 1 to indicate IO space.

### 22.1.13 SVID2 - Subsystem Vendor Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	2C-2Dh
Default Value:	0000h
Access:	R/WO
Size:	16 bits

Bit	Access	Default Value	Description
15:0	R/WO	0000h	<b>Subsystem Vendor ID:</b> This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.



## 22.1.14 SID2 - Subsystem Identification

B/D/F/Type:	0/2/0/PCI
Address Offset:	2E-2Fh
Default Value:	0000h
Access:	R/WO
Size:	16 bits

Bit	Access	Default Value	Description
15:0	R/WO	0000h	<b>Subsystem Identification:</b> This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

## 22.1.15 ROMADR - Video BIOS ROM Base Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	30-33h
Default Value:	00000000h
Access:	RO;
Size:	32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Access	Default Value	Description
31:18	RO	0000h	<b>ROM Base Address:</b> Hardwired to 0's
17:11	RO	00h	<b>Address Mask:</b> Hardwired to 0's to indicate 256-KB address range.
10:1	RO	00h	<b>Reserved</b>
0	RO	0b	<b>ROM BIOS Enable:</b> 0 = ROM not accessible.

## 22.1.16 CAPPOINT - Capabilities Pointer

B/D/F/Type:	0/2/0/PCI
Address Offset:	34h
Default Value:	90h
Access:	RO;
Size:	8 bits

Bit	Access	Default Value	Description
7:0	RO	90h	<b>Capabilities Pointer Value:</b> This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List which is the MSI Capabilities ID register at address 90h or the Power Management Capabilities ID registers at address D0h. The value is determined by CAPL[0]



### 22.1.17 INTRLINE - Interrupt Line

B/D/F/Type: 0/2/0/PCI  
Address Offset: 3Ch  
Default Value: 00h  
Access: R/W  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	R/W	00h	<b>Interrupt Connection:</b> Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to.

### 22.1.18 INTRPIN - Interrupt Pin

B/D/F/Type: 0/2/0/PCI  
Address Offset: 3Dh  
Default Value: 01h  
Access: RO;  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	01h	<b>Interrupt Pin:</b> As a single function device, the IGD specifies INTA# as its interrupt pin. 01h:INTA#.

### 22.1.19 MINGNT - Minimum Grant

B/D/F/Type: 0/2/0/PCI  
Address Offset: 3Eh  
Default Value: 00h  
Access: RO;  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Minimum Grant Value:</b> The IGD does not burst as a PCI compliant master.



### 22.1.20 MAXLAT - Maximum Latency

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 3Fh  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Maximum Latency Value:</b> The IGD has no specific requirements for how often it needs to access the PCI bus.

### 22.1.21 MCAPPTR - Capabilities Pointer (to Mirror of Dev0 CAPID)

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 44h  
 Default Value: 48h  
 Access: RO  
 Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	48h	<b>Capabilities Pointer Value:</b> In this case the first capability is the product-specific capability Identifier (CAPID0).

### 22.1.22 MGGC - Mirror of Dev0 (G)MCH Graphics Control

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 52-53h  
 Default Value: 0030h  
 Access: RO  
 Size: 16 bits

All the Bits in this register are Intel TXT locked. In Intel TXT mode R/W bits are RO.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:12	RO	0000b	<b>Reserved</b>
11:8	RO	0h	<b>Reserved</b>



(Sheet 2 of 2)

Bit	Access	Default Value	Description
7:4	RO	0011b	<p><b>Graphics Mode Select (GMS):</b> This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>0000: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80.</p> <p>0001 = Reserved.</p> <p>0010 = Reserved.</p> <p>0011 = Reserved.</p> <p>0100 = Reserved.</p> <p>0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer.</p> <p>0110 = Reserved.</p> <p>0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer.</p> <p>1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer.</p> <p>1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer.</p> <p>1010 = DVMT (UMA) mode, 96 MB of memory pre-allocated for frame buffer.</p> <p>1011 = DVMT (UMA) mode, 160 MB of memory pre-allocated for frame buffer.</p> <p>1100 = DVMT (UMA) mode, 224 MB of memory pre-allocated for frame buffer.</p> <p>1101 = DVMT (UMA) mode, 352 MB of memory pre-allocated for frame buffer.</p>
3:2	RO	00b	<b>Reserved</b>
1	RO	0b	<p><b>IGD VGA Disable (IVD):</b></p> <p>0 = Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.</p> <p>1 = Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80.</p>
0	RO	0b	<b>Reserved</b>



### 22.1.23 MDEVENdev0F0 - Mirror of Dev0 DEVEN

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 54-57h  
 Default Value: 0000001Bh  
 Access: RO  
 Size: 32 bits

Allows for enabling/disabling of PCI devices and functions that are within the MCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

All the Bits in this register are Intel TXT locked. In Intel TXT mode R/W bits are RO.

Bit	Access	Default Value	Description
31:8	RO	000000h	<b>Reserved</b>
7	RO	0b	<b>Reserved</b>
6:5	RO	00b	<b>Reserved</b>
4	RO	1b	<b>Internal Graphics Engine Function 1 (D2F1EN):</b> 0 = Bus 0 Device 2 Function 1 is disabled and hidden. 1 = Bus 0 Device 2 Function 1 is enabled and visible. If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit.
3	RO	1b	<b>Internal Graphics Engine Function 0 (D2F0EN):</b> 0 = Bus 0 Device 2 Function 0 is disabled and hidden. 1 = Bus 0 Device 2 Function 0 is enabled and visible. If this (G)MCH does not have internal graphics capability then Device 2 Function 0 is disabled and hidden independent of the state of this bit.
2	RO	0b	<b>Reserved</b>
1	RO	1b	<b>PCI Express Graphics Port Enable. (D1EN):</b> 0 = Bus 0 Device 1 Function 0 is disabled and hidden. Also gates PCI Express internal clock (lgclk) and asserts PCI Express internal reset (lgrstB). 1 = Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by the device capabilities, SDVO presence HW strap and SDVO/PCI Express concurrent HW strap. Device 1 is disabled on Reset if PCI Express Port is disabled OR the SDVO present strap is sampled high and the SDVO/PCI Express concurrent strap is sampled low.
0	RO	1b	<b>Host Bridge:</b> Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.



## 22.1.24 SSRW - Software Scratch Read Write

B/D/F/Type: 0/2/0/PCI  
Address Offset: 58-5Bh  
Default Value: 00000000h  
Access: R/W  
Size: 32 bits

Bit	Access	Default Value	Description
31:0	R/W	00000000h	<b>Reserved</b>

## 22.1.25 BSM - Base of Stolen Memory

B/D/F/Type: 0/2/0/PCI  
Address Offset: 5C-63h  
Default Value: 0000000000000000h  
Access: RO  
Size: 64 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, (G)MCH claims 1 to 64 MB of DRAM for internal graphics if enabled.

Bit	Access	Default Value	Description
63:36	RO	0000000h	<b>Reserved</b>
35:32	RO	0h	<b>Base of Stolen Memory</b>
31:20	RO	000h	<b>Base of Data Stolen Memory (BSM):</b> This register contains bits 31 to 20 of the base address of data stolen DRAM memory. The host interface determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO	0000h	<b>Reserved</b>



## 22.1.26 HSRW - Hardware Scratch Read Write

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 64-65h  
 Default Value: 0000h  
 Access: R/W  
 Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/W	0000h	<b>Scratchpad Bits</b>

## 22.1.27 MSAC - Multi Size Aperture Control

B/D/F/Type: 0/2/0/PCI  
 Address Offset: 66h  
 Default Value: 02h  
 Access: RO; R/W  
 Size: 8 bits

This register determines the size of the graphics memory aperture in Function 0. By default the aperture size is 256 MB. Only the System BIOS will write this register based on pre-boot address allocation efforts, but the graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.

Bit	Access	Default Value	Description
7:4	R/W	0h	<b>Scratch Bits Only:</b> Have no physical effect on hardware.
3	RO	0b	<b>Reserved</b>
2:1	R/W	01b	<b>Aperture Size (LHSAS):</b> 11 = bits [28:27] of GMADR register are made Read only and forced to zero, allowing only 512 MB of GMADR 01 = bit [28] of GMADR is made R/W and bit [27] of GMADR is forced to zero allowing 256 MB of GMADR 00/10 = Illegal programming. This bit is Intel® TXT locked, becomes read-only when trusted environment is launched.
0	RO	0b	<b>Reserved</b>



## 22.1.28 MC - Message Control

B/D/F/Type:	0/2/0/PCI
Address Offset:	92-93h
Default Value:	0000h
Access:	RO; R/W
Size:	16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access	Default Value	Description												
15:8	RO	00h	<b>Reserved</b>												
7	RO	0b	<b>64-bit Address Capable:</b> Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32-bit/4-GB limit.												
6:4	R/W	000b	<b>Multiple Message Enable (MME):</b> System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.												
3:1	RO	000b	<b>Multiple Message Capable (MMC):</b> System software reads this field to determine the number of messages being requested by this device. Value: Number of Messages Requested 000: 1 All of the following are reserved in this implementation: 0012 <table border="1"><tr><td>010</td><td>4</td></tr><tr><td>011</td><td>8</td></tr><tr><td>100</td><td>16</td></tr><tr><td>101</td><td>32</td></tr><tr><td>110</td><td>Reserved.</td></tr><tr><td>111</td><td>Reserved.</td></tr></table>	010	4	011	8	100	16	101	32	110	Reserved.	111	Reserved.
010	4														
011	8														
100	16														
101	32														
110	Reserved.														
111	Reserved.														
0	R/W	0b	<b>MSI Enable (MSIEN):</b> Controls the ability of this device to generate MSIs.												



## 22.1.29 MA - Message Address

B/D/F/Type:	0/2/0/PCI
Address Offset:	94-97h
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

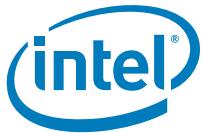
A read from this register produces undefined results.

Bit	Access	Default Value	Description
31:2	R/W	00000000h	<b>Message Address:</b> Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	<b>Force Dword Align:</b> Hardwired to 0 so that addresses assigned by system software are always aligned on a dword address boundary.

## 22.1.30 MD - Message Data

B/D/F/Type:	0/2/0/PCI
Address Offset:	98-99h
Default Value:	0000h
Access:	R/W
Size:	16 bits

Bit	Access	Default Value	Description
15:0	R/W	0000h	<b>Message Data:</b> Base message data pattern assigned by system software and used to handle an MSI from the device.  When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.



### 22.1.31 PMCAPID - Power Management Capabilities ID

B/D/F/Type: 0/2/0/PCI  
Address Offset: D0-D1h  
Default Value: 0001h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	<b>NEXT_PTR (NEXT_PTR):</b> This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO	01h	<b>CAP_ID (CAP_ID):</b> SIG defines this ID is 01h for power management.

### 22.1.32 PMCAP - Power Management Capabilities

B/D/F/Type: 0/2/0/PCI  
Address Offset: D2-D3h  
Default Value: 0023h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	<b>PME Support (PME_SUPPORT):</b> This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO	0b	<b>D2 (D2):</b> The D2 power management state is not supported. This bit is hardwired to 0.
9	RO	0b	<b>D1 (D1):</b> Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO	000b	<b>Reserved. (RSVD):</b>
5	RO	1b	<b>Device Specific Initialization (DSI):</b> Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO	0b	<b>Auxiliary Power Source (AUXPWRSRC):</b> Hardwired to 0.
3	RO	0b	<b>PME Clock (PMECLK):</b> Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO	011b	<b>Version (VER):</b> A value of 011b indicates that this function complies with revision 1.2 of the <i>PCI Power Management Interface Specification</i>



### 22.1.33 PMCS - Power Management Control/Status

B/D/F/Type: 0/2/0/PCI  
 Address Offset: D4-D5h  
 Default Value: 0000h  
 Access: RO; R/W  
 Size: 16 bits

Bit	Access	Default Value	Description															
15	RO	0b	<b>PME_Status (PME_STATUS):</b> This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).															
14:13	RO	00b	<b>Reserved</b>															
12:9	RO	0h	<b>Reserved</b>															
8	RO	0b	<b>PME_En (PME_EN):</b> This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.															
7:4	RO	0h	<b>Reserved</b>															
3	RO	0b	<b>Reserved</b>															
2	RO	0b	<b>Reserved</b>															
1:0	R/W	00b	<p><b>PowerState (PWR_STATE):</b> This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs.</p> <p>On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the BIOS specification.</p> <table border="1"> <thead> <tr> <th>Bits[1:0]</th> <th>Power state</th> <th></th> </tr> </thead> <tbody> <tr> <td>00</td> <td>D0</td> <td>Default</td> </tr> <tr> <td>01</td> <td>D1</td> <td>Not Supported</td> </tr> <tr> <td>10</td> <td>D2</td> <td>Not Supported</td> </tr> <tr> <td>11</td> <td>D3</td> <td></td> </tr> </tbody> </table>	Bits[1:0]	Power state		00	D0	Default	01	D1	Not Supported	10	D2	Not Supported	11	D3	
Bits[1:0]	Power state																	
00	D0	Default																
01	D1	Not Supported																
10	D2	Not Supported																
11	D3																	



### 22.1.34 SWSMI - Software SMI

B/D/F/Type:	0/2/0/PCI
Address Offset:	E0-E1h
Default Value:	0000h
Access:	R/W
Size:	16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2F0address E0h-E1h must be reserved for this register.

Bit	Access	Default Value	Description
15:8	R/W	00h	<b>SW Scratch Bits (SW_SCRATCH)</b>
7:1	R/W	00h	<b>Software Flag (SOFTWARE_FLAG):</b> Used to indicate caller and SMI function desired, as well as return result.
0	R/W	0b	<b>(G)MCH Software SMI Event ((G)MCH_SOFT_SMI_EVENT):</b> When Set this bit will trigger an SMI. Software must write a 0 to clear this bit.

### 22.1.35 ASLE - System Display Event Register

B/D/F/Type:	0/2/0/PCI
Address Offset:	E4-E7h
Default Value:	00000000h
Access:	R/W
Size:	32 bits

The exact use of these bytes including whether they are addressed as bytes, words, or as a dword, is not pre-determined but subject to change by driver and System BIOS teams (acting in unison).

Bit	Access	Default Value	Description
31:24	R/W	00h	<b>ASLE Scratch Trigger3 (ASLE_SCRATCH_3):</b> When written, this scratch byte triggers an interrupt when IEF Bit 0 is enabled and IMR Bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	R/W	00h	<b>ASLE Scratch Trigger2 (ASLE_SCRATCH_2):</b> When written, this scratch byte triggers an interrupt when IEF Bit 0 is enabled and IMR Bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	R/W	00h	<b>ASLE Scratch Trigger 1 (ASLE_SCRATCH_1):</b> When written, this scratch byte triggers an interrupt when IEF Bit 0 is enabled and IMR Bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	R/W	00h	<b>ASLE Scratch Trigger 0 (ASLE_SCRATCH_0):</b> When written, this scratch byte triggers an interrupt when IEF Bit 0 is enabled and IMR Bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.



## 22.1.36 GCFC - Graphics Clock Frequency Control

B/D/F/Type: 0/2/0/PCI  
 Address Offset: F0-F1h  
 Default Value: 1606h  
 Access: RO; R/W  
 Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	<b>Reserved</b>
14	R/W	0b	<b>Gate Core Display Clock (GCRC):</b> 0 = cdclk is running 1 = cdclk is gated
13	RO	0b	<b>Reserved</b>
12	R/W	1b	<b>Reserved</b>
11:8	R/W	0110b	<b>Reserved</b>
7	RO	0b	<b>Reserved</b>
6	R/W	0b	<b>Reserved</b>
5	R/W	0b	<b>Reserved</b>
4	R/W	0b	<b>Reserved</b>
3:0	R/W	0110b	<b>Graphics Core Render Clock Select (CRCLKFREQ)</b> 1000 = 266 MHz 1001 = 320 MHz 1011 = 400 MHz 1101 = 533 MHz 1110 = Reserved Others = Reserved



### 22.1.37 LBB - Legacy Backlight Brightness

B/D/F/Type: 0/2/0/PCI  
Address Offset: F4-F7h  
Default Value: 00000000h  
Access: R/W  
Size: 32 bits

This register can be accessed by either Byte, Word, or dword PCI config cycles. A write to this register will cause the Backlight Event (Display B Interrupt) if enabled.

Bit	Access	Default Value	Description
31:24	R/W	00h	<b>LBPC Scratch Trigger3 (LBPC_SCRATCH_3):</b> When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	R/W	00h	<b>LBPC Scratch Trigger2 (LBPC_SCRATCH_2):</b> When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	R/W	00h	<b>LBPC Scratch Trigger1 (LBPC_SCRATCH_1):</b> When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	R/W	00h	<b>Legacy Backlight Brightness (LBES):</b> The value of zero is the lowest brightness setting and 255 is the brightest. A write to this register will cause a flag to be set (LBES) in the PIPEBSTATUS register and cause an interrupt if Backlight event in the PIPEBSTATUS register and cause an Interrupt if Backlight Event (LBEE) and Display B Event is enabled by software.



### 22.1.38 ASLS - ASL Storage

B/D/F/Type:	0/2/0/PCI
Address Offset:	FC-FFh
Default Value:	00000000h
Access:	R/W
Size:	32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software. For each device, the ASL control method will require two bits for \_DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for \_DGS (enable/disable requested), and two bits for \_DCS (enabled now/disabled now, connected or not).

Bit	Access	Default Value	Description
31:0	R/W	00000000h	<b>Software Controlled Usage to Support Device Switching (SOFT_CTRL_DEV_SWITCH):</b> R/W according to a software controlled usage to support device switching

## 22.2 Device 2 Function 1 PCI Configuration Registers

(Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID2	0	1	8086h	RO
Device Identification	DID2	2	3	2A43h	RO
PCI Command	PCICMD2	4	5	0000h	RO; R/W
PCI Status	PCISTS2	6	7	0090h	RO
Revision Identification	RID2	8	8	00h	RO
Class Code Register	CC	9	B	038000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT2	D	D	00h	RO
Header Type	HDR2	E	E	80h	RO
Reserved		F	F		
Memory Mapped Range Address	MMADR	10	17	000000000000004h	RO; R/W
Subsystem Vendor Identification	SVID2	2C	2D	0000h	RO
Subsystem Identification	SID2	2E	2F	0000h	RO
Video BIOS ROM Base Address	ROMADR	30	33	00000000h	RO
Capabilities Pointer	CAPPOINT	34	34	D0h	RO
Minimum Grant	MINGNT	3E	3E	00h	RO
Maximum Latency	MAXLAT	3F	3F	00h	RO
Mirror of Dev0 Capability Pointer	MCAPPTR	44	44	48h	RO



## (Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		48	51		
Mirror of Dev0 (G)MCH Graphics Control	MGGC	52	53	0030h	RO
Mirror of Dev0 DEVEN	MDEVENDev0 F0	54	57	0000001Bh	RO
Software Scratch Read Write	SSRW	58	5B	00000000h	RO
Base of Stolen Memory	BSM	5C	63	000000000000000h	RO
Hardware Scratch Read Write	HSRW	64	65	0000h	RO
Multi Size Aperture Control	MSAC	66	66	02h	RO
Reserved		A8	CF		
Power Management Capabilities ID	PMCAPID	D0	D1	0001h	RO
Power Management Capabilities	PMCAP	D2	D3	0023h	RO
Power Management Control/ Status	PMCS	D4	D5	0000h	RO; R/W
Reserved		DA	DC		
Software SMI	SWSMI	E0	E1	0000h	RO
System Display Event Register	ASLE	E4	E7	00000000h	RO
Software SCI	SWSCI	E8	E9	0000h	RO
Graphics Clock Frequency and Gating Control	GCFG C	F0	F1	1606h	RO
Graphics Clock PLL Control	GCP LLC	F2	F3	0734h	RO
Legacy Backlight Brightness	LBB	F4	F7	00000000h	RO
Manufacturing ID	MID2	F8	FB	00000F90h	RO
ASL Storage	ASLS	FC	FF	00000000h	R/W



## 22.2.1 VID2 - Vendor Identification

B/D/F/Type:	0/2/1/PCI
Address Offset:	0-1h
Default Value:	8086h
Access:	RO
Size:	16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	<b>Vendor Identification Number (VID):</b> PCI standard identification for Intel.

## 22.2.2 DID2 - Device Identification

B/D/F/Type:	0/2/1/PCI
Address Offset:	2-3h
Default Value:	2A43h
Access:	RO
Size:	16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID's is necessary for allowing distinct Plug and Play enumeration of Function 1 when both Function 0 and Function 1 have the same class code.

Bit	Access	Default Value	Description
15:0	RO	2A43h	<b>Device Identification Number (DID2):</b> Identifier assigned to the (G)MCH Device 2 Function 1.



### 22.2.3 PCICMD2 - PCI Command

B/D/F/Type:	0/2/1/PCI
Address Offset:	4-5h
Default Value:	0000h
Access:	RO; R/W
Size:	16 bits

This 16-bit register provides basic control over the IGD ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access	Default Value	Description
15:11	RO	00h	<b>Reserved</b>
10	RO	0b	<b>Reserved</b>
9	RO	0b	<b>Fast Back-to-Back (FB2B):</b> Not Implemented. Hardwired to 0.
8	RO	0b	<b>SERR Enable (SERRE):</b> Not Implemented. Hardwired to 0.
7	RO	0b	<b>Address/Data Stepping Enable (ADSTEP):</b> Not Implemented. Hardwired to 0.
6	RO	0b	<b>Parity Error Enable (PERRE):</b> Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO	0b	<b>VGA Palette Snoop Enable (VGASNOOP):</b> This bit is hardwired to 0 to disable snooping.
4	RO	0b	<b>Memory Write and Invalidate Enable (MWIE):</b> Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO	0b	<b>Special Cycle Enable (SCE):</b> This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W	0b	<b>Bus Master Enable (BME):</b> Set to 1 to enable the IGD to function as a PCI compliant master. Set to 0 to disable IGD bus mastering.
1	R/W	0b	<b>Memory Access Enable (MAE):</b> This bit controls the IGD response to memory space accesses. 0 = Disable 1 = Enable
0	R/W	0b	<b>I/O Access Enable (IOAE):</b> This bit controls the IGD response to I/O space accesses. 0 = Disable 1 = Enable

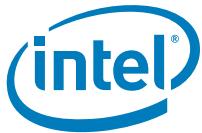


## 22.2.4 PCISTS2 - PCI Status

B/D/F/Type:	0/2/1/PCI
Address Offset:	6-7h
Default Value:	0090h
Access:	RO
Size:	16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access	Default Value	Description
15	RO	0b	<b>Detected Parity Error (DPE):</b> Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO	0b	<b>Signaled System Error (SSE):</b> The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO	0b	<b>Received Master Abort Status (RMAS):</b> The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO	0b	<b>Received Target Abort Status (RTAS):</b> The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO	0b	<b>Signaled Target Abort Status (STAS):</b> Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO	00b	<b>DEVSEL Timing (DEVT):</b> N/A. These bits are hardwired to "00".
8	RO	0b	<b>Master Data Parity Error Detected (DPD):</b> Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO	1b	<b>Fast Back-to-Back (FB2B):</b> Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO	0b	<b>User Defined Format (UDF):</b> Hardwired to 0.
5	RO	0b	<b>66-MHz PCI Capable (66C):</b> N/A - Hardwired to 0.
4	RO	1b	<b>Capability List (CLIST):</b> This bit is set to 1 to indicate that the register at 34h provides an offset into the function PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO	0b	<b>Interrupt Status:</b> Hardwired to 0.
2:0	RO	0h	<b>Reserved</b>



## 22.2.5 RID2 - Revision Identification

B/D/F/Type:	0/2/1/PCI
Address Offset:	8h
Default Value:	00h
Access:	RO
Size:	8 bits

RID Definition: This register contains the revision number of the (G)MCH Device 0. Following PCI Reset, the SRID value is selected to be read. When a write occurs to this register, the write data is compared to the hardwired RID Select Key Value, which is 69h. If the data matches this key, a flag is set that enables the CRID value to be read through this register.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Revision Identification Number (RID):</b> This is an 8-bit value that indicates the revision identification number for the (G)MCH. 07h: B-3 stepping

## 22.2.6 CC - Class Code Register

B/D/F/Type:	0/2/1/PCI
Address Offset:	9-Bh
Default Value:	038000h
Access:	RO
Size:	24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access	Default Value	Description
23:16	RO	03h	<b>Base Class Code (BCC):</b> This is an 8-bit value that indicates the base class code for the (G)MCH. This code has the value 03h, indicating a Display Controller.
15:8	RO	80h	<b>Sub-Class Code (SUBCC):</b> 80h = Non VGA
7:0	RO	00h	<b>Programming Interface (PI):</b> 00h = Hardwired as a Display controller.



## 22.2.7 CLS - Cache Line Size

B/D/F/Type:	0/2/1/PCI
Address Offset:	Ch
Default Value:	00h
Access:	RO
Size:	8 bits

The IGD does not support this register as a PCI slave.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Cache Line Size (CLS):</b> This field is hardwired to 0's. The IGD as a PCI-compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

## 22.2.8 MLT2 - Master Latency Timer

B/D/F/Type:	0/2/1/PCI
Address Offset:	Dh
Default Value:	00h
Access:	RO
Size:	8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

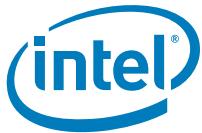
Bit	Access	Default Value	Description
7:0	RO	00h	<b>Master Latency Timer Count Value:</b> Hardwired to 0's.

## 22.2.9 HDR2 - Header Type

B/D/F/Type:	0/2/1/PCI
Address Offset:	Eh
Default Value:	80h
Access:	RO
Size:	8 bits

This register contains the Header Type of the IGD.

Bit	Access	Default Value	Description
7	RO	1b	<b>Multi Function Status (MFunc):</b> Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the Mfunc bit is also set.
6:0	RO	00h	<b>Header Code (H):</b> This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a Type 0 configuration space format.



## 22.2.10 BIST - Built In Self Test

B/D/F/Type:	0/2/1/PCI
Address Offset:	Fh
Default Value:	00h
Access:	RO
Size:	8 bits

This register is used for control and status of Built In Self Test (BIST).

Bit	Access	Default Value	Description
7	RO	0b	<b>BIST Supported:</b> BIST is not supported. This bit is hardwired to 0.
6:0	RO	00h	<b>Reserved</b>

## 22.2.11 MMADR - Memory Mapped Range Address

B/D/F/Type:	0/2/1/PCI
Address Offset:	10-17h
Default Value:	0000000000000004h
Access:	RO; R/W
Size:	64 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by Bits [35:20].

Bit	Access	Default Value	Description
63:36	R/W	0000000h	<b>Reserved</b>
35:20	R/W	0000h	<b>Memory Base Address:</b> Set by the OS, these bits correspond to address signals [35:20].
19:4	RO	0000h	<b>Address Mask:</b> Hardwired to 0's to indicate 512-KB address range (aligned to 1-M boundary).
3	RO	0b	<b>Prefetchable Memory:</b> Hardwired to 0 to prevent prefetching.
2	RO	1b	<b>Memory Type:</b> 0 = To indicate 32-bit base address. 1 = To indicate 64-bit base address.
1	RO	0b	<b>Reserved</b>
0	RO	0b	<b>Memory/IO Space:</b> Hardwired to 0 to indicate memory space.



## 22.2.12 SVID2 - Subsystem Vendor Identification

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 2C-2Dh  
 Default Value: 0000h  
 Access: RO  
 Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	0000h	<p><b>Subsystem Vendor ID:</b> This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.</p> <p><b>NOTE:</b> This is a RO copy of the Dev2Fn0 value.</p>

## 22.2.13 SID2 - Subsystem Identification

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 2E-2Fh  
 Default Value: 0000h  
 Access: RO  
 Size: 16 bits

Bit	Access	Default Value	Description
15:0	RO	0000h	<p><b>Subsystem Identification:</b> This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.</p> <p><b>NOTE:</b> This is a RO copy of the Dev2Fx0 value.</p>

## 22.2.14 ROMADR - Video BIOS ROM Base Address

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 30-33h  
 Default Value: 00000000h  
 Access: RO  
 Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Access	Default Value	Description
31:18	RO	0000h	<b>ROM Base Address:</b> Hardwired to 0.
17:11	RO	00h	<b>Address Mask:</b> Hardwired to 0's to indicate 256-KB address range.
10:1	RO	00h	<b>Reserved</b> Hardwired to 0's.
0	RO	0b	<b>ROM BIOS Enable:</b> 0 = ROM not accessible.



### 22.2.15 CAPPOINT - Capabilities Pointer

B/D/F/Type: 0/2/1/PCI  
Address Offset: 34h  
Default Value: D0h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	D0h	<b>Capabilities Pointer Value (CPV):</b> This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List which is the Power Management Capabilities ID registers at address D0h.

### 22.2.16 MINGNT - Minimum Grant

B/D/F/Type: 0/2/1/PCI  
Address Offset: 3Eh  
Default Value: 00h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Minimum Grant Value:</b> The IGD does not burst as a PCI-compliant master.

### 22.2.17 MAXLAT - Maximum Latency

B/D/F/Type: 0/2/1/PCI  
Address Offset: 3Fh  
Default Value: 00h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Maximum Latency Value:</b> The IGD has no specific requirements for how often it needs to access the PCI bus.



## 22.2.18 MCAPPTR - Mirror of Dev0 Capability Pointer

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 44h  
 Default Value: 48h  
 Access: RO  
 Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	48h	<b>Capabilities Pointer Value:</b> In this case the first capability is the product-specific capability Identifier (CAPID0).

## 22.2.19 MGGC - Mirror of Dev0 (G)MCH Graphics Control

B/D/F/Type: 0/2/1/PCI  
 Address Offset: 52-53h  
 Default Value: 0030h  
 Access: RO  
 Size: 16 bits

All the bits in this register are Intel TXT locked. In Intel TXT mode R/W bits are RO.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:12	RO	0000b	<b>Reserved</b>
11:8	RO	0h	<b>Reserved</b>



## (Sheet 2 of 2)

Bit	Access	Default Value	Description
7:4	RO	0011b	<p><b>Graphics Mode Select (GMS):</b> This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>0000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80.</p> <p>0001 = Reserved.</p> <p>0010 = Reserved.</p> <p>0011 = Reserved.</p> <p>0100 = Reserved.</p> <p>0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer.</p> <p>0110 = Reserved.</p> <p>0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer.</p> <p>1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer.</p> <p>1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer.</p> <p>1010 = DVMT (UMA) mode, 96 MB of memory pre-allocated for frame buffer.</p> <p>1011 = DVMT (UMA) mode, 160 MB of memory pre-allocated for frame buffer.</p> <p>1100 = DVMT (UMA) mode, 224 MB of memory pre-allocated for frame buffer.</p> <p>1101 = DVMT (UMA) mode, 352 MB of memory pre-allocated for frame buffer.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"><li>1. This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. This register is also Intel® TXT lockable.</li><li>2. Hardware does not clear or set any of these bits automatically based on IGD being disabled/ enabled.</li><li>3. BIOS Requirement: BIOS must not set this field to 0000 if IVD (Bit 1 of this register) is 0.</li></ol>
3:2	RO	00b	<b>Reserved</b>
1	RO	0b	<p><b>IGD VGA Disable (IVD):</b></p> <p>0 = Enable (Default). Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is "00."</p> <p>1 = Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 Function 0 Class Code register is 80. "</p>
0	RO	0b	<b>Reserved</b>



## 22.2.20 MDEVENdev0F0 - Mirror of Dev0 DEVEN

B/D/F/Type:	0/2/1/PCI
Address Offset:	54-57h
Default Value:	0000001Bh
Access:	RO
Size:	32 bits

Allows for enabling/disabling of PCI devices and functions that are within the MCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

All the Bits in this register are Intel TXT locked. In Intel TXT mode R/W bits are RO.

Bit	Access	Default Value	Description
31:8	RO	000000h	<b>Reserved</b>
7	RO	0b	<b>Reserved</b>
6:5	RO	00b	<b>Reserved</b>
4	RO	1b	<b>Internal Graphics Engine Function 1 (D2F1EN):</b> 0 = Bus 0 Device 2 Function 1 is disabled and hidden. 1 = Bus 0 Device 2 Function 1 is enabled and visible. If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit.
3	RO	1b	<b>Internal Graphics Engine Function 0 (D2FOEN):</b> 0 = Bus 0 Device 2 Function 0 is disabled and hidden. 1 = Bus 0 Device 2 Function 0 is enabled and visible. If this (G)MCH does not have internal graphics capability then Device 2 Function 0 is disabled and hidden independent of the state of this bit.
2	RO	0b	<b>Reserved</b>
1	RO	1b	<b>PCI Express* Graphics Port Enable. (D1EN):</b> 0 = Bus 0 Device 1 Function 0 is disabled and hidden. Also gates PCI Express internal clock (lgclk) and asserts PCI Express internal reset (lgrstB). 1 = Bus 0 Device 1 Function 0 is enabled and visible. Default value is determined by the device capabilities, SDVO presence HW strap and SDVO/PCI Express concurrent HW strap. Device 1 is disabled on Reset if PCI Express Port is disabled OR the SDVO present strap is sampled high and the SDVO/PCI Express concurrent strap is sampled low.
0	RO	1b	<b>Host Bridge:</b> Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.



### 22.2.21 BSM - Base of Stolen Memory

B/D/F/Type:	0/2/1/PCI
Address Offset:	5C-63h
Default Value:	0000000000000000h
Access:	RO
Size:	64 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, (G)MCH claims 1 to 64 MB of DRAM for internal graphics if enabled.

Bit	Access	Default Value	Description
63:36	RO	0000000h	<b>Reserved</b>
35:32	RO	0h	<b>Base of Stolen Memory:</b>
31:20	RO	000h	<b>Base of Stolen Memory (BSM):</b> This register contains Bits 31 to 20 of the base address of stolen DRAM memory. The host interface determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO	0000h	<b>Reserved</b>

### 22.2.22 HSRW - Hardware Scratch Read Write

B/D/F/Type:	0/2/1/PCI
Address Offset:	64-65h
Default Value:	0000h
Access:	RO
Size:	16 bits

Bit	Access	Default Value	Description
15:0	RO	0000h	<b>Reserved</b>



## 22.2.23 MSAC - Multi Size Aperture Control

B/D/F/Type:	0/2/1/PCI
Address Offset:	66h
Default Value:	02h
Access:	RO
Size:	8 bits

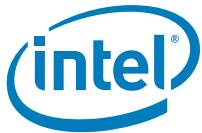
This register determines the size of the graphics memory aperture in Function 0. By default, the aperture size is 256 MB. Only the System BIOS will write this register based on pre-boot address allocation efforts, but the graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.

Bit	Access	Default Value	Description
7:4	RO	0h	<b>Scratch Bits Only:</b> Have no physical effect on hardware.
3	RO	0b	<b>Reserved</b>
2:1	RO	01b	<b>Aperture Size (LHSAS):</b> 11 = Bits [28:27] of GMADR register are made Read only and forced to zero, allowing only 512 MB of GMADR 01 = Bit [28] of GMADR is made R/W and bit [27] of GMADR is forced to zero allowing 256 MB of GMADR 00/10 = Illegal programming. This bit is Intel® TXT locked, becomes read-only when trusted environment is launched.
0	RO	0b	<b>Reserved</b>

## 22.2.24 PMCAPID - Power Management Capabilities ID

B/D/F/Type:	0/2/1/PCI
Address Offset:	D0-D1h
Default Value:	0001h
Access:	RO
Size:	16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	<b>NEXT_PTR (NEXT_PTR):</b> This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO	01h	<b>CAP_ID (CAP_ID):</b> PCI-SIG defines this ID is 01h for power management.



## 22.2.25 PMCAP - Power Management Capabilities

B/D/F/Type: 0/2/1/PCI  
Address Offset: D2-D3h  
Default Value: 0023h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	<b>PME Support (PME_SUPPORT):</b> This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO	0b	<b>D2 (D2):</b> The D2 power management state is not supported. This bit is hardwired to 0.
9	RO	0b	<b>D1 (D1):</b> Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO	000b	<b>Reserved. (RSVD):</b>
5	RO	1b	<b>Device Specific Initialization (DSI):</b> Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO	0b	<b>Auxiliary Power Source (AUX_PWR_SRC):</b> Hardwired to 0.
3	RO	0b	<b>PME Clock (PME_CLK):</b> Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO	011b	<b>Version (VER):</b> A value of 011b indicates that this function complies with revision 1.2 of the <i>PCI Power Management Interface Specification</i>



## 22.2.26 PMCS - Power Management Control/Status

B/D/F/Type: 0/2/1/PCI  
 Address Offset: D4-D5h  
 Default Value: 0000h  
 Access: RO; R/W  
 Size: 16 bits

**Note:** This register is **not** mirrored in Dev2 Func1 space (i.e., Dev2 Func1 PMCS is completely independent register). Bits [1:0] – power state of IGD – should be updated in both Dev2 Func0 and Dev2 Func1.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15	RO	0b	<b>PME_Status (PME_STATUS):</b> This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO	00b	<b>Data Scale (Reserved):</b> The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.
12:9	RO	0h	<b>Data_Select (Reserved):</b> The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.
8	RO	0b	<b>PME_En (PME_EN):</b> This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:4	RO	0h	<b>Reserved (RSVD):</b> Always returns 0 when read, write operations have no effect.
3	RO	0b	<b>No_Soft_reset (NOSOFTRESET):</b> When set (1), this bit indicates that devices transitioning from D <sub>3hot</sub> to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from D <sub>3hot</sub> to the D0 initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.  When clear (0) devices do perform an internal reset upon transitioning from D <sub>3hot</sub> to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D <sub>3hot</sub> to the D0 state, full re-initialization sequence is needed to return the device to D0 initialized.  Regardless of this bit, devices that transition from D <sub>3hot</sub> to D0 by a system or bus segment reset will return to the device state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	RO	0b	<b>Reserved (RSVD):</b> Always returns 0 when read, write operations have no effect.



(Sheet 2 of 2)

Bit	Access	Default Value	Description															
1:0	R/W	00b	<p><b>PowerState (PWR_STATE):</b> This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs.</p> <p>On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the BIOS specification</p> <table border="1"><thead><tr><th>Bits[1:0]</th><th>Power state</th><th></th></tr></thead><tbody><tr><td>00</td><td>D0</td><td>Default</td></tr><tr><td>01</td><td>D1</td><td>Not Supported</td></tr><tr><td>10</td><td>D2</td><td>Not Supported</td></tr><tr><td>11</td><td>D3</td><td></td></tr></tbody></table> <p>Bits [1:0] of PMCS register should be programmed in both dev2 func0 and dev2 func1</p>	Bits[1:0]	Power state		00	D0	Default	01	D1	Not Supported	10	D2	Not Supported	11	D3	
Bits[1:0]	Power state																	
00	D0	Default																
01	D1	Not Supported																
10	D2	Not Supported																
11	D3																	

## 22.2.27 SWSMI - Software SMI

B/D/F/Type: 0/2/0/PCI  
Address Offset: E0-E1h  
Default Value: 0000h  
Access: R/W  
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2F0address E0h-E1h must be reserved for this register.

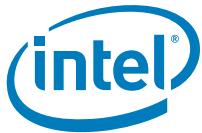
Bit	Access	Default Value	Description
15	RO	0b	<b>SMI or SCI Event Select (SMISCISEL):</b> If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register at offset E0h. If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.
14:1	RO	0000h	<b>SW Scratch Bits (SW_SCRATCH):</b> R/W bits not used by hardware. Scratch.
0	RO	0b	<b>(G)MCH Software SCI Event (GSSCIE):</b> If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, (G)MCH will send a SCI message via DMI link to ICH to cause the TCOSCI_STS bit in its GPE0 register to be set to 1. Software must write a 0 to clear this bit.



## 22.2.28 GCFG - Graphics Clock Frequency and Gating Control

B/D/F/Type: 0/2/1/PCI  
 Address Offset: F0-F1h  
 Default Value: 1606h  
 Access: RO  
 Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	<b>Reserved</b>
14	R/W	0b	<b>Gate Core Display Clock (GCRC):</b> 0 = cdclk is running 1 = cdclk is gated
13	RO	0b	<b>Reserved</b>
12	R/W	1b	<b>Reserved</b>
11:8	R/W	0110b	<b>Reserved</b>
7	RO	0b	<b>Reserved</b>
6	R/W	0b	<b>Reserved</b>
5	R/W	0b	<b>Reserved</b>
4	R/W	0b	<b>Reserved</b>
3:0	R/W	0110b	<b>Reserved</b>



## 22.2.29 LBB - Legacy Backlight Brightness

B/D/F/Type: 0/2/1/PCI  
Address Offset: F4-F7h  
Default Value: 00000000h  
Access: RO  
Size: 32 bits

This register can be accessed by either byte, word, or dword PCI config cycles. A write to this register will cause the Backlight Event (Display B Interrupt) if enabled.

Bit	Access	Default Value	Description
31:24	RO	00h	<b>LBPC Scratch Trigger3 (LBPC_SCRATCH_3):</b> When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR, etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common. (Mirrored from Dev2 Func0)
23:16	RO	00h	<b>LBPC Scratch Trigger2 (LBPC_SCRATCH_2):</b> When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR, etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common. (Mirrored from Dev2 Func0)
15:8	RO	00h	<b>LBPC Scratch Trigger1 (LBPC_SCRATCH_1):</b> When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR, etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common. (Mirrored from Dev2 Func0)
7:0	RO	00h	<b>Legacy Backlight Brightness (LBES):</b> The value of zero is the lowest brightness setting and 255 is the brightest. A write to this register will cause a flag to be set (LBES) in the PIPEBSTATUS register and cause an interrupt if Backlight event in the PIPEBSTATUS register and cause an Interrupt if Backlight Event (LBEE) and Display B Event is enabled by software. (Mirrored from Dev2 Func0)

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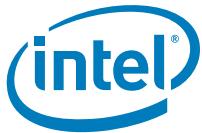


## 23 Intel® Management Engine Subsystem PCI Device 3

### 23.1 Intel® Management Engine Interface (Intel® MEI) PCI Device 3 Function 0

(Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Identifiers	ID	0	3	2A448086h	RO
Command	CMD	4	5	0000h	RO; R/W
Device Status	STS	6	7	0010h	RO
Revision Identification	RID	8	8	00h	RO
Class Code	CC	9	B	078000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HTYPE	E	E	80h	RO
Built-In Self Test	BIST	F	F	00h	RO
HECI MMIO Base Address	HECI_MBAR	10	17	000000000000 00004h	RO; R/W
Sub System Identifiers	SS	2C	2F	00000000h	R/WO
Capabilities Pointer	CAP	34	34	50h	RO
Interrupt Information	INTR	3C	3D	0100h	RO; R/W
Minimum Grant	MGNT	3E	3E	00h	RO
Maximum Latency	MLAT	3F	3F	00h	RO
Host Firmware Status	HFS	40	43	00000000h	RO
PCI Power Management capability ID	PID	50	51	8C01h	RO
PCI Power Management Capabilities	PC	52	53	C803h	RO
PCI Power Management Control and Status	PMCS	54	55	0008h	R/WC; RO; R/W
Message Signaled Interrupt Identifiers	MID	8C	8D	0005h	RO
Message Signaled Interrupt Message Control	MC	8E	8F	0080h	RO; R/W
Message Signaled Interrupt Message Address	MA	90	93	00000000h	RO; R/W



(Sheet 2 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Reserved		94	97		
Message Signaled Interrupt Message Data	MD	98	99	0000h	R/W
HECI Interrupt Delivery Mode	HIDM	A0	A0	00h	R/W

### 23.1.1 ID - Identifiers

B/D/F/Type: 0/3/0/PCI  
Address Offset: 0-3h  
Default Value: 2A448086h  
Access: RO  
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	2A44h	<b>Device ID (DID):</b> Indicates the device number assigned by Intel.
15:0	RO	8086h	<b>Vendor ID (VID):</b> 16-bit field which indicates Intel is the vendor, assigned by the PCI SIG.

### 23.1.2 CMD - Command

B/D/F/Type: 0/3/0/PCI  
Address Offset: 4-5h  
Default Value: 0000h  
Access: RO; R/W  
Size: 16 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:11	RO	00000b	<b>Reserved</b>
10	R/W	0b	<b>Interrupt Disable (ID):</b> Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9	RO	0b	<b>Fast Back-to-Back Enable (FBE):</b> Not implemented, hardwired to 0.
8	RO	0b	<b>SERR# Enable (SEE):</b> Not implemented, hardwired to 0.
7	RO	0b	<b>Wait Cycle Enable (WCC):</b> Not implemented, hardwired to 0.
6	RO	0b	<b>Parity Error Response Enable (PEE):</b> Not implemented, hardwired to 0.
5	RO	0b	<b>VGA Palette Snooping Enable (VGA):</b> Not implemented, hardwired to 0



(Sheet 2 of 2)

Bit	Access	Default Value	Description
4	RO	0b	<b>Memory Write and Invalidate Enable (MWIE):</b> Not implemented, hardwired to 0.
3	RO	0b	<b>Special Cycle Enable (SCE):</b> Not implemented, hardwired to 0.
2	R/W	0b	<b>Bus Master Enable (BME):</b> Controls the Intel MEI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, Intel MEI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an Intel MEI MSI.  When this bit is 0, Intel MEI is blocked from generating MSI to the host CPU.  <b>NOTE:</b> This bit does not block Intel MEI accesses to Intel Management Engine -UMA, i.e., writes or reads to the host and Intel Management Engine circular buffers through the read window and write window registers still cause Intel Management Engine backbone transactions to Intel Management Engine -UMA.
1	R/W	0b	<b>Memory Space Enable (MSE):</b> Controls access to the Intel MEI host controller's memory mapped register space.
0	RO	0b	<b>I/O Space Enable (IOSE):</b> Not implemented, hardwired to 0.



### 23.1.3 STS - Device Status

B/D/F/Type: 0/3/0/PCI  
Address Offset: 6-7h  
Default Value: 0010h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15	RO	0b	<b>Detected Parity Error (DPE):</b> Not implemented, hardwired to 0.
14	RO	0b	<b>Signaled System Error (SSE):</b> Not implemented, hardwired to 0.
13	RO	0b	<b>Received Master-Abort (RMA):</b> Not implemented, hardwired to 0.
12	RO	0b	<b>Received Target Abort (RTA):</b> Not implemented, hardwired to 0.
11	RO	0b	<b>Signaled Target-Abort (STA):</b> Not implemented, hardwired to 0.
10:9	RO	00b	<b>DEVSEL# Timing (DEVT):</b> These bits are hardwired to 00.
8	RO	0b	<b>Master Data Parity Error Detected (DPD):</b> Not implemented, hardwired to 0.
7	RO	0b	<b>Fast Back-to-Back Capable (FBC):</b> Not implemented, hardwired to 0.
6	RO	0b	<b>Reserved</b>
5	RO	0b	<b>66-MHz Capable (C66):</b> Not implemented, hardwired to 0.
4	RO	1b	<b>Capabilities List (CL):</b> Indicates the presence of a capabilities list, hardwired to 1.
3	RO	0b	<b>Interrupt Status (IS):</b> Indicates the interrupt status of the device (1 = asserted).
2:0	RO	000b	<b>Reserved</b>



### 23.1.4 RID - Revision Identification

B/D/F/Type:	0/3/0/PCI
Address Offset:	8h
Default Value:	00h
Access:	RO
Size:	8 bits

RID Definition: This register contains the revision number of the (G)MCH Device 0. Following PCI Reset, the SRID value is selected to be read. When a write occurs to this register, the write data is compared to the hardwired RID Select Key Value, which is 69h. If the data matches this key, a flag is set that enables the CRID value to be read through this register.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Revision ID (RID):</b> Indicates stepping of the Intel® MEI host controller. 07h: B-3 stepping

### 23.1.5 CC - Class Code

B/D/F/Type:	0/3/0/PCI
Address Offset:	9-Bh
Default Value:	078000h
Access:	RO
Size:	24 bits

Bit	Access	Default Value	Description
23:16	RO	07h	<b>Base Class Code (BCC):</b> Indicates the base class code of the Intel® MEI host controller device.
15:8	RO	80h	<b>Sub Class Code (SCC):</b> Indicates the sub class code of the Intel MEI host controller device.
7:0	RO	00h	<b>Programming Interface (PI):</b> Indicates the programming interface of the Intel MEI host controller device.

### 23.1.6 CLS - Cache Line Size

B/D/F/Type:	0/3/0/PCI
Address Offset:	Ch
Default Value:	00h
Access:	RO
Size:	8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Cache Line Size (CLS):</b> Not implemented, hardwired to 0.



### 23.1.7 MLT - Master Latency Timer

B/D/F/Type: 0/3/0/PCI  
Address Offset: Dh  
Default Value: 00h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Master Latency Timer (MLT):</b> Not implemented, hardwired to 0.

### 23.1.8 HTYPE - Header Type

B/D/F/Type: 0/3/0/PCI  
Address Offset: Eh  
Default Value: 80h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7	RO	1b	<b>Multi-Function Device (MFD):</b> Indicates the Intel® MEI host controller is part of a multi-function device.
6:0	RO	0000000b	<b>Header Layout (HL):</b> Indicates that the Intel MEI host controller uses a target device layout.

### 23.1.9 HECI\_MBAR - Intel MEI MMIO Base Address

B/D/F/Type: 0/3/0/PCI  
Address Offset: 10-17h  
Default Value: 0000000000000004h  
Access: RO; R/W  
Size: 64 bits

Bit	Access	Default Value	Description
63:4	R/W	00000000 0000000h	<b>Base Address (BA):</b> Base address of register memory space.
3	RO	0b	<b>Prefetchable (PF):</b> Indicates that this range is not prefetchable
2:1	RO	10b	<b>Type (TP):</b> Indicates that this range can be mapped anywhere in 64-bit address space.
0	RO	0b	<b>Resource Type Indicator (RTE):</b> Indicates a request for register memory space.



### 23.1.10 SS - Sub System Identifiers

B/D/F/Type:	0/3/0/PCI
Address Offset:	2C-2Fh
Default Value:	00000000h
Access:	R/WO
Size:	32 bits

Bit	Access	Default Value	Description
31:16	R/WO	0000h	<b>Subsystem ID (SSID):</b> Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.
15:0	R/WO	0000h	<b>Subsystem Vendor ID (SSVID):</b> Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

### 23.1.11 CAP - Capabilities Pointer

B/D/F/Type:	0/3/0/PCI
Address Offset:	34h
Default Value:	50h
Access:	RO
Size:	8 bits

Bit	Access	Default Value	Description
7:0	RO	50h	<b>Capability Pointer (CP):</b> Indicates the first capability pointer offset. It points to the PCI power management capability offset.

### 23.1.12 INTR - Interrupt Information

B/D/F/Type:	0/3/0/PCI
Address Offset:	3C-3Dh
Default Value:	0100h
Access:	RO; R/W
Size:	16 bits

Bit	Access	Default Value	Description
15:8	RO	01h	<b>Interrupt Pin (IPIN):</b> This indicates the interrupt pin the Intel MEI host controller uses. The value of 01h selects INTA# interrupt pin. Note: As Intel MEI is an internal device in the (G)MCH, the INTA# pin is implemented as an INTA# message to the ICH.
7:0	R/W	00h	<b>Interrupt Line (ILINE):</b> Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.



### 23.1.13 HFS - Host Firmware Status

B/D/F/Type: 0/3/0/PCI  
Address Offset: 40-43h  
Default Value: 00000000h  
Access: RO  
Size: 32 bits

Bit	Access	Default Value	Description
31:0	RO	00000000h	<b>Firmware Status Host Access (FS_HA):</b> Indicates current status of the firmware for the Intel MEI controller. This field is the host's read only access to the FS field in the Intel Management Engine Firmware Status AUX register.

### 23.1.14 PID - PCI Power Management Capability ID

B/D/F/Type: 0/3/0/PCI  
Address Offset: 50-51h  
Default Value: 8C01h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	8Ch	<b>Next Capability (NEXT):</b> Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	RO	01h	<b>Cap ID (CID):</b> Indicates that this pointer is a PCI power management.



### 23.1.15 PC - PCI Power Management Capabilities

B/D/F/Type: 0/3/0/PCI  
 Address Offset: 52-53h  
 Default Value: C803h  
 Access: RO  
 Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	11001b	<b>PME_Support (PSUP):</b> Indicates the states that can generate PME#. Intel MEI can assert PME# from any D-state except D1 or D2 which are not supported by Intel MEI.
10	RO	0b	<b>D2_Support (D2S):</b> The D2 state is not supported for the Intel MEI host controller.
9	RO	0b	<b>D1_Support (D1S):</b> The D1 state is not supported for the Intel MEI host controller.
8:6	RO	000b	<b>Aux_Current (AUXC):</b> Reports the maximum Suspend well current required when in the D3COLD state.
5	RO	0b	<b>Device Specific Initialization (DSI):</b> Indicates whether device-specific initialization is required.
4	RO	0b	<b>Reserved</b>
3	RO	0b	<b>PME Clock (PMEC):</b> Indicates that PCI clock is not required to generate PME#.
2:0	RO	011b	<b>Version (VS):</b> Indicates support for Revision 1.2 of the <i>PCI Power Management Specification</i> .



### 23.1.16 PMCS - PCI Power Management Control and Status

B/D/F/Type: 0/3/0/PCI  
Address Offset: 54-55h  
Default Value: 0008h  
Access: R/WC; RO; R/W  
Size: 16 bits

Bit	Access	Default Value	Description
15	R/WC	0b	<b>PME Status (PMES):</b> The PME Status bit in Intel MEI space can be set to 1 by ARC FW performing a write into AUX register to set PMES. This bit is cleared by host CPU writing a 1 to it. ARC cannot clear this bit. Host CPU writes with value 0 have no effect on this bit. This bit is reset to 0 by MRST#
14:9	RO	000000b	<b>Reserved.</b>
8	R/W	0b	<b>PME Enable (PMEE):</b> This bit is read/write, under control of host S/W. It does not directly have an effect on PME events. However, this bit is shadowed into AUX space so ARC F/W can monitor it. The ARC F/W is responsible for ensuring that F/W does not cause the PME-S bit to transition to 1 while the PMEE bit is 0, indicating that host S/W had disabled PME. This bit is reset to 0 by MRST#
7:4	RO	0000b	<b>Reserved</b>
3	RO	1b	<b>Reserved</b>
2	RO	0b	<b>Reserved</b>
1:0	R/W	00b	<b>Power State (PS):</b> This field is used both to determine the current power state of the Intel MEI host controller and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state The D1 and D2 states are not supported for this Intel MEI host controller. When in the D3HOT state, the HBA's configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked. This field is visible to firmware through the H_PCI_CSR register, and changes to this field may be configured by the H_PCI_CSR register to generate an Intel Management Engine MSI.



### 23.1.17 MID - Message Signaled Interrupt Identifiers

B/D/F/Type: 0/3/0/PCI  
 Address Offset: 8C-8Dh  
 Default Value: 0005h  
 Access: RO  
 Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Next Pointer (NEXT):</b> Indicates the next item in the list. This can be other capability pointers (such as PCI-X or PCI Express) or it can be the last item in the list.
7:0	RO	05h	<b>Capability ID (CID):</b> Capabilities ID indicates MSI.

### 23.1.18 MC - Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/0/PCI  
 Address Offset: 8E-8Fh  
 Default Value: 0080h  
 Access: RO; R/W  
 Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Reserved</b>
7	RO	1b	<b>64-Bit Address Capable (C64):</b> Specifies whether capable of generating 64-bit messages.
6:4	RO	000b	<b>Multiple Message Enable (MME):</b> Not implemented, hardwired to 0.
3:1	RO	000b	<b>Multiple Message Capable (MMC):</b> Not implemented, hardwired to 0.
0	R/W	0b	<b>MSI Enable (MSIE):</b> If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.



### 23.1.19 MA - Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/0/PCI  
Address Offset: 90-93h  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

Bit	Access	Default Value	Description
31:2	R/W	00000000h	<b>Address (ADDR):</b> Lower 32 bits of the system specified message address, always DW aligned. MSI is not translated in Intel® VT-d, therefore, in order to avoid sending bad MSI with address bit [31:20] will be masked internally to generate 12'hFEE regardless of content in register. Register attribute remains as R/W.
1:0	RO	00b	<b>Reserved</b>

### 23.1.20 MD - Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/0/PCI  
Address Offset: 98-99h  
Default Value: 0000h  
Access: R/W  
Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/W	0000h	<b>Data (Data):</b> This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.



### 23.1.21 HIDM - Intel MEI Interrupt Delivery Mode

B/D/F/Type:	0/3/0/PCI
Address Offset:	A0h
Default Value:	00h
Access:	R/W
Size:	8 bits
BIOS Optimal Default	00h

This register is used to select interrupt delivery mechanism for Intel MEI to Host CPU interrupts.

Bit	Access	Default Value	Description
7:2	RO	0h	<b>Reserved</b>
1:0	R/W	00b	<b>Intel MEI Interrupt Delivery Mode (HIDM):</b> These bits control what type of interrupt the Intel MEI will send. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI



## 23.2 Intel MEI PCI Device 3 Function 1

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Identifiers	ID	0	3	2A458086h	RO
Command	CMD	4	5	0000h	RO; R/W
Device Status	STS	6	7	0010h	RO
Revision Identification	RID	8	8	00h	RO
Class Code	CC	9	B	078000h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HTYPE	E	E	80h	RO
Built-In Self Test	BIST	F	F	00h	RO
HECI MMIO Base Address	HECI_MBAR	10	17	0000000000000000 004h	RO; R/W
Sub System Identifiers	SS	2C	2F	00000000h	R/WO
Capabilities Pointer	CAP	34	34	50h	RO
Interrupt Information	INTR	3C	3D	0400h	RO; R/W
Reserved		3E	3F		
Host Firmware Status	HFS	40	43	00000000h	RO
PCI Power Management Capability ID	PID	50	51	8C01h	RO
PCI Power Management Capabilities	PC	52	53	C803h	RO
PCI Power Management Control and Status	PMCS	54	55	0008h	RO; R/W; R/ WC
Message Signaled Interrupt Identifiers	MID	8C	8D	0005h	RO
Message Signaled Interrupt Message Control	MC	8E	8F	0080h	RO; R/W
Message Signaled Interrupt Message Address	MA	90	93	00000000h	RO; R/W
Message Signaled Interrupt Message Data	MD	98	99	0000h	R/W
HECI Interrupt Delivery Mode	HIDM	A0	A0	00h	R/W



### 23.2.1 ID - Identifiers

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 0-3h  
 Default Value: 2A458086h  
 Access: RO  
 Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	2A45h	<b>Device ID (DID):</b> Indicates what device number assigned by Intel.
15:0	RO	8086h	<b>Vendor ID (VID):</b> 16-bit field which indicates Intel is the vendor, assigned by the PCI SIG.

### 23.2.2 CMD - Command

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 4-5h  
 Default Value: 0000h  
 Access: RO; R/W  
 Size: 16 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15:11	RO	00000b	<b>Reserved</b>
10	R/W	0b	<b>Interrupt Disable (ID):</b> Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9	RO	0b	<b>Fast Back-to-Back Enable (FBE):</b> Not implemented, hardwired to 0.
8	RO	0b	<b>SERR# Enable (SEE):</b> Not implemented, hardwired to 0.
7	RO	0b	<b>Wait Cycle Enable (WCC):</b> Not implemented, hardwired to 0.
6	RO	0b	<b>Parity Error Response Enable (PEE):</b> Not implemented, hardwired to 0.
5	RO	0b	<b>VGA Palette Snooping Enable (VGA):</b> Not implemented, hardwired to 0
4	RO	0b	<b>Memory Write and Invalidate Enable (MWIE):</b> Not implemented, hardwired to 0.
3	RO	0b	<b>Special Cycle Enable (SCE):</b> Not implemented, hardwired to 0.



(Sheet 2 of 2)

Bit	Access	Default Value	Description
2	R/W	0b	<b>Bus Master Enable (BME):</b> Controls the Intel MEI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, Intel MEI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an Intel Management Engine MSI. When this bit is 0, Intel MEI is blocked from generating MSI to the host CPU. <b>NOTE:</b> This bit does not block Intel MEI accesses to Intel Management Engine -UMA, i.e., writes or reads to the host and Intel Management Engine circular buffers through the read window and write window registers still cause Intel Management Engine backbone transactions to Intel Management Engine -UMA.
1	R/W	0b	<b>Memory Space Enable (MSE):</b> Controls access to the Intel MEI host controller's memory mapped register space.
0	RO	0b	<b>I/O Space Enable (IOSE):</b> Not implemented, hardwired to 0.

### 23.2.3 STS - Device Status

B/D/F/Type: 0/3/1/PCI  
Address Offset: 6-7h  
Default Value: 0010h  
Access: RO  
Size: 16 bits

(Sheet 1 of 2)

Bit	Access	Default Value	Description
15	RO	0b	<b>Detected Parity Error (DPE):</b> Not implemented, hardwired to 0.
14	RO	0b	<b>Signaled System Error (SSE):</b> Not implemented, hardwired to 0.
13	RO	0b	<b>Received Master-Abort (RMA):</b> Not implemented, hardwired to 0.
12	RO	0b	<b>Received Target Abort (RTA):</b> Not implemented, hardwired to 0.
11	RO	0b	<b>Signaled Target-Abort (STA):</b> Not implemented, hardwired to 0.
10:9	RO	00b	<b>DEVSEL# Timing (DEVT):</b> These bits are hardwired to 00.
8	RO	0b	<b>Master Data Parity Error Detected (DPD):</b> Not implemented, hardwired to 0.
7	RO	0b	<b>Fast Back-to-Back Capable (FBC):</b> Not implemented, hardwired to 0.
6	RO	0b	<b>Reserved</b>



(Sheet 2 of 2)

Bit	Access	Default Value	Description
5	RO	0b	<b>66-MHz Capable (C66):</b> Not implemented, hardwired to 0.
4	RO	1b	<b>Capabilities List (CL):</b> Indicates the presence of a capabilities list, hardwired to 1.
3	RO	0b	<b>Interrupt Status (IS):</b> Indicates the interrupt status of the device (1 = asserted).
2:0	RO	000b	<b>Reserved</b>

### 23.2.4 RID - Revision Identificatin

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 8h  
 Default Value: 00h  
 Access: RO  
 Size: 8 bits

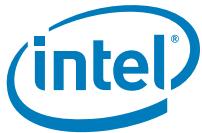
RID Definition: This register contains the revision number of the (G)MCH Device 0. Following PCI Reset, the SRID value is selected to be read. When a write occurs to this register, the write data is compared to the hardwired RID Select Key Value, which is 69h. If the data matches this key, a flag is set that enables the CRID value to be read through this register.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Revision ID (RID):</b> Indicates stepping of the Intel® MEI host controller.

### 23.2.5 CC - Class Code

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 9-Bh  
 Default Value: 078000h  
 Access: RO  
 Size: 24 bits

Bit	Access	Default Value	Description
23:16	RO	07h	<b>Base Class Code (BCC):</b> Indicates the base class code of the Intel MEI host controller device.
15:8	RO	80h	<b>Sub Class Code (SCC):</b> Indicates the sub class code of the Intel® MEI host controller device.
7:0	RO	00h	<b>Programming Interface (PI):</b> Indicates the programming interface of the Intel MEI host controller device.



### 23.2.6 CLS - Cache Line Size

B/D/F/Type: 0/3/1/PCI  
Address Offset: Ch  
Default Value: 00h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Cache Line Size (CLS):</b> Not implemented, hardwired to 0.

### 23.2.7 MLT - Master Latency Timer

B/D/F/Type: 0/3/1/PCI  
Address Offset: Dh  
Default Value: 00h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Master Latency Timer (MLT):</b> Not implemented, hardwired to 0.

### 23.2.8 HTYPE - Header Type

B/D/F/Type: 0/3/1/PCI  
Address Offset: Eh  
Default Value: 80h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7	RO	1b	<b>Multi-Function Device (MFD):</b> Indicates the Intel® MEI host controller is part of a multi-function device.
6:0	RO	0000000b	<b>Header Layout (HL):</b> Indicates that the Intel MEI host controller uses a target device layout.



### 23.2.9 BIST - Built-In Self Test

B/D/F/Type:	0/3/1/PCI
Address Offset:	Fh
Default Value:	00h
Access:	RO
Size:	8 bits

Bit	Access	Default Value	Description
7	RO	0b	<b>BIST Capable (BC):</b> Not implemented, hardwired to 0.
6:0	RO	0000000b	<b>Reserved</b>

### 23.2.10 HECL\_MBAR - Intel MEI MMIO Base Address

B/D/F/Type:	0/3/1/PCI
Address Offset:	10-17h
Default Value:	0000000000000004h
Access:	RO; R/W
Size:	64 bits

This register allocates space for the Intel MEI memory mapped registers.

Bit	Access	Default Value	Description
63:4	R/W	00000000 0000000h	<b>Base Address (BA):</b> Base address of register memory space.
3	RO	0b	<b>Prefetchable (PF):</b> Indicates that this range is not prefetchable
2:1	RO	10b	<b>Type (TP):</b> Indicates that this range can be mapped anywhere in 32-bit address space
0	RO	0b	<b>Resource Type Indicator (RTE):</b> Indicates a request for register memory space.



### 23.2.11 SS - Sub System Identifiers

B/D/F/Type: 0/3/1/PCI  
Address Offset: 2C-2Fh  
Default Value: 00000000h  
Access: R/WO  
Size: 32 bits

Bit	Access	Default Value	Description
31:16	R/WO	0000h	<b>Subsystem ID (SSID):</b> Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.
15:0	R/WO	0000h	<b>Subsystem Vendor ID (SSVID):</b> Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

### 23.2.12 CAP - Capabilities Pointer

B/D/F/Type: 0/3/1/PCI  
Address Offset: 34h  
Default Value: 50h  
Access: RO  
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RO	50h	<b>Capability Pointer (CP):</b> Indicates the first capability pointer offset. It points to the PCI power management capability offset.



### 23.2.13 INTR - Interrupt Information

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 3C-3Dh  
 Default Value: 0400h  
 Access: RO; R/W  
 Size: 16 bits

<b>Bit</b>	<b>Access</b>	<b>Default Value</b>	<b>Description</b>
15:8	RO	04h	<b>Interrupt Pin (IPIN):</b> This indicates the interrupt pin the Intel® MEI host controller uses. The value of 01h selects INTA# interrupt pin. <b>NOTE:</b> As Intel MEI is an internal device in the (G)MCH, the INTA# pin is implemented as an INTA# message to the ICH.
7:0	R/W	00h	<b>Interrupt Line (ILINE):</b> Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

### 23.2.14 HFS - Host Firmware Status

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 40-43h  
 Default Value: 00000000h  
 Access: RO  
 Size: 32 bits

<b>Bit</b>	<b>Access</b>	<b>Default Value</b>	<b>Description</b>
31:0	RO	00000000h	<b>Firmware Status Host Access (FS_HA):</b> Indicates current status of the firmware for the Intel® MEI controller. This field is the host's read only access to the FS field in the Intel Management Engine Firmware Status AUX register.



### 23.2.15 PID - PCI Power Management capability ID

B/D/F/Type: 0/3/1/PCI  
Address Offset: 50-51h  
Default Value: 8C01h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	8Ch	<b>Next Capability (NEXT):</b> Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	RO	01h	<b>Cap ID (CID):</b> Indicates that this pointer is a PCI power management.

### 23.2.16 PC - PCI Power Management Capabilities

B/D/F/Type: 0/3/1/PCI  
Address Offset: 52-53h  
Default Value: C803h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	11001b	<b>PME_Support (PSUP):</b> Indicates the states that can generate PME#. Intel® MEI can assert PME# from any D-state except D1 or D2 which are not supported by Intel MEI.
10	RO	0b	<b>D2_Support (D2S):</b> The D2 state is not supported for the Intel MEI host controller.
9	RO	0b	<b>D1_Support (D1S):</b> The D1 state is not supported for the Intel MEI host controller.
8:6	RO	000b	<b>Aux_Current (AUXC):</b> Reports the maximum Suspend well current required when in the D3COLD state.
5	RO	0b	<b>Device Specific Initialization (DSI):</b> Indicates whether device-specific initialization is required.
4	RO	0b	<b>Reserved</b>
3	RO	0b	<b>PME Clock (PMEC):</b> Indicates that PCI clock is not required to generate PME#.
2:0	RO	011b	<b>Version (VS):</b> Indicates support for Revision 1.2 of the <i>PCI Power Management Specification</i> .



### 23.2.17 PMCS - PCI Power Management Control an Status

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 54-55h  
 Default Value: 0008h  
 Access: RO; R/W; R/WC  
 Size: 16 bits

Bit	Access	Default Value	Description
15	R/WC	0b	<b>PME Status (PMES):</b> The PME Status bit in Intel MEI space can be set to 1 by ARC FW performing a write into AUX register to set PMES. This bit is cleared by host CPU writing a 1 to it. ARC cannot clear this bit. Host CPU writes with value 0 have no effect on this bit. This bit is reset to 0 by MRST#
14:9	RO	000000b	<b>Reserved</b>
8	R/W	0b	<b>PME Enable (PMEE):</b> This bit is read/write, under control of host SW. It does not directly have an effect on PME events. However, this bit is shadowed into AUX space so ARC FW can monitor it. The ARC FW is responsible for ensuring that FW does not cause the PME-S bit to transition to 1 while the PMEE bit is 0, indicating that host SW had disabled PME. This bit is reset to 0 by MRST#
7:4	RO	0000b	<b>Reserved</b>
3	RO	1b	<b>Reserved</b>
2	RO	0b	<b>Reserved</b>
1:0	R/W	00b	<b>Power State (PS):</b> This field is used both to determine the current power state of the Intel MEI host controller and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state The D1 and D2 states are not supported for this Intel MEI host controller. When in the D3HOT state, the HBA's configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked. This field is visible to firmware through the H_PCI_CSR register, and changes to this field may be configured by the H_PCI_CSR register to generate an Intel Management Engine MSI.



### 23.2.18 MID - Message Signaled Interrupt Identifiers

B/D/F/Type: 0/3/1/PCI  
Address Offset: 8C-8Dh  
Default Value: 0005h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Next Pointer (NEXT):</b> Indicates the next item in the list. This can be other capability pointers (such as PCI-X or PCI Express) or it can be the last item in the list.
7:0	RO	05h	<b>Capability ID (CID):</b> Capabilities ID indicates MSI.

### 23.2.19 MC - Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/1/PCI  
Address Offset: 8E-8Fh  
Default Value: 0080h  
Access: RO; R/W  
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Reserved</b>
7	RO	1b	<b>64-Bit Address Capable (C64):</b> Specifies whether capable of generating 64-bit messages.
6:4	RO	000b	<b>Multiple Message Enable (MME):</b> Not implemented, hardwired to 0.
3:1	RO	000b	<b>Multiple Message Capable (MMC):</b> Not implemented, hardwired to 0.
0	R/W	0b	<b>MSI Enable (MSIE):</b> If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.



### 23.2.20 MA - Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 90-93h  
 Default Value: 00000000h  
 Access: RO; R/W  
 Size: 32 bits

Bit	Access	Default Value	Description
31:2	R/W	00000000h	<b>Address (ADDR):</b> Lower 32 bits of the system specified message address, always DW aligned. MSI is not translated in Intel® VT-d, therefore, in order to avoid sending bad MSI with address bit [31:20] will be masked internally to generate 12'hFEE regardless of content in register. Register attribute remains as R/W.
1:0	RO	00b	<b>Reserved</b>

### 23.2.21 MD - Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/1/PCI  
 Address Offset: 98-99h  
 Default Value: 0000h  
 Access: R/W  
 Size: 16 bits

Bit	Access	Default Value	Description
15:0	R/W	0000h	<b>Data (Data):</b> This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.



### 23.2.22 HIDM - Intel MEI Interrupt Delivery Mode

B/D/F/Type: 0/3/1/PCI  
Address Offset: A0h  
Default Value: 00h  
Access: R/W  
Size: 8 bits  
BIOS Optimal Default 00h

This register is used to select interrupt delivery mechanism for Intel MEI to Host CPU interrupts.

Bit	Access	Default Value	Description
7:2	RO	0h	<b>Reserved</b>
1:0	R/W	00b	<b>Intel® MEI Interrupt Delivery Mode (HIDM):</b> These bits control what type of interrupt the Intel MEI will send when ARC writes to set the M_IG bit in AUX space. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI

## 23.3 Intel® Management Engine Interface PCI Device 3 Function 2 (AMT IDER)

(Sheet 1 of 2)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Identification	ID	0	3	2A468086h	RO
Command Register	CMD	4	5	0000h	RO; R/W
Device Status	STS	6	7	00B0h	RO
Revision Identification	RID	8	8	00h	RO
Class Codes	CC	9	B	010185h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT	D	D	00h	RO
Reserved		E	F		
Primary Command Block IO Bar	PCMDBA	10	13	00000001h	RO; R/W
Primary Control Block Base Address	PCTLBA	14	17	00000001h	RO; R/W
Secondary Command Block Base Address	SCMDBA	18	1B	00000001h	RO; R/W
Secondary Control Block base Address	SCTLBA	1C	1F	00000001h	RO; R/W
Legacy Bus Master Base Address	LBAR	20	23	00000001h	RO; R/W
Reserved		24	27		



(Sheet 2 of 2)

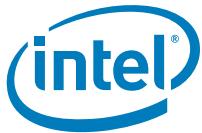
Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Sub System Identifiers	SS	2C	2F	00008086h	R/WO
Reserved		30	33		
Capabilities Pointer	CAP	34	34	C8h	RO
Interrupt Information	INTR	3C	3D	0300h	RO; R/W
Minimum Grant	MGNT	3E	3E	00h	RO
Maximum Latency	MLAT	3F	3F	00h	RO
PCI Power Management Capability ID	PID	C8	C9	D001h	RO
PCI Power Management Capabilities	PC	CA	CB	0023h	RO
PCI Power Management Control and Status	PMCS	CC	CF	00000000h	RO; R/W/V
Message Signaled Interrupt Capability ID	MID	D0	D1	0005h	RO
Message Signaled Interrupt Message Control	MC	D2	D3	0080h	RO; R/W
Message Signaled Interrupt Message Address	MA	D4	D7	00000000h	RO; R/W
Message Signaled Interrupt Message Upper Address	MAU	D8	DB	00000000h	RO; R/W
Message Signaled Interrupt Message Data	MD	DC	DD	0000h	R/W

### 23.3.1 ID - Identification

B/D/F/Type: 0/3/2/PCI  
 Address Offset: 0-3h  
 Default Value: 2A468086h  
 Access: RO  
 Size: 32 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
31:16	RO	2A46h	<b>Device ID (DID):</b> Indicates device number assigned by Intel.
15:0	RO	8086h	<b>Vendor ID (VID):</b> 16-bit field which indicates the company vendor as Intel



### 23.3.2 CMD - Command Register

B/D/F/Type: 0/3/2/PCI  
Address Offset: 4-5h  
Default Value: 0000h  
Access: RO; R/W  
Size: 16 bits

Reset: Host System reset or D3->D0 transition of function

This register provides basic control over the device's ability to respond to and perform Host system related accesses.

Bit	Access	Default Value	Description
15:11	RO	00h	<b>Reserved</b>
10	R/W	0b	<b>Interrupt Disable (ID):</b> This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt <b>and</b> MSI is not enabled.
9	RO	0b	<b>Fast Back-to-Back Enable (FBE):</b> Reserved
8	RO	0b	<b>SERR# Enable (SEE):</b> The PT function never generates an SERR# Reserved
7	RO	0b	<b>Wait Cycle Enable (WCC):</b> Reserved
6	RO	0b	<b>Parity Error Response Enable (PEE):</b> No Parity detection in PT functions. Reserved
5	RO	0b	<b>VGA Palette Snooping Enable (VGA):</b> Reserved
4	RO	0b	<b>Memory Write and Invalidate Enable (MWIE):</b> Reserved
3	RO	0b	<b>Special Cycle Enable (SCE):</b> Reserved
2	R/W	0b	<b>Bus Master Enable (BME):</b> Controls the PT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	RO	0b	<b>Memory Space Enable (MSE):</b> PT function does not contain target memory space.
0	R/W	0b	<b>I/O Space enable (IOSE):</b> Controls access to the PT function's target I/O space



### 23.3.3 STS - Device Status

B/D/F/Type:	0/3/2/PCI
Address Offset:	6-7h
Default Value:	00B0h
Access:	RO
Size:	16 bits

This register is used by the function to reflect its PCI status to the host for the functionality that it implements.

Bit	Access	Default Value	Description
15	RO	0b	<b>Detected Parity Error (DPE):</b> No parity error on its interface
14	RO	0b	<b>Signaled System Error (SSE):</b> The PT function will never generate an SERR#.
13	RO	0b	<b>Received Master-Abort Status (RMA):</b> Reserved
12	RO	0b	<b>Received Target-Abort Status (RTA):</b> Reserved
11	RO	0b	<b>Signaled Target-Abort Status (STA):</b> The PT Function will never generate a target abort. Reserved
10:9	RO	00b	<b>DEVSEL# Timing Status (DEVT):</b> Controls the device select time for the PT function's PCI interface
8	RO	0b	<b>Master Data Parity Error Detected (DPD):</b> PT function (IDER), as a master, does not detect a parity error. Other PT function is not a master and hence this bit is reserved also.
7	RO	1b	<b>Fast Back-to-Back Capable (RSVD):</b> Reserved
6	RO	0b	<b>Reserved</b>
5	RO	1b	<b>66-MHz Capable (RSVD):</b>
4	RO	1b	<b>Capabilities List (CL):</b> Indicates that there is a capabilities pointer implemented in the device.
3	RO	0b	<b>Interrupt Status (IS):</b> This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTC interrupt asserted to the Host.
2:0	RO	000b	<b>Reserved</b>



### 23.3.4 RID - Revision Identification

B/D/F/Type:	0/3/2/PCI
Address Offset:	8h
Default Value:	00h
Access:	RO
Size:	8 bits

RID Definition: This register contains the revision number of the (G)MCH Device 0. Following PCI Reset, the SRID value is selected to be read. When a write occurs to this register, the write data is compared to the hardwired RID Select Key Value, which is 69h. If the data matches this key, a flag is set that enables the CRID value to be read through this register.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Revision ID (RID)</b>

### 23.3.5 CC - Class Codes

B/D/F/Type:	0/3/2/PCI
Address Offset:	9-Bh
Default Value:	010185h
Access:	RO
Size:	24 bits

This register identifies the basic functionality of the device, i.e., IDE mass storage

Bit	Access	Default Value	Description
23:0	RO	010185h	<b>Programming Interface BCC SCC (PI BCC SCC)</b>

### 23.3.6 CLS - Cache Line Size

B/D/F/Type:	0/3/2/PCI
Address Offset:	Ch
Default Value:	00h
Access:	RO
Size:	8 bits

This register defines the system cache line size in dword increments. Mandatory for master which use the Memory-Write and Invalidate command.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Cache Line Size (CLS):</b> All writes to system memory are Memory Writes.



### 23.3.7 MLT - Master Latency Timer

B/D/F/Type:	0/3/2/PCI
Address Offset:	Dh
Default Value:	00h
Access:	RO
Size:	8 bits

This register defines the minimum number of PCI clocks the bus master can retain ownership of the bus whenever it initiates new transactions.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Master Latency Timer (MLT):</b> Not implemented since the function is in MCH

### 23.3.8 HTYPE - Header Type

B/D/F/Type:	0/3/2/PCI
Address Offset:	Eh
Default Value:	< Not Defined >
Access:	< Not Defined >
Size:	8 bits

Register is not implemented.

### 23.3.9 PCMDBA - Primary Command Block IO Bar

B/D/F/Type:	0/3/2/PCI
Address Offset:	10-13h
Default Value:	00000001h
Access:	RO; R/W
Size:	32 bits

Reset: Host system Reset or D3->D0 transition of the function

This 8-byte I/O space is used in Native Mode for the Primary Controller's Command Block, i.e., BAR 0.

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b>
15:3	R/W	0000h	<b>Base Address (BAR):</b> Base Address of the BAR0 I/O space (eight consecutive I/O locations).
2:1	RO	00b	<b>Reserved</b>
0	RO	1b	<b>Resource Type Indicator (RTE):</b> Indicates a request for I/O space.



### 23.3.10 PCTLBA - Primary Control Block Base Address

B/D/F/Type:	0/3/2/PCI
Address Offset:	14-17h
Default Value:	00000001h
Access:	RO; R/W
Size:	32 bits

Reset: Host system Reset or D3->D0 transition of the function

This 4-byte I/O space is used in Native Mode for the Primary Controller's Control Block, i.e., BAR 1.

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b>
15:2	R/W	0000h	<b>Base Address (BAR):</b> Base Address of the BAR1 I/O space (four consecutive I/O locations).
1	RO	0b	<b>Reserved</b>
0	RO	1b	<b>Resource Type Indicator (RTE):</b> Indicates a request for I/O space.

### 23.3.11 SCMDBA - Secondary Command Block Base Address

B/D/F/Type:	0/3/2/PCI
Address Offset:	18-1Bh
Default Value:	00000001h
Access:	RO; R/W
Size:	32 bits

Reset: Host System Reset or D3->D0 transition of the function

This 8-byte I/O space is used in Native Mode for the secondary Controller's Command Block. Secondary Channel is not implemented and reads return 7F7F7F7F and all writes are dropped.

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b>
15:3	R/W	0000h	<b>Base Address (BAR):</b> Base Address of the I/O space (eight consecutive I/O locations).
2:1	RO	00b	<b>Reserved</b>
0	RO	1b	<b>Resource Type Indicator (RTE):</b> Indicates a request for I/O space.



### 23.3.12 SCTLBA - Secondary Control Block Base Address

B/D/F/Type:	0/3/2/PCI
Address Offset:	1C-1Fh
Default Value:	00000001h
Access:	RO; R/W
Size:	32 bits

Reset: Host System Reset or D3->D0 transition.

This 4-byte I/O space is used in Native Mode for Secondary Controller's Control block. Secondary Channel is not implemented and reads return 7F7F7F7F and all writes are dropped.

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b>
15:2	R/W	0000h	<b>Base Address (BAR):</b> Base Address of the I/O space (four consecutive I/O locations).
1	RO	0b	<b>Reserved</b>
0	RO	1b	<b>Resource Type Indicator (RTE):</b> Indicates a request for I/O space.

### 23.3.13 LBAR - Legacy Bus Master Base Address

B/D/F/Type:	0/3/2/PCI
Address Offset:	20-23h
Default Value:	00000001h
Access:	RO; R/W
Size:	32 bits

Reset: Host system Reset or D3->D0 transition

This Bar is used to allocate I/O space for the SFF-8038i mode of operation (a.k.a. Bus Master IDE).

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b>
15:4	R/W	000h	<b>Base Address (BA):</b> Base Address of the I/O space (16 consecutive I/O locations).
3:1	RO	000b	<b>Reserved</b>
0	RO	1b	<b>Resource Type Indicator (RTE):</b> Indicates a request for I/O space.



### 23.3.14 SS - Sub System Identifiers

B/D/F/Type:	0/3/2/PCI
Address Offset:	2C-2Fh
Default Value:	00008086h
Access:	R/WO
Size:	32 bits

Reset: Host System Reset.

These registers are used to uniquely identify the add-in card or the subsystem that the device resides within.

Bit	Access	Default Value	Description
31:16	R/WO	0000h	<b>Subsystem ID (SSID):</b> This is written by BIOS. No hardware action taken on this value.
15:0	R/WO	8086h	<b>Subsystem Vendor ID (SSVID):</b> This is written by BIOS. No hardware action taken on this value.

### 23.3.15 CAP - Capabilities Pointer

B/D/F/Type:	0/3/2/PCI
Address Offset:	34h
Default Value:	C8h
Access:	RO
Size:	8 bits

This register is used to point to a linked list of new capabilities implemented by the device.

Bit	Access	Default Value	Description
7:0	RO	c8h	<b>capability Pointer (CP):</b> Indicates that the first capability pointer offset is offset c8h (the power management capability).



### 23.3.16 INTR - Interrupt Information

B/D/F/Type: 0/3/2/PCI  
 Address Offset: 3C-3Dh  
 Default Value: 0300h  
 Access: RO; R/W  
 Size: 16 bits

Reset: Host System Reset or D3->D0 reset of the function.

See definitions in the registers below.

Bit	Access	Default Value	Description						
15:8	RO	03h	<p><b>Interrupt Pin (IPIN):</b> a value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Function</th><th>Value</th><th>INTx</th></tr> </thead> <tbody> <tr> <td>(2 IDE)</td><td>03h</td><td>INTC</td></tr> </tbody> </table>	Function	Value	INTx	(2 IDE)	03h	INTC
Function	Value	INTx							
(2 IDE)	03h	INTC							
7:0	R/W	00h	<p><b>Interrupt Line (ILINE):</b> The value written in this register tells which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the OS and the device driver, and has no affect on the HW.</p>						

### 23.3.17 PID - PCI Power Management Capability ID

B/D/F/Type: 0/3/2/PCI  
 Address Offset: C8-C9h  
 Default Value: D001h  
 Access: RO  
 Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	D0h	<p><b>Next Capability (NEXT):</b> Its value of 0xD0 points to the MSI capability</p>
7:0	RO	01h	<p><b>Cap ID (CID):</b> Indicates that this pointer is a PCI power management</p>



### 23.3.18 PC - PCI Power Management Capabilities

B/D/F/Type: 0/3/2/PCI  
Address Offset: CA-CBh  
Default Value: 0023h  
Access: RO  
Size: 16 bits

This register implements the power management capabilities of the function.

Bit	Access	Default Value	Description
15:11	RO	00000b	<b>PME Support (PME):</b> Indicates no PME# in the PT function.
10	RO	0b	<b>D2 Support (D2S):</b> The D2 state is not supported.
9	RO	0b	<b>D1 Support (D1S):</b> The D1 state is not supported.
8:6	RO	000b	<b>Aux Current (AUXC):</b> PME# from D3 (cold) state is not supported, therefore this field is 000b.
5	RO	1b	<b>Device Specific Initialization (DSI):</b> Indicates that no device-specific initialization is required.
4	RO	0b	<b>Reserved</b>
3	RO	0b	<b>PME Clock (PMEC):</b> Indicates that PCI clock is not required to generate PME#.
2:0	RO	011b	<b>Version (VS):</b> Indicates support for revision 1.2 of the <i>PCI Power Management Specification</i> .



### 23.3.19 PMCS - PCI Power Management Control and Status

B/D/F/Type:	0/3/2/PCI
Address Offset:	CC-CFh
Default Value:	00000000h
Access:	RO; R/W/V
Size:	32 bits
BIOS Optimal Default	0000h

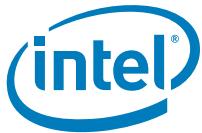
Reset: Host System Reset or D3->D0 transition.

This register implements the PCI PM Control and Status Register to allow PM state transitions and Wake up.

**Note:** The NSR bit of this register. All registers (PCI configuration and Device Specific) marked with D3->D0 transition reset will only do so if this bit reads a 0. If this bit is a 1, the D3->D0 transition will not reset the registers.

(Sheet 1 of 2)

Bit	Access	Default Value	Description
31:16	RO	0h	<b>Reserved (RSVD)</b>
15	RO	0b	<b>PME Status (PMES):</b> This bit is set when a PME event is to be requested. Not supported
14:9	RO	00h	<b>Reserved</b>
8	RO	0b	<b>PME Enable (PMEE):</b> Not Supported
7:4	RO	0000b	<b>Reserved</b>
3	RO/V	0b	<b>No Soft Reset (NSR):</b> When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full re-initialization sequence is needed to return the device to D0 Initialized. Value in this bit is reflects chicken bit in Intel Management Engine -AUX register x13900, bit [7] which is as follows: When 0: Device performs internal reset When 1: Device does not perform internal reset
2	RO	0b	<b>Reserved</b>



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Bit	Access	Default Value	Description
1:0	R/W	00b	<b>Power State (PS):</b> This field is used both to determine the current power state of the PT function and to set a new power state. The values are: 00 – D0 state 11 – D3 <sub>HOT</sub> state When in the D3 <sub>HOT</sub> state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

### 23.3.20 MID - Message Signaled Interrupt Capability ID

B/D/F/Type: 0/3/2/PCI  
Address Offset: D0-D1h  
Default Value: 0005h  
Access: RO  
Size: 16 bits

Message Signaled Interrupt is a feature that allows the device/function to generate an interrupt to the host by performing a dword memory write to a system specified address with system specified data. This register is used to identify and configure an MSI-capable device.

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Next Pointer (NEXT):</b> Value Indicates this is the last item in the capabilities list.
7:0	RO	05h	<b>Capability ID (CID):</b> Capabilities ID value indicates device is capable of generating an MSI.



### 23.3.21 MC - Message Signaled Interrupt Message Control

B/D/F/Type:	0/3/2/PCI
Address Offset:	D2-D3h
Default Value:	0080h
Access:	RO; R/W
Size:	16 bits

Reset: Host System Reset or D3->D0 transition.

This register provides System Software control over MSI.

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Reserved</b>
7	RO	1b	<b>64-Bit Address Capable (C64):</b> Capable of generating 64-bit and 32-bit messages.
6:4	R/W	000b	<b>Multiple Message Enable (MME):</b> These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	RO	000b	<b>Multiple Message Capable (MMC):</b> Only one message is required.
0	R/W	0b	<b>MSI Enable (MSIE):</b> If set MSI is enabled and traditional interrupt pins are not used to generate interrupts.

### 23.3.22 MA - Message Signaled Interrupt Message Address

B/D/F/Type:	0/3/2/PCI
Address Offset:	D4-D7h
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

Reset: Host system Reset or D3->D0 transition.

This register specifies the dword aligned address programmed by system software for sending MSI.

Bit	Access	Default Value	Description
31:2	R/W	00000000h	<b>Address (ADDR):</b> Lower 32 bits of the system specified message address, always DWORD-aligned.
1:0	RO	00b	<b>Reserved</b>



### 23.3.23 MAU - Message Signaled Interrupt Message Upper Address

B/D/F/Type: 0/3/2/PCI  
Address Offset: D8-DBh  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

Reset: Host system Reset or D3->D0 transition.

Upper 32 bits of the message address for the 64-bit address capable device.

Bit	Access	Default Value	Description
31:4	RO	0000000h	<b>Reserved</b>
3:0	R/W	0000b	<b>Address (ADDR):</b> Upper 4 bits of the system specified message address.

### 23.3.24 MD - Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/2/PCI  
Address Offset: DC-DDh  
Default Value: 0000h  
Access: R/W  
Size: 16 bits

Reset: Host system Reset or D3->D0 transition.

This 16-bit field is programmed by system software if MSI is enabled.

Bit	Access	Default Value	Description
15:0	R/W	0000h	<b>Data (DATA):</b> This content is driven onto the lower word of the data bus of the MSI memory write transaction



## 23.4 Device 3 Function 3 (AMT SOL Redirection)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Identification	ID	0	3	2A478086h	RO
Command Register	CMD	4	5	0000h	RO; R/W
Device Status	STS	6	7	00B0h	RO
Revision Identification	RID	8	8	00h	RO
Class Codes	CC	9	B	070002h	RO
Cache Line Size	CLS	C	C	00h	RO
Master Latency Timer	MLT	D	D	00h	RO
Header Type	HTYPE	E	E	< Not Defined >	< Not Defined >
Built In Self Test	BIST	F	F	< Not Defined >	< Not Defined >
KT IO Block Base Address	KTIBA	10	13	00000001h	RO; R/W
KT Mem Block Base Address	KTMBA	14	17	00000000h	RO; R/W
Reserved	RSVD	18	1B	00000000h	RO
Reserved	RSVD	1C	1F	00000000h	RO
Reserved	RSVD	20	23	00000000h	RO
Reserved	RSVD	24	28	0000000000h	< Not Defined >
Sub System Identifiers	SS	2C	2F	00008086h	R/WO
Reserved		30	33		
Capabilities Pointer	CAP	34	34	C8h	RO
Interrupt Information	INTR	3C	3D	0200h	RO; R/W
PCI Power Management Capability ID	PID	C8	C9	D001h	RO
PCI Power Management Capabilities	PC	CA	CB	0023h	RO
PCI Power Management Control and Status	PMCS	CC	CF	00000000h	RO/V; RO; R/W
Message Signaled Interrupt Capability ID	MID	D0	D1	0005h	RO
Message Signaled Interrupt Message Control	MC	D2	D3	0080h	RO; R/W
Message Signaled Interrupt Message Address	MA	D4	D7	00000000h	RO; R/W
Message Signaled Interrupt Message Upper Address	MAU	D8	DB	00000000h	RO; R/W
Message Signaled Interrupt Message Data	MD	DC	DD	0000h	R/W



### 23.4.1 ID - Identification

B/D/F/Type:	0/3/3/PCI
Address Offset:	0-3h
Default Value:	2A478086h
Access:	RO
Size:	32 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
31:16	RO	2A47h	<b>Device ID (DID):</b> Indicates device number assigned by Intel.
15:0	RO	8086h	<b>Vendor ID (VID):</b> 16-bit field which indicates the company vendor as Intel.

### 23.4.2 CMD - Command Register

B/D/F/Type:	0/3/3/PCI
Address Offset:	4-5h
Default Value:	0000h
Access:	RO; R/W
Size:	16 bits

Reset: Host System reset or D3->D0 transition.

This register provides basic control over the device's ability to respond to and perform Host system related accesses.

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Bit	Access	Default Value	Description
15:11	RO	00h	<b>Reserved</b>
10	R/W	0b	<b>Interrupt Disable (ID):</b> This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt <b>and</b> MSI is not enabled.
9	RO	0b	<b>Fast Back-to-Back Enable (FBE):</b> Reserved
8	RO	0b	<b>SERR# Enable (SEE):</b> The PT function never generates an SERR#. Reserved
7	RO	0b	<b>Wait Cycle Enable (WCC):</b> Reserved
6	RO	0b	<b>Parity Error Response Enable (PEE):</b> No Parity detection in PT functions. Reserved
5	RO	0b	<b>VGA Palette Snooping Enable (VGA):</b> Reserved
4	RO	0b	<b>Memory Write and Invalidate Enable (MWIE):</b> Reserved



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Bit	Access	Default Value	Description
3	RO	0b	<b>Special Cycle enable (SCE):</b> Reserved
2	R/W	0b	<b>Bus Master Enable (BME):</b> Controls the KT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands. For KT, the only bus mastering activity is MSI generation.
1	R/W	0b	<b>Memory Space Enable (MSE):</b> Controls Access to the PT function's target memory space.
0	R/W	0b	<b>I/O Space Enable (IOSE):</b> Controls access to the PT function's target I/O space

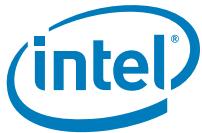
### 23.4.3 STS - Device Status

B/D/F/Type: 0/3/3/PCI  
 Address Offset: 6-7h  
 Default Value: 00B0h  
 Access: RO  
 Size: 16 bits

This register is used by the function to reflect its PCI status to the host for the functionality that it implements.

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Bit	Access	Default Value	Description
15	RO	0b	<b>Detected Parity Error (DPE):</b> No parity error on its interface
14	RO	0b	<b>Signaled System Error (SSE):</b> The PT function will never generate a SERR#.
13	RO	0b	<b>Received Master-Abort Status (RMA):</b> Reserved
12	RO	0b	<b>Received Target-Abort Status (RTA):</b> Reserved
11	RO	0b	<b>Signaled Target-Abort Status (STA):</b> The PT Function will never generate a target abort. Reserved
10:9	RO	00b	<b>DEVSEL# Timing Status (DEVT):</b> Controls the device select time for the PT function's PCI interface
8	RO	0b	<b>Master Data Parity Error Detected (DPD):</b> PT function (IDER), as a master, does not detect a parity error. Other PT function is not a master and hence this bit is reserved also.
7	RO	1b	<b>Fast Back-to-Back Capable (RSVD):</b> Reserved
6	RO	0b	<b>Reserved</b>
5	RO	1b	<b>66-MHz Capable (RSVD)</b>
4	RO	1b	<b>Capabilities List (CL):</b> Indicates that there is a capabilities pointer implemented in the device.



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Bit	Access	Default Value	Description
3	RO	0b	<b>Interrupt Status (IS):</b> This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTB interrupt asserted to the Host.
2:0	RO	000b	<b>Reserved</b>

#### 23.4.4 RID - Revision Identification

B/D/F/Type: 0/3/3/PCI  
Address Offset: 8h  
Default Value: 00h  
Access: RO  
Size: 8 bits

RID Definition: This register contains the revision number of the (G)MCH Device 0. Following PCI Reset, the SRID value is selected to be read. When a write occurs to this register, the write data is compared to the hardwired RID Select Key Value, which is 69h. If the data matches this key, a flag is set that enables the CRID value to be read through this register.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Revision ID (RID):</b> Indicates stepping of the silicon.

#### 23.4.5 CC - Class Codes

B/D/F/Type: 0/3/3/PCI  
Address Offset: 9-Bh  
Default Value: 070002h  
Access: RO  
Size: 24 bits

This register identifies the basic functionality of the device, i.e., Serial Com port.

Bit	Access	Default Value	Description
23:0	RO	070002h	<b>Programming Interface BCC SCC (PI BCC SCC)</b>



### 23.4.6 CLS - Cache Line Size

B/D/F/Type:	0/3/3/PCI
Address Offset:	Ch
Default Value:	00h
Access:	RO
Size:	8 bits

This register defines the system cache line size in dword increments. Mandatory for master which uses the Memory-Write and Invalidate command.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Cache Line Size (CLS):</b> All writes to system memory are Memory Writes.

### 23.4.7 MLT - Master Latency Timer

B/D/F/Type:	0/3/3/PCI
Address Offset:	Dh
Default Value:	00h
Access:	RO
Size:	8 bits

This register defines the minimum number of PCI clocks the bus master can retain ownership of the bus whenever it initiates new transactions.

Bit	Access	Default Value	Description
7:0	RO	00h	<b>Master Latency Timer (MLT):</b> Not implemented since the function is in MCH.

### 23.4.8 KTIBA - KT IO Block Base Address

B/D/F/Type:	0/3/3/PCI
Address Offset:	10-13h
Default Value:	00000001h
Access:	RO; R/W
Size:	32 bits

Reset: Host system Reset or D3->D0 transition.

Base Address for the 8-byte IO space for KT.

Bit	Access	Default Value	Description
31:16	RO	0000h	<b>Reserved</b>
15:3	R/W	0000h	<b>Base Address (BAR):</b> Base Address of the I/O space (eight consecutive I/O locations).
2:1	RO	00b	<b>Reserved</b>
0	RO	1b	<b>Resource Type Indicator (RTE):</b> Indicates a request for I/O space.



### 23.4.9 KTMBA - KT Mem Block Base Address

B/D/F/Type: 0/3/3/PCI  
Address Offset: 14-17h  
Default Value: 00000000h  
Access: RO; R/W  
Size: 32 bits

Reset: Host system Reset or D3->D0 transition.

Base Address of Memory Mapped space.

Bit	Access	Default Value	Description
31:12	R/W	00000h	<b>Base Address (BAR):</b> Memory Mapped IO BAR
11:4	RO	00h	<b>Reserved</b>
3	RO	0b	<b>Prefetchable (PF):</b> Indicates that this range is not prefetchable
2:1	RO	00b	<b>Type (TP):</b> Indicates that this range can be mapped anywhere in 32-bit address space
0	RO	0b	<b>Resource Type Indicator (RTE):</b> Indicates a request for register memory space

### 23.4.10 SS - Sub System Identifiers

B/D/F/Type: 0/3/3/PCI  
Address Offset: 2C-2Fh  
Default Value: 00008086h  
Access: R/WO  
Size: 32 bits

Reset: Host system Reset.

These registers are used to uniquely identify the add-in card or the subsystem that the device resides within.

Bit	Access	Default Value	Description
31:16	R/WO	0000h	<b>Subsystem ID (SSID):</b> This is written by BIOS. No hardware action taken on this value
15:0	R/WO	8086h	<b>Subsystem Vendor ID (SSVID):</b> This is written by BIOS. No hardware action taken on this value



### 23.4.11 CAP - Capabilities Pointer

B/D/F/Type:	0/3/3/PCI
Address Offset:	34h
Default Value:	C8h
Access:	RO
Size:	8 bits

This register is used to point to a linked list of new capabilities implemented by the device.

Bit	Access	Default Value	Description
7:0	RO	c8h	<b>Capability Pointer (CP):</b> Indicates that the first capability pointer offset is offset c8h (the power management capability).

### 23.4.12 INTR - Interrupt Information

B/D/F/Type:	0/3/3/PCI
Address Offset:	3C-3Dh
Default Value:	0200h
Access:	RO; R/W
Size:	16 bits

Reset: Host System Reset or D3->D0 reset of the function.

See individual registers below.

Bit	Access	Default Value	Description						
15:8	RO	02h	<p><b>Interrupt Pin (IPIN):</b> a value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively.</p> <table border="1" style="margin-left: 20px;"> <tr> <th>Function</th> <th>Value</th> <th>INTx</th> </tr> <tr> <td>(3 KT/Serial Port)</td> <td>02h</td> <td>INTB</td> </tr> </table>	Function	Value	INTx	(3 KT/Serial Port)	02h	INTB
Function	Value	INTx							
(3 KT/Serial Port)	02h	INTB							
7:0	R/W	00h	<b>Interrupt Line (ILINE):</b> The value written in this register tells which input of the system interrupt controller the device's interrupt pin is connected to. This value is used by the OS and the device driver, and has no affect on the H/W.						



### 23.4.13 PID - PCI Power Management Capability ID

B/D/F/Type: 0/3/3/PCI  
Address Offset: C8-C9h  
Default Value: D001h  
Access: RO  
Size: 16 bits

Bit	Access	Default Value	Description
15:8	RO	D0h	<b>Next Capability (NEXT):</b> Its value of 0xD0 points to the MSI capability.
7:0	RO	01h	<b>Cap ID (CID):</b> Indicates that this pointer is a PCI power management.

### 23.4.14 PC - PCI Power Management Capabilities

B/D/F/Type: 0/3/3/PCI  
Address Offset: CA-CBh  
Default Value: 0023h  
Access: RO  
Size: 16 bits

This register implements the power management capabilities of the function.

Bit	Access	Default Value	Description
15:11	RO	00000b	<b>PME Support (PME):</b> Indicates no PME# in the PT function.
10	RO	0b	<b>D2 Support (D2S):</b> The D2 state is not Supported.
9	RO	0b	<b>D1 Support (D1S):</b> The D1 state is not supported.
8:6	RO	000b	<b>Aux Current (AUXC):</b> PME# from D3 (cold) state is not supported, therefore this field is 000b.
5	RO	1b	<b>Device Specific Initialization (DSI):</b> Indicates that no device-specific initialization is required.
4	RO	0b	<b>Reserved</b>
3	RO	0b	<b>PME Clock (PMEC):</b> Indicates that PCI clock is not required to generate PME#.
2:0	RO	011b	<b>Version (VS):</b> Indicates support for revision 1.2 of the <i>PCI Power Management Specification</i> .



### 23.4.15 PMCS - PCI Power Management Control and Status

B/D/F/Type:	0/3/3/PCI
Address Offset:	CC-CFH
Default Value:	00000000h
Access:	RO/V; RO; R/W
Size:	32 bits
BIOS Optimal Default	0000h

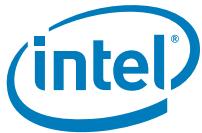
Reset: Host System Reset or D3->D0 transition.

This register implements the PCI PM Control and Status Register to allow PM state transitions and Wake up.

**Note:**

The NSR bit of this register. All registers (PCI configuration and device specific) marked with D3->D0 transition reset will only do so if this bit reads a 0. If this bit is a 1, the D3->D0 transition will not reset the registers.

Bit	Access	Default Value	Description
31:16	RO	0h	<b>Reserved (RSVD)</b>
15	RO	0b	<b>PME Status (PMES):</b> This bit is set when a PME event is to be requested. Not supported.
14:9	RO	00h	<b>Reserved</b>
8	RO	0b	<b>PME Enable (PMEE):</b> Not supported.
7:4	RO	0h	<b>Reserved</b>
3	RO/V	0b	<b>No Soft Reset (NSR):</b> When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full re-initialization sequence is needed to return the device to D0 Initialized. Value in this bit is reflects chicken bit in Intel Management Engine -AUX register x13900, bit [6] which is as follows: When 0: Device performs internal reset When 1: Device does not perform internal reset.
2	RO	0b	<b>Reserved</b>
1:0	R/W	00b	<b>Power State (PS):</b> This field is used both to determine the current power state of the PT function and to set a new power state. The values are: 00 – D0 state 11 – D3 <sub>HOT</sub> state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a '10' or '01' to these bits, the write will be ignored.



### 23.4.16 MID - Message Signaled Interrupt Capability ID

B/D/F/Type:	0/3/3/PCI
Address Offset:	D0-D1h
Default Value:	0005h
Access:	RO
Size:	16 bits

Message Signaled Interrupt is a feature that allows the device/function to generate an interrupt to the host by performing a dword memory write to a system specified address with system specified data. This register is used to identify and configure an MSI capable device.

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Next Pointer (NEXT):</b> Value indicates this is the last item in the list.
7:0	RO	05h	<b>capability ID (CID):</b> Value of Capabilities ID indicates device is capable of generating MSI.

### 23.4.17 MC - Message Signaled Interrupt Message Control

B/D/F/Type:	0/3/3/PCI
Address Offset:	D2-D3h
Default Value:	0080h
Access:	RO; R/W
Size:	16 bits

Reset: Host System Reset or D3->D0 transition

This register provides System Software control over MSI.

Bit	Access	Default Value	Description
15:8	RO	00h	<b>Reserved</b>
7	RO	1b	<b>64-Bit Address Capable (C64):</b> Capable of generating 64-bit and 32-bit messages.
6:4	R/W	000b	<b>Multiple Message Enable (MME):</b> These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	RO	000b	<b>Multiple Message Capable (MMC):</b> Only one message is required.
0	R/W	0b	<b>MSI Enable (MSIE):</b> If set MSI is enabled and traditional interrupt pins are not used to generate interrupts.



### 23.4.18 MA - Message Signaled Interrupt Message Address

B/D/F/Type:	0/3/3/PCI
Address Offset:	D4-D7h
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

Reset: Host system Reset or D3->D0 transition.

This register specifies the dword aligned address programmed by system software for sending MSI.

Bit	Access	Default Value	Description
31:2	R/W	00000000h	<b>Address (ADDR):</b> Lower 32 bits of the system specified message address, always dword-aligned.
1:0	RO	00b	<b>Reserved</b>

### 23.4.19 MAU - Message Signaled Interrupt Message Upper Address

B/D/F/Type:	0/3/3/PCI
Address Offset:	D8-DBh
Default Value:	00000000h
Access:	RO; R/W
Size:	32 bits

Reset: Host system Reset or D3->D0 transition.

Upper 32 bits of the message address for the 64-bit address capable device.

Bit	Access	Default Value	Description
31:4	RO	0000000h	<b>Reserved</b>
3:0	R/W	0000b	<b>Address (ADDR):</b> Upper 4 bits of the system specified message address



### 23.4.20 MD - Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/3/PCI  
Address Offset: DC-DDh  
Default Value: 0000h  
Access: R/W  
Size: 16 bits

Reset: Host system Reset or D3->D0 transition.

This 16-bit field is programmed by system software if MSI is enabled.

Bit	Access	Default Value	Description
15:0	R/W	0000h	<b>Data (DATA):</b> This MSI data is driven onto the lower word of the data bus of the MSI memory write transaction.

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