# Homa (TM15") Block Diagram

Project code: 91.4Z401.001
PCB P/N : 48.4Z401.011
REVISION : 07245-1

CLK GEN.
ICS 9LPRS365
3

Mobile CPU
Penryn
4, 5

EMC2102
25

HOST BUS 667/800/1066MHz@1.05V

DDR2
667/800 MHz
12,13

667/800MHz

DDR2
667/800 MHz
12,13

667/800MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11

CRT 19
LCD 16
HDMI 56

PCIex16

VGA Borad 34

X4 DMI 400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
20,21,22,23

Line In
41

MIC In
41

41
Line Out
(No-SPDIF)

41
INT.SPKR

RealTek
ALC268
39

AZALIA

OP AMP
G1412
40

OP AMP
G1454
40

RJ11

MODEM
MDC Card
28

PCI

Cardbus
OZ711MZ
36

MS/MS Pro/xD
/MMC/SD
5 in 1
31

PCMCIA
SLOT 37

LAN
Giga LAN
BCM5764M 32

TXFM
33

RJ45
33

New card
35

PWR SW
TPS2231 35

PCIex1

Mini Card
Kedron a/b/g/n 38

C Link1

Mini Card
Kedron a/b/g/n 38

LPC BUS

SATA

USB

HDD SATA
26

ODD SATA
25

Mini USB
Blue Tooth 27

Finger
Printer 57

Camera

USB
4 Port 29

KBC
Winbond
WPC775
42

Touch
Pad 42

INT.
KB 42

BIOS
Winbond
W25X80
43

Launch
Buttom
14

LPC
DEBUG
CONN 43

CRT
DVI
RJ45
USBX4
HP OUT
MIC IN
LINE IN

Port Replicator

PCB STACKUP

| | |
|---|---|
| TOP | |
| VCC | |
| S | |
| S | |
| GND | |
| BOTTOM | |

**SYSTEM DC/DC**
TPS51125 49

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 5V_S5(7A)<br>3D3V_S5(7A) |

**SYSTEM DC/DC**
TPS51124 51

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 1D05V_S0(16A)<br>1D8V_S3(16A) |

**TPS51100** 50

| | |
|---|---|
| 5V_S5 | DDR_VREF_S3 (1.5A)<br>DDR_VREF_S3_1 |

**G9131**

| | |
|---|---|
| 3D3V_S0 | 2D5V_S0 (300mA) |

**APL5912** 50

| | |
|---|---|
| 1D8V_S3 | 1D5V_S0 (2.5A) |

**CHARGER**
BQ24750 53

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | CHG_PWR 18V 6.0A<br>UP+5V 5V 100mA |

**CPU DC/DC**
ISL6266A 48

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | VCC_CORE_S0 0~1.3V 38A |

**GFX DC/DC**
ISL6263 48

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | VCC_CORE_S0 0~1.3V 5.5A |

970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

| Size | Document Number | Rev |
|---|---|---|
| A3 | Homa | -1 |

Date: Thursday, April 03, 2008 Sheet 1 of 57

# ICH9M Functional Strap Definitions



| Signal | Usage/When Sampled | Comment |
|---|---|---|
| HDA_SDOUT | XOR Chain Entrance/ PCIE Port Config 1bit1, Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down |
| HDA_SYNC | PCIE config 1 bit 0, Rising Edge of PWROK. | This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h) |
| GNT2#/ GPIO53 | PCIE config2 bit2, Rising Edge of PWROK. | This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h) |
| GPIO20 | Reserved, Rising Edge of PWROK. | This signal has a weak internal pull-down. This signal should not be pulled high. |
| GNT1#/ GPIO51 | ESI Strap (Server Only) Rising Edge of PWROK | Tying this strap low configures DMI for ESI-compatible operation. This signal has a weak internal pull up. ESI compatible mode is for server platforms only.This signal should not be pulled low for desttop and mobile. |
| GNT3#/ GPIO55 | Top-Block Swap Override. Rising Edge of PWROK. | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#: SPI_CS1#/ GPIO58 | Boot BIOS Destination Selection 0:1. Rising Edge of PWROK. | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC. |
| SPI_MOSI | Integrated TPM Enable, Rising Edge of CLPWROK | Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable. |
| GPIO49 | DMI Termination Voltage, Rising Edge of PWROK. | The signal is required to be low for desktop applications and required to be high for mobile applications. |
| SATALED# | PCI Express Lane Reversal. Rising Edge of PWROK. | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8) |
| SPKR | No Reboot. Rising Edge of PWROK. | If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. |
| TP3 | XOR Chain Entrance. Rising Edge of PWROK. | This signal should not be pull low unless using XOR Chain testing. It has a weak internal pull up. |
| GPIO33/ HDA_DOCK _EN# | Flash Descriptor Security Override Strap Rising Edge of PWROK | Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister. |

# ICH9M Integrated Pull-up and Pull-down Resistors



| SIGNAL | Resistor Type/Value |
|---|---|
| CL_CLK[1:0] | PULL-UP 20K |
| CL_DATA[1:0] | PULL-UP 20K |
| CL_RST0# | PULL-UP 10K |
| DPRSLPVR/GPIO16 | PULL-DOWN 20K |
| ENERGY_DETECT | PULL-UP 20K |
| HDA_BIT_CLK | PULL-DOWN 20K |
| HDA_DOCK_EN#/GPIO33 | PULL-UP 20K |
| HDA_RST# | PULL-DOWN 20K |
| HDA_SDIN[3:0] | PULL-DOWN 20K |
| HDA_SDOUT | PULL-DOWN 20K |
| HDA_SYNC | PULL-DOWN 20K |
| GLAN_DOCK# | The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller |
| GNT[3:0]#/GPIO[55,53,51] | PULL-UP 20K |
| GPIO[20] | PULL-DOWN 20K |
| GPIO[49] | PULL-UP 20K |
| LAD[3:0]#/FHW[3:0]# | PULL-UP 20K |
| LAN_RXD[2:0] | PULL-UP 20K |
| LDRQ[0] | PULL-UP 20K |
| LDRQ[1]/GPIO23 | PULL-UP 20K |
| PME# | PULL-UP 20K |
| PWRBTN# | PULL-UP 20K |
| SATALED# | PULL-UP 15K |
| SPI_CS1#/GPIO58/CLGPIO6 | PULL-UP 20K |
| SPI_MOSI | PULL-DOWN 20K |
| SPI_MISO | PULL-UP 20K |
| SPKR | PULL-DOWN 20K |
| TACH_[3:0] | PULL-UP 20K |
| TP[3] | PULL-UP 20K |
| USB[11:0][P,N] | PULL-DOWN 15K |

# Cantiga chipset and ICH9M I/O controller Hub strapping configuration



| Pin Name | Strap Description | Configuration |
|---|---|---|
| CFG[2:0] | FSB Frequency Select | 000 = FSB1066<br>011 = FSB667<br>010 = FSB800<br>others = Reserved |
| CFG[4:3]<br>CFG8<br>CFG[15:14]<br>CFG[18:17] | Reserved | |
| CFG5 | DMI x2 Select | 0 = DMI x2<br>**1 = DMI x4** (Default) |
| CFG6 | iTPM Host Interface | 0= The iTPM Host Interface is enabled(Note2)<br>**1=The iTPM Host Interface is disalbed(default)** |
| CFG7 | Intel Management engine Crypto strap | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality<br>**1 = TLS cipher suite with confidentiality (default)** |
| CFG9 | PCIE Graphics Lane | 0 = Reverse Lanes,15->0,14->1 ect..<br>**1= Normal operation(Default):Lane Numbered in order** |
| CFG10 | PCIE Loopback enable | 0 = Enable (Note 3)<br>**1= Disabled (default)** |
| CFG12 | ALLZ | 0 = ALLZ mode enabled (Note 3)<br>**1 = Disabled (default)** |
| CFG13 | XOR | 0 = XOR mode enabled (Note 3)<br>**1 = Disabled (default)** |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled<br>**1 = Dynamic ODT Enabled (Default)** |
| CFG19 | DMI Lane Reversal | **0 = Normal operation(Default): Lane Numbered in Order**<br>1 = Reverse Lanes<br>DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3)<br>DMI x2 mode[MCH -> ICH]:(3->0,2->1) |
| CFG20 | Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe | **0 = Only Digital Display Port or PCIE is operational (Default)**<br>1 =Digital display Port and PCIe are operting simulataneously via the PEG port |
| SDVO_CTRLDATA | SDVO Present | **0 =No SDVO Card Present (Default)**<br>1 = SDVO Card Present |
| L_DDC_DATA | Local Flat Panel (LFP) Present | **0 = LFP Disabled (Default)**<br>1= LFP Card Present; PCIE disabled |

**NOTE:**
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

3. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

# PCI Routing

page 31

| | IDSEL | INT | REQ | GNT |
|---|---|---|---|---|
| RTS5158 | AD25 | G:CARDBUS | 0 | 0 |

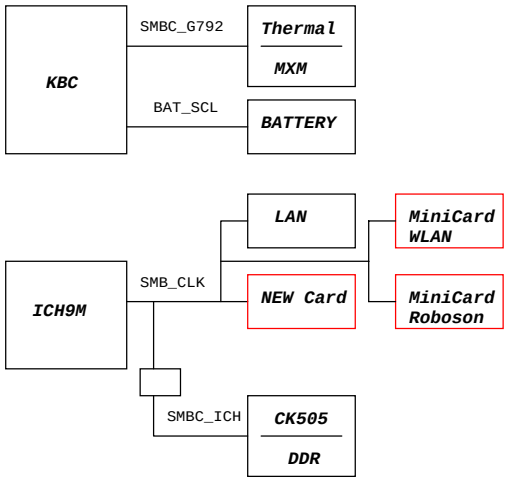
# PCIE Routing

| | |
|---|---|
| LANE1 | LAN BCM5764MKMLG |
| LANE2 | MiniCard WLAN |
| LANE3 | MiniCard Roboson |
| LANE4 | NewCard |

# USB Table

| USB | |
|---|---|
| Pair | Device |
| 0 | USB1 |
| 1 | USB4 |
| 2 | USB2 |
| 3 | DOCK USB |
| 4 | USB3 |
| 5 | Bluetooth |
| 6 | FP |
| 7 | MINIC1 |
| 8 | WEBCAM |
| 9 | NEW1 |
| 10 | MINIC2 |
| 11 | NC |

# SMBus





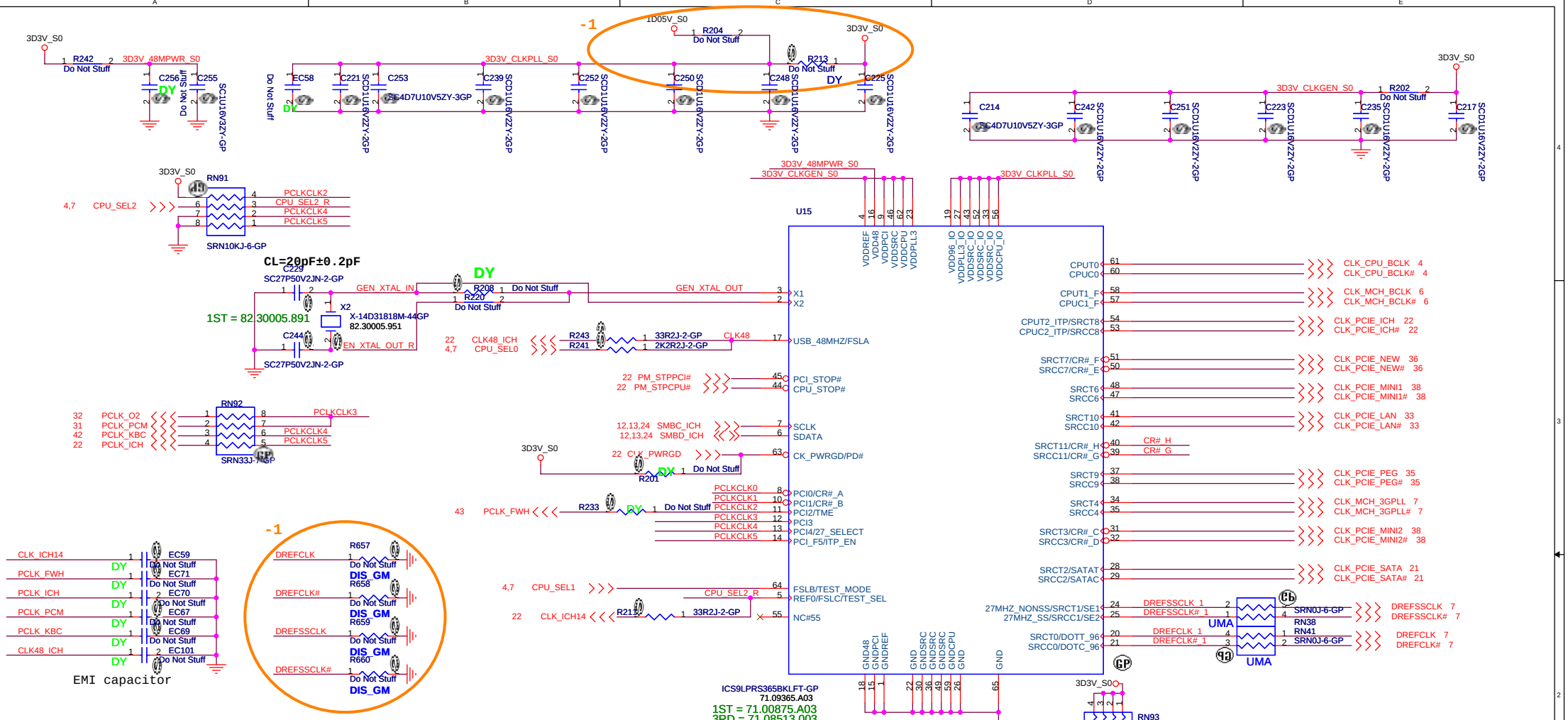

970

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reference**

Size: A3 | Document Number: **Homa** | Rev: **-1**

Date: Thursday, April 03, 2008 | Sheet 2 of 57




## ICS9LPRS365YGLFT setting table

| PIN NAME | DESCRIPTION |
|---|---|
| PCI0/CR#_A | Byte 5, bit 7<br>0 = PCI0 enabled (default)<br>1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair<br>Byte 5, bit 6<br>0 = CR#_A controls SRC0 pair (default),<br>1= CR#_A controls SRC2 pair |
| PCI1/CR#_B | Byte 5, bit 5<br>0 = PCI1 enabled (default)<br>1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair<br>Byte 5, bit 4<br>0 = CR#_B controls SRC1 pair (default)<br>1= CR#_B controls SRC4 pair |
| PCI2/TME | 0 = Overclocking of CPU and SRC Allowed<br>1 = Overclocking of CPU and SRC NOT allowed |
| PCI3 | |
| PCI4/27M_SEL | 0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96#<br>1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0# |
| PCI_F5/ITP_EN | 0 =SRC8/SRC8#<br>1 = ITP/ITP# |
| SRCT3/CR#_C | Byte 5, bit 3<br>0 = SRC3 enabled (default)<br>1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair<br>Byte 5, bit 2<br>0 = CR#_C controls SRC0 pair (default),<br>1= CR#_C controls SRC2 pair |

| PIN NAME | DESCRIPTION |
|---|---|
| SRCC3/CR#_D | Byte 5, bit 1<br>0 = SRC3 enabled (default)<br>1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair<br>Byte 5, bit 0<br>0 = CR#_D controls SRC1 pair (default)<br>1= CR#_D controls SRC4 pair |
| SRCC7/CR#_E | Byte 6, bit 7<br>0 = SRC7# enabled (default)<br>1= CR#_F controls SRC6 |
| SRCT7/CR#_F | Byte 6, bit 6<br>0 = SRC7 enabled (default)<br>1= CR#_F controls SRC8 |
| SRCC11/CR#_G | Byte 6, bit 5<br>0 = SRC11# enabled (default)<br>1= CR#_G controls SRC9 |
| SRCT11/CR#_H | Byte 6, bit 4<br>0 = SRC11 enabled (default)<br>1= CR#_H controls SRC10 |

| SEL2 FSC | SEL1 FSB | SEL0 FSA | CPU | FSB |
|---|---|---|---|---|
| 1 | 0 | 1 | 100M | X |
| 0 | 0 | 1 | 133M | 533M |
| 0 | 1 | 1 | 166M | 667M |
| 0 | 1 | 0 | 200M | 800M |
| 0 | 0 | 0 | 266M | 1067M |

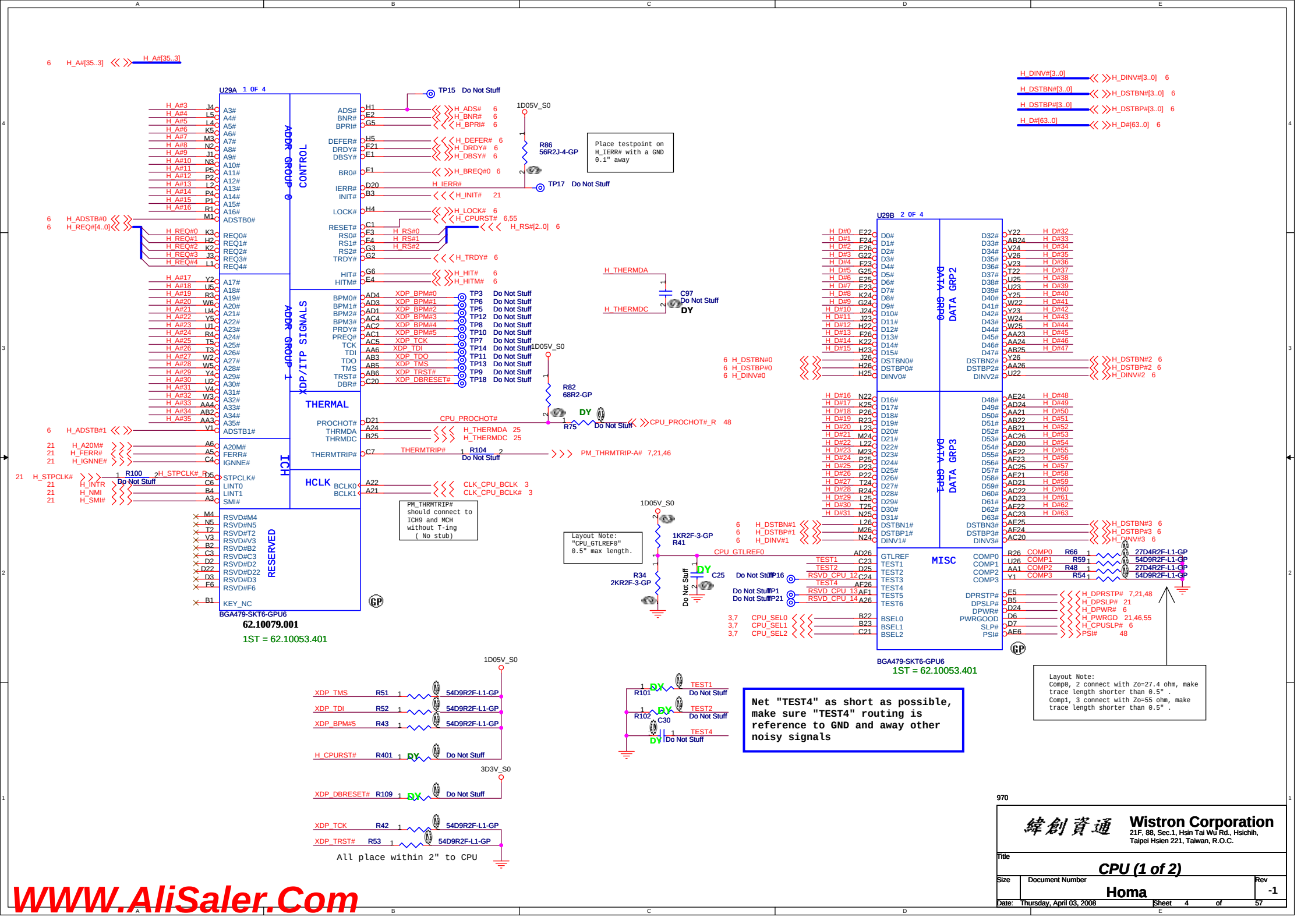
970

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Clock Generator*

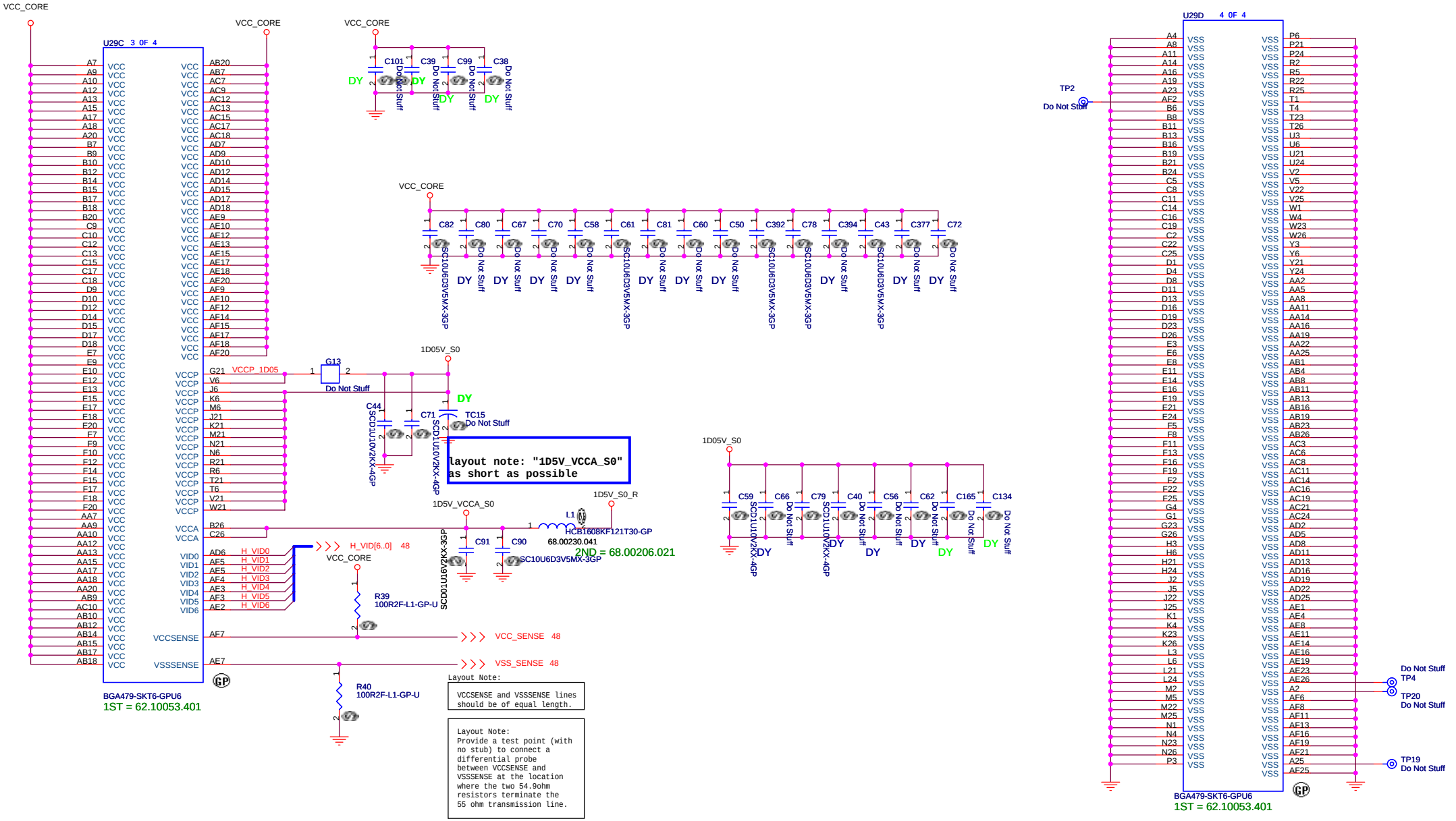
| Size | Document Number | Rev |
|---|---|---|
| | Homa | -1 |

Date: Thursday, April 03, 2008 Sheet 3 of 57




970

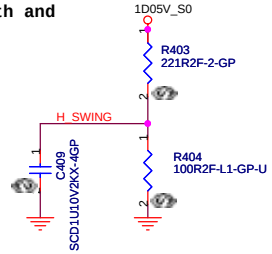
| | |
|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | **CPU (1 of 2)** |
| Size | Document Number: **Homa** Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 4 of 57 |



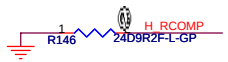

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***CPU (2 of 2)*** | |
| Size | Document Number: **Homa** | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 5 of 57 | |

**H_SWING routing Trace width and Spacing use 10 / 20 mil**

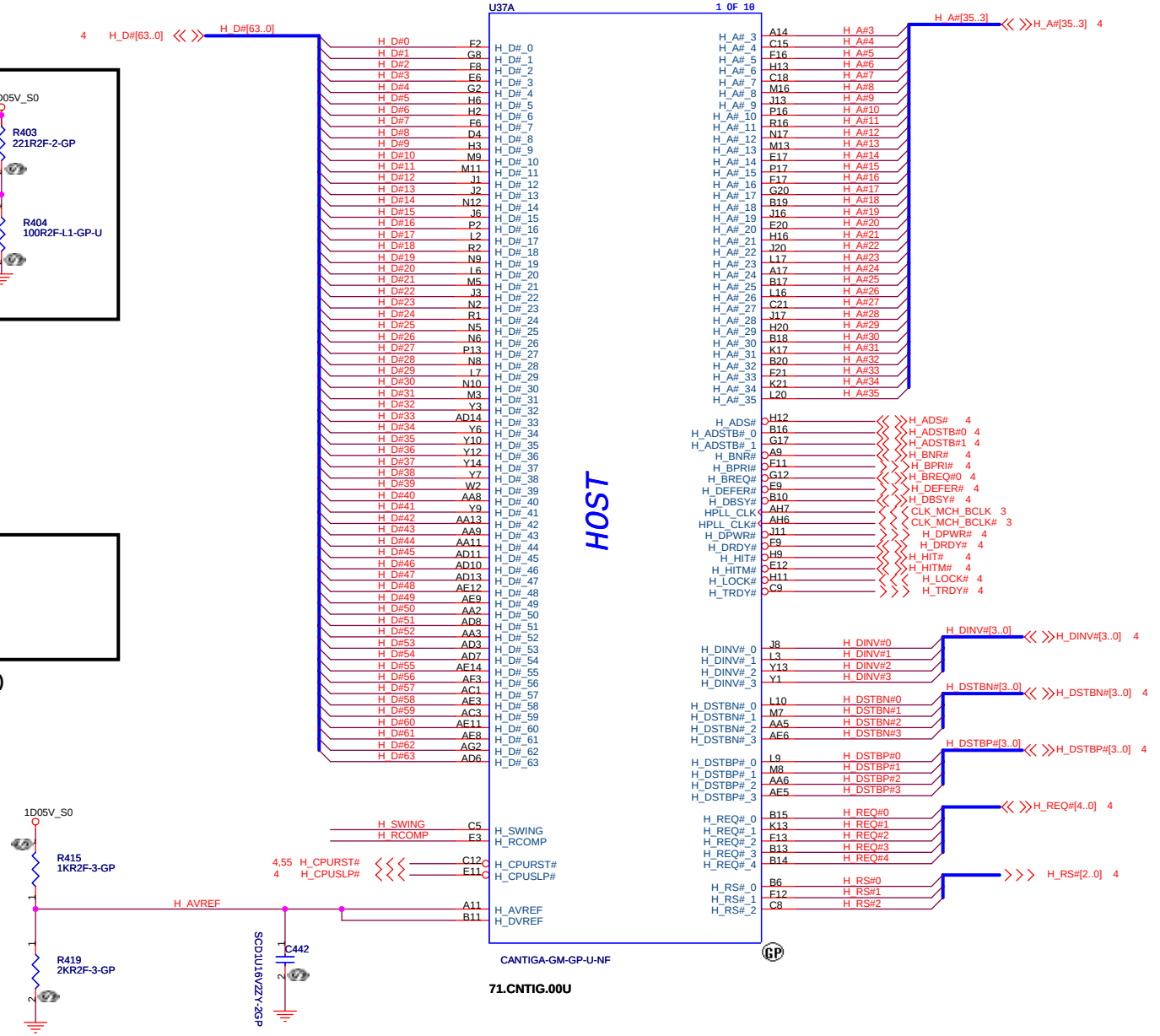
**H_SWING Resistors and Capacitors close MCH 500 mil ( MAX )**




**H_RCOMP routing Trace width and Spacing use 10 / 20 mil**




**Place them near to the chip ( < 0.5")**

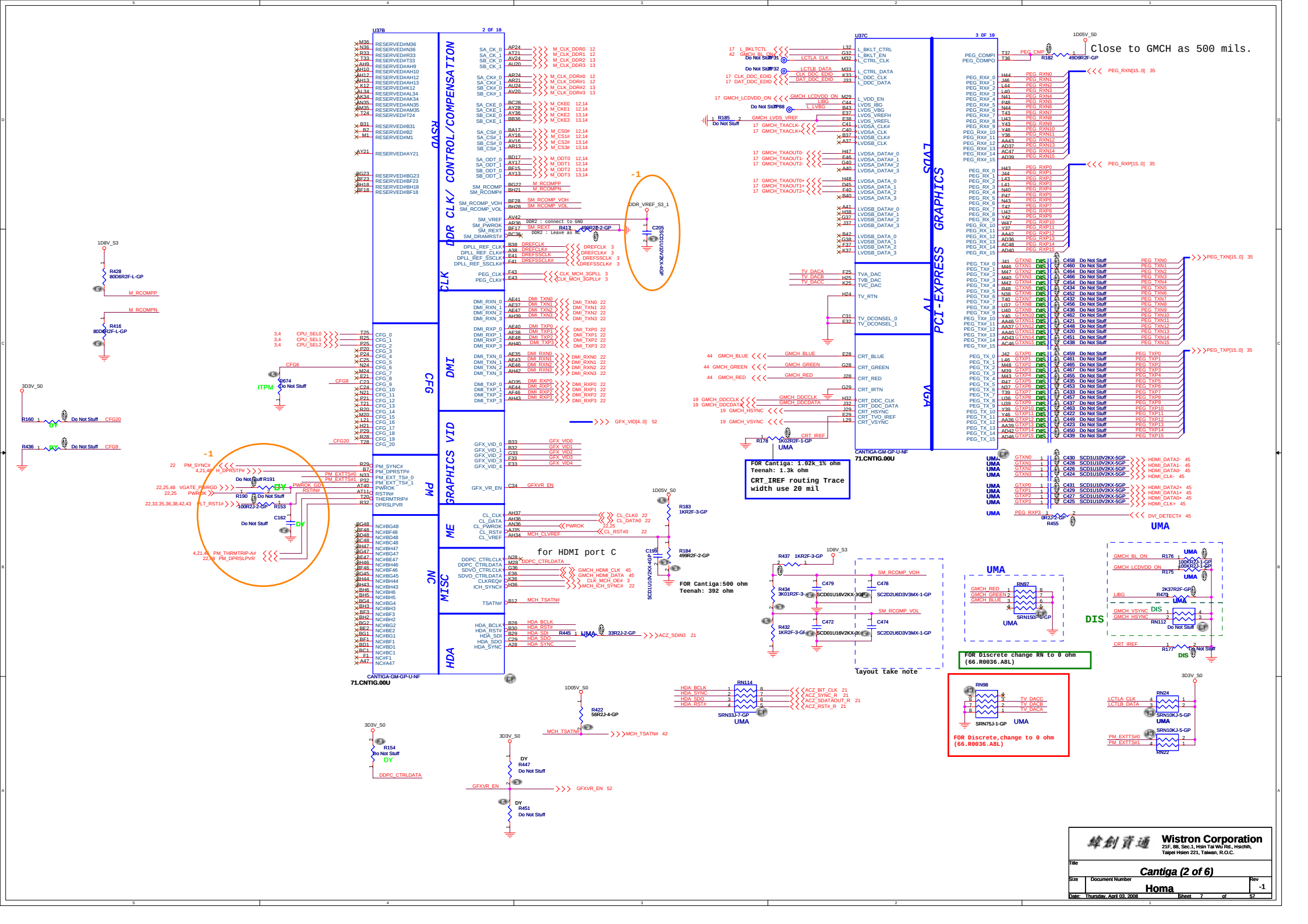


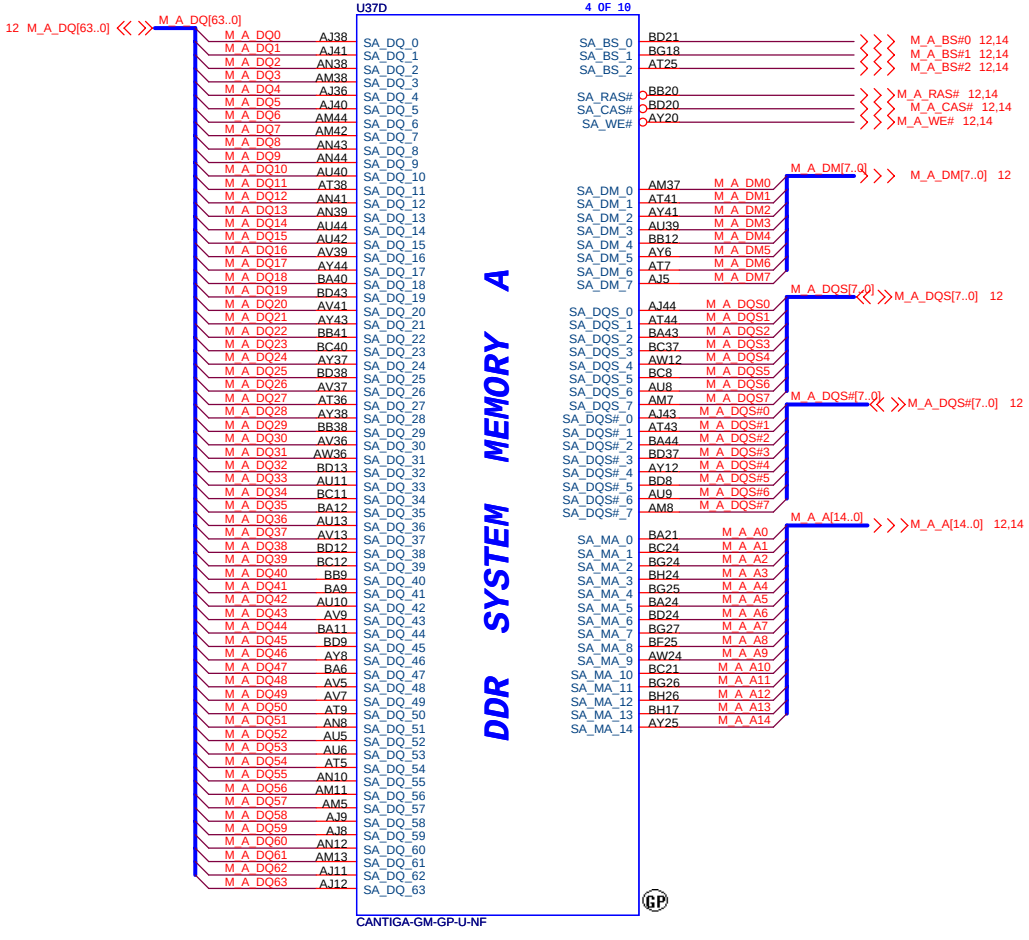


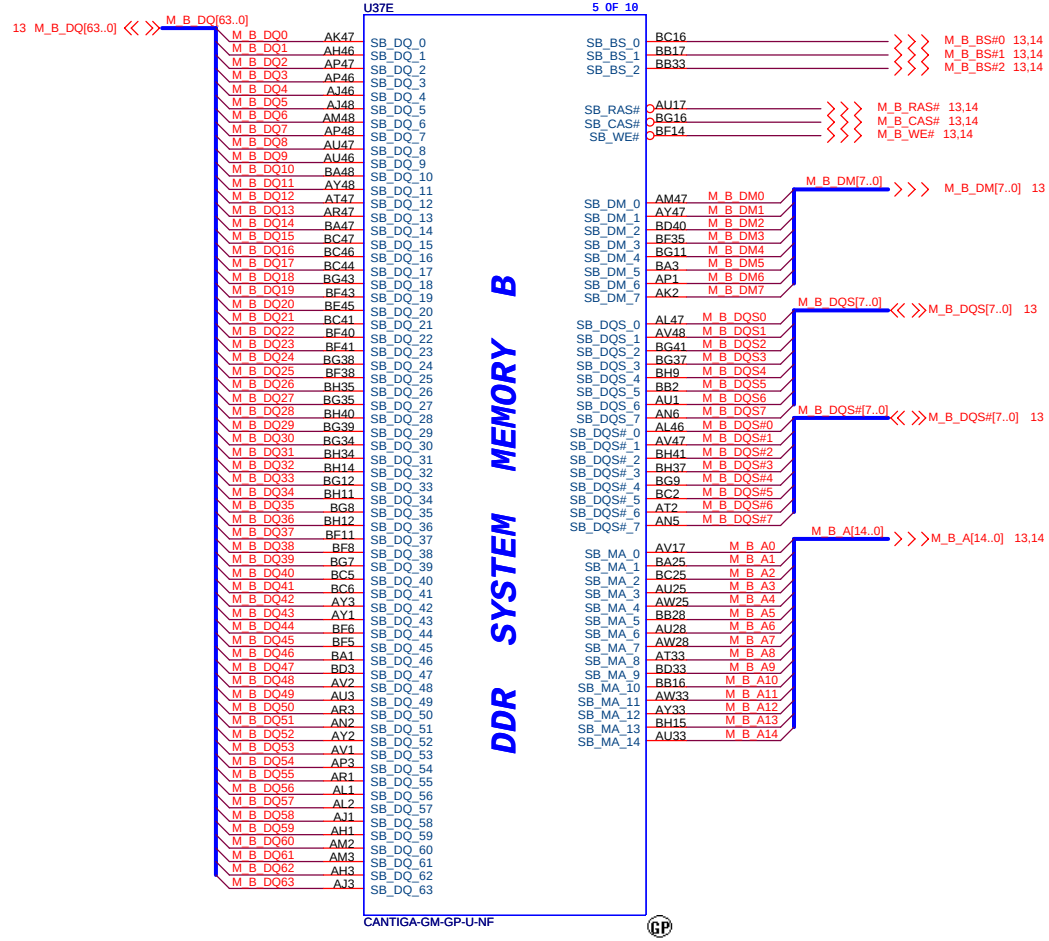

970

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | ***Cantiga (1 of 6)*** | |
| Size | Document Number: **Homa** | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 6 of 57 | |


Close to GMCH as 500 mils.
U37B
2 OF 10
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
U37C
3 OF 10
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
FOR Cantiga:500 ohm
Teenah: 392 ohm
for HDMI port C
layout take note
FOR Discrete change RN to 0 ohm (66.R0036.A8L)
FOR Discrete,change to 0 ohm (66.R0036.A8L)
UMA
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga (2 of 6)
Size
Document Number
Homa
Rev
-1
Date: Thursday, April 03, 2008
Sheet 7 of 57



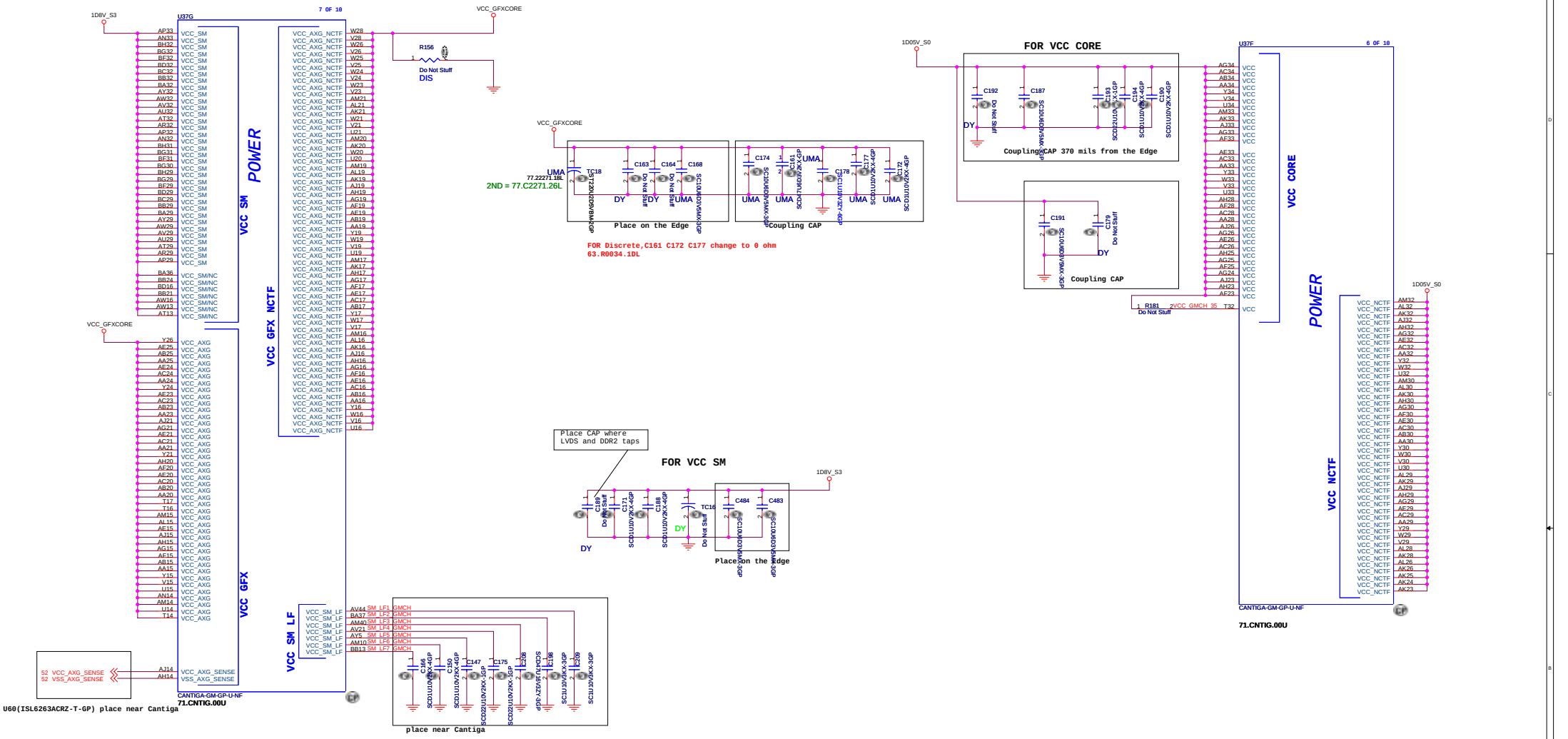



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga (3 of 6)

Size | Document Number: Homa | Rev: -1

Date: Thursday, April 03, 2008 | Sheet 8 of 57



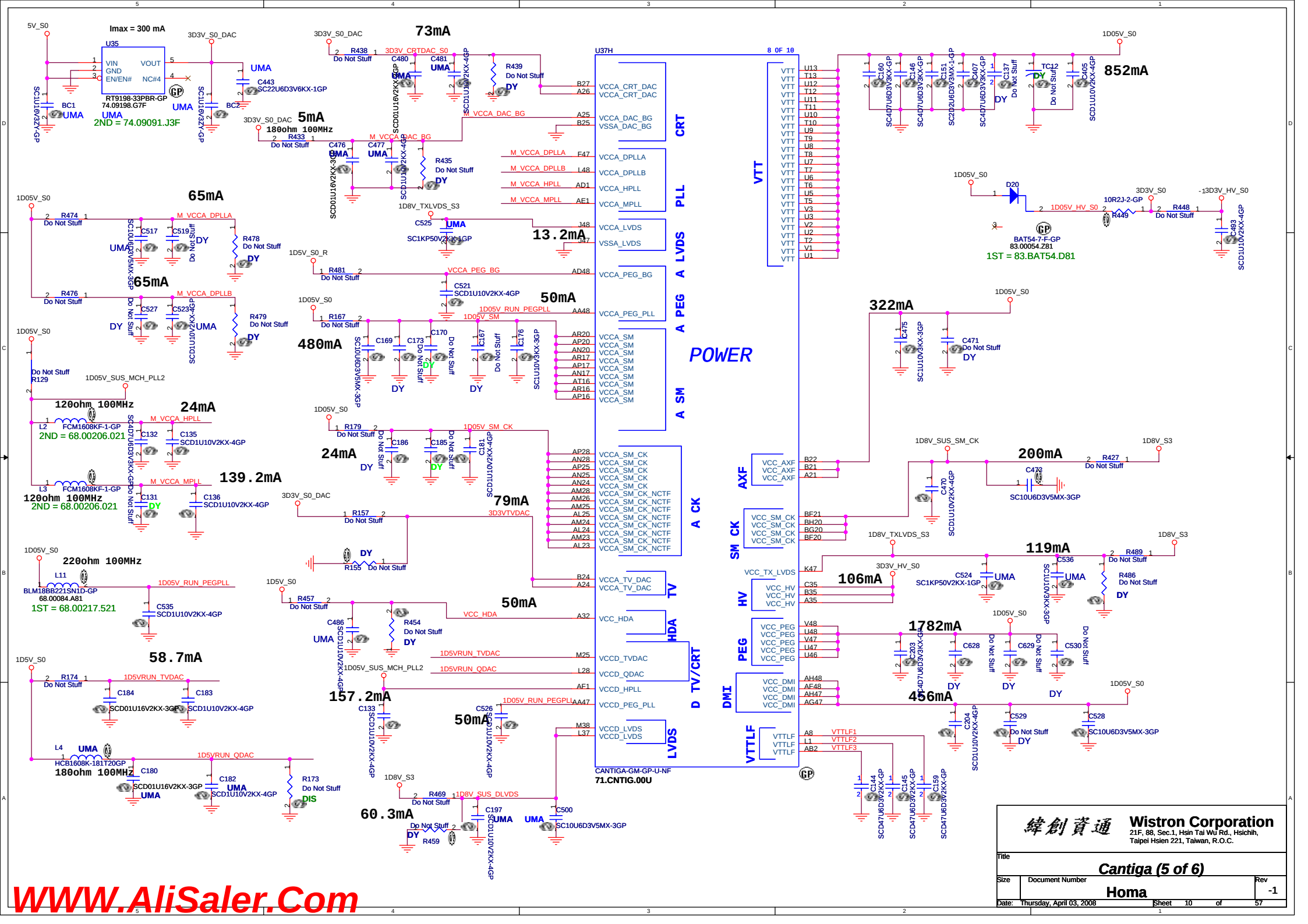


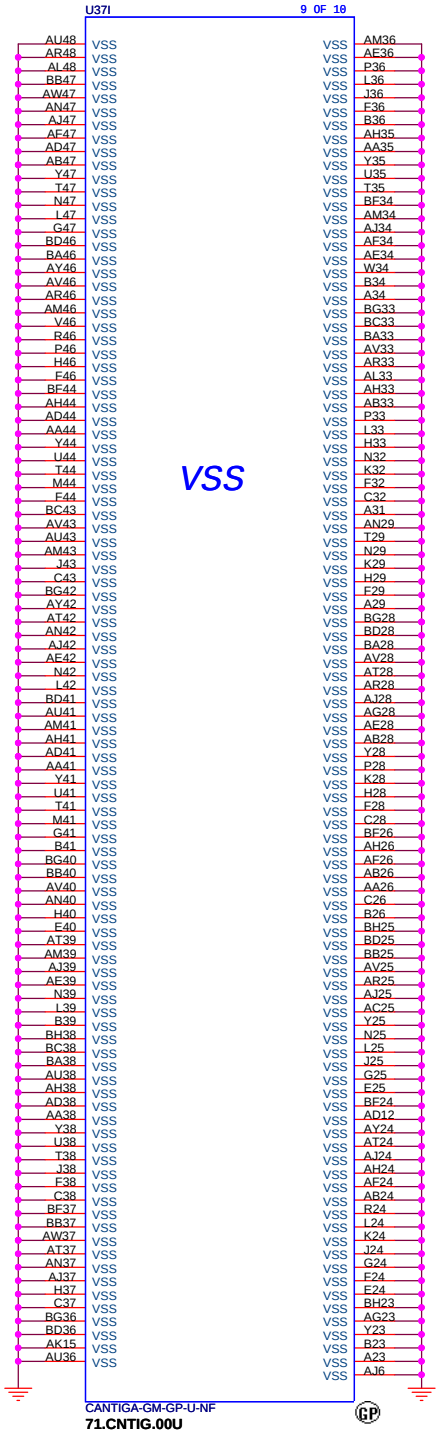
蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

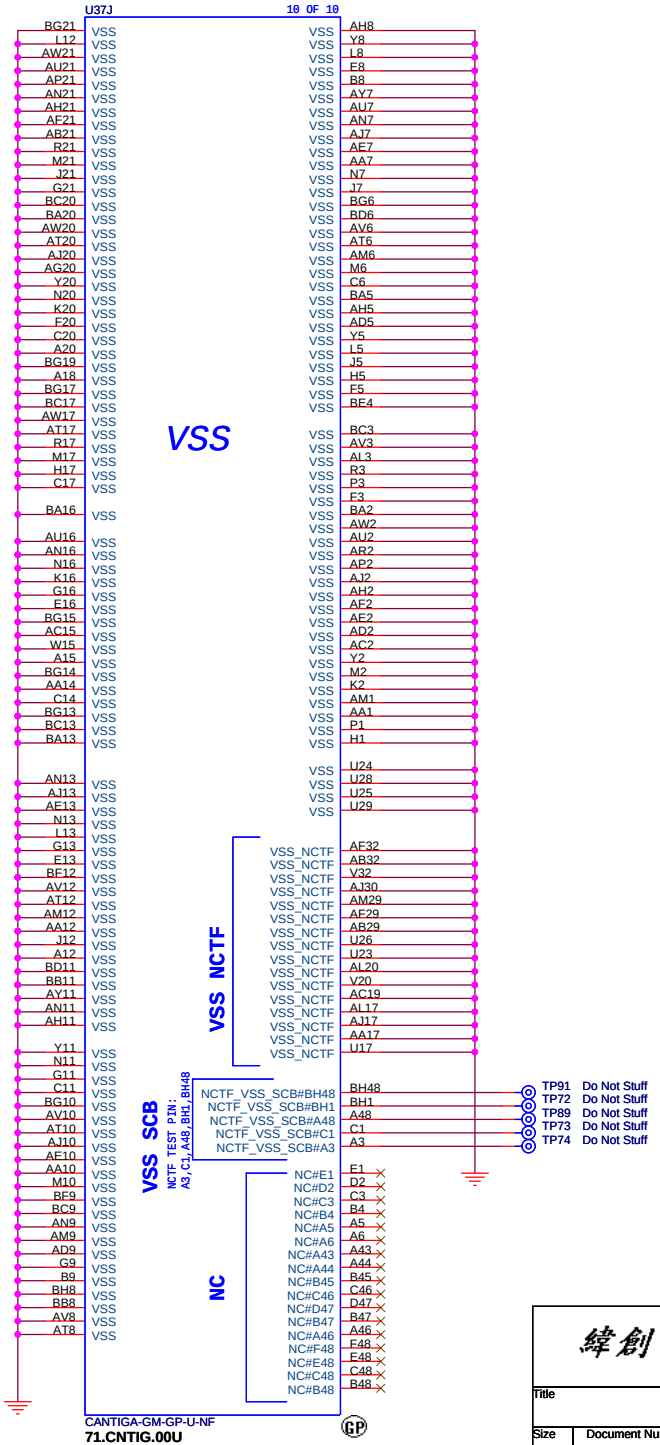

Title: **Cantiga (4 of 6)**

Size: | Document Number: **Homa** | Rev: -1

Date: Thursday, April 03, 2008 Sheet 9 of 57


POWER
U37H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
8 OF 10
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
73mA
5mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
79mA
50mA
157.2mA
50mA
60.3mA
322mA
200mA
119mA
106mA
1782mA
456mA
852mA
58.7mA
Imax = 300 mA
RT9198-33PBR-GP
74.09198.G7F
2ND = 74.09091.J3F
120ohm 100MHz
2ND = 68.00206.021
220ohm 100MHz
68.00084.A81
1ST = 68.00217.521
180ohm 100MHz
BAT54-7-F-GP
83.00054.Z81
1ST = 83.BAT54.D81
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Cantiga (5 of 6)
Homa
Rev -1
Date: Thursday, April 03, 2008
Sheet 10 of 57
WWW.AliSaler.Com



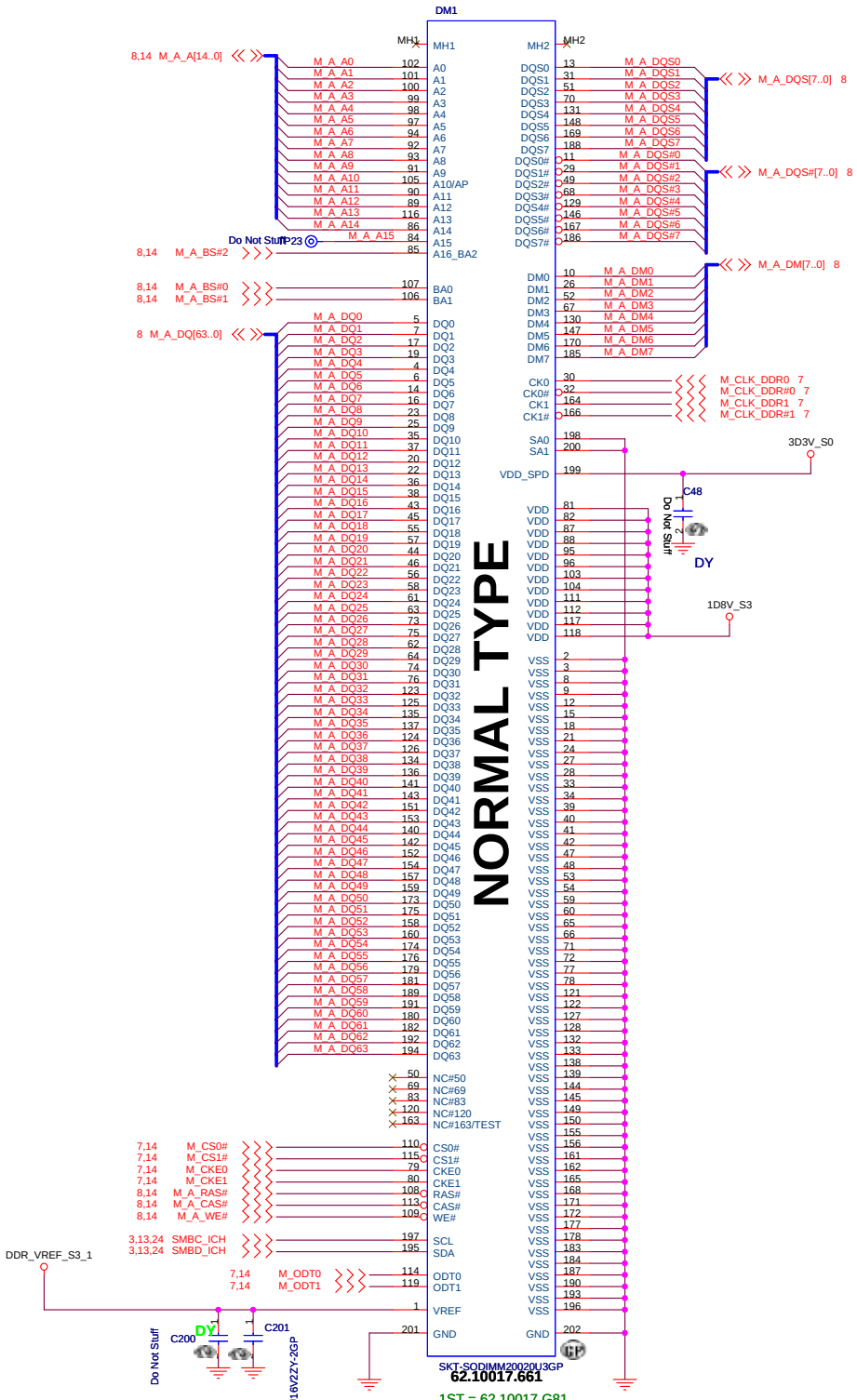




緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cantiga (6 of 6)***

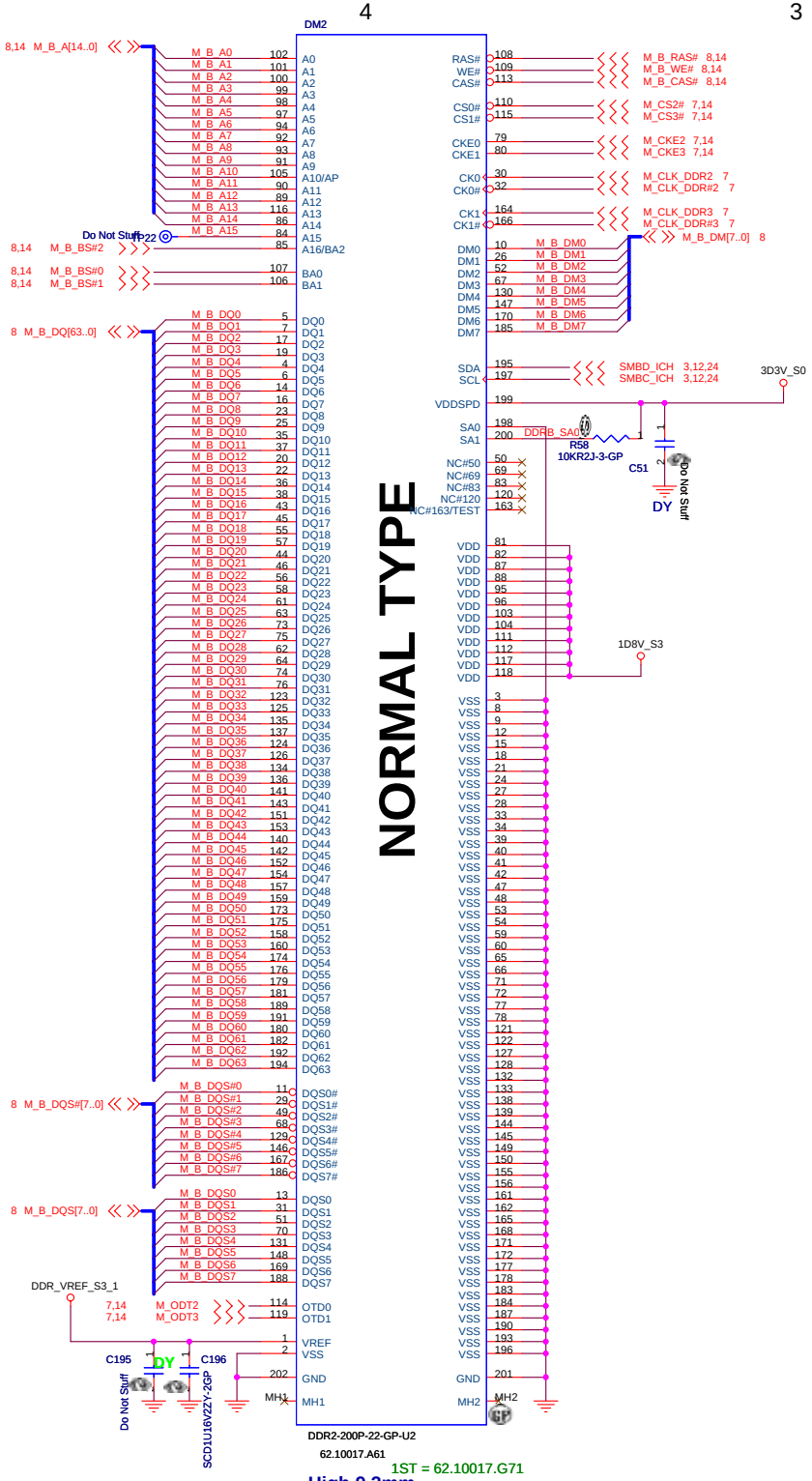
| Size | Document Number | Rev |
|---|---|---|
| | Homa | -1 |

Date: Thursday, April 03, 2008 Sheet 11 of 57





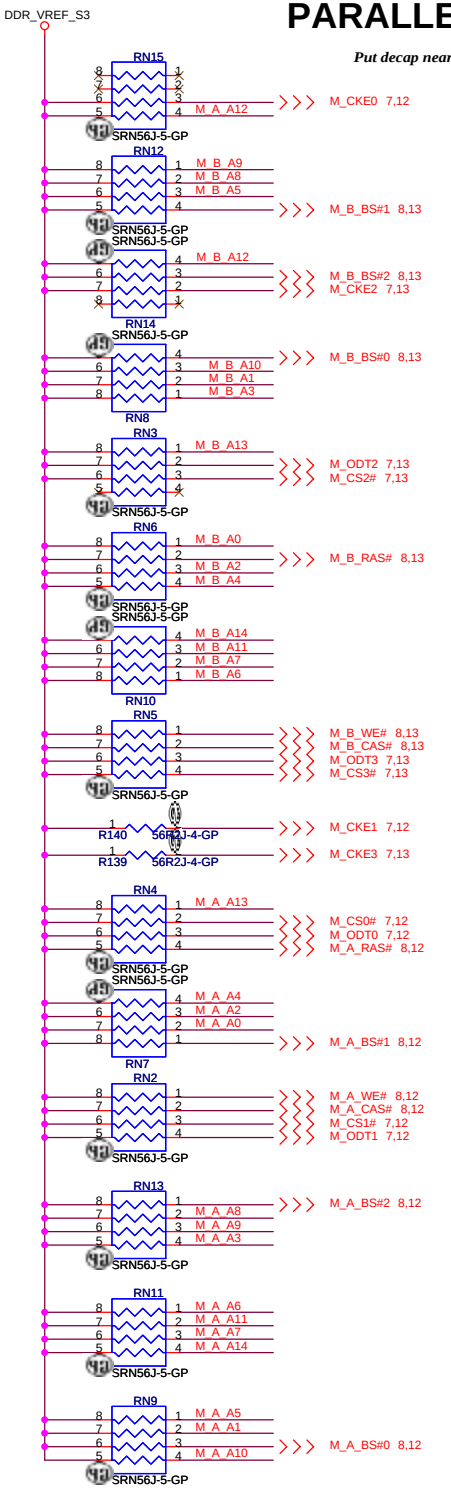

| | | |
|---|---|---|
| 蜂創資通 | Wistron Corporation | |
| | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | DDR2 Socket 1 | |
| Size | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 12 of 57 | |




| | |
|---|---|
| Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | DDR2 Socket 2 |
| Size | Document Number: Homa |
| Rev | -1 |
| Date: Thursday, April 03, 2008 | Sheet 13 of 57 |

# PARALLEL TERMINATION

*Put decap near power(0.9V) and pull-up resistor*

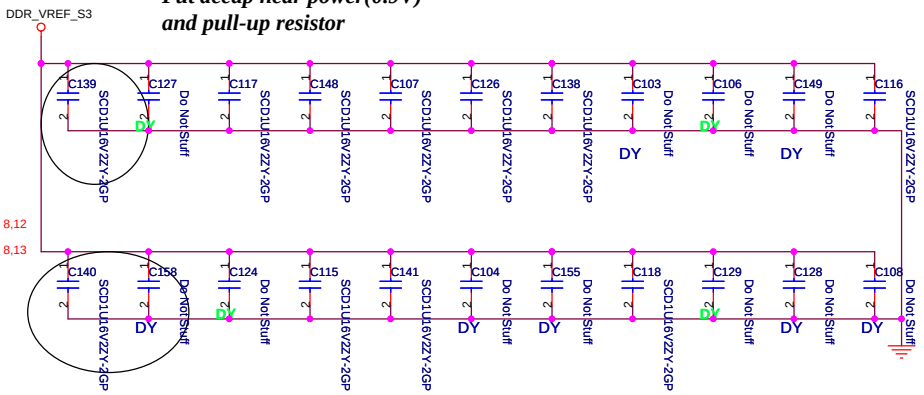


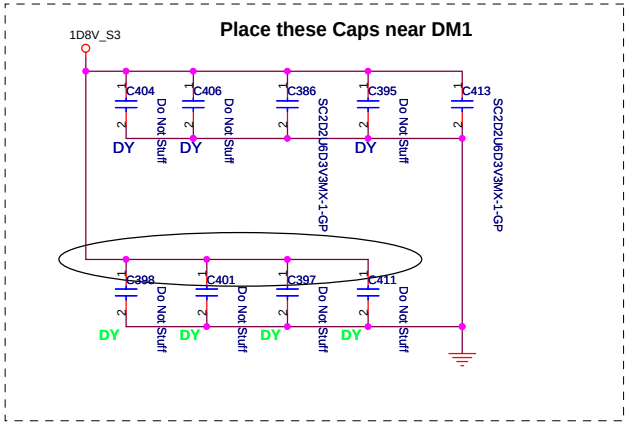

M_A_A[14..0] M_A_A[14..0] 8,12

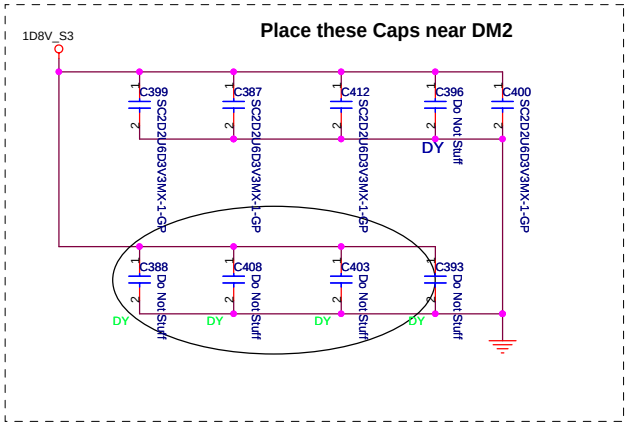
M_B_A[14..0] M_B_A[14..0] 8,13

# Decoupling Capacitor

*Put decap near power(0.9V) and pull-up resistor*

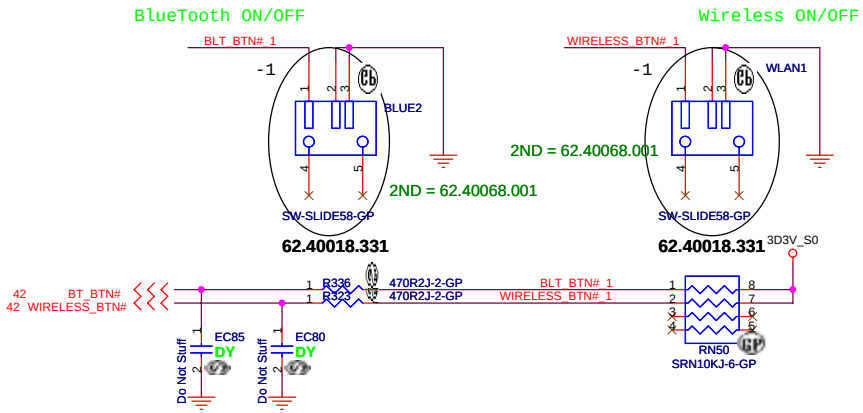





| | |
|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | ***DDR2 Termination Resistor*** |
| Size | Document Number: **Homa** Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 14 of 57 |



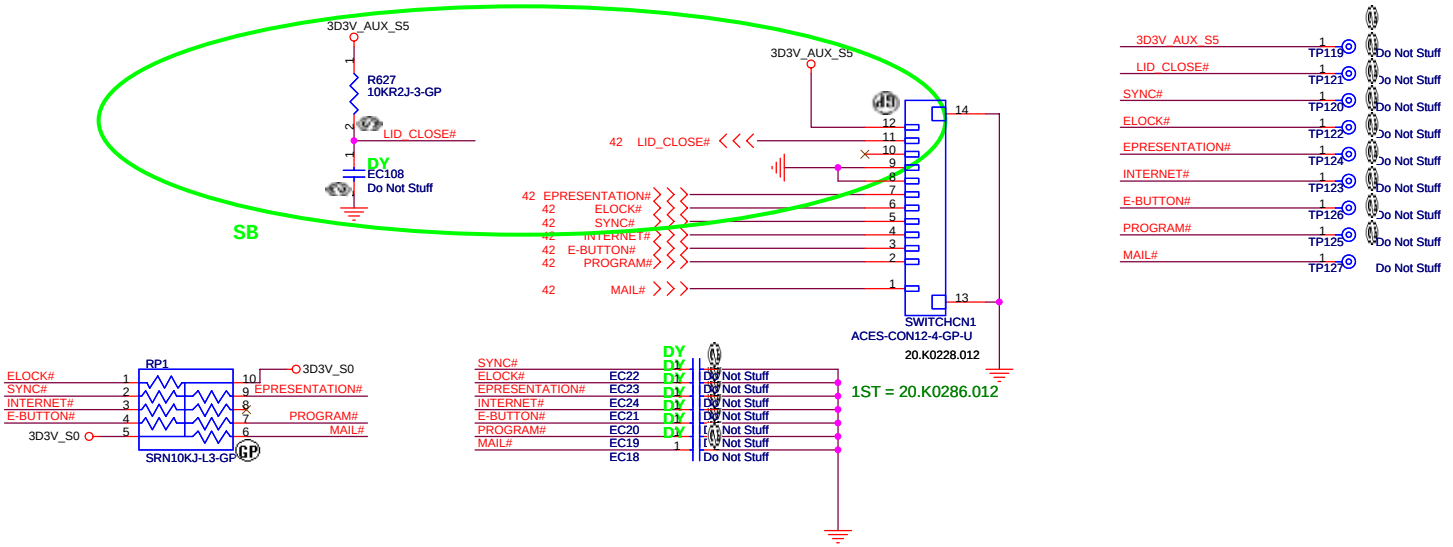

970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SWITCH**

Size | Document Number: Homa | Rev: -1

Date: Thursday, April 03, 2008 | Sheet 15 of 57



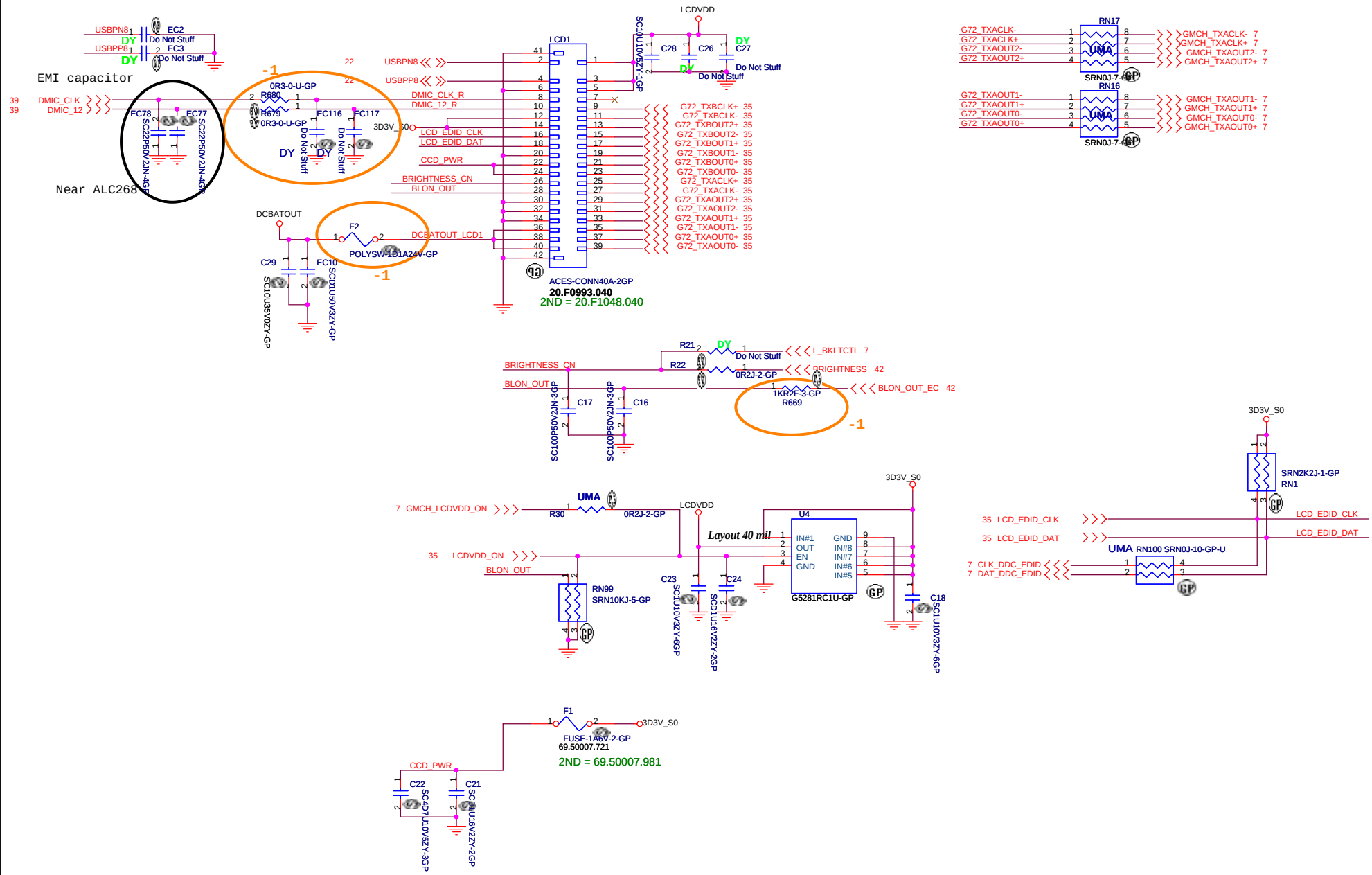




970

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***LAUNCH*** | |
| Size | Document Number<br>**Homa** | Rev<br>-1 |
| Date: Thursday, April 03, 2008 | Sheet 16 of 57 | |

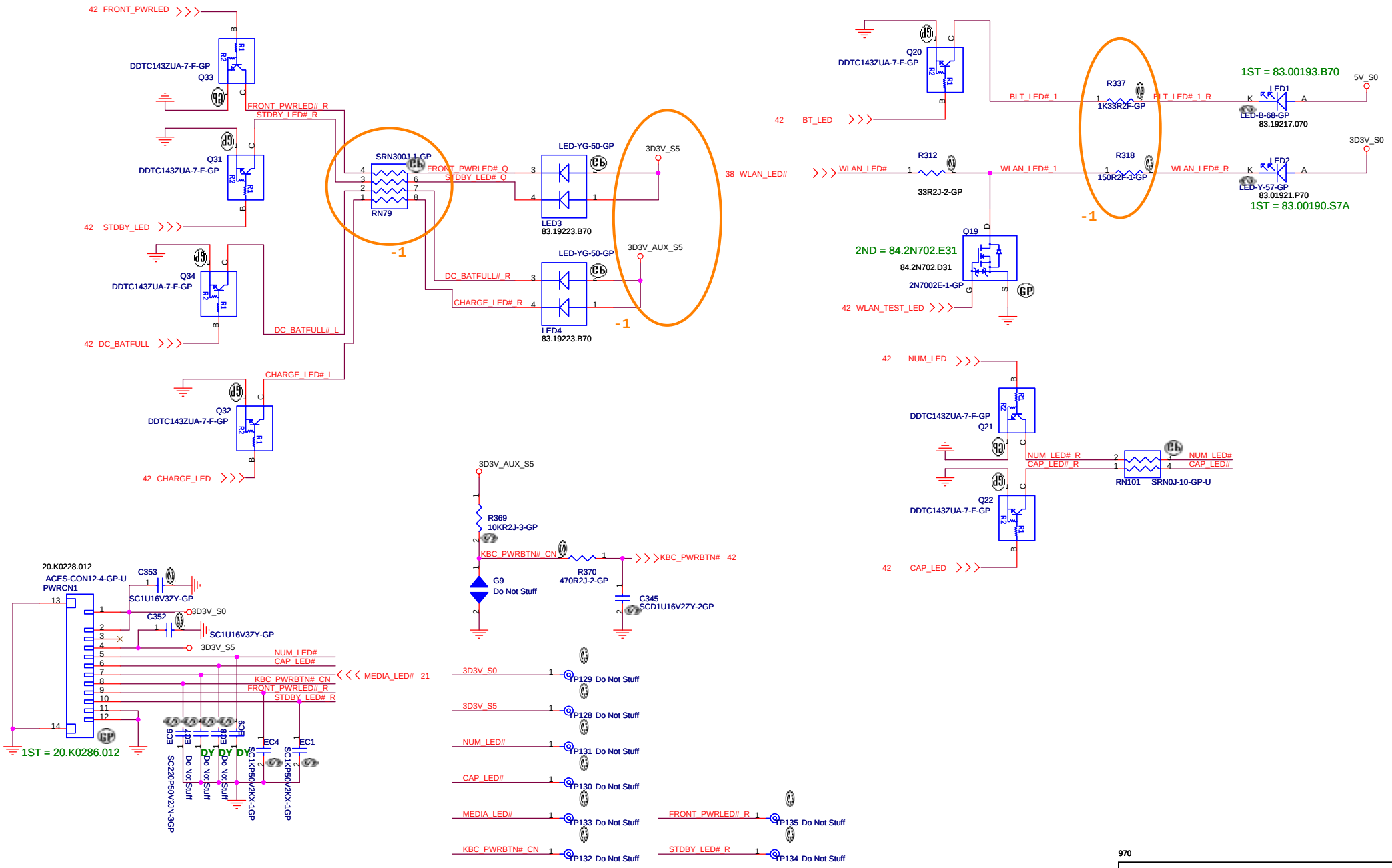
# LCD/INVERTER/CCD CONN




970

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***LCD CONN*** | |
| Size | Document Number<br>**Homa** | Rev<br>-1 |
| Date: Thursday, April 03, 2008 | Sheet 17 of 57 | |

# LED

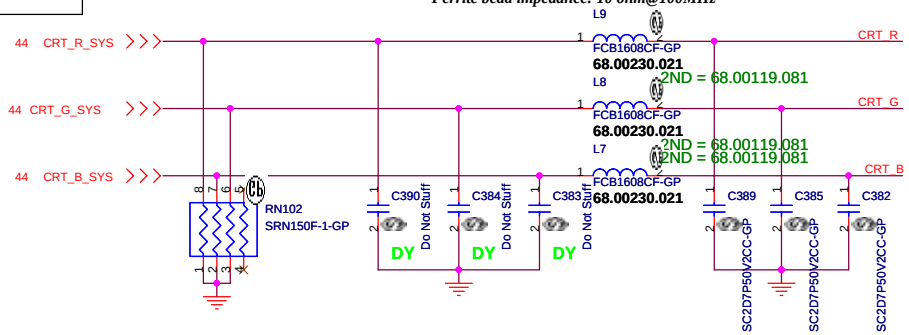



970

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***LED*** | |
| Size | Document Number<br>**Homa** | Rev<br>-1 |
| Date: Thursday, April 03, 2008 | Sheet 18 of 57 | |

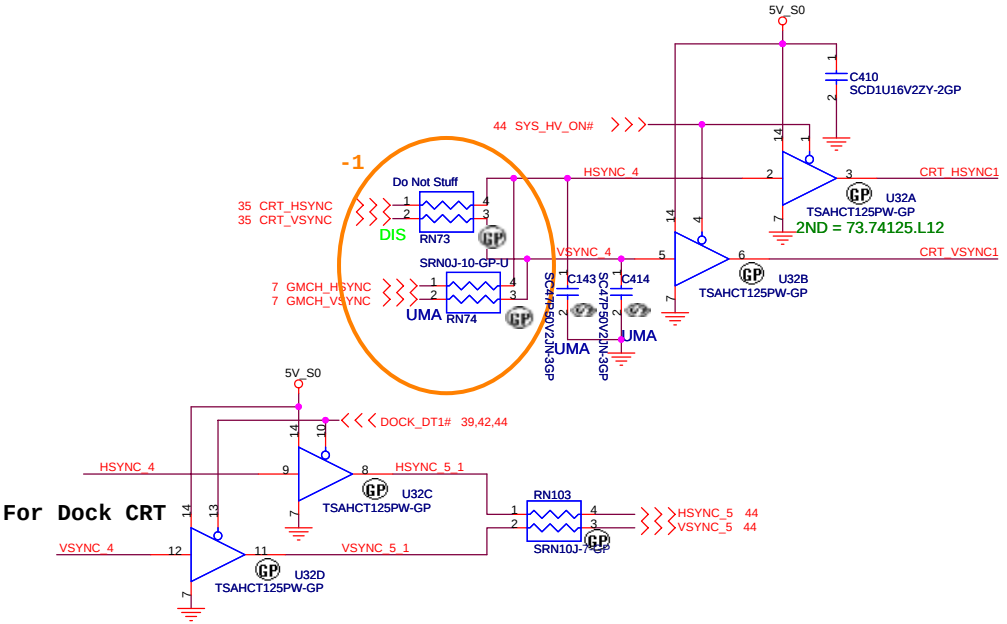
Layout Note:
Place these resistors close to the CRT-out connector

*Ferrite bead impedance: 10 ohm@100MHz*

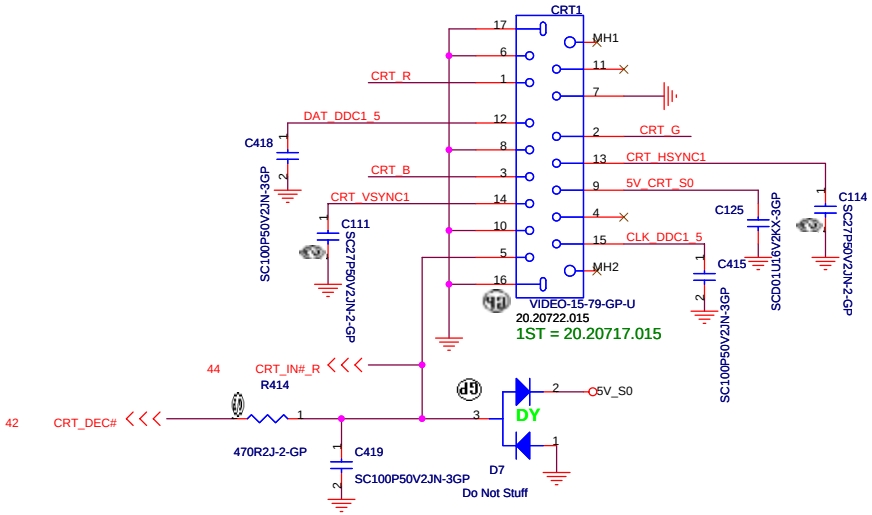



***Layout Note:***
**** Must be a ground return path between this ground and the ground on the VGA connector.***
***Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.***

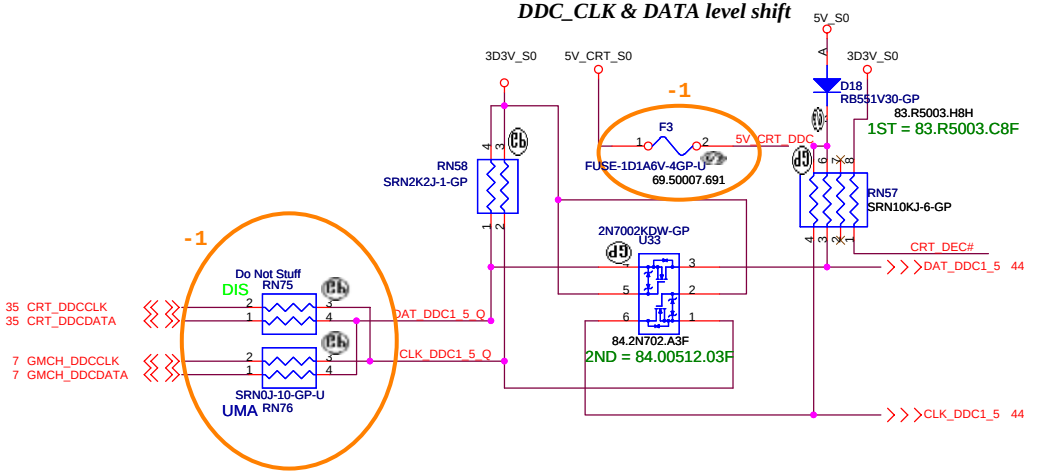
*Hsync & Vsync level shift*




# CRT I/F & CONNECTOR




*DDC_CLK & DATA level shift*



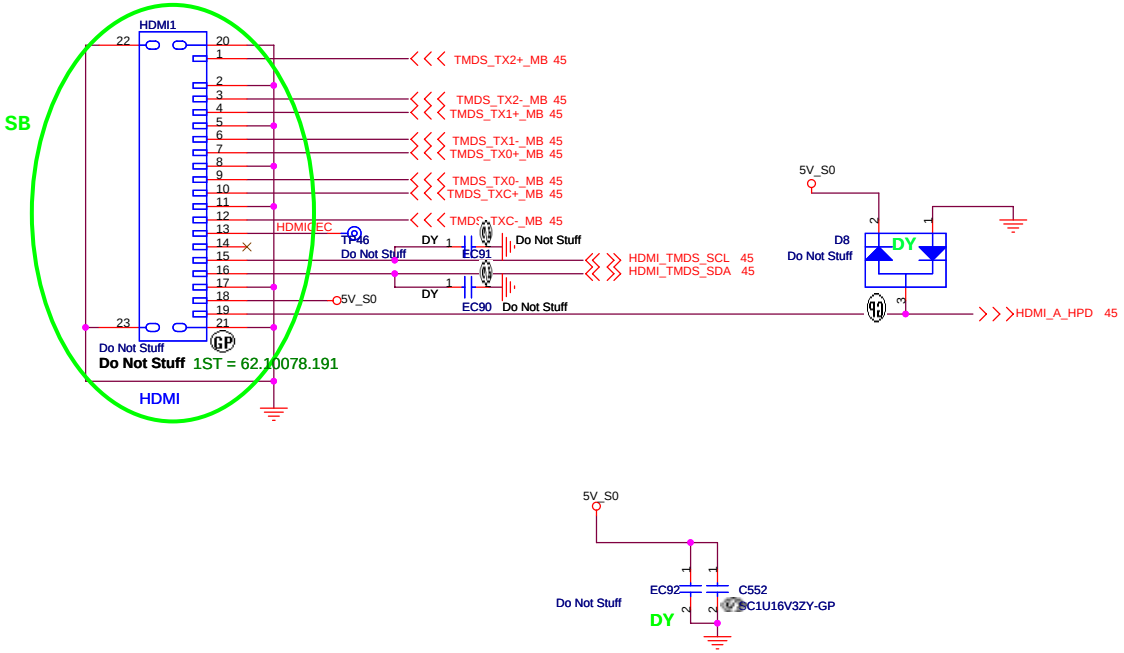

970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

| Size | Document Number | Rev |
|---|---|---|
| | Homa | -1 |

Date: Thursday, April 03, 2008 Sheet 19 of 57

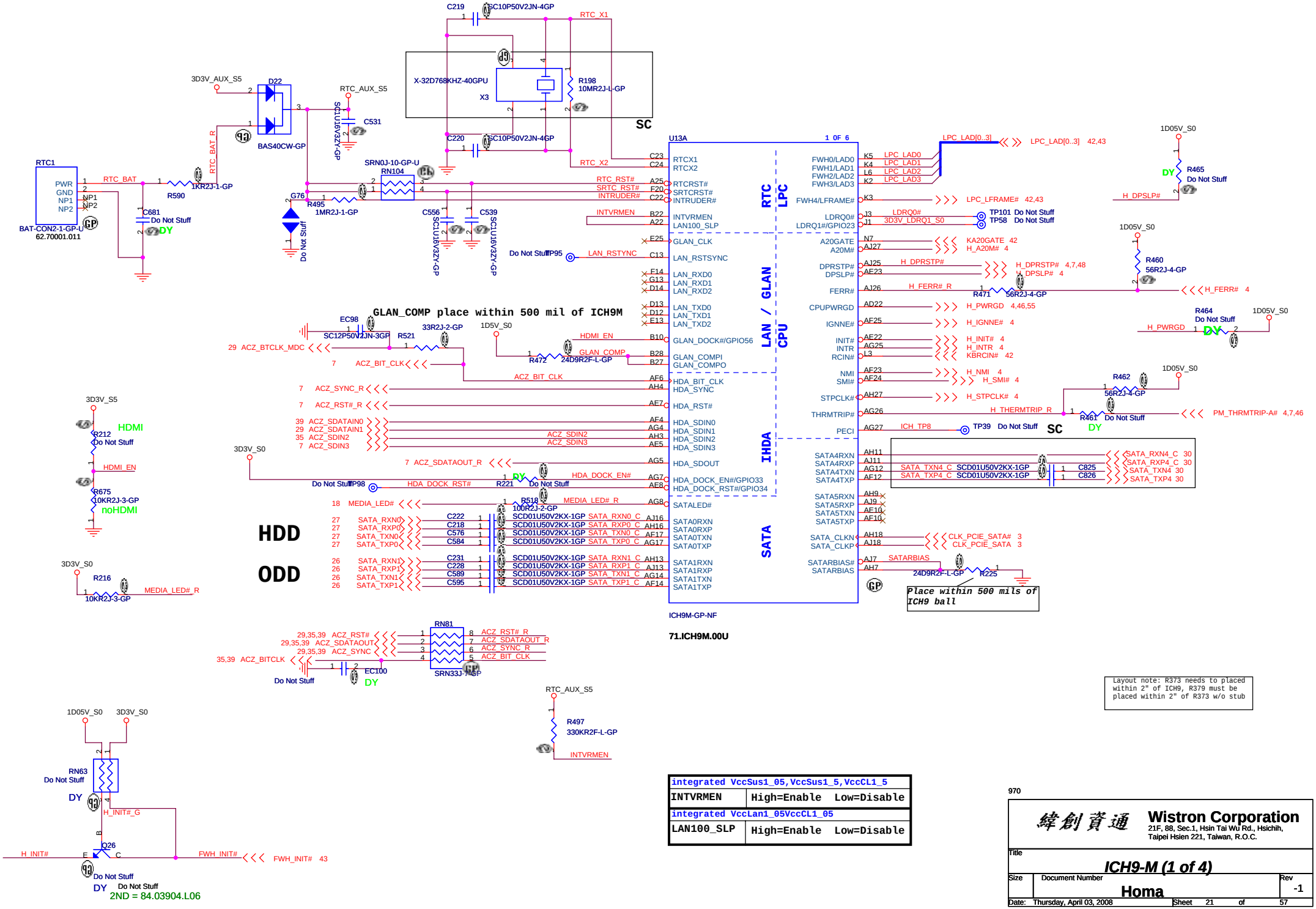


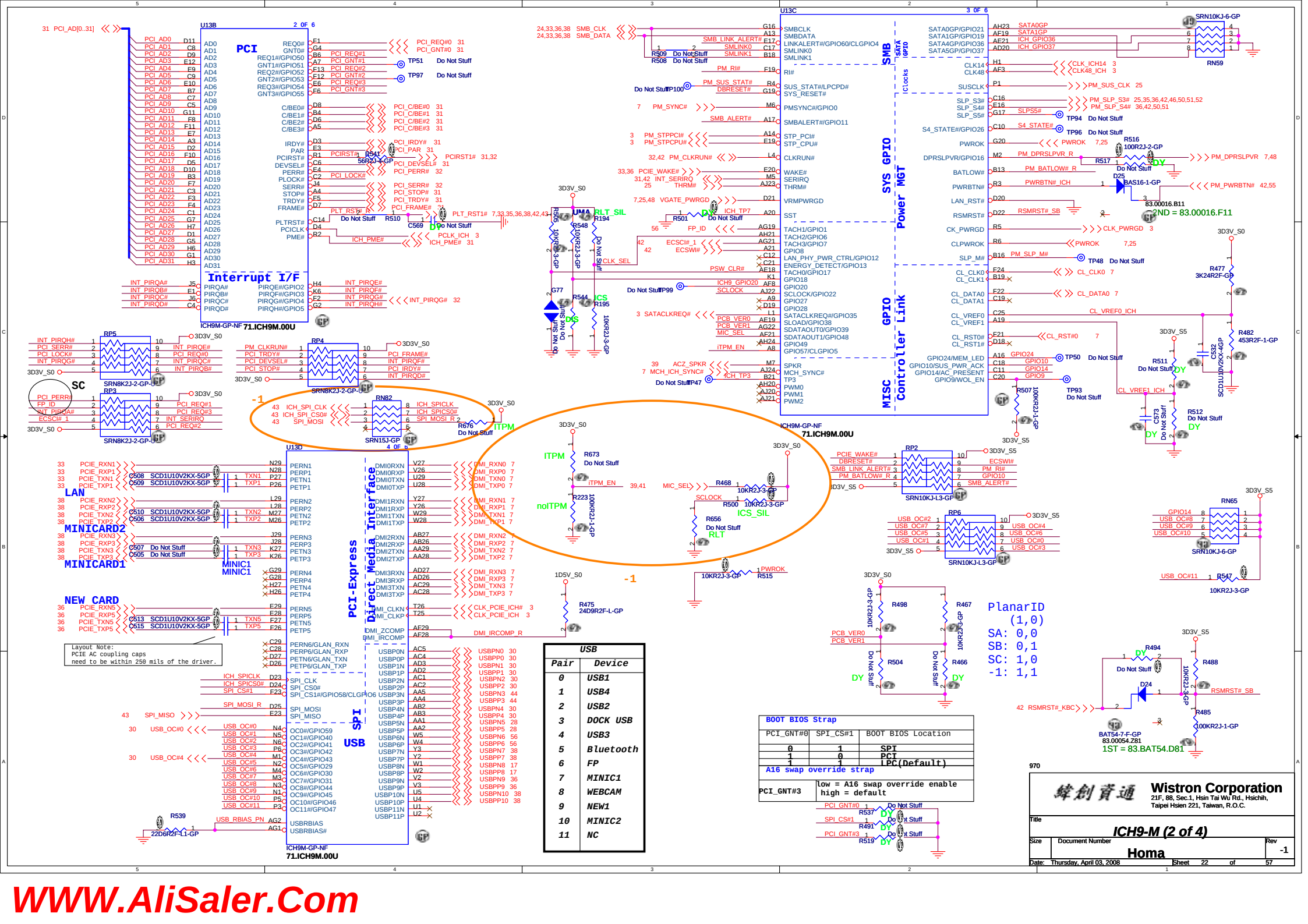


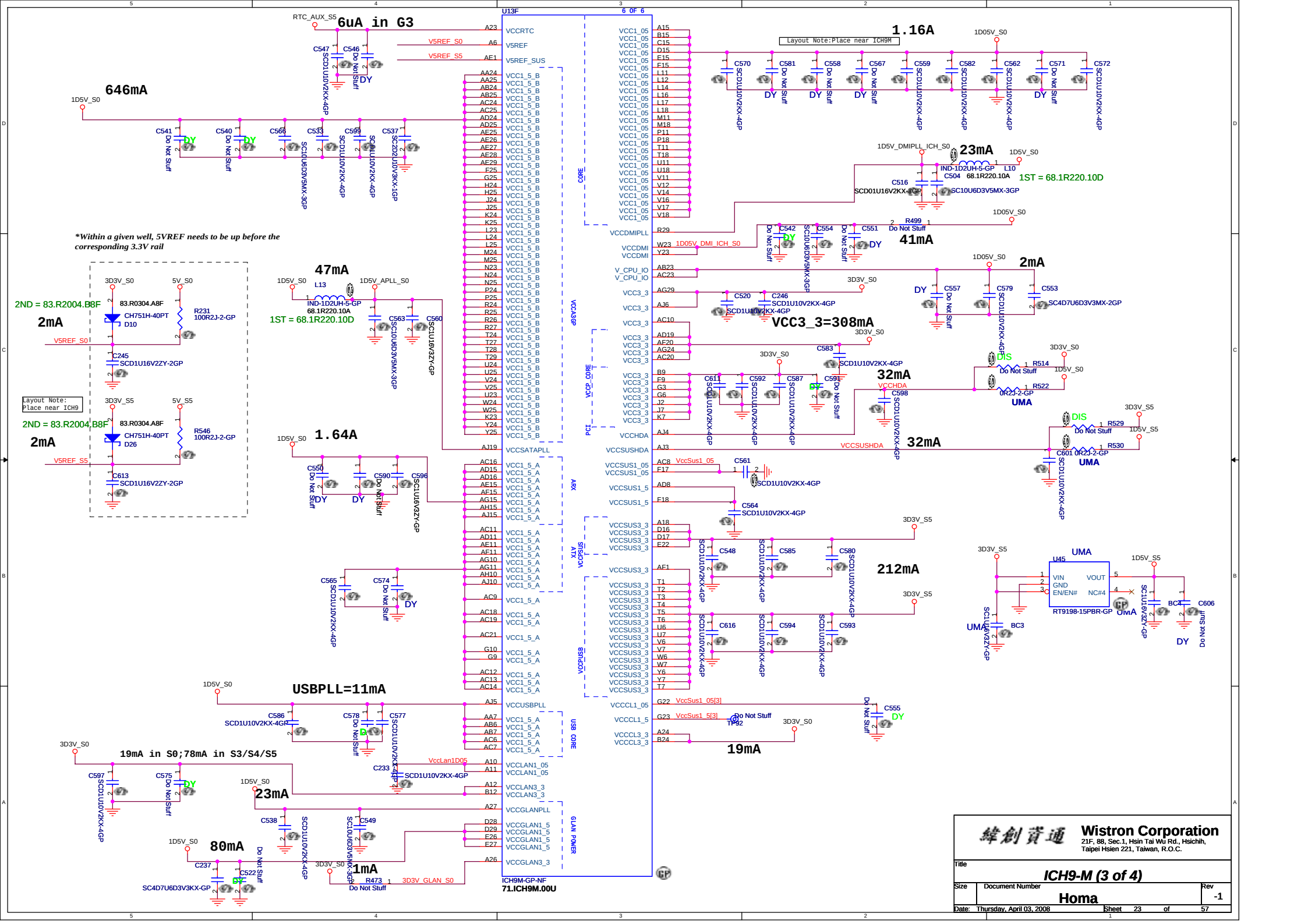


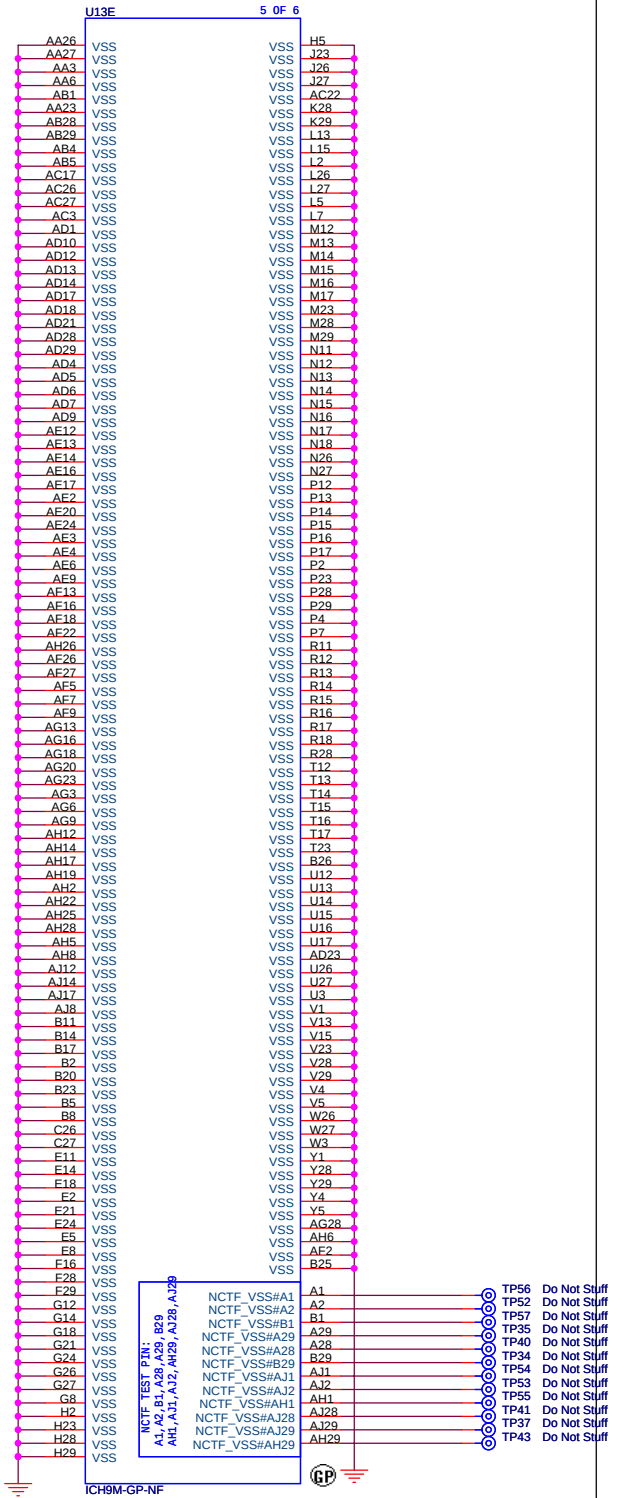
970

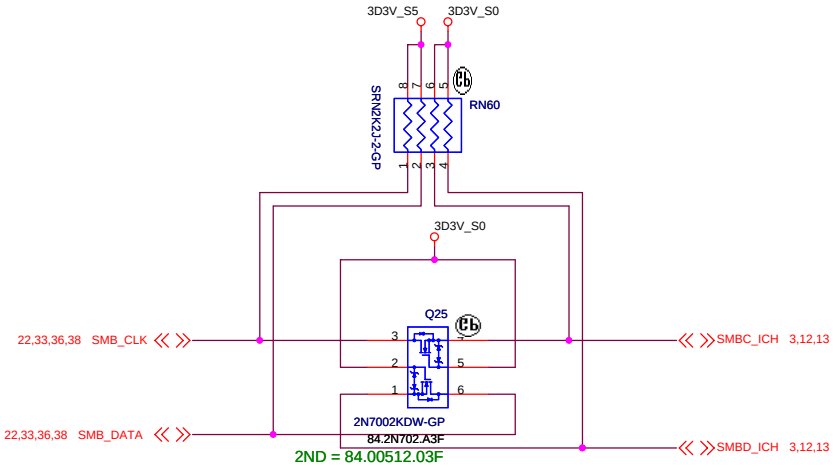
| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: HDMI CONNECTOR | | |
| Size: A3 | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 20 of 57 | |


GLAN_COMP place within 500 mil of ICH9M
HDD
ODD
SC
U13A
1 OF 6
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
ICH9M-GP-NF
71.ICH9M.00U
Place within 500 mils of ICH9 ball
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (1 of 4)
Homa
Date: Thursday, April 03, 2008
Sheet 21 of 57
2ND = 84.03904.L06




6uA in G3
646mA
1.16A
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
2ND = 83.R2004.B8F
2mA
1ST = 68.1R220.10D
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
U13F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
Homa
Thursday, April 03, 2008
Sheet 23 of 57



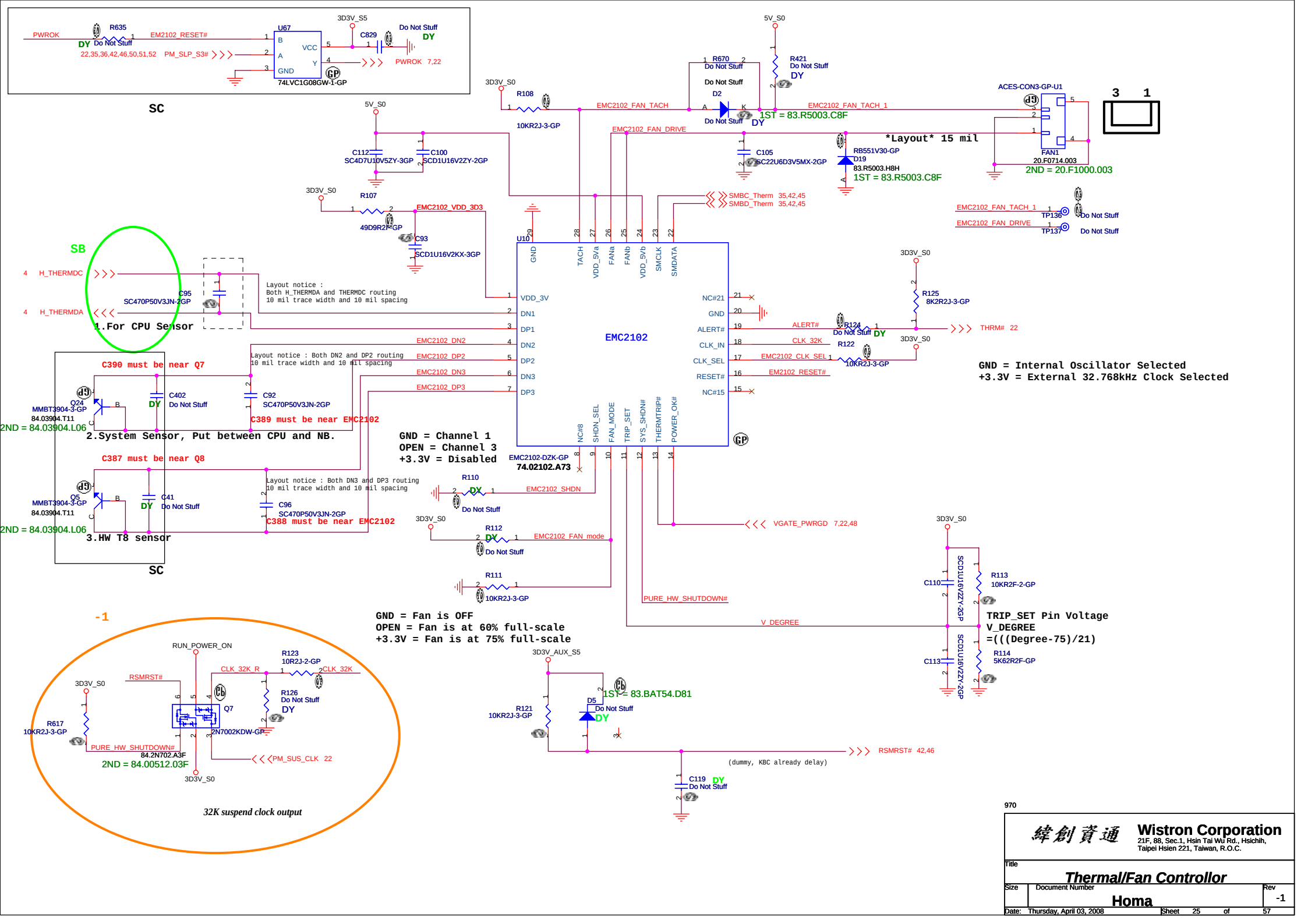




*Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance*

## SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | ICH9-M (4 of 4) | |
| Size | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 24 of 57 | |




970

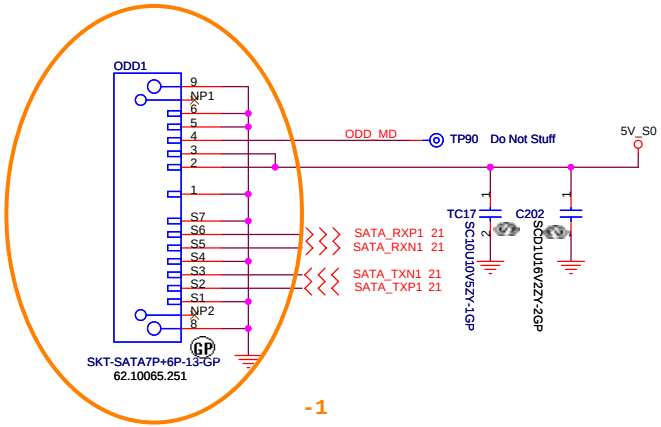
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

| Size | Document Number | Rev |
|---|---|---|
| | Homa | -1 |

Date: Thursday, April 03, 2008 Sheet 25 of 57

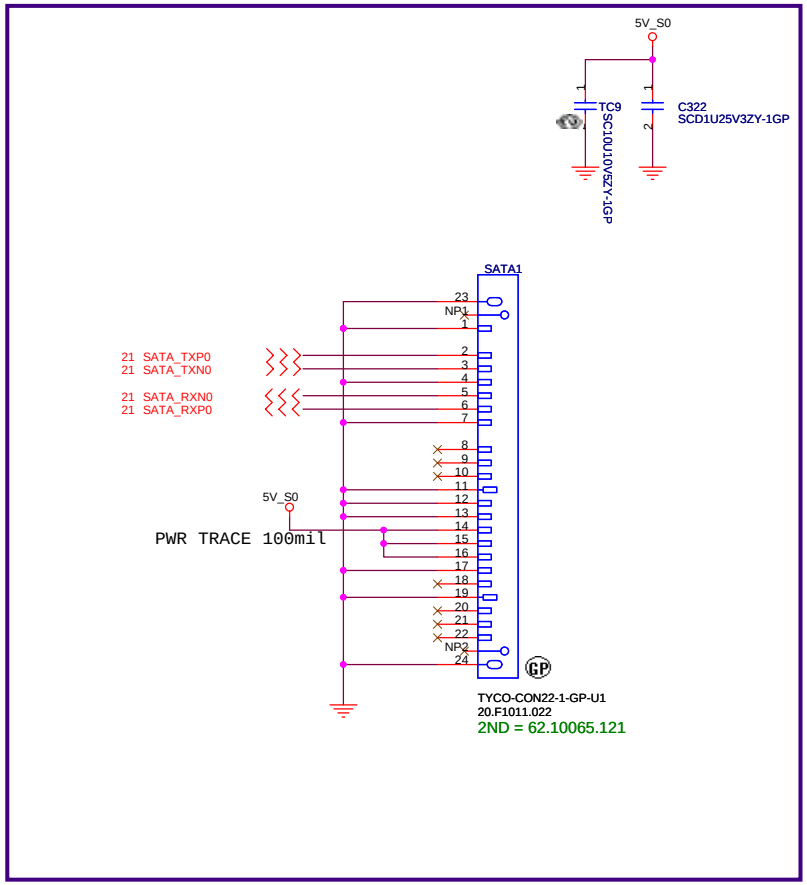
# ODD Connector




970

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: CDROM | | |
| Size | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 26 of 57 | |

# SATA Connector

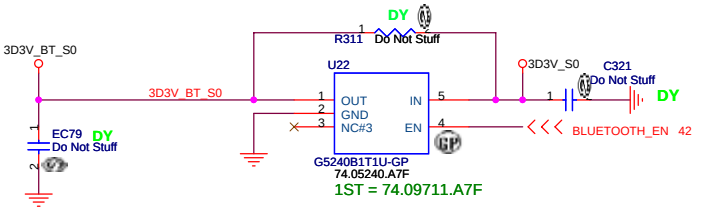



970

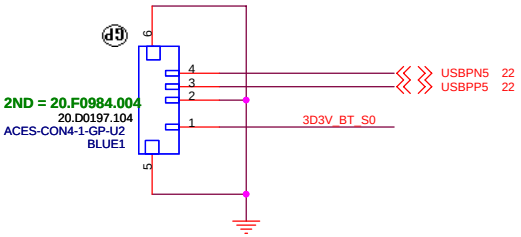
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

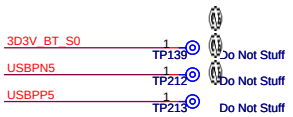
| Title | | |
|---|---|---|
| ***HDD*** | | |
| Size | Document Number | Rev |
| | **Homa** | -1 |
| Date: Thursday, April 03, 2008 | Sheet 27 of 57 | |

# BLUETOOTH MODULE




EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

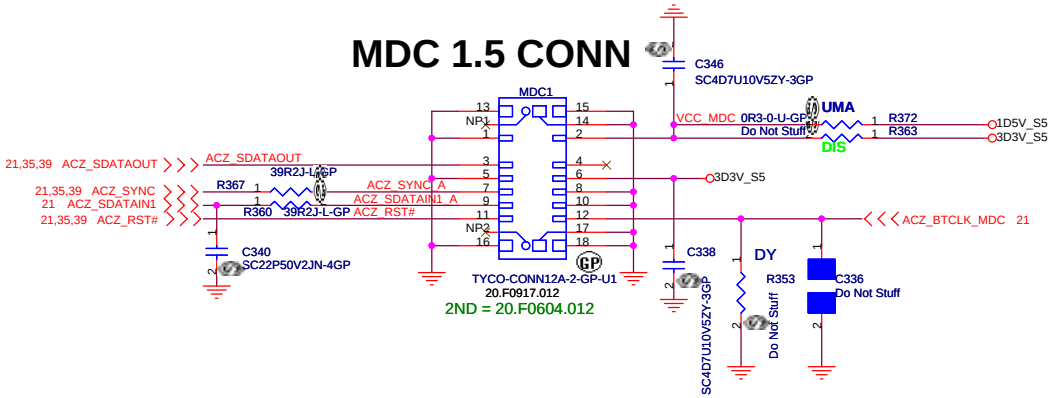



970

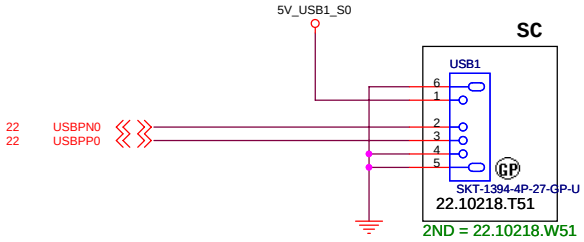
| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: BLUETOOTH | | |
| Size | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 28 of 57 | |

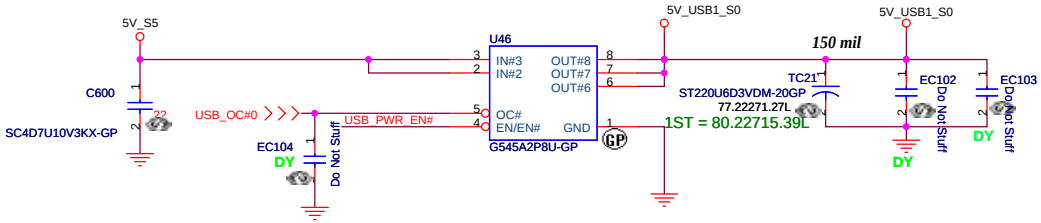
# MDC 1.5 CONN

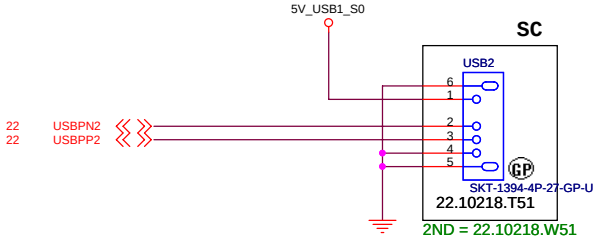


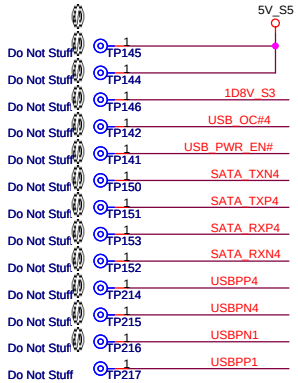

970

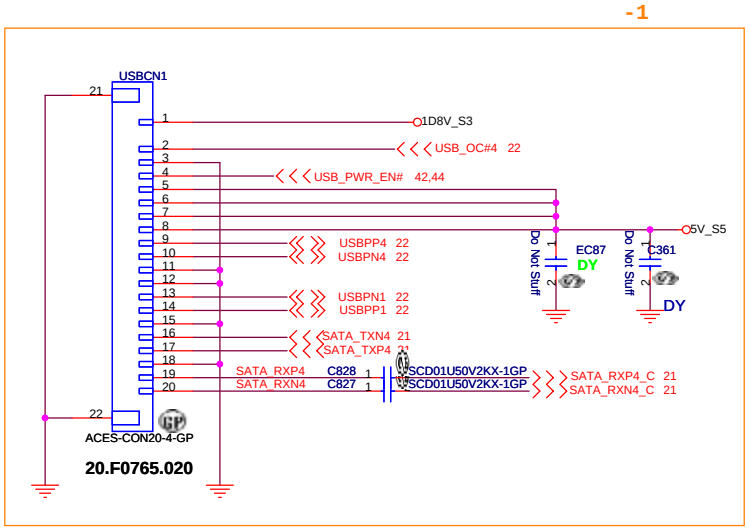
| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: MDC | | |
| Size | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 29 of 57 | |



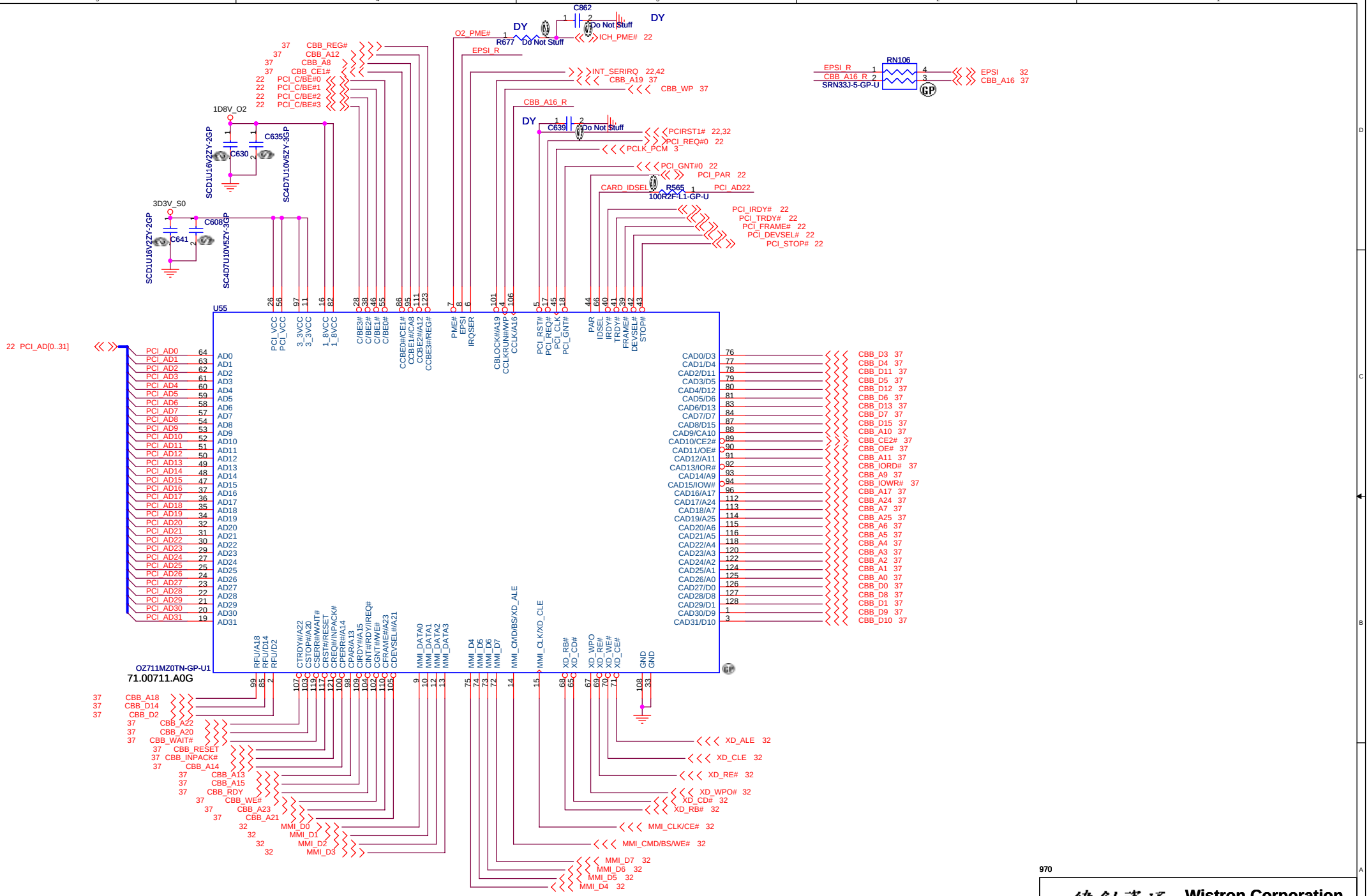

970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB

Size | Document Number: Homa | Rev: -1

Date: Thursday, April 03, 2008 | Sheet 30 of 57



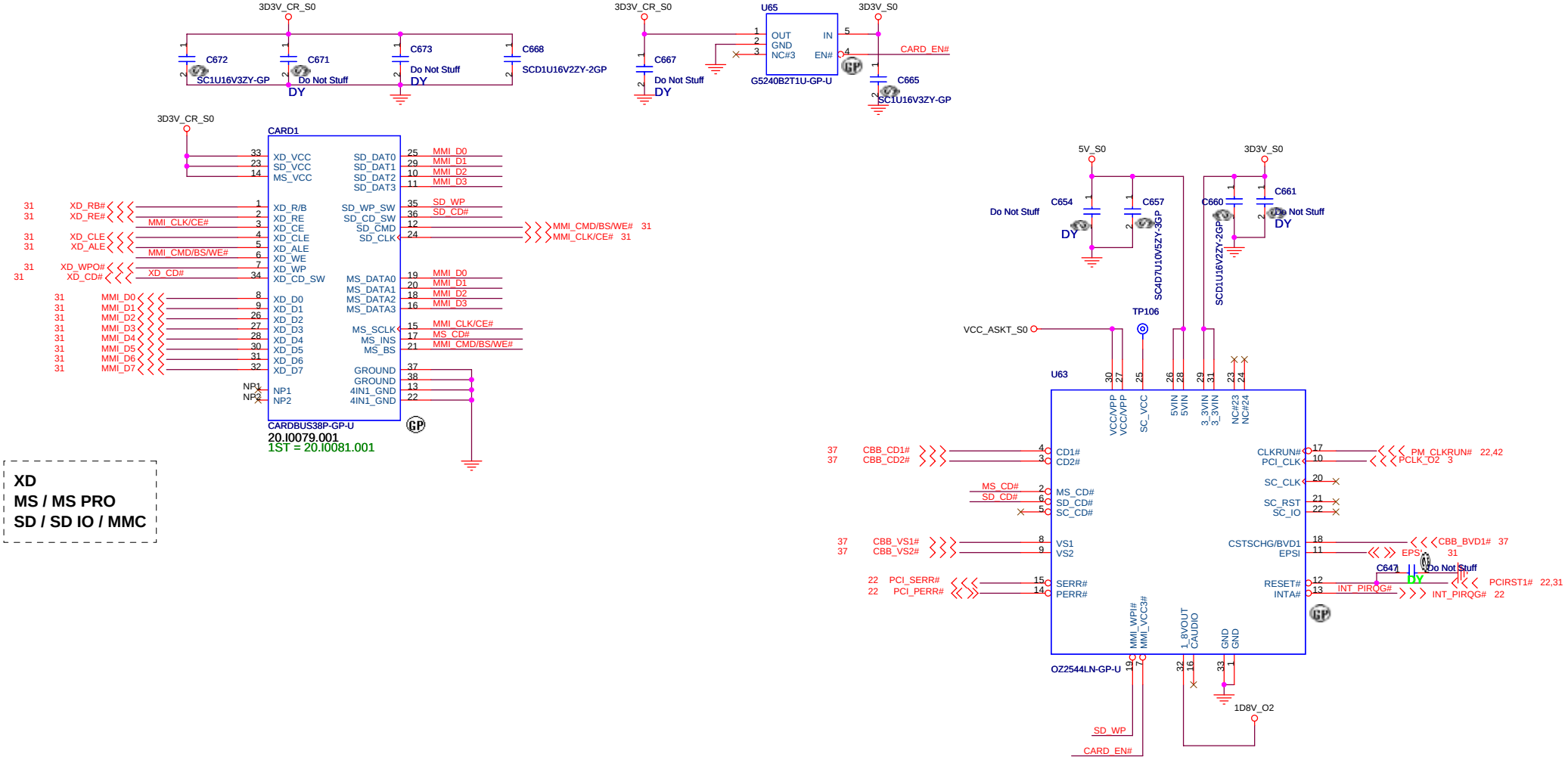

970

**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader Controller - OZ711*

| Size | Document Number | Rev |
|---|---|---|
| | Homa | -1 |

Date: Thursday, April 03, 2008 Sheet 31 of 57



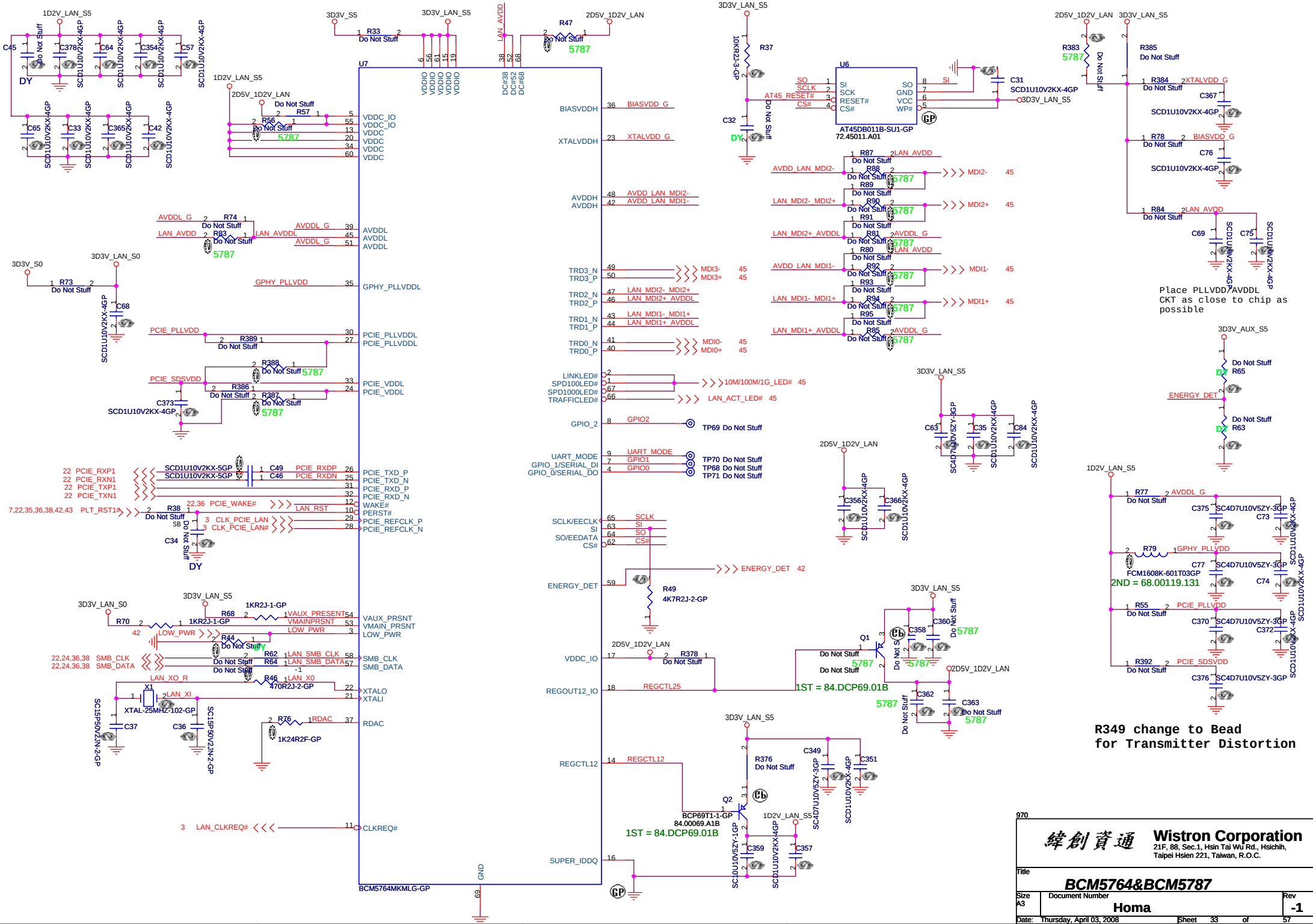

970

**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader Connector*

| Size | Document Number | Rev |
|---|---|---|
| | Homa | -1 |

Date: Thursday, April 03, 2008 Sheet 32 of 57

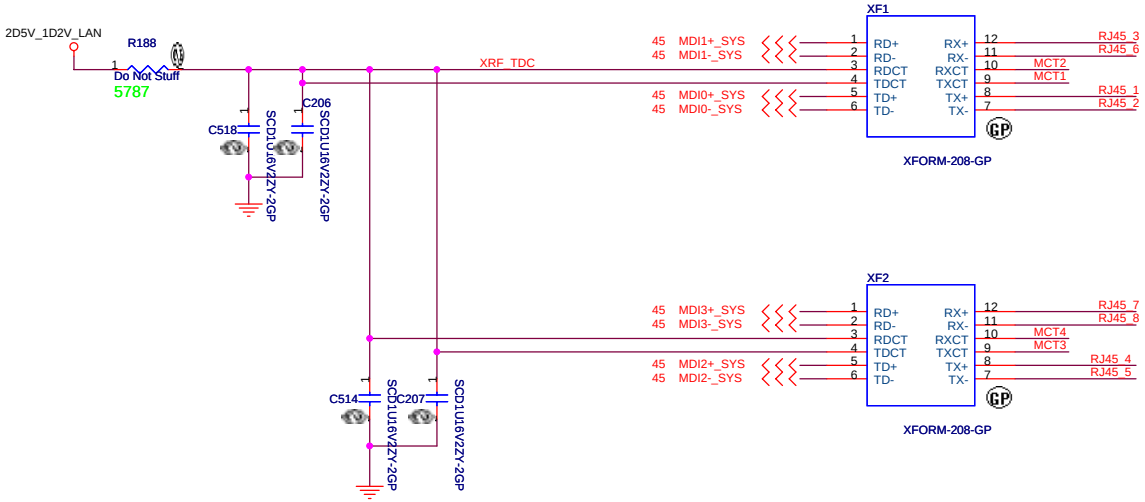

U7
BCM5764MKMLG-GP
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
1ST = 84.DCP69.01B
1ST = 84.DCP69.01B
2ND = 68.00119.131
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM5764&BCM5787
Homa
Thursday, April 03, 2008

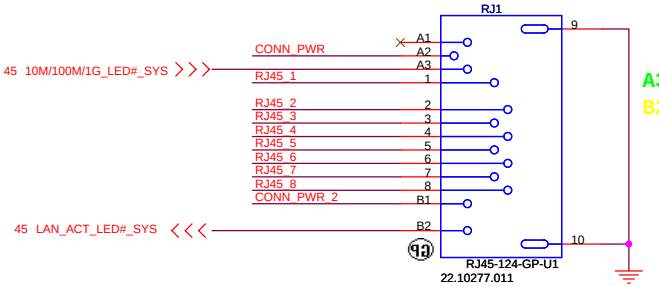
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

# LAN Connector

LAN Connector

GIGA Lan Transformer

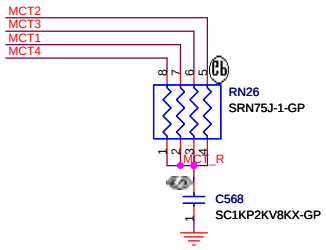


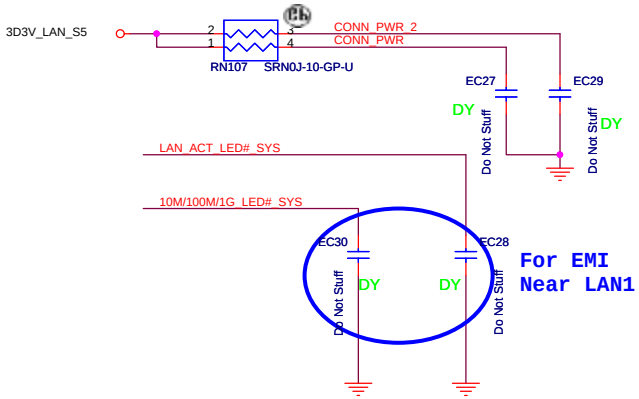




A3:GREEN
B2:Orange

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.




970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

| Size | Document Number | Rev |
|---|---|---|
| A3 | | -1 |

Date: Thursday, April 03, 2008 Sheet 34 of 57

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]

5V_S0
48,49,50,51,52 CPUCORE_ON
22,25,36,42,46,50,51,52 PM_SLP_S3#
R425 Do Not Stuff
R426 Do Not Stuff
DY
PLCORE_ON_MXM
C444 Do Not Stuff
TP76
1D8V_S0
C446 DY Do Not Stuff
C445 DY Do Not Stuff
DIS
Do Not Stuff
MH1
DCBATOUT
C494 DY Do Not Stuff
C495 DY Do Not Stuff
C492 DY Do Not Stuff
C490 DY Do Not Stuff
C491 DY Do Not Stuff

17 G72_TXBOUT0+
17 G72_TXBOUT0-
17 G72_TXBOUT1+
17 G72_TXBOUT1-
17 G72_TXBOUT2+
17 G72_TXBOUT2-
39,44 SPDIF
17 G72_TXBCLK+
17 G72_TXBCLK-
44 CRT_BLUE
44 CRT_GREEN
44 CRT_RED
21,29,39 ACZ_RST#
R149 1 Do Not Stuff DIS

PEG_TXN15 PEG_TXP15 PEG_TXN14 PEG_TXP14 PEG_TXN13 PEG_TXP13 PEG_TXN12 PEG_TXP12 PEG_TXN11 PEG_TXP11 PEG_TXN10 PEG_TXP10 PEG_TXN9 PEG_TXP9 PEG_TXN8 PEG_TXP8 PEG_TXN7 PEG_TXP7 PEG_TXN6 PEG_TXP6 PEG_TXN5 PEG_TXP5 PEG_TXN4 PEG_TXP4 PEG_TXN3 PEG_TXP3 PEG_TXN2 PEG_TXP2 PEG_TXN1 PEG_TXP1 PEG_TXN0 PEG_TXP0
Do Not Stuff TP75
Do Not Stuff TP27

PEG_RXN15 PEG_RXP15 PEG_RXN14 PEG_RXP14 PEG_RXN13 PEG_RXP13 PEG_RXN12 PEG_RXP12 PEG_RXN11 PEG_RXP11 PEG_RXN10 PEG_RXP10 PEG_RXN9 PEG_RXP9 PEG_RXN8 PEG_RXP8 PEG_RXN7 PEG_RXP7 PEG_RXN6 PEG_RXP6 PEG_RXN5 PEG_RXP5 PEG_RXN4 PEG_RXP4 PEG_RXN3 PEG_RXP3 PEG_RXN2 PEG_RXP2 PEG_RXN1 PEG_RXP1 PEG_RXN0 PEG_RXP0

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG
3 MXM_CLKREQ#
7,22,33,36,38,42,43 PLT_RST1#
R456 Do Not Stuff
C489 SB DIS Do Not Stuff
PLT_RST1#_MXM
21,29,39 ACZ_SYNC
21,39 ACZ_BITCLK
25,42,45 SMBD_Therm
R452 Do Not Stuff
SMBD_MXM
25,42,45 SMBC_Therm
R453 Do Not Stuff
SMBC_MXM
49 MXM_THER

19 CRT_HSYNC
19 CRT_VSYNC
19 CRT_DDCCLK
19 CRT_DDCDATA
21 ACZ_SDIN2
21,29,39 ACZ_SDATAOUT

C/BAT_DET
R618 Do Not Stuff DIS
3D3V_S0
SB

G72_TXACLK- 17
G72_TXACLK+ 17
G72_TXAOUT2- 17
G72_TXAOUT2+ 17
G72_TXAOUT1- 17
G72_TXAOUT1+ 17
G72_TXAOUT0- 17
G72_TXAOUT0+ 17
LCD_EDID_DAT 17
LCD_EDID_CLK 17
LCDVDD_ON 17
BLON_IN 42
TMDS_DAT 45
TMDS_CLK 45
2D5V_S0
R412 Do Not Stuff
3D3V_S0
C156 DIS Do Not Stuff
C441 DY Do Not Stuff
MXM1 Do Not Stuff
MH2
TMDS_TX0+ 45
TMDS_TX0- 45
TMDS_TX1+ 45
TMDS_TX1- 45
TMDS_TX2+ 45
TMDS_TX2- 45
TMDS_TXC+ 45
TMDS_TXC- 45
HDMI_HPD_1 45

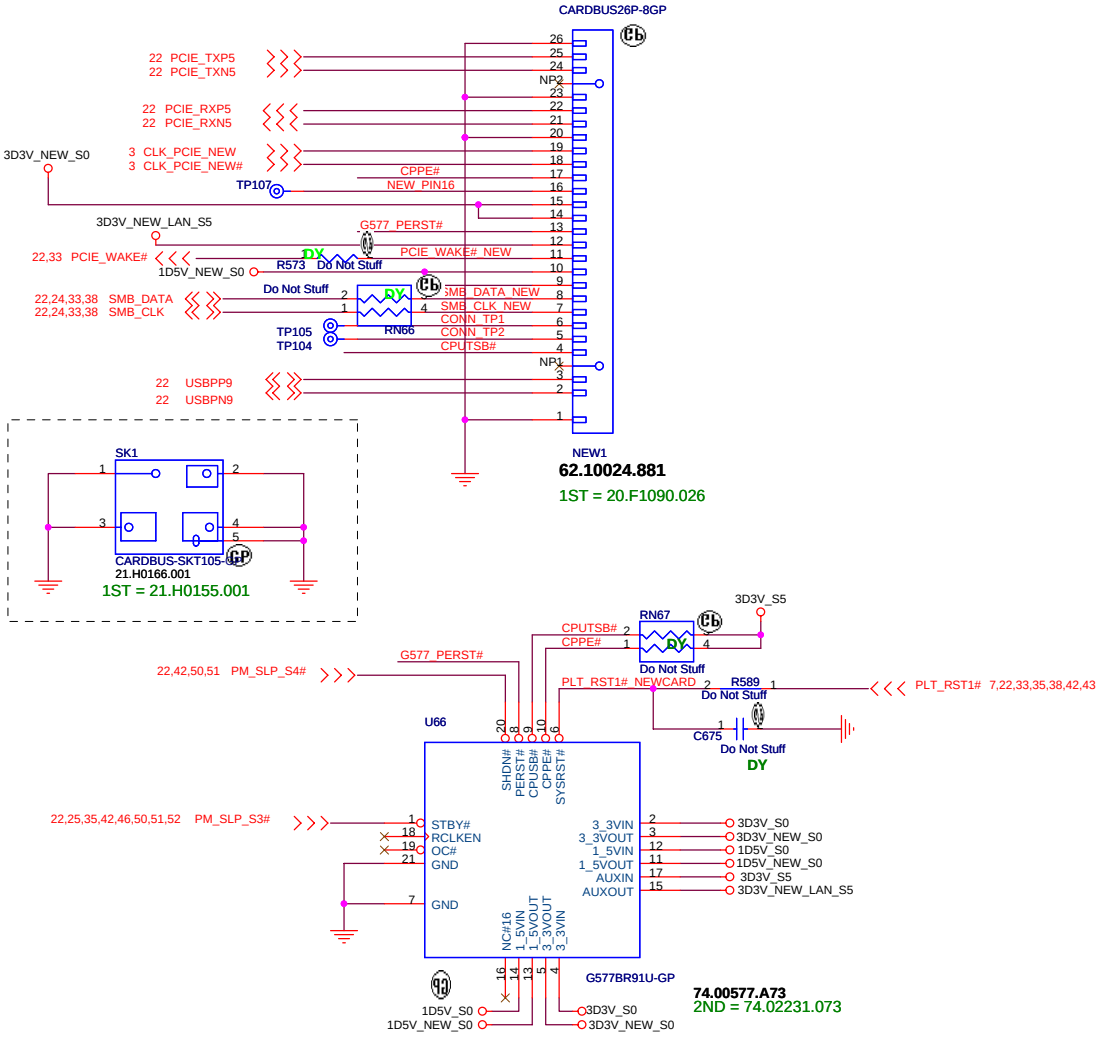
970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

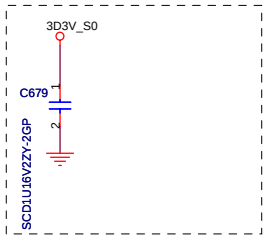
Title: Graphic MXM CONN
Size: A3 | Document Number: Homa | Rev: -1
Date: Thursday, April 03, 2008 | Sheet 35 of 57

# NEWCARD Connector

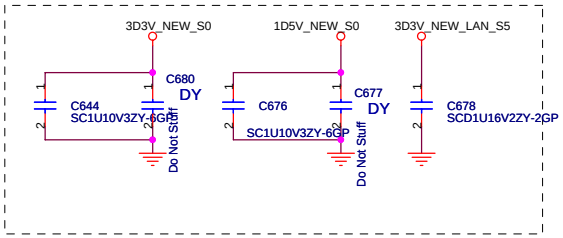
Reserve the symbol
for bottom side
connector




Place them Near to Chip




Place them Near to Connector

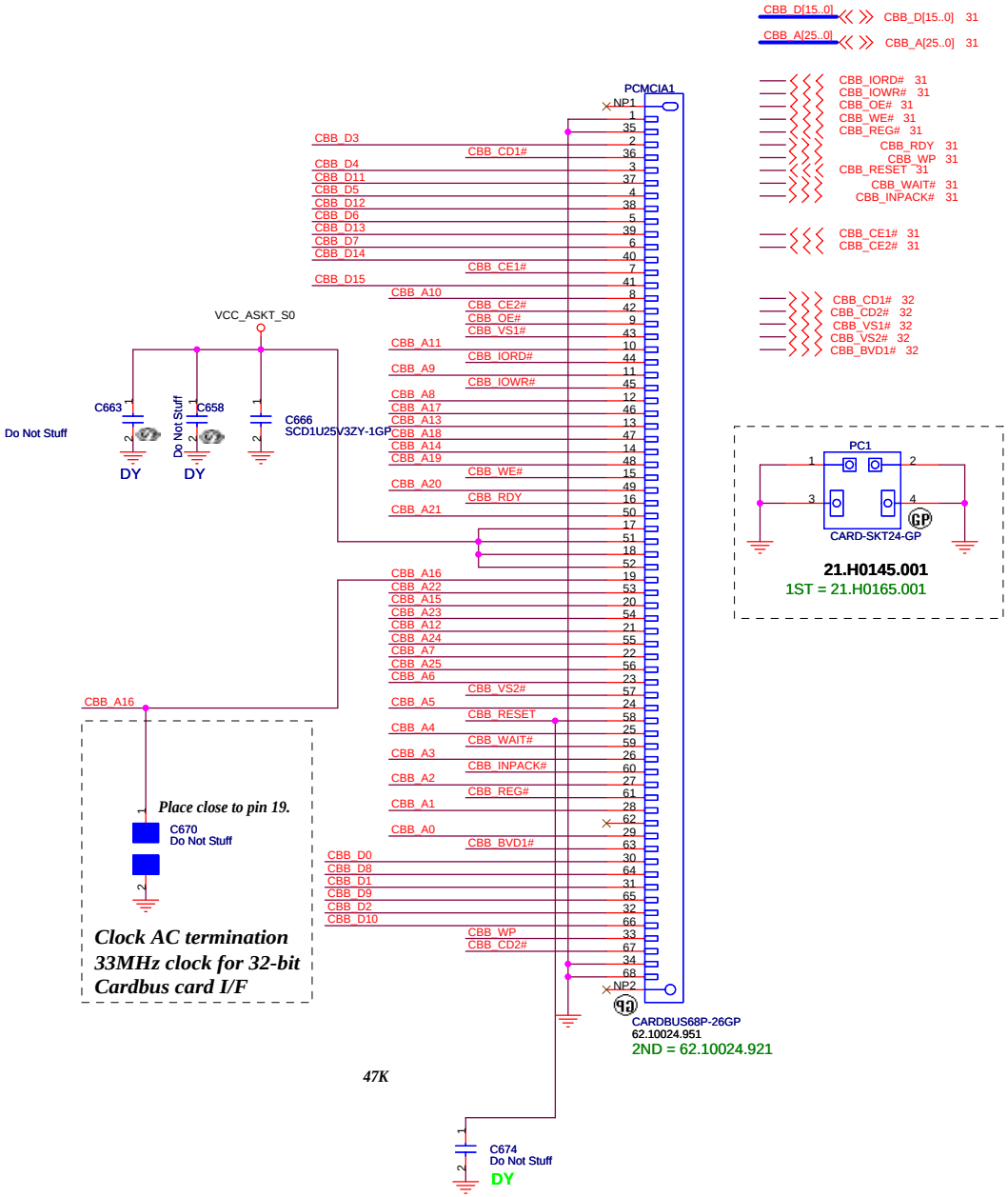



970

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | **NEW CARD** | |
| Size | Document Number<br>**Homa** | Rev<br>-1 |
| Date: Thursday, April 03, 2008 | Sheet 36 of 57 | |

# PCMCIA Socket

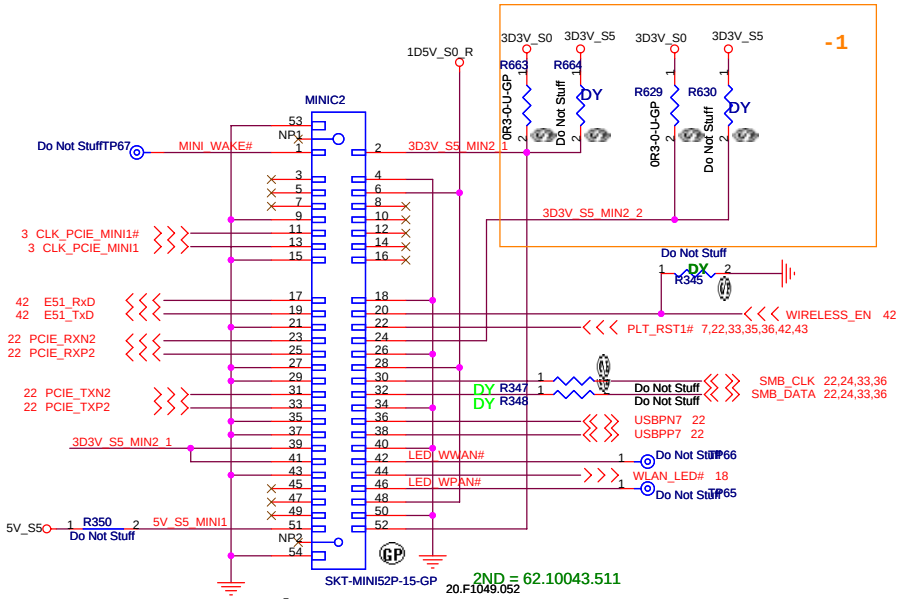
## Cardbus I/F




970

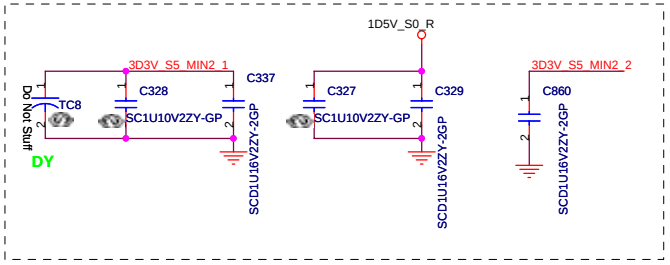
| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***PCMCIA*** | |
| Size<br>A3 | Document Number<br>**Homa** | Rev<br>**-1** |
| Date: Thursday, April 03, 2008 | Sheet 37 of 57 | |

# Mini Card Connector(WLAN)

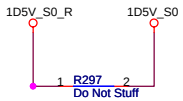



2ND = 62.10043.511

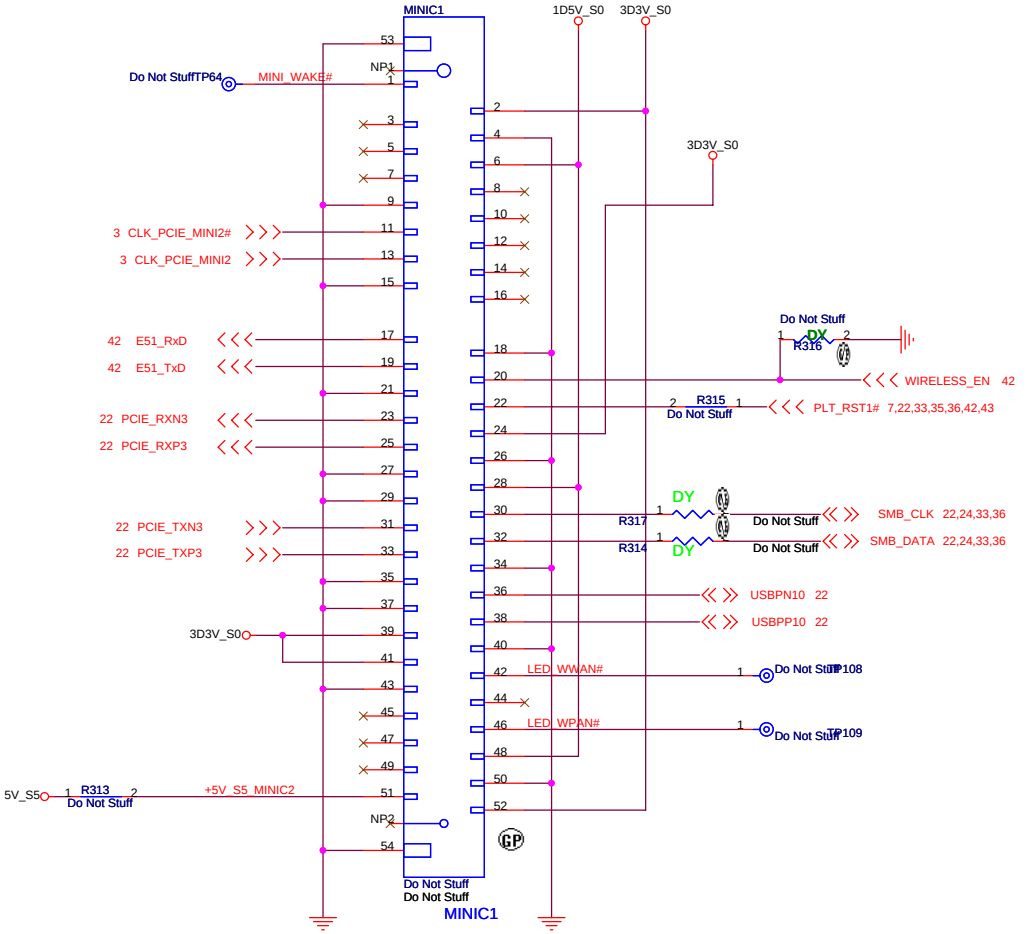
Place near MINIC2




Vo(cal.)=1.5024V OCP>3.2A

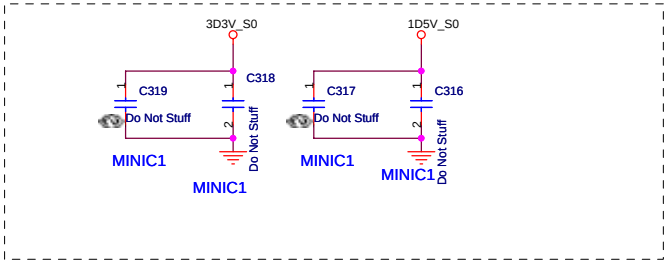



# Mini Card Connector




1ST = 20.F1084.052

Place near MINIC1





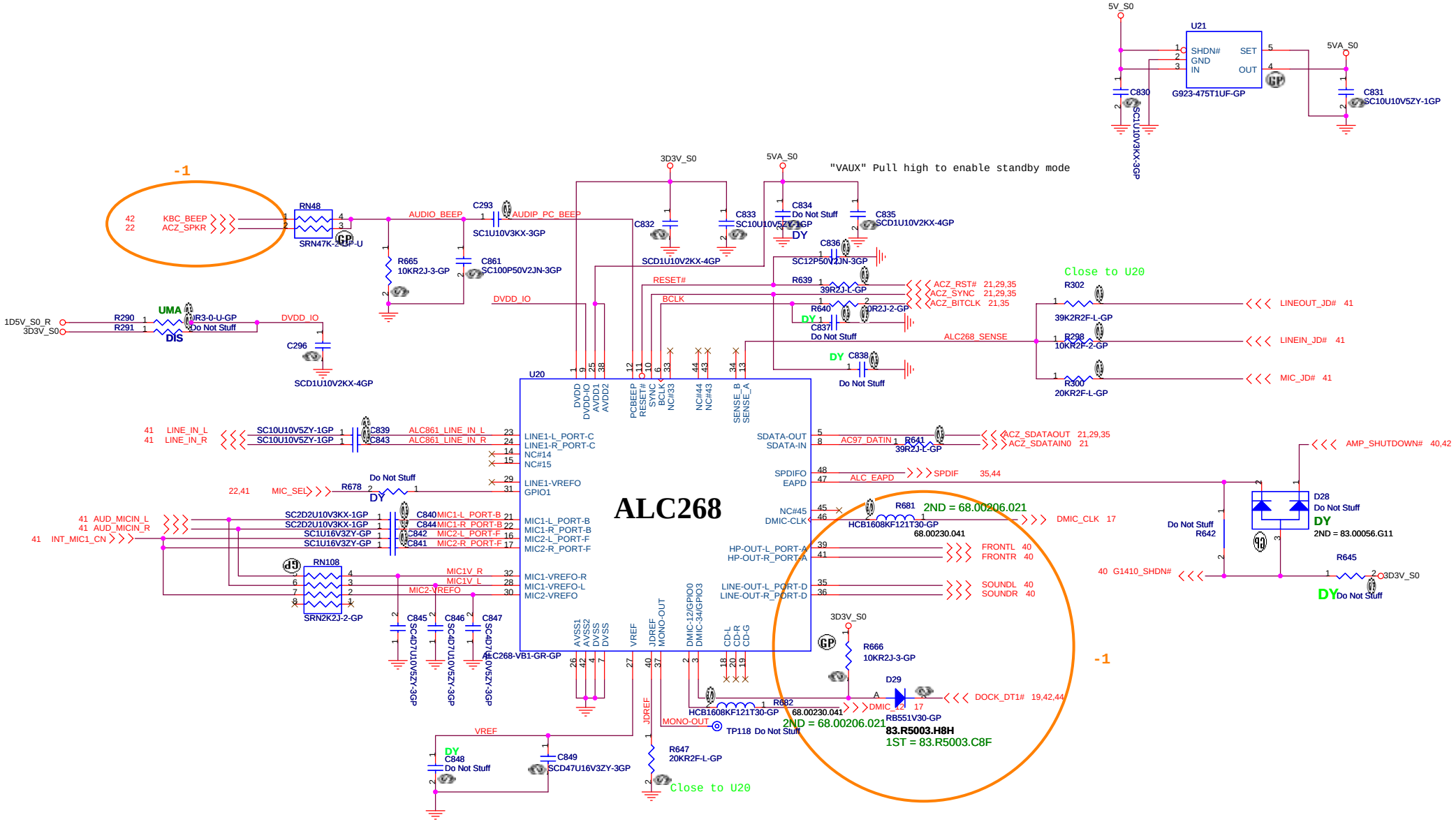

970

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

| Size | Document Number | Rev |
|---|---|---|
| A3 | Homa | -1 |

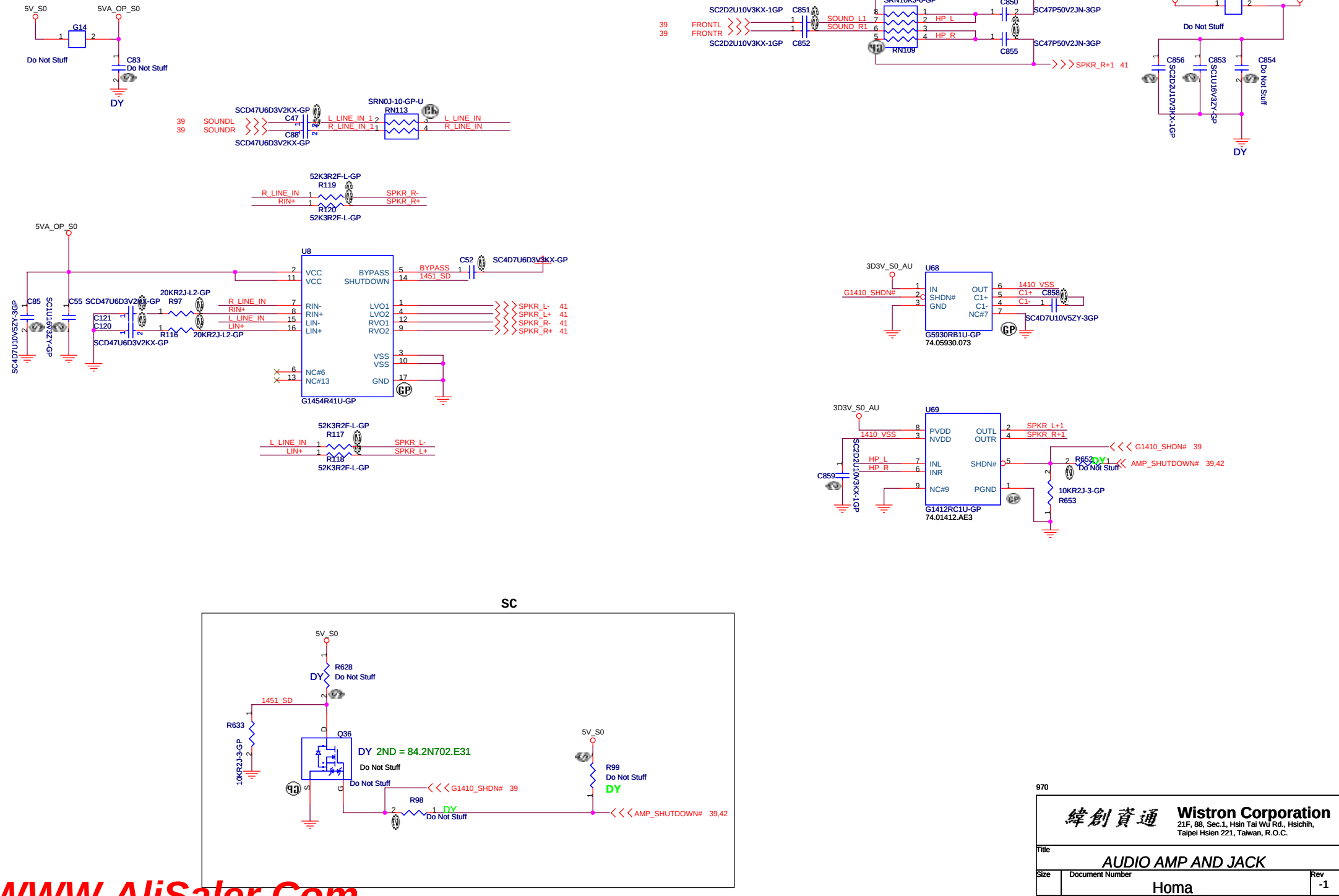
Date: Thursday, April 03, 2008 Sheet 38 of 57




970

| | |
|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | ***Azalia codec ALC268*** |
| Size A3 | Document Number **Homa** Rev **-1** |
| Date: Thursday, April 03, 2008 | Sheet 39 of 57 |

# AUDIO OP AMPLIFIER




970

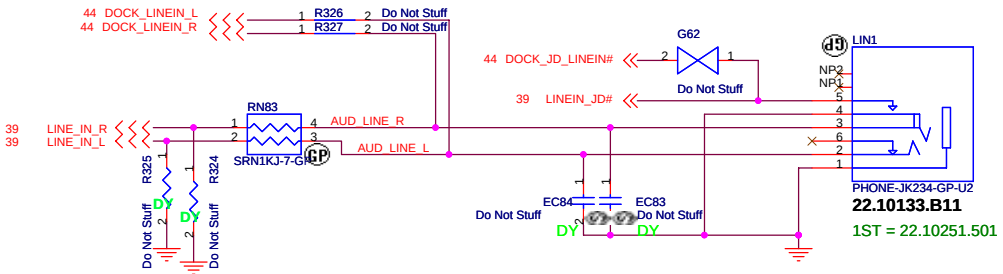
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

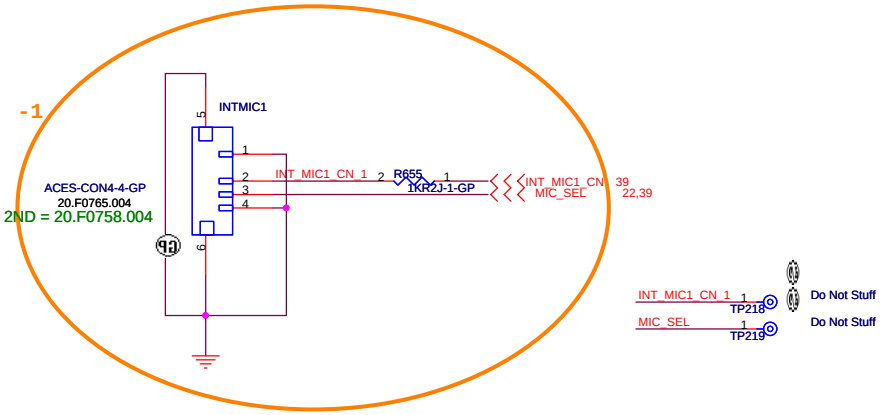
Title: *AUDIO AMP AND JACK*

| Size | Document Number | Rev |
|---|---|---|
| | Homa | -1 |

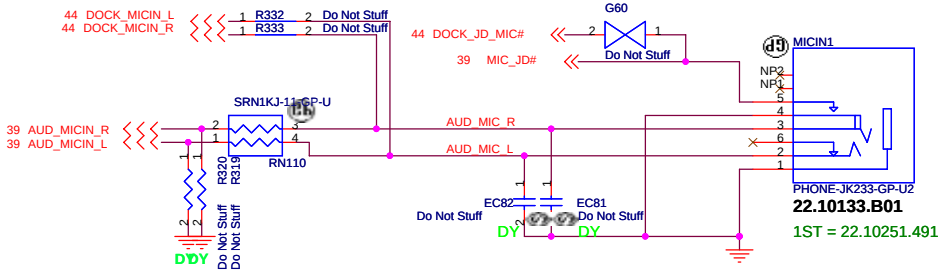
Date: Thursday, April 03, 2008 Sheet 40 of 57

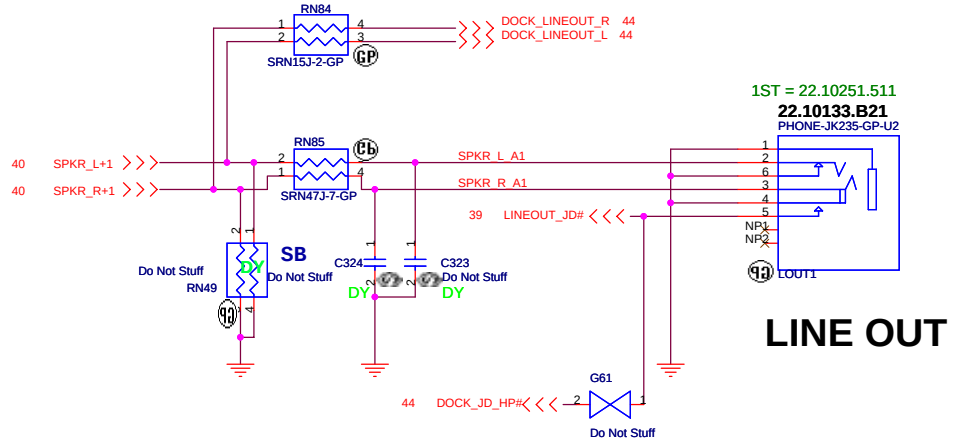
# LINE IN



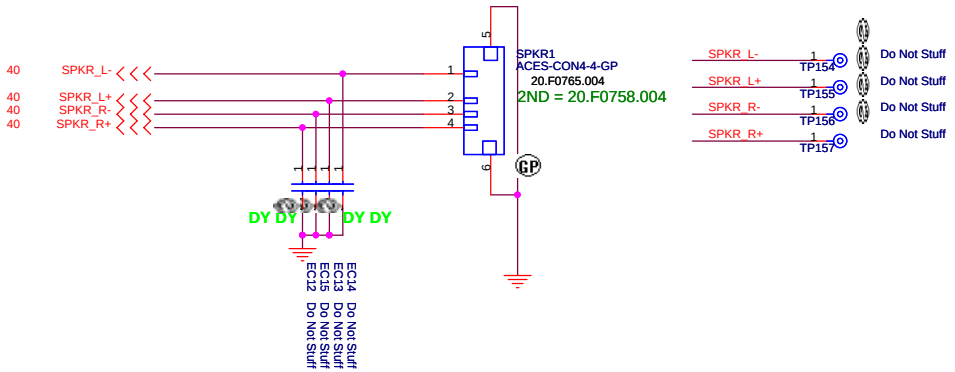

# MIC IN



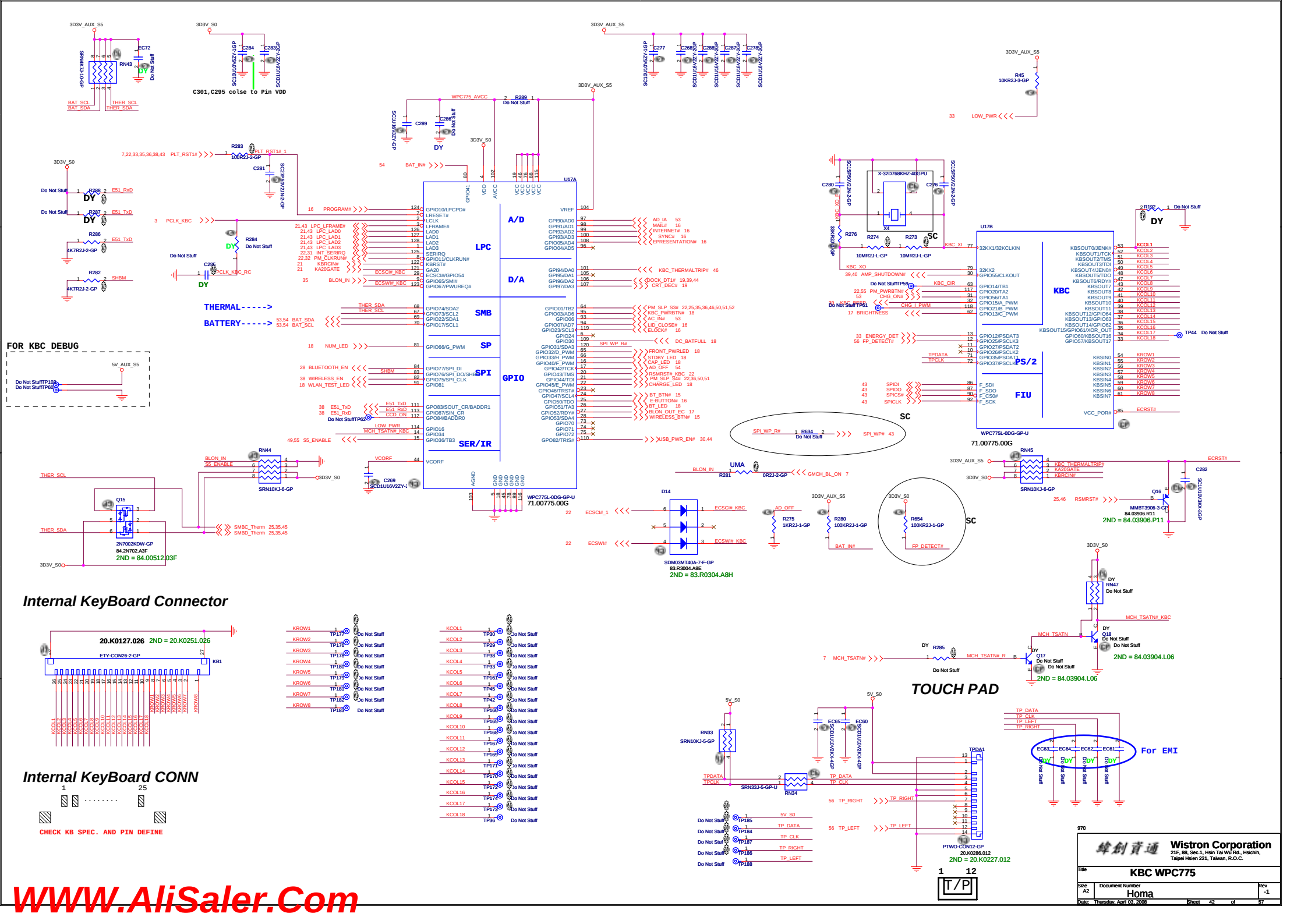

# LINE OUT

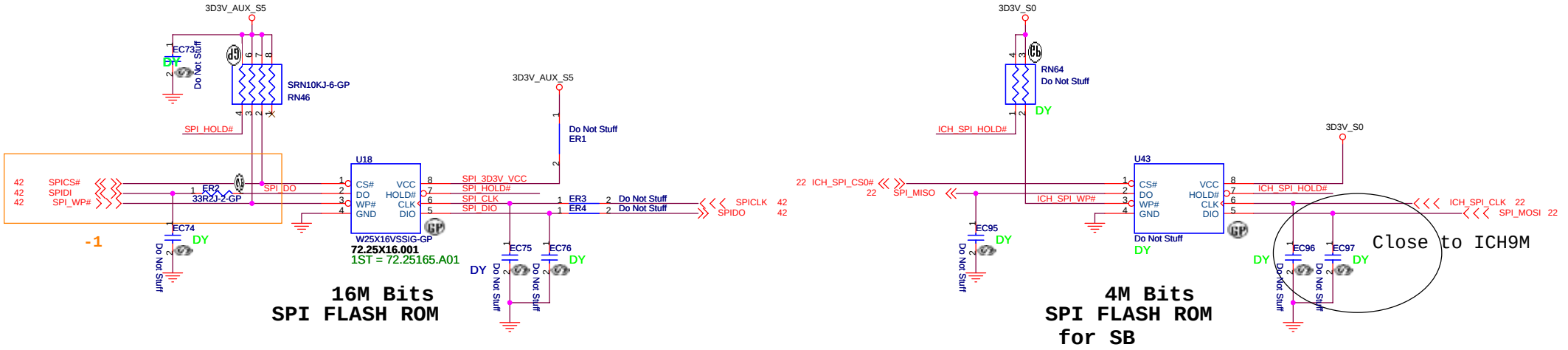
# Internal Speaker

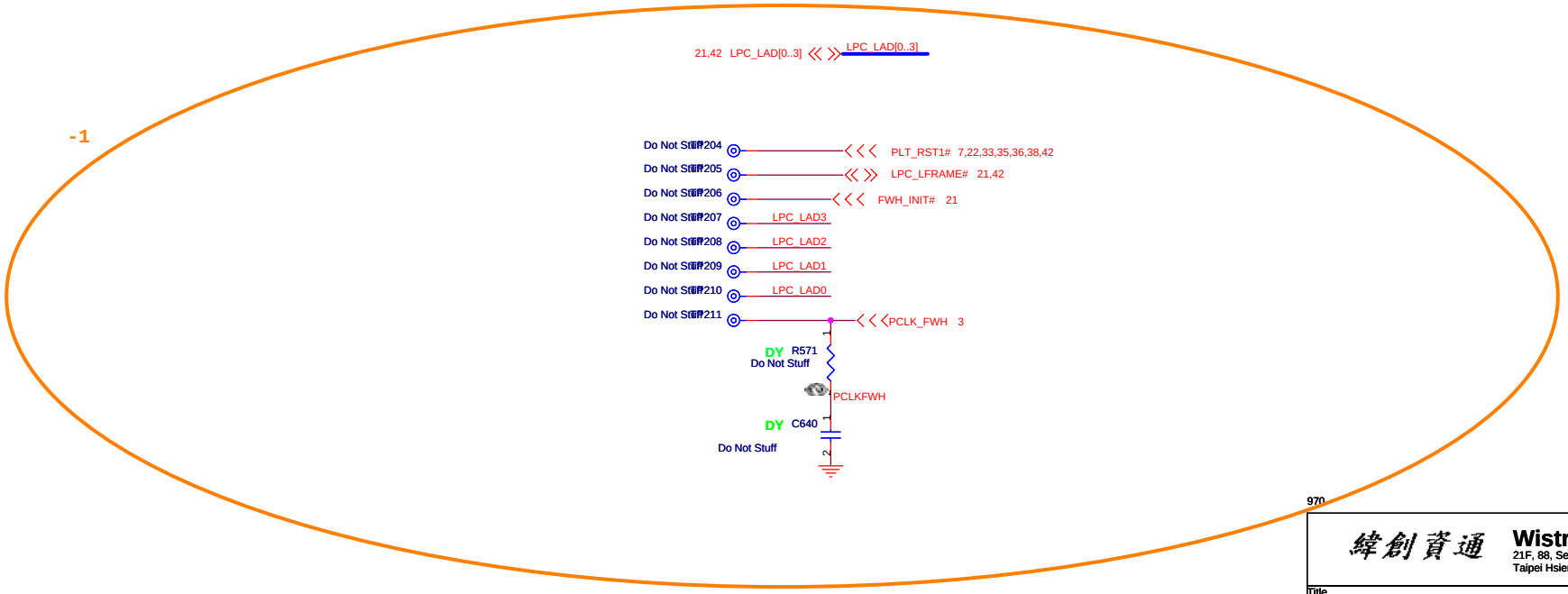



970

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | *AUDIO JACK* | |
| Size | Document Number<br>Homa | Rev<br>-1 |
| Date: Thursday, April 03, 2008 | Sheet 41 of 57 | |


FOR KBC DEBUG
THERMAL----->
BATTERY----->
U17A
WPC775L-0DG-GP-U
71.00775.00G
SC
UMA
PS/2
FIU
KBC
Internal KeyBoard Connector
20.K0127.026
2ND = 20.K0251.026
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
TOUCH PAD
For EMI
2ND = 20.K0227.012
Wistron Corporation
KBC WPC775
Homa
WWW.AliSaler.Com

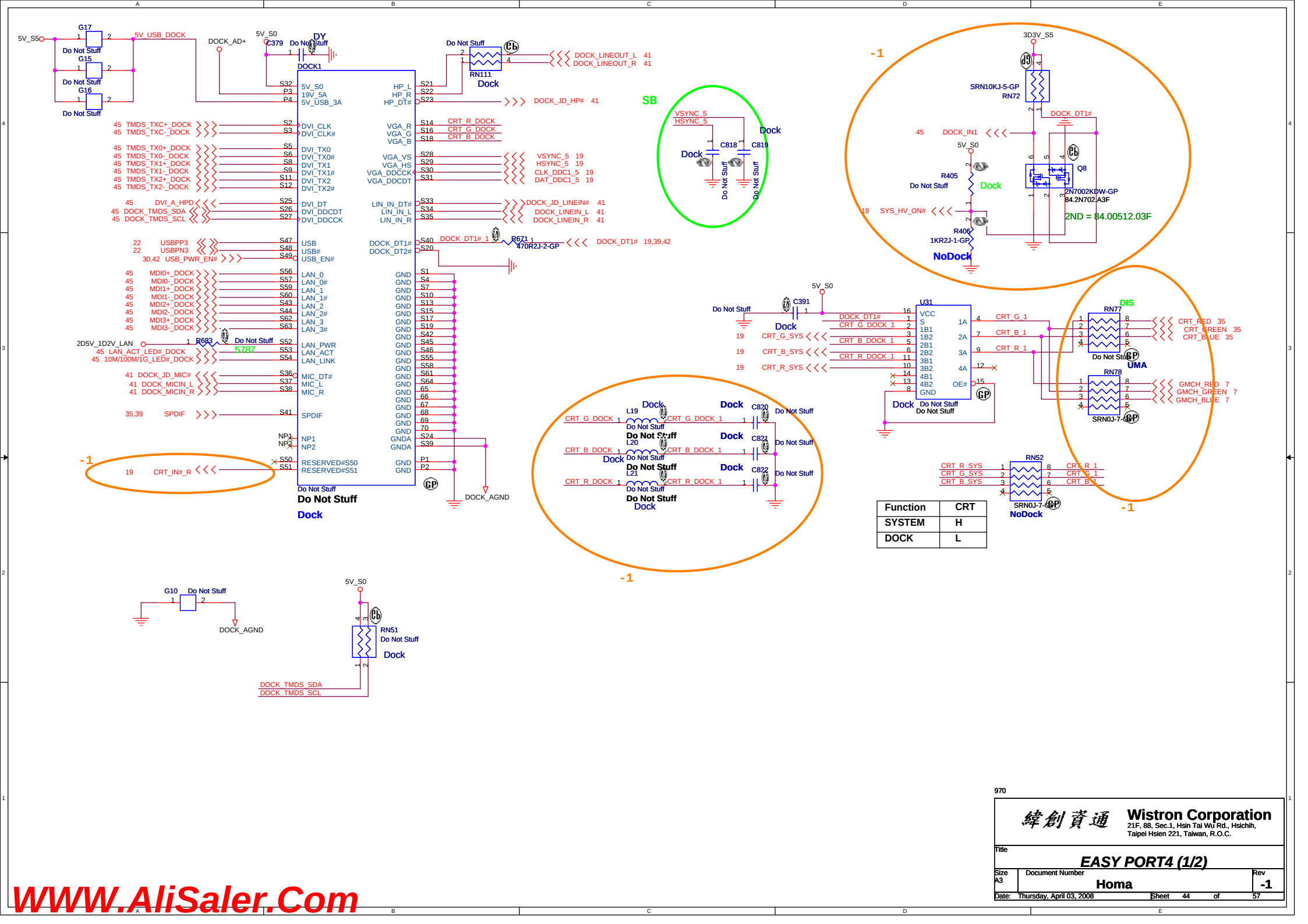


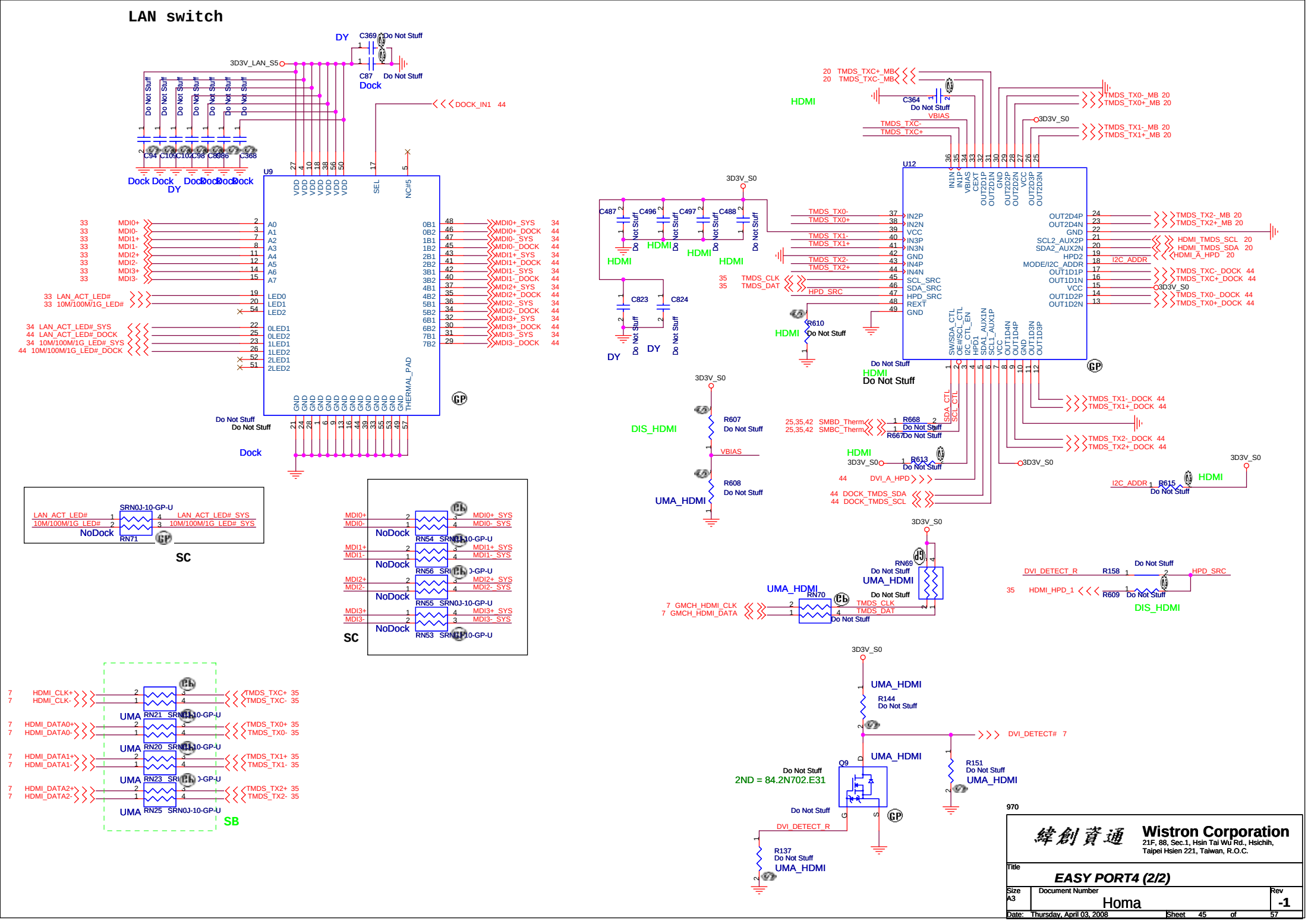

970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | BIOS | |
| Size | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 43 of 57 | |


G17
G15
G16
Do Not Stuff
5V_S5
5V_USB_DOCK
DOCK_AD+
5V_S0
C379
DY
DOCK1
RN111
Dock
DOCK_LINEOUT_L 41
DOCK_LINEOUT_R 41
DOCK_JD_HP# 41
SB
VSYNC_5
HSYNC_5
C818
C819
-1
3D3V_S5
SRN10KJ-5-GP
RN72
DOCK_DT1#
DOCK_IN1
R405
Q8
2N7002KDW-GP
84.2N702.A3F
SYS_HV_ON#
R406
1KR2J-1-GP
NoDock
2ND = 84.00512.03F
DVI_CLK
DVI_CLK#
DVI_TX0
DVI_TX0#
DVI_TX1
DVI_TX1#
DVI_TX2
DVI_TX2#
DVI_DT
DVI_DDCDT
DVI_DDCCK
VGA_R
VGA_G
VGA_B
VGA_VS
VGA_HS
VGA_DDCCK
VGA_DDCDT
LIN_IN_DT#
LIN_IN_L
LIN_IN_R
USB
USB#
USB_EN#
DOCK_DT1#
DOCK_DT2#
LAN_0
LAN_0#
LAN_1
LAN_1#
LAN_2
LAN_2#
LAN_3
LAN_3#
LAN_PWR
LAN_ACT
LAN_LINK
MIC_DT#
MIC_L
MIC_R
SPDIF
NP1
NP2
RESERVED#S50
RESERVED#S51
GND
GNDA
CRT_R_DOCK
CRT_G_DOCK
CRT_B_DOCK
VSYNC_5 19
HSYNC_5 19
CLK_DDC1_5 19
DAT_DDC1_5 19
DOCK_JD_LINEIN# 41
DOCK_LINEIN_L 41
DOCK_LINEIN_R 41
DOCK_DT1# 19,39,42
R671
470R2J-2-GP
R683
5787
2D5V_1D2V_LAN
LAN_ACT_LED#_DOCK
10M/100M/1G_LED#_DOCK
DOCK_JD_MIC#
DOCK_MICIN_L
DOCK_MICIN_R
CRT_IN#_R
DOCK_AGND
C391
U31
DOCK_DT1#
CRT_G_DOCK_1
CRT_B_DOCK_1
CRT_R_DOCK_1
CRT_G_SYS
CRT_B_SYS
CRT_R_SYS
CRT_G_1
CRT_B_1
CRT_R_1
DIS
RN77
RN78
UMA
CRT_RED 35
CRT_GREEN 35
CRT_BLUE 35
GMCH_RED 7
GMCH_GREEN 7
GMCH_BLUE 7
SRN0J-7-GP
RN52
L19
L20
L21
C820
C821
C822
G10
RN51
DOCK_TMDS_SDA
DOCK_TMDS_SCL
Function
CRT
SYSTEM
H
DOCK
L
970
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EASY PORT4 (1/2)
Size
A3
Document Number
Homa
Rev
-1
Date: Thursday, April 03, 2008
Sheet 44 of 57
WWW.AliSaler.Com

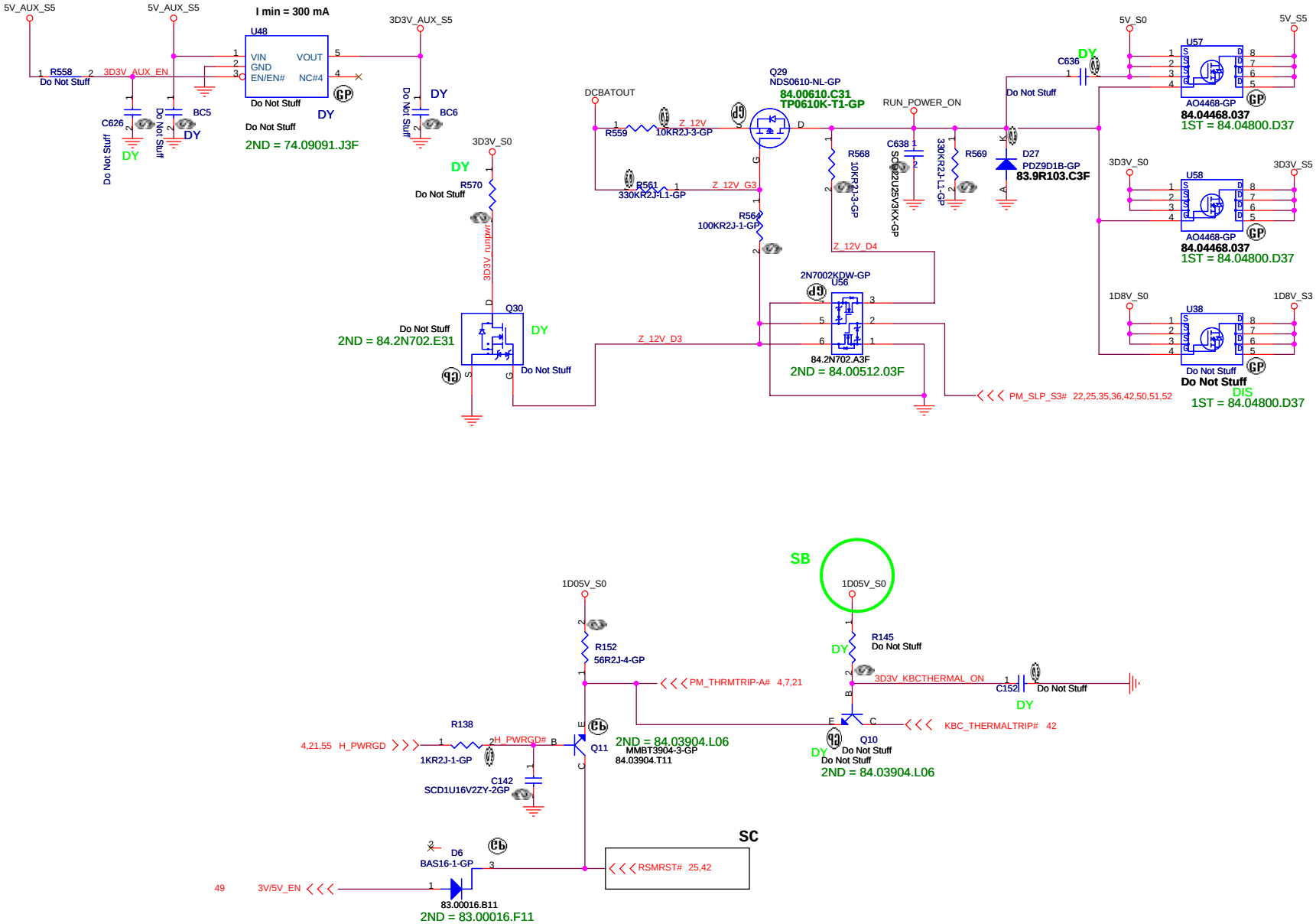
# LAN switch




| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***EASY PORT4 (2/2)*** | |
| Size A3 | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 45 of 57 | |

# Aux Power 3D3V_AUX_S5

# Run Power




970

| | | |
|---|---|---|
| 緯創資通 | Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | RUN POWER and 3D3V_AUX_S5 | |
| Size | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 46 of 57 | |

## CPU_CORE
## ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6266A
5V_S0
3D3V_S0

**VID Setting**
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

**Input Signal**
EN (I / 3.3V)

**Voltage Sense**
VSEN(I / Vcore)
RGND(I / Vcore)

**Input Power**
VCC(I)
VCC(I)
VCC(I)

**Output Signal**
PGOOD

VGATE_PWRGD

**Output Power**
VCC_CORE_PWR(O)

VCC_CORE(Imax=38A)

## TPS51125
## 5V/3D3V

DCBATOUT_51125

PM_SLP_S4#

ALW_PWRGD_3V_5V

**Input Power**
VIN

**Input Signal**
EN0

**Output Signal**
PGOOD

**Output Power**
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)

## RT9018A
## 1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN

1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

## RT9026
## 0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5

VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

## GFX_CORE
## ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

**VID Setting**
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

**Input Power**
VDD
VIN

**Input Signal**
VR_ON

**Voltage Sense**
VSEN(I / Vcore)
RGND(I / Vcore)

**Output Signal**
PGOOD

CPUCORE_ON

**Output Power**
VGFXCORE (O)

VCC_GFXCORE(5.5A)

## G9131
## 2D5V_S0

3D3V_S0

INPUT
OUT

2D5V_S0(0.3A)

## TPS51124
## 1D8V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

**Input Power**
VDD
VCC

**Input Signal**
EN1
EN2

**Output Signal**
PGOOD1
PGOOD2

**Output Power**
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

## Adapter

AD_OFF
AD_JK
5V_AUX_S5

**Input Signal**
(I)

**Input Power**
VCC(I)
VCC(I)

**Output Signal**
(O)

**Output Power**
VCC(O)

AD_IN#
AD+

## Charger BQ24750

CHG_ON#
24750_CELLS

AD+

**Input Signal**
CHGEN#
CELLS

**Input Power**
ACN

**Output Signal**
ACGOOD#
SRSET

**Output Power**
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

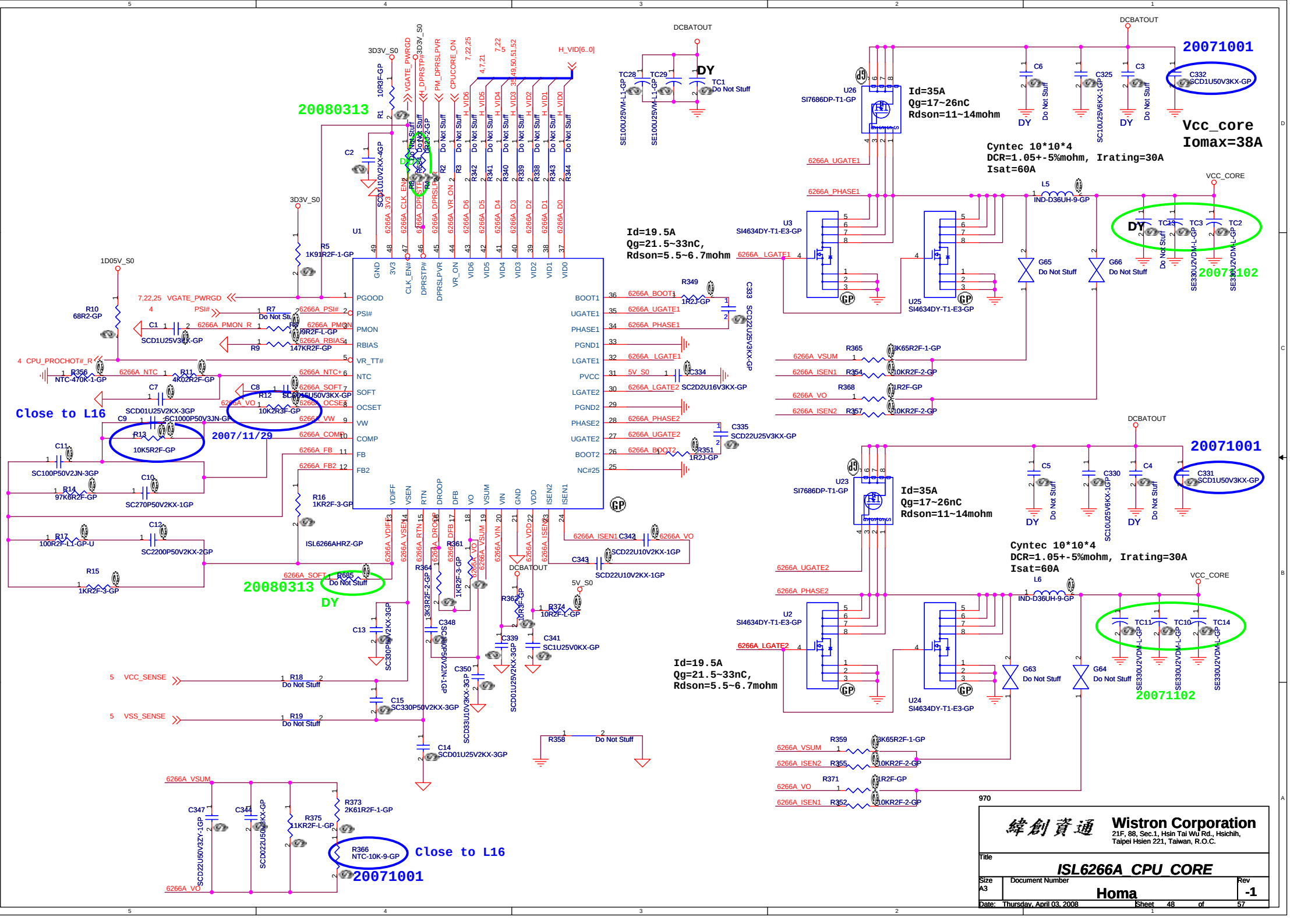
970

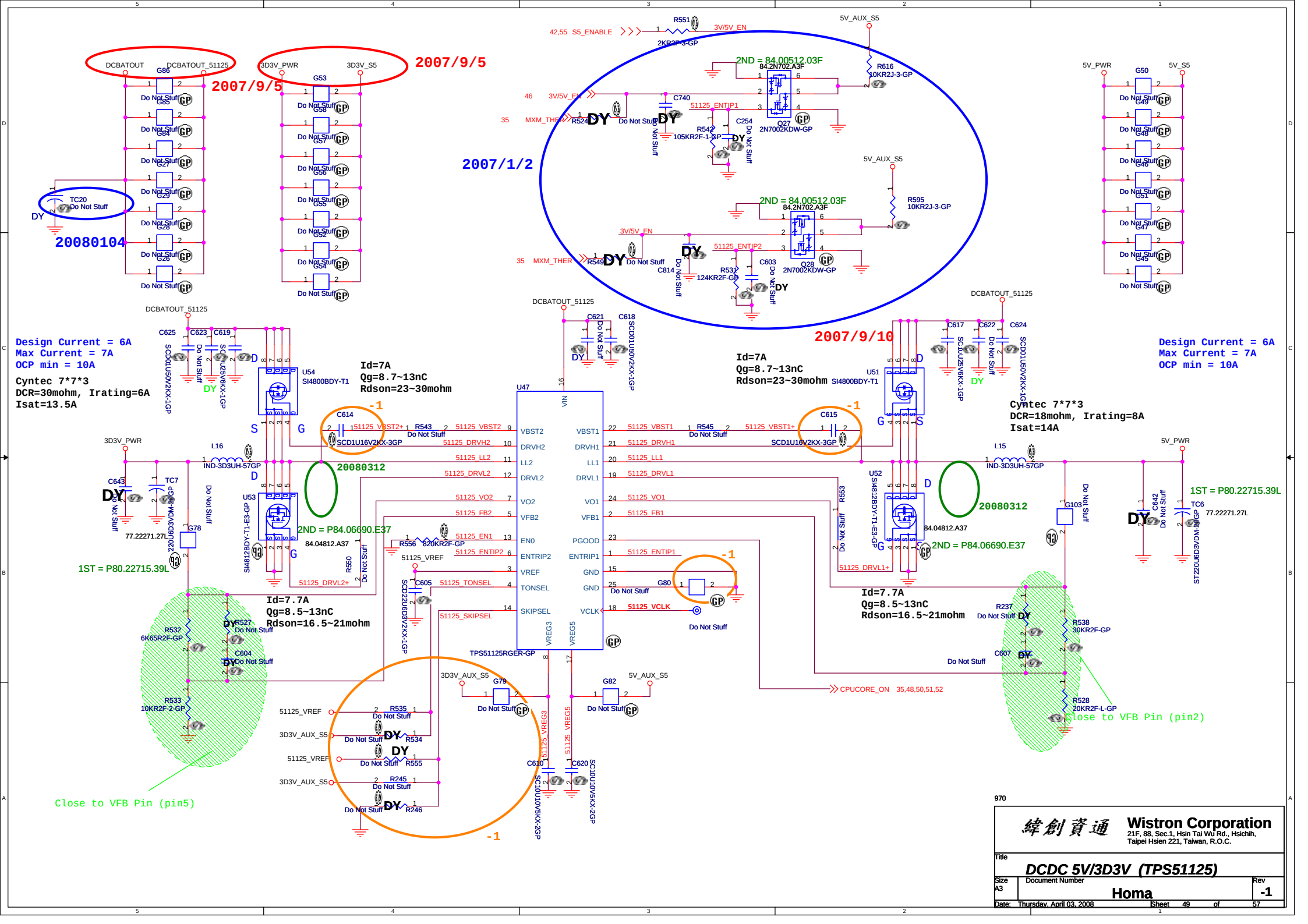

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: **Power Sequence Logic**

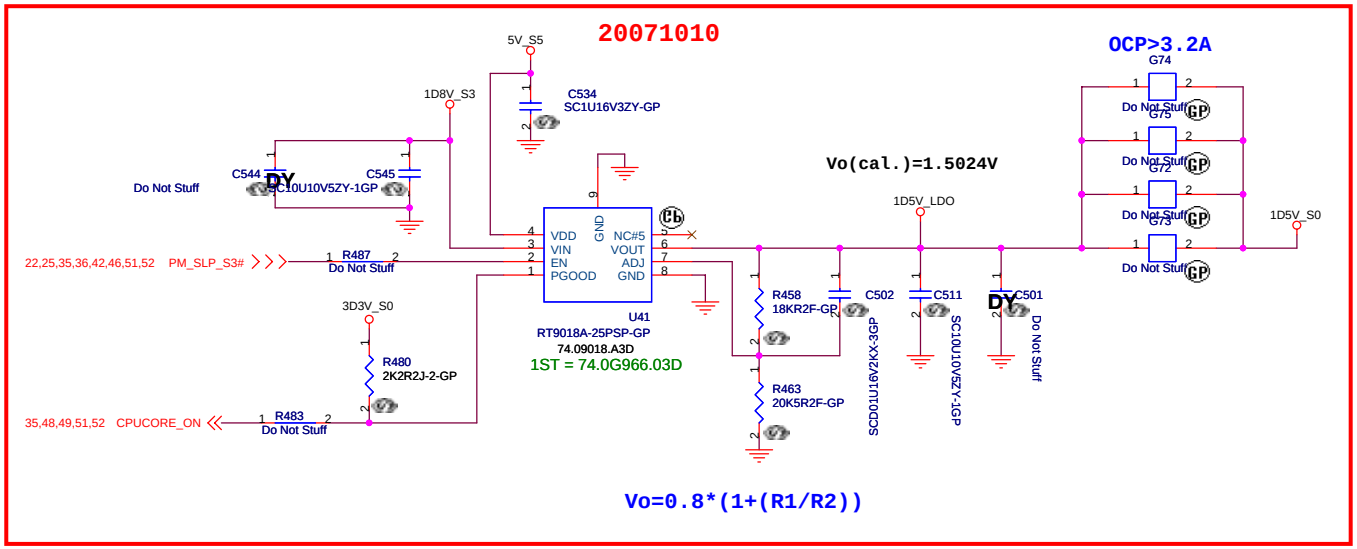
Size: B | Document Number: Homa | Rev: -1

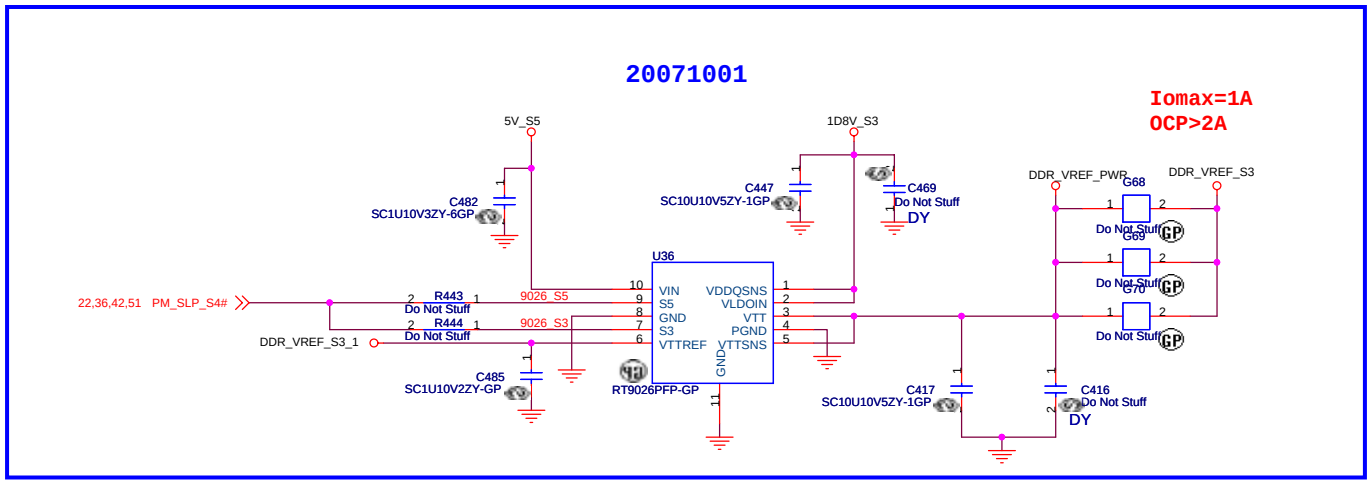
Date: Thursday, April 03, 2008 | Sheet 47 of 57


20080313
Close to L16
2007/11/29
20080313
DY
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Vcc_core
Iomax=38A
20071001
20071102
Close to L16
20071001
970
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size A3
Document Number
Homa
Rev -1
Date: Thursday, April 03, 2008
Sheet 48 of 57

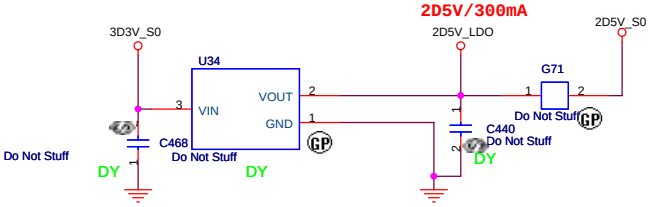

2007/9/5
2007/9/5
2007/1/2
2007/9/10
20080104
20080312
20080312
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
2ND = 84.00512.03F
2ND = P84.06690.E37
2ND = P84.06690.E37
1ST = P80.22715.39L
1ST = P80.22715.39L
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
TPS51125RGER-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Homa
Date: Thursday, April 03, 2008
Sheet 49 of 57

## 1D5V_S0
## Iomax=2.5A



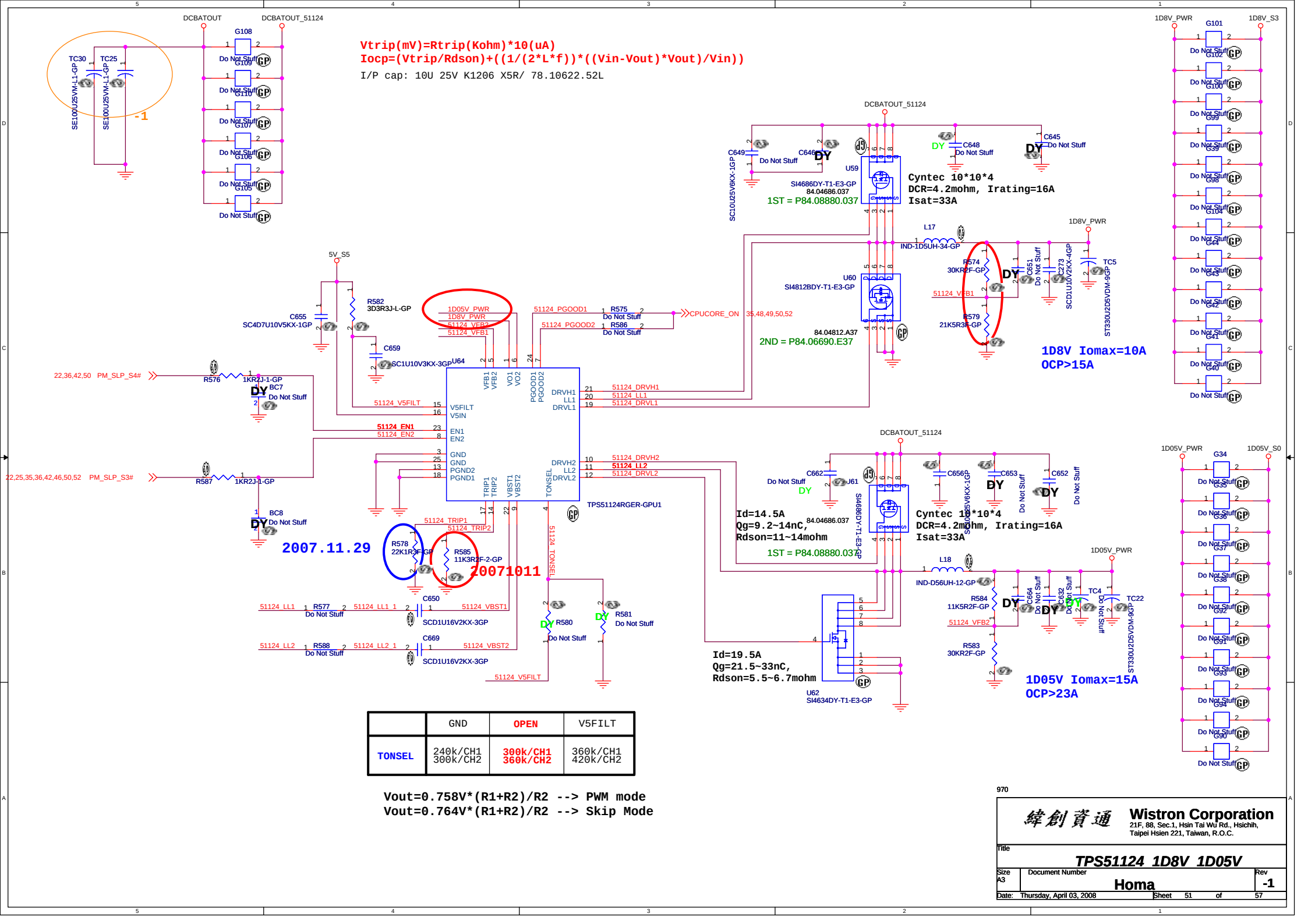




## 2D5V_S0
## Iomax=0.3A




970

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: *1D5V & 0D9V & 2D5V* | | |
| Size: A3 | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 50 of 57 | |




| | GND | OPEN | V5FILT |
|---|---|---|---|
| TONSEL | 240k/CH1<br>300k/CH2 | 300k/CH1<br>360k/CH2 | 360k/CH1<br>420k/CH2 |

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

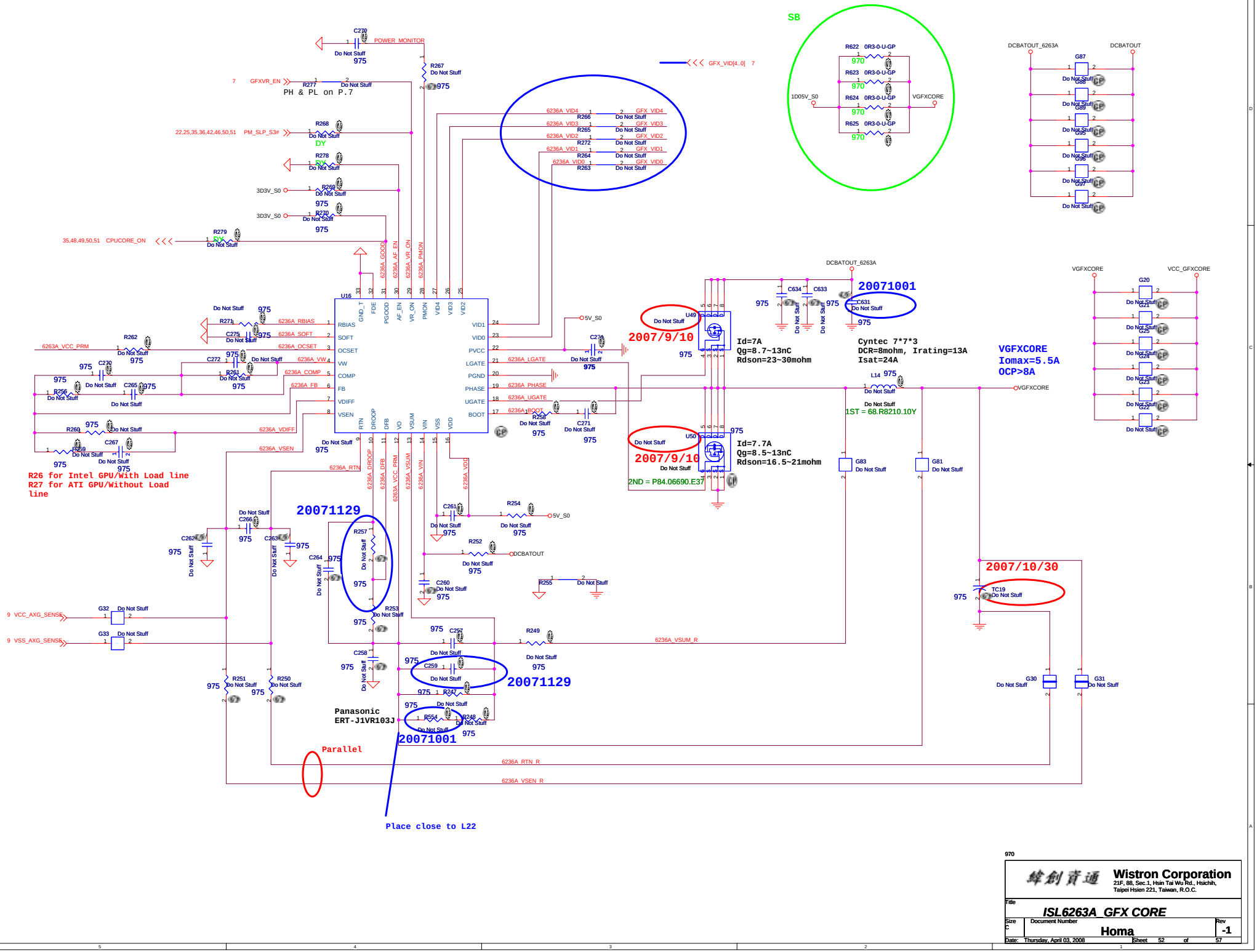
970

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V 1D05V

Size: A3 | Document Number: Homa | Rev: -1

Date: Thursday, April 03, 2008 | Sheet 51 of 57



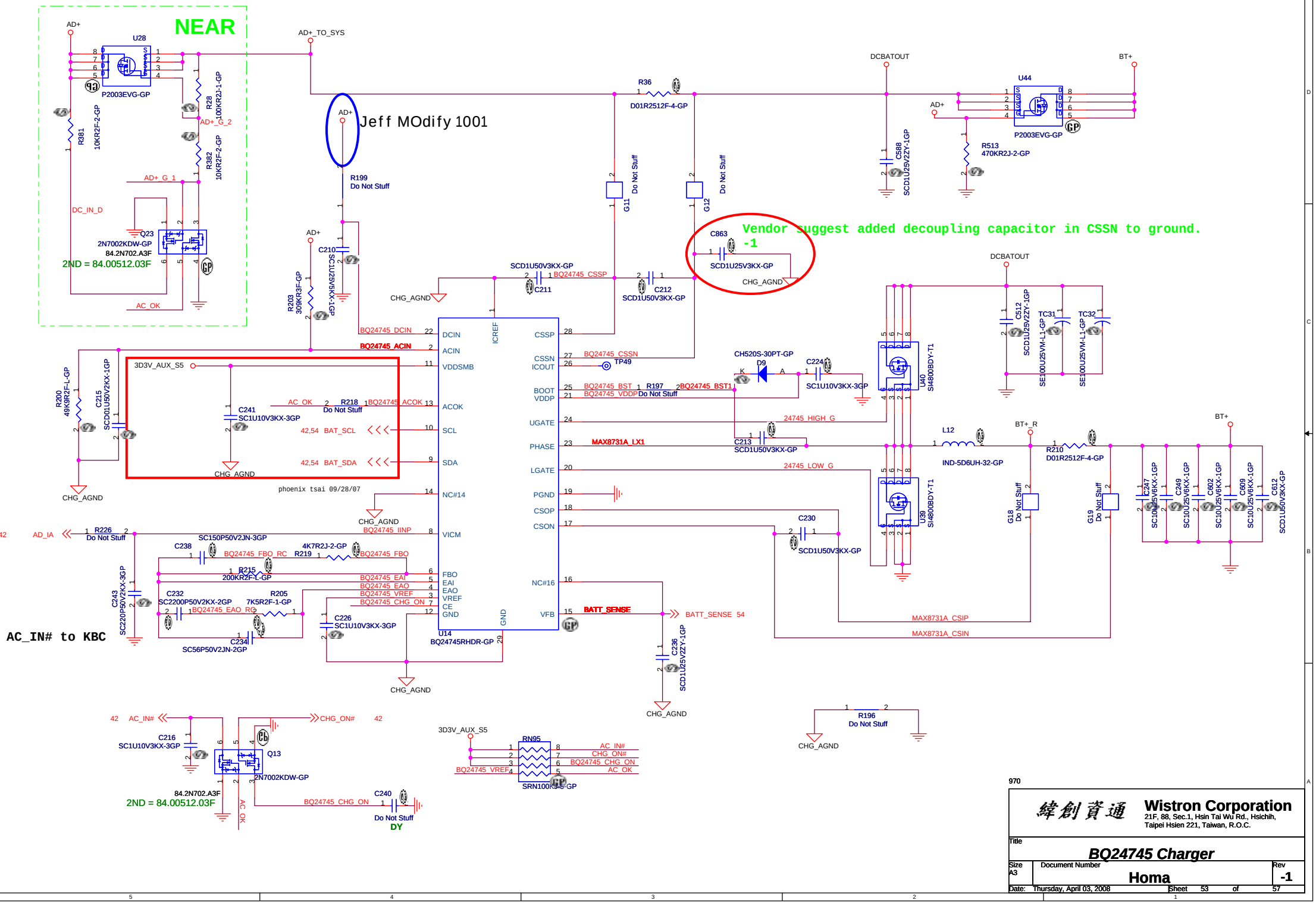

970


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: ISL6263A_GFX CORE

Size: C | Document Number: Homa | Rev: -1

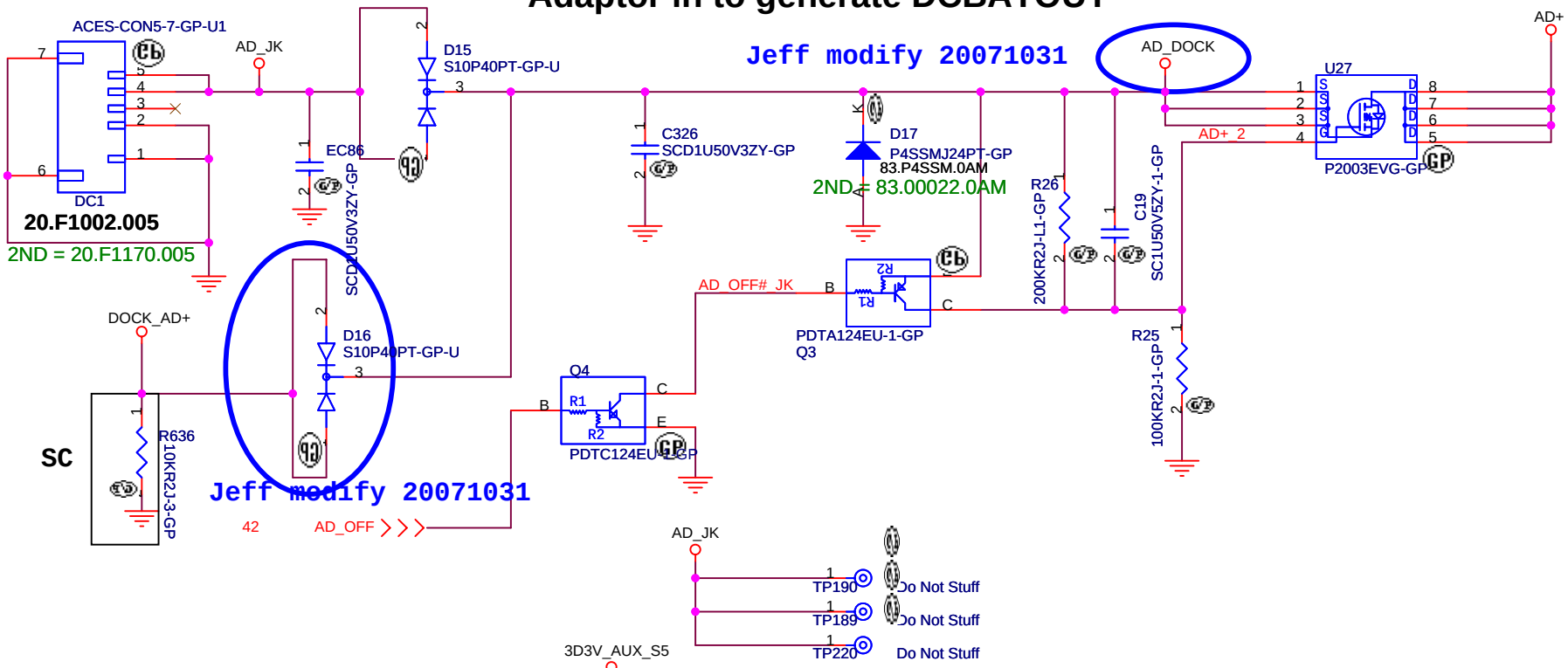
Date: Thursday, April 03, 2008 | Sheet 52 of 57



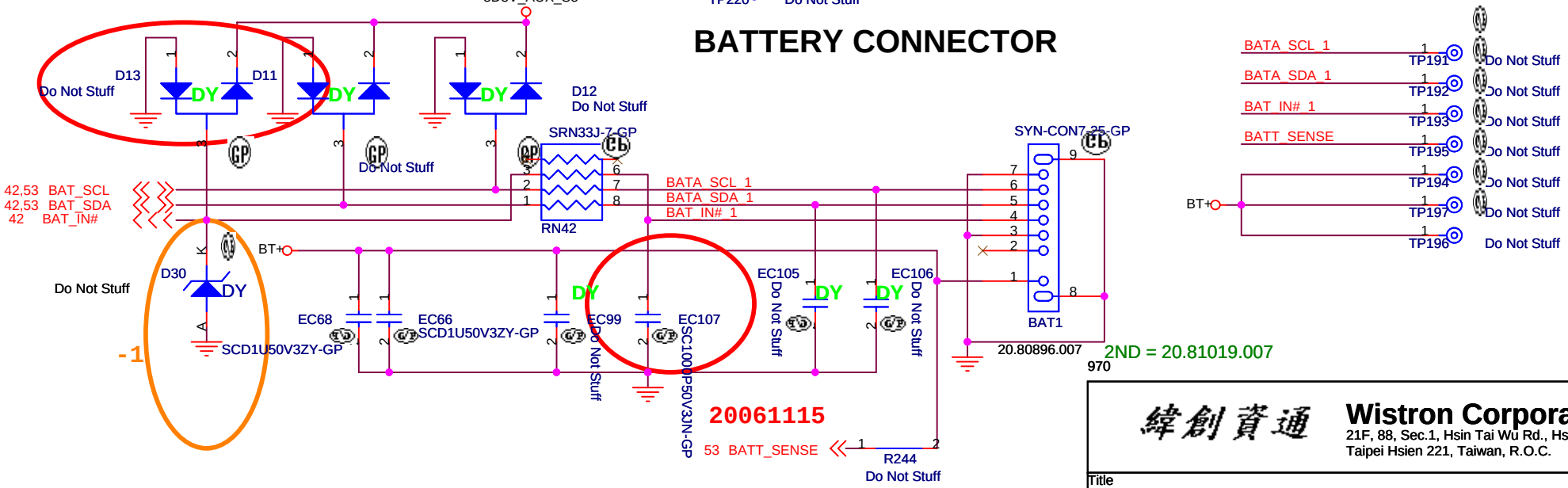

970

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | **BQ24745 Charger** | |
| Size: A3 | Document Number: **Homa** | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 53 of 57 | |

# Adaptor in to generate DCBATOUT



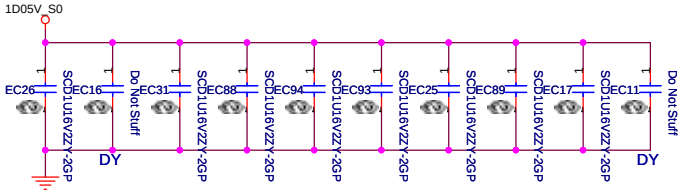

## BATTERY CONNECTOR

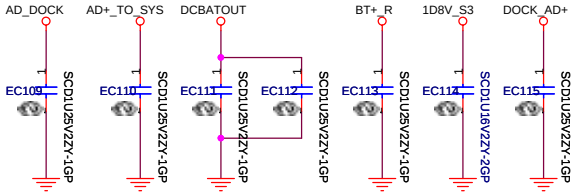




緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


| | | |
|---|---|---|
| Title | AD/BATT CONN | |
| Size | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 54 of 57 | |




## Check test point

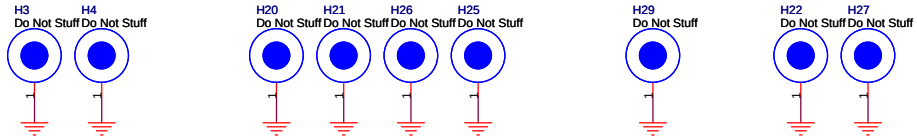

**Test Point放在Dimm Door打開可量測處**

SC

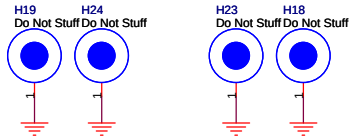
SC

## Stand off Location

**34.42Y01.031**

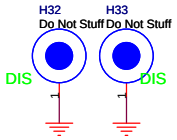



**34.4G502.021**

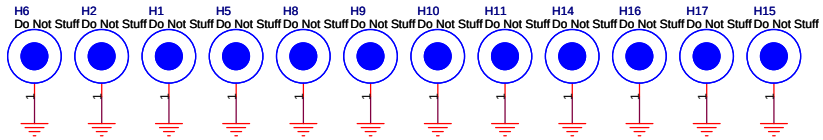



**34.4Z402.011**


**34.4Z401.011**

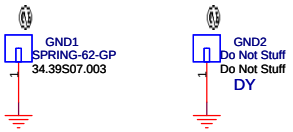



**DELETE MXM**
**STAND-OFF**
**H7;H28;H30;H31**

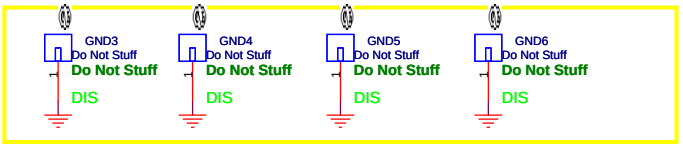


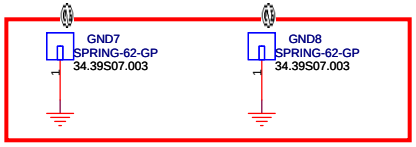

## SPRING ON BOTTOM

**DIMM** **Heat Sink**




## MXM SPRING -1 20080307




970

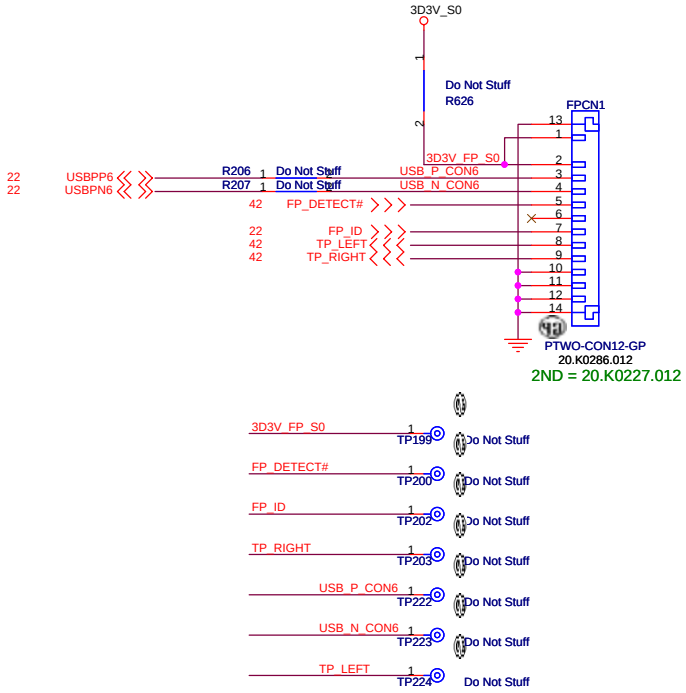
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

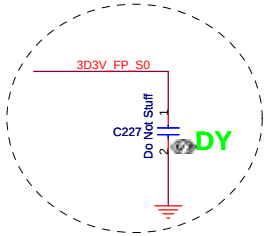
Title: ***EMI/Spring/Boss***

Size | Document Number: **Homa** | Rev: -1

Date: Thursday, April 03, 2008 | Sheet 55 of 57

# Finger printer




For EMI




970

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: FP | | |
| Size: A3 | Document Number: Homa | Rev: -1 |
| Date: Thursday, April 03, 2008 | Sheet 56 of 57 | |

## SA --> SB

1.page25,Change Q24 and Q5 Pin_C and Pin_E net, Swap H_THERMDA and H_THERMDC(only close to C95)
2.page46,Change R145_Pin1 pull hige power to 1D05V_S0
3.page42,Add the Net let link U17_Pin101 and RN45_Pin3
4.page16,SWITCHCN1 pin12 connect to 3D3V_AUX_S5 and pin 11 connect to LID_CLOSE#
5.page20,HDMI1 change to 62.10078.171
6.page44,DOCK1 pin51 connect to CRT_DEC#
7.page53,R214 change to connect BQ24745_VREF as charger modify
8.page26,change ODD1 to 22.10300.141
9.page45,change U12 to PS8122QFN48G-GP and add some components
10.page44,Del U5
11.page20,Del U11,U42,Q9….
12.del G1~G8
13.page45,R614 changed to “DOCK_DT1#” and U12 output port1 and port2 swap,RN68 pin1&2 change to KBC SMBUS,
RN69 pin3&4 change to connect”3D3V_S0”,R615 change to 4K7R2F-GP
14.page49,change Q27&Q28 to 2N7002SPT ,add R595 R616
15.page48,change R12 to 10K2R3F-GP ,R13 to 16K5R2F-1-GP
16.page51,R578 change to 22K1R3-GP
17.page52,R257 change to 2K87R2F-1-GP ,C259 change to SCD033U50V
18.page40,change U8 to G1454R41U-GP
19.page42,Del R29 R27 C20 EC5
20.page41,LID1 change to INTMIC1 and connect to “MIC_L_CN”&”MIC_R_CN”
21.page39,add R619 C815 R621 R620 C816 C817
22.page38,Del C355 C320
23.page56,Del F4  addR626
24.page3,R204 change to connect”3D3V_CLKPLL_S0”
25.page52,add R622~R625
26.page44,add C818~C822 and L19 L20 L21
27.page35,Del TP77~TP82 TP84 TP86 TP87 TP24 TP25 TP26 TP28,add R618 pull up to 3D3V_S0
28.page25,add R617 Q35  del R115
29.page30,change C600 to 4.7U10V
30.page45, swap U12 output port1&pot2
31.page48~52, change power GAPs to close GAPs
32.page49,L15 change to 1ND-3D3UH by power modify
33.page16,add R627 EC108
34.page45,add C823 C824   and R144 R151 Q9 R137

970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change list*

| Size | Document Number | Rev |
|---|---|---|
| A3 | Homa | -1 |

Date: Thursday, April 03, 2008 Sheet 57 of 57