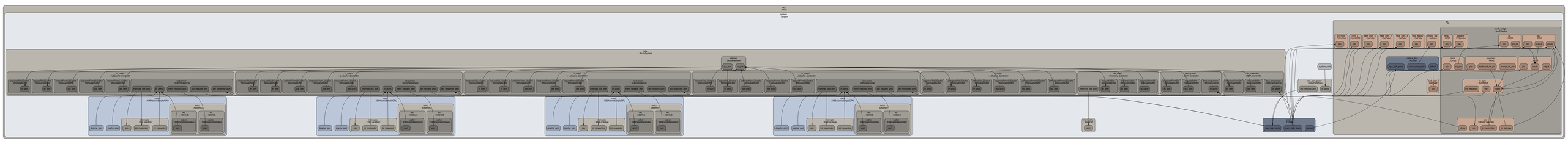

root
: Root

system
: System

pc
: Pc

south_bridge
: SouthBridge

pic1
: I8259

pic2
: I8259

cmos

: Cmos

dma1
: I8237

keyboard
: I8042

pit
: I8254

speaker
: PcSpeaker

io_apic
: I82094AA

ide
: X86IdeController

pci_host
: PcPciHost

com_1
: Uart8250

fake_com_2
: IsaFake

fake_com_3
: IsaFake

fake_com_4
: IsaFake

fake_floppy
: IsaFake

default_bus
: IOXBar

empty_isa
: IsaFake

bad_addr
: BadAddr

iobus
: IOXBar

cpu0
: X86AtomicSimpleCPU

mmu

: X86MMU

itb
: X86TLB

walker
: X86PagetableWalker

dtb
: X86TLB

walker
: X86PagetableWalker

interrupts
: X86LocalApic

cpu1
: X86AtomicSimpleCPU

mmu

: X86MMU

itb
: X86TLB

walker
: X86PagetableWalker

dtb
: X86TLB

walker
: X86PagetableWalker

interrupts
: X86LocalApic

cpu2
: X86AtomicSimpleCPU

mmu

: X86MMU

itb
: X86TLB

walker
: X86PagetableWalker

dtb
: X86TLB

walker
: X86PagetableWalker

interrupts
: X86LocalApic

cpu3
: X86AtomicSimpleCPU

mmu

: X86MMU

itb
: X86TLB

walker
: X86PagetableWalker

dtb
: X86TLB

walker
: X86PagetableWalker

interrupts
: X86LocalApic

ruby
: RubySystem

network
: SimpleNetwork

l1_cntrl0
: L1Cache_Controller

sequencer
: RubySequencer

requestFromL1Cache
: MessageBuffer

responseFromL1Cache
: MessageBuffer

unblockFromL1Cache
: MessageBuffer

requestToL1Cache
: MessageBuffer

responseToL1Cache
: MessageBuffer

l1_cntrl1
: L1Cache_Controller

sequencer
: RubySequencer

requestFromL1Cache
: MessageBuffer

responseFromL1Cache
: MessageBuffer

unblockFromL1Cache
: MessageBuffer

requestToL1Cache
: MessageBuffer

responseToL1Cache
: MessageBuffer

l1_cntrl2
: L1Cache_Controller

sequencer
: RubySequencer

requestFromL1Cache
: MessageBuffer

responseFromL1Cache
: MessageBuffer

unblockFromL1Cache
: MessageBuffer

requestToL1Cache
: MessageBuffer

responseToL1Cache
: MessageBuffer

l1_cntrl3
: L1Cache_Controller

sequencer
: RubySequencer

requestFromL1Cache
: MessageBuffer

responseFromL1Cache
: MessageBuffer

unblockFromL1Cache
: MessageBuffer

requestToL1Cache
: MessageBuffer

responseToL1Cache
: MessageBuffer

l2_cntrl0
: L2Cache_Controller

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

dir_cntrl0
: Directory_Controller

requestToDir
: MessageBuffer

responseToDir
: MessageBuffer

responseFromDir
: MessageBuffer

dma_cntrl0
: DMA_Controller

dma_sequencer
: DMASequencer

responseFromDir
: MessageBuffer

requestToDir
: MessageBuffer

io_controller
: DMA_Controller

dma_sequencer
: DMASequencer

responseFromDir
: MessageBuffer

requestToDir
: MessageBuffer

sys_port_proxy
: RubyPortProxy

mem_ctrls
: MemCtrl

system_port

in_ports

output

inputs

pio inputs

mem_side_ports

output inputs

int_pin

int_secondary int_primary

pio

pio

pio

pio keyboard_int_pin mouse_int_pin

pio pio int_pin

int_requestor

cpu_side_ports

pio

dma pio

pio pio pio pio pio pio

cpu_side_ports

default

mem_side_ports default

pio

pio

dcache_port icache_port pio int_responder int_requestor port port dcache_port icache_port pio int_responder int_requestor port port dcache_port icache_port pio int_responder int_requestor port port dcache_port icache_port pio int_responder int_requestor port port

in_port

out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port out_port

out_port

in_port in_port interrupt_out_port in_ports mem_request_port pio_request_port pio_response_port in_port in_port interrupt_out_port in_ports mem_request_port pio_request_port pio_response_port in_port in_port interrupt_out_port in_ports mem_request_port pio_request_port pio_response_port in_port in_port interrupt_out_port in_ports mem_request_port pio_request_port pio_response_port in_port in_port in_port memory_out_port in_port in_port in_port in_port

port

in_ports in_ports pio_request_port