Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey

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(Invited Paper)

***Abstract*—This paper presents a tutorial overview of ΣΔ modulators, their operating principles and architectures, circuit errors and models, design methods, and practical issues. A review of the state of the art on nanometer CMOS implementations is described, giving a survey of cutting-edge ΣΔ architectures, with emphasis on their application to the next generation of wireless telecom systems.**

***Index Terms*—Sigma-delta modulation, oversampling analog-to-digital conversion.**

I. Introduction

SINCE the first idea underlying the operation of ΣΔ modulators (ΣΔMs) was patented [1] and applied to implement analog-to-digital converters (ADCs) [2] around 50 years ago, there has been a huge number of circuits and systems exploiting ΣΔMs in many different industrial applications—from instrumentation to communications [3]–[16]. Based on the combination of *oversampling* and quantization *error shaping* techniques, ΣΔMs achieve a high degree of insensitivity to analog circuit imperfections, thus making them a good choice (the best one in many cases) to realize embedded analog-to-digital interfaces in modern systems-on-chip (SoCs) integrated in nanometer CMOS.

In spite of the aforementioned advantages, the design of CMOS ΣΔMs involves a number of practical issues and trade-offs that must be taken into account in order to optimize their performance in terms of power consumption, silicon area, and time-to-market deployment. Over the last few years, significant efforts have been made to decrease the power budget and to increase the speed of ΣΔMs, while simultaneously maintaining compatibility with mainstream digital technologies.

Manuscript received September 10, 2010; revised October 27, 2010; accepted November 23, 2010. Date of current version December 30, 2010. This work was supported in part by the Spanish Ministry of Innovation and Science (with support from the European Regional Development Fund) under Contract TEC2007-67247-C02-01/MIC and Contract TEC2010-14825/MIC, and in part by the Regional Ministry of Innovation, Science and Enterprise under Contract TIC-2532. This paper was recommended by Deputy Editor-in-Chief G. Manganaro.

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Digital Object Identifier 10.1109/TCSI.2010.2097652

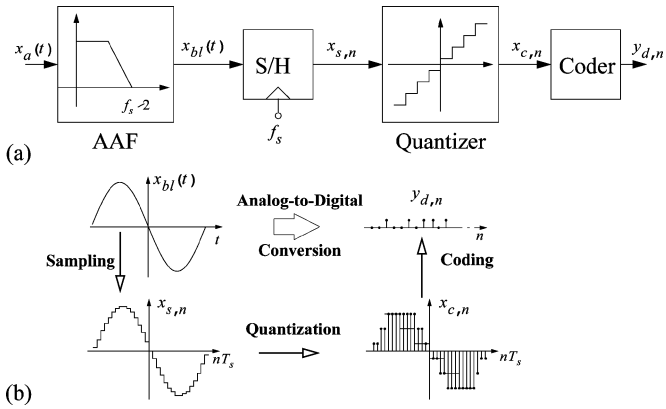

Fig. 1. Conceptual ADC. (a) Block diagram. (b) Signal processing.

This paper presents a broad survey of ΣΔMs,[1] the new advances and trends in architectures, circuit techniques, design methodologies, and practical considerations, with emphasis on nanometer CMOS realization. The paper is organized as follows. Section II gives a brief background regarding fundamentals of ADCs and basic concepts underlying ΣΔMs. Section III surveys the basic ΣΔM architectures and Section IV describes their main building blocks, error mechanisms as well as the application of their analysis and models to the development of design methodologies. Finally, Section V sums up the state-of-the-art performance, trends, and challenges.

II. Fundamentals of ΣΔ Modulators

The operation of ΣΔMs relies on the combination of two signal processing techniques, namely: *oversampling* and quantization error filtering and feedback, commonly referred to as *noise shaping*. Both techniques are related to the fundamental processes involved in an ADC—illustrated in Fig. 1.

Fig. 1(a) shows the conceptual scheme of an ADC intended for the digitization of low-pass (LP) signals, that includes the following components: an *anti-aliasing filter* (AAF), a *sampling-and-hold (S/H)* circuit, a *quantizer*, and a *coder* [17]. The operation of these blocks is illustrated in Fig. 1(b). First, the analog input signal, $x_a(t)$, passes through the AAF block. Otherwise, from the Nyquist sampling theorem, high frequency components of the input signal would be folded or aliased into the signal bandwidth, B_w, thus corrupting the signal information [18]. The resulting band-limited signal, $x_{bl}(t)$,

[1]It is impossible to cover all the topics contained in the huge number of publications dealing with ΣΔMs. Instead, this paper provides an overview of current state of the art, trends, and challenges, without entering into details.

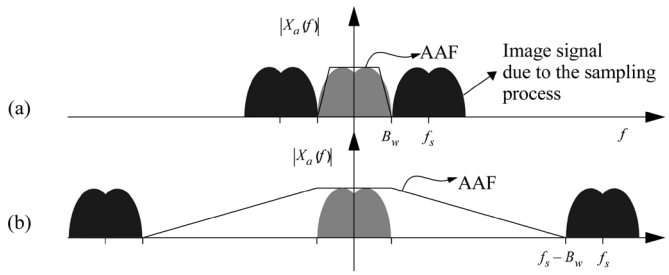

Fig. 2. AAF for: (a) Nyquist-rate and (b) oversampling ADCs.

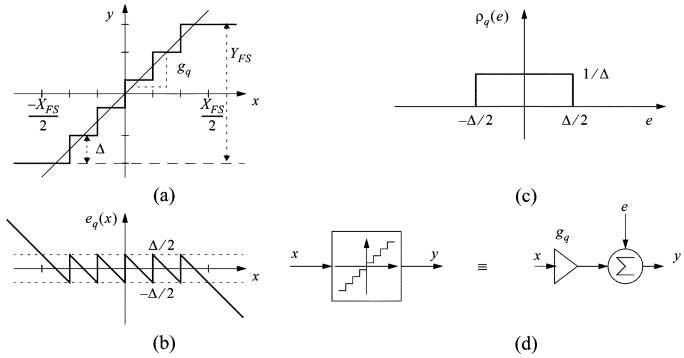

Fig. 3. Quantization process. (a) Ideal characteristic. (b) Quantization error. (c) Probability density function of white quantization noise. (d) Linear model.

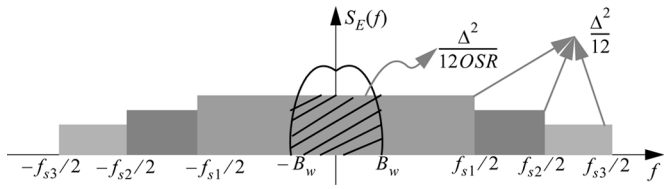

Fig. 4. Illustrating the benefits of oversampling on the in-band noise power.

is sampled at a rate of f_s by the S/H circuit, thus yielding a discrete-time (DT) signal,[2] $x_{s,n} = x_{bl}(nT_s)$. Following the S/H, the quantizer maps the continuous range of amplitudes of $x_{s,n}$ into a discrete set of levels. Finally, the coder assigns a unique binary number to each level providing the output digital data. Therefore, as illustrated in Fig. 1(b), the fundamental processes involved in an ADC are: *sampling* and *quantization*. These two *continuous-to-discrete* transformations limit the performance of ADCs [18].

A. Oversampling

The sampling process imposes a limit on B_w, and hence on the speed of the ADC. According to the Nyquist theorem, which sets that the minimum value of f_s—often referred to as Nyquist frequency and represented by f_N—must be twice the signal bandwidth, i.e., $f_N = 2B_w$. Based on this criterion, those ADCs with $f_s = f_N$ are called *Nyquist-rate* ADCs, while if $f_s > f_N$, the resulting ADCs are known as *oversampling* ADCs, and $\text{OSR} \equiv f_s/f_N$ is defined as the *oversampling ratio* [5]. One of the advantages of oversampling ADCs is that they simplify the requirements placed on the AAF as illustrated in Fig. 2. Note that the AAF for a Nyquist converter must have a sharp transition band, which often introduces phase distortion in signal components located near the cut-off frequency.

B. Quantization Error and White Noise Model

The quantization itself introduces a fundamental limitation on the performance of an ideal ADC. It degrades the quality of the input signal whose continuous-value levels are mapped onto a finite set of discrete levels as illustrated in Fig. 3. This continuous-to-discrete transformation in amplitude generates an error, commonly referred to as *quantization error*. Contrary to the sampling process, quantization is a nonreversible operation, causing a loss in the *resolution* of the digitized signal [18].

Fig. 3(a) shows the transfer characteristic of an ideal quantizer, where g_q denotes the slope of the line intersecting the code steps or quantizer gain, and $e_q(x)$ stands for the quantization error. This error is a nonlinear function of the input signal, x, as shown in Fig. 3(b). Note that, if x is confined to the full-scale input range $[-X_{\text{FS}}/2, X_{\text{FS}}/2]$, the quantization error is bounded by $[-\Delta/2, \Delta/2]$, with Δ being the quantization step, defined as the separation between adjacent output levels in the quantizer. For a B-bit quantizer, the quantization step is defined as $\Delta \equiv Y_{\text{FS}}/(2^B - 1)$, with Y_{FS} being the full-scale output range of the quantizer [see Fig. 3(a)]. For inputs outside of the interval $[-X_{\text{FS}}/2, X_{\text{FS}}/2]$, the absolute value of $e_q(x)$ exceeds $\Delta/2$ and grows monotonically. This situation is known as *overloading* of the quantizer [5]–[7].

As shown in Fig. 3(b), $e_q(x)$ strongly depends on x. However, under some assumptions which are normally met in practice [19]–[22], it can be shown that the quantization error distributes uniformly in the range $[-\Delta/2, \Delta/2]$, with rectangular probability density, $\rho_q(e_q)$, shown in Fig. 3(c), having a constant power spectral density (PSD) [19]. Because of that, the quantization error can be modeled as an additive *white noise source*, e, as shown in Fig. 3(d), usually called *quantization noise*.[3] As the total quantization noise power, $\sigma^2(e)$, is uniformly distributed in the range $[-f_s 2, f_s/2]$, its 2-sided PSD is given by

$$S_E(f) \equiv \frac{\sigma^2(e)}{f_s} = \frac{1}{f_s}\left[\frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de\right] = \frac{\Delta^2}{12 f_s} \tag{1}$$

and the *in-band* noise power, calculated for LP signals as[4]

$$P_E \equiv \int_{-B_w}^{B_w} S_E(f) df = \frac{\Delta^2}{12\text{OSR}} \tag{2}$$

decreases with OSR at a rate of 3 dB/octave. This property is exploited by oversampling ADCs, since when an oversampled signal is quantized, the spectral components of the quantization error are distributed in a larger frequency band as illustrated in Fig. 4, thus attenuating the in-band quantization noise power as compared to the one achieved by Nyquist-rate ADCs.

[2]In this figure, the notation x_n is used to represent $x(nT_s)$, with T_s being the sampling period, defined as $T_s \equiv 1/f_s$.

[3]More accurate (nonlinear) quantizer models are normally used in numerical analysis and simulations. A good example is the *describing-function* based model proposed in [23] and used in the well-known Schreier's Delta-Sigma MATLAB Toolbox [13], [24].

[4]In the case of bandpass (BP) signals centered at a given frequency f_n, (2) is transformed into $P_E = 2\int_{f_n - B_w/2}^{f_n + B_w/2} S_E(f) df = (\Delta^2)/(12\text{OSR})$.

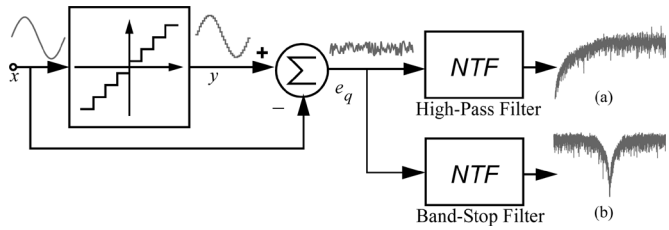

Fig. 5. Illustrating quantization *noise shaping* for: (a) LP and (b) BP signals.

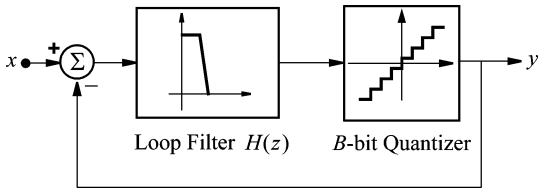

Fig. 6. Conceptual block diagram of a DT ΣΔM.

C. Noise Shaping

The accuracy of an oversampling ADC can be further increased by filtering the quantization noise in such a way that most of its power lies outside the signal band. This is illustrated in Fig. 5, where the quantization error—conceptually generated from substracting the input signal, x, from an analog version of the quantizer output, y—is *shaped* by a filter with a transfer function, usually called noise transfer function (NTF), which can be either of high-pass type [Fig. 5(a)] or band-stop type [Fig. 5(b)], respectively filtering the noise around either dc or at a given frequency, f_n, often referred to as the *notch* frequency. In the case of low-pass *oversampled* signals, low-frequency in-band components of the quantization error can be attenuated by applying a differentiator filter, with a Z-domain transfer function given by

$$\text{NTF}(z) = (1 - z^{-1})^L \tag{3}$$

where L denotes the filter order [15].

Taking into account that $z = e^{j2\pi/f_s}$, $f_s \equiv 2 \cdot \text{OSR} \cdot B_w$, assuming that OSR $\gg 1$ and that the quantization error can be modeled as an additive white noise source, the in-band *shaped* noise power is approximately given by

$$\begin{aligned} P_Q &\equiv \int_{-B_w}^{B_w} \frac{\Delta^2}{12 f_s} |\text{NTF}(f)|^2 df \\ &\simeq \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)\text{OSR}^{2L+1}} \end{aligned} \tag{4}$$

which decreases with OSR by approximately $6L$ dB/octave more than just using oversampling as in (2). This is a direct consequence of the combined action of both oversampling and noise shaping.[5]

[5]Similar reasoning can be followed for BP signals, considering NTF$(z) = (1-z^{-1}z_n)(1-z^{-1}z_n^*)$, where z and z^* are complex conjugate zeroes, which are normally placed in the unit circle, i.e., $z_n = e^{j(2\pi f_n/f_s)}$. The resulting P_Q has a similar expression as in (4) [25].

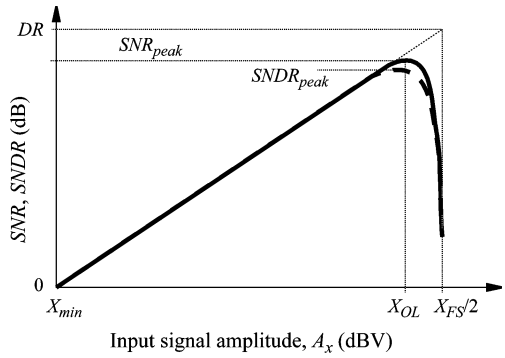

Fig. 7. Illustrating basic performance metrics: SNR, SNDR, and DR.

D. Putting All Pieces Together: ΣΔ Modulation

Oversampling and noise-shaping can be used to build an ADC by embedding a quantizer in a feedback loop[6] as illustrated in Fig. 6—generally known as ΣΔM [2], [5], [6].[7] Let us consider that the gain of the loop filter, $H(z)$, is large inside the signal band and small outside it. Due to the action of the feedback, the input signal, x, and the analog version of the modulator output, y, will practically coincide within the signal band. Consequently, most of the differences between both signals will be placed at higher frequencies, i.e., the quantization error, e_q, is *shaped* and most of its power is pushed outside the signal band. Assuming that the quantizer in Fig. 6 is represented by the linear, additive white noise model of Fig. 3(d), the feedback system in Fig. 6 can be viewed as a two-input, x and e, one-output, y, system, which can be represented in the Z-domain by[8]

$$Y(z) = \text{STF}(z)X(z) + \text{NTF}(z)E(z) \tag{5}$$

where $X(z)$ and $E(z)$ represent the Z-transform of x and e, respectively, and STF(z) and NTF(z) stand for the signal- and noise transfer functions, respectively given by

$$\text{STF}(z) = \frac{g_q H(z)}{1 + g_q H(z)}; \text{NTF}(z) = \frac{1}{1 + g_q H(z)} \tag{6}$$

Note that, if the loop filter is designed such that $|H(f)| \to \infty$ within the signal band, then $|\text{STF}(f)| \to 1$ and $|\text{NTF}(f)| \to 0$, i.e., the input signal is allowed to pass whereas the quantization error is ideally cancelled. However, the error cannot be completely nulled in practice because $H(z)$ has a limited gain, and

[6]Early implementations of Fig. 6 used an integrator as a loop filter. Hence, the system can be viewed as a differencing (Δ) operation at the input followed by a summation (Σ), implemented by the DT integrator. From this point of view, the system in Fig. 6 is called ΔΣM. In contrast, this system can be obtained by cascading an integrator (Σ) with a Δ modulator, and hence it is called ΣΔM. The latter term (ΣΔM) will be used in this paper, although both terms are widely used [13].

[7]As will be discussed later, ΣΔMs can be classified into two main groups: LP and BP, according to the type of the input analog signal. Fig. 6 corresponds to a LP ΣΔM.

[8]This approximation is only valid if the feedback system is stable. Moreover, the analysis presented in this section assumes an ideal implementation of the loop filter, $H(z)$. However, even considering an ideal circuit implementation, the result in (4) can not be achieved in practice due to the scaling required in the loop filter coefficients [13].

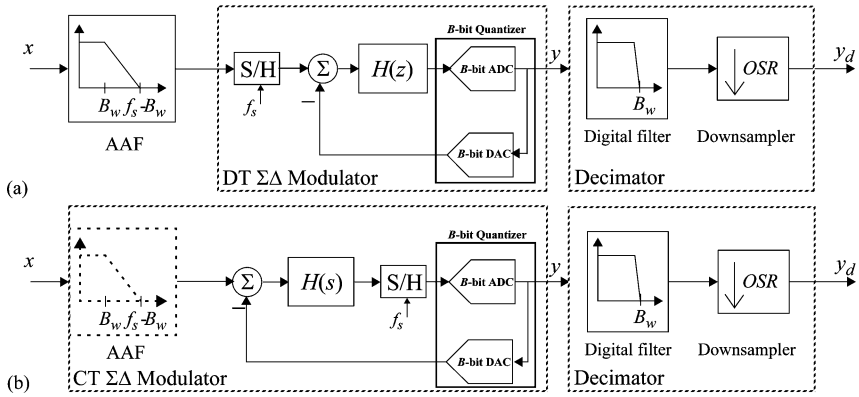

Fig. 8. Block diagram of: (a) DT-ΣΔ ADCs and (b) CT-ΣΔ ADCs.

the in-band noise power is given by (4), whenever $H(z)$ is defined so that NTF(z) is given by (3).

Assuming a sinewave input signal of amplitude A_x, the signal-to-noise ratio (SNR)[9] and the dynamic range (DR) at the output of the modulator are given by[10]

$$\text{SNR} \equiv \frac{A_x^2}{2P_Q}; \text{DR} \equiv \frac{(X_{\text{FS}}/2)^2}{2P_Q}. \tag{7}$$

The above performance metrics are conceptually represented in Fig. 7. Note that SNR increases with A_x until A_x reaches the overload level, X_{OL}. Beyond this level the quantizer input frequently goes outside the nonoverload range of the quantizer and hence the SNR curve drops sharply. As will be discussed in Section IV, the ideal performance depicted in Fig. 7 is degraded as a consequence of other error contributions—both linear and nonlinear—to the in-band error power, apart from quantization error. To take into account all these errors, the signal-to-(noise plus distortion) ratio (SNDR) is defined [26]. The maximum values of SNR and SNDR are often called SNR_{peak} and $\text{SNDR}_{\text{peak}}$, respectively illustrated in Fig. 7. Replacing the expression (4) in (7), the ideal value of DR expressed in dB gives

$$\text{DR}|_{\text{dB}} = 10\log\left[\frac{3(2^B-1)^2(2L+1)\text{OSR}^{2L+1}}{2\pi^{2L}}\right]. \tag{8}$$

Note that the expression of DR for an ideal N-bit Nyquist-rate ADC can be obtained by replacing $B = N, L = 0$ and $\text{OSR} = 1$ in the above expression, yielding [26]

$$\text{DR}|_{\text{dB}} \simeq 6.02N + 1.76. \tag{9}$$

From (8) and (9), it can be established that the *effective number of bits* (ENOB)—defined as the number of bits needed for an ideal Nyquist-rate ADC to achieve the same DR as an ideal ΣΔ ADC—is given by [27][11]

$$\begin{aligned}\text{ENOB}|_{\text{bits}} \equiv N &\simeq \frac{\text{DR}|_{\text{dB}} - 1.76}{6.02} \\ &\simeq \log_2\left[\frac{(2^B-1)(2L+1)}{\pi^{2L}}\right] \\ &\quad + \left(L+\frac{1}{2}\right)\log_2(\text{OSR})\end{aligned} \tag{10}$$

that means that a ΣΔM can achieve the same *effective resolution* as an ideal N-bit Nyquist-rate ADC by properly combining oversampling (OSR) and noise-shaping (L) to improve the accuracy of the embedded coarse quantization (typically $B < 5$).

E. Basic Architecture of a ΣΔ ADC

Fig. 8 shows the basic block diagram of a ΣΔ ADC, where Fig. 8(a) corresponds to a DT implementation (DT-ΣΔ ADC) and Fig. 8(b) is a continuous-time (CT) implementation (CT-ΣΔ ADC). In both cases, LP signals are assumed to be processed. Otherwise, the filters involved must be changed from LP to BP transfer functions.

The scheme in Fig. 8 is made up of three main blocks: an AAF, a ΣΔM, and a *decimator*. Note from Fig. 8(b) that in the case of CT-ΣΔ ADCs, the input signal could be either subject to AAF or fed directly into the modulator without preceding any filtering. This can be done thanks to the implicit AAF which is embedded in CT-ΣΔMs [28]. Indeed, DT-ΣΔMs implement the sampling operation at the modulator input [Fig. 8(a)], whereas CT-ΣΔMs do it at the quantizer input and the loop filter is CT—see Fig. 8(b). Thus, the output signal is DT and a DT-to-CT transformation is needed to create the feedback signal. The process of reconstructing this signal, by using proper output pulse shape of the embedded digital-to-analog converter (DAC), plays a significant role on the overall CT-ΣΔM performance as will be discussed later [14].

The output of the ΣΔM is a B-bit digital stream clocked at f_s. The decimator, which is a purely digital block, removes the high-frequency components of the ΣΔM digital stream through high-selectivity digital filtering, and *decimates* to reduce the

[9]Strictly speaking, the term "signal-to-quantization-noise ratio (SQNR)" should be used if only quantization error is considered. However, for the sake of simplicity, SNR will be used in this paper.

[10]SNR is defined as the ratio of the output power at the frequency of an input sinusoid to the uncorrelated in-band error power. DR is defined as the ratio of the output power at the frequency of an input sinusoid with maximum amplitude $(A_x = A_{x,\max} \equiv X_{\text{FS}}/2)$ to the output power for a small input for which SNR = 0 dB [26].

[11]In practice, the effective resolution of most ΣΔMs is less than the ideal DR due to overload, circuit noise, and nonlinear errors. Hence, a more realistic expression of ENOB can be obtained by replacing DR with $\text{SNDR}_{\text{peak}}$ in (10).

rate of the ΣΔM output stream down to the Nyquist frequency. Hence, the output of the ΣΔ ADC is a digitized version of the input signal—clocked at f_N—with an equivalent resolution given by (10).

Out of the three blocks in Fig. 8, the ΣΔM is the most critical one, responsible for the accuracy of the whole ADC. For that reason, this paper will focus on this block, although taking into account that a ΣΔ ADC needs also the other two blocks [15].

III. Taxonomy of ΣΔ Modulators

A large number of ΣΔM architectures have been reported in the open literature that implement some (or all) the following, nonexclusive, strategies to improve DR [6], [7]:

- *Increasing* L. According to (8), for a given value of OSR, the increase in DR with L leads to $\Delta\text{DR}|_{\text{dB}} \simeq 10\log\{[(2L+3)/(2L+1)][\text{OSR}/\pi]^2\}$. However, the use of high-order modulator loop filtering (usually $L > 3$) gives rise to stability problems, and the necessary loop gain scaling worsens the performance below the ideal one.
- *Increasing OSR* leads to an increment of $(L+1/2)$ bit/octave in the effective resolution. However, for wideband signals the use of high values of OSR is impractical, because of the prohibitive sampling frequencies required, with the subsequent penalty in power consumption.
- *Increasing* B leads to an increase of 6 dB (1 bit) in DR for each extra bit in the quantizer [11]. However, the required multibit feedback DAC is not inherently linear.

The above strategies can be classified according to:

- The *nature of the signals* being handled, resulting in LP and BP ΣΔMs.
- The *number of bits* of the internal quantizers, dividing ΣΔMs into *single-bit* and *multibit* topologies.
- The *number of quantizers* employed. ΣΔMs employing only one quantizer are called *single-loop* structures, whereas those using several quantizers give rise to different topologies, namely: *cascade*, *dual-quantization*, etc.
- The *circuit nature of the loop filter*, classifying ΣΔMs into two main groups DT [Fig. 8(a)] and CT [Fig. 8(b)] implementations. According to this criterion, another type of ΣΔMs, called *hybrid* CT/DT ΣΔMs, tries to take advantage of the benefits of both circuit techniques [29]–[34].

Describing all possible ΣΔM architectures derived from previous classification goes beyond the scope of this paper. A detailed study of them can be found in many papers and books [5]–[16]. Instead, this section will focus on the most representative *families* of ΣΔM topologies.

A. Low-Order Single-Loop ΣΔMs

The simplest way of building a ΣΔM architecture is combining a DT forward-Euler (FE) integrator, i.e., $H(z) = z^{-1}/(1-z^{-1})$ as the loop filter with a single-bit quantizer, i.e., a comparator. The resulting architecture—known as first-order single-bit ΣΔM—is illustrated in Fig. 9(a). Assuming a linear model for the quantizer, the Z-transform of the modulator output is given by (5) with $\text{STF}(z) = z^{-1}$ and $\text{NTF}(z) = (1 - z^{-1})$. This topology has two main disadvantages. On the one hand, DR increases with OSR at a rate of only

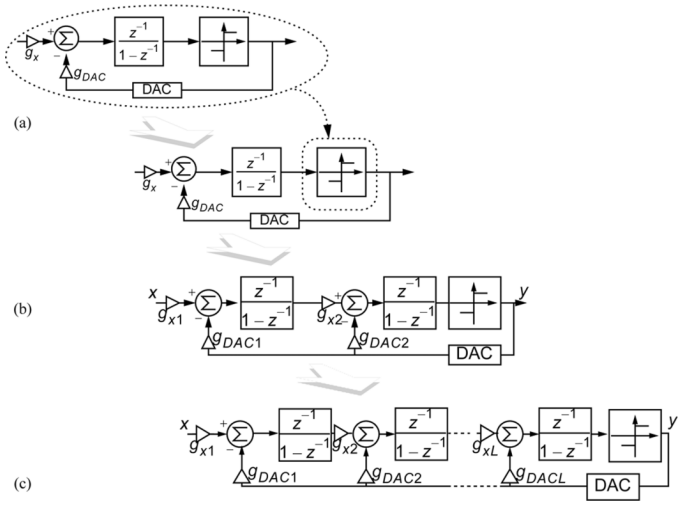

Fig. 9. Basic single-loop ΣΔMs. (a) First order. (b) Second order. (c) Lth order.

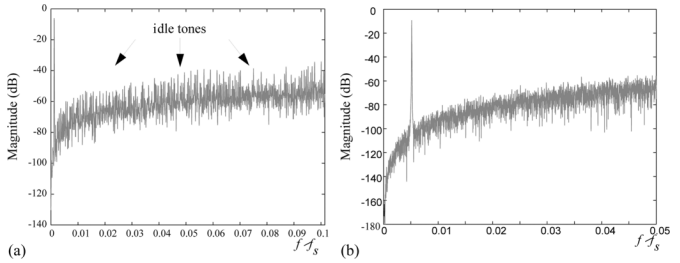

Fig. 10. Output spectrum of a (a) first-order ΣΔM; (b) second-order ΣΔM.

1.5-bit/octave, which implies using very high values of OSR to achieve medium-high effective resolutions. Another important drawback associated to first-order single-bit ΣΔMs is the presence of *pattern noise* and the so-called *idle tones* as illustrated in Fig. 10(a). This tonal behavior, which is present even considering ideal circuit components, is a direct consequence of the strong correlation existing between the input signal and the quantization error. This correlation leads to a colored quantization error, instead of a white noise and—in addition to causing a number of tones within the signal band—gives rise to an in-band error power higher than that predicted by the linear model [19], [22], [35].

The problems of Fig. 9(a) can be mostly avoided if the 1-bit quantizer in a first-order ΣΔM is replaced itself by a first-order ΣΔM as illustrated in Fig. 9(b). The resulting modulator is called second-order ΣΔM, which is stable if $g_{\text{DAC2}} = 2g_{x1}g_{\text{DAC1}}$ [36]. In that case, assuming $g_{x1} = g_{x2} = 1$ and a white noise model for the quantizer, we obtain $\text{STF}(z) = z^{-2}$ and $\text{NTF}(z) = (1 - z^{-1})^2$. Moreover, DR increases with OSR by 2.5-bit/octave, which significantly improves the performance of the first-order modulator in terms of the sampling frequency required. In addition, the use of two integrators also contributes to decorrelate the input signal and the quantization error, thus decreasing the presence of idle tones in the output spectrum as illustrated in Fig. 10(b).

B. High-Order ΣΔMs

The concept underlying first- and second-order single-loop ΣΔMs can be extended towards Lth-order filtering, thus re-

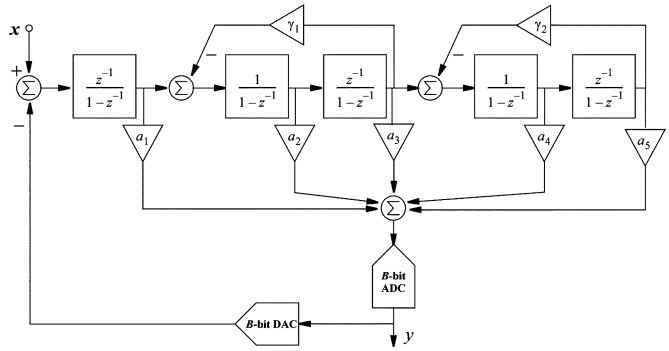

Fig. 11. Fifth-order single-loop ΣΔM with feedforward summation and local resonator feedbacks.

sulting in the modulator topology shown in Fig. 9(c), which is known as L-th order single-loop ΣΔM with distributed feedback. Using a linear model for the quantizer, it can be shown that $\mathrm{STF}(z) = z^{-L}, \mathrm{NTF}(z) = (1 - z^{-1})^L$ and DR is given by (8). However, this performance is not achieved in practice due to stability problems associated to *pure differentiator NTFs*, in which stability can only be conditionally guaranteed for a limited range of input amplitudes when $L > 2$ [37]. In order to address this problem, alternative realizations of high-order single-loop ΣΔMs have been proposed that implement an IIR NTF [6], [7]. A pioneer topology using multiple feedforward and feedback analog paths was proposed by Lee and Sodini, synthesizing NTFs of the form $\mathrm{NTF}(z) = (z-1)^L/D(z)$, with $D(z)$ being a polynomial determined by the feedforward analog coefficients [38]. There are several implementations of this idea. As an illustration, Fig. 11 shows an example that consists of a 5th-order single-loop with an IIR NTF. This modulator—often referred to as cascade of resonators with distributed feedforward (CRFF)—sets $\mathrm{STF}(z) = 1 - \mathrm{NTF}(z)$ [6]. Local resonation feedback coefficients $(\gamma_{1,2})$ can be used to set additional notches in $\mathrm{NTF}(z)$ in order to increase the noise filtering without increasing the loop filter order.

A common disadvantage of most high-order single-loop ΣΔM topologies implementing IIR NTFs is the increased circuit complexity due to the large number of analog coefficients required. A well-known alternative to circumvent instability while obtaining high-order noise-shaping consists of using the so-called MASH (*multistage noise-shaping*) ΣΔMs, often referred to as cascade or multistage ΣΔMs [6], [39]. This architecture is conceptually depicted in Fig. 12. Each stage, consisting of a low-order (typically either second or first order) single-loop ΣΔM, modulates a signal that contains the quantization error generated in the previous stage. Once in the digital domain, the stage outputs are processed and combined by a *digital cancellation logic* (DCL) so that only the quantization error of the last stage remains. Also, this error is shaped by a transfer function whose order equals the sum of the respective orders of all the stages in the cascade, i.e., $L = L_1 + L_2 + \cdots + L_N$. However, in practice, it is well known that the maximum number of stages—and consequently L—is limited by circuit nonidealities, particularly mismatch. This error causes incomplete cancellation of low-order quantization errors at the modulator output [15]. This effect—known as noise *leakage*—is especially critical in cascade CT-ΣΔMs because

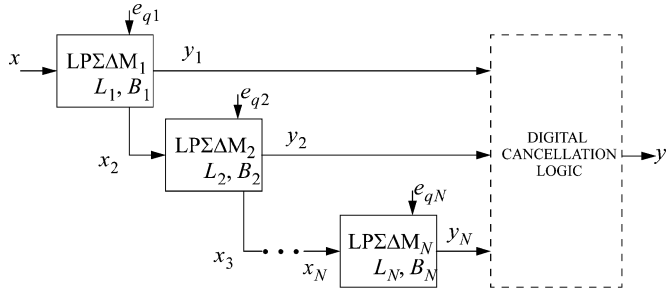

Fig. 12. Conceptual block diagram of a cascade ΣΔM.

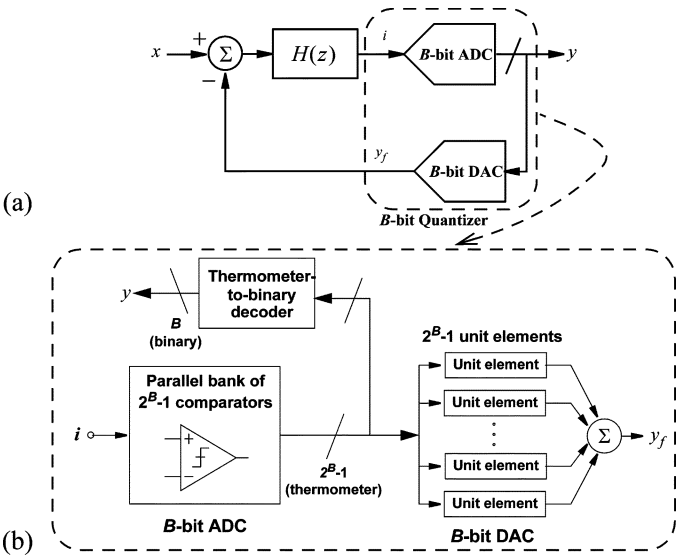

Fig. 13. Conceptual scheme of a ΣΔM with B-bit quantization. (a) Block diagram. (b) Embedded B-bit ADC and DAC.

of their higher sensitivity to circuit element tolerances—a fact which may account for the small number of cascade CT-ΣΔM integrated circuits (ICs) reported so far [40]–[43].

C. Multibit and Dual-Quantization ΣΔMs

According to (10), an alternative way to improve the effective resolution consists of using embedded multibit $(B > 1)$ quantization—conceptually depicted in Fig. 13(a). As illustrated in Fig. 13(b), a multibit DAC commonly uses $2^B - 1$ unit circuit elements (capacitors, resistors, current sources, etc.) to reconstruct the analog feedback signal in the modulator loop with 2^B levels. Thus, the analog output level is generated by summing up the unit element outputs (usually charges or currents). Due to mismatches among different unit elements, a nonlinear input-output DAC characteristic is obtained. The nonlinear errors associated to the multibit feedback DAC are directly injected at the modulator input, thus degrading the modulator performance. Consequently, at least in single-loop topologies like the one conceptually depicted in Fig. 13(a), the embedded feedback DAC must be designed to reach the linearity targeted for the whole ΣΔ ADC [44].

A large number of strategies have been reported in order to achieve highly-linear multibit ΣΔMs, some of them requiring modest component matching [45]. Among other techniques, one of the most popularly used is the so-called dynamic element

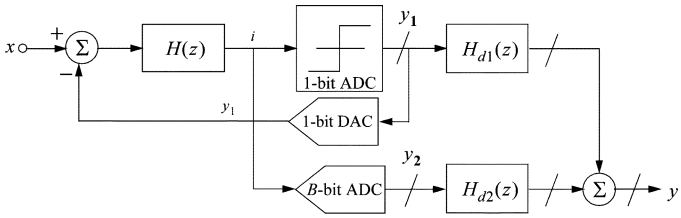

Fig. 14. Dual-quantization concept proposed by Leslie and Singh [55].

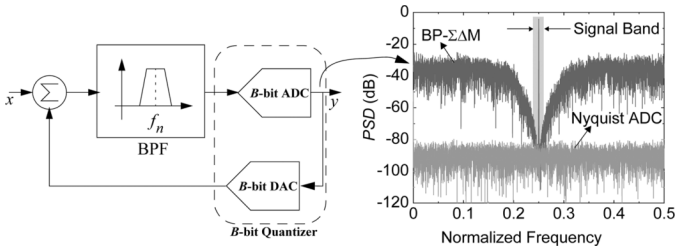

Fig. 15. Conceptual block diagram and output spectrum of a BP-ΣΔM.

matching (DEM) [11], [44]. The basic idea behind DEM techniques consists of breaking the direct correspondence existing between the thermometer input code and their associated DAC output levels, so that the unit elements selected to generate a given DAC output level vary over time. This way, the fixed error of that level will be transformed into a *time-varying error*. To that purpose, a block is added to control the selection of elements at each clock cycle. The selection is done according to simple algorithms[12] that try to drive the average error in each DAC level to zero over time. Thus, part of the DAC error power that laid in the low-frequency range will be moved to higher frequencies, where it can be removed by the decimation filter.

Other alternatives to reduce the impact of DAC nonlinearities are based on deterministic techniques, such as analog calibration [53], digital correction [54], and dual quantization. The latter consists of combining single-bit and multibit quantization in the same modulator topology in order to take advantage of the intrinsic linearity of 1-bit quantization and the reduced quantization error of multibit quantizers [15].

Since the original dual-quantizer general scheme was proposed by Leslie and Singh [55], illustrated in Fig. 14, there has been several ΣΔM topologies based on the same idea [56]. Among others, the most common approach consists of combining dual quantization and cascade topologies, so that only the last-stage quantizer is multibit, while the remaining ones are usually single-bit, i.e., $B_1 = B_2 = \cdots = B_{N-1} = 1$ and $B_N > 1$ in Fig. 12. Therefore, the multibit DAC nonlinear errors are injected in the last stage of the cascade, so that the linearity requirements are relaxed because of the attenuation provided by the gain of the preceding stages within the signal band [57], [58].

D. Bandpass ΣΔMs

BP-ΣΔMs are a particular class of ΣΔMs that place the zeroes of NTF(f) in a given bandwidth around an intermediate frequency (IF) location, usually named center or *notch* frequency, f_n. Therefore, BP-ΣΔMs differ from their LP counterparts in that the loop filter is of BP type instead of LP type as illustrated in Fig. 15 [59]–[62]. This has an obvious application in the front-end of wireless communication systems. Indeed, BP-ΣΔMs are very suited for the implementation of ADCs in such systems because, compared with Nyquist-rate ADCs, BP-ΣΔMs do not need to digitize the whole Nyquist band (from dc to f_s) (see Fig. 15). Instead, they digitize just the signal band, thereby requiring much lower power consumption to obtain a given DR [25], [63]. In addition, IF A/D conversion allows a great part of the signal processing to be moved from the analog domain to the digital domain, including: quadrature mixing, channel selection, gain control, and demodulation. This results in robust radiofrequency (RF) receivers with high degree of programmability and adaptability to a number of standard specifications [64], [65]. BP-ΣΔMs share much in common with their LP counterparts, except for the obvious difference that the quantization noise is suppressed around f_n instead of dc. A common choice is $f_n = f_s/4$, i.e., just in the middle of the Nyquist band. It can be shown that this location optimizes the trade-off between antialiasing filtering and image-reject filtering in digital wireless transceivers [25]. Linked to the choice of $f_n = f_s/4$, BP-ΣΔMs architectures are obtained from LP-ΣΔMs by applying a LP-to-BP transformation method, which in the DT domain is formulated as $z^{-1} \rightarrow -z^{-2}$. As a consequence of this transformation, the zeroes of the original LP NTF(z) are moved from dc to $f_s/4$. Moreover, this transformation keeps all properties of the original LP-ΣΔMs.[13]

The design and analysis of BP-ΣΔMs is the same as that of LP-ΣΔMs, but considering bandpass loop filters instead of lowpass loop filters. Indeed, it can be shown that the main figures of merit, i.e., in-band noise power, DR, SNR, SNDR have the same expressions as the ones obtained in previous sections. In practice, it means that a BP-ΣΔM can be synthesized by replacing integrators by *resonators* in the modulator loop filter as will be described in Section IV [6], [28], [66].

E. Continuous-Time ΣΔMs

The majority of ΣΔMs reported so far have been implemented using DT circuit techniques, mostly based on switched-capacitor (SC) circuits [15]. However, the increasing demand for ever faster ADCs in broadband communication systems has boosted the interest in CT implementations. These modulators are able to operate at higher sampling rates with lower power consumption than their DT counterparts [10], [14], [66].

Looking at both architectures depicted in Fig. 8, one can see several differences between DT- and CT-ΣΔMs. Apart from the CT circuit nature of the loop filter, the most significant difference is related to the point where the sampling process

[12]The interested reader can find a detailed explanation of these algorithms in a number of papers and books [46]–[52].

[13]Placing the signal passband at $f_s/4$ presents some disadvantages. On the one hand, in the presence of nonlinear errors in the analog circuitry of the modulator, any intermodulation distortion products resulting from the mixing of tones located at $f_s/2$ with input signal will fall inside the passband, thus corrupting the signal information. On the other hand, for a given IF signal, the demands for the sampling rate of the modulator are more restrictive than placing the signal passband center frequency between $f_s/4$ and $f_s/2$. Therefore, similarly to LP-ΣΔMs, it may be convenient for BP-ΣΔMs to directly address the synthesis of NTF(f) through proper placement of its poles and zeroes. Many different BP-ΣΔMs—like for instance N-path or quadrature topologies—can be synthesized using this method [25].

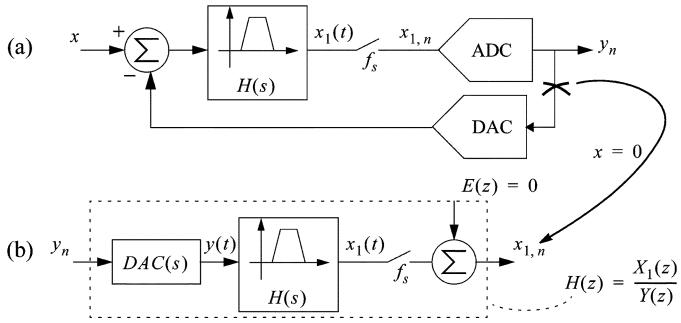

Fig. 16. Conceptual scheme of a CT-ΣΔM. (a) Block diagram. (b) Open-loop filter and CT-DT equivalence.

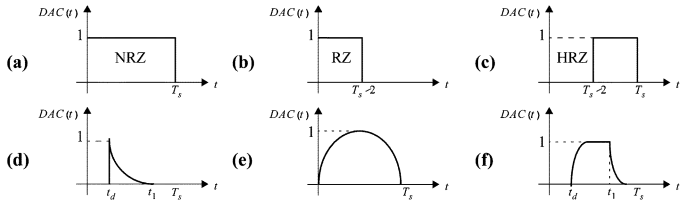

Fig. 17. Common DAC impulse responses [14]. (a) NRZ. (b) RZ. (c) HRZ. (d) Exponential decaying. (e) Cosine. (f) Nonlinear slope.

takes place, which constitutes one of the key advantages of CT-ΣΔMs over their DT counterparts [14]. However, as both DT- and CT- signals are involved, the mathematical analysis (and consequently the synthesis) of CT-ΣΔMs becomes more difficult than in the case of DT-ΣΔMs [10], [28], [63], [66]–[68].

In order to understand the principles of operation underlying the signal processing involved in CT-ΣΔMs, let us consider the conceptual block diagram shown in Fig. 16(a). Note that the modulator output signal must be transformed from DT- to CT- in the feedback loop. This signal reconstruction is very critical and has a significant impact on the overall behavior of the modulator [28]. There are several DAC waveforms that can be used in CT-ΣΔMs. Fig. 17 shows a summary of the most representative possibilities including the nomenclature used for the feedback waveforms—extracted from [14]. Among others, the most commonly used DACs incorporate rectangular feedback pulses of basically three types: nonreturn-to-zero (NRZ) [Fig. 17(a)], return-to-zero (RZ) [Fig. 17(b)], and half-delay return-to-zero (HRZ) [Fig. 17(c)]. Their Laplace S-transforms can be generally written as

$$\mathrm{DAC}(s) = \frac{e^{-sp_1T_s} - e^{-sp_2T_s}}{s} \tag{11}$$

where $(p_1, p_2) = (0,1), (0,1/2)$ and (1/2, 1) for NRZ, RZ, and HRZ DACs, respectively.

Let us consider the transfer function for the DAC in (11) and the basic block diagram of the CT-ΣΔM shown in Fig. 16(a). Because of the presence of a S/H inside the loop, the input-output behavior of the noise shaping loop filter can be described by an equivalent DT transfer function, as illustrated in Fig. 16(b), given by

$$H(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}[\mathrm{DAC}(s)H(s)]\left[\sum_{n=0}^{\infty}\delta(t-nT_s)\right]\right\} \tag{12}$$

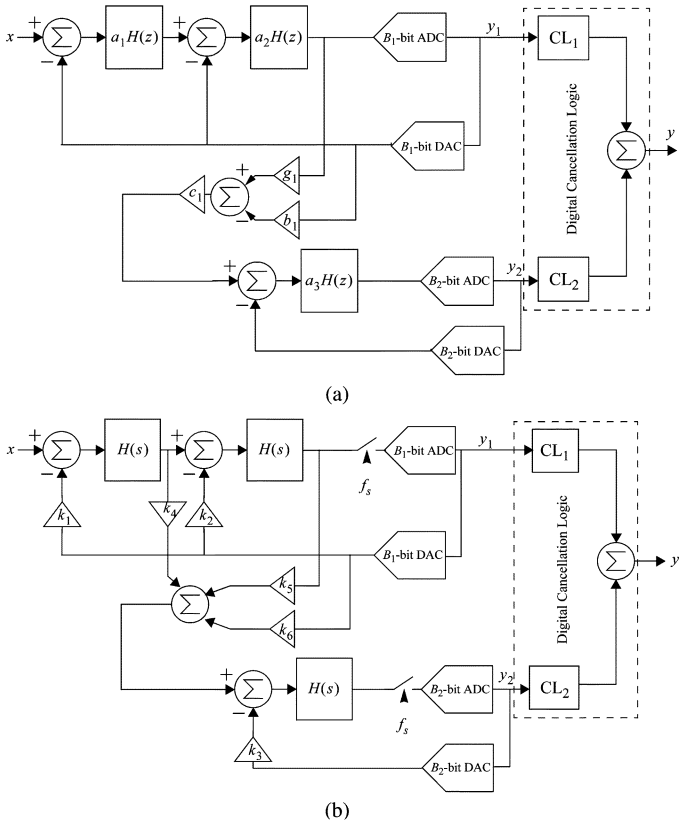

Fig. 18. Cascade 2-1 ΣΔM. (a) DT block diagram. (b) CT equivalent.

where $\mathcal{Z}\{\cdot\}$ and $\mathcal{L}^{-1}\{\cdot\}$ stand for the Z- and inverse L-transform operators, respectively.

Based on the equivalent DT loop filter transfer function shown in (12), the most usual procedure to design CT-ΣΔMs consists of, first, matching this equivalent filter with a reference DT loop filter chosen to fulfill the specifications; then, solving for the coefficients of the CT filter; and finally implementing this filter by CT circuits, usually based on Gm-C or active-RC building blocks. Careful choice of the CT filter structure is needed to have sufficient degrees of freedom to implement the reference DT loop filter [63]. In theory, any arbitrary ΣΔM topology, either single-loop or cascade, can be synthesized using a *DT-to-CT transformation method*. As an illustration, Fig. 18 shows a cascade 2-1 CT-ΣΔM obtained using such a method with its equivalent DT-ΣΔM [14].

The main problem of using the DT-to-CT synthesis method is that it usually yields an increase of the analog circuit complexity, with the subsequent penalty in sensitivity to technology parameter variations. This is particularly critical in the case of cascade CT-ΣΔM topologies, where—in order to get a functional modulator while keeping the digital cancellation logic of the original DT-ΣΔM—every integrator and DAC output must be connected to the integrator input of later stages [14].

An alternative method for the design of the loop filter uses the desired NTF(f) as a starting point. This synthesis method is often referred to as *direct CT synthesis method*. Usually, an inverse Chebychev distribution of the NTF(f) zeroes is considered because it has advantages in terms of SNR and stability. Once the desired NTF(f) has been chosen, the loop filter can be derived from the linearized model [10]. Indeed, it can

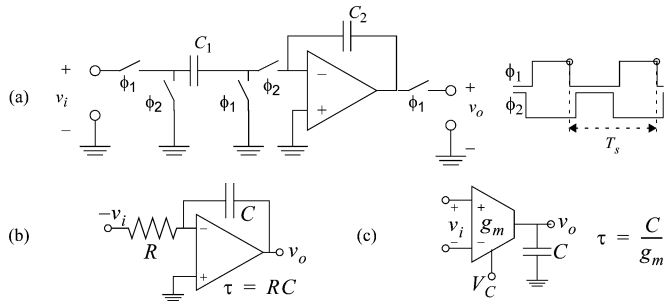

Fig. 19. Basic integrators in ΣΔMs. (a) SC FE. (b) Active-RC. (c) Gm-C.

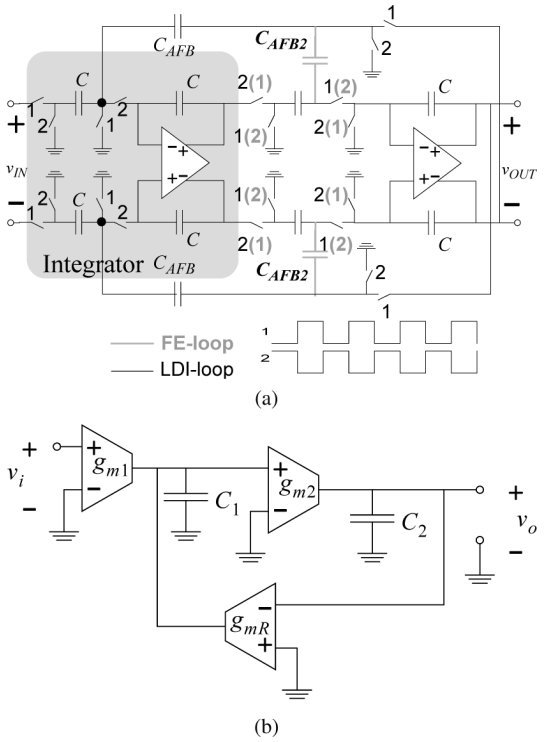

Fig. 20. Basic resonators in BP-ΣΔMs based on: (a) SC lossless direct integrators (LDIs) and FE integrators [71]; (b) Gm-C integrators [77].

be shown that applying the direct-synthesis method to cascade CT-ΣΔMs, more efficient architectures are obtained in terms of loop filter optimization, analog circuitry complexity, power consumption, and robustness to circuit element tolerance errors [69].

IV. Nonideal Performance and Systematic Design

In previous sections, ΣΔMs have been considered ideal systems except for their inherent quantization error. In practice, such an ideal performance is degraded as a consequence of the circuit error mechanisms.[14] Therefore, the impact of circuit nonidealities must be carefully considered during the design phase. This Section gives an overview of main ΣΔM circuit building blocks and their associated errors, with emphasis on their application to the systematic design of ΣΔMs.

[14]A deep study of circuit implementation and the impact of their error mechanisms on the performance of ΣΔ ADCs can be found in [15] and [14], considering SC- and CT- ΣΔMs, respectively.

A. Integrators and Resonators: Basic ΣΔM Building Blocks

Integrator circuits are the most important and critical building blocks of ΣΔMs [7], [14], [66]. Fig. 19 shows the integrator circuit topologies most commonly used in both DT- and CT-ΣΔMs. Fig. 19(a) shows a conceptual scheme of the well-known FE SC integrator, that implements a transfer function $H(z) = z^{-1}/(1 - z^{-1})$. Fig. 19(b) and (c) show the conceptual schematics of the most frequently used CT integrators: Active-RC and Gm-C, respectively.[15] Both CT circuits have an ideal transfer function $H(s) = 1/(\tau s)$, where τ is the time constant, which is the product of the resistive and capacitive elements of the CT integrator—shown in Fig. 19 for each type of implementation. In practice, the behavior of CT integrators involves a number of circuit design trade-offs. Thus, active-RC integrators present better linearity and larger signal swing, whereas Gm-C integrators usually can operate at higher frequencies [70].

As stated in Section III.D, the integrators which form the loop filter in LP-ΣΔMs become resonators in BP-ΣΔMs. There are many resonator filters using either DT or CT circuit techniques that have been included in ΣΔM ICs [25]. Fig. 20(a) shows the schematic of a SC fully differential implementation [71].[16] Both resonator structures have a transfer function of the form $H(z) = z^{-a}/(1 + z^{-2})$, which has poles located at $z_n = e^{(\pm j\pi/2)}$, that is, $f_n = \pm f_s/4$. This is a consequence of the aforementioned $z^{-1} \rightarrow -z^{-2}$ (LP-to-BP) transformation method applied to integrators. In some applications such as *multistandard wireless telecom systems*, it is required to make the resonance frequency variable so that f_n can be tunable (without changing f_s) within a given band. This property can be implemented in the circuits shown in Fig. 20(a) by tuning capacitor ratios $C_{\mathrm{AFB,AFB2}}/C$. In the case of CT (Gm-C) resonators [17]—conceptually depicted in Fig. 20(b)—the resonance frequency, given by $f_n = (1)/(2\pi)\sqrt{(g_{m2}g_{mR})/(C_1C_2)}$, can be electronically tuned by g_{mR} [77].

B. Circuit Errors in ΣΔMs

There are a number of circuit nonidealities and nonlinearities causing a deviation from the ideal behavior of integrators and resonators. The way in which these nonidealities affect the performance of ΣΔMs depends on many different factors, among others: the nature of the error itself; the influence on a given subcircuit; the effect on NTF, etc.

[15]Most frequently used implementations of CT-ΣΔMs include either active-RC or Gm-C integrators or a combination of both types of integrators. In order to benefit from both active-RC and Gm-C integrators, the most common situation in practice (particularly in those modulators targeting medium-high resolution within medium bandwidths) consists of including a front-end active-RC integrator whereas the remaining integrators in the modulator loop are implemented using Gm-C techniques [14].

[16]SC resonators can be also implemented using N-path circuit techniques in order to reduce the number of opamps required. The price to pay is the increase of the circuitry complexity (in terms of switches and capacitors), and clock timing, which needs to be carefully designed to prevent image components from appearing in the signal band [72], [73].

[17]Gm-C resonators can also be implemented by a transconductor driving a LC tank, often referred to as Gm-LC resonators. Either monolithic or off-chip inductors can be used for their implementation involving different design trade-offs among area, frequency accuracy, quality factor, etc. [74]–[76].

In the case of SC implementations, main circuit effects can be grouped according to the $\Sigma\Delta$M circuit they affect as [7], [11], [27], [78]–[80]:

- Amplifiers: Output swing, finite (linear and nonlinear) dc gain, dynamic limitations (gain-bandwidth, GB, and slew-rate, SR), thermal and flicker noise, etc.
- Quantizers: hysteresis, offset, and gain error.
- Capacitors: mismatch and nonlinearity.
- Switches: finite switch-on resistance, thermal noise, charge injection, clock feedthrough, nonlinearity.
- Multibit DACs: offset, gain error, and nonlinearity.

The above errors can be classified according to their effect on the modulator performance into two main families. On the one hand, those errors that change the NTF, such as the amplifier dc gain, capacitor mismatch, and incomplete integrator (linear) settling error. The effect of these errors strongly depends on the modulator topology. For instance, cascade $\Sigma\Delta$Ms are more sensitive to capacitor mismatch and finite dc gain (often referred to as *integrator leakage*) than single-loop architectures. On the other hand, the second category of SC errors are those which can be modeled as additive noise sources at the modulator input and hence, they are not attenuated by the action of feedback. Among others, some errors belonging to this family are: clock jitter error, circuit noise (both thermal and flicker components), and harmonic distortion caused by circuit nonlinearities.

In the case of CT-$\Sigma\Delta$Ms, circuit errors can be divided into two main categories [14], [66]:

- *Building-block errors*, which are the nonideal effects derived from the modulator loop filter implementation—similar to the SC case—such as finite opamp dc gain (for active-RC implementations), integrator time-constant error, integration incomplete transient response, circuit element tolerances, circuit noise, nonlinearities (especially those affecting front-end circuitry like input voltage-to-current Gm-C integrators), etc., [10], [66], [69], [81]–[83].
- *Architectural timing errors*, namely: quantizer metastability, excess loop delay, and clock jitter error [10], [66], [84]–[91].

The former group of errors cause similar effects on the performance of CT-$\Sigma\Delta$Ms as in the case of their DT counterparts. Hence, they can also be classified according to the way they degrade this performance, either causing a deviation in NTF(f) or as additive noise sources. However as stated above, SC implementations have intrinsically lower parameter variations, since most circuit parameters are defined by capacitor ratios instead of absolute parameter values as it is the case of CT circuits. In contrast, CT implementations are potentially faster than SC ones, leading to much more relaxed designs (in terms of power consumption) when high-speed operation is required. For instance, it can be shown that the unity-gain frequency, f_u, of active-RC integrators can be chosen to be in the range of f_s, or even well below f_s, depending on the chosen scaling coefficient [92]. However, typical requirements in DT-$\Sigma\Delta$Ms lead to $f_u \simeq 5f_s$ [34].

In spite of the potential advantage of CT-$\Sigma\Delta$Ms to operate at higher frequencies with less power consumption than their DT counterparts, their performance—particularly in high-speed applications—is largerly impacted by timing errors listed above. The first one—*quantizer metastability*—is essentially due to the variation of comparison time with the input signal—[85]. This effect can be circumvented by including latches between the quantizer and the feedback DAC. Clocking each latch stage on the opposite clock phase from the previous one gives the previous stage a good deal of time to settle. The price to pay is the additional delay introduced in the feedback loop [66]. Indeed, the effect of metastability is a critical issue as the clock frequency increases and the timing errors become limiting factors. However, the use of multiple latches has been demonstrated very effective even for sampling frequencies in the GHz range [93].

The second important timing error is caused by the delay introduced due to the finite transient response of the quantizer and the DAC circuitry in the modulator loop filter response [84]. This delay is often referred to as *excess loop delay*, and mathematically expressed as a fraction of the sampling period, i.e., $\tau_d = \rho_d T_s$. The excess loop delay error introduces additional poles that increase the order of both STF and NTF, which may lead to an unstable behaviour of the resulting CT-$\Sigma\Delta$M. In order to compensate for the effect of excess loop delay, a number of techniques have been reported in literature [94]. Among others, the most commonly used strategies are based on including additional feedback DACs—with their corresponding scaling coefficients—in order to cancel out the additional poles of NTF [53].

Among all timing errors affecting the performance of CT-$\Sigma\Delta$Ms, the most critical one is caused by uncertainties in the clock-signal edges as illustrated in Fig. 21(a)—commonly referred to as *clock jitter* [66]. This error occurs at those points within the modulator architecture where signals are transformed from the CT- domain into the DT- domain and *vice versa*, i.e., at the S/H and reconstruction DAC, respectively as illustrated in Fig. 21(a). The error introduced by S/H is attenuated within the signal band by the modulator noise-shaping effect, and can hence be neglected. However, the jitter error at the DAC—illustrated in Fig. 21(b) for a NRZ and RZ waveforms—occurs without attenuation at the input node, thereby limiting modulator accuracy. The main reason why CT-$\Sigma\Delta$Ms are more sensitive to clock jitter than DT-$\Sigma\Delta$Ms is illustrated in Fig. 21(c), where a typical SC DAC waveform is compared to a CT current-mode waveform. Note that, in the SC case, most of the charge transfer occurs at the start of the clock period, so that the amount of charge lost due to a timing error is relatively small as compared to the total amount of transferred charge. By contrast, in CT-$\Sigma\Delta$Ms, charge is transferred at a constant rate over a clock period, and hence, charge loss from the same timing error is a larger portion of the total charge [95]. The importance of clock jitter error has prompted a significant interest in the open literature as demonstrated by the large number of papers devoted to this topic [10], [66], [86]–[89], [91], [96], [97].

The study of clock jitter and other nonlinear timing/architectural errors may require using specific analytical techniques like *state-space formulation* [86] and/or simulation-based analyses, in order to get *semi-empirical* closed-form design equations relating the error parameters with the effective resolution of the modulator. By contrast, in the case of those nonideal effects as-

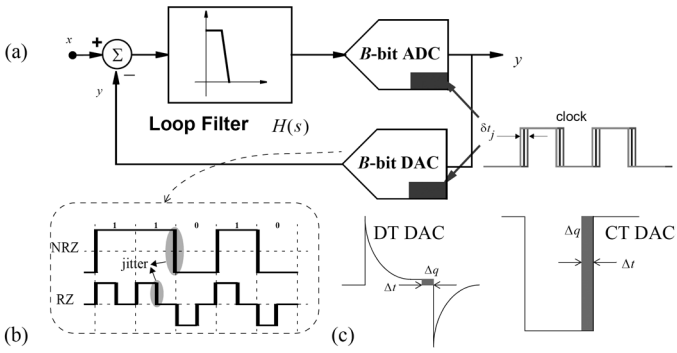

Fig. 21. Clock jitter in CT-$\Sigma\Delta$Ms. (a) Main error sources. (b) 1-bit RZ versus NRZ DAC waveforms. (c) DT versus CT feedback DAC waveforms.

sociated to building blocks, the general procedure commonly used to analyse their impact on the performance of the modulator is the following [7], [14]:

- Obtain an integrator equivalent circuit taking into account the nonideal effect under study.
- Analyse the impact of the nonideality on the integrator transfer function, i.e., $H(z)$ for SC integrators and $H(s)$ for CT integrators, such that $H(z), H(s) \rightarrow H(z,\epsilon), H(s,\epsilon)$, with ϵ being the error vector including all nonideal parameters involved in the integrator circuit equivalent obtained in previous step.
- In order to compute the effect of ϵ on a $\Sigma\Delta$M, the integrator transfer functions are replaced with $H(z,\epsilon), H(s,\epsilon)$, and a linear model of the quantizer is consider to get the nonideal NTF, i.e., NTF(z, L, ϵ) and NTF(f, L, ϵ) for SC and CT $\Sigma\Delta$Ms, respectively.
- The nonideal NTF is integrated within the signal band in order to obtain the in-band noise power as: $P_{Q,\epsilon} = \int_{\text{Signal Band}} (\Delta^2)/(12 f_s) |\text{NTF}(f, L, \epsilon)|^2 df$, which, after some approximations can be explicitly expressed as a function of ϵ and the modulator parameters, i.e., $B, L,$ OSR. Note that, once $P_{Q,\epsilon}$ is known, the corresponding nonideal expressions of DR and SNR can be obtained from their definitions given in (7), respectively.

A detailed description of the above procedure for each $\Sigma\Delta$M nonideality is beyond the scope of this paper and can be found in a number of manuscripts [14], [15]. However, it should be noted that the analysis of circuit errors is extremely important for a designer of $\Sigma\Delta$Ms for three main reasons:

- First, it allows designers to obtain approximate design equations which, in closed-form, express the effect of each nonideality on the performance of both building blocks and the modulator themselves.
- Second, compact expressions that relate architectural parameters (L, OSR, B) with main circuit nonideal effects (mainly finite dc gain, capacitor mismatch, GB, and SR) and technological features can be used in a systematic design procedure to make accurate system-level estimations of the power consumption of different $\Sigma\Delta$M topologies. This analysis is usually done at the earlier phases of the design flow in order to decide the best $\Sigma\Delta$M architecture for a given set of specifications.
- Finally, a precise analysis of errors yield to the obtainment of accurate behavioral models that support fast and precise time-domain simulations, which constitute an essential part of the systematic design procedure of $\Sigma\Delta$ ADCs as detailed in the following sections.

C. Design Methodologies for $\Sigma\Delta$Ms

The design of high-performance $\Sigma\Delta$ ADCs using nanometer CMOS technologies demands for proper design methodology and CAD tools which can optimize the design procedure in terms of efficiency and time-to-market deployment. To this purpose, a number of design methods and tools have been reported for the synthesis of $\Sigma\Delta$Ms [7], [13], [98]–[100]. The majority of them are based on the well-known *top-down/bottom-up* hierarchical design methodology [98]. The design process of a $\Sigma\Delta$M starts from the modulator specifications (essentially effective resolution and signal bandwidth). The first step is the selection of the modulator architecture and NTF that satisfy these specifications. At this step, ideal design equations like (4) and (7)—based on a linear model of the embedded quantizer—can be used to obtain approximate values for the main $\Sigma\Delta$M parameters (OSR, L and B). Once these values have been obtained, more accurate nonlinear models should be used. To this purpose, the well-known Schreier's MATLAB Delta-Sigma toolbox [13], [24] is widely used by the $\Sigma\Delta$M community. After the modulator architecture has been synthesized, the *top-down* design starts with the decomposition of the $\Sigma\Delta$M specifications into a subset of specifications for each system's building blocks. This procedure is known as translation or *mapping of specifications*. This process ends at the bottom level, where active (transistors) and passive (resistors, capacitors, and inductors) devices compose the lower level of abstraction of the blocks. The reverse path—*the bottom-up* process—begins by designing the individual cell-level blocks and ends with the assembly of the system-level circuit.

Fig. 22 shows an example of the application of the hierarchical top-down/bottom-up methodology to the design and synthesis of $\Sigma\Delta$Ms [7]. At each hierarchy level, optimization can be combined with simulation to transmit the specifications to the lower level, i.e., to implement the sizing process at different levels of the modulator hierarchy. Two different synthesis tasks can be distinguished in Fig. 22, namely: *high-level sizing* and *cell-level sizing*. High-level sizing is the process by which building-block nonideal specifications (described in previous sections, like for instance opamp dc gain, output swing, GB, SR, etc.) are obtained as a function of the modulator-level specifications, i.e., effective resolution and signal bandwidth. In the next step, often referred to as cell-level sizing, an electrical (SPICE-like) simulator can be combined with an optimizer to find out the transistor sizes and biasing for given block specifications and minimum power consumption.

Note from Fig. 22 that at cell level, for each subblock, i.e., amplifiers, transconductors, comparators, capacitors, switches, etc. an appropriate topology and/or element arrangement need to be chosen and specification transmission at this lowest hierarchical level directly yield device sizes and bias voltages and currents. In practice, the implementation of this methodology takes into account multiple redesign iterations in case of performance specifications are not fulfilled. At each iteration, circuit performances are evaluated at a given point of the design pa-

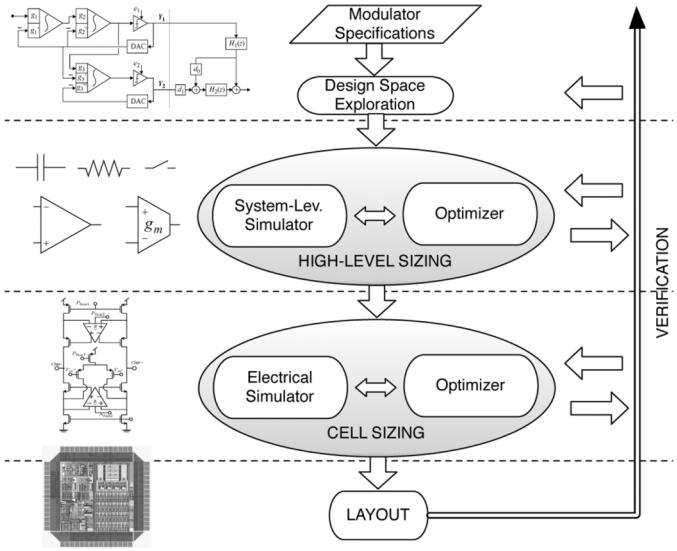

Fig. 22. Top-down/bottom-up design approach applied to $\Sigma\Delta$Ms.

rameter space. According to such an evaluation, a movement is generated in the design space and the process is repeated again [100].

D. Behavioral Modeling and Simulation of $\Sigma\Delta$Ms

The iterative nature of the synthesis procedure described above—usually needing a large number (hundreds or even thousands) of iterations—demands for efficient simulation techniques in terms of CPU time and accurate performance evaluation. In the case of $\Sigma\Delta$Ms, long transient simulations are required to evaluate their main performance specifications because they are nonlinear oversampled-data systems. Therefore, transient analyses involving thousands of clock cycles are typically needed to obtain their main figures of merit, like in-band noise power or SNR. For this reason, transistor-level simulations using SPICE-like simulators yield excessively long CPU times—typically several days, or even weeks. To cope with this problem, different alternatives of dedicated simulators—based on using *macromodels* and/or *multilevel* simulation—have been developed, which at the price of reducing the accuracy in their circuit-element models, increase the simulation speed [7], [99], [101], [102]. Among others, one of the best accuracy-speed trade-offs is achieved by using the so-called *behavioral simulation technique* [102]. In this approach the modulator is broken up into a set of subcircuits, often called *building blocks* or basic blocks. These building blocks are described by equations that express their outputs in terms of their inputs and their internal state variables [98]. Thus, the accuracy of the simulation depends on how precisely those equations—considering the nonideal and nonlinear circuit error mechanisms discussed in previous section—describe the actual behavior of each building block [100], [103]–[105].

Some authors have proposed different approaches for the implementation of behavioral modeling and simulation of $\Sigma\Delta$Ms in the MATLAB/SIMULINK platform [100], [106]–[108]. The use of SIMULINK for the behavioral modeling and simulation of SC $\Sigma\Delta$Ms was first reported in [106] and [107]. The models included in this toolbox [109]—based on the interconnection of SIMULINK standard library blocks—are very intuitive and useful for system-level evaluation. The block library contains only SC circuit models, implemented using MATLAB (M-type) files, with the subsequent penalty in computation time [110], [111]. Another approach consists of using the so-called C-coded *S-functions* [112] to implement time-domain behavioral models in SIMULINK [100].[18] The use of *S-functions* allows to decrease the computational cost to acceptable values for synthesis purposes. For example, the simulation of 2^{16} clock periods of a cascade 2-1-1 SC $\Sigma\Delta$M considering behavioral models with all circuit nonidealities takes a few seconds and it is about 50 times faster than the approach based on using M-file models.

E. From Systems to Circuits

Once the modulator architecture satisfies the required specifications, the next step consists of translating the system-level behavioral model to a circuit-level design, firstly using macromodels and finally a transistor-level implementation. This way, $\Sigma\Delta$M designers can analyse and verify the modulator performance at different stages of the design phase, combining the effect of those building blocks which have been designed (at the transistor level) with those ones which have not been sized yet. To this purpose, electrical simulations—normally using SPICE-like simulators—are carried out to check the modulator performance during different steps of the design process, with no excessive CPU time—typically a few hours. At initial steps of the design procedure, only macromodels (that include main circuit error limitations) are used. In the end, all subcircuits have been sized and a complete transistor-level simulation is required in order to verify the performance of the whole modulator.

The cell-sizing process for different modulator subcircuits can be carried out by following an optimization-based procedure as illustrated in Fig. 22, in which building-block specifications—extracted from the high-level sizing process—are mapped into transistor sizing and biasing. At this design step, potential circuit candidates (for instance different OTA topologies) are explored and the effect of technology corners, temperature variations, and supply voltage tolerances are taken into account. The final verification of the whole modulator schematic must take into account worst-cases of different subcircuits in order to guarantee a correct performance of the circuit.

V. Frontiers of $\Sigma\Delta$Ms and State-of-the-Art Nanometer CMOS ICs

Since the introduction of $\Sigma\Delta$ modulation, there has been a huge number of ICs published, implemented using many diverse technology processes, architectural and circuit techniques, and targeting a number of different applications.[19] To conclude this paper, this section gives an overview of recent state-of-the-art $\Sigma\Delta$Ms, focusing on those ICs implemented in nanometer (beyond 180 nm) CMOS technologies.

[18]The behavioral simulator based on this approach, called SIMSIDES, is freely distributed by the IMSE $\Sigma\Delta$ research group under confidentiality conditions.

[19]As an illustration of the immense number of papers dealing with $\Sigma\Delta$Ms, a search at IEEE *Xplore* using keywords "sigma" and "delta" gave over 4800 results!

TABLE I
STATE-OF-THE-ART SINGLE-LOOP LOW-PASS DT-$\Sigma\Delta$Ms

Ref.	DR (bit)	DOR (MS/s)	OSR	l(nm)	P_w (mW)	FOM_1	FOM_2
SINGLE-BIT QUANTIZATION							
[117]	13.8	0.04	100	180	0.04	0.06	588.15
[118]	11.5	0.04	64	180	0.42	3.63	1.99
[119]	12.2	0.016	64	180	0.08	1.06	11.05
[120]	13.1	0.2	520	130	1.28	0.73	30.18
	9.9	1.00	104			1.33	1.79
	8.1	2.00	52			2.32	0.29
[121]	13.5	0.04	50	130	0.06	0.13	236.07
[122]	14.4	0.04	100	90	0.13	0.15	358.94
MULTI-BIT QUANTIZATION							
[123]	13.7	25	8	180	200	0.60	55.26
[124]	13.8	6	96	180	15	1.75	20.31
[125]	13.8	4	8	180	149	2.61	13.63
[126]	14.0	4.4	33	180	13.8	0.19	213.63
[127]	13.9	2.2	60	180	5.4	0.16	237.63
[128]	16.3	0.05	100	180	0.9	0.17	1228.36
[129]	14.4	3	350	130	8	1.26	41.96
	13.4	1.1	47		7	0.60	43.96
[130]	15.0	0.048	128	130	1.5	0.95	85.76
[131]	11.3	8	13	90	11.8	0.60	10.35
[132]	10.7	3.88	20	90	1.2	0.19	22.33

TABLE II
STATE-OF-THE-ART SINGLE-LOOP LOW-PASS CT-$\Sigma\Delta$Ms

Ref.	DR (bit)	DOR (MS/s)	OSR	l(nm)	P_w (mW)	FOM_1	FOM_2
SINGLE-BIT QUANTIZATION							
[93]	12.4	2.46	813	180	18	1.35	9.96
[133]	14.6	2	32	180	4.7	0.09	655.02
[134]	12.3	1.0	64	180	4.4	0.87	14.43
[135]	14.5	2.0	32	180	2	0.04	1340.03
[136]	15.6	0.048	128	180	0.11	0.05	2686.76
	14.8	0.048	128		0.12	0.09	799.12
[137]	12.0	0.05	64	180	0.37	1.81	5.66
[138]	12.5	2.0	140	180	6	0.52	27.92
[139]	11.3	4.0	38	180	6	0.65	9.62
[140]	11.4	0.86	150	110	3.42	1.51	4.38
	10.4	2.6	50		3.42	0.99	3.32
[141]	11.3	3.84	81	90	12.5	1.26	5.12
[142]	14.0	1.2	213	90	5.4	0.27	148.89
MULTI-BIT QUANTIZATION							
[143]	8.9	40	5	180	103	5.39	0.22
[144]	15.2	0.048	64	180	0.09	0.05	1886.06
[145]	13.3	20	32	180	100	0.50	50.78
[146]	12.0	4	26	130	3	0.18	55.83
[147]	13.0	40	16	130	20	0.06	335.01
[148]	11.0	30	10	130	70	1.14	4.49
[149]	10.0	3.84	48	130	3.1	0.79	3.24
[150]	14.0	0.24	54	130	3.0	0.76	53.60
[151]	11.7	40	25	130	40	0.30	27.63
[152]	10.0	4	26	120	3	0.73	3.49
[153]	11.3	20	15	110	5.3	0.11	59.65
[154]	12.5	1.2	42	90	6	0.86	16.75
[155]	13.2	16	16	65	50	0.33	70.73
[156]	11.2	36	32	65	17	0.20	29.3
	11.8	18	64		17	0.26	33.60
	12.6	9	128		17	0.30	50.93
	11.5	9	64		8	0.31	23.56

Tables I–V sum up the performance of the state-of-the-art $\Sigma\Delta$M ICs reported so far. They have been classified according to their architecture/circuit characteristics into: LP DT (Table I), LP CT (Table II), cascade (Table III), BP (Table IV), and reconfigurable $\Sigma\Delta$Ms (Table V). In all cases, the performance of each reported IC is summarized in terms of:

- DR achieved by the $\Sigma\Delta$M, measured in bits.

TABLE III
STATE-OF-THE-ART CASCADE $\Sigma\Delta$Ms

Ref.	DR (bit)	DOR (MS/s)	OSR	l(nm)	P_w (mW)	FOM_1	FOM_2
SC IMPLEMENTATIONS							
[157]	12.2	20	4	180	240	2.55	4.60
[158]	13.4	0.2	195	130	2.4	1.11	24.30
	10.4	3.84	100		4.3	0.83	4.07
[159]	8.5	80	4	130	175	6.04	0.15
[160]	11.4	40	11	90	27.9	0.26	26.13
[161]	10.8	40	8	90	78	1.09	4.07
[162]	9.4	4	10	90	2.1	0.79	2.08
	10.7	2	20			0.63	6.58
	12.5	0.4	50			0.91	15.95
CT IMPLEMENTATIONS							
[40]	10.9	20	8	180	122	3.27	1.43
	10.9	40			216	2.89	1.62
[43]	11.0	36	10	180	183	2.48	2.06
[41]	12.5	40	9	90	56	0.24	59.82
[42]	9.8	30	7	65	10.5	0.39	5.67
	11.3	20	10.4			0.21	30.2

- *Digital output rate* of the ADC, defined as DOR $\equiv 2B_w$; i.e., the Nyquist rate after decimation, measured in megasamples per second (MS/s).
- Notch frequency, f_n, in the case of BP-$\Sigma\Delta$Ms.
- Oversampling ratio, OSR.
- Minimum length for MOS transistors in the technology process (l).
- Power consumption[20] of the $\Sigma\Delta$M, represented by P_w.

The above performance is quantified in terms of their main specifications (effective resolution, signal bandwidth, and power consumption of the circuit) through the following figures of merit (FOMs), respectively proposed by [113], [114], and [115][21]

$$\text{FOM}_1|_{\text{pJ/conv}} \equiv \frac{P_w(\text{W})}{2^{\text{ENOB(bits)}} \cdot \text{DOR(S/s)}} 10^{12} \tag{13}$$

$$\text{FOM}_2 \equiv 2 \cdot k \cdot T \frac{3 \cdot 2^{2 \cdot \text{ENOB(bits)}} \cdot \text{DOR(S/s)}}{P_w(\text{W})} \tag{14}$$

where k is the Boltzmann constant and T is the circuit temperature (measured in K). FOM_1 emphasizes power consumption, whereas FOM_2 emphasizes effective resolution. The smaller the FOM_1 value and the larger the FOM_2 value,[22] the "better" the $\Sigma\Delta$M is.

The following observations can be made from Tables I–V:

- Although SC circuit techniques have been traditionally used in most reported $\Sigma\Delta$Ms, more and more ICs are being implemented using CT circuits, especially in those applications targeting wideband signals and/or requiring low power consumption.

[20]The data corresponding to P_w accounts only the $\Sigma\Delta$M, excluding the consumption of the decimation filter.

[21]Choosing the appropriate FOM is always a matter of discussion. In this paper (13) and (14) have been used because they are widely considered by the majority of the ADC community [116]. It should be noted that, according to (10), DR was used to compute ENOB. However, in those ICs presenting strongly nonlinear behavior, ENOB is limited by $\text{SNDR}_{\max}$ as stated in Section II.E and hence, its corresponding FOM is worse than the one shown in the tables.

[22]FOM_2 has been multiplied by a scale factor of 10^5 in Tables I–III.

TABLE IV
STATE-OF-THE-ART BAND-PASS $\Sigma\Delta$Ms

Ref.	DR (bit)	f_s, f_n (MHz)	DOR (MS/s)	l(nm)	P_w (mW)	FOM_1
SC IMPLEMENTATIONS						
[163]	14.4	60,40	5	180	150	1.39
[164]	18.3	37,10.7	0.006	150	208	107
	15.3	37,10.7	0.4			12.9
	14.5	37,10.7	0.8			11.2
CT IMPLEMENTATIONS						
[75]	14.7	264,44	17	180	375	0.83
[165]	11.0	48,2	2	180	2.2	0.54
[166]	11.3	800,200	20	180	160	3.17
[167]	19.3	41.7,10.7	0.006	180	210	54.2
	16.0	41.7,10.7	0.4			8.0
	14.0	41.7,10.7	1			12.8
[76]	10.0	3000,2400	128	90	40	0.33

TABLE V
STATE-OF-THE-ART RECONFIGURABLE $\Sigma\Delta$Ms

Ref.	Std.	DR (bit)	DOR (MS/s)	l(nm)	P_w (mW)	FOM_1
SC IMPLEMENTATIONS						
[168]	AMPS	15	0.036	180	30	22.1
	GSM	13.2	0.4		30	5.4
	CDMA	12.5	1.35		30	2.9
	UMTS	11.4	3.84		50	2.8
[169]	GSM	14.3	0.2	130	23.9	0.7
	UMTS	12.8	3.84		24.5	0.3
	WLAN	10.8	20		44.5	0.6
[170]	GSM	14.1	0.2	130	2	0.6
	UMTS	12.5	3.84		5.2	0.2
	LTE	12.2	10		13.6	0.3
		11.6	20		20.2	0.3
		11.4	40		34.7	0.3
[171]	GSM	13.8	0.2	90	3.4	1.2
	Bluetooth	12.5	1		3.7	0.6
	UMTS	10.7	4		6.8	1.0
[172]	GSM	12.7	0.2	90	4.6	3.5
	Bluetooth	11.3	1		5.3	2.1
	GPS	11.6	2		6.2	1.0
	UMTS	10.7	4		8.0	1.2
	DVB-H	10.1	8		8.0	0.9
	WiMAX	8.5	10		11.0	1.6
CT IMPLEMENTATIONS						
[95]	GSM	15.0	0.4	180	9.0	0.69
	Bluetooth	13.5	2.46		8.2	0.29
	UMTS	12.0	7.68		7.6	0.24
[173]	GSM	13.3	0.4	90	1.4	0.35
	Bluetooth	12.2	2		3.4	0.37
	WLAN	8.3	20		7.0	1.07
[174]	Bluetooth	13.5	1	90	5.0	0.43
	UMTS	12.7	3.84		6.4	0.26
	DVB	11.7	4		5.5	0.21
	WLAN	10.8	10		6.8	0.19
[32]	EDGE	14.3	0.27	65	2.6	0.47
	CDMA	13.3	1.23		3.1	0.25
	UMTS	11.8	3.84		3.7	0.26

- CMOS 180 nm standard process has been the technology most commonly employed in recent years, mainly using a single 1.8-V supply voltage.
- Single-loop architectures have been more used than cascade topologies. The latter have been mainly implemented using SC circuits, although recent synthesis methods are making the implementation of CT cascade ICs possible.
- Multibit quantization is more employed than single-bit quantization. The majority of cascade topologies include dual quantization with a multibit quantizer in the last stage. However, increasingly more circuits are including multibit ($B = 2, 3, 4$) quantizers in all stages combined with proper DEM strategies.
- Signals with maximum bandwidths in the order of 10–40 MHz are being handled with DR $\simeq$ 11–13 bits.

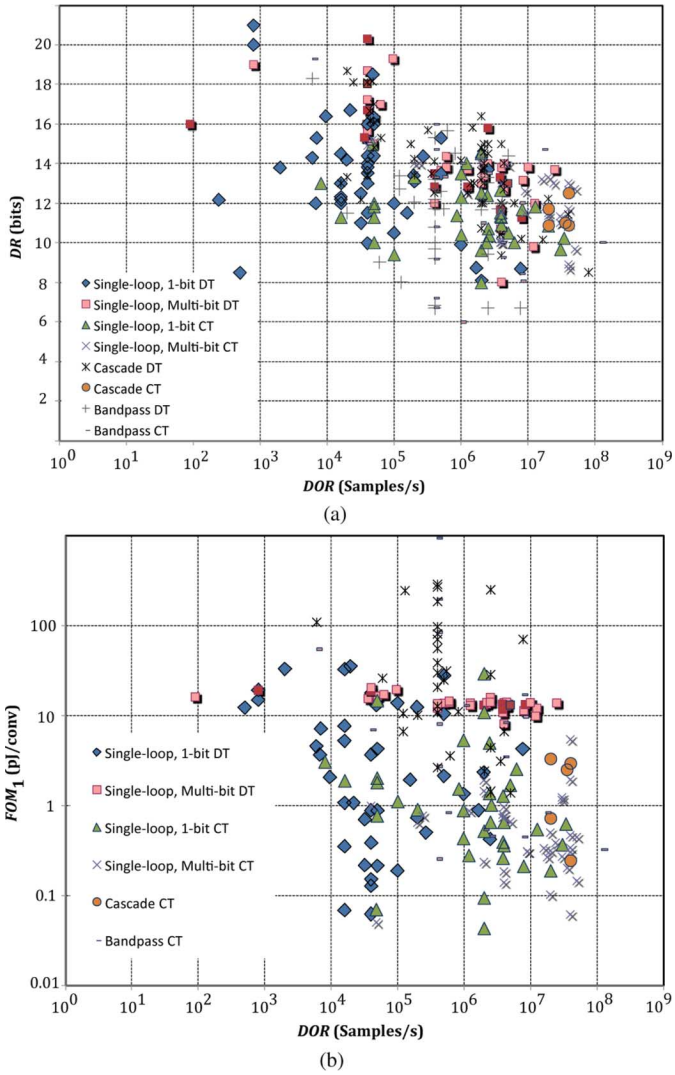

Fig. 23. State-of-the-art CMOS $\Sigma\Delta$M performance. (a) DR versus DOR. (b) FOM_1 versus DOR.

As an illustration, Fig. 23 represents DR versus DOR [Fig. 23(a)] and FOM_1 versus DOR [Fig. 23(b)] for the different families of $\Sigma\Delta$ ADCs. For the sake of completeness, the data[23] contained in Fig. 23 include also the results reported by most state-of-the-art CMOS $\Sigma\Delta$Ms published in the last 15 years. It can be noted that a wide DR-versus-DOR *conversion region* is covered, ranging over six decades in frequency and more than 15 bits in the DR axis.

Fig. 24 compares the state-of-the-art performance of $\Sigma\Delta$Ms with the one achieved by other ADC architectures. The data in this figure were collected from Murmann's ADC survey [175], as well as those used in Fig. 23. It can be observed from Fig. 24(a) that $\Sigma\Delta$ ADCs cover the widest DOR range,

[23]This data are available online at http://www.imse-cnm.csic.es/~jrosa/CMOS-SDMs-Survey-IMSE-JMdelaRosa.xls.

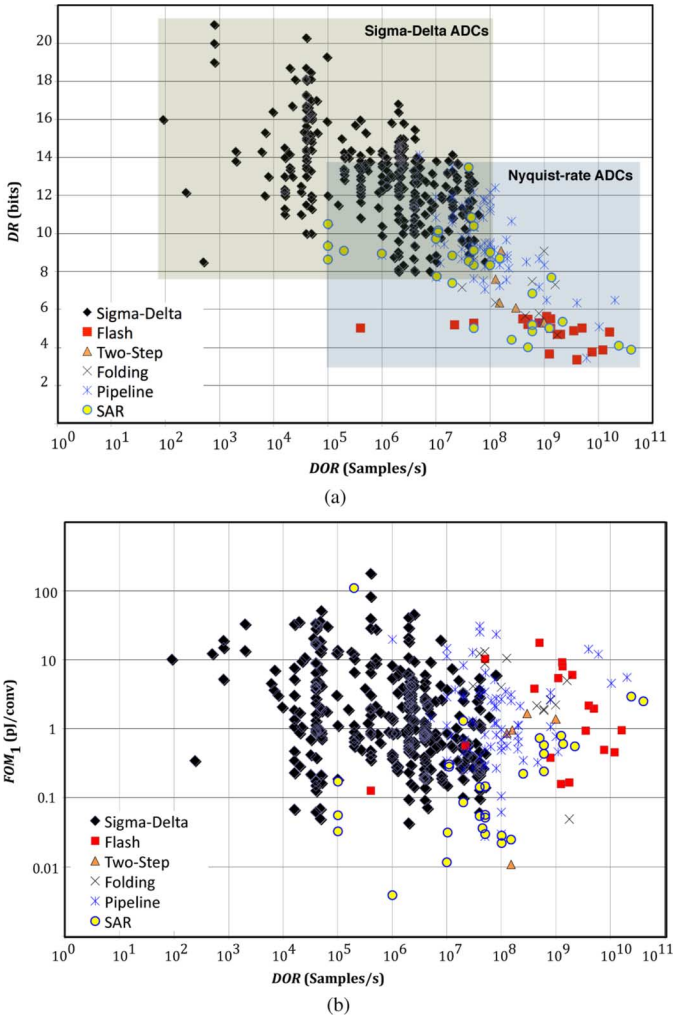

Fig. 24. Comparison of the state-of-the-art performance of ΣΔM-based ADCs and Nyquist-rate ADCs. (a) DR versus DOR. (b) FOM_1 versus DOR.

ranging from hundreds of S/s to hundreds of MS/s, while higher frequencies are dominated by Nyquist-rate ADCs.

In terms of FOM_1 [Fig. 24(b)], ΣΔ ADCs show a better performance up to DORs in the order of 100 kS/s, while SAR ADCs show similar results (even better in some cases) up to DOR $\simeq$ 100 MS/s. ΣΔMs are less efficient for DOR $>$ 10 MS/s, partially due to the low values of OSR used for these operation speeds. Nevertheless, as illustrated in Fig. 24(a), the DR-versus-DOR area covered by ΣΔ ADCs is larger than the one dominated by Nyquist-rate ADCs. The tendendy is toward extending the range of specifications covered by ΣΔ ADCs, particularly increasing DOR. The following subsections present a review of some relevant trends, challenges, and strategies used in cutting-edge ΣΔMs intended for low-voltage wideband telecom applications.

A. Sturdy MASH ΣΔMs and Unity STF

A good alternative to cascade ΣΔM architectures that reduces the sensitivity to noise leakage is the so-called *sturdy* MASH (SMASH) [176], [177]. In this architecture, illustrated in Fig. 25(a) for a 2-stage cascade topology, where $H(z) = z^{-1}/(1 - z^{-1})$, the modulator output can be obtained from the direct digital subtraction of the two stages outputs, with no

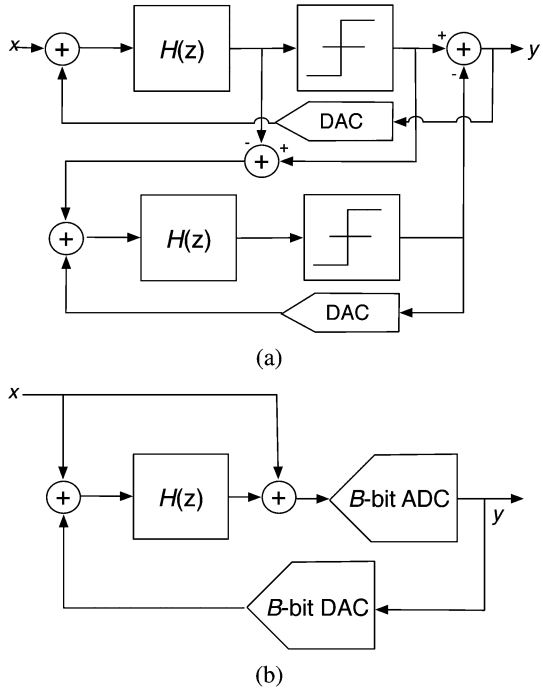

Fig. 25. (a) SMASH ΣΔM [177]. (b) ΣΔM with USTF [179].

need of digital filtering—used in conventional MASH topologies—and therefore, the subsequent elimination of matching requirements between analog and digital filtering. This concept of cascade ΣΔMs has been recently extended to multistage cascade architectures in [178].

The performance of SMASH ΣΔMs can be notably improved if unity STF (USTF) is implemented in all stages of the modulator as proposed in [180]. The concept of USTF is illustrated in Fig. 25(b) [179], [181]. An extra feedforward path is included from the input node to the quantizer input. This way, using a linearized model for the quantizer, it can be shown that STF $= 1$, whereas NTF becomes unaffected by the extra feedforward path. The main advantage of using USTF is that integrators ideally process quantization error only and hence, their output swing can be reduded and the tolerance to amplifiers nonlinearities is increased. One of the main drawbacks of applying USTF to CT-ΣΔMs is that the resulting modulators do feature a worse implicit AAF function.

Fig. 26 shows a ΣΔM architecture that extends the underlying principle of SMASH ΣΔMs to the implementation of USTF in both stages, thus taking advantage of both strategies (SMASH and USTF) to achieve larger SNDR at lower values of OSR with relaxed output swing and gain demands in the amplifiers, while keeping a better sensitivity to mismatch than simple SMASH and cascade topologies. However, a front-end DAC with a full scale larger than that of the quantizers in the cascade (with resolutions B_1 and B_2) is required in order to account for the summation of the digital output of the stages. Nevertheless, the location of the digital adder helps to increase considerably the robustness to capacitor mismatches [180].

B. Time-Enconding Quantizers

In addition to increasing the bandwidth of digitized signals, significant efforts have been carried out in recent

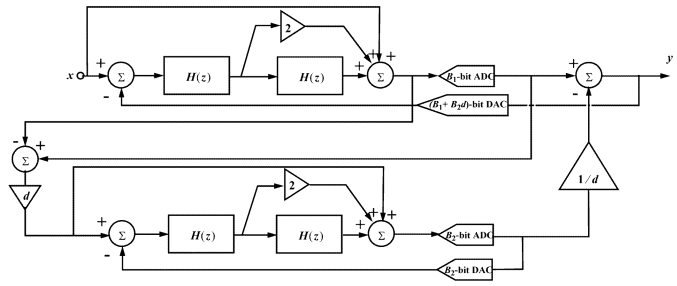

Fig. 26. SMASH $\Sigma\Delta$M with USTF proposed in [180].

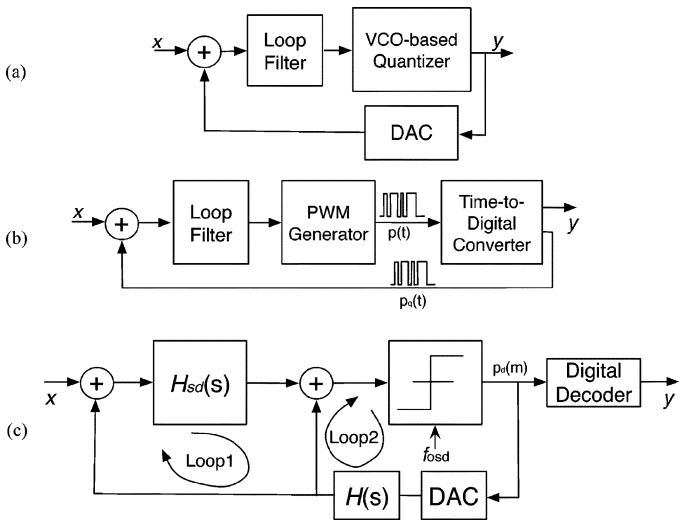

Fig. 27. $\Sigma\Delta$Ms with *time-coded* quantizers. (a) VCO [151]. (b) PWM [184]. (c) TEQ [185].

years to improve the performance of the embedded multibit quantizers—used in most state-of-the-art $\Sigma\Delta$Ms shown in Tables I–V. These quantizers are usually implemented by flash ADCs, made up of a resistive ladder and a bank of comparators. As well known, the number of comparators increases exponentially with B, with the subsequent penalty in silicon area and power dissipation. An alternative technique to reduce the number of comparators is based on the so-called *tracking quantizer* [146], that uses a counter and a switching matrix to connect the reference voltage to the comparators' inputs according to the value of the quantizer input ranges. Nevertheless, the implementation of flash ADCs in nanometer CMOS technologies is limited by the low voltage supply since their dynamic range is reduced as a consequence of the comparator offset and hysteresis [182].

These problems have motivated the exploration of alternative implementations of multibit quantizers. Most of them are based on changing the concept of signal quantization, going from an amplitude coding to a time coding. Hence, the resulting quantization methods are more suited for the implementation in low voltage (< 1 V) nanometer CMOS processes [183], although special care must be taken in terms of clock jitter sensitivity.

There have been essentially three alternative implementations of *time-coded* quantizers successfully reported in state-of-the-art ICs and illustrated in Fig. 27: VCO-based quantizers [Fig. 27(a)] [151], pulsewidth modulation (PWM) [184] [Fig. 27(b)], and time-encoding quantizer (TEQ) [185] [Fig. 27(c)].[24]

The use of a voltage-controlled oscillator (VCO) instead of a multibit quantizer is based on the idea of translating the quantized information in the amplitude domain to the time-domain by means of a voltage-to-frequency conversion, which is implemented in a VCO [151]. The main problem of this quantizer is the nonlinear operation introduced by the VCO. This limitation can be mitigated by using a phase detector instead of a frequency detector as proposed in [187].

An alternative to VCO-based quantizers consists of using PWMs [184]—conceptually shown in Fig. 27(b). The PWM converts the voltage at the output of the loop filter to a pulse $p(t)$ with corresponding width, and a time-to-digital converter (TDC) generates digital codes that are discrete representations of the edges of the $p(t)$ signal, i.e., a time-quantized representation.

One of the main limitations of PWM-based quantizers is their limited dynamic range [182]. This can be enhanced by using the so-called *time-enconding quantizer* (TEQ) as illustrated in Fig. 27(c) [185]. Essentially, the idea underlying TEQ-based $\Sigma\Delta$Ms consists of using a modulator (a CT-$\Sigma\Delta$ in the figure) whose loop filter is split into two loops, one of which is made to oscillate, thus providing an independent control of the oscillation as a difference with PWM-based quantization schemes [188].

C. Digital-Based Loop Filters

Innovations are being carried out not only at architectural level as described above, but also at circuit level. Thus, there has been an increased interest to explore digital (nanometer) CMOS *compatible* circuit techniques to implement the critical $\Sigma\Delta$M building blocks [189]. This is the case of the comparator-based [118] and inverter-based [117], [189] integrators used in $\Sigma\Delta$Ms, in which their embedded operational transconductance amplifiers are replaced by comparators and inverters, respectively.

In addition to the mentioned circuit techniques, there are other alternative digital-based solutions that can be used for the implementation of the $\Sigma\Delta$M loop filter. This is the case of the variable-rate CT-$\Sigma\Delta$M recently proposed in [156]. The circuit is based on a digitally background calibrated ring oscillator with its inverters sampled at the required output sample-rate, without containing analog integrators, comparators or feedback DACs. The advantage of these techniques is twofold. On the one hand, the use of digital circuits benefits from technology downscaling, and particularly their associated power supply reduction. On the other hand, there is a reduction in the power consumption, which is an important advantage in applications like wireless telecom hand-held devices.

D. Reconfigurable $\Sigma\Delta$Ms for Software Defined Radio

$\Sigma\Delta$Ms are very suited for the implementation of reconfigurable ADCs in highly integrated multistandard wireless transceivers using low-cost *digitally oriented* CMOS technologies. Indeed, the combination of different architectural—and circuit

[24]An alternative implementation of transforming amplitude into time information for quantifying and coding signals consists of removing the clock from the $\Sigma\Delta$M loop, giving rise to the so-called *asynchronous* $\Sigma\Delta$Ms [186].

strategies overviewed in this paper, together with the variation of $\Sigma\Delta$M basic parameters, i.e., OSR, L, and B, can contribute to adapt the ADC performance to different specifications with large hardware reuse [172].

Several state-of-the-art multistandard $\Sigma\Delta$Ms—summarized in Table V—are able to handle more than three standard specifications [168], [170], [172], [174]. However, the increasing number of coexisting wireless standards together with the trend towards the implementation of future *software defined radio (SDR)* demands for *flexible* ADCs with the ability to adapt their performance metrics and even to reconfigure system/circuit topology dynamically, depending on the required transmit/receive parameters [174].

Although pushing the analog-digital interface as close as possible to the antenna—an approach commonly referred to as *RF digitization*—is the most evident implementation of a SDR receiver [190], the resulting specifications for the data converters lead to unfeasible power-hungry solutions for practical mobile handsets—where reduced power consumption is a must. However, several BP-$\Sigma\Delta$Ms have been recently reported which—based on digitizing only the desired channel—may result in very promising candidates for the implementation of *mostly-digital* RF transceivers [76], [163], [164], [166], [191], [192]. A good example is the BP-$\Sigma\Delta$M proposed in [76]. The circuit uses the undersampling technique [193] to digitize signals centered at 2.4-GHz with $f_s = 3$ GHz. Recently, the concept of IF digitization based on SC BP-$\Sigma\Delta$Ms has been successfully demonstrated in [166] and [191], the latter being able to program f_n from dc to $0.31f_s$.

The use of $\Sigma\Delta$M techniques for SDRs may benefit from CT circuits to implement radio functions like blocker-rejection filtering, frequency-mixing process, channel-selection and antialiasing filtering, etc [135], [194]–[197]. All these functionalities can be embedded within a $\Sigma\Delta$M feedback loop as conceptually depicted in Fig. 28. The resulting *$\Sigma\Delta$M-based transceivers* may become more efficient than conventional ones in terms of analog circuit complexity, shared building blocks, and reduced power consumption. Moreover, $\Sigma\Delta$M-based SDRs can benefit from their robustness to circuit errors in order to increase their adaptability to many different operation modes and signal conditions, as well as the incorporation of the so-called *spectrum-sensing* capabilities [160].

VI. Conclusion

$\Sigma\Delta$ modulation constitutes one of the best techniques for the implementation of analog-to-digital interfaces in system-on-chip solutions implemented in nanometer CMOS technologies. The state-of-the-art performance summarized in this paper illustrates how $\Sigma\Delta$Ms are targeting more and more applications, covering an increasingly wide region in the resolution-versus-bandwidth plane. This trend is set to continue thanks to advances at both architectural and circuit level. The different $\Sigma\Delta$ techniques overviewed in this paper show that there are many alternatives for digitizing signals with diverse specifications. Technology downscaling imposes new challenges and opportunities for research in this *old* topic of circuits and systems that has given (and continues to give) a huge number of successful industrial results since the first idea was patented around 50 years ago.

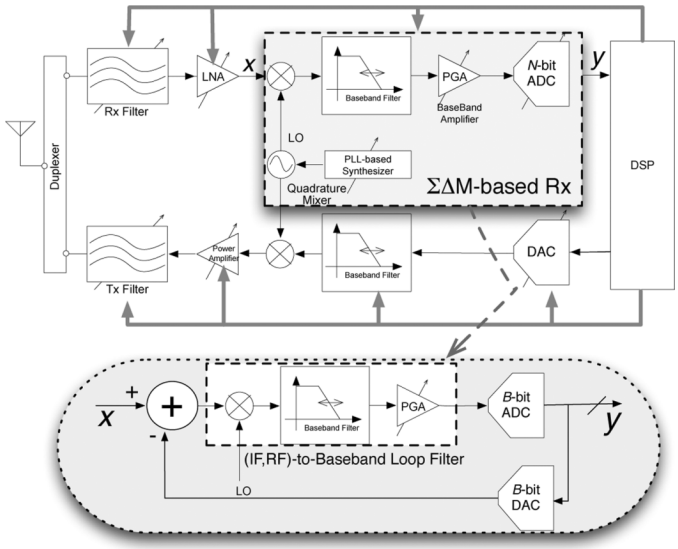

Fig. 28. Conceptual scheme of a $\Sigma\Delta$M-based SDR.

VII. References (Organized by Topics)

The list of references included at the end of this paper can be classified into the following groups, according to the topics they cover:

- *General references*: [3]–[17], [25], [26], [28].
- *Fundamentals and background theory*: [1], [2], [18]–[23], [35]–[37], [70], [72].
- *Taxonomy of $\Sigma\Delta$Ms*: Basic (DT) $\Sigma\Delta$Ms [35], [38], [39]; multibit quantization and linearization techniques [44]–[52], [54]–[58]; BP-$\Sigma\Delta$Ms [59]–[63], [71], [73], [74]; CT-$\Sigma\Delta$Ms [53], [66], [67], [69], [136].
- *Circuit implementation and nonideal performance*: [27], [78]–[80], [82]–[97].
- *Design methodologies*: [24], [98]–[109].
- *State-of-the-art performance*: FOM definitions and surveys [113]–[116], [175]; single-loop LP DT-$\Sigma\Delta$Ms [117]–[132]; single-loop LP CT-$\Sigma\Delta$Ms [133]–[155]; cascade DT-$\Sigma\Delta$Ms [157]–[162]; cascade CT-$\Sigma\Delta$Ms [40]–[43]; BP-$\Sigma\Delta$Ms [75], [163]–[167]; reconfigurable DT-$\Sigma\Delta$Ms [168]–[172]; reconfigurable CT-$\Sigma\Delta$Ms [173], [174].
- *Advanced $\Sigma\Delta$M architectures and current trends*: USTF and SMASH $\Sigma\Delta$Ms [176]–[181]; hybrid CT/DT $\Sigma\Delta$Ms [29]–[34]; time-encoding quantizers [182]–[188]; digital-based implementions [117], [118], [156], [189]; $\Sigma\Delta$Ms for SDR applications [76], [77], [164], [192]–[197].

Acknowledgment

The author would like to express his gratitude to the members of the IMSE-CNM $\Sigma\Delta$ design group, specially to Prof. A. Rodríguez-Vázquez, Prof. B. Pérez-Verdú, Dr. F. Medeiro, Dr. R. del Río, Mr. A. Morgado, and Mr. J.G. García-Sánchez. Some

pieces of material used for the preparation of this paper have been adapted from different manuscripts coauthored by them and the author himself. The author is also grateful to the Associate Editor and the anonymous reviewers for their constructive and valuable comments and suggestions to improve the quality of this paper.

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