Dear EE2020 Students,

Next week (6 & 7 Nov 2017) is the assessment week for the EE2020 FPGA Design Project. You will be assessed in your teams with an allocated time of **30 minutes**.

Excluding the earliest time slots, please arrive 30 minutes before the scheduled time.

Read the following instructions carefully :
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Pre-Evaluation:

- You are required to submit ONE Vivado project archive (.zip file) for your team. The team marks are not awarded if all the features from the team are not combined into one bitstream.
- Ensure that your bitstream has been successfully generated before archiving your Vivado workspace.
  You will not be allowed to change your Verilog codes or generate your bitstream during the assessment.
- To archive your Vivado Project, go to File >> Archive Project. Upload your Vivado Project Archive to IVLE. *Penalties apply for late submissions.*

Submission Deadlines:

- Thursday Lab Group : Project Archive Deadline **5 Nov Sunday 1700**
  Project Report Deadline **13 Nov Monday 2359**
- Friday Lab Group : Project Archive Deadline **6 Nov Monday 1700**
  Project Report Deadline **14 Nov Tuesday 2359**
- Name your Project Archive in this format :

  *Official lab day_Name of any one team member **as indicated on the matriculation card**_Matriculation number 1_Matriculation number 2_Archive*
  Eg. Monday_Harry Nyquist_A0123456Z_A0010101Z_Archive.zip
- Report Guidelines : Refer to
  IVLE >> Workbin >> Digital Fundamentals (Project Submission & Demo) >> EE2020 Project Report Guidelines.pdf

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Evaluation:

- Check that your names are recorded correctly on the grading sheet.
- You are **not allowed** to use your own notebook to upload your bitstream to the FPGA.
- Your bitstream will be uploaded to a BASYS3 before the assessment starts.
- Demonstrate your program as per the assessing G.A.'s instructions
- Ensure that you present all the features you have implemented. Marks are not awarded for features that are not demonstrated.
- The assessing G.A. may ask you team or individual questions anytime during your demonstration regarding your implementation, your Verilog code or your understanding of the project.

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ACADEMIC INTEGRITY:

Reminder from the NUS Code of Student Conduct:
http://www.nus.edu.sg/registrar/adminpolicy/acceptance.html

"Any student found to have **committed** or **aided and abetted** the offence of plagiarism may be subject to disciplinary action"

Both the **source** and **recipient** of the project and/or report are equally responsible in cases of academic dishonesty.

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Post-Evalution: Return BASYS3 FPGA and all PMOD Components!

- Return kit immediately after assessment or within 1 week.
- Ensure that all packaging materials, cables and devices are present.
- Kindly inform the lab officer of any damaged item to avoid re-use of faulty item.

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We hope that you have enjoyed this challenging journey and hope that the FPGA design project has given you the opportunity to experience of process of ideation to creation. We look forward to seeing your projects!

EE2020/EE2026
Teaching and Support Team