Table 12. Pin assignment and description

Pin number										Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100					
-	-	-	-	-	64	64	A2	2	2	B2	PC10	I/O	FT	-	USART3_TX, USART4_TX, TIM1_CH3, SPI3_SCK	-
-	-	-	-	-	1	1	A1	3	3	B1	PC11	I/O	FT	-	USART3_RX, USART4_RX, TIM1_CH4, SPI3_MISO	-
-	-	-	-	-	-	-	-	-	4	C2	PE4	I/O	FT	-	TIM3_CH2	-
-	-	-	-	-	-	-	-	-	5	D3	PE5	I/O	FT	-	TIM3_CH3	-
-	-	-	-	-	-	-	-	-	6	C1	PE6	I/O	FT	-	TIM3_CH4	TAMP_IN3, WKUP3
-	-	-	-	-	2	2	B2	4	7	D2	PC12	I/O	FT	-	LPTIM1_IN1, UCPD1_FRSTX, TIM14_CH1, USART5_TX, SPI3_MOSI	-
-	-	1	1	B11	3	3	C2	5	8	E3	PC13	I/O	FT	(1)(2)	TIM1_BKIN	TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2
-	-	2	2	B13	4	4	C1	6	9	D1	PC14-OSC32_IN	I/O	FT	(1)(2)	TIM1_BKIN2	OSC32_IN
2	2	-	-	-	-	-	-	-	-	-	PC14-OSC32_IN	I/O	FT	(1)(2)	TIM1_BKIN2	OSC32_IN, OSC_IN
3	3	3	3	C12	5	5	B1	7	10	E1	PC15-OSC32_OUT	I/O	FT	(1)(2)	OSC32_EN, OSC_EN, TIM15_BKIN	OSC32_OUT
-	-	4	4	C10	6	6	D3	8	11	E2	VBAT	S	-	-	-	-
-	-	5	5	D11	7	7	D2	9	12	F2	VREF+	S	-	-	-	VREFBUF_OUT
4	4	6	6	D13	8	8	D1	10	13	F1	VDD/VDDA	S	-	-	-	-
5	5	7	7	E12	9	9	E1	11	14	G1	VSS/VSSA	S	-	-	-	-
-	-	8	8	F13	10	10	F1	12	15	H1	PF0-OSC_IN	I/O	FT	-	CRS1_SYNC, EVENTOUT, TIM14_CH1	OSC_IN

Table 12. Pin assignment and description (continued)

Pin number											Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100						
-	6	9	9	G12	11	11	G1	13	16	J1	PF1-OSC_OUT	I/O	FT	-	OSC_EN, EVENTOUT, TIM15_CH1N	OSC_OUT
6	6	10	10	F11	12	12	E2	14	17	G2	PF2-NRST	I/O	RST, FT	(3)	MCO, LPUART2_TX, LPUART2_RTS_DE	NRST
-	-	-	-	-	-	-	-	-	18	H3	PF3	I/O	FT	-	LPUART2_RX, USART6_RTS_DE_CK	-
-	-	-	-	-	-	-	-	-	19	H2	PF4	I/O	FT	-	LPUART1_TX	-
-	-	-	-	-	-	-	-	-	20	J2	PF5	I/O	FT	-	LPUART1_RX	-
-	-	-	-	-	13	13	E3	15	21	K1	PC0	I/O	FT_a	-	LPTIM1_IN1, LPUART1_RX, LPTIM2_IN1, LPUART2_TX, USART6_TX, I2C3_SCL, COMP3_OUT	COMP3_INM7
-	-	-	-	-	14	14	F2	16	22	J3	PC1	I/O	FT_a	-	LPTIM1_OUT, LPUART1_TX, TIM15_CH1, LPUART2_RX, USART6_RX, I2C3_SDA	COMP3_INP1
-	-	-	-	-	15	15	G2	17	23	K2	PC2	I/O	FT	-	LPTIM1_IN2, SPI2_MISO/I2S2_MCK, TIM15_CH2, FDCAN2_RX, COMP3_OUT	-
-	-	-	-	-	16	16	H1	18	24	L1	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI/I2S2_SD, LPTIM2_ETR, FDCAN2_TX	-
7	7	11	11	H13	17	17	H2	19	25	K3	PA0	I/O	FT_a	-	SPI2_SCK/I2S2_CK, USART2_CTS, TIM2_CH1_ETR, USART4_TX, LPTIM1_OUT, UCPD2_FRSTX, COMP1_OUT	COMP1_INM8, ADC_IN0, TAMP_IN2, WKUP1
8	8	12	12	E10	18	18	H3	20	26	L2	PA1	I/O	FT_ea	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM2_CH2, USART4_RX, TIM15_CH1N, I2C1_SMBA, EVENTOUT	COMP1_INP2, ADC_IN1
9	9	13	13	E8	19	19	G3	21	27	M1	PA2	I/O	FT_a	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM2_CH3, UCPD1_FRSTX, TIM15_CH1, LPUART1_TX, COMP2_OUT	COMP2_INM8, ADC_IN2, WKUP4, LSCO

Table 12. Pin assignment and description (continued)

Pin number										Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100					
10	10	14	14	H11	20	20	F3	22	28	K4	PA3	I/O	FT_ea	-	SPI2_MISO/I2S2_MCK, USART2_RX, TIM2_CH4, UCPD2_FRSTX, TIM15_CH2, LPUART1_RX, EVENTOUT	COMP2_INP2, ADC_IN3
-	-	15	15	G10	21	-	H4	23	29	L3	PA4	I/O	TT_a	-	SPI1_NSS/I2S1_WS, SPI2_MOSI/I2S2_SD, USART6_TX, TIM14_CH1, LPTIM2_OUT, UCPD2_FRSTX, EVENTOUT, SPI3_NSS	ADC_IN4, DAC1_OUT1, RTC_OUT2
11	11	-	-	-	-	-	-	-	-	-	PA4	I/O	TT_a	-	SPI1_NSS/I2S1_WS, SPI2_MOSI/I2S2_SD, USART6_TX, TIM14_CH1, LPTIM2_OUT, UCPD2_FRSTX, EVENTOUT, SPI3_NSS	ADC_IN4, DAC1_OUT1, TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2
12	12	16	16	F9	22	22	G4	24	30	M2	PA5	I/O	TT_ea	-	SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, USART6_RX, USART3_TX, LPTIM2_ETR, UCPD1_FRSTX, EVENTOUT	ADC_IN5, DAC1_OUT2
13	13	17	17	F7	23	23	F4	25	31	M3	PA6	I/O	FT_ea	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, USART6_CTS, USART3_CTS, TIM16_CH1, LPUART1_CTS, COMP1_OUT, I2C2_SDA, I2C3_SDA	ADC_IN6
14	14	18	18	H9	24	24	E4	26	32	K5	PA7	I/O	FT_a	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, USART6_RTS_DE_CK, TIM14_CH1, TIM17_CH1, UCPD1_FRSTX, COMP2_OUT, I2C2_SCL, I2C3_SCL	ADC_IN7
-	-	-	-	G8	25	25	H5	27	33	L4	PC4	I/O	FT_a	-	USART3_TX, USART1_TX, TIM2_CH1_ETR, FDCAN1_RX	COMP1_INM7, ADC_IN17
-	-	-	-	G6	26	26	H6	28	34	M4	PC5	I/O	FT_a	-	USART3_RX, USART1_RX, TIM2_CH2, FDCAN1_TX	COMP1_INP0, ADC_IN18, WKUP5

Table 12. Pin assignment and description (continued)

Pin number										Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100					
15	15	19	19	H7	27	27	F5	29	35	L5	PB0	I/O	FT_ea	-	SPI1_NSS/I2S1_WS, TIM3_CH3, TIM1_CH2N, FDCAN2_RX, USART3_RX, LPTIM1_OUT, UCPD1_FRSTX, COMP1_OUT, USART5_TX, LPUART2_CTS	COMP3_INP0, ADC_IN8
16	16	20	20	H5	28	28	G5	30	36	M5	PB1	I/O	FT_ea	-	TIM14_CH1, TIM3_CH4, TIM1_CH3N, FDCAN2_TX, USART3_RTS_DE_CK, LPTIM2_IN1, LPUART1_RTS_DE, COMP3_OUT, USART5_RX, LPUART2_RTS_DE	COMP1_INM6, ADC_IN9
17	-	21	21	G4	29	29	H7	31	37	L6	PB2	I/O	FT_ea	-	SPI2_MISO/I2S2_MCK, MCO2, USART3_TX, LPTIM1_OUT, EVENTOUT	COMP1_INP1, COMP3_INM6, ADC_IN10
-	-	-	-	-	-	-	-	-	38	M6	PF6	I/O	FT	-	LPUART1_RTS_DE	-
-	-	-	-	-	-	-	-	-	39	L7	PF7	I/O	FT	-	LPUART1_CTS, USART5_CTS	-
-	-	-	-	-	-	-	-	32	40	M7	PE7	I/O	FT_a	-	TIM1_ETR, USART5_RTS_DE_CK	COMP3_INP2
-	-	-	-	-	-	-	-	33	41	M8	PE8	I/O	FT_a	-	USART4_TX, TIM1_CH1N	COMP3_INM8
-	-	-	-	-	-	-	-	34	42	K8	PE9	I/O	FT	-	USART4_RX, TIM1_CH1	-
-	-	-	-	-	-	-	-	35	43	L8	PE10	I/O	FT	-	TIM1_CH2N, USART5_TX	-
-	-	-	-	-	-	-	-	-	44	M9	PE11	I/O	FT	-	TIM1_CH2, USART5_RX	-
-	-	-	-	-	-	-	-	-	45	L9	PE12	I/O	FT	-	SPI1_NSS/I2S1_WS, TIM1_CH3N	-
-	-	-	-	-	-	-	-	-	46	M10	PE13	I/O	FT	-	SPI1_SCK/I2S1_CK, TIM1_CH3	-
-	-	-	-	-	-	-	-	-	47	K9	PE14	I/O	FT	-	SPI1_MISO/I2S1_MCK, TIM1_CH4, TIM1_BKIN2	-
-	-	-	-	-	-	-	-	-	48	L10	PE15	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM1_BKIN	-

Table 12. Pin assignment and description (continued)

Pin number										Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100					
-	-	22	22	H3	30	30	G6	36	49	M11	PB10	I/O	FT_fa	-	CEC, LPUART1_RX, TIM2_CH3, USART3_TX, SPI2_SCK/I2S2_CK, I2C2_SCL, COMP1_OUT	ADC_IN11
-	-	23	23	F5	31	31	H8	37	50	L11	PB11	I/O	FT_fa	-	SPI2_MOSI/I2S2_SD, LPUART1_TX, TIM2_CH4, USART3_RX, I2C2_SDA, COMP2_OUT	ADC_IN15
-	-	24	24	E6	32	32	G7	38	51	K10	PB12	I/O	FT_fa	-	SPI2_NSS/I2S2_WS, LPUART1_RTS_DE, TIM1_BKIN, FDCAN2_RX, TIM15_BKIN, UCPD2_FRSTX, EVENTOUT, I2C2_SMBA	ADC_IN16
-	-	25	25	H1	33	33	G8	39	52	M12	PB13	I/O	FT_fs	-	SPI2_SCK/I2S2_CK, LPUART1_CTS, TIM1_CH1N, FDCAN2_TX, USART3_CTS, TIM15_CH1N, I2C2_SCL, EVENTOUT	-
-	-	26	26	G2	34	34	F6	40	53	K11	PB14	I/O	FT_fs	-	SPI2_MISO/I2S2_MCK, UCPD1_FRSTX, TIM1_CH2N, USART3_RTS_DE_CK, TIM15_CH1, I2C2_SDA, EVENTOUT, USART6_RTS_DE_CK	-
-	17	27	27	F3	35	35	F7	41	54	J10	PB15	I/O	FT_fcs	(4)	SPI2_MOSI/I2S2_SD, TIM1_CH3N, TIM15_CH1N, TIM15_CH2, EVENTOUT, USART6_CTS	UCPD1_CC2, RTC_REFIN
18	18	28	28	F1	36	36	F8	42	55	L12	PA8	I/O	FT_fcs	(4)	MCO, SPI2_NSS/I2S2_WS, TIM1_CH1, CRS1_SYNC, LPTIM2_OUT, EVENTOUT, I2C2_SMBA	UCPD1_CC1
19	19	29	29	E4	37	37	E6	43	56	H10	PA9	I/O	FT_fds	(4)	MCO, USART1_TX, TIM1_CH2, SPI2_MISO/I2S2_MCK, TIM15_BKIN, I2C1_SCL, EVENTOUT, I2C2_SCL	UCPD1_DBCC1
20	-	30	-	D5	38	38	E7	44	57	J11	PC6	I/O	FT_s	-	UCPD1_FRSTX, TIM3_CH1, TIM2_CH3, LPUART2_TX	-
-	-	31	-	D3	39	39	E5	45	58	K12	PC7	I/O	FT_s	-	UCPD2_FRSTX, TIM3_CH2, TIM2_CH4, LPUART2_RX	-

Table 12. Pin assignment and description (continued)

Pin number												Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100							
-	-	-	-	-	40	-	-	46	59	J12	PD8	I/O	FT_s	-	USART3_TX, SPI1_SCK/I2S1_CK, LPTIM1_OUT	-
-	-	-	-	-	41	-	-	47	60	H11	PD9	I/O	FT_s	-	USART3_RX, SPI1_NSS/I2S1_WS, TIM1_BKIN2	-
-	-	-	-	-	-	-	-	48	61	H12	PD10	I/O	FT_s	-	MCO	-
-	-	-	-	-	-	-	-	49	62	G11	PD11	I/O	FT_s	-	USART3_CTS, LPTIM2_ETR	-
-	-	-	-	E2	-	40	E8	50	63	G12	VSS	S	-	-	-	-
-	20	-	31	D1	-	41	D8	51	64	F12	VDDIO2	S	-	-	-	-
-	-	-	-	-	-	-	-	52	65	F11	PD12	I/O	FT_s	-	USART3_RTS_DE_CK, LPTIM2_IN1, TIM4_CH1, FDCAN1_RX	-
-	-	-	-	-	-	-	-	53	66	E12	PD13	I/O	FT_s	-	LPTIM2_OUT, TIM4_CH2, FDCAN1_TX	-
-	-	-	-	-	-	-	-	54	67	E11	PD14	I/O	FT_s	-	LPUART2_CTS, TIM4_CH3, FDCAN2_RX	-
-	-	-	-	-	-	-	-	55	68	D11	PD15	I/O	FT_s	-	CRS1_SYNC, LPUART2_RTS_DE, TIM4_CH4, FDCAN2_TX	-
21	21	32	32	C4	42	42	D6	56	69	E10	PA10	I/O	FT_fds	(4)	SPI2_MOSI/I2S2_SD, USART1_RX, TIM1_CH3, MCO2, TIM17_BKIN, I2C1_SDA, EVENTOUT, I2C2_SDA	UCPD1_DBCC2
22	22	33	33	C2	43	43	C8	57	70	D12	PA11 [PA9]	I/O	FT_fus	(5)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, FDCAN1_RX, TIM1_BKIN2, I2C2_SCL, COMP1_OUT	USB_DM
23	23	34	34	B1	44	44	B8	58	71	C12	PA12 [PA10]	I/O	FT_fus	(5)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, FDCAN1_TX, I2S_CKIN, I2C2_SDA, COMP2_OUT	USB_DP
-	-	-	-	-	-	-	-	-	72	D10	PF8	I/O	FT_s	-	-	-

Table 12. Pin assignment and description (continued)

Pin number									Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100						
24	25	35	36	B3	45	46	D7	59	73	C11	PA13	I/O	FT_es	(6)	SWDIO, IR_OUT, USB_NOE, EVENTOUT, LPUART2_RX	-
25	25	36	36	B5	46	46	C7	60	74	B12	PA14-BOOT0	I/O	FT_s	(6)	SWCLK, USART2_TX, EVENTOUT, LPUART2_TX	BOOT0
26	-	37	37	A2	47	47	C6	61	75	B11	PA15	I/O	FT_s	-	SPI1_NSS/I2S1_WS, USART2_RX, TIM2_CH1_ETR, MCO2, USART4_RTS_DE_CK, USART3_RTS_DE_CK, USB_NOE, EVENTOUT, I2C2_SMBA, SPI3_NSS	-
-	-	-	-	-	48	48	A8	62	76	C10	PC8	I/O	FT_s	-	UCPD2_FRSTX, TIM3_CH3, TIM1_CH1, LPUART2_CTS	-
-	-	-	-	-	49	49	B7	63	77	A12	PC9	I/O	FT_s	-	I2S_CKIN, TIM3_CH4, TIM1_CH2, LPUART2_RTS_DE, USB_NOE	-
-	26	38	38	A4	50	50	A7	64	78	B10	PD0	I/O	FT_cs	(4)	EVENTOUT, SPI2_NSS/I2S2_WS, TIM16_CH1, FDCAN1_RX	UCPD2_CC1
-	27	39	39	C6	51	51	B6	65	79	C9	PD1	I/O	FT_ds	(4)	EVENTOUT, SPI2_SCK/I2S2_CK, TIM17_CH1, FDCAN1_TX	UCPD2_DBCC1
-	28	40	40	B7	52	52	A6	66	80	A11	PD2	I/O	FT_cs	(4)	USART3_RTS_DE_CK, TIM3_ETR, TIM1_CH1N, USART5_RX	UCPD2_CC2
-	29	41	41	A6	53	53	D5	67	81	C8	PD3	I/O	FT_ds	(4)	USART2_CTS, SPI2_MISO/I2S2_MCK, TIM1_CH2N, USART5_TX	UCPD2_DBCC2
-	-	-	-	-	54	54	C5	68	82	B9	PD4	I/O	FT_s	-	USART2_RTS_DE_CK, SPI2_MOSI/I2S2_SD, TIM1_CH3N, USART5_RTS_DE_CK	-
-	-	-	-	-	55	55	B5	69	83	A10	PD5	I/O	FT	-	USART2_TX, SPI1_MISO/I2S1_MCK, TIM1_BKIN, USART5_CTS	-
-	-	-	-	-	56	56	A5	70	84	A9	PD6	I/O	FT	-	USART2_RX, SPI1_MOSI/I2S1_SD, LPTIM2_OUT	-

Table 12. Pin assignment and description (continued)

Pin number											Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100						
-	-	-	-	-	-	-	-	71	85	B8	PD7	I/O	FT	-	MCO2	-
-	-	-	-	-	-	-	-	-	86	A8	PF9	I/O	FT	-	USART6_TX	-
-	-	-	-	-	-	-	-	-	87	B7	PF10	I/O	FT	-	USART6_RX	-
-	-	-	-	-	-	-	-	-	88	A7	PF11	I/O	FT	-	USART6_RTS_DE_CK	-
-	-	-	-	-	-	-	-	-	89	B6	PF12	I/O	FT	-	TIM15_CH1, USART6_CTS	-
-	-	-	-	-	-	-	-	-	90	A6	PF13	I/O	FT	-	TIM15_CH2	-
27	-	42	42	A8	57	57	B4	72	91	A5	PB3	I/O	FT_a	-	SPI1_SCK/I2S1_CK, TIM1_CH2, TIM2_CH2, USART5_TX, USART1_RTS_DE_CK, I2C3_SCL, EVENTOUT, I2C2_SCL, SPI3_SCK	COMP2_INM6
28	-	43	43	B9	58	58	C4	73	92	B5	PB4	I/O	FT_a	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, USART5_RX, USART1_CTS, TIM17_BKIN, I2C3_SDA, EVENTOUT, I2C2_SDA, SPI3_MISO	COMP2_INP0
29	-	44	44	A10	59	59	D4	74	93	C5	PB5	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM16_BKIN, FDCAN2_RX, LPTIM1_IN1, I2C1_SMBA, COMP2_OUT, USART5_RTS_DE_CK, SPI3_MOSI	WKUP6
-	-	-	-	-	-	-	-	75	94	A4	PE0	I/O	FT	-	TIM16_CH1, EVENTOUT, TIM4_ETR	-
-	-	-	-	-	-	-	-	76	95	B4	PE1	I/O	FT	-	TIM17_CH1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	96	A3	PE2	I/O	FT	-	TIM3_ETR	-
-	-	-	-	-	-	-	-	77	97	A2	PE3	I/O	FT	-	TIM3_CH1	-

Table 12. Pin assignment and description (continued)

Pin number										Pin name	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32 / UFQFPN32 - GP	LQFP32 / UFQFPN32 - N	LQFP48 / UFQFPN48 - GP	LQFP48 / UFQFPN48 - N	WLCSP52	LQFP64 - GP	LQFP64 - N	UFBGA64 - N	LQFP80	LQFP100	UFBGA100					
30	30	45	45	C8	60	60	A4	78	98	C4	PB6	I/O	FT_fa	-	USART1_TX, TIM1_CH3, TIM16_CH1N, FDCAN2_TX, SPI2_MISO/I2S2_MCK, LPTIM1_ETR, I2C1_SCL, EVENTOUT, USART5_CTS, TIM4_CH1, LPUART2_TX	COMP2_INP1
31	31	46	46	D7	61	61	A3	79	99	B3	PB7	I/O	FT_fa	-	USART1_RX, SPI2_MOSI/I2S2_SD, TIM17_CH1N, USART4_CTS, LPTIM1_IN2, I2C1_SDA, EVENTOUT, TIM4_CH2, LPUART2_RX	COMP2_INM7, PVD_IN
32	32	47	47	A12	62	62	B3	80	100	A1	PB8	I/O	FT_f	-	CEC, SPI2_SCK/I2S2_CK, TIM16_CH1, FDCAN1_RX, USART3_TX, TIM15_BKIN, I2C1_SCL, EVENTOUT, USART6_TX, TIM4_CH3	-
1	1	48	48	D9	63	63	C3	1	1	C3	PB9	I/O	FT_f	-	IR_OUT, UCPD2_FRSTX, TIM17_CH1, FDCAN1_TX, USART3_RX, SPI2_NSS/I2S2_WS, I2C1_SDA, EVENTOUT, USART6_RX, TIM4_CH4	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only provides a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs can be used as current sinks but not as current sources.
2. After an RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers. The RTC registers are not reset upon system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the RM0444 reference manual.
3. RST I/O structure when the PF2-NRST pin is configured as reset (input or input/output mode), FT I/O structure when the PF2-NRST pin is configured as GPIO.
4. Upon reset, a pull-down resistor might be present on PA8, PB15, PD0, or PD2 depending on voltage level on PA9, PA10, PD1, and PD3, respectively. In order to disable this resistor, strobe the UCPDx_STROBE bits in SYSCFG_CFGR1 register during start-up sequence.
5. Pins PA9/PA10 can be remapped in place of pins PA11/PA12 (default mapping), using SYSCFG_CFGR1 register.
6. Upon reset, these pins are configured as SW debug alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.

Table 13. Port A alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK/ I2S2_CK	USART2_CTS	TIM2_CH1_ETR	-	USART4_TX	LPTIM1_OUT	UCPD2_FRSTX	COMP1_OUT
PA1	SPI1_SCK/ I2S1_CK	USART2_RTS _DE_CK	TIM2_CH2	-	USART4_RX	TIM15_CH1N	I2C1_SMBA	EVENTOUT
PA2	SPI1_MOSI/ I2S1_SD	USART2_TX	TIM2_CH3	-	UCPD1_FRSTX	TIM15_CH1	LPUART1_TX	COMP2_OUT
PA3	SPI2_MISO/ I2S2_MCK	USART2_RX	TIM2_CH4	-	UCPD2_FRSTX	TIM15_CH2	LPUART1_RX	EVENTOUT
PA4	SPI1_NSS/ I2S1_WS	SPI2_MOSI/ I2S2_SD	-	USART6_TX	TIM14_CH1	LPTIM2_OUT	UCPD2_FRSTX	EVENTOUT
PA5	SPI1_SCK/ I2S1_CK	CEC	TIM2_CH1_ETR	USART6_RX	USART3_TX	LPTIM2_ETR	UCPD1_FRSTX	EVENTOUT
PA6	SPI1_MISO/ I2S1_MCK	TIM3_CH1	TIM1_BKIN	USART6_CTS	USART3_CTS	TIM16_CH1	LPUART1_CTS	COMP1_OUT
PA7	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N	USART6_RTS _DE_CK	TIM14_CH1	TIM17_CH1	UCPD1_FRSTX	COMP2_OUT
PA8	MCO	SPI2_NSS/ I2S2_WS	TIM1_CH1	-	CRS1_SYNC	LPTIM2_OUT	-	EVENTOUT
PA9	MCO	USART1_TX	TIM1_CH2	-	SPI2_MISO/ I2S2_MCK	TIM15_BKIN	I2C1_SCL	EVENTOUT
PA10	SPI2_MOSI/ I2S2_SD	USART1_RX	TIM1_CH3	MCO2	-	TIM17_BKIN	I2C1_SDA	EVENTOUT
PA11	SPI1_MISO/ I2S1_MCK	USART1_CTS	TIM1_CH4	FDCAN1_RX	-	TIM1_BKIN2	I2C2_SCL	COMP1_OUT
PA12	SPI1_MOSI/ I2S1_SD	USART1_RTS _DE_CK	TIM1_ETR	FDCAN1_TX	-	I2S_CKIN	I2C2_SDA	COMP2_OUT
PA13	SWDIO	IR_OUT	USB_NOE	-	-	-	-	EVENTOUT
PA14	SWCLK	USART2_TX	-	-	-	-	-	EVENTOUT
PA15	SPI1_NSS/ I2S1_WS	USART2_RX	TIM2_CH1_ETR	MCO2	USART4_RTS _DE_CK	USART3_RTS _DE_CK	USB_NOE	EVENTOUT

Table 14. Port A alternate function mapping (AF8 to AF15)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	-	-	-	-	-	-	-
PA1	-	-	-	-	-	-	-	-
PA2	-	-	-	-	-	-	-	-
PA3	-	-	-	-	-	-	-	-
PA4	-	SPI3_NSS	-	-	-	-	-	-
PA5	-	-	-	-	-	-	-	-
PA6	I2C2_SDA	I2C3_SDA	-	-	-	-	-	-
PA7	I2C2_SCL	I2C3_SCL	-	-	-	-	-	-
PA8	I2C2_SMBA	-	-	-	-	-	-	-
PA9	I2C2_SCL	-	-	-	-	-	-	-
PA10	I2C2_SDA	-	-	-	-	-	-	-
PA11	-	-	-	-	-	-	-	-
PA12	-	-	-	-	-	-	-	-
PA13	-	-	LPUART2_RX	-	-	-	-	-
PA14	-	-	LPUART2_TX	-	-	-	-	-
PA15	I2C2_SMBA	SPI3_NSS	-	-	-	-	-	-

Table 15. Port B alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS/ I2S1_WS	TIM3_CH3	TIM1_CH2N	FDCAN2_RX	USART3_RX	LPTIM1_OUT	UCPD1_FRSTX	COMP1_OUT
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	FDCAN2_TX	USART3_RTS _DE_CK	LPTIM2_IN1	LPUART1_RTS _DE	COMP3_OUT
PB2	-	SPI2_MISO/ I2S2_MCK	-	MCO2	USART3_TX	LPTIM1_OUT	-	EVENTOUT
PB3	SPI1_SCK/ I2S1_CK	TIM1_CH2	TIM2_CH2	USART5_TX	USART1_RTS _DE_CK	-	I2C3_SCL	EVENTOUT
PB4	SPI1_MISO/ I2S1_MCK	TIM3_CH1	-	USART5_RX	USART1_CTS	TIM17_BKIN	I2C3_SDA	EVENTOUT
PB5	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM16_BKIN	FDCAN2_RX	-	LPTIM1_IN1	I2C1_SMBA	COMP2_OUT
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	FDCAN2_TX	SPI2_MISO/ I2S2_MCK	LPTIM1_ETR	I2C1_SCL	EVENTOUT
PB7	USART1_RX	SPI2_MOSI/ I2S2_SD	TIM17_CH1N	-	USART4_CTS	LPTIM1_IN2	I2C1_SDA	EVENTOUT
PB8	CEC	SPI2_SCK/ I2S2_CK	TIM16_CH1	FDCAN1_RX	USART3_TX	TIM15_BKIN	I2C1_SCL	EVENTOUT
PB9	IR_OUT	UCPD2_FRSTX	TIM17_CH1	FDCAN1_TX	USART3_RX	SPI2_NSS/ I2S2_WS	I2C1_SDA	EVENTOUT
PB10	CEC	LPUART1_RX	TIM2_CH3	-	USART3_TX	SPI2_SCK/ I2S2_CK	I2C2_SCL	COMP1_OUT
PB11	SPI2_MOSI/ I2S2_SD	LPUART1_TX	TIM2_CH4	-	USART3_RX	-	I2C2_SDA	COMP2_OUT
PB12	SPI2_NSS/ I2S2_WS	LPUART1_RTS _DE	TIM1_BKIN	FDCAN2_RX	-	TIM15_BKIN	UCPD2_FRSTX	EVENTOUT
PB13	SPI2_SCK/ I2S2_CK	LPUART1_CTS	TIM1_CH1N	FDCAN2_TX	USART3_CTS	TIM15_CH1N	I2C2_SCL	EVENTOUT

Table 15. Port B alternate function mapping (AF0 to AF7) (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB14	SPI2_MISO/ I2S2_MCK	UCPD1_FRSTX	TIM1_CH2N	-	USART3_RTS _DE_CK	TIM15_CH1	I2C2_SDA	EVENTOUT
PB15	SPI2_MOSI/ I2S2_SD	-	TIM1_CH3N	-	TIM15_CH1N	TIM15_CH2	-	EVENTOUT

Table 16. Port B alternate function mapping (AF8 to AF15)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	USART5_TX	-	LPUART2_CTS	-	-	-	-	-
PB1	USART5_RX	-	LPUART2_RTS _DE	-	-	-	-	-
PB2	-	-	-	-	-	-	-	-
PB3	I2C2_SCL	SPI3_SCK	-	-	-	-	-	-
PB4	I2C2_SDA	SPI3_MISO	-	-	-	-	-	-
PB5	USART5_RTS _DE_CK	SPI3_MOSI	-	-	-	-	-	-
PB6	USART5_CTS	TIM4_CH1	LPUART2_TX	-	-	-	-	-
PB7	-	TIM4_CH2	LPUART2_RX	-	-	-	-	-
PB8	USART6_TX	TIM4_CH3	-	-	-	-	-	-
PB9	USART6_RX	TIM4_CH4	-	-	-	-	-	-
PB10	-	-	-	-	-	-	-	-
PB11	-	-	-	-	-	-	-	-
PB12	I2C2_SMBA	-	-	-	-	-	-	-
PB13	-	-	-	-	-	-	-	-
PB14	USART6_RTS _DE_CK	-	-	-	-	-	-	-
PB15	USART6_CTS	-	-	-	-	-	-	-

Table 17. Port C alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	LPTIM1_IN1	LPUART1_RX	LPTIM2_IN1	LPUART2_TX	USART6_TX	-	I2C3_SCL	COMP3_OUT
PC1	LPTIM1_OUT	LPUART1_TX	TIM15_CH1	LPUART2_RX	USART6_RX	-	I2C3_SDA	-
PC2	LPTIM1_IN2	SPI2_MISO/ I2S2_MCK	TIM15_CH2	FDCAN2_RX	-	-	-	COMP3_OUT
PC3	LPTIM1_ETR	SPI2_MOSI/ I2S2_SD	LPTIM2_ETR	FDCAN2_TX	-	-	-	-
PC4	USART3_TX	USART1_TX	TIM2_CH1_ETR	FDCAN1_RX	-	-	-	-
PC5	USART3_RX	USART1_RX	TIM2_CH2	FDCAN1_TX	-	-	-	-
PC6	UCPD1_FRSTX	TIM3_CH1	TIM2_CH3	LPUART2_TX	-	-	-	-
PC7	UCPD2_FRSTX	TIM3_CH2	TIM2_CH4	LPUART2_RX	-	-	-	-
PC8	UCPD2_FRSTX	TIM3_CH3	TIM1_CH1	LPUART2_CTS	-	-	-	-
PC9	I2S_CKIN	TIM3_CH4	TIM1_CH2	LPUART2_RTS_ DE	-	-	USB_NOE	-
PC10	USART3_TX	USART4_TX	TIM1_CH3	-	SPI3_SCK	-	-	-
PC11	USART3_RX	USART4_RX	TIM1_CH4	-	SPI3_MISO	-	-	-
PC12	LPTIM1_IN1	UCPD1_FRSTX	TIM14_CH1	USART5_TX	SPI3_MOSI	-	-	-
PC13	-	-	TIM1_BKIN	-	-	-	-	-
PC14	-	-	TIM1_BKIN2	-	-	-	-	-
PC15	OSC32_EN	OSC_EN	TIM15_BKIN	-	-	-	-	-

Table 18. Port D alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	SPI2_NSS/ I2S2_WS	TIM16_CH1	FDCAN1_RX	-	-	-	-
PD1	EVENTOUT	SPI2_SCK/ I2S2_CK	TIM17_CH1	FDCAN1_TX	-	-	-	-
PD2	USART3_RTS _DE_CK	TIM3_ETR	TIM1_CH1N	USART5_RX	-	-	-	-
PD3	USART2_CTS	SPI2_MISO/ I2S2_MCK	TIM1_CH2N	USART5_TX	-	-	-	-
PD4	USART2_RTS _DE_CK	SPI2_MOSI/ I2S2_SD	TIM1_CH3N	USART5_RTS _DE_CK	-	-	-	-
PD5	USART2_TX	SPI1_MISO/ I2S1_MCK	TIM1_BKIN	USART5_CTS	-	-	-	-
PD6	USART2_RX	SPI1_MOSI/ I2S1_SD	LPTIM2_OUT	-	-	-	-	-
PD7	-	-	-	MCO2	-	-	-	-
PD8	USART3_TX	SPI1_SCK/ I2S1_CK	LPTIM1_OUT	-	-	-	-	-
PD9	USART3_RX	SPI1_NSS/ I2S1_WS	TIM1_BKIN2	-	-	-	-	-
PD10	MCO	-	-	-	-	-	-	-
PD11	USART3_CTS	LPTIM2_ETR	-	-	-	-	-	-
PD12	USART3_RTS _DE_CK	LPTIM2_IN1	TIM4_CH1	FDCAN1_RX	-	-	-	-
PD13	-	LPTIM2_OUT	TIM4_CH2	FDCAN1_TX	-	-	-	-
PD14	-	LPUART2_CTS	TIM4_CH3	FDCAN2_RX	-	-	-	-
PD15	CRS1_SYNC	LPUART2_RTS _DE	TIM4_CH4	FDCAN2_TX	-	-	-	-

Table 19. Port E alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0	TIM16_CH1	EVENTOUT	TIM4_ETR	-	-	-	-	-
PE1	TIM17_CH1	EVENTOUT	-	-	-	-	-	-
PE2	-	TIM3_ETR	-	-	-	-	-	-
PE3	-	TIM3_CH1	-	-	-	-	-	-
PE4	-	TIM3_CH2	-	-	-	-	-	-
PE5	-	TIM3_CH3	-	-	-	-	-	-
PE6	-	TIM3_CH4	-	-	-	-	-	-
PE7	-	TIM1_ETR	-	USART5_RTS_DE_CK	-	-	-	-
PE8	USART4_TX	TIM1_CH1N	-	-	-	-	-	-
PE9	USART4_RX	TIM1_CH1	-	-	-	-	-	-
PE10	-	TIM1_CH2N	-	USART5_TX	-	-	-	-
PE11	-	TIM1_CH2	-	USART5_RX	-	-	-	-
PE12	SPI1_NSS/ I2S1_WS	TIM1_CH3N	-	-	-	-	-	-
PE13	SPI1_SCK/ I2S1_CK	TIM1_CH3	-	-	-	-	-	-
PE14	SPI1_MISO/I2S1_MCK	TIM1_CH4	TIM1_BK2	-	-	-	-	-
PE15	SPI1_MOSI/I2S1_SD	TIM1_BK	-	-	-	-	-	-

Table 20. Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	CRS1_SYNC	EVENTOUT	TIM14_CH1	-	-	-	-	-
PF1	OSC_EN	EVENTOUT	TIM15_CH1N	-	-	-	-	-
PF2	MCO	LPUART2_TX	-	LPUART2_RTS_DE	-	-	-	-
PF3	-	LPUART2_RX	-	USART6_RTS_DE_CK	-	-	-	-
PF4	-	LPUART1_TX	-	-	-	-	-	-
PF5	-	LPUART1_RX	-	-	-	-	-	-
PF6	-	LPUART1_RTS_DE	-	-	-	-	-	-
PF7	-	LPUART1_CTS	-	USART5_CTS	-	-	-	-
PF8	-	-	-	-	-	-	-	-
PF9	-	-	-	USART6_TX	-	-	-	-
PF10	-	-	-	USART6_RX	-	-	-	-
PF11	-	-	-	USART6_RTS_DE_CK	-	-	-	-
PF12	TIM15_CH1	-	-	USART6_CTS	-	-	-	-
PF13	TIM15_CH2	-	-	-	-	-	-	-