

Project in CE80665 Embedded Computer Systems Engineering
Department of Computer and Software Engineering
University of Rwanda/College of Science and Technology (UR/CST)

Deadline: Study week 13 @23:59

Project Aim: Simulation & Implementation of a single cycle MIPS processor in system Verilog/VHDL.

1. Project Description

In this project, in part I the individual components of a single cycle MIPS processor should be simulated in system Verilog/VHDL such as **Full Adder with 32 bit inputs, 4 to 1 Multiplexer with 32 bit inputs, 32 bit ALU (Arithmetic Logic Unit)**. During part II of this project, you should implement a complete single cycle MIPS Processor by putting together the individual processor's components.

2. Project Hints

- Read Chapter four from the course book.
- Read the Altera Quartus II Tutorial document.
- Read Appendix B especially section B.4 on page B-20 (Using a Hardware Description Language) & section B.5 on page B-26 (Constructing a Basic Arithmetic Logic Unit).
- Try to understand the Verilog code on page B-25, Fig. B.4.2: A Verilog definition of a 4-to-1 Multiplexer with 32-bit inputs, using a case statement.
- Try to understand the Verilog code on page B-25, Fig. B.4.3: A Verilog behavioral definition of a MIPS ALU.
- Try to understand the Verilog code on page B-37, Fig. B.5.15: A Verilog behavioral definition of a MIPS ALU.
- Try to understand the Verilog code on page B-38, Fig. B.5.16: The MIPS ALU Control: a simple piece of Combinational Control Logic.
- After installing the Verilog software (Altera Quartus II Web Edition), try to simulate the Verilog codes above in System Verilog.

3. About the Verilog software (Altera Quartus II)

Quartus II Web Edition is a free version of the professional-strength Quartus™ II FPGA design tools. It allows students to enter their digital designs in schematic or using either the system Verilog or **VHDL (Very High Speed Integrated Circuit Hardware Description Language)**. After entering the design, students can simulate their circuits using ModelSim™ Altera Starter Edition, which is available with the Altera Quartus II Web Edition. Quartus II Web Edition also includes a built-in logic synthesis tool supporting both system Verilog and VHDL. To get more information about the Altera Quartus II, please refer to the tutorial document.

You should write a short project report (3 to 5 pages) including the simulation results and explaining briefly how those results are obtained in system Verilog/VHDL.

Your names and registration numbers (3 students per group) should appear both on the project report.

Note: Plagiarism, i.e, copying from your group members, will be considered as cheating. This will be checked after the submission of your project reports and attached Verilog codes.

Deadline: you should submit your report in pdf format to the following e-mail address:

wir13.rmu@gmail.com not later than study week 13 @23:59.

Project presentation: After submitting your project report, each group will book a time slot for the project presentation, which will be announced later. Each member of the project group will be examined individually. Project presentations will take place during study weeks 14 & 15.