Computer Organization, Spring 2018

Lab 3: Cache Simulator

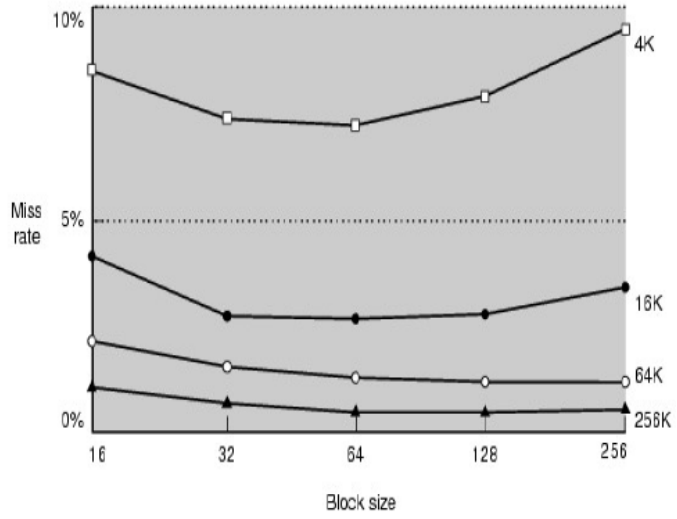
Due: 2018/08/16

1. Goal

Cache performance is important for system performance. In this lab, you are asked to simulate cache behaviors by C/C++ style cache simulators. By this training, you would understand the performance difference between different cache architectures.

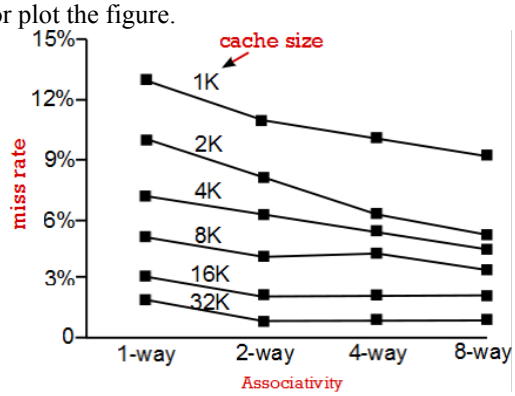
2. Basic Problem (50%)

a. **“direct_mapped_cache.cpp” -**
A simple cache simulator. You should modify this simulator so that it can output the miss rate of the cache. (Hint: see pdf of chapter 5 in page 4.) Please take the file "ICACHE.txt" and "DCACHE.txt" that are provided by the TA, as inputs of the simulator and then run it. First, change the parameters (cache size or block size) when you do the simulation. Then draw a graph as the following example and describe the reason of rise and fall of the lines in the report. (Please separate ICACHE from DCACHE)



3. Advanced Problem (30%)

LRU stands for Least-Recently Used, which is a replacement policy of choosing the one unused for the longest time. In this problem, you have to implement an n-way set-associative cache simulator using LRU (by C/C++, refer to the supplied file “direct_mapped_cache.cpp”). Please name this new simulator as "direct_mapped_cache_lru.cpp". Set block size = 64 bytes. Then input the file "LU.txt" and "RADIX.txt" that are the memory trace from two benchmarks to the simulator. Please draw a graph as the following example and describe the reason of rise and fall of the lines in the report. (Please separate the discussion of LU and RADIX). Also, please compute the total bits (including tags and one valid bit) required for each cache, and show them by table (like following table) or plot the figure.



Associativity / Cache Size	1-way	2-way	4-way	8-way
1K				
2K				
4K				
8K				
16K				
32K				

4. Grade

a. Total score: 110%, **Copy will get 0 point!**

b. Basic score: 50%

c. Advanced score: 30%

d. Report: 30%

e. **Delay: 10% off/ day**

5. Hand in your Assignment

a. Please upload your assignment to E3.

b. Please zip your folder and submit only one *.zip file per team. Either you or your teammate (but not both) may make the submission. Name the *.zip file with your student IDs (e.g., 0516001_0516002.zip). Other filenames and formats such as *.rar and *.7z are **NOT** accepted!

c. Please include **ONLY** *.cpp, your report, and Makefile in the zipped folder - NO OTHER FILE!

d. Command

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if you want to test your basic problem, type the following instruction in the cmd

1. make basic *// to get "direct_mapped_cache" which is an execution file*
2. ./direct_mapped_cache *// execute it*

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if you want to test your advanced problem, type the following instruction in the cmd

1. make advanced *// to get "direct_mapped_cache_lru" which is an execution file*
2. ./direct_mapped_cache_lru *// execute it*

6. Q&A

If you have any question regarding Lab 3, please send email to 黃礪鞍 (vdc159753@gmail.com).