



SICOMM

SCT3811

Direct Conversion Receiver

D/3811/6 August 2021

SCT3811 (enhanced performance)

DATASHEET

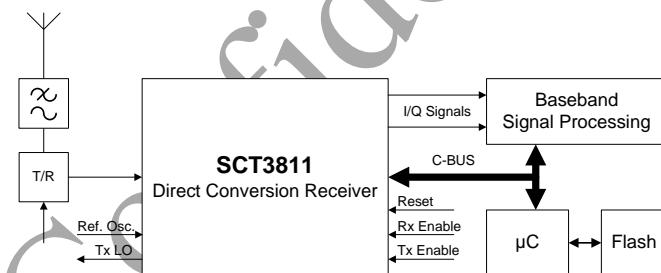
Provisional

Features

- Direct conversion receiver family with PowerTrade™ flexible power vs. performance modes
- Rx single conversion to zero IF, near-zero IF or low IF; zero IF eliminates image responses
- Very high mixer IIP2 for practical zero IF receiver
- 100MHz to 1GHz I/Q demodulator
Extended operation down to 50MHz and up to 1.218GHz
- LNA with gain control
- Precise filtering with 1:2:4 bandwidth select control
- Mixer Bandwidth up to 20MHz
- Local Oscillator
 - Rx LO divide by 2, 4 or 6 modes
 - Tx LO Output with divide by 1, 2, 4, or 6 modes
- 3.0V – 3.6V Low power Operation
- Small size 40-pin VQFN Package

Applications

- Analogue/digital multi-mode radio
- Software Defined Radio (SDR)
- Data telemetry modems
- Satellite communications
- Constant envelope and linear modulation
- Narrowband e.g. 25kHz, 12.5kHz, 6.25kHz
- Wideband Data e.g. >1MHz bandwidth



1 Brief Description

The SCT3811 is a direct conversion receiver IC with PowerTrade™, the ability to dynamically select power vs. performance modes to optimise operating trade-offs. The device includes a broadband LNA with gain control followed by a high dynamic range, very high IIP2, I/Q demodulator. The receiver baseband section includes amplifiers and precise, configurable bandwidth, baseband filter stages. An external LO input is provided with LO dividers are provided for flexible multi-band operation. The device operates from a single 3.3V supply over a temperature range of -40°C to $+85^{\circ}\text{C}$ and is available in a small 40-pin VQFN (Q4) package.

The SCT3811 enables a significant reduction in power by allowing LO phase correction to be turned off. A further reduction is possible by disabling either the I or Q channel in a channel monitoring mode. The device also includes an enhanced performance mode for improved intermodulation in the receive mixers.

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2 History

Version	Changes	Date
6	Section 9.1.3: I/Q demodulator maximum noise figure in Enhanced mode added (17 dB) at 100 MHz	23 rd July 2021
5	Section 9.1.3: I/Q demodulator maximum noise figure in Enhanced mode changed to 17 dB at 450 MHz. Section 9.1.3: I/Q demodulator gain changed to 52 dB (V/V).	30 th November 2020
4	Section 9.1.3: Maximum I/Q amplitude balance changed from $\pm 0.15\text{dB}$ to $\pm 0.2\text{dB}$.	January 2020
3	Section 9.2: Updated Q4 package diagram	December 2019
2	Section 9.1.1: Absolute Maximum Ratings – incorrect pin names corrected. Miscellaneous typographical corrections.	May 2018
1	First published document	January 2018

3 Block Diagram

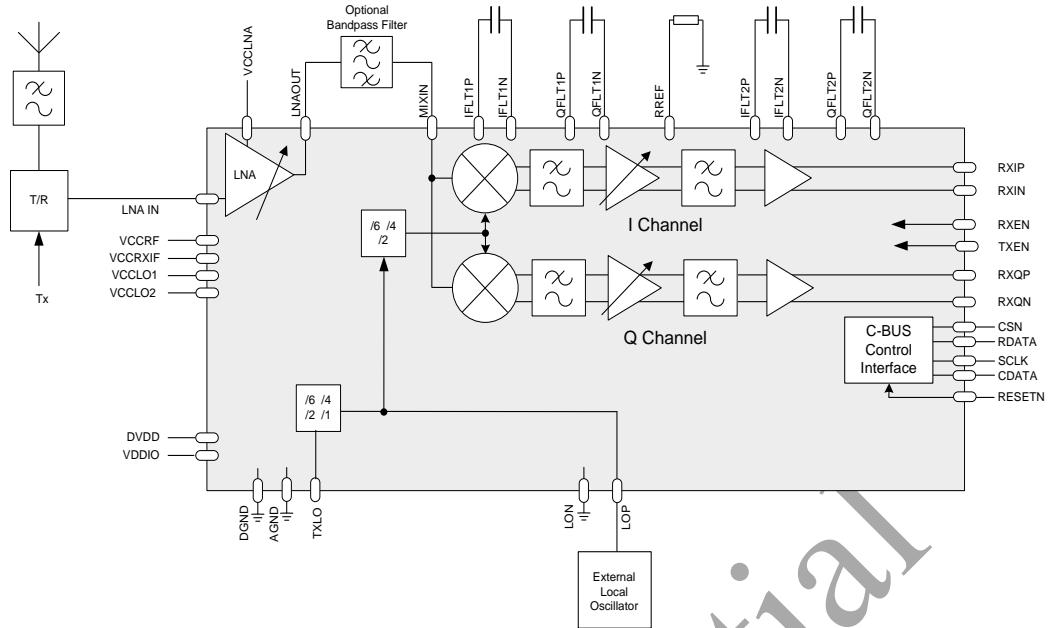


Figure 1 Block Diagram

4 Pin and Signal List

Pin No	Pin Name	Type	Pin Function
1	IFLT2N	IP	I channel 2 nd filter capacitor negative
2	IFLT1P	IP	I channel 1 st filter capacitor positive
3	IFLT1N	IP	I channel 1 st filter capacitor negative
4	VCCRIF	PWR	Supply for baseband circuits
5	VCCLNA	PWR	Supply for LNA
6	LNAIN	IP	LNA input
7	LNAOUT	OP	LNA output
8	VCCRF	PWR	Supply for RF circuits
9	MIXIN	IP	Rx mixer input
10	TXLO	OP	LO output for Tx
11	VCCLO1	PWR	Supply for LO sections
12	LOP	IP	LO positive input
13	LON	IP	LO negative input
14	NC	NC	Do not connect to this pin
15	NC	NC	Do not connect to this pin
16	NC	NC	Do not connect to this pin
17	NC	NC	Do not connect to this pin
18	VCCLO2	PWR	Supply for LO sections
19	NC	NC	Do not connect to this pin
20	NC	NC	Do not connect to this pin
21	DGND	PWR	Digital ground
22	TXEN	IP	Tx Enable
23	RXEN	IP	Rx Enable
24	CSN	IP	C-BUS Chip Select
25	RDATA	TSOP	C-BUS Data output
26	SCLK	IP	C-BUS Clock input
27	CDATA	IP	C-BUS Data input
28	RESETN	IP	C-BUS/Device Reset (Reset when pin Low)
29	DVDD	PWR	Supply to digital circuits
30	VDDIO	PWR	Supply to C-BUS circuits
31	RREF	IP	Reference resistor for I/Q Filters
32	QFLT1N	IP	Q channel 1 st filter capacitor negative
33	QFLT1P	IP	Q channel 1 st filter capacitor positive
34	QFLT2N	IP	Q channel 2 nd filter capacitor negative
35	QFLT2P	IP	Q channel 2 nd filter capacitor positive
36	RXQP	OP	RxQ positive output
37	RXQN	OP	RxQ negative output
38	RXIP	OP	Rxi positive output
39	RXIN	OP	Rxi negative output
40	IFLT2P	IP	I channel 2 nd filter capacitor positive
EXPOSED METAL PAD	AGND	PWR	The exposed metal pad must be electrically connected to analogue ground.

Total = 41 Pins (40 pins and central, exposed metal ground pad)

Notes:	I/P	=	Input	T/S	=	3-state Output
	O/P	=	Output	NC	=	No Connection
	BI	=	Bidirectional	PWR	=	Power

4.1 Signal Definitions

Signal Name	Pins	Usage
V_{max}		The maximum value of the supplies DV_{DD} and AV_{DD}
AV_{DD}	VCCRF, VCCRXIF, VCCLO VCCLNA (see note)	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
VDD_{IO}	VDDIO	Power supply voltage for digital interface (C-BUS)
DV_{SS} (GND)	DGND	Ground for digital circuits
AV_{SS} (GND)	AGND	Ground for analogue circuits

Table 1 Definition of Power Supply and Reference Voltages

Note: The LNA has a separate power connection pin to provide isolation of non-differential signals. This may be connected to a common external supply with suitable de-coupling.

5 External Components

5.1 Power Supply and Decoupling

The SCT3811 has separate supply pins for the analogue and digital circuitry; a 3.3V nominal supply is recommended for all circuits but the data interface can run at a lower voltage than the rest of the device by setting the VDDIO supply to the required interface voltage.

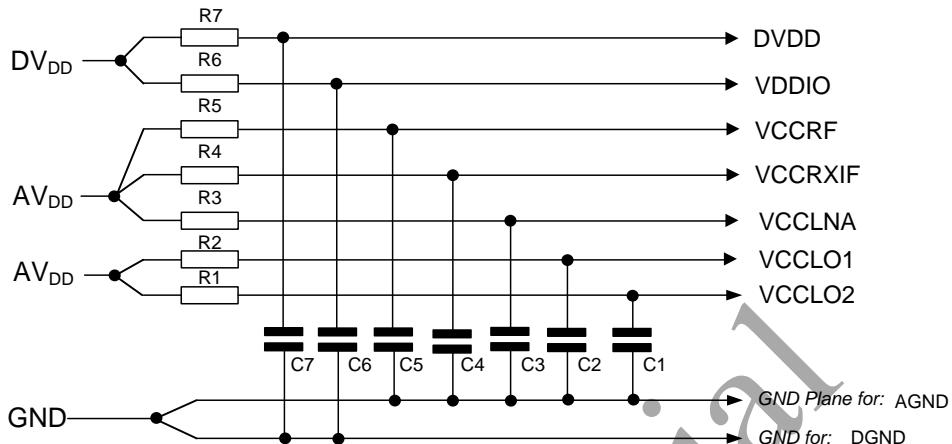


Figure 2 Recommended Power Supply Connections and Decoupling

C1	10nF	R1	10Ω
C2	10nF	R2	3.3Ω
C3	33pF//10nF	R3	3.3Ω
C4	10nF	R4	3.3Ω
C5	10nF	R5	3.3Ω
C6	10nF	R6	10Ω
C7	10nF	R7	10Ω

Table 2 Decoupling Components

Notes:

1. Maximum Tolerances: Resistors $\pm 5\%$, capacitors $\pm 20\%$.
2. It is expected that any low-frequency interference on the 3.3 Volt supply will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. It is particularly important to ensure that there is no interference from the VDDIO (which supplies the digital I/O) or from any other circuit that may use the DV_{DD} supply (such as a microprocessor), to sensitive analogue supplies (AV_{DD}). It is therefore advisable to use separate power supplies for digital and analogue circuits.
3. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well. This may be achieved cost effectively by using the resistor and capacitor values shown. The use of resistors results in small dc voltage drops (up to approx 0.1V). Choosing resistor values approximately inversely proportional to the dc current requirements of each supply ensures the dc voltage drop on each supply is reasonably matched. In any case, the resultant dc voltage change is well within the design tolerance of the device. If higher impedance resistors are used (not recommended) then greater care will be needed to ensure the supply voltages are maintained within tolerance, even when parts of the device are enabled or disabled.
4. It is advisable to have separate ground planes for analogue and digital circuits.
5. Separate regulators for local oscillator sections (VCCLO1, VCCLO2) may be beneficial depending on circuit noise and type of regulator and this is why two AV_{DD} connections are shown.

5.2 Receiver

5.2.1 LNA

The following sections show plots and tables of the LNA input (S_{11}) and output (S_{22}) impedance. Separate data is shown for the 50Ω and 100Ω output modes which are selected by $LNAZ_0$ bit in the Rx Gain Register (b3, \$16; see section 7.7.1).

Note that at low frequencies capacitive loads on the LNA output are not recommended, a high-pass matching network is preferred.

50Ω Mode

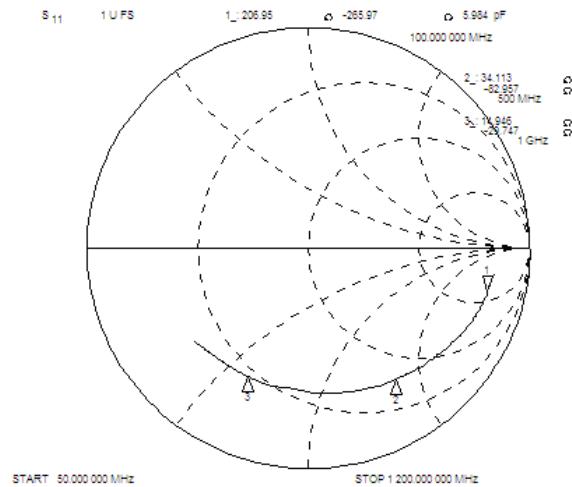


Figure 3 LNA S_{11} (50Ω Mode)

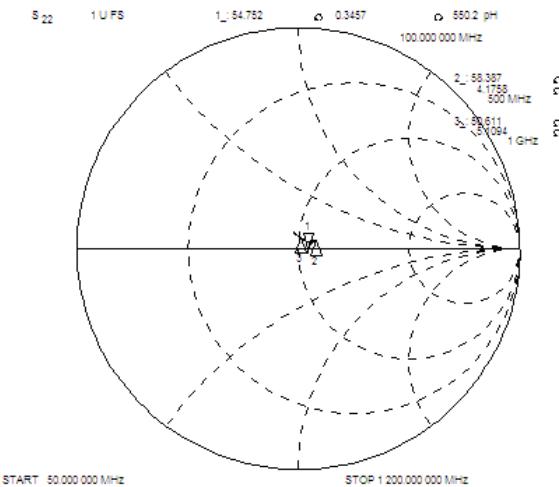
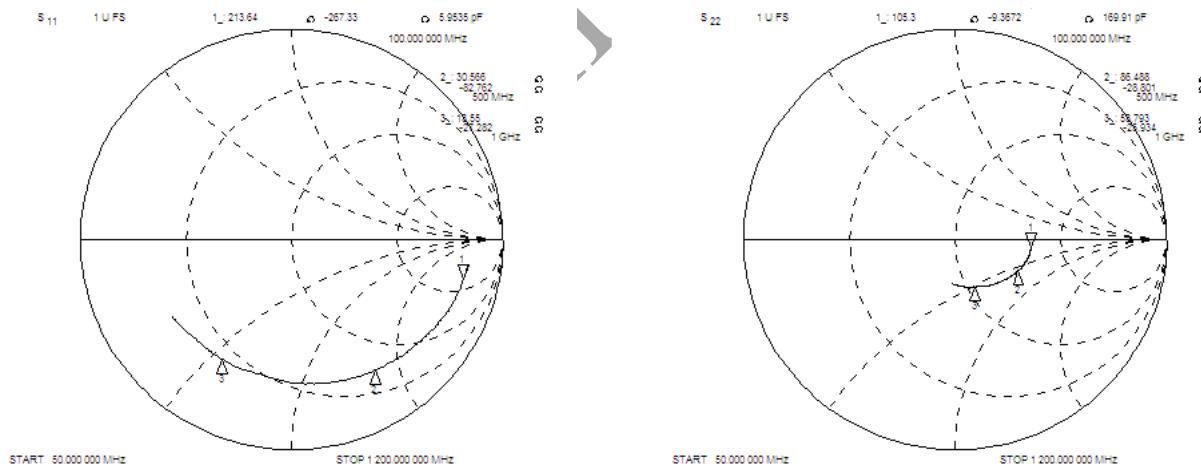


Figure 4 LNA S_{22} (50Ω Mode)

Freq (MHz)	S_{11}		S_{22}	
	Impedance (Ω -/+j Ω)	Equivalent Parallel Circuit (R//C)	Impedance (Ω -/+j Ω)	Equivalent Parallel Circuit (R//C)
50	347 - j296	598.9R // 4.5pF	54.4 - j2.4	54.5R // 2.6pF
100	208 - j263	540.7R // 3.7pF	54.8 + j0.4	54.8R
150	129 - j217	496R // 3.6pF	55.3 + j1.7	55.4R
200	93 - j181	444.5R // 3.5pF	56.1 + j2.9	56.3R
250	72 - j154	401.1R // 3.4pF	56.9 + j3.5	57.1R
300	58 - j130	351R // 3.4pF	57.4 + j3.9	57.6R
350	49 - j114	318R // 3.4pF	57.7 + j4.0	58.0R
400	42 - j102	286.5R // 3.3pF	58.1 + j3.9	58.4R
450	37.7 - j91	256.3R // 3.3pF	58.4 + j4.0	58.7R
500	33.9 - j83	235.3R // 3.3pF	58.4 + j4.2	58.7R
550	29.7 - j74	211.8R // 3.4pF	58.3 + j4.1	58.6R
600	27.0 - j66	190.6R // 3.4pF	57.9 + j3.9	58.2R
650	24.7 - j61	173.1R // 3.5pF	57.3 + j3.8	57.6R
700	22.8 - j55	154.9R // 3.5pF	56.7 + j3.9	57.0R
750	21.3 - j50	136.7R // 3.6pF	55.9 + j3.7	56.1R
800	19.9 - j45	121.5R // 3.7pF	55.3 + j3.6	55.5R
850	18.7 - j41	107R // 3.8pF	54.3 + j3.6	54.5R
900	17.2 - j37.0	96.7R // 3.9pF	52.8 + j3.9	53.1R
950	15.7 - j32.9	84.6R // 4.1pF	51.5 + j4.7	51.9R
1000	14.8 - j29.1	72R // 4.3pF	50.7 + j5.1	51.2R

Table 3 LNA S_{11} and S_{22} Impedances and Parallel Equivalent Circuit in 50Ω Mode100Ω ModeFigure 5 LNA S_{11} (100Ω Mode)Figure 6 LNA S_{22} (100Ω mode)

Freq (MHz)	S ₁₁		S ₂₂	
	Impedance (Ω -/+j Ω)	Equivalent Parallel Circuit (R//C)	Impedance (Ω -/+j Ω)	Equivalent Parallel Circuit (R//C)
50	355 - j291	592.6R // 4.4pF	106 - j7.35	106.6R // 2.1pF
100	210 - j267	549.1R // 3.7pF	105 - j9.5	106R // 1.4pF
150	128 - j222	510.6R // 3.6pF	104 - j2.8	105.7R // 1.2pF
200	92 - j186	469.9R // 3.4pF	103 - j15.7	105.3R // 1.2pF
250	70 - j157	422.4R // 3.4pF	101 - j18.6	104.4R // 1.1pF
300	56 - j134	376.9R // 3.4pF	98 - j21.4	103R // 1.1pF
350	45 - j117	345.3R // 3.4pF	96 - j23.9	101.5R // 1.1pF
400	38 - j103	313.1R // 3.4pF	93 - j26.2	99.9R // 1.1pF
450	34.1 - j91	279.2R // 3.4pF	90 - j27.8	98.3R // 1.1pF
500	30.5 - j82	253R // 3.4pF	87 - j28.9	96.1R // 1.1pF
550	26.4 - j73	228.9R // 3.5pF	83 - j29.7	93.7R // 1.1pF
600	24.0 - j66	203.6R // 3.6pF	80 - j30.5	91.3R // 1.1pF
650	21.7 - j59	183.3R // 3.7pF	76 - j30.7	88.6R // 1.1pF
700	19.9 - j53	162.3R // 3.8pF	73 - j30.5	85.6R // 1.1pF
750	18.7 - j47.7	140.8R // 3.9pF	69 - j30.5	82.6R // 1.1pF
800	17.5 - j42.8	122.2R // 4pF	66 - j30.0	79.7R // 1.1pF
850	16.5 - j38.3	105.5R // 4.1pF	63 - j29.5	76.7R // 1.2pF
900	15.4 - j34.4	92.2R // 4.3pF	60 - j28.4	73R // 1.2pF
950	14.2 - j30.5	79.6R // 4.5pF	57 - j27.1	69.5R // 1.2pF
1000	13.4 - j26.7	66.6R // 4.8pF	54 - j26.0	66.3R // 1.2pF

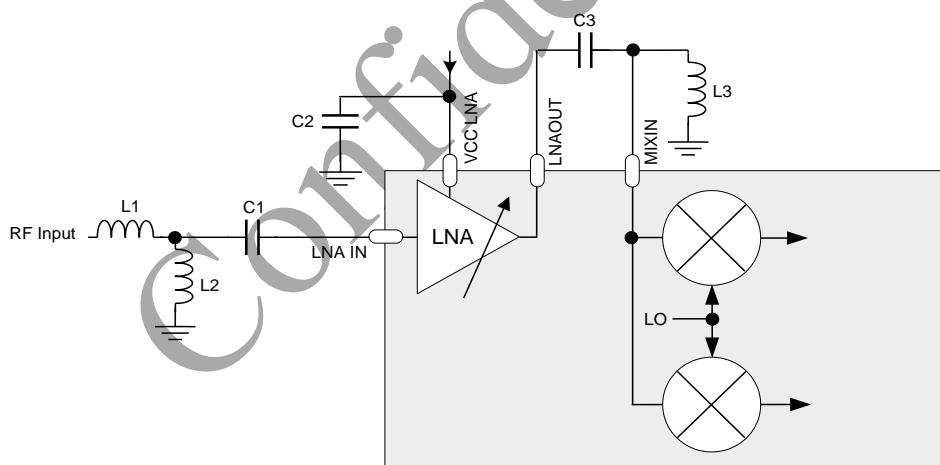
Table 4 LNA S₁₁ and S₂₂ Impedances and Parallel Equivalent Circuit in 100Ω Mode

Figure 7 Recommended LNA Configuration and Inter-stage Match

C1	1nF	L1	150nH
C2	33pF // 10nF	L2	2.7pF (capacitor)
C3	18pF	L3	150nH

Table 5 150MHz LNA and Inter-stage Components (100Ω output mode)

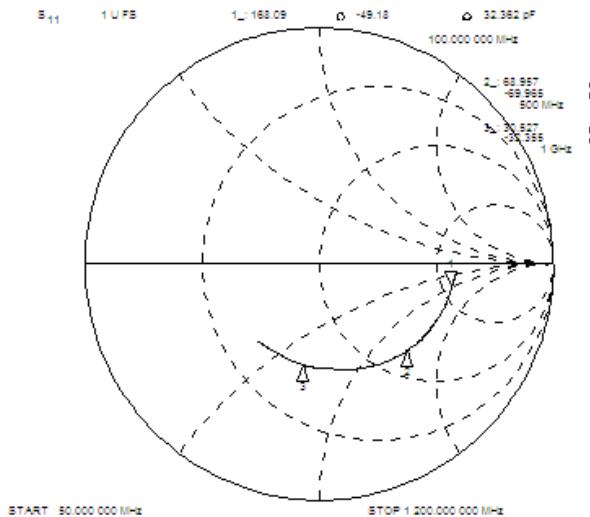
C1	1nF	L1	39nH
C2	33pF // 10nF	L2	82nH
C3	10pF	L3	27nH

Table 6 450MHz LNA and Inter-stage Components (100Ω output mode)

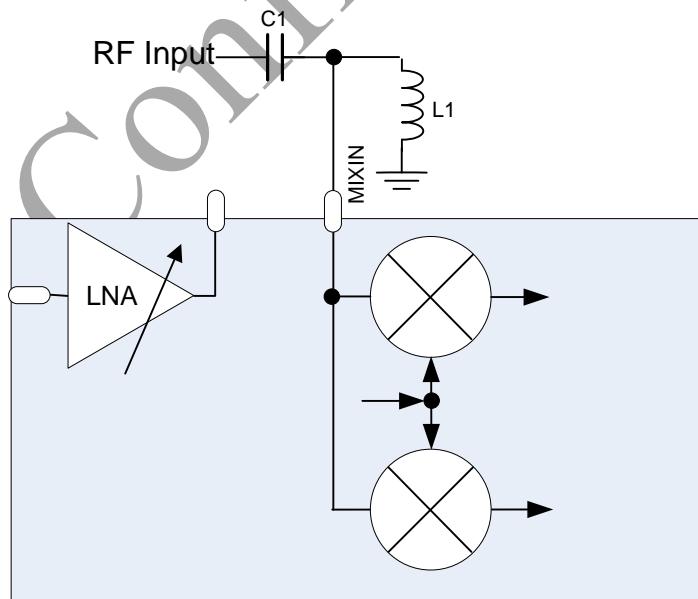
C1	100pF	L1	12nH
C2	33pF //10nF	L2	8.7nH
C3	4.7pF	L3	5.6nH

Table 7 900MHz LNA and Inter-stage Components (50Ω output mode)**5.2.2 Mixers and Baseband Section**

Figure 8 is a plot of the typical Rx Mixer input impedance; gives the measured impedances and the equivalent parallel circuit at some particular frequencies.

**Figure 8 Rx Mixer Input Impedance**

Frequency (MHz)	Impedance (Ω / $+j\Omega$)	Parallel Equivalent Circuit ($R // pF$)
50	172.74-j31.22	178.38R//3.23pF
100	162.72-j47.25	176.44R//2.62pF
150	148.61-j59.99	172.83R//2.48pF
200	132.91-j69.33	169.07R//2.46pF
250	116.95-j74.15	163.96R//2.46pF
300	101.79-j75.64	158R//2.5pF
350	88.21-j74.62	151.33R//2.54pF
400	76.188-j71.96	144.15R//2.61pF
450	66.61-j69.13	138.36R//2.65pF
500	58.42-j65.09	130.94R//2.71pF
550	52.03-j61.31	124.28R//2.74pF
600	46.01-j57.03	116.7R//2.82pF
650	41.25-j52.94	109.19R//2.88pF
700	37.19-j49.13	102.15R//2.94pF
750	34.2-j45.37	94.39R//2.98pF
800	31.82-j41.75	86.6R//3.01pF
850	29.54-j38.33	79.28R//3.06pF
900	27.05-j35.15	72.73R//3.16pF
950	24.62-j31.62	65.23R//3.3pF
1000	22.89-j28.17	57.56R//3.4pF
1050	21.58-j24.89	50.29R//3.48pF
1100	20.55-j21.44	42.92R//3.52pF
1150	19.56-j18.01	36.14R//3.53pF
1200	18.55-j14.59	30.03R//3.47pF

Table 8 Rx Mixer Input Impedances and Parallel Equivalent Circuit**Figure 9 1218MHz Recommended Mixer Input Configuration**

C1	8.2pF	L1	1.8nH
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Table 9 1218MHz Mixer Input Matching Components

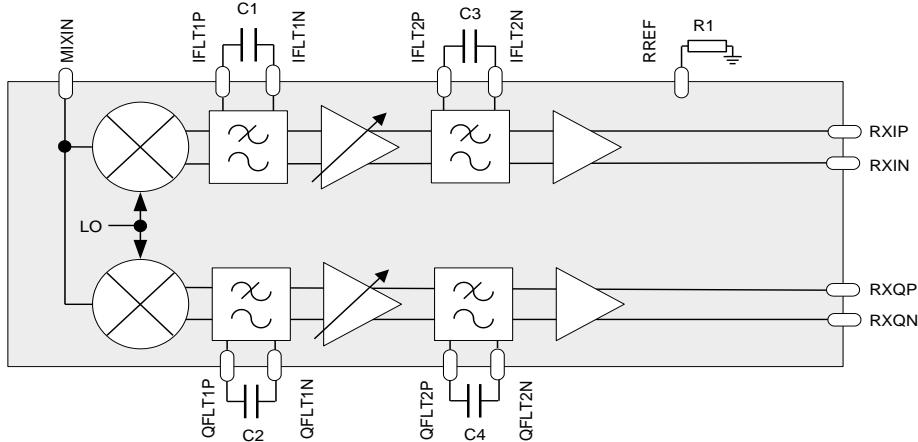


Figure 10 Recommended Receiver Circuit

C1	1.5nF	C4	3.9nF
C2	1.5nF	R1	10kΩ
C3	3.9nF		

Table 10 Receiver Components

The bandwidth of the first baseband filters is set by capacitors C1 and C2. Capacitors C3 and C4 together with the reference resistor R1 set the bandwidth of the second baseband filters. Component selection will vary depending on the desired filter bandwidths. For further details see sections 6.2.2 and 6.2.3.

5.3 Local Oscillator

5.3.1 Local Oscillator Input

LON and LOP signals form a differential signal pair however the LO input may be driven by a single-ended source, in which case pin LOP should be connected to the LO signal and LON may be connected directly to ground. The inputs have internal ac coupling, so external dc blocking capacitors are not required.

5.4 RESETN

The RESETN pin generates a reset signal when low. The RESETN pin has an internal pull-up resistor of 100kΩ connected to VDDIO.

6 General Description

The architecture of the SCT3811 is shown in Figure 1. The SCT3811 is a receiver IC featuring very high IIP2 I/Q demodulators intended for use as a direct conversion receiver to zero IF, near-zero IF and low IF.

The receiver is fully integrated with a Low Noise Amplifier (LNA) preceding the down-converter section. The LNA may be configured with one of two possible output impedance settings (100Ω or 50Ω). With the 50Ω mode selected, there is more gain available but the circuit will consume an additional 2mA of current. The 50Ω mode has primarily been included for use at frequencies of 450MHz or higher. It should be noted that as the output impedance is not the same for each setting, the required matching components between the LNA and mixer will be different for each case.

The high-linearity down-converting mixers are immediately followed by a baseband filter stage. The bandwidth of this section is set by external capacitors. This first stage of filtering is designed to remove off-channel blocking signals prior to baseband amplification. Following these filters, gain is applied via a variable gain amplifier. Further filtering is then applied and again the bandwidth of the filters is determined by external capacitors. A reference resistor must also be fitted; this is used to calibrate the internal filter circuits to ensure the cut-off point of the filters is accurately controlled. This system allows effective correction for the analogue response to be applied in signal processing following the SCT3811. The output of the SCT3811 is differential I/Q signals.

The receiver I/Q chain includes the facility to correct for inherent dc offsets in the hardware. This process is intended to optimise the dynamic range of the system and must be controlled by the microprocessor or DSP that processes the I/Q signals from the SCT3811. DC offsets are a well-known issue with direct conversion receivers. In dynamic signal environments dc offset removal algorithms will be required to track and remove dc offsets generated by off-channel signals. Very high I/Q mixer IIP2 performance minimises such offsets. The receiver sections have a low power mode that reduces current. This mode may be used when reduced intermodulation performance is acceptable.

The Local Oscillator section allows the Rx LO signal to be divided by 2, 4 or 6. There is also a Tx LO output provided and the Tx LO signal may be divided by 1, 2, 4 or 6.

All features of the SCT3811 may be controlled by the C-BUS control interface.

The following sections describe specific features of the SCT3811.

6.1 General Operation

6.1.1 Rx/Tx Enable

The SCT3811 has Tx Enable and Rx Enable pins and the same function can be accessed via C-BUS using the General Control Register (section 7.2). The logical signals 'Tx ON' and 'Rx ON' are the ORed combination of the C-BUS signal and the hardware signals as shown in Table 11. Thus either C-BUS or hardware enable signals may be used, with the unused mode being set to '0'.

Tx (or Rx) Enable Pin	C-BUS Tx (or Rx) Enable	'Tx ON' (or 'Rx ON') Result
0	0	0
1	0	1
0	1	1
1	1	1

Table 11 Tx (or Rx) Enable Operation

'Tx ON' enables the following sections of the device:

- Tx divider (see also Figure 1 and section 7.9.1).

'Rx ON' enables the following sections of the device:

- LNA
- Down-converters and I/Q baseband amplifiers
- Rx LO divider

6.2 Receiver Operation

6.2.1 DC Offset Correction

Digitally-controlled dc offset correction is provided which is capable of reducing the offset to 25mV or less for errors of up to +/-800mV. This represents a reduction in dynamic range of about 0.1dB for a typical ADC input signal range (2Vp-p) and is therefore negligible. The required correction must be measured externally as such measurements are application specific. The correction is applied close to the start of the I/Q baseband chain and therefore maximises dynamic range in the analogue sections.

The correction is applied in a differential manner so positive and negative corrections are possible; see Figure 11. This allows the dc to be corrected to the nominal dc bias level. The voltage sources are scaled in a binary fashion so multiple sources can be added to provide the desired correction. The same arrangement applies independently on both I and Q channels.

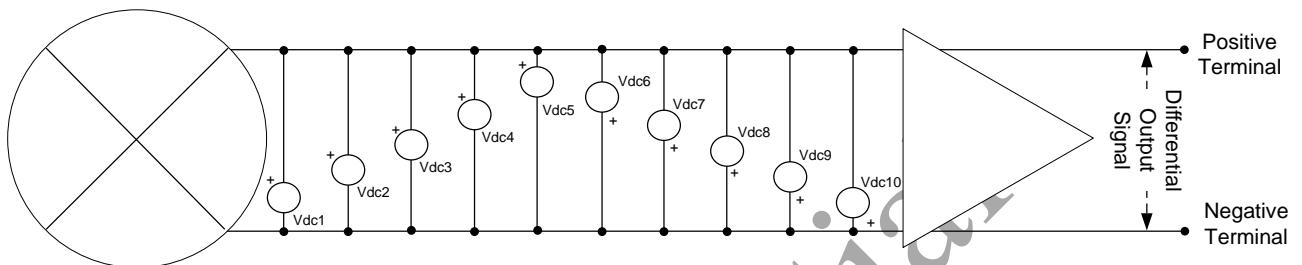


Figure 11 Simplified Schematic of How DC Offset Corrections are Applied

Source	Voltage Correction at Output for Maximum Gain in Baseband Amplifiers	Correction Polarity
Vdc1	25mV	Positive terminal increase, Negative terminal decrease
Vdc2	50mV	Positive terminal increase, Negative terminal decrease
Vdc3	100mV	Positive terminal increase, Negative terminal decrease
Vdc4	200mV	Positive terminal increase, Negative terminal decrease
Vdc5	400mV	Positive terminal increase, Negative terminal decrease
Vdc6	25mV	Negative terminal increase, Positive terminal decrease
Vdc7	50mV	Negative terminal increase, Positive terminal decrease
Vdc8	100mV	Negative terminal increase, Positive terminal decrease
Vdc9	200mV	Negative terminal increase, Positive terminal decrease
Vdc10	400mV	Negative terminal increase, Positive terminal decrease

Table 12 DC Offset Correction Adjustments

6.2.2 Receiver Filters and Bandwidth Options

The I and Q channels incorporate two stages of filtering to reduce blocking signals and to attenuate nearby channels. This allows the wanted signal to be maximised without significant distortion being introduced as a result of unwanted larger signals saturating the later amplification stages.

The SCT3811 supports multiple channel bandwidths, providing scalable filtering in the baseband (I/Q) chain. Two filter stages are provided. The post mixer filter provides rejection of large off-channel signals such as those typically used in blocking tests. With this protection in place some gain is provided before narrower filters that provide rejection of the adjacent channel. Following this filter, the remainder of the receiver gain is provided. Both filter stages have single-pole characteristics, having -3dB frequency points set by separate external capacitors.

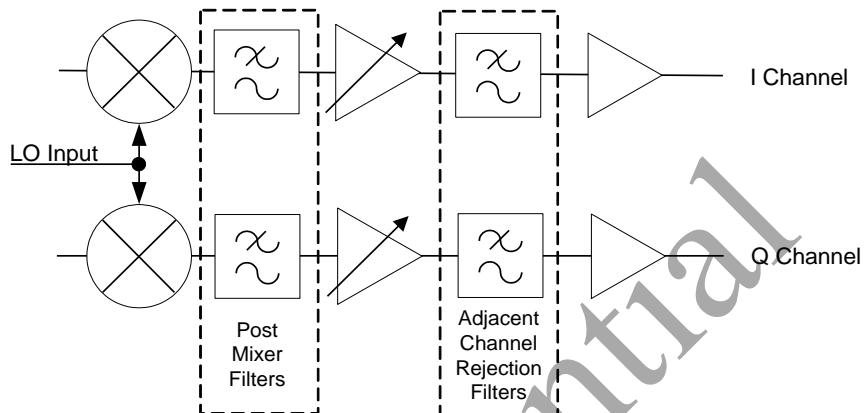


Figure 12 Baseband I/Q Filtering

After setting the second filter stage bandwidth via external capacitors, the bandwidth can then be scaled under serial control to allow multiple channel bandwidths to be supported by the SCT3811. A typical requirement is to support 6.25kHz, 12.5kHz and 25kHz channels, so the scaling of the Adjacent Channel Rejection (ACR) filter is 1 : 2 : 4 via a bandwidth mode control. Using the recommended external capacitors for a 6.25kHz design (see 5.2.2), the ACR filter bandwidth (-3dB) is 2kHz. This provides 9dB rejection of the adjacent channel and 15dB rejection at 12.5kHz. Using the bandwidth scaling control, the 2kHz filter bandwidth can then be changed to 4kHz or 8kHz (see Rx Control Register, section 7.3), without changing external components. See also section 8.1.6.

The ACR filter may introduce some deterministic distortion in the signal passband, this distortion can be compensated by using filters external to the SCT3811; see section 6.2.3 for further information.

The scaling of the post-mixer filter is less critical. The bandwidth (-3dB), using the recommended values, is approximately 88kHz (at maximum gain). This should be suitable for all the channel bandwidths up to 25kHz, so no scaling is provided. Note that the bandwidth of this section will reduce by 30% (typ.) as gain is reduced in the baseband section.

6.2.3 Baseband Filter Design and Required Correction

The pole frequencies of the filter stages are set by the addition of external capacitors (see also section 5.2.2); the resistors are internal to the chip and those on the second filter stage are trimmed so as to match the external 10kΩ reference resistor¹.

¹ The external resistor should be 1% tolerance or better.

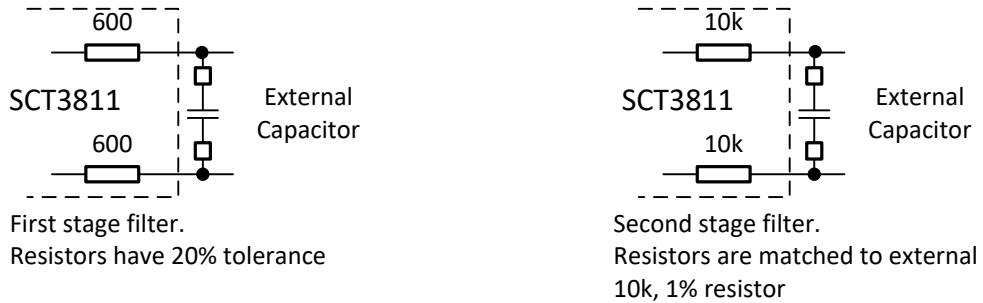


Figure 13 Schematic Representation of Filters used in the I and Q Paths

Filtering close to the passband distorts the signal and increases the BER, so it is necessary to provide correction for the filter distortion in subsequent external digital filtering.

Both filter stages are single-pole filters. The first filter stage is designed to reduce blocking signals and it will typically be set at 4 x the maximum required channel spacing. As a result, tolerance is not particularly critical and it is usually not necessary to compensate the wanted signal for this filter. The second filter is designed to operate close to, or within, the passband. It is therefore important that compensation is provided for the wanted signal.

Different modulation schemes occupy different bandwidths within a channel, so optimisation of the filter positioning will vary depending on the modulation scheme. Some experimentation may be required to get the best results but, as a guide, the second filter stage should have its frequency set to between 30% and 40% of the channel spacing. The aim is to reduce adjacent and close-in channels as much as possible. Provided the filter effects are compensated for later, the lowering of the signal amplitude at the band edges is usually well tolerated, although the extent of this will depend on the modulation scheme used.

The SCT3811 allows up to three different channel spacings to be selected via the C-BUS interface. So if, for example, the three channel spacings required are 6.25kHz, 12.5kHz and 25kHz, then the first filter should be set at a nominal desired frequency to ensure large blocking signals are rejected, typically a cut off frequency around 100kHz would be suitable. If only two channel spacings are required, of 6.25kHz and 12.5kHz for example, then it would be slightly beneficial to set the post mixer filter bandwidth to 50kHz.

Note that the three channel spacings are always in a 1:2:4 ratio relative to the smallest channel spacing, which is set by external components.

The second stage filter capacitor should be selected for the smallest bandwidth requirement. The calculation for the capacitor value is as follows:

$$C = \frac{1}{2\pi f 20,000}$$

Where f = filter pole frequency (-3dB point).

So a capacitor of 4nF would yield a frequency pole of 1989Hz. This may be a typical figure when using a channel spacing of 6.25kHz. To maintain the accuracy of the compensation the capacitor must have a low temperature coefficient and tolerance better than or equal to 2%.

A compensation filter would need to be applied in the digital domain having the inverse characteristic. This would be:

$$H(s) = 1 + \frac{s}{2\pi f}$$

This would normally be implemented as a FIR filter. It should be followed with another non-critical FIR that rolls off the signal when out of band. This second filter may be part of a required channel filter.

Selecting 2x or 4x bandwidth will require the compensation filter to be adjusted in proportion.

The first stage filter capacitor may be calculated in a similar way:

$$C = \frac{1}{2\pi f 1200}$$

Where f = filter pole frequency (-3dB point).

So a capacitor of 1.5nF would yield a frequency pole of 88.4kHz. This may be a typical figure if the maximum channel spacing required were 25kHz. There is a wider tolerance on this, as the internal resistors are not trimmed. Consequently it is not required to have a low tolerance value on the first stage filter capacitor.

Should it be required to have this closer to the passband then a correction filter may be required. This would have the same form as for the correction filter for the second stage. In general a margin of at least 50% between the filter cut-off and wanted channel is recommended to allow for the resistor tolerances and bandwidth change with gain settings noted in section 6.2.2.

Because both filter stages are handling large dynamic signals, the linearity of the external capacitors is important. Use of good dielectric materials is recommended; poor linearity could result in a degradation of the on-channel signal in the presence of large off-channel interferers.

6.2.4 Operation at Wider Bandwidths

It is possible to use a much wider channel bandwidth than those used as examples elsewhere in this document. For maximum I/Q bandwidth (1.6MHz) capacitors C1, C2, C3 and C4 in Figure 10 should be removed. In this case the filter calibration circuit should be disabled using b7 of the VCO Control Register (\$25); see section 7.9.1.

7 C-BUS Interface and Register Descriptions

The C-BUS serial interface supports the transfer of data and control or status information between the SCT3811's internal registers and an external host. Each C-BUS transaction consists of the host sending a single Register Address byte, which may then be followed by zero or more data bytes that are written into the corresponding SCT3811 register, as illustrated in Figure 14.

Data sent from the host on the Command Data (CDATA) line is clocked into the SCT3811 on the rising edge of the Serial Clock (SCLK) input. The C-BUS interface is compatible with common μC/DSP serial interfaces and may also be easily implemented with general purpose I/O pins controlled by a simple software routine. Section gives the detailed C-BUS timing requirements.

Whether a C-BUS register is of the read or write type, it is fixed for a given C-BUS register address thus one cannot both read and write the same C-BUS register address. The SCT3811 supports several pairs of C-BUS register addresses in order to read and write the same information.

C-BUS Write-only Registers

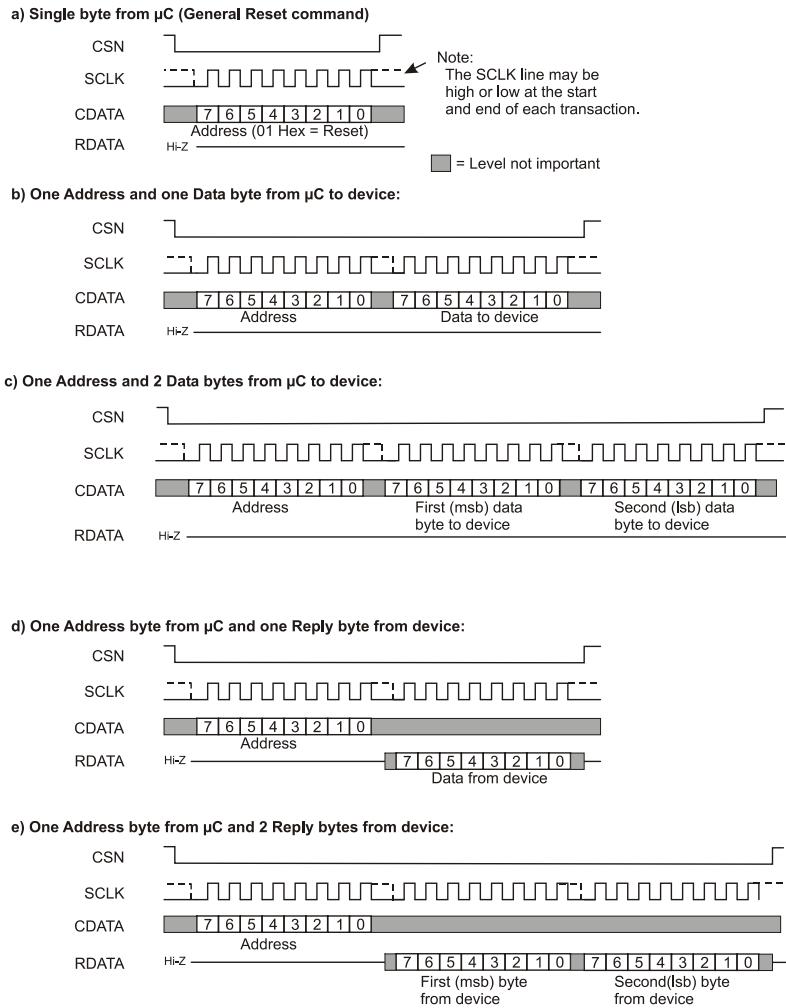
HEX ADDRESS	REGISTER	WORD SIZE (BITS)
\$10	General Reset Register (Address only, no data)	0
\$11	General Control Register, write only	8
\$12	Rx Control Register, write only	8
\$14	LNA IM Control Register, write only	8
\$15	Options Control Register, write only	8
\$16	Rx Gain Register, write only	8
\$17	Extended Rx Offset Register, write only	16
\$25	VCO Control Register, write only	8

C-BUS Read-only Registers

HEX ADDRESS	REGISTER	WORD SIZE (BITS)
\$E1	General Control Register, read only	8
\$E2	Rx Control Register, read only	8
\$E4	LNA IM Control Register, read only	8
\$E5	Options Control Register, read only	8
\$E6	Rx Gain Register, read only	8
\$E7	Extended Rx Offset Register, read only	16
\$D5	VCO Control Register, read only	8

Notes:

- All registers will retain data if DVDD and VDDIO pins are held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices, DVDD and VDDIO must be maintained in their normal operating ranges otherwise ESD protection diodes may cause a problem with loading the signals connected to SCLK, CDATA and RDATA pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.

**Figure 14 C-BUS Transactions****7.1 General Reset: \$10 (no data)**

A command to this register resets the device and clears all bits of all registers. The General Reset command places the device into powersave mode.

Whenever power is applied to the DVDD pin, a built-in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. The RESETN pin on the device will also reset the device to the same state.

7.2 General Control Register

7.2.1 General Control: \$11 - 8-bit write only

This register controls general features such as powersave. All bits of this register are cleared to '0' by a General Reset command.

7	6	5	4	3	2	1	0
En Bias	Freq2	Freq1	LP	Reserved	Reserved	RXEN	TXEN

b7 and 4-0:

These bits control power up/power down of the various blocks of the IC. In all cases '1' = power up, '0' = power down.

- b7 Enables BIAS generator
- b4 Enables low power mode. When b4 = '0' the device is operating normally, when b4= '1' the device will have reduced power consumption and reduced intermodulation performance. See also section 8.1.5 regarding other low power modes.
- b3 *reserved*, clear to '0'.
- b2 *reserved*, clear to '0'.
- b1 C-BUS Rx Enable; see section 6.1.1
- b0 C-BUS Tx Enable; see section 6.1.1

b6, b5

These bits optimise the amplitude of the local oscillator path within the device in order to maintain phase balance and noise performance of the receiver mixers over the full range of operating frequencies.

b6	b5	Operation
0	0	100MHz – 150MHz
0	1	150MHz – 300MHz
1	0	300MHz – 700MHz
1	1	700MHz – 1000MHz

7.2.2 General Control: \$E1 - 8-bit read only

This register reads the value in register \$11; see section 7.2.1 for details of bit functions.

7.3 Rx Control Register

7.3.1 Rx Control: \$12 – 8-bit write only

This register controls general features of the receiver such as Powersave. All bits of this register are cleared to '0' by a General Reset command.

7	6	5	4	3	2	1	0
Mix Pwr	IQ Pwr	LNA Pwr	ACR Flt2	ACR Flt1	DC Range	DIV2	DIV1

b7-5 These bits control power up/power down of the various blocks of the IC.
In all cases '0' = power up, '1' = power down.

b7	Disable receiver mixers and divider (see note)
b6	Disable baseband amplifier and filters (see note)
b5	Disable LNA (see note)

Note: These control signals disable the appropriate blocks of the receiver when 'Rx ON' is active. If 'Rx ON' is not active all receiver circuits will be in powersave mode.

b4,3 The baseband I/Q chain provides a narrow filter for rejecting adjacent channel signals. The bandwidth of this filter may be scaled using these bits. For further details see sections 6.2.2, 6.2.3 and 8.1.6.

b4	b3	Function
0	0	Minimum bandwidth
0	1	Intermediate bandwidth
1	0	Maximum bandwidth
1	1	<i>reserved</i> , do not use

b2 When b2 = '0' the range of DC correction of the I/Q output is nominal (see sections 6.2.1 and 7.4). With b2 = '1' the total correction range is twice the nominal specified in section 7.4 with all steps doubled in value. Note: The device provides an alternative method of achieving increased correction range without losing resolution using the Extended Rx Offset Register (\$17); see section 7.8.

b1,0 Receiver LO divider control

b1	b0	Function
0	0	LO divided by 2
0	1	LO divided by 4
1	0	LO divided by 6
1	1	<i>reserved</i> , do not use

7.3.2 Rx Control: \$E2 – 8-bit read only

This read-only register mirrors the value in register \$12; see section 7.3.1 for details of bit functions.

7.4 Rx Offset Register

7.4.1 Rx Offset: \$13 – 8-bit write only

Note: Increased correction range is available using register \$17; see section 7.8. The bits in registers \$13 and \$17 control the same hardware functions with the most recent write to \$17 or \$13 being applicable at any given time; if \$13 is written then QDC5, QDC4, IDC5 and IDC4 in \$17 are automatically set to '0'. All bits of registers \$13 and \$17 are cleared to '0' by a General Reset command.

b7-0 I/Q DC offset correction; see section 6.2.1 for further details. The step size can be doubled using the Rx Control Register (\$12), b2; see section 7.3.1.

The values in the table below are the effects of the offset at the maximum VGA gain (minimum attenuation) setting. They are proportionately lower for lower gain settings (as set by the Rx Gain Register (b2 – b0). The aim of this Rx Offset Register is to allow output offsets to be reduced sufficiently (typically <25mV) to avoid any significant reduction in the dynamic range of any subsequent ADC. It is expected that demodulation software in the baseband processor would be required to correct for the remaining offset as part of the demodulation process.

See also section 8.1.2.

b3 b7	b2 b6	b1 b5	b0 b4	I Channel at maximum gain Q Channel at maximum gain
1	1	1	1	-175mV
1	1	1	0	-150mV
1	1	0	1	-125mV
1	1	0	0	-100mV
1	0	1	1	-75mV
1	0	1	0	-50mV
1	0	0	1	-25mV
1	0	0	0	No correction
0	1	1	1	+175mV
0	1	1	0	+150mV
0	1	0	1	+125mV
0	1	0	0	+100mV
0	0	1	1	+75mV
0	0	1	0	+50mV
0	0	0	1	+25mV
0	0	0	0	No correction

7.4.2 Rx Offset: \$E3 - 8-bit Read only

This read-only register mirrors the value in register \$13; see section 7.4.1 for details of bit functions.

7.5 LNA Intermodulation Control Register

7.5.1 LNA IM Control: \$14 – 8-bit write only

This register controls features of the receiver that support intermodulation optimisation. All bits of this register are cleared to '0' by a General Reset command.

7	6	5	4	3	2	1	0
0	0	IM5	IM4	IM3	IM2	IM1	IM0

b7,6 *reserved, clear to '0'*

b5-0 These bits allow the user to adjust the intermodulation performance of the LNA. The default value is '0' for all the bits. Improved intermodulation can be achieved with a particular value in these bits. For further details see section 8.1.4.

7.5.2 LNA IM Control: \$E4 – 8-bit read only

This read-only register mirrors the value in register \$14; see section 7.5.1 for details of bit functions.

7.6 Options Control Register

7.6.1 Options Control: \$15 – 8-bit write only

All bits of this register are cleared to '0' by a General Reset command.

7	6	5	4	3	2	1	0
IP3X	Reserved	Reserved	Reserved	PDQ	PDI	PHCON	PHOFF

- b7 '1' enables enhanced mixer intermodulation mode in the receive path mixers; normal operation when set to '0'.
- b6 *reserved*, clear to '0'
- b5 *reserved*, clear to '0'
- b4 *reserved*, clear to '0'
- b3 When set '1' this bit will power down all circuitry in the Q path leaving only the I channel active; normal operation (I and Q paths active) when bit is cleared to '0'.
- b2 When set '1' this bit will power down all circuitry in the I path leaving only the Q channel active; normal operation (I and Q paths active) when bit is cleared to '0'.
- b1-0 LO Phase Correction Control

b1	b0	LO Phase Correction
0	0	Enabled
1	1	Powered down
0	1	<i>reserved</i> , do not use
1	0	<i>reserved</i> , do not use

7.6.2 Options Control: \$E5 – 8-bit read only

This register reads the value in register \$15; see section 7.6.1 for details of bit functions.

7.7 Rx Gain Register

7.7.1 Rx Gain: \$16 – 8-bit write only

This register controls receiver gain control. All bits of this register are cleared to '0' by a General Reset command.

7	6	5	4	3	2	1	0
GS1	GS0	LNA Gain2	LNA Gain1	LNA Z_0	G2	G1	G0

b7,6 LNA Gain Control Step: These bits control the LNA gain steps; the nominal step is 6dB however the actual step size can be adjusted by+0.7dB, +1.4dB or +2.8dB, as shown in the table below. For further information see section 8.1.3.

b7	b6	Function
0	0	Nominal step size of 6dB
0	1	Nominal step size + 0.7dB
1	0	Nominal step size+1.4dB
1	1	Nominal step size +2.8dB

b5,4 LNA Gain Control: These bits control the LNA gain in nominal 6dB steps, as shown in table below; see also b7 - b6.

b5	b4	Function
0	0	LNA gain = Nominal
0	1	LNA gain = Nominal -6dB
1	0	LNA gain = Nominal -12dB
1	1	LNA gain = Nominal -18dB

b3 Sets the LNA output impedance. The LNA output impedance is approximately 100Ω if this bit is set to '0' and approximately 50Ω if this bit is set to '1'. If set to 50Ω the gain will be increased but with an additional LNA current consumption of approximately 2mA.

b2-0 I/Q Baseband VGA Control

b2	b1	b0	VGA Level
1	1	1	VGA = -42dB
1	1	0	VGA = -36dB
1	0	1	VGA = -30dB
1	0	0	VGA = -24dB
0	1	1	VGA = -18dB
0	1	0	VGA = -12dB
0	0	1	VGA = -6dB
0	0	0	VGA = 0dB (Maximum gain)

7.7.2 Rx Gain: \$E6 – 8-bit read only

This read only register mirrors the value in register \$16; see section 7.7.1 for details of bit functions.

7.8 Extended Rx Offset Register

7.8.1 Extended Rx Offset: \$17 – 16-bit write only

All bits of this register are cleared to '0' by a General Reset command.

Note 1: the bits in registers \$13 and \$17 control the same hardware functions with the most recent write to \$17 or \$13 being applicable at any given time; if \$13 is written then QDC5, QDC4, IDC5 and IDC4 will automatically be set to '0'.

Note 2: QDC3 and IDC3 have different function in \$13 and \$17; in \$13 QDC3 and IDC3 sets the correction polarity whereas in \$17 the polarity is set by QDC5 and IDC5.

15	14	13	12	11	10	9	8
0	0	QDC5	QDC4	QDC3	QDC2	QDC1	QDC0
7	6	5	4	3	2	1	0
0	0	IDC5	IDC4	IDC3	IDC2	IDC1	IDC0

b13-8,

b5-0 I/Q DC Offset correction; see section 6.2.1

The values in the table below are the effects of the offset at the maximum VGA gain (minimum attenuation) setting. They are proportionately lower for lower gain settings (as set by the Rx Gain Register (b2 – b0). The aim of this Rx Offset Register is to allow output offsets to be reduced sufficiently (typically <25mV) to avoid any significant reduction in the dynamic range of any subsequent ADC. It is expected that demodulation software in the baseband processor would be required to correct for the remaining offset as part of the demodulation process. See also section 8.1.2

b5	b4	b3	b2	b1	b0	I Channel at maximum gain	Q Channel at maximum gain
b13	b12	b11	b10	b9	b8		
1	1	1	1	1	1	-775mV	
1	1	1	1	1	0	-750mV	
						etc. (i.e. binary count, step 25mV)	
1	0	0	1	0	1	-125mV	
1	0	0	1	0	0	-100mV	
1	0	0	0	1	1	-75mV	
1	0	0	0	1	0	-50mV	
1	0	0	0	0	1	-25mV	
1	0	0	0	0	0	No correction	
0	1	1	1	1	1	+775mV	
0	1	1	1	1	0	+750mV	
						etc. (i.e. binary count, step 25mV)	
0	0	0	1	1	1	+175mV	
0	0	0	1	1	0	+150mV	
0	0	0	1	0	1	+125mV	
0	0	0	1	0	0	+100mV	
0	0	0	0	1	1	+75mV	
0	0	0	0	1	0	+50mV	
0	0	0	0	0	1	+25mV	
0	0	0	0	0	0	No correction	

7.8.2 Extended Rx Offset: \$E7 – 16-bit read only

This read-only register mirrors the value in register \$17; see section 7.8.1 for details of bit functions.

7.9 LO Control Register

7.9.1 LO Control: \$25 - 8-bit write only

This register controls the operation of the LO input. All bits of this register are cleared to '0' by a General Reset command.

Note: it is not recommended that the LO input and the VCO are enabled simultaneously.

7	6	5	4	3	2	1	0
FILT_CAL	TXDIV1	TXDIV0	LO Input EN	reserved	reserved	reserved	reserved

b7 This bit, if set to '1', will disable the Filter Calibration System. The default value is '0'.

b6,5 These bits control the output division of the Tx LO signal available at pin TXLO. The LO signal is divided by the factor as shown in the following table.

b6	b5	Function
0	0	Divide by 2
0	1	Divide by 4
1	0	Divide by 6
1	1	No division

b4 This bit controls power up/power down of the LO section, '1' = power up, '0' = power down
 b3 –b0 *reserved*, clear to '0'.

7.9.2 LO Control: \$D5 - 8-bit read only

This register reads the value in register \$25; see section 7.9.1 for details of bit functions.

8 Application Notes

8.1 Typical Receiver Performance

8.1.1 System Performance

This information is intended as a general guide of what can be expected from a SCT3811 receiver design using the on-chip LNA and I/Q down-conversion stages. The measurement circuit uses the component values given in section 5.2. The results are based on measurements from evaluation of the SCT3811 operating at 450MHz (device in normal mode, not enhanced mode). Results are also given for Low Power (LP) mode operation, i.e. General Control Register (\$11) b4 = '1'; see section 7.2.1.

Gain	63dB (62.5dB in LP mode)
Noise Figure:	4.5dB (also 4.5 dB in LP mode)
Input Third Order Intercept Point:	-3dBm (-9dBm in LP mode)
Input Second Order Intercept Point:	62dBm (60dBm in LP mode)

Notes:

Common settings: max gain, max filter bandwidth, freq control bits = 300 to 700MHz, LNA output impedance = 100Ω , LO at x2 (900MHz, level -10dBm), IM Control Register = 0x3F

Gain is measured from RF input (assumed to be 50 Ohm source /load) to differential voltage measured at output of I or Q channels.

Second Order Intercept Point is the average of values measured from differential signals on I and Q; measured at 1MHz offset.

8.1.2 DC Offsets

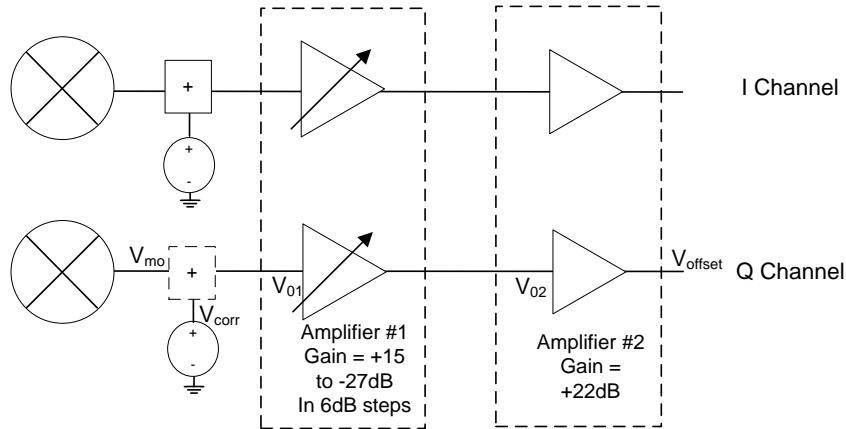
For true direct conversion receivers dc offsets require careful consideration in the receiver demodulator solution. The SCT3811 has been designed to minimise the dc offset challenges by ensuring excellent mixer IIP2 performance.

For Near Zero IF and low IF receiver systems (see section 8.5) the dc offset issues discussed in the following sub-sections can largely be ignored.

8.1.2.1 Static Offsets

To provide an approximate correction of dc offsets use the following procedure: with the attenuation set at minimum (i.e. max gain) measure the offset at the SCT3811 I or Q output, then the table in section 7.4.1 can be used to give the required offset correction. The range double bit (\$12, b2) can be used to increase the correction range if required. Note that at high attenuation settings there may be an additional error due to residual offsets from within the VGA as explained below.

The dc offsets in the SCT3811 baseband path are shown in Figure 15. The voltages are only shown on the Q path but the same considerations apply to the I path. Note that the dc offsets in I and Q paths will be different because they relate to random offsets in a number of components; note also that the I and Q paths are differential and that further details of the dc offset correction mechanism are given in section 6.2.1.



Where:

V_{mo} = dc offset at the output of the mixer

V_{o1} , V_{o2} = input offsets of amplifiers 1 and 2 respectively

V_{corr} = correction voltage (value set in Rx Offset register, \$13)

V_{offset} = dc offset present at the output

Figure 15 I/Q Path dc Offsets

Referring to Figure 15, the approximate dc offset for a given gain setting can be calculated as:

$$V_{offset} = ((V_{mo} + V_{corr} + V_{o1}) \cdot G_1 \cdot G_2) + (V_{o2} \cdot G_2)$$

The offset V_{o2} can be estimated by setting the attenuation in Amplifier #1 to -42dB ($G_1 = -27$ dB) and then measuring V_{offset} , thus $V_{o2} = (V_{offset} / G_2)$. The sum of $(V_{mo} + V_{o1})$ can then be estimated given that the gain setting of G_1 and V_{corr} are known.

Assuming V_{offset} is minimised using V_{corr} at minimum attenuation then increasing the attenuation may result in an increase in V_{offset} , however the error is typically ± 15 mV (± 55 mV absolute maximum). An example of the variation in dc offsets with gain control is shown in Figure 16.

It should be noted that as the attenuation is increased the steps of the offset correction mechanism reduce as the reciprocal of the attenuation. The result is that at maximum attenuation the offset correction steps are

$$25\text{mV} \times 10^{(-42/20)} = 0.2\text{mV}.$$

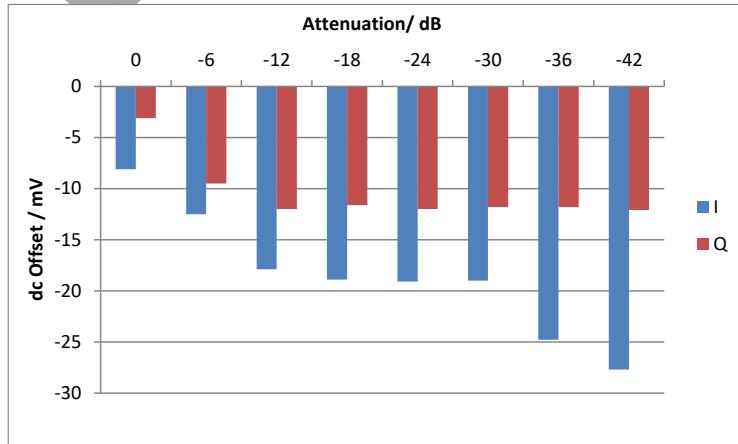


Figure 16 Example Variation in V_{offset} with Gain Control Setting

8.1.2.2 Transient Offsets

When the SCT3811 receiver is enabled there is a small variation in the output dc offset resulting from a change in the thermal conditions of the circuit; this is caused by self-heating of the IC. The effect is small, circa 2mV differential; a typical response is shown in Figure 17. In some radio systems, in particular TDMA systems, the effect may require compensation to avoid an increase in bit errors at the start of reception.

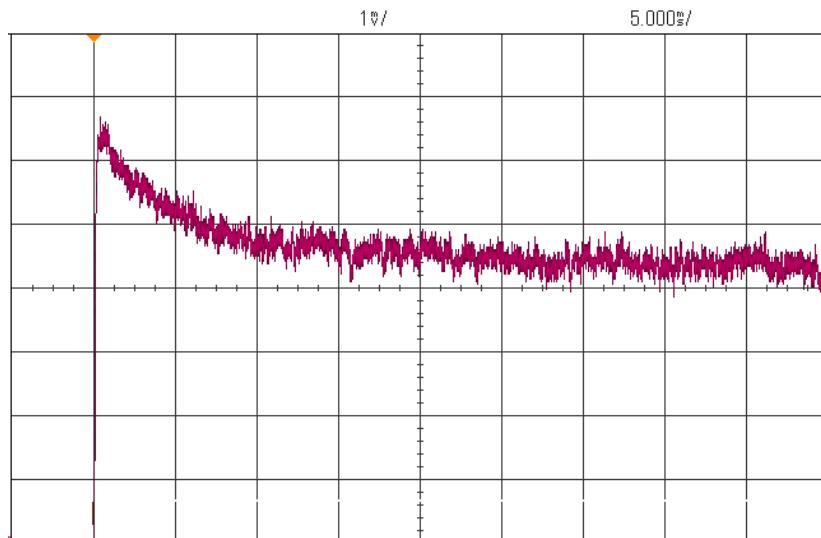


Figure 17 Typical Transient Response, Differential Q Channel, 20°C, no input signal

Notable characteristics of the transients observed in the SCT3811 are:

- the response follows a standard exponential decay ($1 - 1/e^{t/\tau}$)
- the time constant of the response is independent of temperature ($\tau = 5\text{ms}$)
- the amplitude of the transient decreases with reducing temperature (approximately linear relationship)
- the transient amplitude on the I channel is much smaller than that on the Q channel

8.1.2.3 Thermal Drift

In addition to the short-term transient effect discussed in section 8.1.2.2 a longer-term variation in dc offsets occurs until the IC reaches thermal equilibrium. The effect is very slow, taking place over tens of seconds. As a result this effect usually has minimal effect on system operation because for short bursts of reception the variation is negligible and for continuous reception normal dc tracking / correction algorithms compensate adequately for the effect.

8.1.3 Gain Control

The SCT3811 has gain control mechanisms in the LNA and the baseband (see Figure 18) with a total control range of 60dB. The gain can be controlled using the Rx Gain Control Register, \$16; see section 7.7.1.

The LNA gain control steps can be adjusted to achieve the required accuracy using the step size control bits in the Rx Gain Control Register. The effect of the step size control varies with frequency, as shown in Table 13, Table 14 and Table 15 so for optimum accuracy the best settings should be selected to suit the particular application. (Suggested settings for optimum gain accuracy are shaded grey in the tables.)

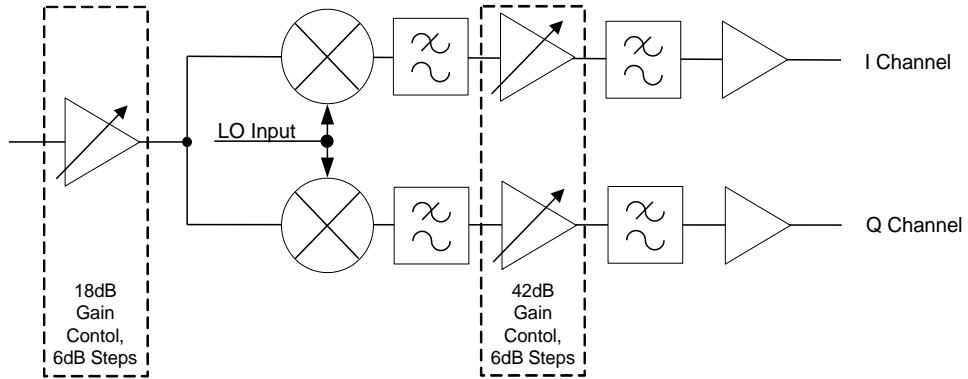


Figure 18 Gain Control

Gain Setting	Gain Cntrl Step Size (dB)	Cumulative Gain Change (dB)	Variation from Nominal (dB)
Nominal step size			
Max		0.0	
-6 dB	-6.9	-6.9	-0.9
-12 dB	-5.4	-12.3	-0.3
-18 dB	-4.2	-16.5	1.5
Nominal +0.7 dB			
Max		0.0	
-6 dB	-7.0	-7.0	-1.0
-12 dB	-6.7	-13.7	-1.7
-18 dB	-4.1	-17.8	0.2
Nominal +1.4 dB			
Max		0.0	
-6 dB	-7.0	-7.0	-1.0
-12 dB	-7.9	-14.9	-2.9
-18 dB	-4.1	-18.9	-0.9
Nominal +2.8 dB			
Max		0.0	
-6 dB	-7.0	-7.0	-1.0
-12 dB	-9.2	-16.2	-4.2
-18 dB	-4.0	-20.2	-2.2

Table 13 Typical LNA Gain Step Sizes at 100MHz, $Z_0=100\Omega$

Gain Setting	Gain Cntrl Step Size (dB)	Cumulative Gain Change (dB)	Variation from Nominal (dB)
Nominal step size			
Max		0.0	
-6 dB	-6.2	-6.2	-0.2
-12 dB	-4.5	-10.7	1.3
-18 dB	-3.7	-14.5	3.6
Nominal +0.7 dB			
Max		0.0	
-6 dB	-6.2	-6.2	-0.2
-12 dB	-5.5	-11.8	0.3
-18 dB	-3.9	-15.6	2.4
Nominal +1.4 dB			
Max		0.0	
-6 dB	-6.3	-6.3	-0.3
-12 dB	-6.6	-12.9	-0.9
-18 dB	-4.0	-16.9	1.1
Nominal +2.8 dB			
Max		0.0	
-6 dB	-6.3	-6.3	-0.3
-12 dB	-7.6	-13.9	-1.9
-18 dB	-4.4	-18.3	-0.3

Table 14 Typical LNA Gain Step Sizes at 450MHz, $Z_o=100\Omega$

Gain Setting	Gain Cntrl Step Size (dB)	Cumulative Gain Change (dB)	Variation from Nominal (dB)
Nominal step size			
Max		0.0	
-6 dB	-6.4	-6.4	-0.4
-12 dB	-5.6	-12.0	0.0
-18 dB	-5.2	-17.2	0.8
Nominal +0.7 dB			
Max	0.0	0.0	
-6 dB	-6.4	-6.4	-0.4
-12 dB	-7.1	-13.5	-1.5
-18 dB	-5.6	-19.1	-1.1
Nominal +1.4 dB			
Max		0.0	
-6 dB	-6.4	-6.4	-0.4
-12 dB	-8.6	-15.1	-3.1
-18 dB	-5.7	-20.7	-2.7
Nominal +2.8 dB			
Max		0.0	
-6 dB	-6.5	-6.5	-0.5
-12 dB	-10.3	-16.8	-4.8
-18 dB	-5.5	-22.3	-4.3

Table 15 Typical LNA Gain Step Sizes at 940MHz, $Z_0=50\Omega$

8.1.4 LNA Intermodulation Optimisation

The intermodulation (IMD) performance of the LNA can be optimised using the IM bits in the IM Control register (\$14); see section 7.5.1.

At higher frequencies, typically 400MHz and above, optimum IMD performance is with the IM bits set to maximum, i.e. 0x3F. The improved IMD performance comes with a reduction in gain of approximately 0.5dB; see Figure 19.

At minimum frequency (circa 100MHz) the IM bits should be set to minimum i.e. 0x00.

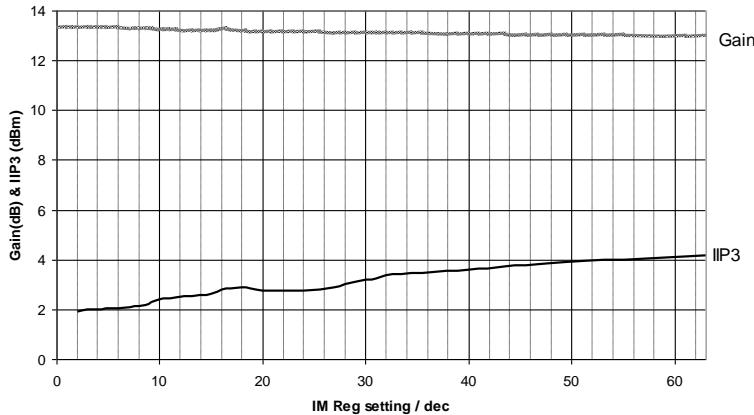


Figure 19 Variation of LNA Gain and IMD with IM Register Setting, 450MHz

8.1.5 Low Power Mode

If the low power mode is enabled, General Control Register (\$11) b4 = 1, the total current drawn in the receiver section reduces by approximately 10mA. For indications of the performance changes in low power mode; see section 8.1.1.

The IP2 performance in low power mode varies with frequency. Below 400MHz the average change between normal mode and low power mode is small. Above 400MHz low power mode causes an increasing degradation reaching 15dB (typical) at maximum operating frequency. Around 450MHz the degradation is typically 2 to 5 dB. As is usual with IP2 measurements, variations in measured values are observed at different frequency offsets, between I and Q channels and between devices, so average values must be considered.

The SCT3811 has other low power modes that are enabled using the Options Control Register (\$15). Power can be reduced by disabling the phase correction circuits (\$15 = \$03) if the excellent I/Q balance provided by the SCT3811 is not needed. Another option is to disable either I or Q path; this facility is useful for minimising power when monitoring a channel for a RF signal.

8.1.6 I/Q Filter Response

The I/Q filter has a well-defined response and an internal calibration scheme makes it very stable with temperature. The response with temperature, measured through the entire receiver, is shown in Figure 20(a). It will be observed that, apart from a small change in overall gain, the filter response does not vary. The scaling with ACR Flt bits (Rx Control Register (\$12), b4-b3) is shown in Figure 20(b).

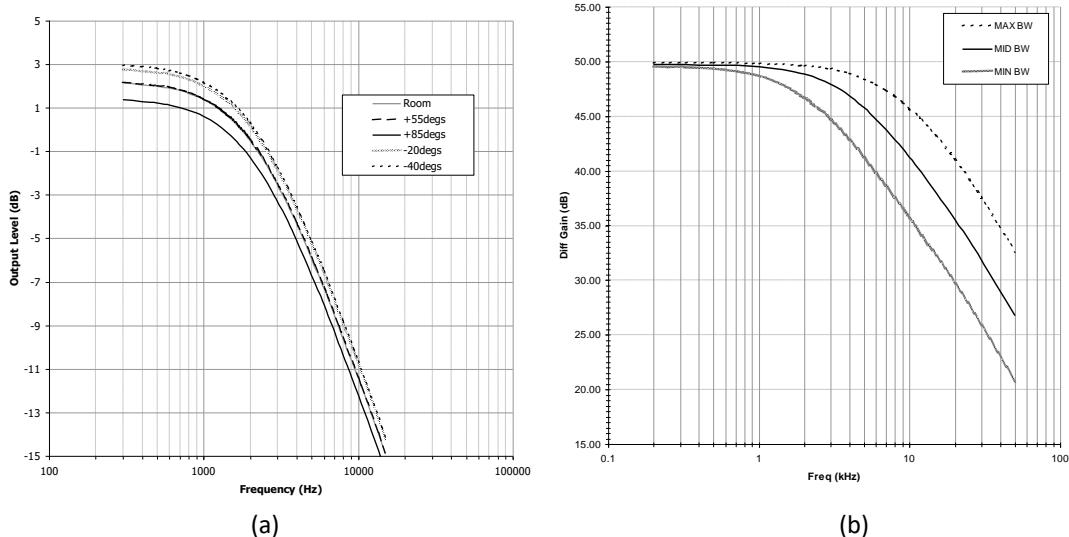


Figure 20 I/Q Filter Response

8.1.7 Baseband Intermodulation

The intermodulation (IMD) performance of the SCT3811 I/Q baseband amplifiers is designed to be good enough to ensure that the overall IMD performance of the down-converter section is dominated by the performance of the mixers. Typical in-band linearity with a very large output signal is demonstrated in Figure 21. Note the absence of IMD products. Care should be taken in the SCT3811 receiver system design to ensure that the baseband sections do not clip in the presence of intermodulation test signals because, if clipping occurs, the overall intermodulation performance of the receiver will be degraded. The SCT3811 provides two I/Q baseband filter stages which can be used to provide selectivity in order to keep IMD test signals within the receiver dynamic range.

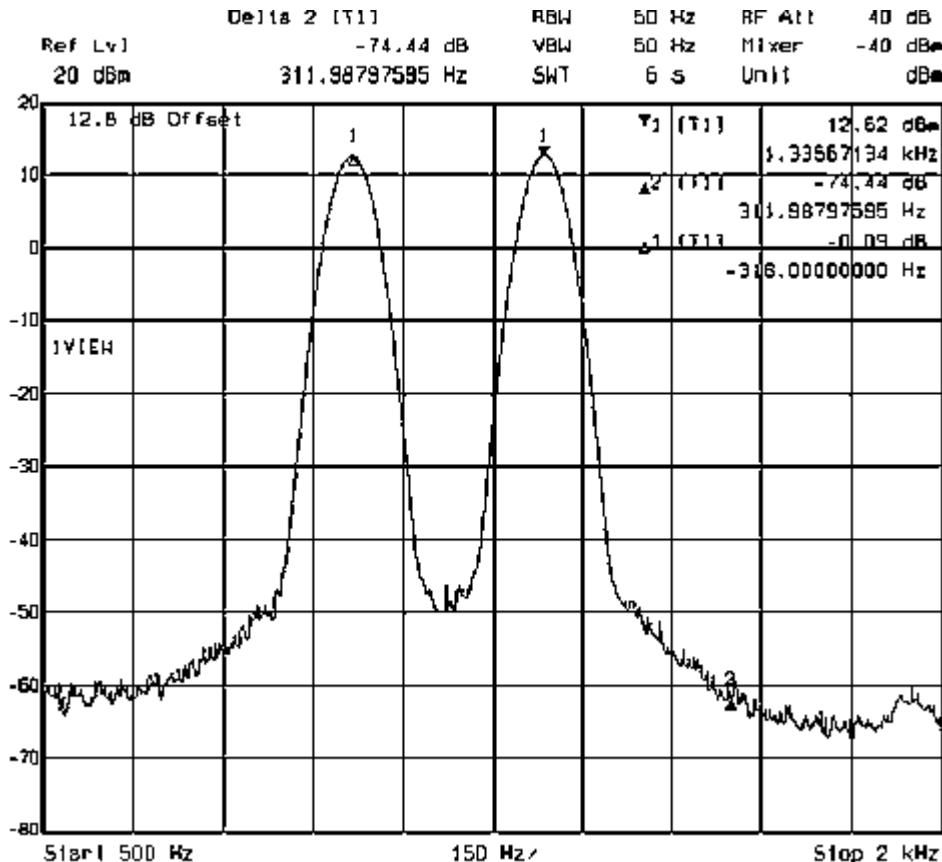


Figure 21 Baseband Intermodulation Test at circa 6Vp-p Differential Output

8.1.8 LO Pulling

The LNA gain control provided by the SCT3811 mitigates this effect; at large input signal levels the LNA gain should be set to minimum. Designs using the SCT3811 with an external LNA should consider this issue and ensure the external LNA provides sufficient gain control range.

Designs that use the SCT3811 with an external VCO / PLL, in particular a Fractional-N type, are less susceptible to such frequency pulling but should still employ suitable isolation between the SCT3811 LO input and an external VCO, for example by using a common-base buffer stage.

Following these guidelines a design can readily achieve good receiver system operation with LNA input levels of >+10dBm.

8.1.9 Power Saving Modes

The SCT3811 provides a number of options which can be used to tailor the power / performance of the device. The host can control this based on a range of parameters so, for example, power can be saved during monitoring of a channel. In the channel monitoring scenario it may be possible to save power by disabling the

I or Q channel. The values in Table 16 show the typical variation in measured values for one SCT3811 device, note operating characteristics are specified in section 9.1.3.

Mode	Phase Correction “off”	Phase Correction “on”
Enhanced mode	61mA	77mA
Normal operation	52mA	68mA
Low power mode	42mA	58mA
Low power mode and I or Q channel off	32mA	48mA

Table 16 Typical Current Consumption in Various Modes

8.1.10 Spurious Responses

An advantage of the direct conversion receiver approach is the inherently low number of spurious responses, however the circuit still has responses at harmonics and sub-harmonics. The circuit designer will need to provide suitable high-pass and low-pass filtering at the SCT3811 input (and/or between LNA and mixers) to prevent such responses.

Note: large signals at sub-harmonic frequencies will generate harmonics in the LNA output which cannot be removed after the LNA because they are on the wanted frequency of the receiver.

8.2 Operation Below 100MHz

The SCT3811 can be safely used below 100MHz, down to at least 30MHz, however performance will degrade at lower frequencies and will fall particularly rapidly below 50MHz.

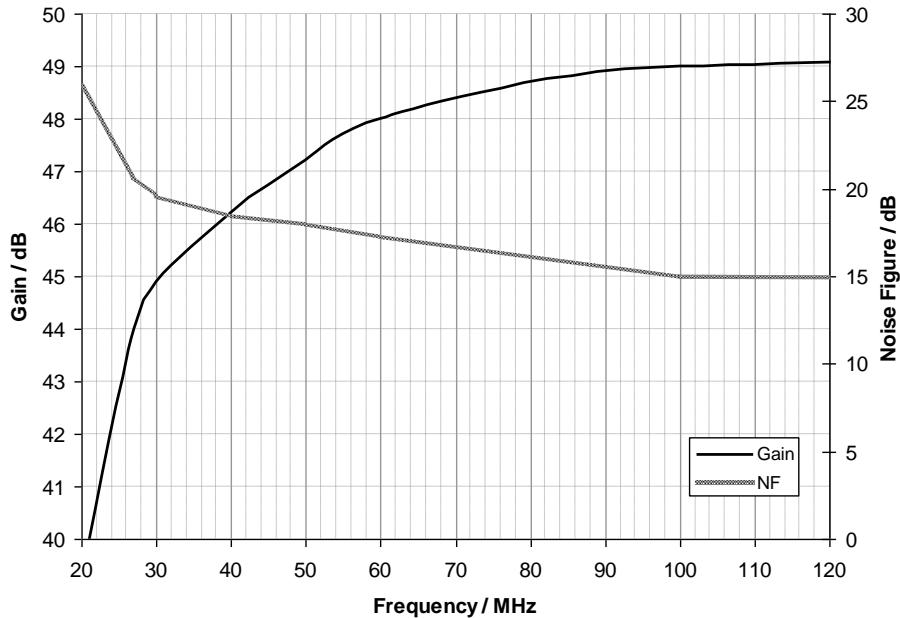


Figure 22 Typical Gain and NF Variation of Demodulator Stages at Low Frequencies

The LNA can be matched for 30MHz giving a gain of 15.5dB and noise figure of 5dB. Intermodulation is typically +3.5dBm.

For a 50MHz application, typical circuit values are shown in Table 17 using the circuit of Figure 7. Typical results using this configuration are shown in Table 18.

C1	1nF	L1	560 nH
C2	33 pF // 10nF	L2	12 pF (capacitor)
C3	1nF	L3	Not Fitted

Table 17 50MHz LNA and Inter-stage Components (100Ω mode)

Parameter	Result
Gain	63.5dB
Noise Figure	5dB
IIP3	-0.5dBm

Table 18 Summary of Results for the Complete Rx Chain at 50MHz

8.3 Operation 1GHz to 1.218GHz

The I/Q demodulator is rated up to 1.218GHz input.

The LNA continues to function above 1GHz however the noise figure degrades significantly. Typical matching values are given in Figure 23 / Table 19 and typical performance is summarised in Table 20 and Table 21.

Operation of the transmitter LO output is not recommended above 1GHz.

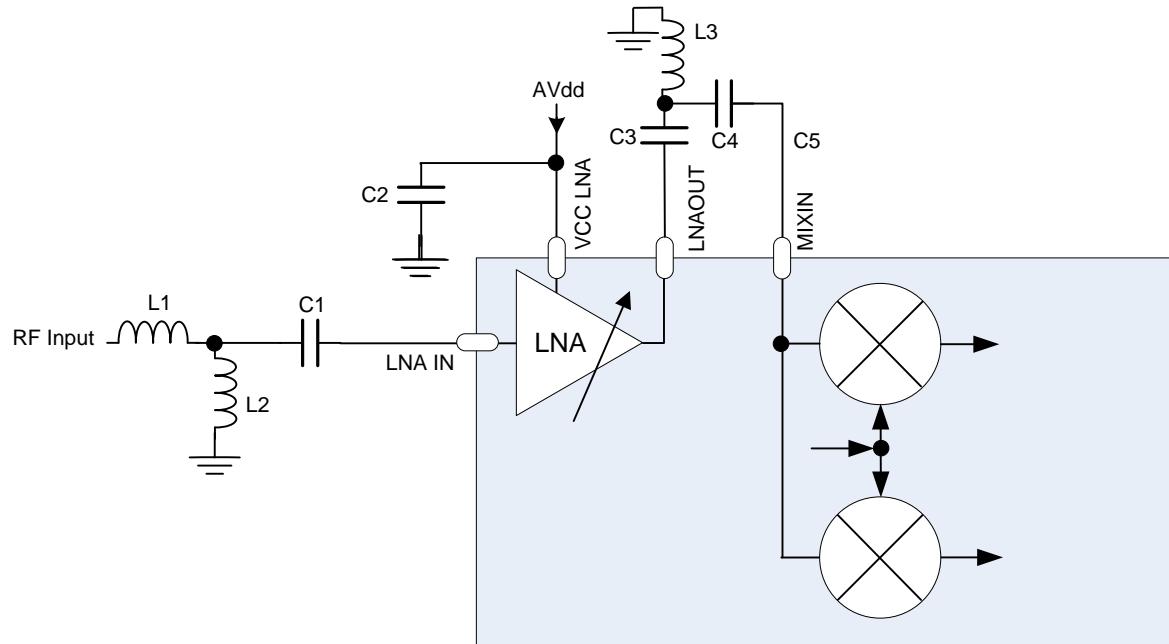


Figure 23 Typical LNA Configuration and Inter-stage Match for 1218MHz

C1	100pF	L1	3.9nH
C2	33pF //10nF	L2	2.2nH
C3	4.7pF	L3	1.8nH
C4	100pF		

Table 19 1218MHz LNA and Inter-stage Components (50Ω output mode)

Parameter	Result
Gain	11dB
Noise Figure	6dB
IIP3	-3dBm

Table 20 Summary of Results for the LNA at 1218MHz

Parameter	Result
Gain	61.5dB
Noise Figure	7.8dB
IIP3	-8dBm

Table 21 Summary of Results for the Complete Rx Chain at 1218MHz

8.4 Transmitter LO Output

The transmitter LO output is taken from the SCT3811 LO source and is independently buffered or divided to the TXLO pin. The division ratio is selected with the TXDIV0 and TXDIV1 bits in the VCO Control register (\$25, b5-b6; see section 7.9.1). The output level variation with frequency of the TXLO output is shown in Figure 24 and typical variation with temperature is shown in Figure 25 and Figure 26.

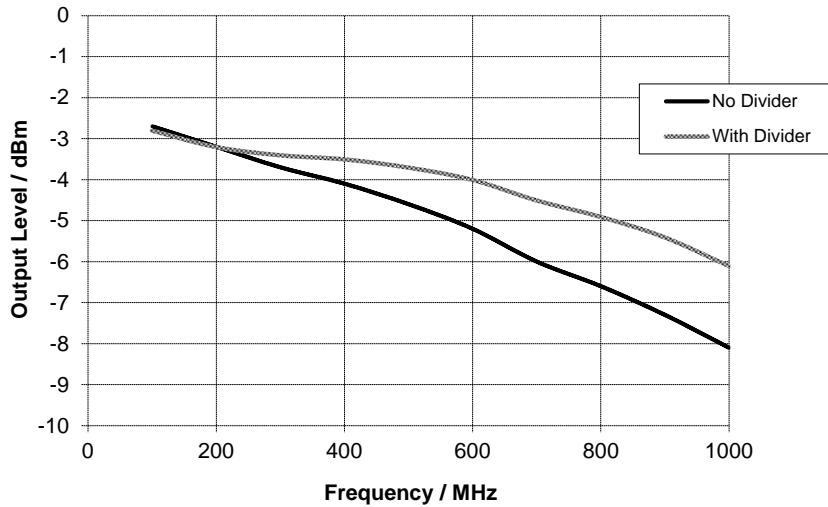


Figure 24 Tx Output Level vs. Frequency

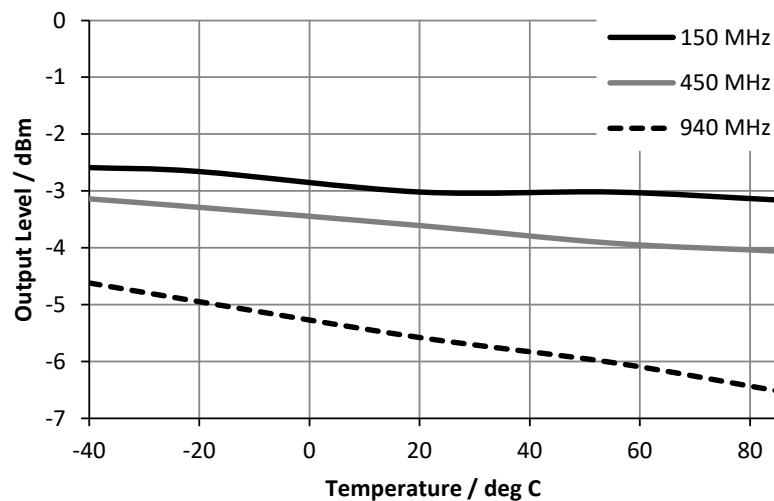


Figure 25 Typical Tx Output Level (With Divider) vs. Temperature

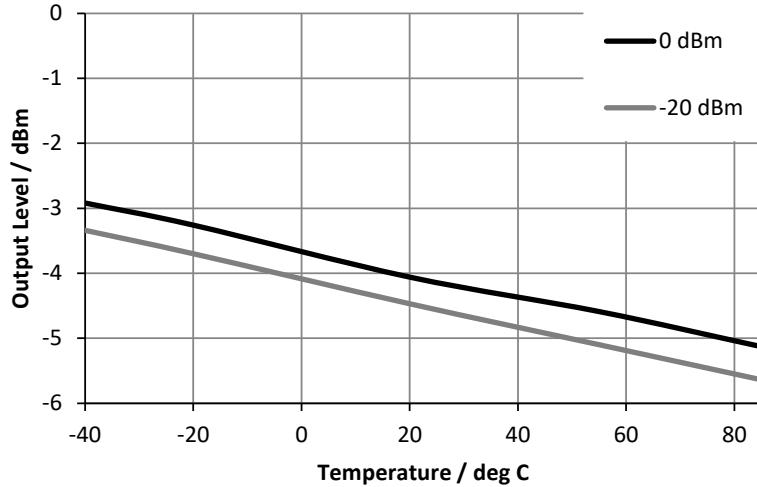


Figure 26 Typical Tx Output Level (No Divider) vs. Temperature for Varying LO Input Level

8.5 Zero IF, near-zero IF and low IF I/Q architectures

The SCT3811 provides a complete receiver signal path including LNA, RF down mixer stage and baseband amplifiers with filters to down convert the wanted RF signal to I/Q baseband while supporting high performance in a small total size. This single conversion approach provides many benefits, e.g. it requires only one LO source, which reduces circuitry and eliminates a source of many spurious responses and relative to multi-stage architectures such as dual superhet, it eliminates one or more bulky image rejection filters. The I/Q output format supports any modulation, including phase coherent constant envelope (e.g. CP-FSK) and linear (QAM) ones.

Mixing the wanted signal down to 0Hz (zero IF) by setting mixer LO and wanted RF signal frequencies to be the same provides a unique benefit, which is that it avoids placing the image of adjacent channel and other close-in interferers at the same frequency band as the wanted modulation. This is especially helpful if one considers that the adjacent channel interferer power may be far greater than the wanted signal's. The zero IF approach also minimises the bandwidth of I/Q output signals, which reduces the cost, power and complexity of ADCs used to sample them. Lastly, it enables a low pass filter on each of I and Q signal paths to provide selectivity, which simplifies design by reducing filter complexity and the required dynamic range of the ADCs. While it is true that second order mixer intermodulation products also lie at 0Hz (DC), the SCT3811 features best in class, (+79dBm) mixer IIP2 performance to attenuate such DC intermod products.

For specific radio systems one may wish to avoid mixing the wanted signal down to 0Hz. The SCT3811 readily supports this by allowing the user to select LO frequencies that do not exactly match the wanted RF signal's carrier.

Near-zero IF I/Q architectures often set the LO frequency to between half to two times the required channel bandwidth, which provides frequency separation between the wanted signal and any DC components in the output I and Q signals. Such architectures then sample (ADC convert) the near-zero I/Q IF signal pair and then use digital baseband processing to both implement a simple high pass filter that removes DC and perform a final frequency mix down to 0Hz. Operating in such a near-zero IF mode requires the SCT3811 baseband low pass filters to be scaled wider appropriately to pass the chosen IF frequency; the filter components external to the SCT3811 will need to be revised; see section 6.2.3. Sampling ADC bandwidth must also be somewhat higher performance and therefore higher power than ADCs used in the zero IF architecture. Another and perhaps more significant trade-off of near-zero IF is that the adjacent channel image generated by unavoidable I/Q gain and phase errors typically now falls on the wanted signal to create a significant interference component if the adjacent channel signal level is high.

The low IF I/Q architecture is a conceptual extension of near-zero IF; it sets the mixer LO frequency to something different than the wanted RF carrier frequency but with even more frequency separation than

near-zero IF uses. The result is that the wanted signal is mixed to an even higher frequency at the I/Q outputs. This approach can permit receiver I/Q outputs to be AC coupled to ADCs. Low IF I/Q trade-offs are of the same type as those presented by near-zero IF but they are more challenging, i.e. wider bandwidth ADCs must be used.

The SCT3811 supports all of zero IF, near-zero IF and low IF I/Q architectures, with the benefits of LNA to I/Q output integration with amplification, low pass filtering, and operating modes selected via serial host control.

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9 Performance Specification

9.1 Electrical Performance

For a definition of voltage and reference signals, see section 4.1.

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.



ESD Warning: This high performance RF integrated circuit is an ESD sensitive device which has unprotected inputs and outputs. Handling and assembly of this device should only be carried out at an ESD protected workstation.

	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS})	-0.3	+4.0	V
Voltage on any pin to AGND or DGND pins	-0.3	$V_{max} + 0.3$	V
Voltage between AV_{DD} and DV_{DD}	-0.3	+0.3	V
Voltage between AGND and DGND pins	-50	+50	mV
Current into or out of DGND, VDDIO, VCCRXIF, VCCRF, VCCLNA, VCCLO1, VCCLO2 or DVDD pins	-75	+75	mA
Current into or out of AGND (exposed metal pad)	-200	+200	mA
Current into or out of any other pin	-20	+20	mA

Note: see section 4.1 for definitions of signals.

Q4 Package	Min.	Max.	Units
Total Allowable Power Dissipation at $T_{AMB} = 25^\circ C$	-	1820	mW
... De-rating	-	18.2	$mW/^\circ C$
Storage Temperature	-55	+125	$^\circ C$
Operating Temperature	-40	+85	$^\circ C$

9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Analogue Supply (AV_{DD}) and Digital Supply (DV_{DD})		3.0	3.6	V
IO Supply (VDD_{IO})		1.6	$DV_{DD} + 0.3$	V
Operating Temperature		-40	+85	$^\circ C$
Maximum continuous input to pin LAIN	A		+3	dBM

Notes: A. For signals that are not continuous, higher input powers are permitted; power levels above +10dBm should be avoided especially when the device is operating close to the maximum rated operating temperature.

9.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$AV_{DD} = DV_{DD} = VDD_{IO} = 3.0V$ to $3.6V$; $V_{SS} = AV_{SS} = DV_{SS}$, $T_{AMB} = +25^{\circ}C$; registers in default condition except where otherwise specified or as necessary to enable the relevant sections of the device for half duplex operation.

DC parameters

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption					
Powersave Mode	1, 2	—	25	—	μA
V_{BIAS} Only	4	—	1.7	3.5	mA
Operating Currents					
Rx Only	5	—	66	80	mA
Rx Only, Low Power Mode	5a	—	56	—	mA
Rx Only, Low Power Mode and Phase Correction off	5c	—	42	—	mA
Rx Only, Low Power Mode and Phase Correction off, I or Q channel disabled	5d	—	33	—	mA
Rx Only, Enhanced Intermodulation Mode	5e	—	74	90	mA
Tx Only	5	—	22	30	mA
Stage currents					
LNA Only	5	—	9	15	mA
LNA in 50Ω Output Mode	5b	—	11	—	mA
I/Q Demodulator	5	—	41	53	mA
Baseband I/Q	5	—	13	15	mA
LO Input	5	—	5	7	mA
Current from VDD_{IO}	3	—	—	600	μA
Logic "1" Input Level		70%	—	—	VDD_{IO}
Logic '0' Input Level		—	—	30%	VDD_{IO}
Output Logic '1' Level ($I_{OH} = 0.6$ mA)		80%	—	—	VDD_{IO}
Output Logic '0' Level ($I_{OL} = -1.0$ mA)		—	—	+0.4	V
Power-up Time					
Internal Bias Supplies	6, 7	—	—	0.5	ms
All Blocks Except Internal Bias	6	—	—	10	μs

- Notes:
1. Powersave mode current applies to both the following operating cases: (a) after a General Reset command has been issued and with all analogue and digital supplies applied and also (b) with DV_{DD} applied but with all analogue supplies disconnected. For case (b), DV_{DD} current will not exceed the specified value and is independent of the state of the registers.
 2. T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.
 3. Assumes 30pF on each C-BUS interface line and an operating serial clock frequency of 5MHz.
 4. The stated current drawn here is with the bandgap reference and accompanying bias current generators enabled only (General Control Register – \$11), all other circuitry is disabled.
 5. Not including any current drawn from the device pins by external circuitry or the bias current.
Rx Only – Rx Circuitry as enabled: Rx Gain Register = 0x00, General Control Register = 0xC2, Rx Control Register = 0x10 and Intermodulation Control Register = 0x3F;
TX Only – General Control Register = 0x81, divide by 2 mode;
LNA Only – 0x82 is written to the General Control Register and 0xC0 to the Rx Control register;
I/Q Demodulator – 0x60 is written to the Rx Control register;
Baseband I/Q – 0xA0 is written to the Rx Control register;
LO Input – 0x84 is written to the General Control Register and 0x10 to the VCO Control Register;
- 5a. As note 5 except General Control Register (\$11) b4 = '1'; see sections 7.2.1 and 8.1.5.
 - 5b. As note 5 except Rx Gain Register (\$16) b3 = '1'; see section 7.7.1.
 - 5c. As note 5 except General Control Register (\$11) b4 = '1'; see section 7.2.1, Option Control Register (\$15) b0 = '1' and b1 = '1'; see section 7.6.1.
 - 5d. As note 5 except General Control Register (\$11) b4 = '1'; see section 6.2.1, Option Control Register (\$15) b3- b0 = '1011 or '0111' section 6.6.1.
 - 5e. As note 5 except Option Control Register (\$15) b8 = '1'; see section 7.6.1
 6. As measured from the rising edge of CSN.
 7. Bias is enabled by General Control Register (\$11) b7; see section 7.2.1

AC Parameters – Low Noise Amplifier Section

LNA	Notes	Min.	Typ.	Max.	Units
Gain					
100MHz	14	–	15	–	dB
450MHz	12,14	–	12.5	–	dB
940MHz	17	–	11	–	dB
Reverse Isolation (S_{12})					
100MHz	14	–	-40	–	dB
450MHz	14	–	-27	–	dB
940MHz	17	–	-19	–	dB
Gain Control Range	16	–	18	–	dB
Gain Control Step Size	16	4	6	8	dB
Noise Figure	14				
100MHz	14	–	2	–	dB
450MHz	14	–	2	–	dB
940MHz	17	–	3.5	–	dB
Third Order Intercept Point (input)					
100MHz	14	–	8	–	dBm
450MHz	11,14	–	8	–	dBm
940MHz	11,14,17	–	0.5	–	dBm
1dB Gain Compression Point (input)					
100MHz	14	–	-11	–	dBm
450MHz	14	–	-12	–	dBm
940MHz	17	–	-10	–	dBm
Input Impedance	10	–	–	–	Ω
Output Impedance	10, 13	–	100R // 1.2pF	–	Ω
Operating Frequency Range	15	100	–	1000	MHz
LO Leakage at LNA Input		–	<-90	–	dBm

- Notes:
- 10. For further details see section 5.2.1
 - 11. Intermodulation optimised using Intermodulation Control Register, for further details see section 6.5.
 - 12. The gain is approximately 2dB higher if the LNA Z_0 (Rx Gain Register b3) is set to '1'.
 - 13. The impedance is approximately 50Ω if the LNA Z_0 (Rx Gain Register b3) is set to '1'.
 - 14. Measured at maximum gain with the LNA Z_0 (Rx Gain Register b3) set to '0'.
 - 15. For extended operation down to 50MHz see section 8.2.
 - 16. See section 8.1.3 for further details
 - 17. LNA $Z_0 = 50\Omega$ (Rx Gain Register b3 set to '1')

AC Parameters – Direct Conversion Receiver Sections (normal mixer intermod mode)

I/Q Demodulator (combined performance of receiver sections, excluding LNA)	Notes	Min.	Typ.	Max.	Units
Gain					
450MHz		–	49	–	dB(V/V)
940MHz		–	49	–	dB(V/V)
1218MHz	24b	–	48	–	dB(V/V)
Noise Figure					
450MHz		–	14.5	–	dB
940MHz		–	16	–	dB
1218MHz	24b	–	17	–	dB
Third Order Intercept Point (Input)					
450MHz		–	11	–	dBm
940MHz		–	9.5	–	dBm
1218MHz	24b	–	7	–	dBm
Second Order Intercept Point (Input)					
100MHz to 600MHz	25	–	79	–	dBm
600MHz to 940MHz	25a	–	73	–	dBm
1dB Compression Point (Input)	24, 24a	–	0	–	dBm
Image Rejection (I/Q Gain/Phase Matching)					
LO Phase Correction On		30	40	–	dB
LO Phase Correction Off	24	25	–	–	dB
I/Q Amplitude Balance					
LO Phase Correction On		–	± 0.03	± 0.2	dB
LO Phase Correction Off	24	–	± 0.1	–	dB
I/Q Phase Balance					
LO Phase Correction On		–	± 0.5	± 2.0	deg.
LO Phase Correction Off	24	–	± 1	± 3	deg.
I/Q DC Offset Correction Steps	22	17	25	33	mV
I/Q DC Offset at Maximum Attenuation	20a	–	±15	±55	mV
I/Q Output Bandwidth	23	–	–	1.6	MHz
LO Divider Ratios (selectable)		–	2, 4 or 6	–	
I/Q Differential Output Voltage Swing	20	–	–	4.0	Vp-p
Blocking	21	93	96	–	dB

AC Parameters – Direct Conversion Receiver Sections (register \$15, b7 set to '1' (enhanced mixer intermodulation mode))

I/Q Demodulator (combined performance of receiver sections, excluding LNA)	Notes	Min.	Typ.	Max.	Units
Gain					
450MHz		–	49	52	dB(V/V)
1000MHz		–	49	52	dB(V/V)
1218MHz	24b	–	48	–	dB(V/V)
Noise Figure					

100MHz	24c	—	14.5	17	dB
450MHz		—	15	17	dB
870MHz		—	16	—	dB
1000MHz		—	16.5	—	dB
1218MHz	24b	—	17	—	dB
Third Order Intercept Point (Input)					
100MHz		—	19	—	dBm
450MHz		—	15	—	dBm
870MHz		—	12	—	dBm
1000MHz		—	11.5	—	dBm
1218MHz	24b	—	10.5	—	dB
Second Order Intercept Point (Input)					
100MHz to 600MHz	25	—	79	—	dBm
600MHz to 1000MHz	25a	—	73	—	dBm
1dB Compression Point (Input)	24, 24a	—	0	—	dBm
Image Rejection (I/Q Gain/Phase Matching)					
LO Phase Correction On		30	40	—	dB
LO Phase Correction Off	24	25	—	—	dB
I/Q Amplitude Balance					
LO Phase Correction On		—	± 0.03	± 0.2	dB
LO Phase Correction Off	24	—	± 0.1	—	dB
I/Q Phase Balance					
LO Phase Correction On		—	± 0.5	± 2.0	deg.
LO Phase Correction Off	24	—	± 1	± 3	deg.
I/Q DC Offset Correction Steps	22	17	25	33	mV
I/Q DC Offset at Maximum Attenuation	20a	—	±15	±55	mV
I/Q Output Bandwidth	23	—	—	1.6	MHz
LO Divider Ratios (selectable)		—	2, 4 or 6	—	
LO Divider Noise Floor		—	-152	—	dBc/Hz
I/Q Differential Output Voltage Swing	20	—	—	4.0	Vp-p
Blocking	21	93	96	—	dB

- Notes:
- 20. This is the maximum swing to guarantee meeting the third order distortion characteristics under the specified conditions and is not the maximum limiting value. For clarity, this means that the device has the capability to produce +/-1V on each of the differential outputs. The outputs are capable of driving a load resistance across the differential outputs of 1kΩ.
 - 20a V_{offset} minimised using V_{corr} at minimum attenuation then with maximum baseband attenuation set V_{offset} is measured, mixer RF input terminated in 50 Ohms; see also section 8.1.2.
 - 21. Test method based on EN 300 166; including operation of selectable dividers.
 - 22. Register \$12, b2 = '0'.
 - 23. This is the maximum bandwidth of the I and Q output signals with no external capacitors fitted and with the filter calibration circuit disabled. The bandwidth of the I/Q output can be adjusted to suit the application by use of the I/Q filters. This bandwidth can be set by using external capacitors (see sections 6.2.2 and 6.2.3). Note that a 25kHz bandwidth on the I/Q filters supports a modulation signal bandwidth of 50kHz.
 - 24. Measured at 450MHz.

- 24a Measured with baseband attenuations settings of 30dB and above, with less attenuation measurement is limited by the output compression point.
- 24b Measurement configuration as Figure 9 / Table 9.
- 24c Maximum noise figure specification based on correlation with 450MHz value.
25. Average value of IIP2 measurements at $\pm 1\text{MHz}$, $\pm 5\text{MHz}$ and $\pm 10\text{MHz}$ offsets using differential signals on I and Q channels, measurements every 100MHz over the range 100MHz to 600MHz.
- 25a Average value of IIP2 measurements at $\pm 1\text{MHz}$, $\pm 5\text{MHz}$ and $\pm 10\text{MHz}$ offsets using differential signals on I and Q channels, measurements at 600MHz and every 50MHz over the range 700MHz to 1000MHz.

Rx Direct Conversion Mixers	Notes	Min.	Typ.	Max.	Units
Gain					
450MHz	26	—	15	—	dB(V/V)
940MHz		—	15	—	dB(V/V)
Noise Figure					
450MHz	27	—	13.5	—	dB
Third Order Intercept Point (Input)					
450MHz	27, 24	—	11	—	dBm
Input Frequency Range	15	100	—	1218	MHz
LO Frequency Range before internal division	15	200	—	2436	MHz
Input Impedance	29	—	—	—	Ω
Zero-IF Signal Bandwidth					
at mixer output with SCT3811 baseband		1	—	—	MHz
at mixer output with external baseband	29a	—	10	—	MHz
LO Leakage at Input	28	—	-80	—	dBm

- Notes:
- 26. Measured from matched input source.
 - 27. This is an indicative specification only as the parameter cannot be independently measured other than as part of the complete Rx Path.
 - 28. Measured at input to mixers with 100 Ohm termination.
 - 29. For further details see section 5.2
 - 29a. A 10MHz zero-IF signal bandwidth on the mixer I/Q output (pins IFLT1N, IFLT1P and QFLT1N, QFLT1P) supports a modulation signal bandwidth of 20MHz. See section 8.1.7.

Zero IF Amplifiers and Filters	Notes	Min.	Typ.	Max.	Units
Gain	26, 30	—	34	—	dB(V/V)
Noise Figure	27	—	—	10	dB
Third Order Intercept Point (Output)	27,30a	—	>50	—	dBm
Output Impedance		—	20	—	Ω
1dB Compression Point	27	-30	—	—	dBm
VGA Control Range	31	—	42	—	dB
VGA Step Size		4	6	8	dB
I/Q Output Bandwidth		—	—	1.6	MHz
I/Q Differential Output Voltage Swing	20	—	—	4.0	Vp-p
I/Q Output Common Mode		—	AV _{DD} /2	—	V
Post Mixer Filter					
Bandwidth (-3dB)	32, 37	—	88	—	kHz
Adjacent Channel Rejection					
Bandwidth (-3dB)	32	—	2	—	kHz
Scaling Factors		—	1 : 2 : 4	—	
Bandwidth Variation	33	—	—	5	%
Third Order Intermodulation					
Post Mixer Filter	27, 35	—	90	—	dBc
1 st Amplifier	27, 35	85	—	—	dBc
2 nd Amplifier	27, 36	85	—	—	dBc

- Notes:
- 30. The first amplifier stage has nominal gain of 15dB, the second stage has nominal gain of 22dB.
 - 30a. In-band intermodulation calculated from output signal assuming 50Ω impedance; see also section 8.1.7.
 - 31. Eight VGA steps.
 - 32. Assumes the recommended external capacitors are used (see section 5.2.2).
 - 33. Assuming external resistors with 1% tolerance and external capacitors with 5% tolerance.
 - 34. Tested at maximum gain setting of VGA.
 - 35. Assuming two 200mVp-p tones at 25kHz and 50kHz.
 - 36. Assuming two 60mVp-p tones at 25kHz and 50kHz.
 - 37. The post mixer filter bandwidth will vary with VGA setting. This may typically be 30%, with the bandwidth reducing at lower gain settings.

AC Parameters – Tx Output

Tx Divider	Notes	Min.	Typ.	Max.	Units
Input Frequency Range		100	–	2000	MHz
Output Frequency Range		100	–	1000	MHz
Divider Ratio		–	1, 2, 4 or 6	–	
Output Level	38	-5.5	-3.5	-1.5	dBm
Noise Floor	39	–	-146	–	dBc/Hz

Notes: 38. 448MHz output with LO divider ratio = 2; see section 8.4 for further information.
 39. Noise at 5MHz offset, measured at 500MHz with 1GHz Local Oscillator.

AC Parameters – LO input

	Notes	Min.	Typ.	Max.	Unit
Input Level	40	-15	-10	-5	dBm
Frequency Range		100	–	2436	MHz

Notes: 40. Single-ended input as described in section 5.3.1.

AC Parameters – C-BUS

C-BUS Timings (See Figure 27)		Notes	Min.	Typ.	Max.	Units
t _{CSE}	CSN-enable to clock-high time		100	–	–	ns
t _{CSH}	Last clock-high to CSN-high time		100	–	–	ns
t _{LOZ}	Clock-low to reply output enable time		0.0	–	–	ns
t _{HIZ}	CSN-high to reply output 3-state time		–	–	1.0	μs
t _{CSOFF}	CSN-high time between transactions		1.0	–	–	μs
t _{NXT}	Inter-byte time		200	–	–	ns
t _{CK}	Clock-cycle time		200	–	–	ns
t _{CH}	Serial clock-high time		100	–	–	ns
t _{CL}	Serial clock-low time		100	–	–	ns
t _{CDS}	Command data set-up time		75.0	–	–	ns
t _{CDH}	Command data hold time		25.0	–	–	ns
t _{RDS}	Reply data set-up time		50.0	–	–	ns
t _{RDH}	Reply data hold time		0.0	–	–	ns

Maximum 30pF load on each C-BUS interface line.

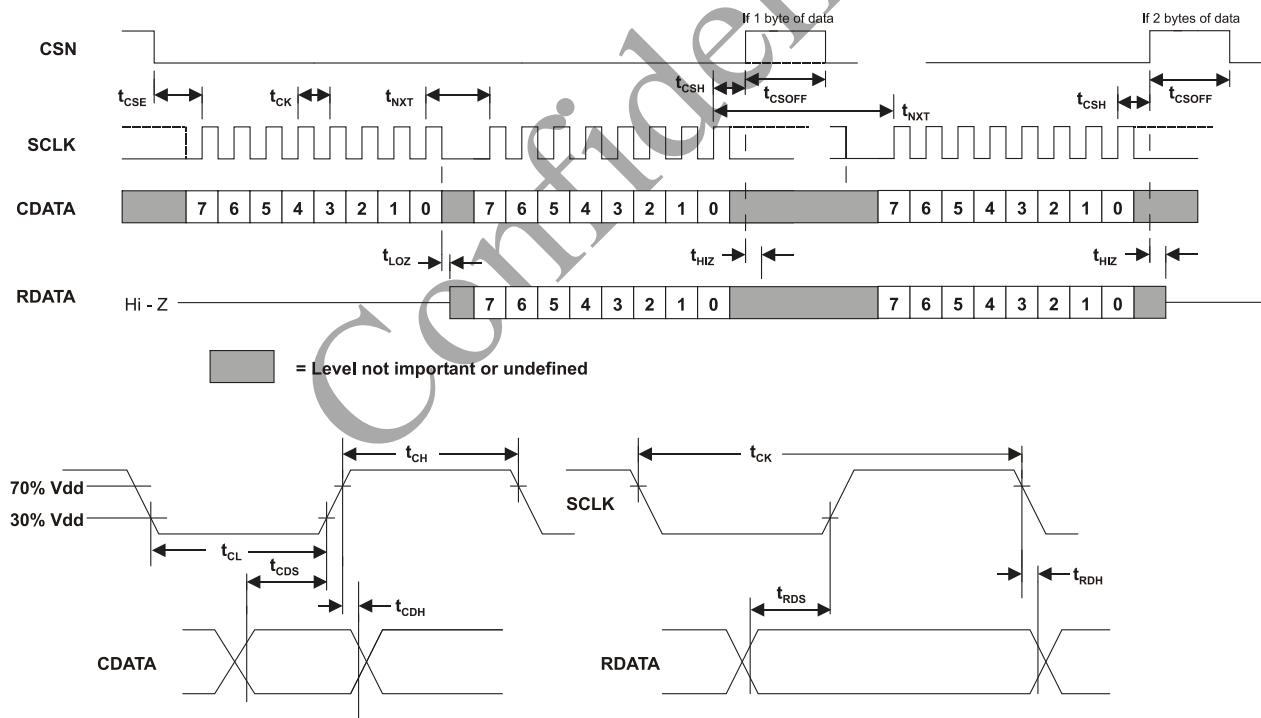
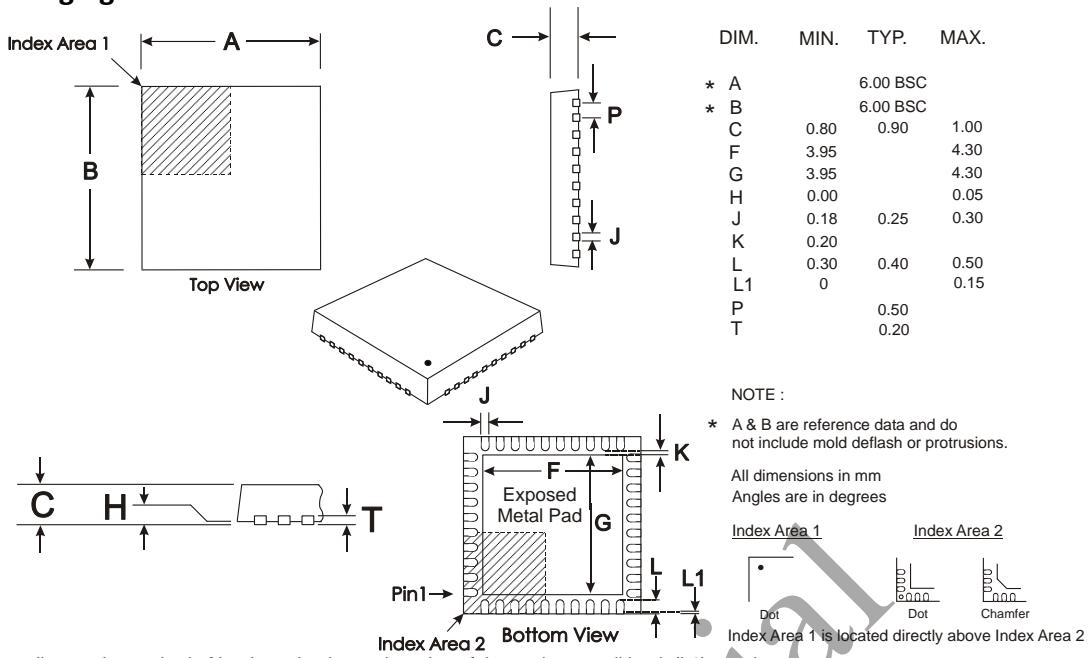


Figure 27 C-BUS Timing

9.2 Packaging



Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.

L minus L1 to be equal to, or greater than 0.3mm

The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Notes:

1. In this device, the underside of the Q4 package should be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.

Figure 28 Q4 Mechanical Outline

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Handling precautions: This product includes input protection, however precautions should be taken to prevent device damage from electro-static discharge. Sicomm does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. Sicomm reserves the right at any time without notice to change the said circuitry and this product specification.