Hangzhou Xinsheng Intelligent Technology Co., Ltd.

XS2002 Audio DSP Chip Specification

Non-public document

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Use this document

The purpose of this document is to provide general information about the specifications and hardware of the XS2002 voice trigger and offline recognition chip. Although every effort has been made to ensure that this document is up-to-date and accurate, but there may be more information that has been updated since this guide produced. In this case, please contact our sales representative for more information that will help the development process.

Contents

Abbreviations

SIMD	Single Instruction Multiple Data
MIC	microphone
PDM	Pulse Density Modulation
TDM	Time Division Multiplexing
VT	Voice Trigger
VAD	Voice Activity Detection
KWS	KeyWord Spotting
AEC	Automatic Echo Cancellation
RISC	Reduced Instruction Set Computer
MAC	Multiply Accumulate
AI	Artificial Intelligence
ADC	Analog-to-Digital Converter
AMIC	Analog MIC
DMIC	Digital MIC
LDO	low dropout regulator
I2S	Inter-IC Sound or Integrated Interchip Sound
PWM	Pulse Width Modulation
AGC	Automatic Gain Control
BF	Beam Formming
Dereverberation	Dereverberation
NS	Noise Suppression
SR	Speaker Recognition
AP	application processor

1 Introduction

1.1 Device overview

XS2002 is a new kind of audio DSP with AI algorithm processing capabilities, with large SRAM and powerful SIMD engine, it is suitable for voice enhancement, beamforming, AEC or voice triggering applications, which takes into account the needs of ultra-low power triggering and high-performance computing at the same time. On the one hand, the low-power chip technology and AI algorithm support Always-on trigger mode, the trigger current is less than 1mA; on the other hand, there is a programmable low-power neural network calculation engine and a CPU that supports SIMD, as well as rich The memory resources, the highest frequency is 200MHz. Supports up to 4 analog MIC inputs or 4 digital MIC PDM inputs at the same time. It supports TDM input and output.

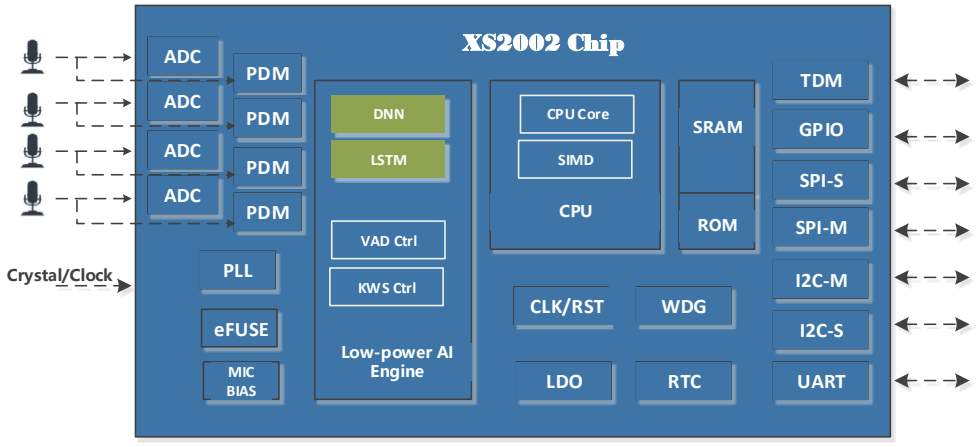


Fig.1 Block Diagram

1.2 Part number

Part number and package.

Tab.1 Chip Package

Part number	Package
XS2002	QFN32 (4mm x 4mm)

2 Features

- 32bit RISC-V CPU, the highest frequency is 200MHz. Support SIMD instructions, parallel MAC calculations, and single-precision floating-point operations
- Large memory space， SRAM of 576kB
- Support DSP library, and support AI processing functions
- Low-power Voice ADC, support four analog MIC at the same time, with 60uA power consumption for each ADC channels, capable of voice sampling at 32kHz, with SNR of 72dB, and internal PGA support -6dB~30dB gain adjustment range
- Support PDM decoding, support four digital MIC at the same time, DMIC clock frequency range 512KHz ~ 3.072MHz
- Low-power technology, There is an LDO inside, support Dynamic voltage and frequency scaling
- Support 32.768KHz, or 8MHz, 12MHz, 19.2MHz, 24MHz etc crystal
- Supports multi-channel TDM (I2S) input and output
- Support SPI-slave/I2C-slave boot mode, support SPI Master boot (IoT application)
- Support SPI-slave/SPI-master/I2C-slave/I2C-master/UART/PWM/GPIO and other peripheral interfaces
- Package: QFN32
- Size: 4mm x 4mm x 0.75mm
- Temperature: -40 ~ 85 ℃

3 Pin Mapping

3.1 QFN Pin Maping

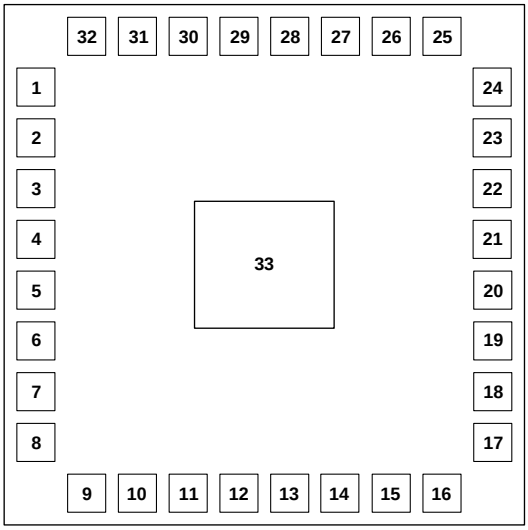


Fig.2 XS2002 QFN32 Pin Map（TOP View）

3.2 Pin Definition

The following table shows the pin names and function definitions of XS2002. See Tab.3. for pin functions.

Tab.2 XS2002 Pin List

No.	Name	Direction	Function
1	XGPIO1/IRQ/MODE_I2C	I/O	mode selection/SPK_PWM/SPK_I2S_DAT/ DMIC_CLK/mic bias/IRQ/TXD, internal pull-down
2	XGPIO2/DMICCLK1/DMICDIN1	I/O	SPIM_CS0/ SPIM_CS1/I2CM_SDA/I2SM_MCLK/ DMIC_CLK/RXD/SPK_I2S_SCLK/mic bias
3	XGPIO3/MIC_BIAS1	I/O	SPIM_DIN/I2CM_SCL/TXD/RXD/SPK_PWM/ SPK_I2S_DAT/mic bias
4	XO	OUT	the output of crystal driver circuit
5	XI	IN	clock input
6	XGPIO4/DMICDIN2	I/O	I2CM_SDA/DMIC_CLK/RXD
7	RSTN	IN	Chip Reset, low active internal pull-up
8	XGPIO5/MIC_EBIAS	I/O	SPIM_DO/I2CM_SDA/RXD/SPK_I2S_LRCK/ MIC_EBIAS
9	VDDIO	N/A	IO power
10	VREG_IN	IN	CORE power input for LDO
11	VREG_OUT	OUT	CORE power output
12	XGPIO6/DMICDIN3	I/O	I2CM_SCL/TXD
13	XGPIO7	IN	OSC mode selection, internal pull-up
14	I2S_LRCK	I/O	I2SM_LRCK/I2SS_LRCK
15	I2S_DOUT	I/O	I2SM_DOUT/I2SS_DOUT
16	I2S_SCLK	I/O	I2SM_SCLK/I2SS_SCLK
17	I2S_DIN	I/O	I2SM_DIN/I2SS_DIN
18	XGPIO8	IN	OSC mode selection, internal pull-up
19	TEST_EN	IN	chip test enable, internal pull-down
20	SPI_CSB	I/O	SPIS_CSB/SPIM_CS0/I2CM_SCL/TXD
21	SPI_DOUT	I/O	SPIS_DOUT/SPIM_DOUT/I2CM_SDA/RXD
22	SPI_DIN	I/O	SPIS_DIN/I2CS_SDA/SPIM_DIN
23	SPI_CLK	I/O	SPIS_CLK/I2CS_SCL/SPIM_CLK
24	XGPIO9/MODE_MST	I/O	mode selection/SPK_PWM/SPK_I2S_DAT/IRQ/ I2SM_MCLK/DMIC_CLK/TXD, internal pull-down
25	XGPIO10/DMICDIN0	I/O	SPIM_CS1/SPIM_DOUT/mic bias internal pull-down
26	XGPIO0/DMICCLK0/DMICDIN1/MIC_BIAS0	I/O	SPIM_CLK/I2CM_SCL/I2SM_MCLK/DMIC_CLK/ TXD/SPK_I2S_MCLK/mic bias
27	AMIC3P/DIN3	IN	MIC input 3

28	VDDIO	N/A	IO power
29	VREF	OUT	reference voltage output for ADC
30	AMIC2P/DIN2	IN	MIC input 2
31	AMIC1P/DIN1	IN	MIC input 1
32	AMIC0P/DIN0	IN	MIC input 0
33	VSS	N/A	ground

3.3 Pin Function

Tab.3 XS2002 Function List

No.	Interface	Signal	Dir	Function
1	SPI slave	SPIS_CSB	IN	Chip select signal of SPI slave interface
2		SPIS_CLK	IN	Clock signal of SPI slave interface
3		SPIS_DIN	IN	Data input of SPI slave interface
4		SPIS_DOUT	OUT	Data output of SPI slave interface
5	I2C slave	I2CS_SCL	IN	Clock signal of I2C slave interface
6		I2CS_SDA	I/O	Data signal of I2C slave interface
7	SPI master	SPIM_CS0	OUT	Chip select signal CS0 of SPI master interface
8		SPIM_CS1	OUT	Chip select signal CS1 of SPI master interface
9		SPIM_CLK	OUT	Clock signal of SPI master interface
10		SPIM_DIN	IN	Data input of SPI master interface
11		SPIM_DOUT	OUT	Data output of SPI master interface
12	I2C master	I2CM_SCL	I/O	Clock signal of I2C master interface
13		I2CM_SDA	I/O	Data signal of I2C master interface
14	I2S slave	I2SS_SCLK	IN	Sclk input of I2S slave interface
15		I2SS_LRCK	IN	Lrck input of I2S slave interface
16		I2SS_DIN	IN	Data input of I2S slave interface
17		I2SS_DOUT	OUT	Data output of I2S slave interface
18	I2S master	I2SM_MCLK	OUT	Mclk output of I2S master interface
19		I2SM_SCLK	OUT	Sclk output of I2S master interface
20		I2SM_LRCK	OUT	Lrck output of I2S master interface
21		I2SM_DIN	IN	Data input of I2S master interface
22		I2SM_DOUT	OUT	Data output of I2S master interface
23	Analog MIC	AMIC0P	IN	Connect the output of an analog microphone
24		AMIC1P	IN	Connect the output of an analog microphone
25		AMIC2P	IN	Connect the output of an analog microphone
26		AMIC3P	IN	Connect the output of an analog microphone
27	Digital MIC	DMIC_CLK	OUT	Clock signal output to digital microphone
28		DIN0	IN	Connect the output of a digital microphone
29		DIN1	IN	Connect the output of a digital microphone
30		DIN2	IN	Connect the output of a digital microphone

31		DIN3	IN	Connect the output of a digital microphone
32	Speak Out I2S	SPK_I2S_MCLK	OUT	Speak Out I2S interface mclk
33		SPK_I2S_SCLK	OUT	Speak Out I2S interface sclk
34		SPK_I2S_LRCK	OUT	Lrck of Speak Out I2S interface
35		SPK_I2S_DAT	OUT	Speak Out I2S interface data output
36	Speak Out PWM	SPK_PWM	OUT	PWM modulation voice output
37	UART	TXD	OUT	UART send data
38		RXD	IN	UART receive data
39	MIC EBIAS	MIC_EBIAS	IN	Turn on the indicator input of the analog microphone
40	mic bias	mic_bias	OUT	Control the bias voltage of the analog microphone
41	IRQ	IRQ	OUT	IRQ interrupt output

4 Description

4.1 MIC Interface

The analog MIC and the digital MIC share 4 dedicated microphone data pins, and the clock of the digital MIC is provided from the function multiplexing pin.

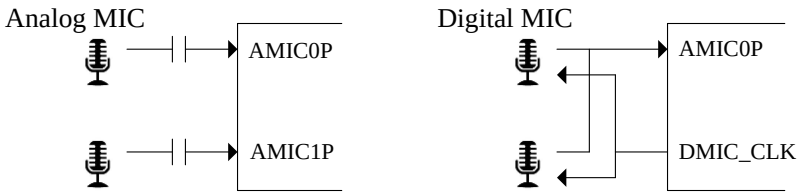


Fig.3 MIC Connect

4.2 SPI-slave Interface

The SPI-slave interface is used to download firmware to XS2002, and can also be used as a status polling or debugging interface.

Features:

- SPI clock frequency up to 24MHz
- Support SPI mode 0
- Support single frame transmission or burst transmission

4.3 I2C-slave Interface

The I2C-slave interface is used to download firmware to XS2002, and can also be used as a status polling or debugging interface.

Features:

- Clock frequency up to 1MHz

4.4 SPI-master Interface

SPI-master interface supports connecting external SPI NOR FLASH, XS2002 support boot by oneself.

Features:

- SPI clock frequency up to 24MHz
- SPI clock frequency can be configured
- Configurable frame length 4-32bits
- Support Motorola SPI/TI SPI/NSC SPI protocol
- Support SPI mode 0-3
- 32x4 Tx/Rx FIFO
- Configurable interrupt

4.5 I2C-master Interface

The I2C-master interface supports connection with external I2C devices.

Features:

- Maximum speed 400Kbps
- Configurable clock frequency
- Configurable ACK bit
- Configurable interrupt

4.6 TDM/I2S Interface

The TDM/I2S interface is used to receive I2S data input, and it can also output audio data from the on-chip RAM.

Features:

- Support external input I2S clock (I2S slave) or internally generated I2S clock (I2S master)
- Support TDM multi-channel audio data reading and writing, up to 4 channels of reading and 2 channels of writing

- The interface protocol of TDM/I2S is configurable and supports multiple modes such as standard I2S mode, left-justified mode, etc.
- Configurable frame length
- Configurable number of channels
- Support TDM bypass mode

4.7 Speak Out Interface

The Speak Out interface of XS2002 supports two modes: I2S output and PWM audio output.

I2S output Features:

- SCLK frequency is 64fs
- Sampling frequency supports 48KHz/96KHz/192KHz, etc.

PWM audio output Features:

- 256 level adjustment
- Modulation frequency support 96KHz/192KHz

4.8 PWM Interface

Common IO pins can be configured as PWM modulation output pins for dimming function.

4.9 GPIO Interface

The GPIO interface is used to control peripherals or transmit status information to the AP.

4.10 MIC Ebias Interface

The MIC Ebias interface is used to receive the AP's analog microphone work flag.

4.11 MIC bias Interface

Mic bias is used to turn on the bias voltage of the analog microphone

4.12 ADC

XS2002 integrates 4 ADCs inside, which can connect 4 analog microphones. Each ADC can be individually enabled and controlled to adapt to different application requirements.

4.13 PDM

PDM supports up to 4 channels of mono digital microphones, or 2 pairs of dual channel stereo digital microphones.

4.14 Power

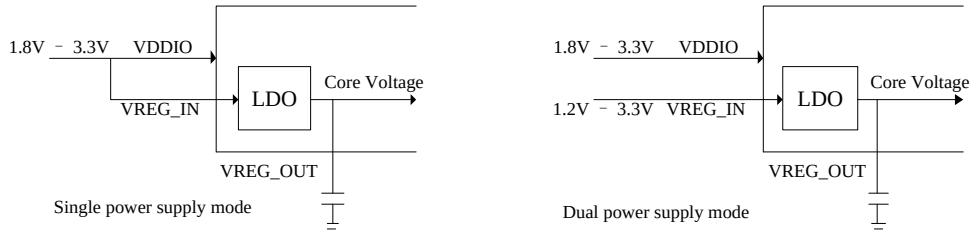


Fig.4 Single power supply and Dual power supply

- There is an internal LDO to supply power for the internal digital logic (VDDIO≥VREG_IN).
- Users can choose single power supply mode or dual power supply mode. The single-supply mode is simple, but because the current of the LDO flows from VDDIO (VDDIO higher than the VREG_IN voltage in the dual-supply mode), the overall power consumption is higher than that in the dual-supply mode.

4.15 Clock

Support external passive crystal oscillator or active crystal oscillator. The internal PLL can support different input clock frequencies.

- 32.768KHz
- Under other input frequencies, some functions of I2S master and PDM may not be supported. Please contact Xinsheng for details

We provide API to control the PLL clock according to different input clocks.

5 Work Mode

5.1 Low-power mode and Working mode

XS2002 could work in low power mode with 110uA power consumption, or other low power mode, depends on whether reboot or re-configure;

XS2002 could change to working mode from low power mode, from SPI interface or GPIO conditions, and in working mode, its power consumption depends on what kinds of algorithm to run, some typical power consumption is as below:

VAD	Without noise suppression	1mA
Noise suppression	Traditional algorithm	2.5mA
Noise suppression	AI algorithm	12mA
AEC	Simple algorithm	7mA
AEC	Enhanced algorithm	12mA

5.3 Crystal Oscillator Configuration

XS2002 supports external passive crystal oscillator or active crystal oscillator, which can be configured through two special pins XGPIO7 and XGPIO8.

Tab.4 crystal oscillator configuration

PIN	Config	Description
XGPIO7	External pull up or NC	Select 32.768KHz frequency crystal oscillator
XGPIO8	External pull up or NC	External passive crystal oscillator
	External pull down	External active crystal oscillator

5.4 System Boot

XS2002 supports three boot methods: SPI slave boot/I2C slave boot/SPI master boot. When using the SPI slave boot method, the AP must first download the firmware through the SPI slave interface of XS2002, and then start XS2002 to run; when using the I2C slave boot method, the AP

must first download the firmware through the I2C slave interface of XS2002, and then start XS2002 Run; when using SPI master boot mode, XS2002 will start automatically after power-on or reset, and then run the firmware in SPI NOR Flash.

XS2002 configures the boot mode through two Strap Pins.

Tab.5 boot mode configuration

Strap Pin	PIN	Config	Description
STRAP0	XGPIO1/IRQ/MODE_I2C	External pull down or NC	SPI slave boot
		External pull up	I2C slave boot
STRAP1	XGPIO9/MODE_MST	External pull down or NC	SPI slave/I2C slave boot
		External pull up	SPI master boot

The configuration priority of XGPIO9/MODE_MST is higher than XGPIO1/IRQ/MODE_I2C.

The startup process is as follows.

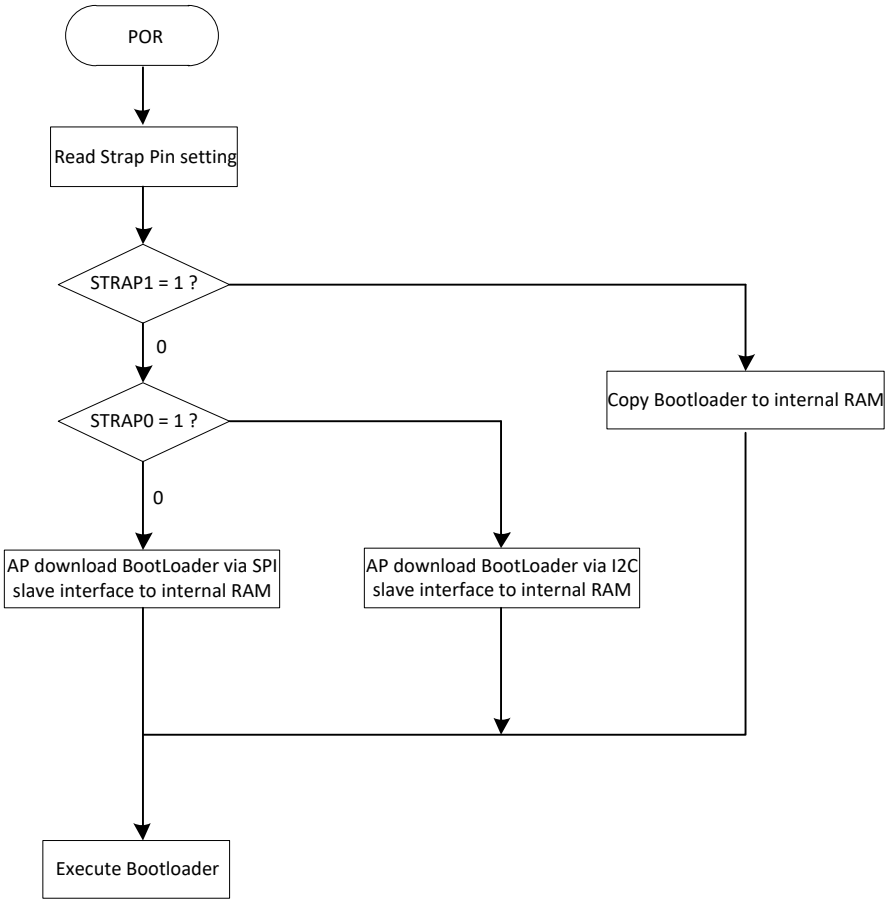


Fig.7 boot process

6 DC Information

Tab.6 Absolute Max Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Analog and I/O power	VDDIO	1.6	1.8/3.3	3.6	V
Digital and DSP LDO input	VREG_IN	1.09	1.2/1.8/3.3	3.6	V
Ambient Operating Temperature	Ta	-20	-	+85	℃
Storage Temperature	Ts	-20	-	+125	℃
HBM ESD (Electrostatic Discharge)					
-			**Susceptibility Voltage**		
All pin			**2KV**		

VDD= 1.8V, Tambient=25°C, with 20pF external load.

Tab.7 electrical characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	Vin	-0.30	-	VDD +0.30	V
High level input voltage	VIH	0.65* VDD	-	-	V
Low level input voltage	VIL	-	-	0.35* VDD	V
High level output voltage	VOH	0.9*VDD	-	-	V
Low level output voltage	VOL	-	-	0.1*VDD	V
Output Pad Drive Current	-	-	8	-	mA
Internal Pull Up/Down Resistance	-	-	1M	-	ohms

Tab.8 analog IP performance

Parameter	Min	Typ	Max	Units
Full Swing Input Voltage AMIC_IN to ADC	-	1.2	-	Vpp
S/N Ratio AMIC_IN to ADC2	-	-	-	dBFSA
Total Harmonic Distortion + Noise when input -3dB of FSIV AMIC_IN to ADC2	-		-	dBFS
Input Impedance AMIC_IN	16K	50K	-	ohms
Pll0 current	-	60	-	uA
Pll1 current	-	50	-	uA
One channel ADC + PGA	-	55	-	uA
PMU	-	30	-	uA

7 Timing Requirements

7.1 Power-On Timing

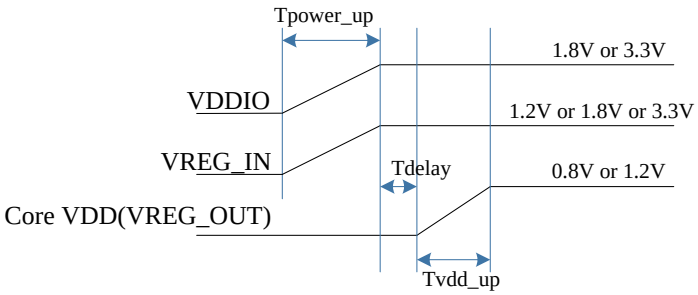


Fig.8 Power Sequence

Tab.9 Power Sequence Timing

Timing	Min	Typ	Max	Description
Tpower_up	100us	500us	1ms	External Power up time
Tdelay	-	100us	-	Delay time to core vdd ramp up
Tvdd_up	-	250us	-	Core vdd ramp up time

7.2 SPI-slave Interface

SPI slave interface supports 4 protocol.

Tab.10 SPI-slave protocol

Protocol	Description
32bit write	Single write 32Bit
32bit read	Single read 32Bit
burst write	Write burst n*32Bit
burst read	Read burst n*32Bit

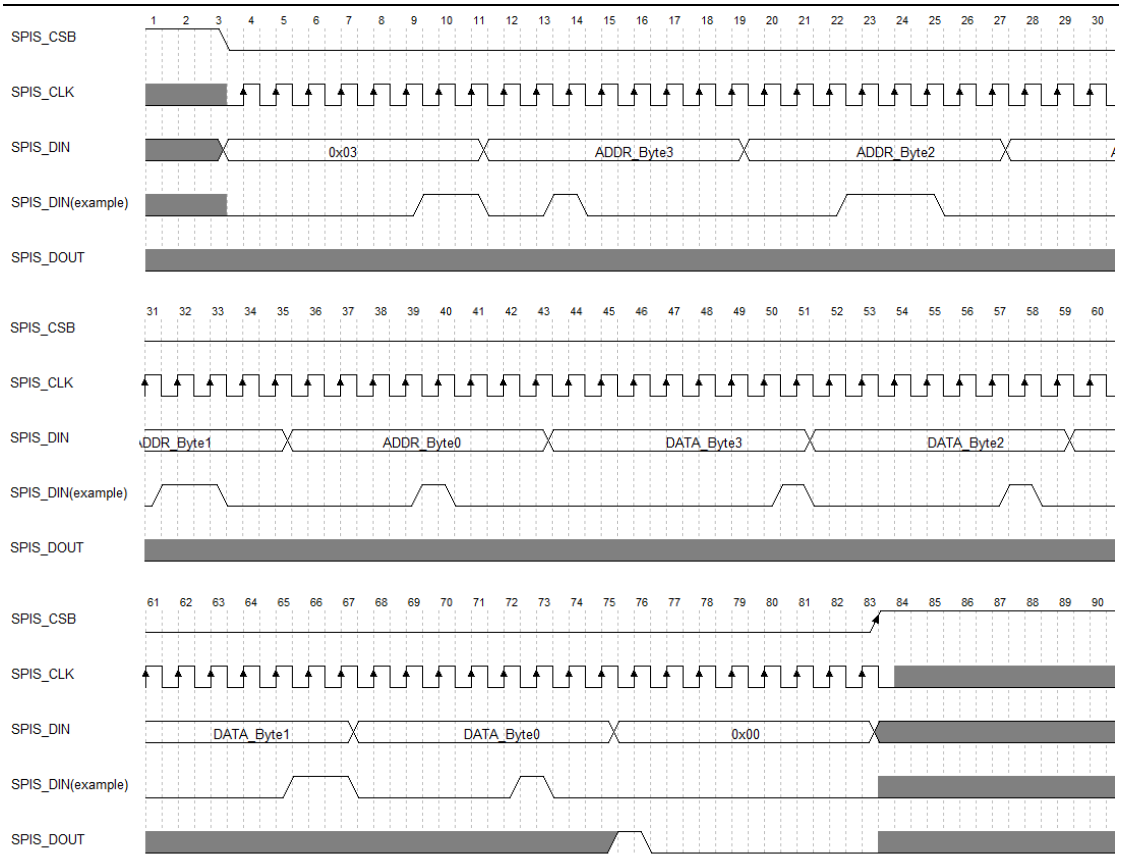
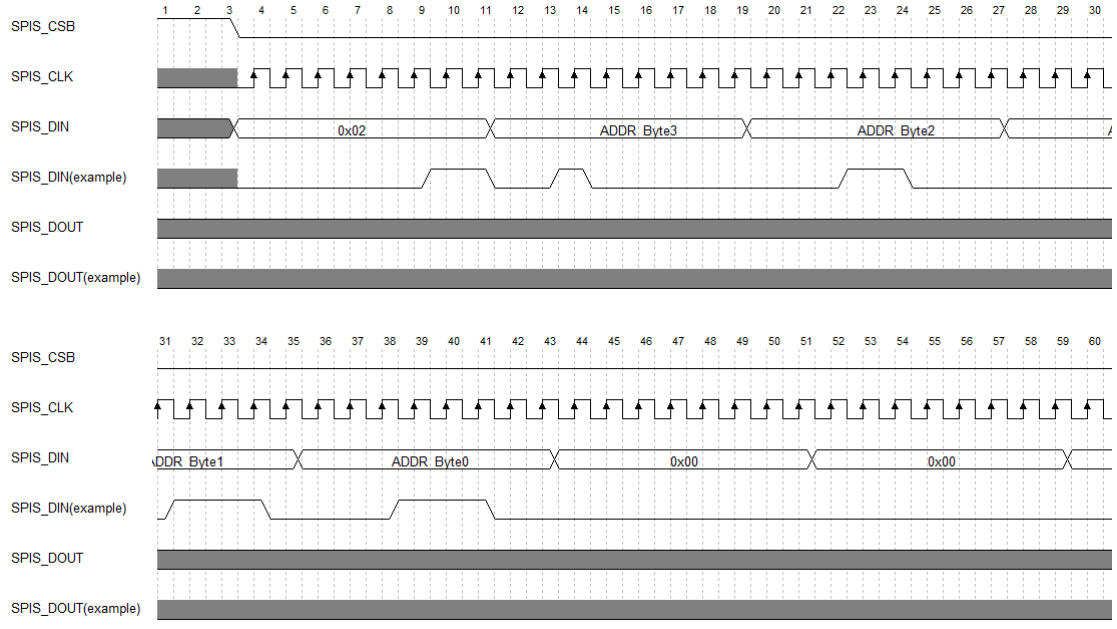


Fig.9 SPI-slave 32bit write protocol



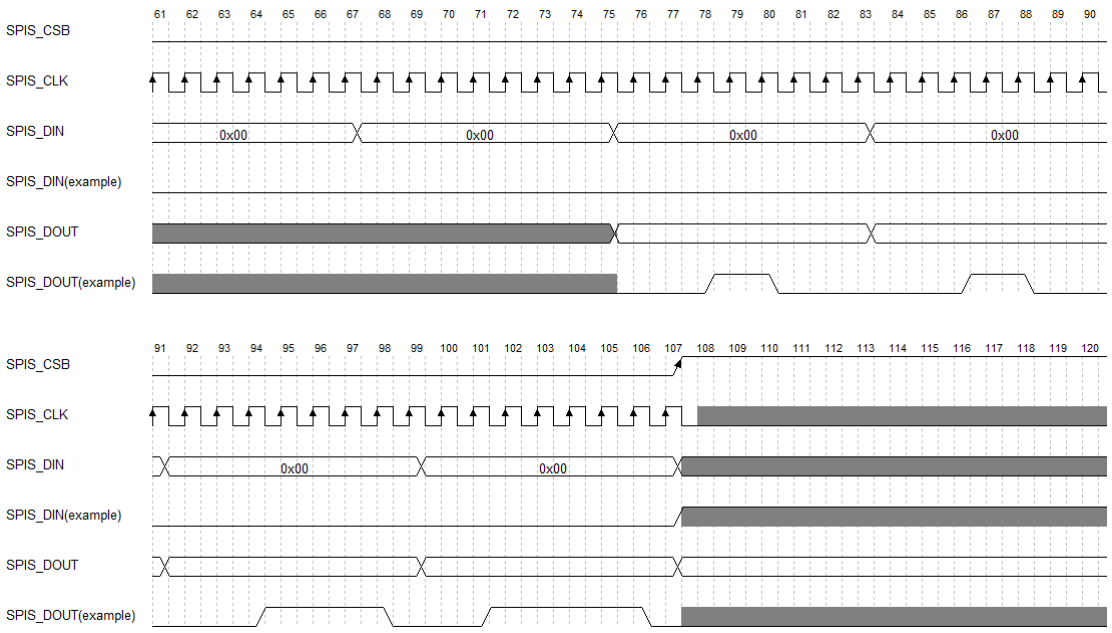
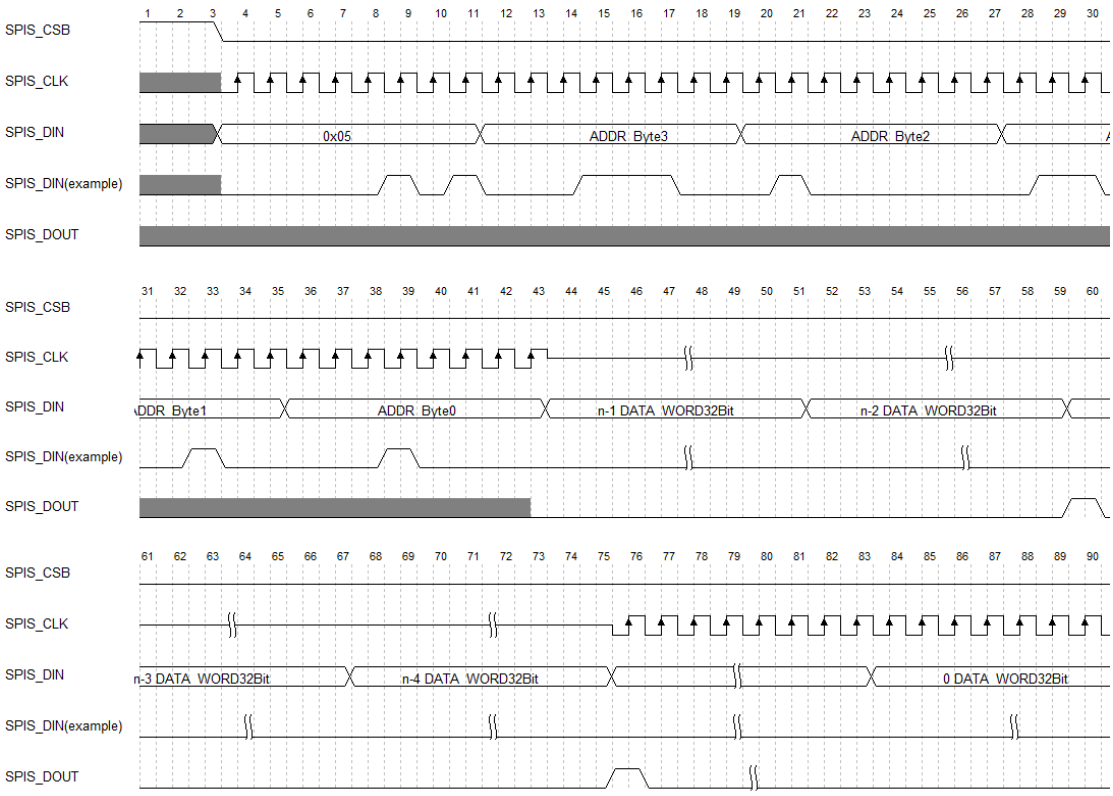


Fig.10 SPI-slave 32bit read protocol



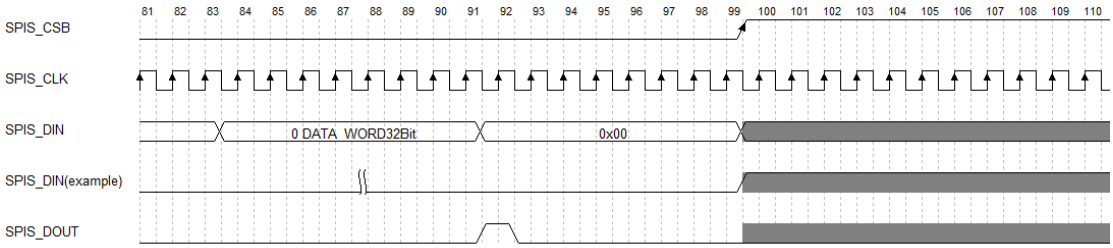
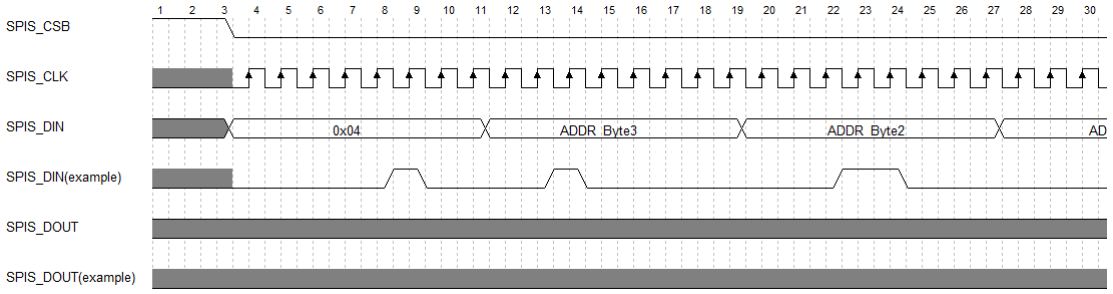
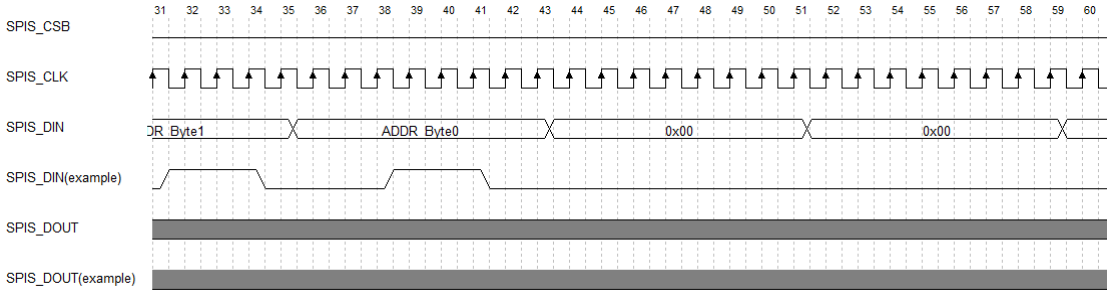
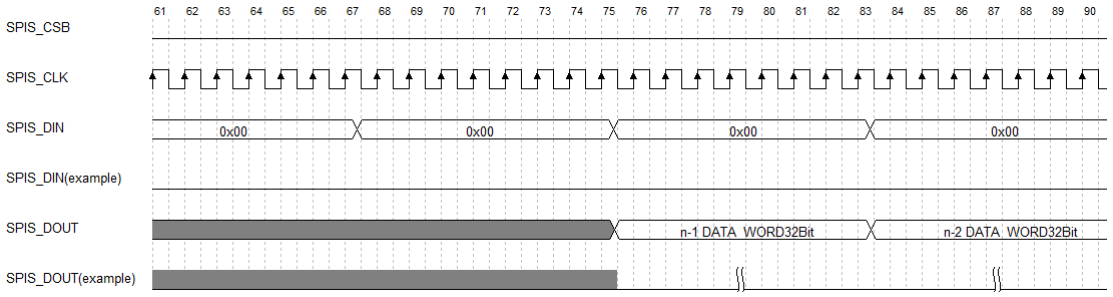
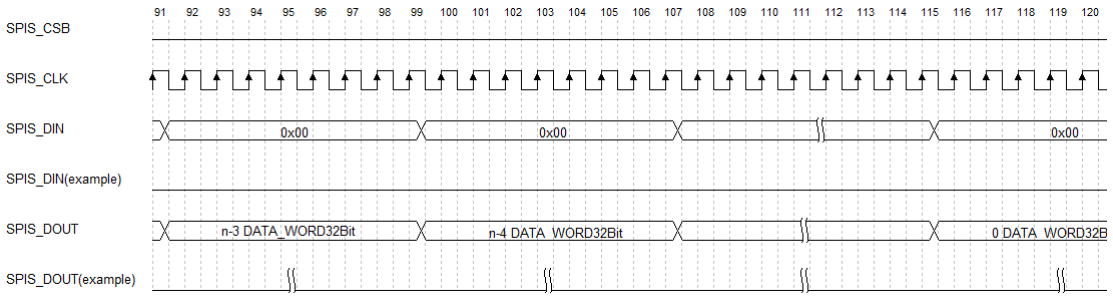


Fig.11 SPI-slave burst write protocol









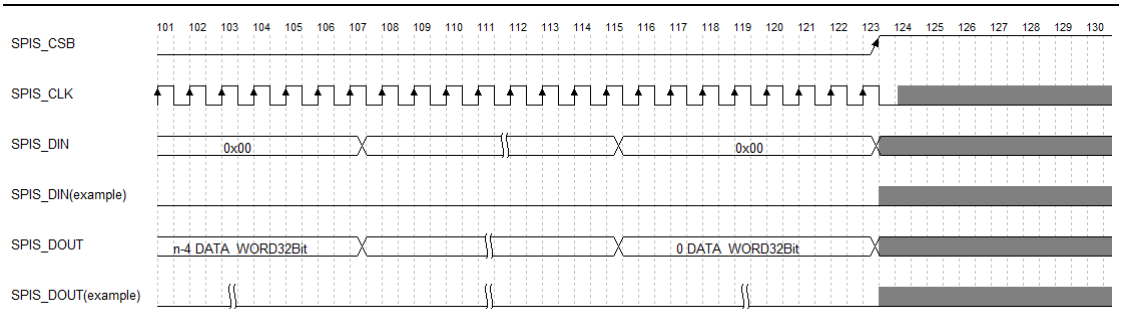


Fig.12 SPI-slave burst read protocol

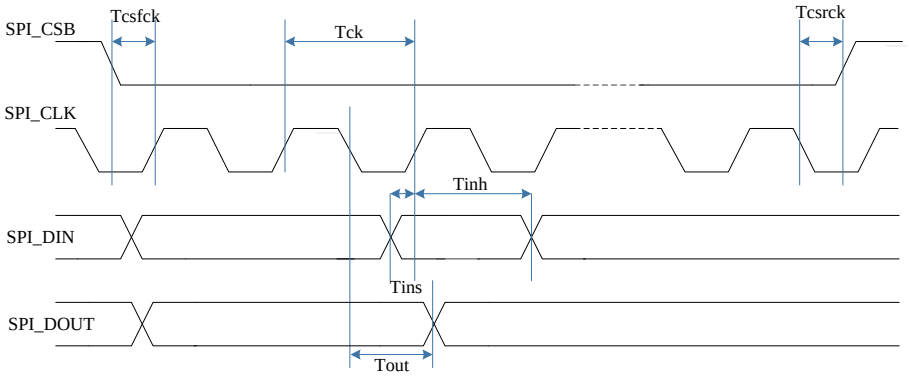


Fig.13 SPI Timing

Tab.11 SPI-slave interface timing

Timing	Min	Typ	Max	Description
Tcsfck	8ns	-	-	SPI_CSB falling edge to SPI_CLK
Tcsrck	8ns	-	-	SPI_CSB rising edge to SPI_CLK
Tck	41.7ns	50ns	-	SPI clock period
Tins	8ns	-	-	SPI_DIN setup time
Tinh	8ns	-	-	SPI_DIN hold time
Tout	-	-	8ns	SPI_DOUT output timing

7.3 I2C-slave Interface

I2C slave interface supports 3 protocol.

Tab.12 I2C-slave protocol

Protocol	Description
32bit write	Single write 32Bit
32bit read	Single read 32Bit
burst write	Write burst n*32Bit

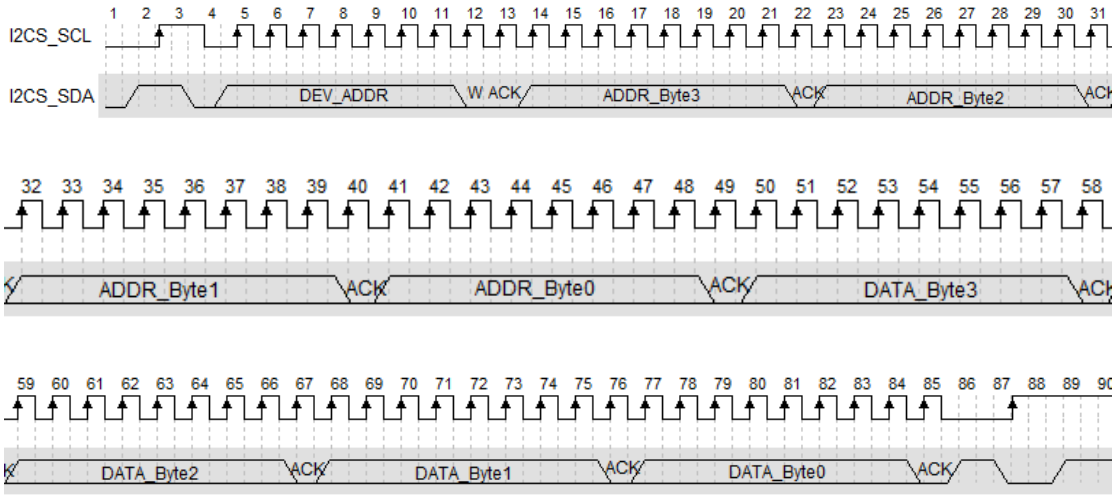


Fig.14 I2C-slave 32bit write protocol

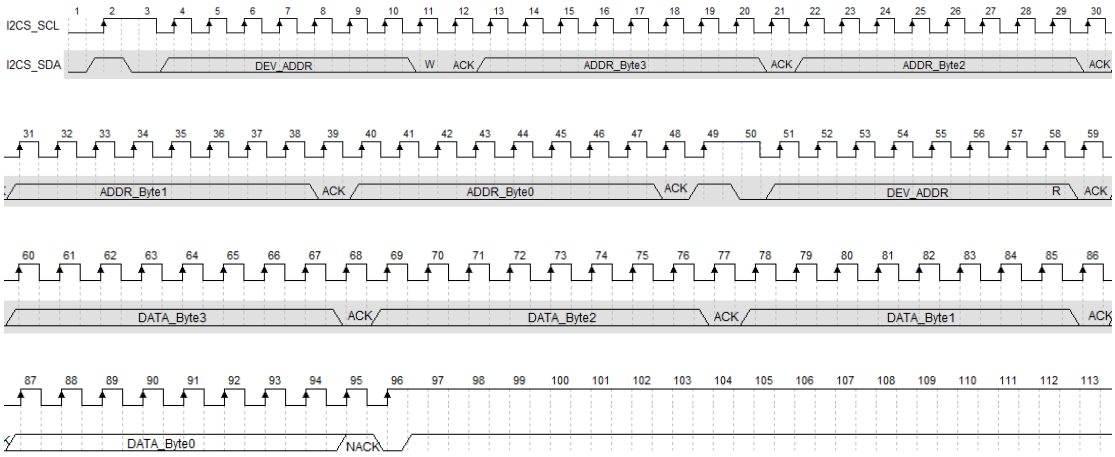
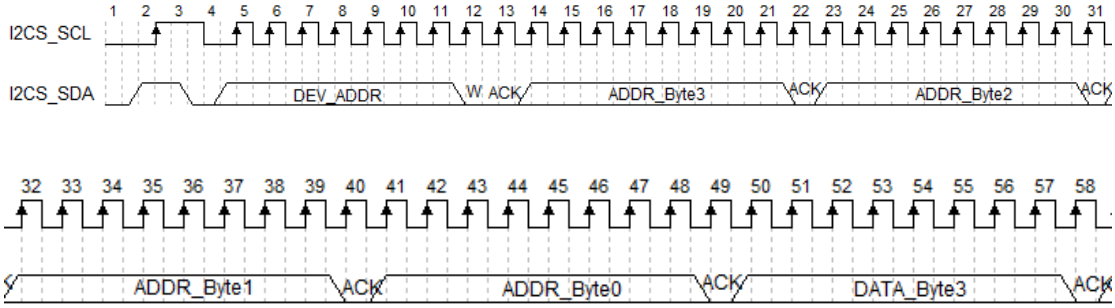


Fig.15 I2C-slave 32bit read protocol



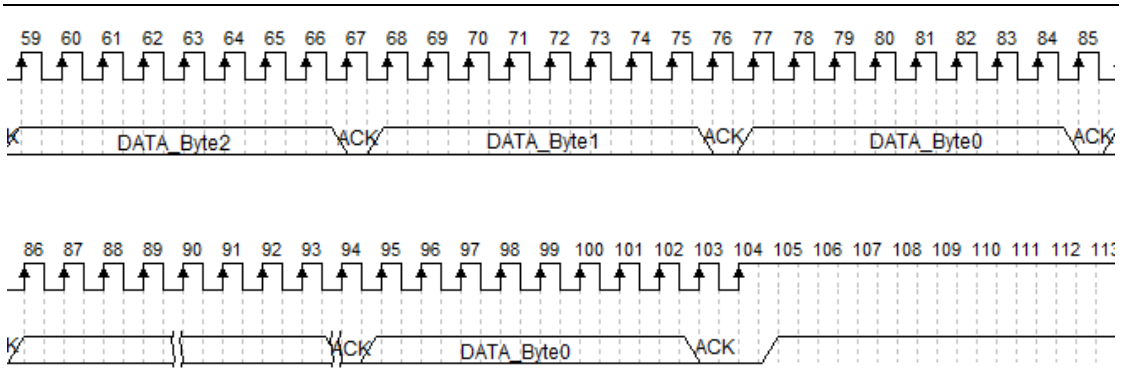


Fig.16 I2C-slave burst write protocol

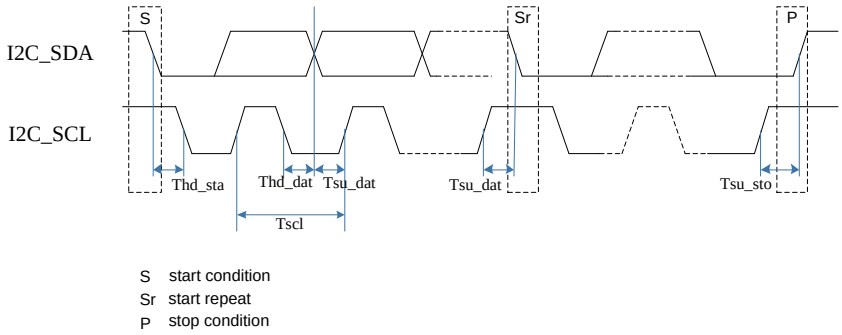


Fig.17 I2C-slave Timing

Tab.13 I2C-slave interface timing

Timing	Min	Typ	Max	Description
Tscl	-	2.5us	-	SCL clock period
Thd_sta	-	0.8us	-	Hold time (repeated) START condition.
Thd_dat	-	0.8us	-	Data hold time
Tsu_dat	-	0.5us	-	Data setup
Tsu_sto	-	0.8us	-	Setup time for STOP condition

7.4 I2S Interface

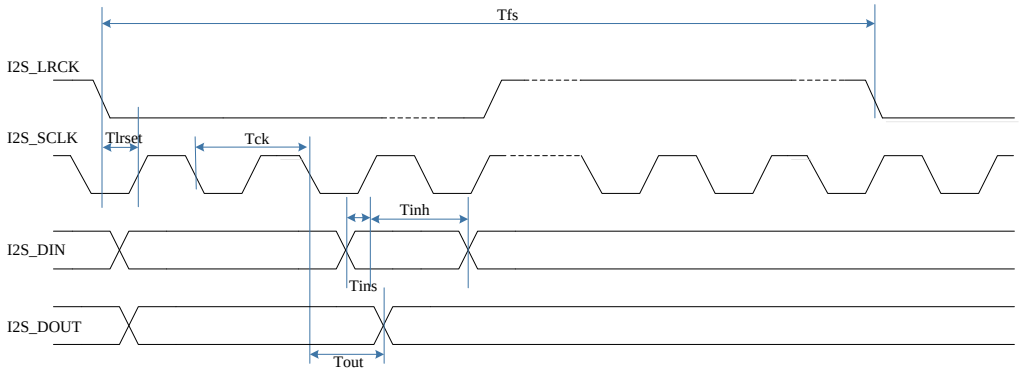


Fig.18 I2S Timing

Tab.14 I2S interface timing

Timing	Min	Typ	Max	Description
Tfs	8kHz		192kHz	I2S_LRCK frequnece
Tlrset	10ns			I2S_LRCK setup time
Tck			12.288MHz	I2S_SCLK frequnece
Tins	10ns			I2S_DIN setup time
Tinh	10ns			I2S_DIN hold time
Tout			10ns	I2S_DOUT output timing
● Support 8KHz ~ 48KHz sampling rate, from 2 channel to 4 channel				

7.5 PDM Interface

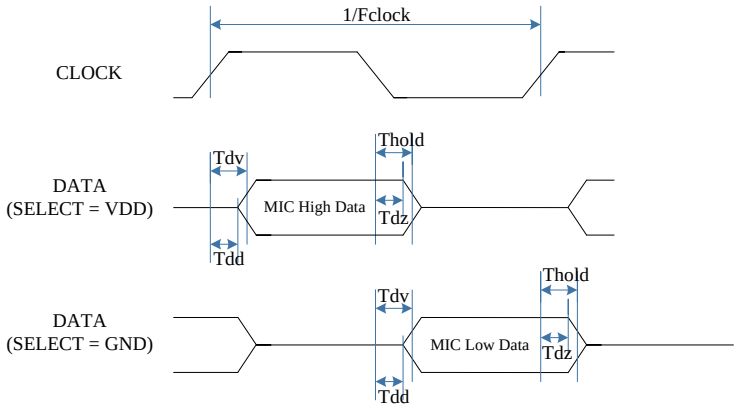
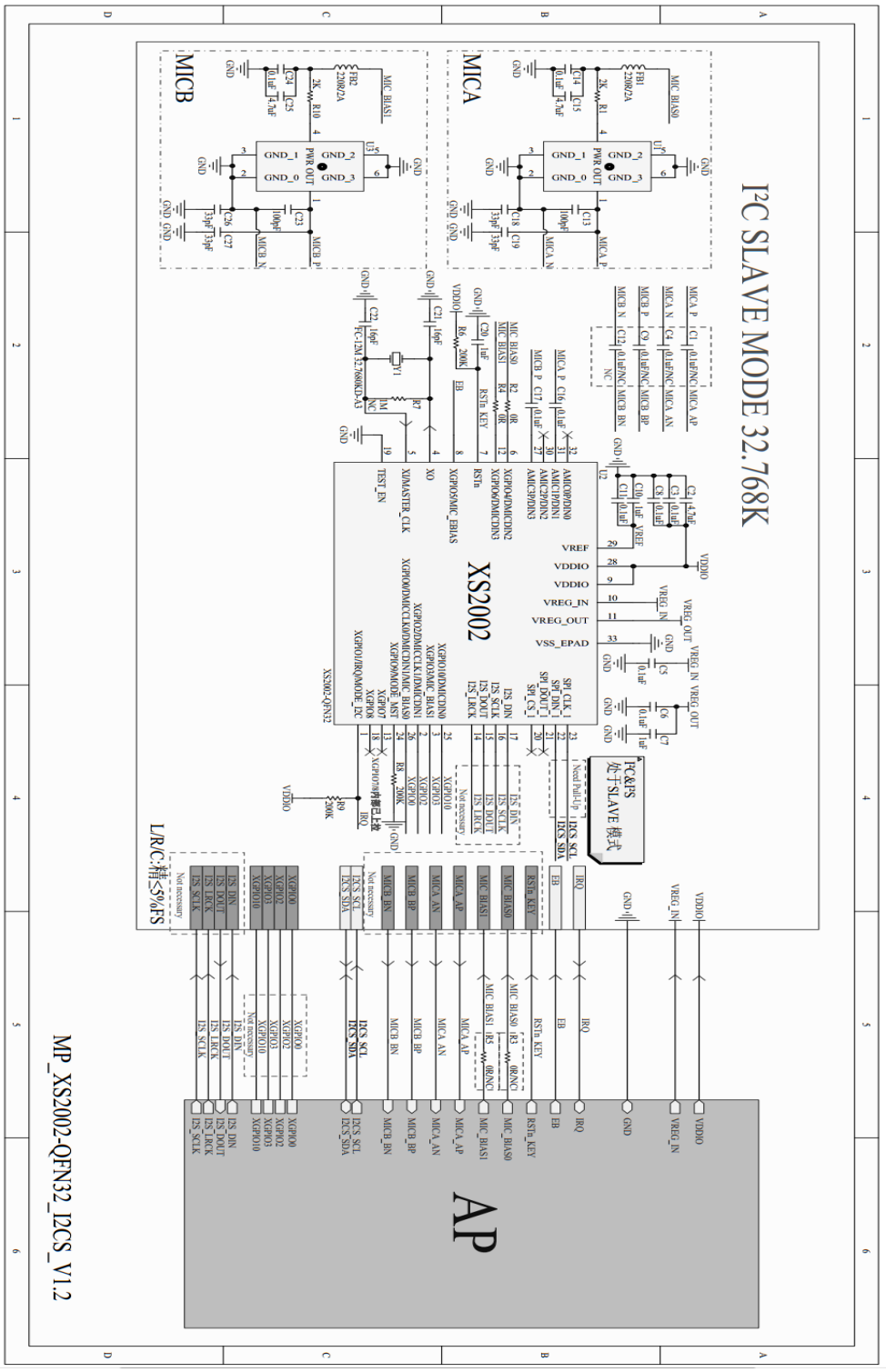


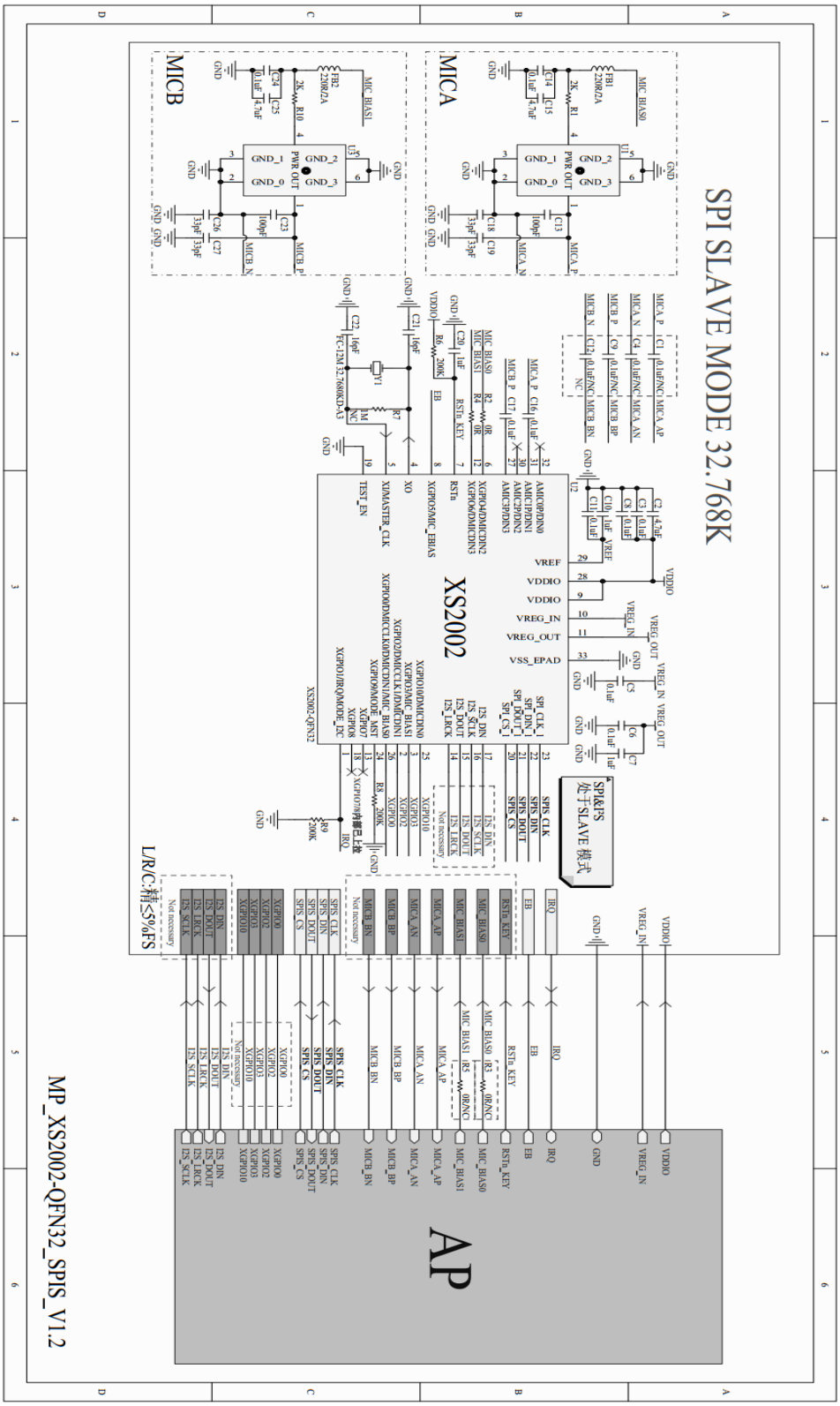
Fig.19 Digital MIC interface timing

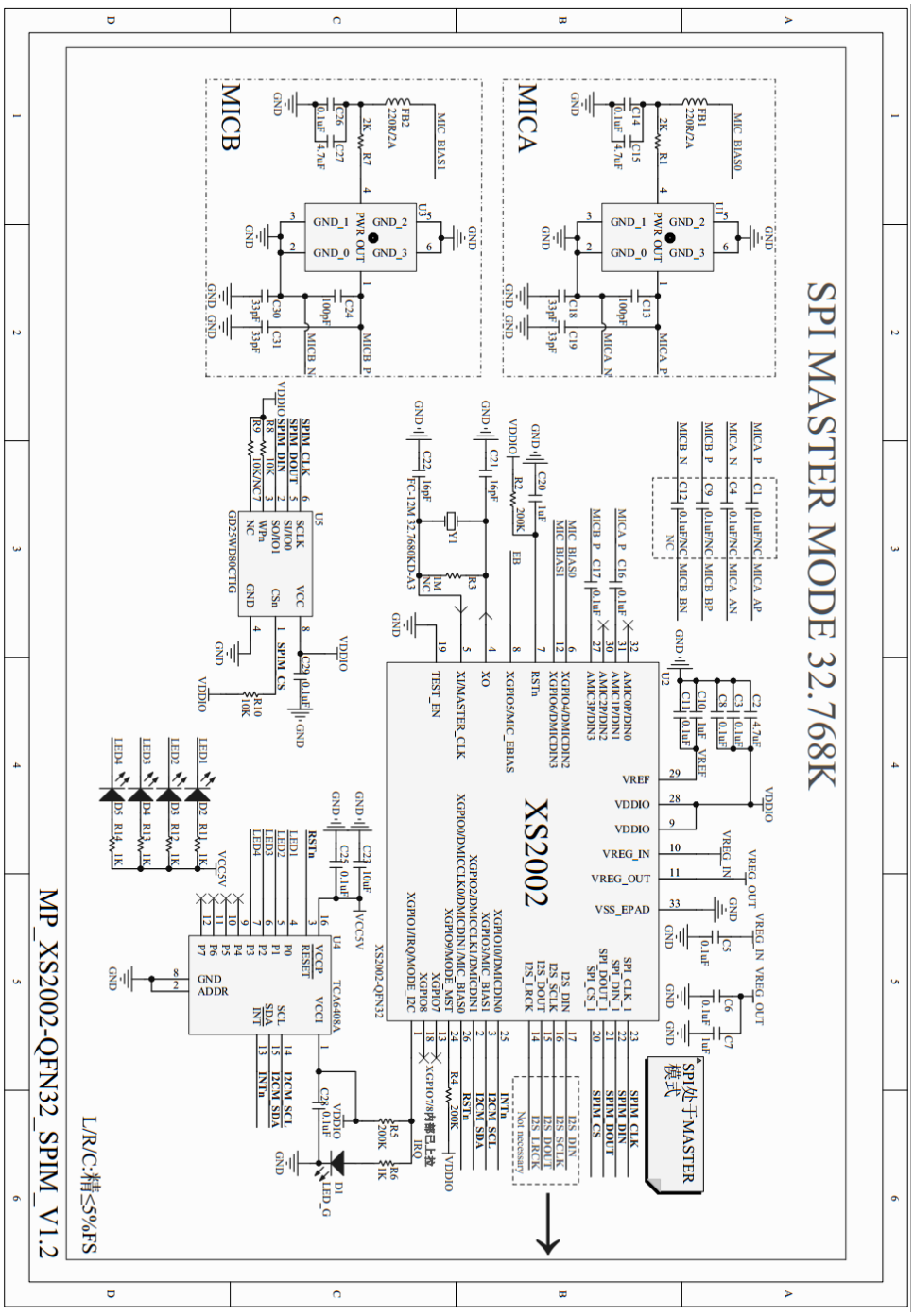
Tab.15 Digital MIC interface timing

Timing	Min	Typ	Max	Description
Fclock	0kHz	-	3.072MHz	PDM clock frequency
Tdd	18ns	-	40ns	Delay time to data line driven
Tdv	-	-	100ns	Delay time to valid data
Tdz	3ns	-	16ns	Delay time to High-Z
Thold	3ns	-	-	Hold time

8. Hardware and Layout Design Guide

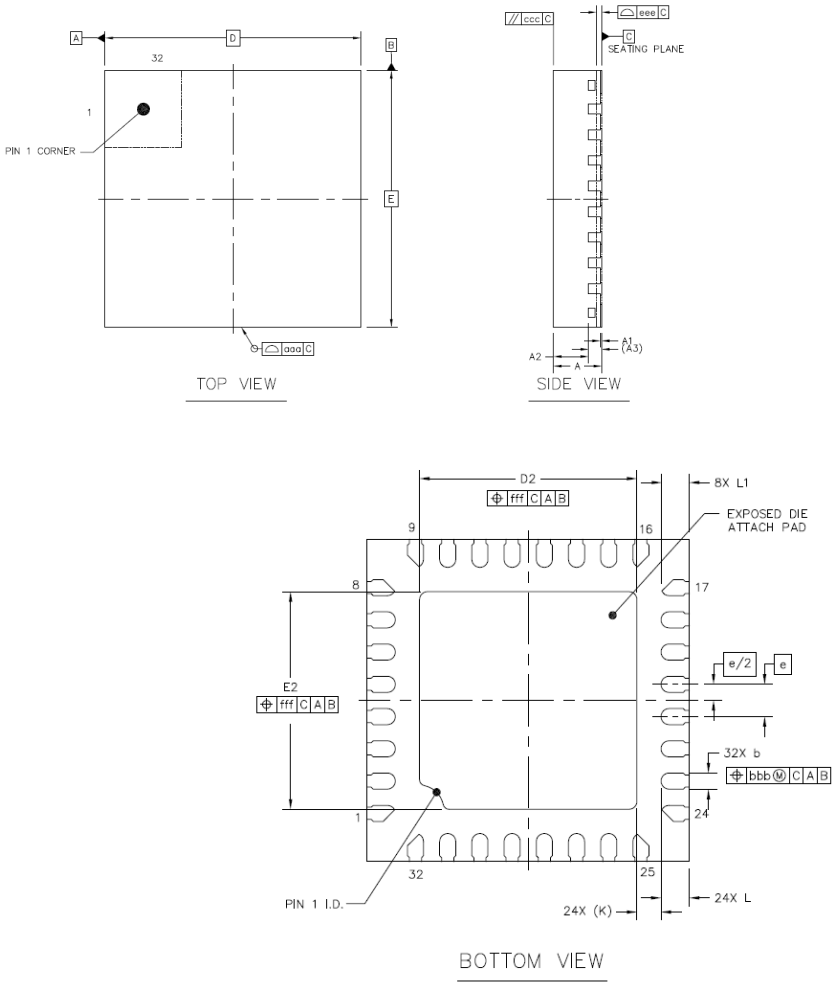



SPI SLAVE MODE 32.768K
MICA
MICB
XS2002
AP
SPI&IFS 处于SLAVE 模式
L/R/C:精≤5%FS
MP_XS2002-QFN32_SPIS_V1.2


SPI MASTER MODE 32.768K
MICA
MICB
XS2002
XS2002-QFN32
SPI_CLK
SPI_DIN
SPI_DOUT
SPI_CS
SPI处于MASTER模式
L/R/C:精≤5%FS
MP_XS2002-QFN32_SPIM_V1.2

9. Package and Packing material

a) QFN32 Package



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	2.6	2.7	2.8
	Y	E2	2.6	2.7	2.8
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.24	0.34	0.44
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

b) Packing material

Part number	Num	information
XS2002	2000	QFN32(4x4x0.75)， Tape&Reel
XS2002	5000	QFN32(4x4x0.75)， Tape&Reel