CMX940
High Performance RF Synthesizer

Low-power high performance Frac-N PLL with fully integrated VCO

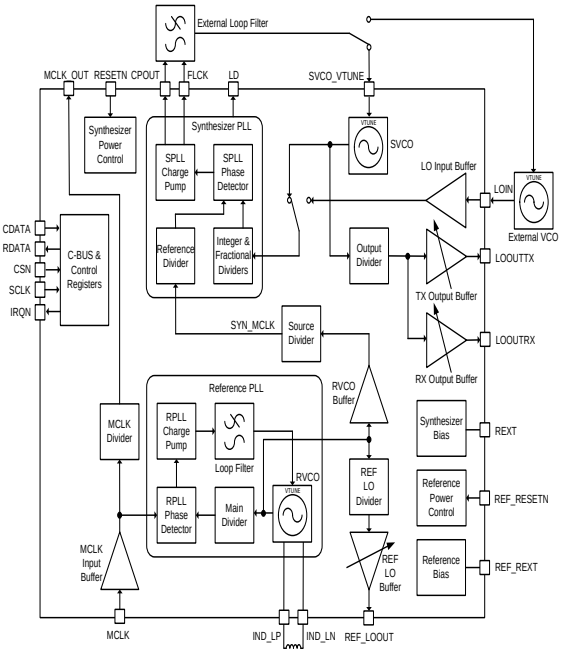
D/940/1 September 2020 Advance

Features

- RF output frequency 49 - 2040 MHz
- Low current consumption
- Supply voltage 3.0 - 3.6 V
- Low 1 Hz normalized PLL noise floor -225 dBc/Hz
- Phase noise -123 dBc/Hz, 25 kHz offset at 435 MHz
- Dual programmable RF outputs
- Low noise VCO -142 dBc/Hz, 1 MHz offset at 435 MHz
- Low level of spurious products
- Automatic VCO selection and calibration
- 16- and 24-bit fractional-N PLL modes
- High comparison frequency 120 MHz
- Very fast frequency switching <50 µs
- Compatible with EN 300 113, EN 300 086

Applications

- PMR / LMR
- Wireless Data Modem
- GNSS RTK
- General Purpose RF and IF
- Marine Radio



1 Brief Description

The CMX940 is a low-power high performance Fractional-N PLL with fully integrated wideband VCO and programmable output divider, generating RF signals over a continuous frequency range of 49 MHz to 2040 MHz. It has two single-ended RF outputs to support Tx and Rx sub-systems. A configurable reference path can be used to minimize close-in phase noise and mitigate integer boundary spurious. On-chip registers are controlled by an SPI compatible C-BUS serial interface.

Available in a 48-pin 7x7 mm LGA package, CMX940 is highly integrated to reduce component count and PCB board area, requiring only loop filter and clock reference to provide a complete and very compact RF synthesizer solution. Low operating voltage and low power consumption make it the perfect choice for a wide variety of portable and battery powered wireless applications, including digital narrowband two-way radio equipment compliant with ETSI standards.

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It is recommended that you check for the latest product datasheet version from the CMX940 product page of the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
1	First public release	September 2020

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.

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2 Block Diagram

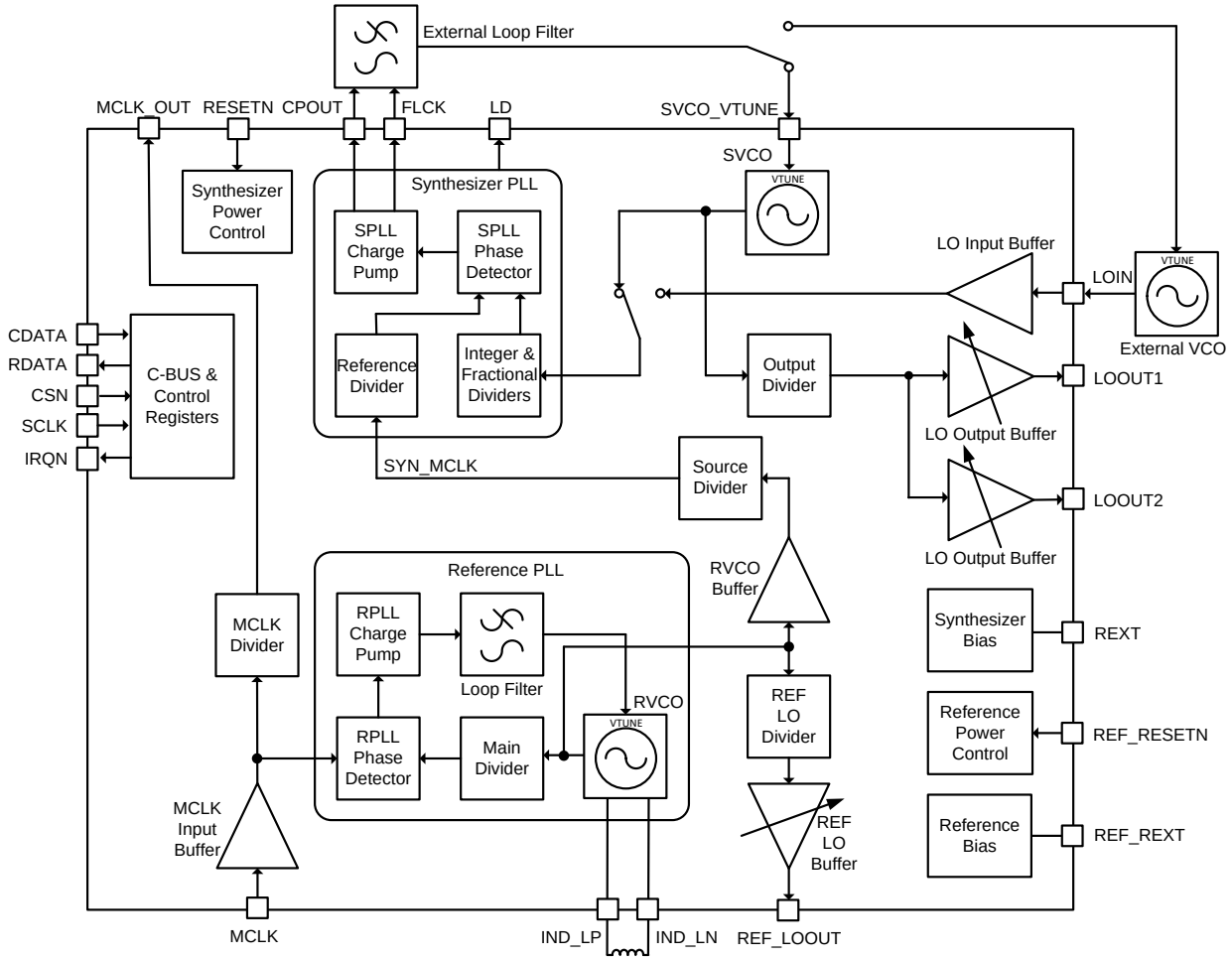

Figure 1 CMX940 Block Diagram

Note: Power and decoupling pins are not shown for clarity.

3 Pin and Signal List

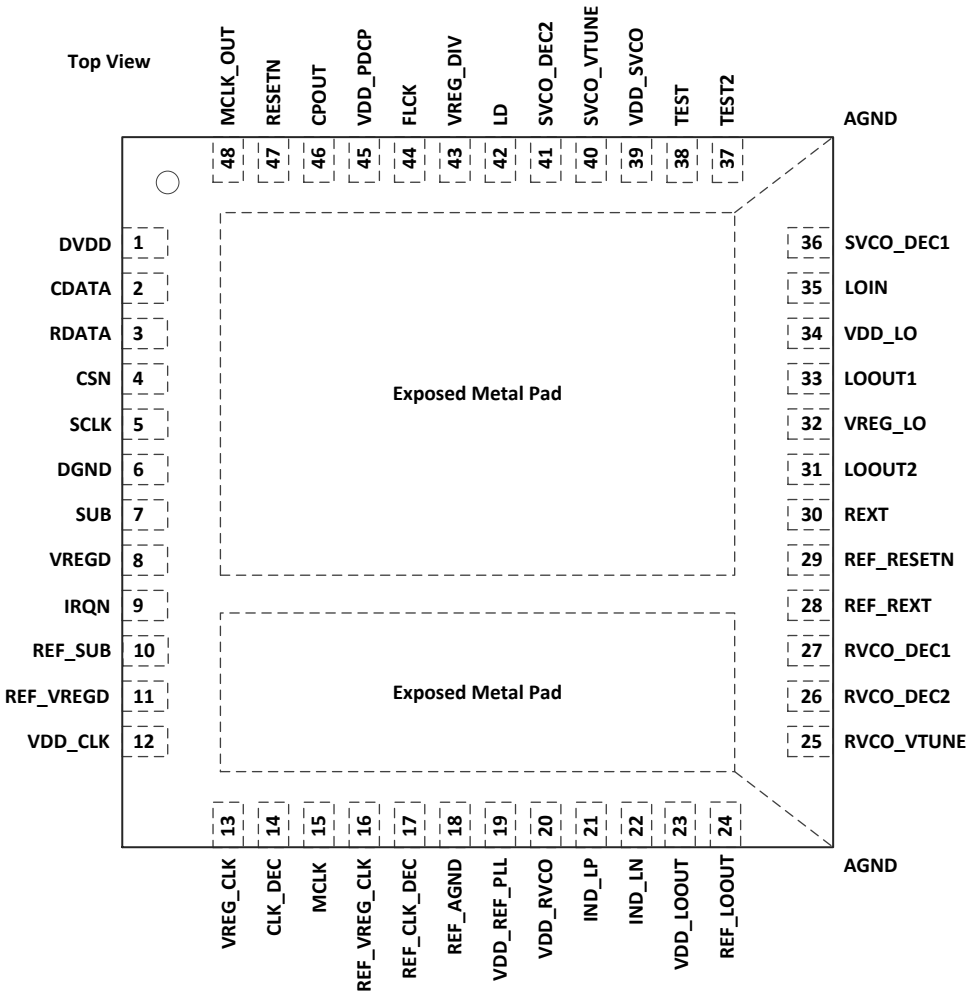

Figure 2 Package Diagram

Pin No.	Pin Name	Type	Description
1	DVDD	Power	Positive 3.3 V supply for the digital logic. This should be decoupled to DV_{SS} by a 10 nF capacitor mounted close to the supply pin.
2	CDATA	I/P	C-BUS serial data input from the µC.
3	RDATA	T/S	3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC. An external pullup resistor of 100kΩ to DV_{DD} is required.
4	CSN	I/P	Chip Select. An active low logic input is used to enable a C-BUS data read or write operation.
5	SCLK	I/P	C-BUS serial clock input from the µC.

Pin No.	Pin Name	Type	Description
6	DGND	Power	Ground for digital circuits.
7	SUB	Power	Digital logic substrate. Should be connected to DV_{SS}.
8	VREGD	Dec	An internally generated 1.8 V supply. This pin should be decoupled to DV_{SS} by a 100 nF capacitor mounted close to the supply pin.
9	IRQN	O/P	'Wire-ORable' output for connection to the host µC's Interrupt Request input. This output has a low impedance pull down to DV_{SS} when active and is high impedance when inactive. An external pullup resistor of 100 kΩ to DV_{DD} is required.
10	REF_SUB	Power	Reference digital logic substrate. Should be connected to DV_{SS}.
11	REF_VREGD	Dec	Internally-generated 1.8 V supply. This pin should be decoupled to DV_{SS} by a 100 nF capacitor mounted close to the supply pin.
12	VDD_CLK	Power	Positive 3.3 V supply for the MCLK voltage regulator. This should be decoupled to AV_{SS} by a 10 nF capacitor mounted close to the supply pin.
13	VREG_CLK	Dec	Internally-generated 1.8 V supply. This pin should be decoupled to AV_{SS} by a 470 nF capacitor mounted close to the supply pin.
14	CLK_DEC	Dec	Synthesizer MCLK voltage regulator filter. This pin should be decoupled to AV_{SS} by a 4.7 nF capacitor mounted close to the supply pin.
15	MCLK	I/P	Master clock input (10 MHz - 40 MHz). The input requires a suitable ac coupling capacitor.
16	REF_VREG_CLK	Dec	Internally-generated 1.8 V supply. This pin should be decoupled to AV_{SS} by a 470 nF capacitor mounted close to the supply pin.
17	REF_CLK_DEC	Dec	Reference MCLK voltage regulator filter. This pin should be decoupled to AV_{SS} by a 4.7 nF capacitor mounted close to the supply pin.
18	REF_AGND	Power	Reference PLL Analogue Ground (connect to AGND).
19	VDD_REF_PLL	Power	Positive 3.3 V supply for Reference PLL. This should be decoupled to AV_{SS} by a 10 nF capacitor mounted close to the supply pin.
20	VDD_RVCO	Power	Positive 3.3 V supply for the Reference VCO. This should be decoupled to AV_{SS} by a 10 nF capacitor mounted close to the supply pin.
21	IND_LP	I/P	Reference VCO inductor positive terminal.
22	IND_LN	I/P	Reference VCO inductor negative terminal.
23	VDD_LOOUT	Power	Positive 3.3 V supply for REF_LOOUT. This should be decoupled to AV_{SS} by a 10 nF capacitor mounted close to the supply pin.
24	REF_LOOUT	O/P	Reference LO Output
25	RVCO_TUNE	O/P	Reference VCO tune voltage output (test-point only).
26	RVCO_DEC2	Dec	Reference VCO decoupling pin 2 should be connected to AV_{SS} by a 47 nF capacitor mounted close to the supply pin.

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Pin No.	Pin Name	Type	Description
27	RVCO_DEC1	Dec	Reference VCO decoupling pin1 should be connected to AV_{SS} by a 27 nF capacitor mounted close to the supply pin.
28	REF_REXT	I/P	External 47.5 kΩ bias resistor connected to $AV_{SS.}$
29	REF_RESETN	I/P	Active high 3.3 V logic input which enables and resets the reference circuit. If REF_RESETN is low, the reference circuit is completely powered down and a reference power-on-reset event will occur the next time REF_RESETN is taken high to DV_{DD}. An external pullup resistor of 100kΩ to DV_{DD} is required.
30	REXT	I/P	External 47.5 kΩ bias resistor connected to $AV_{SS.}$
31	LOOUT2	O/P	Local oscillator output 2. The output requires a suitable ac coupling capacitor.
32	VREG_LO	Dec	Internally-generated 1.8 V supply (local oscillator voltage regulator). This pin should be decoupled to AV_{SS} by a 100nF capacitor mounted close to the supply pin.
33	LOOUT1	O/P	Local oscillator output 1. The output requires a suitable ac coupling capacitor.
34	VDD_LO	Power	Positive 3.3 V supply for local oscillator. This should be decoupled to AV_{SS} by a 10 nF capacitor mounted close to the supply pin.
35	LOIN	I/P	External local oscillator RF input (to lock an external VCO). If enabled, the input is high impedance and internally ac coupled. For best sensitivity, this should be LC matched to the operating freqeuency, but can be used with a broadband termination. If not used, connect to AV_{SS}
36	SVCO_DEC1	Dec	Synthesizer VCO decoupling pin1 should be connected to AV_{SS} by a 470 nF capacitor mounted close to the supply pin.
37	TEST2	NC	No user connection required.
38	TEST	O/P	Test-point only
39	VDD_SVCO	Power	Positive 3.3 V supply for the Synthesizer VCO. This should be decoupled to AV_{SS} by a 10uF and 1nF capacitor mounted close to the supply pin. Note that this should be used as the reference point for the loop filter when the internal VCO is used.
40	SVCO_VTUNE	I/P	Synthesizer VCO tune voltage input.
41	SVCO_DEC2	Dec	Synthesizer VCO decoupling pin 2 should be connected to AV_{SS} by a 470 nF capacitor mounted close to the supply pin.
42	LD	O/P	Lock Detect Output (active high = PLL locked)
43	VREG_DIV	Dec	Internally-generated 1.8 V supply (Fractional-N divider voltage regulator). This should be decoupled to AV_{SS} by a 100 nF capacitor mounted close to the supply pin.
44	FLCK	O/P	Fast Lock Output. Refer to Figure 4 and section 6.7.11.
45	VDD_PDCP	Power	Positive 3.3 V supply for the Synthesizer Phase Detector and Charge Pump. This should be decoupled to AV_{SS} by a 10 nF capacitor mounted close to the supply pin.
46	CPOUT	O/P	Synthesizer Charge Pump output.

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Pin No.	Pin Name	Type	Description
47	RESETN	I/P	Active high 3.3 V logic input which enables and resets the synthesizer circuit. If RESETN is low, the synthesizer circuit is completely powered down and a synthesizer power-on-reset event will occur the next time RESETN is taken high to DV_{DD}. An external pullup resistor of 100 kΩ to DV_{DD} is required.
48	MCLK_OUT	O/P	MCLK output.
EXPOSED METAL PADS	AGND	Power	Ground for analogue circuits. The central metal pads must be connected to AV_{SS}.

Notes: I/P = Input
O/P = Output
BI = Bidirectional
T/S = 3-state Output
NC = No Connection
Dec = Decoupling

3.1 Signal Definitions

Signal Name	Pins	Usage
AV_{DD}	VDD_CLK, VDD_REF_PLL, VDD_RVCO, VDD_LO, VDD_SVCO, VDD_PDCP	Power supply for analogue circuits.
DV_{DD}	DVDD	Power supply for digital circuits.
DV_{SS}	DGND, SUB	Ground for digital circuits.
AV_{SS}	AGND	Ground for analogue circuits.

Table 1 Definition of Power Supply and Reference Voltages

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4 External Components

4.1 Power Supply and Decoupling

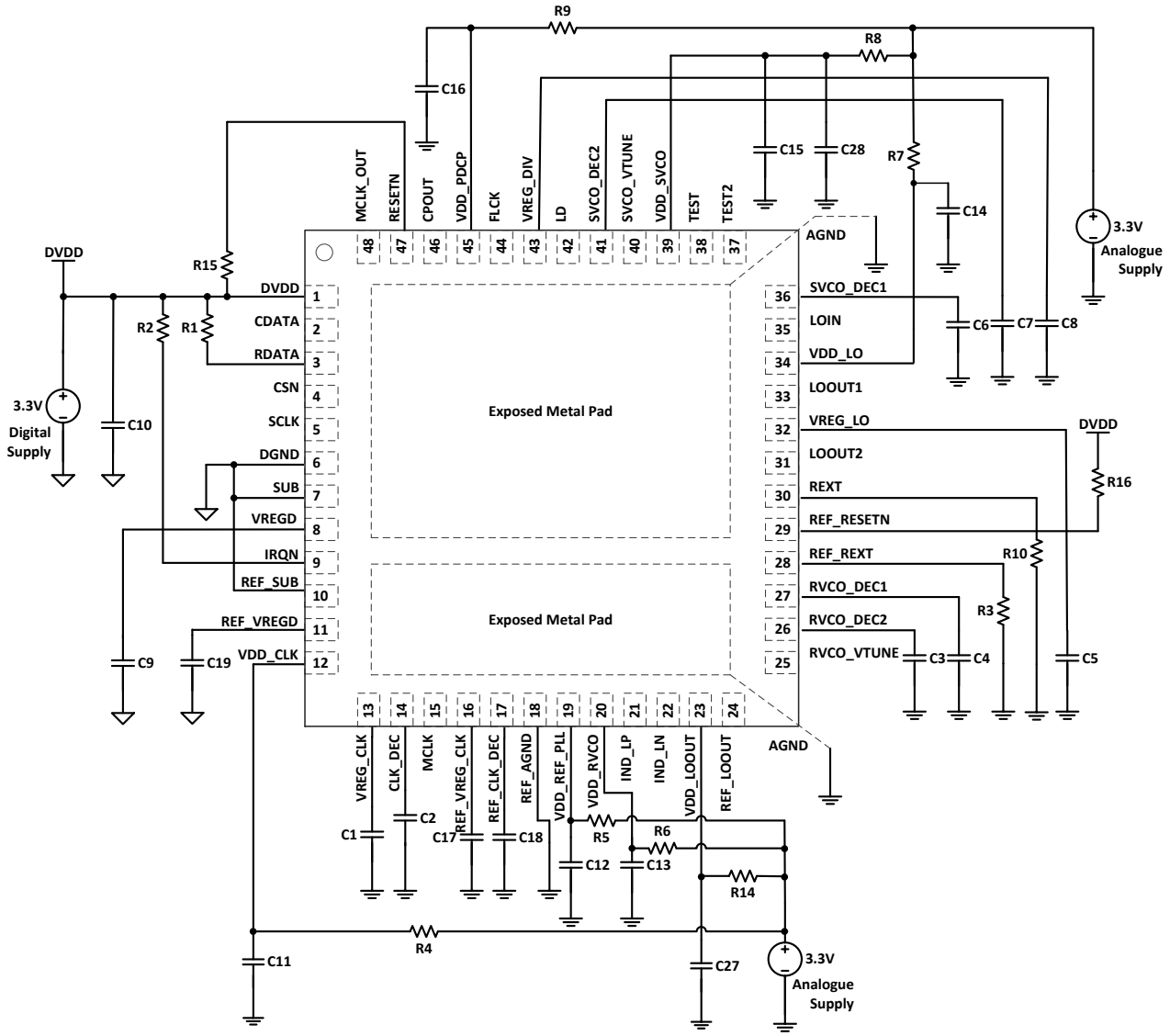

Figure 3 Power Supply and Decoupling External Components

Table 2 Typical Power Supply and Decoupling External Component Values

Component	Value	Tolerance
R1,2,15,16	100 kΩ	1%
R3,10	47.5 kΩ	1%
R4,5,6,7,14	10 Ω	1%
R8,9	3.3 Ω	1%
C5,8,9,19	100 nF	10%
C1,6,7,17	470 nF	10%
C2,18	4.7 nF	10%
C3	47 nF	10%

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C4	27 nF	10%
C10,11,12,13,14,16,27	10 nF	10%
C15	10 µF	10%
C28	1 nF	10%

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4.2 RF System

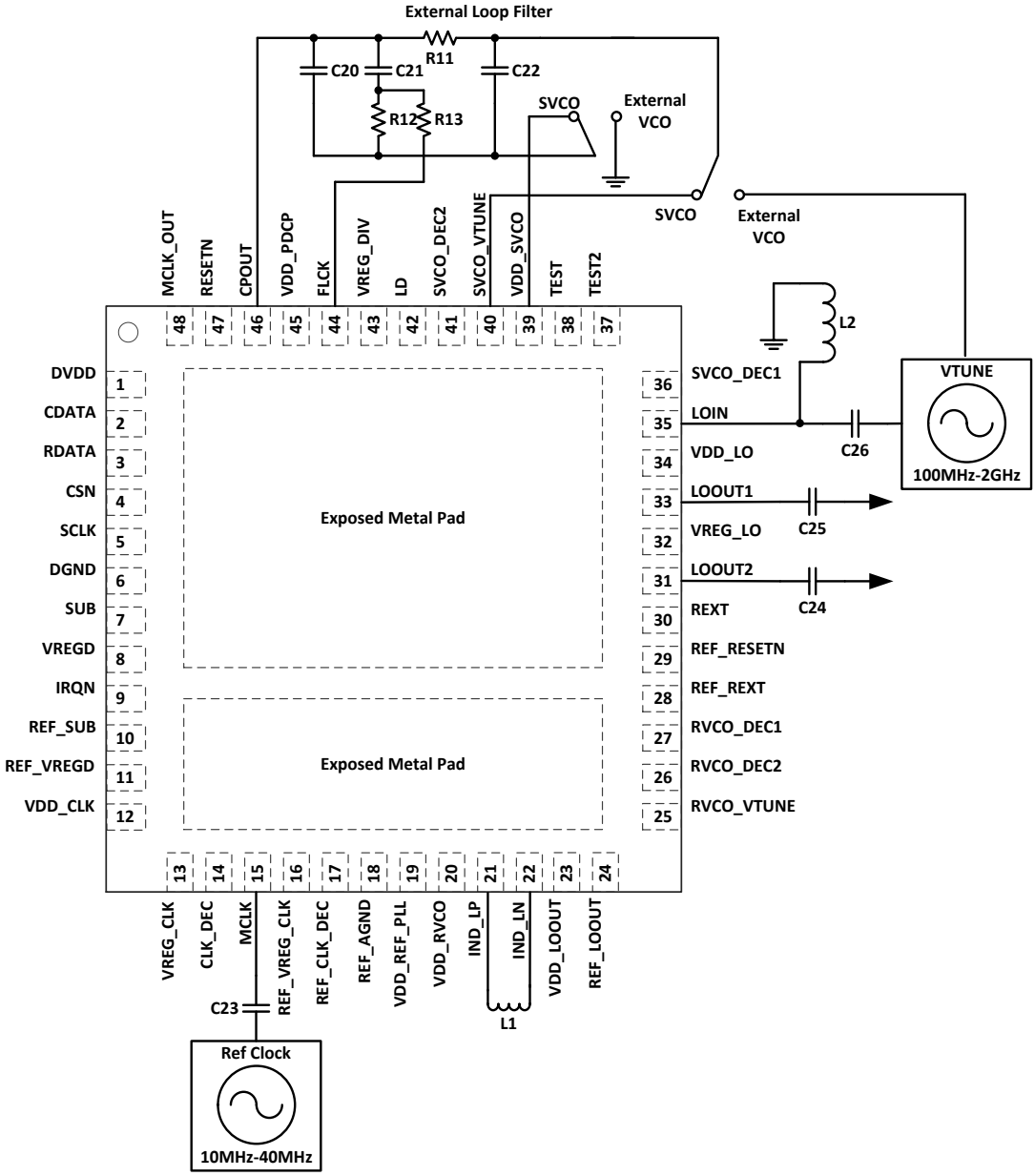

Figure 4 RF System External Components

Table 3 Typical RF System External Component Values

Component	Value	Tolerance	Notes
R11	1.8 kΩ	1%	Typical loop filter component values. See section 7.3 for further details. R13 is used for 'fast lock' with an external VCO – see section 6.7.11.
R12	470 Ω	1%	
R13	-	1%	
C20	680 pF	5%	
C21,23	10 nF	10%	
C22	68 pF	5%	

C24,25	100 pF	5%	ac coupling capacitors
L1	2.2 nH - 18.0 nH	2%	Depends on RVCO centre frequency - see Table 4.
C26	1.5 pF	5%	Only required for external VCO matching (see L2)
L2	15nH	5%	Only required for external VCO matching. These values are optimised for 800 MHz to 1 GHz operation and will be different for other frequencies. A broadband input match can be obtained with L2 = 50 Ω and C26 = 0 Ω with reduced sensitivity.

Note: PCB parasitics may contribute and the above match values should be verified in the user's layout.

Table 4 Typical RVCO Centre Frequency and Approximate Tuning Range with External Inductor

Centre Frequency (MHz)	Tuning Range (MHz)	External Inductor L1 (nH)
552	TBD	-
638	570 - 700	15.0
977	880 - 1075	4.7
1050	940 - 1150	3.9
1100	960 - 1190	3.3
1158	TBD	-
1228	TBD	-

Notes:

- The approximate external inductor value L1 can be selected for the required RVCO centre frequency f_c by use of the following equation:

  $f_c = 1/(2\pi\sqrt{((1.6nH + L1) * 4.2pF)})$

  where:
  - 1.6 nH is the value of the package and typical PCB inductance.
  - 4.2 pF is the on-chip capacitance at the centre frequency.
- The integrated RVCO calibration function adjusts the on-chip capacitance from 3.2 pF to 5.2 pF.
- The above inductor values assume that there is ~2.5 mm of PCB track length from each chip output to the corresponding inductor pad.
- The tuning ranges shown above are the approximate usable ranges for reliable calibration given the use of a 2% inductor. Use of a wider tolerance inductor will result in a greater spread of calibration values. Use near the high or low extremes of the frequency calibration range is not recommended for reliable operation.

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5 General Description

5.1 Overview

The CMX940 is a low noise general purpose 48.57 MHz - 2.04 GHz RF synthesizer. Utilising a novel dual-loop architecture, the CMX940 integrates a 24-bit fractional-N Synthesizer PLL (SPLL) and a low-noise Reference PLL (REF_PLL).

The SPLL operates from an internal 2.72 GHz - 4.08 GHz VCO (SVCO) or alternatively an external 100 MHz - 2 GHz VCO. The SPLL requires external components to implement the loop-filter, which gives the user greater flexibility to optimise the loop response for a given application. The SPLL reference clock may be sourced either from the internal REF_PLL or optionally from an external reference source.

The REF_PLL integrates a 600 MHz - 1.2 GHz fixed-frequency VCO (RVCO) with on-chip loop filter components and only requires one external VCO tuning inductor. Innovative techniques have been used to provide an exceptionally low noise method of multiplying the master reference frequency. This multiplier, when combined with the post divider, gives the user the option to avoid integer boundary spurs. The REF_PLL reference Master clock is sourced from an external 10 MHz – 40 MHz reference frequency.

The synthesizer includes a lock detect, fast lock functions and comprehensive automatic calibration.

The CMX940 includes a programmable Synthesizer VCO output divider and dual variable gain output buffers, with linear gain control, which are intended to provide the LO frequency sources to the Rx and Tx paths within a system.

5.2 Device Reset

The CMX940 Synthesizer logic is completely powered down if the RESETN pin is held low. If the RESETN pin goes high to DVDD, the on-chip Synthesizer digital logic voltage regulator is enabled and an integrated Power-On-Reset (POR) circuit resets the Synthesizer control registers to their default values.

The CMX940 REF_PLL logic is completely powered down if the REF_RESETN pin is held low. If the REF_RESETN pin goes high to DVDD, the on-chip REF_PLL digital logic voltage regulator is enabled and an integrated POR circuit resets the Reference control registers to their default values.

The POR sequences complete 100µs after their respective reset pin is driven high. C-BUS accesses to the device should not be attempted if either reset pin is low or during a POR period.

5.3 Main Clocks

The Reference Master Clock (MCLK) is input on the MCLK pin and used as a time base for calibration functions and as a reference clock for the REF_PLL. Prior to enabling MCLK in the REF_GCR ($75) register, the device must be configured with the external MCLK frequency by writing to the REF_MCLK_FREQ ($76) register so that a time base may be correctly established. The MCLK frequency range is 10 MHz to 40 MHz.

The Synthesizer Main Clock (SYN_MCLK) is the divided RVCO signal produced at the output of the Source Divider. SYN_MCLK is used as a time base for calibration functions and as a reference clock for the SPLL. Prior to enabling SYN_MCLK in the SYN_GCR ($2E) register, the device must be configured with the required Source Divider Value and the correct SYN_MCLK frequency by writing to the SYN_SDIV ($4D) and SYN_MCLK_FREQ ($2F) registers respectively so that a time base may be correctly established. The SYN_MCLK frequency range is 10 MHz to 120 MHz.

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5.4 Reference PLL

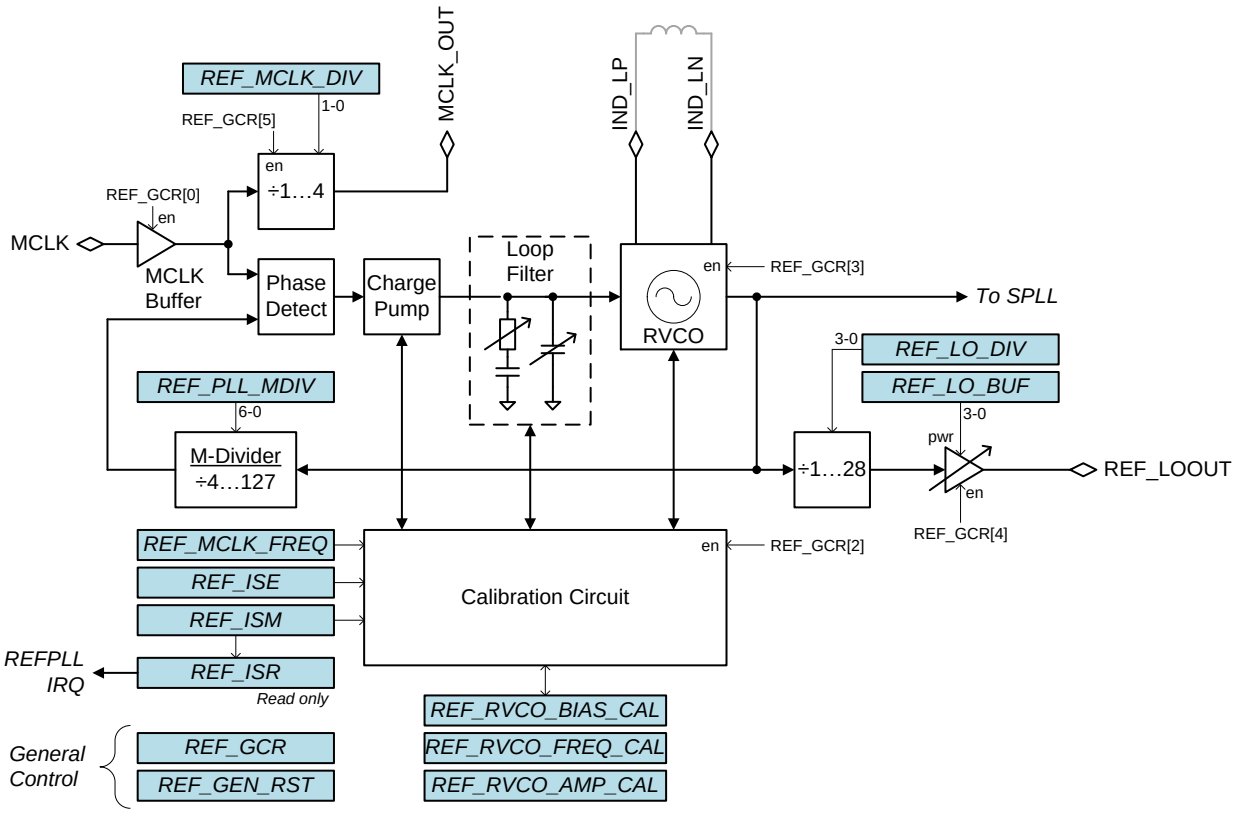

Figure 5 Reference PLL

The Reference PLL (REF_PLL), Figure 5, is designed to provide a low noise reference source frequency for the SPLL and enables boundary spurs to be reduced in the SPLL output. The REF_PLL reference frequency is sourced directly from the MCLK pin. The REF_PLL integer-M Divider value may be set to 4-127 using the REF_PLL_MDIV ($7A) register.

Prior to using the REF_PLL it must be calibrated. This should be done after configuring REF_MCLK_FREQ ($76), REF_PLL_MDIV ($7A), and the interrupt configuration registers REF_ISE ($77) and REF_ISM ($78). The calibration is performed automatically when bit 2 of the REF_PLL general control register REF_GCR ($75) is set. After calibration is complete, the calibration settings for that specific REF_PLL configuration get stored in the REF_RVCO_BIAS_CAL ($09), REF_RVCO_FREQ_CAL ($0B) and REF_RVCO_AMP_CAL ($2C) registers. For frequency hopping applications, these registers can be read by, and subsequently rewritten by, the host µC to rapidly reinstate the calibration settings for a particular REF_PLL configuration without performing a time-consuming re-calibration operation.

The user should choose REF_PLL_MDIV values that operate the RVCO around the centre of its tuning range in order to guarantee reliable calibration over tolerances of the RVCO inductor, internal tolerances, temperature, etc. Operating the REF_PLL with MDIV values +/- 1 or 2 of nominal to generate the SPLL reference can be used as a powerful spur avoidance technique. Operating the RVCO at lower frequencies (using a lower value inductor) results in a lower number of possible MDIV values that can be used.

In addition to providing a reference frequency for the SPLL, the REF_PLL circuit provides two outputs from the CMX940 device. MCLK_OUT is a logic level signal that is a divided version of the MCLK input with a divider range of 1-4, programmed by register REF_MCLK_DIV ($7D). The REF_LOOUT signal is a buffered version of the RVCO output with a divider range of 1-28 (restricted) and with adjustable output power level; this signal is programmed by the registers REF_LO_DIV ($7B) and REF_LO_BUF ($7C).The

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output level is lower with the output divider set to 1. Note that enabling this output may compromise the spurious performance of the main Synthesizer PLL output.

5.5 Synthesizer PLL

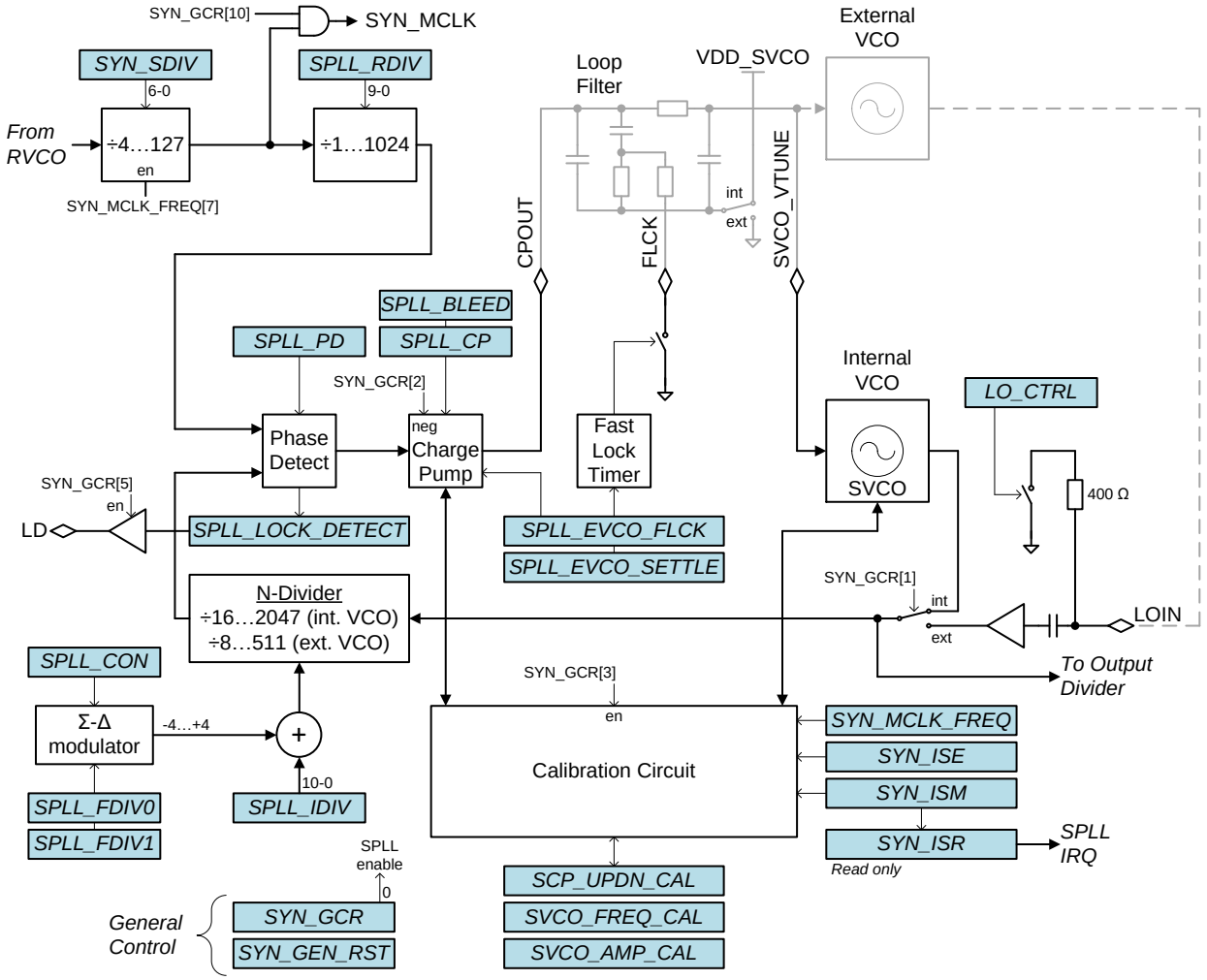

Figure 6 Synthesizer PLL

The Synthesizer PLL (SPLL), Figure 6, may be configured to operate with the integrated SVCO (which has a negative tuning slope) or alternatively an external VCO (with either a positive or negative tuning slope).

The internal SPLL clock signal SYN_MCLK must be enabled for all synthesizer functions. SYN_MCLK is obtained from the divided RVCO signal produced at the output of the Source Divider. The Source Divider may be programmed to divide between 4 and 127 by the SYN_SDIV ($4D) register. The maximum SYN_MCLK frequency is 120 MHz.

The SPLL contains a reference divider which integer divides SYN_MCLK to produce the SPLL comparison frequency. The maximum permitted comparison frequency is 120 MHz when using the internal SVCO or 50 MHz when using an external VCO. The SPLL reference divider may be programmed to divide between 1 and 1024 by the SPLL_RDIV ($6A) register.

The SPLL contains a fractional-N divider which may be configured to operate in either pure integer mode or 16/24-bit fractional-N mode using the SPLL_CON ($34) register. The full range of integer divider values is 16-2047 when using the internal VCO and 8-511 when using an external VCO. In fractional-N mode the allowed integer value range is reduced to 20-2043 and 12-507 respectively. The overall N divider value is programmed by the integer SPLL_IDIV ($39) and fractional SPLL_FDIV0 ($3A) and SPLL_FDIV1 ($3B) registers.

Linearisation of the SPLL charge-pump and phase-detector is controlled by the SPLL_BLEED ($35) and SPLL_PD ($37) registers respectively which enable the SPLL noise and spur performance to be optimised.

Flexible control of the SPLL bandwidth is achieved by the selection of the external loop-filter components and the charge-pump current which is controlled by the SPLL_CP ($36) register.

A digital lock detection function with programmable sensitivity and response time is configured by the SPLL_LOCK_DETECT ($3F) register. The locked or unlocked status may be indicated using dedicated interrupt status bits, output to the LD device pin or read from the SPLL_LOCK_DETECT_RD ($8F) register.

An integrated fast-lock function reduces the SPLL settling-time from start-up when operating with an external VCO by pre-charging the external loop filter via the FLCK device pin. The fast-lock function is controlled using the SPLL_EVCO_FLCK ($7E) register. The fast-lock function allows the allocated SPLL settling-time in the SPLL_EVCO_SETTLE ($71) register to be appropriately reduced.

Prior to using the SPLL it must be calibrated. This should be done after calibrating the REF_PLL system, and after configuring SYN_MCLK_FREQ ($2F), SYN_ISE ($31), SYN_ISM ($32) and the other SPLL divider and configuration registers. The calibration is performed automatically when bit 3 of the SPLL general control register SYN_GCR ($2E) is set. After calibration is complete, the calibration settings for that specific SPLL configuration get stored in the SCP_UPDN_CAL ($65), SVCO_FREQ_CAL ($53) and SVCO_AMP_CAL ($67) registers Note that in external VCO mode only the charge pump gets calibrated, so only the SCP_UPDN_CAL register gets updated. For frequency hopping applications, these registers can be read by and subsequently rewritten by the host µC to rapidly reinstate the calibration settings for a particular SPLL configuration without performing a time-consuming re-calibration operation.

5.6 Synthesizer Output Divider and Buffers

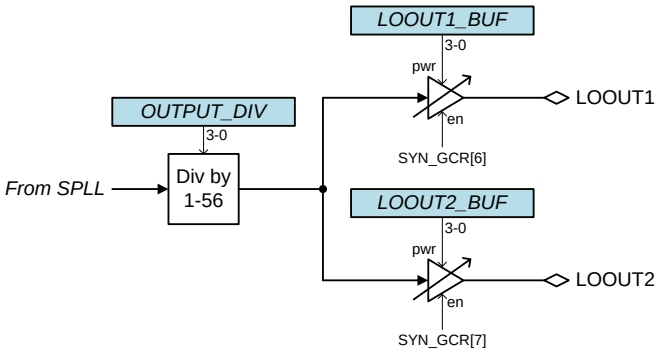

Figure 7 Synthesizer Output Divider and Buffers

The Output Divider divides the internal SVCO signal using specific integer values from 1-56 in the OUTPUT_DIV ($40) register. The divided SVCO signal is buffered by variable gain amplifiers and output to the LOOUT1 and LOOUT2 device pins. The output power of the two LO buffers may be independently varied by the LOOUT1_BUF ($41) and LOOUT2_BUF ($42) registers. The outputs are similar in terms of

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freqeuency response etc, however LOOUT1 has marginally lower spurious than LOOUT2 due to internal coupling effects.

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6 Registers

All register addresses are 8-bits wide. The registers are either write (W), read (R) or command (CMD) types. The write and read registers are 8 or 16 data bits wide. Command registers have no data bits. The device addresses are listed in Table 5.

Table 5 Device Registers

Name (Address)	Type	Description
Reference System Control		
REF_GCR ($75)	W8	Reference General Control Register
REF_MCLK_FREQ ($76)	W8	Reference MCLK Frequency
REF_ISE ($77)	W8	Reference Interrupt Status Enable
REF_ISM ($78)	W8	Reference Interrupt Status Mask
REF_GEN_RST ($79)	CMD	Reference General Reset
REF_GCR_RD ($C5)	R8	Reference General Control Read
REF_MCLK_FREQ_RD ($C6)	R8	Reference MCLK Frequency Read
REF_ISE_RD ($C7)	R8	Reference Interrupt Status Enable Read
REF_ISM_RD ($C8)	R8	Reference Interrupt Status Mask Read
REF_ISR_RD ($C9)	R8	Reference Interrupt Status Register Read
Reference PLL		
REF_PLL_MDIV ($7A)	W8	Reference PLL Main Divider Value
REF_PLL_MDIV_RD ($CA)	R8	Reference PLL Main Divider Value Read
Refererence Calibration		
REF_RVCO_BIAS_CAL ($09)	W8	Reference VCO Bias Calibration Code
REF_RVCO_FREQ_CAL ($0B)	W16	Reference VCO Frequency Calibration Code
REF_RVCO_AMP_CAL ($2C)	W8	Reference VCO Amplitude Calibration Code
REF_RVCO_BIAS_CAL_RD ($D9)	R8	Reference VCO Bias Calibration Code Read
REF_RVCO_FREQ_CAL_RD ($DB)	R16	Reference VCO Frequency Calibration Code Read
REF_RVCO_AMP_CAL_RD ($D6)	R8	Reference VCO Amplitude Calibration Code Read
Reference LO Divider and Buffer		
REF_LO_DIV ($7B)	W8	Reference LO Divider Value
REF_LO_BUF ($7C)	W8	Reference LO Buffer Power Control
REF_LO_DIV_RD ($CB)	R8	Reference LO Divider Value Read
REF_LO_BUF_RD ($CC)	R8	Reference LO Buffer Power Control Read
MCLK Divider		
REF_MCLK_DIV ($7D)	W8	Reference MCLK Divider Value
REF_MCLK_DIV_RD ($CD)	R8	Reference MCLK Divider Value Read
Synthesizer System Control		
SYN_GCR ($2E)	W16	Synthesizer General Control Register
SYN_MCLK_FREQ ($2F)	W8	Synthesizer Main Clock Frequency
SYN_GEN_RST ($30)	CMD	Synthesizer General Reset
SYN_ISE ($31)	W8	Synthesizer Interrupt Status Enable
SYN_ISM ($32)	W8	Synthesizer Interrupt Status Mask
SYN_SDIV ($4D)	W8	Synthesizer Source Divider Value
SYN_GCR_RD ($AE)	R16	Synthesizer General Control Read
SYN_MCLK_FREQ_RD ($AF)	R8	Synthesizer Main Clock Frequency Read
SYN_ISR_RD ($B0)	R8	Synthesizer Interrupt Status Register Read
SYN_ISE_RD ($B1)	R8	Synthesizer Interrupt Status Enable Read
SYN_ISM_RD ($B2)	R8	Synthesizer Interrupt Status Mask Read
SYN_SDIV_RD ($AD)	R8	Synthesizer Source Divider Value Read
Synthesizer PLL		
SPLL_CON ($34)	W8	SPLL Mode Control
SPLL_BLEED ($35)	W16	SPLL Bleed Current
SPLL_CP ($36)	W16	SPLL Charge Pump

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SPLL_PD ($37)	W8	SPLL Phase Detector
SPLL_IDIV ($39)	W16	SPLL Integer Divider Value
SPLL_FDIV0 ($3A)	W16	SPLL Fractional Divider Value (Least Significant Word)
SPLL_FDIV1 ($3B)	W8	SPLL Fractional Divider Value (Most Significant Byte)
SPLL_LOCK_DETECT ($3F)	W8	SPLL Lock Detection Control
SPLL_RDIV ($6A)	W16	SPLL Reference Divider Value
SPLL_CON_RD ($84)	R8	SPLL Mode Control Read
SPLL_EVCO_SETTLE ($71)	W8	SPLL External VCO Setting Time
SPLL_EVCO_FLCK ($7E)	W16	SPLL External VCO Fast Lock
SPLL_BLEED_RD ($85)	R16	SPLL Bleed Current Read
SPLL_CP_RD ($86)	R16	SPLL Charge Pump Read
SPLL_PD_RD ($87)	R8	SPLL Phase Detector Read
SPLL_IDIV_RD ($89)	R16	SPLL Integer Divider Value Read
SPLL_FDIV0_RD ($8A)	R16	SPLL Fractional Divider Value (Least Significant Word) Read
SPLL_FDIV1_RD ($8B)	R8	SPLL Fractional Divider Value (Most Significant Byte) Read
SPLL_LOCK_DETECT_RD ($8F)	R8	SPLL Lock Detection Control Read
SPLL_RDIV_RD ($BA)	R16	SPLL Reference Divider Value Read
SPLL_EVCO_SETTLE_RD ($F1)	R8	SPLL External VCO Settling Time Read
SPLL_EVCO_FLCK_RD ($FE)	R16	SPLL External VCO Fast Lock Read
Synthesizer Calibration		
SCP_UPDN_CAL ($65)	W8	Synthesizer Charge Pump Up-Down Calibration Code
SVCO_FREQ_CAL ($53)	W16	Synthesizer VCO Frequency Calibration Code
SVCO_AMP_CAL ($67)	W8	Synthesizer VCO Amplitude Calibration Code
SCP_UPDN_CAL_RD ($B5)	R8	Synthesizer Charge Pump Up-Down Calibration Code
SVCO_FREQ_CAL_RD ($93)	R16	Synthesizer VCO Frequency Calibration Code
SVCO_AMP_CAL_RD ($B7)	R8	Synthesizer VCO Amplitude Calibration Code
Synthesizer Output Divider and Buffers		
OUTPUT_DIV ($40)	W8	Output Divider Value
LOOUT1_BUF ($41)	W8	LO1 Output Buffer Power Control
LOOUT2_BUF ($42)	W8	LO2 Output Buffer Power Control
OUTPUT_DIV_RD ($C0)	R8	Output Divider Value Read
LOOUT1_BUF_RD ($C1)	R8	LO1 Output Buffer Power Control Read
LOOUT2_BUF_RD ($C2)	R8	LO2 Output Buffer Power Control Read
Synthesizer External LO		
LO_CTRL ($6F)	W8	LO Control
LO_CTRL_RD ($BF)	R8	LO Control Read

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6.1 Reference System Control

6.1.1 REF_GCR ($75)

Reference General Control Register
8-bit Write
Reset Value: $00

7	6	5	4	3	2	1	0
0		MCLK_ OUT	REF_ LOOUT	RVCO_ EN	CAL	RPLL	MCLK

MCLK_OUT	**MCLK Output (b5)**
0	Disabled
1	Enabled

REF_LOOUT	**Reference LO Output (b4)**
0	Disabled
1	Enabled -

RVCO_EN	**RVCO Enable (b3)**
0	Disabled
1	Enabled – required to feed the SPLL Source Divider.

CAL	**Reference PLL Calibration (b2)**
0	Disabled
1	Triggered – also requires REF_GCR bit 1 to be set to 1

The corresponding CAL bit in the REF_GCR_RD ($C5) register is cleared when calibration is complete. A calibration complete interrupt may be configured by setting the CAL bit in the REF_ISE ($77) register prior to initiating a calibration. Calibration of the RVCO bias, frequency and amplitude are performed.

RPLL	**Reference PLL Enable (b1)**
0	Disabled
1	Enabled – also requires MCLK (b0) to be set to 1

MCLK	**MCLK Enable (b0)**
0	Disabled
1	Enabled - MCLK is required for all functions

C-BUS write and read capability is unaffected by the MCLK state.

If the MCLK_READY bit in the REF_ISE ($77) register is set, an MCLK_READY interrupt will be observed in the REF_ISR_RD ($C9) register.

6.1.2 REF_MCLK_FREQ ($76)

Reference Main Clock Frequency
8-bit Write
Reset value: $26

7	6	5	4	3	2	1	0
0		FREQ					

FREQ	**MCLK Frequency (b5-b0)**
0-9	Invalid
10-40	10-40 MHz
41-63	Invalid

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Set FREQ to the MCLK frequency in MHz rounded to the nearest integer. This register must not be modified if MCLK is active. The default setting of $26 (38 decimal) is suitable for a 38.4MHz oscillator.

6.1.3 REF_ISE ($77)

Reference Interrupt Status Enable
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0					CAL	RECAL	MCLK_ READY

If an Interrupt Status Enable register bit is set to 1 then the corresponding interrupt event will be stored in the REF_ISR_RD ($C9) register. When an interrupt bit in the REF_ISR_RD ($C9) register is set to 1, the corresponding ISE bit is automatically cleared to 0.

Name	Bit	Description
CAL	2	Enable REF_PLL calibration complete interrupt
RECAL	1	Enable REF_PLL re-calibration interrupt
MCLK_READY	0	Enable MCLK ready interrupt

6.1.4 REF_ISM ($78)

Reference Interrupt Status Mask
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0					CAL	RECAL	MCLK_ READY

If an Interrupt Status Mask register bit is set to 1 and the corresponding interrupt bit in the SYN_ISR_RD ($B0) register is set to 1 then the IRQN pin will be driven low.

Name	Bit	Description
CAL	2	REF_PLL calibration complete
RECAL	1	REF_PLL requires re-calibration
MCLK_READY	0	MCLK ready - indicates that MCLK buffer has powered up and stabilised

6.1.5 REF_GEN_RST ($79)

Reference General Reset
8-bit Command
This C-BUS command resets the device and sets all bits of Reference registers to their default state.

6.1.6 REF_GCR_RD ($C5)

Reference General Control Register Read
8-bit Read
This register reads the value of REF_GCR ($75).

6.1.7 REF_MCLK_FREQ_RD ($C6)

Reference Main Clock Frequency Read
8-bit Read
This register reads the value of REF_MCLK_FREQ ($76).

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6.1.8 REF_ISE_RD ($C7)

Reference Interrupt Status Enable Read
8-bit Read
This register reads the value of REF_ISE ($77).

6.1.9 REF_ISM_RD ($C8)

Reference Interrupt Status Mask Read
8-bit Read
This register reads the value of REF_ISM ($78).

6.1.10 REF_ISR_RD ($C9)

Reference Interrupt Status Register Read
8-bit Read

7	6	5	4	3	2	1	0
0					CAL	RECAL	MCLK_ READY

The register is automatically cleared to 0 when read.

Name	Bit	Description
CAL	2	REF_PLL calibration complete
RECAL	1	REF_PLL requires re-calibration
MCLK_READY	0	MCLK is ready

6.2 Reference PLL

6.2.1 REF_PLL_MDIV ($7A)

Reference PLL Main Divider Value
8-bit Write
Reset value: $1F

7	6	5	4	3	2	1	0
0	MDIV						

MDIV	Reference PLL Main Divider Value (b6-b0)
0-3	Invalid
4-127	4-127

6.2.2 REF_PLL_MDIV_RD ($CA)

Reference PLL Main Divider Value Read
8-bit Read
This register reads the value of REF_PLL_MDIV ($7A).

6.3 Reference Calibration

6.3.1 REF_RVCO_BIAS_CAL ($09)

RVCO Bias Calibration Code
8-bit Write
Reset value: $10

7	6	5	4	3	2	1	0
0			BIAS				

BIAS **Reference VCO Bias Calibration Code Setting (b4-b0)**
0-31 Writing to this register sets the RVCO bias calibration code - may be written prior to starting MCLK or after MCLK_READY observed in REF_ISR_RD ($C9) register.

6.3.2 REF_RVCO_FREQ_CAL ($0B)

RVCO Frequency Calibration Code
16-bit Write
Reset value: $0102

15	14	13	12	11	10	9	8
TIMEOUT (R)	0						FREQ[8]
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FREQ[7:0]							

TIMEOUT **Calibration Error Timeout - Read Only (b15)**
0 Frequency calibration did not timeout.
1 Frequency calibration timeout error. The RPLL_RECAL interrupt status bit is also set if the interrupt is enabled. The TIMEOUT status bit is cleared down at the start of the next calibration or if this register is written.

FREQ **Reference VCO Frequency Calibration Code (b8-b0)**
0-511 Writing to this register sets the RVCO frequency calibration code - may be written prior to starting MCLK or after MCLK_READY observed in REF_ISR_RD ($C9) register.

6.3.3 REF_RVCO_AMP_CAL ($2C)

RVCO Amplitude Calibration Code
8-bit Write
Reset value: $20

7	6	5	4	3	2	1	0
0		AMP					

AMP **Reference VCO Amplitude Calibration Code Setting (b5-b0)**
0-63 Writing to this register sets the RVCO amplitude calibration code - may be written prior to starting MCLK or after MCLK_READY observed in REF_ISR_RD ($C9) register

6.3.4 REF_RVCO_BIAS_CAL_RD ($D9)

RVCO Bias Calibration Code Read
8-bit Read
This register is updated following a write to REF_RVCO_BIAS_CAL ($09) or during calibration and will be valid after CAL is observed in the REF_ISR_RD ($C9) register.

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6.3.5 REF_RVCO_FREQ_CAL_RD ($DB)

RVCO Frequency Calibration Code Read
16-bit Read
This register is updated following a write to REF_RVCO_FREQ_CAL ($0B) or during calibration and will be valid after CAL is observed in the REF_ISR_RD ($C9) register.

6.3.6 REF_RVCO_AMP_CAL_RD ($D6)

RVCO Amplitude Calibration Code Read
8-bit Read
This register is updated following a write to REF_RVCO_AMP_CAL ($2C) or during calibration and will be valid after CAL is observed in the REF_ISR_RD ($C9) register.

6.4 Reference LO Divider and Buffer

6.4.1 REF_LO_DIV ($7B)

Reference LO Divider Value
8-bit Write
Reset value: $03

7	6	5	4	3	2	1	0
0			RESERVED	ODIV			

RESERVED **Reserved – always write 0 (b4)**

ODIV	**Output Divider Ratio (b3-b0)**
0	1 (used only for debug purposes and results in reduced output power)
1-14	2-28 in steps of 2
15	3

The selected output divider value must not yield an output frequency less than 37.5MHz which is the minimum operating frequency limit of the Reference LO output buffer.

6.4.2 REF_LO_BUF ($7C)

Reference LO Buffer Power Control
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0				PWR_CTRL			

PWR_CTRL	**Output Power (b3-b0)**
0	-17 dBm
1	-14 dBm
2	-13 dBm
3	-12 dBm
4	-11 dBm
5	-9.7 dBm
6	-6.5 dBm
7	-4.8 dBm
8	-1.9 dBm
9	-0.4 dBm
10	+1.3 dBm
11	+2.0 dBm

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12	+3.0 dBm
13-15	Invalid

6.4.3 REF_LO_DIV_RD ($CB)

Reference LO Divider Value Read
8-bit Read
This register reads the value of REF_LO_BUF ($7C).

6.4.4 REF_LO_BUF_RD ($CC)

Reference LO Buffer Power Control Read
8-bit Read
This register reads the value of REF_LO_BUF ($7C).

6.5 Reference MCLK Divider

6.5.1 REF_MCLK_DIV ($7D)

Reference MCLK Divider Value
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0						RDIV	

RDIV	Divide Ratio (b1-b0)
0	Divide by 1
1	Divide by 2
2	Divide by 3
3	Divide by 4

This divider is used to provide a divided version of the reference master clock to MCLK_OUT (pin 48) for use in other parts of a transceiver system design (e.g. a modem clock). It is recommended to configure the MCLK Divider prior to setting the MCLK_OUT bit in the REF_GCR ($75) register.

6.5.2 REF_MCLK_DIV_RD ($CD)

Reference MCLK Divider Value Read
8-bit Read
This register reads the value of REF_MCLK_DIV ($7D).

6.6 Synthesizer System Control

6.6.1 SYN_GCR ($2E)

Synthesizer General Control Register
16-bit Write
Reset Value: $0000

15	14	13	12	11	10	9	8
0					SYN_ MCLK	0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LO2_ OUTPUT	LO1_ OUTPUT	LOCK_ DETECT	0	SPLL_CAL	SPLL_ EVCO_INV	SPLL_ EVCO	SPLL

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0 **Reserved (b15-b11)**

SYN_MCLK **SYN_MCLK Enable (b10)**
0 Disabled
1 Enabled - SYN_MCLK is required for all synthesizer functions

C-BUS write and read capability is unaffected by the SYN_MCLK state.

If the SYN_MCLK_READY bit in the SYN_ISE ($31) register is set, a SYN_MCLK_READY interrupt will be observed in the SYN_ISR_RD ($B0) register.

LO2_OUTPUT **LO2 Output (b7)**
0 Disabled
1 Enabled

LO1_OUTPUT **LO1 Output (b6)**
0 Disabled
1 Enabled

LOCK_DETECT **Lock Detection (b5)**
0 Disabled
1 Enabled

SPLL_CAL **Synthesizer PLL Calibration (b3)**
0 Disabled
1 Triggered – also requires SPLL (b0) to be set to 1

The corresponding SPLL_CAL bit in the SYN_GCR_RD ($AE) register is cleared when calibration is complete. A calibration complete interrupt may be configured by setting the SPLL_CAL bit in the SYN_ISE ($31) register prior to initiating a calibration.

With an external VCO (SPLL_EXT_VCO b1=1) calibration of the SPLL charge pump is performed. With an internal VCO (SPLL_EXT_VCO b1=0) calibration of the SPLL charge pump, internal VCO frequency and amplitude are performed.

SPLL_EVCO_INV **Synthesizer PLL External VCO Control Characteristic (b2)**
0 External VCO positive gain
1 External VCO negative gain

SPLL_EVCO **Synthesizer PLL External VCO Select (b1)**
0 SPLL Internal VCO
1 SPLL External VCO (input on LOIN pin)

SPLL **Synthesizer PLL Enable (b0)**
0 Disabled
1 Enabled. Also enables internal SVCO unless SPLL_EVCO (b1) = 1

6.6.2 SYN_MCLK_FREQ ($2F)

Synthesizer Main Clock Frequency
8-bit Write
Reset value: $26

7	6	5	4	3	2	1	0
SRC	FREQ						

SRC	**Source Divider Enable (b7)**
0	Source Divider Disabled
1	Source Divider Enabled

FREQ	**SYN_MCLK Frequency (b6-b0)**
0-9	Invalid
10-120	10-120 MHz
121-127	Invalid

Set FREQ to the output frequency of the Source Divider in MHz rounded to the nearest integer. This register must not be modified if SYN_MCLK is active.

6.6.3 SYN_GEN_RST ($30)

Synthesizer General Reset
8-bit Command
This C-BUS command resets the device and sets all bits of Synthesizer registers to their default state.

6.6.4 SYN_ISE ($31)

Synthesizer Interrupt Status Enable
8-bit Write
Reset value: $40

7	6	5	4	3	2	1	0
0	SYN_MCLK _READY	SPLL_ CAL	0	SPLL_ OUTLOCK	SPLL_ INLOCK	SPLL_ RECAL	0

If an Interrupt Status Enable register bit is set to 1 then the corresponding interrupt event will be stored in the SYN_ISR_RD ($B0) register. When an interrupt bit in the SYN_ISR_RD ($B0) register is set to 1, the corresponding ISE bit is automatically cleared to 0.

Name	**Bit**	**Description**
SYN_MCLK_READY	6	Enable SYN_MCLK ready interrupt
SPLL_CAL	5	SPLL calibration complete
SPLL_OUTLOCK	3	Enable SPLL out of lock interrupt
SPLL_INLOCK	2	Enable SPLL in lock interrupt
SPLL_RECAL	1	Enable SPLL re-calibration interrupt

6.6.5 SYN_ISM ($32)

Synthesizer Interrupt Status Mask
8-bit Write
Reset value: $40

7	6	5	4	3	2	1	0
0	SYN_MCLK _READY	SPLL_ CAL	0	SPLL_ OUTLOCK	SPLL_ INLOCK	SPLL_ RECAL	0

If an Interrupt Status Mask register bit is set to 1 and the corresponding interrupt bit in the SYN_ISR_RD ($B0) register is set to 1 then the IRQN pin will be driven low.

Name	**Bit**	**Description**
SYN_MCLK_READY	6	SYN_MCLK ready
SPLL_CAL	5	SPLL calibration complete
SPLL_OUTLOCK	3	SPLL out of lock
SPLL_INLOCK	2	SPLL in lock
SPLL_RECAL	1	SPLL requires re-calibration

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6.6.6 SYN_SDIV ($4D)

Synthesizer Source Divider Value
8-bit Write
Reset value: $08

7	6	5	4	3	2	1	0
0	SDIV						

SDIV	Synthesizer Source Divider Value (b6-b0)
0-3	Invalid
4-127	4-127

6.6.7 SYN_GCR_RD ($AE)

Synthesizer General Control Register Read
16-bit Read
This register reads the value of SYN_GCR ($2E).

6.6.8 SYN_MCLK_FREQ_RD ($AF)

Synthesizer Main Clock Frequency Read
8-bit Read
This register reads the value of SYN_MCLK_FREQ ($2F).

6.6.9 SYN_ISR_RD ($B0)

Synthesizer Interrupt Status Register Read
8-bit Read

7	6	5	4	3	2	1	0
0	SYN_MCLK _READY	SPLL_ CAL	0	SPLL_ OUTLOCK	SPLL_ INLOCK	SPLL_ RECAL	0

The register is automatically cleared to 0 when read.

Name	Bit	Description
SYN_MCLK_READY	6	SYN_MCLK is ready
SPLL_CAL	5	SPLL calibration complete
SPLL_OUTLOCK	3	SPLL is out of lock
SPLL_INLOCK	2	SPLL is in lock
SPLL_RECAL	1	SPLL requires re-calibration

6.6.10 SYN_ISE_RD ($B1)

Synthesizer Interrupt Status Enable Read
8-bit Read
This register reads the value of SYN_ISE ($31).

6.6.11 SYN_ISM_RD ($B2)

Synthesizer Interrupt Status Mask Read
8-bit Read
This register reads the value of SYN_ISM ($32).

6.6.12 SYN_SDIV_RD ($AD)

Synthesizer Source Divider Value Read
8-bit Read
This register reads the value of SYN_SDIV ($4D).

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6.7 Synthesizer PLL

6.7.1 SPLL_CON ($34)

SPLL Control
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0		RESERVED	RES	0	MODE		

RESERVED **Reserved – always write 0 (b5)**

RES **Resolution (b4)**
0 24-bit fraction (SPLL_FDIV1 and SPLL_FDIV0 determine fractional value)
1 16-bit fraction (SPLL_FDIV0 determines fractional value)

MODE **PLL Division Mode (b2-b0)**
0 Integer-N mode
2 Fractional-N mode
All other modes are reserved

If MODE is modified, the register SPLL_FDIV0 ($3A) must be subsequently re-written for the fractional value to take effect.

6.7.2 SPLL_BLEED ($35)

SPLL Bleed Current
16-bit Write
Reset value: $0200

15	14	13	12	11	10	9	8
EN	0					BIAS	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GAIN		SET					

EN **Bleed Current Enable (b15)**
0 Bleed current disabled
1 Bleed current enabled

BIAS **Bleed Bias Current (b9-b8)**
0 50 µA - lowest bleed current signal-to-noise ratio
1 100 µA
2 200 µA
3 400 µA - highest bleed current signal-to-noise ratio

GAIN **Bleed Current Gain (b7-b6)**
0 1
1 0.5
2 0.25
3 0.125

SET **Bleed Set Current (b5-b0)**
0-63 12.5-800 µA in 12.5 µA steps

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The applied bleed current is given by:

$$I_{BLEED} = 0.5^{GAIN} \times (SET + 1) \times 12.5\mu A$$

For example, with GAIN=1 and SET=8,

$$I_{BLEED} = 0.5^{1} \times (8 + 1) \times 12.5\mu A = 56.25\mu A$$

6.7.3 SPLL_CP ($36)

SPLL Charge Pump
16-bit Write
Reset value: $0400

15	14	13	12	11	10	9	8
0					BIAS		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GAIN		CPI					

BIAS	**Charge Pump Bias Current (b10-b8)**
0	50 µA – lowest charge pump current signal-to-noise ratio
1	100 µA
2	200 µA
3	400 µA
4	800 µA
5	1600 µA - highest charge pump current signal-to-noise ratio
6-7	Invalid – do not use

GAIN	**Charge Pump Current Gain (b7-b6)**
0	1
1	0.5
2	0.25
3	0.125

CPI	**Charge Pump Current (b5-b0)**
0-47	50-2400 µA in 50 µA steps
48-63	Invalid – do not use

The applied charge pump current is given by:

$$I_{CP} = 0.5^{GAIN} \times (CPI + 1) \times 50\mu A$$

For example, with GAIN=2 and CPI=6,

$$I_{CP} = 0.5^{2} \times (6 + 1) \times 50\mu A = 87.5\mu A$$

6.7.4 SPLL_PD ($37)

SPLL Phase Detector
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0					PD_PULSE_WIDTH		

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PD_PULSE_WIDTH	Synthesizer PLL Minimum Pulse Width (b2-b0)
0	0.93 ns
1	1.33 ns
2	1.56 ns
3	1.90 ns
4	1.96 ns
5	2.16 ns
6	2.28 ns
7	2.48 ns

6.7.5 SPLL_IDIV ($39)

SPLL Integer Divider Value
16-bit Write
Reset value: $0040

15	14	13	12	11	10	9	8
0					IDIV[10:8]		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IDIV[7:0]							

IDIV	Synthesizer PLL Main Divider Integer Value (b10-b0)
0-7	Invalid – do not use
8-2047	Divide by 8-2047 in integer steps

These bits represent the integer portion closest to the desired fractional-N divider value. The integer value is combined with the fractional value from registers SPLL_FDIV0 ($3A) and SPLL_FDIV1 ($3B) to select the desired VCO frequency.

In integer-N mode, SPLL_CON ($34) b2-b0=0, the SPLL_FDIV0 ($3A) and SPLL_FDIV1 ($3B) registers are ignored, and the minimum/maximum IDIV value is 16/2047 for the internal SVCO and 8/511 for an external VCO. In integer-N mode, the N-divider value is loaded after writing to SPLL_IDIV ($39).

In fractional-N mode, SPLL_CON ($34) b2-b0=2, the minimum/maximum IDIV value is 20/2043 for the internal SVCO and 12/507 for an external VCO. In fractional-N mode, the N-divider value is loaded after writing to SPLL_FDIV0 ($3A).

6.7.6 SPLL_FDIV0 ($3A)

SPLL Fractional Divider Value (Least Significant Word)
16-bit Write
Reset value: $0000

15	14	13	12	11	10	9	8
FDIV[15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FDIV[7:0]							

FDIV[15:0] **Synthesizer PLL Main Divider Fractional Value LS Word (b15-b0)**

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6.7.7 SPLL_FDIV1 ($3B)

SPLL Fractional Divider Value (Most Significant Byte)
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
FDIV[23:16]							

FDIV[23:16] Synthesizer PLL Main Divider Fractional Value MS Byte (b7-b0)

The fractional divide value resolution is determined by the RES bit (b4) in the SPLL_CON ($34) register.

Table 6 Fractional Divider Control

SPLL_CON RES (b4)	FDIV Bits	FDIV Divisor	Fractional Range
0	24	2^{24}	-0.5 to +0.499 999 94
1	16	2^{16}	-0.5 to +0.499 984 74

With fractional resolution set to 24-bits, the SPLL_FDIV0 ($3A) and SPLL_FDIV1 ($3B) registers are concatenated to form a 24-bit two's complement number FDIV[23:0]. The fractional divide value is equal to FDIV/2^{24}.

With fractional resolution set to 16 bits, the SPLL_FDIV1 ($3B) register is ignored and the SPLL_FDIV0 ($3A) register is treated as a 16-bit two's complement number FDIV[15:0]. The fractional divide value is equal to FDIV/2^{16}.

The SPLL_FDIV0 ($3A) and SPLL_FDIV1 ($3B) registers may be reconfigured during SPLL operation. Note, following a write to SPLL_FDIV0 ($3A), the fractional-N modulator is automatically reset with the initial conditions required to minimise structural tone generation.

6.7.8 SPLL_LOCK_DETECT ($3F)

SPLL Lock Detection Control
8-bit (Write)
Reset value: $0B

7	6	5	4	3	2	1	0
LD (R)	0	LD_OE	TOL		PERIOD		

LD **Lock Detect Status (b7) – Read Only, see SPLL_LOCK_DETECT_RD**
0 Unlocked
1 Locked

LD_OE **Lock Detect Output Enable (b5)**
0 Disabled
1 Enabled - Lock Detect Status output on LD pin

TOL **Lock Detect Count Tolerance (b4-b3)**
0 1
1 2 (default)
2 3
3 4

PERIOD	Lock Detect Count Periods of Reference Clock (b2-b0)
0	100
1	250
2	500
3	1000 (default)
4	2500
5	5000
6	10 000
7	15 000

Note, it is recommended to configure TOL and PERIOD prior to enabling LOCK_DETECT in the SYN_GCR ($2E) register.

6.7.9 SPLL_RDIV ($6A)

SPLL Reference Divider Value
16-bit Write
Reset value: $0001

15	14	13	12	11	10	9	8
0						RDIV[9:8]	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDIV[7:0]							

RDIV	SPLL Reference Divider Value (b9-b0)
0	1024
1-1023	1-1023

The SPLL reference divider divides the reference source frequency to produce the comparison frequency. The maximum permitted comparison frequency is 120MHz when using the internal SVCO and 50MHz when using an external VCO.

6.7.10 SPLL_EVCO_SETTLE ($71)

SPLL External VCO Settling Time
8-bit Write
Reset value: $7D

7	6	5	4	3	2	1	0
TIME							

TIME	Settling Time (b7-b0)
0	8192 µs
1-255	32-8160 µs in 32 µs steps

The time allowed for the Synthesizer PLL to settle on start-up with an external VCO is determined by the PLL loop-bandwidth and the fast lock function. This register should be configured prior to enabling the SPLL with an external VCO in the SYN_GCR ($2E) register.

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6.7.11 SPLL_EVCO_FLCK ($7E)

SPLL External VCO Fast Lock
16-bit Write
Reset value: $0000

15	14	13	12	11	10	9	8
FLCK (R)	EN	FLCK_CPI					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PERIOD							

FLCK **Fast Lock Status – Read Only (b15)**
0 Fast lock inactive – FLCK pin is high-impedance
1 Fast lock active – FLCK pin is ground

EN **Fast Lock Enable (b14)**
0 Fast lock disabled
1 Fast lock enabled

FLCK_CPI **Fast Lock Charge Pump Current (b13-b8)**
0-47 50-2400 µA in 50 µA steps
48-63 Invalid – do not use

PERIOD **Fast Lock Period (b7-b0)**
0 8192 µs
1-255 32-8160 µs in 32 µs steps

Fast lock is used to reduce the settling time of the SPLL with an external VCO by a factor of approximately √M, where M is the ratio between the fast lock charge-pump current and the normal charge-pump current. In practice, an even greater reduction is often achieved because fast lock may reduce or eliminate “cycle slippage” in the SPLL phase-detector.

If enabled (b14 = 1), fast lock will be activated on SPLL start-up or each time the SPLL divider settings are updated. While fast lock is active, the associated FLCK pin is pulled to ground and the fast lock charge-pump current (b13-b8) is applied for the duration of the fast lock period (b7-b0). After the fast lock period, the FLCK pin returns to a high-impedance state and the charge-pump current reverts to the normal charge-pump current determined by GAIN and CPI in SPLL_CP ($36).

For example, with FLCK_CPI=11 (600 µA) and SPLL_CP ($36) settings of GAIN=2 (0.25) and CPI=2 (150 µA), the CPI multiplier ratio is:

$$M = \frac{600}{0.25 \times 150} = 16$$

To maintain loop stability with fast lock active for a chosen CPI multiplier ratio ‘M’, the resistor R13 shown in Figure 4 will typically need to be set to the following value:

$$R13 \approx \frac{\mathrm{R12}}{\sqrt{\mathrm{M}} - 1}$$

With fast lock enabled, SPLL_EVCO_SETTLE ($71) may be reduced accordingly to no less than the fast lock period.

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6.7.12 SPLL_CON_RD ($84)
SPLL Control Read
8-bit Read
This register reads the value of SPLL_CON ($34).

6.7.13 SPLL_BLEED_RD ($85)
SPLL Bleed Current Read
16-bit Read
This register reads the value of SPLL_BLEED ($35).

6.7.14 SPLL_CP_RD ($86)
SPLL Charge Pump Read
16-bit Read
This register reads the value of SPLL_CP ($36).

6.7.15 SPLL_PD_RD ($87)
SPLL Phase Detector Read
8-bit Read

This register reads the value of SPLL_PD ($37).

6.7.16 SPLL_IDIV_RD ($89)
SPLL Integer Divider Value Read
16-bit Read
This register reads the value of SPLL_IDIV ($39).

6.7.17 SPLL_FDIV0_RD ($8A)
SPLL Fractional Divider Value (Least Significant Word) Read
16-bit Read
This register reads the value of SPLL_FDIV0 ($3A).

6.7.18 SPLL_FDIV1_RD ($8B)
SPLL Fractional Divider Value (Most Significant Byte) Read
8-bit Read
This register reads the value of SPLL_FDIV1 ($3B).

6.7.19 SPLL_LOCK_DETECT_RD ($8F)
SPLL Lock Detection Control Read
8-bit Read
This register reads the value of SPLL_LOCK_DETECT ($3F).

6.7.20 SPLL_RDIV_RD ($BA)
SPLL Reference Divider Value Read
16-bit Read
This register reads the value of SPLL_RDIV ($6A).

6.7.21 SPLL_EVCO_SETTLE_RD ($F1)
SPLL External VCO Settling Time Read
8-bit Read
This register reads the value of SPLL_EVCO_SETTLE ($71).

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6.7.22 SPLL_EVCO_FLCK_RD ($FE)

SPLL External VCO Fast Lock Read
16-bit Read
This register reads the value of SPLL_EVCO_FLCK ($7E).

6.8 Synthesizer Calibration

6.8.1 SCP_UPDN_CAL ($65)

Synthesizer Charge Pump Up-Down Calibration Code
8-bit Write
Reset value: $40

7	6	5	4	3	2	1	0
0	UPDN						

UPDN **SPLL Charge Pump Up/Down Current Calibration Code (b6-b0)**
0-127 Writing to this register sets the SCP up/down current calibration code - may be written prior to starting MCLK or after MCLK_READY observed in SYN_ISR_RD ($B0) register.

6.8.2 SVCO_FREQ_CAL ($53)

Synthesizer VCO Frequency Calibration Code
16-bit Write
Reset value: $0102

15	14	13	12	11	10	9	8
VCOSEL	CALSEL	TIMEOUT (R)	0				FREQ[8]
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FREQ[7:0]							

VCOSEL **Synthesizer VCO Select (b15)**
0 Low frequency band SVCO.
1 High frequency band SVCO.

CALSEL **Synthesizer VCO Calibration Select (b14)**
0 Automatically select the low or high frequency band SVCO during calibration.
1 Calibrate only the selected SVCO (see b15 - VCOSEL).

TIMEOUT **Calibration Error Timeout - Read Only (b13)**
0 Frequency calibration did not timeout.
1 Frequency calibration timeout error. The SPLL_RECAL interrupt status bit is also set if the interrupt is enabled. The TIMEOUT status bit is cleared down at the start of the next calibration or if this register is written.

FREQ **Synthesizer VCO Frequency Calibration Code (b8-b0)**
0-511 Writing to this register sets the SVCO frequency calibration code.

This register may be written prior to starting MCLK or after MCLK_READY observed in ISR_RD ($B0) register.

6.8.3 SVCO_AMP_CAL ($67)

Synthesizer VCO Amplitude Calibration Code
8-bit Write
Reset value: $40

7	6	5	4	3	2	1	0
0	AMP						

AMP **Synthesizer VCO Amplitude Calibration Code Setting (b6-b0)**
0-127 Writing to this register sets the SVCO amplitude calibration code - may be written prior to starting MCLK or after MCLK_READY observed in SYN_ISR_RD ($B0) register.

6.8.4 SCP_UPDN_CAL_RD ($B5)

Synthesizer Charge Pump Up-Down Calibration Code Read
8-bit Read
This register is updated following a write to SCP_UPDN_CAL ($65) or during calibration and will be valid after SPLL_CAL is observed in the SYN_ISR_RD ($B0) register.

6.8.5 SVCO_FREQ_CAL_RD ($93)

Synthesizer VCO Frequency Calibration Code Read
16-bit Read
This register is updated following a write to SVCO_FREQ_CAL ($53) or during calibration and will be valid after SPLL_CAL is observed in the SYN_ISR_RD ($B0) register.

6.8.6 SVCO_AMP_CAL_RD ($B7)

Synthesizer VCO Amplitude Calibration Code Read
8-bit Read
This register is updated following a write to SVCO_AMP_CAL ($67) or during calibration and will be valid after SPLL_CAL is observed in the SYN_ISR_RD ($B0) register.

6.9 Synthesizer Output Divider and Buffers

6.9.1 OUTPUT_DIV ($40)

Output Divider Value
8-bit Write
Reset value: $03

7	6	5	4	3	2	1	0
0			RESERVED	ODIV			

RESERVED **Reserved – always write 0 (b4)**

ODIV	**Output Divider Ratio (b3-b0)**
0	1 (used only for debug purposes and results in significantly reduced output power)
1	2
2	3
3	4
4	6
5	8
6	12
7	16
8	20
9	28
10	40
11-15	56

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6.9.2 LOOUT1_BUF ($41)

LO1 Output Buffer Power Control
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0				LO1_PWR_CTRL			

LO1_PWR_CTRL	Nominal Power[1]
0	-17 dBm
1	-14 dBm
2	-13 dBm
3	-12 dBm
4	-11 dBm
5	-9.7 dBm
6	-6.5 dBm
7	-4.8 dBm
8	-1.9 dBm
9	-0.4 dBm
10	+1.3 dBm
11	+2.0 dBm
12	+3.0 dBm
13-15	Invalid

6.9.3 LOOUT2_BUF ($42)

LO2 Output Buffer Power Control
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0				LO2_PWR_CTRL			

LO2_PWR_CTRL	Nominal Power[1]
0	-17 dBm
1	-14 dBm
2	-13 dBm
3	-12 dBm
4	-11 dBm
5	-9.7 dBm
6	-6.5 dBm
7	-4.8 dBm
8	-1.9 dBm
9	-0.4 dBm
10	+1.3 dBm
11	+2.0 dBm
12	+3.0 dBm
13-15	Invalid

[1] The stated nominal output power shows typical values at 500 MHz (see parametric information in section 8.1.3). This will vary with output frequency.

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6.9.4 OUTPUT_DIV_RD ($C0)

Output Divider Value Read
8-bit Read
This register reads the value of OUTPUT_DIV ($40).

6.9.5 LOOUT1_BUF_RD ($C1)

LO1 Output Buffer Power Control Read
8-bit Read
This register reads the value of LOOUT1_BUF ($41).

6.9.6 LOOUT2_BUF_RD ($C2)

LO2 Output Buffer Power Control Read
8-bit Read
This register reads the value of LOOUT2LOOUT2_BUF ($42).

6.10 Synthesizer External LO

6.10.1 LO_CTRL ($6F)

LO Control
8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
0							TERM

TERM	External LO Input Buffer Resistive Termination (b0)
0	None (high impedance)
1	400 Ω – may be used to aid matching for the external LO where a broadband termination is not used

6.10.2 LO_CTRL_RD ($BF)

LO Control Read
8-bit Read
This register reads the value of LO_CTRL ($6F).

7 Application Notes

7.1 Application Programming Examples

7.1.1 Example 1 - Internal SVCO Operation

In this example, a 2 GHz signal is required to be output on the LOOUT1 pin at maximum power.

The device will be configured to synthesise a 4 GHz frequency from the SPLL using the internal SVCO and a low-noise reference frequency of 120 MHz. To obtain a 120 MHz low-noise reference frequency, the REF_PLL will be configured to generate a 960 MHz from a 38.4 MHz external MCLK oscillator. The 960 MHz RVCO frequency will then be divided by 8 to provide a 120 MHz reference frequency for the SPLL.

To guard against spurious emissions, it is necessary to ensure that the device raises an interrupt if the SPLL goes out of lock. It is also required to confirm that the SPLL has locked.

The calibration of the REF_PLL and SPLL should always be performed if the device is enabled from cold. In this application example, the device will be used for an extensive period. In order to obtain the lowest phase noise performance, the device must be recalibrated if required as indicated by the recalibration interrupts. The required device configuration is shown in Figure 8.

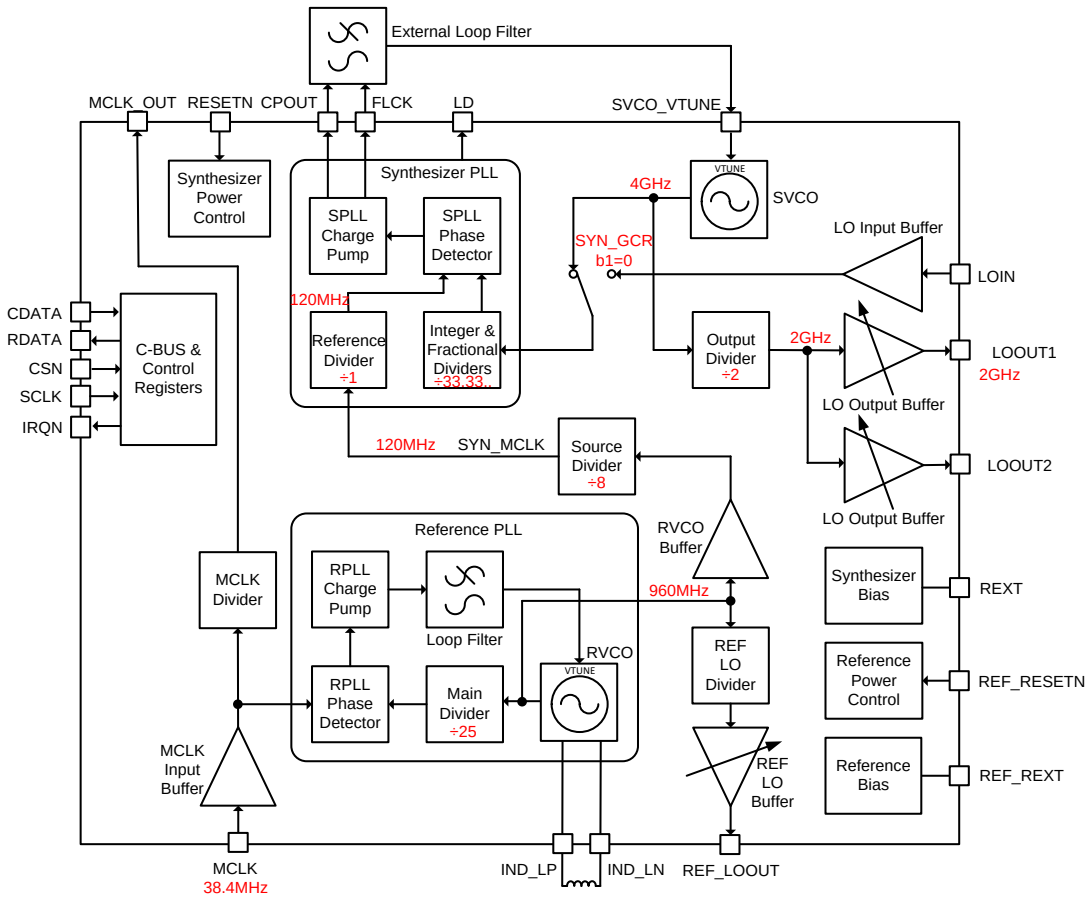

Figure 8 SPLL with Internal SVCO

It is recommended to configure the device prior to activating the writing to the REF_GCR ($75) and SYN_GCR ($2E) registers to activate the various RF blocks. It is first recommended to configure and enable the Reference system before the Synthesizer system. The recommended sequence of C-BUS writes to configure and enable the Reference PLL is shown in Table 7

Table 7 C-BUS Writes to Reference Registers (Example 1)

Register (Address)	Write Data	Notes
REF_MCLK_FREQ ($76)	$26	MCLK frequency set to 38 decimal (integer nearest 38.4).
REF_PLL_MDIV ($7A)	$19	Set REF_PLL integer divider to 960MHz/38.4MHz = 25.
REF_ISE ($77)	$07	Enable all interrupt sources to indicate MCLK_READY, REF_PLL calibration completion and REF_PLL recalibration indicator.
REF_ISM ($78)	$07	Drive IRQN pin low if an interrupt is triggered.
REF_GCR ($75)	$0F	Enable all reference functions.

The expected sequence of interrupt status values read from the REF_ISR_RD ($C9) register in response to the IRQN pin going low is shown in Table 8.

Table 8 Expected Reference Interrupt Status Sequence (Example 1)

Register (Address)	Read Data	Notes
REF_ISR_RD ($C9)	$01	MCLK ready
REF_ISR_RD ($C9)	$04	Calibration complete.

REF_ISR_RD ($C9) register bit1 (RECAL) may be triggered in response to extreme voltage and temperature changes.

Following the calibration complete indication of the Reference PLL, the recommended sequence of C-BUS writes to configure and enable the Synthesizer system is shown in Table 9.

Table 9 C-BUS Writes to Synthesizer Registers (Example 1)

Register (Address)	Write Data	Notes
SYN_MCLK_FREQ ($2F)	$F8	Set FREQ to 120 decimal and SRC to 1.
SYN_SDIV ($4D)	$08	Set source-divider to 960 MHz/120 MHz = 8.
SPLL_RDIV ($6A)	$0001	Set SPLL reference divider to pass 120 MHz SYN_MCLK undivided.
SPLL_CON ($34)	$02	24-bit fractional mode.
SPLL_BLEED ($35)	$8317	Enable bleed and configure 400 µA bleed bias and 300 µA bleed set currents.
SPLL_CP ($36)	$051F	Set charge pump bias to 1600 µA and current 1600 µA.
SPLL_PD ($37)	$00	Set minimum phase detector pulse width.
SPLL_IDIV ($39)	$0021	4 GHz/120 MHz = 33.333rec. Nearest integer value is 33.
SPLL_FDIV1 ($3B)	$55	24-bit fractional value is 2^{24} x 1/3 = 5 592 405. Always load SPLL_FDIV1 before SPLL_FDIV0 in 24-bit fractional mode.
SPLL_FDIV0 ($3A)	$5555	
OUTPUT_DIV ($40)	$01	Output divider set to divide by 2.
LOOUT1_BUF ($41)	$0C	Maximum power.
SYN_ISE ($31)	$6E	Enable all interrupt sources to indicate SYN_MCLK_READY, SPLL calibration completion, SPLL lock, SPLL out-of-lock and SPLL recalibration indicator.
SYN_ISM ($32)	$6E	Drive IRQN pin low if an interrupt is triggered.

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Register (Address)	Write Data	Notes
SYN_GCR ($2E)	$0469	Enable all synthesizer functions except external VCO controls and LO1_OUTPUT.

The expected sequence of interrupt status values read from the SYN_ISR_RD register in response to the IRQN pin going is shown in Table 10.

Table 10 Expected Synthesizer Interrupt Status Sequence (Example 1)

Register (Address)	Read Data	Notes
SYN_ISR_RD ($B0)	$40	SYN_MCLK ready.
SYN_ISR_RD ($B0)	$20	SPLL calibration complete.
SYN_ISR_RD ($B0)	$04	SPLL in-lock.

SYN_ISR_RD ($B0) register bit1 (SPLL_RECAL) and bit3 (SPLL_OUTLOCK) may be triggered in response to extreme voltage and temperature changes.

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7.1.2 Example 2 - External VCO Operation

An external VCO is required to be tuned to 1.82 GHz.

The device will be configured to synthesise 1.82 GHz from the SPLL using an external VCO with non-inverted VCO gain from a 40 MHz comparison frequency. The 40 MHz comparison frequency will be derived from a 960 MHz reference signal produced by the RVCO. Note, when using an external VCO, the maximum permitted comparison frequency is 50 MHz.

In this application example, the device will be used for short periods and then disabled. The REF_PLL and SPLL will be calibrated when re-enabling the device so the REF_PLL and SPLL recalibration indicators are not required.

As a safeguard to guard against spurious emissions, it is required to ensure that the SPLL does not go out-of-lock. The required device configuration is shown in Figure 9.

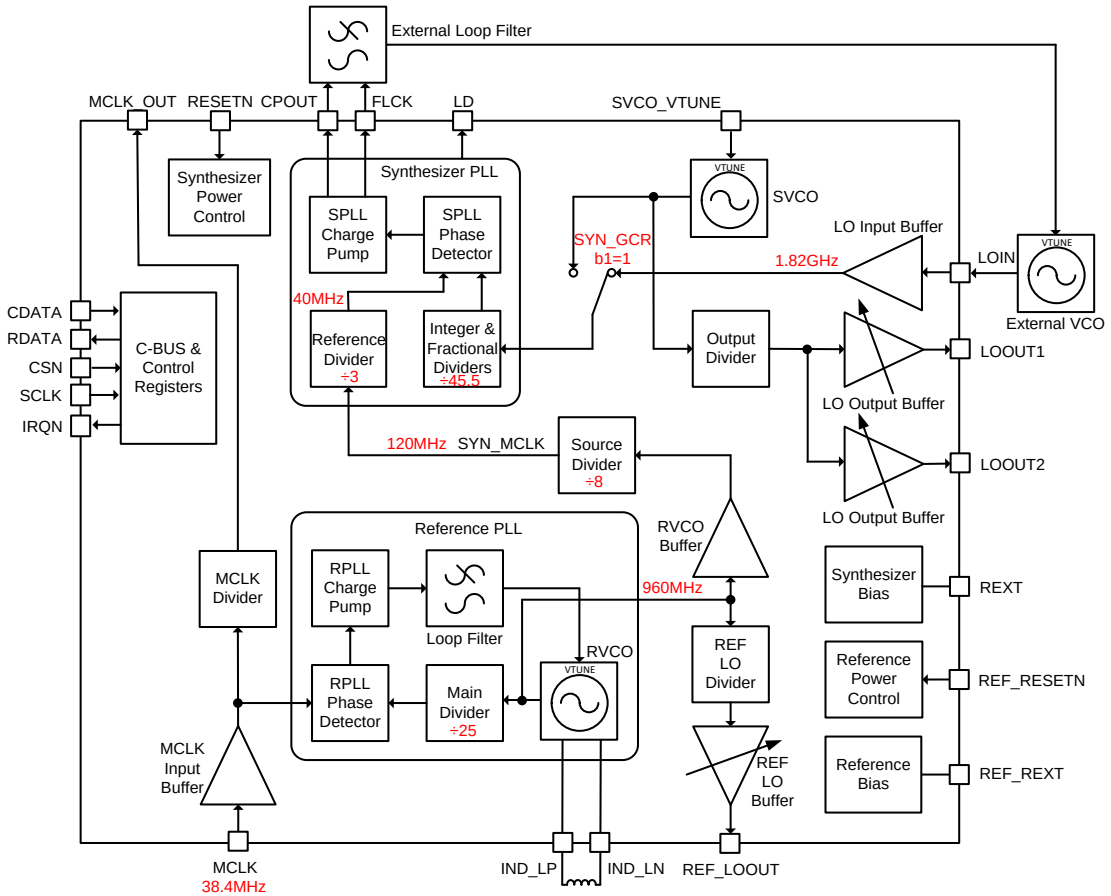

Figure 9 SPLL with External VCO

Table 11 C-BUS Writes to Reference Registers (Example 2)

Register (Address)	Write Data	Notes
REF_MCLK_FREQ ($76)	$26	MCLK frequency set to 38 decimal (integer nearest 38.4).
REF_PLL_MDIV ($7A)	$19	Set REF_PLL integer divider to 960 MHz/38.4 MHz = 25.
REF_ISE ($77)	$04	Enable REF_PLL calibration completion interrupt.
REF_ISM ($78)	$04	Drive IRQN pin low if interrupt is triggered.

Register (Address)	Write Data	Notes
REF_GCR ($75)	$0F	Enable all reference functions.

The expected sequence of interrupt status values read from the REF_ISR_RD ($C9) register in response to the IRQN pin going is shown in Table 12.

Table 12 Expected Reference Interrupt Status Sequence (Example 2)

Register (Address)	Read Data	Notes
REF_ISR_RD ($C9)	$04	Calibration complete.

Following the calibration complete indication of the Reference PLL, the recommended sequence of C-BUS writes to configure and enable the Synthesizer system is shown in Table 13.

Table 13 C-BUS Writes for SPLL Operation (Example 2)

Register (Address)	Write Data	Notes
SYN_MCLK_FREQ ($2F)	$F8	Set FREQ to 120 decimal and SRC to 1.
SYN_SDIV ($4D)	$08	Set source-divider to 960 MHz/120 MHz = 8.
SPLL_RDIV ($6A)	$0003	Set SPLL reference divider to divide by 3 (120 MHz/40 MHz).
SPLL_CON ($34)	$02	24-bit fractional mode.
SPLL_BLEED ($35)	$8317	Enable bleed and configure 400 µA bleed bias and 300 µA bleed set currents.
SPLL_CP ($36)	$051F	Set charge pump bias to 1600 µA and current 1600 µA.
SPLL_PD ($37)	$00	Set minimum phase detector pulse width.
SPLL_IDIV ($39)	$002E	1.820 GHz/40 MHz = 45.5. Use integer value of 46.
SPLL_FDIV1 ($3B)	$80	24-bit fractional value is 2^{24} x -0.5 = -8 388 608. Always load SPLL_FDIV1 before SPLL_FDIV0 in 24-bit fractional mode.
SPLL_FDIV0 ($3A)	$0000	
SYN_ISE ($31)	$08	SPLL out-of-lock.
SYN_ISM ($32)	$08	Drive IRQN pin low when SPLL out-of-lock interrupt is triggered.
SYN_GCR ($2E)	$042B	SYN_MCLK, lock detection, SPLL calibration, non-inverted external VCO gain, external VCO and SPLL.

In this example, the IRQN pin will only go low if SYN_ISR_RD ($B0) register bit3 (SPLL_OUTLOCK) is set - this interrupt may be triggered in response to extreme voltage and temperature changes.

7.1.3 Example 3 - Internal SVCO Operation, 435 MHz output

In this example, a 435.525 MHz signal is required to be output on the LOOUTT1 pin at maximum power.

The device will be configured to synthesise a 3484.2 GHz frequency from the SPLL using the internal SVCO and a low-noise reference frequency of 120 MHz. To obtain a 120 MHz low-noise reference frequency, the REF_PLL will be configured to generate a frequency of 960 MHz from a 38.4 MHz external MCLK oscillator. The 960 MHz RVCO frequency will then be divided by 8 to provide a 120 MHz reference frequency for the SPLL.

To guard against spurious emissions, it is required to ensure that the device raises an interrupt if the SPLL goes out of lock. It is also required to confirm that the SPLL has locked.

The calibration of the REF_PLL and SPLL should always be performed if the device is enabled from cold. In this application example, the device will be used for an extensive period. In order to obtain the lowest phase noise performance, the device must be recalibrated, if required, as indicated by the recalibration interrupts. The required device configuration is shown in Figure 10.

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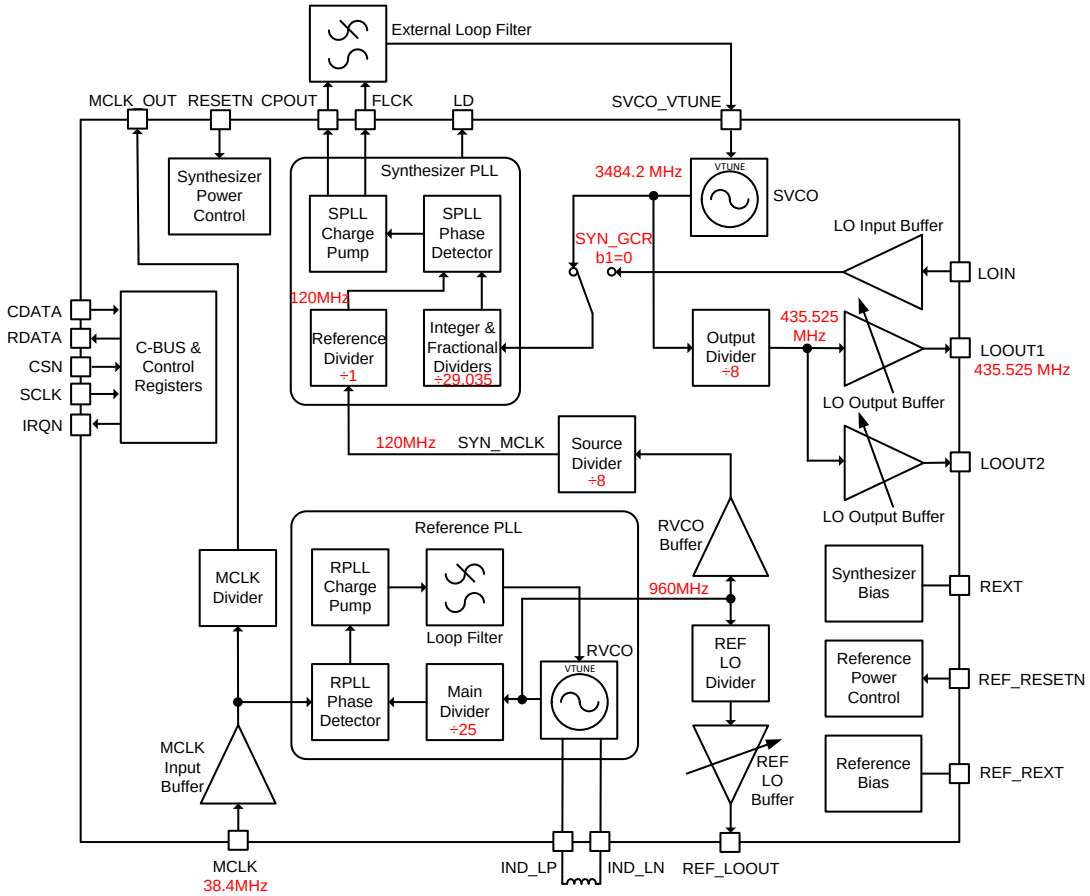


Figure 10 SPLL with Internal SVCO

The Reference PLL settings are as per the earlier example 1 in section 7.1.1. Following the calibration complete indication of the Reference PLL, the recommended sequence of C-BUS writes to configure and enable the Synthesizer system is shown in Table 9.

Table 14 C-BUS Writes to Synthesizer Registers (Example 3)

Register (Address)	Write Data	Notes
SYN_MCLK_FREQ ($2F)	$F8	Set FREQ to 120 decimal and SRC to 1.
SYN_SDIV ($4D)	$08	Set source-divider to 960 MHz/120 MHz = 8.
SPLL_RDIV ($6A)	$0001	Set SPLL reference divider to pass 120 MHz SYN_MCLK undivided.
SPLL_CON ($34)	$02	24-bit fractional mode.
SPLL_BLEED ($35)	$8317	Enable bleed and configure 400 µA bleed bias and 300 µA bleed set currents.
SPLL_CP ($36)	$051F	Set charge pump bias to 1600 µA and current 1600 µA.
SPLL_PD ($37)	$00	Set minimum phase detector pulse width.
SPLL_IDIV ($39)	$001D	3.4842 GHz/120 MHz = 29.035. Nearest integer value is 29.
SPLL_FDIV1 ($3B)	$08	24-bit fractional value is 2^{24} x 0.35 = 587 203. Always load SPLL_FDIV1 before SPLL_FDIV0 in 24-bit fractional mode.
SPLL_FDIV0 ($3A)	$F5C3	
OUTPUT_DIV ($40)	$05	Output divider set to divide by 8.
LOOUT1_BUF ($41)	$0C	Maximum power.

Register (Address)	Write Data	Notes
SYN_ISE ($31)	$6E	Enable all interrupt sources to indicate SYN_MCLK_READY, SPLL calibration completion, SPLL lock, SPLL out-of-lock and SPLL recalibration indicator.
SYN_ISM ($32)	$6E	Drive IRQN pin low if an interrupt is triggered.
SYN_GCR ($2E)	$0469	Enable all synthesizer functions except external VCO controls and LO1_OUTPUT.

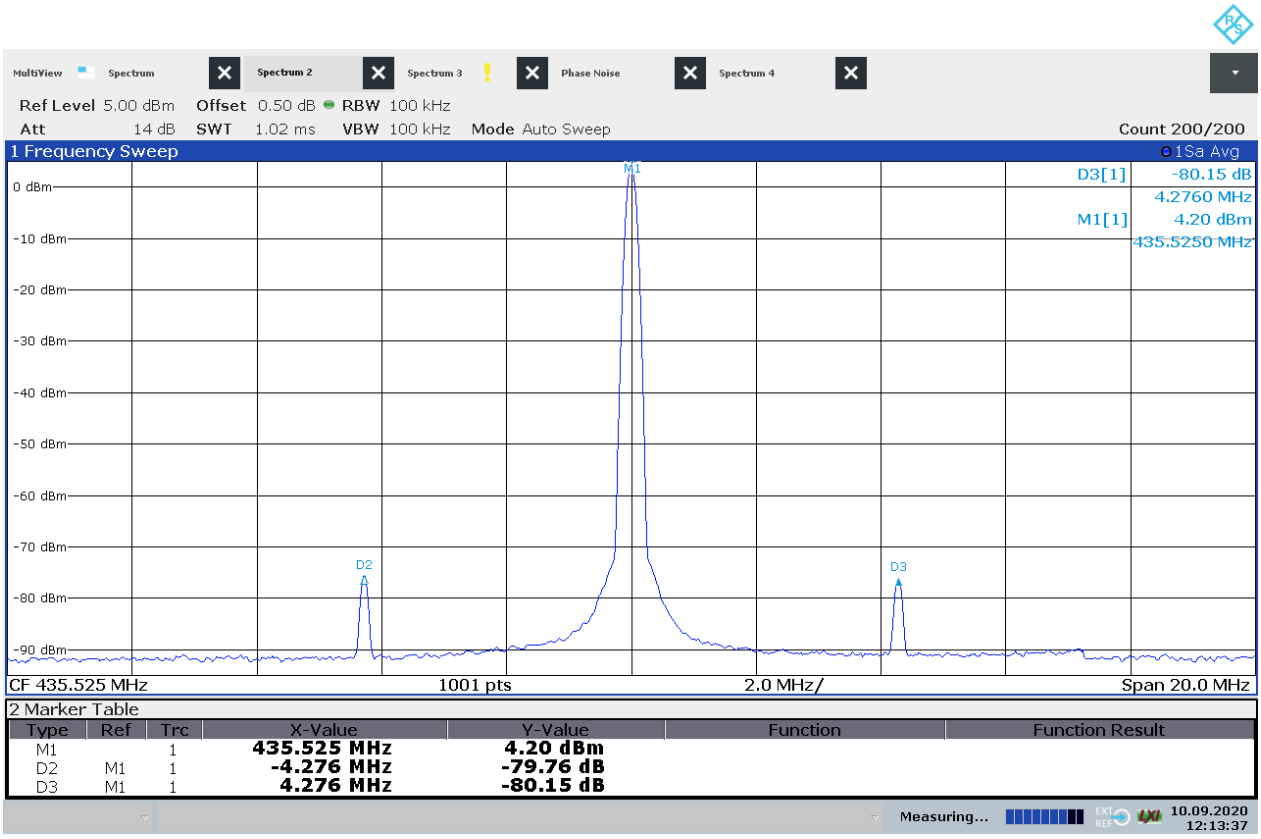
The expected sequence of interrupt status values read from the SYN_ISR_RD register in response to the IRQN pin going low is shown in Table 10.

Table 15 Expected Synthesizer Interrupt Status Sequence (Example 3)

Register (Address)	Read Data	Notes
SYN_ISR_RD ($B0)	$40	SYN_MCLK ready.
SYN_ISR_RD ($B0)	$20	SPLL calibration complete.
SYN_ISR_RD ($B0)	$04	SPLL in-lock.

SYN_ISR_RD ($B0) register bit 1 (SPLL_RECAL) and bit 3 (SPLL_OUTLOCK) may be triggered in response to extreme voltage and temperature changes.

Note that with the above low fraction value of only 0.035, a boundary spur will occur at around 0.035 * 120 = 4.2 MHz. This is attenuated by the action of the loop filter and suppressed to -80 dBc. A change to the SPLL reference to obtain a higher fraction would result in a lower spurious level,



12:13:37 10.09.2020

Figure 11 - Boundary spurious from 435.525 MHz output at -80 dBc.

7.2 PLL Register Value Calculations

Register value calculated from wanted frequency, including output divider.

Reference PLL (REF_PLL)

The main Synthesizer PLL reference frequency can derived from the REF_PLL sub-system. The decimal REF_PLL values can be calculated from the following:

SYN_MCLK (MHz) = RVCO frequency (MHz) / SYN_SDIV

And

RVCO frequency (MHz) = Reference MCLK (MHz)* REF_PLL_MDIV

This can be further divided by the value of SPLL_RDIV to provide the comparison frequency for the SPLL. From the above, it can be shown that:

SYN_MCLK (MHz) / Reference MCLK frequency (MHz) = REF_PLL_MDIV / SYN_SDIV

Example:
SYN_MCLK (120 MHz) / Reference MCLK (38.4 MHz) = REF_PLL_MDIV (25) / SYN_SDIV (8)
The RVCO then operates at 38.4 *25 = 960 MHz.

Synthesizer PLL (SPLL)

The output frequency of the SPLL is set by the following calculation:

$$F_{VCO} = f_{ref} \times (N / SPLL\_RDIV)$$

where:

F_{VCO} = The desired VCO frequency in MHz – this could be the internal SVCO or an external module.
f_{ref} = The reference frequency supplied to the SPLL (SYN_MCLK) in MHz
N = Divider value programmed in the N divider registers (This comprises the Integer and Fractional components, SPLL_IDIV, SPLL_FDIV1 and SPLL_FDIV0.)
SPLL_RDIV = Divider value programmed in the SPLL_R divider register ($6A)

Also note that the comparison frequency $f_{comp} = f_{ref} / SPLL\_RDIV$

To operate the RFPLL in 16-bit fractional mode with an internal VCO frequency f_{VCO} = 3568.375 MHz, SYN_MCLK = 120 MHz and a PLL comparison frequency f_{COMP} = 60 MHz.

SPLL_RDIV = 120 MHz ÷ 60 MHz = 2

Ndiv = $f_{VCO} \div f_{COMP}$ = 3568.375 MHz ÷ 60 MHz = 59.472 916 67

Splitting the N divider value into integer and fractional parts:

SPLL_IDIV = Round (59.472 916 67) = 59 (decimal) = 0x003B (hex)

Fdiv (16-bit mode) = Round ($2^{16} \times$ (Ndiv – Idiv)) = 30 993 (decimal) = 0x7911 (hex)

So the C-BUS register values are:
SPLL_IDIV = 0x003B
SPLL_FDIV0 = 0x7911

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With the output divider OUTPUT_DIV set to 0 x 05 (divide by 8), the output is at 446.046 875 MHz.

The frequency resolution at the output in this example is

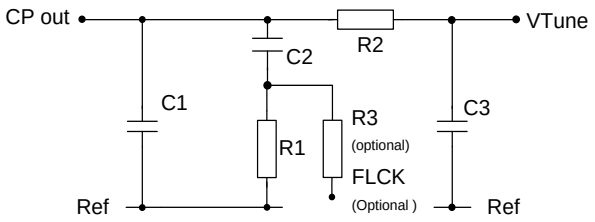
$f_{COMP} \div (2^N * OUTPUT\_DIV)$
Where N =Number of fractional bits, OUTPUT_DIV = output divider value

60 MHz ÷ $(2^{16} * 8) \approx 114.44$ Hz.

7.3 Loop Filter Design

The design of the loop filter for phase-locked loops is relatively simple in principle but can be complex in practice. It is impossible in a datasheet to cover all aspects of loop filter design; for those interested in the detail please consult one of the many text books on phase-locked loops. This datasheet provides some specific guidance for the CMX940 SPLL loop filter.

The Loop Filter design is based upon the use of a passive 3rd order Loop Filter as shown below.



The loop filter can be considered as two pole filter (R1, C1, C2) with the addition of a single pole spur filter (R2,C3) added to attenuate spurs.

The two pole loop filter consists of a resistor R1 in series with a capacitor C2 and C1. The resistor provides the stabilising zero to improve the phase margin and hence improve the transient response of the PLL. However, the resistor causes a ripple of value I_{CP} x R1 on the control voltage at the beginning of each phase detector pulse. At the end of the pulse, a ripple of equal value occurs in the opposite direction. This ripple modulates the VCO frequency and introduces excessive jitter in the output. A small capacitor C1 is added in parallel with the R1 and C2 network to suppress the glitch generated by the charge pump at every phase comparison instant, which in turn lowers the ripple on the control voltage and acts to suppress the induced jitter.

The value of C1 should be less than the value of C2 by a factor of approximately 10 to avoid underdamped settling. The choice of the loop parameters, R1, C2 and C1 can be determined by assuming a continuous time approximation. In a typical application the loop bandwidth is set to between F_{Comp} /25 and F_{Comp} /100. This value is a compromise as a lower loop bandwidth helps to filter out reference or integer boundary spurs in the PLL output, but a higher loop bandwidth decreases lock time and helps reduce PLL jitter by filtering out noise (esp. flicker noise) within the loop bandwidth.

The frequency at which the PLL open loop phase margin is a maximum, should coincide with the chosen loop bandwidth.
The resistor R1, in combination with C1 & C2 capacitors in the two pole loop filter, determines the frequency where the peak phase margin is achieved.

The important loop equations for the two pole filter are as follows:

(1) $C2 = I_{cp} K_{vco} / N (2\pi F_n)^2$

(2) $R1 = 2\xi\sqrt{(N/ I_{cp} K_{vco}C2)}$
(3) $C1 = C2/10$
(4) $BW = \pi F_n [\xi + (1/4 \xi)]$
(5) $\omega_n = 2\pi F_n$
(6) $PM \sim 100\xi$

where

F_{Comp} is the phase detector comparison frequency (= Fref / N)
N is feedback divider value
I_{cp} is charge pump current (A/2π rad)
K_{vco} is vco gain (MHz/V)
F_n is the natural loop frequency
BW is the loop bandwidth
PM is the phase margin
ξ is the damping factor

Now looking at the single pole spur filter R2 and C3, the attenuation and time constant T3 can be defined as:

(7) $Atten = 10\log [(2\pi F_{Comp} R2{\cdot}C3)^2 + 1]$ and
(8) $T3 = R2{\cdot}C3$.

Then in terms of the attenuation of the comparison frequency spurs added by the single pole filter we have:

(9) $T3 = \sqrt{[(10^{(Atten/10)} - 1)/(2\pi F_{Comp})^2]}$

The additional pole must be lower than the comparison frequency F_{Comp} in order to attenuate spurs, but should be at least 5 times greater than the loop bandwidth, otherwise the loop may become unstable.

In general C3 should be ≤ C1/10 and R2 should be ≥ 2×R1 otherwise T3 will interfere with the filter's primary section comprising R1, C1 and C2.

The value of C3 should also account for the input capacitance of the VCO tuning input. For external VCOs this could be several picofarads. For the on-chip CMX940 VCO, this is around 2 pF.

Worked example:
VCO frequency = 3.4 GHz, F_{Comp} = 120 MHz, I_{cp} = 1600 µA, K_{vco} = 45 MHz/V, Loop BW = 300 kHz, ξ = 0.707

a) N = 28.3333
b) C2 = 6.43 nF
c) R1 = 349 Ω
d) C1 = 643 pF
e) T3 = 5.63 e-08
f) Let R2 = 5 * R1, = 1.748 kΩ
g) C3 = T3/R2 = 32 pF

The choice should now be made of preferred values for R1, R2, C1, C2 and C3 using +/-1% on resistors and +/- 5% on capacitors, which would be C1 = 680 pF, C2 = 6.8 nF, C3 = 33 pF, R1 = 330 Ω, R2 = 1.8 kΩ.

The preferred values chosen should then be tested in the application and adjustment can then be made to optimise the loop response as required.

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7.4 Spurs and Spur Avoidance

The CMX940 has a dual loop architecture, the REF_PLL providing a reference for the higher frequency fractional-N SPLL.

Spurious signals from a Fractional-N PLL can occur at offsets from the main output of:

- The input Master reference frequency (sidebands at +/- MCLK and harmonics)
- The loop comparison frequency (sidebands at +/- F_{Comp}, and harmonics)
- Frequencies offset from the integer-N frequency (e.g. at N x F_{Comp}, also referred to as 'Integer Boundary Spurs' or 'IBS'). These can be reduced by the action of the loop filter.
- Frequencies offset from simple fractions of the integer-N frequency (also referred to as 'high order boundary spurs'). These can be reduced by the action of the loop filter.
- Smaller offsets caused by longer strings of zeros in the lower significant bits of the fractional value.

Avoidance techniques can be used to minimise some of these effects, and is a particular strength of the CMX940 architecture. Production of a complete frequency plan for the particular application is advised.

Spurious can also be reduced in level through use of the output frequency dividers (although other spurs can also be generated).

All of the above spur types can be observed in the CMX940 SPLL.

In addition:

- Low-level sub-fractional spurs can also be observed. These can be improved by application of bleed current (see section 6.7.2).
- Leakage from the reference RVCO can also be observed at the SPLL outputs, which may also need to be considered in a frequency plan. Operating the RVCO with a different inductor value may be required to enable this to be more effectively filtered out by later stages of the RF system.
- If harmonics of the main SPLL output are close in frequency to the RVCO, the mix of these can produce spurious at the SPLL output. These can be avoided by reprogramming the REF_PLL to a different RVCO frequency.
- Spurious can be observed when generating an output close to harmonics of the reference MCLK (MCLK Boundaries). LOOUT1 can give marginally lower spurious outputs than LOOUT2 in this respect.

7.4.1 **MCLK** Sideband spurs

Spurious sidebands can occur at offsets of the master input reference frequency (i.e. at +/- MCLK and harmonics). PCB Layout, decoupling, MCLK frequency, signal level and harmonic content can all have an effect on these levels. Fast MCLK edges are required for the lowest noise performance, but this can be at the detriment of spur level.
In the CMX940, the use of a dual-loop architecture provides higher isolation between the input reference and the output and ensures that these spurs are at a low level.

7.4.2 Comparison Frequency Sidebands

Sidebands can occur at offsets of the Comparison Frequency (+/- F_{Comp} and harmonics). These spurs are largely reduced by the action of the loop filter.

In the CMX940, use of a large SPLL comparison frequency (up to 120 MHz) compared to the loop bandwidth reduces these spurs significantly, and at large offsets can be effectively filtered out easily by the later stages of the RF system.

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7.4.3 FComp Boundary Spurs

Spurs can occur where F_{VCO} is close to N x F_{Comp}.

Mathematically, these spurs occur at frequency offsets of +/- the fractional component of N from the VCO frequency. If these are at a sufficiently large offset, then they are supressed adequately by the action of the loop filter. At small offsets, these can result in products close to or within the loop bandwidth and so can be much larger (typically -43 dBc).

The CMX940 can overcome this through reprogramming of the reference PLL and / or the SPLL SDIV or reference divider path, setting a different comparison frequency for the SPLL and therefore creating a larger fractional offset. This requires no change to the input reference MCLK value. A software routine can be used to determine if the calculated fractional offset is sufficiently small to cause a problem.

7.4.4 Higher Order Boundary Spurs

These spurs occur where the fractional offset is close to a simple fractional value (e.g. ½, ⅓, ¼ etc.) At small offsets from a simple fraction, these can land within the loop bandwidth. For example, if a frequency is programmed at say 10 kHz from a 0.5 fraction, spurs can occur at +/- 20 kHz (and at a lower level at harmonics of 20 kHz); if 10 kHz from a 0.3333 fraction, spurs can occur at approximately +/- 30kHz and harmonics; if a frequency is programmed at 10 kHz from a 0.25 fraction, spurs occur at +/- 40 kHz and harmonics, and so on.

The amplitude of these reduce with order and offset from the simple fraction. At offsets close to 6^{th} order and above, these spurious may be sufficiently small as to be of little consequence in most radio systems. In practice, a value of ⅓ cannot be exactly represented as a finite binary fraction, so there will then be a strong fractional component at +/- (offset + FComp /(2^N)) where N is the number of fractional bits.

Frequency planning can predict where these high order boundaries occur, so again the power of the CMX940 architecture means that different REF_PLL values can be used to avoid these.

Boundary spurious can also be reduced by applying a small value of bleed current (see section 6.7.2). This can increase the level of the comparison frequency spurs, though this may be an acceptable compromise.

7.4.5 Sub-Fractional Spurs

These spurs are caused by a sub-fractional pattern within the fractional value due to a continuous string of zeros in the lower significant bits of FDIV0. These spurious occur as sidebands from the carrier at frequency intervals of:

ResVCO * (2 ^ (n-1))
Where n = number of LSB 0 bits.
ResVCO = Frequency Resolution at VCO (before output division)
These spurs are usually at a low level but may be reduced further by the following:

1- The polarity of the lowest significant bit can be changed (e.g. an FDIV0 Hex value ending xxx0 changed to xxx1). This does add a very small frequency error but this should be tolerable in the majority of systems, particularly in 24-bit mode.
2- Application of bleed current.

7.4.6 MCLK Boundaries

Spurs can occur where F_{VCO} is very close to N x MCLK, resulting in a product close to or within the loop bandwidth, so a large MCLK creates the lowest number of MCLK boundaries. For a given application, a frequency plan should avoid these where possible.

In the CMX940, use of a dual loop architecture minimises this effect.

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An alternative, though more costly, solution is to use two non-harmonically related MCLK sources and switching between them as appropriate.

7.5 Layout

Please refer to the Evaluation Kit data for recommended PCB layout information. Good RF practice should be used in terms of ground planes, vias, short trace /path lengths for decoupling and isolation between critical signals, etc. Capacitors should be placed as close as possible to pins.

In particular, care should be taken that the input MCLK signal, charge pump output and VCO tuning voltage lines are isolated and shielded from potential interference sources.

7.6 Typical performance

7.6.1 LO input sensitivity

TBD

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8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (AV_{DD} - GND) and (DV_{DD} - GND)	-0.3	+3.6	V
Voltage on any pin to relative to GND	-0.3	V_{DD} + 0.3	V
Voltage between pins DGND and AGND	-30	+30	mV
Current into or out of any pin	-100	+100	mA

# Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25ºC		800	mW
...Derating		13	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
AV_{DD}, DV_{DD} Supply voltage		3.0	3.6	V
Operating Temperature		-40	+85	ºC
Serial Clock Frequency			10	MHz

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8.1.3 Operating Characteristics

Operating Characteristics apply for the following conditions unless otherwise specified:
AV_{DD}= 3.0V to 3.6V, DV_{DD}= 3.0V to 3.6V, T_{AMB} -40 to +85 ºC.
Typical values are at $DV_{DD} = AV_{DD}$ = 3.3V, T_{AMB} = 25ºC.

DC Characteristics

Parameter	Min	Typ	Max	Units	Comment
Supply Current					
Sleep		TBD		mA	Register contents retained
MCLK active		2		mA	
REF PLL active (excluding o/p divider & buffers)		8		mA	
REF_LOOUT buffer		17		mA	Max level from RPLL, no division, 960 MHz
REF_LOOUT buffer + DIV		25		mA	Max level from RPLL, 40 MHz
REF_PLL + SPLL only, Internal VCO (locked)		49		mA	No output divider or buffer, Fvco = 3120 MHz, Fcomp 120 MHz, MCLK input = 38.4 MHz,
REF_PLL + SPLL only, External VCO input		23		mA	Fin = 851 MHz, Fcomp 48 MHz, MCLK input = 38.4 MHz,
Combined REF_PLL + SPLL + Output divider 2 & output buffer (LOOUT1 or 2), -15 dBm output..		53		mA	Fout = 1450 MHz, Fcomp = 96 MHz, MCLK input = 38.4 MHz, CP current 1250µA Integer N
Combined REF_PLL + SPLL + Output divider 4 & output buffer (LOOUT1 or 2), -10 dBm output.		55		mA	Fout = 730 MHz, Fcomp = 120 MHz, MCLK input = 38.4 MHz, CP current 1250µA
Combined REF_PLL + SPLL + Output divider 8 & output buffer (LOOUT1 or 2), -10 dBm output..		58		mA	Fout = 480 MHz, Fcomp = 96 MHz, MCLK input = 38.4 MHz, CP current 1250µA Integer N
Combined REF_PLL + SPLL + Output divider 8 & output buffer (LOOUT1 or 2), +3 dBm output.		62		mA	Fout = 360 MHz, Fcomp = 120 MHz, MCLK input = 38.4 MHz, CP current 1250µA Integer N
Combined REF_PLL + SPLL + Output divider 20 & output buffer (LOOUT1 or 2), +3 dBm output..		64		mA	Fout = 144 MHz, Fcomp = 120 MHz, MCLK input = 38.4 MHz, CP current 1250µA Integer N
Logic ‘1’ Input Level	TBD	-	-	V	
Logic ‘0’ Input Level			TBD	V	
Hysteresis	-	TBD		mV	
Input Threshold Rising		TBD		V	
Input Threshold Falling		TBD		V	
Logic ‘1’ Output Level	TBD	-	-	V	I_{OH} = 4mA
Logic ‘0’ Output Level	-	-	TBD	V	I_{OL} = 4mA
Digital IO Source/Sink Current Limit	TBD			mA	
Digital IO pin capacitance		TBD		pF	

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AC Characteristics

Parameter	Min	Typ	Max	Units	Comment
RF Output					
RF output range	48.57		2040	MHz	Output available 2040 to 4080 MHz as a test mode, level is not specified.
RF output level	-15	0	3	dBm	Power delivered into 50 ohm load.; push-pull mode, Fout = 480 MHz.
RF Output power variation with frequency		4		dB	50 to 2040MHz
RF output power step size	1	2	3	dB	
Muted output power		-34		dBm	Note 1
Second Harmonic		-24		dBc	at 480MHz & 0dBm
PLL					
MCLK input					
Frequency	10		120	MHz	
Level dc coupled	0.7		1.8	Vp-p	Typically square wave
Level ac coupled	0.7		1.35	Vp-p	Typically clipped sinewave; see also Note 2
Slew rate	300			V/µs	
Ref divider range	1		1023		
Ref PLL post divider range	1		1023		
Synthesizer					
Comparison frequency (f_{PD})	10		120	MHz	Max 50 MHz with external VCO.
External LO input frequency	100		2000	MHz	
RF input level 100 MHz – 1 GHz 1 GHz – 2 GHz	 -15 -10		 0 0	dBm	Note 3
Divider (N counter)	24-bit Fractional-N				
N-Divider range (Integer mode)	16		2047		
N-Divider range (Fractional mode)	20		2043		
Charge pump current	50		2400	µA	48 steps of 50uA
Charge pump mismatch			2	%	At Icp=1.6mA after cal. Note 4
Charge pump compliance	0.6		V_{DD} - 0.6	V	Note 4
1 Hz normalized phase noise (PN1Hz)		-225		dBc/Hz	Charge pump at 2.4mA. Comparison frequency 120 MHz, f_{rf} = 1200 MHz (N = 10), wide loop BW
1 Hz normalized phase noise		-219		dBc/Hz	Charge pump at 2.4mA. Comparison frequency 120 MHz, f_{rf} = 875 MHz (N = 7.291667)
1 Hz normalized phase noise		-217		dBc/Hz	Charge pump at 2.4mA. Comparison frequency 120 MHz. generated by R-PLL, f_{rf} = 875 MHz (N = 7.291667)
1 Hz normalized phase noise		-219		dBc/Hz	Charge pump 2.4mA. Comparison frequency 19.2 MHz, f_{rf} = 875 MHz (N = 45.57292)

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Parameter	Min	Typ	Max	Units	Comment
Spurious Products					
Integer Boundary Spurs		-40		dB	Measurement conditions to be defined within the PLL loop bandwidth
Sub integer boundary spurs		-56		dB	Note 5
Other non-harmonic spurious products		-76		dB	Note 6
Internal VCO's					
Frequency	2720		4080	MHz	
Tuning sensitivity (K_{vco})		50		MHz/V	
Phase noise @ 1 MHz offset		-135		dBc/Hz	Measured at, or scaled to, 1 GHz
Phase noise @ 10 MHz offset		-154		dBc/Hz	Measured at, or scaled to, 1 GHz (Measurement may be limited by divider output stage)
Output divider (measured at chip output, including buffer)					
ratios		1†,2,3,4,6,8,12, 16,20,28,40,56			† divide by 1 (no division) is a test mode only
Duty cycle	40:60	50:50	60:40		Note 4
Nominal load impedance		50 Ω			

Notes

1. Measured on RX output with RX disabled and TX enabled or measured on TX output with TX disabled and RX enabled.
2. Current saving of 0.4 mA with 1.8 V logic input compared with 0.8 Vp-p clipped sinewave.
3. Broadband 50Ω termination case. Operation to 0 dBm but, recommend operation at -5dBm or below for best performance. Sensitivity can be improved over a limited band by use of matching components.
4. Parameter evaluated during design, not tested on every device.
5. Typ -56 dBc at 2nd order, improves with higher orders
6. Operating conditions and PCB layout are critical to meeting this figure

Reference PLL

Parameter	Min	Typ	Max	Units	Comment
Reference input					
Frequency	10		40	MHz	
Level dc coupled	0.7		1.8	Vp-p	Typically square wave
Level ac coupled	0.7		1.35	Vp-p	Typically clipped sinewave; see also Note 2
Slew rate	300			V/µs	
PLL					
M-Divider range	4		127		
SPLL Source divider range	4		127		

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Parameter	Min	Typ	Max	Units	Comment
VCO					
Frequency	0.6		1.2	GHz	With suitable external inductor
Tuning sensitivity (K_{vco})		22.5		MHz/V	
Phase noise @ 1 MHz offset		-130		dBc/Hz	At 960 MHz
Phase noise @ 10 MHz offset		-144		dBc/Hz	At 960 MHz

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8.1.4 Operating Characteristics - C-BUS Timings

Operating Characteristics apply for the following conditions unless otherwise specified:
V_{DD} = 3.0V to 3.6V, T_{AMB} -40 to +85 ºC. Typical values are at DV_{DD} = 3.3V T_{AMB} = 25ºC.

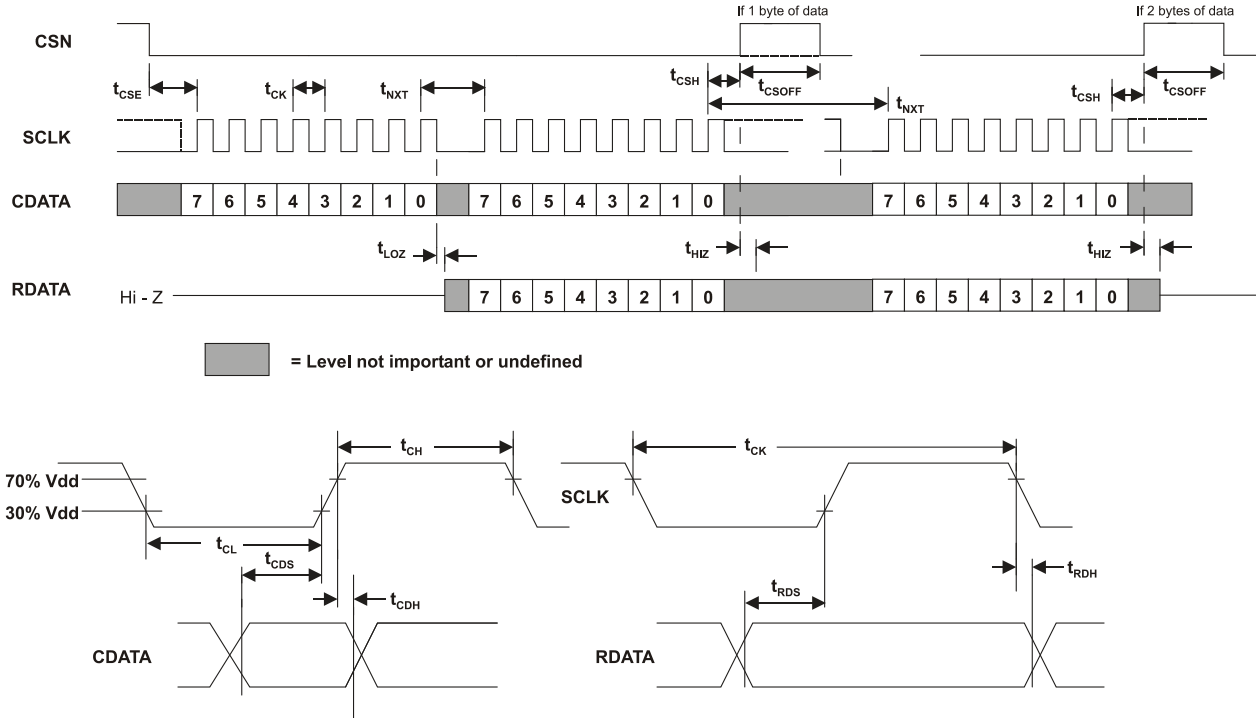

Figure 12 C-BUS Serial Interface Timings

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	50	ns
t_{CSOFF}	CSN high time between transactions		100	–	–	ns
t_{NXT}	Inter-byte time		100	–	–	ns
t_{CK}	SCLK cycle time		100	–	–	ns
t_{CH}	SCLK high time		50	–	–	ns
t_{CL}	SCLK low time		50	–	–	ns
t_{CDS}	CDATA setup time		25	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		25	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

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8.1.5 Typical Performance Characteristics

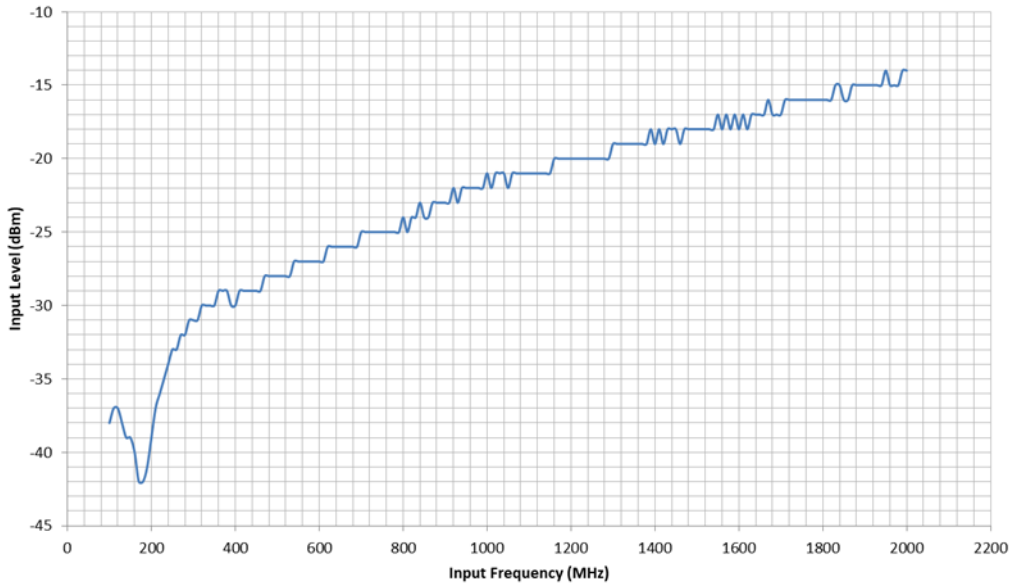
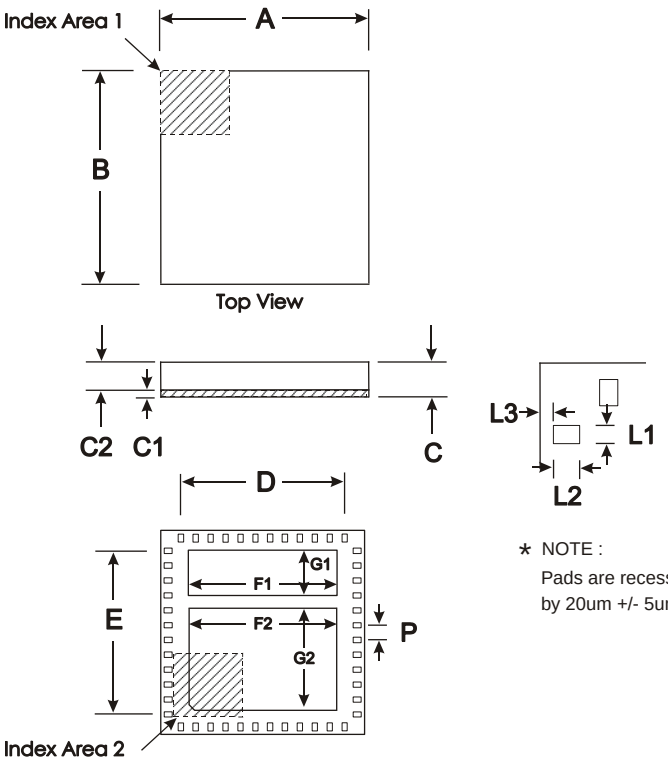


Figure 13 Typical LOIN Sensitivity, Measured Using a Broadband 50Ω Termination (see reference to L2, section 4.2)

8.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	6.95	7.00	7.05
B	6.95	7.00	7.05
C	0.92	1.01	1.10
C1	0.17	0.21	0.25
C2	0.75	0.80	0.85
D		5.50	
E		5.50	
F1		5.03	
F2		5.03	
G1		1.58	
G2		3.59	
L1		0.22	
L2		0.30	
L3	0.065	0.100	0.135
P		0.50	

* NOTE :
Pads are recessed
by 20um +/- 5um

* NOTE :

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

The underside of the package has exposed metal pads which must be soldered to the pcb and electrical connection to analogue ground must be made.

Figure 14 T1 Mechanical Outline

Order as part no. CMX940T1

8.3 Additional Qualification

ESD HBM as defined by JEDEC JS-001 and JEP-155	TBD
ESD CDM as defined by JEDEC JS-002 and JEP-157	TBD

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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