1. Description

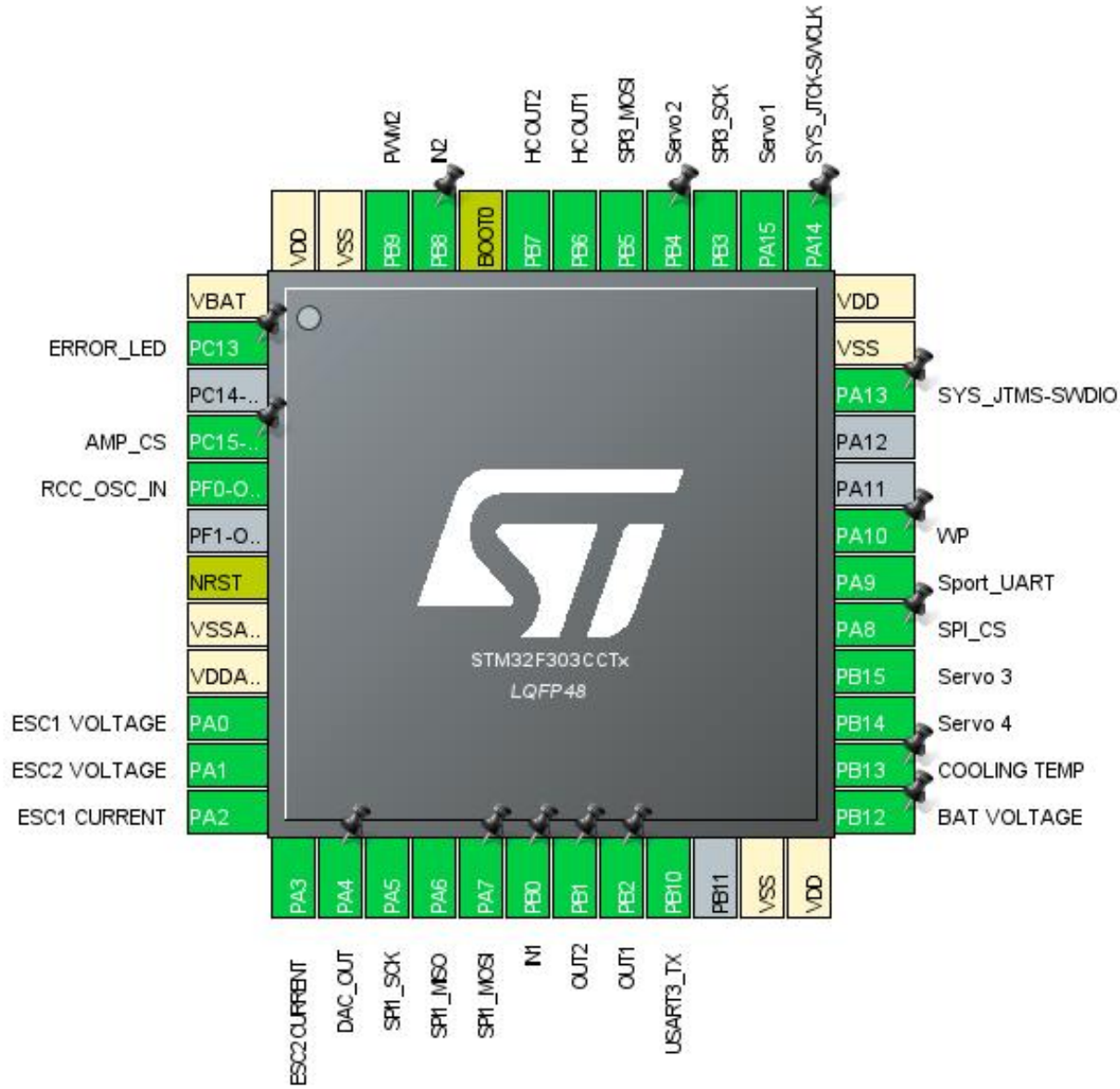
1.1. Project

Project Name	RCTelemetry
Board Name	custom
Generated with:	STM32CubeMX 5.2.1
Date	07/23/2019

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303CCTx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration



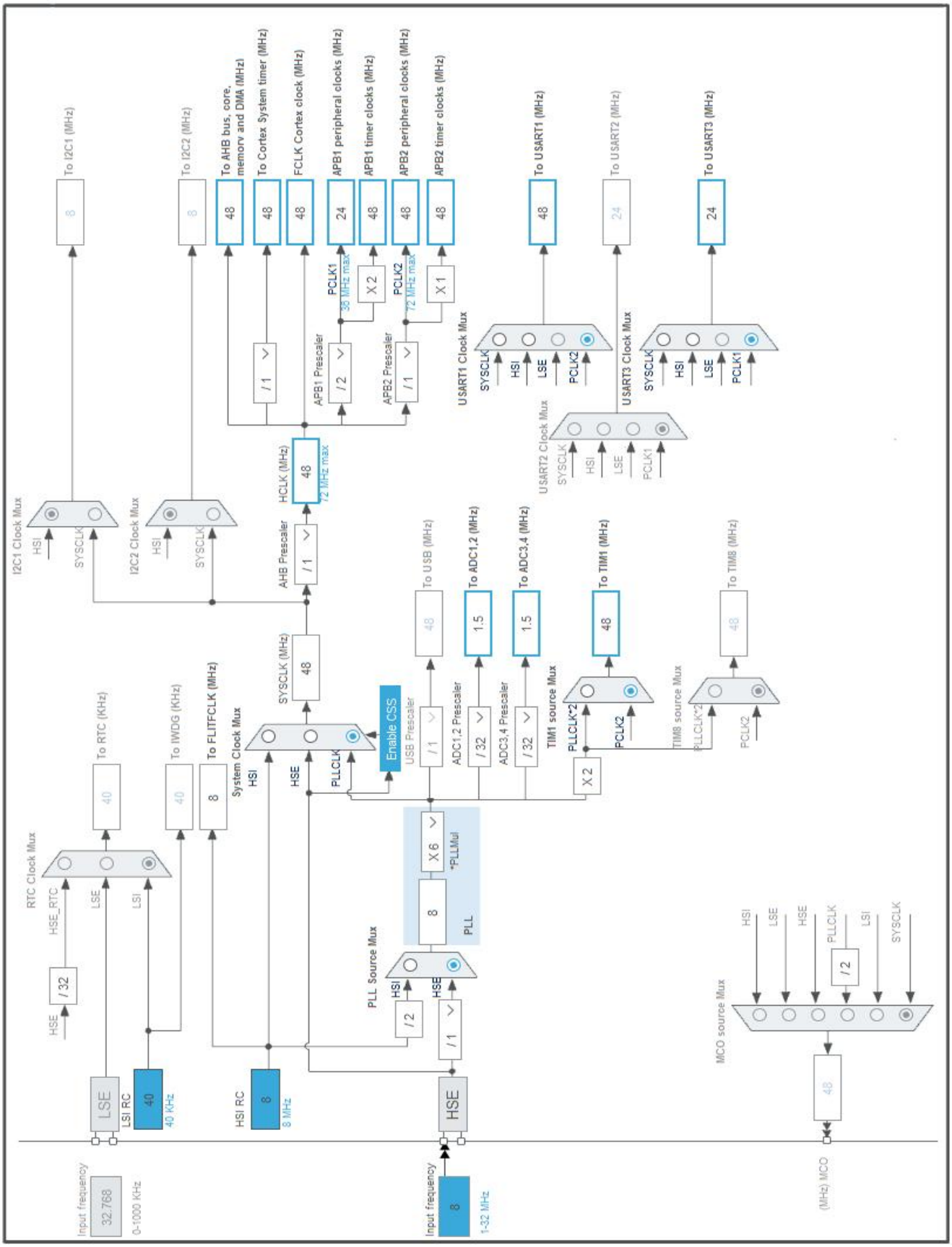
3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	ERROR_LED
4	PC15-OSC32_OUT *	I/O	GPIO_Output	AMP_CS
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	ADC1_IN1	ESC1 VOLTAGE
11	PA1	I/O	ADC1_IN2	ESC2 VOLTAGE
12	PA2	I/O	ADC1_IN3	ESC1 CURRENT
13	PA3	I/O	ADC1_IN4	ESC2 CURRENT
14	PA4	I/O	DAC_OUT1	DAC_OUT
15	PA5	I/O	SPI1_SCK	
16	PA6	I/O	SPI1_MISO	
17	PA7	I/O	SPI1_MOSI	
18	PB0 *	I/O	GPIO_Input	IN1
19	PB1 *	I/O	GPIO_Output	OUT2
20	PB2 *	I/O	GPIO_Output	OUT1
21	PB10	I/O	USART3_TX	
23	VSS	Power		
24	VDD	Power		
25	PB12	I/O	ADC4_IN3	BAT VOLTAGE
26	PB13	I/O	ADC3_IN5	COOLING TEMP
27	PB14	I/O	TIM15_CH1	Servo 4
28	PB15	I/O	TIM15_CH2	Servo 3
29	PA8 *	I/O	GPIO_Output	SPI_CS
30	PA9	I/O	USART1_TX	Sport_UART
31	PA10 *	I/O	GPIO_Output	WP
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
38	PA15	I/O	TIM2_CH1	Servo 1
39	PB3	I/O	SPI3_SCK	
40	PB4	I/O	TIM16_CH1	Servo 2
41	PB5	I/O	SPI3_MOSI	

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PB6	I/O	TIM4_CH1	HC OUT1
43	PB7	I/O	TIM4_CH2	HC OUT2
44	BOOT0	Boot		
45	PB8 *	I/O	GPIO_Input	IN2
46	PB9	I/O	TIM4_CH4	PWM2
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	RCTelemetry
Project Folder	D:\Files\GIT\rctelemetry\sw
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.10.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303CCTx
Datasheet	023353_Rev13

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

mode: IN4

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 4 ***
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	Channel 1
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	Channel 1
Sampling Time	

	7.5 Cycles *
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	Channel 1
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC3

mode: IN5

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software

External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC4

IN3: IN3 Single-ended

7.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1

Channel	Channel 3
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. CRC

mode: Activated

7.4.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.5. DAC

mode: OUT1 Configuration

7.5.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled

7.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.7. SPI1

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**12.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.8. SPI3

Mode: Transmit Only Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**12.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.9. SYS

Debug: Serial Wire

Timebase Source: TIM7

7.10. TIM1

Clock Source : Internal Clock

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

7.11. TIM2

Clock Source : Internal Clock

Channel1: Output Compare CH1

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**24000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**2000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1:

Mode	**Active Level on match ***
Pulse (32 bits value)	0
CH Polarity	High

7.12. TIM3

Clock Source : Internal Clock

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.13. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel4: PWM Generation CH4

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**48000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.14. TIM6

mode: Activated

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**64535 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.15. TIM15

mode: Clock Source

Channel1: Output Compare CH1

Channel2: Output Compare CH2

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 1:

Mode	Frozen (used for Timing base)

Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

7.16. TIM16

mode: Activated

Channel1: Output Compare CH1

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

7.17. USART1

Mode: Single Wire (Half-Duplex)

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	**57600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	**Enable ***
RX Pin Active Level Inversion	**Enable ***
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.18. USART3

Mode: Single Wire (Half-Duplex)

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	**100000 ***
Word Length	**9 Bits (including Parity) ***
Parity	**Even ***
Stop Bits	**2 ***

Advanced Parameters:

Data Direction	**Receive Only ***
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	**Enable ***
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. FREERTOS

Interface: CMSIS_V1

7.19.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**5256 ***

Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.19.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled

xTaskGetHandle	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	ESC1 VOLTAGE
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	ESC2 VOLTAGE
	PA2	ADC1_IN3	Analog mode	No pull up pull down	n/a	ESC1 CURRENT
	PA3	ADC1_IN4	Analog mode	No pull up pull down	n/a	ESC2 CURRENT
ADC3	PB13	ADC3_IN5	Analog mode	No pull up pull down	n/a	COOLING TEMP
ADC4	PB12	ADC4_IN3	Analog mode	No pull up pull down	n/a	BAT VOLTAGE
DAC	PA4	DAC_OUT1	Analog mode	No pull up pull down	n/a	DAC_OUT
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull up pull down	**High ***	
SPI3	PB3	SPI3_SCK	Alternate Function Push Pull	No pull up pull down	**High ***	
	PB5	SPI3_MOSI	Alternate Function Push Pull	No pull up pull down	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull up pull down	Low	Servo 1
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull up pull down	Low	HC OUT1
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull up pull down	Low	HC OUT2
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull up pull down	Low	PWM2
TIM15	PB14	TIM15_CH1	Alternate Function Push Pull	No pull up pull down	Low	Servo 4
	PB15	TIM15_CH2	Alternate Function Push Pull	No pull up pull down	Low	Servo 3
TIM16	PB4	TIM16_CH1	Alternate Function Push Pull	No pull up pull down	Low	Servo 2
USART1	PA9	USART1_TX	Alternate Function Open Drain	No pull up pull down	**High ***	Sport_UART
USART3	PB10	USART3_TX	Alternate Function Open Drain	No pull up pull down	**High ***	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull up pull down	Low	ERROR_LED
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull up pull down	Low	AMP_CS
	PB0	GPIO_Input	Input mode	No pull up pull down	n/a	IN1
	PB1	GPIO_Output	Output Push Pull	No pull up pull down	Low	OUT2
	PB2	GPIO_Output	Output Push Pull	No pull up pull down	Low	OUT1
	PA8	GPIO_Output	Output Push Pull	No pull up pull down	Low	SPI_CS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA10	GPIO_Output	Output Push Pull	No pull up pull down	Low	WP
	PB8	GPIO_Input	Input mode	No pull up pull down	n/a	IN2

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
DAC_CH1	DMA1_Channel3	Memory To Peripheral	**Medium ***
ADC3	DMA2_Channel5	Peripheral To Memory	Low
ADC1	DMA1_Channel1	Peripheral To Memory	**High ***
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
ADC4	DMA2_Channel2	Peripheral To Memory	Low

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

DAC_CH1: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC3: DMA2_Channel5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable

Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC4: DMA2_Channel2 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	5	0
DMA1 channel3 global interrupt	true	5	0
DMA1 channel4 global interrupt	true	5	0
DMA1 channel5 global interrupt	true	5	0
TIM1 trigger, commutation and TIM17 interrupts	true	5	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	5	0
TIM7 global interrupt	true	0	0
DMA2 channel2 global interrupt	true	5	0
DMA2 channel5 global interrupt	true	5	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	unused		
ADC3 global interrupt	unused		
SPI3 global interrupt	unused		
Timer 6 interrupt and DAC underrun interrupts	unused		
ADC4 interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

9. Software Pack Report