ADC_INTERFACE_LTC2325CUKG

Module Design Document

Background

The ADC_INTERFACE_LTC2325CUKG is responsible for the interface to the LTC2325CUKG ADC chip. The interface to the ADC is as shown below in Figure 1.

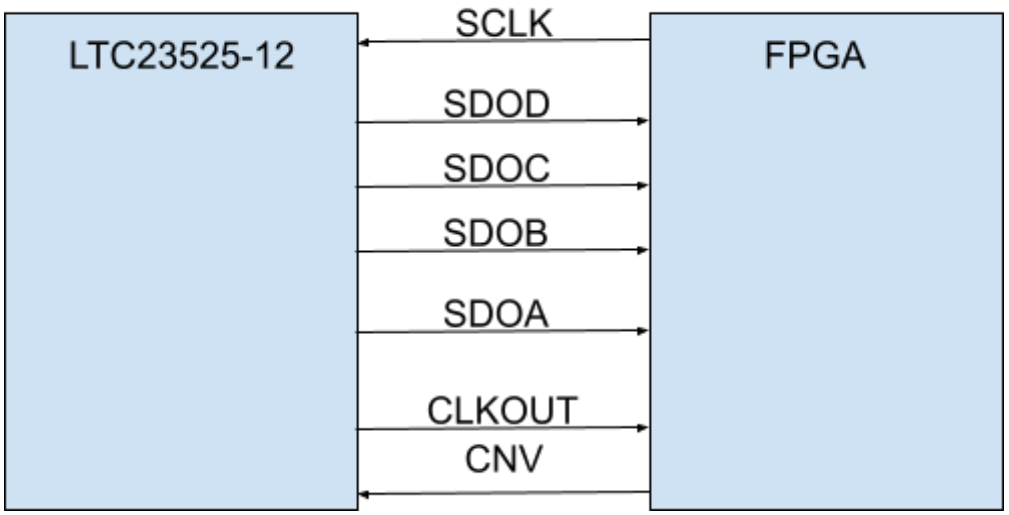

Figure 1 - ADC Interface

The following assumptions are made in the design:

- The chip shall be configured to be in SDR mode (SDR/DDR Pin 23 = GND), such that serial data is only read on a rising edge of the SCLK signal.
- This chip shall be configured such that it uses the CMOS interface, by setting the '*CMOS /LVDS'* pin to low.
- The Module shall be driven off a 100MHz clock.

The timing diagram of the chip in SDR / CMOS mode is shown below in Figure2.

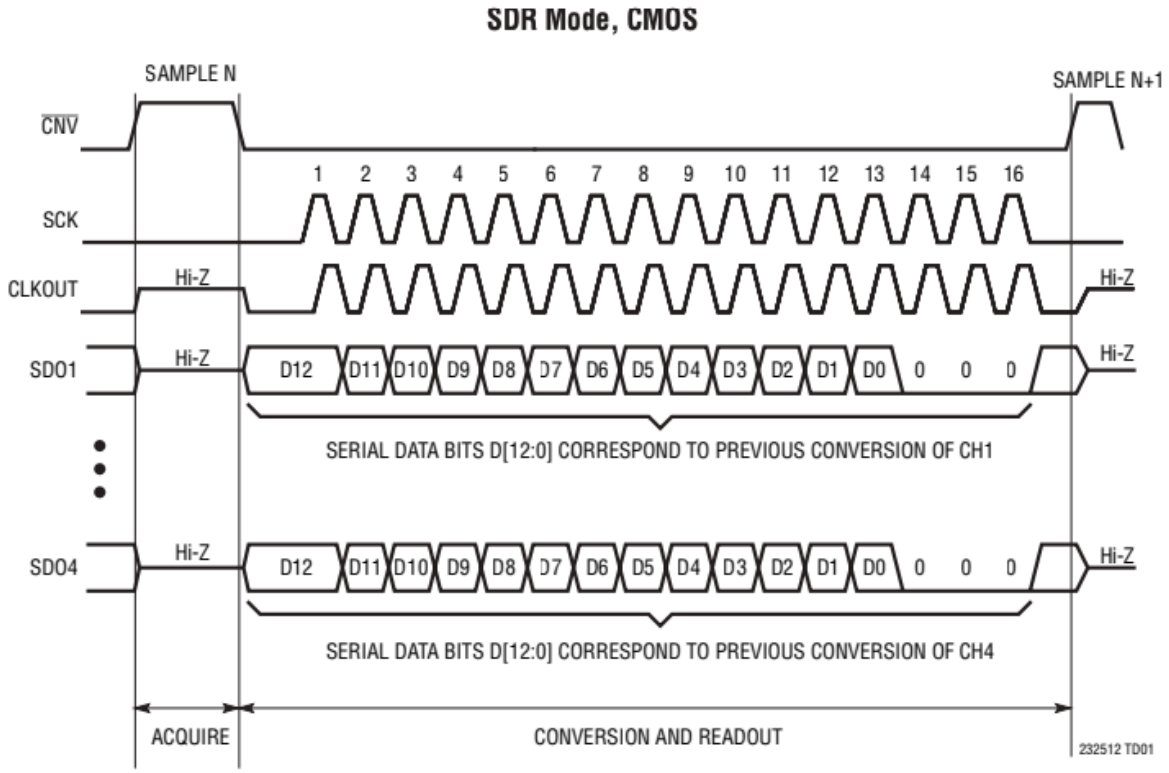

Figure 2 - ADC Timing diagram in CMOS / SDR Mode

A block diagram of the ADC_INTERFACE_LTC2325CUKG module is shown below in FIgure 3.

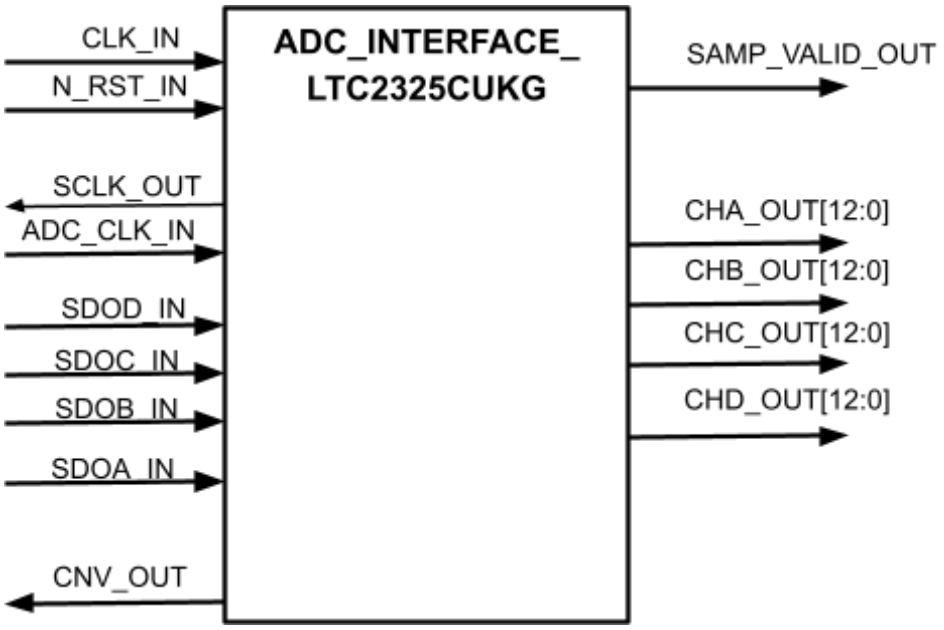

Figure 2 - ADC_INTERFACE_LTC2325CUKG Module Block Diagram

References

[1] - ‘LTC2325-12 - Quad, 12-Bit + Sign, 5Msps/Ch Simultaneous Sampling ADC’ Datasheet, Analog Devices.