Introduction to VLSI - Computer Exercise 2

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- **Lab account: Rg15**
- **Amount of hours invested: 65.**

2 Behavioral Synthesis

1. Which are the two big differentiated modules? Which are the inputs and outputs of each module?

The two big differentiated modules are the datapath (dp) & the controller (cont).

- For controller:

Inputs	**outputs**
Clk, Reset	Memread ,memwrite ,alusrca
zero	Memtoreg, iord, pcen
Op (opcode)	Regwrite, regdst
Funct (function code)	Pcsrc, alusrcb
	alucontrol
	Irwrite

- For datapath:

Inputs	**outputs**
Clk, Reset	zero
memdata	Op
Alusrca, Memtoreg, iord	Funct
Regwrite, regdst, pcen	Adr, writedata
Pcsrc, alusrcb	
Irwrite	
alucontrol	

2. How many different types of FF are defined?

There are 3 different types of FF that are defined : flop, flopen & flopenr.

3. Maximum delay:

(a) What is the maximum delay? Is there a problem of maximum delay? How much is the slack?5 How many gates are involved in this path?

The slack is -1.29 ns. The required maximum delay in the constrains is 2ns and the obtained delay is 3.22ns. so there is a problem because the desired and obtained delay are not equal.

There are 22 gates involved in this path.

(b) What are the clock-to-out time tclk→out and the setup time tsetup of the technology?

Tsetup of the technology is 0.07ns

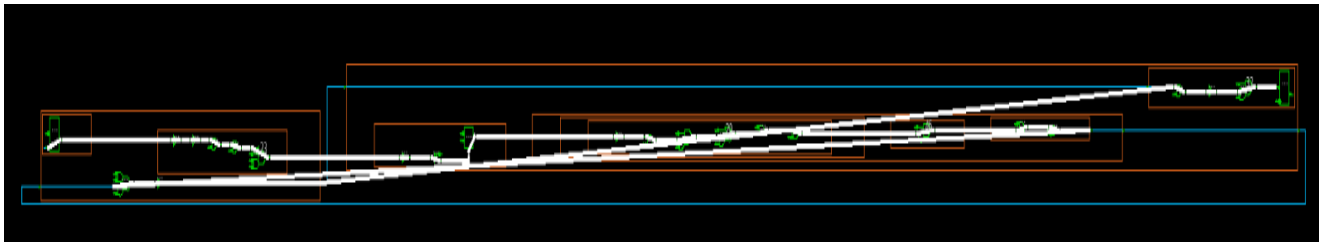
tclk→out is 0.34ns.

(c) Report the critical path.6 Which top-level blocks of the design are part of this path? Include a print-screen of the schematic view with this path highlighted.

From: cont/statelog/state_reg_3_

To: dp/pcreg/q_reg_4_

The top-level blocks of the design in this path are: cont, dp.



4. Minimum delay:

(a) What is the minimum delay? What is the slack?

The minimum delay is 0.31ns.

The slack is 0.34ns.

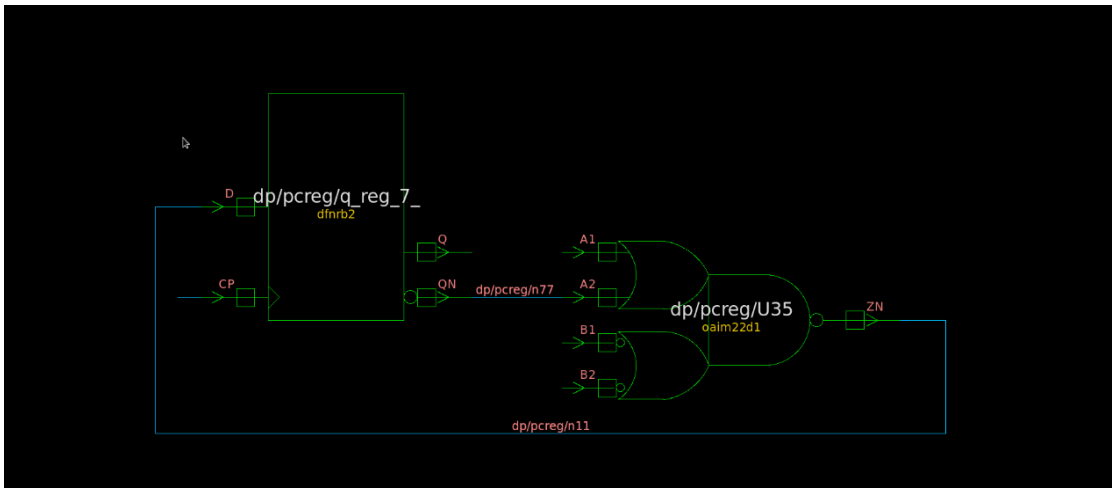
(b) What is the hold time thold of the technology?

The thold is 0.04ns.

(c) How many gates are involved in the min-delay? What's the particularity of this path?

There are 1 gate involved in the min-delay path. The particularity of this path is that it's a loop.

(d) Report the critical path for min-delay. Include a print-screen of the schematic view with this path highlighted.



```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : mips
Version: J-2014.09-SP2
Date   : Thu Jan 10 12:55:00 2019
****************************************

Operating Conditions: tsl18fs120_typ   Library: tsl18fs120_typ
Wire Load Model Mode: enclosed

  Startpoint: dp/pcreg/q_reg_7_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp/pcreg/q_reg_7_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips               4000                  tsl18fs120_typ
  flopenr_WIDTH8     ForQA                 tsl18fs120_typ

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dp/pcreg/q_reg_7_/CP (dfnrb2)            0.00       0.00 r
  dp/pcreg/q_reg_7_/QN (dfnrb2)            0.25       0.25 r
  dp/pcreg/U35/ZN (oaim22d1)               0.06       0.31 f
  dp/pcreg/q_reg_7_/D (dfnrb2)             0.00       0.31 f
  data arrival time                                   0.31

  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dp/pcreg/q_reg_7_/CP (dfnrb2)            0.00       0.00 r
  library hold time                       -0.04      -0.04
  data required time                                 -0.04
  -----------------------------------------------------------
  data required time                                 -0.04
  data arrival time                                  -0.31
  -----------------------------------------------------------
  slack (MET)                                         0.34
```

5. Area:

(a) What is the obtained area? Does it meet the constraint?

The obtained area is : 2261.752

The required area in the constrains is : 2500

The obtained area meets the constrains because it's smaller than the required.

(b) What is the slack? Which constraints influence the area?

The slack is = 2500 - 2261.752 = 238.248

Each library has different area for the standard cells depending on the technology parameters, here for example we used 0.18μm technology.

6. Power:

(a) What is the ratio between dynamic and leakage power? Is this a reasonable result?

Total dynamic power= 6.1273 mW

Total leakage power= 45.4877 nW

$$\frac{6.1273\ \text{mW}}{45.4877\ \text{nW}} = 134702.3481$$

The result is reasonable because we expect the dynamic power to be greater than the leakage power.

2.7 Optimization

8. How does each of the aforementioned changes affect the results? Relate to period, area and power.

changes	period	area	Dynamic power	Leakage power
original	1.93ns	2261.752	6.1273 mW	45.4877 nW
FO: 1->4	1.93ns	2039.242985	6.2992 mW	43.5664 nW
FO: 1->4 Period: 2->10	9.92ns	1861.399024	1.1570 mW	32.3350 nW
FO: 1->4 Period: 2->10 Area: 2500->2000	9.92ns	1862.083914	1.1578 mW	32.2957 nW
FO: 1->4 Period: 2->10 Area: 2500->2000 useUltra: 0->1	9.85ns	1560.657229	1.0420 mW	27.5425 nW

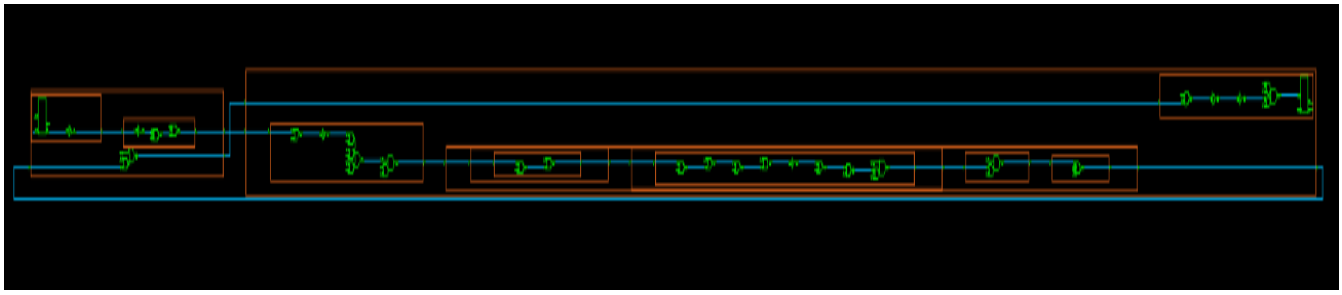
9. Choose a specific logical path between two registers (use Path Slack tool). Explain how and why the synthesis tool changes the gates used to implement this path when we change the constraints.

Present an example of cells that were changed while you modified the constraint file.

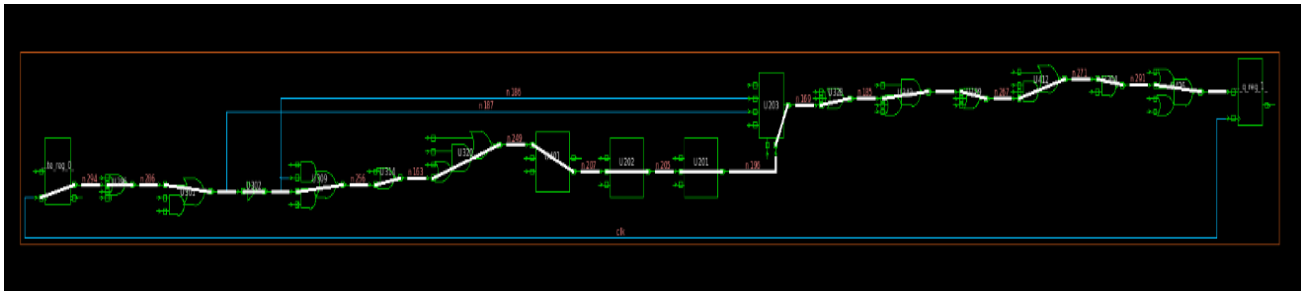
We picked a path between the registers : reg0 and reg1.

From	To
cont/statelog/state_reg_0_/CP	dp/pcreg/q_reg_1_/D

Before changing the constrains:



After changing the constrains:



We can see that due to the change in the area, delay, fanout & useUltra the logical path between the two registers changes and the number of gates is changed (the load capacitance changed), that's because we used a bigger fanout in the constraint and a bigger period, and smaller area.

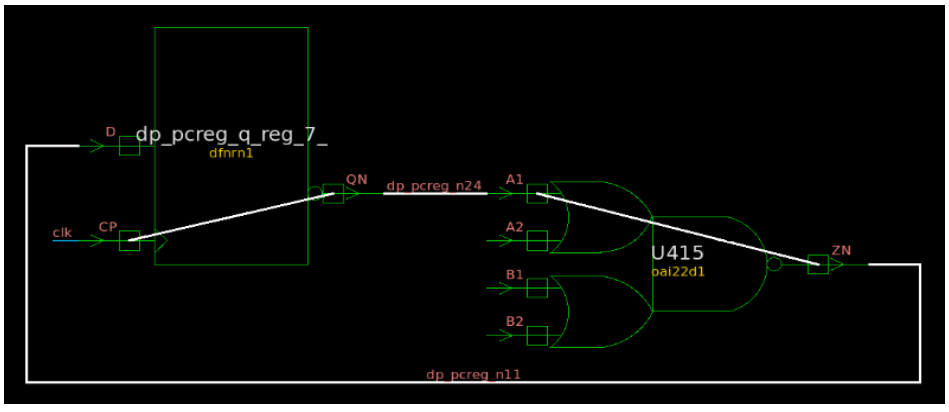
10. What can you say about the hierarchical organization while compiling with Ultra and without it? Why does it improve the results?

compiling with Ultra causes hierarchical organization and that lead to better optimization due to the blocks.

11. Minimum delay:

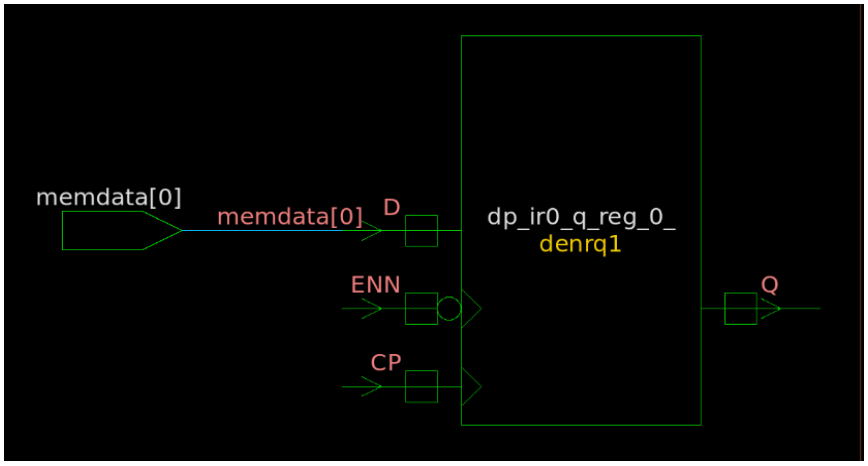
(a) What is the worst slack? Include a print-screen of the schematic view with this path highlighted.

Slack	From	To
0.376591	dp_pcreg_q_reg_7_/CP	dp_pcreg_q_reg_7_/D



(b) What is the best slack? Include a print-screen of the schematic view with this path highlighted.

Slack	From	To
0.590389	memdata[0]	dp_ir0_q_reg_0_/D



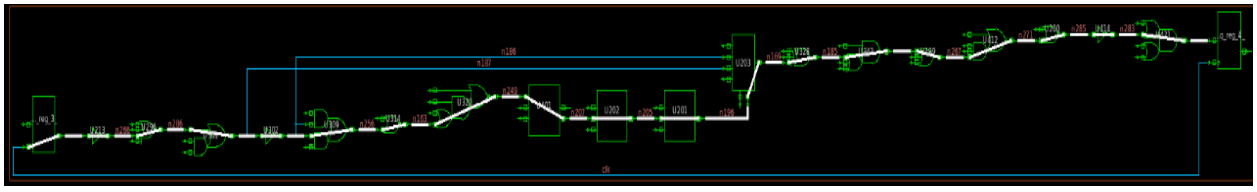
(c) Is it the same critical path as the beginning? Why?

No, the critical path changes due to the change in the constrains because the change affects each path differently and that will lead to a change in the critical path.

12. Maximum delay:

(a) What is the worst maximum delay slack? Include a print-screen of the schematic view with this path highlighted.

Slack	From	To
5.0806	cont_statelog_state_reg_3_/CP	dp_pcreg_q_reg_5_/D



(b) Why is this the critical path? What's the functionality of this path?

It's very logical that this is the critical path, since the PC register is the leftmost thing in the MIPS diagram. The paths will all be loops that start at the PC register and go through various blocks and finally end up back ad the same point to update the next instruction.

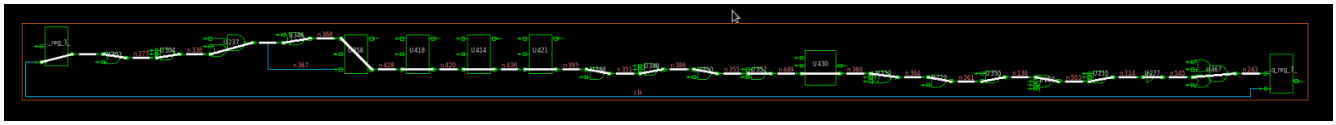
2.8 Fixing maximum delay problems.

The path that is given in the example:

```
From: cont_statelog_state_reg_3_/CP
To: dp_pcreg_q_reg_7_/D
```

is not the critical path because we still get slack = 0.06.

By performing a spectrogram on all the path we get a path that gives us 0.002 slack.



```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : mips
Version: J-2014.09-SP2
Date   : Thu Jan 24 12:22:46 2019
****************************************

Operating Conditions: tsl18fs120_typ   Library: tsl18fs120_typ
Wire Load Model Mode: enclosed

  Startpoint: cont_statelog_state_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp_pcreg_q_reg_7_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips               4000                  tsl18fs120_typ

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  cont_statelog_state_reg_1_/CP (dfnrq1)                  0.00       0.00 r
  cont_statelog_state_reg_1_/Q (dfnrq1)                   0.34       0.34 f
  U303/ZN (nr02d1)                                        0.13       0.48 r
  U304/ZN (nd03d1)                                        0.13       0.61 f
  U237/ZN (oai21d2)                                       0.33       0.94 r
  U346/Z (xr02d1)                                         0.29       1.23 f
  U358/CO (ad01d1)                                        0.30       1.54 f
  U418/CO (ad01d1)                                        0.27       1.80 f
  U414/CO (ad01d1)                                        0.27       2.07 f
  U421/CO (ad01d1)                                        0.28       2.34 f
  U348/ZN (nd02d1)                                        0.08       2.42 r
  U349/ZN (nd03d1)                                        0.12       2.54 f
  U350/ZN (nd02d1)                                        0.10       2.64 r
  U352/ZN (nd03d2)                                        0.08       2.72 f
  U430/CO (ad01d0)                                        0.23       2.95 f
  U210/Z (xr03d1)                                         0.20       3.15 r
  U213/ZN (nd02d0)                                        0.09       3.23 f
  U355/ZN (nd12d1)                                        0.12       3.36 r
  U250/Z (or04d1)                                         0.14       3.50 r
  U215/Z (an03d1)                                         0.19       3.68 r
  U277/ZN (inv0d4)                                        0.07       3.75 f
  U467/ZN (oai22d1)                                       0.15       3.90 r
  dp_pcreg_q_reg_7_/D (dfnrn1)                            0.00       3.90 r
  data arrival time                                                  3.90

  clock clk (rise edge)                                   4.00       4.00
  clock network delay (ideal)                             0.00       4.00
  dp_pcreg_q_reg_7_/CP (dfnrn1)                           0.00       4.00 r
  library setup time                                     -0.10       3.90
  data required time                                                 3.90
  --------------------------------------------------------------------------
  data required time                                                 3.90
  data arrival time                                                 -3.90
  --------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

14. Calculate the maximum delay of this path in the SSSSS corner. Would the circuit (of this path) work under these circumstances?

Tmax=1.2(Tpd(ff)+Tpd(CL)+Tsetup)+Tskew+Tjitter

Tpd(ff)+Tpd(CL)+Tsetup = 0.34+3.56+0.1 = 4 // makes sense that T = 4 as required

Tmax=1.2(4) + 0.8 + 0.2 = 5.8 ns

We can see that Tmax is greater than T that we applied in the constrains (T=4ns) and therefore the circuit won't work.

15. If it does not work, how would you fix the problem? Relate to frequency, skew, changes in the µArch, adding FFs.

Frequency: We can fix the problem by reducing the frequency and that will cause a bigger Tclk which will be greater than Tmax.

Skew: Adding skew to the following flipflop can help by making Tmax smaller than T applied in the constrains. But we must care for the Thold condition as well.

changes in the µArch: making changes to the µArch that will cause a smaller Tmax. (such as adding more levels to the pipeline.)

Adding FFs : We can add flip flops to the path which will make shorter paths and thus smaller Tmax which is smaller than the T applied in the constrains.

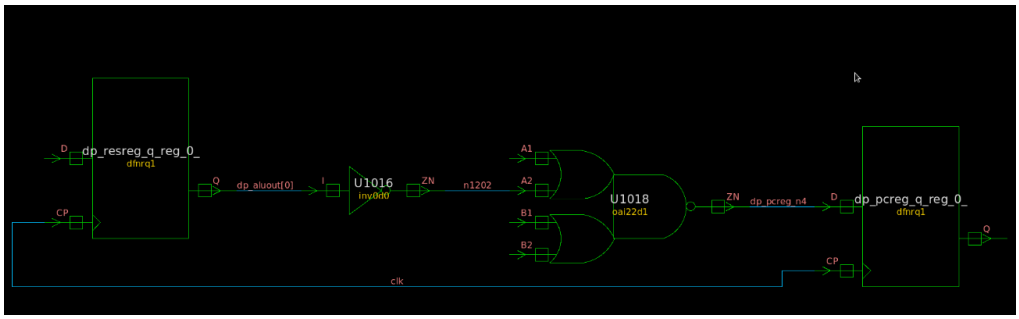
16. Will these techniques solve the maximum delay problem in all critical paths (worst maximum delay path) in our MIPS? If not, what else may be required?

Not all the techniques that were offered will solve the problem in all critical paths, because not all of them affect all the paths in the same way. For example, adding skew to the critical path will help solve the problem but it might damage the Thold condition for another path.

Reducing the frequency (getting a bigger Tclk that is greater than Tmax) will affect every path in the circuit by making Tclk bigger and will solve the problem definitely.

Adding flipflops will affect the whole circuit and fix the problem if we care for all the critical paths.

2.9 Fixing minimum delay problems.



17. Calculate the minimum delay for this path. Would the circuit work under these circumstances?

```
        -max_paths 1
        -sort_by group
Design : mips
Version: J-2014.09-SP2
Date   : Thu Jan 10 18:47:24 2019
****************************************

Operating Conditions: tsl18fs120 typ   Library: tsl18fs120 typ
Wire Load Model Mode: enclosed

  Startpoint: dp_resreg_q_reg_0
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp_pcreg_q_reg_0
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips               4000                  tsl18fs120 typ

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dp_resreg_q_reg_0_/CP (dfnrq1)           0.00       0.00 r
  dp_resreg_q_reg_0_/Q (dfnrq1)            0.27       0.27 r
  U1016/ZN (inv0d0)                        0.07       0.34 f
  U1018/ZN (oai22d1)                       0.11       0.46 r
  dp_pcreg_q_reg_0_/D (dfnrq1)             0.00       0.46 r
  data arrival time                                   0.46

  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dp_pcreg_q_reg_0_/CP (dfnrq1)            0.00       0.00 r
  library hold time                       -0.05      -0.05
  data required time                                 -0.05
  -----------------------------------------------------------
  data required time                                 -0.05
  data arrival time                                  -0.46
  -----------------------------------------------------------
  slack (MET)                                         0.51


***** End Of Report *****
```

Thold+Tskew+Tjitter< 0.8(Tcd(ff)+Tcd(CL))

-0.05+0.8+0.2<0.8(0.27+0.19)

0.95<0.368

We can see that the circuit won't work under these circumstances.

18. If not, how would you fix the problem? Relate to frequency, skew, adding buffers in the path,changes in the µArch, adding FFs.

Frequency: the frequency doesn't affect the minimum delay because the Thold condition doesn't rely on Tclk.

Skew: finding negative skew will fix the problem by making the left side of the equation smaller, such that we don't damage the maximum condition of the other paths, and still meets the hold condition.

Adding buffers: adding buffers to the logic will fix the problem by adding delay to the data but we must care for the Tclk conditions as well.

changes in the µArch: making changes in the architecture will apply the Thold conditions and fix the problem.

Adding FFs: adding FFs doesn't always fix the problem, it might damage it. (because its splits the logic and right side of the equation might get smaller)

2.10 Final synthesis

$$period = \left(15 - \frac{ID_1 + ID_2}{2}\right) = \left(15 - \frac{6+1}{2}\right) = 11.5$$

19. Go through the final netlist (mips.v) and answer:

(a) Give an example of different types of inverters that are used (at least 3).

- Inv0d0
- Nd02d0
- Nd03d1

(b) What is the difference between those inverter gates?

The difference is the number of gates the total gate includes and the delay.

Inv0d0: is an inverter gate with one input and one output and the delay is 0.

Nd02d0: is a nand gate with two inputs and the delay is 0.

Nd03d1: is a nand gate with three inputs and the delay is 1.

20. Submit your final constraints file. Name it constraints rg##.tcl (## is your account number).

Files are submitted.

3.5 Power Grid

23. What is the purpose of power rings and stripes in a chip? Which phenomena do they prevent/reduce?

The purpose of power rings and stripes in a chip is to distribute the power equally. We want the power Vdd to be the same for every cell, but when we route long wires that might not happen because of the IR drop and we won't have equal distribution of Vdd and Vss for every cell. And that will prevent problems in the delay and the performances.

24. Make a table including: length and number of vias of each metal layer.

Metal	Length [μm]	Number of vias
M1	**0**	**1541**
M2	**1.563e+04**	**2415**
M3	**1.650e+04**	**39**
M4	**1.010e+02**	**0**
M5	**0**	**0**
M6	**0**	**0**

25. Can you suggest why the length of M1 is 0 µm?

The length of M1 is 0 µm because it's not included in the standard cell and the synthesis tool doesn't recognize it.

26. Can you suggest why the number of vias increases from top layer to bottom layer?

We use top metals for main and general connections and that's why we need less vias.

That also relate to the fact that increasing the number of vias reduces the resistance and that is good in case we want to make a lot of connections between the cells and that's the reason we use higher metals with a greater number of vias.

3.7 Static Timing Analysis I

27. What is the critical path slack? Is it the same path than in the behavioral synthesis? If not,explain why.

the critical path slack is 3.886. the critical path is from I0/cont_statelog_state_reg_3_ to I0/dp_pcreg_q_reg_3_ . we can see that the path has changes and it's different than the path in the behavioral synthesis and that's due to the optimization and the use of the strip& power rings and in the behavioral synthesis we created a gate level description of the design and we took ideal cases for the skew and delay and in the timing analysis we took more realistic cases in the layout with considering the skew and other factors like the effect of diffusion models of the performance.

```
innovus 11> report_timing -from I0/cont_statelog_state_reg_3_ -to I0/dp_pcreg_q_reg_3_
#####################################################################
#  Generated by:      Cadence Innovus 16.13-s045_1
#  OS:                Linux x86_64(Host ID orion75)
#  Generated on:      Mon Jan 21 14:34:38 2019
#  Design:            top
#  Command:           report_timing -from I0/cont_statelog_state_reg_3_ -to I0/dp_pcreg_q_reg_3_
#####################################################################
Path 1: MET Setup Check with Pin I0/dp_pcreg_q_reg_3_/CP
Endpoint:   I0/dp_pcreg_q_reg_3_/D          (v) checked with  leading edge of
'clk'
Beginpoint: I0/cont_statelog_state_reg_3_/Q (^) triggered by  leading edge of
'clk'
Path Groups: {clk}
Analysis View: SlowView
Other End Arrival Time          0.000
- Setup                         0.145
+ Phase Shift                  11.500
= Required Time                11.355
- Arrival Time                  7.469
= Slack Time                    3.886
     Clock Rise Edge                 0.000
     + Clock Network Latency (Ideal) 0.000
     = Beginpoint Arrival Time       0.000
     +-------------------------------------------------------------------------------------------+
     |           Instance             |     Arc      |   Cell   | Delay | Arrival | Required |
     |                                |              |          |       |  Time   |   Time   |
     |--------------------------------+--------------+----------+-------+---------+----------|
     | I0/cont_statelog_state_reg_3_  | CP ^         |          |       |   0.000 |    3.886 |
     | I0/cont_statelog_state_reg_3_  | CP ^ -> Q ^  | dfnrq1   | 0.339 |   0.339 |    4.224 |
     | I0/U218                        | I ^ -> ZN v  | inv0d0   | 0.282 |   0.620 |    4.506 |
     | I0/U300                        | A4 v -> ZN ^ | nr04d0   | 1.086 |   1.707 |    5.592 |
     | I0/U305                        | B1 ^ -> ZN v | aoi21d1  | 0.359 |   2.065 |    5.951 |
     | I0/U201                        | I v -> ZN ^  | inv0d0   | 0.854 |   2.919 |    6.805 |
     | I0/U312                        | B1 ^ -> Z ^  | aoim22d1 | 0.419 |   3.338 |    7.223 |
     | I0/U317                        | A2 ^ -> ZN v | nr02d0   | 0.120 |   3.457 |    7.343 |
     | I0/U321                        | C2 v -> ZN ^ | oan211d1 | 0.409 |   3.866 |    7.752 |
     | I0/U402                        | A ^ -> CO ^  | ad01d0   | 0.340 |   4.206 |    8.092 |
     | I0/U206                        | B ^ -> CO ^  | cg01d0   | 0.292 |   4.498 |    8.384 |
     | I0/U205                        | B ^ -> CO ^  | cg01d0   | 0.335 |   4.833 |    8.719 |
     | I0/U208                        | S1 ^ -> Z v  | mx04d0   | 0.600 |   5.433 |    9.319 |
     | I0/U329                        | A3 v -> Z v  | xr03d1   | 0.391 |   5.825 |    9.711 |
     | I0/U343                        | B1 v -> ZN ^ | oai31d1  | 0.232 |   6.057 |    9.942 |
     | I0/U203                        | A1 ^ -> ZN v | nr03d0   | 0.126 |   6.183 |   10.069 |
     | I0/U412                        | B3 v -> ZN ^ | aoi31d1  | 0.297 |   6.480 |   10.366 |
     | I0/U204                        | A2 ^ -> ZN v | nr02d0   | 0.127 |   6.607 |   10.493 |
     | I0/U414                        | I v -> ZN ^  | inv0d0   | 0.696 |   7.303 |   11.189 |
     | I0/U423                        | A2 ^ -> ZN v | oai22d1  | 0.165 |   7.469 |   11.354 |
     | I0/dp_pcreg_q_reg_3_           | D v          | dfnrq1   | 0.001 |   7.469 |   11.355 |
     +-------------------------------------------------------------------------------------------+
```

28. Search for the critical path obtained in the behavioral synthesis, what's the delay? Submit the report of this path. Hint: Use report timing -from [starting point] -to [end point].

We took the path we got the worst slack for and the slack is 3.897 and the arrival time is 7.46.

```
innovus 12> report_timing -from I0/cont_statelog_state_reg_3_ -to I0/dp_pcreg_q_reg_5_
#####################################################################
#  Generated by:      Cadence Innovus 16.13-s045_1
#  OS:                Linux x86_64(Host ID orion75)
#  Generated on:      Mon Jan 21 14:35:07 2019
#  Design:            top
#  Command:           report_timing -from I0/cont_statelog_state_reg_3_ -to I0/dp_pcreg_q_reg_5_
#####################################################################
Path 1: MET Setup Check with Pin I0/dp_pcreg_q_reg_5_/CP
Endpoint:   I0/dp_pcreg_q_reg_5_/D          (v) checked with  leading edge of
'clk'
Beginpoint: I0/cont_statelog_state_reg_3_/Q (^) triggered by  leading edge of
'clk'
Path Groups: {clk}
Analysis View: SlowView
Other End Arrival Time          0.000
- Setup                         0.142
+ Phase Shift                  11.500
= Required Time                11.358
- Arrival Time                  7.460
= Slack Time                    3.897
     Clock Rise Edge                0.000
     + Clock Network Latency (Ideal) 0.000
     = Beginpoint Arrival Time      0.000
     +-------------------------------------------------------------------------------------+
     |           Instance            |     Arc      |   Cell   | Delay | Arrival | Required |
     |                               |              |          |       |  Time   |   Time   |
     |-------------------------------+--------------+----------+-------+---------+----------|
     | I0/cont_statelog_state_reg_3_ | CP ^         |          |       |   0.000 |    3.897 |
     | I0/cont_statelog_state_reg_3_ | CP ^ -> Q ^  | dfnrq1   | 0.339 |   0.339 |    4.236 |
     | I0/U218                       | I ^ -> ZN v  | inv0d0   | 0.282 |   0.620 |    4.517 |
     | I0/U300                       | A4 v -> ZN ^ | nr04d0   | 1.086 |   1.707 |    5.604 |
     | I0/U305                       | B1 ^ -> ZN v | aoi21d1  | 0.359 |   2.065 |    5.962 |
     | I0/U201                       | I v -> ZN ^  | inv0d0   | 0.854 |   2.919 |    6.816 |
     | I0/U312                       | B1 ^ -> Z ^  | aoim22d1 | 0.419 |   3.338 |    7.235 |
     | I0/U317                       | A2 ^ -> ZN v | nr02d0   | 0.120 |   3.457 |    7.355 |
     | I0/U321                       | C2 v -> ZN ^ | oan211d1 | 0.409 |   3.866 |    7.763 |
     | I0/U402                       | A ^ -> CO ^  | ad01d0   | 0.340 |   4.206 |    8.104 |
     | I0/U206                       | B ^ -> CO ^  | cg01d0   | 0.292 |   4.498 |    8.396 |
     | I0/U205                       | B ^ -> CO ^  | cg01d0   | 0.335 |   4.833 |    8.730 |
     | I0/U208                       | S1 ^ -> Z v  | mx04d0   | 0.600 |   5.433 |    9.331 |
     | I0/U329                       | A3 v -> Z v  | xr03d1   | 0.391 |   5.825 |    9.722 |
     | I0/U343                       | B1 v -> ZN ^ | oai31d1  | 0.232 |   6.057 |    9.954 |
     | I0/U203                       | A1 ^ -> ZN v | nr03d0   | 0.126 |   6.183 |   10.080 |
     | I0/U412                       | B3 v -> ZN ^ | aoi31d1  | 0.297 |   6.480 |   10.377 |
     | I0/U204                       | A2 ^ -> ZN v | nr02d0   | 0.127 |   6.607 |   10.504 |
     | I0/U414                       | I v -> ZN ^  | inv0d0   | 0.696 |   7.303 |   11.201 |
     | I0/U419                       | A2 ^ -> ZN v | oai22d1  | 0.156 |   7.460 |   11.357 |
     | I0/dp_pcreg_q_reg_5_          | D v          | dfnrq1   | 0.000 |   7.460 |   11.358 |
     +-------------------------------------------------------------------------------------+
```

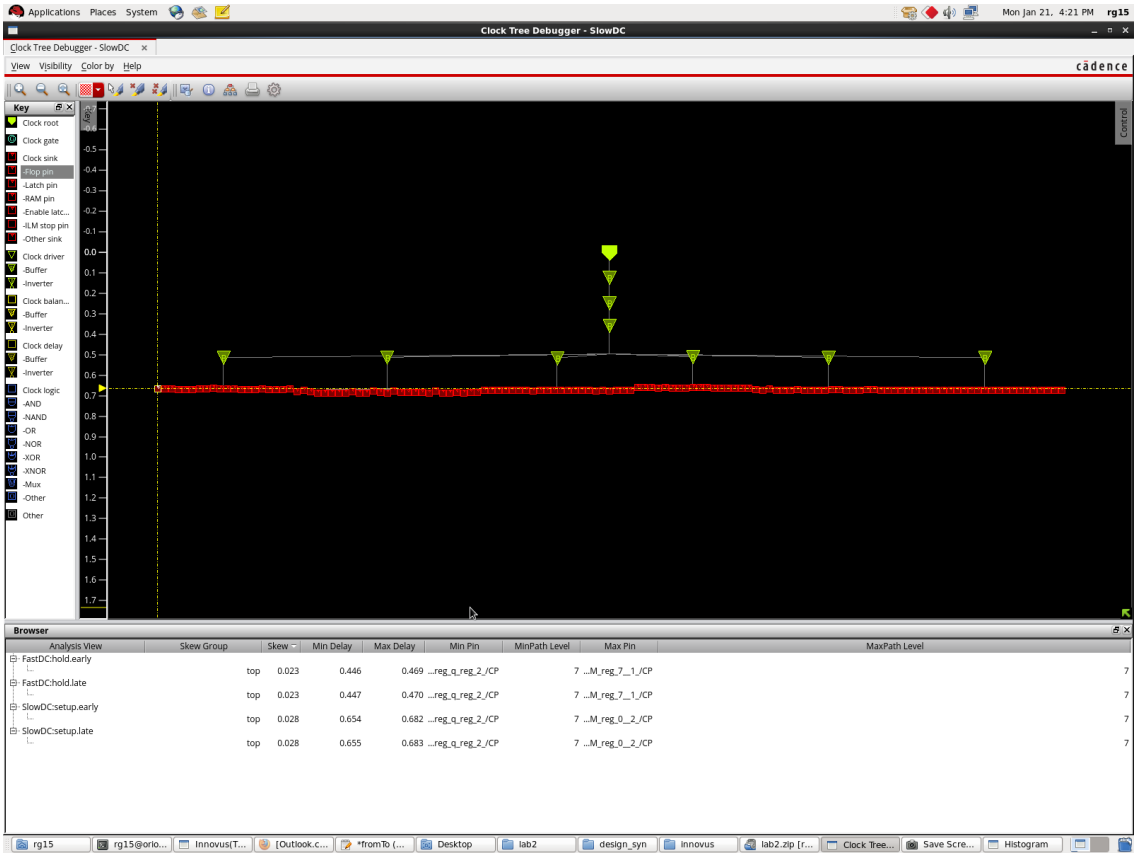
```
Path 8: MET Hold Check with Pin I0/dp_pcreg_q_reg_5_/CP
Endpoint:   I0/dp_pcreg_q_reg_5_/D (v) checked with  leading edge of 'clk'
Beginpoint: I0/dp_ir0_q_reg_3_/Q   (v) triggered by  leading edge of 'clk'
Path Groups: {reg2reg}
Analysis View: FastView
Other End Arrival Time          -0.459
+ Hold                          -0.005
+ Phase Shift                    0.000
= Required Time                 -0.464
  Arrival Time                  -0.092
  Slack Time                     0.372
     Clock Rise Edge                      0.000
     + Source Insertion Delay            -0.459
     = Beginpoint Arrival Time           -0.459
     Timing Path:
     +-----------------------------------------------------------------------------------------------------+
     |               Pin                | Edge |      Net       |  Cell   | Delay | Arrival | Required |
     |                                  |      |                |         |       |  Time   |   Time   |
     |----------------------------------+------+----------------+---------+-------+---------+----------|
     | I5/CIN                           |  ^   | wire_clk       |         |       |  -0.459 |   -0.830 |
     | I0/CTS_cmf_BUF_top_G0_L1_1/I     |  ^   | wire_clk       | bufbd1  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_cmf_BUF_top_G0_L1_1/Z     |  ^   | I0/CTS_34      | bufbd1  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_ccl_BUF_top_G0_L2_1/I     |  ^   | I0/CTS_34      | bufbd1  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_ccl_BUF_top_G0_L2_1/Z     |  ^   | I0/CTS_33      | bufbd1  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_ccl_BUF_top_G0_L3_1/I     |  ^   | I0/CTS_33      | bufbd7  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_ccl_BUF_top_G0_L3_1/Z     |  ^   | I0/CTS_32      | bufbd7  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_cpc_drv_BUF_top_G0_L4_1/I |  ^   | I0/CTS_32      | bufbd7  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_cpc_drv_BUF_top_G0_L4_1/Z |  ^   | I0/CTS_35      | bufbd7  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_ccl_BUF_top_G0_L5_1/I     |  ^   | I0/CTS_35      | bufbd7  | 0.000 |  -0.459 |   -0.830 |
     | I0/CTS_ccl_BUF_top_G0_L5_1/Z     |  ^   | I0/CTS_26      | bufbd7  | 0.000 |  -0.459 |   -0.830 |
     | I0/dp_ir0_q_reg_3_/CP            |  ^   | I0/CTS_26      | denrq1  | 0.000 |  -0.459 |   -0.830 |
     | I0/dp_ir0_q_reg_3_/Q             |  v   | I0/funct[3]    | denrq1  | 0.251 |  -0.207 |   -0.579 |
     | I0/U418/B1                       |  v   | I0/funct[3]    | aoi22d1 | 0.001 |  -0.207 |   -0.578 |
     | I0/U418/ZN                       |  ^   | I0/n276        | aoi22d1 | 0.081 |  -0.126 |   -0.497 |
     | I0/U419/A1                       |  ^   | I0/n276        | oai22d1 | 0.000 |  -0.125 |   -0.497 |
     | I0/U419/ZN                       |  v   | I0/dp_pcreg_n9 | oai22d1 | 0.033 |  -0.093 |   -0.464 |
     | I0/dp_pcreg_q_reg_5_/D           |  v   | I0/dp_pcreg_n9 | dfnrq1  | 0.000 |  -0.092 |   -0.464 |
     +-----------------------------------------------------------------------------------------------------+
     Clock Rise Edge                      0.000
     + Source Insertion Delay            -0.459
     = Beginpoint Arrival Time           -0.459
     Other End Path:
     +-----------------------------------------------------------------------------------------+
     |               Pin                | Edge |    Net     |  Cell   | Delay | Arrival | Required |
     |                                  |      |            |         |       |  Time   |   Time   |
     |----------------------------------+------+------------+---------+-------+---------+----------|
     | I5/CIN                           |  ^   | wire_clk   |         |       |  -0.459 |   -0.087 |
     | I0/CTS_cmf_BUF_top_G0_L1_1/I     |  ^   | wire_clk   | bufbd1  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_cmf_BUF_top_G0_L1_1/Z     |  ^   | I0/CTS_34  | bufbd1  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_ccl_BUF_top_G0_L2_1/I     |  ^   | I0/CTS_34  | bufbd1  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_ccl_BUF_top_G0_L2_1/Z     |  ^   | I0/CTS_33  | bufbd1  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_ccl_BUF_top_G0_L3_1/I     |  ^   | I0/CTS_33  | bufbd7  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_ccl_BUF_top_G0_L3_1/Z     |  ^   | I0/CTS_32  | bufbd7  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_cpc_drv_BUF_top_G0_L4_1/I |  ^   | I0/CTS_32  | bufbd7  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_cpc_drv_BUF_top_G0_L4_1/Z |  ^   | I0/CTS_35  | bufbd7  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_ccl_BUF_top_G0_L5_1/I     |  ^   | I0/CTS_35  | bufbd7  | 0.000 |  -0.459 |   -0.087 |
     | I0/CTS_ccl_BUF_top_G0_L5_1/Z     |  ^   | I0/CTS_26  | bufbd7  | 0.000 |  -0.459 |   -0.087 |
     | I0/dp_pcreg_q_reg_5_/CP          |  ^   | I0/CTS_26  | dfnrq1  | 0.000 |  -0.459 |   -0.087 |
     +-----------------------------------------------------------------------------------------+
```

3.8 Clock Tree Synthesis (CTS)

29. What's the average delay from the clock port to the clock pin of the FFs?

the average delay is 0.670

```
  skew_group top: insertion delay [min=0.655, max=0.683, avg=0.670, sd=0.007], skew [0.028 vs 0.200, 100% {0.655, 0.670, 0.683}] (wid=0.042 ws=0.017) (gid=0.641 gs=0.011)
Clock network insertion delays are now [0.655ns, 0.683ns] average 0.670ns std.dev 0.007ns
Logging CTS constraint violations...
```



30. How many buffers were inserted? What's the purpose of buffers in the CTS?

There were 9 buffers that were inserted. we pre-route the buffers before the main logic placement and routing is completed in order to minimize skew i.e. to achieve zero/minimum skew or balanced skew.

31. What is the average skew between the FFs? Considering the max/min delay timing analysis, would this skew work? Answer quantitatively.

The average skew is 0.028.

According to the results of the critical path:

MAXIMUM CONDITION:

T>(Tpd(ff)+Tpd(CL)+Tsetup)+Tskew

11.5> 0.339+7.121+0.142+0.028

11.5>7.63

We can see that this skew the maximum condition is met.

MINIMUM CONDITION:

Thold+Tskew < (Tcd(ff)+Tcd(CL))

0.028 = Tskew < (Tcd(ff)+Tcd(CL)) – Thold = (T_arrival_time) – Thold = (-0.092)-(-0.005) = -0.087

So we can see that with this skew the minimum condition is not met.

3.9 Static Timing Analysis II

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 SlowView

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  3.921  |  3.921  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   187   |   187   |    0    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 9.632%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.78 sec
Total Real time: 0.0 sec
Total Memory Usage: 1503.351562 Mbytes
innovus 57>
```

3.10 Fill spaces

32. Why are most odd metal layers routed horizontally and most even metal layers routed vertically?

That is done because we want to prevent a case of parallel routing of metals because we want to minimize the cross-section area in order to minimize the capacitance. Placing close metals perpendicularly will help, it will minimize the noise, increase the reliability and decrease the parasitic capacity.

33. Why are VSS and VDD lines placed in an interleaved manner?

VSS and VDD lines are placed in an interleaved manner because we want to connect vdd and vss every cell and and by placing them this way we reduce the area and the distribution between the cells will be better and more effective.

3.12 Power Analysis

```
Begin Power Computation

      ------------------------------------------------------------
      # of cell(s) missing both power/leakage table: 0
      # of cell(s) missing power table: 0
      # of cell(s) missing leakage table: 0
      # of MSMV cell(s) missing power_level: 0
      ------------------------------------------------------------


Starting Calculating power
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT)
 ... Calculating switching power
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 10%
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 20%
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 30%
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 40%
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 50%
 ... Calculating internal and leakage power
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 60%
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 70%
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 80%
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT): 90%

Finished Calculating power
2019-Jan-21 18:20:00 (2019-Jan-21 16:20:00 GMT)
Ended Power Computation: (cpu=0:00:00, real=0:00:00, mem(process/total)=1337.91MB/1337.91MB)

Begin Processing User Attributes

Ended Processing User Attributes: (cpu=0:00:00, real=0:00:00, mem(process/total)=1337.95MB/1337.95MB)

Ended Power Analysis: (cpu=0:00:00, real=0:00:00, mem(process/total)=1337.96MB/1337.96MB)

Begin Static Power Report Generation
*

  8 instances have no static power
** WARN:  (VOLTUS_POWR-2152): Instance PAD_G1 (pv0a) has no static power.

** WARN:  (VOLTUS_POWR-2152): Instance PAD_G3 (pv0c) has no static power.

** WARN:  (VOLTUS_POWR-2152): Instance PAD_I1 (pvda) has no static power.

** WARN:  (VOLTUS_POWR-2152): Instance PAD_I3 (pvdc) has no static power.

** WARN:  (VOLTUS_POWR-2152): Instance Pcornerlr (pfrelr) has no static power.

** WARN:  (VOLTUS_POWR-2152): Instance Pcornerll (pfrelr) has no static power.

** WARN:  (VOLTUS_POWR-2152): Instance Pcornerur (pfrelr) has no static power.

** WARN:  (VOLTUS_POWR-2152): Instance Pcornerul (pfrelr) has no static power.


Total Power
--------------------------------------------------------------------------------------
Total Internal Power:        2.75083252            91.5234%
Total Switching Power:       0.24327122             8.0939%
Total Leakage Power:         0.01150114             0.3827%
Total Power:                 3.00560492
--------------------------------------------------------------------------------------
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total)=1338.25MB/1338.25MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00,
mem(process/total)=1338.35MB/1338.35MB)

Output file is .//top.rpt
```

34. Compare dynamic power obtained here to the dynamic power reported by behavioral synthesis. What can you say about the difference between them? Is it an “apples to apples” comparison even possible?

It’s not an “apples to apples” comparison because of the following differences:

- Physical synthesis:

  Dynamic power: 3.00560492 - 0.01150114 = 2.99410378 mW

- behavioral synthesis:

  dynamic power: 1.0420 mW (after the 4 changes)

we can see that the dynamic power increased because now the synthesis is physical and that changes factors that affect the dynamic power such as capacitance and wiring and frequency.

35. Compare static power (i.e., leakage) obtained here to the static power reported by behavioral synthesis. What can you say about the difference between them?

- Physical synthesis:

  Static Power (leakage power) : 0.01150114 mW

- behavioral synthesis:

  leakage power (leakage power): 45.4877 nW

we can see that the static power increased greatly due to the diffusion leakage that causes greater leakage current.

3.13 Timing Analysis III

```
################################################################################
# Design Stage: PostRoute
# Design Name: top
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: SPEF/RCDB
# Signoff Settings: SI On
################################################################################
AAE_INFO: 1 threads acquired from CTE.
Calculate early delays in OCV mode...
Calculate late delays in OCV mode...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
AAE_INFO: 1 threads acquired from CTE.
Total number of fetched objects 415
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 438,  92.9 percent of the nets selected for SI analysis
End delay calculation. (MEM=1633.66 CPU=0:00:00.7 REAL=0:00:01.0)
Save waveform /tmp/innovus_temp_17192_orion75_rg15_kT1bzb/.AAE_l5i8ld/.AAE_17192/waveform.data...
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 1633.7M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 1633.7M)
Starting SI iteration 2
AAE_INFO: 1 threads acquired from CTE.
Calculate early delays in OCV mode...
Calculate late delays in OCV mode...
Glitch Analysis: View SlowView -- Total Number of Nets Skipped = 0.
Glitch Analysis: View SlowView -- Total Number of Nets Analyzed = 415.
Total number of fetched objects 415
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 438,  0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=1641.7 CPU=0:00:00.0 REAL=0:00:00.0)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 SlowView

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  4.312  |  4.312  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   187   |   187   |    0    |
+--------------------+---------+---------+---------+

+----------------+-----------------------------+------------------+
|                |             Real            |       Total      |
|    DRVs        +-----------------+-----------+------------------|
|                |  Nr nets(terms) | Worst Vio |  Nr nets(terms)  |
+----------------+-----------------+-----------+------------------+
|   max_cap      |      0 (0)      |   0.000   |      0 (0)       |
|   max_tran     |      0 (0)      |   0.000   |      0 (0)       |
|   max_fanout   |      0 (0)      |     0     |      0 (0)       |
|   max_length   |      0 (0)      |     0     |      0 (0)       |
+----------------+-----------------+-----------+------------------+

Density: 9.632%
      (124.796% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 1.44 sec
Total Real time: 1.0 sec
Total Memory Usage: 1545.257812 Mbytes
Reset AAE Options
innovus 59>
```

34. Compare the critical path reported here to the critical path reported by behavioral synthesis. Are they the same path? Are they similar? If they are not the same path, can you find the path delays for each of the two paths reported by the two different tools, and explain the differences?

the critical path reported here isn't the same as the path from the behavioral synthesis

critical path here:

I0/cont_statelog_state_reg_**2**_ → I0/dp/pcreg_q_reg_**2**_

Critical path in behavioral synthesis:

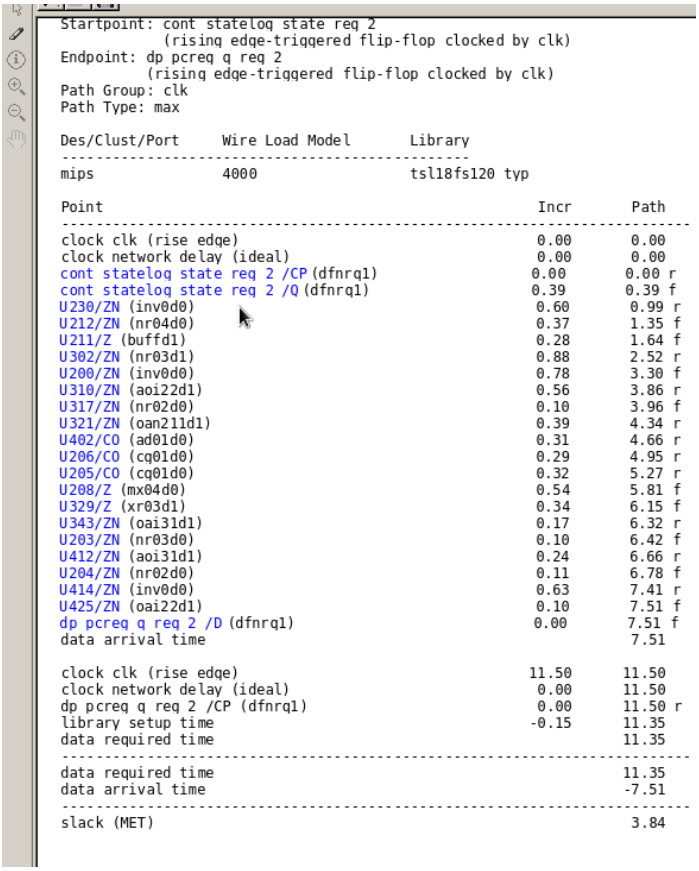
I0/cont_statelog_state_reg_**3**_ → I0/dp/pcreg_q_reg_**5**_

Reports:

- The critical path (I0/cont_statelog_state_reg_**2**_ → I0/dp/pcreg_q_reg_**2**_) report in the **physical synthesis** tool:

```
innovus 60> report_timing -nworst 1
#------------------------------------------------------------
#  Generated by:      Cadence Innovus 16.13-s045_1
#  OS:                Linux x86_64(Host ID orion75)
#  Generated on:      Mon Jan 21 19:13:28 2019
#  Design:            top
#  Command:           report_timing -nworst 1
#------------------------------------------------------------
Path 1: MET Setup Check with Pin I0/dp_pcreg_q_reg_2_/CP
Endpoint:   I0/dp_pcreg_q_reg_2_/D          (v) checked with  leading edge of
'clk'
Beginpoint: I0/cont_statelog_state_reg_2_/Q (v) triggered by  leading edge of
'clk'
Path Groups: {clk}
Analysis View: SlowView
Other End Arrival Time          0.649
- Setup                         0.144
+ Phase Shift                  11.500
= Required Time                12.005
- Arrival Time                  7.693
= Slack Time                    4.312
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  -0.021
     = Beginpoint Arrival Time       -0.021
     +-------------------------------------------------------------------------------+
     |           Instance            |     Arc      |   Cell   | Delay | Arrival |  Required  |
     |                               |              |          |       |  Time   |    Time    |
     |-------------------------------+--------------+----------+-------+---------+------------|
     | I0/cont_statelog_state_reg_2_ | CP ^         |          |       |  -0.021 |     4.291 |
     | I0/cont_statelog_state_reg_2_ | CP ^ -> Q v  | dfnrq1   | 0.432 |   0.412 |     4.724 |
     | I0/U230                       | I v -> ZN ^  | inv0d0   | 0.513 |   0.925 |     5.237 |
     | I0/U212                       | A4 ^ -> ZN v | nr04d0   | 0.106 |   1.031 |     5.343 |
     | I0/FE_OFC1_n151               | I v -> Z v   | buffd1   | 0.292 |   1.323 |     5.635 |
     | I0/U302                       | A1 v -> ZN ^ | nr03d1   | 0.849 |   2.173 |     6.484 |
     | I0/U200                       | I ^ -> ZN v  | inv0d0   | 0.689 |   2.862 |     7.173 |
     | I0/U314                       | B2 v -> ZN ^ | aoi22d1  | 0.362 |   3.223 |     7.535 |
     | I0/U315                       | B1 ^ -> Z ^  | aoim22d1 | 0.332 |   3.556 |     7.867 |
     | I0/U316                       | A ^ -> ZN v  | aoi21d1  | 0.066 |   3.622 |     7.933 |
     | I0/U321                       | C1 v -> ZN ^ | oan211d1 | 0.390 |   4.011 |     8.323 |
     | I0/U402                       | A ^ -> CO ^  | ad01d0   | 0.343 |   4.355 |     8.666 |
     | I0/U206                       | B ^ -> CO ^  | cg01d0   | 0.301 |   4.656 |     8.968 |
     | I0/U205                       | B ^ -> CO ^  | cg01d0   | 0.338 |   4.994 |     9.305 |
     | I0/U208                       | S1 ^ -> Z v  | mx04d0   | 0.604 |   5.597 |     9.909 |
     | I0/U329                       | A3 v -> Z v  | xr03d1   | 0.393 |   5.990 |    10.302 |
     | I0/U343                       | B1 v -> ZN ^ | oai31d1  | 0.277 |   6.268 |    10.579 |
     | I0/U203                       | A1 ^ -> ZN v | nr03d0   | 0.125 |   6.393 |    10.704 |
     | I0/U412                       | B3 v -> ZN ^ | aoi31d1  | 0.340 |   6.733 |    11.044 |
     | I0/U204                       | A2 ^ -> ZN v | nr02d0   | 0.130 |   6.862 |    11.174 |
     | I0/U414                       | I v -> ZN ^  | inv0d0   | 0.680 |   7.542 |    11.854 |
     | I0/U425                       | A2 ^ -> ZN v | oai22d1  | 0.151 |   7.693 |    12.005 |
     | I0/dp_pcreg_q_reg_2_          | D v          | dfnrq1   | 0.000 |   7.693 |    12.005 |
     +-------------------------------------------------------------------------------+
```

- The critical path (I0/cont_statelog_state_reg_**2**_ → I0/dp/pcreg_q_reg_**2**_) report in the **behavioral synthesis** tool:



```
Startpoint: cont_statelog_state_reg_2
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: dp_pcreg_q_reg_2
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
mips               4000                  tsl18fs120_typ

Point                                                  Incr       Path
-----------------------------------------------------------------------
clock clk (rise edge)                                  0.00       0.00
clock network delay (ideal)                            0.00       0.00
cont_statelog_state_reg_2_/CP (dfnrq1)                 0.00       0.00 r
cont_statelog_state_reg_2_/Q (dfnrq1)                  0.39       0.39 f
U230/ZN (inv0d0)                                       0.60       0.99 r
U212/ZN (nr04d0)                                       0.37       1.35 f
U211/Z (buffd1)                                        0.28       1.64 f
U302/ZN (nr03d1)                                       0.88       2.52 r
U200/ZN (inv0d0)                                       0.78       3.30 f
U310/ZN (aoi22d1)                                      0.56       3.86 r
U317/ZN (nr02d0)                                       0.10       3.96 f
U321/ZN (oan211d1)                                     0.39       4.34 r
U402/CO (ad01d0)                                       0.31       4.66 r
U206/CO (cq01d0)                                       0.29       4.95 r
U205/CO (cq01d0)                                       0.32       5.27 r
U208/Z (mx04d0)                                        0.54       5.81 f
U329/Z (xr03d1)                                        0.34       6.15 f
U343/ZN (oai31d1)                                      0.17       6.32 r
U203/ZN (nr03d0)                                       0.10       6.42 f
U412/ZN (aoi31d1)                                      0.24       6.66 r
U204/ZN (nr02d0)                                       0.11       6.78 f
U414/ZN (inv0d0)                                       0.63       7.41 r
U425/ZN (oai22d1)                                      0.10       7.51 f
dp_pcreg_q_reg_2_/D (dfnrq1)                           0.00       7.51 f
data arrival time                                                 7.51

clock clk (rise edge)                                 11.50      11.50
clock network delay (ideal)                            0.00      11.50
dp_pcreg_q_reg_2_/CP (dfnrq1)                          0.00      11.50 r
library setup time                                    -0.15      11.35
data required time                                               11.35
-----------------------------------------------------------------------
data required time                                               11.35
data arrival time                                                -7.51
-----------------------------------------------------------------------
slack (MET)                                                       3.84
```

- The critical path (I0/cont_statelog_state_reg_3_ → I0/dp/pcreg_q_reg_5_) (the one we found in **behavioral synthesis** tool) report inside the **physical synthesis** tool:

```
innovus 62> report_timing -from I0/cont_statelog_state_reg_3_ -to I0/dp_pcreg_q_reg_5_
#####################################################################
#  Generated by:      Cadence Innovus 16.13-s045_1
#  OS:                Linux x86_64(Host ID orion75)
#  Generated on:      Mon Jan 21 19:23:02 2019
#  Design:            top
#  Command:           report_timing -from I0/cont_statelog_state_reg_3_ -to I0/dp_pcreg_q_reg_5_
#####################################################################
Path 1: MET Setup Check with Pin I0/dp_pcreg_q_reg_5_/CP
Endpoint:   I0/dp_pcreg_q_reg_5_/D          (v) checked with  leading edge of
'clk'
Beginpoint: I0/cont_statelog_state_reg_3_/Q (v) triggered by  leading edge of
'clk'
Path Groups: {clk}
Analysis View: SlowView
Other End Arrival Time          0.672
- Setup                         0.144
+ Phase Shift                  11.500
= Required Time                12.028
- Arrival Time                  7.668
= Slack Time                    4.360
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  -0.019
     = Beginpoint Arrival Time       -0.019
     +-------------------------------------------------------------------------------------+
     |           Instance            |     Arc      |   Cell   | Delay | Arrival | Required |
     |                               |              |          |       |  Time   |   Time   |
     |-------------------------------+--------------+----------+-------+---------+----------|
     | I0/cont_statelog_state_reg_3_ | CP ^         |          |       |  -0.019 |    4.341 |
     | I0/cont_statelog_state_reg_3_ | CP ^ -> Q v  | dfnrq1   | 0.424 |   0.404 |    4.764 |
     | I0/U218                       | I v -> ZN ^  | inv0d0   | 0.526 |   0.931 |    5.290 |
     | I0/U300                       | A4 ^ -> ZN v | nr04d0   | 0.357 |   1.288 |    5.647 |
     | I0/U302                       | A2 v -> ZN ^ | nr03d1   | 0.849 |   2.137 |    6.497 |
     | I0/U200                       | I ^ -> ZN v  | inv0d0   | 0.689 |   2.826 |    7.186 |
     | I0/U314                       | B2 v -> ZN ^ | aoi22d1  | 0.362 |   3.187 |    7.547 |
     | I0/U315                       | B1 ^ -> Z ^  | aoim22d1 | 0.332 |   3.520 |    7.880 |
     | I0/U316                       | A ^ -> ZN v  | aoi21d1  | 0.066 |   3.586 |    7.946 |
     | I0/U321                       | C1 v -> ZN ^ | oan211d1 | 0.390 |   3.976 |    8.335 |
     | I0/U402                       | A ^ -> CO ^  | ad01d0   | 0.343 |   4.319 |    8.679 |
     | I0/U206                       | B ^ -> CO ^  | cg01d0   | 0.301 |   4.620 |    8.980 |
     | I0/U205                       | B ^ -> CO ^  | cg01d0   | 0.337 |   4.958 |    9.318 |
     | I0/U208                       | S1 ^ -> Z v  | mx04d0   | 0.604 |   5.562 |    9.921 |
     | I0/U329                       | A3 v -> Z v  | xr03d1   | 0.393 |   5.955 |   10.314 |
     | I0/U343                       | B1 v -> ZN ^ | oai31d1  | 0.277 |   6.232 |   10.592 |
     | I0/U203                       | A1 ^ -> ZN v | nr03d0   | 0.125 |   6.357 |   10.717 |
     | I0/U412                       | B3 v -> ZN ^ | aoi31d1  | 0.340 |   6.697 |   11.057 |
     | I0/U204                       | A2 ^ -> ZN v | nr02d0   | 0.130 |   6.826 |   11.186 |
     | I0/U414                       | I v -> ZN ^  | inv0d0   | 0.680 |   7.506 |   11.866 |
     | I0/U419                       | A2 ^ -> ZN v | oai22d1  | 0.161 |   7.667 |   12.027 |
     | I0/dp_pcreg_q_reg_5_          | D v          | dfnrq1   | 0.001 |   7.668 |   12.028 |
     +-------------------------------------------------------------------------------------+

innovus 63>
```

- The critical path (I0/cont_statelog_state_reg_3_ → I0/dp/pcreg_q_reg_5_) (the one we found in **behavioral synthesis** tool) report inside the **behavioral synthesis** tool:

```
Startpoint: cont_stateloq_state_req_3
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: dp_pcreq_q_req_5
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
mips               4000                  tsl18fs120_typ

Point                                                  Incr       Path
-----------------------------------------------------------------------
clock clk (rise edge)                                  0.00       0.00
clock network delay (ideal)                            0.00       0.00
cont_stateloq_state_req_3_/CP (dfnrq1)                 0.00       0.00 r
cont_stateloq_state_req_3_/Q (dfnrq1)                  0.29       0.29 r
U218/ZN (inv0d0)                                       0.43       0.71 f
U301/ZN (nr04d1)                                       1.32       2.03 r
U305/ZN (aoi21d1)                                      0.19       2.22 f
U201/ZN (inv0d0)                                       1.25       3.47 r
U312/Z (aoim22d1)                                      0.39       3.86 r
U317/ZN (nr02d0)                                       0.11       3.97 f
U321/ZN (oan211d1)                                     0.39       4.36 r
U402/CO (ad01d0)                                       0.31       4.67 r
U206/CO (cq01d0)                                       0.29       4.96 r
U205/CO (cq01d0)                                       0.32       5.29 r
U208/Z (mx04d0)                                        0.54       5.83 f
U329/Z (xr03d1)                                        0.34       6.17 f
U343/ZN (oai31d1)                                      0.17       6.34 r
U203/ZN (nr03d0)                                       0.10       6.44 f
U412/ZN (aoi31d1)                                      0.24       6.68 r
U204/ZN (nr02d0)                                       0.11       6.79 f
U414/ZN (inv0d0)                                       0.63       7.42 r
U419/ZN (oai22d1)                                      0.10       7.52 f
dp_pcreq_q_req_5_/D (dfnrq1)                           0.00       7.52 f
data arrival time                                                 7.52

clock clk (rise edge)                                 11.50      11.50
clock network delay (ideal)                            0.00      11.50
dp_pcreq_q_req_5_/CP (dfnrq1)                          0.00      11.50 r
library setup time                                    -0.15      11.35
data required time                                               11.35
-----------------------------------------------------------------------
data required time                                               11.35
data arrival time                                                -7.52
-----------------------------------------------------------------------
slack (MET)                                                       3.83
```

Summary and explanation of the differences:

(I0/cont_statelog_state_reg_2_ → I0/dp/pcreg_q_reg_2_):

Data Arrival Time:

- **Physical: 7.693**
- **Behavioral: 7.51**

Slack:

- **Physical: 4.312**
- **Behavioral: 3.84**

(I0/cont_statelog_state_reg_3_ → I0/dp/pcreg_q_reg_5_):

Data Arrival Time:

- **Physical: 7.668**
- **Behavioral: 7.52**

Slack:

- **Physical: 4.360**
- **Behavioral: 3.83**

We clearly can see that in the **Physical Synthesis** the values we get are higher as expected, for slack and delay, and that's because the physical synthesis takes into consideration the routing and the lengths of the metals which increase the delay, and not only from a logical point of view like we did in **Behavioral Synthesis**.

35. Compare maximum achievable frequency reported by each of the two tools, and explain any differences. By the way, sometimes this is the most critical, most expensive, and most time consuming question asked by VLSI design teams...

- **Behavioral synthesis:**

According to Section 14, T = (Tclk-out + TpdCL + Tsetup) was calculated with the following values respectively :

T = 0.34+3.56+0.1 = 4ns

$f_{max} = \frac{1}{4} = 250.00\ MHZ$

- **Physical synthesis:**

T = 0.424+(7.668- 0.4224) + 0.144= 7.832 ns

$f_{max} = \frac{1}{7.832} = 127.681\ MHZ$

After the physical synthesis the delay got bigger because all the extra parameters that the tool considered like: wire resistance and delay, diffusion leakage.

36. Submit the .summary file. You may need to unzip it, use the command gunzip #file.

Files are submitted.

3.14

BONUS:

```
------ Design Summary:
Total Standard Cell Number   (cells) : 384
Total Block Cell Number      (cells) : 0
Total I/O Pad Cell Number    (cells) : 292
Total Standard Cell Area     ( um^2) : 16322.88
Total Block Cell Area        ( um^2) : 0.00
Total I/O Pad Cell Area      ( um^2) : 911400.00
```

```
Total Power
-----------------------------------------------------------------------
Total Internal Power:        2.75083252            91.5234%
Total Switching Power:       0.24327122             8.0939%
Total Leakage Power:         0.01150114             0.3827%
Total Power:                 3.00560492
-----------------------------------------------------------------------
```

Total Standard Cell Area $= 16322.88\ \mu m^2$

F $= 127.681\ MHZ = 0.127681$ GHZ

Power $= 3.00560492$ mW

$$FOM = \frac{f}{AxP} = \frac{0.127681\ \text{GHZ}}{16322.88\mu m^2 \cdot (3.00560492\ \text{mW})} = \frac{0.127681 \cdot 10^9\ (s^{-1})}{16322.88(10^{-6}m)^2 \cdot (3.00560492(10^{-3}\ \text{W})} =$$

$$2.602541087210569009785640421188605043546954699766038 2 \times 10^{18}\ \left[\frac{1}{s \cdot m^2 \cdot W}\right]$$