Introduction to VLSI - Computer Exercise 2

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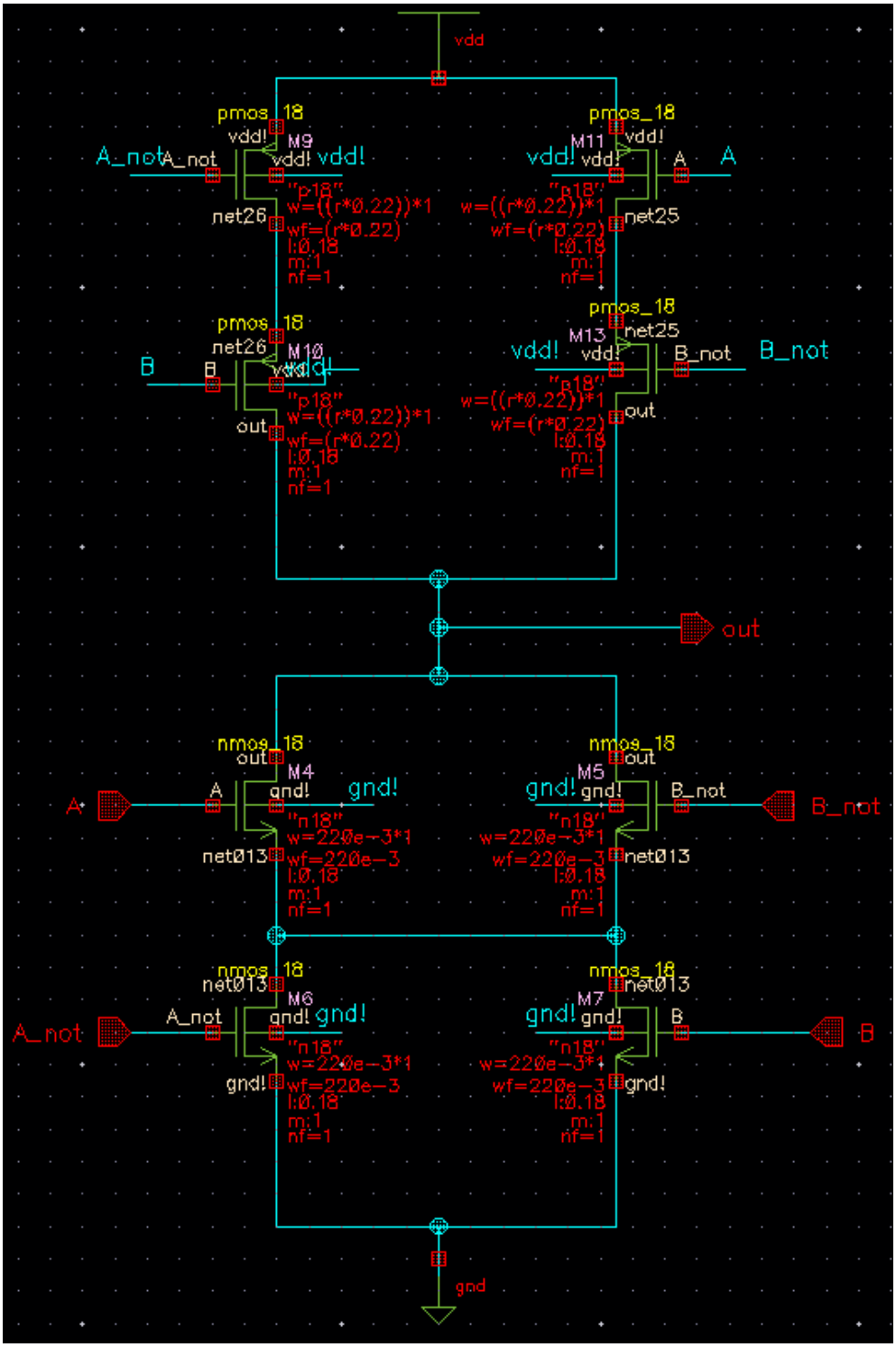
- **Lab account: Rg15**
- **Amount of hours invested: 55.**

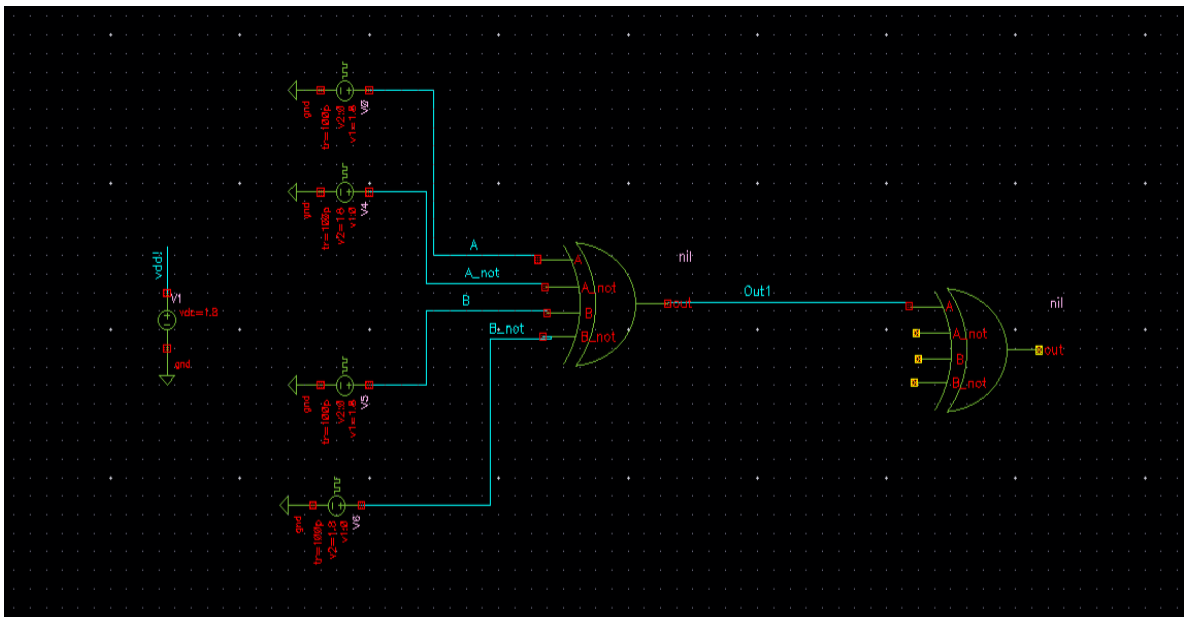
2. Schematic of an XOR2

1.

- **Print screen of the XOR2 schematic:**



- **Print screen of the test circuit (FO1):**



2. Explain how you implemented the input sources and include the output waveform that shows the 4 cases.

We implemented 4 pulse voltage input sources: a, b,$\bar{a}$, $\bar{b}$.

- $\bar{b}$: *the pulse varies between the voltages* $0v$ *and* $1.8v$.
  while $v1$ *is* 0 *and* $v2$ *is* 1.8.
  the rise and fall times are equal and are $100[psec]$.
  the pulse width is $5[nsec]$.
  the pulse period equals $20[nsec]$.
  And the delay time is 10[nsec].

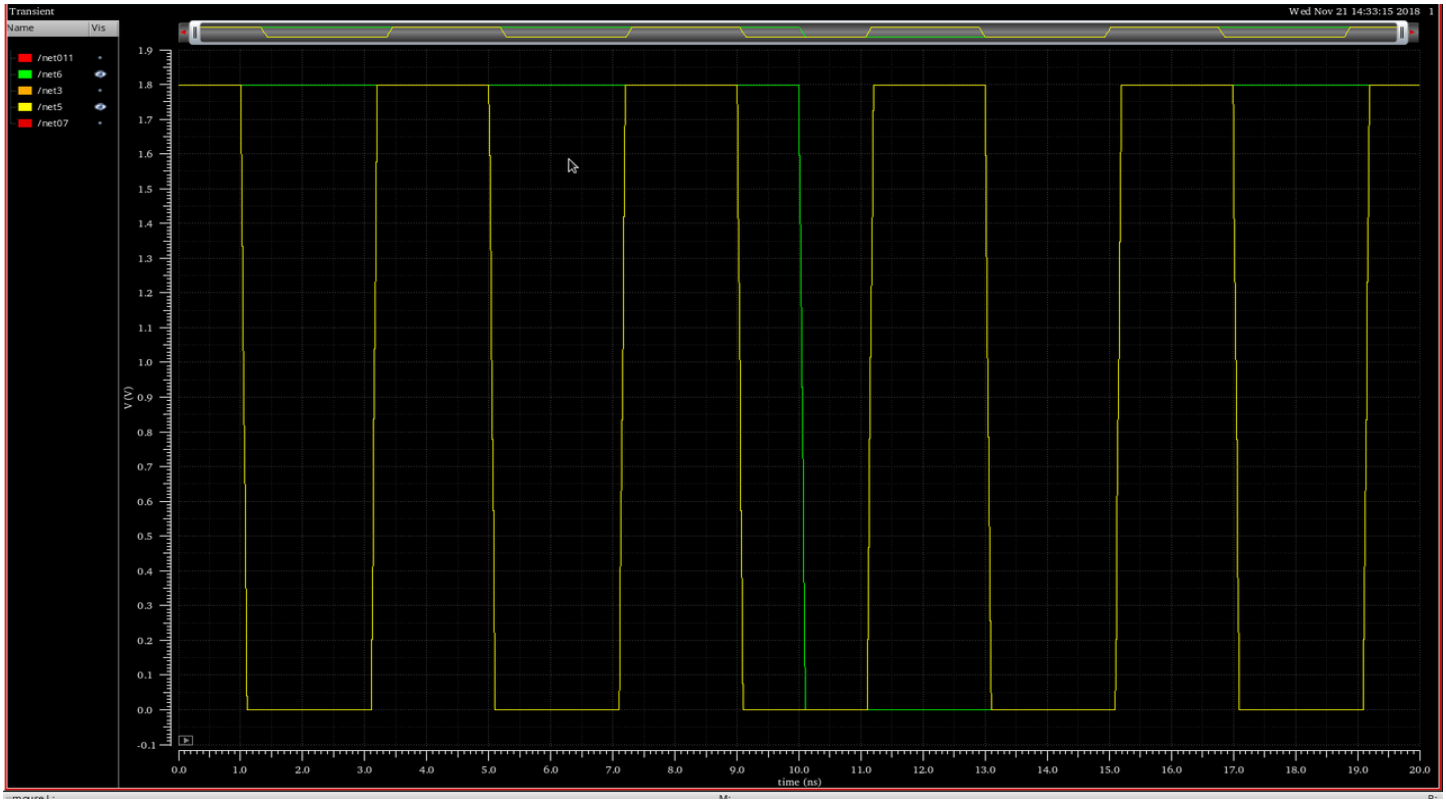
- b: *the pulse varies between the voltages* $1.8v$ *and* $0v$.
  while $v1$ *is* 1.8 *and* $v2$ *is* 0.
  the rise and fall times are equal and are $100[psec]$.
  the pulse width is $5[nsec]$.
  the pulse period equals $20[nsec]$.
  And the delay time is 10[nsec].

- $\bar{a}$: *the pulse varies between the voltages* $0v$ *and* $1.8v$.
  while $v1$ *is* 0 *and* $v2$ *is* 1.8.
  the rise and fall times are equal and are $100[psec]$.
  the pulse width is $2[nsec]$.
  the pulse period equals $4[nsec]$.

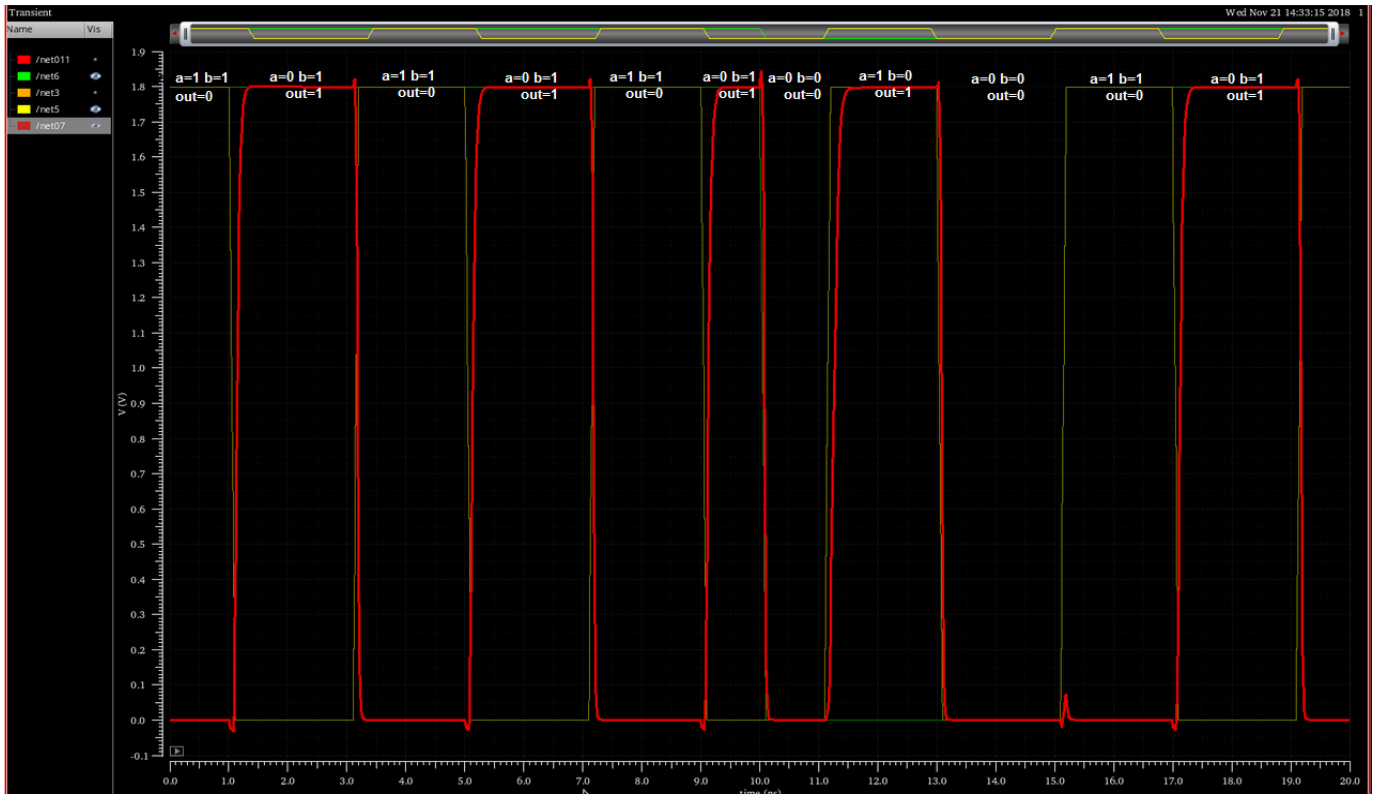
And the delay time is 1[nsec].

- a: *the pulse varies between the voltages* $1.8v$ *and* $0v$.
  while $v1$ *is* 1.8 *and* $v2$ *is* 0.
  the rise and fall times are equal and are $100[psec]$.
  the pulse width is $2[nsec]$.
  the pulse period equals $4[nsec]$.
  And the delay time is 1[nsec].

The inputs: (yellow=a, green=b):



The output:



3. **What's the worst case scenario you should simulate for tprd and tpfd (propagation fall and rise delay respectively)?**

Tpdf:

In order to have a discharge we need two active nmos transistors that are connected serially.

The worst case scenario will be if the transistor that is closer to the gnd switches voltage so that we will have a discharge path, if A=1 & B=0 switch to A=1 & B=1 the transistor that gets the input b which is closer to the gnd will have to discharge more diffusion capacity than if A=1 & B=0 switch to A=0 and B=0.

The same is if A=0 & B=1 switches to A=0 & B=0, that is worse than switching to (A=1 &B=1).

Tpdr:

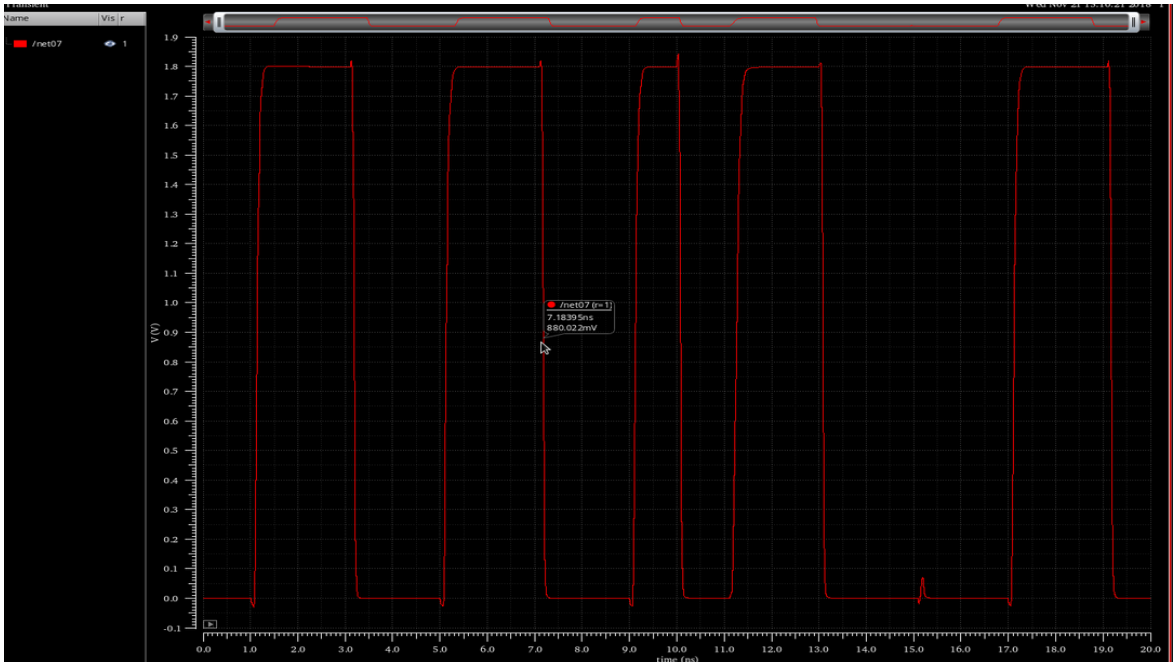
In order to have a charge we need two active pmos transistors that are connected serially. The worst case scenario will be if the transistor that is closer to the vdd switches voltage so that we will have a charge path, if A=0 & B=0 switch to A=1 & B=0 the transistor that gets the input A which is closer to the vdd will have to charge more diffusion capacity than if A=0 & B=0 switch to A=0 and B=1.

The same is if A=1 & B=1 switches to A=0 & B=1, that is worse than switching to (A=1 &B=0).

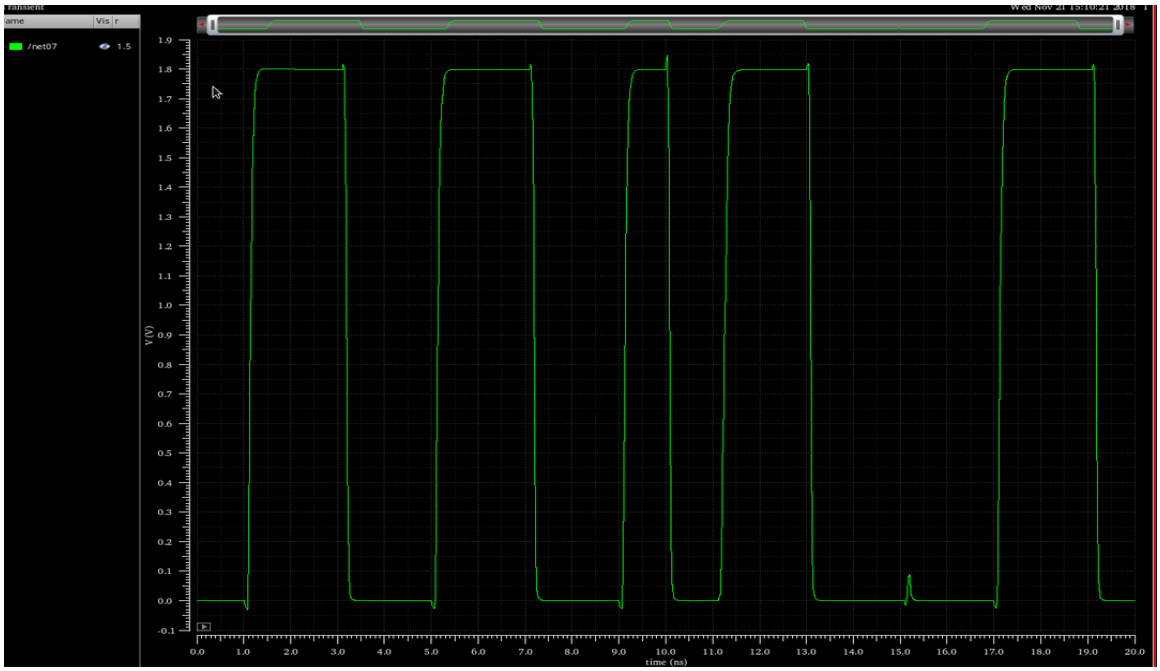
3. Schematic Simulation

4. Simulation waveforms of the parametric sweep of r (submit at least 3 cases).

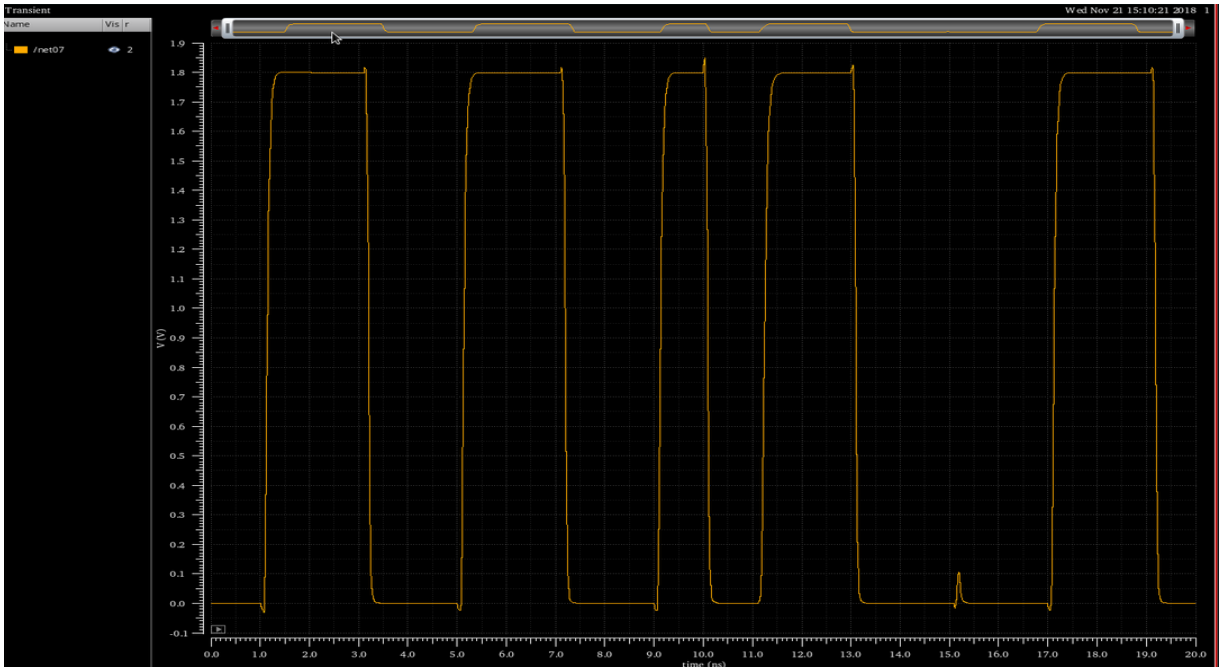
- **R=1 :**



- **R=1.5:**



- **R=2:**



5. Make a table showing tpdf and tpdr for every r.

	r=1	**r=1.5**	**r=2**	**r=2.5**	**r=3**	**r=3.5**	**r=4**
tpdr	82.67E-12	84.21E-12	85.13E-12	82.73E-12	81.24E-12	80.18E-12	79.37E-12
tpdf	33.37E-12	41.61E-12	49.22E-12	56.78E-12	64.53E-12	72.36E-12	80.19E-12
Tavg	58.02E-12	62.91E-12	67.175E-12	69.755E-12	72.885E-12	76.27E-12	79.78E-12

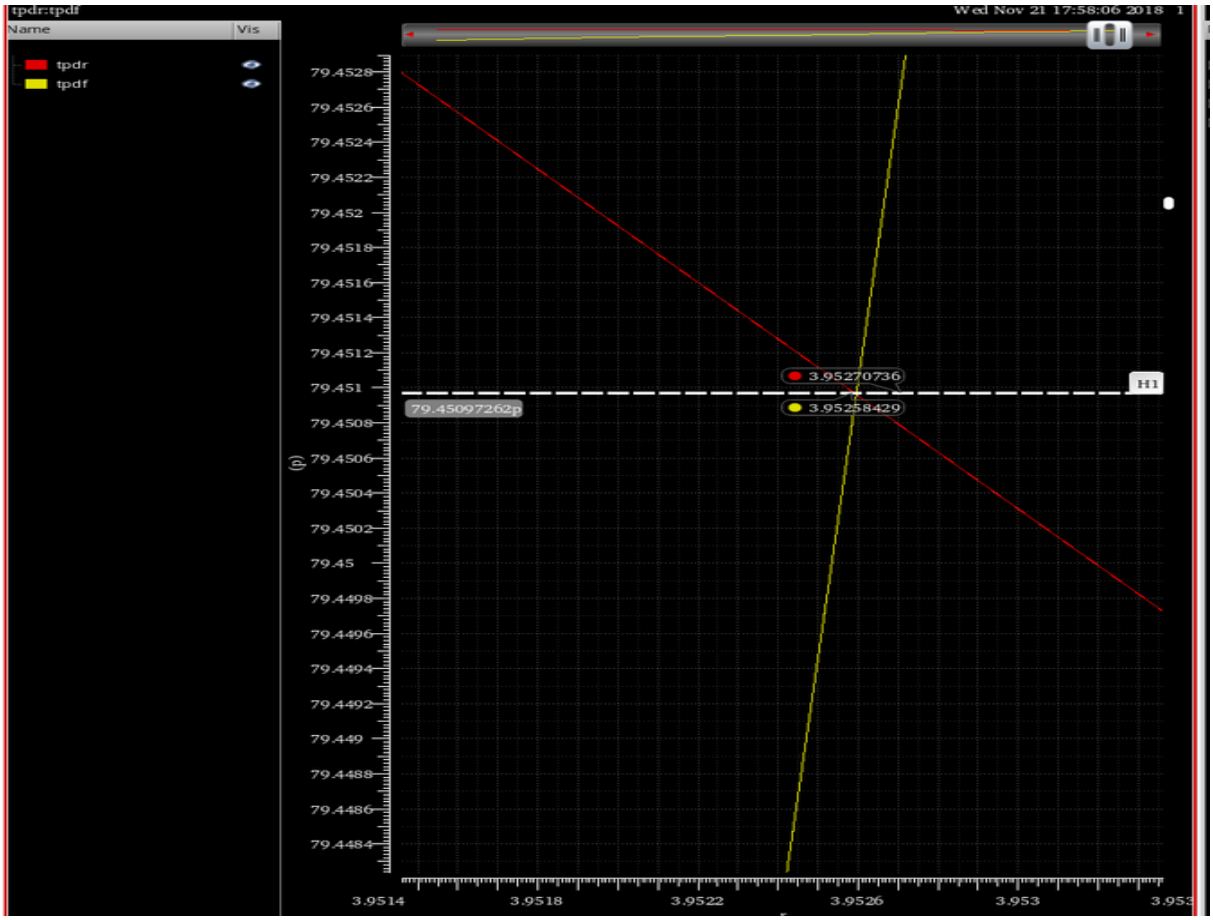
6. Based on the simulations, what is WPopt (WP that results in an optimal/minimum delay)?

The minimum delay equals : $\langle T \rangle = \frac{t_{pdr}+t_{pdf}}{2}$

We can see that the minimum delay is 58.02e-12 at r=1.

Wp= Wn = 0.22[μm].

7. Based on the simulations, what is WPsym (WP that results in a symmetric gate i.e., equal tpdf and tpdr)?



$$t_{pdr} = t_{pdf} \approx 79.4509[p\text{Sec}]\ (for\ \text{optimal r=3.952})$$

We can see that the tpdr graph and the tpdf graph intersect at r=3.952.

$$Wp = 0.22 * r = 0.86944[\mu m]$$

8. How are tpdf and tpdr changed/influenced by the input-order-of-arrival i.e., when the inputs do not arrive simultaneously?

when the inputs don't arrive simultaneously we might get a case of metastability, in a case where a and $\bar{a}$ or b and $\bar{b}$ don't arrive at the same time different transistors will conduct and the output will be indefinite and we might get unwanted discharge and charge path and that will affect the tpdr and tpdf.

In a case where a and b don't arrive at the same time that will affect the logic of the circuit because the output will consider the previous input. And that will affect the discharge path as well as the charge path and also the capacity of the circuit and the tpdr and tpdf.

9. Calculate, theoretically and using the technology parameters, WPopt for minimum propagation delay.

$$T_f = \frac{1}{\frac{C_{ox}\mu_n W_n}{L\ \ 2}(V_{DD}-V_{tn})}\left[Cox \cdot L(W_n + W_p) + C_{ja}X(W_n + 2W_p)\right]$$

$$T_r = \frac{1}{\frac{C_{ox}\mu_p W_p}{L\ \ 2}(V_{DD}-|V_{tp}|)}\left[Cox \cdot L(W_n + W_p) + C_{ja}X(2W_n + 2W_p)\right]$$

$$\langle T\rangle = \frac{T_{pd_r}+T_{pd_f}}{2}$$

$$\langle T\rangle = \frac{1}{2}\left\{\frac{1}{\frac{C_{ox}\mu_n W_n}{L\ \ 2}(V_{DD}-V_{tn})}\left[Cox \cdot L(W_n + W_p) + C_{ja}X(2W_n + 2W_p)\right] + \frac{1}{\frac{C_{ox}\mu_p W_p}{L\ \ 2}(V_{DD}-|V_{tp}|)}\left[Cox \cdot L(W_n + W_p) + C_{ja}X(2W_n + 2W_p)\right]\right\}$$

$$= \frac{1}{2}\left[\frac{2}{\mu_n W_n(V_{DD}-V_{tn})} + \frac{2}{\mu_p W_p(V_{DD}-|V_{tp}|)}\left(\underbrace{\frac{C_{ox}L}{\frac{C_{ox}}{L}}}_{\beta}(W_n + W_p) + \underbrace{\frac{C_{ja}X}{\frac{C_{ox}}{L}}}_{\alpha}(2W_n + 2W_p)\right)\right] =$$

$$= \frac{1}{2}\left\{\beta\left(\frac{2}{\mu_n(V_{DD}-V_{tn})} + \frac{2}{\mu_p \cdot r(V_{DD}-|V_{tp}|)} + \frac{2r}{\mu_n(V_{DD}-V_{tn})} + \frac{2}{\mu_p(V_{DD}-|V_{tp}|)}\right) + \alpha\left(\frac{4}{\mu_n(V_{DD}-V_{tn})} + \frac{4}{\mu_p \cdot r(V_{DD}-|V_{tp}|)} + \frac{4r}{\mu_n(V_{DD}-V_{tn})} + \frac{4}{\mu_p(V_{DD}-|V_{tp}|)}\right)\right\}$$

$$\frac{d\langle T\rangle}{dr} = 0 \rightarrow \beta\left(-\frac{2}{\mu_p(V_{DD}-|V_{tp}|)\cdot r^2} + \frac{2}{\mu_n(V_{DD}-V_{tn})}\right) + \alpha\left(-\frac{4}{\mu_p(V_{DD}-|V_{tp}|)\cdot r^2} + \frac{4}{\mu_n(V_{DD}-V_{tn})}\right) = 0$$

$$\left.\begin{matrix} C_{ja} \rightarrow 0 \\ \alpha \rightarrow 0 \end{matrix}\right\} \rightarrow r = \sqrt{\frac{\mu_n(V_{DD}-V_{tn})}{\mu_p(V_{DD}-|V_{tp}|)}} = \sqrt{\frac{291(1.8-0.5)}{71(1.8+0.42)}} = 1.54$$

$$Wp = 0.22 * r = 0.34[\mu m]$$

10. Table with results of Corners Simulations:

Corner	Tpd_r[pSec]	Tpd_f[pSec]	Tavg
TTTT	82.34[psec]	85.39[psec]	83.865[psec]
TTSS	110[psec]	78.95[psec]	94.475[psec]
TTFF	60[psec]	87.17[psec]	73.585[psec]

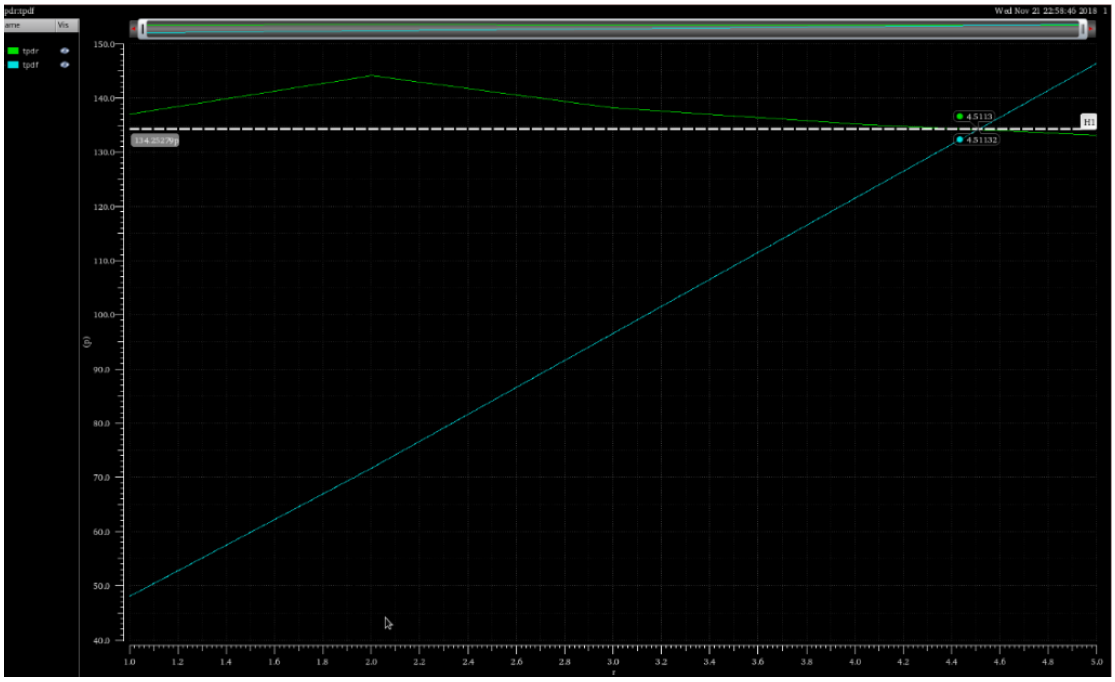
11. Explain why and how tpd changes in every case.

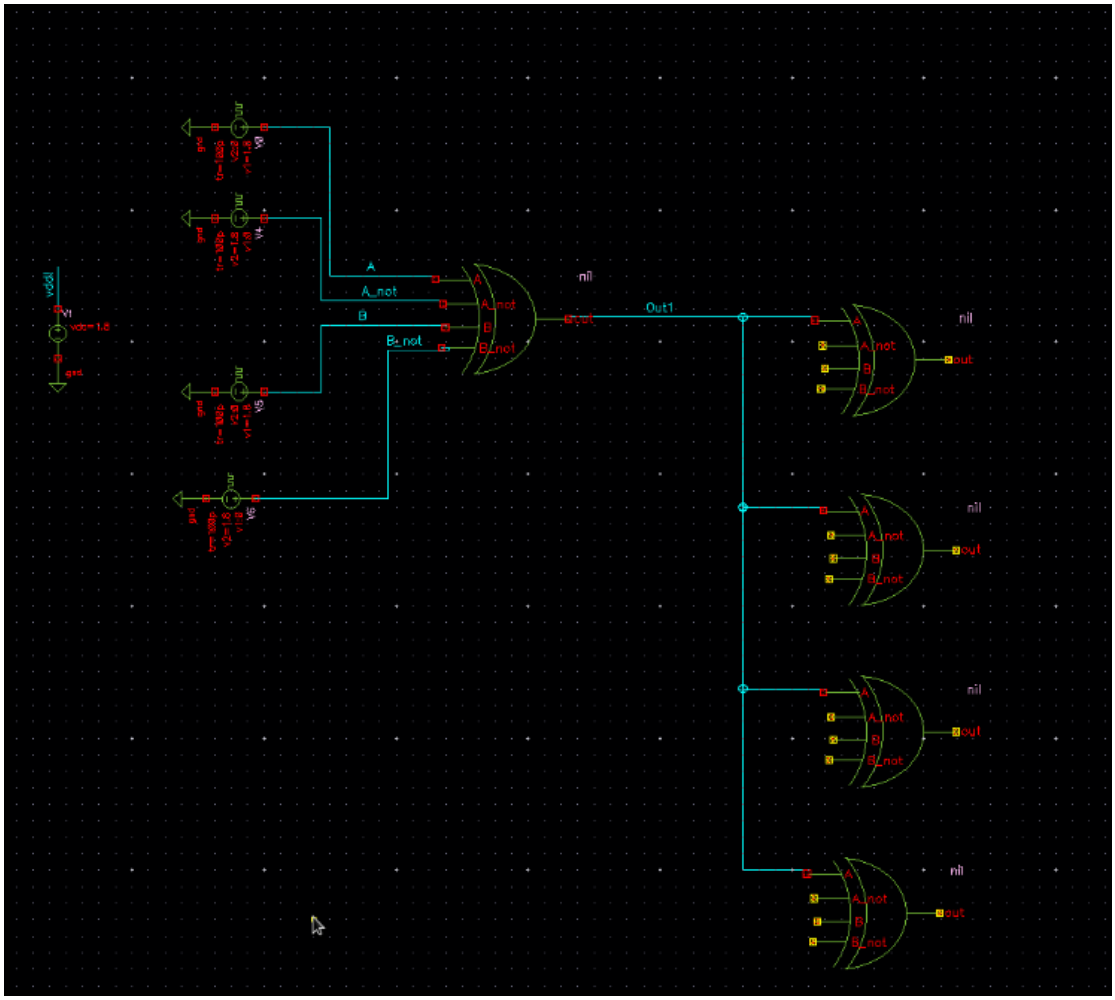
We can see that when the temperature goes up the Tavg increases and we can relate that to the fact the mobility goes down (in this case) and it takes more time to charge.

When the voltage goes up the Tavg decreases because the current increases with the voltage.

12. Simulation results of FO4.

For roptimal=4.5114 for symmetry purposes, we get
Tpdr[pSec]≈Tpdf[pSec]=134.2527[pSec]





13. Explain why and how tpd changes. Relate to the linear delay model (logical effort).

Cout (the load capaticance) of the first Xor changed, and since τ=RC, the delay increase.

Q.14 What is the maximum frequency that can be achieved in a synchronous circuit as Fig. 10(b) if tsetup = 0 and tclk–out = 0?

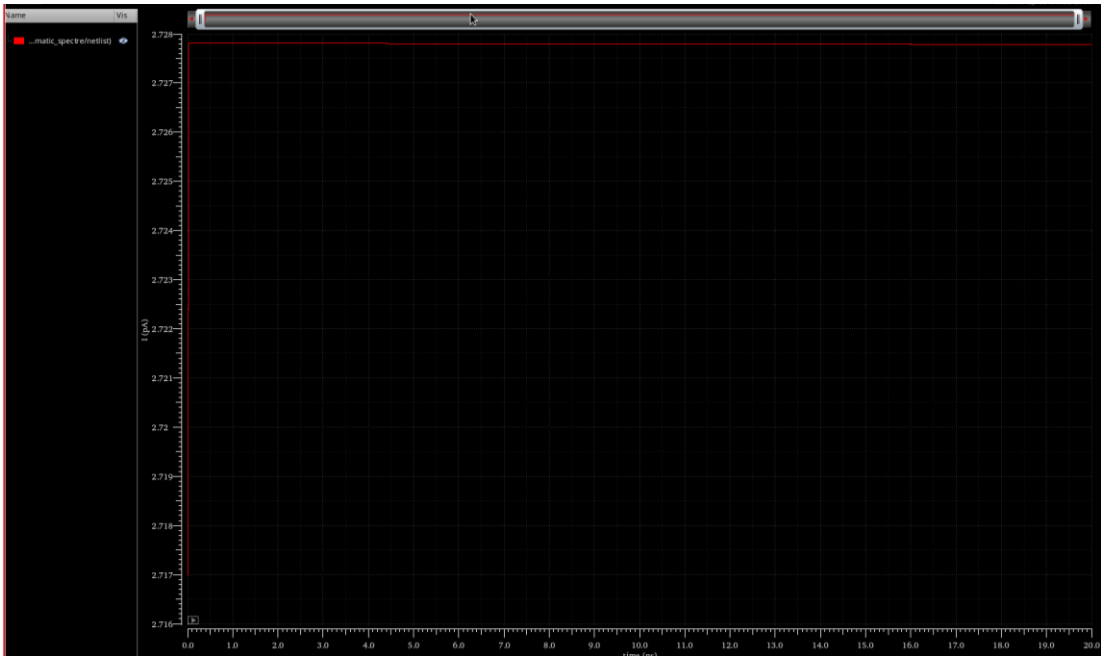
Fmax=1/Tmin
Tmin=Tpd(FF0)+Tpd(logic)+Tsetup(FF1)=Tpd(logic)=2*Tpd(xor)=
2*134.2527=268.5[pSec]
Fmax=3.72[GHz]

3.5) Power Estimation.

15&16:

- **3.5.1) Static dissipation:**

Simulation:
Static Dissipation: (the upper graph is I_{static}) and the lower graph is:
$P_{static} = I_{static} \cdot Vdd$ = 2.728[pA]·1.8[v]=4.896 pW



- **3.5.2) Dynamic:**

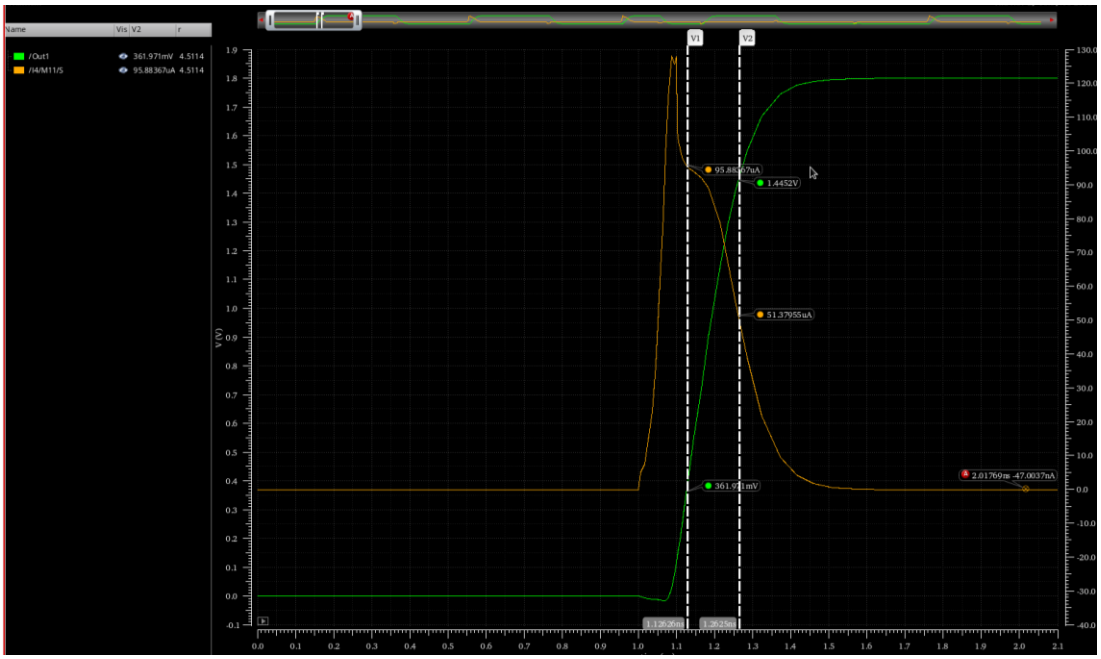
$$p_{dynamic} = \alpha \cdot C_L \cdot vdd^2 \cdot f$$

$$C_L = \underset{Fanout=4}{4 \cdot} C_{ox} L_{\min}(2w_{\min} + 2b \cdot w_{\min}) = \underset{b=\frac{\mu_n}{\mu_p}=4}{\underset{Fanout=4}{4 \cdot}} C_{ox} L_{\min}(2w_{\min} + 2 \cdot 4 \cdot w_{\min}) = 4C_{ox} L_{\min}(10w_{\min})$$

$$= \underset{w_{\min}=W_N}{4C_{ox} L_{\min}(10W_N)} = 4 \cdot (6.81 \cdot 10^{-3}[f])(0.18 \cdot 10^{-6}[m])(10 \cdot 0.22[\mu m]) = 1.079 \cdot 10^{-14}[F]$$

$$\rightarrow p_{dynamic} = \alpha \cdot C_L \cdot vdd^2 \cdot f = \frac{1}{2} \cdot (1.079 \cdot 10^{-14})(1.8)^2 (4.67 \cdot 10^9) = 81.699[\mu W]$$

- **3.5.3) Short Circuit:**



At 20% change of the output the current is: 95.88367 µA
At 80% change of the output the current is: 51.379 µA

The average current: $\frac{95.88367+51.379}{2} = 73.63$ µA

$P_{short-cuircit} = I_{short-cuircit} \cdot vdd = 73.63 \cdot 1.8 = 132.534$ µW

17. What is the best strategy to reduce the dynamic power? Relate to the parameters CL, V 2 DD and f, and to scaling. What are the pros and cons of each strategy?

Pdynamic = α*CLV* $2VDD^2$*f
From this equation we can see that the dynamic power can be controlled by the parameters CL,VDD and f. let's examine how:

- by reducing CL we reduce the dynamic power and the parameters of the transistor (we can change W_N but L is technology constant). finally, we will reach the limit of the technology where the dimension of the transistor can't get smaller due to the technology we're using. the result of that will be that we will get weaker transistors.

- by reducing VDD we reduce the dynamic power, and due to the exponent, the dynamic power is reduced noticeably. However, that affects the current as well, the current reduces and that causes the tpdr and tpdf to increases so that will impact the performance of the circuit. In addition, we can reduce the dynamic power by controlling vdd in different areas, we can use different levels of Vdd and we can also locally turn off VDD.
- by reducing f we reduce the dynamic power but on the other side that affects the T(CLK) of the circuit and the throughput. So the performance of the transistors will get worse and slower.

- we can reduce the dynamic power by scaling. We change the width of the channel and that will reduce the capacitance(CL) and therefore the dynamic power, but that will weaken the transistors because reducing the width causes lower current and thus higher tpdr and tpdf.

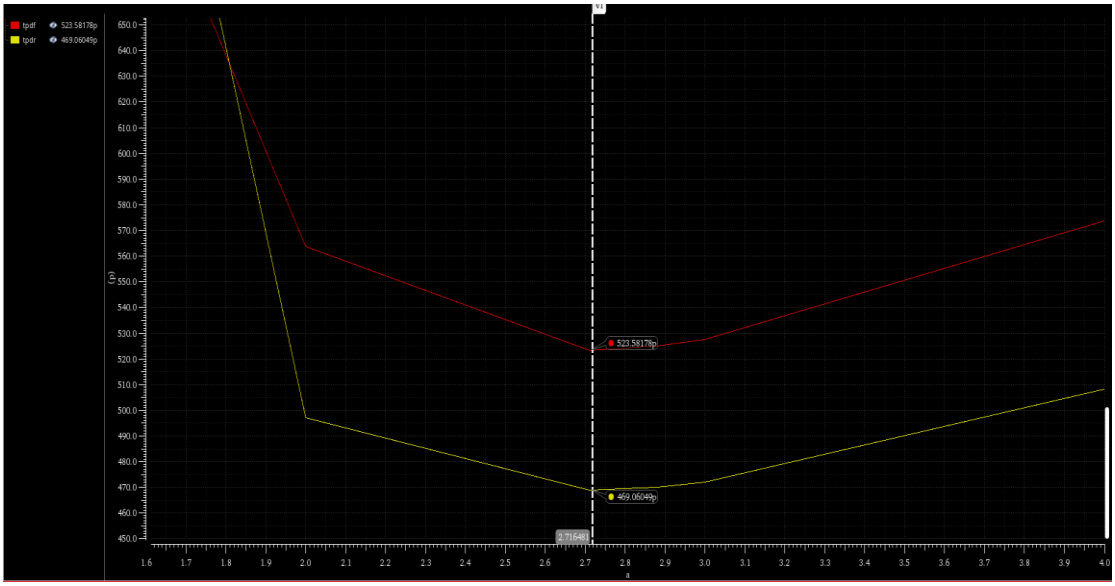
18. How can you reduce the short circuit power dissipation?

we can reduce the short circuit power dissipation by reducing the voltage (VDD) or the current in the circuit. And we can reduce the current for example by increasing the threshold voltage or by changing K or W. and that clearly will affect the performance of the transistors.
In addition, we can reduce it by controlling Vt. Using transistors with higher Vt will reduce the time that the input will be in voltage between VDD-VTp and VTn and therefore the short circuit power dissipation will reduce.

3.6 Sizing

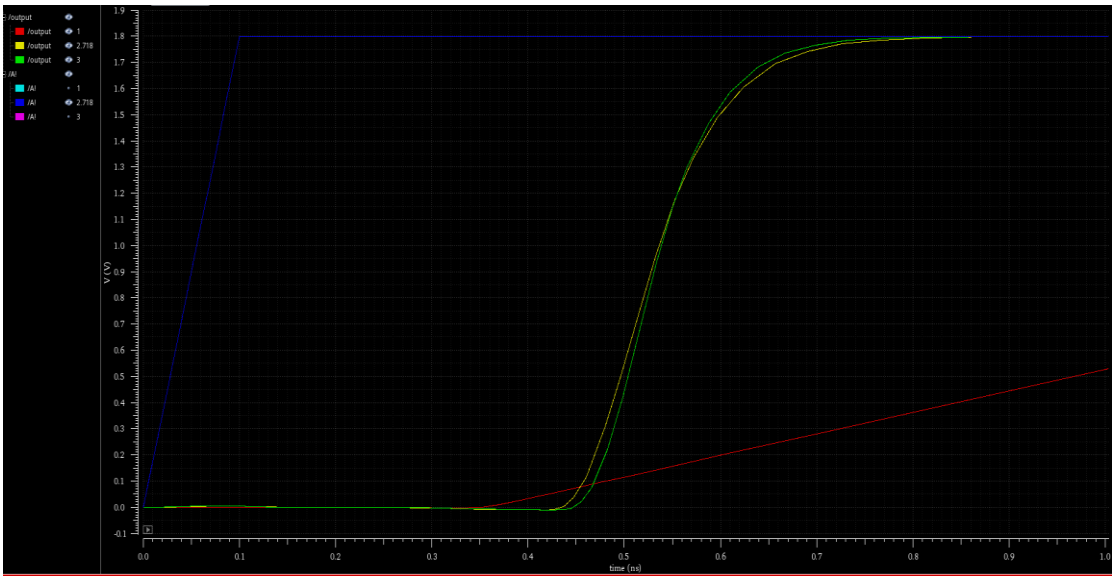
19. What's the optimal a (a_{opt}) for minimum delay?

We got that $a_{opt} = 2.716481$, and that's a good approximation of the anticipated earlier number that we're expecting according to the theoretical proof we learned in Electronic Switching Circuits.



20. Simulation results (include just 3 cases, including aopt). Explain what happens when a = 1.

Input = Blue.
Output: Yellow (a=2.718), Green (a=3), Red (a=1)



We can see that when a=1 the graph is linear, and the change is very slow.

3.7 Buffer insertion

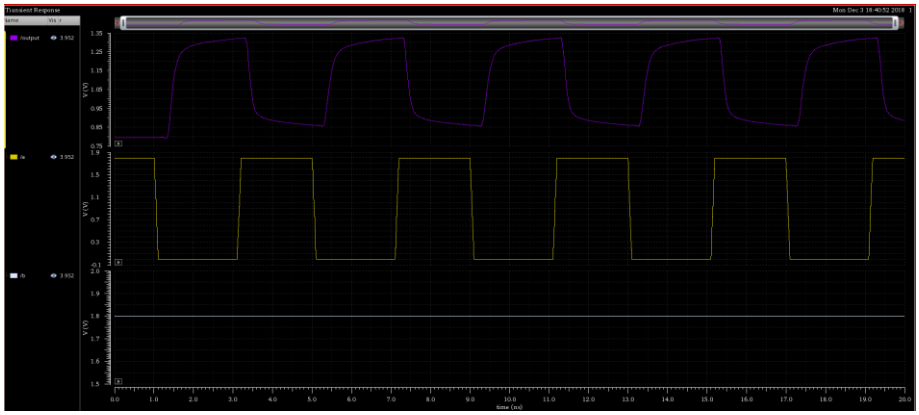
21. What is the optimal N_{opt}?

Theoretically (from Switching Circuits Course):

$$N_{opt} = ln\left(\frac{Cout}{cin}\right) = ln\left(\frac{Cout}{a \cdot Cox \cdot L \cdot (Wn+Wp)}\right) = ln\left(\frac{Cout}{a \cdot Cox \cdot L \cdot (Wn+2\times b\times Wn)}\right) =$$
$$ln\left(\frac{100}{(2.6)\cdot(8.5)\cdot(0.18)\cdot(0.22\times 1+2\times 2\times 0.22)}\right) = 3.129$$

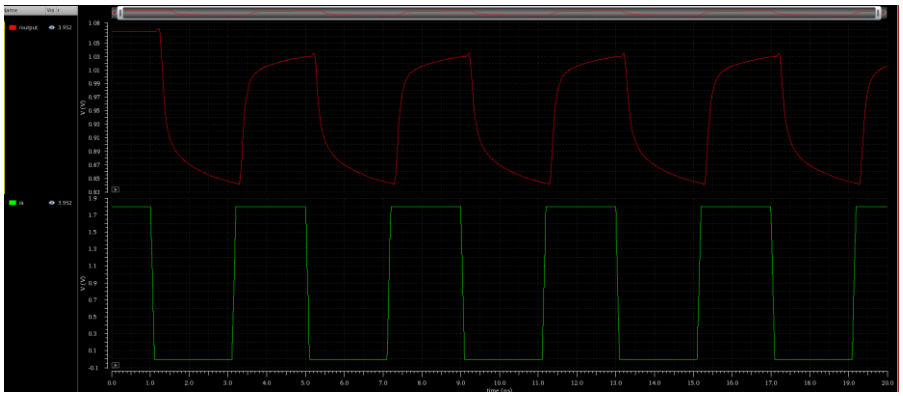
22. Simulation results (include just 3 cases).

For 4 inverters:



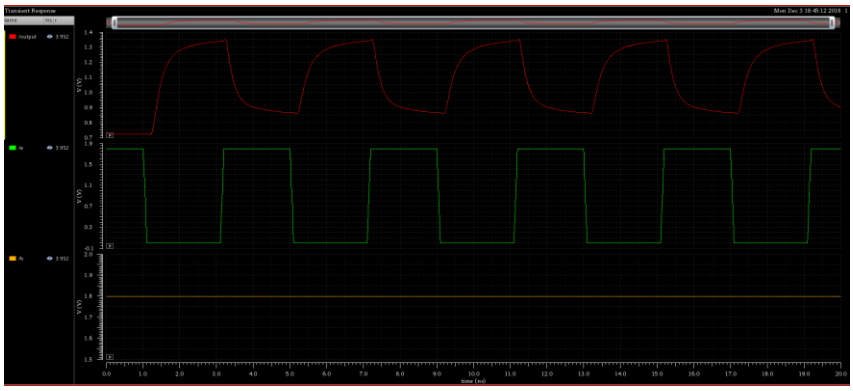
Tpdr	346.6[psec]
Tpdf	630.6[psec]

For 3 inverters:



Tpdr	218.7[psec]
Tpdf	511.8[psec]

For 2 inverters:

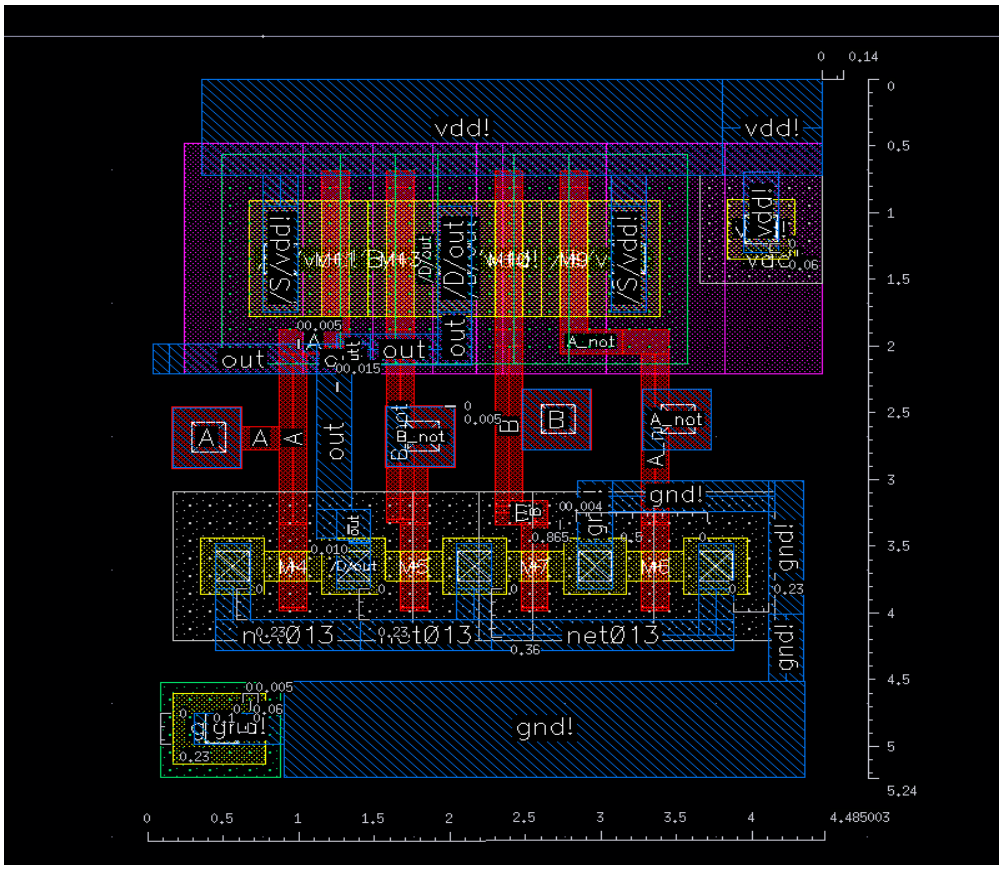


Tpdr	306.8[psec]
Tpdf	903.8[psec]

The minimum delay is achieved by taking 3 inverters as expected.

4 Layout

23. Layout print-screen with a rule on each axis showing the cell's dimensions.



24. What is the total area of your cell?

The total area= width*area=5.24*4.485003=23.5 μm^2

25. Explain how does the placement of one NMOS (PMOS) above and aside the other affects the gate performance. Which parameters are changed?

Placing a 2 NMOS transistors aside each other is more efficient that placing them above each other. That way, by connecting the source of one NMOS to the drain of other NMOS will save us two contacts and extra metal.

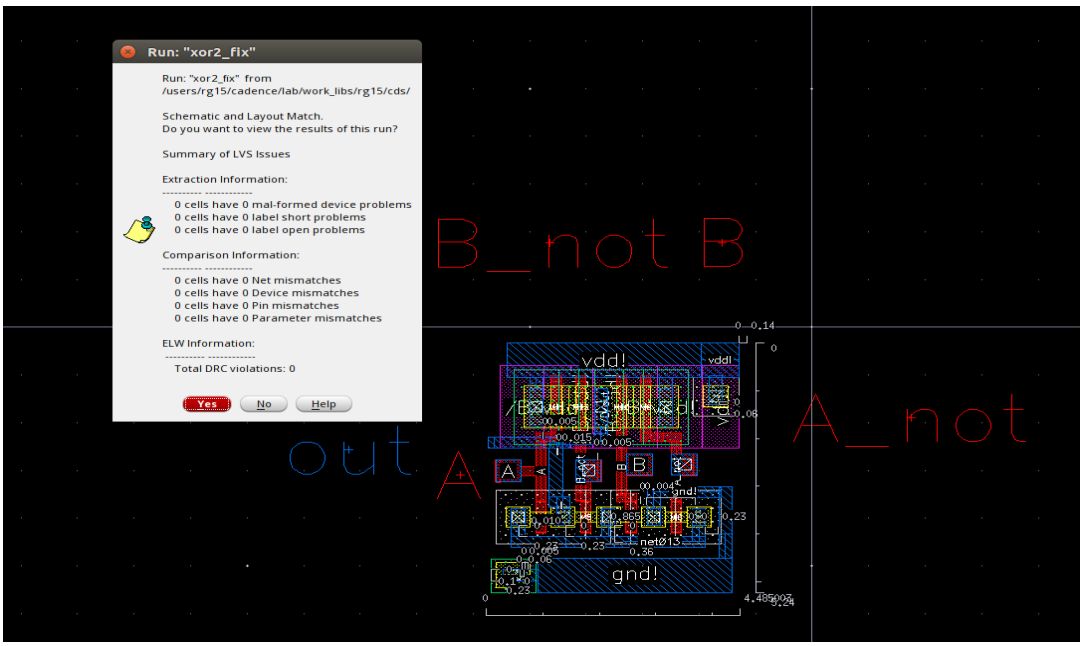
Thus we decrease the total capacitance and the resistance of the circuit.

Also, our implementation using this technique, helped us minimize the length of the poly lines for each gate, were our main goal was to make them straight as possible without bending, in order to decrease capacitance and resistance.

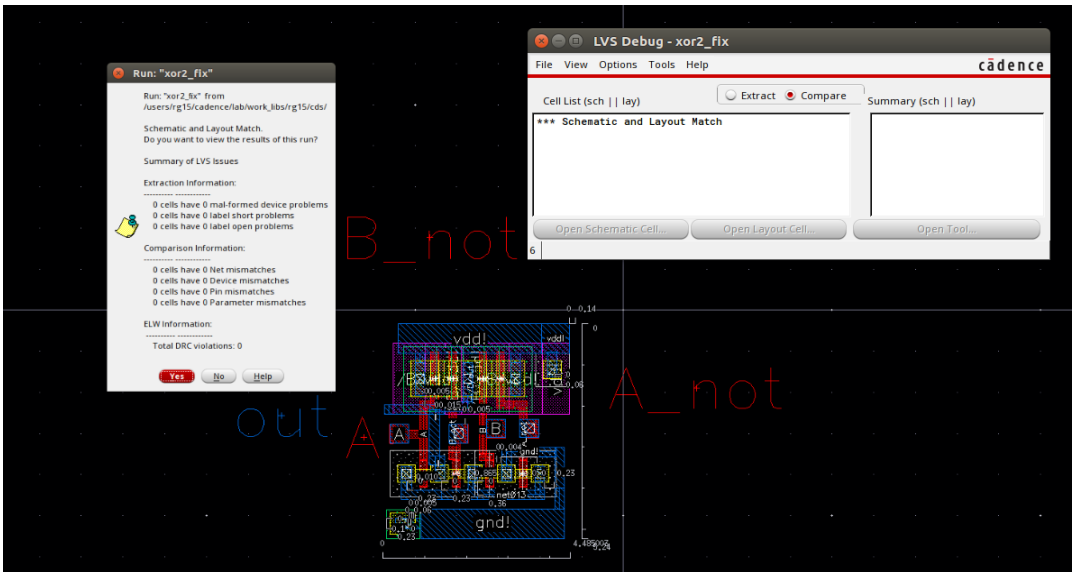
In addition, the diffusion capacitance will decrease as well due to the common connection between the transistors.

26. Print screen of the DRC and LVS reports.

- **DRC:**

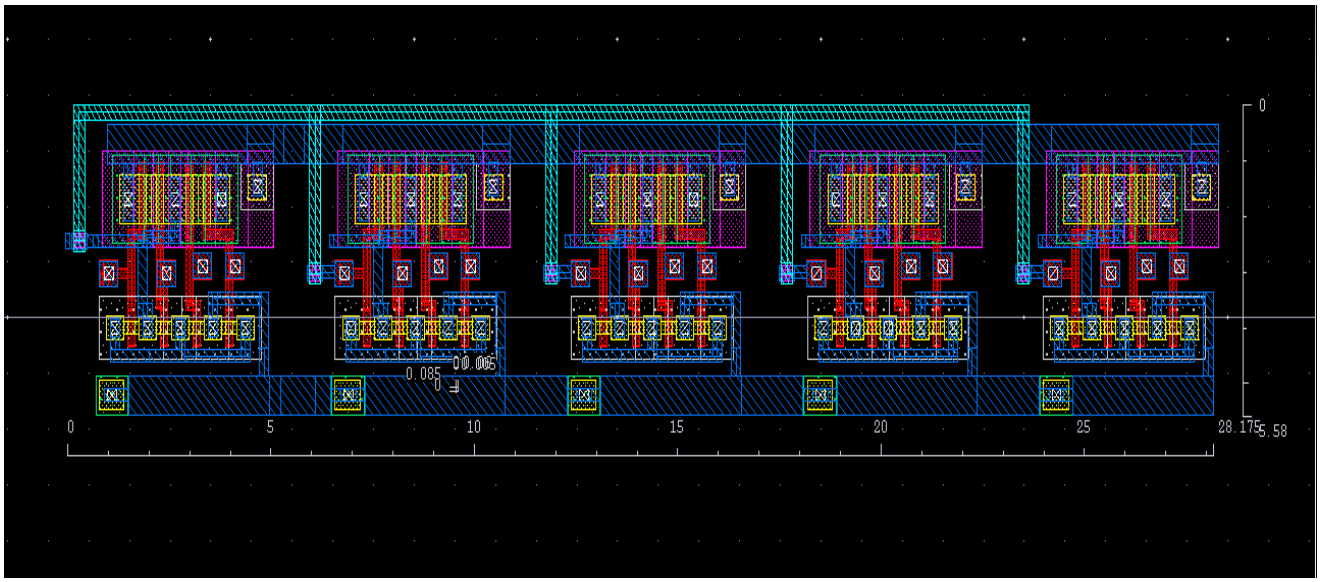


- **LVS:**



5 Hierarchical Design

27. Layout print-screen with a rule on each axis showing the cell's dimensions.

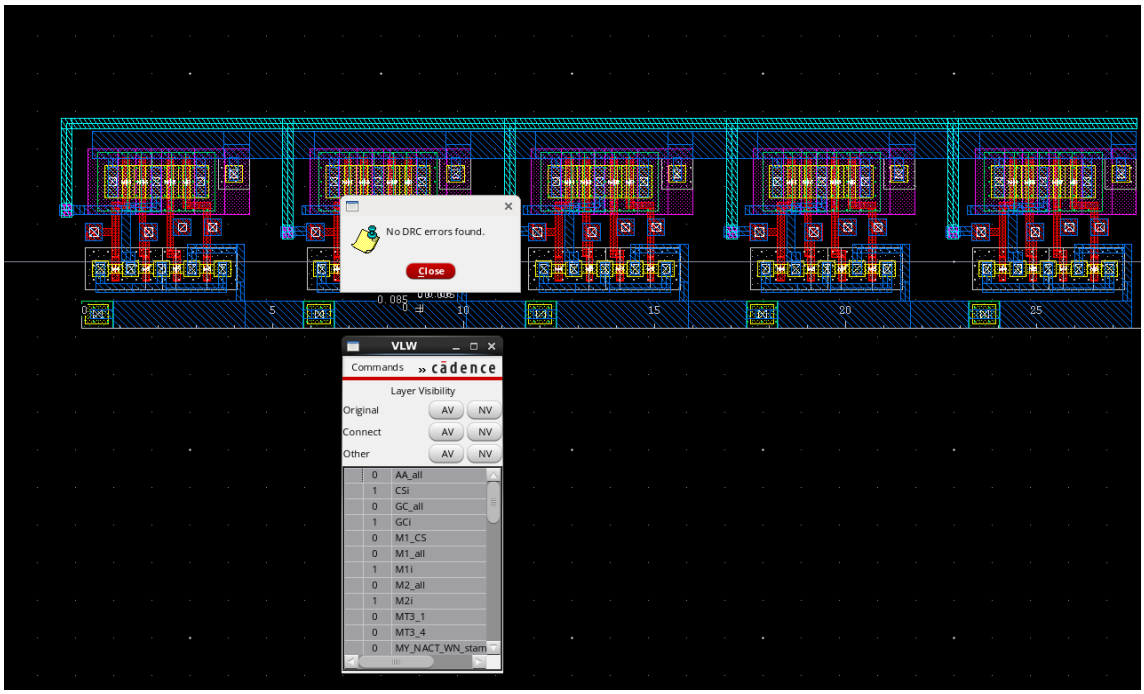


28. What is the total area?

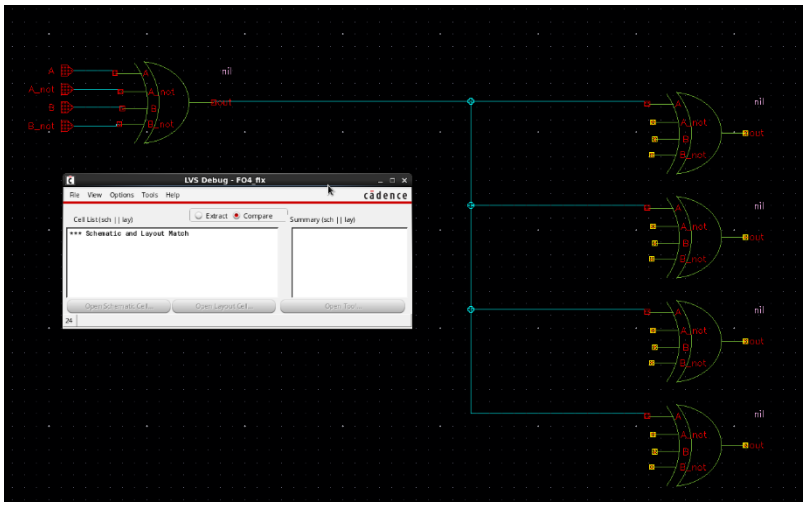
The total area= width*length=157.2165[μm^2]

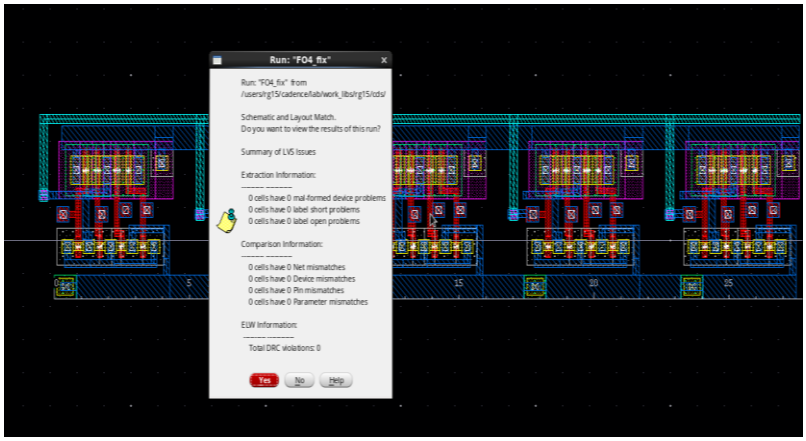
29. Print-screen of the DRC and LVS results.

- DRC:



- LVS:





30. Explain (shortly) how Place & Route influence the chip's performance. In your answer refer to: area, speed and power.

Place & route influence the chip's performance significantly. Placing the transistors far from each other will increase the total area of the chip and that will cause the performances to decrease. That will also require using longer wires which will increase the delay and thus to decrease the speed. And that will cause a higher power consumption.

Have long wires can cause increasing in the delay because $\tau \propto \frac{L^2}{2} rc$, one way to solve that would be to insert buffers in order to cut the wire into smaller pieces and make the signal travel shorter distance from one unit to another. But that on the other hand that will cost us area.

31. Indicate pros and cons of hierarchical design using 'Standard Cells'. Is it the best layout we could do? In your answer refer to: area, speed and power.

Pros: layout using hierarchical design using 'standard cells' is easier and faster.

Cons: This will lead to an excess area and wires that we could have reduced by building the layout from the start without using standard cells. And that excess area and wires will affect the performance of the cell and cause it to be slower and cause a higher power consumption.

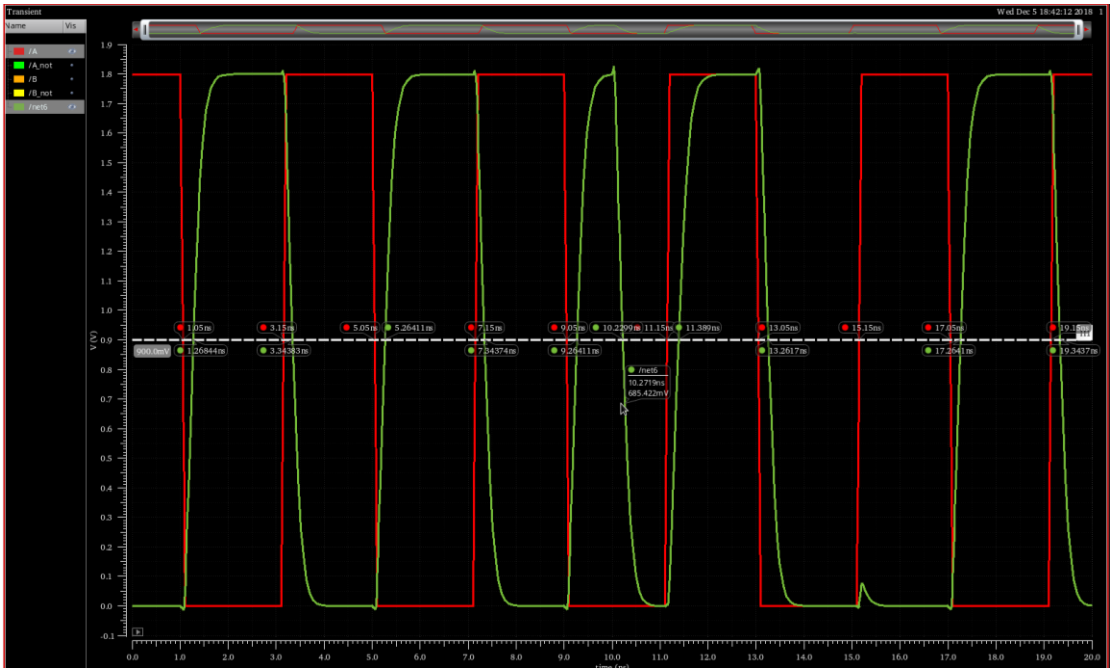
32. Why do we use constant-height cells?

Using constant height cells will cause building the hierarchical design and wiring between the cells to be easier. And that will also help keeping the design rules(DRC).

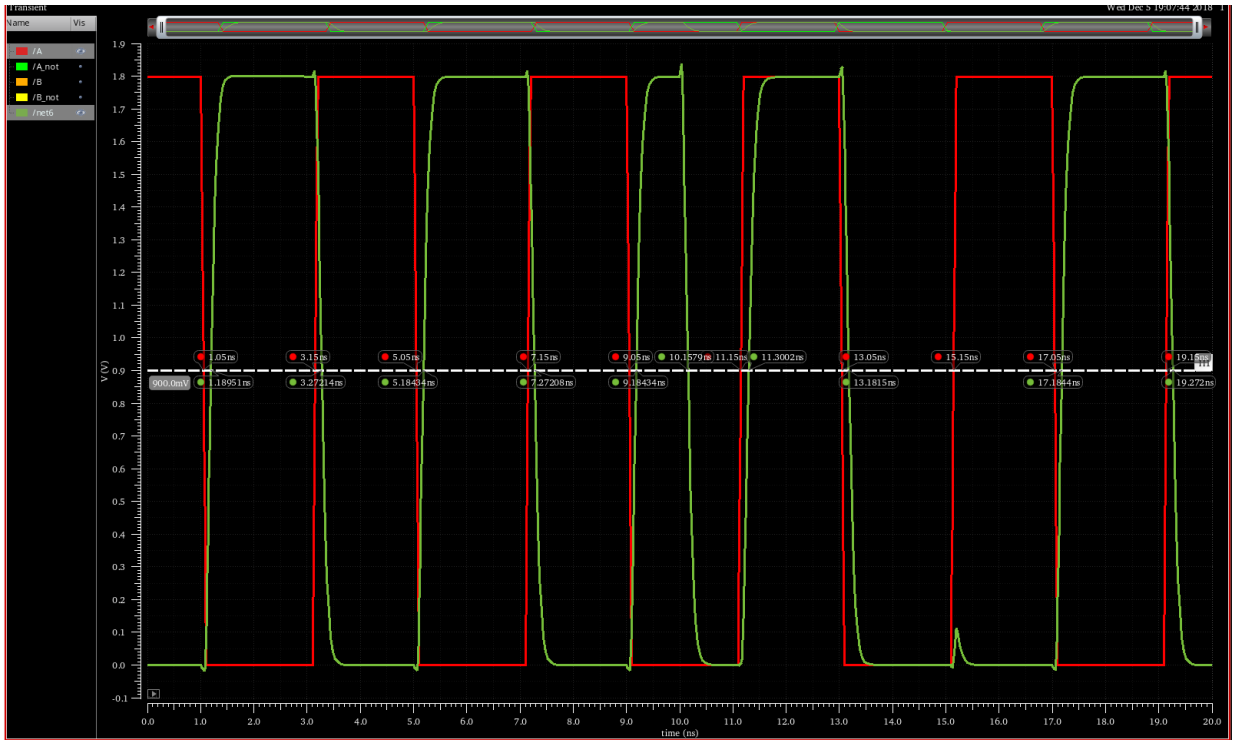
And usually it easier to have fixed height for the cells because if want to connect VDD and GND to the cells they are expected to be at certain position (assuming we're adding the chip to a bigger circuit).

33. Submit the waveforms of the delay simulations with and without the RCX for the fixed FO4 circuit. Include a table with the results.

- **with RCX:**



- without RCX:



	Tpdr	**Tpdf**
Without RCX	134[psec]	122[psec]
With RCX	239[psec]	214.1[psec]

34. What's the increment in the tpdr, tpdf , and tpd considering the parasitics?

The increment considering the parasitics is:

	Tpdr	Tpdf	Tpd
Increment	105[psec]	92.1[psec]	98.55[psec]

35. How could you reduce the parasitic in your layout to reduce the delay?

1. avoiding parallel and overlapping metals.

2. using higher metal than M2.

3. minimizing the total area of Poly (it has high resistivity).

4. minimizing the distance between each XOR2 unit in the hierarchical design so it will take shorter wires to connect between the gates, and between the units themselves.