A CPU with 4+2 means 4 cores and 2 graphic processing units. TGL Power Map --- Please defer to component EDS/datasheet for offical numbers. Non-intel devices are current estimates. Updated: 2020-August Voltage Regulators (VRs) Load Switches (LS) **Load Summary** Max R_{dsON} RAIL NAME SUB-RAIL NAME LOAD NAME V_{OUT} I_{TDC} Enable I_{MAX} I_{MAX} V_{IN} $V_{NOMINAL}$ SVID 65.00 A TGL SKU: UP3-R 4+2 28W VCCIN (IMVP9) VDC SVID 65.00 A CPU PL2/4 Config: Performance Deep Sleep: Deep Sleep Enabled Memory: 32GB DDR4 3200 MT/s VDC VID 27.00 A VCCIN AUX 1 80 V 27 00 A Additional Options: Connected Standby +VCC1P05 OUT FET (internal rail in PCH FIVR) SLP_S3# PCH FIVR 1.050 V 1 050 V 0 30 A 1.20 V 7.90 A 1.20 V Adapter Non-NVDC 0.60 V 0.40 A 0.60 V Charge 1.00 A 2.5V NVDC 1.80 V 1.30 A SLP SUS# 1.80 V 1.300 A V1.8A FLASH 1.80 V N/A Battery V1.8A_EC 1.80 V N/A SLP_S3# V1.8A 1.80 V N/A *CCG recommends NVDC charger and 2SxP battery for better VR ▶ ¥ V1.8S_PLATFORM SLP_S0# && SLP_S3# V1.8A **→** V1.8S_SSD 1.80 V N/A performance, however traditional 3SxP battery and non-NVDC V1.8S_SDCARD 1.80 V N/A charger may implemented in some designs 1.80 V 0.000 A V1.8Dx_WIFI 1.80 V N/A 1.80 V N/A SoC Power Levels VCC_V1P05EXT_1P05 28 64 <----Hover over PL connecting to GND is allowed, but not recommended due to extra leakage value for a definiion PL3: 66 VCC_VNNEXT_1P05 121 V3.3_DSW VDC 3.30 V 0.20 A VCCDSW 3P3 3.30 V N/A 0.202 A VCCPRIM 3P3 3.30 V V3.3A_EC 3.30 V N/A V3.3 DSW SLP S3# V3.35 3.30 V N/A Note: Use of a GPIO+BIOS control is also allowed: consult PDG. ► V3.3Dx_PLATFORM SLP_S0# && SLP_S3# V3.3_DSW V3.3Dx SSD 3.30 V N/A V3.3Dx_EDP 3.30 V N/A **Engerized States** V3.3Dx_DPWP 3.30 V N/A On in SO, SOix /3.3Dx_TOUCHSCREEN 3.30 V N/A On in S0 - S3 V3.3Dx_CAMERA 3.30 V N/A On in S0 - S5 V3.3Dx SDCARD 3.30 V N/A On in SO - DS4/DS5 N/A 3.30 V 3.30 V N/A V3.3S AUDIO V3.3_DSW GPIO AUDIO V3.3S AUDIO 3.30 V N/A V3.3S SENSORS 3.30 V N/A 5.00 V 2.00 A SLP SUS# VDC 5.00 V N/A → V5S_PLATFORM VSA VSS ALIDIO N/A 5 00 V N/A 2.000 A V5Dx_HDMIWP 5.00 V V5Dx USBWP 5.00 V **VDCDx_EDP** VDC VDCDx EDP VDC N/A