SPI FLASH

SPI_CLK & SPI_MOSI matched to within 500 mil
SPI_CLK & SPI_CS[0,1] matched to within 500 mil

+5VA, +5V_LDO, R290 NOP 0R, R291 0R, +5V_SPI_SW, +3V3DSW, +3V3A
R292 100K, C535 100nF, R293 100K
U29 Bus switch, 3384 (VCC, OE1, OE2, GND)
to MCP: SPI_MOSI, SPI_MISO, SPI_CS0, SPI_CLK
to ATP: SPI_ATP_CLK, SPI_ATP_CS0, SPI_ATP_SO, SPI_ATP_SI
OE Vin(IH) = 2 V
OE Vin(LOW) = 0.8 V
Q33 NDS335N,3A, R301 100k, R302 10k
SPI_ATP_CNTR_PQ, SPI_ATP_CNTR_P, SPI_ATP_CTRL#

WSON6x8-8
U30 (DI, DO, CS#, SCK, WP#, HOLD#, VCC, GND, EPAD)
C536 1uF
R294 SPI_SI_FL_R 33R SPI_SI_FL
R297 SPI_SO_FL_R 33R SPI_SO_FL
R298 SPI_CLK_FL_R 33R SPI_CLK_FL
SPI_CS0_FL
R295 100K, R296 100K
R299 SPI_WP 33R SPI_IO2
R300 SPI_HOLD 33R SPI_IO3
SPI_FLASH 256Mbit, WSON6x8-8

Supervisor
SPI_ATP_CNTR_PQ
SPI_ATP_CNTR_PQ: High if SPI_SV2FL# or SPI_SV2PCH# is low (in order to disconnect flash from PCH)
R303 10k
C537 100nF
U31 Bus switch, 3384 (VCC, OE1, OE2, GND)
SPI_SV_CLK, SPI_SV_CS0, SPI_SV_SO, SPI_SV_SI
SPI_CLK_FL_R, SPI_CS0_FL, SPI_SO_FL_R, SPI_SI_FL_R
SPI FLASH
SPI_MOSI, SPI_MISO, SPI_CS0, SPI_CLK
PCH
R304 10k, R305 10k
SPI_SV2FL#, SPI_SV2PCH#

SPI TPM Header

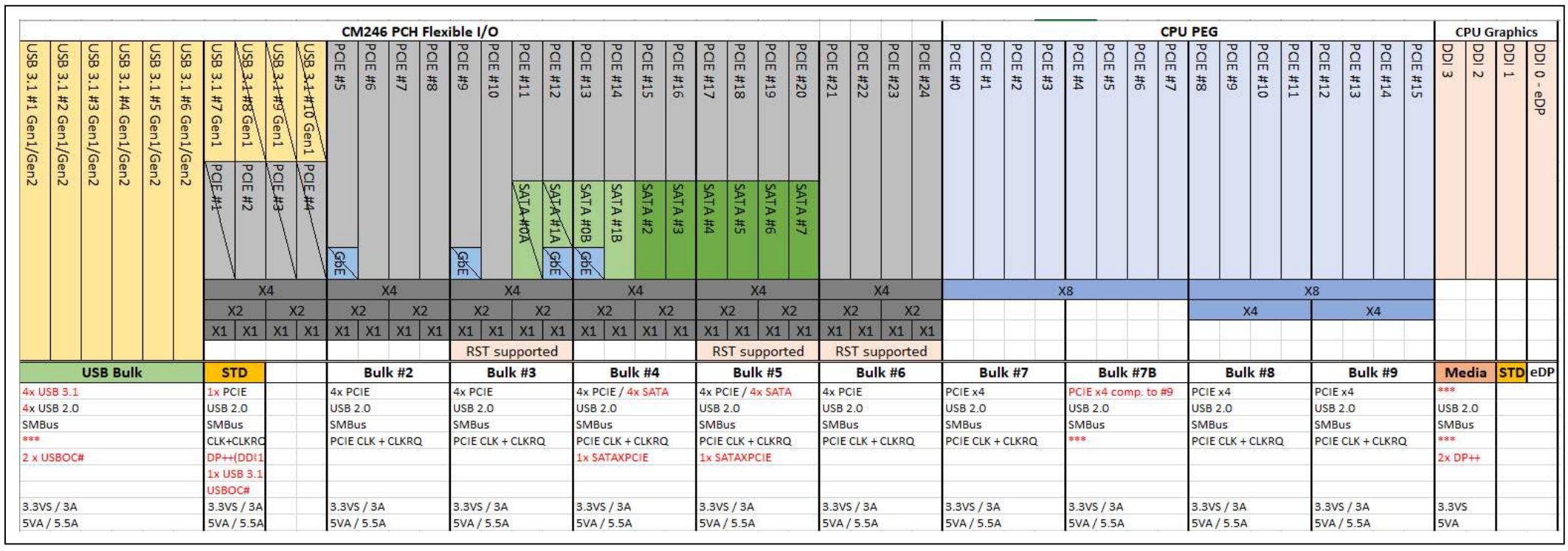
J12 5x2, 50mil, SMT, bot. entry
Short SPI stubs
SPI_SI_FL_R 33R R309 SPI_SI_TPM
SPI_SO_FL_R 33R R310 SPI_SO_TPM
33R R311 SPI_CS2_TPM
SPI_CLK_FL_R 33R R312 SPI_CLK_TPM
SPI_CS2, TPM_PIRQ#, TPM_GPIO
PLTRST# R313 0R PLTRST#_TPM
R306 10k, R307 10k, R308 100k, R314 10k NOP
C538 1uF, C539 100nF NOP

U54A
BE36 GPP_A11/PME#/SD_VDD2_PWR_EN#
R15 RSVD2, R13 RSVD1
AL37 VSS, AN35 PCH_TP_AN35, TP25
RSVD Strap (int. PU) AU41
SPI_MOSI BA45 SPI0_MOSI
SPI_MISO AY47 SPI0_MISO
SPI_CS0 AW47 SPI0_CS0#
SPI_CLK AW48 SPI0_CLK
SPI_CS1 SPI0_CS1#
SPI_IO2, SPI_IO3, SPI_CS2
SPI0_IO[2,3] - RSVD Strap (PU) AY48
BA46 SPI0_IO3, AT40 SPI0_CS2#
BE19 GPP_D1/SPI1_CLK/SBK1_BK1
BF19 GPP_D0/SPI1_CS#/SBK0_BK0
BF18 GPP_D3/SPI1_MOSI/SBK3_BK3
BE18 GPP_D2/SPI1_MISO/SBK2_BK2
BC17 GPP_D22/SPI1_IO3
BD17 GPP_D21/SPI1_IO2
GPP_B13/PLTRST# AV29
GPP_K16/GSXCLK Y47, GPP_K12/GSXDOUT Y46, GPP_K13/GSXSLOAD Y48, GPP_K14/GSXDIN W46, GPP_K15/GSXRESET# AA45
GPP_E3/CPU_GP0 AL47, GPP_E7/CPU_GP1 AM45, GPP_B3/CPU_GP2 BF32, GPP_B4/CPU_GP3 BC33
GPP_H18/SML4ALERT# AE44, GPP_H17/SML4DATA AJ46, GPP_H16/SML4CLK AE43, GPP_H15/SML3ALERT# AC47, GPP_H14/SML3DATA AD48, GPP_H13/SML3CLK AF47, GPP_H12/SML2ALERT# AB47, GPP_H11/SML2DATA AD47, GPP_H10/SML2CLK AE48, INTRUDER# BB44
GPP_H12: eSPI sharing Strap (int. PD)
CNP_H_IP_CFL 1 OF 13

For MB: PLTRST#
For ribbons: PLTRST#_BUF
PLTRST# Q
Q31 Dual N,0.5A,20V
C661 NOP 100nF
R238 10K, R239 2.21K
+3V3A, R497 100K, PCH_PU_H15
INTRUDER#

SBC-CLH

1.3



BL1

BIOS
LICENSE
AMI

BIOS LICENSE AMI

ZZ1

P/N = 188Z10030

PARSER_VERSION_1.0

PCB1

PCB, SBC-CLH, Rev 1.3

Title	01-Index	
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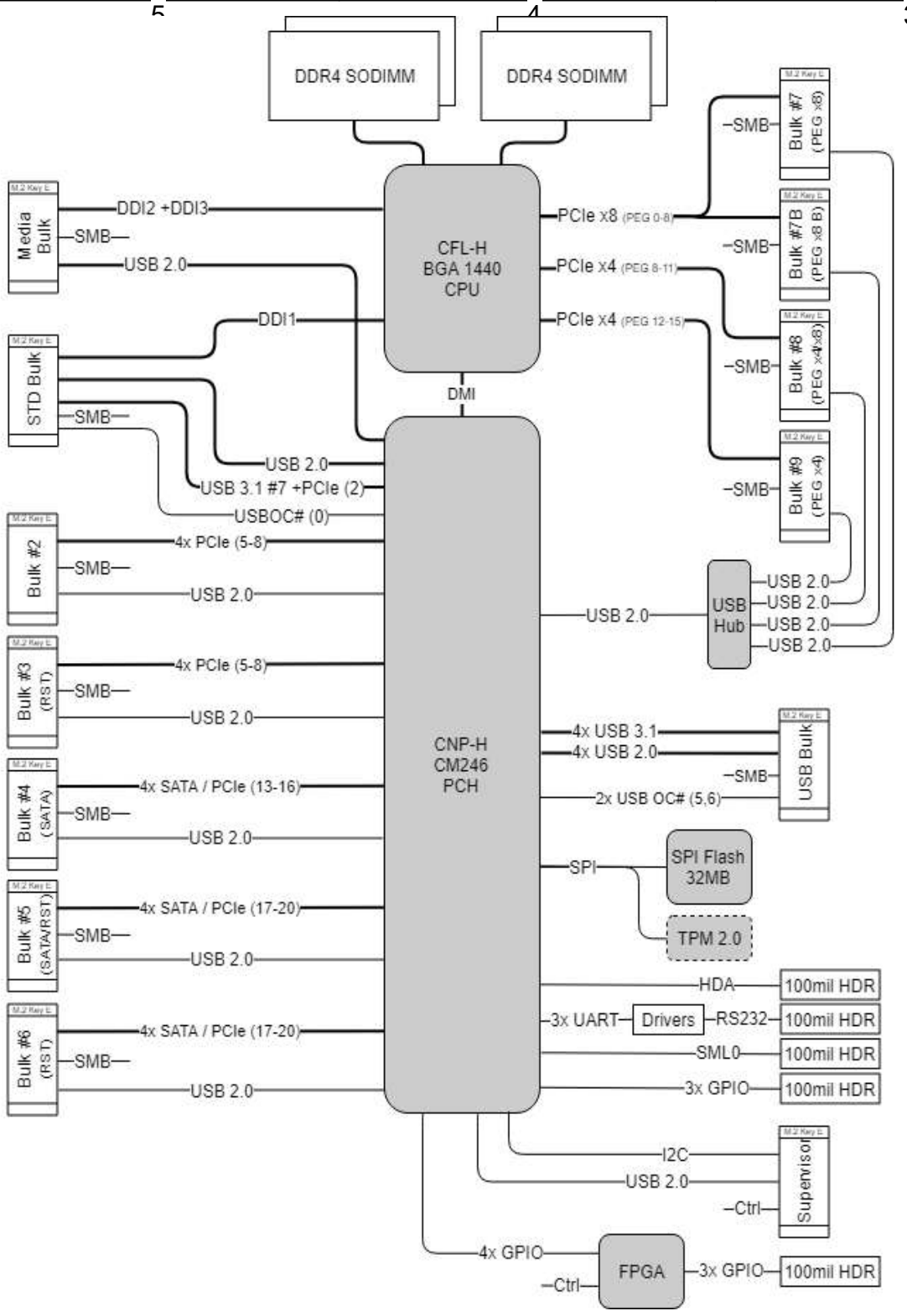

Title	02-Block Diagram	
Size A4	Document Number SBC-CLH	Rev 1.3
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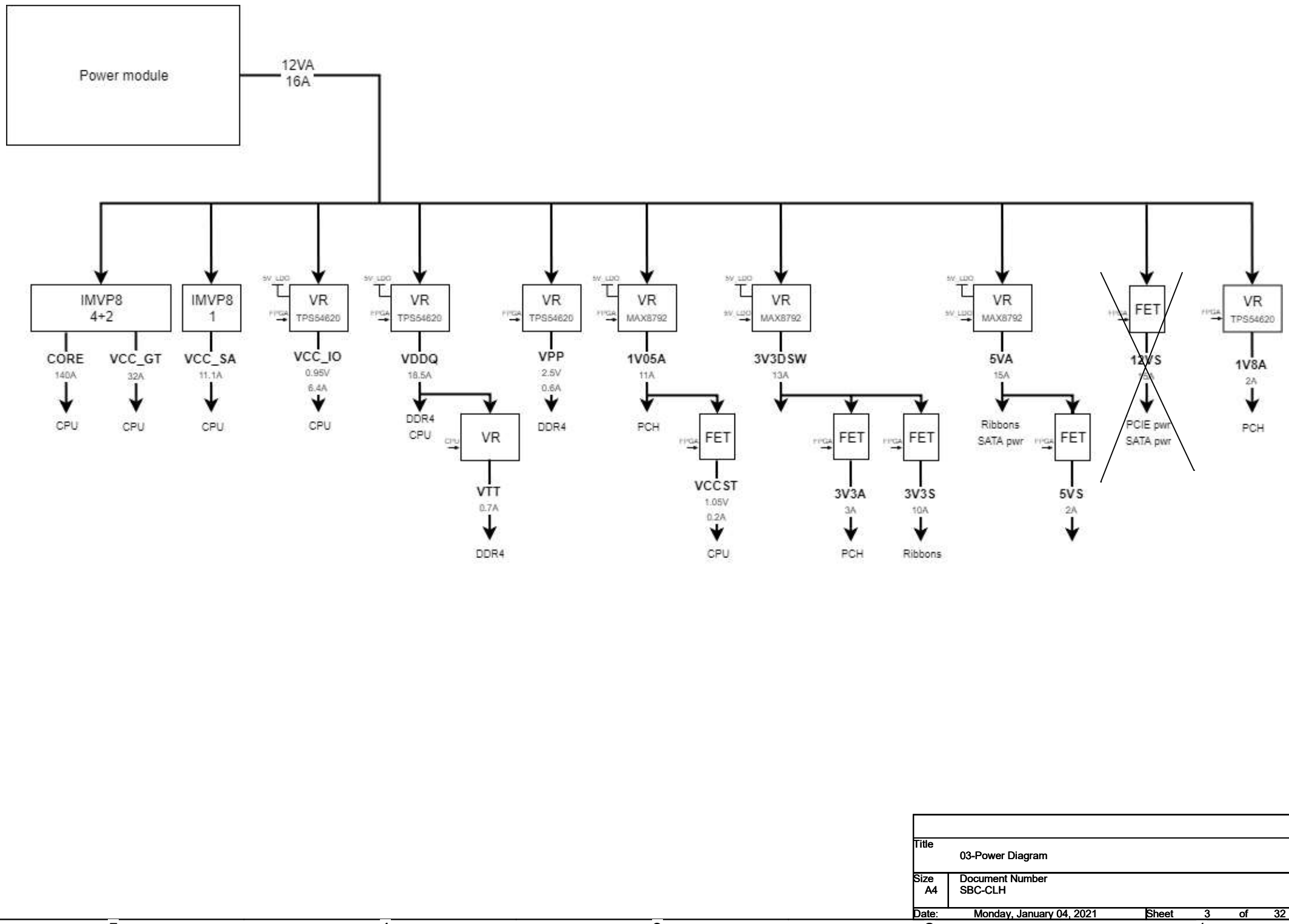

Title	03-Power Diagram	
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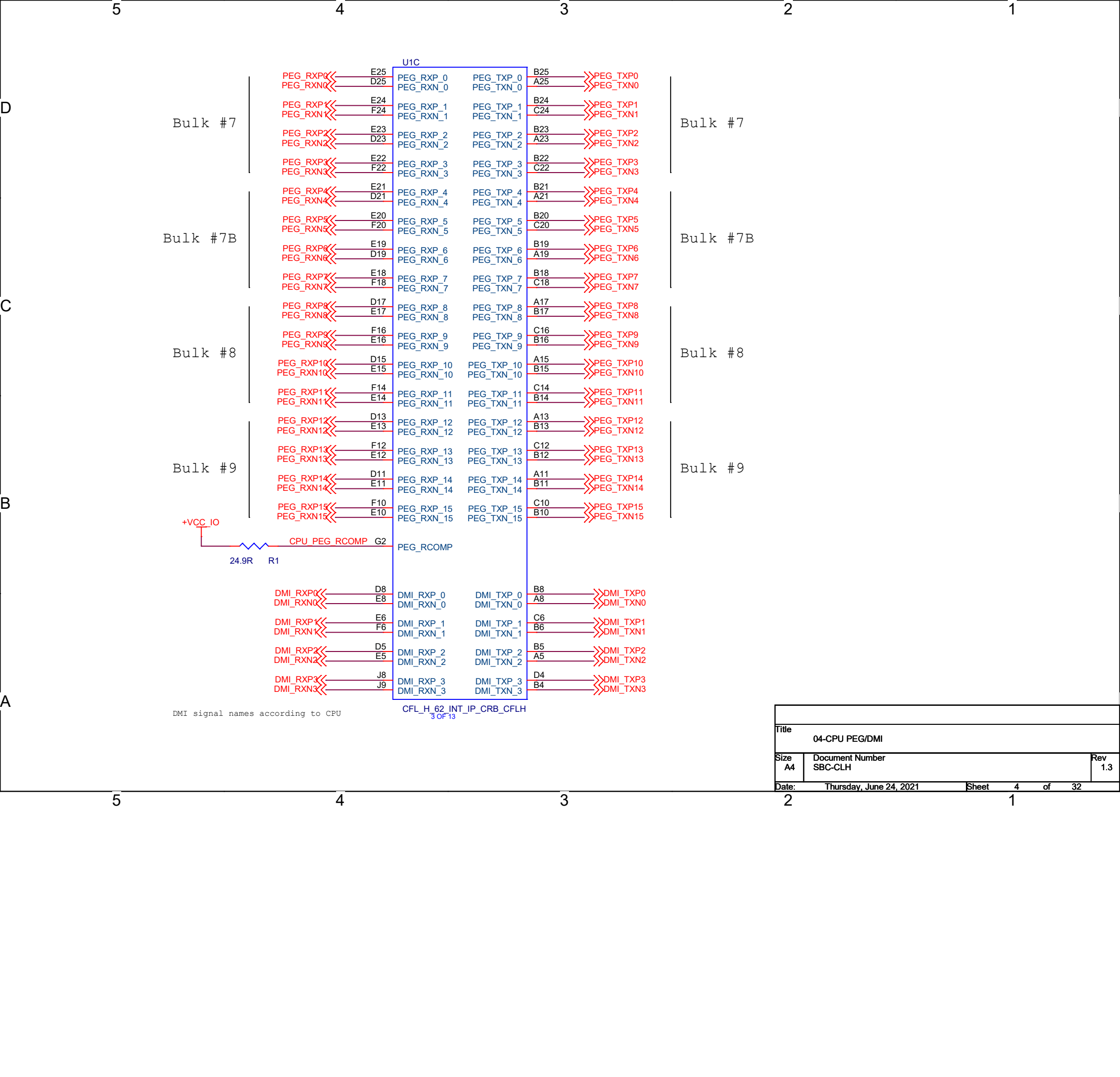

Title	04-CPU PEG/DMI	
Size: A4	Document Number: SBC-CLH	Rev: 1.3
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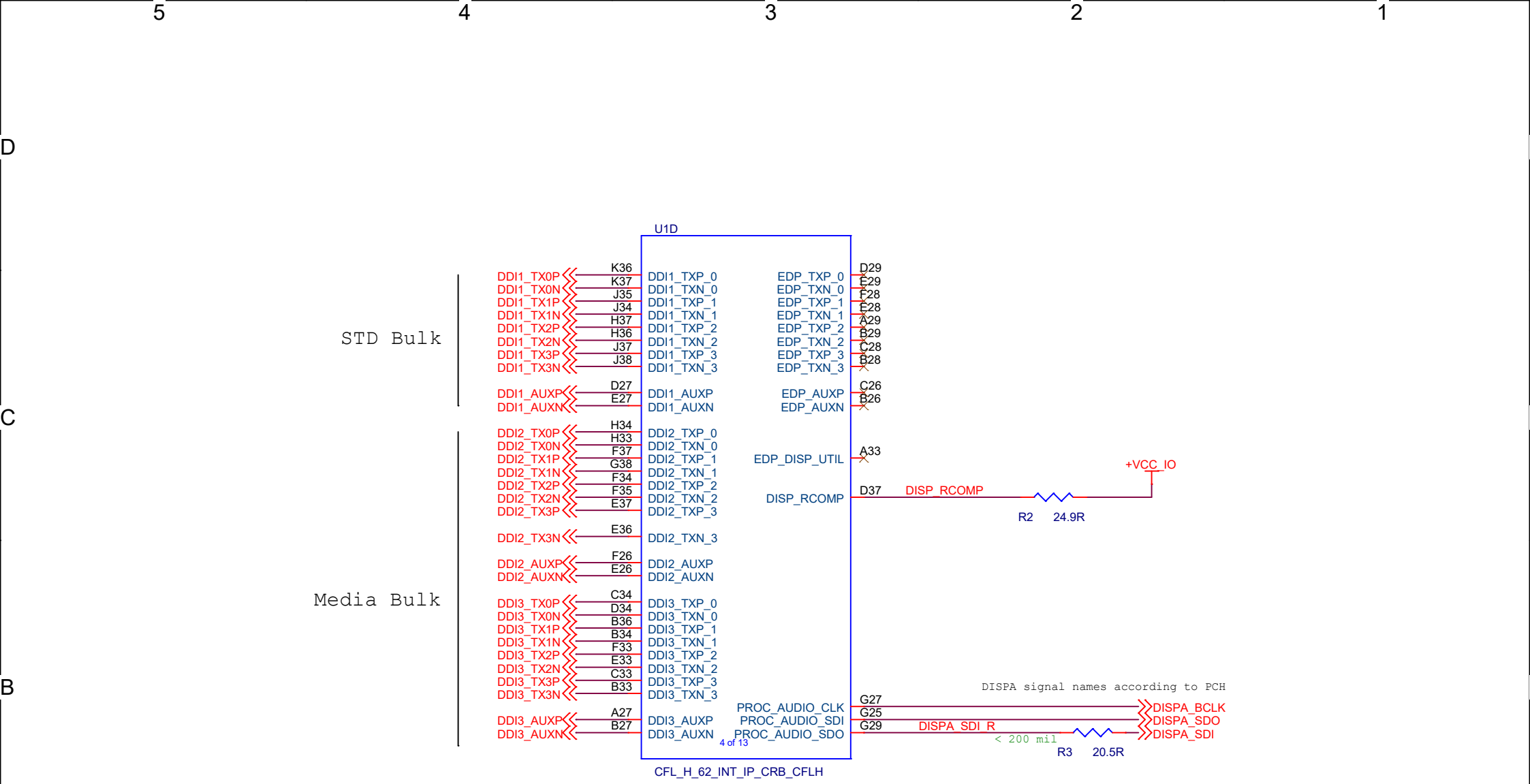

Title	05-CPU DDI	
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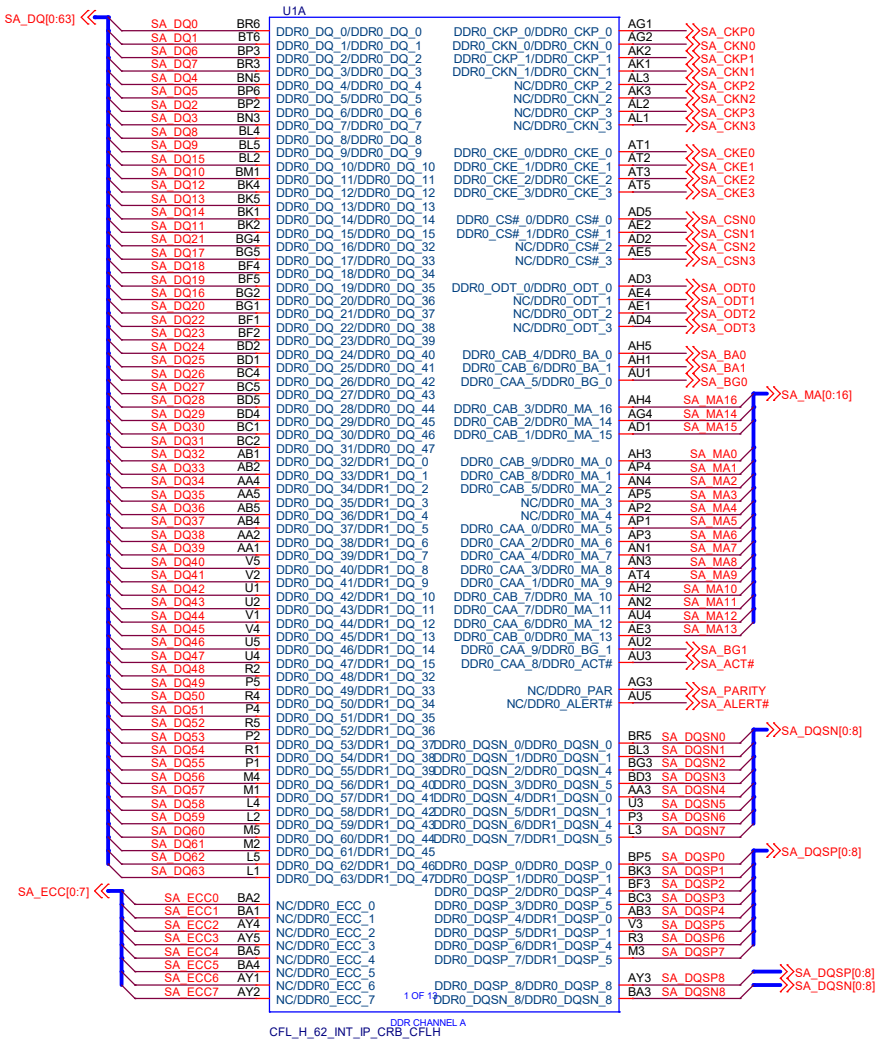
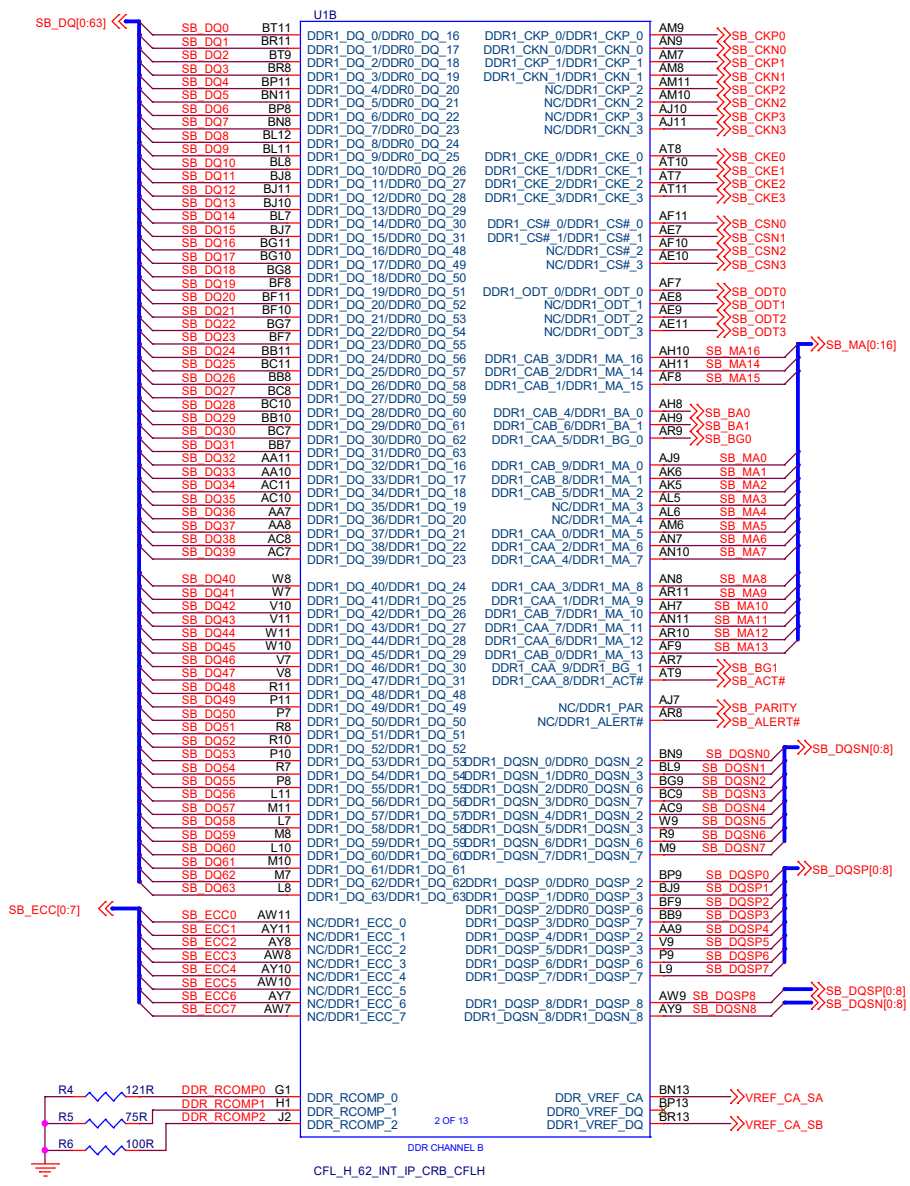
Data bits can be swapped within a byte

Interleaved mapping



Data bits can be swapped within a byte

Interleaved mapping



Title	06-CPU DDR4	
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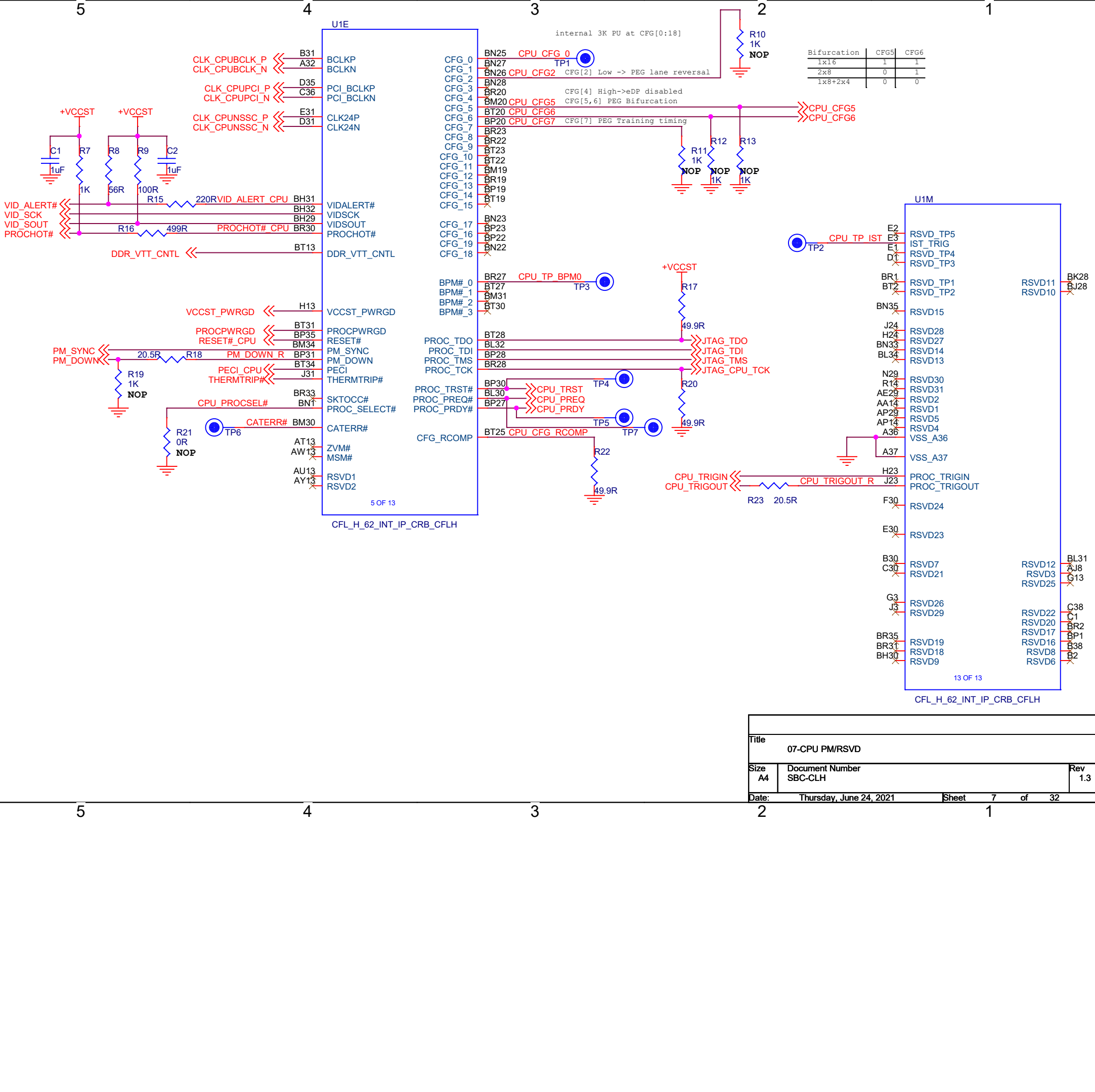

Title	07-CPU PM/RSVD
Size	A4
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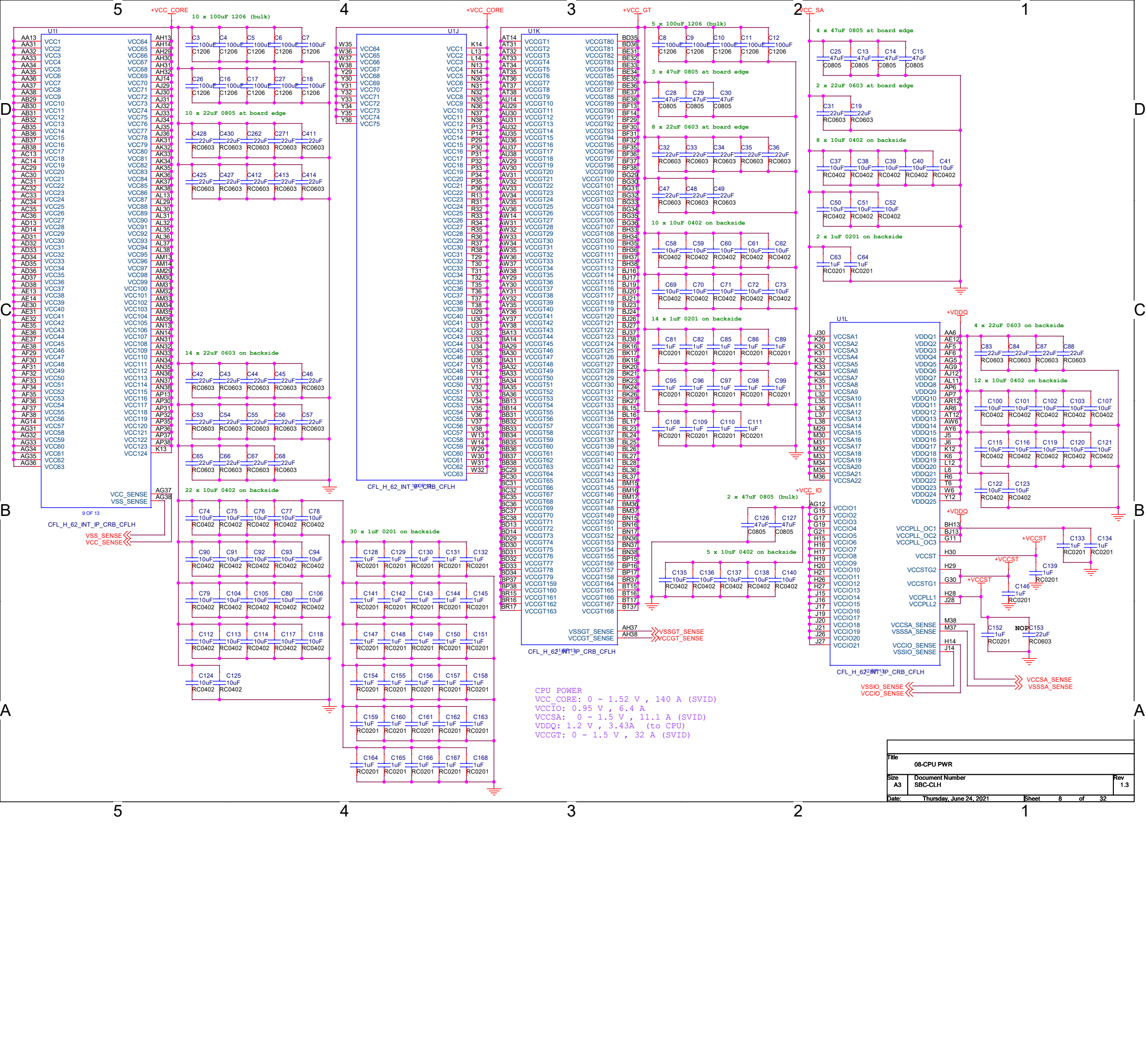
+VCC_CORE
10 x 100uF 1206 (bulk)
10 x 22uF 0805 at board edge
14 x 22uF 0603 on backside
22 x 10uF 0402 on backside
30 x 1uF 0201 on backside
+VCC_GT
5 x 100uF 1206 (bulk)
3 x 47uF 0805 at board edge
8 x 22uF 0603 at board edge
10 x 10uF 0402 on backside
14 x 1uF 0201 on backside
2 x 47uF 0805 (bulk)
5 x 10uF 0402 on backside
+VCC_SA
4 x 47uF 0805 at board edge
2 x 22uF 0603 at board edge
8 x 10uF 0402 on backside
2 x 1uF 0201 on backside
+VDDQ
4 x 22uF 0603 on backside
12 x 10uF 0402 on backside
+VCC_IO
U1I
U1J
U1K
U1L
CFL_H_62_INT_IP_CRB_CFLH
VCC_SENSE
VSS_SENSE
VSSGT_SENSE
VCCGT_SENSE
VCCSA_SENSE
VSSSA_SENSE
VSSIO_SENSE
VCCIO_SENSE
+VCCST
CPU POWER
VCC_CORE: 0 - 1.52 V , 140 A (SVID)
VCCIO: 0.95 V , 6.4 A
VCCSA: 0 - 1.5 V , 11.1 A (SVID)
VDDQ: 1.2 V , 3.43A (to CPU)
VCCGT: 0 - 1.5 V , 32 A (SVID)
Title
08-CPU PWR
Size
A3
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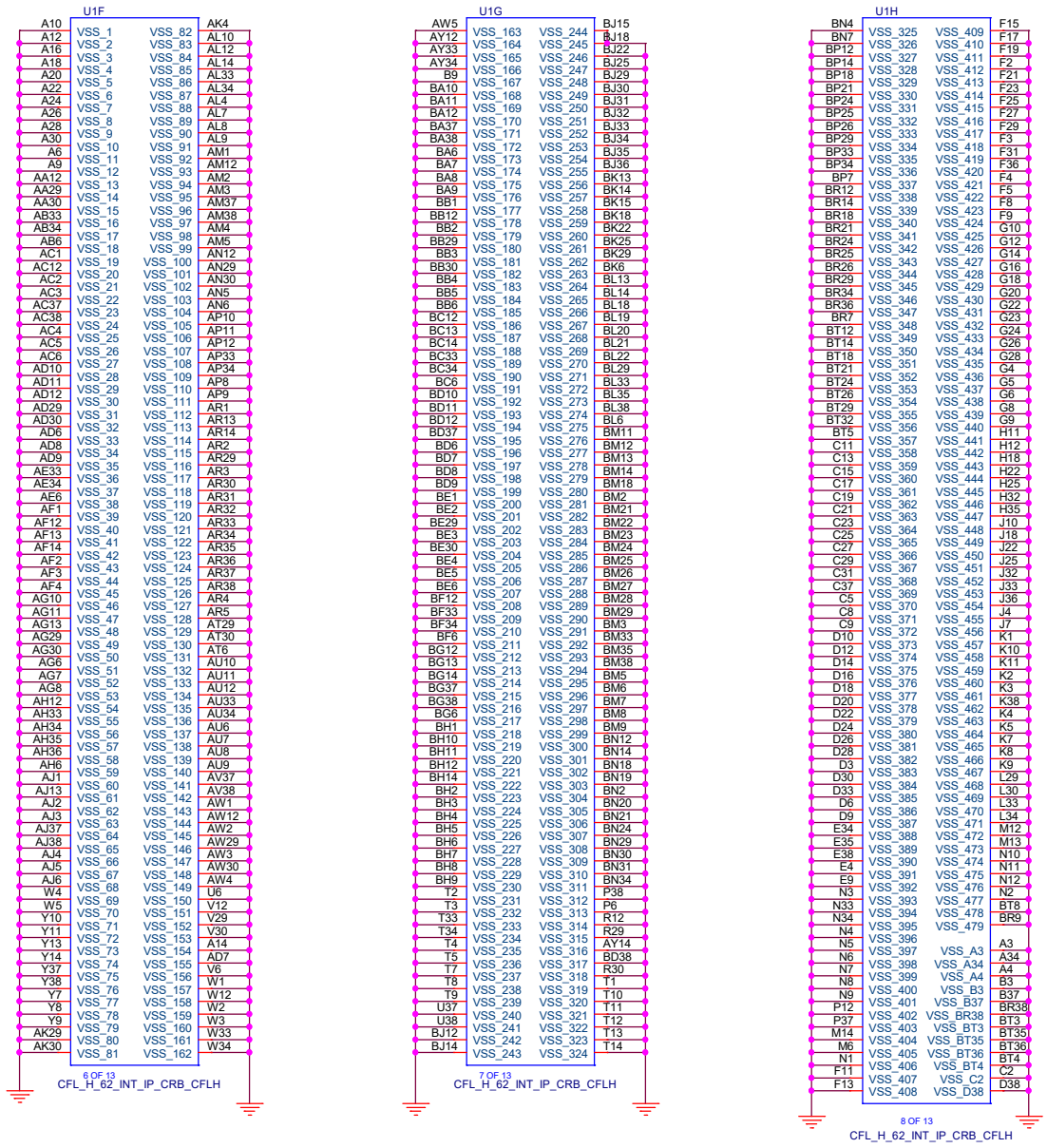

Title	09-CPU GND	
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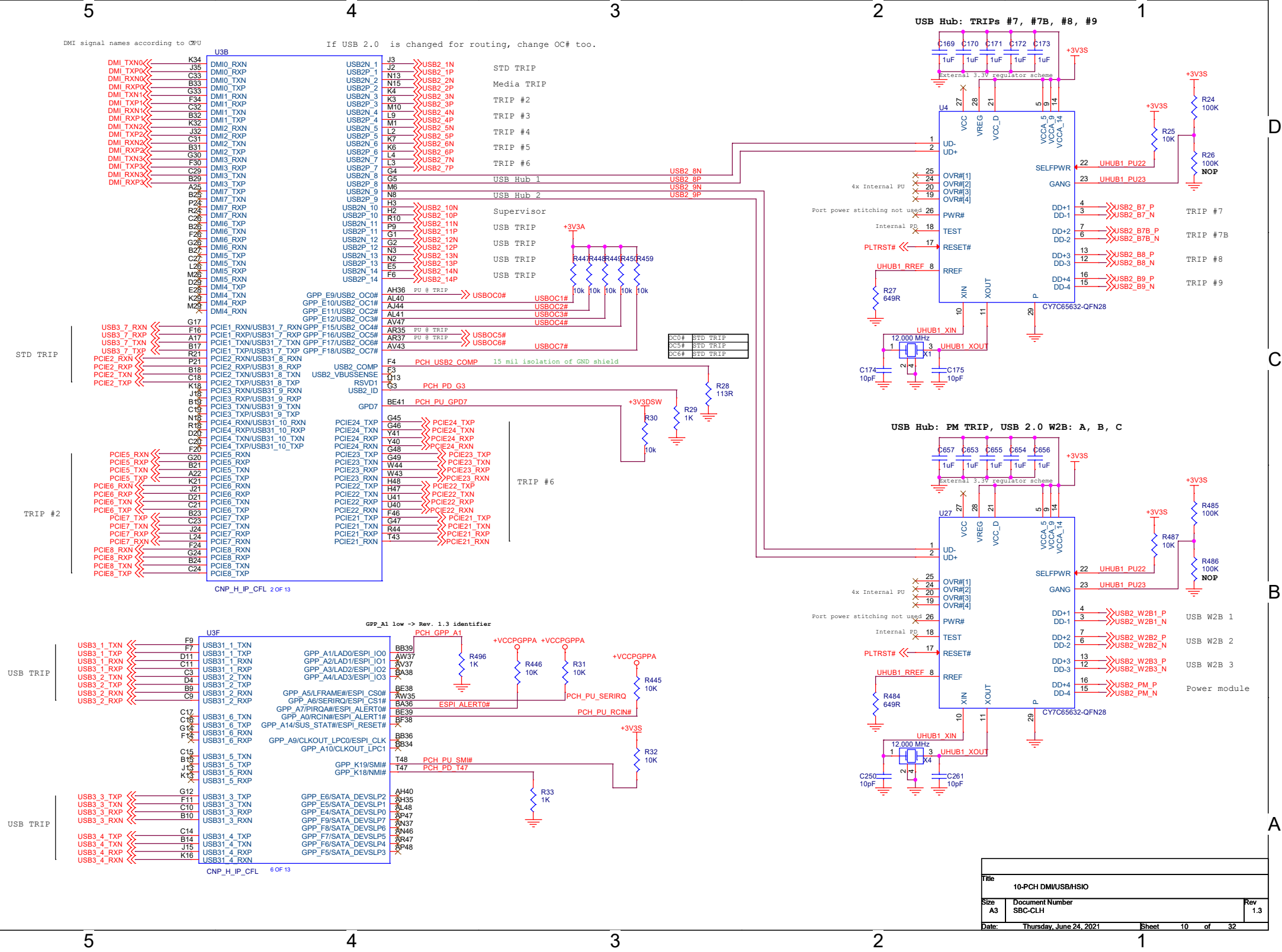

Title	10-PCH DMI/USB/HSIO		
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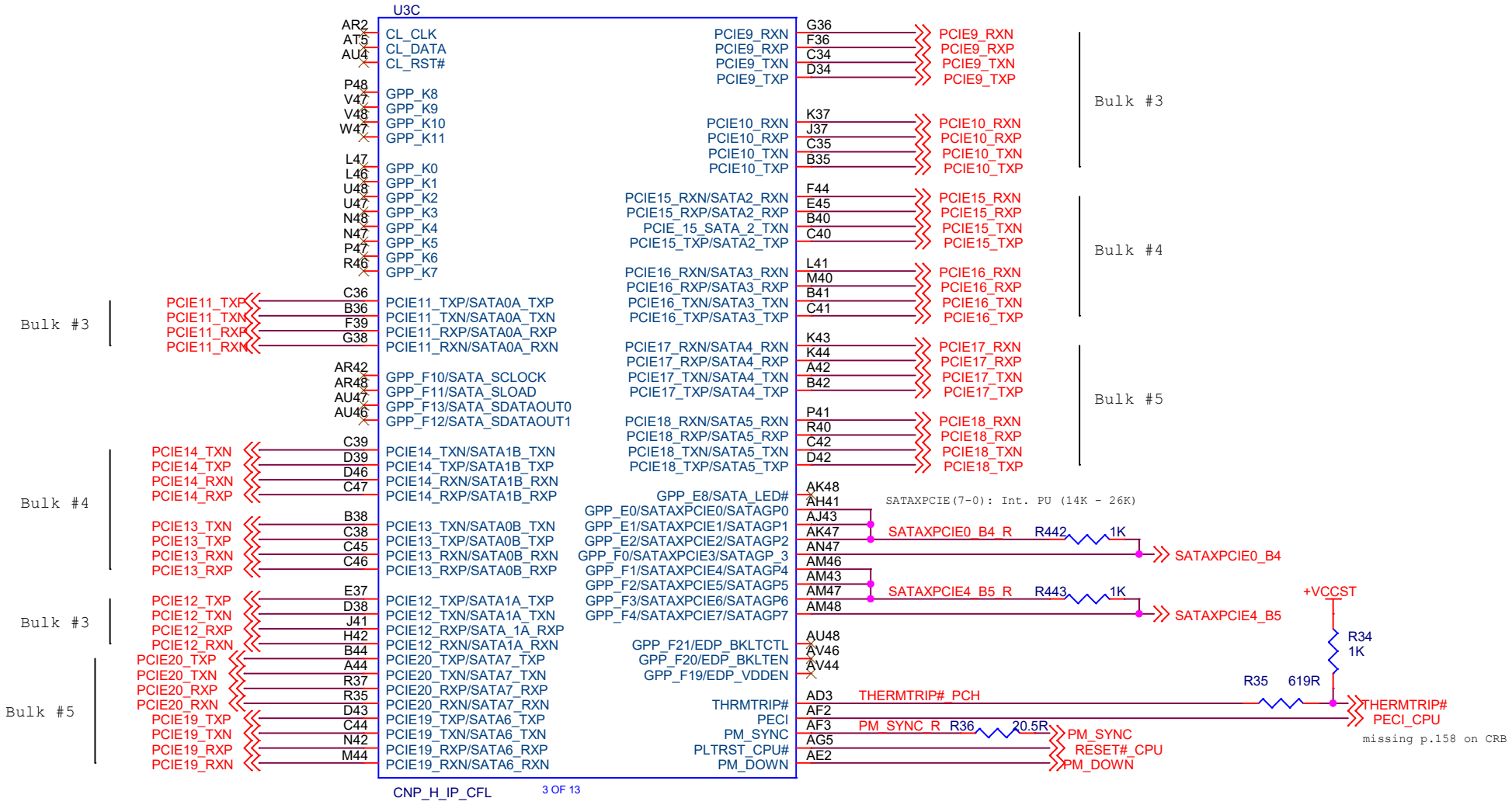

Title	11-PCH SATA/HSIO	
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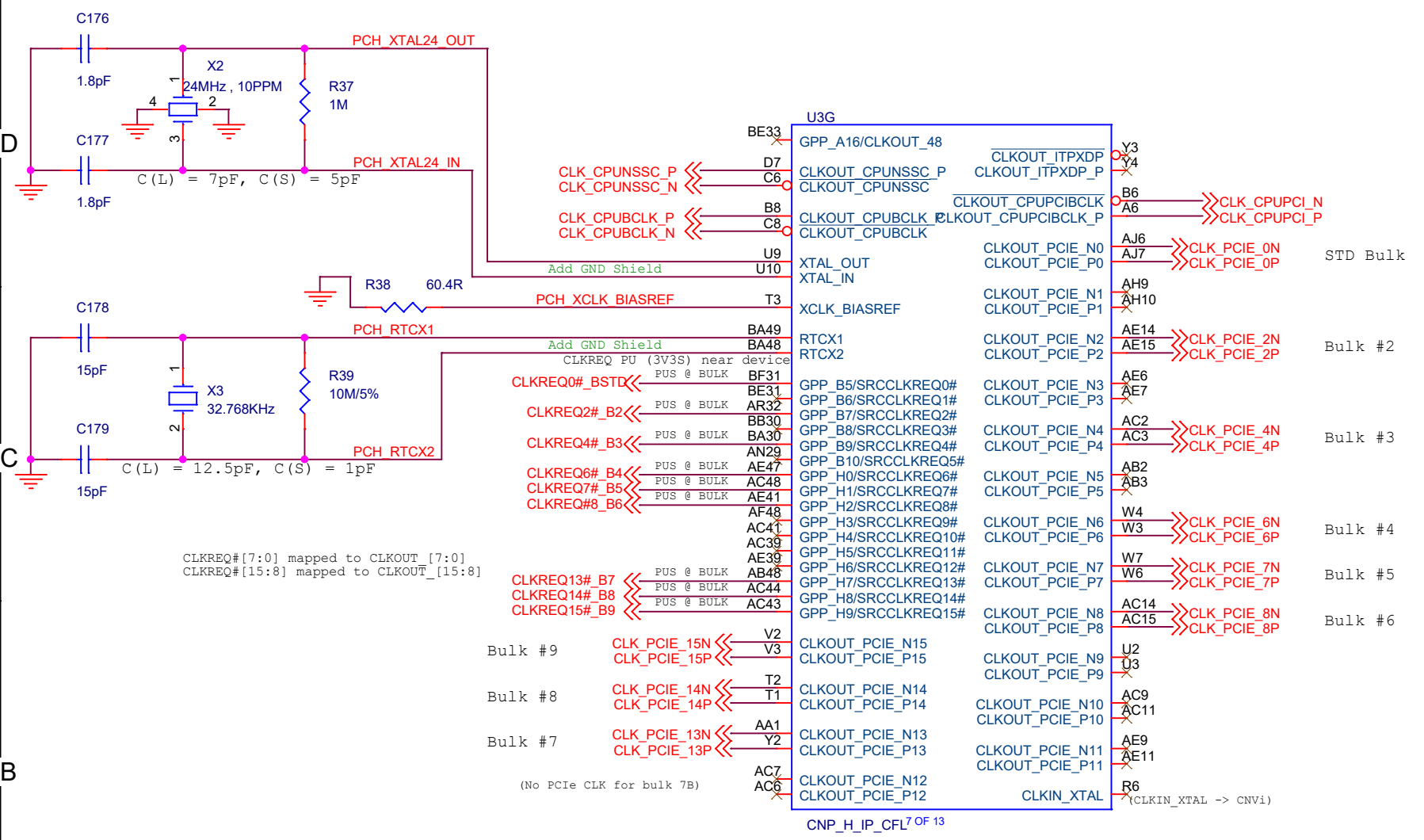

Title	12-PCH CLK
Size	A4
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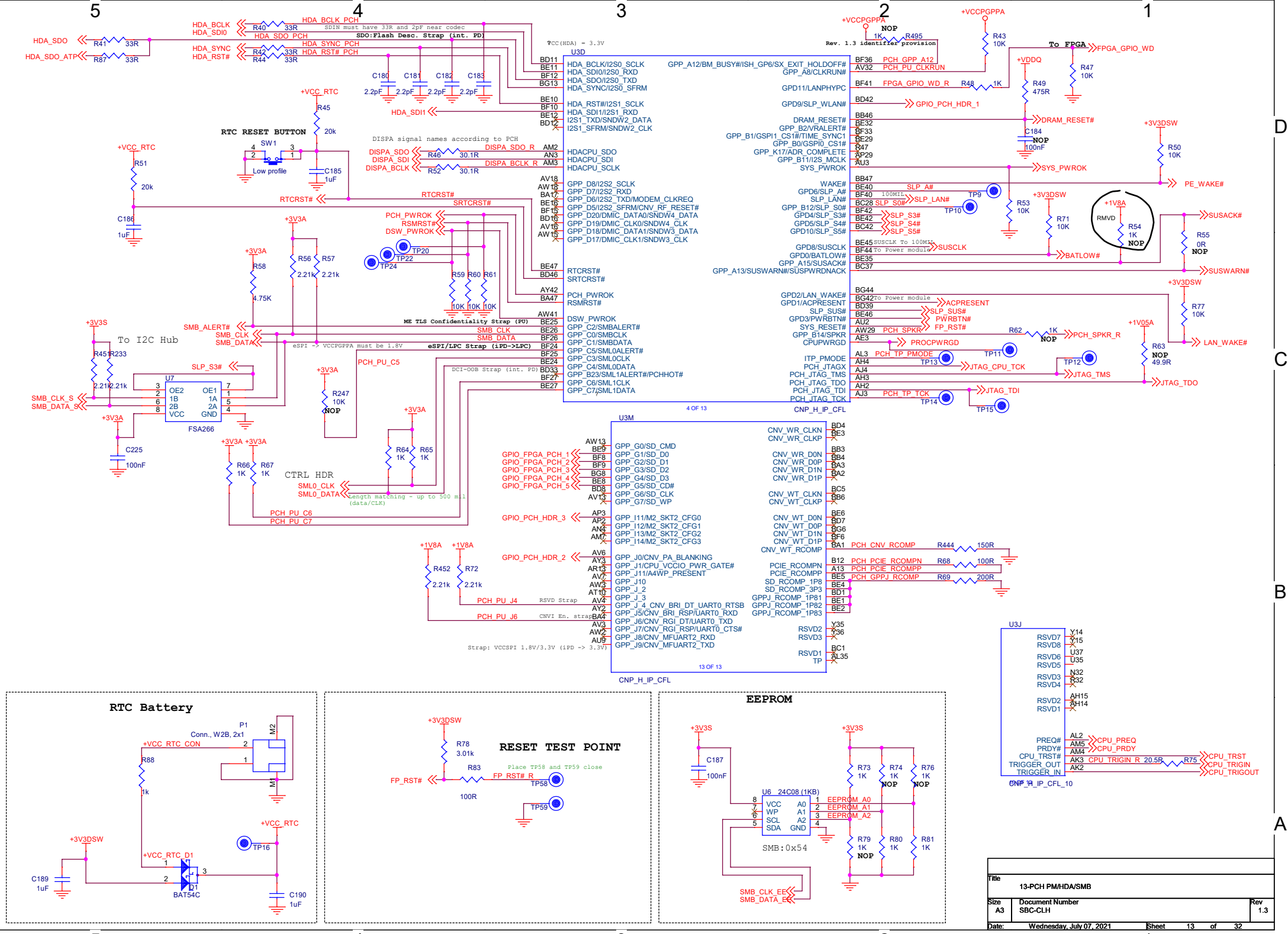

Title	13-PCH PM/HDA/SMB
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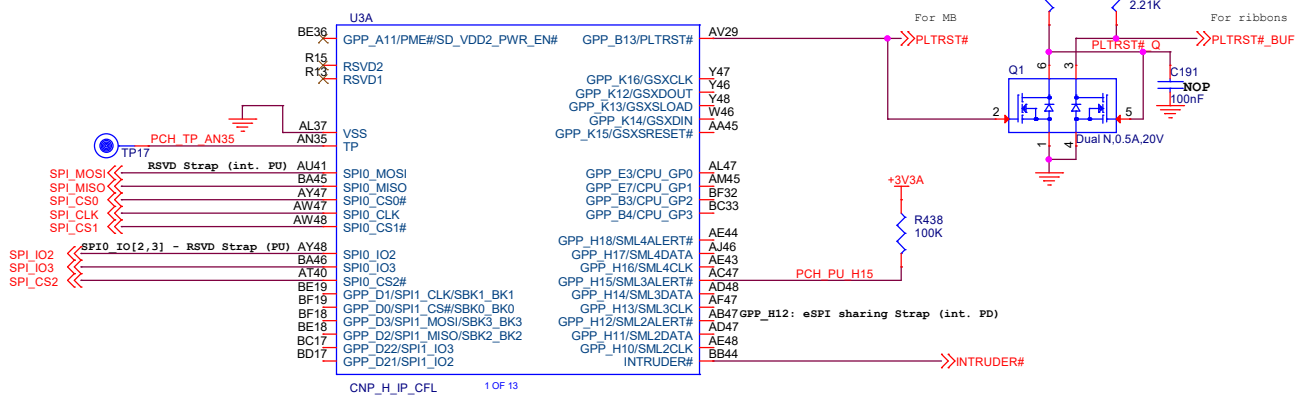

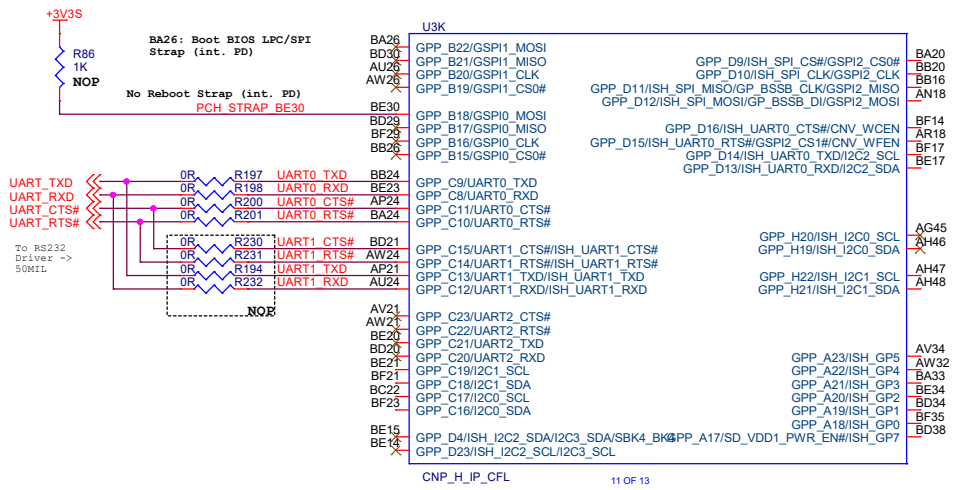

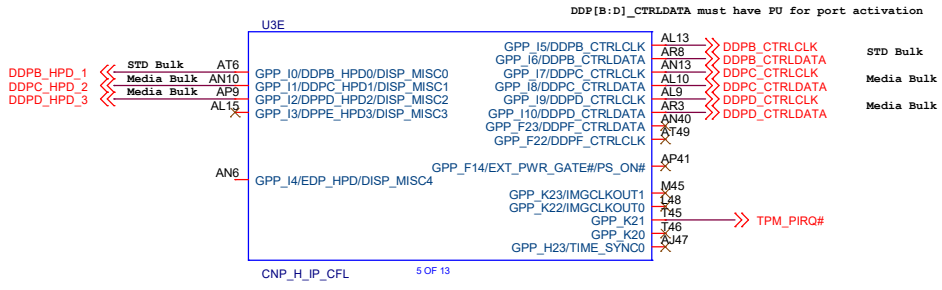

Title	14-PCH UART/SPI/GPP	
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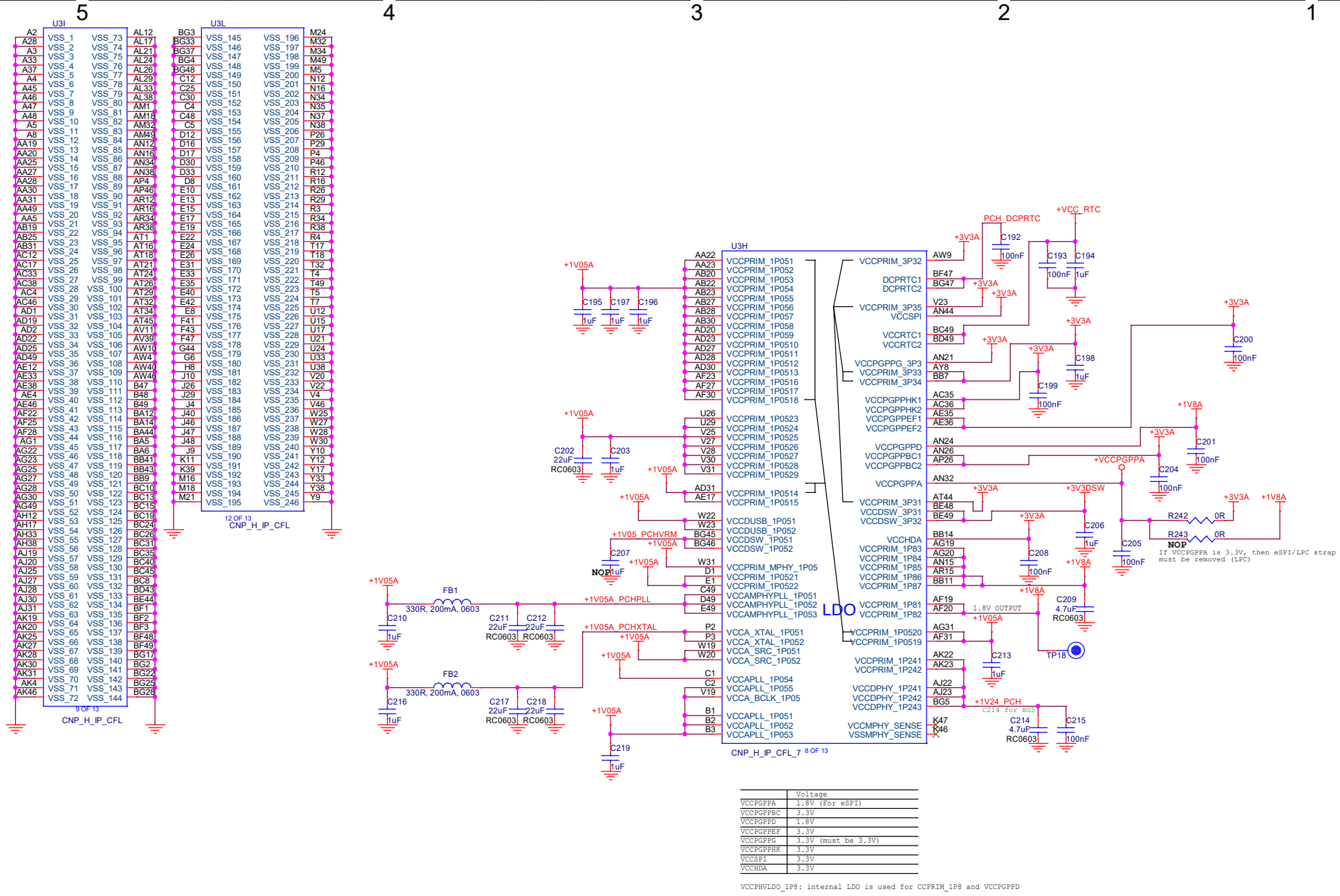

	Voltage
VCCPGPPA	1.8V (For eSPI)
VCCPGPPBC	3.3V
VCCPGPPD	1.8V
VCCPGPPEF	3.3V
VCCPGPPC	3.3V (must be 3.3V)
VCCPGPPHK	3.3V
VCCSPI	3.3V
VCCHDA	3.3V

VCCPHVLDO_1P8: internal LDO is used for CCPRIM_1P8 and VCCPGPPD

Title	15-PCH PWR/GND
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+VCC_CORE, +VCC_GT

U9 — ISL69137 — PWM: 3.3V logic

U8 / U10 / U12 / U14 — CORE PH 0 / CORE PH 1 / CORE PH 2 / CORE PH 3 — SPS, ISL99227, 60A — 0.36uH,36A,0.82mOhm

U13 — GT PH 1 — SPS, ISL99227, 60A — 0.36uH,36A,0.82mOhm

U15 — GT PH 0 — SPS, ISL99227, 60A — 0.36uH,36A,0.82mOhm

U11 — FSA266

Q2 — Dual N,0.5A,20V

Q6, Q8, Q29, Q30 — Dual N,0.5A,20V

PMBUS Address = 60

NOP

BYPASS

Title	16-PWR CPU CORE/GT
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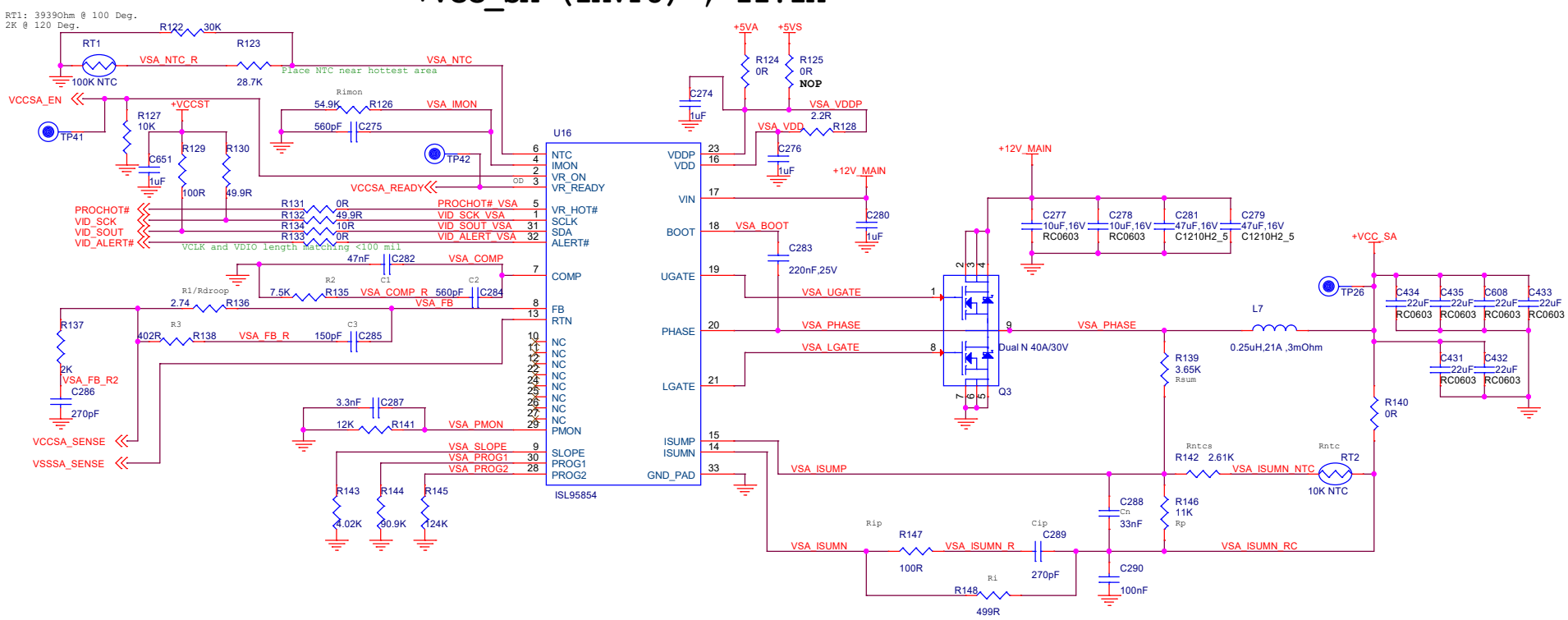
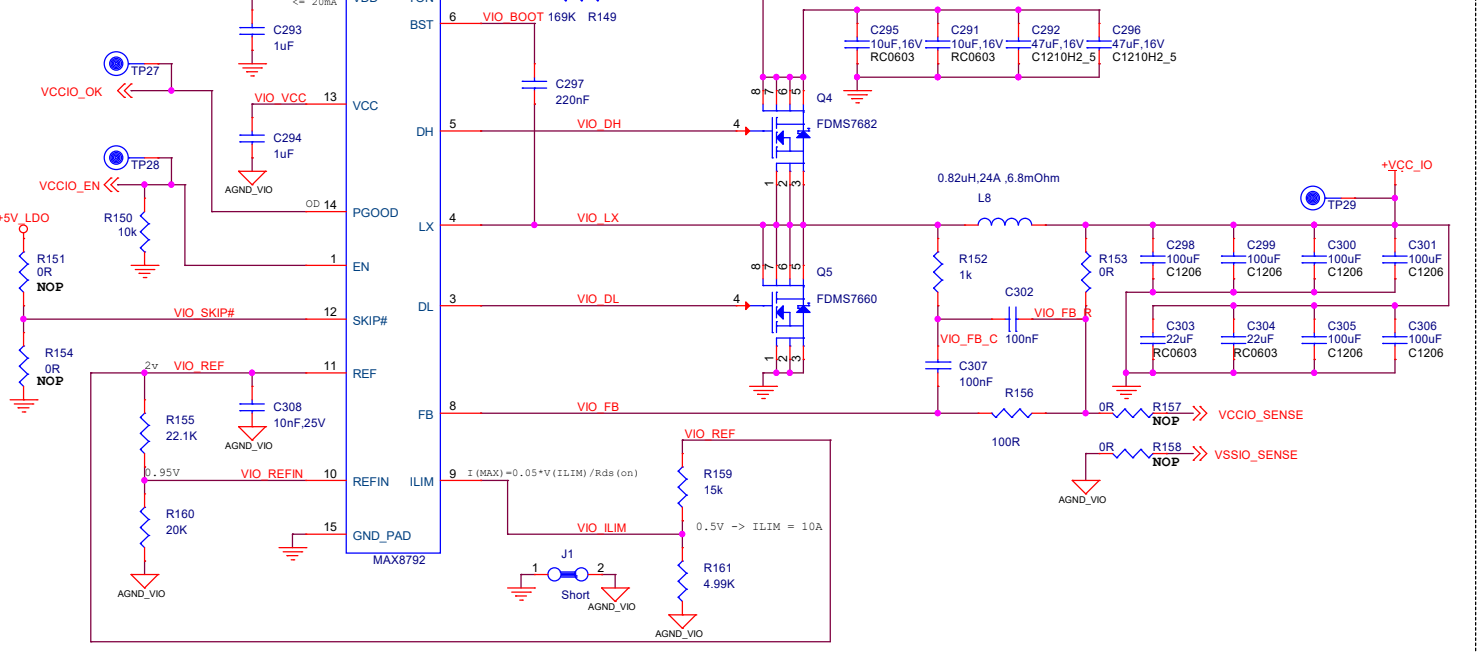
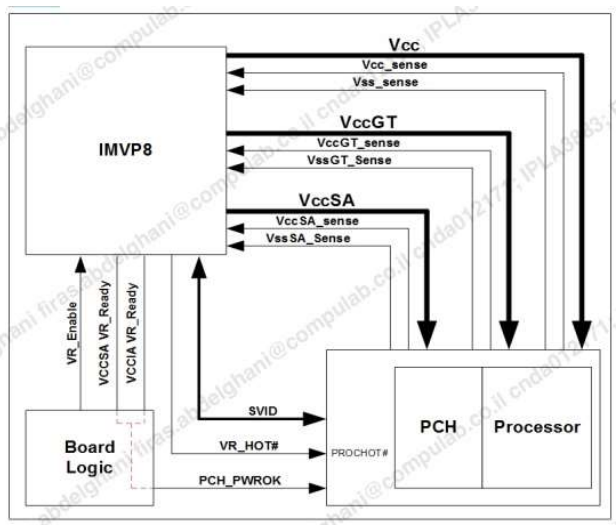
+VCC_SA (IMVP8) , 11.1A



VCC_IO (0.95V) , 7A





Title	17-PWR CPU SA/IO	
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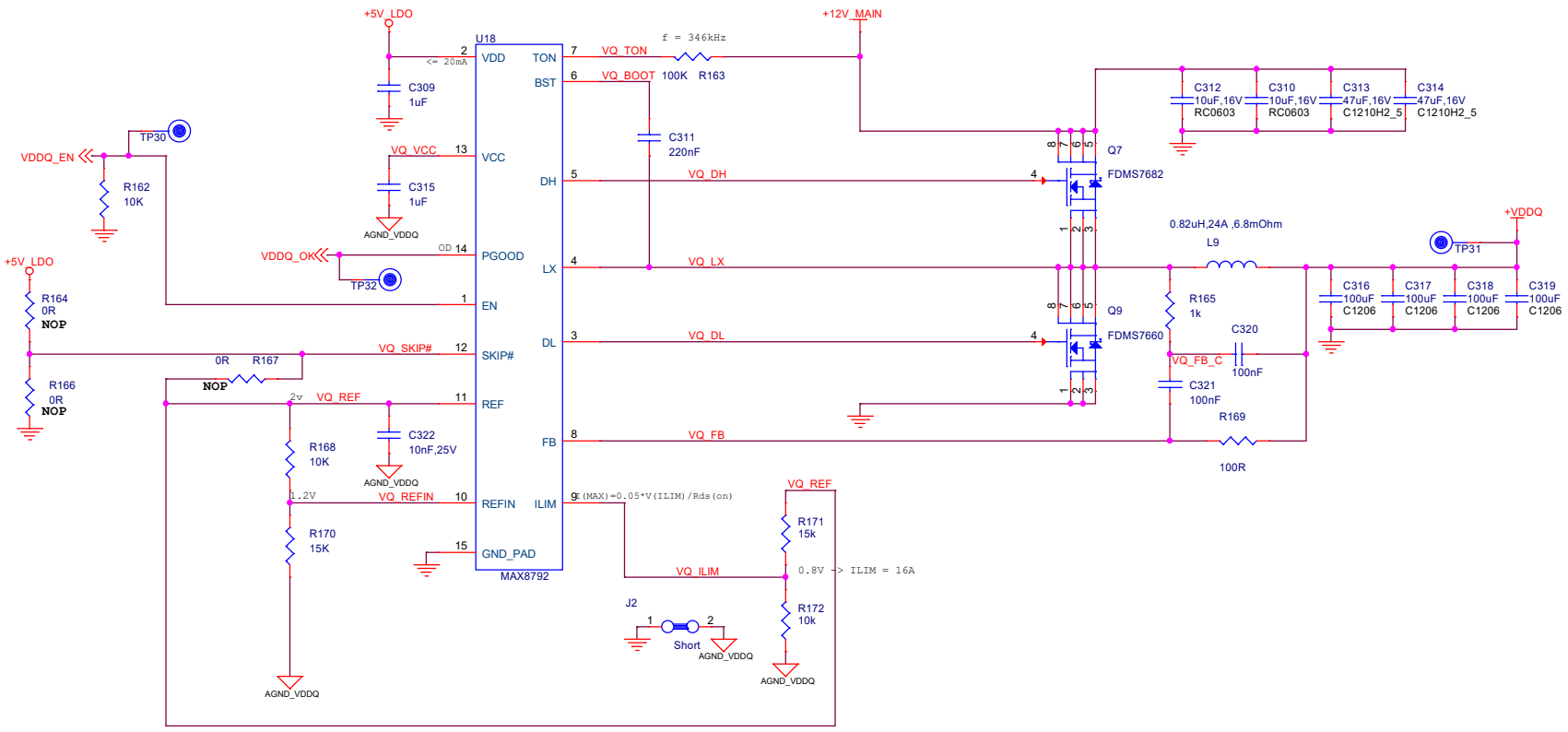
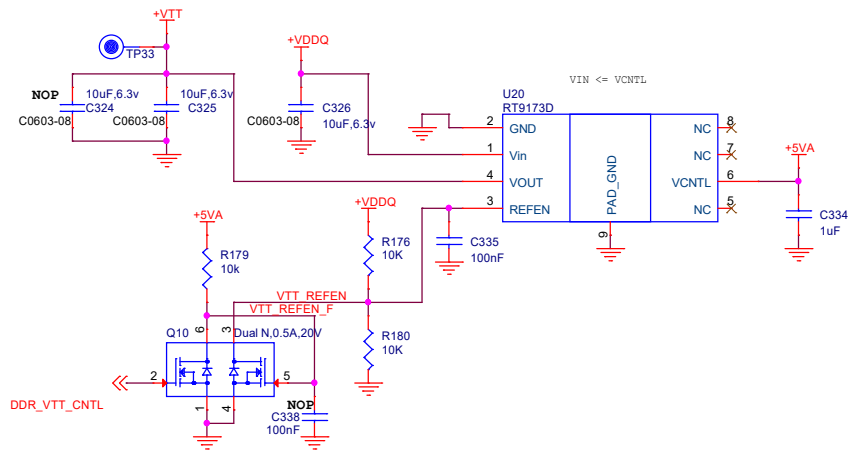
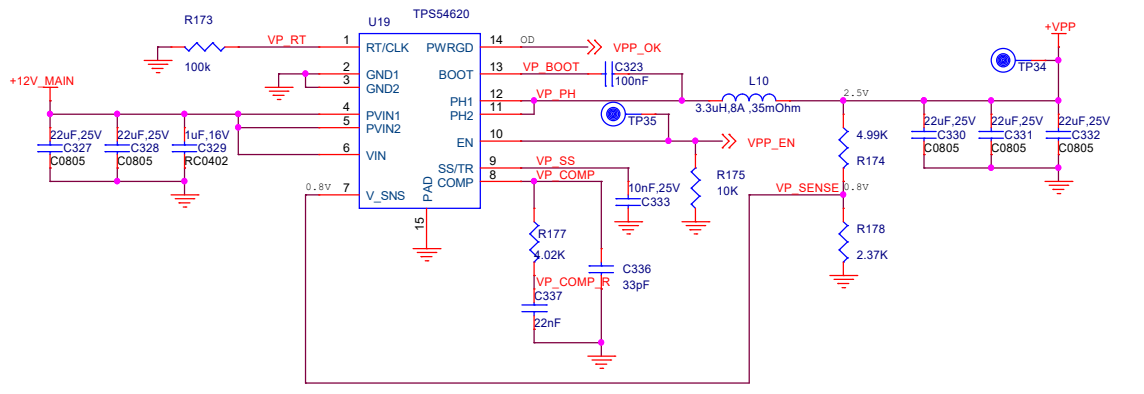
VDDQ = 1.2V , 15A



VTT = 0.6V , 0.75A



VPP = 2.5V , 0.6A



Title	18-PWR VDDQ/VTT/VPP	
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3.3V , 13A

U21 MAX8792 — VDD, TON, BST, VCC, DH, LX, DL, PGOOD, EN, SKIP#, REF, FB, ILIM, REFIN, GND_PAD

+5V_LDO → VDD (<= 20mA) via C339 1uF; VCC via C349 1uF; AGND_V33

+12V_MAIN → f = 490kHz; V33_TON → TON via 200K R181

V33_BOOT → BST via C344 100nF

V33_DH → DH → Q13 FDMS7682; C345 10uF,16V RC0603; C346 10uF,16V RC0603; C347 47uF,16V C1210H2_5; C348 47uF,16V C1210H2_5

V33_LX → LX; L11 2.2uH,14A ,18mOhm; +3V3DSW via TP38

V33_DL → DL → Q18 FDMS7660

C353 100uF C1206; C354 100uF C1206; C355 100uF C1206; C356 100uF C1206

C357 NOP 100uF C1206; C358 NOP 100uF C1206; C359 100uF C1206

R193 6.49K

V33_FB → FB; 2v V33_REF; R195 15k; C361 100nF NOP; R196 10k

V33_ILIM → ILIM; 0.8V (16A max); R199 10k

V33DSW_OK (OD) → PGOOD via TP39

+5V_LDO → TP40; V33DSW_EN → EN via 0R R190 NOP

V33_SKIP# → SKIP# via 0R R191 NOP; 0R R192 NOP

V33_REF → REF via C360 10nF,25V

J3 Short AGND_V33

+3V3A , 3A

NDS335N,3A Q11; +12V_MAIN; R183 10k; +3V3DSW; R187 10k; V33A_GATE

C340 22uF,6.3v C0805; C341 100uF C1206; TP36 +3V3A

C351 220nF; Q14 NDS335N,3A; R185 100R; V33A_DIS; Q15 NDS335N,3A

V33A_EN#; NOP R189 10k

+3V3S , 10A

FDMS7682,15A Q12; +12V_MAIN; R184 10k; +3V3DSW; V33S_GATE; R188 10k

C342 22uF,6.3v C0805; C343 100uF C1206; TP37 +3V3S

C352 220nF; Q16 NDS335N,3A; R186 100R; V33S_DIS; Q17 NDS335N,3A

V33S_EN#

Plane stitching capacitors

+5VA: C362 C363 C364 C365 C366 (220nF)

C367 C368 C369 C370 C371 (220nF)

C486 C650 (220nF)

+3V3A: C534 C612 C618 C645 C646 (220nF)

C647 C648 C649 (220nF)

+5V_LDO, 500mA

+12V_MAIN; LT3065 U24 — VIN, VOUT, SHD#, IMAX, GND, ADJ REF/BP, PWRGD

1uF,16V C373 RC0402

TP43 +5V_LDO

20K R202; C375 2.2uF; C376 2.2uF

V5LDO_FB (0.6V); V5LDO_SS; C382 10nF,25V; R204 2.74K

5V , 15A

+5V_LDO → VDD (<= 20mA) via C374 1uF; VCC via C372 1uF; AGND_V5

+12V_MAIN → f = 423KHz; V5_TON → TON via 357K R203

V5_BOOT → BST via C377 100nF

V5_DH → DH → Q19 FDMS7682; C378 10uF,16V RC0603; C379 10uF,16V RC0603; C380 47uF,16V C1210H2_5; C381 47uF,16V C1210H2_5

V5_LX → LX; L13 2.2uH,14A ,18mOhm; +5VA via TP44

V5_DL → DL → Q21 FDMS7660

C383 100uF C1206; C384 100uF C1206; C385 1uF,50V RC0603

R208 7.5K

V5_FB → FB; 2v V5_REF; R214 15k; C391 100nF NOP; R213 4.99K

I(MAX)=0.05*V(ILIM)/Rds(on); V5_ILIM → ILIM; 0.8V (16A max); R215 10k

J4 Short AGND_V5

V5A_OK → PGOOD via TP46

V5A_EN → EN via R206 10k

+5V_LDO → NOP 0R R205 V5_SKIP#; NOP 0R R207; NOP 0R R211

V5_REF → REF via C390 10nF,25V

Q20 FDMS7682,15A; +12V_MAIN; R209 10k; +3V3DSW; V5S_GATE; R212 10k; V5S_EN#

C389 100nF; Q22 NDS335N,3A; Q23 NDS335N,3A; R210 100R; V5S_DIS

C386 1uF,50V RC0603; C387 100uF C1206; C388 NOP 100uF C1206; TP45 +5VS

Title	19-PWR 3.3/5/1.8		
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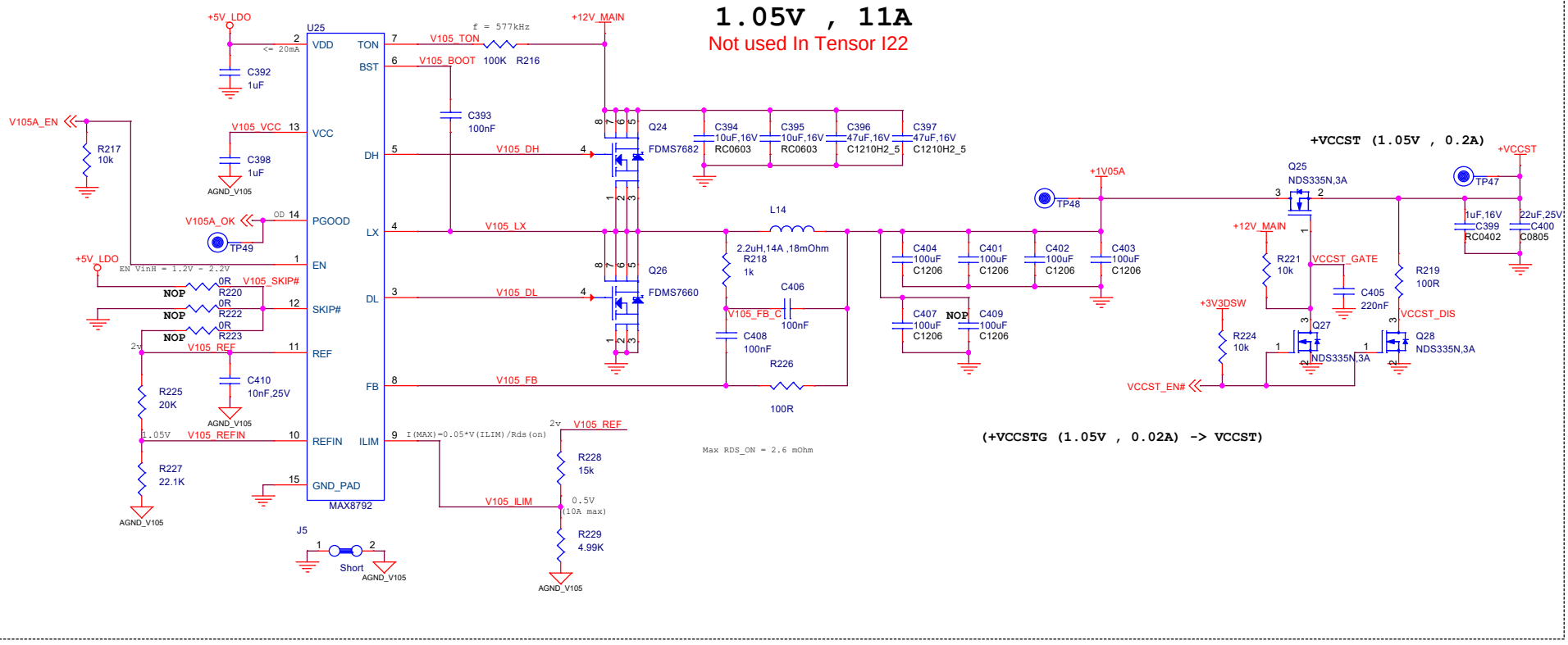
1.05V , 11A

Not used In Tensor I22



Title	20-PWR 12/1.05	
Size A3	Document Number SBC-CLH	Rev 1.3
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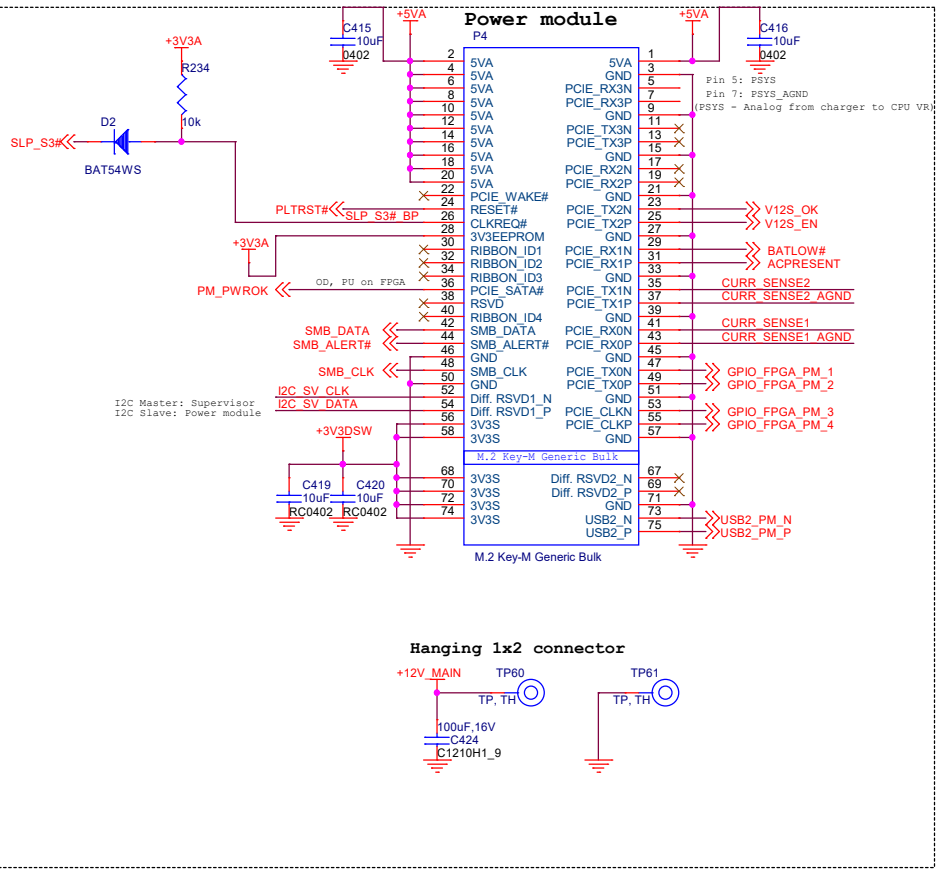
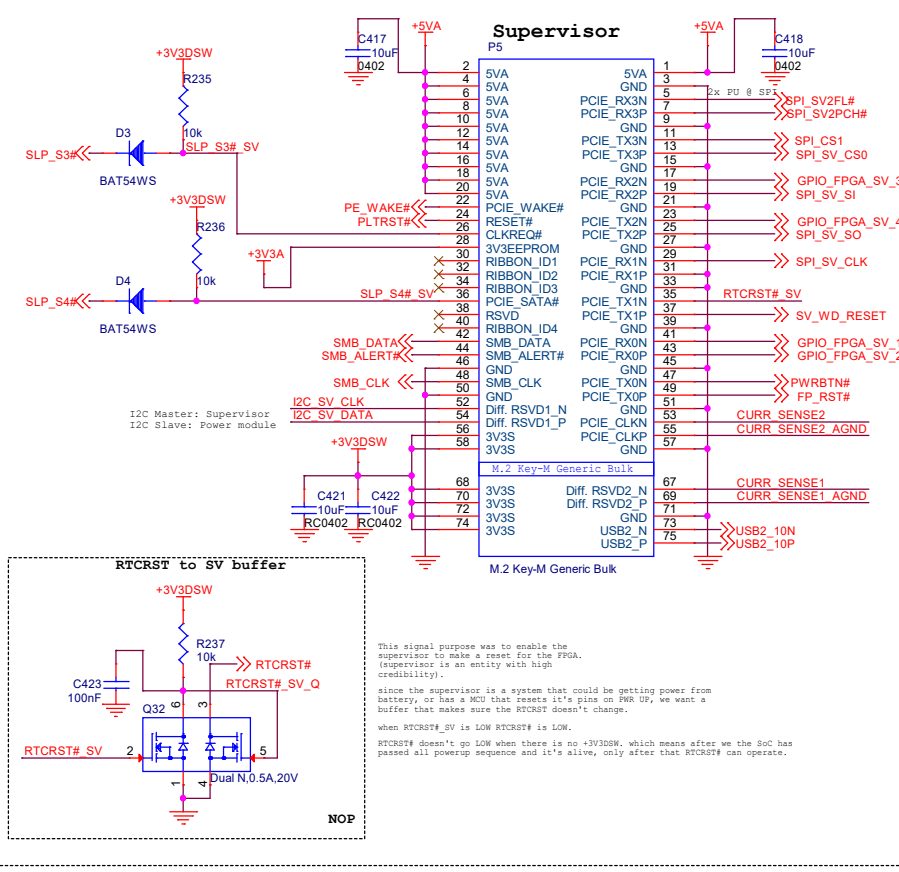
Power module



Supervisor



RTCRST to SV buffer

This signal purpose was to enable the supervisor to make a reset for the FPGA. (supervisor is an entity with high credibility).

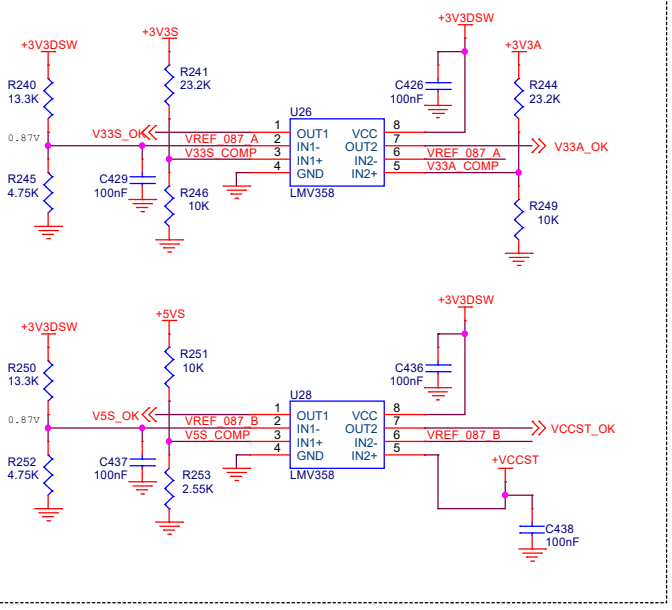
since the supervisor is a system that could be getting power from battery, or has a MCU that resets it's pins on PWR UP, we want a buffer that makes sure the RTCRST doesn't change.

when RTCRST#_SV is LOW RTCRST# is LOW.

RTCRST# doesn't go LOW when there is no +3V3DSW. which means after we the SoC has passed all powerup sequence and it's alive, only after that RTCRST# can operate.

Hanging 1x2 connector

+3V3S, +5VS, +3V3A, +VCCST PWRGD



Title	21-PWROK/PM/SV/LED		
Size A3	Document Number SBC-CLH		Rev 1.3
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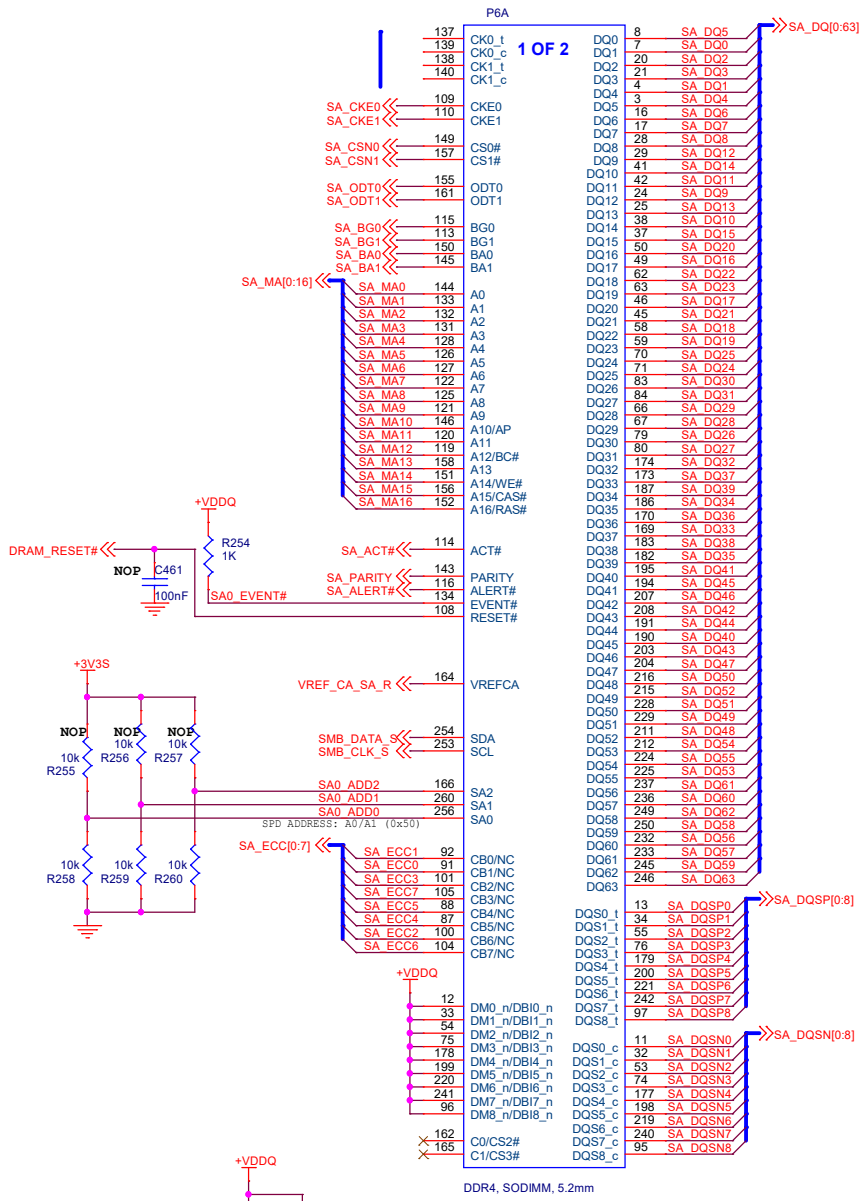
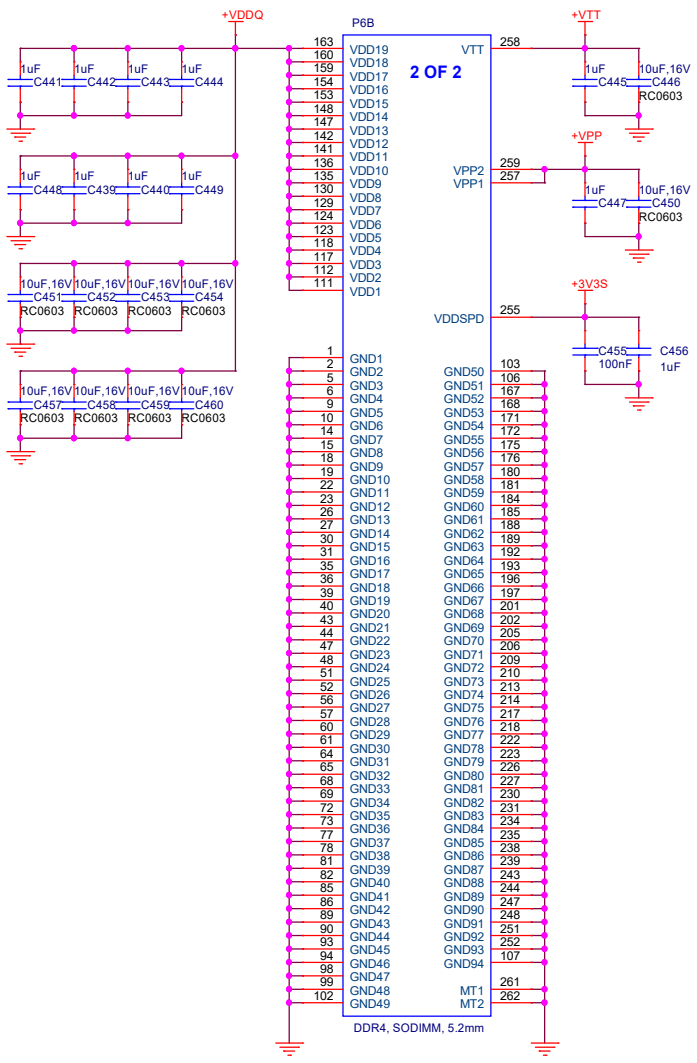
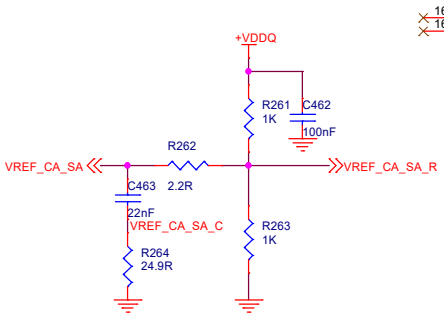
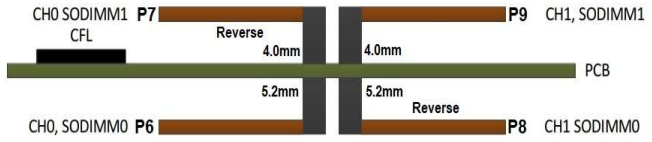
DDR4 CH A SODIMM 0



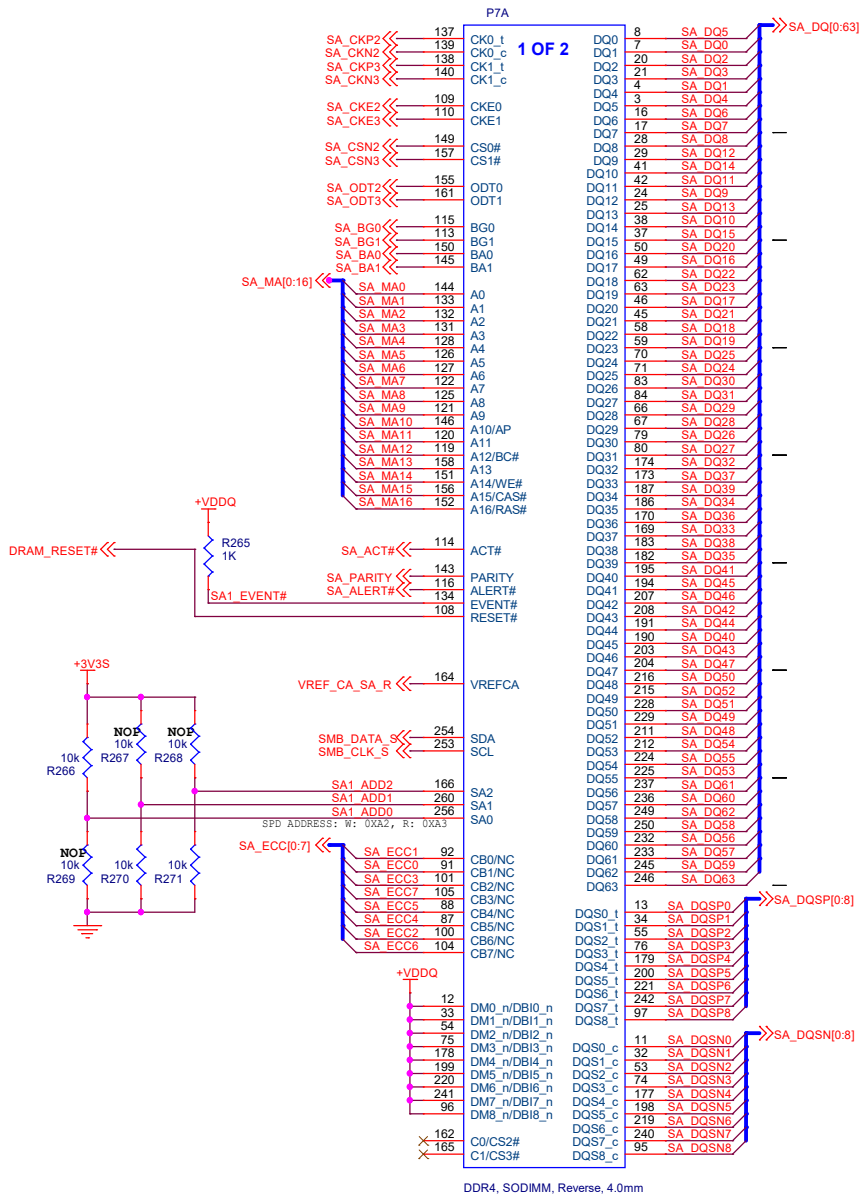


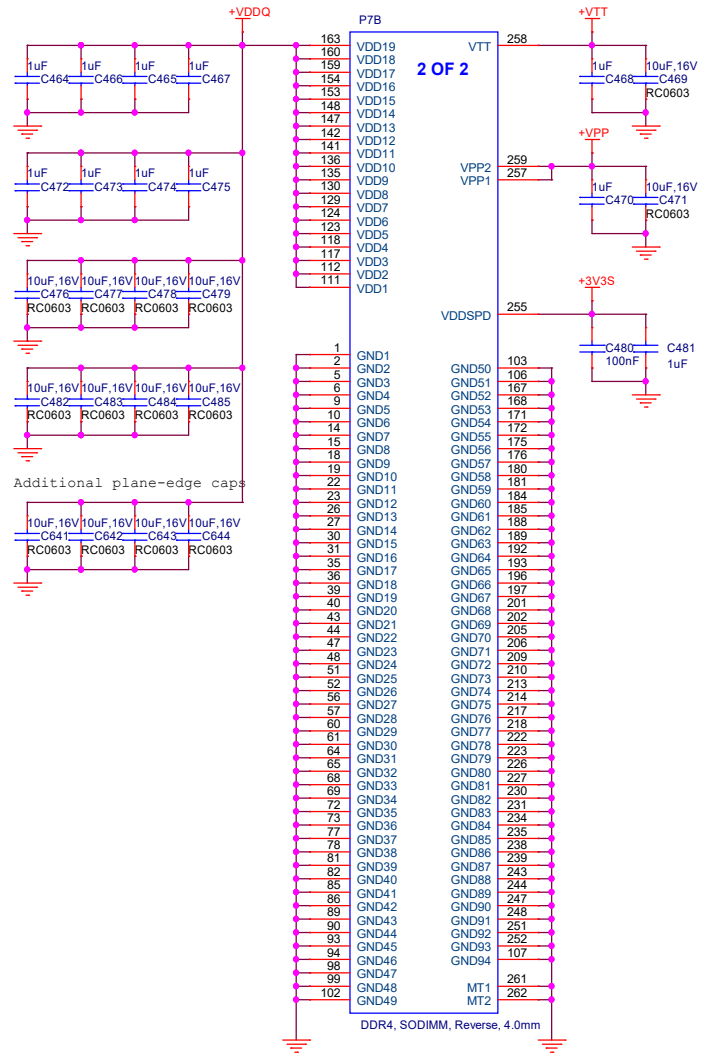


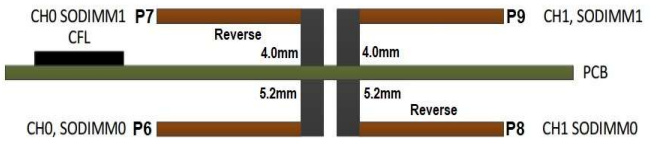


Title	22-DDR A0	
Size A3	Document Number SBC-CLH	Rev 1.3
Date: Thursday, June 24, 2021	Sheet 22 of 32	

DDR4 CH A SODIMM 1







Title	23-DDR A1	
Size A3	Document Number SBC-CLH	Rev 1.3
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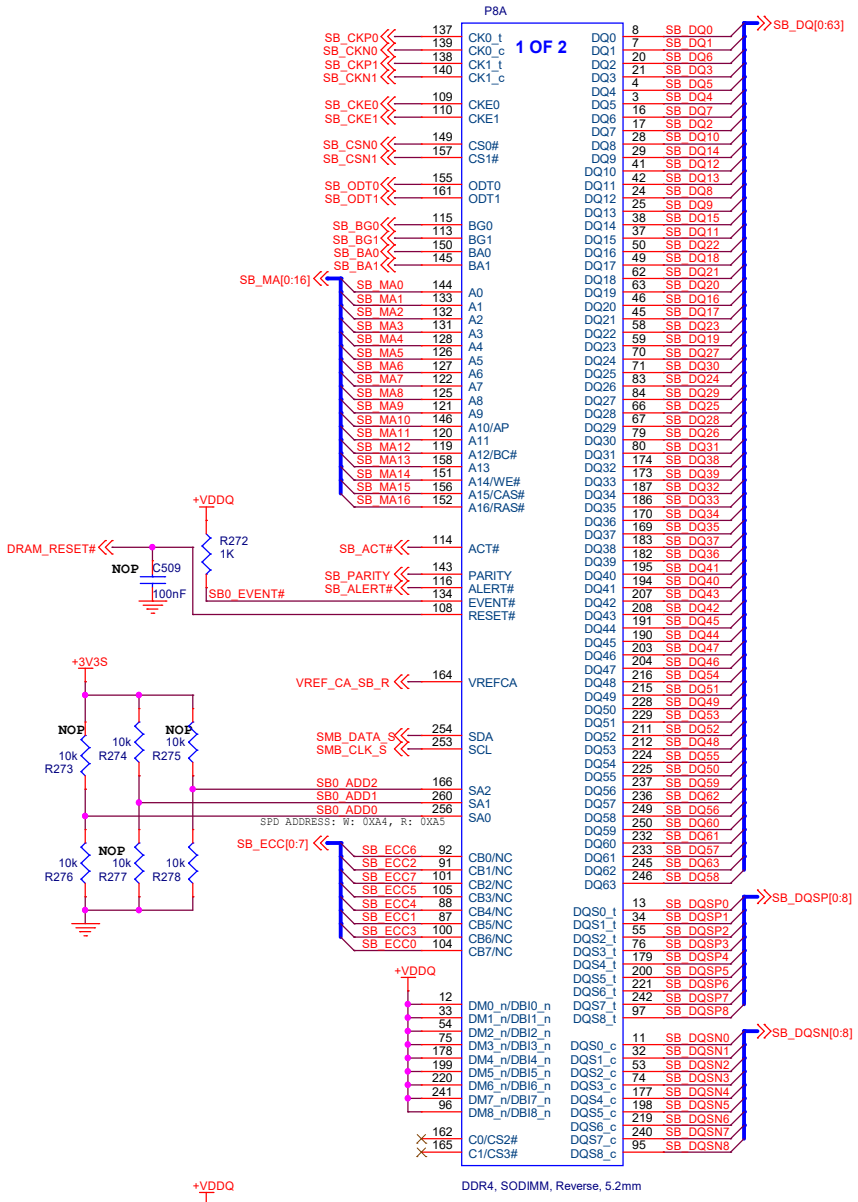
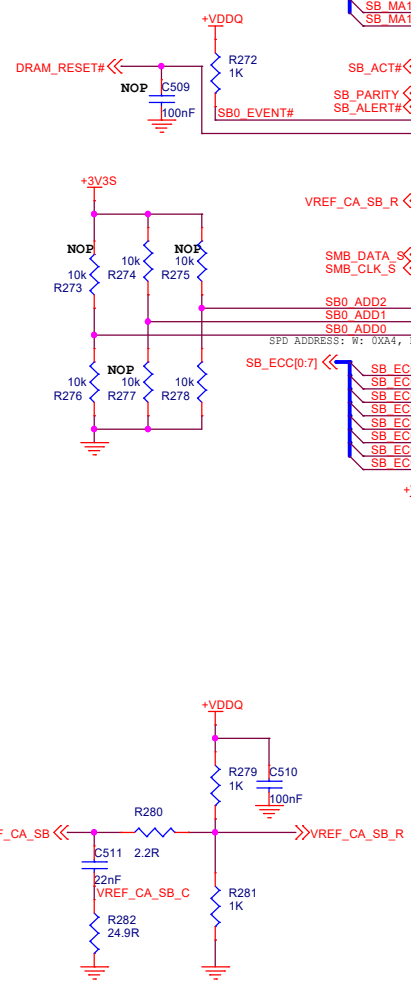
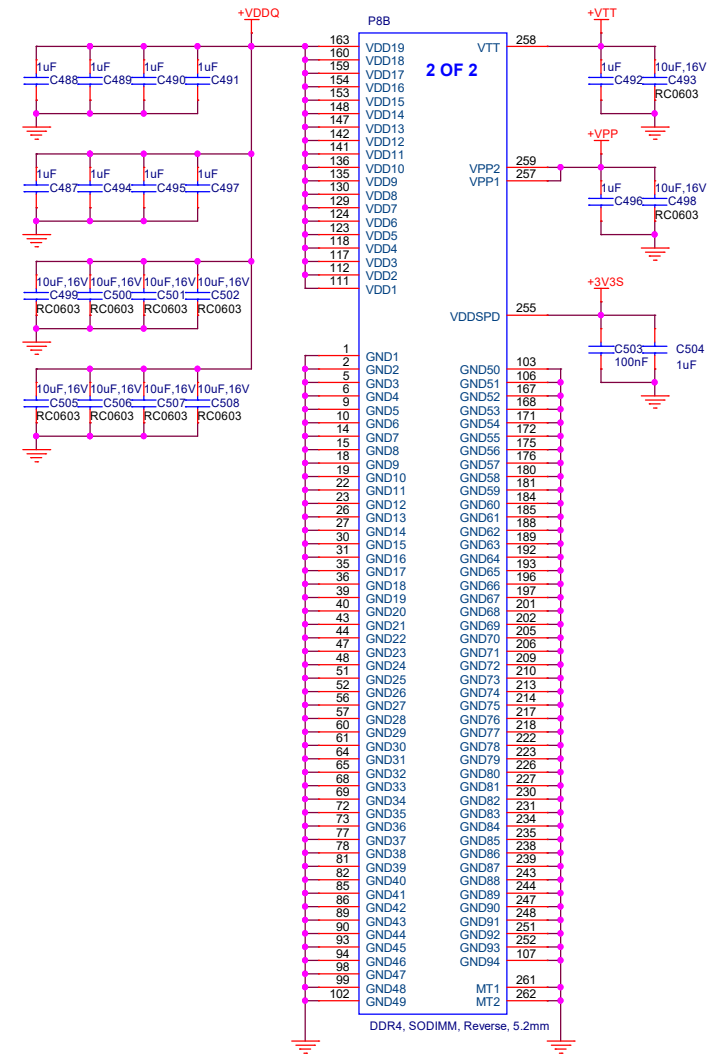
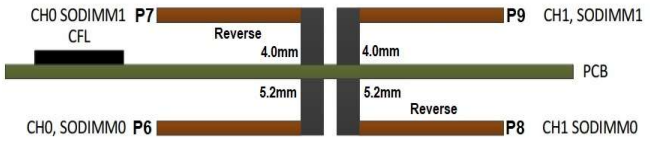
DDR4 CH B SODIMM 0









Title	24-DDR B0	
Size A3	Document Number SBC-CLH	Rev 1.3
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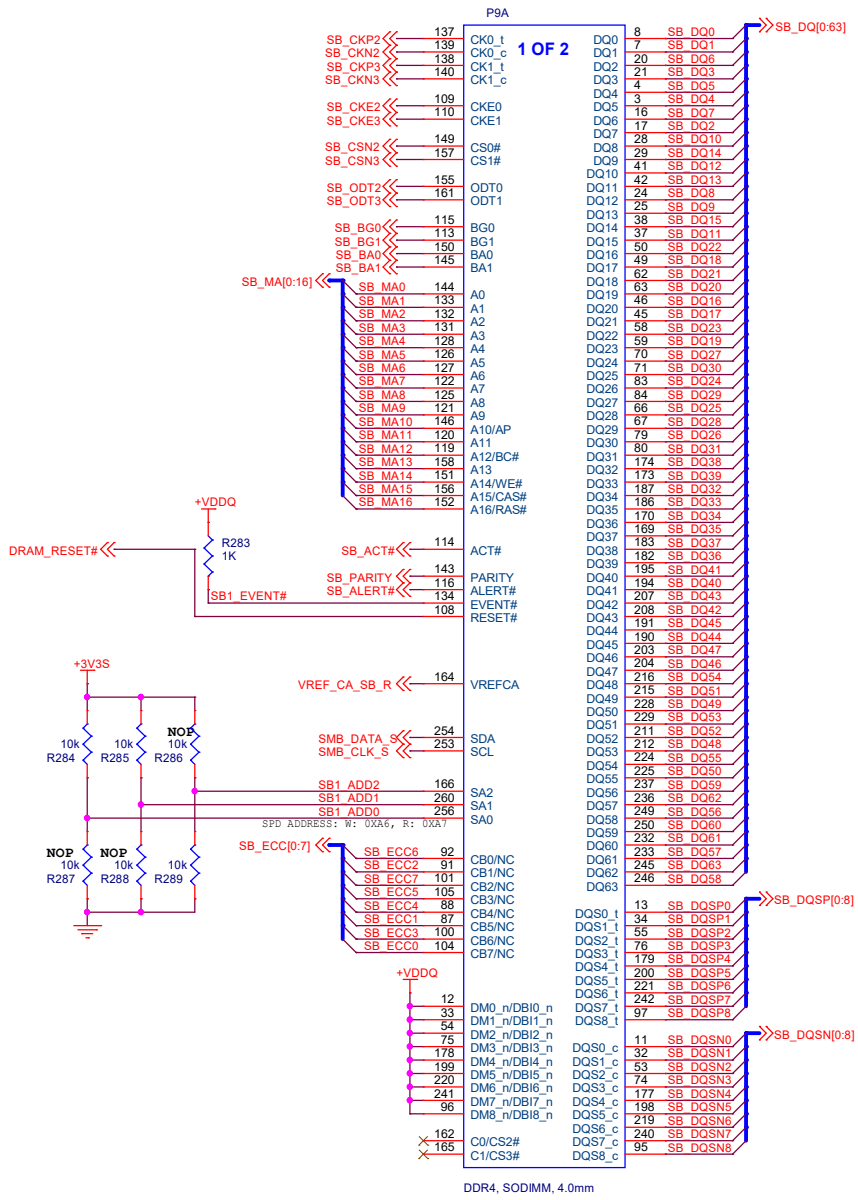
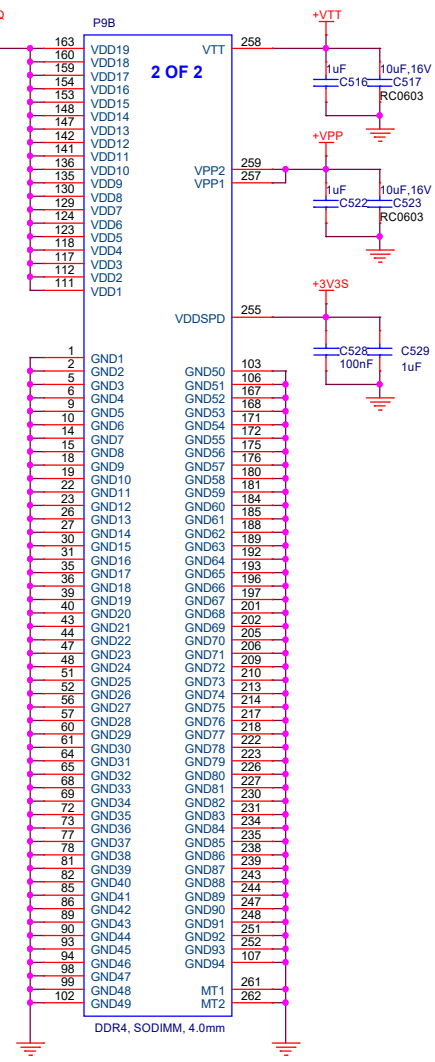
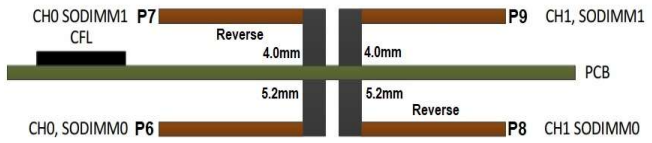
DDR4 CH B SODIMM 1







Title	25-DDR B1	
Size A3	Document Number SBC-CLH	Rev 1.3
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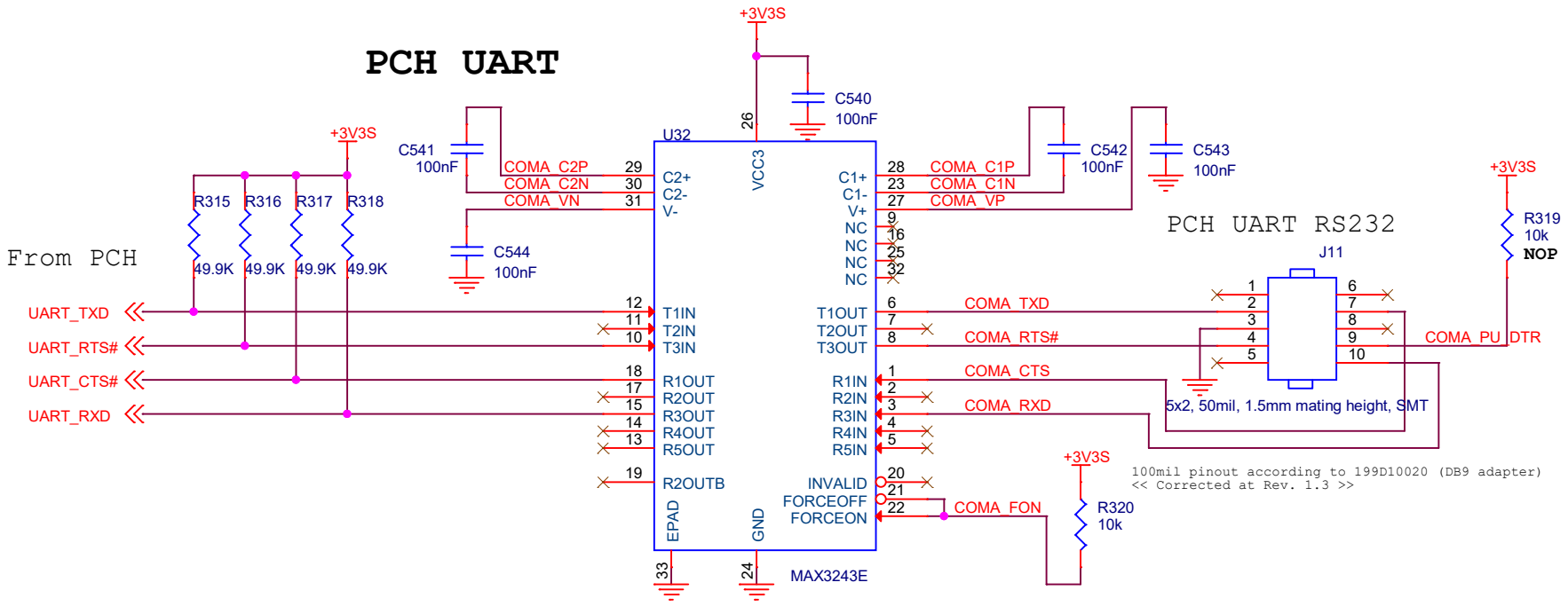
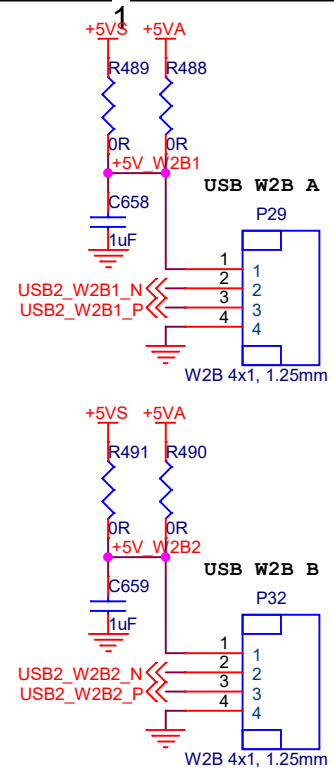
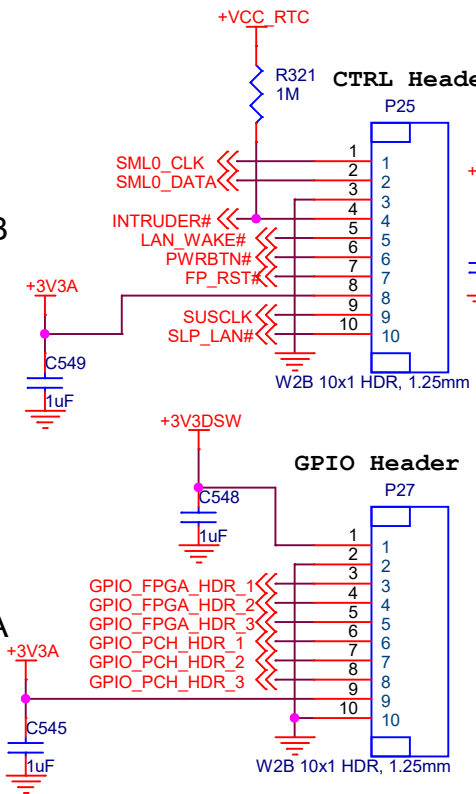
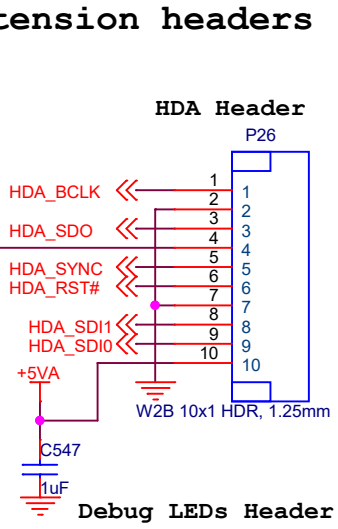
PCH UART

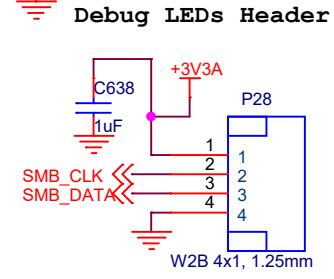


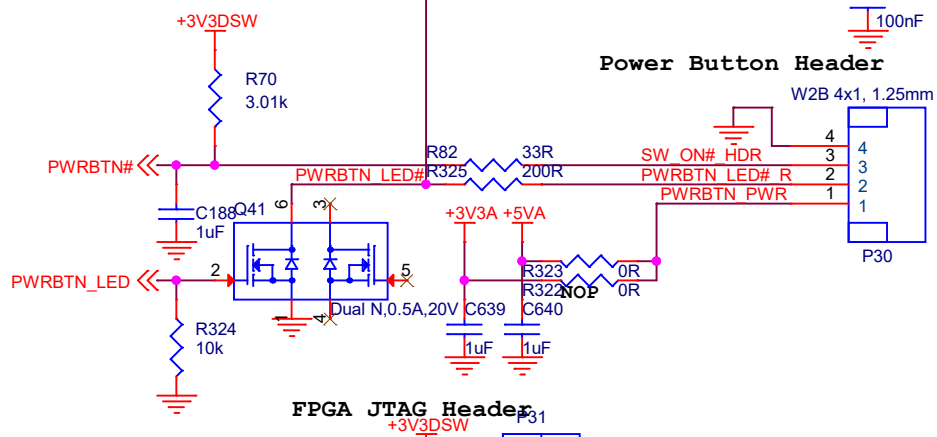


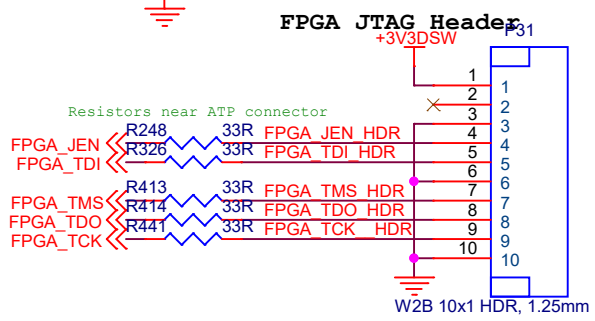
Extension headers











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Size A4	Document Number SBC-CLH	Rev 1.3
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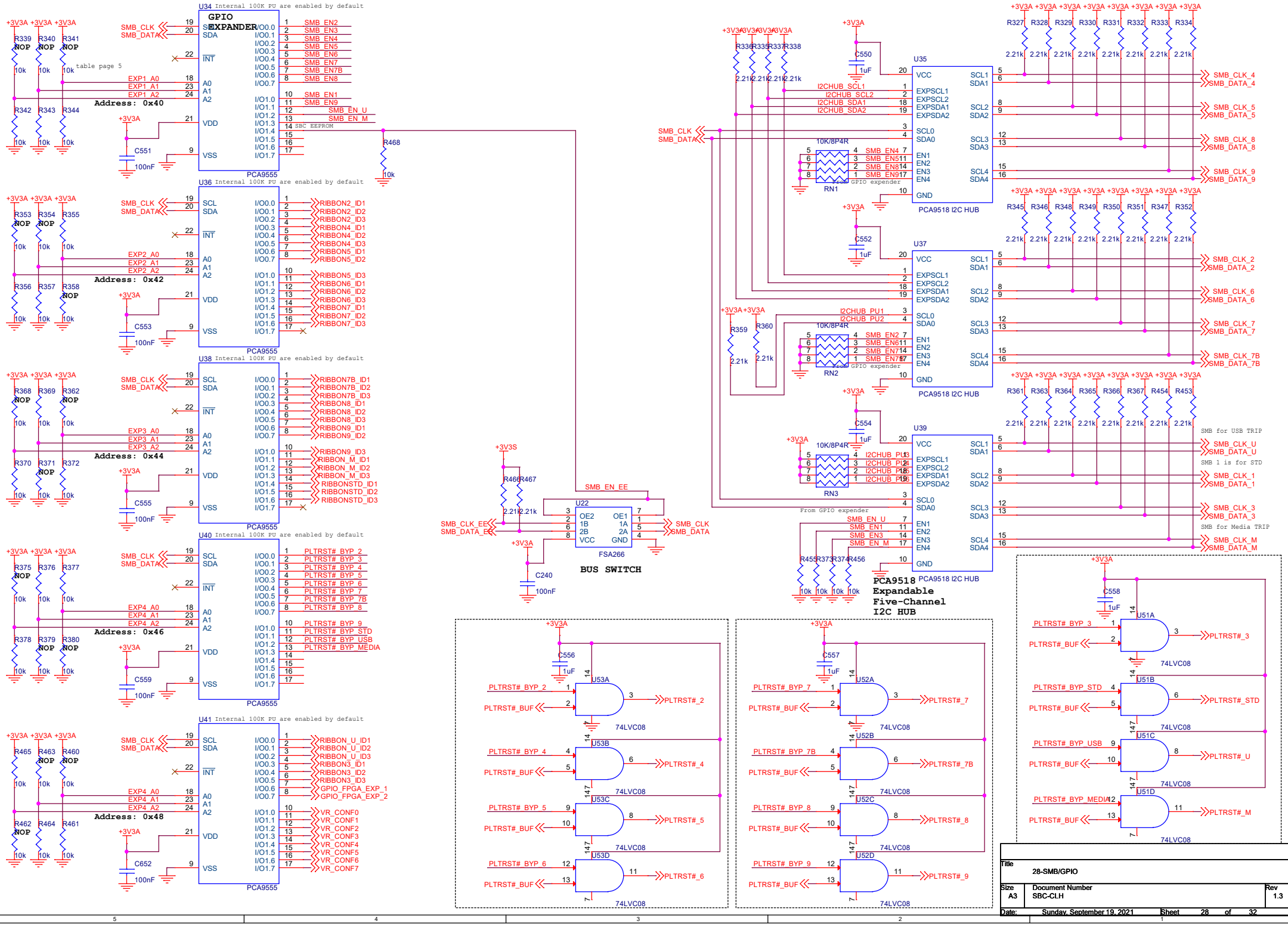

Title	28-SMB/GPIO
Size	A3
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STD TRIP

P10

M.2 Key-M STD Bulk

HPD: level shifter/current blocking must be implemented on TEL

DP 1 dual mode

Q34, Q35 — Dual N,0.5A,20V

U45, U46 — 7SZ05

USB TRIP

P11

M.2 Key-M USB Bulk

D6 — BAT54WS

Media TRIP

P12

M.2 Key-M Media Bulk

HPD: level shifter/current blocking must be implemented on TEL

DP 2 dual mode

Q36, Q38 — Dual N,0.5A,20V

U47, U49 — 7SZ05

DP 3 dual mode

Q37, Q39 — Dual N,0.5A,20V

U48, U50 — 7SZ05

Media TRIP alert LED

Q93 — Dual N,0.5A,20V

STD TRIP alert LED

Q94 — Dual N,0.5A,20V

USB TRIP alert LED

Q95 — Dual N,0.5A,20V

Title	29-TRIPS STD/MEDIA/USB	
Size A3	Document Number SBC-CLH	Rev 1.3
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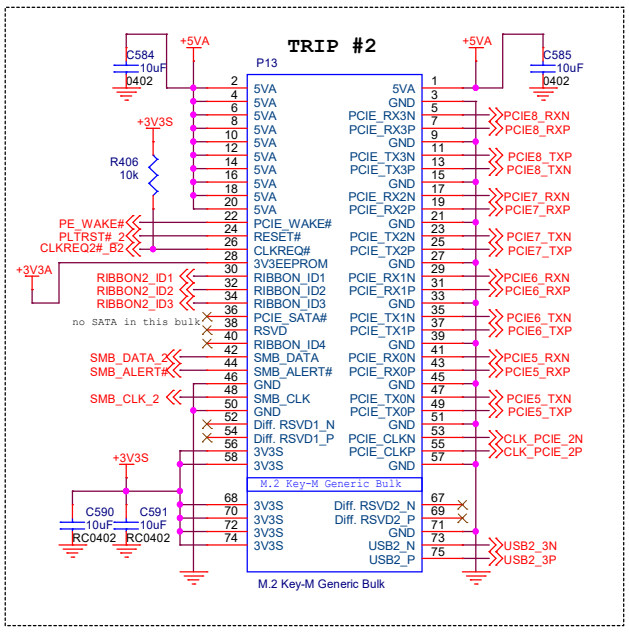
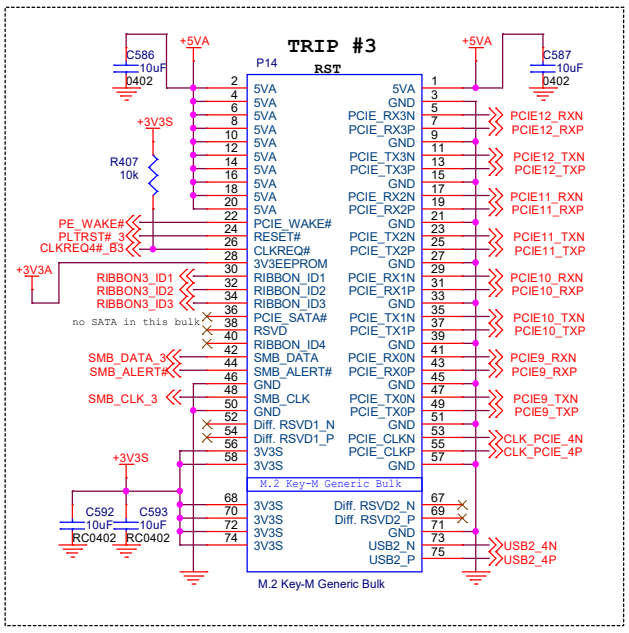
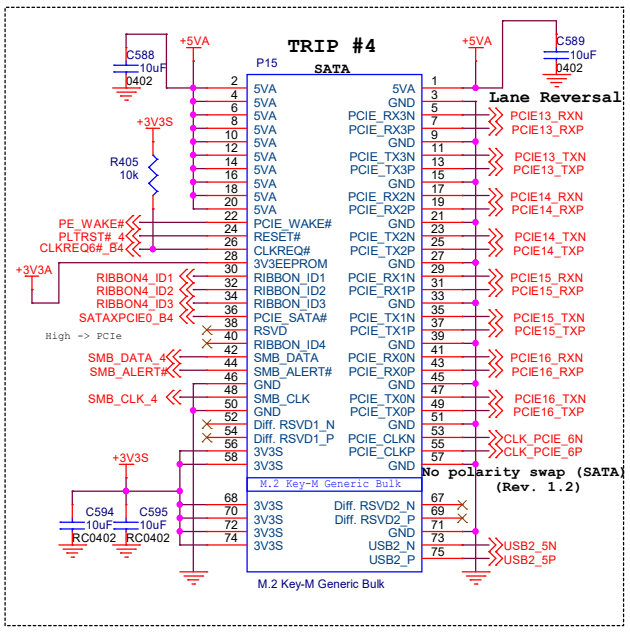
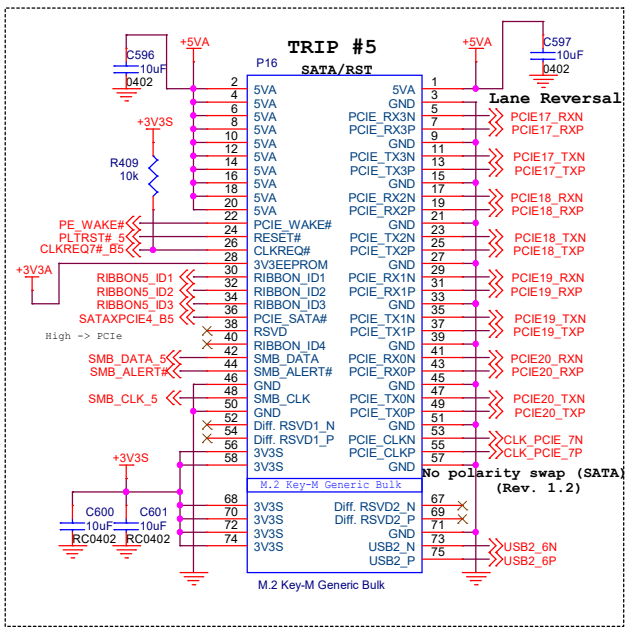
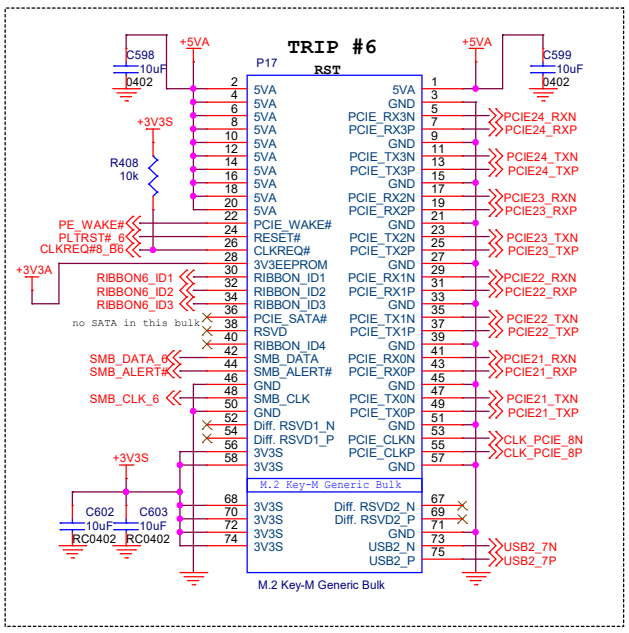
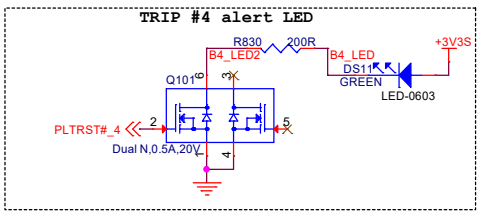


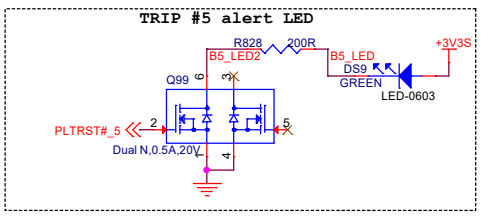


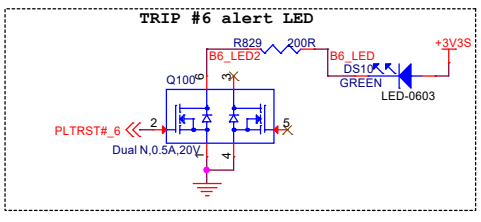




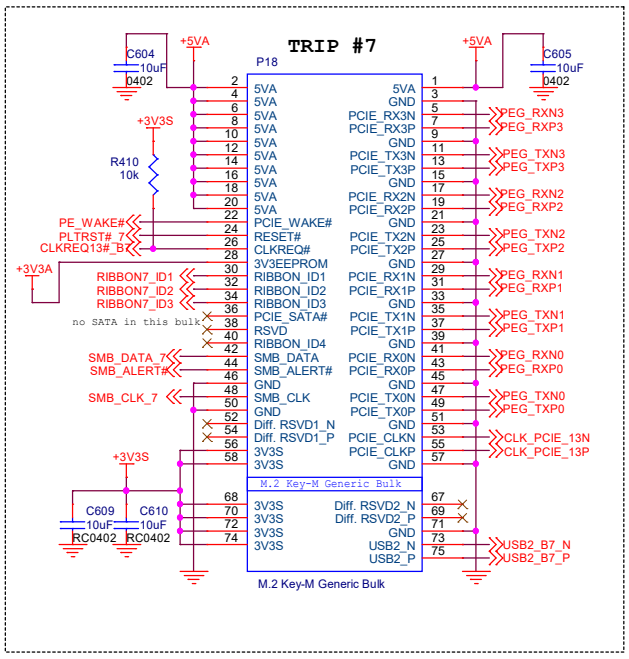


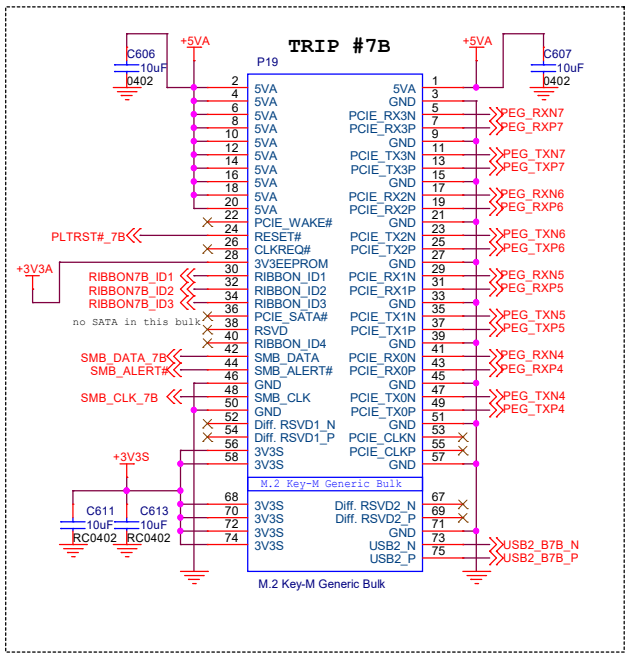


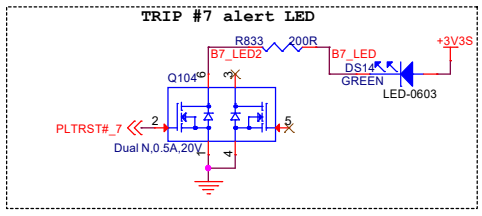


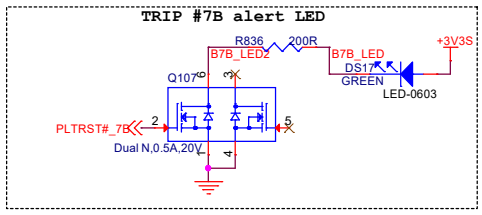


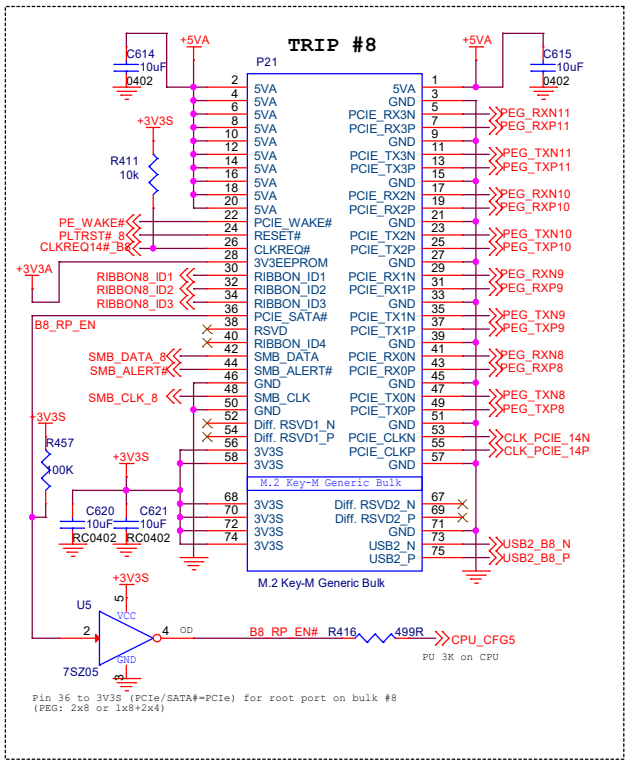
Title	30-TRIPS 2-6	
Size A3	Document Number SBC-CLH	Rev 1.3
Date: Monday, July 05, 2021	Sheet 30 of 32	

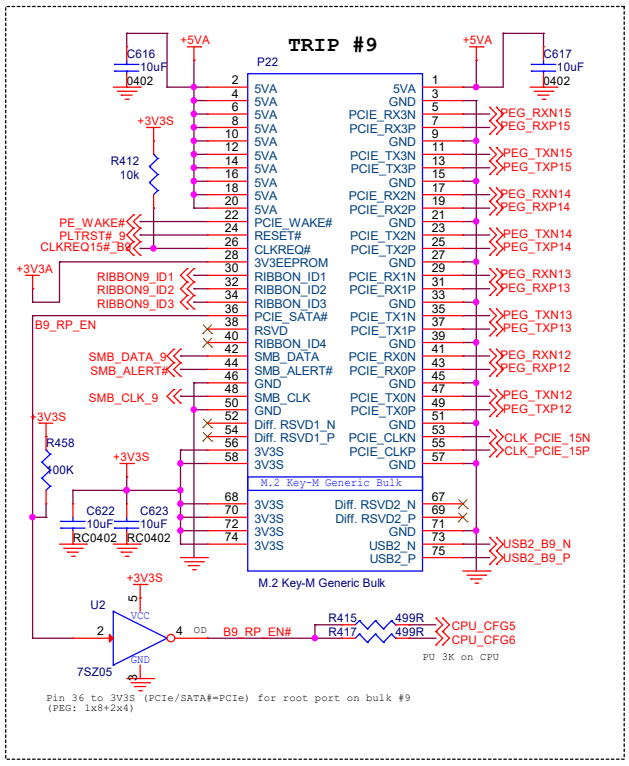


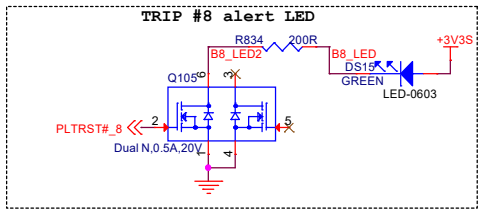


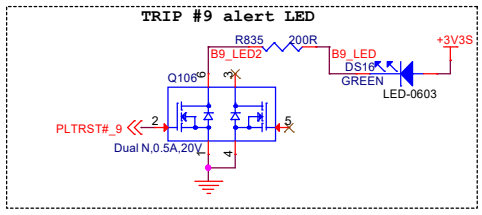












Title	31-TRIPS PEG 7-9	
Size A3	Document Number SBC-CLH	Rev 1.3
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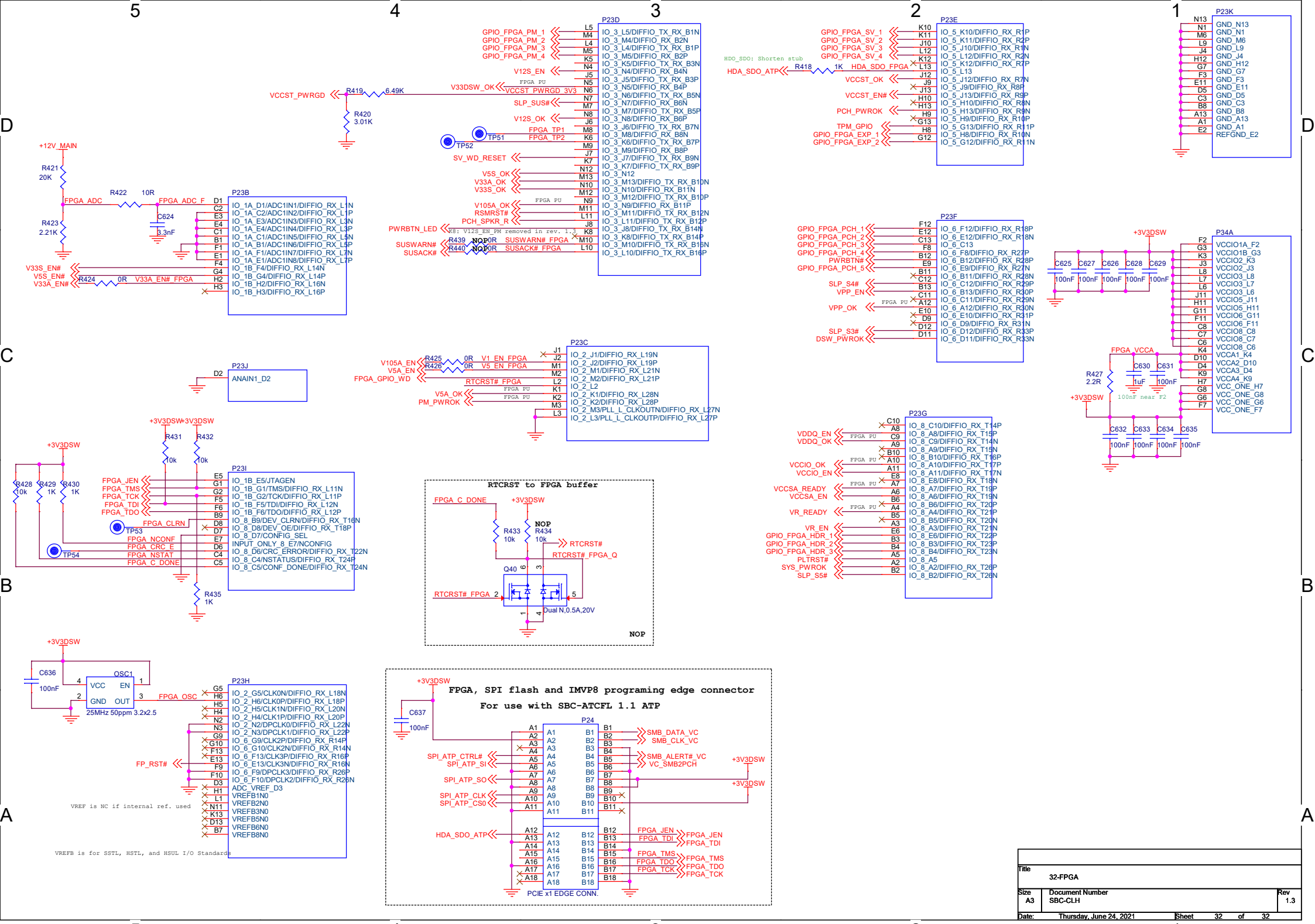

Title	32-FPGA
Size	A3
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