Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform

Customer Reference Board Schematics

Revision 1.0

December 2019

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Revision History

Document Number	Revision Number	Description	Revision Date
609003	0.5	• Initial Draft Release	January 2019
	0.7	• Added Power Meter Circuits. **NOTE:** Refer to PDG for PDBOM recommendation. The PDBOM provided in this design is specific to the RVP Implementation.	February 2019
	0.71	• Updated SoC Symbol file: — Sub-parts 2 and 3 are updated for alignment. — Sub-part 8 updated for latest ball-map specification (Rev 0.7).	March 2019
	0.8	• Updated SoC symbol file. • Replaced R3G68 resistor by 4.7K PU. • Replaced R6W9 resistor by 4.7K PU. • Changed R7U4 to 68.1K. • R8G15 stuffed.	July 2019
	1.0	• Updated SoC symbol to Rev 1.6.	December 2019

NOTE: Refer to Tiger Lake UP3 Platform Symbol (# 615721) for latest TGL UP3 symbol updates.

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REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE

TGL UP3 DDR4 SODIMM RVP

REV:- 1P0

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS.
   PLEASE REFER TO SPECIFIC PRODUCT PBA EPL FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

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CHK_BY <CHK_BY>	<CHK_BY_DATE>	TITLE TGL UP3 DDR4 SODIMM RVP			
ENGR_APVD <ENGR_APVD>	<ENGR_APVD_DATE>				
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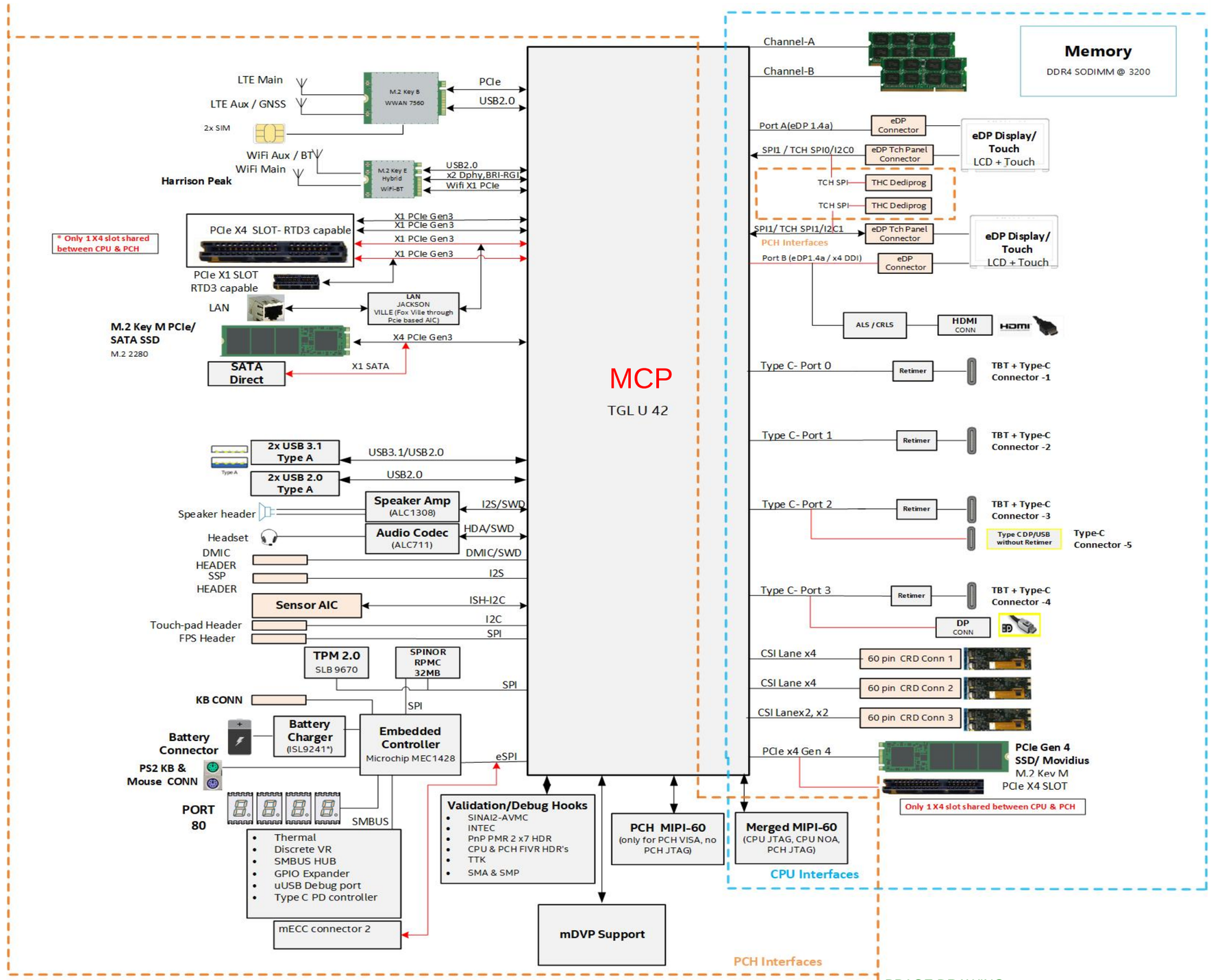
MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=BLOCK DIAGRAM]

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

RefDes	LED Description
DS4G1	V1P05_CTRL
DS4G2	VNN_CTRL
DS8H5	S3 STATE
DS8H3	S4 STATE
DS8H4	S5 STATE
DS8H2	DSW STATE
DS8H1	M0/M3 STATE
DS3H1	ME PWR Gate

RefDes	LED Description
DS8G6	SLP S0 LED
DS8G4	PWRGD
DS8G5	CATERR
DS6G1	C10 GATE
DS6G2	CS INDICATE

RefDes	LED Description
DS8H6	CAPS LOCK
DS8H7	NUM LOCK
DS7G1	POWER BUTTON
DS7H1	BAT STATUS LED

RefDes	LED Description
DS9B1	SATA Direct connect DEVSLP
DS9E1	M.2 SSD DEVSLP
DS8G7	SATA ACTIVITY
DS6D1	PCIE LINK DOWN
DS4G4	WLAN
DS4G3	BT
DS7D1	WWAN

Error Type	Error Code	Caps Lock LED (DS9H2)	Scroll Lock LED (DS7G1)	Num Lock LED (DS9J1)
No Error	0	Off	Off	Off
RSMRST_PWRGD_N	1	Off	Off	Flash
PM_SLP_S5_N	2	Off	Flash	Off
PM_SLP_S4_N	3	Off	Flash	Flash
PM_SLP_S3_N	4	Flash	Off	Off
PM_SLP_M_N	5	Flash	Off	Flash
ALL_SYS_PWRGD	6	Flash	Flash	Off
PLT_RST_N	7	Flash	Flash	Flash
DOCK_SYS_PWRGD_N	8	On	On	Flash
SUSWARNB	9	On	Flash	On

Note: KSC Thermal Shutdown is indicated by flashing of Num _Lock and Caps _ Lock LEDs alternatively.
DS7G1 acts as led indication for error code in case of any error otherwise works as power button LED

[PAGE_TITLE= LED DISCRIPTION]

MODULE REV DETAILS		
MODULE NAME	REV	DATE

Interface	WHL	TGL
Board ID		
PCIE Gen4 – DEKEL PHY	No	Yes
TYPE C	No	Yes
XTAL_IN	24MHz	38.4MHz
Memory	1 Channel	2 channel
CSI	No	Yes

No.	Changes	WHL	TGL	Status
1	XXDP_COMP	24.9 ohm PU to VCCIO	24.9 ohm PU to VCCIN /+VCC1P05_OUT_FET (default) on extra added pin on one of the spare pins of TGL_A0.	implemented
2	XXDDR_COMP[0]	121 ohm PD	121 ohm PD on Pin DW 49	implemented
3	XXDDR_COMP[1]	80.6 ohm PD	80.6 ohm PD on pin DW47	implemented
STRAP				
4	SVID DISABLE STRAP	J3B1 to 1-2	J3B1 to 1-X	WIP
5	GPPC_F10	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K	WIP
6	GPPC_F0*	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K	WIP

[PAGE_TITLE=Z0 VS A0 PINLIST]

MODULE REV DETAILS		
MODULE NAME	REV	DATE

TGL-U 42 ROW RVP's Mphy Allocation

			TGL U RVP mPHY allocation- DDR4		
PCIe Controller	Lane #	Flex IO	HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 3 (SV SKU)
x4 Controller 1	Lane 0	PCIE3_1_USB31_1	USB3/2 Type-A Con 1		HSIO Connector
	Lane 1	PCIE3_2_USB31_2	USB3/2 Type-A Con 2		
	Lane 2	PCIE3_3_USB31_3	M.2 Hybrid Key E- WLAN		
	Lane 3	PCIE3_4_USB31_4	M.2 Key-B WWAN		
x4 Controller 2	Lane 4	PCIE3_5	Lane 0 for x4 PCIe slot	x4 PCIe Slot	
	Lane 5	PCIE3_6	Lane 1 for x4 PCIe slot		
	Lane 6	PCIE3_7_LAN_0A_UFS_00	Jacksonville Gbe LAN		
	Lane 7	PCIE3_8_LAN_0B_UFS_01	x1 PCIe Slot		
x4 Controller 3	Lane 8	PCIE3_9_LAN_0C_UFS_1_00	M.2 Key M x4 SSD(Lane reversal for x4 PCIe)		
	Lane 9	PCIE3_10_UFS__1_01			
	Lane 10	PCIE3_11_SATA_0		SATA Direct Connect	
	Lane 11	PCIE3_12_SATA_1			
x4 Controller 4 (Gen 4 North side)	CPU Lane0	CPU_PCIE_0	M.2 Key M x4 SSD	x4 PCIe Slot	
	CPU Lane1	CPU_PCIE_1			
	CPU Lane2	CPU_PCIE_2			
	CPU Lane3	CPU_PCIE_3			

[PAGE_TITLE=TABLE - MPHY MAPPING]

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

IC name	ALC711 ES-1	ALC711 ES-2
package	QFN-48	QFN-48
Bilingual mode(HD-A/SdW)	O	O
Combo jack (HP+MIC2) + Line1	O	O
Line2 (In) port	O	O
SdW Master I/F	O	O
SdW Slave I/F	O	O
Line1(in)/Line2(in)	O	O
VAD energy detector	X	O
VAD buffer(64KB) with SRAM controller	X	O
USB type-c switch and analog switch	X	O
DMIC	2ch	2ch
HP JD type	JD port	Decide by AGPI and CC1/CC2 status
Power strap	Slew rate(MSB)	Slew rate/self-time turn off/SdW slave ID
GPIO2	X	O
LDO4	X	O
LINE2-VREFO	X	O

[PAGE_TITLE - ALC711 ES1 vs ES2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.9
Tue Oct 15 12:48:27 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	9	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

SRC CLK	SRC CLKREQ	TGL U RVP mPHY allocation- DDR4		
		HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 3 (SV SKU)
0	0	CPU Gen4 PCIE x4 M.2 SSD	CPU Gen4 x4 PCIe Slot	
1	1	M.2 Hybrid Key E- (WLAN x1 PCIE)		HSIO Connector
2	2	M.2 Key-B WWAN X1 PCIE		
3	3	x4 M.2 SSD(Lane reversal for x4 PCIe)		
4	4	Gbe LAN		
5	5	x1 PCIe Slot		
6	6	PCH PCIE x4 PCIe DT Slot		

[PAGE_TITLE=CLK_SRC MAPPING]

MODULE REV DETAILS		
MODULE NAME	REV	DATE

RefDes	Jumper Description	Default
J1A3	MIPI60_OVERRIDE_N	'1-X'
J2H3	MIPI60_PRESENT1_N	'1-X'
J1C1	TYPEC_DISABLE	'1-X'
J1F3	NO REBOOT STRAP	'1-X'
J1F4	FLASH DESCRIPTOR SECURITY OVERRIDE STRAP	'1-X'
J3B1	SVID DISABLE STRAP	'1-X'
J1F4	A0 PERSONALITY STRAP	'1-X'
J3H1	DDI3_HPD	'1-X'
J9J5	BT_RF_KILL_N, WIFI_RF_KILL_N	'1-X,3-X'
J9J4	CNVI Disable	'1-2'
J5U1	TOUCH PANEL POWER SUPPLY GENERATION	'1-2'
J8J3	PROCHOT_EC JPR	'1-X'
J9J3	SMC_RST_N JPR	'1-X'
J9J2	SMC_LID JPR	'1-X'
J8D2	SVID CLOCK	'1-2,3-X'
J8D3	SVID ALERT	'1-2,3-X'
J8D4	SVID DATA	'1-2,3-X'
J8G3	PCH GLITCH ISSUE MITIGATION	'1-X'
J7G1	SRTC/RTC CLEAR CMOS JPR	'1-X'
J7H2	SPD_PRSNT JPR	'1-2'
J8H3	FRU SMB_CLK_S3	'1-2'
J8H5	FRU SMB_DATA_S3	'1-2'
J6J1	PECI_MUX_CTRL_SNI_R	'1-X'
J8J1	FRU POWER SUPPLY	'1-2'
J6G4	H_PECI_CPU JPR	'1-X'

RefDes	Jumper Description	Default
SW4V1	MIPI60 FN[0:3]	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW5V1	1 - VDDQ_VR_PWRGD - IMVP_VR_EN 2 - ALL_SYS_PWRGD - IMVP_VR_EN 3 - SATAXPCIE_0_SATAGP_0_R 4 - BIOS_REC	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW6J2	1 - EC_SHD_CS_SW 2 - NC 3 - RETIMER_BYPASS_STRAP 4 - ESPI_TESTCRD_DET	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW9C1	1 - BUF_PLT_RST_1.8 - WF_CAM_RST_N 2 - WF_CAM_RST_ND - WF_CAM_RST_N 3 +V1.8A - XTAL_SEL1_J 4 +V3.3A - XTAL_IN_J	1-8(OFF); 2-7(ON); 3-6(OFF); 4-5(OFF)
SW8W1	1 - PNP_NPNP_SKU 2 - VIRTUAL_DOCK_DET_N 3 - VIRTUAL_BATTERY 4 - FLIP_TO_TABLET_MODE	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)

[PAGE_TITLE=JUMPER/SWITCH SETTINGS]

MODULE REV DETAILS		
MODULE NAME	REV	DATE

U4E1
SOC
1.6
BGA
TGL_UP3_IP_EXT

1 OF 21

Signal	Pin	Dir	Pin	Signal
DDIA_LANE3_DP	AC2	OUT	DDIA_TXP_3	
DDIA_LANE3_DN	AC1	OUT	DDIA_TXN_3	
DDIA_LANE2_DP	AD2	OUT	DDIA_TXP_2	
DDIA_LANE2_DN	AD1	OUT	DDIA_TXN_2	
DDIA_LANE1_DP	AF1	OUT	DDIA_TXP_1	
DDIA_LANE1_DN	AF2	OUT	DDIA_TXN_1	
DDIA_LANE0_DP	AG2	OUT	DDIA_TXP_0	
DDIA_LANE0_DN	AG1	OUT	DDIA_TXN_0	
DDIA_AUX_DP	AJ2	BI	DDIA_AUX_P	
DDIA_AUX_DN	AJ1	BI	DDIA_AUX_N	
GPPC_E22_DDPA_CTRLCLK	DN4	BI	GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD	
GPPC_E23_DDPA_CTRLDATA	DT6	BI	GPP_E23/DDPA_CTRLDATA	
GPPC_E14_DDSP_HPD_A	DR5	IN	GPP_E14/DDSP_HPDA/DISP_MISCA	
DDIB_LANE3_DP	T12	OUT	DDIB_TXP_3	
DDIB_LANE3_DN	T11	OUT	DDIB_TXN_3	
DDIB_LANE2_DP	Y11	OUT	DDIB_TXP_2	
DDIB_LANE2_DN	Y9	OUT	DDIB_TXN_2	
DDIB_LANE1_DP	T9	OUT	DDIB_TXP_1	
DDIB_LANE1_DN	P9	OUT	DDIB_TXN_1	
DDIB_LANE0_DP	V11	OUT	DDIB_TXP_0	
DDIB_LANE0_DN	V9	OUT	DDIB_TXN_0	
DDIB_AUX_DP	AB9	BI	DDIB_AUX_P	
DDIB_AUX_DN	AD9	BI	DDIB_AUX_N	
GPPC_H16_DDPB_CTRLCLK_PCIE_LNK_DOWN	DM29	BI	GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN	
GPPC_H17_DDPB_CTRLDATA	DK27	BI	GPP_H17/DDPB_CTRLDATA	
GPPC_A18_DDSP_HPD_B_I2S4_RXD	DG43	IN	GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD	
GPPC_A21_DDPC_CTRLCLK_I2S5_TXD	DG47	BI	GPP_A21/DDPC_CTRLCLK/I2S5_TXD	
GPPC_A22_DDPC_CTRLDATA_I2S5_RXD	DJ47	BI	GPP_A22/DDPC_CTRLDATA/I2S5_RXD	
GPPC_E18_DDP1_CTRLCLK_TBT_LSX0_TXD	DU8	BI	GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD	
GPPC_E19_DDP1_CTRLDATA_TBT_LSX0_RXD	DV8	BI	GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD	
GPPC_E20_DDP2_CTRLCLK_TBT_LSX1_TXD	DF6	BI	GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD	
GPPC_E21_DDP2_CTRLDATA_TBT_LSX1_RXD	DD6	BI	GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD	
GPPC_D9_ISH_SPI_CS_N_DDP3_CTRLCLK_GSPI2_CS0_N_TBT_LSX2_TXD	DN23	BI	GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#	
GPPC_D10_ISH_SPI_CLK_DDP3_CTRLDATA_GSPI2_CLK_TBT_LSX2_RXD	DM23	BI	GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK	
GPPC_D11_ISH_SPI_MISO_DDP4_CTRLCLK_GSPI2_MISO_TBT_LSX3_TXD	DK23	BI	GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO	
GPPC_D12_ISH_SPI_MOSI_DDP4_CTRLDATA_GSPI2_MOSI_TBT_LSX3_RXD	DN21	BI	GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI	
GPPC_A17_DISP_MISC_C_I2S4_TXD	DF43	BI	GPP_A17/DISP_MISCC/I2S4_TXD	
GPPC_A19_DDSP_HPD_1_I2S5_SCLK	DF45	IN	GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK	
GPPC_A20_DDSP_HPD_2_I2S5_SFRM	DF47	IN	GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM	
GPPC_A14_DDSP_HPD_3_I2S3_RXD_DMIC_CLK_B1	DH52	IN	GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1	
GPPC_A15_DDSP_HPD_4_I2S4_SCLK	DK45	IN	GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK	
EDP1_VDD_EN	DM8	OUT	EDP_VDDEN	
EDP1_BKLT_EN	DN8	OUT	EDP_BKLTEN	
EDP1_BKLT_CTRL	DG10	OUT	EDP_BKLTCTL	

Signal	Pin	Dir	Pin	Signal
TCP0_TXRX_P1	AY2	BI	TCP0_TXRX1_DP	
TCP0_TXRX_N1	AY1	BI	TCP0_TXRX1_DN	
TCP0_TXRX_P0	BB1	BI	TCP0_TXRX0_DP	
TCP0_TXRX_N0	BB2	BI	TCP0_TXRX0_DN	
TCP0_TX_P1	AM5	OUT	TCP0_TX1_DP	
TCP0_TX_N1	AM7	OUT	TCP0_TX1_DN	
TCP0_TX_P0	AT7	OUT	TCP0_TX0_DP	
TCP0_TX_N0	AT5	OUT	TCP0_TX0_DN	
TCP0_AUX_P	AP7	BI	TCP0_AUX_DP	
TCP0_AUX_N	AP5	BI	TCP0_AUX_DN	
TCP1_TXRX_P1	AT2	BI	TCP1_TXRX1_DP	
TCP1_TXRX_N1	AT1	BI	TCP1_TXRX1_DN	
TCP1_TXRX_P0	AU1	BI	TCP1_TXRX0_DP	
TCP1_TXRX_N0	AU2	BI	TCP1_TXRX0_DN	
TCP1_TX_P1	AD5	OUT	TCP1_TX1_DP	
TCP1_TX_N1	AD7	OUT	TCP1_TX1_DN	
TCP1_TX_P0	AH7	OUT	TCP1_TX0_DP	
TCP1_TX_N0	AH5	OUT	TCP1_TX0_DN	
TCP1_AUX_P	AF7	BI	TCP1_AUX_DP	
TCP1_AUX_N	AF5	BI	TCP1_AUX_DN	
TCP2_TXRX_P1	BF1	BI	TCP2_TXRX1_DP	
TCP2_TXRX_N1	BF2	BI	TCP2_TXRX1_DN	
TCP2_TXRX_P0	BE2	BI	TCP2_TXRX0_DP	
TCP2_TXRX_N0	BE1	BI	TCP2_TXRX0_DN	
TCP2_TX_P1	BD7	OUT	TCP2_TX1_DP	
TCP2_TX_N1	BD5	OUT	TCP2_TX1_DN	
TCP2_TX_P0	AY5	OUT	TCP2_TX0_DP	
TCP2_TX_N0	AY7	OUT	TCP2_TX0_DN	
TCP2_AUX_P	BB5	BI	TCP2_AUX_DP	
TCP2_AUX_N	BB7	BI	TCP2_AUX_DN	
TCP3_TXRX_P1	BK1	BI	TCP3_TXRX1_DP	
TCP3_TXRX_N1	BK2	BI	TCP3_TXRX1_DN	
TCP3_TXRX_P0	BJ2	BI	TCP3_TXRX0_DP	
TCP3_TXRX_N0	BJ1	BI	TCP3_TXRX0_DN	
TCP3_TX_P1	BM7	OUT	TCP3_TX1_DP	
TCP3_TX_N1	BM5	OUT	TCP3_TX1_DN	
TCP3_TX_P0	BH5	OUT	TCP3_TX0_DP	
TCP3_TX_N0	BH7	OUT	TCP3_TX0_DN	
TCP3_AUX_P	BK5	BI	TCP3_AUX_DP	
TCP3_AUX_N	BK7	BI	TCP3_AUX_DN	
TC_RCOMP_P	AN2		TCRCOMP_DP	
TC_RCOMP_N	AN1		TCRCOMP_DN	
DSI_DE_TE_2	M8	OUT	DSI_DE_TE_2	
DDI_RCOMP	AB1		DP_RCOMP	
DISP_UTILS/DSI_DE_TE_1	CE4	OUT	XXDISP_UTILS	

R4D18: 150, 1/16W1%, 0402, CHIP, A93548-005

R4D17: 150, 1%, 1/16W, CHIP, 0402, A93548-005

LPID6529

DESIGN NOTE:

LSX_A:LSX TXD, LSX_B:LSX RXD

DESIGN NOTE:

LSX_A:BSSB RXD, LSX_B:BSSB TXD

DESIGN NOTE:

GPPC_A17=VDDEN, GPPC_A21=BKLT_EN & GPPC_A22=BKLT_CTRL

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

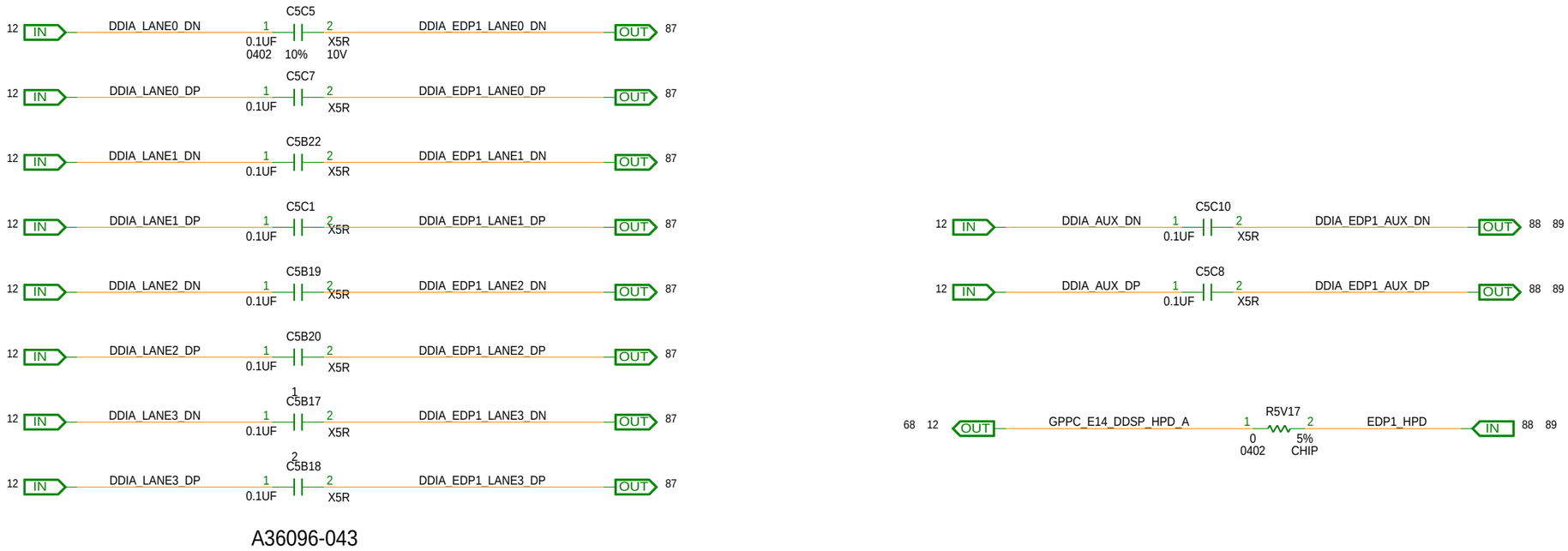
[PAGE_TITLE=TGL-U MCP (1 OF 21) - DISPLAY & TYPE-C (TBT/DISPLAY)

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.12
Wed Dec 18 18:05:26 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	12	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



A36096-043

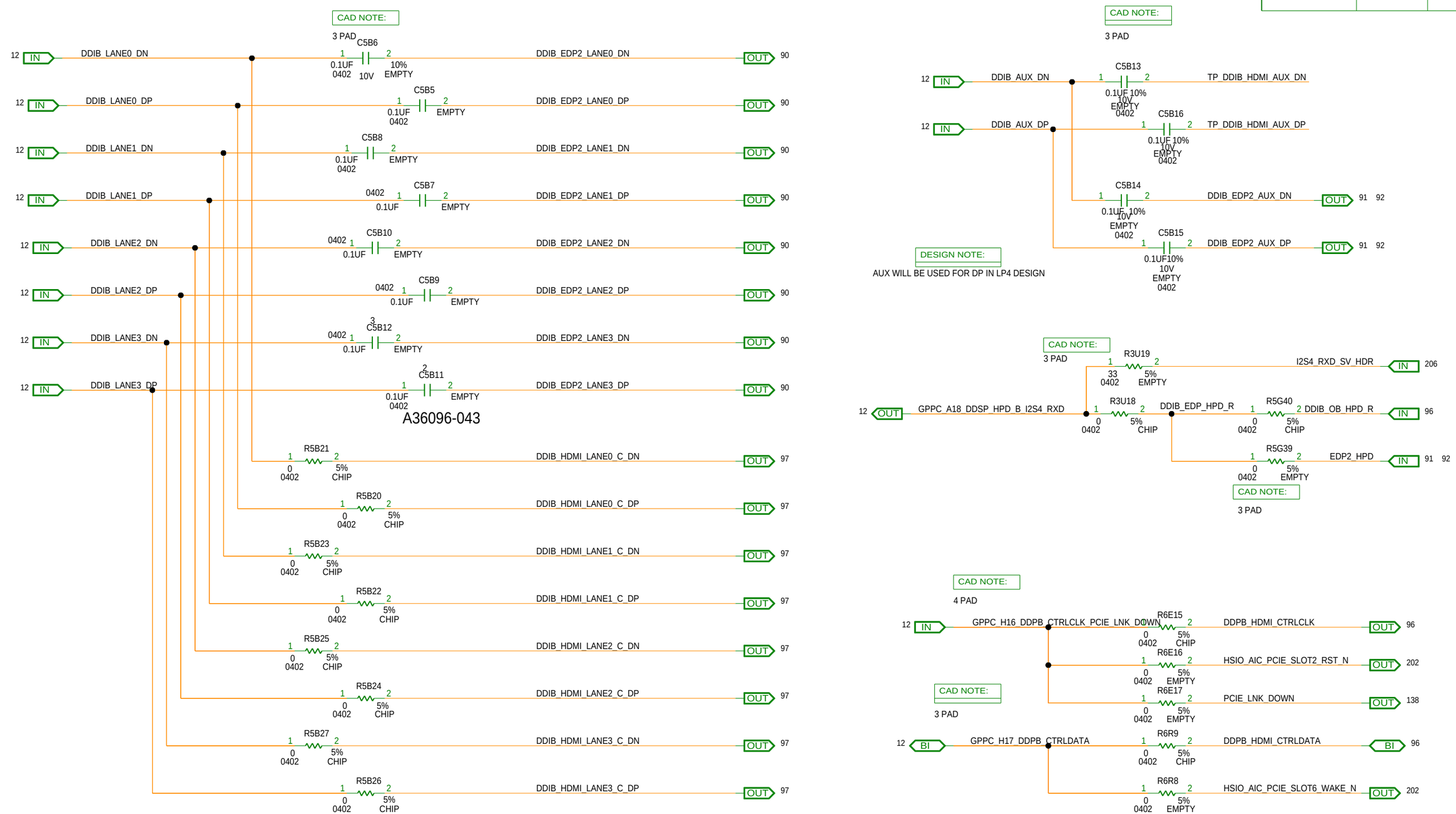
[PAGE_TITLE=DISPLAY - DDIA - PORT AC CAPS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.13
Wed Dec 18 18:05:27 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	13	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=DISPLAY - DDIB - PORT SHARING, AC CAPS]

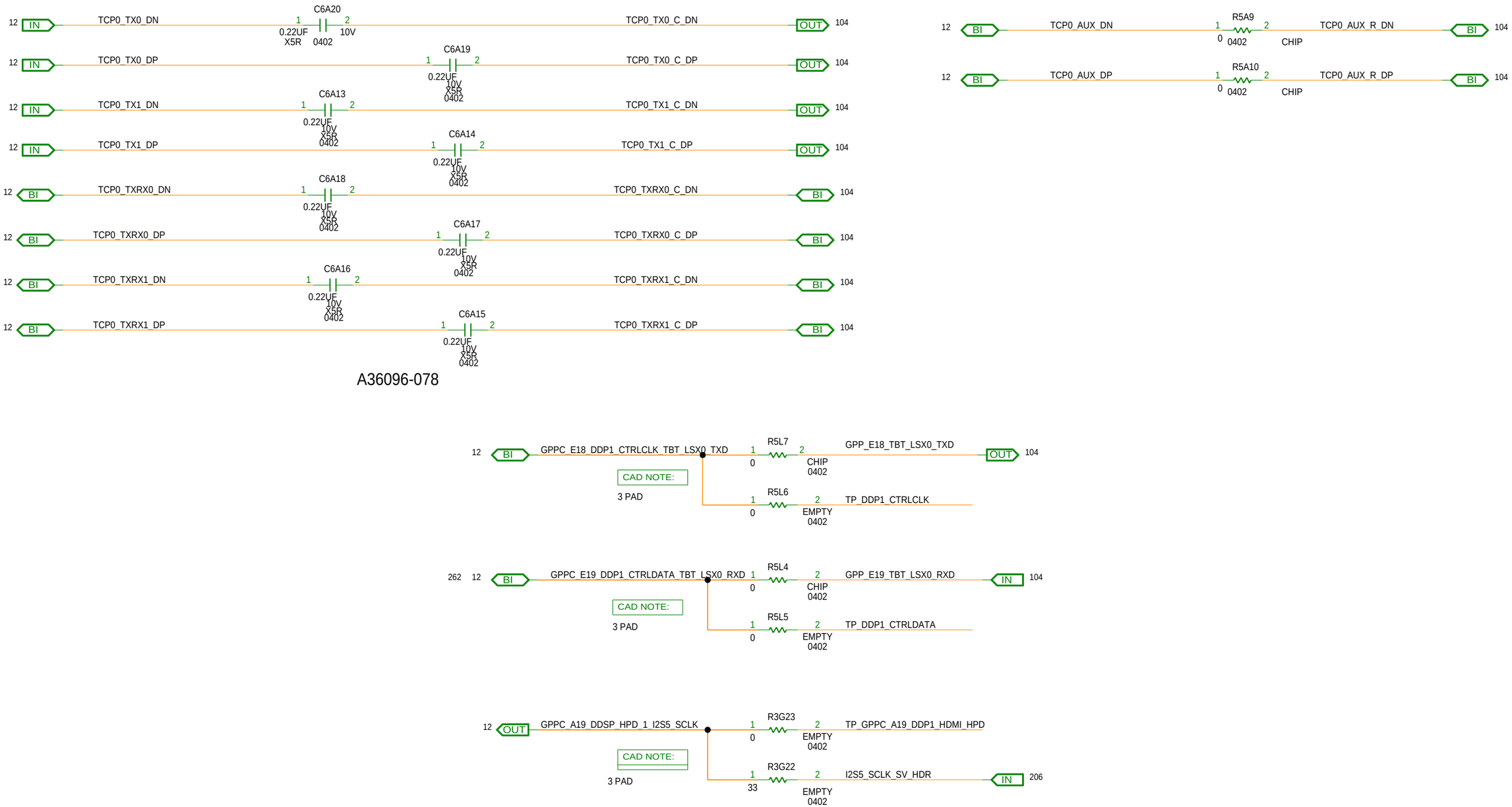
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.14
Wed Dec 18 18:05:28 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	14	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE:
PLACE CAPS CLOSE TO RETIMER

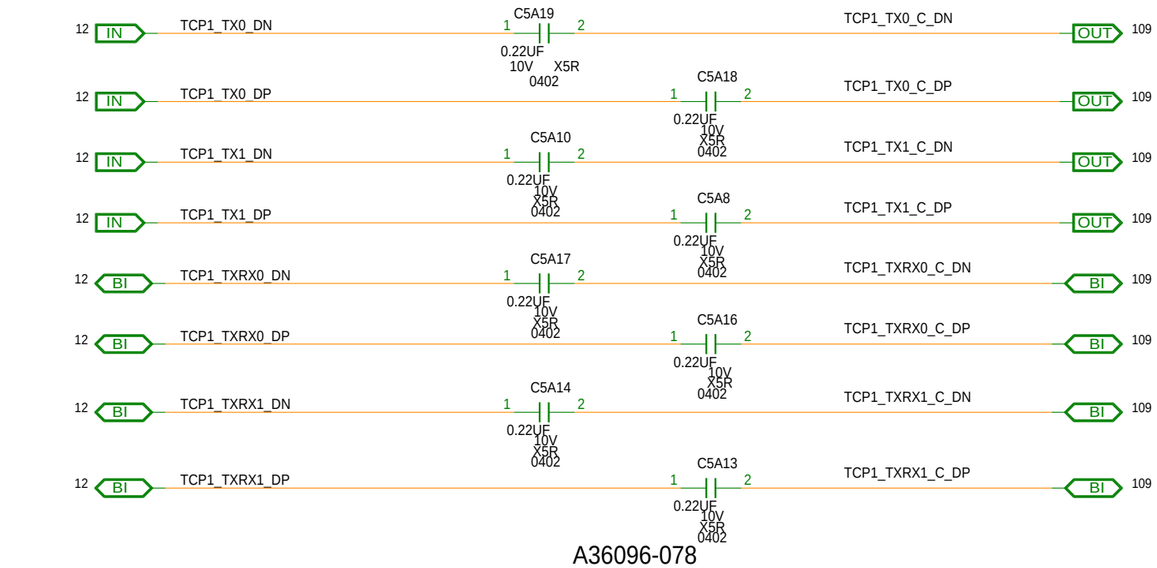


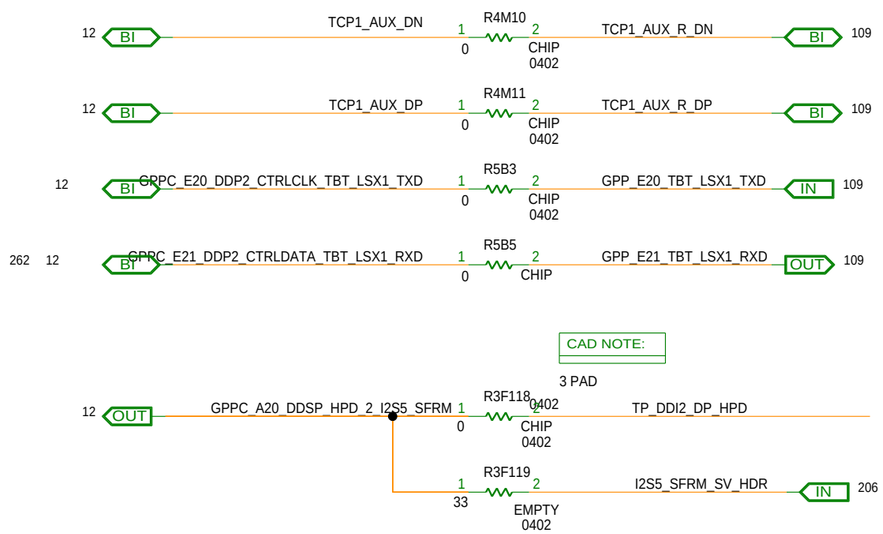
[PAGE_TITLE=DISPLAY - TYPE-C PORT 0 SHARING, AC CAPS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.15
Wed Dec 18 18:05:29 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	15	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE





[PAGE_TITLE=DISPLAY - TYPE-C PORT 1 AC CAPS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.16
Wed Dec 18 18:05:30 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	16	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE: BELOW CAPS SHOULD BE 3 PAD

Net	Dir	Page	C	Net	Dir	Page
TCP2_TX0_DN	IN	12	C9D33 0.22UF X5R 0402 10V	TCP2_TX0_C_DN	OUT	114
TCP2_TX0_DP	IN	12	C9D32 0.22UF X5R 0402 10V	TCP2_TX0_C_DP	OUT	114
TCP2_TX1_DN	IN	12	C9D26 0.22UF X5R 0402 10V	TCP2_TX1_C_DN	OUT	114
TCP2_TX1_DP	IN	12	C9D27 0.22UF X5R 0402 10V	TCP2_TX1_C_DP	OUT	114
TCP2_TXRX0_DN	BI	12	C9D31 0.22UF X5R 0402 10V	TCP2_TXRX0_C_DN	BI	114
TCP2_TXRX0_DP	BI	12	C9D30 0.22UF X5R 0402 10V	TCP2_TXRX0_C_DP	BI	114
TCP2_TXRX1_DN	BI	12	C9D28 0.22UF X5R 0402 10V	TCP2_TXRX1_C_DN	BI	114
TCP2_TXRX1_DP	BI	12	C9D29 0.22UF X5R 0402 10V	TCP2_TXRX1_C_DP	BI	114

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Net	Dir	Page	R	Net	Dir	Page
TCP2_DIRECT_TX0_R_DN	OUT	108	R9D68 0 0402 EMPTY			
TCP2_DIRECT_TX0_R_DP	OUT	108	R9D67 0 0402 EMPTY			
TCP2_DIRECT_TX1_R_DN	OUT	108	R9D58 0 0402 EMPTY			
TCP2_DIRECT_TX1_R_DP	OUT	108	R9D59 0 0402 EMPTY			
TCP2_DIRECT_TXRX0_R_DN	BI	108	R9D66 0 0402 EMPTY			
TCP2_DIRECT_TXRX0_R_DP	BI	108	R9D65 0 0402 EMPTY			
TCP2_DIRECT_TXRX1_R_DN	BI	108	R9D62 0 0402 EMPTY			
TCP2_DIRECT_TXRX1_R_DP	BI	108	R9D63 0 0402 EMPTY			

Net	Dir	Page	R	Net	Dir	Page
TCP2_AUX_DN	BI	12	R9D48 0 CHIP 0402	TCP2_AUX_R_DN	BI	114
TCP2_AUX_DP	BI	12	R9D47 0 CHIP 0402	TCP2_AUX_R_DP	BI	114
			G10604-001 C9D21 0.1UF 10V EMPTY 0402	TCP2_DIRECT_AUX_DN	BI	113
			C9D20 0.1UF 10V EMPTY 0402	TCP2_DIRECT_AUX_DP	BI	113
GPP_E22_AUX_PBIAS	BI	71	R8D27 100K A93548-128 EMPTY 0402			
GPPC_E23_DNX_IN_PROG_AUX_NBIAS	BI	71 13	R8D25 100K EMPTY 0402			

CAD NOTE: 3 PAD

FOR DIRECT PORT AUX BIASING AS SWITCH DOESN'T TAKE CARE.

Net	Dir	Page	R	Net	Dir	Page
GPPC_D9_ISH_SPI_CS_N_DDP3_CTRLCLK_GSPI2_CS0_N_TBT_LSX2_TXD	BI	12	R4G100 0 CHIP 0402	GPP_D9_TBT_LSX2_TXD	IN	114
			R4G101 0 EMPTY 0402	ISH_SPI_CS_N_SNSR_HDR	OUT	149
GPPC_D10_ISH_SPI_CLK_DDP3_CTRLDATA_GSPI2_CLK_TBT_LSX2_RXD	BI	261 12	R4F66 0 CHIP 0402	GPP_D10_TBT_LSX2_RXD	OUT	114
			RS R4F65 0 EMPTY 0402	ISH_SPI_CLK_SNSR_HDR	OUT	149

CAD NOTE: 3 PAD

CAD NOTE: PLACE THE RESISTOR RS WITH 25.4MM FROM PCH

Net	Dir	Page	R	Net	Dir	Page
GPPC_A14_DDSP_HPD_3_I2S3_RXD_DMIC_CLK_B1	OUT	72 12	R3F18 0 EMPTY 0402	DDI3_HPD	IN	210
			R3F17 33 EMPTY 0402	I2S3_RXD_DMIC_CLK_B1_SV_HDR	IN	206
			R3F19 0 CHIP 0402	GPPC_A14_ONBOARD_X4_PCIE_SLOT1_PWREN_N	IN	198
			R3T6 33 EMPTY 0402	I2S3_RXD_WWAN	IN	162

CAD NOTE: 4 PAD

[PAGE_TITLE=DISPLAY - TYPE-C PORT 2 AC CAPS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.17
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	17	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE: BELOW CAPS SHOULD BE 3 PAD

A36096-009

12	IN	TCP3_TX0_DN	C9E26	0.1UF 0402	EMPTY	DDI4_DP_TX0_C_DN	OUT 122
12	IN	TCP3_TX0_DP	C9E24	0.1UF 0402	EMPTY	DDI4_DP_TX0_C_DP	OUT 122
12	IN	TCP3_TX1_DN	C9E17	0.1UF 0402	EMPTY	DDI4_DP_TX2_C_DN	OUT 122
12	IN	TCP3_TX1_DP	C9E14	0.1UF 0402	EMPTY	DDI4_DP_TX2_C_DP	OUT 122
12	BI	TCP3_TXRX0_DN	C9E29	0.1UF 0402	EMPTY	DDI4_DP_TX1_C_DN	OUT 122
12	BI	TCP3_TXRX0_DP	C9E27	0.1UF 0402	EMPTY	DDI4_DP_TX1_C_DP	OUT 122
12	BI	TCP3_TXRX1_DN	C9E20	0.1UF 0402	EMPTY	DDI4_DP_TX3_C_DN	OUT 122
12	BI	TCP3_TXRX1_DP	C9E19	0.1UF 0402	EMPTY	DDI4_DP_TX3_C_DP	OUT 122

A36096-009

A36096-078

0402			C9E25	0.22UF 10V X5R		TCP3_TX0_C_DN	OUT 118
			C9E23	0.22UF 10V X5R 0402		TCP3_TX0_C_DP	OUT 118
			C9E16	0.22UF 10V X5R 0402		TCP3_TX1_C_DN	OUT 118
			C9E15	0.22UF 10V X5R 0402		TCP3_TX1_C_DP	OUT 118
			C9E30	0.22UF 10V X5R 0402		TCP3_TXRX0_C_DN	BI 118
			C9E28	0.22UF 10V X5R 0402		TCP3_TXRX0_C_DP	BI 118
			C9E21	0.22UF 10V X5R 0402		TCP3_TXRX1_C_DN	BI 118
			C9E18	0.22UF 10V X5R 0402		TCP3_TXRX1_C_DP	BI 118

A93549-001

12	BI	TCP3_AUX_DN	R9E26	0	CHIP 0402	TCP3_AUX_R_DN	BI 118
12	BI	TCP3_AUX_DP	R9E27	0	CHIP 0402	TCP3_AUX_R_DP	BI 118

CAD NOTE: 3 PAD

G10604-001

			C9E10	0.1UF 10V	EMPTY 0402	DDI4_DP_AUX_DN	BI 124 125
			C9E11	0.1UF 10V	EMPTY 0402 G10604-001	DDI4_DP_AUX_DP	BI 124 125

12	BI	GPPC_D11_ISH_SPI_MISO_DDP4_CTRLCLK_GSPI2_MISO_TBT_LSX3_TXD	R4G18	0	CHIP 0402	GPP_D11_TBT_LSX3_TXD	IN 118
			R4G17	0	EMPTY 0402	DDP4_DP_DNG_CTRLCLK	BI 124
			RS R4G19	0	EMPTY 0402	ISH_SPI_MISO_SNSR_HDR	IN 149

CAD NOTE: 4 PAD

CAD NOTE: PLACE THE RESISTOR RS WITH 25.4MM FROM PCH

261 12	BI	GPPC_D12_ISH_SPI_MOSI_DDP4_CTRLDATA_GSPI2_MOSI_TBT_LSX3_RXD	R4F45	0	CHIP 0402	GPP_D12_TBT_LSX3_RXD	OUT 118
			R4F47	0	EMPTY 0402	DDP4_DP_DNG_CTRLDATA	BI 124
			RS R4F46	0	EMPTY 0402	ISH_SPI_MOSI_SNSR_HDR	OUT 149

CAD NOTE: 4 PAD

CAD NOTE: PLACE THE RESISTOR RS WITH 25.4MM FROM PCH

72 12	OUT	GPPC_A15_DDSP_HPD_4_I2S4_SCLK	R3G19	0	CHIP 0402	DDI4_DP_HPD	IN 125
			R3G18	33	EMPTY 0402	I2S4_SCLK_SV_HDR	IN 206

CAD NOTE: 3 PAD

[PAGE_TITLE=DISPLAY - TYPE-C PORT3 SHARING, AC CAPS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.18
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	18	1.0

CUSTOM TEXT BPAGE

U4E1 SOC 1.6 TGL_UP3_IP_EXT

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78	BI	M_0_DQ_0<7>	CP53	DDR0_DQ0_7/DDR0_DQ0_7/DDR0_DQ0_7	DDR0_CLK_P1/DDR3_CLK_P/DDR3_CLK_P/DDR3_CLK_P	BT42	M_0_CLK_DDR1_DP
78	BI	M_0_DQ_0<6>	CP52	DDR0_DQ0_6/DDR0_DQ0_6/DDR0_DQ0_6	DDR0_CLK_N1/DDR3_CLK_N/DDR3_CLK_N/DDR3_CLK_N	BT41	M_0_CLK_DDR1_DN
78	BI	M_0_DQ_0<5>	CP50	DDR0_DQ0_5/DDR0_DQ0_5/DDR0_DQ0_5	NC/DDR2_CLK_P/DDR2_CLK_P/DDR2_CLK_P	BP52	TP_DDR_NC_2CLKP_2CLKP_2CLKP
78	BI	M_0_DQ_0<4>	CP49	DDR0_DQ0_4/DDR0_DQ0_4/DDR0_DQ0_4	NC/DDR2_CLK_N/DDR2_CLK_N/DDR2_CLK_N	BP53	TP_DDR_NC_2CLKN_2CLKN_2CLKN
78	BI	M_0_DQ_0<3>	CU53	DDR0_DQ0_3/DDR0_DQ0_3/DDR0_DQ0_3	NC/DDR1_CLK_P/DDR1_CLK_P/DDR1_CLK_P	CD42	TP_DDR_NC_1CLKP_1CLKP_1CLKP
78	BI	M_0_DQ_0<2>	CU52	DDR0_DQ0_2/DDR0_DQ0_2/DDR0_DQ0_2	NC/DDR1_CLK_N/DDR1_CLK_N/DDR1_CLK_N	CD41	TP_DDR_NC_1CLKN_1CLKN_1CLKN
78	BI	M_0_DQ_0<1>	CU50	DDR0_DQ0_1/DDR0_DQ0_1/DDR0_DQ0_1	DDR0_CLK_P0/DDR0_CLK_P/DDR0_CLK_P/DDR0_CLK_P	CC52	M_0_CLK_DDR0_DP
78	BI	M_0_DQ_0<0>	CU49	DDR0_DQ0_0/DDR0_DQ0_0/DDR0_DQ0_0	DDR0_CLK_N0/DDR0_CLK_N/DDR0_CLK_N/DDR0_CLK_N	CC53	M_0_CLK_DDR0_DN
78	BI	M_0_DQ_1<7>	CH53	DDR0_DQ1_7/DDR0_DQ1_7/DDR0_DQ1_7	DDR4/LP4/LP5/LP5 CMD Flip		
78	BI	M_0_DQ_1<6>	CH52	DDR0_DQ1_6/DDR0_DQ1_6/DDR0_DQ1_6	NC/DDR3_CKE0/DDR3_WCK_P/DDR3_WCK_P	BT45	TP_DDR_NC_3CKE0_3WCKP_3WCKP
78	BI	M_0_DQ_1<5>	CH50	DDR0_DQ1_5/DDR0_DQ1_5/DDR0_DQ1_5	NC/DDR3_CKE1/DDR3_WCK_N/DDR3_WCK_N	BT47	TP_DDR_NC_3CKE1_3WCKN_3WCKN
78	BI	M_0_DQ_1<4>	CH49	DDR0_DQ1_4/DDR0_DQ1_4/DDR0_DQ1_4	NC/DDR2_CKE0/DDR2_WCK_P/DDR2_WCK_P	BN51	TP_DDR_NC_2CKE0_2WCKP_2WCKP
78	BI	M_0_DQ_1<3>	CL53	DDR0_DQ1_3/DDR0_DQ1_3/DDR0_DQ1_3	NC/DDR2_CKE1/DDR2_WCK_N/DDR2_WCK_N	BN53	TP_DDR_NC_2CKE1_2WCKN_2WCKN
78	BI	M_0_DQ_1<2>	CL52	DDR0_DQ1_2/DDR0_DQ1_2/DDR0_DQ1_2	NC/DDR1_CKE0/DDR1_WCK_P/DDR1_WCK_P	CD45	TP_DDR_NC_1CKE0_1WCKP_1WCKP
78	BI	M_0_DQ_1<1>	CL50	DDR0_DQ1_1/DDR0_DQ1_1/DDR0_DQ1_1	NC/DDR1_CKE1/DDR1_WCK_N/DDR1_WCK_N	CD47	TP_DDR_NC_1CKE1_1WCKN_1WCKN
78	BI	M_0_DQ_1<0>	CL49	DDR0_DQ1_0/DDR0_DQ1_0/DDR0_DQ1_0	NC/DDR0_CKE0/DDR0_WCK_P/DDR0_WCK_P	CA51	TP_DDR_NC_0CKE0_0WCKP_0WCKP
78	BI	M_0_DQ_2<7>	CT47	DDR1_DQ0_7/DDR0_DQ2_7/DDR1_DQ0_7	NC/DDR0_CKE1/DDR0_WCK_N/DDR0_WCK_N	CA53	TP_DDR_NC_0CKE1_0WCKN_0WCKN
78	BI	M_0_DQ_2<6>	CV47	DDR1_DQ0_6/DDR0_DQ2_6/DDR1_DQ0_6	DDR4/LP4/LP5/LP5 CMD Flip		
78	BI	M_0_DQ_2<5>	CT45	DDR1_DQ0_5/DDR0_DQ2_5/DDR1_DQ0_5	DDR0_CKE1/DDR2_CA4/DDR2_CA5/DDR2_CA1	BU52	M_0_CKE_1
78	BI	M_0_DQ_2<4>	CV45	DDR1_DQ0_4/DDR0_DQ2_4/DDR1_DQ0_4	DDR0_CKE0/DDR2_CA5/DDR2_CA6/DDR2_CA0	BL50	M_0_CKE_0
78	BI	M_0_DQ_2<3>	CT42	DDR1_DQ0_3/DDR0_DQ2_3/DDR1_DQ0_3	DDR4/LP4/LP5/LP5 CMD Flip		
78	BI	M_0_DQ_2<2>	CV42	DDR1_DQ0_2/DDR0_DQ2_2/DDR1_DQ0_2	DDR0_CS1/DDR1_CA1/DDR1_CA1/DDR1_CA5	CF42	M_0_CS1_N
78	BI	M_0_DQ_2<1>	CT41	DDR1_DQ0_1/DDR0_DQ2_1/DDR1_DQ0_1	DDR0_CS0/NC/DDR1_CS1/DDR1_CA4	CF47	M_0_CS0_N
78	BI	M_0_DQ_2<0>	CV41	DDR1_DQ0_0/DDR0_DQ2_0/DDR1_DQ0_0	DDR4/LP4/LP5/LP5 CMD Flip		
78	BI	M_0_DQ_3<7>	CK47	DDR1_DQ1_7/DDR0_DQ3_7/DDR1_DQ1_7	NC/DDR0_CA0/DDR0_CA0/DDR0_CA6	CE53	TP_DDR_NC_0CA0_0CA0_0CA6
78	BI	M_0_DQ_3<6>	CM47	DDR1_DQ1_6/DDR0_DQ3_6/DDR1_DQ1_6	NC/DDR0_CA1/DDR0_CA1/DDR0_CA5	CE50	TP_DDR_NC_0CA1_0CA1_0CA5
78	BI	M_0_DQ_3<5>	CK45	DDR1_DQ1_5/DDR0_DQ3_5/DDR1_DQ1_5	NC/DDR2_CS0/DDR2_CA2/DDR2_CA2	BL53	TP_DDR_NC_2CS0_2CA2_2CA2
78	BI	M_0_DQ_3<4>	CM45	DDR1_DQ1_4/DDR0_DQ3_4/DDR1_DQ1_4	NC/DDR3_CA5/DDR3_CA6/DDR3_CA0	BP47	TP_DDR_NC_3CA5_3CA6_3CA0
78	BI	M_0_DQ_3<3>	CK42	DDR1_DQ1_3/DDR0_DQ3_3/DDR1_DQ1_3	NC/DDR3_CA4/DDR3_CA5/DDR3_CA1	BP42	TP_DDR_NC_3CA4_3CA5_3CA1
78	BI	M_0_DQ_3<2>	CM42	DDR1_DQ1_2/DDR0_DQ3_2/DDR1_DQ1_2	NC/DDR3_CA3/DDR3_CA4/DDR3_CS1	BP45	TP_DDR_NC_3CA3_3CA4_3CS1
78	BI	M_0_DQ_3<1>	CM41	DDR1_DQ1_1/DDR0_DQ3_1/DDR1_DQ1_1	NC/DDR3_CA2/DDR3_CA3/DDR3_CS0	BP44	TP_DDR_NC_3CA2_3CA3_3CS0
78	BI	M_0_DQ_3<0>	CK41	DDR1_DQ1_0/DDR0_DQ3_0/DDR1_DQ1_0	LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)		
78	BI	M_0_DQ_4<7>	BF53	DDR2_DQ0_7/DDR0_DQ4_7/DDR0_DQ2_7	DDR3_DQSP_1/DDR0_DQSP_7/DDR1_DQSP_3	BB44	M_0_DQS_7_DP
78	BI	M_0_DQ_4<6>	BF52	DDR2_DQ0_6/DDR0_DQ4_6/DDR0_DQ2_6	DDR3_DQSN_1/DDR0_DQSN_7/DDR1_DQSN_3	BD44	M_0_DQS_7_DN
78	BI	M_0_DQ_4<5>	BF50	DDR2_DQ0_5/DDR0_DQ4_5/DDR0_DQ2_5	DDR3_DQSP_0/DDR0_DQSP_6/DDR1_DQSP_2	BK44	M_0_DQS_6_DP
78	BI	M_0_DQ_4<4>	BF49	DDR2_DQ0_4/DDR0_DQ4_4/DDR0_DQ2_4	DDR3_DQSN_0/DDR0_DQSN_6/DDR1_DQSN_2	BH44	M_0_DQS_6_DN
78	BI	M_0_DQ_4<3>	BH53	DDR2_DQ0_3/DDR0_DQ4_3/DDR0_DQ2_3	DDR2_DQSP_1/DDR0_DQSP_5/DDR0_DQSP_3	BA51	M_0_DQS_5_DP
78	BI	M_0_DQ_4<2>	BH52	DDR2_DQ0_2/DDR0_DQ4_2/DDR0_DQ2_2	DDR2_DQSN_1/DDR0_DQSN_5/DDR0_DQSN_3	BA50	M_0_DQS_5_DN
78	BI	M_0_DQ_4<1>	BH50	DDR2_DQ0_1/DDR0_DQ4_1/DDR0_DQ2_1	DDR2_DQSP_0/DDR0_DQSP_4/DDR0_DQSP_2	BG51	M_0_DQS_4_DP
78	BI	M_0_DQ_4<0>	BH49	DDR2_DQ0_0/DDR0_DQ4_0/DDR0_DQ2_0	DDR2_DQSN_0/DDR0_DQSN_4/DDR0_DQSN_2	BG50	M_0_DQS_4_DN
78	BI	M_0_DQ_5<7>	AY53	DDR2_DQ1_7/DDR0_DQ5_7/DDR0_DQ3_7	DDR1_DQSP_1/DDR0_DQSP_3/DDR1_DQSP_1	CK44	M_0_DQS_3_DP
78	BI	M_0_DQ_5<6>	AY52	DDR2_DQ1_6/DDR0_DQ5_6/DDR0_DQ3_6	DDR1_DQSN_1/DDR0_DQSN_3/DDR1_DQSN_1	CM44	M_0_DQS_3_DN
78	BI	M_0_DQ_5<5>	AY50	DDR2_DQ1_5/DDR0_DQ5_5/DDR0_DQ3_5	DDR1_DQSP_0/DDR0_DQSP_2/DDR1_DQSP_0	CT44	M_0_DQS_2_DP
78	BI	M_0_DQ_5<4>	AY49	DDR2_DQ1_4/DDR0_DQ5_4/DDR0_DQ3_4	DDR1_DQSN_0/DDR0_DQSN_2/DDR1_DQSN_0	CV44	M_0_DQS_2_DN
78	BI	M_0_DQ_5<3>	BC53	DDR2_DQ1_3/DDR0_DQ5_3/DDR0_DQ3_3	DDR0_DQSP_1/DDR0_DQSP_1/DDR0_DQSP_1	CK51	M_0_DQS_1_DP
78	BI	M_0_DQ_5<2>	BC52	DDR2_DQ1_2/DDR0_DQ5_2/DDR0_DQ3_2	DDR0_DQSN_1/DDR0_DQSN_1/DDR0_DQSN_1	CK50	M_0_DQS_1_DN
78	BI	M_0_DQ_5<1>	BC50	DDR2_DQ1_1/DDR0_DQ5_1/DDR0_DQ3_1	DDR0_DQSP_0/DDR0_DQSP_0/DDR0_DQSP_0	CR51	M_0_DQS_0_DP
78	BI	M_0_DQ_5<0>	BC49	DDR2_DQ1_0/DDR0_DQ5_0/DDR0_DQ3_0	DDR0_DQSN_0/DDR0_DQSN_0/DDR0_DQSN_0	CR50	M_0_DQS_0_DN
78	BI	M_0_DQ_6<7>	BK47	DDR3_DQ0_7/DDR0_DQ6_7/DDR1_DQ2_7	DDR4/LP4/LP5/LP5 CMD Flip		
78	BI	M_0_DQ_6<6>	BK45	DDR3_DQ0_6/DDR0_DQ6_6/DDR1_DQ2_6	DDR0_ODT1/DDR1_CA0/DDR1_CA0/DDR1_CA6	CF44	M_0_ODT1
78	BI	M_0_DQ_6<5>	BH47	DDR3_DQ0_5/DDR0_DQ6_5/DDR1_DQ2_5	DDR0_ODT0/DDR1_CS0/DDR1_CA2/DDR1_CA2	CF45	M_0_ODT0
78	BI	M_0_DQ_6<4>	BH45	DDR3_DQ0_4/DDR0_DQ6_4/DDR1_DQ2_4	DDR4/LP4/LP5/LP5 CMD Flip		
78	BI	M_0_DQ_6<3>	BH42	DDR3_DQ0_3/DDR0_DQ6_3/DDR1_DQ2_3	DDR0_MA16/DDR1_CA4/DDR1_CA5/DDR1_CA1	CB47	M_0_MA16_RAS_N
78	BI	M_0_DQ_6<2>	BK42	DDR3_DQ0_2/DDR0_DQ6_2/DDR1_DQ2_2	DDR0_MA15/DDR1_CA3/DDR1_CA4/DDR1_CS1	CB44	M_0_MA15_CAS_N
78	BI	M_0_DQ_6<1>	BK41	DDR3_DQ0_1/DDR0_DQ6_1/DDR1_DQ2_1	DDR0_MA14/DDR1_CA2/DDR1_CA3/DDR1_CS0	CB45	M_0_MA14_WE_N
78	BI	M_0_DQ_6<0>	BH41	DDR3_DQ0_0/DDR0_DQ6_0/DDR1_DQ2_0	DDR0_MA13/DDR1_CS1/DDR1_CS0/DDR1_CA3	CF41	M_0_MA13
78	BI	M_0_DQ_7<7>	BD47	DDR3_DQ1_7/DDR0_DQ7_7/DDR1_DQ3_7	DDR0_MA12/DDR2_CA1/DDR2_CA1/DDR2_CA5	BU53	M_0_MA12
78	BI	M_0_DQ_7<6>	BB47	DDR3_DQ1_6/DDR0_DQ7_6/DDR1_DQ3_6	DDR0_MA11/NC/DDR2_CS1/DDR2_CA4	BT51	M_0_MA11
78	BI	M_0_DQ_7<5>	BD45	DDR3_DQ1_5/DDR0_DQ7_5/DDR1_DQ3_5	DDR0_MA10/DDR3_CA1/DDR3_CA1/DDR3_CA5	BV42	M_0_MA10
78	BI	M_0_DQ_7<4>	BB45	DDR3_DQ1_4/DDR0_DQ7_4/DDR1_DQ3_4	DDR0_MA9/DDR2_CA0/DDR2_CA0/DDR2_CA6	BU50	M_0_MA9
78	BI	M_0_DQ_7<3>	BB42	DDR3_DQ1_3/DDR0_DQ7_3/DDR1_DQ3_3	DDR0_MA8/DDR0_CA2/DDR0_CA3/DDR0_CS0	BY53	M_0_MA8
78	BI	M_0_DQ_7<2>	BB41	DDR3_DQ1_2/DDR0_DQ7_2/DDR1_DQ3_2	DDR0_MA7/DDR0_CA4/DDR0_CA5/DDR0_CA1	CA50	M_0_MA7
78	BI	M_0_DQ_7<1>	BD42	DDR3_DQ1_1/DDR0_DQ7_1/DDR1_DQ3_1	DDR0_MA6/DDR0_CA3/DDR0_CA4/DDR0_CS1	BY52	M_0_MA6
78	BI	M_0_DQ_7<0>	BD41	DDR3_DQ1_0/DDR0_DQ7_0/DDR1_DQ3_0	DDR0_MA5/DDR0_CA5/DDR0_CA6/DDR0_CA0	BY50	M_0_MA5
					DDR0_MA4/DDR0_CS0/DDR0_CA2/DDR0_CA2	CD51	M_0_MA4
					DDR0_MA3/DDR0_CS1/DDR0_CS0/DDR0_CA3	CD53	M_0_MA3
					DDR0_MA2/DDR3_CS0/DDR3_CA2/DDR3_CA2	BV47	M_0_MA2
					DDR0_MA1/NC/DDR0_CS1/DDR0_CA4	CE52	M_0_MA1
					DDR0_MA0/NC/DDR3_CS1/DDR3_CA4	BV41	M_0_MA0
					DDR4/LP4/LP5/LP5 CMD Flip		
					DDR0_BG1/DDR2_CA2/DDR2_CA3/DDR2_CS0	BN50	M_0_BG1
					DDR0_BG0/DDR2_CA3/DDR2_CA4/DDR2_CS1	BL52	M_0_BG0
					DDR4/LP4/LP5/LP5 CMD Flip		
					DDR0_BA1/DDR1_CA5/DDR1_CA6/DDR1_CA0	CB42	M_0_BA1
					DDR0_BA0/DDR3_CA0/DDR3_CA0/DDR3_CA6	BV44	M_0_BA0
					DDR4/LP4/LP5/LP5 CMD Flip		
					DDR0_ACT#/DDR2_CS1/DDR2_CS0/DDR2_CA3	BT53	M_0_ACT_N
					DDR4/LP4/LP5/LP5 CMD Flip		
					DDR0_PAR/DDR3_CS1/DDR3_CS0/DDR3_CA3	BV45	M_0_PARITY
					DDR0_ALERT#	AU50	M_0_ALERT_N
					DDR0_VREF_CA	AU49	+V_D4CH0_CA_VREF
					DDR_VTT_CTL	E52	DDR_VTT_CTRL
					DRAM_RESET#	DV47	DRAM_RESET_N
					DDR_RCOMP	C49	DDR_COMP_0

LPID6529

BT42	M_0_CLK_DDR1_DP	OUT 78
BT41	M_0_CLK_DDR1_DN	OUT 78
CC52	M_0_CLK_DDR0_DP	OUT 78
CC53	M_0_CLK_DDR0_DN	OUT 78
BU52	M_0_CKE_1	OUT 78
BL50	M_0_CKE_0	OUT 78
CF42	M_0_CS1_N	OUT 78
CF47	M_0_CS0_N	OUT 78
BB44	M_0_DQS_7_DP	BI 78
BD44	M_0_DQS_7_DN	BI 78
BK44	M_0_DQS_6_DP	BI 78
BH44	M_0_DQS_6_DN	BI 78
BA51	M_0_DQS_5_DP	BI 78
BA50	M_0_DQS_5_DN	BI 78
BG51	M_0_DQS_4_DP	BI 78
BG50	M_0_DQS_4_DN	BI 78
CK44	M_0_DQS_3_DP	BI 78
CM44	M_0_DQS_3_DN	BI 78
CT44	M_0_DQS_2_DP	BI 78
CV44	M_0_DQS_2_DN	BI 78
CK51	M_0_DQS_1_DP	BI 78
CK50	M_0_DQS_1_DN	BI 78
CR51	M_0_DQS_0_DP	BI 78
CR50	M_0_DQS_0_DN	BI 78
CF44	M_0_ODT1	OUT 78
CF45	M_0_ODT0	OUT 78
CB47	M_0_MA16_RAS_N	OUT 78
CB44	M_0_MA15_CAS_N	OUT 78
CB45	M_0_MA14_WE_N	OUT 78
CF41	M_0_MA13	OUT 78
BU53	M_0_MA12	OUT 78
BT51	M_0_MA11	OUT 78
BV42	M_0_MA10	OUT 78
BU50	M_0_MA9	OUT 78
BY53	M_0_MA8	OUT 78
CA50	M_0_MA7	OUT 78
BY52	M_0_MA6	OUT 78
BY50	M_0_MA5	OUT 78
CD51	M_0_MA4	OUT 78
CD53	M_0_MA3	OUT 78
BV47	M_0_MA2	OUT 78
CE52	M_0_MA1	OUT 78
BV41	M_0_MA0	OUT 78
BN50	M_0_BG1	OUT 78
BL52	M_0_BG0	OUT 78
CB42	M_0_BA1	OUT 78
BV44	M_0_BA0	OUT 78
BT53	M_0_ACT_N	OUT 78
BV45	M_0_PARITY	OUT 78
AU50	M_0_ALERT_N	IN 78
AU49	+V_D4CH0_CA_VREF	OUT 84
E52	DDR_VTT_CTRL	OUT 226
DV47	DRAM_RESET_N	
C49	DDR_COMP_0	

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

+VDD2_MEM

R1P4 470 5% 1/16W CHIP 0402 A93549-013

A93549-001 R1P5 0 5% 1/16W CHIP 0402

DRAM_RESET_N_R OUT 78 80

R3D3 100 1% 1/16W CHIP 0402 G21796-017

CAD NOTE:

USE SEPARATE VIA TO GND

CAD NOTE:

PLACE AS CLOSE AS POSSIBLE TO MCP

BPAGE DRAWING

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MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=TGL-U MCP (2 OF 21) - MEMORY CHANNEL - A]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	19	1.0

CUSTOM TEXT BPAGE

U4E1
SOC
1.6
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80	BI	M_1_DQ_0<7>	AL53	DDR4_DQ0_7/DDR1_DQ0_7/DDR0_DQ4_7
80	BI	M_1_DQ_0<6>	AL52	DDR4_DQ0_6/DDR1_DQ0_6/DDR0_DQ4_6
80	BI	M_1_DQ_0<5>	AL50	DDR4_DQ0_5/DDR1_DQ0_5/DDR0_DQ4_5
80	BI	M_1_DQ_0<4>	AL49	DDR4_DQ0_4/DDR1_DQ0_4/DDR0_DQ4_4
80	BI	M_1_DQ_0<3>	AP53	DDR4_DQ0_3/DDR1_DQ0_3/DDR0_DQ4_3
80	BI	M_1_DQ_0<2>	AP52	DDR4_DQ0_2/DDR1_DQ0_2/DDR0_DQ4_2
80	BI	M_1_DQ_0<1>	AP50	DDR4_DQ0_1/DDR1_DQ0_1/DDR0_DQ4_1
80	BI	M_1_DQ_0<0>	AP49	DDR4_DQ0_0/DDR1_DQ0_0/DDR0_DQ4_0
80	BI	M_1_DQ_1<7>	AF53	DDR4_DQ1_7/DDR1_DQ1_7/DDR0_DQ5_7
80	BI	M_1_DQ_1<6>	AF52	DDR4_DQ1_6/DDR1_DQ1_6/DDR0_DQ5_6
80	BI	M_1_DQ_1<5>	AF50	DDR4_DQ1_5/DDR1_DQ1_5/DDR0_DQ5_5
80	BI	M_1_DQ_1<4>	AF49	DDR4_DQ1_4/DDR1_DQ1_4/DDR0_DQ5_4
80	BI	M_1_DQ_1<3>	AH53	DDR4_DQ1_3/DDR1_DQ1_3/DDR0_DQ5_3
80	BI	M_1_DQ_1<2>	AH52	DDR4_DQ1_2/DDR1_DQ1_2/DDR0_DQ5_2
80	BI	M_1_DQ_1<1>	AH50	DDR4_DQ1_1/DDR1_DQ1_1/DDR0_DQ5_1
80	BI	M_1_DQ_1<0>	AH49	DDR4_DQ1_0/DDR1_DQ1_0/DDR0_DQ5_0
80	BI	M_1_DQ_2<7>	AR41	DDR5_DQ0_7/DDR1_DQ2_7/DDR1_DQ4_7
80	BI	M_1_DQ_2<6>	AV42	DDR5_DQ0_6/DDR1_DQ2_6/DDR1_DQ4_6
80	BI	M_1_DQ_2<5>	AR42	DDR5_DQ0_5/DDR1_DQ2_5/DDR1_DQ4_5
80	BI	M_1_DQ_2<4>	AV41	DDR5_DQ0_4/DDR1_DQ2_4/DDR1_DQ4_4
80	BI	M_1_DQ_2<3>	AR45	DDR5_DQ0_3/DDR1_DQ2_3/DDR1_DQ4_3
80	BI	M_1_DQ_2<2>	AV45	DDR5_DQ0_2/DDR1_DQ2_2/DDR1_DQ4_2
80	BI	M_1_DQ_2<1>	AR47	DDR5_DQ0_1/DDR1_DQ2_1/DDR1_DQ4_1
80	BI	M_1_DQ_2<0>	AV47	DDR5_DQ0_0/DDR1_DQ2_0/DDR1_DQ4_0
80	BI	M_1_DQ_3<7>	AJ41	DDR5_DQ1_7/DDR1_DQ3_7/DDR1_DQ5_7
80	BI	M_1_DQ_3<6>	AJ42	DDR5_DQ1_6/DDR1_DQ3_6/DDR1_DQ5_6
80	BI	M_1_DQ_3<5>	AL41	DDR5_DQ1_5/DDR1_DQ3_5/DDR1_DQ5_5
80	BI	M_1_DQ_3<4>	AL42	DDR5_DQ1_4/DDR1_DQ3_4/DDR1_DQ5_4
80	BI	M_1_DQ_3<3>	AJ45	DDR5_DQ1_3/DDR1_DQ3_3/DDR1_DQ5_3
80	BI	M_1_DQ_3<2>	AJ47	DDR5_DQ1_2/DDR1_DQ3_2/DDR1_DQ5_2
80	BI	M_1_DQ_3<1>	AL45	DDR5_DQ1_1/DDR1_DQ3_1/DDR1_DQ5_1
80	BI	M_1_DQ_3<0>	AL47	DDR5_DQ1_0/DDR1_DQ3_0/DDR1_DQ5_0
80	BI	M_1_DQ_4<7>	A43	DDR6_DQ0_7/DDR1_DQ4_7/DDR0_DQ6_7
80	BI	M_1_DQ_4<6>	B43	DDR6_DQ0_6/DDR1_DQ4_6/DDR0_DQ6_6
80	BI	M_1_DQ_4<5>	D43	DDR6_DQ0_5/DDR1_DQ4_5/DDR0_DQ6_5
80	BI	M_1_DQ_4<4>	E44	DDR6_DQ0_4/DDR1_DQ4_4/DDR0_DQ6_4
80	BI	M_1_DQ_4<3>	A46	DDR6_DQ0_3/DDR1_DQ4_3/DDR0_DQ6_3
80	BI	M_1_DQ_4<2>	B46	DDR6_DQ0_2/DDR1_DQ4_2/DDR0_DQ6_2
80	BI	M_1_DQ_4<1>	D46	DDR6_DQ0_1/DDR1_DQ4_1/DDR0_DQ6_1
80	BI	M_1_DQ_4<0>	E47	DDR6_DQ0_0/DDR1_DQ4_0/DDR0_DQ6_0
80	BI	M_1_DQ_5<7>	E38	DDR6_DQ1_7/DDR1_DQ5_7/DDR0_DQ7_7
80	BI	M_1_DQ_5<6>	D38	DDR6_DQ1_6/DDR1_DQ5_6/DDR0_DQ7_6
80	BI	M_1_DQ_5<5>	B38	DDR6_DQ1_5/DDR1_DQ5_5/DDR0_DQ7_5
80	BI	M_1_DQ_5<4>	A38	DDR6_DQ1_4/DDR1_DQ5_4/DDR0_DQ7_4
80	BI	M_1_DQ_5<3>	E41	DDR6_DQ1_3/DDR1_DQ5_3/DDR0_DQ7_3
80	BI	M_1_DQ_5<2>	D40	DDR6_DQ1_2/DDR1_DQ5_2/DDR0_DQ7_2
80	BI	M_1_DQ_5<1>	B40	DDR6_DQ1_1/DDR1_DQ5_1/DDR0_DQ7_1
80	BI	M_1_DQ_5<0>	A40	DDR6_DQ1_0/DDR1_DQ5_0/DDR0_DQ7_0
80	BI	M_1_DQ_6<7>	G42	DDR7_DQ0_7/DDR1_DQ6_7/DDR1_DQ6_7
80	BI	M_1_DQ_6<6>	G41	DDR7_DQ0_6/DDR1_DQ6_6/DDR1_DQ6_6
80	BI	M_1_DQ_6<5>	J41	DDR7_DQ0_5/DDR1_DQ6_5/DDR1_DQ6_5
80	BI	M_1_DQ_6<4>	J42	DDR7_DQ0_4/DDR1_DQ6_4/DDR1_DQ6_4
80	BI	M_1_DQ_6<3>	G45	DDR7_DQ0_3/DDR1_DQ6_3/DDR1_DQ6_3
80	BI	M_1_DQ_6<2>	J45	DDR7_DQ0_2/DDR1_DQ6_2/DDR1_DQ6_2
80	BI	M_1_DQ_6<1>	G47	DDR7_DQ0_1/DDR1_DQ6_1/DDR1_DQ6_1
80	BI	M_1_DQ_6<0>	J47	DDR7_DQ0_0/DDR1_DQ6_0/DDR1_DQ6_0
80	BI	M_1_DQ_7<7>	G38	DDR7_DQ1_7/DDR1_DQ7_7/DDR1_DQ7_7
80	BI	M_1_DQ_7<6>	G36	DDR7_DQ1_6/DDR1_DQ7_6/DDR1_DQ7_6
80	BI	M_1_DQ_7<5>	H36	DDR7_DQ1_5/DDR1_DQ7_5/DDR1_DQ7_5
80	BI	M_1_DQ_7<4>	H38	DDR7_DQ1_4/DDR1_DQ7_4/DDR1_DQ7_4
80	BI	M_1_DQ_7<3>	N36	DDR7_DQ1_3/DDR1_DQ7_3/DDR1_DQ7_3
80	BI	M_1_DQ_7<2>	L36	DDR7_DQ1_2/DDR1_DQ7_2/DDR1_DQ7_2
80	BI	M_1_DQ_7<1>	L38	DDR7_DQ1_1/DDR1_DQ7_1/DDR1_DQ7_1
80	BI	M_1_DQ_7<0>	N38	DDR7_DQ1_0/DDR1_DQ7_0/DDR1_DQ7_0

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

DDR4/LP4/LP5/LP5 CMD Flip

DDR1_CLK_P1/DDR7_CLK_P/DDR7_CLK_P/DDR7_CLK_P	R41	M_1_CLK_DDR1_DP	OUT 80
DDR1_CLK_N1/DDR7_CLK_N/DDR7_CLK_N/DDR7_CLK_N	R42	M_1_CLK_DDR1_DN	OUT 80
NC/DDR6_CLK_P/DDR6_CLK_P/DDR6_CLK_P	M52	TP_DDR_NC_6CLKP_6CLKP_6CLKP	
NC/DDR6_CLK_N/DDR6_CLK_N/DDR6_CLK_N	M53	TP_DDR_NC_6CLKN_6CLKN_6CLKN	
NC/DDR5_CLK_P/DDR5_CLK_P/DDR5_CLK_P	AC42	TP_DDR_NC_5CLKP_5CLKP_5CLKP	
NC/DDR5_CLK_N/DDR5_CLK_N/DDR5_CLK_N	AC41	TP_DDR_NC_5CLKN_5CLKN_5CLKN	
DDR1_CLK_P0/DDR4_CLK_P/DDR4_CLKP/DDR4_CLK_P	Y52	M_1_CLK_DDR0_DP	OUT 80
DDR1_CLK_N0/DDR4_CLK_N/DDR4_CLK_N/DDR4_CLK_N	Y53	M_1_CLK_DDR0_DN	OUT 80

DDR4/LP4/LP5/LP5 CMD Flip

NC/DDR7_CKE0/DDR7_WCK_P/DDR7_WCK_P	R47	TP_DDR_NC_7CKE0_7WCKP_7WCKP
NC/DDR7_CKE1/DDR7_WCK_N/DDR7_WCK_N	R45	TP_DDR_NC_7CKE1_7WCKN_7WCKN
NC/DDR6_CKE0/DDR6_WCK_P/DDR6_WCK_P	K51	TP_DDR_NC_6CKE0_6WCKP_6WCKP
NC/DDR6_CKE1/DDR6_WCK_N/DDR6_WCK_N	K53	TP_DDR_NC_6CKE1_6WCKN_6WCKN
NC/DDR5_CKE0/DDR5_WCK_P/DDR5_WCK_P	AC47	TP_DDR_NC_5CKE0_5WCKP_5WCKP
NC/DDR5_CKE1/DDR5_WCK_N/DDR5_WCK_N	AC45	TP_DDR_NC_5CKE1_5WCKN_5WCKN
NC/DDR4_CKE0/DDR4_WCK_P/DDR4_WCK_P	W51	TP_DDR_NC_4CKE0_4WCKP_4WCKP
NC/DDR4_CKE1/DDR4_WCK_N/DDR4_WCK_N	W53	TP_DDR_NC_4CKE1_4WCKN_4WCKN

DDR4/LP4/LP5/LP5 CMD Flip

DDR1_CKE1/DDR6_CA4/DDR6_CA5/DDR6_CA1	P52	M_1_CKE_1 OUT 80
DDR1_CKE0/DDR6_CA5/DDR6_CA6/DDR6_CA0	J50	M_1_CKE_0 OUT 80

DDR4/LP4/LP5/LP5 CMD Flip

DDR1_CS1/DDR5_CA1/DDR5_CA1/DDR5_CA5	AE42	M_1_CS1_N OUT 80
DDR1_CS0/NC/DDR5_CS1/DDR5_CA4	AE47	M_1_CS0_N OUT 80

DDR4/LP4/LP5/LP5 CMD Flip

NC/DDR7_CA5/DDR7_CA6/DDR7_CA0	N42	TP_DDR_NC_7CA5_7CA6_7CA0
NC/DDR7_CA4/DDR7_CA5/DDR7_CA1	N45	TP_DDR_NC_7CA4_7CA5_7CA1
NC/DDR7_CA3/DDR7_CA4/DDR7_CS1	N44	TP_DDR_NC_7CA3_7CA4_7CS1
NC/DDR7_CA2/DDR7_CA3/DDR7_CS0	N47	TP_DDR_NC_7CA2_7CA3_7CS0
NC/DDR6_CS0/DDR6_CA2/DDR6_CA2	J53	TP_DDR_NC_6CS0_6CA2_6CA2
NC/DDR4_CA1/DDR4_CA1/DDR4_CA5	AC50	TP_DDR_NC_4CA1_4CA1_4CA5
NC/DDR4_CA0/DDR4_CA0/DDR4_CA6	AC53	TP_DDR_NC_4CA0_4CA0_4CA6

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

DDR7_DQSP_1/DDR1_DQSP_7/DDR1_DQSP_7	K36	M_1_DQS_7_DP BI 80
DDR7_DQSN_1/DDR1_DQSN_7/DDR1_DQSN_7	K38	M_1_DQS_7_DN BI 80
DDR7_DQSP_0/DDR1_DQSP_6/DDR1_DQSP_6	G44	M_1_DQS_6_DP BI 80
DDR7_DQSN_0/DDR1_DQSN_6/DDR1_DQSN_6	J44	M_1_DQS_6_DN BI 80
DDR6_DQSP_1/DDR1_DQSP_5/DDR0_DQSP_7	D39	M_1_DQS_5_DP BI 80
DDR6_DQSN_1/DDR1_DQSN_5/DDR0_DQSN_7	C39	M_1_DQS_5_DN BI 80
DDR6_DQSP_0/DDR1_DQSP_4/DDR0_DQSP_6	C45	M_1_DQS_4_DP BI 80
DDR6_DQSN_0/DDR1_DQSN_4/DDR0_DQSN_6	D45	M_1_DQS_4_DN BI 80
DDR5_DQSP_1/DDR1_DQSP_3/DDR1_DQSP_5	AJ44	M_1_DQS_3_DP BI 80
DDR5_DQSN_1/DDR1_DQSN_3/DDR1_DQSN_5	AL44	M_1_DQS_3_DN BI 80
DDR5_DQSP_0/DDR1_DQSP_2/DDR1_DQSP_4	AV44	M_1_DQS_2_DP BI 80
DDR5_DQSN_0/DDR1_DQSN_2/DDR1_DQSN_4	AR44	M_1_DQS_2_DN BI 80
DDR4_DQSP_1/DDR1_DQSP_1/DDR0_DQSP_5	AG51	M_1_DQS_1_DP BI 80
DDR4_DQSN_1/DDR1_DQSN_1/DDR0_DQSN_5	AG50	M_1_DQS_1_DN BI 80
DDR4_DQSP_0/DDR1_DQSP_0/DDR0_DQSP_4	AN51	M_1_DQS_0_DP BI 80
DDR4_DQSN_0/DDR1_DQSN_0/DDR0_DQSN_4	AN50	M_1_DQS_0_DN BI 80

DDR4/LP4/LP5/LP5 CMD Flip

DDR1_ODT1/DDR5_CA0/DDR5_CA0/DDR5_CA6	AE44	M_1_ODT1 OUT 80
DDR1_ODT0/DDR5_CS0/DDR5_CA2/DDR5_CA2	AE45	M_1_ODT0 OUT 80

DDR4/LP4/LP5/LP5 CMD Flip

DDR1_MA16/DDR5_CA4/DDR5_CA5/DDR5_CA1	AA47	M_1_MA16_RAS_N OUT 80
DDR1_MA15/DDR5_CA3/DDR5_CA4/DDR5_CS1	AA44	M_1_MA15_CAS_N OUT 80
DDR1_MA14/DDR5_CA2/DDR5_CA3/DDR5_CS0	AA45	M_1_MA14_WE_N OUT 80
DDR1_MA13/DDR5_CS1/DDR5_CS0/DDR5_CA3	AE41	M_1_MA13 OUT 80
DDR1_MA12/DDR6_CA1/DDR6_CA1/DDR6_CA5	P53	M_1_MA12 OUT 80
DDR1_MA11/NC/DDR6_CS1/DDR6_CA4	N51	M_1_MA11 OUT 80
DDR1_MA10/DDR7_CA1/DDR7_CA1/DDR7_CA5	U42	M_1_MA10 OUT 80
DDR1_MA9/DDR6_CA0/DDR6_CA0/DDR6_CA6	P50	M_1_MA9 OUT 80
DDR1_MA8/DDR4_CA2/DDR4_CA3/DDR4_CS0	U53	M_1_MA8 OUT 80
DDR1_MA7/DDR4_CA4/DDR4_CA5/DDR4_CA1	W50	M_1_MA7 OUT 80
DDR1_MA6/DDR4_CA3/DDR4_CA4/DDR4_CS1	U52	M_1_MA6 OUT 80
DDR1_MA5/DDR4_CA5/DDR4_CA6/DDR4_CA0	U50	M_1_MA5 OUT 80
DDR1_MA4/DDR4_CS0/DDR4_CA2/DDR4_CA2	AA51	M_1_MA4 OUT 80
DDR1_MA3/DDR4_CS1/DDR4_CS0/DDR4_CA3	AA53	M_1_MA3 OUT 80
DDR1_MA2/DDR7_CS0/DDR7_CA2/DDR7_CA2	U47	M_1_MA2 OUT 80
DDR1_MA1/NC/DDR4_CS1/DDR4_CA4	AC52	M_1_MA1 OUT 80
DDR1_MA0/NC/DDR7_CS1/DDR7_CA4	U41	M_1_MA0 OUT 80

DDR4/LP4/LP5/LP5 CMD Flip

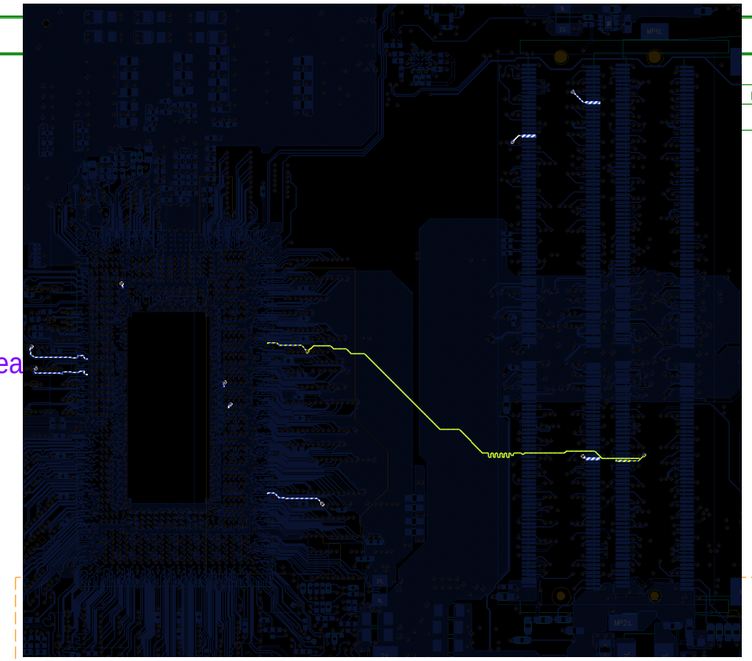
DDR1_BG1/DDR6_CA2/DDR6_CA3/DDR6_CS0	K50	M_1_BG1 OUT 80
DDR1_BG0/DDR6_CA3/DDR6_CA4/DDR6_CS1	J52	M_1_BG0 OUT 80

DDR4/LP4/LP5/LP5 CMD Flip

DDR1_BA1/DDR5_CA5/DDR5_CA6/DDR5_CA0	AA42	M_1_BA1 OUT 80
DDR1_BA0/DDR7_CA0/DDR7_CA0/DDR7_CA6	U44	M_1_BA0 OUT 80
DDR1_ACT#/DDR6_CS1/DDR6_CS0/DDR6_CA3	N53	M_1_ACT_N OUT 80
DDR1_PAR/DDR7_CS1/DDR7_CS0/DDR7_CA3	U45	M_1_PARITY OUT 80
DDR1_ALERT#	AU53	M_1_ALERT_N IN 80
DDR1_VREF_CA	AU52	+V_D4CH1_CA_VREF OUT 84

LPID6529

NOTE: Plea



1.6
TGL_UP3_IP_EXT
U4E1
SOC

4 OF 21

RSVD_2	DV24
RSVD_3	DW47
RSVD_4	DW49
RSVD_5	A48

LPID6529

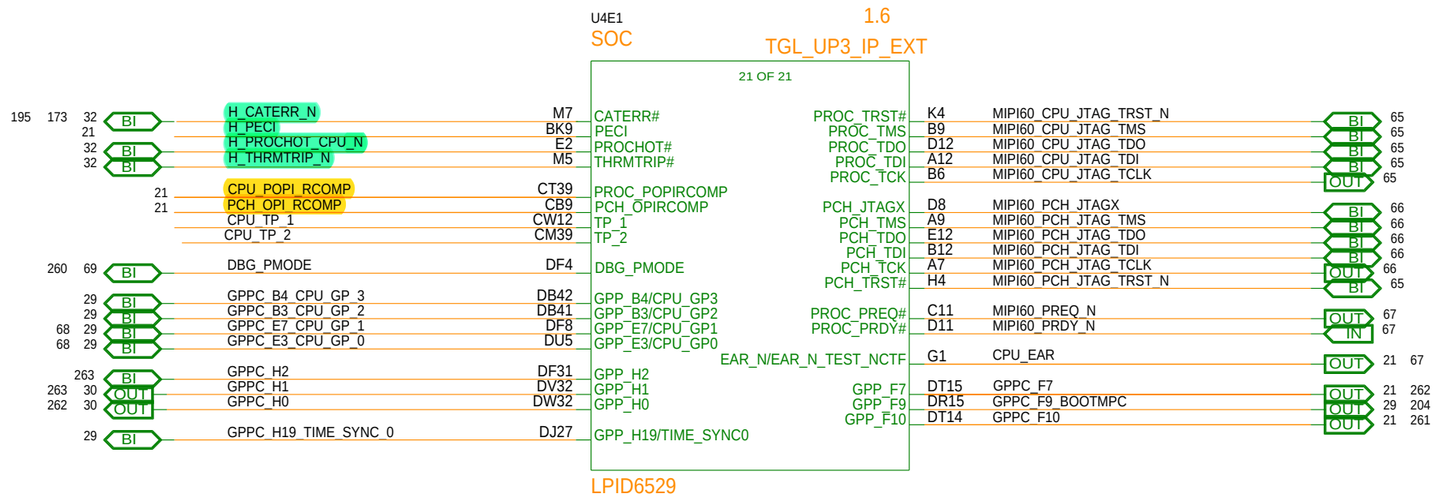
[PAGE_TITLE=TGLU MCP (3 OF 21) - MEMORY CHANNEL - B]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.20
Thu Dec 26 15:55:31 2019

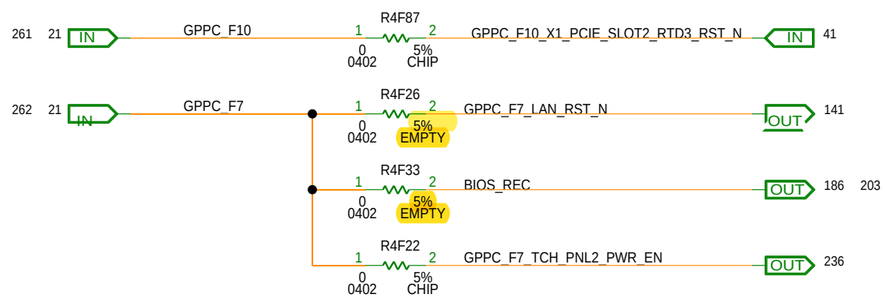
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	20	1.0

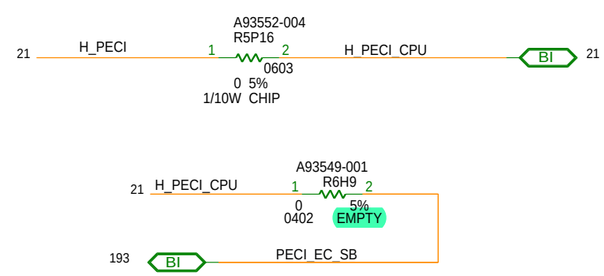
CUSTOM TEXT BPAGE

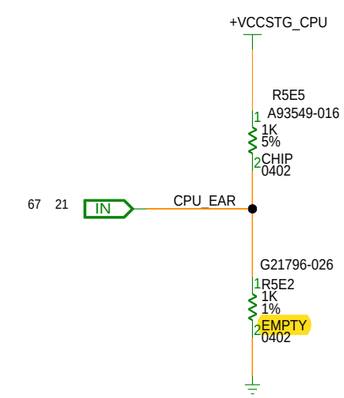
MODULE REV DETAILS		
MODULE NAME	REV	DATE

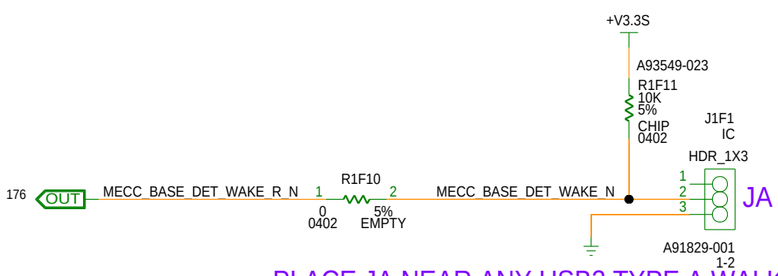


NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

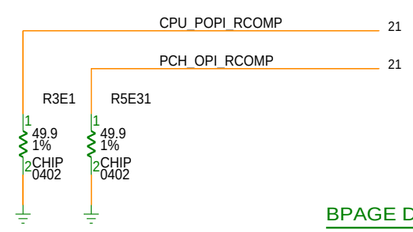








PLACE JA NEAR ANY USB2 TYPE A WALK UP PORT

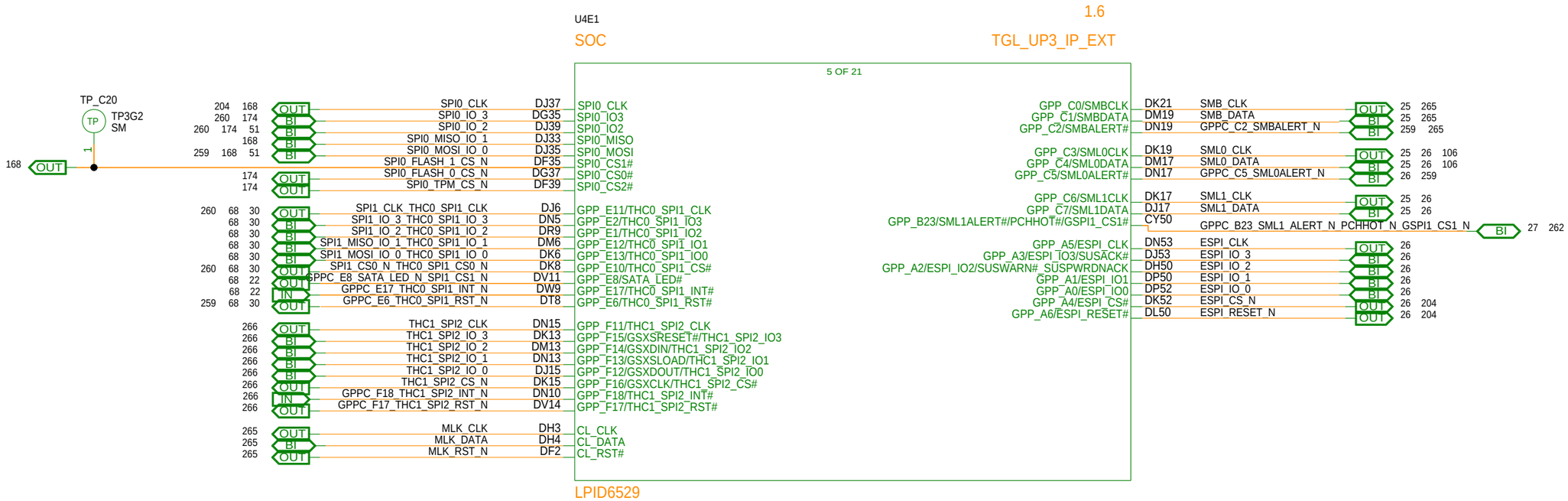


[PAGE_TITLE=TGL-U MCP (21 OF 21) - CPU MISC]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.21
Wed Dec 18 18:05:35 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	21	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE



CAD NOTE:
PLACE CLOSE TO J5U2

CAD NOTE:
3 PAD WITH R4V4

68 22 IN GPPC_E8_SATA_LED_N_SPI1_CS1_N — R4V5 (1 – 2, 0 0402, 5% CHIP) — GPPC_E8_SATA_LED_N_SPI1_CS1_R_N OUT 30

CAD NOTE:
3 PAD WITH R5V28

68 22 IN GPPC_E17_THC0_SPI1_INT_N — R5V27 (1 – 2, 0 0402, 5% CHIP) — GPPC_E17_THC0_SPI1_INT_R_N OUT 30

CAD NOTE:
FOR ALL SIGNALS IN THIS PAGE, PLEASE OPEN THE VIA MASKS NEAR TO PCH BREAKOUT FOR PROBING

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL-U MCP (5 OF 21) - LSIO - SPI, ESPI, THC, MLINK, SMLINK, SMBUS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.22
Wed Dec 18 18:05:36 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	22	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

U4E1

SOC

1.6

TGL_UP3_IP_EXT

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27	OUT	GPPC_B16_GSPI0_CLK	DC53	GPP_B16/GSPI0_CLK	GPP_D14/ISH_UART0_TXD	DR27	GPPC_D14_ISH_UART0_TXD_SML0BCLK
259 27	OUT	GPPC_B18_GSPI0_MOSI	DA51	GPP_B18/GSPI0_MOSI	GPP_D13/ISH_UART0_RXD	DW27	GPPC_D13_ISH_UART0_RXD_SML0BDATA
27	IN	GPPC_B17_GSPI0_MISO	DC49	GPP_B17/GSPI0_MISO	GPP_D16/ISH_UART0_CTS#	DV25	GPPC_D16_ISH_UART0_CTSB_SML0B_ALERT#
259 173 27	OUT	GPPC_B14_SPKR_TIME_SYNC_1_GSPI0_CS1_N	DC50	GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#	GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5	DT25	GPPC_D15_ISH_UART0_RTSB_GSPI2_CS1_N
27	OUT	GPPC_B15_GSPI0_CS0_N	DC52	GPP_B15/GSPI0_CS0#			
27	OUT	GPPC_B20_GSPI1_CLK	CY49	GPP_B20/GSPI1_CLK	GPP_B6/ISH_I2C0_SCL	DB45	GPPC_B6_ISH_I2C0_SCL
27	OUT	GPPC_B22_GSPI1_MOSI	CY53	GPP_B22/GSPI1_MOSI	GPP_B5/ISH_I2C0_SDA	DB44	GPPC_B5_ISH_I2C0_SDA
27	IN	GPPC_B21_GSPI1_MISO	CY52	GPP_B21/GSPI1_MISO	GPP_B8/ISH_I2C1_SCL	CY39	GPPC_B8_ISH_I2C1_SCL
27	OUT	GPPC_B19_GSPI1_CS0_N	DA50	GPP_B19/GSPI1_CS0#	GPP_B7/ISH_I2C1_SDA	DB47	GPPC_B7_ISH_I2C1_SDA
27	OUT	GPPC_C9_UART0_TXD	DV21	GPP_C9/UART0_TXD	GPP_B10/I2C5_SCL/ISH_I2C2_SCL	DD47	GPPC_B10_I2C5_SCL_ISH_I2C2_SCL
27	IN	GPPC_C8_UART0_RXD	DT21	GPP_C8/UART0_RXD	GPP_B9/I2C5_SDA/ISH_I2C2_SDA	DD44	GPPC_B9_I2C5_SDA_ISH_I2C2_SDA
27	IN	GPPC_C11_UART0_CTS_N	DR21	GPP_C11/UART0_CTS#	GPP_E16/ISH_GP7	DJ8	GPPC_E16_ISH_GP_7
27	OUT	GPPC_C10_UART0_RTS_N	DW21	GPP_C10/UART0_RTS#	GPP_E15/ISH_GP6	DR7	GPPC_E15_ISH_GP_6
31	OUT	GPPC_C13_UART1_TXD_ISH_UART1_TXD	DV19	GPP_C13/UART1_TXD/ISH_UART1_TXD	GPP_D18/ISH_GP5	DR24	GPPC_D18_ISH_GP_5
31	IN	GPPC_C12_UART1_RXD_ISH_UART1_RXD	DT19	GPP_C12/UART1_RXD/ISH_UART1_RXD	GPP_D17/ISH_GP4	DU25	GPPC_D17_ISH_GP_4
31	IN	GPPC_C15_UART1_CTSB_ISH_UART1_CTS_N	DR18	GPP_C15/UART1_CTS#/ISH_UART1_CTS#	GPP_D3/ISH_GP3/BK3/SBK3	DV31	GPPC_D3_ISH_GP_3
31	OUT	GPPC_C14_UART1_RTSB_ISH_UART1_RTS_N	DU19	GPP_C14/UART1_RTS#/ISH_UART1_RTS#	GPP_D2/ISH_GP2/BK2/SBK2	DU31	GPPC_D2_ISH_GP_2
190	OUT	GPPC_C21_UART2_TXD	DJ21	GPP_C21/UART2_TXD	GPP_D1/ISH_GP1/BK1/SBK1	DT27	GPPC_D1_ISH_GP_1
190	IN	GPPC_C20_UART2_RXD	DG23	GPP_C20/UART2_RXD	GPP_D0/ISH_GP0/BK0/SBK0	DV27	GPPC_D0_ISH_GP_0
190	IN	GPPC_C23_UART2_CTS_N	DJ19	GPP_C23/UART2_CTS#	GPP_RCOMP	DR51	GPPC_RCOMP
190	OUT	GPPC_C22_UART2_RTS_N	DF21	GPP_C22/UART2_RTS#	GPP_T3	DN33	GPPC_T3_I2C7_SCL_FUSA_DIAGTEST_MODE
265 28	OUT	GPPC_C17_I2C0_SCL	DV18	GPP_C17/I2C0_SCL	GPP_T2	DT35	GPPC_T2_I2C7_SDA_FUSA_DIAGTEST_EN
265 28	BI	GPPC_C16_I2C0_SDA	DW18	GPP_C16/I2C0_SDA	GPP_U5	DG17	GPPC_U5_GSPI3_CLK
28	OUT	GPPC_C19_I2C1_SCL	DJ23	GPP_C19/I2C1_SCL	GPP_U4	DG19	GPPC_U4_GSPI3_CS0B
28	BI	GPPC_C18_I2C1_SDA	DT18	GPP_C18/I2C1_SDA			
28	OUT	GPPC_H5_I2C2_SCL	DJ29	GPP_H5/I2C2_SCL			
28	BI	GPPC_H4_I2C2_SDA	DJ31	GPP_H4/I2C2_SDA			
28	OUT	GPPC_H7_I2C3_SCL	DF29	GPP_H7/I2C3_SCL			
28	BI	GPPC_H6_I2C3_SDA	DG29	GPP_H6/I2C3_SDA			
28	OUT	GPPC_H9_I2C4_SCL_CNV_MFUART2_TXD	DF25	GPP_H9/I2C4_SCL/CNV_MFUART2_TXD			
28	BI	GPPC_H8_I2C4_SDA_CNV_MFUART2_RXD	DF27	GPP_H8/I2C4_SDA/CNV_MFUART2_RXD			

LPID6529

31	OUT		
31	IN		
31	OUT		
31	OUT		
28 265	OUT		
28 265	BI		
28	OUT		
28	BI		
23 68	IN		
31 68	IN		
31	IN		
31	IN		
31	IN		
31	IN		
31	IN		
31	IN		
23			
23			

R3F16

1 — 2

200 1% 23

1/16W CHIP

0402

CAD NOTE:

FOR ALL SIGNALS IN THIS PAGE, PLEASE OPEN THE VIA MASKS NEAR TO PCH BREAKOUT FOR PROBING

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

CAD NOTE:

PLACE CLOSE TO J5U2

CAD NOTE:

3 PAD WITH R5V34

68 23 IN — GPPC_E16_ISH_GP_7 — 1 R5V33 2 — GPPC_E16_ISH_GP_7_R — OUT 31

0 5%

0402 CHIP

J1C2

HDR_1X4

23	GPPC_T3_I2C7_SCL_FUSA_DIAGTEST_MODE	1
23	GPPC_T2_I2C7_SDA_FUSA_DIAGTEST_EN	2
23	GPPC_U5_GSPI3_CLK	3
23	GPPC_U4_GSPI3_CS0B	4

H48488-001

I2C7 IS NOT AVAILABLE ON CCG PACKAGE

PLEASE DO NOT USE FOR I2C PURPOSES

HDR ONLY FOR IOTG VALIDATION

[PAGE_TITLE=TGL-U MCP (6 OF 21) - LPSS - GSPI, UART/I2C, ISH - SPI,ISH UART, ISH I2C/GPIO]

BPAGE DRAWING

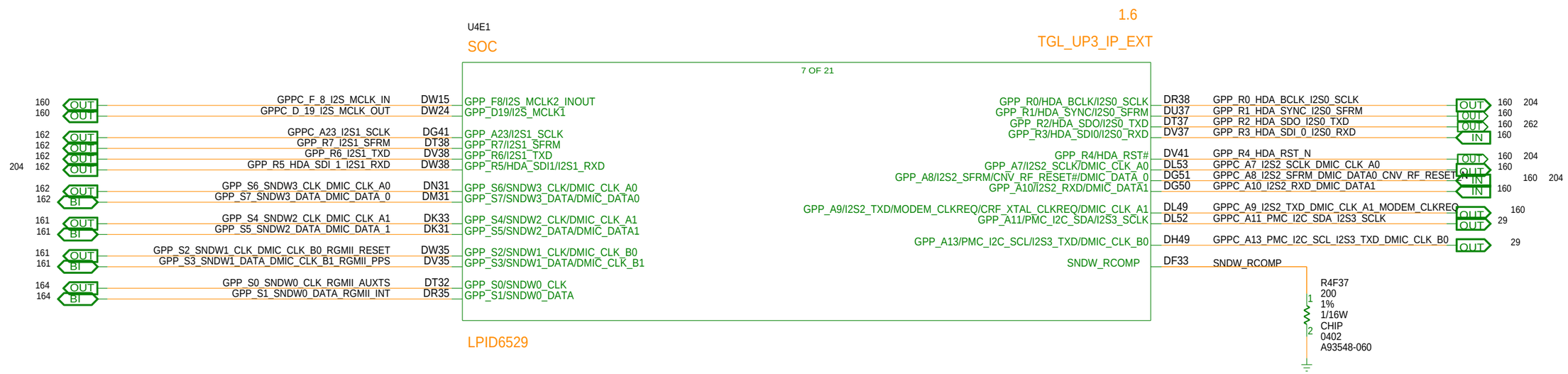
tigerlake_u_ddr4.sch_1.23

Wed Dec 18 18:05:37 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	23	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

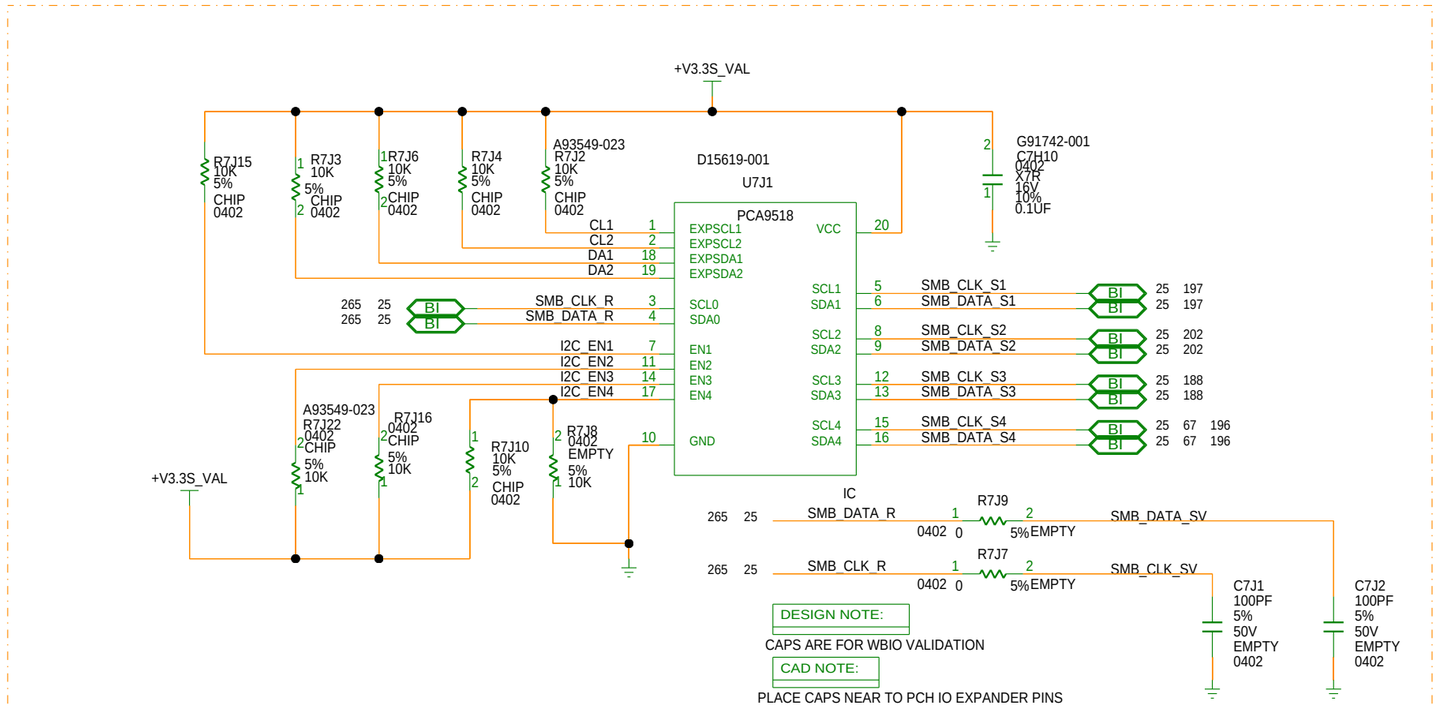
[PAGE_TITLE=TGL-U MCP (7 OF 21) - AUDIO]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.24
Wed Dec 18 18:05:38 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	24	1.0

CUSTOM TEXT BPAGE

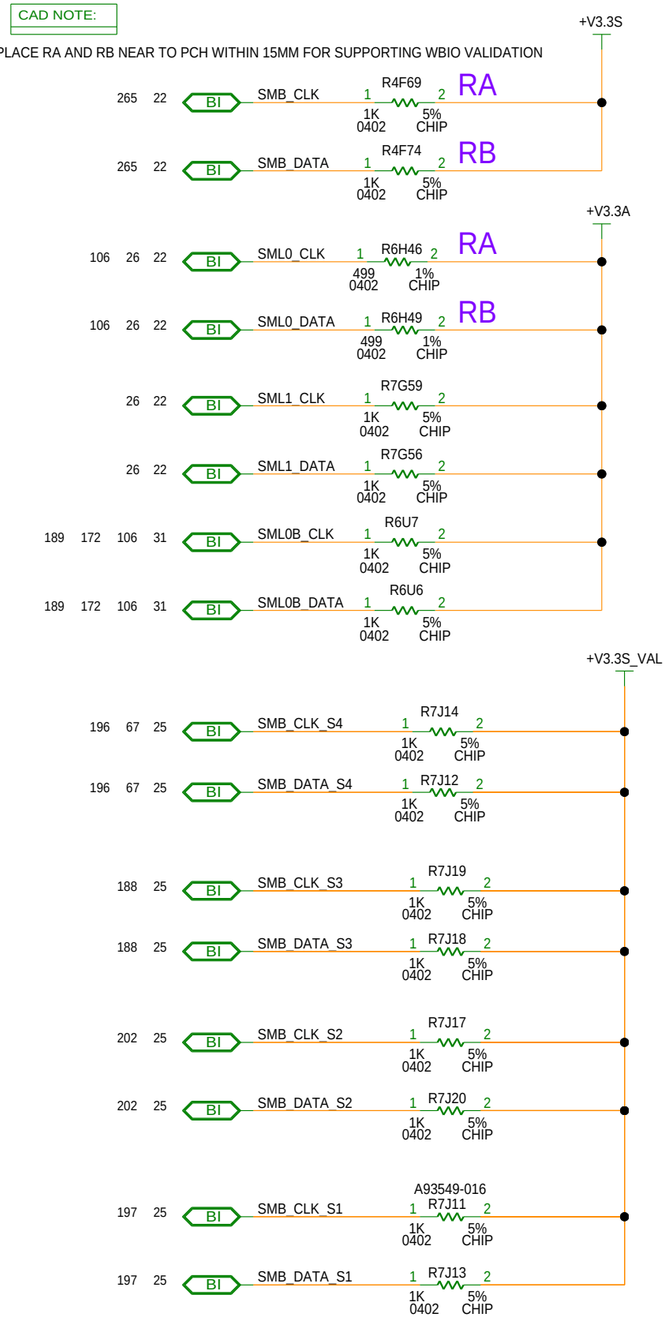
PCH SMBUS IO EXPANDER



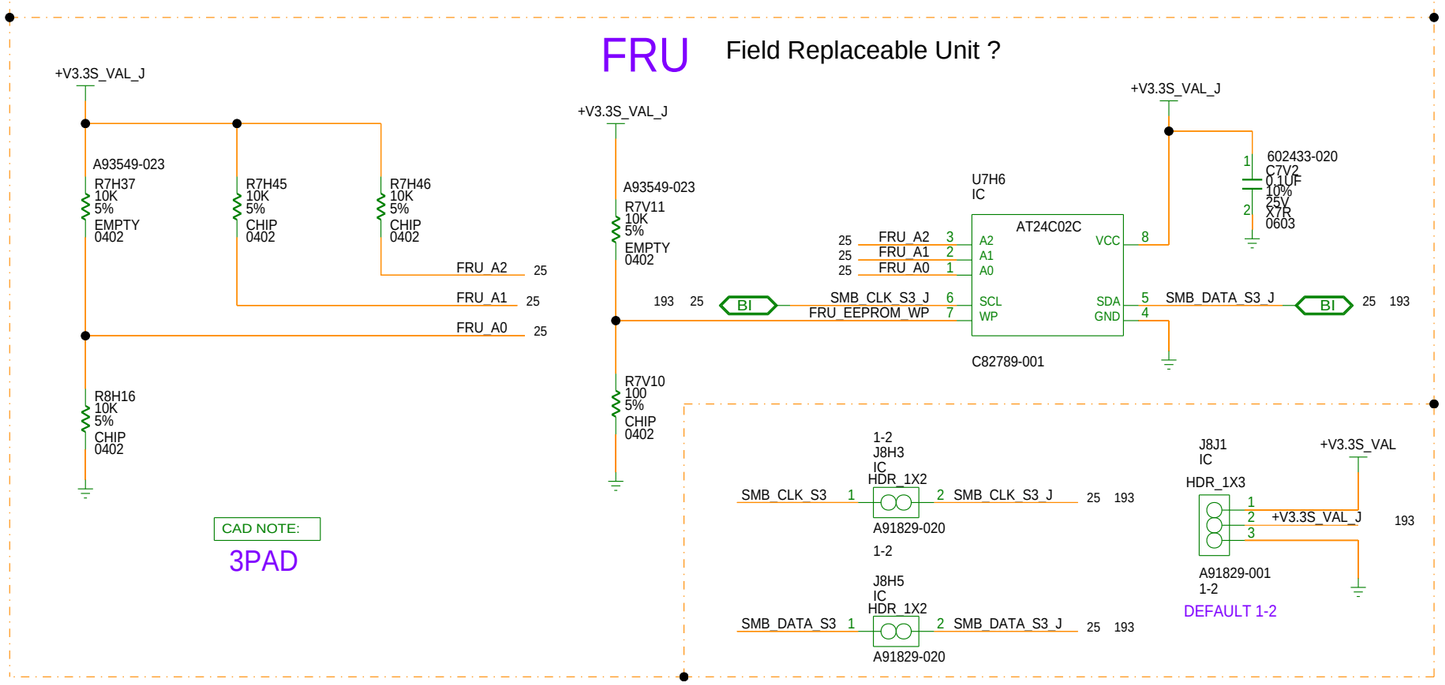
SMBUS AND SMLINK PULL UPS

CAD NOTE:

PLACE RA AND RB NEAR TO PCH WITHIN 15MM FOR SUPPORTING WBIO VALIDATION



FRU Field Replaceable Unit ?



[PAGE_TITLE=PCH SMBUS EXPANDER, FRU

MODULE REV DETAILS		
MODULE NAME	REV	DATE

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.25
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	25	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

ESPI SHARING OPTIONS - DEFAULT DUAL LOAD- EC AND ESPI HEADER

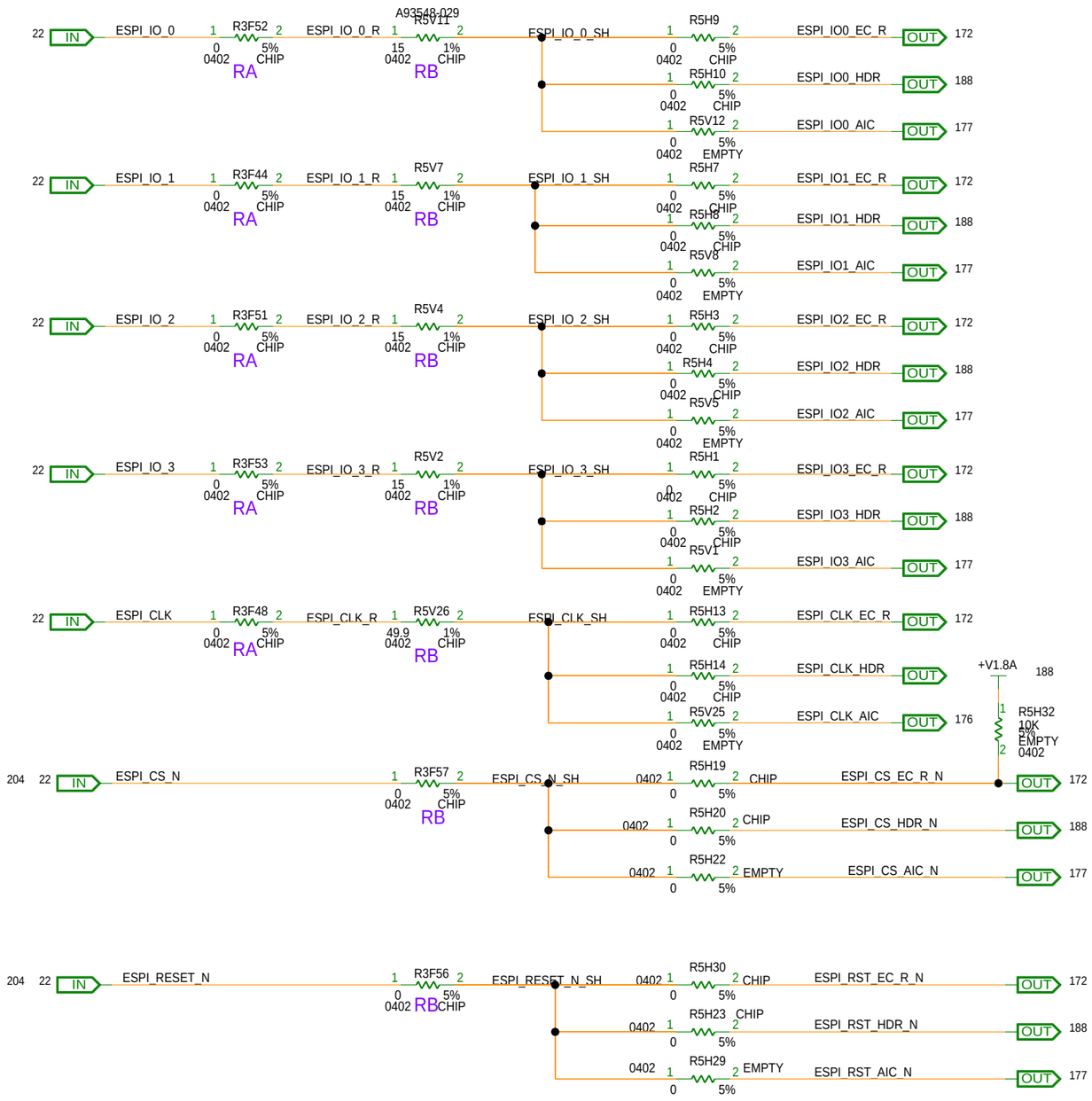
CAD NOTE:

NO PAD SHARING
PLACE ALL ESPI SERIES RESISTORS 'RA' CLOSE TO PCH - WITHIN 25.4MM
PLACE ALL RB WITHIN 112MM FROM PCH
PLACE ALL RB AND BRANCHING RESISTORS TOGETHER WITHIN 5MM
PLACE BRANCHING RESISTORS WITHIN 100MM FROM THE LOADS

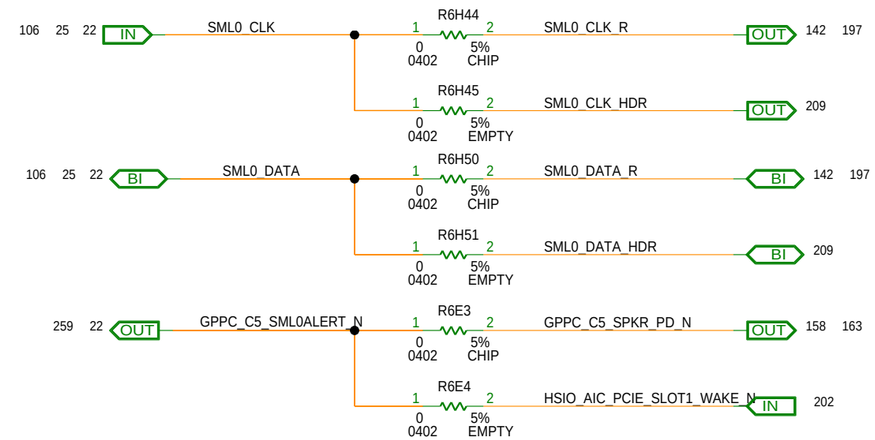
DESIGN NOTE:

SINGLE LOAD: RA= 50E ON ESPI_CLK, RA=15E ON ESPI_IO[0:3] AND RB=0E
DUAL LOAD (DEFAULT): RA=0E, RB=50E ON ESPI_CLK, RB=15E ON ESPI_IO[3:0]

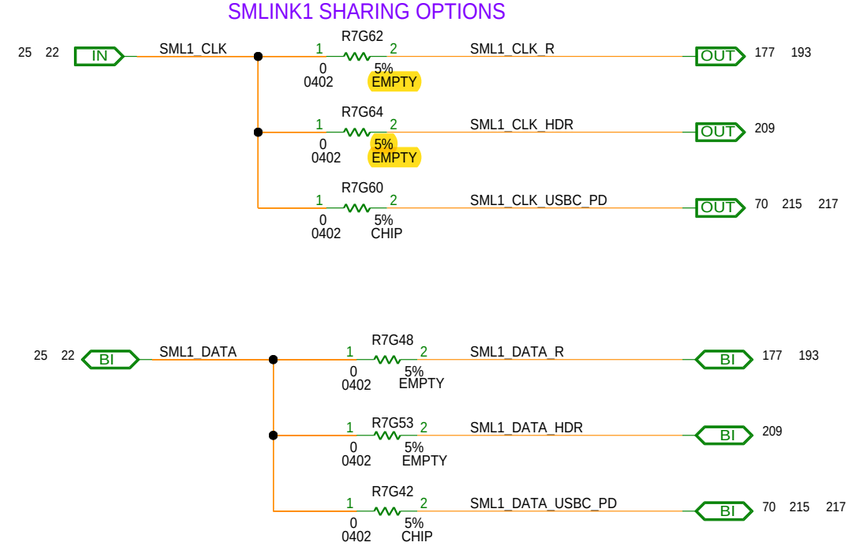
BRANCHING RESISTORS



SMLINK0 SHARING OPTIONS



SMLINK1 SHARING OPTIONS



NOTE: SMLINK0B SHARING OPTIONS IS DEFINED IN ISHUART SECTION

[PAGE_TITLE=SHARING OPTIONS - 1 - ESPI, SMLINKS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.26
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	26	1.0

CUSTOM TEXT BPAGE

GSPI0 SHARING OPTIONS

23 IN GPPC_B15_GSPI0_CS0_N — RA R3G42 0 0402 5% CHIP — GPPC_B15_WIFI_RF_KILL_N IN 144 145
CAD NOTE: 3 PAD
RB R3G43 0 0402 5% EMPTY — GSPI0_CS0_N_SV_HDR OUT 207
R3G44 0 0402 5% EMPTY — HSIO_AIC_M.2_SLOT2_PWR_EN_N OUT 202

CAD NOTE:
TRIPAD RA AND RB. RA, RB SHOULD BE PLACED WITHIN 25.4MM FROM PCH

23 OUT GPPC_B16_GSPI0_CLK — RA R3F28 0 0402 5% CHIP — GPPC_B16_M2_PCH_SSD_PWREN OUT 237
CAD NOTE: 3 PAD
RB R3F29 0 0402 5% EMPTY — GSPI0_CLK_SV_HDR OUT 207

DESIGN NOTE:
1.8V IO:RA=RB= 0E, 3.3V IO: RA=RB=15E TO BE PLACED ON GSPI[0:2]_CLK AND GSPI[0:2]_MOSI

23 OUT GPPC_B17_GSPI0_MISO — RA R3E4 0 0402 5% CHIP — GPPC_B17_WWAN_PERST_N OUT 41
CAD NOTE: 3 PAD
RB R3E5 0 0402 5% EMPTY — GSPI0_MISO_SV_HDR IN 207

259 23 OUT GPPC_B18_GSPI0_MOSI — RA R3E3 0 0402 5% CHIP — GPPC_B18_CRD_CAM_STROBE_1 OUT 132
CAD NOTE: 3 PAD
RB R3E2 0 0402 5% EMPTY — GSPI0_MOSI_SV_HDR OUT 207

259 173 23 IN GPPC_B14_SPKR_TIME_SYNC_1_GSPI0_CS1_N — R3F34 0 0402 5% CHIP — GPPC_B14_FPS_RST_N OUT 129
R3F36 0 0402 5% EMPTY — GSPI0_CS1_N_SV_HDR OUT 207
R3F35 0 0402 5% EMPTY — CRD_TIME_SYNC_1 OUT 132

GSPI1 SHARING OPTIONS

CAD NOTE: 4 PAD
DESIGN NOTE:
1.8V IO:RA=RB= 0E, 3.3V IO: RA=RB=15E TO BE PLACED ON GSPI[0:2]_CLK AND GSPI[0:2]_MOSI
OPEN: SERIES RESISTOR VALUES TO BE UPDATED BASED ON THE IO VOLTAGE

23 IN GPPC_B19_GSPI1_CS0_N — R3U10 0 0402 5% CHIP — GSPI1_CS0_FPS_R_N OUT 129
CAD NOTE: 4 PAD
R3U9 0 0402 5% EMPTY — GSPI1_CS0_N_SV_HDR OUT 207
R3U8 0 0402 5% EMPTY — MECC_SLAVE_SPI_CS_N OUT 176

CAD NOTE:
TRIPAD RA AND RB. RA, RB SHOULD BE PLACED WITHIN 25.4MM FROM PCH

23 IN GPPC_B20_GSPI1_CLK — R3F12 15 CHIP — GSPI1_CLK_FPS_R OUT 129 44
CAD NOTE: 4 PAD
R3F14 0 0402 5% EMPTY — B20_GSPI1_CLK_NFC_CLK_SV_HDR OUT 207
R3F13 0 0402 5% EMPTY — MECC_SLAVE_SPI_CLK OUT 176

23 OUT GPPC_B21_GSPI1_MISO — R3F39 0 0402 5% CHIP — GSPI1_MISO_FPS_R IN 129
CAD NOTE: 4 PAD
R3F40 0 0402 5% EMPTY — GSPI1_MISO_NFC_CLKREQ_SV_HDR IN 207
R3F41 0 0402 5% EMPTY — MECC_SLAVE_SPI_MISO IN 176

23 IN GPPC_B22_GSPI1_MOSI — R3F23 15 CHIP — GSPI1_MOSI_FPS_R OUT 129
CAD NOTE: 4 PAD
R3F24 0 0402 5% EMPTY — GSPI1_MOSI_SV_HDR OUT 207
R3F25 0 0402 5% EMPTY — MECC_SLAVE_SPI_MOSI OUT 176

262 22 OUT GPPC_B23_SML1_ALERT_N_PCHHOT_N_GSPI1_CS1_N — R3U11 0 0402 5% CHIP — GPPC_B23_CRD_CAM_PWREN IN 130
CAD NOTE: 3 PAD
R3U13 0 0402 5% EMPTY — GSPI1_CS1_N_SV_HDR OUT 207
R3U12 0 0402 5% EMPTY — GPPC_B23_USB_CAM_PWREN OUT 152 177

MODULE REV DETAILS

MODULE NAME	REV	DATE

UART0 SHARING OPTIONS

177 OUT GPPC_C8_TCH_PAD_INT_N_ECAIC — R4G1 0 0402 5% EMPTY

23 IN GPPC_C8_UART0_RXD — R4G5 0 0402 5% CHIP — GPPC_C8_TCH_PAD_INT_N IN 128
CAD NOTE: 3 PAD
R4G8 0 0402 5% EMPTY — UART0_RXD_SV_HDR IN 208

23 OUT GPPC_C9_UART0_TXD — R4G21 0 0402 5% CHIP — GPPC_C9_M.2_WWAN_WAKE_N IN 147
CAD NOTE: 3 PAD
R4G20 0 0402 5% EMPTY — UART0_TXD_SV_HDR OUT 208

23 IN GPPC_C10_UART0_RTS_N — R4G29 0 0402 5% CHIP — GPPC_C10_WWAN_RST_N OUT 147
CAD NOTE: 3 PAD
R4G28 0 0402 5% EMPTY — UART0_RTS_N_SV_HDR OUT 208

23 IN GPPC_C11_UART0_CTS_N — R4G6 0 0402 5% CHIP — GPPC_C11_WWAN_FCP_OFF_N OUT 147
CAD NOTE: 3 PAD
R4G7 0 0402 5% EMPTY — UART0_CTS_N_SV_HDR IN 208

CNVI UART0 SHARING OPTIONS

+V1.8A
R5H35 20K 5% EMPTY 0402

44 OUT GPPC_F1_CNV_BRI_RSP_UART0_RXD — RA R5H33 49.9 0402 1% CHIP — M.2_CNV_BRI_RSP_BT_UART0_RX IN 145
CAD NOTE: RB R5H34 0 0402 5% EMPTY — CNV_BRI_RSP_UART0_RXD_SV_HDR IN 208
3 PAD RA AND RB. RA TO BE PLACED 12.7MM (CAN BE EXTENDED TO 25.4MM) FROM THE CONNECTOR

IN — OUT
GPPC_F2_CNV_RGI_DT_UART0_TXD — RA R4F39 0 0402 5% CHIP — GPPC_F2_CNV_RGI_DT_R_UART0_TXD — R4H15 0 0402 5% CHIP — M.2_CNV_RGI_DT_BT_UART0_TX 145
CAD NOTE: 3 PAD
RB R4H14 0 0402 5% EMPTY — CNV_RGI_DT_UART0_TXD_SV_HDR OUT 208
RA TO BE PLACED 12.7MM (CAN BE EXTENDED TO 25.4MM) FROM THE PCH

261 44 IN GPPC_F0_CNV_BRI_DT_UART0_RTS_N — RA R4F20 0 0402 5% CHIP — M.2_CNV_BRI_DT_BT_UART0_RTS OUT 145
RB R4F21 0 0402 5% EMPTY — CNV_BRI_DT_UART0_RTS_N_SV_HDR OUT 208
CAD NOTE:
3 PAD RA AND RB. RA TO BE PLACED 12.7MM (CAN BE EXTENDED TO 25.4MM) FROM THE PCH

+V1.8A
R5H40 20K 5% EMPTY 0402

44 OUT GPPC_F3_CNV_RGI_RSP_UART0_CTS_N — RA R5H42 49.9 0402 1% CHIP — M.2_CNV_RGI_RSP_BT_UART0_CTS IN 145
CAD NOTE: RB R5H41 0 0402 5% EMPTY — CNV_RGI_RSP_UART0_CTS_N_SV_HDR IN 208
3 PAD RA AND RB. RA TO BE PLACED 12.7MM (CAN BE EXTENDED TO 25.4MM) FROM THE CONNECTOR

[PAGE_TITLE=GPIO - LPSS SHARING OPTIONS - 2 - GSPI, UART]

BPAGE DRAWING
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	27	1.0

CUSTOM TEXT BPAGE

CAD NOTE:
PLACE ALL THE RESISTORS WITHIN 25MM OF PCH

CAD NOTE:
DAISY CHAIN ROUTING FOR I2C0. PLACE ALL RESISTOR CLOSE TO TOUCH PAD CONNECTOR

LPSS I2C0 (1.8V IO)

265 23 IN GPPC_C17_I2C0_SCL
- 0402 1 R9T26 2 0 5% CHIP — I2C0_SCL_TCH_PAD OUT 128
- 0402 1 R2H18 2 0 5% CHIP — I2C0_SCL_AUDIO_CODEC OUT 158 159 163
- 0402 1 R9P35 2 0 5% EMPTY — I2C0_SCL_RT_TCP3 OUT 120 264
- 0402 1 R5G25 2 0 5% CHIP — I2C0_SCL_TCH_PNL2 OUT 127
- 0402 1 R8D26 2 0 5% EMPTY — I2C0_SCL_SV_HDR OUT 209

DESIGN NOTE:
TBT RETIMER I2C IO VOLTAGE IS 3.3V.
PLEASE MAKE SURE TO DISCONNECT OTHER
1.8V IO DEVICES WHILE CONFIGURING IO VOLTAGE AT 3.3V

265 23 BI GPPC_C16_I2C0_SDA
- 0402 1 R9U1 2 0 5% CHIP — I2C0_SDA_TCH_PAD BI 128
- 0402 1 R2H16 2 0 5% CHIP — I2C0_SDA_AUDIO_CODEC BI 158 159 163
- 0402 1 R9P39 2 0 5% EMPTY — I2C0_SDA_RT_TCP3 BI 120 264
- 0402 1 R5G30 2 0 5% CHIP — I2C0_SDA_TCH_PNL2 BI 127
- 0402 1 R8D24 2 0 5% EMPTY — I2C0_SDA_SV_HDR BI 209

LPSS I2C1(1.8V IO)

23 IN GPPC_C19_I2C1_SCL
- 0402 1 R4G37 2 0 5% CHIP — I2C1_SCL_TCH_PNL1 OUT 126
- 0402 1 R4G38 2 0 5% EMPTY — I2C1_SCL_SV_HDR OUT 209
- 0402 1 R4G117 2 0 5% EMPTY — I2C1_SCL_SV_DIPSW_HDR OUT 266

23 BI GPPC_C18_I2C1_SDA
- 0402 1 R4G35 2 0 5% CHIP — I2C1_SDA_TCH_PNL1 BI 126
- 0402 1 R4G36 2 0 5% EMPTY — I2C1_SDA_SV_HDR BI 209
- 0402 1 R4G116 2 0 5% EMPTY — I2C1_SDA_SV_DIPSW_HDR OUT 266

LPSS I2C2 (1.8V IO)

23 IN GPPC_H5_I2C2_SCL
- 0402 1 R4G89 2 0 5% CHIP — I2C2_SCL_CSI OUT 131
- 0402 1 R4G88 2 0 5% EMPTY — I2C2_SCL_TCH_PNL2 OUT 127
- 0402 1 R4G87 2 0 5% EMPTY — I2C2_SCL_SV_HDR OUT 209

23 BI GPPC_H4_I2C2_SDA
- 0402 1 R4G59 2 0 5% CHIP — I2C2_SDA_CSI BI 131
- 0402 1 R4G46 2 0 5% EMPTY — I2C2_SDA_TCH_PNL2 BI 127
- 0402 1 R4G58 2 0 5% EMPTY — I2C2_SDA_SV_HDR BI 209

LPSS I2C3 (1.8V IO)

23 IN GPPC_H7_I2C3_SCL
- 0402 1 R3U16 2 0 5% CHIP — I2C3_SCL_CSI OUT 130
- 0402 1 R3U17 2 0 5% EMPTY — I2C3_SCL_SV_HDR OUT 209

23 BI GPPC_H6_I2C3_SDA
- 0402 1 R3U21 2 0 5% CHIP — I2C3_SDA_CSI BI 130
- 0402 1 R3U20 2 0 5% EMPTY — I2C3_SDA_SV_HDR BI 209

LPSS I2C4 (USED AS CNVI MFUART)

CAD NOTE:
PLACE ALL THE RESISTORS WITHIN 25MM OF PCH

23 IN GPPC_H9_I2C4_SCL_CNV_MFUART2_TXD
- 0402 1 R3G47 2 0 5% CHIP — CNV_MFUART2_TXD OUT 146
- 0402 1 R3G48 2 0 5% EMPTY — I2C4_SCL_SV_HDR OUT 209

CAD NOTE:
3 PAD

23 OUT GPPC_H8_I2C4_SDA_CNV_MFUART2_RXD
- 0402 1 R3G50 2 0 5% CHIP — CNV_MFUART2_RXD IN 146
- 0402 1 R3G49 2 0 5% EMPTY — I2C4_SDA_SV_HDR BI 209

CAD NOTE:
3 PAD

LPSS I2C5/ ISH I2C2 (1.8V IO, USED AS LPSS I2C5)

23 IN GPPC_B10_I2C5_SCL_ISH_I2C2_SCL
- 0402 1 R3F105 2 0 5% CHIP — I2C5_SCL_CSI OUT 130
- 0402 1 R3F103 2 0 5% CHIP — I2C5_SCL_PSS OUT 196 264
- 0402 1 R3F104 2 0 5% CHIP — I2C5_SCL_PWRMTR OUT 212
- 0402 1 R3F102 2 0 5% EMPTY — ISH_I2C2_SCL_SNSR_HDR OUT 149

23 BI GPPC_B9_I2C5_SDA_ISH_I2C2_SDA
- 0402 1 R3F83 2 0 5% CHIP — I2C5_SDA_CSI BI 130
- 0402 1 R3F84 2 0 5% CHIP — I2C5_SDA_PSS BI 196 264
- 0402 1 R3F85 2 0 5% CHIP — I2C5_SDA_PWRMTR BI 212
- 0402 1 R3F86 2 0 5% EMPTY — ISH_I2C2_SDA_SNSR_HDR BI 149

ISH I2C0 (1.8V/3.3V IO)

265 23 IN GPPC_B6_ISH_I2C0_SCL
- 0402 1 R3F10 2 0 5% CHIP — ISH_I2C0_SCL_SNSR_HDR OUT 149
- 0402 1 R3F9 2 0 5% EMPTY — ISH_EEPROM_CLK OUT 149
- 0402 1 R3F8 2 0 5% EMPTY — ISH_I2C0_SCL_TTK OUT 264
- 0402 1 R3F128 2 0 5% EMPTY — ISH_I2C0_SCL_SV_DIPSW_HDR OUT 266

CAD NOTE:
PLACE ALL THE RESISTORS WITHIN 25MM OF PCH

265 23 BI GPPC_B5_ISH_I2C0_SDA
- 0402 1 R3F3 2 0 5% CHIP — ISH_I2C0_SDA_SNSR_HDR BI 149
- 0402 1 R3F2 2 0 5% EMPTY — ISH_EEPROM_DATA BI 149
- 0402 1 R3F1 2 0 5% EMPTY — ISH_I2C0_SDA_TTK BI 264
- 0402 1 R3F129 2 0 5% EMPTY — ISH_I2C0_SDA_SV_DIPSW_HDR OUT 266

ISH I2C1 (1.8V/3.3V IO)

23 IN GPPC_B8_ISH_I2C1_SCL
- 0402 1 R3F77 2 0 5% CHIP — ISH_I2C1_SCL_SNSR_HDR OUT 149

210 191 177 172 228 224 219 212 BI SMB_BS_CLK
- 0402 1 R3F89 2 0 5% EMPTY

CAD NOTE:
3 PAD

23 BI GPPC_B7_ISH_I2C1_SDA
- 0402 1 R3F78 2 0 5% CHIP — ISH_I2C1_SDA_SNSR_HDR BI 149

210 191 177 172 228 224 219 212 BI SMB_BS_DATA
- 0402 1 R3F90 2 0 5% EMPTY

CAD NOTE:
3 PAD

MODULE REV DETAILS

MODULE NAME	REV	DATE

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.28
Wed Dec 18 18:05:42 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	28	1.0

CUSTOM TEXT BPAGE

[PAGE_TITLE=GPIO - LPSS SHARING OPTIONS - 3 - I2C, ISH I2C]

MODULE REV DETAILS		
MODULE NAME	REV	DATE

34 IN GPPC_H12_M2_SKT2_CFG_0 — R4U7 (0 0402 5% CHIP) — GPPC_H12_CAM2_RST_N OUT 130

34 OUT GPPC_H13_M2_SKT2_CFG_1 — R4G22 (0 0402 5% CHIP) — GPPC_H13_CAM3_RST_N IN 131

34 IN GPPC_H14_M2_SKT2_CFG_2 — R4U42 (0 0402 5% CHIP) — GPPC_H14_TCH_PNL_PWR_EN OUT 236

34 OUT GPPC_H15_M2_SKT2_CFG_3 — R6E31 (0 0402 5% CHIP) — GPPC_H15_CAM3_PWREN OUT 131
- R6E30 (0 0402 5% EMPTY) — HSIO_AIC_PCIE_SLOT2_PWR_EN_N OUT 202

68 34 IN GPPC_E4_SATA_DEVSLP_0 — R4V7 (0 0402 5% CHIP) — SATA_DIRECT_DEVSLP OUT 138 139
- R4V8 (0 0402 5% EMPTY) — HSIO_AIC_PCIE_SLOT2_WAKE_N OUT 202

CAD NOTE: 3 PAD

68 34 IN GPPC_E5_SATA_DEVSLP_1 — R5V23 (0 0402 5% CHIP) — M2_SSD_DEVSLP OUT 138 140

24 IN GPPC_A11_PMC_I2C_SDA_I2S3_SCLK — R3F31 (33 0402 5% EMPTY) — I2S3_SCLK_WWAN OUT 162
- R3F33 (0 0402 5% CHIP) — GPPC_A11_M2_CPU_SSD_RST_N OUT 41
- R3F32 (33 0402 5% EMPTY) — I2S3_SCLK_SV_HDR OUT 206

CAD NOTE: 4 PAD

260 68 34 OUT GPPC_E9_USB2_OCB_0 — R5V22 (0 0402 5% CHIP) — TCPC01_TYPEA12_OC0_N IN 70 152 215

34 OUT GPPC_A16_USB2_OCB_3_I2S4_SFRM — R3G27 (0 0402 5% CHIP) — TCPC23_TYPEA34_OC3_N IN 154 217
- R3G28 (33 0402 5% EMPTY) — I2S4_SFRM_SV_HDR OUT 206

CAD NOTE: 3 PAD

34 IN GPPC_E0_SATAXPCIE_0_SATAGP_0_R — R5V58 (0 0402 5% EMPTY) — HSIO_AIC_PCIE_SLOT1_PWR_EN_N OUT 202
- R5V59 (0 0402 5% EMPTY) — SATAXPCIE_0_SATAGP_0 OUT 139
- R5V57 (0 0402 5% CHIP) — GPPC_E0_ME_PWR_GATE_LED OUT 138

34 OUT GPPC_A12_SATAXPCIE_1_SATAGP_1_I2S3_SFRM — R3F99 (33 0402 5% EMPTY) — M.2_WWAN_I2S3_LRCLK OUT 147
- R3F101 (0 0402 5% CHIP) — M.2_SSD_PEDET_R IN 140
- R3F100 (33 0402 5% EMPTY) — I2S3_SFRM_SV_HDR OUT 206

CAD NOTE: 4 PAD

68 21 OUT GPPC_E3_CPU_GP_0 — R4V25 (0 0402 5% CHIP) — GPPC_E3_FPS_INT IN 129

68 21 IN GPPC_E7_CPU_GP_1 — R5V19 (0 0402 5% CHIP) — GPPC_E7_EC_SMI_N OUT 51 171 177 188 250

21 OUT GPPC_B3_CPU_GP_2 — R5G16 (0 0402 5% CHIP) — TP_GPPC_B3_ONBOARD_X4_PCIE_SLOT1_WAKE_N

21 IN GPPC_B4_CPU_GP_3 — R3F106 (0 0402 5% CHIP) — GPPC_B4_SATA_DIRECT_PWREN OUT 237

TPS16 TP5H4 SM (TP)

21 OUT GPPC_H19_TIME_SYNC_0 — R4G106 (0 0402 5% CHIP) — GPPC_H19_UART_BT_WAKE_N IN 145
- R4G96 (0 0402 5% EMPTY) — HSIO_AIC_PCIE_SLOT5_WAKE_N IN 202
- R4G103 (0 0402 5% EMPTY) — CRD_TIME_SYNC_0 OUT 132
- R4G110 (0 0402 5% EMPTY) — SIDEBAND_TIME_SYNC_0 OUT 193

204 21 IN GPPC_F9_BOOTMPC — R6E23 (0 0402 5% CHIP) — GPPC_F9_X1_PCIE_SLOT2_PWR_EN IN 252 255
- R6E24 (0 0402 5% EMPTY) — HSIO_AIC_PCIE_SLOT4_PWR_EN_N OUT 202

261 49 IN GPD_7 — R3T10 (0 0402 5% CHIP) — GPD_7_TCP_RETIMER_PERST_N OUT 111

24 IN GPPC_A13_PMC_I2C_SCL_I2S3_TXD_DMIC_CLK_B0 — R3F116 (33 0402 5% EMPTY) — M.2_WWAN_I2S3_OUT OUT 147
- R3F115 (0 0402 5% CHIP) — GPPC_A13_BT_RF_KILL_N OUT 144 145
- R3F117 (33 0402 5% EMPTY) — I2S3_TXD_DMIC_CLK_B0_SV_HDR OUT 206
- R3F123 (0 0402 5% EMPTY) — HSIO_AIC_M.2_SLOT1_WAKE_N OUT 202

CAD NOTE: 4 PAD

[PAGE_TITLE=GPIO - LPSS SHARING OPTIONS - 4 - I2C]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.29
Wed Dec 18 18:05:44 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	29	1.0

CUSTOM TEXT BPAGE

THC0 SPI SHARING OPTIONS

CAD NOTE: RA, RB SHOULD BE PLACED WITHIN 150 MM FROM PCH AND 50MM FROM THE TOUCH CONNECTOR/ SV HEADERS

260 68 22 BI SPI1_CLK_THC0_SPI1_CLK
- RA: R4U33 (0 0402 5% CHIP) → THC0_SPI1_CLK_TCH_PNL1 → OUT 126
- RB: R4U34 (33 0402 5% EMPTY) → SPI1_CLK_THC0_SPI1_CLK_SV_HDR → BI 267

CAD NOTE: 3 PAD RA, RB

68 22 BI SPI1_IO_3_THC0_SPI1_IO_3
- RA: R4G112 (0 0402 5% CHIP) → THC0_SPI1_IO_3_TCH_PNL1 → OUT 126
- RB: R4G113 (33 0402 5% EMPTY) → SPI1_IO_3_THC0_SPI1_IO_3_SV_HDR → BI 267

CAD NOTE: 3 PAD RA, RB

68 22 BI SPI1_IO_2_THC0_SPI1_IO_2
- RA: R4U39 (0 0402 5% CHIP) → THC0_SPI1_IO_2_TCH_PNL1 → BI 126
- RB: R4U38 (33 0402 5% EMPTY) → SPI1_IO_2_THC0_SPI1_IO_2_SV_HDR → BI 267

CAD NOTE: 3 PAD RA, RB

68 22 BI SPI1_MISO_IO_1_THC0_SPI1_IO_1
- RA: A93549-001 R5U29 (0 0402 5% CHIP) → THC0_SPI1_IO_1_TCH_PNL1 → OUT 126
- RB: R5U30 (33 0402 5% EMPTY) → SPI1_MISO_IO_1_THC0_SPI1_IO_1_SV_HDR → BI 267

CAD NOTE: 3 PAD RA, RB

68 22 BI SPI1_MOSI_IO_0_THC0_SPI1_IO_0
- RA: A93549-001 R5U23 (0 0402 5% CHIP) → THC0_SPI1_IO_0_TCH_PNL1 → OUT 126
- RB: R5U22 (33 0402 5% EMPTY) → SPI1_MOSI_IO_0_THC0_SPI1_IO_0_SV_HDR → BI 267

CAD NOTE: 3 PAD RA, RB

260 68 22 BI SPI1_CS0_N_THC0_SPI1_CS0_N
- RA: R4U28 (0 0402 5% CHIP) → THC0_SPI1_CS0_N_TCH_PNL1 → BI 126
- RB: R4U29 (0 0402 5% EMPTY) → SPI1_CS0_N_THC0_SPI1_CS0_N_SV_HDR → BI 267

CAD NOTE: 3 PAD RA, RB

22 IN GPPC_E8_SATA_LED_N_SPI1_CS1_R_N
- RA: R5T15 (0 0402 5% CHIP) → GPPC_E8_EC_SLP_S0_CS_N → OUT 96 173
- RB: R5T14 (0 0402 5% EMPTY) → SPI1_CS1_N_SV_HDR → OUT 267
- RC: R5T13 (0 0402 5% EMPTY) → SATA_LED_R_N → OUT 138

CAD NOTE: 3 PAD RA, RB

22 OUT GPPC_E17_THC0_SPI1_INT_R_N
- RA: R4F91 (0 0402 5% CHIP) → THC0_SPI1_INT_N_TCH_PNL1 → IN 126
- RB: R4F92 (0 0402 5% EMPTY) → THC0_SPI1_INT_N_SV_HDR → IN 267
- RC: R4F90 (0 0402 5% EMPTY) → HSIO_AIC_PCIE_SLOT3_WAKE_N → IN 202

CAD NOTE: 4 PAD

259 68 22 IN GPPC_E6_THC0_SPI1_RST_N
- RA: R4G14 (0 0402 5% CHIP) → THC0_SPI1_RST_N_TCH_PNL1 → OUT 126
- RB: R4G12 (0 0402 5% EMPTY) → THC0_SPI1_RST_N_SV_HDR → OUT 267

CAD NOTE: 3 PAD

I2S SHARING OPTIONS

12 IN GPPC_A17_DISP_MISC_C_I2S4_TXD
- R3G35 (33 0402 5% EMPTY) → I2S4_TXD_SV_HDR → BI 206
- R3G34 (0 0402 5% CHIP) → EDP2_VDD_EN → BI 239

CAD NOTE: 3 PAD

12 IN GPPC_A21_DDPC_CTRLCLK_I2S5_TXD
- R3F126 (33 0402 5% EMPTY) → I2S5_TXD_SV_HDR → BI 206
- R3F127 (0 0402 5% CHIP) → EDP2_BKLT_EN → BI 92 239

CAD NOTE: 3 PAD

12 IN GPPC_A22_DDPC_CTRLDATA_I2S5_RXD
- R3F125 (33 0402 5% EMPTY) → I2S5_RXD_SV_HDR → BI 206
- R3F124 (0 0402 5% CHIP) → EDP2_BKLT_CTRL → BI 91

CAD NOTE: 3 PAD

262 21 IN GPPC_H0
- R6R12 (0 0402 5% CHIP) → GPPC_H0_M2_SSD_RST_N → OUT 41
- R6R11 (0 0402 5% EMPTY) → HSIO_AIC_PCIE_SLOT4_RST_N → OUT 202

CAD NOTE: 3 PAD

263 21 IN GPPC_H1
- R3G31 (0 0402 5% CHIP) → GPPC_H1_TCH_PAD_TCH_PNL2_LS_EN → OUT 236 244
- R3G32 (0 0402 5% EMPTY) → GPPC_H1_AUDIO_PWREN → OUT 235

44 IN GPPC_F4_CNV_RF_RESET_N
- R4G2 (0 0402 5% EMPTY) → CNV_RF_RESET_R_N → OUT 145
- R4G3 (0 0402 5% CHIP) → GPPC_F4_X1_PCIE_SLOT2_WAKE_N → OUT 200

44 IN GPPC_F5_MODEM_CLKREQ
- R5V10 (0 0402 5% EMPTY) → MODEM_CLKREQ_R → OUT 145
- R5V9 (0 0402 5% CHIP) → GPPC_F5_ONBOARD_X4_PCIE_SLOT1_WAKE_N → OUT 198

[PAGE_TITLE=GPIO - SHARING OPTIONS -1 - THC, SPI, UART]

MODULE REV DETAILS

MODULE NAME	REV	DATE

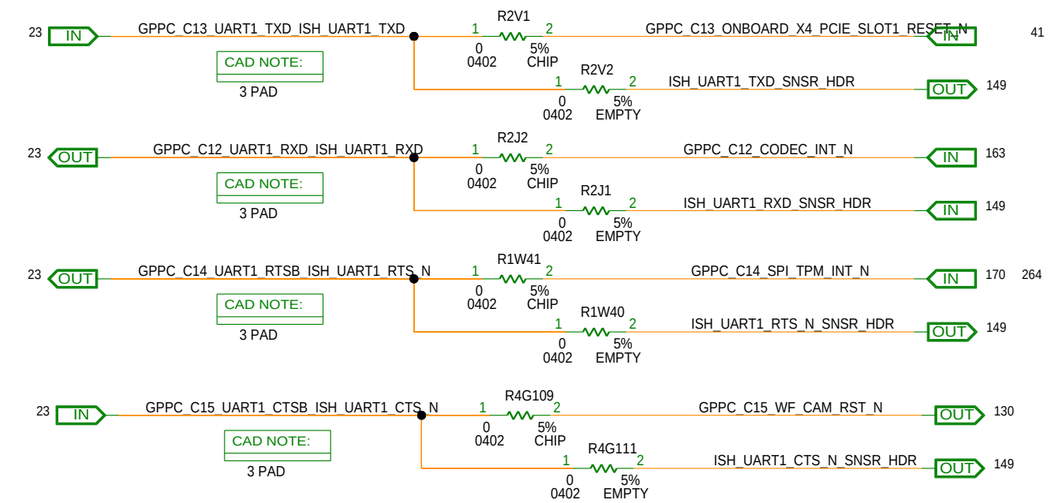
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.30
Wed Dec 18 18:05:45 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	30	1.0

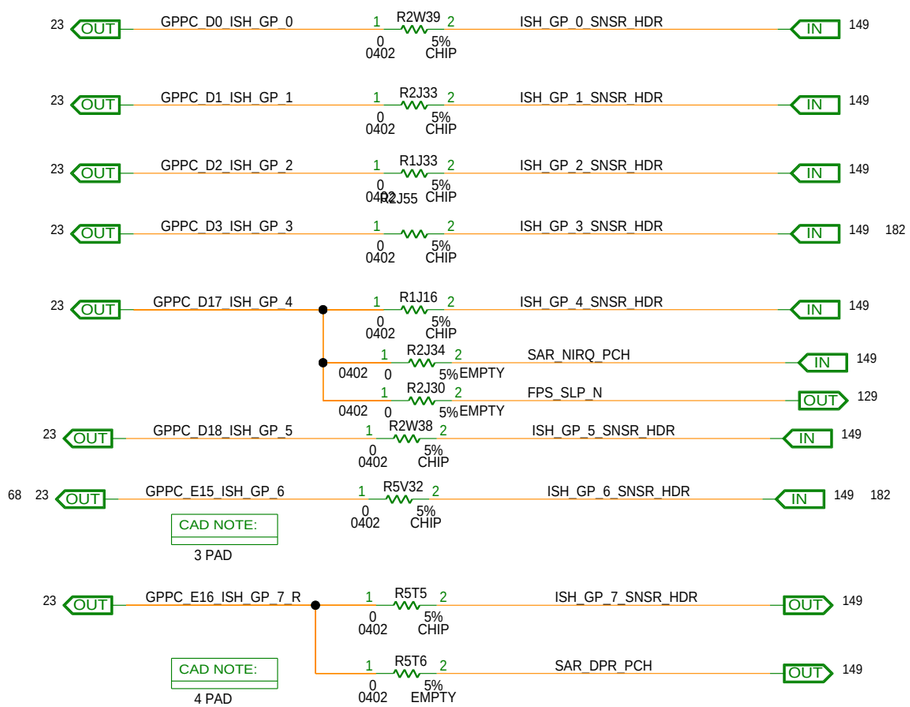
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

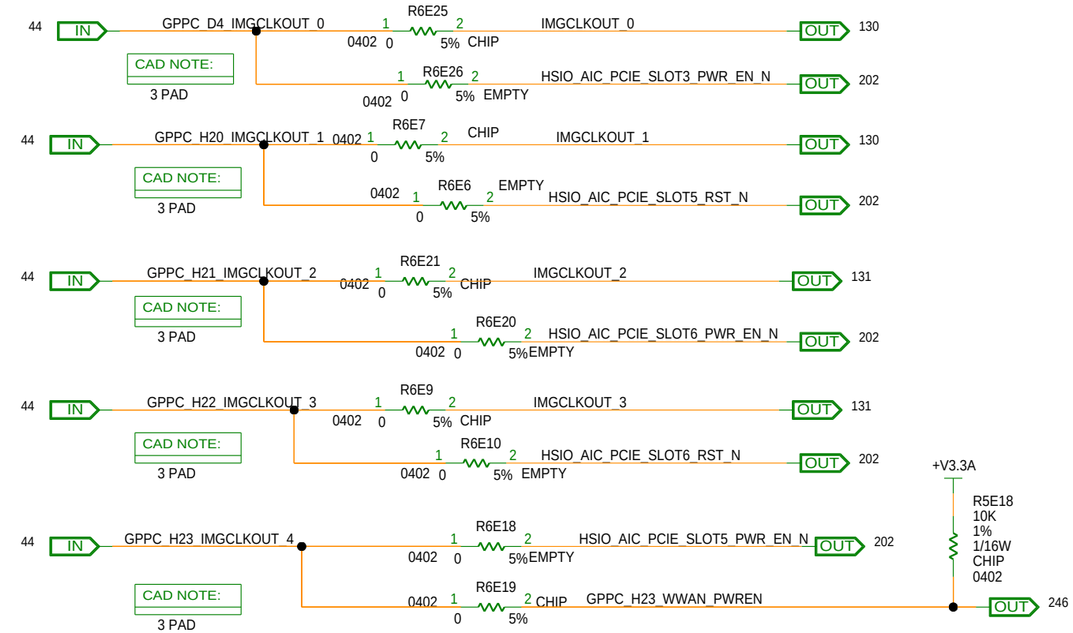
LPSS UART1/ ISH UART1 SHARING OPTIONS



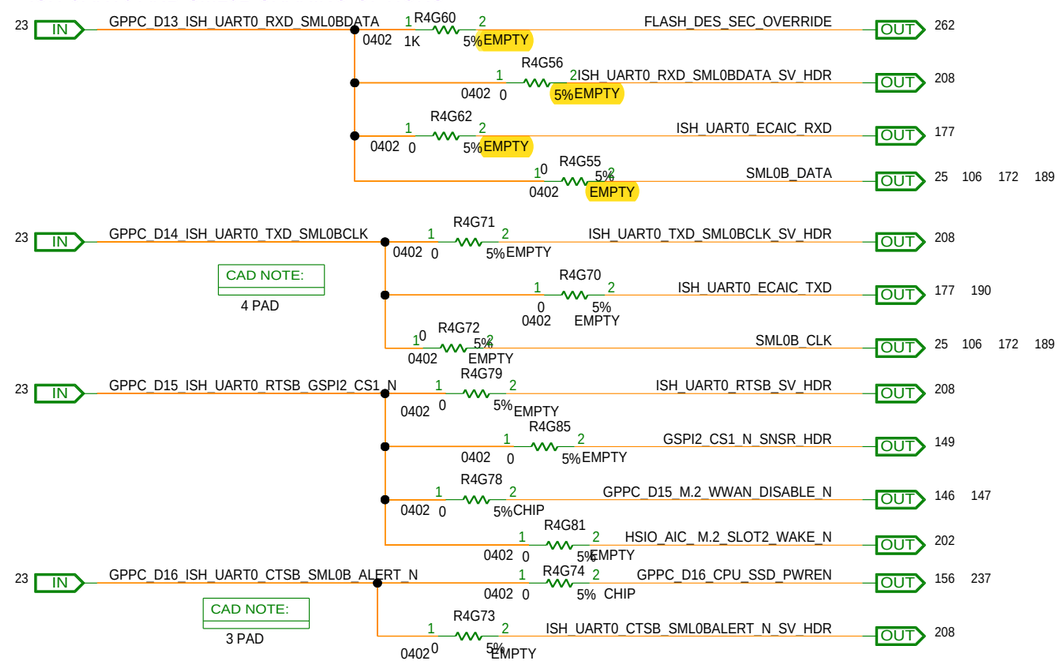
ISH GPIO SHARING OPTIONS



IMGCLKOUT SHARING OPTIONS



ISH UART0 AND SML0B SHARING OPTIONS



[PAGE_TITLE=GPIO - ISH SHARING OPTIONS -2 - I2C, UART ,GPIO]

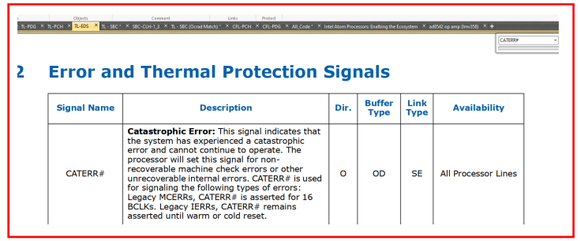
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.31
Wed Dec 18 18:05:46 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	31	1.0

CUSTOM TEXT BPAGE

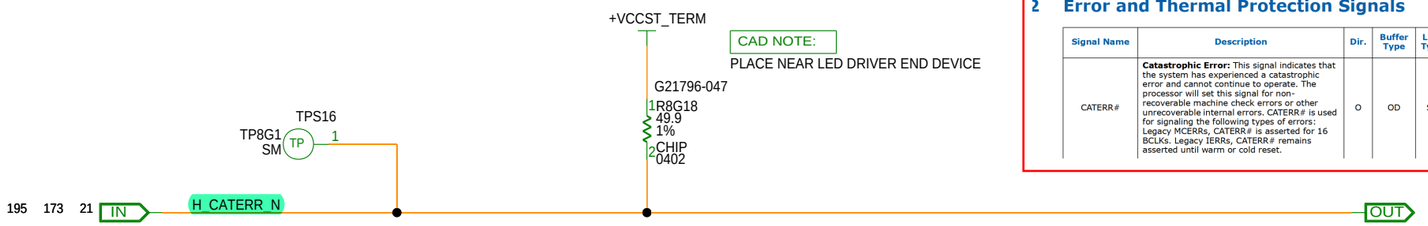
MODULE REV DETAILS		
MODULE NAME	REV	DATE

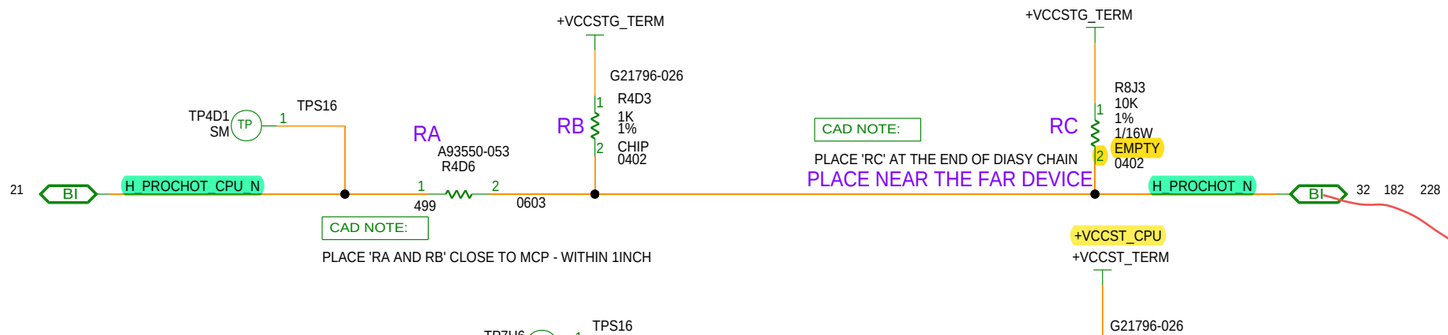
CPU SIDEBAND SIGNALS

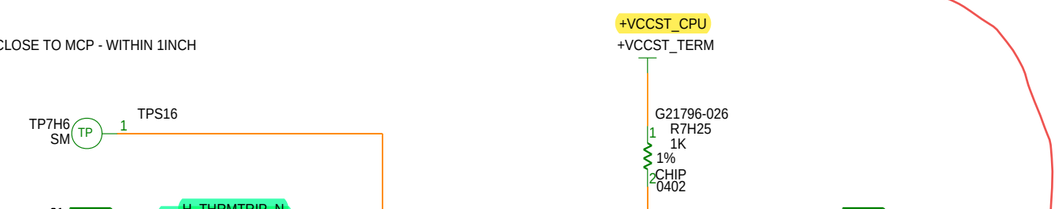


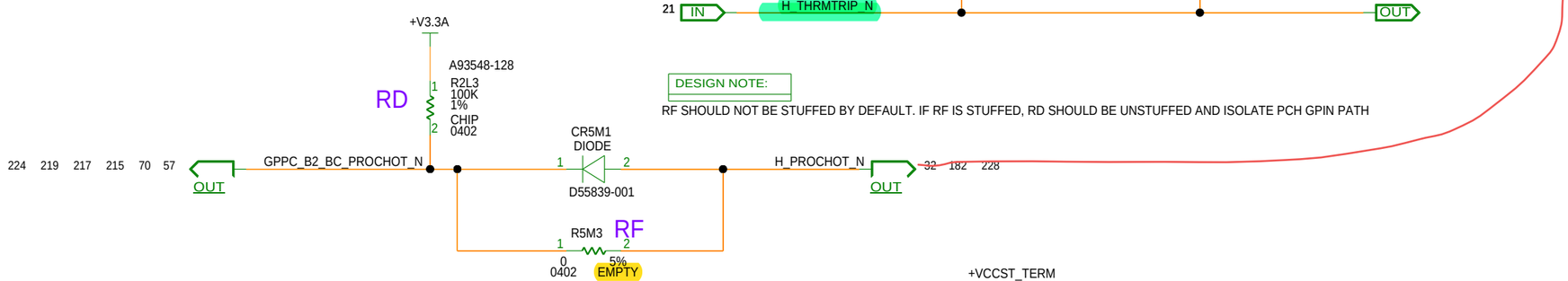
2 Error and Thermal Protection Signals

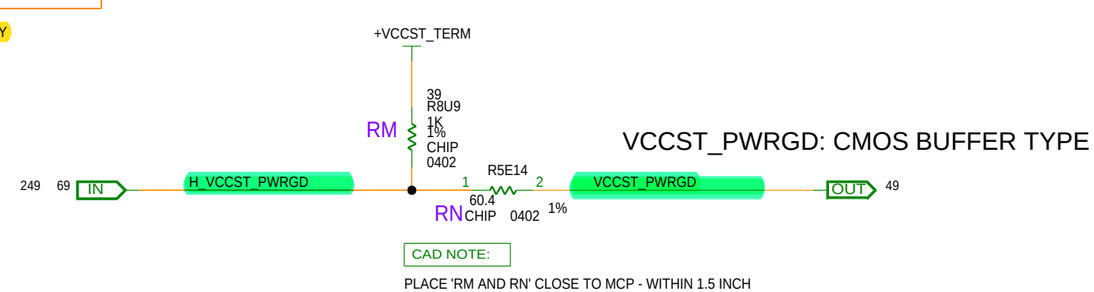
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.	O	OD	SE	All Processor Lines











[PAGE_TITLE=GPIO - OTHER PCH GPIO SHARING OPTIONS - 1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.32
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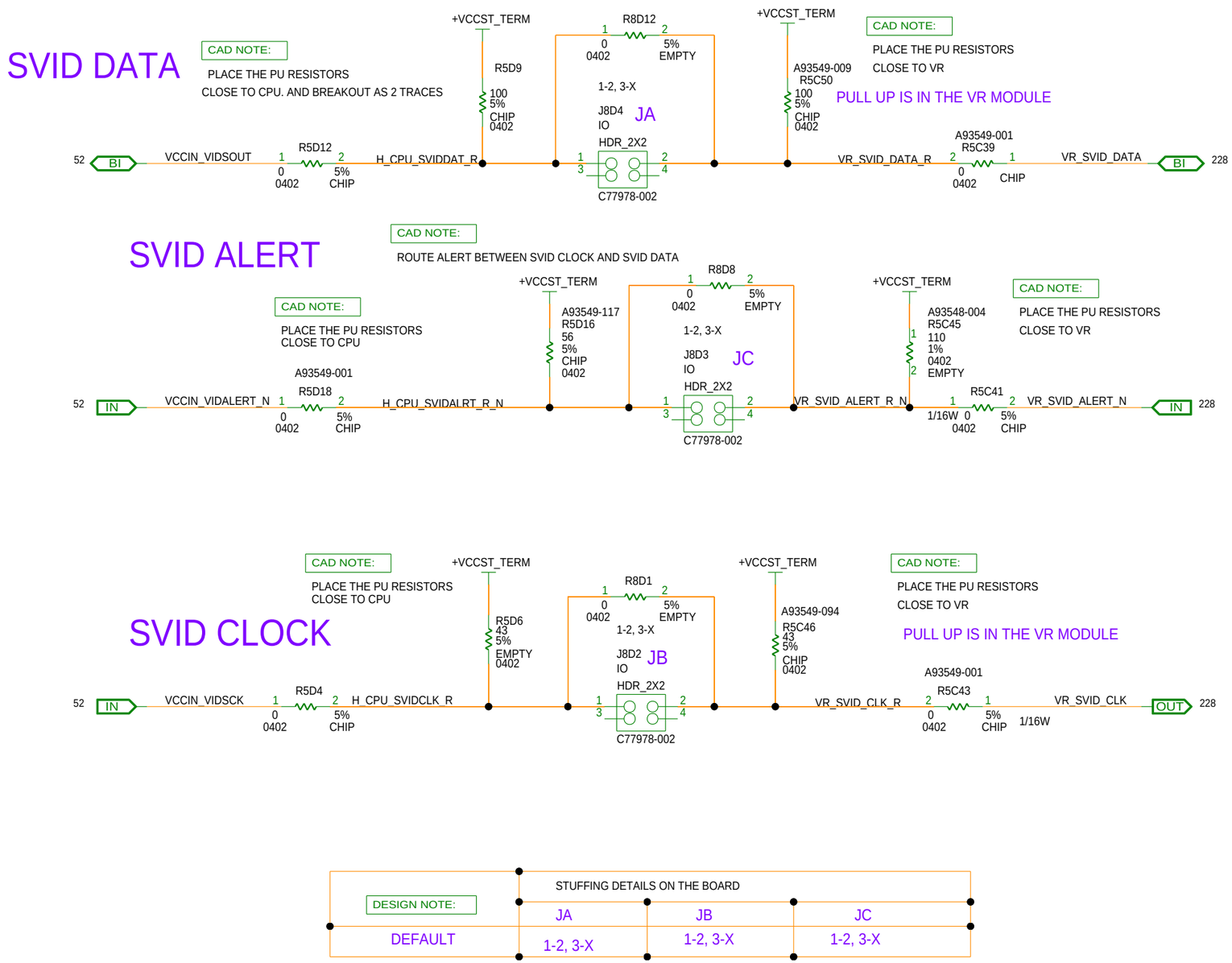
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	32	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=SVID SIGNALS

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.33
Wed Dec 18 18:05:48 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	33	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

U4E1

SOC

1.6

TGL_UP3_IP_EXT

9 OF 21

40	OUT	PCIE3_P12_SATA_1_TSN_0D_TX_DP	BT7	PCIE12_TXP/SATA1_TXP
40	OUT	PCIE3_P12_SATA_1_TSN_0D_TX_DN	BT8	PCIE12_TXN/SATA1_TXN
40	IN	PCIE3_P12_SATA_1_TSN_0D_RX_DP	CE2	PCIE12_RXP/SATA1_RXP
40	IN	PCIE3_P12_SATA_1_TSN_0D_RX_DN	CE1	PCIE12_RXN/SATA1_RXN
40	OUT	PCIE3_P11_SATA_0_TSN_0C_TX_DP	BT9	PCIE11_TXP/SATA0_TXP
40	OUT	PCIE3_P11_SATA_0_TSN_0C_TX_DN	BV9	PCIE11_TXN/SATA0_TXN
40	IN	PCIE3_P11_SATA_0_TSN_0C_RX_DP	CF4	PCIE11_RXP/SATA0_RXP
40	IN	PCIE3_P11_SATA_0_TSN_0C_RX_DN	CF3	PCIE11_RXN/SATA0_RXN
39	OUT	PCIE3_P10_UFS_11_TX_DP	BV7	PCIE10_TXP
39	OUT	PCIE3_P10_UFS_11_TX_DN	BV8	PCIE10_TXN
39	IN	PCIE3_P10_UFS_11_RX_DP	CG2	PCIE10_RXP
39	IN	PCIE3_P10_UFS_11_RX_DN	CG1	PCIE10_RXN
39	OUT	PCIE3_P9_UFS_10_LAN_0C_TX_DP	BY7	PCIE9_TXP
39	OUT	PCIE3_P9_UFS_10_LAN_0C_TX_DN	BY8	PCIE9_TXN
39	IN	PCIE3_P9_UFS_10_LAN_0C_RX_DP	CG5	PCIE9_RXP
39	IN	PCIE3_P9_UFS_10_LAN_0C_RX_DN	CG4	PCIE9_RXN
38	OUT	PCIE3_P8_UFS_01_LAN_0B_TSN_0B_TX_DP	CB8	PCIE8_TXP
38	OUT	PCIE3_P8_UFS_01_LAN_0B_TSN_0B_TX_DN	CB7	PCIE8_TXN
38	IN	PCIE3_P8_UFS_01_LAN_0B_TSN_0B_RX_DP	CK5	PCIE8_RXP
38	IN	PCIE3_P8_UFS_01_LAN_0B_TSN_0B_RX_DN	CK4	PCIE8_RXN
38	OUT	PCIE3_P7_UFS_00_LAN_0A_TSN_0A_TX_DP	CD9	PCIE7_TXP
38	OUT	PCIE3_P7_UFS_00_LAN_0A_TSN_0A_TX_DN	CD8	PCIE7_TXN
38	IN	PCIE3_P7_UFS_00_LAN_0A_TSN_0A_RX_DP	CK1	PCIE7_RXP
38	IN	PCIE3_P7_UFS_00_LAN_0A_TSN_0A_RX_DN	CK2	PCIE7_RXN
37	OUT	PCIE3_P6_TX_DP	CG8	PCIE6_TXP
37	OUT	PCIE3_P6_TX_DN	CG7	PCIE6_TXN
37	IN	PCIE3_P6_RX_DP	CL4	PCIE6_RXP
37	IN	PCIE3_P6_RX_DN	CL3	PCIE6_RXN
37	OUT	PCIE3_P5_TX_DP	CJ8	PCIE5_TXP
37	OUT	PCIE3_P5_TX_DN	CJ7	PCIE5_TXN
37	IN	PCIE3_P5_RX_DP	CN2	PCIE5_RXP
37	IN	PCIE3_P5_RX_DN	CN1	PCIE5_RXN
36	OUT	PCIE3_P4_USB31_P4_TX_DP	CR8	PCIE4_TXP/USB31_4_TXP
36	OUT	PCIE3_P4_USB31_P4_TX_DN	CR7	PCIE4_TXN/USB31_4_TXN
36	IN	PCIE3_P4_USB31_P4_RX_DP	CN5	PCIE4_RXP/USB31_4_RXP
36	IN	PCIE3_P4_USB31_P4_RX_DN	CN4	PCIE4_RXN/USB31_4_RXN
36	OUT	PCIE3_P3_USB31_P3_TX_DP	CU8	PCIE3_TXP/USB31_3_TXP
36	OUT	PCIE3_P3_USB31_P3_TX_DN	CU7	PCIE3_TXN/USB31_3_TXN
36	IN	PCIE3_P3_USB31_P3_RX_DP	CT2	PCIE3_RXP/USB31_3_RXP
36	IN	PCIE3_P3_USB31_P3_RX_DN	CT1	PCIE3_RXN/USB31_3_RXN
35	OUT	PCIE3_P2_USB31_P2_TX_DP	CW8	PCIE2_TXP/USB31_2_TXP
35	OUT	PCIE3_P2_USB31_P2_TX_DN	CW7	PCIE2_TXN/USB31_2_TXN
35	IN	PCIE3_P2_USB31_P2_RX_DP	CU3	PCIE2_RXP/USB31_2_RXP
35	IN	PCIE3_P2_USB31_P2_RX_DN	CT4	PCIE2_RXN/USB31_2_RXN
35	OUT	PCIE3_P1_USB31_P1_TX_DP	DA8	PCIE1_TXP/USB31_1_TXP
35	OUT	PCIE3_P1_USB31_P1_TX_DN	DA7	PCIE1_TXN/USB31_1_TXN
35	IN	PCIE3_P1_USB31_P1_RX_DP	CV2	PCIE1_RXP/USB31_1_RXP
35	IN	PCIE3_P1_USB31_P1_RX_DN	CV1	PCIE1_RXN/USB31_1_RXN

LPID6529

USB2P_10	CV4	USB2_P10_DP	BI	144
USB2N_10	CY3	USB2_P10_DN	BI	144
USB2P_9	DD5	USB2_P9_DP	BI	154
USB2N_9	DD4	USB2_P9_DN	BI	154
USB2P_8	CW9	USB2_P8_DP	BI	151
USB2N_8	DA9	USB2_P8_DN	BI	151
USB2P_7	DD1	USB2_P7_DP	BI	72
USB2N_7	DD2	USB2_P7_DN	BI	72
USB2P_6	DA1	USB2_P6_DP	BI	43
USB2N_6	DA2	USB2_P6_DN	BI	43
USB2P_5	DA12	USB2_P5_DP	BI	43
USB2N_5	DA11	USB2_P5_DN	BI	43
USB2P_4	DC8	USB2_P4_DP	BI	151
USB2N_4	DC7	USB2_P4_DN	BI	151
USB2P_3	DB4	USB2_P3_DP	BI	154
USB2N_3	DB3	USB2_P3_DN	BI	154
USB2P_2	DA5	USB2_P2_DP	BI	43
USB2N_2	DA4	USB2_P2_DN	BI	43
USB2P_1	DC11	USB2_P1_DP	BI	43
USB2N_1	DC9	USB2_P1_DN	BI	43
GPP_E0/SATAXPCIE0/SATAGP0	DP4	GPPC_E0_SATAXPCIE_0_SATAGP_0	BI	34 68
GPP_A12/SATAXPCIE1/SATAGP1/I2S3_SFRM	DF41	GPPC_A12_SATAXPCIE_1_SATAGP_1_I2S3_SFRM	BI	29
GPP_E9/USB_OC0#	DD8	GPPC_E9_USB2_OCB_0	BI	29 68 260
GPP_A16/USB_OC3#/I2S4_SFRM	DJ45	GPPC_A16_USB2_OCB_3_I2S4_SFRM	BI	29
GPP_E5/DEVSLP1	DN6	GPPC_E5_SATA_DEVSLP_1	BI	29 68
GPP_E4/DEVSLP0	DG8	GPPC_E4_SATA_DEVSLP_0	BI	29 68
GPP_H15/M2_SKT2_CFG3	DN29	GPPC_H15_M2_SKT2_CFG_3	BI	29
GPP_H14/M2_SKT2_CFG2	DK29	GPPC_H14_M2_SKT2_CFG_2	BI	29
GPP_H13/M2_SKT2_CFG1	DT31	GPPC_H13_M2_SKT2_CFG_1	BI	29
GPP_H12/M2_SKT2_CFG0	DR32	GPPC_H12_M2_SKT2_CFG_0	BI	29
PCIE_RCOMP_P	DV9	PCIE_RCOMPP		
PCIE_RCOMP_N	DT9	PCIE_RCOMPN		
USB_VBUSSENSE	DC12	USB2_VBUSSENSE		
USB_ID	DF1	USB2_ID		
USB2_COMP	DE1	USB2_COMP		
RSVD_BSCAN	E3	RSVD_BSCAN		202

R4F11 100 0402 CHIP 1%

TP_C25 TP4F1 SM

TP_C25 TP5F1 SM

G21796-341 R4F1 113 1% 1/16W CHIP 0402

R4F53 10K 5% 1/16W CHIP 0402

R4F55 10K 5% 1/16W CHIP 0402

CAD NOTE:

PLACE CLOSE TO XDP

CAD NOTE:

3 PAD WITH R5V55

68 34 IN GPPC_E0_SATAXPCIE_0_SATAGP_0 R4V13 0 0402 5% CHIP GPPC_E0_SATAXPCIE_0_SATAGP_0_R OUT 29

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL-U MCP (9 OF 21) - MODPHY

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.34
Wed Dec 18 18:05:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

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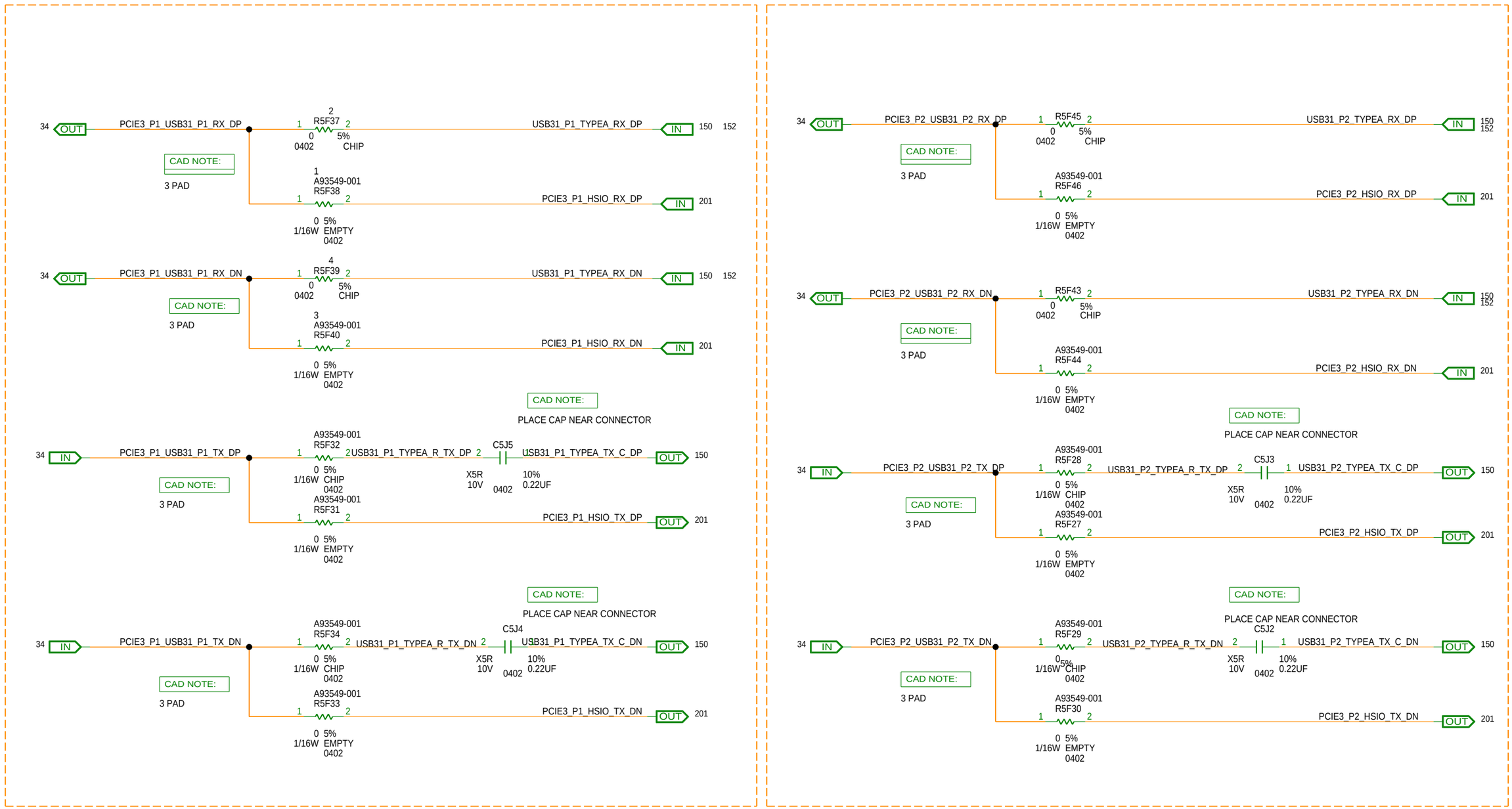
MODULE NAME	REV	DATE



[PAGE_TITLE=PCIE PORT 1&2 SHARING OPTIONS, AC CAPS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.35
Wed Dec 18 18:05:50 2019

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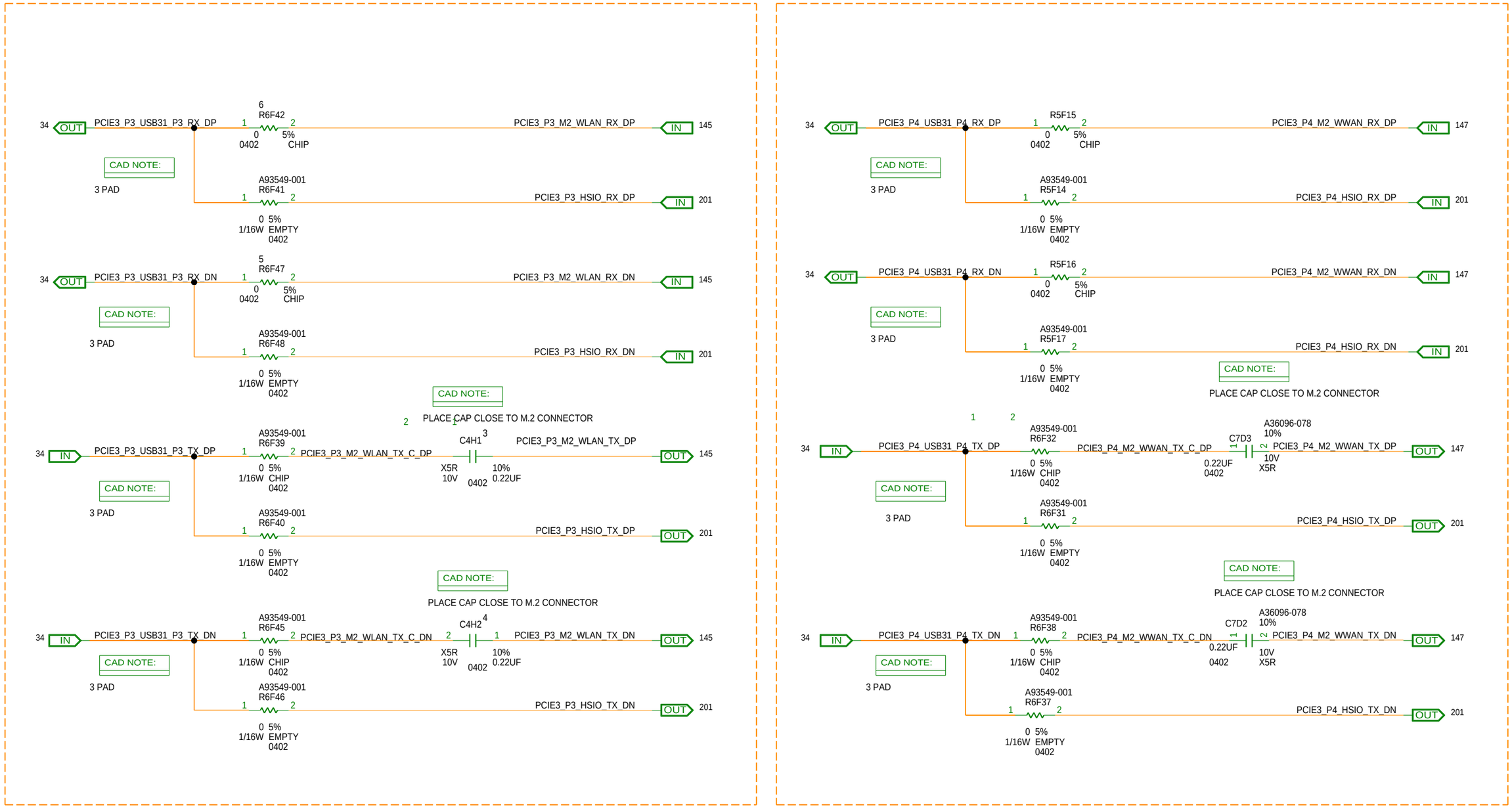

[PAGE_TITLE=PCIE PORT 3&4 SHARING OPTIONS, AC CAPS]

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Wed Dec 18 18:05:51 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

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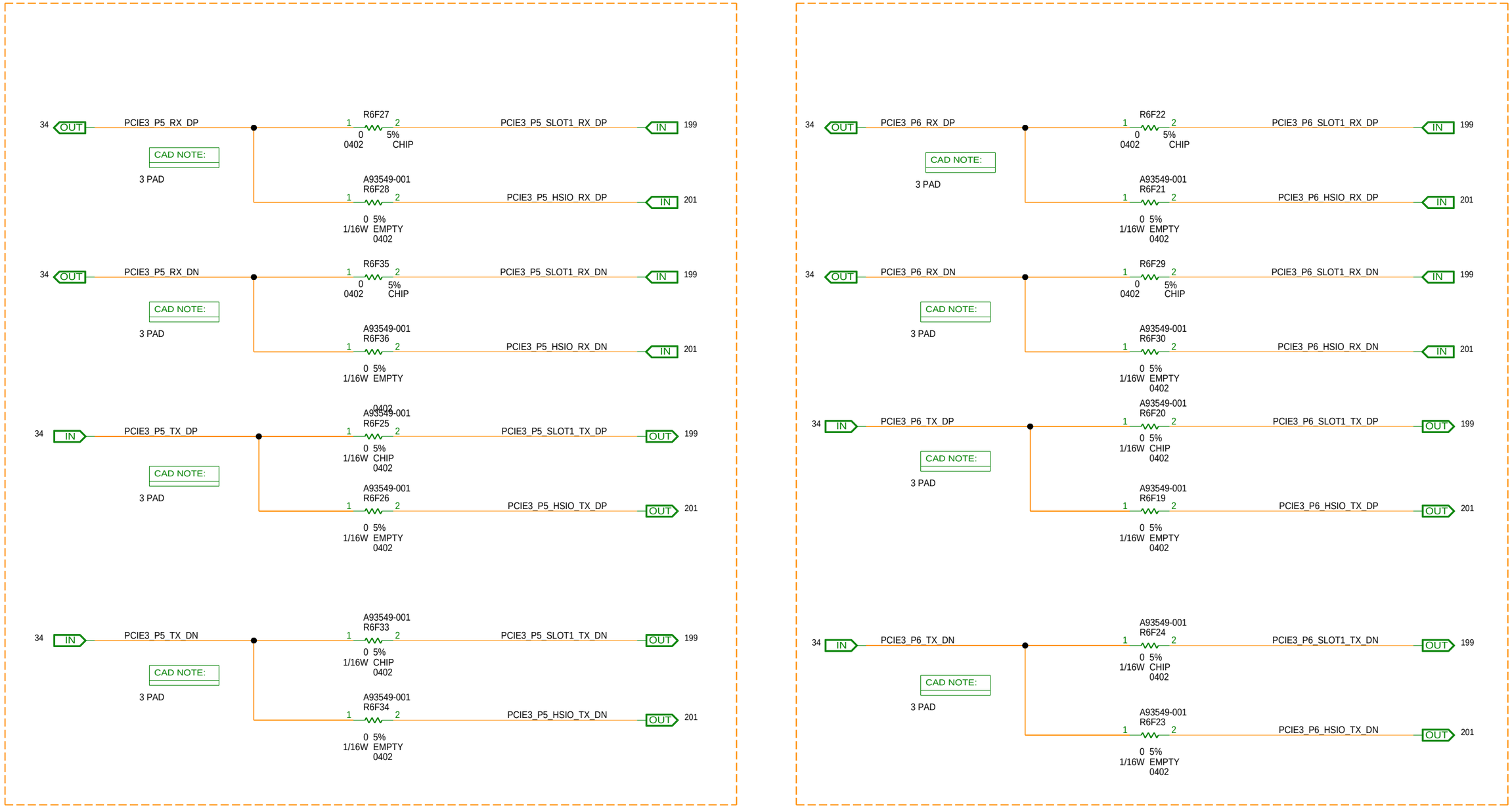

[PAGE_TITLE=PCIE PORT 5&6 SHARING OPTIONS, AC CAPS]

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Wed Dec 18 18:05:52 2019

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CUSTOM TEXT BPAGE

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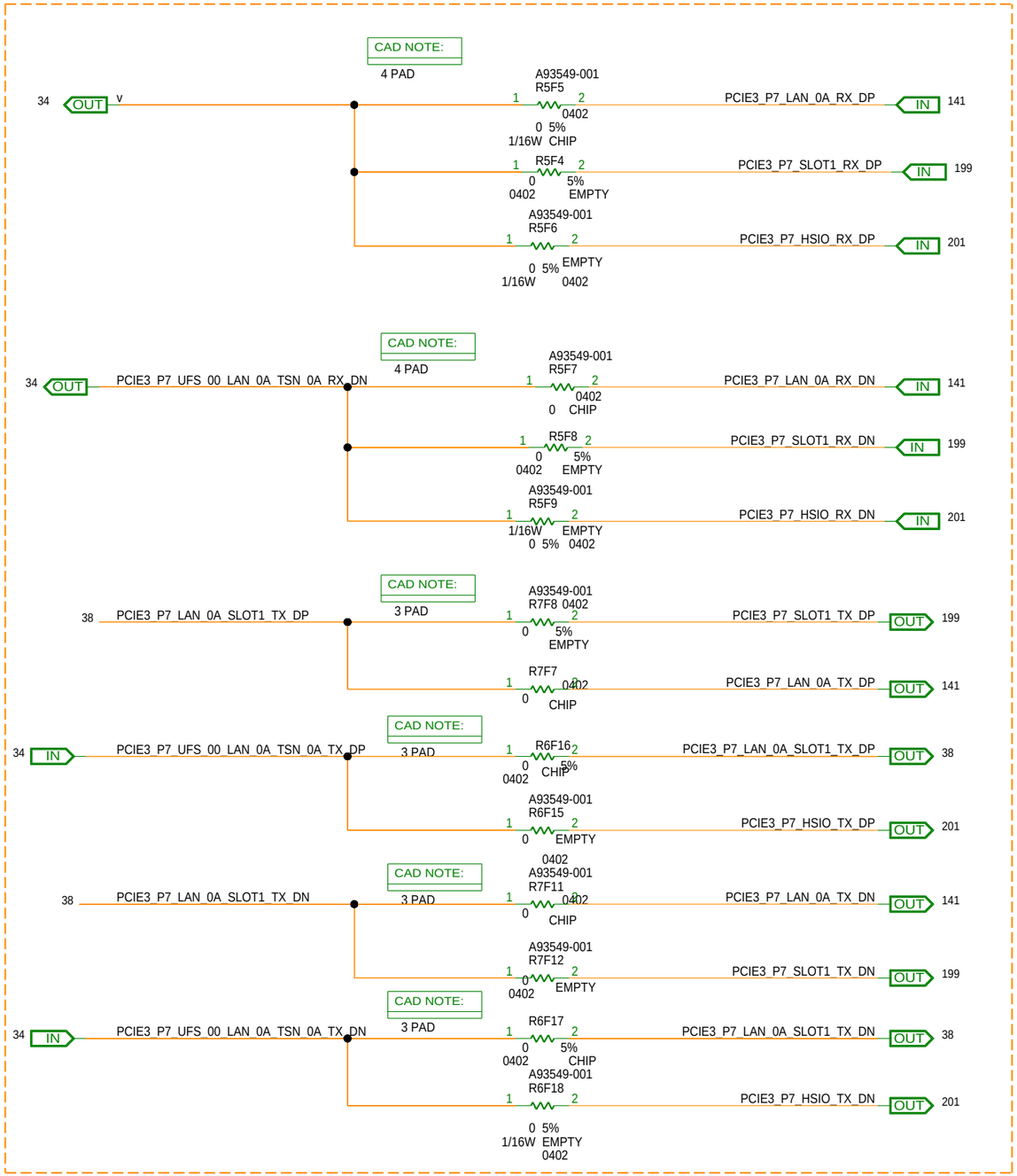

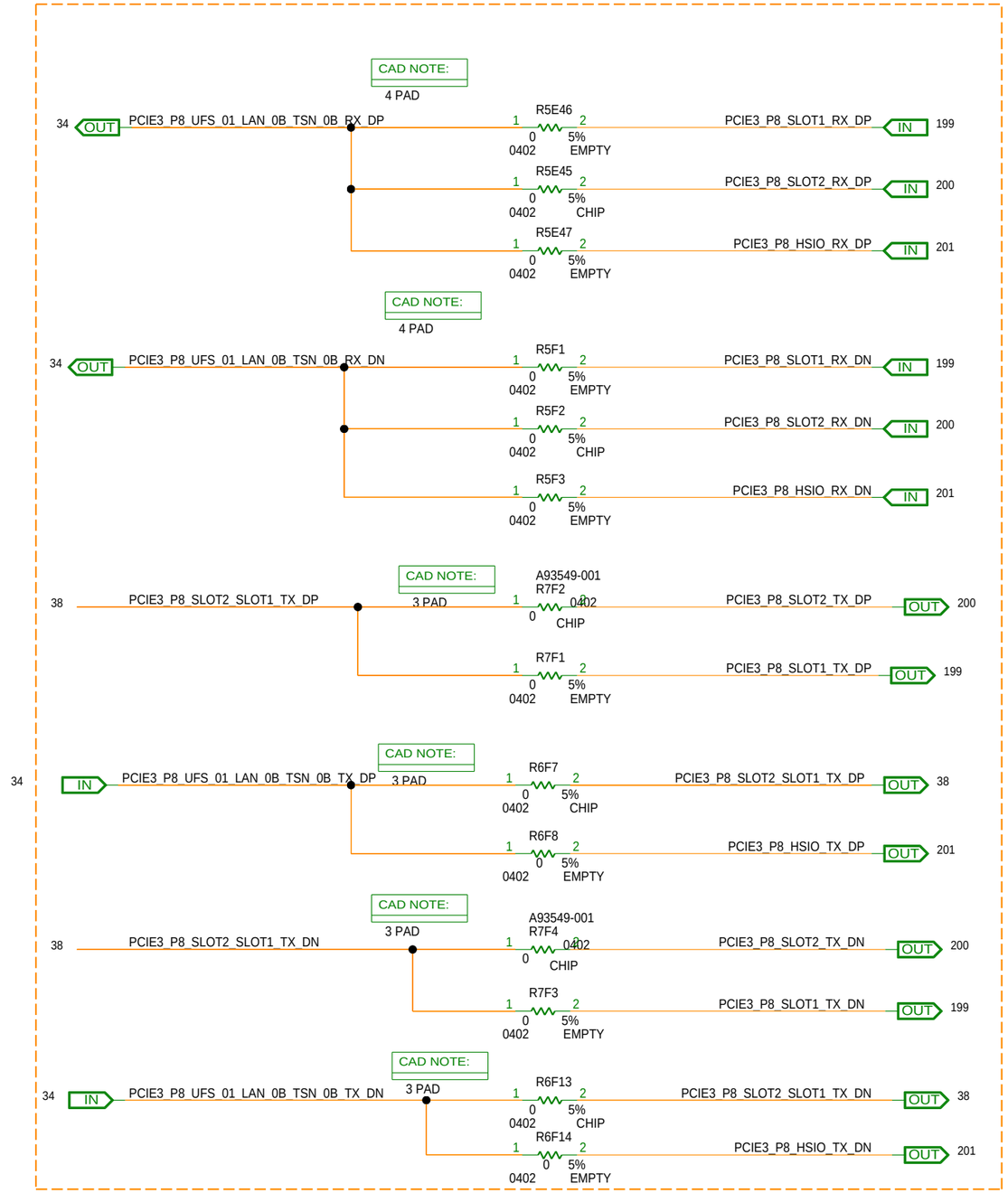

[PAGE_TITLE=PCIE PORT 7&8 SHARING OPTIONS, AC CAPS]

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Wed Dec 18 18:05:54 2019

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CUSTOM TEXT BPAGE

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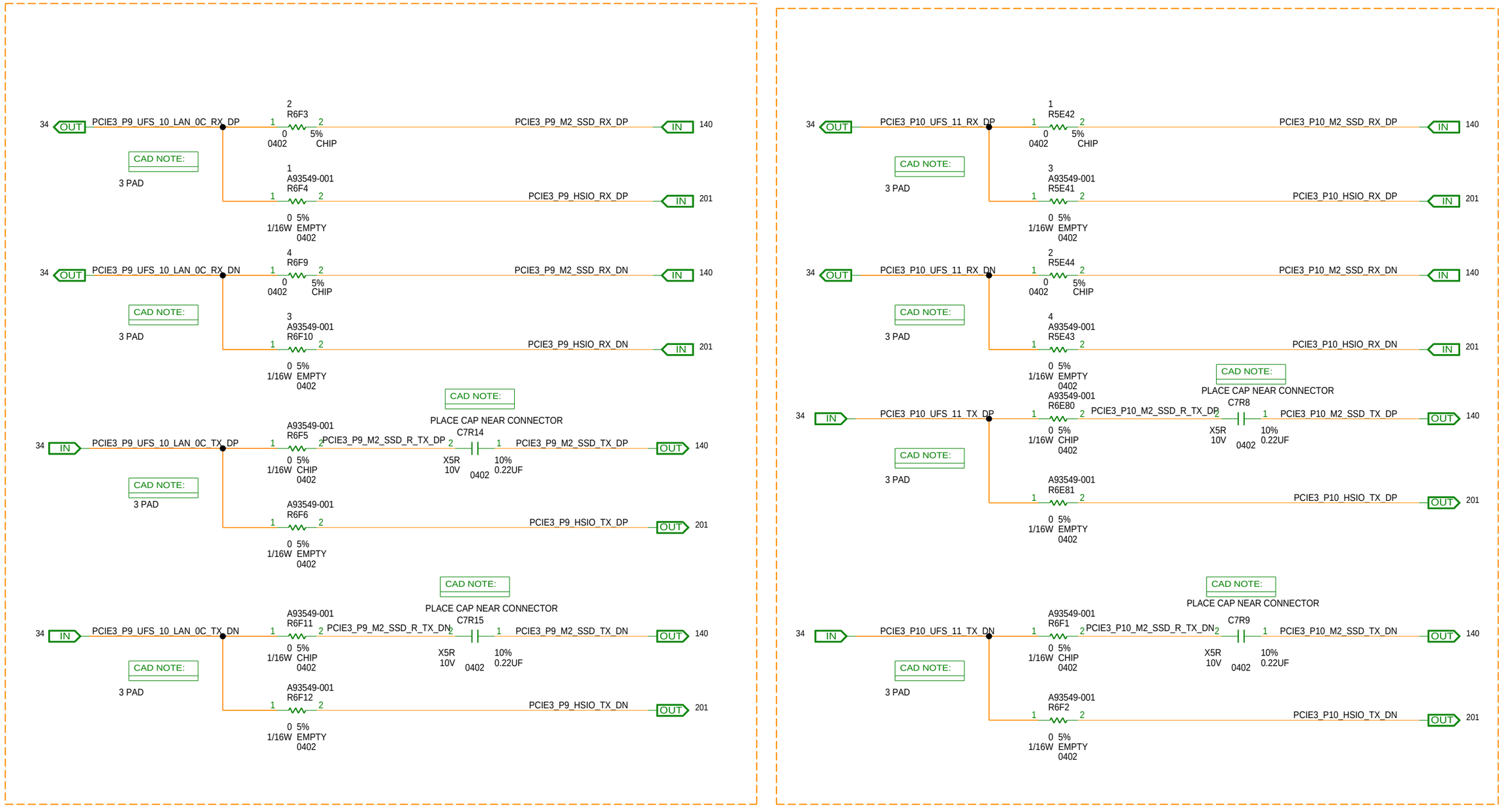

[PAGE_TITLE=PCIE PORT 9&10 SHARING OPTIONS, AC CAPS]

BPAGE DRAWING
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Wed Dec 18 18:05:55 2019

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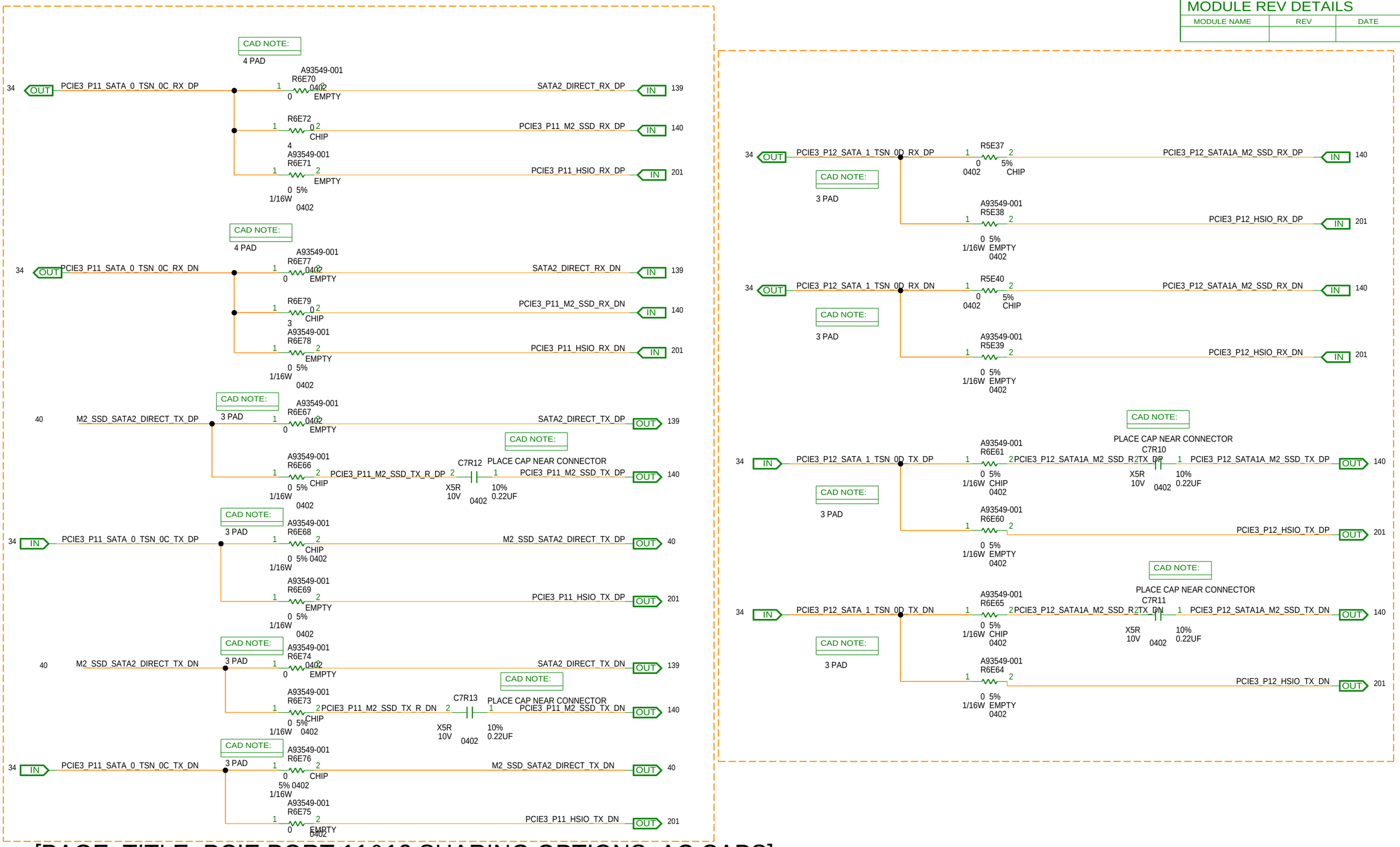

[PAGE_TITLE=PCIE PORT 11&12 SHARING OPTIONS, AC CAPS]

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Wed Dec 18 18:05:56 2019

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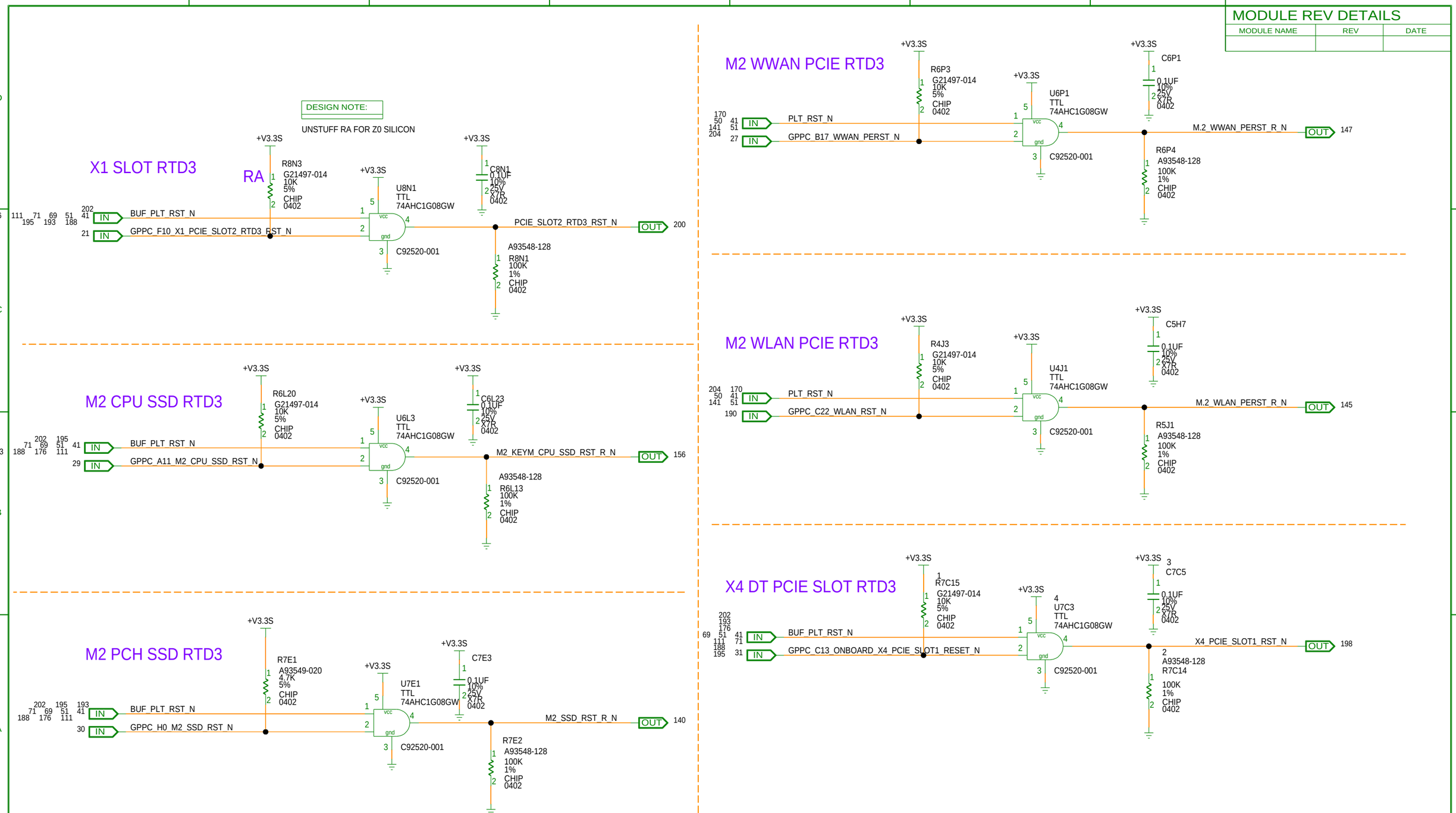

[PAGE_TITLE=PCIE PORT RESET RTD3 CIRCUIT

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Wed Dec 18 18:05:58 2019

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CUSTOM TEXT BPAGE

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MODULE NAME	REV	DATE

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Tue Oct 15 12:49:02 2019

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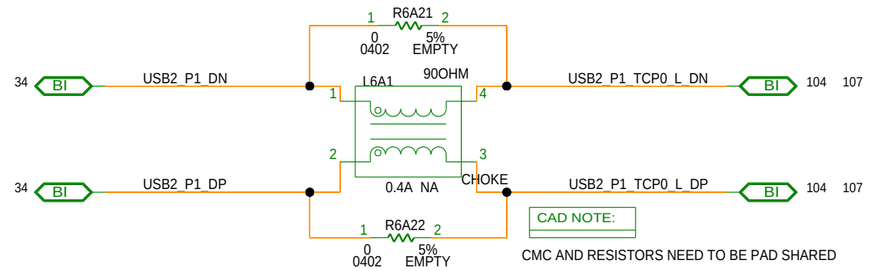
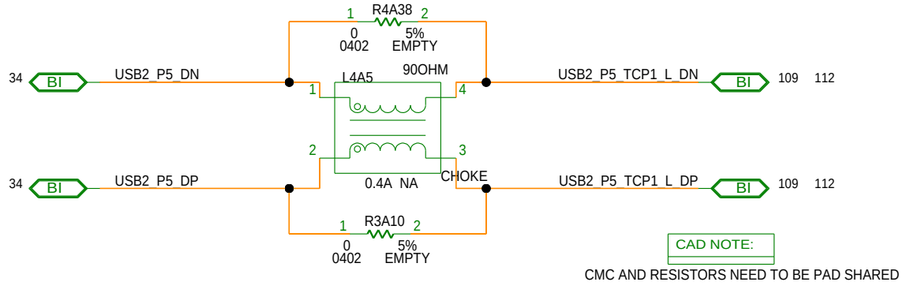
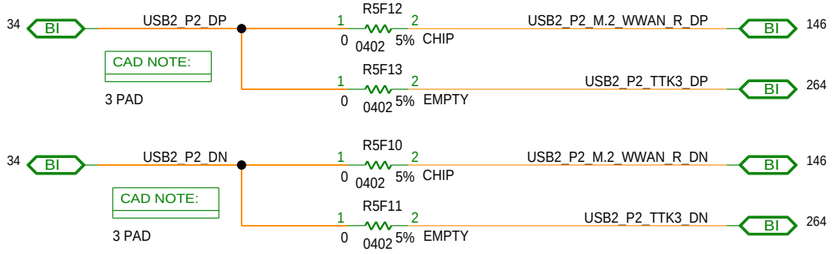
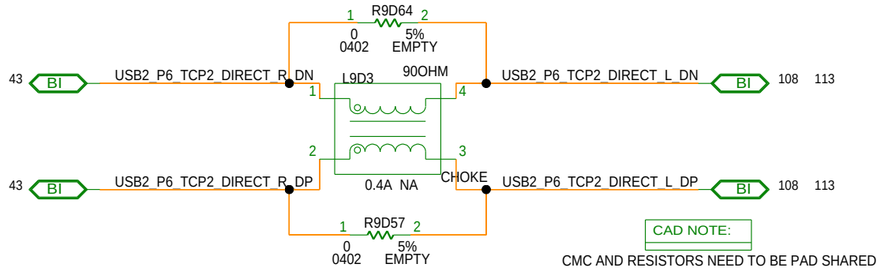
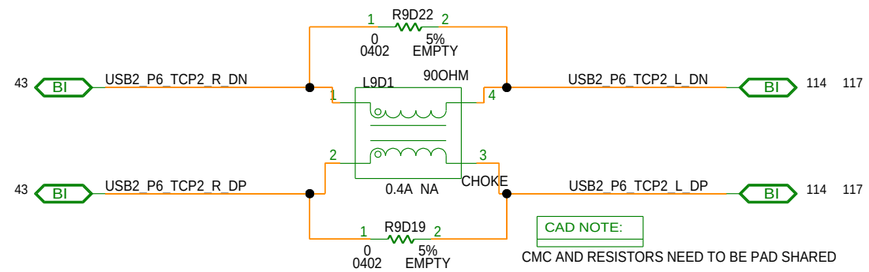




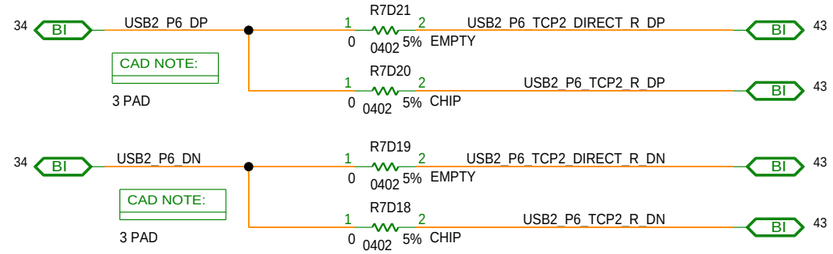
USB2 PORT2 SHARING OPTION

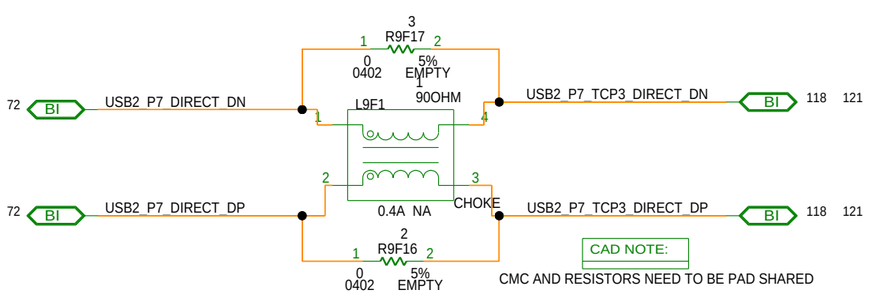






USB2 PORT6 SHARING OPTION





[PAGE_TITLE= USB2 CMC & SHARING]

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Wed Dec 18 18:06:00 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

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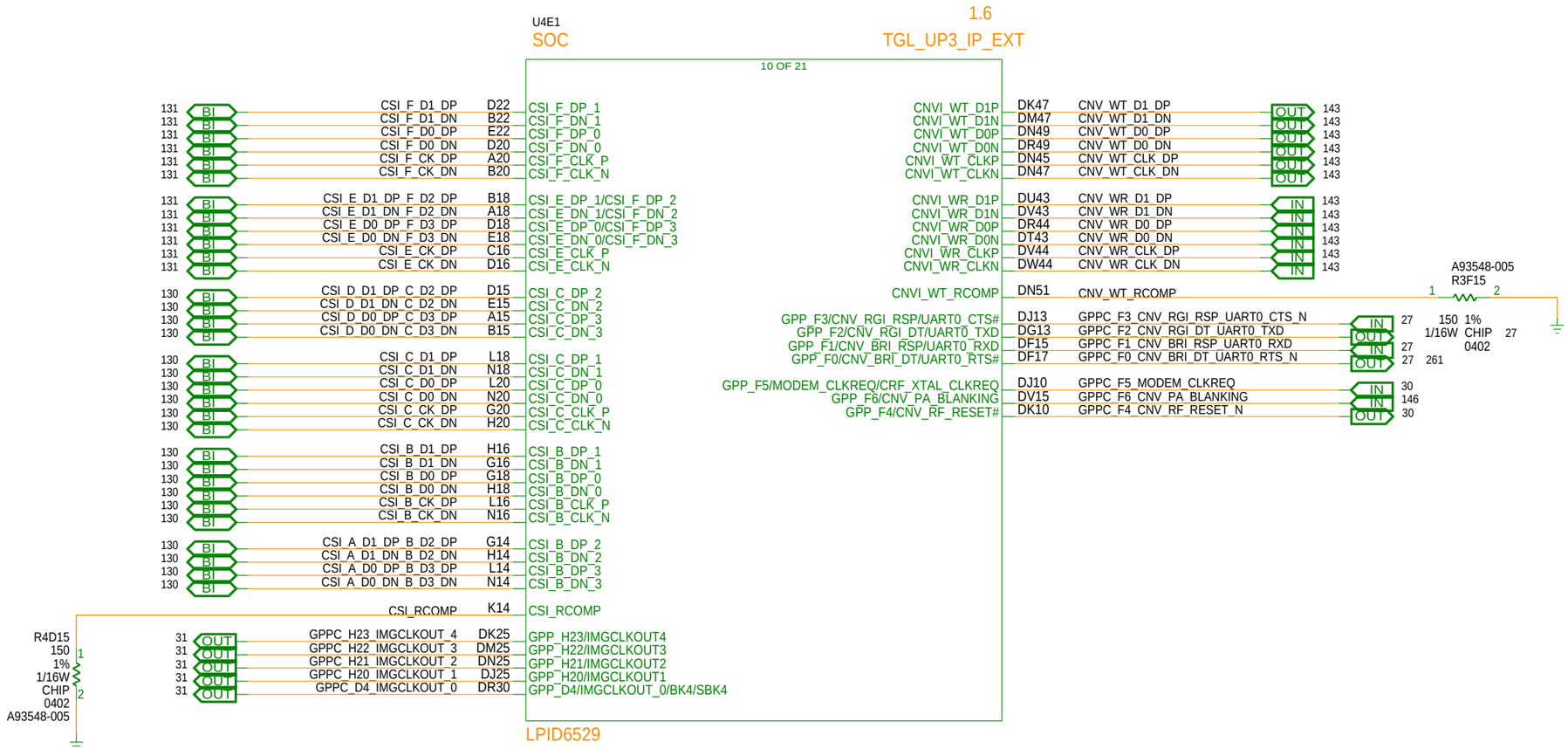
MODULE NAME	REV	DATE

DIDNT IMPLEMENT YET



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL-U MCP (10 OF 21) - CSI2, CNVI]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.44
Wed Dec 18 18:06:01 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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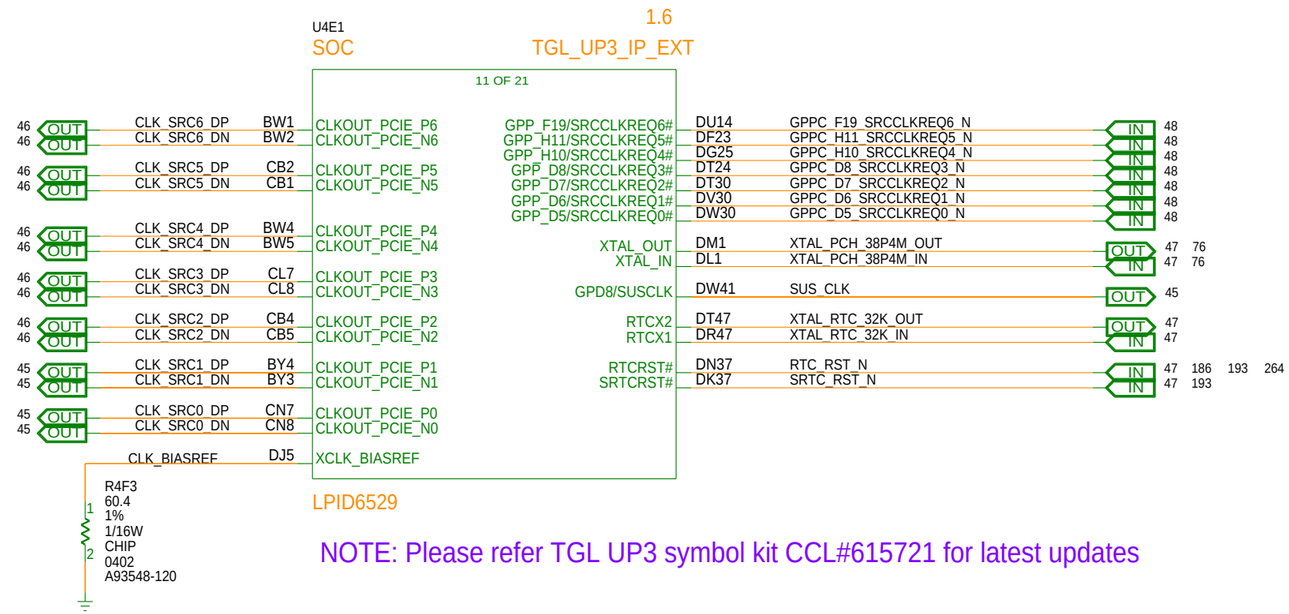
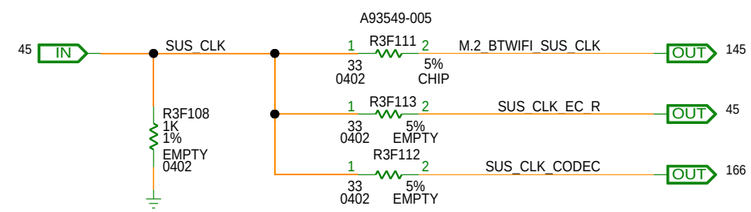
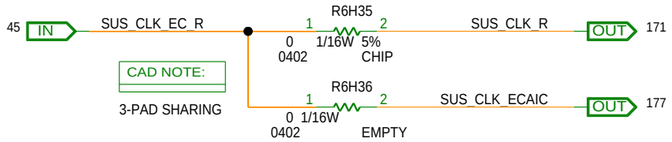
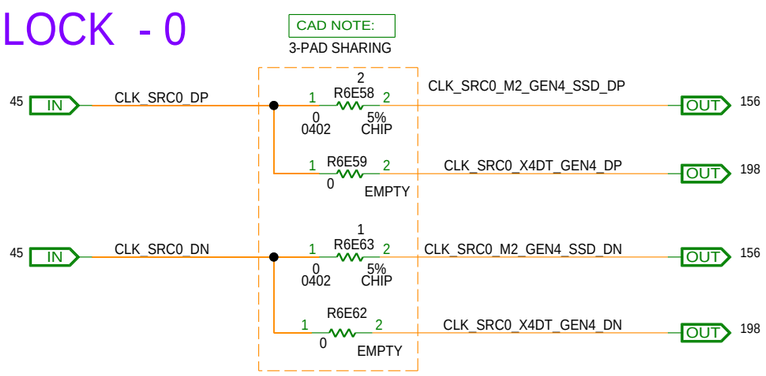


NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

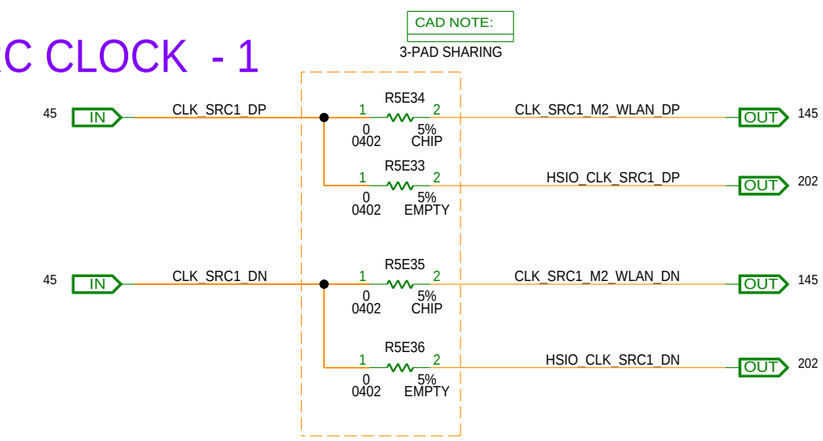




SRC CLOCK - 0



SRC CLOCK - 1



[PAGE_TITLE=TGL-U MCP (11 OF 21) - CLOCK SIGNALS]

BPAGE DRAWING
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Wed Dec 18 18:06:02 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	45	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

SRC CLOCK - 3

CAD NOTE:
3-PAD SHARING

45 IN CLK_SRC3_DP → R6E46 (0 0402 5% CHIP) → CLK_SRC3_M2_SSD_DP OUT 140
R6E47 (0 0402 5% EMPTY) → HSIO_CLK_SRC3_DP OUT 202

45 IN CLK_SRC3_DN → R6E51 (0 0402 5% CHIP) → CLK_SRC3_M2_SSD_DN OUT 140
R6E50 (0 0402 5% EMPTY) → HSIO_CLK_SRC3_DN OUT 202

SRC CLOCK - 4

CAD NOTE:
3-PAD SHARING

45 IN CLK_SRC4_DP → R6E48 (0 0402 5% CHIP) → CLK_SRC4_LAN_DP OUT 141
R6E49 (0 0402 5% EMPTY) → HSIO_CLK_SRC4_DP OUT 202

45 IN CLK_SRC4_DN → R6E53 (0 0402 5% CHIP) → CLK_SRC4_LAN_DN OUT 141
R6E52 (0 0402 5% EMPTY) → HSIO_CLK_SRC4_DN OUT 202

C5V4 A36094-015 2.2PF 10% 50V EMPTY 0402 CA
C5V3 A36094-015 2.2PF 10% 50V EMPTY 0402 CB

CAD NOTE:
PLACE CA AND CB CLOSE TO LAN CHIP

SRC CLOCK - 2

CAD NOTE:
3-PAD SHARING

45 IN CLK_SRC2_DP → R6E54 (0 0402 5% CHIP) → CLK_SRC2_M2_WWAN_DP OUT 147
R6E55 (0 0402 5% EMPTY) → HSIO_CLK_SRC2_DP OUT 202

45 IN CLK_SRC2_DN → R6E56 (0 0402 5% CHIP) → CLK_SRC2_M2_WWAN_DN OUT 147
R6E57 (0 0402 5% EMPTY) → HSIO_CLK_SRC2_DN OUT 202

SRC CLOCK - 5

CAD NOTE:
3-PAD SHARING

CAD NOTE:
PLACE CC AND CD CLOSE TO X1 PCIE SLOT

45 IN CLK_SRC5_DP → R5E26 (0 0402 5% CHIP) → CLK_SRC5_SLOT_2_DP OUT 200
R5E25 (0 0402 5% EMPTY) → HSIO_CLK_SRC5_DP OUT 202

C8C2 A36094-015 2.2PF 10% 50V EMPTY 0402 CC

45 IN CLK_SRC5_DN → R5E30 (0 0402 5% CHIP) → CLK_SRC5_SLOT_2_DN OUT 200
R5E29 (0 0402 5% EMPTY) → HSIO_CLK_SRC5_DN OUT 202

C8C3 A36094-015 2.2PF 10% 50V EMPTY 0402 CD

SRC CLOCK - 6

CAD NOTE:
3-PAD SHARING

45 IN CLK_SRC6_DP → R6E43 (0 0402 5% CHIP) → CLK_SRC6_SLOT1_DP OUT 198
R6E42 (0 0402 5% EMPTY) → HSIO_CLK_SRC6_DP OUT 202

45 IN CLK_SRC6_DN → R6E45 (0 0402 5% CHIP) → CLK_SRC6_SLOT1_DN OUT 198
R6E44 (0 0402 5% EMPTY) → HSIO_CLK_SRC6_DN OUT 202

[PAGE_TITLE=SRC SHARING OPTIONS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.46
Wed Dec 18 18:06:03 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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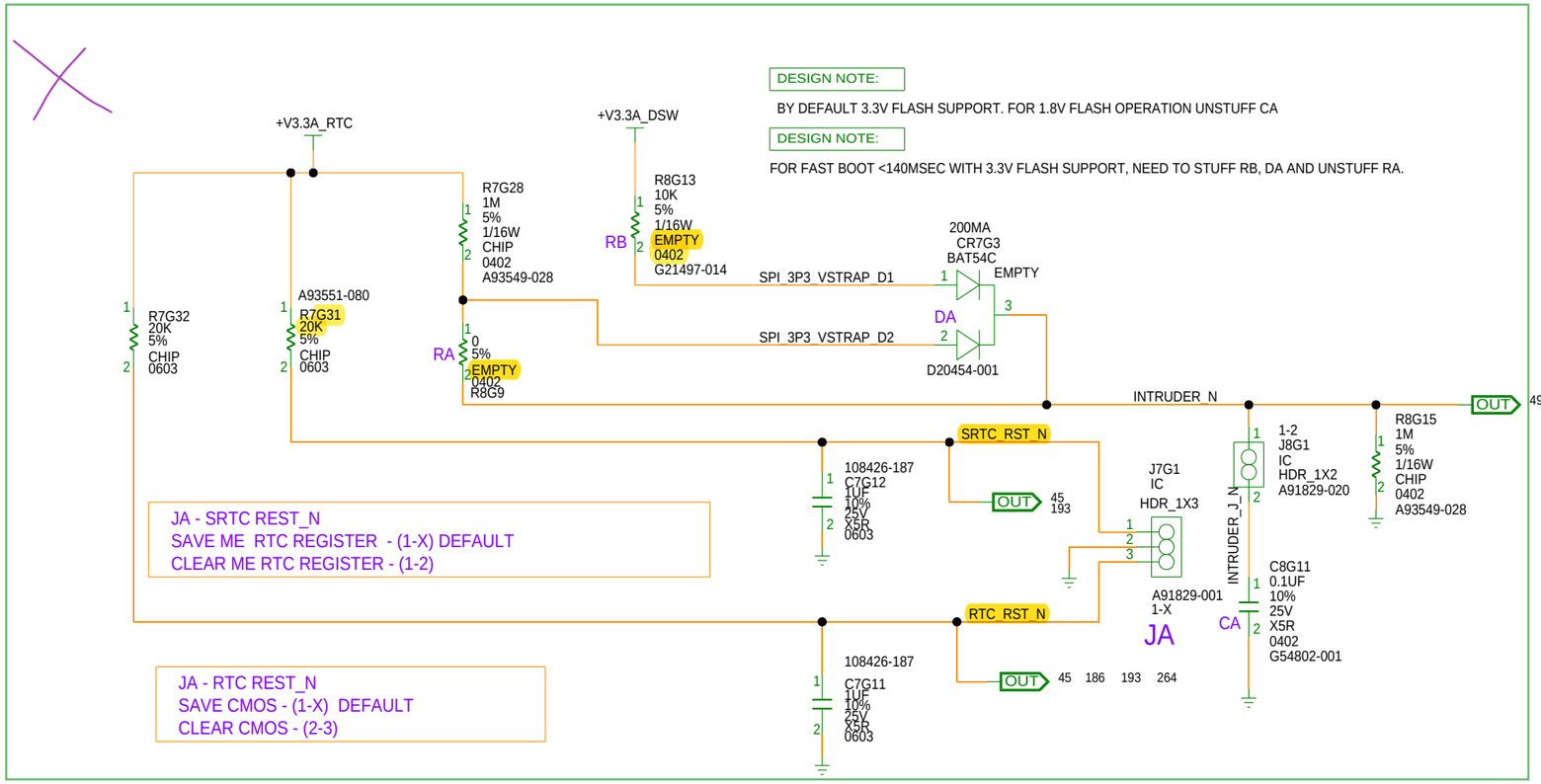
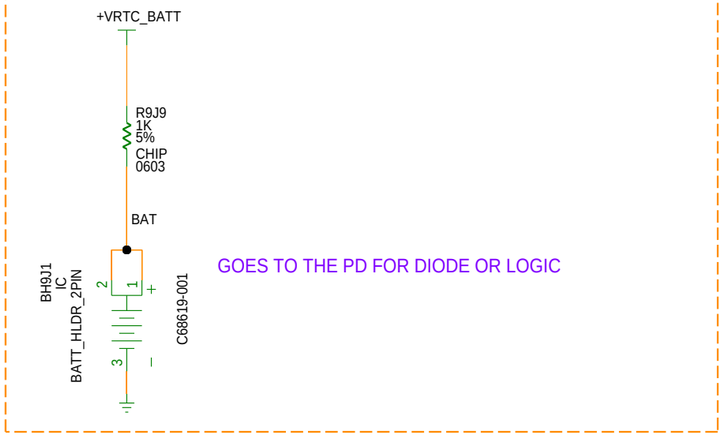
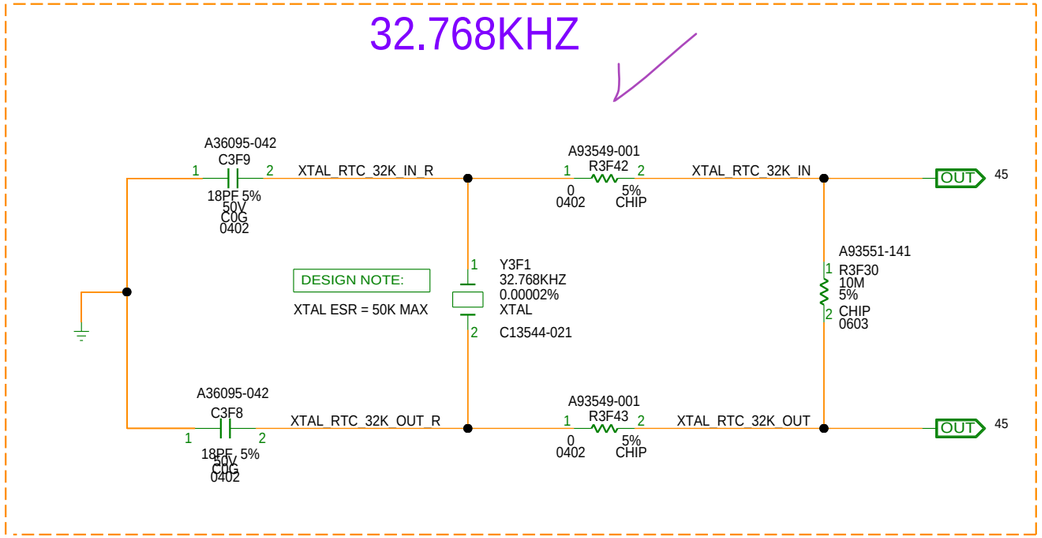


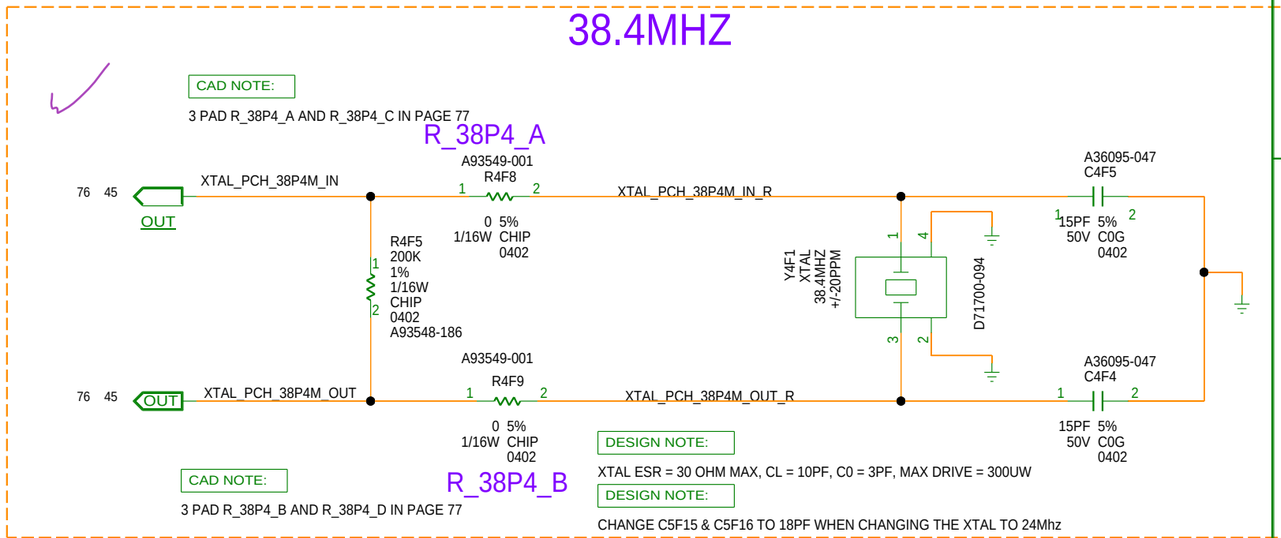
+V3.3A_RTC GENERATION



32.768KHZ



38.4MHZ



[PAGE_TITLE=CLOCK - CRYSTAL]

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tigerlake_u_ddr4.sch_1.47
Wed Dec 18 18:06:04 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

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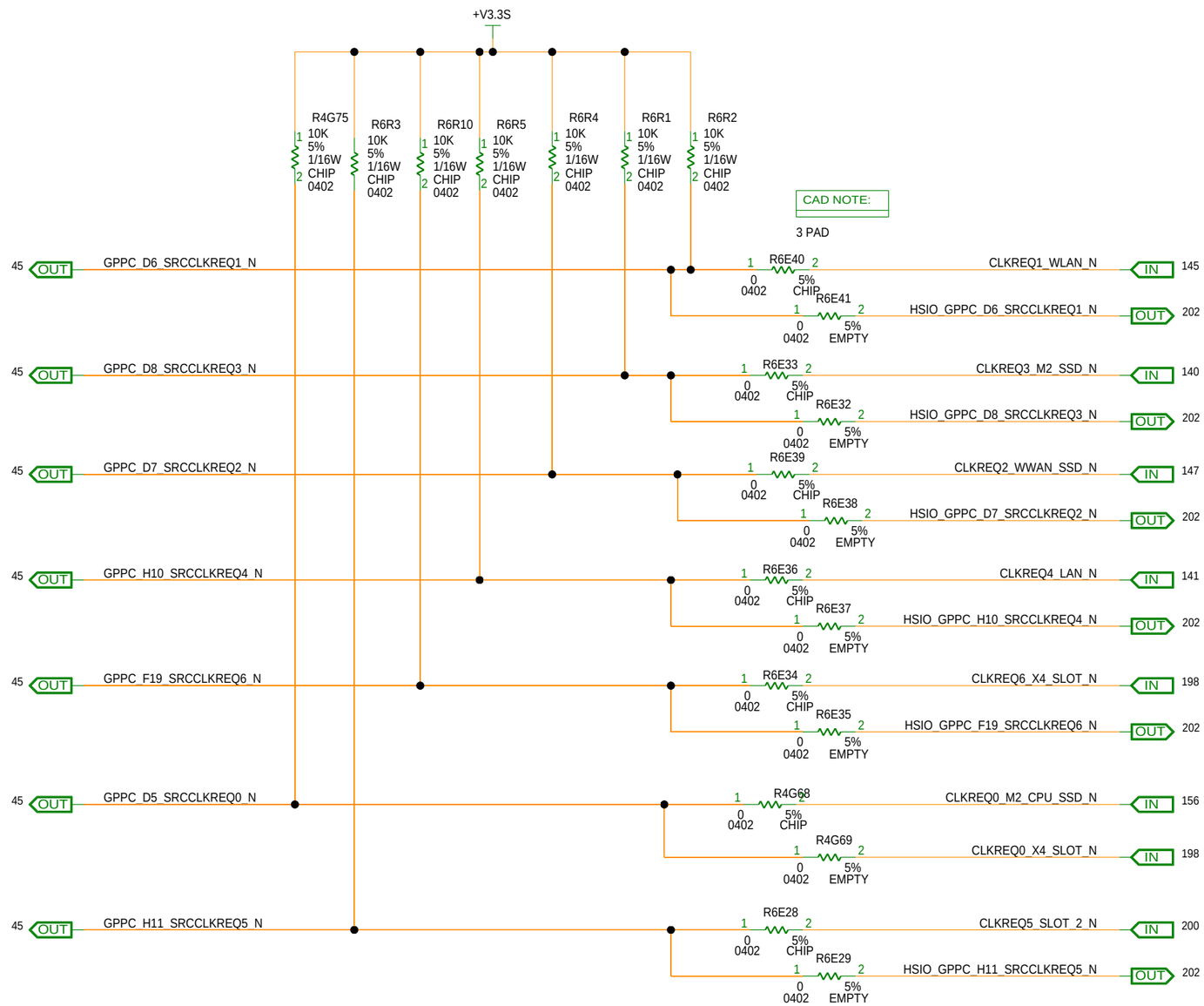

[PAGE_TITLE=SRC REQ MAPPING]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.48
Wed Dec 18 18:06:05 2019

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CUSTOM TEXT BPAGE

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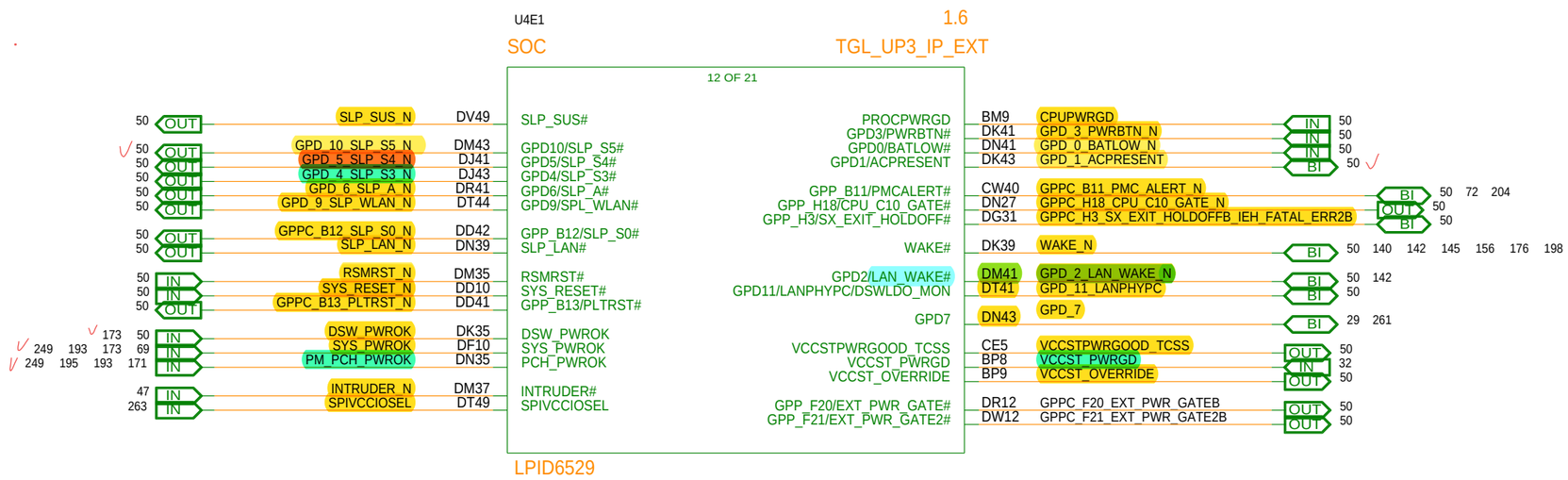


NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

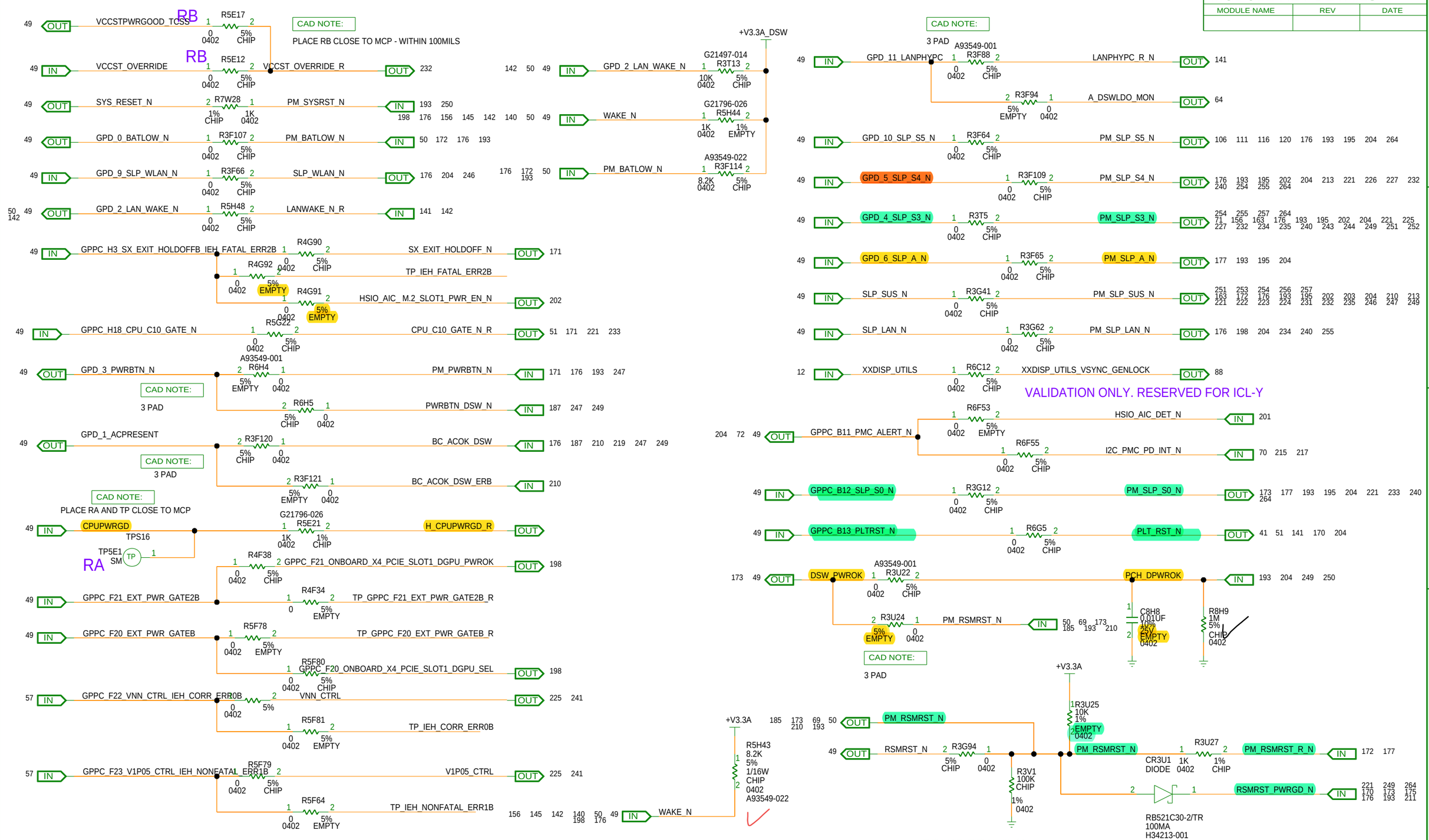
[PAGE_TITLE=TGL-U MCP (12 OF 21) - SYSTEM POWER MANAGEMENT]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.49
Mon Nov 04 11:10:31 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	49	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=SYATEM POWER MANAGEMENT OPTIONS]

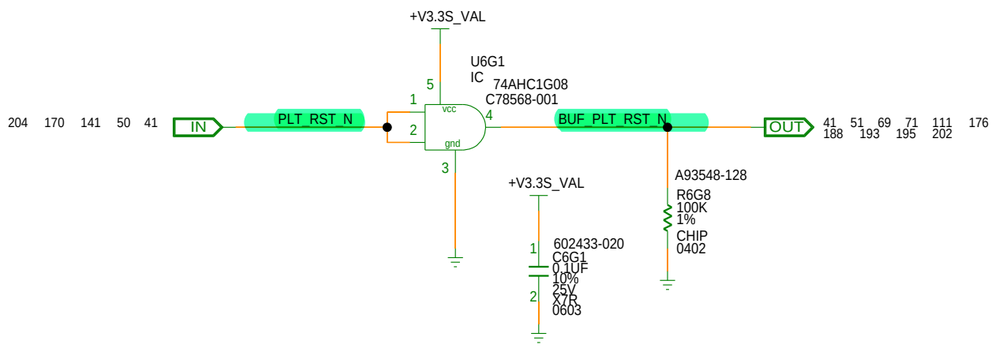
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.50
Wed Dec 18 18:06:07 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	50	1.0

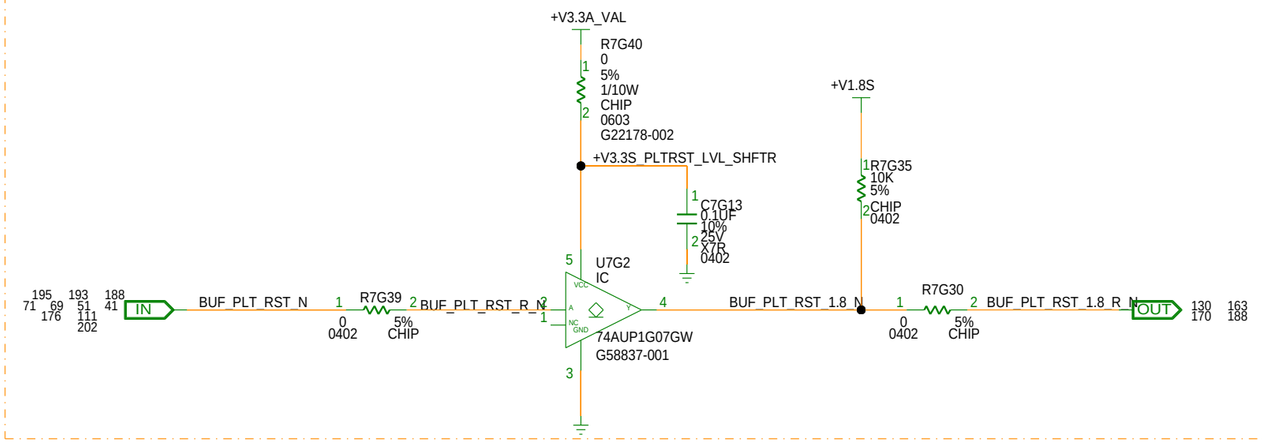
CUSTOM TEXT BPAGE

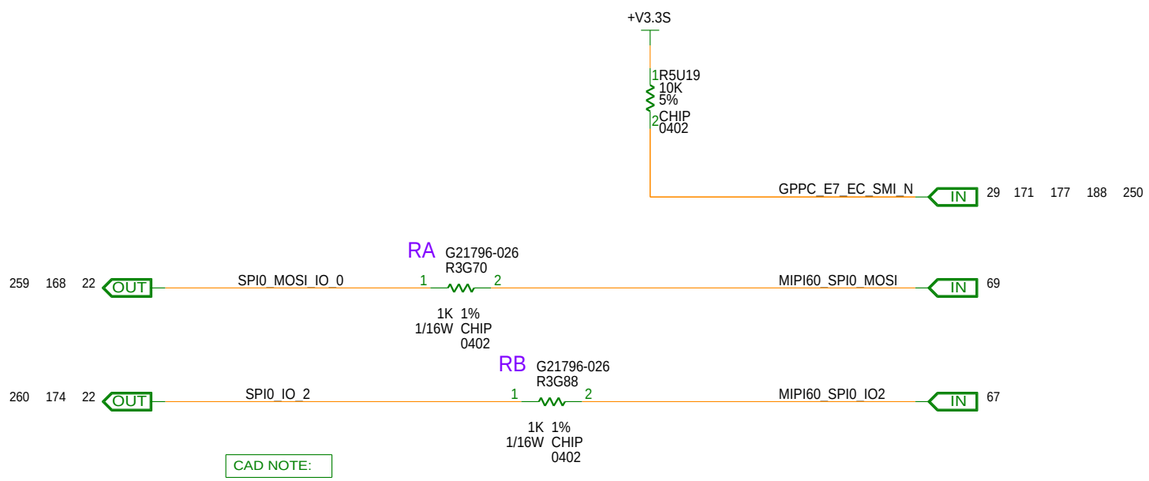
MODULE REV DETAILS		
MODULE NAME	REV	DATE

BUFFER TO REDUCE LOADING ON PLT_RST_N



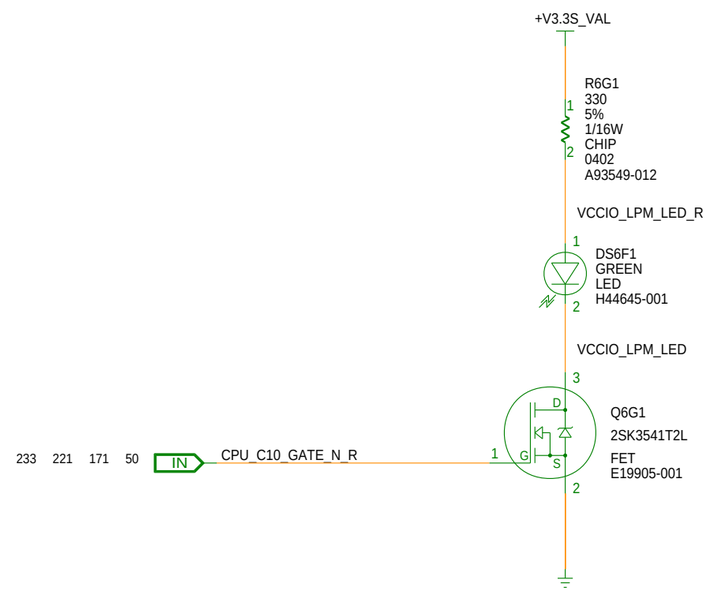
PLATFORM RESET LEVEL SHIFTER - 3.3V TO 1.8V





CAD NOTE:

RA AND RB RESISTORS NEED TO BE PLACED NEAR TO MCP, WITHOUT STUB ON SPI



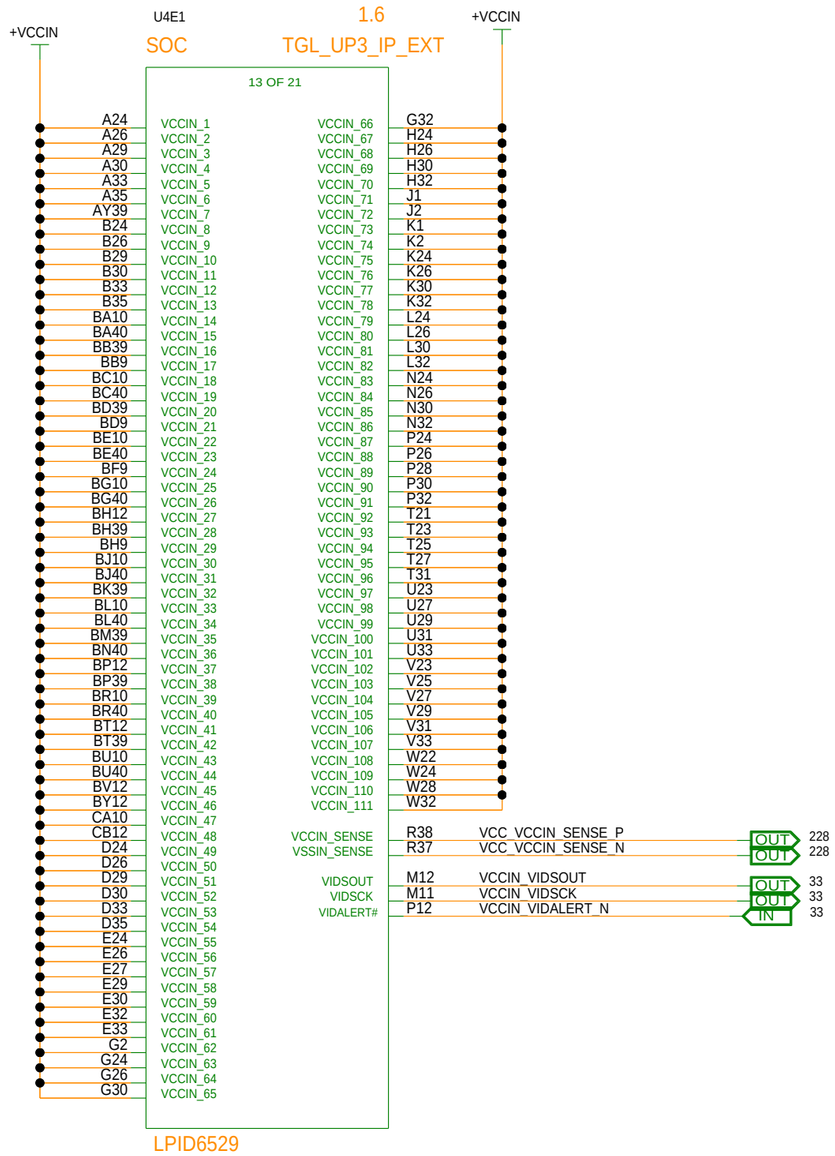
[PAGE_TITLE=PLATFORM RESET BUFFER]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.51
Wed Dec 18 18:06:08 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	51	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

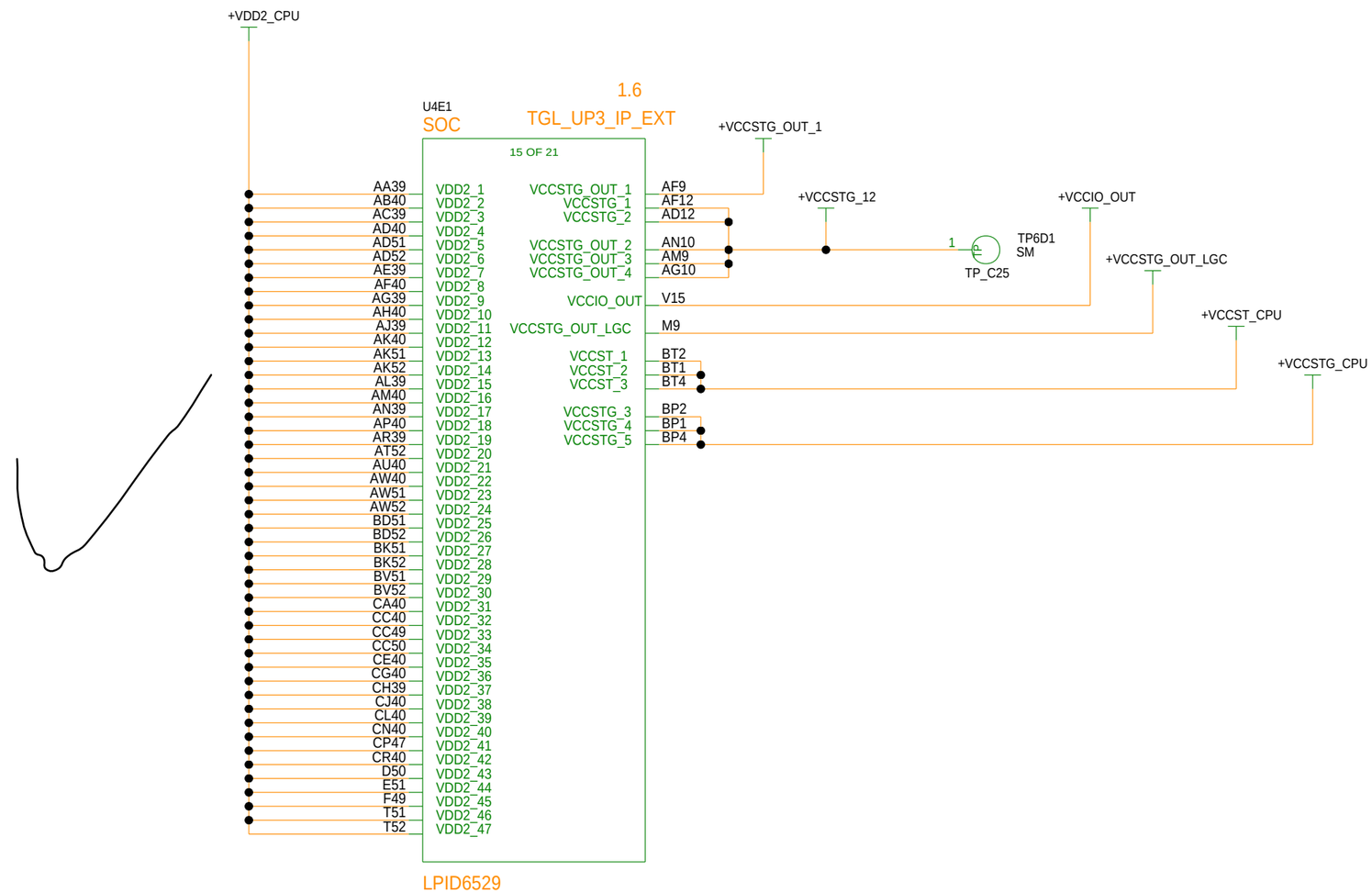
[PAGE_TITLE=TGL U MCP (13 OF 21) - CPU POWER 1 OF 2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.52
Wed Dec 18 18:06:09 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	52	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL-U MCP (15 OF 21) - CPU POWER 2 OF 2]

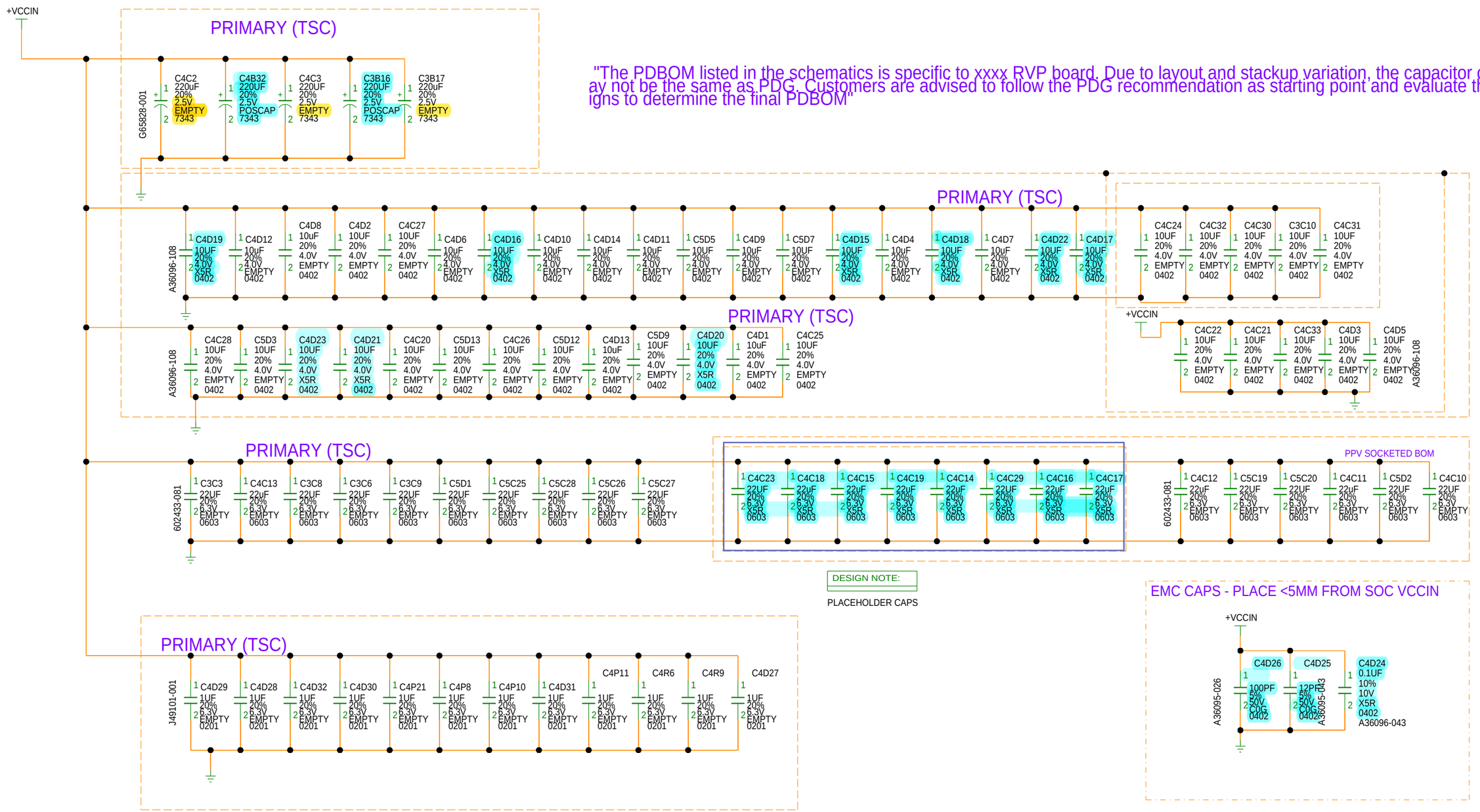
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.53
Wed Dec 18 18:42:47 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	53	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

C3B16,C3B17,C4B32,C4C2,C4C3

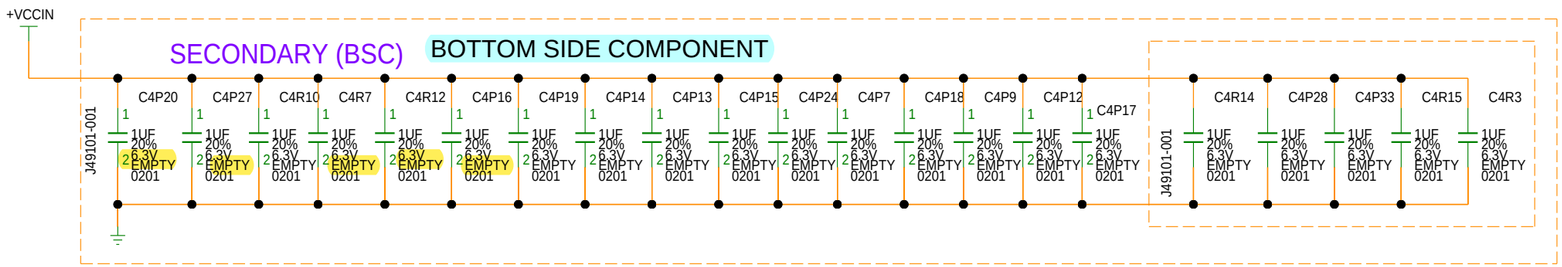


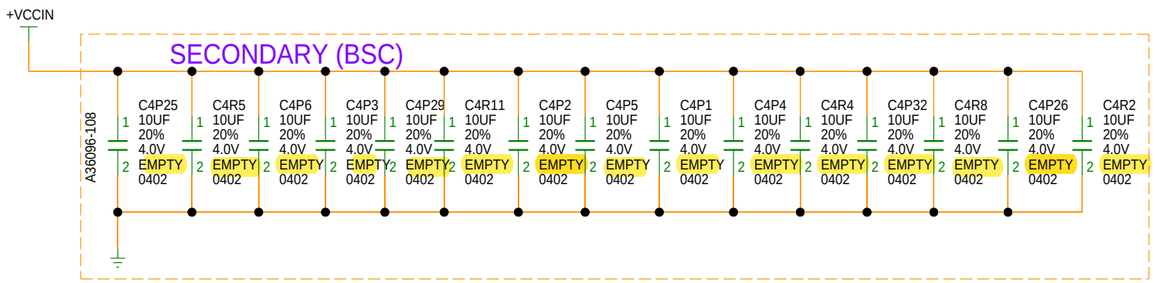
4P7,C4P8,C4P9,C4P10,C4P11,C4P12,C4P13,C4P14,C4P15,C4P16,C4P17,C4P18,C4P19,C4P20,C4P21,C4P22,C4P24,C4P27,C4P30,C4P33,C4R3,C4R6,C4R7,C4R9,C4R10,C4R12,C4R14,C4R15,VTP_1397,VTP_1552,VTP_1553

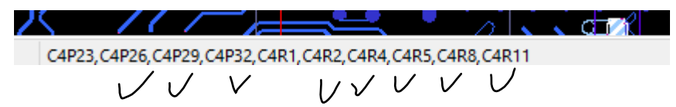
[PAGE_TITLE=CPU PDBOM 1 OF 2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.54
Wed Dec 18 18:06:12 2019

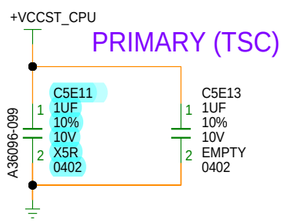
MODULE REV DETAILS		
MODULE NAME	REV	DATE





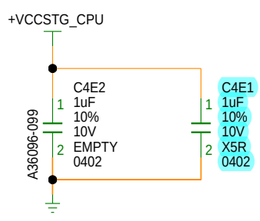


"The PDBOM listed in the schematics is specific to xxxx RVP board. Due to layout and stackup variation, the capacitor counts may not be the same as PDG. Customers are advised to follow the PDG recommendation as starting point and evaluate their own designs to determine the final PDBOM"

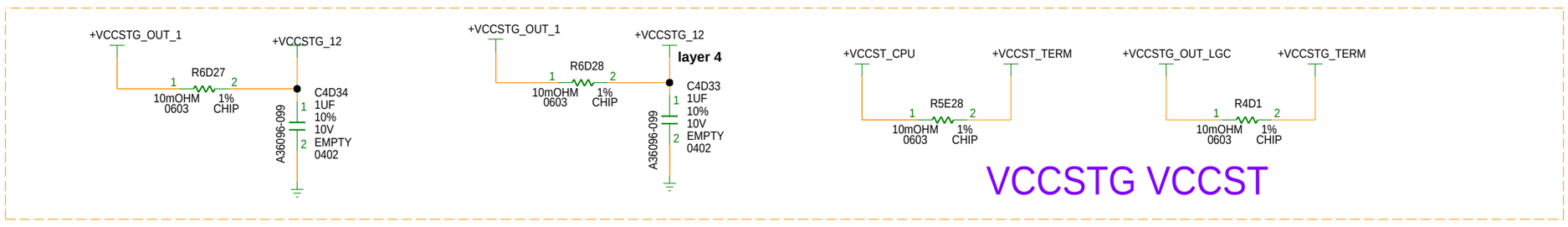


PLACE AS CLOSE AS POSSIBLE TO THE BGA PINS.
POWER ROUTING ON THE BOARD NEED TO BE ATLEAST ON >2 ROUTE LAYERS, PREFERABLY ON 4 LAYERS. FOLLOW GUIDELINES SHOWN IN BREAKOUT BOARD.
PMR OF 1MOHM NEED TO BE PLACED IN PARALLEL TO POWERGATE.
PG RDSON NEED TO BE <=5MOHM.

Ultra-low Ohmic Chip Resistors for Current Detection (PMR series)



PLACE AS CLOSE AS POSSIBLE TO THE BGA PINS.
POWER ROUTING ON THE BOARD NEED TO BE ATLEAST ON >2 ROUTE LAYERS, PREFERABLY ON 4 LAYERS. FOLLOW GUIDELINES SHOWN IN BREAKOUT BOARD.
PMR OF 1MOHM NEED TO BE PLACED IN PARALLEL TO POWERGATE.
PG RDSON NEED TO BE <=5MOHM.



[PAGE_TITLE=PCH PDBOM 2 OF 2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.55
Wed Dec 18 18:42:06 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	55	1.0

CUSTOM TEXT BPAGE

VDD2

MODULE REV DETAILS		
MODULE NAME	REV	DATE

+VDD2_CPU

CAD NOTE:
PLACE ON TOP SIDE

PRIMARY (TSC)

A36096-099: C3D1, C3D2, C3D3, C3E1, C3E2, C3E3, C3E4, C3E5, C3E7, C3P7, C3P13, C4P23, C3P18, C3R5, C3R7, C3R11
1uF 10% 10V X5R 0402 / 1uF 10% 10V EMPTY 0402

I put 10/16

PRIMARY (TSC)

A36096-108: C3P9, C3P17, C3P22, C3P10, C3P16, C3P23, C3R15, C3R14, C3R20, C3R17
10UF 20% 4.0V EMPTY 0402 / 10UF 20% 4.0V X5R 0402

A36096-108: C3R10, C3R9, C3R18, C3P24, C3R27, C3R26
10UF 20% 4.0V EMPTY 0402 / 10UF 20% 4.0V X5R 0402

I put 12/16

602433-109: C3E10, C3E9, C3E6, C3E8
47UF 20% 6.3V EMPTY 0603 / 47UF 20% 6.3V X5R 0603

PRIMARY (TSC)
PLACE NEAR BOARD PMIC

"The PDBOM listed in the schematics is specific to xxxx RVP board. Due to layout and stackup variation, the capacitor counts may not be the same as PDG. Customers are advised to follow the PDG recommendation as starting point and evaluate their own designs to determine the final PDBOM"

EMC CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART

+VDD2_CPU

A36094-015: C4R1 — 2.2PF 10% 50V COG 0402
A36095-043: C3P6 — 12PF 5% 50V COG 0402

+VDD2_CPU

C3P21 — 2.2PF 10% 50V COG 0402
C3P20 — 12PF 5% 50V COG 0402

+VDD2_CPU

C3R13 — 2.2PF 10% 50V COG 0402
C3R23 — 12PF 5% 50V COG 0402

SECONDARY (BSC)

C83410-025: C3P3, C3P12, C3P15, C3P8, C3R2, C4P30, C4R22, C3R6, C3R16, C3R21, C4R18, C4R25, C4P37, C3R3, C3R19, C3R8, C3R12, C3P14, C3P4, C3P2, C3R24
1uF 20% 10V EMPTY 0201 / 1uF 20% 10V X5R 0201

PRIMARY (TSC)

H68700-001: C3R29, C3R28, C3R25
22UF 20% 6.3V X5R 0603 / 22UF 20% 6.3V EMPTY 0603

+VDD2_CPU

SECONDARY (BSC)

J49101-001: C3R4, C4R13, C4P22, C3P19, C3R1, C3P5, C3P1, C3R22, C3P11, C4P34
1UF 20% 6.3V EMPTY 0201 / 1UF 20% 6.3V X5R 0201

C3R2,C3R3,C3R6,C3R16,C3R21,C3R22,C4P30,C4P33,C4P34,C4P37,C4R3,C4R13,C4R18,C4R22,C4R25

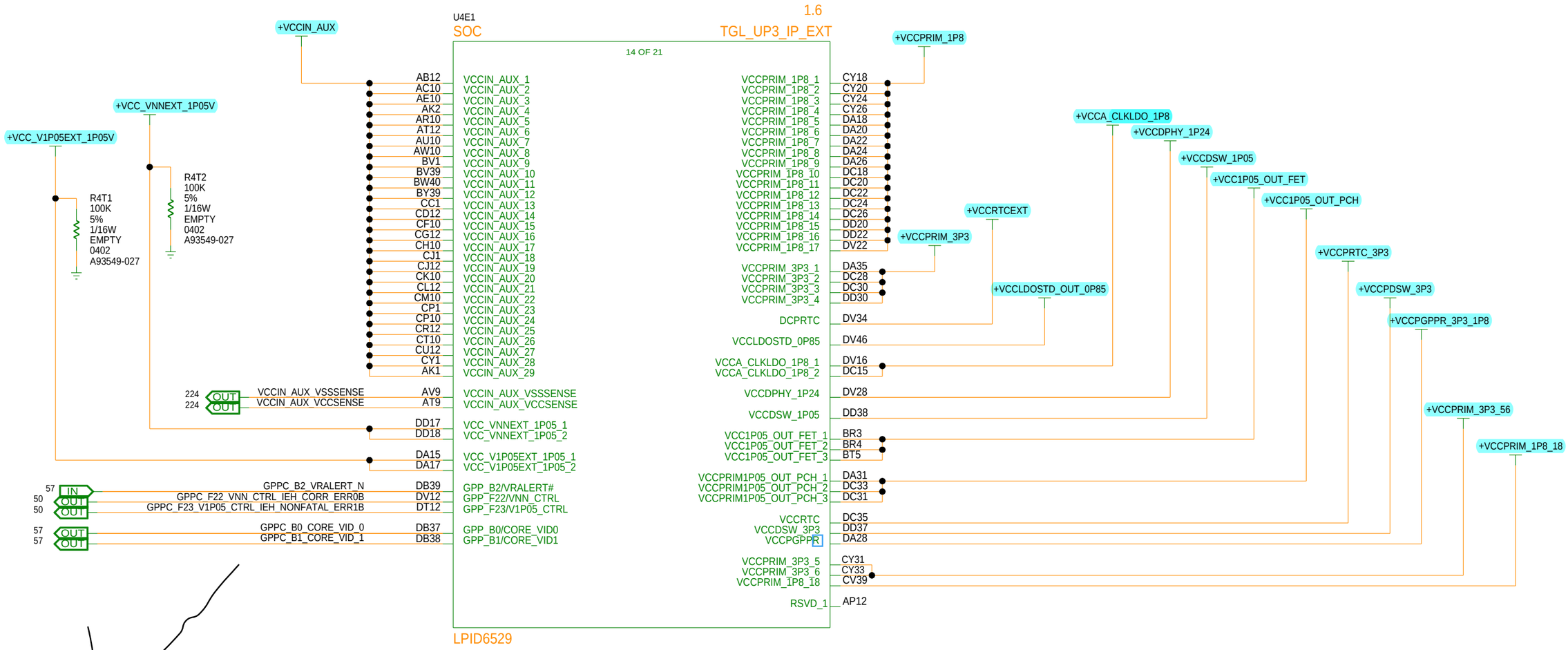
[PAGE_TITLE=CPU PDBOM 2 OF 2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.56
Wed Dec 18 18:06:14 2019

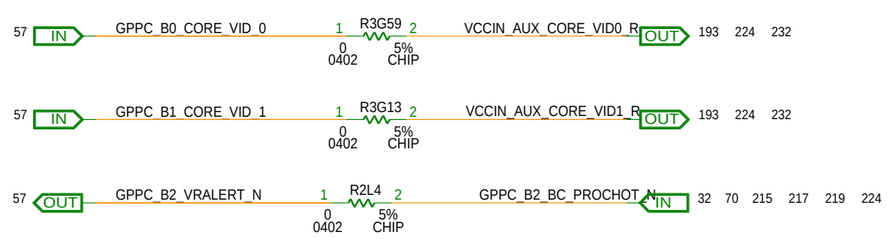
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	56	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates



[PAGE_TITLE=TGL-U MCP (14 OF 21)- PCH POWER 1 OF 2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.57
Wed Dec 18 18:26:15 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	57	1.0

CUSTOM TEXT BPAGE

VCCIN_AUX_1P8

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PRIMARY (TSC)

+VCCIN_AUX

SOLDERED DOWN BOM
MPI (ISC) SOCKETED BOM
PPV SOCKETED BOM

MPI (ISC) SOCKETED BOM
PPV SOCKETED BOM

CAD NOTE: PLACE TOP SIDE

G13063-001

C5F6 220uF 20% 6.3V EMPTY 7343
C5E21 220uF 20% 6.3V POSCAP 7343
C5E29 220UF 20% 6.3V EMPTY 7343
C5T5 220uF 20% 6.3V EMPTY 7343

PRIMARY (TSC)

CAD NOTE: PLACE TOP SIDE

A36096-108

C5E27 10UF 20% 4.0V EMPTY 0402
C5F7 10UF 20% 4.0V EMPTY 0402
C5F9 10UF 20% 4.0V EMPTY 0402
C4D35 10uF 20% 4.0V X5R 0402
C5E19 10uF 20% 4.0V X5R 0402
C4E7 10uF 20% 4.0V X5R 0402
C4E3 10uF 20% 4.0V X5R 0402
C5E16 10uF 20% 4.0V X5R 0402
C5E15 10uF 20% 4.0V X5R 0402
C5E35 10uF 20% 4.0V X5R 0402
C5F1 10UF 20% 4.0V EMPTY 0402
C5E20 10uF 20% 4.0V X5R 0402
C5E22 10uF 20% 4.0V X5R 0402
C5E23 10uF 20% 4.0V X5R 0402
C4D36 10UF 20% 4.0V X5R 0402
C5E37 10uF 20% 4.0V X5R 0402
C5F3 10UF 20% 4.0V EMPTY 0402
C5E30 10UF 20% 4.0V EMPTY 0402
C5F2 10UF 4.0V EMPTY 0402
C5F8 10UF 4.0V EMPTY 0402

SOLDERED DOWN BOM
MPI (ISC) SOCKETED BOM

C5E26 10UF 4.0V EMPTY 0402
C5E36 10uF 4.0V X5R 0402
C5E31 10UF 4.0V EMPTY 0402

PPV SOCKETED BOM

C5E14 10UF 4.0V X5R 0402
C5E32 10uF 4.0V X5R 0402
C5E28 10uF 4.0V X5R 0402
C5F10 10UF 4.0V EMPTY 0402
C5F13 10UF 4.0V EMPTY 0402

SECONDARY (BSC)

MPI (ISC) SOCKETED BOM PPV SOCKETED BOM

CAD NOTE: PLACE BOTTOM SIDE

A36096-108

C4P31 10uF 20% 4.0V X5R 0402
C5R5 10uF 20% 4.0V X5R 0402
C5R9 10uF 20% 4.0V X5R 0402
C5R11 10uF 20% 4.0V X5R 0402
C5R6 10uF 20% 4.0V X5R 0402
C4P35 10uF 20% 4.0V X5R 0402
C5R12 10uF 20% 4.0V X5R 0402
C5R3 10uF 4.0V X5R 0402
C5R4 10uF 4.0V X5R 0402
C5R10 10uF 4.0V X5R 0402

+VCCIN_AUX

SECONDARY (BSC)

MPI (ISC) SOCKETED BOM PPV SOCKETED BOM

J49101-001

C4R24 1UF 20% 6.3V EMPTY 0201
C4R26 1UF 20% 6.3V EMPTY 0201
C4R21 1UF 20% 6.3V EMPTY 0201
C4R23 1UF 20% 6.3V EMPTY 0201
C4R27 1UF 20% 6.3V EMPTY 0201
C4R17 1UF 20% 6.3V EMPTY 0201
C4R20 1UF 20% 6.3V EMPTY 0201
C4R16 1UF 20% 6.3V EMPTY 0201
C4R19 1UF 20% 6.3V EMPTY 0201
C4R28 1UF 20% 6.3V EMPTY 0201

PRIMARY (TSC)

MPI (ISC) SOCKETED BOM
PPV SOCKETED BOM
SOLDERED DOWN BOM

CAD NOTE: PLACE TOP SIDE

644066-115

C5E24 47uF 20% 6.3V X5R 0805
C5F4 47uF 20% 6.3V EMPTY 0805
C5F11 47uF 20% 6.3V EMPTY 0805
C5E33 47uF 20% 6.3V EMPTY 0805

644066-115

+VCCIN_AUX

C4P36 10UF 20% 4.0V X5R 0402 A36096-108

CAP ADDED FOR PI SIMULATION AS PER PI FEEBACK
PLACE CLOSE TO PIN AK1 of SoC

MPI (ISC) SOCKETED BOM
SOLDERED DOWN BOM
PPV SOCKETED BOM

602433-081

C5R13 22uF 20% 6.3V X5R 0603
C5R14 22uF 20% 6.3V X5R 0603
C5T1 22uF 20% 6.3V X5R 0603
C5T4 22uF 20% 6.3V EMPTY 0603
C5T7 22uF 20% 6.3V EMPTY 0603
C5T6 22uF 20% 6.3V EMPTY 0603

PPV SOCKETED BOM

C5R8 22uF 20% 6.3V X5R 0603
C5R7 22uF 20% 6.3V X5R 0603
C5T2 22uF 20% 6.3V EMPTY 0603
C5T3 22uF 20% 6.3V EMPTY 0603
C5R1 22uF 20% 6.3V X5R 0603
C5R2 22uF 20% 6.3V X5R 0603

C5F15 22uF 20% 6.3V X5R 0603
C5F5 22uF 20% 6.3V X5R 0603
C5E17 22uF 20% 6.3V X5R 0603
C5E34 22uF 20% 6.3V X5R 0603
C5F12 22uF 20% 6.3V X5R 0603
C5E25 22uF 20% 6.3V X5R 0603

EMC CAPS - PLACE <5MM FROM SOC VCCIN_AUX

+VCCIN_AUX

A36095-026 C4E5 100PF 5% 50V C0G 0402
A36095-043 C4E6 12PF 5% 50V C0G 0402
A36096-043 C4E4 0.1UF 10% 10V X5R 0402

CAD NOTE: PLACE BOTTOM SIDE

[PAGE_TITLE=PDBOM- VCCIN_AUX]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.58
Wed Dec 18 18:42:42 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	58	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

VCCRTCEXT MAY NOT BE REQUIRED AS THIS RAIL IS NOT THERE AS PER PI IPDG DOC

+VCCPRIM_1P8

CAD NOTE:
PLACE NEAR SOC

C4F1
1UF
10%
10V
EMPTY
0402
A36096-099

+VCCRTCEXT

C4F3
0.1UF
10%
10V
X5R
0402
A36096-043

CAD NOTE:
PLACE NEAR BGA

supply

+VCCA_CLKLDO_1P8_R

J65894-001
L4F1
0.68UH 30%
EMPTY
LPDDR
GENERIC
R4F56
10mOHM 1%
0603 CHIP

CPU

+VCCA_CLKLDO_1P8

VCCA_CLKLDO_RC

R4F29
0.1
1%
1/8W
CHIP
0402
G58224-001

C4F7
47UF
20%
6.3V
X5R
0603
602433-109

+VCCPRIM_3P3

CAD NOTE:
PLACE CAP CLOSEST POSSIBLE TO THE BGA

C4F11
1UF
10%
10V
EMPTY
0402
A36096-099

C4F10
0.1UF
10%
10V
EMPTY
0402
A36096-043

+VCCPDSW_3P3

CAD NOTE:
PLACE CAP CLOSEST POSSIBLE TO THE BGA

C4F6
1UF
10%
10V
EMPTY
0402
A36096-099

+VCCPRTC_3P3

CAD NOTE:
PLACE CAP CLOSEST POSSIBLE TO THE BGA

C4R29
1UF
10%
10V
X5R
0402
A36096-099

C4T1
0.1UF
10%
10V
X5R
0402
A36096-043

+VCCDSW_1P05

TP_C20
TP3G1
SM

CAD NOTE:
PLACE CAP CLOSEST POSSIBLE TO THE BGA.

C3R30
1UF
10%
10V
X5R
0402
A36096-099

+VCCLDOSTD_OUT_0P85

TP_C20
TP3T1
SM

C3F3
2.2UF
20%
6.3V
X5R
0402
A36096-088

CAD NOTE:
PLACE CAP CLOSEST POSSIBLE TO THE BGA WITHIN 3MM FROM PACKAGE

+VCCDPHY_1P24

C4F2
4.7UF
20%
6.3V
X5R
0402
A36096-107

CAD NOTE:
PLACE NEAR BGA WITHIN 3MM FROM PACKAGE

+VCC_VNNEXT_1P05V

C4R30
1UF
10%
10V
EMPTY
0402
A36096-099

CAD NOTE:
PLACE CAP CLOSEST POSSIBLE TO THE BGA.

+VCC_V1P05EXT_1P05V

C4T2
1UF
10%
10V
EMPTY
0402
A36096-099

CAD NOTE:
PLACE CAP CLOSEST POSSIBLE TO THE BGA.

[PAGE_TITLE=PCH PDBOM 1 OF 2]

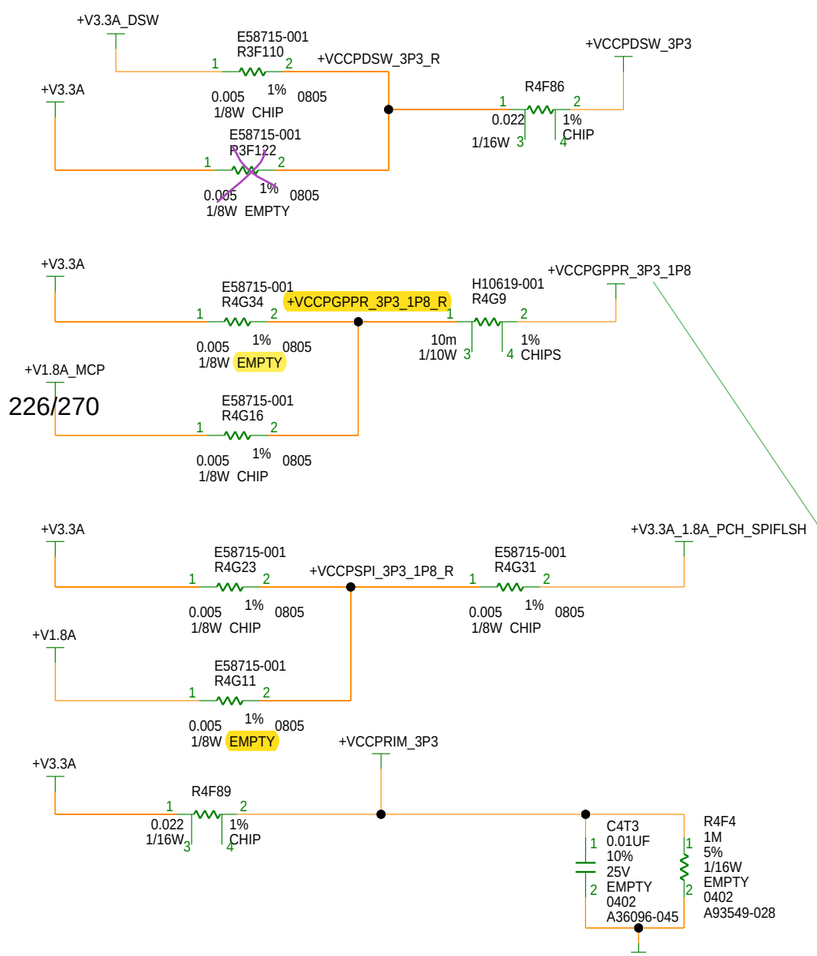
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.59
Wed Dec 18 18:06:17 2019

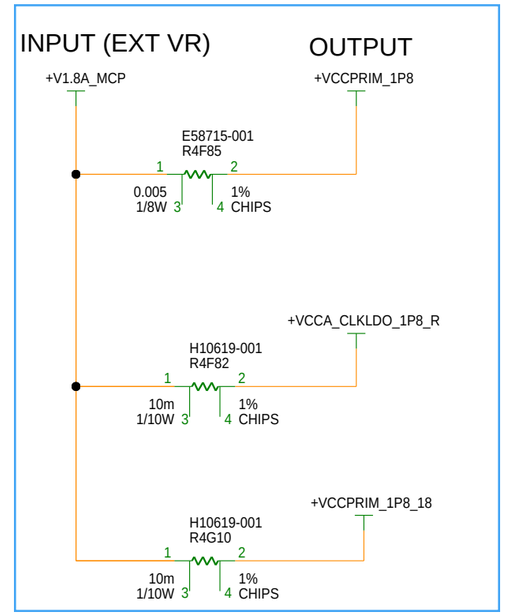
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	59	1.0

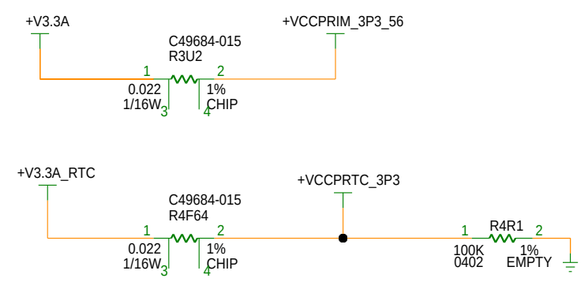
CUSTOM TEXT BPAGE

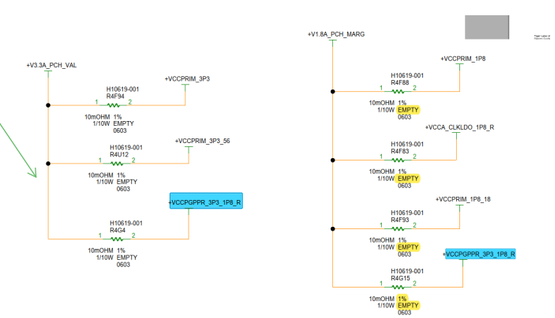
MODULE REV DETAILS		
MODULE NAME	REV	DATE

PCH DERIVED RAILS









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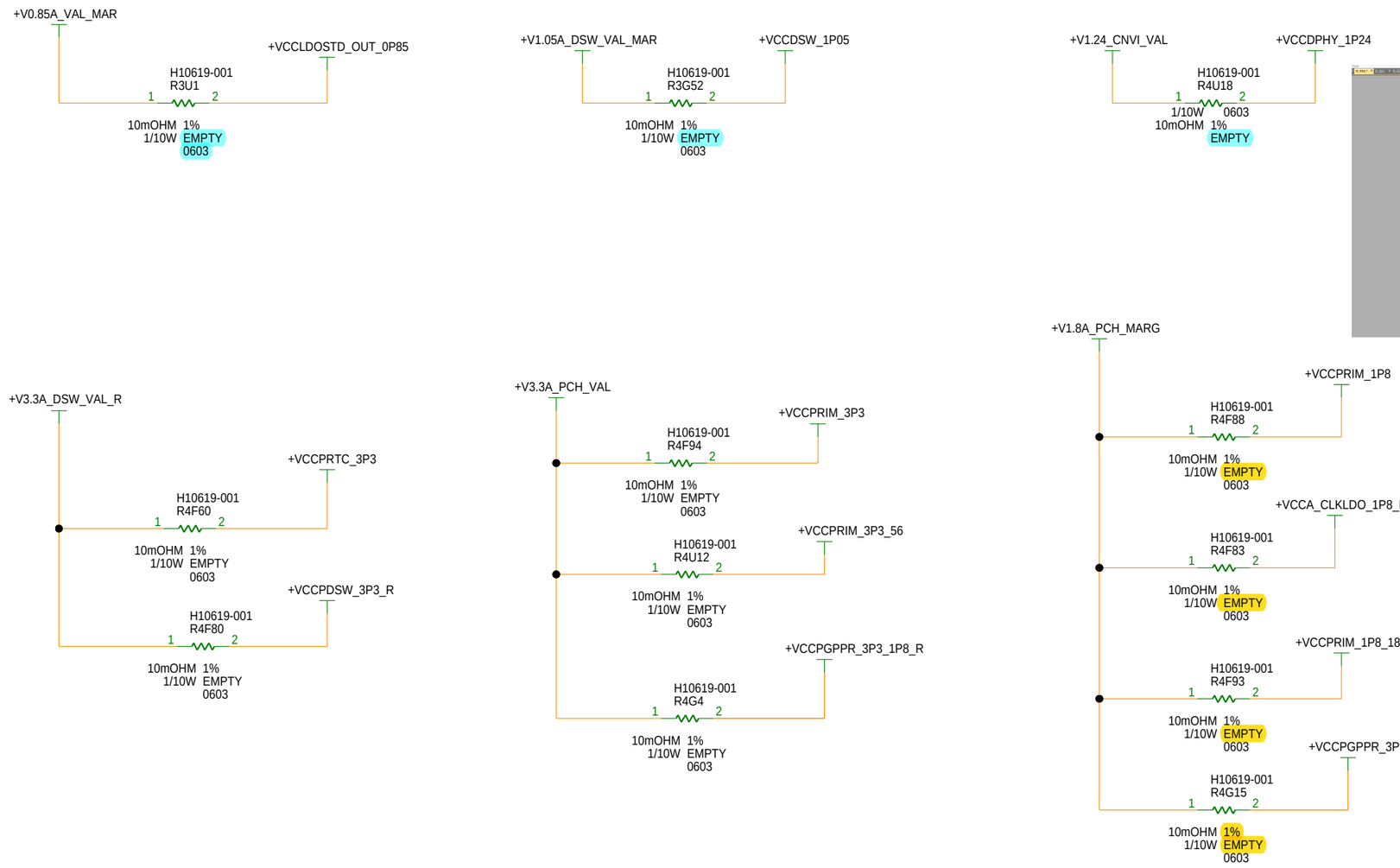
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.60
Wed Dec 18 18:42:38 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	60	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PCH MARGINING RAILS



S02.0	Always Enable					
S02.1	Always Enable					
S02.2	-	-	NO	-	-	YES
S03.0	Always Enable					
S03.1	Always Enable					
S03.2	NO	NO	-	-	-	-
S03.3	-	-	NO	-	-	YES

Table 237. No Direct Switching or No External Bypass Supported

State Enable	Q1 CNVi	Q2 ISH	Q3 Type A	Q4 C-Link	Q5 SMBus	Q6 PHY PG
S02.0	Always Enable					
S02.1	Always Enable					
S02.2	-	-	NO	-	-	YES
S03.0	NO	NO	-	-	-	-
S03.1	NO	NO	-	-	-	-
S03.2	NO	NO	-	-	-	-
S03.3	NO	NO	NO	-	-	YES

Voltage Margining

Voltage margining allows bypass VRs to reduce their voltages depending on S0i3.x states. To enable this feature, VNN_CTRL and V1P05_CTRL GPIO pins should be configured. This feature can reduce power in S0ix states.

Tiger Lake UP3 UP4 H35 UP3 Refresh Platform
Design Guide

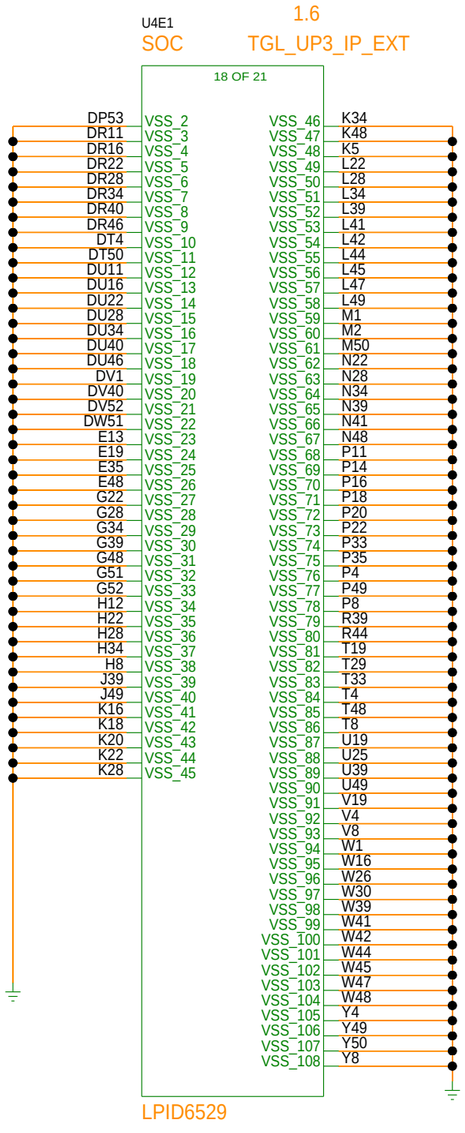
[PAGE_TITLE=PCH MARGINING RAILS]

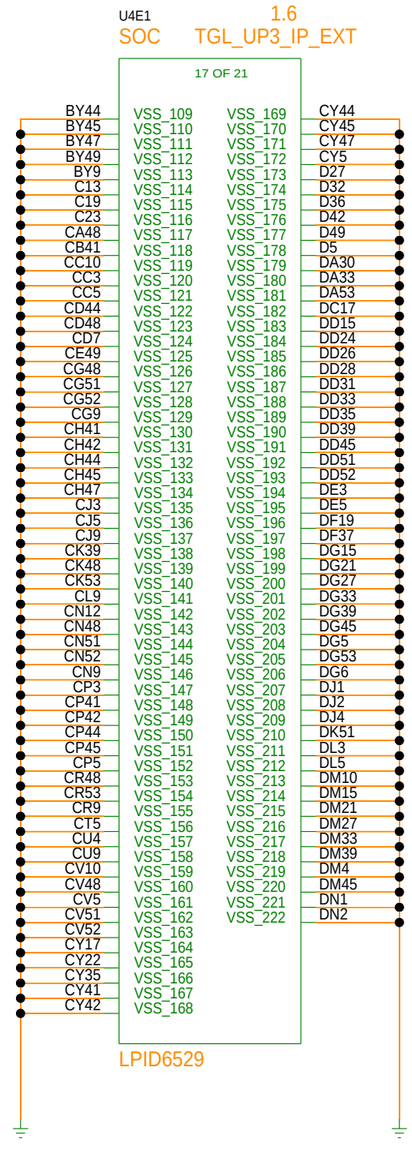
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.61
Wed Dec 18 18:06:19 2019

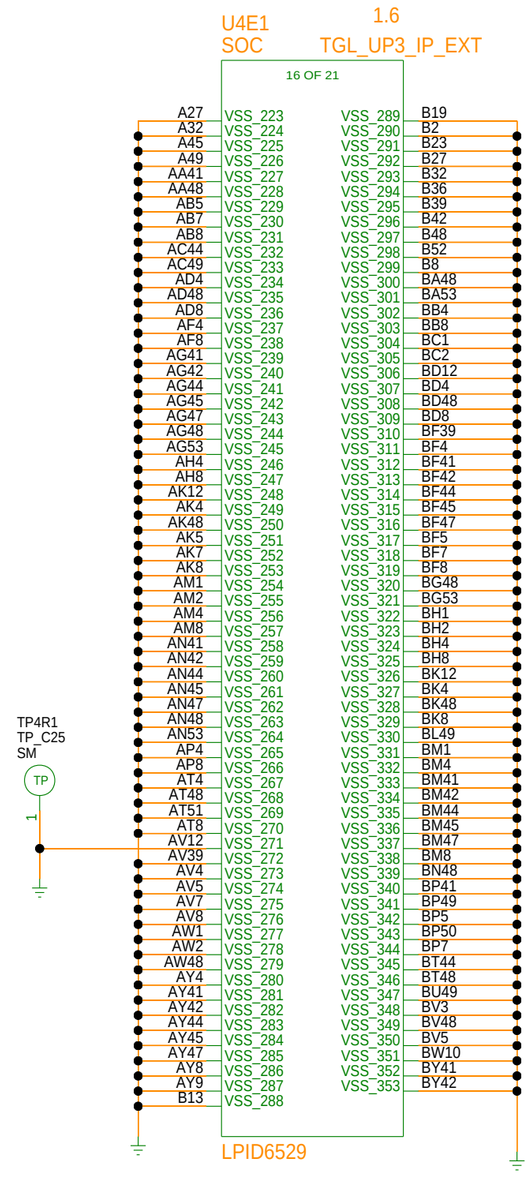
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	61	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE







NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

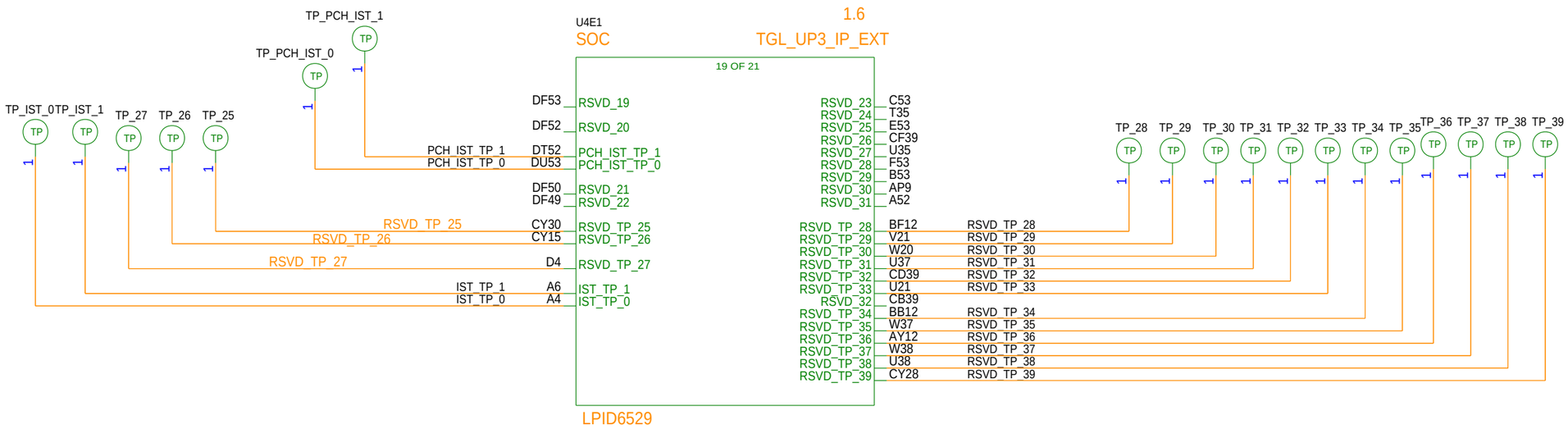
[PAGE_TITLE=TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.62
Wed Dec 18 18:06:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	62	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

NOTE:
RECOMENDED TO CONNECT PHYSICAL /VIA TEST POINTS FOR RSVD_TP PINS.

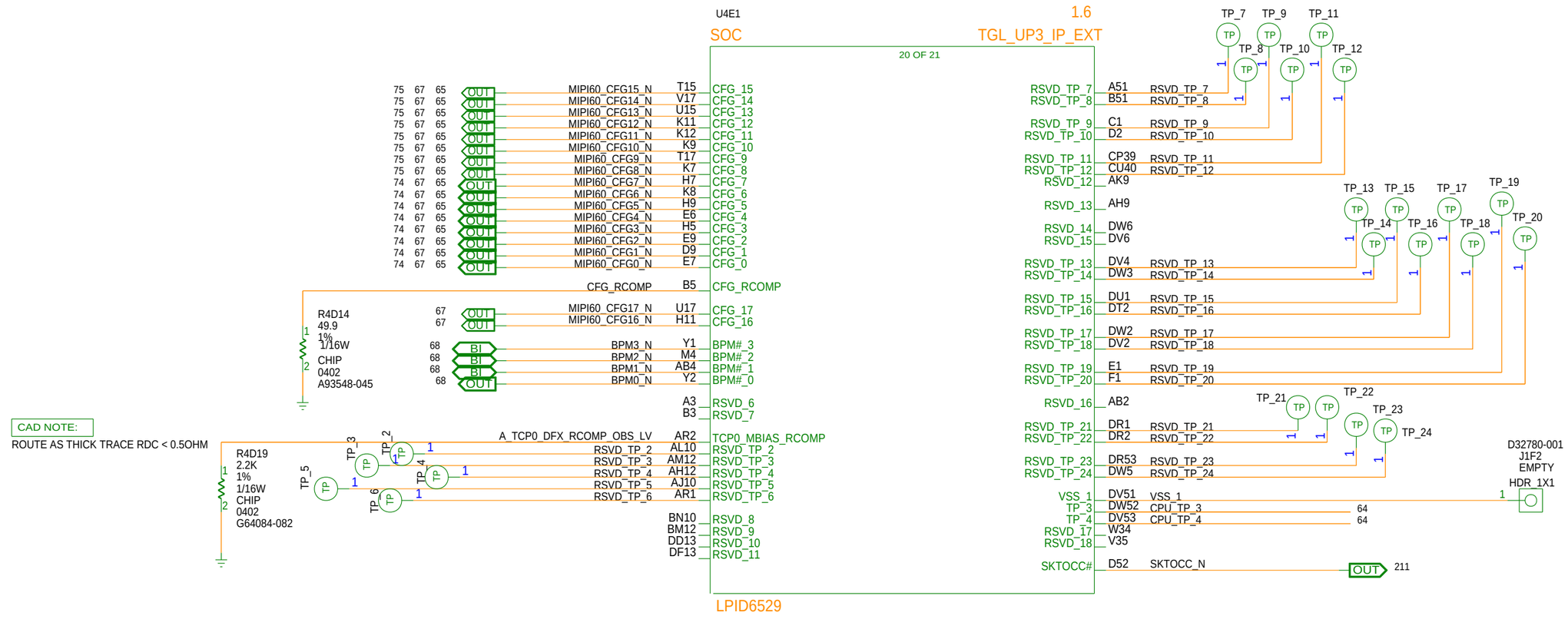
[PAGE_TITLE=TGL-U MCP (19 OF 21) - FIVR DEBUG]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.63
Wed Dec 18 15:48:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	63	1.0

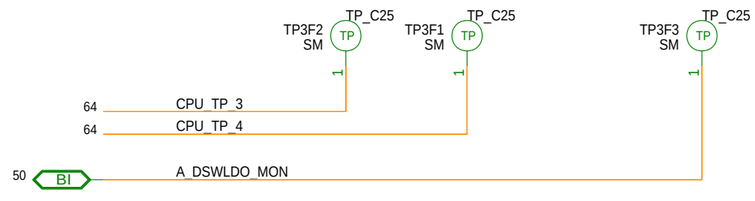
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

NOTE:
RECOMENDED TO CONNECT PHYSICAL /VIA TEST POINTS FOR RSVD_TP PINS.



[PAGE_TITLE=TGL-U MCP (20 OF 21) - RESERVED SIGNALS]

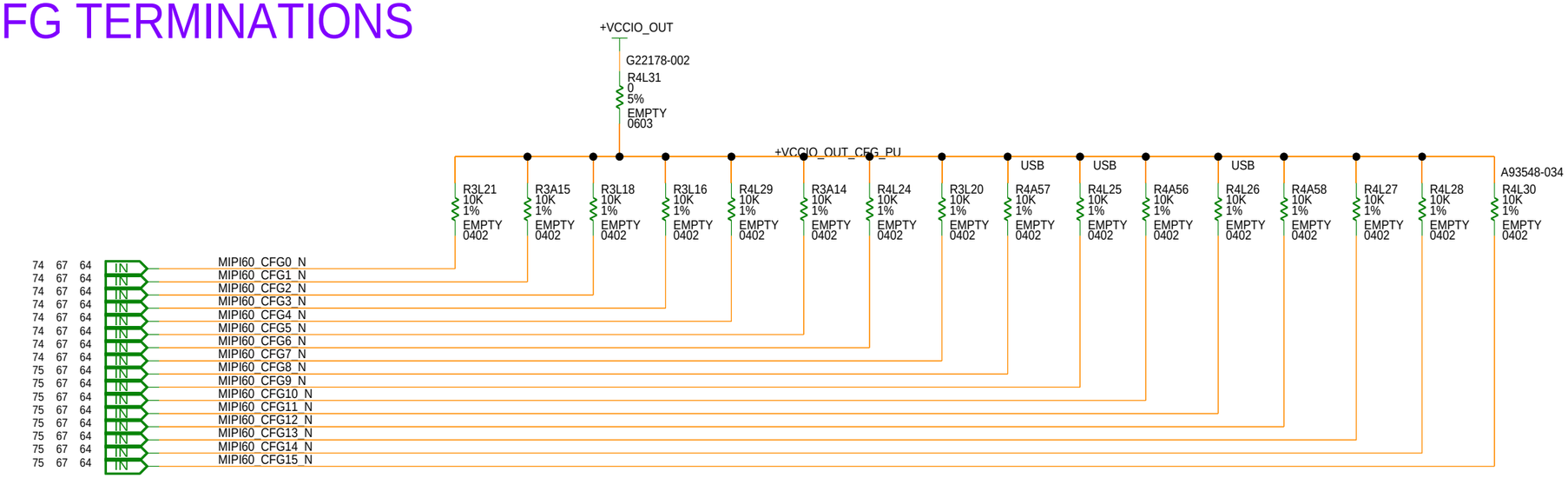
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.64
Wed Dec 18 18:06:22 2019

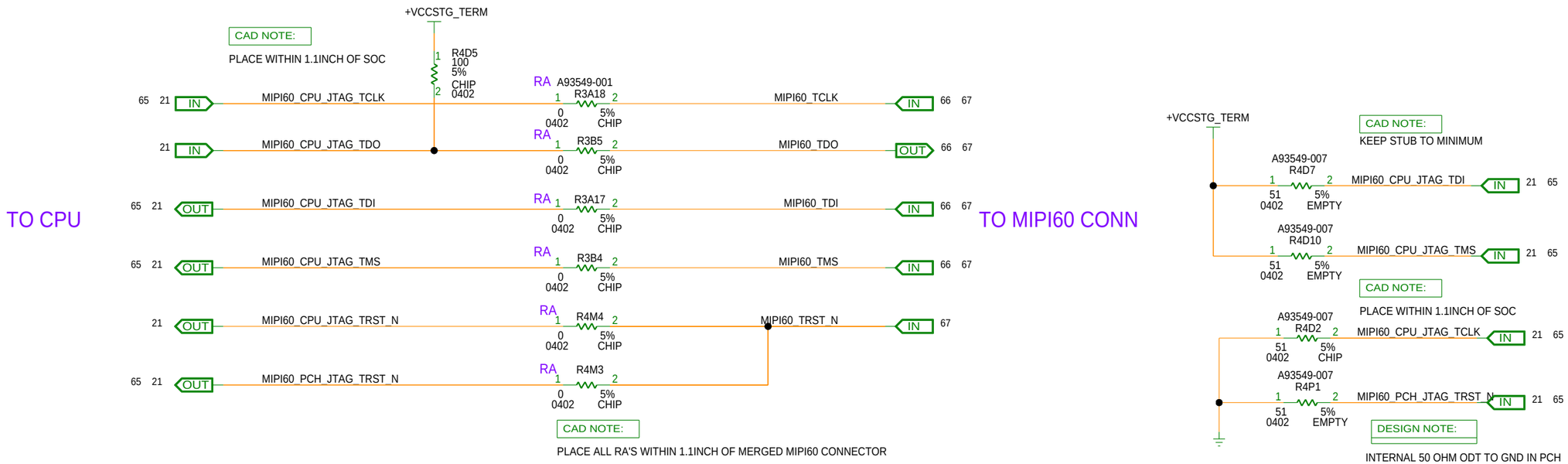
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	64	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CFG TERMINATIONS





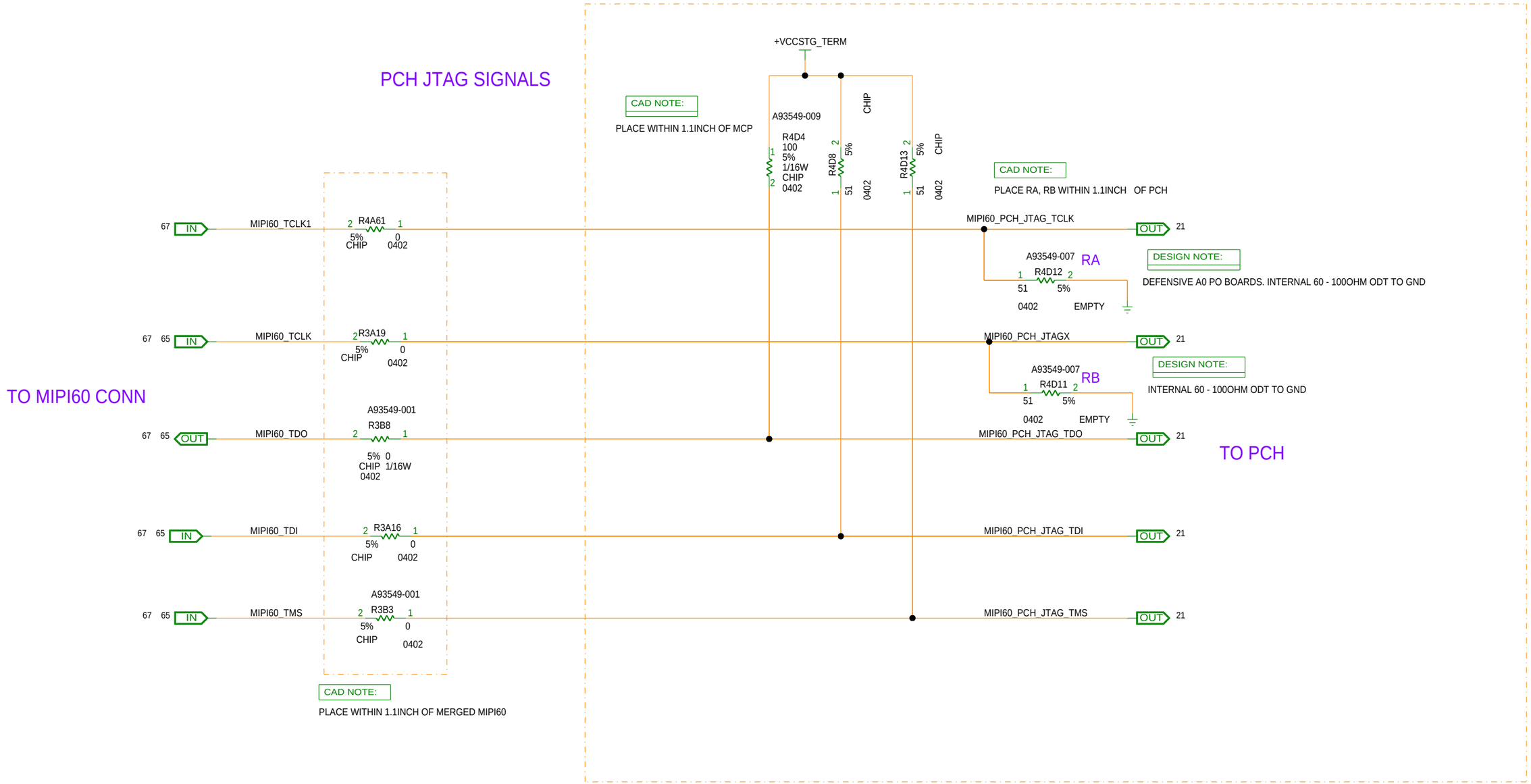
[PAGE_TITLE=JTAG/CFG - CFG TERMINATIONS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.65
Wed Dec 18 18:06:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	65	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=JTAG/CFG - MERGED JTAG OPTIONS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.66
Wed Dec 18 18:06:24 2019

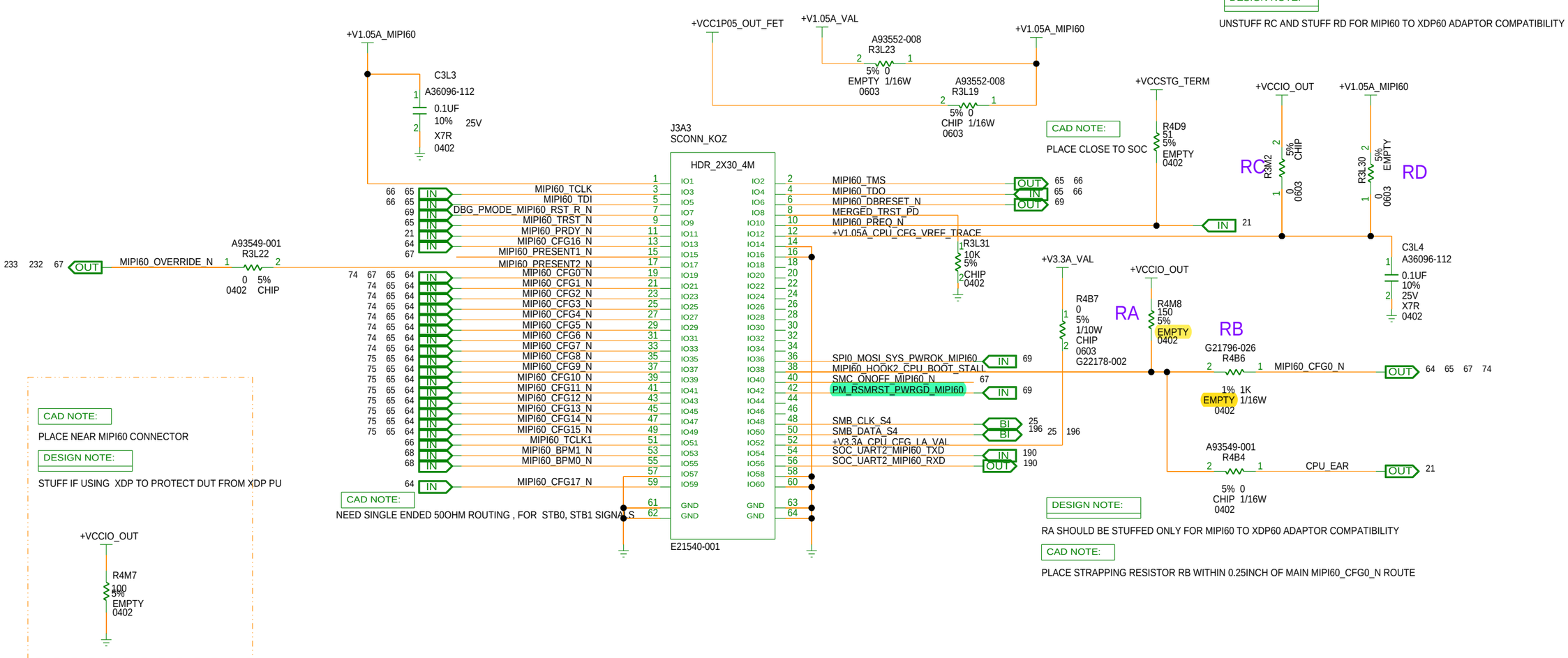
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	66	1.0

CUSTOM TEXT BPAGE

MIPI 60

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:
UNSTUFF RC AND STUFF RD FOR MIPI60 TO XDP60 ADAPTOR COMPATIBILITY



CAD NOTE:
PLACE CLOSE TO SOC

CAD NOTE:
NEED SINGLE ENDED 50OHM ROUTING , FOR STB0, STB1 SIGNALS

DESIGN NOTE:
RA SHOULD BE STUFFED ONLY FOR MIPI60 TO XDP60 ADAPTOR COMPATIBILITY

CAD NOTE:
PLACE STRAPPING RESISTOR RB WITHIN 0.25INCH OF MAIN MIPI60_CFG0_N ROUTE

CAD NOTE:
PLACE NEAR MIPI60 CONNECTOR

DESIGN NOTE:
STUFF IF USING XDP TO PROTECT DUT FROM XDP PU

CAD NOTE:
PLACE NEAR MIPI60 CONNECTOR

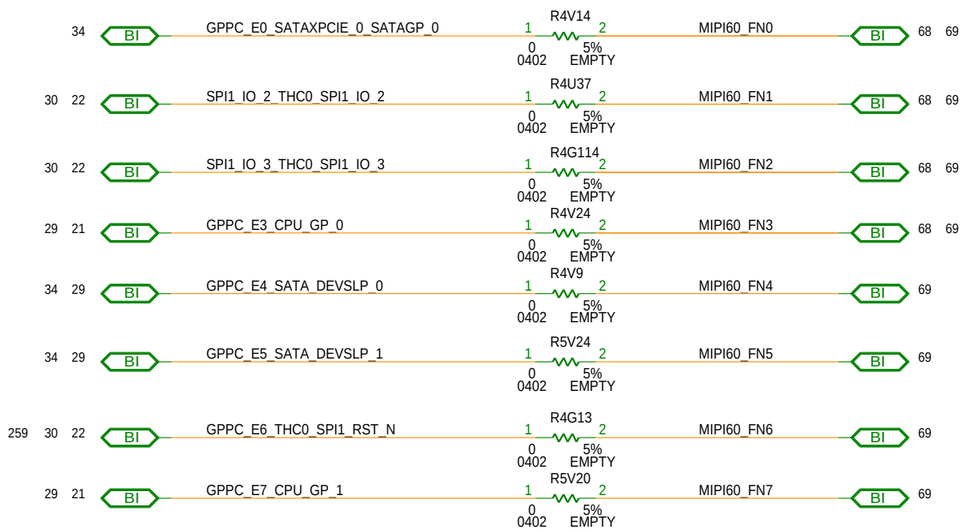
[PAGE_TITLE=JTAG/CFG - CPU/PCH MERGED MIPI 60 CONNECTOR]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.67
Wed Dec 18 18:06:25 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	67	1.0

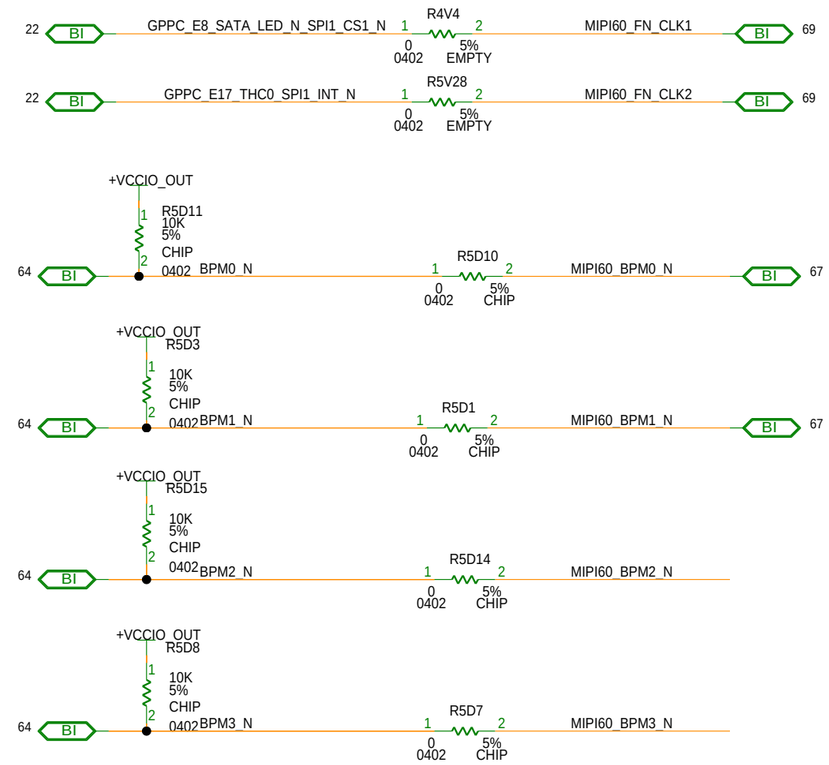
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

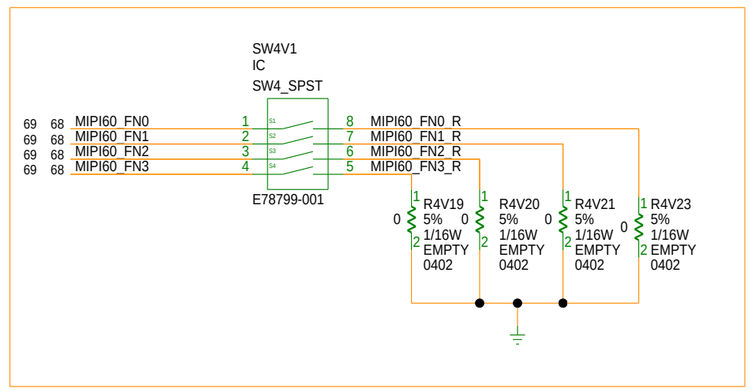


GENERAL CAD NOTE: USE 3 PAD OR 4 PAD SHARING WITH THE RESPECTIVE RESISTORS

CAD NOTE: IN PCH GPIO GENERATION PAGES



Recommended to have TP for BPM2/3,if required



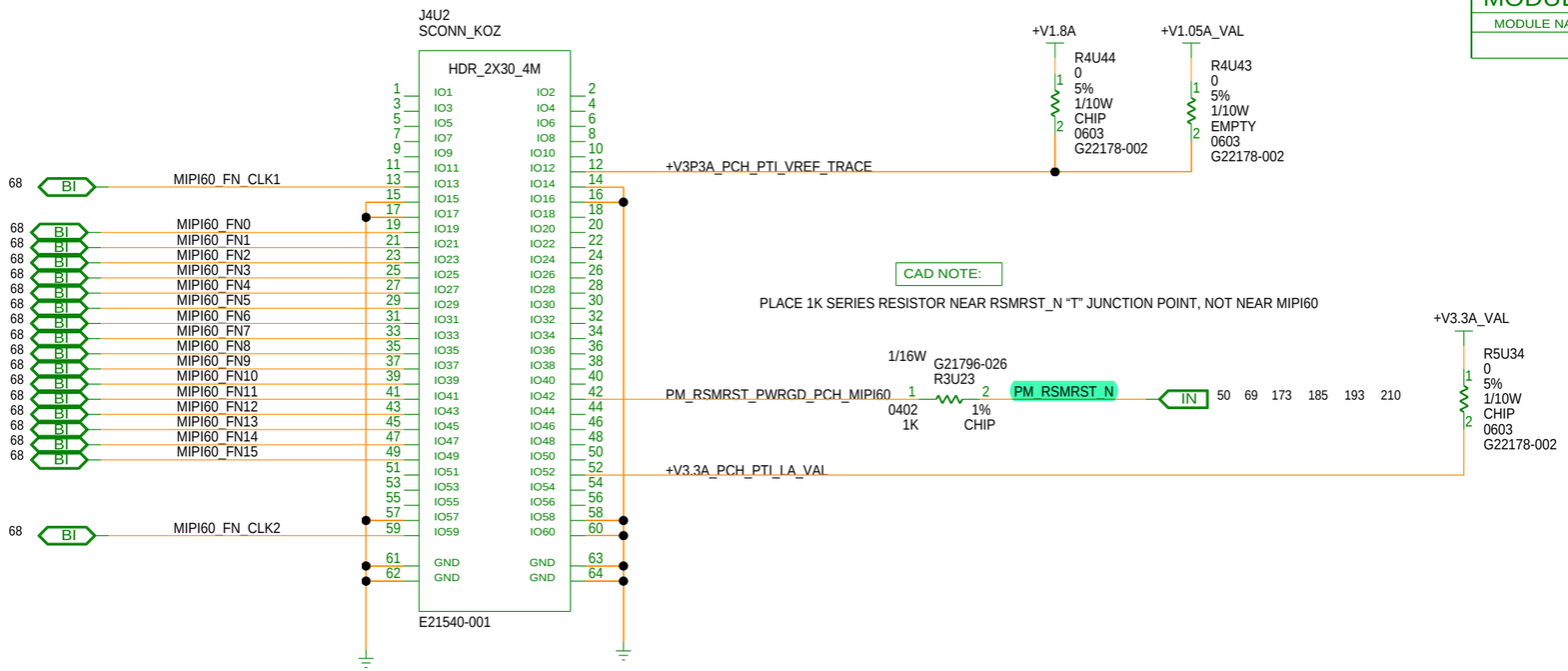
[PAGE_TITLE=JTAG/CFG - PCH DEBUG SHARING OPTIONS]

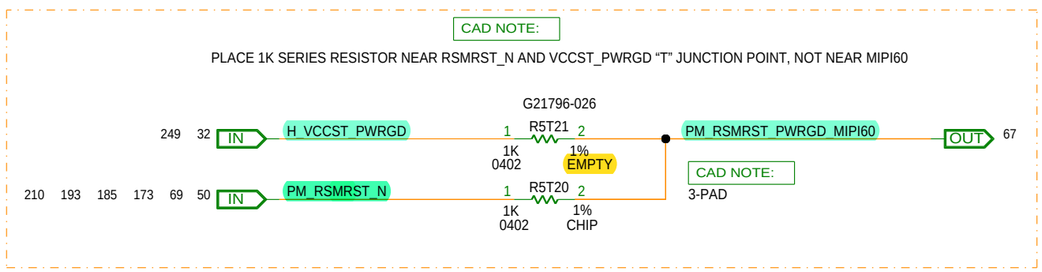
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.68
Thu Dec 26 15:55:35 2019

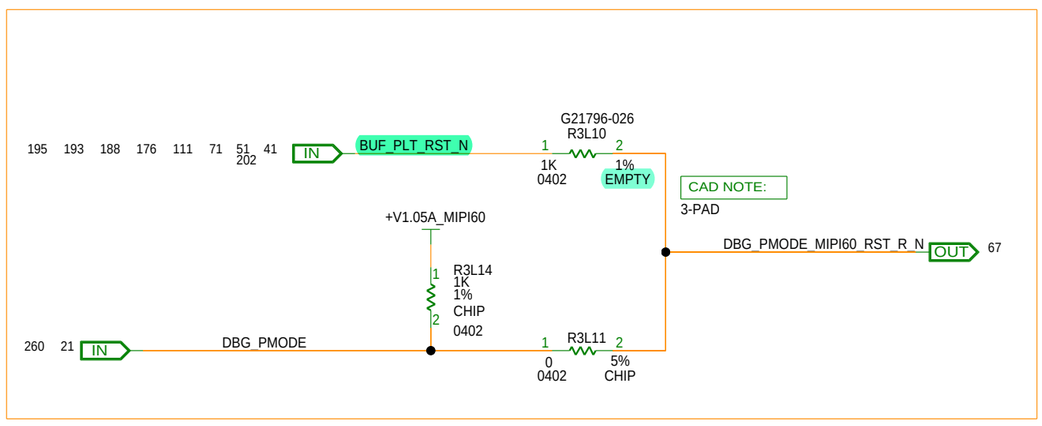
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	68	1.0

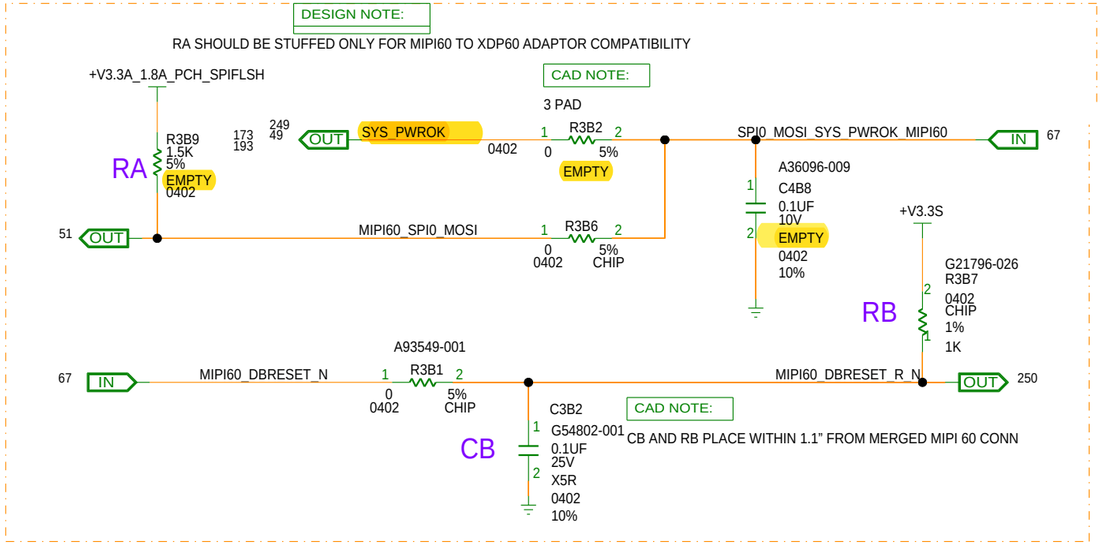
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE









[PAGE_TITLE=JTAG/CFG - PCH MIPI 60 VISA CONNECTOR]

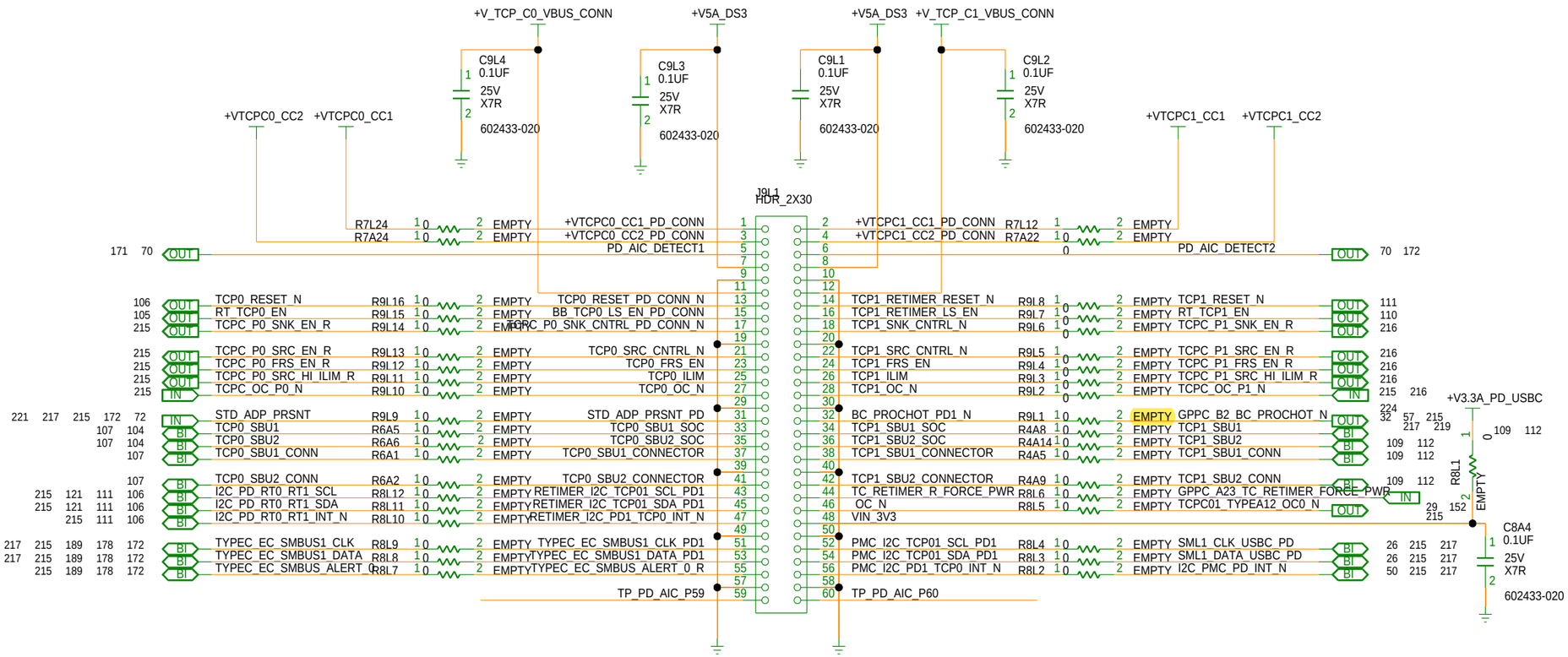
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.69
Wed Dec 18 18:06:27 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	69	1.0

CUSTOM TEXT BPAGE

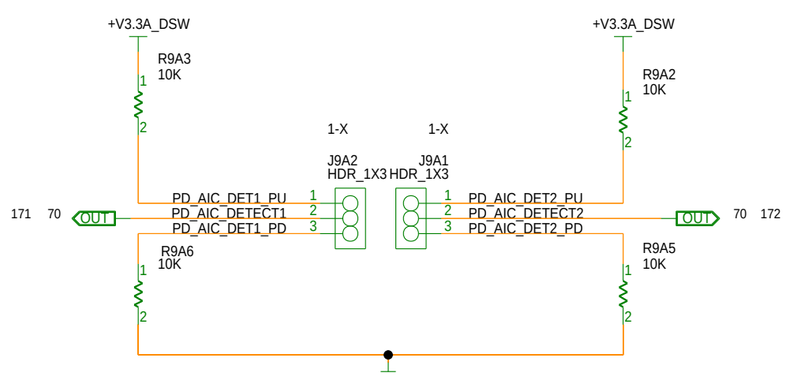
MODULE REV DETAILS		
MODULE NAME	REV	DATE

PD AIC CONTROLLER



CAD NOTE:

ALL THE RESISTORS IN THIS PAGE SHOULD BE TRIPAD WITH RESPECTIVE RESISTOR IN OTHER SECTION



[PAGE_TITLE=PD AIC CONNECTOR]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.70
Wed Dec 18 18:06:28 2019

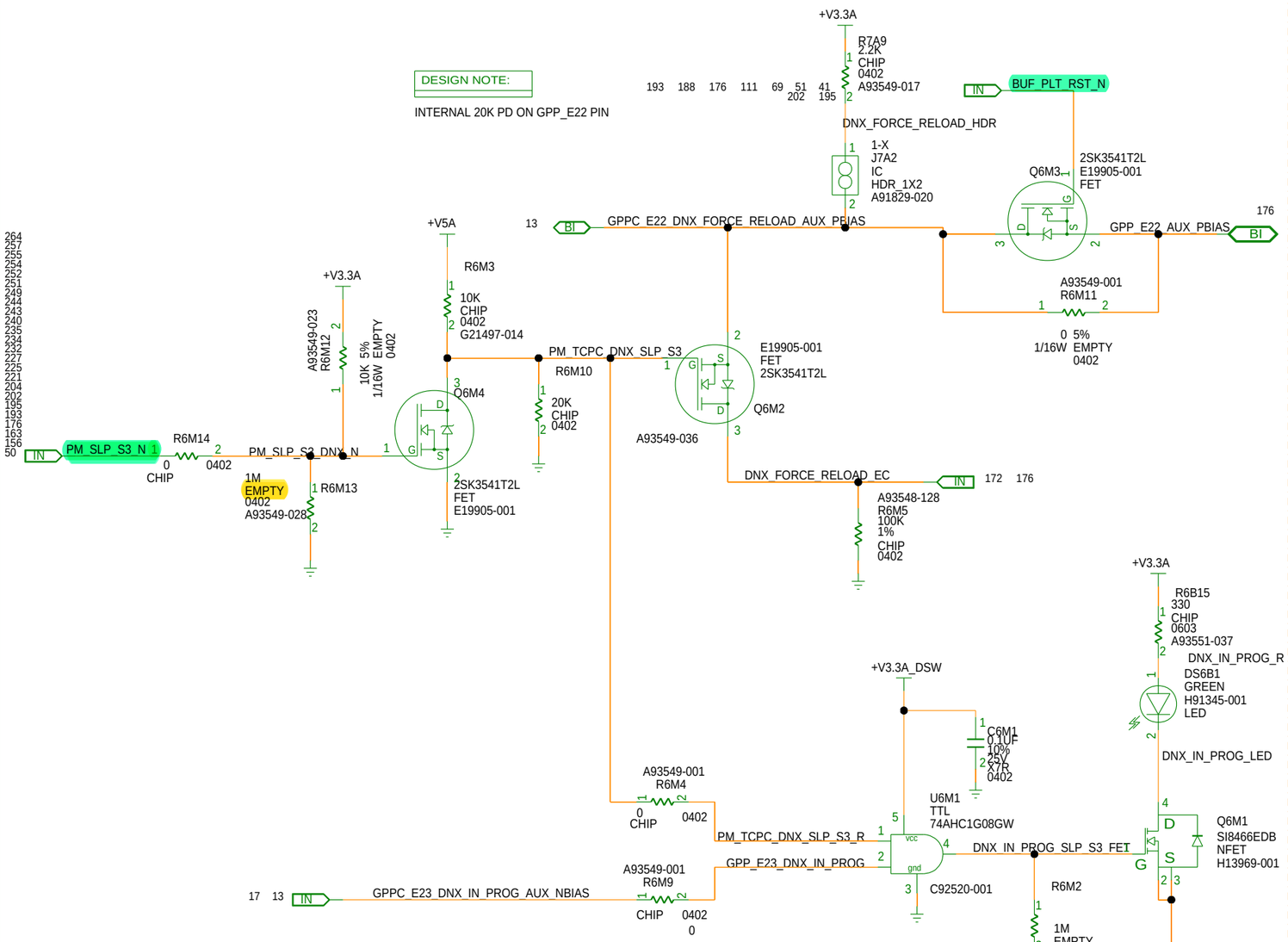
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	70	1.0

CUSTOM TEXT BPAGE

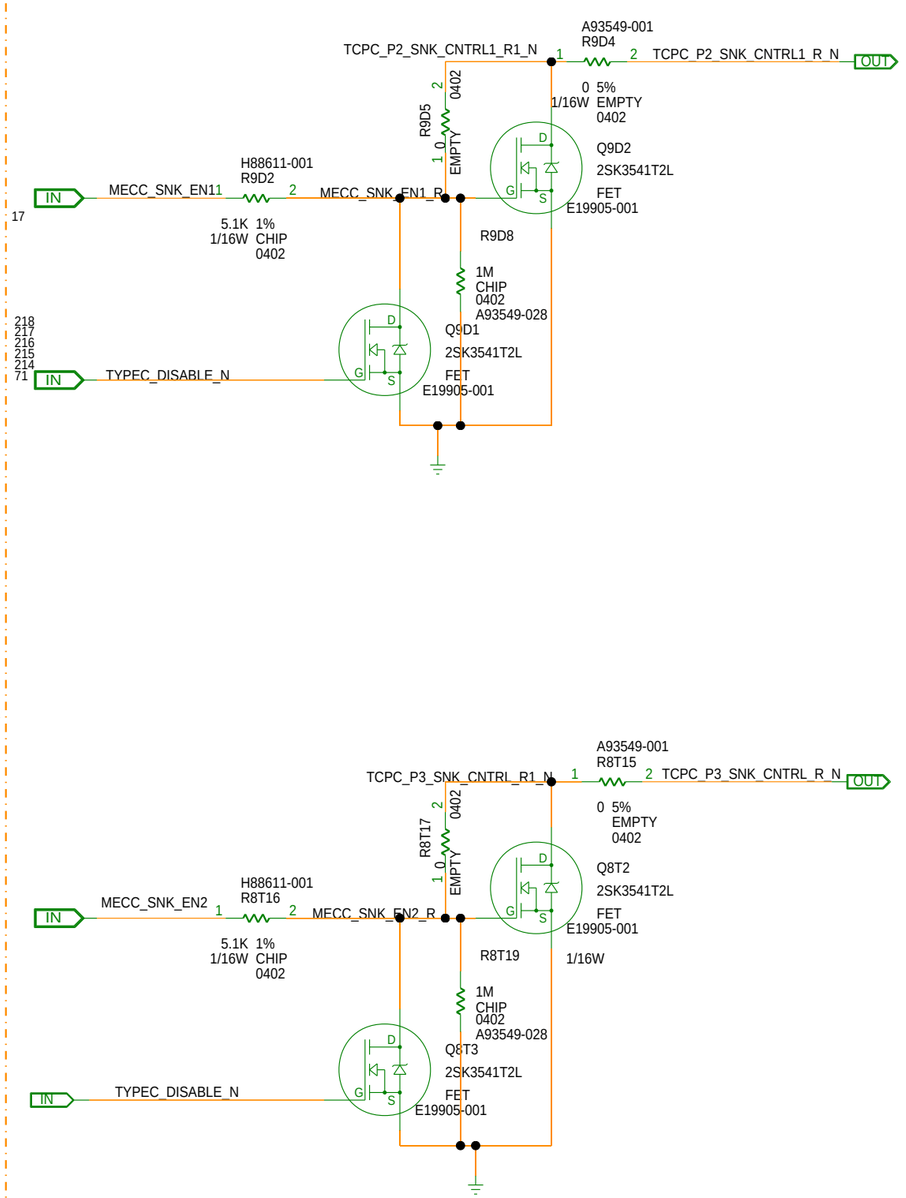
MODULE REV DETAILS		
MODULE NAME	REV	DATE

DNX CIRCUIT

DESIGN NOTE:
INTERNAL 20K PD ON GPP_E22 PIN



MECC SOURCE CONTROL



[PAGE_TITLE= USBC DNX CIRCUIT]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.71
Wed Dec 18 18:06:29 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	71	1.0

CUSTOM TEXT BPAGE

USB2 FROM MECC TO USBC CONNECTOR

177 IN MECC_USBC_PD_CON2_DP — R7F9 (0, EMPTY 0402) — USB2_P7_DIRECT_DP OUT 43

CAD NOTE: 3 PAD

72 IN USB2_P7_R_DP — R7F10 (0, CHIP 0402) — USB2_P7_DIRECT_DP

177 IN MECC_USBC_PD_CON2_DN — R7F5 (0, EMPTY 0402) — USB2_P7_DIRECT_DN

CAD NOTE: 3 PAD

72 IN USB2_P7_R_DN — R7F6 (0, CHIP 0402) — USB2_P7_DIRECT_DN OUT 43

USB2 FROM SOC TO MECC

34 IN USB2_P7_DP — R7F16 (0, EMPTY 0402) — MECC_USBC_PD_HOST2_DP OUT 176

CAD NOTE: 3 PAD

R7F15 (0, CHIP 0402) — USB2_P7_R_DP OUT 72

34 IN USB2_P7_DN — R7F13 (0, EMPTY 0402) — MECC_USBC_PD_HOST2_DN OUT 176

CAD NOTE: 3 PAD

R7F14 (0, CHIP 0402) — USB2_P7_R_DN OUT 72

SBU

114 IN TCP2_SBU1 — R9P28 (0, EMPTY 0402) — MECC_SBU1_1 OUT 176

CAD NOTE: DO NOT 3 PAD

R9P27 (0, CHIP 0402) — TCP2_SBU1_DIRECT OUT 117

114 IN TCP2_SBU2 — R9P29 (0, EMPTY 0402) — MECC_SBU2_1 OUT 176

CAD NOTE: DO NOT 3 PAD

R9P26 (0, CHIP 0402) — TCP2_SBU2_DIRECT OUT 117

RESET AND LOAD SWITCH

116 OUT TCP2_RETIMER_RESET_N — R9D20 (0, EMPTY 0402) — MECC_RETIMER_RESET_N_1 IN 189

120 OUT TCP3_RETIMER_RESET_N — R9T13 (0, EMPTY 0402) — MECC_RETIMER_RESET_N_2 IN 177

115 OUT +V3.3DX_RT_TCP2_EN — R8P6 (0, EMPTY 0402) — MECC_RETIMER_LS_EN_1 IN 177

119 OUT +V3.3DX_RT_TCP3_EN — R8E44 (0, EMPTY 0402) — MECC_RETIMER_LS_EN_2 IN 177

215 162 116 106 111 120 172 217 70 IN GPPC_A23_TC_RETIMER_FORCE_PWR — R6G20 (0, EMPTY 0402) — MECC_RETIMER_FORCE_PWR OUT 189

CC SIGNALS

CAD NOTE: 3 PAD WITH RA2, RB2 IN PG 119

217 117 BI +VTCPC2_CC1 — R8E34 (0, EMPTY 0402) — +VTCPC2_CC1_MECC BI 176

217 117 BI +VTCPC2_CC2 — R9P18 (0, EMPTY 0402) — +VTCPC2_CC2_MECC BI 176

CAD NOTE: 3 PAD WITH RC2, RD2 IN PG 243

217 121 BI +VTCPC3_CC1 — R8R10 (0, EMPTY 0402) — +VTCPC3_CC1_MECC BI 176

217 121 BI +VTCPC3_CC2 — R8R17 (0, EMPTY 0402) — +VTCPC3_CC2_MECC BI 176

VBUS CONTROL PINS

217 OUT TCPC_P2_SRC_EN_R — R9P24 (0, EMPTY 0402) — MECC_SRC_EN1 IN 176

218 OUT TCPC_P3_SRC_EN_R — R9F32 (0, EMPTY 0402) — MECC_SRC_EN2 IN 176

217 OUT TCPC_P2_FRS_EN_R — R9P23 (0, EMPTY 0402) — MECC_FRS_EN1 IN 189

218 OUT TCPC_P3_FRS_EN_R — R9T18 (0, EMPTY 0402) — MECC_FRS_EN2 IN 189

BI +V_TCP_C2_VBUS_CONN_R — R8P1 (0, EMPTY 0603) — +V_MECC_VBUS_1

BI +V_TCP_C3_VBUS_CONN_R — R1A2 (0, EMPTY 0603) — +V_MECC_VBUS_2

FAULT SIGNALS

217 IN TCPC_OC_P2_N — R8E4 (0, EMPTY 0402) — MECC_OC_P1_N OUT 189

CAD NOTE: 3 PAD

R8E5 (0, CHIP 0402) — TCPC_OC_DIRECT_P2_N OUT 217

218 IN TCPC_OC_P3_N — R8E18 (0, EMPTY 0402) — MECC_OC_P2_N OUT 189

CAD NOTE: 3 PAD

R8E19 (0, CHIP 0402) — TCPC_OC_DIRECT_P3_N OUT 217

221 217 172 70 215 IN STD_ADP_PRSNT — R7A30 (0, EMPTY 0402) — MECC_STD_ADP_PRSNT OUT 177

RETIMER I2C TO MECC CONNECTOR

BI I2C_PD_RT2_RT3_SDA — R8T7 (0, EMPTY 0402) — MECC_USBC_RETIMER_I2C1_DATA BI 189

BI I2C_PD_RT2_RT3_SCL — R8T2 (0, EMPTY 0402) — MECC_USBC_RETIMER_I2C1_CLK BI 189

OUT I2C_PD_RT2_RT3_INT_N — R9F15 (0, EMPTY 0402) — MECC_USBC_RETIMER_ALRT_P1 IN 189

SECOND RETIMER I2C ISOLATION FOR MECC CONNECTOR

BI I2C_PD_RT2_RT3_SDA — 59 R9T8 (0, CHIP 0402) — I2C_PD_RT2_RT3_ISO_SDA BI 120

BI I2C_PD_RT2_RT3_SCL — 60 R9T10 (0, CHIP 0402) — I2C_PD_RT2_RT3_ISO_SCL BI 120

BI I2C_PD_RT2_RT3_INT_N — 73 R9F12 (0, CHIP 0402) — I2C_PD_RT2_RT3_INT_ISO_N IN 120

OUT GPPC_A14_DDSP_HPD_3_I2S3_RXD_DMIC_CLK_B1 — R3T7 (0, EMPTY 0402) — MECC_HPD1 IN 176

OUT GPPC_A15_DDSP_HPD_4_I2S4_SCLK — R3G17 (0, EMPTY 0402) — MECC_HPD2 IN 176

OUT GPPC_B11_PMC_ALERT_N — R6F54 (0, EMPTY 0402) — MECC_PMC_ALERT_N IN 177

[PAGE_TITLE= MECC TRIPAD SHARING

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.72
Wed Dec 18 18:06:30 2019

MODULE REV DETAILS		
MODULE NAME	REV	DATE

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	72	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

U4E1
SOC
1.6
TGL_UP3_IP_EXT
8 OF 21
LPID6529

73	PCIE4_P3_TX_DP	P5	PCIE4_TX_P_3	PCIE4_TX_P_1	V5	PCIE4_P1_TX_DP	73
73	PCIE4_P3_TX_DN	P7	PCIE4_TX_N_3	PCIE4_TX_N_1	V7	PCIE4_P1_TX_DN	73
73	PCIE4_P3_RX_DP	N1	PCIE4_RX_P_3	PCIE4_RX_P_1	T1	PCIE4_P1_RX_DP	73
73	PCIE4_P3_RX_DN	N2	PCIE4_RX_N_3	PCIE4_RX_N_1	T2	PCIE4_P1_RX_DN	73
73	PCIE4_P2_TX_DP	T5	PCIE4_TX_P_2	PCIE4_TX_P_0	Y5	PCIE4_P0_TX_DP	73
73	PCIE4_P2_TX_DN	T7	PCIE4_TX_N_2	PCIE4_TX_N_0	Y7	PCIE4_P0_TX_DN	73
73	PCIE4_P2_RX_DP	R1	PCIE4_RX_P_2	PCIE4_RX_P_0	V1	PCIE4_P0_RX_DP	73
73	PCIE4_P2_RX_DN	R2	PCIE4_RX_N_2	PCIE4_RX_N_0	V2	PCIE4_P0_RX_DN	73
				PCIE4_RCOMP_P	Y12	PCIE4_RCOMP_P	
				PCIE4_RCOMP_N	V12	PCIE4_RCOMP_N	

RX_P1_DP/DN SWAPPED IN REV1P2 BALLMAP CHANGE

R4D16 1 2 2.2K 1% 1/16W CHIP G64084-082 0402

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

CAD NOTE:
3 PAD

73	PCIE4_P0_TX_DP	R7N22	A93549-001 CHIP	PCIE4_P0_M.2_SSD_TX_DP	OUT 155
		R7N21	A93549-001 EMPTY	PCIE4_P0_SLOT1_TX_DP	OUT 199
73	PCIE4_P0_TX_DN	R7N17	A93549-001 CHIP	PCIE4_P0_M.2_SSD_TX_DN	OUT 155
		R7N18	A93549-001 EMPTY	PCIE4_P0_SLOT1_TX_DN	OUT 199
73	PCIE4_P1_TX_DP	R6N22	A93549-001 CHIP	PCIE4_P1_M.2_SSD_TX_DP	OUT 155
		R6N21	A93549-001 EMPTY	PCIE4_P1_SLOT1_TX_DP	OUT 199
73	PCIE4_P1_TX_DN	R6N20	A93549-001 CHIP	PCIE4_P1_M.2_SSD_TX_DN	OUT 155
		R6N19	A93549-001 EMPTY	PCIE4_P1_SLOT1_TX_DN	OUT 199
73	PCIE4_P2_TX_DP	R7N9	A93549-001 CHIP	PCIE4_P2_M.2_SSD_TX_DP	OUT 155
		R7N10	A93549-001 EMPTY	PCIE4_P2_SLOT1_TX_DP	OUT 199
73	PCIE4_P2_TX_DN	R7N6	A93549-001 CHIP	PCIE4_P2_M.2_SSD_TX_DN	OUT 155
		R7N5	A93549-001 EMPTY	PCIE4_P2_SLOT1_TX_DN	OUT 199
73	PCIE4_P3_TX_DP	R6N17	A93549-001 CHIP	PCIE4_P3_M.2_SSD_TX_DP	OUT 155
		R6N18	A93549-001 EMPTY	PCIE4_P3_SLOT1_TX_DP	OUT 199
73	PCIE4_P3_TX_DN	R6N15	A93549-001 CHIP	PCIE4_P3_M.2_SSD_TX_DN	OUT 155
		R6N14	A93549-001 EMPTY	PCIE4_P3_SLOT1_TX_DN	OUT 199

73	PCIE4_P0_RX_DP	R6N25	0402 CHIP	PCIE4_P0_M.2_SSD_RX_DP	IN 156
		R6N26	A93549-001 EMPTY	PCIE4_P0_SLOT1_RX_DP	IN 199
73	PCIE4_P0_RX_DN	R6N24	0402 CHIP	PCIE4_P0_M.2_SSD_RX_DN	IN 156
		R6N23	A93549-001 EMPTY	PCIE4_P0_SLOT1_RX_DN	IN 199
73	PCIE4_P1_RX_DP	R7N29	0402 CHIP	PCIE4_P1_M.2_SSD_RX_DP	IN 156
		R7N30	A93549-001 EMPTY	PCIE4_P1_SLOT1_RX_DP	IN 199
73	PCIE4_P1_RX_DN	R7N33	0402 CHIP	PCIE4_P1_M.2_SSD_RX_DN	IN 156
		R7N34	A93549-001 EMPTY	PCIE4_P1_SLOT1_RX_DN	IN 199
73	PCIE4_P2_RX_DP	R6N28	0402 CHIP	PCIE4_P2_M.2_SSD_RX_DP	IN 156
		R6N27	A93549-001 EMPTY	PCIE4_P2_SLOT1_RX_DP	IN 199
73	PCIE4_P2_RX_DN	R6N30	0402 CHIP	PCIE4_P2_M.2_SSD_RX_DN	IN 156
		R6N29	A93549-001 EMPTY	PCIE4_P2_SLOT1_RX_DN	IN 199
73	PCIE4_P3_RX_DP	R7N42	0402 CHIP	PCIE4_P3_M.2_SSD_RX_DP	IN 156
		R7N41	A93549-001 EMPTY	PCIE4_P3_SLOT1_RX_DP	IN 199
73	PCIE4_P3_RX_DN	R7N45	0402 CHIP	PCIE4_P3_M.2_SSD_RX_DN	IN 156
		R7N46	A93549-001 EMPTY	PCIE4_P3_SLOT1_RX_DN	IN 199

CAD NOTE:
3 PAD

[PAGE_TITLE=TGL U MCP(8 OF 21)- PCIE GEN4]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.73
Wed Dec 18 18:06:31 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	73	1.0

CUSTOM TEXT BPAGE

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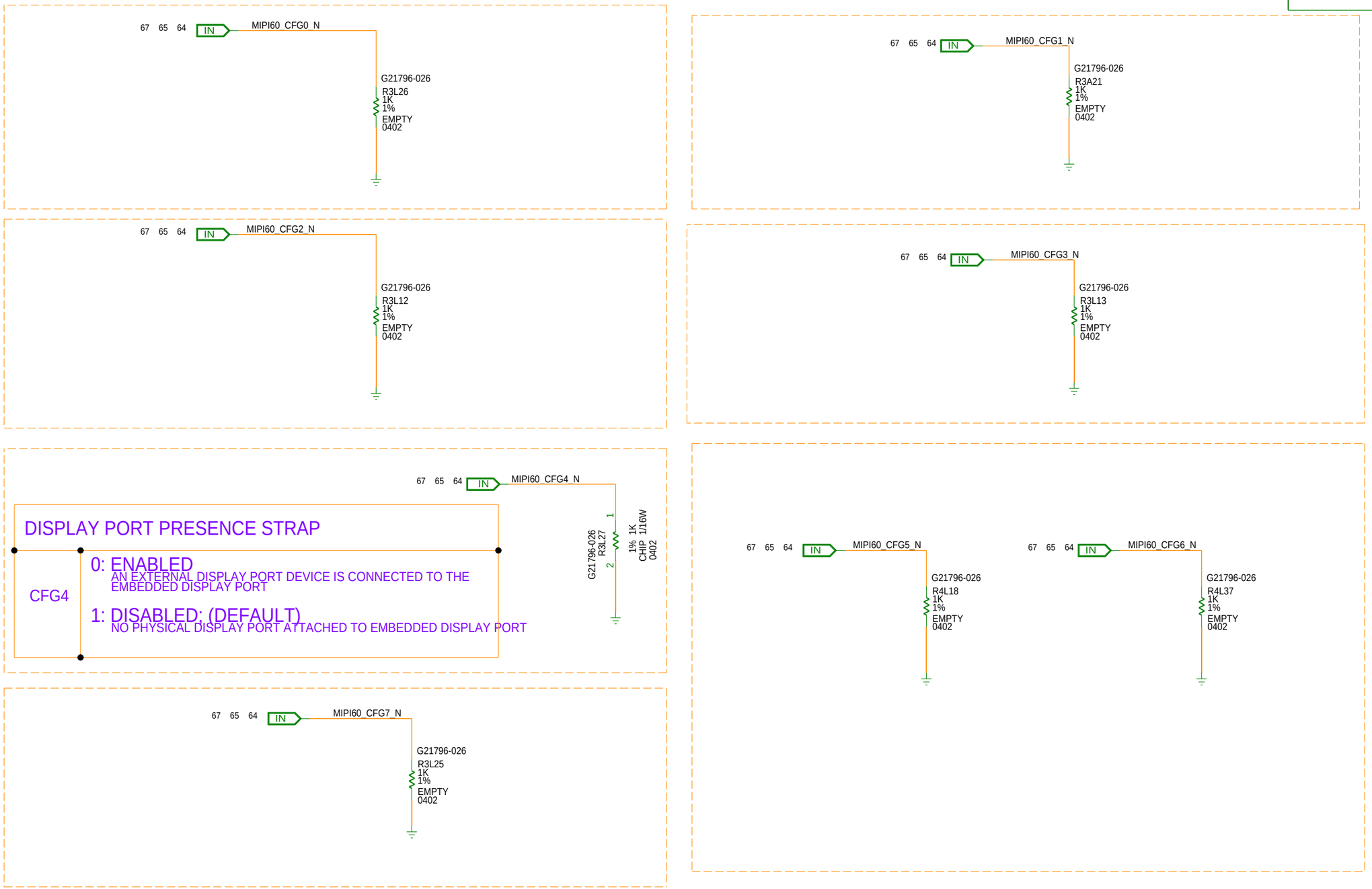
MODULE NAME	REV	DATE



[PAGE_TITLE= CPU_STRAPS_1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.74
Wed Dec 18 18:06:32 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	74	1.0

CUSTOM TEXT BPAGE

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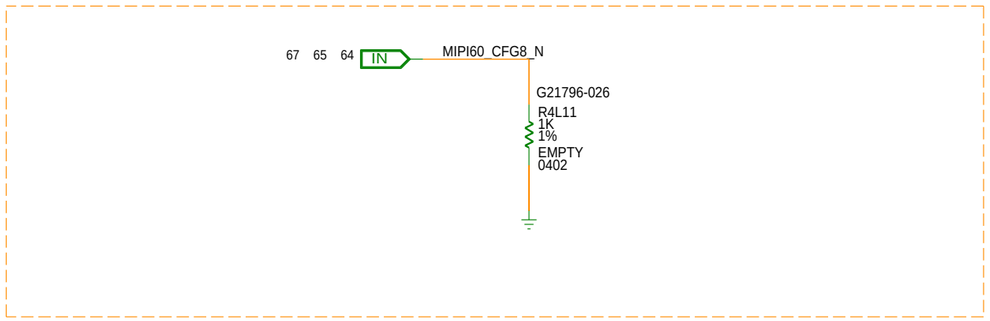
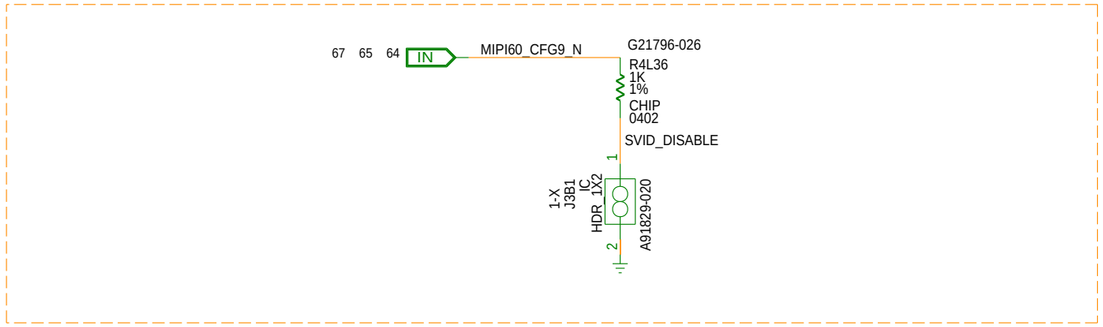
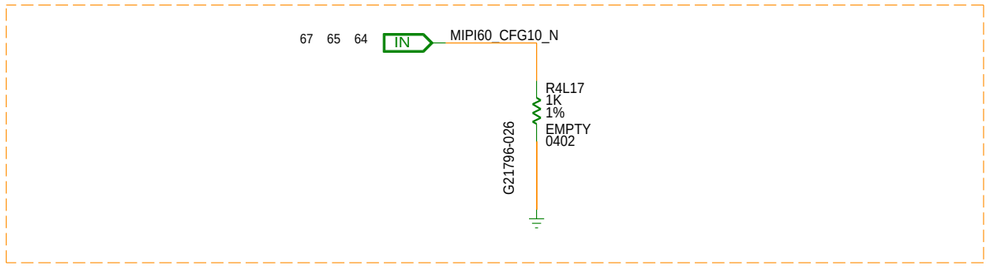
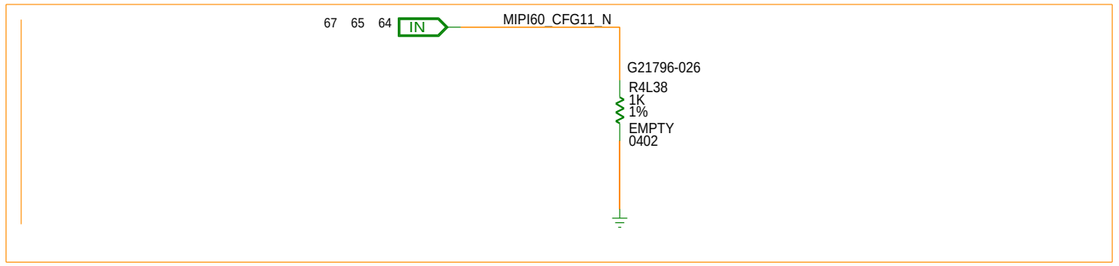
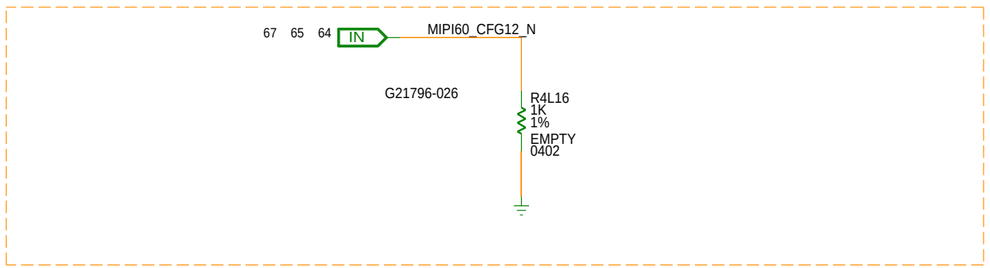
MODULE NAME	REV	DATE

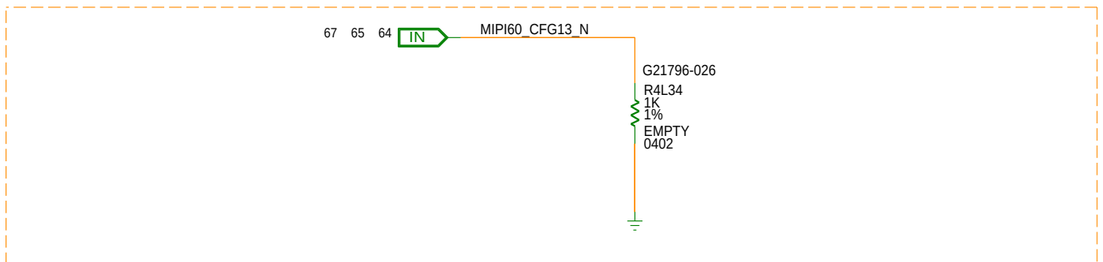


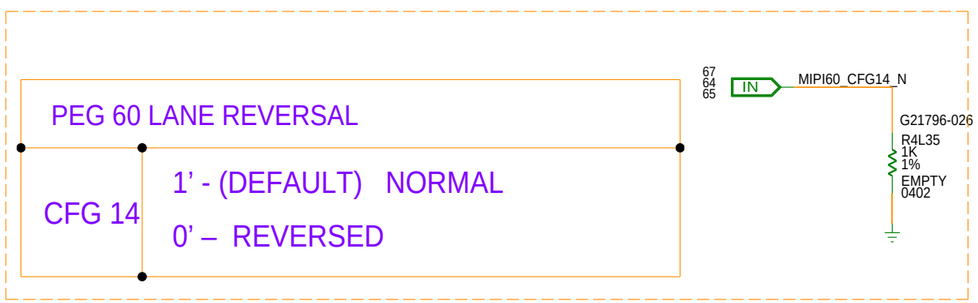


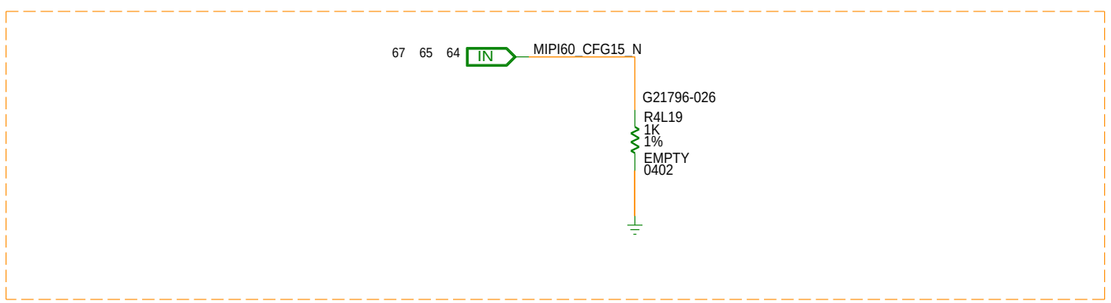












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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.75
Wed Dec 18 18:06:33 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

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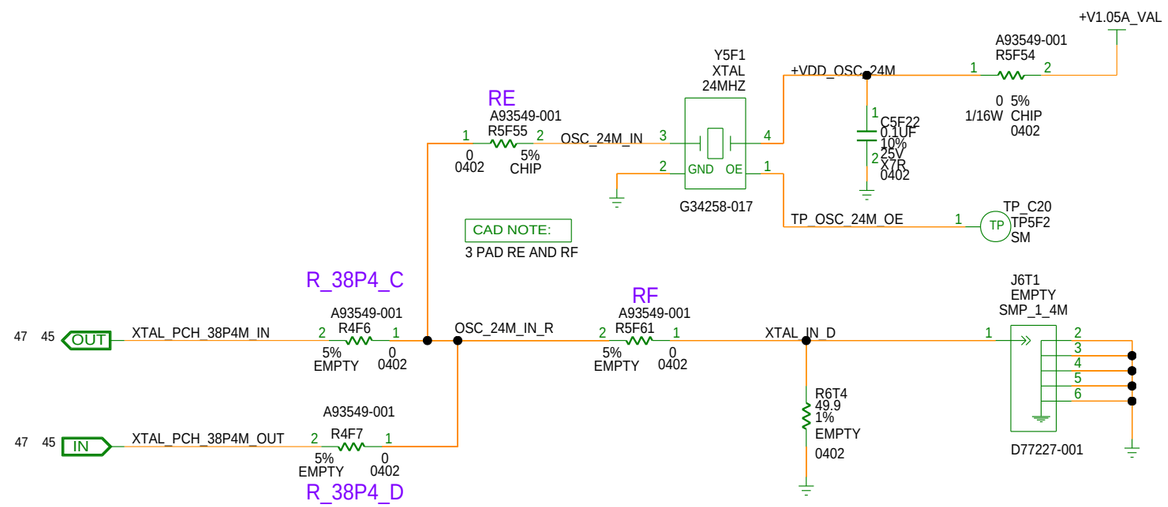
MODULE NAME	REV	DATE



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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.76
Wed Dec 18 18:06:34 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	76	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

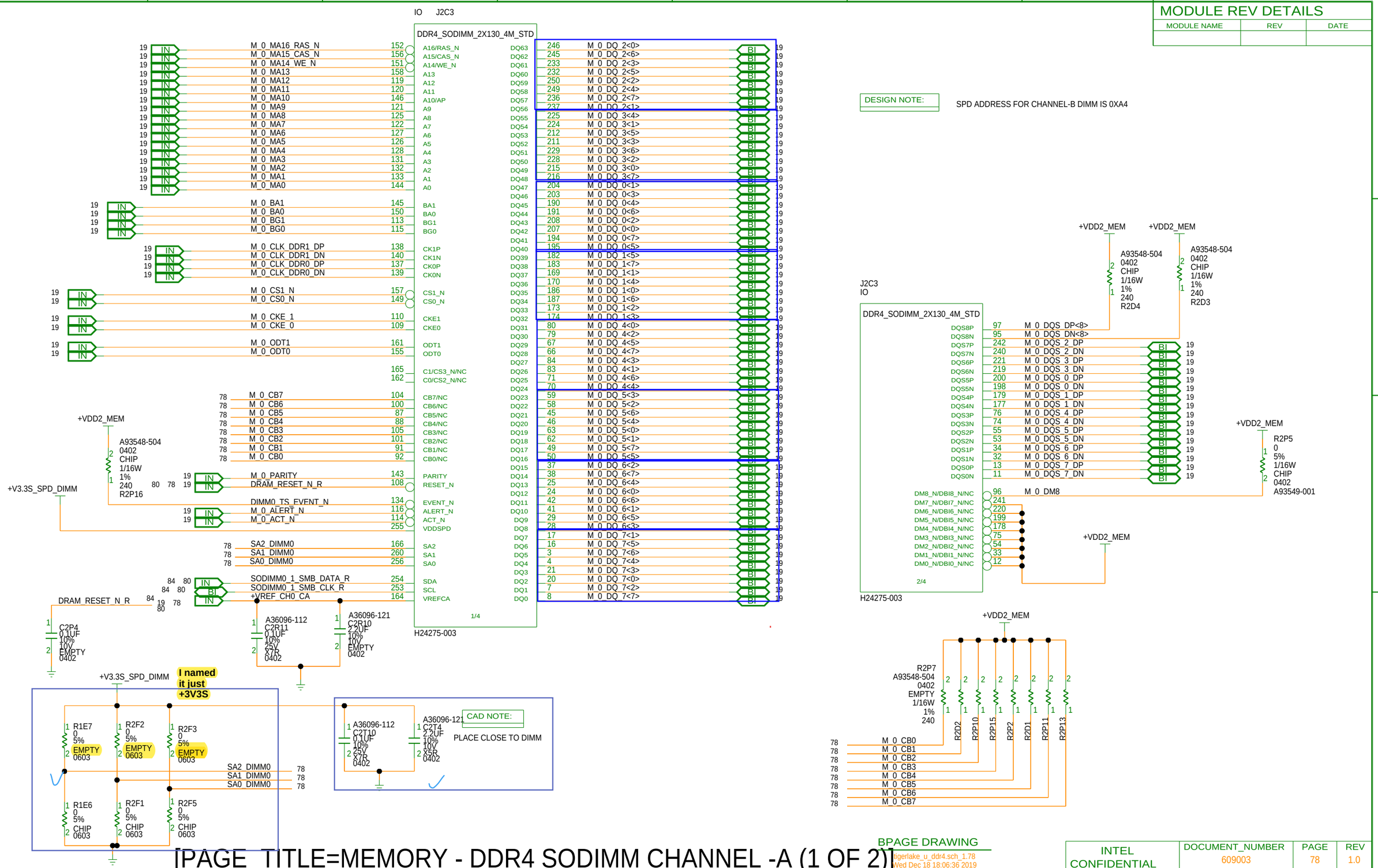
[PAGE_TITLE=RESERVE]

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.77
Tue Oct 15 12:49:33 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	77	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE



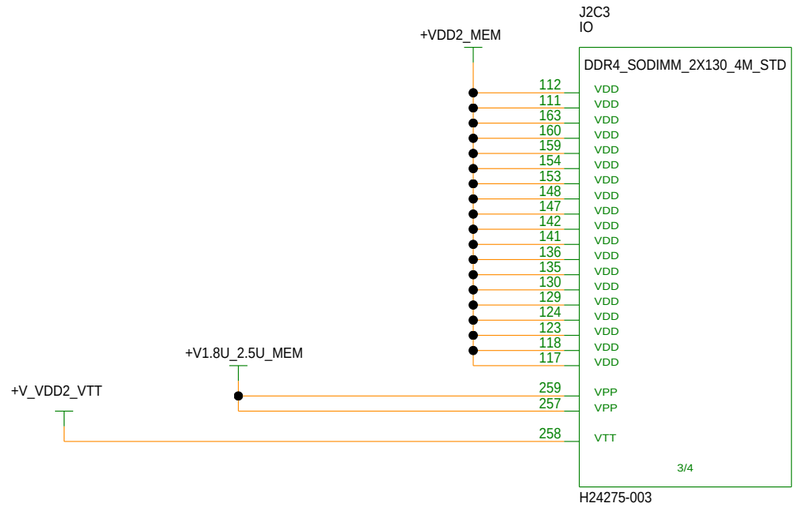
[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -A (1 OF 2)]

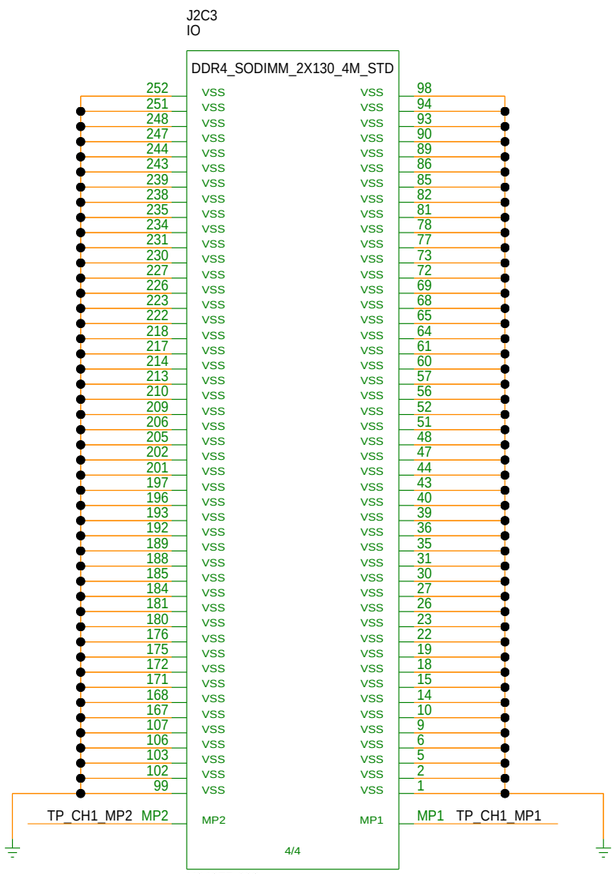
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.78
Wed Dec 18 18:06:36 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	78	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE





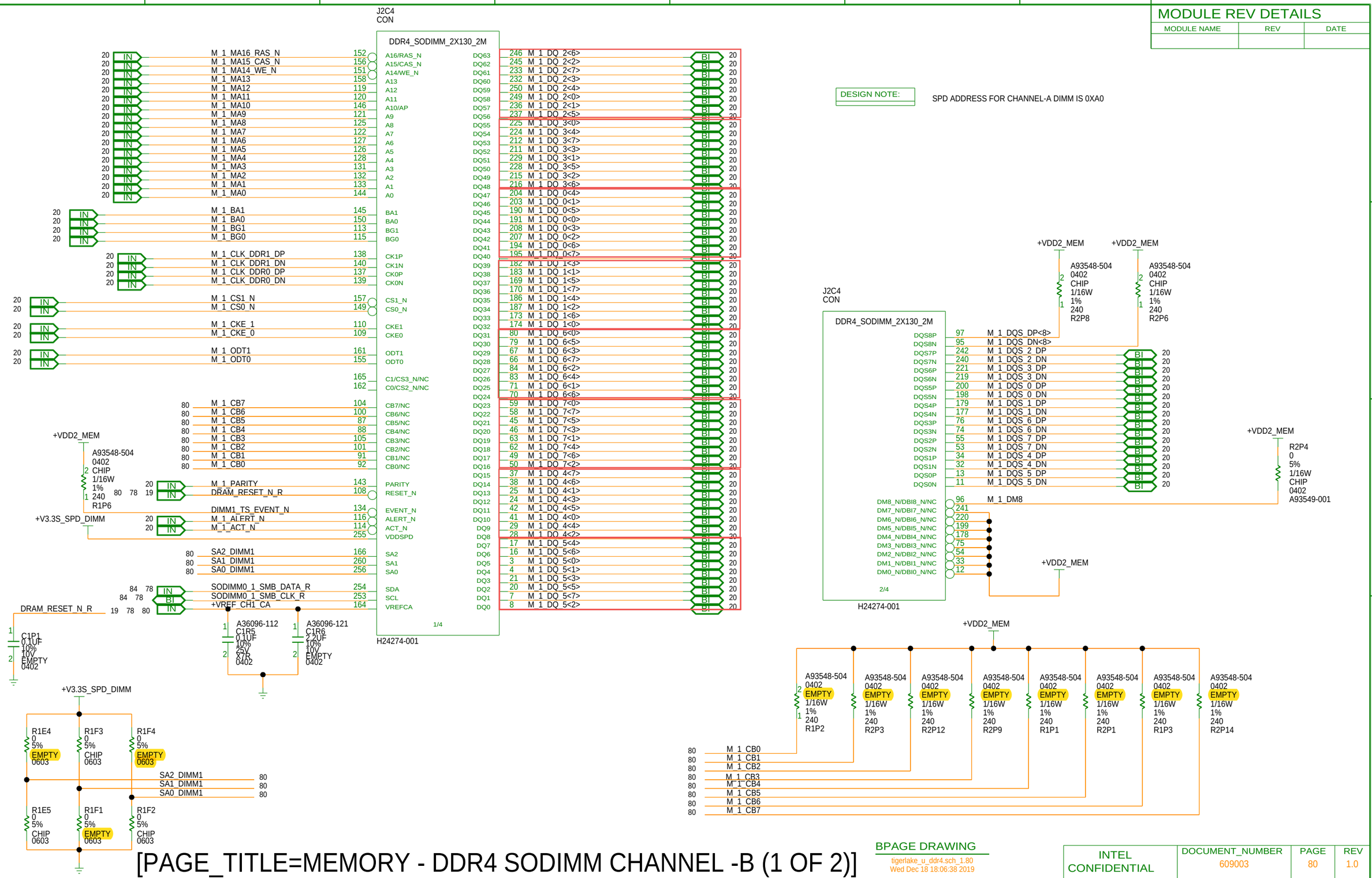
[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -A (2 OF 2)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.79
Wed Dec 18 18:06:37 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	79	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -B (1 OF 2)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.80
Wed Dec 18 18:06:38 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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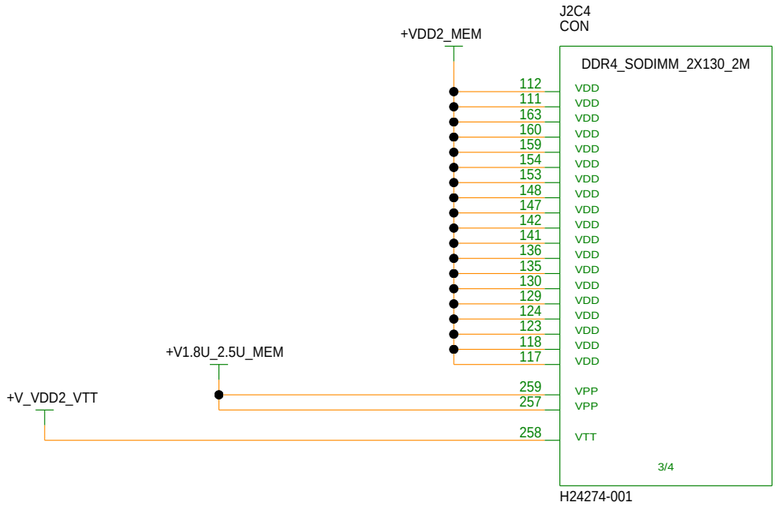
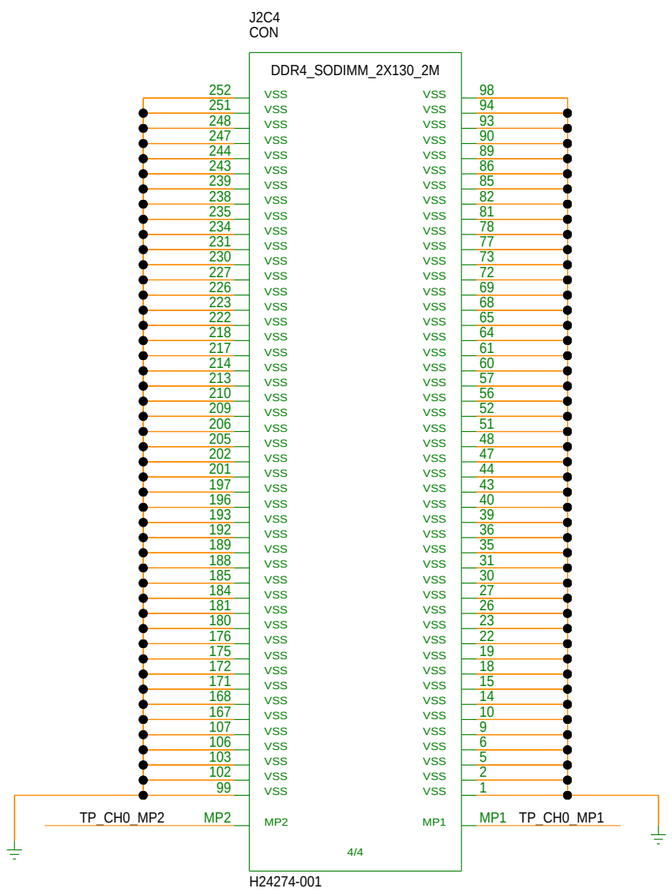
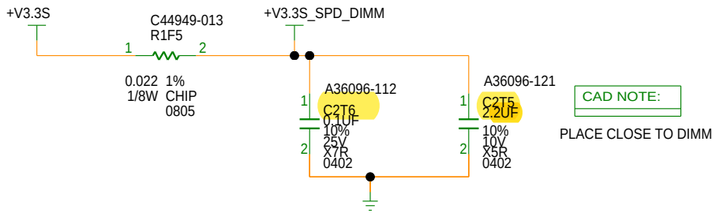
MODULE REV DETAILS		
MODULE NAME	REV	DATE







[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -B (2 OF 2)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.81
Wed Dec 18 18:06:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	81	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

VTT DECAPS

PLACE THESE CAPS CLOSE TO SODIMM

CAD NOTE:

+V_VDD2_VTT

17 C2T3 1UF 10% 25V X5R 0402 A36096-143

17 C2T8 1UF 10% 25V X5R 0402 A36096-143

CAD NOTE:
2 CAPS PER DRAM, AS CLOSE AS POSSIBLE

18 602433-075 C2F3 10UF 20% 6.3V X5R 0603

CAD NOTE:
PLACED ON VTT PLANE CLOSE TO DIMM, 1 CAP STUFFED, 1 PLACEHOLDER

VPP DECAPS

PLACE THESE CAPS CLOSE TO SODIMM

CAD NOTE:

+V1.8U_2.5U_MEM

C2F1 1UF 10% 25V X5R 0402 A36096-143

602433-075 C2F2 10UF 20% 6.3V X5R 0603

CAD NOTE:
AS CLOSE AS POSSIBLE

VCC_VCCIN_SENSE_P

+VDD2_MEM

C2P1 12PF 5% 50V C0G 0402 A36095-043

C2R16 12PF 5% 50V C0G 0402 A36095-043

C2P9 12PF 5% 50V C0G 0402 A36095-043

C2R13 12PF 5% 50V C0G 0402 A36095-043

C2R15 12PF 5% 50V C0G 0402 A36095-043

+VDD2_MEM

C2P2 2.2PF 10% 50V C0G 0402 A36094-015

C2T1 2.2PF 10% 50V C0G 0402 A36094-015

C2P12 2.2PF 10% 50V C0G 0402 A36094-015

C2R12 2.2PF 10% 50V C0G 0402 A36094-015

C2R14 2.2PF 10% 50V C0G 0402 A36094-015

CAD NOTE:
ABOVE CAPS ARE ADDED FOR EMC LAYOUT FEEDBACK

VDDQ DECAPS

+VDD2_MEM

J2C3

CAD NOTE:
4 CAPS NEAR EACH SIDE OF DIMM CONNECTOR CLOSE TO VDD PINS

C2P18 1UF 10% 25V X5R 0402 A36096-143

C2D1 1UF 10% 25V X5R 0402 A36096-143

C2E1 1UF 10% 25V X5R 0402 A36096-143

C2R4 1UF 10% 25V X5R 0402 A36096-143

C2P19 1UF 10% 25V X5R 0402 A36096-143

C2P7 1UF 10% 25V X5R 0402 A36096-143

C2P13 1UF 10% 25V X5R 0402 A36096-143

C2R3 1UF 10% 25V X5R 0402 A36096-14

CAD NOTE:
4 CAPS NEAR EACH SIDE OF DIMM CONNECTOR CLOSE TO VDD PINS

602433-075 C2P6 10UF 20% 6.3V X5R 0603

602433-075 C2P16 10UF 20% 6.3V X5R 0603

602433-075 C2E2 10UF 20% 6.3V X5R 0603

602433-075 C2R8 10UF 20% 6.3V X5R 0603

5 602433-075 C2P5 10UF 20% 6.3V X5R 0603

5 602433-075 C2P10 10UF 20% 6.3V X5R 0603

5 602433-075 C2R7 10UF 20% 6.3V X5R 0603

602433-075 C2R2 10UF 20% 6.3V X5R 0603

CAD NOTE:
PLACEHOLDER

C2R9 330UF 20% 6.3V EMPTY 7343 724613-064

CAD NOTE:
PLACE THESE CAPS CLOSE TO SODIMM
OUT OF 8 DECAPS, PLACE 4 ON EACH SIDE OF SODIMM

[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -A PD BOM]

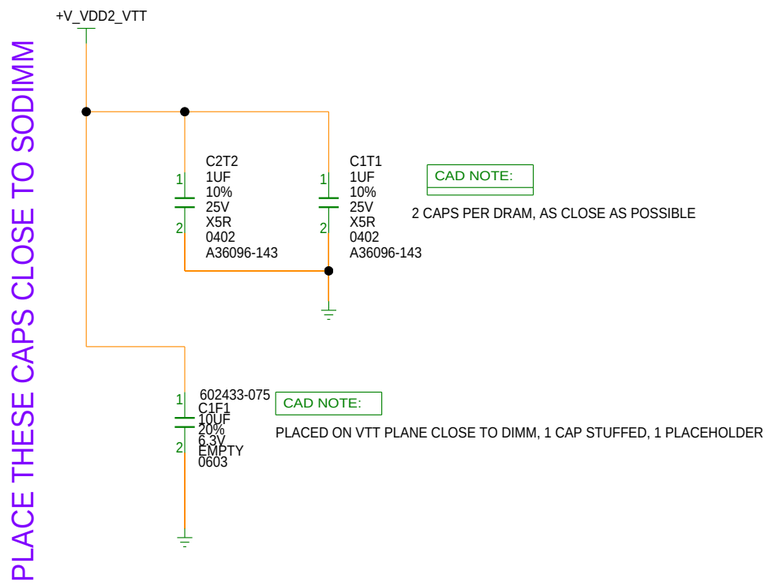
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.82
Wed Dec 18 18:06:40 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	82	1.0

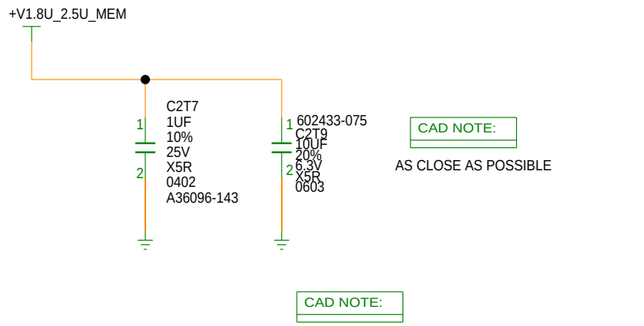
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

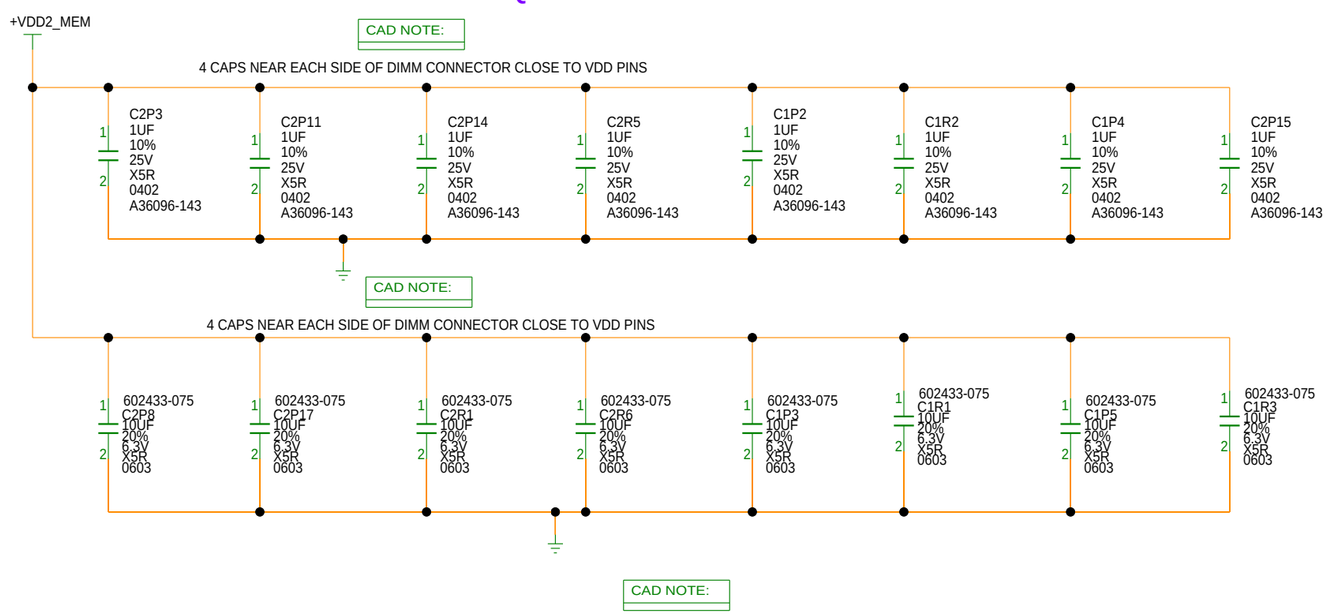
VTT DECAPS



VPP DECAPS



VDDQ DECAPS



[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -BPD BOM]

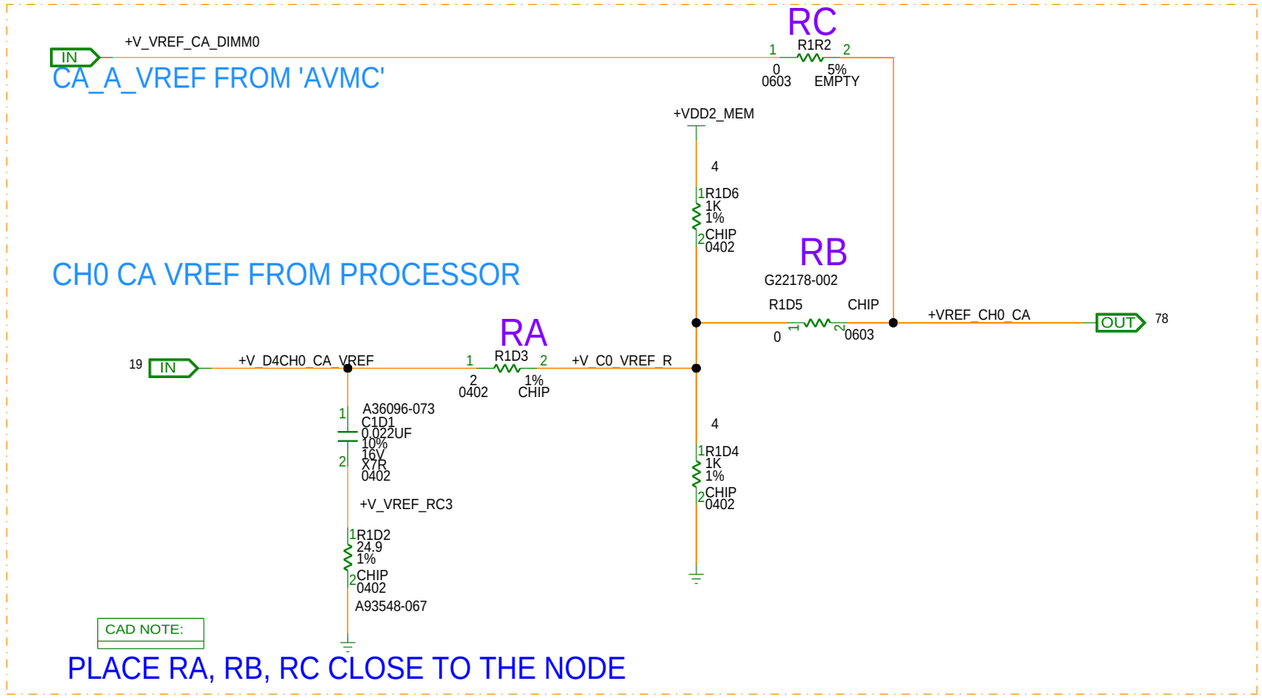
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.83
Wed Dec 18 18:06:41 2019

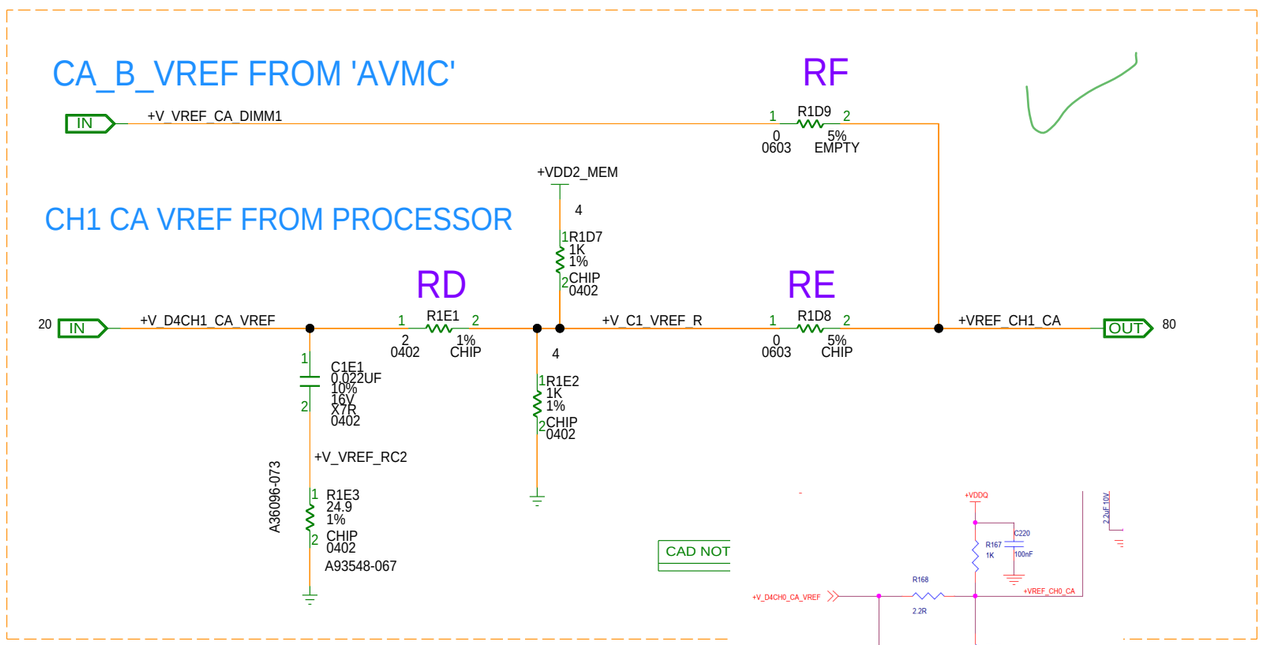
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	83	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

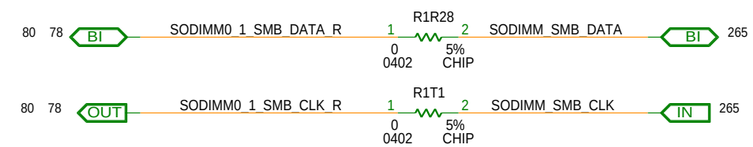
VREF CIRCUITRY

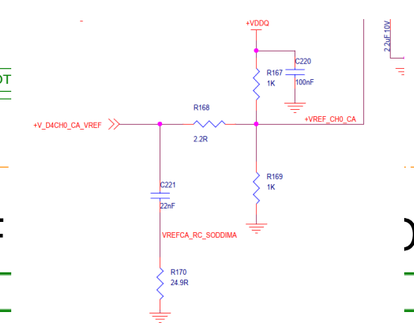




DESIGN NOTE:

DDR VREF DIFFERENT OPTIONS (OPTION 1 AND 2 IS DEFAULT)
1: VOLTAGE DIVIDER NETWORK (DEFAULT)
2: FROM PROCESSOR (DEFAULT)
3: FROM AVMC





[PAGE_TITLE=MEMORY - DDR VREF ... OCESSOR, OPTIONS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.84
Wed Dec 18 18:06:42 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	84	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=MEMORY - RESERVE]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.85
Tue Oct 15 12:49:41 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	85	1.0

MODULE REV DETAILS

MODULE NAME	REV	DATE

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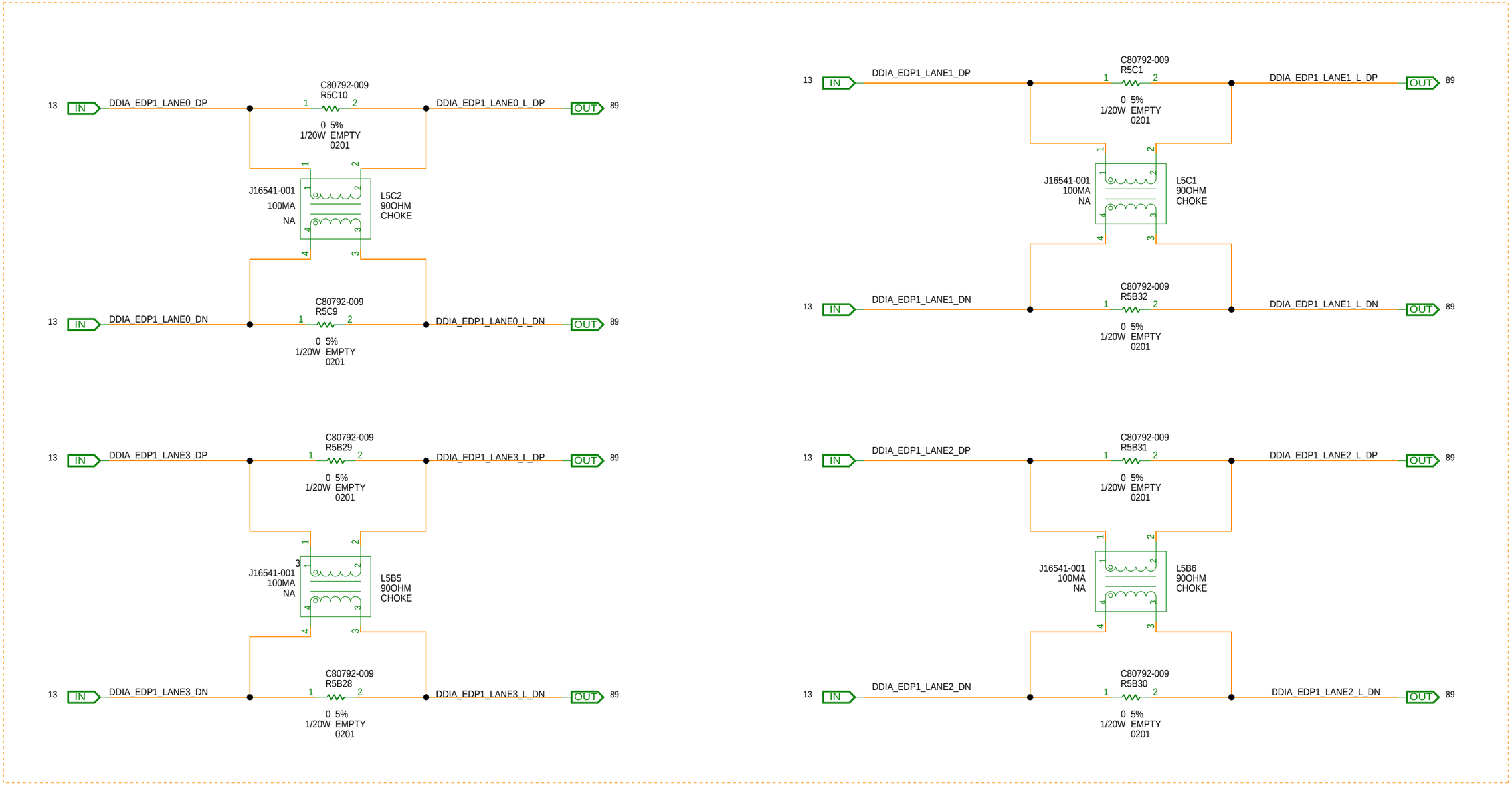
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.86
Wed Dec 18 16:29:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	86	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

EDP CONNECTOR 1 - CMC



[PAGE_TITLE=DISPLAY - eDP connector 1 - CMC]

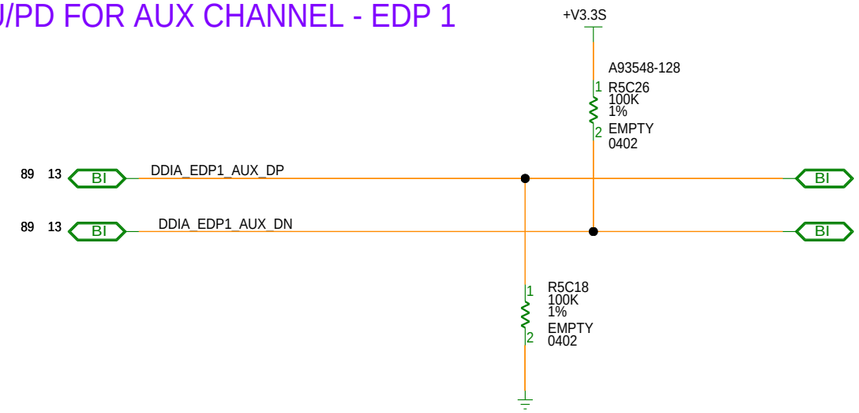
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.87
Tue Oct 15 12:49:42 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	87	1.0

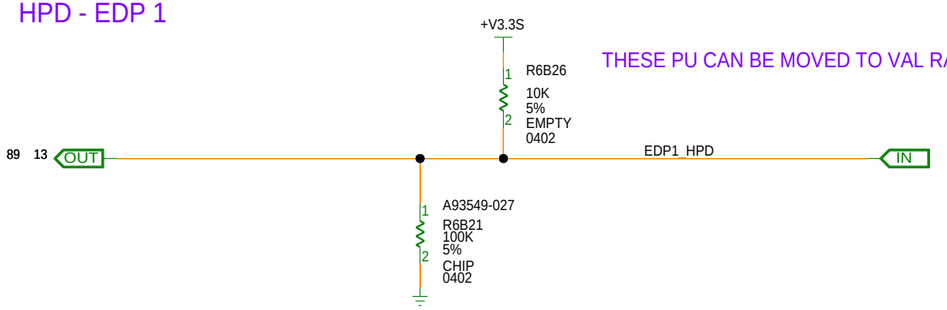
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

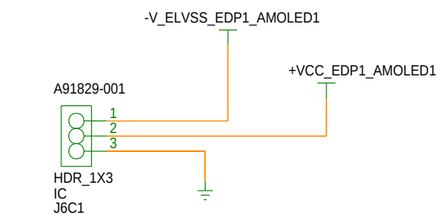
PU/PD FOR AUX CHANNEL - EDP 1



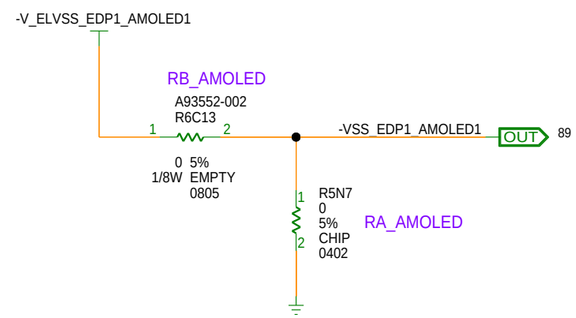
HPD - EDP 1

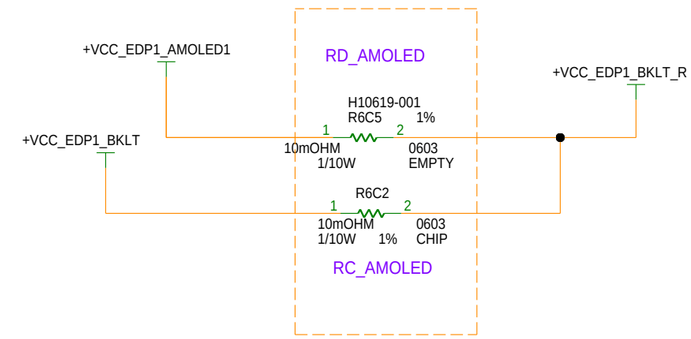


ADDITIONAL AMOLED POWER REQUIREMENTS

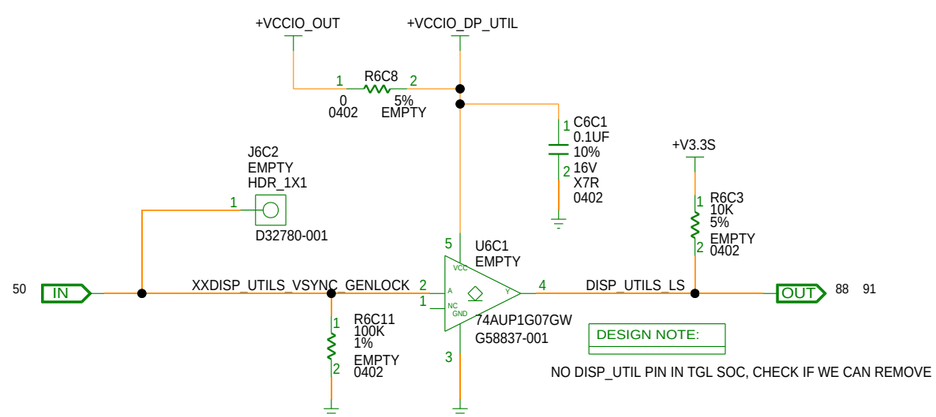


	STUFF	UNSTUFF
NORMAL EDP PANEL	RA_AMOLED & RC_AMOLED	RB_AMOLED & RD_AMOLED
AMOLED EDP PANEL	RB_AMOLED & RD_AMOLED	RA_AMOLED & RC_AMOLED

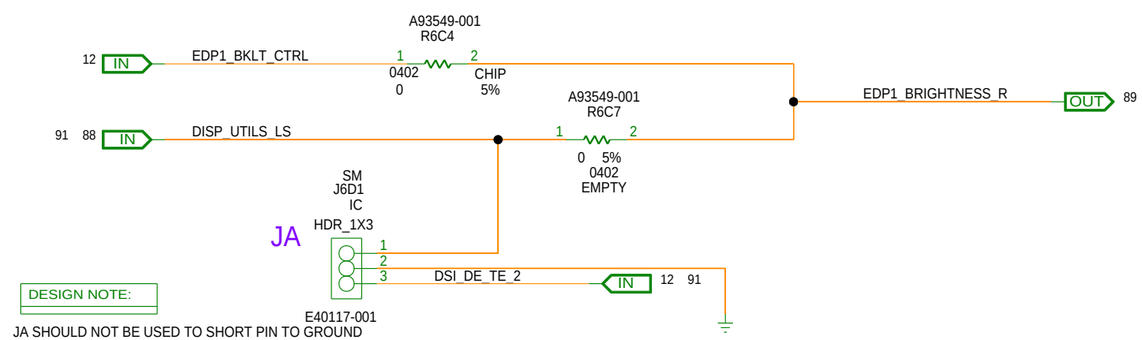




DISPLAY UTILITY LEVEL SHIFTER



BACKLIGHT CONTROL USING DISPLAY UTILITY PIN



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tigerlake_u_ddr4.sch_1.88
Wed Dec 18 18:06:45 2019

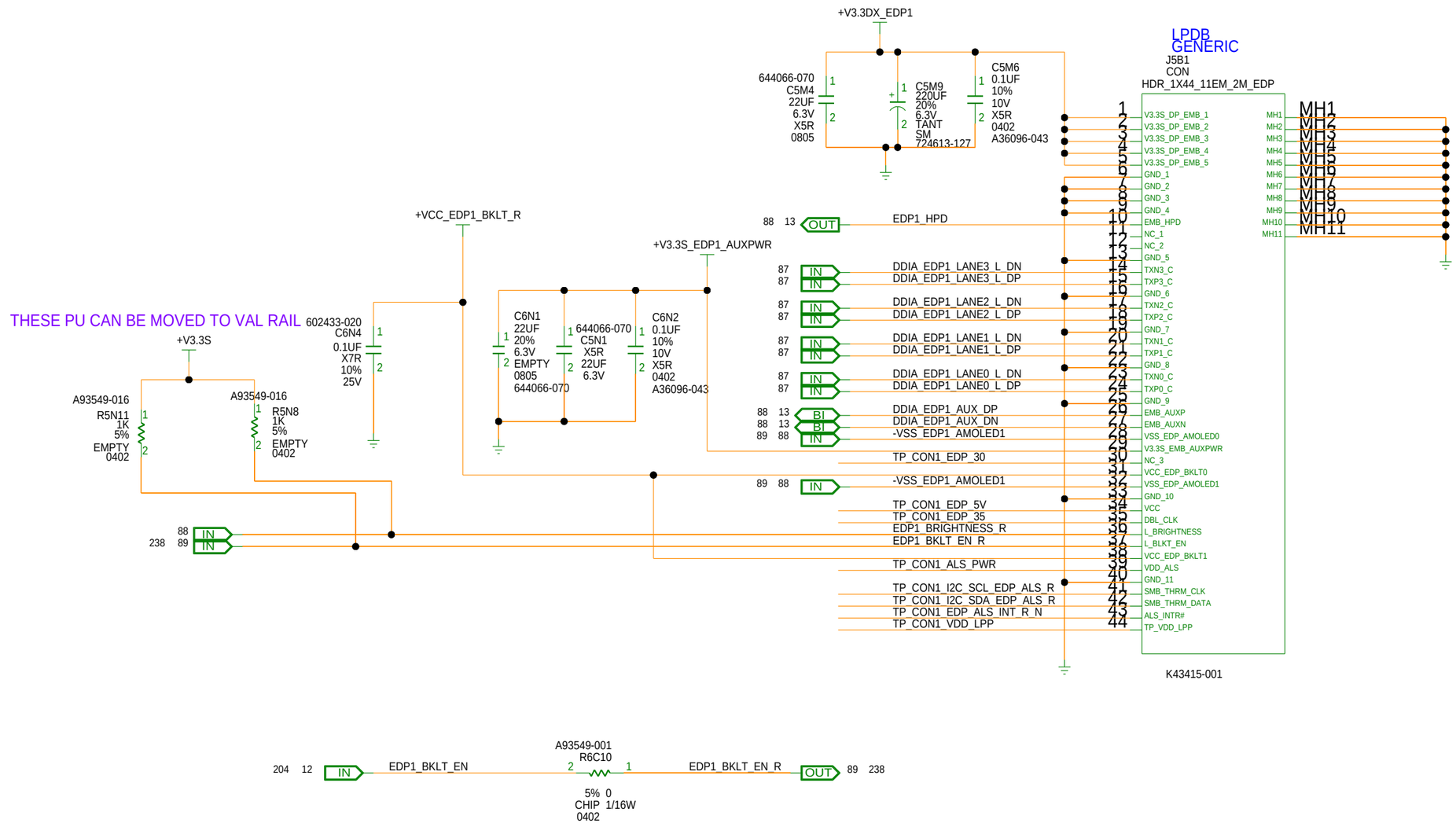
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	88	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

EDP CONNECTOR 1

CHANGE TANT CAP TO LOWER VALUE

THESE PU CAN BE MOVED TO VAL RAIL



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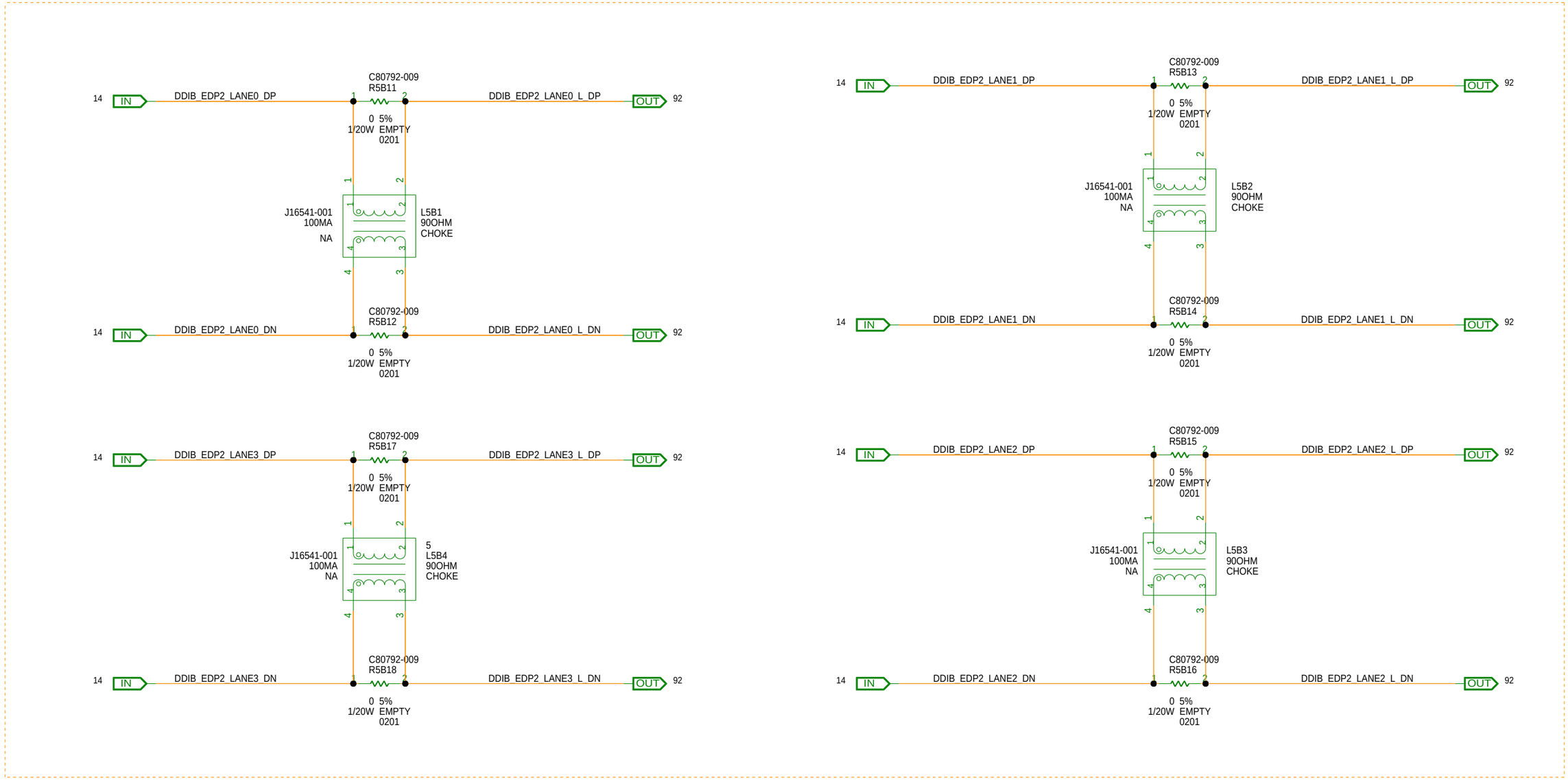
tigerlake_u_ddr4.sch_1.89
Wed Dec 18 18:06:46 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	89	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

EDP CONNECTOR 2 - CMC



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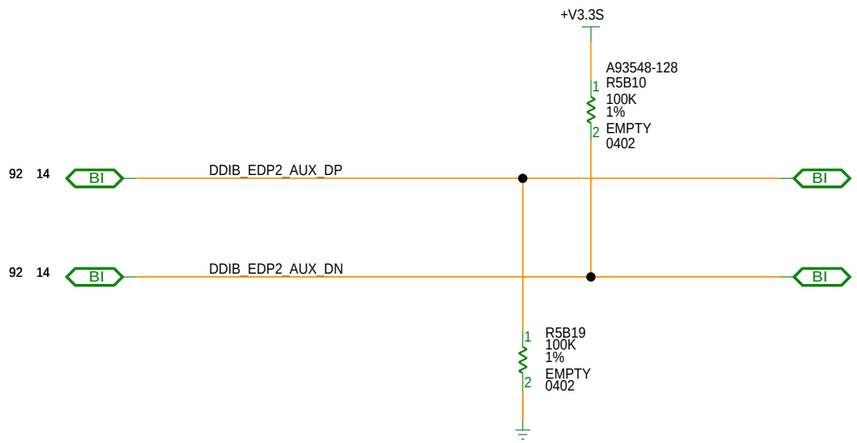
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.90
Tue Oct 15 12:49:45 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	90	1.0

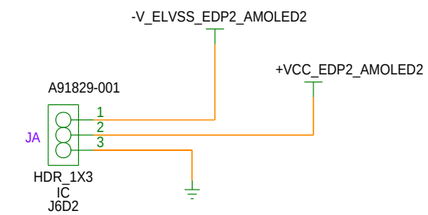
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

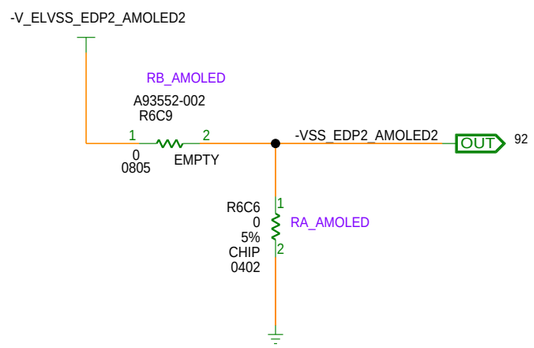
PU/PD FOR AUX CHANNEL - EDP 2

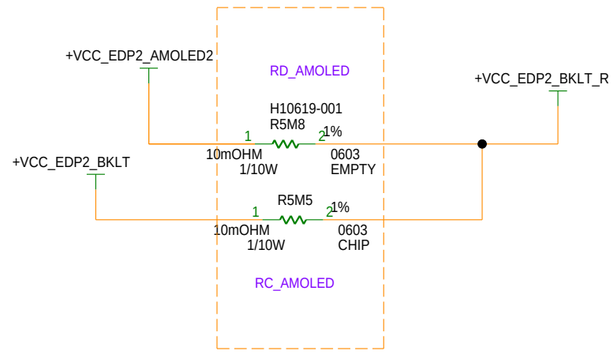


ADDITIONAL AMOLED POWER REQUIREMENTS

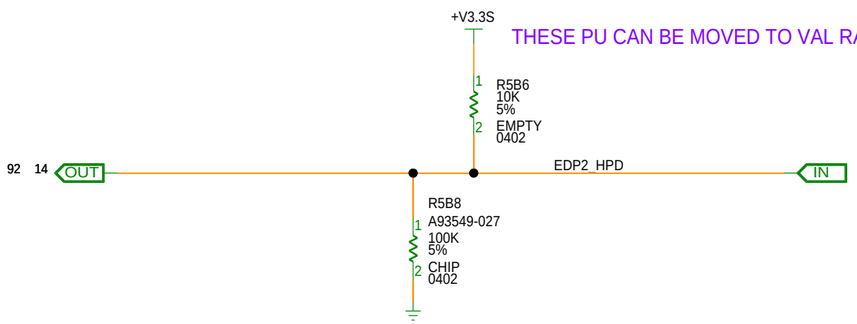


	STUFF	UNSTUFF
NORMAL EDP PANEL	RA_AMOLED & RC_AMOLED	RB_AMOLED & RD_AMOLED
AMOLED EDP PANEL	RB_AMOLED & RD_AMOLED	RA_AMOLED & RC_AMOLED

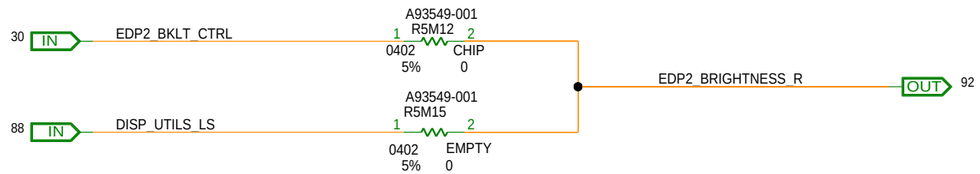


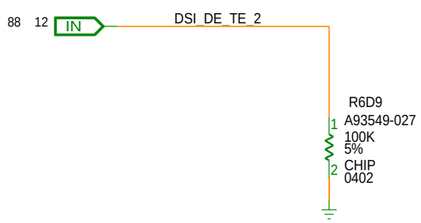


EDP 2 HPD



BACKLIGHT CONTROL USING DISPLAY UTILITY PIN





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Wed Dec 18 18:06:48 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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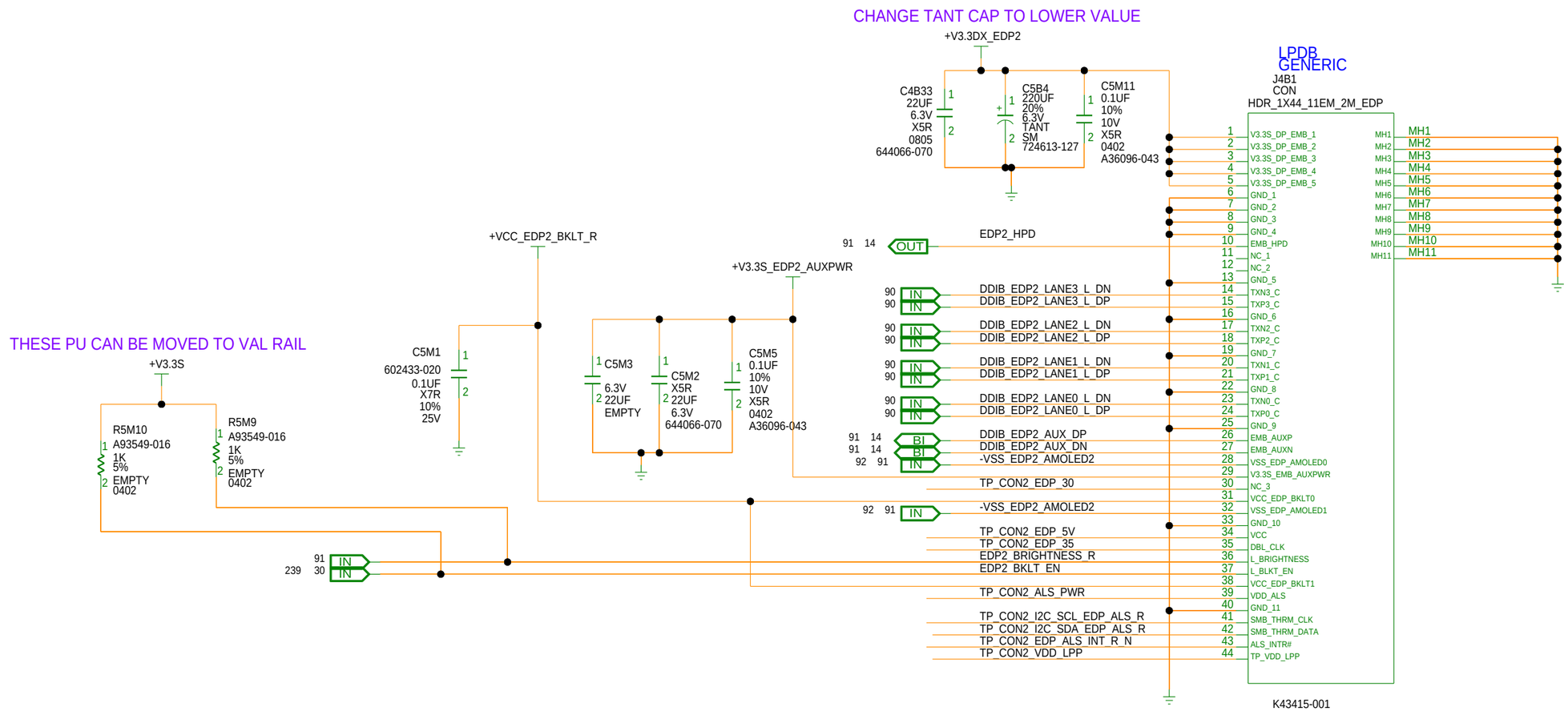
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

EDP CONNECTOR 2



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Wed Dec 18 18:06:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.93
Tue Oct 15 12:49:48 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS

MODULE NAME	REV	DATE

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BPAGE DRAWING
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Tue Oct 15 12:49:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS

MODULE NAME	REV	DATE

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BPAGE DRAWING
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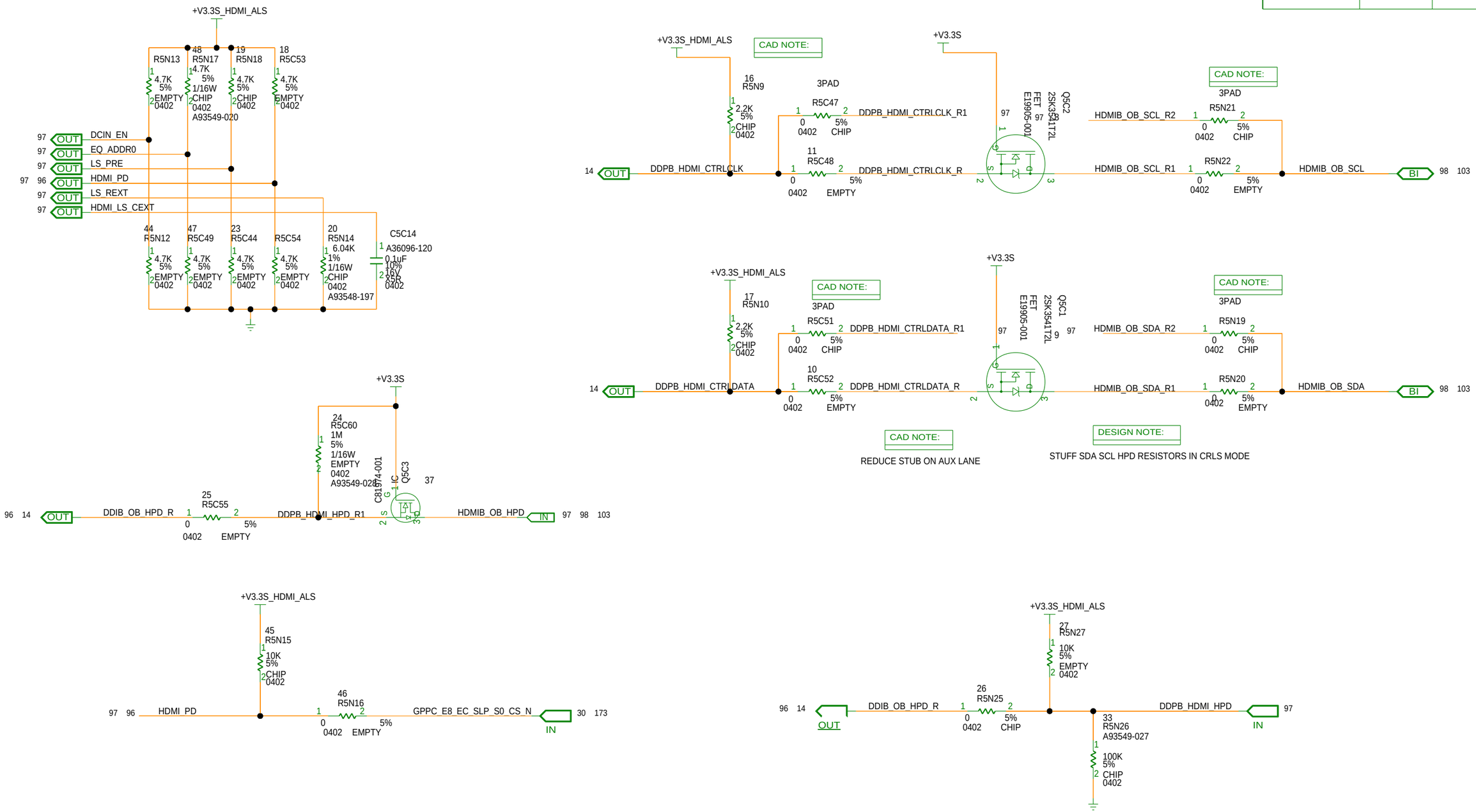
Tue Oct 15 12:49:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	95	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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BPAGE DRAWING
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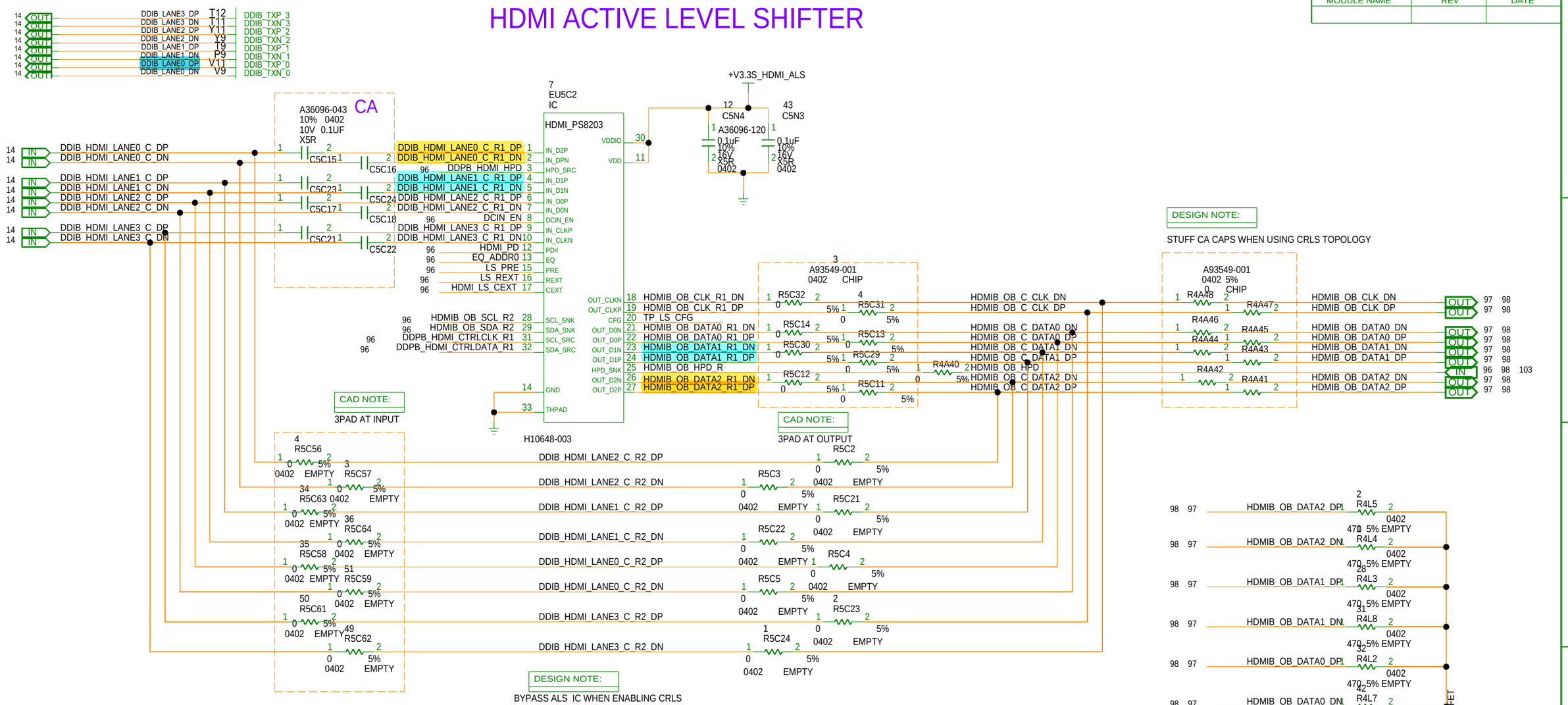
Wed Dec 18 18:06:53 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	96	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

HDMI ACTIVE LEVEL SHIFTER



DESIGN NOTE:

STUFF CA CAPS WHEN USING CRLS TOPOLOGY

CAD NOTE:

3PAD AT INPUT

CAD NOTE:

3PAD AT OUTPUT

DESIGN NOTE:

BYPASS ALS IC WHEN ENABLING CRLS

[PAGE_TITLE=DISPLAY - HDMI CONNECTOR - ALS AND CRLS]

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.97
Wed Dec 18 18:06:54 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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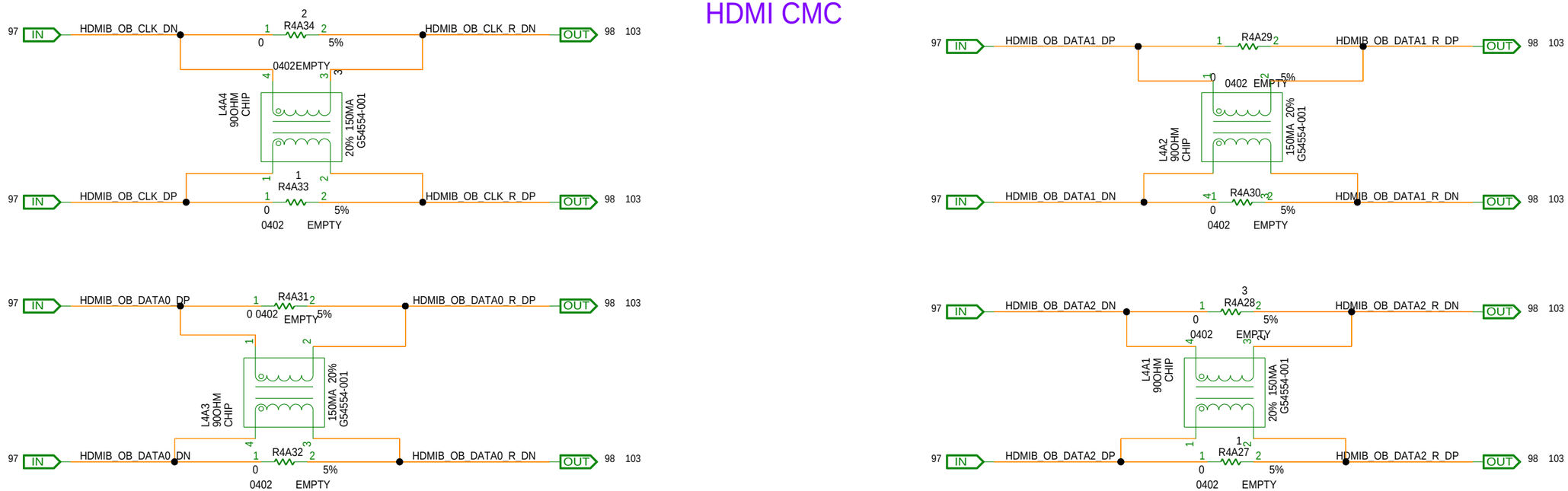
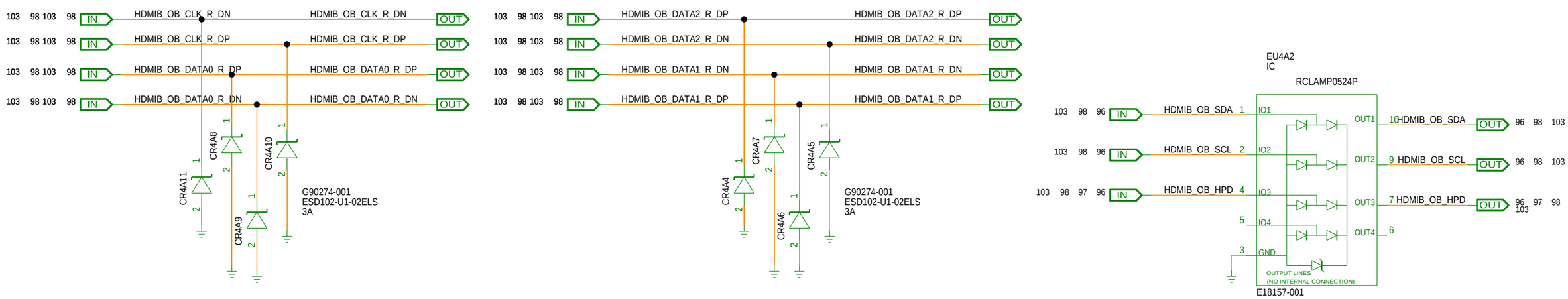
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

HDMI CMC



HDMI ESD



[PAGE_TITLE=DISPLAY - HDMIC CONNECTOR - CMC & ESD]

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Wed Dec 18 18:06:55 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	98	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DP CONNECTOR 2 - CMC

[PAGE_TITLE=DISPLAY - DP CONNECTOR 2 CMC]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.99
Tue Oct 15 12:49:53 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

DP CONNECTOR 2 - ESD

[PAGE_TITLE=DISPLAY - DP CONNECTOR 2 - ESD]

BPAGE DRAWING
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Tue Oct 15 12:49:54 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

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BPAGE DRAWING
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DISPLAY - DDI 1&2 HPD & CONNECTOR

MODULE REV DETAILS		
MODULE NAME	REV	DATE

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Tue Oct 15 12:49:56 2019

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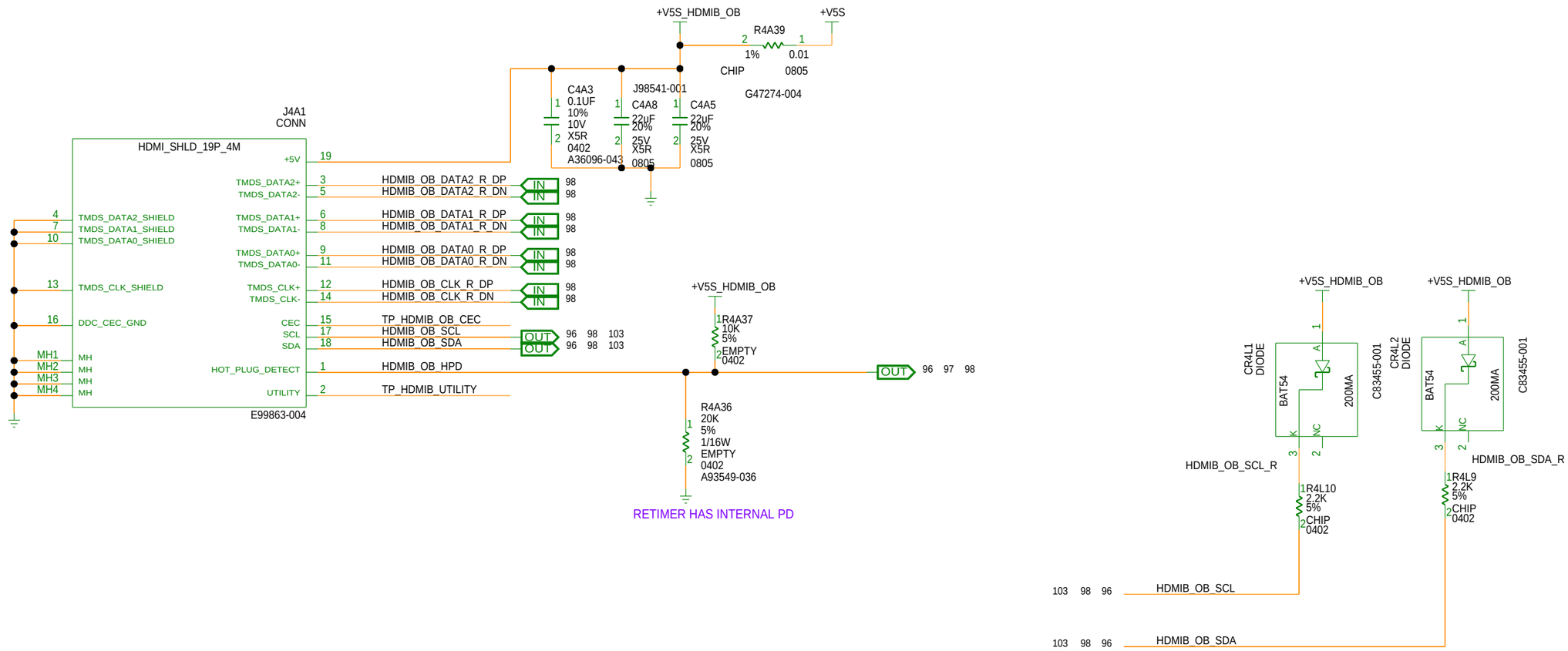
MODULE NAME	REV	DATE



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BPAGE DRAWING
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Wed Dec 18 18:06:59 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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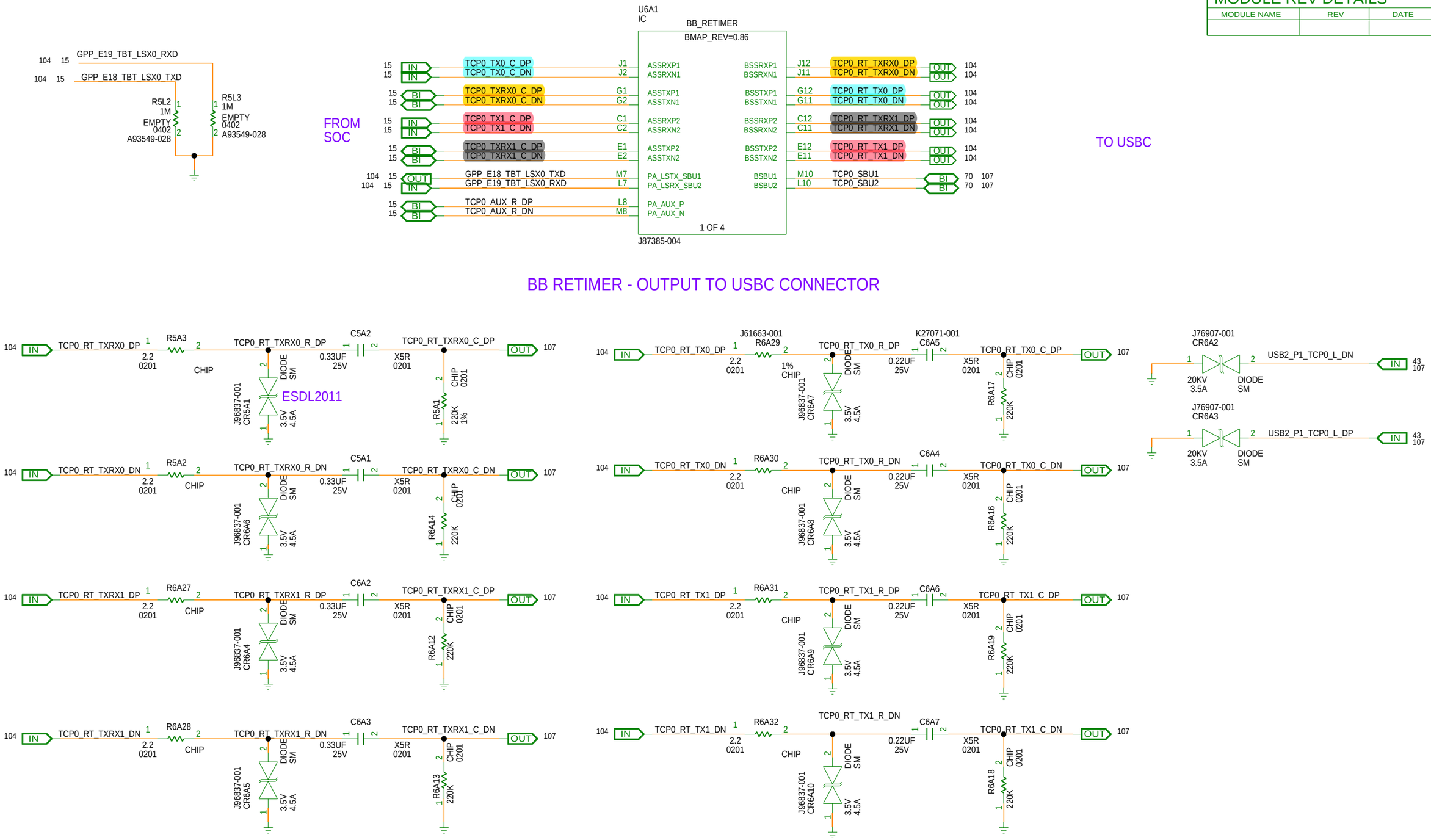
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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tigerlake_u_ddr4.sch_1.104
Wed Dec 18 18:07:00 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

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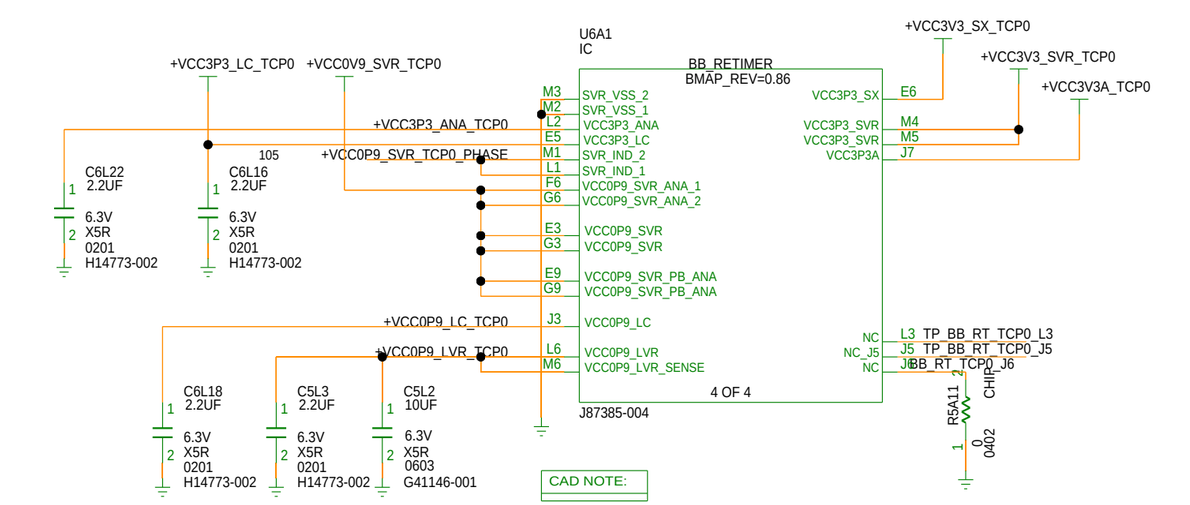
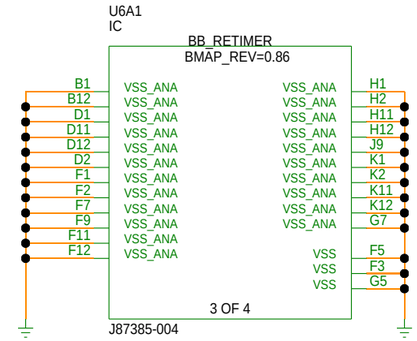
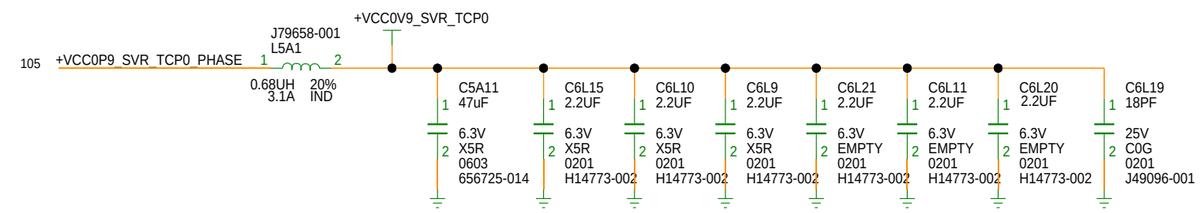
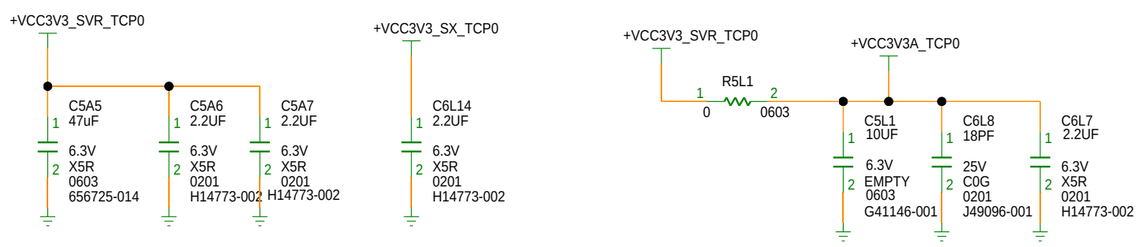
MODULE NAME	REV	DATE

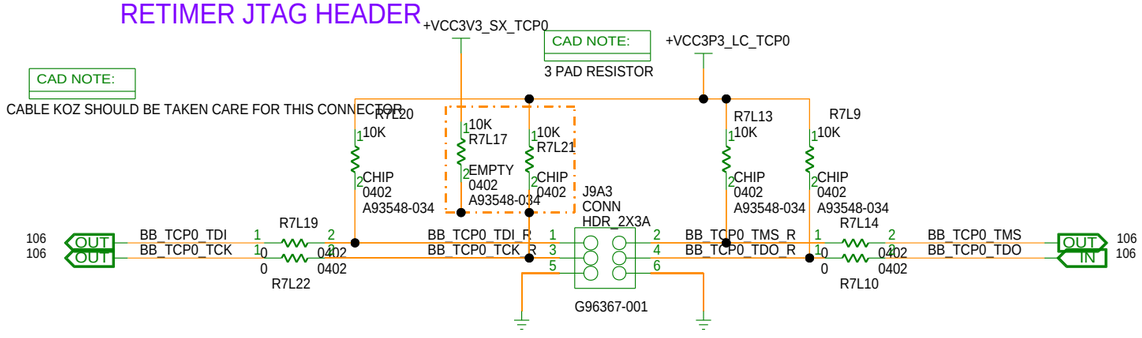




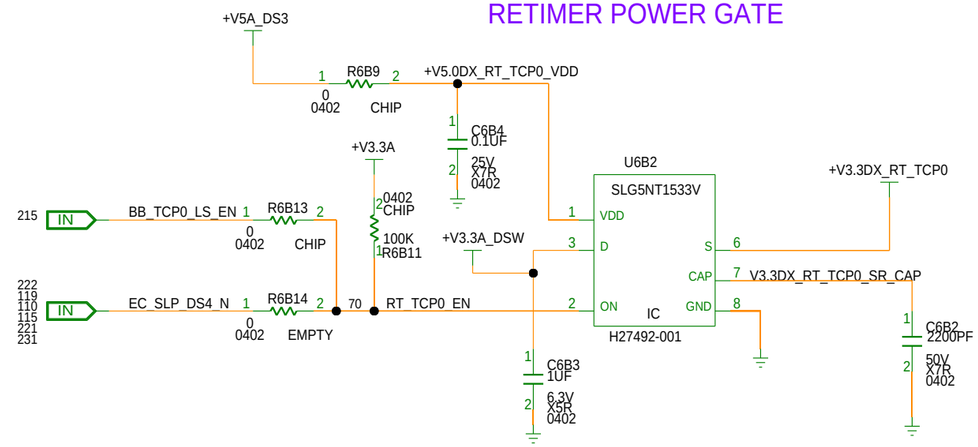


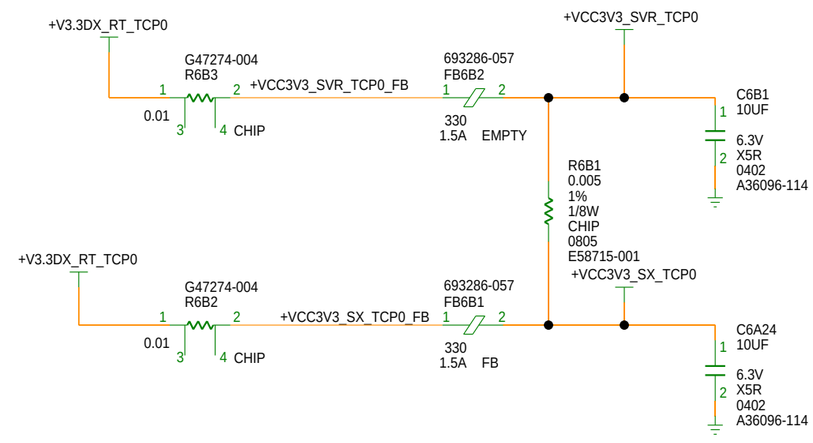


RETIMER JTAG HEADER



RETIMER POWER GATE





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Wed Dec 18 18:07:01 2019

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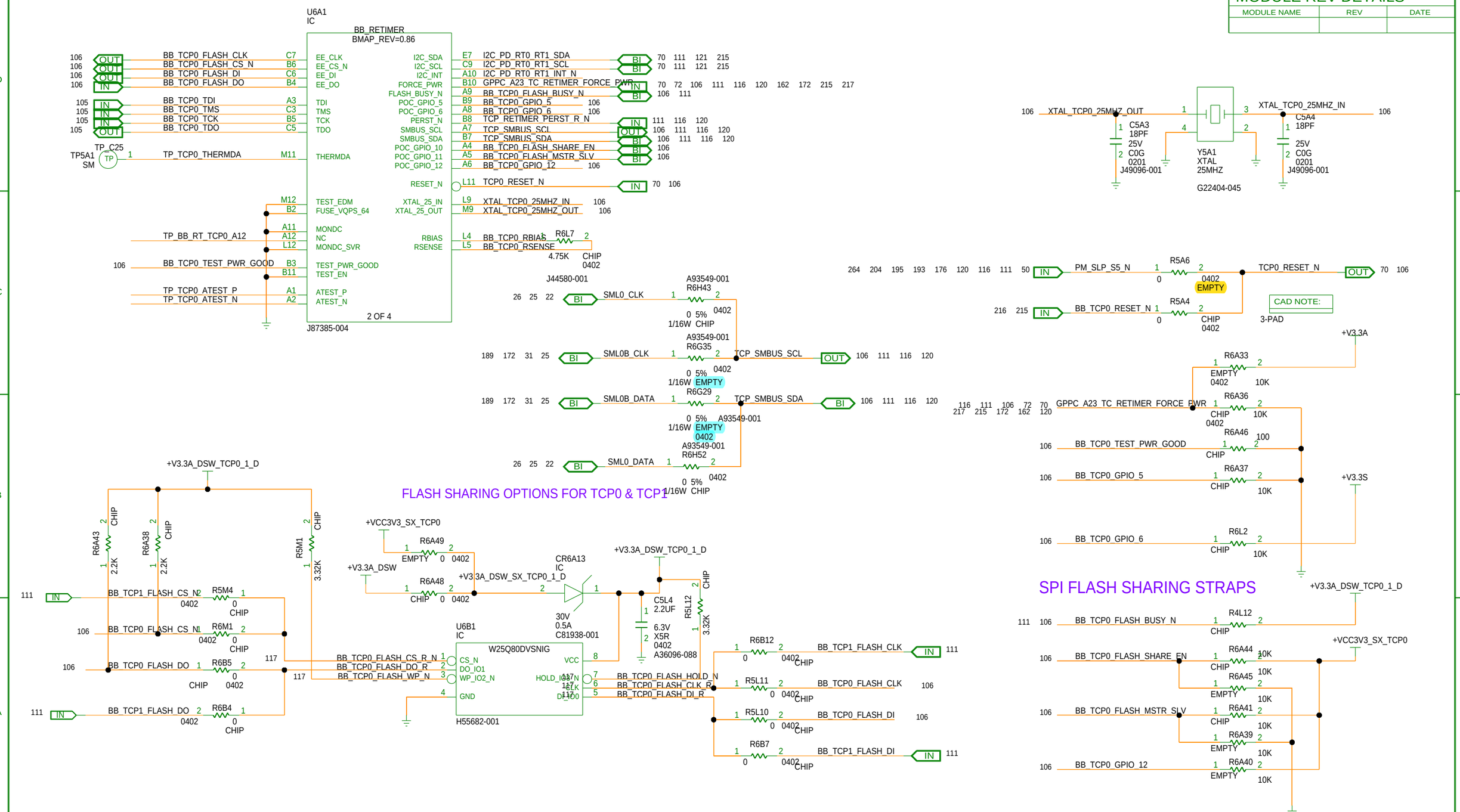
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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Wed Dec 18 18:07:02 2019

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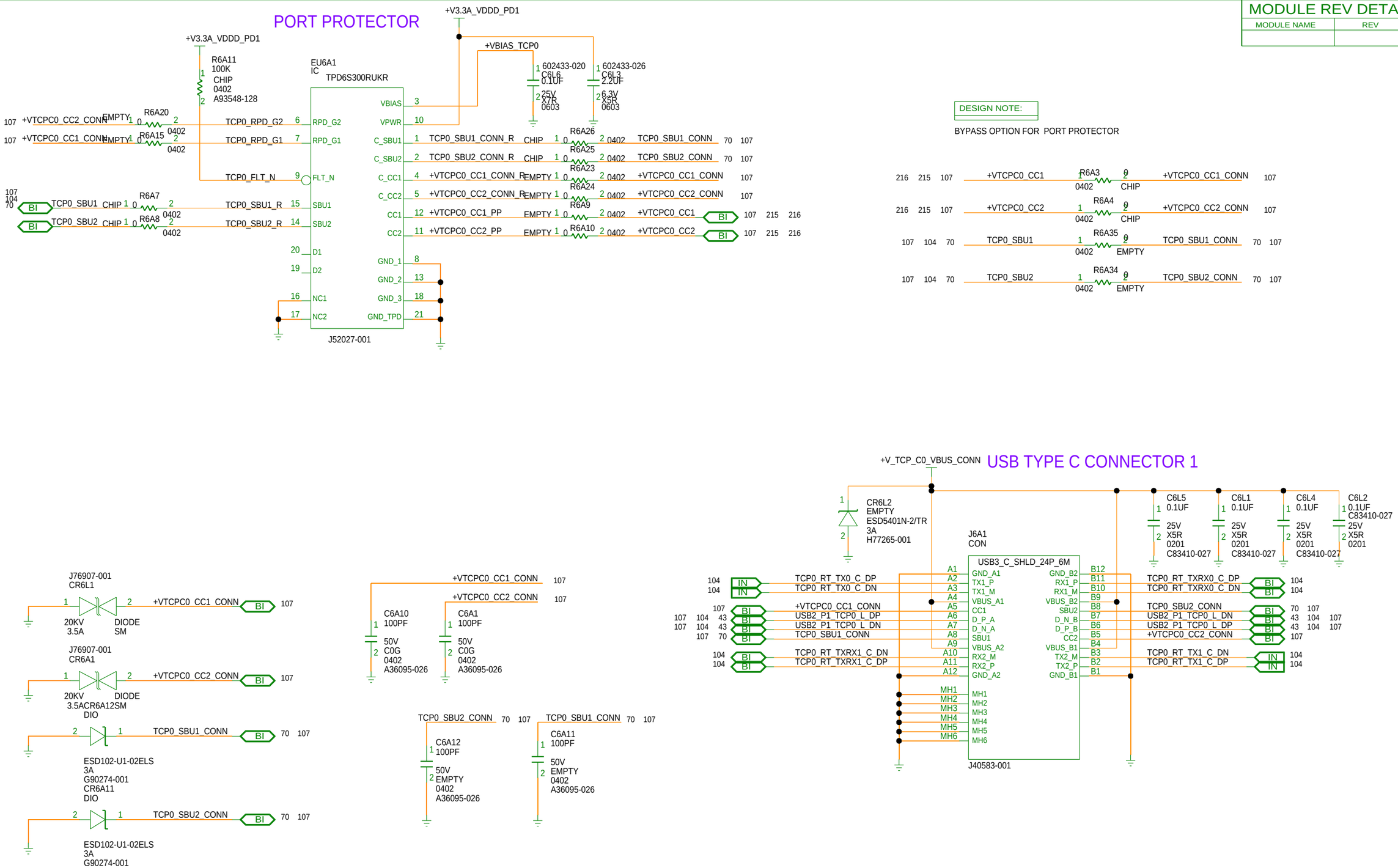
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.107
Wed Dec 18 18:07:03 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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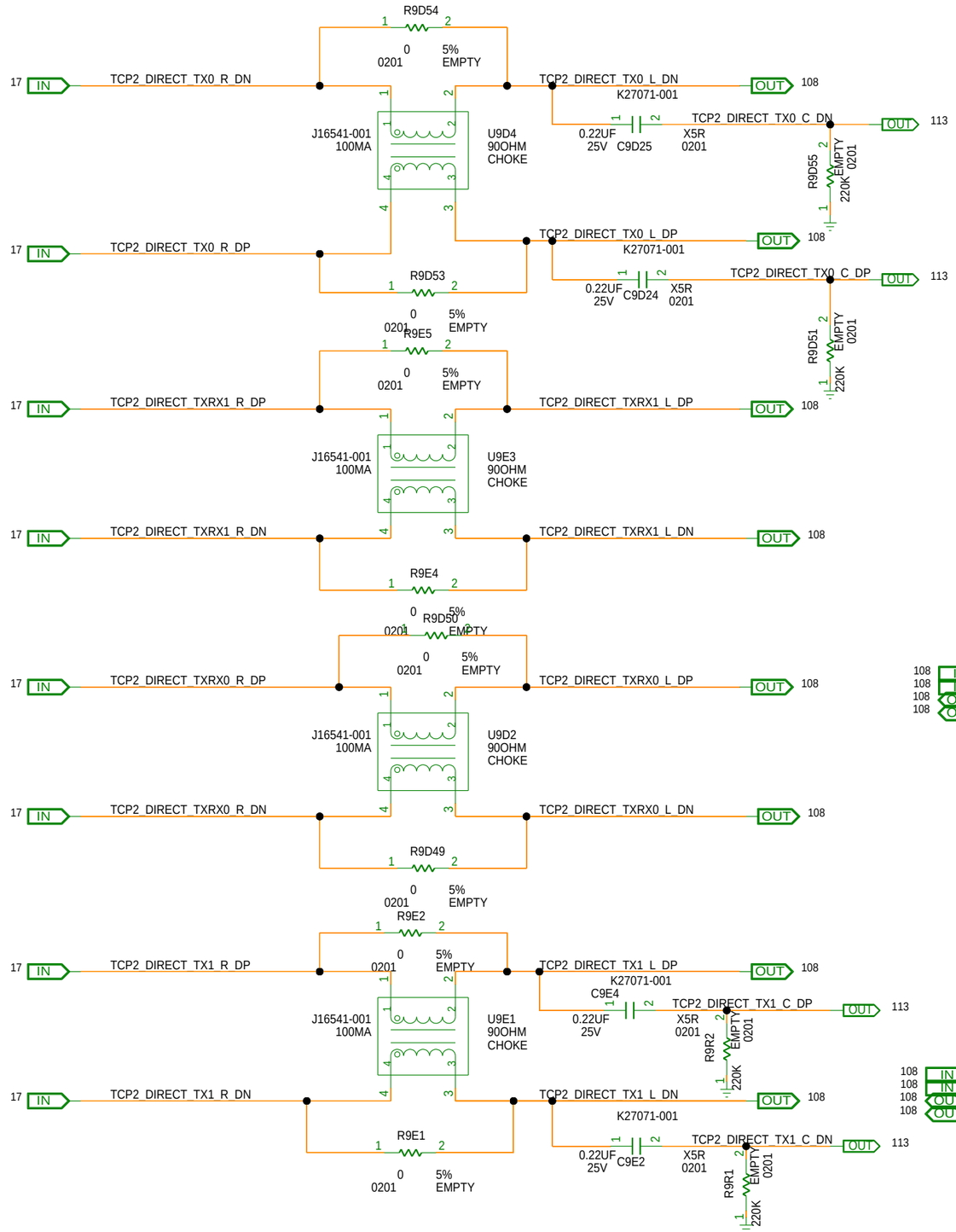
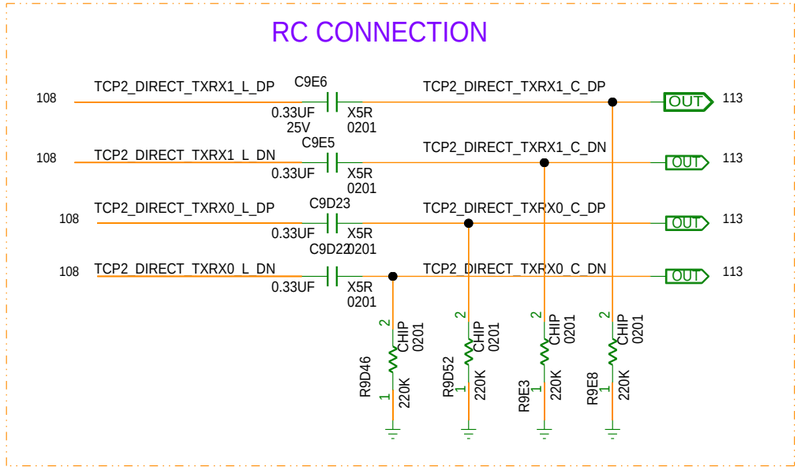
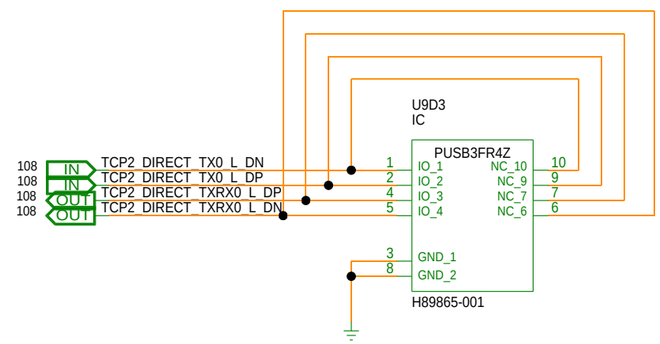
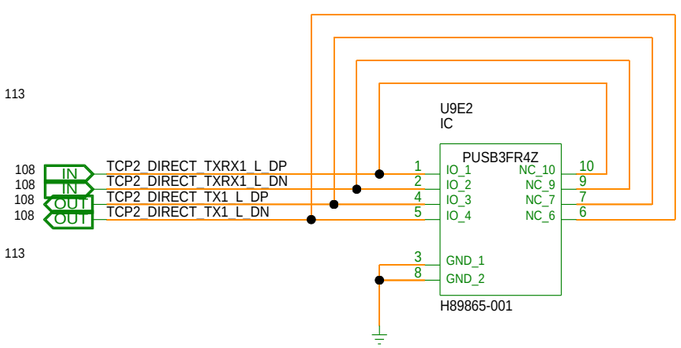
MODULE REV DETAILS		
MODULE NAME	REV	DATE

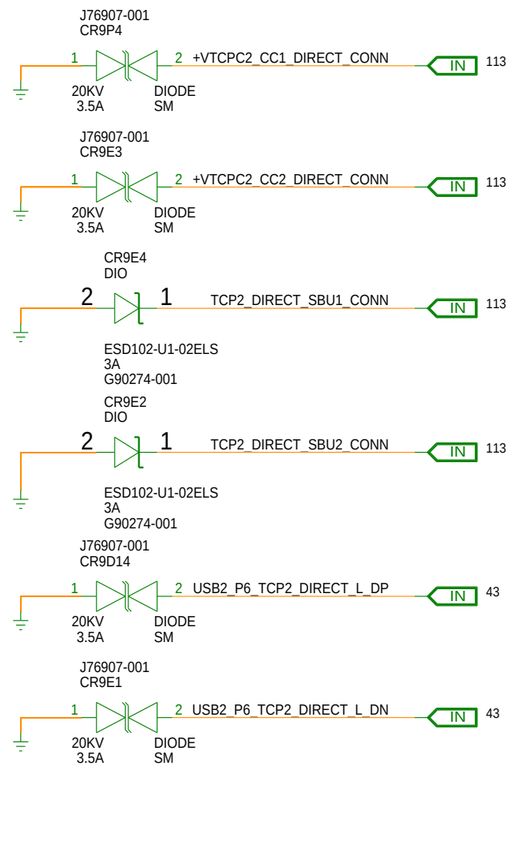


RC CONNECTION









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BPAGE DRAWING
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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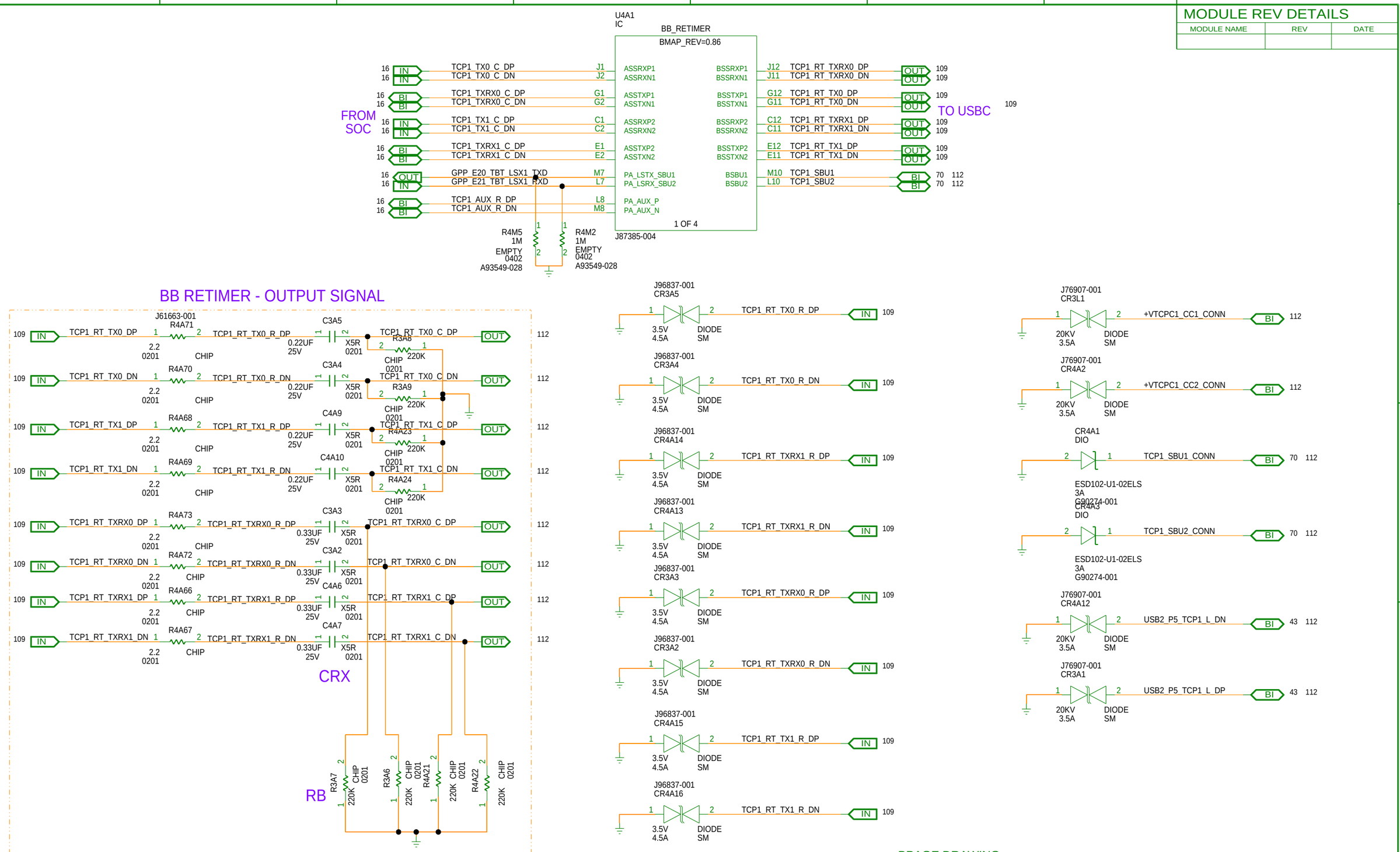
MODULE REV DETAILS		
MODULE NAME	REV	DATE



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BPAGE DRAWING
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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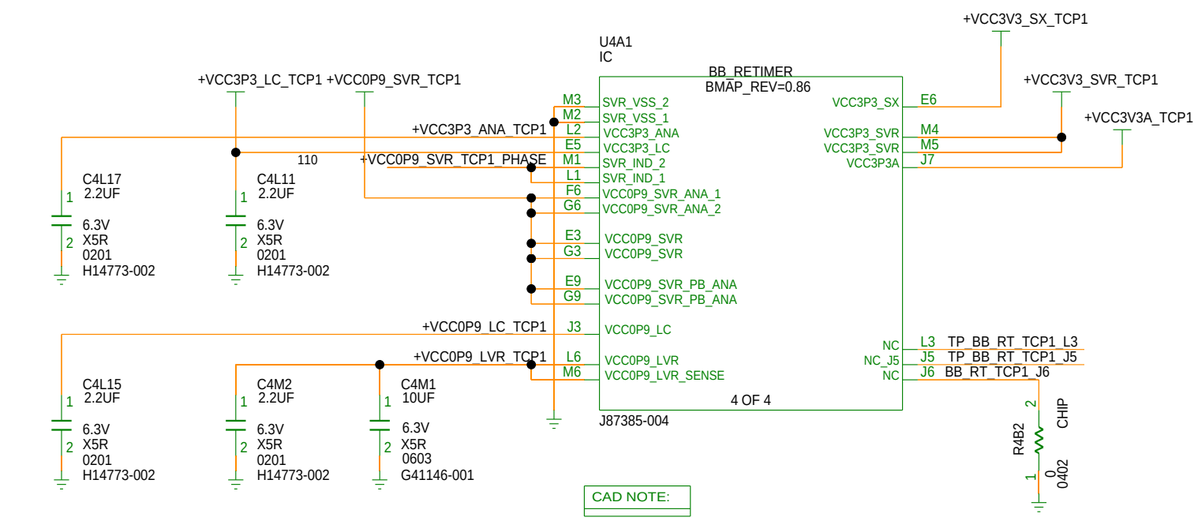
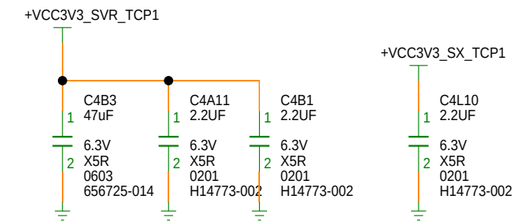
CUSTOM TEXT BPAGE

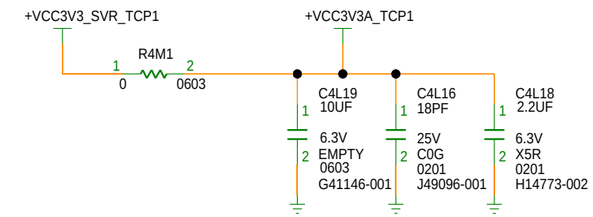
MODULE REV DETAILS		
MODULE NAME	REV	DATE

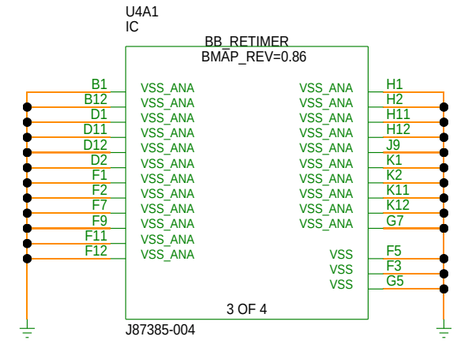


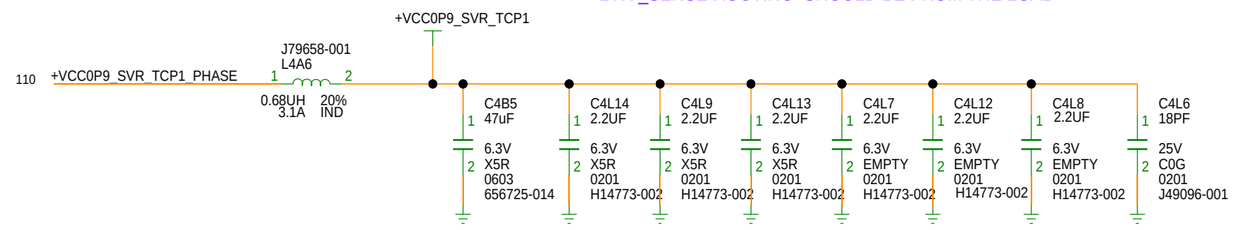
CAD NOTE:

LVR _SENSE ROUTING SHOULD BE FROM THE LOAD

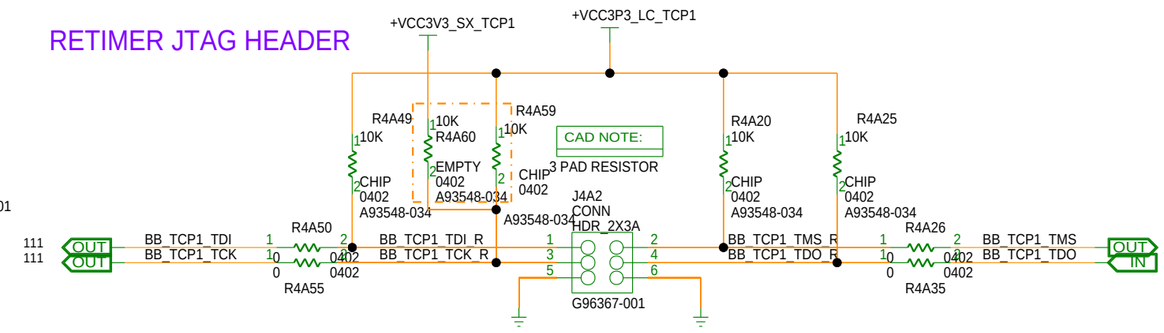






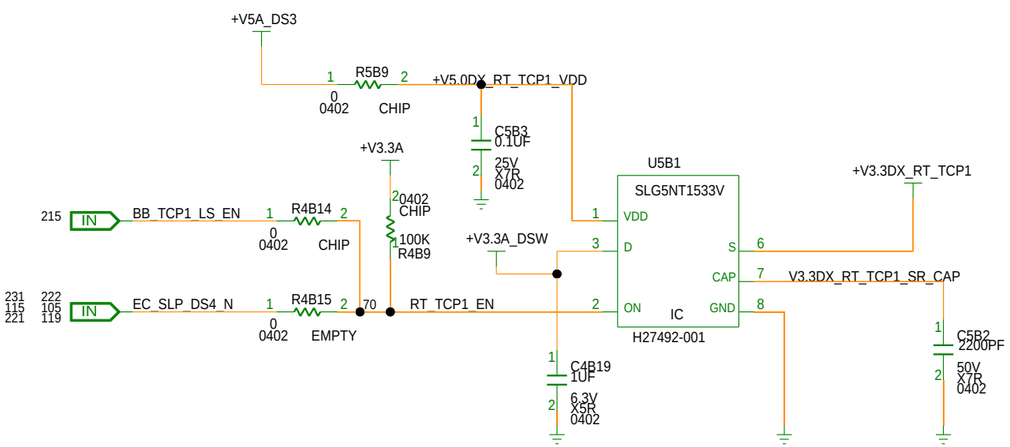


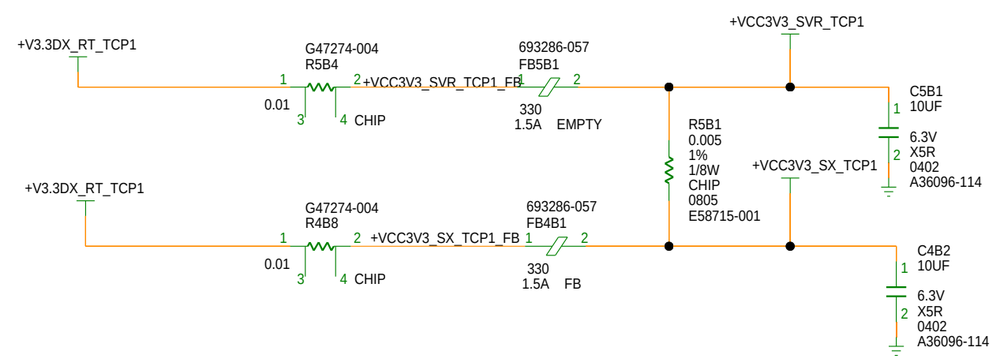
RETIMER JTAG HEADER



CAD NOTE:

CABLE KOZ SHOULD BE TAKEN CARE FOR THIS CONNECTOR





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Wed Dec 18 18:07:06 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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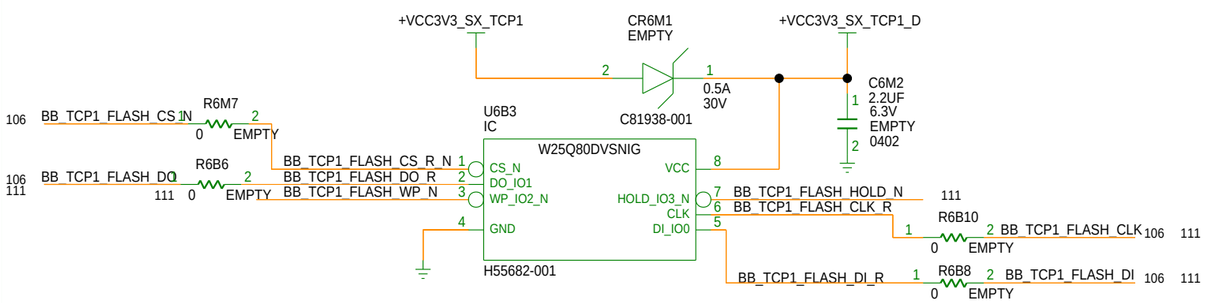
CUSTOM TEXT BPAGE

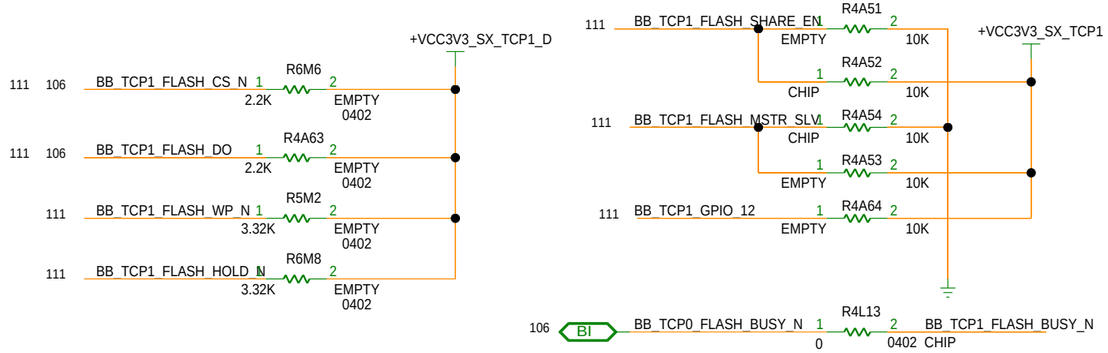
MODULE REV DETAILS		
MODULE NAME	REV	DATE

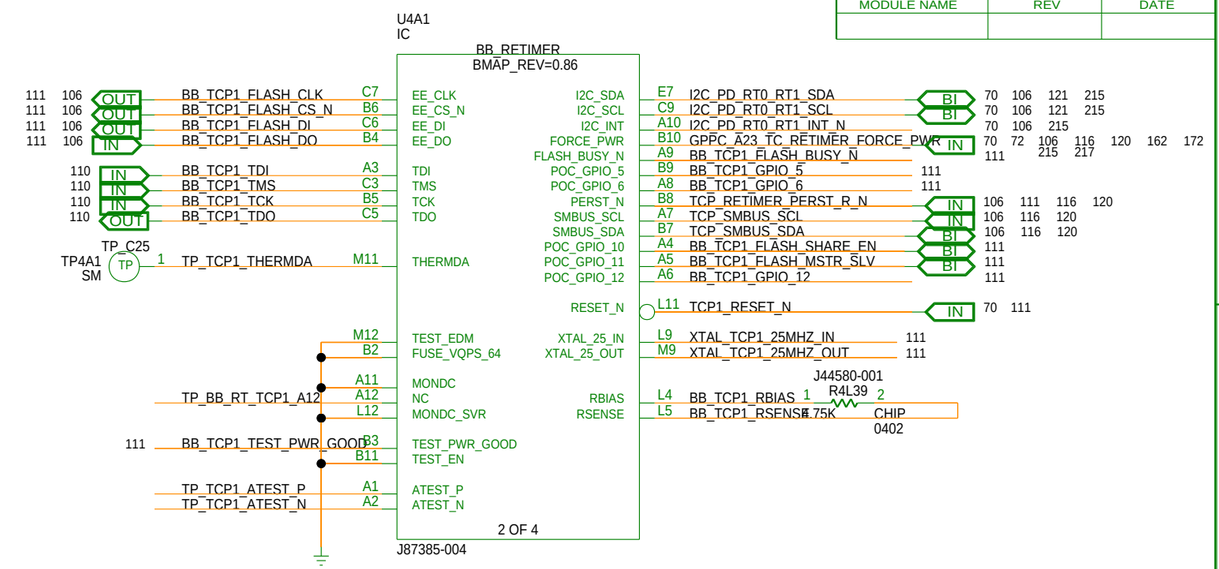
INDEPENDENT FLASH OPTION FOR BB RETIMER

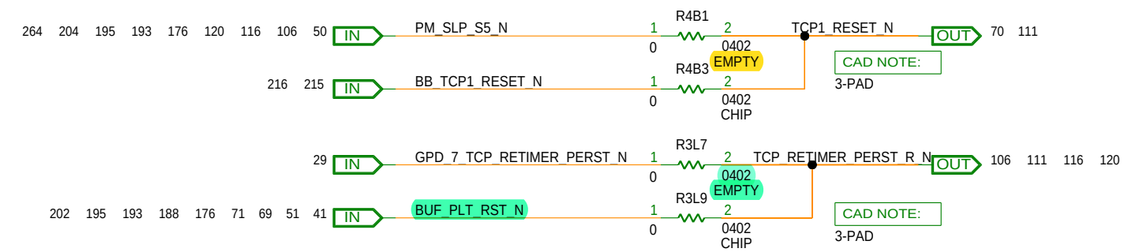
DEFAULT- FLASH SHARING



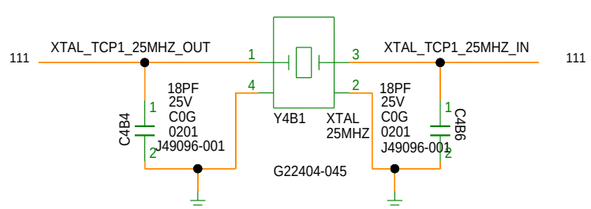
BB RETIMER FLASH SHARING CONFIGURATION

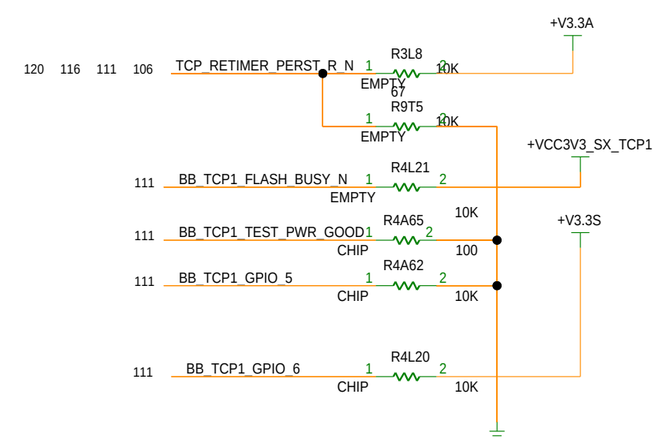






TCP1 RETIMER CRYSTAL





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Wed Dec 18 18:07:07 2019

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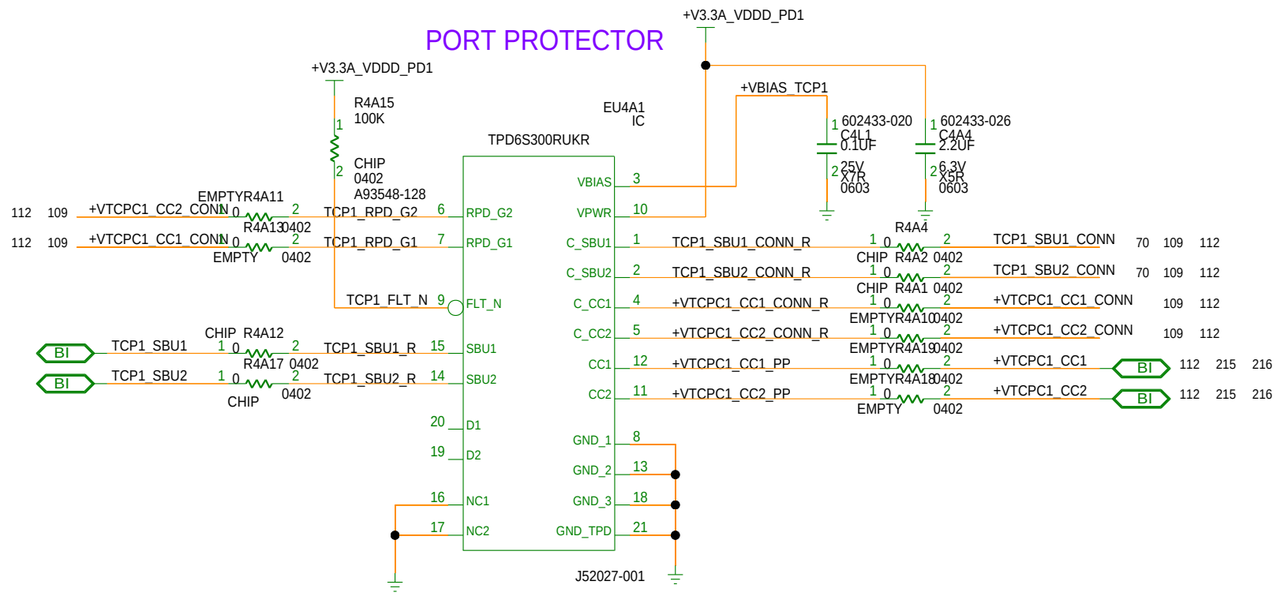
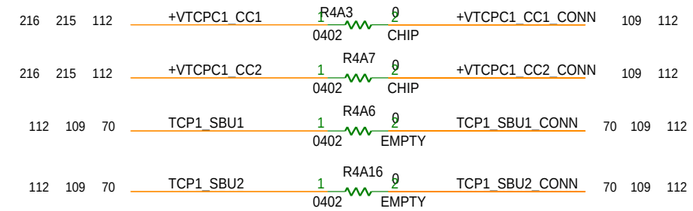
CUSTOM TEXT BPAGE

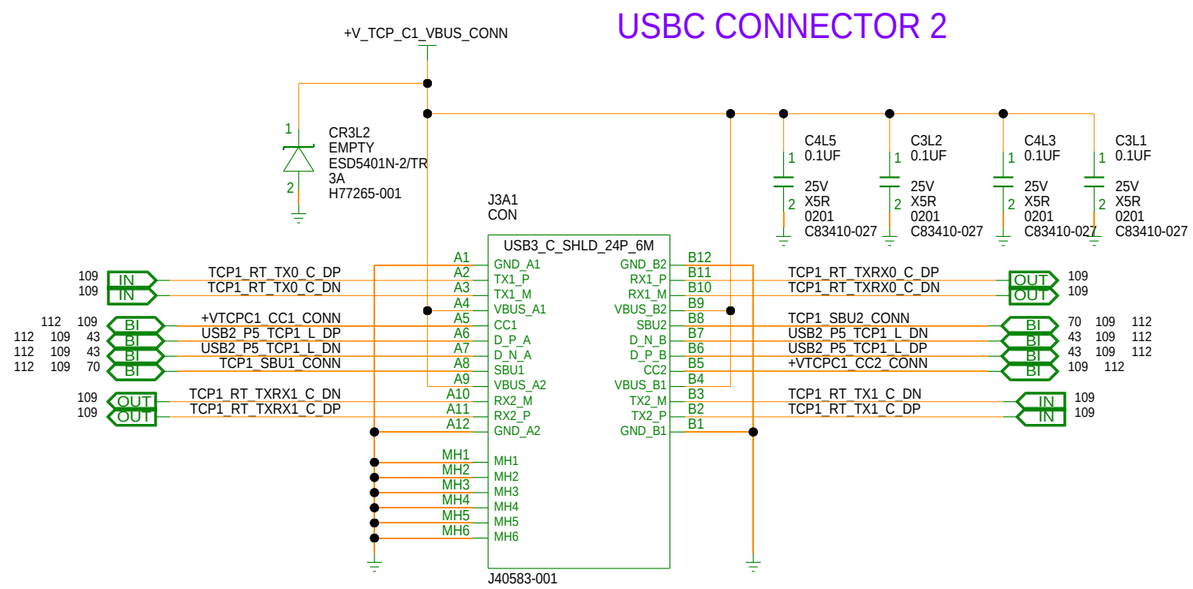
MODULE REV DETAILS		
MODULE NAME	REV	DATE

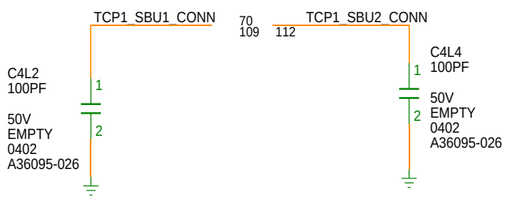


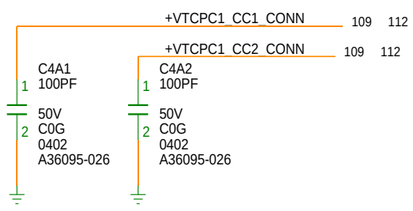
DESIGN NOTE:

BYPASS OPTION FOR PORT PROTECTOR









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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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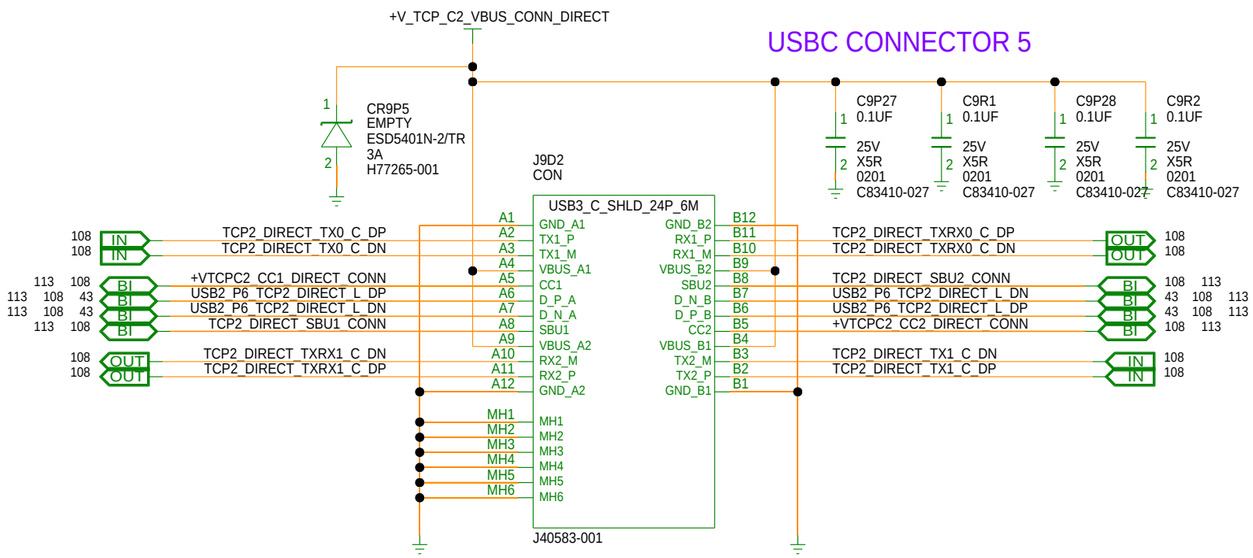
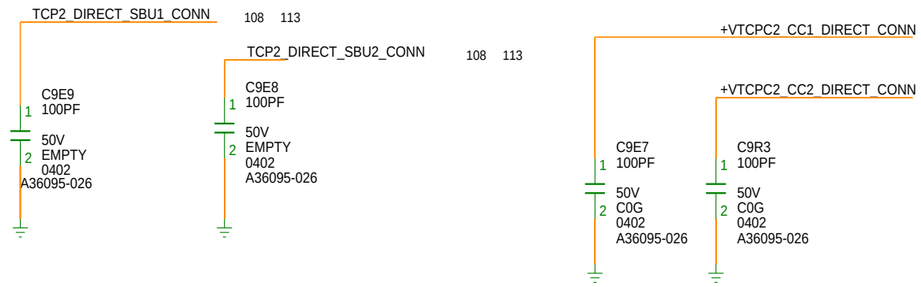
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

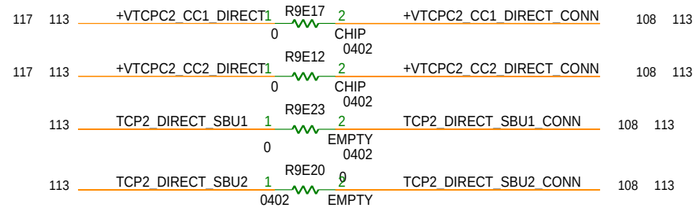
USBC CONNECTOR 5



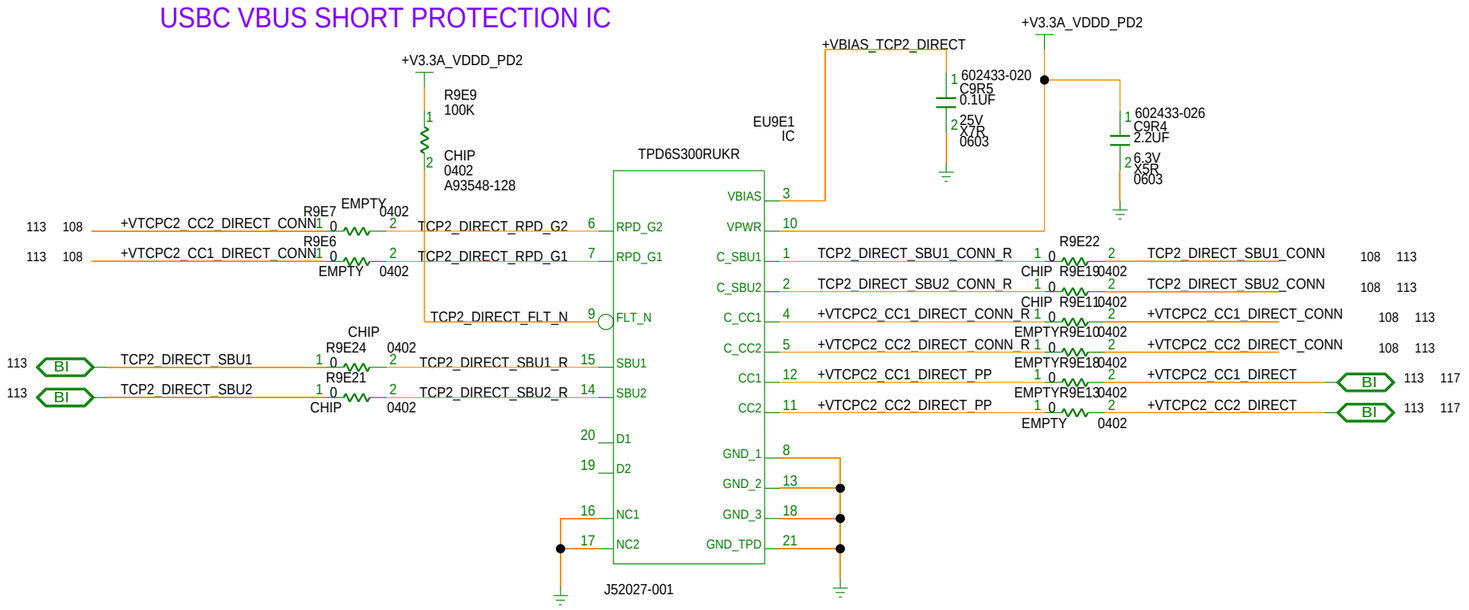


DESIGN NOTE:

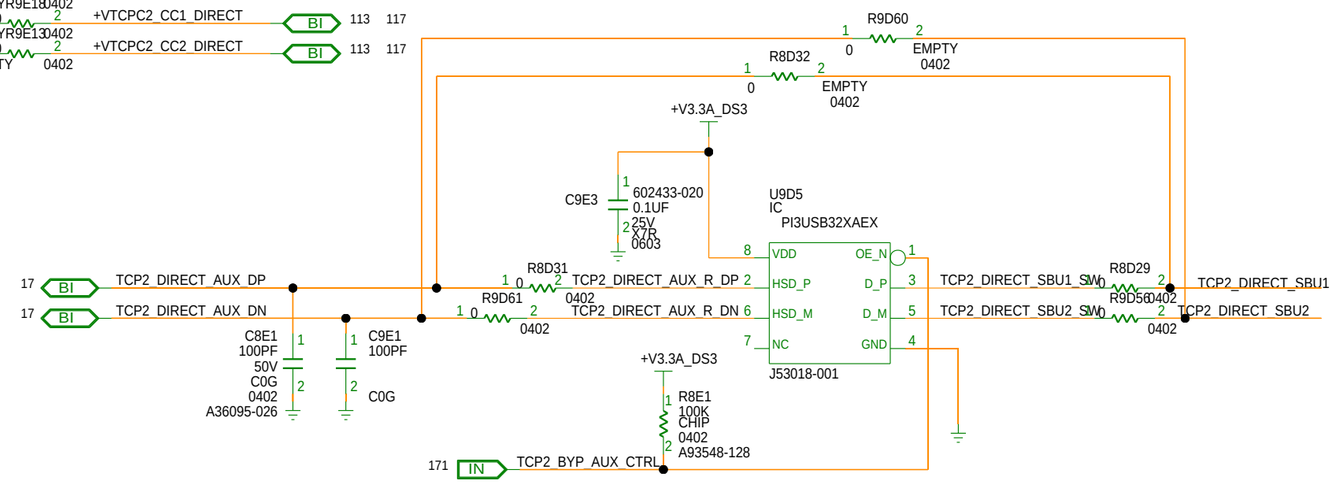
BYPASS OPTION FOR PORT PROTECTOR



USBC VBUS SHORT PROTECTION IC



AUX SWITCH FOR USB/DP MODE



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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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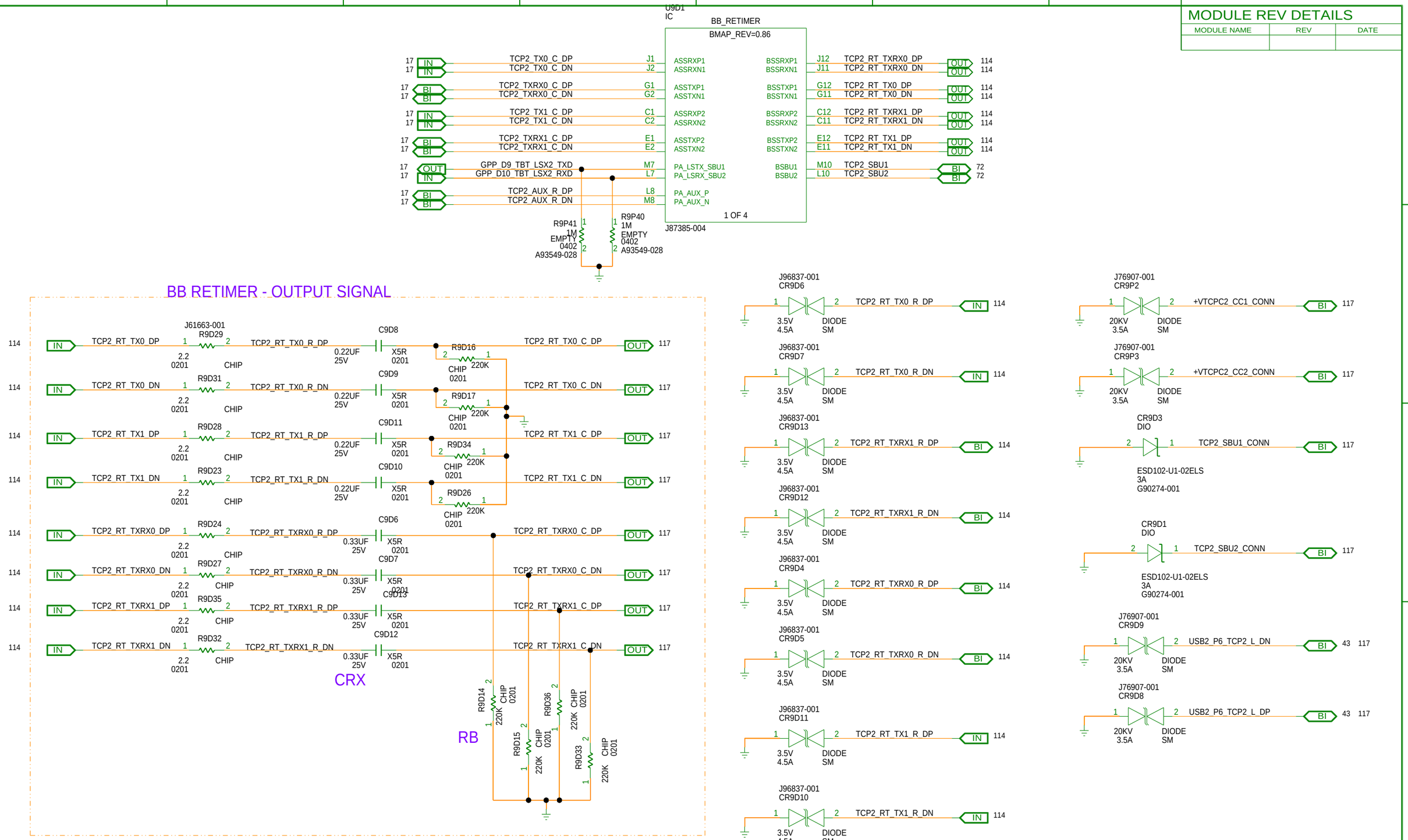
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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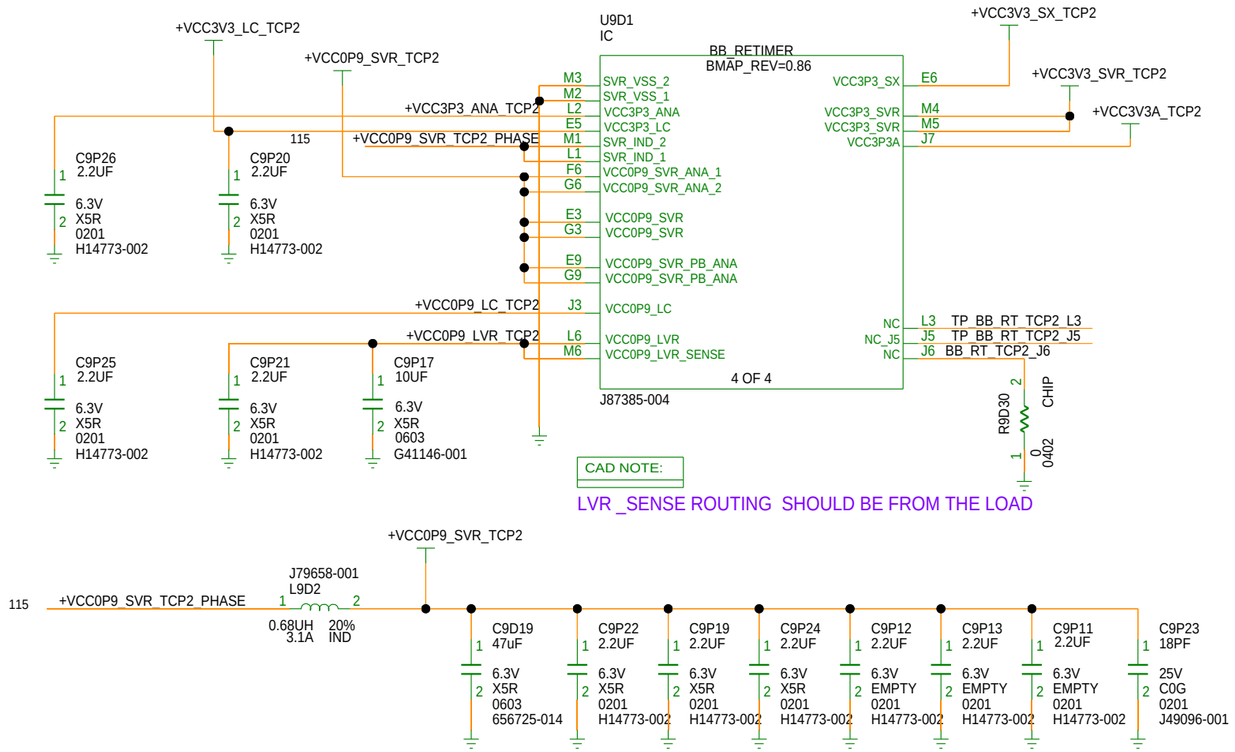
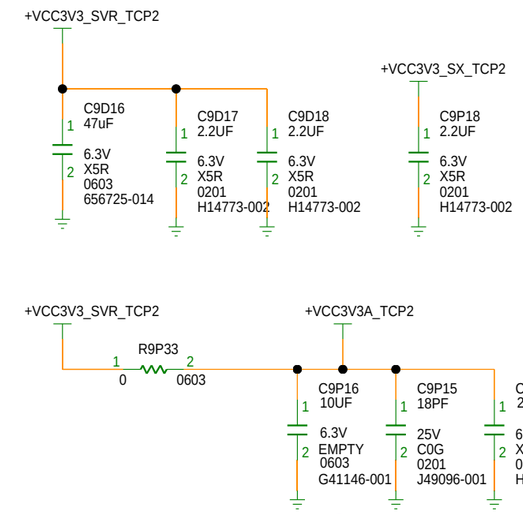
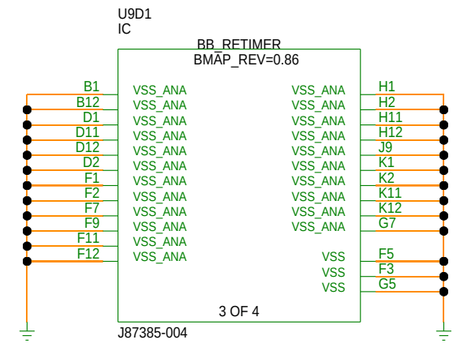
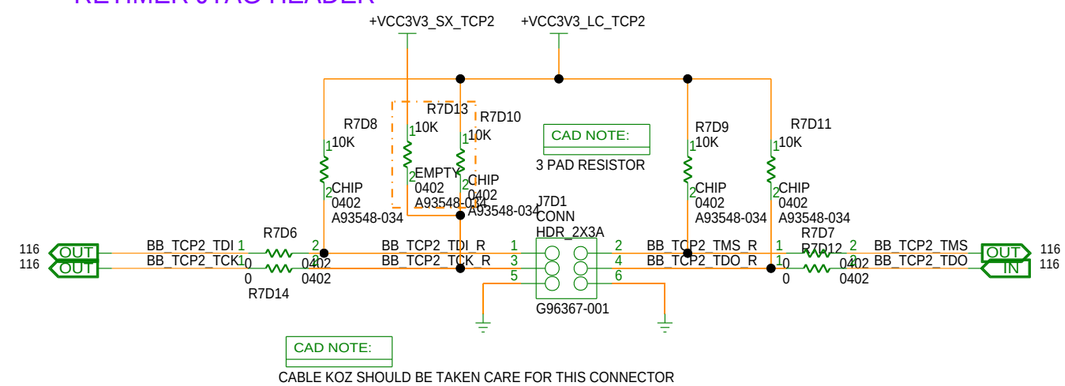
MODULE NAME	REV	DATE

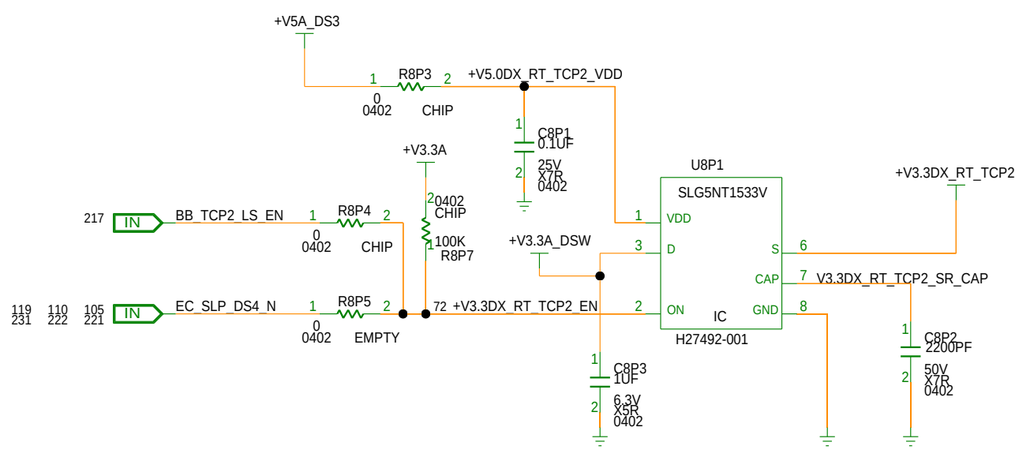


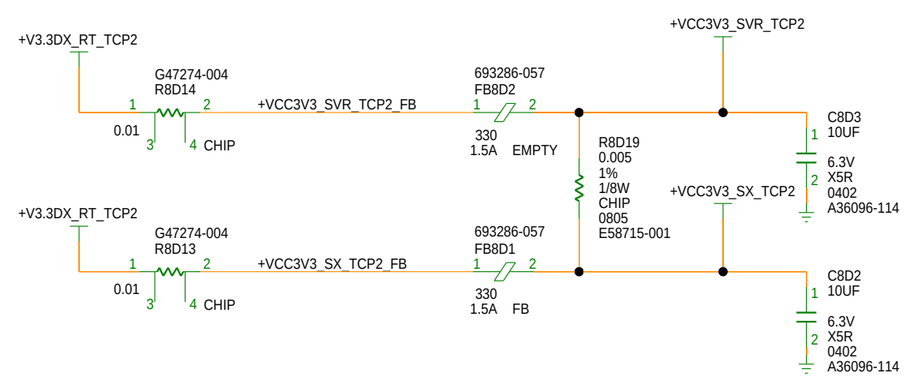




RETIMER JTAG HEADER







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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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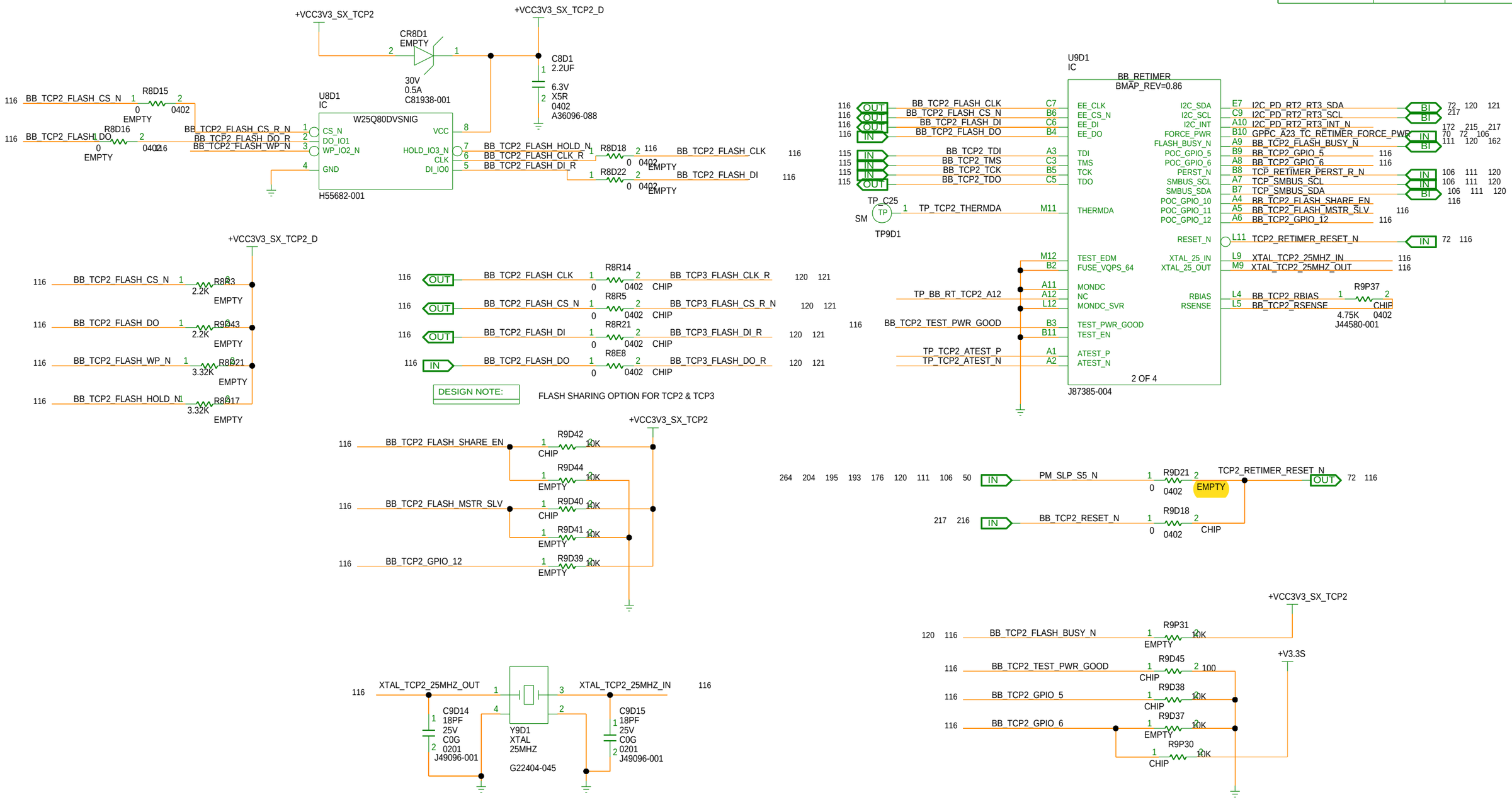

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Wed Dec 18 18:07:12 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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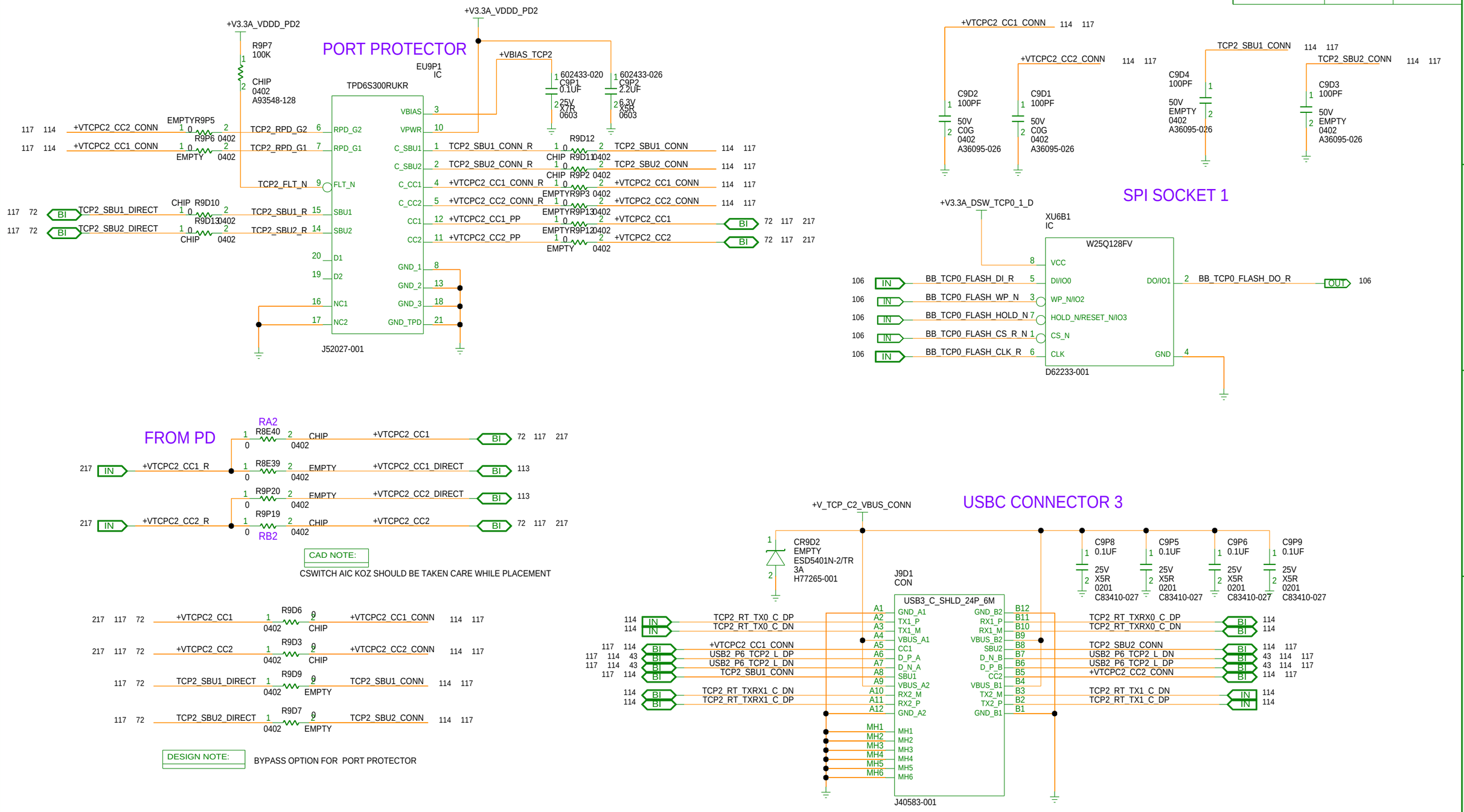
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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Wed Dec 18 18:07:14 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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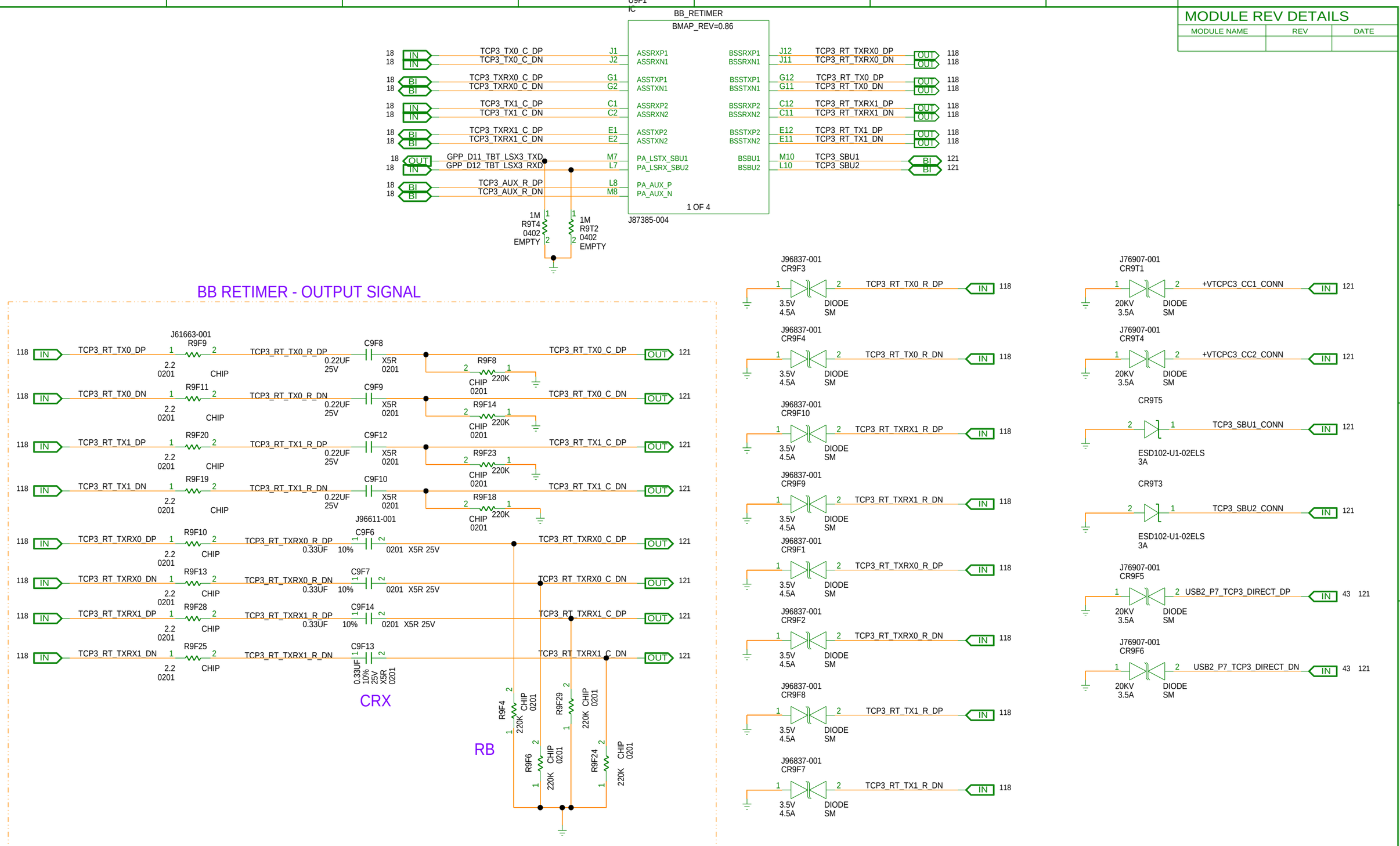
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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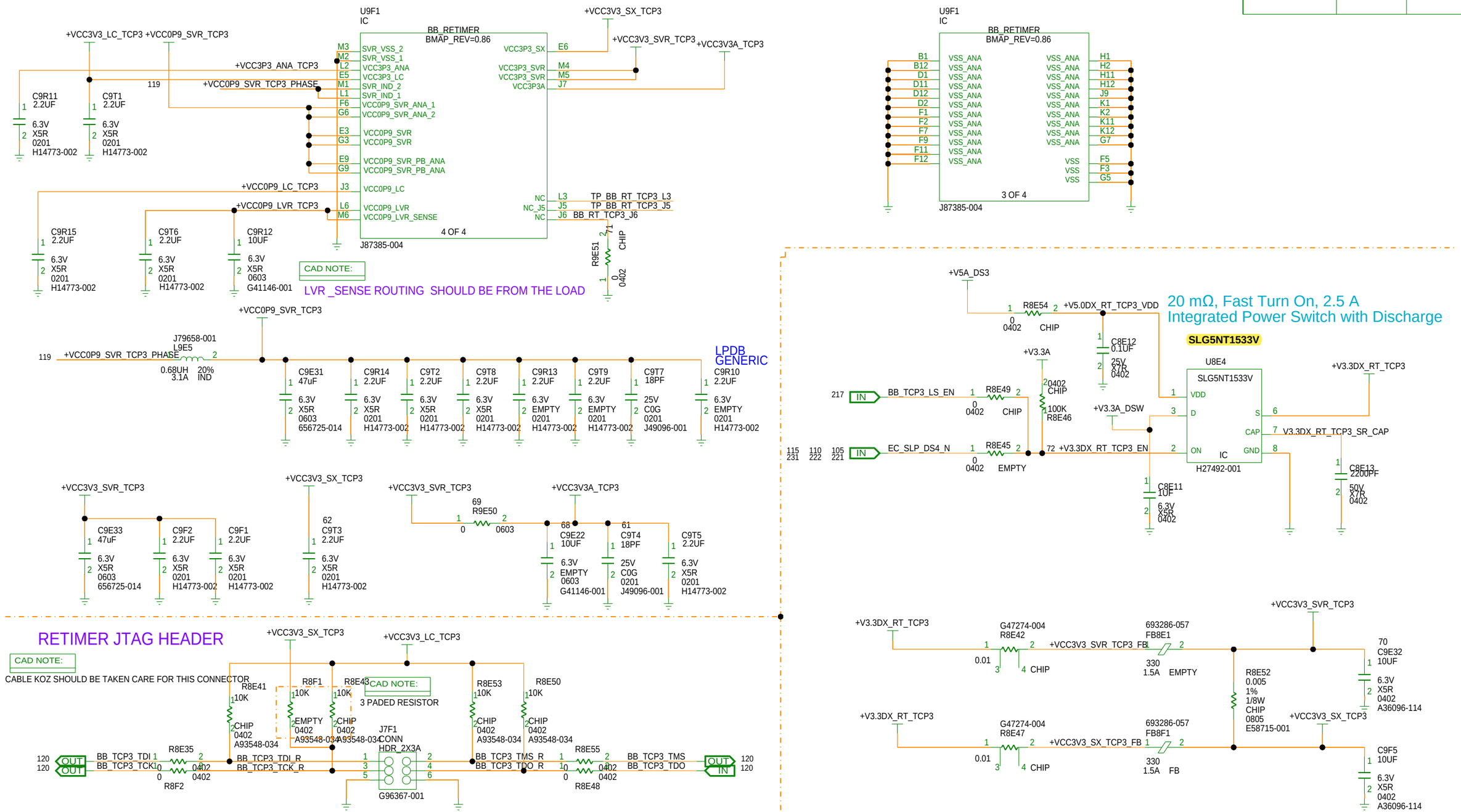
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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BPAGE DRAWING
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Wed Dec 18 18:07:16 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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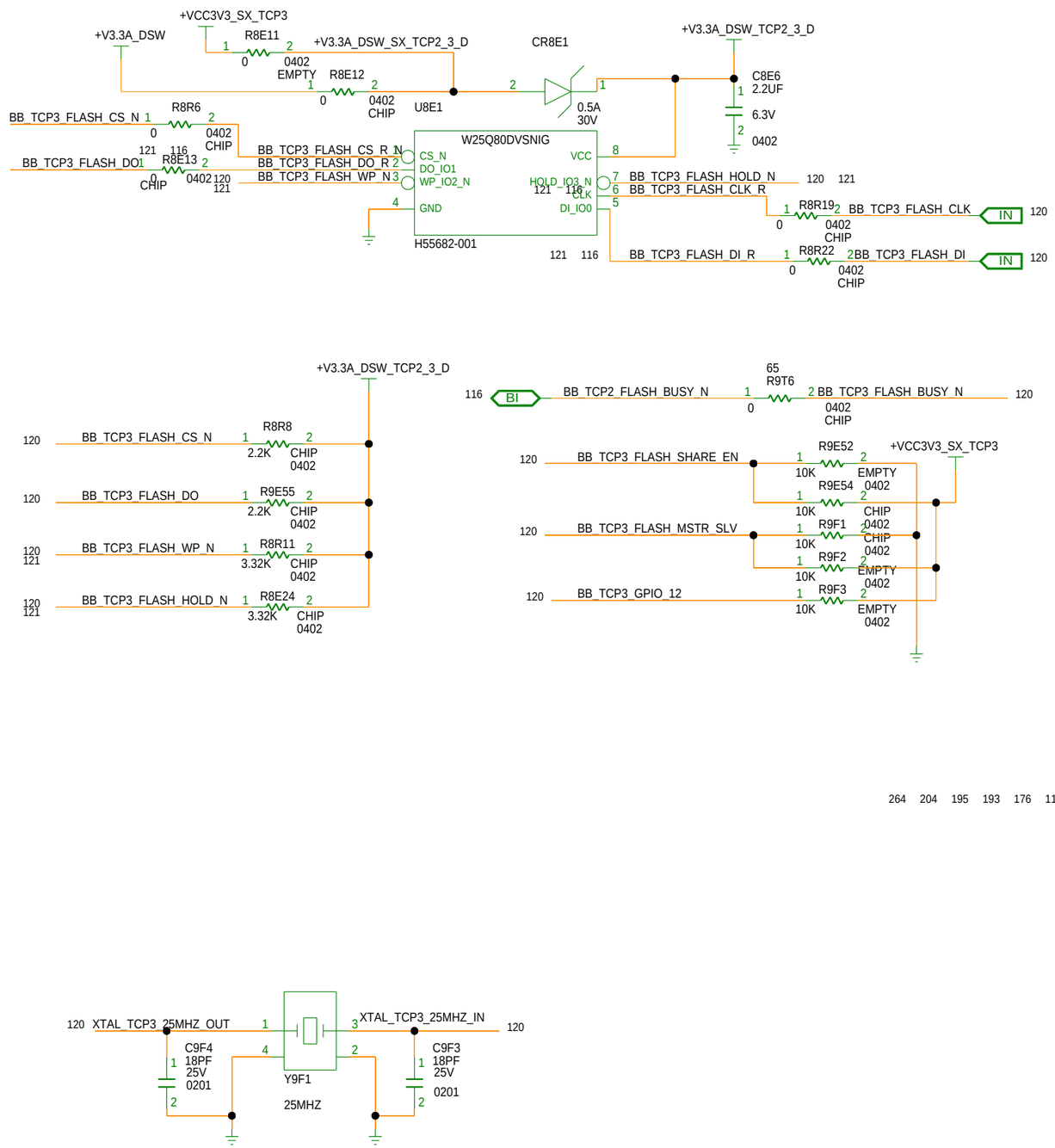
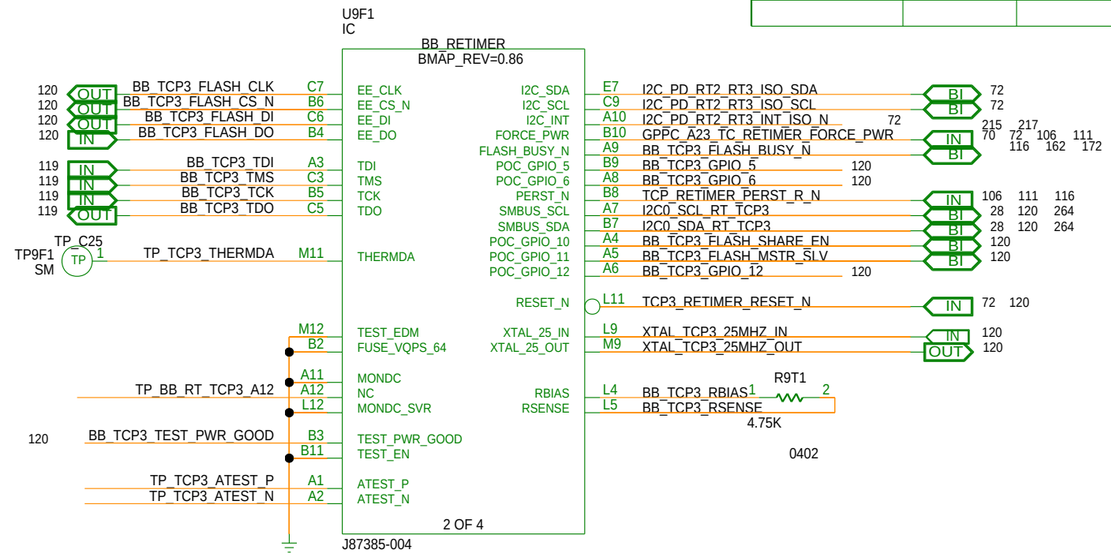
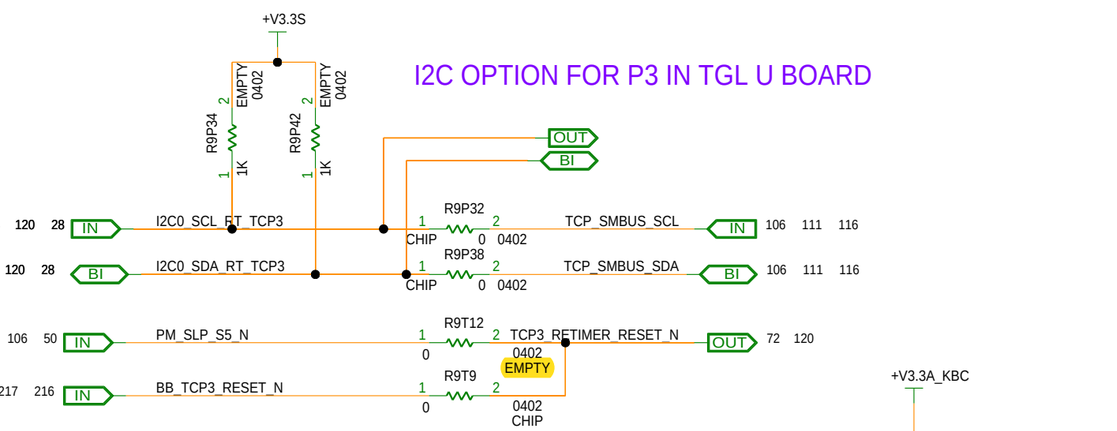
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE







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Wed Dec 18 18:07:17 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

MODULE REV DETAILS		
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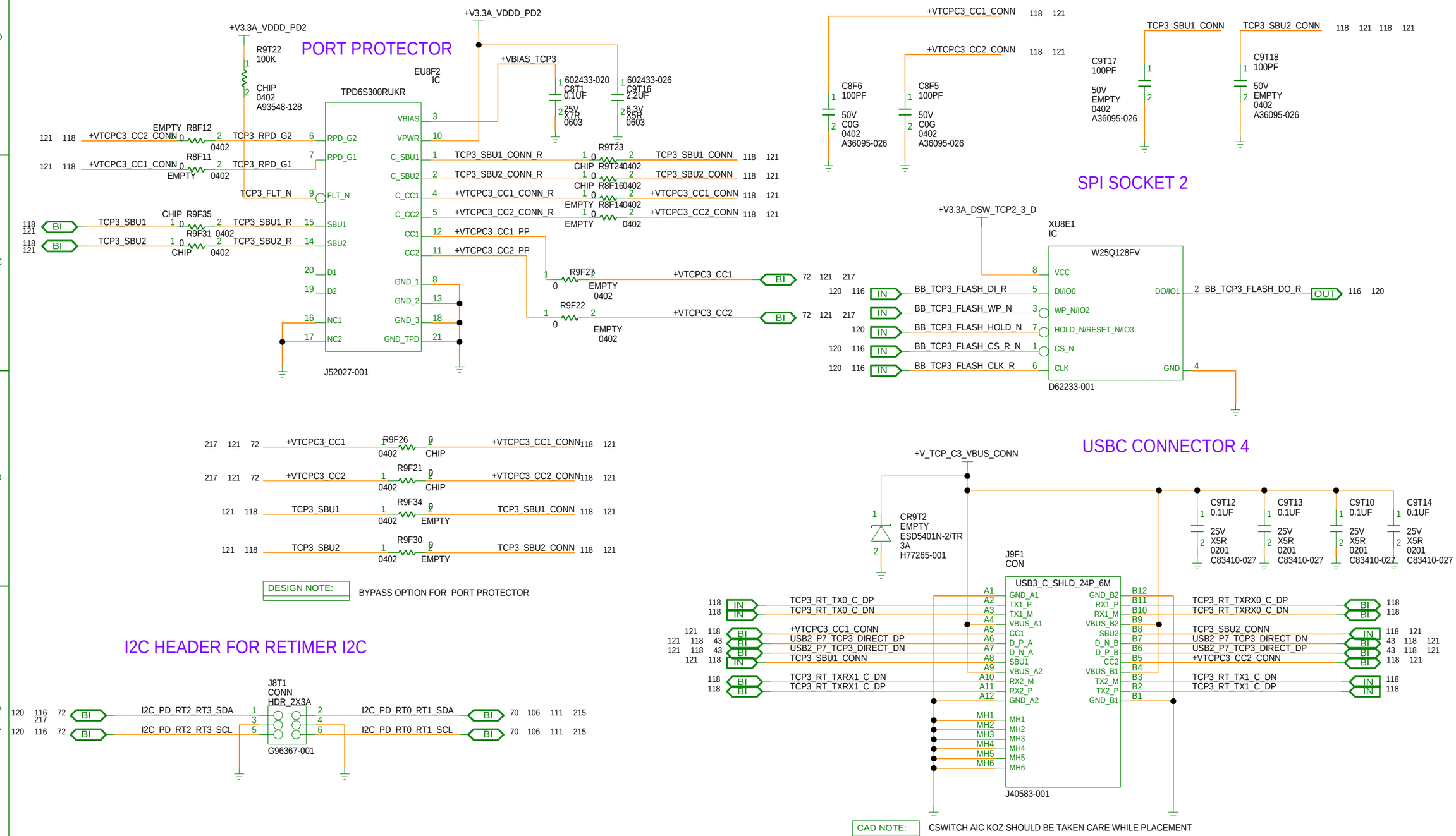

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BPAGE DRAWING
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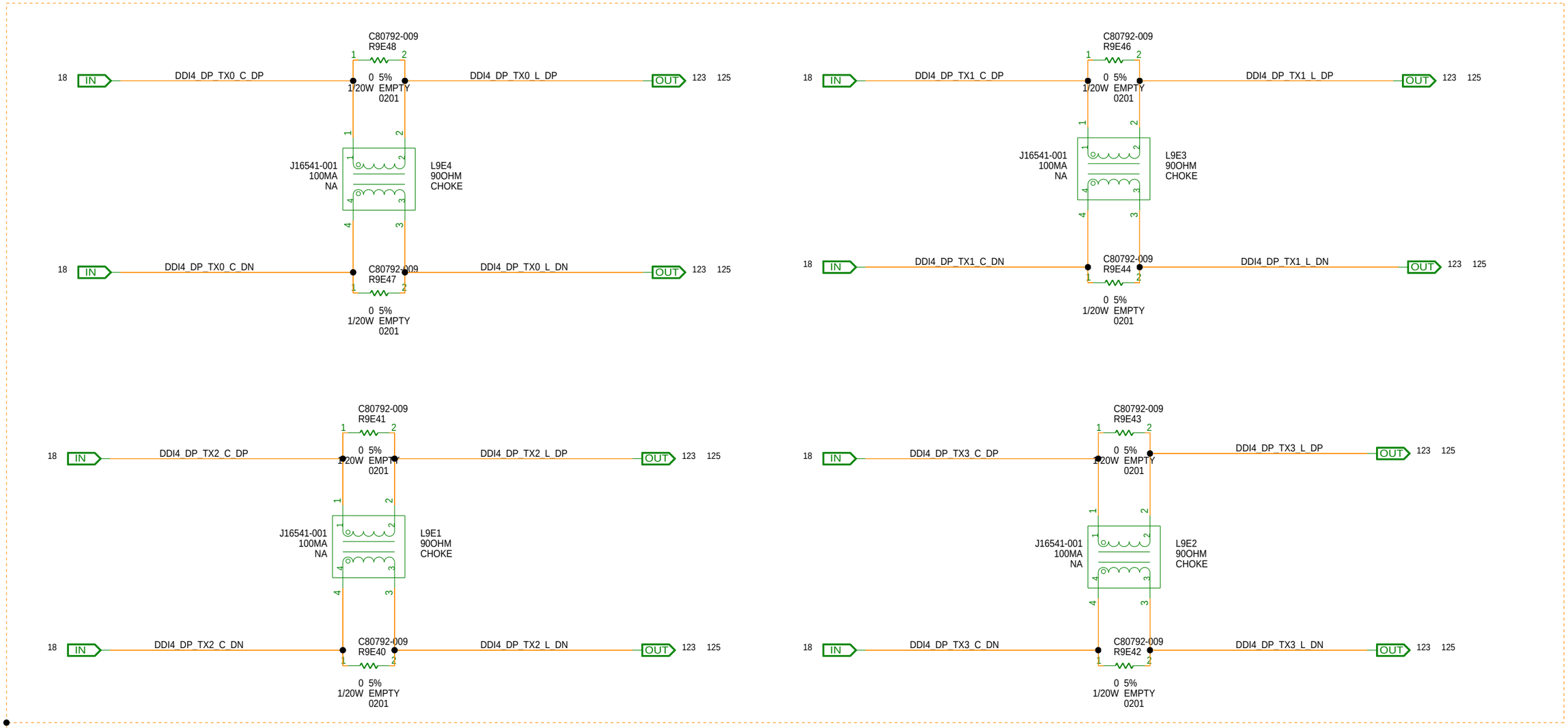
Wed Dec 18 18:07:18 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	121	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DP CONNECTOR 3 - CMC



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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.122
Tue Oct 15 12:50:18 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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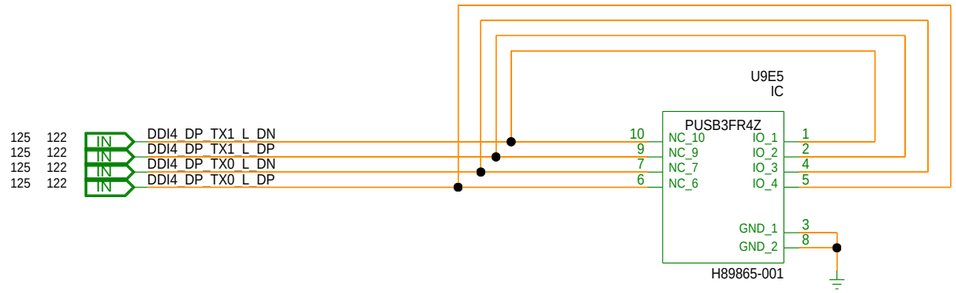
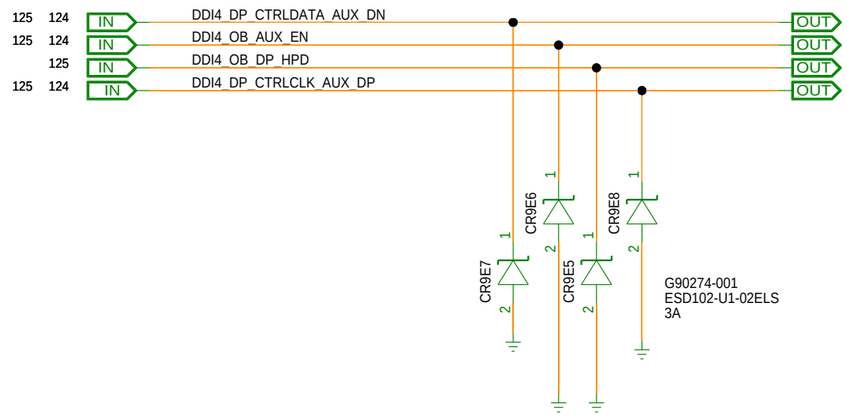
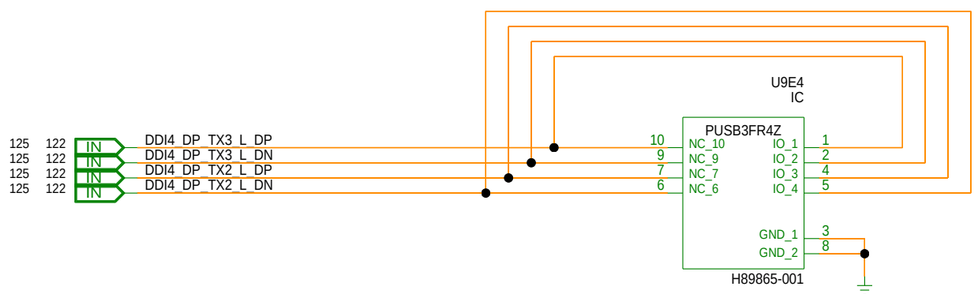
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DP CONNECTOR 3 - ESD







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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.123
Wed Dec 18 18:07:20 2019

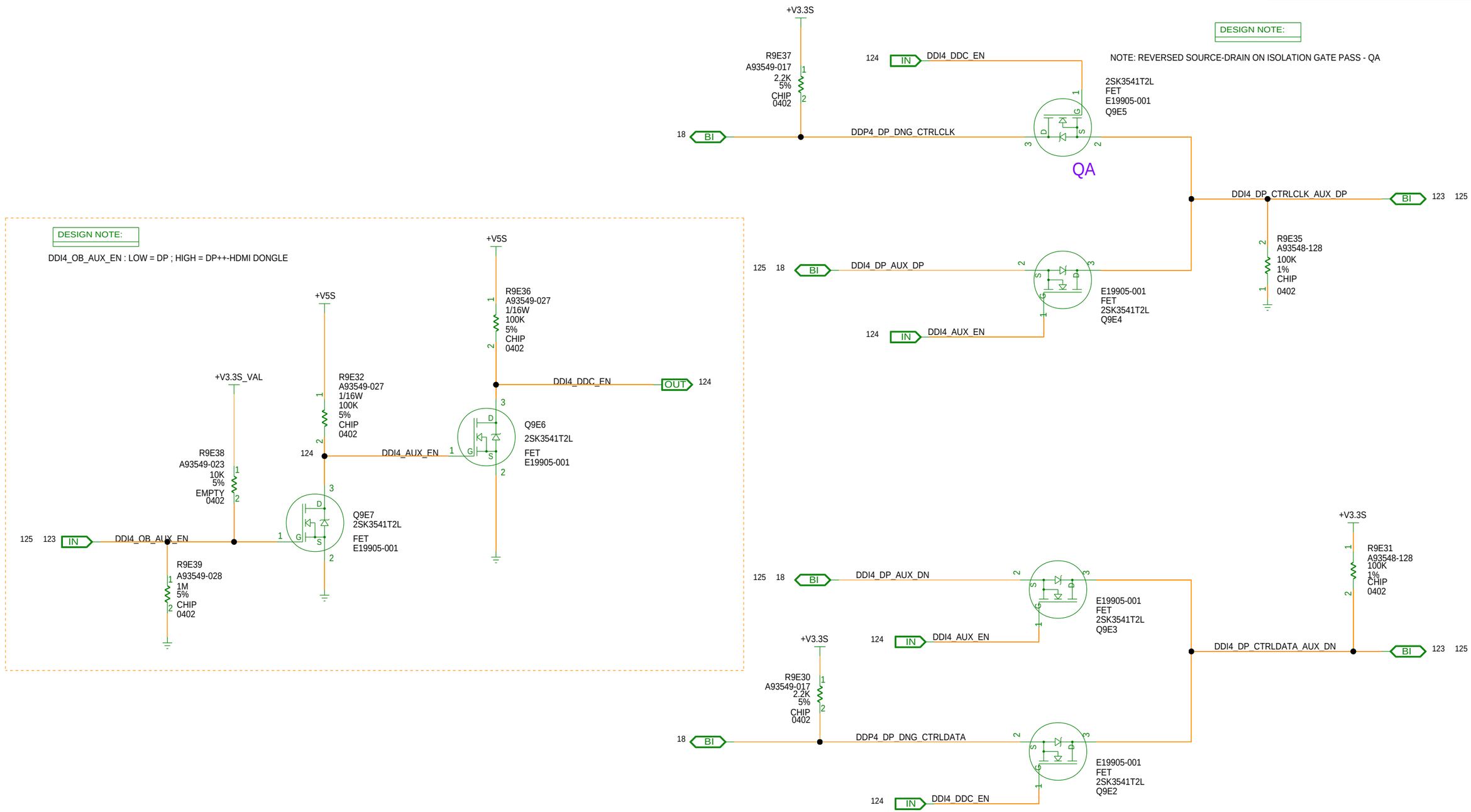
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	123	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:

NOTE: REVERSED SOURCE-DRAIN ON ISOLATION GATE PASS - QA



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BPAGE DRAWING
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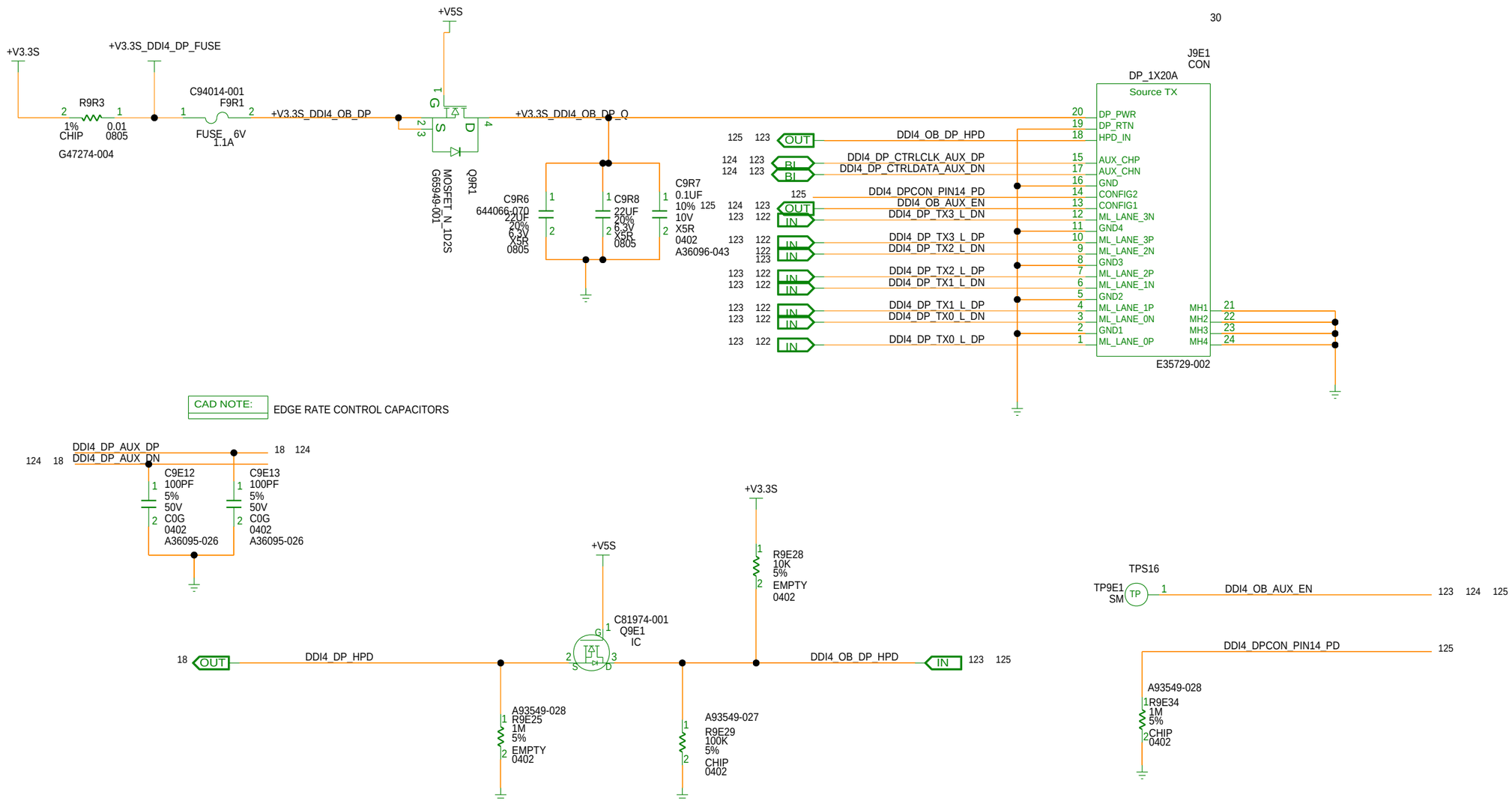
Wed Dec 18 18:07:21 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	124	1.0

CUSTOM TEXT BPAGE

DP CONNECTOR 3

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=DISPLAY - DP CONNECTOR 3]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.125
Wed Dec 18 18:07:22 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	125	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

NOTE: TOUCH PANEL CONNECTIONS ARE SUBJECTED TO CHANGE BASED ON PANEL SELECTION

DESIGN NOTE:
CPAS ARE FOR WBIO VALIDATION AND EMI PROTECTION

CAD NOTE:
PLACE THESE CAPS NEAR CONNECTOR

+V3.3DX_V1.8DX_TCH_PNL1_R

J4G1
CONN
HDR_1X10

126 IN THC0_SPI1_IO_0_I2C1_SCL_TCH_PNL1 — 1
126 BI THC0_SPI1_IO_1_I2C1_SDA_TCH_PNL1 — 2
126 30 OUT THC0_SPI1_INT_N_TCH_PNL1 — 3
126 30 IN THC0_SPI1_RST_N_TCH_PNL1 — 4
126 IN THC0_SPI1_CLK_I2C_SPI_MODE_SEL_TCH_PNL1 — 5
6
126 30 IN THC0_SPI1_CS0_N_TCH_PNL1 — 7
126 BI THC0_SPI1_IO_2_TCH_PNL1_R — 8
126 BI THC0_SPI1_IO_3_TCH_PNL1_R — 9
10

G70133-001

C4U12 0.1UF 10% 16V X7R 0402

C4U13 4.7UF 20% 6.3V X5R 0402

THC0_SPI1_CLK_I2C_SPI_MODE_SEL_TCH_PNL1 — C4G3 47PF 10% 25V EMPTY 0402

THC0_SPI1_IO_3_TCH_PNL1_R — C4U17 47PF 10% 25V EMPTY 0402

THC0_SPI1_IO_2_TCH_PNL1_R — C4G4 47PF 10% 25V EMPTY 0402

THC0_SPI1_IO_1_I2C1_SDA_TCH_PNL1 — C4G2 47PF 10% 25V EMPTY 0402

THC0_SPI1_IO_0_I2C1_SCL_TCH_PNL1 — C4G5 47PF 10% 25V EMPTY 0402 — 126

CAD NOTE: PLACE RA, RB CLOSE TO TOUCH PANEL CONNECTOR WITHIN 15MM, FOR ALL SIGNALS

CAD NOTE: PLACE TOUCH CONNECTOR WITHIN 150MM FROM PCH

CAD NOTE: TRIPAD RA AND RB

CAD NOTE: PLACE TESTPOINTS NEAR TO CONNECTOR

DESIGN NOTE:
ONLY SINGLE LOAD IS SUPPORTED. 1.8V IO:RA=33E, 3.3V IO IS NOT POR AND NOT SUPPORTED
MAX CABLE LENGTH SUPPORTED IS 203MM

+V3.3DX_V1.8DX_V1.8S_TCH_PNL1_PU

R4U19 47K 5% EMPTY 0402

126 30 IN THC0_SPI1_RST_N_TCH_PNL1

R4G53 10K 5% EMPTY 0402

+V3.3DX_V1.8DX_V1.8S_TCH_PNL1_PU

+V1.8S

+V3.3DX_V1.8DX_TCH_PNL1_R

2-3
J9G5
HDR_1X3

1 IO1
2 IO2
3 IO3

DEFAULT 2-3

G25849-001

DESIGN NOTE:
VDD= 3.3V AND IOVDD=1.8V/3.3V FOR ELANTEC TOUCH CONTROLLER

30 IN THC0_SPI1_CLK_TCH_PNL1 — R4U26 33 0402 5% EMPTY — RA — THC0_SPI1_CLK_I2C_SPI_MODE_SEL_TCH_PNL1 OUT 126

126 IN I2C_SPI_MODE_SEL_TCH_PNL1 — R4G48 0 0402 5% CHIP — RB

30 IN THC0_SPI1_IO_0_TCH_PNL1 — R4G49 33 0402 5% EMPTY — RA — THC0_SPI1_IO_0_I2C1_SCL_TCH_PNL1 OUT 126

126 28 IN I2C1_SCL_TCH_PNL1 — R4G52 0 0402 5% CHIP — RB

30 BI THC0_SPI1_IO_1_TCH_PNL1 — R4U20 33 0402 5% EMPTY — RA — THC0_SPI1_IO_1_I2C1_SDA_TCH_PNL1 BI 126

126 28 IN I2C1_SDA_TCH_PNL1 — R4G50 0 0402 5% CHIP — RB

30 BI THC0_SPI1_IO_2_TCH_PNL1 — R4G51 33 0402 5% EMPTY — THC0_SPI1_IO_2_TCH_PNL1_R BI 126

30 BI THC0_SPI1_IO_3_TCH_PNL1 — R4U36 33 0402 5% EMPTY — THC0_SPI1_IO_3_TCH_PNL1_R BI 126

+V3.3DX_V1.8DX_V1.8S_TCH_PNL1_PU

R4U31 47K 5% CHIP 0402

THC0_SPI1_INT_N_TCH_PNL1 OUT 30 126

+V3.3DX_V1.8DX_V1.8S_TCH_PNL1_PU

R4U32 47K 5% CHIP 0402

126 30 IN THC0_SPI1_CS0_N_TCH_PNL1

+V3.3DX_V1.8DX_V1.8S_TCH_PNL1_PU

LPDB GENERIC — R5G33 1K 5% EMPTY 0402

LPDB GENERIC — R4U17 1K 5% EMPTY 0402

I2C1_SDA_TCH_PNL1 BI 28 126

I2C1_SCL_TCH_PNL1 IN 28 126

+V3.3DX_V1.8DX_V1.8S_TCH_PNL1_PU

R4G43 10K 5% EMPTY 0402

126 OUT I2C_SPI_MODE_SEL_TCH_PNL1

RB — 0402 CHIP 1/16W 5% 0 R4G42

DESIGN NOTE:
STUFF RB FOR I2C MODE, UNSTUFF RB FOR THC MODE

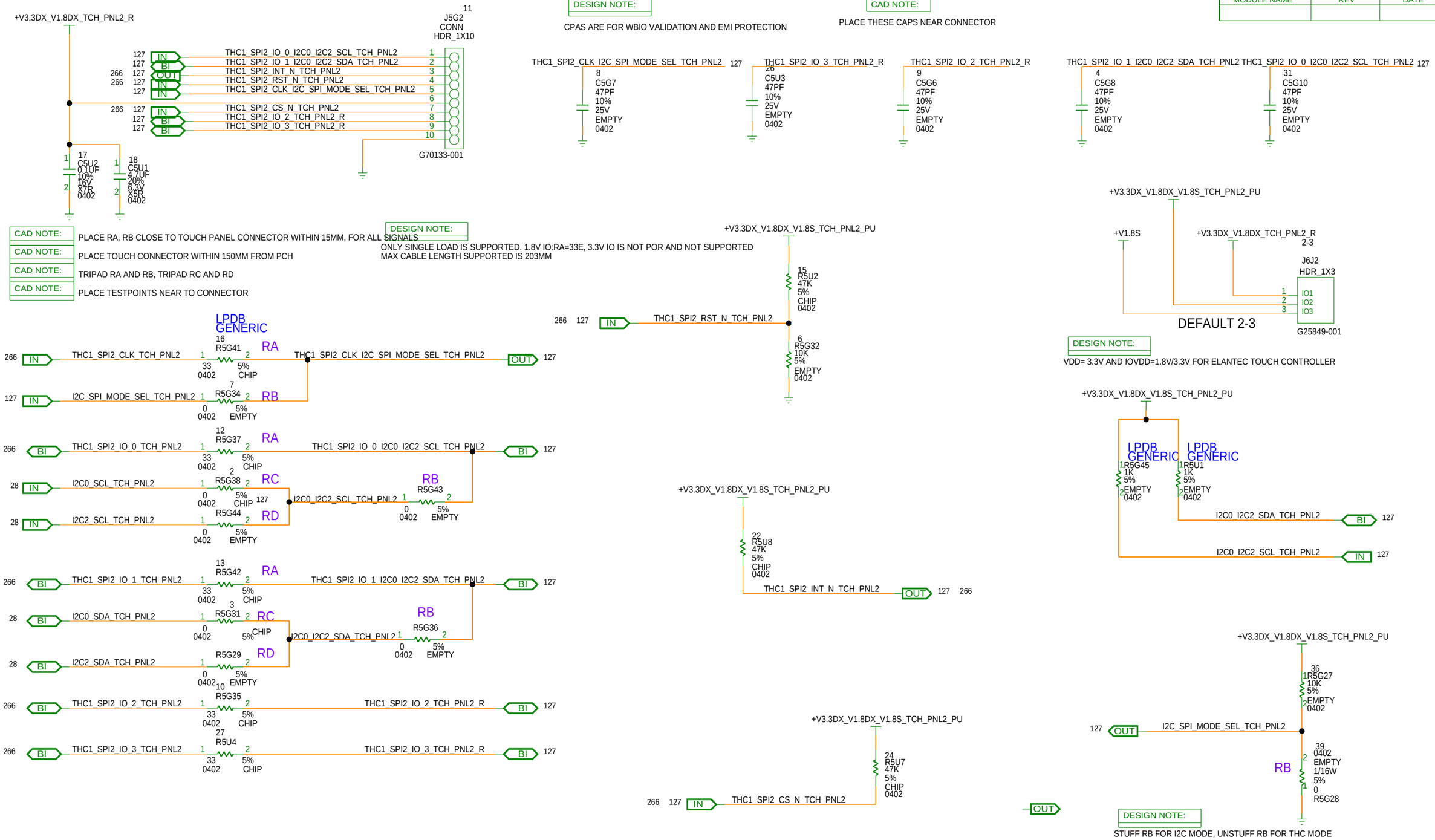
[PAGE_TITLE=TOUCH PANEL CONNECTOR 1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.126
Wed Dec 18 18:07:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	126	1.0

CUSTOM TEXT BPAGE

NOTE: TOUCH PANEL CONNECTIONS ARE SUBJECTED TO CHANGE BASED ON PANEL SELECTION



MODULE REV DETAILS

MODULE NAME	REV	DATE

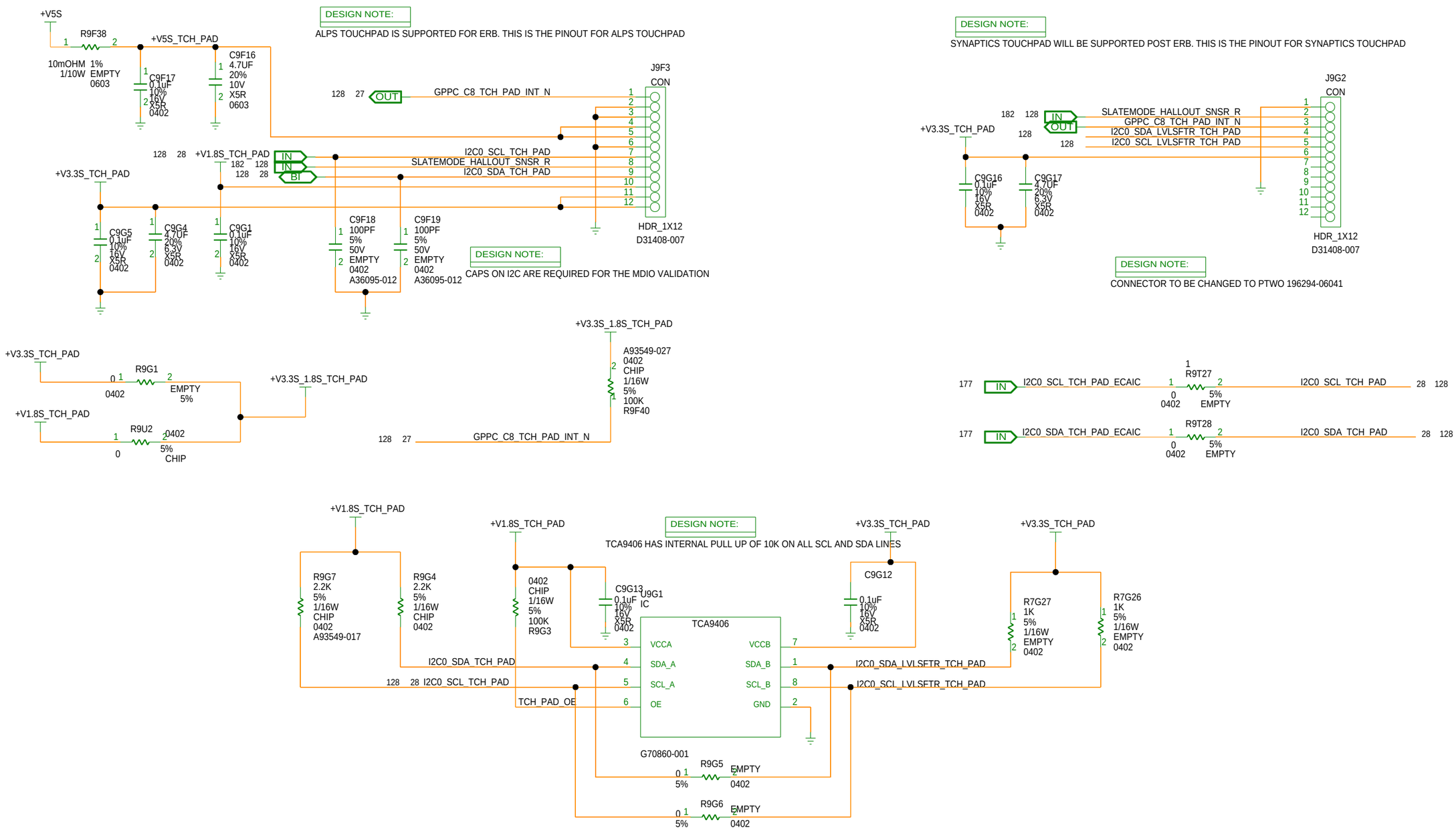
[PAGE_TITLE=TOUCH PANEL CONNECTOR 2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.127
Wed Dec 18 18:07:24 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	127	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=TOUCH PAD CONNECTOR]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.128
Wed Dec 18 18:07:25 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	128	1.0

CUSTOM TEXT BPAGE

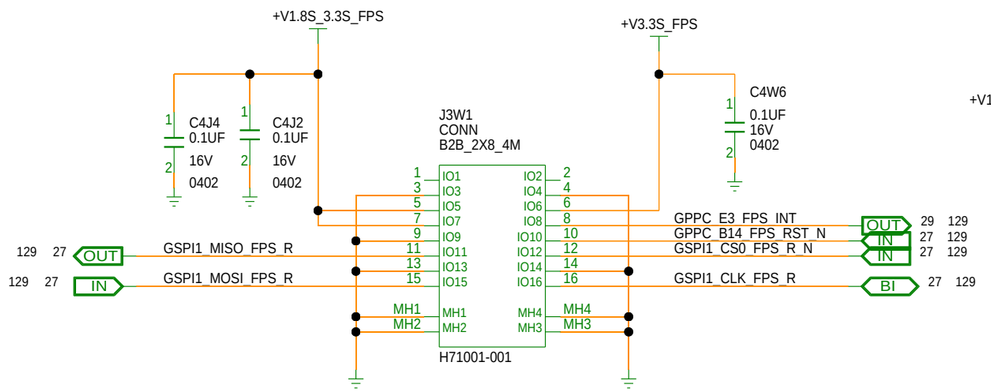
MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:

FPS FROM FPC COMPANY WILL BE SUPPORTED ON ERB

CAD NOTE:

TO BE PLACED ON BOTTOM SIDE OF THE BOARD EXACTLY BELOW J13101



NOTE: ALL THE GPIOS AND SPI LINES ARE PULLED UP TO +V1.8S_3.3S_FPS; AIC SHOULD USE THE SAME SUPPLY FOR SENSOR I/O

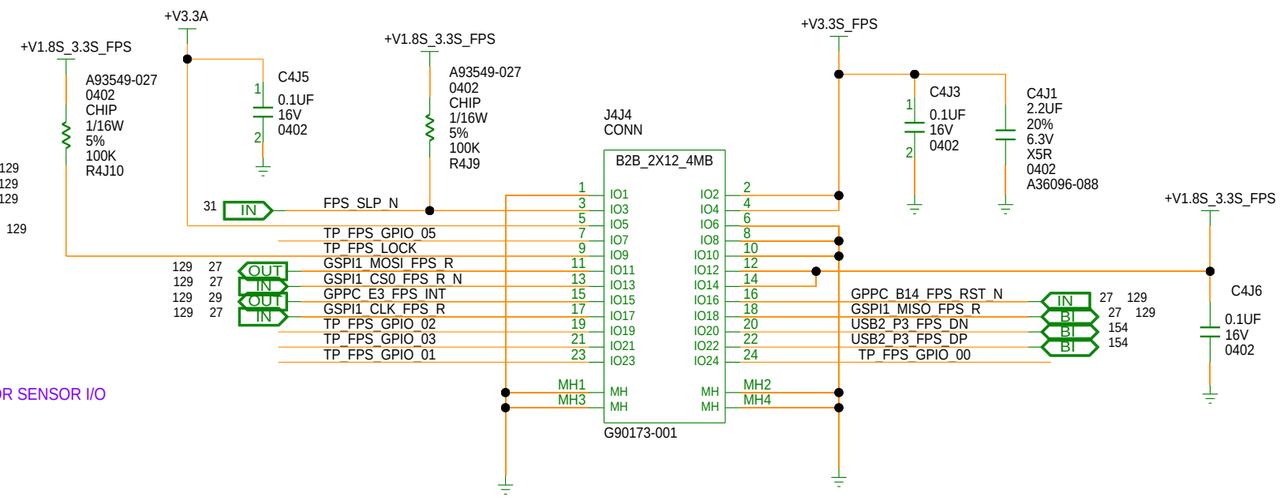
CAD NOTE:

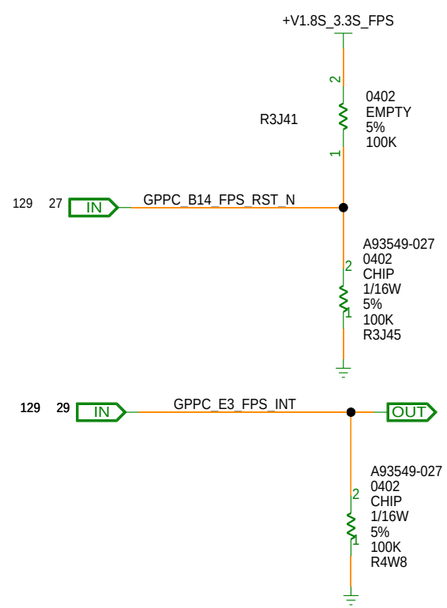
THIS NEEDS TO BE AN EDGE CONNECTOR ON THE TOP OF RVP

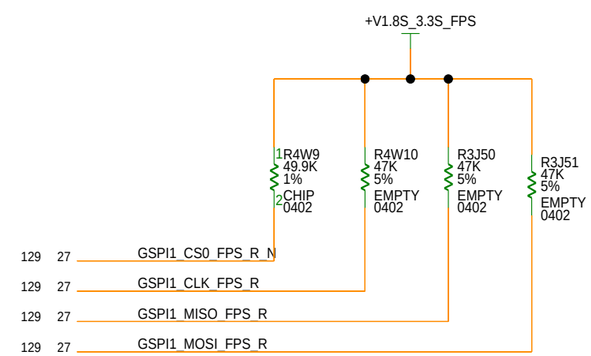
DESIGN NOTE:

FPS FROM SYNAPTICS COMPANY WILL BE SUPPORTED ON ERB AND CRB

NOTE: CONNECTIONS NEED TO BE FINALIZED. WAITING FOR THE PINOUT FROM SYNAPTICS







[PAGE_TITLE=FPS CONNECTOR]

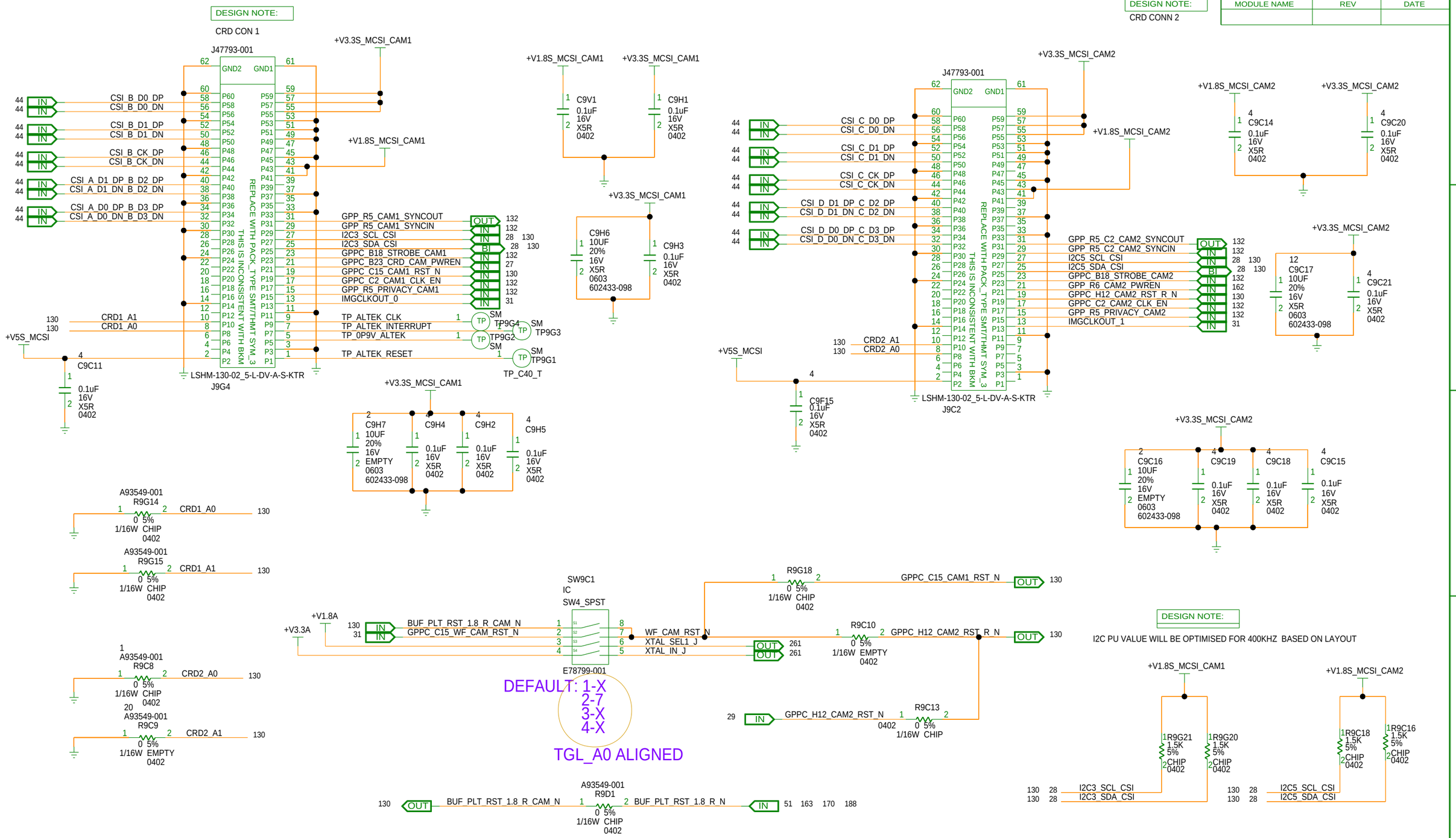
BPAGE DRAWING

tigerlake_u_ddr4.sch_1.129
Wed Dec 18 18:07:26 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	129	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



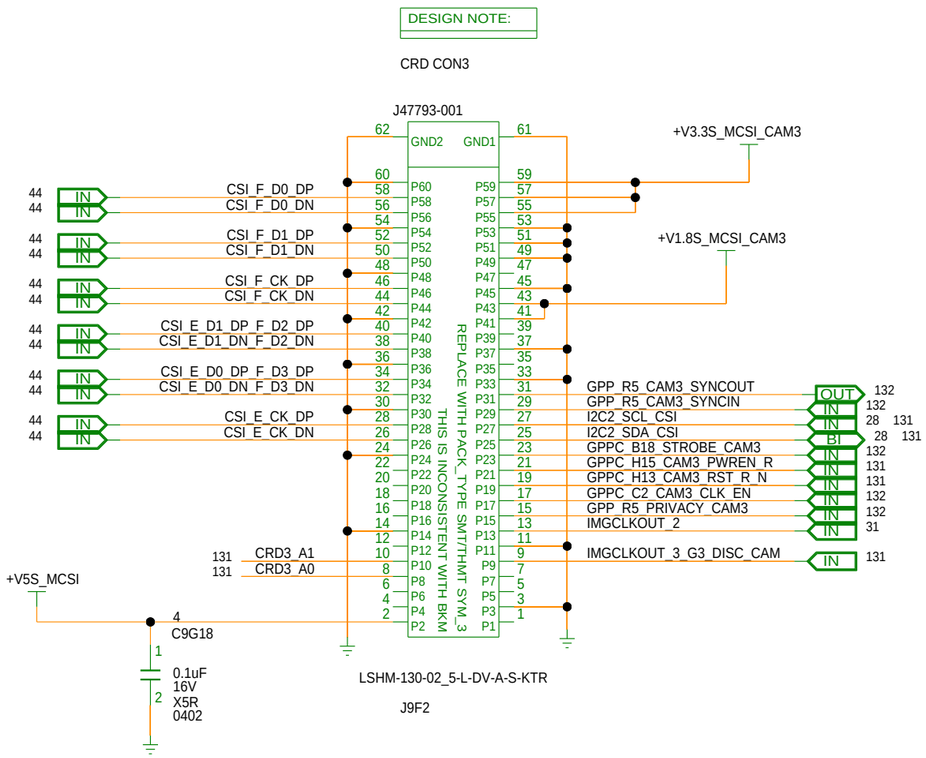
[PAGE_TITLE=IMAGING - CRD CONNECTOR 1&2]

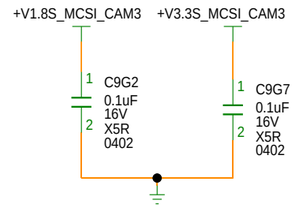
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.130
Wed Dec 18 18:07:27 2019

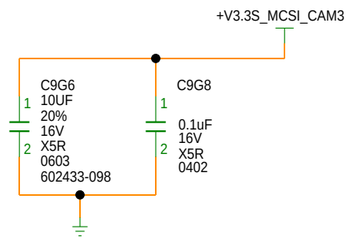
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	130	1.0

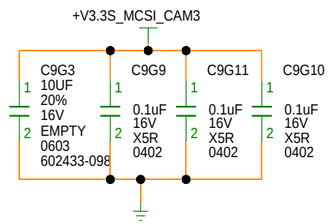
CUSTOM TEXT BPAGE

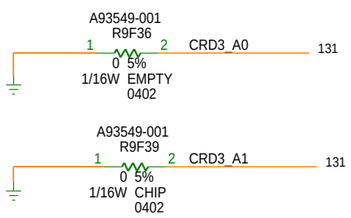
MODULE REV DETAILS		
MODULE NAME	REV	DATE

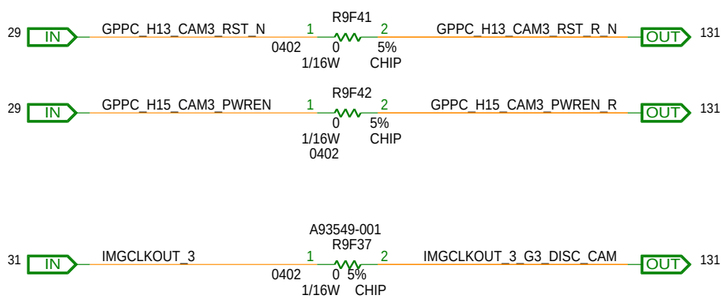






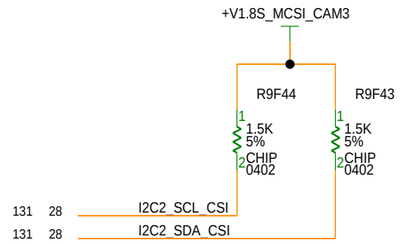






DESIGN NOTE:

I2C PU VALUE WILL BE OPTIMISED FOR 400KHZ BASED ON LAYOUT



[PAGE_TITLE=IMAGING - CRD CONNECTOR 3]

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Wed Dec 18 18:07:28 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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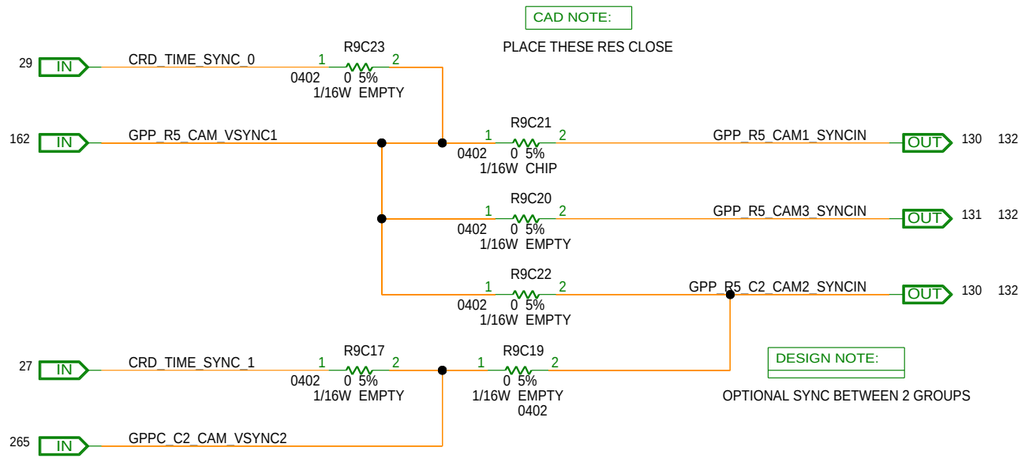
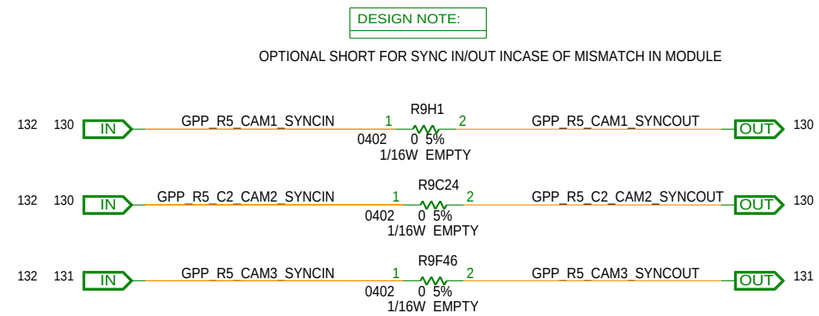
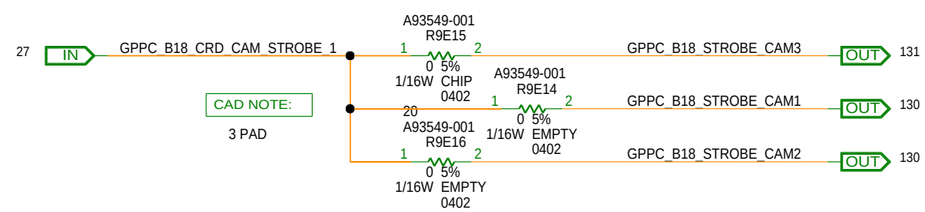
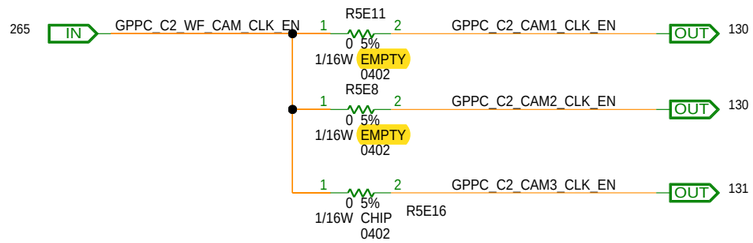
CUSTOM TEXT BPAGE

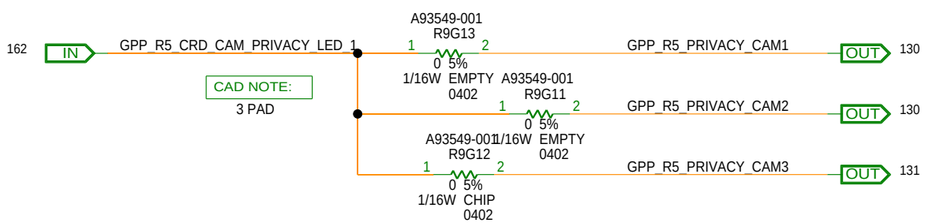
MODULE REV DETAILS		
MODULE NAME	REV	DATE











[PAGE_TITLE=IMAGING CRD GPIO SHARING]

BPAGE DRAWING
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Wed Dec 18 18:07:29 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE= RESERVE]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.133
Tue Oct 15 12:50:30 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS

MODULE NAME	REV	DATE

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BPAGE DRAWING

tigerlake_u_ddr4.sch_1.134
Tue Oct 15 12:50:31 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS

MODULE NAME	REV	DATE

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BPAGE DRAWING

tigerlake_u_ddr4.sch_1.135
Tue Oct 15 12:50:32 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS

MODULE NAME	REV	DATE

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Tue Oct 15 12:50:33 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=RESERVE]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.137
Tue Oct 15 12:50:34 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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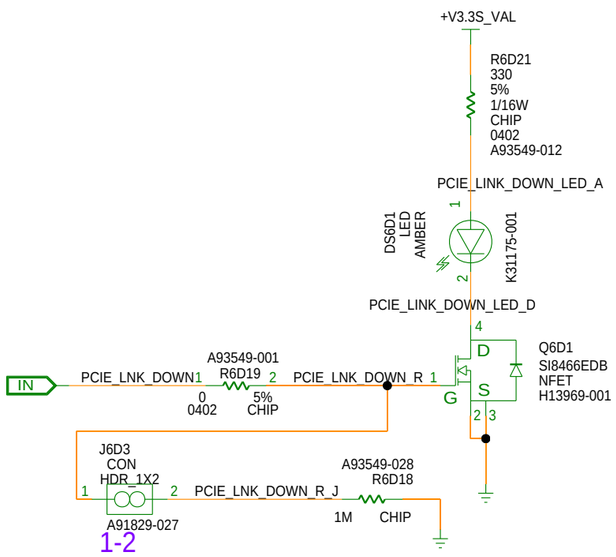
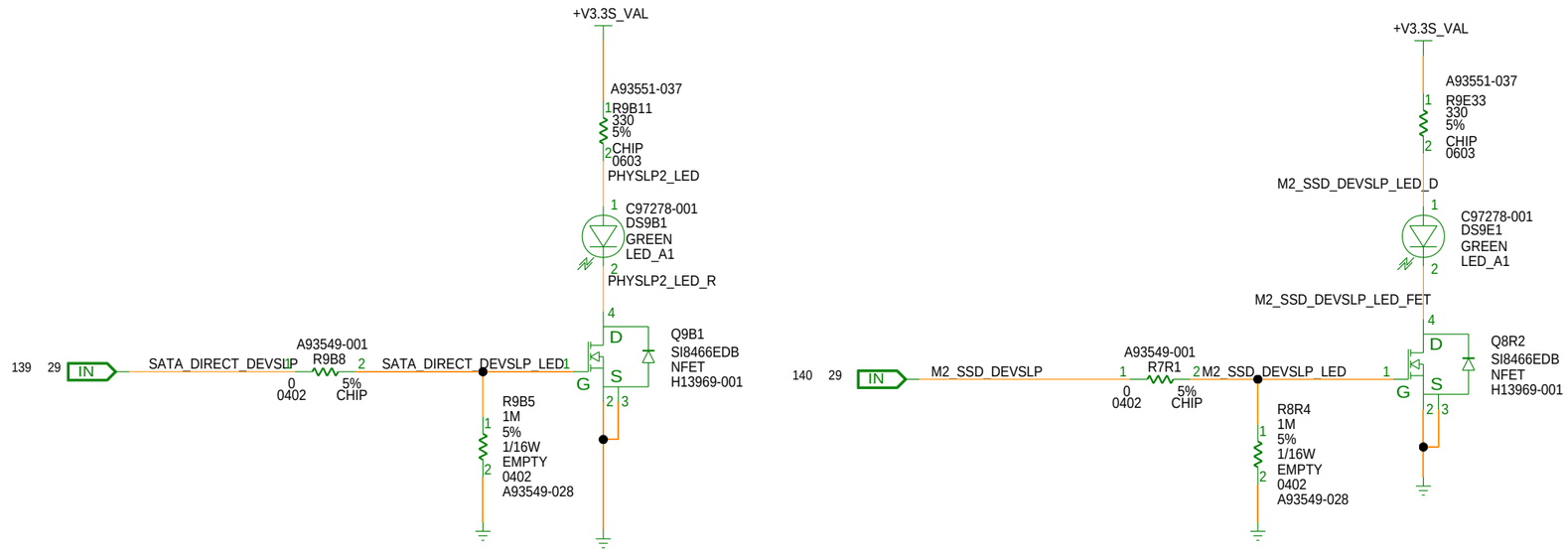
MODULE REV DETAILS		
MODULE NAME	REV	DATE

PCIE_LINK_DOWN_LED

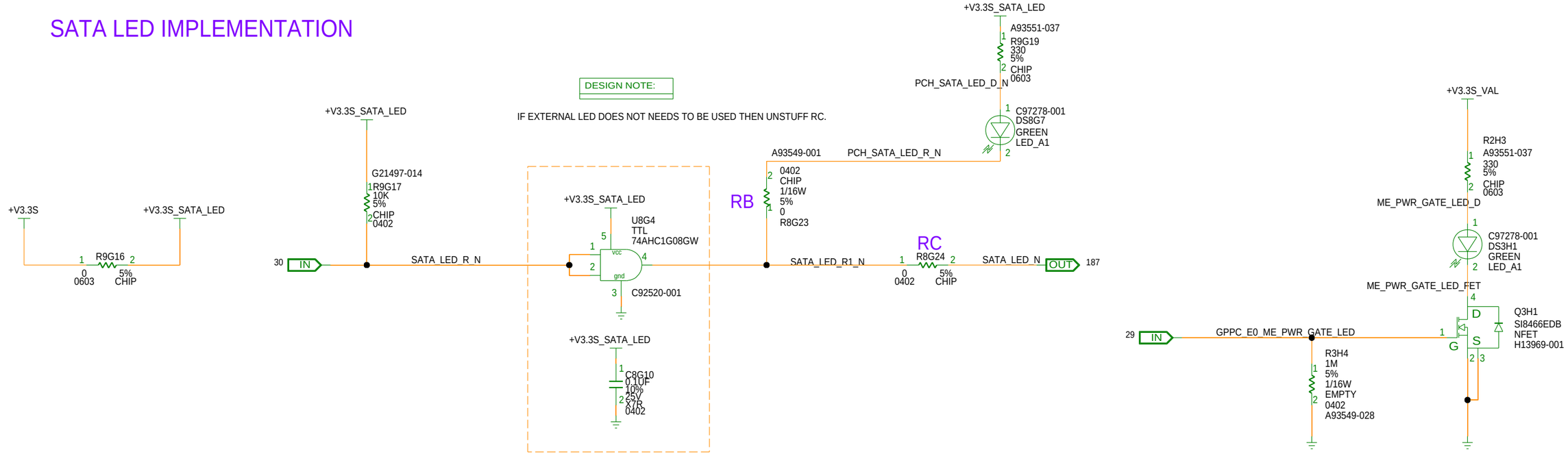


1-2

SATA DEV SLEEP LED



SATA LED IMPLEMENTATION



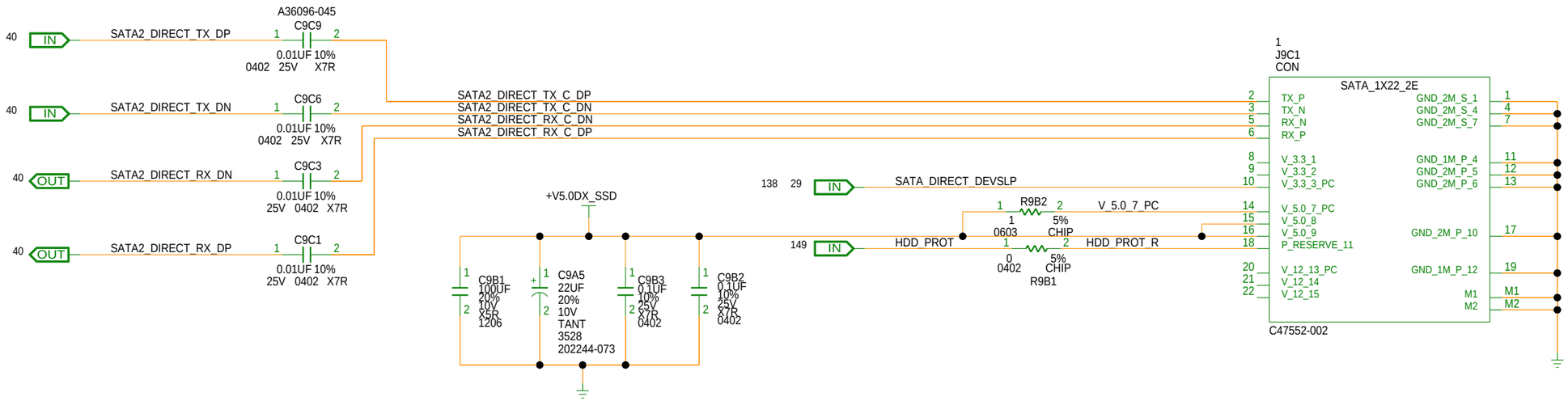
[PAGE_TITLE=SATA DEVSLEEP LED]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.138
Wed Dec 18 18:07:33 2019

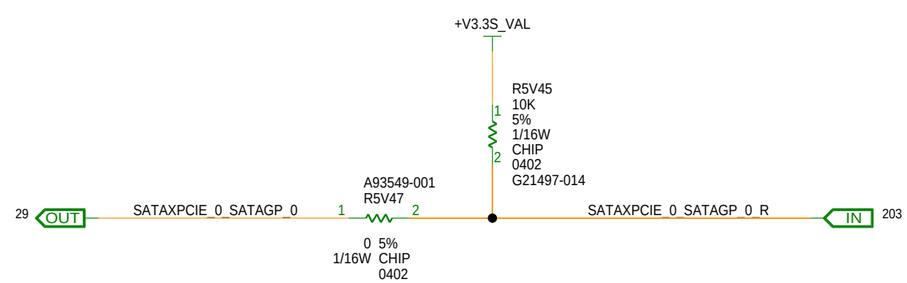
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	138	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

RIGHT-ANGLE SATA DIRECT CONNECT



SATA HOT-PLUG VALIDATION



[PAGE_TITLE=STORAGE - SATA DIRECT CONNECT]

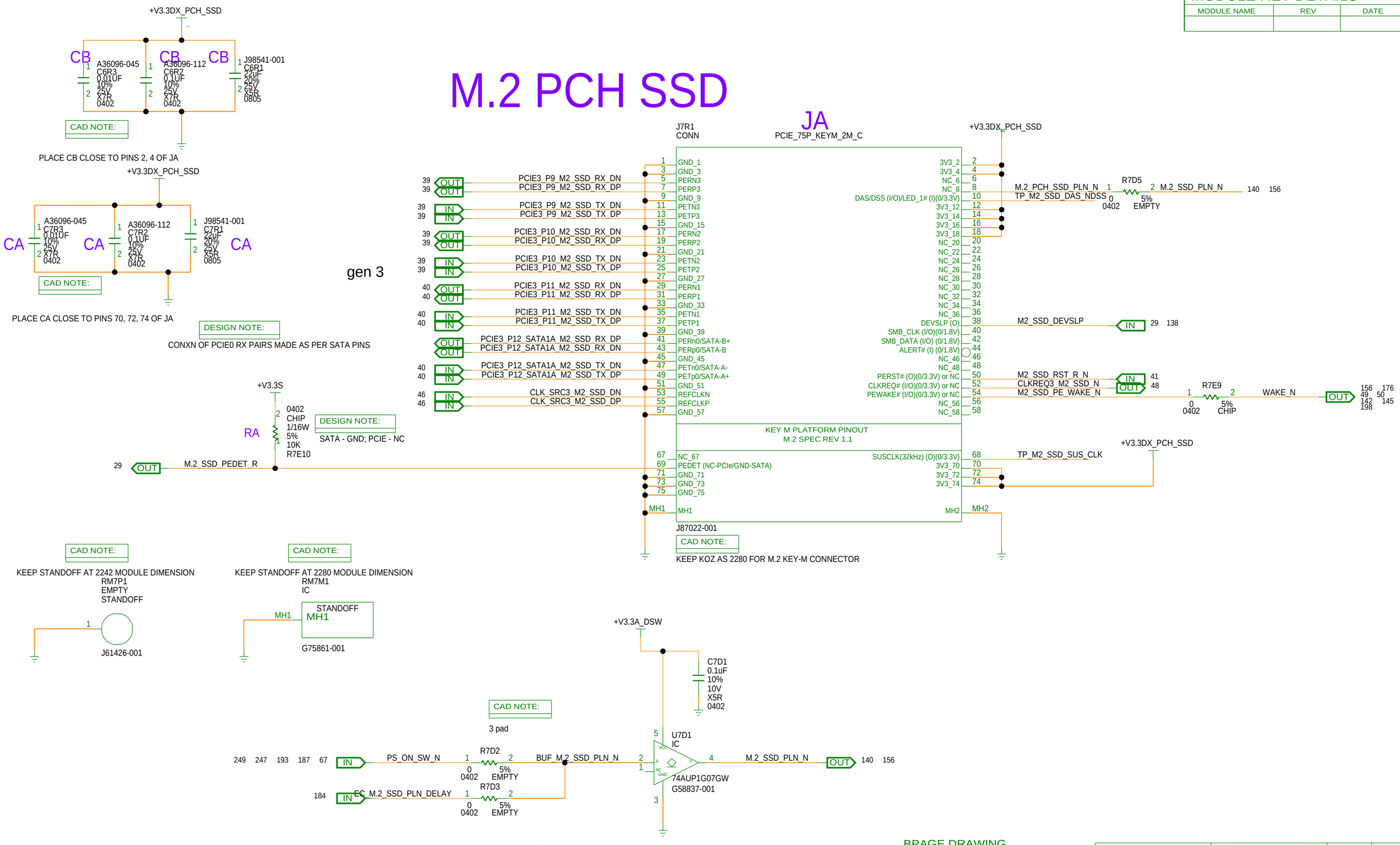
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.139
Wed Dec 18 18:07:34 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	139	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

M.2 PCH SSD



[PAGE_TITLE=STORAGE - M.2 KEY-M SSD]

BPAGE DRAWING
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Wed Dec 18 18:07:35 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	140	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

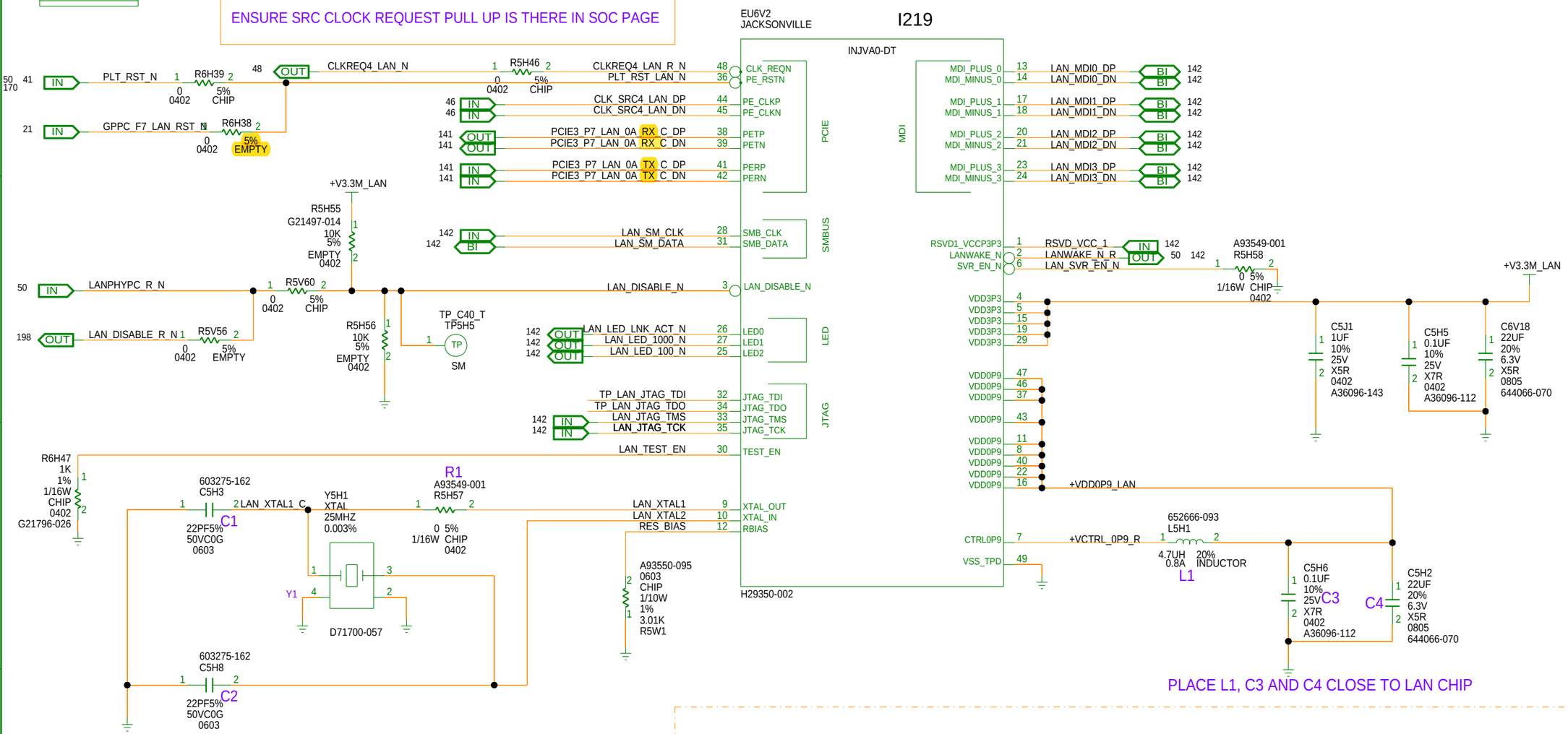
LAN PHY CHIP - JACKSONVILLE

ADD RTD3 AND LOGIC

DESIGN NOTE:

DESIGN NOTE:

ENSURE SRC CLOCK REQUEST PULL UP IS THERE IN SOC PAGE



DESIGN NOTE:

SMBUS DEVICE ADDRESS - JACKSONVILLE LAN CHIP

0XC8

[PAGE_TITLE=CONNECTIVITY - GBIT LAN - JACKSONVILLE LAN PHY CHIP]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.141
Wed Dec 18 18:07:36 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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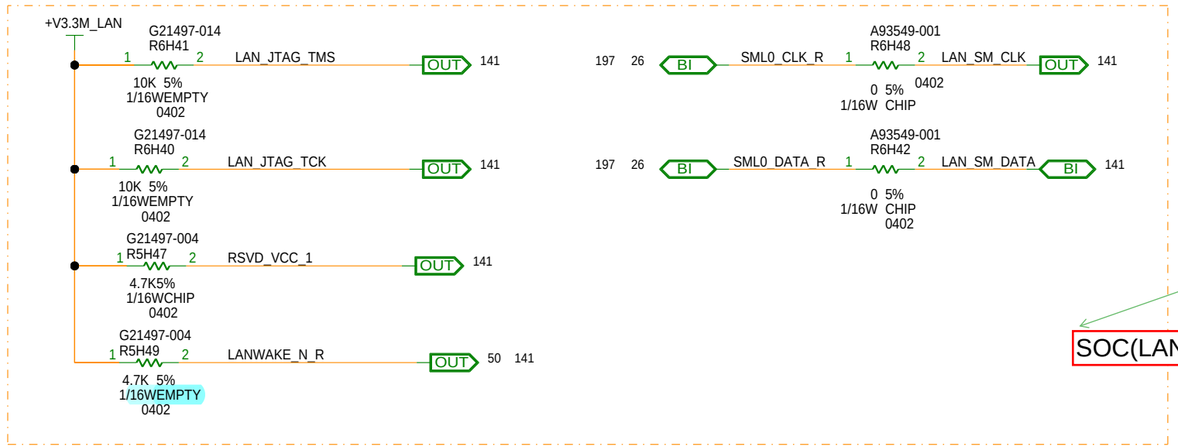
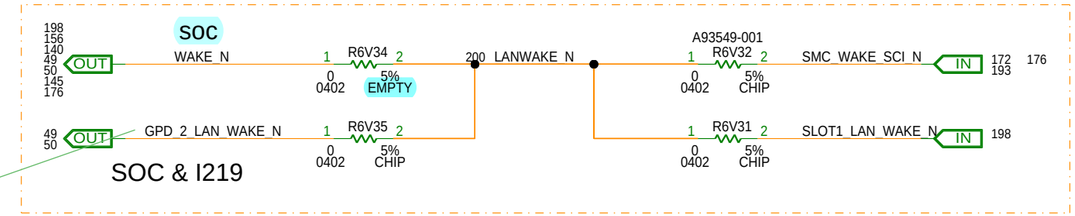
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



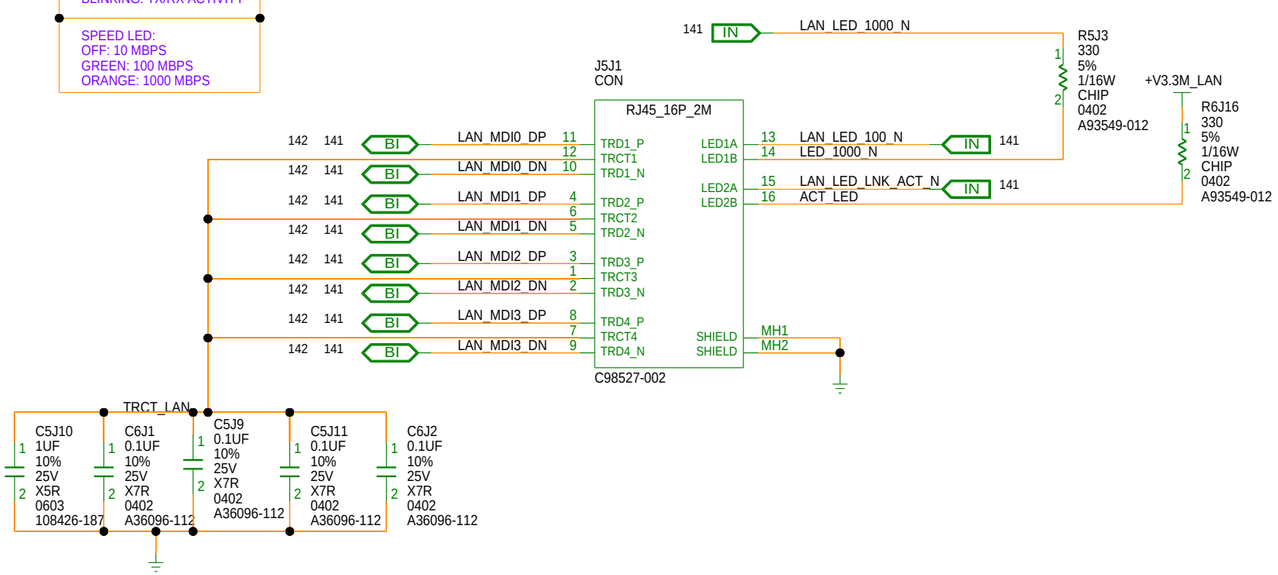


SOC(LAN_WAKE#) -> GPD_2_LAN_WAKE_N -> LANWAKE_N_R -> i219(LANWAKE_N)

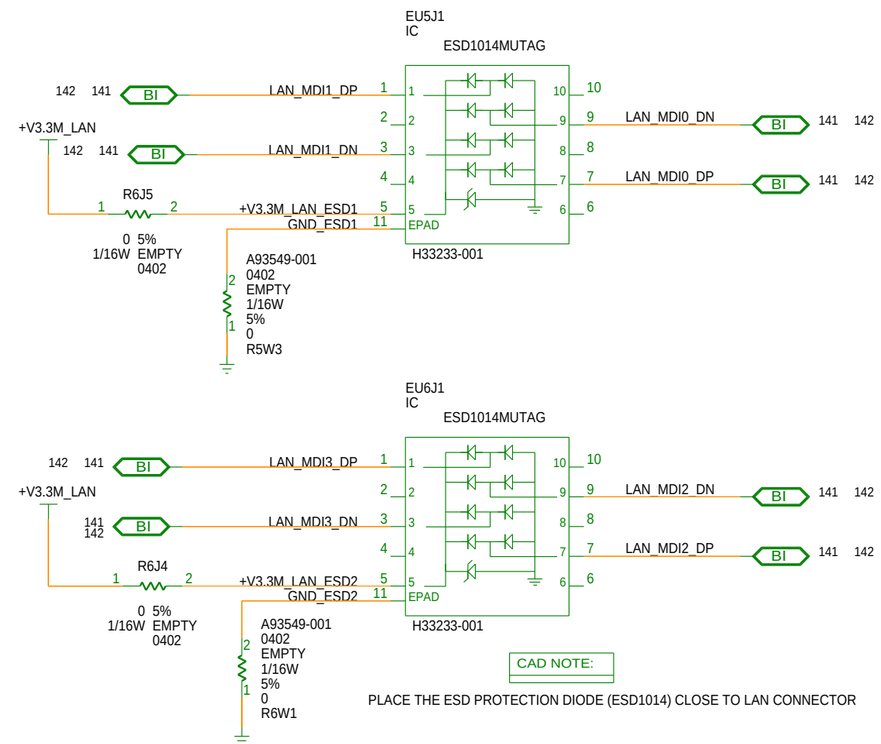
RJ-45 CONNECTOR WITH BUILT-IN MAGNETICS

ACTIVITY LED:
GREEN: LINK UP
BLINKING: TX/RX ACTIVITY

SPEED LED:
OFF: 10 MBPS
GREEN: 100 MBPS
ORANGE: 1000 MBPS



ESD PROTECTION DIODES



CAD NOTE:

PLACE THE ESD PROTECTION DIODE (ESD1014) CLOSE TO LAN CONNECTOR

[PAGE_TITLE=CONNECTIVITY - GBIT LAN CONNECTOR]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.142
Wed Dec 18 18:07:37 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	142	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

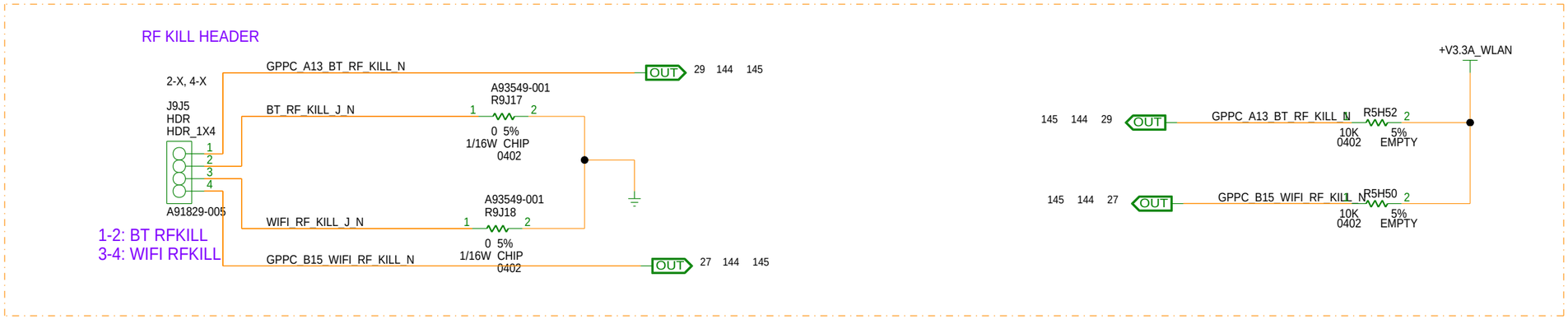
[PAGE_TITLE=CONNECTIVITY - M.2 KEY-E WLAN/BT]

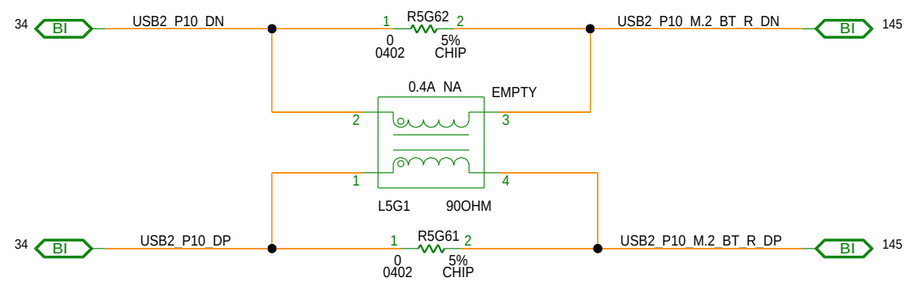
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.143
Tue Oct 15 12:50:40 2019

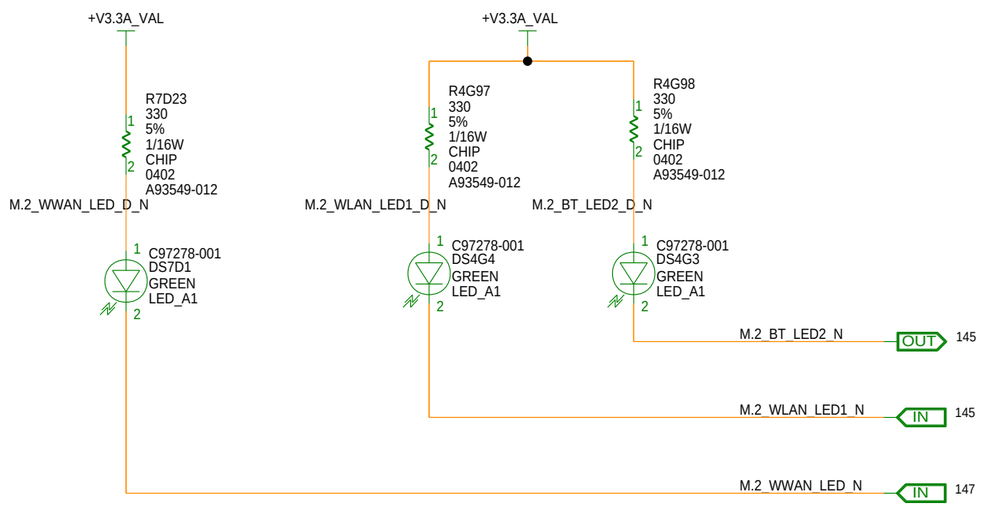
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	143	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE







[PAGE_TITLE=CONNECTIVITY - M.2 KEY-E WLAN/BT - LED'S, MISC]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.144
Wed Dec 18 18:07:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	144	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

M.2 SOCKET 1 - WLAN/BT

wifi

CAD NOTE:
PLACE CA CLOSE TO PIN 2 AND 4

+V3.3A_WLAN

C5G16	C5G15	C5G17	C5G14
0.01UF	0.01UF	0.1UF	10UF
10%	10%	10%	10%
25V	25V	25V	16V
EMPTY	X7R	X7R	X7R
0402	0402	0402	1206
A36096-045	A36096-045	A36096-112	644066-086

J4H1
CONN

PCIE_75P_KEY_E_2M

Pin	Signal	Net	Dir	Page
144	BI	USB2_P10_M.2_BT_R_DP		
144	BI	USB2_P10_M.2_BT_R_DN		
143	OUT	CNV_WR_D1_R_DN		
143	OUT	CNV_WR_D1_R_DP		
143	OUT	CNV_WR_D0_R_DN		
143	OUT	CNV_WR_D0_R_DP		
143	OUT	CNV_WR_CLK_R_DN		
143	OUT	CNV_WR_CLK_R_DP		
36	IN	PCIE3_P3_M2_WLAN_TX_DP		
36	IN	PCIE3_P3_M2_WLAN_TX_DN		
36	OUT	PCIE3_P3_M2_WLAN_RX_DP		
36	OUT	PCIE3_P3_M2_WLAN_RX_DN		
45	IN	CLK_SRC1_M2_WLAN_DP		
45	IN	CLK_SRC1_M2_WLAN_DN		
48	OUT	CLKREQ1_WLAN_N		
145	OUT	M.2_WLAN_PE_WAKE_N		
143	IN	CNV_WT_D1_R_DN		
143	IN	CNV_WT_D1_R_DP		
143	IN	CNV_WT_D0_R_DN		
143	IN	CNV_WT_D0_R_DP		
143	IN	CNV_WT_CLK_R_DN		
143	IN	CNV_WT_CLK_R_DP		
1	GND[1]			
3	USB_DP			
5	USB_DN			
7	GND[2]			
9	WGR_D1N			
11	WGR_D1P			
13	GND[3]			
15	WGR_D0N			
17	WGR_D0P			
19	GND[5]			
21	WGR_CLKN			
23	WGR_CLKP			
33	GND[6]			
35	PETP0			
37	PETN0			
39	GND[7]			
41	PERP0			
43	PERN0			
45	GND[8]			
47	REFCLKP0			
49	REFCLKN0			
51	GND[9]			
53	CLKREQ0_N			
55	PEWAKE0_N			
57	GND[10]			
59	WT_D1N			
61	WT_D1P			
63	GND[11]			
65	WT_D0N			
67	WT_D0P			
69	GND[12]			
71	WT_CLKN			
73	WT_CLKP			
75	GND[13]			
MH2	MH2			
2	3V3[1]			
4	3V3[2]			
6	LED1_N	M.2_WLAN_LED1_N	OUT	144
8	PCM_CLK	M.2_BT_PCMCLK	IN	160
10	PCM_SYNC/LCP_RSTN	M.2_BT_PCMFRM_CRF_RST_N	IN	145 160
12	PCM_IN	M.2_BT_PCMIN	OUT	160
14	PCM_OUT/CLKREQ0	M.2_BT_PCMOUT_CLKREQ	IN	145 160
16	LED2_N	M.2_BT_LED2_N	OUT	144
18	GND[4]			
20	UART_WAKE_N	GPPC_H19_UART_BT_WAKE_N		
22	UART_RX/BRI_RSP	M.2_CNV_BRI_RSP_BT_UART0_RX	OUT	27
32	UART_TX/RGI_DT	M.2_CNV_RGI_DT_BT_UART0_TX	IN	27
34	UART_CTS/RGI_RSP	M.2_CNV_RGI_RSP_BT_UART0_CTS	OUT	27
36	UART_RTS/BRI_DT	M.2_CNV_BRI_DT_BT_UART0_RTS	IN	27
38	CLINK_RESET	M.2_WLAN_CL_RST_N	IN	265
40	CLINK_DATA	M.2_WLAN_CL_DATA	BI	265
42	CLINK_CLK	M.2_WLAN_CL_CLK	IN	265
44	COEX3	DISC_WLAN_WWAN_COEX3	IN	146
46	COEX2	DISC_WLAN_WWAN_COEX2	OUT	146
48	COEX1	DISC_WLAN_WWAN_COEX1	OUT	146
50	SUSCLK	M.2_BT.WIFI_SUS_CLK	IN	45
52	PERST0_N	M.2_WLAN_PERST_R_N	IN	41
54	W_DISABLE2_N	GPPC_A13_BT_RF_KILL_N	IN	29 144
56	W_DISABLE1_N	GPPC_B15_WIFI_RF_KILL_N	IN	27 144
58	A4WP_I2C_DATA	TP_A4WP_I2C_DATA		
60	A4WP_I2C_CLK	TP_A4WP_I2C_CLK		
62	A4WP_IRQ_N	TP_A4WP_IRQ_N		
64	REFCLK0	TP_VAL_PULSAR_38P4M_REFCLK		
66	PERST1_N	TP_M.2_PERST1_N		
68	CLKREQ1_N	TP_M.2_CLKREQ1_N		
70	PEWAKE1_N	TP_M.2_PEWAKE1_N		
72	3V3[3]			
74	3V3[4]			
MH1	MH1			

KEY E

G64002-001

+V3.3A_WLAN

R5H54
10K
5%
1/16W
CHIP
0402
G21497-014

OUT 29

TPS16 TP5H1 SM
TPS16 TP4H1 SM
TPS16 TP5H2 SM
TP5H3 SM TPS16

THIS CLOCK IS ONLY FOR ICL N-1 INTERPOSER

+V3.3A_WLAN

A93549-027
0402
CHIP
1/16W
5%
100K
R5H53

190 OUT GPPC_C23_WIFI_WAKE_N

R5H51
0
0402
5%
CHIP

M.2_WLAN_PE_WAKE_N 145

198 176 156 142 140 50 49 OUT WAKE_N

R5H45
0
0402
5%
EMPTY

TH6H1
IC

MH1 STANDOFF MH1

G75861-001

CAD NOTE:
3 PAD

CAD NOTE:
PLACE CB CLOSE TO PIN 72 AND 74

+V3.3A_WLAN

C5V5	C5V6	C5H1	C5H4
0.01UF	0.01UF	0.1UF	10UF
10%	10%	10%	10%
25V	25V	25V	16V
EMPTY	X7R	X7R	X7R
0402	0402	0402	1206
A36096-045	A36096-045	A36096-112	644066-086

160 145 M.2_BT_PCMFRM_CRF_RST_N

R5H21
0
0402
5%
CHIP

CNV_RF_RESET_R_N IN 30

R5H18
75K
1%
1/16W
CHIP
0402

160 145 M.2_BT_PCMOUT_CLKREQ

R5H28
0
0402
5%
CHIP

MODEM_CLKREQ_R IN 30

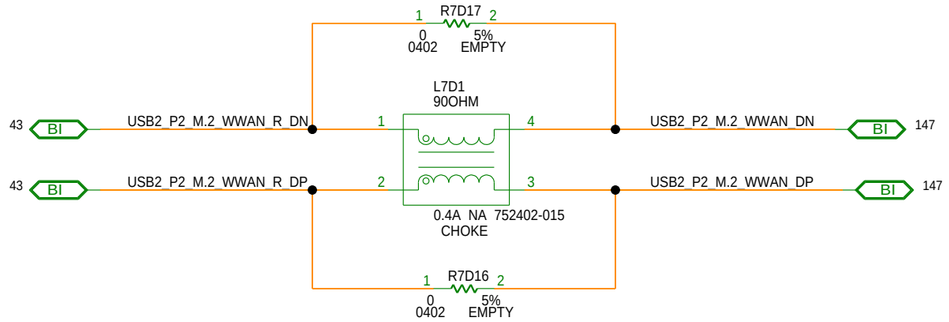
[PAGE_TITLE=CONNECTIVITY - M.2 KEY-E CONNECTOR - WLAN/BT]

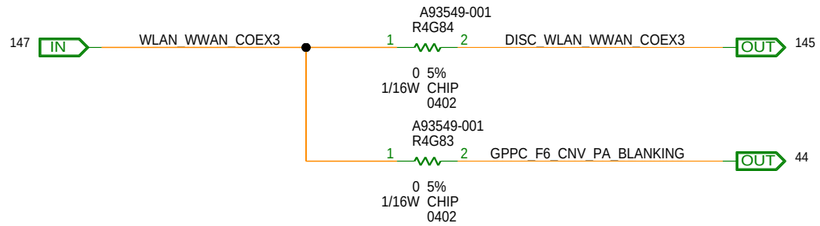
PAGE DRAWING
tigerlake_u_ddr4.sch_1.145
Wed Dec 18 18:07:40 2019

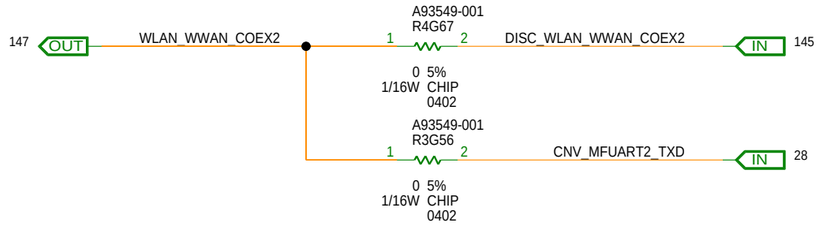
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	145	1.0

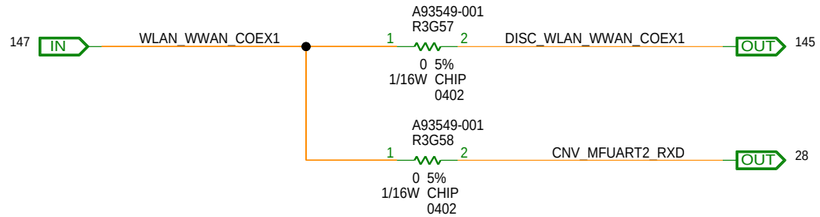
CUSTOM TEXT BPAGE

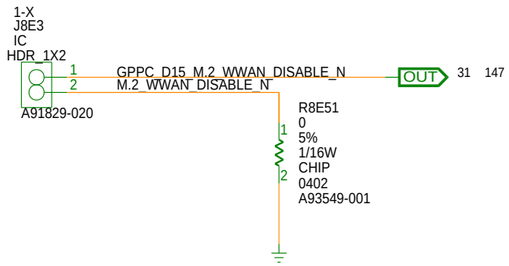
MODULE REV DETAILS		
MODULE NAME	REV	DATE











[PAGE_TITLE=CONNECTIVITY - M.2 KEY-B WWAN - USB CMC, MISC]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.146
Wed Dec 18 18:07:41 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	146	1.0

CUSTOM TEXT BPAGE

M.2 SOCKET 2 : WWAN

JA

J7D2
CONN

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PCIE_M_2_KEY_B

Pin	Signal	Net	Page
1	CONFIG_3	M.2_WWAN_DET_1	
7	USB_D+	USB2_P2_M.2_WWAN_DP (BI)	146
9	USB_D-	USB2_P2_M.2_WWAN_DN (BI)	146
3	GND		
5	GND		
11	GND		
2	3.3V	+V3.3A_WWAN	
4	3.3V	+V3.3A_WWAN	
6	FULL_CARD_POWER_OFF_N	GPPC_C11_WWAN_FCP_OFF_N (IN)	27
8	W_DISABLE1_N	GPPC_D15_M.2_WWAN_DISABLE_N (IN)	31, 146
10	GPIO_9/DAS/DSS_N/LED1_N	M.2_WWAN_LED_N (OUT)	144

MECHANICAL KEY B

Pin	Signal	Net	Page
21	CONFIG_0	TP_M.2_WWAN_DET_21	
23	GPIO_11	TP_M.2_WWAN_WAKE	
25	DPR	SAR_DPR_WWAN (IN)	149
29	PERN1/USB3.0-RX-/SSIC-RXN		
31	PERP1/USB3.0-RX+/SSIC-RXP		
35	PETN1/USB3.0-TX-/SSIC-TXN		
37	PETP1/USB3.0-TX+/SSIC-TXP		
41	PERN0/SATA-B+	PCIE3_P4_M2_WWAN_RX_DN (OUT)	36
43	PERP0/SATA-B-	PCIE3_P4_M2_WWAN_RX_DP (OUT)	36
47	PETN0/SATA-A-	PCIE3_P4_M2_WWAN_TX_DN (IN)	36
49	PETP0/SATA-A+	PCIE3_P4_M2_WWAN_TX_DP (IN)	36
53	REFCLKN	CLK_SRC2_M2_WWAN_DN (IN)	46
55	REFCLKP	CLK_SRC2_M2_WWAN_DP (IN)	46
59	ANTCTL0	TP_M.2_WWAN_ANTCTL0	
61	ANTCTL1	TP_M.2_WWAN_ANTCTL1	
63	ANTCTL2	TP_M.2_WWAN_ANTCTL2	
65	ANTCTL3	TP_M.2_WWAN_ANTCTL3	
67	RESET_N	GPPC_C10_WWAN_RST_N (IN)	27, 147
69	CONFIG_1	M2_WWAN_SSD_DET	
75	CONFIG_2	M.2_WWAN_DET_75	
27	GND		
33	GND		
39	GND		
45	GND		
51	GND		
57	GND		
71	GND		
73	GND		
MTG76	MTG76		
MTG77	MTG77		
20	GPIO_5	M.2_WWAN_SNDWCLK_I2S3_BCLK (IN)	162
22	GPIO_6	M.2_WWAN_I2S3_OUT (IN)	29
24	GPIO_7	M.2_WWAN_SNDWDATA_I2S3_IN (OUT)	162
26	GPIO_10	GNSS_DISABLE_N	
28	GPIO_8	M.2_WWAN_I2S3_LRCLK (IN)	29
30	UIM-RESET	M.2_WWAN_UIM1_RST_N (OUT)	148
32	UIM-CLK	M.2_WWAN_UIM1_CLK (OUT)	148
34	UIM-DATA	M.2_WWAN_UIM1_DATA (BI)	148
36	UIM-PWR		
38	DEVSLP	TP_M.2_WWAN_DEVSLP_NC	
40	GPIO_0	M.2_SIM2_DET (IN)	148
42	GPIO_1	M.2_WWAN_UIM2_DATA (BI)	148
44	GPIO_2	M.2_WWAN_UIM2_CLK (OUT)	148
46	GPIO_3	M.2_WWAN_UIM2_RST_N (OUT)	148
48	GPIO_4		
50	PERST_N	M.2_WWAN_PERST_R_N (IN)	41
52	CLKREQ_N	CLKREQ2_WWAN_SSD_N (OUT)	48
54	PEWAKE_N	GPPC_C9_M.2_WWAN_WAKE_N (OUT)	27
56	NC	TP_M.2_WWAN_NC_56	
58	NC	TP_M.2_WWAN_NC	
60	COEX3	WLAN_WWAN_COEX3 (OUT)	146
62	COEX2	WLAN_WWAN_COEX2 (IN)	146
64	COEX1	WLAN_WWAN_COEX1 (OUT)	146
66	SIM_DETECT	M.2_SIM1_DET (IN)	148
68	SUSCLK	TP_WWAN_SUS_CLK (TP) TP6D2 SM 1	
70	3.3V	+V3.3A_WWAN	
72	3.3V	+V3.3A_WWAN	
74	3.3V	+V3.3A_WWAN	

G63994-001

CONFIG 1 = GND/0 FOR WWAN

+V3.3A_WWAN
R7D15 100K 1% 1/16W EMPTY 0402 A93548-128

R7D22 100K 1% 1/16W EMPTY 0402 A93548-128

+V3.3A_WWAN
R6D23 100K 1% 1/16W EMPTY 0402 A93548-128
R6D22 100K 1% 1/16W EMPTY 0402 A93548-128

+V1.8A
R6D20 10K 5% CHIP 0402
GPPC_C10_WWAN_RST_N 27 147

+V3.3A_WWAN
R6E5 10K 5% CHIP 0402

+V3.3A_WWAN
R7P15 10K 5% EMPTY 0402

+V1.8A
R7P12 10K 5% EMPTY 0402

+V_UIM1_PWR

+V_UIM2_PWR

+V3.3A_WWAN
R6P5 100K 1% CHIP 0402

+V3.3A_WWAN
C7D7 0.01UF 10% 25V X7R 0402 A36096-045 (CA)
C7D8 0.1UF 10% 25V X7R 0402 A36096-112 (CA)
C7E1 100UF 20% 10V X5R 1206 108426-203 (CA)
C7D9 33PF 5% 50V C0G 0402 A36095-031

CAD NOTE:
PLACE CA
CLOSE TO PINS 70, 72, 74 OF JA

+V3.3A_WWAN
C6E2 0.01UF 10% 25V X7R 0402 A36096-045 (CB)
C6E1 0.1UF 10% 25V X7R 0402 A36096-112 (CB)
C7E2 100UF 20% 10V X5R 1206 108426-203 (CB)
C6E3 33PF 5% 50V C0G 0402 A36095-031

CAD NOTE:
PLACE CB
CLOSE TO PINS 2, 4 OF JA

TH7F1
IC
MH1 STANDOFF
G75861-001

[PAGE_TITLE=CONNECTIVITY - M.2 KEY-B WWAN - CONNECTOR]

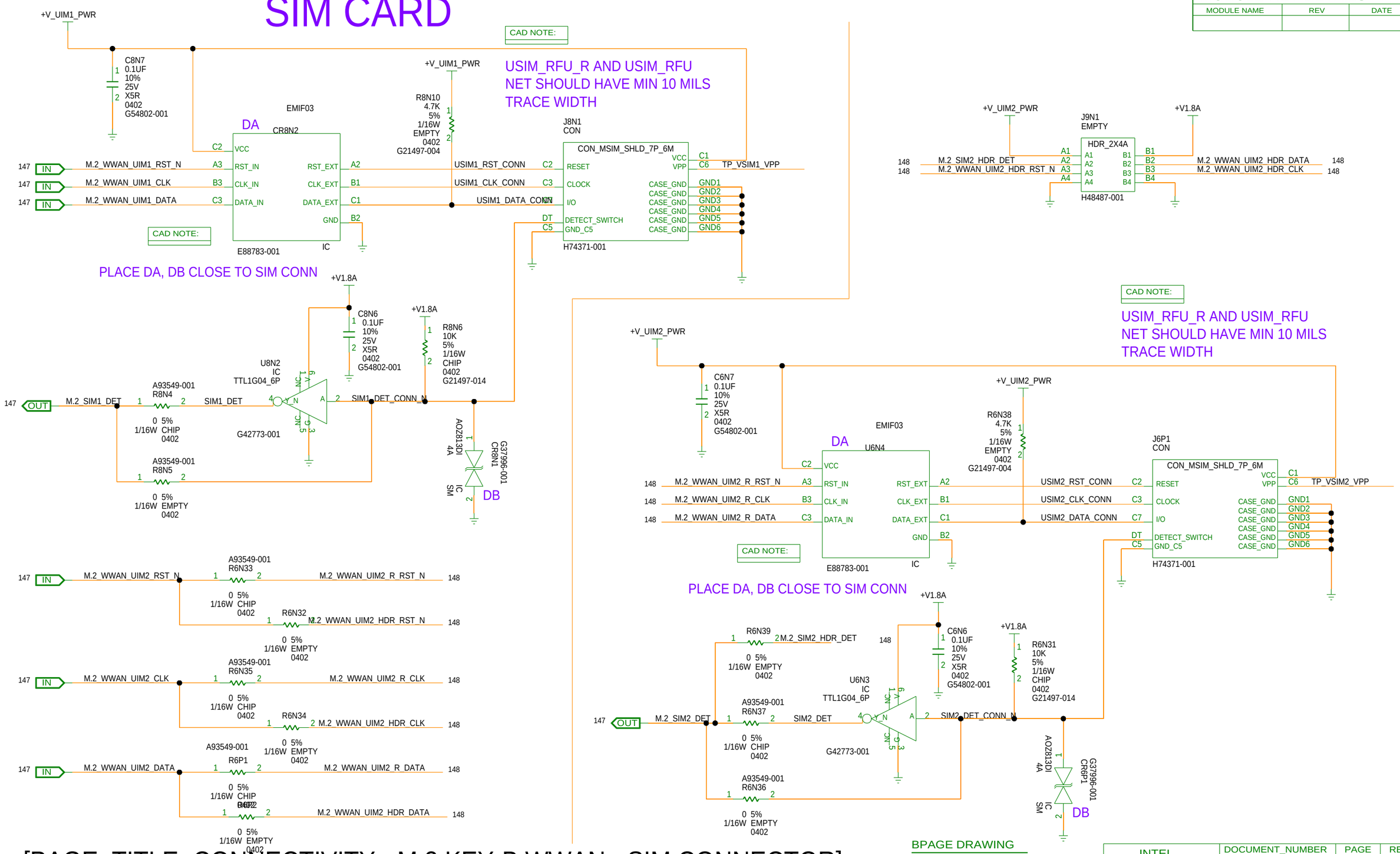
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.147
Wed Dec 18 18:07:42 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	147	1.0

CUSTOM TEXT BPAGE

SIM CARD

MODULE REV DETAILS		
MODULE NAME	REV	DATE



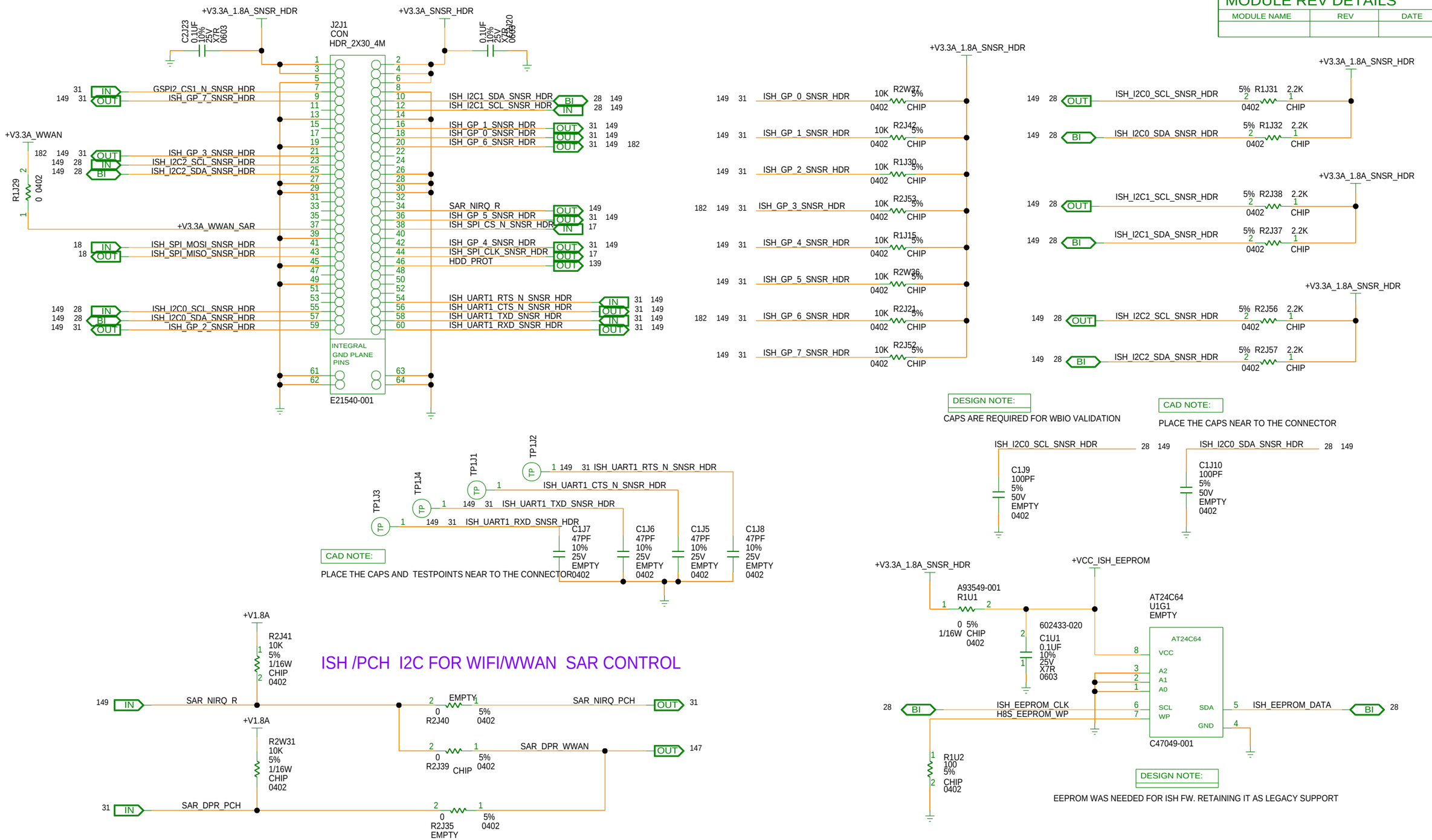
[PAGE_TITLE=CONNECTIVITY - M.2 KEY-B WWAN - SIM CONNECTOR]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.148
Wed Dec 18 18:07:43 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	148	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



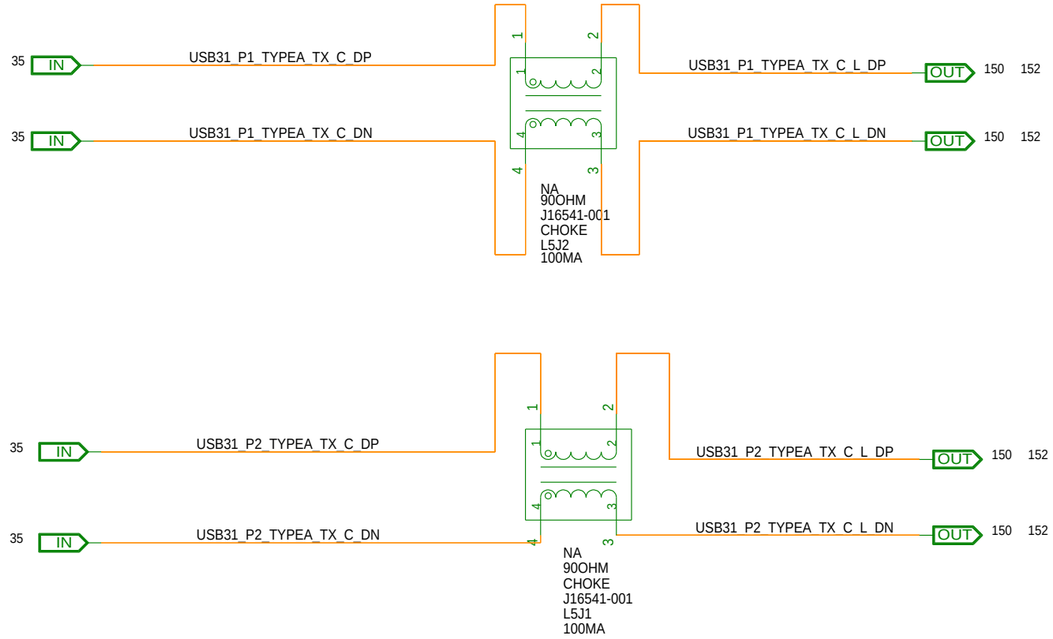
[PAGE_TITLE=SENSOR HEADER]

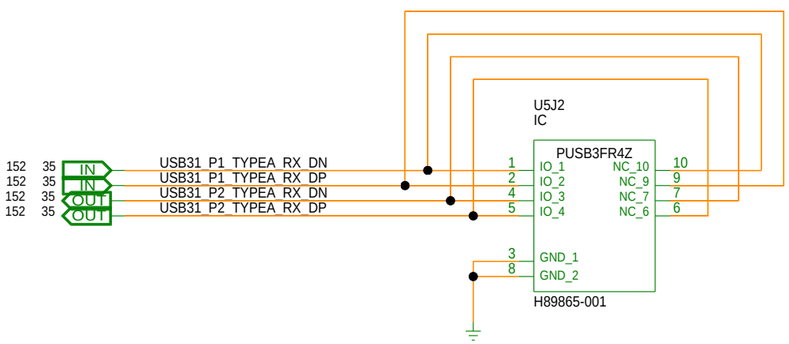
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.149
Wed Dec 18 18:07:44 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	149	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

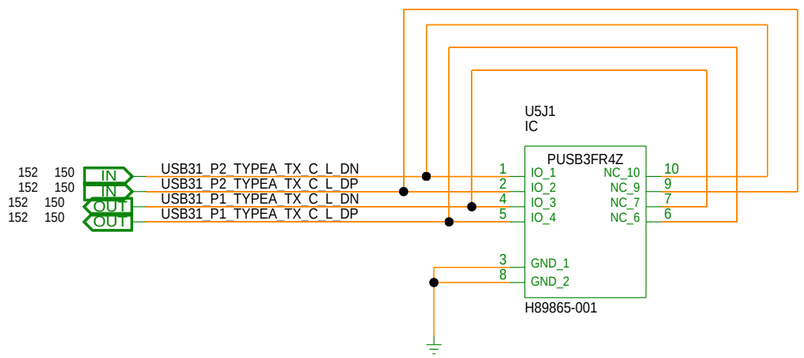
USB3.1 CMC/ESD





CAD NOTE:

PLACE ESD PROTECTION DIODE CLOSE TO TYPE-A CONNECTOR



CAD NOTE:

PLACE ESD PROTECTION DIODE CLOSE TO TYPE-A CONNECTOR

[PAGE_TITLE=USB 3/2 TYPE-A CONNECTOR -1&2 STACKED POWER SWITCH]

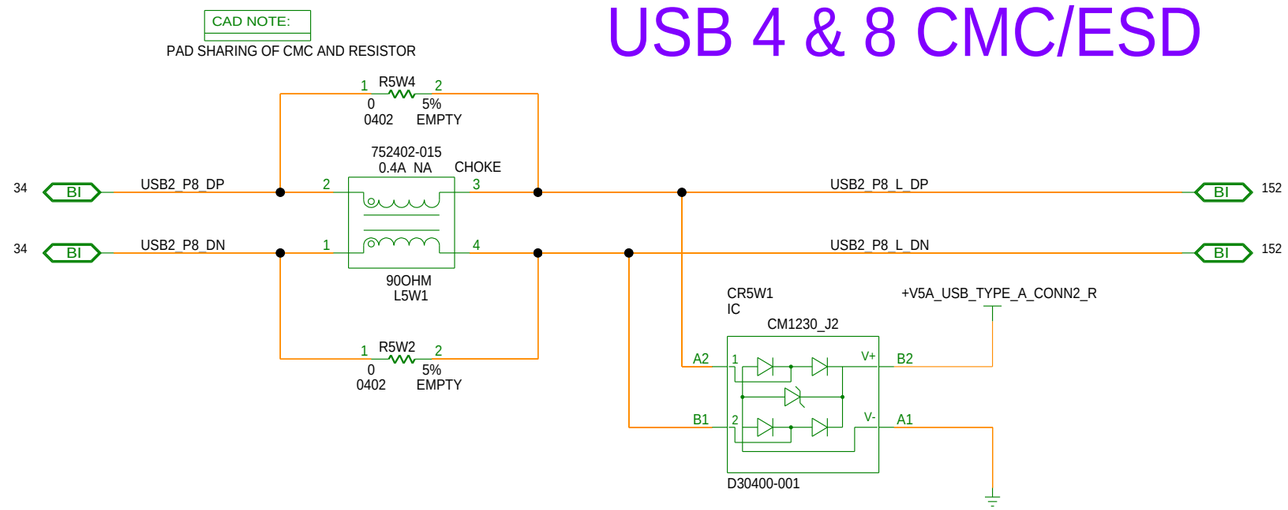
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.150
Wed Dec 18 18:07:46 2019

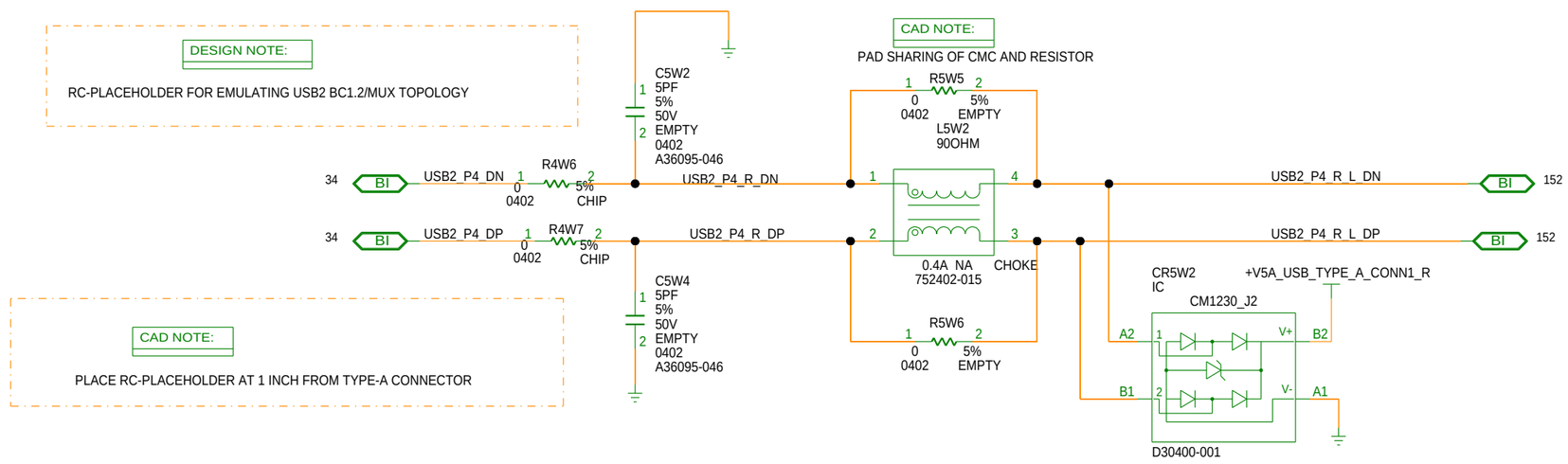
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	150	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

USB 4 & 8 CMC/ESD





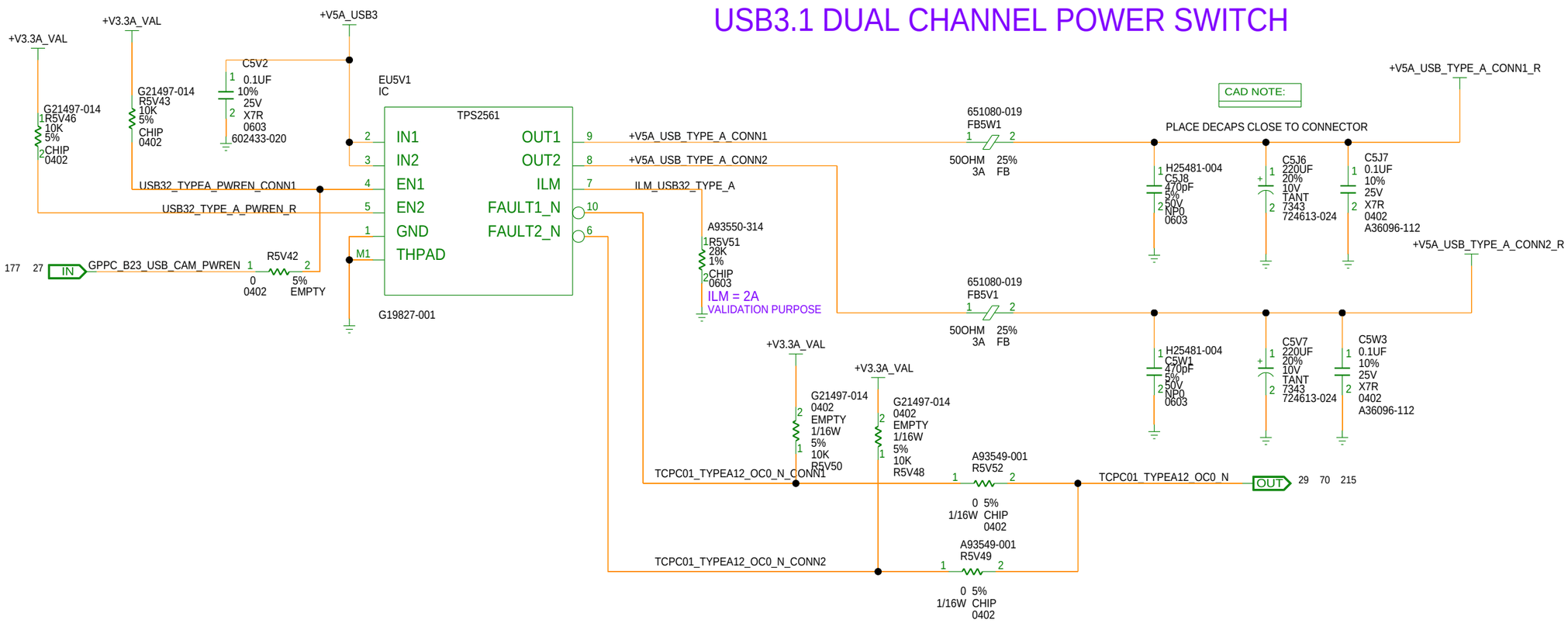
[PAGE_TITLE=USB 3/2 TYPE-A CMC AND ESD]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.151
Wed Dec 18 18:07:47 2019

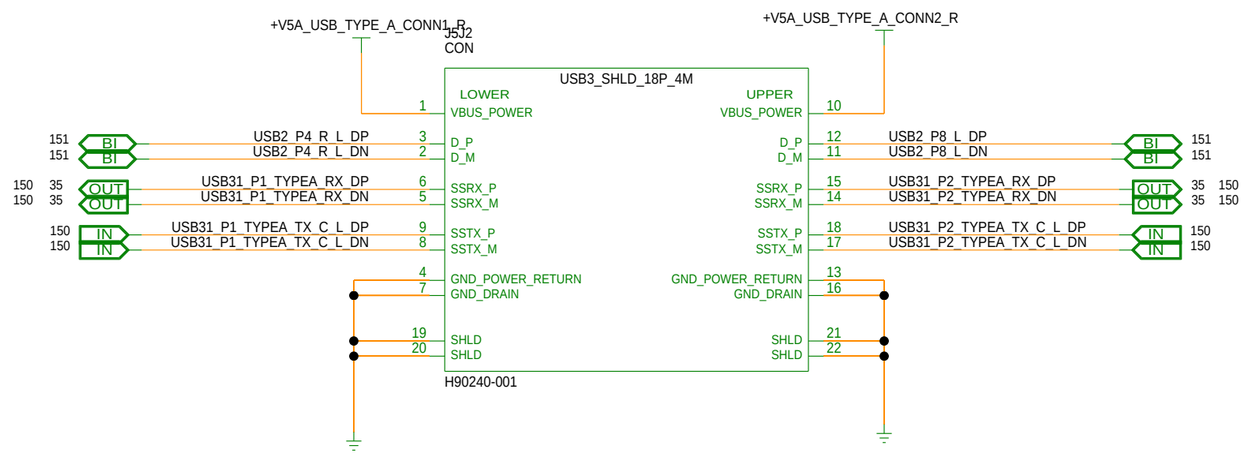
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	151	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

USB3.1 DUAL CHANNEL POWER SWITCH



USB3.1 TYPE-A STACKED PORT



[PAGE_TITLE=USB 3/2 TYPE-A CONNECTOR -1&2 STACKED]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.152
Wed Dec 18 18:07:48 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	152	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=RESERVE]

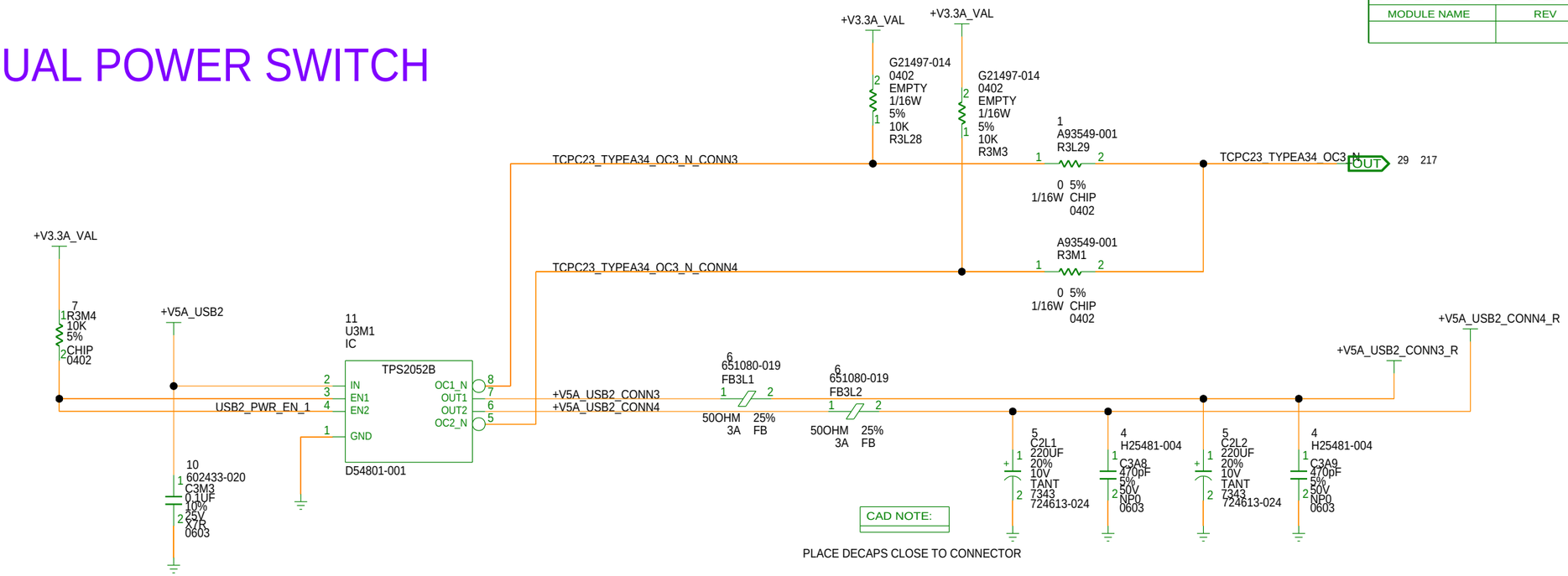
BPAGE DRAWING

tigerlake_u_ddr4.sch_1.153
Tue Oct 15 12:50:51 2019

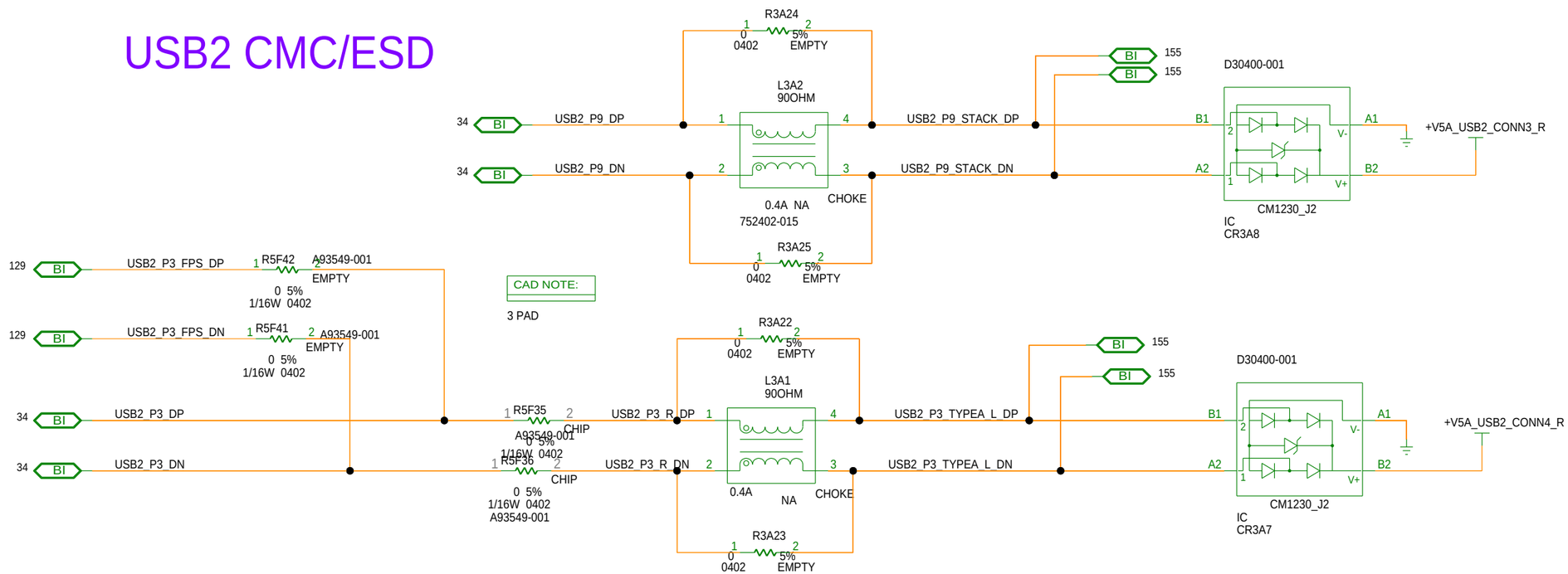
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	153	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

USB2 DUAL POWER SWITCH



USB2 CMC/ESD



[PAGE_TITLE=USB 2 TYPE-A CONNECTOR - 3&4 STACKED CMC, ESD]

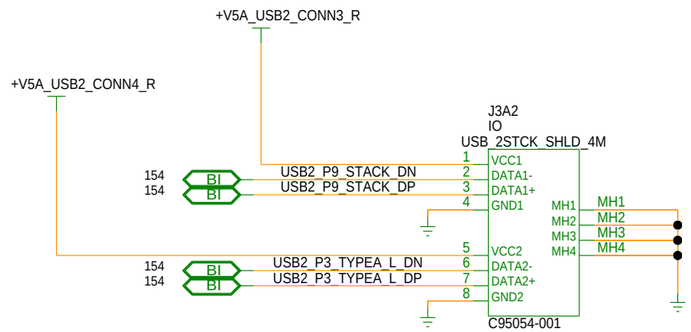
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.154
Wed Dec 18 18:07:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	154	1.0

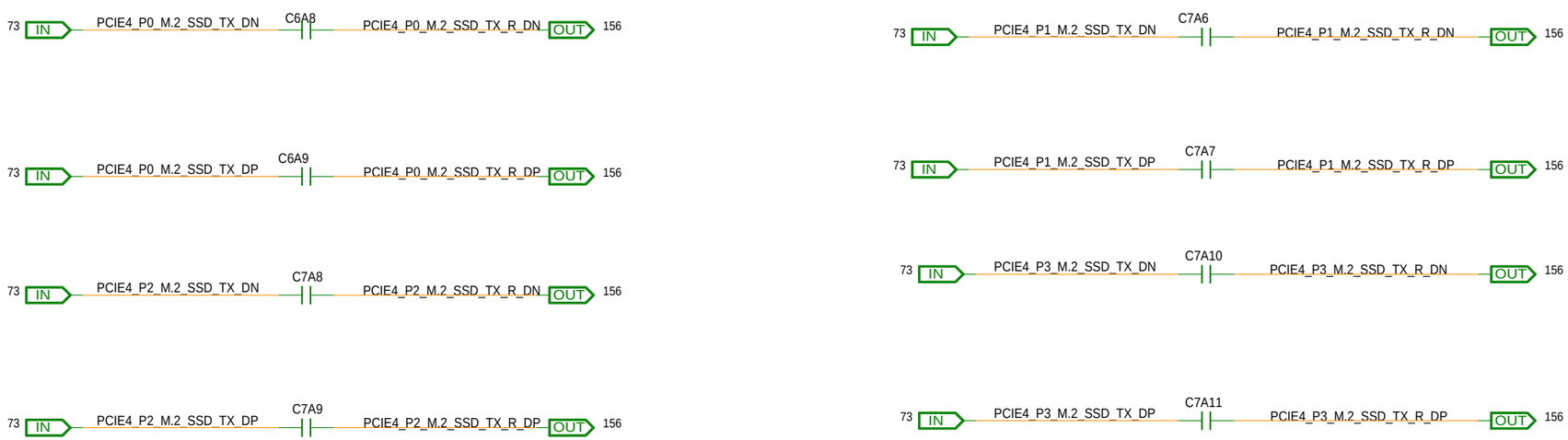
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

USB2 STACK CONNECTOR
PORT 9 & 10



PCIE GEN4 CAP



ALL CAPS STUFFED
0.22UF
10%
10V
0402

[PAGE_TITLE=USB 2 TYPE-A CONNECTOR AND PCIE GEN4 CMC]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.155
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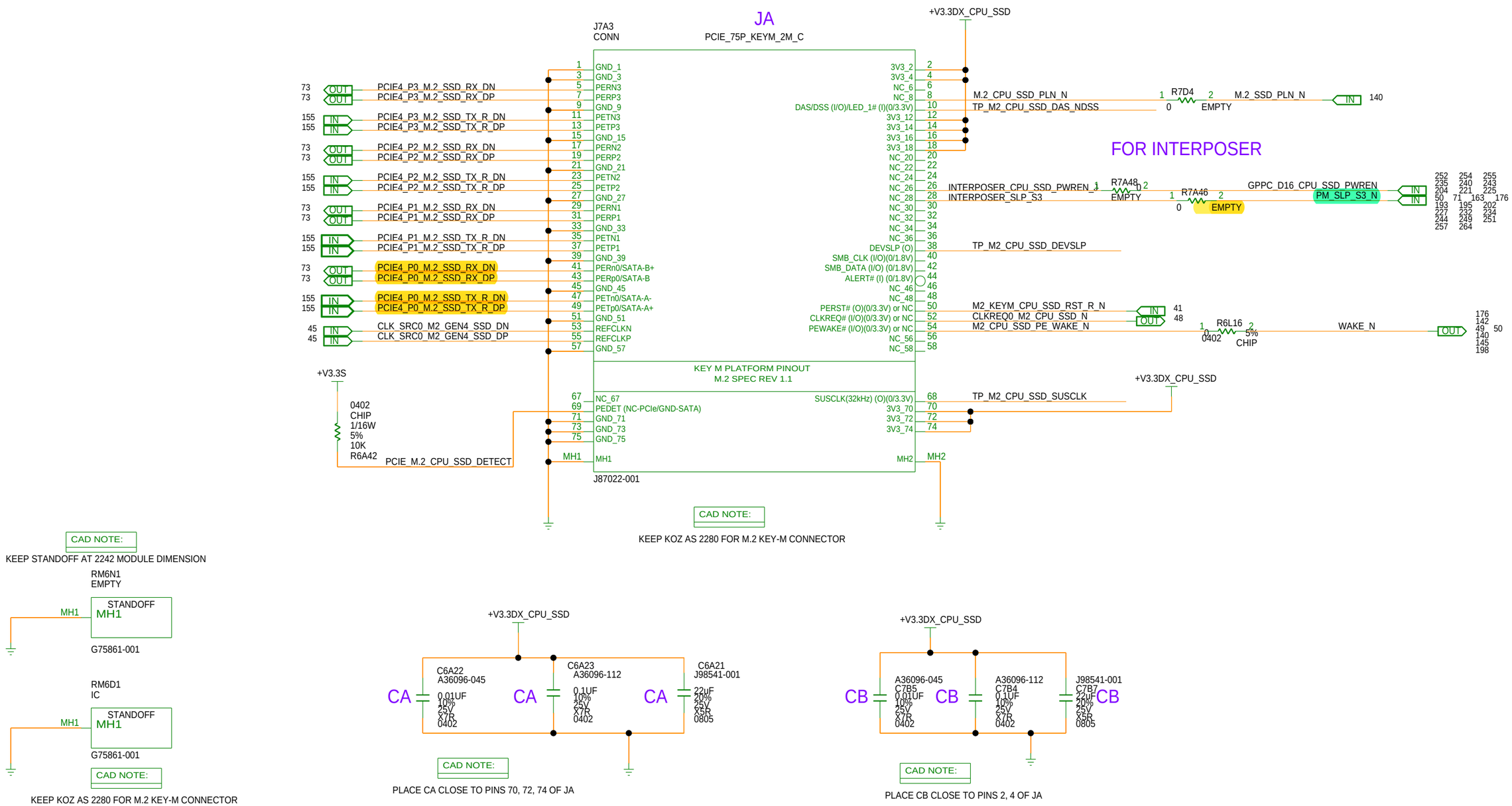
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	155	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PCIE GEN4 SSD



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BPAGE DRAWING
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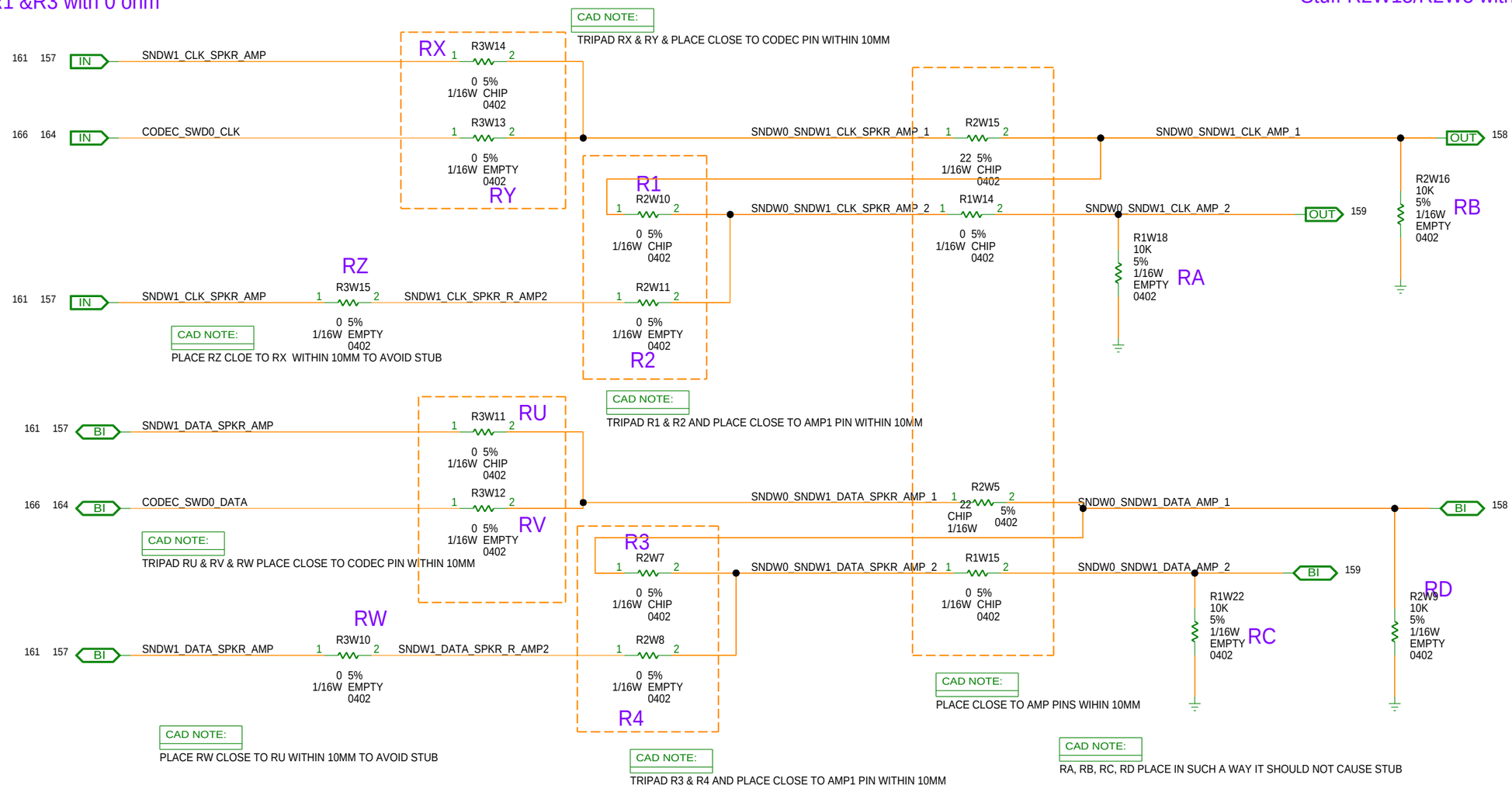
MODULE REV DETAILS		
MODULE NAME	REV	DATE

1-load codec
empty R3W13/R3W12

3-load codec (daisy chain)
Stuff R3W13/R3W12 (RY/RV) with 0ohm
Empty R3W14/R3W11 (RX/RU)
Stuff R2W15/R2W5 and R1W14/R1W15 with 0 ohm
Stuff R1 &R3 with 0 ohm

1-load Speaker Amp
Empty RX/RU, RY/RV and R1/R3
Stuff RZ/RW and R2/R4 with 0 ohm
Stuff R1W14/R1W15 with 0 ohm

2-Load Speaker Amp (Daisy)
Stuff RX/RU and R1/R3 with 0 ohm
Empty RY/RV and RZ/RW
Stuff R1W14/R1W15 with 0 ohm
Stuff R2W15/R2W5 with 22 ohm



[PAGE_TITLE= SOUND WIRE OPTION FOR SPEAKER AMP

BPAGE DRAWING
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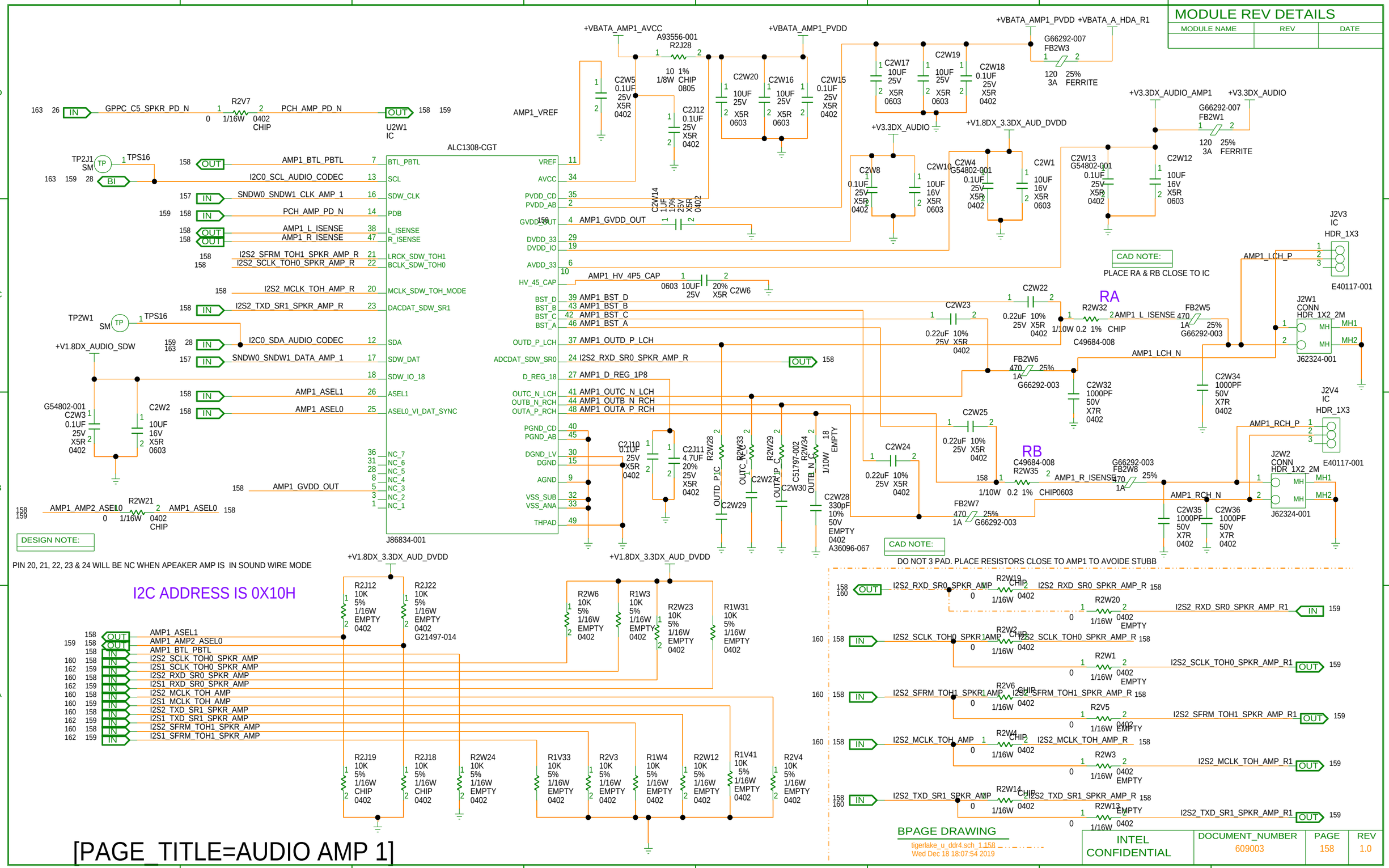
Wed Dec 18 18:07:52 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	157	1.0

CUSTOM TEXT BPAGE

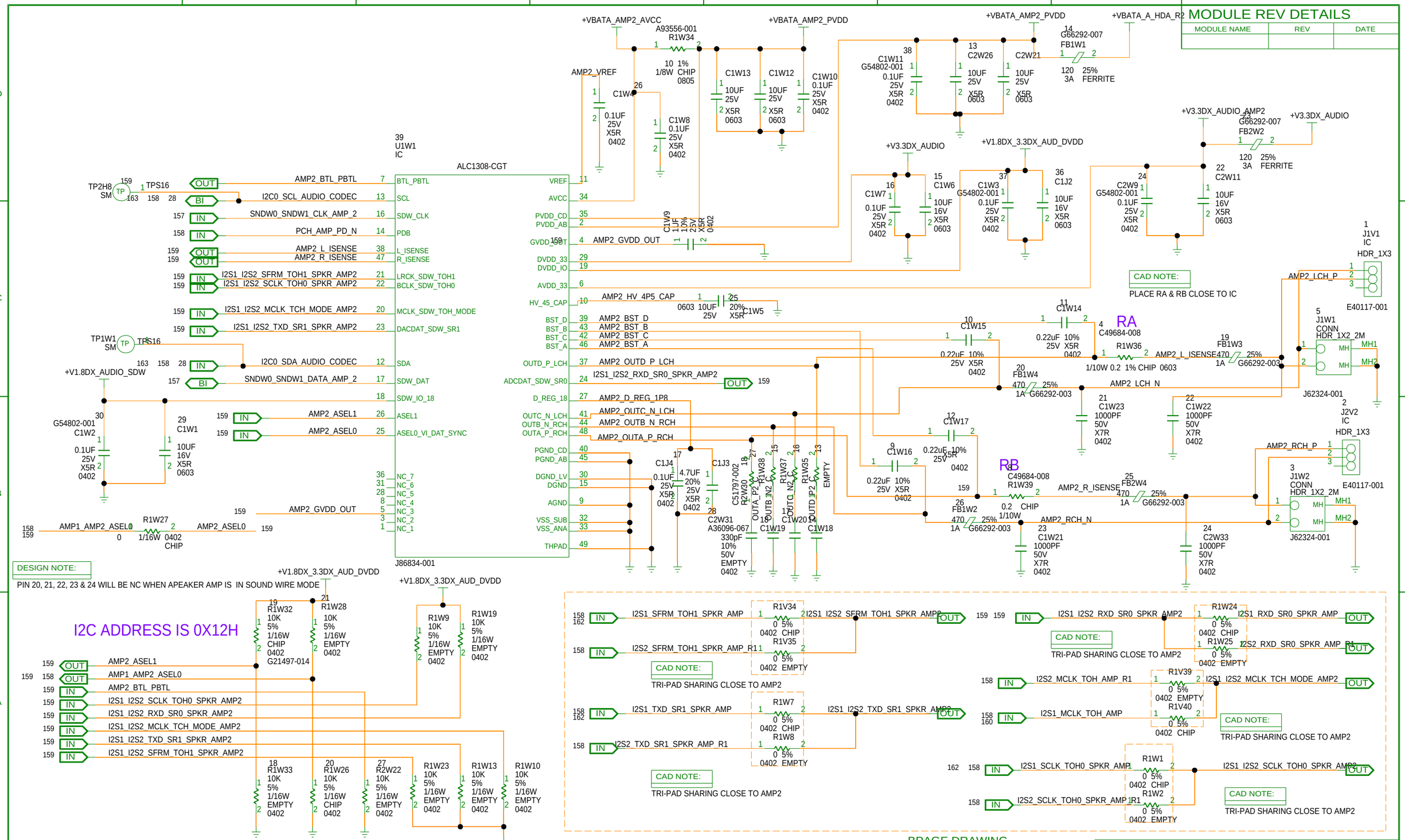
MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=AUDIO AMP 1]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	158	1.0

CUSTOM TEXT BPAGE


MODULE REV DETAILS
MODULE NAME
REV
DATE
ALC1308-CGT
U1W1 IC
J86834-001
AMP2_BTL_PBTL
I2C0_SCL_AUDIO_CODEC
SNDW0_SNDW1_CLK_AMP_2
PCH_AMP_PD_N
AMP2_L_ISENSE
AMP2_R_ISENSE
I2S1_I2S2_SFRM_TOH1_SPKR_AMP2
I2S1_I2S2_SCLK_TOH0_SPKR_AMP2
I2S1_I2S2_MCLK_TCH_MODE_AMP2
I2S1_I2S2_TXD_SR1_SPKR_AMP2
I2C0_SDA_AUDIO_CODEC
SNDW0_SNDW1_DATA_AMP_2
AMP2_ASEL1
AMP2_ASEL0
AMP2_GVDD_OUT
AMP2_HV_4P5_CAP
AMP2_BST_D
AMP2_BST_B
AMP2_BST_C
AMP2_BST_A
AMP2_OUTD_P_LCH
I2S1_I2S2_RXD_SR0_SPKR_AMP2
AMP2_D_REG_1P8
AMP2_OUTC_N_LCH
AMP2_OUTB_N_RCH
AMP2_OUTA_P_RCH
AMP1_AMP2_ASEL0
+V1.8DX_AUDIO_SDW
+V1.8DX_3.3DX_AUD_DVDD
+VBATA_AMP2_AVCC
+VBATA_AMP2_PVDD
+VBATA_A_HDA_R2
+V3.3DX_AUDIO_AMP2
+V3.3DX_AUDIO
AMP2_LCH_P
AMP2_LCH_N
AMP2_RCH_P
AMP2_RCH_N
AMP2_L_ISENSE
AMP2_R_ISENSE
J1V1 IC HDR_1X3
J2V2 IC HDR_1X3
J1W1 CONN HDR_1X2_2M
J1W2 CONN HDR_1X2_2M
J62324-001
E40117-001
RA
RB
CAD NOTE:
PLACE RA & RB CLOSE TO IC
DESIGN NOTE:
PIN 20, 21, 22, 23 & 24 WILL BE NC WHEN APEAKER AMP IS IN SOUND WIRE MODE
I2C ADDRESS IS 0X12H
TRI-PAD SHARING CLOSE TO AMP2
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.159
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[PAGE_TITLE=AUDIO AMP 2]

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE:
REFER TO PDG FOR CAP PLACEMENT

CAD NOTE:
3 PAD SHARING

204 24 IN GPP_R0_HDA_BCLK_I2S0_SCLK
TP2G1 SM TP 1 TPS16
R2G3 1 2 33 1/16W EMPTY 0402 — HDA_CODEC_BCLK — OUT 166
R2G2 1 2 33 1/16W EMPTY 0402 — HDA_BCLK_I2S0_SCLK_HDR — OUT 163 164

24 IN GPP_R1_HDA_SYNC_I2S0_SFRM
R3F73 1 2 33 1/16W EMPTY 0402 — HDA_CODEC_SYNC — OUT 166
R3F74 1 2 33 1/16W EMPTY 0402 — HDA_SYNC_I2S0_SFRM_HDR — OUT 163 164

262 24 IN GPP_R2_HDA_SDO_I2S0_TXD
R3F59 1 2 33 1/16W EMPTY 0402 — HDA_CODEC_SDO — OUT 166
R3F60 1 2 33 1/16W EMPTY 0402 — HDA_SDO_I2S0_TXD_HDR — OUT 163 164

24 OUT GPP_R3_HDA_SDI_0_I2S0_RXD
R4F10 0402 1 2 0 1/16W CHIP — HDA_SDI_0_I2S0_RXD_R
A93549-005
R3J35 1 2 33 1/16W EMPTY 0402 — HDA_CODEC_SDI — IN 166
R3J34 1 2 33 1/16W EMPTY 0402 — HDA_SDI0_I2S0_RXD_HDR — IN 163 164

TP3J7 SM TP 1 TPS16

CAD NOTE:
SDI: PLACE R AND C CLOSE TO CODEC, OTHERS: PLACE CLOSE TO PCH

DESIGN NOTE:
OPEN: UNSTUFF HDA TO CODEC IF SNDW NEEDS TO BE DEF

24 IN GPPC_F_8_I2S_MCLK_IN
R4F13 1 2 33 1/16W EMPTY 0402 — I2S_MCLK_IN_HDR — OUT 163

CAD NOTE:
TRI-PAD, PLACE CLOSE TO PCH

DESIGN NOTE:
HDA_CODEC_RESTO IS OUTPUT FROM CODEC AND SHOULD NOT BE CONNECTED TO PCH

R2G8 1 2 33 1/16W EMPTY 0402 — HDA_CODEC_RESETO — IN 166

204 24 IN GPP_R4_HDA_RST_N
R2G9 1 2 33 1/16W EMPTY 0402 — HDA_RST_N_HDR
R3J4 1 2 0 1/16W EMPTY 0402 — HDA_RST_N_I2S_MCLK_HDR — OUT 163

R4F57 1 2 33 1/16W EMPTY 0402 — I2S0_MCLK_HDR
R3J6 1 2 0 1/16W EMPTY 0402

CAD NOTE:
TRI-PAD, PLACE CLOSE TO HDR

24 IN GPPC_D_19_I2S_MCLK_OUT
R4F42 1 2 33 1/16W CHIP 0402 — I2S1_MCLK_R_HDR
R2J27 1 2 0 1/16W CHIP0402 — I2S1_MCLK_HDR — OUT 163
R2J26 1 2 0 1/16W EMPTY 0402 — I2S1_MCLK_TOH_AMP — OUT 158 159

CAD NOTE:
DO NOT TRI-PAD, PLACE THEM V CLOSE AND ALSO CLOSE TO PCH
R4F54 1 2 33 0402 5% EMPTY — I2S2_MCLK_TOH_AMP — OUT 158

DESIGN NOTE:
FOLLOW PDG RECOMENDATION FOR I2S SERIES RES
FOR I2S MASTER MODE USE 33 OHM FOR SLAVE MODE USE 13 OHM SERIES RESISTOR

CAD NOTE: PLACE CLOSE TO PCH SERIRES RESISTOR

CAD NOTE: 3 PAD SHARING, PLACE CLOSE TO PCH

DESIGN NOTE:
CAP IS ADDED TO MEET EMC REQUIREMENT FOR DMIC INTERFACE

24 IN GPPC_A7_I2S2_SCLK_DMIC_CLK_A0
R3F68 1 2 33 0402 5% CHIP — M.2_BT_PCMCLK — OUT 145
R3F67 1 2 22 0402 5% EMPTY — I2S2_SCLK_DMIC_CLK_A0_HDR — OUT 163 164
R3F69 1 2 33 0402 5% EMPTY — I2S2_SCLK_TOH0_SPKR_AMP — OUT 158

204 24 IN GPPC_A8_I2S2_SFRM_DMIC_DATA0_CNV_RF_RESET_N
R3F63 1 2 33 0402 5% CHIP — M.2_BT_PCMFRM_CRF_RST_N — OUT 145
R3F62 1 2 33 0402 5% EMPTY — I2S2_SFRM_DMIC_DATA0_HDR — OUT 163 164
R3F61 1 2 33 0402 5% EMPTY — I2S2_SFRM_TOH1_SPKR_AMP — OUT 158

C3F10 1 2 27PF 5% 50V EMPTY 0402 A36095-038

24 IN GPPC_A9_I2S2_TXD_DMIC_CLK_A1_MODEM_CLKREQ
R3F92 1 2 33 0402 5% CHIP — M.2_BT_PCMOUT_CLKREQ — OUT 145
R3F91 1 2 22 0402 5% EMPTY — I2S2_TXD_DMIC_CLK_A1_HDR — OUT 163 164
R3F93 1 2 33 0402 5% EMPTY — I2S2_TXD_SR1_SPKR_AMP — OUT 158

24 OUT GPPC_A10_I2S2_RXD_DMIC_DATA1
R3F70 1 2 33 0402 5% CHIP — M.2_BT_PCMIN — IN 145
R3F72 1 2 33 0402 5% EMPTY — I2S2_RXD_DMIC_DATA1_HDR — IN 163 164
R3F71 1 2 33 0402 5% EMPTY — I2S2_RXD_SR0_SPKR_AMP — IN 158

C3F11 1 2 27PF 5% 50V EMPTY 0402 A36095-038

[PAGE_TITLE=AUDIO - PORT SHARING OPTIONS - HAD/I2S/SNDW - 1]

BPAGE DRAWING
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	609003	160	1.0

CUSTOM TEXT BPAGE

SNDW1 STAR TOPOLOGY

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE: TRIPAD RX & RY, RZ

CAD NOTE: PLACE RA & C1 CLOSE TO PCH

24 IN GPP_S2_SNDW1_CLK_DMIC_CLK_B0_RGMII_RESET — R3F80 (RA) A93549-001 1/16W CHIP 0402 — SNDW1_CLK_DMIC_CLK_B0_RGMII_RESET_R

C3F12 27PF 5% 50V EMPTY 0402 A36095-038 (C1)

SNDW1_CLK_DMIC_CLK_B0_RGMII_RESET_R → R3F96 (RZ) 1/16W EMPTY0402 → SNDW1_CLK_SPKRFLEX → OUT 161

SNDW1_CLK_DMIC_CLK_B0_RGMII_RESET_R → R3F98 (RY) A93549-001 1/16W CHIP 0402 → SNDW1_CLK_SPKR_AMP → OUT 157

SNDW1_CLK_DMIC_CLK_B0_RGMII_RESET_R → R3F97 (RX) A93549-001 1/16W EMPTY 0402 → SNDW1_CLK_RGMII_RESET_R

R1 (R1H43) A93549-059 4.7 5% 0402 1/16W CHIP

DESIGN NOTE: R1 = 4.7E FOR STAR

SNDW1_CLK_RGMII_RESET_R1 → R3 (R1H63) 1/16W EMPTY0402 A93549-030 → SNDW1_CLK_HDR_1_RGMII_RESET → OUT 163 165

SNDW1_CLK_RGMII_RESET_R1 → R2 (R1H51) 1/16W EMPTY0402 A93549-030 → SNDW1_CLK_HDR_2 → OUT 163

CAD NOTE: DO NOT TRI PAD R3, R2

2-load speaker flex
Stuff RA/RD with 13 ohm
Stuff RZ/RU with 0 ohm
Empty RY/RV, RX/RW

1-load speaker amp
Stuff RA/RD with 13 ohm
Stuff RY/RV with 0 ohm
Empty RZ/RU and RX/RW

CAD NOTE: PLACE RD & CC CLOSE TO PCH

24 IN GPP_S3_SNDW1_DATA_DMIC_CLK_B1_RGMII_PPS — R3G14 (RD) A93549-001 1/16W CHIP 0402 — SNDW1_DATA_DMIC_CLK_B1_RGMII_PPS_R

C3G5 27PF 5% 50V EMPTY 0402 A36095-038 (CC)

SNDW1_DATA_DMIC_CLK_B1_RGMII_PPS_R → R3G6 (RU) 1/16W EMPTY0402 → SNDW1_DATA_SPKRFLEX → OUT 161

SNDW1_DATA_DMIC_CLK_B1_RGMII_PPS_R → R3G5 (RV) 1/16W CHIP 0402 → SNDW1_DATA_SPKR_AMP → OUT 157

SNDW1_DATA_DMIC_CLK_B1_RGMII_PPS_R → R3G4 (RW) A93549-001 1/16W EMPTY 0402 → SNDW1_DATA_RGMII_PPS_R

R7 (R2H9) A93549-059 4.7 5% 0402 1/16W CHIP

SNDW1_DATA_RGMII_PPS_R1 → R5 (R2H13) 1/16W EMPTY0402 → SNDW1_DATA_HDR_1_RGMII_PPS → BI 163 165

SNDW1_DATA_RGMII_PPS_R1 → R6 (R2H10) 1/16W EMPTY0402 → SNDW1_DATA_HDR_2 → BI 163

CAD NOTE: TRIPAD RU & RV, RW

CAD NOTE: PLACE R1, R2, R3 CLOSE TO CONN (FOLLOW PDG), PLACE R2 AND R3 CLOSE SUCH THAT THERE IS NO STUB FOR P2P SNDW2

CAD NOTE: DO NOT TRI PAD R5, R6

CAD NOTE: PLACE R7, R5, R6 CLOSE TO CONN (FOLLOW PDG), PLACE R2 AND R3 CLOSE SUCH THAT THERE IS NO STUB FOR P2P SNDW2

2-load speaker amp
Stuff RA/RD with 0ohm
Stuff RY/RV with 0 ohm
Empty RZ/RU and RX/RW

2-load star
Stuff RA/RD and RX/RW with 0 ohm
Stuff R1/R7 with 4.7 ohm
Stuff R2/R6 and R3/R5 with 20ohm
Empty RZ/RU and RY/RV

FLEX CONN FOR SDW SPKR

+VBATA_SDW

C3J22 10UF 25V X5R 0805

C3J18 0.1UF 25V X5R 0402

+V1.8DX_AUDIO_SDW

C3J21 0.1UF G54802-00125V X5R 0402

+V1.8DX_AUDIO_SDW

+VBATA_SDW

J3J3 CONN CON_2X3_4M

161 BI SNDW1_CLK_SPKRFLEX — R3W23 1/16W CHIP 0402 — SNDW1_CLK_SPKRFLEX_HDR

B1 B2 B3 MH1 MH3 — A1 A2 A3 MH2 MH4

J49951-001 (JF)

SNDW1_DATA_SPKRFLEX_HDR — R3W22 1/16W CHIP 0402 — SNDW1_DATA_SPKRFLEX → IN 161

CAD NOTE: PLACE C5 CLOSE TO RY, PLACE THESE CLOSE TO PCH

24 IN GPP_S4_SNDW2_CLK_DMIC_CLK_A1 — R3G1 (RY) 1/16W CHIP 0402 — SDW2_CLK_DMIC_CLK_A1_HDR → OUT 165

C3G1 27PF 5% 50V EMPTY 0402 A36095-038 (C5)

R2H4 100K 1% 1/16W EMPTY 0402 A93548-128

SNDW2 header:
Stuff RY/RZ with 13 ohm
Stuff R2H5/R2G30 with 0 ohm
DMIC1:
Stuff RY with 33 ohm
Stuff RZ with 0 ohm

24 BI GPP_S5_SNDW2_DATA_DMIC_DATA1 — R3U3 (RZ) 1/16W CHIP 0402 — SDW2_DATA_DMIC_DATA1_HDR → BI 165

CAD NOTE: PLACE RZ CLOSE TO PCH

[PAGE_TITLE=AUDIO - PORT SHARING OPTIONS -HDA/I2S/SNDW - 2]

BPAGE DRAWING
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	161	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

24 IN GPP_R7_I2S1_SFRM — R4F41 33 1/16W EMPTY 0402 — I2S1_SFRM_HDR — OUT 163
CAD NOTE: TRI PAD SHARE, PLACE CLOSE TO PCH
R4F40 33 1/16W CHIP 0402 — I2S1_SFRM_TOH1_SPKR_AMP — OUT 158 159

24 IN GPP_R6_I2S1_TXD — R4F75 33 1/16W EMPTY 0402 — I2S1_TXD_HDR — OUT 163 164
R4F76 0 1/16W CHIP 0402 — GPP_R6_CAM2_PWREN — OUT 130
R4F77 33 1/16W EMPTY 0402 — I2S1_TXD_SR1_SPKR_AMP — OUT 158 159
CAD NOTE: 33 AND 0 OHMS RESISTORS CLOSER TO SOC; PAD SHARING

204 24 OUT GPP_R5_HDA_SDI_1_I2S1_RXD — R3F45 33 1/16W EMPTY 0402 — GPP_R5_HDA_SDI_1_R_IS1_RXD
R3J44 0 1/16W CHIP 0402 — I2S1_RXD_SR0_SPKR_AMP — IN 158 159
R3J43 0 1/16W EMPTY 0402 — HDA_SDI_1_I2S1_RXD_HDR — IN 163
CAD NOTE: TRI PAD SHARE, PLACE CLOSE TO PCH
CAD NOTE: 4 PAD SHARE, PLACE CLOSE TO PCH
R3F47 0 1/16W EMPTY 0402 — GPP_R5_CRD_CAM_PRIVACY_LED_1 — OUT 132
R3F46 0 1/16W CHIP 0402 — GPP_R5_CAM_VSYNC1 — OUT 132

SNDW3 Header:
Stuff RA/R2 with 13 ohm
empty RB/R1
Stuff R2G23/R2H2 with 0ohm

SNDW3 M.2 WWAN:
Stuff RB/R1 with 13 ohm
Empty RA/R2
Stuff RE/R4 with 0 ohm
Empty RF/R3

DMIC0 Header:
Stuf RA with 33 ohm
Stuff R2 with 0ohm
Empty RB/R1
Stuff R2H2 with 0ohm
Stuff R2G23 with 33 ohm

CAD NOTE: TR-PAD R3, R4. PLACE CLOSE TO HDR
17 BI I2S3_RXD_WWAN — R3 R7P10 0 1/16W CHIP 0402 — M.2_WWAN_SNDWDATA_I2S3_IN — BI 147
R7P13 0 1/16W EMPTY 0402 R4

CAD NOTE: TRI PAD SHARE, PLACE CLOSE TO PCH
24 BI GPP_S7_SNDW3_DATA_DMIC_DATA_0 — R1 R4F36 33 1/16W EMPTY0402 — SNDW3_DATA_WWAN
R2 R4F35 13 1/16W CHIP 0402 — SNDW3_DATA_DMIC_DATA_0_R — R2G23 0 1/16W CHIP 0402 — SNDW3_DATA_DMIC_DATA_0_HDR — BI 163 165
166 BI CODEC_GPIO2_DMIC_DATA2_R — R2G24 0 1/16W EMPTY 0402
CAD NOTE: TR1-PAD R1, R2 PLACE CLOSE TO PCH

24 IN GPP_S6_SNDW3_CLK_DMIC_CLK_A0 — A93549-068 R4F44 13 1/16W CHIP 0402 — SNDW3_CLK_DMIC_CLK_A0_R
RA
CA — C4F9 27PF 5% 50V EMPTY 0402 A36095-038
CAD NOTE: PLACE CAP CLOSE TO PCH SERIRES RESISTOR
A93549-001 R2H2 0 1/16W CHIP 0402 — SNDW3_CLK_DMIC_CLK_0_HDR — OUT 163 165
CAD NOTE: TRI-PAD RES; PLACE CLOSE TO CONN
R2H7 100K 1% 1/16W EMPTY 0402 A93548-128
CAD NOTE: 4 PAD SHARE, PLACE CLOSE TO PCH
DESIGN NOTE: CAP IS ADDED TO MEET EMC REQUIREMENT FOR DMIC INTERFACE
165 IN CODEC_DMIC_CLK_R2 — R2H8 0 1/16W EMPTY 0402

RB
R4F43 13 1/16W EMPTY0402 — SNDW3_CLK_WWAN
CAD NOTE: PLACE CA CLOSE TO RA, PLACE THESE CLOSE TO PCH; TRI=PAD RA,, RB
RE
CAD NOTE: TRI-PAD RE, RF; PLACE CLOSE TO CONN
R7P14 0 1/16W EMPTY 0402 — M.2_WWAN_SNDWCLK_I2S3_BCLK — OUT 147
RF
RC
29 IN I2S3_SCLK_WWAN — R7P11 0 1/16W CHIP 0402

TO DMIC HEADER

24 IN GPPC_A23_I2S1_SCLK
RD
R3F22 33 1/16W EMPTY 0402 — I2S1_SCLK_HDR — OUT 163 164
CAD NOTE: TR-PAD RC, RD. PLACE CLOSE TO PCH
R3G8 330 1/16W EMPTY 0402 — 217
R3F20 33 1/16W CHIP 0402 — GPPC_A23_TC_RETIMER_FORCE_PWR — OUT 120 172 215 70 72 106 111 116
R3F21 33 1/16W EMPTY 0402 — I2S1_SCLK_TOH0_SPKR_AMP — OUT 158 159

[PAGE_TITLE=AUDIO - PORT SHARING OPTIONS - DMIC]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.162
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	162	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PM_SLP_S3_N — IN — R3J38 0 1/16W EMPTY 0402

CAD NOTE: 3 PAD

PM_SLP_SUS_N — IN — R3J32 0 1/16W CHIP 0402 — HDA_SDI3_PCH_PWREN — OUT 163

R3J33 330 1/16W EMPTY 0402

GPPC_C5_SPKR_PD_N — IN — R2V8 0 1/16W CHIP 0402 — SPKR_PD_N_HDR_R — BI 163

GPPC_C12_CODEC_INT_N — OUT — R2J8 0 1/16W EMPTY 0402 — CODEC_IRQ_HDR_R — IN 163

BUF_PLT_RST_1.8_R_N — IN — R2J7 0 1/16W CHIP 0402 — BUF_PLT_RST_1V8_AUDIO_HDR_N — OUT 163

+V1.8DX_AUDIO_DVDD — R2W17 2.2K 5% 1/16W EMPTY 0402 — I2C0_SCL_AUDIO_CODEC — IN

+V1.8DX_AUDIO_DVDD — R2W18 2.2K 5% 1/16W EMPTY 0402 — I2C0_SDA_AUDIO_CODEC — BI

I2S1_SFRM_HDR — IN — R3W21 0 1/20W CHIP 0201 — I2S1_SFRM_RXD_HDA_SDI_1_HDR_JB — BI 163 164

HDA_SDI_1_I2S1_RXD_HDR — OUT — R3W20 0 1/20W EMPTY 0201

HDA_SDI_1_I2S1_RXD_HDR — OUT — R3J40 0 1/16W CHIP 0402 — HDA_SDI_1_I2S1_RXD_SFRM_HDR_JA — BI 163 164

I2S1_SFRM_HDR — IN — R3J46 0 1/16W EMPTY 0402

DESIGN NOTE: OPTION ADDED TO SWAP I2S1 SFRM AND I2S1_RXD FOR SV TEAM

CAD NOTE: PAD SHARE

CAD NOTE: PLACE JA, JB, CLOSE

JA

J3J1 HDR HDR_2X8_K12 — A91836-050

HDA_BCLK_I2S0_SCLK_HDR
HDA_RST_N_I2S_MCLK_HDR
HDA_SYNC_I2S0_SFRM_HDR
HDA_SDO_I2S0_TXD_HDR
HDA_SDI0_I2S0_RXD_HDR
HDA_SDI_1_I2S1_RXD_SFRM_HDR_JA
HDA_SDI3_PCH_PWREN
I2S1_SCLK_HDR

+V1.8DX_3.3DX_AUD_DVDDIO
+V_3.3DX_3.3_1.8_DVDD
+VBATA_5DX_AUDIO

R3J1 0 CHIP 5% 1/10W 0603 — +V3.3DX_AUDIO
R3H19 0 CHIP 5% 1/10W 0603 EMPTY — +V1.8DX_3.3DX_AUD_DVDD
R3J20 0 CHIP 5% 1/10W 0603 — +VBATA_A_HDA_R1
R3J23 0 5% 1/10W EMPTY 0603 — +V5DX_AUDIO — G22178-002

CAD NOTE: TRIPAD

CAD NOTE: J3J1 TO J3H4 KOZ TO BE CLEARED. NEED 157MILS GAP BETWEEN ADJACENT 2 HDR'S

JB

J2H5 CON TSM-106-01-L-DV — E15792-001

+V1.8DX_3.3DX_I2S1 — +V5DX_AUDIO

I2C0_SCL_AUDIO_CODEC — I2C0_SDA_AUDIO_CODEC
CODEC_IRQ_HDR_R — BUF_PLT_RST_1V8_AUDIO_HDR_N
I2S1_SFRM_RXD_HDA_SDI_1_HDR_JB — SPKR_PD_N_HDR_R
I2S1_TXD_HDR — I2S1_MCLK_HDR
I2S_MCLK_IN_HDR

JC

J3H4 HDR_KOZ HDR_2X3A — E54876-001

+V1.8DX_3.3DX_I2S2

I2S2_SCLK_DMIC_CLK_A0_HDR — I2S2_SFRM_DMIC_DATA0_HDR
I2S2_RXD_DMIC_DATA1_HDR — I2S2_TXD_DMIC_CLK_A1_HDR

CAD NOTE: J3H2 TO J3H4 KOZ TO BE CLEARED. NEED 157MILS GAP BETWEEN ADJACENT 2 HDR'S

CAD NOTE: TRI PAD

+V1.8DX_3.3DX_DMIC — G22178-002 — R2G28 0 CHIP 5% 1/10W 0603 — +V1.8DX_3.3DX_DMIC_SDW

R2G29 0 5% 1/10W EMPTY 0603 — G22178-002 — +V1.8DX_AUDIO_SDW

DESIGN NOTE: SDW IS 1.8V ONLY

JD

J2H2 CON HDR_2X4 — G45658-001

SNDW3_CLK_DMIC_CLK_0_HDR — SNDW3_DATA_DMIC_DATA_0_HDR — +V5DX_AUDIO_SDW
SDW2_DMIC_CLK_A1_CODEC_DMIC_CLK — SDW2_DMIC_DATA1_CODEC_DMIC_DATA

CAD NOTE: PLACE JD AT <20 CM FROM PCH TO SUPPORT SMALL SYSTEM SNDW TOPOLOGY

JE

J2H4 CON HDR_2X5 — E46690-001

+V1.8DX_AUDIO_SDW

SNDW0_CLK_MASTER_RGMII_AUXTS_HDR — SNDW0_DATA_MASTER_RGMII_INT_HDR
SNDW1_CLK_HDR_1_RGMII_RESET — SNDW1_DATA_HDR_1_RGMII_PPS
SNDW1_CLK_HDR_2 — +VBATA_5DX_AUDIO_SDW — SNDW1_DATA_HDR_2

CAD NOTE: TRI PAD

G22178-002 R2H11 0 CHIP 5% 0603 — +VBATA_SDW
1/10W — +V5DX_AUDIO_SDW
R2H12 0 5% 1/10W EMPTY 0603 — G22178-002

[PAGE_TITLE=AUDIO - AUDIO HEADER -1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.163
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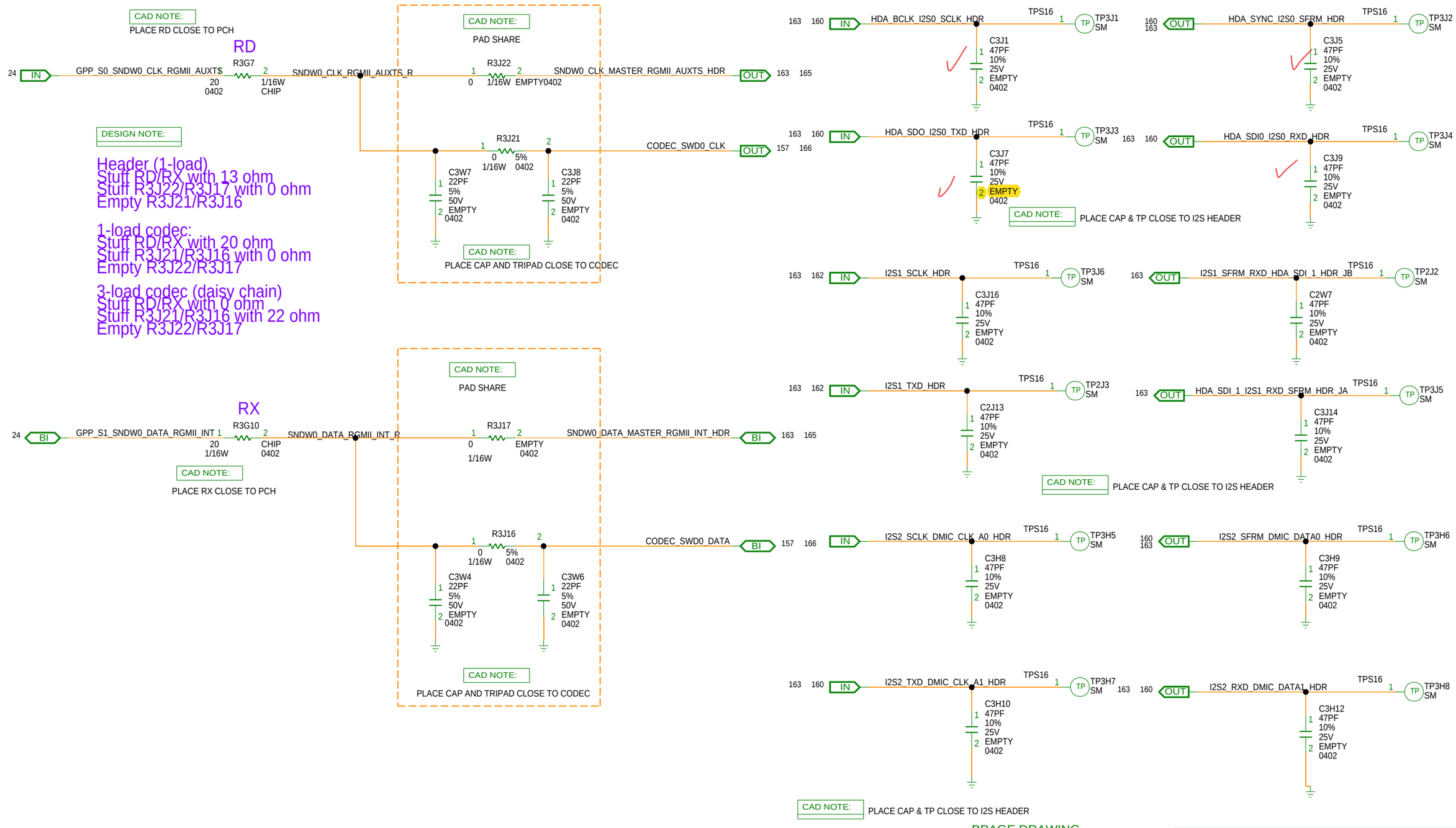
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	163	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

SNDW0 TOPOLOGY



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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.164
Wed Dec 18 18:08:00 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	164	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE: PLACE TP AND LOADING CAPS ON SNDW CLOSE TO CONN

DESIGN NOTE: TP ADDED NEAR SRC AND LOAD SIDES FOR EV

DESIGN NOTE: TP ADDED NEAR SRC AND LOAD SIDES FOR EV

164 163 IN SNDW0_CLK_MASTER_RGMII_AUXTS_HDR — TPS16 1 — TP TP2H7 SM
C2H9 47PF 10% 25V EMPTY 0402

164 163 BI SNDW0_DATA_MASTER_RGMII_INT_HDR — TPS16 1 — TP TP2H6 SM
C2H8 47PF 10% 25V EMPTY 0402

163 161 IN SNDW1_CLK_HDR_1_RGMII_RESET — TPS16 1 — TP TP1H1 SM
C1H3 47PF 10% 25V EMPTY 0402

163 161 BI SNDW1_DATA_HDR_1_RGMII_PPS — TPS16 1 — TP SM TP2H5
C2H7 47PF 10% 25V EMPTY 0402

165 161 IN SDW2_CLK_DMIC_CLK_A1_HDR — TPS16 1 — TP TP2H4 SM
C2H3 47PF 10% 25V EMPTY 0402

165 161 BI SDW2_DATA_DMIC_DATA1_HDR — TPS16 1 — TP SM TP2H1
C2H1 47PF 10% 25V EMPTY 0402

163 162 IN SNDW3_CLK_DMIC_CLK_0_HDR — TPS16 1 — TP SM TP2H3
C2H4 47PF 10% 25V EMPTY 0402

163 162 BI SNDW3_DATA_DMIC_DATA_0_HDR — TPS16 1 — TP TP2H2 SM
C2H2 47PF 10% 25V EMPTY 0402 H87099-001

+V5DX_AUDIO — +V5DX_AUDIO_FIL
G66290-002 FB3H1 600OHM 300MA 25% CHIP
602433-098 C3H13 10UF 20% 16V X5R 0603
CR3H1 DIO T5V0S5-7 1MA G95181-001
AUDIO_AGND

CAD NOTE: PLACE R & C CLOSE TO CODEC

CAD NOTE: PAD SHARE ALL RES BELOW

166 IN CODEC_DMIC_CLK — R3J12 22 1/16W 5% 0402 — C3J6 10PF 0.5PF 50V C0G 0402 — CODEC_DMIC_CLK_R1 — R2H6 0 1/16W EMPTY 0402 — SDW2_DMIC_CLK_A1_CODEC_DMIC_CLK OUT 163

165 161 IN SDW2_CLK_DMIC_CLK_A1_HDR — R2H5 0 1/16W CHIP 0402

R3H18 22 1/16W 5% 0402 — C3H14 10PF 0.5PF 50V C0G 0402 — CODEC_DMIC_CLK_R2 OUT 162

166 OUT CODEC_DMIC_DATA — R3W19 0 1/16W 5% 0402 — CODEC_DMIC_DATA_R — R2G31 0 1/16W EMPTY 0402 — SDW2_DMIC_DATA1_CODEC_DMIC_DATA BI 163

165 161 BI SDW2_DATA_DMIC_DATA1_HDR — R2G30 0 1/16W CHIP 0402

SNDW2 Header
Empty R2H6/R2G31
Stuff R2H5/R2G30 with 0 ohm

DMIC1:
Empty R2H6/R2G31
Stuff R2H5 with 33 ohm
Stuff R2G30 with 0 ohm

+V1.8DX_CORE_CODEC — +V1.8DX_CORE_CODEC_FIL
693286-055 FB2J1 600OHM 1A 25% CHIP
C1H5 10UF 16V X5R 0603

[PAGE_TITLE=AUDIO - AUDIO CODEC MISC]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.165
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	165	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:

STUFF R2J9, UNSTUFF R2J11 FOR ES1
UNSTUFF R2J9, STUFF R2J11 FOR ES2

DESIGN NOTE:
STUFF C3J11 FOR ES2

CAD NOTE:
PLACE CLOSE TO PIN38

GENERIC LPDB
EU3J2
IC

ALC711-VB1-CG

K42023-001

CAD NOTE:
PLACE AT THE BOTTOM OF CODEC

DESIGN NOTE:
STUFF C2J16 FOR ES2

DESIGN NOTE:
STUFF CC FOR ES2

DESIGN NOTE:
STUFF CA, RD UNSTUFF RB FOR ES2

MODE CONTROL FOR CODEC

DESIGN NOTE:
STUFF PD AND UNSTUFF PU FOR SWD MODE

ES2 STRAPS

DESIGN NOTE:
STUFF RA FOR ES2 TO ENABLE VAD

CAD NOTE:
PLACE NEAR CONN, ISOLATED FROM HIGH SPEED AND POWER TRACES

DESIGN NOTE:
ES2
STUFF R2, R4, R6, R8 FOR ES2
UNSTUFF R1, R3, R5, R7, R9 & R10 FOR ES2

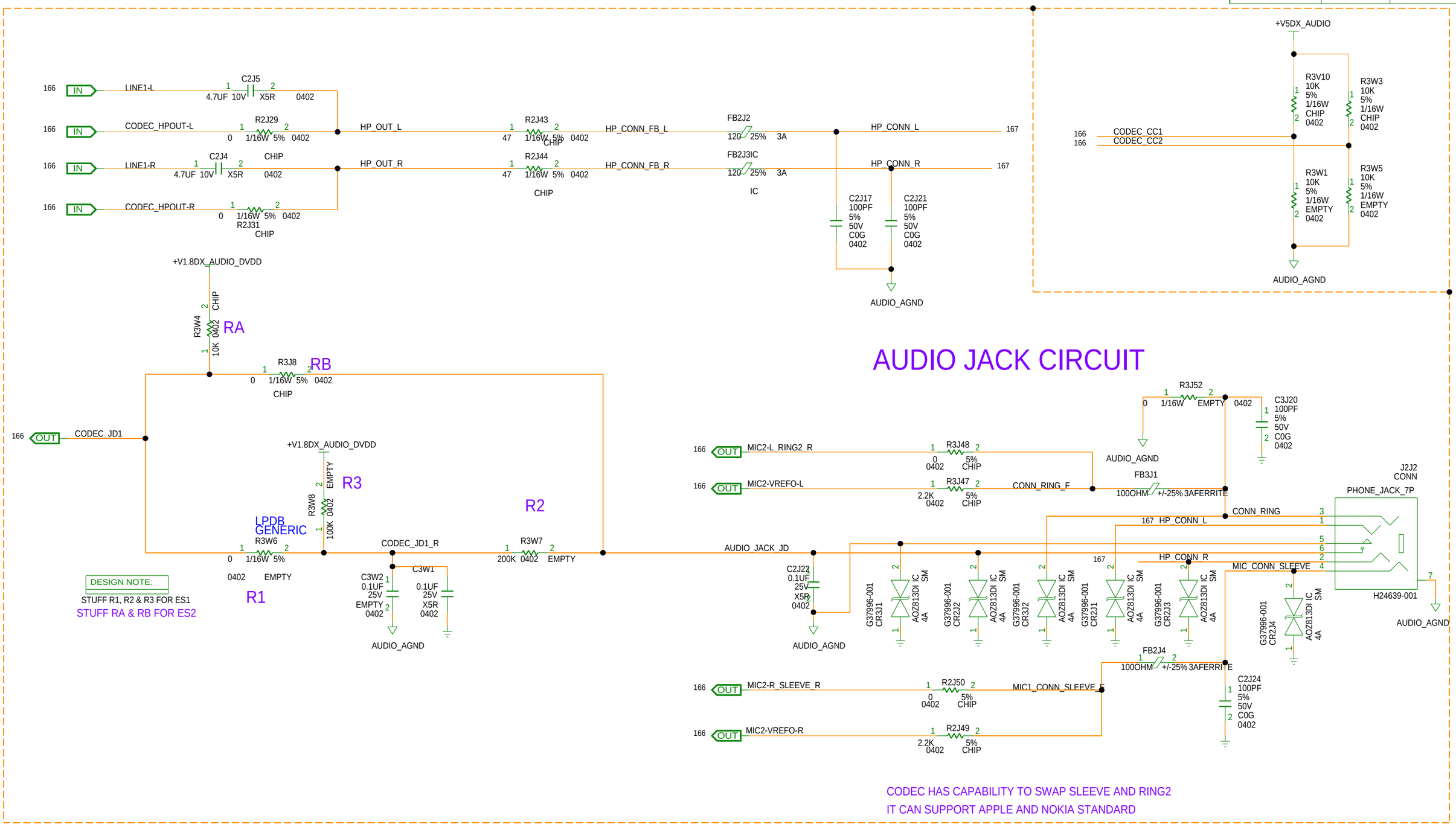
[PAGE_TITLE=AUDIO - AUDIO CODEC ALC711]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.166
Wed Dec 18 18:08:02 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	166	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=AUDIO - JACK CIRCUIT]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.167
Wed Dec 18 18:08:03 2019

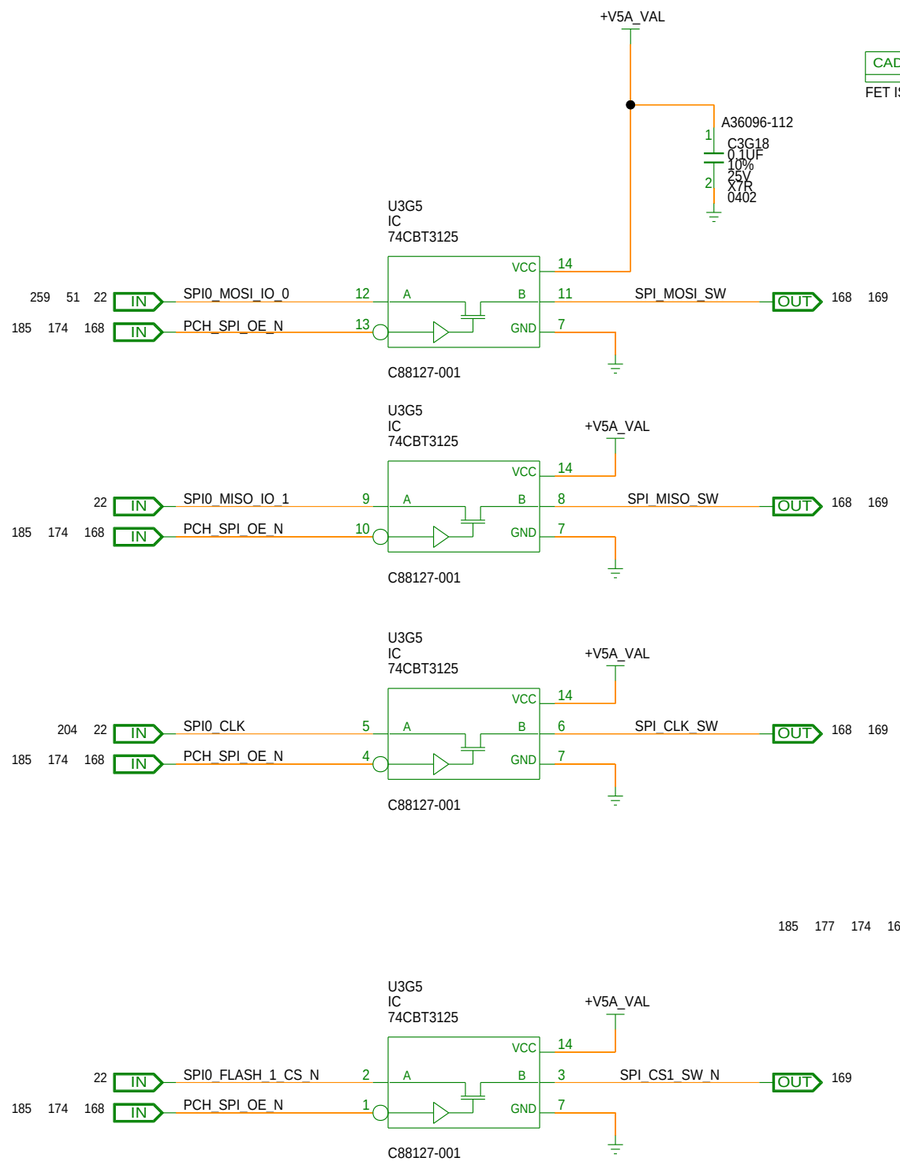
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	167	1.0

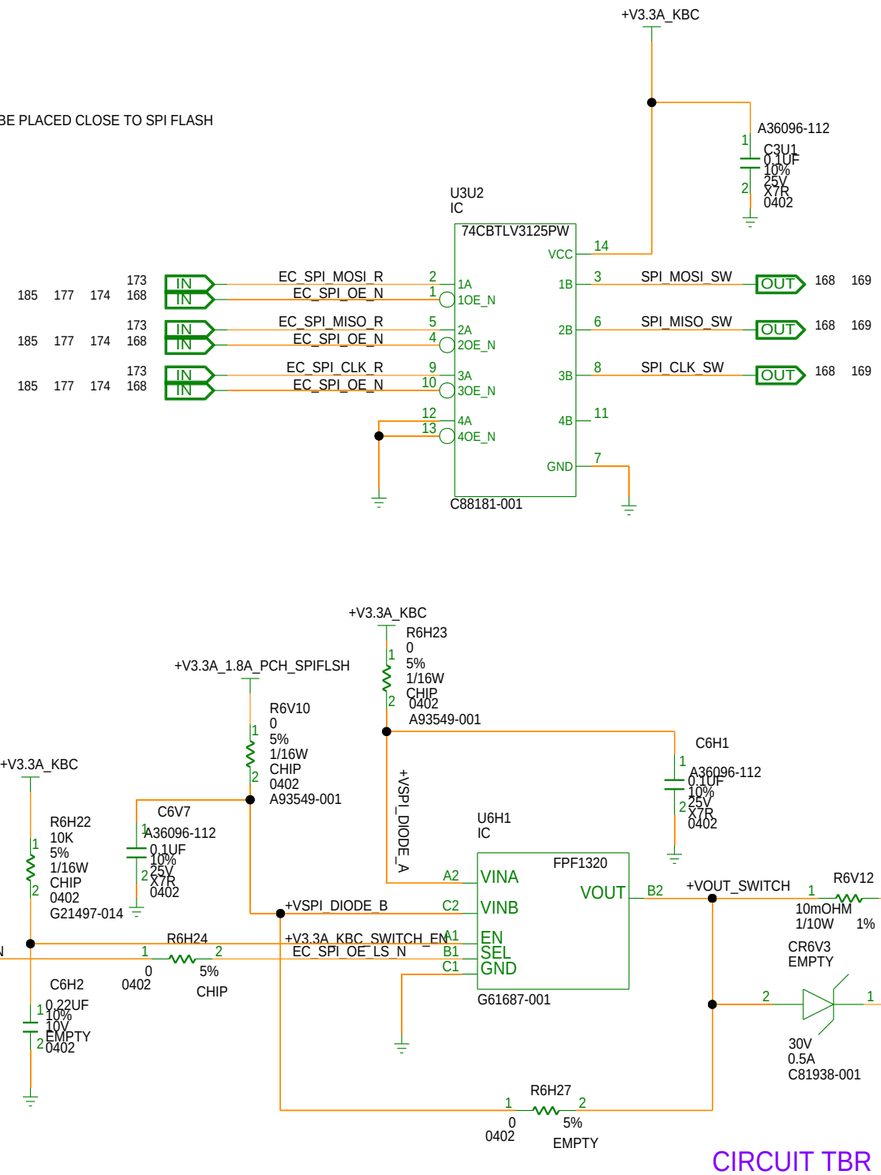
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

FET SWITCH FOR ISOLATION

CAD NOTE:
FET ISOLATION SWITCH SHOULD BE PLACED CLOSE TO SPI FLASH





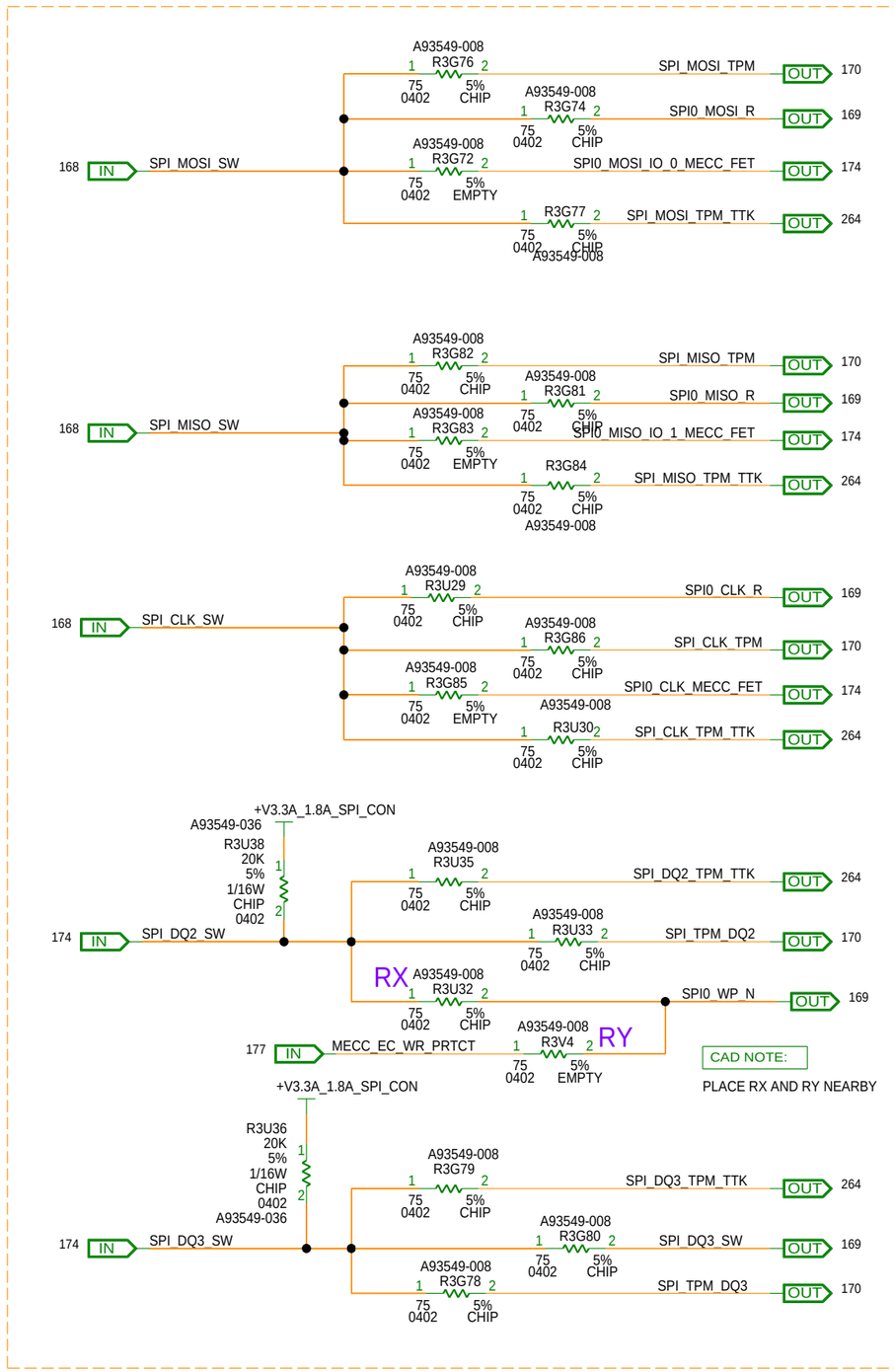
CIRCUIT TBR

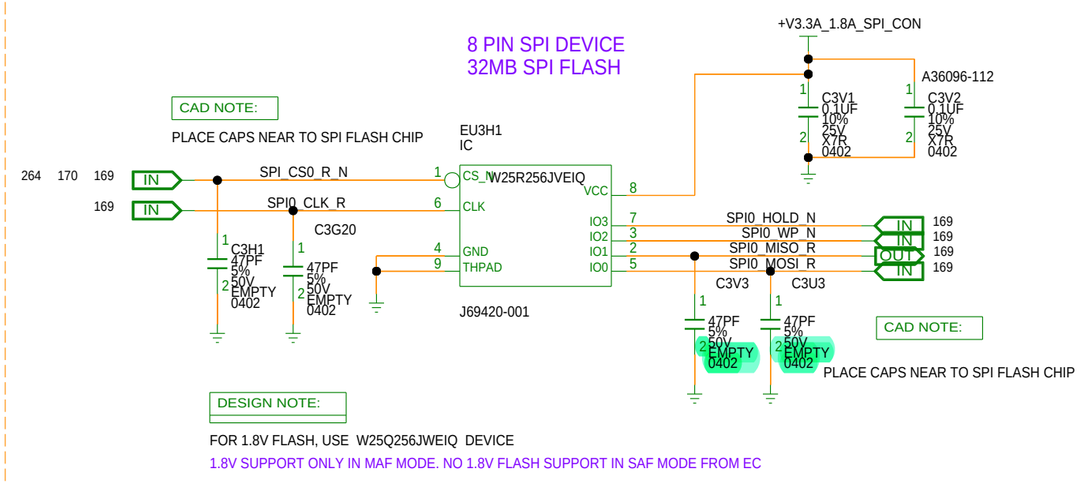
[PAGE_TITLE=SPI - FLASH MUX CIRCUIT]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.168
Wed Dec 18 18:08:04 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	168	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE





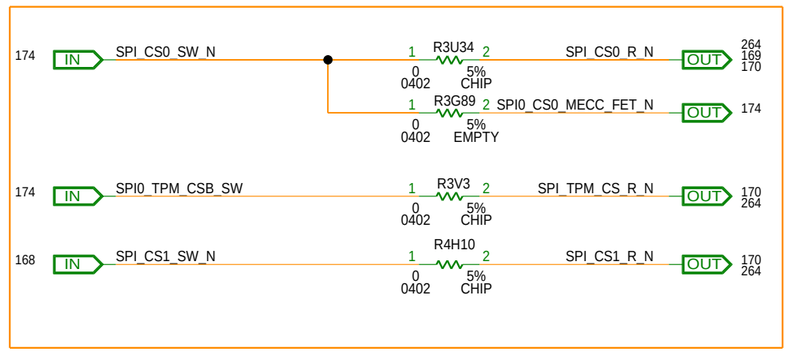
CAD NOTE:

KEEP COMMON FOOTPRINT FOR 1.8V AND 3.3V FLASH

CAD NOTE:

KEEP KOZ AS PER 8PIN SPI SOCKET

NOTE : THE PRESENT SPI TOPOLOGY RESISTOR VALUES ARE SPECIFIC TO CRB ONLY. CUSTOMERS HAVE TO REFER TO THE PDG FOR THE SPI REQUIREMENTS.



[PAGE_TITLE=SPI - FLASH]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.169
Wed Dec 18 18:08:05 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	169	1.0

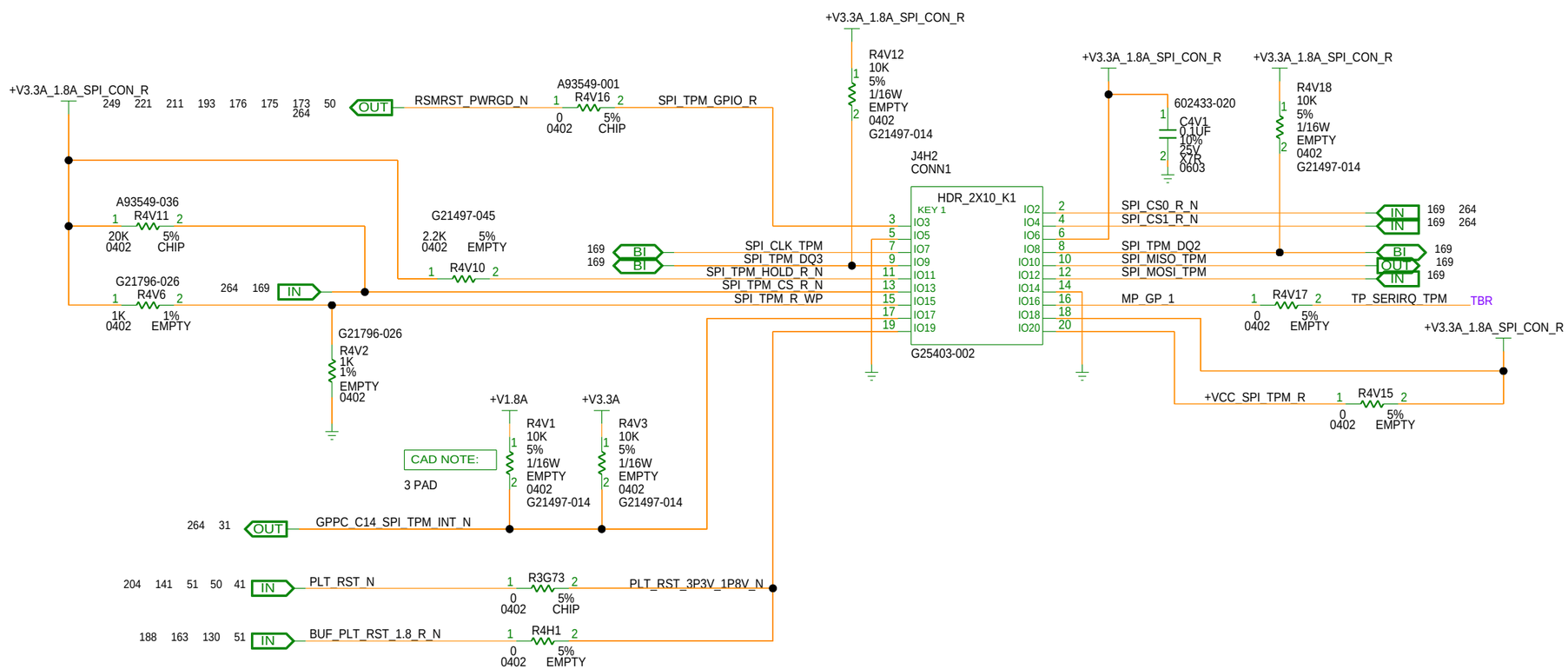
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

SF600 BASED SPI BASED TPM HEADER

CAD NOTE:

SPI0_FLASH_1_CS_N SIGNAL TO BE ROUTED 1.5 INCH MORE LENGTH THAN OTHER SPI0 SIGNALS



[PAGE_TITLE=SPI - PROGRAMING SF600/TPM HEADER]

BPAGE DRAWING
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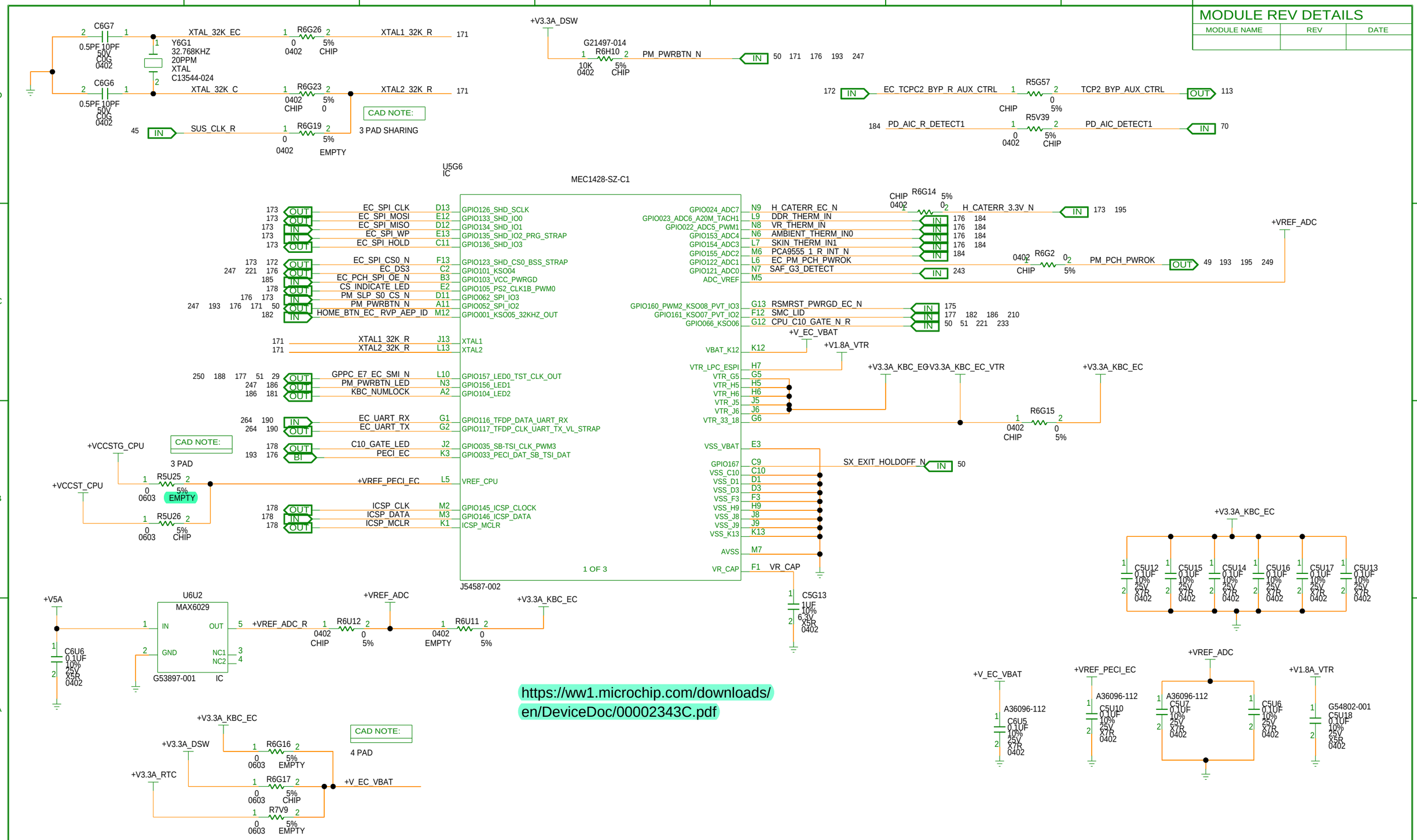
Wed Dec 18 18:08:06 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	170	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



https://ww1.microchip.com/downloads/en/DeviceDoc/00002343C.pdf

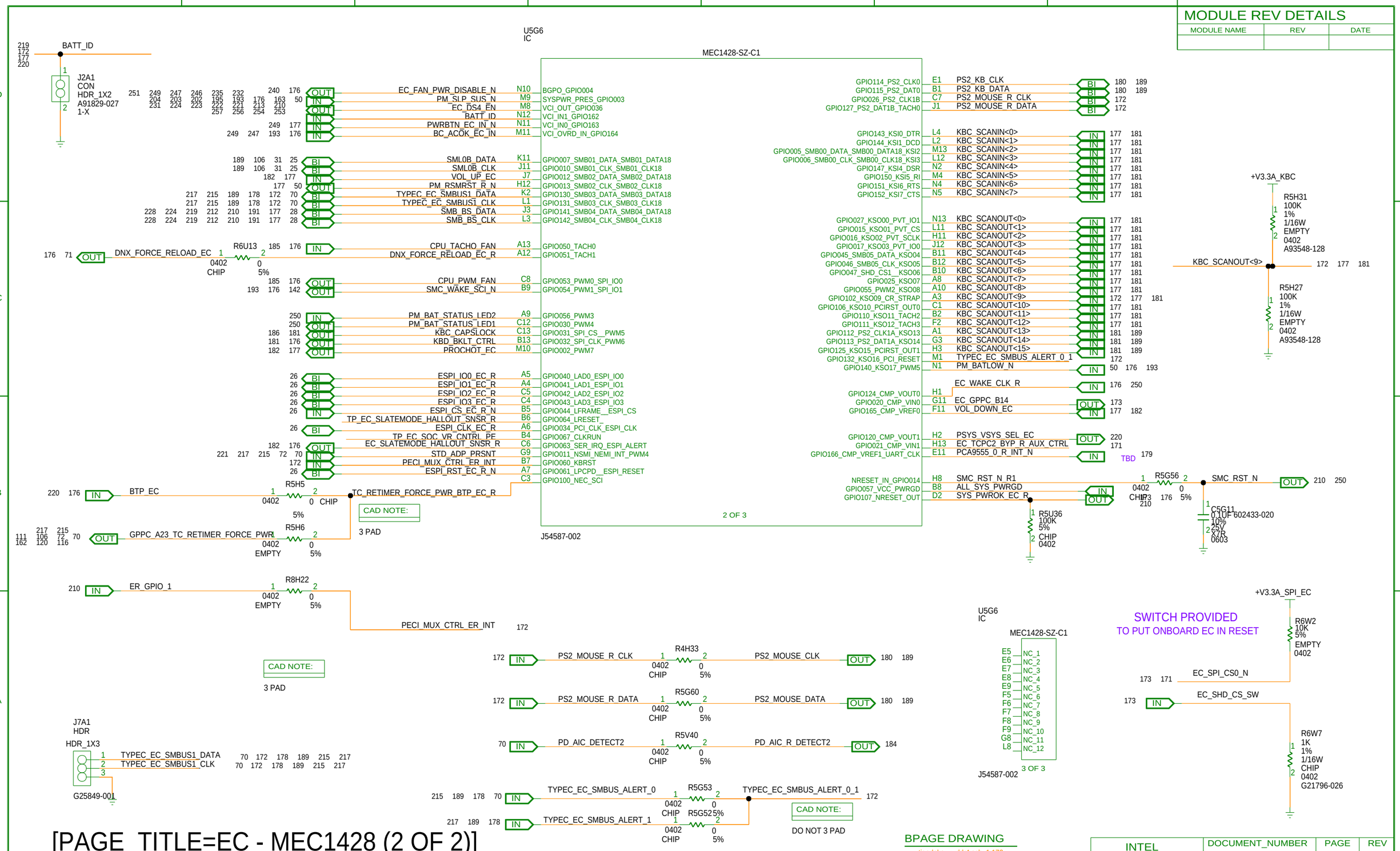
[PAGE_TITLE=EC - MEC1428 (1 OF 2)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.171
Wed Dec 18 18:08:07 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	171	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=EC - MEC1428 (2 OF 2)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.172
Wed Dec 18 18:08:09 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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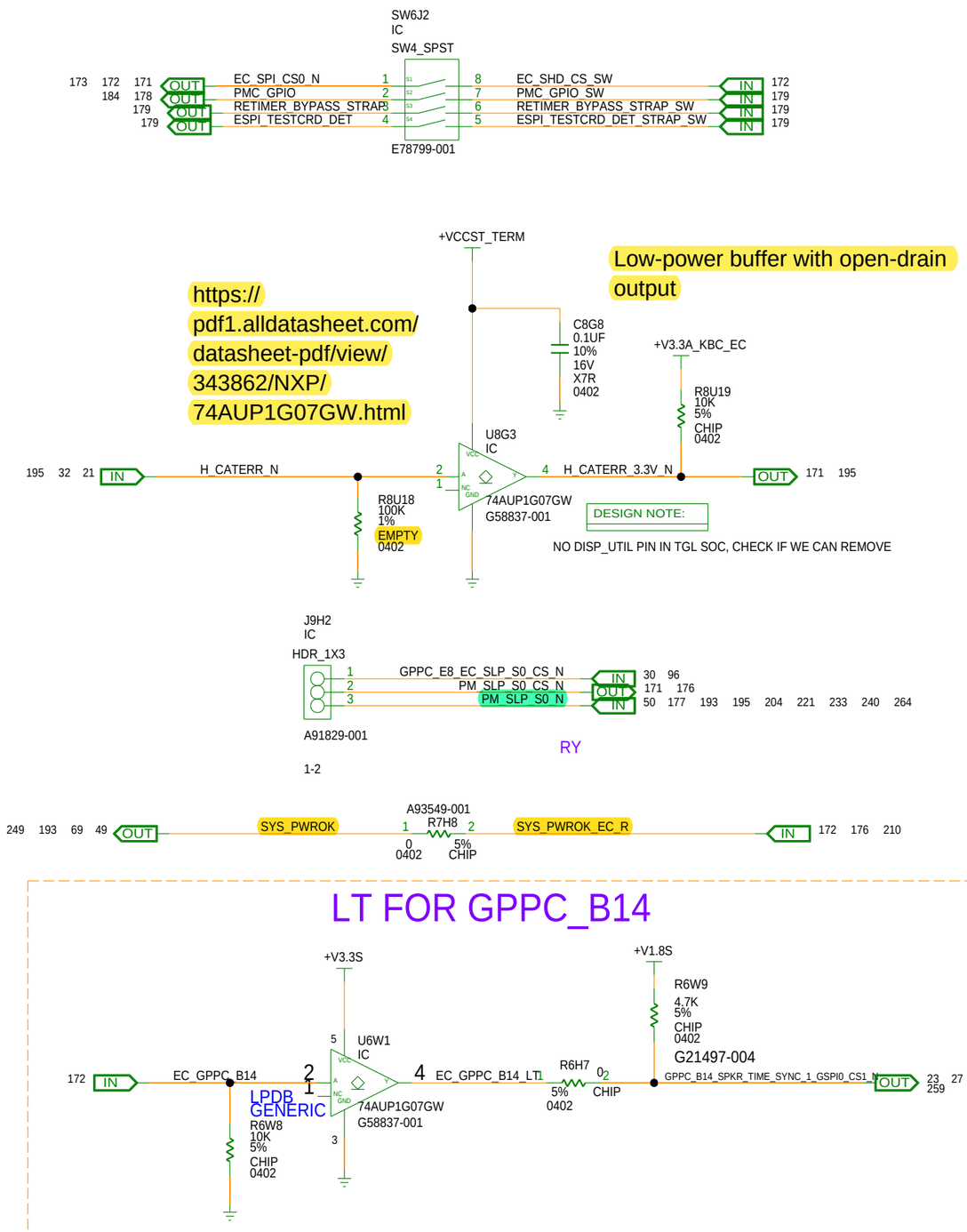
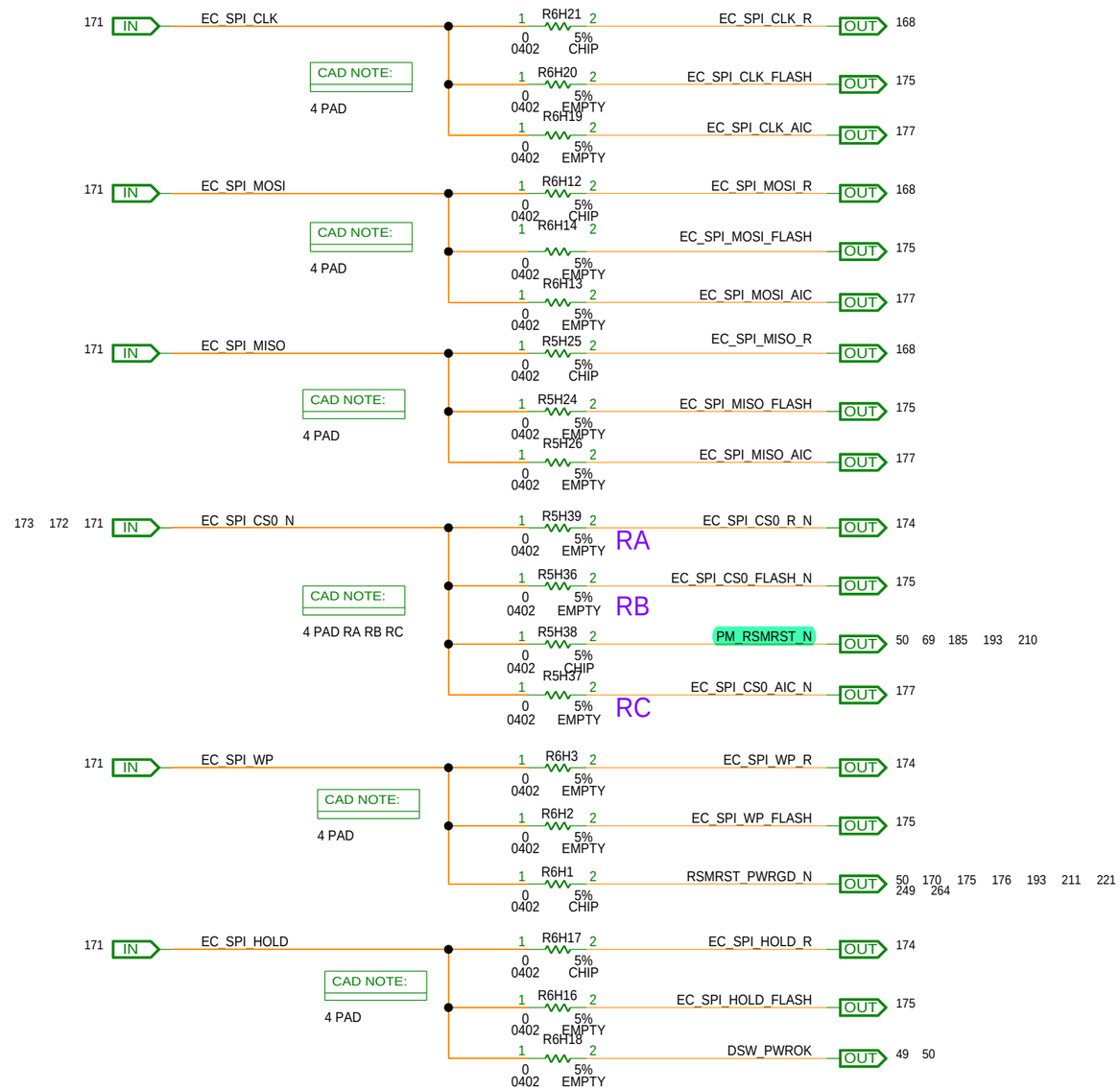
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE





[PAGE_TITLE=EC - GPIO SHARING OPTIONS]

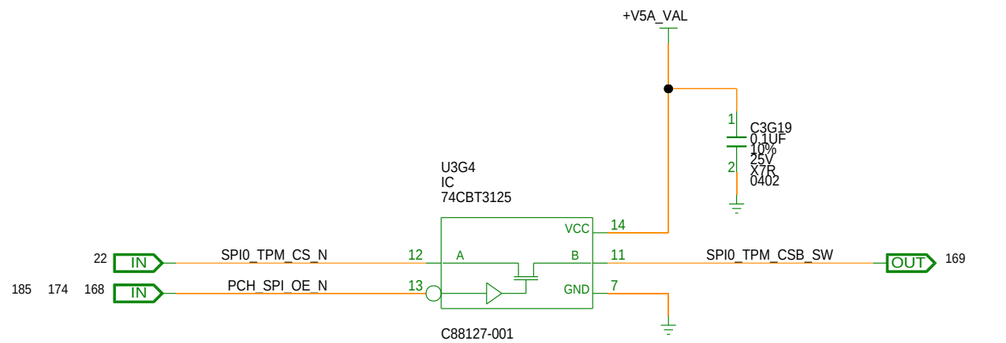
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.173
Wed Dec 18 18:08:10 2019

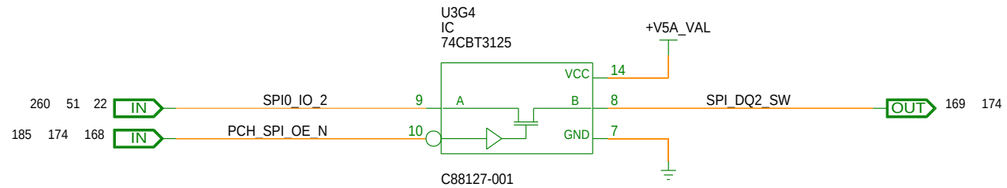
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	173	1.0

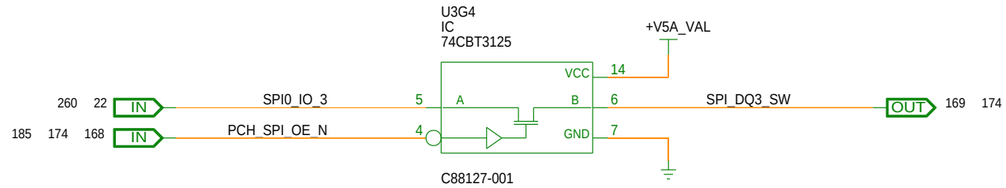
CUSTOM TEXT BPAGE

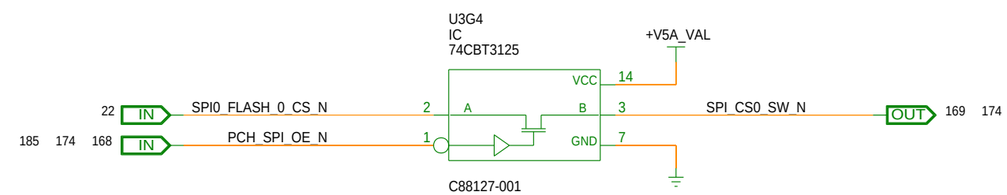
FET SWITCH FOR ISOLATION

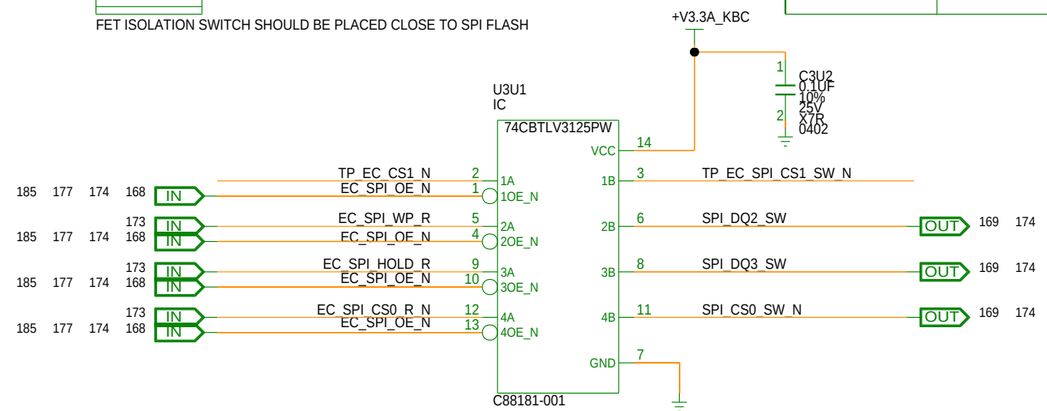
CAD NOTE:
FET ISOLATION SWITCH SHOULD BE PLACED CLOSE TO SPI FLASH

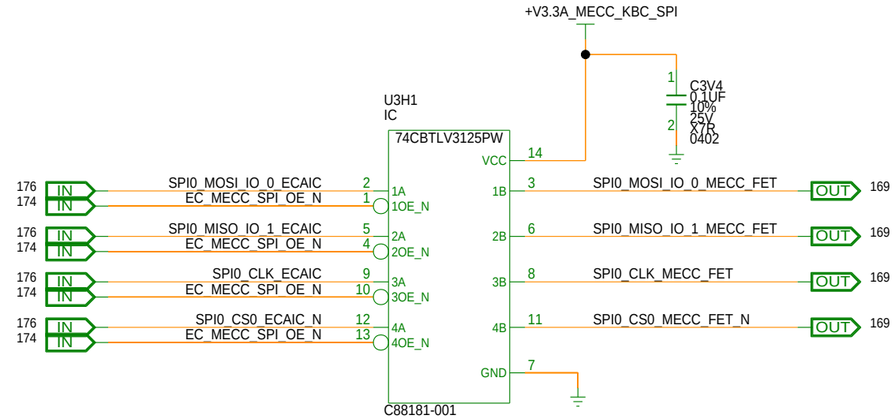


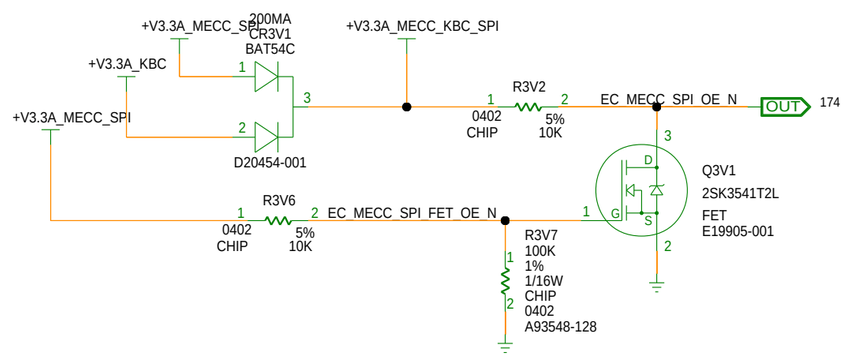












MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=EC - SPI FLASH SHARING & FLASH]

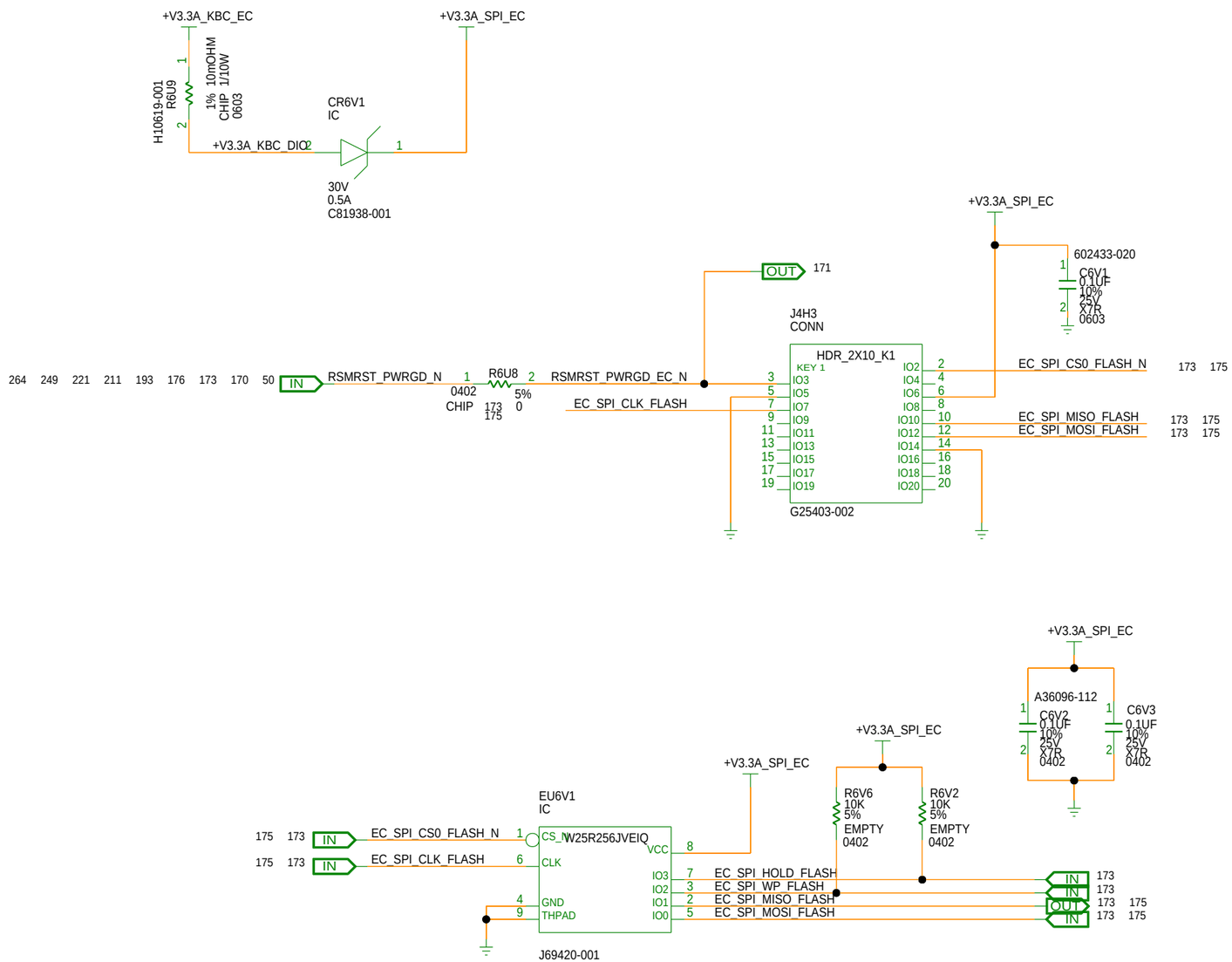
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.174
Wed Dec 18 18:08:10 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	174	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

SF600 BASED TPM HEADER (DEDICATED FOR EC)



[PAGE_TITLE=EC - SPI FLASH SF600 PROGRAMER]

BPAGE DRAWING
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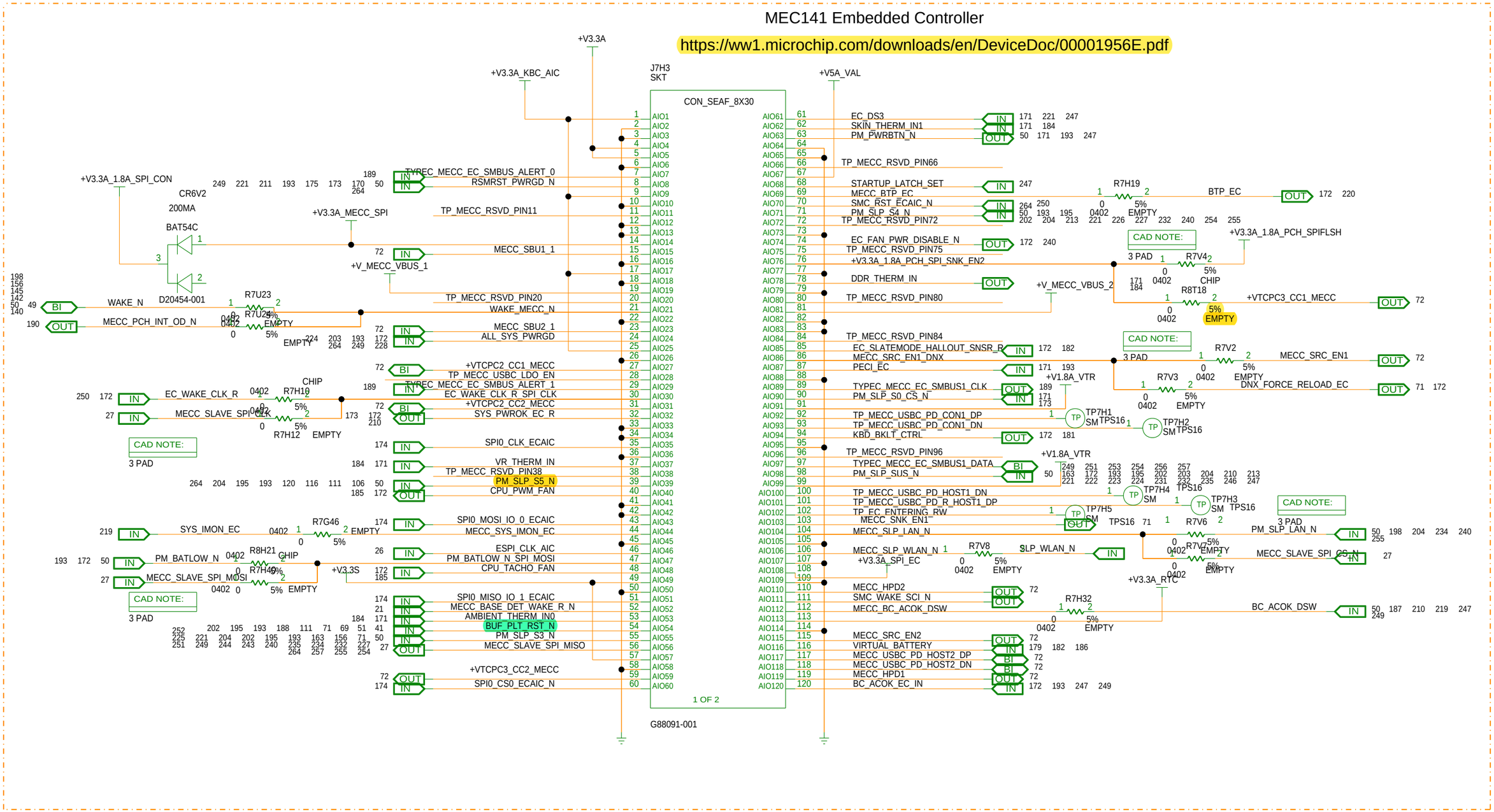
Wed Dec 18 18:08:11 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	175	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=EC - MECC AIC (1 OF 2)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.176
Wed Dec 18 18:08:12 2019

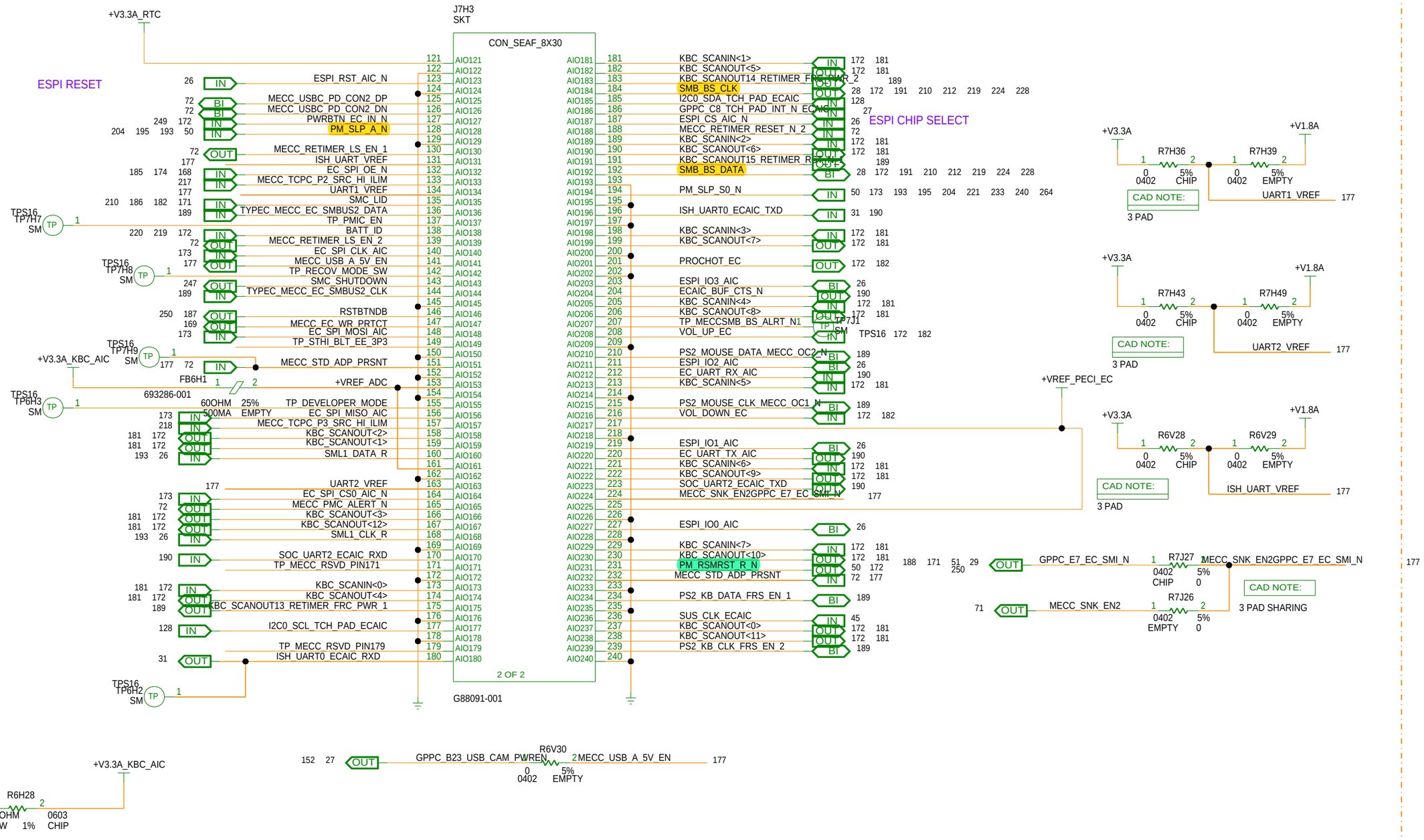
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	176	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

MEC140x/1x embedded controller

https://ww1.microchip.com/downloads/en/DeviceDoc/00001956E.pdf



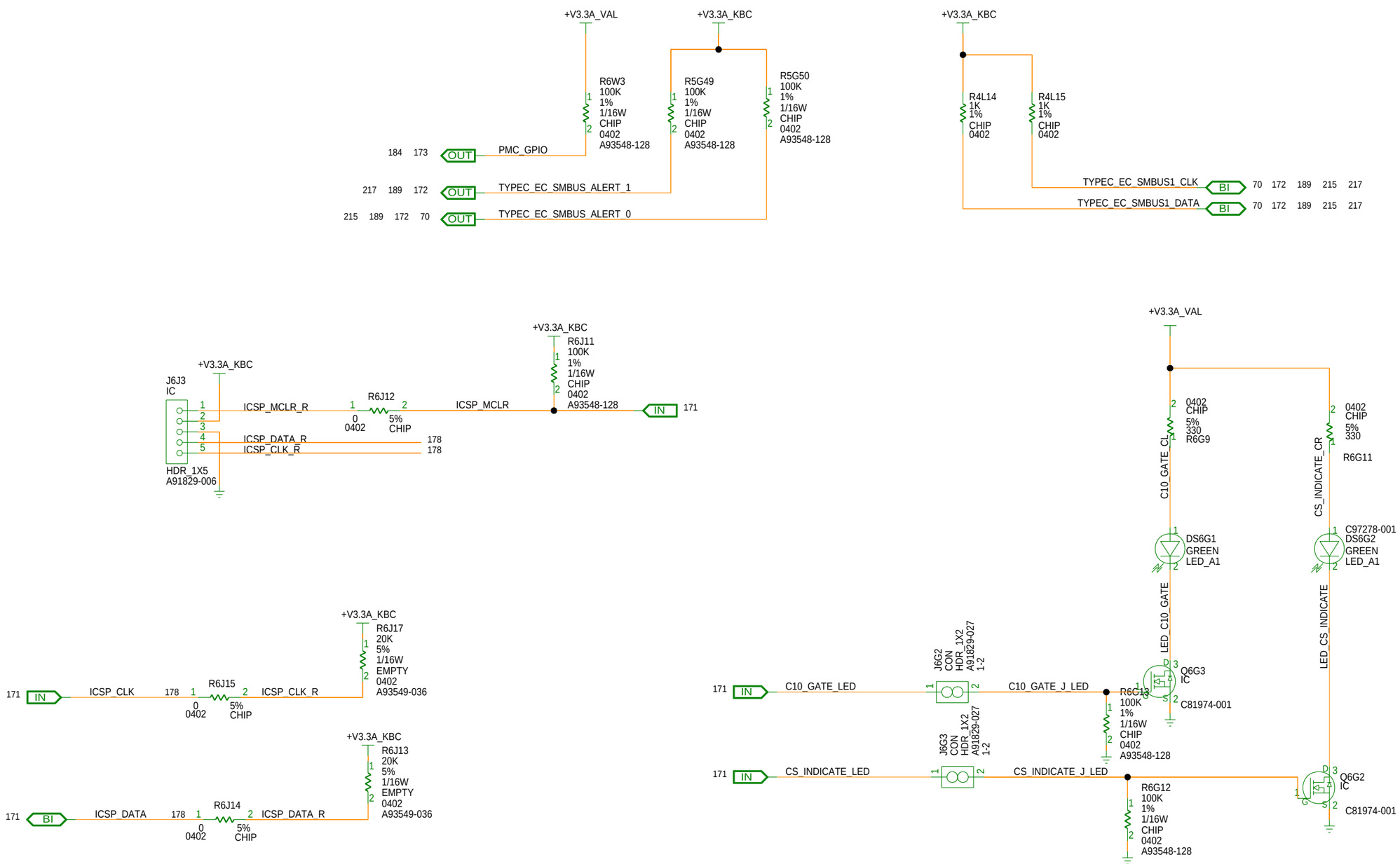
[PAGE_TITLE=EC - MECC AIC (2 OF 2)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.177
Wed Dec 18 18:08:13 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	177	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=EC - RESERVED -1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.178
Wed Dec 18 18:08:14 2019

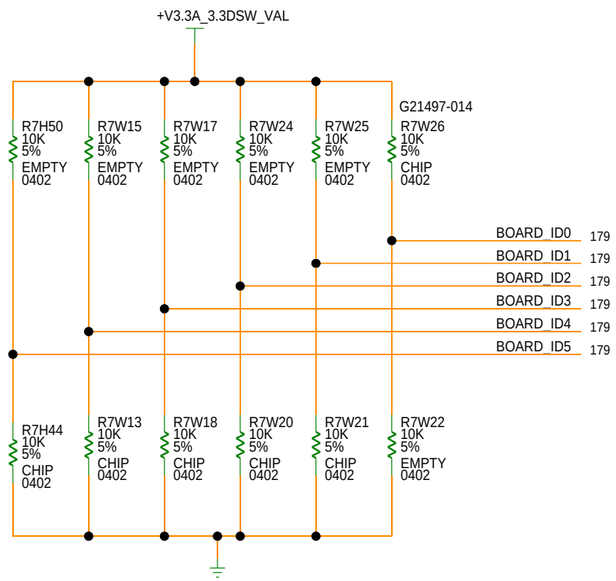
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	178	1.0

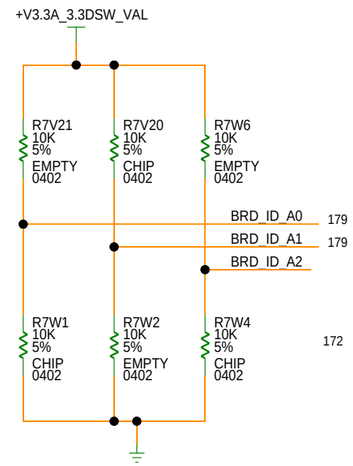
CUSTOM TEXT BPAGE

BOARD ID ,FAB ID & I/O EXPANDER

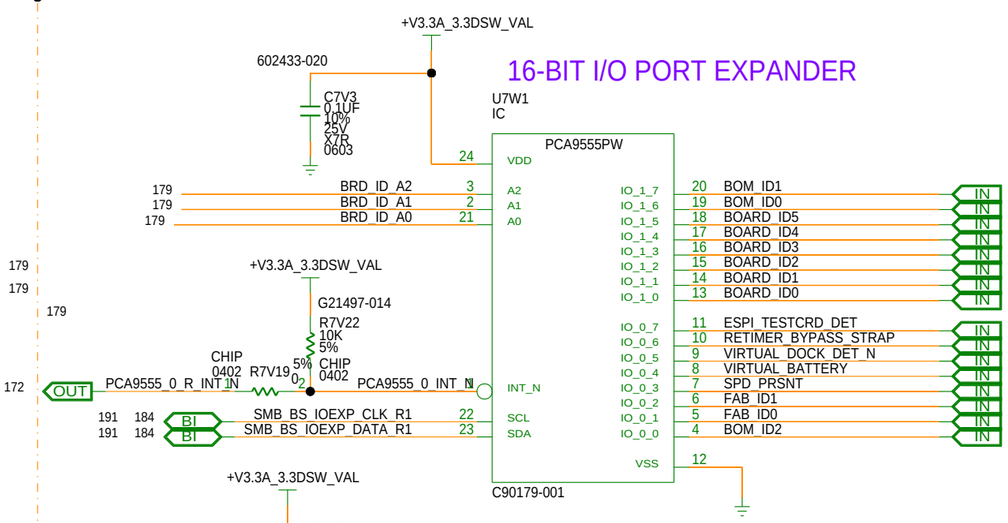
MODULE REV DETAILS		
MODULE NAME	REV	DATE

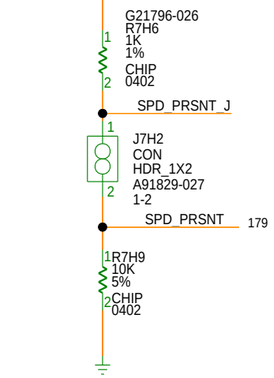
BOARD REVISION





16-BIT I/O PORT EXPANDER



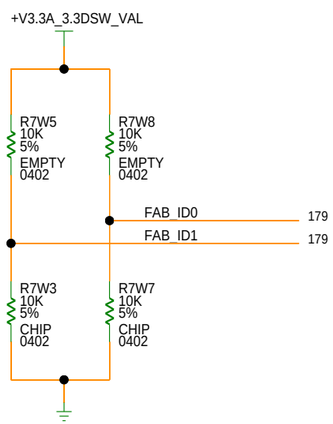


SLAVE ADDRESS

0	1	0	0	A2	A1	A0	R/W
FIXED				PROGRAMMABLE			

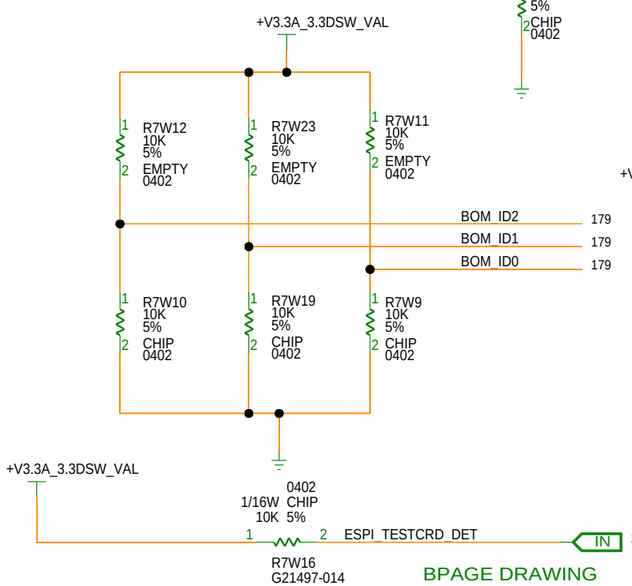
PCA9555 ADDRESS

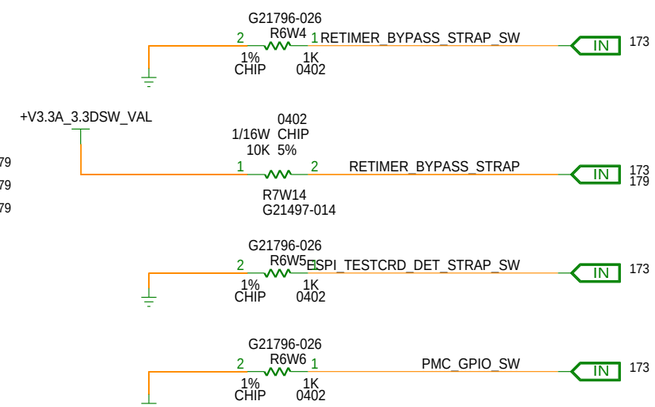
FAB REVISION



FAB ID TABLE

I/OS		FAB ID
0	0	1
0	1	2
1	0	3
1	1	4





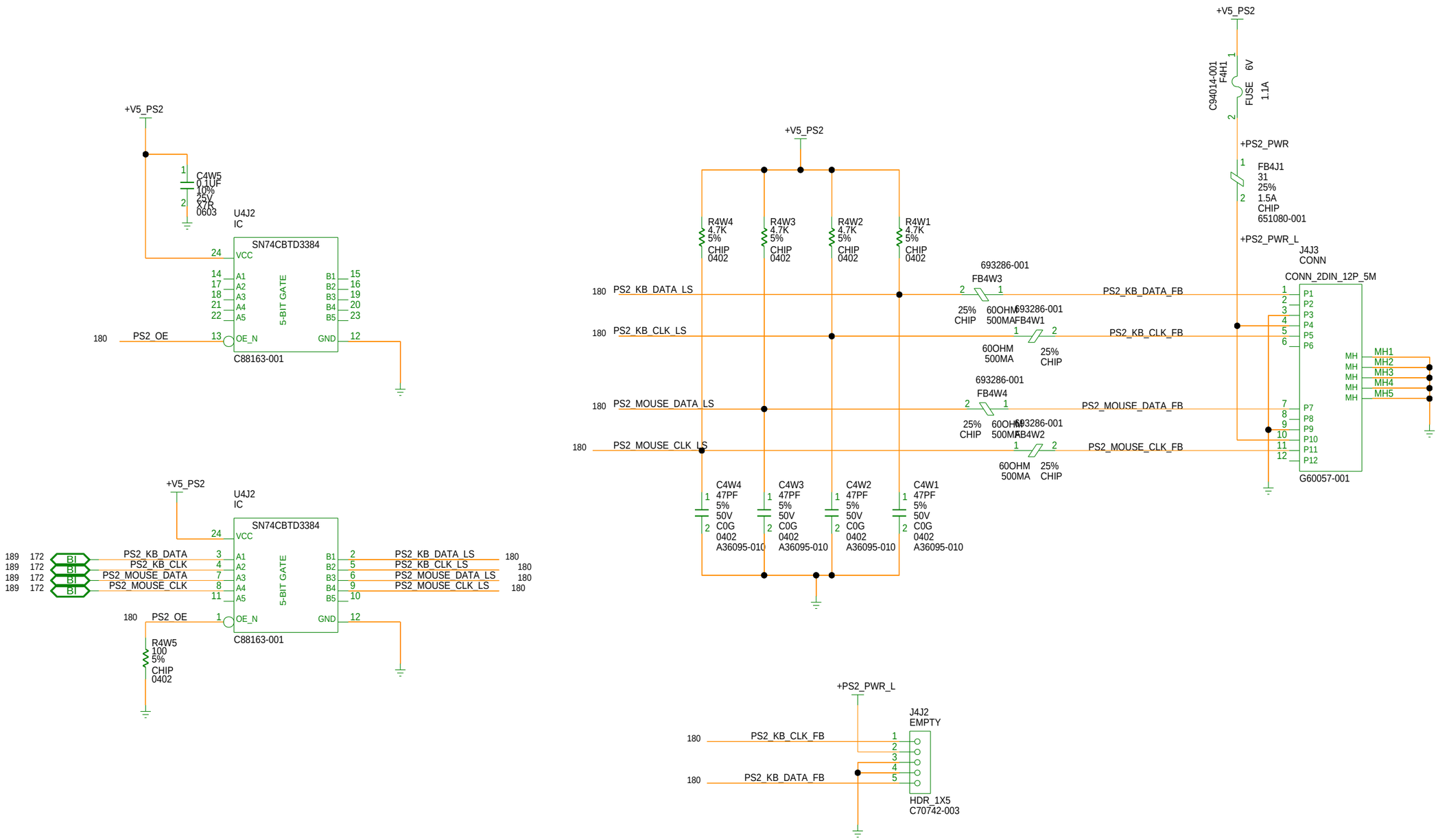
[PAGE_TITLE=EC - BOARD ID, FAB ID, IO EXPANDER]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.179
Wed Dec 18 18:08:15 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	179	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



FOR PPV ONLY. PS2 WILL BE UNSTUFFED FOR PPV SKU

[PAGE_TITLE=EC - PS2 KEYBOARD & MOUSE]

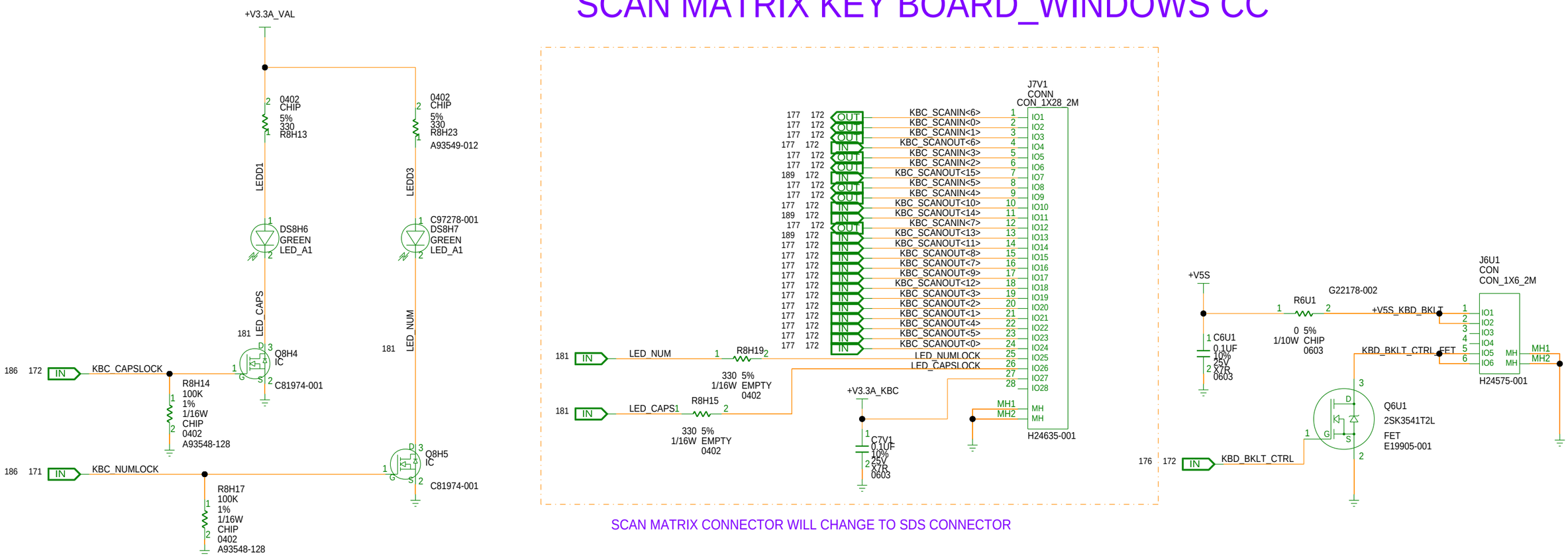
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.180
Wed Dec 18 18:08:16 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	180	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

SCAN MATRIX KEY BOARD_WINDOWS CC



SCAN MATRIX CONNECTOR WILL CHANGE TO SDS CONNECTOR

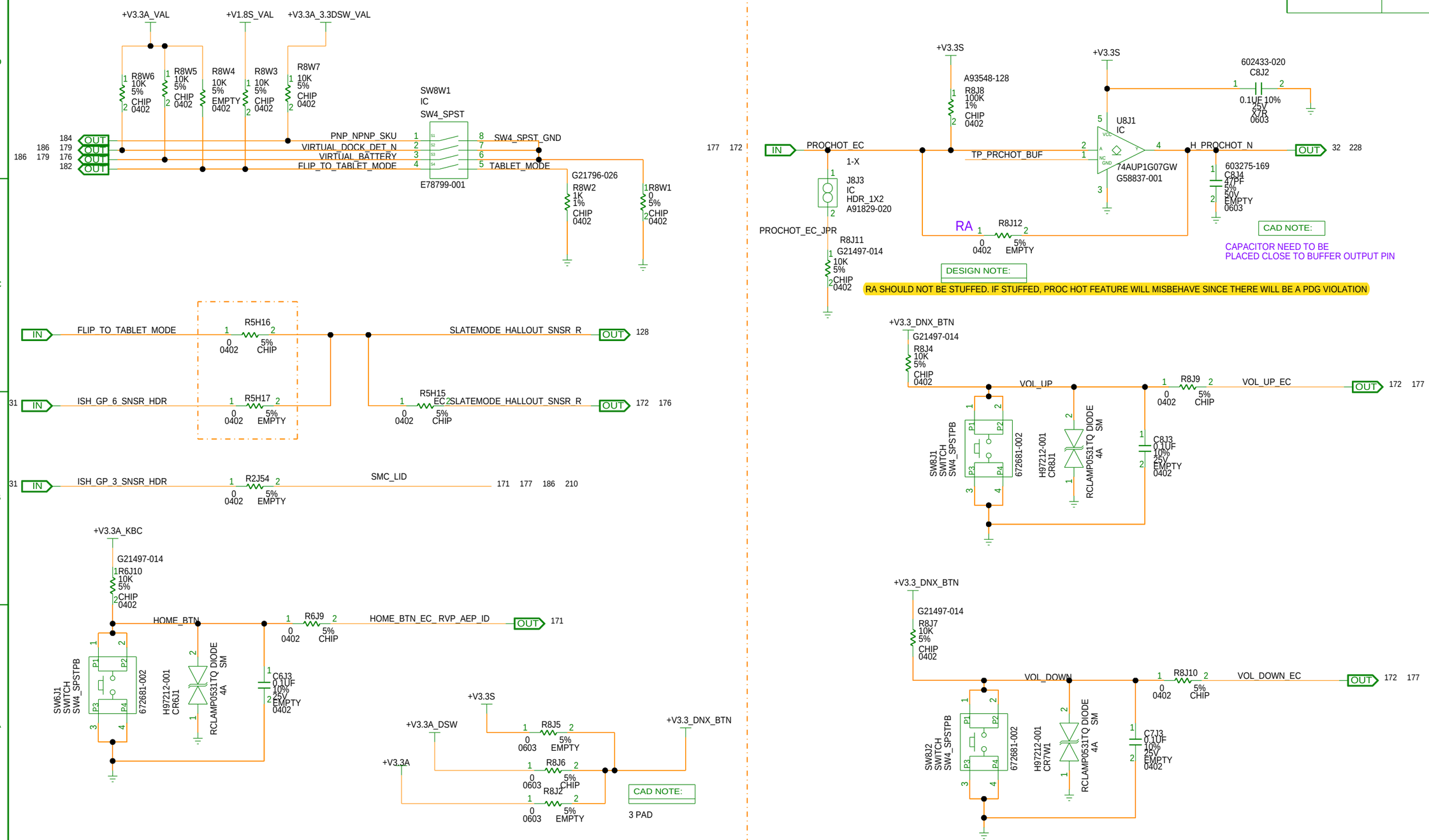
[PAGE_TITLE=EC - SCAN MATRIX KEY BOARD]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.181
Wed Dec 18 18:08:17 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	181	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



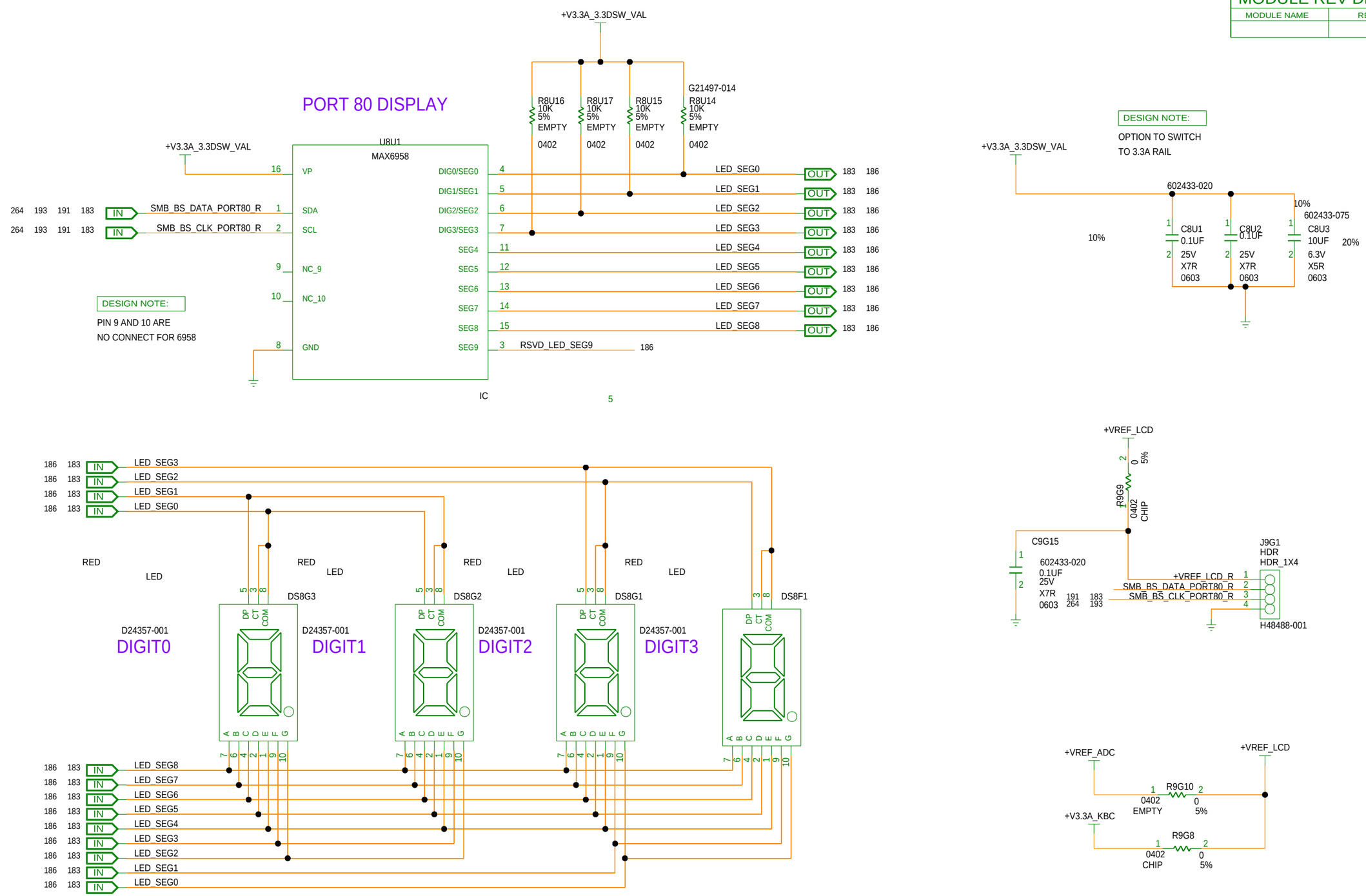
[PAGE_TITLE=EC - SWITCHES]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.182
Wed Dec 18 18:08:18 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	182	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



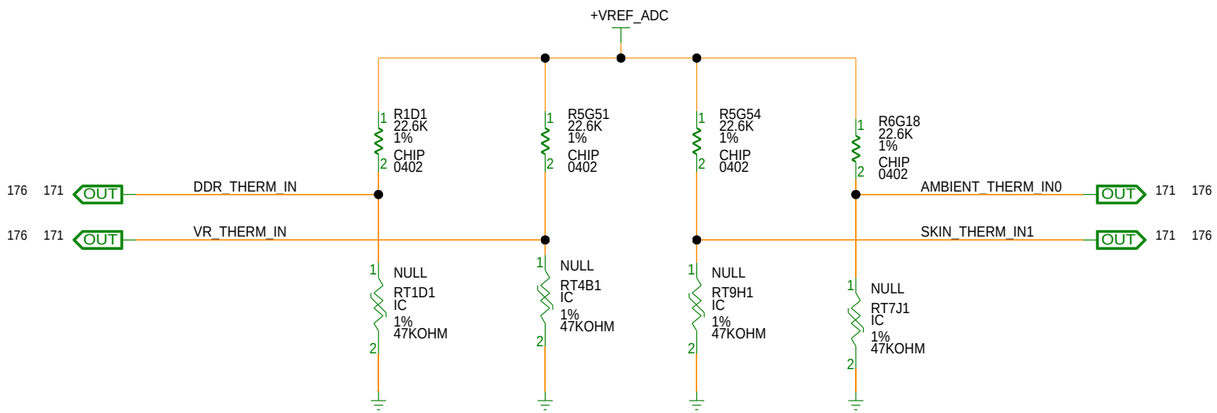
[PAGE_TITLE=EC - PORT 80 DISPLAY & HEADER]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.183
Wed Dec 18 18:08:19 2019

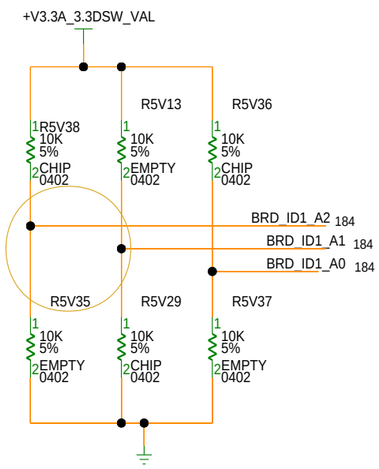
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	183	1.0

CUSTOM TEXT BPAGE

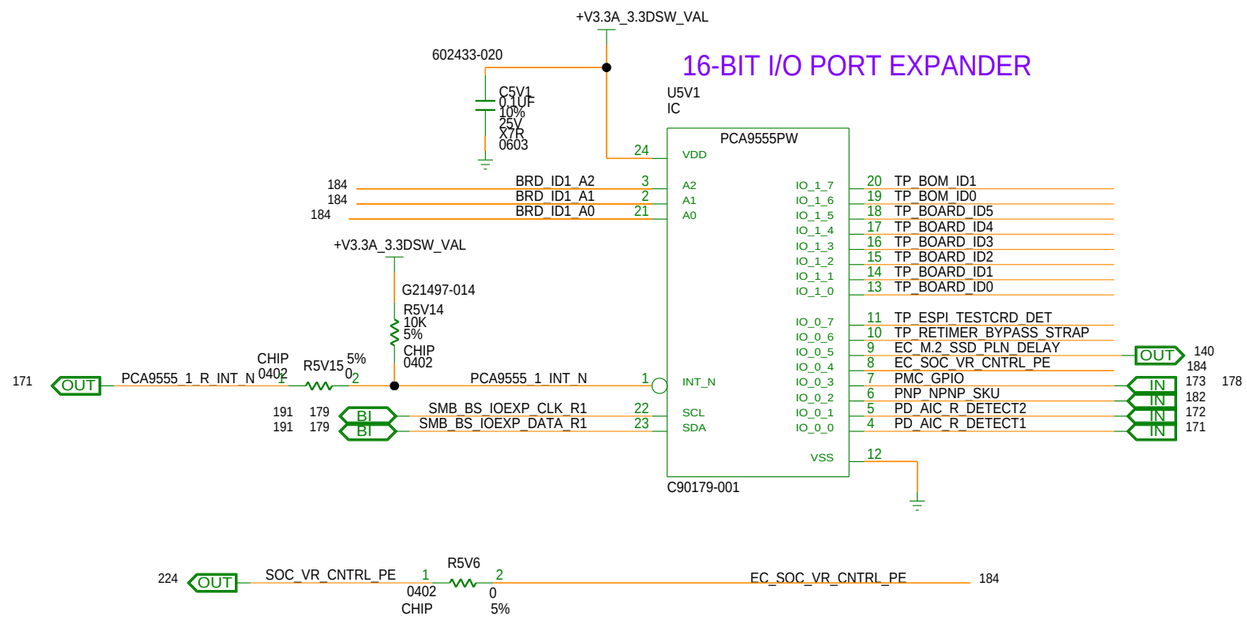
MODULE REV DETAILS		
MODULE NAME	REV	DATE



THIS HAS TO BE PLACED IN HOT SPOT



ADDRESS NEED TO BE CHANGED



[PAGE_TITLE=EC - THERMISTERS]

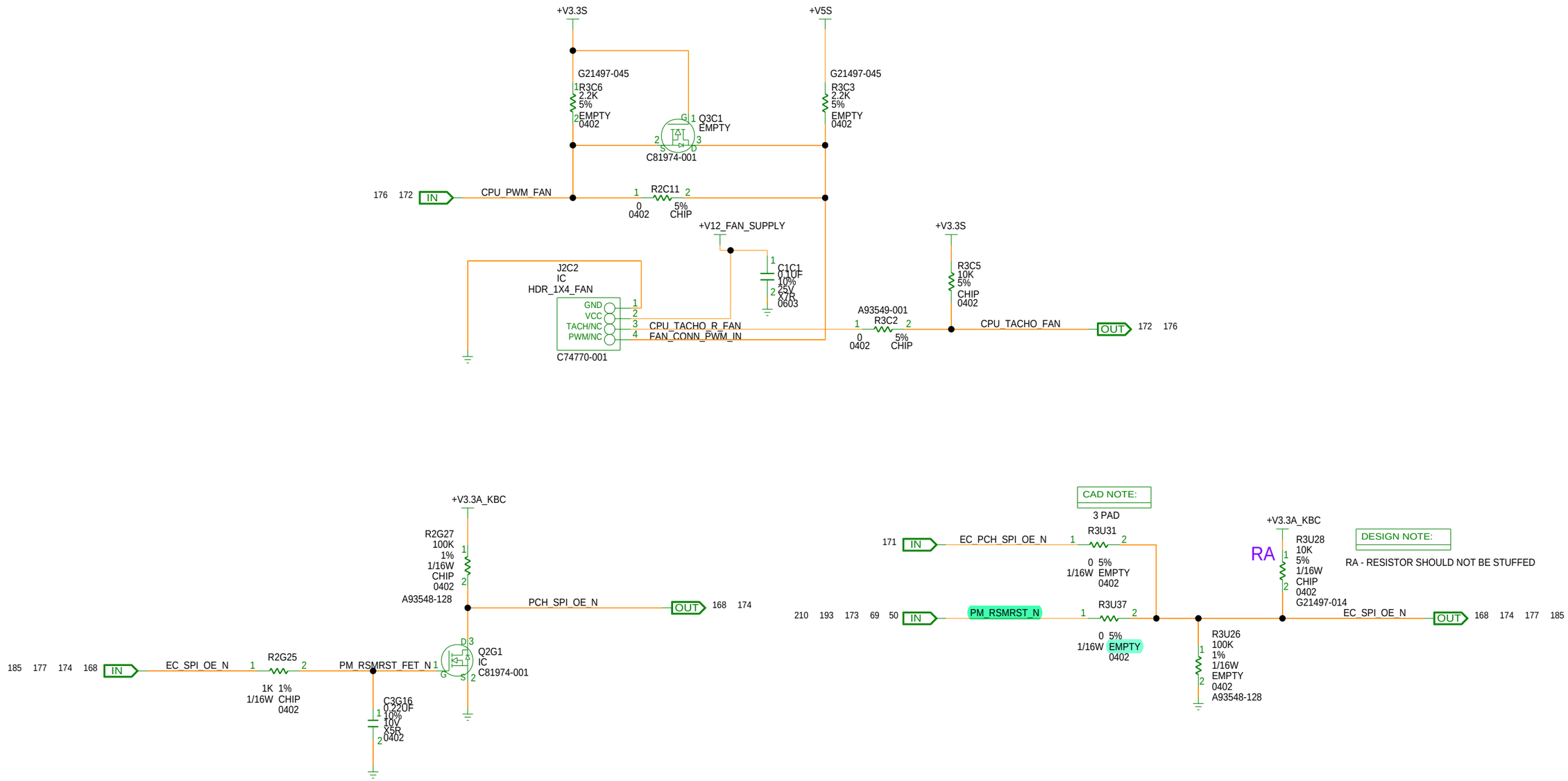
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.184
Wed Dec 18 18:08:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	184	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PROCESSOR FAN CONTROL



[PAGE_TITLE=EC - FAN HEADER]

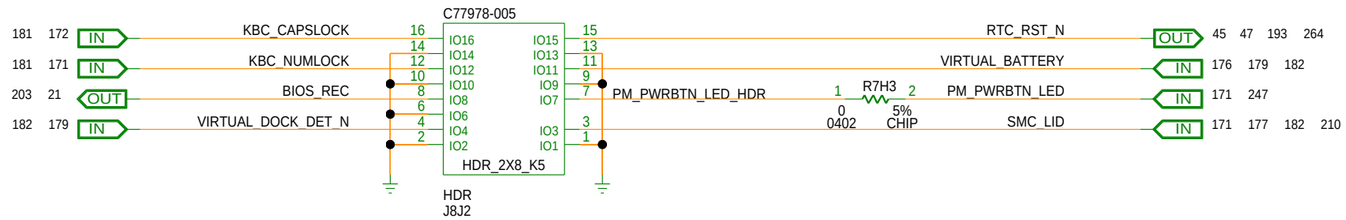
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.185
Wed Dec 18 18:08:21 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	185	1.0

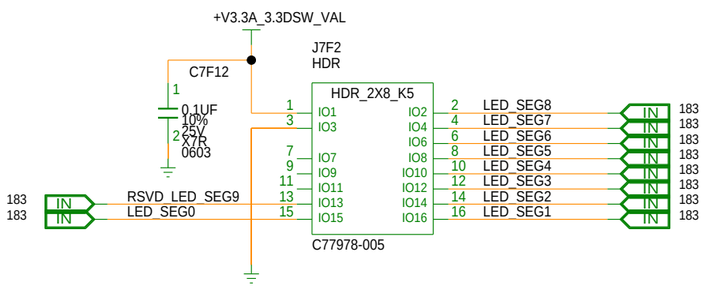
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

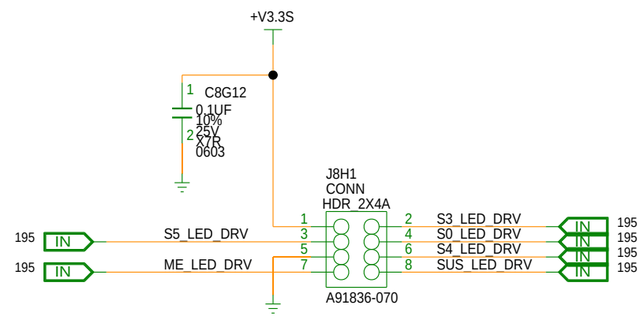
NOTE: REMOVE RSVD_TEST_RNG OFF-PAGE CONNECTOR
FROM CUSTOMER VERSION OF SCHEMATICS



SAS HEADER



8-PIN HEADER



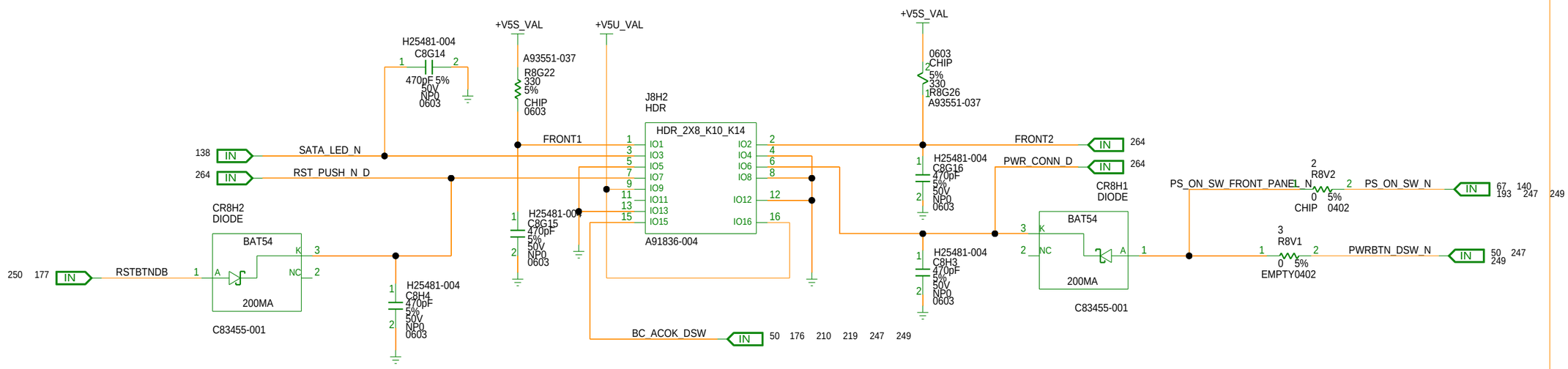
[PAGE_TITLE=EC - SAS HEADER]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.186
Wed Dec 18 18:08:22 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	186	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

FRONT PANEL HEADER



[PAGE_TITLE=EC - FRONT PANEL HEADER]

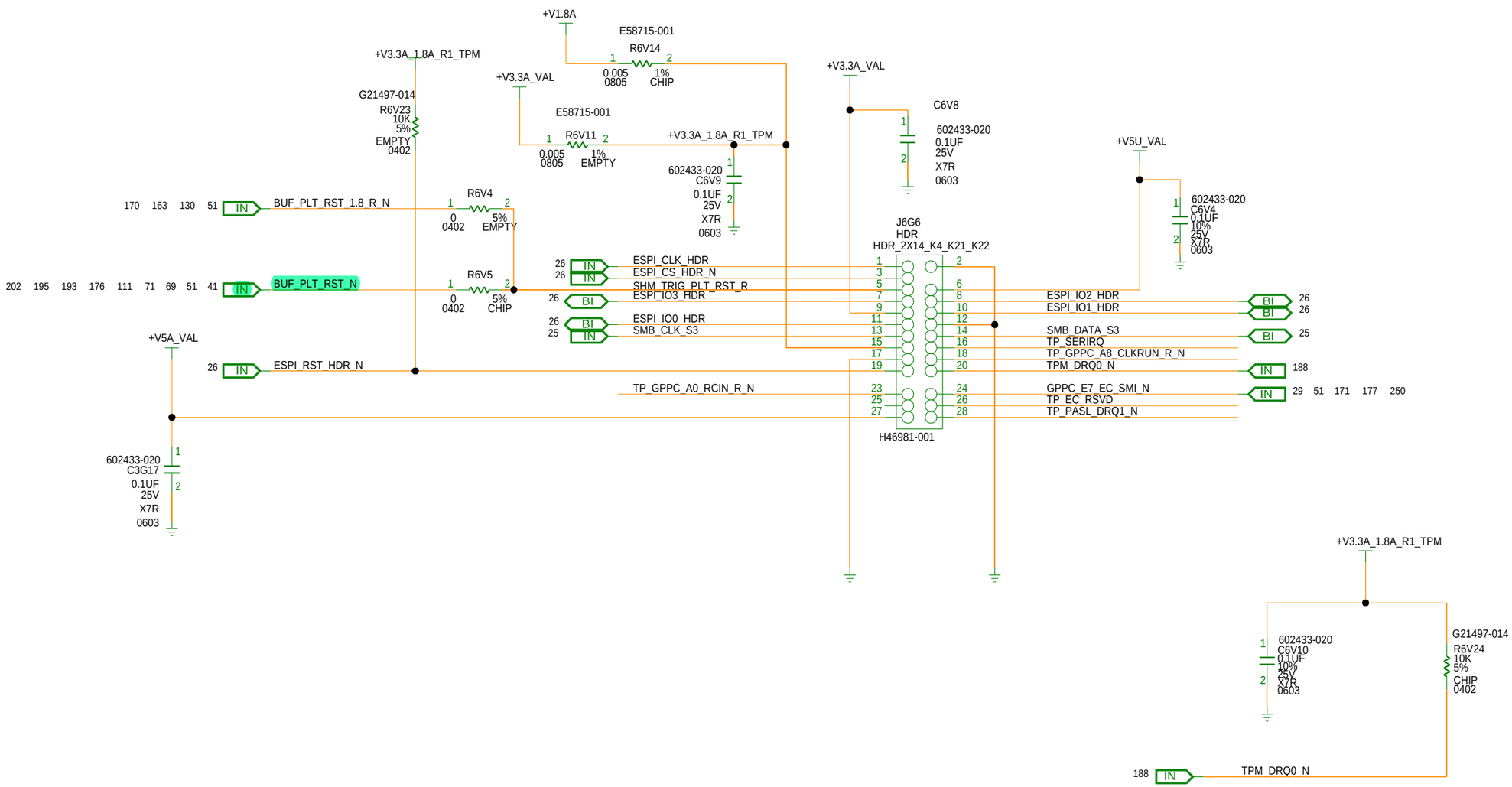
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.187
Wed Dec 18 18:08:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	187	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

ESPI BUS HEADER



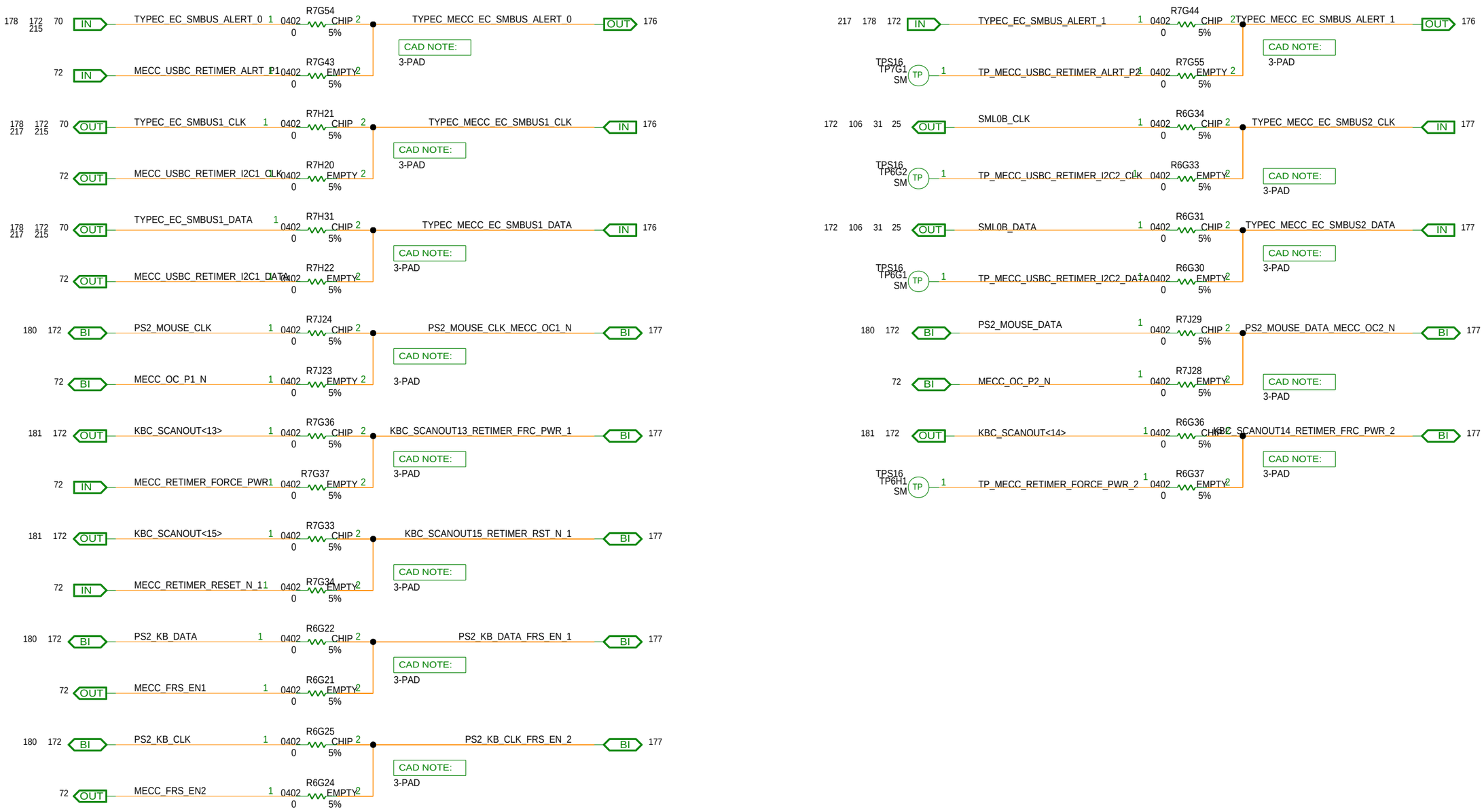
[PAGE_TITLE=EC - TPM HEADER FOR ESPI ONLY]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.188
Wed Dec 18 18:08:24 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	188	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



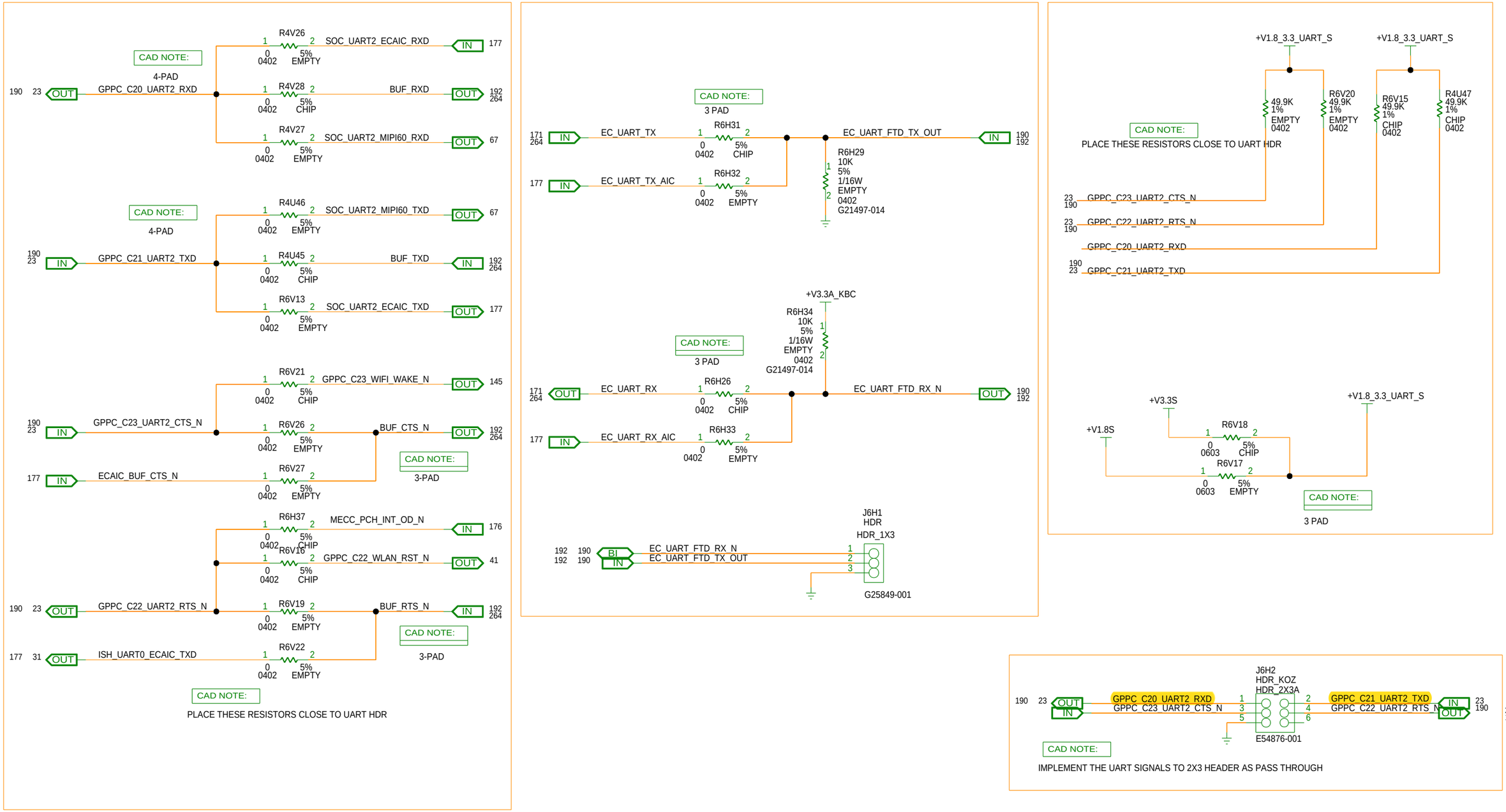
[PAGE_TITLE=MECC CHROME SIGNALS

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.189
Tue Oct 15 12:51:35 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	189	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



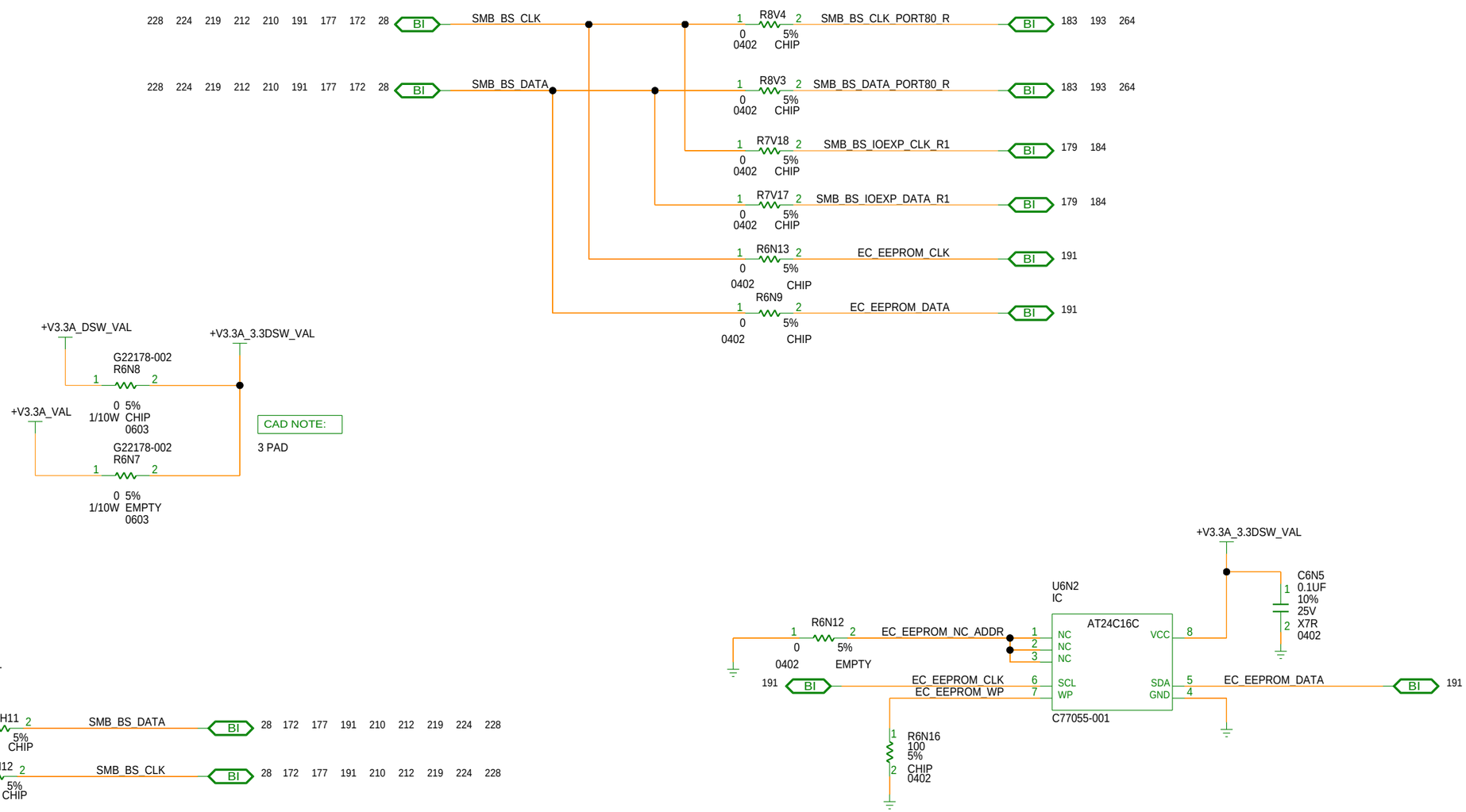
[PAGE_TITLE=EC - SERIAL DEBUG PORT]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.190
Wed Dec 18 18:08:25 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	190	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



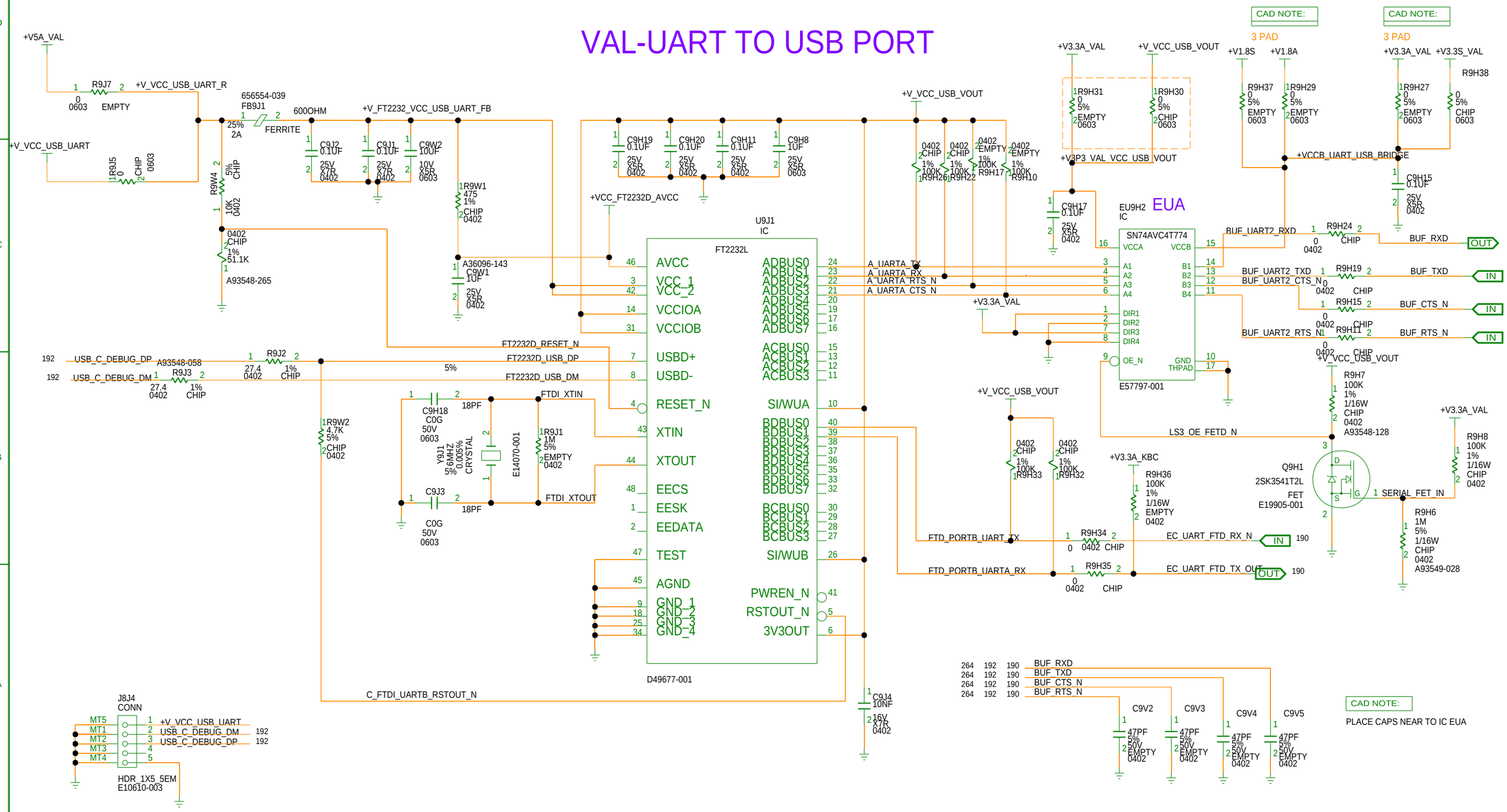
[PAGE_TITLE=EC - RESERVED -2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.191
Wed Dec 18 18:08:26 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	191	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

VAL-UART TO USB PORT



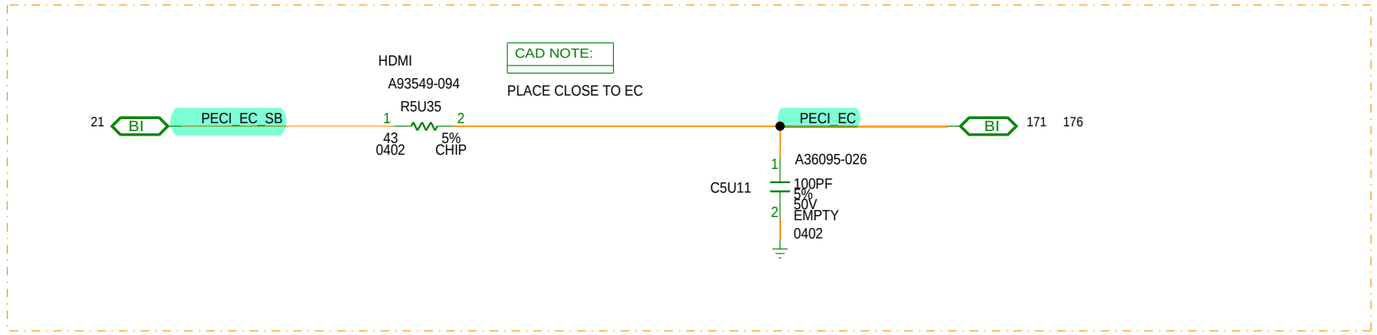
[PAGE_TITLE=VAL-UART TO USB PORT]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.192
Wed Dec 18 18:08:27 2019

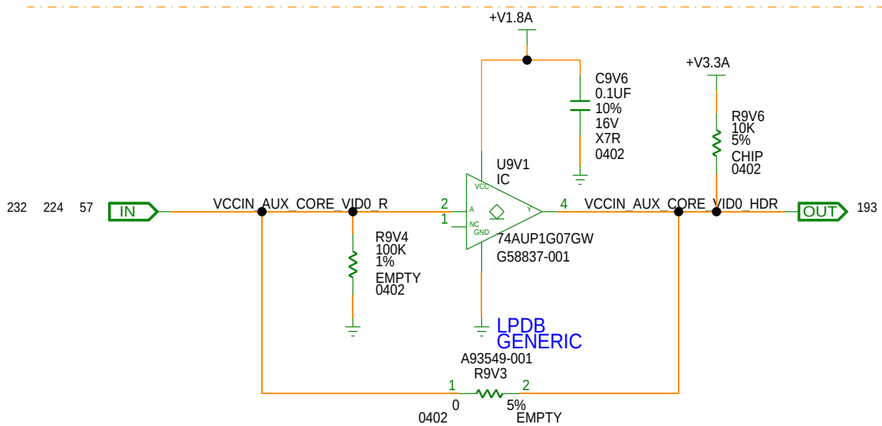
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	192	1.0

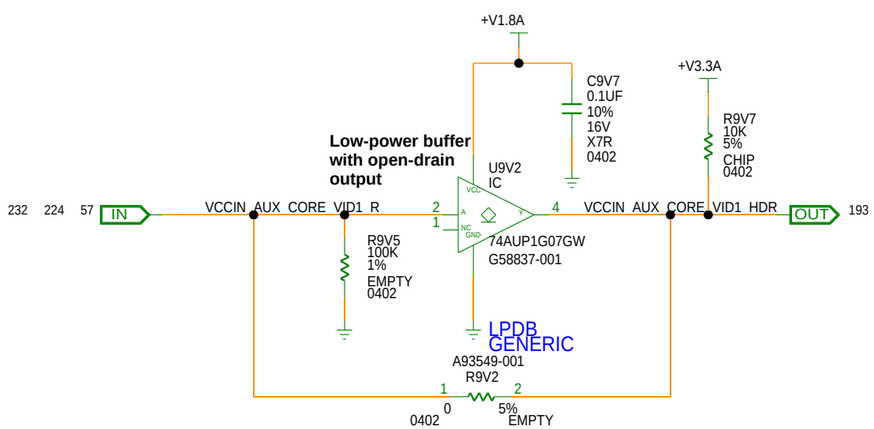
CUSTOM TEXT BPAGE

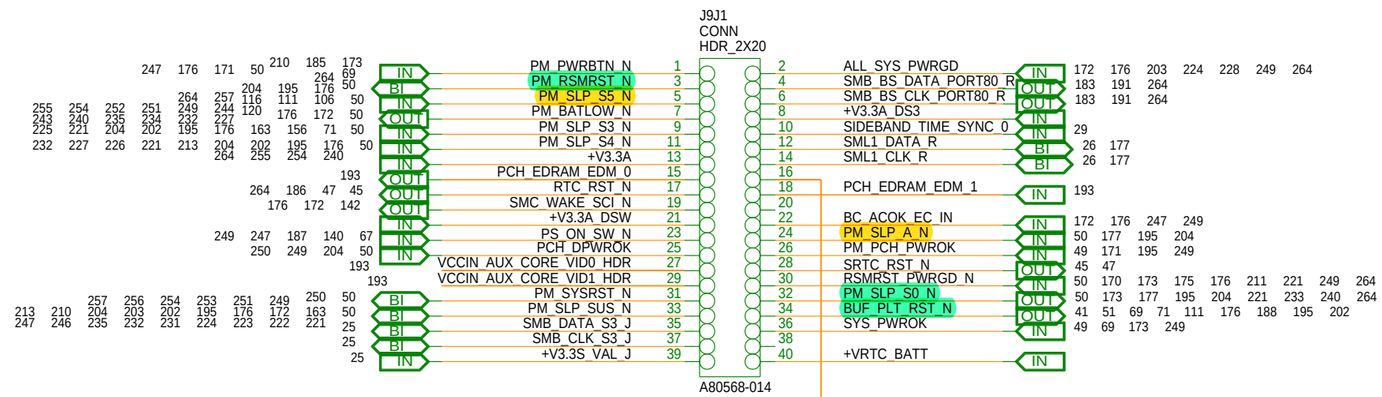
MODULE REV DETAILS		
MODULE NAME	REV	DATE

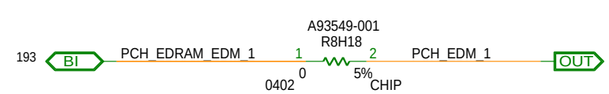


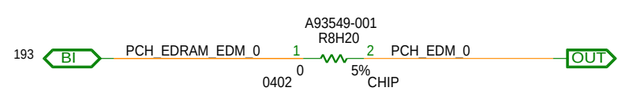
PM SIDE BAND HEADER











[PAGE_TITLE=PM SIDEBAND HEADER]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.193
Wed Dec 18 18:08:28 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	193	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

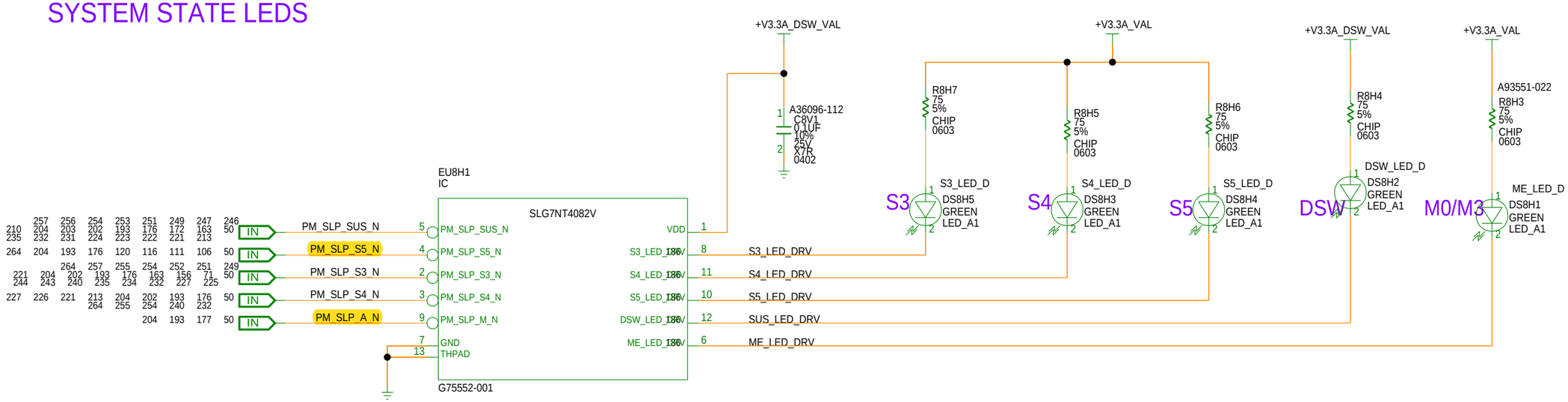
[PAGE_TITLE=RESERVED]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.194
Tue Oct 15 12:51:41 2019

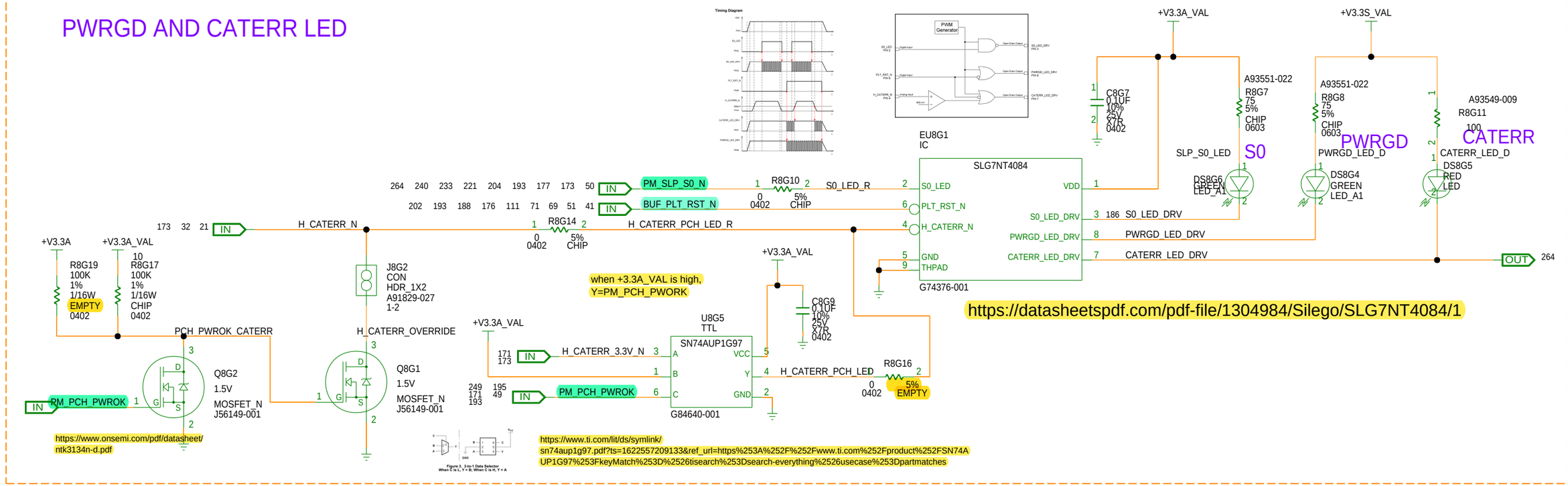
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	194	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

SYSTEM STATE LEDS



PWRGD AND CATERR LED



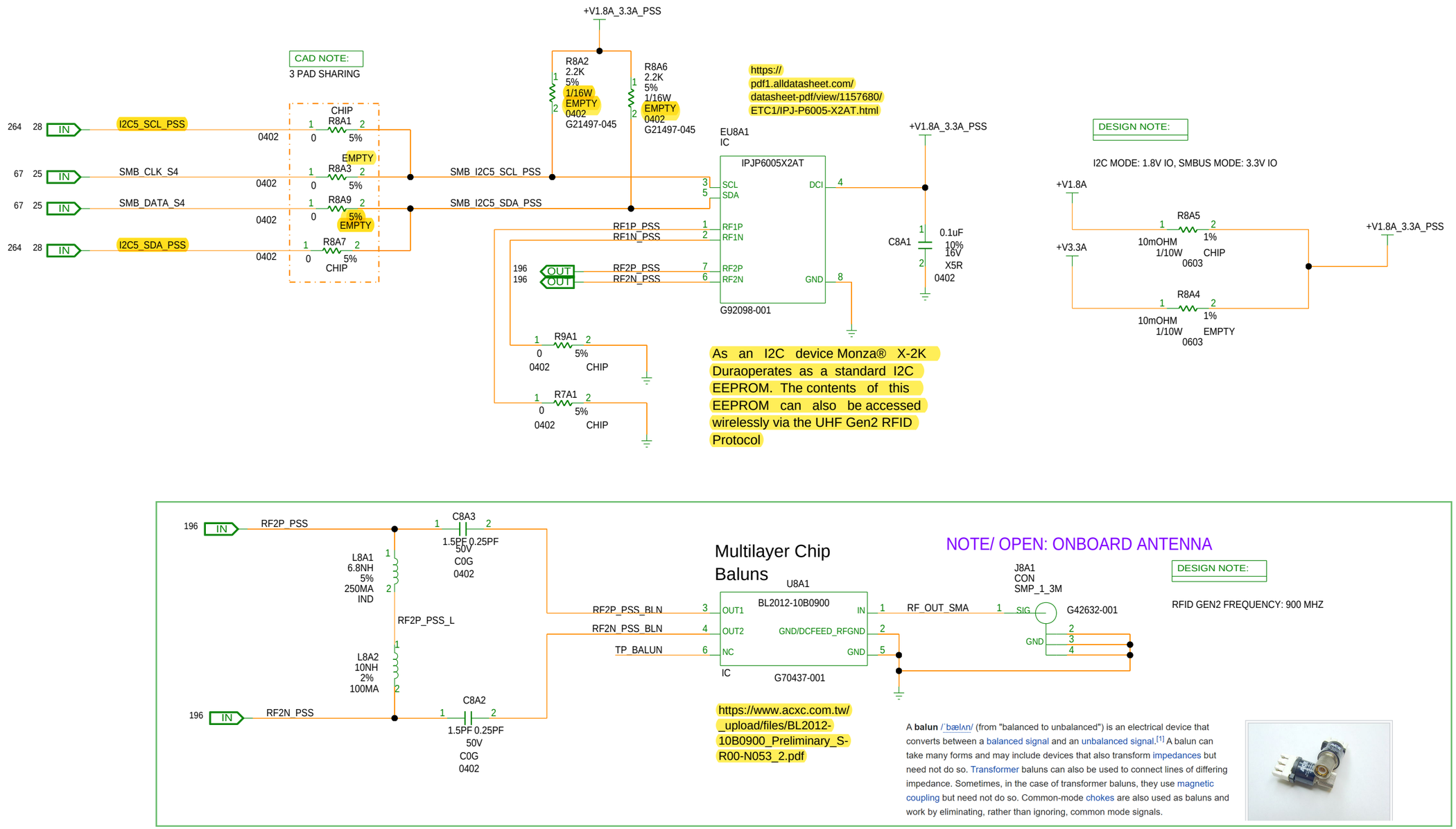
[PAGE_TITLE=SYSTEM STATE LED CIRCUITRY]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.195
Wed Dec 18 18:08:30 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	195	1.0

CUSTOM TEXT BPAGE

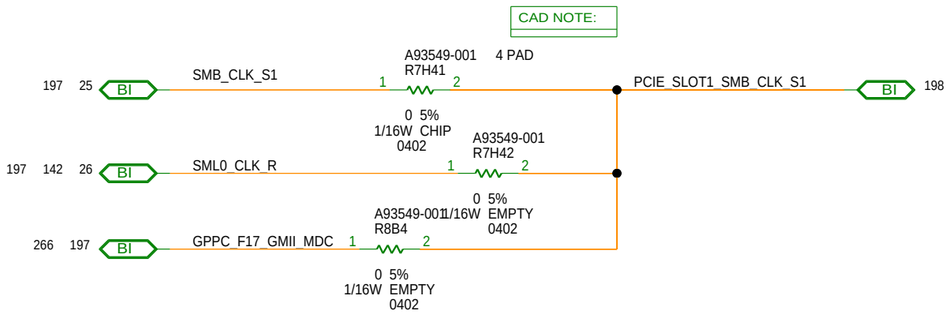
MODULE REV DETAILS		
MODULE NAME	REV	DATE

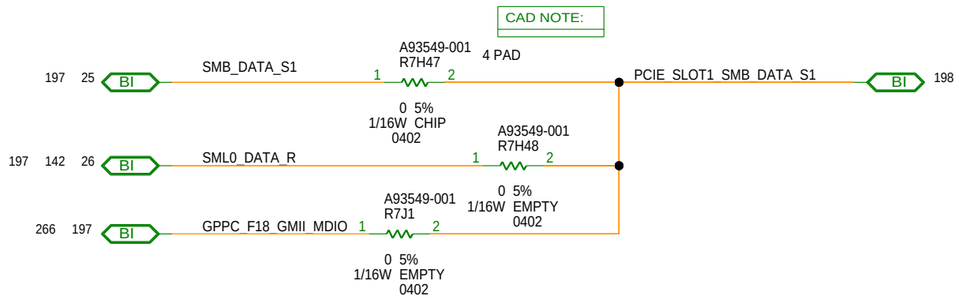


[PAGE_TITLE=PSS - PROCESSOR SECURE STORAGE- RFID ACCESSIBLE EEPROM 8K]

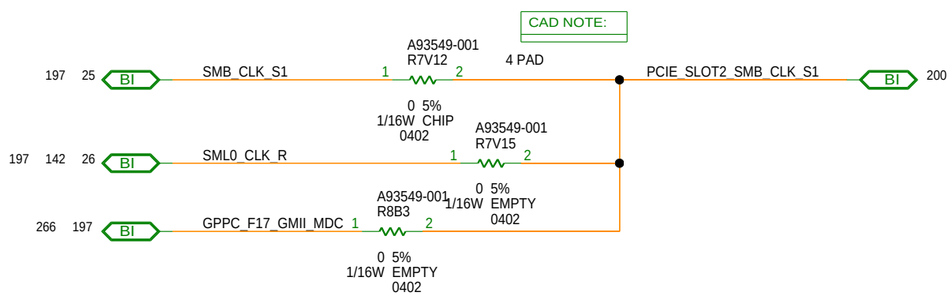
MODULE REV DETAILS		
MODULE NAME	REV	DATE

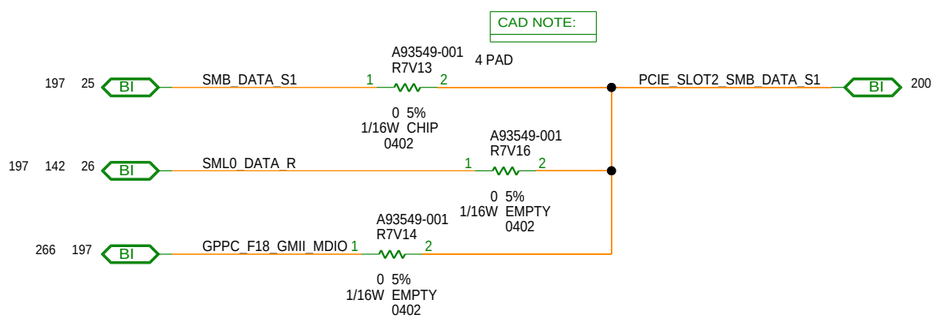
PCIE SLOT 1 SMB SIGNALS





PCIE SLOT 2 SMB SIGNALS





BPAGE DRAWING
tigerlake_u_ddr4.sch_1.197
Wed Dec 18 18:08:31 2019

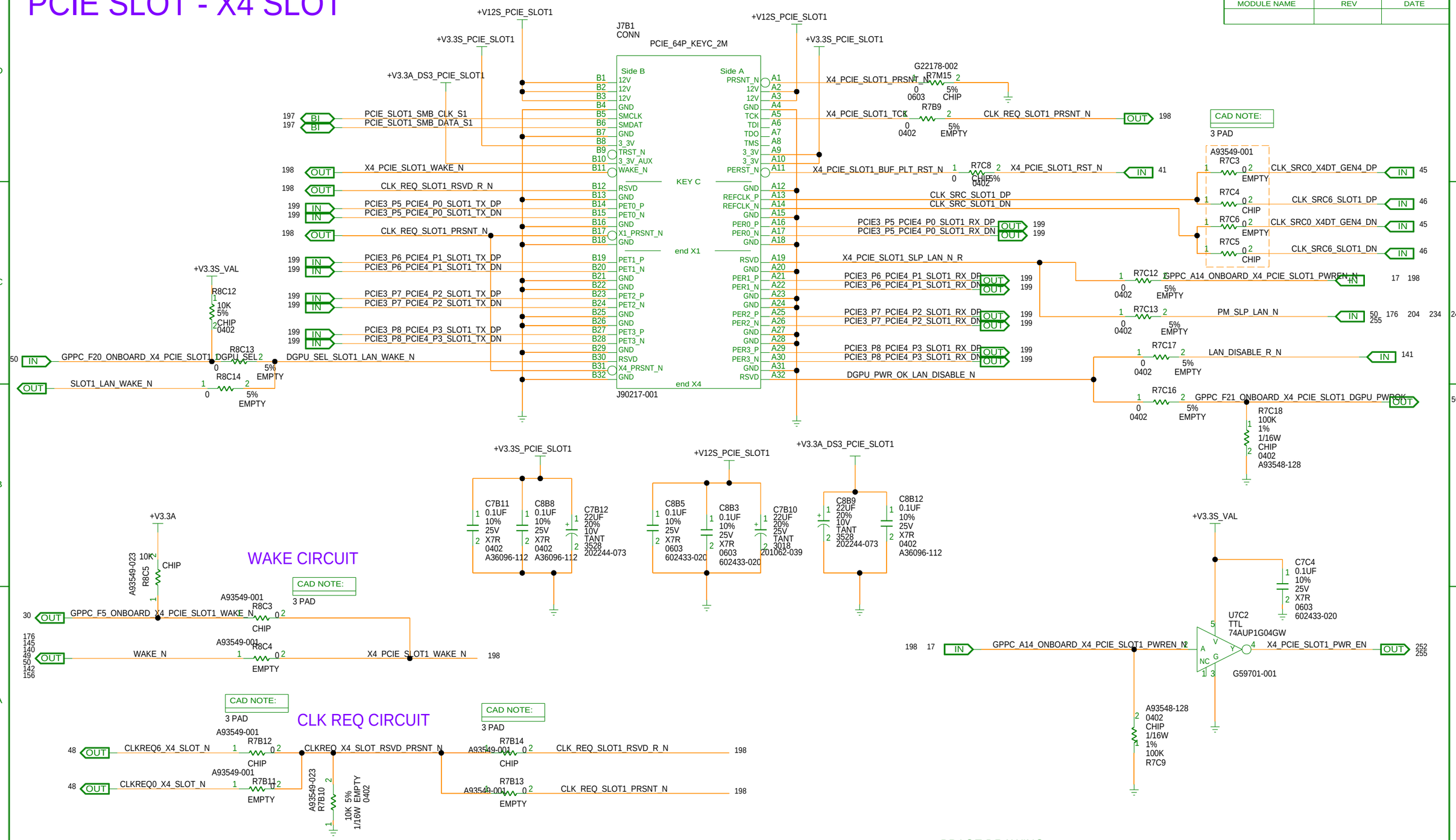
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	197	1.0

CUSTOM TEXT BPAGE

[PAGE_TITLE=SMB AND SML MAPPING]

PCIE SLOT - X4 SLOT

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=PCIE SLOT - X4 SLOT]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.198
Wed Dec 18 18:08:32 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	198	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE: 3 PAD

CAD NOTE: 3 PAD

CAD NOTE: PLACE CAP NEAR CONNECTOR

198	IN	PCIE3_P5_PCIE4_P0_SLOT1_RX_DP	3 A93549-001 R7N28 0 5% EMPTY	PCIE4_P0_SLOT1_RX_DP	OUT	73	73	IN	PCIE4_P0_SLOT1_TX_DP	2 A93549-001 0402 1/16W 5% R7N23 0 EMPTY	PCIE3_P5_PCIE4_P0_SLOT1_C_TX_DP	C8N3 0.22uF X5R	PCIE3_P5_PCIE4_P0_SLOT1_TX_DP	OUT	198
			A93549-001 R7N27 0 5% CHIP	PCIE3_P5_SLOT1_RX_DP	OUT	37	37	IN	PCIE3_P5_SLOT1_TX_DP	R7N24 0 CHIP					
198	IN	PCIE3_P5_PCIE4_P0_SLOT1_RX_DN	A93549-001 R7N26 0 5% EMPTY	PCIE4_P0_SLOT1_RX_DN	OUT	73	73	IN	PCIE4_P0_SLOT1_TX_DN	R7N19 0 EMPTY	PCIE3_P5_PCIE4_P0_SLOT1_C_TX_DN	C8N2 0.22uF X5R	PCIE3_P5_PCIE4_P0_SLOT1_TX_DN	OUT	198
			A93549-001 R7N25 0 5% CHIP	PCIE3_P5_SLOT1_RX_DN	OUT	37	37	IN	PCIE3_P5_SLOT1_TX_DN	R7N20 0 CHIP					
198	IN	PCIE3_P6_PCIE4_P1_SLOT1_RX_DP	A93549-001 R7N31 0 5% EMPTY	PCIE4_P1_SLOT1_RX_DP	OUT	73	73	IN	PCIE4_P1_SLOT1_TX_DP	R7N15 0 EMPTY	PCIE3_P6_PCIE4_P1_SLOT1_C_TX_DP	C8N5 0.22uF X5R	PCIE3_P6_PCIE4_P1_SLOT1_TX_DP	OUT	198
			A93549-001 R7N32 0 5% CHIP	PCIE3_P6_SLOT1_RX_DP	OUT	37	37	IN	PCIE3_P6_SLOT1_TX_DP	R7N16 0 CHIP					
198	IN	PCIE3_P6_PCIE4_P1_SLOT1_RX_DN	A93549-001 R7N36 0 5% EMPTY	PCIE4_P1_SLOT1_RX_DN	OUT	73	73	IN	PCIE4_P1_SLOT1_TX_DN	R7N13 0 EMPTY	PCIE3_P6_PCIE4_P1_SLOT1_C_TX_DN	C8N4 0.22uF X5R	PCIE3_P6_PCIE4_P1_SLOT1_TX_DN	OUT	198
			A93549-001 R7N35 0 5% CHIP	PCIE3_P6_SLOT1_RX_DN	OUT	37	37	IN	PCIE3_P6_SLOT1_TX_DN	R7N14 0 CHIP					
198	IN	PCIE3_P7_PCIE4_P2_SLOT1_RX_DP	A93549-001 R7N37 0 5% EMPTY	PCIE4_P2_SLOT1_RX_DP	OUT	73	73	IN	PCIE4_P2_SLOT1_TX_DP	R7N11 0 EMPTY	PCIE3_P7_PCIE4_P2_SLOT1_C_TX_DP	C7N4 0.22uF X5R	PCIE3_P7_PCIE4_P2_SLOT1_TX_DP	OUT	198
			A93549-001 R7N38 0 5% CHIP	PCIE3_P7_SLOT1_RX_DP	OUT	38	38	IN	PCIE3_P7_SLOT1_TX_DP	R7N12 0 CHIP					
198	IN	PCIE3_P7_PCIE4_P2_SLOT1_RX_DN	A93549-001 R7N39 0 5% EMPTY	PCIE4_P2_SLOT1_RX_DN	OUT	73	73	IN	PCIE4_P2_SLOT1_TX_DN	R7N7 0 EMPTY	PCIE3_P7_PCIE4_P2_SLOT1_C_TX_DN	C7N3 0.22uF X5R	PCIE3_P7_PCIE4_P2_SLOT1_TX_DN	OUT	198
			A93549-001 R7N40 0 5% CHIP	PCIE3_P7_SLOT1_RX_DN	OUT	38	38	IN	PCIE3_P7_SLOT1_TX_DN	R7N8 0 CHIP					
198	IN	PCIE3_P8_PCIE4_P3_SLOT1_RX_DP	4 A93549-001 R7N44 0 5% EMPTY	PCIE4_P3_SLOT1_RX_DP	OUT	73	73	IN	PCIE4_P3_SLOT1_TX_DP	R7N3 0 EMPTY	PCIE3_P8_PCIE4_P3_SLOT1_C_TX_DP	C7N2 0.22uF X5R	PCIE3_P8_PCIE4_P3_SLOT1_TX_DP	OUT	198
			1 A93549-001 R7N43 0 5% CHIP	PCIE3_P8_SLOT1_RX_DP	OUT	38	38	IN	PCIE3_P8_SLOT1_TX_DP	R7N4 0 CHIP					
198	IN	PCIE3_P8_PCIE4_P3_SLOT1_RX_DN	2 A93549-001 R7N48 0 5% EMPTY	PCIE4_P3_SLOT1_RX_DN	OUT	73	73	IN	PCIE4_P3_SLOT1_TX_DN	R7N1 0 EMPTY	PCIE3_P8_PCIE4_P3_SLOT1_C_TX_DN	C7N1 0.22uF X5R	PCIE3_P8_PCIE4_P3_SLOT1_TX_DN	OUT	198
			3 A93549-001 R7N47 0 5% CHIP	PCIE3_P8_SLOT1_RX_DN	OUT	38	38	IN	PCIE3_P8_SLOT1_TX_DN	R7N2 0 CHIP					

[PAGE_TITLE=PCIE SLOT - X4 SLOT SIGNAL MUX GEN3/GEN4

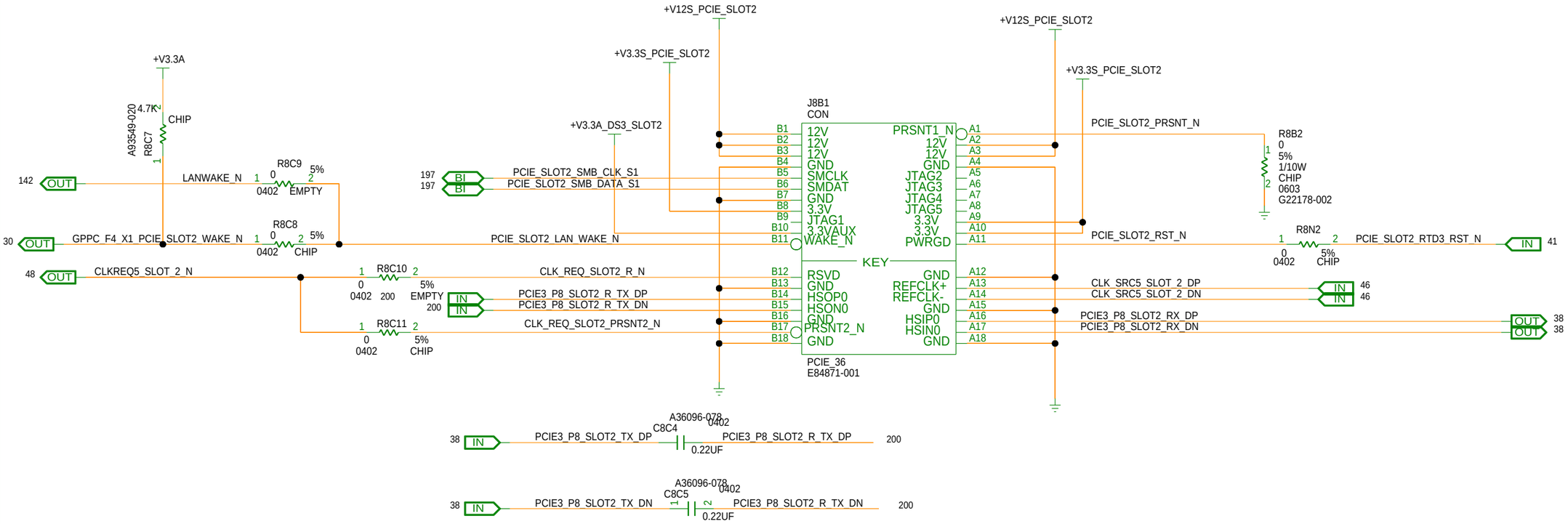
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.199
Wed Dec 18 18:08:33 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	199	1.0

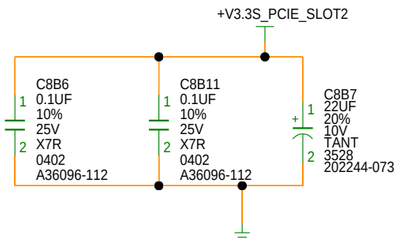
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

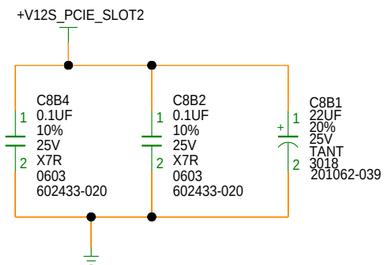
PCIE SLOT - X1 SLOT



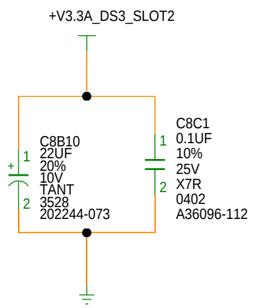
CAD NOTE:
PLACE NEAR PIN B8,A9,A10



CAD NOTE:
PLACE CAP NEAR B1,B2,B3



CAD NOTE:
PLACE CAP NEAR B10



[PAGE_TITLE=PCIE SLOT - X1 SLOT]

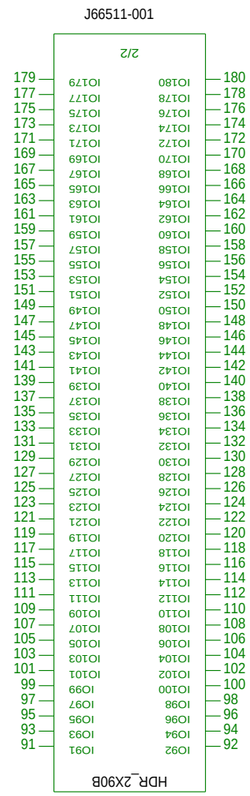
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.200
Wed Dec 18 18:08:34 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	200	1.0

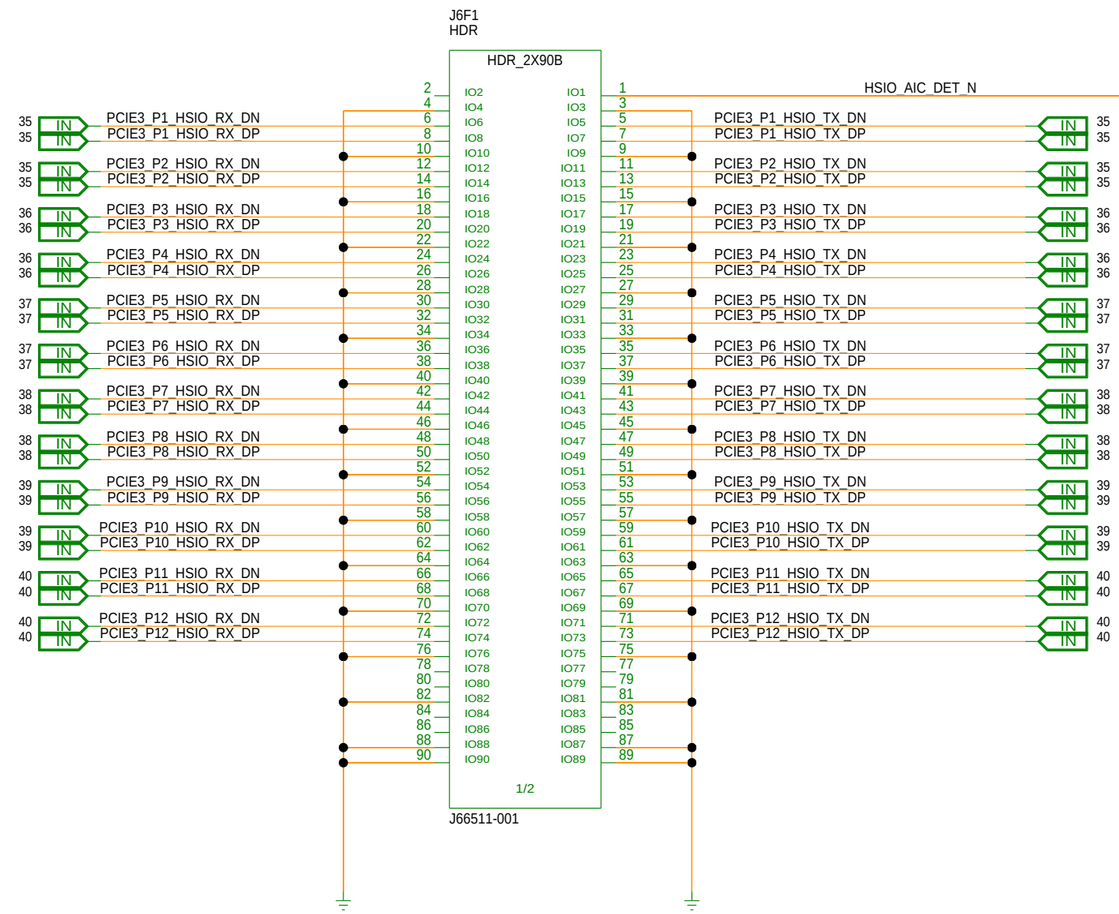
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



J6D4
EMPTY



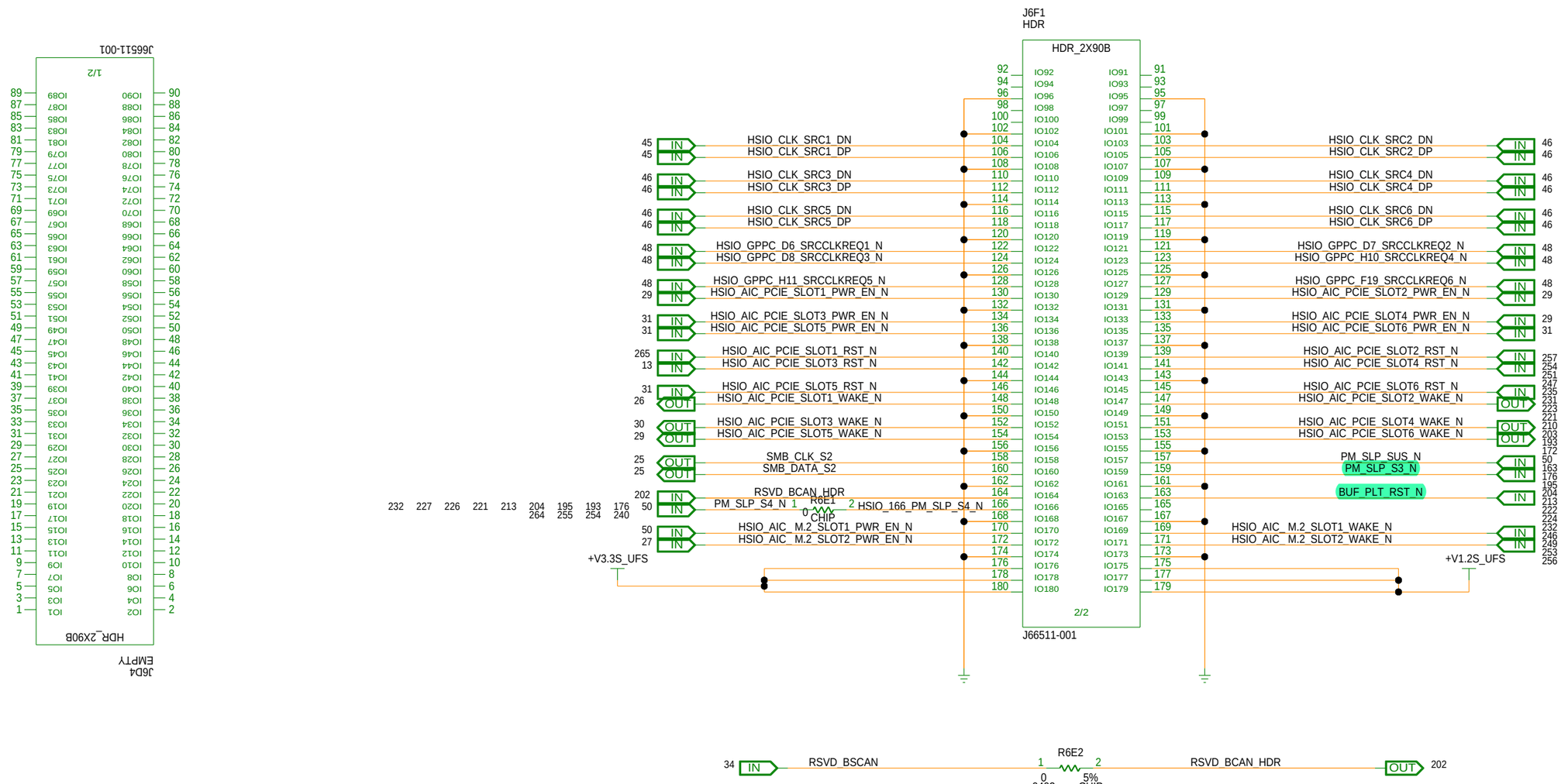
[PAGE_TITLE=HSIO CONNECTOR (1 OF 4)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.201
Wed Dec 18 18:08:35 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	201	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



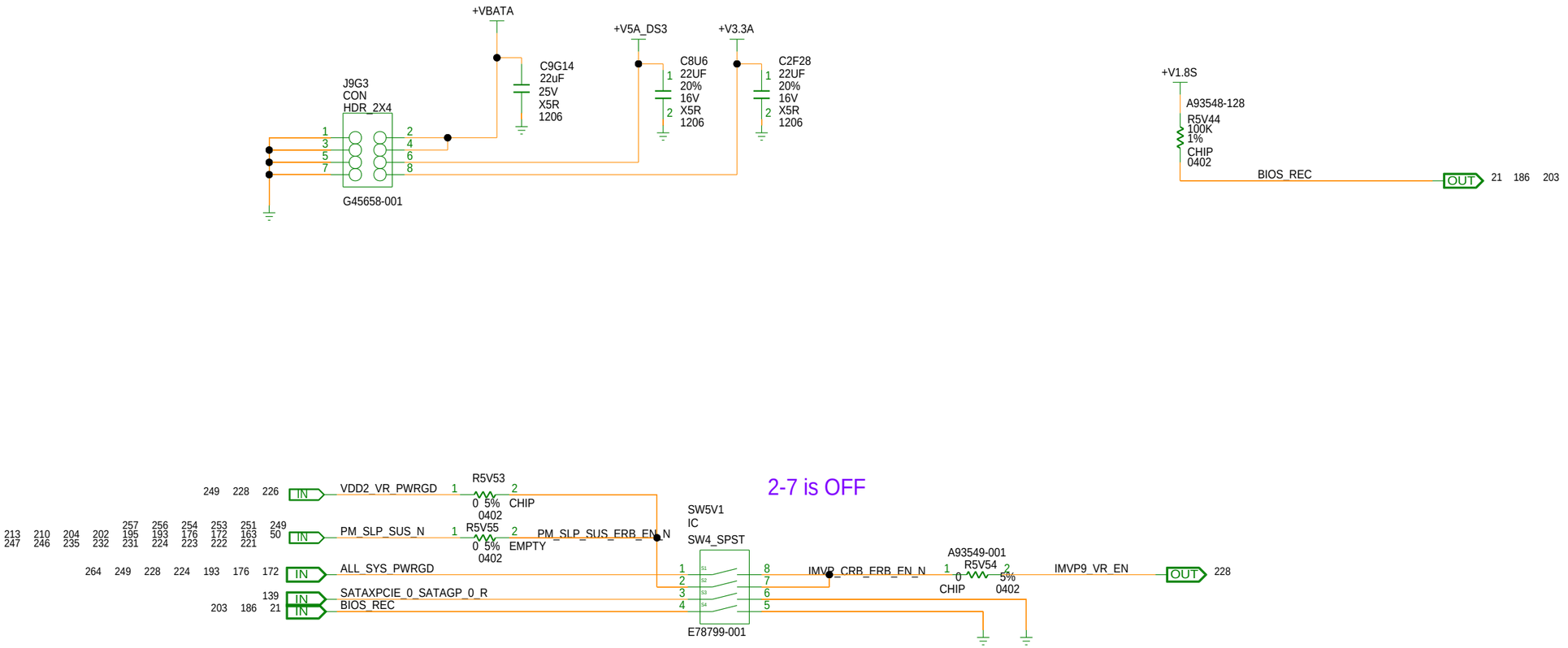
[PAGE_TITLE=HSIO CONNECTOR (2 OF 4)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.202
Wed Dec 18 18:08:36 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	202	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



STRAP/GPIO NAME	DEFAULT CONFIG REQUIRED	CONFIG CHANGE IF REQ
SATA_HOT_PLUG	OPEN(NO HOT PLUG)	CLOSED(HOT PLUG)
BIOS RECOVERY	OPEN(NO BIOS REC)	CLOSED (BIOS REC)

ENABLE THROUGH FIRMWARE CHANGES

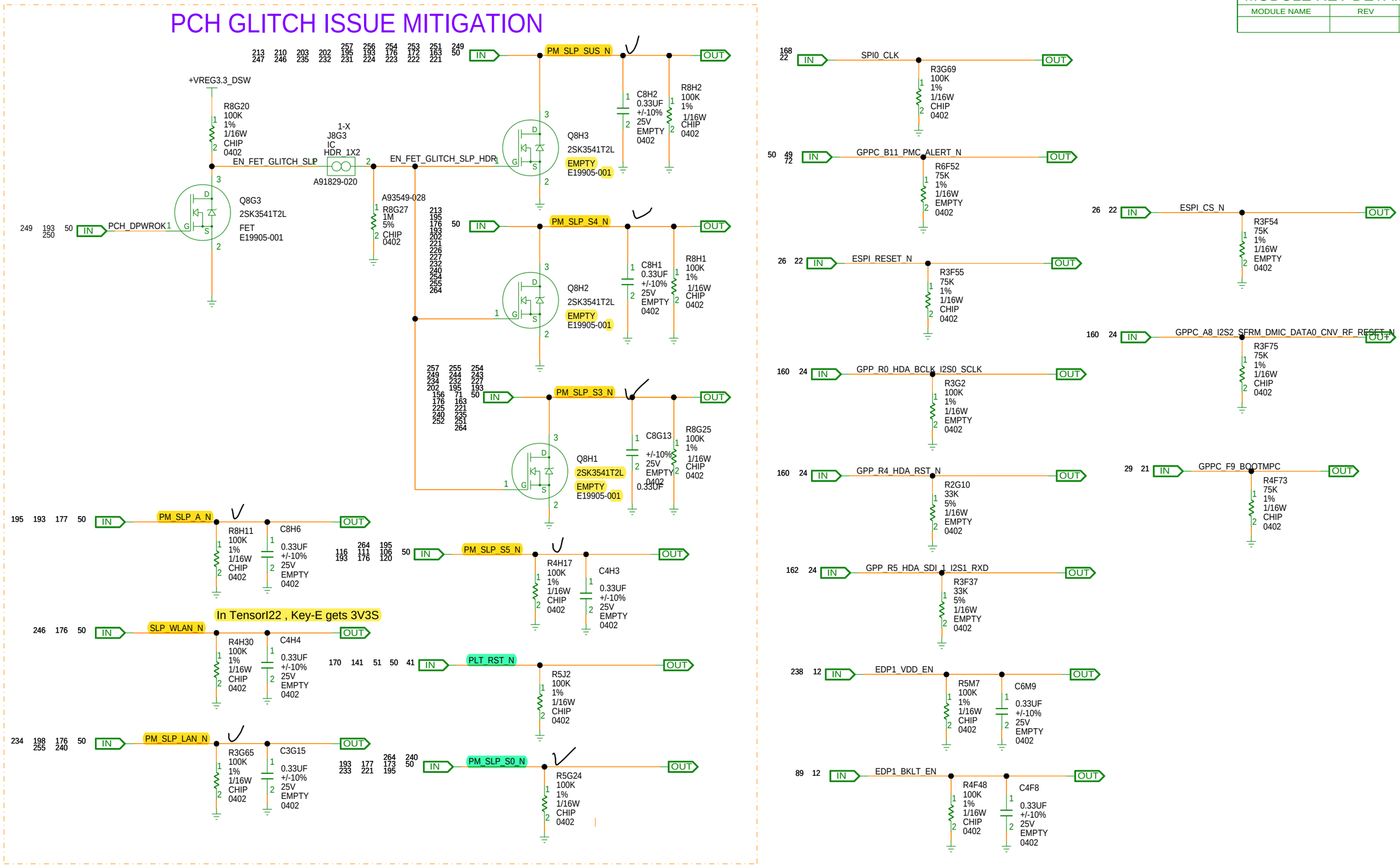
[PAGE_TITLE=POWER HEADER FOR INTERPOSER]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.203
Wed Dec 18 18:08:37 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	203	1.0

CUSTOM TEXT BPAGE

PCH GLITCH ISSUE MITIGATION



MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=GLITCH FREE CIRCUIT]

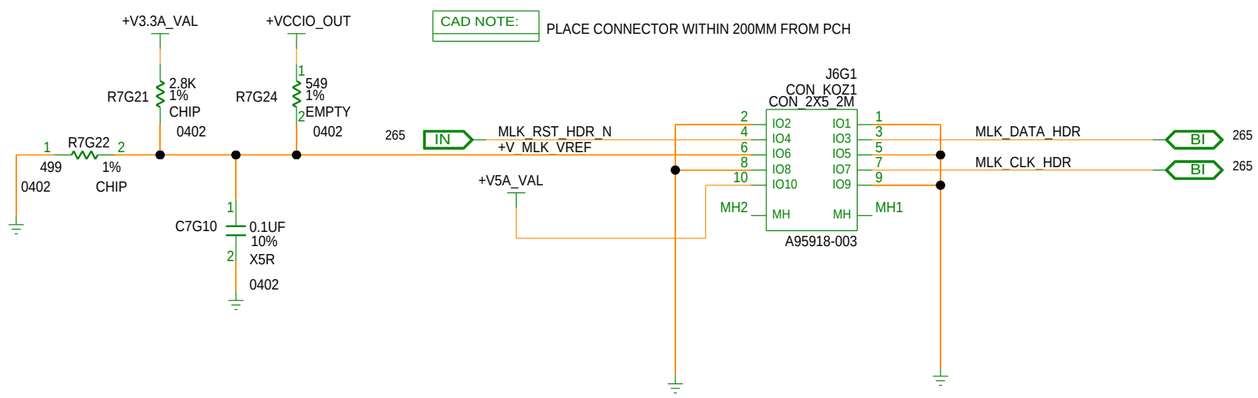
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.204
Wed Dec 18 18:08:38 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	204	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

MLINK HEADER



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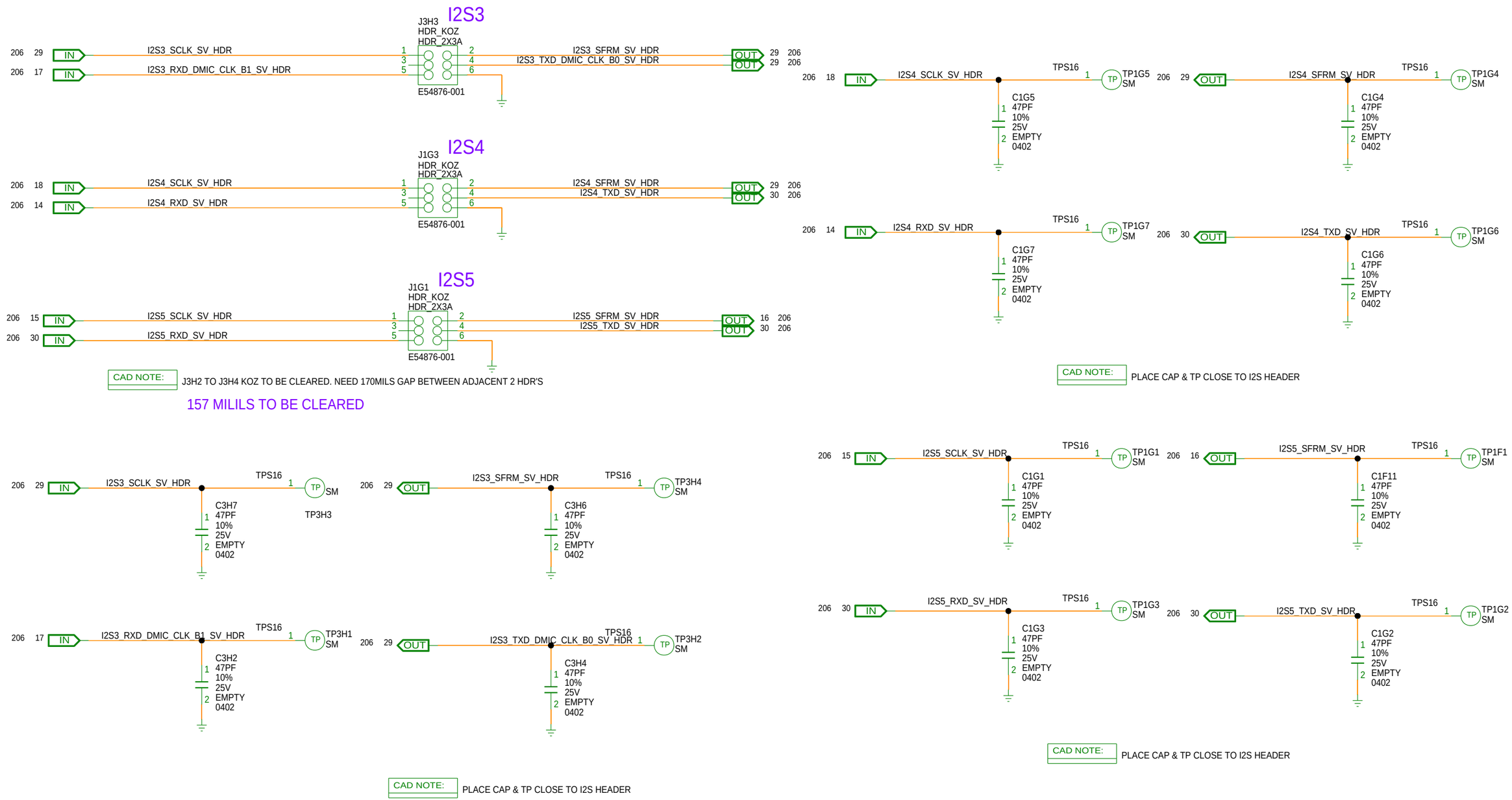
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.205
Wed Dec 18 18:08:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	205	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=IO - HEADERS - 1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.206
Wed Dec 18 18:08:40 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	206	1.0

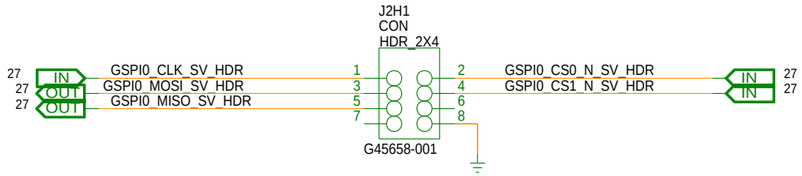
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE: MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

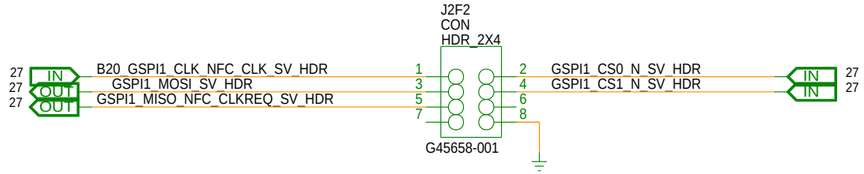
CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

GSPI0 HEADER



CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

GSPI1 HEADER



GSPI2 IS AVAILABLE ON ISH SPI AND ISH UART HEADER
SPI1 IS AVAILABLE ON THC SV HEADER

[PAGE_TITLE=IO - HEADERS - GSPI]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.207
Wed Dec 18 18:08:41 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	207	1.0

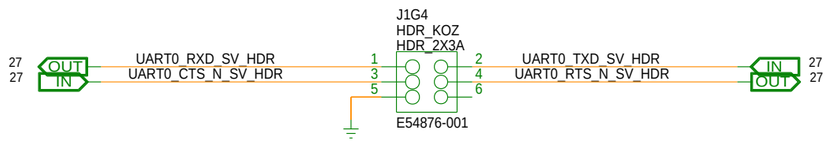
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE: MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

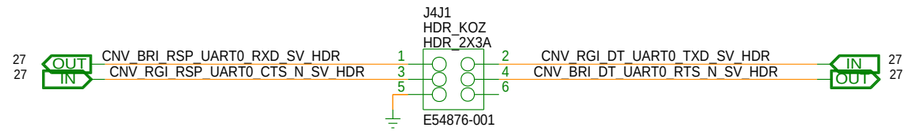
LPSS UART0 HEADER

CAD NOTE: PLACE CONNECTOR WITHIN 300MM FROM PCH



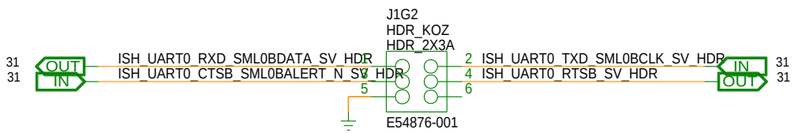
CNV UART0 HEADER

CAD NOTE: PLACE CONNECTOR WITHIN 300MM FROM PCH



ISH UART0 / SMLINK0B HEADER

CAD NOTE: PLACE CONNECTOR WITHIN 300MM FROM PCH



[PAGE_TITLE= IO HEADERS - UART HEADERS]

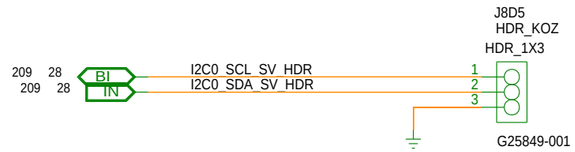
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.208
Wed Dec 18 18:08:42 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	208	1.0

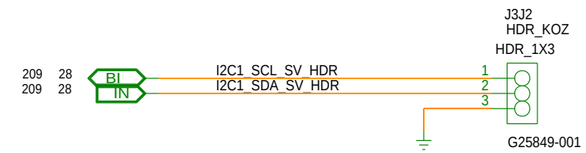
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

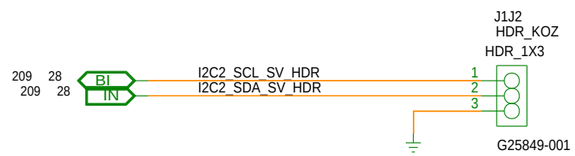
LPSS I2C0 SV HEADER



LPSS I2C1 SV HEADER

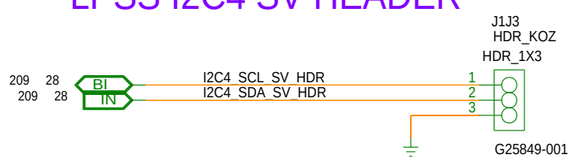


LPSS I2C2 SV HEADER



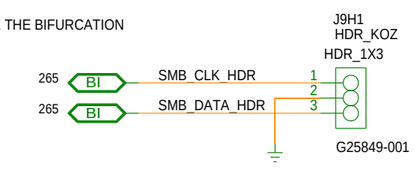
LPSS I2C3 SV HEADER

LPSS I2C4 SV HEADER



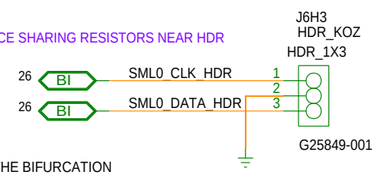
SMBUS SV HEADER

DESIGN NOTE:
SMBUS PULL UPS ARE BEFORE THE BIFURCATION



SMLINK0 SV HEADER OR MDIO GPIO HEADER

PLACE SHARING RESISTORS NEAR HDR



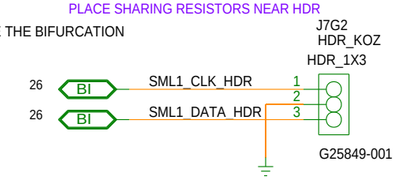
DESIGN NOTE:
SMLINK PULL UPS ARE BEFORE THE BIFURCATION

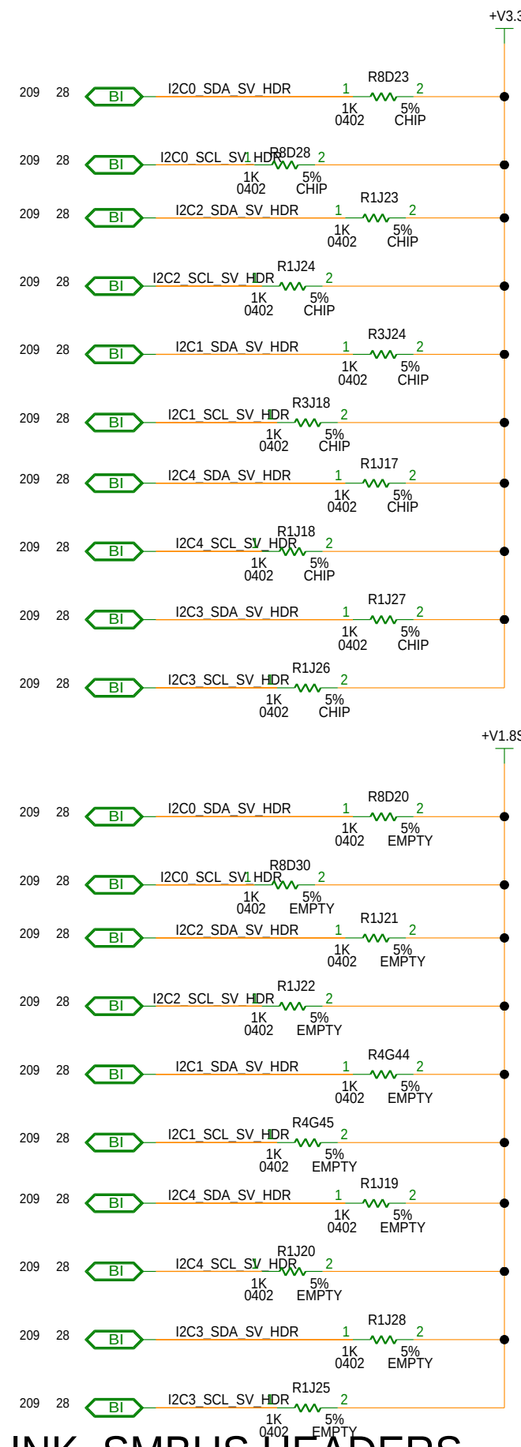
DESIGN NOTE:
REMOVE THE SMLINK0 PULL UPS WHILE USING AS MDIO GPIOS FOR IOTG VALIDATION

SMLINK1 SV HEADER

DESIGN NOTE:
SMLINK PULL UPS ARE BEFORE THE BIFURCATION

PLACE SHARING RESISTORS NEAR HDR





[PAGE_TITLE=IO HEADERS- LPSS I2C, SMLINK, SMBUS HEADERS

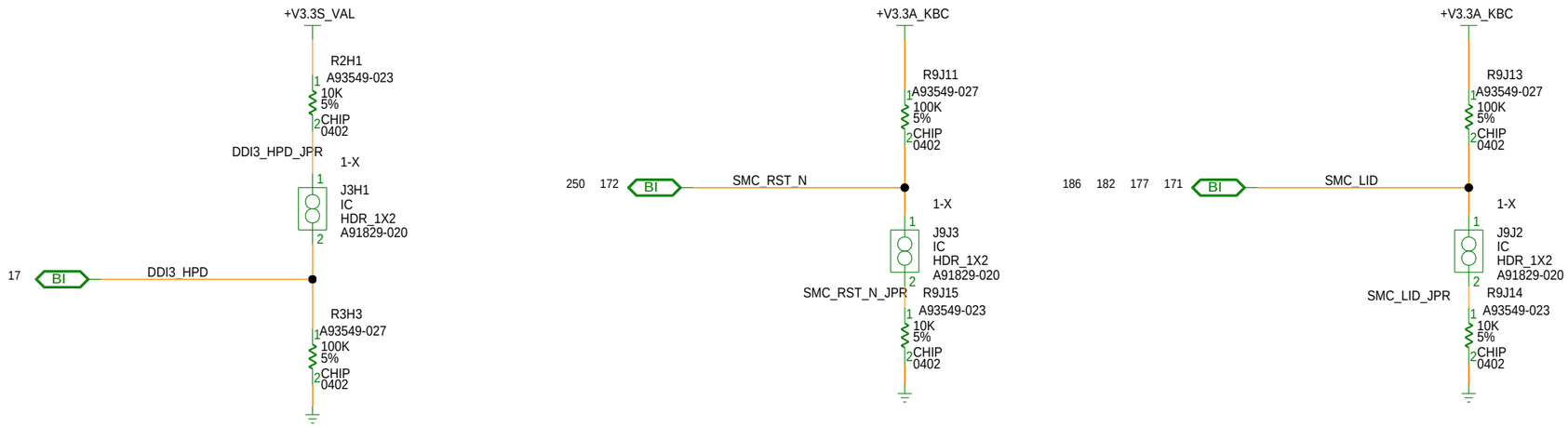
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.209
Wed Dec 18 18:08:42 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	209	1.0

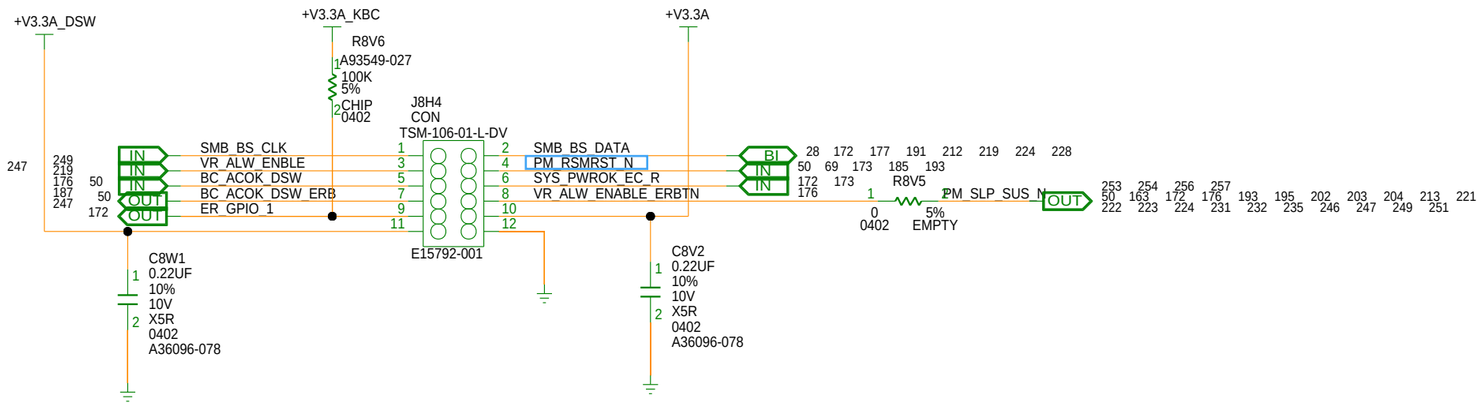
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

JUMPERS FOR VALIDATION



EYE RIVER VALIDATION HEADER



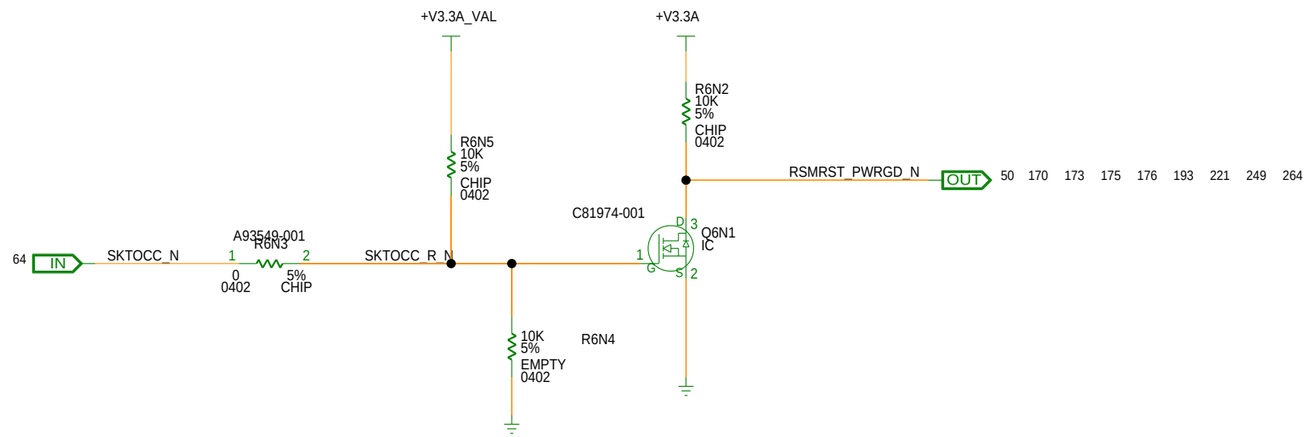
[PAGE_TITLE= IO HEADERS- EYE RIVER HEADER AND OTHER JUMPERS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.210
Wed Dec 18 18:08:43 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	210	1.0

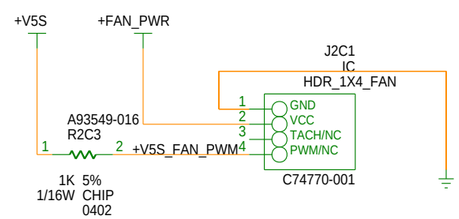
MODULE REV DETAILS		
MODULE NAME	REV	DATE

SKTOCC_N -> H_PRESENT_N (CPU DETECT,SKTOCC_N)



CONNECT TO A PROPER VSS PIN OF PCH
PROCESSOR & PCH PART DETECT

FAN HEADER



DESIGN NOTE:

J2A4 FAN CONNECTOR ON & STANDBY(S3)

[PAGE_TITLE=RESERVED

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.211
Wed Dec 18 18:08:45 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	211	1.0

Single/Multi-Channel DC Power/Energy Monitor with Accumulator

CHANGED PU VOLTAGE TO VCCIO_OUT oF U3C1

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE:

CAD NOTE: PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB

USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS

IC PAC1934T-I/J6CX J55617-001

U3C1

https://ww1.microchip.com/downloads/en/DeviceDoc/PAC1931-Family-Data-Sheet-DS20005850E.pdf

PWR MON1 7BIT I2C ADDR: 0X18

CAD NOTE: PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB

USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS

CAD NOTE: 3 PAD

CAD NOTE: 3 PAD

CAD NOTE: PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB

CAD NOTE: USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS

U6B4

PWR MON2 7BIT I2C ADDR: 0X11

U3G1

PWR MON3 7BIT I2C ADDR: 0X1E

BPAGE DRAWING

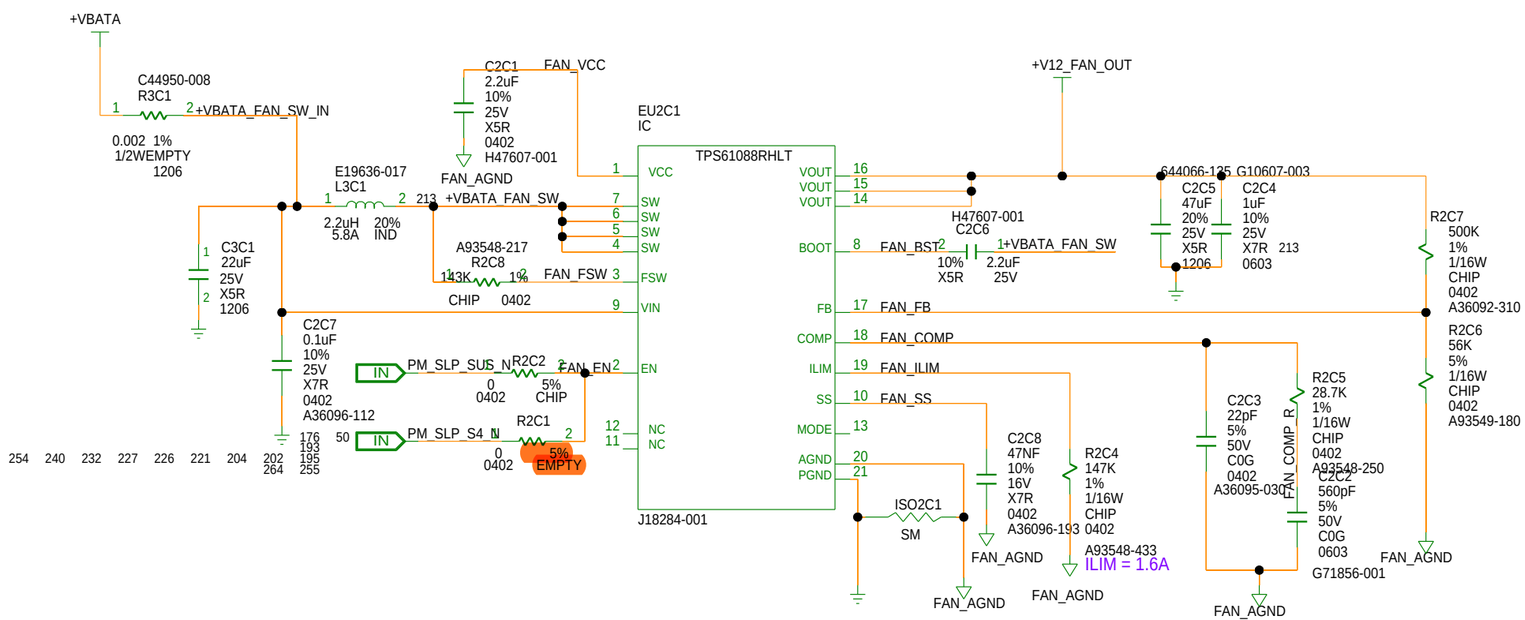
tigerlake_u_ddr4.sch_1.212
Wed Dec 18 18:08:46 2019

[PAGE_TITLE=POWER METER - EAC]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	212	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=FAN_BOOST CONVERTER]

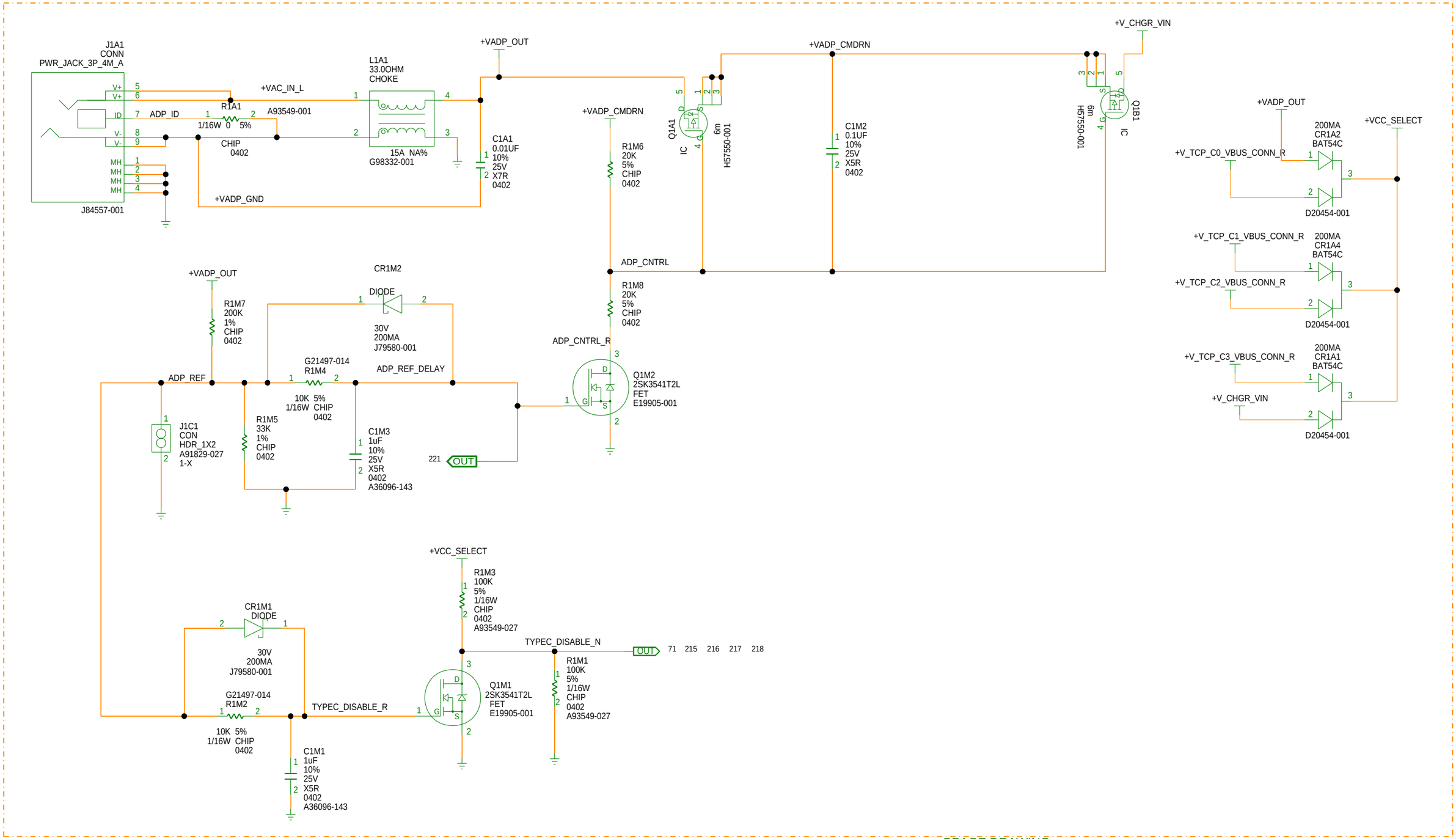
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.213
Wed Dec 18 18:08:47 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	213	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

STANDARD AC BRICK - POWER SELECTION CIRCUITRY



[PAGE_TITLE= STANDARD AC BRICK - POWER SELECTION CIRCUITRY]

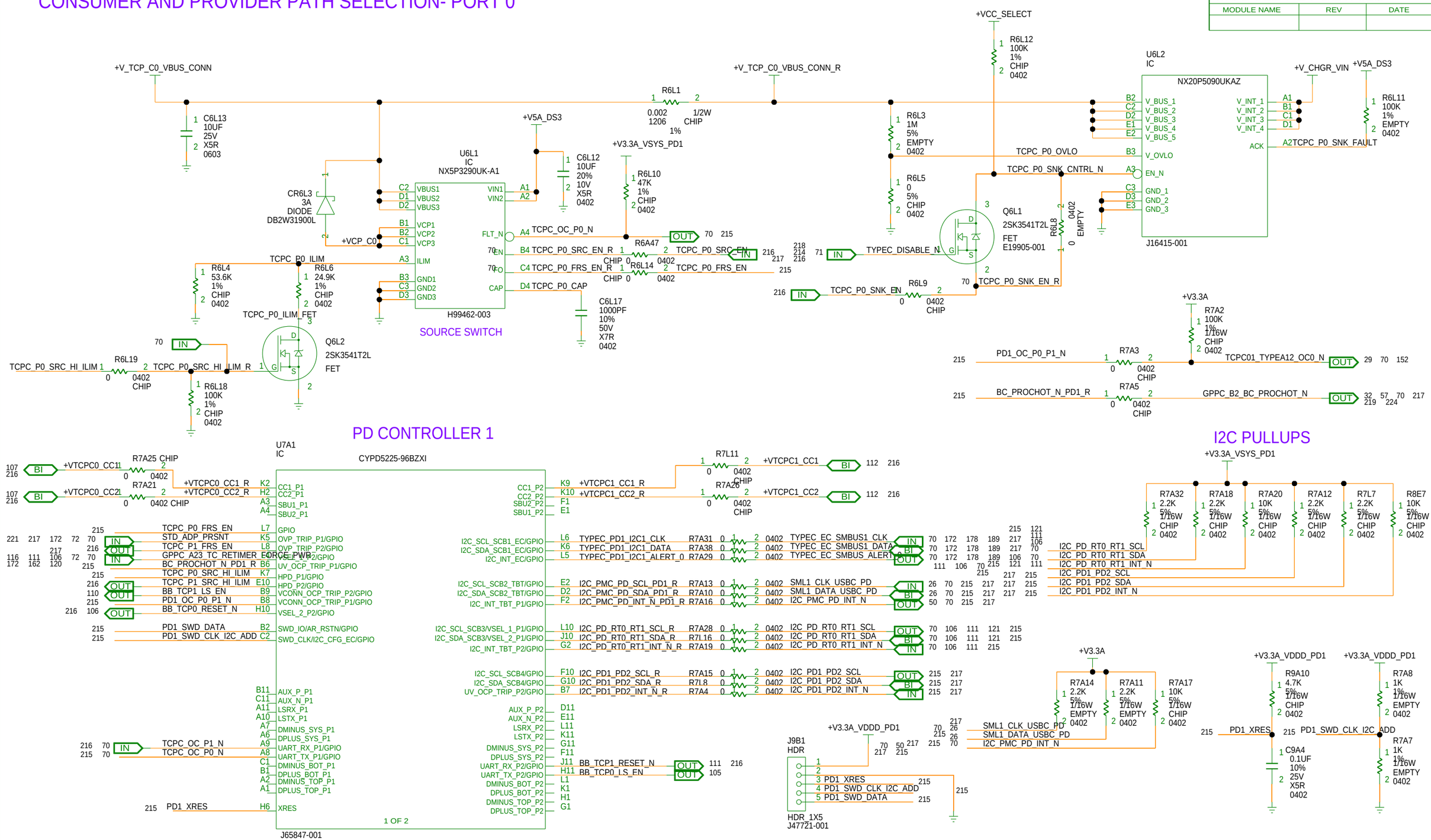
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.214
Wed Dec 18 18:08:48 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	214	1.0

CUSTOM TEXT BPAGE

CONSUMER AND PROVIDER PATH SELECTION- PORT 0

MODULE REV DETAILS		
MODULE NAME	REV	DATE



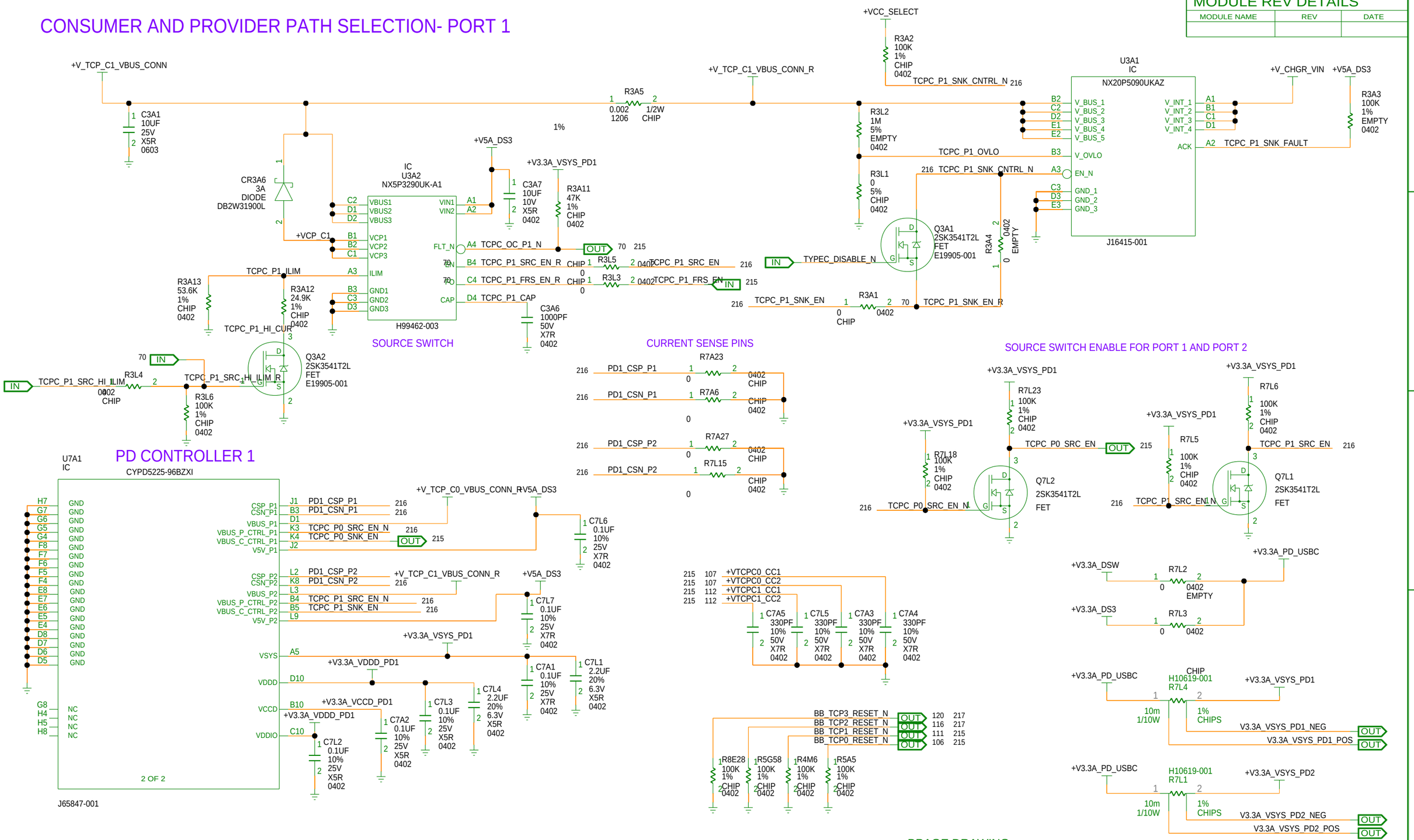
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.215
Wed Dec 18 18:08:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	215	1.0

[PAGE_TITLE= CONSUMER AND PROVIDER PATH SELECTION - PORT 0]

CONSUMER AND PROVIDER PATH SELECTION- PORT 1

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= CONSUMER AND PROVIDER PATH SELECTION - PORT 1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.216
Wed Dec 18 18:08:50 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	216	1.0

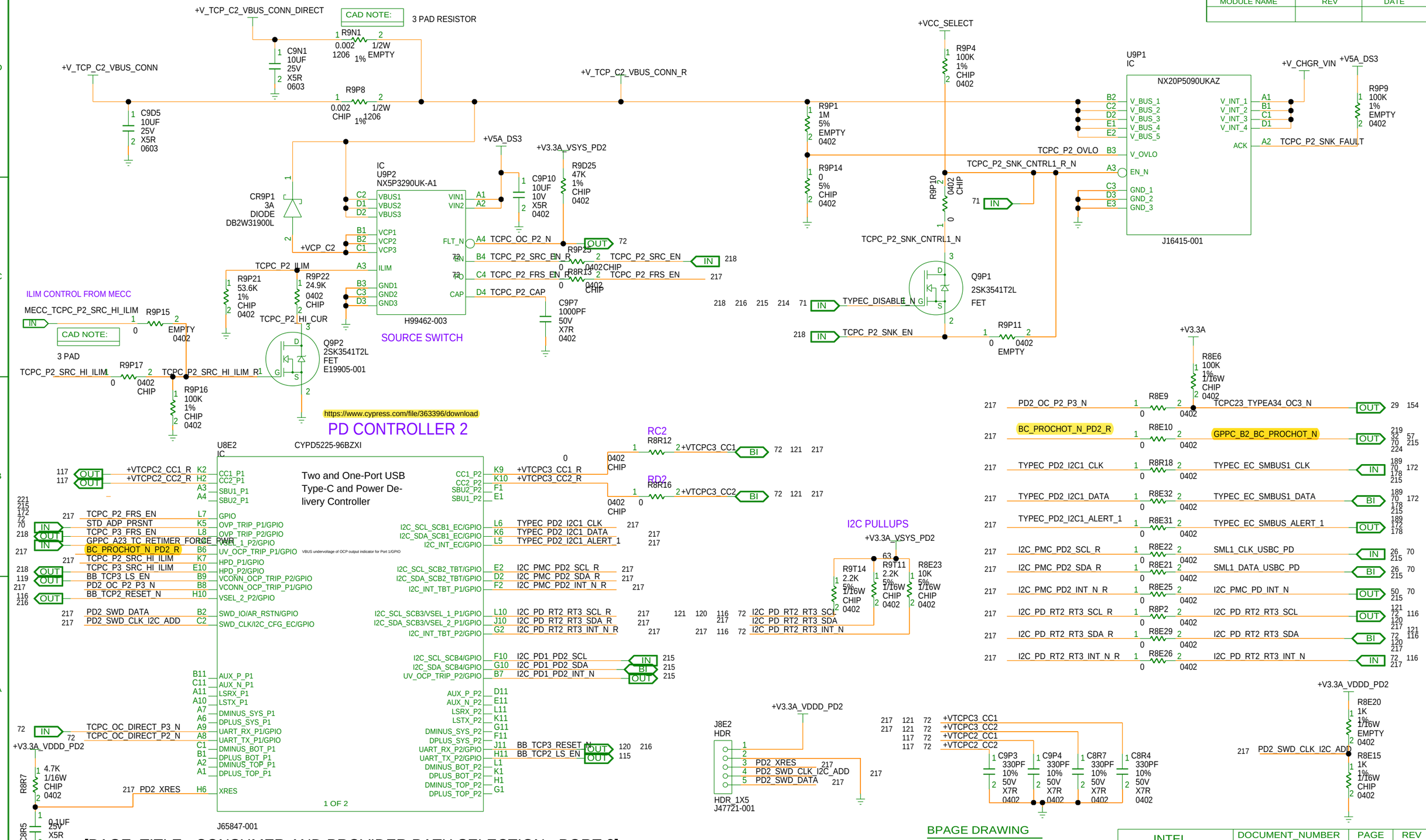
CUSTOM TEXT BPAGE

MOUNTING HOLES

CR-217 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE217

CONSUMER AND PROVIDER PATH SELECTION- PORT 2

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= CONSUMER AND PROVIDER PATH SELECTION - PORT 2]

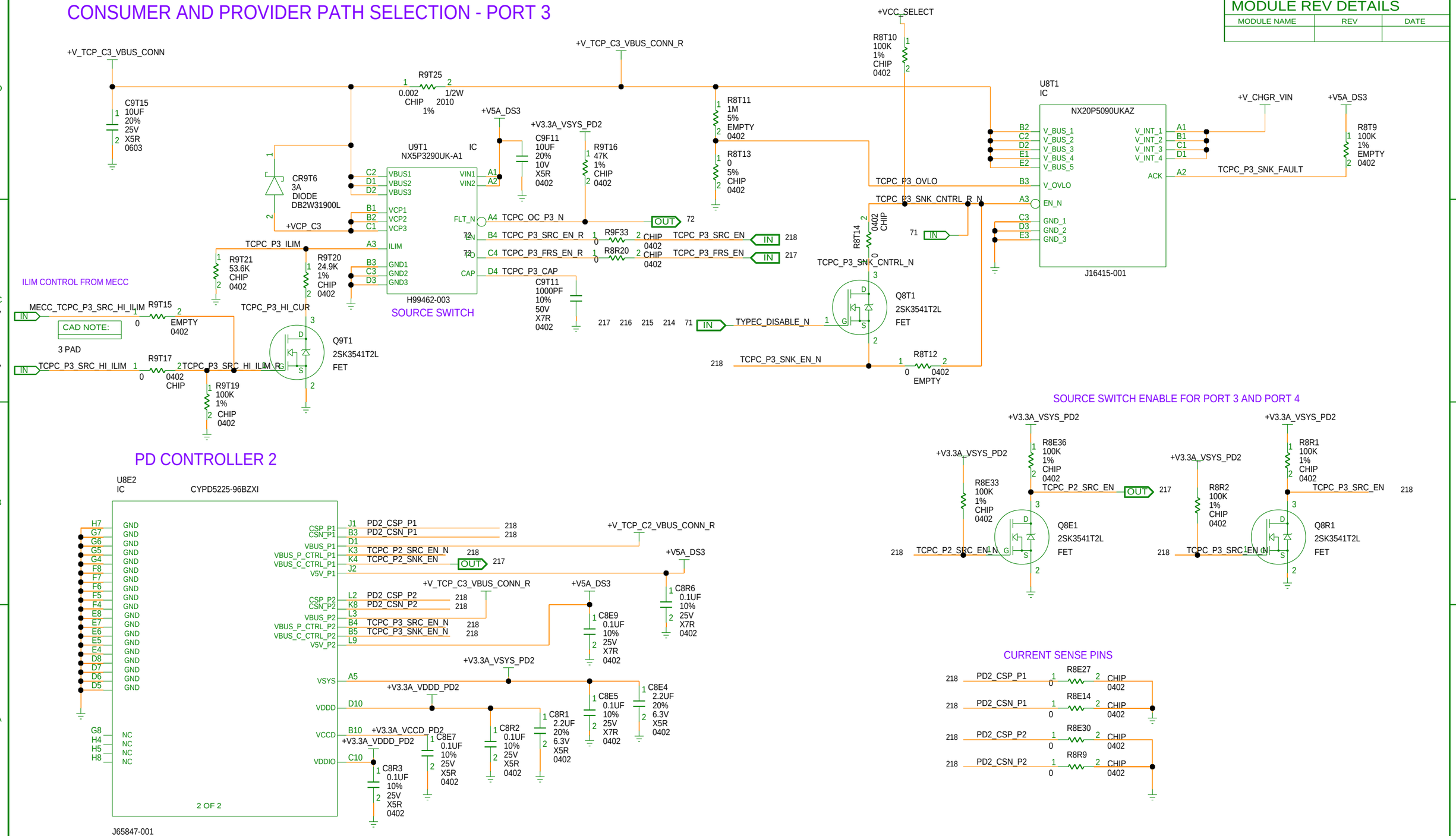
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.217
Wed Dec 18 18:08:51 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	217	1.0

CUSTOM TEXT BPAGE

CONSUMER AND PROVIDER PATH SELECTION - PORT 3

MODULE REV DETAILS		
MODULE NAME	REV	DATE



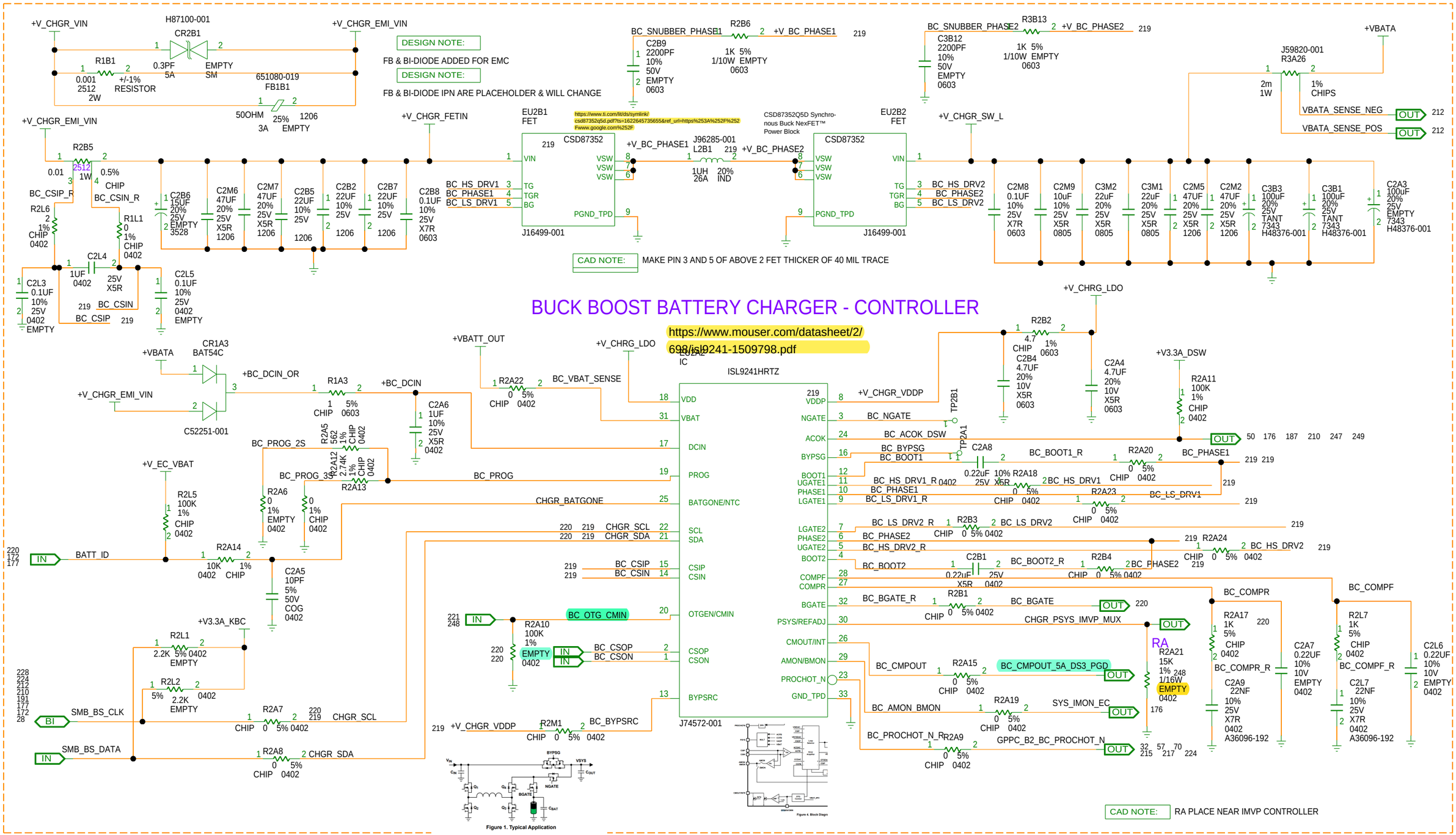
[PAGE_TITLE= CONSUMER AND PROVIDER PATH SELECTION - PORT 3]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.218
Wed Dec 18 18:08:52 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	218	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

BUCK BOOST BATTERY CHARGER - POWER STAGE

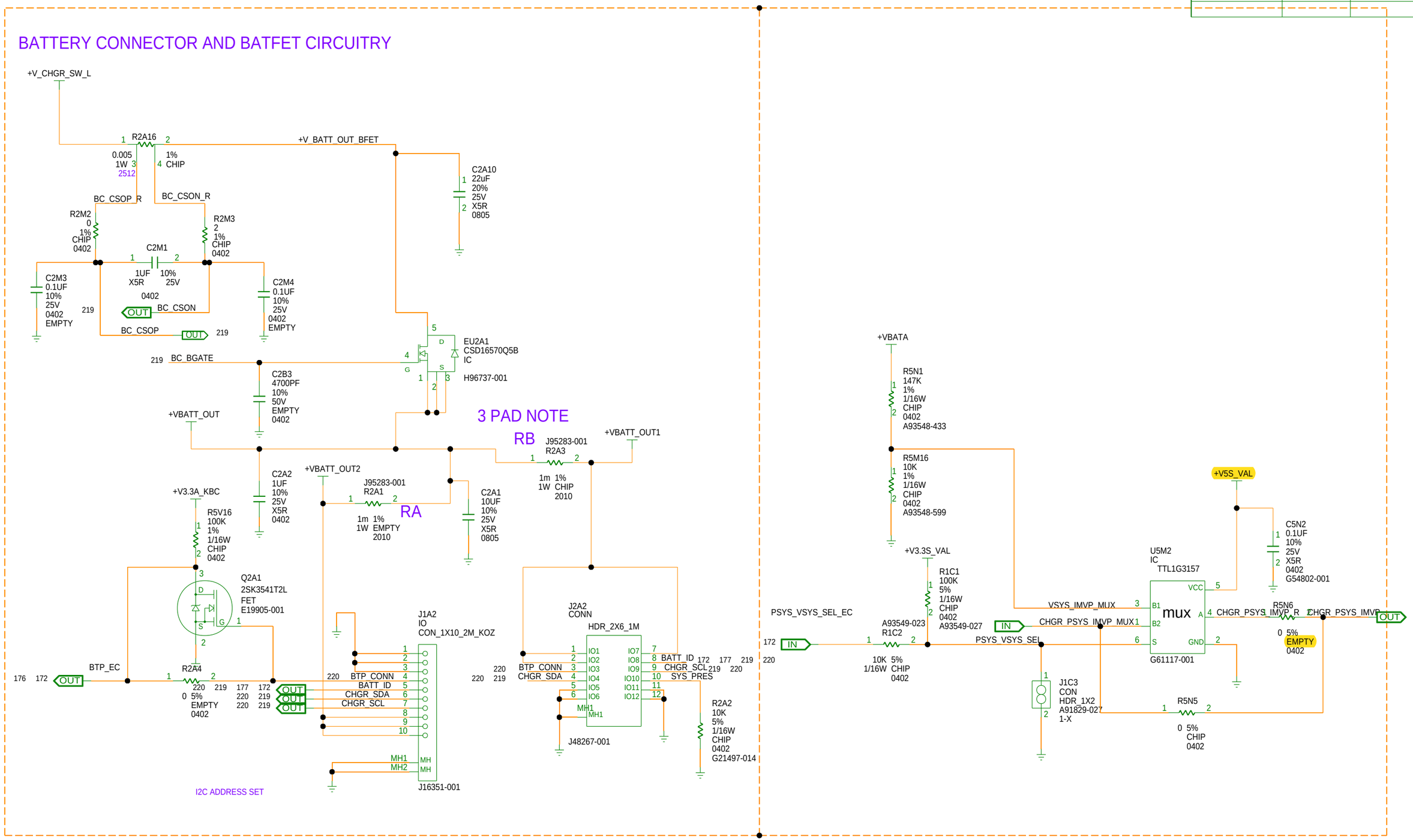


[PAGE_TITLE= BUCK BOOST BATTERY CHARGER - POWER STAGE]

BPAGE DRAWING	INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
tigerlake_u_ddr4.sch_1.219 Tue Sep 03 14:17:26 2013		609003	219	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

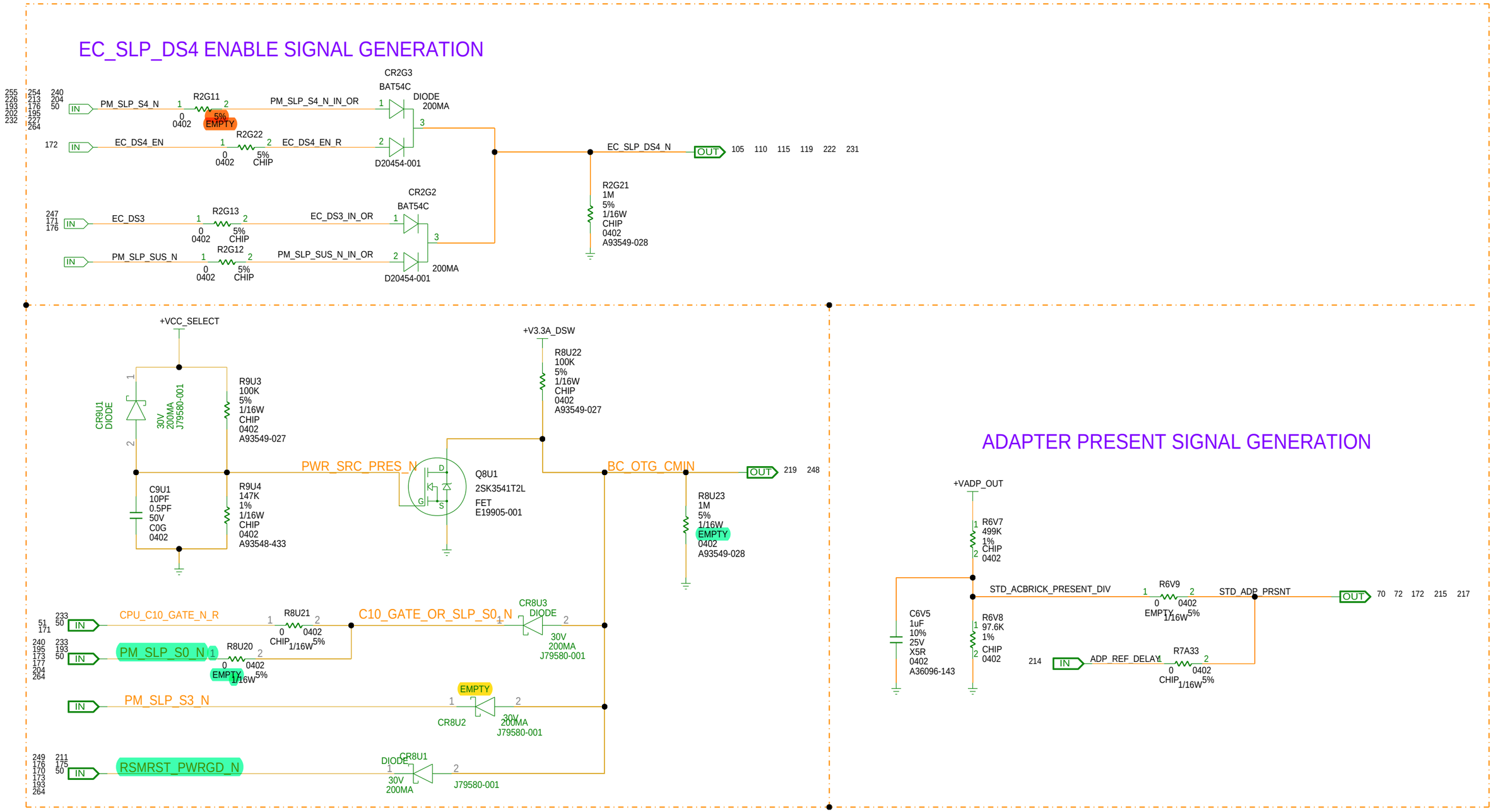


[PAGE_TITLE= BATTERY CONNECTOR, BATFET]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.220
Wed Dec 18 18:08:54 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	220	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= EC_SLP_DS4, KBC_MUX AND ADAPTER PRESENT RAILS - ENABLE GENERATION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.221
Wed Dec 18 18:08:55 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	221	1.0

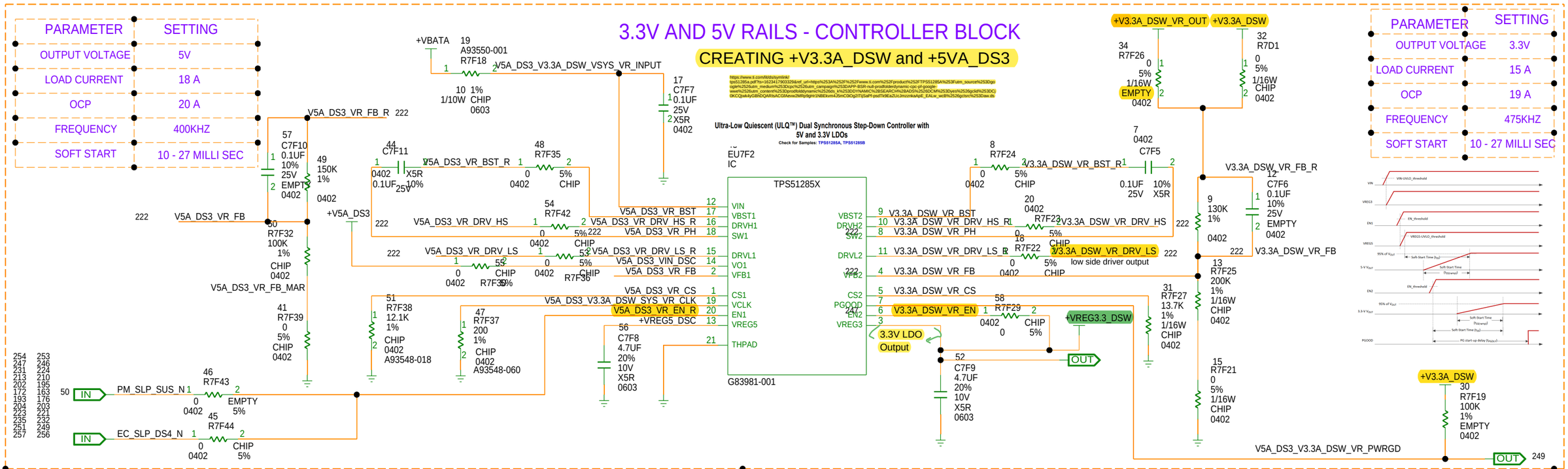
MODULE REV DETAILS		
MODULE NAME	REV	DATE

3.3V AND 5V RAILS - CONTROLLER BLOCK

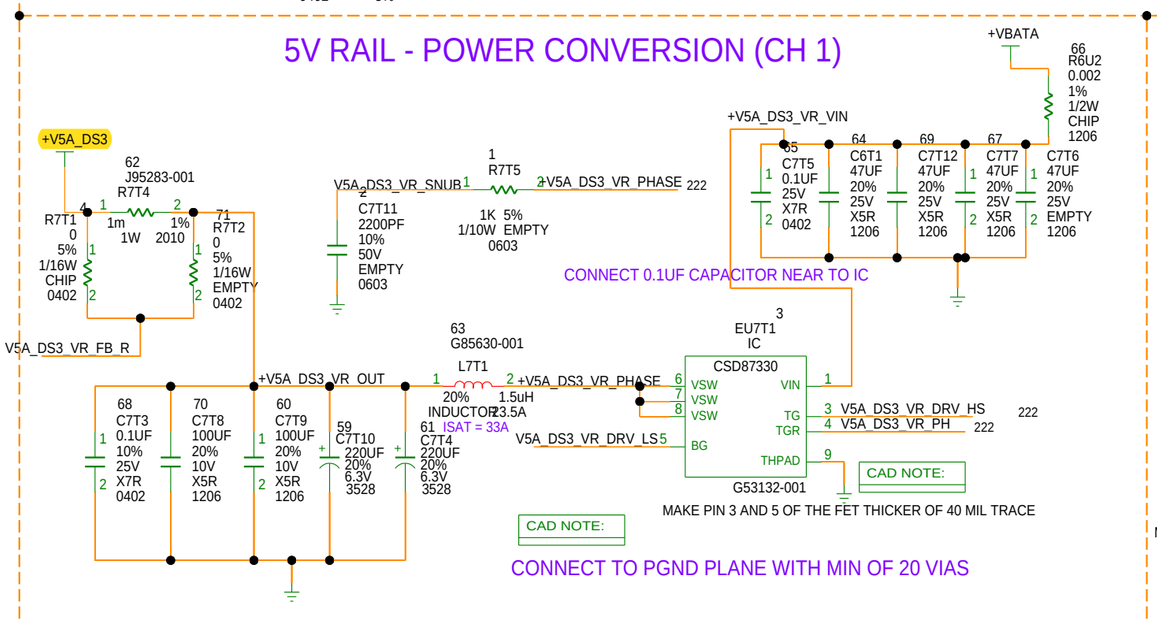
CREATING +V3.3A_DSW and +5VA_DS3

PARAMETER	SETTING
OUTPUT VOLTAGE	5V
LOAD CURRENT	18 A
OCP	20 A
FREQUENCY	400KHZ
SOFT START	10 - 27 MILLI SEC

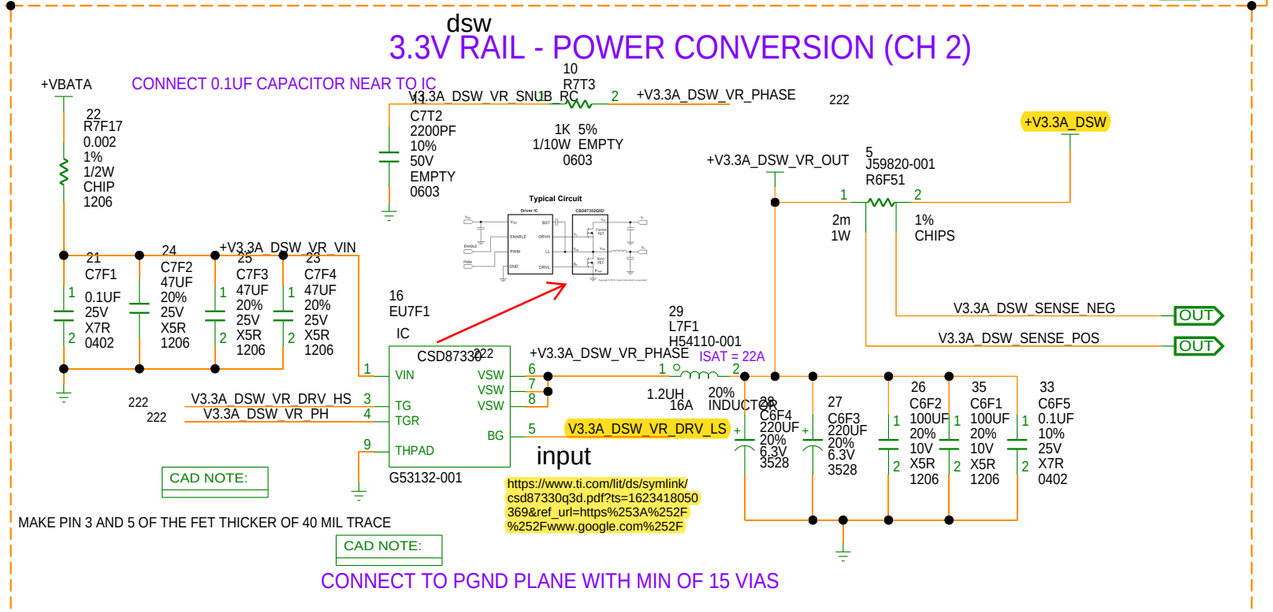
PARAMETER	SETTING
OUTPUT VOLTAGE	3.3V
LOAD CURRENT	15 A
OCP	19 A
FREQUENCY	475KHZ
SOFT START	10 - 27 MILLI SEC



5V RAIL - POWER CONVERSION (CH 1)



dsw 3.3V RAIL - POWER CONVERSION (CH 2)



[PAGE_TITLE= 3.3V AND 5V RAILS - POWER CONVERSION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.222
Tue Sep 03 14:17:26 2013

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	222	1.0

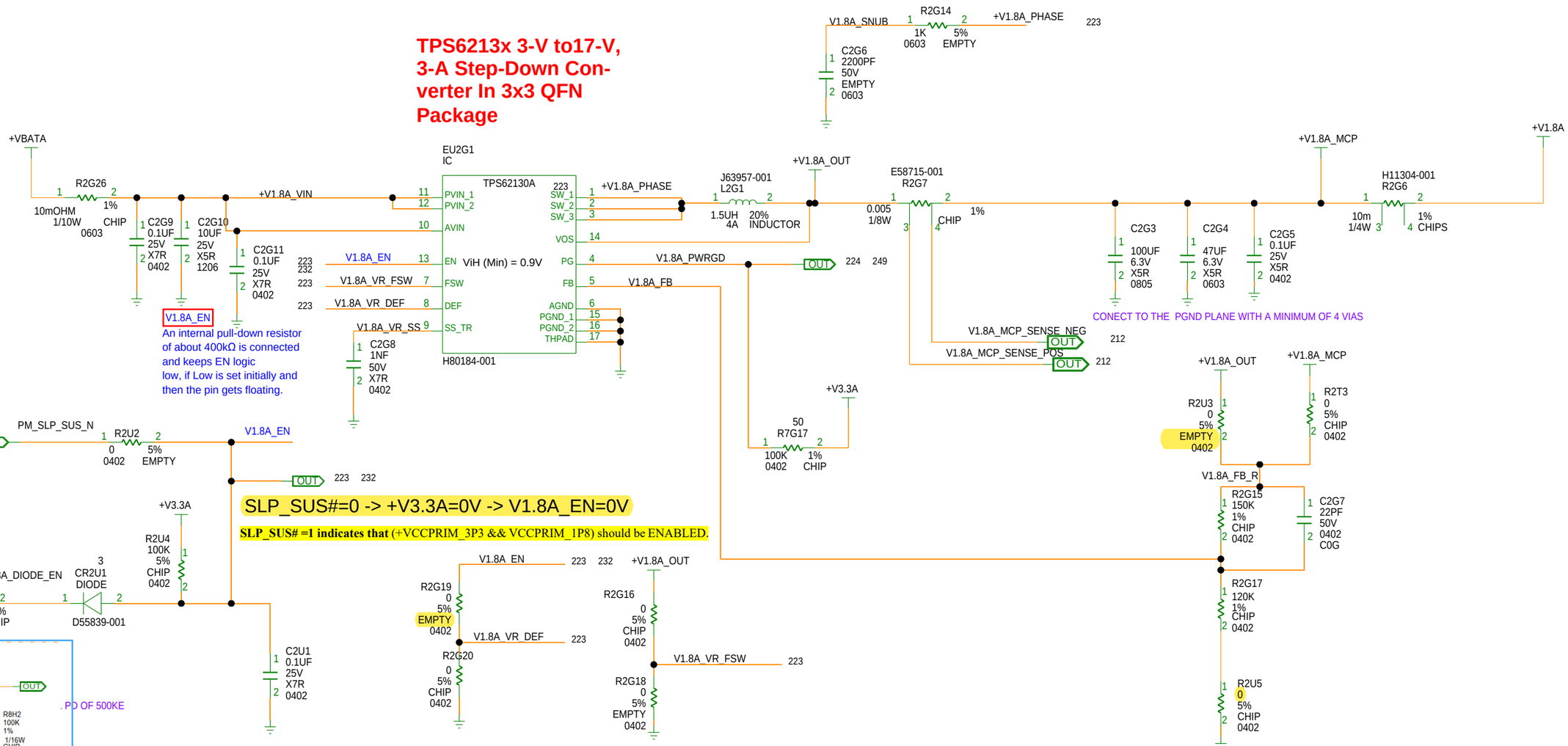
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

V1.8A RAIL POWER CONVERSION

PARAMETER	SETTING
OUTPUT VOLTAGE	1.8V
LOAD CURRENT	3 A
OCP	3.75 A
FREQUENCY	1.25 MHZ
SOFT START	500 U SEC

TPS6213x 3-V to17-V, 3-A Step-Down Converter In 3x3 QFN Package



= V1.8A RAIL POWER CONVERSION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.223
Wed Dec 18 18:08:56 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	223	1.0

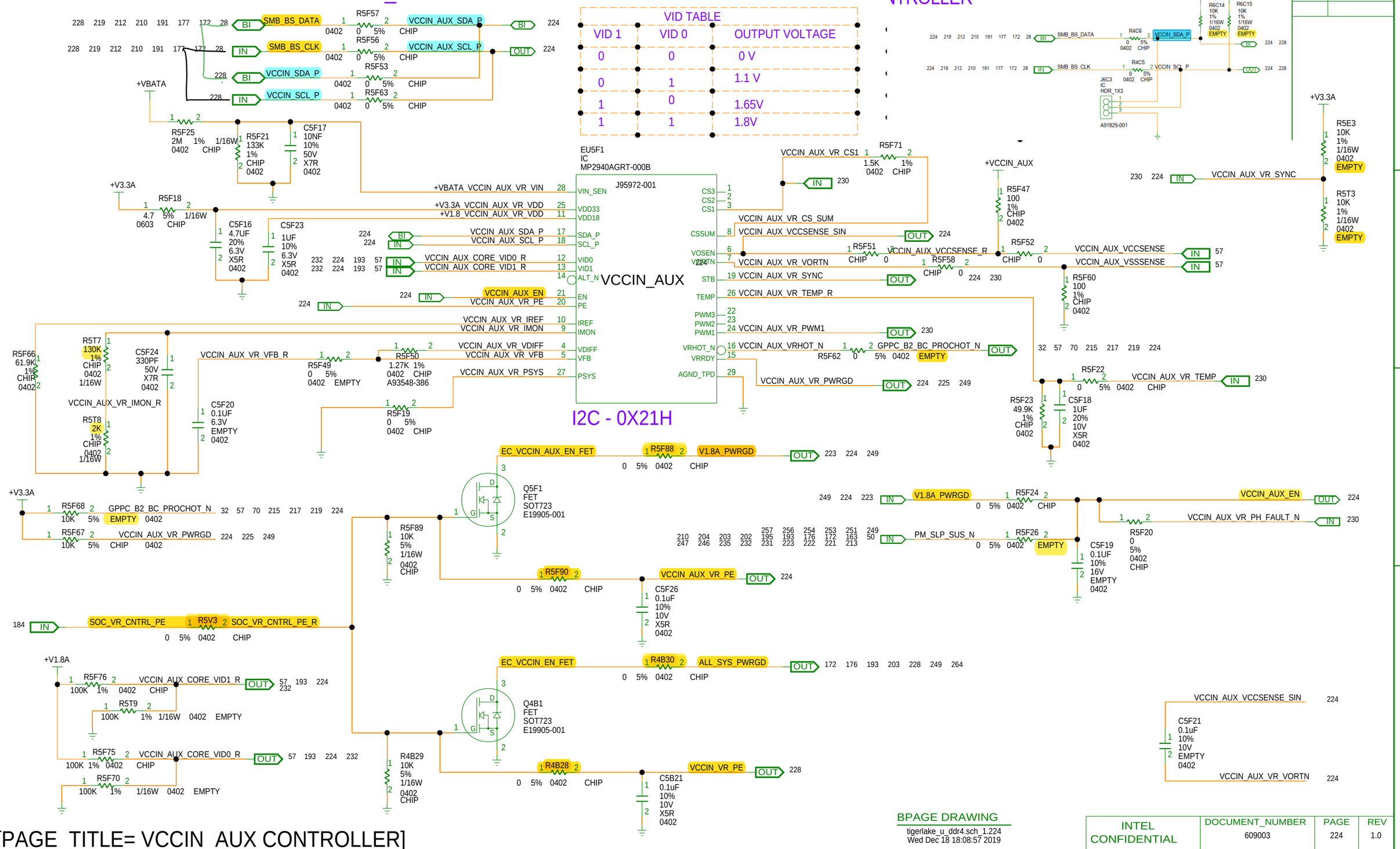
VCCIN_AUX RAIL POWER CONVERSION

VID TABLE

VID 1	VID 0	OUTPUT VOLTAGE
0	0	0 V
0	1	1.1 V
1	0	1.65V
1	1	1.8V

MODULE REV DETAILS

REV	DATE



[PAGE_TITLE= VCCIN_AUX CONTROLLER]

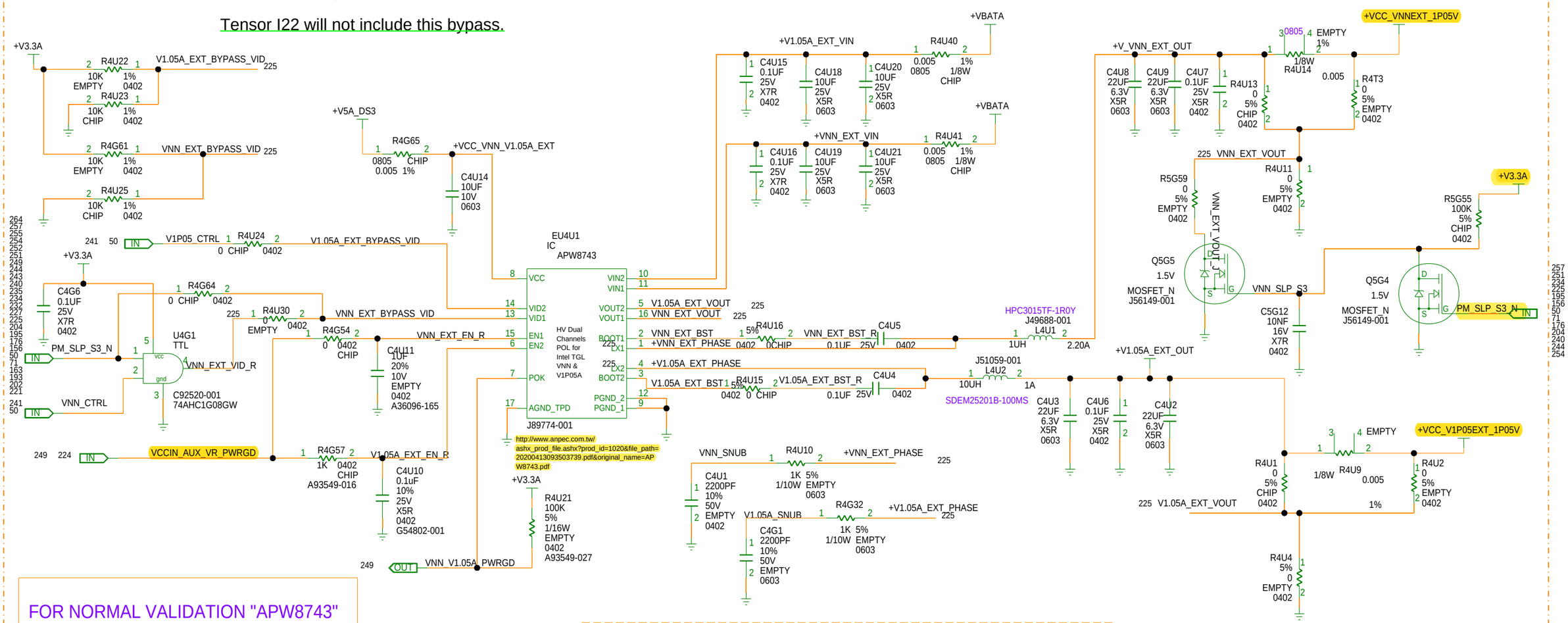
MODULE REV DETAILS		
MODULE NAME	REV	DATE

VNN & V1.05A BYPASS RAIL

Tensor I22 will not include this bypass.

BYPASS RAILS IS PRESENTLY ISLANDS ON ERB

DESIGN NOTE:



FOR NORMAL VALIDATION "APW8743"

3 VID LEVEL TESTING, USE "APW8743A"

VNN

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

PARAMETER	SETTING
OUTPUT VOLTAGE	0.76 V
LOAD CURRENT	0.5 A
OCP	1 A
FREQUENCY	600 KHZ
SOFT START SLEW RATE	10 MILLI V/ USEC

V1.05A

PARAMETER	SETTING
OUTPUT VOLTAGE	1.05 V
LOAD CURRENT	0.5 A
OCP	1.0 A
FREQUENCY	600 KHZ
SOFT START SLEW RATE	10 MILLI V/ USEC

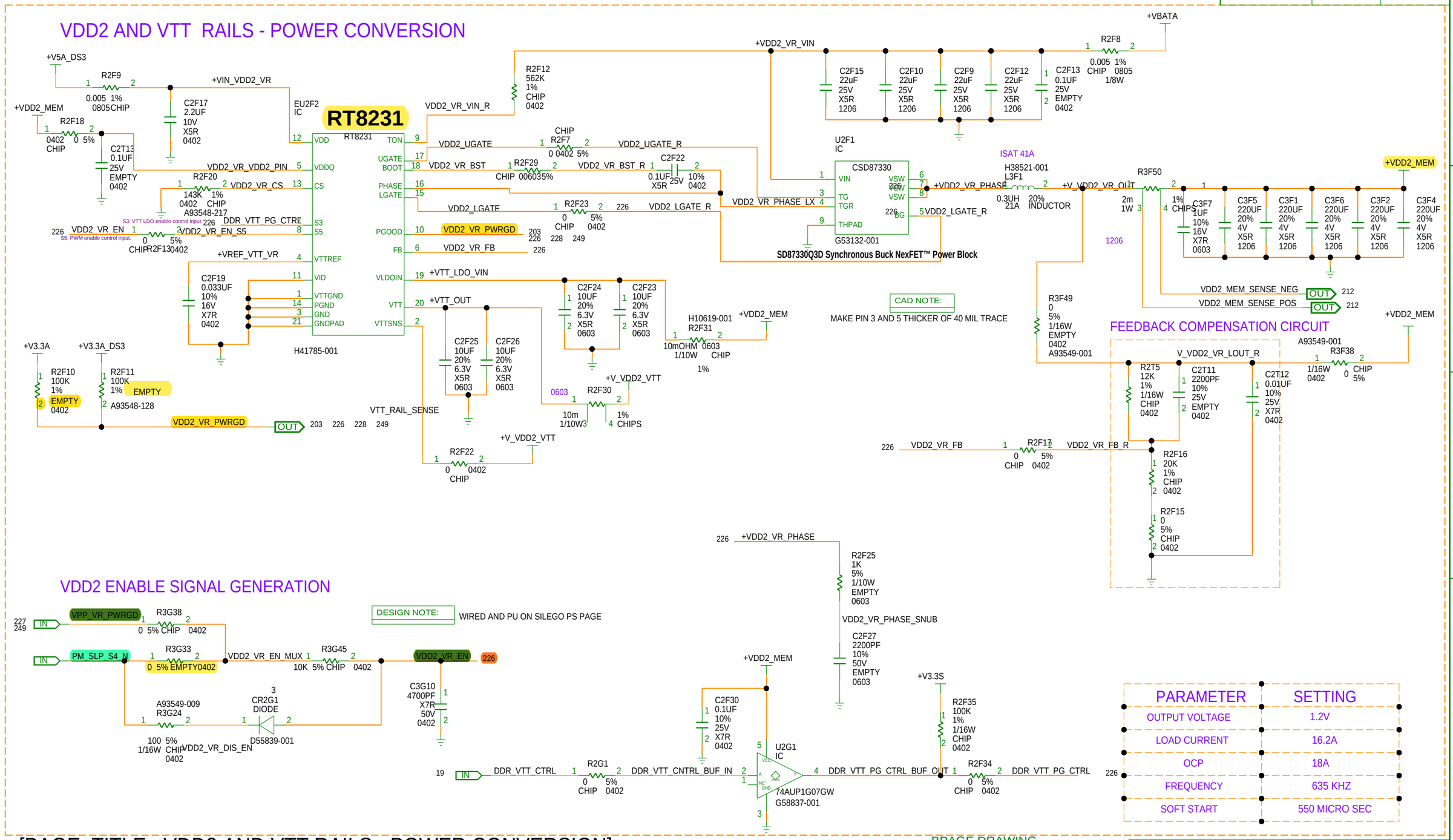
[PAGE_TITLE= VNN & V1.05A BYPASS RAIL - POWER CONVERSION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.225
Wed Dec 18 18:08:58 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	225	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



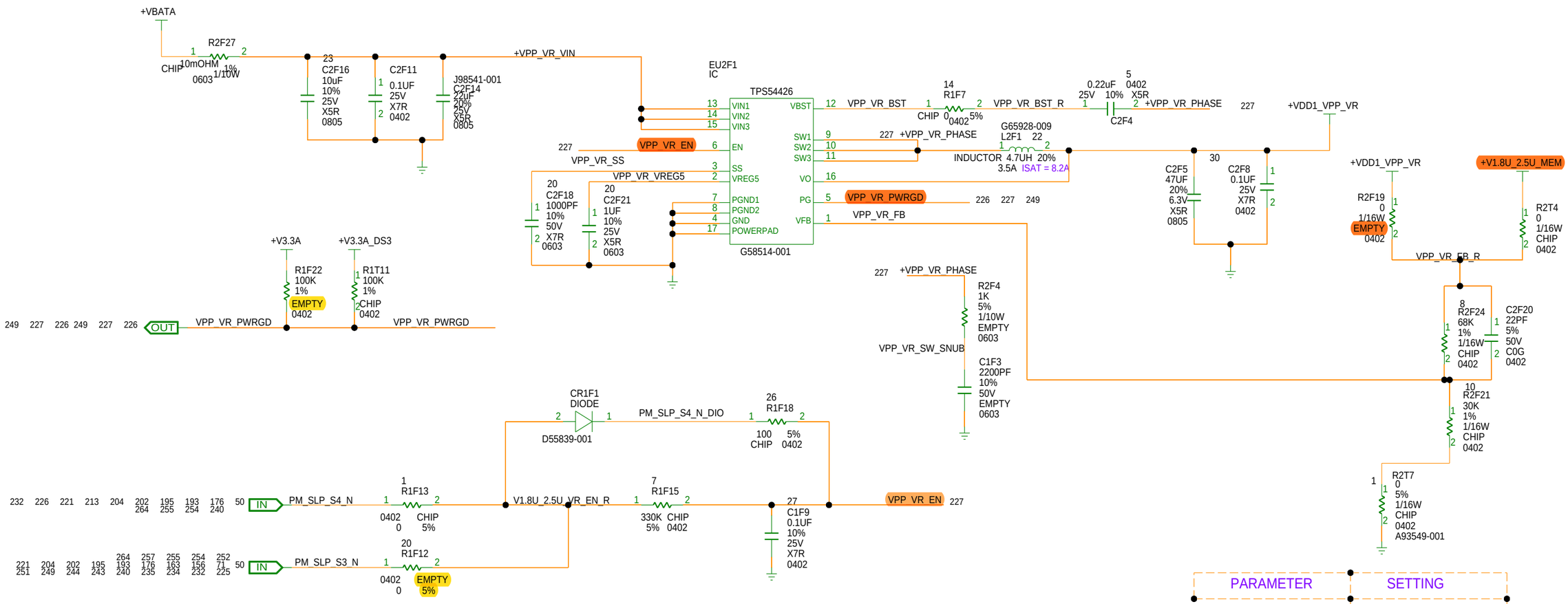
[PAGE_TITLE= VDD2 AND VTT RAILS - POWER CONVERSION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.226
Wed Dec 18 18:08:59 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	226	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

VPP (1.8V / 2.5V) RAIL - POWER CONVERSION



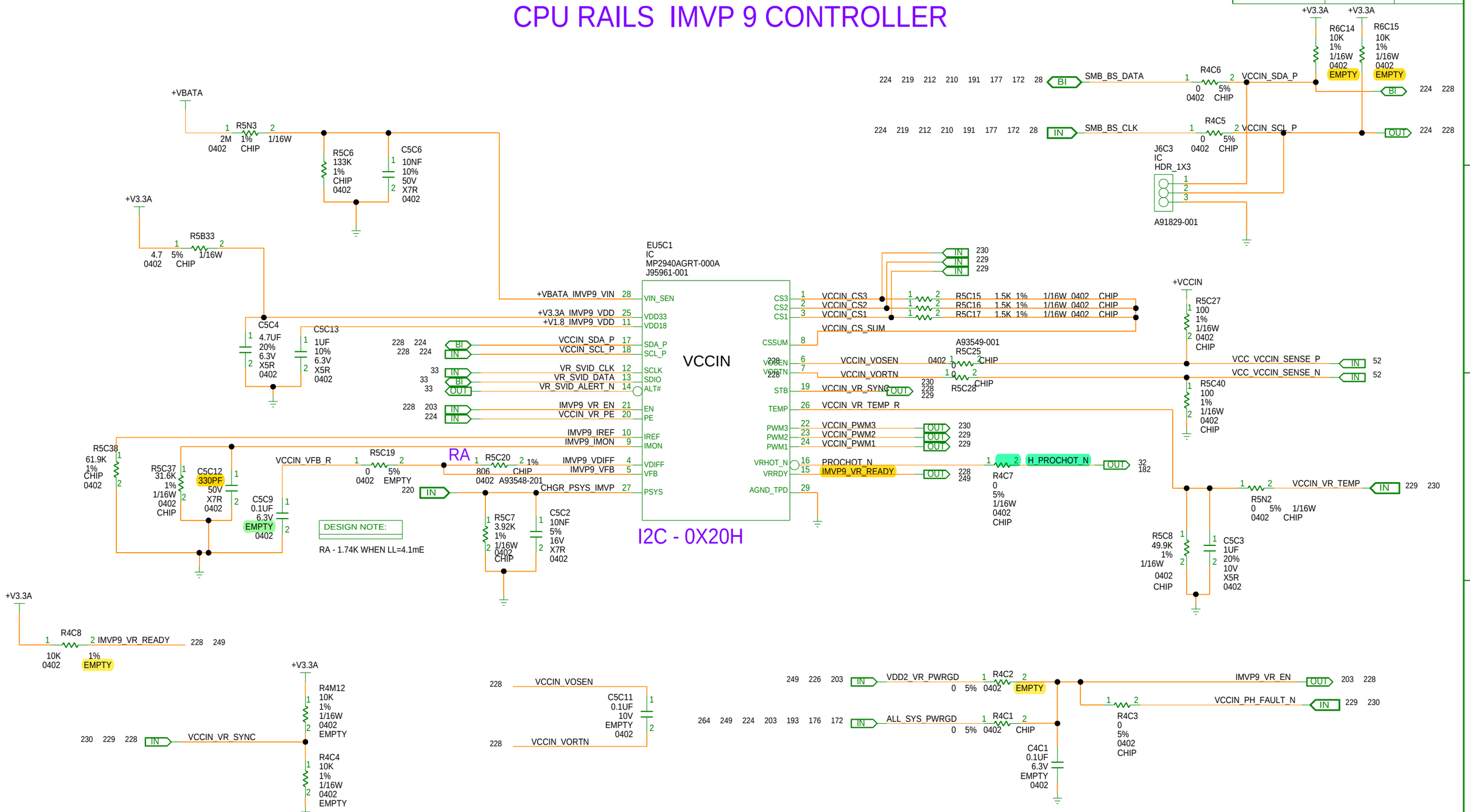
DDR4_DIS_LP4X_EN_N	VR VOLTAGE
HIGH (DEFAULT)	2.5V (DDR4)
LOW	1.8V (LP4/LP4X)

PARAMETER	SETTING
OUTPUT VOLTAGE	2.5V
LOAD CURRENT	1A
OCP	4.5A
FREQUENCY	700 KHZ
SOFT START	227 MICRO SEC

[PAGE_TITLE= VPP (1.8V / 2.5V) RAIL - POWER CONVERSION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.227
Wed Dec 18 18:09:00 2019

CPU RAILS IMVP 9 CONTROLLER



MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE= VCCIN_IMVP9 CONTROLLER]

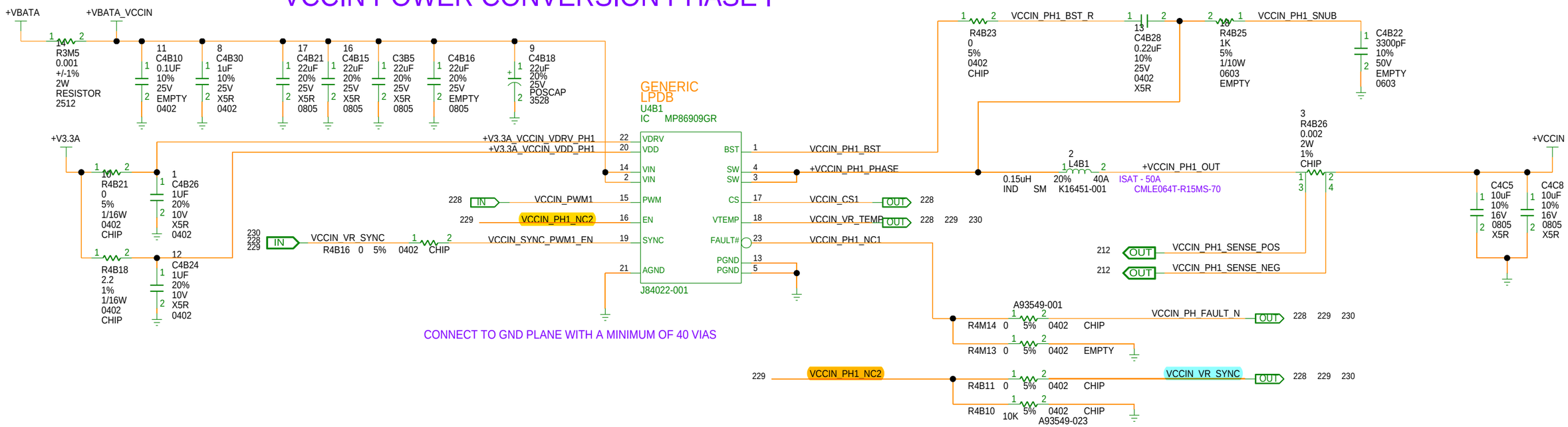
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.228
Wed Dec 18 18:09:01 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	228	1.0

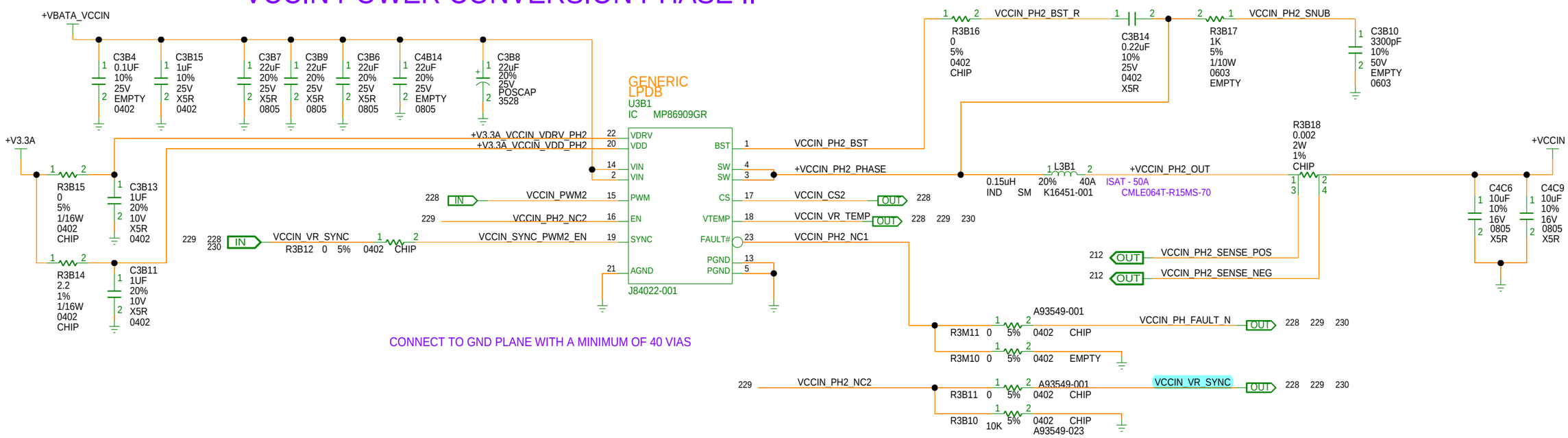
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

VCCIN POWER CONVERSION PHASE I



VCCIN POWER CONVERSION PHASE II



[PAGE_TITLE= VCCIN_IMVP9- POWER CONVERSION]

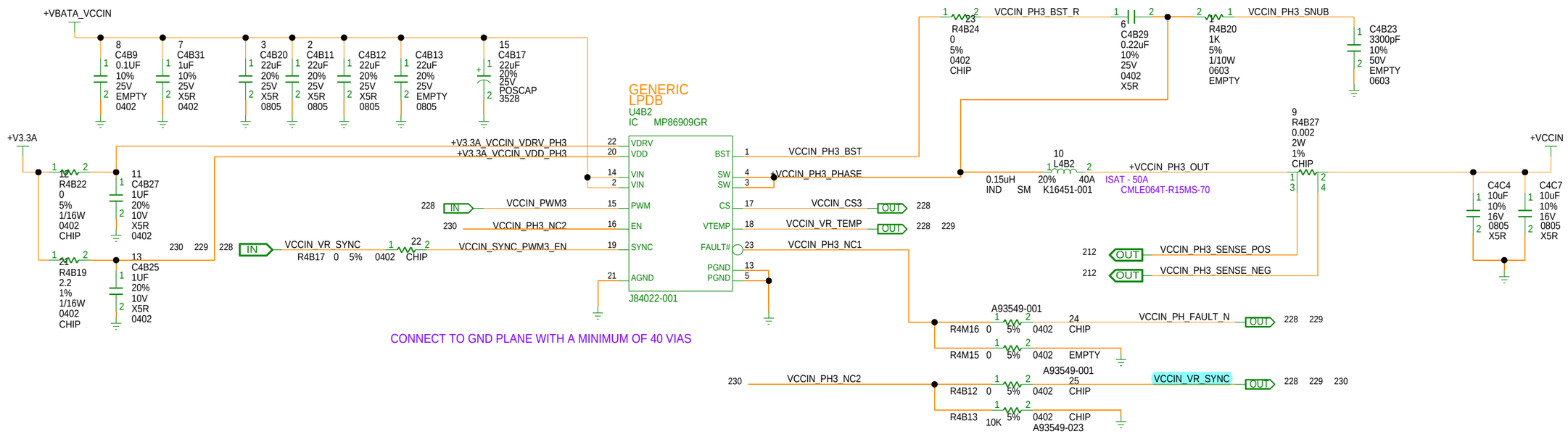
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.229
Wed Dec 18 18:09:02 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	229	1.0

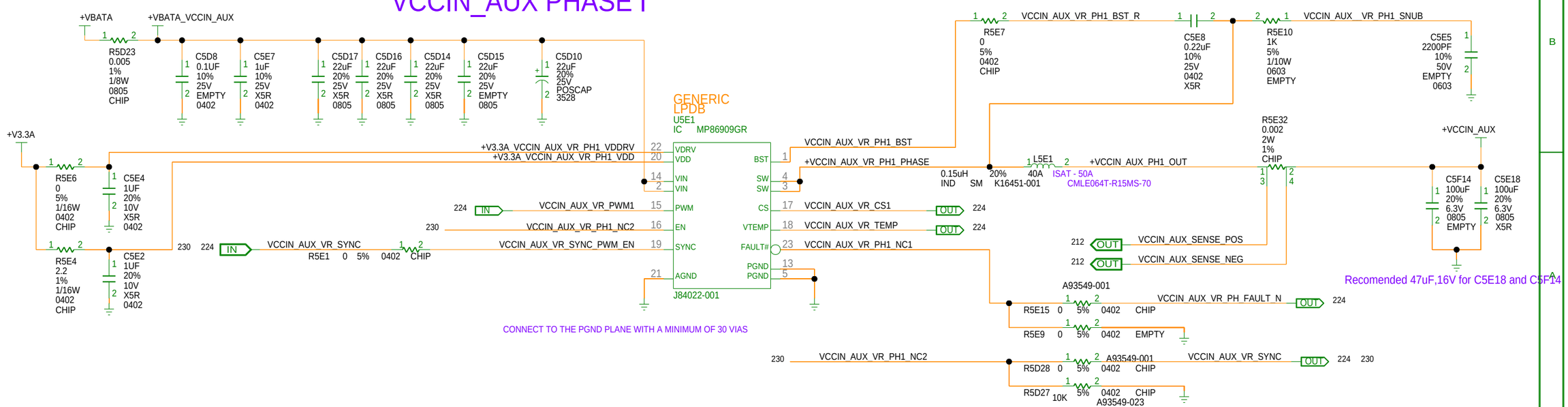
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

VCCIN POWER CONVERSION PHASE III



VCCIN_AUX PHASE I



[PAGE_TITLE= VCCIN_IMVP9 - POWER CONVERSION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.230
Wed Dec 18 18:09:02 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	230	1.0

CUSTOM TEXT BPAGE

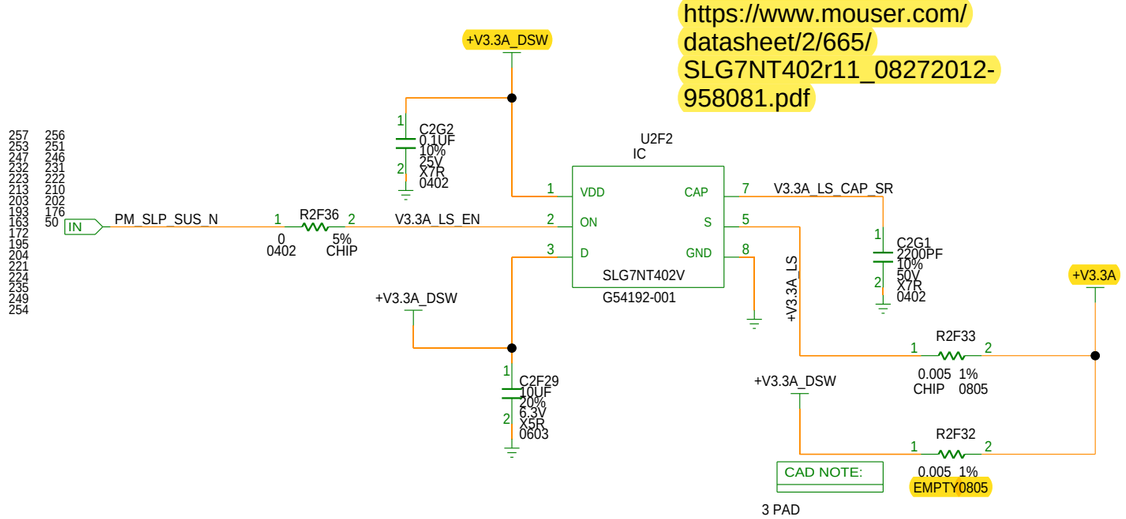
230 1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

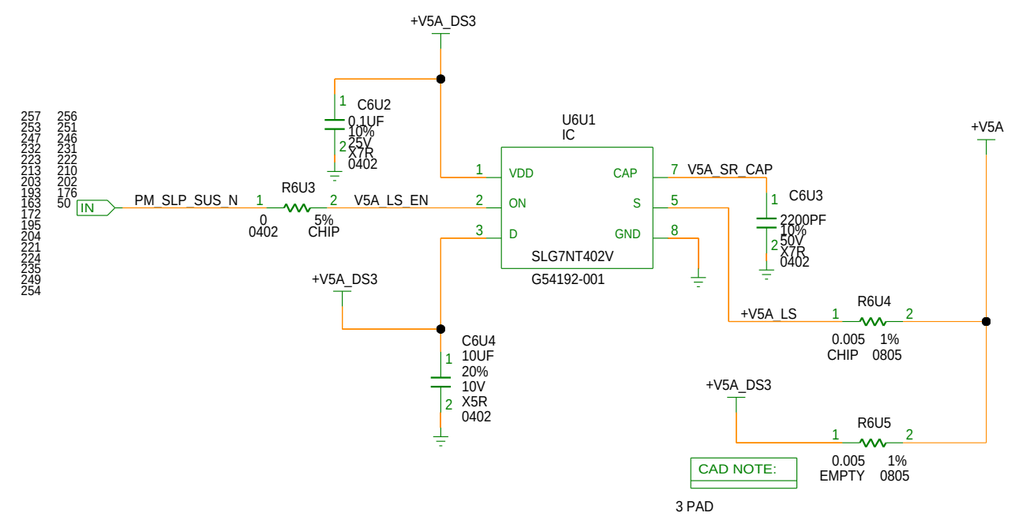
V3.3A RAIL GENERATION

Ultra-small 7.8 mΩ
4 A Load Switch with Dis-
charge

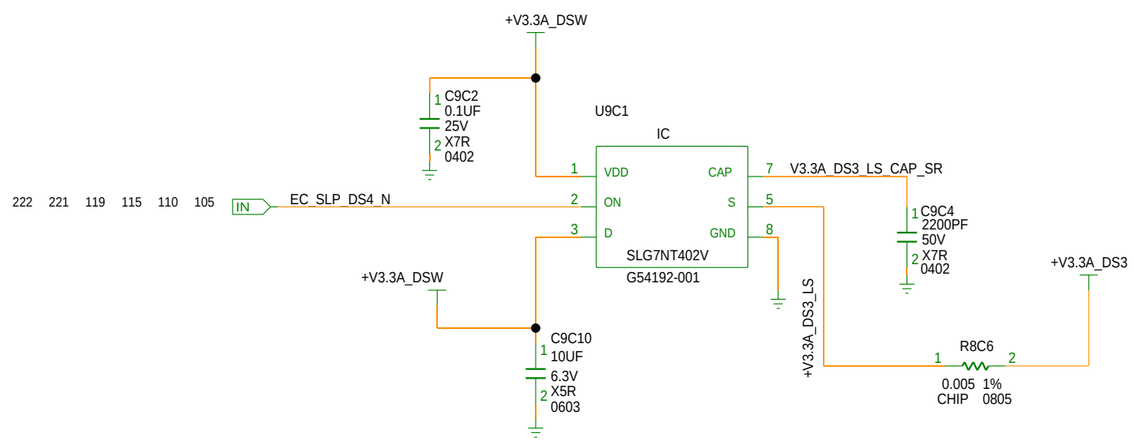
https://www.mouser.com/
datasheet/2/665/
SLG7NT402r11_08272012-
958081.pdf



V5A RAIL GENERATION



V3.3A_DS3 RAIL GENERATION



[PAGE_TITLE= A RAILS POWER GENERATION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.231
Wed Dec 18 18:09:03 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	231	1.0

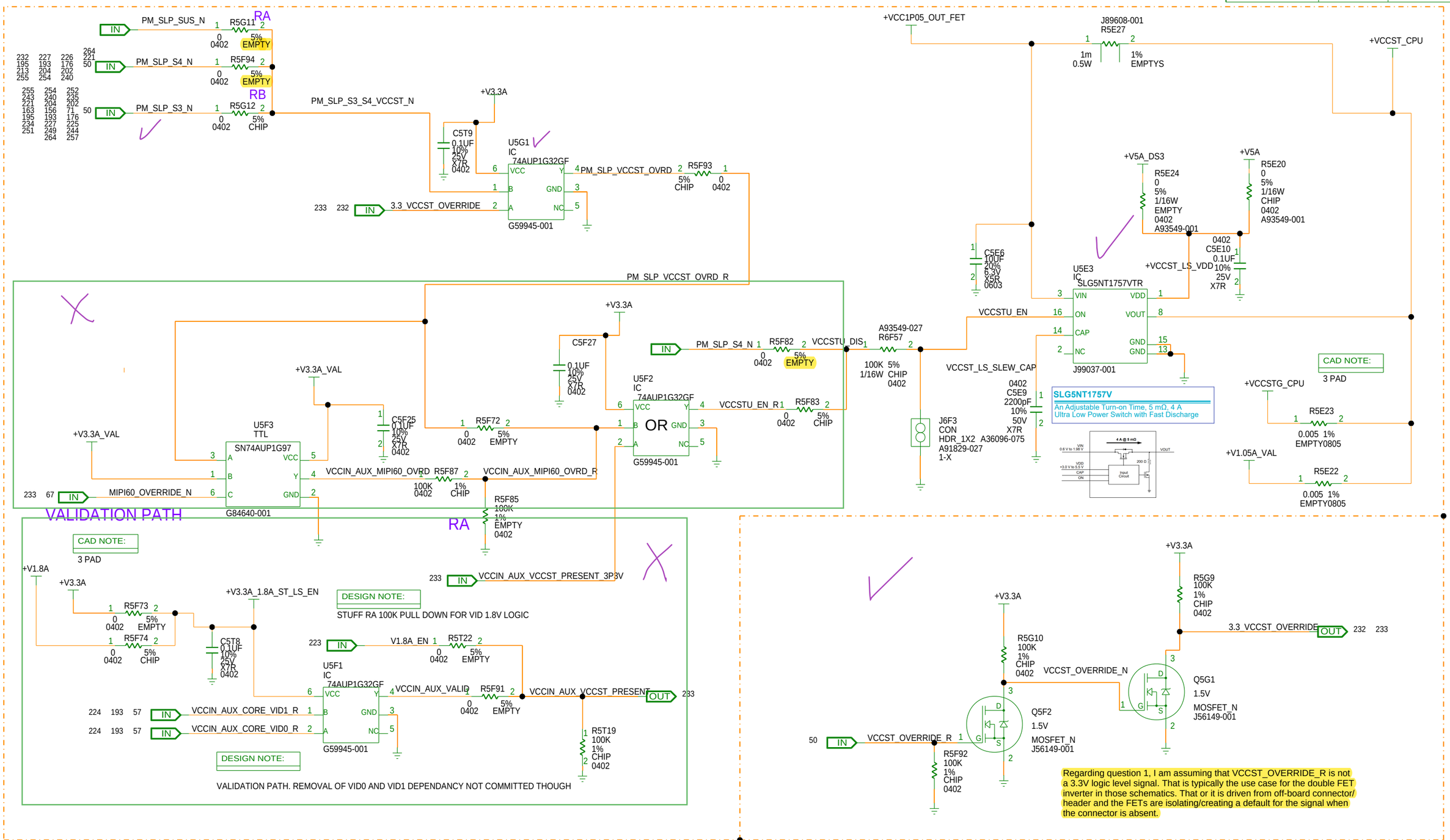
VCCST, VCCSFR, DS3 AND LAN RAILS POWER GENERATI

CR-232 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE2

V1.05A (internal rail in PCH FIVR)						
VCCST	SLP_S3#	PCH FIVR		VCCST	1.050 V	0.50 A
VccSTG	CPU_C10_GATE#	PCH FIVR		VCCSTG	1.050 V	0.30 A

MODULE REV DETAILS		
MODULE NAME	REV	DATE

V1.05U_CPU, VCCST_CPU AND VCCSFR GENERATION



[PAGE_TITLE= VCCST AND LAN RAILS POWER GENERATION]

wtm2_icrb.sch_1.225
Wed Dec 18 18:09:04 2019

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.232

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	232	1.0

CUSTOM TEXT BPAGE

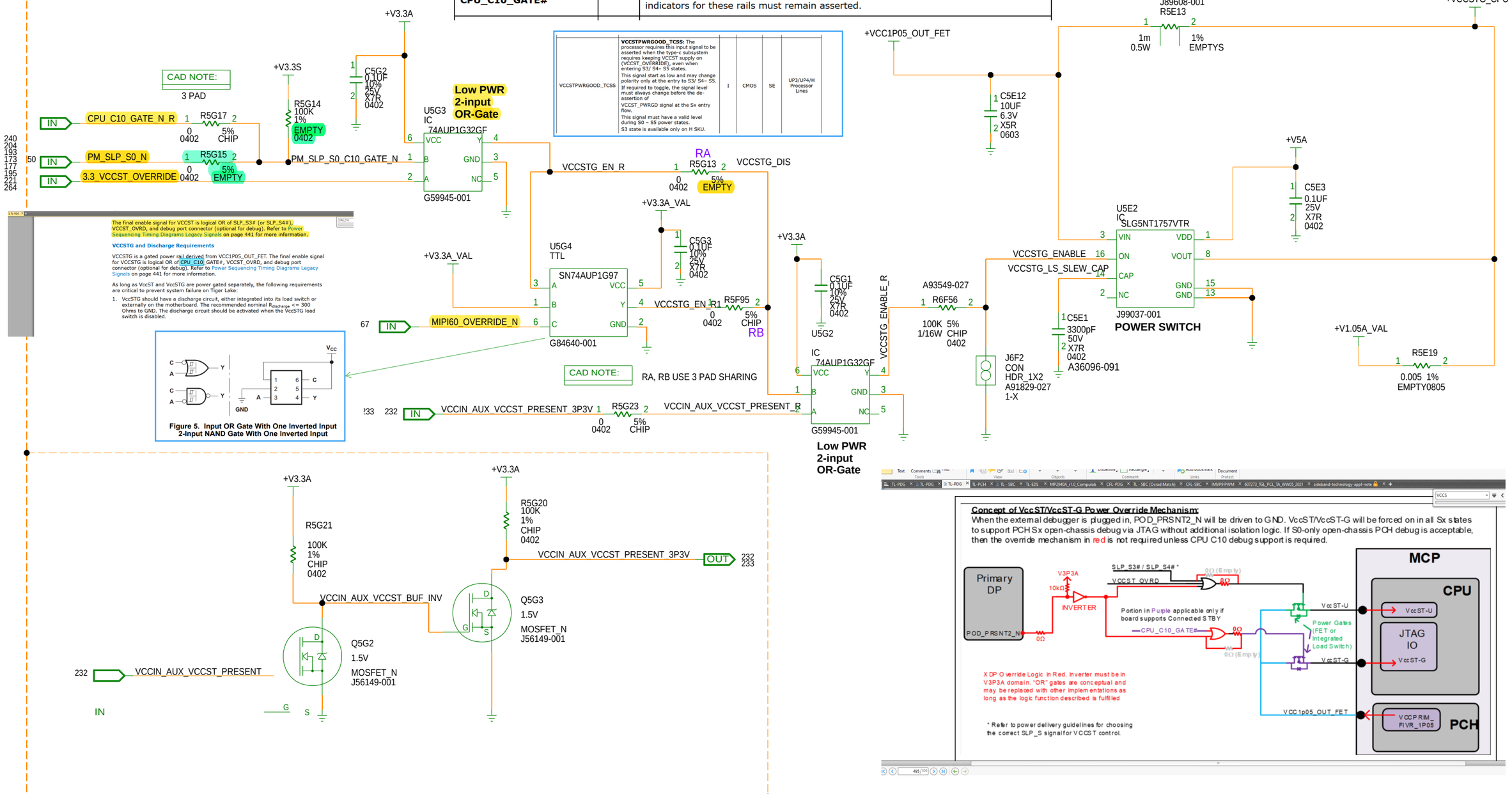
Name	Type	Description
VCCST_OVERRIDE	O	**VccST Override**: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWRGOOD_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

MODULE REV DETAILS		
MODULE NAME	REV	DATE

+VCCSTG RAIL GENERATION

Name	Type	Description
GPP_H18 / **CPU_C10_GATE#**	O	**External Power Gate**: Control for VCCIO, VCCSTG and VCCPLL_OC during C10. When asserted, VCCIO, VCCSTG and VCCPLL_OC can be 0 V, however the power good indicators for these rails must remain asserted.

VCCSTPWRGOOD_TCSS	**VCCSTPWRGOOD_TCSS:** The processor requires this input signal to be asserted when the type-c subsystem requires keeping VCCST supply on (VCCST_OVERRIDE), even when entering S3/ S4– S5 states. This signal start as low and may change polarity only at the entry to S3/ S4– S5. If required to toggle, the signal level must always change before the de-assertion of VCCST_PWRGD signal at the Sx entry flow. This signal must have a valid level during S0 – S5 power states. S3 state is available only on H SKU.	I	CMOS	SE	UP3/UP4/H Processor Lines



The final enable signal for VCCST is logical OR of SLP_S3# (or SLP_S4#), VCCST_OVRD, and debug port connector (optional for debug). Refer to Power Sequencing Timing Diagrams Legacy Signals on page 441 for more information.

VCCSTG and Discharge Requirements

VCCSTG is a gated power rail derived from VCC1P05_OUT_FET. The final enable signal for VCCSTG is logical OR of CPU_C10_GATE#, VCCST_OVRD, and debug port connector (optional for debug). Refer to Power Sequencing Timing Diagrams Legacy Signals on page 441 for more information.

As long as VccST and VccSTG are power gated separately, the following requirements are critical to prevent system failure on Tiger Lake:

1. VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal $R_{discharge}$ <= 300 Ohms to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.

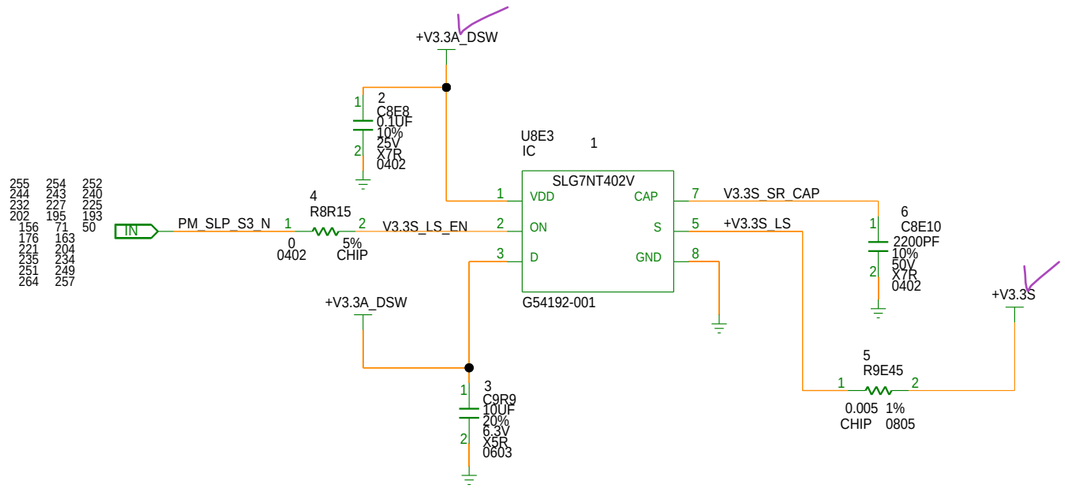
[PAGE_TITLE= VCCSTG AND VCCSFR_OC RAIL GENERATION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.233
Wed Dec 18 18:09:05 2019

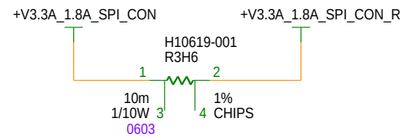
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	233	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

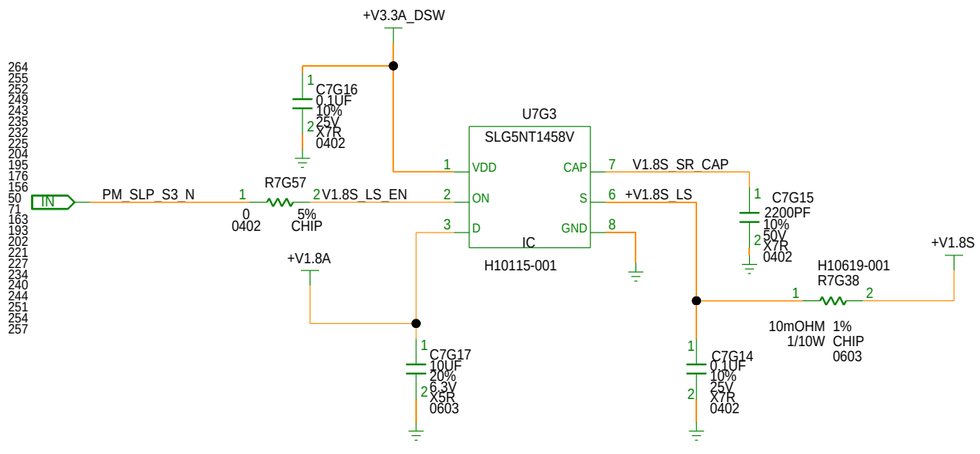
+V3.3S POWER GENERATION



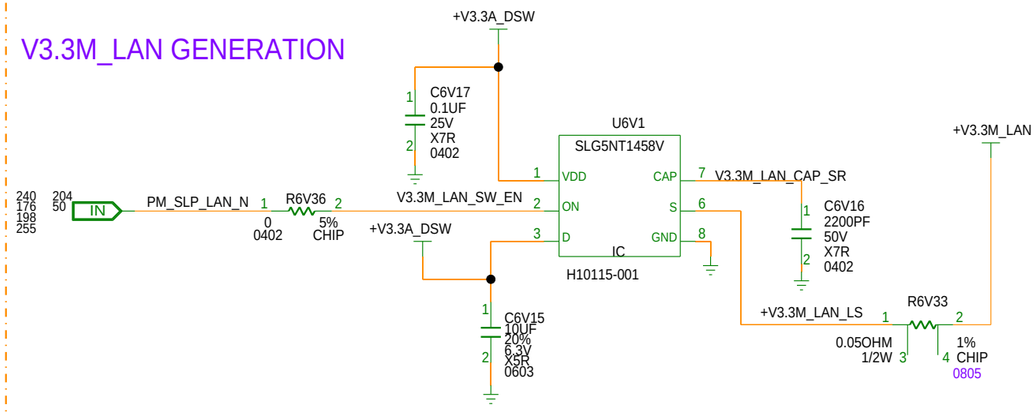
SPI RAIL POWER GENERATION



+V1.8S POWER GENERATION



V3.3M_LAN GENERATION



[PAGE_TITLE= 3.3S AND 1.8S RAIL GENERATION]

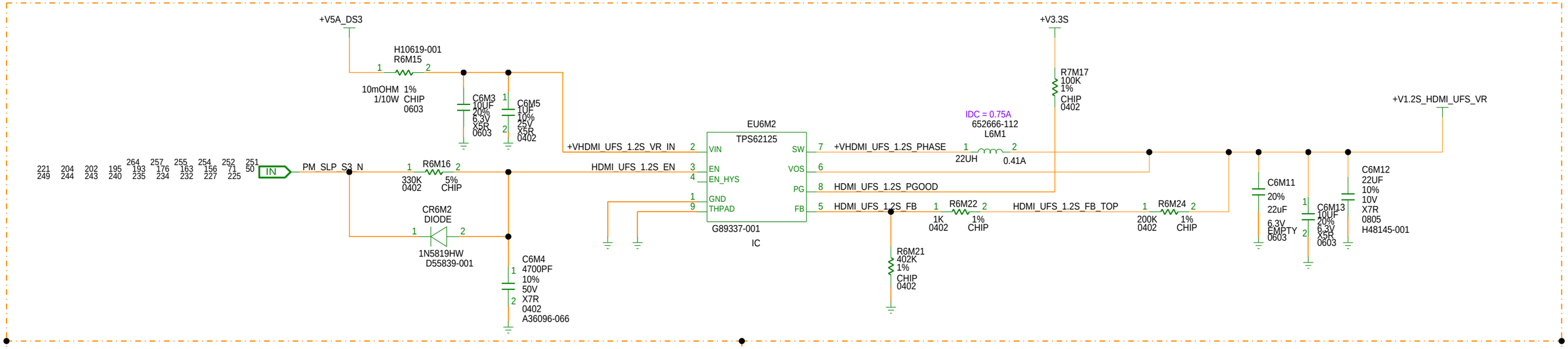
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.234
Wed Dec 18 18:09:06 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	234	1.0

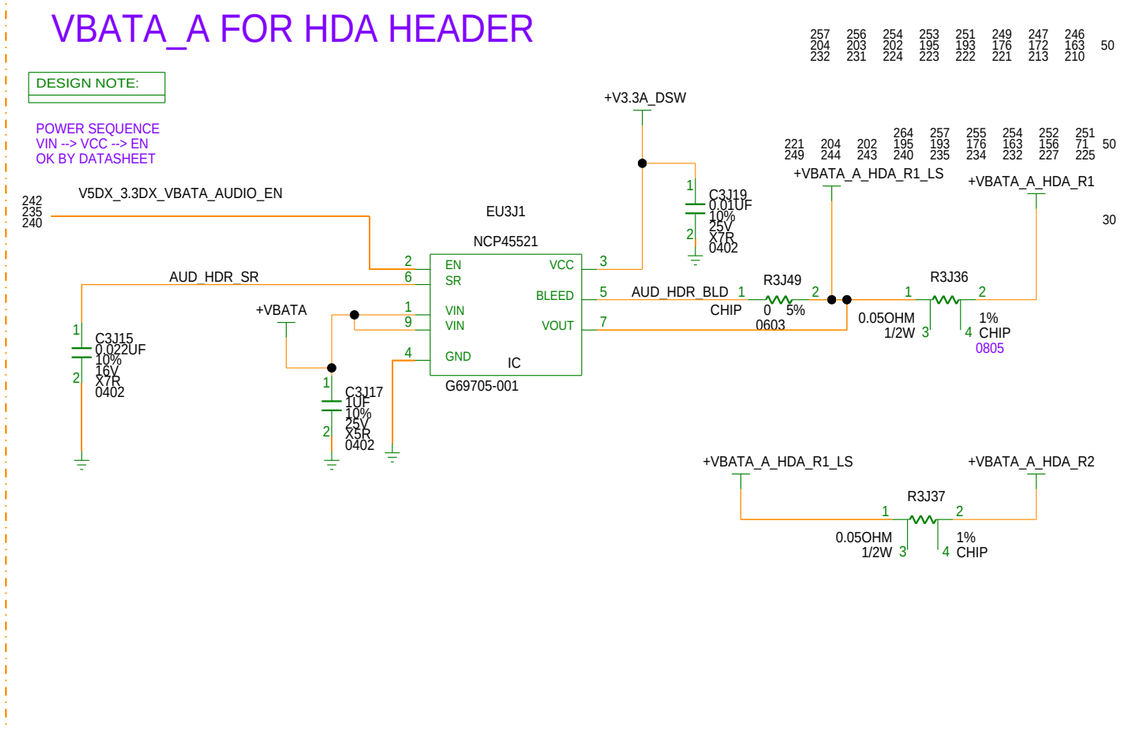
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

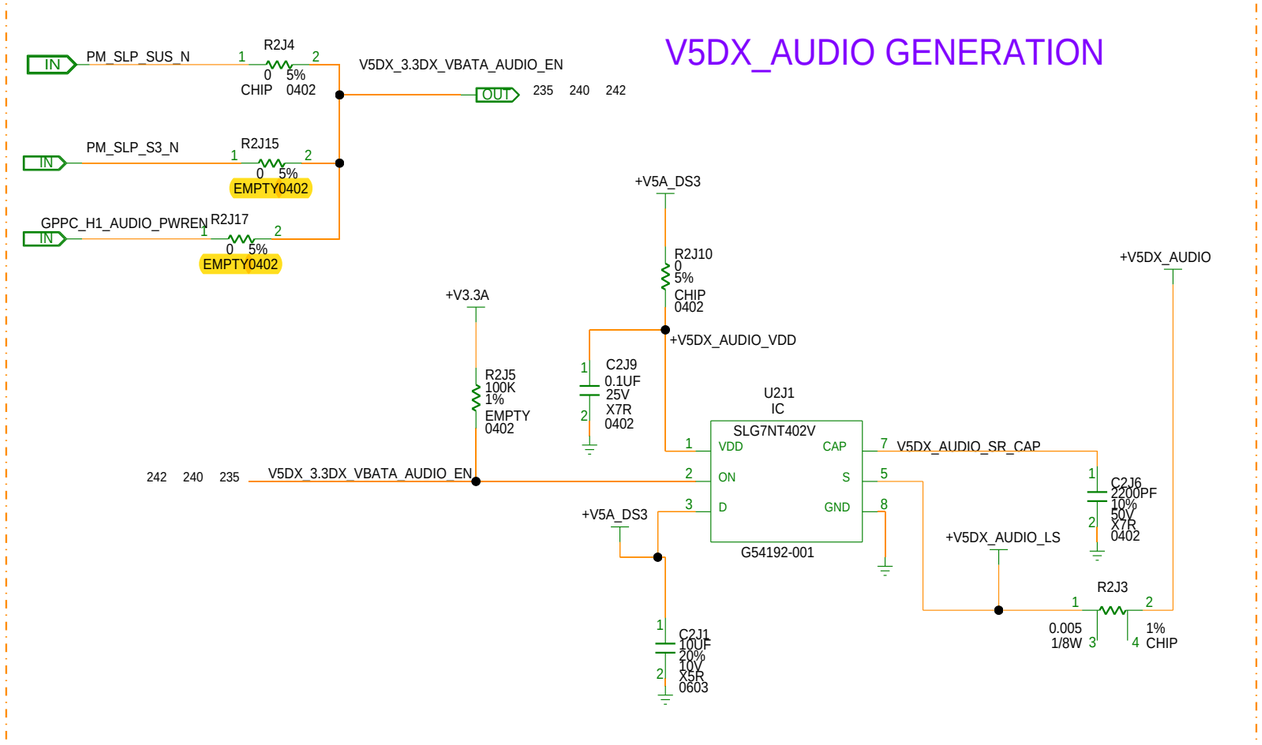
1.2V RAIL FOR HDMI AND UFS - POWER CONVERSION



VBATA_A FOR HDA HEADER



V5DX_AUDIO GENERATION



[PAGE_TITLE= 1.2V RAIL FOR HDMI AND UFS, VBATA_A FOR HDA AND AUDIO POWER GENERATION]

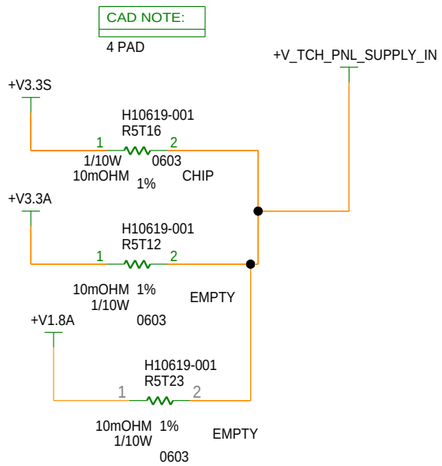
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.235
Wed Dec 18 18:09:07 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	235	1.0

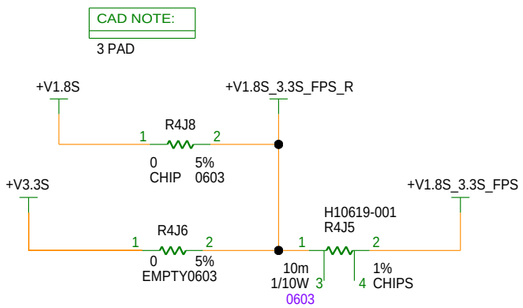
CUSTOM TEXT BPAGE

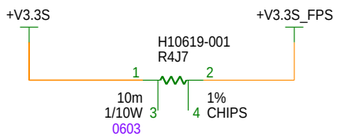
MODULE REV DETAILS		
MODULE NAME	REV	DATE

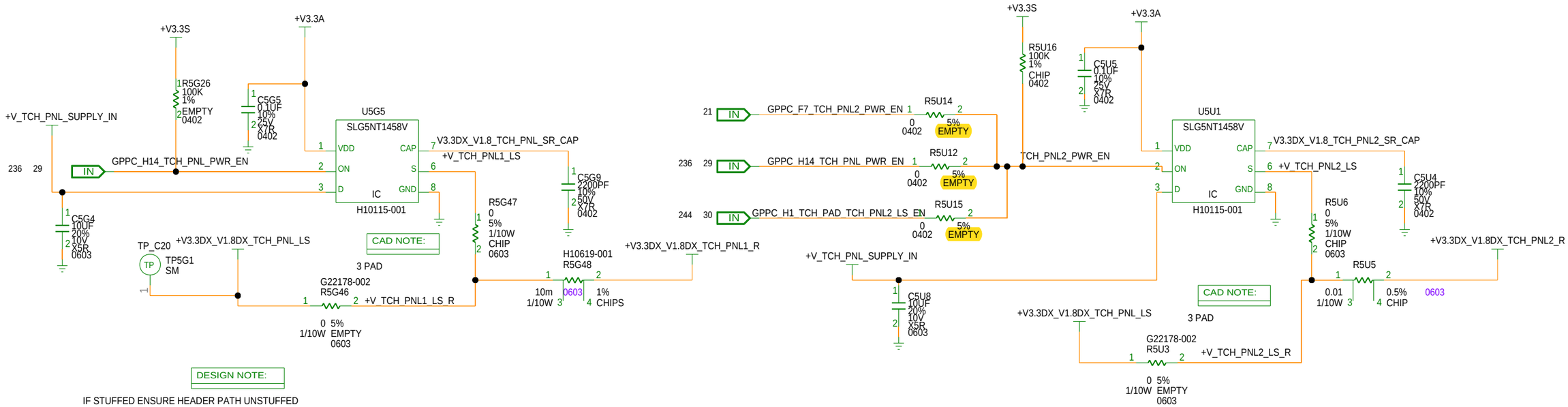
TOUCH PANEL POWER SUPPLY GENERATION



FINGER PRINT POWER SUPPLY GENERATION







[PAGE_TITLE= TOUCH PANEL AND FINGER PRINT POWER SUPPLY GENERATION]

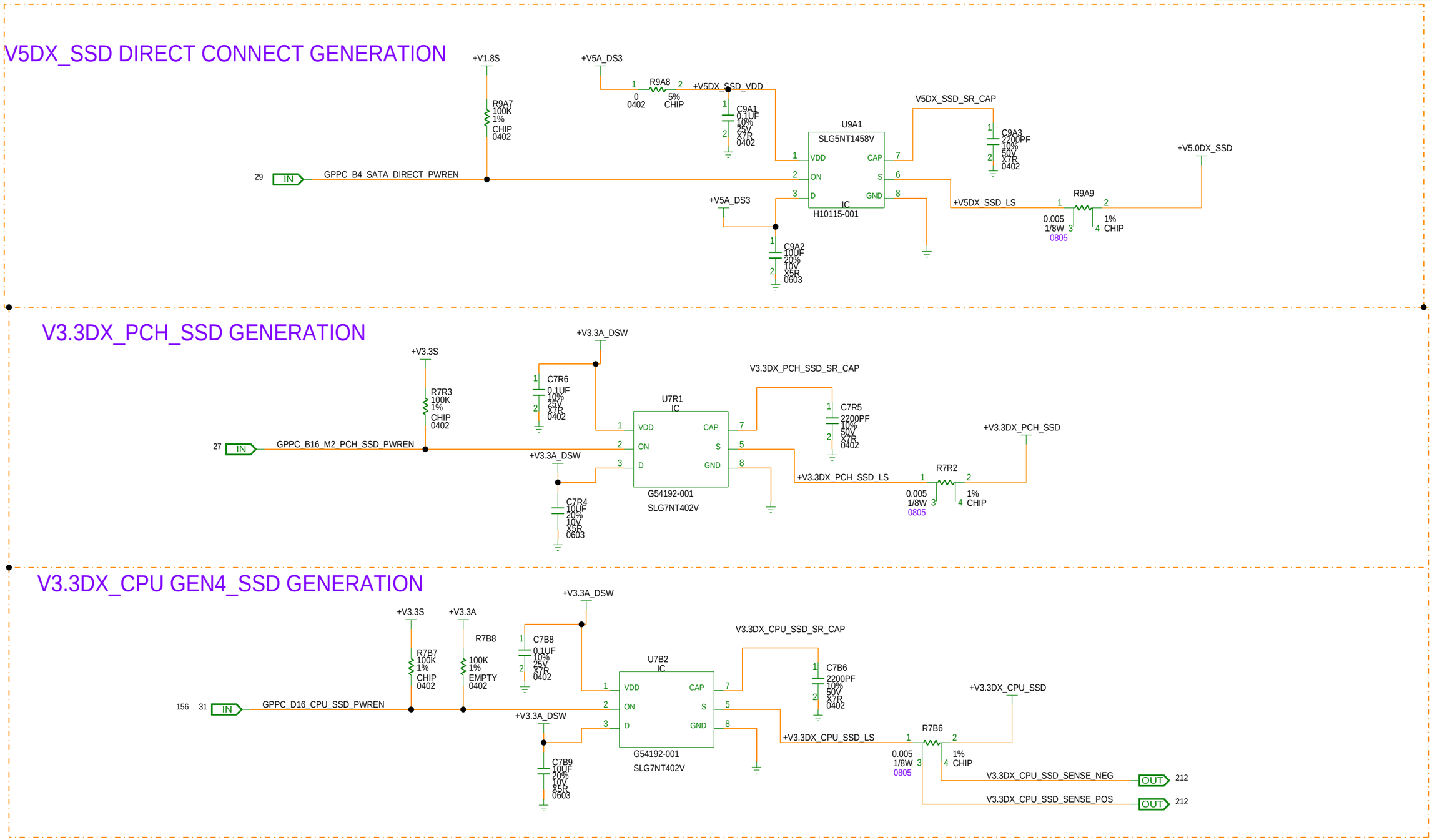
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.236
Wed Dec 18 18:09:07 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	236	1.0

RTD3 LOAD SWITCH --> SSD]

CR-237 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE237

MODULE REV DETAILS		
MODULE NAME	REV	DATE



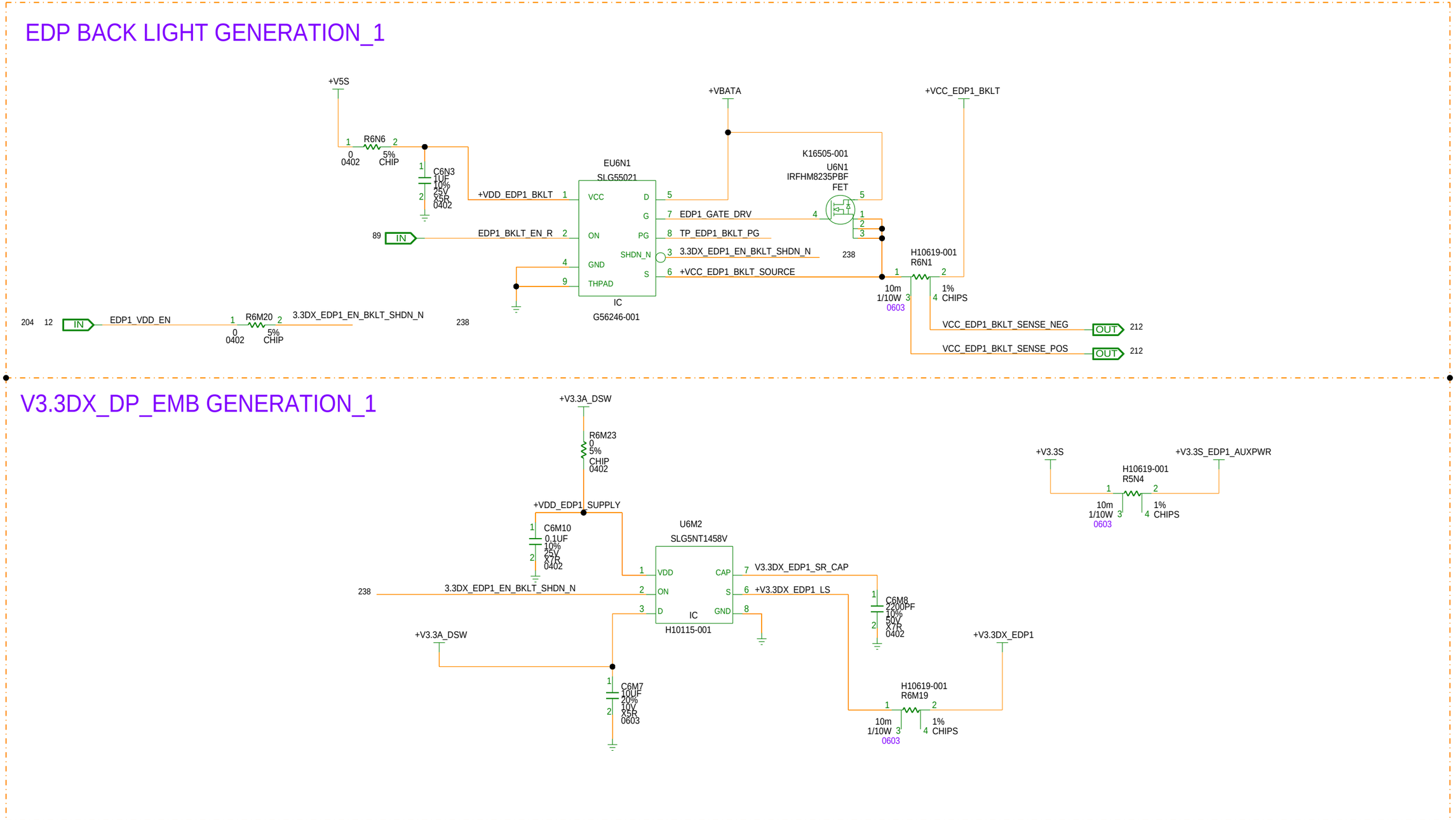
[PAGE_TITLE= V5DX_SSD DIRECT CONNECT AND V3.3DX_SSD GENERATION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.237
Wed Dec 18 18:09:08 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	237	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= EDP BACKLIGHT AND V3.3DX_DP_EMB RAILS GENERATION_1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.238
Wed Dec 18 18:09:09 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	238	1.0

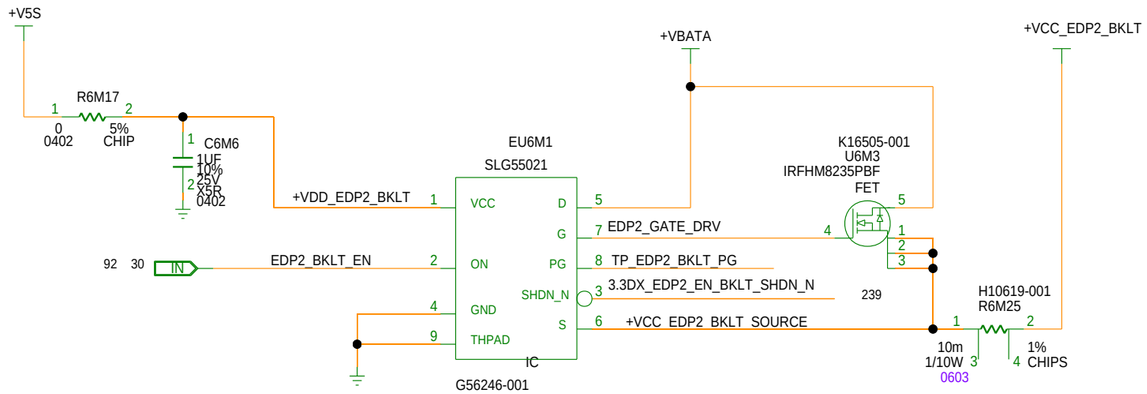
CUSTOM TEXT BPAGE

2X10 HEADERS FOR ID DETECTION

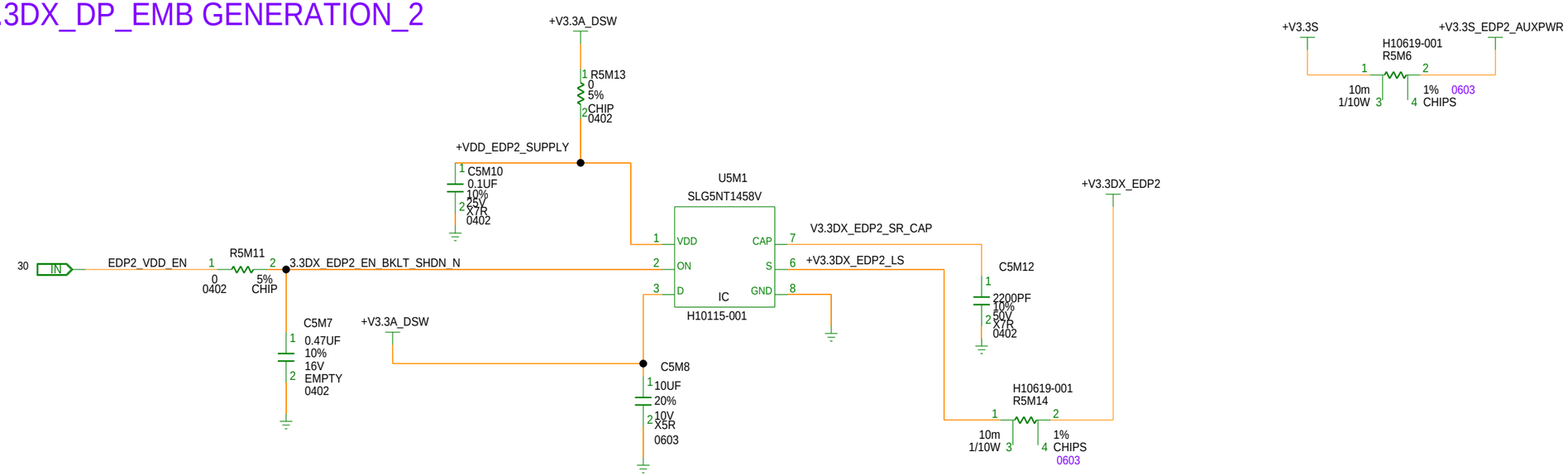
CR-239 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE239

MODULE REV DETAILS		
MODULE NAME	REV	DATE

EDP BACK LIGHT GENERATION_2



V3.3DX_DP_EMB GENERATION_2



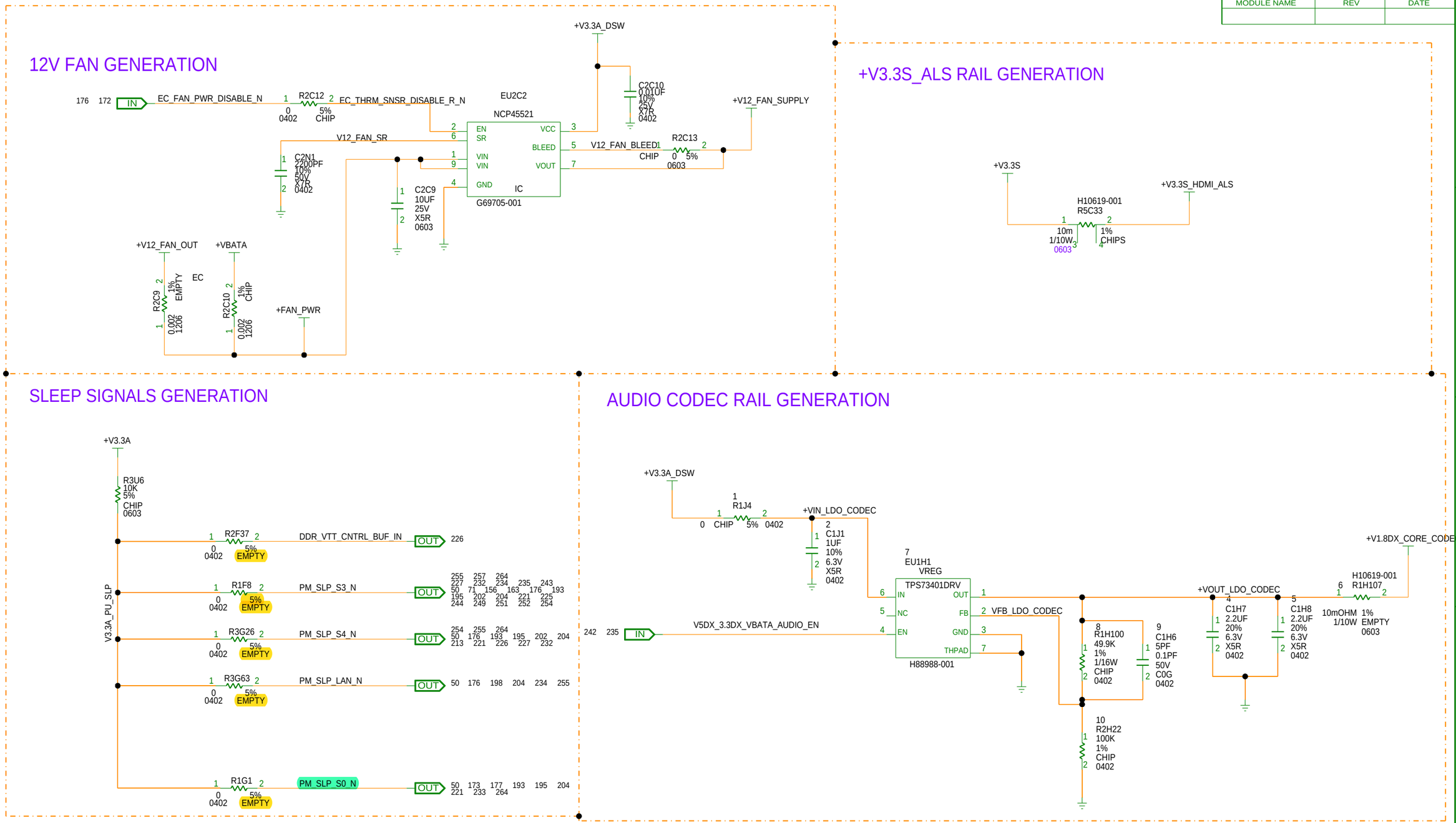
[PAGE_TITLE= EDP BACKLIGHT AND V3.3DX_DP_EMB RAILS GENERATION_2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.239
Wed Dec 18 18:09:10 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	239	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= 5V FAN RAIL,SLEEP SIGNAL V3.3S_ALS AND AUDIO CODEC RAIL GENERATION]

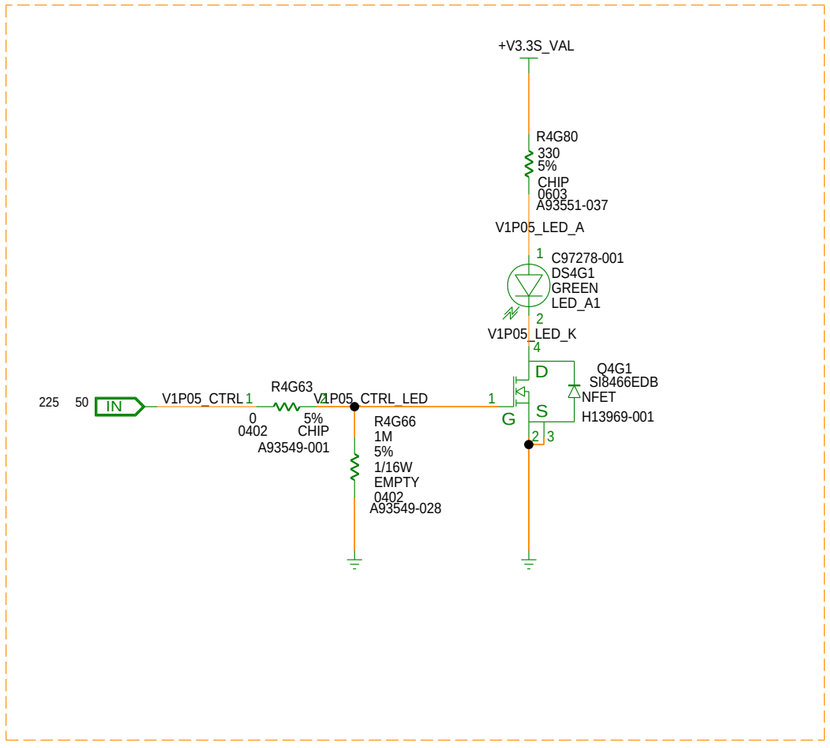
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.240
Wed Dec 18 18:09:11 2019

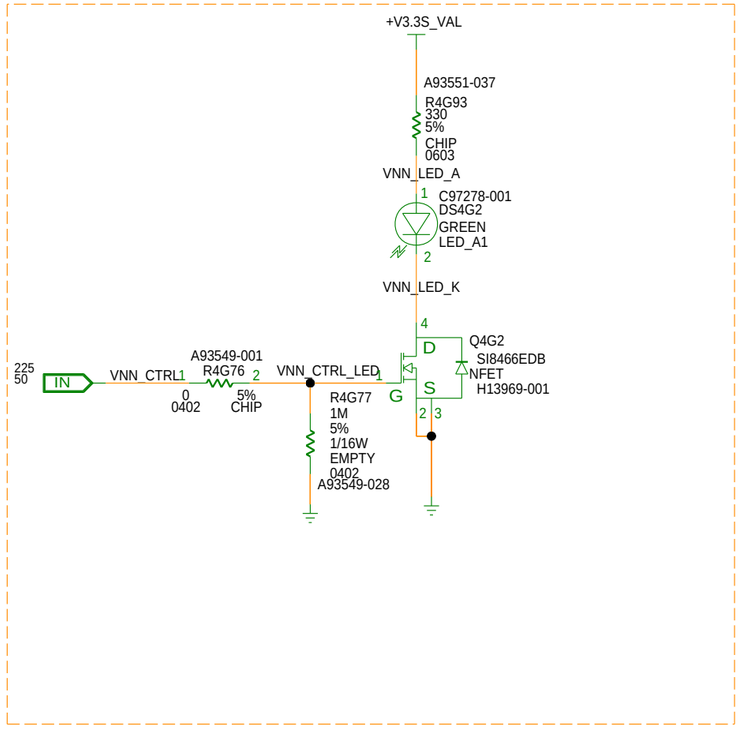
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	240	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

S0iX LED



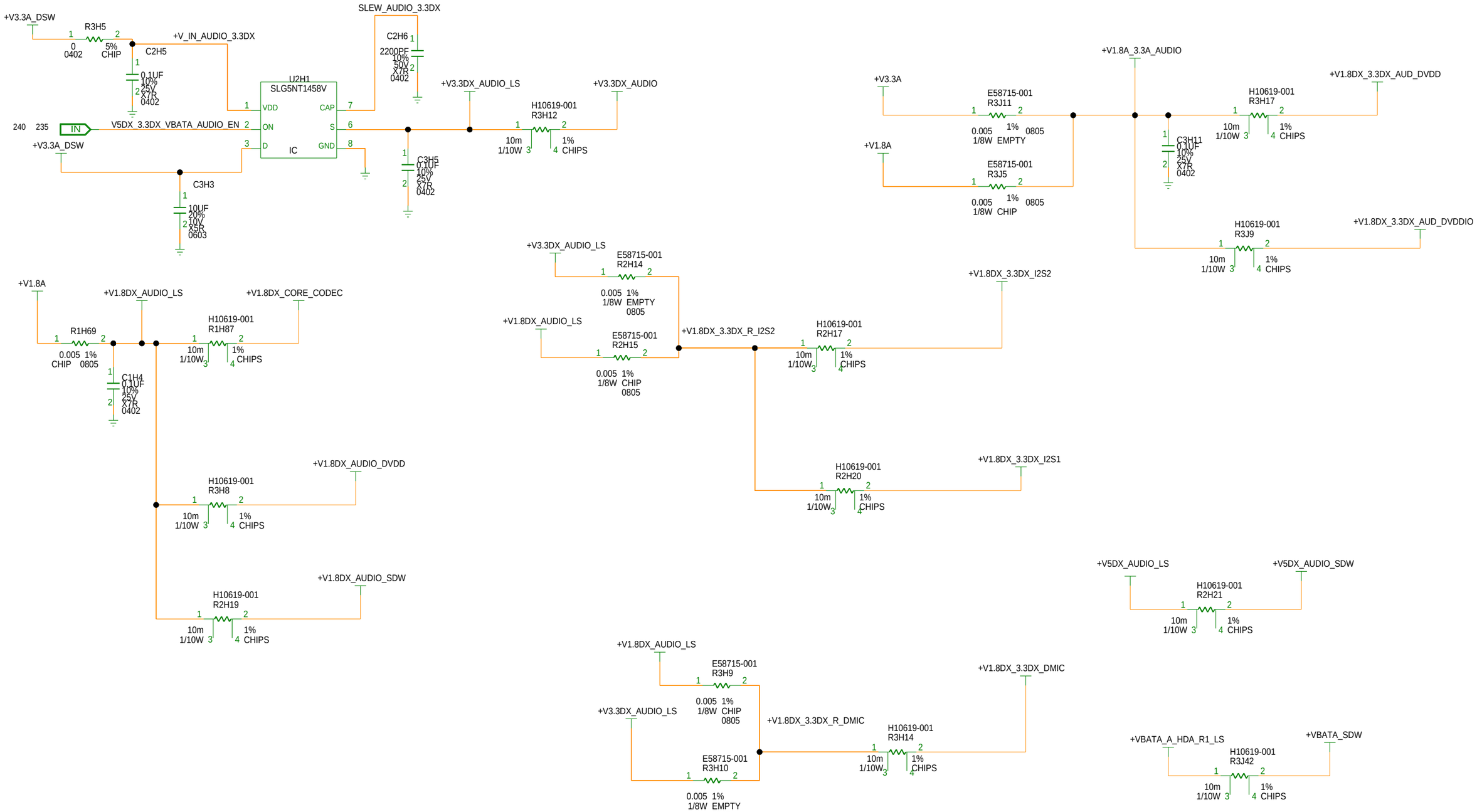


[PAGE_TITLE= SOIX LED]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.241
Wed Dec 18 18:09:11 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	241	1.0

AUDIO POWER SUPPLY GENERATION



MODULE REV DETAILS

MODULE NAME	REV	DATE

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.242
Wed Dec 18 18:09:12 2019

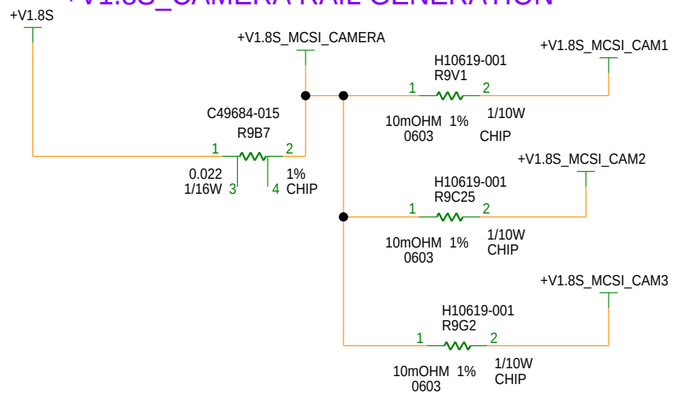
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	242	1.0

[PAGE_TITLE= AUDIO POWER SUPPLY GENERATION]

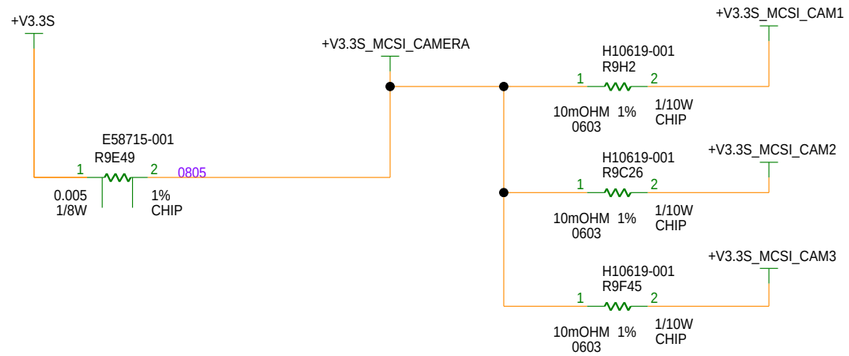
MODULE REV DETAILS		
MODULE NAME	REV	DATE

DERIVED CAMERA RAILS

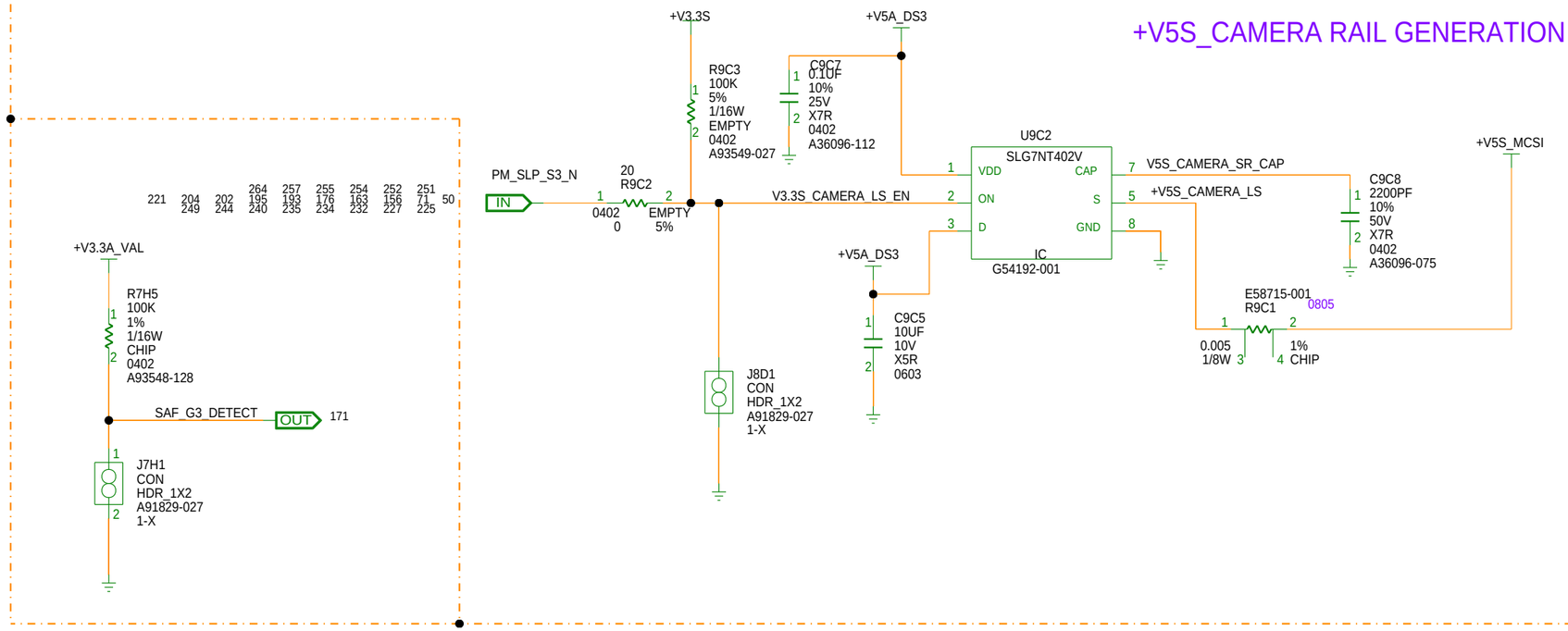
+V1.8S_CAMERA RAIL GENERATION



+V3.3S_CAMERA RAIL GENERATION



+V5S_CAMERA RAIL GENERATION



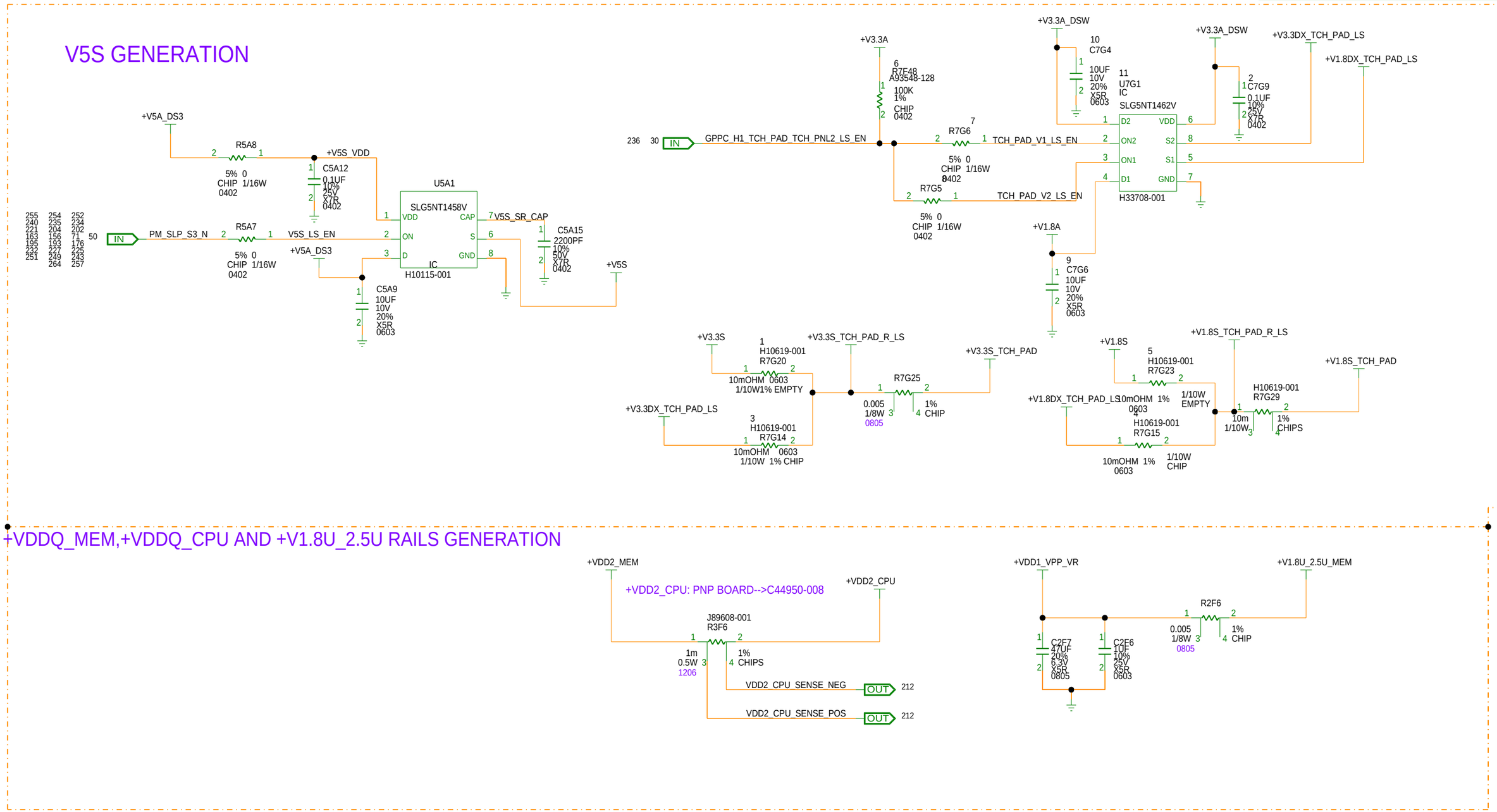
[PAGE_TITLE= SD POWER RAILS GENERATION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.243
Wed Dec 18 18:09:13 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	243	1.0

CR-244 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE244

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= V5S, V1.8U_2.5U_MEM AND VDDQ_CPU RAILS GENERATION

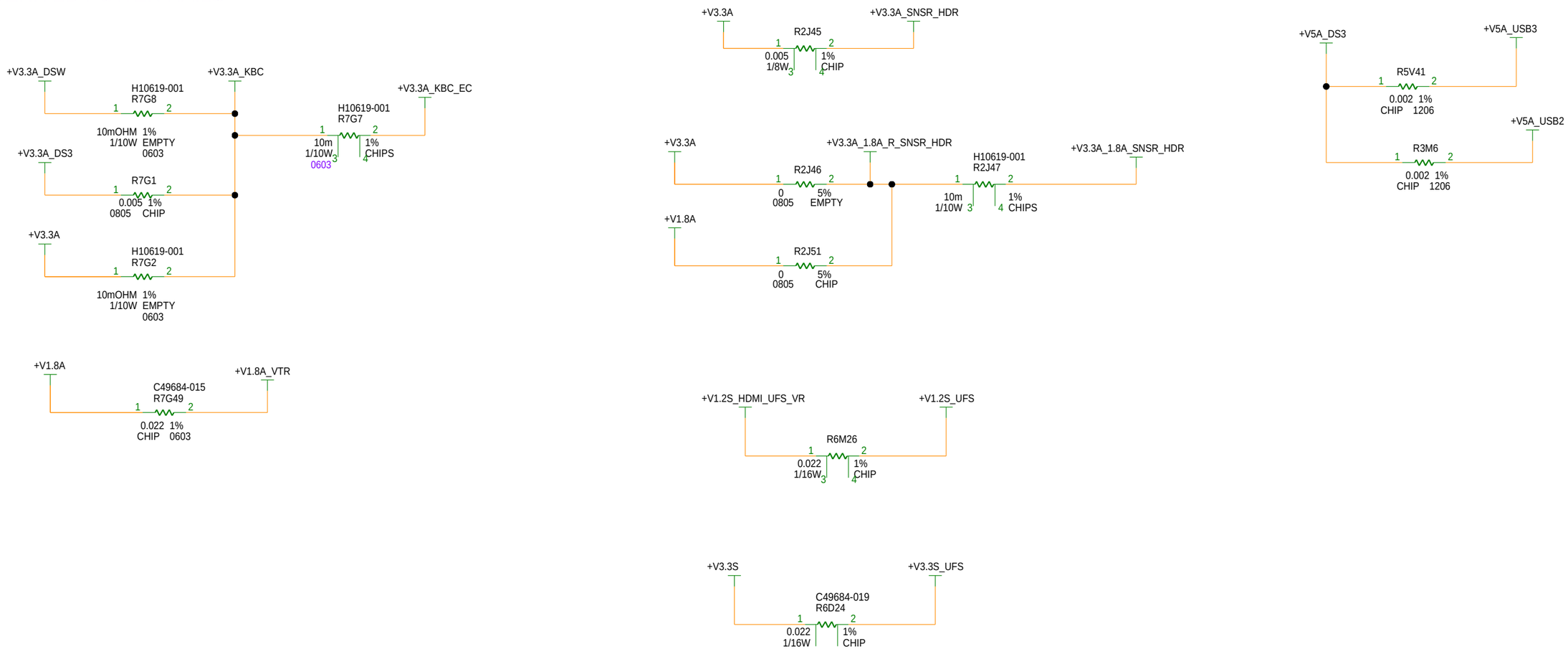
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.244
Wed Dec 18 18:09:14 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	244	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DERIVED POWER RAILS



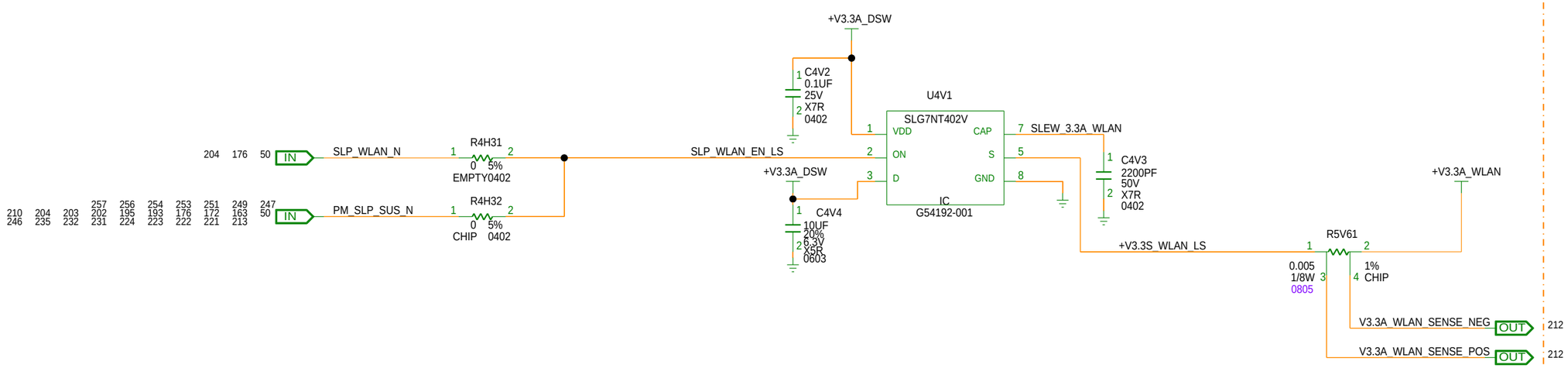
[PAGE_TITLE=POWER MEASUREMENT RESISTORS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.245
Wed Dec 18 18:09:15 2019

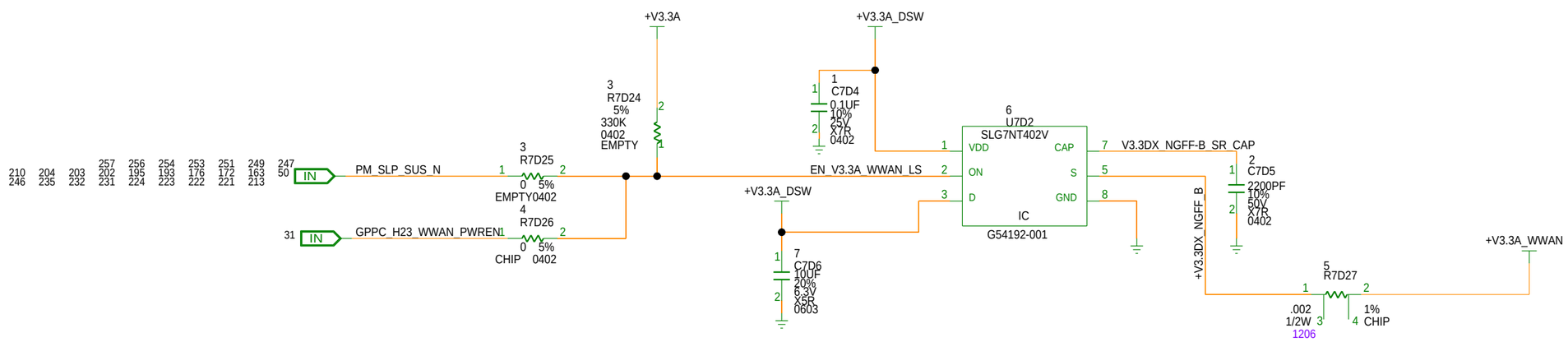
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	245	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

+V3.3A_WLAN RAIL GENERATION



V3.3A_WWAN GENERATION



[PAGE_TITLE= CAMERA, WLAN AND WWAN POWER GENERATION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.246
Wed Dec 18 18:09:16 2019

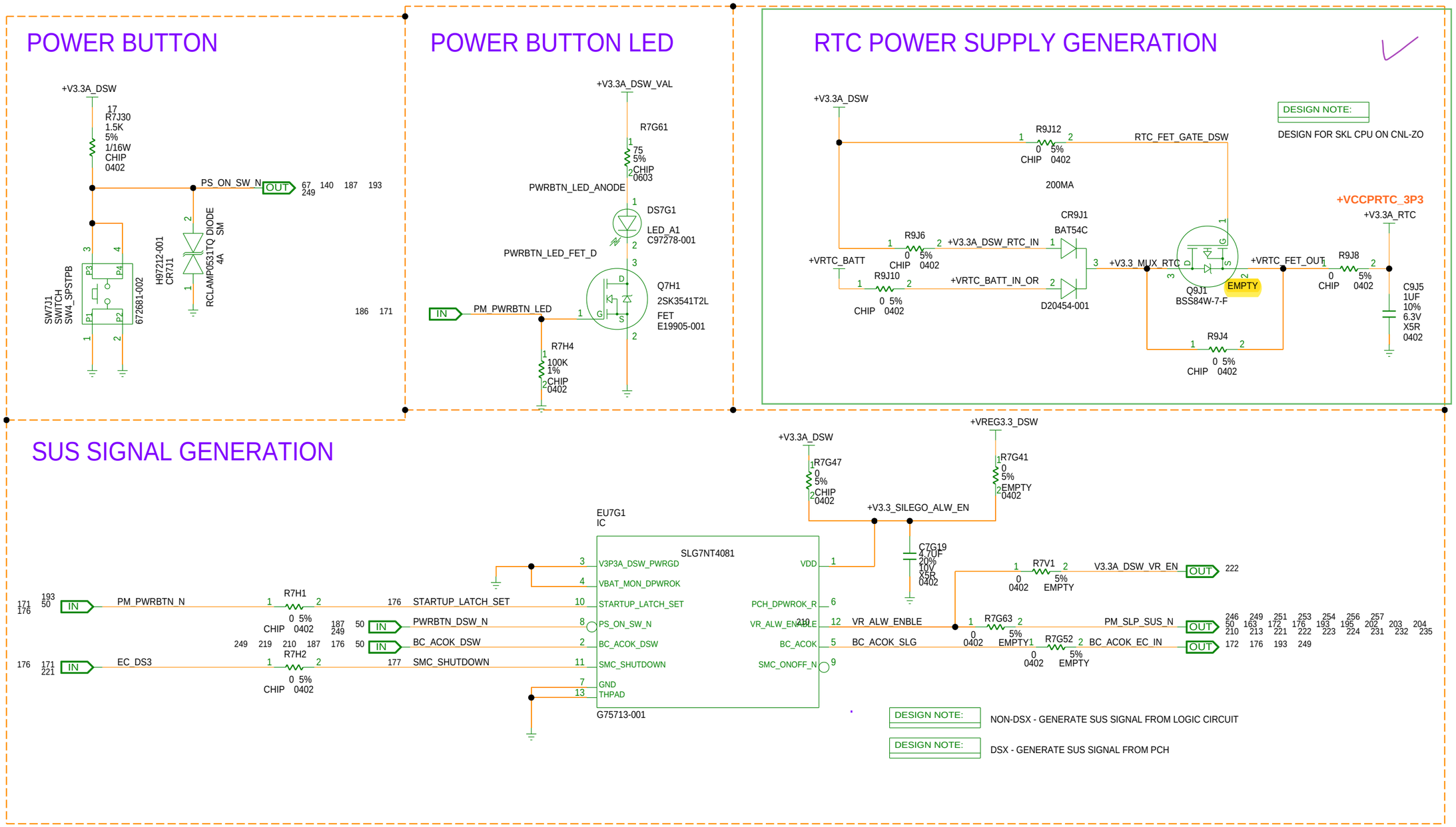
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	246	1.0

CUSTOM TEXT BPAGE

POWER BUTTON AND SLP_SUS# CIRCUITRY

CR-247 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE247

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= POWER BUTTON, RTC AND SLP_SUS# CIRCUITRY]

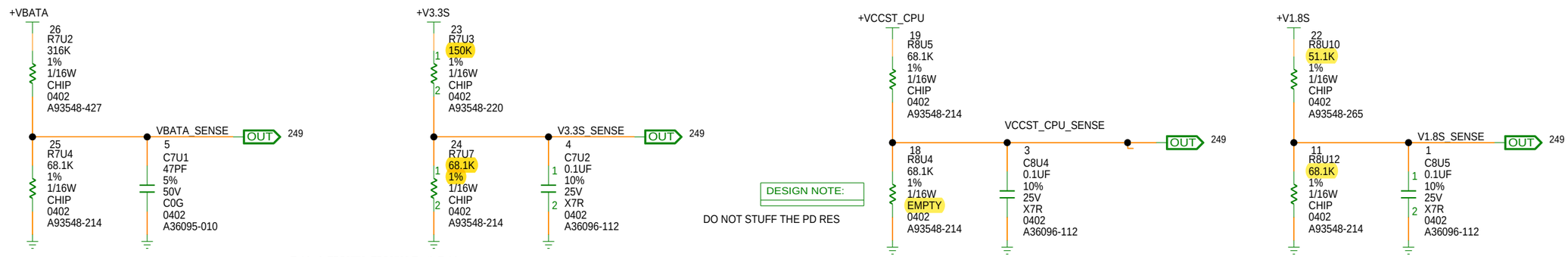
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.247
Tue Sep 03 14:17:26 2013

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	247	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

POWER SEQUENCING LOGIC - PAGE I



DESIGN NOTE:

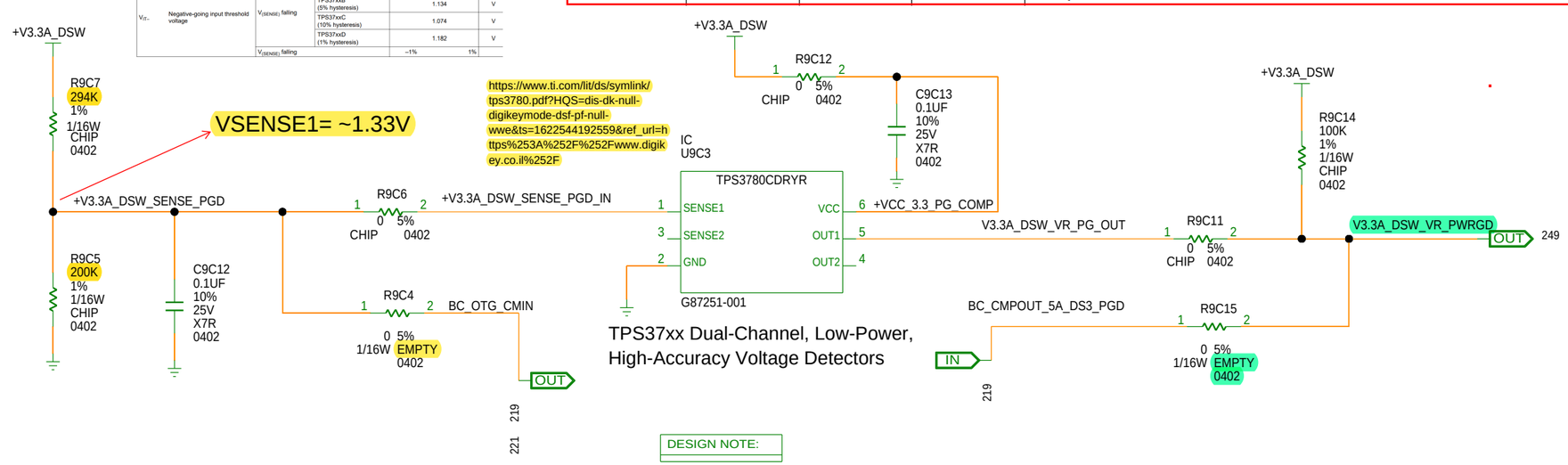
DO NOT STUFF THE PD RES

Table 1. TPS3779, TPS3780 Truth Table

CONDITIONS	OUTPUT
SENSE1 < V_{IT-}	OUT1 = low
SENSE2 < V_{IT-}	OUT2 = low
SENSE1 > V_{IT+}	OUT1 = high
SENSE2 > V_{IT+}	OUT2 = high

V_{IT+}	Positive-going input threshold voltage	$V_{(SENSE)}$ rising			1.194	V
				−1%	1%	
V_{IT-}	Negative-going input threshold voltage	$V_{(SENSE)}$ falling	TPS37xxA (0.5% hysteresis)		1.188	V
			TPS37xxB (5% hysteresis)		1.134	V
			TPS37xxC (10% hysteresis)		1.074	V
			TPS37xxD (1% hysteresis)		1.182	V
		$V_{(SENSE)}$ falling		−1%	1%	

OUT1	5	2	O	OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below V_{IT-}. OUT1 is deasserted (goes high) after SENSE1 rises higher than V_{IT+}. OUT1 is a push-pull output for the TPS3779 and an open-drain output for the TPS3780. The open-drain device (TPS3780) can be pulled up to 6.5 V independent of VDD; a pull-up resistor is required for this device.



DESIGN NOTE:

SENSE2 COMPARATOR IS NOT USED

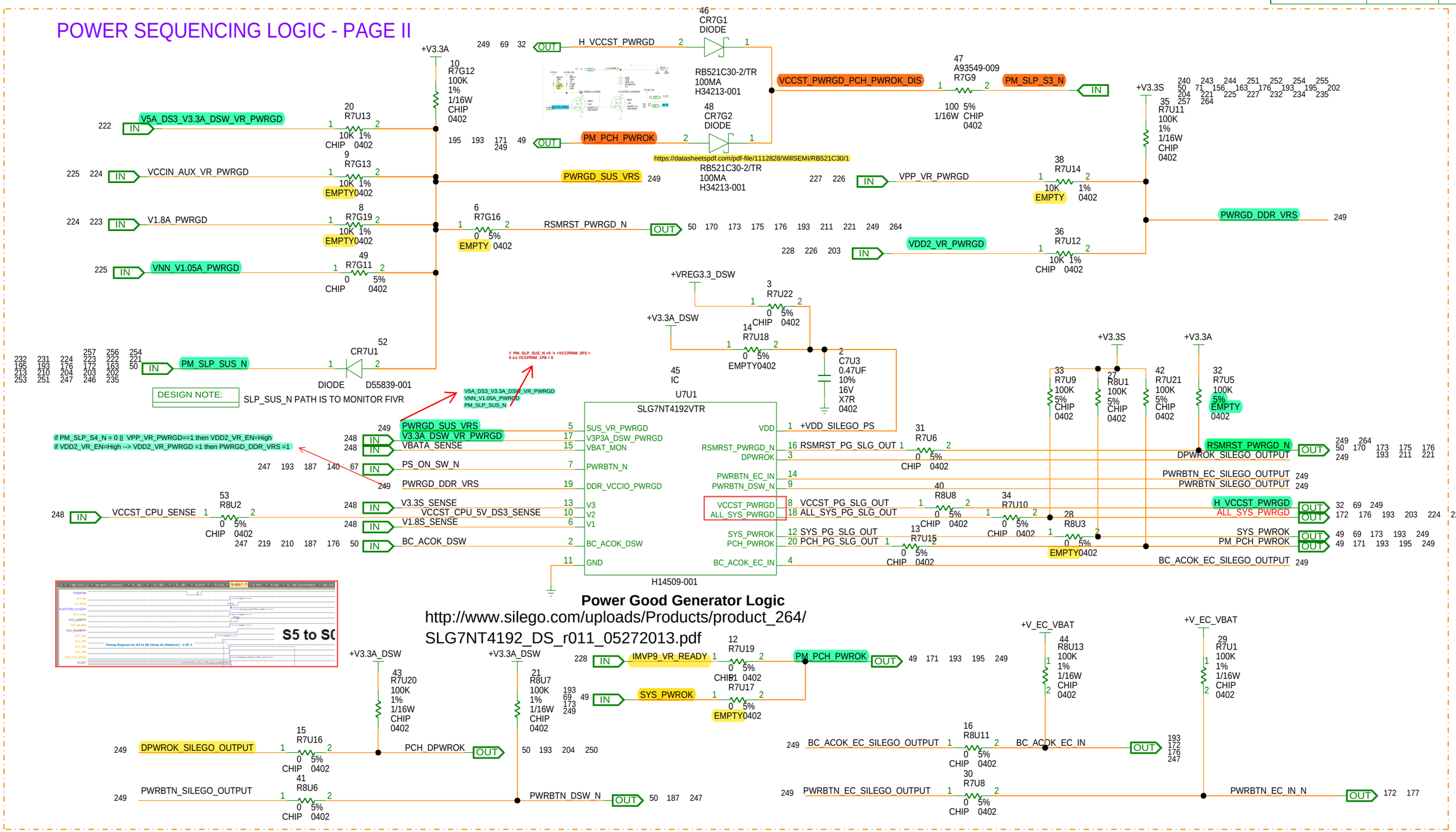
[PAGE_TITLE= POWER SEQUENCING LOGIC - PAGE I]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.248
Wed Dec 18 18:09:17 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	248	1.0

MODULE REV DETAILS		
MODULE NAME	REV	DATE

POWER SEQUENCING LOGIC - PAGE II



[PAGE_TITLE= POWER SEQUENCING LOGIC - PAGE II]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.249
Wed Dec 18 18:09:18 2019

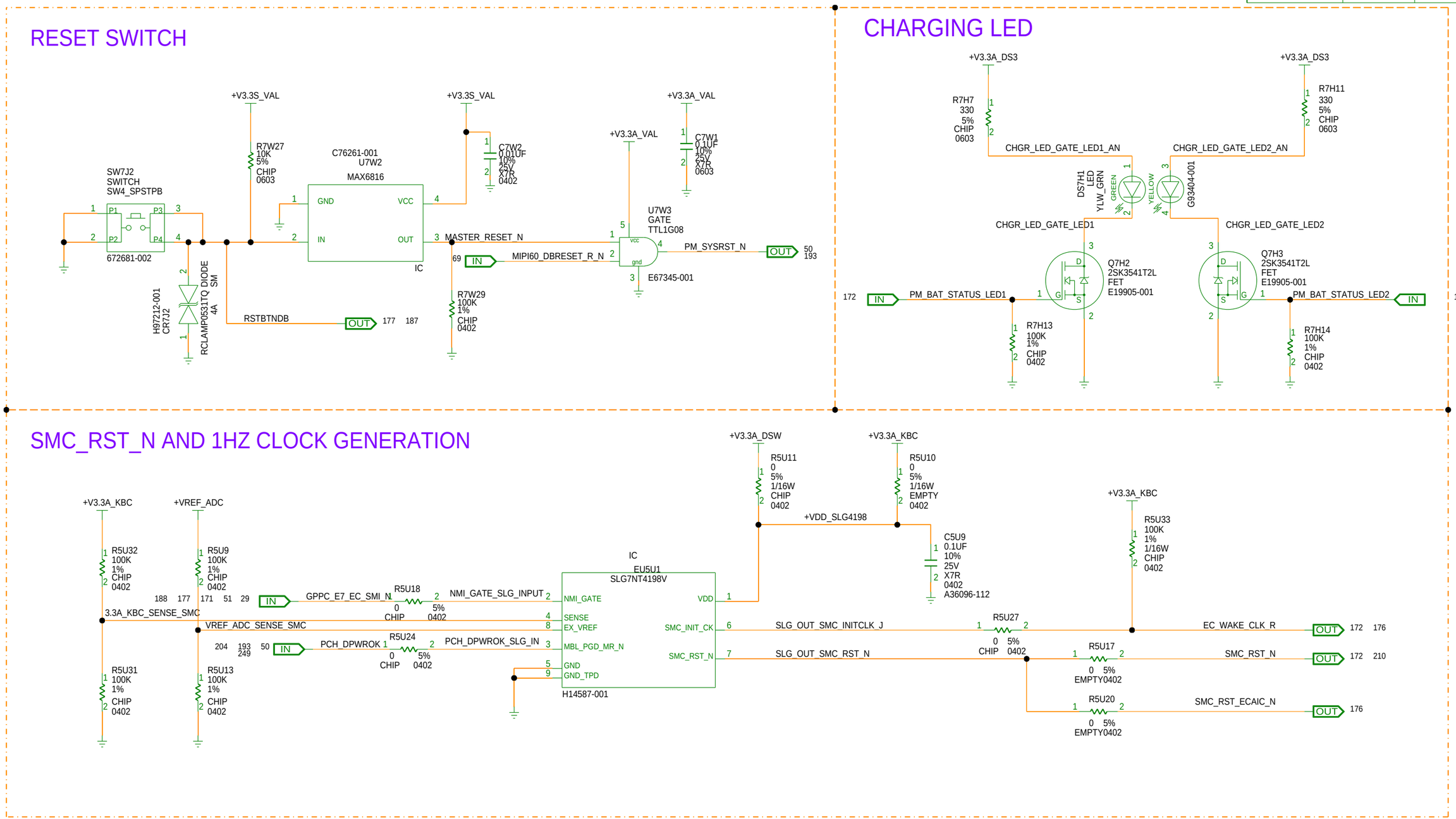
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	249	1.0

CUSTOM TEXT BPAGE

RESET SWITCH AND SMC RST IMPLEMENTATION

CR-250 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE250

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= RESET SWITCH, CHARGING LED AND SMC RST IMPLEMENTATION]

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.250
Wed Dec 18 18:09:19 2019

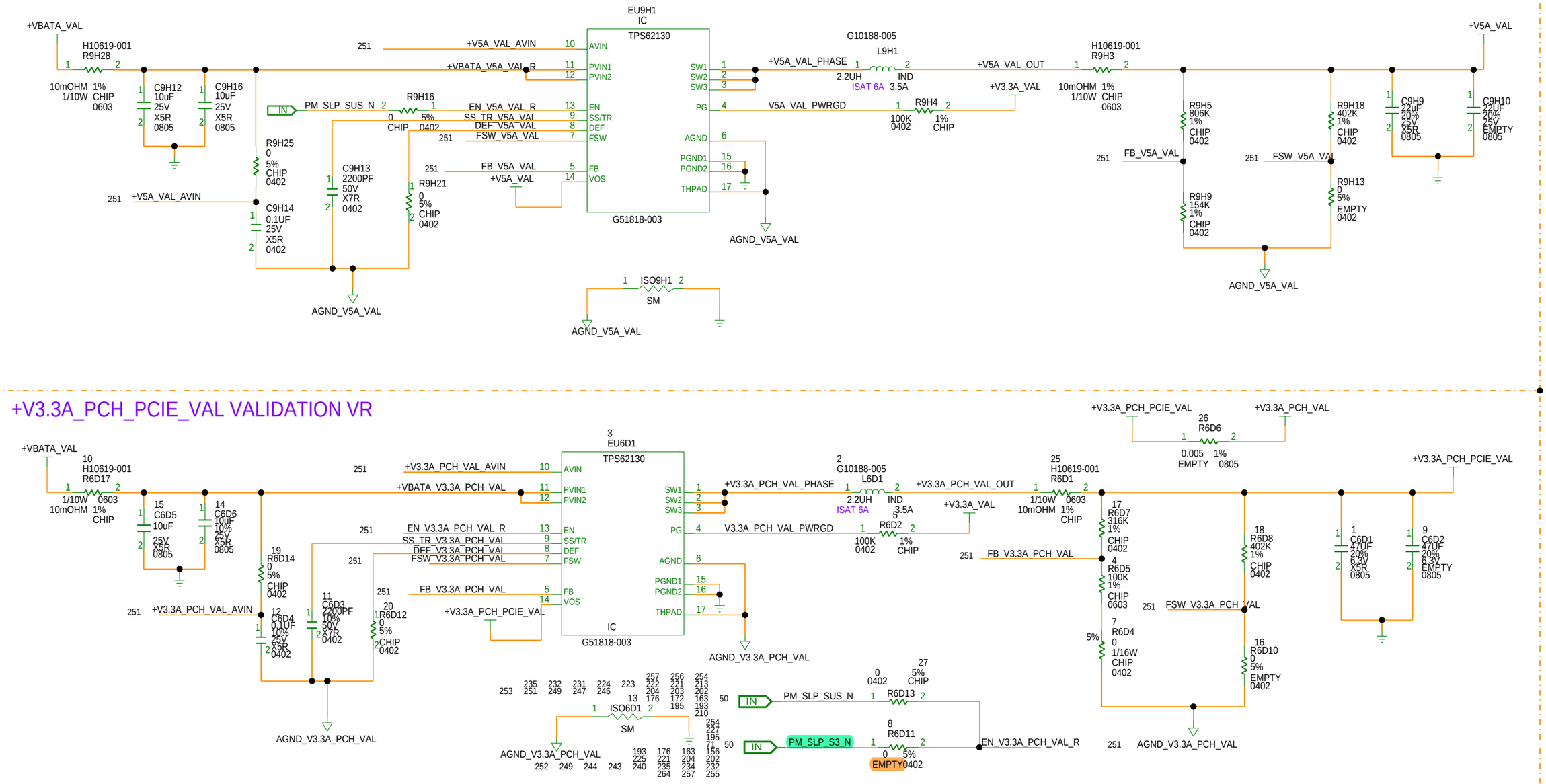
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	250	1.0

CUSTOM TEXT BPAGE

CR-251 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE251

MODULE REV DETAILS		
MODULE NAME	REV	DATE

+V5A_VAL VALIDATION VR



+V3.3A_PCH_PCIE_VAL VALIDATION VR

[PAGE_TITLE= V5A AND 3.3.A_PCH VAL RAILS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.251
Wed Dec 18 18:09:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	251	1.0

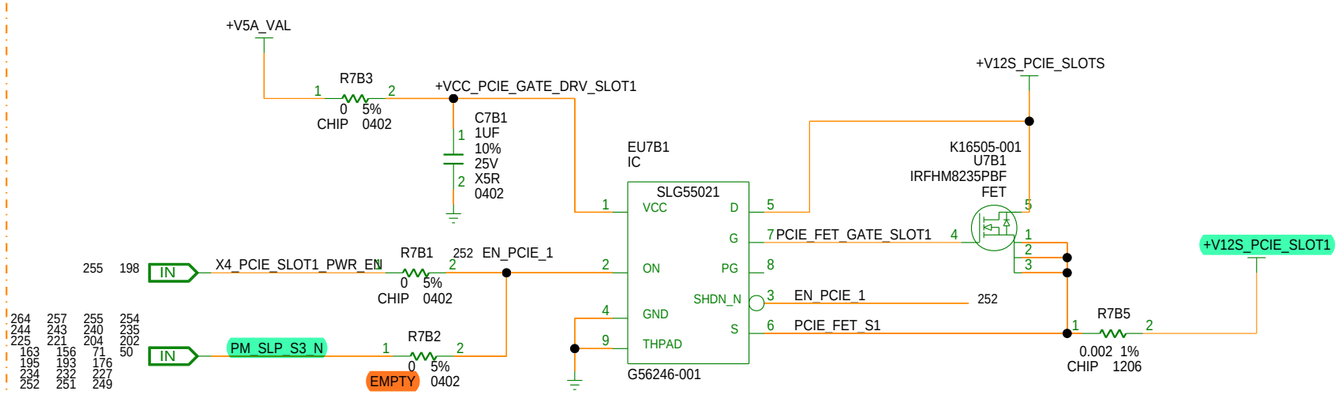
CUSTOM TEXT BPAGE

1.05A_VAL POWER RAIL GENERATION

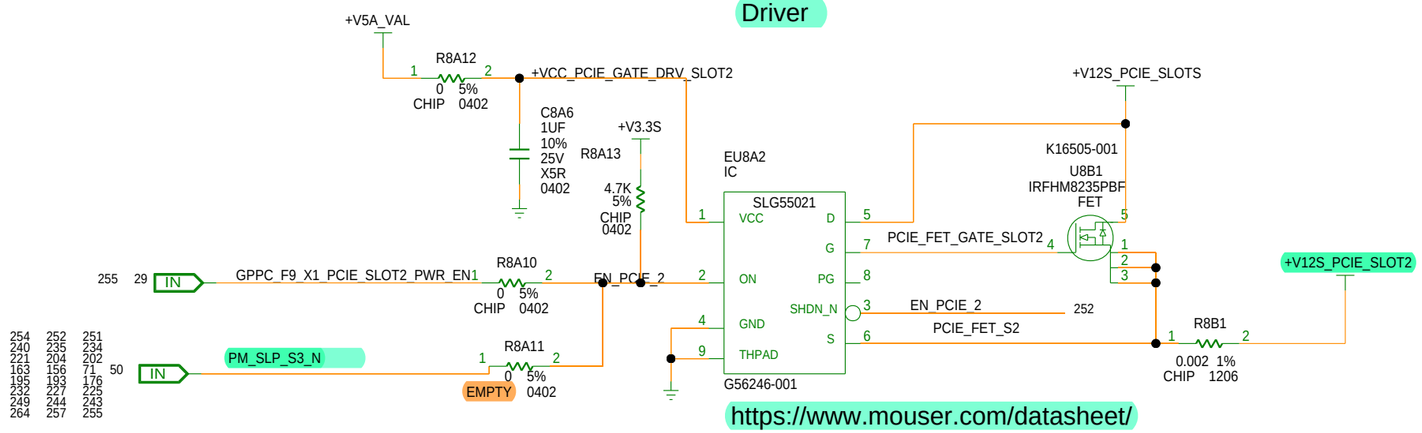
CR-252 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE252

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PCIE SLOT1 POWER GENERATION



GreenFETTM High Voltage Gate Driver



https://www.mouser.com/datasheet/2/665/xSLG55021-200010r101_06172014-765194.pdf

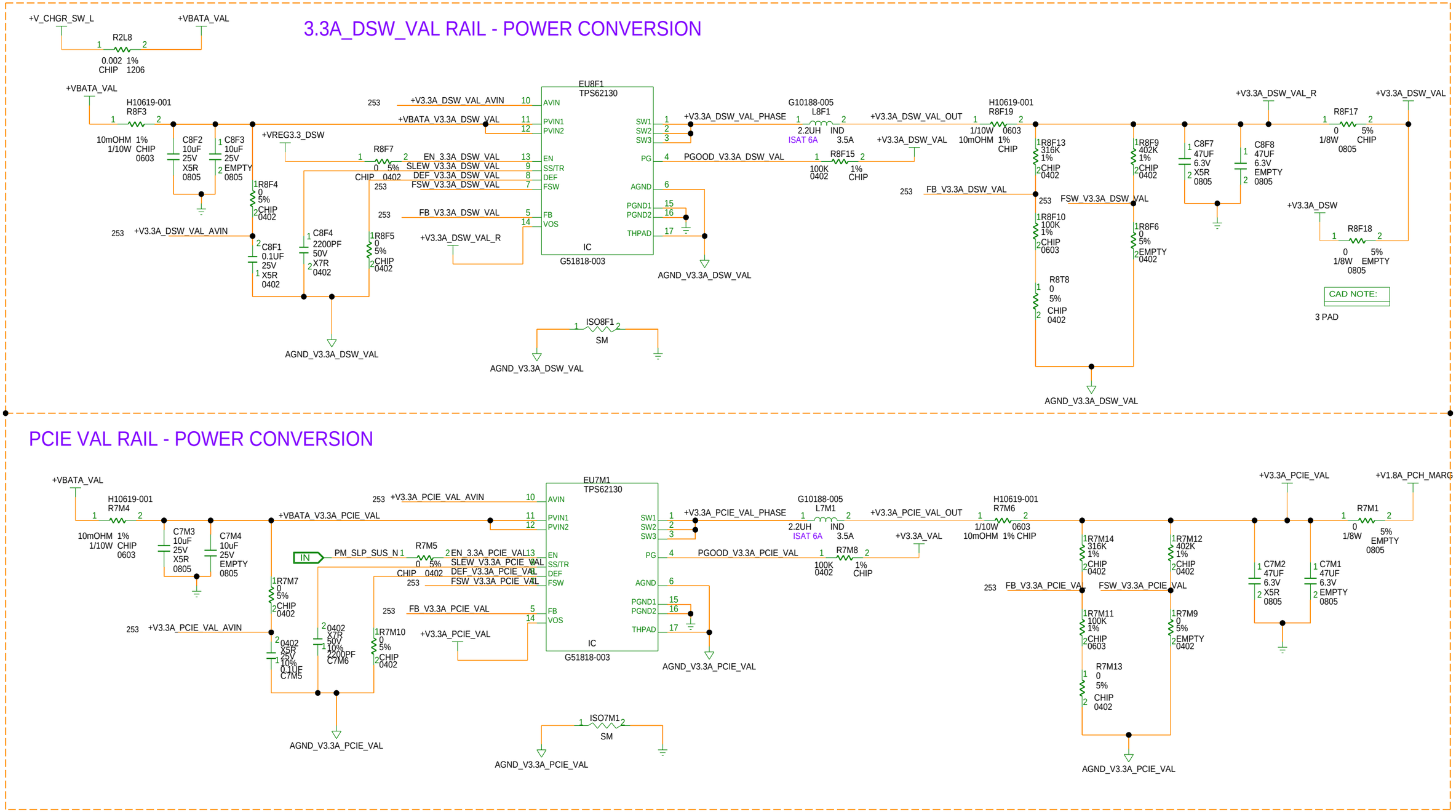
[PAGE_TITLE= PCIE SLOT1 AND V3.3A_VAL POWER RAIL GENERATION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.252
Wed Dec 18 18:09:21 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	252	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= V3.3A_DSW_VAL AND PCIE VAL RAIL GENERATION]

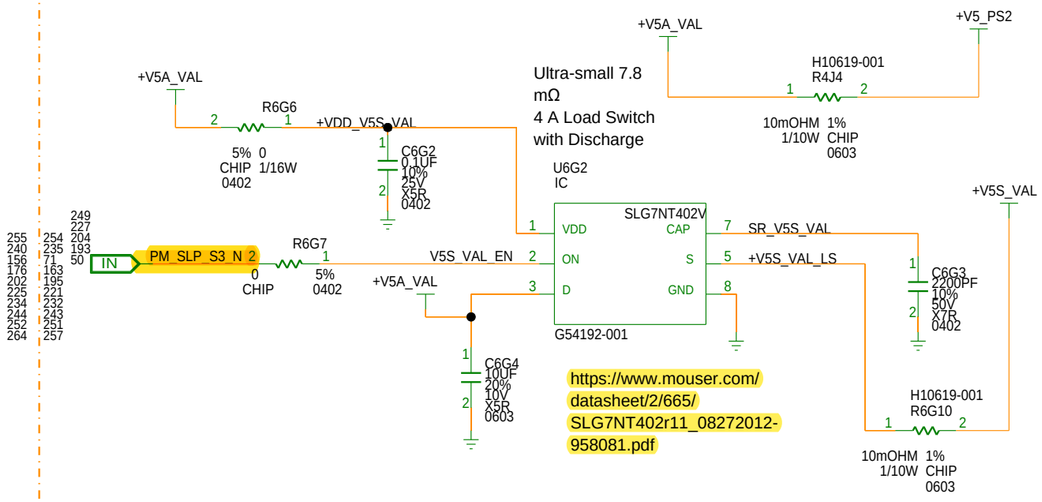
BPAGE DRAWING
tigerlake_u_ddr4.sch_1.253
Wed Dec 18 18:09:22 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	253	1.0

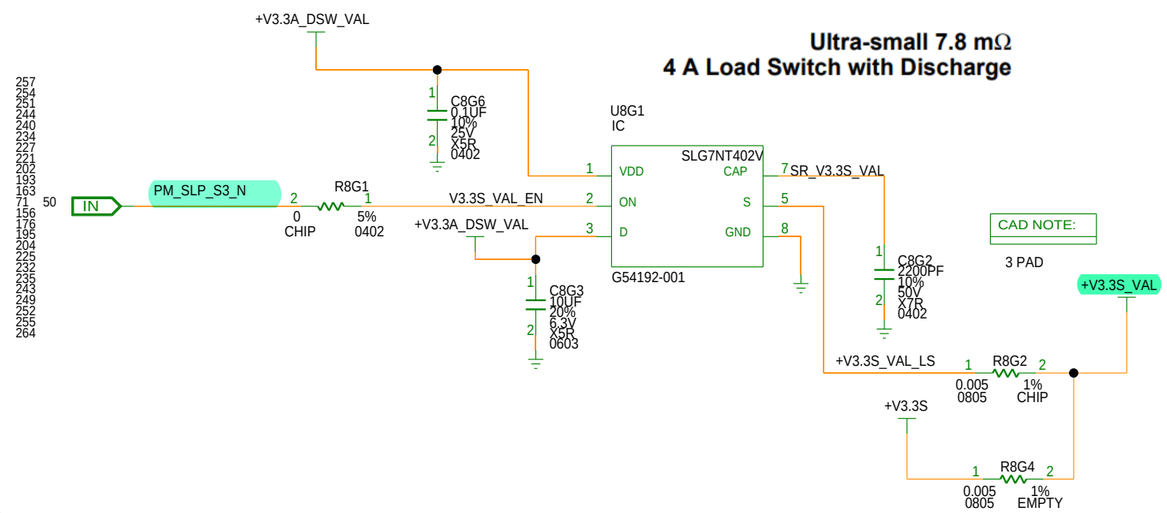
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

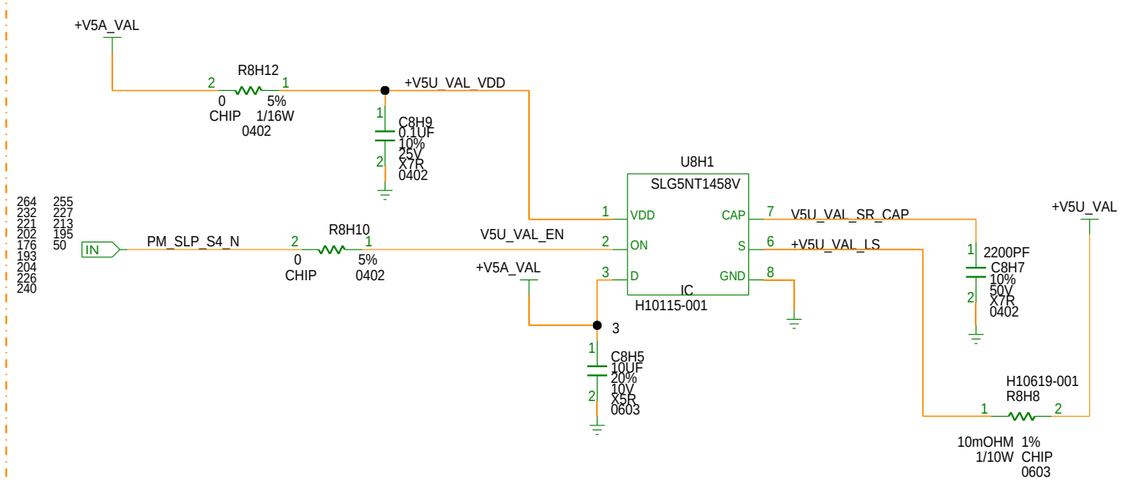
V5S_VAL GENERATION



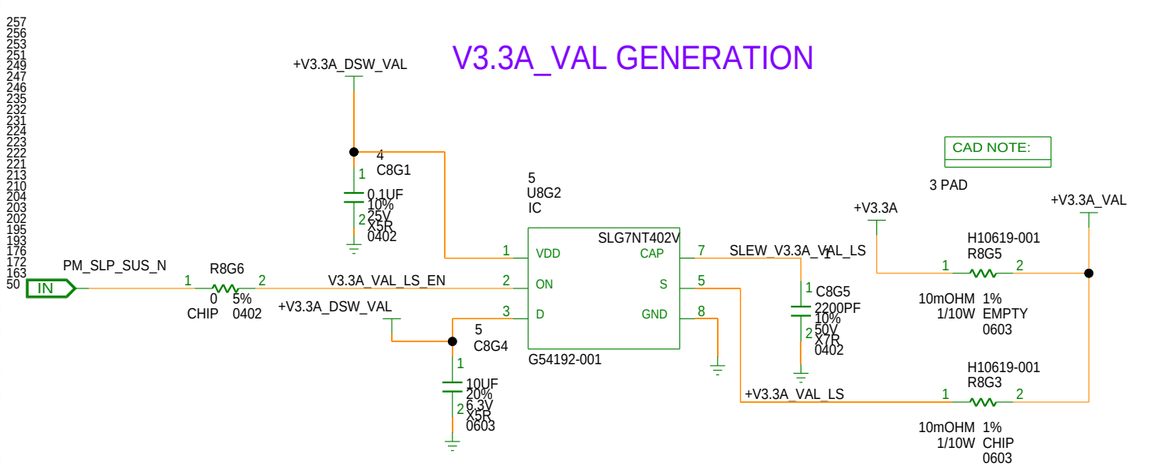
V3.3S_VAL GENERATION



V5U_VAL GENERATION



V3.3A_VAL GENERATION



[PAGE_TITLE= U AND S VALIDATION RAILS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.254
Wed Dec 18 18:09:22 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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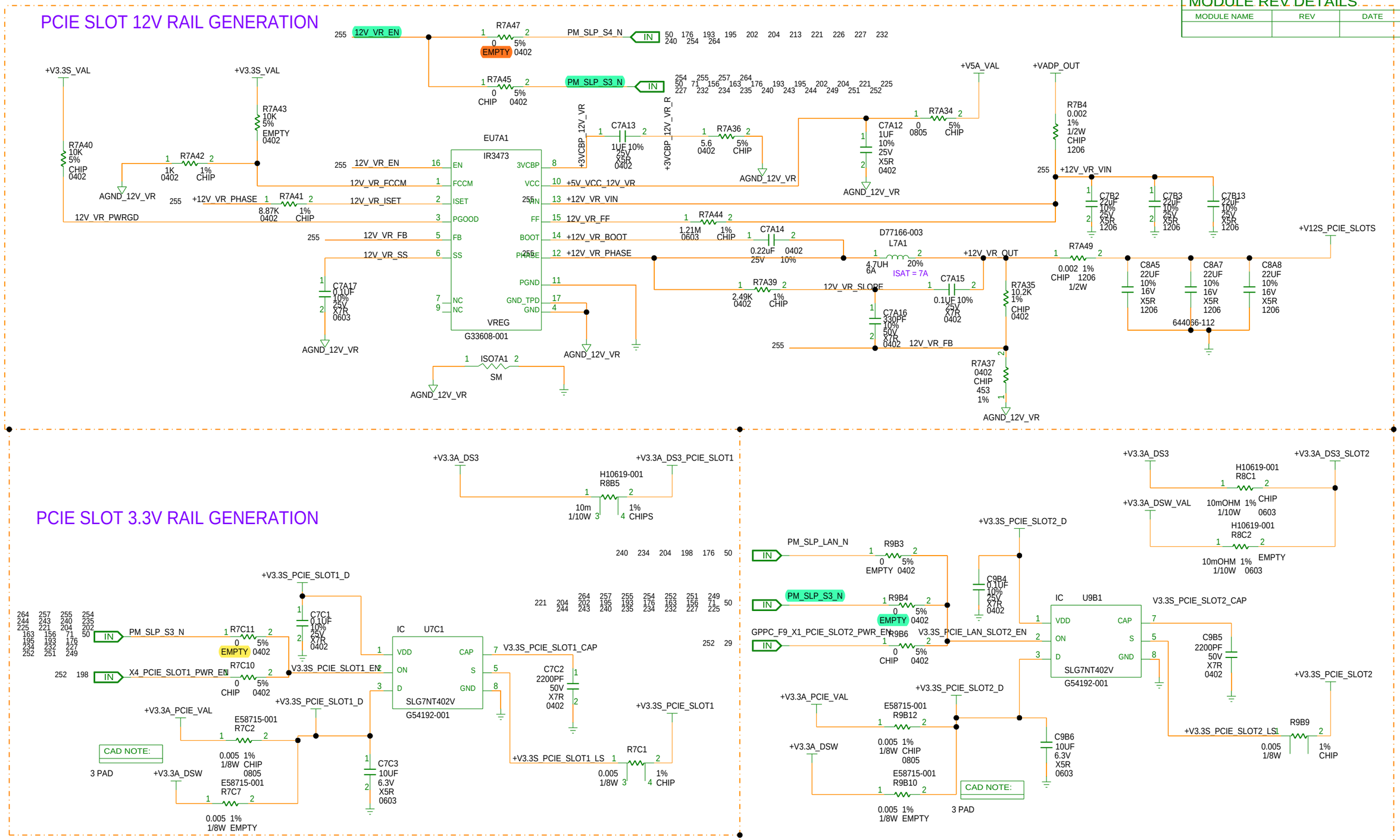
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= PCIE SLOT 12V, 3.3V, V5_PS2 AND V3.3_KBC_SR RAIL GENERATION]

BPAGE DRAWING
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Wed Dec 18 18:09:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	255	1.0

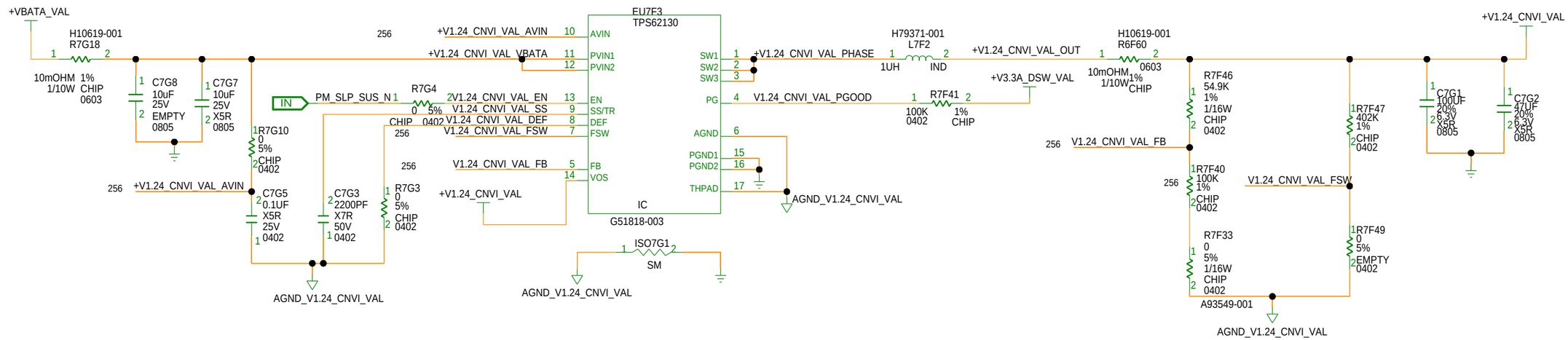
CUSTOM TEXT BPAGE

MOUNTING HOLES

CR-256 : @TIGERLAKE_LIB.TIGERLAKE_U_DDR4(SCH_1):PAGE256

MODULE REV DETAILS		
MODULE NAME	REV	DATE

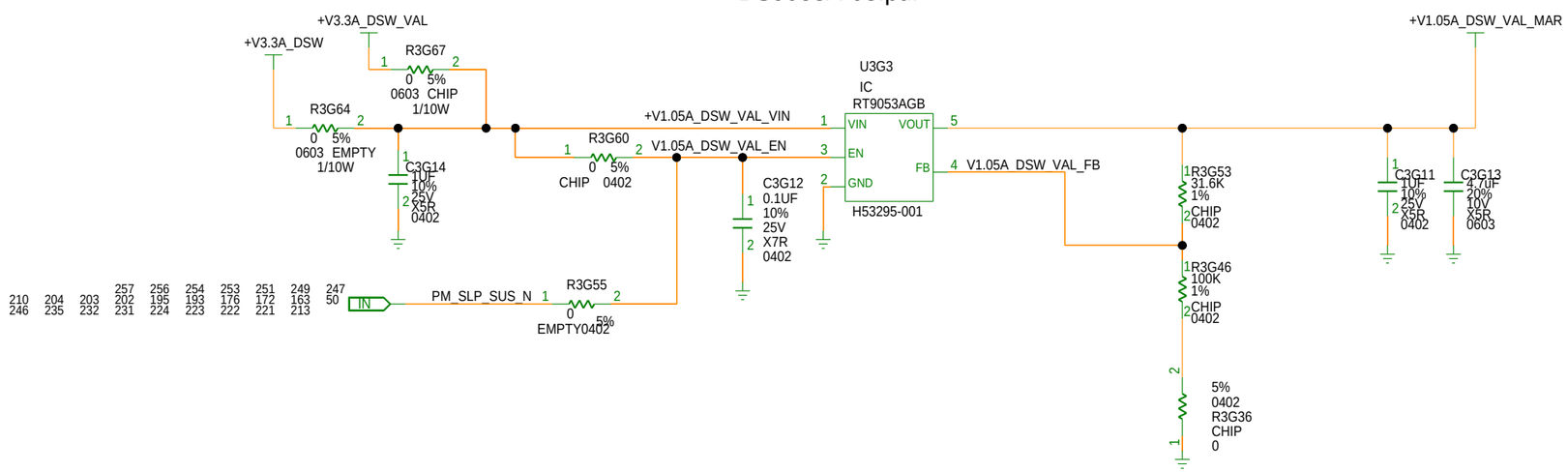
VAL RAIL FOR DPHY 1.24 BLOCK



+V1.05A_DSW_VAL_MAR RAIL

https://www.richtek.com/assets/product_file/RT9053A/DS9053A-03.pdf

Low Dropout, 400mA Adjustable Linear Regulator



[PAGE_TITLE= VAL RAILS FOR DPY 1.24 AND V1.05A_VAL]

BPAGE DRAWING
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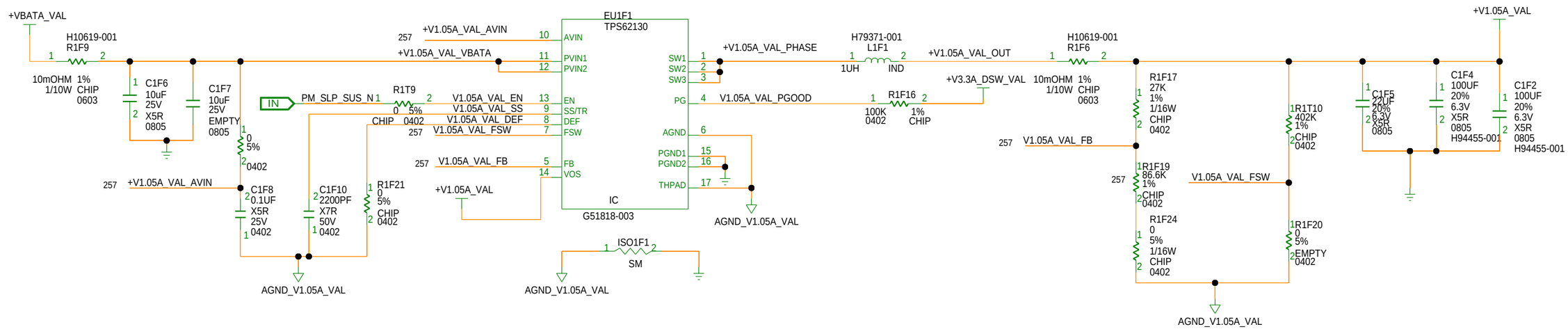
Wed Dec 18 18:09:24 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	256	1.0

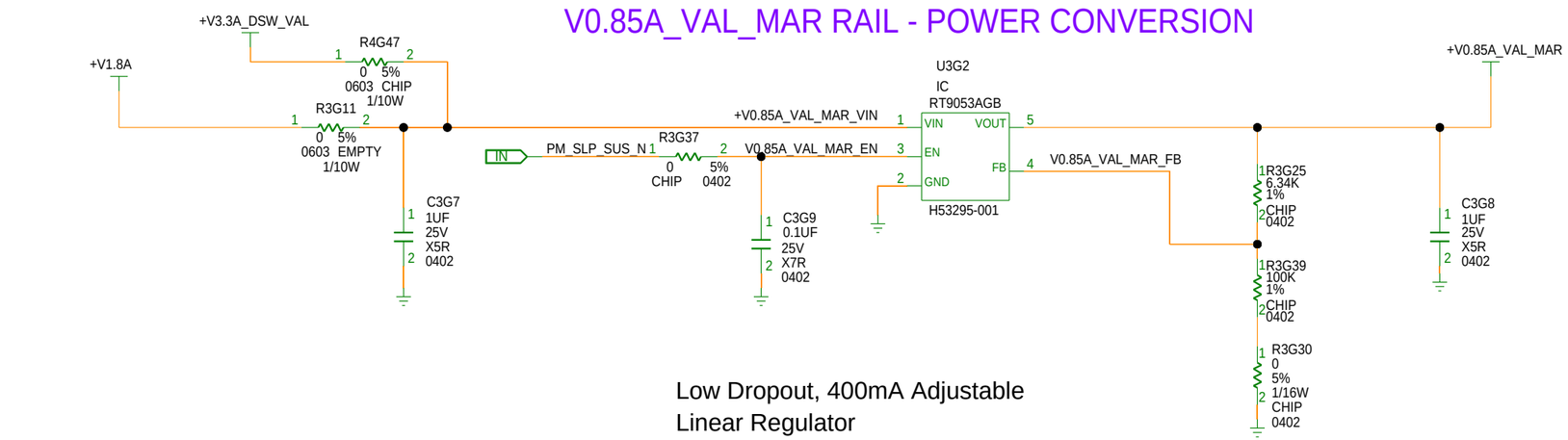
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

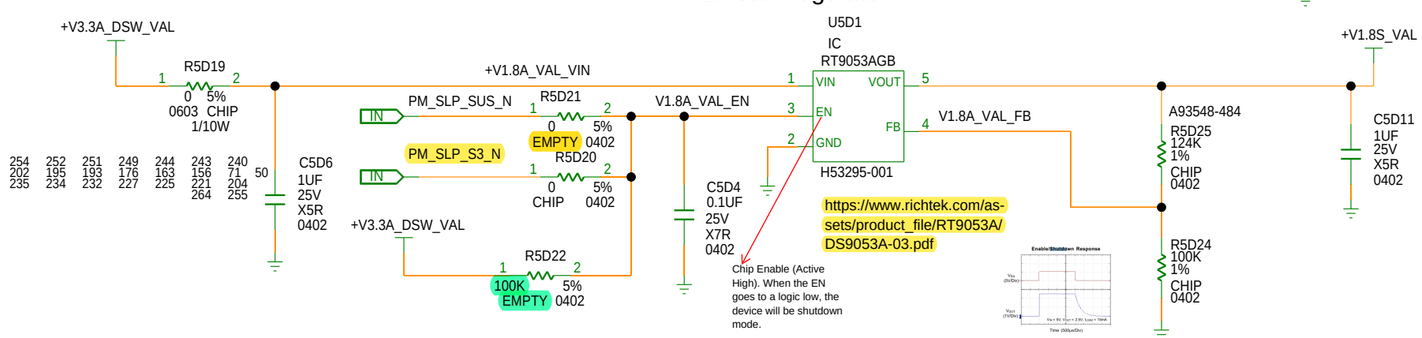
V1.05A_VAL RAIL - POWER CONVERSION



V0.85A_VAL_MAR RAIL - POWER CONVERSION



Low Dropout, 400mA Adjustable
Linear Regulator



[PAGE_TITLE= V1.05A_VAL AND V0.85A_VAL_MAR RAIL GENERATION]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.257
Tue Sep 03 14:17:26 2013

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	257	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

STF_MTG_HOLE
EMPTY
MH6J1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH1B1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH6F1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH1J1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH6A1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
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MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
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NC9 9
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G39082-001

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MH9J1
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NC9 9
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MH9F1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

TH1D1
EMPTY
MTG_HOLE
MH1
MH1
NA_44528

ADDED FOR MEMORY INTERPOSER

[PAGE_TITLE=MOUNTING HOLES]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.258
Wed Dec 18 18:09:26 2019

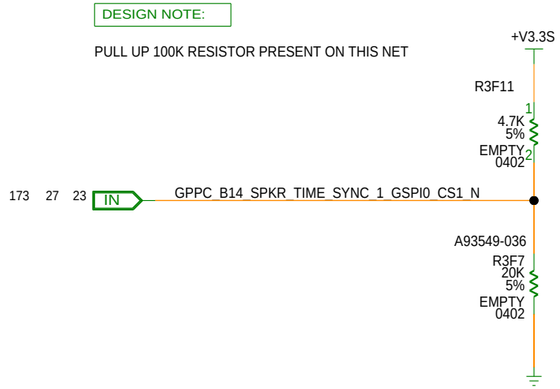
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	258	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:

PULL UP 100K RESISTOR PRESENT ON THIS NET



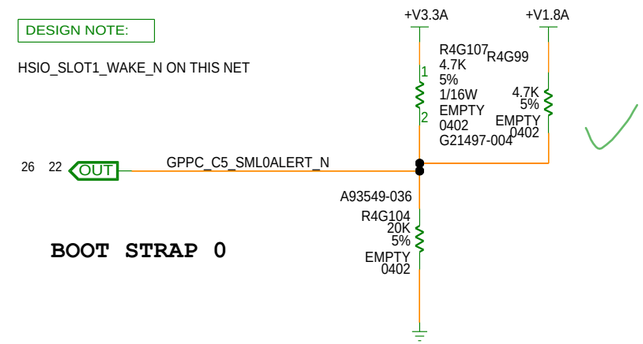
TOP SWAP OVERRIDE

HIGH- TOP SWAP ENABLED
LOW-DISABLED

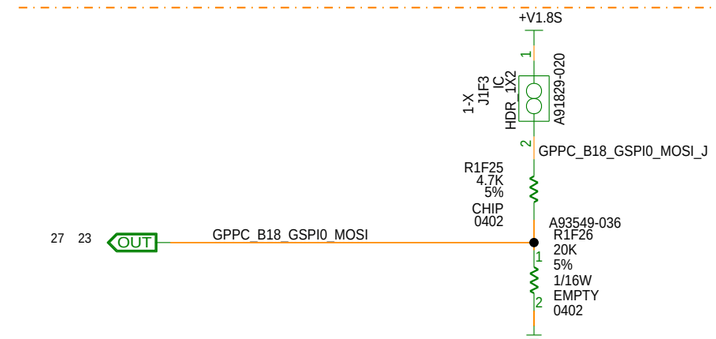
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

DESIGN NOTE:

HSIO_SLOT1_WAKE_N ON THIS NET



BOOT STRAP 0

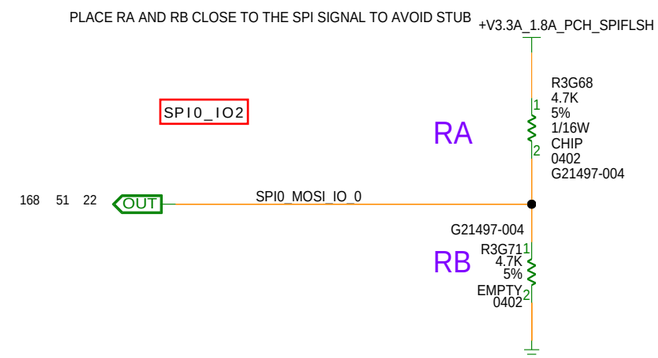


NO REBOOT

HIGH - NO REBOOT
LOW- REBOOT ENABLED
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

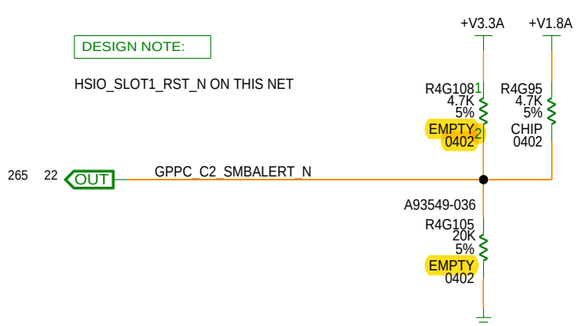
CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



DESIGN NOTE:

HSIO_SLOT1_RST_N ON THIS NET



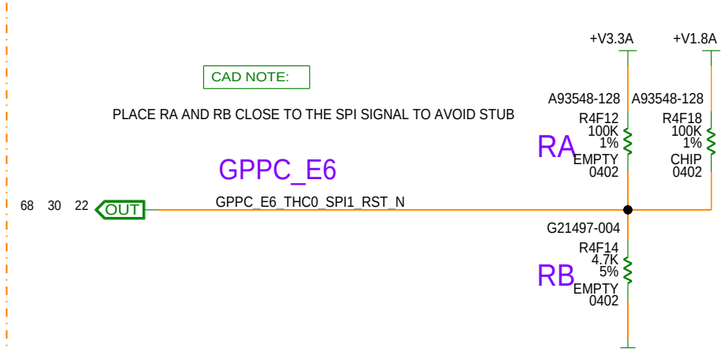
TLS CONFIDENTIALITY

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



[PAGE_TITLE=PCH STRAPS 1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.259
Wed Dec 18 18:09:27 2019

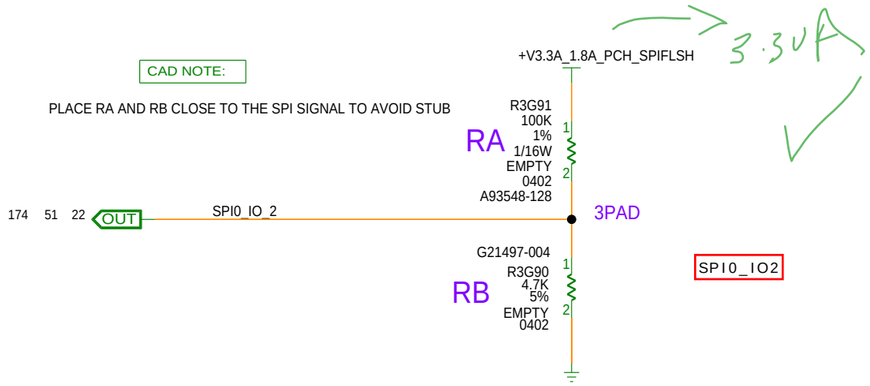
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	259	1.0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

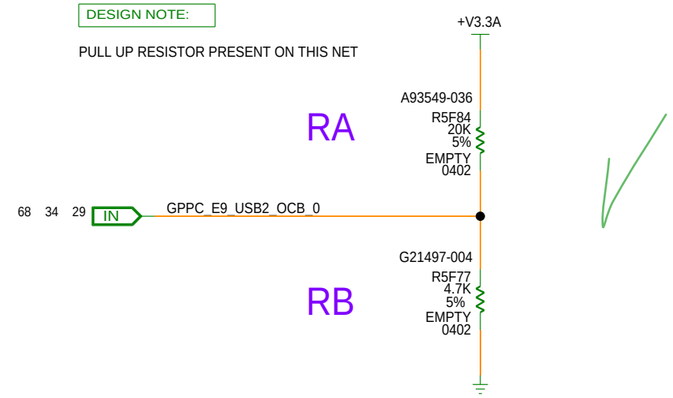
CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



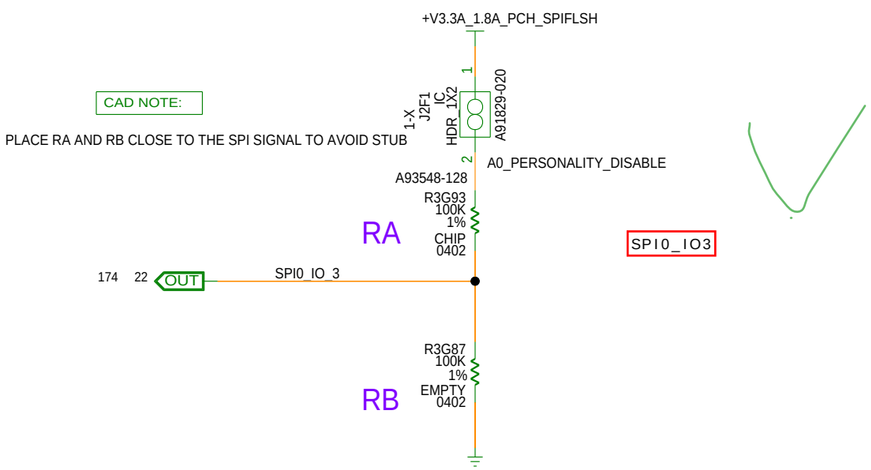
DESIGN NOTE:

PULL UP RESISTOR PRESENT ON THIS NET



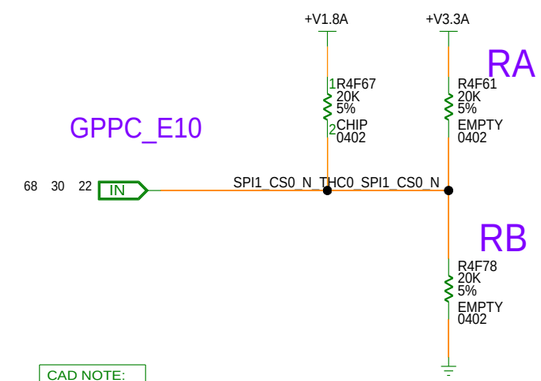
CAD NOTE:

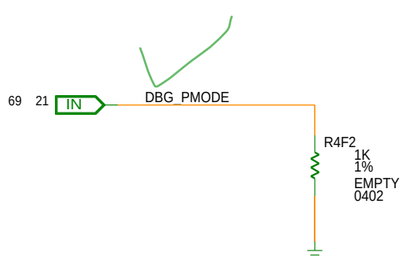
PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



CAD NOTE:

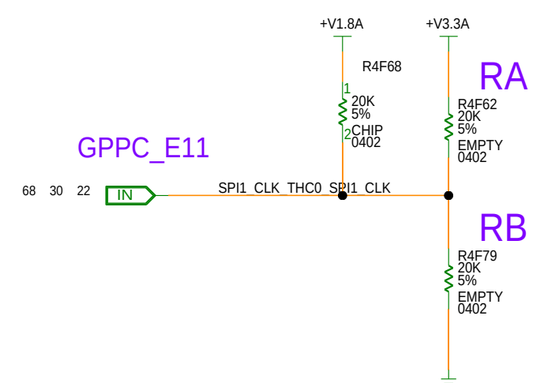
PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB





CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



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BPAGE DRAWING

tigerlake_u_ddr4.sch_1.260
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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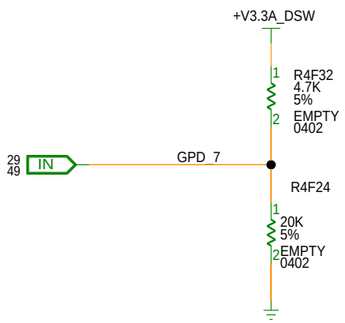
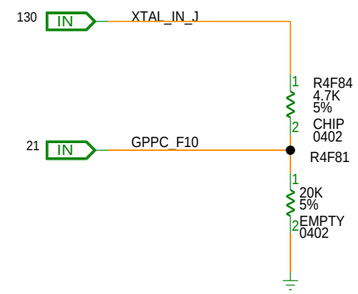
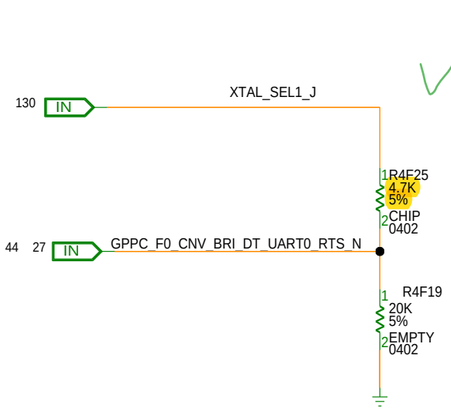
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE







XTAL SEL1

LOW: 38.4/19.2MHZ (DEFAULT)

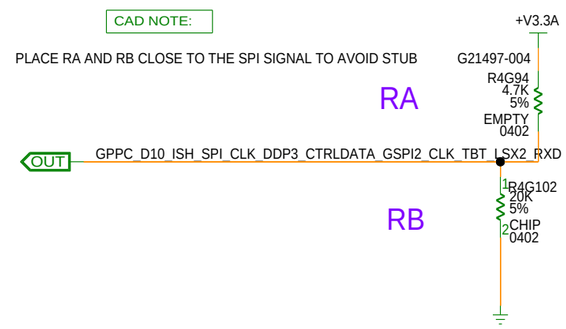
HIGH = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



TBT LSX #2 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

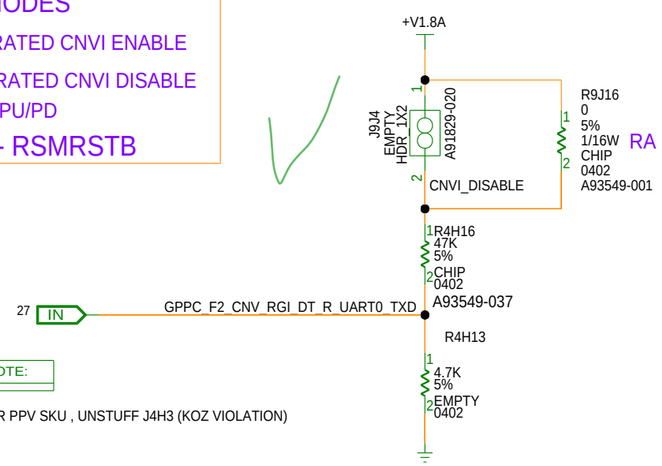
M.2 CNVI MODES

LOW-> INTEGRATED CNVI ENABLE

HIGH-> INTEGRATED CNVI DISABLE

NO INTERNAL PU/PD

SAMPLING - RSMRSTB



DESIGN NOTE:

STUFF RA FOR PPV SKU , UNSTUFF J4H3 (KOZ VIOLATION)

TBT LSX #3 PINS VCCIO CONFIGURATION

HIGH: 3.3V

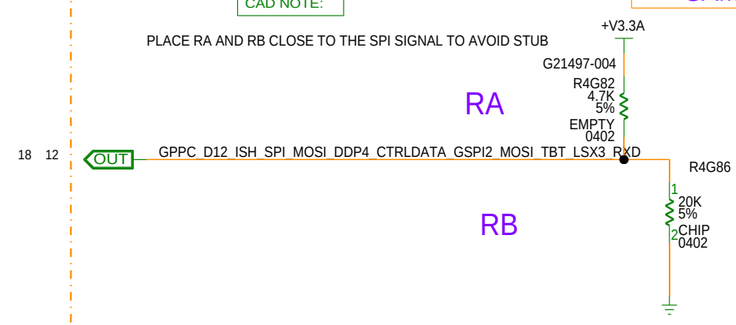
LOW: 1.8V

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



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BPAGE DRAWING

tigerlake_u_ddr4.sch_1.261

Wed Dec 18 18:09:28 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	261	1.0

CUSTOM TEXT BPAGE

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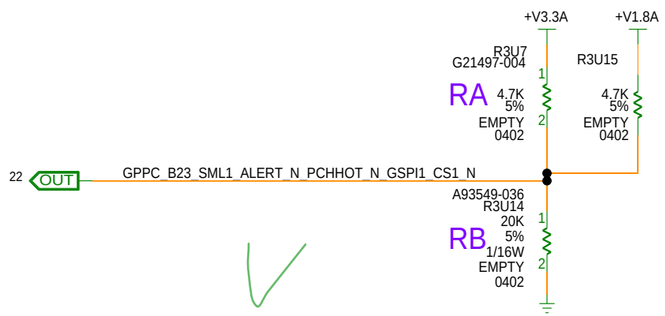
MODULE NAME	REV	DATE



CPUNSSC CLOCK FREQ

HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)

LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)

WEAK INTERNAL PD 20K

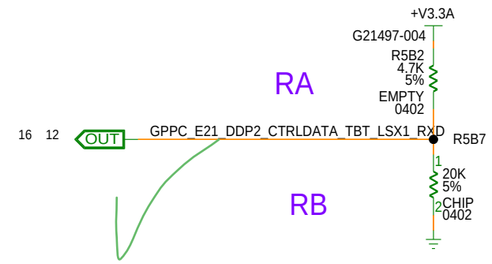
SAMPLING - RSMRSTB

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



TBT LSX #1 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

FOR UNFUSED A0 SILICON STUFF 1-X

FLASH DESCRIPTOR SECURITY OVERRIDE

HIGH: OVERRIDEN

LOW: SECURITY MEASURES NOT OVERRIDEN

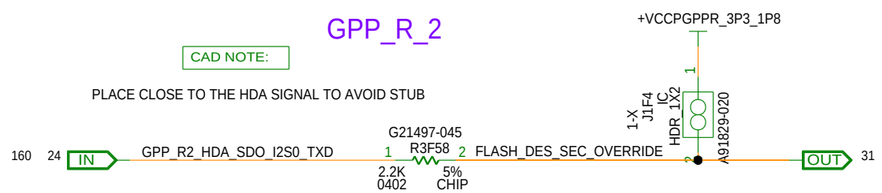
WEAK INTERNAL PD 20K

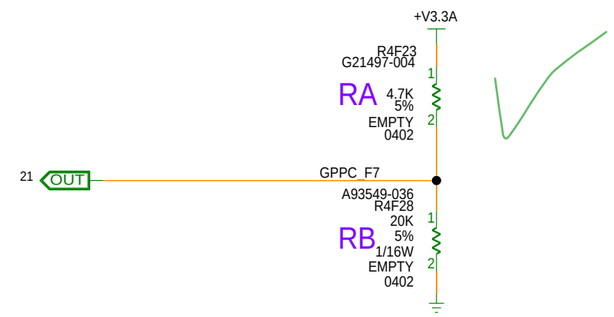
SAMPLING- PCH_PWROK

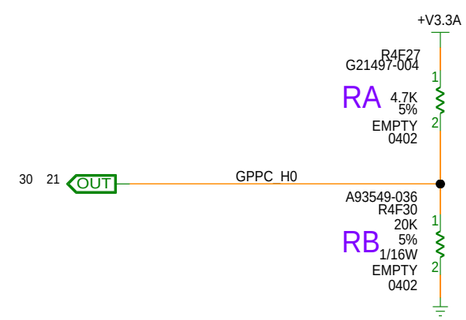
GPP_R_2

CAD NOTE:

PLACE CLOSE TO THE HDA SIGNAL TO AVOID STUB







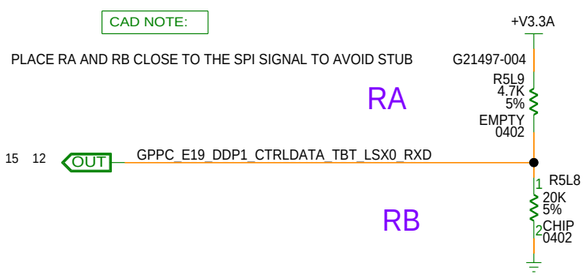
BFX STRAP 1- BIT 2

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



TBT LSX #0 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

[PAGE_TITLE=PCH STRAPS 4]

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.262

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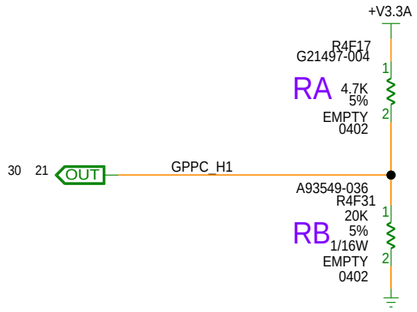
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	262	1.0

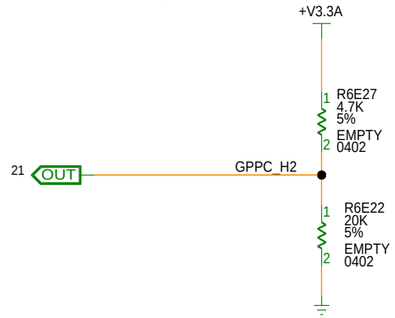
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



BFX STRAP 2- BIT 3

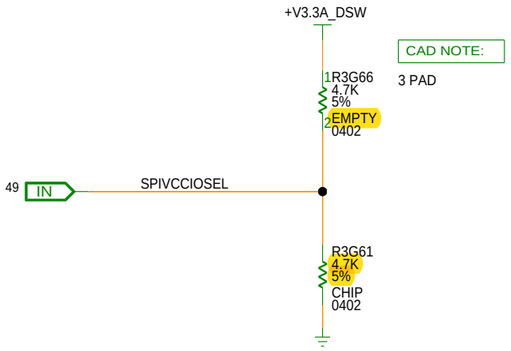
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB



BFX STRAP 3- BIT 4

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

STRAP FOR SPI 1.8V/3.3V SELECTION



CAD NOTE:

3 PAD

LOW-> 3.3 V

HIGH-> 1.8 V

NO TERMINATION
NOT SAMPLED

DEFAULT 3.3V

[PAGE_TITLE=PCH STRAPS 5]

BPAGE DRAWING
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TTK3 UNIFIED HEADER

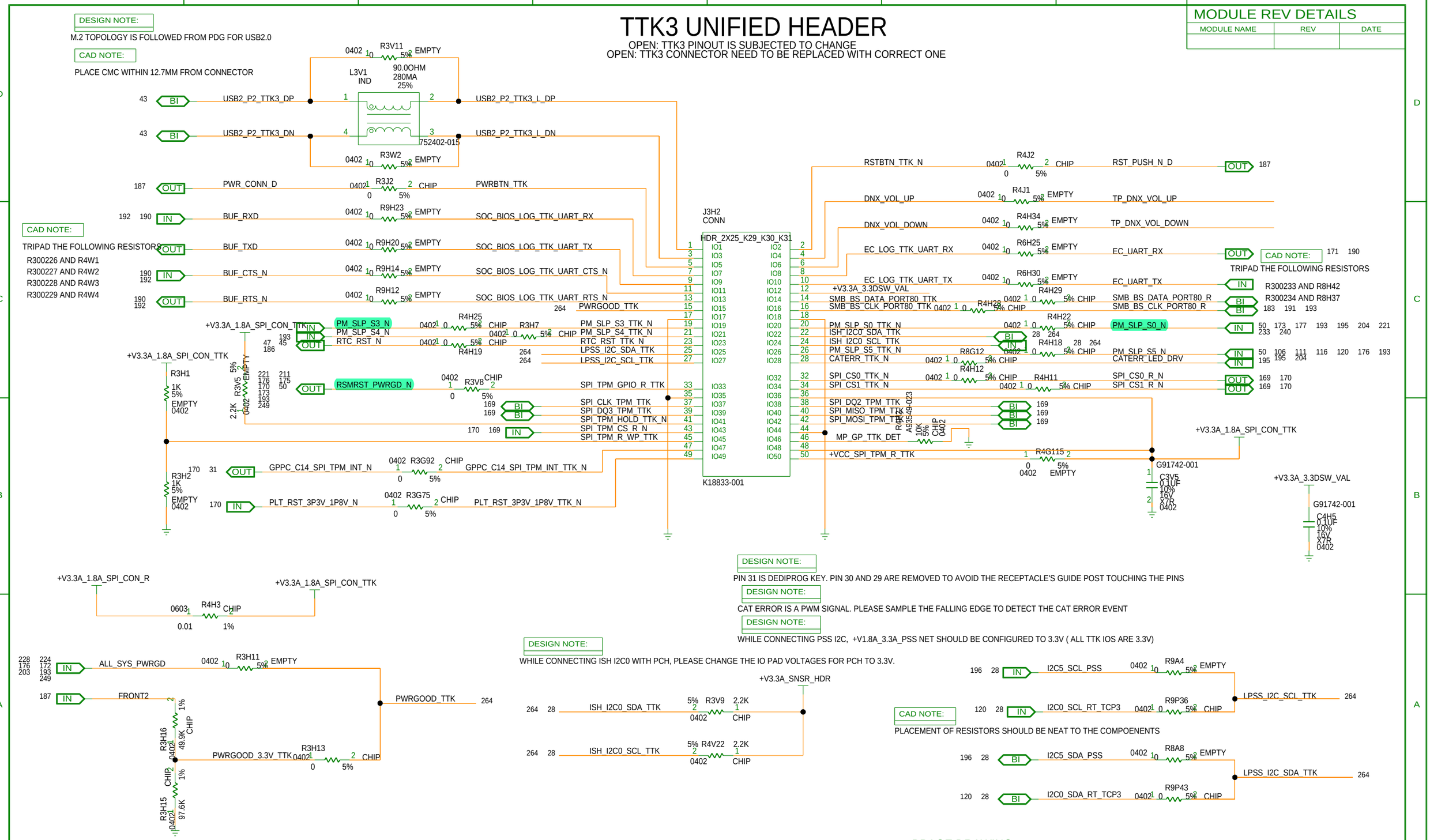
OPEN: TTK3 PINOUT IS SUBJECTED TO CHANGE
OPEN: TTK3 CONNECTOR NEED TO BE REPLACED WITH CORRECT ONE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:
M.2 TOPOLOGY IS FOLLOWED FROM PDG FOR USB2.0

CAD NOTE:
PLACE CMC WITHIN 12.7MM FROM CONNECTOR

CAD NOTE:
TRIPAD THE FOLLOWING RESISTORS
R300226 AND R4W1
R300227 AND R4W2
R300228 AND R4W3
R300229 AND R4W4



[PAGE_TITLE=TTK3 UNIFIED HEADER]

BPAGE DRAWING
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	609003	274	1.0

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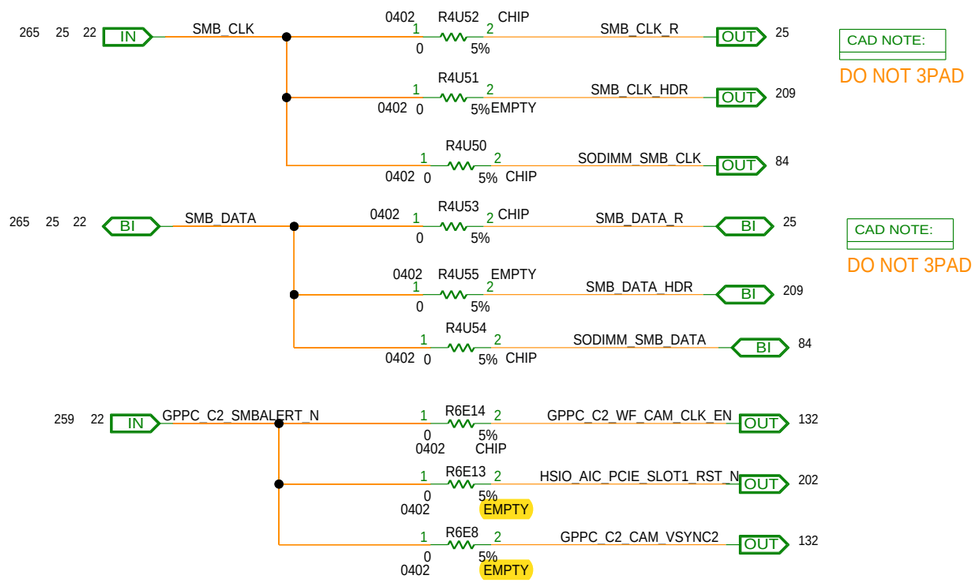
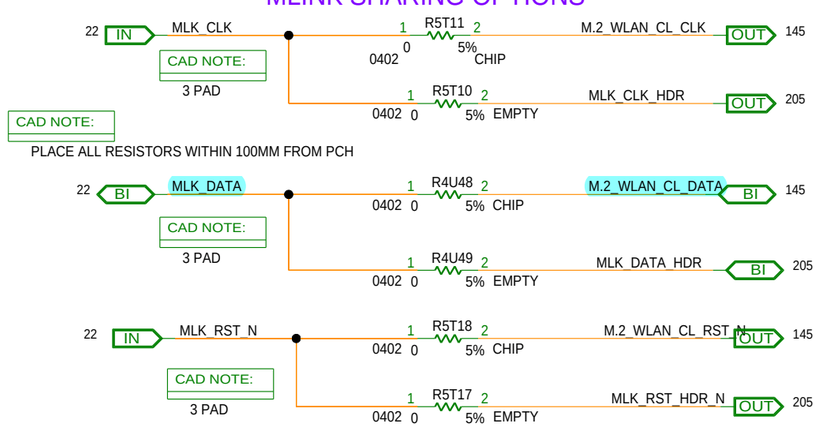
SMBUS SHARING OPTIONS



CAD NOTE:
DO NOT 3PAD

CAD NOTE:
DO NOT 3PAD

MLINK SHARING OPTIONS



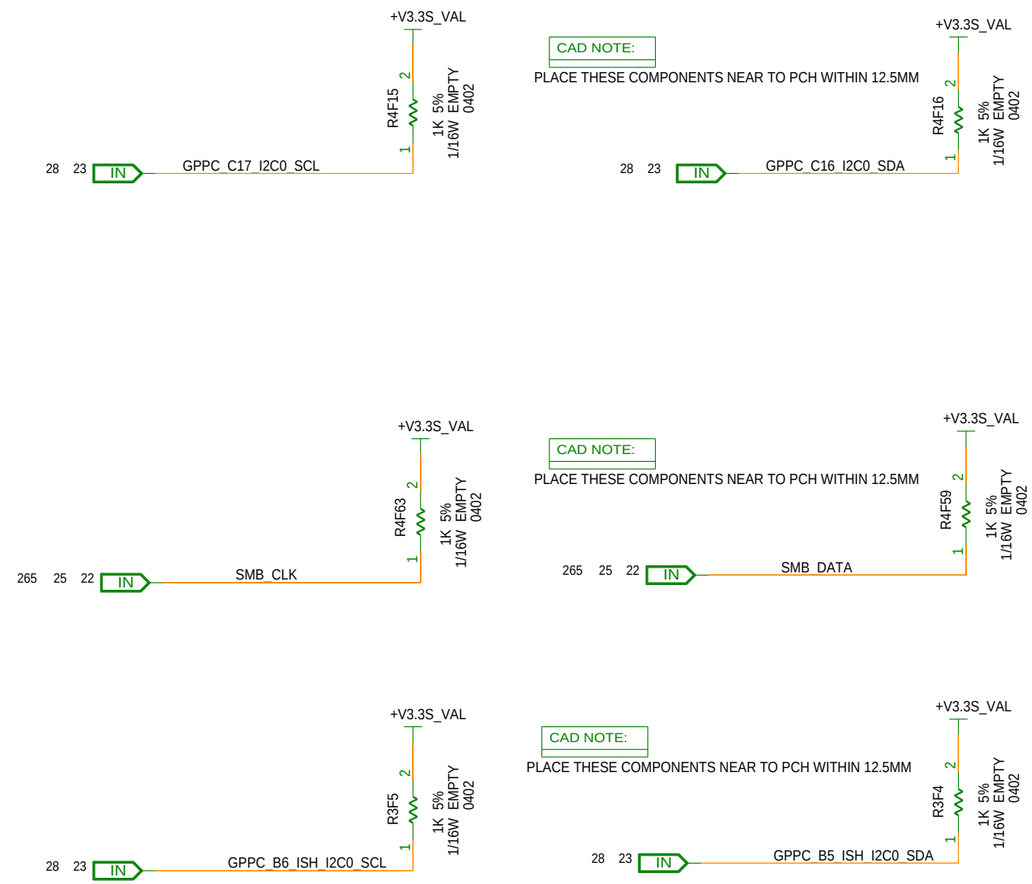
CAD NOTE:
3 PAD

CAD NOTE:
PLACE ALL RESISTORS WITHIN 100MM FROM PCH

CAD NOTE:
3 PAD

CAD NOTE:
3 PAD

WBIO TESTING OPTIONS



CAD NOTE:
PLACE THESE COMPONENTS NEAR TO PCH WITHIN 12.5MM

CAD NOTE:
PLACE THESE COMPONENTS NEAR TO PCH WITHIN 12.5MM

CAD NOTE:
PLACE THESE COMPONENTS NEAR TO PCH WITHIN 12.5MM

CAD NOTE:
PLACE THESE COMPONENTS NEAR TO PCH WITHIN 12.5MM

MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE= SHARING OPTIONS - MLINK, SMBUS

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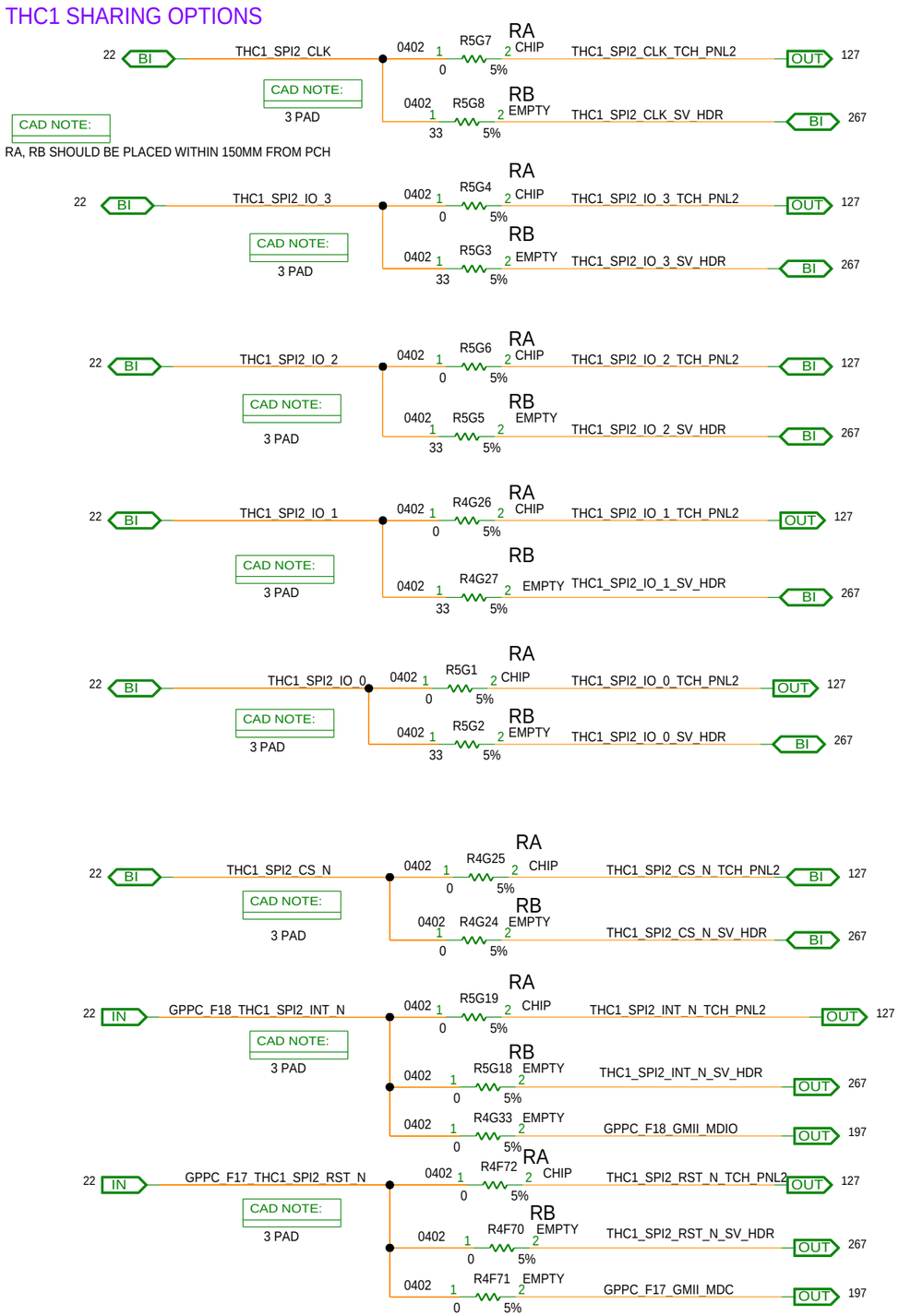
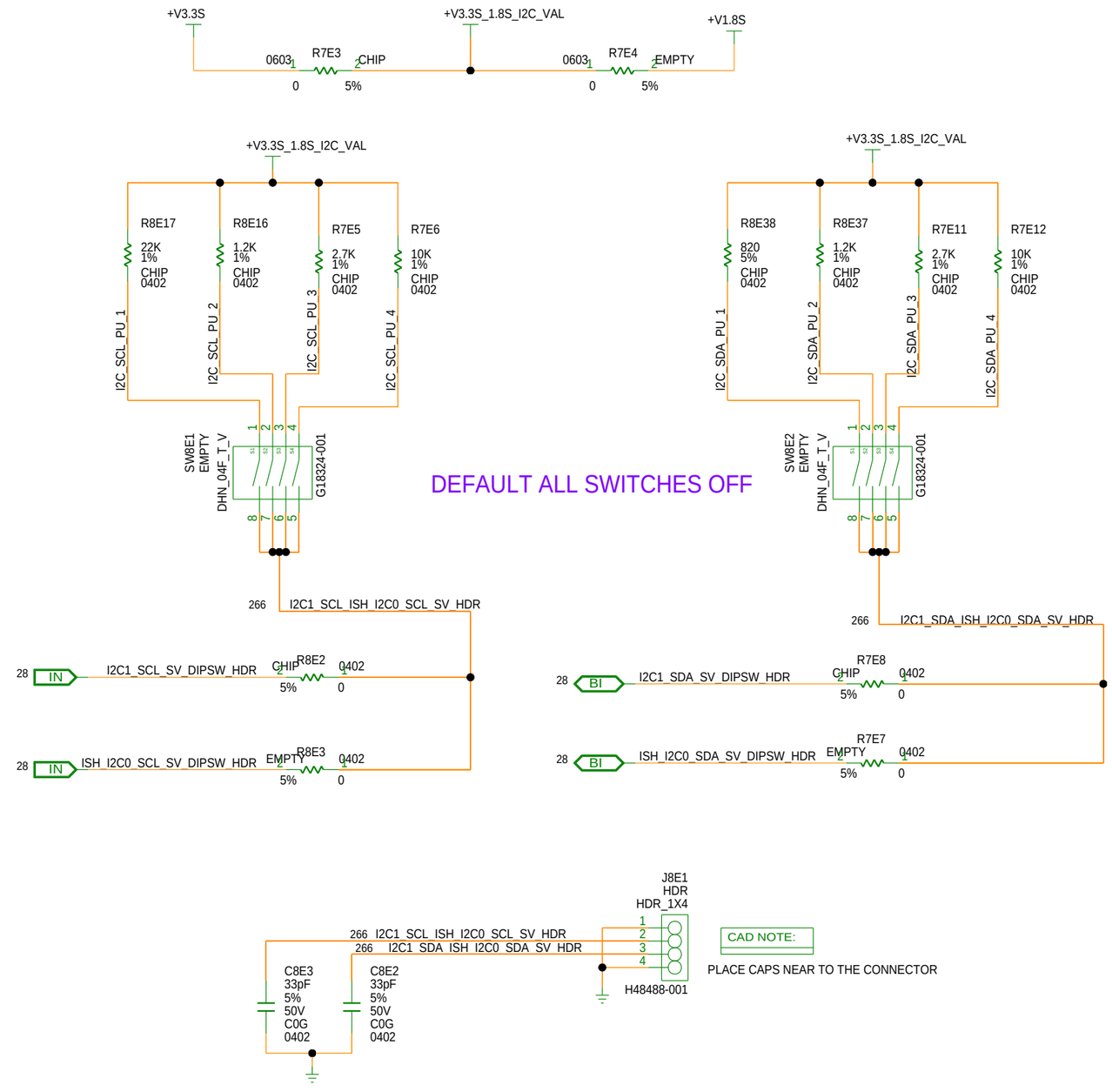
MODULE REV DETAILS		
MODULE NAME	REV	DATE

THC1 SHARING OPTIONS



I2C SV OPTIONS



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MODULE REV DETAILS		
MODULE NAME	REV	DATE

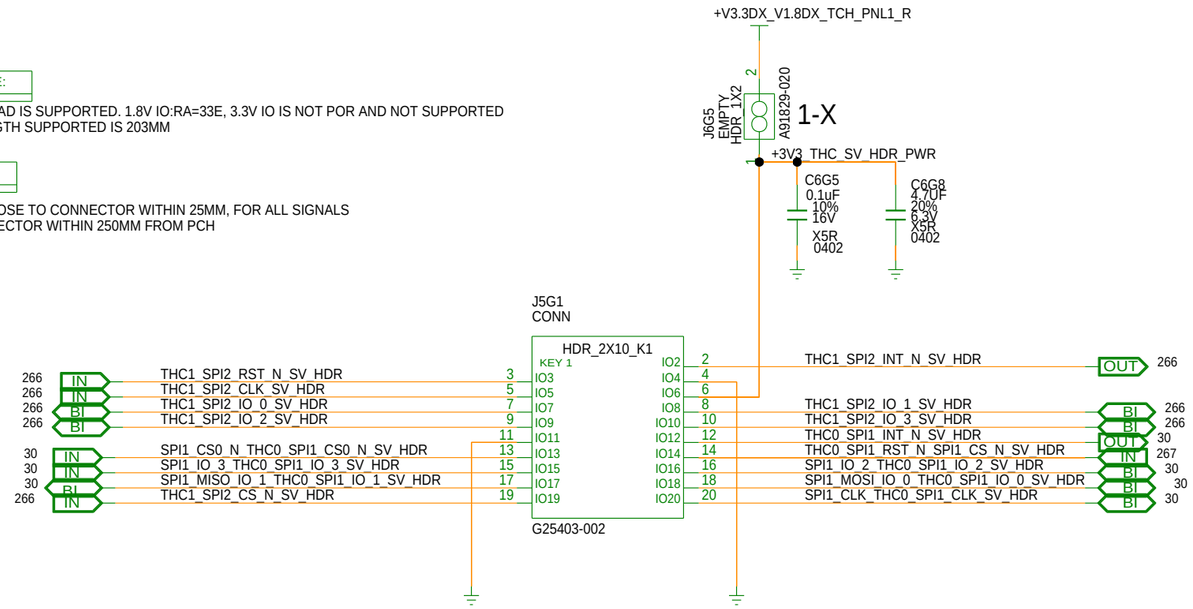
THC0 , THC1 AND SPI1 SV VALIDATION HEADER

DESIGN NOTE:

ONLY SINGLE LOAD IS SUPPORTED. 1.8V IO:RA=33E, 3.3V IO IS NOT POR AND NOT SUPPORTED
MAX CABLE LENGTH SUPPORTED IS 203MM

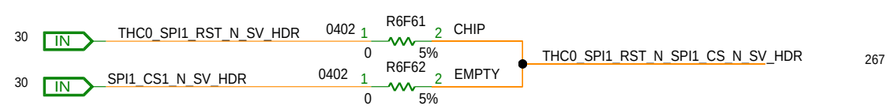
CAD NOTE:

PLACE RA CLOSE TO CONNECTOR WITHIN 25MM, FOR ALL SIGNALS
PLACE CONNECTOR WITHIN 250MM FROM PCH



DESIGN NOTE:

ON LKF, SPI1 CS1 AND THC0 RESET ARE MULTIPLEXED. HENCE SAME OPTION IS MAINTAINED VIA RESISTOR STUFFING REWORK ON TGL FOR UNIFICATION BETWEEN PLATFORMS



[PAGE_TITLE= SV HEADERS - THC0 SPI1, THC1]

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	609003	277	1.0

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