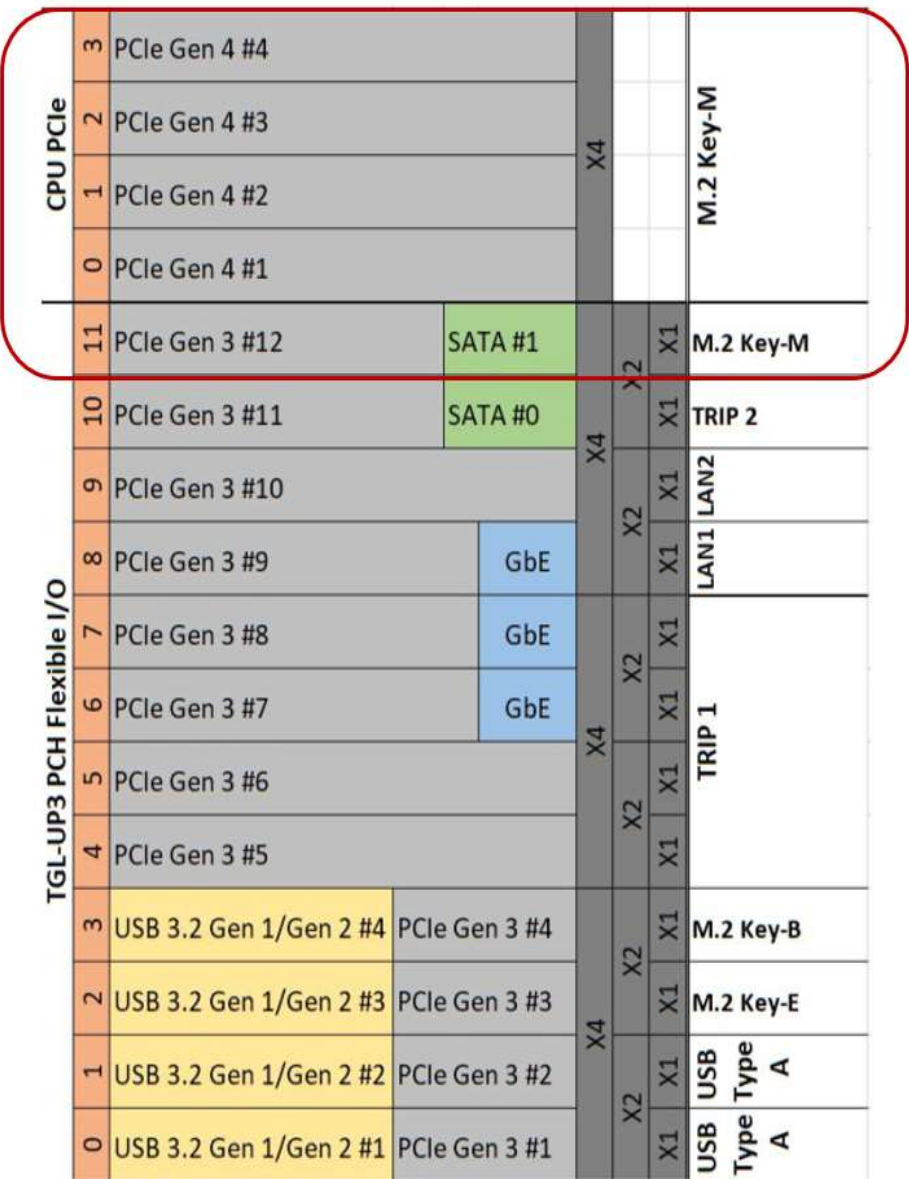


OPTION 1: TRIP1 is PCIe x4, TRIP2: PCIe x1 or SATA
OPTION 2: TRIP1 is 2x(Pcie x1), TRIP2: only SATA



SSD (NVMe Gen 4)

PCIE12

PCIE11

Could be (PCIE3 x1) or (SATA#0)

Indication from M.2 to CPU: SATA/PCIE0

PCIE10

I210 (Symbol 9 OF 21)

PCIE9

I219 (Only Phy, Mac Inside PCH)

TRIP 1 & 2:

FT.CA-LAN4
FT.C-LAN2
FT.EC-USB2V4
FT.ED-USB3PCIV4
FT.F-M2NVME
FT.HA-SER1
FT.H-SER4
FT.I-M2B
FT.J-M2E
FT.L-PCIEmini
FT.M-TBT2
FT.N-PCIEx16
FT.Q-CAN
FT.S-GPIO
FT.T-SATA1
FT.U-POE2
FT.W-OPLN2

WWAN

PCIE4

WiFi/BT

PCIE3

USB 3.2 Gen 2 (10 Gb/s) PORT 1 USB 3.2 Gen 2 (10 Gb/s) PORT 1 - B2B

USB 3.2 Gen 2 (10 Gb/s) PORT 1 USB 3.2 Gen 2 (10 Gb/s) PORT 2 - B2B

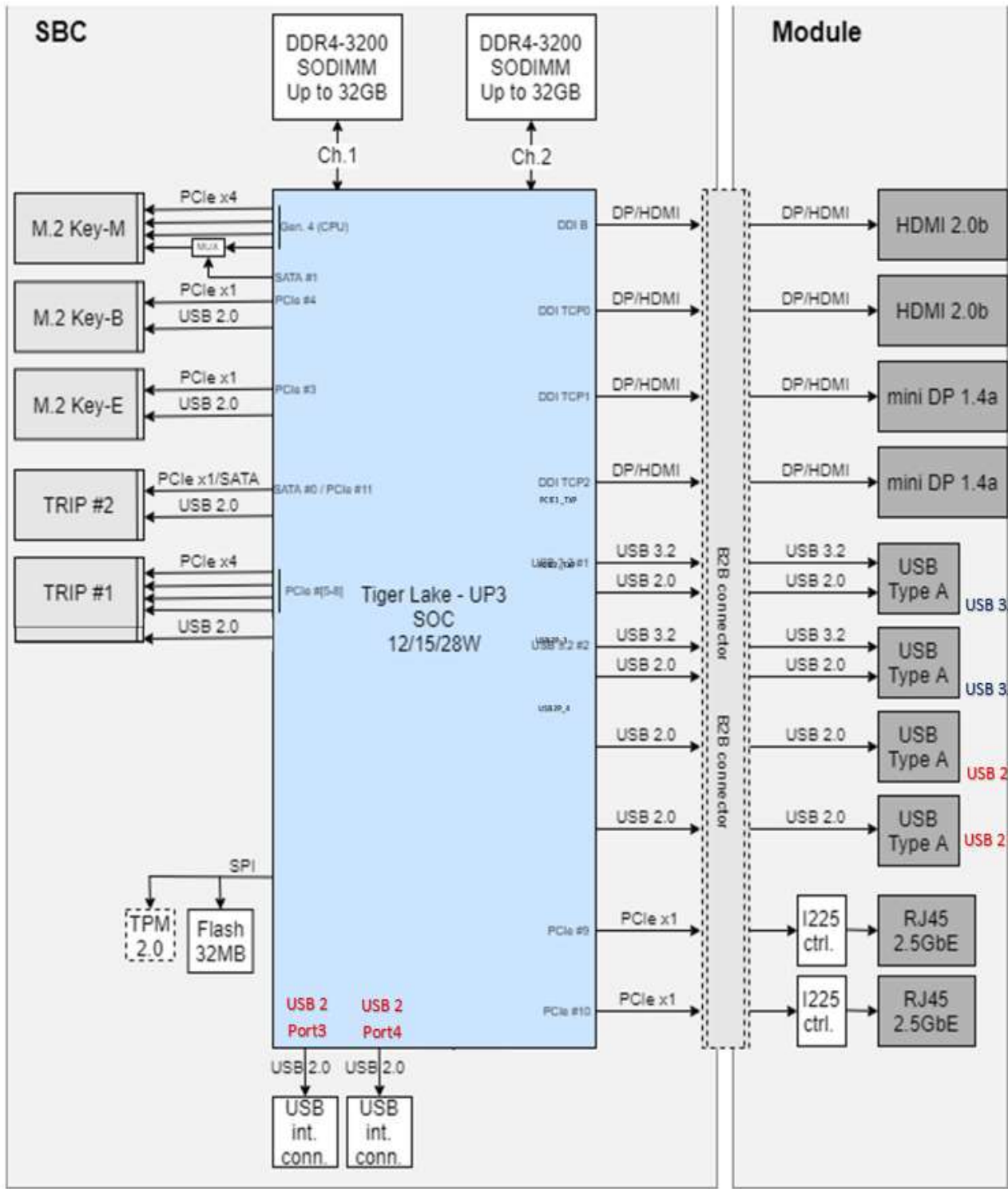
Tiger Lake UP3 Platform

Tiger Lake UP3 Key Feature Summary

Feature	Description
Thermal (SoC)	UP3 4+2: 15W
SoC	TGL UP3 CPU (4+2) PCH - LP
CPU IO	PCIe Gen4, 4x Type-C (TBT, USB 4.0, DP), DDR4, LPDDR4x, LPDDR5, CSI, DSI, DDI, eDP
PCH-LP	12 lanes HSIO, USB2, USB 3.2, eSPI, SPI, LPSS, I2C, SMBus
Power Delivery	CPU FIVR/PCH FIVR w/discrete VR ROP USB-C PD Controller
Memory	DDR4 - Max 64GB @ 3200MT/s LPDDR4x - Max 32GB @ 4266MT/s
Storage	PCIe/SATA
Boot	SPI NOR
Discrete Graphics	Optional x4 PCIe - Hybrid Graphics support w/Hot Plug
Internal Display	eDP, MIPI DSI
External displays	4 Wired Type-C (DP/TBT) Wireless (Miracast2.0 r2) (Wi-Fi) DDI(DP, HDMI)
Wireless	Quasar CNVi w/Harrison Peak (Wi-Fi/BT) module WWAN - XMM 7560
Clocking	38.4MHz Platform Xtal
Wired COMMS	Integrated GbE w/ discrete Gbit Lan Phy

continued...

Feature	Description
Imaging	4x WF/UF 2D Camera - (13MP WF, 2MP UF, 2MP Others) Other Cameras: AutoFocus, Face Tracking, Image Biometrics
Docking/Walk-up-Port	4x Ports Max: Type-C/Type-A
Audio	3.5mm Headphone Jack, Integrated Speakers/Mic, Docking Soundwire, Intel HD Audio, I2S, USB
Sensors	Ambient Light Sensor, Gyroscope, Accelerometer, Compass, Proximity, Pressure
Misc, GPIO's	Power/Vol button/Indicator LEDs/Keyboard/Touchpad/etc



ZZ1

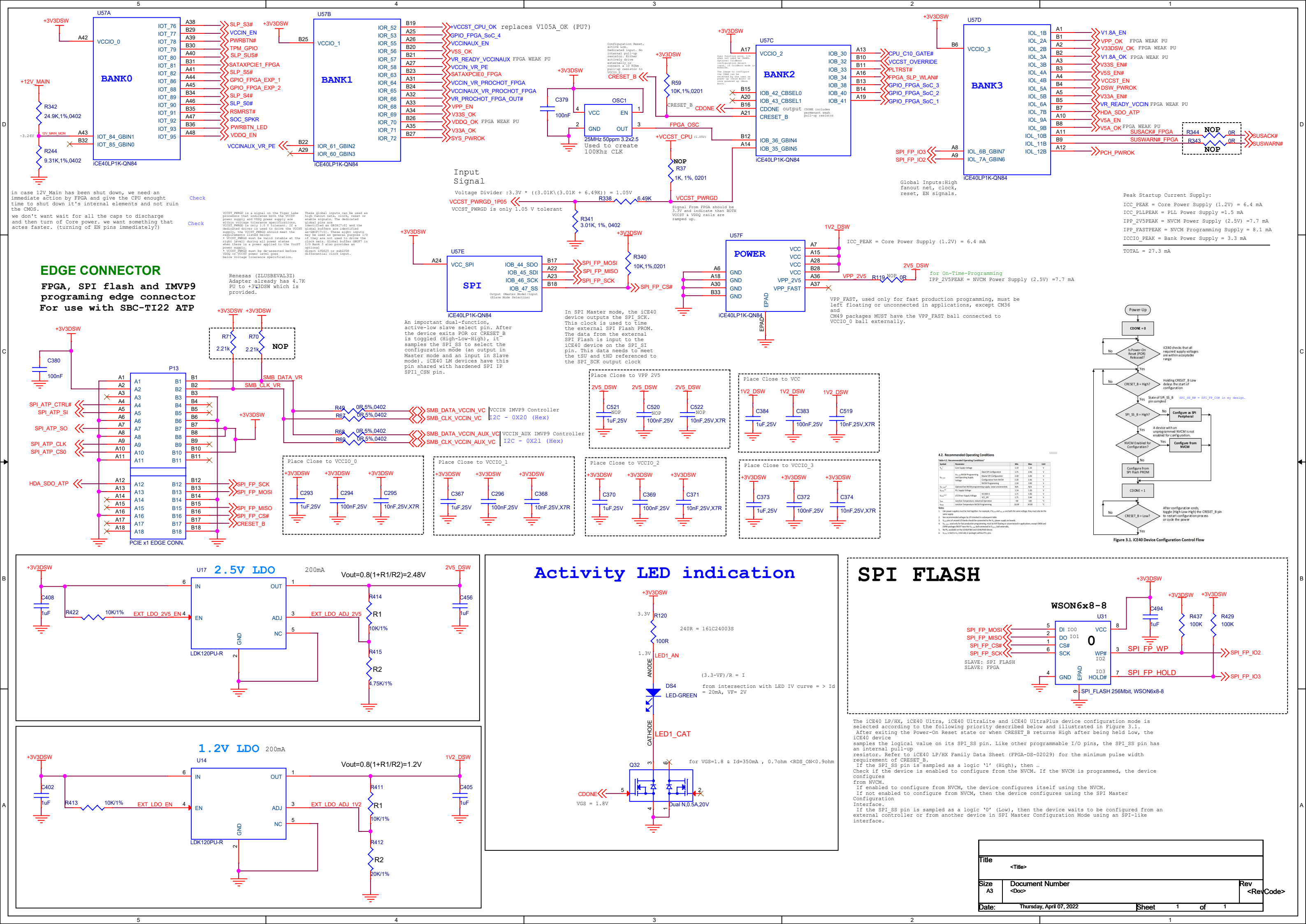
P/N = 188210030

PARSER_VERSION_1.0

PCB1

PCB, SBC-TI22, Rev 1.0

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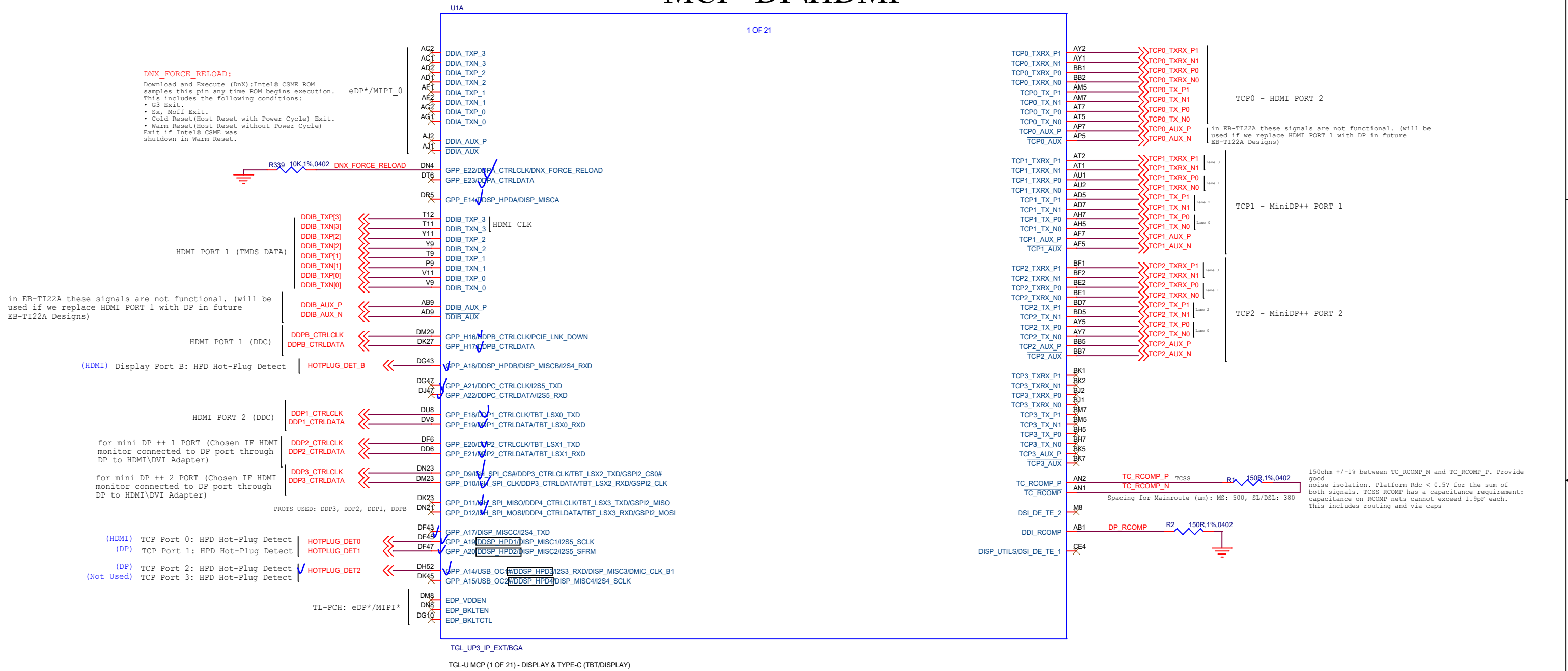


TIGER LAKE PCH:

- The PCH provides extensive I/O support. The functions and capabilities include:
- ACPI Power Management Logic Support, Revision 5.0a
 - PCI Express Base Specification Revision 3.0
 - Integrated Serial ATA Host controller 3.2, supports data transfer rates of up to 6 Gb/s on all ports
 - USB 3.2 Gen 2x1 (10 Gb/s) eXtensible Host Controller (xHCI)
 - USB 3.2 Gen 1x1 (5 Gb/s) Dual Role (eXtensible Device Controller - xDCI) Capability
 - Serial Peripheral Interface (SPI)
 - Enhanced Serial Peripheral Interface (eSPI)
 - Flexible I/O-Allows some high speed I/O signals to be configured as PCIe or USB 3.2
 - General Purpose Input Output (GPIO)
 - Interrupt controller
 - Timer functions
 - System Management Bus (SMBus) Specification, Version 2.0
 - Integrated Clock Controller (ICC)/Real Time Clock Controller (RTCC)
 - Intel® High Definition Audio and Intel® Smart Sound Technology (Intel® SST), supporting I2S, MIPI* SoundWire*, and DMIC
 - Intel® Serial I/O UART Host controllers
 - Intel® Serial I/O I2C Host controllers
 - Integrated 10/100/1000 Gigabit Ethernet MAC
 - Integrated Sensor Hub (ISH)
 - Supports Intel® Rapid Storage Technology (Intel® RST)
 - Supports Intel® Active Management Technology (Intel® AMT) (AMT)
 - Supports Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
 - Supports Intel® Trusted Execution Technology (Intel® TXT)
 - JTAG Boundary Scan support
 - Intel® Trace Hub (Intel® TH) and Direct Connect Interface (DCI) for debug
 - Supports Intel® CSME (CSME)
 - Supports Integrated connectivity (CNVi)



MCP -DP\HDMI



Name	Type	Description
GPP_E14 / DDSP_HPDA / DISP_MISCA	I	Display Port A: HPD Hot-Plug Detect
GPP_A18 / DDSP_HPDB / DISP_MISCB / I2S4_RXD	I	Display Port B: HPD Hot-Plug Detect
GPP_A19 / DDSP_HPDI / DISP_MISC1 / I2S5_SCLK	I	TCP Port 1: HPD Hot-Plug Detect
GPP_A20 / DDSP_HPDI / DISP_MISC2 / I2S5_SFRM	I	TCP Port 2: HPD Hot-Plug Detect
GPP_A14 / USB_OC1# / DDSP_HPDI / I2S3_RXD / DISP_MISC3 / DMIC_CLK_B1	I	TCP Port 3: HPD Hot-Plug Detect
GPP_A15 / USB_OC2# / DDSP_HPDI / DISP_MISC4 / I2S4_SCLK	I	TCP Port 4: HPD Hot-Plug Detect

5.3

Display Interfaces

Table 33.

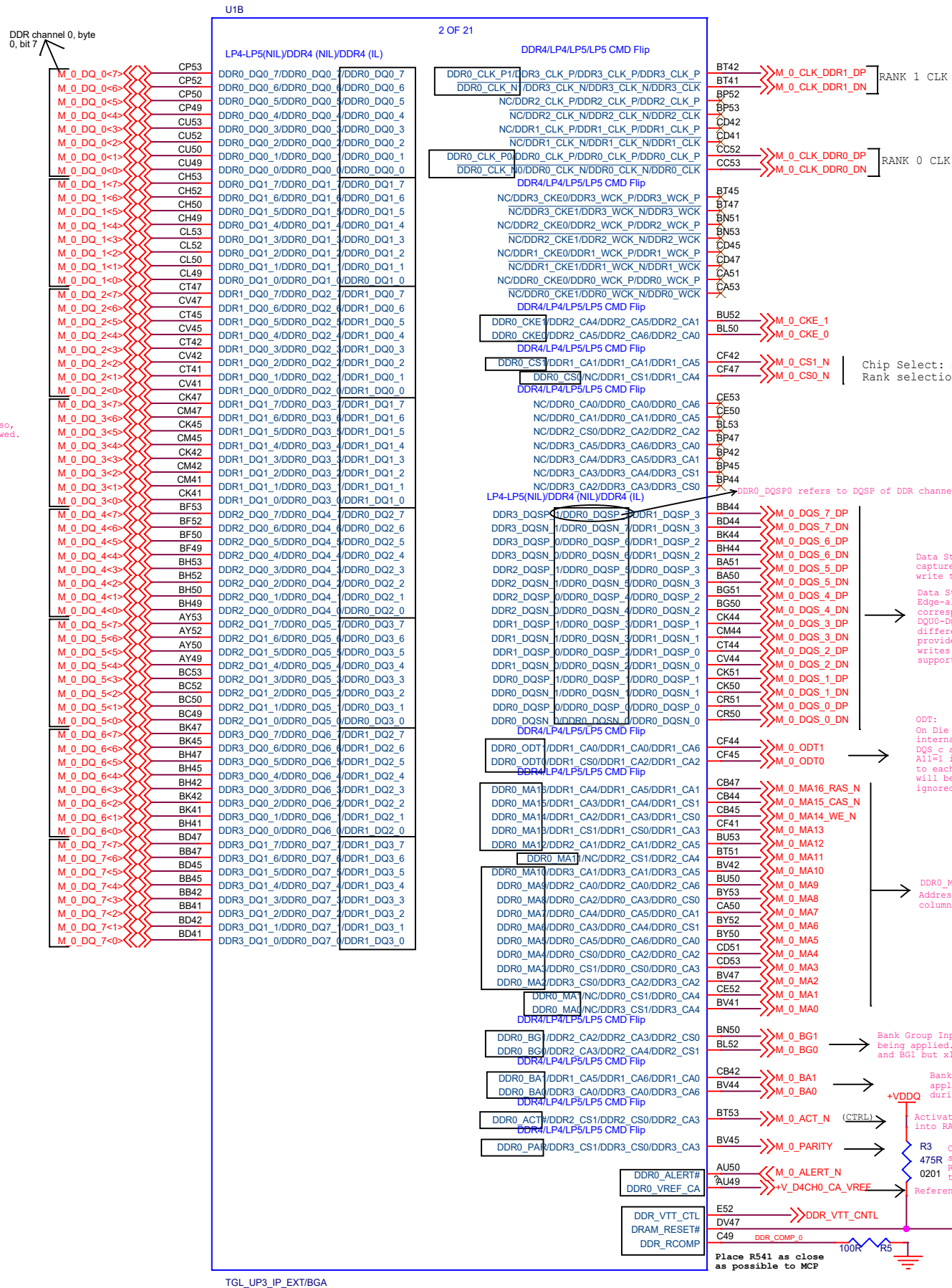
DDI Ports Availability

SKU	UP4 Processor Line	UP3 Processor Line
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	eDP*/DP*/HDMI*/MIPI_1	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*

Note: HBR3 supported on TCP ports only.
Each of the TCP port can support DPoC* (DisplayPort* over Type-C)

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MEMORY CHANNEL A



1.CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.
2.DQ Bit swapping is allowed within the same byte
3.Byte Swapping is allowed within the same channel
4.QDSP and DQSN differential signal swapping within a pair is not allowed.

NOTES:
Each lane of 8bits (Byte) of Data has it's own Data Strobe

1.CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.

Chip Select: All commands are masked when CS n is registered HIGH. CS n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.

Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during reading and write transactions.
Data Strobe: output with read data, input with write data.
Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQ10-DQ17; DQSU corresponds to the data on DQ00-DQ07. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

ODT:
On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A16P1 in MR11) signal for X8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_c, DQSU_t, DQSL_t, DQSL_c, DMU_n, and DMU_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.

DDR0_MA[16:0]
Address: These signals are used to provide the multiplexed row and column address to the SDRAM.

Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.

Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.

Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.

Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW.
Reference voltage for control, command, and address pins.

Pin Descriptions

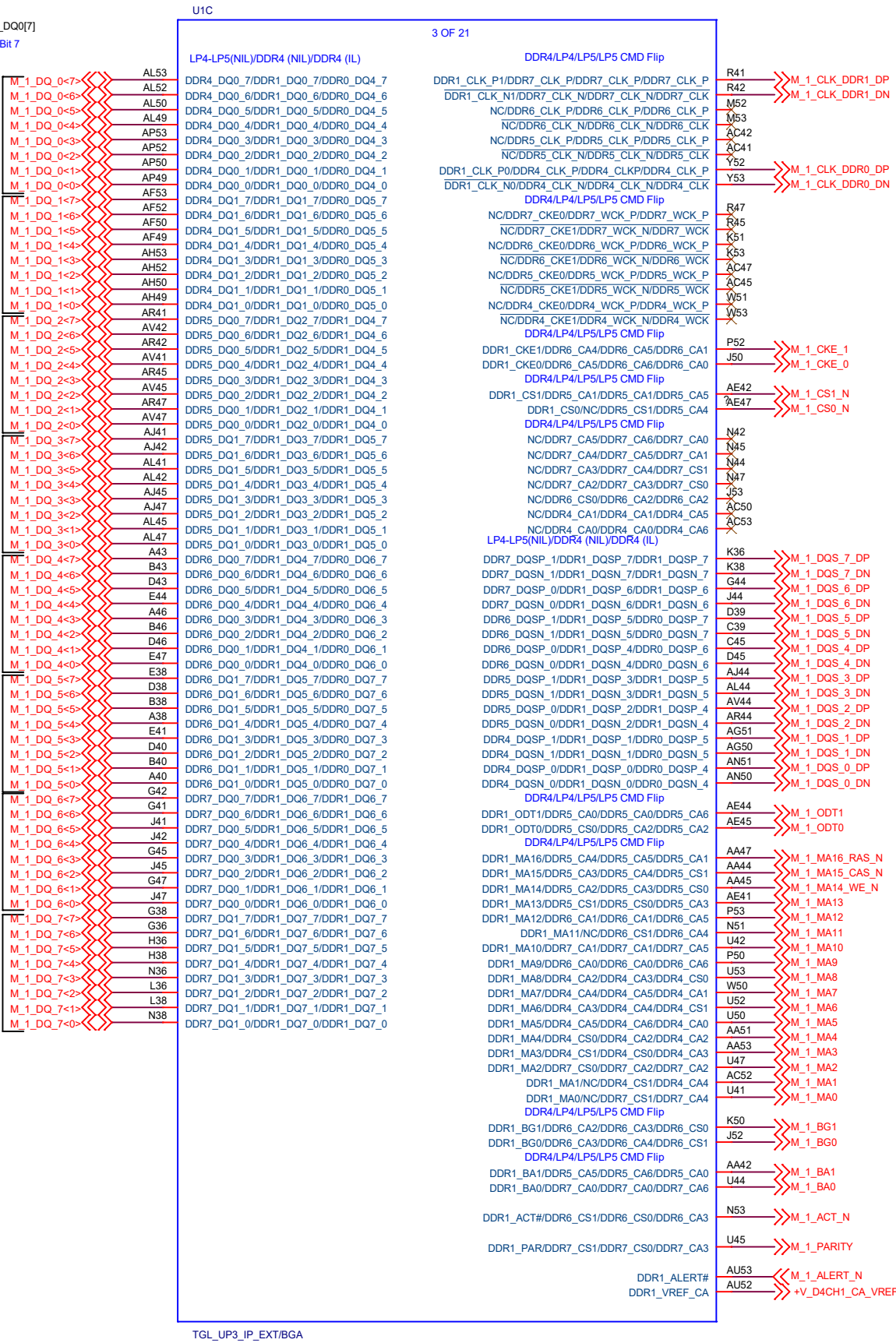
Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I ² C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I ² C serial data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0-SA2	I ² C slave address select for SPD/TS and register
RAS_n ²	Register row address strobe input	PAR	Register parity input
CAS_n ³	Register column address strobe input	VDD	SDRAM core power
WE_n ⁴	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

- RAS_n is a multiplexed function with A16.
- CAS_n is a multiplexed function with A15.
- WE_n is a multiplexed function with A14.

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MEMORY CHANNEL B

AL53: DDR4_DQ0[7]/DDR1_DQ0[7]
DDR channel 4(1), Byte 0, Bit 7



CATERR#

Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRS, CATERR# is asserted for 16 BCLKs. Legacy IERRS, CATERR# remains asserted until warm or cold reset.

PROCHOT#

The PROCHOT# (processor hot) signal is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling. The PROCHOT# signal can be configured to the following modes:

- Input Only: PROCHOT is driven by an external device.
- Output Only: PROCHOT is driven by processor.
- Bi-Directional: Both Processor and external device can drive PROCHOT signal

Time Synchronization GPIO 0: Timed GPIO event for time synchronization for interfaces that do not support time synchronization natively.

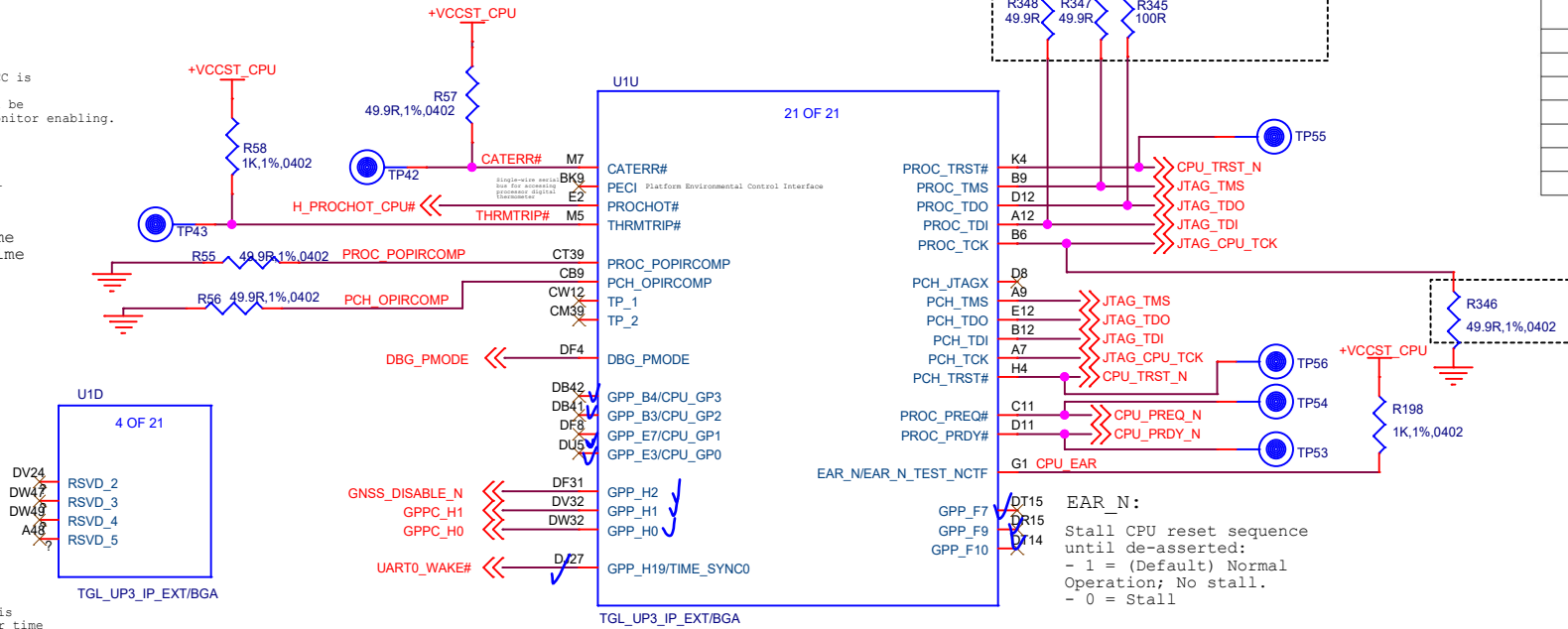
Time Synchronization: Used for synchronization both input (latch time when pin asserted) and output (toggle pin when programmed time is hit).

TIME_SYNC:

The PCH supports two Timed GPIOs as native function (TIME_SYNC) that is muxed on GPIO pins. The intent usage of the Timed GPIO function is for time synchronization purpose.

Timed GPIO can be an input or an output.

- As an input, a GPIO input event triggers the HW to capture the PCH Always Running Timer (ART) time in the Time Capture register. The GPIO input event must be asserted for at least two crystal oscillator clocks period in order for the event to be recognized.
- As an output, a match between the ART time and the software programmed time value triggers the HW to generate a GPIO output event and capture the ART time in the Time Capture register. If periodic mode is enabled, HW generates the periodic GPIO events based on the programmed interval. The GPIO output event is asserted by HW for at least two crystal oscillator clocks period.

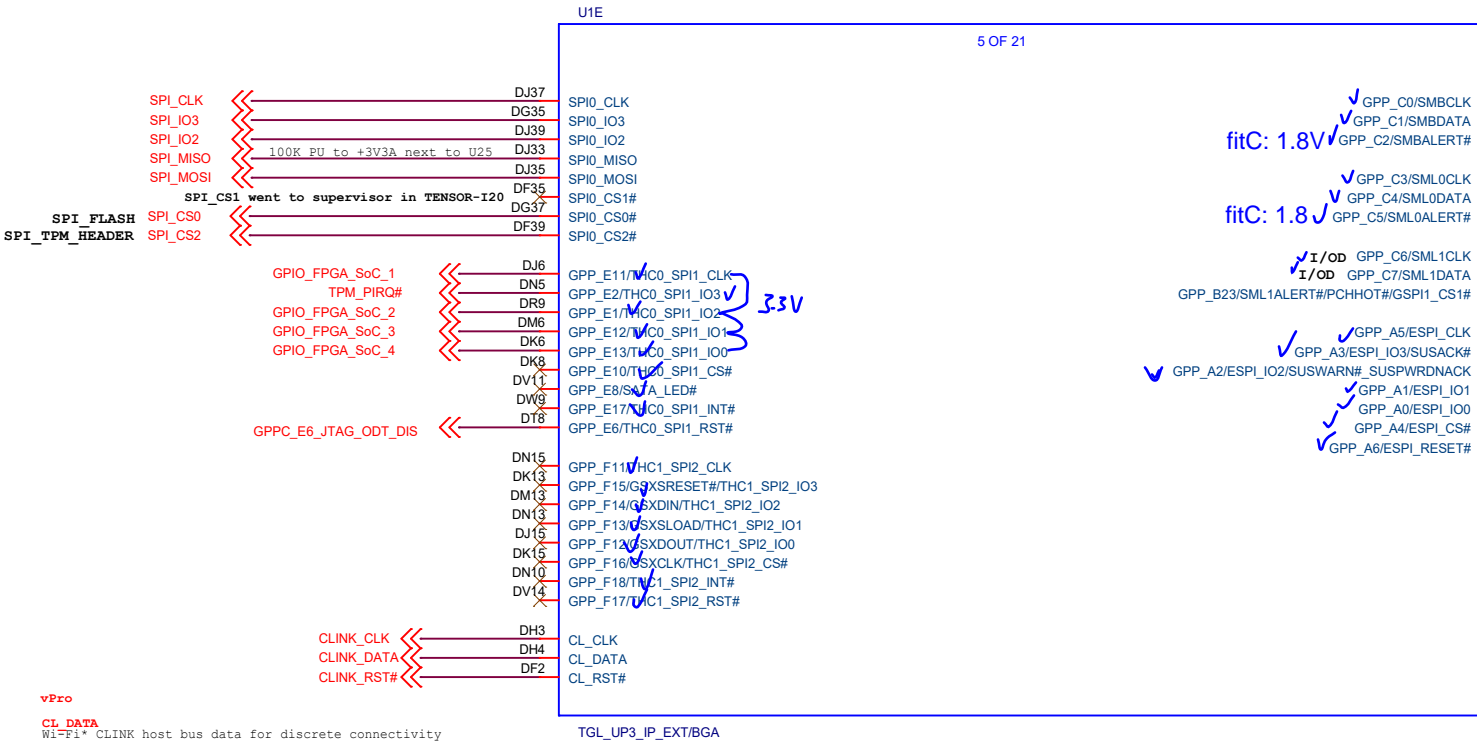


Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM#[3:0]	Pull Up/Pull Down	VCC _{ID_OUT}	16-60 Ω
PROC_PREQ#	Pull Up	VCC _{STG}	3 KΩ
PROC_TDI	Pull Up	VCC _{STG}	3 KΩ
PROC_TMS	Pull Up	VCC _{STG}	3 KΩ
PROC_TRST#	Pull Down	VCC _{STG}	3 KΩ
PROC_TCK	Pull Down	VCC _{STG}	3 KΩ
CFG[17:0]	Pull Up	VCC _{ID_OUT}	3 KΩ

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BPM#[3:0]	Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	UP3/UP4/H Processor Lines
PROC_PRDY#	Probe Mode Ready: PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	O	OD	SE	UP3/UP4/H Processor Lines
PROC_PREQ#	Probe Mode Request: PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TCK	Test Clock: This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal should be driven low or allowed to float during power on Reset.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TDI	Test Data In: This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TDO	Test Data Out: This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O	OD	SE	UP3/UP4/H Processor Lines
PROC_TMS	Test Mode Select: A JTAG specification support signal used by debug tools.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TRST#	Test Reset: Resets the Test Access Port (TAP) logic. This signal should be driven low during power on Reset. Refer to the appropriate processor Debug Port Design Guide (Refer to Section 1.10, "Related Documents") for complete implementation details.	I	GTL	SE	UP3/UP4/H Processor Lines

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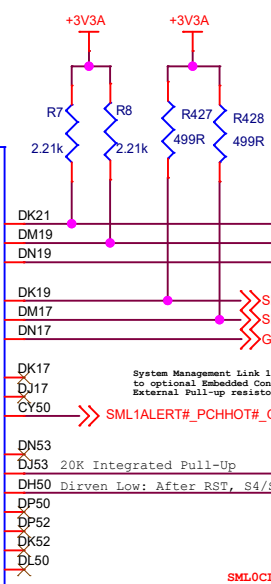


vPro
CL_DATA
Wi-Fi* CLINK host bus data for discrete connectivity with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK data pin on the Intel® vPro™ Wi-Fi* module.

CL_CLK
Wi-Fi* CLINK host bus clock for discrete connectivity with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK clock pin on the Intel® vPro™ Wi-Fi* module.

fitC: 1.8V
fitC: 1.8V

✓ GPP_C0/SMBCLK
✓ GPP_C1/SMBDATA
✓ GPP_C2/SMBALERT#
✓ GPP_C3/SML0CLK
✓ GPP_C4/SML0DATA
✓ GPP_C5/SML0ALERT#
✓ I/OD GPP_C6/SML1CLK
✓ I/OD GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#/GSP1_CS1#
✓ GPP_A5/ESPI_CLK
✓ GPP_A3/ESPI_I03/SUSACK#
✓ GPP_A2/ESPI_I02/SUSWARN# SUSPWRDNACK
✓ GPP_A1/ESPI_I01
✓ GPP_A0/ESPI_I00
✓ GPP_A4/ESPI_CS#
✓ GPP_A6/ESPI_RESET#



SML0CLK & SML0DATA
System Management Link clock signal interface to Intel® Ethernet Connection I219. Refer to System Management Interface and SMLink for details on the SML0CLK signal.
Note: The Intel® Ethernet Connection I219 connects to SML0CLK signal.

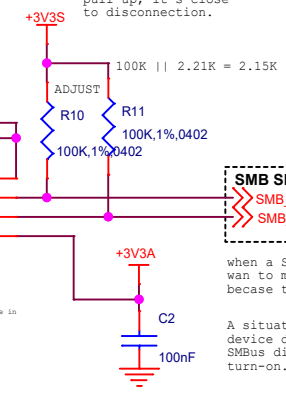
FUNCTIONALITY:
The SMLink interfaces are controlled by the Intel® CSME.
SMLink0 is mainly used for integrated LAN. When an Intel LAN PHY is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of up to 1 MHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled using a soft strap.
SMLink1 can be used with an Embedded Controller (EC) or Baseboard Management Controller (BMC). Both SMLink0 and SMLink1 support up to 1 MHz.

SUSACK# & SUSWARN#:
This function is only applicable to platforms supporting Deep Sleep Wells.
This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (using SLP_SUS#). The EC/ motherboard control logic must observe edges on this pin, preparing for Primary well power loss on a falling edge and preparing for Prim well related activity (host/Intel ME wakes and runtime events) on a rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#.

BUS SWITCH

When OE is HIGH, the switch is ON and Port A is connected to Port B. When OE is LOW, the switch is OPEN and a high-impedance state exists between the two ports.
when we are in sleep: SLP_S3# = 0, in that case we don't want to pass anything.

the value of resistors affects the transition speed, but here the total resistance is close to 2.2K. if we put 1M pull-up, it's close to disconnection.



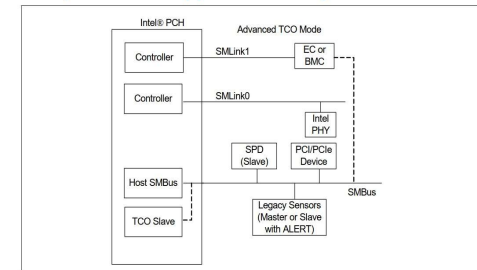
SMB SLEEP
SMB_CLK_S
SMB_DATA_S
Goes to DDR4 SODDIMM

ALL SLAVES THAT HAS +3V3S AS POWER SUPPLY ARE CONNECTED TO THIS BY5 ONLY.

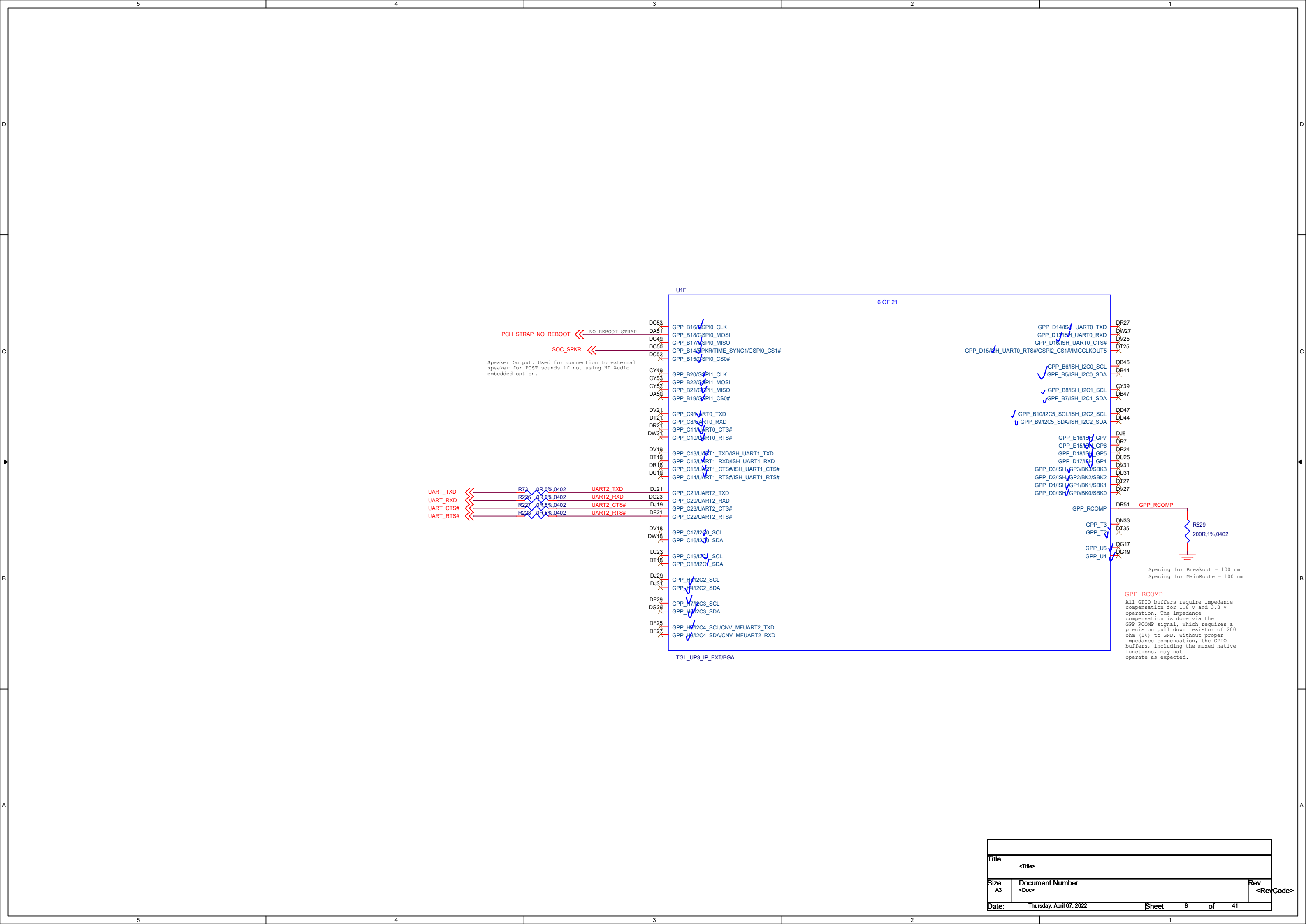
when a SLAVE supply power is cut-off we wan to make sure it doesn't have pull-up because that could cause a leakage.

A situation from past experience: a certain device didn't have supply power but it's SMBus did have power and it didn't turn-on.

TL-PDG P.189/507
SMBus / SMLink Connectivity (Advanced TCO Mode)



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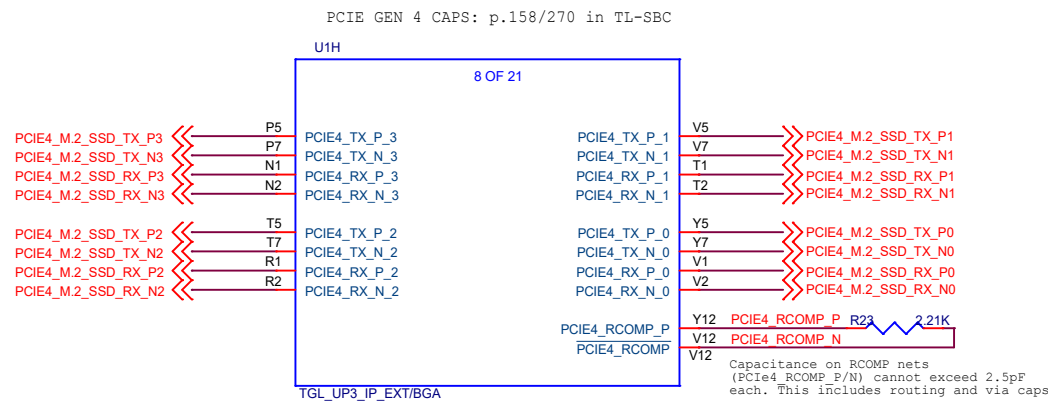
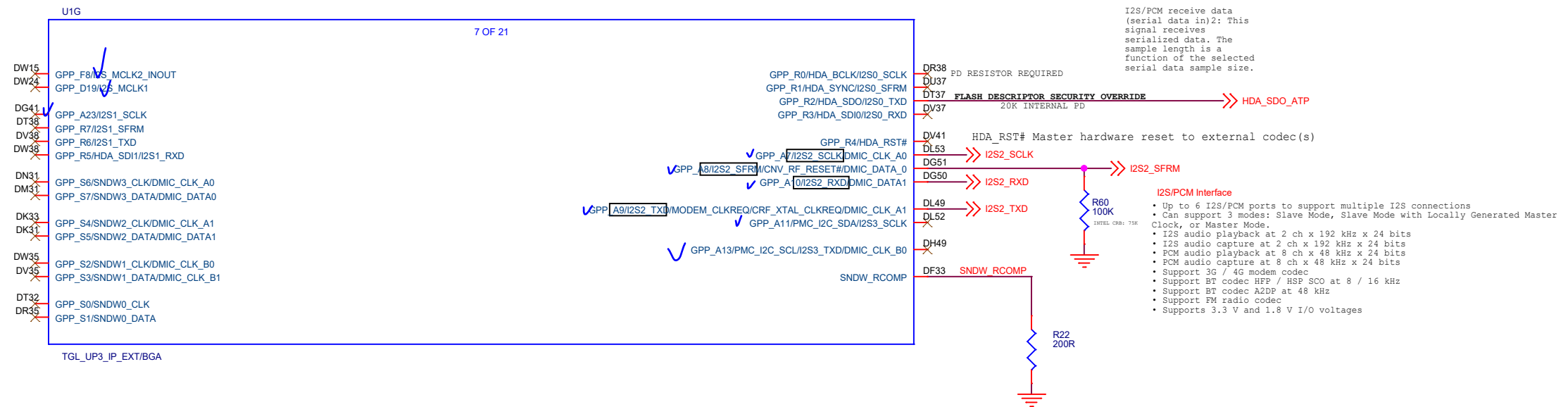
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For the Tiger Lake platform, SoundWire* is still the newest audio interface targeting (but not limited to) the phone, mobile, and desktop market as an alternative to Slimbus. Its main advantage is the connection simplicity with a 2 wire multi-drop topology + PDM streaming capabilities. For the Tiger Lake PCH there are 4 separate SoundWire interfaces that can be used.

On the Tiger Lake platform the SoundWire* interface and other audio interfaces can be configured by itself or at the same time with other interfaces for connection to end devices. Refer Tiger Lake PCH-LP External Design Specification (#576591) for specific sku pins assignments.

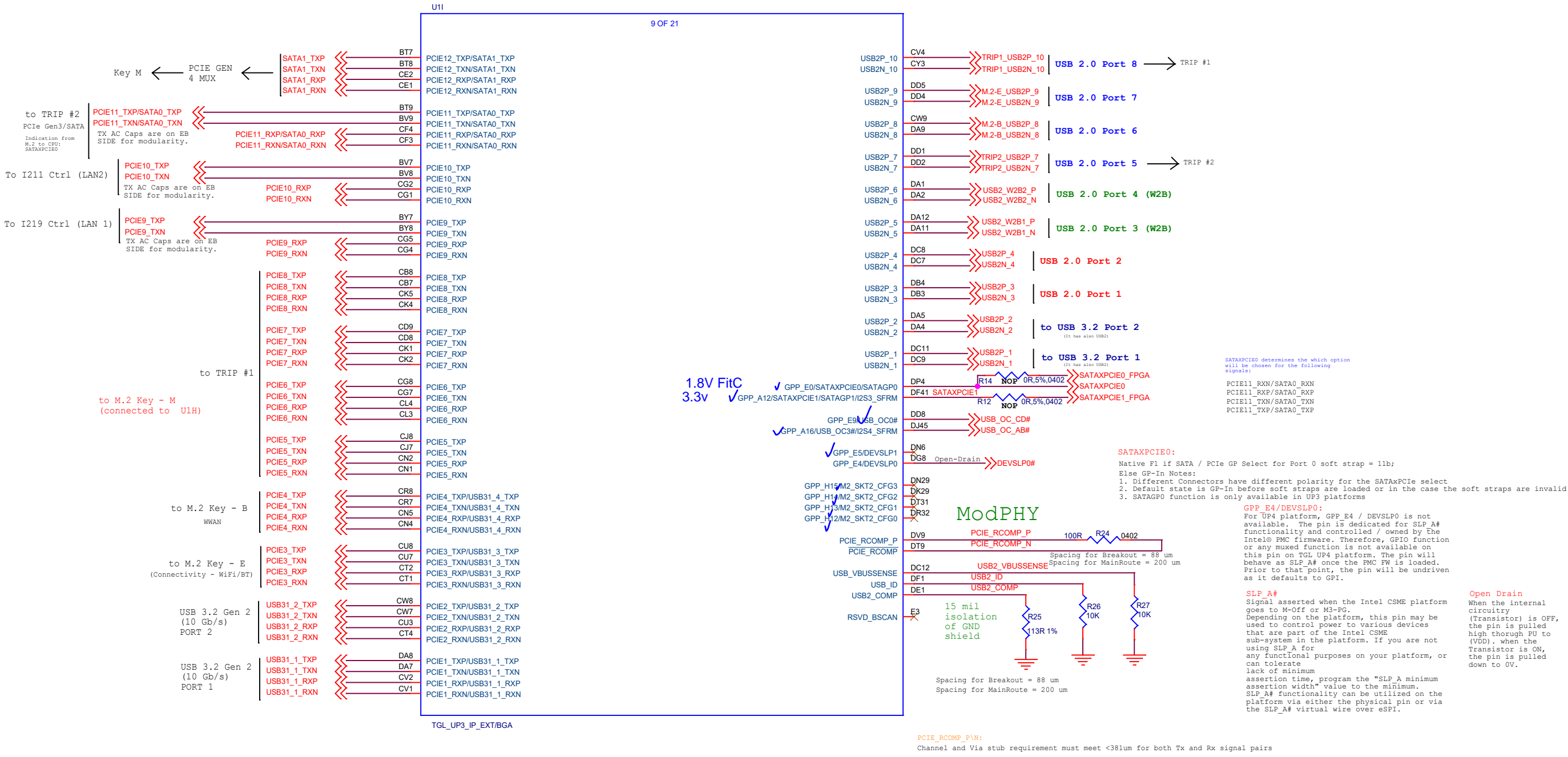
Table 87. SoundWire* Signals

Signal Name	Description
SNDW0_DATA	SoundWire Data 0: Serialized data line containing frame and data being transmitted /Received
SNDW0_CLK	SoundWire Clock 0: Serial bit clock used to control the timing of a transfer.
SNDW1_DATA	SoundWire Data 1: Serialized data line containing frame and data being transmitted /Received
SNDW1_CLK	SoundWire Clock 1: Serial bit clock used to control the timing of a transfer.
SNDW2_DATA	SoundWire Data 2: Serialized data line containing frame and data being transmitted /Received
SNDW2_CLK	SoundWire Clock 2: Serial bit clock used to control the timing of a transfer.
SNDW3_DATA	SoundWire Data 3: Serialized data line containing frame and data being transmitted /Received
SNDW3_CLK	SoundWire Clock 3: Serial bit clock used to control the timing of a transfer.



Signal Name	Description	Dir	Buffer Type	Link Type	Availability
PCIE4_RCOMP_P PCIE4_RCOMP_N	Resistance Compensation for PEG channel	I	Analog	Diff	UP3/UP4/H Processor Lines
PCIE4_TX_P[3:0] PCIE4_TX_N[3:0]	PCIE Transmit Differential Pairs	O	PCIE	Diff	UP3/UP4/H Processor Lines
PCIE4_RX_P[3:0] PCIE4_RX_N[3:0]	PCIE Receive Differential Pairs	I	PCIE	Diff	UP3/UP4/H Processor Lines

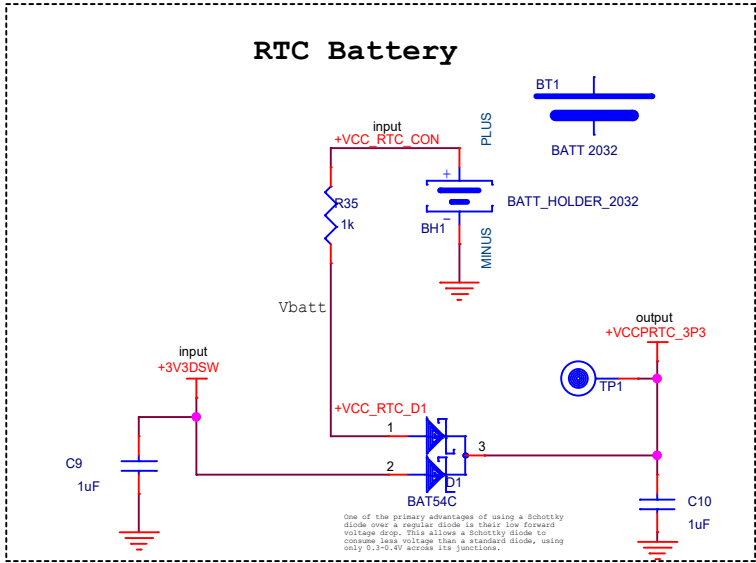
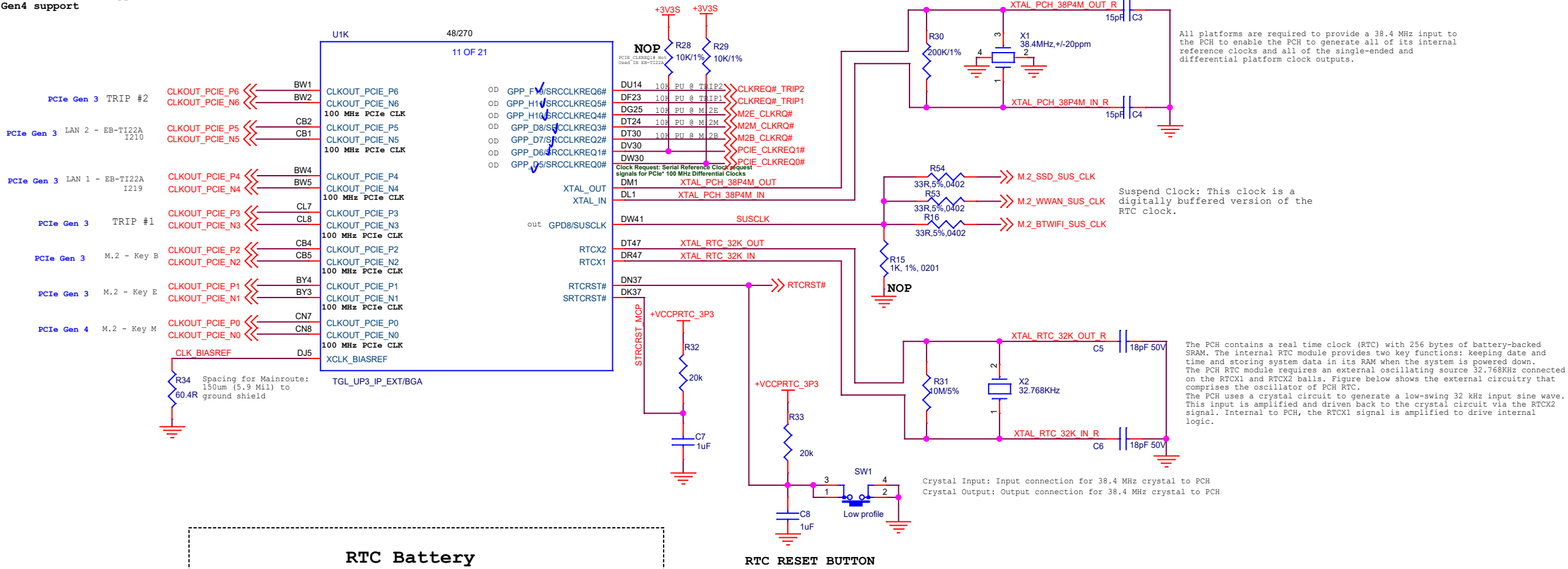
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PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices

- CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support
- CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support



When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed. The RTCRST# signal may also be used to detect a low battery voltage. RTCRST# will be asserted during a power up from G3 state if the battery voltage is below 2V. This will set the RTC_PWR_STS bit as described above. If desired, BIOS may request that the user replace the battery. This RTCRST# circuit is combined with the diode circuit (refer figure above) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. The above figure is an example of this circuitry that is used in conjunction with the external diode circuit.

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SLP_S0#
S0 Sleep Control. When PCH is idle and processor is in C10 state, this pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.

SLP_S5#
This signal is for power plane control. When asserted (low), it will shutoff power to all non-critical systems in S5 (Soft Off) states.

SLP_S4#
S4 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S4 (Suspend to Disk) and lower (S5).

SLP_S3#
S3 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S3 (Suspend to RAM) and lower (S4, S5).

SLP_A#
This signal is used to control power to devices on the platform in conjunction with the Intel® ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timings as SLP_S3#.

SYS_RESET#
When the SYS_RESET# pin is detected as active (on signal's falling edge if de-bounce logic is disabled, or after 16 ms if 16 ms debounce logic is enabled), the PCH attempts to perform a "graceful" reset by entering a host partition reset entry sequence. Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the SYS_RESET# input remains asserted or not. It cannot occur again until SYS_RESET# has been detected inactive after the de-bounce logic, and the system is back to a full S0 state with PLTRST# inactive.

+VCCPRTC_3P3
R18
1M,5%,0402

INTRUDER#
Intruder Detect: This signal can be set to disable the system if box detected open

The PCH has an input signal, INTRUDER#, that can be attached to a switch that is activated by the system's case being open. This input has a two RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD_DET bit in the TCTL2 register. The INTRD_SEL bits in the TCTL2 register can enable the PCH to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP_EN bit.

The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD_DET bit. This allows the signal to be used as a GPI if the intruder function is not required. If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET bit will go to a 0 when INTRUDER# input signal goes inactive.

RTC-Well Input Strap Requirements
All RTC-well inputs (RSMRST#, RTCRST#, SRTCST#, INTRUDER#, PCH_PWROK, DSW_PWROK) must be either pulled up to VccRTC or pulled down to ground while in the G3 state. RTCRST# when configured as shown in Figure 63 on page 126 meets this requirement. RSMRST# should have a weak external pull-down to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICORTC leakage that can cause excessive current drain. The PCH_PWROK and DSW_PWROK input signal should also be configured with an external weak pull-down.

(SLP_SUS# = HIGH --> Exist from Deep Sx)
(SLP_SUS# = LOW --> Enter Deep Sx) **P.460**
SLP_SUS#
Deep Sx Indication: When asserted (driven low), this signal indicates PCH is in Deep Sx state where internal primary power is shut off for enhanced power saving. When de-asserted (driven high), this signal indicates exit from Deep Sx state and primary power can be applied to PCH. For non- Deep Sx, this pin also needs to use to turn on VCCPRIM 1P8 VR. This pin cannot left unconnected. Note: This is in the DSW power well.

RSMRST# (Platform --> PCH)
This signal is used for resetting the Primary power plane logic. This signal must be asserted for at least 10 ms after the Primary power wells are valid. When de-asserted, this signal is an indication that the power wells are stable.

SLP_SUS#
R38
10K,1%
+3V3A
R454
2.21K
+3V3A
R358
10K
Q34
Dual N,0.5A,20V
C493
100nF
PLTRST#_BUF
PLTRST#_Q
PLTRST#

DSW_PWROK
Input to SoC (FPGA OUTPUT)
TP5
R42
10K,1%
C290
10nF,25V,X7R
TP6
R44
10K,1%
TP7
R48
10K,1%
TP8
R19
1M,5%,0402
C414
100nF,25V

SYS_PWROK
Input to SoC (FPGA OUTPUT)
TP6
R42
10K,1%
C290
10nF,25V,X7R
TP6
R44
10K,1%
TP7
R48
10K,1%
TP8
R19
1M,5%,0402
C414
100nF,25V

PCH_PWROK
Input to SoC (FPGA OUTPUT)
TP7
R48
10K,1%
TP8
R19
1M,5%,0402
C414
100nF,25V

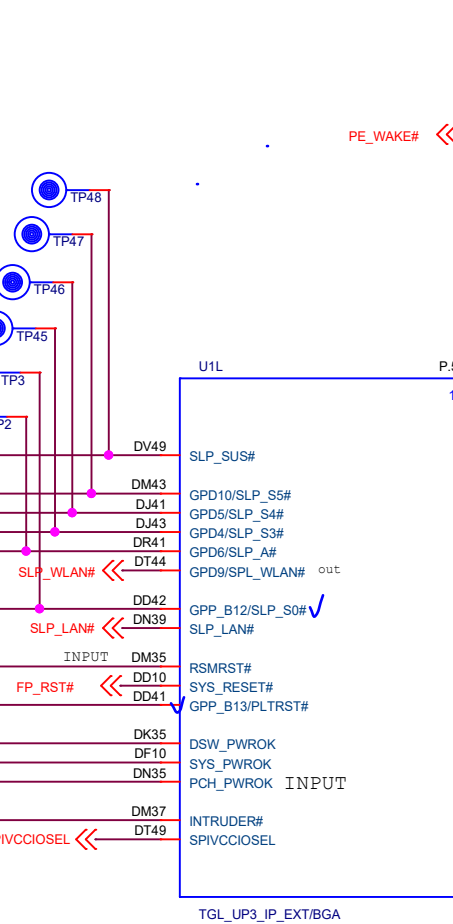
INTRUDER#
Intruder Detect: This signal can be set to disable the system if box detected open

SLP_WLAN# (GPD9)
The PCH controls the voltage rails into the external wireless LAN PHY using the SLP_WLAN# pin.
• The wireless LAN PHY is always powered when the Host is running.
– SLP_WLAN#='1' whenever SLP_S3#='1'.
• If Wake on Wireless LAN (WoWLAN) is required from S3/S4/S5 states, the host BIOS must set HOST WLAN PP EN.
• If WoWLAN is required from Deep Sx, the host BIOS must set DSW WLAN PP EN.
• If Intel® CSME has access to the Wireless LAN device:
– The Wireless LAN device must always be powered as long as Intel® CSME is powered.
SLP_WLAN#='1' whenever SLP_A#='1'.
• If Wake on Wireless LAN (WoWLAN) is required from M-Off state, Intel® CSME will configure SLP_WLAN#='1' in Sx/M-Off.
Intel® CSME configuration of SLP_WLAN# in Sx/M-Off is dependent on Intel® CSME power policy configuration.
When the Wireless LAN device is an integrated connectivity device (CNVi) the power to the CNVi external RF chip (CRP) must be always on. In this case the SLP_WLAN# shall not control the CRP 3.3 V power rail.

PLTRST# PLTRST# = High (De-Asserted)
Reset Behavior
When a reset is triggered, the PCH will send a warning message to the processor to allow the processor to attempt to complete any outstanding memory cycles and put memory into a safe state before the platform is reset. When the processor is ready, it will send an acknowledge message to the PCH. Once the message is received the PCH asserts PLTRST#.

The PCH does not require an acknowledge message from the processor to trigger PLTRST#. A global reset will occur after four seconds if an acknowledge from the processor is not received. When the PCH causes a reset by asserting PLTRST#, its output signals will go to their reset states. A reset in which the host platform is reset and PLTRST# is asserted is called a Host Reset or Host Partition Reset. Depending on the trigger a host reset may also result in power cycling, refer to the below table for details. If a host reset is triggered and the PCH times out before receiving an acknowledge message from the processor a Global Reset with power-cycle will occur. A reset in which the host and Intel® CSME partitions of the platform are reset is called a Global Reset. During a Global Reset, all PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. Intel® CSME and Host power back up after the power-cycle period. Straight to S5 is another reset type where all power wells that are controlled by the SLP_S3#, SLP_S4#, and SLP_A# pins, as well as SLP_S5# and SLP_LAN# (if pins are not configured as GPIOs), are turned off. All PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. The host stays there until a valid wake event occurs.

RESET TEST POINT
FP_RST#
R51
3.01k
R52
100R
TP9
TP10



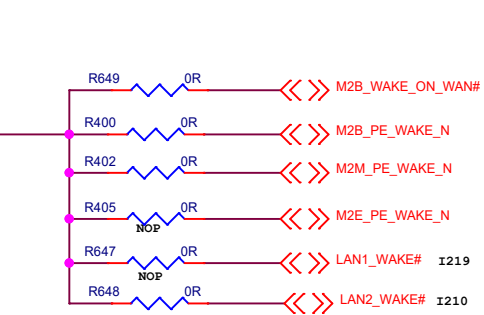
PCH_PWROK, SYS_PWROK and other PWROK Signal Generation
The power sequencing consists of multiple stages of power state transitions. During each stage, different VRs will be turned on through various control signals from the processor such as the SLP_SUS#, SLP_S5#, SLP_S4#, SLP_S3#, SLP_A# and CPU/C10_GATE#. In response, the platform will ramp the required voltage rails in the Required order and then asserted the various powergood signals required by the processor, and other platform components, after the necessarily timing requirements have been met. The below figure shows a high-level representative control signal and the powerpool logic diagram for generating the PCH_PWROK and SYS_PWROK signals. This figure shows the recommended power-on sequencing flow steps from SLP_S4# de-assertion until PLTRST# de-assertion for the Tiger Lake platform. During G3/Sx, S5 to S0 transitions, the platform will need to generate the DSW_PWROK and RSMRST# signals. In this phase of the power up sequence, the DSW and Primary power well voltage rails are ramped to the processor. During S5 to S0 and S0s to S0 transitions, the platform will need to generate the VCCST_PWROK, PCH_PWROK and SYS_PWROK signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up. The PCH_PWROK signal is expected to be asserted by the platform to indicate to the processor that all required CPU voltage rails are up and stable, and that the processor may continue the final boot sequence leading up to PLTRST# de-assertion, such as starting to turn on clocks and executing other internal pre-reset activities. SYS_PWROK is expected to be asserted by the platform to indicate that the system and all of its non-CPU components are ready for PLTRST# de-assertion. During power state transition to S0, the SYS_PWROK signal is the final platform controlled hardware gate before PLTRST# de-assertion. Platform designers may optimize when the SYS_PWROK signal is asserted with respect to the PCH_PWROK signal to help optimize overall boot latency, depending on system and component timing requirements.

PLTRST# PLTRST# = High (De-Asserted)
Reset Behavior
When a reset is triggered, the PCH will send a warning message to the processor to allow the processor to attempt to complete any outstanding memory cycles and put memory into a safe state before the platform is reset. When the processor is ready, it will send an acknowledge message to the PCH. Once the message is received the PCH asserts PLTRST#.

The PCH does not require an acknowledge message from the processor to trigger PLTRST#. A global reset will occur after four seconds if an acknowledge from the processor is not received. When the PCH causes a reset by asserting PLTRST#, its output signals will go to their reset states. A reset in which the host platform is reset and PLTRST# is asserted is called a Host Reset or Host Partition Reset. Depending on the trigger a host reset may also result in power cycling, refer to the below table for details. If a host reset is triggered and the PCH times out before receiving an acknowledge message from the processor a Global Reset with power-cycle will occur. A reset in which the host and Intel® CSME partitions of the platform are reset is called a Global Reset. During a Global Reset, all PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. Intel® CSME and Host power back up after the power-cycle period. Straight to S5 is another reset type where all power wells that are controlled by the SLP_S3#, SLP_S4#, and SLP_A# pins, as well as SLP_S5# and SLP_LAN# (if pins are not configured as GPIOs), are turned off. All PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. The host stays there until a valid wake event occurs.

RESET TEST POINT
FP_RST#
R51
3.01k
R52
100R
TP9
TP10

RESET TEST POINT
FP_RST#
R51
3.01k
R52
100R
TP9
TP10



WAKE#
WAKE# *: Can be used by the LAN PHY as a wake signal. PCI Express* ports can wake the platform from S4, S5, or Deep Sx using the WAKE# pin. WAKE# is treated as a wake event, but does not cause any bits to go active in the GPE_STS register.

PCI Express* WAKE# pin is an Output in S0ix states hence this pin cannot be used to wake up the system during S0ix states.

BATLOW#
Battery Low: An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S4/S5 states or exit from Deep Sx state. This signal can also be enabled to cause an SMI# when asserted. This signal is multiplexed with GPD0.

Note: For any platform not using this pin functionality, this signal must be tied high to VCCBATT_3V3. An external pull-up resistor to VCCBATT_3V3 is required.

CPU_C10_GATE#
CPU_C10_GATE# is a signal from the Tiger Lake SoC that can be used for GPD0/ACPRESENT, the CPU_C10_GATE# pin. In this phase of the power up sequence, the DSW and Primary power well voltage rails are ramped to the processor. During S5 to S0 and S0s to S0 transitions, the platform will need to generate the VCCST_PWROK, PCH_PWROK and SYS_PWROK signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up. The PCH_PWROK signal is expected to be asserted by the platform to indicate to the processor that all required CPU voltage rails are up and stable, and that the processor may continue the final boot sequence leading up to PLTRST# de-assertion, such as starting to turn on clocks and executing other internal pre-reset activities. SYS_PWROK is expected to be asserted by the platform to indicate that the system and all of its non-CPU components are ready for PLTRST# de-assertion. During power state transition to S0, the SYS_PWROK signal is the final platform controlled hardware gate before PLTRST# de-assertion. Platform designers may optimize when the SYS_PWROK signal is asserted with respect to the PCH_PWROK signal to help optimize overall boot latency, depending on system and component timing requirements.

LAN1_WAKE#
LAN WAKE: LAN Wake Indicator from the GbE PHY. Note: LAN WAKE# functionality is only supported with Intel PHY I219. Connection of a third party LAN device's wake signal to LAN_WAKE# is not supported.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

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Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

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VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

BATLOW#
Battery Low: An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S4/S5 states or exit from Deep Sx state. This signal can also be enabled to cause an SMI# when asserted. This signal is multiplexed with GPD0.

Note: For any platform not using this pin functionality, this signal must be tied high to VCCBATT_3V3. An external pull-up resistor to VCCBATT_3V3 is required.

CPU_C10_GATE#
CPU_C10_GATE# is a signal from the Tiger Lake SoC that can be used for GPD0/ACPRESENT, the CPU_C10_GATE# pin. In this phase of the power up sequence, the DSW and Primary power well voltage rails are ramped to the processor. During S5 to S0 and S0s to S0 transitions, the platform will need to generate the VCCST_PWROK, PCH_PWROK and SYS_PWROK signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up. The PCH_PWROK signal is expected to be asserted by the platform to indicate to the processor that all required CPU voltage rails are up and stable, and that the processor may continue the final boot sequence leading up to PLTRST# de-assertion, such as starting to turn on clocks and executing other internal pre-reset activities. SYS_PWROK is expected to be asserted by the platform to indicate that the system and all of its non-CPU components are ready for PLTRST# de-assertion. During power state transition to S0, the SYS_PWROK signal is the final platform controlled hardware gate before PLTRST# de-assertion. Platform designers may optimize when the SYS_PWROK signal is asserted with respect to the PCH_PWROK signal to help optimize overall boot latency, depending on system and component timing requirements.

LAN1_WAKE#
LAN WAKE: LAN Wake Indicator from the GbE PHY. Note: LAN WAKE# functionality is only supported with Intel PHY I219. Connection of a third party LAN device's wake signal to LAN_WAKE# is not supported.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

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Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

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Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

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Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

BATLOW#
Battery Low: An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S4/S5 states or exit from Deep Sx state. This signal can also be enabled to cause an SMI# when asserted. This signal is multiplexed with GPD0.

Note: For any platform not using this pin functionality, this signal must be tied high to VCCBATT_3V3. An external pull-up resistor to VCCBATT_3V3 is required.

CPU_C10_GATE#
CPU_C10_GATE# is a signal from the Tiger Lake SoC that can be used for GPD0/ACPRESENT, the CPU_C10_GATE# pin. In this phase of the power up sequence, the DSW and Primary power well voltage rails are ramped to the processor. During S5 to S0 and S0s to S0 transitions, the platform will need to generate the VCCST_PWROK, PCH_PWROK and SYS_PWROK signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up. The PCH_PWROK signal is expected to be asserted by the platform to indicate to the processor that all required CPU voltage rails are up and stable, and that the processor may continue the final boot sequence leading up to PLTRST# de-assertion, such as starting to turn on clocks and executing other internal pre-reset activities. SYS_PWROK is expected to be asserted by the platform to indicate that the system and all of its non-CPU components are ready for PLTRST# de-assertion. During power state transition to S0, the SYS_PWROK signal is the final platform controlled hardware gate before PLTRST# de-assertion. Platform designers may optimize when the SYS_PWROK signal is asserted with respect to the PCH_PWROK signal to help optimize overall boot latency, depending on system and component timing requirements.

LAN1_WAKE#
LAN WAKE: LAN Wake Indicator from the GbE PHY. Note: LAN WAKE# functionality is only supported with Intel PHY I219. Connection of a third party LAN device's wake signal to LAN_WAKE# is not supported.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCST_OVERRIDE
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VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

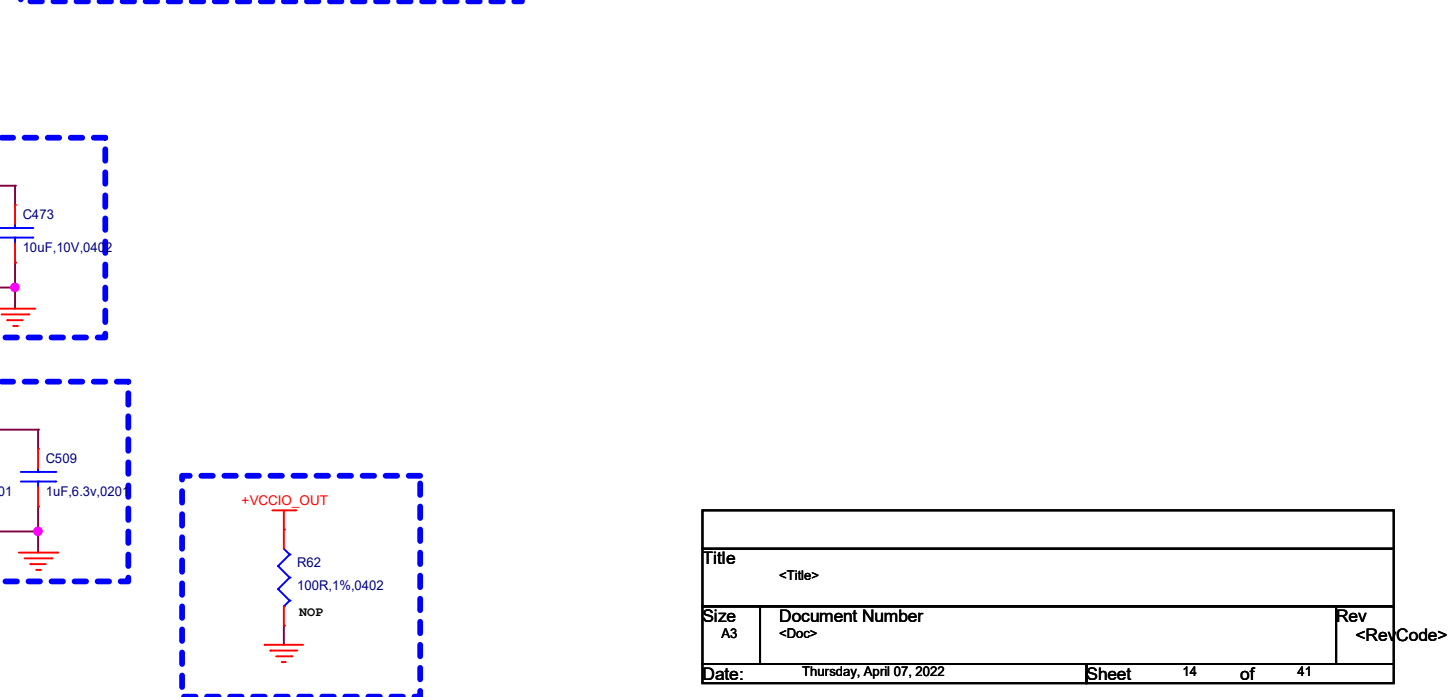
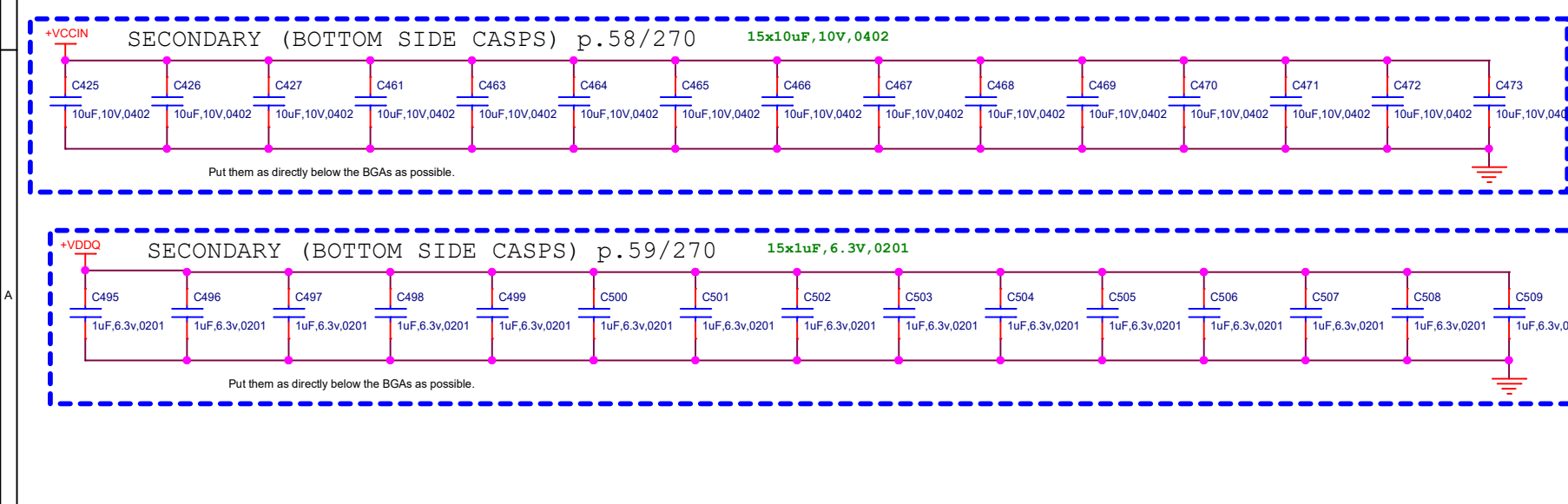
VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

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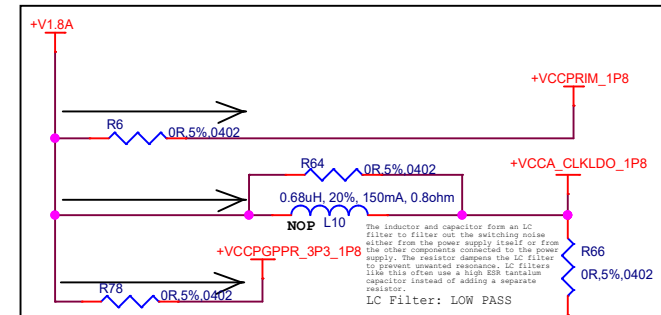
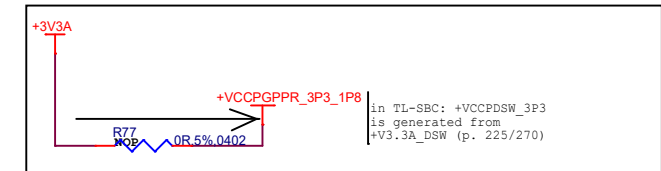
VCCST_OVERRIDE
Vccst Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWROK_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

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From
External
DC\DC
to SoC



R66:
Option 1: stuff with 0
ohm if the inductor is
not stuffed. Option 2:
stuff 100 mohm if the
inductor stuffed

LC Filter: LOW PASS

RC_CLKLDO

C211

47uF,6.3V,X5R

TP52 TP51 TP50 TP49

VCCIN_AUX_VSSSENSE

VCCIN_AUX_VCCSENSE

VCC_VNNEXT_1P05_1

VCC_VNNEXT_1P05_2

VCC_V1P05EXT_1P05_1

VCC_V1P05EXT_1P05_2

VRALERT_MCP#

GPPC_B2_BC_PROCHOT_N

VCCIN_AUX_CORE_VID0_R

VCCIN_AUX_CORE_VID1_R

GPPC_B0_CORE_VID_0

GPPC_B1_CORE_VID_1

GPP_B2/VRALERT#

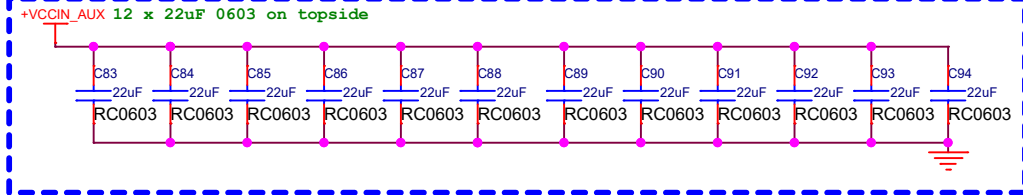
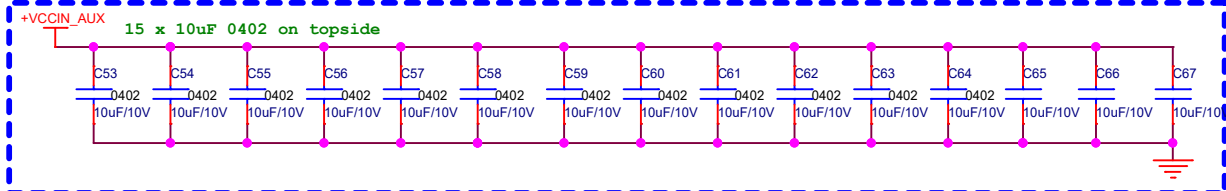
GPP_F22_VN_CTRL

GPP_F23/V1P5_CTRL

GPP_B0/CORE_VID0

GPP_B1/CORE_VID1

VRALERT#: ICC Max. throttling indicator from the PCH voltage regulators. VRALERT# pin allows the VR to force PCH throttling to prevent an over current shutdown. PMC based on the VRALERT# and messages from the processor. The messages from the processor allows the processor to constrain the PCH to a particular power budget.



C510,C11,C512 (Deleted, See Ver4.5)

Use 2.5V rating caps.
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth, or 600kHz switching frequency assuming BW= ¼ of Fsw.
Place board caps as close as possible to package in this order where 0402 to be the closest to package pins:
VR 77343? 0805? 0603-> 0402 ? package.
*a DCLL of 3.3mohm is required and bulk capacitors must be used.

Pair board caps with power/ground PTHs.
Align caps along current flow path from VR to package pins.

The VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two optional dedicated voltage regulators that save platform power during low power states.

VCCIN_AUX, VCCPRIM

+VCCIN_AUX

AB12

AC10

AE10

AK2

AR10

AT12

AU10

AW10

BV1

BV39

BW40

BY39

CC1

CD12

CF10

CG12

CH10

CJ1

CJ12

CK10

CL12

CM10

CP1

CR12

CT10

CJ12

CU12

CY1

AK1

VCCIN_AUX_1

VCCIN_AUX_2

VCCIN_AUX_3

VCCIN_AUX_4

VCCIN_AUX_5

VCCIN_AUX_6

VCCIN_AUX_7

VCCIN_AUX_8

VCCIN_AUX_9

VCCIN_AUX_10

VCCIN_AUX_11

VCCIN_AUX_12

VCCIN_AUX_13

VCCIN_AUX_14

VCCIN_AUX_15

VCCIN_AUX_16

VCCIN_AUX_17

VCCIN_AUX_18

VCCIN_AUX_19

VCCIN_AUX_20

VCCIN_AUX_21

VCCIN_AUX_22

VCCIN_AUX_23

VCCIN_AUX_24

VCCIN_AUX_25

VCCIN_AUX_26

VCCIN_AUX_27

VCCIN_AUX_28

VCCIN_AUX_29

VCCIN_AUX_VSSSENSE

VCCIN_AUX_VCCSENSE

VCC_VNNEXT_1P05_1

VCC_VNNEXT_1P05_2

VCC_V1P05EXT_1P05_1

VCC_V1P05EXT_1P05_2

GPP_B2/VRALERT#

GPP_F22_VN_CTRL

GPP_F23/V1P5_CTRL

GPP_B0/CORE_VID0

GPP_B1/CORE_VID1

U1N

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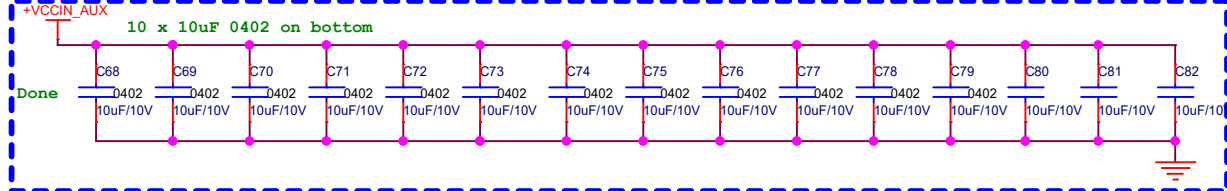
VCCPRIM_1P8_1
VCCPRIM_1P8_2
VCCPRIM_1P8_3
VCCPRIM_1P8_4
VCCPRIM_1P8_5
VCCPRIM_1P8_6
VCCPRIM_1P8_7
VCCPRIM_1P8_8
VCCPRIM_1P8_9
VCCPRIM_1P8_10
VCCPRIM_1P8_11
VCCPRIM_1P8_12
VCCPRIM_1P8_13
VCCPRIM_1P8_14
VCCPRIM_1P8_15
VCCPRIM_1P8_16
VCCPRIM_1P8_17
VCCPRIM_3P3_1
VCCPRIM_3P3_2
VCCPRIM_3P3_3
VCCPRIM_3P3_4
DCPRTC
VCCLDOSTD_0P85
VCCA_CLKLDO_1P8_1
VCCA_CLKLDO_1P8_2
VCCDPHY_1P24
VCCDSW_1P05
VCC1P05_OUT_FET_1
VCC1P05_OUT_FET_2
VCC1P05_OUT_FET_3
VCCPRIM1P05_OUT_PCH_1
VCCPRIM1P05_OUT_PCH_2
VCCPRIM1P05_OUT_PCH_3
VCCRTC
VCCDSW_3P3
VCCPGPPR
VCCPRIM_3P3_5
VCCPRIM_3P3_6
VCCPRIM_1P8_18
RSVD_1

CY18
CY20
CY24
CY26
DA18
DA20
DA22
DA24
DA26
DC18
DC20
DC22
DC24
DC26
DD20
DD22
DV22
DA35
DC28
DC30
DD30
DV34
DV16
DC15
DV28
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BT5
DA31
DC33
DC31
DC35
DD37
DA28
CY31
CY83
CV89
AP12

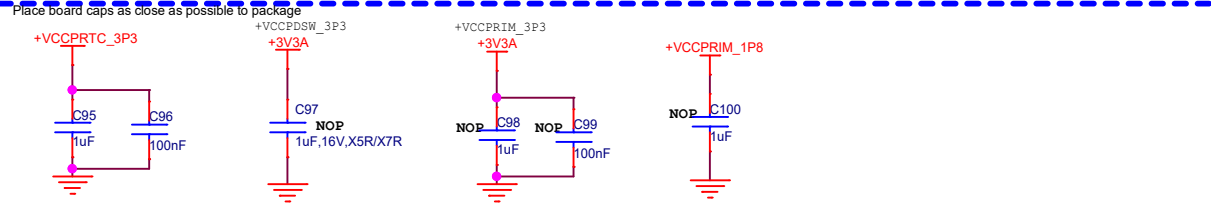
input
+VCCPRIM_1P8 (+V1.8A)
+VCCPRIM_3P3
3.3 V Primary Well.
+3V3A
+VCCRTCEXT
+VCCLDOSTD_OUT_0P85
+VCCA_CLKLDO_1P8
+VCCDPHY_1P24_SOC
+VCCDSW_1P05_SOC
+VCC1P05_OUT_FET
+VCC1P05_OUT_PCH
+VCCPRTC_3P3
+VCCPRIM_3P3
3.3 V Primary Well.
+3V3A
+VCCPRIM_1P8
1.8 V Primary Well.
input
PCH I/O and Misc 3.3V Rail(Primary Well)
PCH I/O and Misc 1.8V Rail(Primary Well)
input

RTC de-coupling capacitor only. This rail should not be driven by any motherboard power rails.
This rail is generated internally and needs to be routed out to the motherboard for decoupling purposes.
Not Connected to any target except decoupling capacitor: C105
1.24 V for CNVi logic. This rail is generated internally with an LDO and needs to be routed to the motherboard for decoupling purpose only. This rail should not be driven by any motherboard power rails.
Not Connected to any target except decoupling capacitor: C107
Deep Sx Well: 1.05 V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic.
Not Connected to any target except decoupling capacitor: C104
1.05 V Primary Well: for CNVi and other internal I/O blocks.
(Make small plane not connected to anything except these 3 balls)
Audio Power 3.3 V or 1.8 V.
Is supplied from +V1.8A or from +V3A
p234/270 TL-SBC

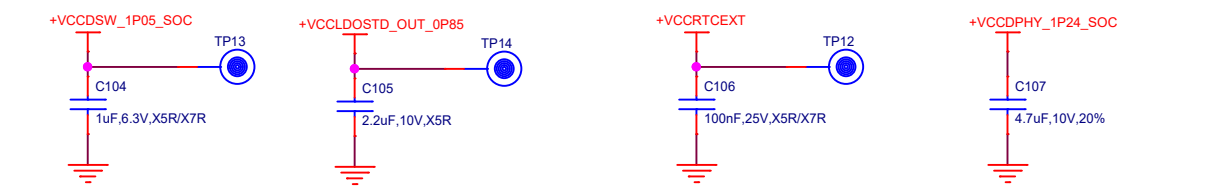
TGL_UP3_IP_EXT/BGA



Use 2.5V rating caps.
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth, or 600kHz switching frequency assuming BW= ¼ of Fsw.
Place board caps as close as possible to package



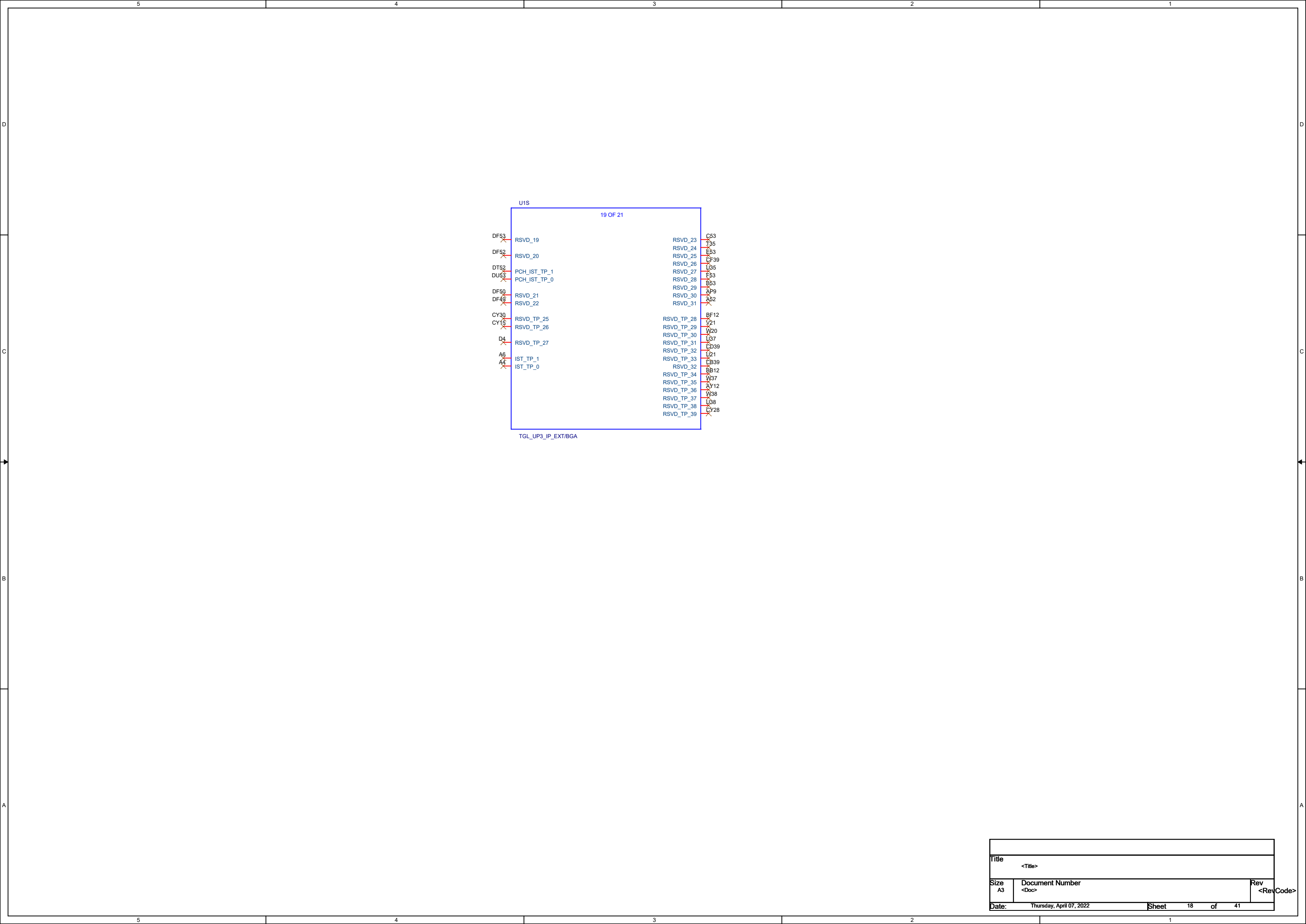
NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA



Trade-offs - Volume vs. Premium Power Maps:

Power maps are broken into two tiers: Volume and Premium. Volume focuses on cost savings with the fewest VRs and Premium focuses on the smallest solution size with the lowest power consumption. For a design focused on S0ix or Modern Standby* power, the Premium power map is recommended. The designer may choose to implement a hybrid between Volume and Premium as long as guidelines are followed.

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Headers

audio

Extension headers

Note: The Intel® Ethernet Connection I219 can be connected to one of the following PCI Express* ports 7, 8 or, 9

PCH UART

This Circuit purpose is for the BIOS to be able to send commands to the BIOS Engineer PC and be able to read them. the BIOS Engineer will use DP9 Adapter to read the messages.

B2B Receptacle

Maximum Current Per Contact: 0.5A
Maximum Voltage Per Contact: 100V

Supply Voltages

USB 3.2 Port 1

USB 3.2 Port 2

I219

I211

LAN 1

LAN 2

USB2 Port 1

USB2 Port 2

OVER CURR

LAN

GPIOs

vPro

SMBus

POWER

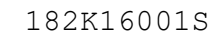
mini DP ++ 2

HDMI PORT 2

mini DP++ 1

HDMI PORT 1

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[illegible]

Maximum Current Per Contact: 0.5A

Maximum Voltage Per Contact: 100V

Max Current Consumption is ~180mA per 5V/3V Device
Max Current Consumption is ~630mA per I225 Device

Supply Voltages

USB 3.2

I219

I211

I210

LAN

I219

SML0

SLP

POWER

TCP 2 (DP/HDMI) (/USB-C)

TCP 0 (DP/HDMI)

TCP 1 (DP/HDMI)

DDI B (DP/HDMI)

SMBus

POWER

see TL-PDG p 104/506 table 49: DDI port signal mapping to the HDMI connector.

mini DP ++ 2

for this Face Module, this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they belong to HDMI.

HDMI PORT 2

for this Face Module, this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in EB-TI22A Connector.

mini DP++ 1

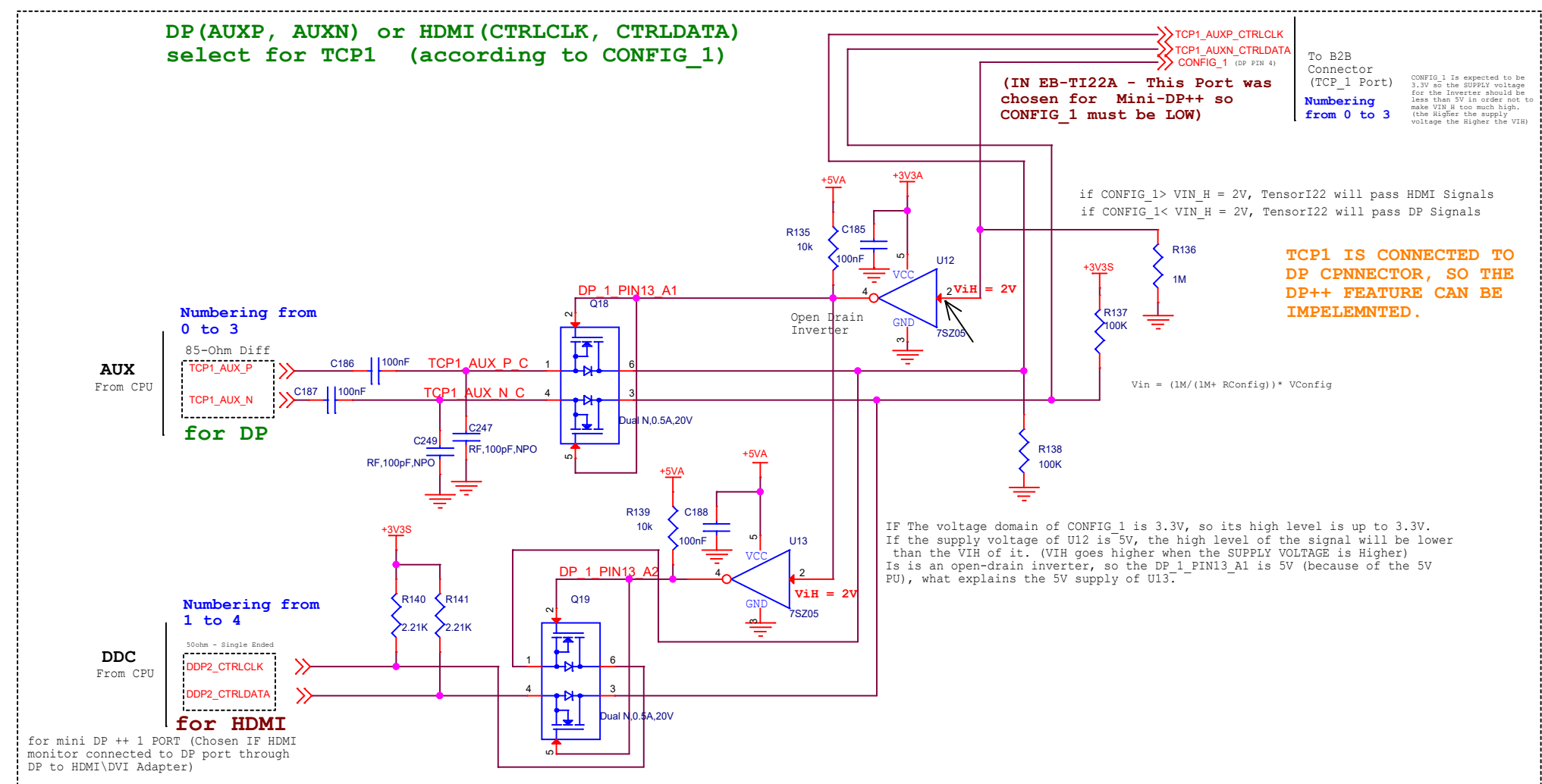
see TL-PDG p 103/506 table 48: DDI: TCP Port Signal Mapping for HDMI connector.

HDMI PORT 1

for this Face Module, this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they belong to HDMI.

Conn., B2B, 2x80 cont. P=0.635mm, Rec., H=4mm (mated 6.7,8,9,10mm), SMT

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12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] DDIB_TXN[3:0]	TX Digital Display Interface Transmit: DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P DDIB_AUX_N	AUX Digital Display Interface Display Port Auxiliary: Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

Table 38. DisplayPort* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx) TX	DDIX_TXP/N[3:0]	N/A	N/A	1
	TCPX_TX_P/N[1:0] and TCPX_TXRX_P/N[1:0]	N/A	N/A	2
Aux Channel AUX	DDIX_AUXP/N	N/A	N/A	1
	TCPX_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

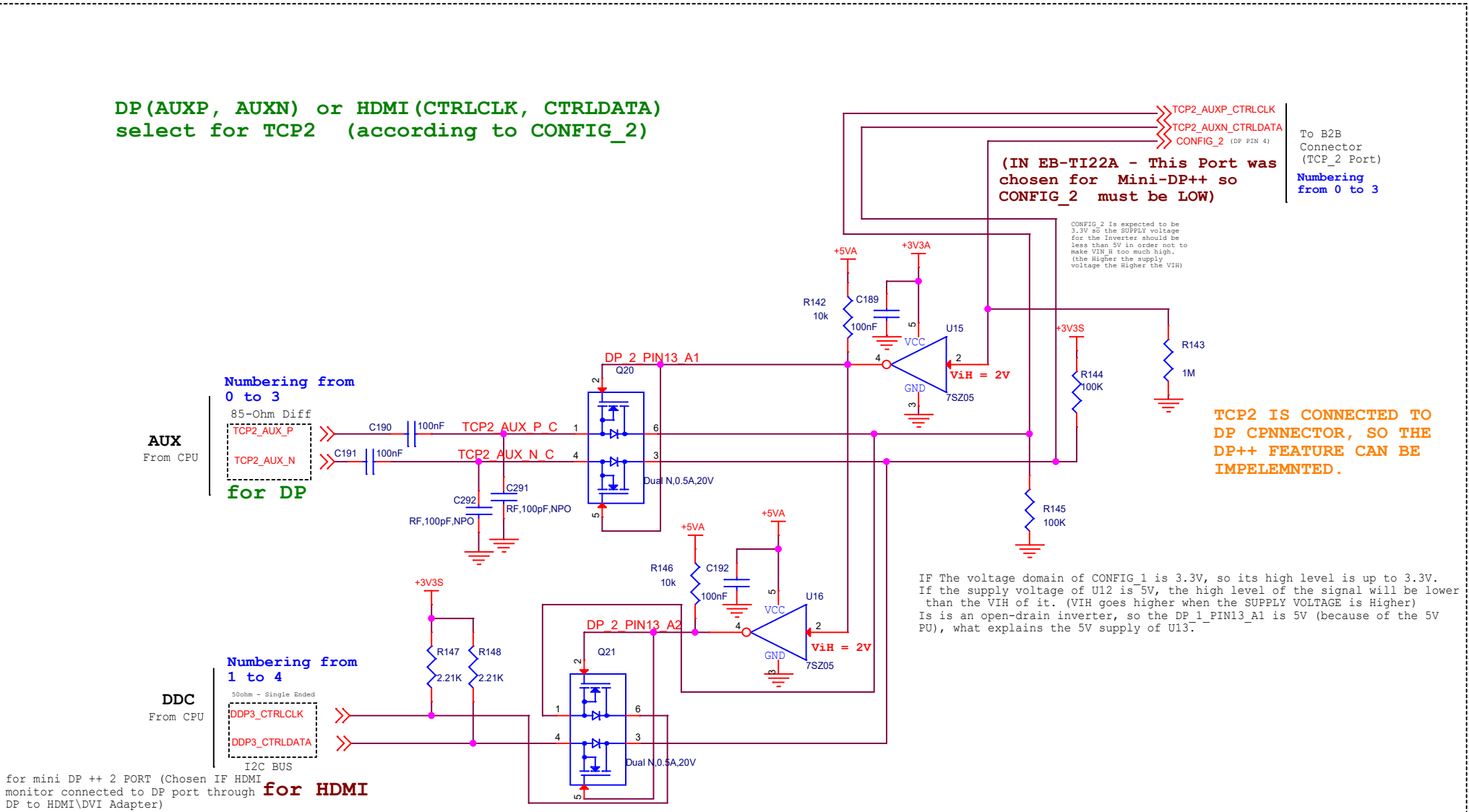


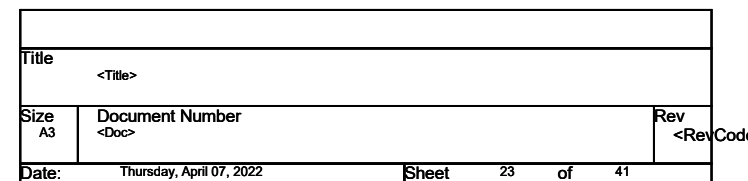
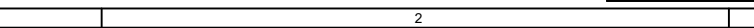
Table 47. HDMI* Signals

Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx) TX	DDIX_TXP/N[3:0]	N/A	1
	TCPX_TX_P/N[0:1] and TCPX_TXRX_P/N[0:1]	N/A	2
DDC DDC	N/A	DDPX_CTRLCLK and DDPX_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

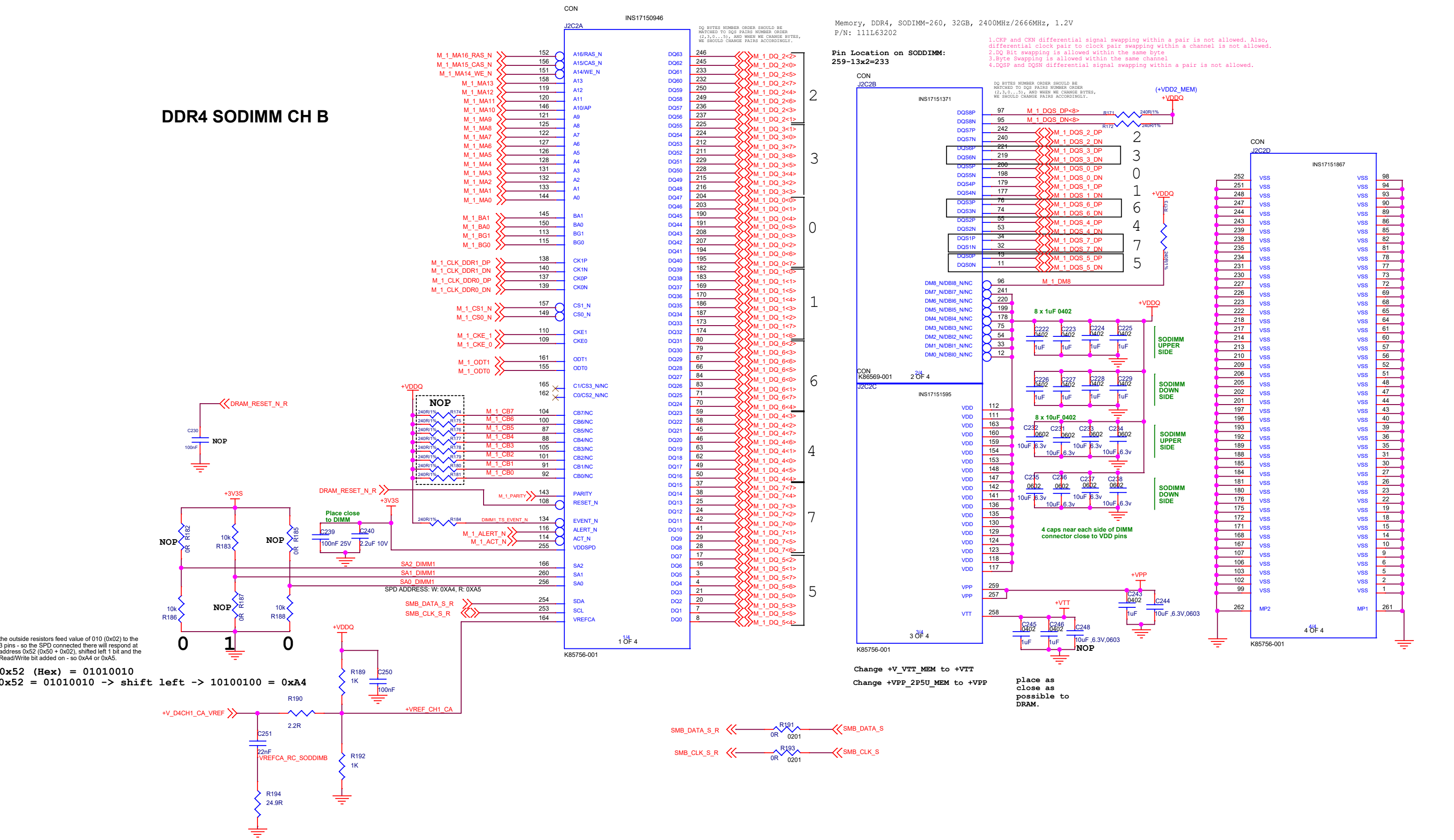
Note:
1. Signal names apply for DDI A/B ports.
2. Signal names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

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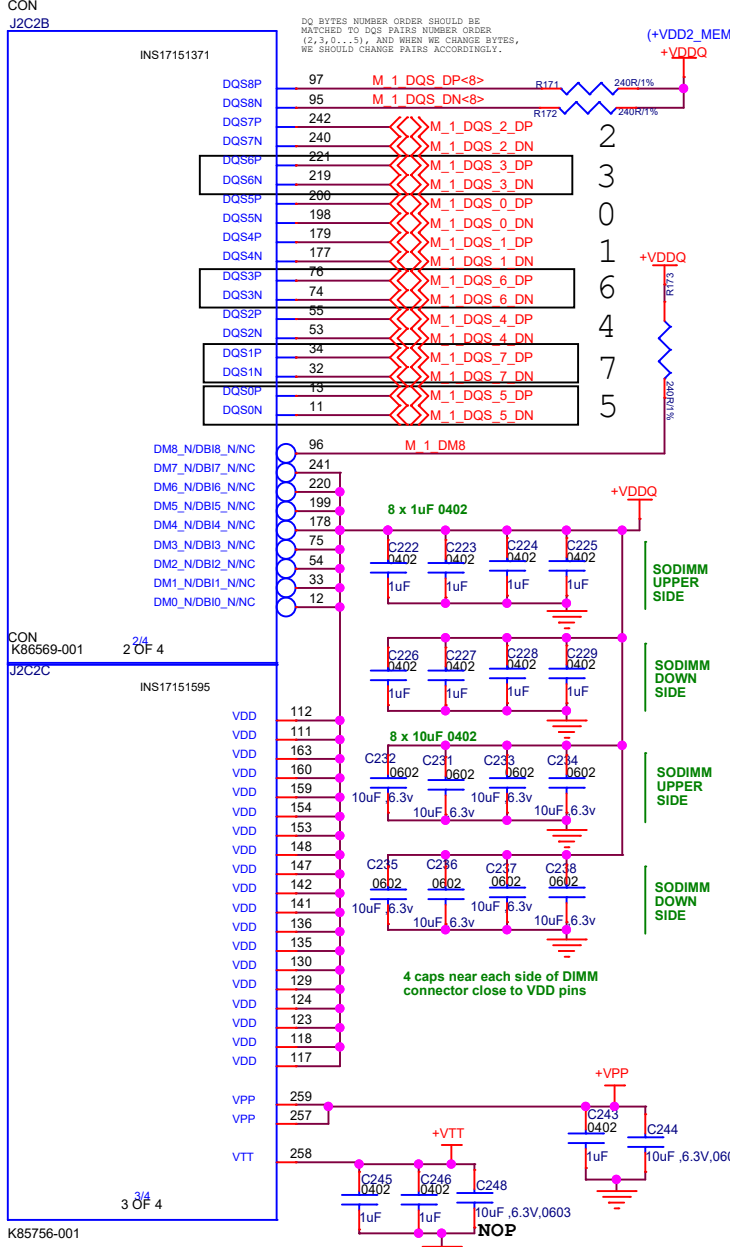
DDR4 SODIMM CH B



Memory, DDR4, SODIMM-260, 32GB, 2400MHz/2666MHz, 1.2V
P/N: 111L63202

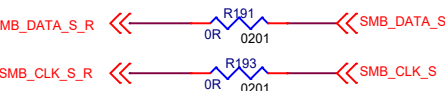
Pin Location on SODIMM:
259-13x2=233

- 1.CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.
- 2.DQ Bit swapping is allowed within the same byte
- 3.Byte Swapping is allowed within the same channel
- 4.DQSP and DQSN differential signal swapping within a pair is not allowed.

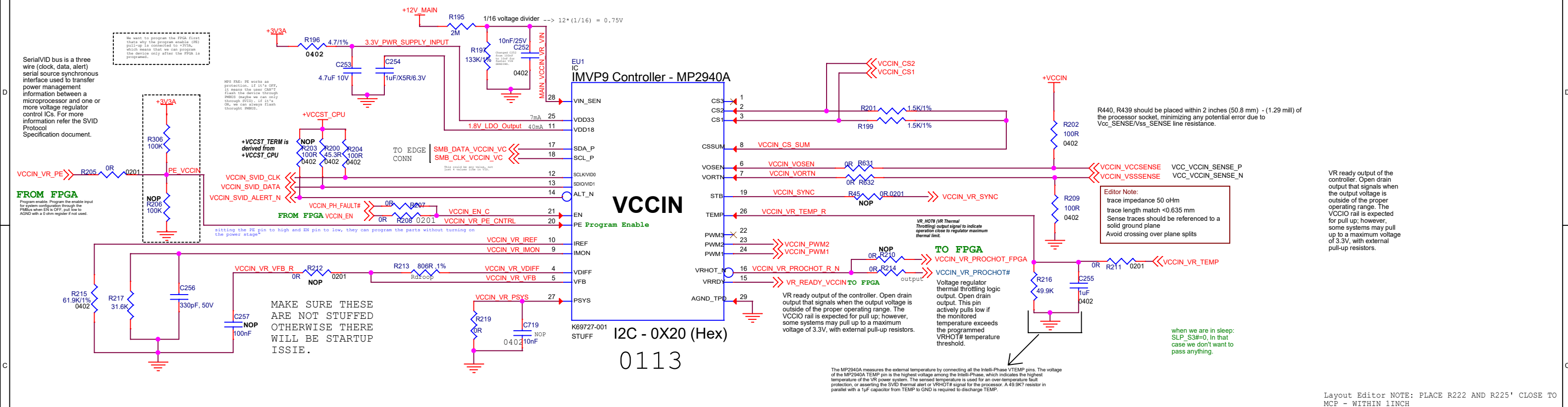


Change +V_VTT_MEM to +VTT
Change +VPP_2P5U_MEM to +VPP

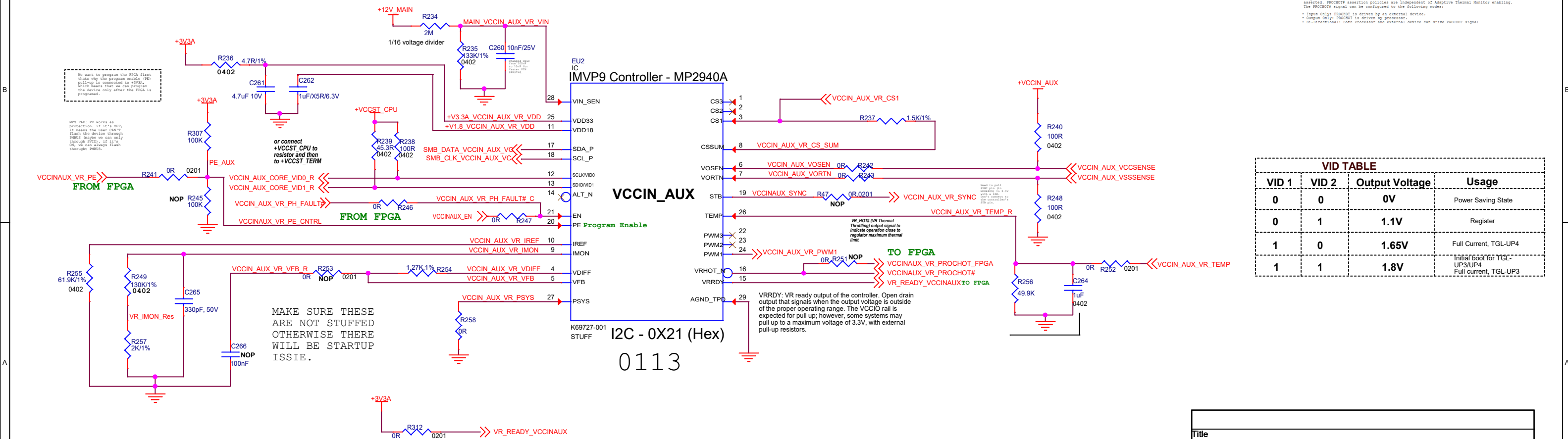
place as close as possible to DRAM.



VCCIN RAIL POWER CONVERSION

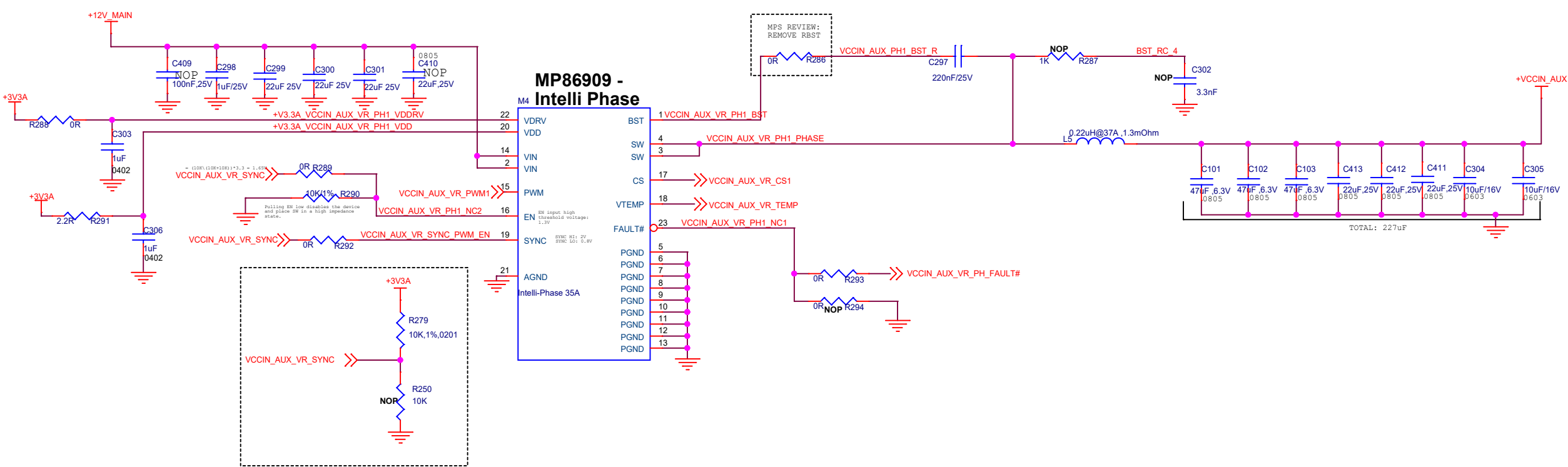


VCCIN AUX RAIL POWER CONVERSION

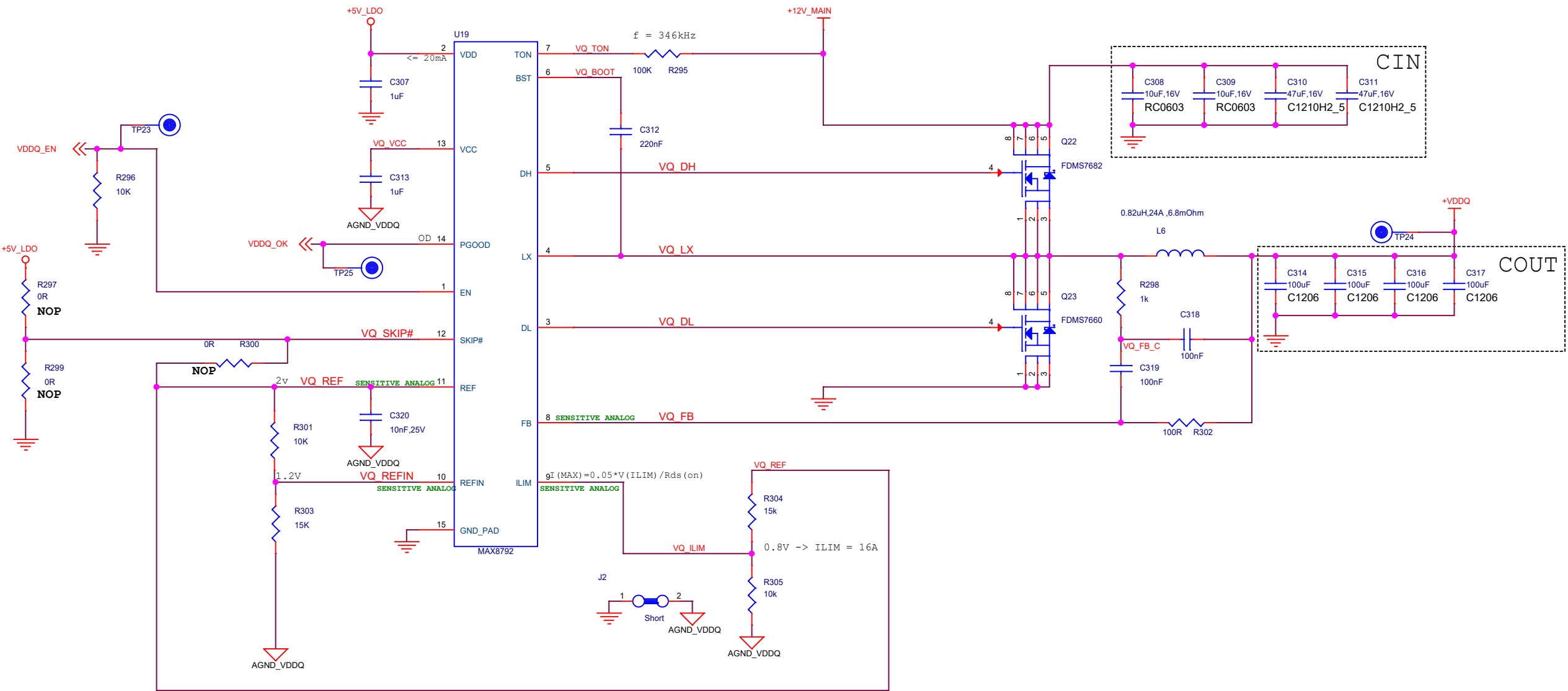


VID TABLE			
VID 1	VID 2	Output Voltage	Usage
0	0	0V	Power Saving State
0	1	1.1V	Register
1	0	1.65V	Full Current, TGL-UP4
1	1	1.8V	Initial boot for TGL-UP3/UP4 Full current, TGL-UP3

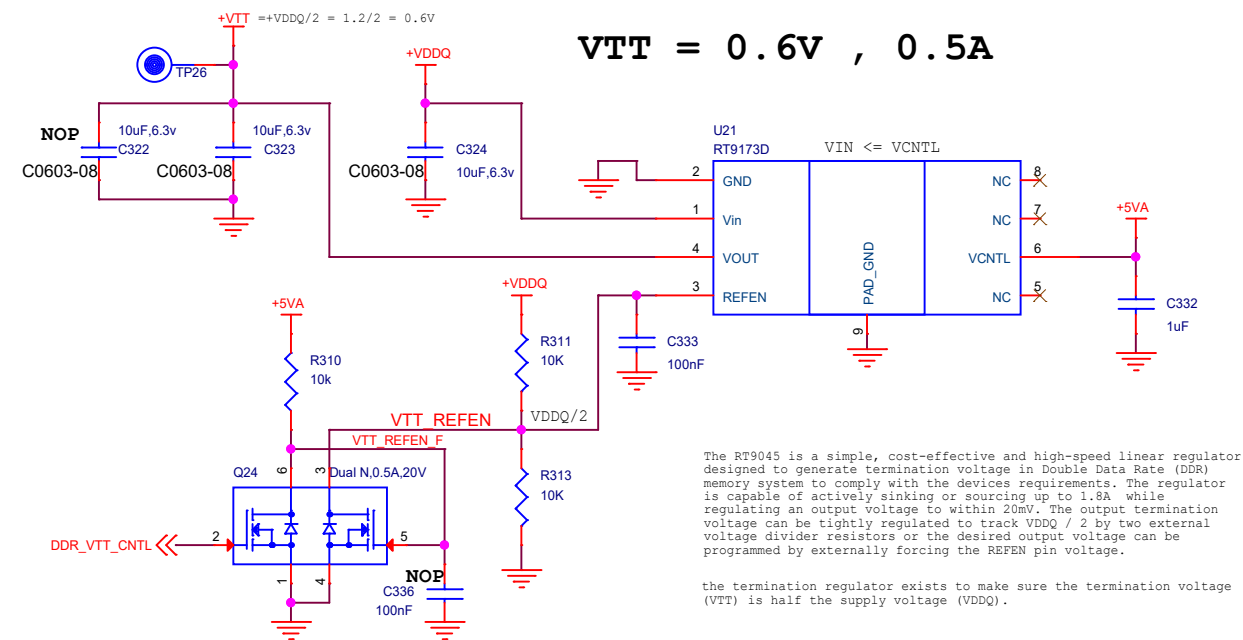
VCCIN_AUX POWER CONVERSION PHASE I



VDDQ = 1.2V , 15A



VTT = 0.6V , 0.5A

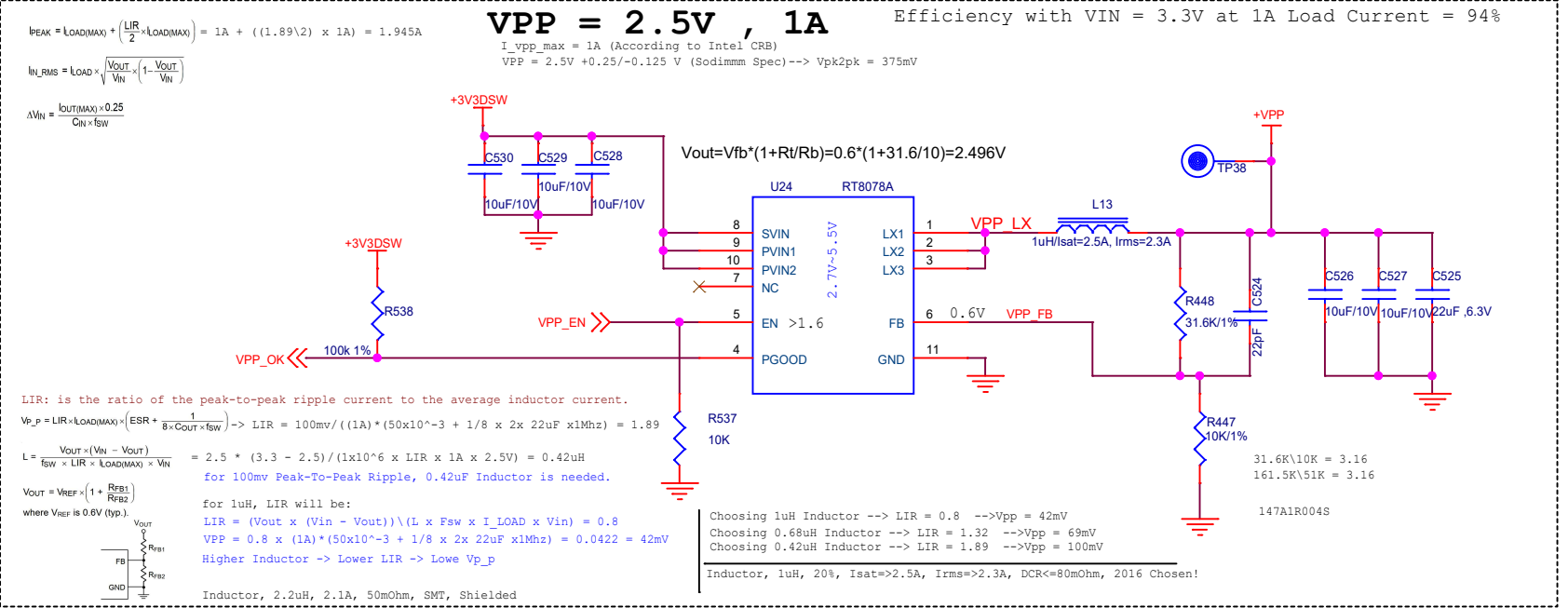


The RT9045 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in Double Data Rate (DDR) memory system to comply with the devices requirements. The regulator is capable of actively sinking or sourcing up to 1.8A while regulating an output voltage to within 20mV. The output termination voltage can be tightly regulated to track VDDQ / 2 by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

the termination regulator exists to make sure the termination voltage (VTT) is half the supply voltage (VDDQ).

VPP = 2.5V , 1A

Efficiency with VIN = 3.3V at 1A Load Current = 94%



LIR: is the ratio of the peak-to-peak ripple current to the average inductor current.

$$V_{p,p} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \rightarrow LIR = 100mV / ((1A) \times (50 \times 10^{-3} + 1/8 \times 2 \times 22\mu F \times 1MHz)) = 1.89$$

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}} = 2.5 \times (3.3 - 2.5) / (1 \times 10^6 \times 1.89 \times 1A \times 2.5V) = 0.42\mu H$$
for 100mV Peak-To-Peak Ripple, 0.42uF Inductor is needed.

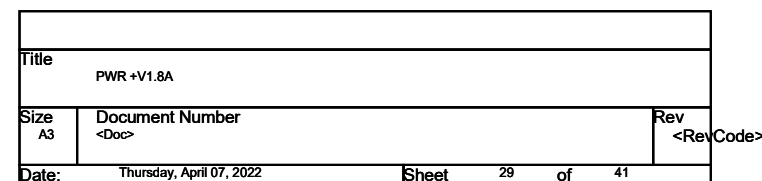
for 1uH, LIR will be:

$$LIR = (V_{OUT} \times (V_{IN} - V_{OUT})) / (L \times f_{SW} \times I_{LOAD} \times V_{IN}) = 0.8$$

$$VPP = 0.8 \times (1A) \times (50 \times 10^{-3} + 1/8 \times 2 \times 22\mu F \times 1MHz) = 0.0422 = 42mV$$
Higher Inductor -> Lower LIR -> Lower Vp,p

Choosing 1uH Inductor --> LIR = 0.8 --> Vpp = 42mV
Choosing 0.69uH Inductor --> LIR = 1.32 --> Vpp = 69mV
Choosing 0.42uH Inductor --> LIR = 1.89 --> Vpp = 100mV
Inductor, 2.2uH, 2.1A, 50mOhm, SMT, Shielded

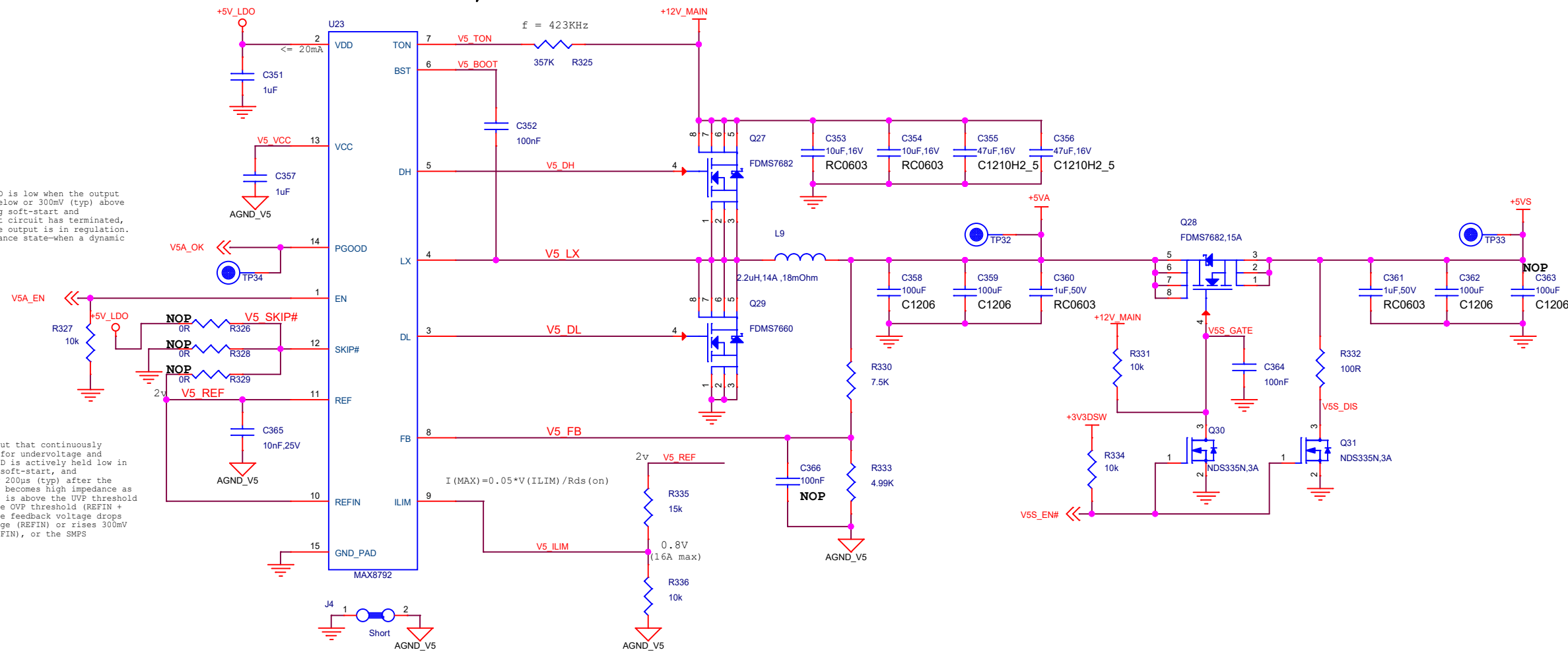
Title		
PWR VDDQ/VTT/VPP		
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5V , 15A

Open-Drain Power-Good Output. PGOOD is low when the output voltage is more than 200mV (typ) below or 300mV (typ) above the target voltage (VREFIN), during soft-start and soft-shutdown. After the soft-start circuit has terminated, PGOOD becomes high impedance if the output is in regulation. PGOOD is blanked-forced high-impedance state-when a dynamic REFIN transition is detected.

PGOOD is the open-drain output that continuously monitors the output voltage for undervoltage and overvoltage conditions. PGOOD is actively held low in shutdown (EN = GND), during soft-start, and soft-shutdown. Approximately 200ps (typ) after the soft-start terminates, PGOOD becomes high impedance as long as the feedback voltage is above the UVP threshold (REFIN - 200mV) and below the OVP threshold (REFIN + 300mV). PGOOD goes low if the feedback voltage drops 200mV below the target voltage (REFIN) or rises 300mV above the target voltage (REFIN), or the SMPS controller is shut down.



+5VA Plane stitching capacitors

C135-C154 (see in Ver4.5)

Title		
PWR 5V		
Size	Document Number	Rev
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Date:	Thursday, April 07, 2022	Sheet 30 of 41

PCH STRAPS

TOP SWAP OVERRIDE

GPP_B14

The strap has a 20 kohm \pm 30% internal pull-down.

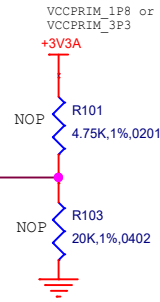
0=>Disable "Top Swap" mode. (Default)
1=>Enable "Top Swap" mode.

This inverts an address on access to SPI, so the processor fetches the alternate boot block instead of the original boot-block. PCH will invert the appropriate address lines (A[23:16]) as selected in Top Swap Block size soft strap.

1. The internal pull-down is disabled after PCH PWROK is high.
2. Software will not be able to clear the Top Swap (TS) bit (Bus0, Device31, Function0, offset DCh, bit 4) until the system is rebooted.
3. The status of this strap is readable using the Top Swap bit.
4. This signal is in the primary well.

Sampled at Rising edge of PCH_PWROK

OK



TLS CONFIDENTIALITY

GPP_CS / SML0ALERT#

ME TLS Confidentiality Strap (PU)

This strap has a 20 kohm \pm 30% internal pull-down.

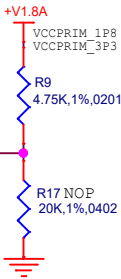
0=>Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1=>Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

Native FI if Intel SMBus ASD Mode Configuration soft strap = 1, else GP-Out; Strap read at rising edge of RSMRST#. The internal 20 kohm \pm 30% pull-down is disabled after RSMRST# de-asserts.

Sampled at Rising edge of RSMRST#

OK



NO REBOOT

GPP_B18 / GSPi0_MOSI

The strap has a 20 kohm \pm 30% internal pull-down.
0=>Disable "No Reboot" mode. (Default)
1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

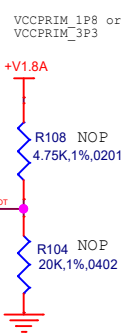
Notes:

1. The internal pull-down is disabled after PCH PWROK is high.
2. This signal is in the primary well.

HIGH - NO REBOOT
LOW- REBOOT ENABLED
WEAK INTERNAL PD 20K

Sampled at Rising edge of PCH_PWROK

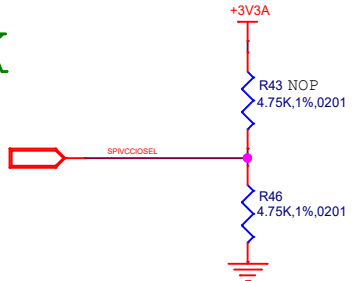
OK



STRAP FOR SPI 1.8V/3.3V SELECTION

(NOT A GPIO)

OK



There is no internal pull-up or pull-down on the strap. An external resistor is required.
0 = SPI voltage is 3.3 V (4.7 kohm pull-down to GND)
1 = SPI voltage is 1.8 V (4.7 kohm pull-up to VCCDSW_3P3)

Not sampled. This strap must always be driven to a valid logic level

DDP3 I2C / TBT LSX2 pins VCC configuration

GPP_D10 / ISH_SPI_CLK / DDP3_CTRLDATA / TBT_LSX2_RXD / BSSB_LS2_TX / GSPi2_CLK

Already Has 100K PU (R144) to 3V3S at the DP++ HANDLING (Page 22)

This strap has a 20 kohm \pm 30% internal pull-down.

0 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 1.8 V
1 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 3.3 V

Strap read at rising edge of RSMRST#. External pull-up is required if signal used as HDMI Display I2C. The internal 20 kohm \pm 30% pull-down is disabled after RSMRST# de-asserts

Sampled at Rising edge of RSMRST#

OK

VCCPRIM_1P8 or VCCPRIM_3P3

SPI0_IO2 STRAP - RSVD

PU PLACED NEXT TO SPI FLASH (U26)

SPI0_IO3 STRAP - RSVD

PU PLACED NEXT TO SPI FLASH (U26)

Flash Descriptor Security Override

GPP_R2 / HDA_SDO / I2S0_TXD STRAP

HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN

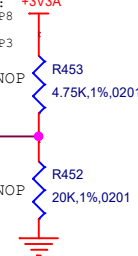
WEAK INTERNAL PD 20K

THIS SIGNAL IS TIED TO A JUMPER ON ATP CARD (IF JUMPER INSIDE HDA_SDO_ATP IS PULLED TO +3V3DSW THROUGH 1K PU)

Strap read at rising edge of PCH_PWROK. The internal 20 kohm \pm 30% pull-down is disabled after PCH_PWROK is high.

To support Intel® ME, a SPI flash is required on the platform with sufficient space to hold system BIOS, Intel® ME firmware, Intel® Integrated Sensor Solution firmware and any additional third party data storage. The SPI flash needs to be powered in states S0 through S5, independent of Intel® ME power state.
GPP_R2 / HDA_SDO / I2S0_TXD signal is used for Flash Descriptor Security Override (which is also known as Intel® ME Debug Mode). This signal input should be tied to a jumper which connects to power through an external pull-up (1 K Ω \pm 5%) only. When this signal is asserted, the Flash Security gets overridden for ease of image programming.

Sampled at Rising edge of PCH_PWROK



JTAG ODT DISABLE - GPP_E6

GPP_E6 / THC0_SPI1_RST#

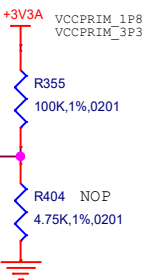
This strap does not have an internal pull-up or pull-down. External pull-up is recommended
0=> JTAG ODT is disabled
1=> JTAG ODT is enabled

CAD NOTE:

Strap read at rising edge of RSMRST#. External pull-up is required. Recommend 100 kohm. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

PLACE R355 AND R404 CLOSE TO THE SPI SIGNAL TO AVOID STUB

OK



USB_OC_CD#

10K PU at EB-TI22A

OK

GPP_E10 / THC0_SPI1_CS#

THC0_SPI1 Chip Select: Used to select the touch devices if it is connected to THC0_SPI1 interface.

THC NOT USED IN TENSOR-I22

CAD NOTE:

PLACE R414,R415 AND R422 CLOSE TO THE SPI SIGNAL TO AVOID STUB

OK

GPP_E11 / THC0_SPI1_CLK

THC0_SPI1 Clock: THC0 SPI1 clock output from PCH. Supports 20 Mhz, 33 Mhz and 50 Mhz.

THC NOT USED IN TENSOR-I22

CAD NOTE:

PLACE R429,R430 AND R431 CLOSE TO THE SPI SIGNAL TO AVOID STUB

OK

XTAL Frequency Selection

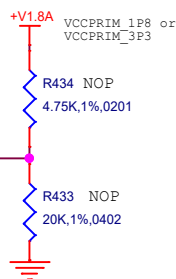
GPP_F0 / CNV_BRI_DT / UART0_RTS#

GPP_F0 Pin is at 0 (38.4 Mhz) by the internal PD.

This strap has a 20 kohm \pm 30% internal pull-down.
0 = 38.4 MHz (default)
1 = 24 MHz
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

OK



M.2 CNVi Mode Select

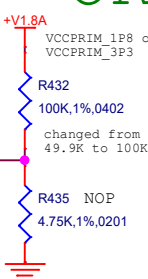
GPP_F2 / CNV_RGI_DT / UART0_TXD

A weak external PU is required to disable CNVi by default. When a companion chip is connected, the required PD on the device will pull the strap low to enable CNVi.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.
0= Integrated CNVi enabled.
1= Integrated CNVi disabled.
Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

Sampled at Rising edge of RSMRST#

OK



USB_OC_AB#

10K PU at EB-TI22A

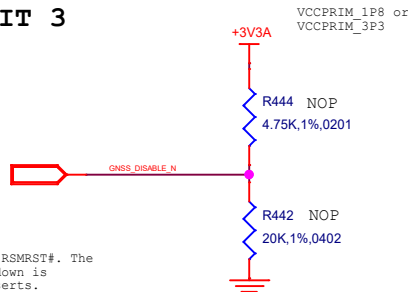
OK

BOOT STRAP - BIT 3

GPP_H2

Strap read at rising edge of RSMRST#. The internal 20 kohm \pm 30% pull-down is disabled after RSMRST# de-asserts.

OK

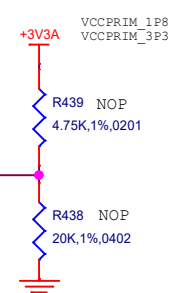


BOOT STRAP - BIT 1

GPP_H0

used for M2 PCH SSD RTD3, using AND between BUF_PLTRST# and GPPC_H0
Check TL-SBC (44/270)

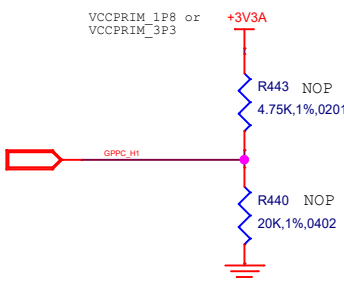
OK



BOOT STRAP - BIT 2

GPP_H1

OK



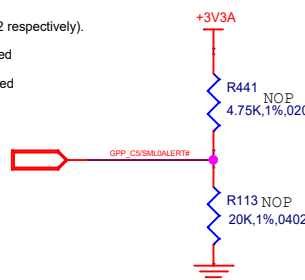
BOOT STRAP - BIT 0

This strap has a 20 kohm \pm 30% internal pull-down. This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration.
This strap is used in conjunction with Boot Strap 1,2,3. (on GPP_H0, GPP_H1, GPP_H2 respectively).
4-bit boot strap configuration encodings:
0000 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is enabled

0010 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / Intel CSME on eSPI attached device)
1100 = BIOS on eSPI peripheral Channel; Intel CSME on slave attached SPI.
Others: Reserved
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Strap read at rising edge of RSMRST#. The internal 20 kohm \pm 30% pull-down is disabled after RSMRST# de-asserts.

OK



Title			
PCH STRAPS (1 OF 2)			
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PCH STRAPS

DDP1 I2C / TBT_LSX0 pins VCC configuration

GPP_E19 / DDP1_CTRLDATA / TBT_LSX0_RXD / BSSB_LS0_TX

VCCPRIM_1P8
or
VCCPRIM_3P3

OK

Already Has 100K PU (R130) to 3V3S at the DP++ HANDLING (Page 21)

This strap has a 20 kohm ± 30% internal pull-down.
0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8 V
1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

there is 2.2K PU on DDP1_CTRLDATA

Sampled at Rising edge of RSMRST#

DDP2 I2C / TBT_LSX1 pins VCC configuration

GPP_E21 / DDP2_CTRLDATA / TBT_LSX1_RXD / BSSB_LS1_TX

NOTE: BSSB - Boundary Scan Sideband Low Speed Receive 1 for debug purposes

HIGH: 3.3V

LOW: 1.8V

Already Has 100K PU (R137) to 3V3S at the DP++ HANDLING (Page 22)

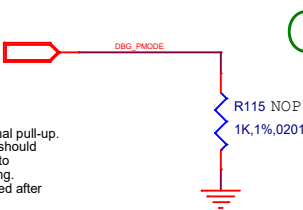
LSx Interface:
The PCH LSx interface enables communication between one thunderbolt controller to another. TGL UP3/UP4 supports 4 pairs of LSx signals. The LSx signals use a UART interface. It operates at a 1 MHz baud rate and shares identical electrical characteristics/routing guidelines as UART.

This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 1.8 V
1 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

DBG_PMODE

RESERVED



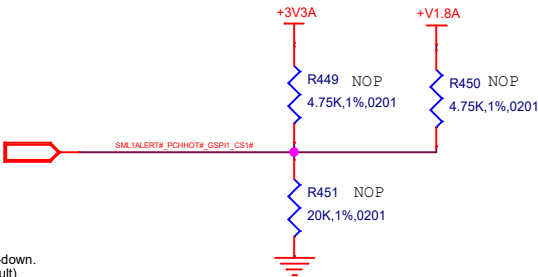
This strap has a 20 kohm ± 30% internal pull-up.
This strap should sample high. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-up is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

CPUNSSC CLOCK FREQ

GPP_B23 / SML1ALERT# / PCHHOT# / GSP11_CS1#

OK



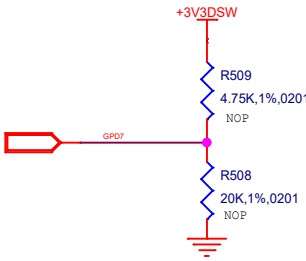
This strap has a 20 kohm ± 30% internal pull-down.
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal)
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150 kohm pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.

GPD7

STRAP: RESERVED

OK

Strap read at rising edge of DSW_PWR0K. The internal pull-down 20 kohm ± 30% is disabled after DSW_PWR0K is high. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



GPP_F10

STRAP: RESERVED

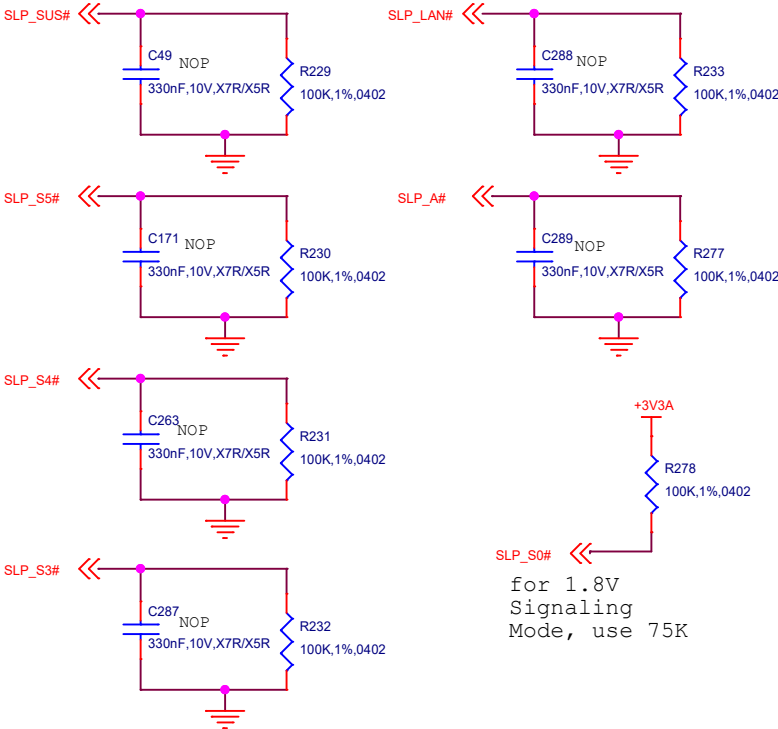
OK

This strap has a 20 kohm ± 30% internal pull-down.
This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

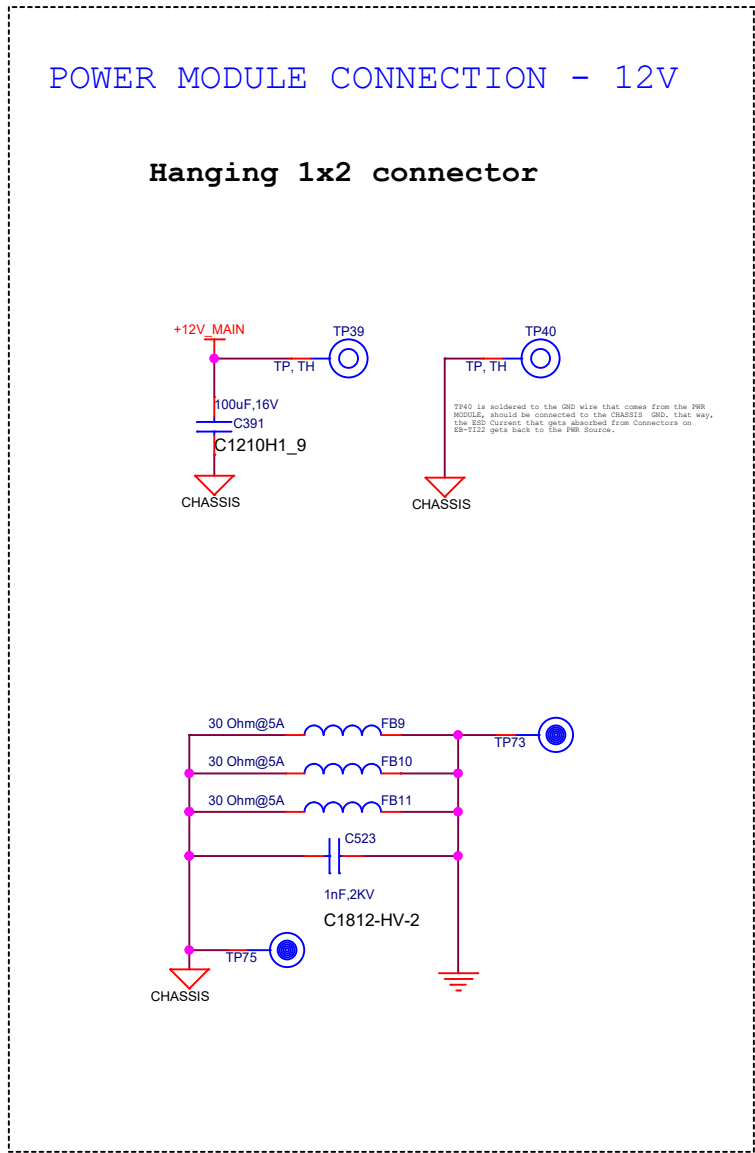
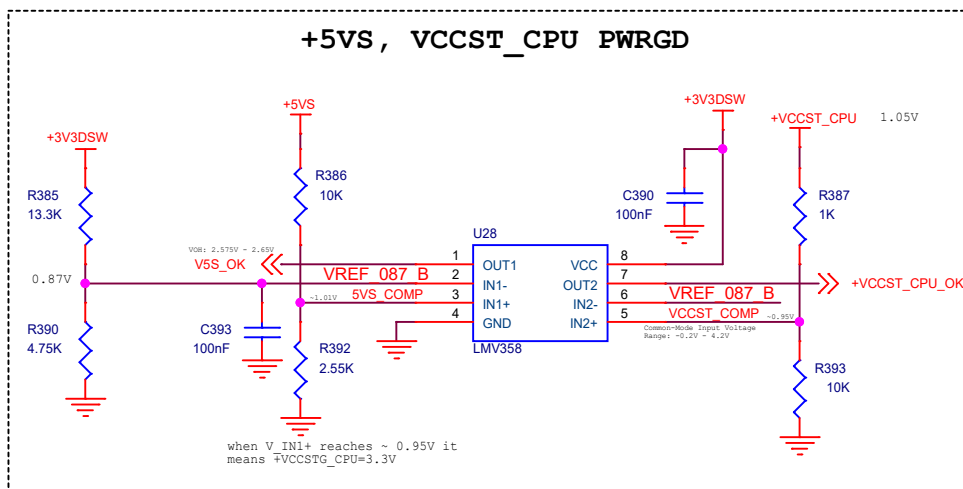
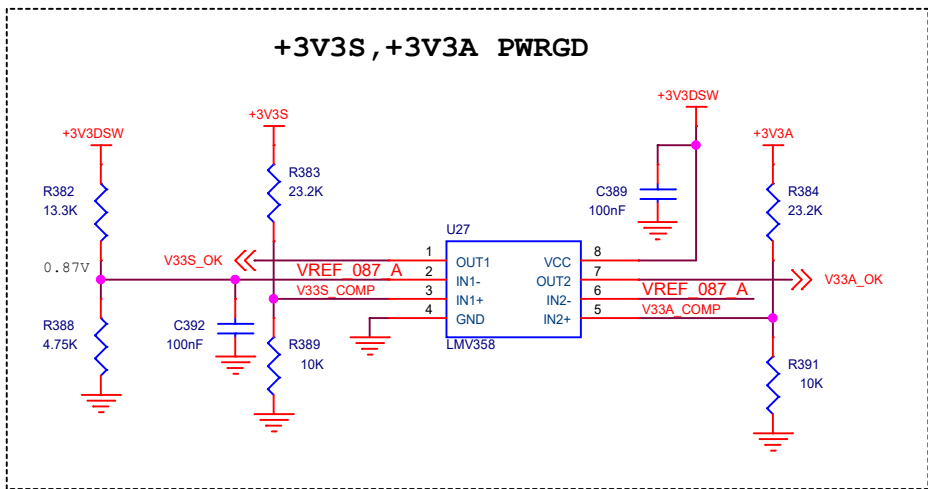
Sampled at Rising edge of RSMRST#

PCH GLITCH ISSUE MITIGATION

RC0201



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PCH STRAPS (2 OF 2)		
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Peak Current: 950mA

(Connectivity - WiFi/BT)

No need for the common mode filter on USB 2.0 interface. It doesn't go outside of the box.



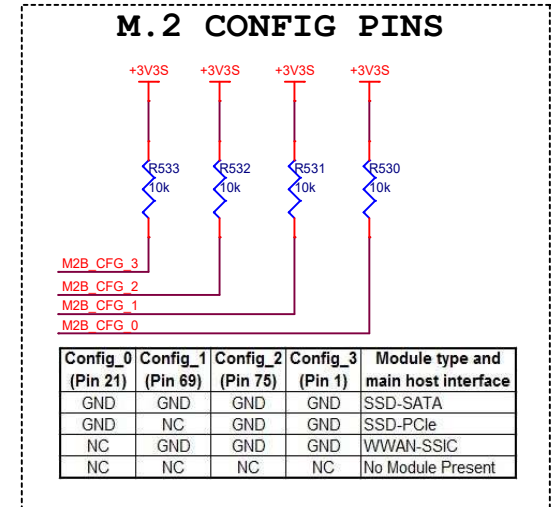
PIN 20: PCIE_DQS

The PCIE DQS signal is provided for host interface selection:

- PCIE single lane interface—Leave signal unconnected or tie to GND
- USB interface—Drive signal high (1.8V)

LOW: Min -0.3V, Typ:—, Max = 0.5V
High: Min 1.35V, Typ: 1.8V, MAX = 2.10V

No need for the common mode filter on USB 2.0 interface. It doesn't go outside of the box.

Product Side
Pinout EM919X

Pin	Signal name	Pin type ^a	Description	Direction ^b	Active state	Voltage levels (V)		
						Min	Typ	Max
41	PCIE_TXM0		PCie Negative Transmit Data0	Output	Differential	–	–	–
42	QTM1_PON ^d	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	–	1.8
					Low	0	–	0.45
43	PCIE_TXP0		PCie Positive Transmit Data0	Output	Differential	–	–	–
44	QTM2_PON ^d	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	–	1.8
					Low	0	–	0.45
45	GND	V	Ground	Input	Power	–	0	–
46	QTM3_PON ^d	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	–	1.8
					Low	0	–	0.45
47	PCIE_RXM0		PCie Negative Receive Data0	Input	Differential	–	–	–
48	QTM_IO_1.9V ^d	V	1.904 V power supply	Output	Power	1.8	1.904	2
49	PCIE_RXP0		PCie Positive Receive Data0	Input	Differential	–	–	–
50	PCIE_PERST_N		PCie Reset	Input	Low	0	–	0.7
					High	1.5	–	VCC
51	GND	V	Ground	Input	Power	–	0	–
52	PCIE_CLKREQ_N	OC	PCie Clock Request	Output	Low	0	–	0.35
53	PCIE_REFCLKM		PCie Negative Reference Clock	Input	Differential	–	–	–
54	PCIE_PEWAKE_N	OC	PCie Wake	Output	Low	0	–	0.35
55	PCIE_REFCLKP		PCie Positive Reference Clock	Input	Differential	–	–	–
56	NC		Reserved—Host must not repurpose this pin.					
57	GND	V	Ground	Input	Power	–	0	–
58	NC		Reserved—Host must not repurpose this pin.					
59	ANT_CTRL0		Antenna tuning control (low bands)	Output	High	1.35	–	1.8
				Output	Low	0	–	0.45
60	Reserved		Reserved—Host must not repurpose this pin.					
61	ANT_CTRL1		Antenna tuning control (low bands)	Output	High	1.35	–	1.80
				Output	Low	0	–	0.45

J8 NC

M3 Spacer SMT 2.5mm

J7 NC

M3 Spacer SMT 2.5mm

J6 NC

M3 Spacer SMT 2.5mm

Title M.2 B (WWAN)			
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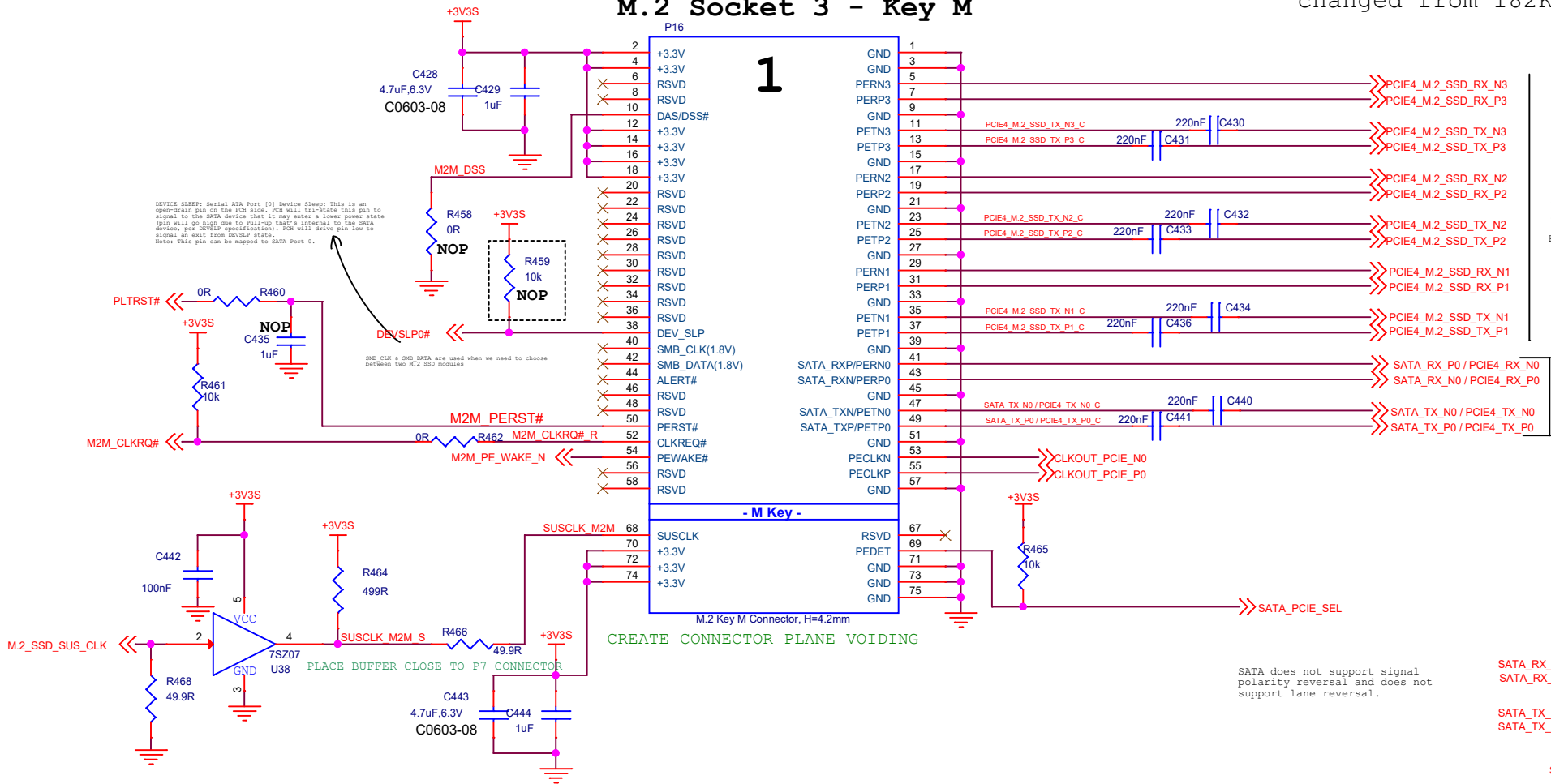
P 143/270 IN TL-SBC

980 PRO PCIe 4.0 NVMe M.2 250GB SSD

changed from H=4.2mm to H=6.7mm

changed from 182K06700S to 182K06706S

M.2 Socket 3 - Key M



A PCIe* Lane is composed of a single pair of Transmit (TX) and Receive (RX) differential pairs, for a total of four data wires per PCIe* Lane (such as, PCIe[3]_TXP/PCIe[3]_TXN and PCIe[3]_RXP/PCIe[3]_RXN make up PCIe Lane 3). A connection between two PCIe* devices is known as a PCIe* Link, and is built up from a collection of one or more PCIe* Lanes which make up the width of the link (such as bundling 2 PCIe* Lanes together would make a x2 PCIe* Link). A PCIe* Link is addressed by the lowest number PCIe* Lane it connects to and is known as the PCIe* Root Port (such as a x2 PCIe* Link connected to PCIe* Lanes 3 and 4 would be called x2 PCIe* Root Port 3).

PCIe-GEN4

PCIe Gen4 : 16.0 GT/s = 1.969 GB/s (per lane)

PCIe gen. 3
muxed with
SATA 3

SATA_RX_N0 / PCIe4_RX_P0
SATA_RX_P0 / PCIe4_RX_N0
SATA_TX_P0 / PCIe4_TX_N0
SATA_TX_N0 / PCIe4_TX_P0

SATA_PCIE_SEL

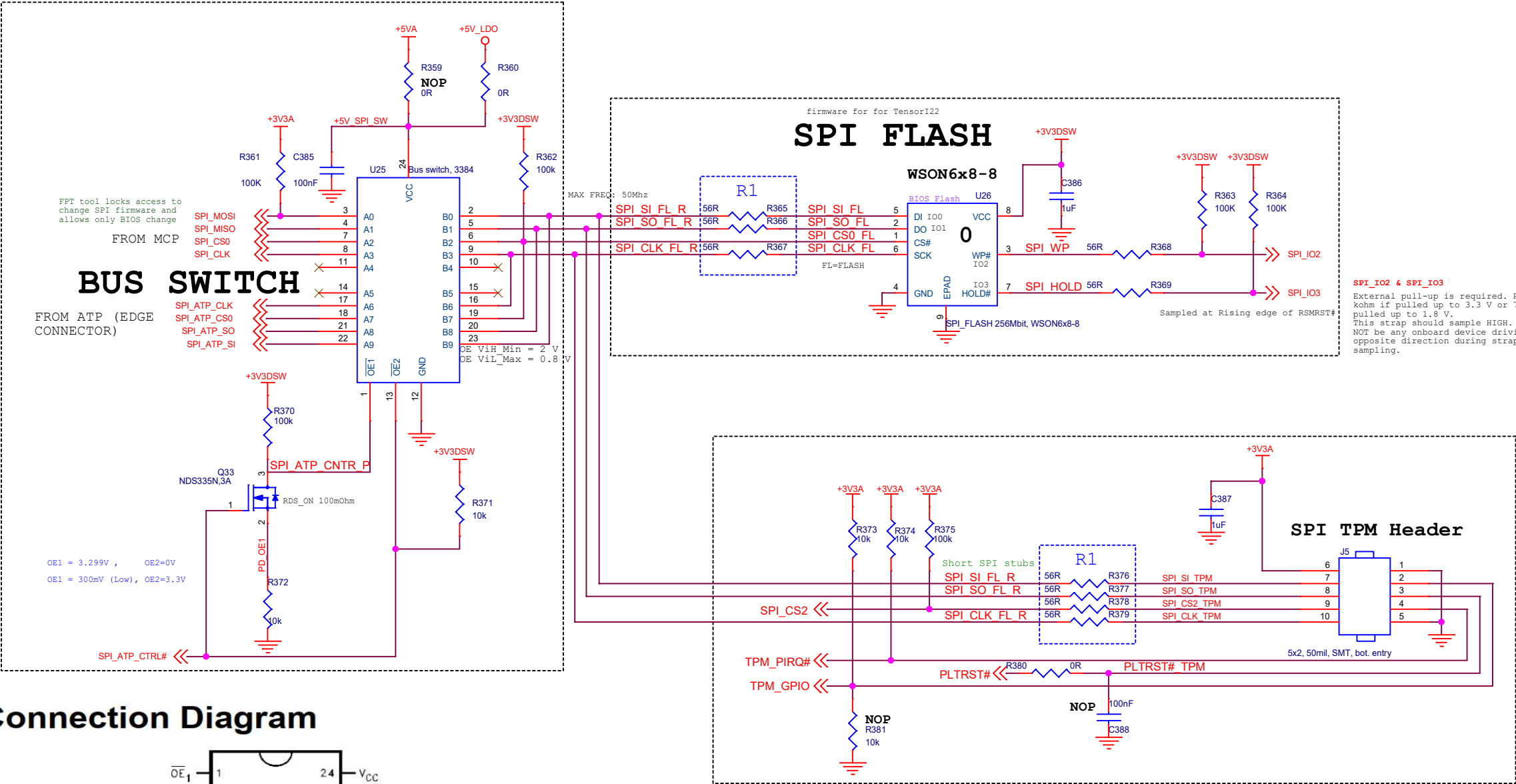
SATA #1
(From PCH)

PCIe-GEN4
(From CPU)

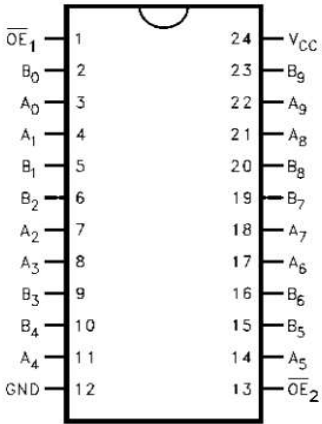
SATA #1 and PCIe-GEN4 come from two different sources which have constant type of signals.
It's not like SATAxPCIEx BX signals in SBC-CLH that could be SATA or PCIe.

Title		
M.2 M (SSD)		
Size	Document Number	Rev
A3	<Doc>	<RevCode>
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2-Load Branch MAF Topology (Master Attached Flash)

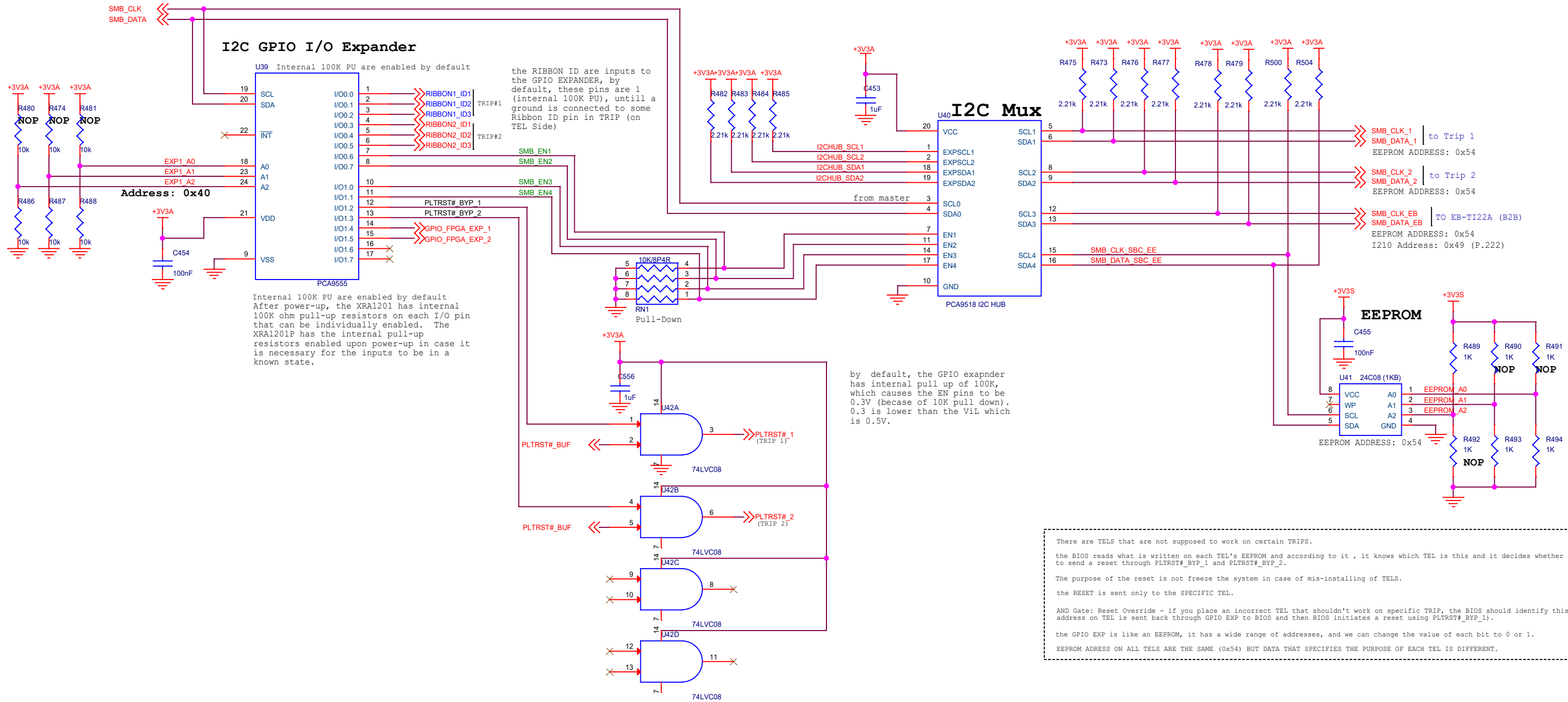


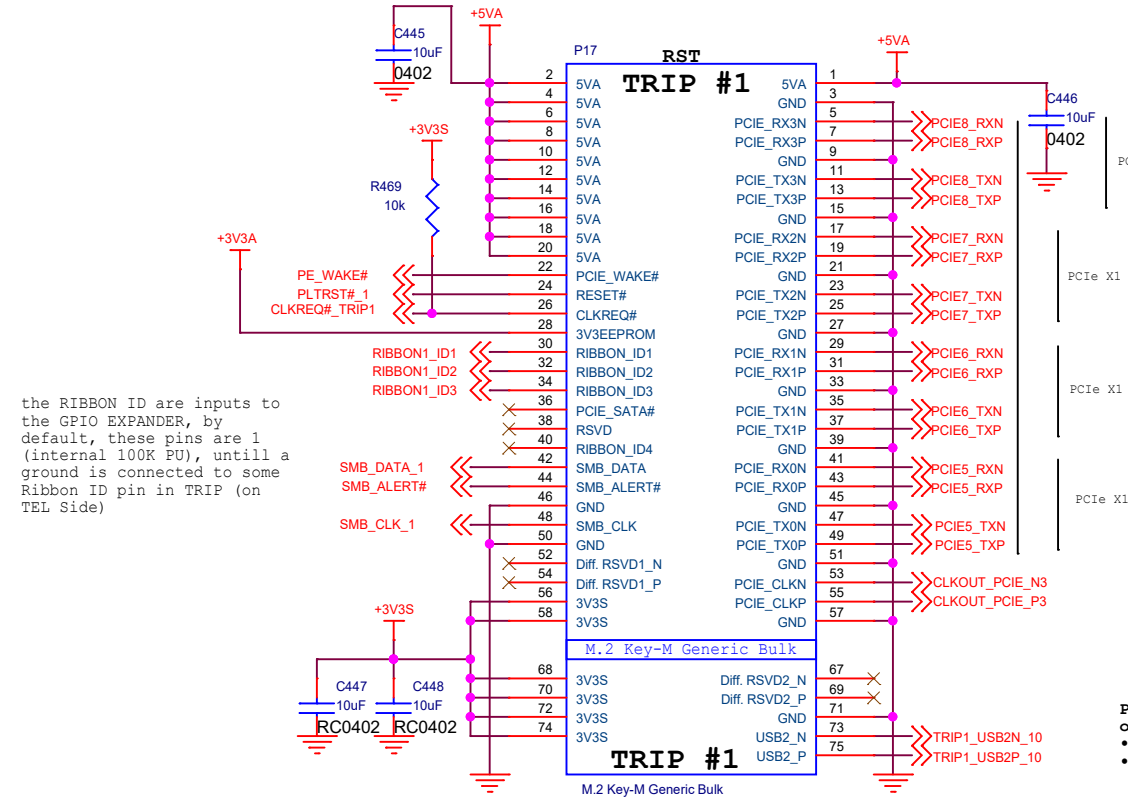
Connection Diagram



Truth Table

OE1	OE2	B0-B4	B5-B9	Function
L	L	A0-A4	A5-A9	Connect
L	H	A0-A4	HIGH-Z State	Connect
H	L	HIGH-Z State	A5-A9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

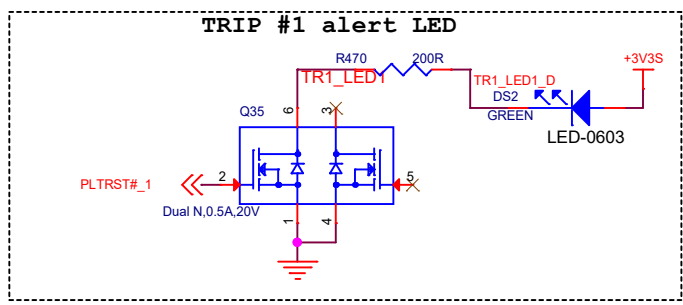




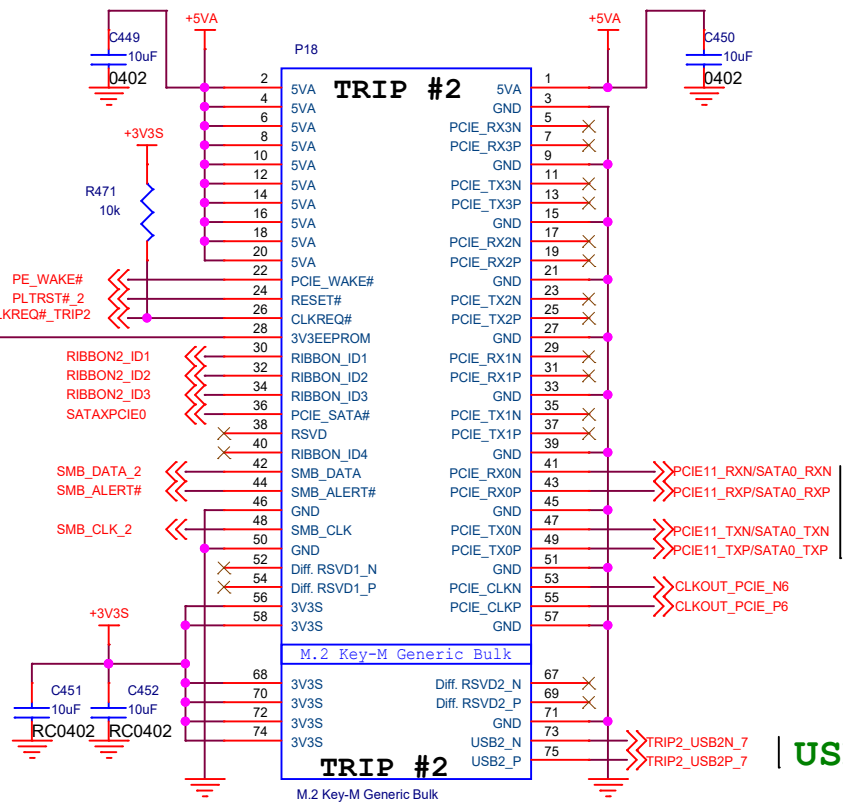
the RIBBON ID are inputs to the GPIO EXPANDER, by default, these pins are 1 (internal 100K PU), until a ground is connected to some Ribbon ID pin in TRIP (on TEL Side)

The TX capacitors should be near the connector of the device (in TRIP case, on the TEL), and the RX capacitors will be on the device's PCB.
If the PCIe is for a chip which is on you board, both TX and RX capacitors should be located near the device IC.

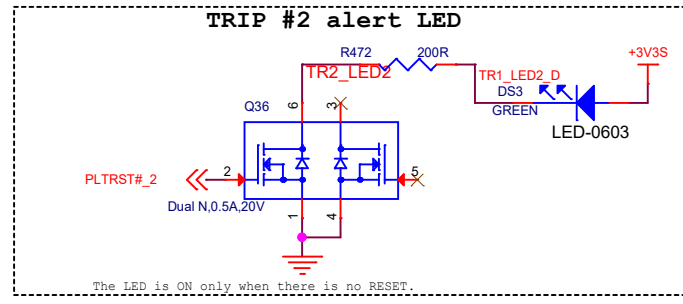
PCIE-GEN3



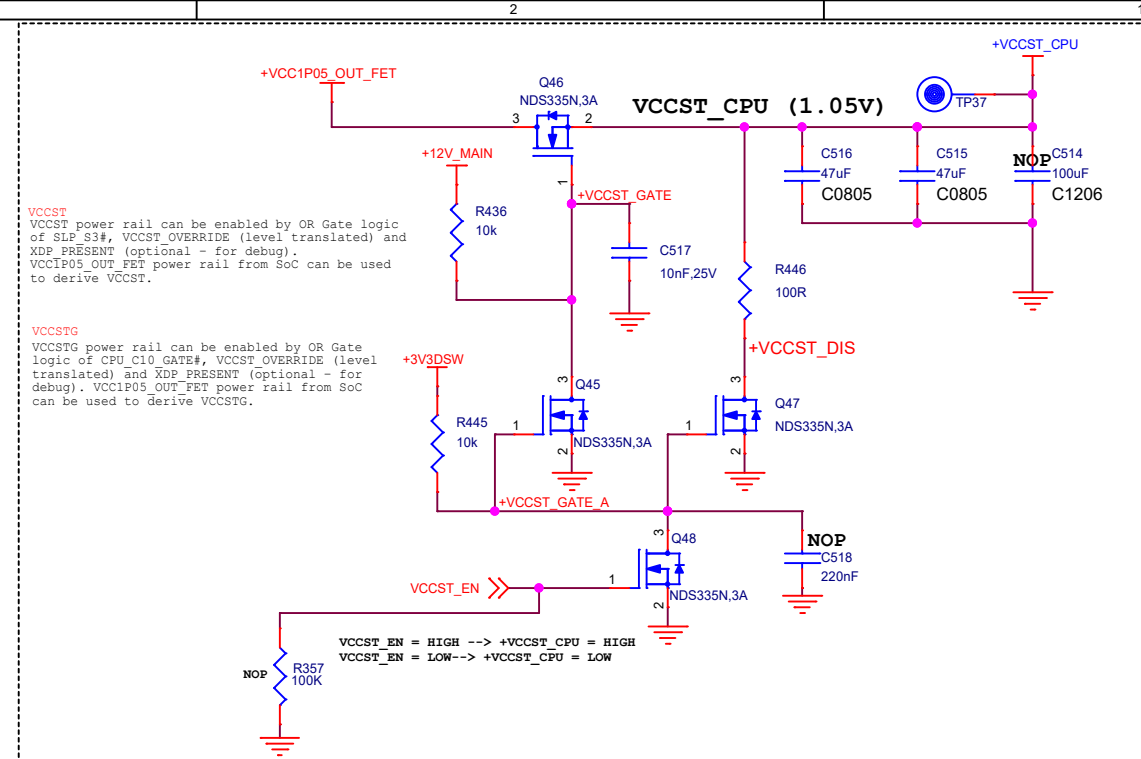
PCI Express* Clock Output: Serial Reference 100 Mhz PCIe* specification compliant differential output clocks to PCIe* devices
• CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support
• CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support



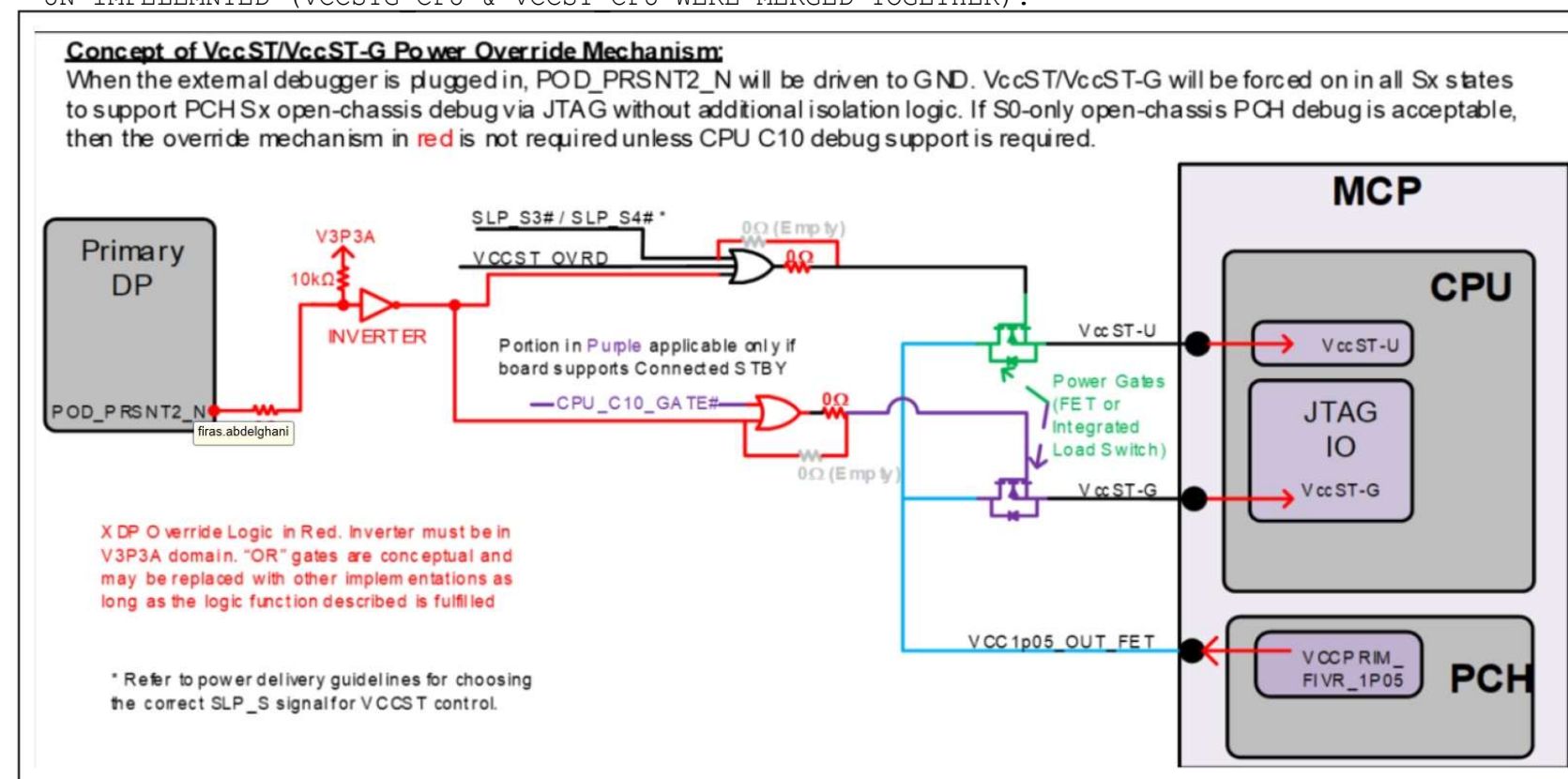
PCIE x1/SATA



USB 2.0



UN-IMPELEMNTED (VCCSTG CPU & VCCST CPU WERE MERGED TOGETHER) :



IN VOLUME: VccSTG gated by SLP_S3#

IN Premium, VccSTG gated by {CPU_C10_GATE#}

Figure 247. Premium PWROK Generation Flow Diagram

