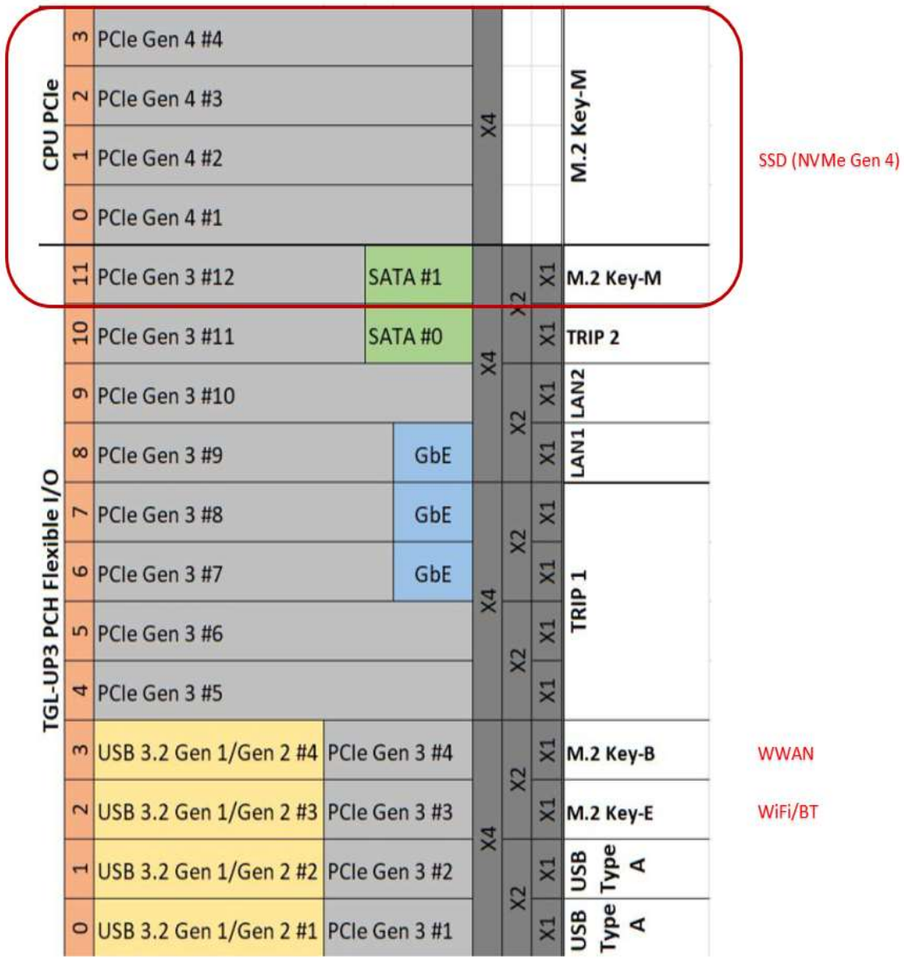
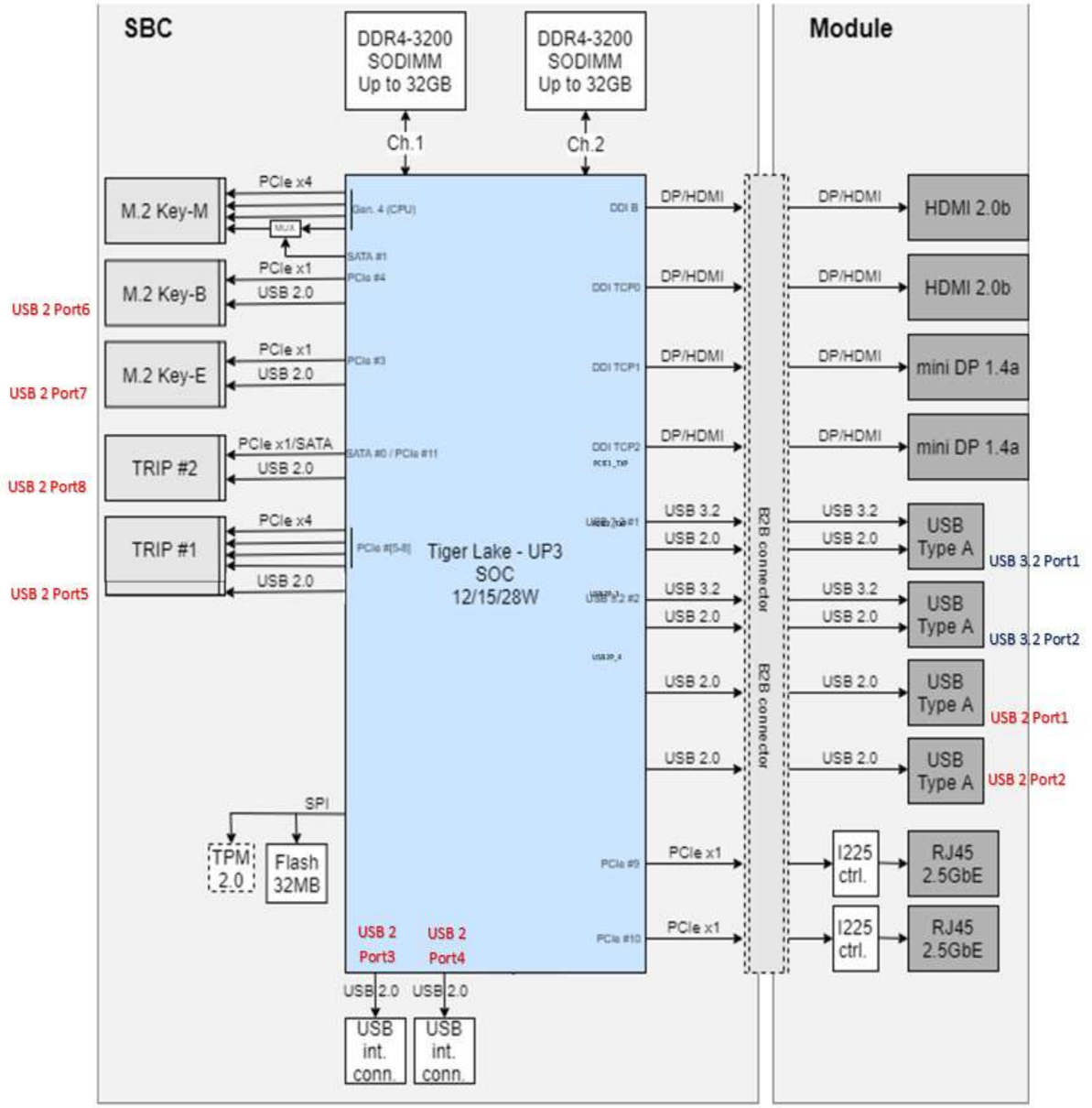


SSD (NVMe Gen 4)

WWAN

WiFi/BT



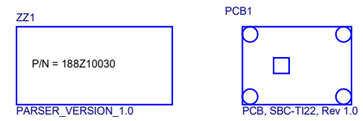
Tiger Lake UP3 Platform

Tiger Lake UP3 Key Feature Summary

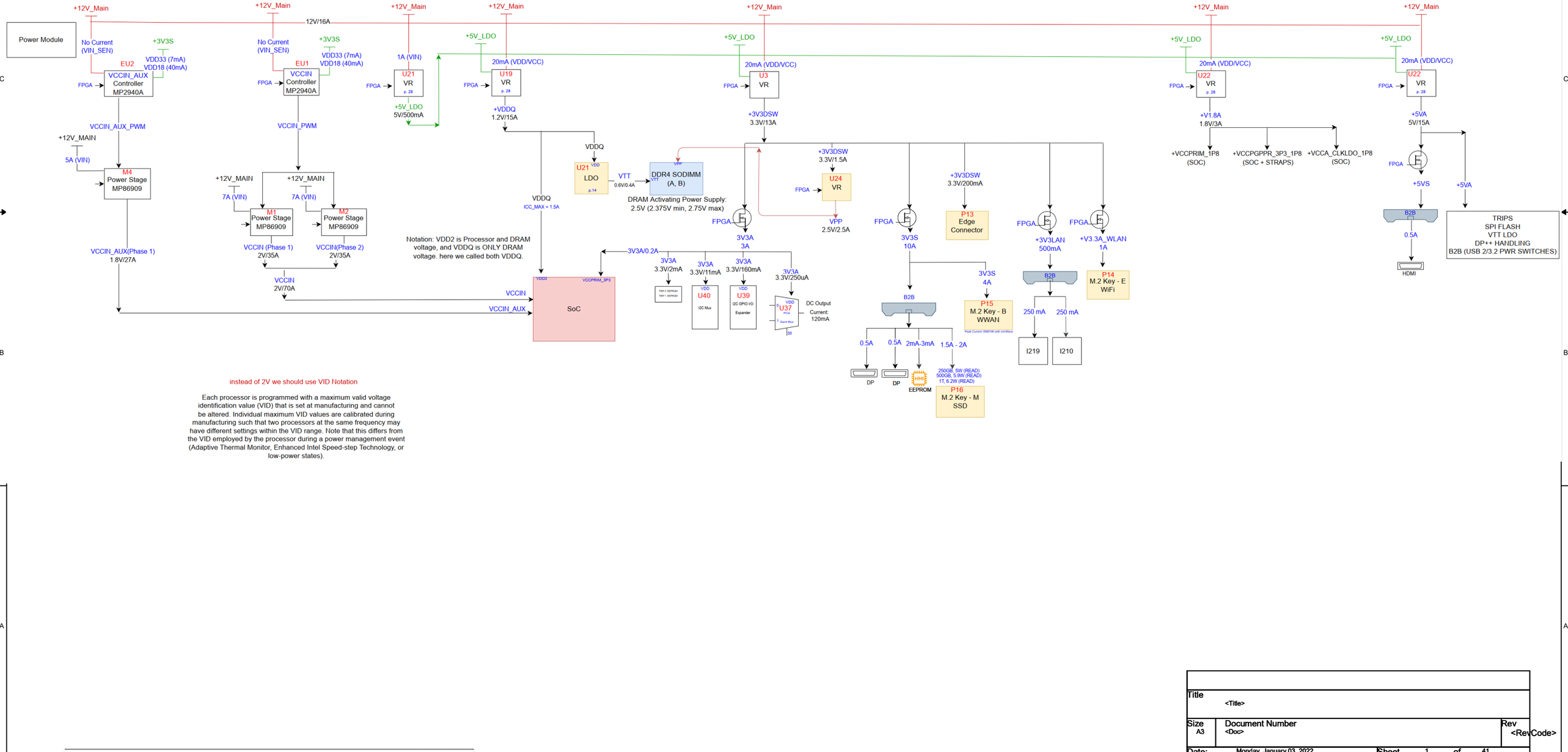
Feature	Description
Thermal (SoC)	UP3 4+2: 15W
SoC	TGL UP3 CPU (4+2) PCH – LP
CPU IO	PCIe Gen4, 4x Type-C (TBT, USB 4.0, DP), DDR4,LPDDR4x, LPDDR5, CSI, DSi, DDI, eDP
PCH-LP	12 lanes HSIO, USB2, USB 3.2, eSPI, SPI, LPSS, I2C, SMBus
Power Delivery	CPU FIVR/PCH FIVR w/discrete VR ROP USB-C PD Controller
Memory	DDR4 - Max 64GB @ 3200MT/s LPDDR4x - Max 32GB @ 4266MT/s
Storage	PCIe/SATA
Boot	SPI NOR
Discrete Graphics	Optional x4 PCIe – Hybrid Graphics support w/Hot Plug
Internal Display	eDP , MIPI DSI
External displays	4 Wired Type-C (DP/TBT) Wireless (Miracast2.0 r2) (Wi-Fi) DDI(DP, HDMI)
Wireless	Quasar CNVi w/Harrison Peak (Wi-Fi/BT) module WWAN – XMM 7560
Clocking	38.4MHz Platform Xtal
Wired COMMs	Integrated GbE w/ discrete Gbit Lan Phy

continued...

Feature	Description
Imaging	4x WF/UF 2D Camera – (13MP WF, 2MP UF, 2MP Others) Other Cameras: AutoFocus, Face Tracking, Image Biometrics
Docking/Walk-up-Port	4x Ports Max: Type-C/Type-A
Audio	3.5mm Headphone Jack, Integrated Speakers/Mic, Docking Soundwire, Intel HD Audio, I2S, USB
Sensors	Ambient Light Sensor, Gyroscope, Accelerometer, Compass, Proximity, Pressure
Misc, GPIO's	Power/Vol button/Indicator LEDs/Keyboard/Touchpad/etc



SBC-TI22 Power Diagram



instead of 2V we should use VID Notation

Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Adaptive Thermal Monitor, Enhanced Intel Speed-step Technology, or low-power states).

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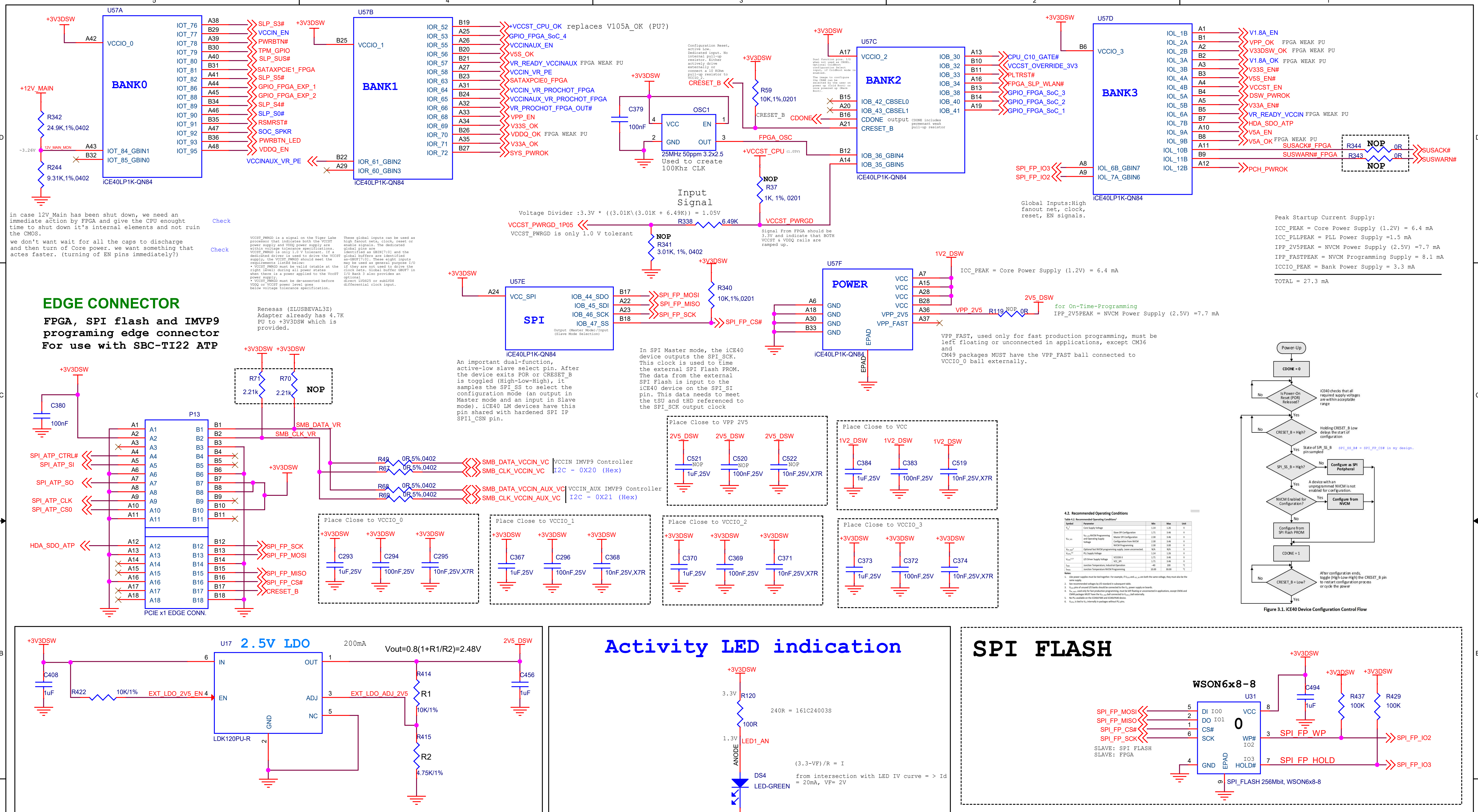

U57A
BANK0
VCCIO_0
IOT_84_GBIN1
IOT_85_GBIN0
iCE40LP1K-QN84
+3V3DSW
+12V_MAIN
R342
24.9K,1%,0402
R244
9.31K,1%,0402
SLP_S3#
VCCIN_EN
PWRBTN#
TPM_GPIO
SLP_SUS#
SATAXPCIE1_FPGA
SLP_S5#
GPIO_FPGA_EXP_1
GPIO_FPGA_EXP_2
SLP_S4#
SLP_S0#
RSMRST#
SOC_SPKR
PWRBTN_LED
VDDQ_EN
VCCINAUX_VR_PE
U57B
BANK1
VCCIO_1
IOR_61_GBIN2
IOR_60_GBIN3
iCE40LP1K-QN84
+VCCST_CPU_OK replaces V105A_OK (PU?)
GPIO_FPGA_SoC_4
VCCINAUX_EN
V5S_OK
VR_READY_VCCINAUX FPGA WEAK PU
VCCIN_VR_PE
SATAXPCIE0_FPGA
VCCIN_VR_PROCHOT_FPGA
VCCINAUX_VR_PROCHOT_FPGA
VR_PROCHOT_FPGA_OUT#
VPP_EN
V33S_OK
VDDQ_OK FPGA WEAK PU
V33A_OK
SYS_PWROK
OSC1
C379
100nF
25MHz 50ppm 3.2x2.5
Used to create
100Khz CLK
FPGA_OSC
CRESET_B
R59
10K,1%,0201
CDONE
U57C
BANK2
VCCIO_2
IOB_42_CBSEL0
IOB_43_CBSEL1
CDONE output
CRESET_B
IOB_36_GBIN4
IOB_35_GBIN5
iCE40LP1K-QN84
CPU_C10_GATE#
VCCST_OVERRIDE_3V3
PLTRST#
FPGA_SLP_WLAN#
GPIO_FPGA_SoC_3
GPIO_FPGA_SoC_2
GPIO_FPGA_SoC_1
+VCCST_CPU
NOP
R37
1K, 1%, 0201
Input
Signal
Voltage Divider :3.3V * ((3.01K\(3.01K + 6.49K)) = 1.05V
VCCST_PWRGD_1P05
R338 6.49K
VCCST_PWRGD
VCCST_PWRGD is only 1.0 V tolerant
NOP
R341
3.01K, 1%, 0402
Signal From FPGA should be 3.3V and indicate that BOTH VCCST & VDDQ rails are ramped up.
U57D
BANK3
VCCIO_3
IOL_6B_GBIN7
IOL_7A_GBIN6
iCE40LP1K-QN84
V1.8A_EN
VPP_OK FPGA WEAK PU
V33DSW_OK FPGA WEAK PU
V1.8A_OK FPGA WEAK PU
V33S_EN#
V5S_EN#
VCCST_EN
DSW_PWROK
V33A_EN#
VR_READY_VCCIN FPGA WEAK PU
HDA_SDO_ATP
V5A_EN
V5A_OK FPGA WEAK PU
SUSACK#_FPGA
SUSWARN#_FPGA
R344 0R
R343 0R
NOP
SUSACK#
SUSWARN#
PCH_PWROK
SPI_FP_IO3
SPI_FP_IO2
Global Inputs:High fanout net, clock, reset, EN signals.
in case 12V_Main has been shut down, we need an immediate action by FPGA and give the CPU enought time to shut down it's internal elements and not ruin the CMOS.
we don't want wait for all the caps to discharge and then turn of Core power. we want something that actes faster. (turning of EN pins immediately?)
Check
Check
Peak Startup Current Supply:
ICC_PEAK = Core Power Supply (1.2V) = 6.4 mA
ICC_PLLPEAK = PLL Power Supply =1.5 mA
IPP_2V5PEAK = NVCM Power Supply (2.5V) =7.7 mA
IPP_FASTPEAK = NVCM Programming Supply = 8.1 mA
ICCIO_PEAK = Bank Power Supply = 3.3 mA
TOTAL = 27.3 mA
EDGE CONNECTOR
FPGA, SPI flash and IMVP9 programing edge connector
For use with SBC-TI22 ATP
Renesas (ZLUSBEVAL3Z) Adapter already has 4.7K PU to +3V3DSW which is provided.
U57E
SPI
VCC_SPI
IOB_44_SDO
IOB_45_SDI
IOB_46_SCK
IOB_47_SS
iCE40LP1K-QN84
SPI_FP_MOSI
SPI_FP_MISO
SPI_FP_SCK
SPI_FP_CS#
R340
10K,1%,0201
An important dual-function, active-low slave select pin. After the device exits POR or CRESET_B is toggled (High-Low-High), it samples the SPI_SS to select the configuration mode (an output in Master mode and an input in Slave mode). iCE40 LM devices have this pin shared with hardened SPI IP SPI1_CSN pin.
In SPI Master mode, the iCE40 device outputs the SPI_SCK. This clock is used to time the external SPI Flash PROM. The data from the external SPI Flash is input to the iCE40 device on the SPI_SI pin. This data needs to meet the tSU and tHD referenced to the SPI_SCK output clock
U57F
POWER
VCC
GND
VPP_2V5
VPP_FAST
EPAD
iCE40LP1K-QN84
1V2_DSW
ICC_PEAK = Core Power Supply (1.2V) = 6.4 mA
2V5_DSW
VPP_2V5 R119 NOP 0R
for On-Time-Programming
IPP_2V5PEAK = NVCM Power Supply (2.5V) =7.7 mA
VPP_FAST, used only for fast production programming, must be left floating or unused in applications, except CM36 and CM49 packages MUST have the VPP_FAST ball connected to VCCIO_0 ball externally.
C380
100nF
P13
R71 2.21k
R70 2.21k
NOP
SMB_DATA_VR
SMB_CLK_VR
SPI_ATP_CTRL#
SPI_ATP_SI
SPI_ATP_SO
SPI_ATP_CLK
SPI_ATP_CS0
HDA_SDO_ATP
R49 0R,5%,0402
R67 0R,5%,0402
R68 0R,5%,0402
R69 0R,5%,0402
SMB_DATA_VCCIN_VC
SMB_CLK_VCCIN_VC
VCCIN IMVP9 Controller
I2C - 0X20 (Hex)
SMB_DATA_VCCIN_AUX_VC
SMB_CLK_VCCIN_AUX_VC
VCCIN_AUX IMVP9 Controller
I2C - 0X21 (Hex)
SPI_FP_SCK
SPI_FP_MOSI
SPI_FP_MISO
SPI_FP_CS#
CRESET_B
PCIE x1 EDGE CONN.
Place Close to VPP 2V5
C521 NOP 1uF,25V
C520 NOP 100nF,25V
C522 NOP 10nF,25V,X7R
Place Close to VCC
C384 1uF,25V
C383 100nF,25V
C519 10nF,25V,X7R
Place Close to VCCIO_0
C293 1uF,25V
C294 100nF,25V
C295 10nF,25V,X7R
Place Close to VCCIO_1
C367 1uF,25V
C296 100nF,25V
C368 10nF,25V,X7R
Place Close to VCCIO_2
C370 1uF,25V
C369 100nF,25V
C371 10nF,25V,X7R
Place Close to VCCIO_3
C373 1uF,25V
C372 100nF,25V
C374 10nF,25V,X7R
Figure 3.1. iCE40 Device Configuration Control Flow
U17 2.5V LDO 200mA
Vout=0.8(1+R1/R2)=2.48V
C408 1uF
R422 10K/1%
EXT_LDO_2V5_EN
EXT_LDO_ADJ_2V5
R414 R1 10K/1%
R415 R2 4.75K/1%
C456 1uF
LDK120PU-R
1.2V LDO 200mA
U14
Vout=0.8(1+R1/R2)=1.2V
C402 1uF
R413 10K/1%
EXT_LDO_EN
EXT_LDO_ADJ_1V2
R411 R1 10K/1%
R412 R2 20K/1%
C405 1uF
LDK120PU-R
Activity LED indication
R120 100R
240R = 161C24003S
LED1_AN
DS4 LED-GREEN
(3.3-VF)/R = I
from intersection with LED IV curve = > Id = 20mA, VF= 2V
LED1_CAT
Q32
for VGS=1.8 & Id=350mA , 0.7ohm <RDS_ON<0.9ohm
CDONE
VGS = 1.8V
Dual N,0.5A,20V
SPI FLASH
WSON6x8-8
U31
C494 1uF
R437 100K
R429 100K
SPI_FP_MOSI
SPI_FP_MISO
SPI_FP_CS#
SPI_FP_SCK
SLAVE: SPI FLASH
SLAVE: FPGA
SPI_FP_WP
SPI_FP_HOLD
SPI_FP_IO2
SPI_FP_IO3
SPI_FLASH 256Mbit, WSON6x8-8

The iCE40 LP/HX, iCE40 Ultra, iCE40 UltraLite and iCE40 UltraPlus device configuration mode is selected according to the following priority described below and illustrated in Figure 3.1. After exiting the Power-On Reset state or when CRESET_B returns High after being held Low, the iCE40 device samples the logical value on its SPI_SS pin. Like other programmable I/O pins, the SPI_SS pin has an internal pull-up resistor. Refer to iCE40 LP/HX Family Data Sheet (FPGA-DS-02029) for the minimum pulse width requirement of CRESET_B.

If the SPI_SS pin is sampled as a logic '1' (High), then … Check if the device is enabled to configure from the NVCM. If the NVCM is programmed, the device configures from NVCM.

If enabled to configure from NVCM, the device configures itself using the NVCM.

If not enabled to configure from NVCM, then the device configures using the SPI Master Configuration Interface.

If the SPI_SS pin is sampled as a logic '0' (Low), then the device waits to be configured from an external controller or from another device in SPI Master Configuration Mode using an SPI-like interface.

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TIGER LAKE PCH:

The PCH provides extensive I/O support. The functions and capabilities include:
- ACPI Power Management Logic Support, Revision 5.0a
- PCI Express Base Specification Revision 3.0
- Integrated Serial ATA Host controller 3.2, supports data transfer rates of up to 6 Gb/s on all ports
- USB 3.2 Gen 2x1 (10 Gb/s) eXtensible Host Controller (xHCI)
- USB 3.2 Gen 1x1 (5 Gb/s) Dual Role (eXtensible Device Controller - xDCI) Capability
- Serial Peripheral Interface (SPI)
- Enhanced Serial Peripheral Interface (eSPI)
- Flexible I/O—Allows some high speed I/O signals to be configured as PCIe or USB 3.2
- General Purpose Input Output (GPIO)
- Interrupt controller
- Timer functions
- System Management Bus (SMBus) Specification, Version 2.0
- Integrated Clock Controller (ICC)/Real Time Clock Controller (RTCC)
- Intel® High Definition Audio and Intel® Smart Sound Technology (Intel® SST), supporting I2S, MIPI* SoundWire*, and DMIC
- Intel® Serial I/O UART Host controllers
- Intel® Serial I/O I2C Host controllers
- Integrated 10/100/1000 Gigabit Ethernet MAC
- Integrated Sensor Hub (ISH)
- Supports Intel® Rapid Storage Technology (Intel® RST)
- Supports Intel® Active Management Technology (Intel® AMT) (AMT)
- Supports Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Supports Intel® Trusted Execution Technology (Intel® TXT)
- JTAG Boundary Scan support
- Intel® Trace Hub (Intel® TH) and Direct Connect Interface (DCI) for debug
- Supports Intel® CSME (CSME)
- Supports Integrated connectivity (CNVi)

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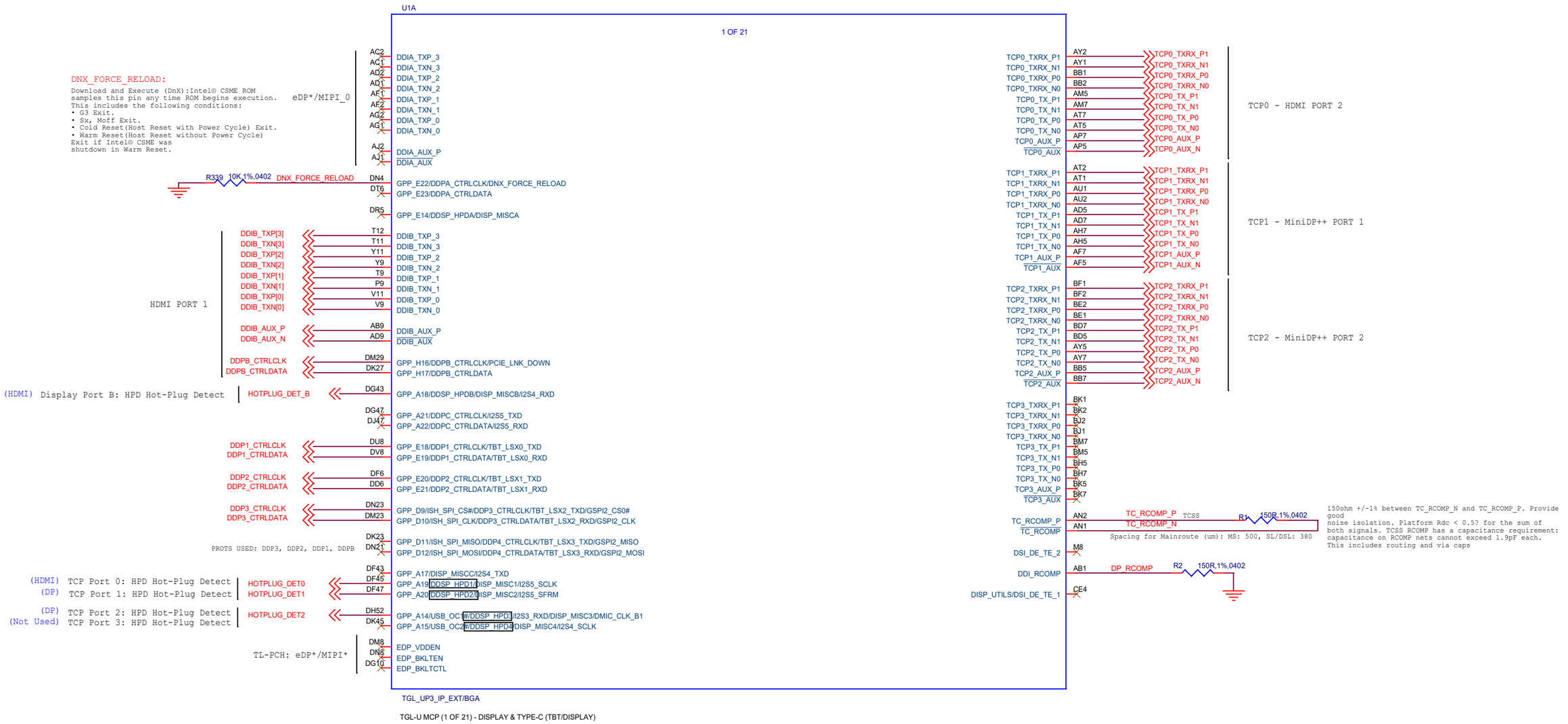
MCP -DP\HDMI



5.3 Display Interfaces

Table 33. DDI Ports Availability

SKU	UP4 Processor Line	UP3 Processor Line
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	eDP*/DP*/HDMI*/MIPI_1	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*
Note: HBR3 supported on TCP ports only. Each of the TCP port can support DPoC* (DisplayPort* over Type-C)		

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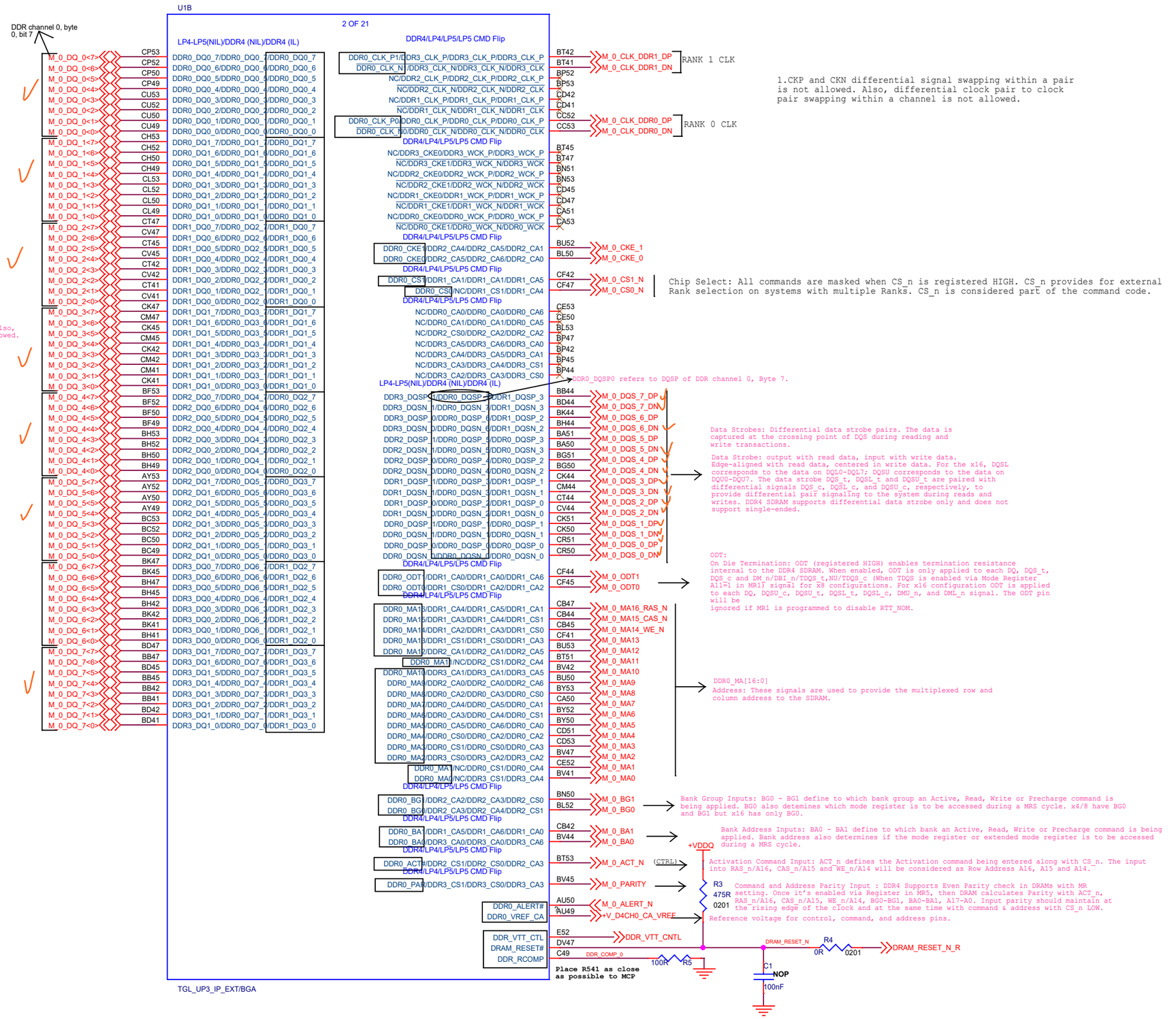
MEMORY CHANNEL A



1.CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.
2.DQ Bit swapping is allowed within the same byte
3.Byte Swapping is allowed within the same channel
4.DQSP and DQSN differential signal swapping within a pair is not allowed.

NOTES:

Each lane of 8bits (Byte) of Data has it's own Data Strobe

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS and register
BA0, BA1	Regsiter bank select input	SDA	I^2C serial data line for SPD/TS and register
BG0, BG1	Regsiter bank group select input	SA0-SA2	I^2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power
WE_n[4]	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12V	Optional Power Supply on socket but not used on RDIMM
CKE0, CEK1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of dif-ferential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.

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MEMORY CHANNEL B

AL53: DDR4_DQ0[7]/DDR1_DQ0[7]
DDR channel 4(1), Byte 0, Bit 7

U1C
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		LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_0<7>	AL53	DDR4_DQ0_7/DDR1_DQ0_7/DDR0_DQ4_7	DDR1_CLK_P1/DDR7_CLK_P/DDR7_CLK_P/DDR7_CLK_P	R41	M_1_CLK_DDR1_DP
M_1_DQ_0<6>	AL52	DDR4_DQ0_6/DDR1_DQ0_6/DDR0_DQ4_6	DDR1_CLK_N1/DDR7_CLK_N/DDR7_CLK_N/DDR7_CLK	R42	M_1_CLK_DDR1_DN
M_1_DQ_0<5>	AL50	DDR4_DQ0_5/DDR1_DQ0_5/DDR0_DQ4_5	NC/DDR6_CLK_P/DDR6_CLK_P/DDR6_CLK_P	M52	
M_1_DQ_0<4>	AL49	DDR4_DQ0_4/DDR1_DQ0_4/DDR0_DQ4_4	NC/DDR6_CLK_N/DDR6_CLK_N/DDR6_CLK	M53	
M_1_DQ_0<3>	AP53	DDR4_DQ0_3/DDR1_DQ0_3/DDR0_DQ4_3	NC/DDR5_CLK_P/DDR5_CLK_P/DDR5_CLK_P	AC42	
M_1_DQ_0<2>	AP52	DDR4_DQ0_2/DDR1_DQ0_2/DDR0_DQ4_2	NC/DDR5_CLK_N/DDR5_CLK_N/DDR5_CLK	AC41	
M_1_DQ_0<1>	AP50	DDR4_DQ0_1/DDR1_DQ0_1/DDR0_DQ4_1	DDR1_CLK_P0/DDR4_CLK_P/DDR4_CLKP/DDR4_CLK_P	Y52	M_1_CLK_DDR0_DP
M_1_DQ_0<0>	AP49	DDR4_DQ0_0/DDR1_DQ0_0/DDR0_DQ4_0	DDR1_CLK_N0/DDR4_CLK_N/DDR4_CLK_N/DDR4_CLK	Y53	M_1_CLK_DDR0_DN
M_1_DQ_1<7>	AF53	DDR4_DQ1_7/DDR1_DQ1_7/DDR0_DQ5_7	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_1<6>	AF52	DDR4_DQ1_6/DDR1_DQ1_6/DDR0_DQ5_6	NC/DDR7_CKE0/DDR7_WCK_P/DDR7_WCK_P	R47	
M_1_DQ_1<5>	AF50	DDR4_DQ1_5/DDR1_DQ1_5/DDR0_DQ5_5	NC/DDR7_CKE1/DDR7_WCK_N/DDR7_WCK	R45	
M_1_DQ_1<4>	AF49	DDR4_DQ1_4/DDR1_DQ1_4/DDR0_DQ5_4	NC/DDR6_CKE0/DDR6_WCK_P/DDR6_WCK_P	K51	
M_1_DQ_1<3>	AH53	DDR4_DQ1_3/DDR1_DQ1_3/DDR0_DQ5_3	NC/DDR6_CKE1/DDR6_WCK_N/DDR6_WCK	K53	
M_1_DQ_1<2>	AH52	DDR4_DQ1_2/DDR1_DQ1_2/DDR0_DQ5_2	NC/DDR5_CKE0/DDR5_WCK_P/DDR5_WCK_P	AC47	
M_1_DQ_1<1>	AH50	DDR4_DQ1_1/DDR1_DQ1_1/DDR0_DQ5_1	NC/DDR5_CKE1/DDR5_WCK_N/DDR5_WCK	AC45	
M_1_DQ_1<0>	AH49	DDR4_DQ1_0/DDR1_DQ1_0/DDR0_DQ5_0	NC/DDR4_CKE0/DDR4_WCK_P/DDR4_WCK_P	W51	
M_1_DQ_2<7>	AR41	DDR5_DQ0_7/DDR1_DQ2_7/DDR1_DQ4_7	NC/DDR4_CKE1/DDR4_WCK_N/DDR4_WCK	W53	
M_1_DQ_2<6>	AV42	DDR5_DQ0_6/DDR1_DQ2_6/DDR1_DQ4_6	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_2<5>	AR42	DDR5_DQ0_5/DDR1_DQ2_5/DDR1_DQ4_5	DDR1_CKE1/DDR6_CA4/DDR6_CA5/DDR6_CA1	P52	M_1_CKE_1
M_1_DQ_2<4>	AV41	DDR5_DQ0_4/DDR1_DQ2_4/DDR1_DQ4_4	DDR1_CKE0/DDR6_CA5/DDR6_CA6/DDR6_CA0	J50	M_1_CKE_0
M_1_DQ_2<3>	AR45	DDR5_DQ0_3/DDR1_DQ2_3/DDR1_DQ4_3	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_2<2>	AV45	DDR5_DQ0_2/DDR1_DQ2_2/DDR1_DQ4_2	DDR1_CS1/DDR5_CA1/DDR5_CA1/DDR5_CA5	AE42	M_1_CS1_N
M_1_DQ_2<1>	AR47	DDR5_DQ0_1/DDR1_DQ2_1/DDR1_DQ4_1	DDR1_CS0/NC/DDR5_CS1/DDR5_CA4	AE47	M_1_CS0_N
M_1_DQ_2<0>	AV47	DDR5_DQ0_0/DDR1_DQ2_0/DDR1_DQ4_0	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_3<7>	AJ41	DDR5_DQ1_7/DDR1_DQ3_7/DDR1_DQ5_7	NC/DDR7_CA5/DDR7_CA6/DDR7_CA0	N42	
M_1_DQ_3<6>	AJ42	DDR5_DQ1_6/DDR1_DQ3_6/DDR1_DQ5_6	NC/DDR7_CA4/DDR7_CA5/DDR7_CA1	N45	
M_1_DQ_3<5>	AL41	DDR5_DQ1_5/DDR1_DQ3_5/DDR1_DQ5_5	NC/DDR7_CA3/DDR7_CA4/DDR7_CS1	N44	
M_1_DQ_3<4>	AL42	DDR5_DQ1_4/DDR1_DQ3_4/DDR1_DQ5_4	NC/DDR7_CA2/DDR7_CA3/DDR7_CS0	N47	
M_1_DQ_3<3>	AJ45	DDR5_DQ1_3/DDR1_DQ3_3/DDR1_DQ5_3	NC/DDR6_CS0/DDR6_CA2/DDR6_CA2	J53	
M_1_DQ_3<2>	AJ47	DDR5_DQ1_2/DDR1_DQ3_2/DDR1_DQ5_2	NC/DDR4_CA1/DDR4_CA1/DDR4_CA5	AC50	
M_1_DQ_3<1>	AL45	DDR5_DQ1_1/DDR1_DQ3_1/DDR1_DQ5_1	NC/DDR4_CA0/DDR4_CA0/DDR4_CA6	AC53	
M_1_DQ_3<0>	AL47	DDR5_DQ1_0/DDR1_DQ3_0/DDR1_DQ5_0	LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)		
M_1_DQ_4<7>	A43	DDR6_DQ0_7/DDR1_DQ4_7/DDR0_DQ6_7	DDR7_DQSP_1/DDR1_DQSP_7/DDR1_DQSP_7	K36	M_1_DQS_7_DP
M_1_DQ_4<6>	B43	DDR6_DQ0_6/DDR1_DQ4_6/DDR0_DQ6_6	DDR7_DQSN_1/DDR1_DQSN_7/DDR1_DQSN_7	K38	M_1_DQS_7_DN
M_1_DQ_4<5>	D43	DDR6_DQ0_5/DDR1_DQ4_5/DDR0_DQ6_5	DDR7_DQSP_0/DDR1_DQSP_6/DDR1_DQSP_6	G44	M_1_DQS_6_DP
M_1_DQ_4<4>	E44	DDR6_DQ0_4/DDR1_DQ4_4/DDR0_DQ6_4	DDR7_DQSN_0/DDR1_DQSN_6/DDR1_DQSN_6	J44	M_1_DQS_6_DN
M_1_DQ_4<3>	A46	DDR6_DQ0_3/DDR1_DQ4_3/DDR0_DQ6_3	DDR6_DQSP_1/DDR1_DQSP_5/DDR0_DQSP_7	D39	M_1_DQS_5_DP
M_1_DQ_4<2>	B46	DDR6_DQ0_2/DDR1_DQ4_2/DDR0_DQ6_2	DDR6_DQSN_1/DDR1_DQSN_5/DDR0_DQSN_7	C39	M_1_DQS_5_DN
M_1_DQ_4<1>	D46	DDR6_DQ0_1/DDR1_DQ4_1/DDR0_DQ6_1	DDR6_DQSP_0/DDR1_DQSP_4/DDR0_DQSP_6	C45	M_1_DQS_4_DP
M_1_DQ_4<0>	E47	DDR6_DQ0_0/DDR1_DQ4_0/DDR0_DQ6_0	DDR6_DQSN_0/DDR1_DQSN_4/DDR0_DQSN_6	D45	M_1_DQS_4_DN
M_1_DQ_5<7>	E38	DDR6_DQ1_7/DDR1_DQ5_7/DDR0_DQ7_7	DDR5_DQSP_1/DDR1_DQSP_3/DDR1_DQSP_5	AJ44	M_1_DQS_3_DP
M_1_DQ_5<6>	D38	DDR6_DQ1_6/DDR1_DQ5_6/DDR0_DQ7_6	DDR5_DQSN_1/DDR1_DQSN_3/DDR1_DQSN_5	AL44	M_1_DQS_3_DN
M_1_DQ_5<5>	B38	DDR6_DQ1_5/DDR1_DQ5_5/DDR0_DQ7_5	DDR5_DQSP_0/DDR1_DQSP_2/DDR1_DQSP_4	AV44	M_1_DQS_2_DP
M_1_DQ_5<4>	A38	DDR6_DQ1_4/DDR1_DQ5_4/DDR0_DQ7_4	DDR5_DQSN_0/DDR1_DQSN_2/DDR1_DQSN_4	AR44	M_1_DQS_2_DN
M_1_DQ_5<3>	E41	DDR6_DQ1_3/DDR1_DQ5_3/DDR0_DQ7_3	DDR4_DQSP_1/DDR1_DQSP_1/DDR0_DQSP_5	AG51	M_1_DQS_1_DP
M_1_DQ_5<2>	D40	DDR6_DQ1_2/DDR1_DQ5_2/DDR0_DQ7_2	DDR4_DQSN_1/DDR1_DQSN_1/DDR0_DQSN_5	AG50	M_1_DQS_1_DN
M_1_DQ_5<1>	B40	DDR6_DQ1_1/DDR1_DQ5_1/DDR0_DQ7_1	DDR4_DQSP_0/DDR1_DQSP_0/DDR0_DQSP_4	AN51	M_1_DQS_0_DP
M_1_DQ_5<0>	A40	DDR6_DQ1_0/DDR1_DQ5_0/DDR0_DQ7_0	DDR4_DQSN_0/DDR1_DQSN_0/DDR0_DQSN_4	AN50	M_1_DQS_0_DN
M_1_DQ_6<7>	G42	DDR7_DQ0_7/DDR1_DQ6_7/DDR1_DQ6_7	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_6<6>	G41	DDR7_DQ0_6/DDR1_DQ6_6/DDR1_DQ6_6	DDR1_ODT1/DDR5_CA0/DDR5_CA0/DDR5_CA6	AE44	M_1_ODT1
M_1_DQ_6<5>	J41	DDR7_DQ0_5/DDR1_DQ6_5/DDR1_DQ6_5	DDR1_ODT0/DDR5_CS0/DDR5_CA2/DDR5_CA2	AE45	M_1_ODT0
M_1_DQ_6<4>	J42	DDR7_DQ0_4/DDR1_DQ6_4/DDR1_DQ6_4	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_6<3>	G45	DDR7_DQ0_3/DDR1_DQ6_3/DDR1_DQ6_3	DDR1_MA16/DDR5_CA4/DDR5_CA5/DDR5_CA1	AA47	M_1_MA16_RAS_N
M_1_DQ_6<2>	J45	DDR7_DQ0_2/DDR1_DQ6_2/DDR1_DQ6_2	DDR1_MA15/DDR5_CA3/DDR5_CA4/DDR5_CS1	AA44	M_1_MA15_CAS_N
M_1_DQ_6<1>	G47	DDR7_DQ0_1/DDR1_DQ6_1/DDR1_DQ6_1	DDR1_MA14/DDR5_CA2/DDR5_CA3/DDR5_CS0	AA45	M_1_MA14_WE_N
M_1_DQ_6<0>	J47	DDR7_DQ0_0/DDR1_DQ6_0/DDR1_DQ6_0	DDR1_MA13/DDR5_CS1/DDR5_CS0/DDR5_CA3	AE41	M_1_MA13
M_1_DQ_7<7>	G38	DDR7_DQ1_7/DDR1_DQ7_7/DDR1_DQ7_7	DDR1_MA12/DDR6_CA1/DDR6_CA1/DDR6_CA5	P53	M_1_MA12
M_1_DQ_7<6>	G36	DDR7_DQ1_6/DDR1_DQ7_6/DDR1_DQ7_6	DDR1_MA11/NC/DDR6_CS1/DDR6_CA4	N51	M_1_MA11
M_1_DQ_7<5>	H36	DDR7_DQ1_5/DDR1_DQ7_5/DDR1_DQ7_5	DDR1_MA10/DDR7_CA1/DDR7_CA1/DDR7_CA5	U42	M_1_MA10
M_1_DQ_7<4>	H38	DDR7_DQ1_4/DDR1_DQ7_4/DDR1_DQ7_4	DDR1_MA9/DDR6_CA0/DDR6_CA0/DDR6_CA6	P50	M_1_MA9
M_1_DQ_7<3>	N36	DDR7_DQ1_3/DDR1_DQ7_3/DDR1_DQ7_3	DDR1_MA8/DDR4_CA2/DDR4_CA3/DDR4_CS0	U53	M_1_MA8
M_1_DQ_7<2>	L36	DDR7_DQ1_2/DDR1_DQ7_2/DDR1_DQ7_2	DDR1_MA7/DDR4_CA4/DDR4_CA5/DDR4_CA1	W50	M_1_MA7
M_1_DQ_7<1>	L38	DDR7_DQ1_1/DDR1_DQ7_1/DDR1_DQ7_1	DDR1_MA6/DDR4_CA3/DDR4_CA4/DDR4_CS1	U52	M_1_MA6
M_1_DQ_7<0>	N38	DDR7_DQ1_0/DDR1_DQ7_0/DDR1_DQ7_0	DDR1_MA5/DDR4_CA5/DDR4_CA6/DDR4_CA0	U50	M_1_MA5
			DDR1_MA4/DDR4_CS0/DDR4_CA2/DDR4_CA2	AA51	M_1_MA4
			DDR1_MA3/DDR4_CS1/DDR4_CS0/DDR4_CA3	AA53	M_1_MA3
			DDR1_MA2/DDR7_CS0/DDR7_CA2/DDR7_CA2	U47	M_1_MA2
			DDR1_MA1/NC/DDR4_CS1/DDR4_CA4	AC52	M_1_MA1
			DDR1_MA0/NC/DDR7_CS1/DDR7_CA4	U41	M_1_MA0
			DDR4/LP4/LP5/LP5 CMD Flip		
			DDR1_BG1/DDR6_CA2/DDR6_CA3/DDR6_CS0	K50	M_1_BG1
			DDR1_BG0/DDR6_CA3/DDR6_CA4/DDR6_CS1	J52	M_1_BG0
			DDR4/LP4/LP5/LP5 CMD Flip		
			DDR1_BA1/DDR5_CA5/DDR5_CA6/DDR5_CA0	AA42	M_1_BA1
			DDR1_BA0/DDR7_CA0/DDR7_CA0/DDR7_CA6	U44	M_1_BA0
			DDR1_ACT#/DDR6_CS1/DDR6_CS0/DDR6_CA3	N53	M_1_ACT_N
			DDR1_PAR/DDR7_CS1/DDR7_CS0/DDR7_CA3	U45	M_1_PARITY
			DDR1_ALERT#	AU53	M_1_ALERT_N
			DDR1_VREF_CA	AU52	+V_D4CH1_CA_VREF

TGL_UP3_IP_EXT/BGA

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CATERR#

Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The
processor will set this signal for non-
recoverable machine check errors or other
unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.

PROCHOT#

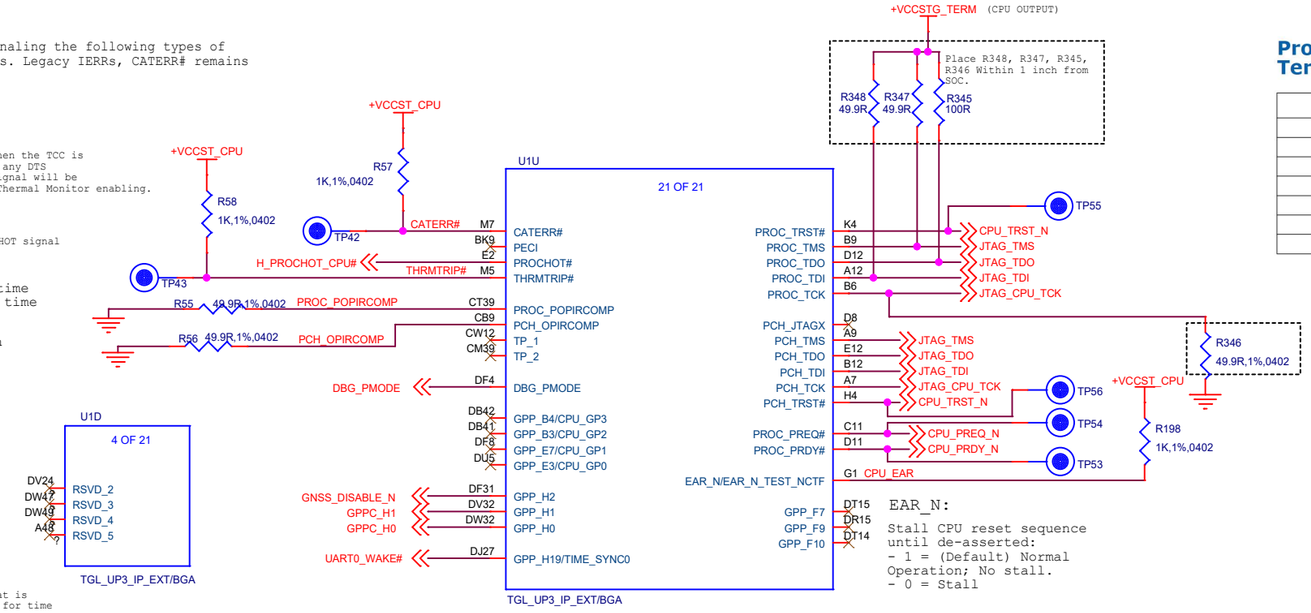
The PROCHOT# (processor hot) signal is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling. The PROCHOT# signal can be configured to the following modes:

- Input Only: PROCHOT is driven by an external device.
- Output Only: PROCHOT is driven by processor.
- Bi-Directional: Both Processor and external device can drive PROCHOT signal

Time Synchronization GPIO 0: Timed GPIO event for time synchronization for interfaces that do not support time synchronization natively.

Time Synchronization: Used for synchronization both input (latch time when pin asserted) and output (toggle pin when programmed time is hit).

TIME_SYNC:
The PCH supports two Timed GPIOs as native function (TIME_SYNC) that is muxed on GPIO pins. The intent usage of the Timed GPIO function is for time synchronization purpose.
Timed GPIO can be an input or an output.
- As an input, a GPIO input event triggers the HW to capture the PCH Always Running Timer (ART) time in the Time Capture register. The GPIO input event must be asserted for at least two crystal oscillator clocks period in order for the event to be recognized.
- As an output, a match between the ART time and the software programmed time value triggers the HW to generate a GPIO output event and capture the ART time in the Time Capture register. If periodic mode is enabled, HW generates the
periodic GPIO events based on the programmed interval. The GPIO output event is asserted by HW for at least two crystal oscillator clocks period.



Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM#[3:0]	Pull Up/Pull Down	VCC_{IO_OUT}	16-60 Ω
PROC_PREQ#	Pull Up	VCC_{STG}	3 KΩ
PROC_TDI	Pull Up	VCC_{STG}	3 KΩ
PROC_TMS	Pull Up	VCC_{STG}	3 KΩ
PROC_TRST#	Pull Down	VCC_{STG}	3 KΩ
PROC_TCK	Pull Down	VCC_{STG}	3 KΩ
CFG[17:0]	Pull Up	VCC_{IO_OUT}	3 KΩ

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BPM#[3:0]	**Breakpoint and Performance Monitor Signals:** Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	UP3/UP4/H Processor Lines
PROC_PRDY#	**Probe Mode Ready:** PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	O	OD	SE	UP3/UP4/H Processor Lines
PROC_PREQ#	**Probe Mode Request:** PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TCK	**Test Clock:** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal should be driven low or allowed to float during power on Reset.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TDI	**Test Data In:** This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TDO	**Test Data Out:** This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O	OD	SE	UP3/UP4/H Processor Lines
PROC_TMS	**Test Mode Select:** A JTAG specification support signal used by debug tools.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TRST#	**Test Reset:** Resets the Test Access Port (TAP) logic. This signal should be driven low during power on Reset. Refer to the appropriate processor Debug Port Design Guide (Refer to Section 1.10, "Related Documents") for complete implementation details.	I	GTL	SE	UP3/UP4/H Processor Lines

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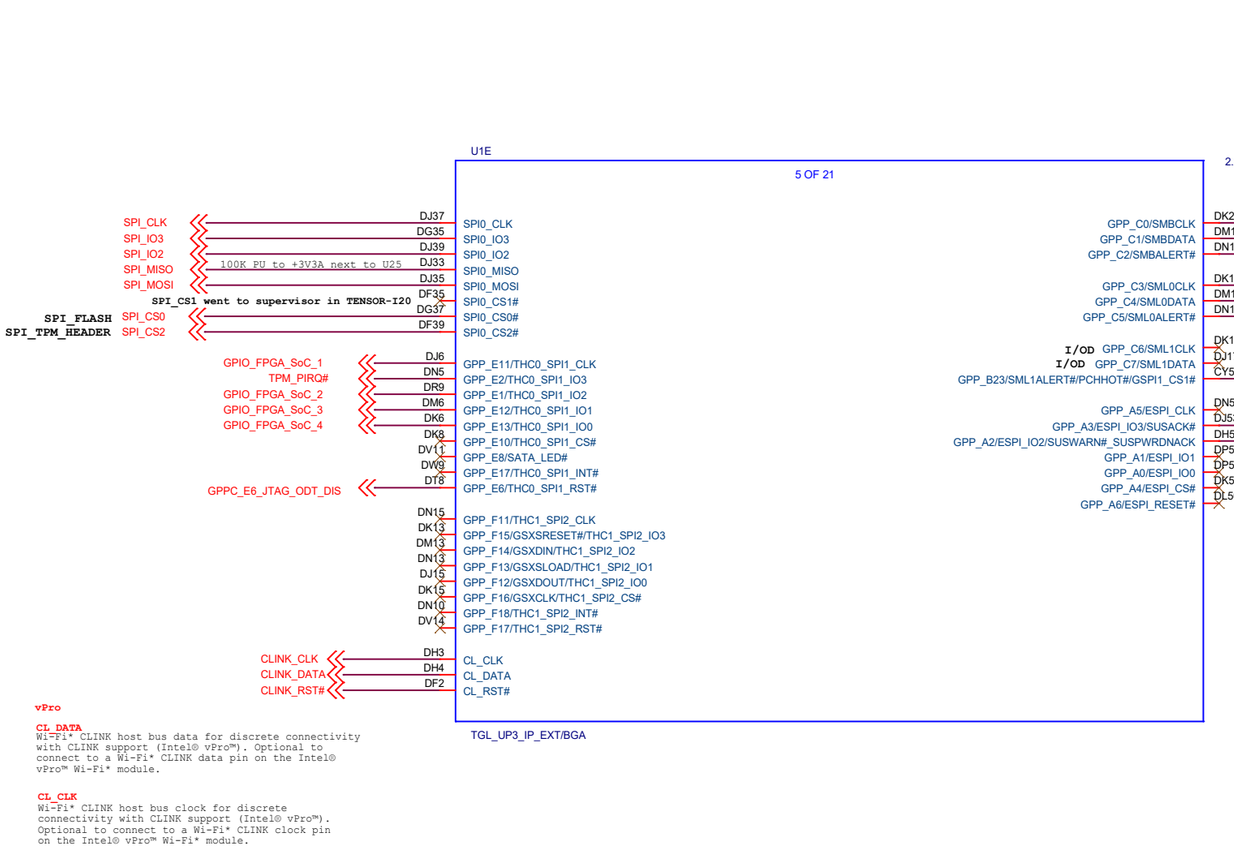
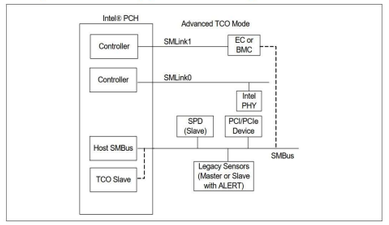


SML0CLK & SML0DATA
System Management Link clock signal interface to Intel® Ethernet Connection I219. Refer to System Management Interface and SMLink for details on the SML0CLK signal.
Note: The Intel® Ethernet Connection I219 connects to SML0CLK signal.

FUNCTIONALITY:
The SMLink interfaces are controlled by the Intel® CSME.
SMLink0 is mainly used for integrated LAN. When an Intel LAN PHY is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of up to 1 MHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled using a soft strap.
SMLink1 can be used with an Embedded Controller (EC) or Baseboard Management Controller (BMC). Both SMLink0 and SMLink1 support up to 1 MHz.

SUSACK# & SUSWARN#:
This function is only applicable to platforms supporting Deep Sleep Wells
This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (using SLP_SUS#). The EC/ motherboard control logic must observe edges on this pin, preparing
for Primary well power loss on a falling edge and preparing for Prim
well related activity (host/Intel ME wakes and runtime events) on a
rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#.

SMBus / SMlink Connectivity (Advanced TCO Mode)



vPro

CL_DATA
Wi-Fi* CLINK host bus data for discrete connectivity with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK data pin on the Intel® vPro™ Wi-Fi* module.

CL_CLK
Wi-Fi* CLINK host bus clock for discrete connectivity with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK clock pin on the Intel® vPro™ Wi-Fi* module.

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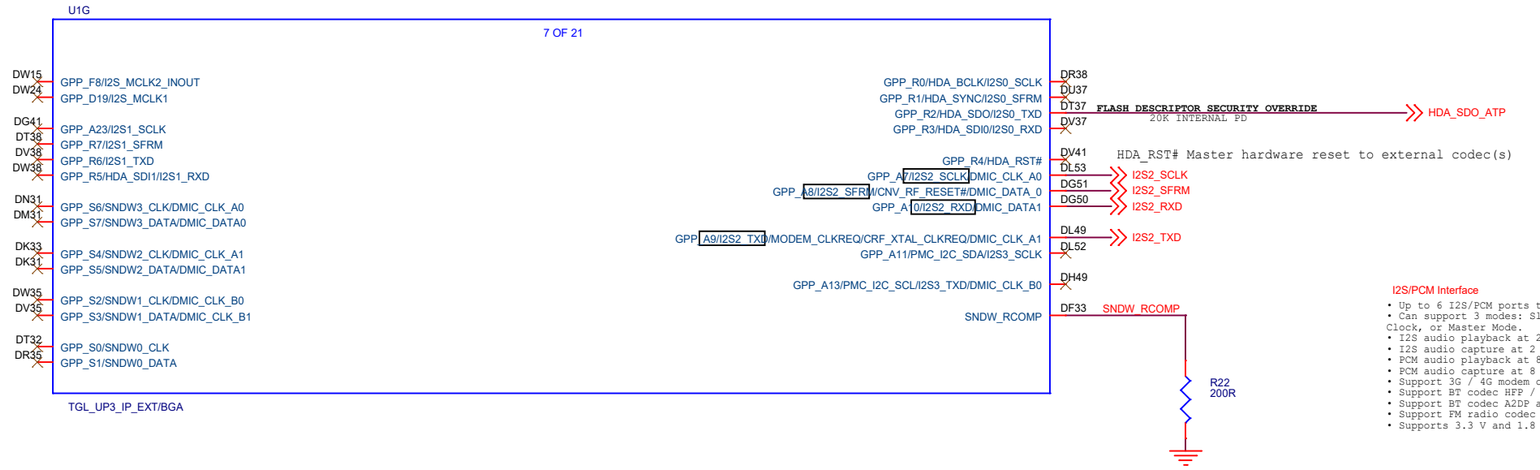
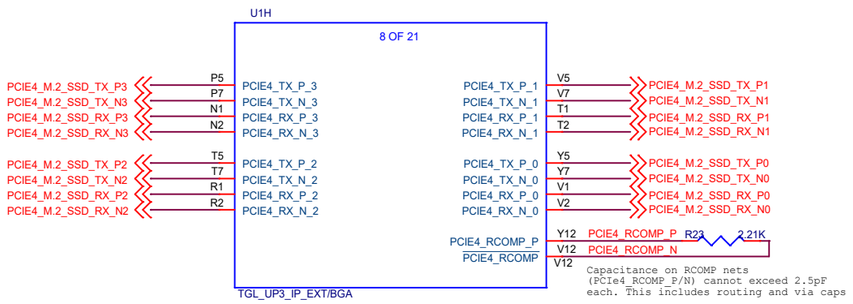


PCIE GEN 4 CAPS: p.158/270 in TL-SBC



12.2 PCIe4 Gen4 Interface Signals

Signal Name	Description	Dir	Buffer Type	Link Type	Availability
PCIE4_RCOMP_P PCIE4_RCOMP_N	Resistance Compensation for PEG channel	I	Analog	Diff	UP3/UP4/H Processor Lines
PCIE4_TX_P[3:0] PCIE4_TX_N[3:0]	PCIe Transmit Differential Pairs	O	PCIE	Diff	UP3/UP4/H Processor Lines
PCIE4_RX_P[3:0] PCIE4_RX_N[3:0]	PCIe Receive Differential Pairs	I	PCIE	Diff	UP3/UP4/H Processor Lines

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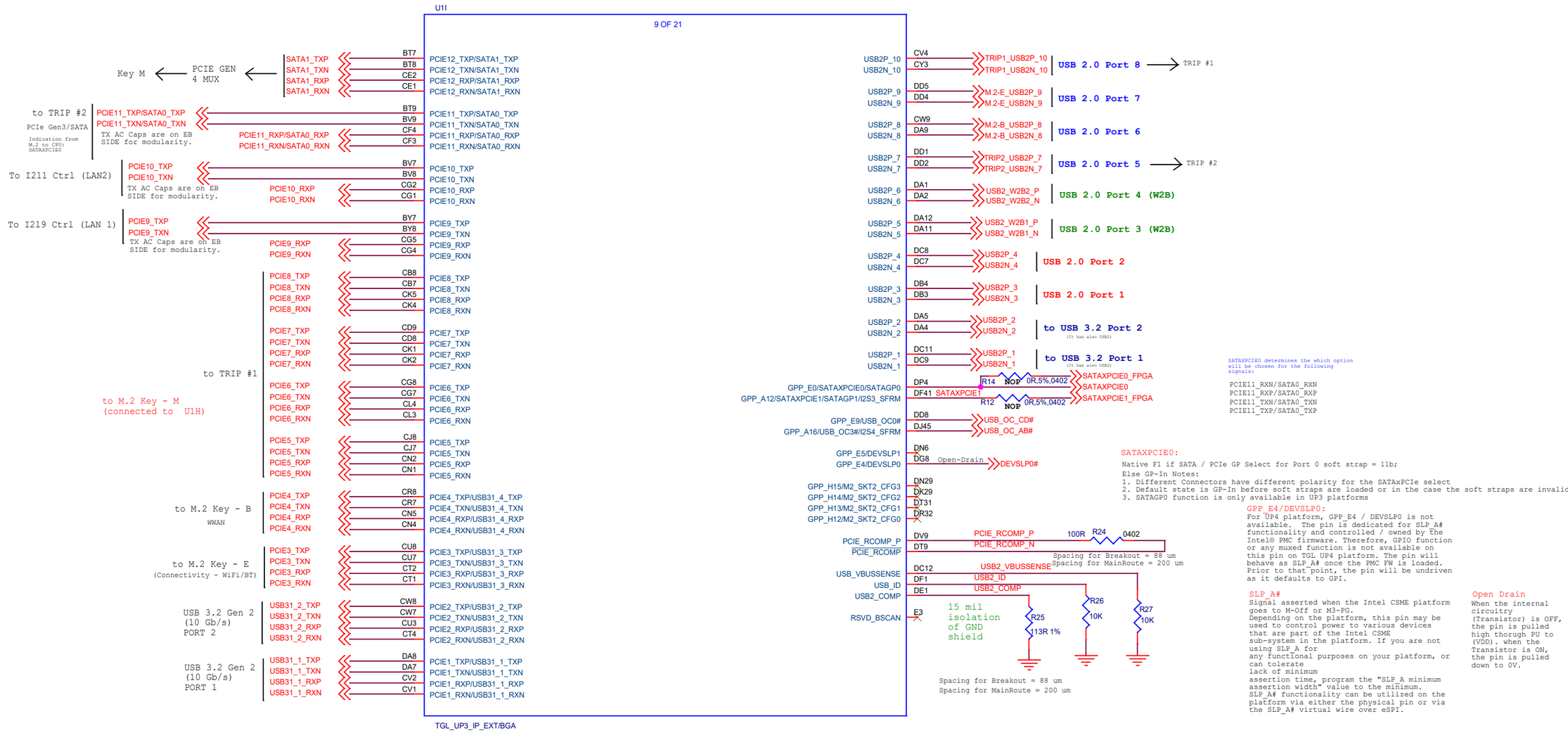

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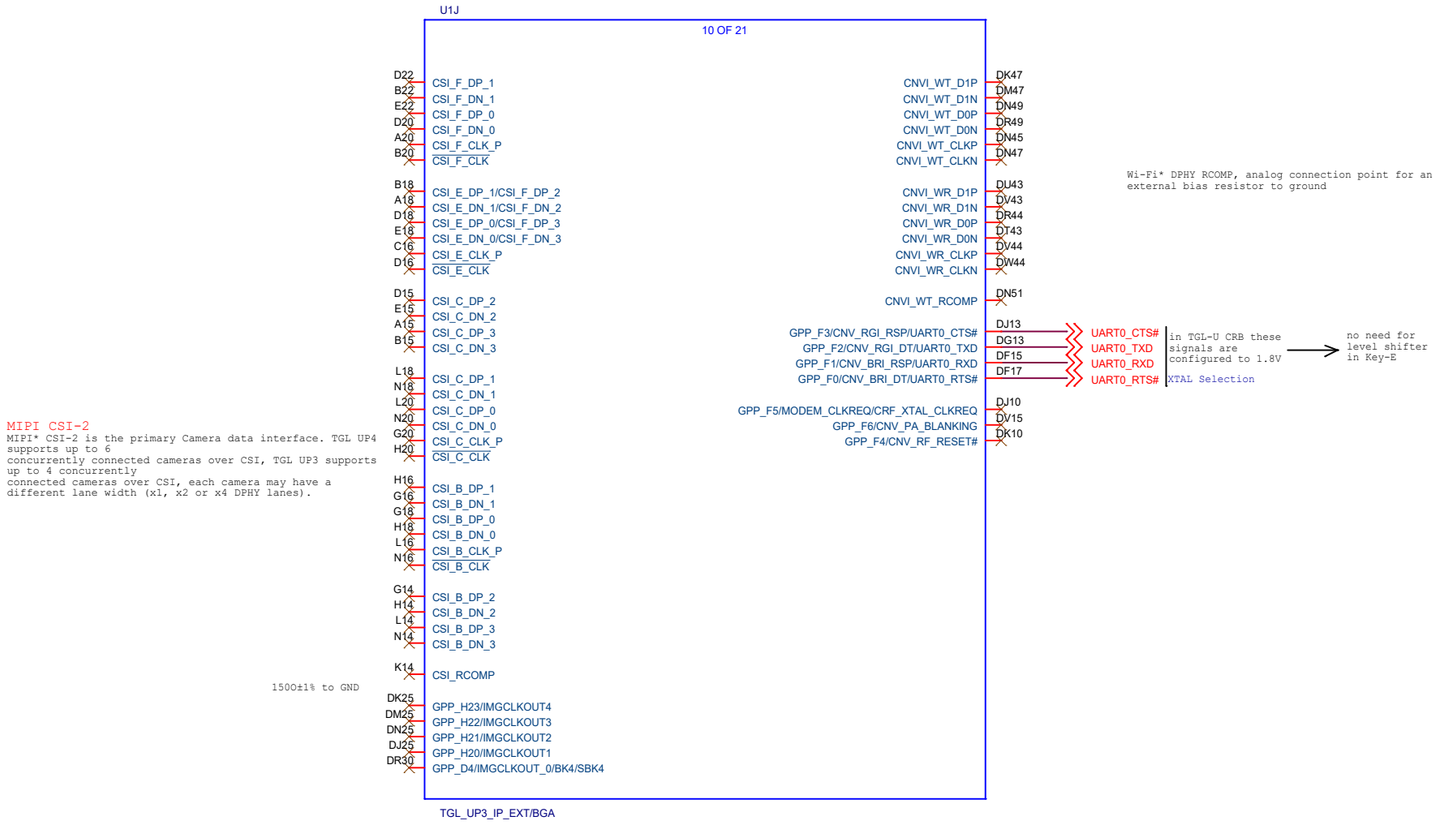

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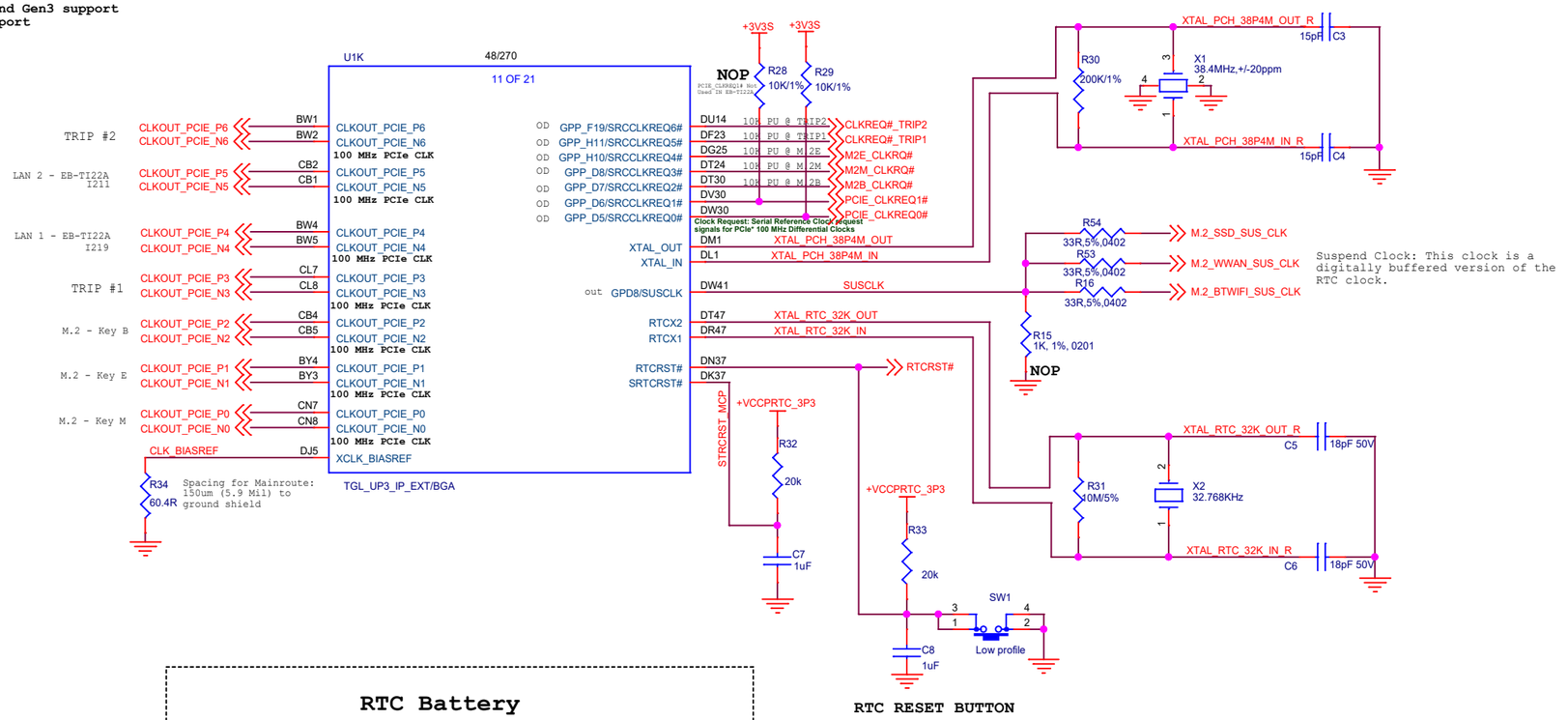
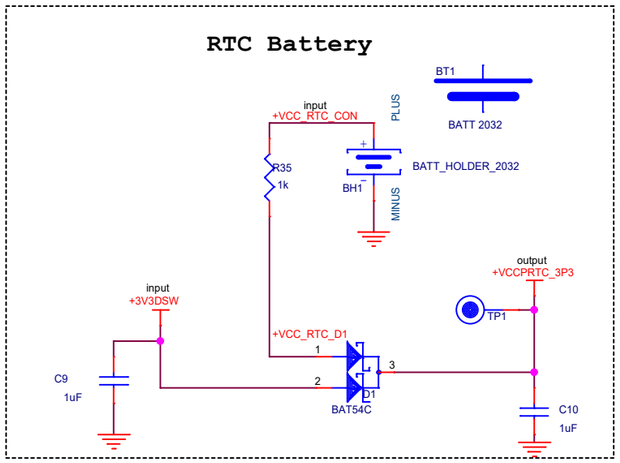
PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices

- **CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support**
- **CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support**



RTC RESET BUTTON

RTC Battery



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SLP_S0#
S0 Sleep Control. When PCH is idle and processor is in C10 state, this pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.

SLP_S5#
This signal is for power plane control. When asserted (low), it will shutoff power to all non-critical systems in S5 (Soft Off) states.

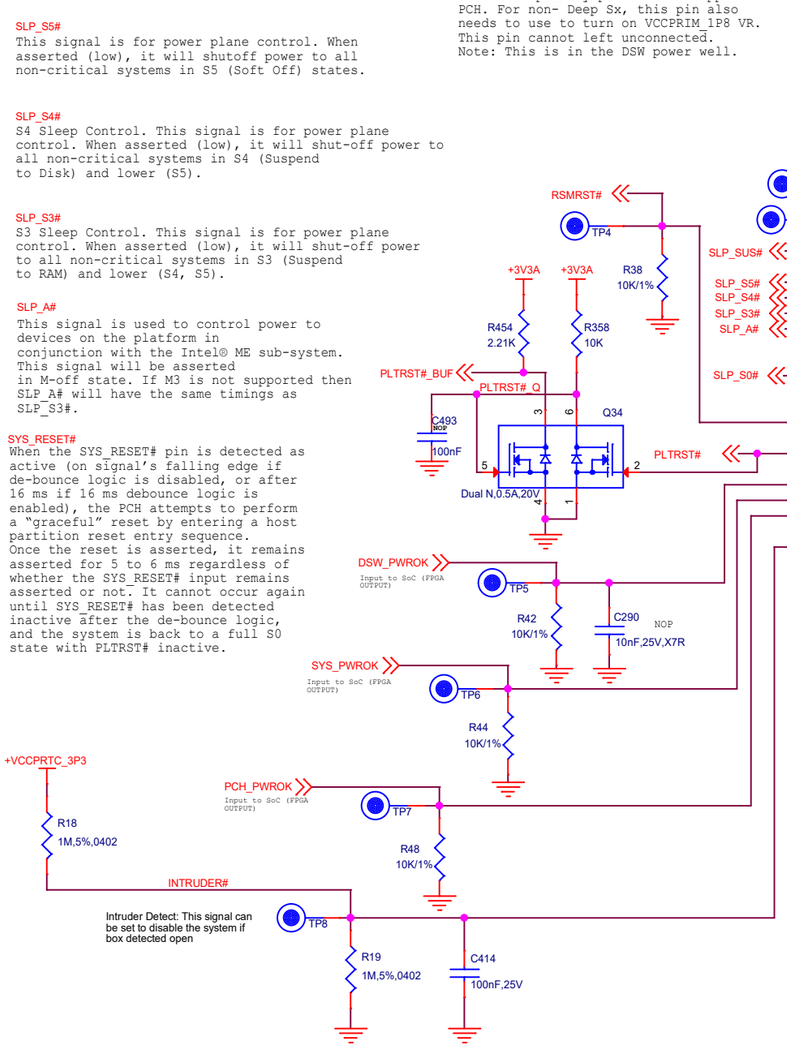
SLP_S4#
S4 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S4 (Suspend to Disk) and lower (S5).

SLP_S3#
S3 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S3 (Suspend to RAM) and lower (S4, S5).

SLP_A#
This signal is used to control power to devices on the platform in conjunction with the Intel® ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timings as SLP_S3#.

SYS_RESET#
When the SYS_RESET# pin is detected as active (on signal's falling edge if de-bounce logic is disabled, or after 16 ms if 16 ms debounce logic is enabled), the PCH attempts to perform a "graceful" reset by entering a host partition reset entry sequence. Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the SYS_RESET# input remains asserted or not. It cannot occur again until SYS_RESET# has been detected inactive after the de-bounce logic, and the system is back to a full S0 state with PLTRST# inactive.

SLP_SUS# (High = Exist from Deep Sx)
Deep Sx Indication: When asserted (driven low), this signal indicates PCH is in Deep Sx state where internal primary power is shut off for enhanced power saving. When de-asserted (driven high), this signal indicates exit from Deep Sx state and primary power can be applied to PCH. For non- Deep Sx, this pin also needs to use to turn on VCCPRIM_1P8 VR. This pin cannot left unconnected.
Note: This is in the DSW power well.



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SLP_SUS#
GPD10/SLP_S5#
GPD5/SLP_S4#
GPD4/SLP_S3#
GPD6/SLP_A#
GPD9/SPL_WLAN# out
GPP_B12/SLP_S0#
SLP_LAN#
RSMRST#
SYS_RESET#
GPP_B13/PLTRST#
DSW_PWROK
SYS_PWROK
PCH_PWROK
INTRUDER#
SPIVCCIOSEL

TGL_UP3_IP_EXT/BGA

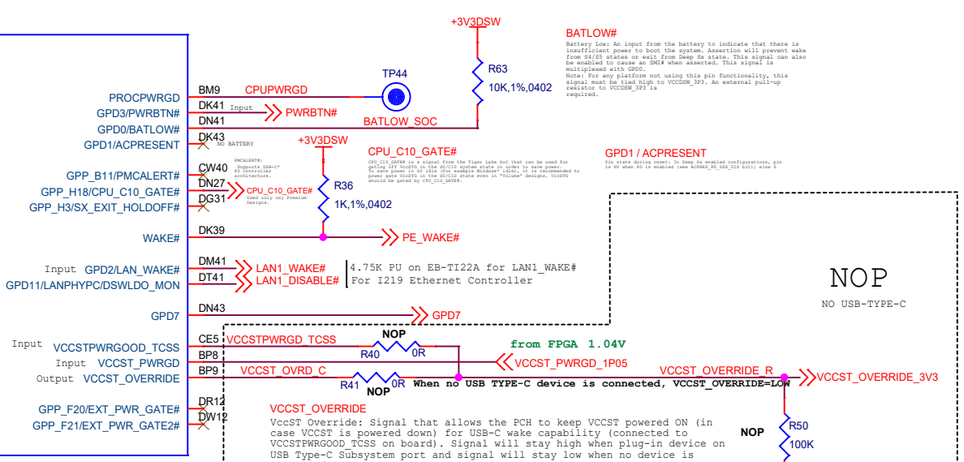
PCH Power OK: When asserted, PCH_PWROK is an indication to the PCH that all of its core power rails have been stable.
The platform may drive asynchronously. When PCH_PWROK is de-asserted, the PCH asserts PLTRST#. Note: PCH_PWROK must not glitch, even if RSMRST# is low.

SYS_PWROK
System Power OK: This generic power good input to the PCH is driven and utilized in a platform-specific manner. While PCH_PWROK always
indicates that the primary wells of the PCH are stable, SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset.

WAKE#
WAKE #: Can be used by the LAN PHY as a wake signal.

PCI Express* ports can wake the platform from S4, S5, or Deep Sx using the WAKE# pin. WAKE# is treated as a wake event, but does not cause any bits to go active in the GPE_STS register.

PCI Express* WAKE# pin is an Output in S0ix states hence this pin cannot be used to wake up the system during S0ix states.



BATLOW#
Battery Low: An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S4/S5 states or exit from Deep Sx state. This signal can also be enabled to cause an SMI# when asserted. This signal is multiplexed with GPIO.
Note: For any platform not using this pin functionality, this signal must be tied high to VCCDSW_3P3. An external pull-up resistor to VCCDSW_3P3 is required.

GPD1 / ACPRESENT

CPU_C10_GATE#

VCCST_OVERRIDE
VccST Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWRGOOD_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

NOP
NO USB-TYPE-C

When no USB TYPE-C device is connected, VCCST_OVERRIDE=LOW

VCCSTPWRGOOD_TCSS
VCCSTPWRGOOD_TCSS: The processor requires this input signal to be asserted when the type-c subsystem requires keeping VCCST supply on (VCCST_OVERRIDE), even when entering S3/ S4- S5 states.
This signal start as low and may change polarity only at the entry to S3/ S4- S5. If required to toggle, the signal level must always change before the de-assertion of
VCCST_PWRGD signal at the Sx entry flow.
This signal must have a valid level during S0 - S5 power states.
S3 state is available only on H SKU.

LAN_WAKE#
LAN WAKE: LAN Wake Indicator from the GbE PHY.
Note: LAN_WAKE# functionality is only supported with Intel PHY I219. Connection of a third party LAN device's wake signal to LAN_WAKE# is not supported.

SLP_A#
Signal asserted when the Intel CSME platform goes to M-Off or M3-PG.
Depending on the platform, this pin may be used to control power to various devices that are part of the Intel CSME sub-system in the platform. If you are not using SLP_A for any functional purposes on your platform, or can tolerate lack of minimum
assertion time, program the "SLP_A minimum assertion width" value to the minimum. SLP_A# functionality can be utilized on the platform via either the physical pin or via the SLP_A# virtual wire over eSPI.

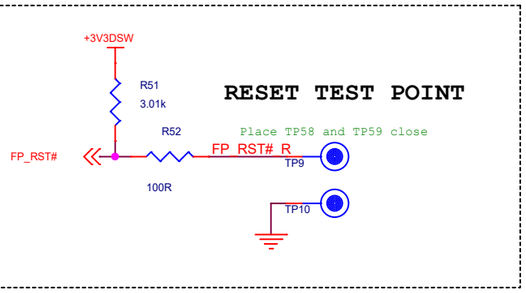
Sx_Exit_Holdoff#
When S4/S5 is entered and SLP_A# is asserted, Sx_Exit_Holdoff# can be asserted by a platform component to delay resume to S0. SLP_A# de-assertion is an indication of the intent to resume to S0 (power up), but this will be delayed so long as Sx_Exit_Holdoff# is asserted. Sx_Exit_Holdoff is ignored outside of an S4/S5 entry sequence with SLP_A# asserted. With the de-assertion of RSMRST# (either from G3->S0 or DeepSx->S0), this pin is a GPIO input and must be programmed by BIOS to operate as Sx_Exit_Holdoff. When SLP_A# is asserted (or it is de-asserted but Sx_Exit_Holdoff# is asserted), the PCH will not access SPI Flash. How a platform uses this signal is platform specific.

Wake up on LAN / SLP_LAN#
SLP_LAN# is used to indicate when power to the LAN PHY is needed. If Host Wake On LAN or Intel® ME Wake on LAN is enabled, the SLP_LAN# signal will remain high to keep power on to the LAN PHY. The Integrated LAN (VccLAN) rail does not need to be powered in Sx/M-Off state unless they are needed as indicated by the TGP-LP signals like SLP_S3# and SUSPWRDNACK.

LANPHYPC
LAN PHY Power Control: LANPHYPC should be connected to LAN_DISABLE_N on the PHY. PCH will drive LANPHYPC low to put the PHY into a low power state when functionality is not needed. Note: LANPHYPC can only be driven low if SLP_LAN# is de-asserted.

SLP_LAN#
SLP_LAN# is used to indicate when power to the LAN PHY is needed. If Host Wake On LAN or Intel® ME Wake on LAN is enabled, the SLP_LAN# signal will remain high to keep power on to the LAN PHY.
The Integrated LAN (VccLAN) rail does not need to be powered in Sx/M-Off state unless they are needed as indicated by the TGP-LP signals like SLP_S3# and SUSPWRDNACK.

LAN Sub-System Sleep Control: If the Gigabit Ethernet Controller is enabled, when SLP_LAN# is de-asserted (LOW) it indicates that the PHY device must be powered. When SLP_LAN# is asserted, power can be shut off to the PHY device.
Note: If Gigabit Ethernet Controller is statically disabled via
BIOS, SLP_LAN# will be driven low.



PLTRST# PLTRST# = High (De-Asserted)

Reset Behavior
When a reset is triggered, the PCH will send a warning message to the processor to allow the processor to attempt to complete any outstanding memory cycles and put memory into a safe state before the platform is reset. When the processor is ready, it
will send an acknowledge message to the PCH. Once the message is received the PCH asserts PLTRST#.
The PCH does not require an acknowledge message from the processor to trigger PLTRST#. A global reset will occur after four seconds if an acknowledge from the
processor is not received.
When the PCH causes a reset by asserting PLTRST#, its output signals will go to their reset states.
A reset in which the host platform is reset and PLTRST# is asserted is called a Host Reset or Host Partition Reset. Depending on the trigger a host reset may also result in power cycling, refer to the below table for details. If a host reset is triggered and the PCH times out before receiving an acknowledge message from the processor a Global Reset with power-cycle will occur.
A reset in which the host and Intel® CSME partitions of the platform are reset is called a Global Reset. During a Global Reset, all PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. Intel® CSME and Host power back up after the power-cycle period.
Straight to S5 is another reset type where all power wells that are controlled by the SLP_S3#, SLP_S4#, and SLP_A# pins, as well as SLP_S5# and SLP_LAN# (if pins are not configured as GPIOs), are turned off. All PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. The host stays there until a valid wake event occurs.

The PCH has an input signal, INTRUDER#, that can be attached to a switch that is
activated by the system's case being open. This input has a two RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD_DET bit in the TCTL2 register. The INTRD_SEL bits in the TCTL2 register can enable the PCH to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP_EN bit.

The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD_DET bit. This allows the signal to be used as a GPI if the intruder function is not required.
If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET bit will go to a 0 when INTRUDER# input signal goes
inactive.

RTC-Well Input Strap Requirements
All RTC-well inputs (RSMRST#, RTCRST#, SRTCRST#, INTRUDER#, PCH_PWROK, DSW_PWROK) must be either pulled up to VccRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in Figure 63 on page 126 meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PCH_PWROK and DSW_PWROK input signal should also be configured with an external weak pull-down.

SLP_WLAN# (GPD9)
The PCH controls the voltage rails into the external wireless LAN PHY using the SLP_WLAN# pin.
• The wireless LAN PHY is always powered when the Host is running.
– SLP_WLAN#='1' whenever SLP_S3#='1'.
• If Wake on Wireless LAN (WoWLAN) is required from S3/S4/S5 states, the host BIOS must set HOST_WLAN_PP_EN.
• If WoWLAN is required from Deep Sx, the host BIOS must set DSX_WLAN_PP_EN.
• If Intel® CSME has access to the Wireless LAN device:

– The Wireless LAN device must always be powered as long as Intel® CSME is powered. SLP_WLAN#='1' whenever SLP_A#='1'.
– If Wake on Wireless LAN (WoWLAN) is required from M-Off state, Intel® CSME will configure SLP_WLAN#='1' in Sx/M-Off.
Intel® CSME configuration of SLP_WLAN# in Sx/M-Off is dependent on Intel® CSME power policy configuration.
When the Wireless LAN device is an integrated connectivity device (CNVi) the power to the CNVi external RF chip (CRF) must be always on. In this case the SLP_WLAN# shall not control the CRF 3.3 V power rail.

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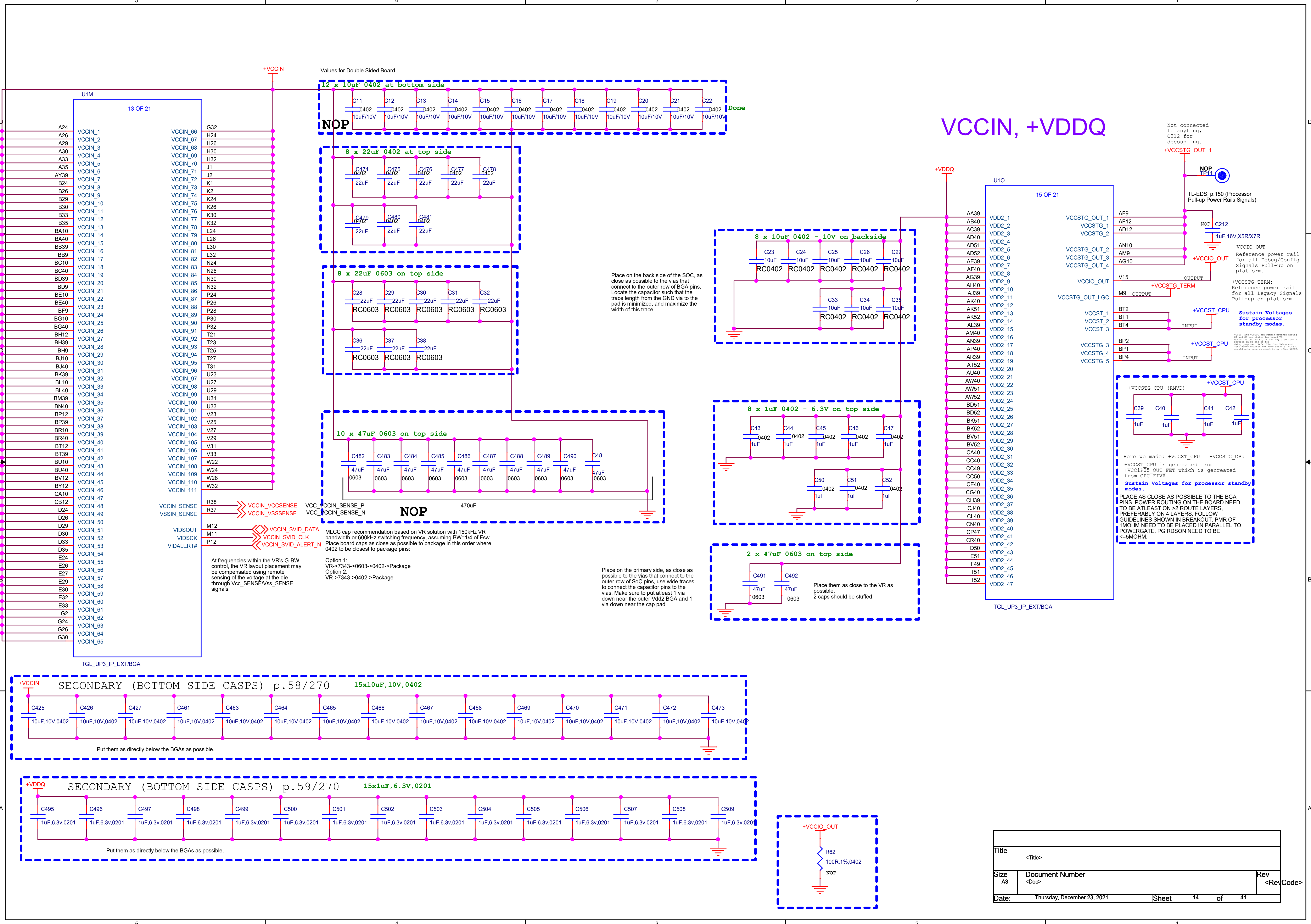

VCCIN, +VDDQ
+VCCIN
Values for Double Sided Board
U1M
13 OF 21
TGL_UP3_IP_EXT/BGA
12 x 10uF 0402 at bottom side
NOP
Done
8 x 22uF 0402 at top side
8 x 22uF 0603 on top side
10 x 47uF 0603 on top side
NOP
470uF
VCCIN_SENSE
VSSIN_SENSE
R38
R37
VCCIN_VCCSENSE
VCCIN_VSSSENSE
VCC_VCCIN_SENSE_P
VCC_VCCIN_SENSE_N
VIDSOUT
VIDSCK
VIDALERT#
VCCIN_SVID_DATA
VCCIN_SVID_CLK
VCCIN_SVID_ALERT_N
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth or 600kHz switching frequency, assuming BW=1/4 of Fsw. Place board caps as close as possible to package in this order where 0402 to be closest to package pins:
Option 1: VR->7343->0603->0402->Package
Option 2: VR->7343->0402->Package
At frequencies within the VR's G-BW control, the VR layout placement may be compensated using remote sensing of the voltage at the die through Vcc_SENSE/Vss_SENSE signals.
Place on the back side of the SOC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
Place on the primary side, as close as possible to the vias that connect to the outer row of SoC pins, use wide traces to connect the capacitor pins to the vias. Make sure to put atleast 1 via down near the outer Vdd2 BGA and 1 via down near the cap pad
+VDDQ
U1O
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TGL_UP3_IP_EXT/BGA
8 x 10uF 0402 - 10V on backside
8 x 1uF 0402 - 6.3V on top side
2 x 47uF 0603 on top side
Place them as close to the VR as possible.
2 caps should be stuffed.
Not connected to anyting, C212 for decoupling.
+VCCSTG_OUT_1
NOP TP11
TL-EDS: p.150 (Processor Pull-up Power Rails Signals)
VCCSTG_OUT_1
VCCSTG_1
VCCSTG_2
VCCSTG_OUT_2
VCCSTG_OUT_3
VCCSTG_OUT_4
VCCIO_OUT
VCCSTG_OUT_LGC
VCCST_1
VCCST_2
VCCST_3
VCCSTG_3
VCCSTG_4
VCCSTG_5
C212
1uF,16V,X5R/X7R
+VCCIO_OUT
+VCCIO_OUT Reference power rail for all Debug/Config Signals Pull-up on platform.
+VCCSTG_TERM
+VCCSTG_TERM: Reference power rail for all Legacy Signals Pull-up on platform
+VCCST_CPU
Sustain Voltages for processor standby modes.
+VCCSTG_CPU (RMVD)
Here we made: +VCCST_CPU = +VCCSTG_CPU
+VCCST_CPU is generated from +VCC1P05_OUT_FET which is genreated from CPU FIVR
Sustain Voltages for processor standby modes.
PLACE AS CLOSE AS POSSIBLE TO THE BGA PINS. POWER ROUTING ON THE BOARD NEED TO BE ATLEAST ON >2 ROUTE LAYERS, PREFERABLY ON 4 LAYERS. FOLLOW GUIDELINES SHOWN IN BREAKOUT. PMR OF 1MOHM NEED TO BE PLACED IN PARALLEL TO POWERGATE. PG RDSON NEED TO BE <=5MOHM.
SECONDARY (BOTTOM SIDE CASPS) p.58/270
15x10uF,10V,0402
Put them as directly below the BGAs as possible.
SECONDARY (BOTTOM SIDE CASPS) p.59/270
15x1uF,6.3V,0201
Put them as directly below the BGAs as possible.
+VCCIO_OUT
R62
100R,1%,0402
NOP
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VCCIN_AUX, VCCPRIM

From External DC\DC to SoC

U1N

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TGL_UP3_IP_EXT/BGA

in TL-SBC: +VCCPDSW_3P3 is generated from +V3.3A_DSW (p. 225/270)

+3V3A — R77 0R,5%,0402 (NOP) — +VCCPGPPR_3P3_1P8

+V1.8A — R6 0R,5%,0402 — +VCCPRIM_1P8

R64 0R,5%,0402 — 0.68uH, 20%, 150mA, 0.8ohm (NOP L10) — +VCCA_CLKLDO_1P8

+VCCPGPPR_3P3_1P8 — R78 0R,5%,0402

The inductor and capacitor form an LC filter to filter out the switching noise either from the power supply itself or from the other components connected to the power supply. The resistor dampens the LC filter to prevent unwanted resonance. LC filters like this often use a high ESR tantalum capacitor instead of adding a separate resistor.

LC Filter: LOW PASS

R66 0R,5%,0402

RC_CLKLDO — C211 47uF,6.3V,X5R

R66: Option 1: stuff with 0 ohm if the inductor is not stuffed. Option 2: stuff 100 mohm if the inductor stuffed

+VCCIN_AUX

AB12	VCCIN_AUX_1
AC10	VCCIN_AUX_2
AE10	VCCIN_AUX_3
AK2	VCCIN_AUX_4
AR10	VCCIN_AUX_5
AT12	VCCIN_AUX_6
AU10	VCCIN_AUX_7
AW10	VCCIN_AUX_8
BV1	VCCIN_AUX_9
BV39	VCCIN_AUX_10
BW40	VCCIN_AUX_11
BY39	VCCIN_AUX_12
CC1	VCCIN_AUX_13
CD12	VCCIN_AUX_14
CF10	VCCIN_AUX_15
CG12	VCCIN_AUX_16
CH10	VCCIN_AUX_17
CJ1	VCCIN_AUX_18
CJ12	VCCIN_AUX_19
CK10	VCCIN_AUX_20
CL12	VCCIN_AUX_21
CM10	VCCIN_AUX_22
CP1	VCCIN_AUX_23
CP10	VCCIN_AUX_24
CR12	VCCIN_AUX_25
CT10	VCCIN_AUX_26
CU12	VCCIN_AUX_27
CY1	VCCIN_AUX_28
AK1	VCCIN_AUX_29

TP52 TP51 TP50 TP49

VCCIN_AUX_VSSSENSE	AV9	VCCIN_AUX_VSSSENSE
VCCIN_AUX_VCCSENSE	AT9	VCCIN_AUX_VCCSENSE
VCC_VNNEXT_1P05_1	DD17	VCC_VNNEXT_1P05_1
VCC_VNNEXT_1P05_2	DD18	VCC_VNNEXT_1P05_2
VCC_V1P05EXT_1P05_1	DA15	VCC_V1P05EXT_1P05_1
VCC_V1P05EXT_1P05_2	DA17	VCC_V1P05EXT_1P05_2
VRALERT_MCP# — 0R R74 — VRALERT_MCP#_C	DB39	GPP_B2/VRALERT#
	DV12	GPP_F22/VNN_CTRL
	DT12	GPP_F23/V1P05_CTRL
VCCIN_AUX_CORE_VID0_R — 0R R75 — GPPC_B0_CORE_VID_0	DB37	GPP_B0/CORE_VID0
VCCIN_AUX_CORE_VID1_R — 0R R76 — GPPC_B1_CORE_VID_1	DB38	GPP_B1/CORE_VID1

VRALERT#: ICC Max. throttling indicator from the PCH voltage regulators. VRALERT# pin allows the VR to force PCH throttling to prevent an over current shutdown. PMC based on the VRALERT# and messages from the processor. The messages from the processor allows the processor to constrain the PCH to a particular power budget.

1.8 V Primary Well. +VCCPRIM_1P8 (+V1.8A)

VCCPRIM_1P8_1	CY18
VCCPRIM_1P8_2	CY20
VCCPRIM_1P8_3	CY24
VCCPRIM_1P8_4	CY26
VCCPRIM_1P8_5	DA18
VCCPRIM_1P8_6	DA20
VCCPRIM_1P8_7	DA22
VCCPRIM_1P8_8	DA24
VCCPRIM_1P8_9	DA26
VCCPRIM_1P8_10	DC18
VCCPRIM_1P8_11	DC20
VCCPRIM_1P8_12	DC22
VCCPRIM_1P8_13	DC24
VCCPRIM_1P8_14	DC26
VCCPRIM_1P8_15	DD20
VCCPRIM_1P8_16	DD22
VCCPRIM_1P8_17	DV22

+VCCPRIM_3P3 3.3 V Primary Well. +3V3A

VCCPRIM_3P3_1	DA35
VCCPRIM_3P3_2	DC28
VCCPRIM_3P3_3	DC30
VCCPRIM_3P3_4	DD30

RTC de-coupling capacitor only. This rail should not be driven by any motherboard power rails.

+VCCRTCEXT

DCPRTC	DV34
VCCLDOSTD_0P85	DV46

+VCCLDOSTD_OUT_0P85

This rail is generated internally and needs to be routed out to the motherboard for decoupling purposes.

Not Connected to any target except decoupling capacitor: C105

+VCCA_CLKLDO_1P8

VCCA_CLKLDO_1P8_1	DV16	INPUT
VCCA_CLKLDO_1P8_2	DC15	

1.24 V for CNVi logic. This rail is generated internally with an LDO and needs to be routed to the motherboard for decoupling purpose only. This rail should not be driven by any motherboard power rails.

Not Connected to any target except decoupling capacitor: C107

+VCCDPHY_1P24_SOC

VCCDPHY_1P24	DV28	OUTPUT
VCCDSW_1P05	DD38	

Deep Sx Well: 1.05 V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic.

Not Connected to any target except decoupling capacitor: C104

+VCCDSW_1P05_SOC

+VCC1P05_OUT_FET

1.05 V Primary Well: for CNVi and other internal I/O blocks.

(Make small plane not connected to anything except these 3 balls)

+VCC1P05_OUT_PCH

merge pins together

VCC1P05_OUT_FET_1	BR3	
VCC1P05_OUT_FET_2	BR4	
VCC1P05_OUT_FET_3	BT5	

+VCCPRTC_3P3

Deep Sx Well +3V3A

VCCPRIM1P05_OUT_PCH_1	DA31	
VCCPRIM1P05_OUT_PCH_2	DC33	
VCCPRIM1P05_OUT_PCH_3	DC31	

+VCCPGPPR_3P3_1P8: Audio Power 3.3 V or 1.8 V. If powered at 3.3 V, the 3.3 V supply can come from the VCCPRIM_3P3 supply. If powered at 1.8 V, the 1.8 V supply can come from the VCCPRIM_1P8 supply.

+VCCPRIM_3P3 3.3 V Primary Well. +3V3A

p234/270 TL-SBC

VCCRTC	DC35	
VCCDSW_3P3	DD37	3.3-V supply for Deep Sx wells. (input)
VCCPGPPR	DA28	

VCCPRIM_3P3_5	CY31	PCH I/O and Misc 3.3V Rail(Primary Well)
VCCPRIM_3P3_6	CY33	
VCCPRIM_1P8_18	CV39	PCH I/O and Misc 1.8V Rail(Primary Well)
RSVD_1	AP12	

1.8 V Primary Well. +VCCPRIM_1P8

+VCCIN_AUX — 15 x 10uF 0402 on topside

C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 — 0402 10uF/10V

+VCCIN_AUX — 12 x 22uF 0603 on topside

C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 — 22uF RC0603

+VCCIN_AUX — 3 x 47uF 0805 on topside

C510 C511 C512 — 0805 47uF ,6.3V

Use 2.5V rating caps.
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth, or 600kHz switching frequency assuming BW= ¼ of Fsw.
Place board caps as close as possible to package in this order where 0402 to be the closest to package pins: VR ?7343? 0805? 0603-> 0402 ? package.
*a DCLL of 3.3mohm is required and bulk capacitors must be used.

Pair board caps with power/ground PTHs.
Align caps along current flow path from VR to package pins.

+VCCIN_AUX — 10 x 10uF 0402 on bottom

Done

C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82 — 0402 10uF/10V

Use 2.5V rating caps.
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth, or 600kHz switching frequency assuming BW= ¼ of Fsw.

VCCA_CLKLDO_1P8 is supplying to PCH ClocK. (analog supply)

Place board caps as close as possible to package

+VCCPRTC_3P3 — C95 1uF, C96 100nF

+VCCPDSW_3P3 / +3V3A — C97 NOP 1uF,16V,X5R/X7R

+VCCPRIM_3P3 / +3V3A — C98 NOP 1uF, C99 NOP 100nF

+VCCPRIM_1P8 — C100 NOP 1uF

NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA

+VCCDSW_1P05_SOC — TP13 — C104 1uF,6.3V,X5R/X7R

+VCCLDOSTD_OUT_0P85 — TP14 — C105 2.2uF,10V,X5R

+VCCRTCEXT — TP12 — C106 100nF,25V,X5R/X7R

+VCCDPHY_1P24_SOC — C107 4.7uF,10V,20%

Table 214.	Differences between Power Maps

Volume	Premium
VccSTG gated by SLP_S3#	VccSTG gated by {CPU_C10_GATE#}
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC _V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load
Various system devices share load switches	Various system devices have their own independent load switches

Note:

1. VCC_VNNEXT_1P05 is also known as VNN BYP
2. VCC _V1P05EXT_1P05 is also known as VP105 BYP
3. Other changes may be present. Refer to the Power Map for details.

The VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two optional dedicated voltage regulators that save platform power during low power states.

Trade-offs - Volume vs. Premium Power Maps:

Power maps are broken into two tiers: Volume and Premium. Volume focuses on cost savings with the fewest VRs and Premium focuses on the smallest solution size with the lowest power consumption. For a design focused on S0ix or Modern Standby* power, the Premium power map is recommended. The designer may choose to implement a hybrid between Volume and Premium as long as guidelines are followed.

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+3V3DSW/+3V3A/+3V3S

3.3V , 13A

U3 MAX8792

VDD, VCC, PGOOD, EN, SKIP#, REF, REFIN, GND_PAD, TON, BST, DH, LX, DL, FB, ILIM

+5V_LDO <= 20mA

C108 1uF

C118 1uF

C119 NOP 1uF

R80 10K

V33_VCC

V33DSW_OK

V33DSW_EN

V33_SKIP#

R88 0R NOP

R89 0R NOP

R90 0R NOP

2v V33_REF

C132 10nF,25V

J1 Jumper 1 2 Short

AGND_V33

f = 490kHz

+12V_MAIN

V33_TON

R79 200K

V33_BOOT

C113 100nF

V33_DH

Q3 FDMS7682

C114 10uF,16V RC0603

C115 10uF,16V RC0603

C116 47uF,16V C1210H2_5

C117 47uF,16V C1210H2_5

V33_LX

L1 2.2uH,14A ,18mOhm

+3V3DSW

TP17

C122 100uF C1206

C123 100uF C1206

C124 100uF C1206

C125 100uF C1206

Q8 FDMS7660

V33_DL

R91 6.49K

C126 100uF C1206

C127 NOP 100uF C1206

C128 NOP 100uF C1206

V33_FB

2v V33_REF

I(MAX)=0.05*V(ILIM)/Rds(on)

R92 15k

C133 100nF NOP

R93 10k

V33_ILIM

0.8V (16A max)

R96 10K

AGND_V33

+3V3A , 3A

NDS335N,3A

Q1 H=1.15mm

+12V_MAIN

R81 10k

+3V3DSW

R85 10k

V33A_GATE

Q4 NDS335N,3A

C120 220nF

Q5 NDS335N,3A

V33A_DIS

R83 100R

TP15 +3V3A

C109 22uF,6.3v C0805

C110 100uF C1206

V33A_EN#

NOP R87 10k

V33A_EN# = LOW --> 3V3A High
V33A_EN# = High--> 3V3A LOW

p234/270 TL-SBC

+3V3S , 10A

FDMS7682,15A

Q2 H=1.12mm

+12V_MAIN

R82 10k

+3V3DSW

V33S_GATE

R86 10k

Q6 NDS335N,3A

C121 220nF

Q7 NDS335N,3A

R84 100R

V33S_DIS

V33S_EN#

TP16 +3V3S

C111 22uF,6.3v C0805

C112 100uF C1206

V33S_EN# = HIGH --> 3V3S LOW
V33S_EN# = LOW --> 3V3S HIGH

3.3V for LAN

Q9 NDS335N,3A

+12V_MAIN

R94 10k

V33LAN_GATE

C134 10nF,25V

R95 100R

V33LAN_DIS

Q10 NDS335N,3A

Q11 NDS335N,3A

R97 10k

+3V3A

V33LAN_GATE_A

Q12 NDS335N,3A

SLP_LAN#

NOP C155 220nF

TP20 +3V3LAN

C129 47uF C0805

C130 47uF C0805

C131 100uF C1206

SLP_LAN# = HIGH --> +3V3LAN = HIGH (SYSTEM NOT ON SLEEP)
SLP_LAN# = LOW--> +3V3LAN = LOW
TensorI20 had no PHY on any TEL. so this circuit wasn't used.
it was used in Airtop3.

the larger VGS the less Rds(on) Reistance for the same current

+3V3A

C142 220nF C143 220nF C137 220nF C138 220nF C144 220nF

C150 220nF C151 220nF C152 220nF

+5V_LDO, 500mA

+12V_MAIN

LT3065 U4

VIN, VIN, VOUT, VOUT, PWRGD, SHD#, IMAX, ADJ, GND, GND, REF/BP

1uF,16V C156 RC0402

TP21 +5V_LDO

20K R98

C157 2.2uF

C158 2.2uF

0.6V V5LDO_FB

V5LDO_SS

C159 10nF,25V

R99 2.74K

3.3V for WLAN

+3V3DSW

Q39 NDS335N,3A

+12V_MAIN

R352 10k

V3.3A_WLAN_GATE

C378 10nF,25V

R353 100R

V3.3A_WLAN_DIS

+3V3A

Q38 NDS335N,3A

R354 10k

Q40 NDS335N,3A

V3.3A_WLAN_GATE_A

+3V3A

R356 100K 1%,0201

SLP_WLAN#

NOP R409 0R 5% 0201

FPGA_SLP_WLAN#

NOP R410 0R 5% 0201

Q41 NDS335N,3A

NOP C513 220nF

TP35 +V3.3A_WLAN

C377 47uF C0805

C376 47uF C0805

C375 100uF C1206

SLP_WLAN# = HIGH --> +3V3_WLAN = HIGH (SYSTEM NOT ON SLEEP)
SLP_WLAN# = LOW--> +3V3_WLAN = LOW
TensorI20 had no PHY on any TEL. so this circuit wasn't used.
it was used in Airtop3.

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Size A3	Document Number <Doc>	Rev <RevCode>
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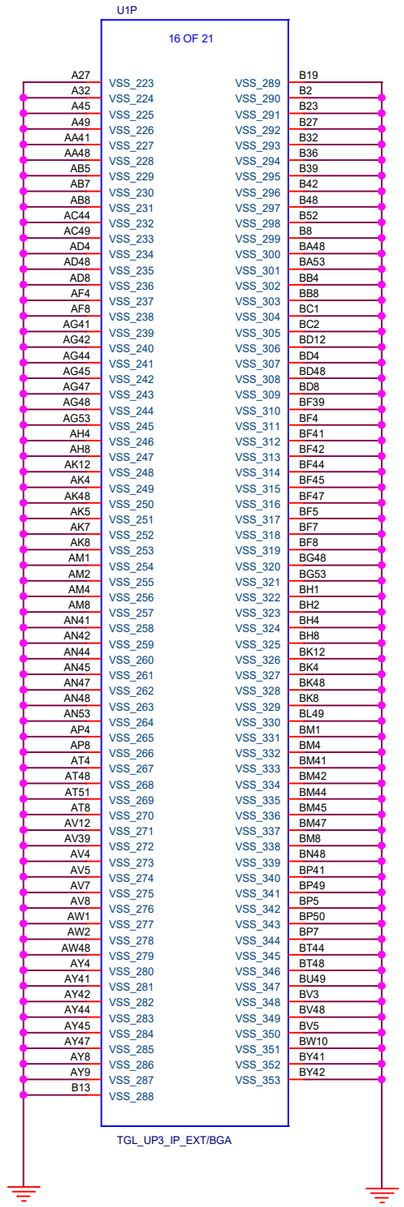

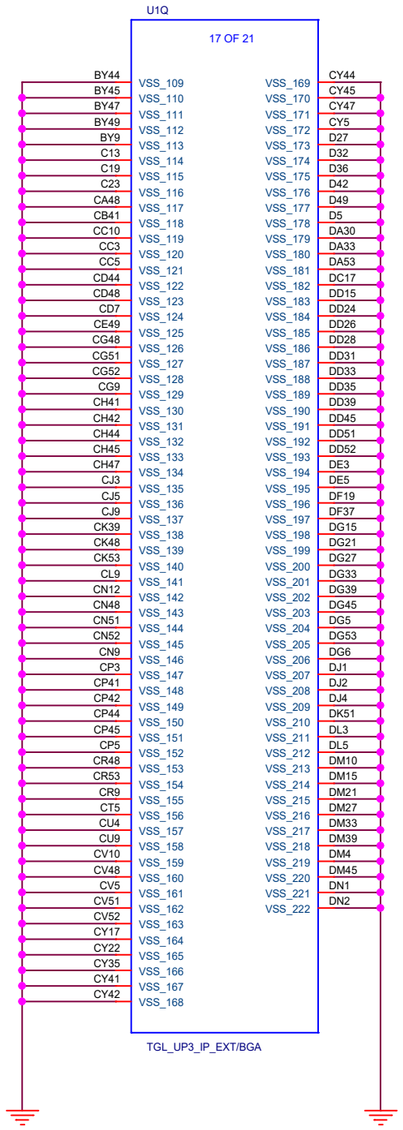

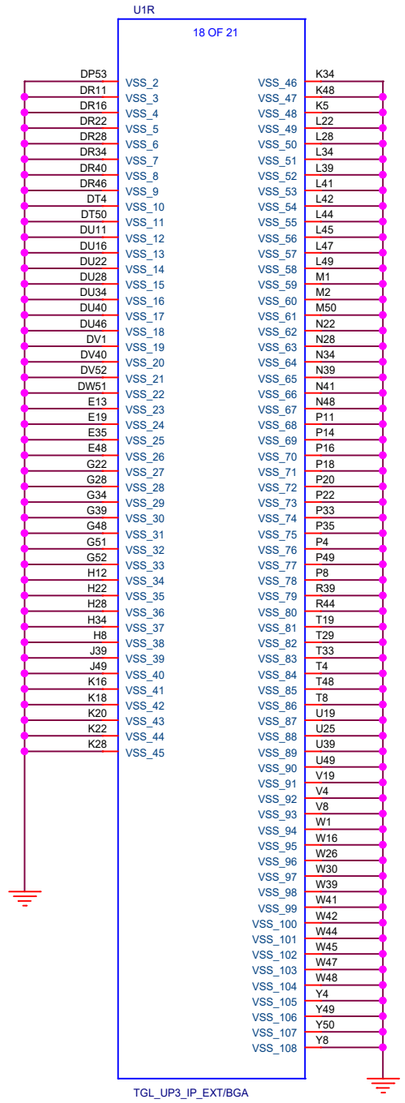

Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
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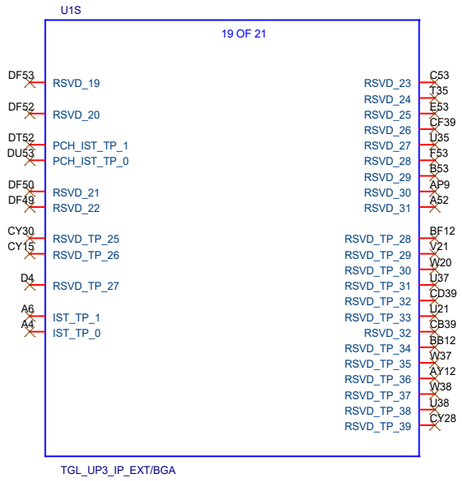

Title <Title>		
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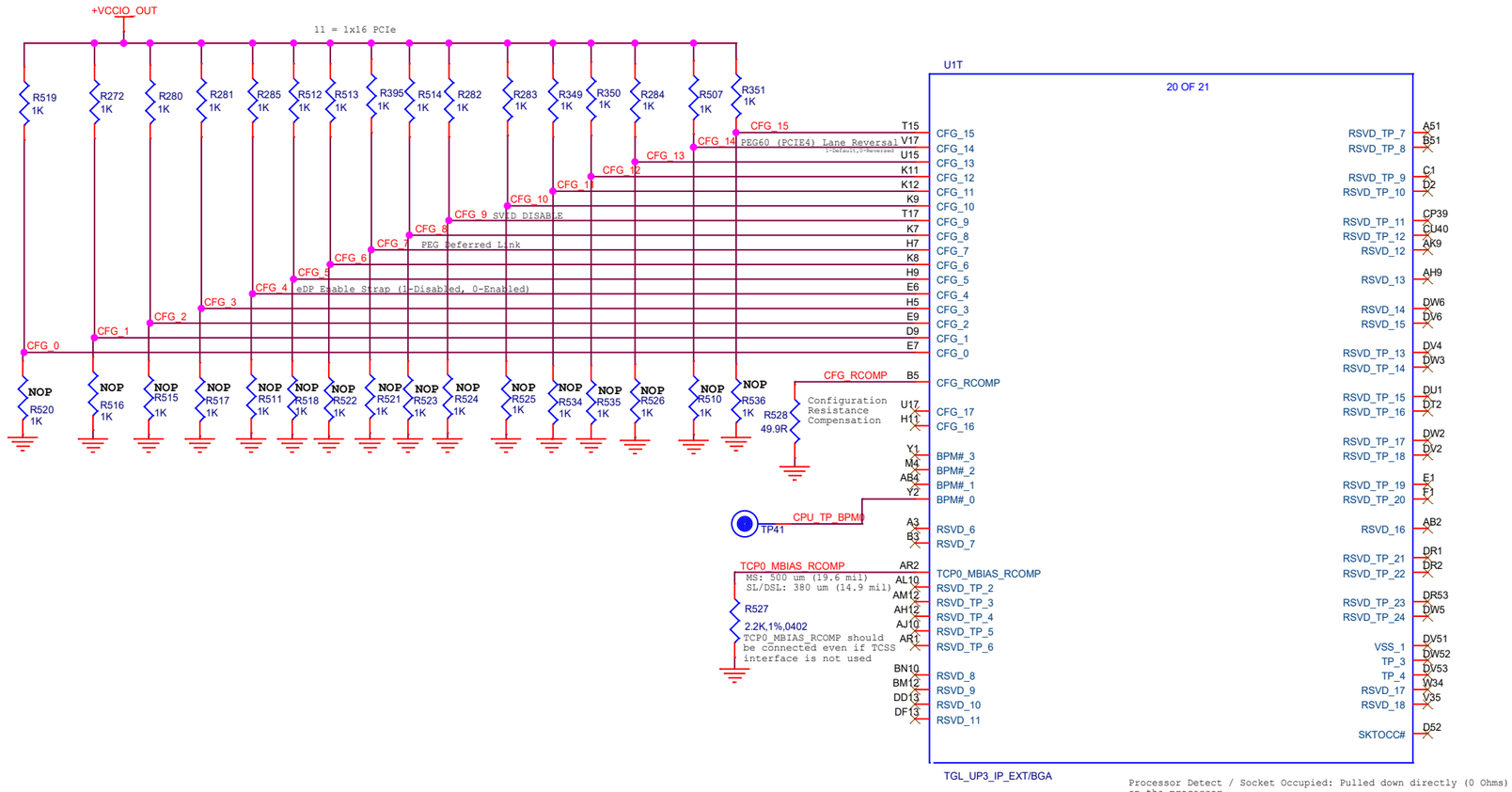
CFG[17:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[3], CFG[0]**: Reserved configuration lane. • **CFG[2]: TGL UP4/UP3** Reserved • **CFG[2]: H** PCI Express* Static x16 Lanes Numbering Reversal. — 1 - (Default) Normal — 0 - Reversed • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]: TGL UP4/UP3** Reserved • **CFG[6:5]: H** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[13:7]:** Reserved configuration lanes. • **CFG[14]**: PEG60 (PCIE4) Lane Reversal: — 1 - (Default) Normal — 0 - Reversed • **CFG[17:15]:** Reserved configuration lanes.	I	GTL	SE	UP3/UP4/H Processor Lines



BPM#[3:0]
Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM#[3:0]	Pull Up/Pull Down	VCC_{IO}_OUT	16-60 Ω
PROC_PREQ#	Pull Up	VCC_{STG}	3 KΩ
PROC_TDI	Pull Up	VCC_{STG}	3 KΩ
PROC_TMS	Pull Up	VCC_{STG}	3 KΩ
PROC_TRST#	Pull Down	VCC_{STG}	3 KΩ
PROC_TCK	Pull Down	VCC_{STG}	3 KΩ
CFG[17:0]	Pull Up	VCC_{IO}_OUT	3 KΩ

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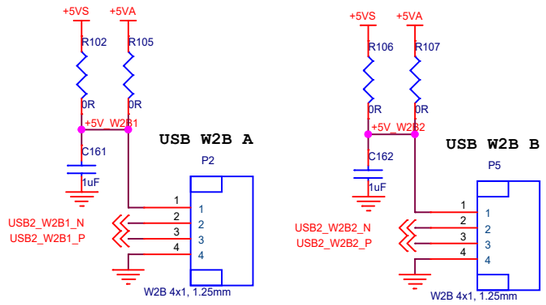
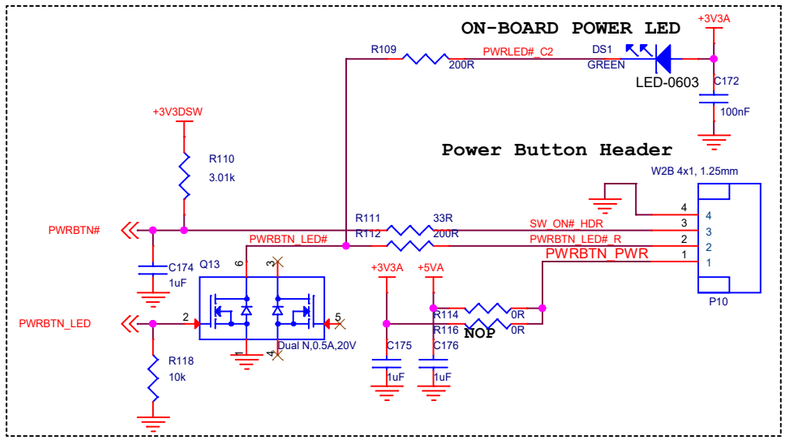
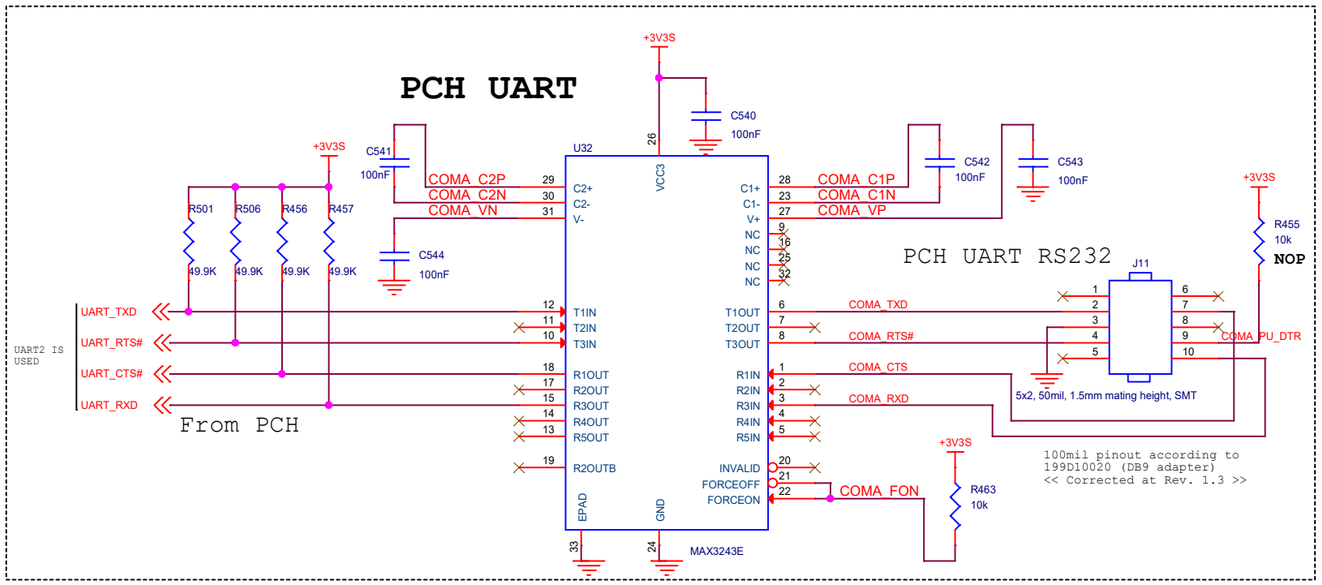
Headers



audio **Extension headers**

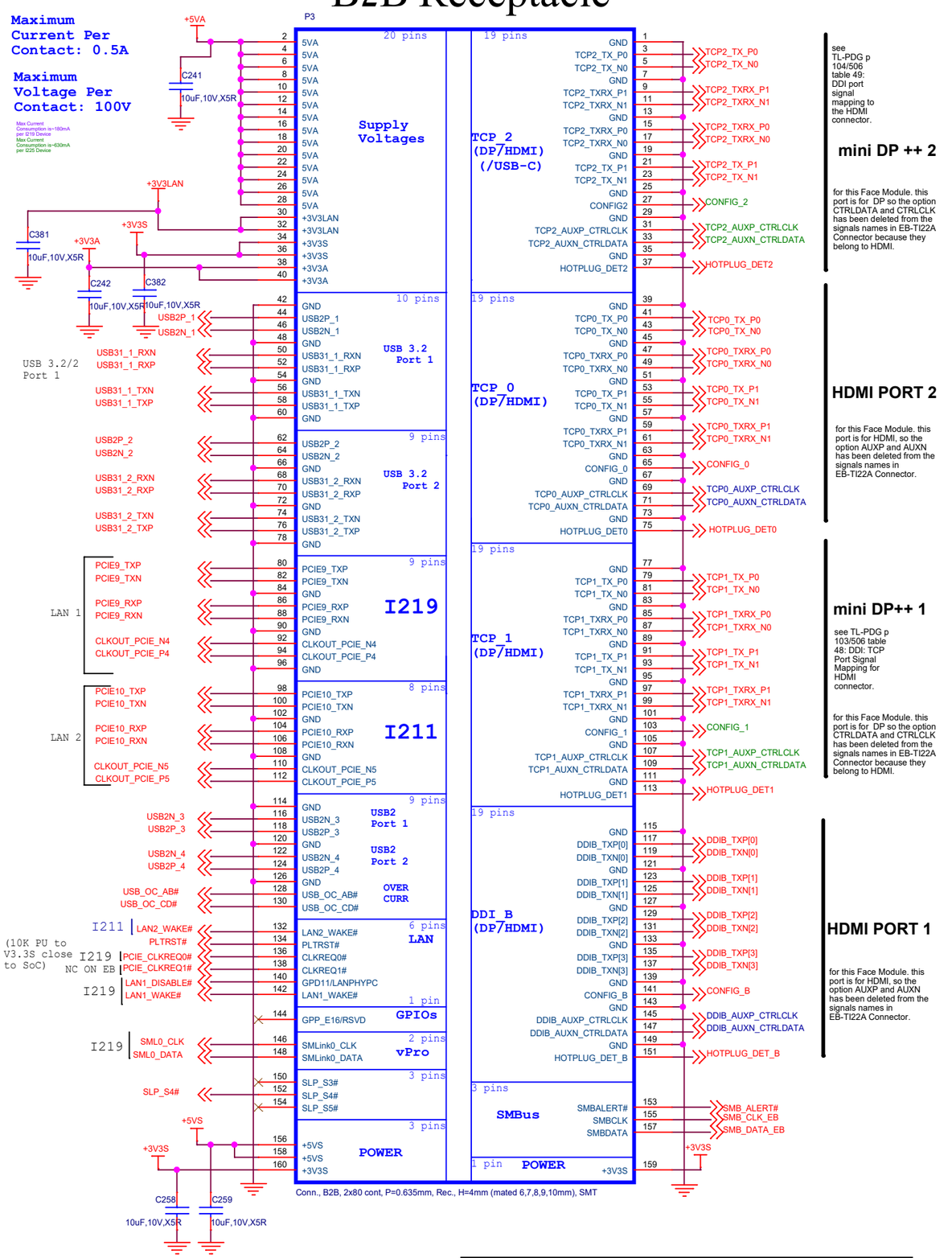
Note: The Intel® Ethernet Connection I219 can be connected to one of the following PCI Express* ports 7, 8 or, 9





182K16001S

B2B Receptacle



see TL-PDG p 104/506 table 49: DDI port signal mapping to the HDMI connector.

mini DP ++ 2

for this Face Module. this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they belong to HDMI.

HDMI PORT 2

for this Face Module. this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in EB-TI22A Connector.

mini DP++ 1

see TL-PDG p 103/506 table 48: DDI: TCP Port Signal Mapping for HDMI connector.

for this Face Module. this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they belong to HDMI.

HDMI PORT 1

for this Face Module. this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in EB-TI22A Connector.

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p.143/187 TL-EDS

12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] **TX** DDIB_TXN[3:0]	**Digital Display Interface Transmit:** DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P **AUX** DDIB_AUX_N	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

p.103/507 TL-TDG

Table 38. DisplayPort* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx) **TX**	DDIx_TXP/N[3:0]	N/A	N/A	1
	TCPx_TX_P/N[1:0] and TCPx_TXRX_P/N[1:0]	N/A	N/A	2
Aux Channel **AUX**	DDIx_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

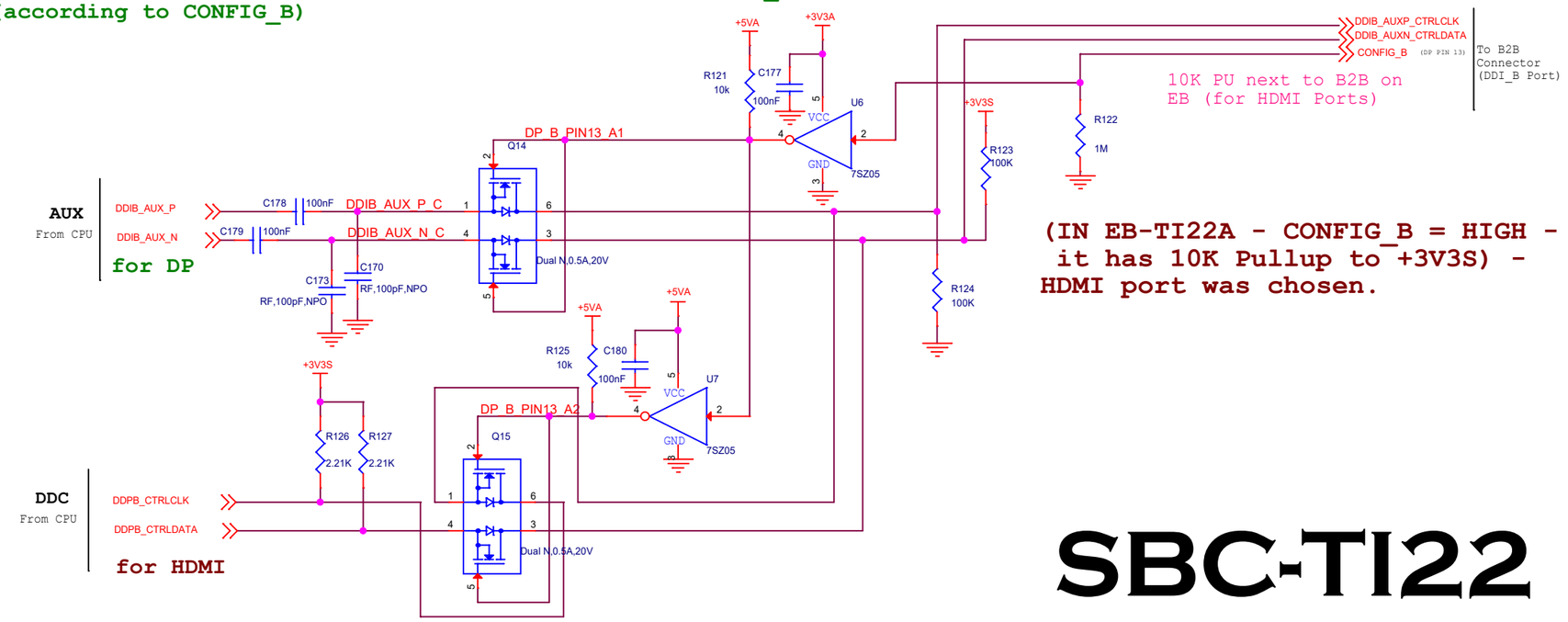
p.103/507 TL-TDG

Table 47. HDMI* Signals

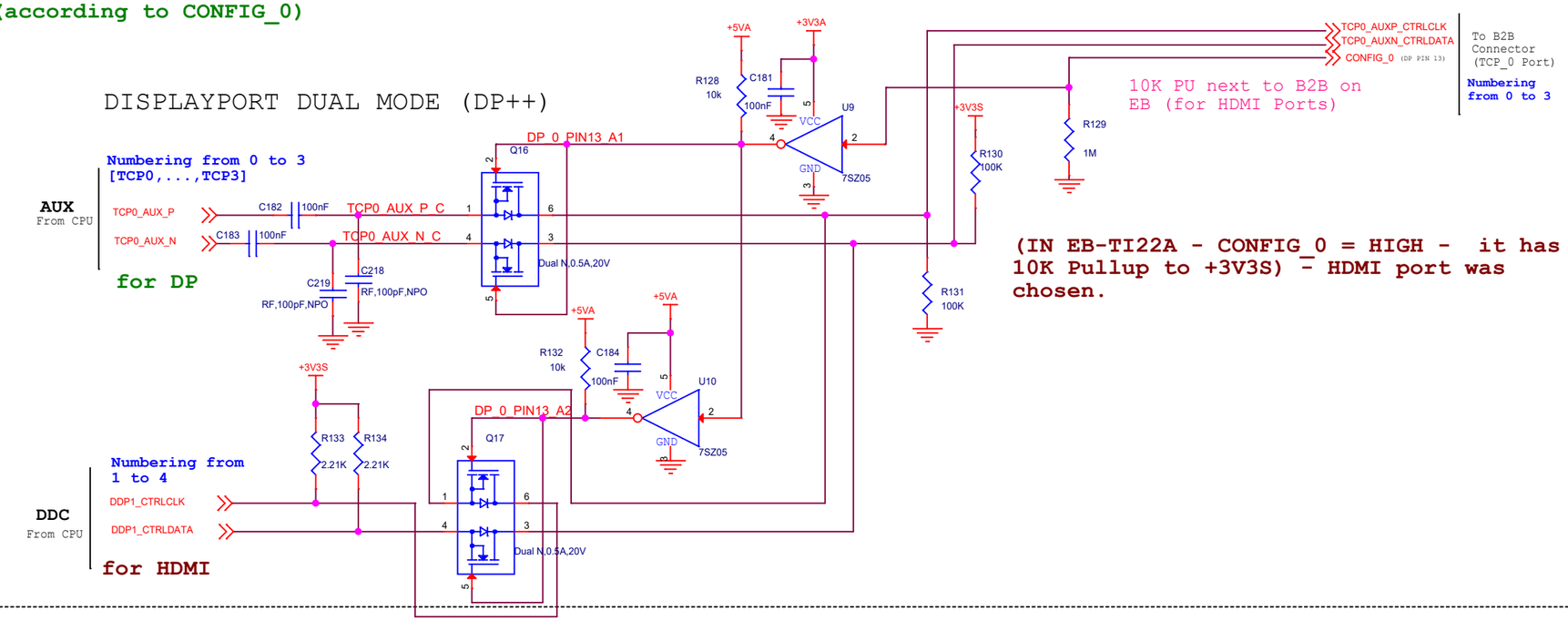
Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx) **TX**	DDIx_TXP/N[3:0]	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	2
DDC **DDC**	N/A	DDPx_CTRLCLK and DDPx_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

Note:
1. Signal names apply for DDI A/B ports.
2. Signal names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

DP(AUXP, AUXN) or HDMI(CTRLCLK, CTRLDATA) select for DDI_B (according to CONFIG_B)



DP(AUXP, AUXN) or HDMI(CTRLCLK, CTRLDATA) select for TCP0 (according to CONFIG_0)



SBC-TI22

Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode>
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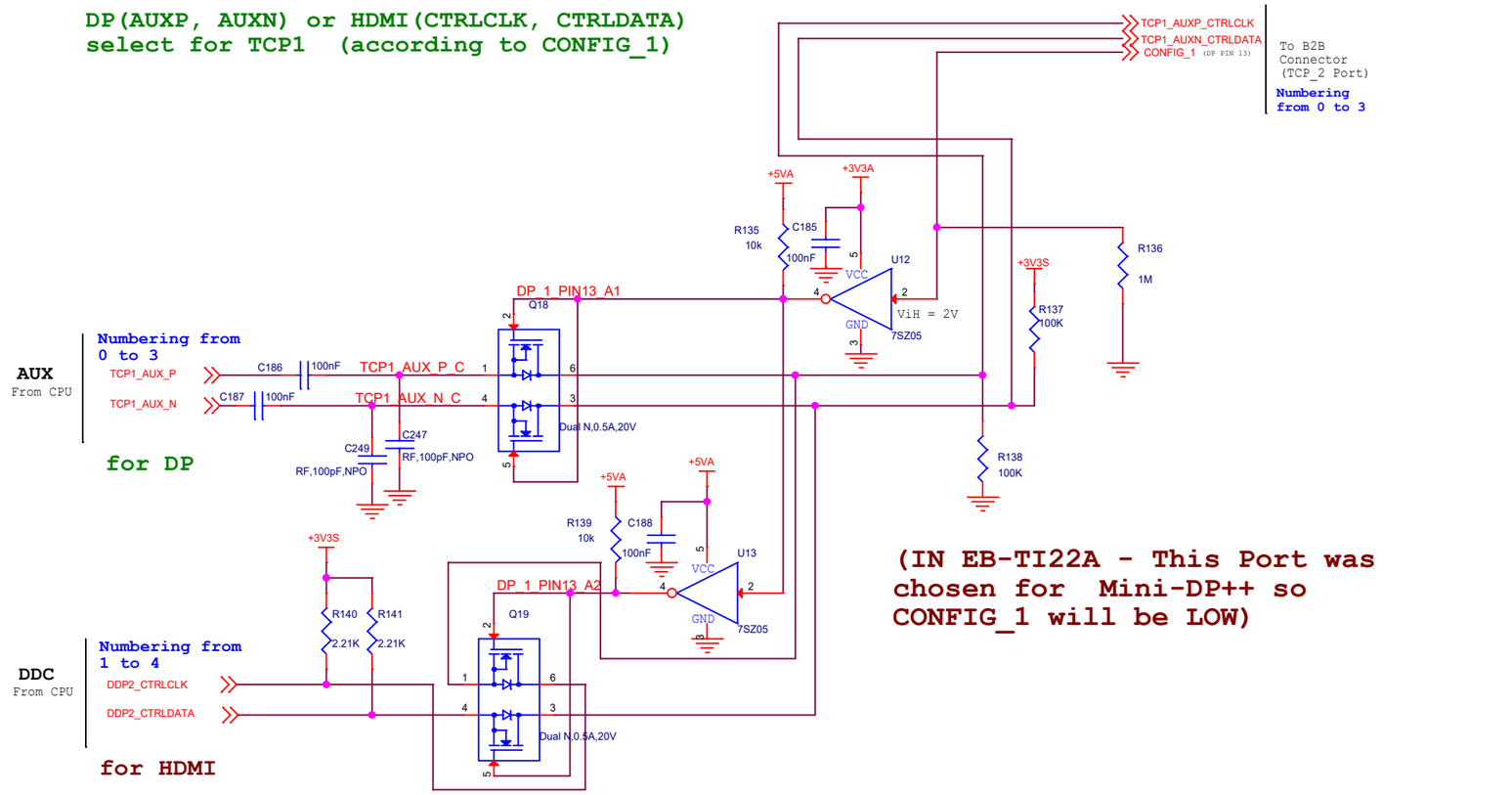

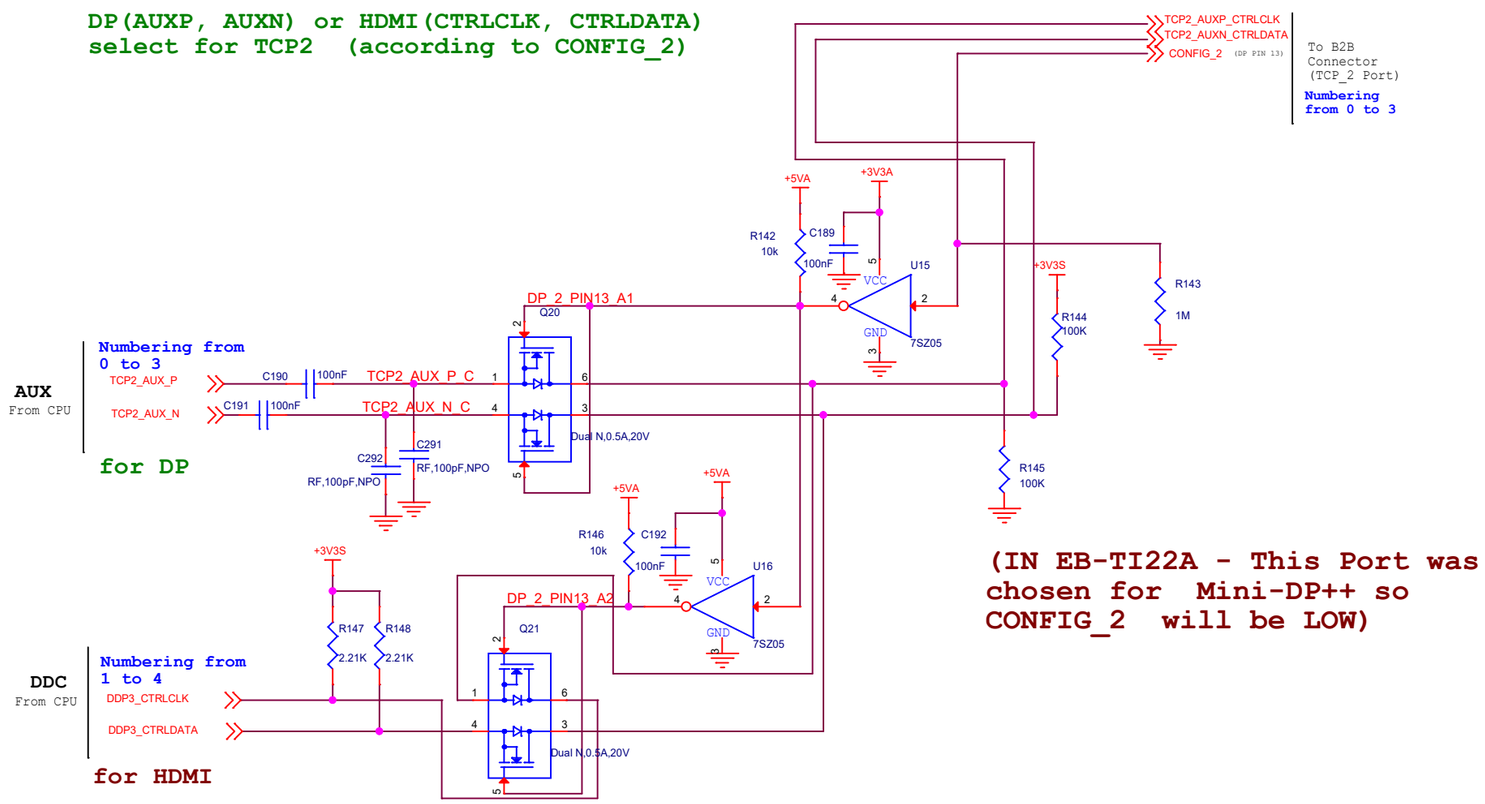

12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] DDIB_TXN[3:0] TX	**Digital Display Interface Transmit:** DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P DDIB_AUX_N AUX	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

Table 38. DisplayPort* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx) TX	DDIx_TXP/N[3:0]	N/A	N/A	1
	TCPx_TX_P/N[1:0] and TCPx_TXRX_P/N[1:0]	N/A	N/A	2
Aux Channel AUX	DDIx_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

Table 47. HDMI* Signals

Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx) TX	DDIx_TXP/N[3:0]	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	2
DDC DDC	N/A	DDPx_CTRLCLK and DDPx_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

Note:
1. Signal names apply for DDI A/B ports.
2. Signal names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

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C:\Users\firas.abdelghani\Dropbox\Board-Design\Design Techniques\DDR4\ACPI DDR4 SO-DIMM 32GB CMA6-5IH01BAR01M00.pdf

Memory, DDR4, SODIMM-260, 32GB, 2400MHz/2666MHz, 1.2V 111L63202

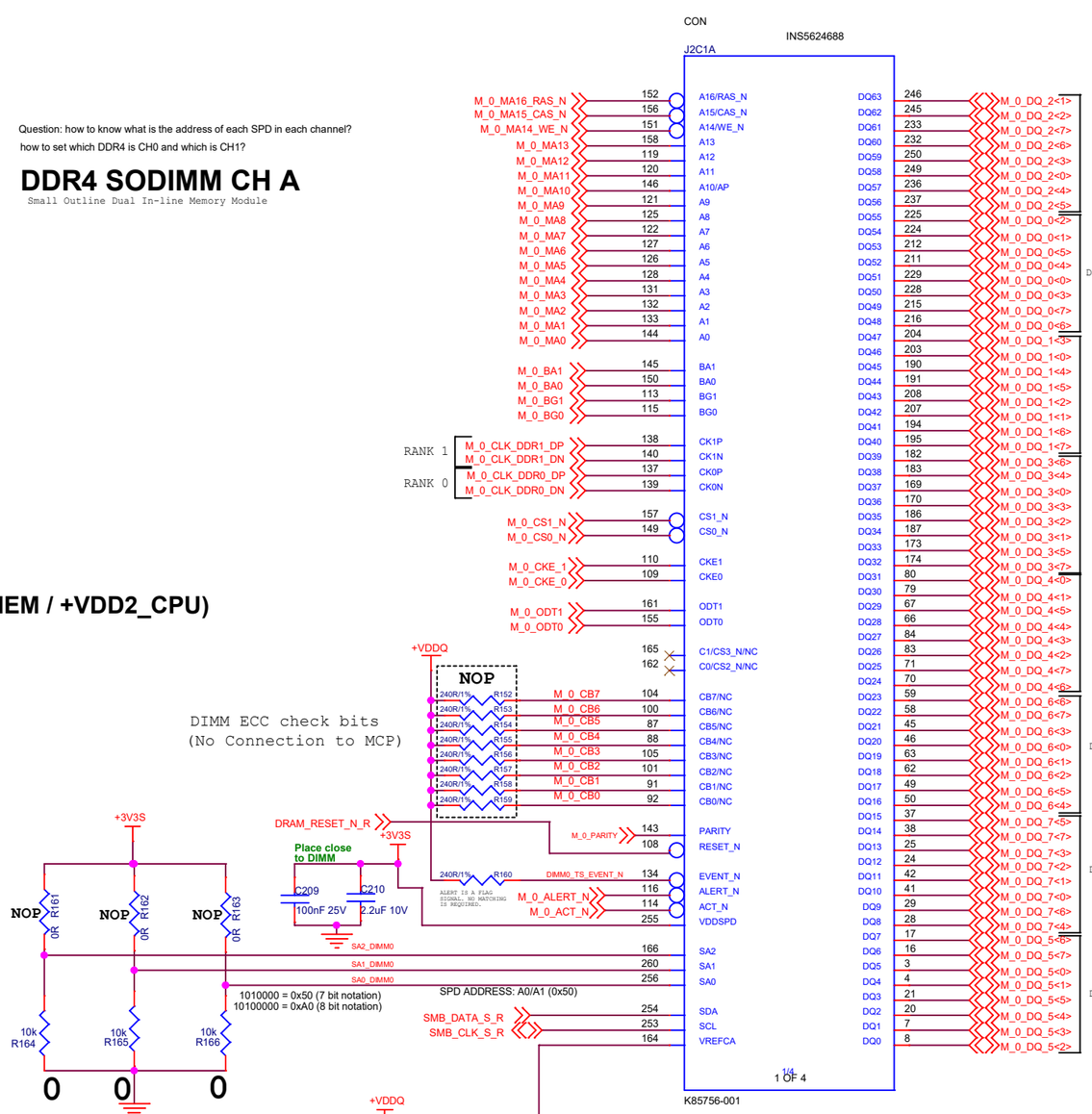
Question: how to know what is the address of each SPD in each channel?
how to set which DDR4 is CH0 and which is CH1?

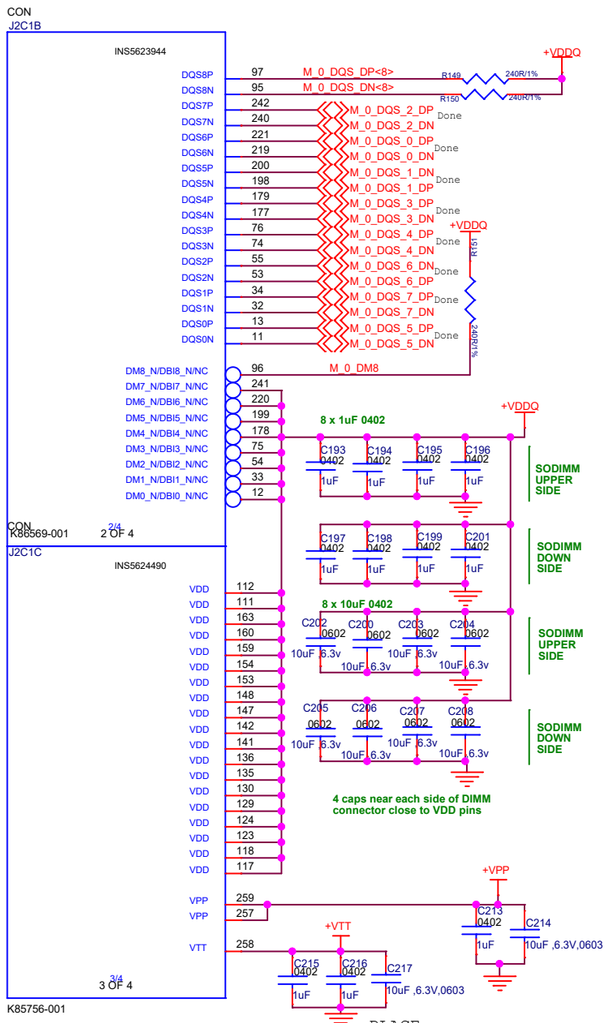
DDR4 SODIMM CH A

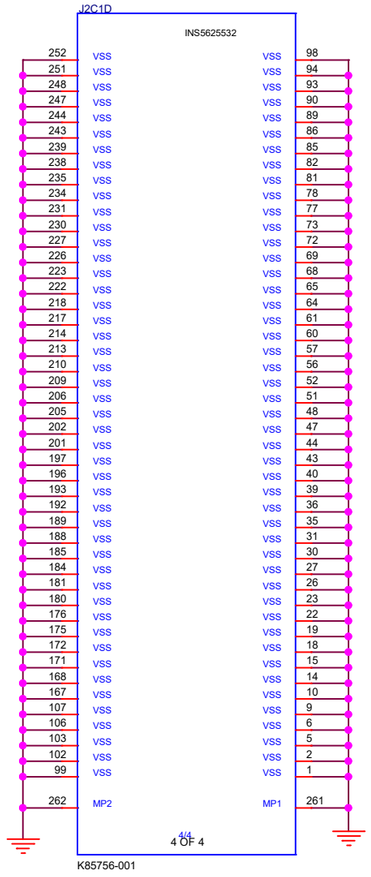
Small Outline Dual In-line Memory Module

+VDDQ (+VDD2_MEM / +VDD2_CPU)

DIMM ECC check bits
(No Connection to MCP)

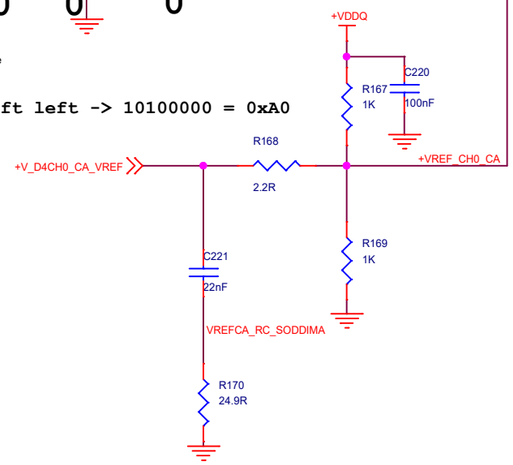






the outside resistors feed value of 000 (0x00) to the 3 pins - so the SPD connected there will respond at address 0x52 (0x50 + 0x00), shifted left 1 bit and the Read/Write bit added on - so 0xA0 or 0xA1

0x50 (Hex) = 01010000
0x50 = 01010000 -> shift left -> 10100000 = 0xA0



PLACE C217 ON VTT PLANE CLOSE TO DIMM

Title	<Title>	
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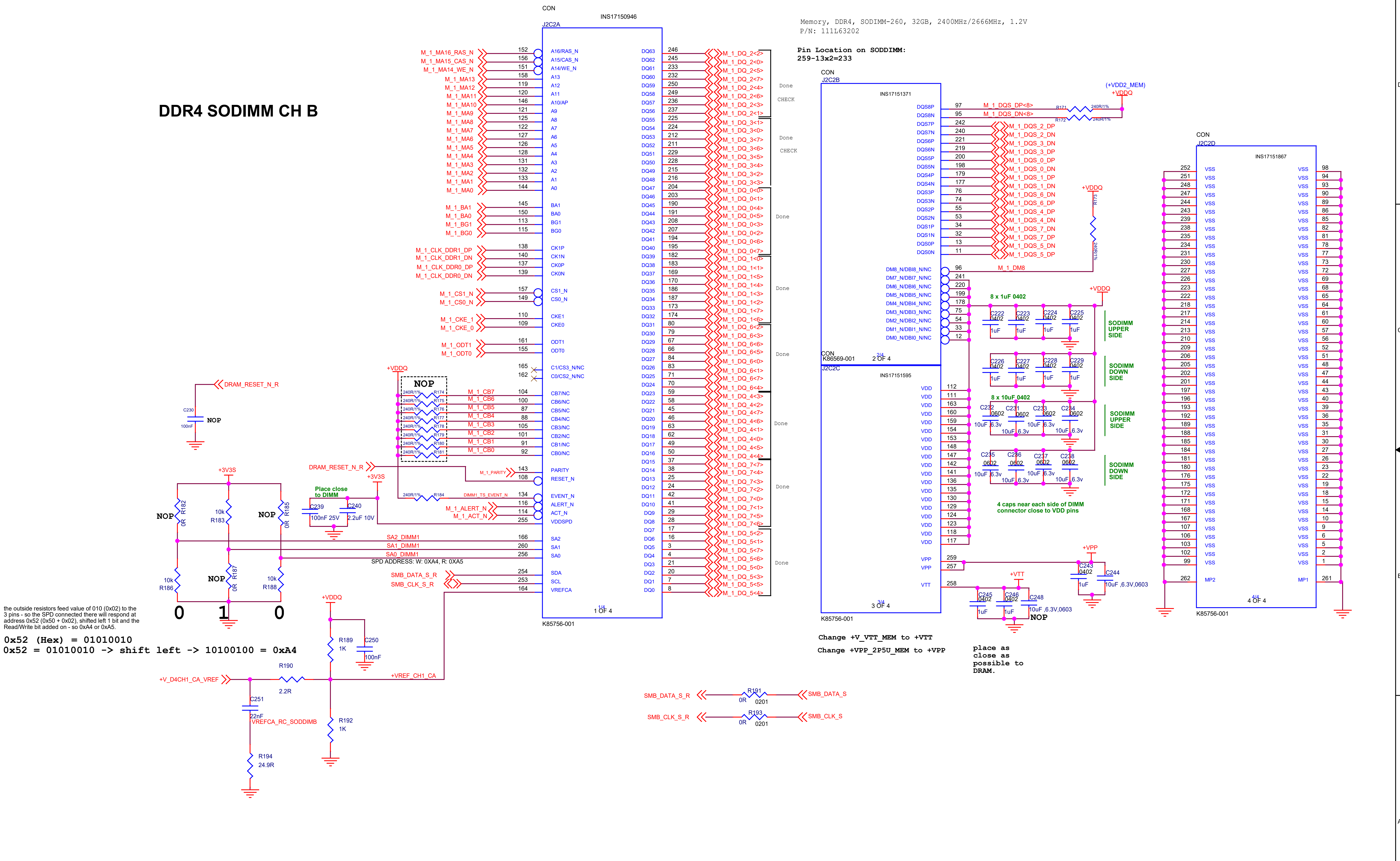
Memory, DDR4, SODIMM-260, 32GB, 2400MHz/2666MHz, 1.2V111L63202

DDR4 SODIMM CH B



Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
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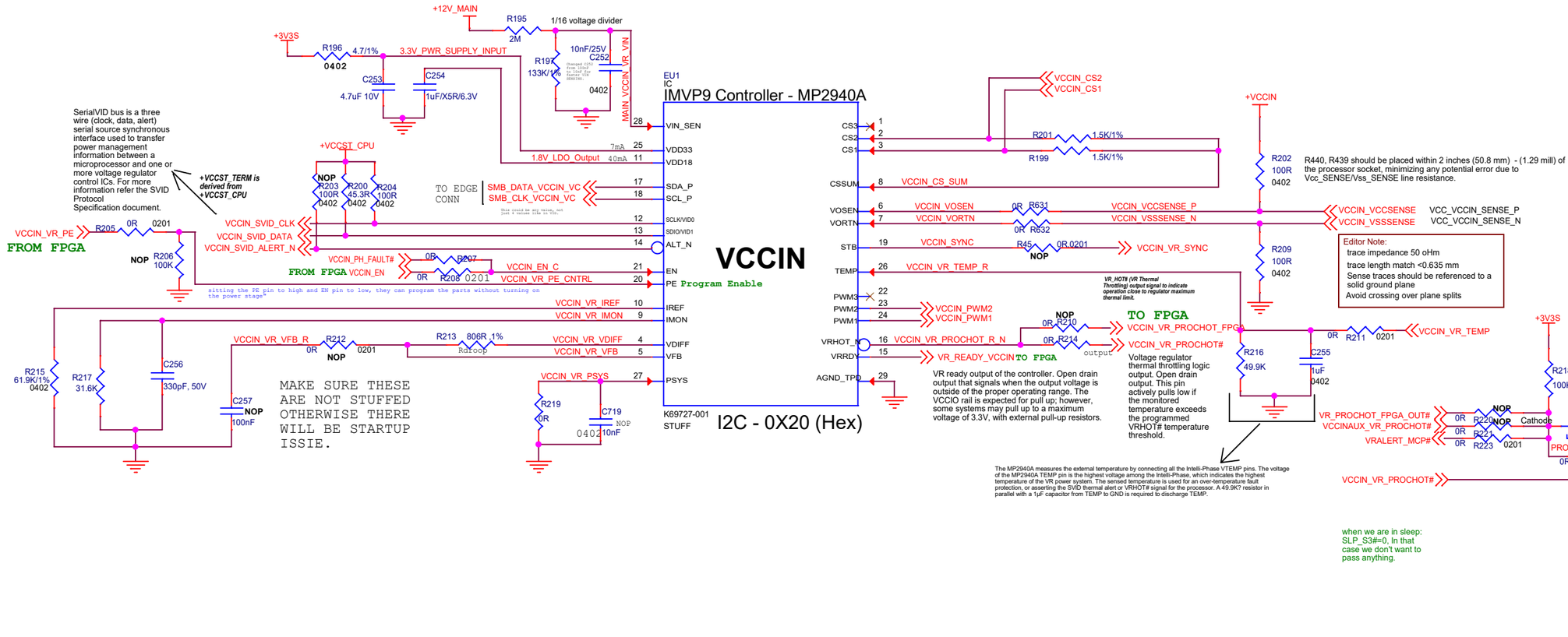
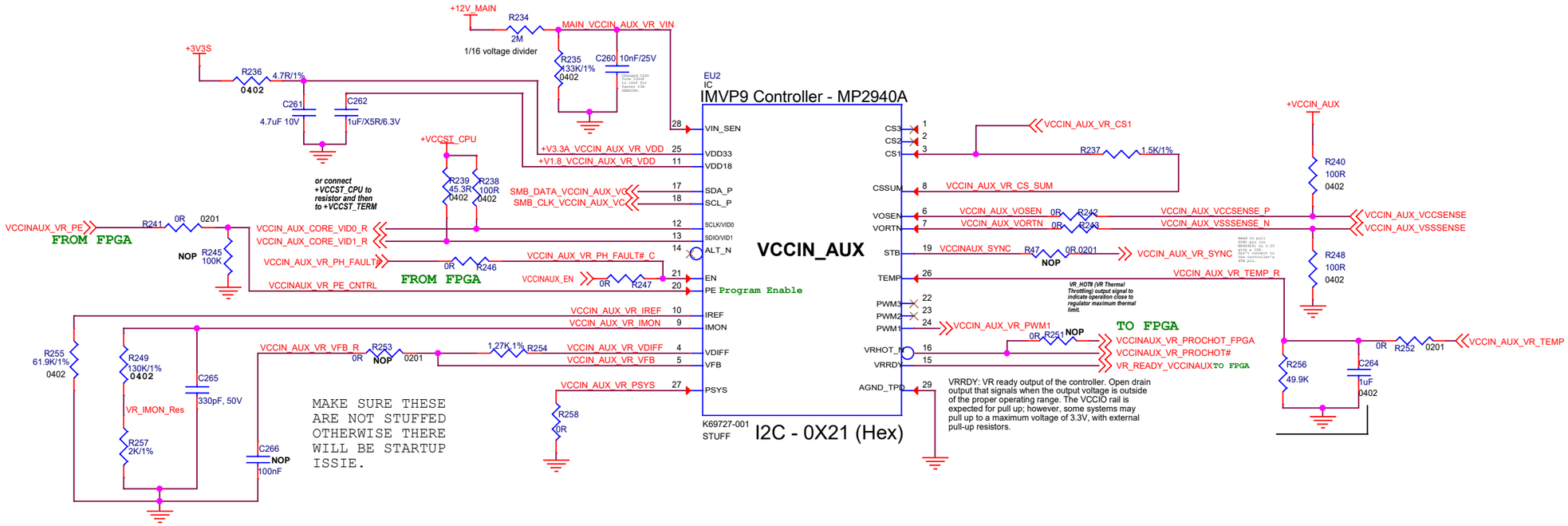
VCCIN RAIL POWER CONVERSION



VCCIN_AUX RAIL POWER CONVERSION



VID TABLE			
VID 1	VID 2	Output Voltage	Usage
0	0	0V	Power Saving State
0	1	1.1V	Register
1	0	1.65V	Full Current, TGL-UP4
1	1	1.8V	Initial boot for TGL-UP3/UP4 Full current, TGL-UP3

Title	IMVP9 CTLR-VCCIN / VCCIN_AUX	
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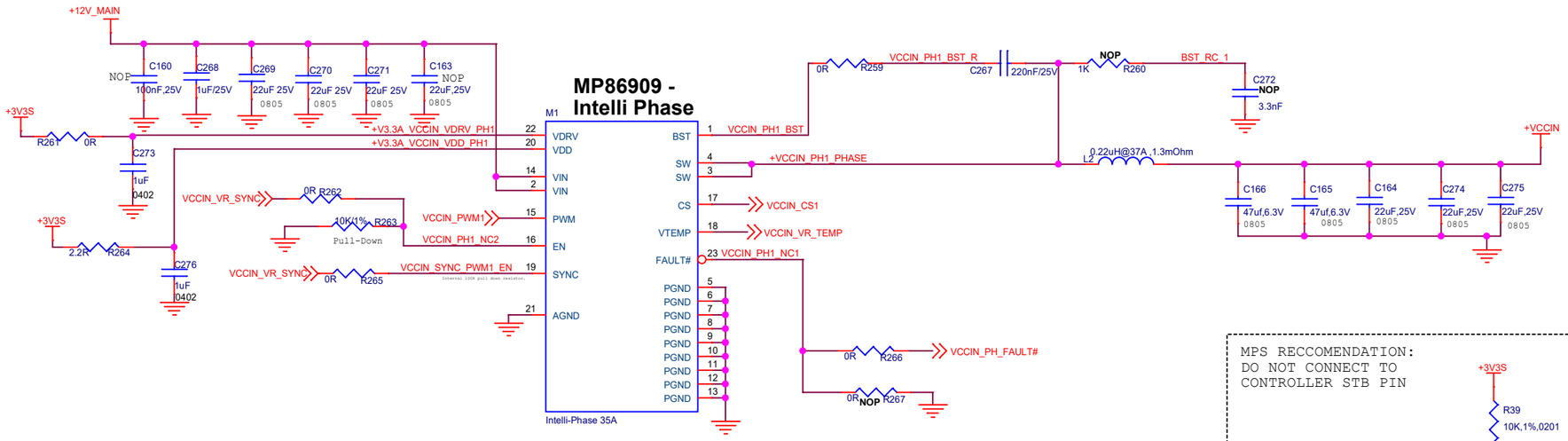
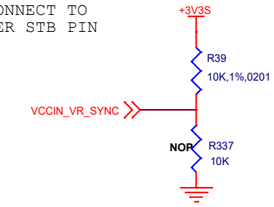
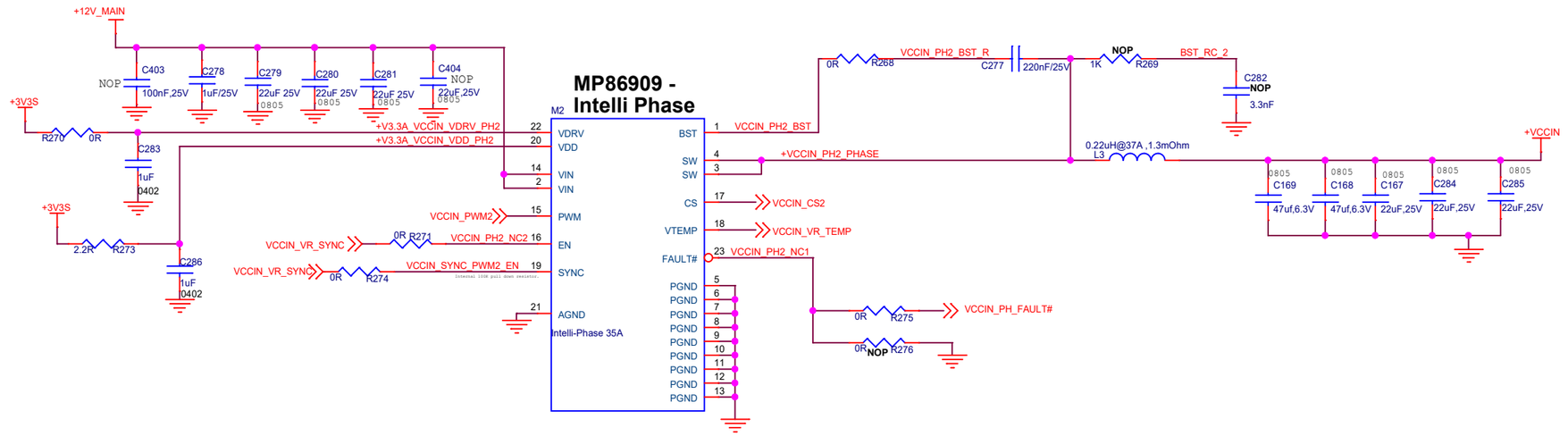


VCCIN POWER CONVERSION PHASE I

MPS RECCOMENDATION:
DO NOT CONNECT TO
CONTROLLER STB PIN





VCCIN POWER CONVERSION PHASE II

Title	PWR IMVP9- VCCIN PH1/PH2/PH3		
Size A3	Document Number <Doc>		Rev <RevCode>
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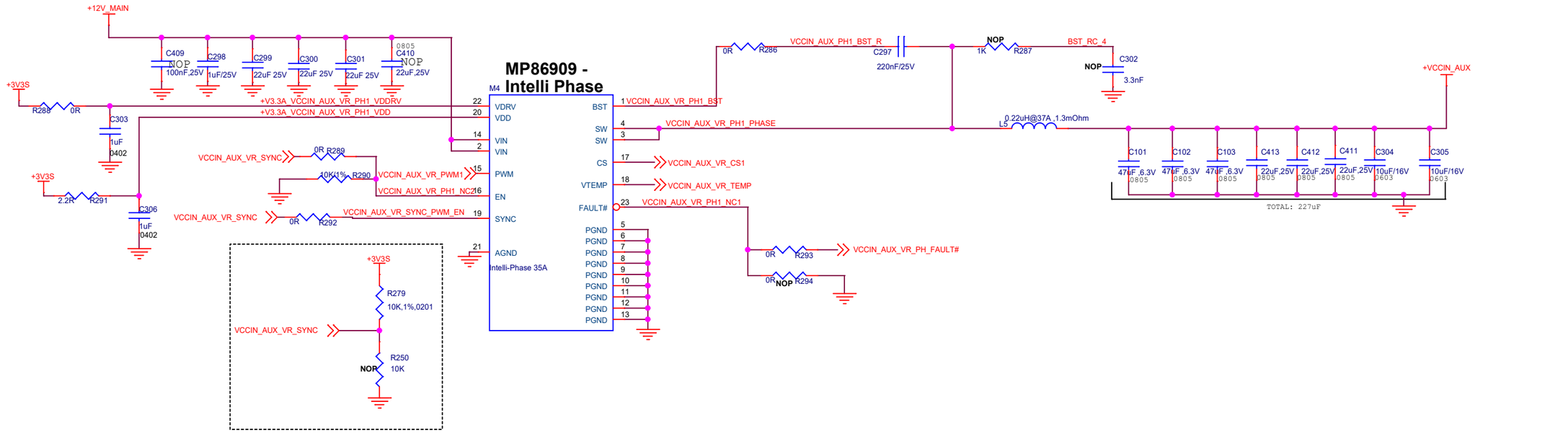
VCCIN_AUX POWER CONVERSION PHASE I



Title	PWR IMVP9- VCCIN_AUX PH1	
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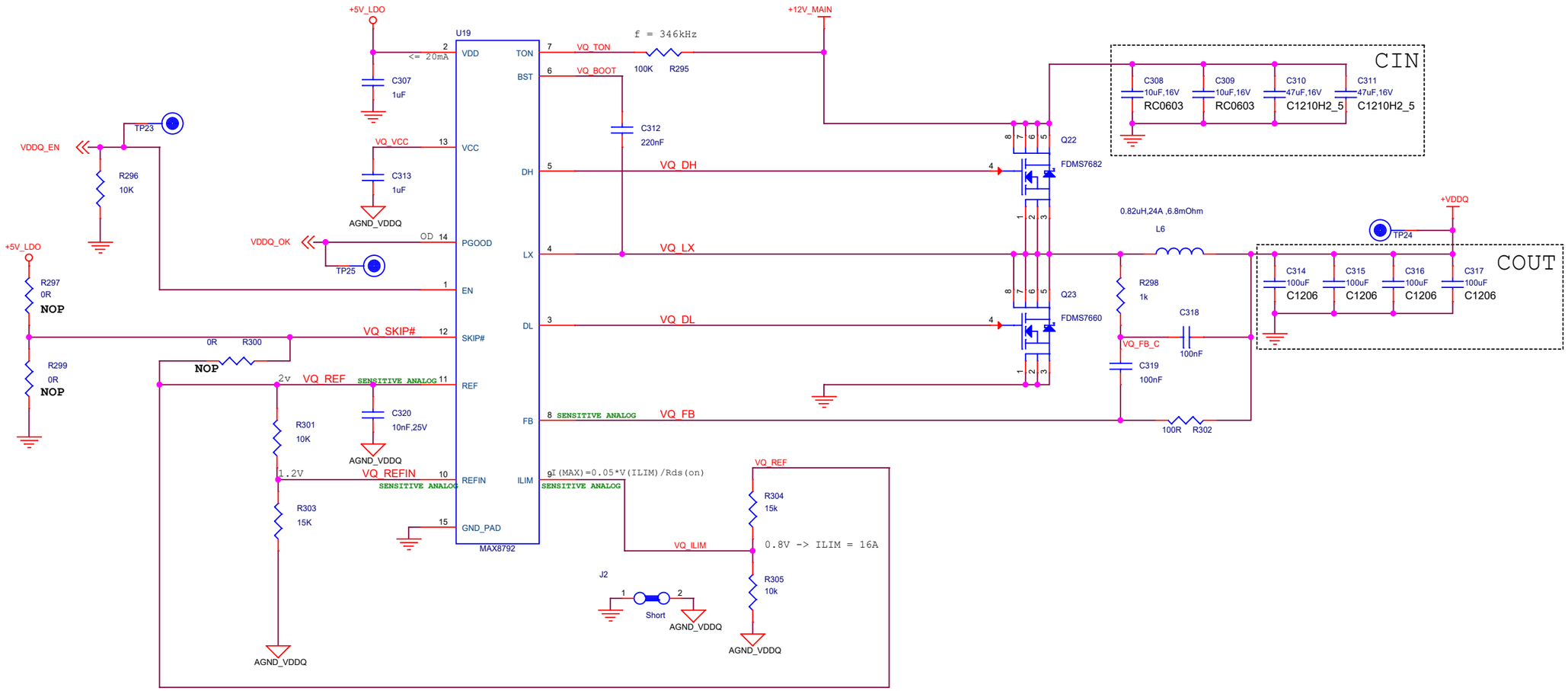
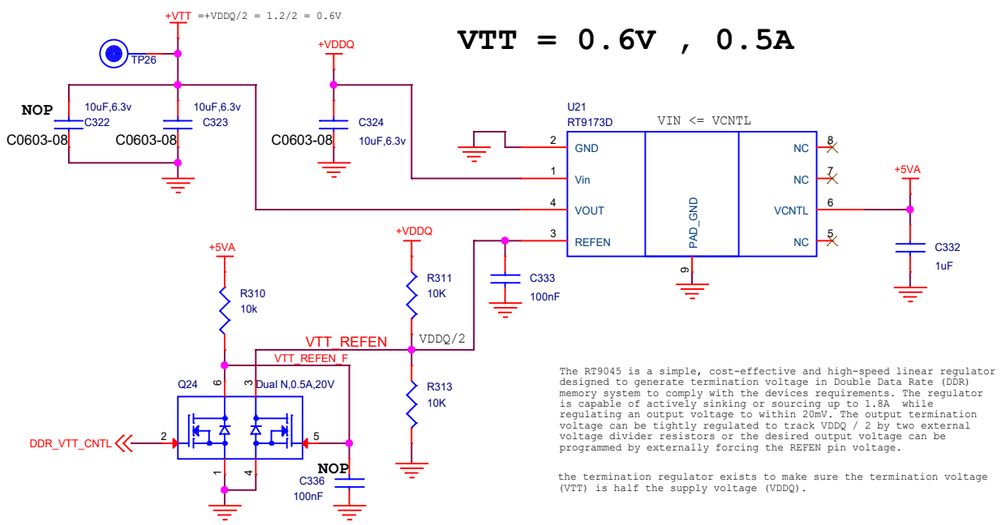
VDDQ = 1.2V , 15A



VTT = 0.6V , 0.5A



The RT9045 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in Double Data Rate (DDR) memory system to comply with the devices requirements. The regulator is capable of actively sinking or sourcing up to 1.8A while regulating an output voltage to within 20mV. The output termination voltage can be tightly regulated to track VDDQ / 2 by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

the termination regulator exists to make sure the termination voltage (VTT) is half the supply voltage (VDDQ).

VPP = 2.5V , 1A

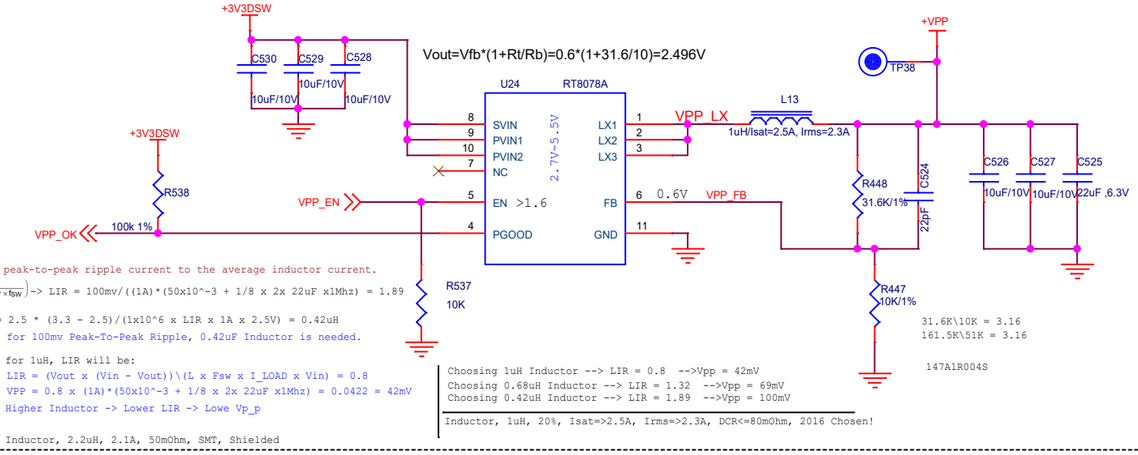
Efficiency with VIN = 3.3V at 1A Load Current = 94%

$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$ = 1A + ((1.89\2) x 1A) = 1.945A

$I_{IN\_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$

$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{IN} \times f_{SW}}$

I_vpp_max = 1A (According to Intel CRB)
VPP = 2.5V +0.25/-0.125 V (Sodimmm Spec)--> Vpk2pk = 375mV



LIR: is the ratio of the peak-to-peak ripple current to the average inductor current.

$V_{P\_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$ -> LIR = 100mv/((1A)*(50x10^-3 + 1/8 x 2x 22uF x1Mhz) = 1.89

$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$ = 2.5 * (3.3 - 2.5)/(1x10^6 x LIR x 1A x 2.5V) = 0.42uH

for 100mv Peak-To-Peak Ripple, 0.42uF Inductor is needed.

$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$

where V_{REF} is 0.6V (typ.).

for 1uH, LIR will be:
LIR = (Vout x (Vin - Vout))\(L x Fsw x I_LOAD x Vin) = 0.8
VPP = 0.8 x (1A)*(50x10^-3 + 1/8 x 2x 22uF x1Mhz) = 0.0422 = 42mV
Higher Inductor -> Lower LIR -> Lowe Vp_p

Inductor, 2.2uH, 2.1A, 50mOhm, SMT, Shielded

Choosing 1uH Inductor --> LIR = 0.8 -->Vpp = 42mV
Choosing 0.68uH Inductor --> LIR = 1.32 -->Vpp = 69mV
Choosing 0.42uH Inductor --> LIR = 1.89 -->Vpp = 100mV

Inductor, 1uH, 20%, Isat=>2.5A, Irms=>2.3A, DCR<=80mOhm, 2016 Chosen!

Title: PWR VDDQ/VTT/VPP		
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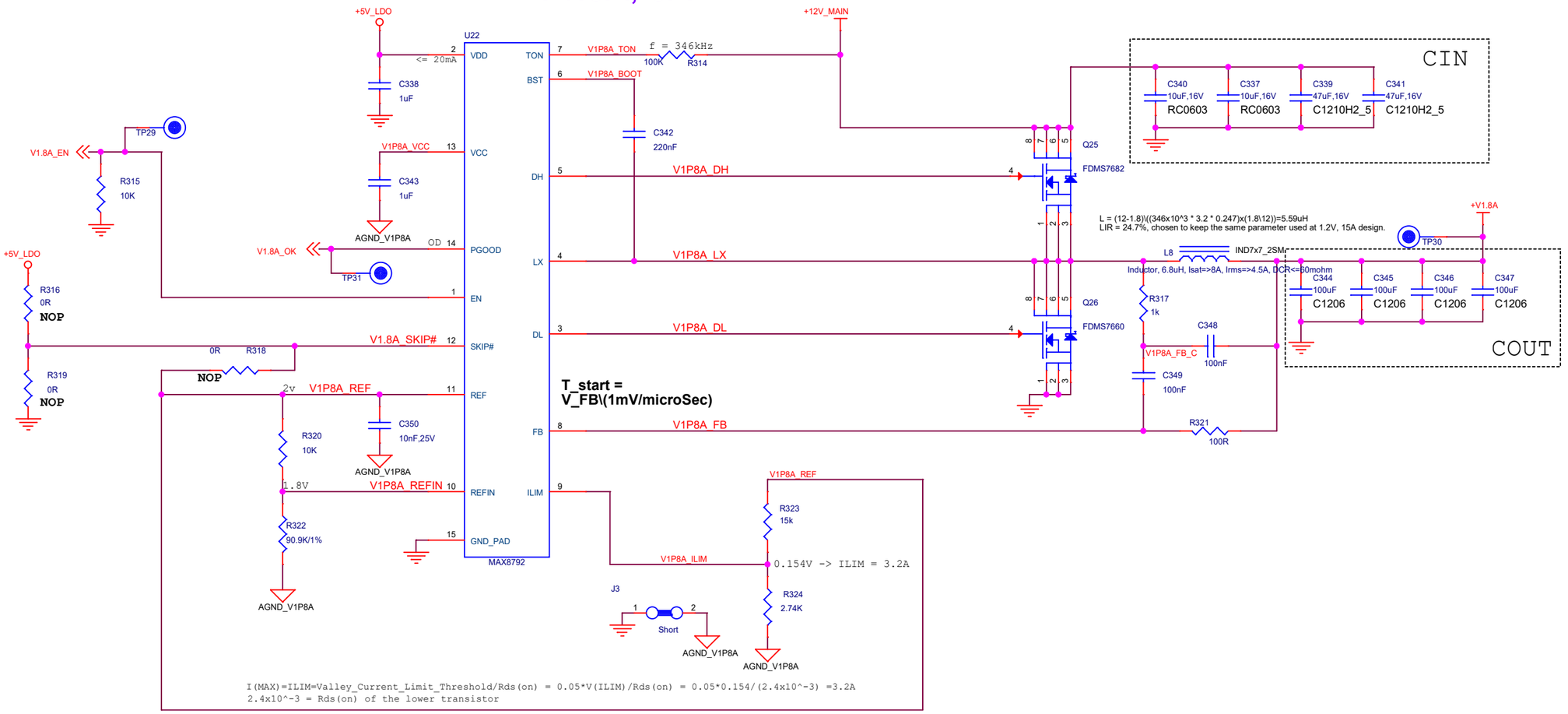
+V1.8A, 3A



Title	PWR +V1.8A	
Size A3	Document Number <Doc>	Rev <RevCode>
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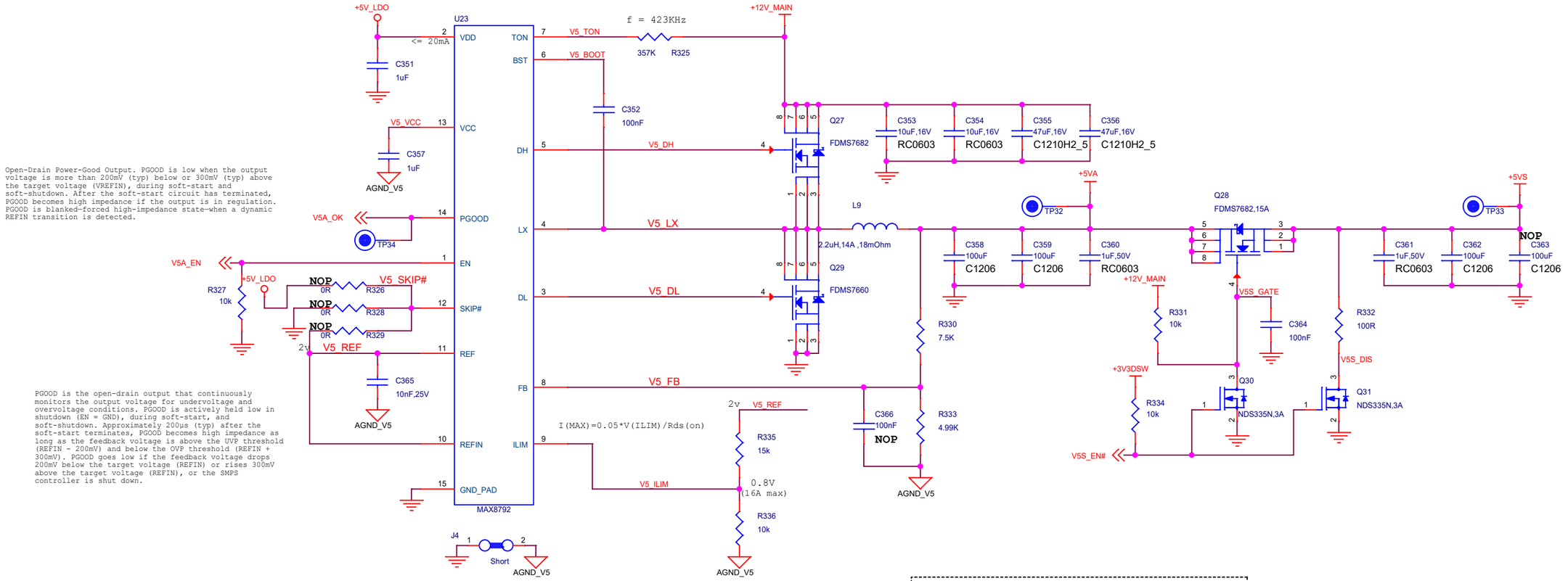
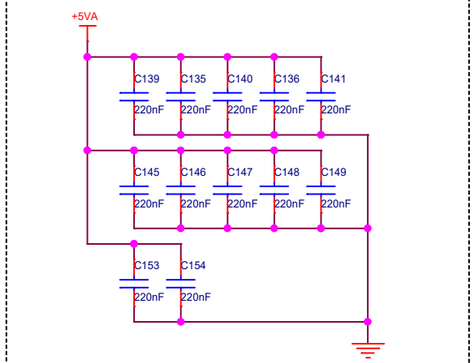
5V , 15A



Plane stitching capacitors



Title	PWR 5V		
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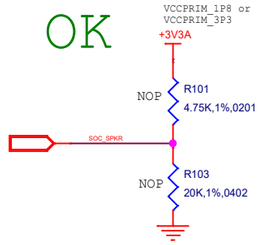
PCH STRAPS

TOP SWAP OVERRIDE

GPP_B14

OK



The strap has a 20 kohm ± 30% internal pull-down.

0=>Disable "Top Swap" mode. (Default)
1=>Enable "Top Swap" mode.

This inverts an address on access to SPI, so the processor fetches the alternate boot block instead of the original boot-block. PCH will invert the appropriate address lines (A[23:16]) as selected in Top Swap Block size soft strap.

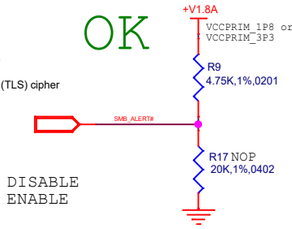
1. The internal pull-down is disabled after PCH_PWROK is high.
2. Software will not be able to clear the Top Swap (TS) bit (Bus0, Device31, Function0, offset DCh, bit 4) until the system is rebooted.
3. The status of this strap is readable using the Top Swap bit.
4. This signal is in the primary well.

Sampled at Rising edge of PCH_PWROK

TLS CONFIDENTIALITY

GPP_C5 / SML0ALERT#

OK



ME TLS Confidentiality Strap (PU)
This strap has a 20 kohm ± 30% internal pull-down.
0=>Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1=>Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

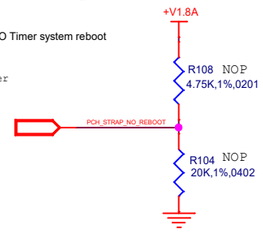
Native F1 if Intel SMBus ASD Mode Configuration soft strap = 1, else GP-Out; Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.

Sampled at Rising edge of RSMRST#

NO REBOOT

GPP_B18 / GSPI0_MOSI

OK



The strap has a 20 kohm ± 30% internal pull-down.
0=>Disable "No Reboot" mode. (Default)
1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

Notes:
1. The internal pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

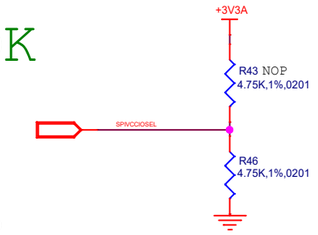
HIGH - NO REBOOT
LOW- REBOOT ENABLED
WEAK INTERNAL PD 20K

Sampled at Rising edge of PCH_PWROK

STRAP FOR SPI 1.8V/3.3V SELECTION

(NOT A GPIO)

OK



There is no internal pull-up or pull-down on the strap. An external resistor is required.
0 = SPI voltage is 3.3 V (4.7 kohm pull-down to GND)
1 = SPI voltage is 1.8 V (4.7 kohm pull-up to VCCDSW_3P3)

Not sampled. This strap must always be driven to a valid logic level

DDP3 I2C / TBT_LSX2 pins VCC configuration

GPP_D10 / ISH_SPI_CLK / DDP3_CTRLDATA / TBT_LSX2_RXD / BSSB_LS2_TX / GSPI2_CLK

OK

VCCPRIM_1P8 or VCCPRIM_3P3

Already Has 100K PU (R144) to 3V3S at the DP++ HANDLING (Page 22)

This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 1.8 V
1 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 3.3 V

Strap read at rising edge of RSMRST#. External pull-up is required if signal used as HDMI Display I2C. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts

Sampled at Rising edge of RSMRST#

SPI0_IO2 STRAP - RSVD

PU PLACED NEXT TO SPI FLASH (U26)

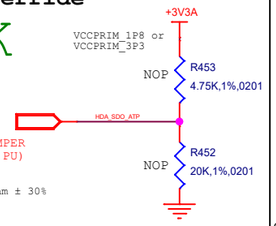
SPI0_IO3 STRAP - RSVD

PU PLACED NEXT TO SPI FLASH (U26)

Flash Descriptor Security Override

GPP_R2 / HDA_SDO / I2S0_TXD STRAP

OK



HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN

WEAK INTERNAL PD 20K

THIS SIGNAL IS TIED TO A JUMPER ON ATP CARD (IF JUMPER INSIDE HDA_SDO_ATP IS PULLED TO +V3VDSW THROUGH 1K PU)

Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% pull-down is disabled after PCH_PWROK is high.

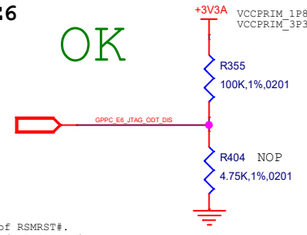
To support Intel® ME, a SPI flash is required on the platform with sufficient space to hold system BIOS, Intel® ME firmware, Intel® Integrated Sensor Solution firmware and any additional third party data storage. The SPI flash needs to be powered in states S0 through S5, independent of Intel® ME power state.
GPP_R2 / HDA_SDO / I2S0_TXD signal is used for Flash Descriptor Security Override (which is also known as Intel® ME Debug Mode). This signal input should be tied to a jumper which connects to power through an external pull-up (1 KΩ ±5%) only. When this signal is asserted, the Flash Security gets overridden for ease of image programming.

Sampled at Rising edge of PCH_PWROK

JTAG ODT DISABLE - GPP_E6

GPP_E6 / THC0_SPI1_RST#

OK



This strap does not have an internal pull-up or pull-down. External pull-up is recommended
0=> JTAG ODT is disabled
1=> JTAG ODT is enabled

CAD NOTE:

Strap read at rising edge of RSMRST#. External pull-up is required. Recommend 100 kohm. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

PLACE R355 AND R404 CLOSE TO THE SPI SIGNAL TO AVOID STUB

USB_OC_CD#

OK

10K PU at EB-TI22A

GPP_E10 / THC0_SPI1_CS#

OK

THC0_SPI1 Chip Select: Used to select the touch devices if it is connected to THC0_SPI1 interface.

THC NOT USED IN TENSOR-I22

CAD NOTE:

PLACE R414,R415 AND R422 CLOSE TO THE SPI SIGNAL TO AVOID STUB

GPP_E11 / THC0_SPI1_CLK

OK

THC0_SPI1 Clock: THC0 SPI1 clock output from PCH. Supports 20 MHz, 33 MHz and 50 MHz.

THC NOT USED IN TENSOR-I22

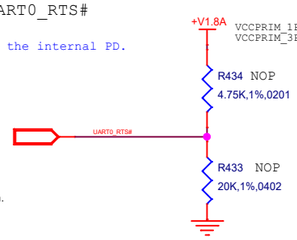
CAD NOTE:

PLACE R429,R430 AND R431 CLOSE TO THE SPI SIGNAL TO AVOID STUB

XTAL Frequency Selection

GPP_F0 / CNV_BRI_DT / UART0_RTS#

OK



GPP_F0 Pin is at 0 (38.4 Mhz) by the internal PD.

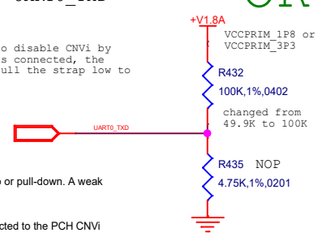
This strap has a 20 kohm ± 30% internal pull-down.
0 = 38.4 MHz (default)
1 = 24 MHz
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

M.2 CNVi Mode Select

GPP_F2 / CNV_RGI_DT / UART0_TXD

OK



A weak external PU is required to disable CNVi by default. When a companion chip is connected, the required PD on the device will pull the strap low to enable CNVi.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.
0= Integrated CNVi enabled.
1= Integrated CNVi disabled.
Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

Sampled at Rising edge of RSMRST#

USB_OC_AB#

OK

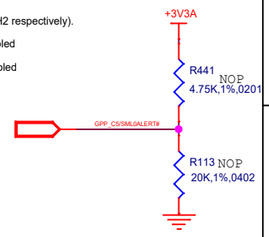
10K PU at EB-TI22A

BOOT STRAP - BIT 0

OK

This strap has a 20 kohm ± 30% internal pull-down.
This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration.
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).
4-bit boot strap configuration encodings:
0000 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is enabled

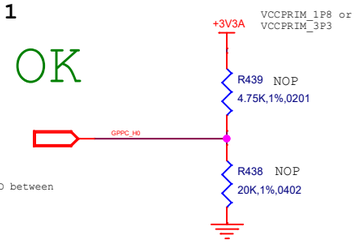
0010 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / Intel CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; Intel CSME on slave attached SPI.
Others: Reserved
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.



Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.

BOOT STRAP - BIT 1

OK



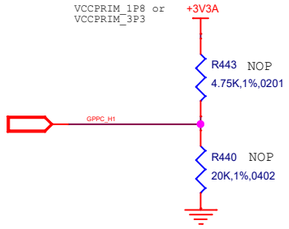
used for M2 PCH SSD RTD3, using AND between BUF_PLTRST# and GPPC_H0

Check TL-SBC (44/270)

BOOT STRAP - BIT 2

GPP_H1

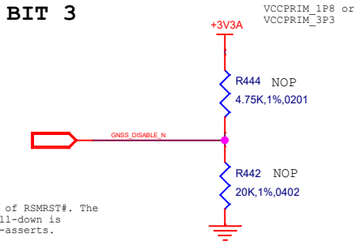
OK



BOOT STRAP - BIT 3

GPP_H2

OK



Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.

Title	PCH STRAPS (1 OF 2)	
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PCH STRAPS

DDP1 I2C / TBT_LSX0 pins VCC configuration

GPP_E19 / DDP1_CTRLDATA / TBT_LSX0_RXD / BSSB_LS0_TX

VCCPRIM_1P8 or VCCPRIM_3P3

OK

Already Has 100K PU (R130) to 3V3S at the DP++ HANDLING (Page 21)

This strap has a 20 kohm ± 30% internal pull-down.
0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8 V
1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

there is 2.2K PU on DPP1_CTRLDATA

Sampled at Rising edge of RSMRST#

DDP2 I2C / TBT_LSX1 pins VCC configuration

GPP_E21 / DDP2_CTRLDATA / TBT_LSX1_RXD / BSSB_LS1_TX

NOTE: BSSB - Boundary Scan Sideband Low Speed Receive 1 for debug purposes

HIGH: 3.3V
LOW: 1.8V

OK

Already Has 100K PU (R137) to 3V3S at the DP++ HANDLING (Page 22)

LSx Interface:
The PCH LSx interface enables communication between one thunderbolt controller to another. TGL UP3/UP4 supports 4 pairs of LSx signals. The LSx signals use a UART interface. It operates at a 1 MHz baud rate and shares identical electrical characteristics/routing guidelines as UART.

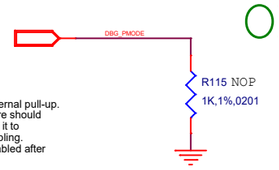
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 1.8 V
1 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

DBG_PMODE

RESERVED

OK



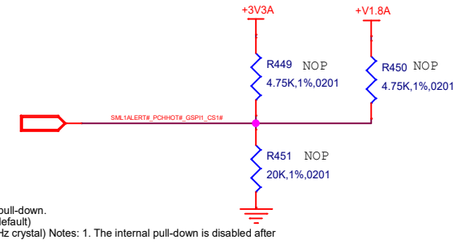
This strap has a 20 kohm ± 30% internal pull-up.
This strap should sample high. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-up is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

CPUNSSC CLOCK FREQ

GPP_B23 / SML1ALERT# / PCHHOT# / GSPI1_CS1#

OK



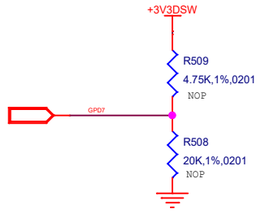
This strap has a 20 kohm ± 30% internal pull-down.
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal) Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150 kohm pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.

GPD7

STRAP: RESERVED

Strap read at rising edge of DSW_PWROK. The internal pull-down 20 kohm ± 30% is disabled after DSW_PWROK is high . This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

OK



GPP_F10

STRAP: RESERVED

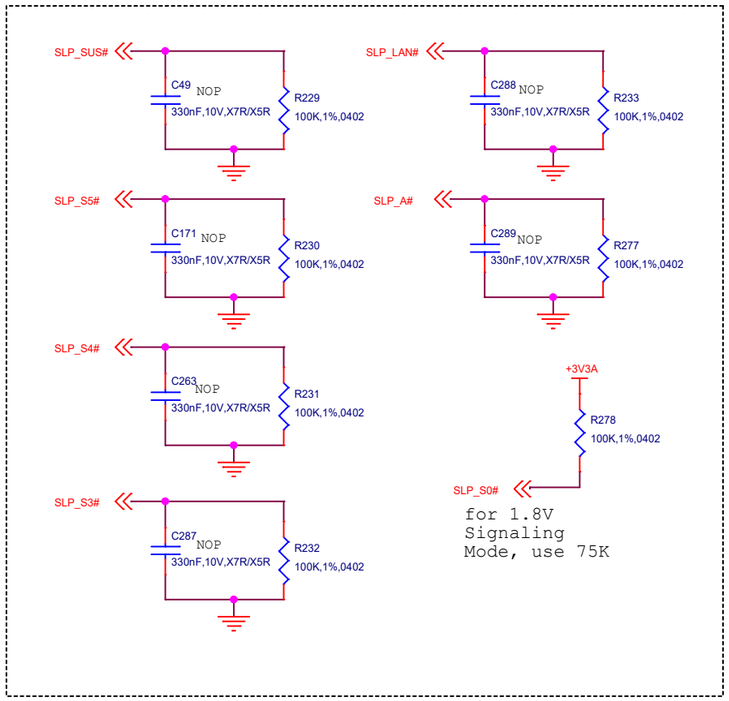
This strap has a 20 kohm ± 30% internal pull-down.
This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

OK

Sampled at Rising edge of RSMRST#

PCH GLITCH ISSUE MITIGATION

RC0201



Title: PCH STRAPS (2 OF 2)		
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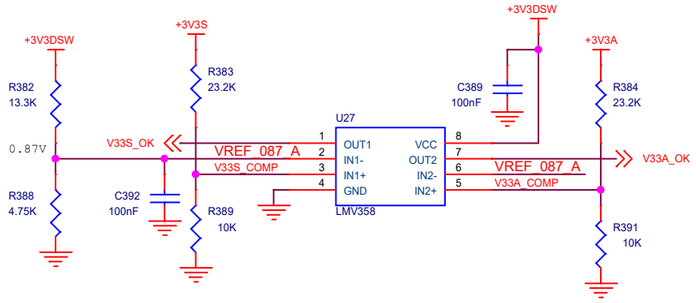
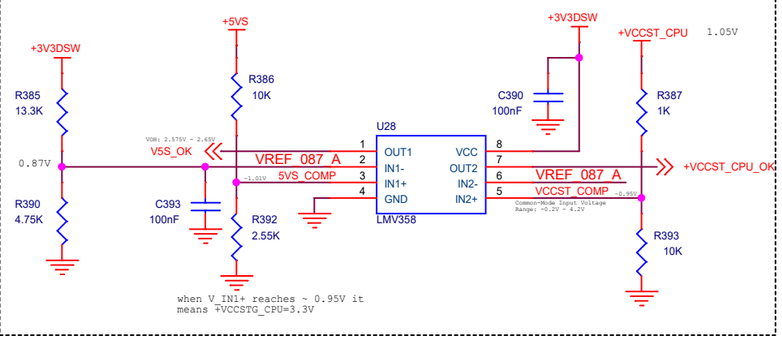
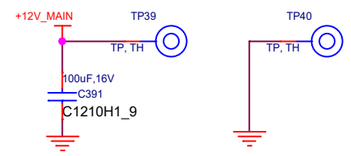
+3V3S,+3V3A PWRGD



+5VS, VCCST_CPU PWRGD



Hanging 1x2 connector



Title	3V3S\3V3A\VCCCST PWRGD	
Size A3	Document Number <Doc>	Rev <RevCo
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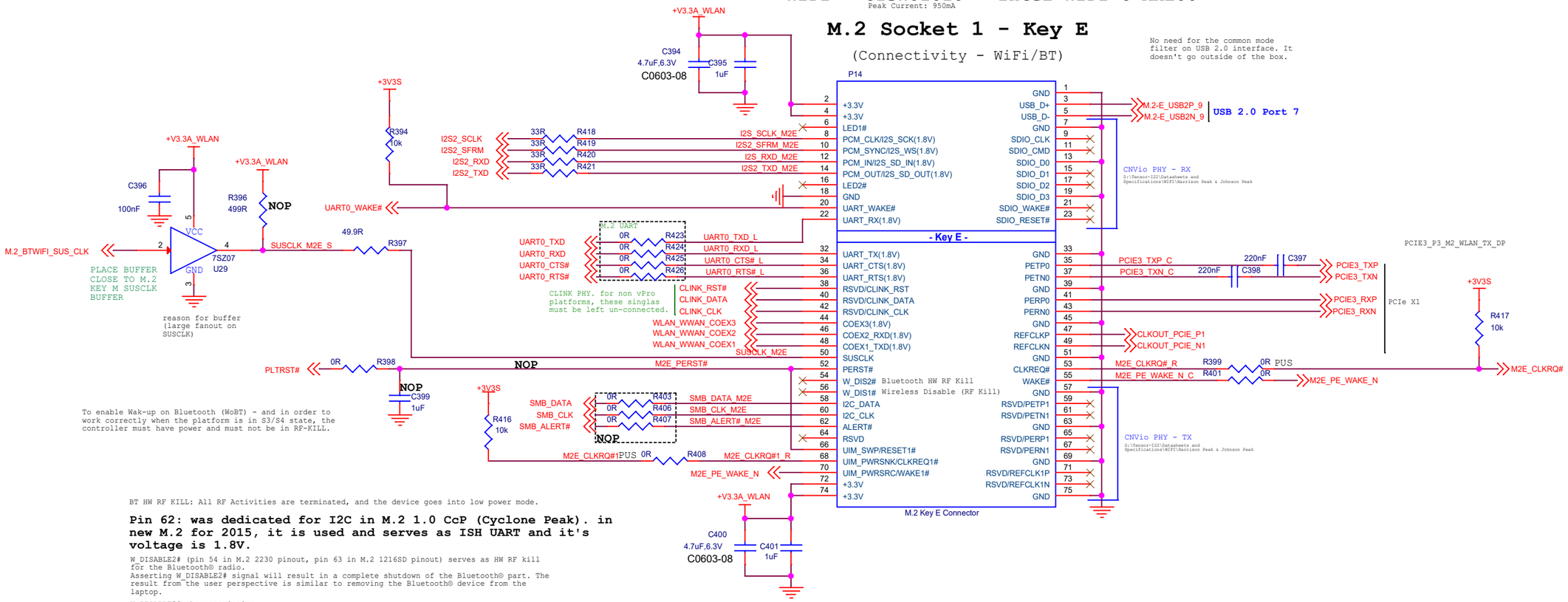
WIFI - 613W01010 - Intel WIFI 6 AX200

Peak Current: 950mA

M.2 Socket 1 - Key E

(Connectivity - WiFi/BT)

No need for the common mode filter on USB 2.0 interface. It doesn't go outside of the box.



BT HW RF KILL: All RF Activities are terminated, and the device goes into low power mode.

Pin 62: was dedicated for I2C in M.2 1.0 CcP (Cyclone Peak). in new M.2 for 2015, it is used and serves as ISH UART and it's voltage is 1.8V.

W_DISABLE2# (pin 54 in M.2 2230 pinout, pin 63 in M.2 1216SD pinout) serves as HW RF kill for the Bluetooth® radio.
Asserting W_DISABLE2# signal will result in a complete shutdown of the Bluetooth® part. The result from the user perspective is similar to removing the Bluetooth® device from the laptop.

W_DISABLE2# characteristics

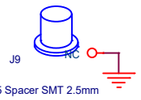
Internal pull-up resistor min 100 kOhm, max 200kOhm

VIL for asserting min 0V, max 0.6V

VIH for de-asserting min 1.26V, max 3.3V or float (not connected)

The recommendation is to use HW RF kill functionality by using a GPIO pin provided by the ACPI to turn on/off the radio of the Bluetooth® device.
BIOS shall implement ACPI function for HW RF-Kill implementation in the OS.
For more information, please refer to Intel document 559910, Intel Connectivity Platform BIOS Guidelines, Section 3.1.5.6, "BT RTD3 control."

SPACER for Key-E



Title	M.2 E (WiFi/BT)	
Size A3	Document Number <Doc>	Rev <RevCo
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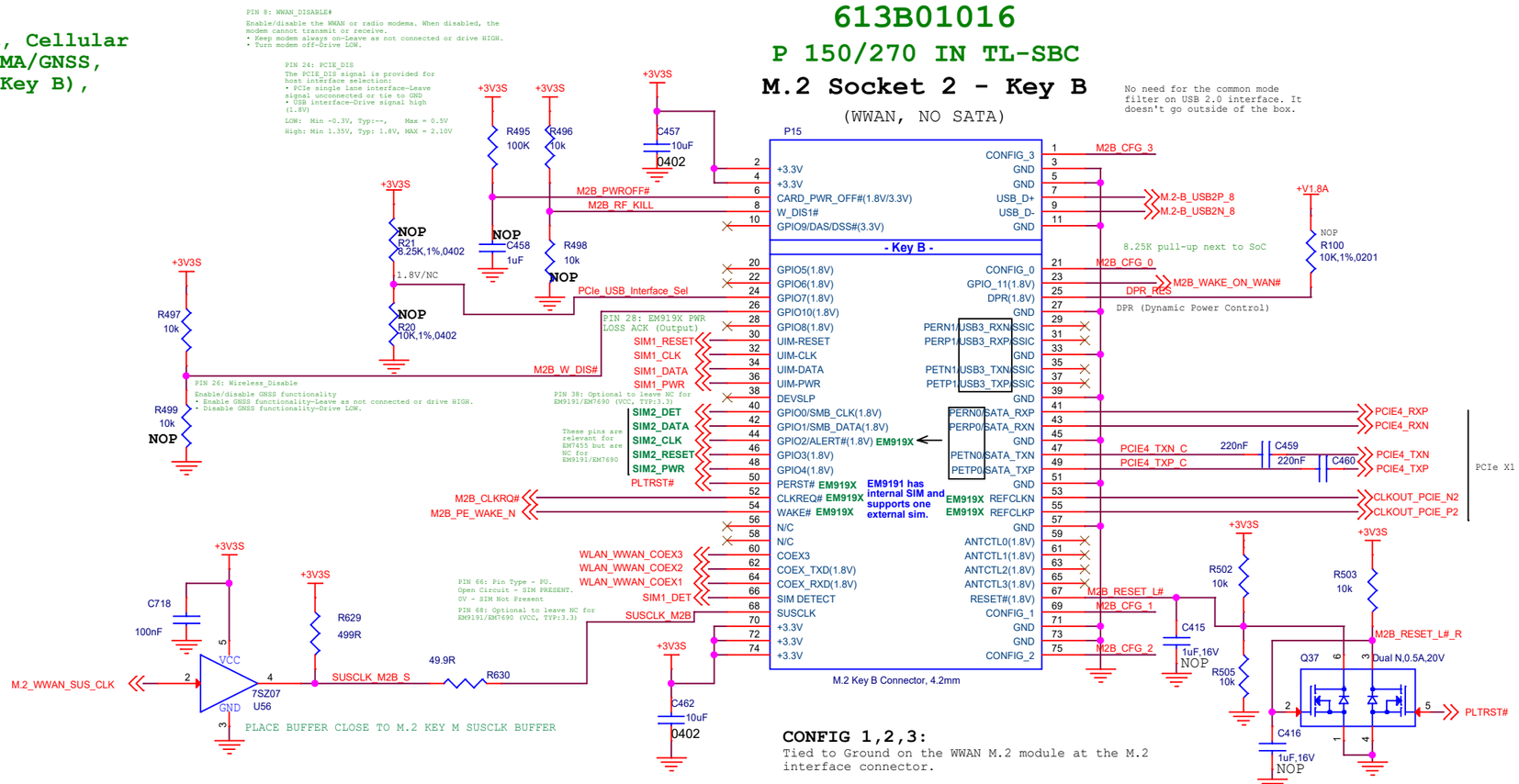
Communication Equipment, Cellular Modem, 5G/LTE/HSPA+/WCDMA/GNSS, Global-Band, M.2 3052 (Key B), Sierra EM9191

613B01016

P 150/270 IN TL-SBC

M.2 Socket 2 - Key B

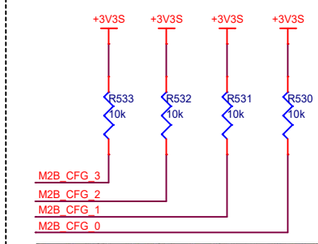
(WWAN, NO SATA)



CONFIG 1,2,3:
Tied to Ground on the WWAN M.2 module at the M.2 interface connector.

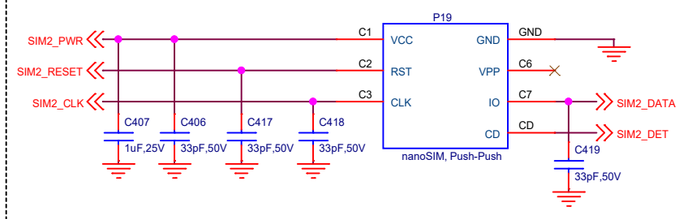
CONFIG 0:
This signal is not connected on the WWAN M.2 module.

M.2 CONFIG PINS

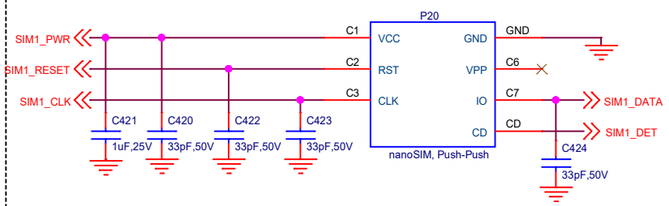


Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module type and main host interface
GND	GND	GND	GND	SSD-SATA
GND	NC	GND	GND	SSD-PCIe
NC	GND	GND	GND	WWAN-SSIC
NC	NC	NC	NC	No Module Present

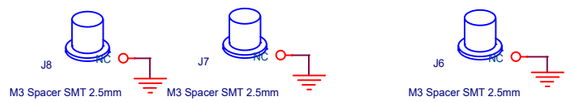
nanoSIM_2 with detect (w/o tray)



nanoSIM_1 with detect (w/o tray)



Spacers for Key-B & Key-M Heatsink



Title	M.2 B (WWAN)	
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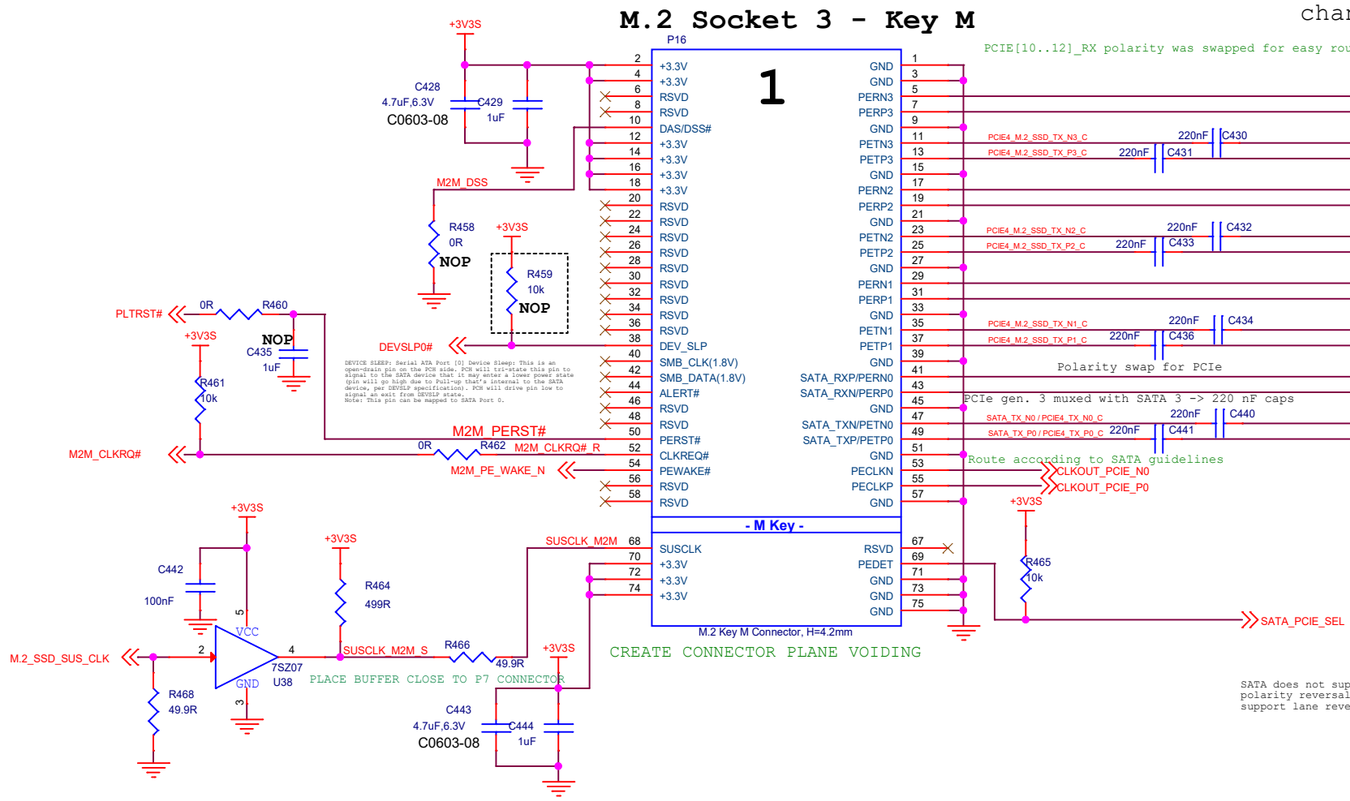
P 143/270 IN TL-SBC

980 PRO PCIe 4.0 NVMe M.2 250GB SSD

changed from H=4.2mm to H=6.7mm

changed from 182K06700S to 182K06706S

M.2 Socket 3 - Key M



Title	M.2 M (SSD)		
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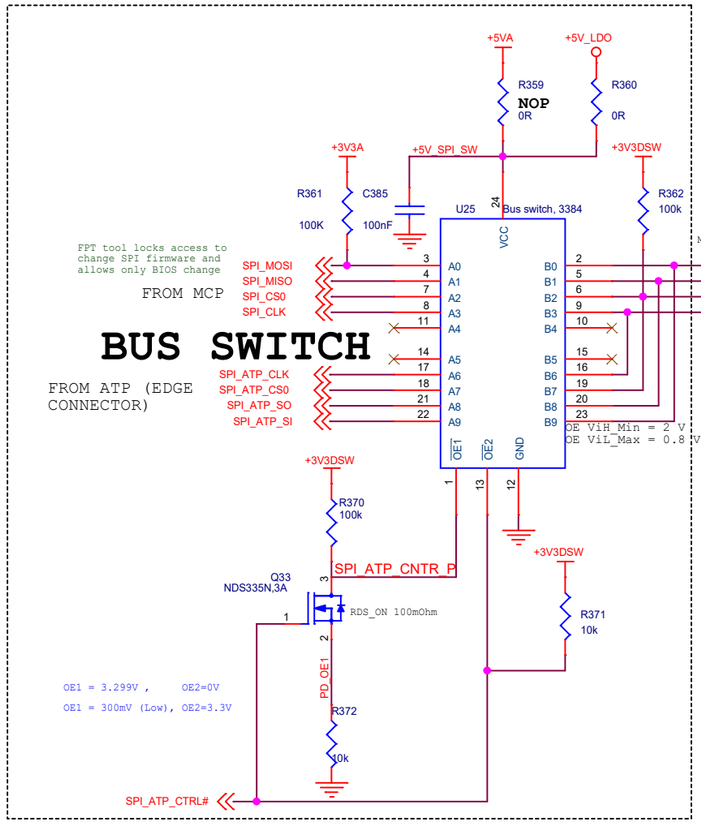
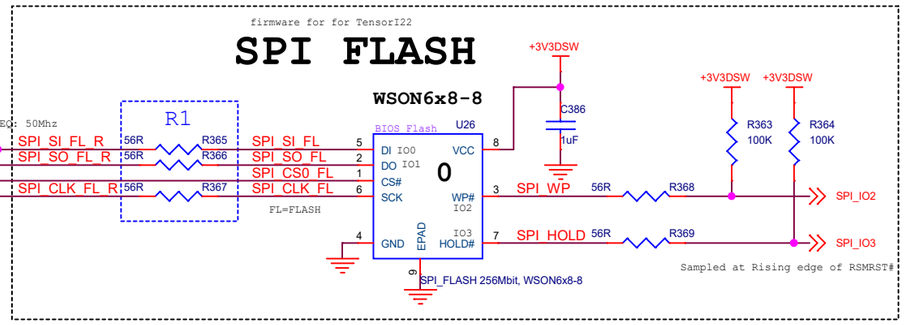
2-Load Branch MAF Topology (Master Attached Flash)

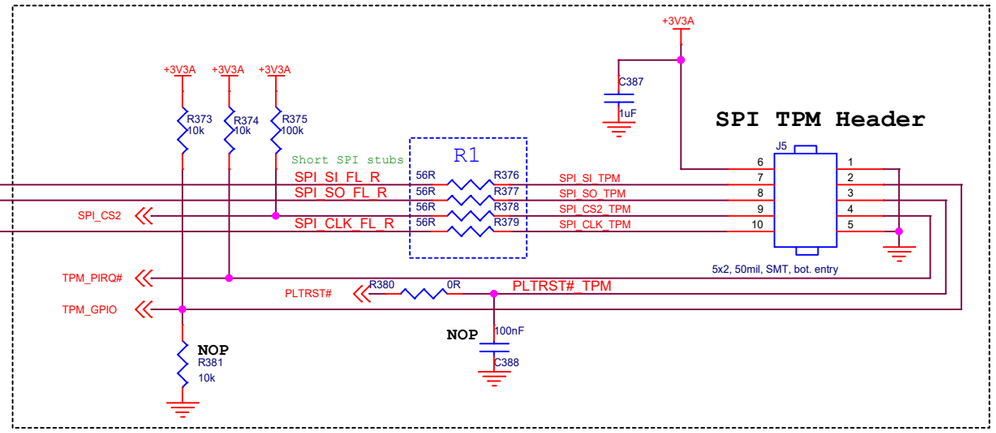
SPI_CLK & SPI_MOSI matched to within 500 mil
SPI_CLK & SPI_CS[0,1] matched to within 500 mil



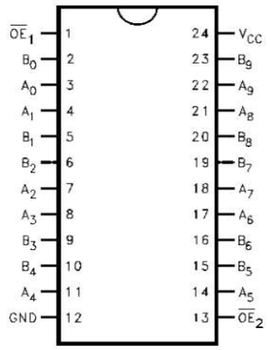
if SPI_ATP_CNTR# = 0V then SPI_ATP_CNTR_P = 3.299V
if SPI_ATP_CNTR# = 3.3V SPI_ATP_CNTR_P = 300mv < 0.8V (V_IL,MAX)



SPI_IO2 & SPI_IO3
External pull-up is required. Recommend 100 kohm if pulled up to 3.3 V or 75 kohm if pulled up to 1.8 V.
This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.



Connection Diagram



Truth Table

$\overline{OE}_1$	$\overline{OE}_2$	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

Title	SPI FLASH/TPM		
Size A3	Document Number <Doc>		Rev <RevC
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I2C GPIO I/O Expander

U39 Internal 100K PU are enabled by default

PCA9555

Address: 0x40

the RIBBON ID are inputs to the GPIO EXPANDER, by default, these pins are 1 (internal 100K PU), untill a ground is connected to some Ribbon ID pin in TRIP (on TEL Side)

Internal 100K PU are enabled by default
After power-up, the XRA1201 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled. The XRA1201P has the internal pull-up resistors enabled upon power-up in case it is necessary for the inputs to be in a known state.

I2C Mux

U40

PCA9518 I2C HUB

from master

Pull-Down

RN1 10K/8P4R

by default, the GPIO exapnder has internal pull up of 100K, which causes the EN pins to be 0.3V (becase of 10K pull down). 0.3 is lower than the ViL which is 0.5V.

SMB_CLK_1 | to Trip 1
EEPROM ADDRESS: 0x54

SMB_CLK_2 | to Trip 2
EEPROM ADDRESS: 0x54

SMB_CLK_EB | TO EB-TI22A (B2B)
EEPROM ADDRESS: 0x54
I210 Address: 0x49 (P.222)

EEPROM

U41 24C08 (1KB)

EEPROM ADDRESS: 0x54

There are TELS that are not supposed to work on certain TRIPS.

the BIOS reads what is written on each TEL's EEPROM and according to it , it knows which TEL is this and it decides whether to send a reset through PLTRST#_BYP_1 and PLTRST#_BYP_2.

The purpose of the reset is not freeze the system in case of mis-installing of TELS.

the RESET is sent only to the SPECIFIC TEL.

AND Gate: Reset Override - if you place an incorrect TEL that shouldn't work on specific TRIP, the BIOS should identify this (the address on TEL is sent back through GPIO EXP to BIOS and then BIOS initiates a reset using PLTRST#_BYP_1).

the GPIO EXP is like an EEPROM, it has a wide range of addresses, and we can change the value of each bit to 0 or 1.

EEPROM ADRESS ON ALL TELS ARE THE SAME (0x54) BUT DATA THAT SPECIFIES THE PURPOSE OF EACH TEL IS DIFFERENT.

Title	SMBus_MUX/GPIO_EXPANDER	
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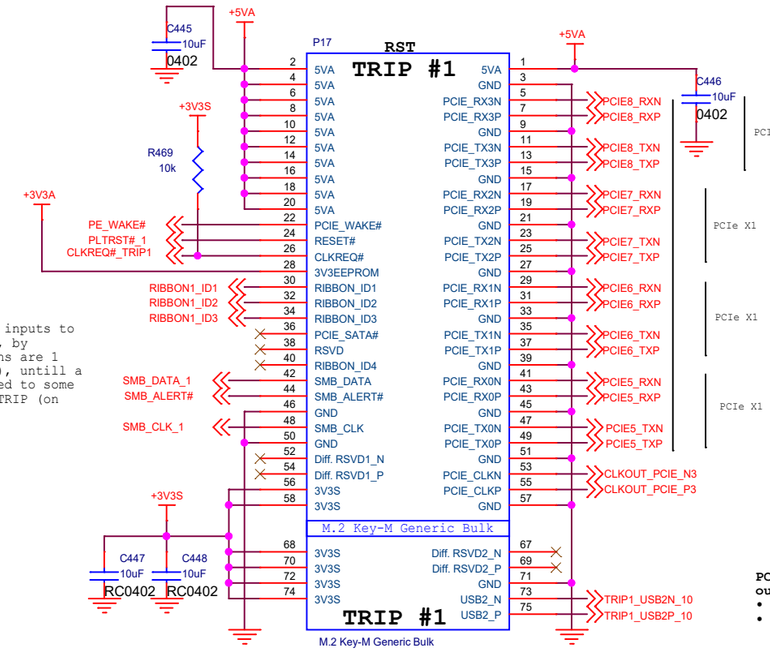
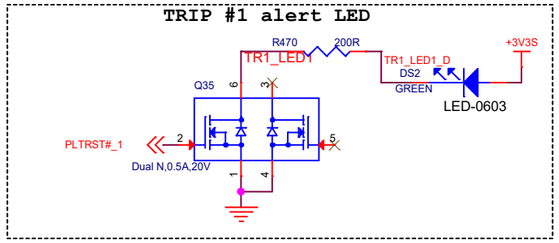


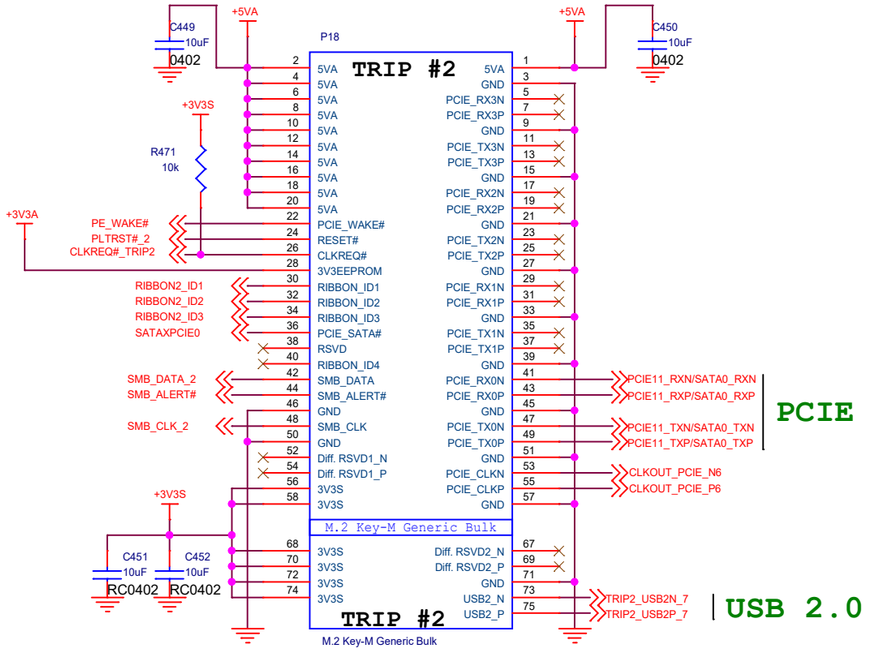
the RIBBON ID are inputs to the GPIO EXPANDER, by default, these pins are 1 (internal 100K PU), untill a ground is connected to some Ribbon ID pin in TRIP (on TEL Side)

The TX capacitors should be near the connector of the device (in TRIP case, on the TEL), and the RX capacitors will be on the device's PCB.
If the PCIe is for a chip which is on you board, both TX and RX capacitors should be located near the device IC.

PCIE-GEN3

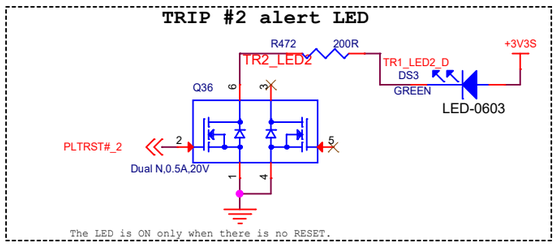


PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices
- **CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support**
- **CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support**



PCIE x1/SATA

USB 2.0



The LED is ON only when there is no RESET.

Title: TRIP 1&2			
Size: A3	Document Number: <Doc>		Rev: <RevCode>
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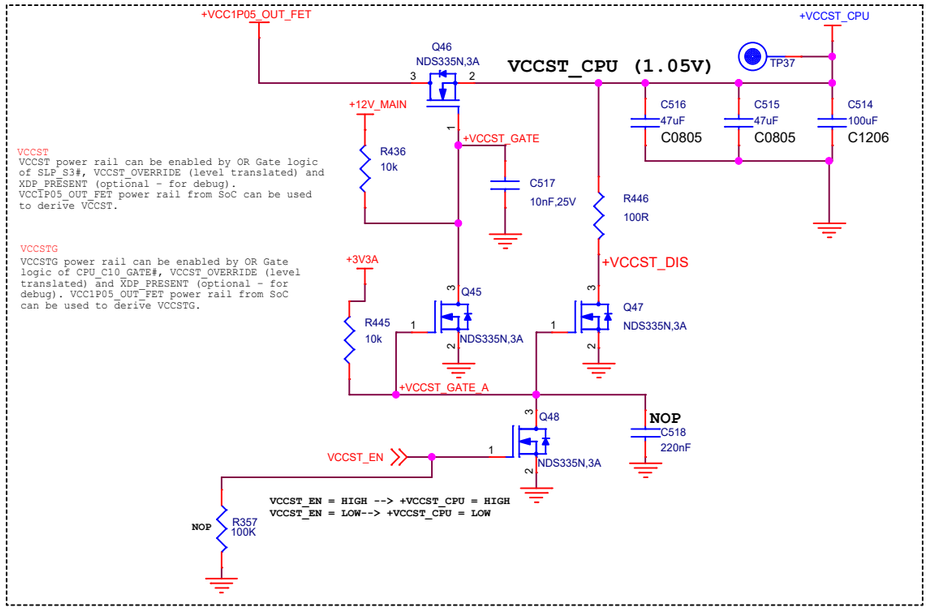
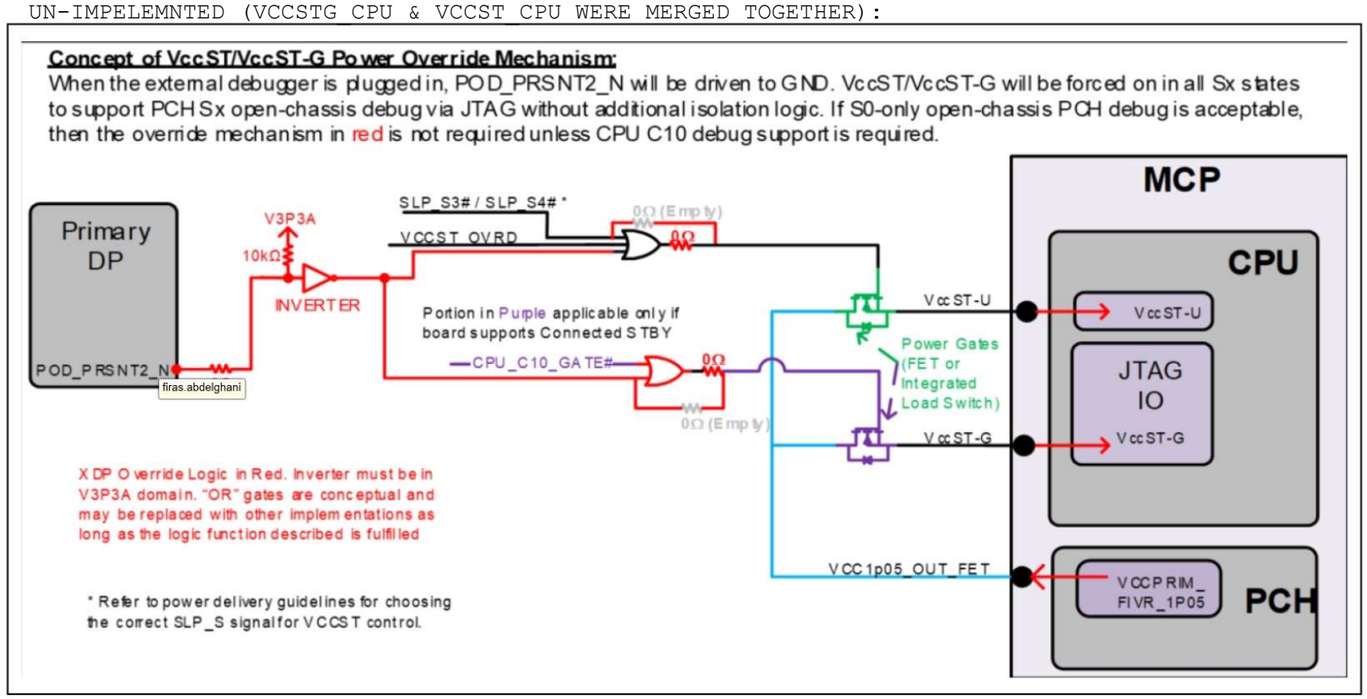


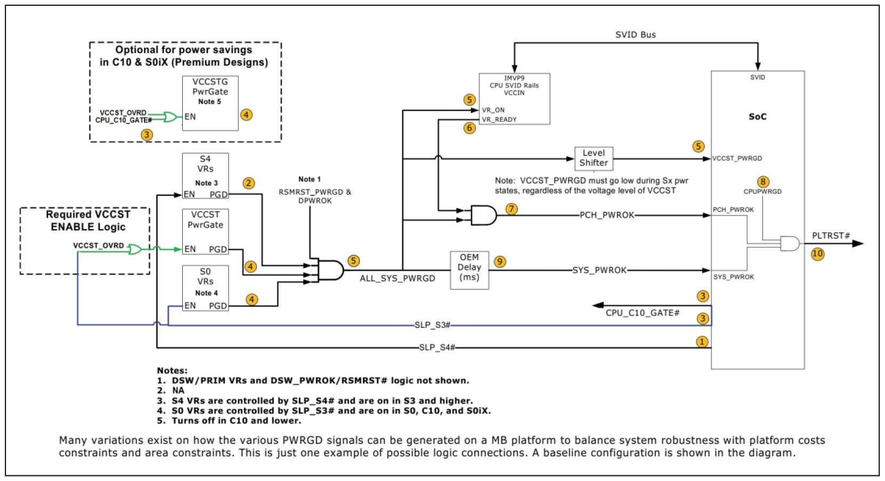
UN-IMPELEMNTED (VCCSTG_CPU & VCCST_CPU WERE MERGED TOGETHER):



IN VOLUME: VccSTG gated by SLP_S3#

IN Premium, VccSTG gated by {CPU_C10_GATE#}

Figure 247. Premium PWROK Generation Flow Diagram



Many variations exist on how the various PWRGD signals can be generated on a MB platform to balance system robustness with platform costs constraints and area constraints. This is just one example of possible logic connections. A baseline configuration is shown in the diagram.

Title	<Title>	
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