Tiger Lake UP3 Platform Reference Validation Platform (RVP)

User Guide

Revision 2.0

March 2021

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Contents

1 Introduction 12
1.1 Terminology 12
1.2 Reference Documents 13

2 High Level Overview 15
2.1 Tiger Lake UP3 15
2.1.1 Board Layout – Top View 16
2.1.2 Actual Board Snapshot – Top View 16
2.1.3 Board Layout – Bottom View 17
2.1.4 Actual Board Snapshot – Bottom View 18
2.1.5 IO Ports Board Snapshot - North Side View 18
2.1.6 IO Ports Board Snapshot - West Side View 19
2.1.7 IO Ports Board Snapshot - South Side View 19
2.1.8 MODPHY Mapping 20
2.2 Memory 23
2.2.1 TGL UP3 RVP - Memory Specification 23
2.2.2 Memory Topology 25
2.3 Display 26
2.3.1 TGL UP3 RVP - Display Mapping 26
2.4 Touch Panel and Touch Pad 27
2.4.1 TGL UP3 RVP Touch Panel/Pad 27
2.5 Thunderbolt™ Type C Interface 28
2.5.1 Type C Support 28
2.6 Storage 33
2.6.1 TGL UP3 RVP Storage Interfaces – High Level 33
2.7 Communications 34
2.7.1 Connectivity Overview 34
2.7.2 Connectivity Block Diagram 34
2.7.3 Connectivity – Modules Supported 35
2.8 Modem 35
2.8.1 Modem Block Diagram 35
2.9 Audio 36
2.9.1 TGL UP3 RVP Audio Block Diagram 36
2.9.2 Audio Overview 37
2.9.3 Board Layout – Top Audio HDR 40
2.10 Camera 40
2.10.1 Camera Support 40
2.10.2 TGL UP3 Camera Configuration Support 41
2.10.3 Fingerprint Sensor Block Diagram 43
2.11 Sensors 43
2.11.1 Sensors and Sensor AIC Block Diagram 43
2.11.2 LPSS I^2C Devices Mapping 44
2.11.3 LPSS UART and LPSS GSPI Mapping 44
2.11.4 Serial Interface Devices Mapping 45
2.11.5 ISH Interface Mapping 46
2.12 Embedded Controller 46
2.12.1 Embedded Controller Block Diagram 47
2.12.2 Master Attached Flash (MAF) Sharing 47
2.12.3 Slave Attached Flash Sharing (SAF) 48

2.13 Debug and Validation 48
2.13.1 Debug Technologies 48
2.13.2 Traditional XDP Support on TGL RVP 49
2.13.3 Additional Tools and Cables 49
2.13.4 Four Wire Solution with Type A 49
2.14 Power Delivery Implementation Details 50
2.14.1 TGL UP3 RVP Power Sources 50
2.14.2 TGL UP3 RVP Key PD Sub-systems 51
2.14.3 TGL UP3 RVP Power Map 52
2.14.4 TGL UP3 RVP Voltage Levels of Critical Rails 56
2.14.5 System State Overview 56
2.14.6 TGL UP3 RVP Power States Map 57
2.14.7 TGL UP3 RVP Sequencing Details 57
2.14.8 TGL UP3 RVP Sequencing Block Diagram 58
2.14.9 TGL UP3 RVP Sequencing Block Diagram (Cont.) 59
2.14.10 TGL UP3 RVP Power Source Priority 59
2.15 Quick Start 59
2.15.1 Board Bring Up Steps 60
2.15.2 SF600 Programming 61
2.16 TGL UP3 A0 - Heatsink Retention Solution 62
2.16.1 Mechanical Parts Overview 62
2.16.2 Required Tools and Consumables 62
2.16.3 PIN-1 Indicators 63
2.16.4 TGL UP3 Interposer Hardware Installation 64
2.16.5 Cooper Shim Installation 66
2.16.6 Heads Up 67
2.16.7 Troubleshooting 67
2.17 TGL UP3 270 um Rework Strategy 68
2.17.1 Package Identification 68
2.17.2 TGL UP3 Heatsink/Retention Strategy: Upgrade Kits 68
2.17.3 TGL UP3 Thermal Tool Strategy 69
2.17.4 TGL UP3 270 Risks 70
2.18 BackUp 70
2.18.1 EC Error Code Indication 70
2.18.2 Jumpers on TGL UP3 DDR4 RVP 71
2.18.3 TGL UP3 DDR4 RVP LED Indication 72
2.18.4 CPU and PCH Straps 73
2.18.5 TGL UP3 RVP PCIe* Slots 74
2.18.6 CRD Camera AOB Pinout 74
2.18.7 SPI through Dediprog SF600 75

3 RVP Reworks 78
3.1 Mandatory Reworks 78
3.1.1 Rework to Enable 3.3V SPI Voltage Selection 78
3.1.2 Rework for BOOT HALT to Sample Correctly 79
3.1.3 Rework to Enable ES-2 Codec on TGL UP3 DDR4 RVP 80
3.1.4 Rework to VCCIN and VCCIN_AUX VR in TGL UP3 LP4x 87
3.1.5 Rework for VDDQ_TX Power Good Isolation in TGL UP3 LP5 RVP 90
3.1.6 Rework for AUX VID Signal Isolation from VCCST and VCCSTG Rail Enable Logic in TGL UP3 RVP 91
3.1.7 Rework to Power on TGL UP3 LP4x EXS ERB with TGL UP3 and EXS Silicon 94
3.1.8 Rework for DCLL Change in TGL UP3 Design 97
3.1.9 Rework to Enable SPI QUAD MODE Functionality at 50 MHz 100

3.2 Featured Rework 108
3.2.1 Rework to Enable SoundWire* in ALC711 108
3.2.2 Rework to Enable SoundWire* on AIOC for ALC1308 111
3.2.3 Rework to Enable SoundWire* on AIOC for ALC711 114
3.2.4 Rework to Enable I2S on RVP for ALC1308 117
3.2.5 Rework to Enable I2S on AIOC for ALC1308 121
3.2.6 Rework to Enable BBR Bypass Mode on TCP2 Port of TGL UP3 DDR4 RVP 123
3.2.7 Rework to Enable DP++ Connector (Standard Size) on Dekel PHY-Type C Port 4 on TGL UP3 DDR4 RVP 129
3.2.8 Rework to Enable PCH Debug Support on PCH MIPI60 Port on TGL UP3 RVP 132
3.2.9 Rework to Enable USB-based BT® on TGL UP3 RVP 136
3.2.10 Rework to Enable SATA Port Connected to SATA Connector on RVP 137
3.2.11 Rework to Enable PCIe* Gen4 on x4DT Slot 140
3.2.12 Rework to Enable THC SPI Touch Panel Connection on TGL RVP . 149
3.2.13 Rework to Enable HDA in ALC711 in TGL UP3 DDR4 Board 156
3.2.14 Rework to Enable HDMI with CRLS on TGL UP3 DDR4 159
3.2.15 Rework for HDMI (with Retimer) on TCP0 Port 164
3.2.16 Rework to Enable HDMI (Vertical) with CRLS on TCP3 Port 167
3.2.17 Rework to Enable ALC1013 (AMP) 170
3.2.18 Rework to Get Correct PWM Frequency and Output from ALC1308 (Amplifier) 173
3.2.19 Rework to Enable eDP on DDIB Combo Port 175
3.2.20 Rework to Enable Time-Sensitive Networking (TSN) Ethernet Controller 180
3.2.21 MAF Configuration to SAF Rework on TGL UP3 RVP 184
3.2.22 Rework to Change MAF Configuration to G3 on TGL UP3 RVP 191
3.2.23 Rework to Enable Elixir VCCST and VCCSTG Gates 196
3.2.24 Rework to Enable FIVR External Bypass on TGL UP3 DDR4 198
3.2.25 Rework to Enable EC MECC Connector for TGL UP3 201
3.2.26 Rework for Vmin Active Protection (VAP) Enable Function and Improve PROCHOT Drive Strength 214
3.2.27 Rework to Enable Foxville card on TGL UP3 220
3.2.28 Rework to Enable Virtual Wire OC Indication to PCH through EC in TGL 223
3.2.29 Rework to Enable MIPI Connector on DDIA Combo Port on TGL UP3 LPDDR5 226
3.2.30 Rework to enable_INTRUDER_functionality on TGL_UP3 230
3.2.31 Rework to Enable Mini HDMI on TGL UP3 LP5 Board 232
3.3 Optional Reworks 235
3.3.1 Rework to Enable DeepSx Exit Flow in MAF Mode on TGL UP3 RVP 235
3.3.2 Rework to Enable SPI QUAD MODE Functionality at 50 MHz 236
3.3.3 Rework to Change the VBATA Caps to Higher Voltage Rating 238
3.3.4 Rework to Enable TBT™ Compliance on iTBT Ports on RVP 239
3.3.5 Rework to Isolate External VNN and V1.05A VR Power Good 246
3.3.6 Rework to Optimize the EC power in TGL UP3 DDR4 250
3.3.7 Rework to Reduce PCH VCCPRIM_1P8 Power from GPPC_B14 GPIO 256
3.3.8 Rework to Avoid EYE Diagram Failure on TGL UP3 DDIB HDMI ... 259
3.3.9 Rework to Change the ILIM on the USB-C Source Switch for PD Compliance. 261

3.3.10 Rework to Enable M.2 WWAN 7560-R+ Module on TGL UP3 Boards. 263

Figures

Figure 2-1. TGL UP3 Block Diagram 15
Figure 3-1. Schematic Snapshot 79
Figure 3-2. Layout Snapshot (Top Layer) 79
Figure 3-3. Schematic Snapshot 80
Figure 3-4. Layout Snapshot (Top Layer) 80
Figure 3-5. Schematic Snapshot TGL UP3 DDR4 RVP 82
Figure 3-6. Layout Snapshot (Top Layer) TGL UP3 DDR4 RVP 84
Figure 3-7. Layout Snapshot (Bottom Layer) 86
Figure 3-8. Layout Snapshot (Top Layer) 86
Figure 3-9. Layout Snapshot (Bottom Layer) 87
Figure 3-10. Schematic Snapshot TGL UP3 LPDDR4X RVP 88
Figure 3-11. Layout Snapshot (Top Layer) 89
Figure 3-12. Schematic Snapshot 90
Figure 3-13. Layout Snapshot (Bottom Layer) 91
Figure 3-14. Schematic Snapshot 92
Figure 3-15. Layout Snapshot (Top Layer) 93
Figure 3-16. Schematic Snapshot 95
Figure 3-17. Layout Snapshot (Top Layer) 96
Figure 3-18. Layout Snapshot (Bottom Layer) 97
Figure 3-19. Schematic Snapshot 98
Figure 3-20. Layout Snapshot (Top Layer) 99
Figure 3-21. Schematic Snapshot: TGL UP3 DDR4 103
Figure 3-22. Schematic Snapshot: TGL UP3 LP4X 104
Figure 3-23. Schematic Snapshot: TGL UP3 LP5 105
Figure 3-24. Layout Snapshot (Top Layer): TGL UP3 DDR4 106
Figure 3-25. Layout Snapshot (Bottom Layer): TGL UP3 DDR4 106
Figure 3-26. Layout Snapshot (Top Layer): TGL UP3 LP4X 107
Figure 3-27. Layout Snapshot (Bottom Layer): TGL UP3 LP4X 107
Figure 3-28. Layout Snapshot (Top Layer): TGL UP3 LP5 108
Figure 3-29. Layout Snapshot (Bottom Layer): TGL UP3 LP5 108
Figure 3-30. Schematic Snapshot 109
Figure 3-31. Layout Snapshot (Top Layer) 110
Figure 3-32. Layout Snapshot (Bottom Layer) 111
Figure 3-33. Schematic Snapshot 112
Figure 3-34. Layout Snapshot (Top Layer) 113
Figure 3-35. Schematic Snapshot 115
Figure 3-36. Layout Snapshot (Top Layer) 116
Figure 3-37. Schematic Snapshot 119
Figure 3-38. Layout Snapshot (Top Layer) 120
Figure 3-39. Schematic Snapshot 122
Figure 3-40. Layout Snapshot (Top Layer) 122
Figure 3-41. Schematic Snapshot 125
Figure 3-42. Layout Snapshot (Top Layer) 128
Figure 3-43. Schematic Snapshot 131
Figure 3-44. Layout Snapshot (Top Layer) 131
Figure 3-45. Schematic Snapshot 134
Figure 3-46. Layout Snapshot (Top Layer) 135

Figure 3-47. Layout Snapshot (Bottom Layer) 136
Figure 3-48. Schematic Snapshot 137
Figure 3-49. Layout Snapshot (Top Layer) 137
Figure 3-50. Schematic Snapshot 139
Figure 3-51. Layout Snapshot (Top Layer) 140
Figure 3-52. Schematic Snapshot 146
Figure 3-53. Layout Snapshot (Top Layer) 147
Figure 3-54. Layout Snapshot (Bottom Layer) 149
Figure 3-55. Schematic Snapshot 151
Figure 3-56. Layout Snapshot (Top Layer) 152
Figure 3-57. Layout Snapshot (Bottom Layer) 152
Figure 3-58. Schematic Snapshot 153
Figure 3-59. Layout Snapshot (Top Layer) 154
Figure 3-60. Layout Snapshot (Bottom Layer) 155
Figure 3-61. Schematic Snapshot 157
Figure 3-62. Layout Snapshot (Top Layer) 158
Figure 3-63. Layout Snapshot (Bottom Layer) 159
Figure 3-64. Schematic Snapshot 161
Figure 3-65. Layout Snapshot (Top Layer) 163
Figure 3-66. Layout Snapshot (Bottom Layer) 163
Figure 3-67. Schematic Snapshot 165
Figure 3-68. Layout Snapshot (Top Layer) 166
Figure 3-69. Layout Snapshot (Bottom Layer) 167
Figure 3-70. Schematic Snapshot 169
Figure 3-71. Layout Snapshot (Top Layer) 169
Figure 3-72. Layout Snapshot (Bottom Layer) 170
Figure 3-73. Schematic Snapshot 171
Figure 3-74. Layout Snapshot (Top Layer) 172
Figure 3-75. Schematic Snapshot 174
Figure 3-76. Layout Snapshot (Bottom Layer) 175
Figure 3-77. Schematic Snapshot 178
Figure 3-78. Layout Snapshot (Top Layer) 179
Figure 3-79. Layout Snapshot (Bottom Layer) 179
Figure 3-80. Schematic Snapshot 181
Figure 3-81. Layout Snapshot (Top Layer) 183
Figure 3-82. Schematic Snapshot 185
Figure 3-83. Layout Snapshot (Bottom Layer) 188
Figure 3-84. Layout Snapshot (Top Layer) 189
Figure 3-85. Schematic Snapshot 192
Figure 3-86. Layout Snapshot (Bottom Layer) (Flip View) 194
Figure 3-87. Layout Snapshot (Top Layer) 195
Figure 3-88. Schematic Snapshot 197
Figure 3-89. Layout Snapshot (Top Layer) 197
Figure 3-90. Schematic Snapshot 200
Figure 3-91. Layout Snapshot (Bottom Layer) 201
Figure 3-92. Schematic Snapshot 203
Figure 3-93. Layout Snapshot (Top Layer) 209
Figure 3-94. Layout Snapshot (Bottom Layer) 213
Figure 3-95. Schematic Snapshot 216
Figure 3-96. Layout Snapshot 217
Figure 3-97. Schematic Snapshot 222
Figure 3-98. Layout Snapshot (Top Layer) 222
Figure 3-99. Layout Snapshot (Bottom Layer) 223
Figure 3-100. Schematic Snapshot..... 224
Figure 3-101. Schematic Snapshot..... 225

Figure 3-102. Layout Snapshot (Top Layer) 225
Figure 3-103. Layout Snapshot (Top Layer) 226
Figure 3-104. Schematic Snapshot..... 227
Figure 3-105. Layout Snapshot (Top Layer) 229
Figure 3-106. Layout Snapshot (Bottom Layer) 229
Figure 3-107. Schematic Snapshot..... 231
Figure 3-108. Layout Snapshot (Top Layer) 231
Figure 3-109. Layout Snapshot (Top Layer) 232
Figure 3-110. Schematic Snapshot..... 233
Figure 3-111. Layout Snapshot (Top Layer) 234
Figure 3-112. Layout Snapshot (Bottom Layer) 234
Figure 3-113. Schematic Snapshot..... 235
Figure 3-114. Layout Snapshot (Top Layer) 236
Figure 3-115. Schematic Snapshot..... 237
Figure 3-116. Layout Snapshot (Top Layer) 237
Figure 3-117. Schematic Snapshot: TGL UP3 DDR4 and TGL UP3 LP4X..... 238
Figure 3-118. Layout Snapshot (Top Layer) 239
Figure 3-119. Layout Snapshot (Top Layer) 239
Figure 3-120. Schematic Snapshot: TGL UP3 DDR4 240
Figure 3-121. Schematic Snapshot: TGL UP3 LP4X..... 242
Figure 3-122. Layout Snapshot (Top Layer) 244
Figure 3-123. Layout Snapshot (Bottom Layer) 244
Figure 3-124. Layout Snapshot (Top Layer) 245
Figure 3-125. Layout Snapshot (Bottom Layer) 245
Figure 3-126. Schematic Snapshot..... 247
Figure 3-127. Layout Snapshot..... 249
Figure 3-128. Schematic Snapshot: TGL UP3 DDR4 251
Figure 3-129. Schematic Snapshot: TGL UP3 LPDDR4X 252
Figure 3-130. Layout Snapshot (Top Layer): TGL UP3 DDR4 253
Figure 3-131. Layout Snapshot (Bottom Layer): TGL UP3 DDR4 254
Figure 3-132. Layout Snapshot (Top Layer): TGL UP3 LPDDR4X 255
Figure 3-133. Layout Snapshot (Bottom Layer): TGL UP3 LPDDR4X 256
Figure 3-134. Schematic Snapshot: TGL UP3 DDR4 257
Figure 3-135. Schematic Snapshot: TGL UP3 LPDDR4X 258
Figure 3-136. Layout Snapshot (Bottom Layer): TGL UP3 DDR4 258
Figure 3-137. Layout Snapshot (Top Layer): TGL UP3 LPDDR4X 259
Figure 3-138. Schematic Snapshot: TGL UP3 DDR4 260
Figure 3-139. Layout Snapshot (Bottom Layer): TGL UP3 DDR4 260
Figure 3-140. Schematic Snapshot: TGL UP3 DDR4 RVP 262
Figure 3-141. Layout Snapshot (Top Layer): TGL UP3 DDR4 RVP..... 262
Figure 3-142. Layout Snapshot (Bottom Layer): TGL UP3 DDR4 263
Figure 3-143. Schematic Snapshot: TGL UP3 DDR4 RVP 264
Figure 3-144. Layout Snapshot (Top Layer): TGL UP3 DDR4 RVP..... 264

Tables

Table 2-1. TGL UP3 42 RVP's MPHY Allocation 20
Table 2-2. TGL UP3 RVP M.2 2230 Module Support 35
Table 3-1. Rework Details..... 78
Table 3-2. Rework Details..... 80
Table 3-3. Rework Details: TGL UP3 DDR4 RVP 81
Table 3-4. Rework Details..... 88
Table 3-5. Rework Details..... 90

Table 3-6. Rework Details 91
Table 3-7. Rework Details: TGL UP3 LP4X RVP 94
Table 3-8. Rework Details: TGL UP3 DDR4 97
Table 3-9. Rework Details: TGL UP3 LP4X 97
Table 3-10. Rework Details: TGL UP3 LP5 98
Table 3-11. Rework Details: TGL UP3 DDR4 101
Table 3-12. Rework Details: TGL UP3 LP4X 101
Table 3-13. Rework Details: TGL UP3 LP5 102
Table 3-14. Rework Details 109
Table 3-15. Rework Details 112
Table 3-16. Rework Details 114
Table 3-17. Rework Details 118
Table 3-18. Reference Designator Comparison 118
Table 3-19. Rework Details 121
Table 3-20. Rework Details 124
Table 3-21. Rework Details 130
Table 3-22. Rework Details 132
Table 3-23. Rework Details 136
Table 3-24. Rework Details 138
Table 3-25. Rework Details 141
Table 3-26. Reference Designator Comparison Table 143
Table 3-27. Rework Details 150
Table 3-28. Rework Details 153
Table 3-29. Rework Details 156
Table 3-30. Reference Designator comparison table 156
Table 3-31. Rework Details 159
Table 3-32. Rework Details 164
Table 3-33. Rework Details 168
Table 3-34. Rework Details 171
Table 3-35. Rework Details 173
Table 3-36. Rework Details 176
Table 3-37. Reference Designator Comparison 176
Table 3-38. Rework Details 180
Table 3-39. Rework Details 184
Table 3-40. Reference Designator Comparison 185
Table 3-41. Rework Details 191
Table 3-42. Reference Designator Comparison 192
Table 3-43. Rework Details 196
Table 3-44. Rework Details 198
Table 3-45. Rework Details 199
Table 3-46. Rework Details 202
Table 3-47. Rework Details 203
Table 3-48. Rework Details: TGL UP3 DDR4 215
Table 3-49. Rework Details: TGL UP3 LPDDR4X 215
Table 3-50. Rework Details: TGL UP3 LPDDR5 216
Table 3-51. Rework Details: TGL UP3 DDR4 RVP 220
Table 3-52. Rework Details: TGL UP3 LP4x RVP 221
Table 3-53. Reference Designator Comparison 221
Table 3-54. Rework Details: TGL UP3 DDR4 RVP 224
Table 3-55. Rework Details: TGL UP3 LP4X RVP 224
Table 3-56. Reference Designator Comparison 224
Table 3-57. Rework Details: TGL UP3 LPDDR5 ERB 226
Table 3-58. Rework Details: TGL UP3 DDR4 and LP4 RVP 230
Table 3-59. Rework Details: TGL UP3 LP5 RVP 232
Table 3-60. Rework Details 235

Table 3-61. Rework Details 237
Table 3-62. Rework Details: TGL UP3 DDR4 and TGL UP3 LP4X 238
Table 3-63. Rework Details: TGL UP3 DDR4 240
Table 3-64. Rework Details: TGL UP3 LP4X 240
Table 3-65. Rework Details: 246
Table 3-66. Rework Details: TGL UP3 DDR4 250
Table 3-67. Rework Details: TGL UP3 LPDDR4X 251
Table 3-68. Rework Details: TGL UP3 DDR4 256
Table 3-69. Rework Details: TGL UP3 LPDDR4X 257
Table 3-70. Rework Details: TGL UP3 DDR4 259
Table 3-71. Rework Details: TGL UP3 DDR4 RVP 261
Table 3-72. Reference Designator Comparison 263
Table 3-73. Rework Details: TGL UP3 DDR4 RVP 264
Table 3-74. Reference Designator Comparison 265

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Revision History

Document Number	Revision Number	Description	Revision Date
612924	0.5	• Initial release **NOTE:** TGL UP3 RVP feature set is added in next revision of User Guide.	June 2019
	0.6	• Added mandatory reworks (Sections 3.1.5 to 3.1.6) • Added featured reworks (Sections 3.2.19 to 3.2.23)	July 2019
	0.7	• Added Section 2 "High level RVP overview"	September 2019
	0.8	• Added Section 3.2.24 • Added Feature Reworks in Section 3.2.25 and 3.2.26 and Optional Rework in Section 3.3.2	December 2019
	0.9	• Added Feature Rework in Section 3.2.27 and 3.2.28, • Mandatory Rework in Section 3.1.7, 3.1.8,and 3.1.9 • Optional Rework in Section 3.3.3, 3.3.4, 3.3.5, 3.3.7 and 3.3.8	May 2020
	1.0	• Added Feature Rework in Section 3.2.29 and Section 3.2.30.	August 2020
	1.1	• Added Feature Rework in Section 3.2.31	September 2020
	1.2	• Updated Feature Reworks in Section 3.2.4, 3.2.6, 3.2.7, 3.2.8, 3.2.11, 3.2.13, 3.2.15, 3.2.19, 3.2.21, 3.2.22, 3.2.24, 3.2.25, 3.2.27 and 3.2.28	November 2020
	2.0	• Added Section 3.3.9 and Section 3.3.10	March 2021

NOTES:

1. For all references in this training document for TGL U and TGL Y, refer to below naming guidelines for future use.
   a. The Tiger Lake U processor line is now named to Tiger Lake UP3 or TGL UP3.
   b. The Tiger Lake Y processor line is now named to Tiger Lake UP4 or TGL UP4.
2. Refer to Tiger Lake Platform Component List Technical Advisory (#607273) for part numbers corresponding to IPN mentioned in the document

§§

1 Introduction

This document describes the typical hardware set-up procedures, features, and use of Tiger Lake-UP3 DDR4, LPDDR4x, and LPDDR5 Platform RVP. This document must be read in its entirety, with both the schematic and RVP alongside (recommended), prior to powering ON the RVP.

1.1 Terminology

Term	Description
ACPI	Advanced Configuration Power Interface
AIC	Add-in-Card
BGA	Ball Grid Array
BIOS	Basic Input / Output System
TGL	Tiger Lake
CMC	Common Mode Choke
DDR	Double Data Rate
DMI	Direct Media Interface
EDP	Embedded Display Port
eMMC	Embedded Multi Media Card
ESD	Electrostatic Discharge
eSPI	Enhanced Serial Peripheral Interface
FIR	Fast Infra-Red
GPIO	General Purpose Input Output
GSPI	Generic Serial Peripheral Interface
PCH	Platform Controller Hub
IDE	Integrated Device Electronics
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
KBC	Keyboard Controller
LAN	Local Area Network
LED	Light Emitting Diode
MCP	Multi-Chip Package
FCIM	Full Clock Integration Mode
MDC	Mobile Daughter Card
OS	Operating System
PCB	Printed Circuit Board

Term	Description
PCI	Peripheral Control Interface
PCIe*	PCI Express*
PCH	Platform Control Hub
PEG*	PCI Express* Graphics
PLL	Phase Lock Loop
PGA	Pin Grid Array
RTC	Real Time Clock
SATA	Serial AT Attachment
SDVO	Serial Digital Video Output
SIO	Super Input Output
SMC	System Management Controller
SODIMM	Small Outline Dual In-line Memory Module
TCPM	Type C Policy Manager
UART	Universal Asynchronous Receiver/Transmitter
UFS	Universal Flash Storage
USB	Universal Serial Bus
VGA	Video Graphics Array
VR	Voltage Regulator
EC	Embedded Controller
XDP	Extended Debug Port

1.2 Reference Documents

Document Number	Document Title
575683	Tiger Lake Processor External Design Specification Volume 1 of 2
575681	Tiger Lake Processor External Design Specification Volume 2a of 2
576591	Intel® 500 Series Chipset Family On-Package Platform Controller Hub External Design Specification, Volume 1 of 2
575857	Intel® 500 Series Chipset Family On-Package Platform Controller Hub External Design Specification, Volume 2 of 2
607038	Intel® 500 Series Chipset Family On-Package PCH GPIO Implementation Summary
604917	Tiger Lake UP3 4+2 Processor Line BGA Package Ballout Mechanical Specification
607872	Tiger Lake UP3/UP4 Platform Design Guide

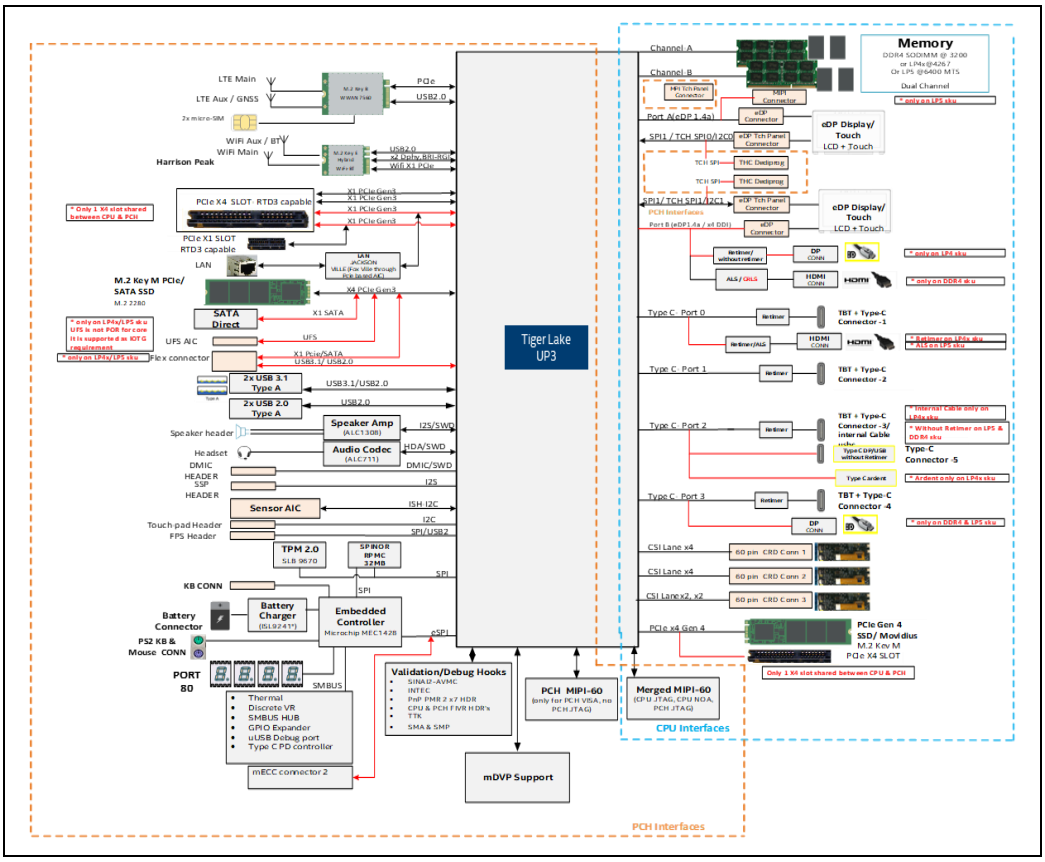
610161	Tiger Lake UP3 UP4 Intel Platform Design Studio
607873	Tiger Lake Mobile Platform Thermal and Mechanical Design Guide
609003	Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit
612304	Tiger lake UP3 LPDDR4x Reference Validation Platform Technical Documentation Kit
613798	Tiger Lake UP3 LPDDR5 Reference Validation Platform Technical Documentation Kit
612924	Tiger Lake UP3 Platform Reference Validation Platform (RVP) User Guide
609182	Tiger Lake UP3 LPDDR4/4x Advanced Enabling Platform (AEP) Technical Documentation Kit
613217	Tiger Lake UP3/UP4 Platform System Memory Interface Technical White Paper

§§

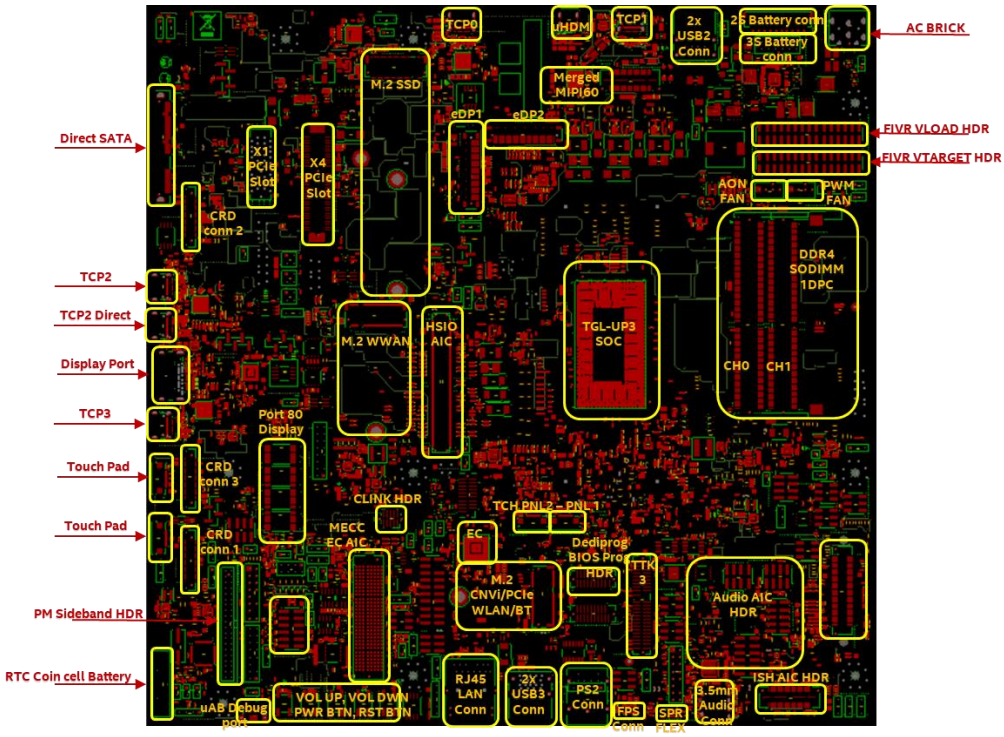
2 High Level Overview

2.1 Tiger Lake UP3

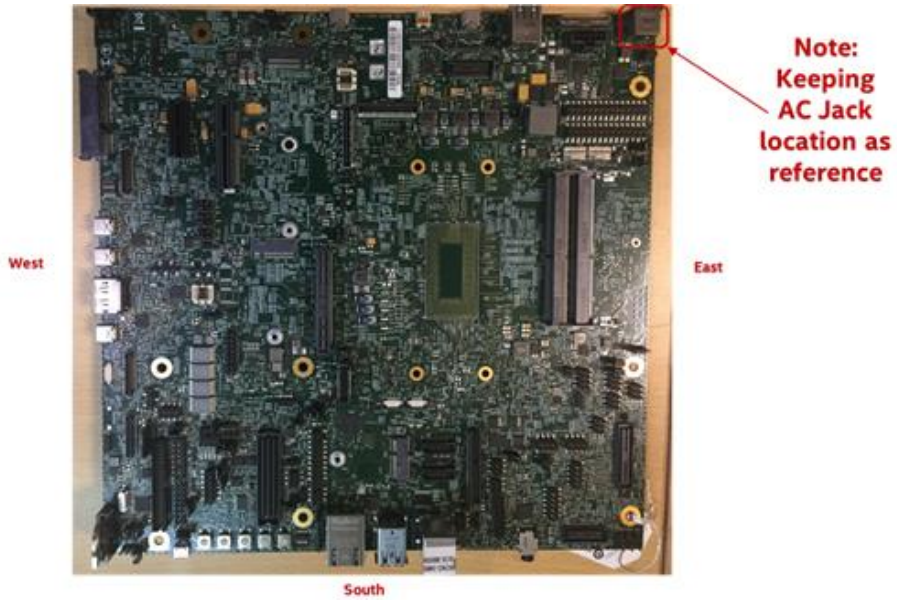
Figure 2-1. TGL UP3 Block Diagram



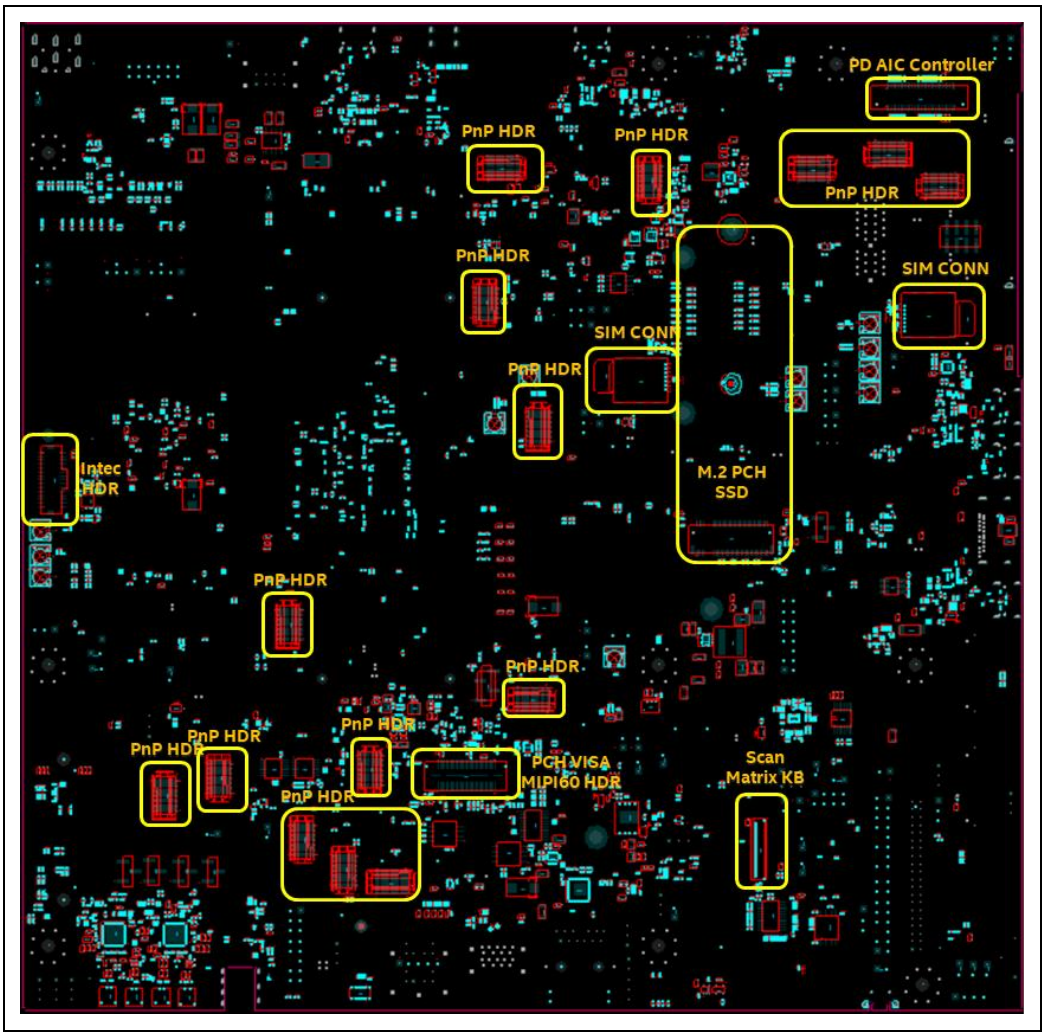
2.1.1 Board Layout – Top View



2.1.2 Actual Board Snapshot – Top View

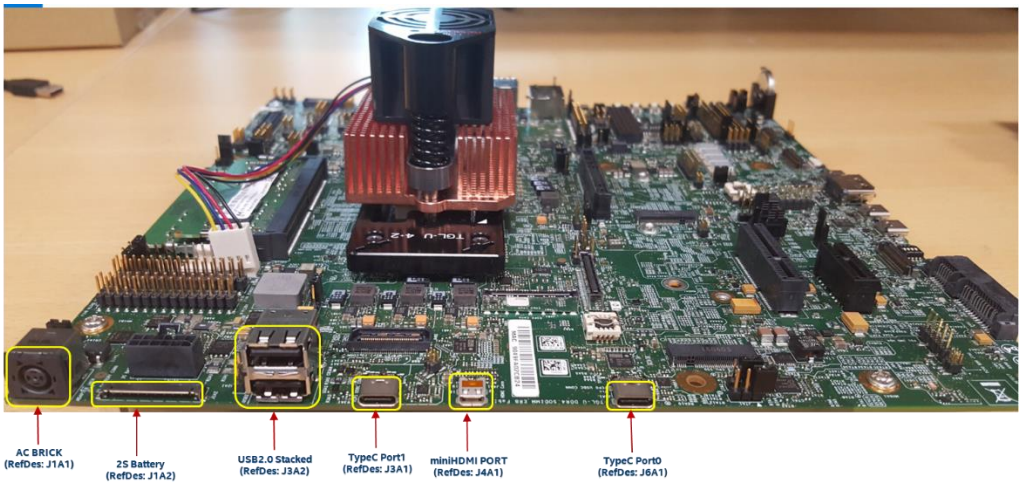


2.1.3 Board Layout – Bottom View

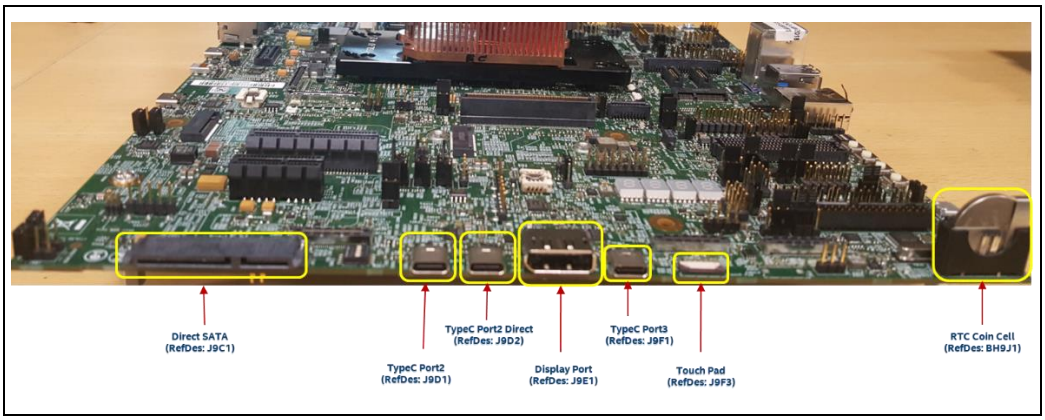


2.1.4 Actual Board Snapshot – Bottom View

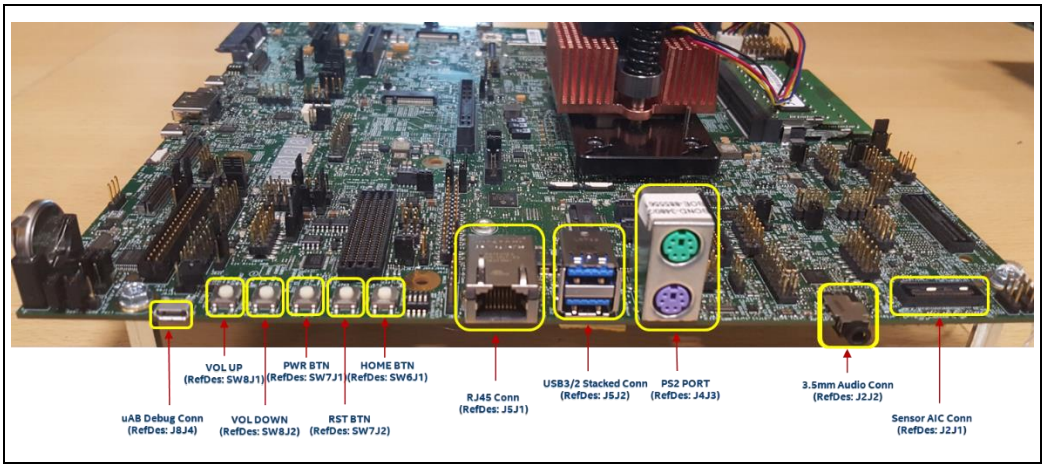
2.1.5 IO Ports Board Snapshot - North Side View



2.1.6 IO Ports Board Snapshot - West Side View



2.1.7 IO Ports Board Snapshot - South Side View



2.1.8 MODPHY Mapping

2.1.8.1 TGL UP3 RVP MPHY Mapping

Table 2-1. TGL UP3 42 RVP's MPHY Allocation

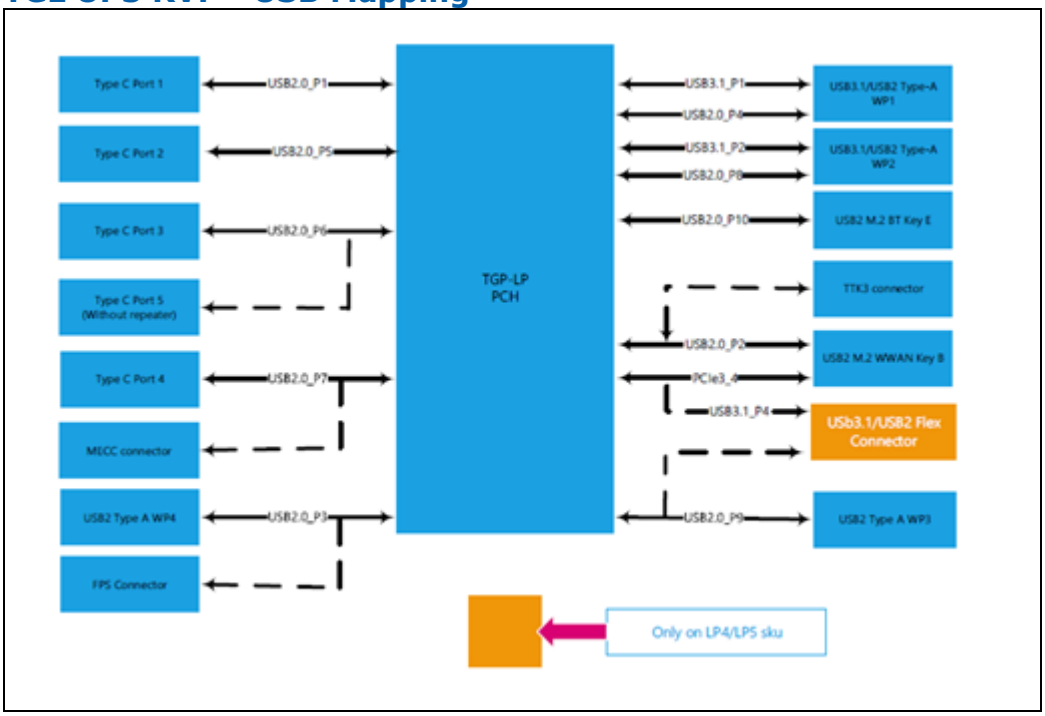
			TGL UP3 RVP mPHY Allocation- DDR4			TGL UP3 RVP mPHY Allocation-LP4x		TGL UP3 RVP mPHY Allocation-LP5	
PCIe* Controller	Lane #	Flex IO	HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 3 (SV SKU)	HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 1 (Default)	HSIO Topology 2
x4 Controller 1	Lane 0	PCIE3_1_ USB31_1	USB3/2 Type-A Con 1		HSIO Connector	USB3/2 Type-A Con 1		USB3/2 Type-A Con 1	
	Lane 1	PCIE3_2_ USB31_2	USB3/2 Type-A Con 2			USB3/2 Type-A Con 2		USB3/2 Type-A Con 2	
	Lane 2	PCIE3_3_ USB31_3	M.2 Hybrid Key E- WLAN			M.2 Hybrid Key E- WLAN		x1 M.2 Key E- Wif-Fi	
	Lane 3	PCIE3_4_ USB31_4	M.2 Key-B WWAN			M.2 Key-B WWAN	USB3.1 Gen1 Flex Connector	M.2 Key-B WWAN	USB3.1 Gen1 Flex Connector
x4 Controller 2	Lane 4	PCIE3_5	Lane 0 for x4 PCIe* slot	x4 PCIe* Slot		Lane 0 for x4 PCIe* slot	x4 PCIe* Slot	Lane 0 for x4 PCIe* slot	x4 PCIe* Slot
	Lane 5	PCIE3_6	Lane 1 for x4 PCIe* slot			Lane 1 for x4 PCIe* slot		Lane 1 for x4 PCIe* slot	
	Lane 6	PCIE3_7_LAN_0A_UFS_00	Jacksonville Gbe LAN			Jacksonville Gbe LAN		Jacksonville Gbe LAN	
	Lane 7	PCIE3_8_LAN_0B_UFS_01	x1 PCIe* Slot			x1 PCIe* Slot		x1 PCIe* Slot	
x4 Controller 3	Lane 8	PCIE3_9_LAN_0C_UFS_1_00							

			TGL UP3 RVP mPHY Allocation- DDR4			TGL UP3 RVP mPHY Allocation-LP4x		TGL UP3 RVP mPHY Allocation-LP5	
PCIe* Controller	**Lane #**	**Flex IO**	**HSIO Topology 1 (Default)**	**HSIO Topology 2**	**HSIO Topology 3 (SV SKU)**	**HSIO Topology 1 (Default)**	**HSIO Topology 2**	**HSIO Topology 1 (Default)**	**HSIO Topology 2**
	Lane 9	PCIE3_10_UFS__1_01	M.2 Key M x4 SSD (Lane reversal for x4 PCIe*)			M.2 Key M x4 SSD (Lane reversal for x4 PCIe*)		M.2 Key M x4 SSD (Lane reversal for x4 PCIe*)	
	Lane 10	PCIE3_11_SATA_0		SATA Direct Connect			SATA Direct Connect		SATA Direct Connect
	Lane 11	PCIE3_12_SATA_1					PCIe* Flex Connector (SATA supported through separate IFWI)		PCIe* Flex Connector (SATA supported through separate IFWI)
x4 Controller 4 (Gen 4 North side)	CPU Lane 0	CPU_PCIE_0	M.2 Key M x4 SSD	x4 PCIe* Slot		M.2 Key M x4 SSD	x4 PCIe* Slot	x4 PCIe* Slot	M.2 Key M x4 SSD
	CPU Lane 1	CPU_PCIE_1							
	CPU Lane 2	CPU_PCIE_2							
	CPU Lane 3	CPU_PCIE_3							

2.1.8.2 TGL UP3 RVP - SRC Clock Mapping

SRC CLK	SRC CLK REQ	TGL UP3 RVP mPHY Allocation- DDR4			TGL UP3 RVP mPHY Allocation-LP4x		TGL UP3 RVP mPHY Allocation- LP5	
		HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 3 (SV SKU)	HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 1 (Default)	HSIO Topology 2
0	0	CPU Gen4 PCIE* x4 M.2 SSD	CPU Gen4 x4 PCIe* Slot		CPU Gen4 PCIE* x4 M.2 SSD	CPU Gen4 x4 PCIe* Slot	CPU Gen4 PCIE* x4 M.2 SSD	CPU Gen4 x4 PCIe* Slot
1	1	M.2 Hybrid Key E- (WLAN x1 PCIE*)		HSIO Connector	M.2 Hybrid Key E- (WLAN x1 PCIE*)		M.2 Hybrid Key E- (WLAN x1 PCIE*)	
2	2	M.2 Key-B WWAN X1 PCIE*			M.2 Key-B WWAN X1 PCIE*		M.2 Key-B WWAN X1 PCIE*	
3	3	x4 M.2 SSD(Lane reversal for x4 PCIe*)			x4 M.2 SSD(Lane reversal for x4 PCIe*)	PCIe* Flex Connector(SATA supported through separate IFWI)	x4 M.2 SSD(Lane reversal for x4 PCIe*)	PCIe* Flex Connector(SATA supported through separate IFWI)
4	4	Gbe LAN			Gbe LAN		Gbe LAN	
5	5	x1 PCIe* Slot			x1 PCIe* Slot		x1 PCIe* Slot	x4 M.2 PCH SSD (Hybrid SSD)
6	6	PCH PCIE* x4 PCIe* DT Slot			PCH PCIE* x4 PCIe* DT Slot		PCH PCIE* x4 PCIe* DT Slot	

2.1.8.3 TGL UP3 RVP - USB Mapping

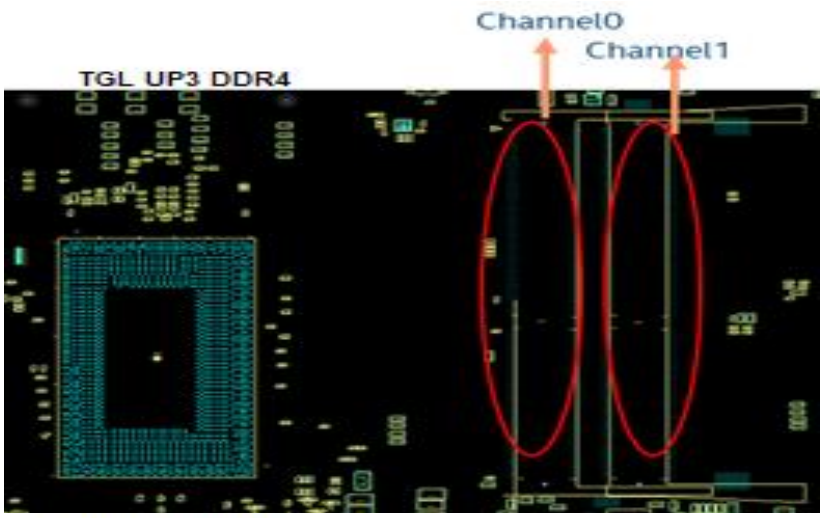


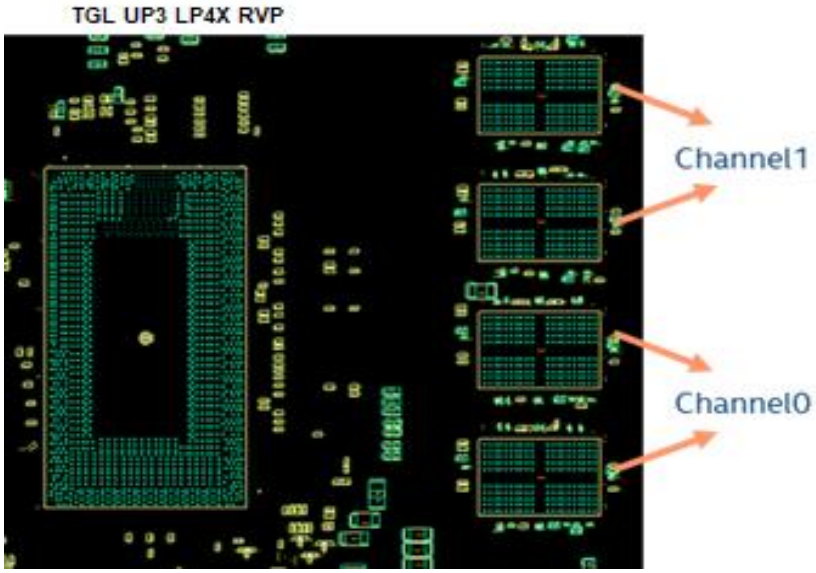
2.2 Memory

2.2.1 TGL UP3 RVP - Memory Specification

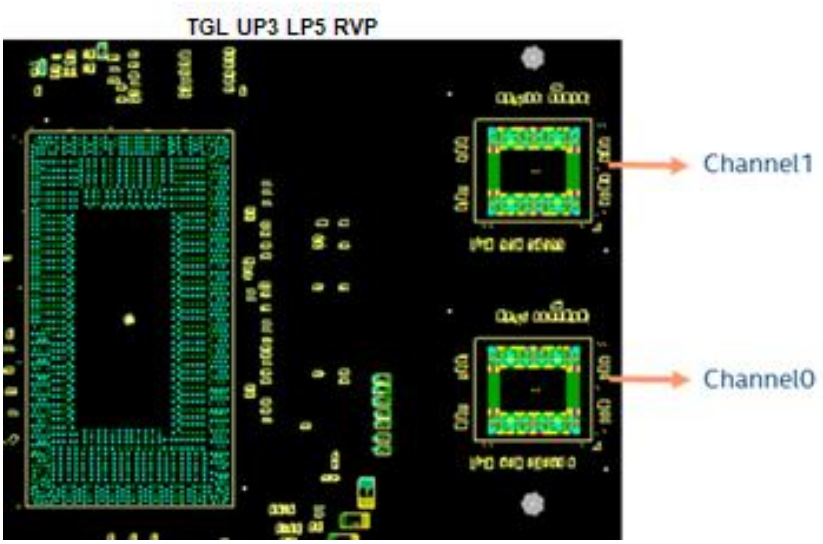
Default Memory Details	
Type	**DDR4 SODIMM, 1DPC, 2 Channel**
Topology	Non-Interleaved routing
Size	Total 16 GB (8 GB per channel)
Placement	1*9.2 mm DIMM and 1*5 mm DIMM placed back to back, one above the other (refer to layout snapshot below)
POR SPEED	3200 MT/sec

Default Memory Details	
Type	**LPDDR4 X32, 2 Devices Channel**
Topology	Non-Interleaved routing
Size	Total 16 GB (8 GB per channel)
Placement	Device down / Socketed
POR SPEED	4267 MT/sec



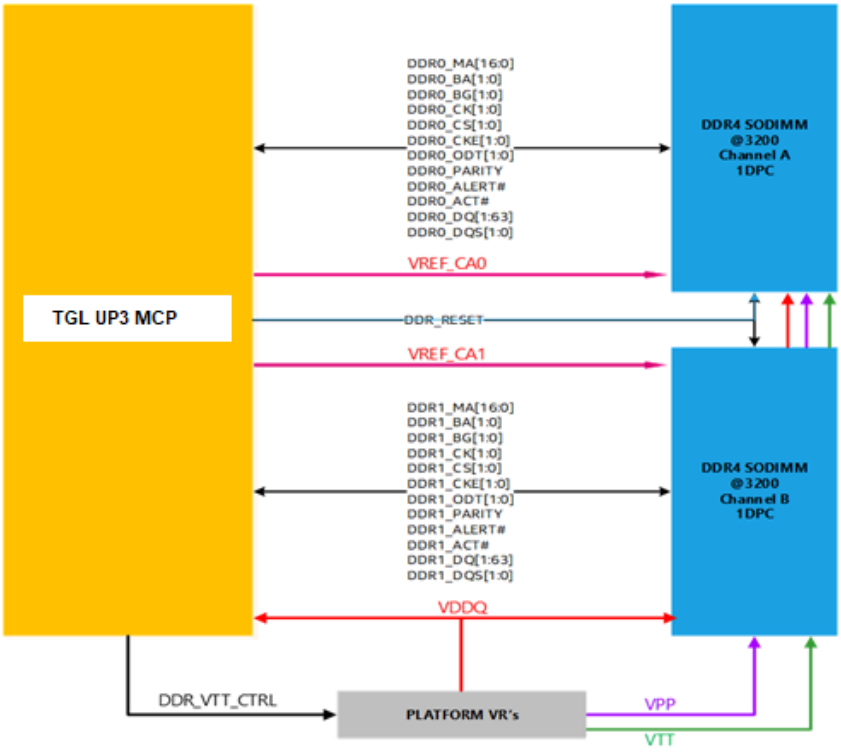


Default Memory Details	
Type	**LPDDR5 X64, 2 Devices Channel**
Topology	Non-Interleaved routing
Size	Total 12 GB (6 GB per channel)
Placement	Device down / Socketed
POR SPEED	5400 MT/sec



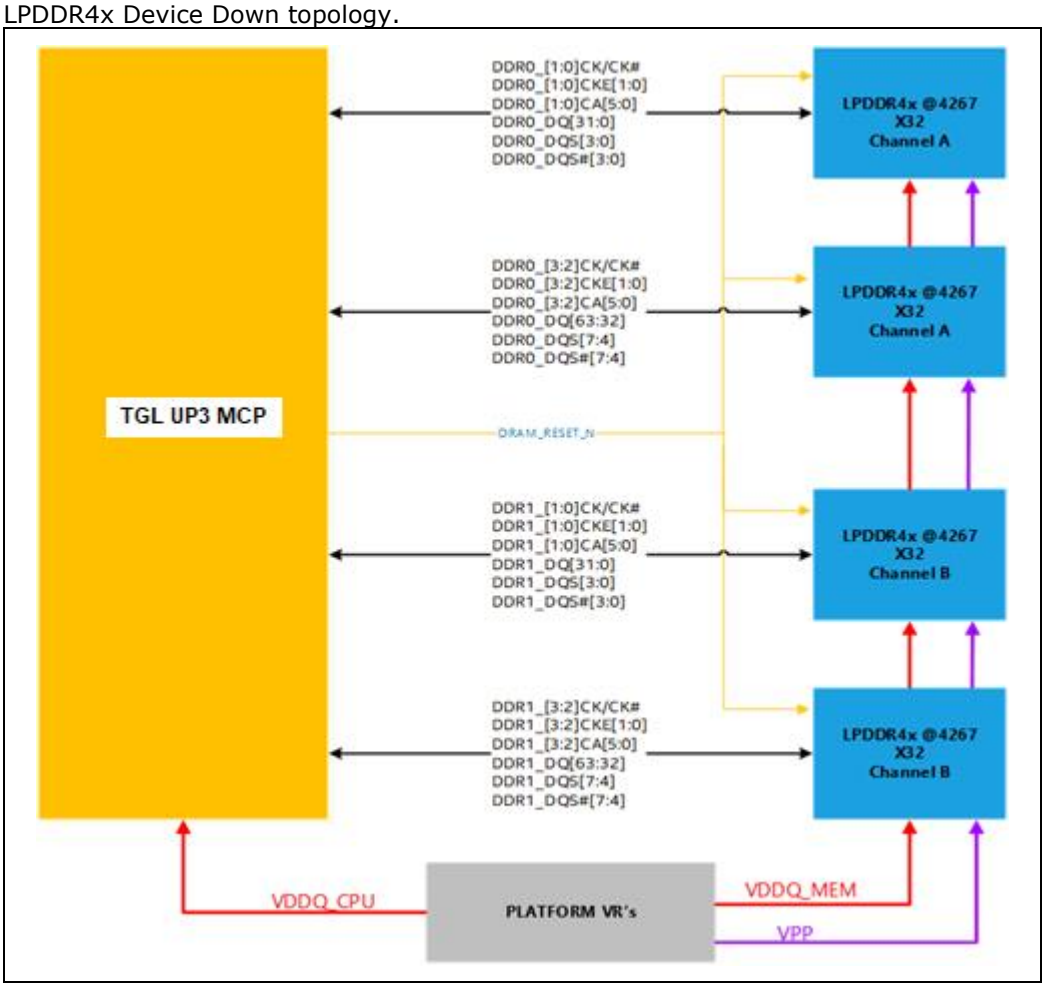
2.2.2 Memory Topology

TGL UP3 DDR4 SODIMM RVP follows Non-interleaved memory configuration for 2x 1DPC SODIMM.



2.2.2.1 Memory Topology (LPDDR4x Device Down)

TGL UP3 LPDDR4x RVPs follows Non-interleaved memory configuration for 4 X32 LPDDR4x Device Down topology.



2.3 Display

2.3.1 TGL UP3 RVP - Display Mapping

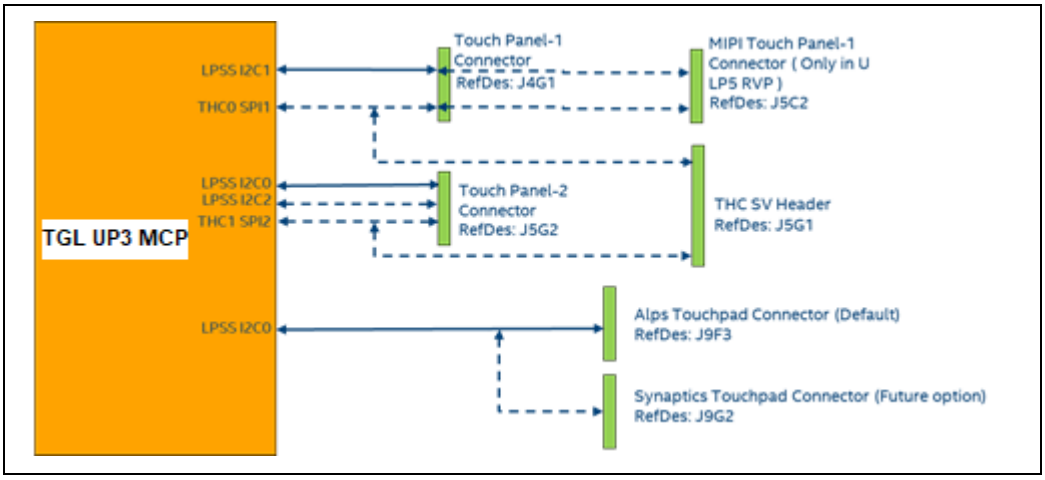
TGL UP3 Silicon Interface	TGL UP3 DDR4 RVP		TGL UP3 LP4x RVP		TGL UP3 LP5 RVP	
	Option 1 (Default)	Option 2 (Unstuffed)	Option 1 (Default)	Option 2 (Unstuffed)	Option 1 (Default)	Option 2 (Unstuffed)
DDIA	eDP Connector	-- NA --	eDP Connector	-- NA --	eDP Connector	MIPI Connector
DDIB	HDMI2.0 with ALS	eDP /HDMI with CRLS	DP++ Connector	eDP Connector	HDMI2.0 with Retimer	eDP Connector

TGL UP3 Silicon Interface	TGL UP3 DDR4 RVP		TGL UP3 LP4x RVP		TGL UP3 LP5 RVP	
	Option 1 (Default)	Option 2 (Unstuffed)	Option 1 (Default)	Option 2 (Unstuffed)	Option 1 (Default)	Option 2 (Unstuffed)
TCP0	TCP port 1	NA	TCP port 1	HDMI 2.0 with Retimer	HDMI2.0 with ALS	TCP Port1
TCP1	TCP port 2	NA	TCP port 2	NA	TCP port 2	-- NA --
TCP2	TCP port 3	TCP Direct Port 5 (without retimer)	TCP port 3	Ardent Connector USBC	TCP port 3	TCP Direct Port 5 (Without retimer)
TCP3	TCP port 4	DP++ Connector	TCP port 4	HDMI 2.0 with CRLS	TCP port 4	DP++ Connector

HDMI Topology	Manufacturer Part Number	Description
Active Level Shifter (ALS)	PS8203	Ultra-Low Power 3.0 GBPS HDMI Level Shifter
HDMI 2.0 Retimer	SN75DP159RGZT	6.0 Gbps TMDS to HDMI Level shifter Retimer

2.4 Touch Panel and Touch Pad

2.4.1 TGL UP3 RVP Touch Panel/Pad



Note: Solid line indicates default support on the board. Dotted lines indicate the need for rework.

Both THC and I^2C are PoR for TGL for Touch connectivity. I^2C is enabled by default and THC option is provided through the feature rework.

Touch Panel-2 has an option of I^2C2 also to validate the 1 MHz I^2C speed cases.

For touchpad, use Alps touchpad as an option for Synaptics touchpad and is also provided, since Alps touchpad has become EOL.

2.5 Thunderbolt™ Type C Interface

2.5.1 Type C Support

Board/Port	TGL UP3 DDR4	TGL UP3 LP4x	TGL UP3 LP5
TCP0	Type C Connector 1	Type C Connector 1	Type C Connector 1
TCP1	Type C Connector 2	Type C Connector 2	Type C Connector 2
TCP2	Type C Connector 3	Type C Connector 3 via internal cable	Type C Connector 3
TCP3	Type C Connector 4 Type C Connector 5 (re-timer bypass; rework required)	Type C Connector 4 Ardent connector	Type C Connector 4 Type C Connector 5 (re-timer bypass; rework required)

TGL UP3 SoC supports max 4 Type C Thunderbolt™ ports at a time. Below is the RVP wise type C port mapping (Refer to Section 2.3 for optional display mapping on TCP ports that is available in Display section).

Using the three Pad Caps rework, TGL-UP3 RVP can support optional legacy Display outputs. Refer to Display section (Section 2.3) for details.

One of the TCP port supports re-timer less configuration for USB 3.1 Gen2/ DP validation. The port does not support TBT. AUX signals orientation supported on board with extra SoC GPIO's and EC control.

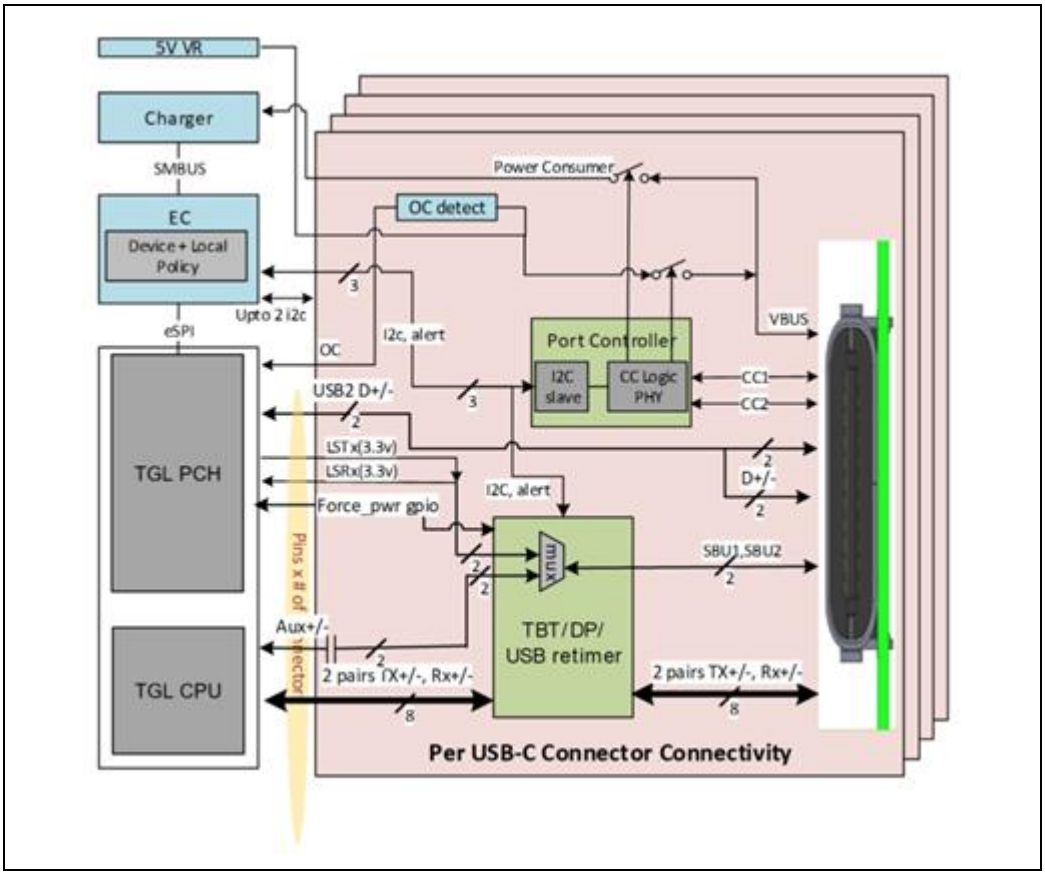
Burnside Bridge Thunderbolt™ Re-timer is soldered down on TGL UP3. RVP is the PoR for TGL ROW RVP.

TCP0 on all the TGL RVP is routed to maximum pre- channel (SoC to re-timer) length requested for electrical validation. Rest of the TCP ports are routed based on the connector placement meeting Platform Design Guideline (PDG).

2.5.1.1 TGL Type C Architecture

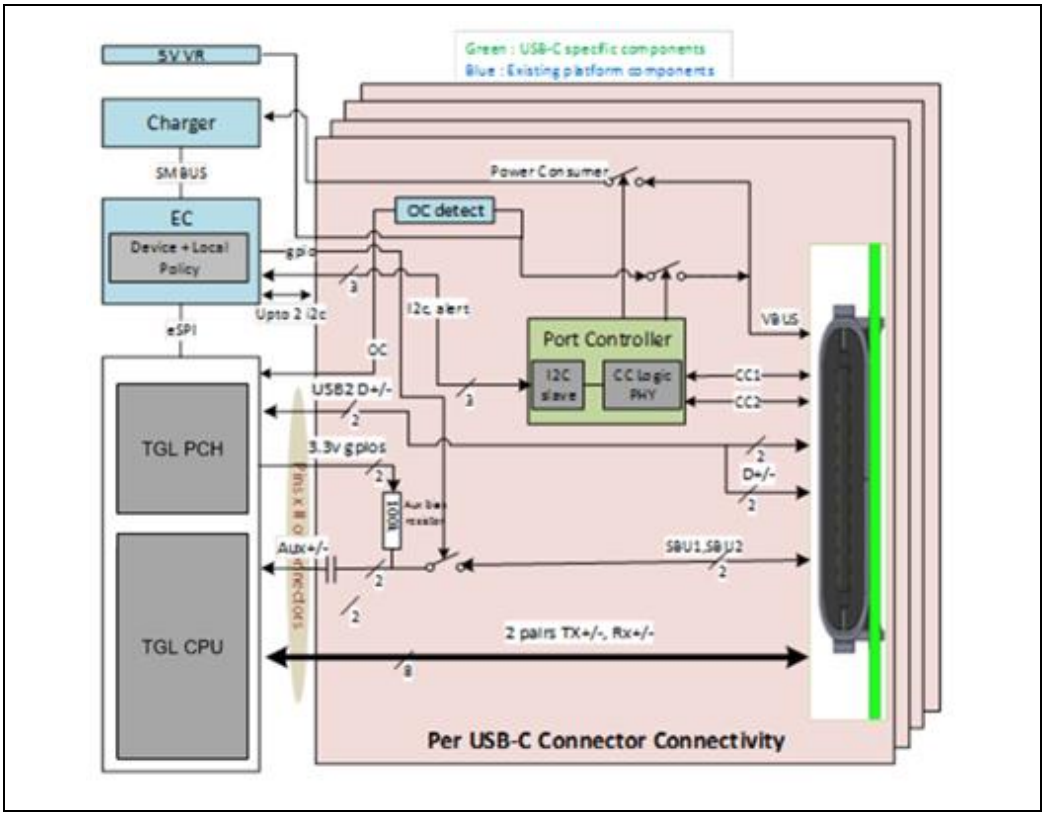
- **Port Configuration:**
  - UP3 42 → 4 Ports
- **PD Controller and EC:**
  - CCG5- TGL UP3;
  - Detecting attach/orientation of cable.
  - Connects VCONN/VBUS to connector.
  - Provides UFP/DFP roles and USB Power delivery protocol.
  - Makes decisions on USB PD policy along with help of OS.

- **Re-timer:**
  - Boosts signal strength/condition the high-speed signals.
  - AUX and LSx signals cannot be muxed inside the SoC due to different signal characteristics.
  - LSx (UART) Signals are used for FW loading.
- **Intel® Vpro Over Type C dock:**
  - SMLink0 is used for Ethernet communication over Type C on SBU Lines.
  - Connected to Intel® CSME over Re-timer SMBUS.



2.5.1.2 TGL Type C Architecture – Without Retimer

- **AUX Signals orientation logic:**
  - GPIO's from PCH are connected AUX P and N Signals with 100 K Resistor.
  - By Default, signals connected to AUX_N are Driven High and Signal Connected to AUX_P will be Driven Low.
  - Depends on the direction of Type C cable Insertion GPIO function is changed to Drive High/Low.
  - Same Port Controller is used for TCP Port 2 with and without Retimer paths, BOM Changes to be done to enable without Retimer path.



2.5.1.3 Retimer Flash Sharing

RVP Name	TCP0	TCP1	TCP2	TCP3
TGL UP3 DDR4/LP4x/LP5 RVP	Flash shared between TCP0/1		Flash shared between TCP2/3	

Type C Retimers has an option to share the Flash between 2 Retimers for BOM cost saving.

Only one Retimer have the access for flash at a time. This is controlled by the FLASH Busy signal connected between the Re-timers. Flash share setting is done in Hardware.

2.5.1.4 USBC Enablement on RVP

TGL UP3 DDR4 RVP has PD AIC connector to enable third party PD controller vendor. It is supported on TCP0 and TCP1 ports through rework.

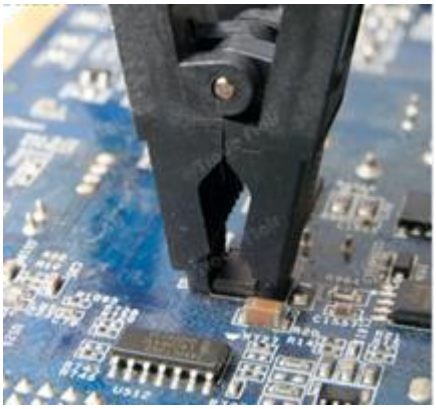
TGL UP3 RVP supports TCP2 and TCP3 port control through the MECC AIC for Chrome* early enabling. Rework is needed to enable the port controller on AIC and BC1.2 support over USB2 port.

2.5.1.5 DnX Support

- DnX:
  - Download and execute is a feature that allows updating the system FW from a host through USB2 port
  - Supported on TCP0 port in TGL UP3 RVP
  - Could be triggered
    - By pressing VOL_UP and VOL_DOWN together during early boot
  - LED indicates, if the FW download/execution is in progress, after DnX is triggered during boot up
  - Supported in both TGL UP3 and TGL UP4 RVP SKU.

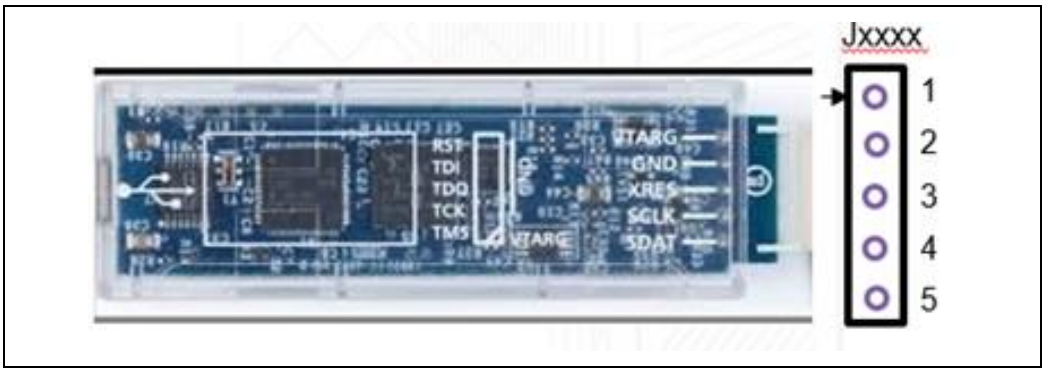
2.5.1.6 Retimer Flash Programing

- Retimer Flash devices does not have the Dedicated Connector for Flash programming.
- Dediprog SF600 with Clips can be used for Flash Programming. https://www.dediprog.com/pd/programmer-accessories/EM-TC-8



2.5.1.7 PD Controller Programming

TGL UP3 RVP supports Cypress* CCG5 PD controller on board. This PD controller FW could be programmed/updated using PSoC programmer through1x5 header on the RVP.



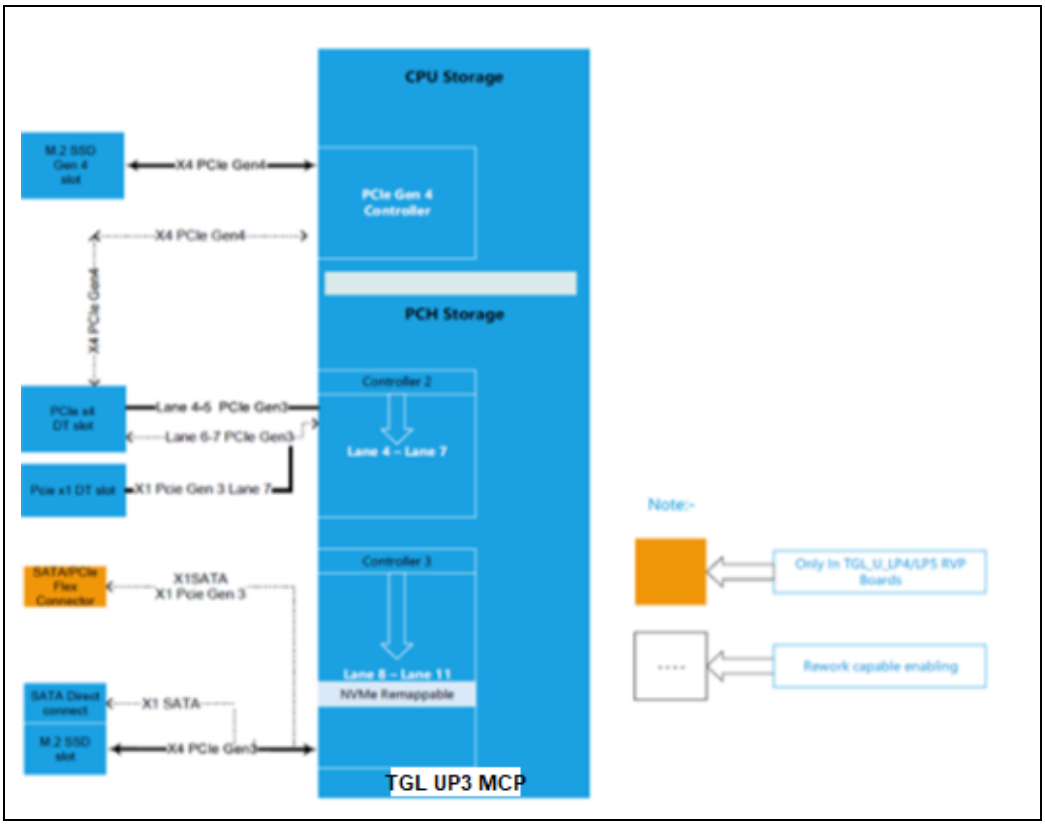
RVP SKU	Programming Header for PD1 and PD2
TGL UP3 DDR4 RVP	J9B1 and J8E2
TGL UP3 LP4x RVP	J9B1 and J8E2
TGL UP3 LP5 RVP	J9B1 and J9D2

Programming guidelines for CCG5:

- PD1 supports 2 ports and PD2 supports 1 port. Same PD FW could be flashed for both the ports.
- Each PD controller has SF600 header provided to update PD FW. Dediprog utility could be used to program the FW, similar to IFWI programming.

2.6 Storage

2.6.1 TGL UP3 RVP Storage Interfaces – High Level

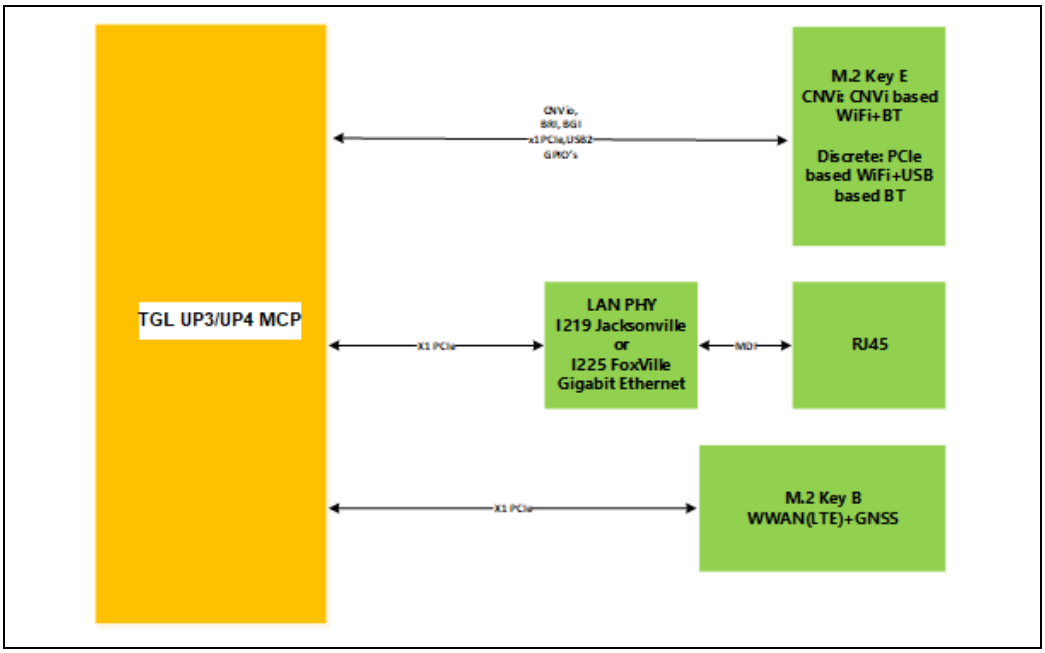


Description	Refdes
PCH M.2 SSD SLOT PCIE_75P_KEYM_2M_C	J7R1
CPU M.2 SSD SLOT PCIE_75P_KEYM_2M_C	J7A3
SATA Direct connector	J9C1

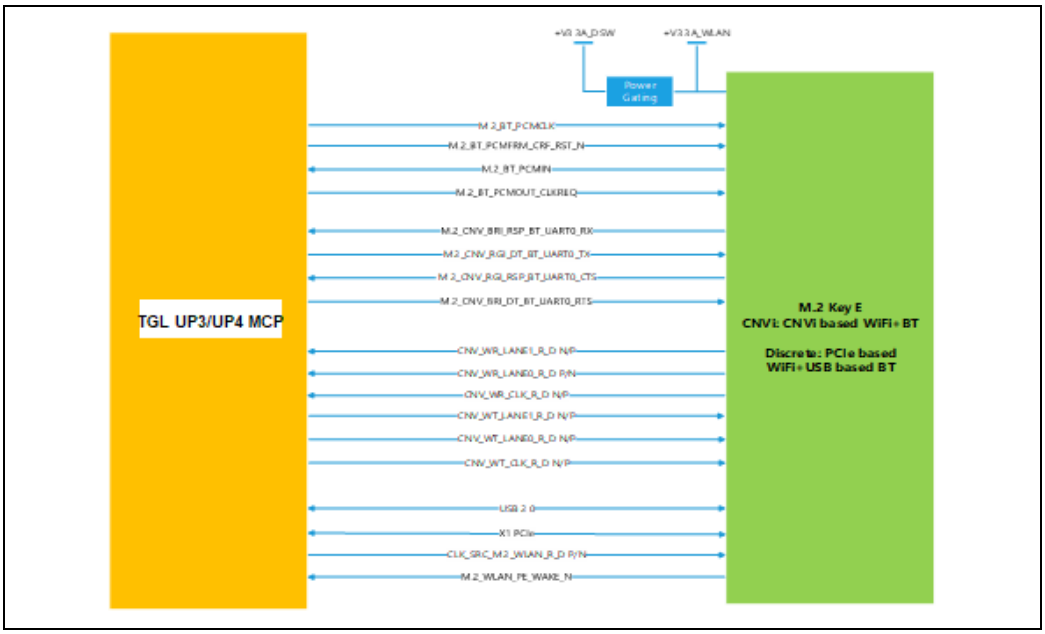
PCIe*-SATA-USB Flex Connector sharing option is available on TGL UP3 LP4x and TGL UP3 LP5 board.

2.7 Communications

2.7.1 Connectivity Overview



2.7.2 Connectivity Block Diagram



2.7.3 Connectivity – Modules Supported

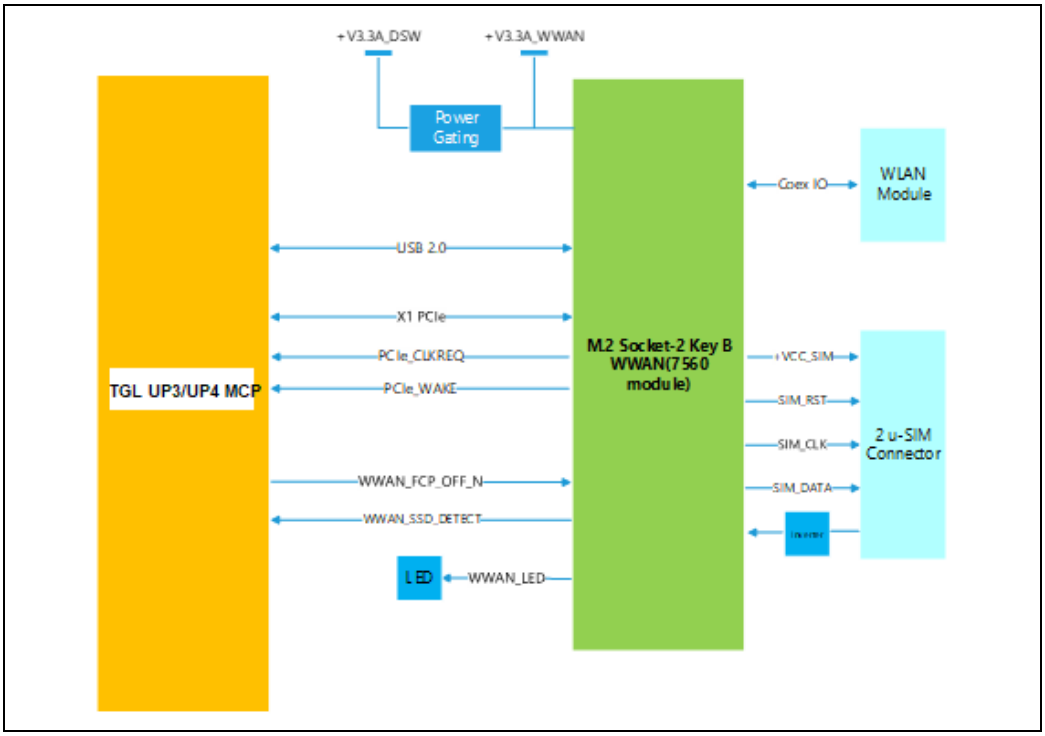
TGL UP3 RVP supports M.2 CNVi modules and discrete modules on a single M.2 2230 connector.

Table 2-2. TGL UP3 RVP M.2 2230 Module Support

M.2 Module	Module Names	Host Interfaces
CNVi	Harrison Peak	DPHY TX/RX (Wi-Fi) BRI/RGI (BT®)
Discrete	Thunder Peak	PCIe* TX/RX (Wi-Fi) UART+PCM (BT®) or USB2.0 (BT®)

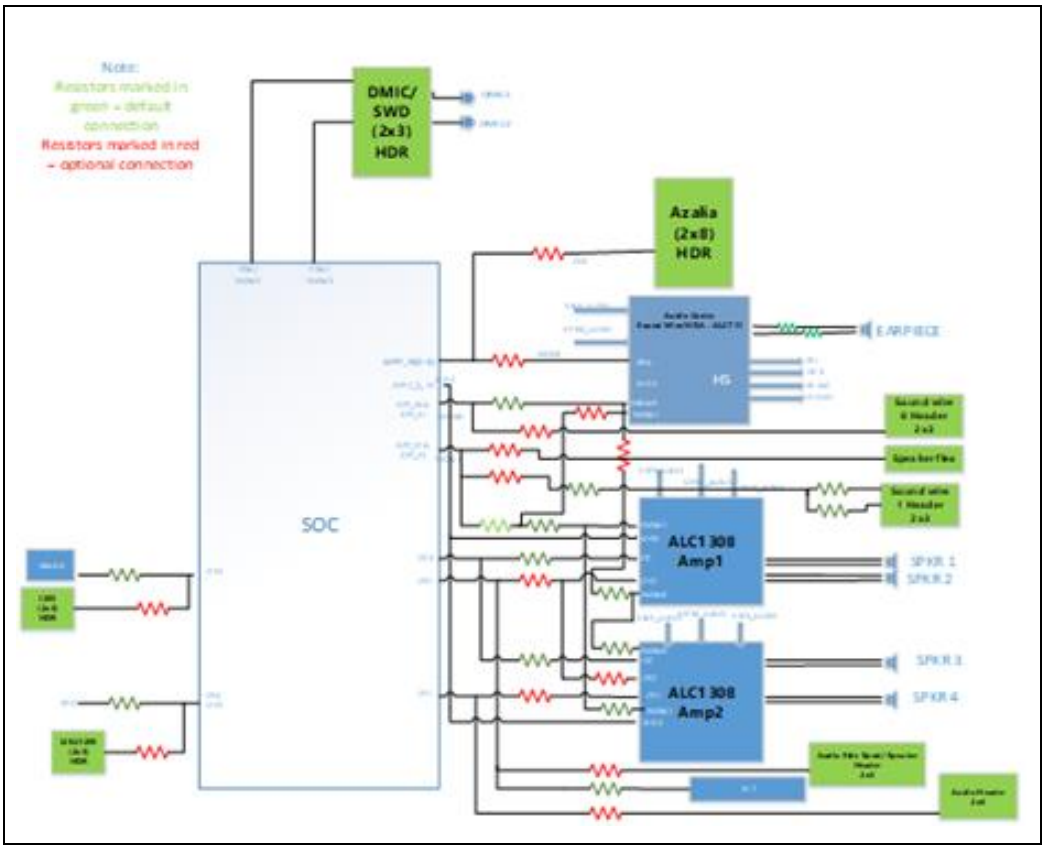
2.8 Modem

2.8.1 Modem Block Diagram

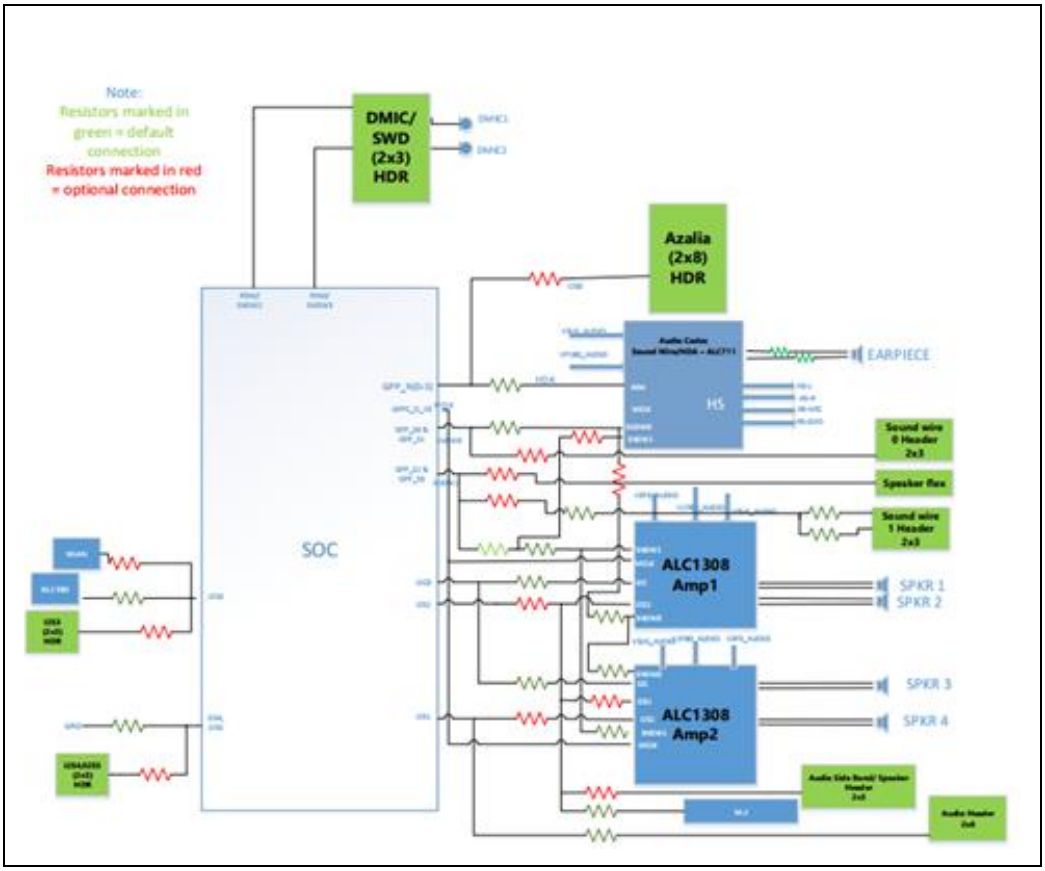


2.9 Audio

2.9.1 TGL UP3 RVP Audio Block Diagram



Default path for ALC711	• Headset codec is SoundWire* 0. • It can also be enabled by HDA by rework.
Default path for ALC1308	• Amplifier is SoundWire* 1. • Can also be enabled by I^2S1 and I^2S2.
Default path for ALC715	• DMIC is SoundWire* 2 and 3.



- Default path for ALC711- Headset codec is HDA.
  - It can also be enabled by SoundWire* 0.
- Default path for ALC1308 – Amplifier is SoundWire* 1.
  - Can also be enabled by I2S1 and I2S2 for TGL UP3 RVP.
- Default path for ALC715 – DMIC is SoundWire* 2 and 3.

2.9.2 Audio Overview

TGL Silicon support I²S, HDA and SoundWire* interfaces for audio.

Default ALC711 codec configuration is SoundWire* in all RVPs.

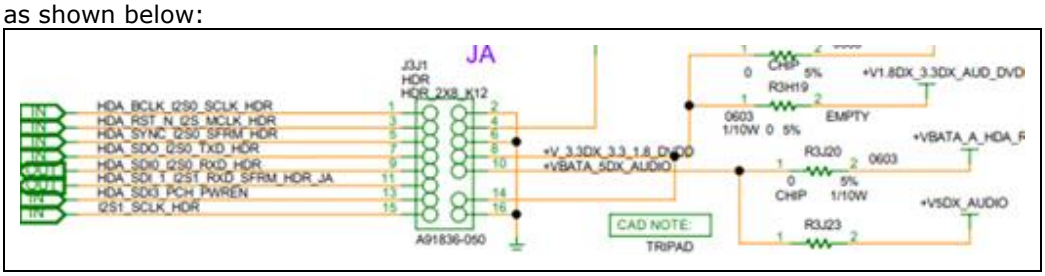
Audio links include:

- I²S/SSP Interfaces for platform peripherals.
- Dual-channel Platform HD-A controller for attaching HD-A compatible peripherals [Two SDI signals to support two external codecs].
- Two dual-channel PDM directly attached microphone interfaces.
- Four SoundWire* Interfaces for platform peripherals.
- On board 3.5 mm headset combo jack is provided.

Note: Below are the details of the HDR supported on RVP:

2.9.2.1 HD-A Header

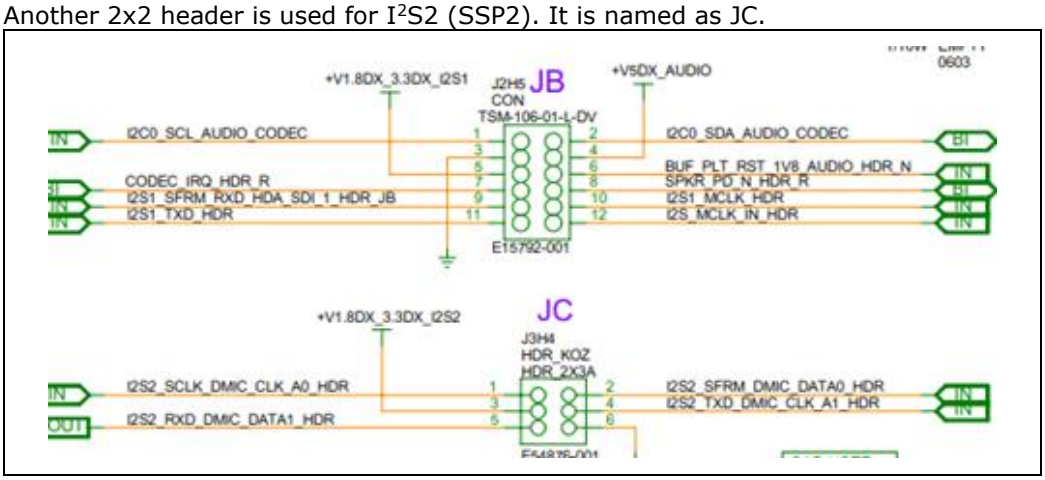
An external third-party codec validation can be done using this header. The pin-out is as shown below:



2.9.2.2 Speaker/I²S Header

The 2x6 header is used for I²C0, I²S1 and GPIO pinout is shown below. It is named as JB. This can be used to connect external speaker or external I²S based codec AIC.

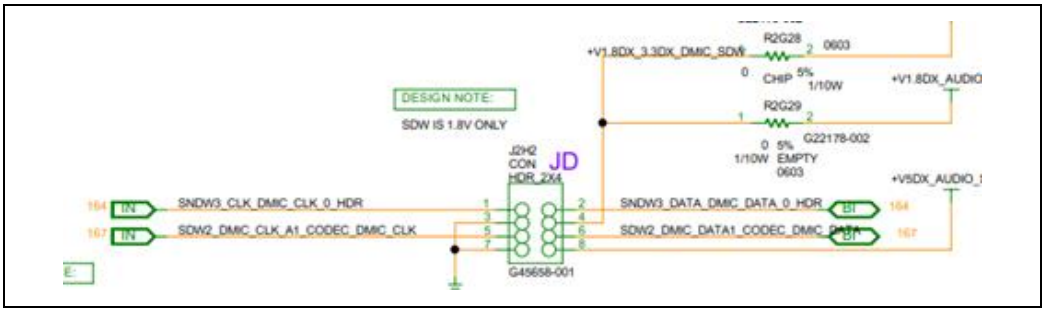
Another 2x2 header is used for I²S2 (SSP2). It is named as JC.



2.9.2.3 DMIC/SDW MIC Header

An external digital MIC validation can be done using this header, JD.

JD is used for connecting PDM microphones and SDW MIC. Two MIC devices can be connected to one DMIC header.

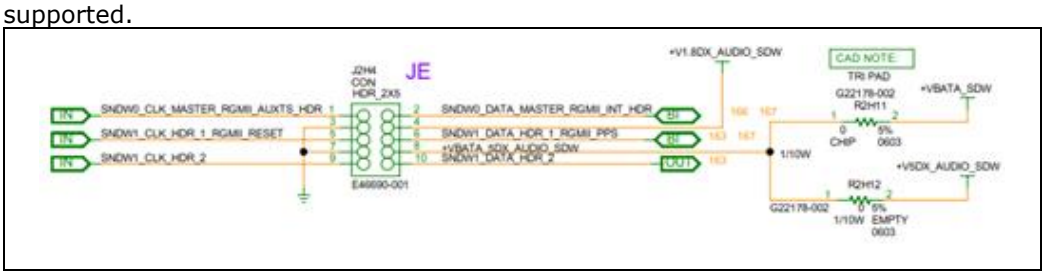


2.9.2.4 Amplifier and Digital Speaker Header

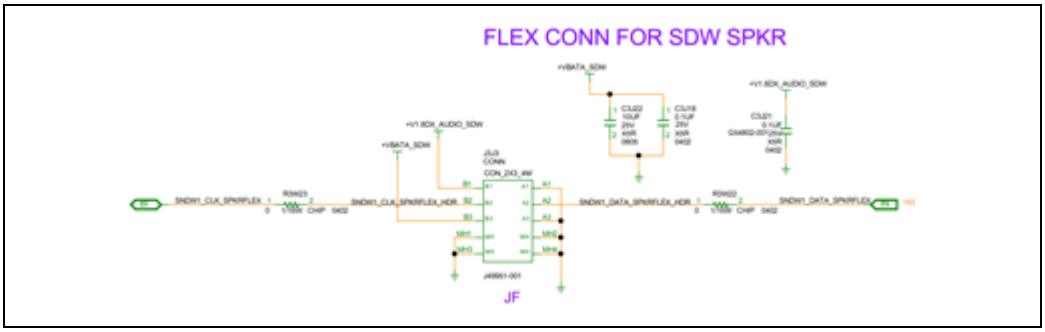
An external amplifier and digital speaker can be validated using this header. The TGL-UP3 RVP supports ALC711 or external Codec connectivity options on this header.

The default connectivity is for the PCH with ALC711 codec or external codec options selected through resistor reworks.

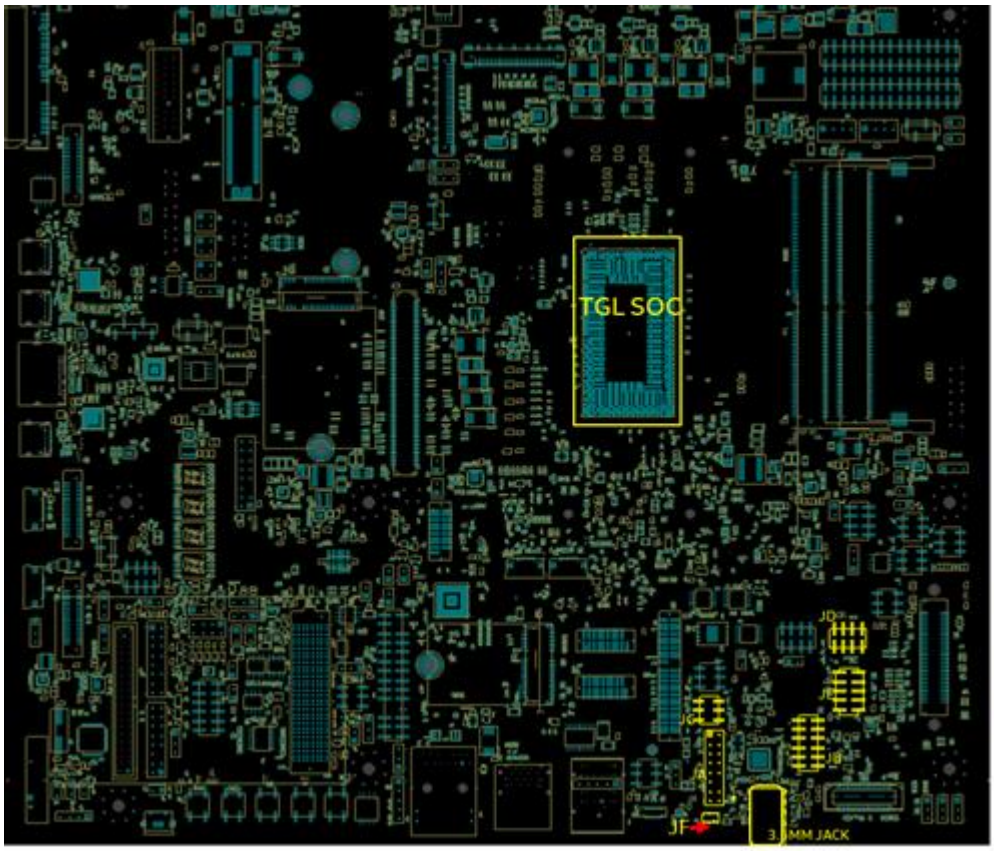
Another 2x5 HDR, JE is added to support SoundWire* speaker. Star topology is also supported.



There is an option to connect the DSM+FPC module from Trigence on RVP. JF is the connector.



2.9.3 Board Layout – Top Audio HDR



2.10 Camera

2.10.1 Camera Support

RVP contains 3 CRD 60 pin connector on TGL UP3 RVP to support MIPI Based Camera.

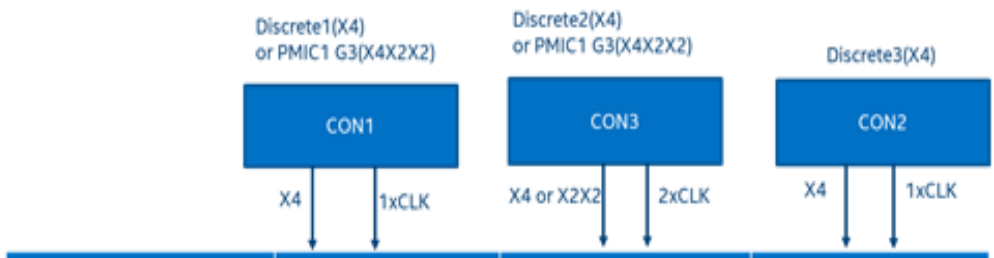
Can support maximum 4 camera interfaces on TGL UP3 RVP.

There are two CRD Camera AIC that can be supported on TGL UP3 RVP as below:

- Discrete CRD AIC -> x4 support.
- PMIC based G3 Card> x4, x2, x2 Support (This plugs over two CRD connectors).

2.10.2 TGL UP3 Camera Configuration Support

TGL UP3 Pin Name	RVP Connector Name	Possible Camera Configurations	
		Option 1	Option 2 (Default)
CSI_A_D0P_B_D3P	CRD Conn 1	X4 lane	X4 lane (Use CRD G3 card)
CSI_A_D0N_B_D3N			
CSI_A_D1P_B_D2P			
CSI_A_D1N_B_D2N			
CSI_B_CKP			
CSI_B_CKN			
CSI_B_D0P			
CSI_B_D0N			
CSI_B_D1P			
CSI_B_D1N			
CSI_C_D1P	CRD Conn 2	X4 lane	X4 lane
CSI_C_D1N			
CSI_C_D0P			
CSI_C_D0N			
CSI_C_CKP			
CSI_C_CKN			
CSI_D_D1P_C_D2P			
CSI_D_D1N_C_D2N			
CSI_D_D0P_C_D3P			
CSI_D_D0N_C_D3N			
CSI_E_CKP	CRD Conn 3	Not used	X2 lane (Use CRD G3 card)
CSI_E_CKN			
CSI_E_D0P_F_D3P		X4 lane	
CSI_E_D0N_F_D3N			
CSI_E_D1P_F_D2P			
CSI_E_D1N_F_D2N			
CSI_F_CKP			X2 lane (Use CRD G3 card)
CSI_F_CKN			
CSI_F_D0P			
CSI_F_D0N			
CSI_F_D1P			
CSI_F_D1N			



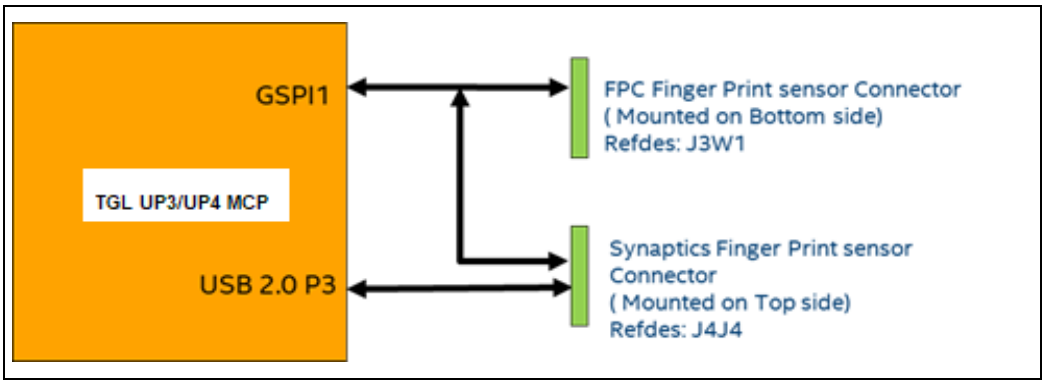
GPIOs	Discrete1 or PMIC1 G3	Discrete2 or PMIC1 G3	Discrete3
1X PWREN	✓	✓	✓
1X RST	✓	✓	✓
1X Flash_Trigger	✓	(optional path from con1)	(optional path from con1)
1X Privacy LED(shared with VSync1)	(optional path from con2)	(optional path from con2)	✓
1X CLK Enable(shared with VSync2)	✓	×	×
VSYNC	VSync1	Option from VSync1	Option from VSync1/VSync2
I2C	I2C3	I2C2	I2C5

Below are the current set of PoR camera sensor/Modules defined for TGL, which are subject to change.

Note: RVP team does not work on the module list and the adapters for these modules on the CRD card.

Vendor	Sensor	Module p/n	Details
Sunny Optical*	IMX362	A12N08B-200	12 MP, 2 PD (MD-Depth), SVE
Sunex*	IMX477		12MP, Multi-Exposure (DOL), 90FPS, WFOV (Chief Ray Angle), PDAF T1, 240 fps@1080p
Azure Wave*	IMX488	AM-7BF56B6	1.07 MP, RGB-IR 4x4
Omni Vision*	OV2775+TI	OV02775-MC02-FD00	2 MP, Multi-Exposure (GDC DOL) with Dual Conversion Gain

2.10.3 Fingerprint Sensor Block Diagram

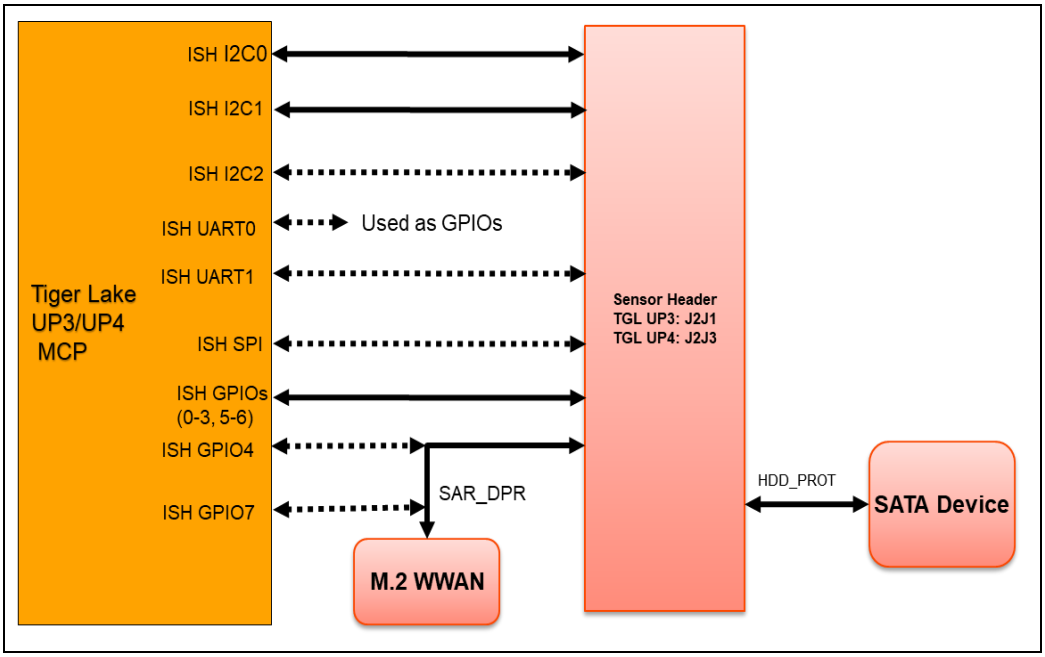


NOTES:

1. Solid line indicates default support on the board. Dotted lines indicate the need for rework.
2. Both USB2.0 and GSPI are PoR for TGL for FPS connectivity. Since, customers are mostly using USB2.0 based FPS, 3PE recommendation is to use USB2.0. Also, the GSPI Fingerprint sensor is EOL.
3. Enabling a new FPS with USB2.0 and GSPI capable from Synaptics/GOodix for TGL RVP/AEP. The connector pinout supports both USB2.0 and GSPI.

2.11 Sensors

2.11.1 Sensors and Sensor AIC Block Diagram



NOTES:
1. Solid line indicates default support on the board. Dotted lines indicate the need for rework.
2. ISH UART0, ISH UART1 are used as GPIOs. ISH_SPI is used for LSX signals for TBT™.
3. ISH I2C2 is used as LPSS I2C5.
4. Refer to PCL for list of sensor part numbers.

2.11.2 LPSS I²C Devices Mapping

LPSS I2C MAPPING	TGL-UP3
LPSS I²C0	Touch Pad I²S based codec Header ALC1308 Chip#1 ALC1308 Chip#2 Thunderbolt™ re-timer Chip#2 Thunderbolt™ re-timer Chip#3 Thunderbolt™ re-timer Chip#4 Touch Panel-2
LPSS I²C1	Touch Panel-1
LPSS I²C2	Cam_Connector-3 (1 sensor on G3 card#1) Touch Panel-2
LPSS I²C3	Cam_Connector-1 (2 sensors on G3 card#1)
LPSS I²C4/ CNVi MFUART2	Not used (Used as CNVi MFUART signal, I2C4 cannot be used)
LPSS I²C5/ ISH I2C2	Cam_Connector-2 (1 sensor on G1 card#1) Processor secure storage (PSS) Power meter Chip#1 Power meter Chip#2 Power meter Chip#3

NOTE: Default Support is 1.8 V and Support for 3.3 V can be enabled through rework and IFWI image changes.

2.11.3 LPSS UART and LPSS GSPI Mapping

LPSS UART Mapping	TGL UP3/UP4
LPSS UART0	Used as GPIOs
LPSS UART1/ISH UART1	▪ Used as GPIOs ▪ Sensor Header
LPSS UART2	▪ Serial debug port ▪ 2X3 Header ▪ MECC AIC ▪ MIPI 60 connector

LPSS GSPI Mapping	TGL UP3/UP4
LPSS GSPI0	Used as GPIO
LPSS GSPI1	Finger Print Sensor
LPSS GSPI2/ISH SPI	Sensor Header

2.11.4 Serial Interface Devices Mapping

SPI, THC SPI, eSPI MAPPING	TGL UP3
SPI0	• BIOS Flash • TPM • Dediprog Header/ TTK3 Header for Flash Programming (SF600) • MECC AIC
SPI1/ THC0 SPI1	Touch Panel-1 connector
THC1 SPI2	Touch Panel-2 connector
eSPI	• EC • eSPI Bus Header • MECC AIC

SMBUS, SMLINK, MLINK MAPPING	TGL UP3
SMBUS	• SMBus expander • SODIMM • X4 PCIe* Slot • X1 PCIe* Slot • HSIO Connector • eSPI Bus header • MIPI 60 connector • FRU • PM Sideband Header • PSS
SMLINK0	• LAN • Thunderbolt™ Retimer • X4 PCIe* Slot
SMLINK1	• PM side band header • MECC AIC • PD controller

SMBUS, SMLINK, MLINK MAPPING	TGL UP3
MLINK	• M.2 WLAN

2.11.5 ISH Interface Mapping

ISH SPI and GPIOS MAPPING	TGL UP3
ISH SPI	Sensor Header
ISH GPIOs	Sensor Header

ISH I^2C MAPPING	TGL UP3
ISH I^2C0	Sensor Header ISH EEPROM
ISH I^2C1	Sensor Header
ISH I^2C2/ LPSS I^2C5	Sensor Header

ISH UART MAPPING	TGL UP3
ISH UART0	Used as GPIO MECC AIC 2X3A SV Header
ISH UART1/ LPSS UART1	Used as GPIO Sensor Header

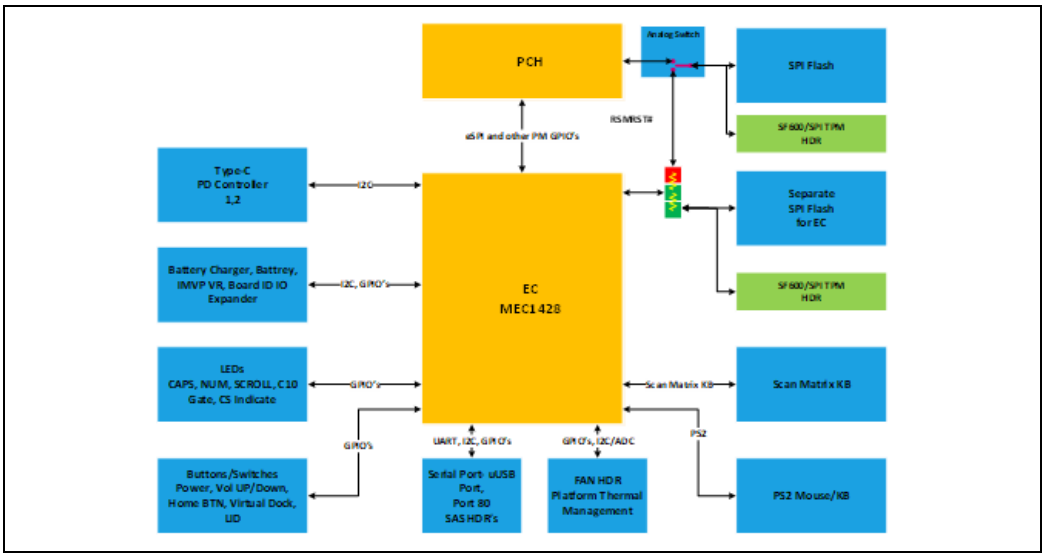
2.12 Embedded Controller

TGL RVP supports MEC1428 Microchip* Embedded Controller (EC) onboard. MEC1428 supports ESPI mode of operation. LPC mode is not supported in TGL. EC controls the preliminary platform power sequencing and does system and power management. EC is the platform thermal controller that monitors and throttles CPU or controls CPU Fan. MECC 2.0 AIC is supported on TGL UP3 RVP SKU's. The Key functionalities of EC on the platform are listed below,

- External PS2 Keyboard and Mouse.
- Thermal Management like CPU Fan control, Chassis Fan control, PECI, DIMM temperature and so on.
- TGL lacks the PECI and PECI over eSPI needs to be used.
- Platform Power management like Power sequencing, Sx and Deep Sx entry/exits.
- Modern Standby requirements to be implemented inside EC.
- Handles the Board-ID, Fab-ID, BOMSKU-ID, messages to the BIOS.
- RVP supports all three: SAF, MAF, G3 Flash configuration, default is be MAF.

- In addition, to MECC AIC support, 2x14 pin eSPI header is also be supported
- Separate PMR resistors is added for 1.8 V and 3.3 V rails going to EC.

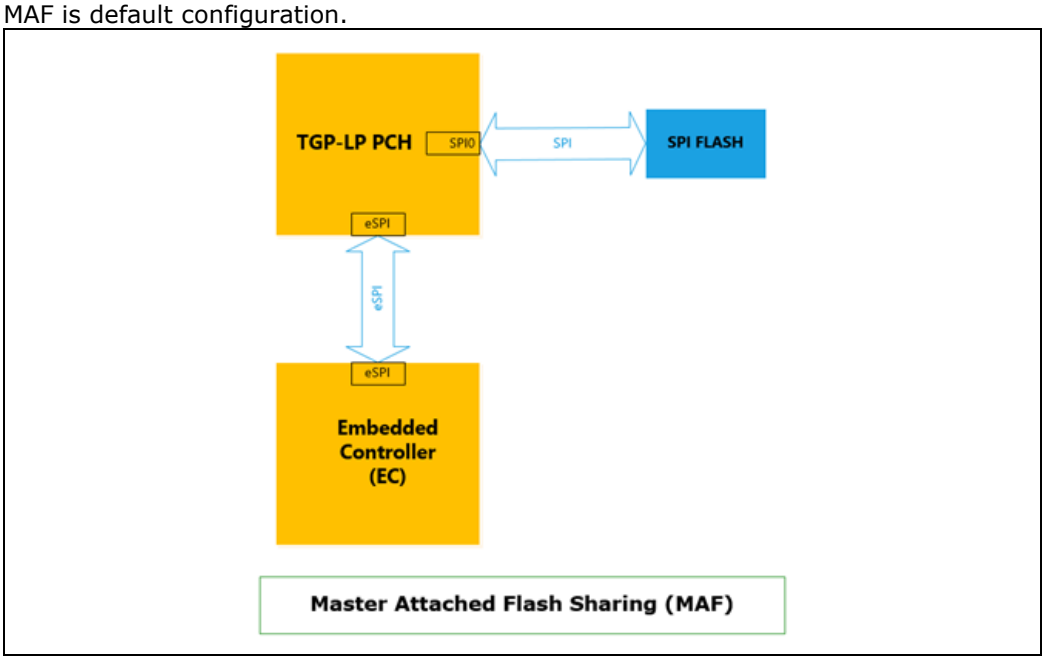
2.12.1 Embedded Controller Block Diagram



2.12.2 Master Attached Flash (MAF) Sharing

MAF is one of the Flash sharing Mechanism, where PCH is the master, which access flash over PCH SPI0 Controller and EC sharing the same flash accesses over eSPI.

MAF is default configuration.

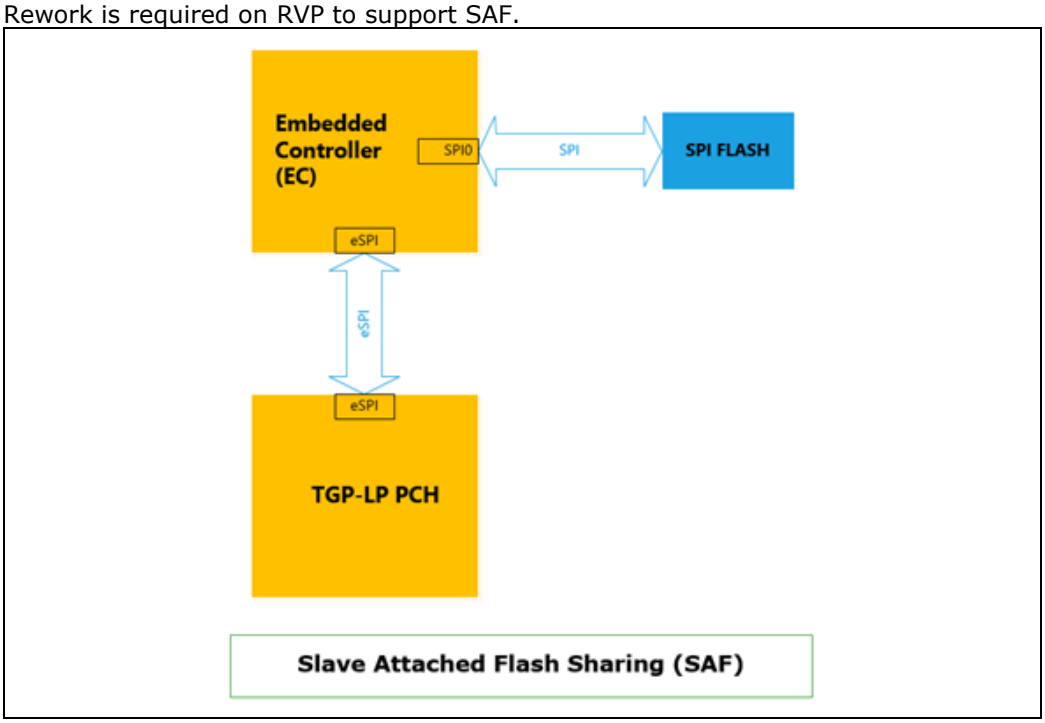


2.12.3 Slave Attached Flash Sharing (SAF)

SAF is one of the Flash sharing Mechanism, where EC is the master, which access flash over its SPI Controller and PCH sharing the same flash accesses over eSPI.

MEC1428 Microchip* Embedded Controller can support SAF mode flashing.

Rework is required on RVP to support SAF.



2.13 Debug and Validation

2.13.1 Debug Technologies

Open Chassis Debug Method:

— CPU/PCH Merged MIPI60 (Lauterbach)

Closed Chassis Debug Method:

1. **DCI OOB 4 Wire:** Over Type A PCH USB3 Port
2. **USB2.0 DbC:** USB 2.0 DbC can be used only when the target is in a UFP (device) USB role.
3. **USB3.0 DbC:** USB 3.0 DbC can be used when the target is in a DFP (host) USB role.
4. **MIPI60-to-LAI HS Adapter:** https://www.samtec.com/products/hqcd

Use the following description values: HQCD-030-04.00-TEU-STL-1.

2.13.2 Traditional XDP Support on TGL RVP

TGL RVP, by default, support MIPI60 Connector.

To support XDP/ITP blue box on TGL RVP, user must rework on board and also use MIPI60 to XDP adaptor board.

https://designintools.intel.com/product_p/itpmipi602itp60v2.htm

2.13.3 Additional Tools and Cables

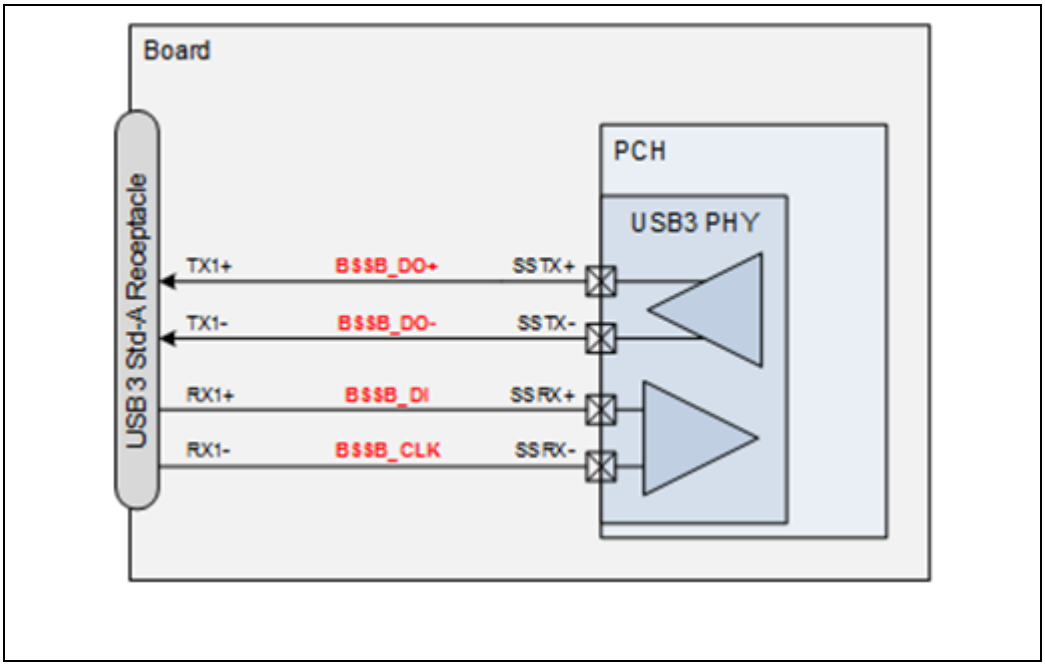
- For Lauterbach* Tools and License details.
  - www.lauterbach.com
- For Intel® Silicon View Technology Closed Chassis Adapter (also known as SVTCCA or BSSB) from below given link:
  - https://designintools.intel.com/ProductDetails.asp?ProductCode=ITPXDPSVT
- For DCI DbC2/3 A-to-C UFP Debug Cable 1.8 Meter
  - Https: //designintools.intel.com/product_p/itpdciamcm2mu.htm
- For DCI DbC2/3 A-to-A Debug Cable 1.8 Meter
  - https: //designintools.intel.com/product_p/itpdciamam2m.htm

2.13.4 Four Wire Solution with Type A

USB STD-A USB3.1 Walk-Up Port receptacle that supports a direct (no repeater/re-timer) connection to the USB 3 PHY to enable four Wire BSSB.

All the USB3.1 Walk Up ports on TGL RVP supports four Wire BSSB.

Ref-Des: J5J2, both the ports of this stacked USB 3.1 connector support four Wire BSSB.



2.14 Power Delivery Implementation Details

2.14.1 TGL UP3 RVP Power Sources

Standard AC Adapter:

An adapter with 230 W capability is selected to support power numbers of various Tiger Lake flavors (UP3 and UP4).

Type C Adapter:

Tiger Lake UP3 RVP has 4 Type C ports on the board. All these Type C ports can be used for powering the Tiger-lake Lake UP3 RVP design. By default, the priority is given to standard AC adapter.

Battery Pack:

- **TGL UP3 design**: The battery pack considered for TGL UP3 is of 3S3P type and has a capacity of 97 Whr. Maximum charger and discharge current are 8.7 A and 8 A respectively. For regular 0.5 C charging, the charging current required is 5.6 A and for 1 C fast charging, the charging current required is 8.7 A
- **Recommendation**: Use standard AC adapter for all validations. Only on need basis, use Type C adapter or battery pack.

2.14.2 TGL UP3 RVP Key PD Sub-systems

Battery Charger:

A buck boost charger is used to support the overall system power needs and also to charge the 3S3P battery pack for TGL UP3 design. The battery charger works seamlessly with both standard AC adapter and Type C adapter.

Discrete VRs:

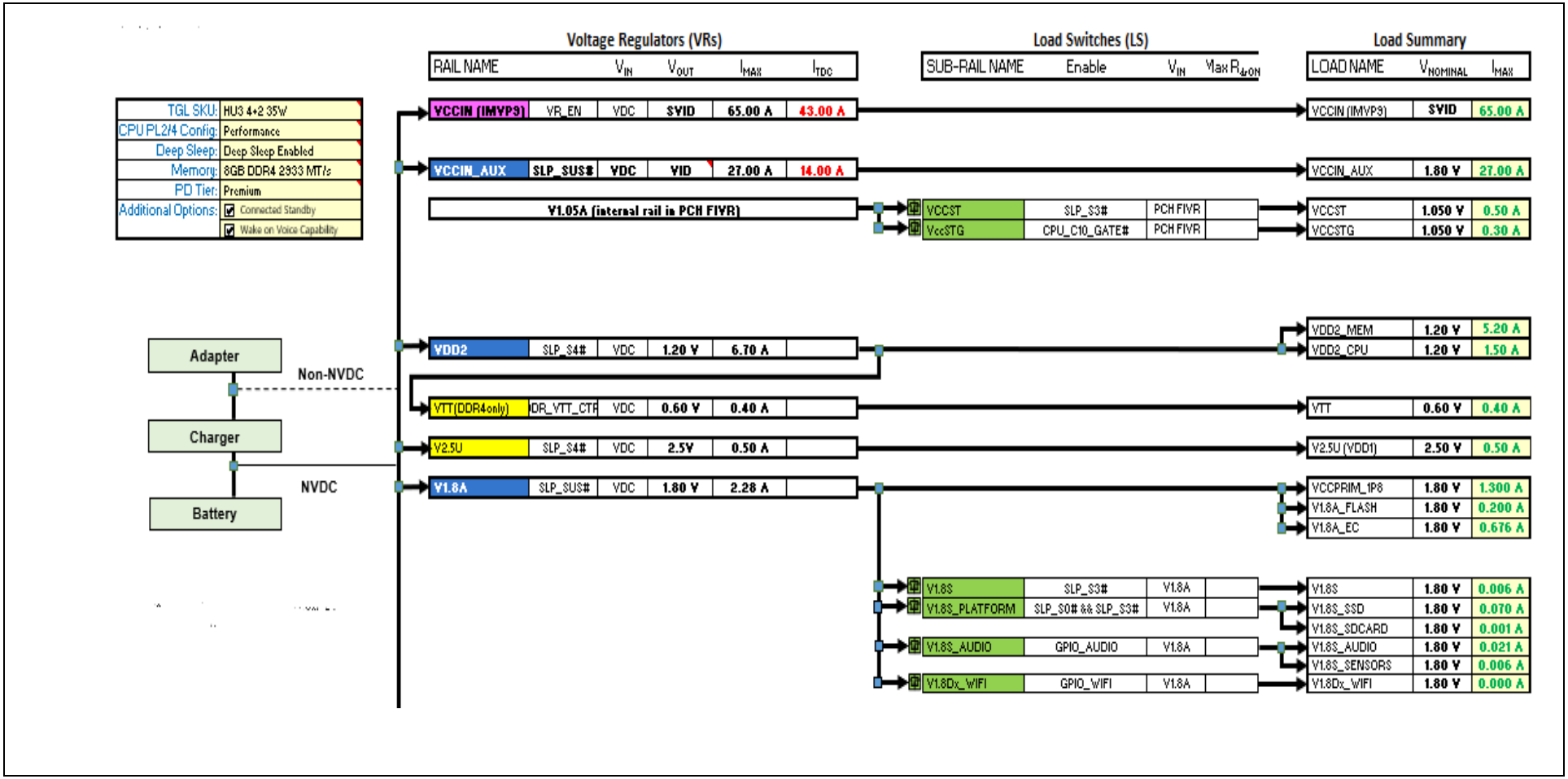
Tiger Lake UP3 RVP has discrete on-board voltage regulators to generate the rails required for powering the CPU, PCH and platform components.

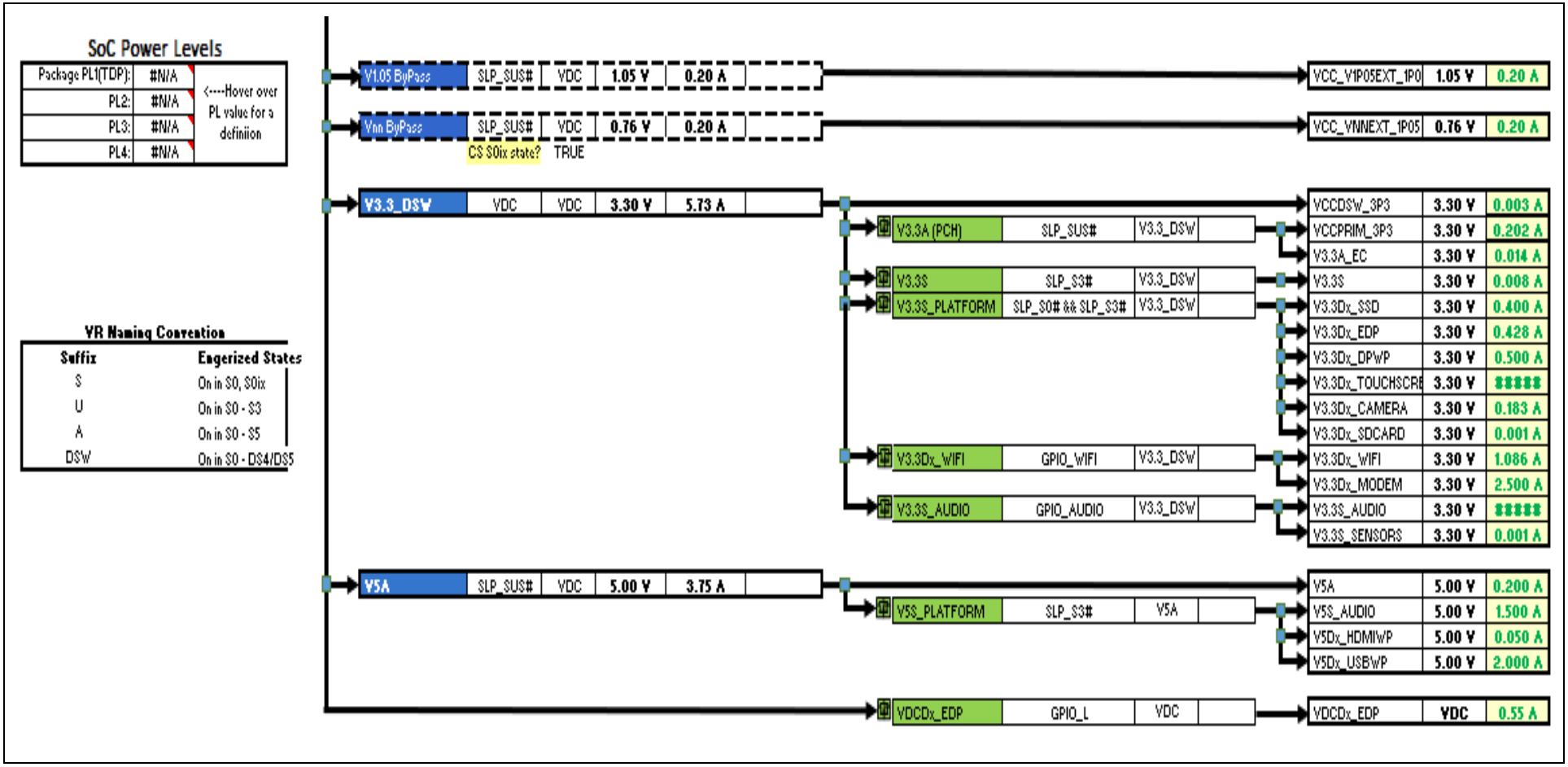
IMVP9 VRs:

Tiger Lake UP3 CPU requires to support single SVID voltage rails (VCCIN) with IMVP9 SVID protocol compliant. An IMVP9 controller from MPS (MP2940AGRT-000A for TGL UP3 design) is used to generate the SVID rail. The IMVP9 solution is down on the mother board.

2.14.3 TGL UP3 RVP Power Map

Note: Refer to TGL EDS and PDG for latest updates from Section 2.14.3 to Section 2.14.10.





Note: It is recommended to use NVDC charger and 2SxP battery for better VR performance, however traditional 3SxP battery and non-NVDC charger maybe implemented in some designs

System Rail Level Connections

LOAD NAME	Load Description	V	Icc_{Max}	ΔP_{STNDBY}*	I_{TDC}	
VCCIN (IMVP9)	FIVR input	SVID	65.000 A	0.0 - 0.0 mA	43.000 A	CPU
VCCIN_AUX	CPU and PCH merged auxiliary FIVR	1.80 V	27.000 A		14.000 A	CPU
						CPU
VCCSTG	Gated sustain voltage for processor standby modes	1.05 V	0.300 A	0.0 - 0.0 mA		CPU
VCCST	Sustain voltage + VccPLL	1.05 V	0.500 A	0.0 - 0.0 mA		CPU
VDD2_CPU	CPU VDDQ, VDDQC +VCCPLL_OC	1.20 V	1.500 A	0.0 - 0.0 mA		CPU
VDD2_MEM	DRAM VDDQ	1.2 V	5.200 A			DRAM
VDDQ_Tx	LPDDR4x and LPDDR5 only: DDR IO buffers	N/A	N/A			DRAM
V1.8U (VDD1)	LPDDR3 and LPDDR4 only:VDD1	N/A	N/A			DRAM
VTT	DDR4 only: DRAM termination	0.60 V	0.400 A			DRAM
V2.5U (VDD1)	DDR4 only: VDD1	2.50 V	0.500 A			DRAM
VCCPRIM_3P3	3.3V Primary Well	3.30 V	0.202 A			PCH
VCCDSW_3P3	3.3V for Deep Sx Well	3.30 V	0.003 A			PCH
VCCPRIM_1P8	1.8V Primary Well	1.80 V	1.300 A			PCH
						PCH
VCC_V1P05EXT_1P05	VCCPRIM_1P05 and other 1.05V Primary PCH loads	1.05 V	0.200 A			PCH
VCC_VNNEXT_1P05	PCH core	0.76 V	0.200 A			PCH
VCCRTC	Real Time Clock	3.00 V	0.005 A			PCH

VDCDx_EDP	eDP panel	VDC	0.550 A		eDP	System Devices
V3.3Dx_EDP	eDP panel	3.30 V	0.423 A			
V3.3Dx_CAMERA	Ft. Camera, Back Camera, Finger Print Sensor	3.30 V	0.133 A		Camera	
V3.3S_SENSORS	Sensors	3.30 V	0.001 A		Sensors	
V1.3S_SENSORS	Sensors	1.30 V	0.006 A			
V3.3Dx_TOUCHSCREEN	Touch Screen	3.30 V	0.200 A		Touchsc	
V3.3Dx_SSD	M.2	3.30 V	0.400 A		SSD	
V1.3S_SSD	I/O	1.30 V	0.070 A			
V3.3Dx_SDCARD	Multi-media card slot (SD/eMMC Add-in slot)	3.30 V	0.001 A		SD Card	
V1.3S_SDCARD	I/O	1.30 V	0.001 A			
V3.3Dx_MODEM	PCIE or SSIC or USB3 for 3G/4G	3.30 V	2.500 A		WWAN	
V1.3Dx_MODEM	I/O	1.30 V	0.070 A			
V3.3Dx_WIFI	WIFI/BT/GPS Radio	3.30 V	1.036 A		WIFI	
V1.3Dx_WIFI	I/O	1.30 V	0.000 A		WIFI	
V5S_AUDIO	Analog	5.00 V	1.500 A		HD Audio	
V3.3S_AUDIO	Core	3.30 V	0.200 A			
V1.3S_AUDIO	I/O	1.30 V	0.021 A			
V3.3A_EC	Embedded Controller	3.30 V	0.014 A		Embedd ed Controll	
V1.3A_EC	Embedded Controller (eSPI)	1.30 V	0.676 A			
V5Dx_USBWP	USB Wakup ports (2)	5.00 V	2.000 A		Wakup Ports	
V5Dx_HDMIWP	HDMI Wakup Port	5.00 V	0.050 A			
V3.3Dx_DPWP	DP 1.3/1.4 Wakup Port	3.30 V	0.500 A			
V1.3A_FLASH	BIOS Flash	1.30 V	0.200 A		Flash	
V1.3S	Misc components	1.30 V	0.006 A		Misc	
V3.3S	Misc components	3.30 V	0.003 A			
V5A	Misc components & VRs	5.00 V	0.200 A			
Total			113.130 A			

2.14.4 TGL UP3 RVP Voltage Levels of Critical Rails

Voltage Rail/ Voltage Regulator	Default Voltage Level	Comments
+V3.3 A_DSW	3.3 V	
+V5A_DS3	5.0 V	
+V1.8 A	1.8 V	
+VCCIN AUX	0V/1.1V/1.65V/1.8 V	Boot voltage =1.8 V
+VDD1	2.5V/1.8 V	Depends on the memory type (DDR4: 2.5V; LP4x/ LP5: 1.8 V)
+VDD2	1.2/1.1/1.05 V	Depends on the memory type (DDR4: 1.2V; LP4x: 1.1V; LP5: 1.05 V)
+V_VDDQ_VTT	0.6 V	Half of the DDR voltage (Only for DDR4), **NOTE:** This rail is available only TGL UP3 DDR4 SKU
+VDDQ_Tx	0.6/0.5 V	For LP4x :0.6 V and LP5:0.5 V
+VNN_BYPASS	0.78 V	1.05 V in S3 and lower system state. Applicable to power optimized SKUs only.
+VCCIN	0V (Boot Voltage)	CPU adjusts the output voltage through SVID.
+V1.05_BYPASS	1.05 V	Applicable to power optimized SKUs only.
+VCCST_CPU / +VCCSTG_CPU	1.05 V	Derived from PCH FIVR
+VCC_MODPHY / +VCC_ISCLK	1.05	Derived from PCH FIVR. **NOTE:** These rails available in only TGL UP4 design.

2.14.5 System State Overview

Tiger Lake supports the following system states and detailed voltage rail information. By default, all the SKU support Deep-Sx.

System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wake-up on PCH).
G2/S5	Soft off. All power lost (except wake-up on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

2.14.6 TGL UP3 RVP Power States Map

VR Rail Gated Rail	Enable	Voltage	S0 (Active)	S0 (C10)	S0i3	S3	S4	S5	DS5	G3
+VCCIN	ALL_SYS_PWRGD	SVID	ON	0V (PS4)	0V (PS4)	OFF	OFF	OFF	OFF	OFF
+V_VDDQ_VTT	DDR_VTT_CNTRL	0.60 V	ON	ON	ON/ OFF	OFF	OFF	OFF	OFF	OFF
+VNN BYPASS	VCCIN AUX PWRGD	0.78 V	ON	ON	ON	ON	ON	ON	OFF	OFF
+VDD2	VPP_VR_PWRGD	1.20 V	ON	ON	ON	ON	OFF	OFF	OFF	OFF
+VDD1	SLP_S4#	2.50 V/ 1.8 V	ON	ON	ON	ON	OFF	OFF	OFF	OFF
VDDQ_Tx	VDD2_VR_PWRGD	0.6 V/ 0.5 V	ON	ON	ON	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX	V1.8A_PWRGD	1.8 V	ON	ON	ON	ON	ON	ON	OFF	OFF
+VCCST_CPU	SLP_S3# OR VCCST override OR VCCIN AUX VID 0,1	1.05 V	ON	ON	ON	ON	OFF	OFF	OFF	OFF
+VCCSTG	CPU C10 GATE OR VCCST override OR VCCIN AUX VID 0,1	1.05 V	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
+V1.8A	SLP_SUS#	1.80 V	ON	ON	ON	ON	ON	ON	OFF	OFF
+V5A_DS3	SLP_SUS# Or EC_DS4 Or SLP_S4# Or EC_DS3	5.00 V	ON	ON	ON	ON	ON	ON	ON	OFF
+V5A	SLP_SUS#	5.00 V	ON	ON	ON	ON	ON	ON	OFF	OFF
+V5S	SLP_S3#	5.00 V	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
+V3.3A_DSW	VBATA	3.30 V	ON	ON	ON	ON	ON	ON	ON	OFF
+V3.3A	SLP_SUS#	3.30 V	ON	ON	ON	ON	ON	ON	OFF	OFF
+V3.3S	SLP_S3#	3.30 V	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
+V3.3A_DS3	SLP_SUS# Or EC_DS4 or SLP_S4# Or EC_DS3	3.30 V	ON	ON	ON	ON	ON	ON	ON	OFF

2.14.7 TGL UP3 RVP Sequencing Details

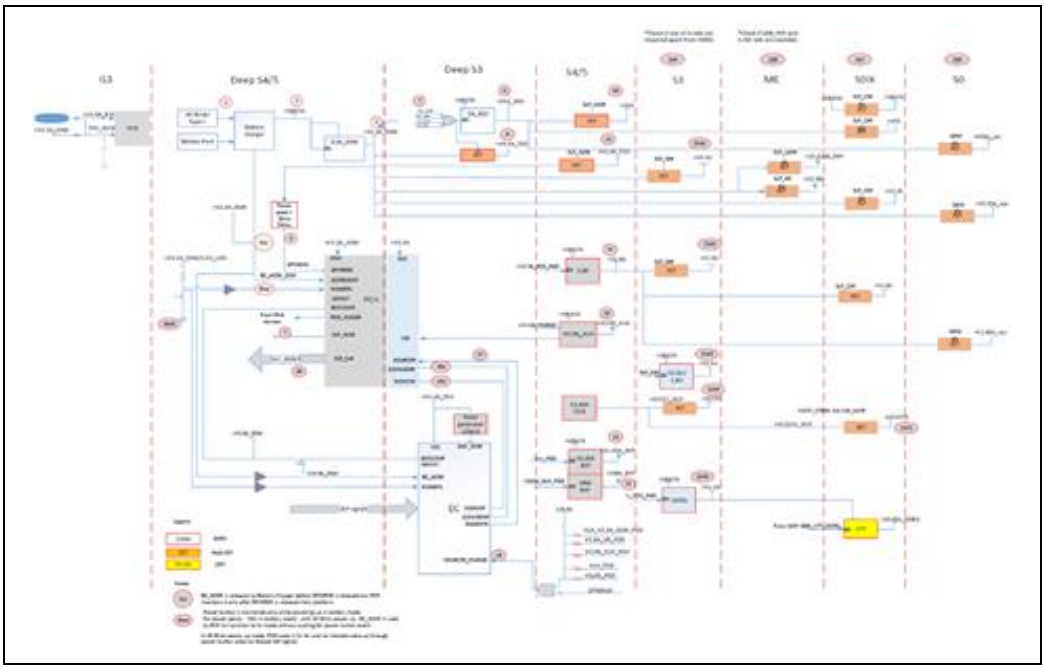
Power Sequencing Details:

- Tiger Lake UP3 CPU have FIVR. IMVP9 rail (SVID compliant) feeds power to CPU only and a VID capable voltage regulator for VCCIN AUX feeds power to both PCH

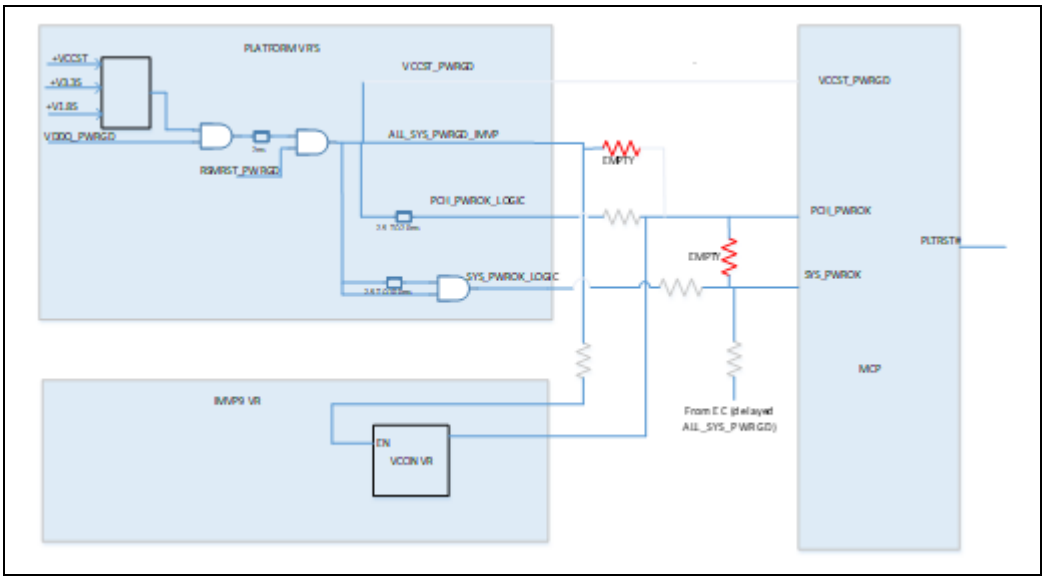
and CPU. VCCST and VCCSTG rails power gate input are supplied from PCH FIVR output feeding back to CPU.

- IMVP9 voltage regulators are enabled by ALL_SYS_PWRGD signal, which indicates all the platform rails along with VCCIN AUX are stable.
- IMVP9 VR has boot voltage requirement of 0 V and VCCIN AUX VR has boot voltage requirement of 1.8 V.
- SVID communication is required to change the voltage of IMVP9 VRs. Max. VID voltage on the platform is limited to 2.2 V over SVID for IMVP9 rail.
- PCH FIVR rail (VCCIN AUX) requires supporting four different Voltage levels. Each voltage level is set through the GPIOs from PCH as needed.

2.14.8 TGL UP3 RVP Sequencing Block Diagram



2.14.9 TGL UP3 RVP Sequencing Block Diagram (Cont.)



2.14.10 TGL UP3 RVP Power Source Priority

Available Sources	Priority Given To
Standard AC Adapter	Standard AC Adapter
Type C Adapter *	Type C Adapter
Battery Pack	Battery Pack
Standard AC Adapter + Type C Adapter	Standard AC Adapter
Standard AC Adapter + Type C Adapter + Battery Pack	Standard AC Adapter

2.15 Quick Start

Required Peripherals:

- MCP socket and MCP
- Heat sink assembly for MCP
- DDR4 SoDIMM Memory modules
- Mobile 19 V AC Brick
- Keyboard, Mouse (PS2/USB)
- Hard disk drive or M.2 SSD
- PCI Express* Graphics Card – for Silicon with no GFx support
- External display (Example: eDP, DP, HDMI)
- SF600 programmer for BIOS programming
- uAB cable for debug log

2.15.1 Board Bring Up Steps

Make sure all peripherals mention in the previous foil is available before starting board bring up

Step 0:

Go to the TGL RVP Rework tracker to know all applicable rework for board.

Step 1:

Place the processor (RefDes: U4E1) with socket and the hardware assembly (make sure to align the chip to the pin 1 marking).

Step 2:

Insert DDR4 DIMM modules into stacked SO-DIMM connector (RefDes: J2C3 and J2C4).

Step 3:

Verify presence of RTC coin cell in Battery Holder (RefDes: BH9J1).

Step 4:

Insert hard disk drive in SATA direct connect (RefDes: J9C1) or PCIe*/SATA based SSD in M.2 socket 3 (RefDes: J7R1 [M.2 PCH SSD] or J7A3 [M.2 CPU SSD conn]).

Step 5:

Connect display. It can be either eDP (RefDes: J5B1) or HDMI (RefDes: J4A1). If initial silicon does not support graphics then use PCIe* slot connector (RefDes: J7B1) with the help of external graphics card.

Step 6:

a. Connect a PS/2 keyboard in J4J3 (bottom) or a USB keyboard in one of the default USB Walkup ports.
b. Connect a PS/2 mouse in J4J3 (top) or a USB mouse in one of the default USB Walkup ports.

Step 7:

Insert dediProg (RefDes: J4H2) and follow the steps to flash IFWI image (EC+BIOS merged image).

Step 8:

Connect the AC brick or battery pack or Type C adapter to provide power to board.

Step 9:

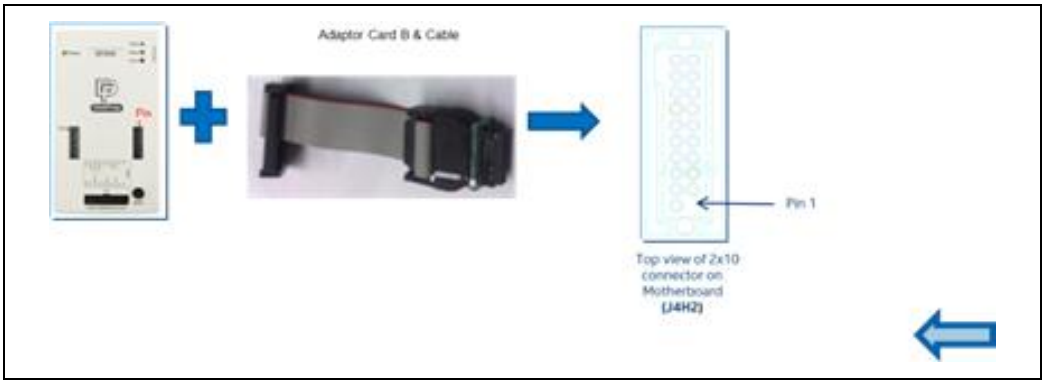
a. As the system boots, press F2 to enter the BIOS setup screen.
b. Check time, date, and configuration settings. The default settings should be sufficient for most users with the exception of Intel® Speed Step Technology. This feature is disabled by default and can be enabled in setup.
c. Save and Exit the BIOS setup.

d. The system boots and is ready for use.

2.15.2 SF600 Programming

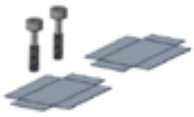
1. Can be programmed in Single I/O mode as well as quad mode for more speed.
2. Connect Dediprog SF600 to header at RefDes: J4H2.
3. Launch the Dediprog tool and confirm the settings from config → miscellaneous settings → Quad IO option → Enable Quad IO. Default is single I/O.
4. Ensure that "currently working on" is in "Application Memory Chip 1". For TGL, single 32 MB chip is PoR.
5. Ensure no separate images for BIOS and EC. It is a single merged IFWI image.
6. Go to **File** and select the .bin file to program chip1.
7. Execute the batch operation to erase and program the chip.

Note: For SF600 programmer and top side connector of Adaptor Card, which connect to programmer: Pin 1 at top left.



2.16 TGL UP3 A0 - Heatsink Retention Solution

2.16.1 Mechanical Parts Overview

QTY	DESCRIPTION	PART PICTURE
1x	➢ Board Plates Assy 1x Stiffener Plate 1x Back Plate 1x Insulator 4x Screws ➢ Load System w/Heatsink ➢ A0 Pusher **Color Black**	
1x	ISC Socket, 1499BGA NSP MAX CYCES:30	
1X	**SPARES:** **J98755-001_302** VcTIM **J93703-001_104** Screw M3 for stiffener	

2.16.2 Required Tools and Consumables

ITEM	DESCRIPTION	PART PICTURE
1	Torque Screwdriver ¼"HEX Drive	
2	Isopropyl Alcohol Wipes Vendor: POLIWATER PN: FO-1	
3	2.5mm Hex Bit, ¼" Hex Shank Suggestion: McMaster PN: 7389A22	

2.16.3 PIN-1 Indicators

2.16.4 TGL UP3 Interposer Hardware Installation

STEP 1

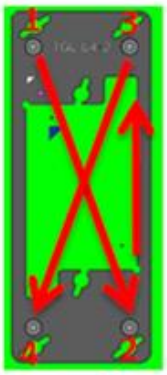
-Matching the board pin1 and pin1 corners

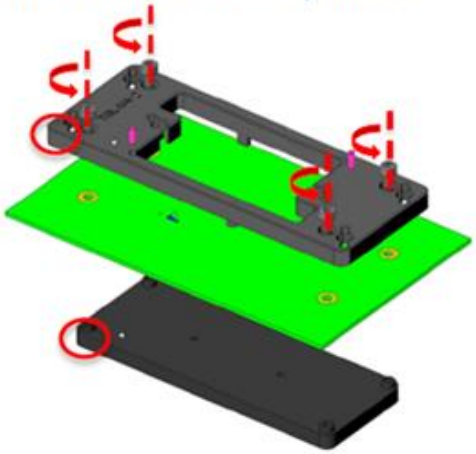
-Align back plate and stiffener holes with the 4 mounting holes on the board.

-Tighten the four screws two turns at a time in a cross pattern

Torque: 6in-lb

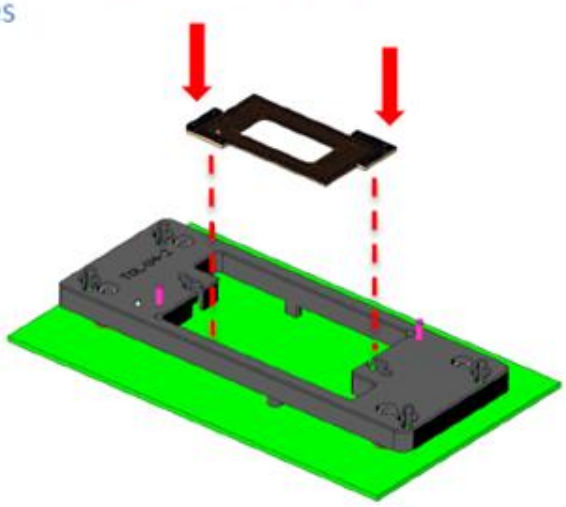
Bit Hex: 2.5mm





STEP 2

Matching pin-1 marks, place ISC Socket on the board by inserting the Socket alignment pins (2X) into the board alignment holes

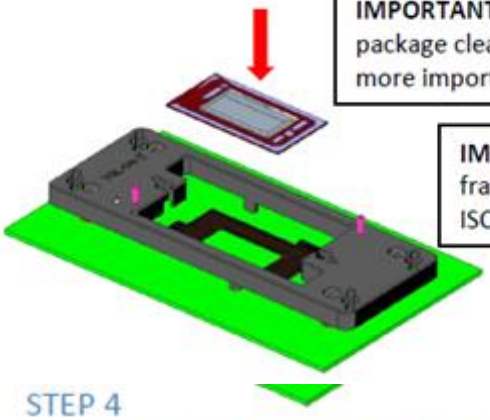


STEP 3

Place TGL-U package on top of the ISC socket. Don't forget matching pin1

IMPORTANT: Before place the silicon package clean the socket using air (it's more important after a couple of cycles)

IMPORTANT: Handle the elastomer by frame only. Do **NOT** touch the pads
ISC SOCKET- MAX CYCLES: 30



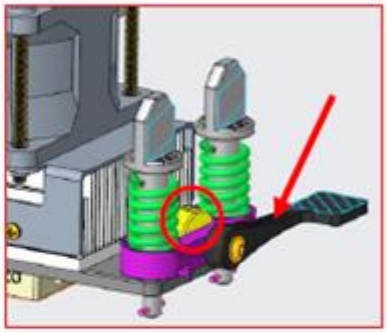
STEP 4

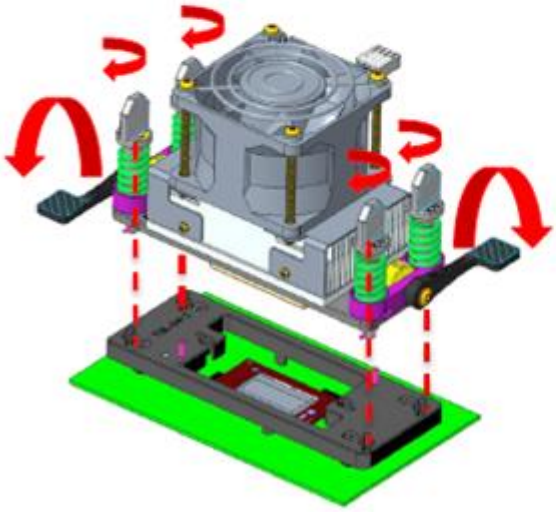
-Matching pin-1 corners, align and place heatsink assembly using the four plungers and dowel pins on the top plate.

-levers have to be in unlooked position, check cam and lever label before activate them

-Turn plungers to lock position

-Activate two levers **at same time,** locked label has to be shown





END OF INSTALLATION

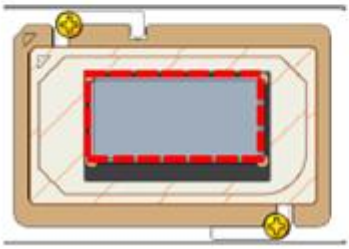
2.16.5 Cooper Shim Installation

ADDITIONAL STEP

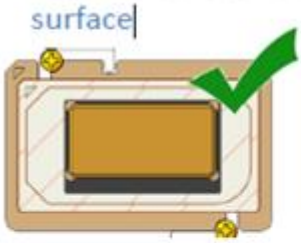
-Cooper shim upgrade: It is not part of the retention hardware kit, it will delivery in separate package. If you don't receive the it please contact the Mechanical Engineer

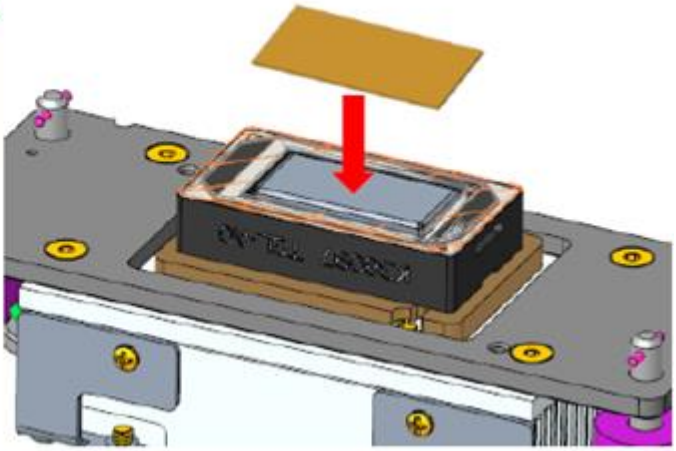
-Taking the adhesive protective cover off

-Align it in direction of the VCTim area



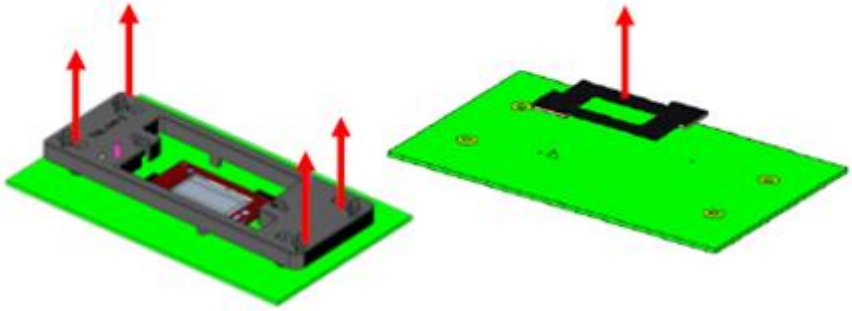
-Stick it on the VCTim and verify it cover all the VCTim top surface



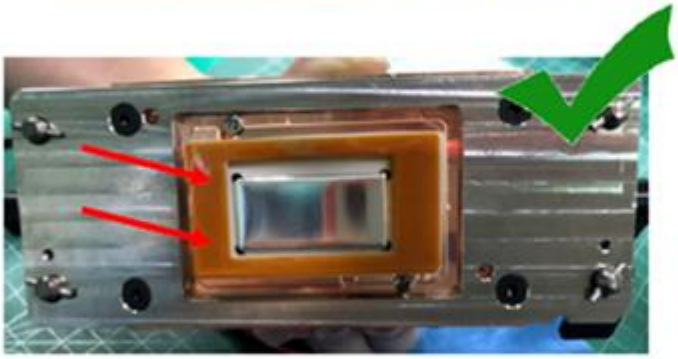


2.16.6 Heads Up

- Remove stiffener plate first if you want to replace the socket to avoid any damage in the socket alignment pins.
  Socket replacement has to be in straight line up



- TGLU A0 hardware has a kapton sheet on the pusher area to protect silicone surface and avoid sticky area touch the silicon substrate
  Please don't remove it, if so pusher will stick on the silicon



2.16.7 Troubleshooting

If the assembly is not working properly:

1. Disassemble the Heatsink and Retention HW.
2. Check the ISC Socket and package orientation.
3. Inspect the socket alignment on the board.
4. Clean the pads on the board with an alcohol wipe.

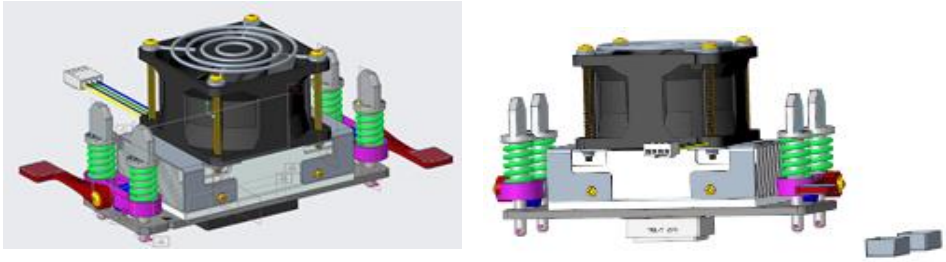
5. Check for foreign particles on the ISC Socket and if necessary clean with compressed air.
6. Inspect the pusher and rubber+kapton area.
7. Reassemble by following the instructions properly.

2.17 TGL UP3 270 um Rework Strategy

2.17.1 Package Identification

- Additional markings are being placed on stiffener to identify 270 um units.
- Proposed Solution

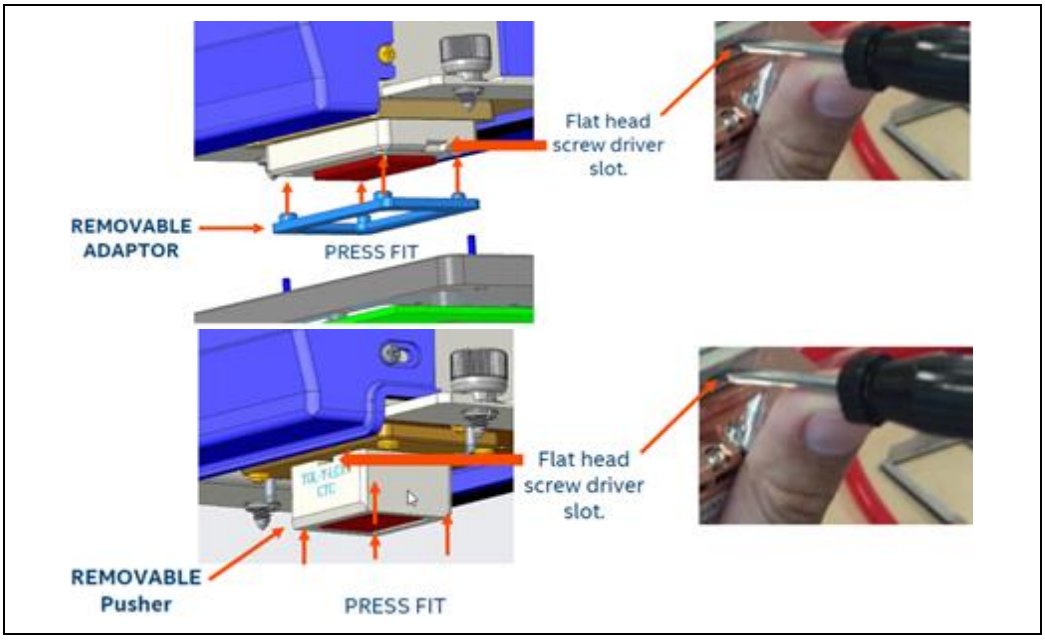
2.17.2 TGL UP3 Heatsink/Retention Strategy: Upgrade Kits



- Upgrades boot kit to support 270um.
- Contains heatsink assembly and updated pedestal for 270um die.
- Does not contain board mounting components (stiffener and back side support)
- Easily identifiable by red lever latch handles and 270 sticker above Pin 1

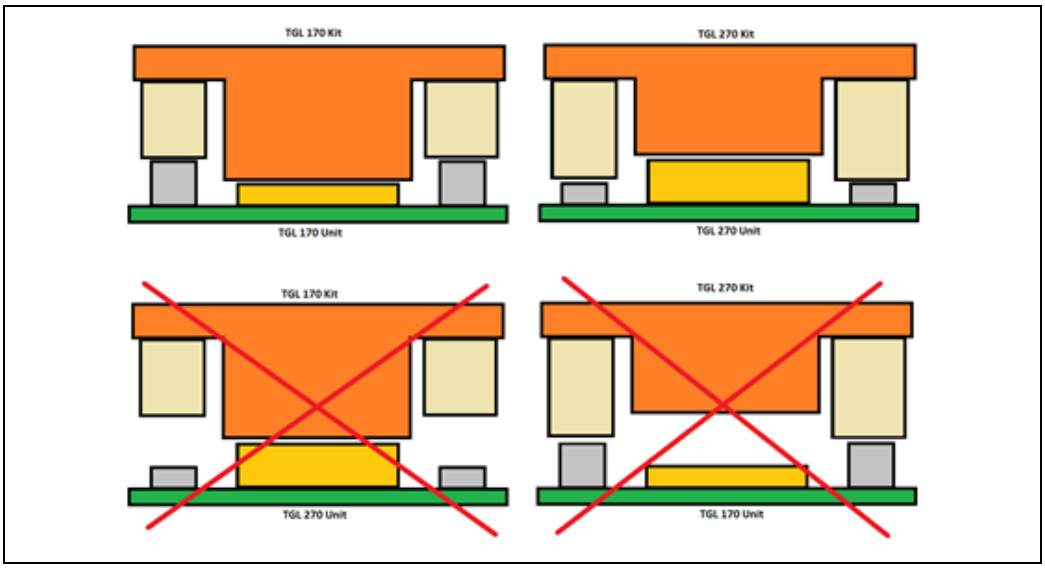
- This will enable labs to transition back and forth between 170um and 270um units easily.
  - Risks associated with wrong heatsink/unit combo include thermal run-away, open/shorts
  - Risk of die crack with 170 um HW with 270 um package exists,but deemed low.

2.17.3 TGL UP3 Thermal Tool Strategy



- Rework Effort: Replace Pusher Adapter or entire Pusher depending on the configuration.

2.17.4 TGL UP3 270 Risks



Risks associated with wrong heatsink/unit combo include thermal run-away, socket connection issues, and potential die crack

- TGL 170 Units with TGL 270 HW:
  - This will create an instance where there is no contact between the heatsink/thermal tool and the die
  - Result: Thermal Run-away
- TGL 270 Units with TGL 170 HW:
  - This will create an instance where there is no contact with the substrate
  - Result: Open socket issues
  - Slight risk of Die Crack.

2.18 BackUp

2.18.1 EC Error Code Indication

Error Type	Error Code	Caps Lock LED (DS9H2)	Scroll Lock LED (DS7G1)	Num Lock LED (DS9J1)
No Error	0	Off	Off	Off
RSMRST_PWRGD_N	1	Off	Off	Flash
PM_SLP_S5_N	2	Off	Flash	Off
PM_SLP_S4_N	3	Off	Flash	Flash
PM_SLP_S3_N	4	Flash	Off	Off
PM_SLP_M_N	5	Flash	Off	Flash
ALL_SYS_PWRGD	6	Flash	Flash	Off

Error Type	Error Code	Caps Lock LED (DS9H2)	Scroll Lock LED (DS7G1)	Num Lock LED (DS9J1)
PLT_RST_N	7	Flash	Flash	Flash
DOCK_SYS_PWRGD_N	8	On	On	Flash
SUSWARNB	9	On	Flash	On
NOTE: KSC Thermal Shutdown is indicated by flashing of Num _Lock and Caps _ Lock LEDs alternatively. DS7G1 acts as led indication for error code in case of any error otherwise works as power button LED				

2.18.2 Jumpers on TGL UP3 DDR4 RVP

RefDes	Jumper Description	Default
J1A3	MIPI60_OVERRIDE_N	'1-X'
J2H3	MIPI60_PRESENT1_N	'1-X'
J1C1	TYPEC_DISABLE	'1-X'
J1F3	NO REBOOT STRAP	'1-X'
J1F4	FLASH DESCRIPTOR SECURITY OVERRIDE STRAP	'1-X'
J3B1	SVID DISABLE STRAP	'1-X’
J2F1	A0 PERSONALITY STRAP	'1-X'
J3H1	DDI3_HPD	'1-X'
J9J5	BT_RF_KILL_N, WIFI_RF_KILL_N	'1-X,3-X'
J9J4	CNVI Disable	'1-2'
J8J3	PROCHOT_EC JPR	'1-X'
J9J3	SMC_RST_N JPR	'1-X'
J9J2	SMC_LID JPR	'1-X'
J8D2	SVID CLOCK	'1-2,3-X'
J8D3	SVID ALERT	'1-2,3-X'
J8D4	SVID DATA	'1-2,3-X'
J8G3	PCH GLITCH ISSUE MITIGATION	'1-X'
J7G1	SRTC/RTC CLEAR CMOS JPR	'1-X'
J7H2	SPD_PRSNT JPR	'1-2'
J8H3	FRU SMB_CLK_S3	'1-2'
J8H5	FRU SMB_DATA_S3	'1-2'
J6J1	PECI_MUX_CTRL_SNI_R	'1-X'
J8J1	FRU POWER SUPPLY	'1-2'
J6G4	H_PECI_CPU JPR	'1-X'

RefDes	Jumper Description	Default
RefDes	Jumper Description	Default
SW4V1	MIPI60 FN[0:3]	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW5V1	1 - VDDQ_VR_PWRGD - IMVP_VR_EN 2 - ALL_SYS_PWRGD - IMVP_VR_EN 3 - SATAXPCIE_0_SATAGP_0_R 4 - BIOS_REC	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW6J2	1 - EC_SHD_CS_SW 2 - NC 3 - RETIMER_BYPASS_STRAP 4 - ESPI_TESTCRD_DET	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW9C1	1 - BUF_PLT_RST_1.8 - WF_CAM_RST_N 2 - WF_CAM_RST_ND - WF_CAM_RST_N 3 +V1.8A - XTAL_SEL1_J 4 +V3.3A - XTAL_IN_J	1-8(OFF); 2-7(ON); 3-6(OFF); 4-5(OFF)
SW8W1	1 - PNP_NPNP_SKU 2 - VIRTUAL_DOCK_DET_N 3 - VIRTUAL_BATTERY 4 - FLIP_TO_TABLET_MODE	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)

2.18.3 TGL UP3 DDR4 RVP LED Indication

RefDes	LED Description
DS4G1	V1P05_CTRL
DS4G2	VNN_CTRL
DS8H5	S3 STATE
DS8H3	S4 STATE
DS8H4	S5 STATE
DS8H2	DSW STATE
DS8H1	M0/M3 STATE
DS3H1	ME PWR Gate

RefDes	LED Description
DS8G6	SLP S0 LED
DS8G4	PWRGD
DS8G5	CATERR
DS6G1	C10 GATE
DS6G2	CS INDICATE

RefDes	LED Description
DS8H6	CAPS LOCK
DS8H7	NUM LOCK
DS7G1	POWER BUTTON
DS7H1	BAT STATUS LED

RefDes	LED Description
DS9B1	SATA Direct connect DEVSLP
DS9E1	M.2 SSD DEVSLP
DS8G7	SATA ACTIVITY
DS6D1	PCIE* LINK DOWN
DS4G4	WLAN
DS4G3	BT®
DS7D1	WWAN

2.18.4 CPU and PCH Straps

For list of CPU and PCH Straps, refer to TGL EDS and PDG.

2.18.5 TGL UP3 RVP PCIe* Slots

Description	Refdes
x4 PCIe* SLOT PCIE_64P_KEYC_2M	J7B1
X1 PCIe* SLOT	J8B1

2.18.6 CRD Camera AOB Pinout

RVP CRD Connector Pin Number	Pin Functionality		RVP CRD Connector Pin Number	Pin Functionality
60	GND		59	3.3 V Flash supply
58	CSI_LANE1_DP		57	3.3 V Flash supply
56	CSI_LANE1_DN		55	3.3 V Flash supply
54	GND		53	GND
52	CSI_LANE2_DP		51	GND
50	CSI_LANE2_DN		49	GND
48	GND		47	2.7 V-2.8 V Power Supply (AVDD)
46	CSI_CLK1_DP		45	GND

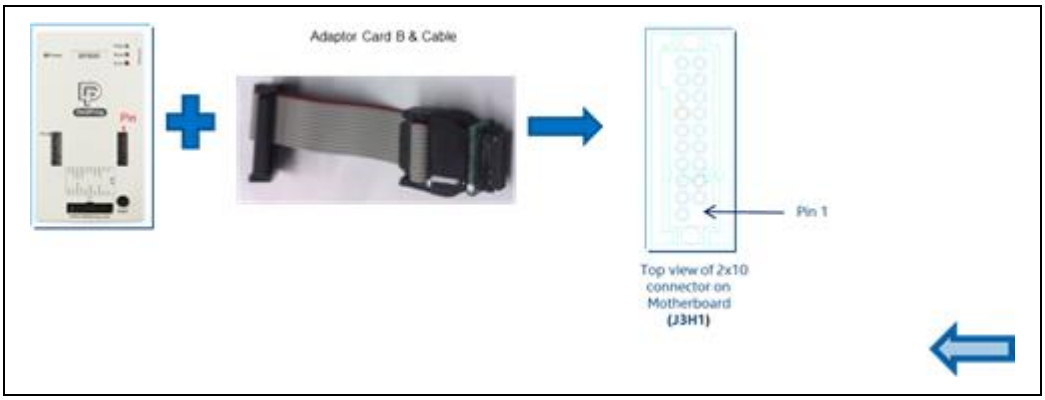
RVP CRD Connector Pin Number	Pin Functionality		RVP CRD Connector Pin Number	Pin Functionality
44	CSI_CLK1_DN		43	1.8 V Power Supply (DOVDD)
42	GND		41	1.8 V (Ungated Power supply +V1.8S)
40	CSI_LANE3_DP		39	0.9-1.2 V power Supply (DVDD)
38	CSI_LANE3_DN		37	GND
36	GND		35	2.8 V Power Supply (AF_VDD)
34	CSI_LANE4_DP		33	GND
32	CSI_LANE4_DN		31	Sync Stereo OUT
30	GND		29	Sync Stereo IN
28	CSI_CLK2_DP		27	CRD I2C Clock
26	CSI_CLK2_DN		25	CRD I2C DATA
24	GND		23	Flash Triger
22	SPI_CS		21	Power On (GPIO)
20	SPI_MOSI		19	Reset (Active low GPIO)
18	SPI_MISO/I2C_SDA		17	Clock Enable GPIO
16	SPI_CLK/I2C_SCL		15	Privacy Led
14	GND		13	Imaging_REF_CLK1
12	Power_ON2/TX_SYNC_PULSE		11	GND
10	PMIC_A1		9	ALTEK_CLK/REF_CLK2
8	PMIC_A0		7	ALTEK_INTERRUPT/CLK_EN2
6	FLASH_LED0		5	0.9V_ALTEK
4	FLASH_LED1		3	GND
2	+V5P0_BOOST		1	ALTEK_RESET/GPIO_RST2

2.18.7 SPI through Dediprog SF600

DediProg's SF600 programmer is used for programming the SPI Flash on the RVP platform.QUAD I/O mode of programming is for faster speeds along with Dual I/O mode as well as Single I/O mode.

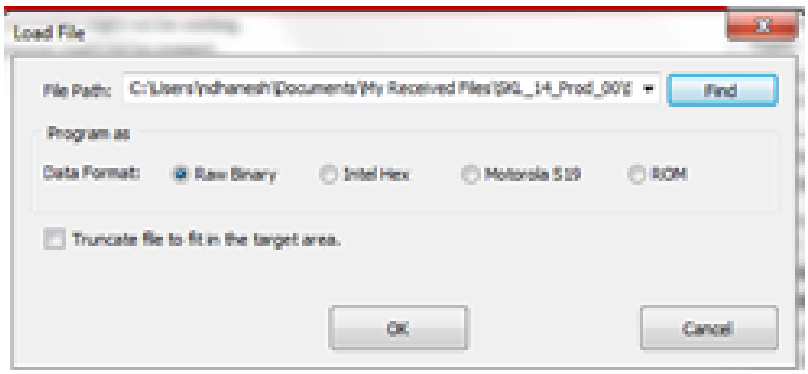
Latest version of the DediProg firmware can be downloaded from the DediProg's website

Note: For SF600 programmer and top side connector of Adaptor Card, which connects to programmer: Pin 1 at top left.

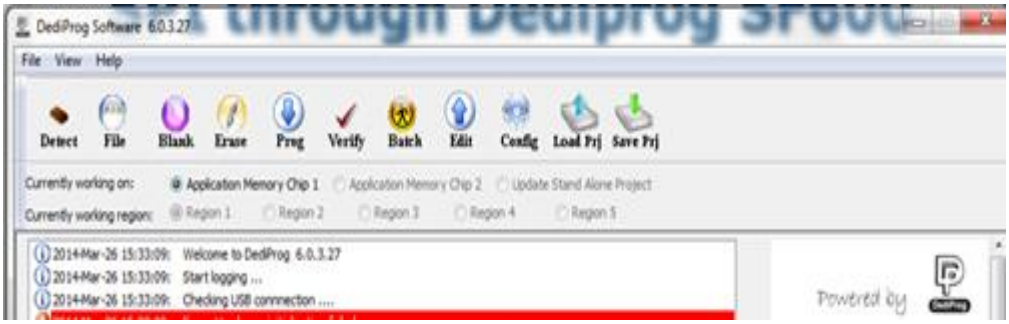


Programming:

1. **Location**: Identify the position of SPI connector for programming the BIOS on board. Make sure the AC power is off before continuing.
2. **Connect Dediprog**: Connected Dediprog cable to Dediprog Header, J4G1. Ensure orientation is correct i.e. Pin 1 of header is connected to Red strap of cable.
3. **Launch Dediprog Software**: Launch Dediprog software from Start->Dediprog->SF600->Dediprog Engineering after installed.
4. **Dediprog Software**: Make sure the program is able to detect correct type of SPI. In this example, W25R256JVEIQ is used. SPI can be damaged, if program with different algorithm. Good practice to restart the program, when different board is used. Verify that "Application Memory Chip" is selected.
5. **Load File**: After blank check operation is completed without problem, click **File**. Find and open the file. If the suffix is .bin, select Data Format: **Raw Binary**. Finally, click **Ok**.



6. **Batch**: Click **Batch**.


DediProg Software 6.0.3.27
File View Help
Detect
File
Blank
Erase
Prog
Verify
Batch
Edit
Config
Load Prj
Save Prj
Currently working on:
Application Memory Chip 1
Application Memory Chip 2
Update Stand Alone Project
Currently working region:
Region 1
Region 2
Region 3
Region 4
Region 5
2014-Mar-26 15:33:09: Welcome to DediProg 6.0.3.27
2014-Mar-26 15:33:09: Start logging ...
2014-Mar-26 15:33:09: Checking USB connection ....
Powered by

§§

3 RVP Reworks

3.1 Mandatory Reworks

3.1.1 Rework to Enable 3.3V SPI Voltage Selection

Description: This rework is required to enable 3.3V SPI, and to enable quad mode SPI. Due to the intruder functionality, the SPI voltage select is not sampled correctly.

Impact if not done: SPI Flash does not function. Post rework, Intruder functionality does not work.

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LP4x RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191101, IPTL191301, IPTL191601, and, IPTL191702.

For the Schematic reference description and layout snapshot, refer to Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit (#609003).

Table 3-1. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R8G9	RES D, 0402,0.0 Ohm, 5.00%, 1/10W	NA
Stuff	Resistor	R8G15	NA	RES D, 0402, 1Meg Ohm, 5.00%, 1/10 W
Set	Jumper	J8G1	NA	Jumper setting (1-2)

Figure 3-1. Schematic Snapshot

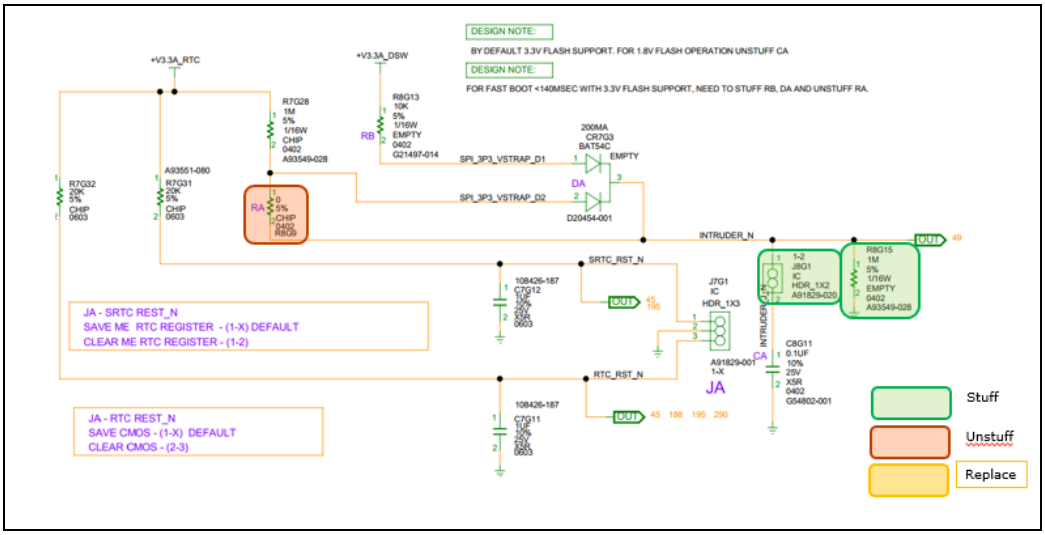
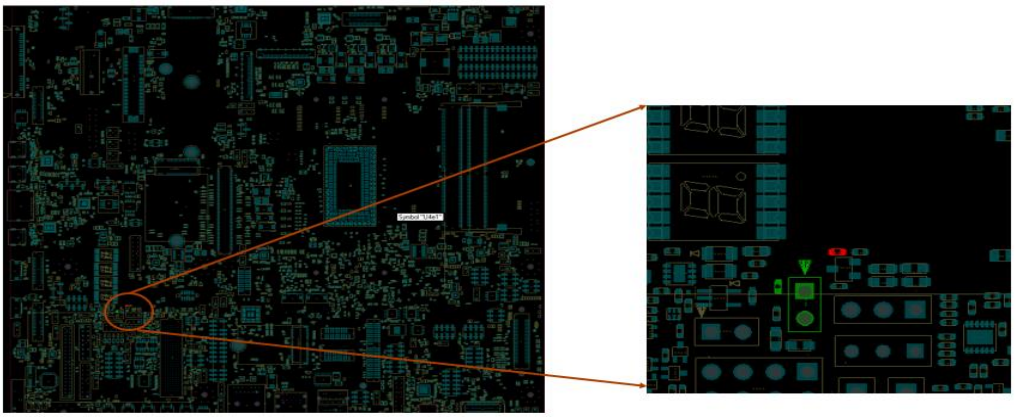


Figure 3-2. Layout Snapshot (Top Layer)



3.1.2 Rework for BOOT HALT to Sample Correctly

Description: The boot halt voltage is sampled incorrectly due to weak pull up.

Impact if not done: Boot halt strap does not sample correctly. System may not boot.

Details: SMD Resistor rework.

Applicable To: TGL UP3 RVP boards.

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, and IPTL191101.

The Schematic reference description and layout snapshot, refer to Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit (#609003).

Table 3-2. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R3G68	RES 0402, 100K, 5%	RES 0402, 4.7K, 5%

Figure 3-3. Schematic Snapshot

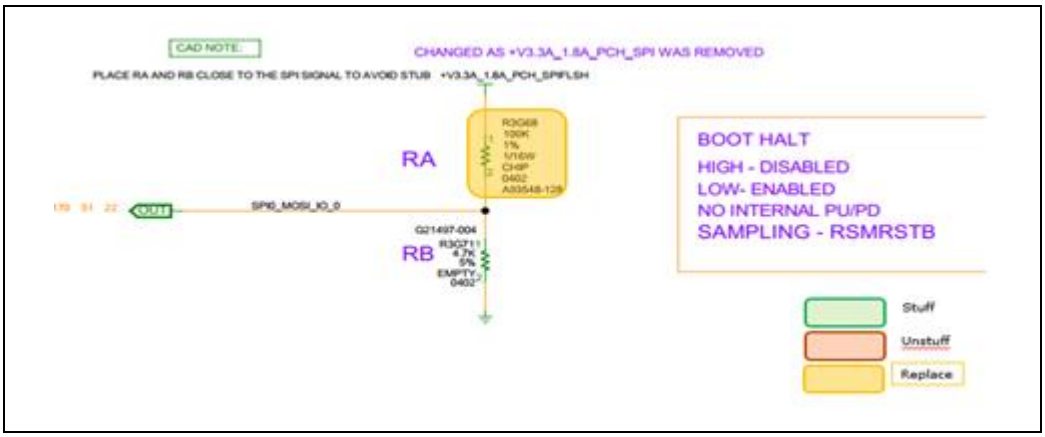
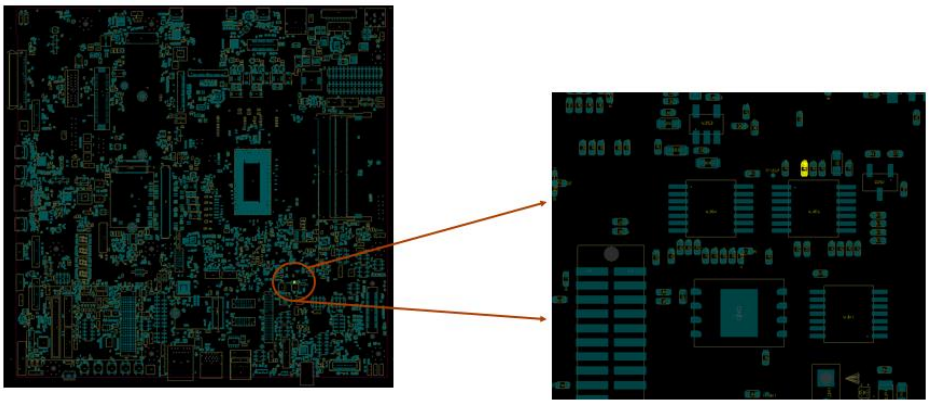


Figure 3-4. Layout Snapshot (Top Layer)



3.1.3 Rework to Enable ES-2 Codec on TGL UP3 DDR4 RVP

Description: This rework is required to enable ES2 AUDIO CODEC and to avoid CODEC getting damaged.

Impact if not done: Audio Codec does not function.

Details: SMD Resistor and capacitor rework.

Applicable To: TGL UP3 DDR4 RVP.

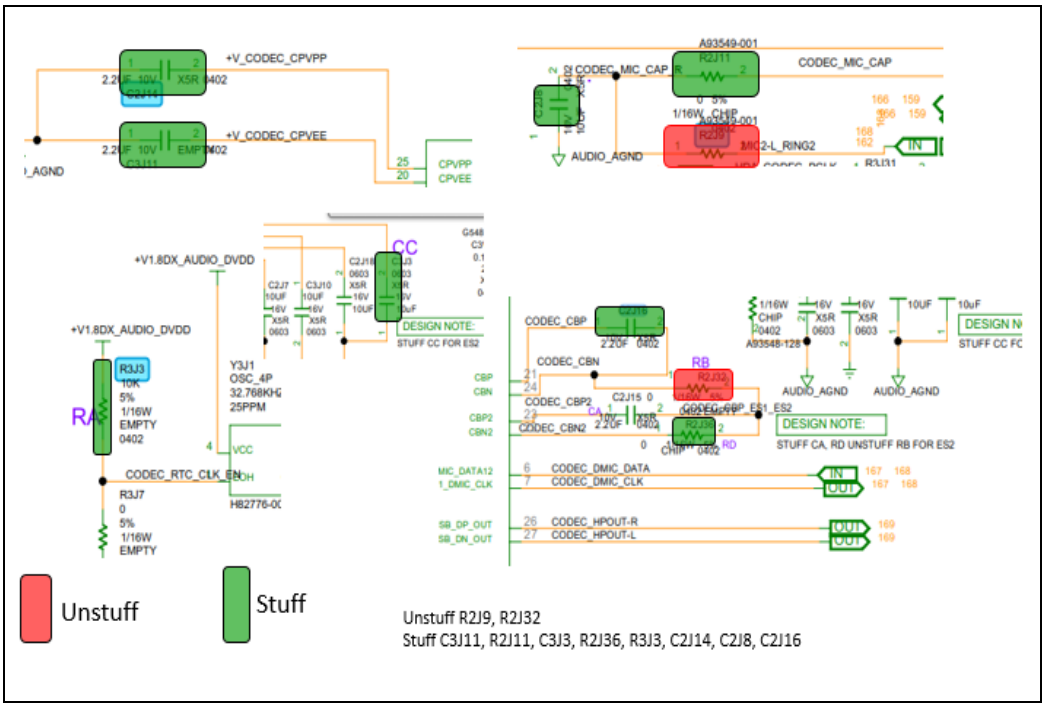
WO# Applicable for this Rework: IPTL184901 and IPTL185001.

Table 3-3. Rework Details: TGL UP3 DDR4 RVP

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Capacitor	C2J14	NA	CAPC, X5R, 0402, 2.2UF, 10.00 V, +/- 10%
Stuff	Capacitor	C3J11	NA	CAPC, X5R, 0402, 2.2UF, 10.00 V, +/- 10%
Unstuff	Resistor	R2J9	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W	NA
Stuff	Resistor	R2J11	NA	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W
Stuff	Capacitor	C2J8	NA	CAPC, X5R, 0402, 10.0uF, 10 V
Stuff	Resistor	R3J3	NA	RES_D, 0402, 10.0K Ohm, 5%, 1/16 W
Stuff	Capacitor	C3J3	NA	CAPC, X5R, 0603,10.00uF, 16 V
Unstuff	Resistor	R2J32	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W	NA
Stuff	Capacitor	C2J16	CAPC, X5R, 0402, 2.2 uF,10 V	NA
Unstuff	Resistor	R2J16	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W	NA
Stuff	Resistor	R2J36	NA	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W
Unstuff	Resistor	R2J25 R2J48 R2W27 R2W25	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W	NA
Stuff	Resistor	R2J24 R2J23 R2J20 R2J14	NA	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W
Unstuff	Resistor	R3W7	RES D, 0402, 200K Ohm,	NA
Unstuff	Resistor	R3W8	RES D, 0402, 100K Ohm	NA
Unstuff	Resistor	R3W6	RES D,0402, 0.00 Ohm, 5.00%, 1/16 W	NA

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R3J8	NA	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W
Stuff	Resistor	R3W4	NA	RES_D, 0402,10.0k Ohm, 5.00%, 1/16 W

Figure 3-5. Schematic Snapshot TGL UP3 DDR4 RVP



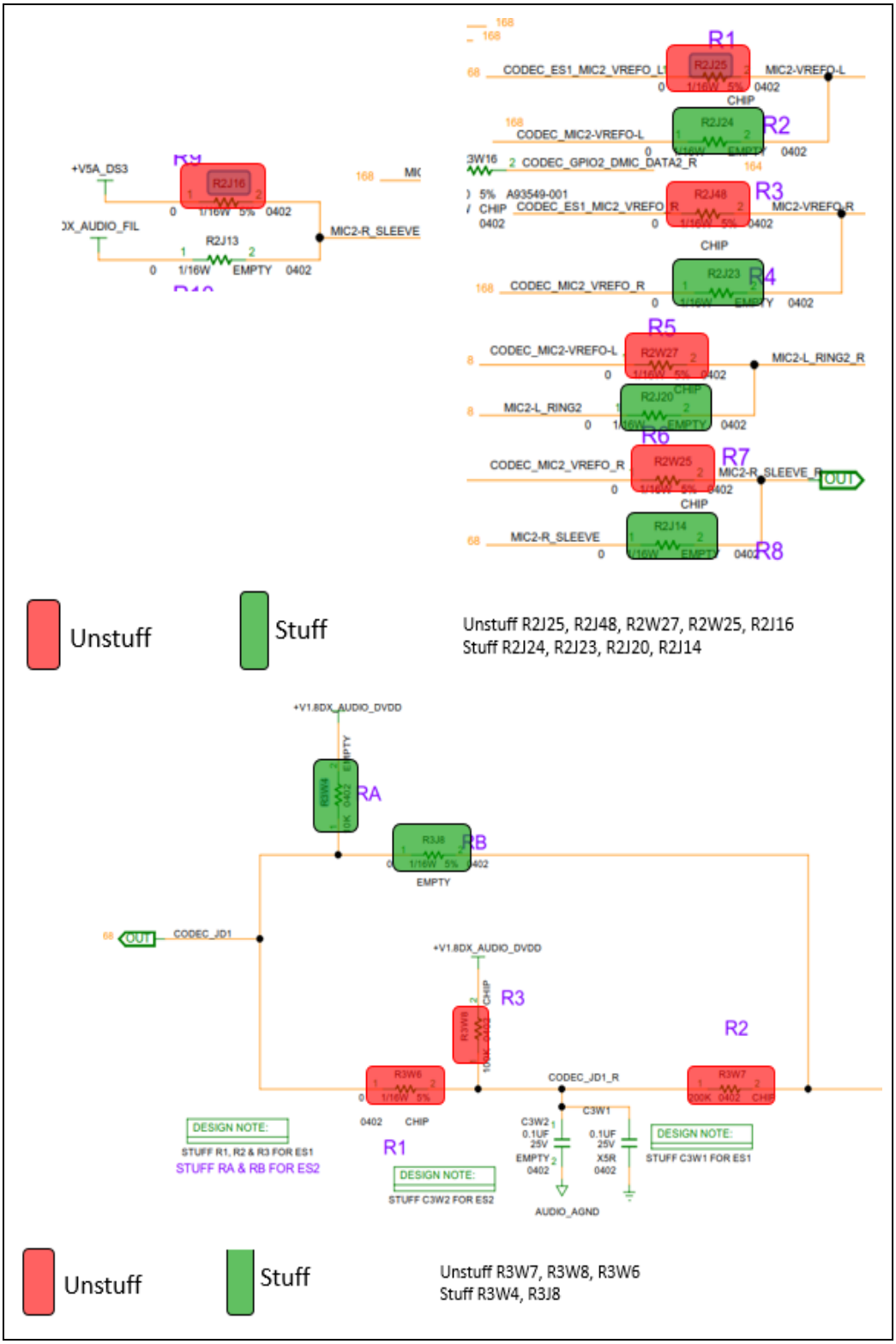
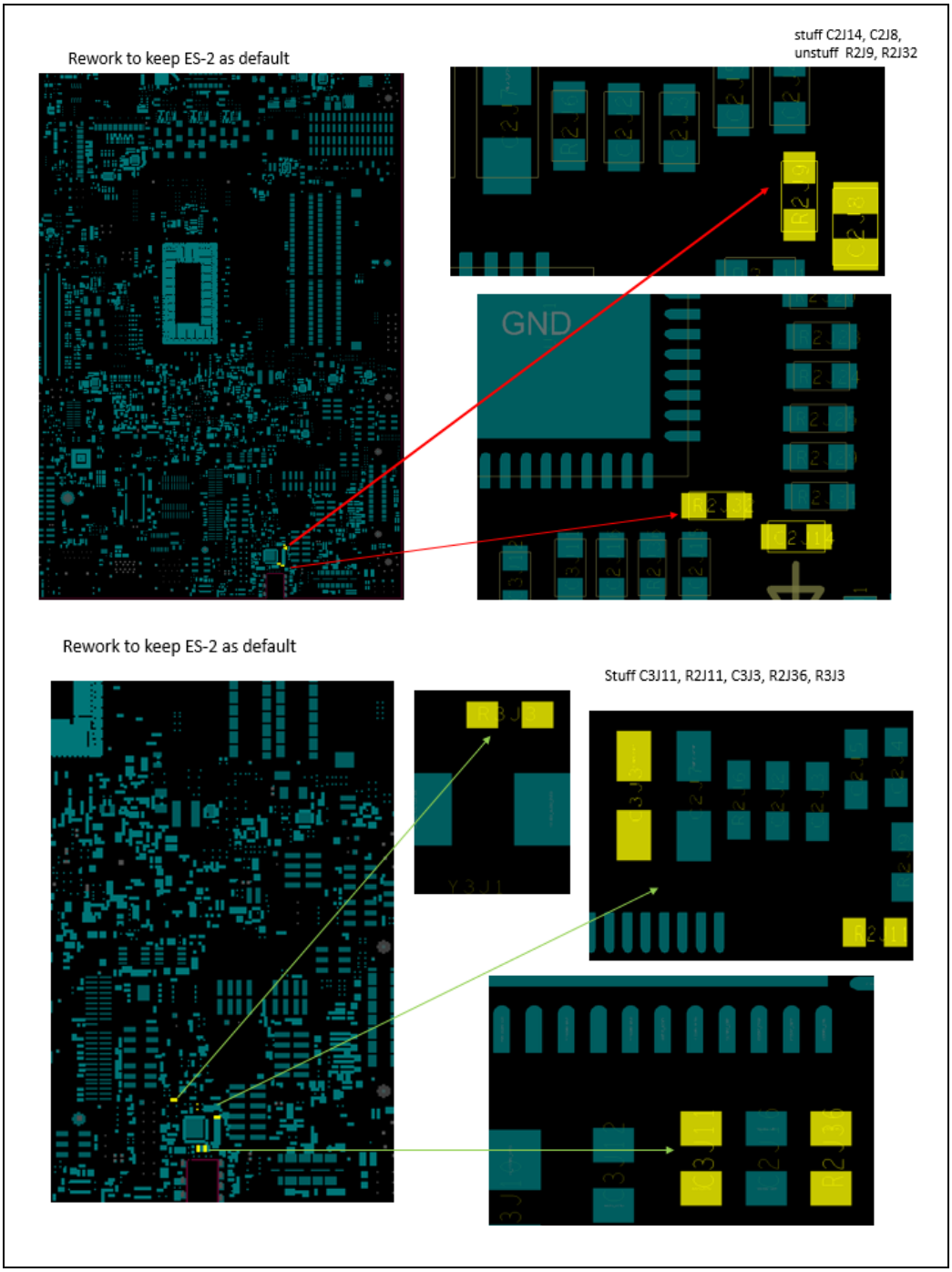

R1
R2
R3
R4
R5
R6
R7
R8
R9
CODEC_ES1_MIC2_VREFO_L
MIC2-VREFO-L
CODEC_MIC2-VREFO-L
CODEC_GPIO2_DMIC_DATA2_R
CODEC_ES1_MIC2_VREFO_R
MIC2-VREFO_R
CODEC_MIC2_VREFO_R
MIC2-L_RING2_R
MIC2-L_RING2
MIC2-R_SLEEVE_R
MIC2-R_SLEEVE
+V5A_DS3
MIC2-R_SLEEVE
Unstuff
Stuff
Unstuff R2J25, R2J48, R2W27, R2W25, R2J16
Stuff R2J24, R2J23, R2J20, R2J14
+V1.8DX_AUDIO_DVDD
RA
RB
EMPTY
CODEC_JD1
R3
R2
R1
CODEC_JD1_R
DESIGN NOTE:
STUFF R1, R2 & R3 FOR ES1
STUFF RA & RB FOR ES2
DESIGN NOTE:
STUFF C3W2 FOR ES2
DESIGN NOTE:
STUFF C3W1 FOR ES1
AUDIO_AGND
Unstuff
Stuff
Unstuff R3W7, R3W8, R3W6
Stuff R3W4, R3J8

Figure 3-6. Layout Snapshot (Top Layer) TGL UP3 DDR4 RVP



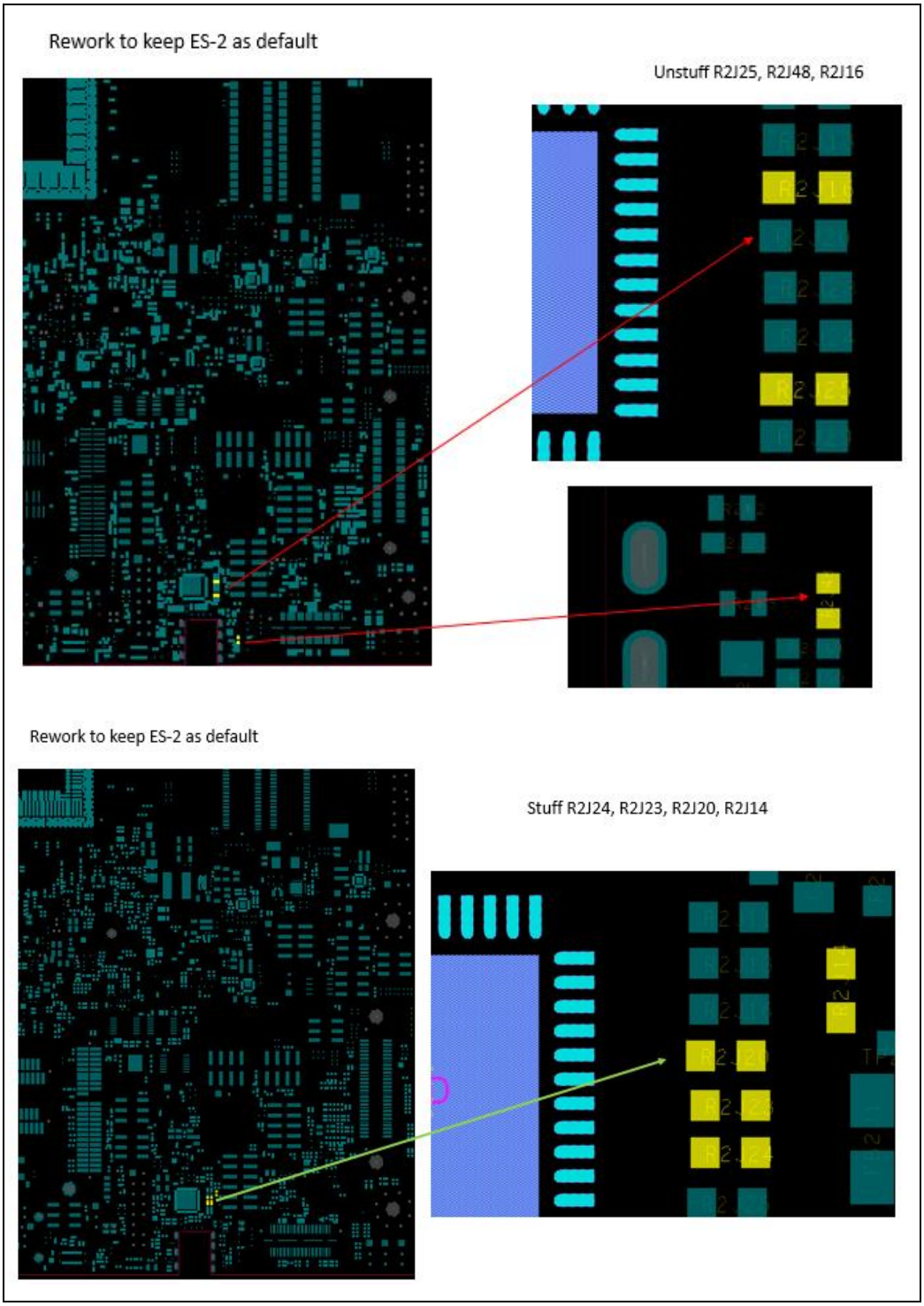

Rework to keep ES-2 as default
Unstuff R2J25, R2J48, R2J16
Rework to keep ES-2 as default
Stuff R2J24, R2J23, R2J20, R2J14

Figure 3-7. Layout Snapshot (Bottom Layer)

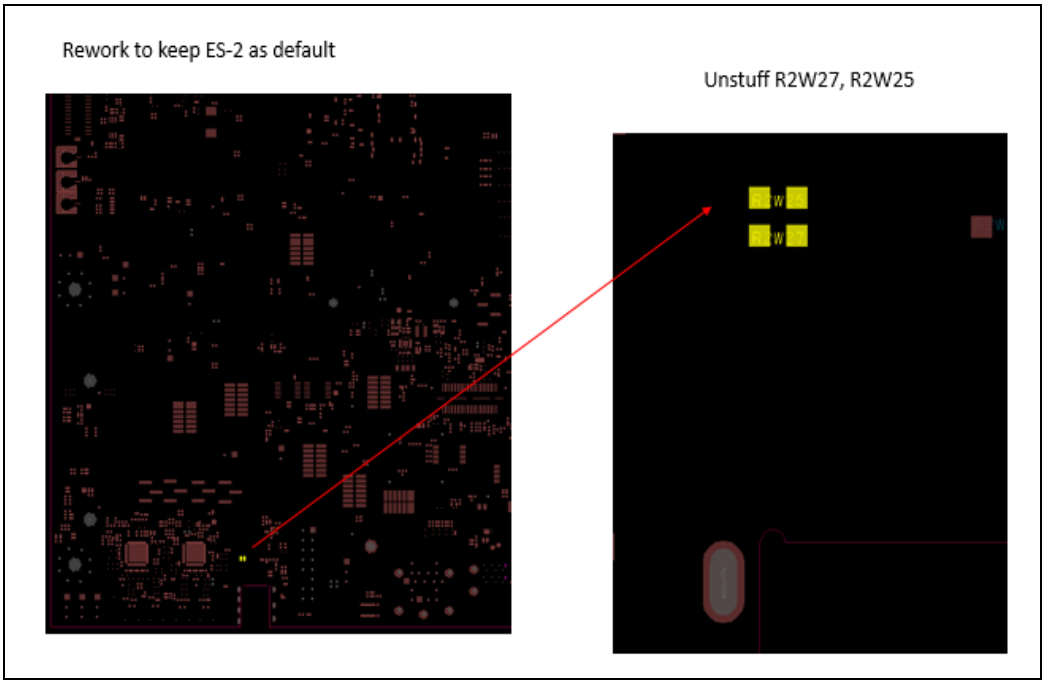


Figure 3-8. Layout Snapshot (Top Layer)

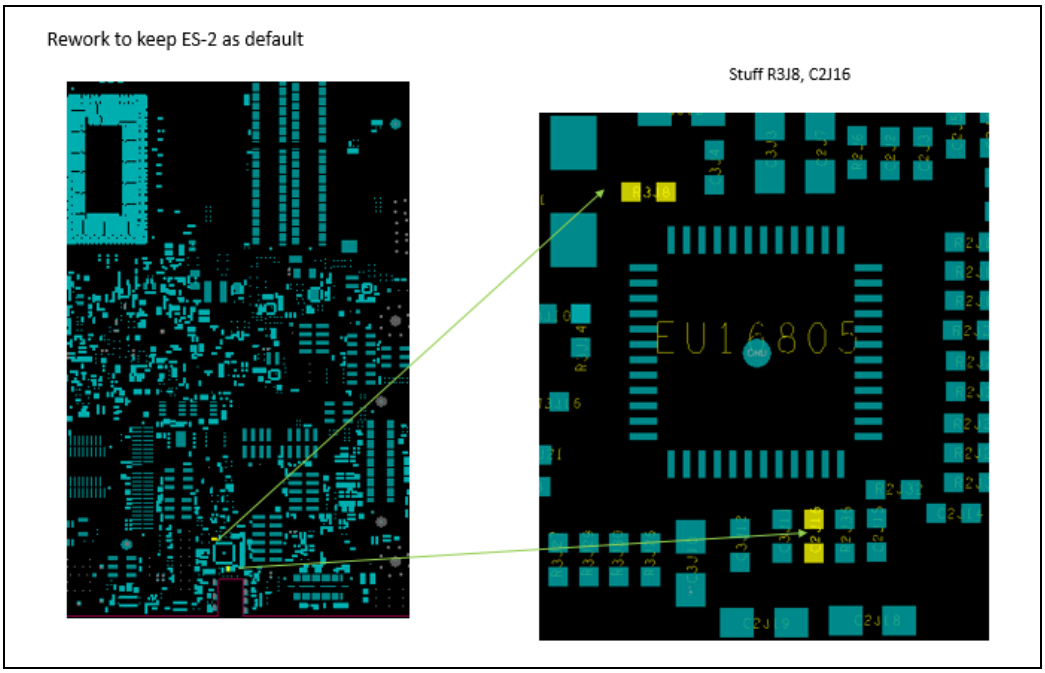
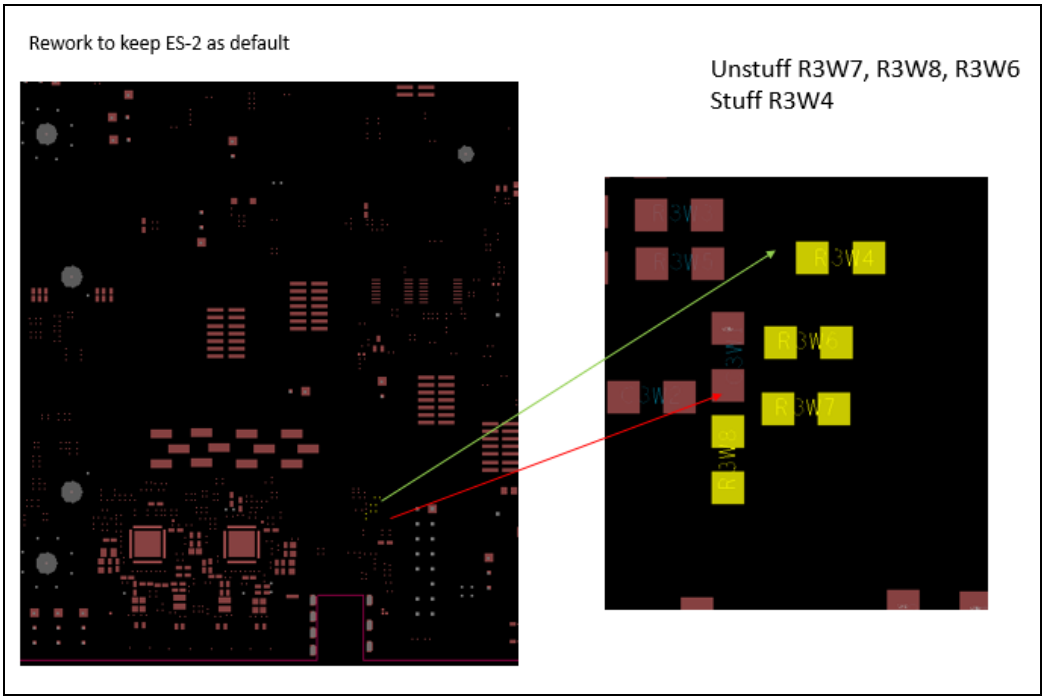


Figure 3-9. Layout Snapshot (Bottom Layer)



3.1.4 Rework to VCCIN and VCCIN_AUX VR in TGL UP3 LP4x

Description: The board must do this rework on VCCIN and VCCIN_AUX VR in TGL UP3 LP4x design to boot.

Impact if not done: The board does not boot.

Details: SMD Resistor rework

Applicable To: TGL UP3 LP4x RVP

WO# Applicable for this Rework: IPTL191101

Table 3-4. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistors	R5F17 R4C3 R5E15 R5D28 R4M14 R4B11 R3M11 R3B11 R4M16 R4B12	NA	RES D,0402,0.0 Ohm, 5.00%, 1/10 W

Figure 3-10. Schematic Snapshot TGL UP3 LPDDR4X RVP

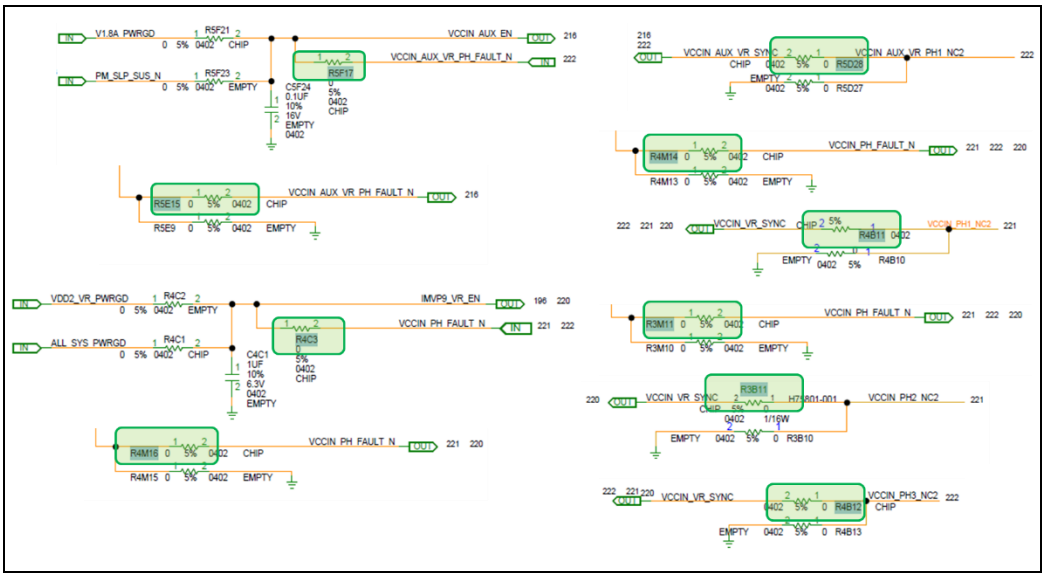
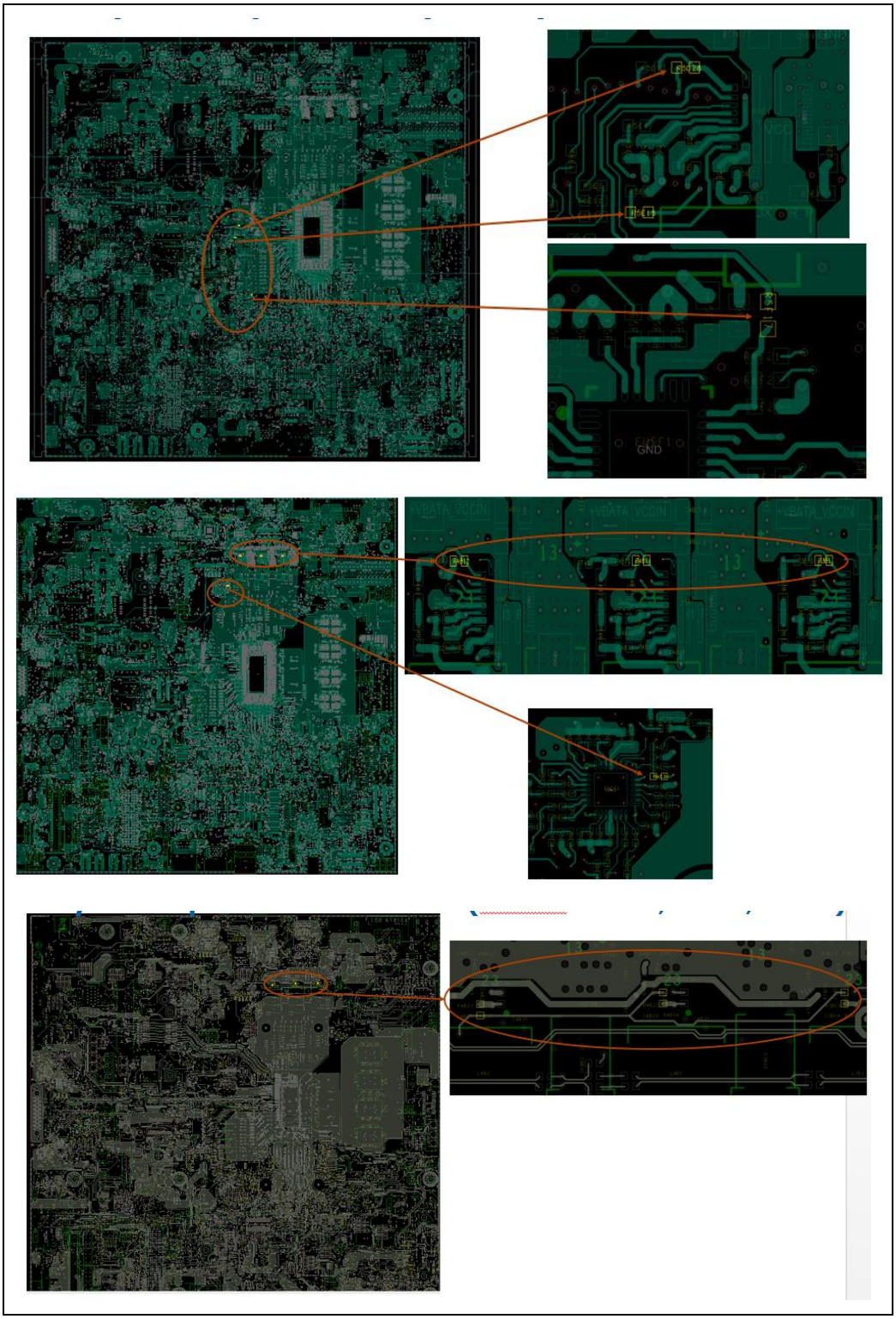


Figure 3-11. Layout Snapshot (Top Layer)



3.1.5 Rework for VDDQ_TX Power Good Isolation in TGL UP3 LP5 RVP

Description: This rework is for VDDQ_TX power good isolation from rest of power sequencing tree due to VDDQ_TX VR power good issue in TGL UP3 LP5 RVP.

Impact if not done: None

Details: SMD Resistor rework

Applicable To: TGL UP3 LP5 designs

WO# Applicable for this Rework: IPTL191502 and IPTL191701.

Table 3-5. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R7U12	NA	Resistor 0402, 10k Ohm, 5%
Unstuff	Resistor	R7U15	Resistor 0402, 10k Ohm, 5%	NA

Figure 3-12. Schematic Snapshot

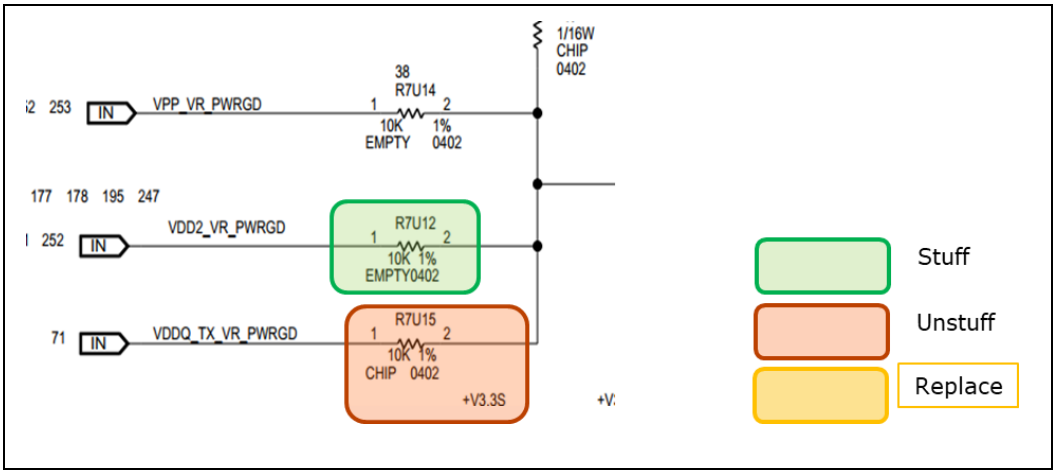
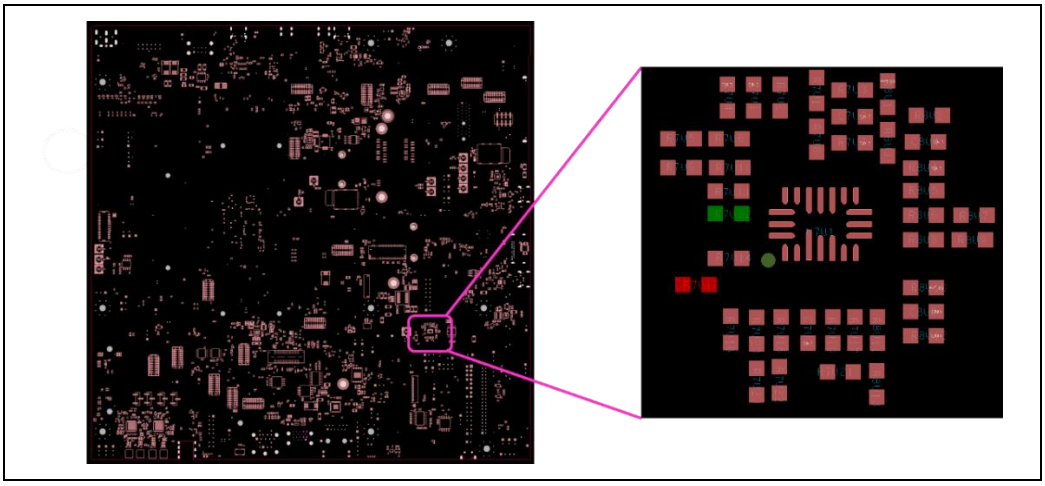


Figure 3-13. Layout Snapshot (Bottom Layer)



3.1.6 Rework for AUX VID Signal Isolation from VCCST and VCCSTG Rail Enable Logic in TGL UP3 RVP

Description: This rework is for AUX VID signal isolation from VCCST and VCCSTG rail enable logic to turn off VCCST and VCCSTG rail in C10 state saving 50 mW power in TGL UP3 RVP.

Impact if not done: None

Details: SMD Resistor rework

Applicable To: TGL UP3 designs

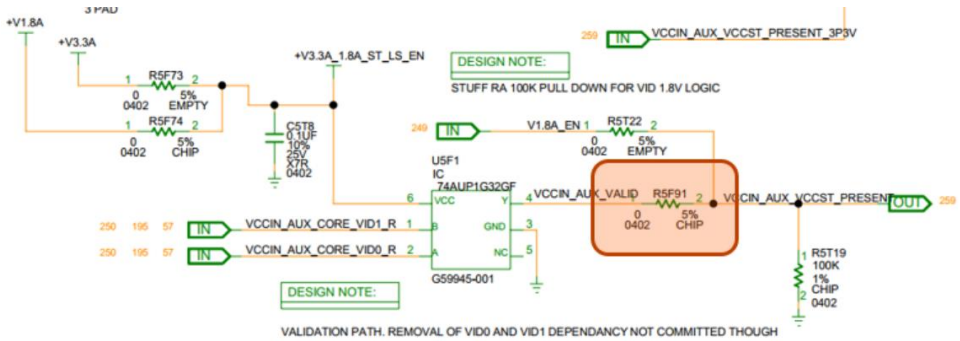
WO# Applicable for this Rework: IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL191502, IPTL191701, IPTY190802, IPTY191801 IPTY191802, IPTY191901, IPTY191902, and IPTY191903

Table 3-6. Rework Details

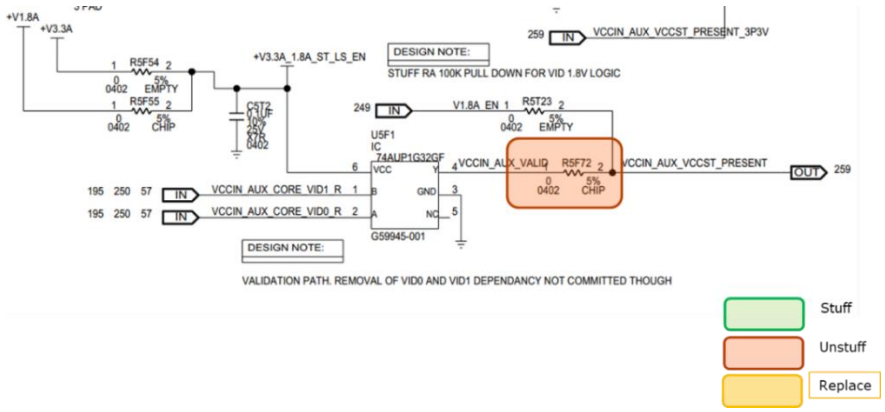
Action	Item	Reference Description	Description of Existing Part	Description of New Part	Applicable to
Unstuff	Resistor	R5F91	Resistor 0402, 0 Ohm, 5%	NA	TGL UP3 DDR4 RVP
Unstuff	Resistor	R5F72	Resistor 0402, 0 Ohm, 5%	NA	TGL UP3 LP4x RVP
Unstuff	Resistor	R5F76	Resistor 0402, 0 Ohm, 5%	NA	TGL UP3 LP5 RVP

Figure 3-14. Schematic Snapshot

TGL UP3 DDR4 RVP:



TGL UP3 LP4x RVP:



TGL UP3 LP5 RVP:

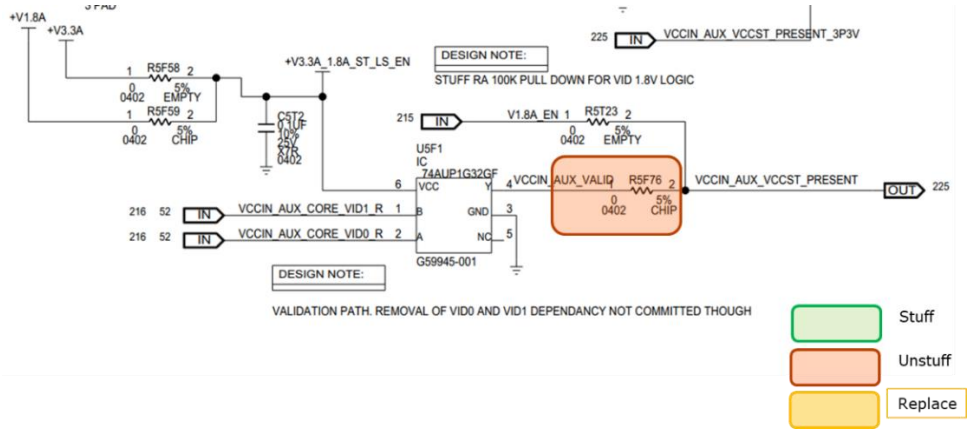
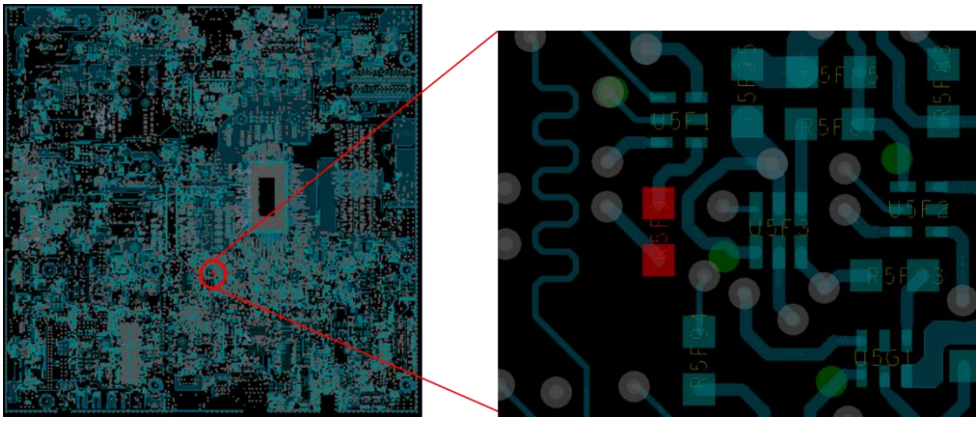
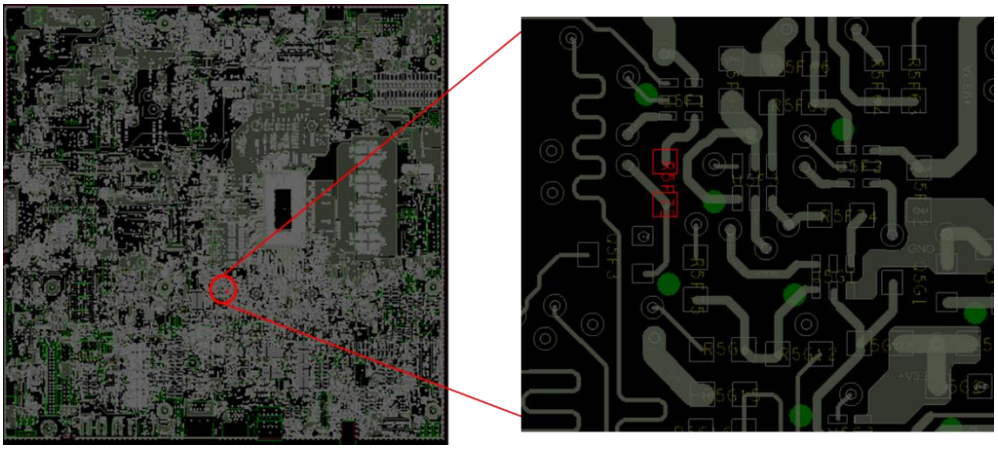


Figure 3-15. Layout Snapshot (Top Layer)

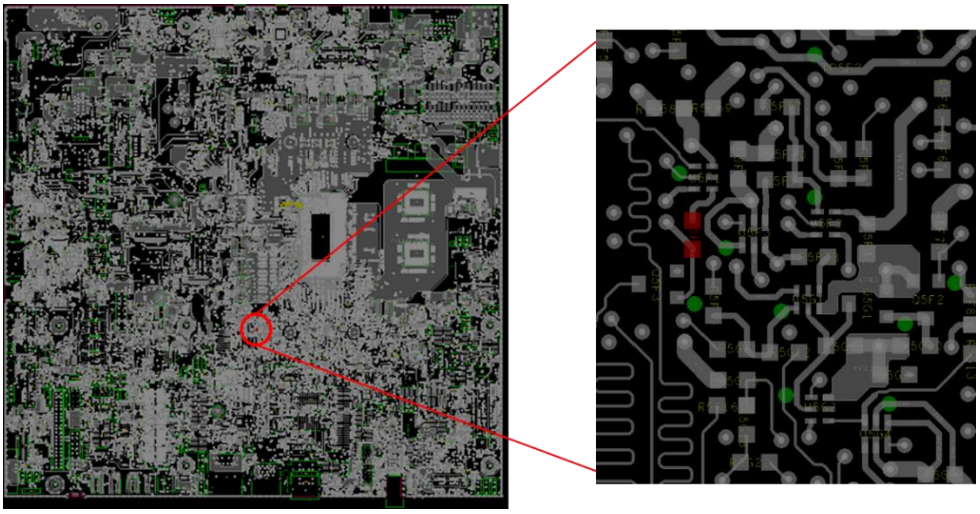
TGL UP3 DDR4 RVP board:



TGL UP3 LP4x RVP board:



TGL UP3 LP5 RVP board:



3.1.7 Rework to Power on TGL UP3 LP4x EXS ERB with TGL UP3 and EXS Silicon

Description: This rework to boot TGL UP3 LP4x EXS ERB with TGL UP3 and EXS silicon

Enables board to boot

- JTAG TDO PU enables the EXS tap
- SPI device to PCH connection issue resolved
- DPWROK needs strong PU which is reworked to resolve the issue on V1P8A_PWRGD_1V8
- A0 PERSONALITY STRAP setting corrected

Impact if not done: NA

Rework Details: SMD Resistor rework and jumper setting.

Applicable To: TGL UP3 LP4X EXS ERB

WO# Applicable for this Rework: IPTL192401 and IPTL193101

Table 3-7. Rework Details: TGL UP3 LP4X RVP

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R4	NA	RES D,0402,1.00 kohm,5.00%,1/16W
Replace	Resistor	R57	RES D,0402,100.00 kOHM,5.00%,1/16W	RES_D,0402,2.2kOHM,1 .00%,1/16W,
Un-Stuff	Resistor	R3U34	RES D,0402,0.00 OHM,5.00%,1/16W	NA
Stuff	Resistor	R3U31	NA	RES_D,0402,10.0kOHM, 5.00%,1/16W,
Set	Jumper	J2F1	NA	Set the jumper 1-2

Figure 3-16. Schematic Snapshot

TGL UP3 LP4X EXS ERB:

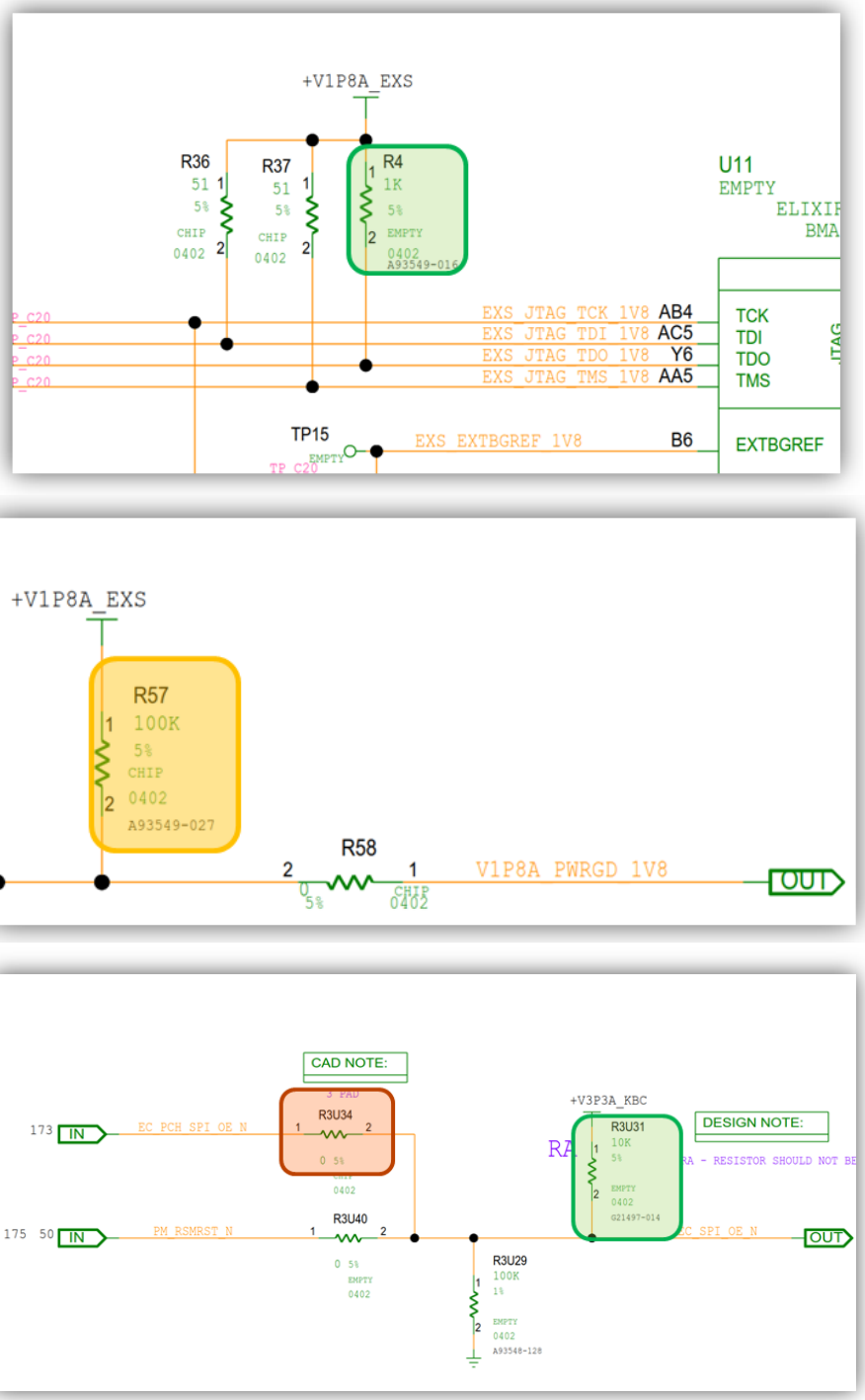
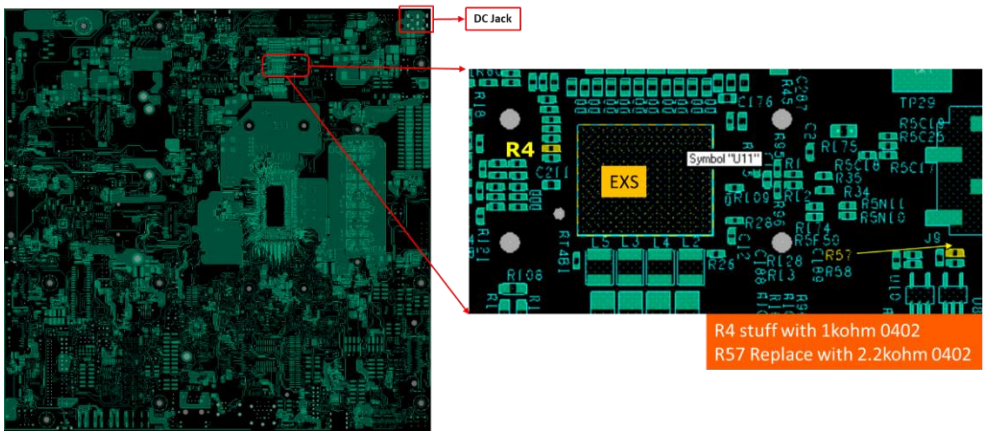


Figure 3-17. Layout Snapshot (Top Layer)

TGL UP3 LP4X EXS ERB:



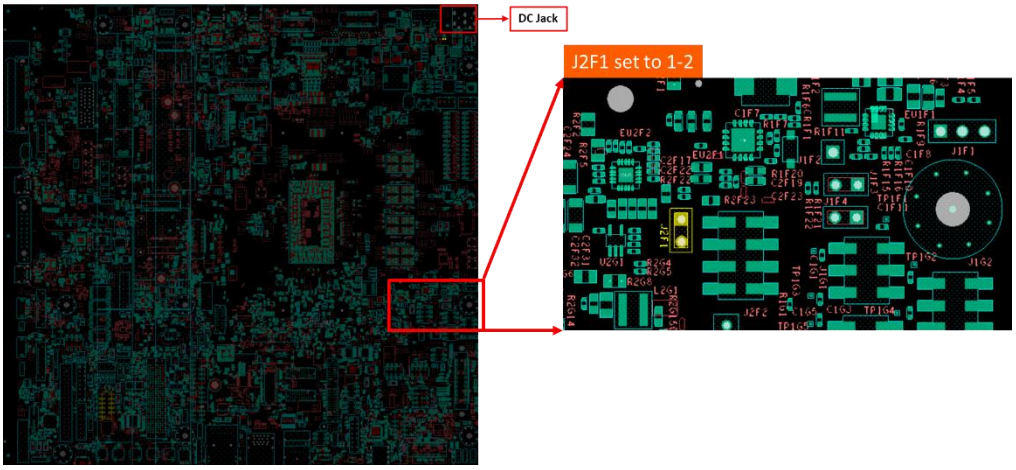
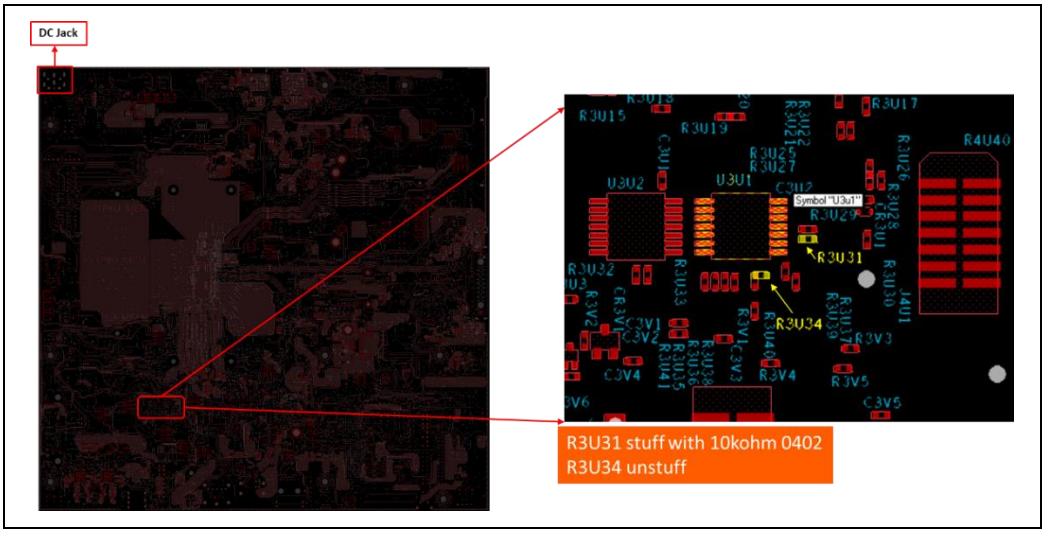


Figure 3-18. Layout Snapshot (Bottom Layer)



3.1.8 Rework for DCLL Change in TGL UP3 Design

Description: Due to change in the DC loadline (DCLL), DCLL resistor needs to be changed. This is needed to for the high-performance workload functions.

Impact if not done: NA

Rework Details: SMD Resistor rework

Applicable To: TGL UP3 RVPs

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201 IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTL203003.

Table 3-8. Rework Details: TGL UP3 DDR4

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R5C20	RES D,0402,1.87 kOHM,1.00%,1/16W	RES D,0402,806.00 ohm,1.00%,1/16W

Table 3-9. Rework Details: TGL UP3 LP4X

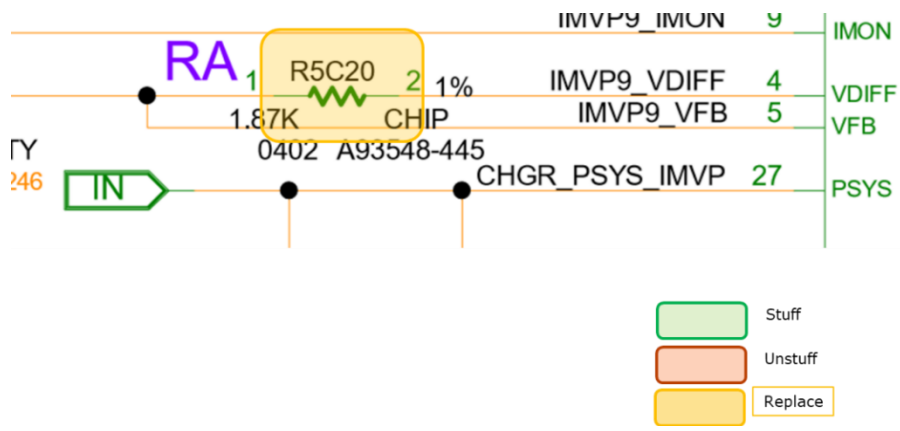
Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R5C12	RES D,0402,1.87 kOHM,1.00%,1/16W	RES D,0402,806.00 ohm,1.00%,1/16W

Table 3-10. Rework Details: TGL UP3 LP5

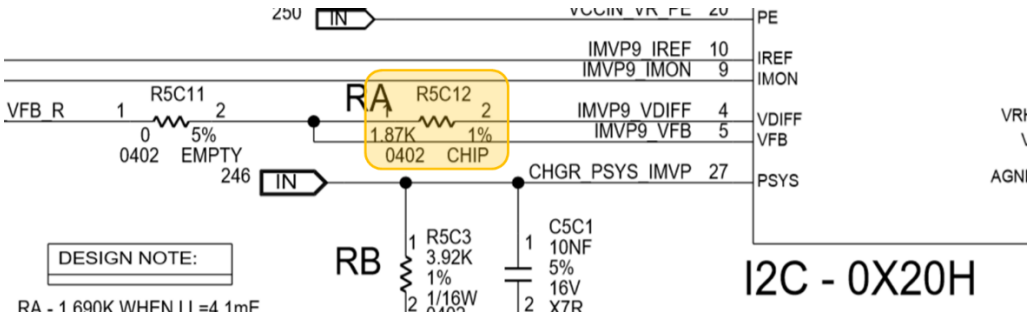
Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R5C16	RES D,0402,1.87 kOHM,1.00%,1/16W	RES D,0402,806.00 OHM,1.00%,1/16W

Figure 3-19. Schematic Snapshot

TGL UP3 DDR4 RVP:



TGL UP3 LP4X:



TGL UP3 LP5:

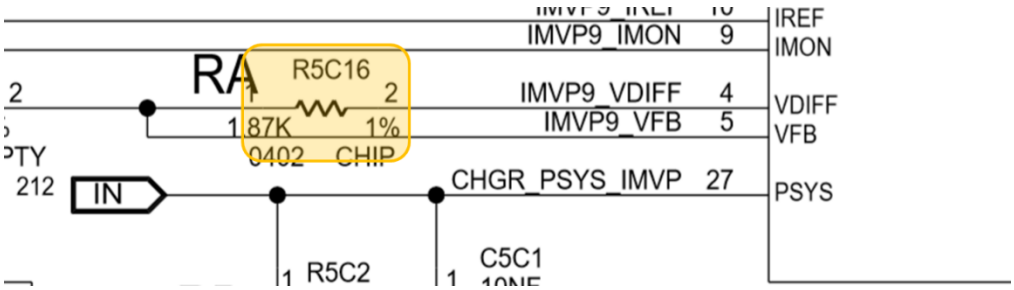
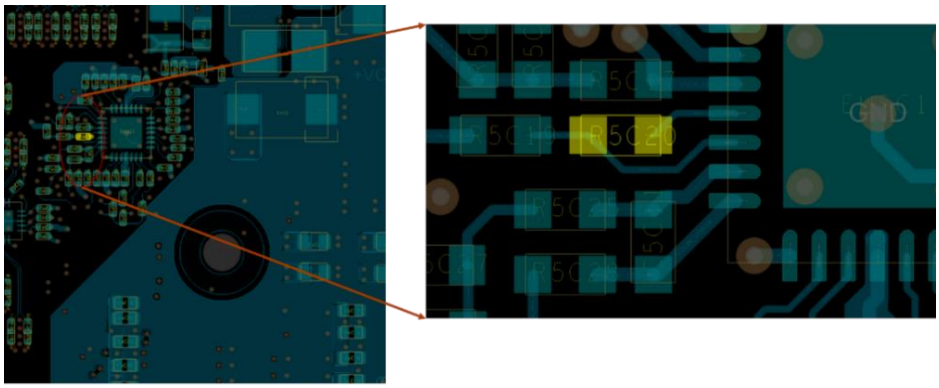
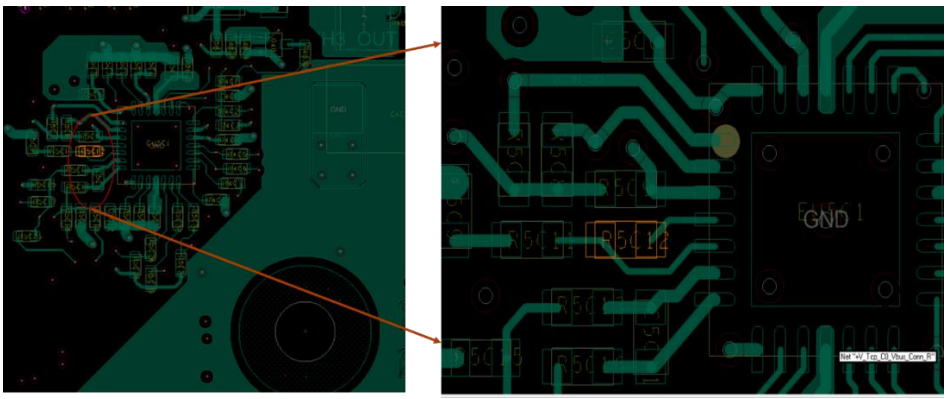


Figure 3-20. Layout Snapshot (Top Layer)

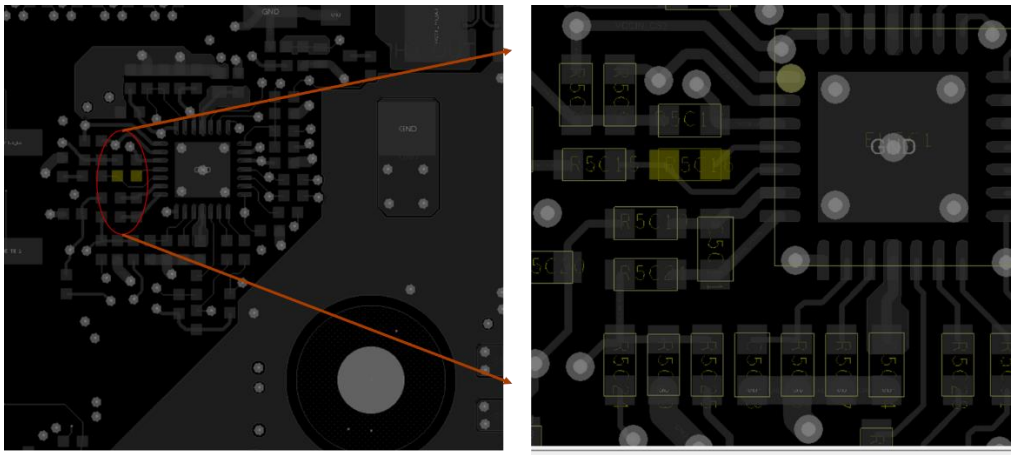
TGL UP3 DDR4:



TGL UP3 LP4X



TGL UP3 LP5



3.1.9 Rework to Enable SPI QUAD MODE Functionality at 50 MHz

Description: Series termination change from 75ohms to 33ohms.

Impact if not done: NA

Note: This rework is mandatory only for the B0 – Package. If Optional rework Section 3.3.2 is done already, change the SPI buffer strength to default value – by following procedure in below document. Note: In step 5 (Refer to the attachment in this document AN0000025.pdf), Type "11 60" instead of "11 00".

Rework Details: SMD Resistor rework

Applicable To: TGL UP3 boards (Applicable only for **B0 package**)

WO# Applicable for this Rework: IPTL191002, IPTL191201 IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603 IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL194702, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTY191801, IPTY191802 IPTY191901, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTL201901, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-11. Rework Details: TGL UP3 DDR4

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R3G76 R3G74 R3G77 R3G82 R3G81 R3G84 R3U29 R3G86 R3U30 R3U35 R3U33 R3U32 R3G79 R3G80 R3G78	RES D,0402,75 Ohms,5.00%,1/10W	33Ohms, 0402

Table 3-12. Rework Details: TGL UP3 LP4X

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R3G77 R3G75 R3G78 R3G83 R3G82 R3G85 R3U32 R3G87 R3U33 R3U38 R3U36 R3U35 R3G80 R3G81 R3G79	RES D,0402,75 Ohms,5.00%,1/10W	33Ohms, 0402

Table 3-13. Rework Details: TGL UP3 LP5

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R3G77 R3G75 R3G78 R3G83 R3G82 R3G85 R3U30 R3G87 R3U31 R3U36 R3U34 R3U33 R3G80 R3G81 R3G79	RES D,0402,75 OHM,5.00%,1/10W	33 Ohms, 0402

Figure 3-21. Schematic Snapshot: TGL UP3 DDR4

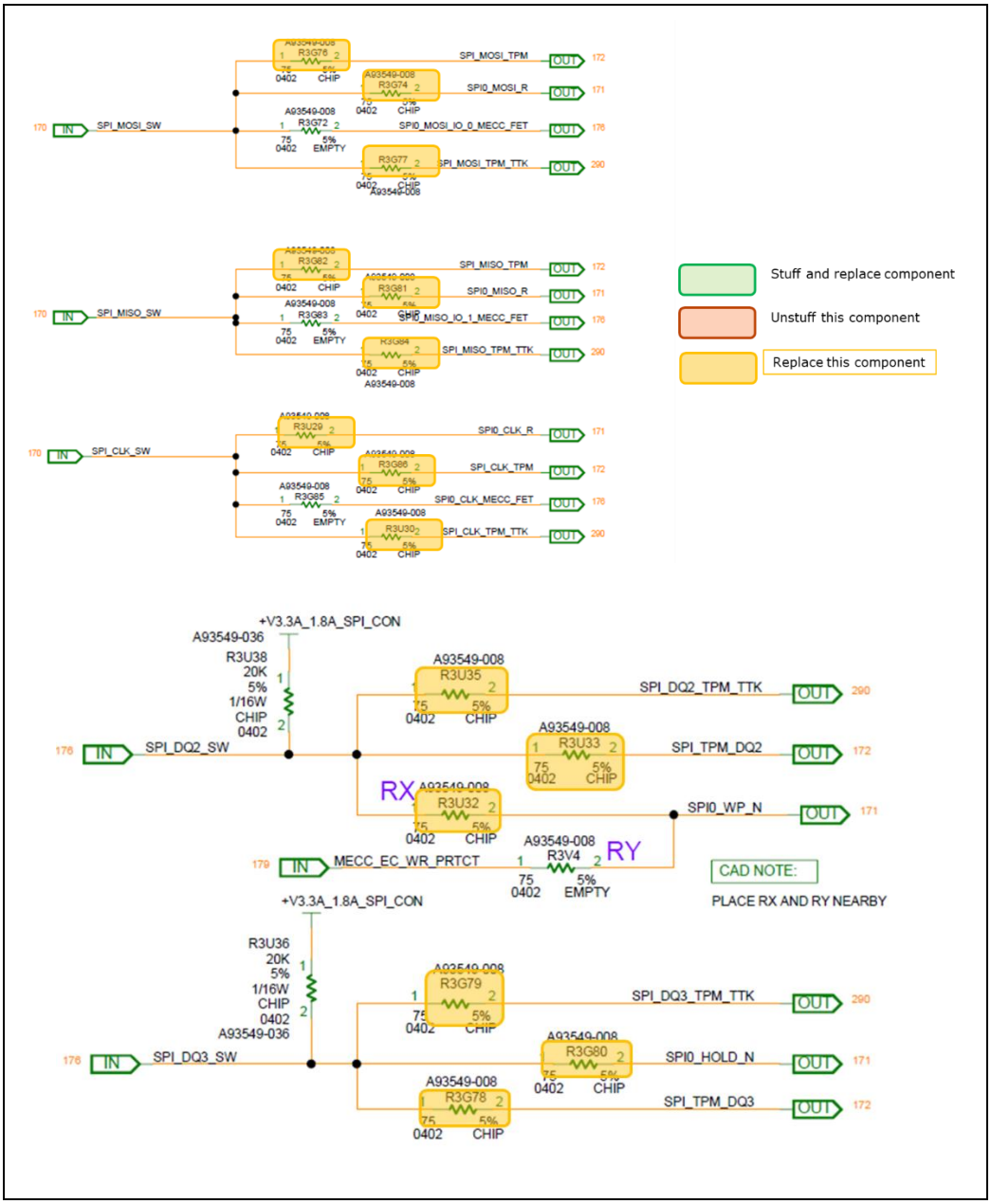


Figure 3-22. Schematic Snapshot: TGL UP3 LP4X

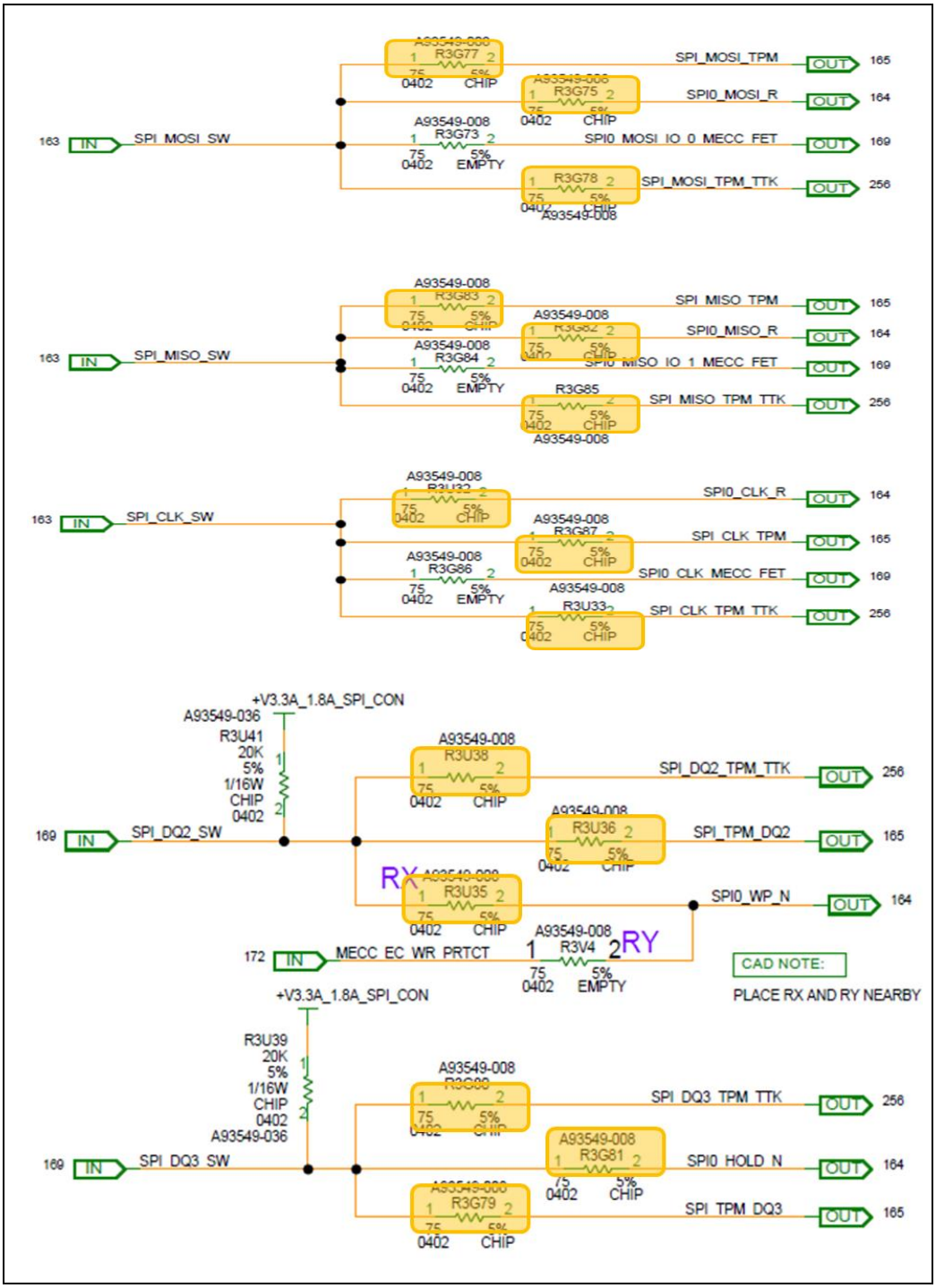


Figure 3-23. Schematic Snapshot: TGL UP3 LP5

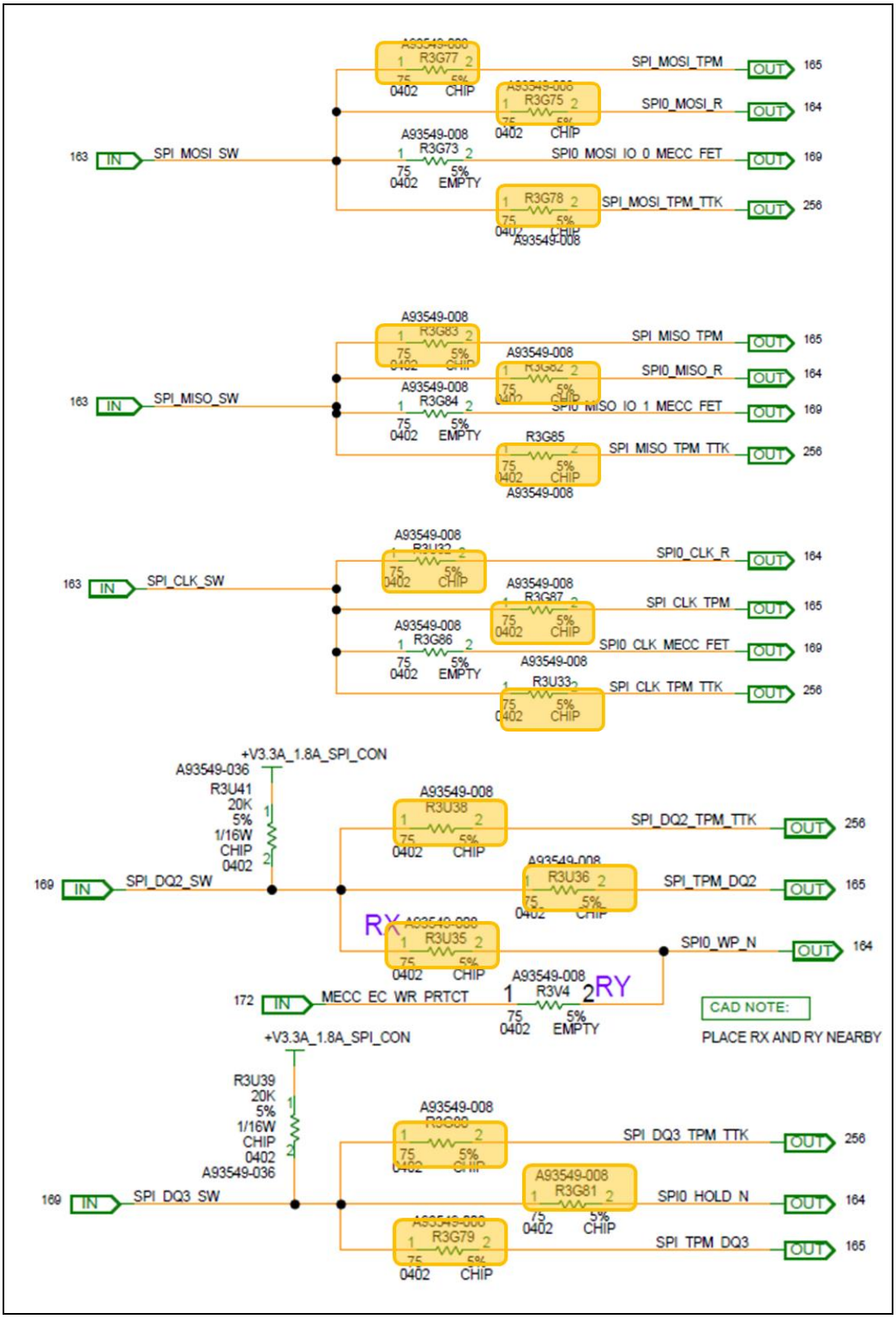


Figure 3-24. Layout Snapshot (Top Layer): TGL UP3 DDR4

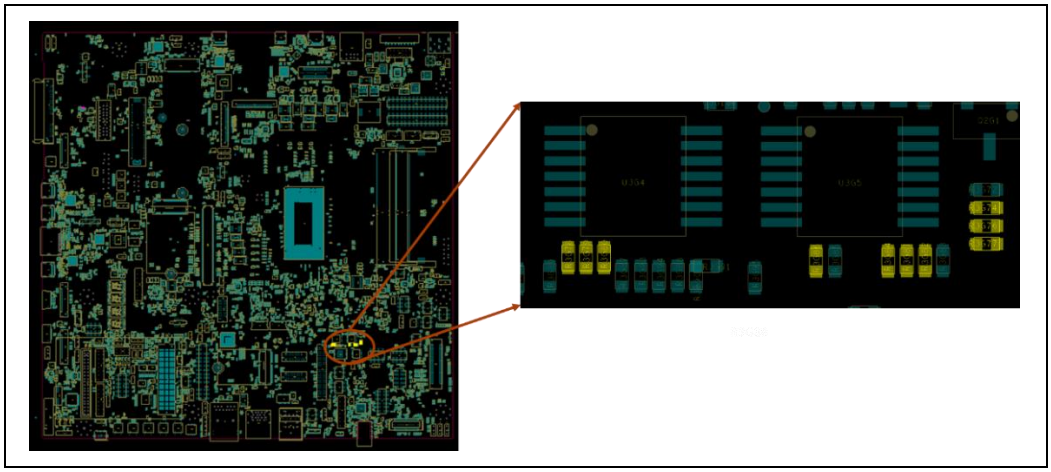


Figure 3-25. Layout Snapshot (Bottom Layer): TGL UP3 DDR4

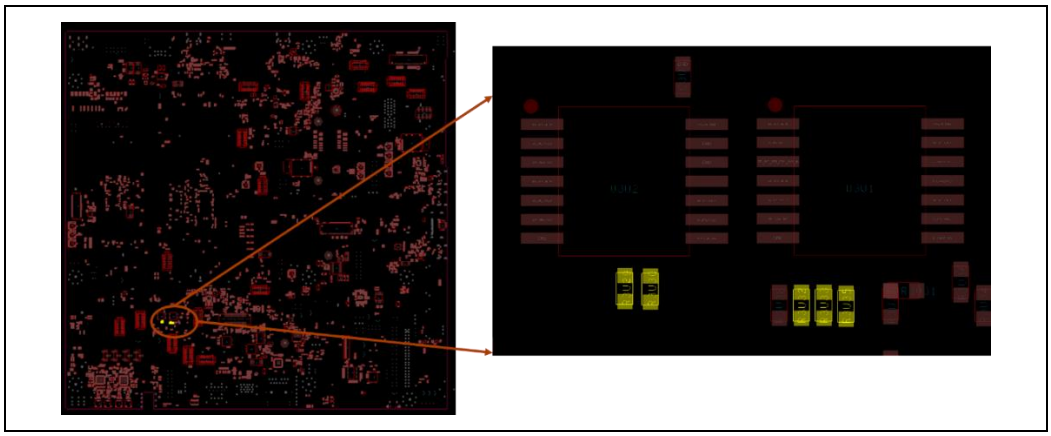


Figure 3-26. Layout Snapshot (Top Layer): TGL UP3 LP4X

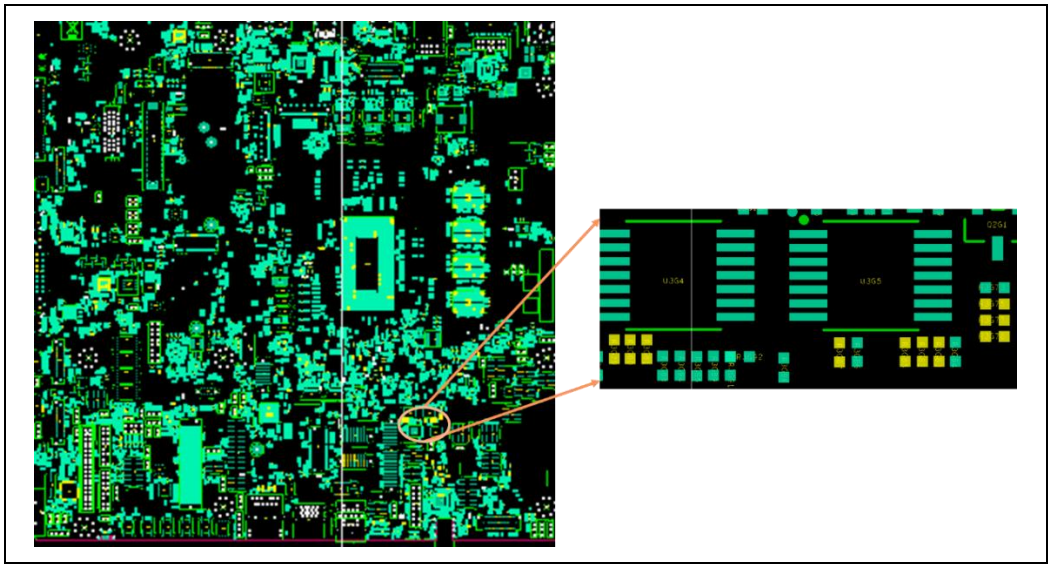


Figure 3-27. Layout Snapshot (Bottom Layer): TGL UP3 LP4X

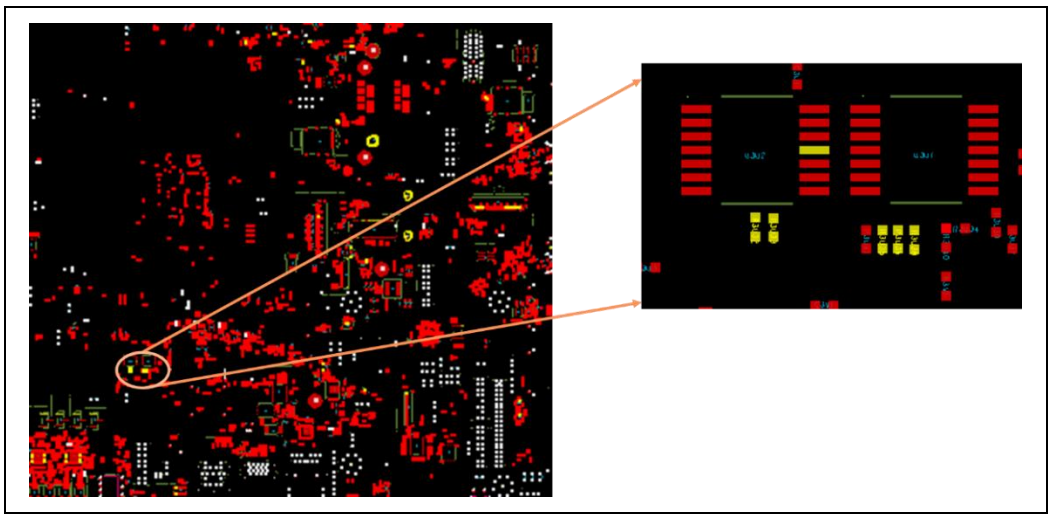


Figure 3-28. Layout Snapshot (Top Layer): TGL UP3 LP5

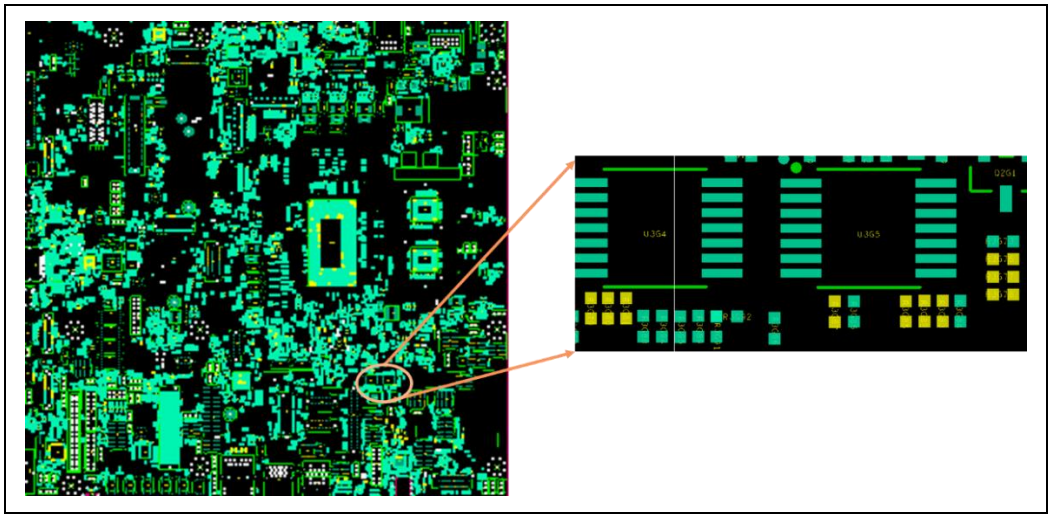
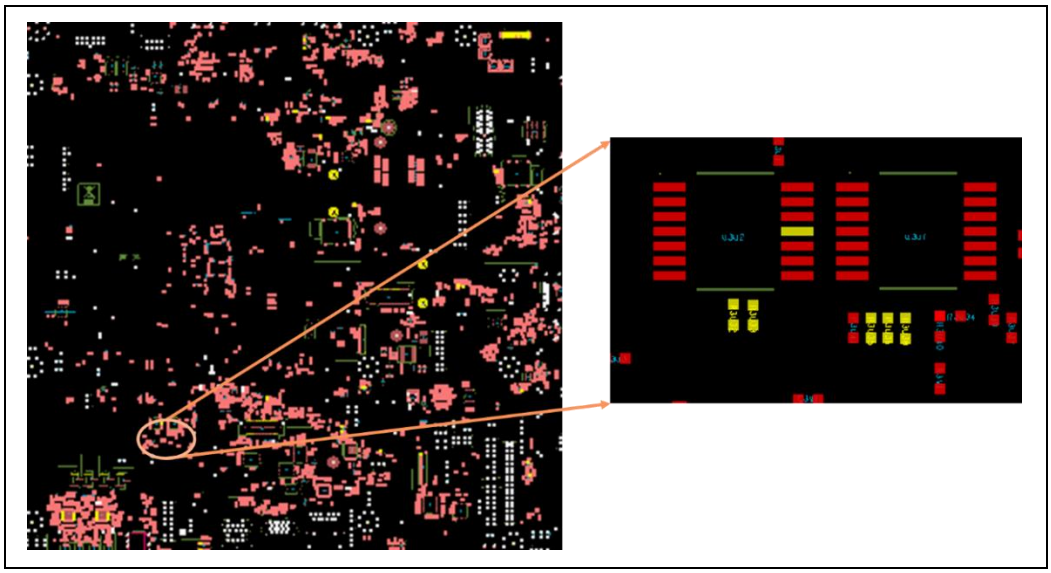


Figure 3-29. Layout Snapshot (Bottom Layer): TGL UP3 LP5



3.2 Featured Rework

3.2.1 Rework to Enable SoundWire* in ALC711

Description: Defining the path for codec to operate in SoundWire* mode.

Impact if done: By implementing this rework, SoundWire* path is enabled for ALC711 (HEADSET CODEC). If not implemented, ALC711 (HEADSET CODEC) defaults to operate in HDA Audio Codec.

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP

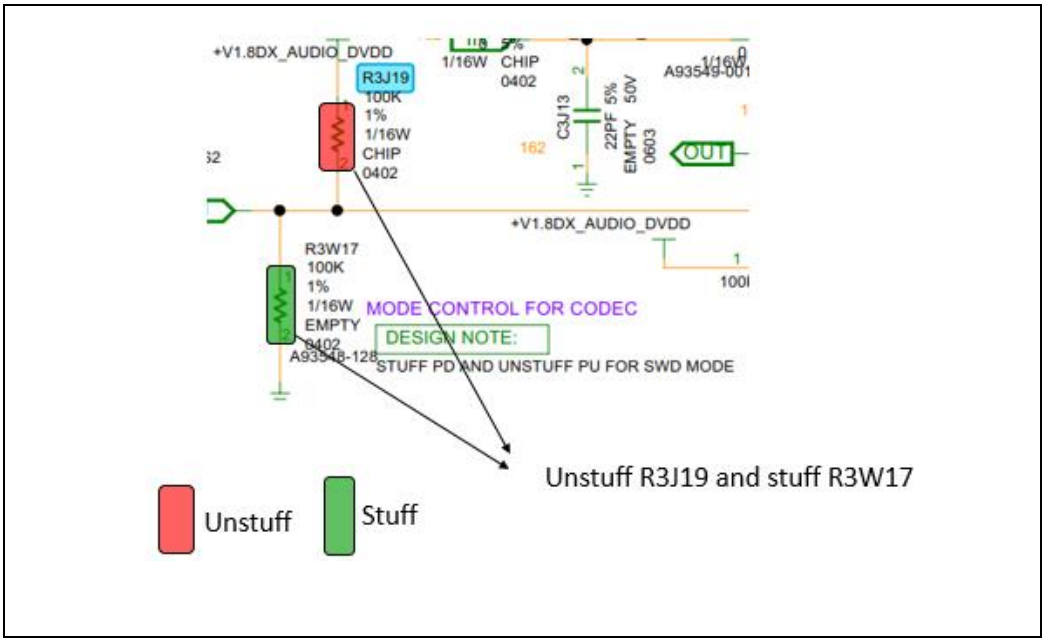
WO# Applicable for this Rework: IPTL184901 and IPTL185001

Table 3-14. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R3J19	100K, 1%, 1/16 W, 0402	NA
Unstuff	Resistor	R2G3 R3F73 R3F59 R3J35	33 Ohm, 1/16 W, 0402	NA
Stuff	Resistor	R3W17	NA	100K, 1%, 1/16 W, 0402

NOTE: For the Schematic reference description and layout snapshot, refer to Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit (#609003).

Figure 3-30. Schematic Snapshot



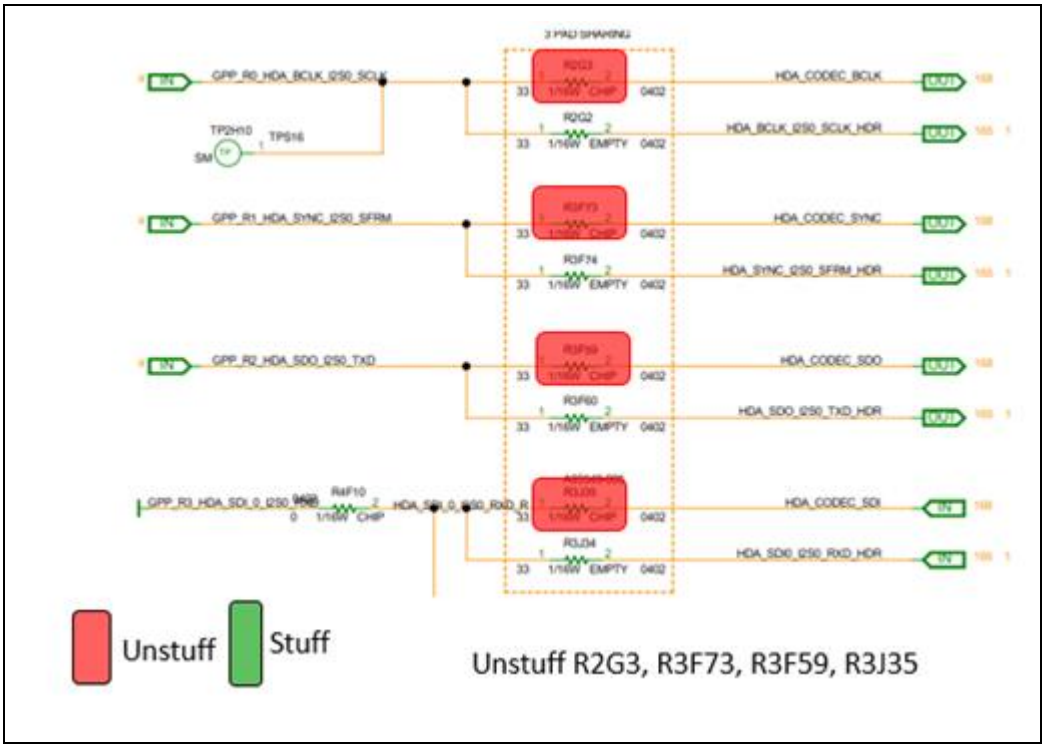
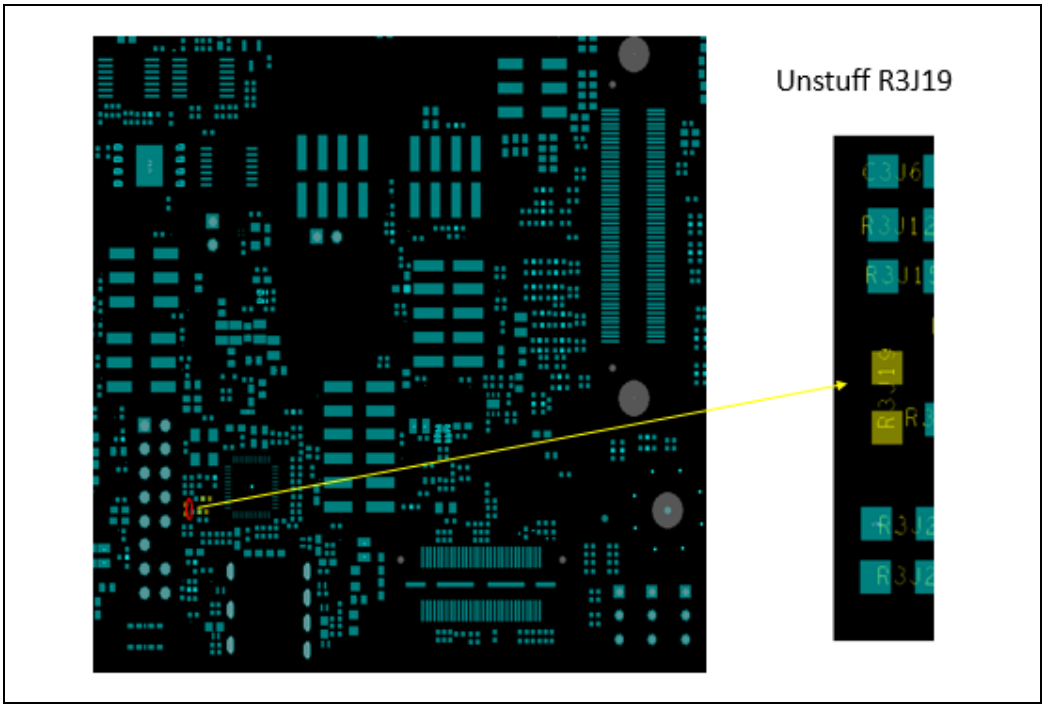


Figure 3-31. Layout Snapshot (Top Layer)



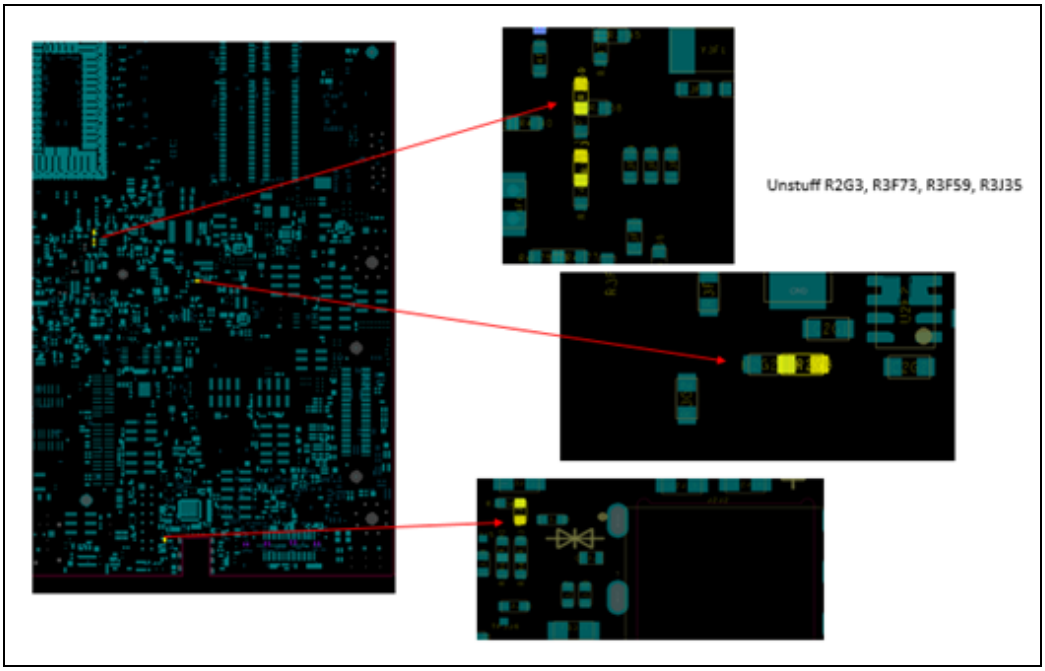
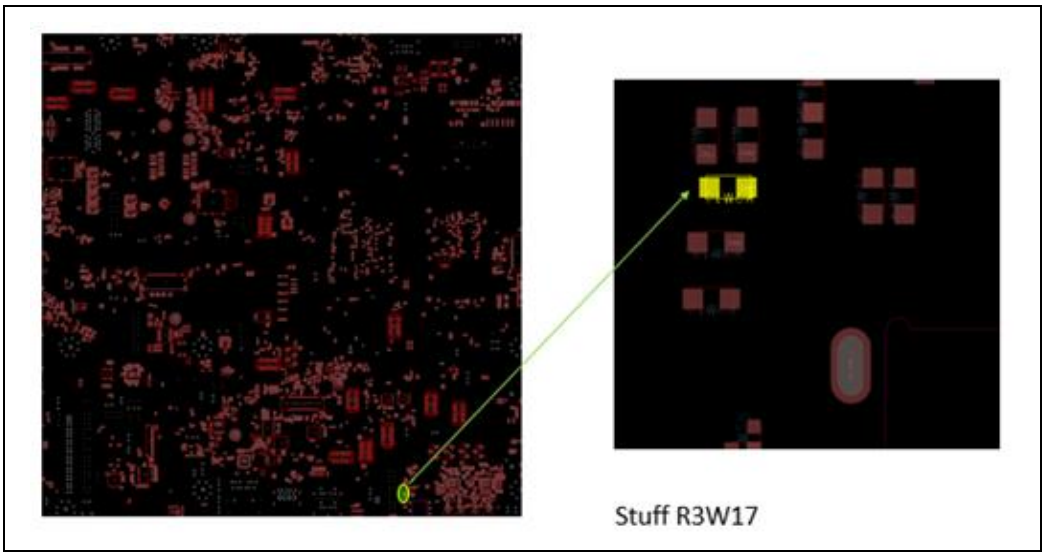


Figure 3-32. Layout Snapshot (Bottom Layer)



3.2.2 Rework to Enable SoundWire* on AIOC for ALC1308

Description: Defining the path for Amplifier to operate in SoundWire* mode in AIOC.

Impact if done: Implementing this rework enables SoundWire* path for ALC1308 to AIC via RVP. If not implemented, onboard ALC1308 (amp) is enabled by default.

Details: SMD Resistor rework

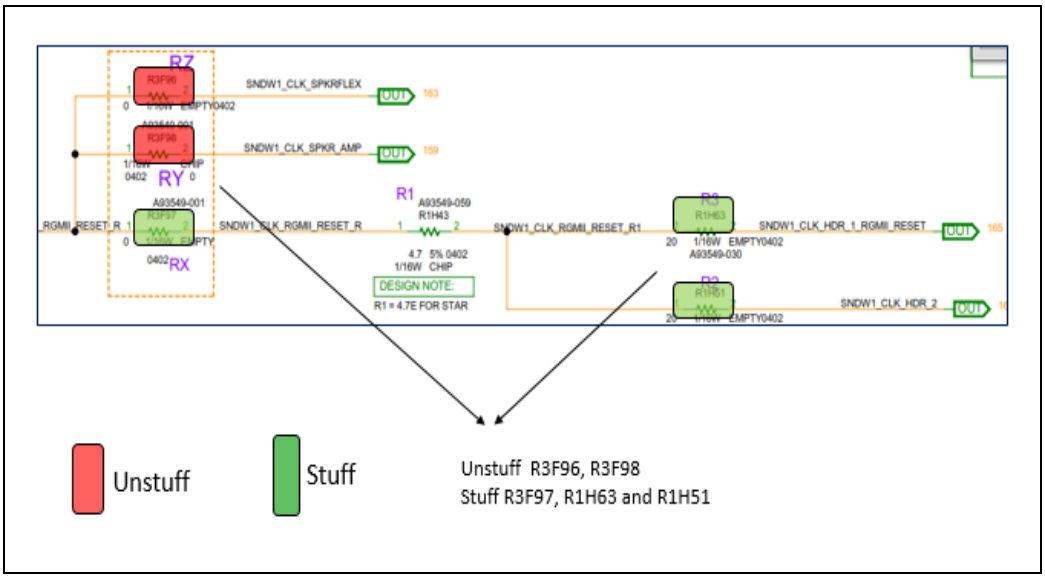
Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

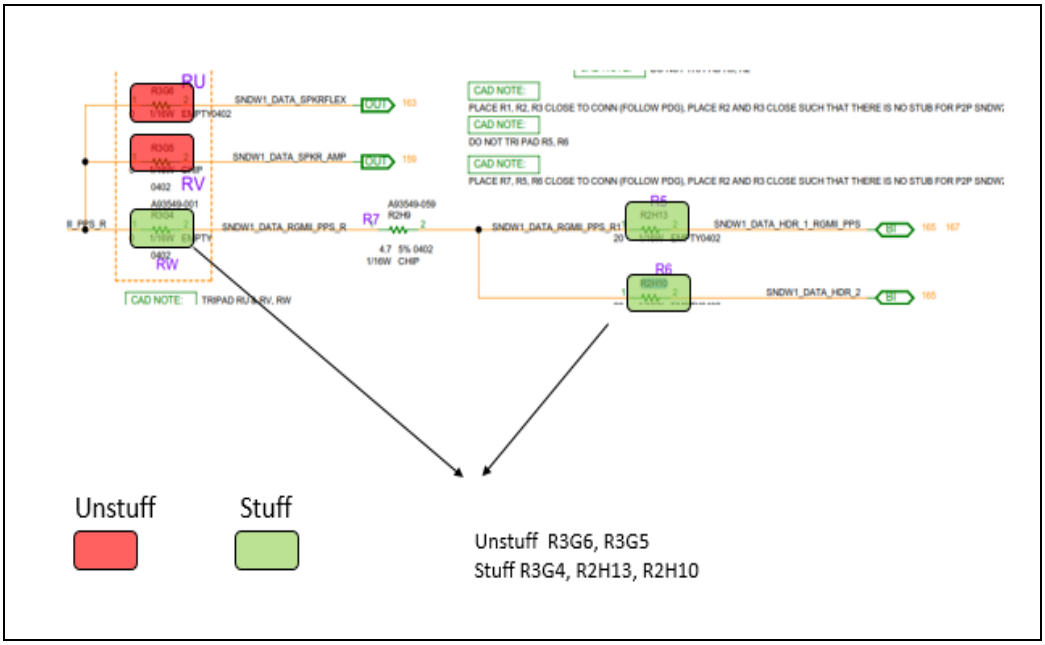
WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL191502, IPTL191701, IPTY190802, IPTY191801, IPTY191901, IPTY191902, IPTY191903, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY193902, IPTY201701, IPTL201901, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-15. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R3F96 R3F98 R3G6 R3G5	0 Ohm, 5%, 1/16 W, 0402	NA
Stuff	Resistor	R3F97 R3G4	NA	0 Ohm, 5%, 1/16 W, 0402
Stuff	Resistor	R1H63 R1H51 R2H13 R2H10	NA	20 Ohm, 5%, 1/16 W, 0402

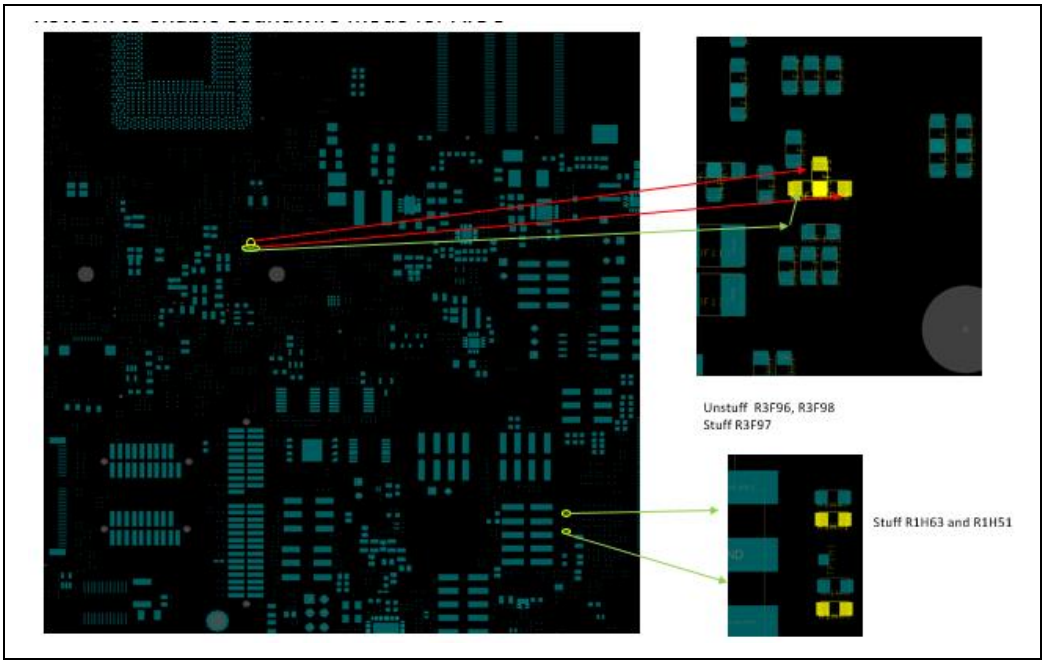
Figure 3-33. Schematic Snapshot

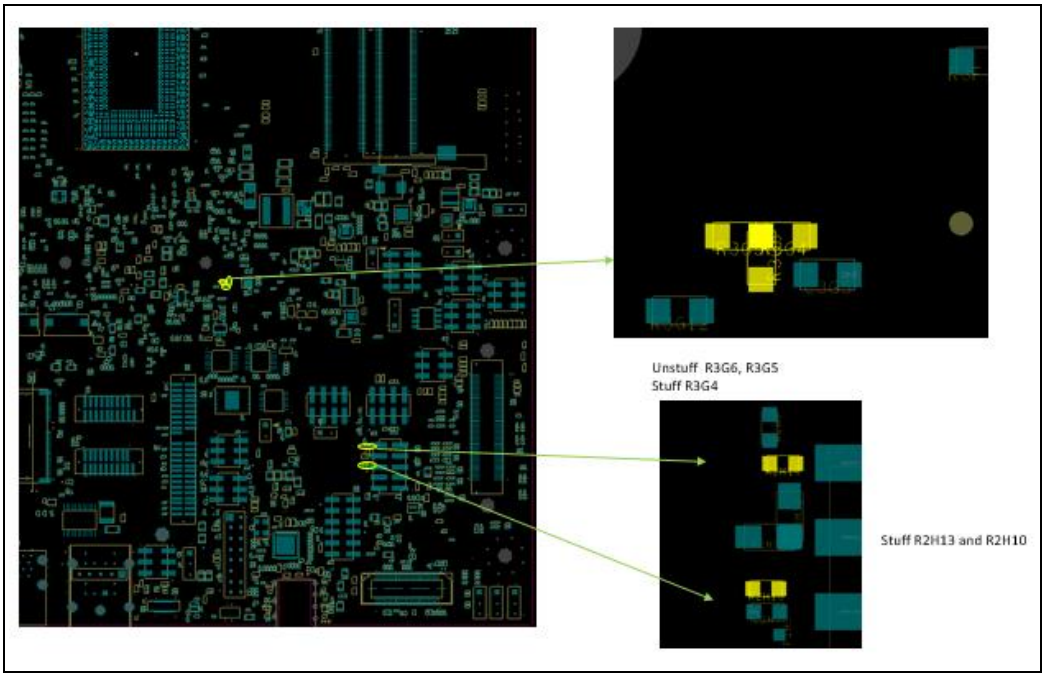




NOTE: For the Schematic reference description and layout snapshot, refer to Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit (#609003).

Figure 3-34. Layout Snapshot (Top Layer)





3.2.3 Rework to Enable SoundWire* on AIOC for ALC711

Description: Defining the path for headset codec to operate in SoundWire* mode in AIOC.

Impact if done: Implementing this rework enables SoundWire* path for ALC711 to AIC via RVP header. If not implemented, onboard ALC711 (codec) is enabled by default.

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL191502, IPTL191701, IPTY190802, IPTY191801, IPTY191901, IPTY191902, IPTY191903, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTL201901, IPTY193902, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

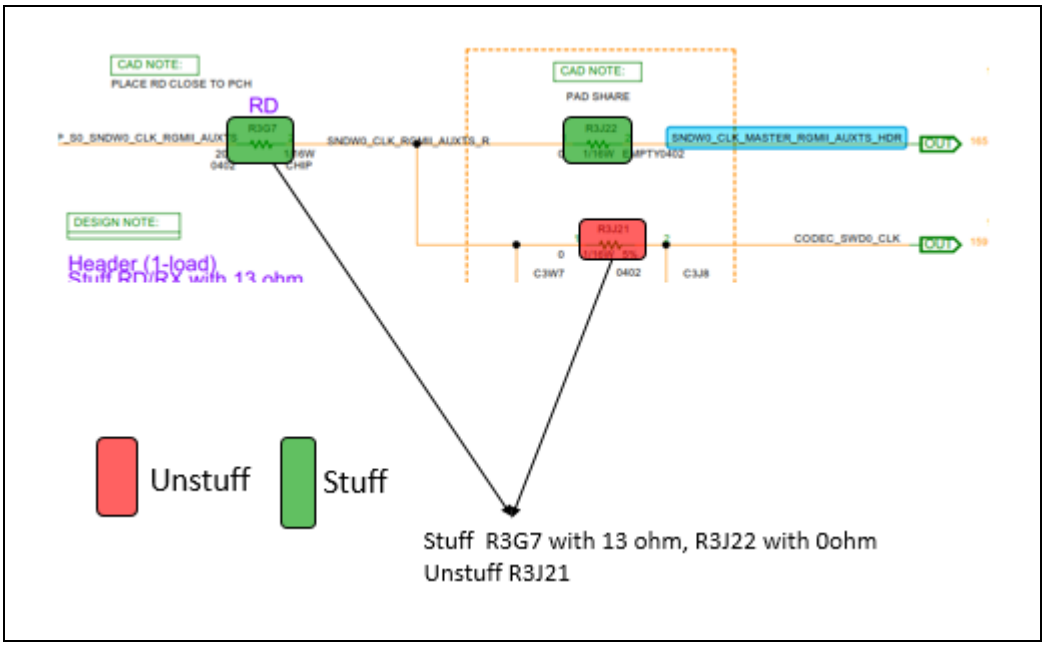
Table 3-16. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R3J21 R3J16	0 Ohm, 5%, 1/16 W, 0402	NA

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R3G7 R3G10	NA	13 Ohm, 5%, 1/16 W, 0402
Stuff	Resistor	R3J22 R3J17	NA	0 Ohm, 5%, 1/16 W, 0402

NOTE: For the Schematic reference description and layout snapshot, refer to Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit (#609003).

Figure 3-35. Schematic Snapshot



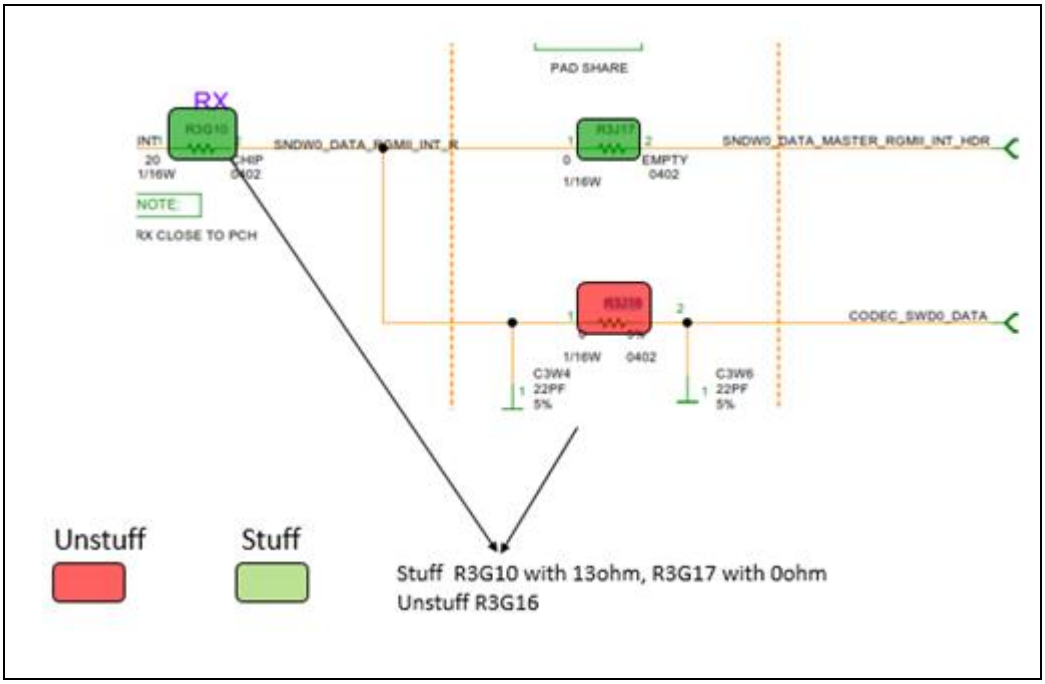
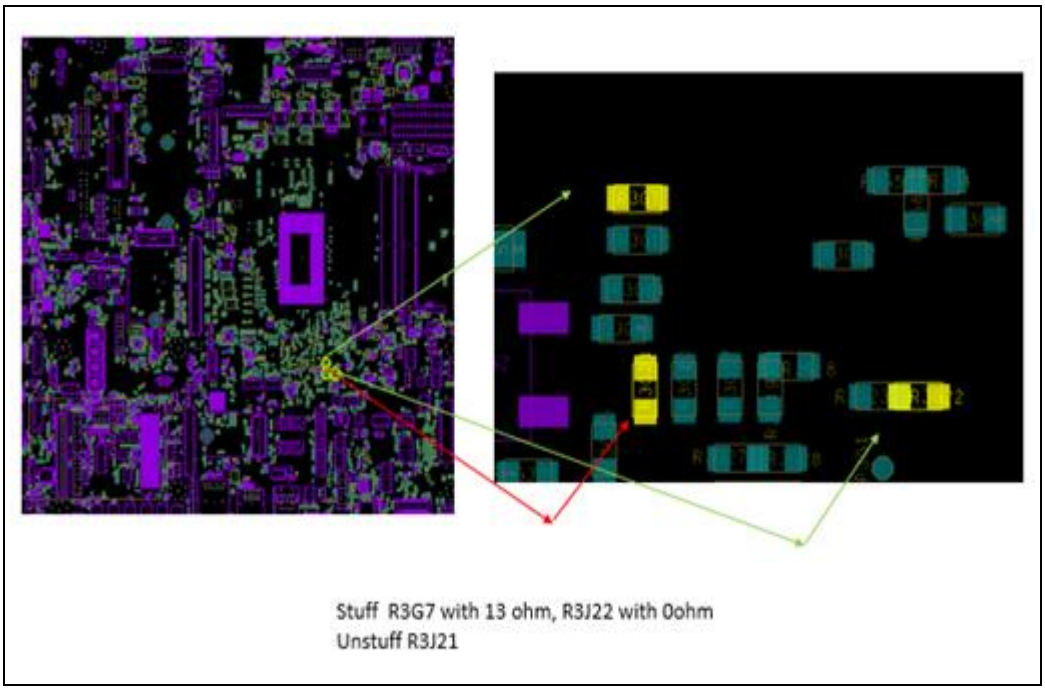
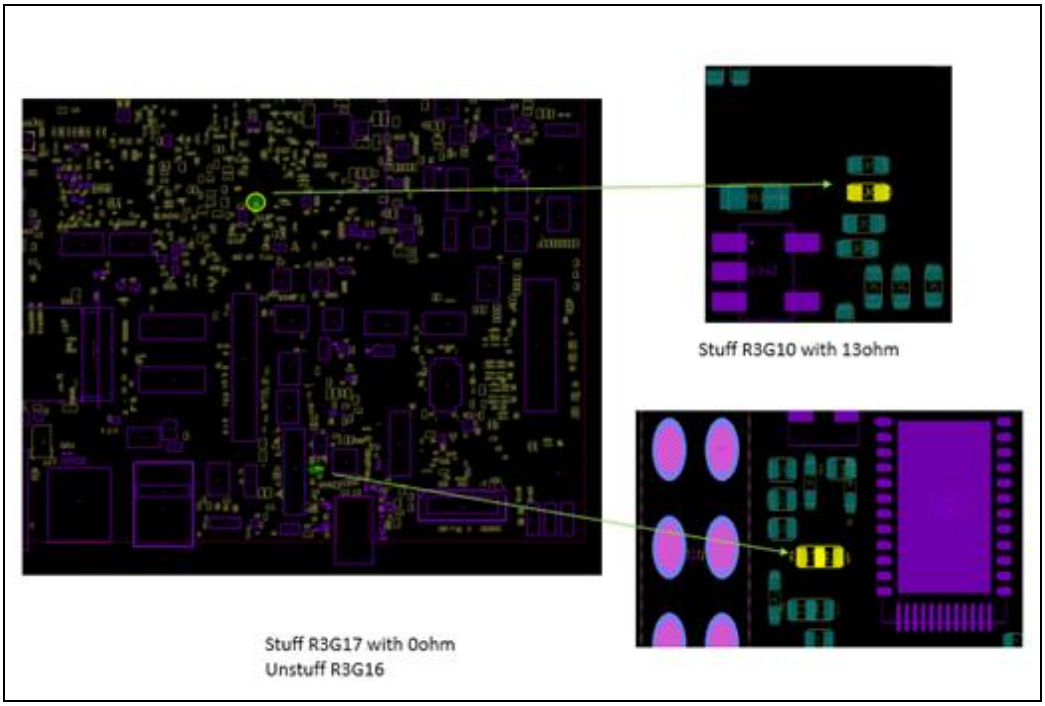


Figure 3-36. Layout Snapshot (Top Layer)





3.2.4 Rework to Enable I2S on RVP for ALC1308

Description: Defining the path for Amplifier to operate in I^2S mode in RVP.

Impact if done:

TGL-UP3:

Camera functionalities such as privacy led and also retimer force power will not work

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL191502, IPTL191701, IPTY190802, IPTY191801, IPTY191901, IPTY191902, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTL201901, IPTY193902, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-17. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R3F68 R3F63 R3F92 R3F70	NA	33 Ohm, 5%, 1/16 W, 0402
Unstuff	Resistor	R3F69 R3F61 R3F71 R4F54 R3F93 R3F20	33 Ohm, 5%, 1/16 W, 0402	NA
Unstuff	Resistor	R2J27 R3F46 R4F76	0 Ohm, 5%, 1/16 W, 0402	NA
Stuff	Resistor	R3F21 R3F45 R4F77	NA	33 Ohm, 5%, 1/16 W, 0402
Stuff	Resistor	R2J26	NA	0 Ohm, 5%, 1/16 W, 0402

Note: Rework is not tested

Table 3-18. Reference Designator Comparison

Action	TGL UP3 RVP (DDR4)	TGL UP3 LP4x	TGL UP3 LP5
Un-Stuff	R3F69, R3F61, R3F71, R3F93, R4F54, R3F20, R2J27, R3F46, R4F76	R3F66, R3F60, R3F91, R3F70, R4F53, R3F21, R2J25, R3F44, R4F75	R3F67, R3F63, R3F93, R3F72, R4F50, R3F21, R2J26, R3F45, R4F72
Stuff	R3F68, R3F63, R3F92, R3F70, R3F21, R2J26, R3F45, R4F77	R3F68, R3F62, R3F92, R3F71, R3F22, R2J26, R3F46, R4F77	R3F69, R3F61, R3F91, R3F70, R3F24, R2J25, R3F47, R4F71

Figure 3-37. Schematic Snapshot

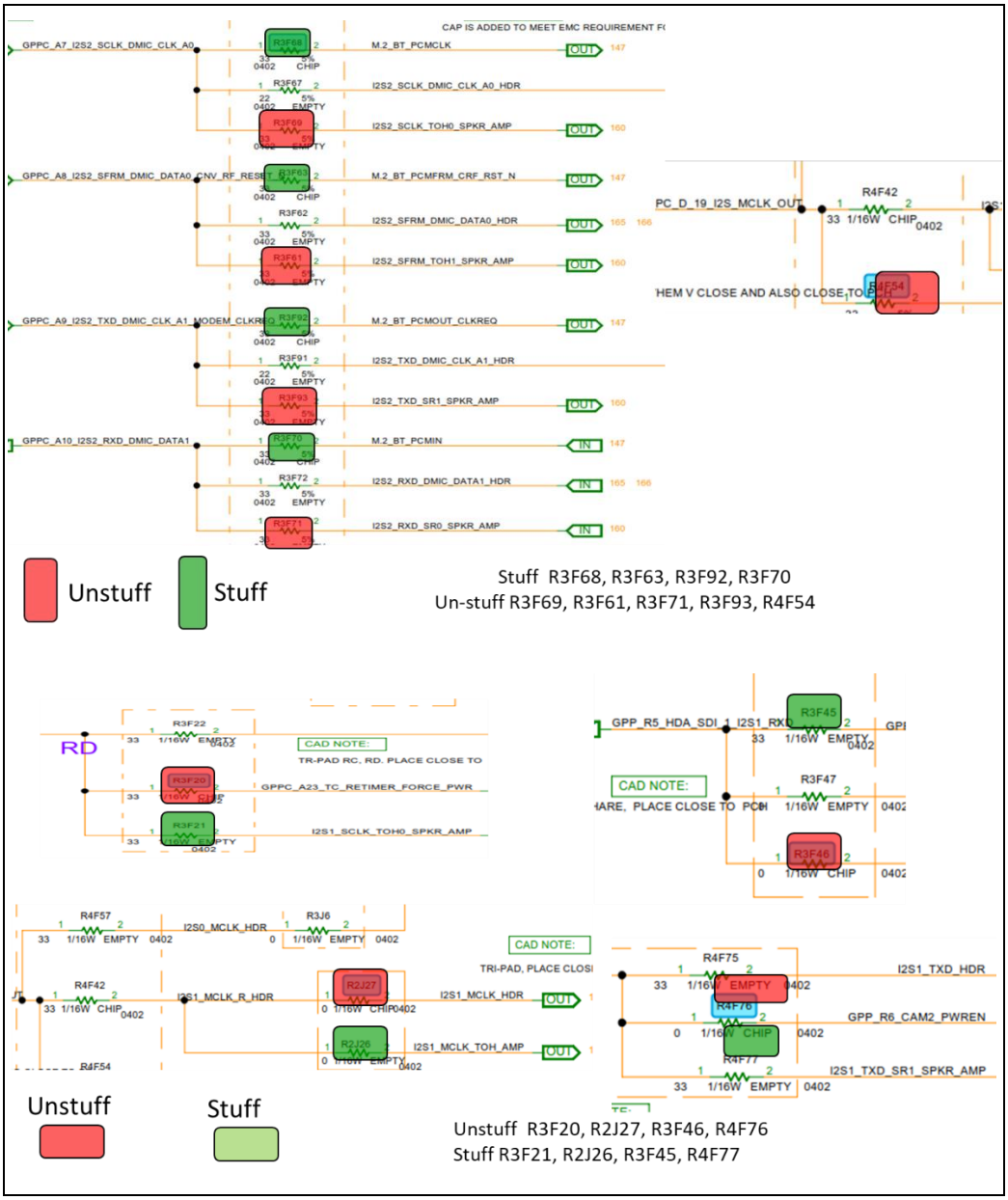
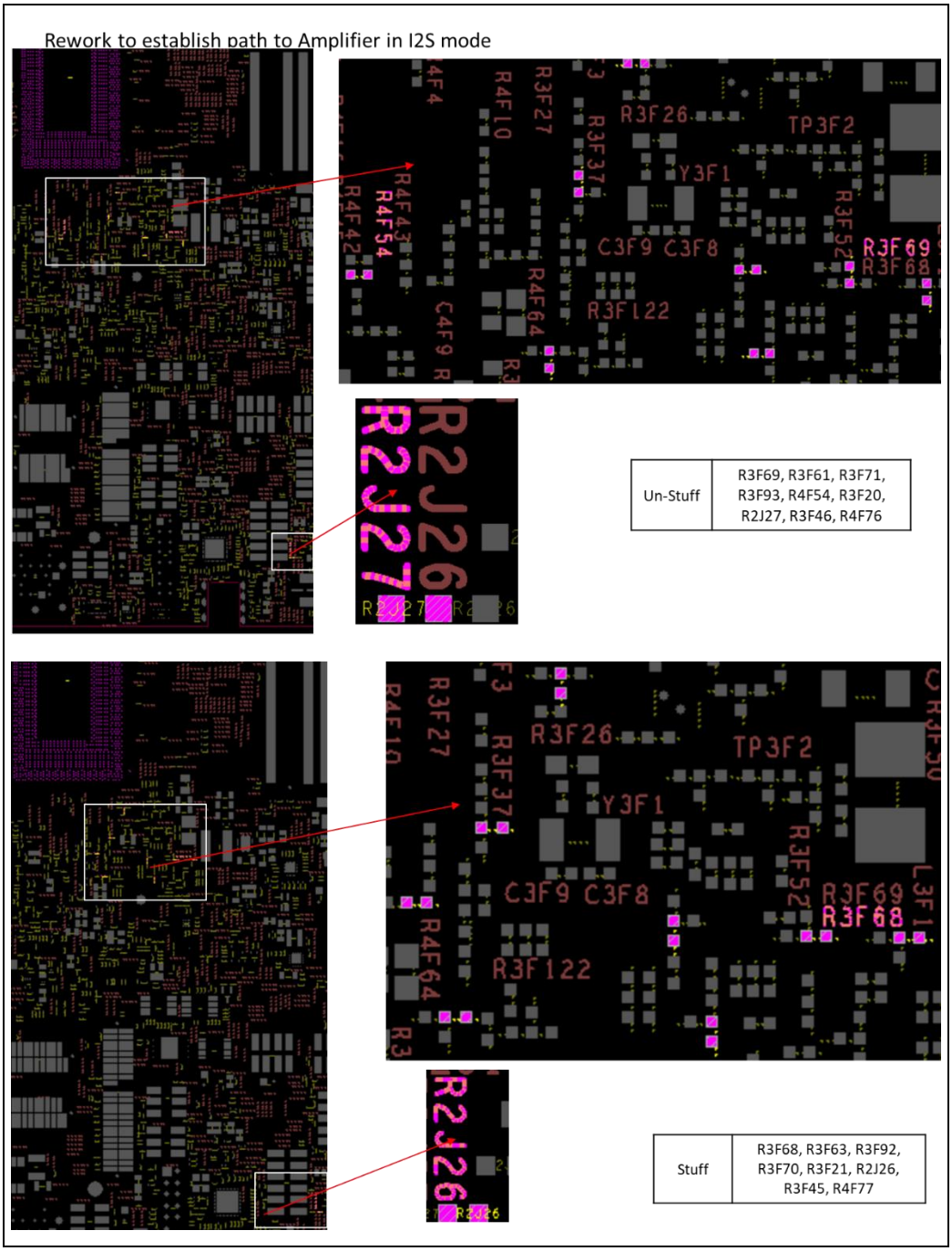


Figure 3-38. Layout Snapshot (Top Layer)



3.2.5 Rework to Enable I2S on AIOC for ALC1308

Description: Defining the path for Amplifier to operate in I^2S mode in AIOC.

Impact if done: Implementing this rework enables I^2S path for ALC1308 to AIC via RVP header. M.2 BT® is disabled onboard.

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL191502, IPTL191701, IPTY190802, IPTY191801, IPTY191901, IPTY191902, IPTY191903, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTL201901, IPTY193902, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-19. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R3F68 R3F63 R3F92 R3F70	33 Ohm, 5%, 1/16 W, 0402	NA
Stuff	Resistor	R3F67 R3F62 R3F72 R3F91	NA	33 Ohm, 5%, 1/16 W, 0402

NOTE: The Schematic reference description and layout snapshot refer to Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit (#609003).

Figure 3-39. Schematic Snapshot

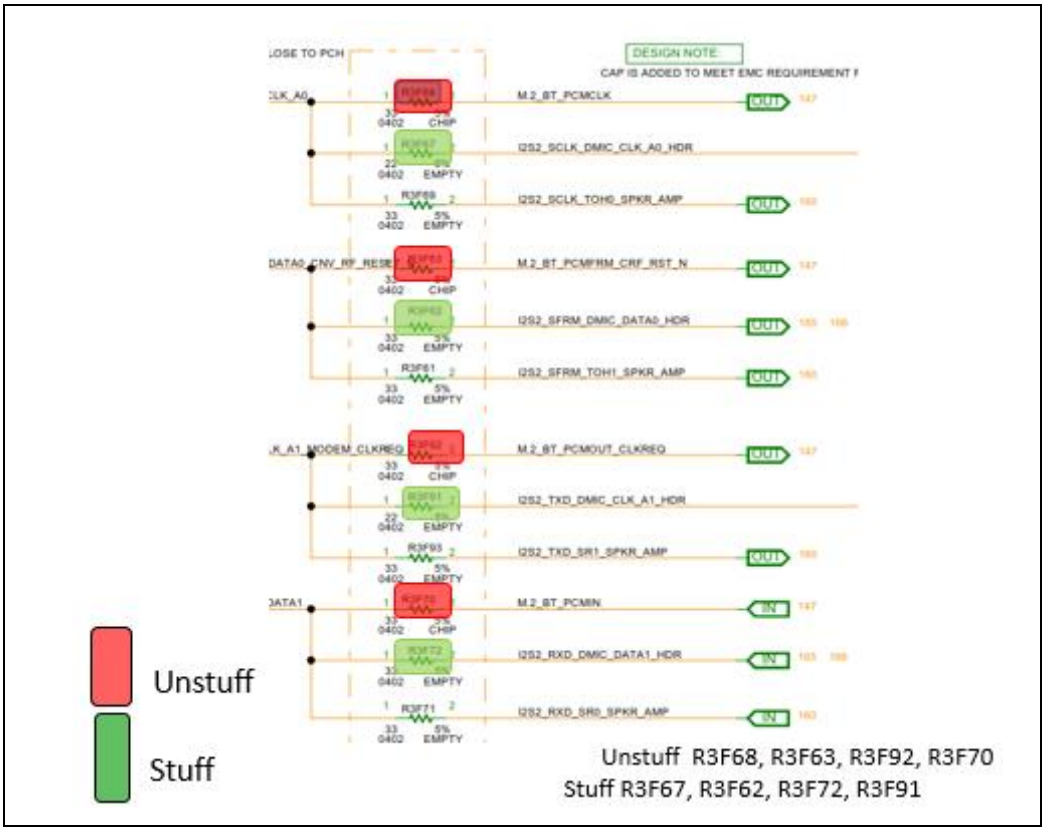
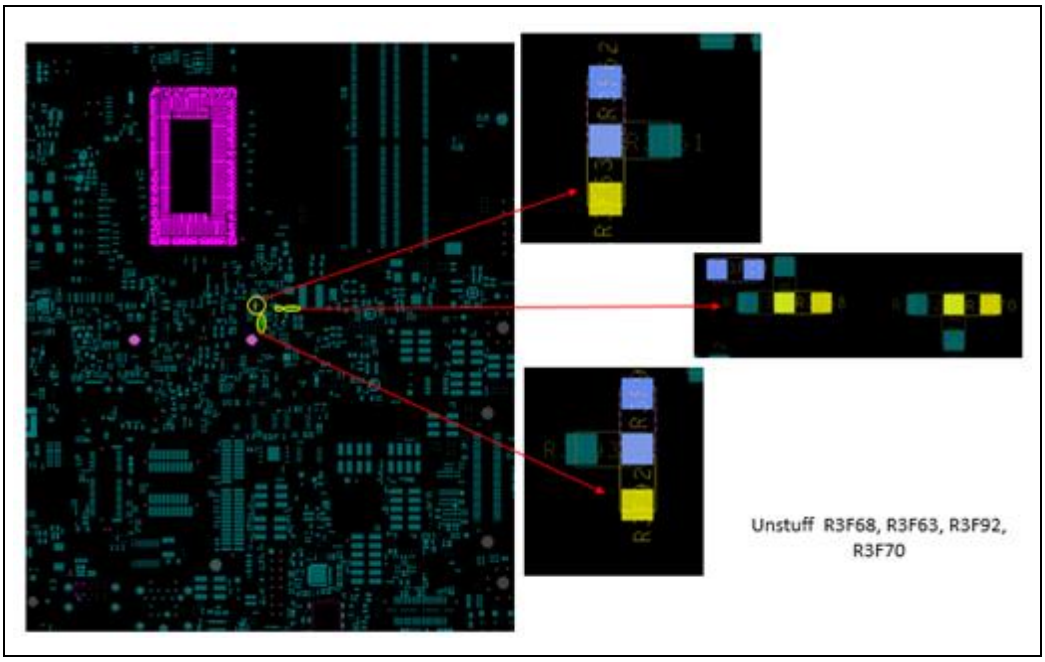
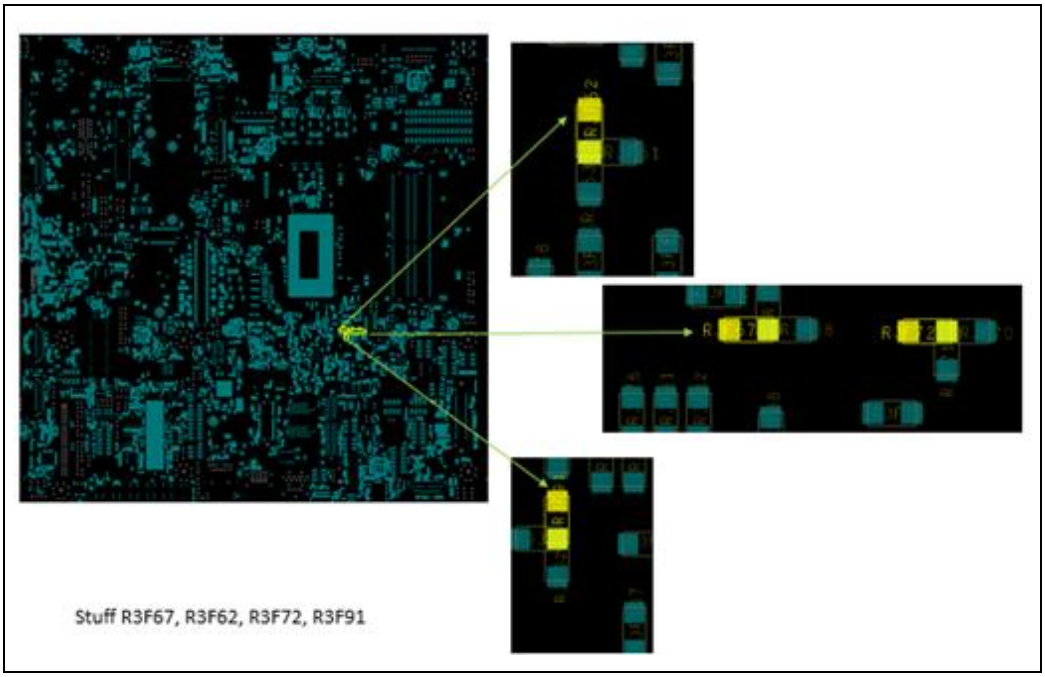


Figure 3-40. Layout Snapshot (Top Layer)





3.2.6 Rework to Enable BBR Bypass Mode on TCP2 Port of TGL UP3 DDR4 RVP

Description: This rework would enable USB-C connector 5 in USB/DP mode by bypassing the Burnside bridge re-timer.

Impact if done: This rework disables the USB-C connector 3.

Details: SMD Resistor and Capacitor rework

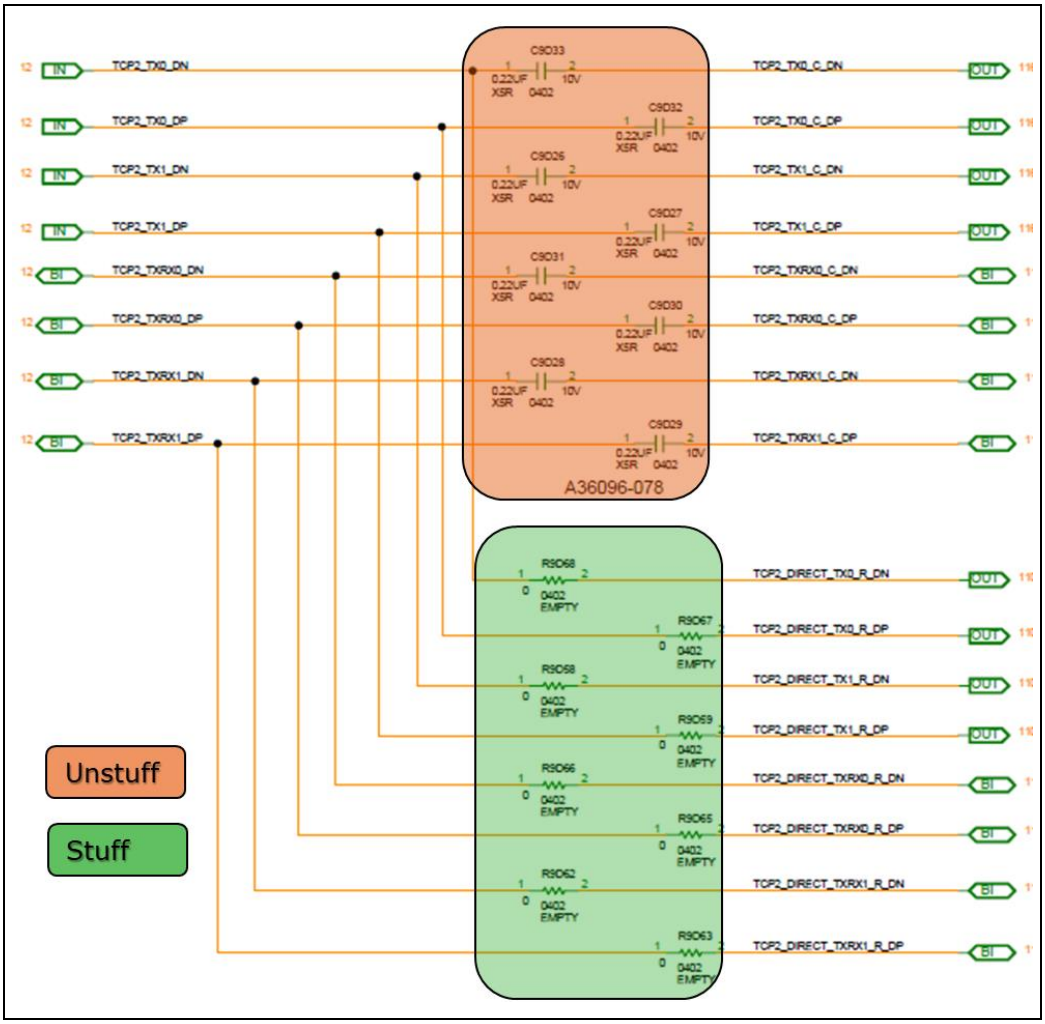
Applicable To: TGL UP3 DDR4 RVP

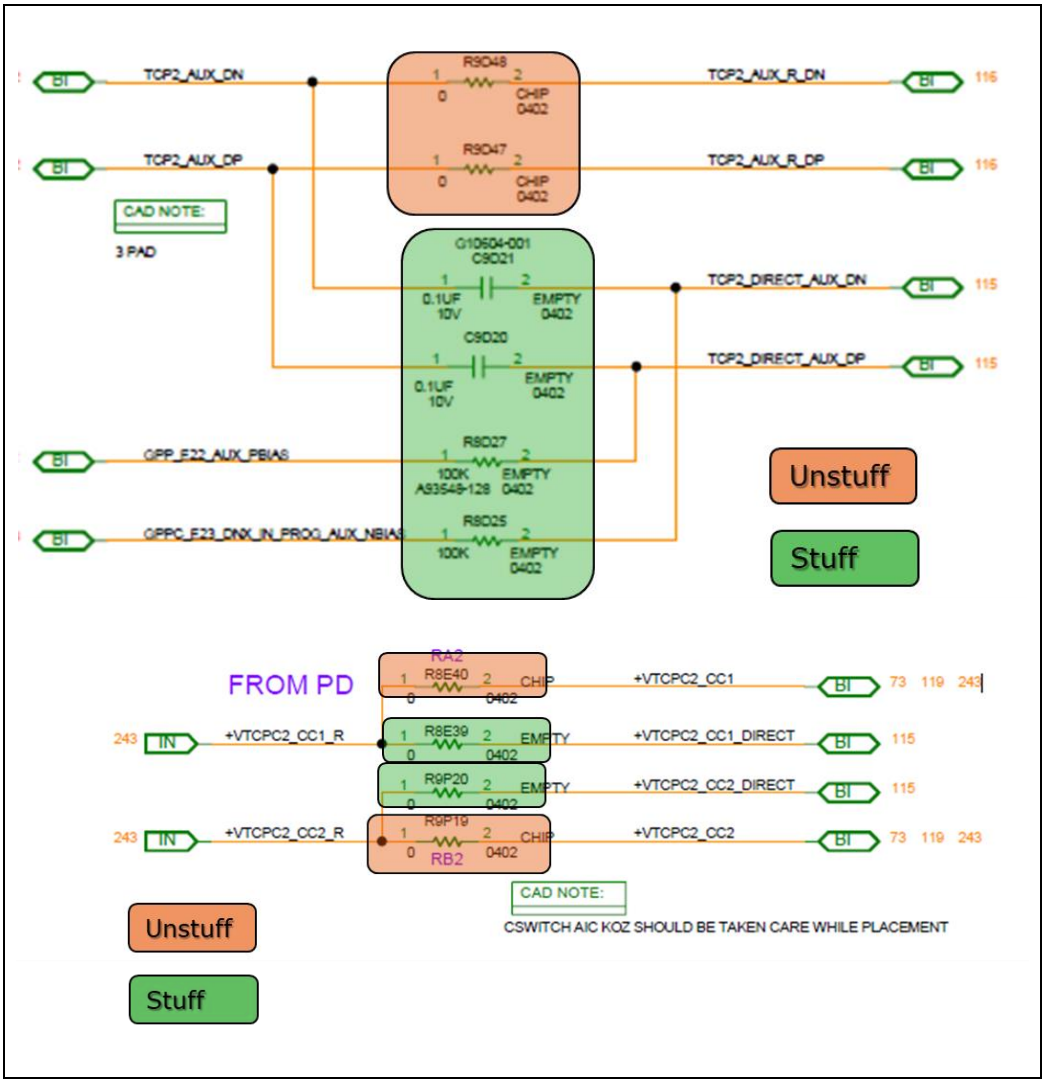
WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

Table 3-20. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Capacitor	C9D33 C9D32 C9D26 C9D27 C9D31 C9D30 C9D28 C9D29	0.22uF, x5R,10 V, 0402	NA
Stuff	Resistor	R9D68 R9D67 R9D58 R9D59 R9D66 R9D65 R9D62 R9D63	NA	0, 0402, 5%
Unstuff	Resistor	R9D48 R9D47	0, 0402, 5%	NA
Stuff	Capacitor	C9D21 C9D20	NA	0.1uF, 10 V, 0402
Stuff	Resistor	R8D27 R8D25	NA	100K, 0402, 5%
Unstuff	Resistor	R8E40 R9P19	0 ohm, 0402, 5%	NA
Stuff	Resistor	R8E39 R9P20	NA	0 ohm, 0402, 5%
Unstuff	Resistor	R7D20 R7D18	0 ohm, 0402, 5%	NA
Stuff	Resistor	R7D21 R7D19	NA	0 ohm, 0402, 5%
Stuff	Resistor	R9N1	NA	RES_D,1206,2.00mOHM
Unstuff	Resistor	R9P8	RES_D,1206,2.00m OHM	NA

Figure 3-41. Schematic Snapshot




TCP2_AUX_DN
TCP2_AUX_DP
R9D48
R9D47
CHIP
0402
TCP2_AUX_R_DN
TCP2_AUX_R_DP
CAD NOTE:
3 PAD
G10604-001
C9D21
0.1UF
10V
EMPTY
0402
C9D20
TCP2_DIRECT_AUX_DN
TCP2_DIRECT_AUX_DP
GPP_E22_AUX_PBIAS
R8D27
100K
A93548-128
R8D25
GPPC_E23_DNX_IN_PROG_AUX_NBIAS
Unstuff
Stuff
FROM PD
RA2
R8E40
+VTCPC2_CC1
+VTCPC2_CC1_R
R8E39
+VTCPC2_CC1_DIRECT
R9P20
+VTCPC2_CC2_DIRECT
R9P19
RB2
+VTCPC2_CC2_R
+VTCPC2_CC2
CAD NOTE:
CSWITCH AIC KOZ SHOULD BE TAKEN CARE WHILE PLACEMENT
Unstuff
Stuff

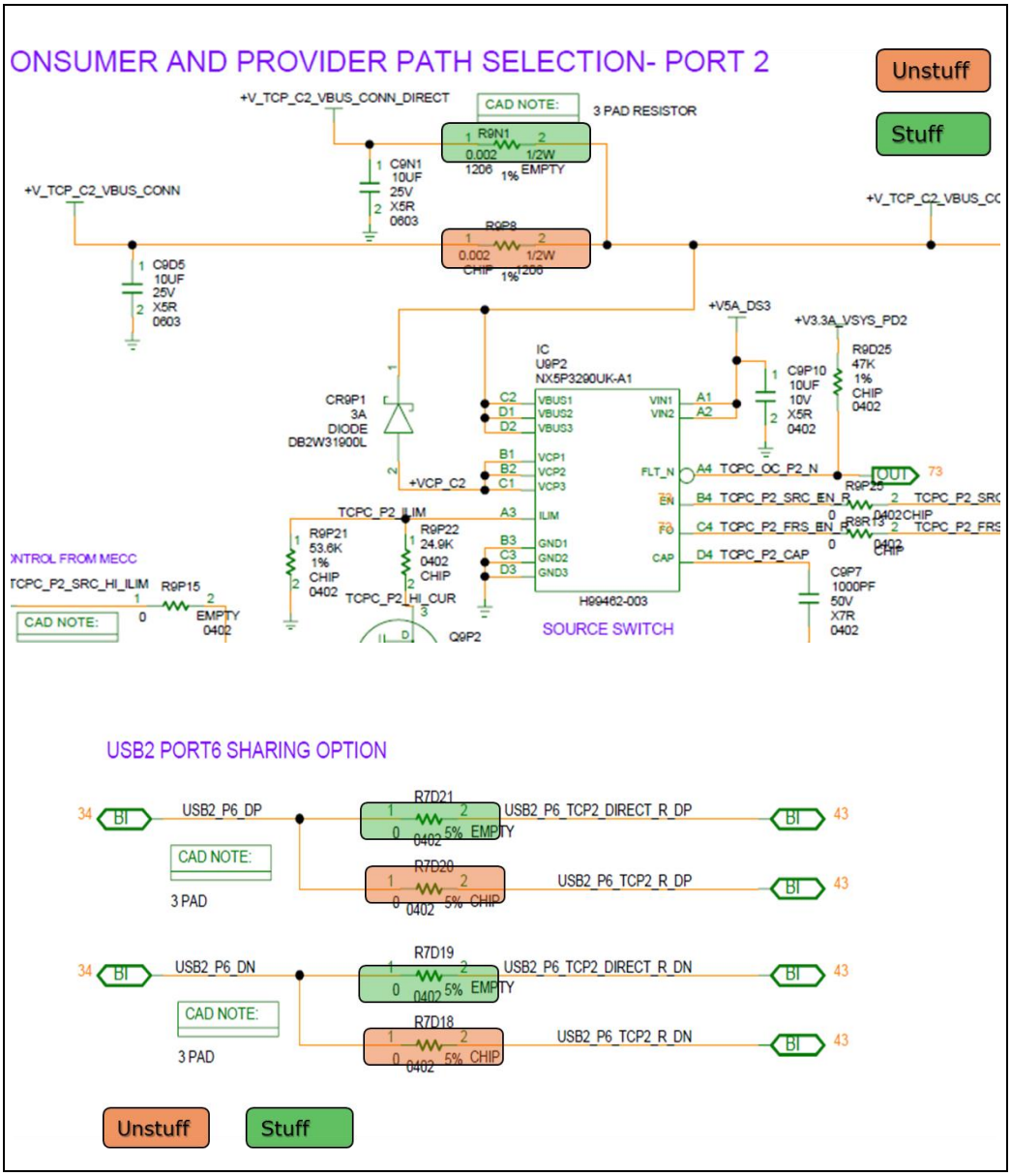
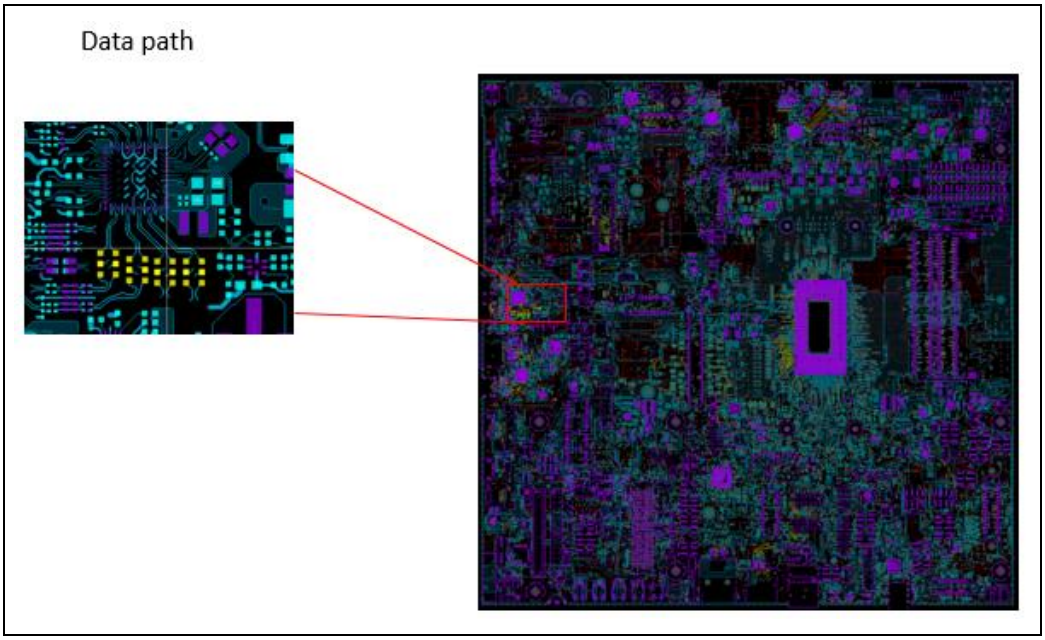
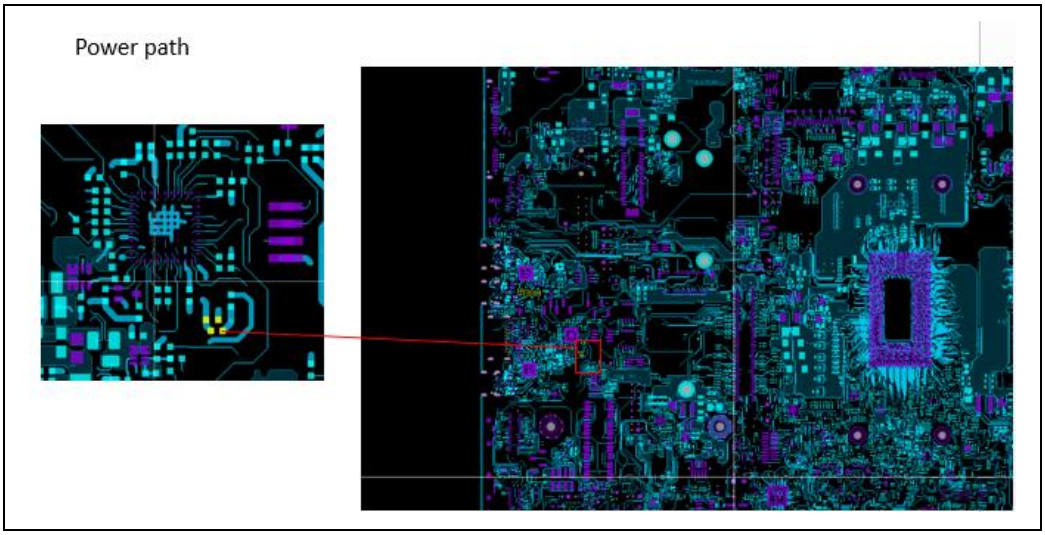
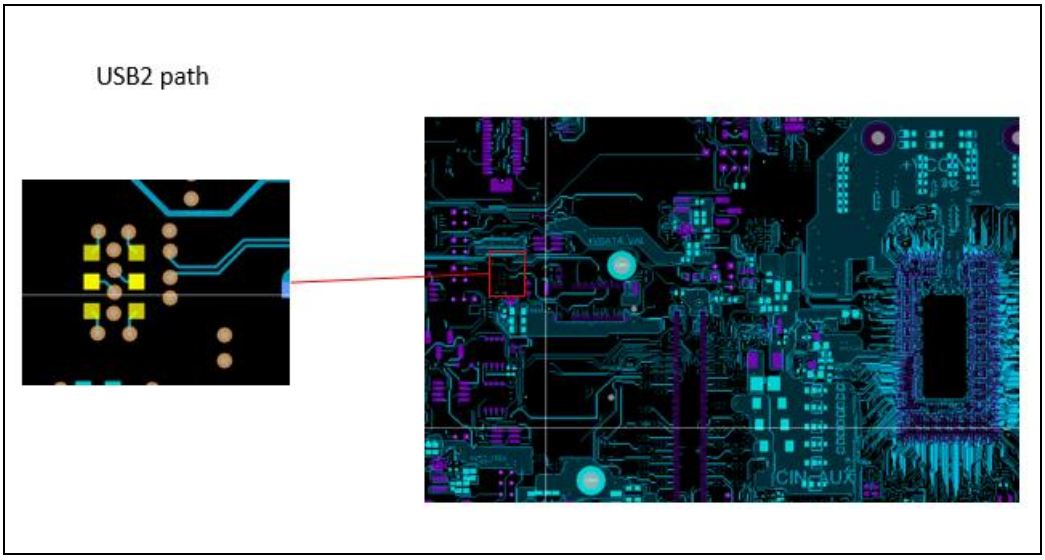

ONSUMER AND PROVIDER PATH SELECTION- PORT 2
Unstuff
Stuff
+V_TCP_C2_VBUS_CONN_DIRECT
CAD NOTE:
3 PAD RESISTOR
R9N1
0.002
1/2W
1206
1%
EMPTY
C9N1
10UF
25V
X5R
0603
+V_TCP_C2_VBUS_CONN
R9P8
0.002
1/2W
CHIP
1%
1206
C9D5
10UF
25V
X5R
0603
+V5A_DS3
+V3.3A_VSYS_PD2
R9D25
47K
1%
CHIP
0402
C9P10
10UF
10V
X5R
0402
IC
U9P2
NX5P3290UK-A1
CR9P1
3A
DIODE
DB2W31900L
VBUS1
VBUS2
VBUS3
VIN1
VIN2
VCP1
VCP2
VCP3
FLT_N
A4 TCPC_OC_P2_N
OUT
73
+VCP_C2
TCPC_P2_ILIM
ILIM
EN
B4 TCPC_P2_SRC_EN_R
TCPC_P2_SRC
FO
C4 TCPC_P2_FRS_EN_R
TCPC_P2_FRS
R9P21
53.6K
1%
CHIP
0402
R9P22
24.9K
0402
CHIP
GND1
GND2
GND3
CAP
D4 TCPC_P2_CAP
C9P7
1000PF
50V
X7R
0402
H99462-003
SOURCE SWITCH
TCPC_P2_HI_CUR
Q9P2
NTROL FROM MECC
TCPC_P2_SRC_HI_ILIM
R9P15
EMPTY
0402
CAD NOTE:
USB2 PORT6 SHARING OPTION
34
BI
USB2_P6_DP
R7D21
USB2_P6_TCP2_DIRECT_R_DP
EMPTY
CAD NOTE:
3 PAD
R7D20
USB2_P6_TCP2_R_DP
CHIP
43
USB2_P6_DN
R7D19
USB2_P6_TCP2_DIRECT_R_DN
R7D18
USB2_P6_TCP2_R_DN
Unstuff
Stuff

Figure 3-42. Layout Snapshot (Top Layer)







Extra information:
- USBC 3 connector will not work after the rework.
- This rework would need support from IFWI for the DP alternate mode support.

3.2.7 Rework to Enable DP++ Connector (Standard Size) on Dekel PHY-Type C Port 4 on TGL UP3 DDR4 RVP

Description: This rework is to enable DP++ port on Type C Port 4.

Impact if done: Type C Port 4 J9F1 will not work.

Details: SMD Capacitor and Resistor rework

Applicable To: TGL UP3 DDR4 RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTY193902, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

Table 3-21. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Capacitor	C9E26 C9E24 C9E17 C9E14 C9E29 C9E27 C9E20 C9E19 C9E10 C9E11	NA	Cap, 0402, 0.1UF
Stuff	Resistor	R4G17 R4F47	NA	Res, 0402, 0 Ohm
Unstuff	Capacitor	C9E25 C9E23 C9E16 C9E15 C9E30 C9E28 C9E21 C9E18	CAPC, X5R, 0402, 0.220UF, 10 V	NA
Unstuff	Resistor	R9E26 R9E27 R4G18 R4F45	Res, 0402, 0 Ohm	NA

Figure 3-43. Schematic Snapshot

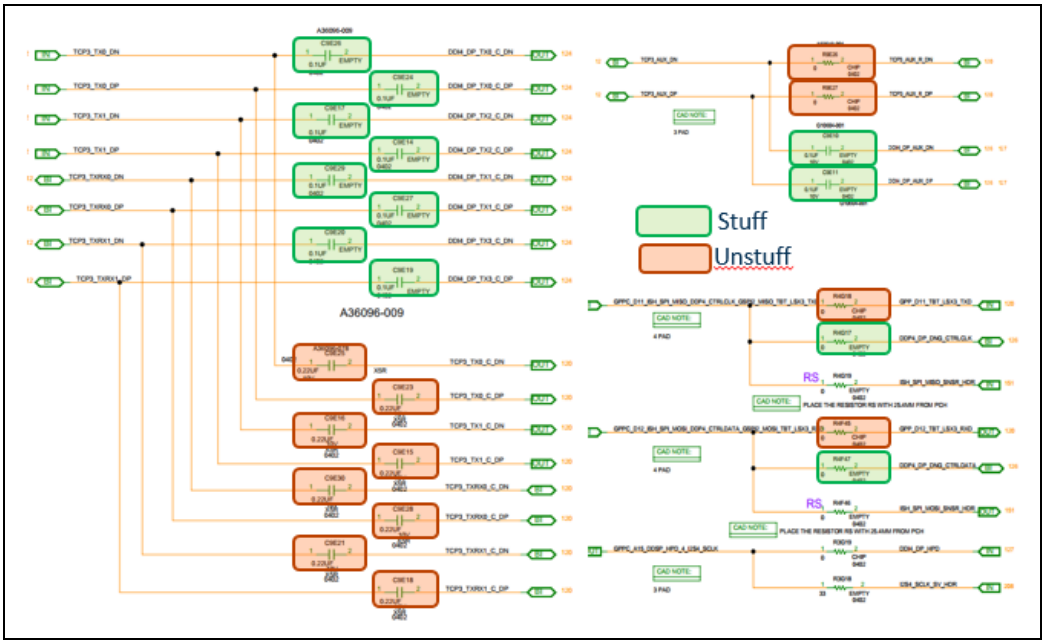
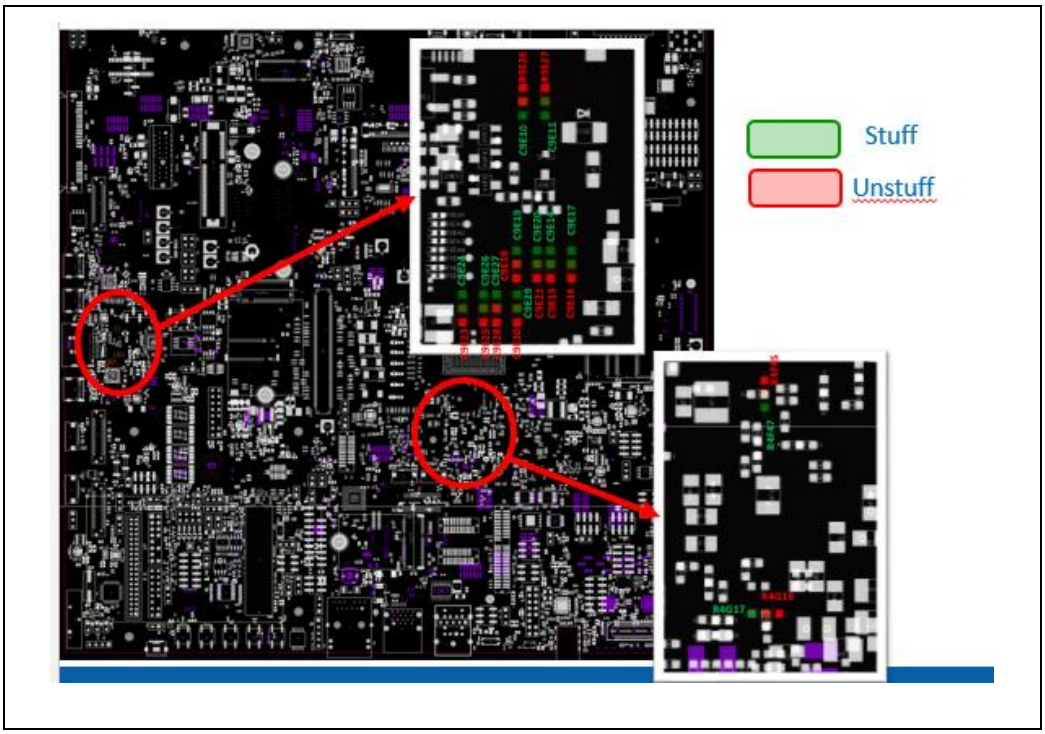


Figure 3-44. Layout Snapshot (Top Layer)



Extra information:
- Need to set Dekel Phy 4th Port in DDI mode in soft strap.
- VBIOS should configure this Type-c port as DP++ port

3.2.8 Rework to Enable PCH Debug Support on PCH MIPI60 Port on TGL UP3 RVP

Description: This rework is to enable PCH Debug on PCH MIPI60 port.

Impact if done: Certain GPIO cannot be used after performing the rework.

Details: SMD Resistor rework

Applicable To: TGL UP3 RVP boards

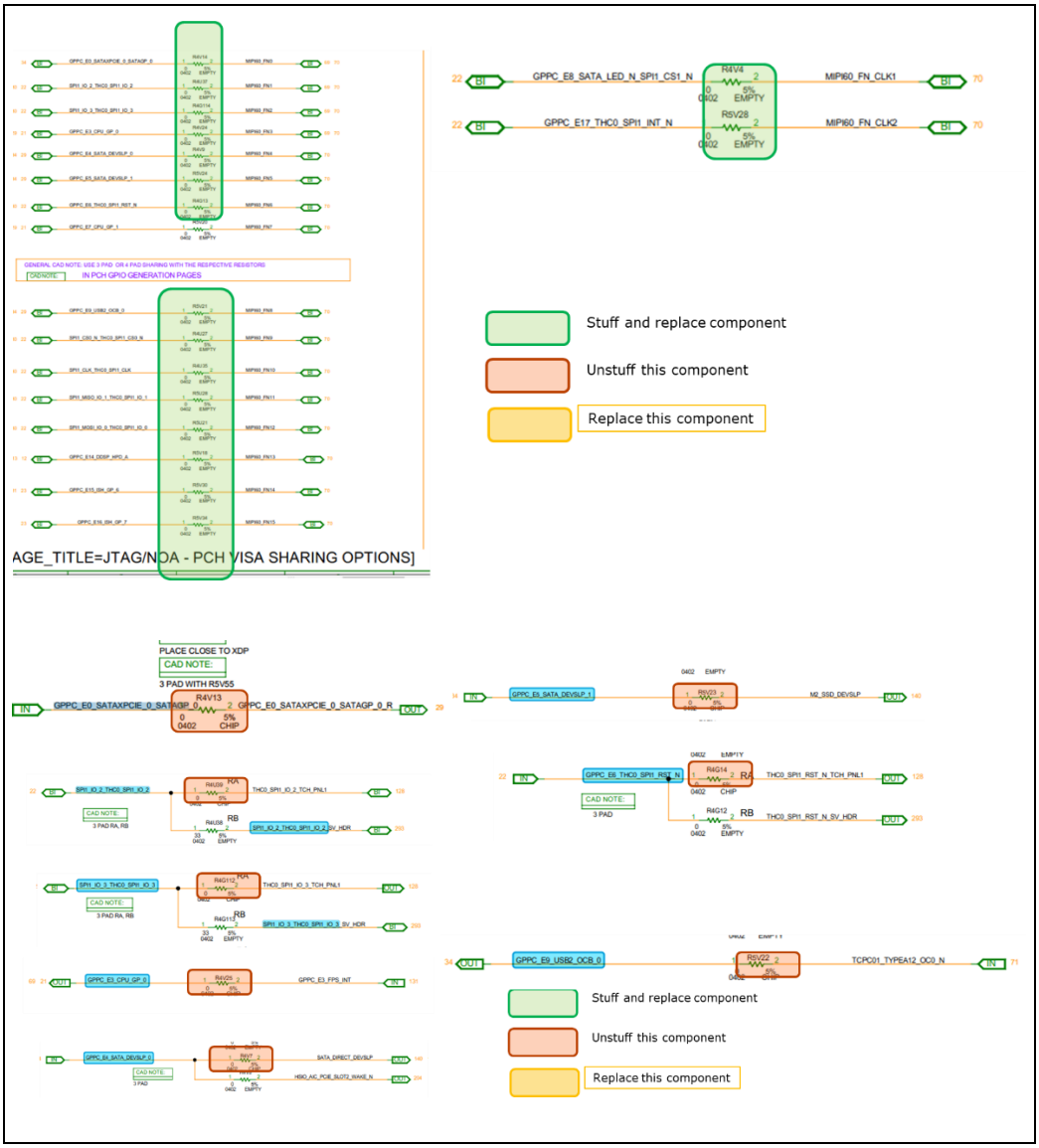
WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL191502, IPTL191701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL201201, IPTL201901, IPTL194202, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-22. Rework Details

Schematic reference description and layout snapshots are from Tiger Lake UP3 DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit (#609003).

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R4V13 R4U39 R4G112 R4V25 R4V7 R5V23 R4G14 R5V22 R4U28 R4U33 R5U29 R5U23 R5V17 R5V27 R5V32 R5V33 R4V5	RES D, 0402, 0.0 Ohm, 5.00%, 1/10 W	NA
Stuff	Resistor	R4V14 R4U37 R4G114 R4V24 R4V9 R5V24 R4G13 R5V21 R4U27 R4U35 R5U28 R5U21 R5V18 R5V30 R5V34 R4V4 R5V28	NA	RES D, 0402, 0.0 Ohm, 5.00%, 1/10 W

Figure 3-45. Schematic Snapshot



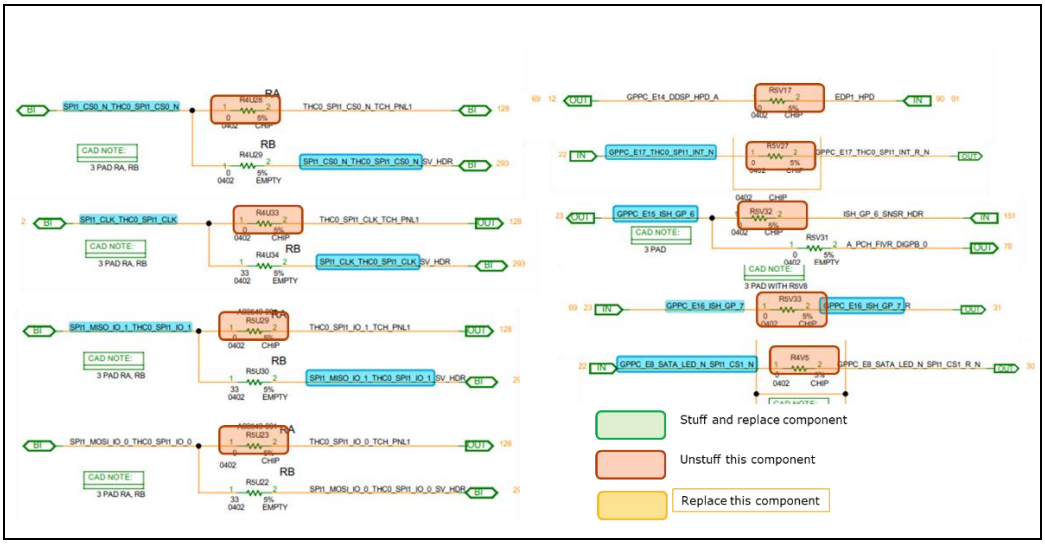


Figure 3-46. Layout Snapshot (Top Layer)

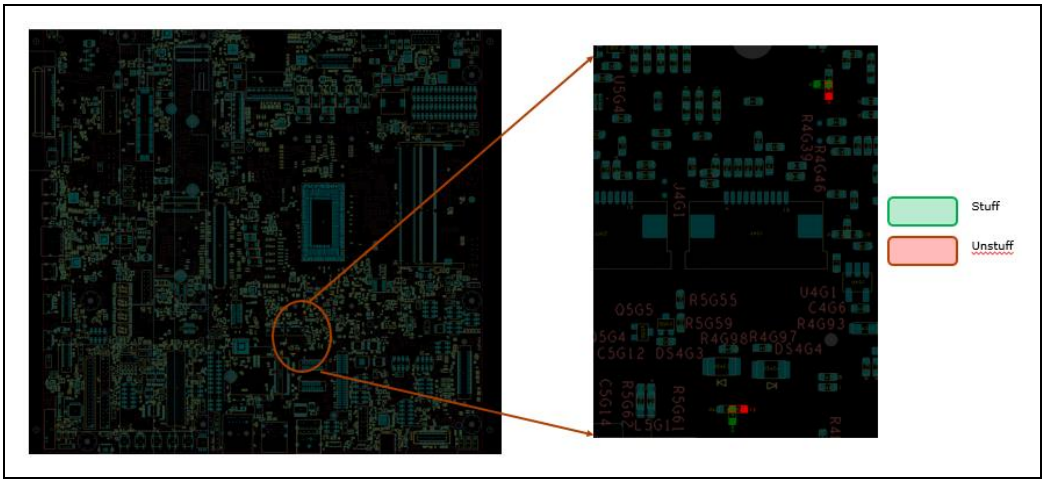
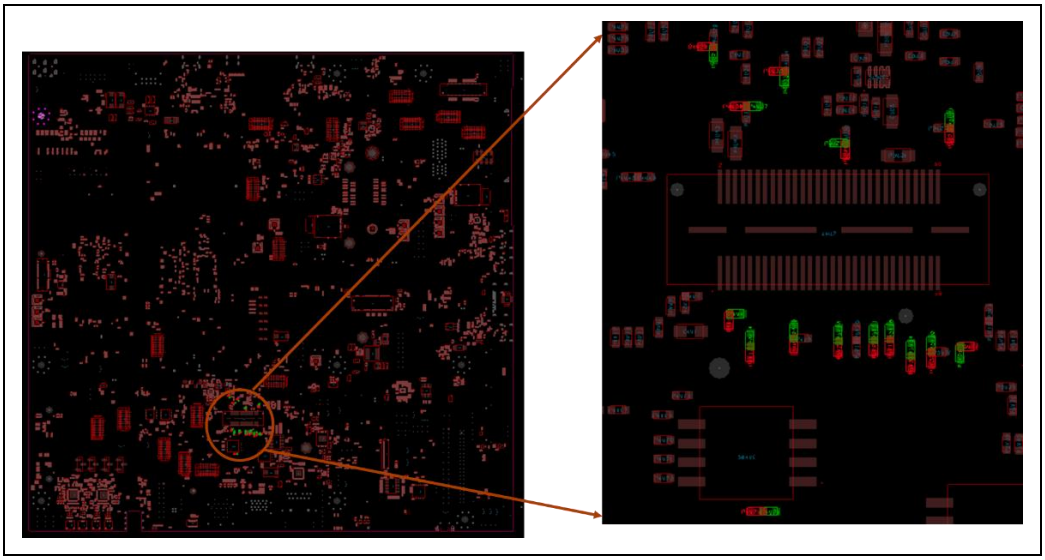


Figure 3-47. Layout Snapshot (Bottom Layer)



3.2.9 Rework to Enable USB-based BT® on TGL UP3 RVP

Description: Rework to enable USB-based BT®.

Impact if done: After performing the rework, we can use the FPS on USB.

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTY201701 and IPTL191001

Table 3-23. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R5F42 R5F41	RES D, 0402, 0.0 Ohm, 5.00%, 1/10 W	NA
Stuff	Resistor	R5F35 R5F36	NA	RES D, 0402, 0.0 Ohm, 5.00%, 1/10 W

Figure 3-48. Schematic Snapshot

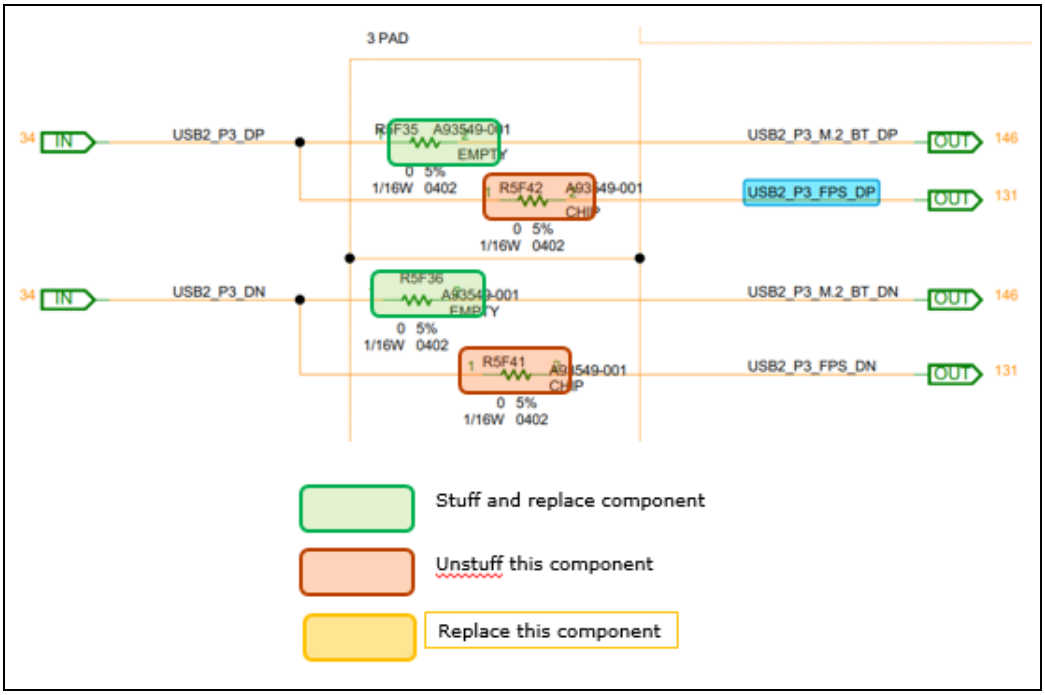
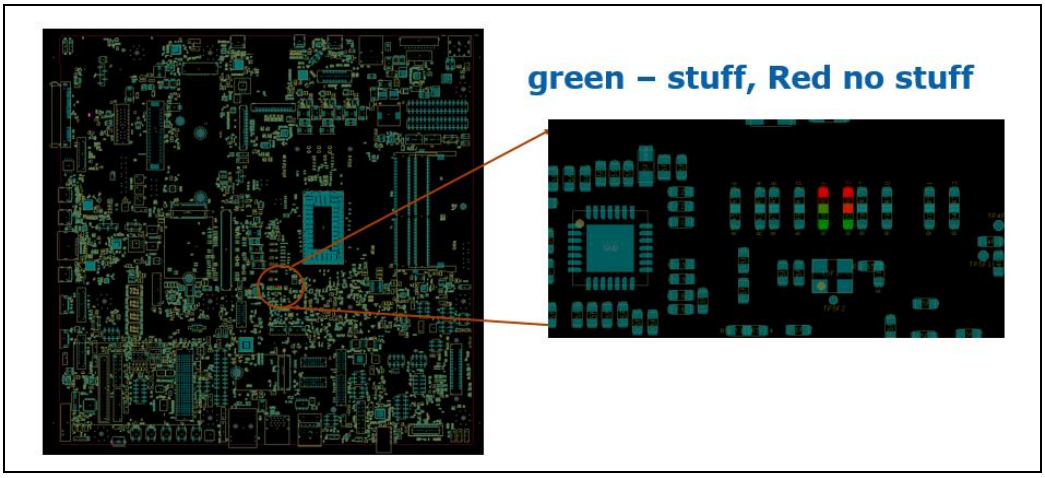


Figure 3-49. Layout Snapshot (Top Layer)



3.2.10 Rework to Enable SATA Port Connected to SATA Connector on RVP

Description: This rework is done to use the SATA connector on RVP.

Impact if done: After performing the rework, M.2 PCH slot connected to NVMe* SSD does not work.

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL191502, IPTL191701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL201201, IPTL201901, IPTL194202, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-24. Rework Details

Schematic reference description and layout snapshots are from TGL UP3 DDR4 SODIMM RVP board.

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R6E72 R6E79 R6E66 R6E73	RES D, 0402, 0.0 Ohm, 5.00%, 1/10 W	NA
Stuff	Resistor	R6E70 R6E77 R6E67 R6E74	NA	RES D, 0402, 0.0 Ohm, 5.00%, 1/10 W

Figure 3-50. Schematic Snapshot

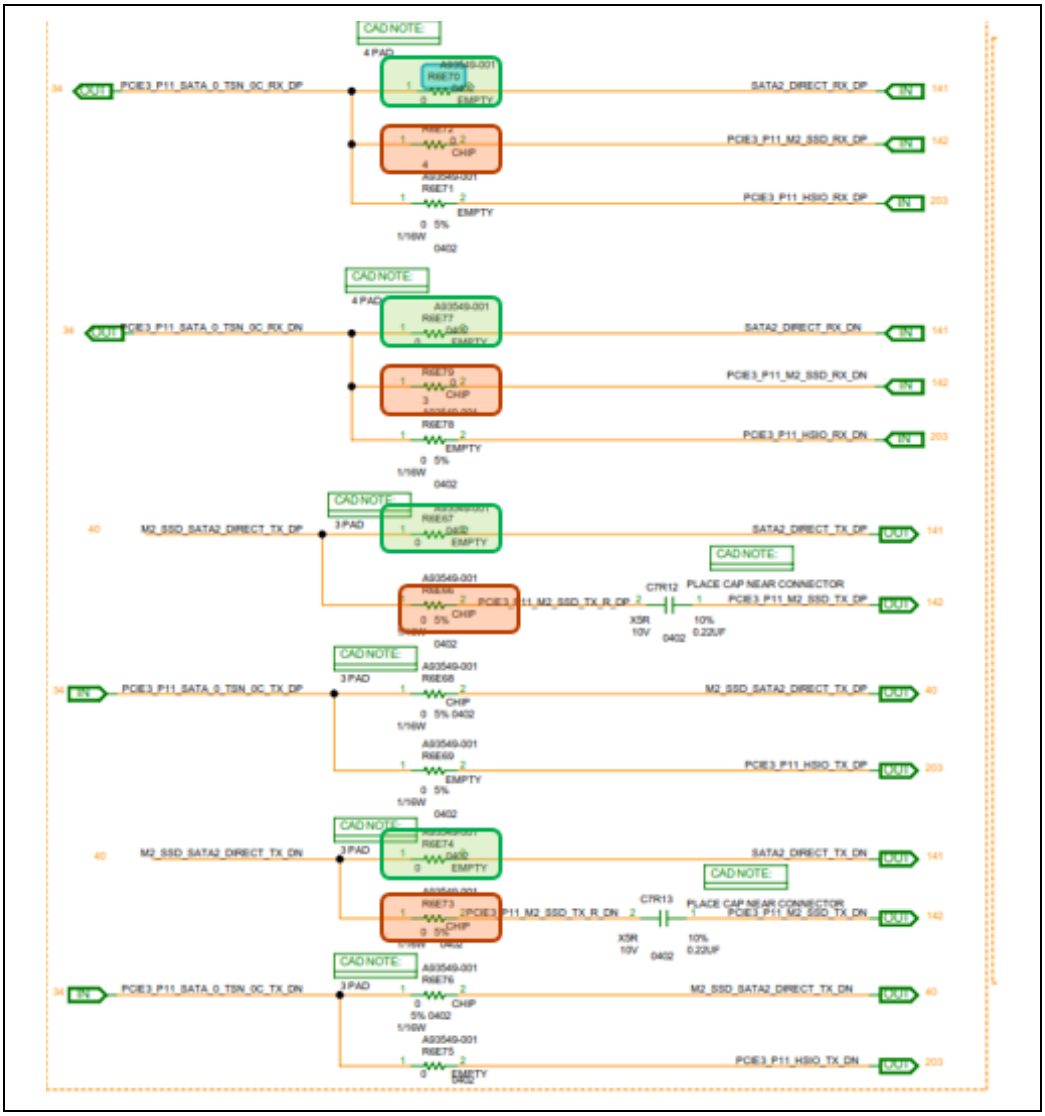
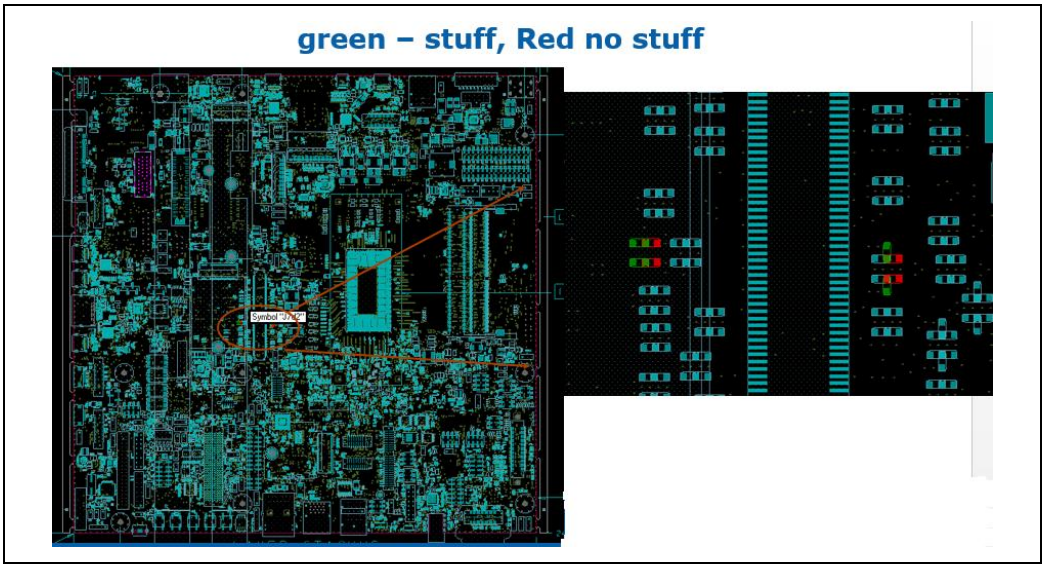


Figure 3-51. Layout Snapshot (Top Layer)



3.2.11 Rework to Enable PCIe* Gen4 on x4DT Slot

Description: To enable PCIe* Gen4 lanes on x4 DT slot on TGL UP3 DDR4 A0 boards.

Impact if done: After performing the reworks, PCIe* Gen4 lanes are connected to x4DT slot.

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL191502, IPTL191701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTL201901, IPTY193902, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-25. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R7N22 R7N17 R6N22 R6N20 R7N9 R7N6 R6N17 R6N15 R6N25 R6N24 R7N29 R7N33 R6N28 R6N30 R7N42 R7N45 R7C4 R7C5 R6E58 R6E63 R4G68 R7N27 R7N25 R7N32 R7N35 R7N38 R7N40 R7N43 R7N47 R7N24 R7N20 R7N16 R7N14 R7N12 R7N8 R7N4 R7N2 R7B12	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W	NA

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R7N21 R7N18 R6N21 R6N19 R7N10 R7N5 R6N18 R6N14 R6N26 R6N23 R7N30 R7N34 R6N27 R6N29 R7N41 R7N46 R7C3 R7C6 R6E59 R6E62 R4G69 R7N28 R7N26 R7N31 R7N36 R7N37 R7N39 R7N44 R7N48 R7N23 R7N19 R7N15 R7N13 R7N11 R7N7 R7N3 R7N1 R7B11	NA	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W

Table 3-26. Reference Designator Comparison Table

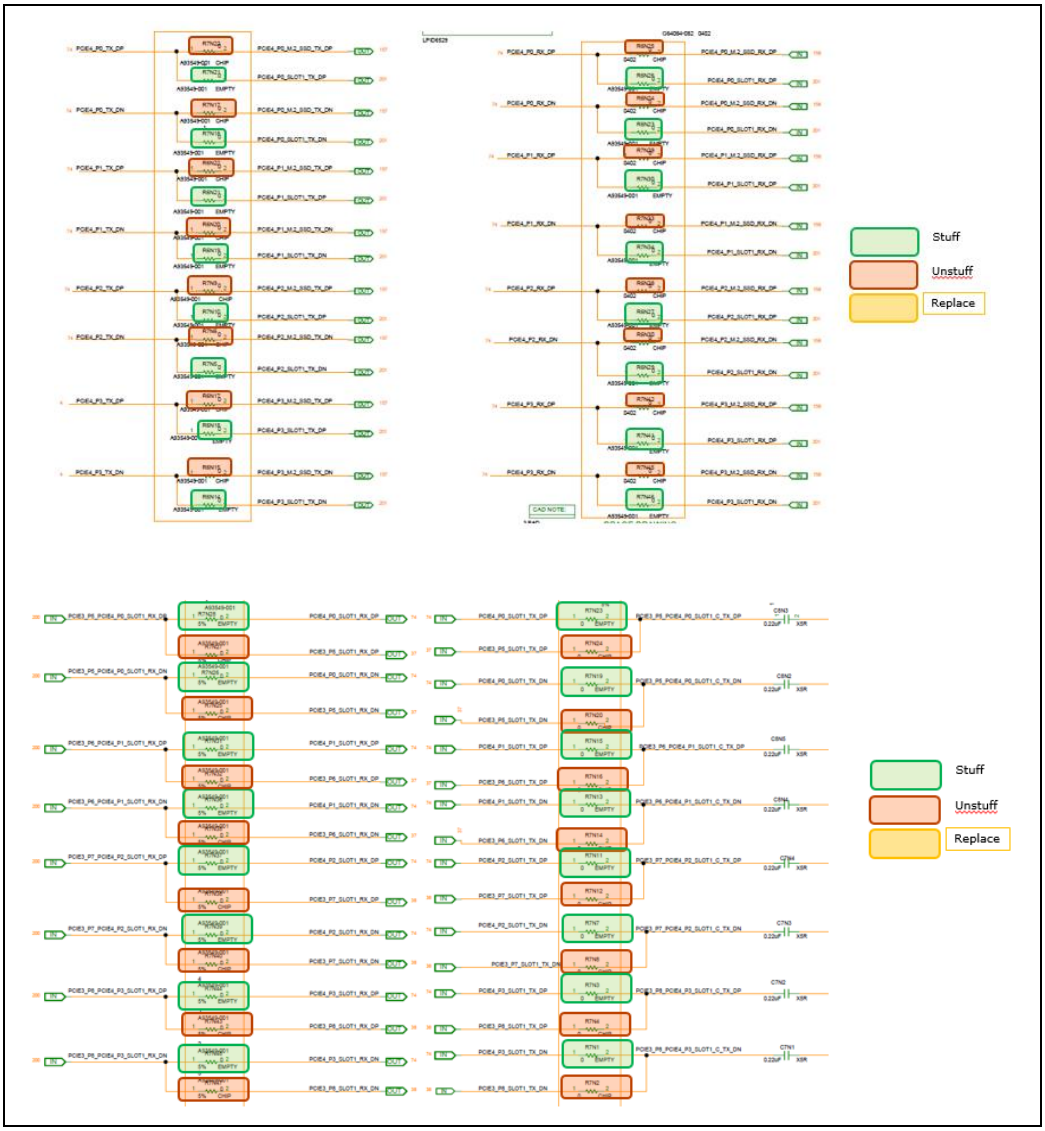
TGL UP3 DDR4 REFDES	TGL UP3 LP4x REFDES
R7N22	R7N22
R7N17	R7N18
R6N22	R6N22
R6N20	R6N19
R7N9	R7N10
R7N6	R7N5
R6N17	R6N17
R6N15	R6N14
R6N25	R6N25
R6N24	R6N23
R7N29	R7N29
R7N33	R7N33
R6N28	R6N27
R6N30	R6N29
R7N42	R7N42
R7N45	R7N46
R7C4	R7C4
R7C5	R7C5
R6E58	R6R17
R6E63	R6R14
R4G68	R4G72

TGL UP3 DDR4 REFDES	TGL UP3 LP4x REFDES
R7N27	R7N28
R7N25	R7N25
R7N32	R7N31
R7N35	R7N35
R7N38	R7N38
R7N40	R7N40
R7N43	R7N44
R7N47	R7N47
R7N24	R7N24
R7N20	R7N20
R7N16	R7N16
R7N14	R7N14
R7N12	R7N12
R7N8	R7N8
R7N4	R7N4
R7N2	R7N2
R7B12	R7B12
R7N21	R7N21
R7N18	R7N17
R6N21	R6N21
R6N19	R6N20
R7N10	R7N9
R7N5	R7N6
R6N18	R6N18

TGL UP3 DDR4 REFDES	TGL UP3 LP4x REFDES
R6N14	R6N15
R6N26	R6N26
R6N23	R6N24
R7N30	R7N30
R7N34	R7N34
R6N27	R6N28
R6N29	R6N30
R7N41	R7N41
R7N46	R7N45
R7C3	R7C3
R7C6	R7C6
R6E59	R6R16
R6E62	R6R13
R4G69	R4G71
R7N28	R7N27
R7N26	R7N26
R7N31	R7N32
R7N36	R7N36
R7N37	R7N37
R7N39	R7N39
R7N44	R7N43
R7N48	R7N48
R7N23	R7N23
R7N19	R7N19
R7N15	R7N15
R7N13	R7N13
R7N11	R7N11

TGL UP3 DDR4 REFDES	TGL UP3 LP4x REFDES
R7N7	R7N7
R7N3	R7N3
R7N1	R7N1
R7B11	R7B11

Figure 3-52. Schematic Snapshot



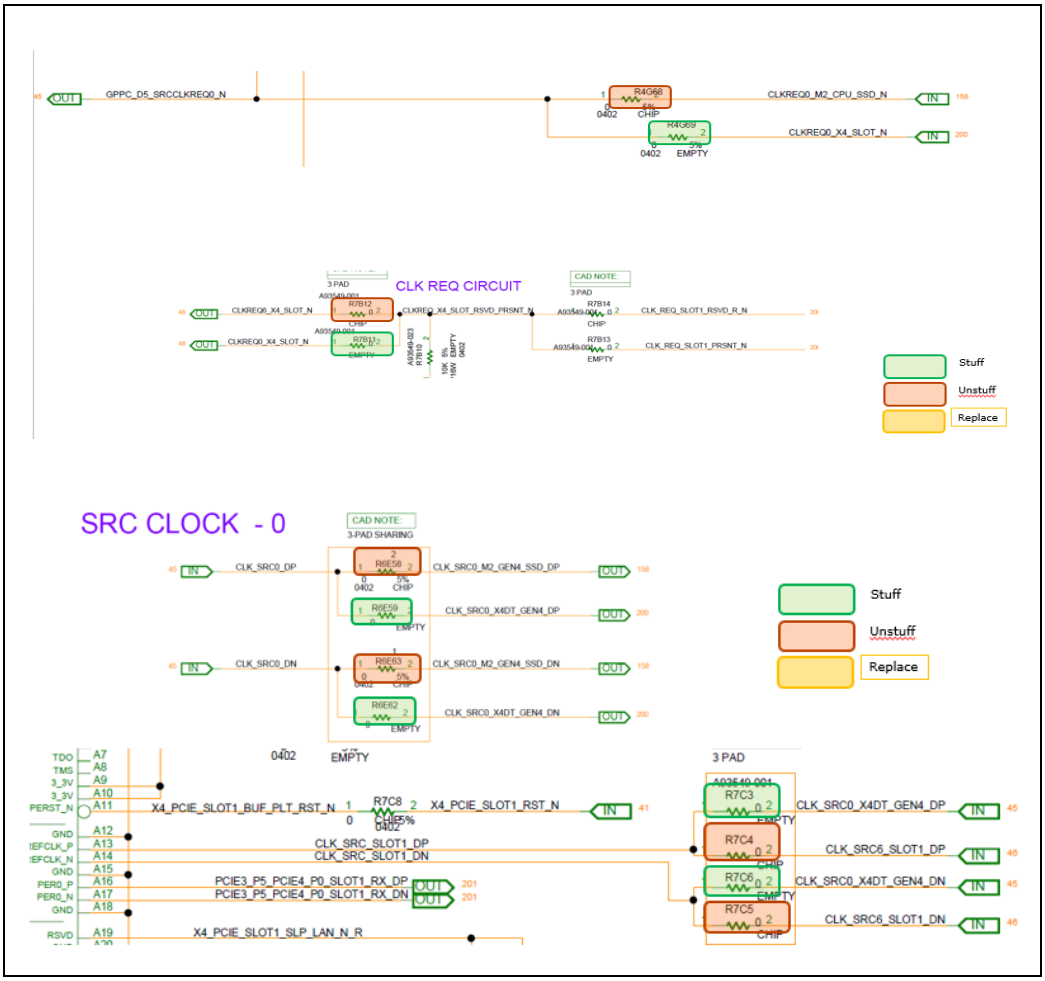
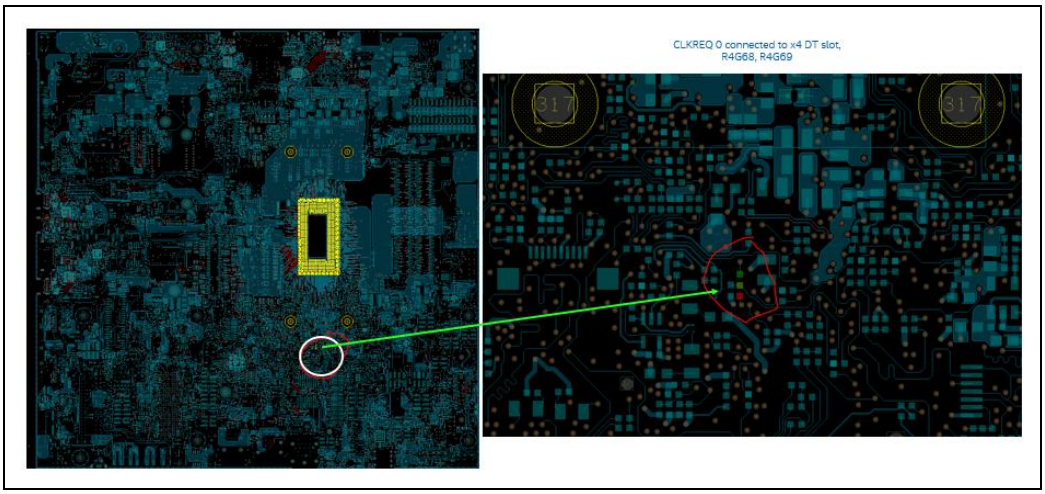
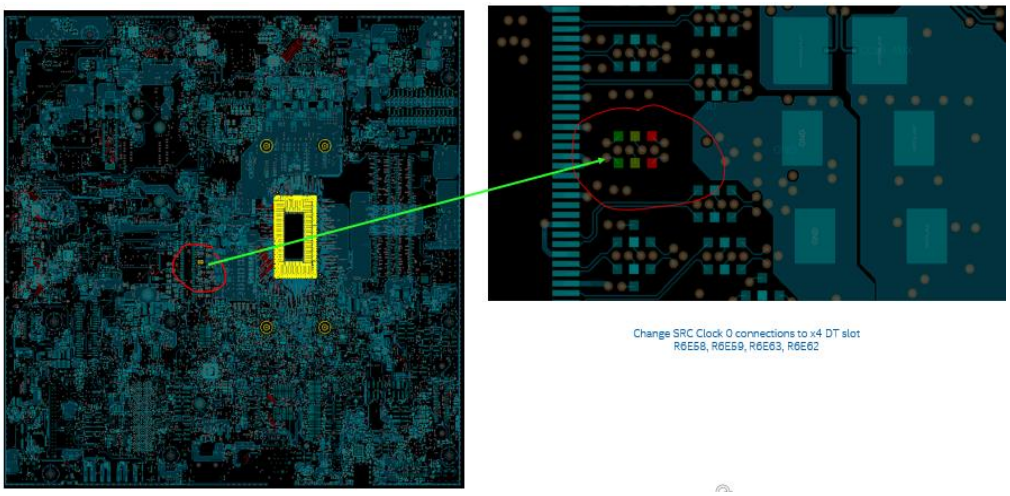
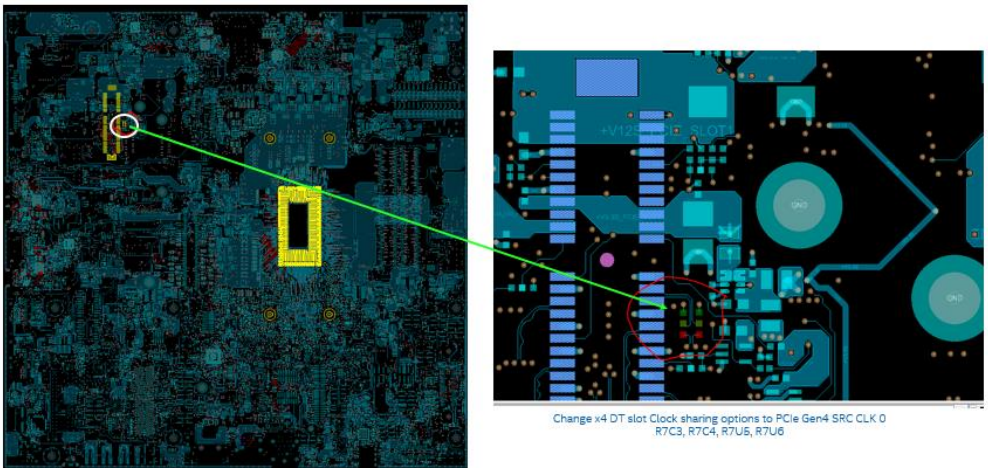


Figure 3-53. Layout Snapshot (Top Layer)

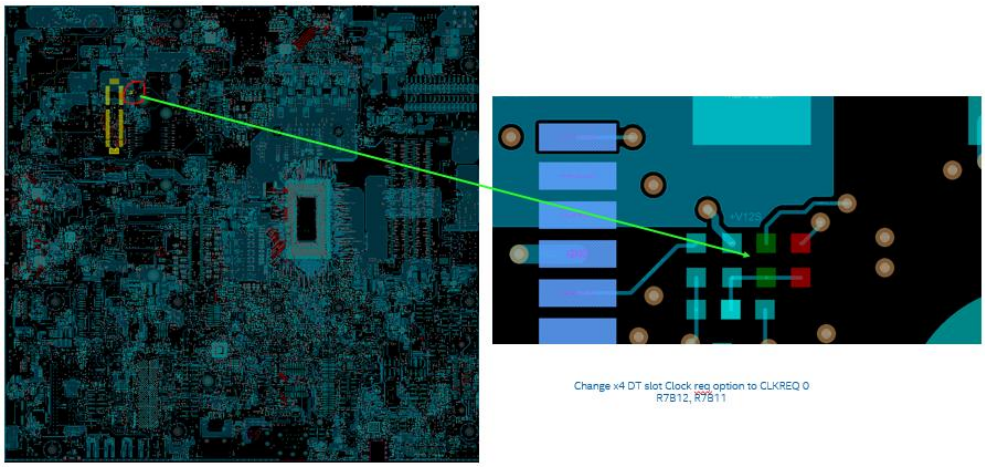




Change SRC Clock 0 connections to x4 DT slot
R6E58, R6E59, R6E63, R6E62

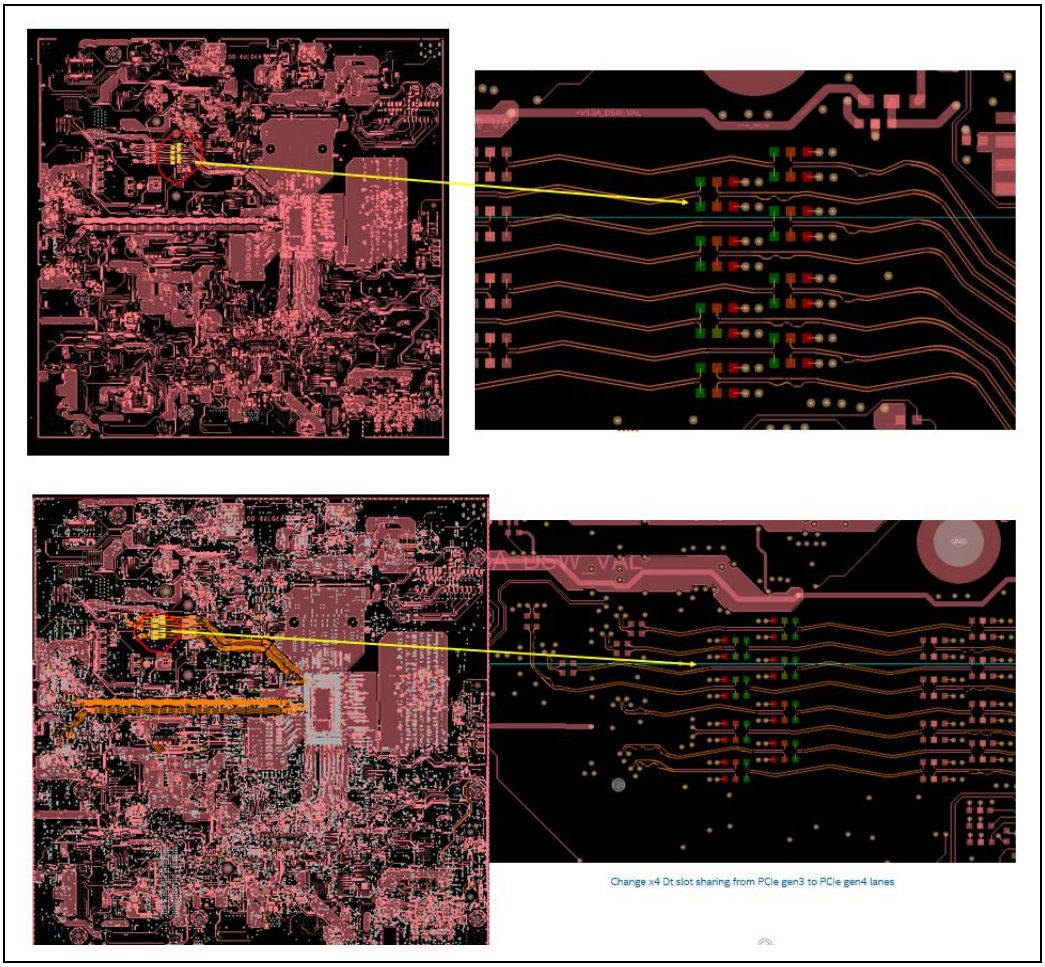


Change x4 DT slot Clock sharing options to PCIe Gen4 SRC CLK 0
R7C3, R7C4, R7U5, R7U6



Change x4 DT slot Clock req option to CLKREQ 0
R7B12, R7B11

Figure 3-54. Layout Snapshot (Bottom Layer)



3.2.12 Rework to Enable THC SPI Touch Panel Connection on TGL RVP

Description: There are two Touch panel connectors on TGL RVP. Both connectors have I^2C and THC SPI interfaces routed; but, I^2C path is stuffed by default. In order to enable the THC SPI path and validate the THC-based Touch Panels, the reworks should be done. The rework described here is needed for enabling the THC SPI path on both panels. Customers can enable the THC SPI path for either one or both Touch connectors.

Impact if done: After performing the reworks, I^2C based touch panels and THC SV header does not work as they share the same IOs (tripaded).

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

WO# Applicable for this Rework: IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101,

IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192501, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL191502, IPTL191701, IPTY190802, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY193902, IPTL201901, IPTY201701, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

3.2.12.1 Rework to Enable THC0 SPI Touch Panels Connection on TGL UP3 RVP

Table 3-27. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R4G48 R4G50 R4G52 R4G42 R4U42	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W	NA
Stuff	Resistor	R4U26 R4U36 R4G51 R4U20 R4G49	NA	RES D, 0402, 33.00 Ohm, 5.00%, 1/16 W
Stuff	Resistor	R5G26	NA	RES D, 0402, 100.00 kilo-ohm, 1.00%, 1/16 W

Figure 3-55. Schematic Snapshot

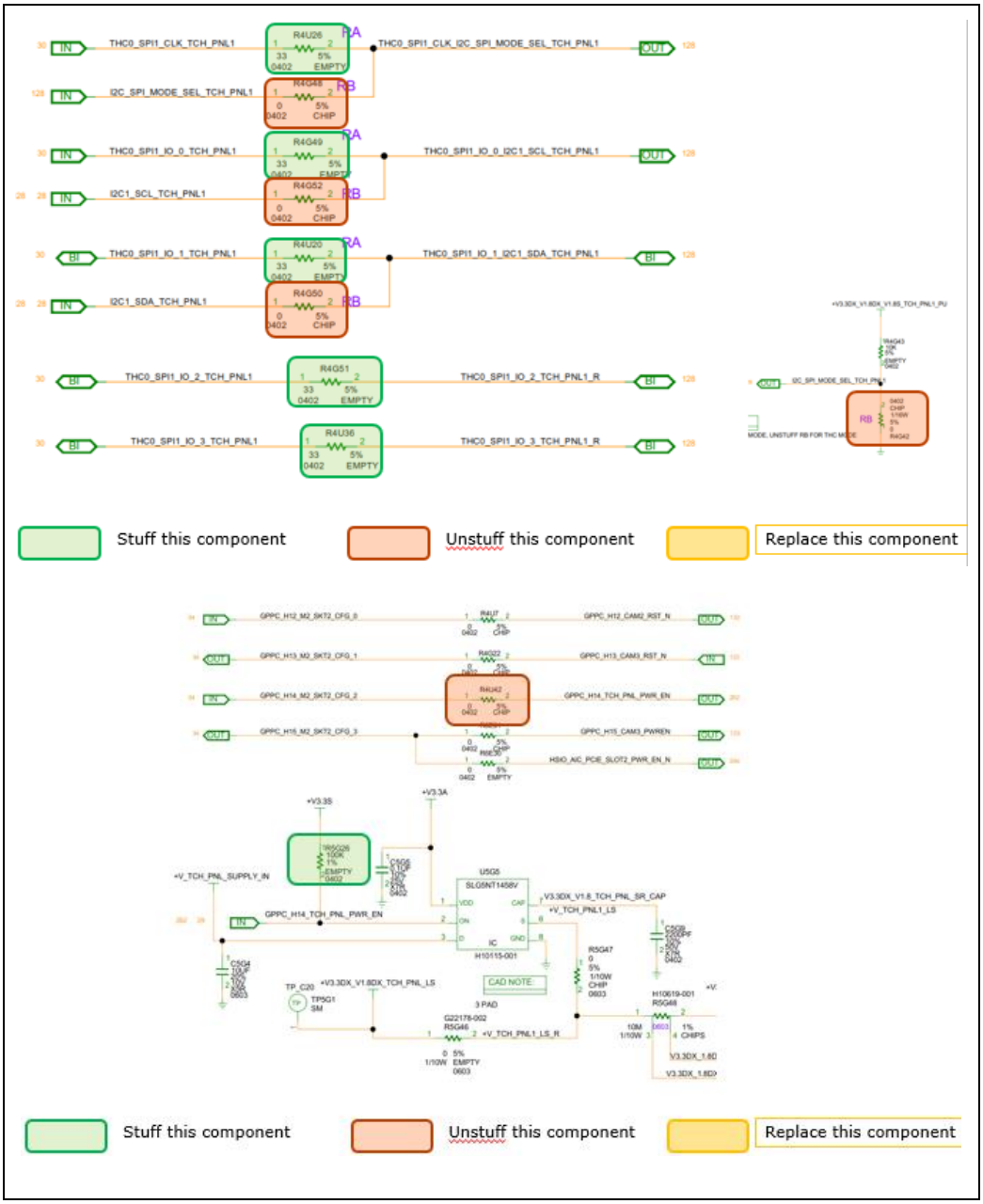


Figure 3-56. Layout Snapshot (Top Layer)

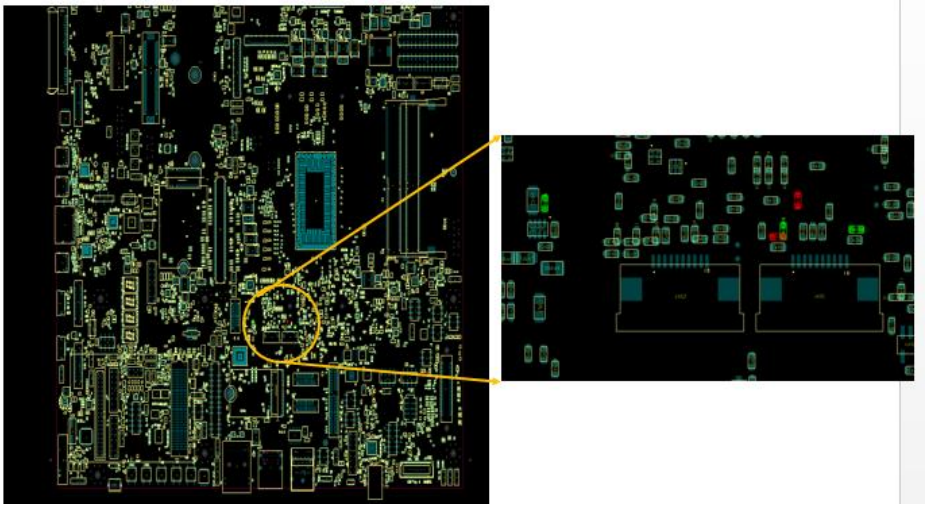
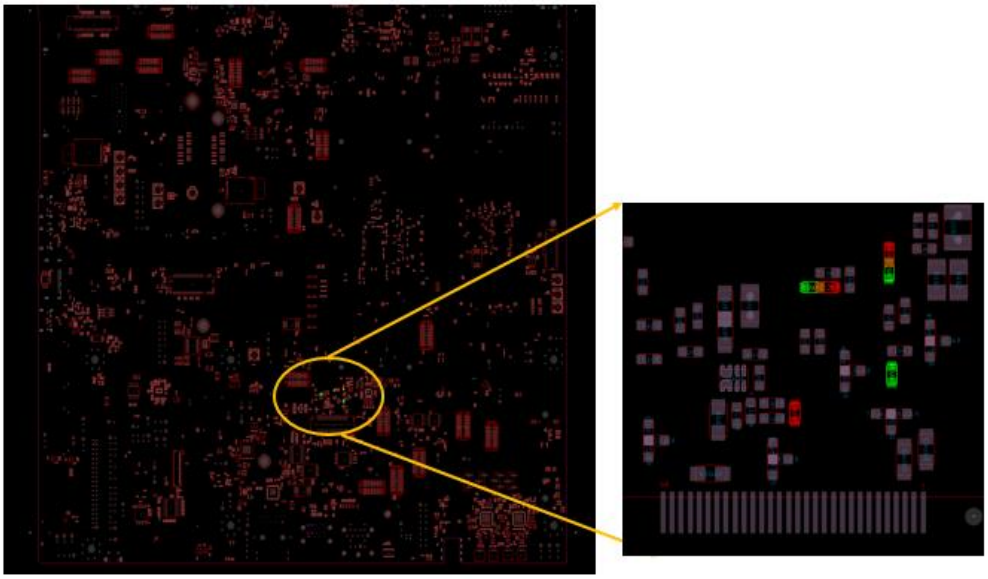


Figure 3-57. Layout Snapshot (Bottom Layer)

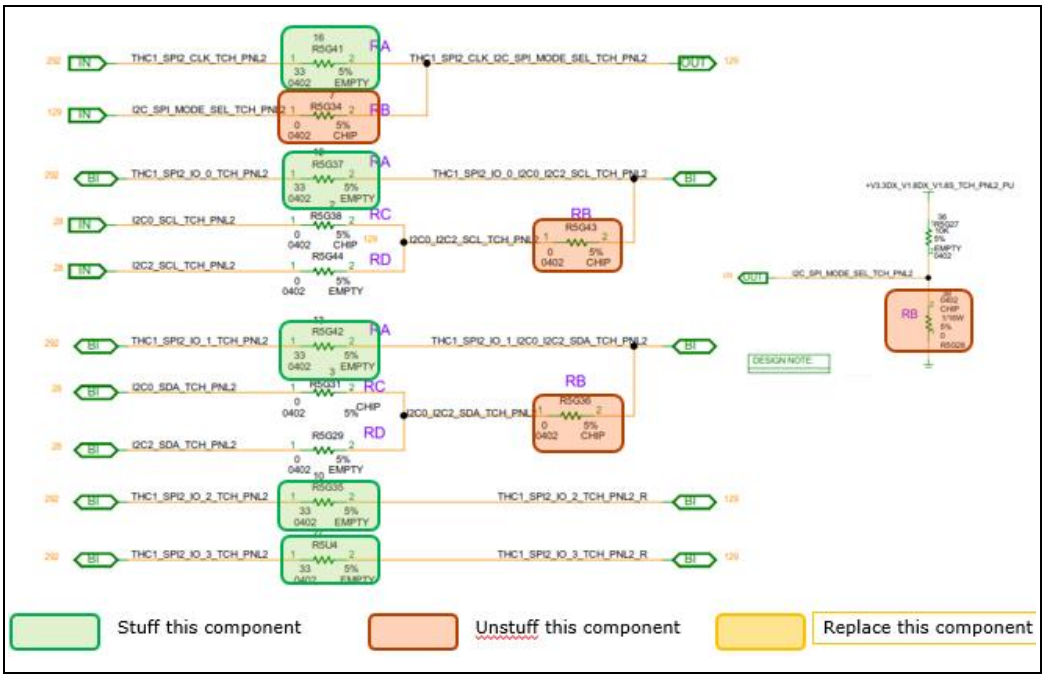


3.2.12.2 Rework to Enable THC1 SPI2 Interface on Second Touch Panel Connector

Table 3-28. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R5G34 R5G43 R5G36 R5G28 R4U42	RES D, 0402, 0.00 Ohm, 5.00%, 1/16 W	NA
Stuff	Resistor	R5G41 R5G37 R5G42 R5G35 R5U4	NA	RES D, 0402, 33.00 Ohm, 5.00%, 1/16 W
Stuff	Resistor	R5G26	NA	RES D, 0402, 100.00 kilo-ohm, 1.00%, 1/16 W

Figure 3-58. Schematic Snapshot



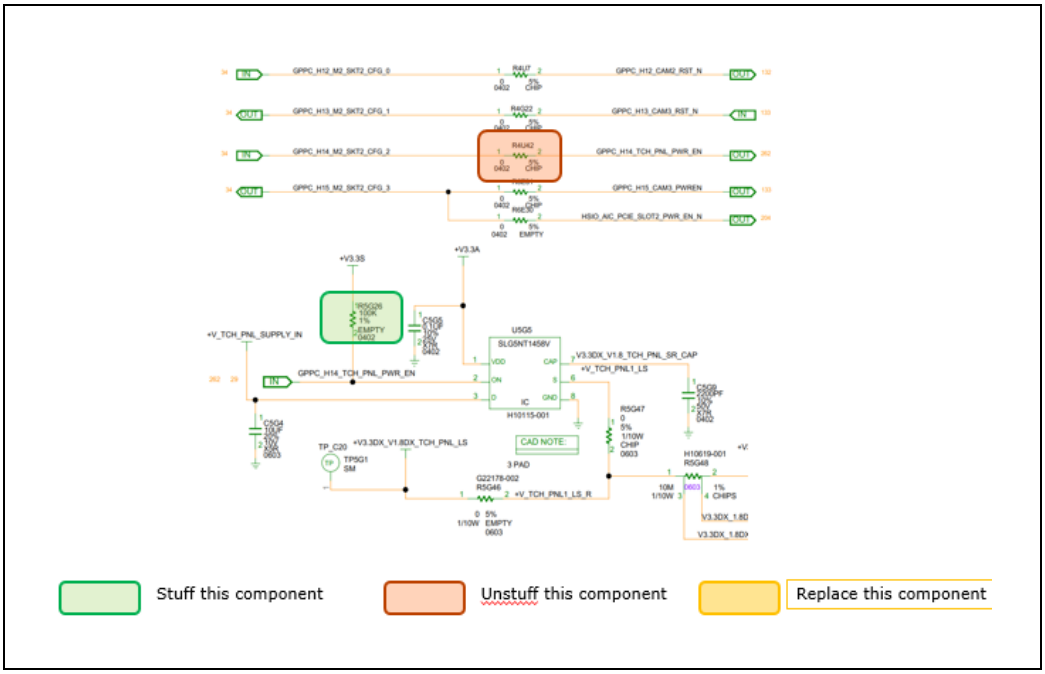


Figure 3-59. Layout Snapshot (Top Layer)

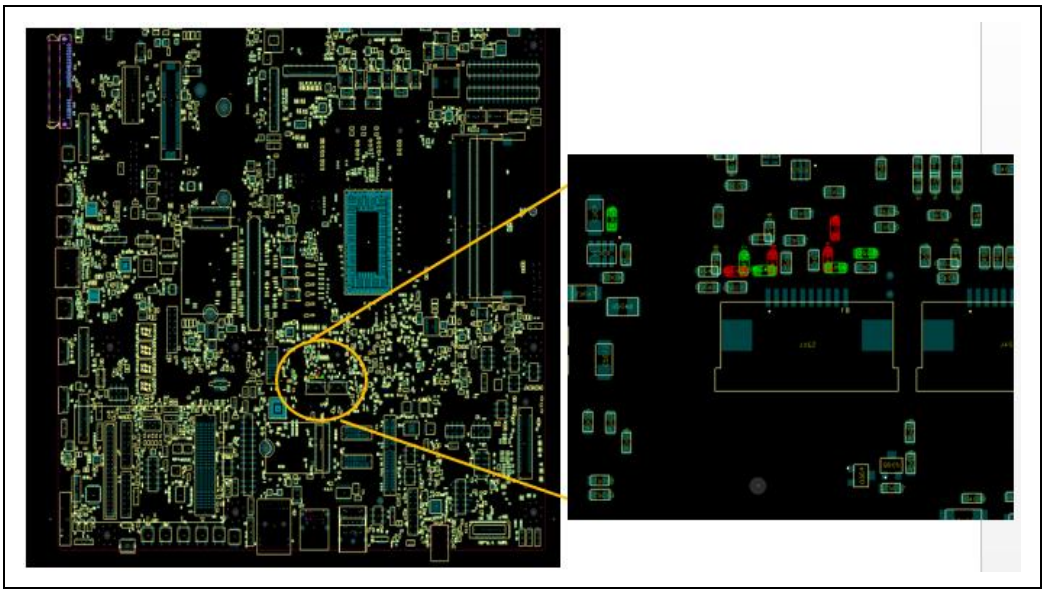


Figure 3-60. Layout Snapshot (Bottom Layer)

Action	TGL UP3 DDR4 SODIMM RVP	TGL UP3 LPDDR4x RVP
Unstuff	R4G48	R4G38
Unstuff	R4G50	R4U19
Unstuff	R4G52	R4G55
Unstuff	R4G42	R4G34
Unstuff	R4U42	R4U42
Stuff	R4U26	R4G48
Stuff	R4U36	R4U36
Stuff	R4G51	R4G54
Stuff	R4U20	R4U21
Stuff	R4G49	R4G53
Stuff	R5G26	R5G25
Unstuff	R5G34	R5G34
Unstuff	R5G43	R5G41
Unstuff	R5G36	R5G36
Unstuff	R5G28	R5G27
Unstuff	R4U42	R4U42
Stuff	R5G41	R5G39
Stuff	R5G37	R5G37
Stuff	R5G42	R5G40
Stuff	R5G35	R5G35
Stuff	R5U4	R5U4
Stuff	R5G26	R5G25

3.2.13 Rework to Enable HDA in ALC711 in TGL UP3 DDR4 Board

Description: Defining the path for codec to operate in HDA mode.

Impact if done: Implementing this rework enables HDA path for onboard ALC711. If not implemented, onboard ALC711 (codec) does not work in HD-A mode. SoundWire* mode is enabled by default. Will require BIOS/IFWI changes for HDA mode enabling

Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

WO# Applicable for this Rework: IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL191502, IPTL191701, IPTY190802, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTL201901, IPTY193902, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-29. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R3W17	100K, 1%, 1/16 W, 0402	NA
Stuff	Resistor	R3J19	NA	100K, 1%, 1/16 W, 0402
Stuff	Resistor	R2G3 R3F73 R3F59 R3J35	NA	33 Ohm, 1/16 W, 0402

Table 3-30. Reference Designator comparison table

Action	TGL UP3 DDR4	TGL UP3 LP4X	TGL UP3 LP5
Un stuff	R3W17	R3W17	R3W17
Stuff	R3J19, R2G3, R3F73, R3F59, R3J35	R3J19, R3G10, R3F72, R3F57, R3J34	R3J19, R3G9, R3F73, R3F59, R3J34

Figure 3-61. Schematic Snapshot

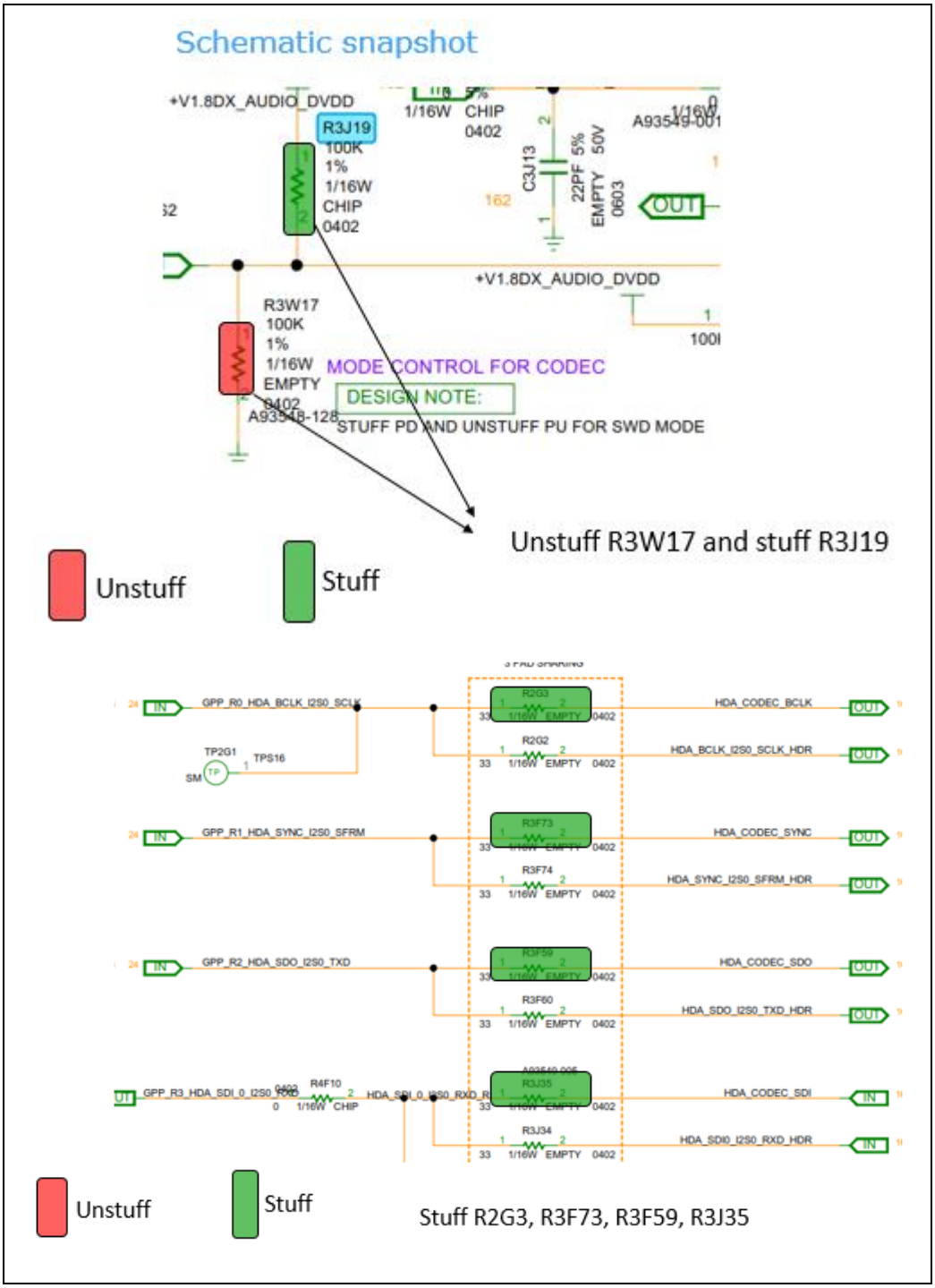


Figure 3-62. Layout Snapshot (Top Layer)

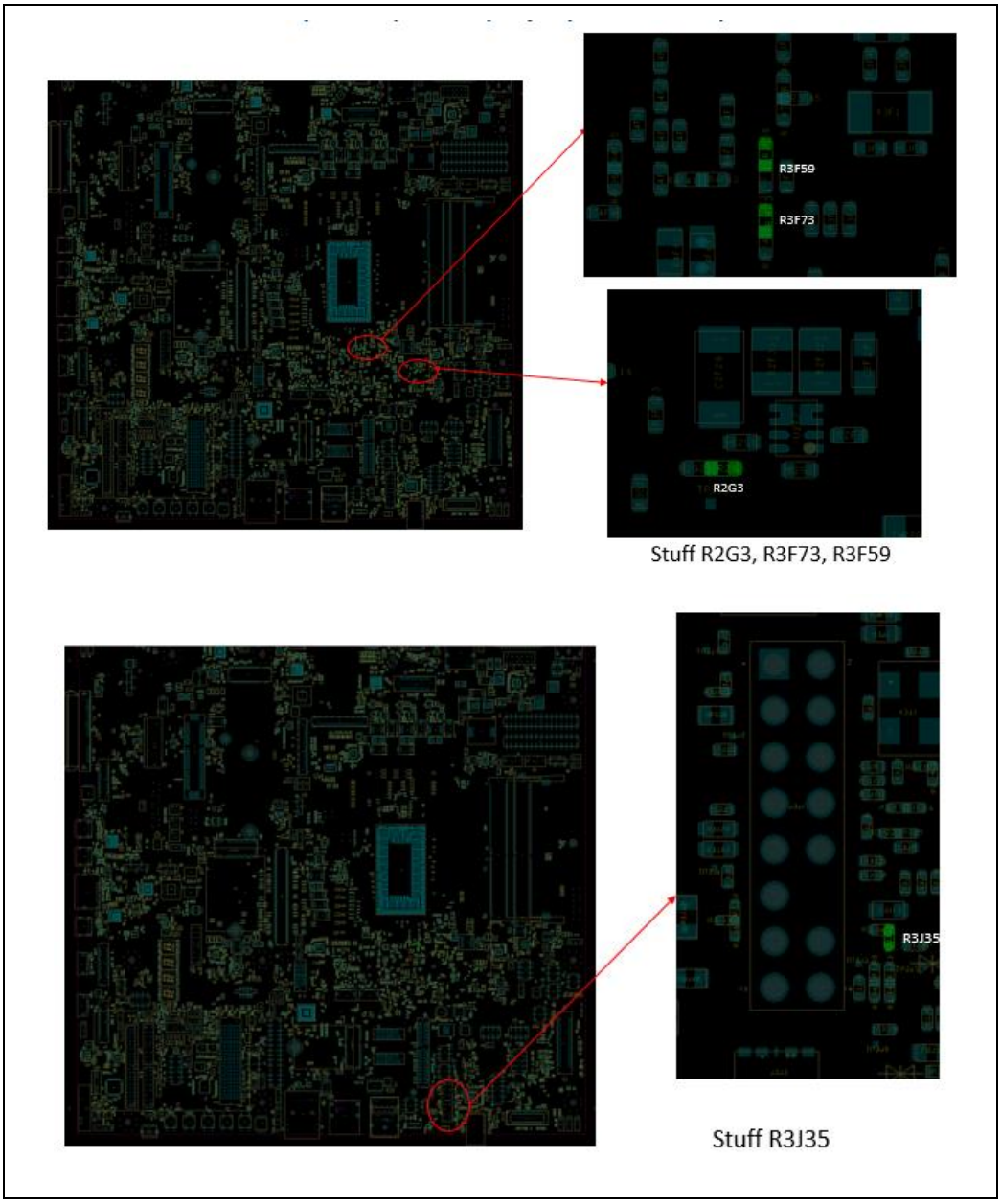
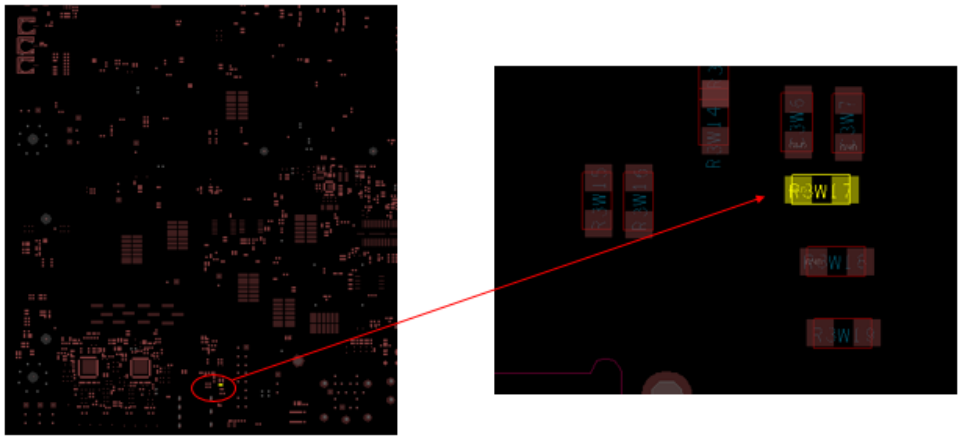


Figure 3-63. Layout Snapshot (Bottom Layer)



3.2.14 Rework to Enable HDMI with CRLS on TGL UP3 DDR4

Description: This rework is to enable vertical HDMI with CRLS on TGL UP3 DDR4.

Impact if not done: HDMI with ALS will not be functional.

Details: SMD Capacitor and Resistor rework.

Applicable To: TGL UP3 DDR4 RVP.

WO# Applicable for this Rework: IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194702, IPTL201201, IPTY201701, IPTL194202, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

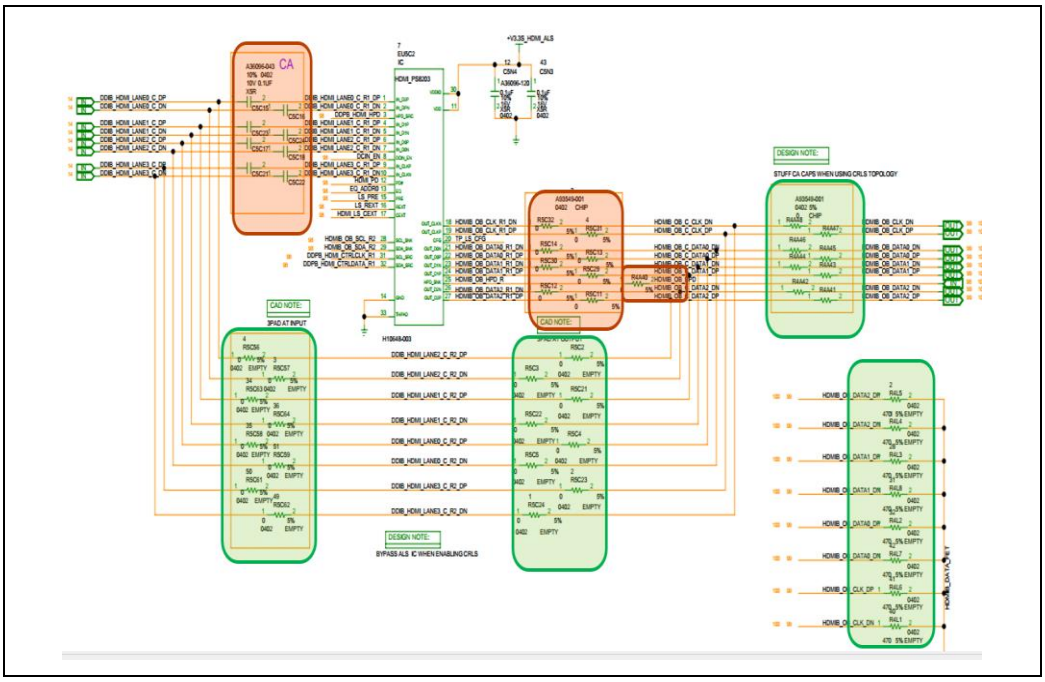
Table 3-31. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Capacitor	C5C15 C5C16 C5C23 C5C24 C5C17 C5C18 C5C21 C5C22	0.1uF, 10 V, 0402	NA

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R5C56 R5C57 R5C63 R5C64 R5C58 R5C59 R5C61 R5C62 R5C2 R5C3 R5C21 R5C22, R5C4 R5C5 R5C23 R5C24	NA	0 Ohm, 0402
Replace	Resistor	R4A48 R4A47 R4A46 R4A45 R4A44 R4A43 R4A42 R4A41	0 Ohm, 0402	0.1uF, 10 V, 0402
Stuff	Resistor	R4L5 R4L4 R4L3 R4L8 R4L2 R4L7 R4L6 R4L1	NA	470 Ohm, 5% 0402
Unstuff	Resistor	R5C47 R5C51 R5N21 R4A40 R5N25 R5N19	0 Ohm, 0402	0 Ohm, 5%, 0402

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R5C48 R5C52 R5N22 R5N20 R5C55	NA	0 Ohm, 5%, 0402
Stuff	Resistor	R5C60	NA	1M Ohm, 5%, 0402
Unstuff	Resistor	R5C32 R5C14 R5C30 R5C12 R5C13 R5C31 R5C29 R5C11	0 Ohm, 5% 0402	NA
Stuff	Resistor	R4A36	NA	20k Ohm, 0402

Figure 3-64. Schematic Snapshot



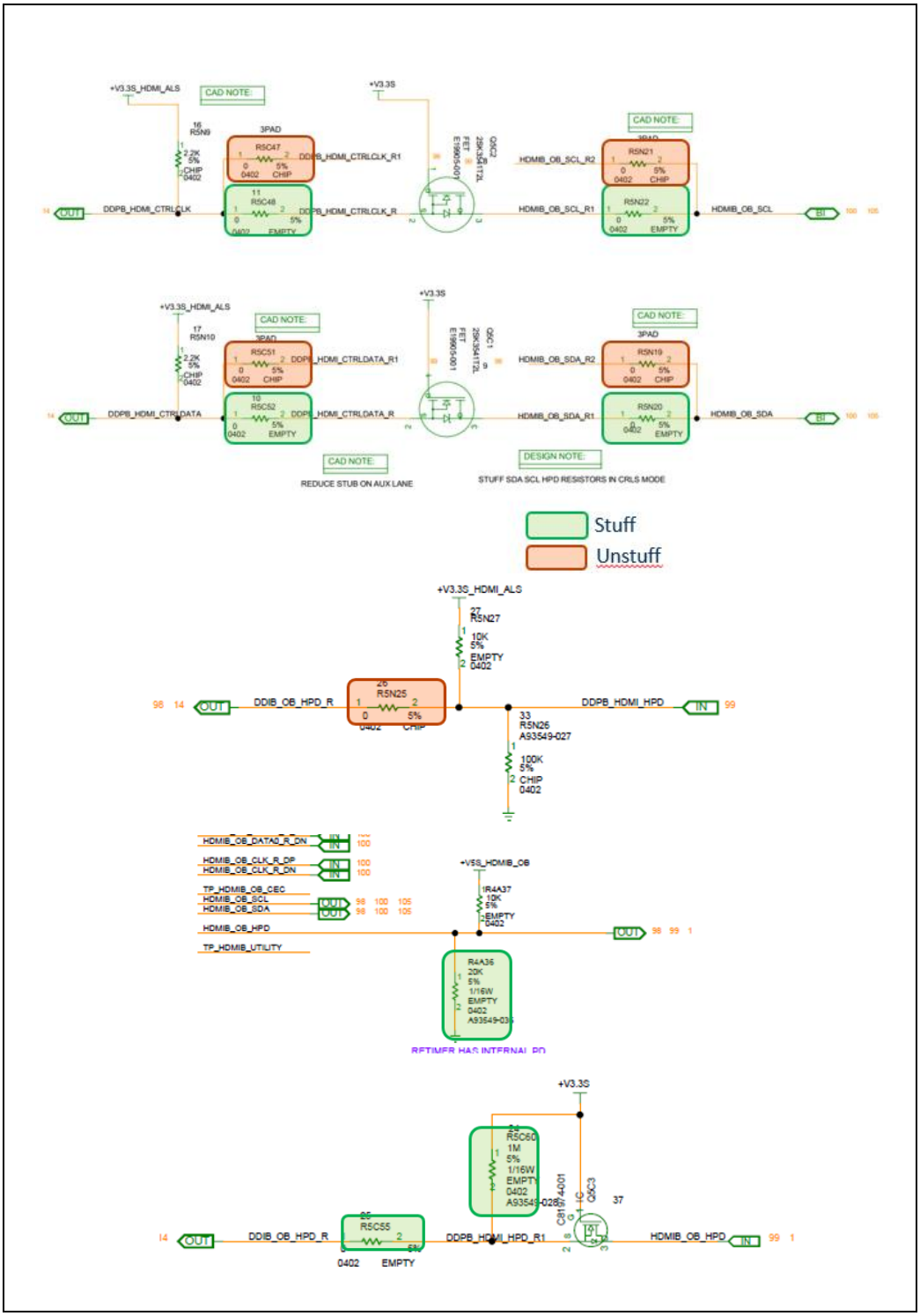

+V3.3S_HDMI_ALS
CAD NOTE:
+V3.3S
16
R5N9
2.2K
5%
CHIP
0402
3PAD
R5C47
DDPB_HDMI_CTRLCLK_R1
11
R5C48
DDPB_HDMI_CTRLCLK_R
OUT
DDPB_HDMI_CTRLCLK
Q5C2
29K3541T2L
FET
E19905-001
HDMIB_OB_SCL_R2
R5N21
HDMIB_OB_SCL_R1
R5N22
HDMIB_OB_SCL
BI
17
R5N10
R5C51
DDPB_HDMI_CTRLDATA_R1
10
R5C52
DDPB_HDMI_CTRLDATA_R
DDPB_HDMI_CTRLDATA
Q5C1
HDMIB_OB_SDA_R2
R5N19
HDMIB_OB_SDA_R1
R5N20
HDMIB_OB_SDA
EMPTY
REDUCE STUB ON AUX LANE
DESIGN NOTE:
STUFF SDA SCL HPD RESISTORS IN CRLS MODE
Stuff
Unstuff
27
R5N27
10K
EMPTY
0402
26
R5N25
DDIB_OB_HPD_R
DDPB_HDMI_HPD
IN
33
R5N26
AS3549-027
100K
CHIP
HDMIB_OB_DATA0_R_DN
HDMIB_OB_CLK_R_DP
HDMIB_OB_CLK_R_DN
TP_HDMIB_OB_CEC
HDMIB_OB_SCL
HDMIB_OB_SDA
HDMIB_OB_HPD
TP_HDMIB_UTILITY
+VSS_HDMIB_OB
1R4A37
R4A36
20K
1/16W
AS3549-036
RETIMER HAS INTERNAL PD
24
R5C60
1M
AS3549-028
Q5C3
37
25
R5C55
DDPB_HDMI_HPD_R1

Figure 3-65. Layout Snapshot (Top Layer)

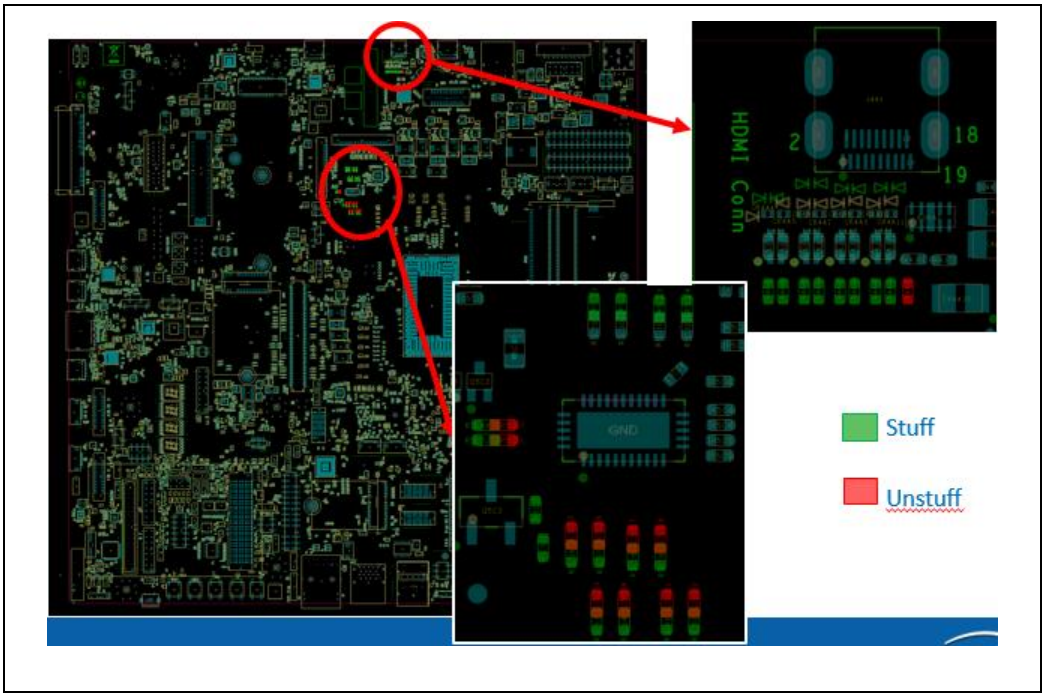
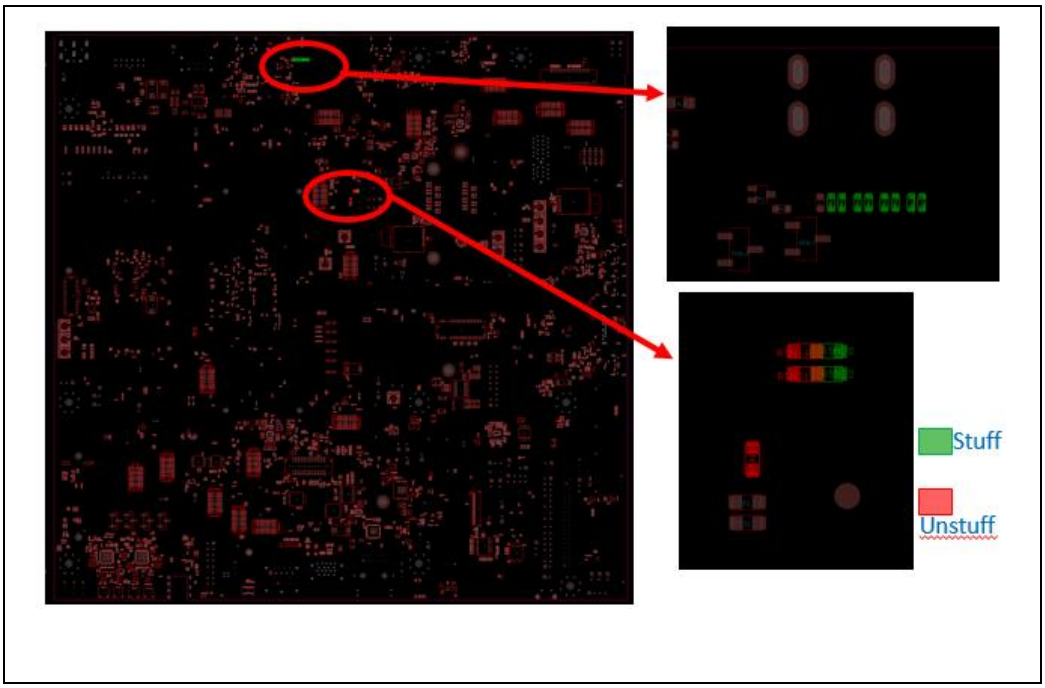


Figure 3-66. Layout Snapshot (Bottom Layer)



3.2.15 Rework for HDMI (with Retimer) on TCP0 Port

Description: This rework is to enable the HDMI port on TCP0 Port.

Impact if done: Type C port J6A1 is not functional for TBT™/USB3/DP functionality.

Details: SMD Capacitor and Resistor rework

Applicable To: TGL UP3 LP4x RVP

WO# Applicable for this Rework: IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL191502, IPTL201901, IPTL191701, IPTL203003.

Table 3-32. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Capacitor	C6A29 C6A17 C6A15 C6A26 C6A24 C6A22 C6A21 C6A19	NA	Cap,0402, 0.1UF
Stuff	Resistor	R5A39 R5A38 R5L12 R5L9	NA	Res, 0402, 0 Ohm
Unstuff	Capacitor	C6A28 C6A27 C6A14 C6A16 C6A25 C6A23 C6A20 C6A18	CAPC, X5R, 0402, 0.220UF, 10 V	NA
Unstuff	Resistor	R5A40 R5A37 R5L11 R5L10 R5A35	Res, 0402, 0 Ohm	NA

Figure 3-67. Schematic Snapshot

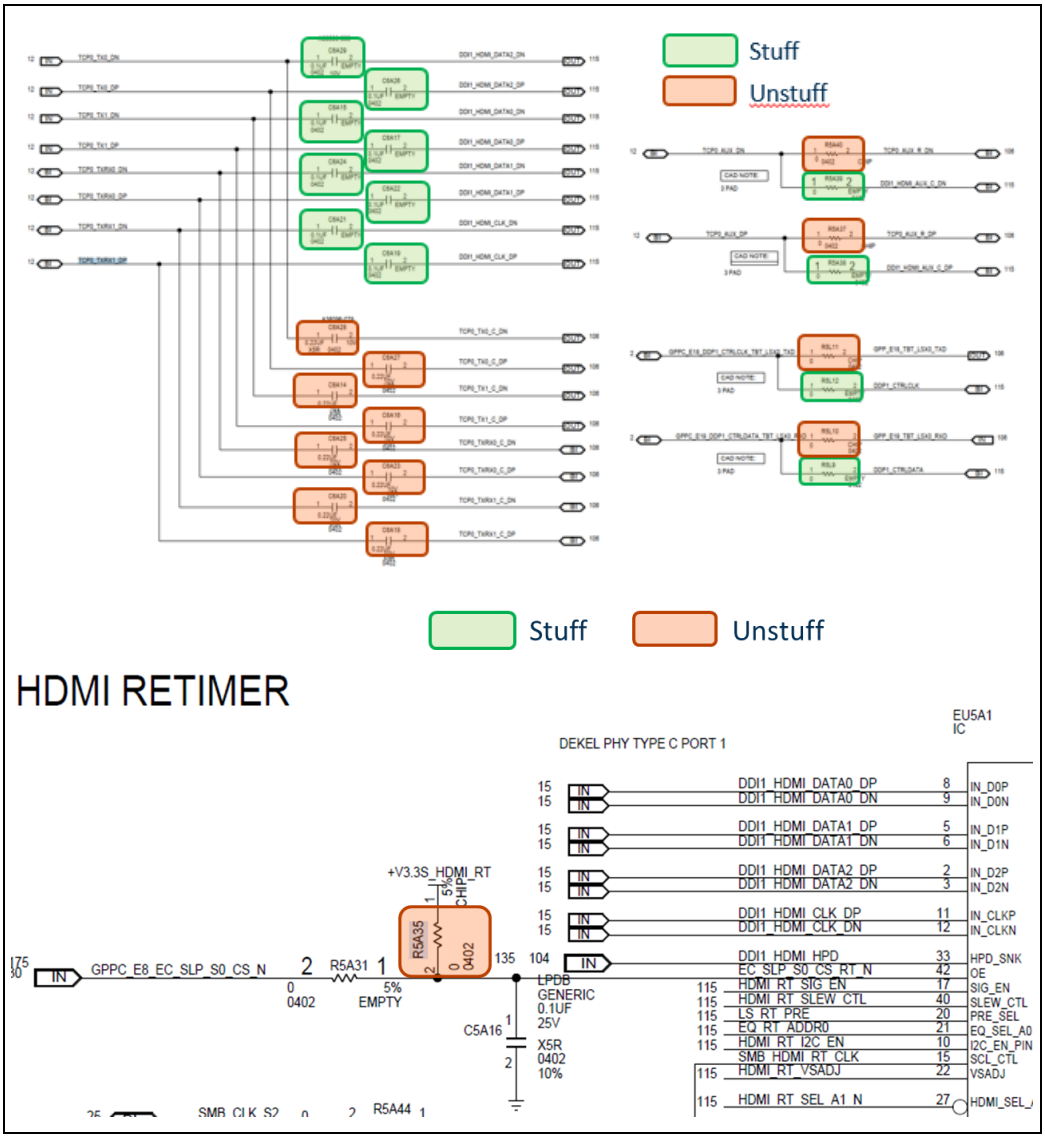


Figure 3-68. Layout Snapshot (Top Layer)

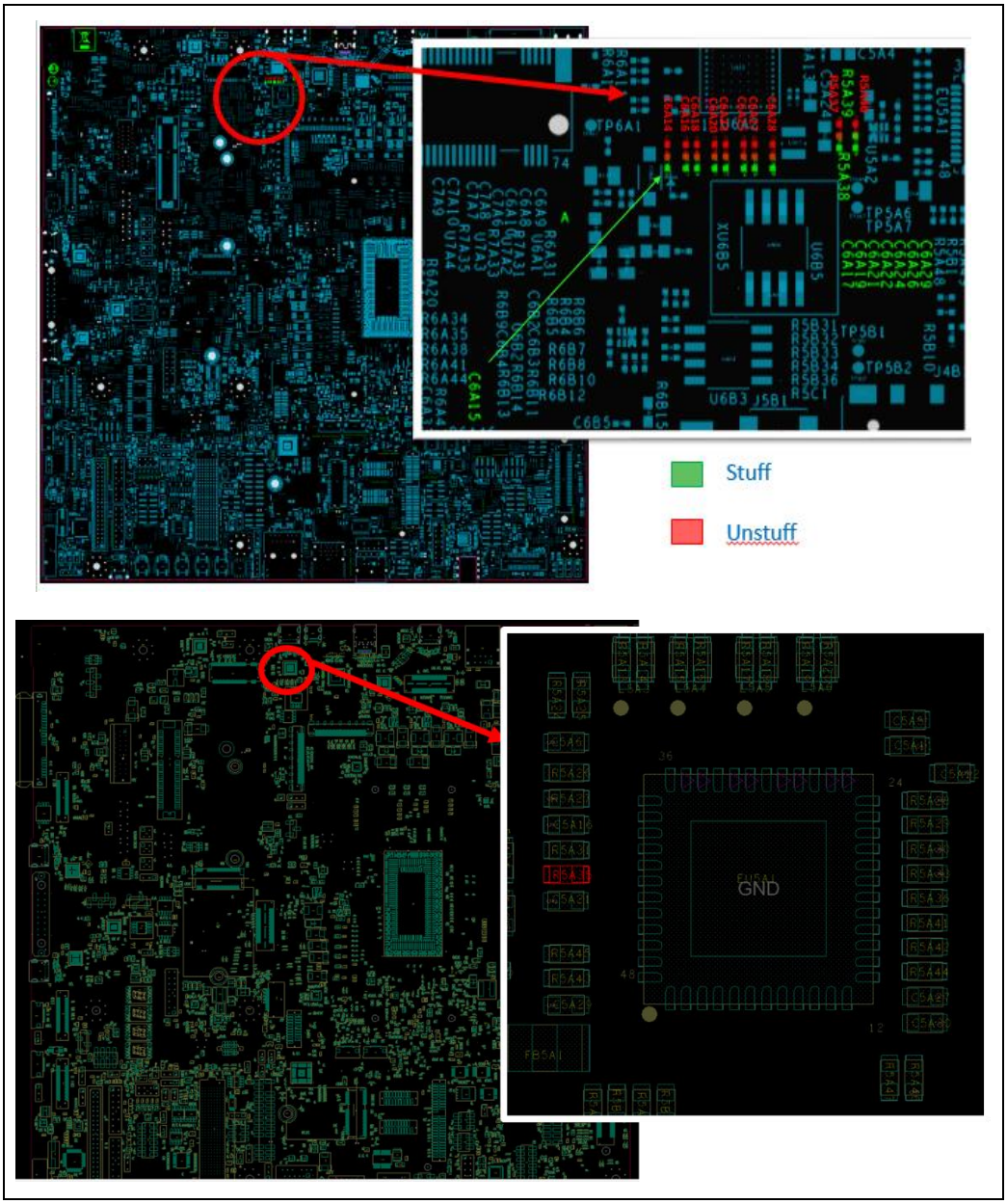
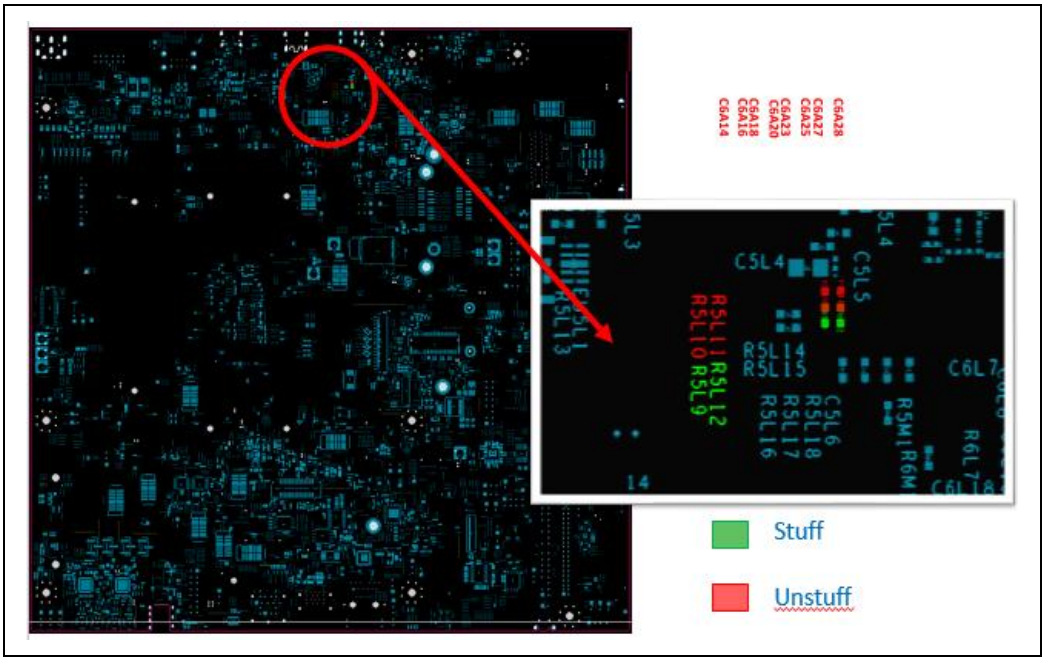


Figure 3-69. Layout Snapshot (Bottom Layer)



Extra information:

The Soft strap and VBIOS change required to configure the Dekel Phy TCP0 port as HDMI.

3.2.16 Rework to Enable HDMI (Vertical) with CRLS on TCP3 Port

Description: This rework is to enable vertical HDMI port on TCP3 port.

Impact if done: Type C port J9F1 is not functional for USB3/DP/TBT™.

Details: SMD Capacitor and Resistor rework

Applicable To: TGL UP3 LP4x RVP

WO# Applicable for this Rework: IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL191502, IPTL201901, IPTL191701, IPTL203001, IPTL203002, IPTL203003.

Table 3-33. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Capacitor	C6F1 C6F2 C6F5 C6F6 C6F3 C6F4 C6F11 C6F10	NA	Cap, 0402, 0.1UF
Stuff	Resistor	R6R11 R6R8 R6R18 R6R19 R6R15 R6R12 R6R20 R6R21 R4G18 R4F44	NA	Res, 0402, 0 Ohm
Unstuff	Capacitor	C6R6 C6R4 C6R11 C6R12 C6R9 C6R8 C6R15 C6R16	CAPC, X5R, 0402, 0.220UF, 10 V	NA
Unstuff	Resistor	R4G19 R4F45	Res, 0402, 0 Ohm	NA

Figure 3-70. Schematic Snapshot

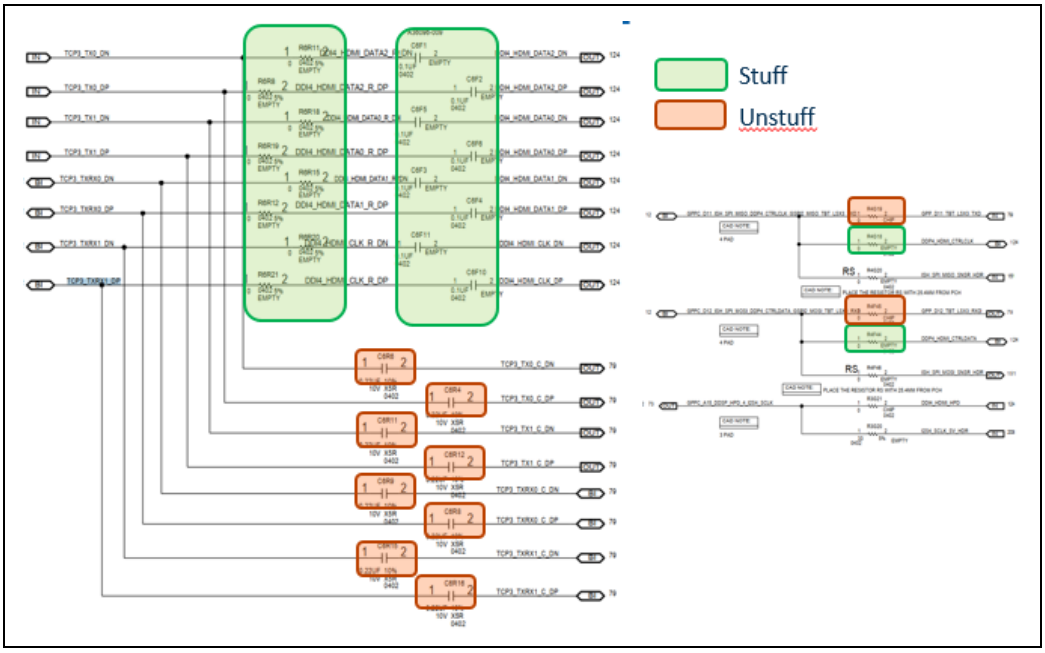


Figure 3-71. Layout Snapshot (Top Layer)

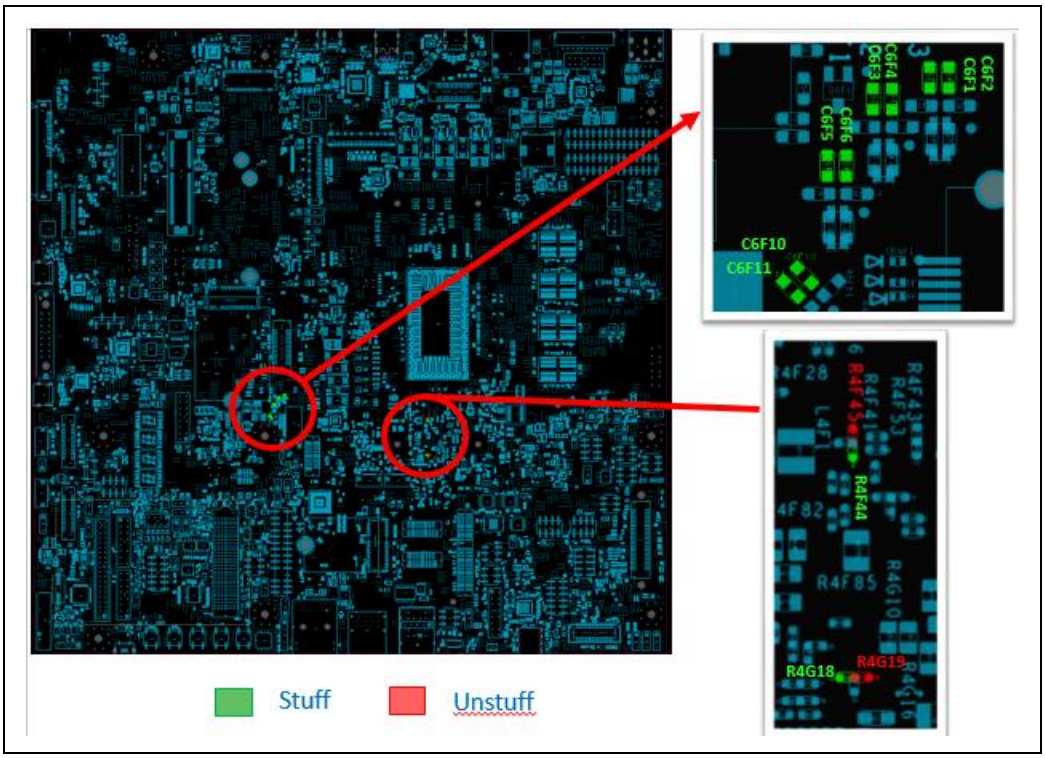
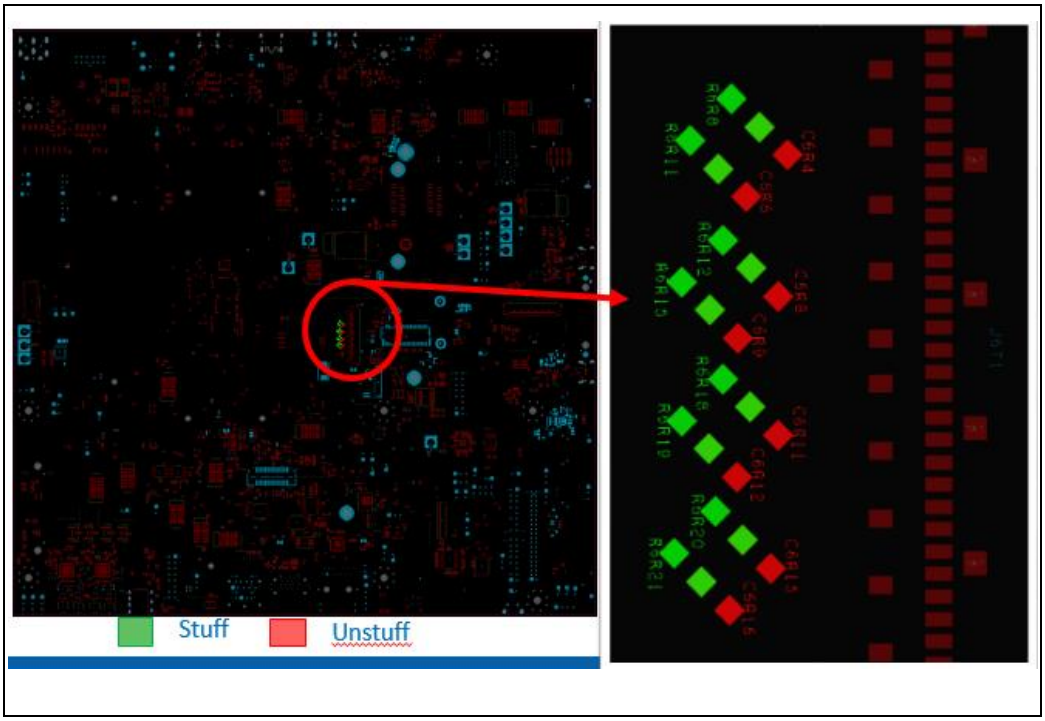


Figure 3-72. Layout Snapshot (Bottom Layer)



3.2.17 Rework to Enable ALC1013 (AMP)

Description: Defining the path for ALC1013.

Impact if done: Implementing this rework enables SoundWire* path for ALC1013 (AMP). Onboard AMP – ALC1308 is disabled by not implementing; ALC1308 (AMP) is enabled by default.

Details: SMD Resistor rework

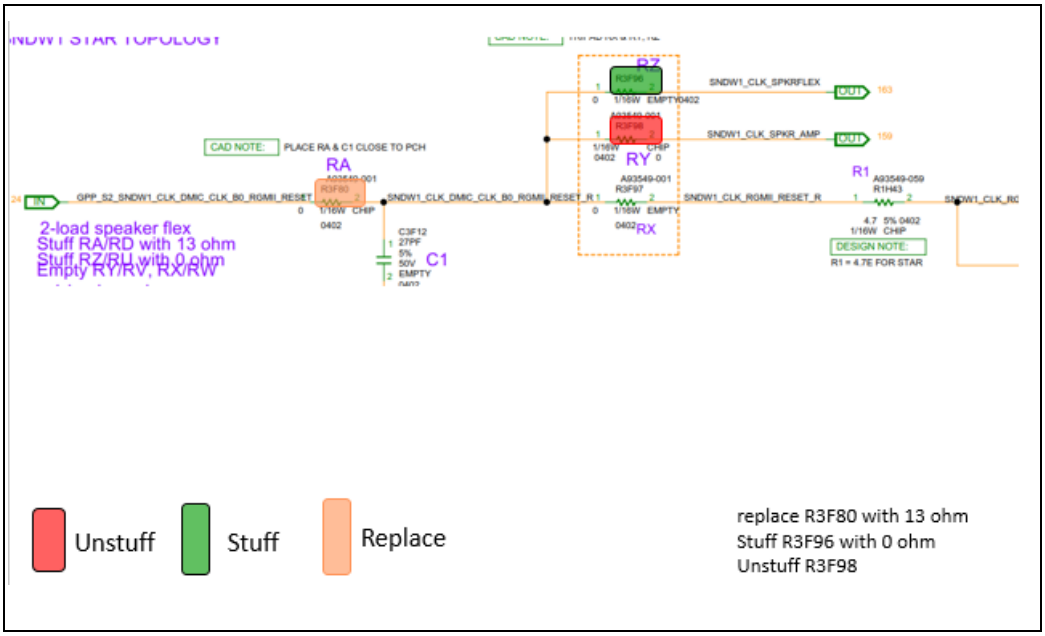
Applicable To: TGL UP3 DDR4 RVP and TGL UP3 LPDDR4x RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001 IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402 IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL191502, IPTL191701, IPTY190802, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTL201901, IPTY193902, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-34. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R3F80 R3G14	0 Ohm, 5%, 1/16 W, 0402	13 Ohm, 5%, 1/16 W, 0402
Stuff	Resistor	R3F96 R3G6	0 Ohm, 5%, 1/16 W, 0402	NA
Unstuff	Resistor	R3F98 R3G5	0 Ohm, 5%, 1/16 W, 0402	NA

Figure 3-73. Schematic Snapshot



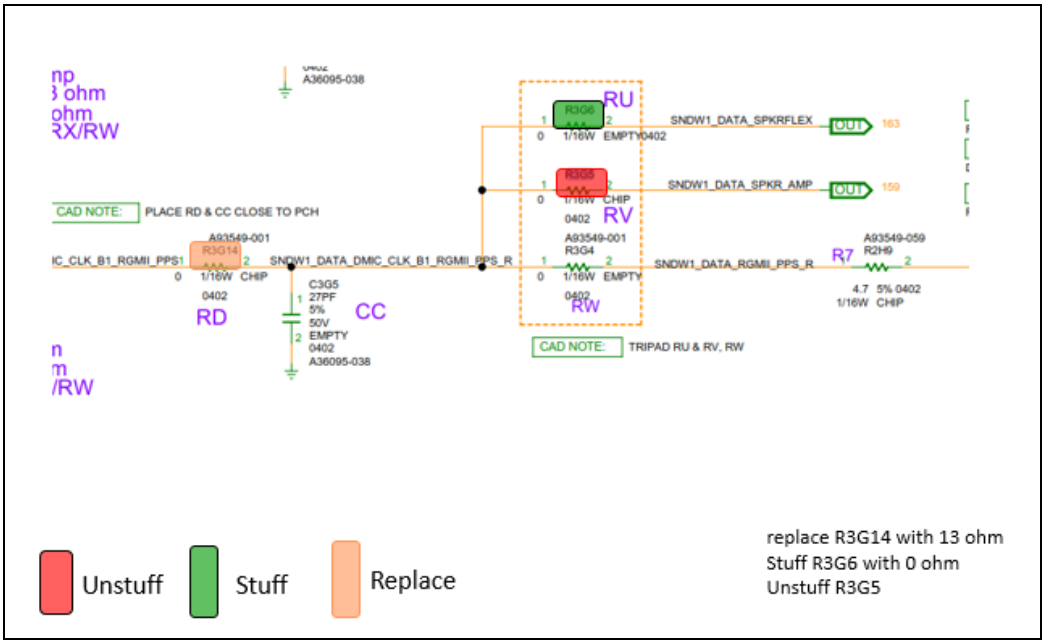
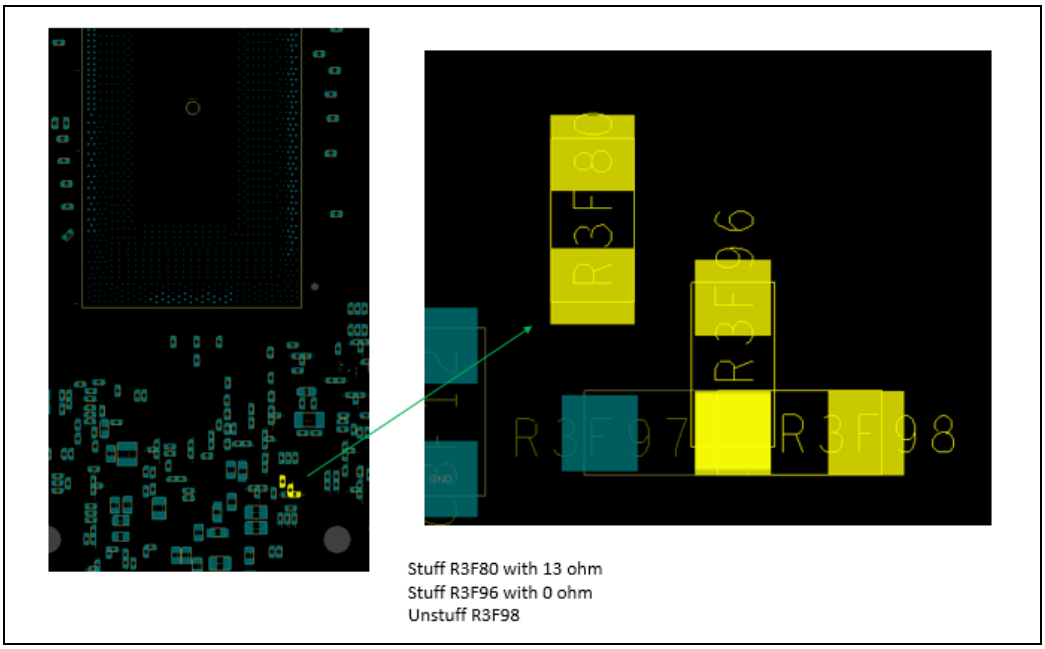
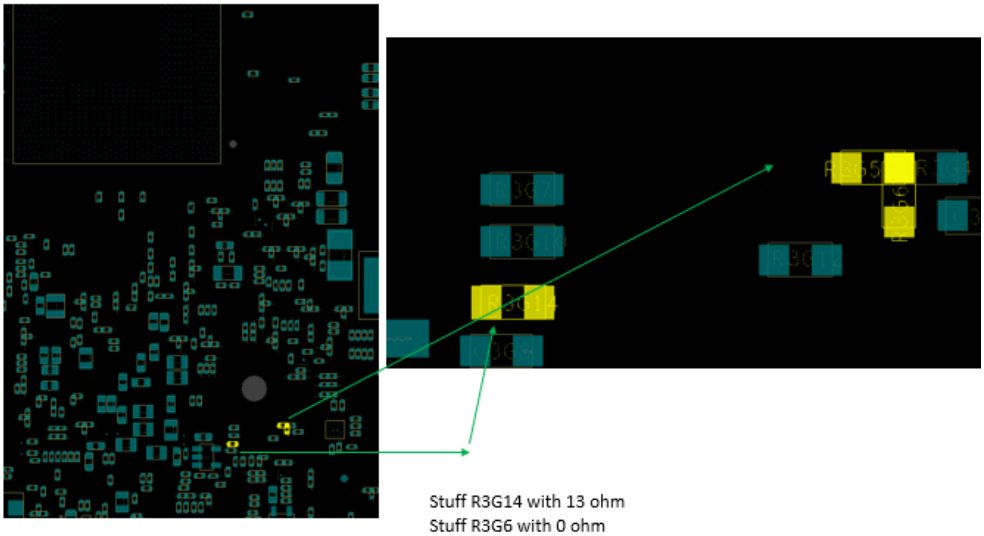


Figure 3-74. Layout Snapshot (Top Layer)





3.2.18 Rework to Get Correct PWM Frequency and Output from ALC1308 (Amplifier)

Description: Enabling to get right PWM frequency and thereby get output from amplifier (ALC1308).

Impact if done: By implementing this rework, right PWM frequency from ALC1308 is obtained. ALC1308 does not give output if not implemented.

Details: Blue wiring

Applicable To: TGL UP3 DDR4 RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTY190802, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY201701 and IPTY191903.

Table 3-35. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Blue wire	Solder wire	U2W1.4 to U2W1.5 U1W1.4 to U1W1.5	NA	NA

Figure 3-75. Schematic Snapshot

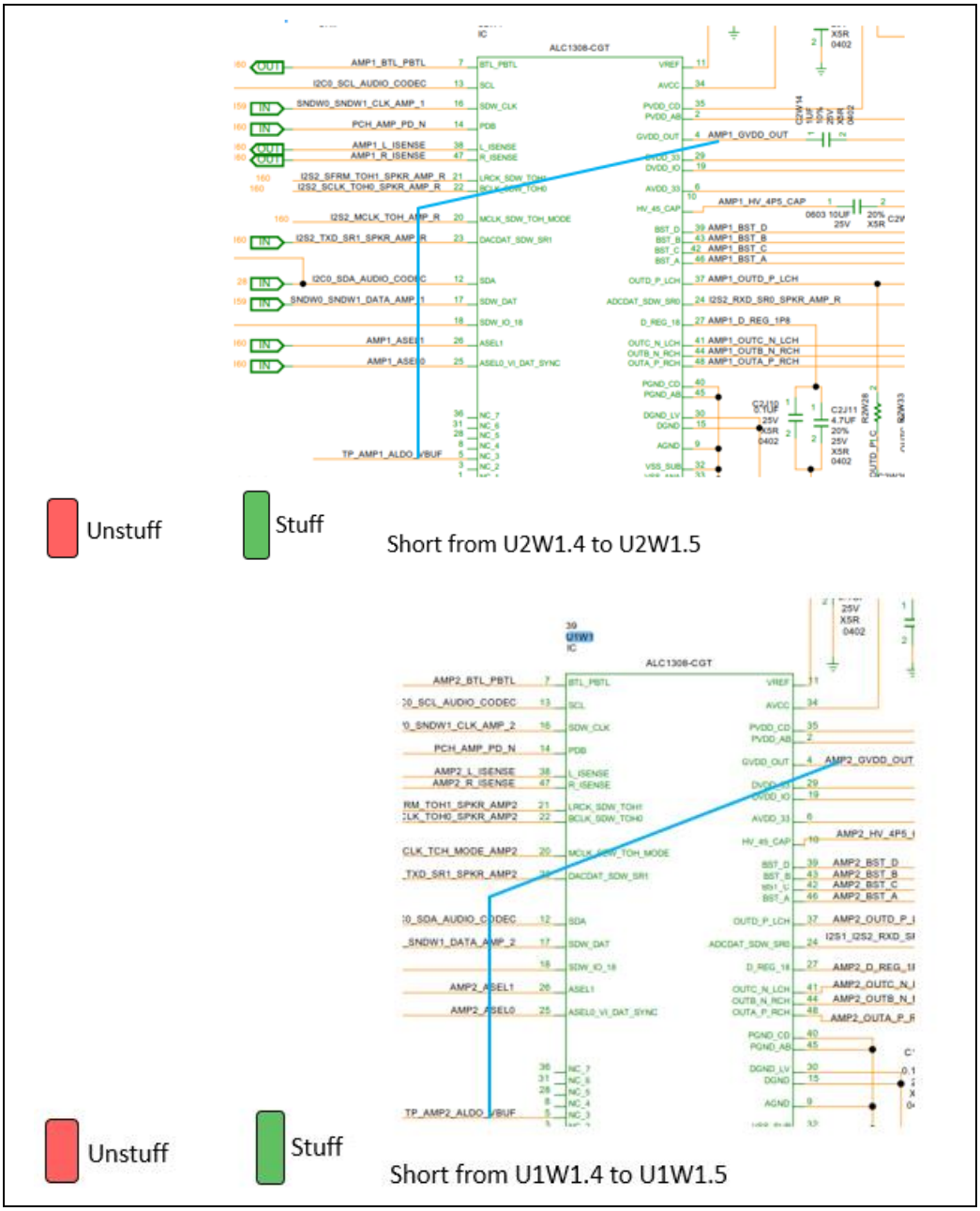
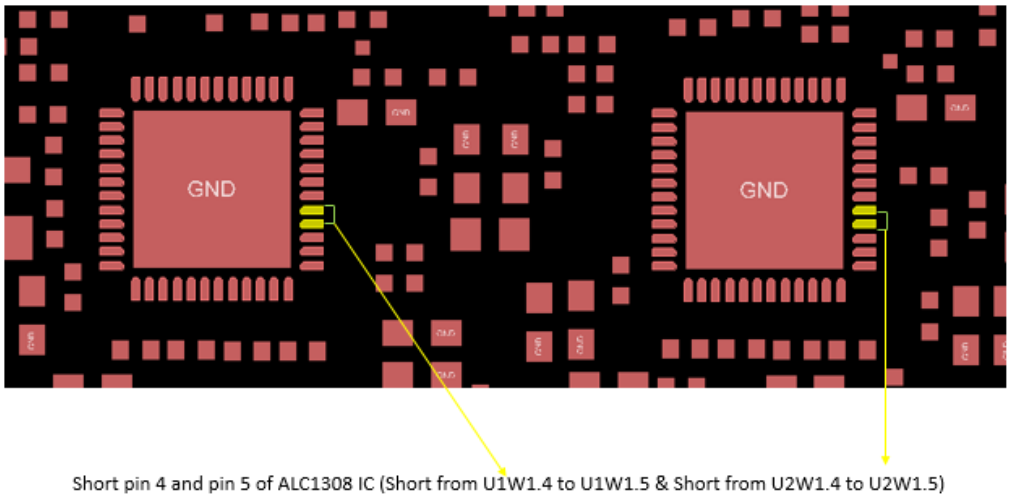


Figure 3-76. Layout Snapshot (Bottom Layer)



Short pin 4 and pin 5 of ALC1308 IC (Short from U1W1.4 to U1W1.5 & Short from U2W1.4 to U2W1.5)

– This rework is suggested since there was a mistake in datasheet regarding the supply. This connection is required in order to get 500Khz PWM frequency and AMP output

3.2.19 Rework to Enable eDP on DDIB Combo Port

Description: This rework is to enable the second eDP on DDIB port.

Impact if done: By implementing this rework, HDMI connector J4A1 does not work.

Details: SMD Capacitor rework

Applicable To: TGL UP3 DDR4 RVP

WO# Applicable for this Rework: IPTY191801, ITPY191802, IPTY191901, IPTY191902, ITPY191903, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTY193902, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

Table 3-36. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Capacitor	C5B6 C5B5 C5B8 C5B7 C5B10 C5B9 C5B12 C5B11 C5B14 C5B15	NA	Cap, 0402, 0.1UF
Stuff	Resistor	R5G39	NA	Res, 0402, 0 Ohm
Stuff	Resistor	R7W23 R7W11	NA	Res, 0402, 10K ohms
Unstuff	Resistor	R5B21 R5B20 R5B23 R5B22 R5B25 R5B24 R5B27 R5B26 R5G40	Res, 0402, 0 Ohm	NA
Unstuff	Resistor	R7W19 R7W9	Res, 0402, 10K ohms	NA

Table 3-37. Reference Designator Comparison

TGL UP3 DDR4	TGL UP3 LP4x
C5B6	C5B6
C5B5	C5B5
C5B8	C5B8
C5B7	C5B7
C5B10	C5B10
C5B9	C5B9

TGL UP3 DDR4	TGL UP3 LP4x
C5B12	C5B12
C5B11	C5B11
C5B14	C5B14
C5B15	C5B16
R7W23	R7W23
R7W19	R7W19
R7W11	R7W11
R7W9	R7W9
R5B21	R5B24
R5B20	R5B23
R5B23	R5B26
R5B22	R5B25
R5B25	R5B28
R5B24	R5B27
R5B27	R5B30
R5B26	R5B29
R5G40	R3U23
R5G39	R3U24

Figure 3-77. Schematic Snapshot

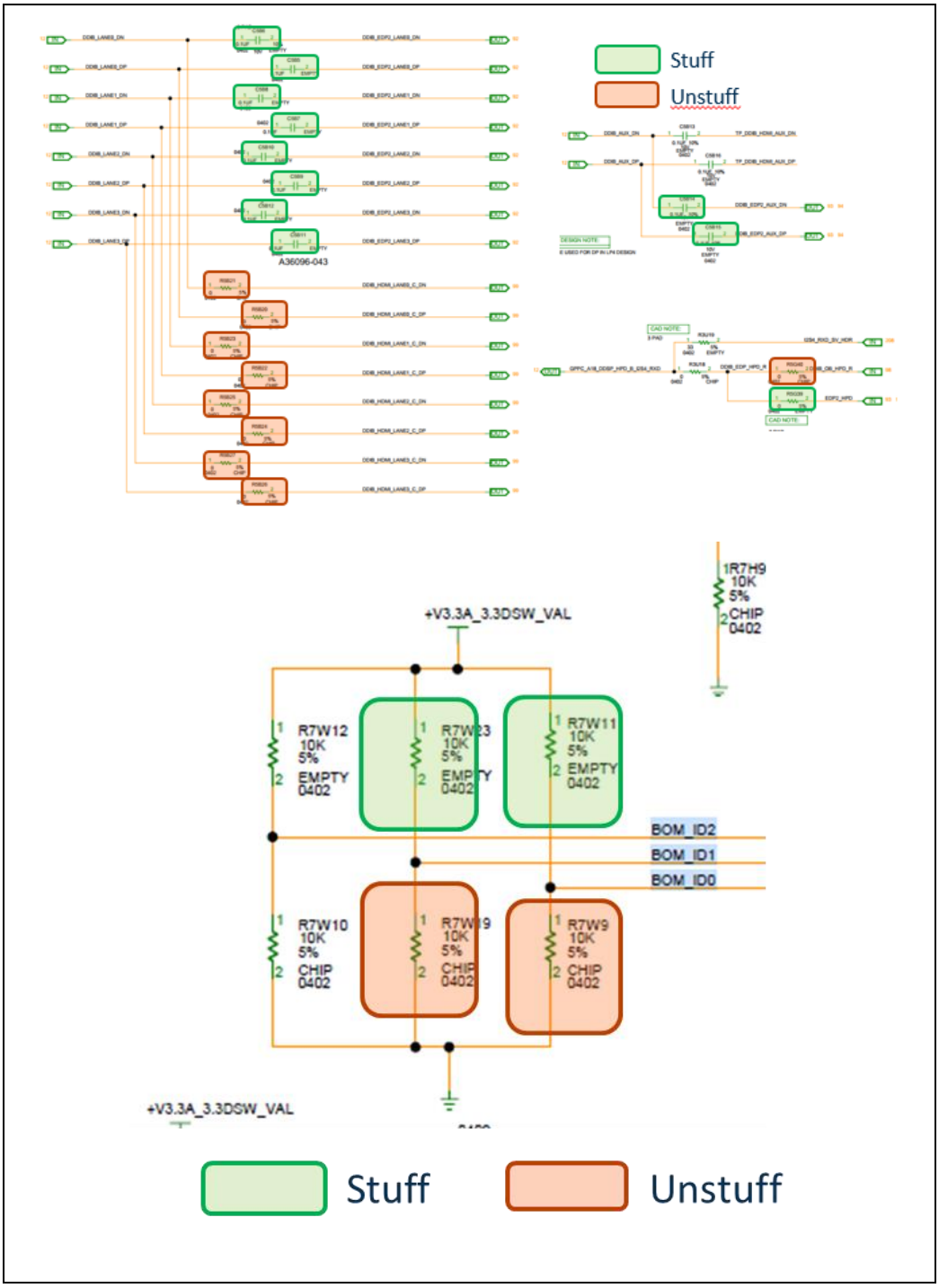


Figure 3-78. Layout Snapshot (Top Layer)

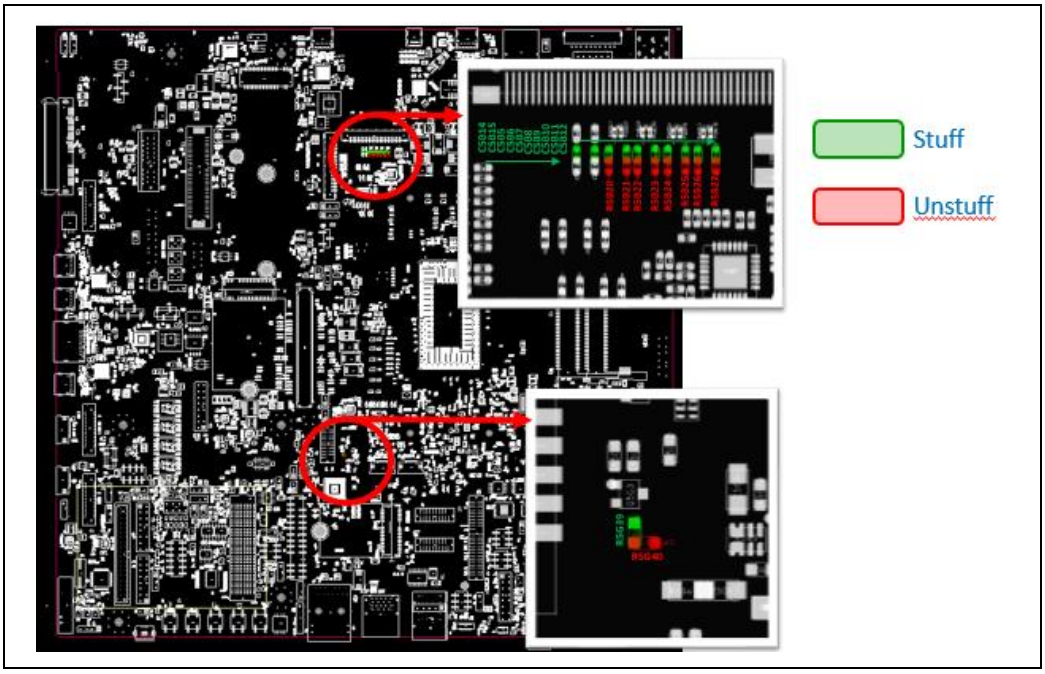
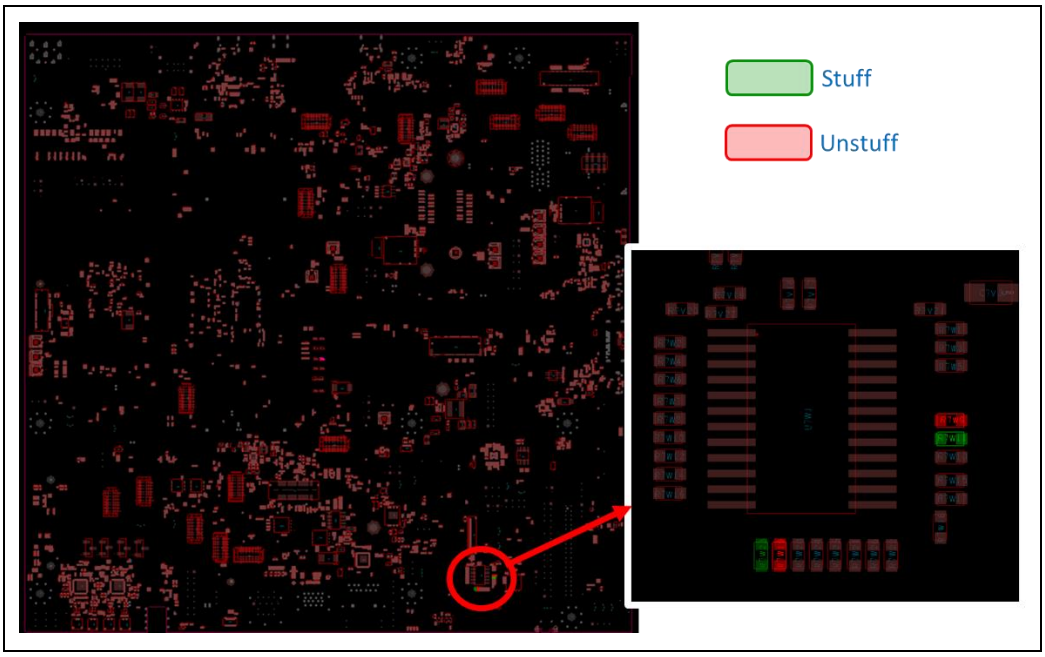


Figure 3-79. Layout Snapshot (Bottom Layer)



3.2.20 Rework to Enable Time-Sensitive Networking (TSN) Ethernet Controller

Description: This rework is required in order for TSN controller to communicate to TSN PHY on AIC (add-in card) through the MDIO bus. This rework also routes the misc. GPIO pins to headers on the RVP, which can be connected to the PHY via flying leads.

Impact if not done: After this rework is applied, the PCIe* x1 slot will be non-functional for other PCIe* cards.

Details: SMD Resistor rework

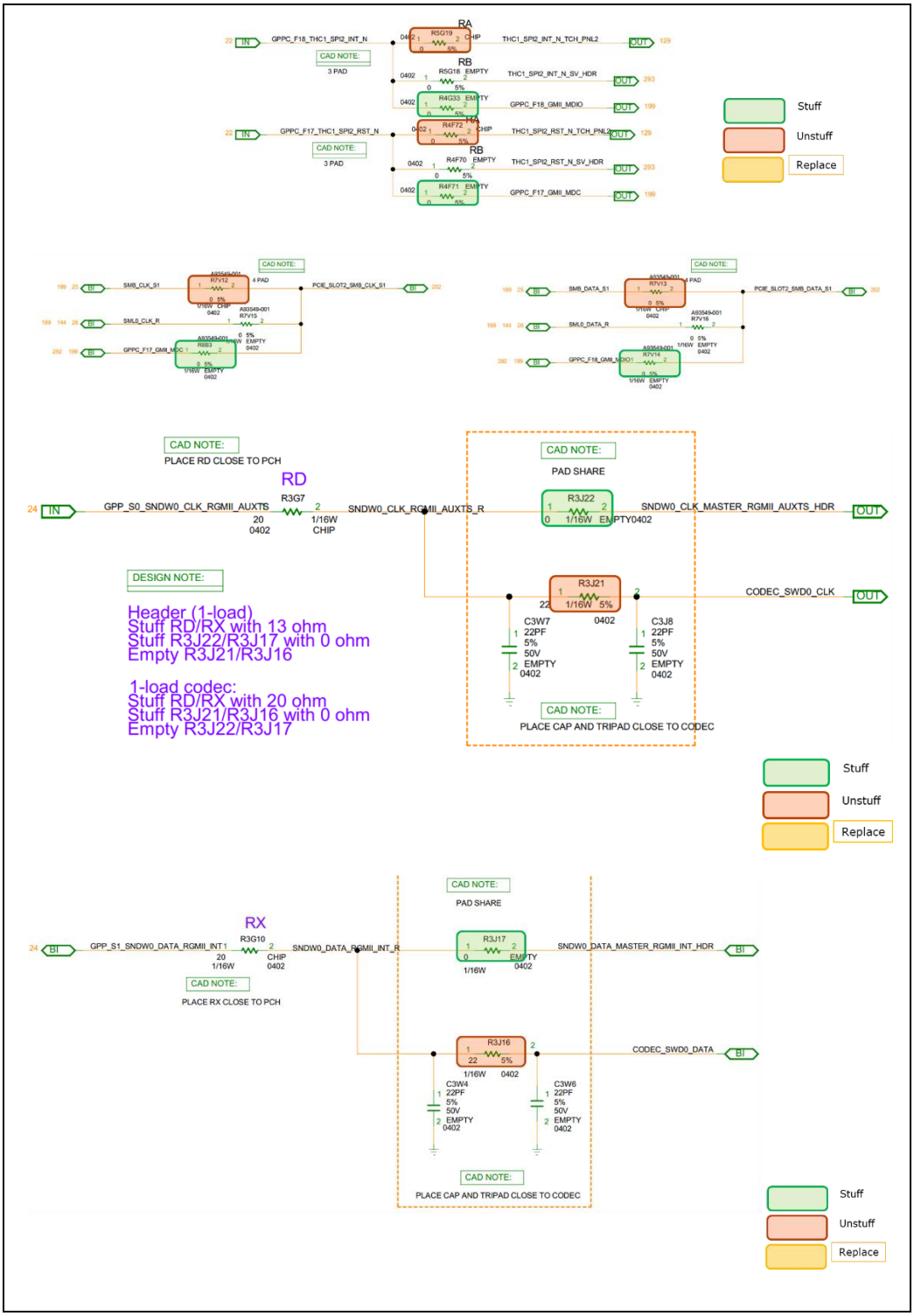
Applicable To: TGL UP3 RVP boards

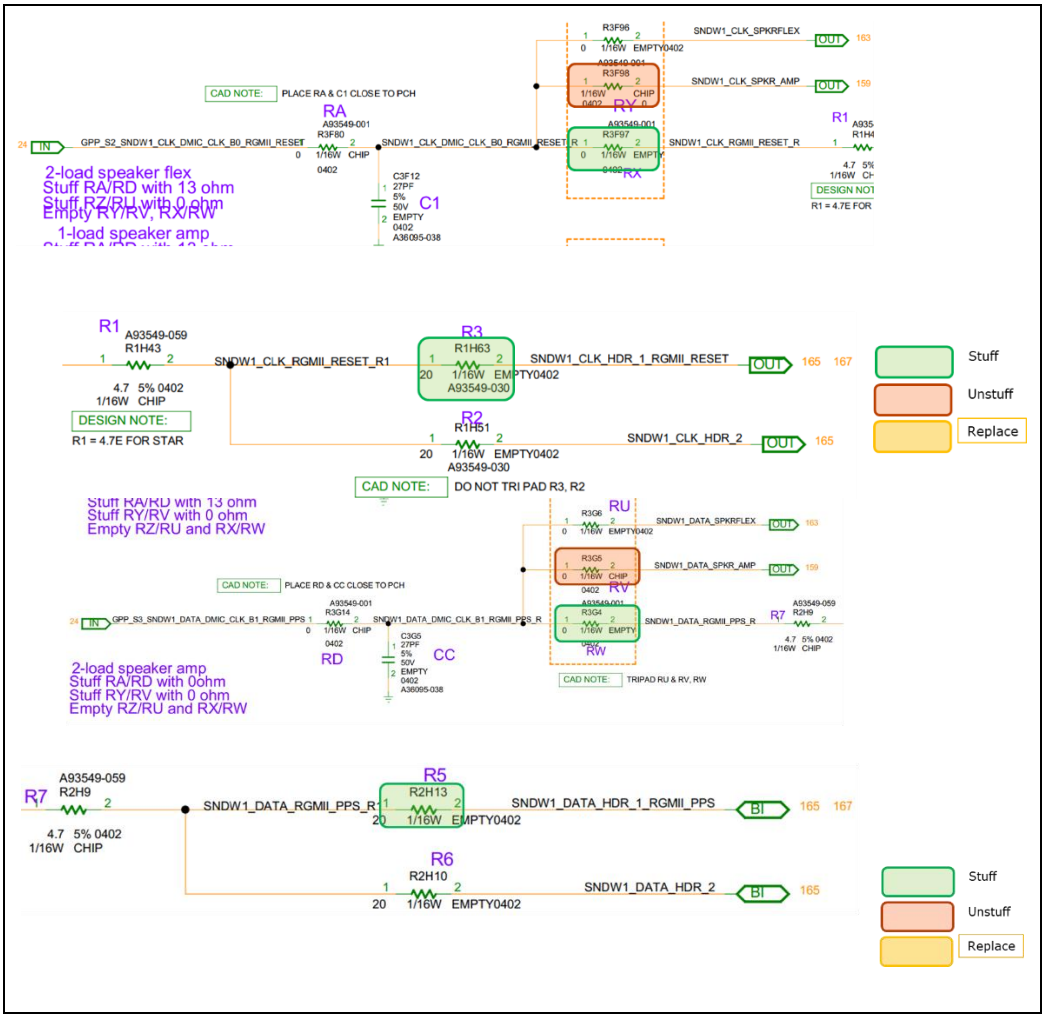
WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191203, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, and IPTL192701

Table 3-38. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R5G19 R4F72 R7V12 R7V13 R3J21 R3J16 R3F98 R3G5	RES D, 0402, 0.0 Ohm, 5.00%, 1/10 W	NA
Stuff	Resistor	R4G33 R4F71 R8B3 R7V14 R3J22 R3J17 R3F97 R1H63 R3G4 R2H13	NA	RES D, 0402, 0.0 Ohm, 5.00%, 1/10 W

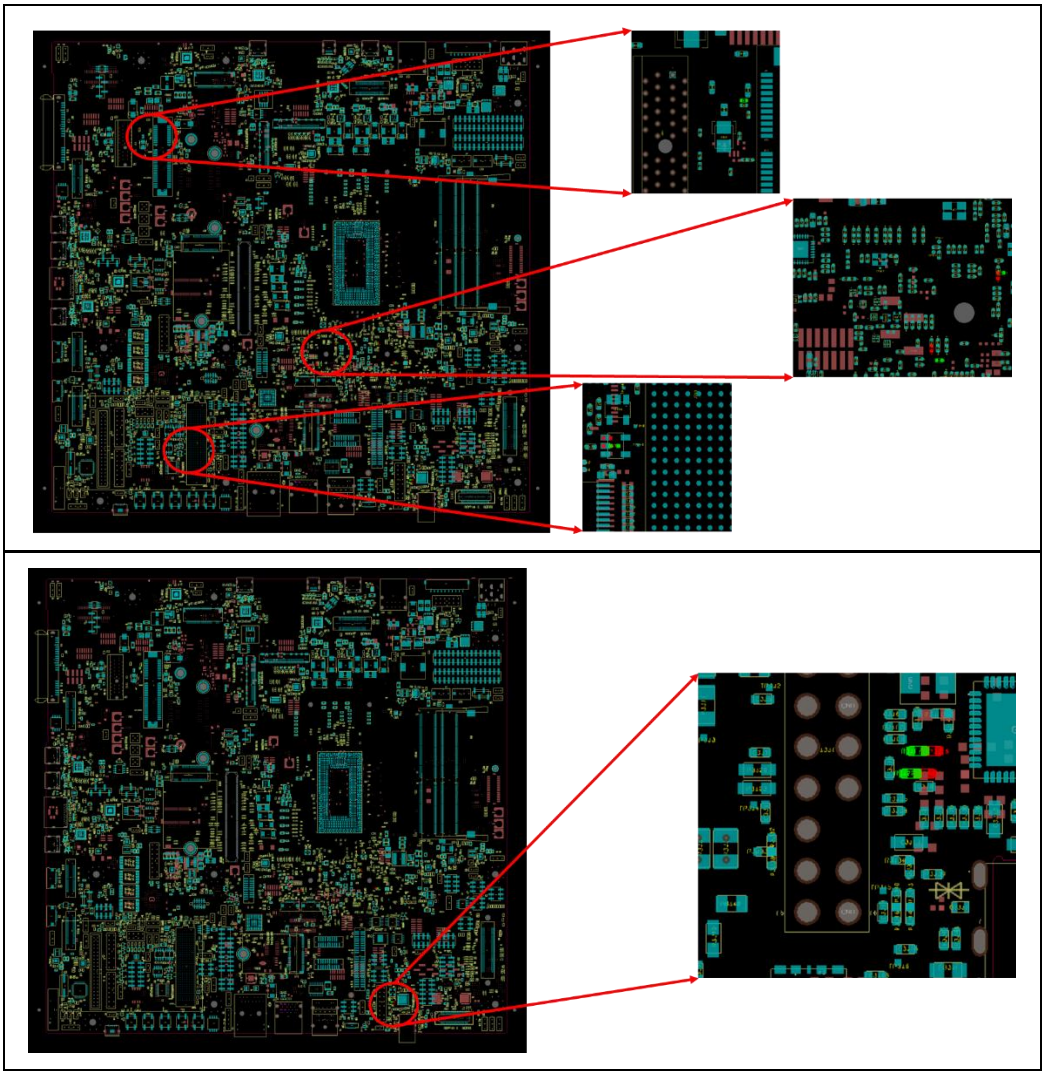
Figure 3-80. Schematic Snapshot

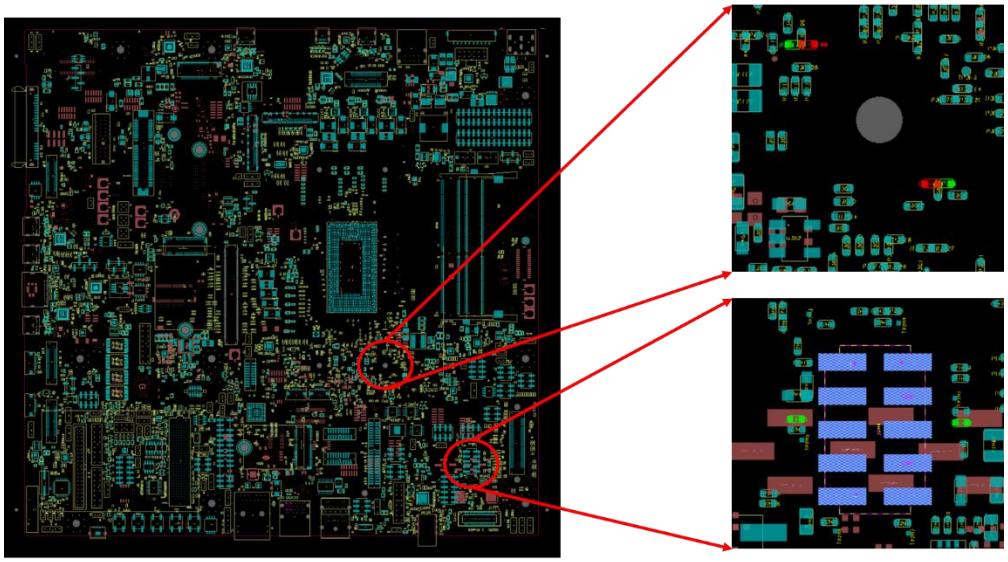




NOTE: The schematic reference description and layout snapshot refers to TGL UP3 DDR4 SoDIMM RVP board.

Figure 3-81. Layout Snapshot (Top Layer)





3.2.21 MAF Configuration to SAF Rework on TGL UP3 RVP

Description: This rework enables SAF configuration from MAF on TGL UP3 RVP.

Impact if done: By implementing this rework, TGL UP3 RVP works in SAF mode, while MAF/G3 Flash sharing mode is not worked.

Details: SMD Unstuff/stuff

Applicable To: All TGL UP3 RVPs

WO# Applicable for this Rework: IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194702, IPTL201901 and IPTL194202.

Table 3-39. Rework Details

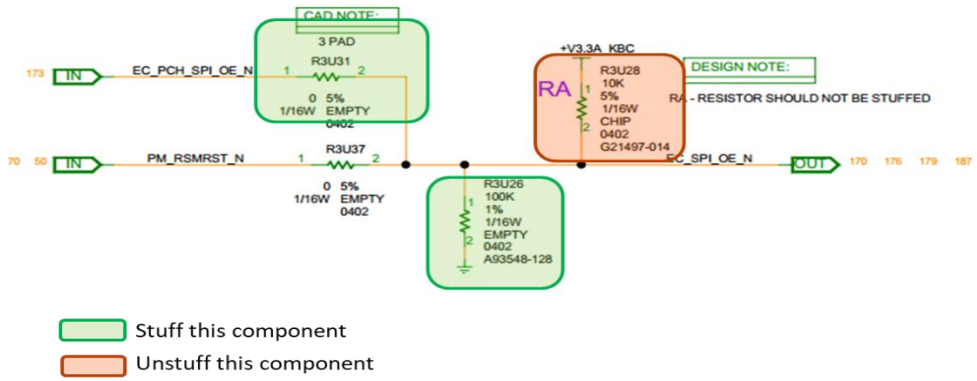
Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R5H38 R6H1	0E, 5%, 0402	NA
Unstuff	Capacitor	C3G16	0.220UF, 0402, 10 V	NA
Unstuff	Resistor	R3U28	10K, 5%, 0402	NA

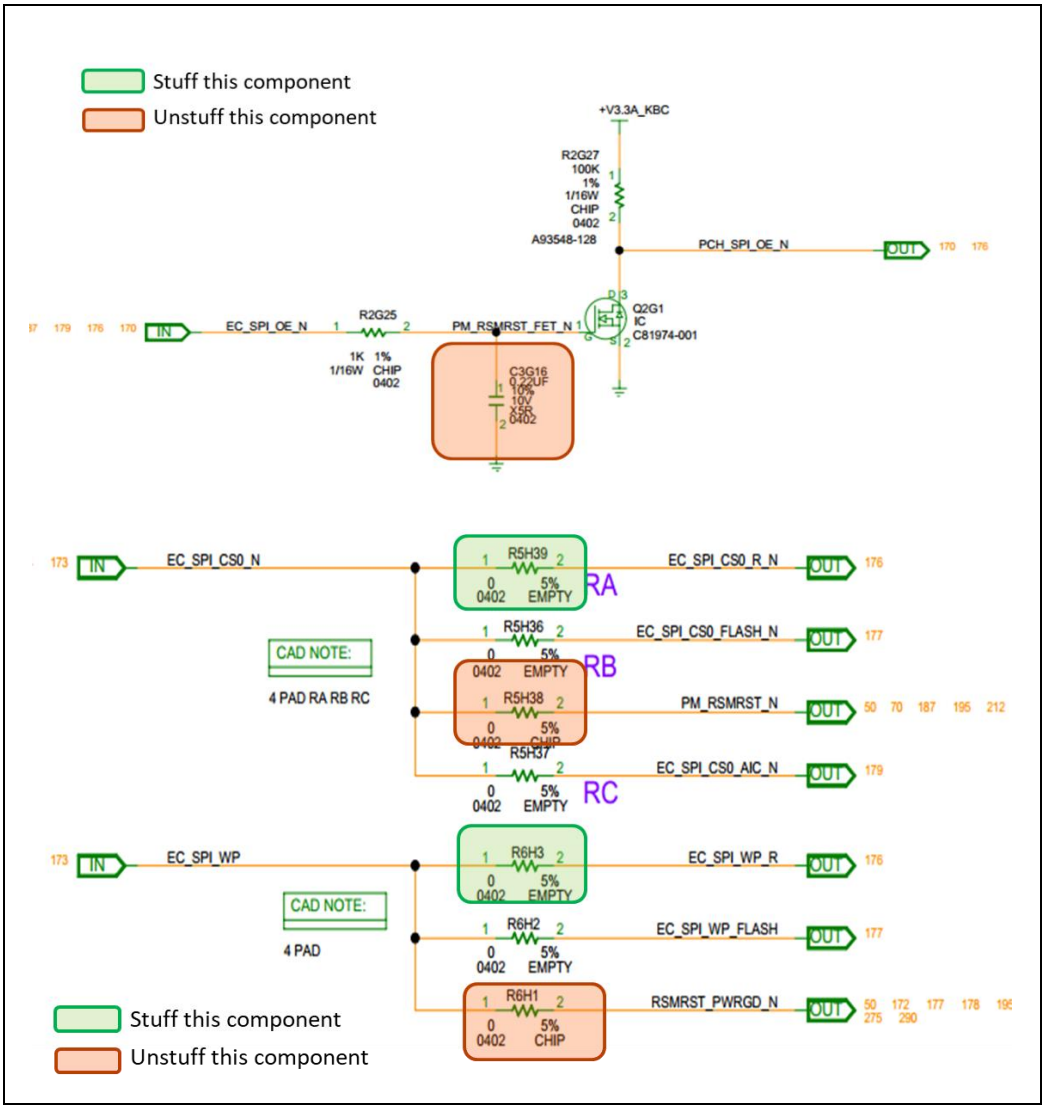
Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R3U31 R5H39 R6H3	NA	0E, 5%, 0402
Stuff	Resistor	R6W2	NA	10K, 5%, 0402
Stuff	Resistor	R6E27	NA	4.7K, 5%, 0402
NOTE: Set the jumper J7H1(1-2)				

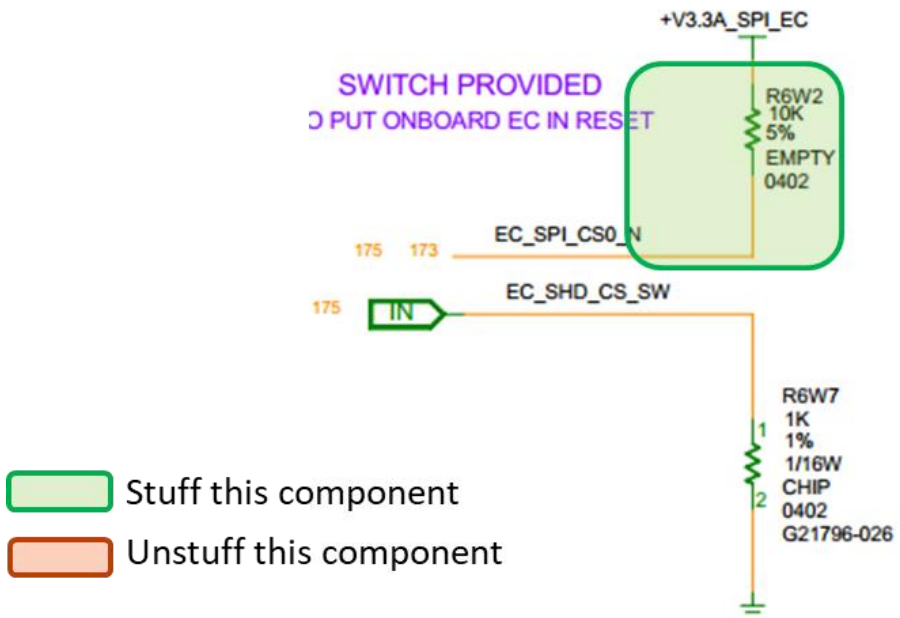
Table 3-40. Reference Designator Comparison

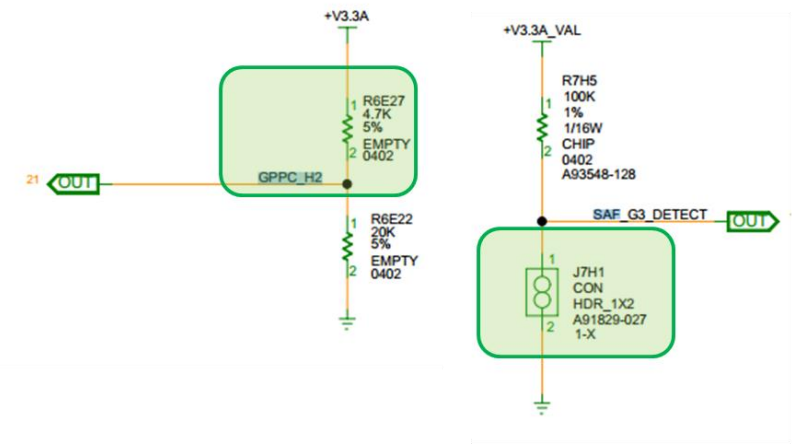
TGL UP3 DDR4	TGL UP3 LP4x	TGL UP3 LP5
R5H38	R5H36	R5H38
R6H1	R6H2	R6H2
C3G16	C3G16	C3G16
R3U28	R3U31	R3U31
R3U31	R3U34	R3U32
R5H39	R5H39	R5H39
R6H3	R6H3	R6H1
R6W2	R6W2	R6W2
R6E27	R6E18	R6E13
J7H1	J7H1	J7H1

Figure 3-82. Schematic Snapshot




Stuff this component
Unstuff this component
+V3.3A_KBC
R2G27
100K
1%
1/16W
CHIP
0402
A93548-128
PCH_SPI_OE_N
OUT
170
176
Q2G1
IC
C81974-001
IN
EC_SPI_OE_N
R2G25
1K 1%
1/16W CHIP
0402
PM_RSMRST_FET_N
C3G16
0.22UF
10%
10V
X5R
0402
173
EC_SPI_CS0_N
R5H39
0
0402
5%
EMPTY
RA
EC_SPI_CS0_R_N
177
R5H36
EC_SPI_CS0_FLASH_N
CAD NOTE:
4 PAD RA RB RC
RB
R5H38
PM_RSMRST_N
50
70
187
195
212
R5H37
EC_SPI_CS0_AIC_N
179
RC
EC_SPI_WP
R6H3
EC_SPI_WP_R
CAD NOTE:
4 PAD
R6H2
EC_SPI_WP_FLASH
R6H1
CHIP
RSMRST_PWRGD_N
172
275
290
Stuff this component
Unstuff this component





Stuff this component

Unstuff this component

- Set the jumper J7H1 (1-2)

Figure 3-83. Layout Snapshot (Bottom Layer)

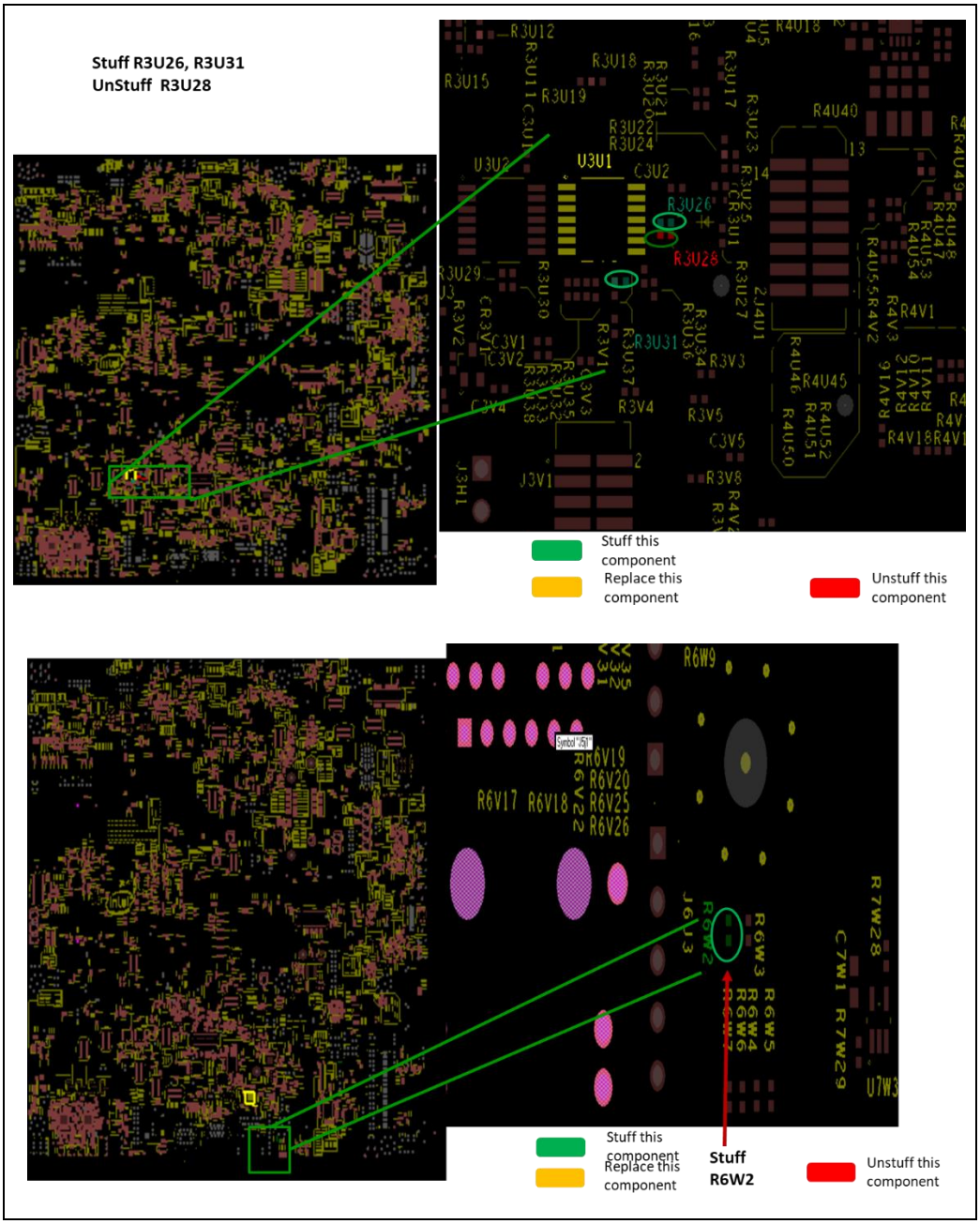
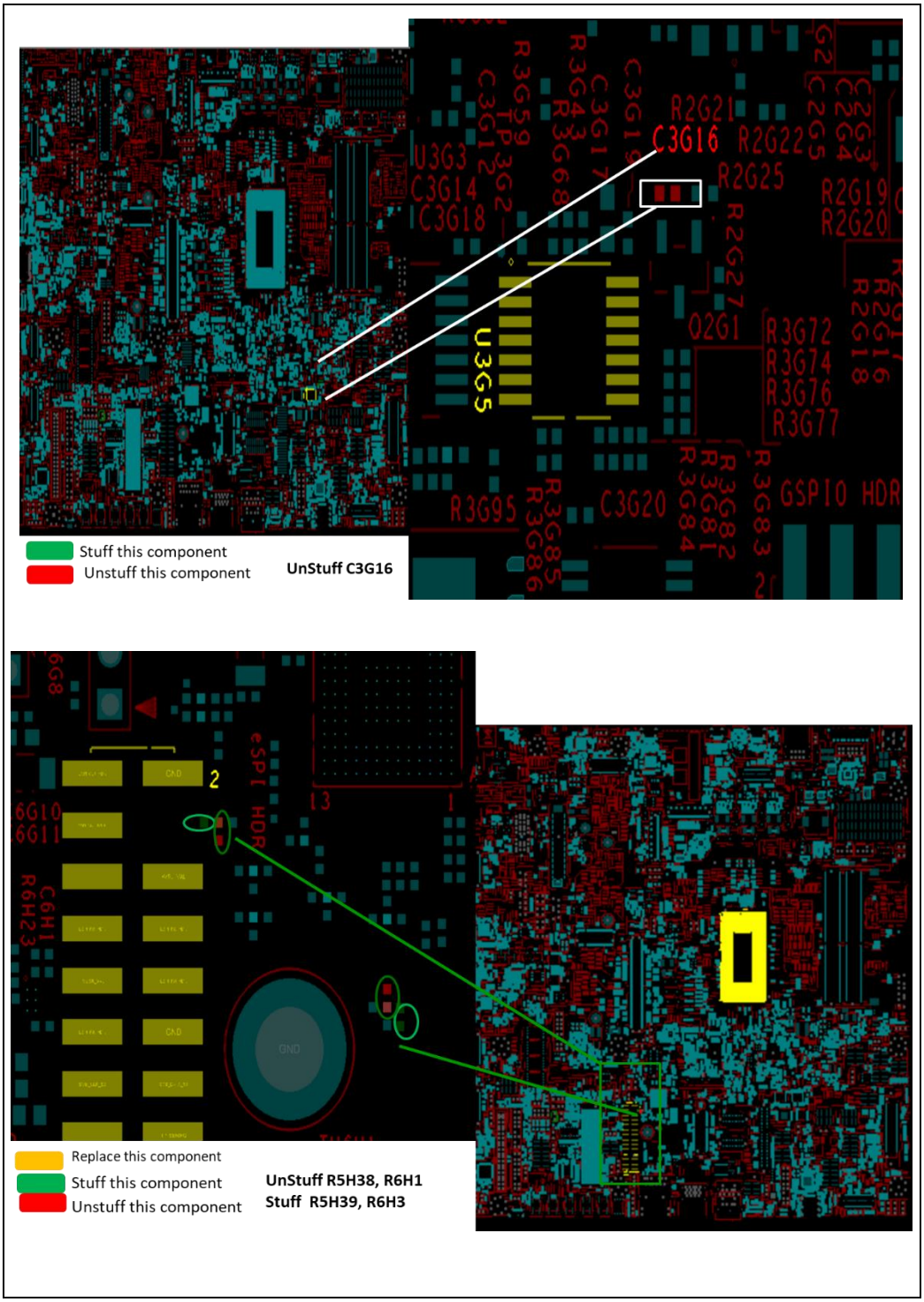
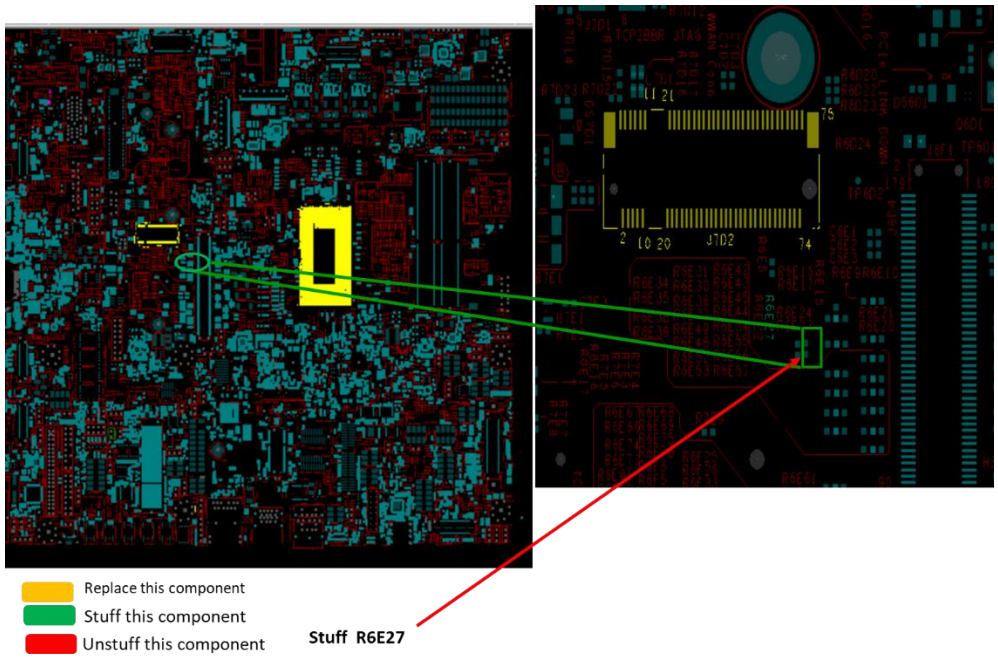
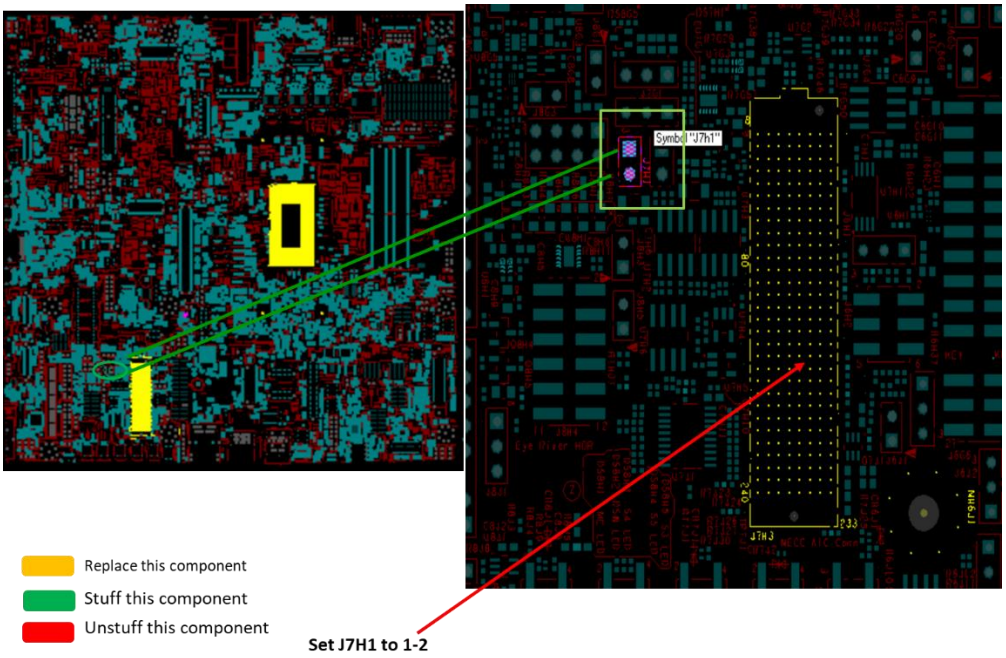


Figure 3-84. Layout Snapshot (Top Layer)




Replace this component
Stuff this component
Unstuff this component
Stuff R6E27


Replace this component
Stuff this component
Unstuff this component
Set J7H1 to 1-2

3.2.22 Rework to Change MAF Configuration to G3 on TGL UP3 RVP

Description: This rework enables G3 configuration from MAF on TGL UP3 RVP.

Impact if not done: By implementing this rework, TGL UP3 RVP works in G3 Mode and MAF/SAF Flash sharing mode is not worked.

Details: SMD Unstuff/Stuff

Applicable To: All TGL UP3 RVPs

WO# Applicable for this Rework: IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192702, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL201201, IPTL194202, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

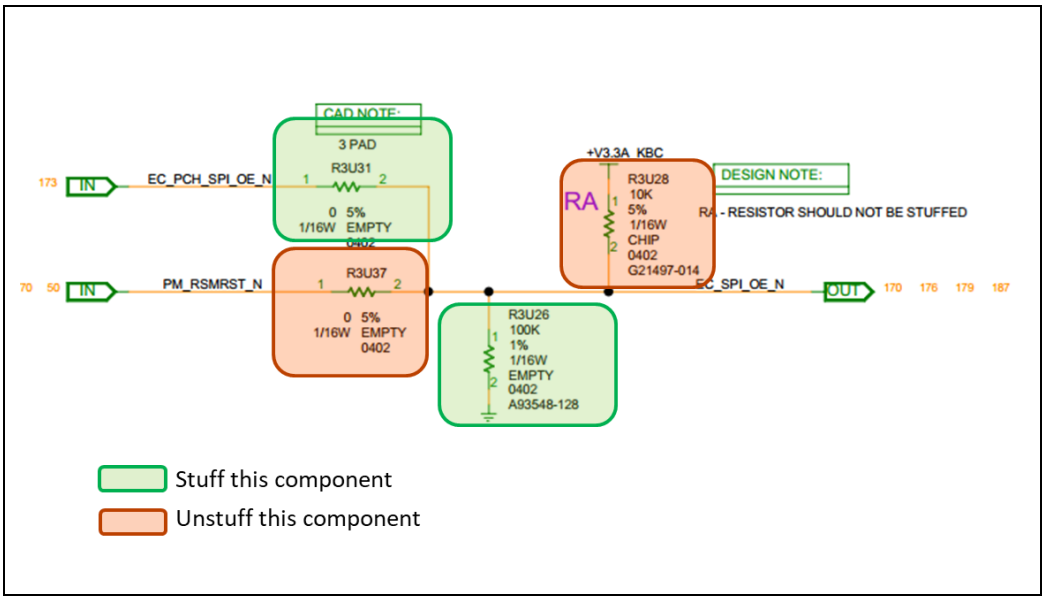
Table 3-41. Rework Details

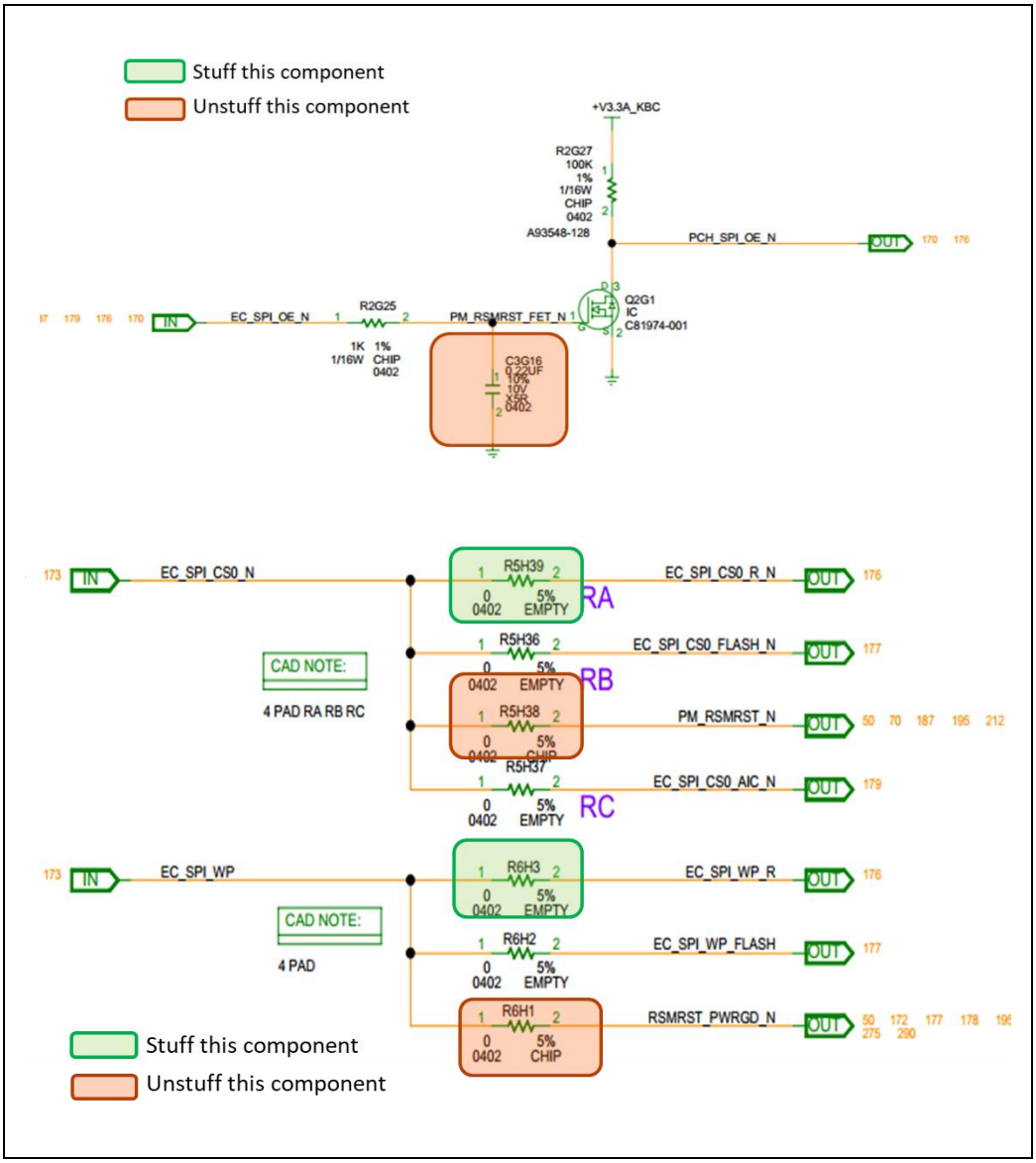
Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R3U31	NA	0E, 5%, 0402
Unstuff	Resistor	R3U37	0E, 5%, 0402	NA
Unstuff	Resistor	R3U28	10K, 5%, 0402	NA
Unstuff	Capacitor	C3G16	0.22UF, 10%, 0402	NA
Stuff	Resistor	R5H39	NA	0E, 5%, 0402
Unstuff	Resistor	R5H38	10K, 5%, 0402	NA
Stuff	Resistor	R6H3	NA	0E, 5%, 0402
Unstuff	Resistor	R6H1	0E, 5%, 0402	NA
Stuff	Resistor	R6W2	NA	10K, 5%, 0402
Stuff	Resistor	R3U26	NA	100K, 5%, 0402

Table 3-42. Reference Designator Comparison

TGL UP3 DDR4	TGL UP3 LP4x	TGL UP3 LP5
R5H38	R5H36	R5H38
R6H1	R6H2	R6H2
C3G16	C3G16	C3G16
R3U28	R3U31	R3U31
R3U31	R3U34	R3U32
R5H39	R5H39	R5H39
R6H3	R6H3	R6H1
R6W2	R6W2	R6W2
R3U37	R3U40	R3U38
R3U26	R3U29	R3U27

Figure 3-85. Schematic Snapshot




Stuff this component
Unstuff this component
+V3.3A_KBC
R2G27
100K
1%
1/16W
CHIP
0402
A93548-128
PCH_SPI_OE_N
OUT
170 176
Q2G1
IC
C81974-001
IN
EC_SPI_OE_N
R2G25
1K 1%
1/16W CHIP
0402
PM_RSMRST_FET_N
C3G16
0.22UF
10%
10V
X5R
0402
173
IN
EC_SPI_CS0_N
R5H39
0
0402
5%
EMPTY
RA
EC_SPI_CS0_R_N
OUT
176
R5H36
0
0402
5%
EMPTY
RB
EC_SPI_CS0_FLASH_N
OUT
177
CAD NOTE:
4 PAD RA RB RC
R5H38
0
0402
5%
CHIP
PM_RSMRST_N
OUT
50 70 187 195 212
R5H37
0
0402
5%
EMPTY
RC
EC_SPI_CS0_AIC_N
OUT
179
173
IN
EC_SPI_WP
R6H3
0
0402
5%
EMPTY
EC_SPI_WP_R
OUT
176
CAD NOTE:
4 PAD
R6H2
0
0402
5%
EMPTY
EC_SPI_WP_FLASH
OUT
177
R6H1
0
0402
5%
CHIP
RSMRST_PWRGD_N
OUT
50 172 177 178
275 290
Stuff this component
Unstuff this component

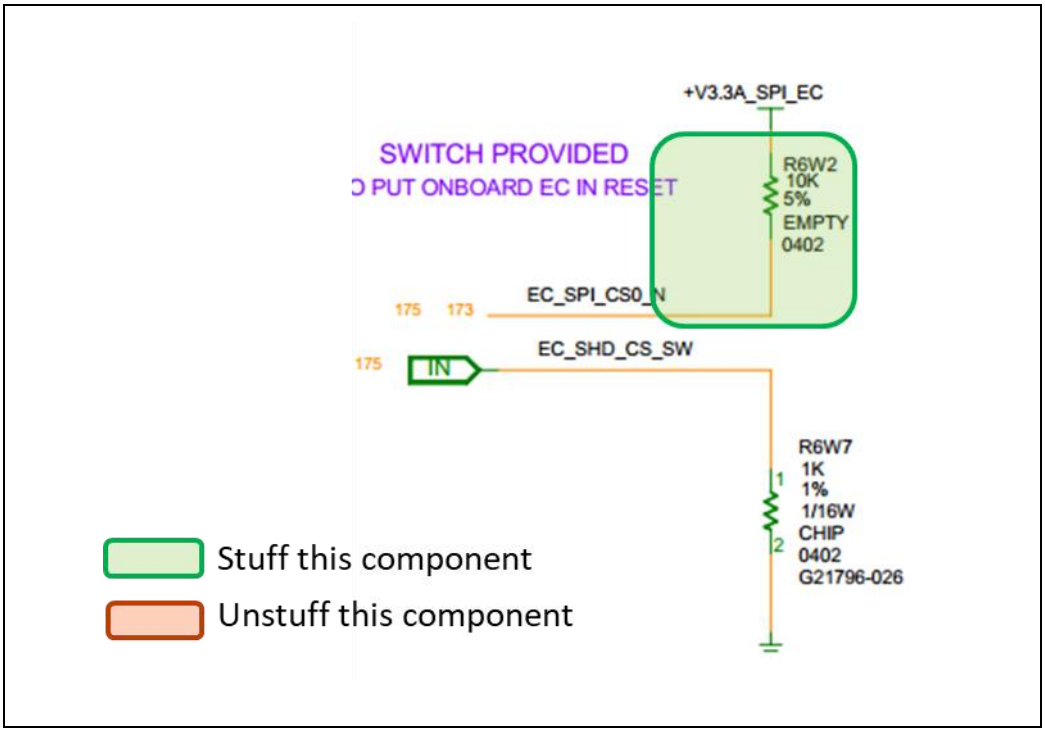
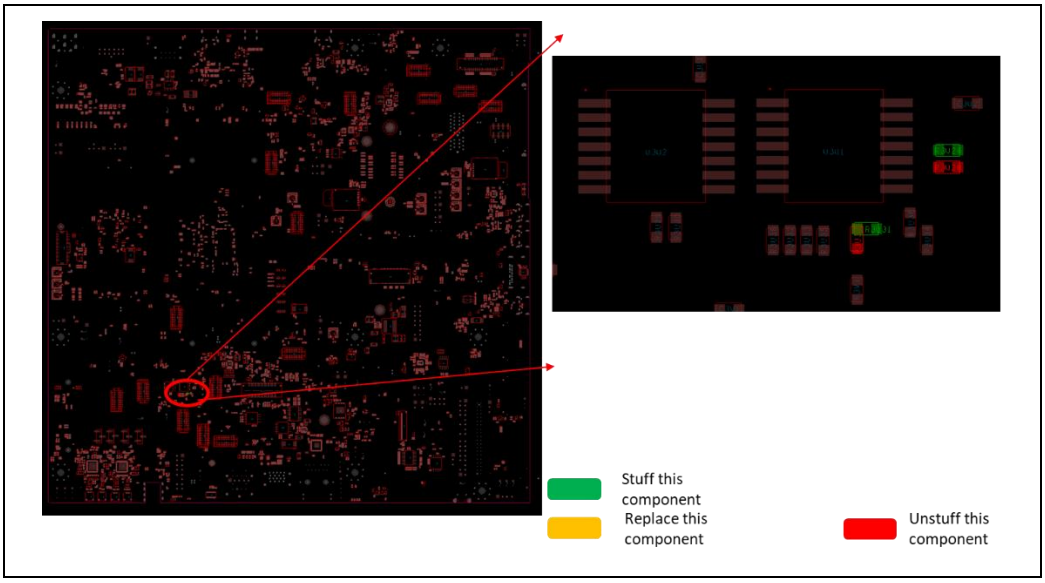


Figure 3-86. Layout Snapshot (Bottom Layer) (Flip View)



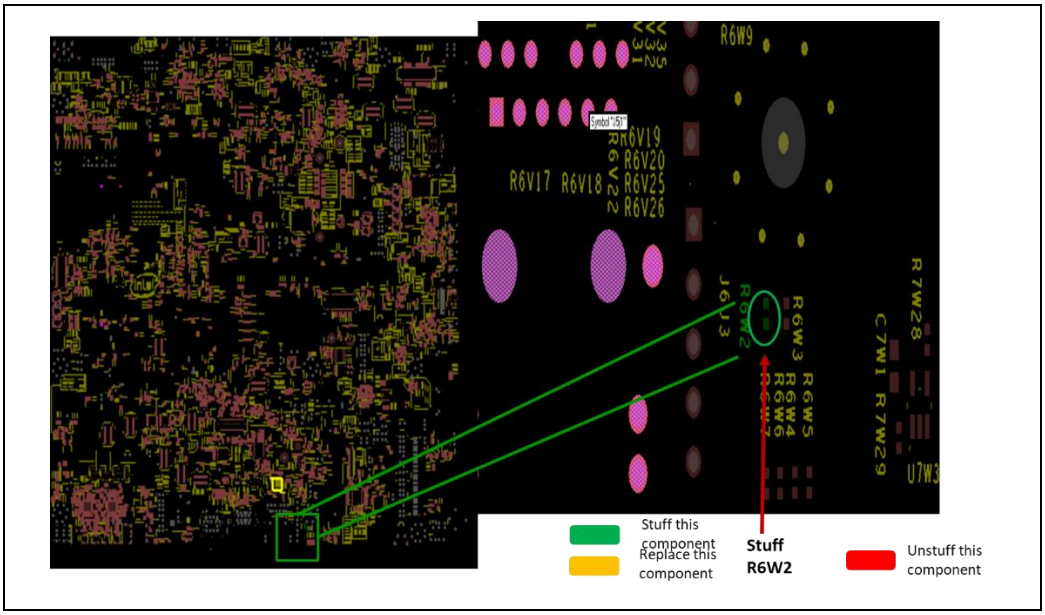
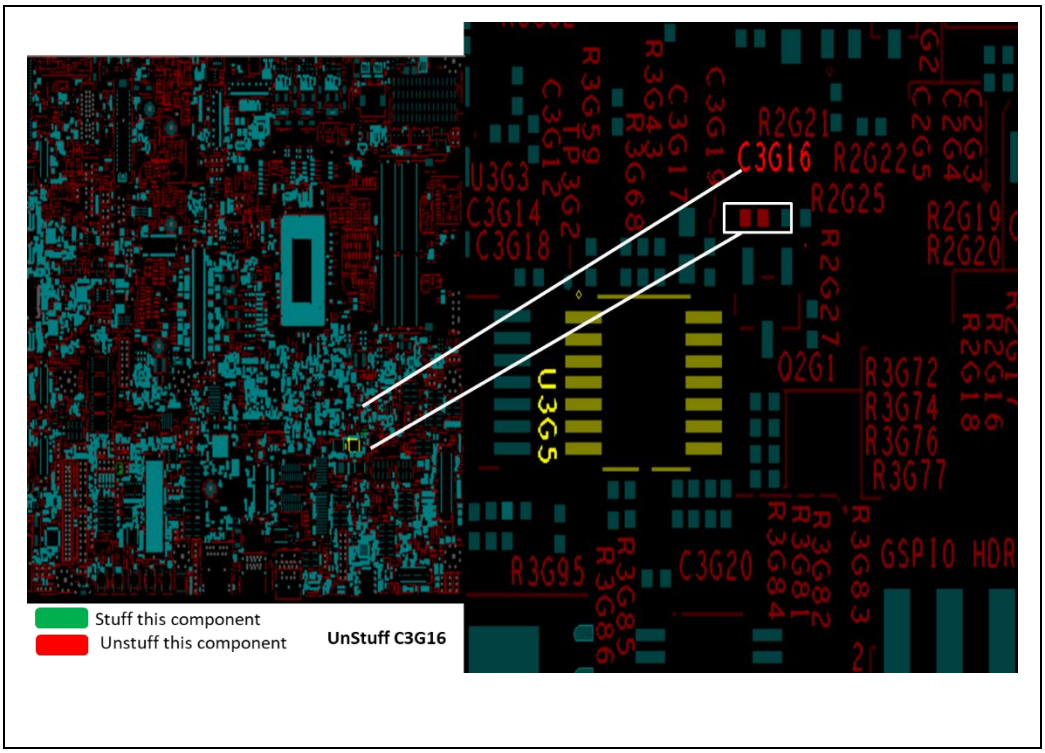
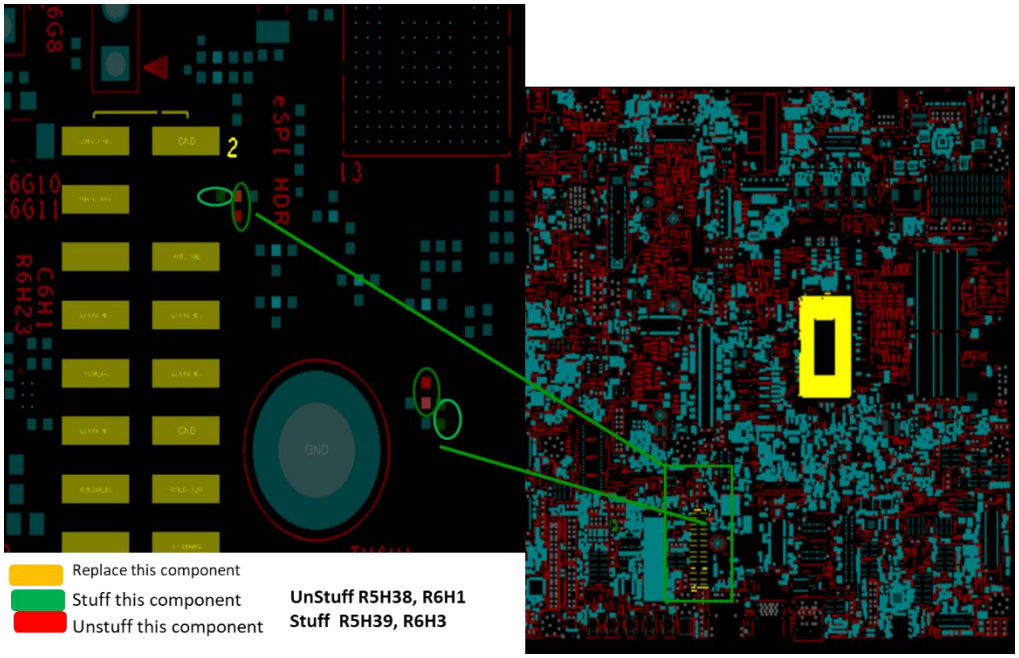


Figure 3-87. Layout Snapshot (Top Layer)





3.2.23 Rework to Enable Elixir VCCST and VCCSTG Gates

Description: This rework is to enable the elixir VCCST and VCCSTG gates for the system boot (and disable External Power Gates).

Impact if not done: Currently, board has external gates to enable the VCCST and VCCSTG. This rework disables the External Power Gates and enables the EXS Power Gates.

Details: Jumper set

Applicable To: TGL UP3 LP4x EXS ERB boards

WO# Applicable for this Rework: IPTL192401

Table 3-43. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Set	Jumper	J5F1	NA	Set the jumper 1-2
Set	Jumper	J6F2	NA	Set the jumper 1-2

Figure 3-88. Schematic Snapshot

TGL UP3EXS LP4 RVP:

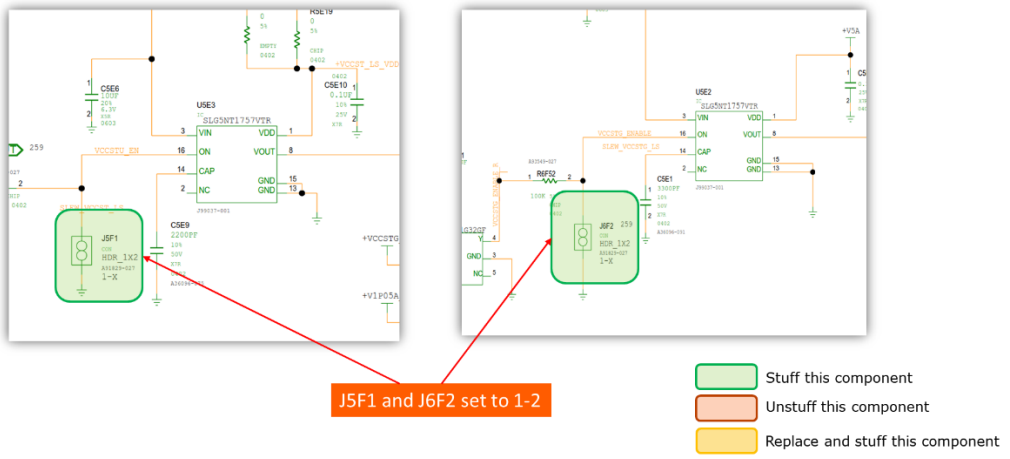
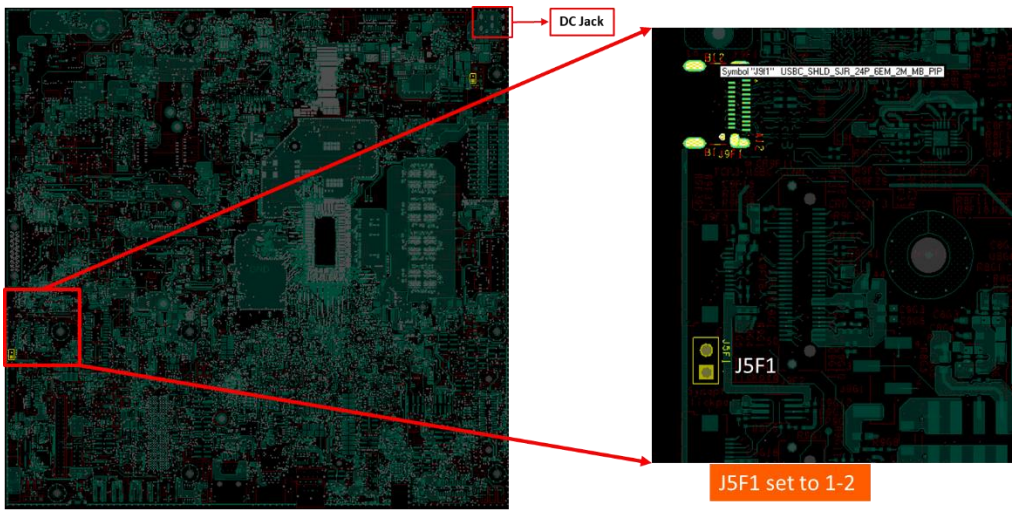
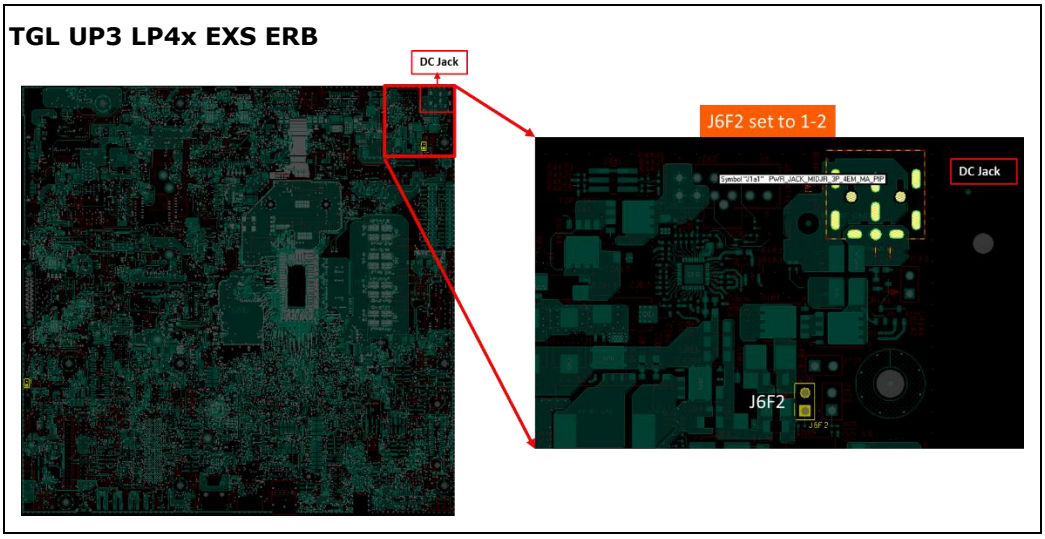


Figure 3-89. Layout Snapshot (Top Layer)

TGL UP3 LP4x EXS ERB





3.2.24 Rework to Enable FIVR External Bypass on TGL UP3 DDR4

Description: Rework to enable FIVR external bypass on TGL UP3 DDR4

Impact if done: FIVR VR will be bypassed.

Rework Details: SMD Resistor rework

Applicable To: TGL UP3 DDR4, TGL UP3 LP4x SKU

WO# Applicable for this Rework: IPTL191002, IPTL191201, IPTL191204, IPTL191202, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192502, IPTL192601, IPTL192604, IPTL192701, IPTL192801, IPTL193501 IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202 IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192702, IPTL192802 IPTL193502, IPTL193601,, IPTY191801, IPTY191802, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTL194702, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY193901, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

Table 3-44. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R4U14	NA	Res, 0805, 0.005 Ohms
Unstuff	Resistor	R4U13	Res, 0402, 0 Ohms	NA
Stuff	Resistor	R4T3	NA	Res, 0402, 0 Ohms

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R4U9	NA	Res, 0805, 0.005 Ohms
Unstuff	Resistor	R4U1	Res, 0402, 0 Ohms	NA
Stuff	Resistor	R4U2	NA	Res, 0402, 0 Ohms

Table 3-45. Rework Details

TGL-UP3 DDR4	TGL-UP3 LP4x
R4U14	R4U14
R4U13	R4U13
R4T3	R4T3
R4U9	R4U9
R4U1	R4U1
R4U2	R4U2

Figure 3-90. Schematic Snapshot

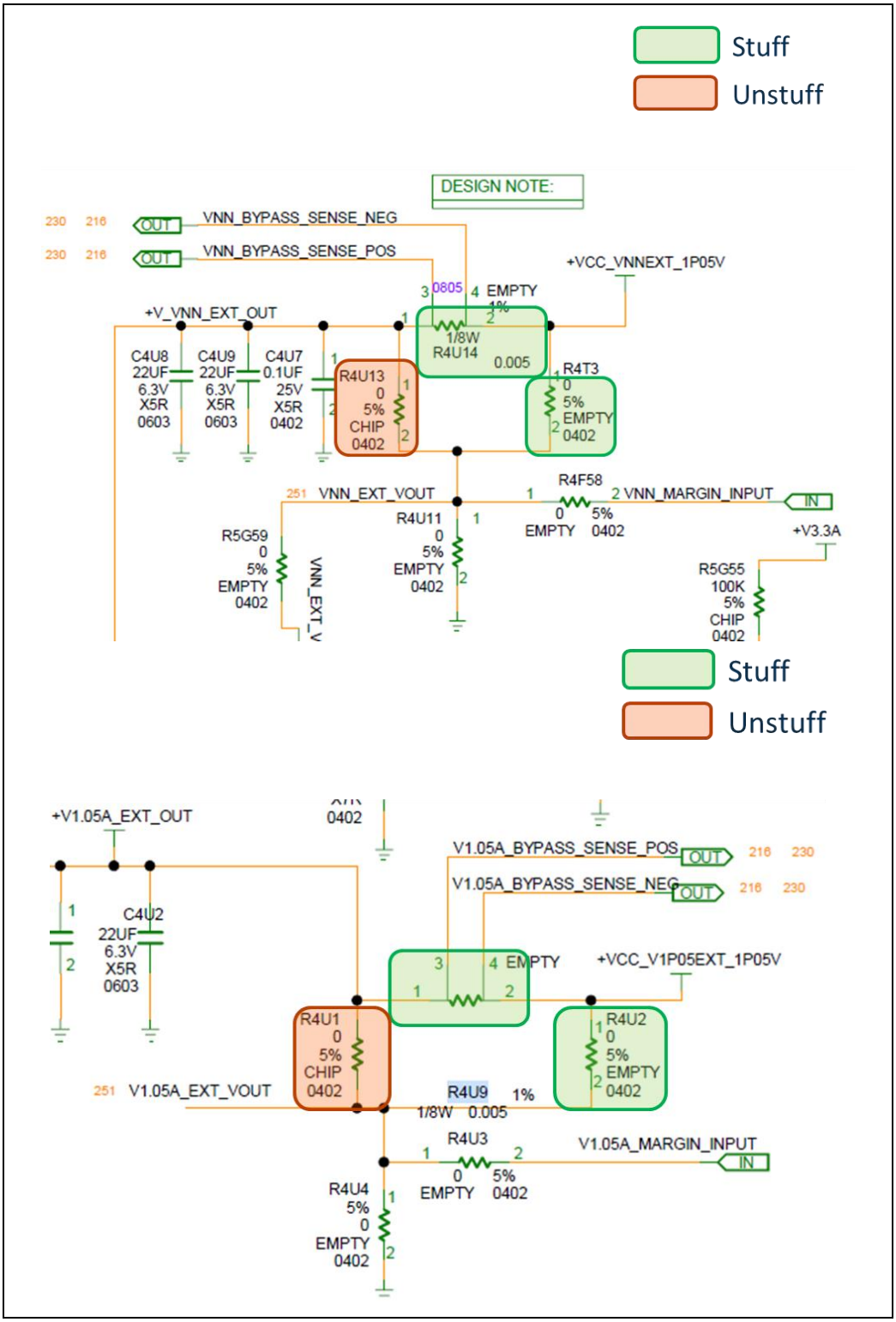
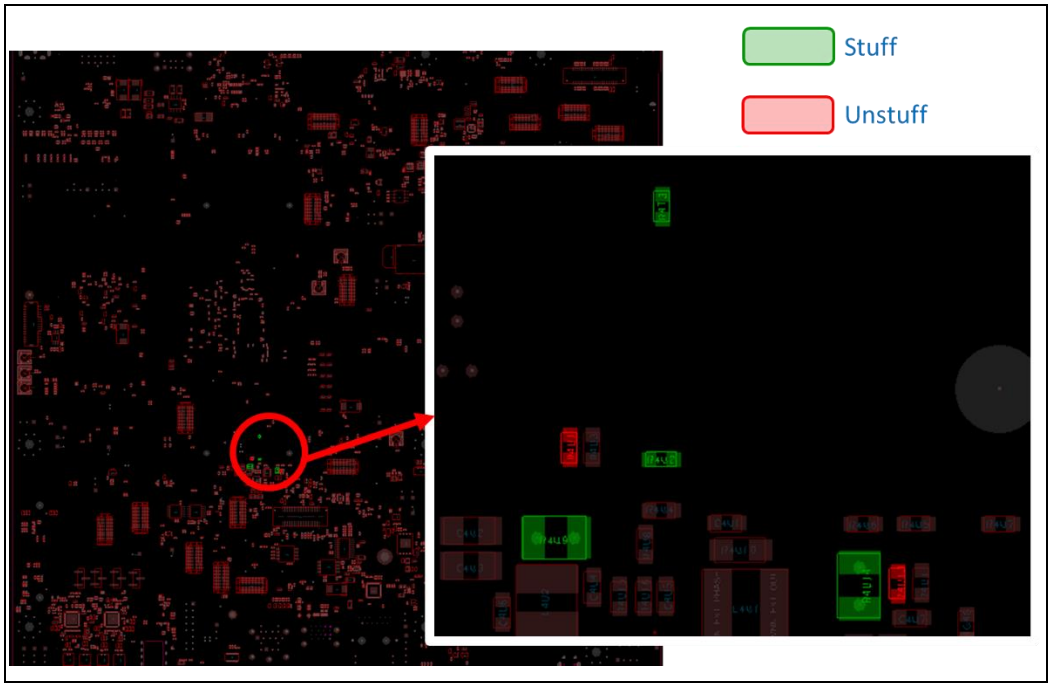


Figure 3-91. Layout Snapshot (Bottom Layer)



3.2.25 Rework to Enable EC MECC Connector for TGL UP3

Description: Rework to enable EC MECC connector for TGL UP3

Impact if not done: System can't boot with onboard EC.

"Rework to change MAF configuration to G3 on TGL UP3 RVP" – This rework should be applied before this rework to get the board working in G3 mode.

Rework Details: SMD Stuff/Unstuff

Applicable To: All TGL UP3 RVPs

WO# Applicable for this Rework: IPTL191002, IPTL191203, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192701, IPTL192801, IPTL193402, IPTL193501, IPTL193702, IPTL193801, IPTL193901, IPTL194702, IPTL194101, IPTL202401, IPTL203002.

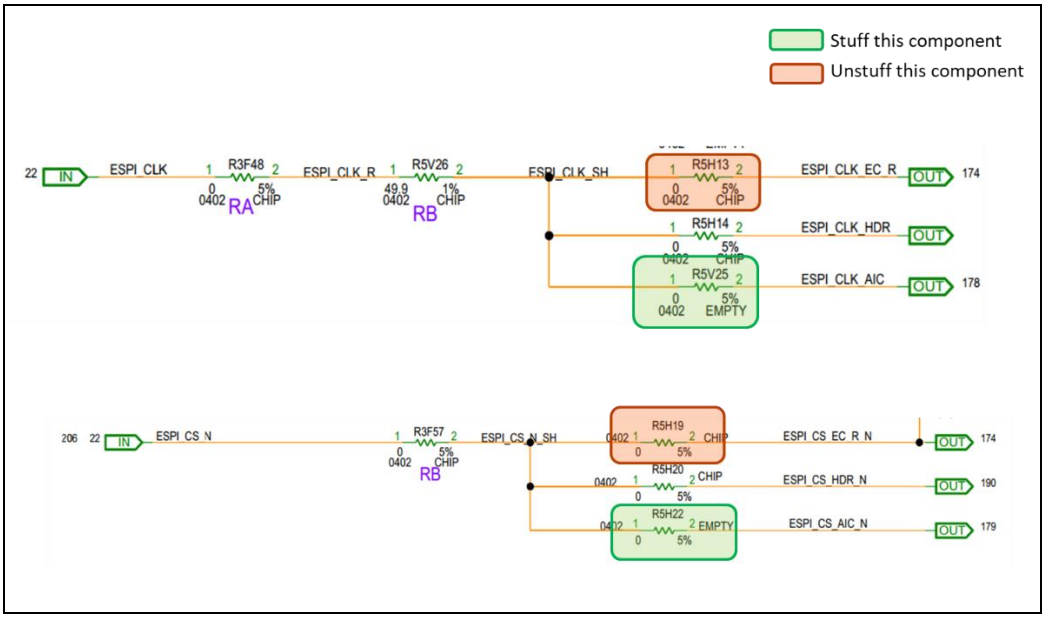
Table 3-46. Rework Details

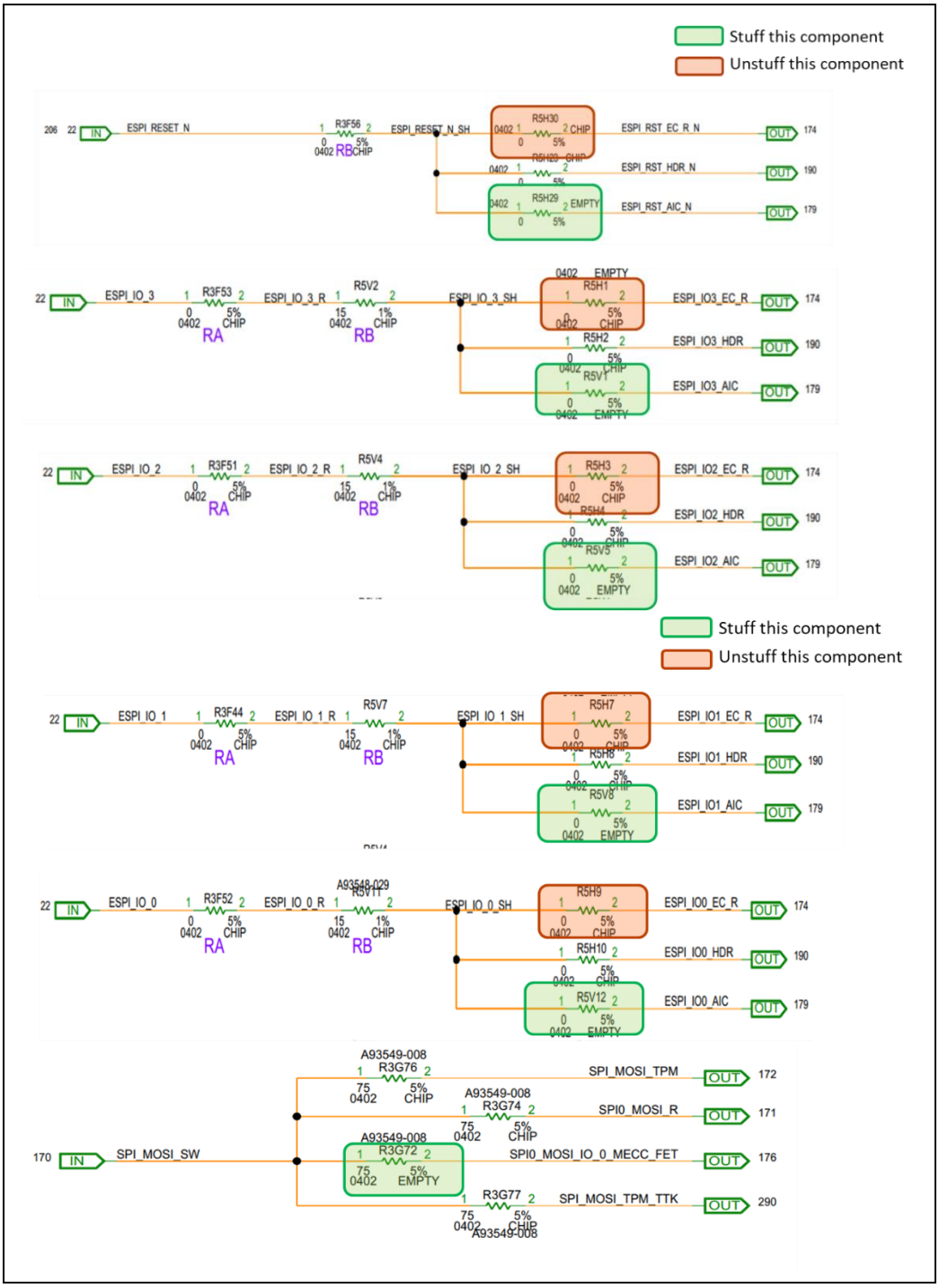
Action	Item	Reference Description	Description of Existing Part	Description of New Part
UnStuff	Resistor	R5H13, R5H19, R5H30, R5H1, R5H3, R5H7, R5H9, R4G5, R6H35, R5U20, R6H21, R6H12, R5H25, R5H39, R6H26, R6H31, R6V21	0ohms, 5%, 0402	NA
UnStuff	Resistor	R3F111	0ohms, 5%, 0402	NA
UnStuff	Resistor	R3U26	100K, 1%, 0402	NA
Stuff	Resistor	R5V25, R5H22, R5H29, R5V1, R5V5, R5V8, R5V12, R3G89, R4G1, R6H36, R6V27, R6V22, R6H19, R6H13, R5H26, R5H37, R9T27, R9T28, R4G70, R4G62, R6H33, R6H32, R7G48, R7G62	NA	0ohms,5%, 0402
Stuff	Resistor	R3G72, R3G83, R3G85	NA	75 Ohm, 5%, 0402
Stuff	Resistor	R3F113	NA	33 Ohm, 5%, 0402
Stuff	Resistor	R3U28	NA	10 K Ohm, 5% 0402

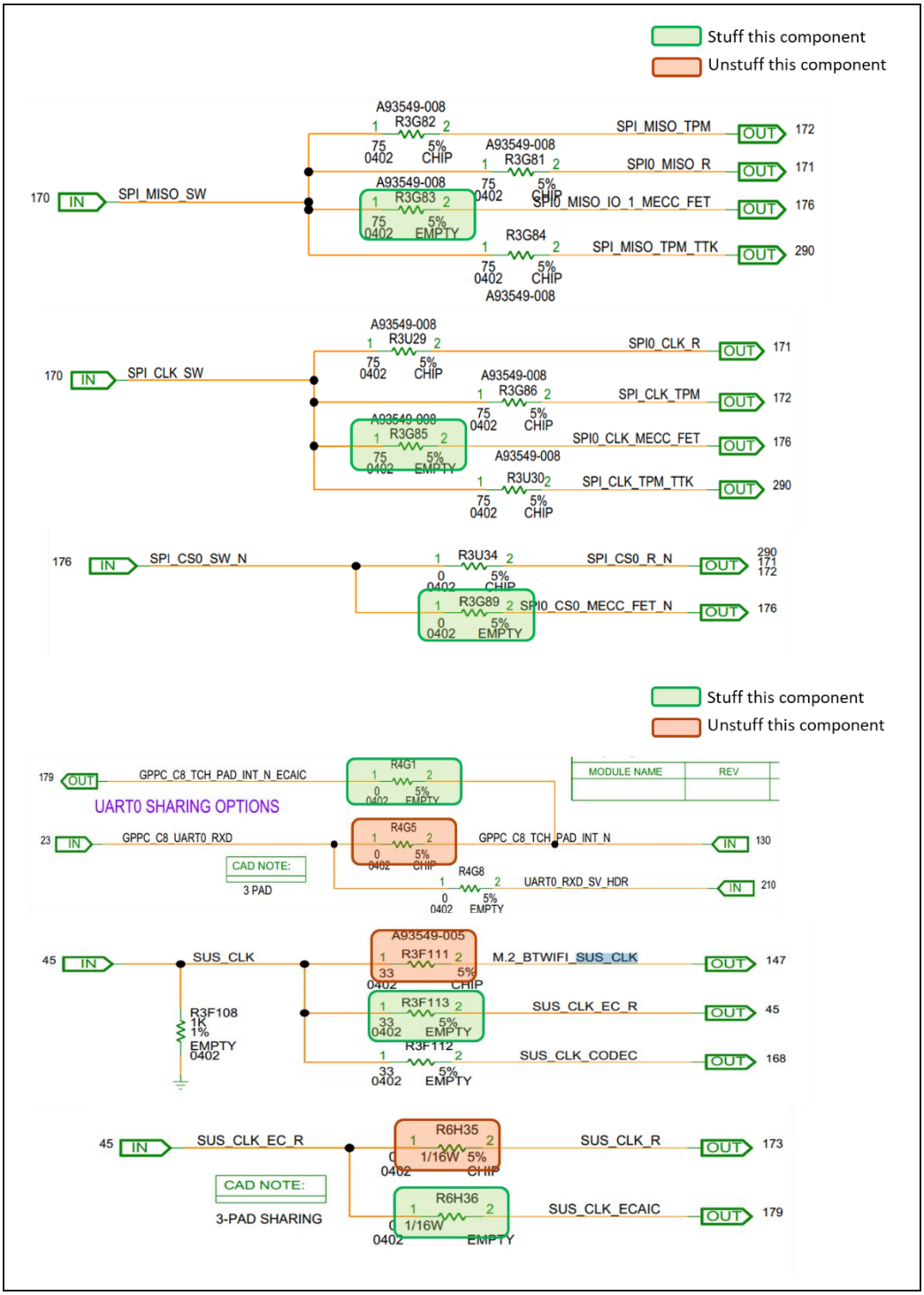
Table 3-47. Rework Details

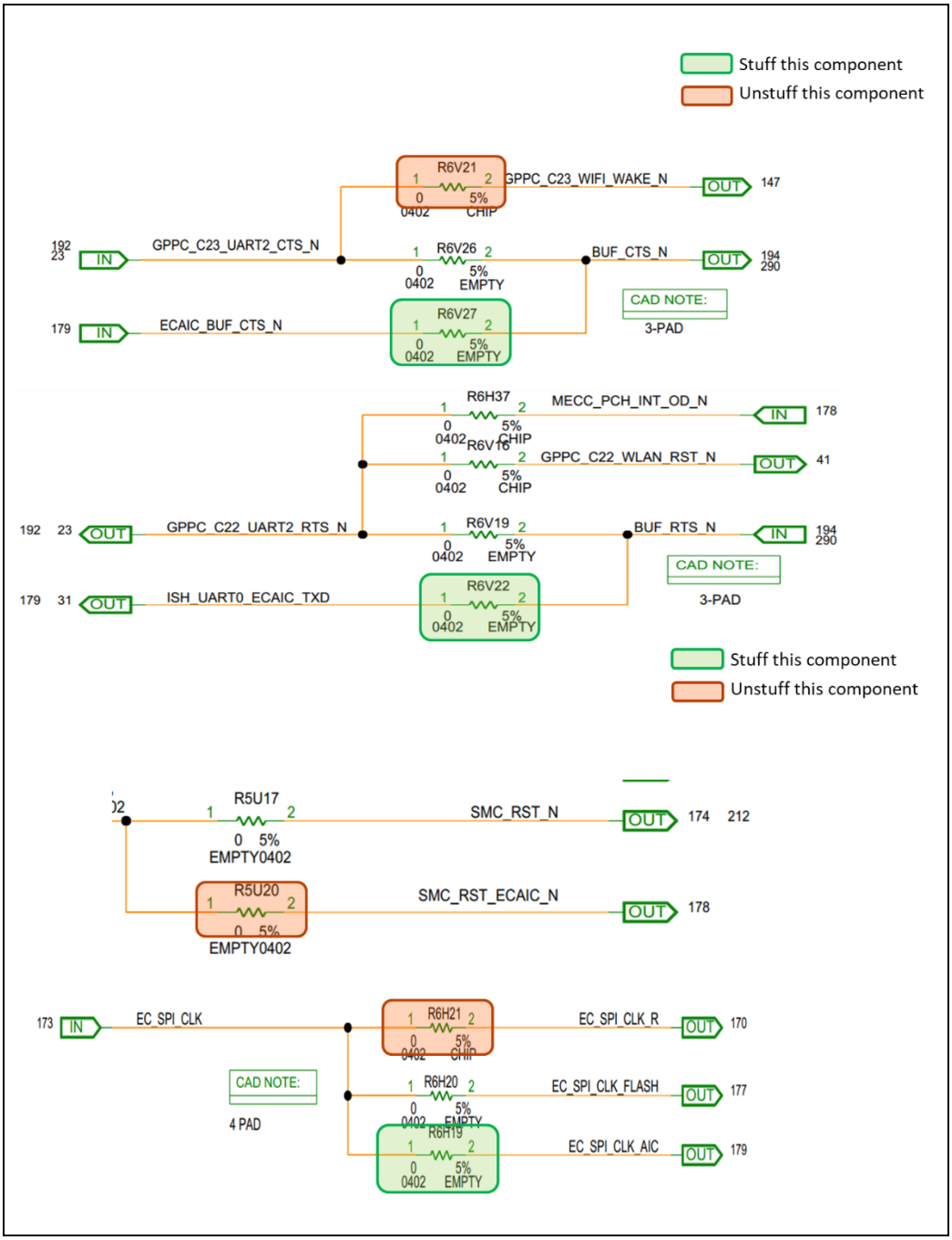
Action	Item	TGL UP3 DDR4	TGL UP3 LP4x
UNSTUFF	Resistor	R5H13, R5H19, R5H30, R5H1, R5H3, R5H7, R5H9, R4G5, R6H35, R5U20, R6H21, R6H12, R5H25, R5H39, R6H26, R6H31, R6V21	R5H13, R5H19, R5H30, R5H1, R5H3, R5H7, R5H9, R4G9, R6H35, R5U20, R6H19, R6H11, R5H25, R5H39, R6H25, R6H30, R6V21
UNSTUFF	Resistor	R3F111	R3F111
UNSTUFF	Resistor	R3U26	R3U29
STUFF	Resistor	R5V25, R5H22, R5H29, R5V1, R5V5, R5V8, R5V12, R3G89, R4G1, R6H36, R6V27, R6V22, R6H19, R6H13, R5H26, R5H37, R9T27, R9T28, R4G70, R4G62, R6H33, R6H32, R7G48, R7G62	R5V25, R5H22, R5H29, R5V1, R5V5, R5V8, R5V11, R3G90, R4G1, R6H34, R6V27, R6V22, R6H20, R6H13, R5H24, R5H37, R9T31, R9T32, R4G74, R4G65, R6H32, R6H31, R7G48, R7G62
STUFF	Resistor	R3G72, R3G83, R3G85	R3G73, R3G84, R3G86
STUFF	Resistor	R3F113	R3F113
STUFF	Resistor	R3U28	R3U31

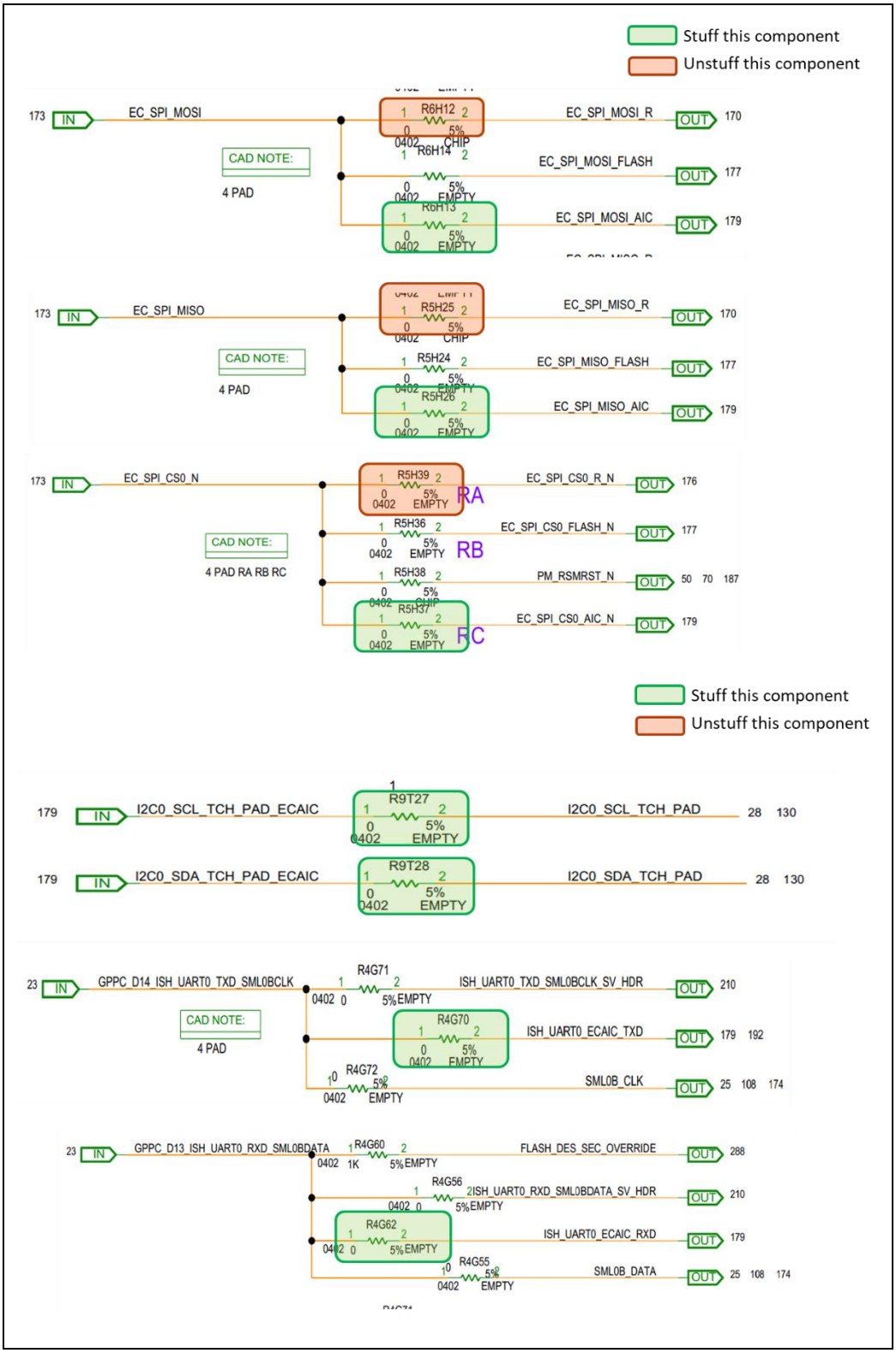
Figure 3-92. Schematic Snapshot




Stuff this component
Unstuff this component
ESPI_RESET_N
R3F56
ESPI_RESET_N_SH
R5H30
ESPI_RST_EC_R_N
ESPI_RST_HDR_N
R5H29
ESPI_RST_AIC_N
ESPI_IO_3
R3F53
ESPI_IO_3_R
R5V2
ESPI_IO_3_SH
R5H1
ESPI_IO3_EC_R
R5H2
ESPI_IO3_HDR
R5V1
ESPI_IO3_AIC
ESPI_IO_2
R3F51
ESPI_IO_2_R
R5V4
ESPI_IO_2_SH
R5H3
ESPI_IO2_EC_R
R5H4
ESPI_IO2_HDR
R5V5
ESPI_IO2_AIC
ESPI_IO_1
R3F44
ESPI_IO_1_R
R5V7
ESPI_IO_1_SH
R5H7
ESPI_IO1_EC_R
R5H8
ESPI_IO1_HDR
R5V8
ESPI_IO1_AIC
ESPI_IO_0
R3F52
ESPI_IO_0_R
ESPI_IO_0_SH
R5H9
ESPI_IO0_EC_R
R5H10
ESPI_IO0_HDR
R5V12
ESPI_IO0_AIC
SPI_MOSI_SW
R3G76
SPI_MOSI_TPM
R3G74
SPI0_MOSI_R
R3G72
SPI0_MOSI_IO_0_MECC_FET
R3G77
SPI_MOSI_TPM_TTK
A93549-008
EMPTY
CHIP
RA
RB


Stuff this component
Unstuff this component
170 IN SPI_MISO_SW
A93549-008 R3G82 75 0402 5% CHIP SPI_MISO_TPM OUT 172
A93549-008 R3G81 75 0402 5% CHIP SPI0_MISO_R OUT 171
A93549-008 R3G83 75 0402 5% EMPTY SPI0_MISO_IO_1_MECC_FET OUT 176
R3G84 75 0402 5% CHIP A93549-008 SPI_MISO_TPM_TTK OUT 290
170 IN SPI_CLK_SW
A93549-008 R3U29 75 0402 5% CHIP SPI0_CLK_R OUT 171
A93549-008 R3G86 75 0402 5% CHIP SPI_CLK_TPM OUT 172
A93549-008 R3G85 75 0402 5% EMPTY SPI0_CLK_MECC_FET OUT 176
A93549-008 R3U30 75 0402 5% CHIP SPI_CLK_TPM_TTK OUT 290
176 IN SPI_CS0_SW_N
R3U34 0 0402 5% CHIP SPI_CS0_R_N OUT 290 171 172
R3G89 0 0402 5% EMPTY SPI0_CS0_MECC_FET_N OUT 176
Stuff this component
Unstuff this component
179 OUT GPPC_C8_TCH_PAD_INT_N_ECAIC
R4G1 0 0402 5% EMPTY
MODULE NAME REV
UART0 SHARING OPTIONS
23 IN GPPC_C8_UART0_RXD
R4G5 0 0402 5% CHIP GPPC_C8_TCH_PAD_INT_N IN 130
CAD NOTE: 3 PAD
R4G8 0 0402 5% EMPTY UART0_RXD_SV_HDR IN 210
45 IN SUS_CLK
A93549-005 R3F111 33 0402 5% CHIP M.2_BTWIFI_SUS_CLK OUT 147
R3F108 1K 1% EMPTY 0402
R3F113 33 0402 5% EMPTY SUS_CLK_EC_R OUT 45
R3F112 33 0402 5% EMPTY SUS_CLK_CODEC OUT 168
45 IN SUS_CLK_EC_R
R6H35 1/16W 5% 0402 CHIP SUS_CLK_R OUT 173
CAD NOTE: 3-PAD SHARING
R6H36 1/16W 0402 EMPTY SUS_CLK_ECAIC OUT 179


Stuff this component
Unstuff this component
R6V21
GPPC_C23_WIFI_WAKE_N
OUT
147
192
23
IN
GPPC_C23_UART2_CTS_N
R6V26
BUF_CTS_N
OUT
194
290
0
0402
5%
EMPTY
CAD NOTE:
3-PAD
179
IN
ECAIC_BUF_CTS_N
R6V27
R6H37
MECC_PCH_INT_OD_N
IN
178
R6V16
GPPC_C22_WLAN_RST_N
OUT
41
192
23
OUT
GPPC_C22_UART2_RTS_N
R6V19
BUF_RTS_N
IN
194
290
179
31
OUT
ISH_UART0_ECAIC_TXD
R6V22
Stuff this component
Unstuff this component
R5U17
SMC_RST_N
OUT
174
212
0 5%
EMPTY0402
R5U20
SMC_RST_ECAIC_N
OUT
178
173
IN
EC_SPI_CLK
R6H21
EC_SPI_CLK_R
OUT
170
CAD NOTE:
4 PAD
R6H20
EC_SPI_CLK_FLASH
OUT
177
R6H19
EC_SPI_CLK_AIC
OUT
179


Stuff this component
Unstuff this component
173 IN EC_SPI_MOSI
R6H12 0402 CHIP
EC_SPI_MOSI_R OUT 170
CAD NOTE:
4 PAD
R6H14 0402 EMPTY
EC_SPI_MOSI_FLASH OUT 177
R6H13 0402 EMPTY
EC_SPI_MOSI_AIC OUT 179
173 IN EC_SPI_MISO
R5H25 0402 CHIP
EC_SPI_MISO_R OUT 170
CAD NOTE:
4 PAD
R5H24 0402 EMPTY
EC_SPI_MISO_FLASH OUT 177
R5H26 0402 EMPTY
EC_SPI_MISO_AIC OUT 179
173 IN EC_SPI_CS0_N
R5H39 0402 EMPTY RA
EC_SPI_CS0_R_N OUT 176
CAD NOTE:
4 PAD RA RB RC
R5H36 0402 EMPTY RB
EC_SPI_CS0_FLASH_N OUT 177
R5H38 0402 CHIP
PM_RSMRST_N OUT 50 70 187
R5H37 0402 EMPTY RC
EC_SPI_CS0_AIC_N OUT 179
Stuff this component
Unstuff this component
179 IN I2C0_SCL_TCH_PAD_ECAIC
R9T27 0402 EMPTY
I2C0_SCL_TCH_PAD 28 130
179 IN I2C0_SDA_TCH_PAD_ECAIC
R9T28 0402 EMPTY
I2C0_SDA_TCH_PAD 28 130
23 IN GPPC_D14_ISH_UART0_TXD_SML0BCLK
R4G71 0402 EMPTY
ISH_UART0_TXD_SML0BCLK_SV_HDR OUT 210
CAD NOTE:
4 PAD
R4G70 0402 EMPTY
ISH_UART0_ECAIC_TXD OUT 179 192
R4G72 0402 EMPTY
SML0B_CLK OUT 25 108 174
23 IN GPPC_D13_ISH_UART0_RXD_SML0BDATA
R4G60 0402 1K EMPTY
FLASH_DES_SEC_OVERRIDE OUT 288
R4G56 0402 EMPTY
ISH_UART0_RXD_SML0BDATA_SV_HDR OUT 210
R4G62 0402 EMPTY
ISH_UART0_ECAIC_RXD OUT 179
R4G55 0402 EMPTY
SML0B_DATA OUT 25 108 174

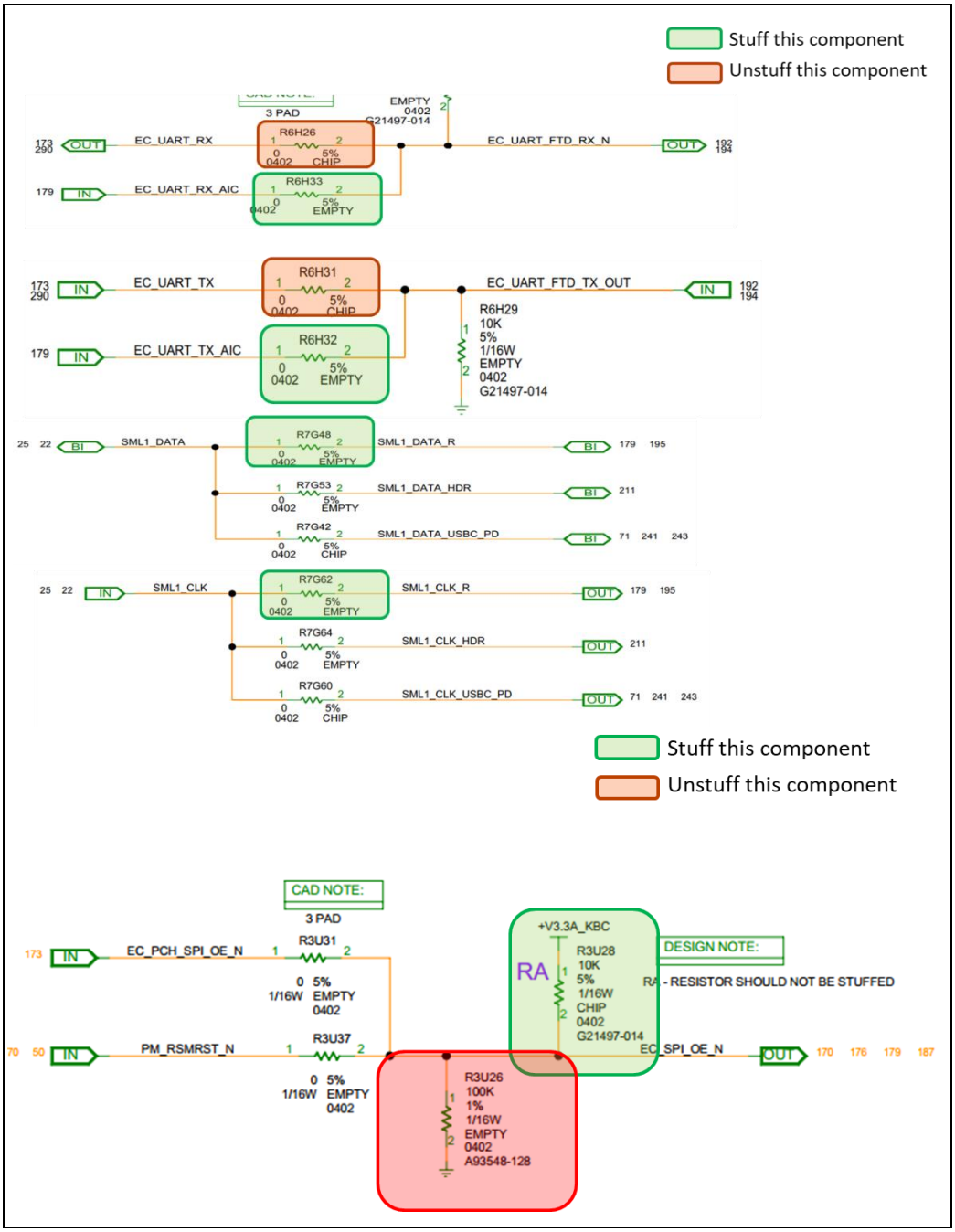
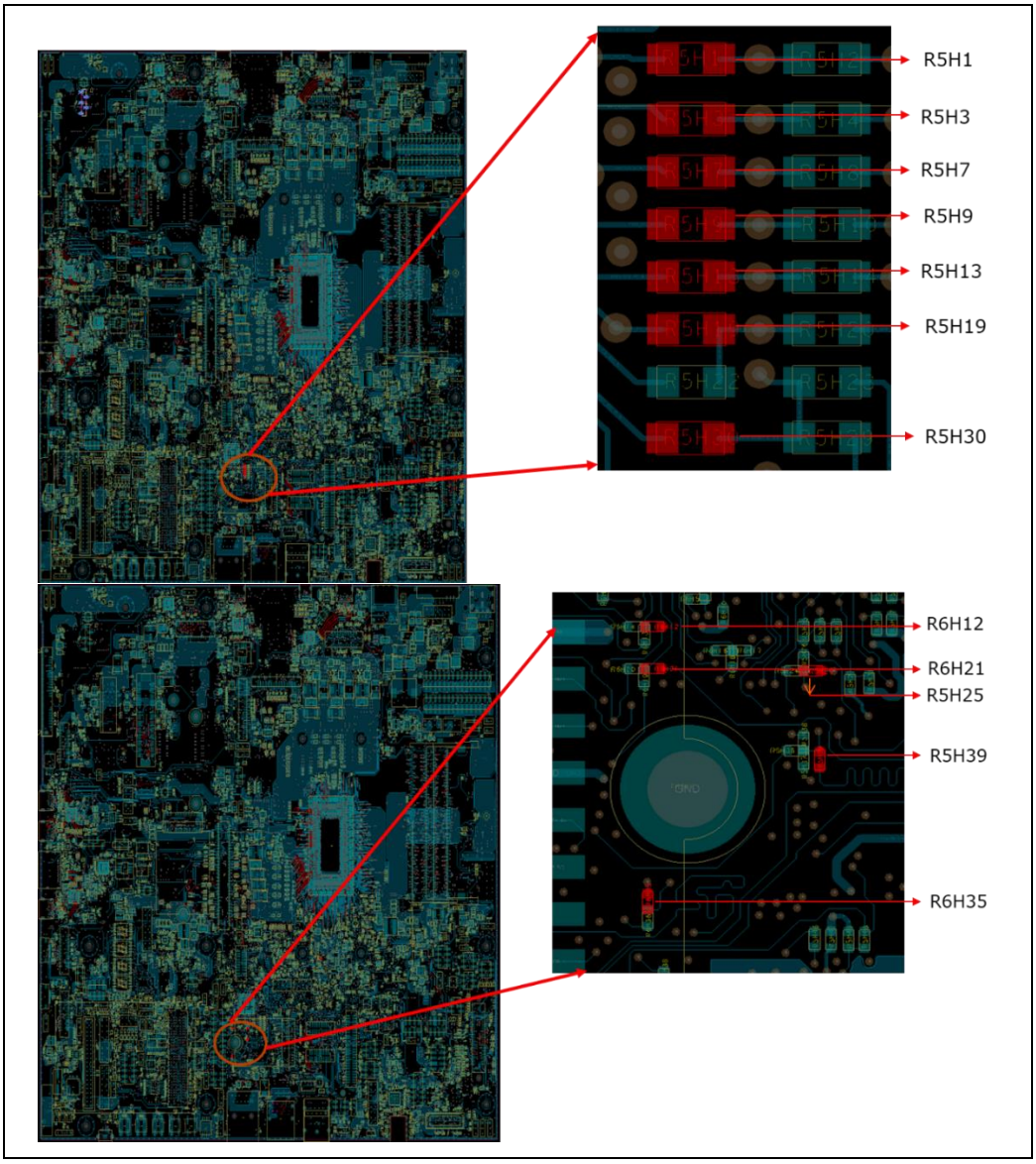
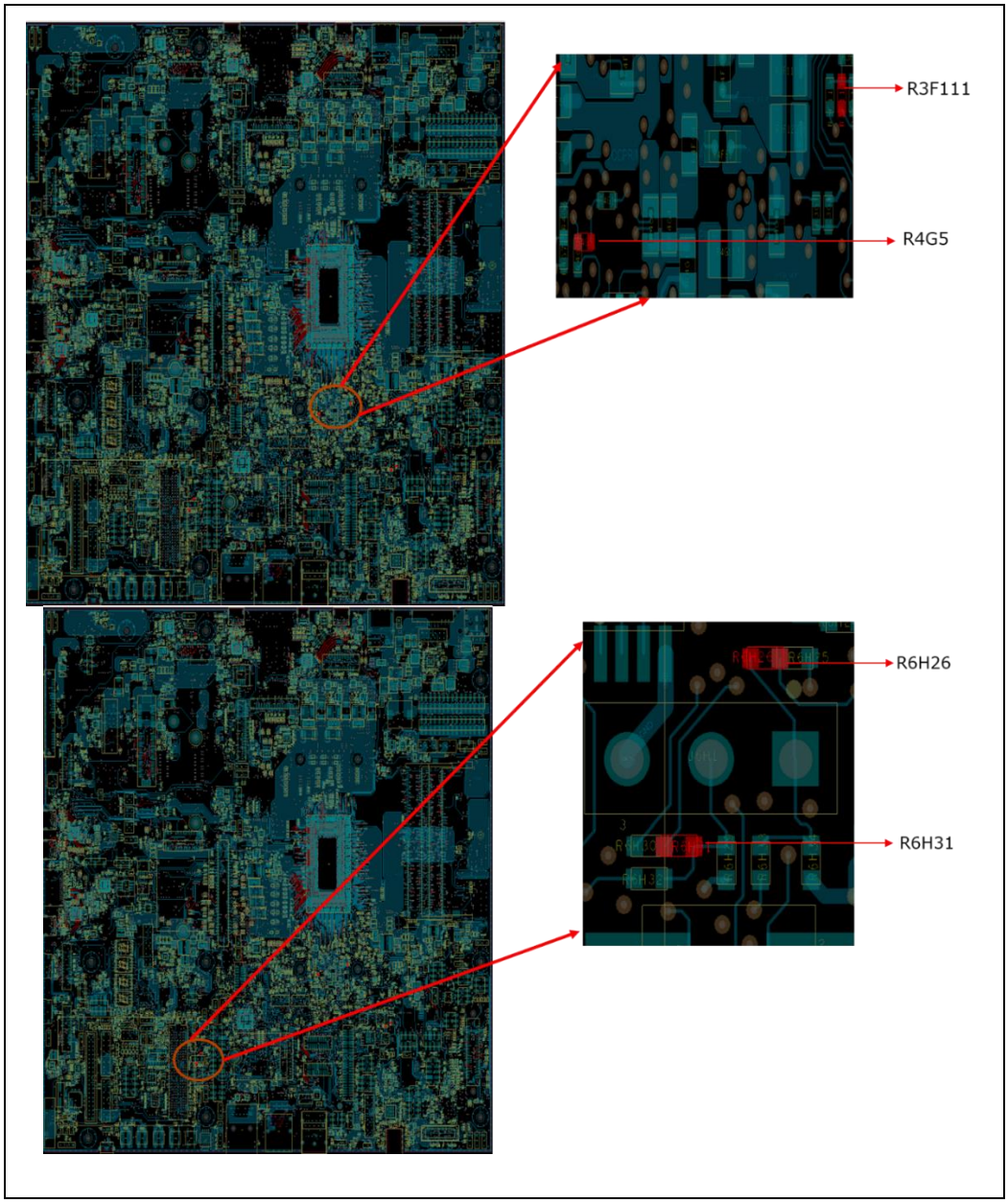
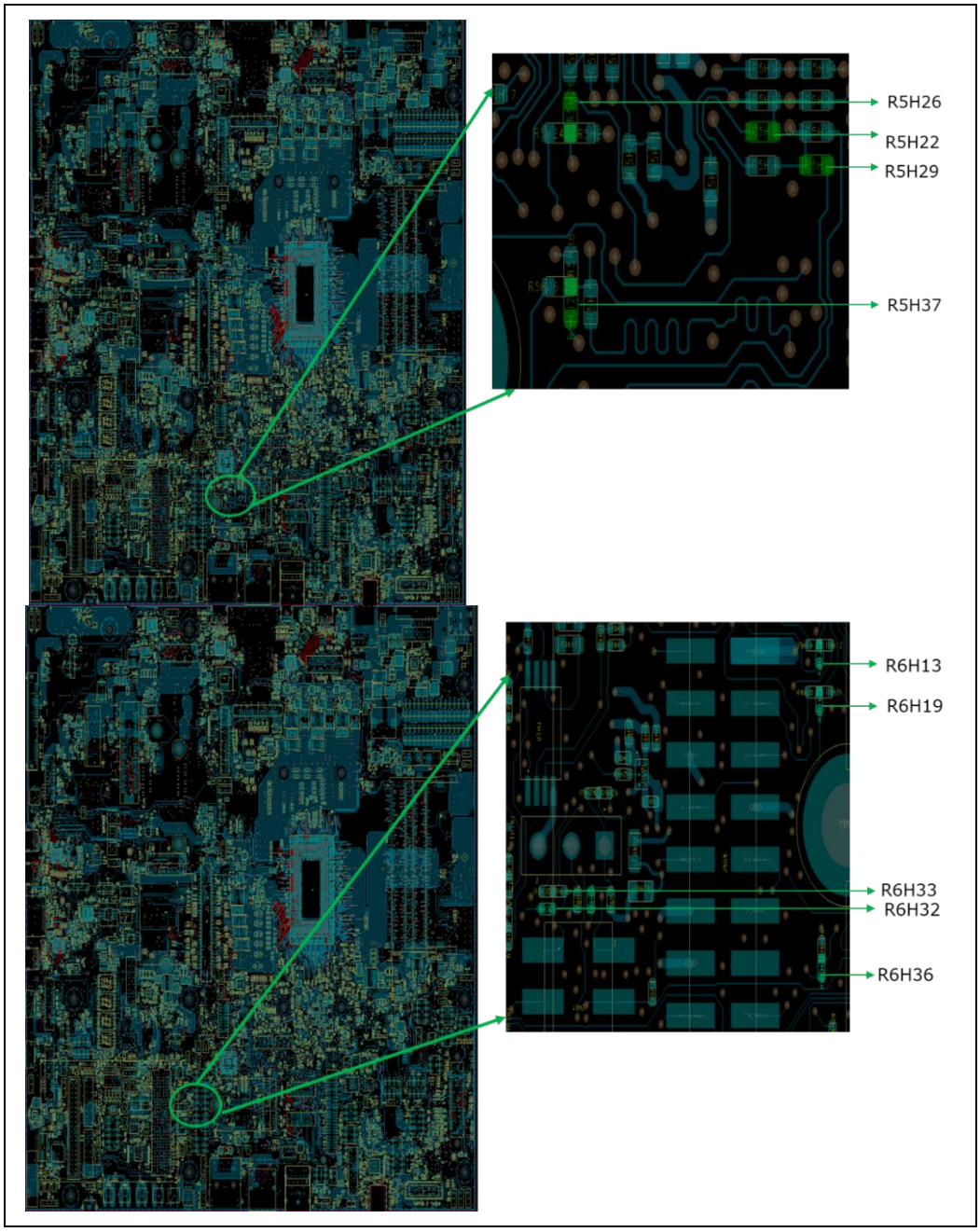

Stuff this component
Unstuff this component
3 PAD
EMPTY
0402
G21497-014
R6H26
0
5%
0402
CHIP
EC_UART_RX
EC_UART_FTD_RX_N
R6H33
EC_UART_RX_AIC
EMPTY
R6H31
EC_UART_TX
EC_UART_FTD_TX_OUT
R6H29
10K
5%
1/16W
EMPTY
0402
G21497-014
R6H32
EC_UART_TX_AIC
R7G48
SML1_DATA
SML1_DATA_R
R7G53
SML1_DATA_HDR
R7G42
SML1_DATA_USBC_PD
R7G62
SML1_CLK
SML1_CLK_R
R7G64
SML1_CLK_HDR
R7G60
SML1_CLK_USBC_PD
Stuff this component
Unstuff this component
CAD NOTE:
3 PAD
R3U31
EC_PCH_SPI_OE_N
0 5%
1/16W EMPTY
0402
R3U37
PM_RSMRST_N
+V3.3A_KBC
RA
R3U28
10K
5%
1/16W
CHIP
0402
G21497-014
DESIGN NOTE:
RA - RESISTOR SHOULD NOT BE STUFFED
EC_SPI_OE_N
R3U26
100K
1%
1/16W
EMPTY
0402
A93548-128

Figure 3-93. Layout Snapshot (Top Layer)




R3F111
R4G5
R6H26
R6H31


R5H26
R5H22
R5H29
R5H37
R6H13
R6H19
R6H33
R6H32
R6H36

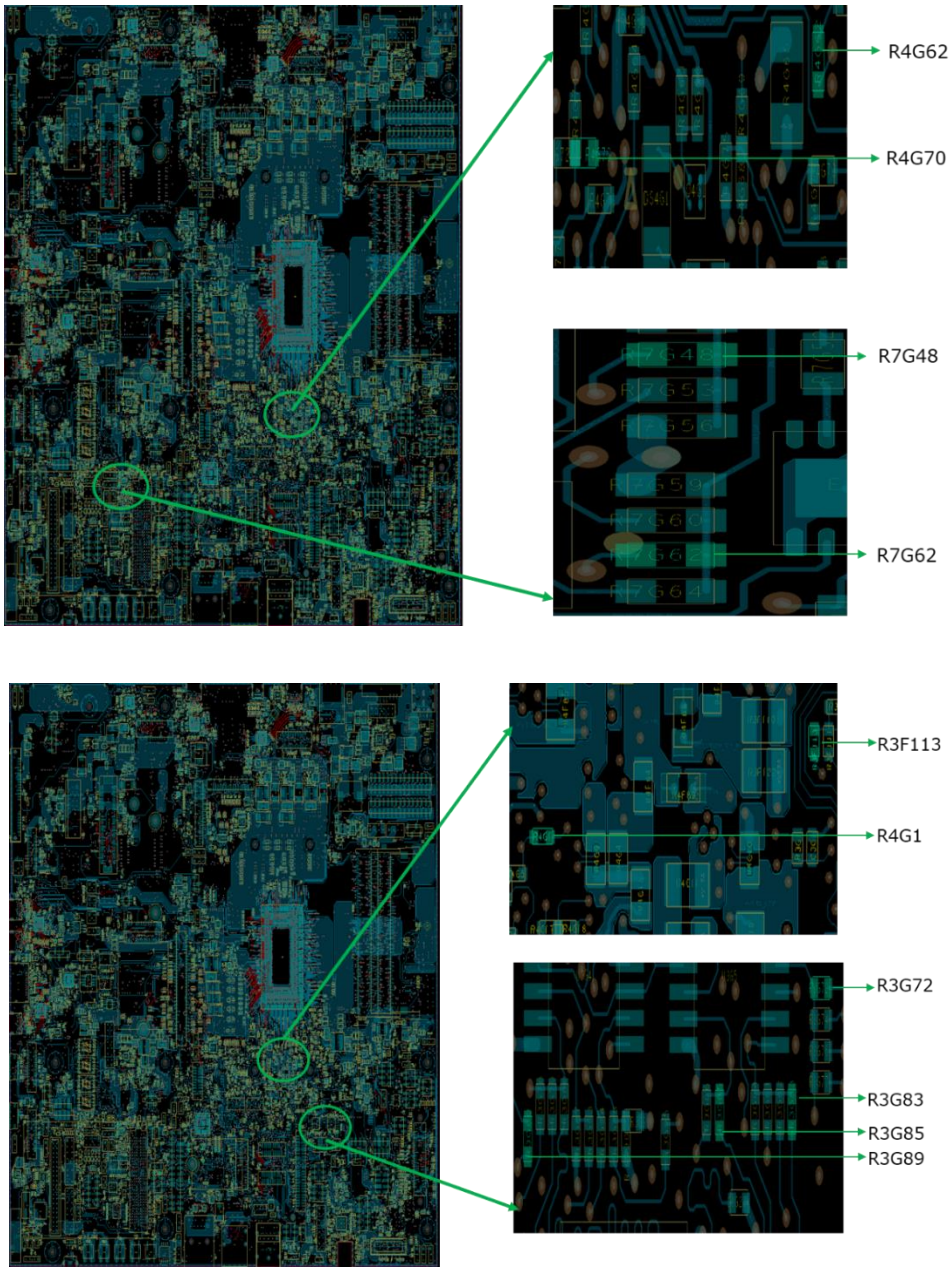
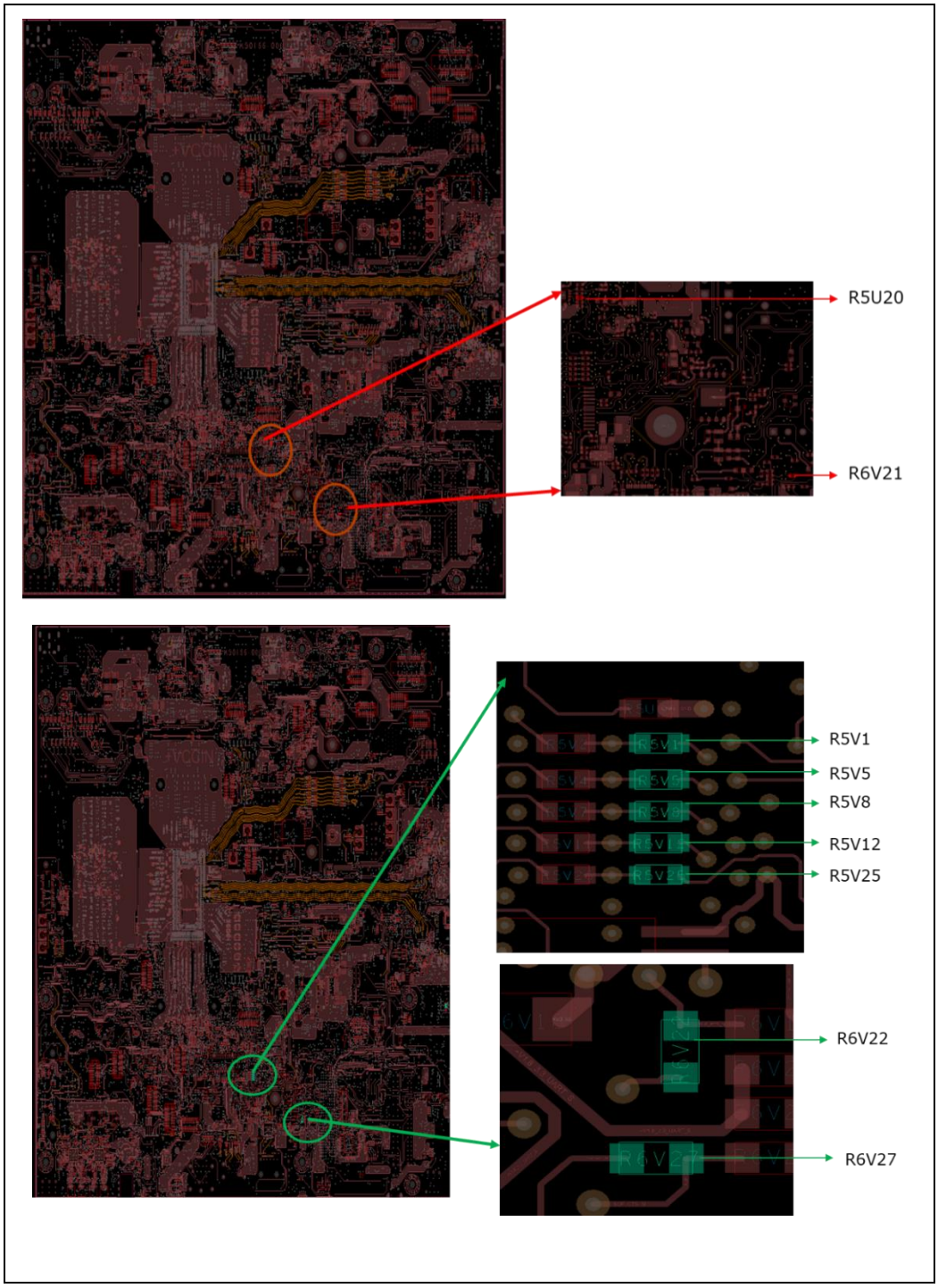
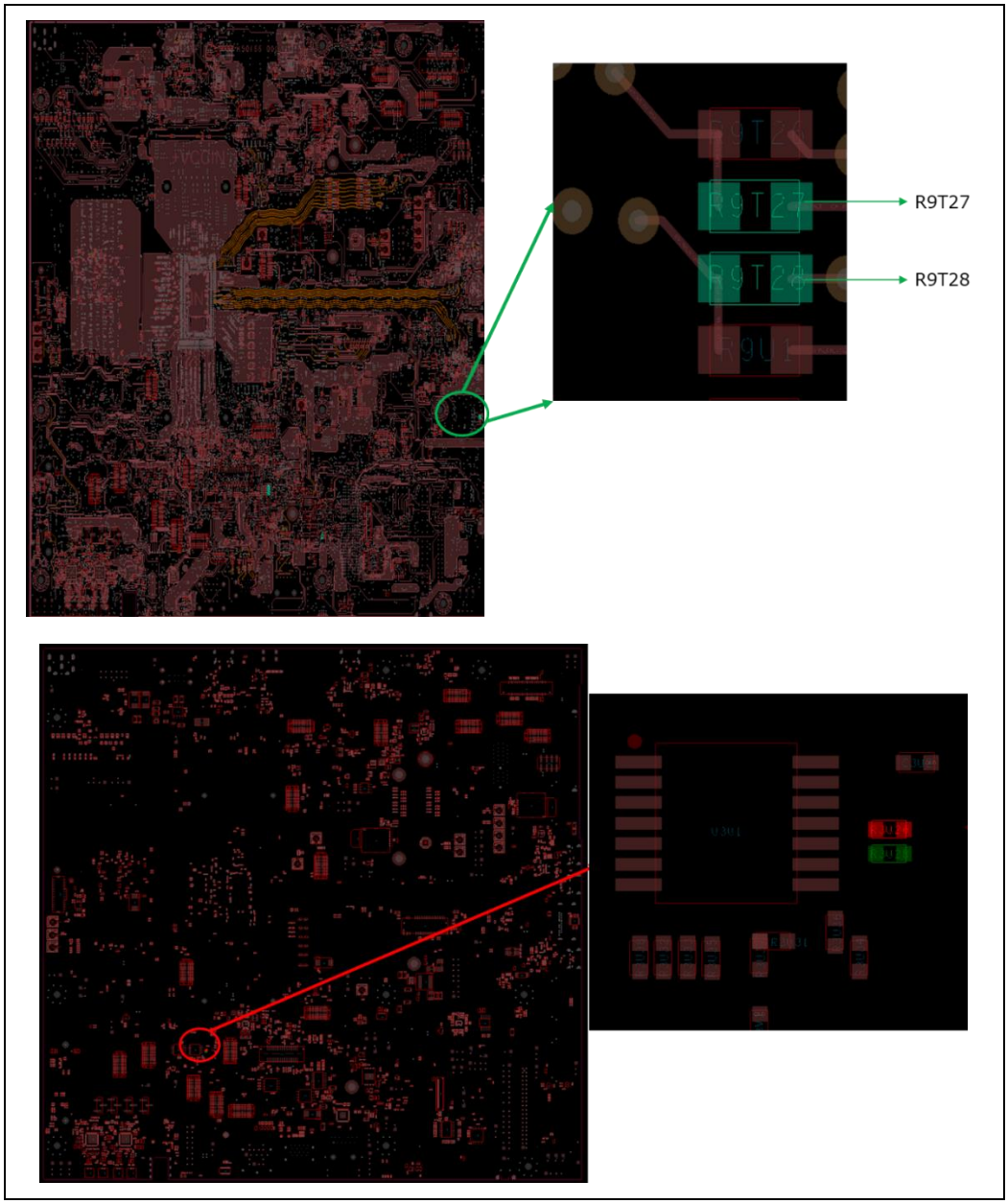

R4G62
R4G70
R7G48
R7G62
R3F113
R4G1
R3G72
R3G83
R3G85
R3G89

Figure 3-94. Layout Snapshot (Bottom Layer)





3.2.26 Rework for Vmin Active Protection (VAP) Enable Function and Improve PROCHOT Drive Strength

Description: Rework for Vmin Active Protection enable function and improve PROCHOT drive strength

Impact if not done: No impact.

Rework Details: SMD Resistor and Diode rework

Applicable To: TGL UP3 DDR4, TGL UP3 LPDDR4x, and TGL UP3 LPDDR5.

WO# Applicable for this Rework: IPTL191101, IPTL191301 IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501 IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTY193102, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL19210, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTY201701, IPTL201901, IPTL192901, IPTL203003

Table 3-48. Rework Details: TGL UP3 DDR4

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace OR disconnect CR1A1.2	Diode	CR1A1	IC, DS, DIO, SOT323, BAT54CWT1G, SHTKY	IC, DS, DIO, SOT323, BAT54W -7-F,SHTKY,
Replace	Resistor	R9U4	RES D,0402,20.00 kOHM,5.00%,1/16W	RES D,0402,147.00 kOHM,1.00%,1/16W, YES
Replace	Resistor	R2L3	RES D,0402,100.00 kOHM,5.00%,1/16W	RES D,0402,10.00 kOHM,1.00%,1/16W, YES

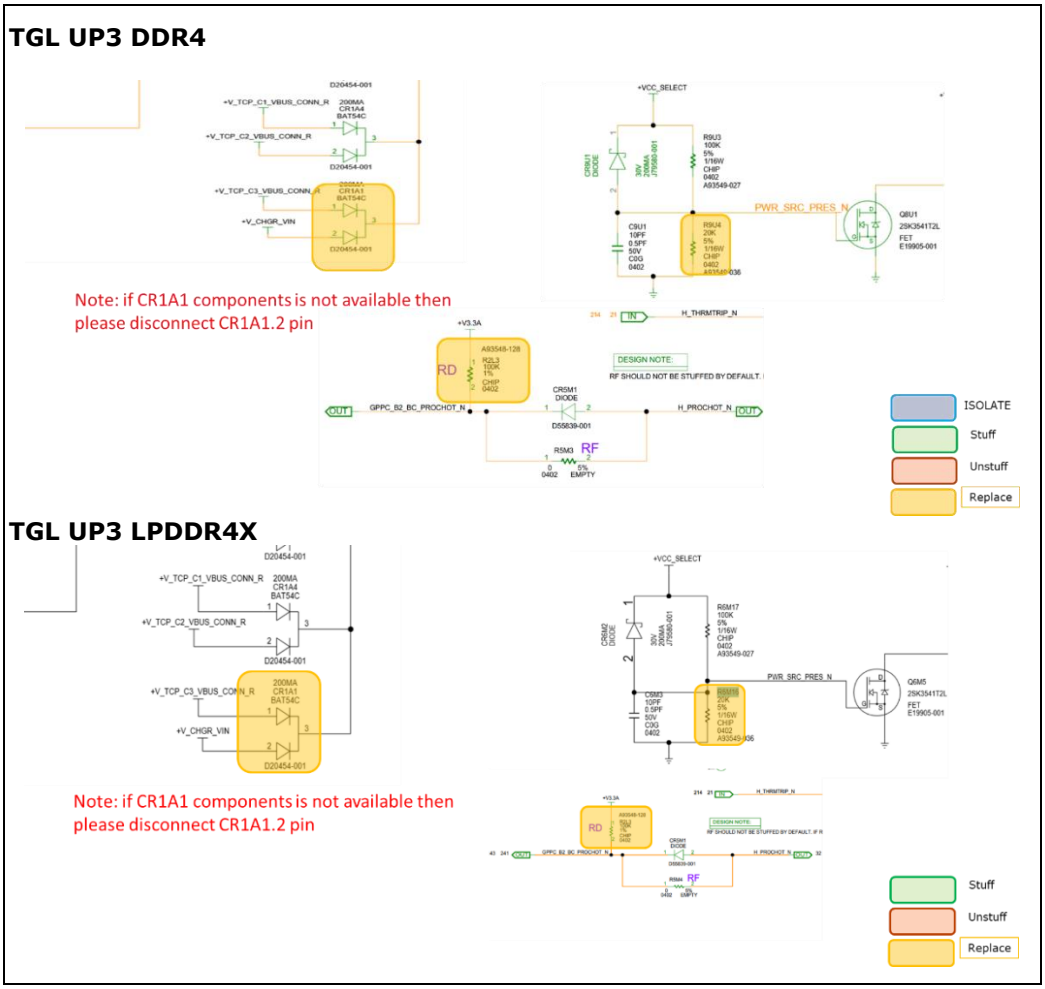
Table 3-49. Rework Details: TGL UP3 LPDDR4X

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace OR disconnect CR1A1.2	Diode	CR1A1	IC, DS, DIO, SOT323, BAT54CWT1G, SHTKY	IC, DS, DIO, SOT323, BAT54W -7-F, SHTKY,
Replace	Resistor	R6M16	RES D,0402,20.00 kOHM,5.00%,1/16W	RES D,0402,147.00 kOHM,1.00%,1/16W ,YES
Replace	Resistor	R2L3	RES D,0402,100.00 kOHM,5.00%,1/16W	RES D,0402,10.00 kOHM,1.00%,1/16W ,YES

Table 3-50. Rework Details: TGL UP3 LPDDR5

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace OR disconnect CR1A1.2	Diode	CR1A1	IC, DS, DIO, SOT323, BAT54CWT1G, SHTKY	IC, DS, DIO, SOT323, BAT54W - 7-F, SHTKY,
Replace	Resistor	R6M17	RES D,0402,20.00 kOHM,5.00%,1/16 W	RES D,0402,147.00 kOHM,1.00%,1/16W ,YES
Replace	Resistor	R2L3	RES D,0402,100.00 kOHM,5.00%,1/16W	RES D,0402,10.00 kOHM,1.00%,1/16W ,YES

Figure 3-95. Schematic Snapshot



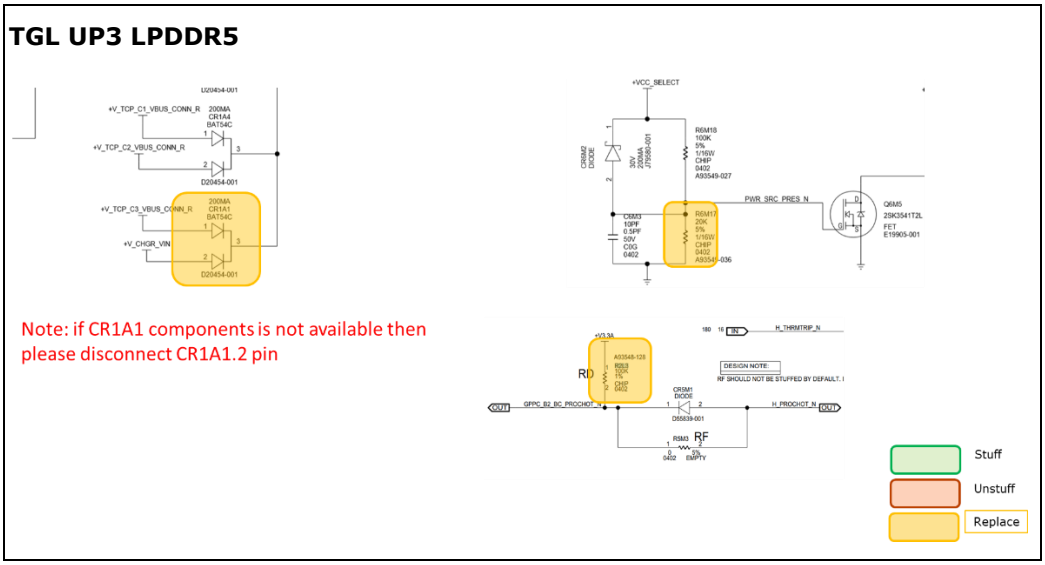
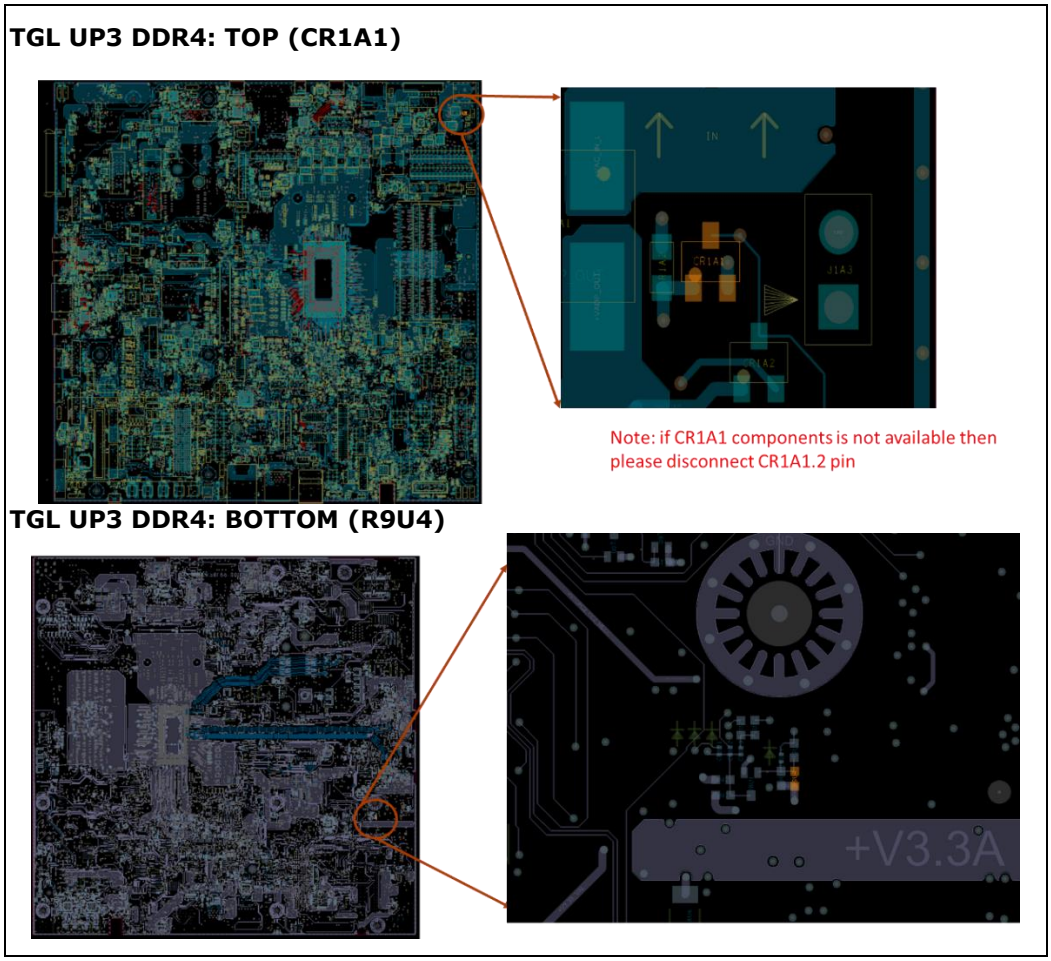
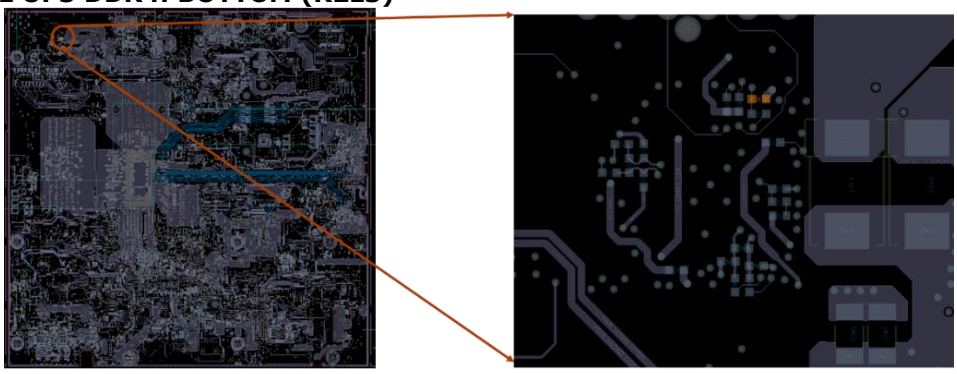


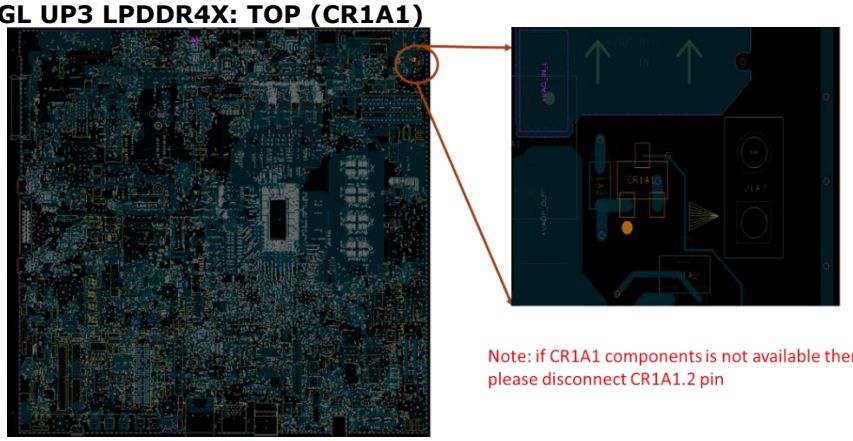
Figure 3-96. Layout Snapshot



TGL UP3 DDR4: BOTTOM (R2L3)

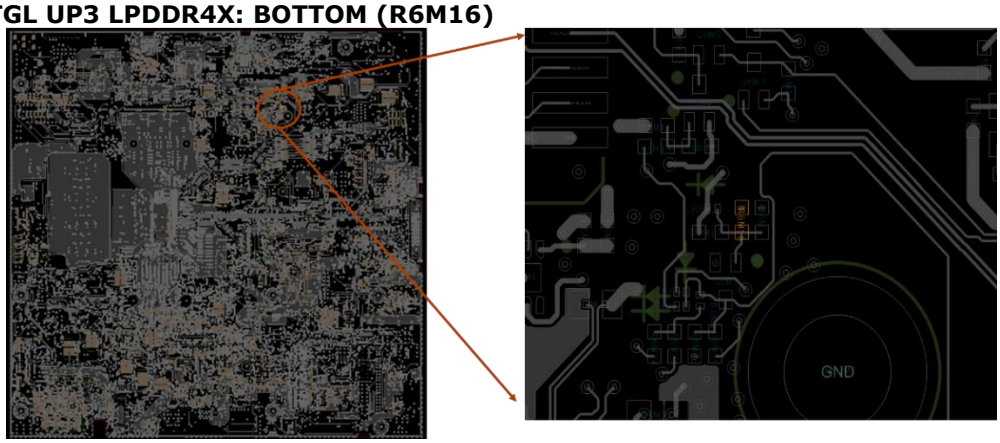


TGL UP3 LPDDR4X: TOP (CR1A1)

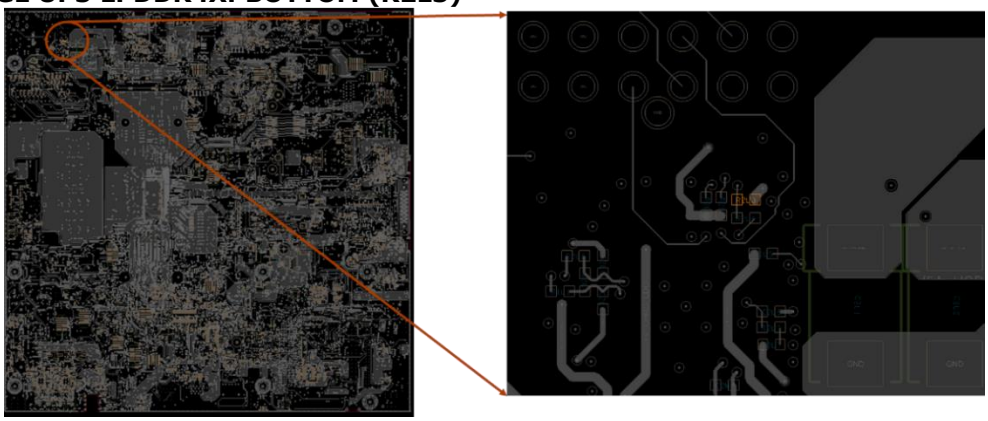


Note: if CR1A1 components is not available then please disconnect CR1A1.2 pin

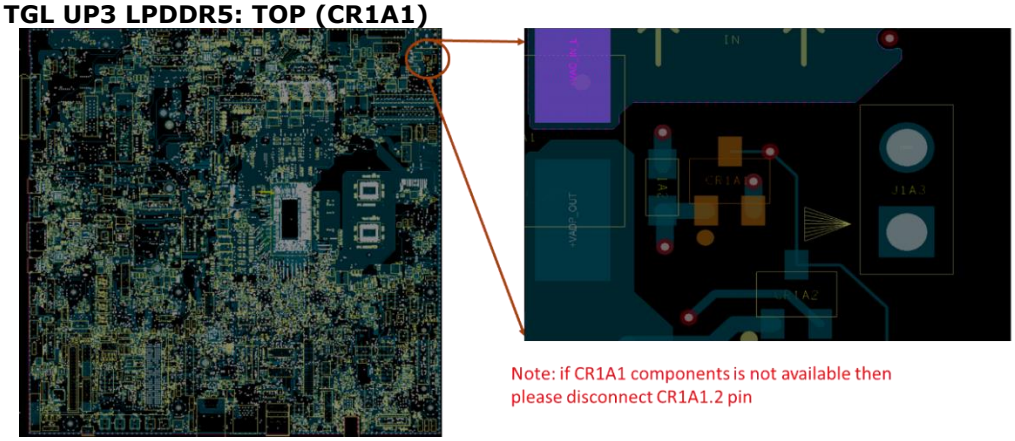
TGL UP3 LPDDR4X: BOTTOM (R6M16)



TGL UP3 LPDDR4X: BOTTOM (R2L3)

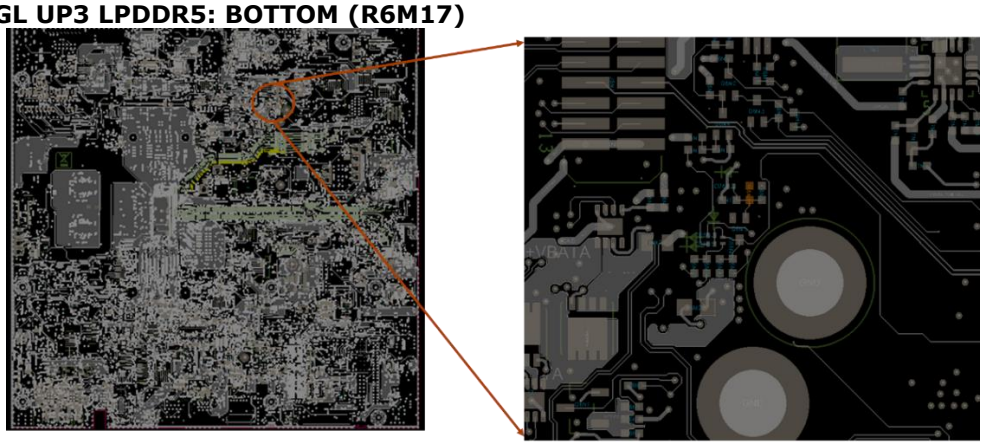


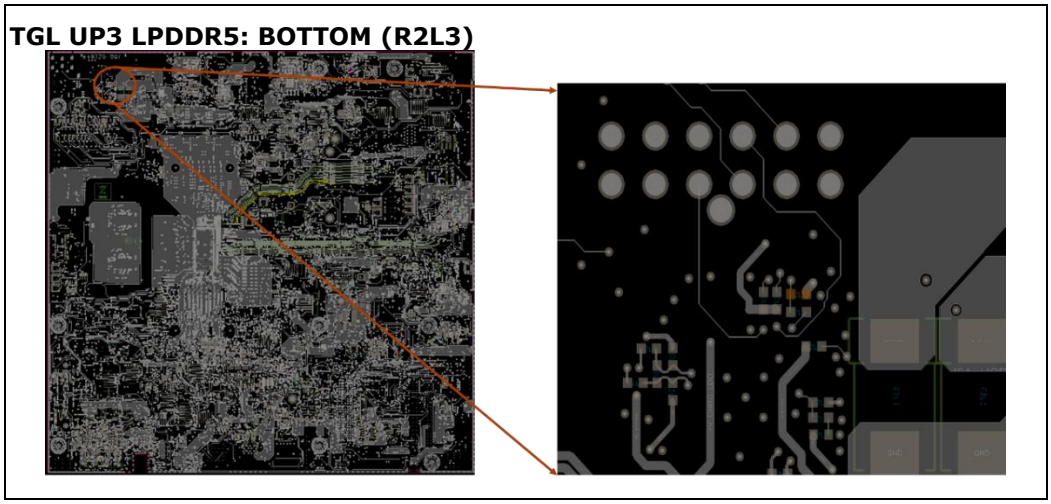
TGL UP3 LPDDR5: TOP (CR1A1)



Note: if CR1A1 components is not available then please disconnect CR1A1.2 pin

TGL UP3 LPDDR5: BOTTOM (R6M17)





3.2.27 Rework to Enable Foxville card on TGL UP3

Description: Present pin mapping change according to latest Foxville guidelines to avoid enumeration issues.

Impact if done: No impact

Rework Details: SMD Resistor and SMD Diode rework.

Applicable To: TGL UP3 DDR4

WO# Applicable for this Rework: IPTY19180, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603 IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL201201, IPTL194702, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

Table 3-51. Rework Details: TGL UP3 DDR4 RVP

For x4 slot: F11 Required to enable x4 slot

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R7B13	N/A	RES D,0402,0 OHM,5.00%,1/16W
Un-stuff	Resistor	R7M15	RES D,0402,0 OHM,5.00%,1/16W	N/A

For x1 slot:

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R8C10	N/A	RES D,0402,0 OHM,5.00%,1/16W
Un-stuff	Resistor	R8B2	RES D,0402,0 OHM,5.00%,1/16W	N/A

Table 3-52. Rework Details: TGL UP3 LP4x RVP

For x4 slot: F11 Required to enable x4 slot

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R7B13	N/A	RES D,0402,0 OHM,5.00%,1/16W
Un-stuff	Resistor	R7M15	RES D,0402,0 OHM,5.00%,1/16W	N/A

For x1 slot:

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R8C10	N/A	RES D,0402,0 OHM,5.00%,1/16W
Un-stuff	Resistor	R8B2	RES D,0402,0 OHM,5.00%,1/16W	N/A

Table 3-53. Reference Designator Comparison

Action	TGL UP3 DDR4	TGL UP3 LP4x	TGL UP3 LP5
Stuff	R7B13	R7B13	R7B14
Un-stuff	R7M15	R7M15	R7M16
Stuff	R8C10	R8C10	R8C10
Un-stuff	R8B2	R8B2	R8B2

Figure 3-97. Schematic Snapshot

TGL UP3 DDR4:

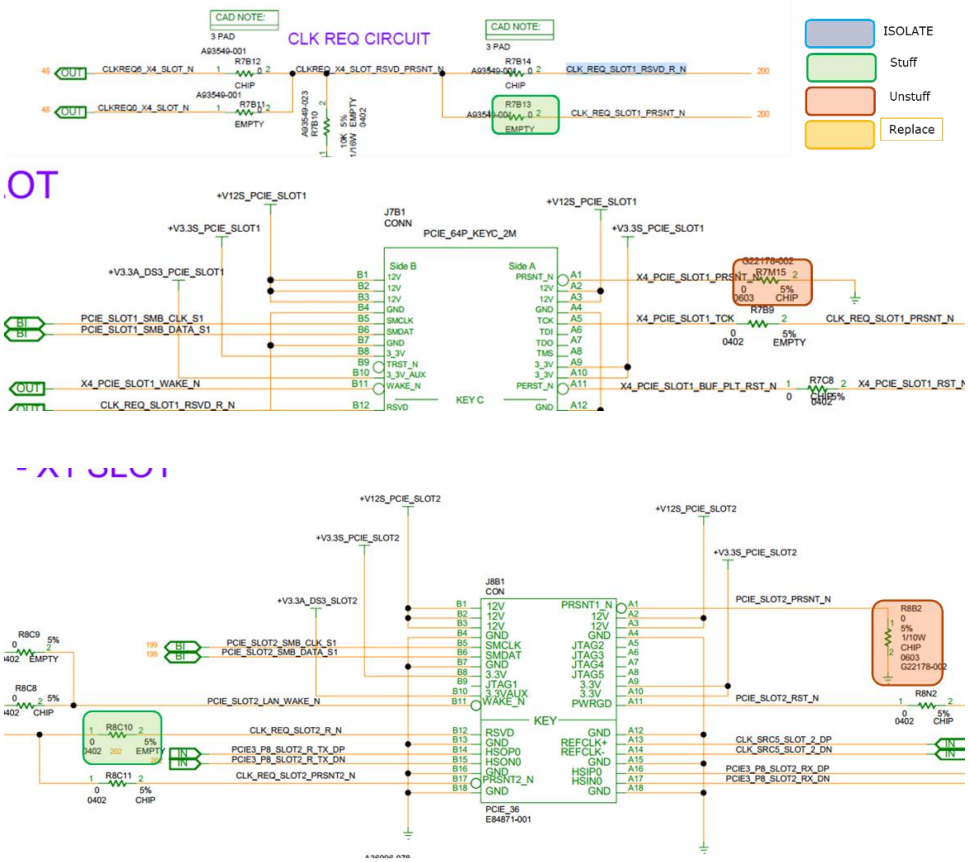


Figure 3-98. Layout Snapshot (Top Layer)

TGL UP3 DDR4 RVP:

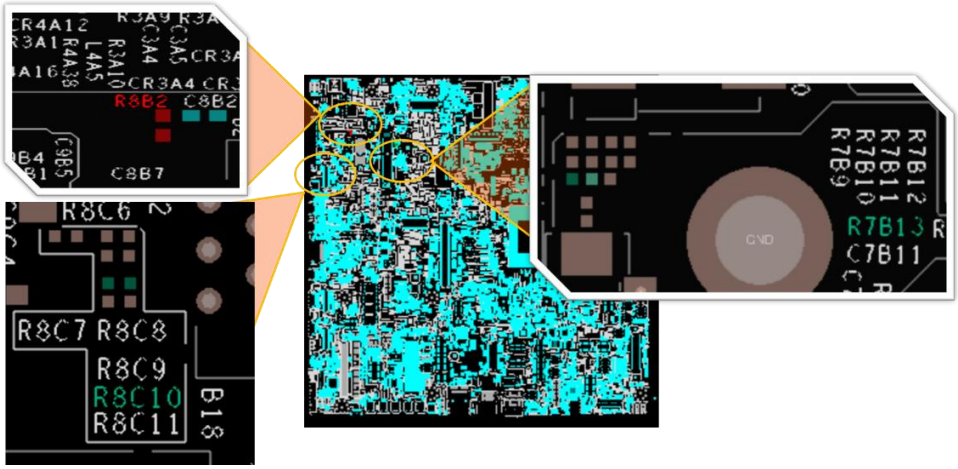
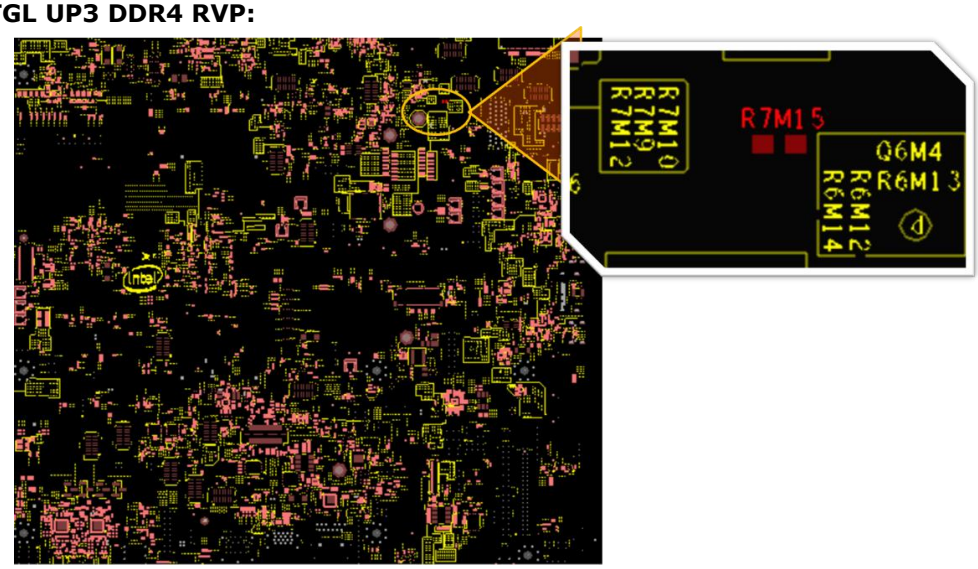


Figure 3-99. Layout Snapshot (Bottom Layer)

TGL UP3 DDR4 RVP:



3.2.28 Rework to Enable Virtual Wire OC Indication to PCH through EC in TGL

Description: This rework is to disconnect physical OC pin to PCH. OC would be driven by EC over eSPI for USBC ports.

Impact: After rework OC will not be asserted to PCH physically. Hence, EC FW with virtual wire support needs to be updated in the system after rework

Rework Details: SMD Resistor and SMD Diode rework.

Applicable To: TGL UP3 RVP SKU

WO# Applicable for this Rework: IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901 IPTL194101, IPTL194202, IPTL194702, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201 IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTY193102, IPTY201701, IPTL201201, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-54. Rework Details: TGL UP3 DDR4 RVP

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Un-stuff	Resistor	R7A3	0, 5%, 1/16W, 0402	N/A
Un-stuff	Resistor	R8E9	0, 5%, 1/16W, 0402	N/A

For VW OC validation through EC, F31 SAF enabling rework needs to be implemented along with this rework.

Table 3-55. Rework Details: TGL UP3 LP4X RVP

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Un-stuff	Resistor	R7A3	0, 5%, 1/16W, 0402	N/A
Un-stuff	Resistor	R8E8	0, 5%, 1/16W, 0402	N/A

Table 3-56. Reference Designator Comparison

Action	TGL UP3 DDR4	TGL UP3 LP4x	TGL UP3 LP5
Un-Stuff	R7A3, R8E9	R7A3, R8E8	R7A3, R8E17

Figure 3-100. Schematic Snapshot

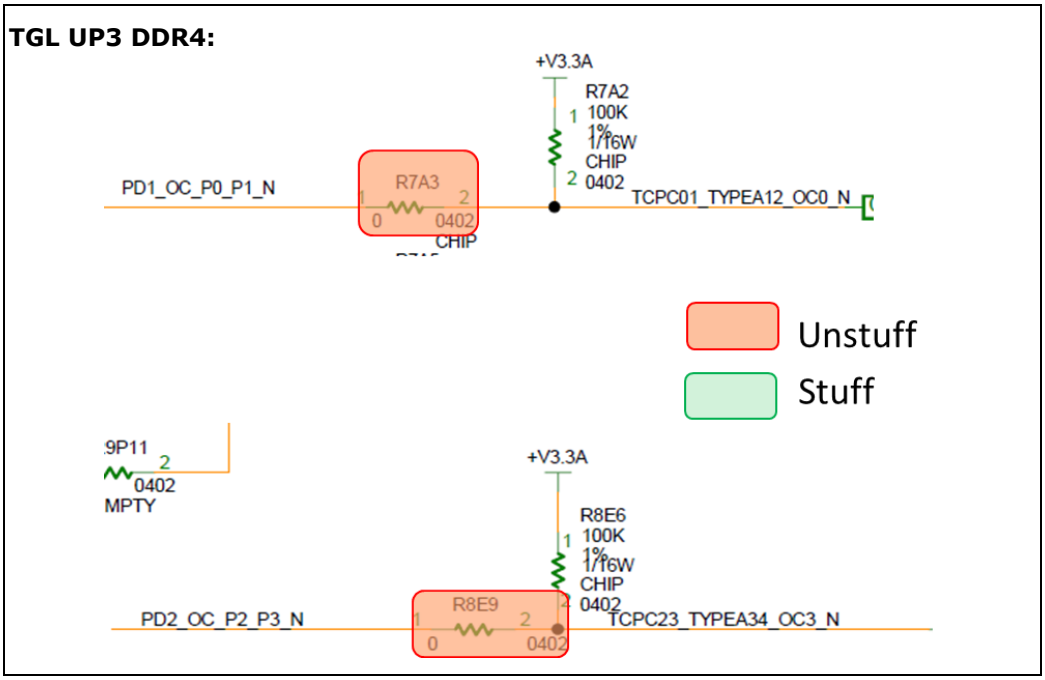


Figure 3-101. Schematic Snapshot

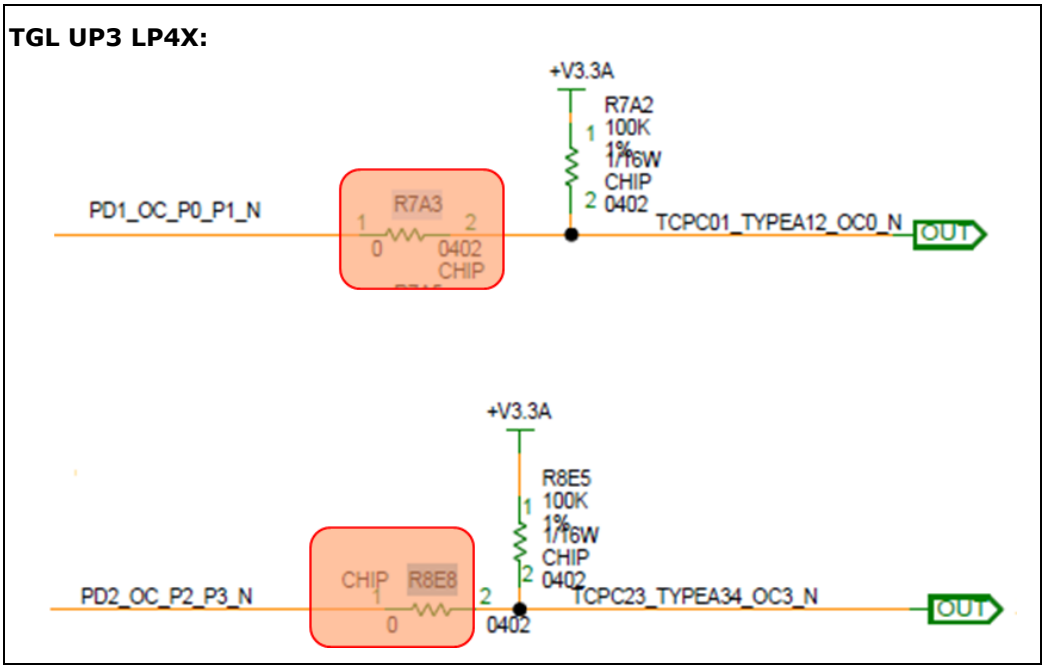


Figure 3-102. Layout Snapshot (Top Layer)

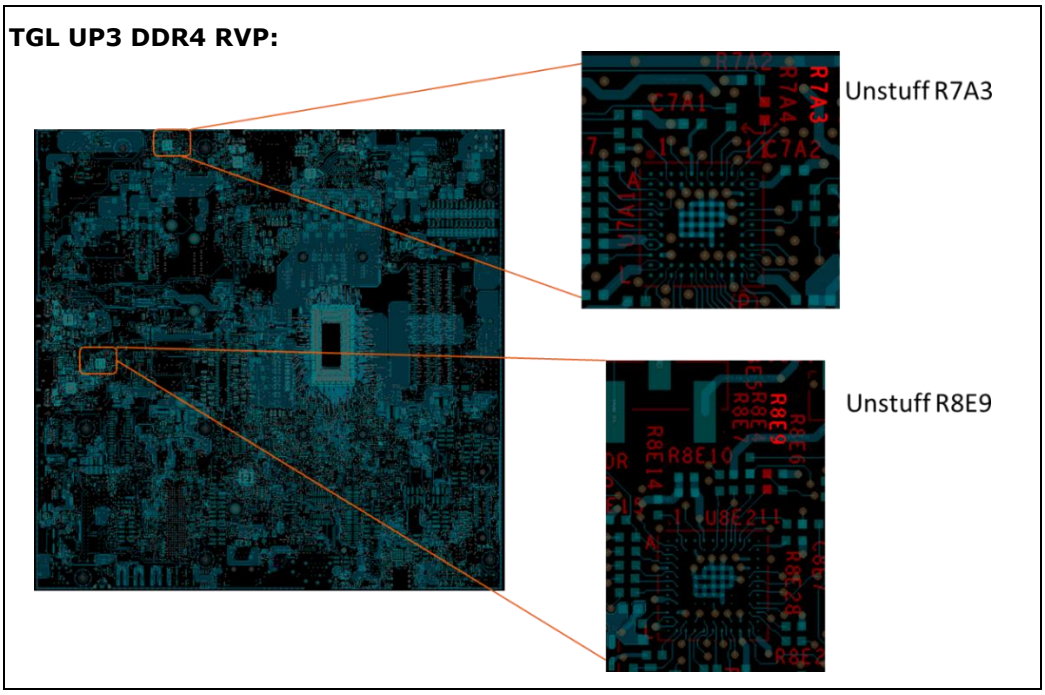
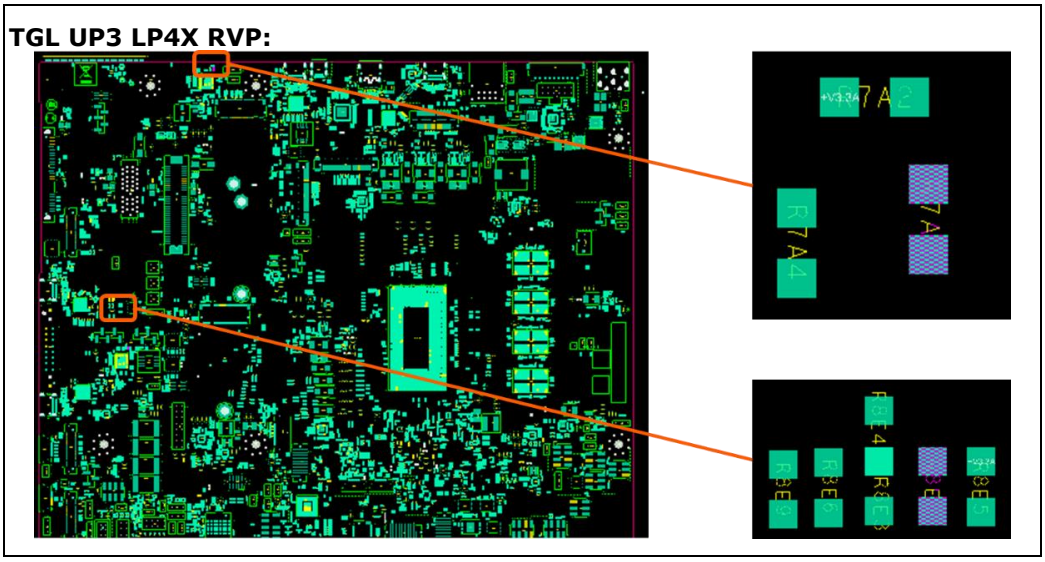


Figure 3-103. Layout Snapshot (Top Layer)



3.2.29 Rework to Enable MIPI Connector on DDIA Combo Port on TGL UP3 LPDDR5

Description: This rework is for enabling MIPI connector on DDIA combo port.

Impact: eDP will not work on DDIA port

Rework Details: SMD resistor/capacitor rework.

Applicable To: TGL UP3 LPDDR5 ERB boards

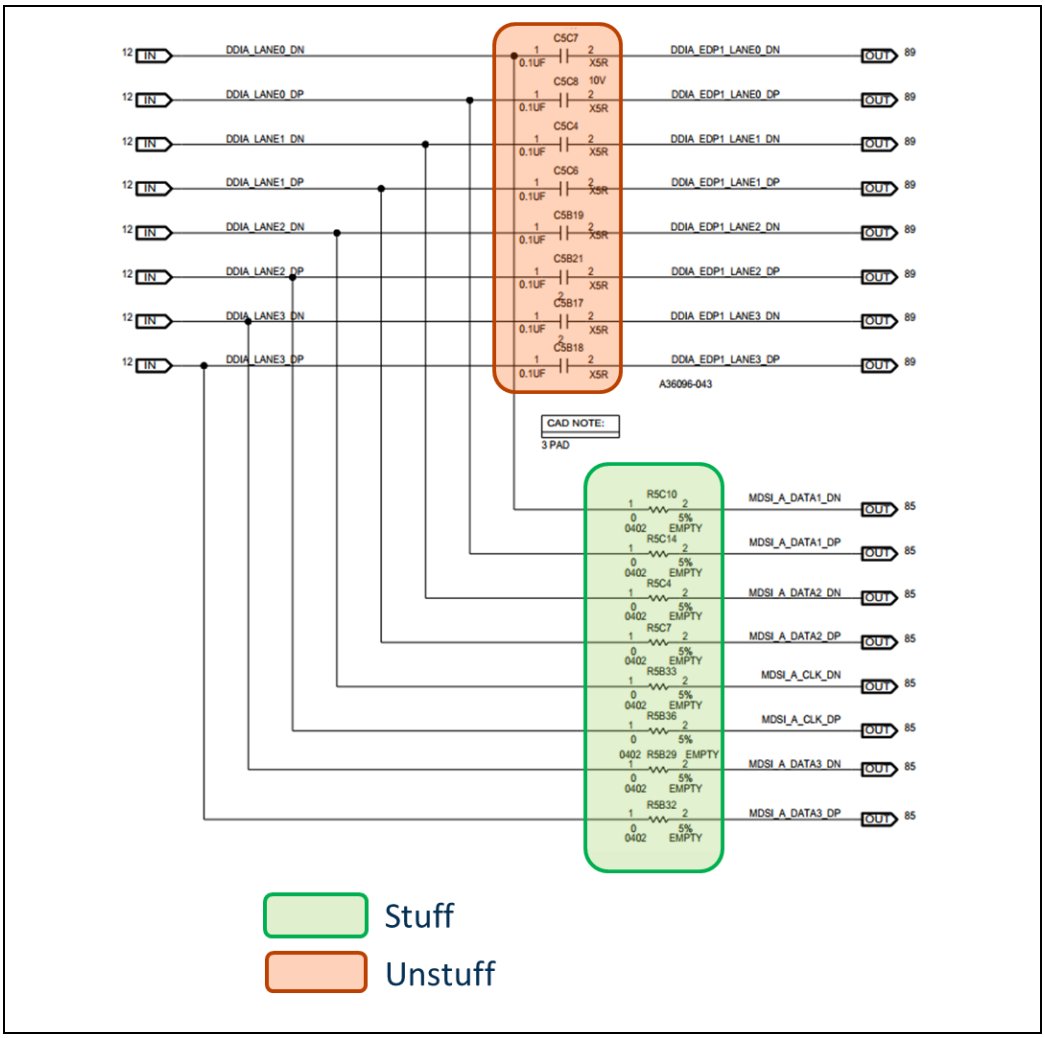
WO# Applicable for this Rework: IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTL203003.

Table 3-57. Rework Details: TGL UP3 LPDDR5 ERB

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Capacitor	C5C7, C5C8, C5C4, C5C6, C5B19, C5B21, C5B17, C5B18, C5C12, C5C10	CAPC,X5R,0402,0.100UF,10.000V,+/- 10%	NA
Stuff	Capacitor	C7C6	NA	CAPC,X5R,0402,0.100UF,10.000V,+/- 10%

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R5C10, R5C14, R5C4, R5C7, R5B33, R5B36, R5B29, R5B32, R6C16, R6C6, R5M7, R5C23, R5C18, R6C5,	NA	RES D,0402,0.00 OHM,5.00%,1/16W
Unstuff	Resistor	R6C2, R6C14, R6C8	RES D,0402,0.00 OHM,5.00%,1/16W	NA
Stuff	Resistor	R7C17	NA	RES D,0402,10.00 kOHM,5.00%,1/16W

Figure 3-104. Schematic Snapshot



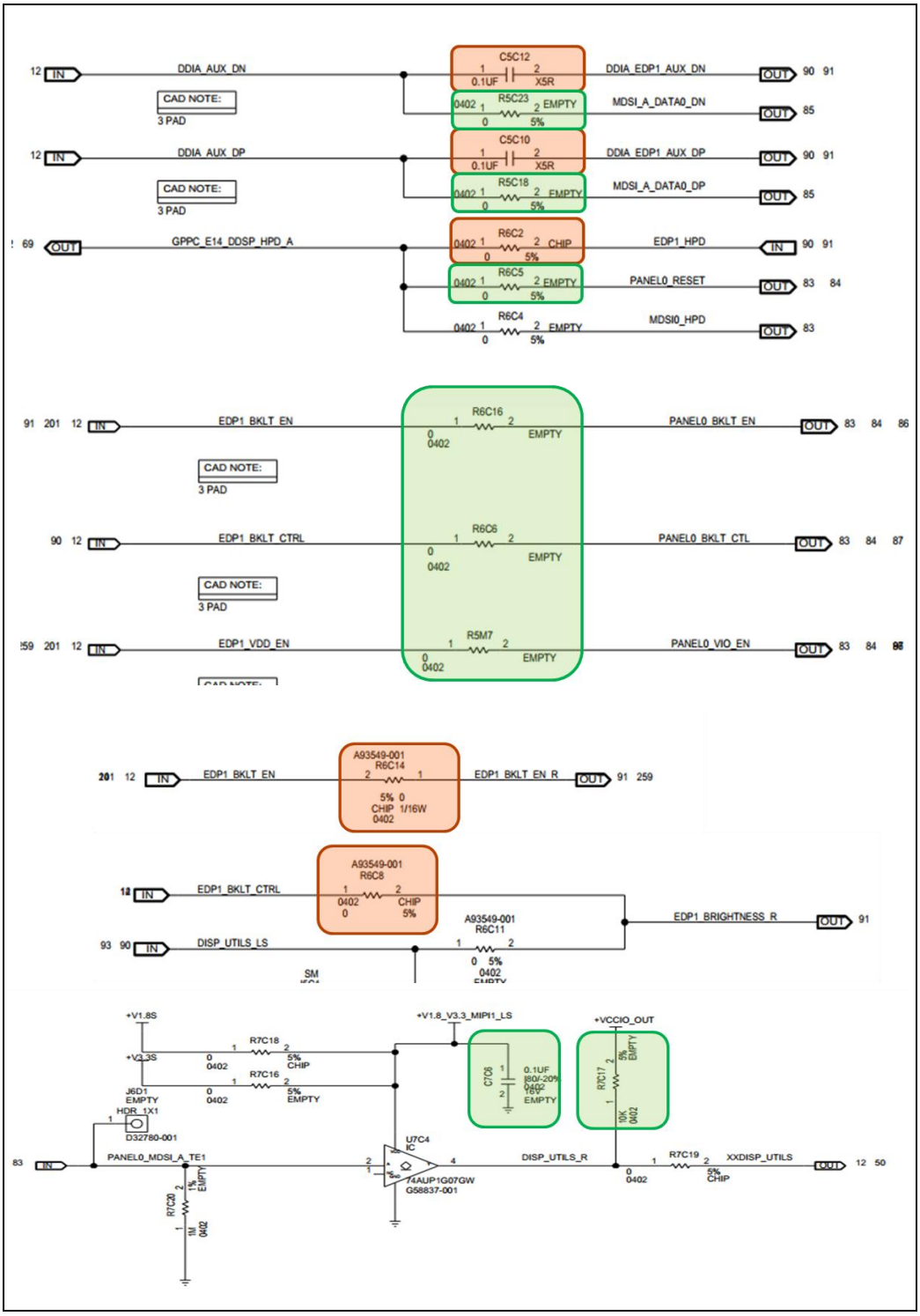

DDIA_AUX_DN
C5C12
0.1UF
X5R
DDIA_EDP1_AUX_DN
CAD NOTE:
3 PAD
R5C23
EMPTY
MDSI_A_DATA0_DN
DDIA_AUX_DP
C5C10
DDIA_EDP1_AUX_DP
R5C18
MDSI_A_DATA0_DP
GPPC_E14_DDSP_HPD_A
R6C2
CHIP
EDP1_HPD
R6C5
PANEL0_RESET
R6C4
MDSI0_HPD
EDP1_BKLT_EN
R6C16
PANEL0_BKLT_EN
EDP1_BKLT_CTRL
R6C6
PANEL0_BKLT_CTL
EDP1_VDD_EN
R5M7
PANEL0_VIO_EN
A93549-001
R6C14
EDP1_BKLT_EN_R
R6C8
R6C11
EDP1_BRIGHTNESS_R
DISP_UTILS_LS
+V1.8S
+V3.3S
R7C18
R7C16
J6D1
HDR_1X1
D32780-001
+V1.8_V3.3_MIPI1_LS
+VCCIO_OUT
C7C6
R7C17
U7C4
IC
74AUP1G07GW
G58837-001
PANEL0_MDSI_A_TE1
R7C20
DISP_UTILS_R
R7C19
XXDISP_UTILS

Figure 3-105. Layout Snapshot (Top Layer)

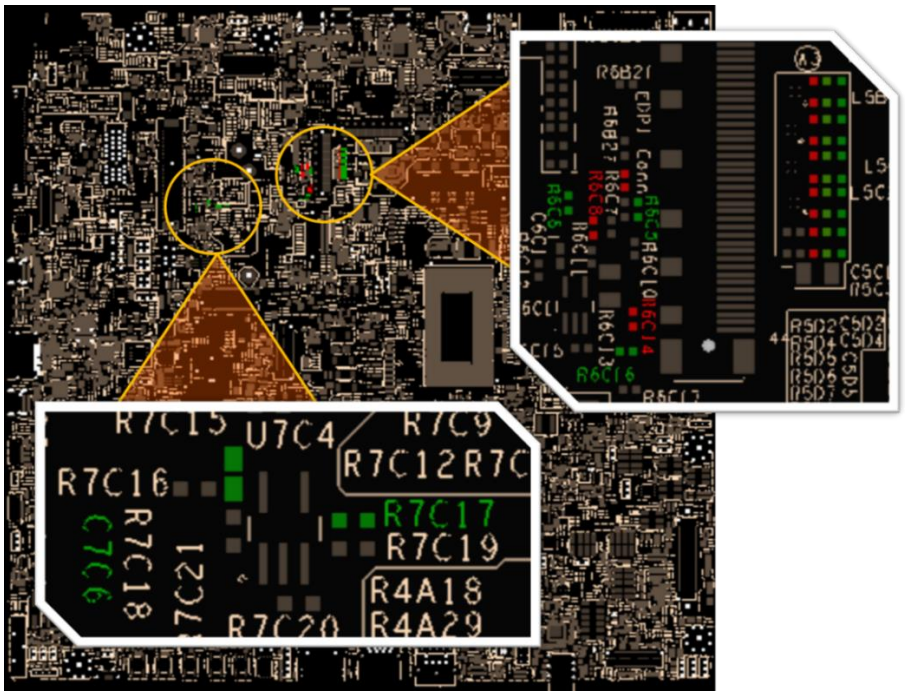
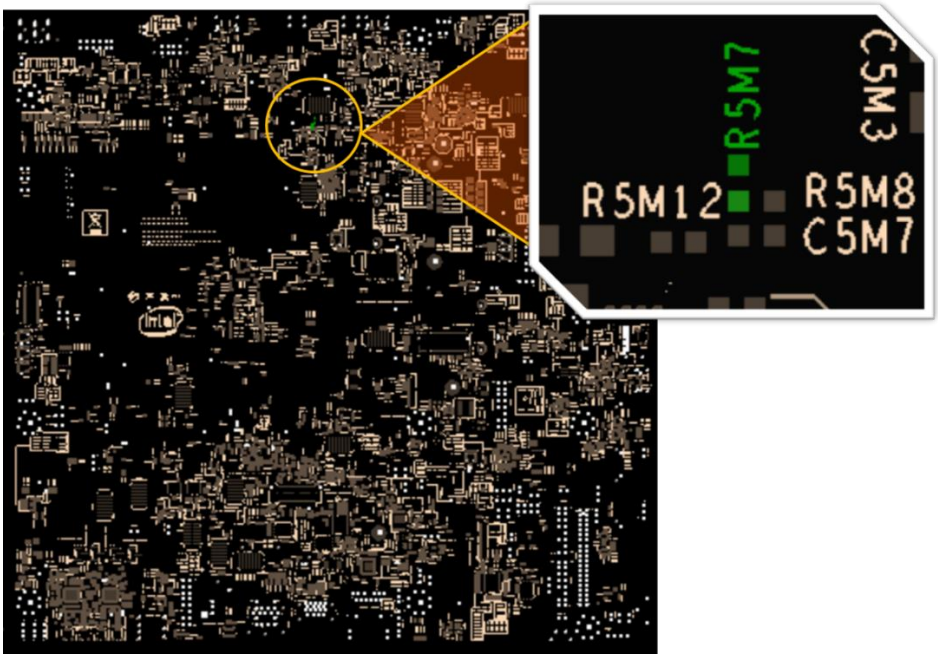


Figure 3-106. Layout Snapshot (Bottom Layer)



3.2.30 Rework to enable_INTRUDER_functionality on TGL_UP3

Description: This rework would enable to test the INTRUDER functionality.

Impact: NA

Rework Details: SMD Resistor rework and stuff jumper.

Applicable To: TGL UP3 RVP SKU

WO# Applicable for this Rework: IPTL184901, IPTL185001 IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402 IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL194702, IPTL201201, IPTL202001, IPTL202201, IPTL202401, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502 IPTL193601, IPTL201901, IPTL202402, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTY200601, IPTY201501, IPTY201901, IPTY201201 IPTY193102, IPTY201701, IPTL192401, IPTL193101, IPTL193301, IPTL193802, IPTY193101, IPTY194101, IPTL195001, IPTY202601IPTL203001, IPTL203002, IPTL203003.

Table 3-58. Rework Details: TGL UP3 DDR4 and LP4 RVP

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Un Stuff	Resistor	R8G15	RES, 0402, 1M, 5%	N/A
Stuff	Resistor	R8G9	N/A	0,0402,5%

Stuff jumper J8G1 1-2 for the INTRUDER functionality

Figure 3-107. Schematic Snapshot

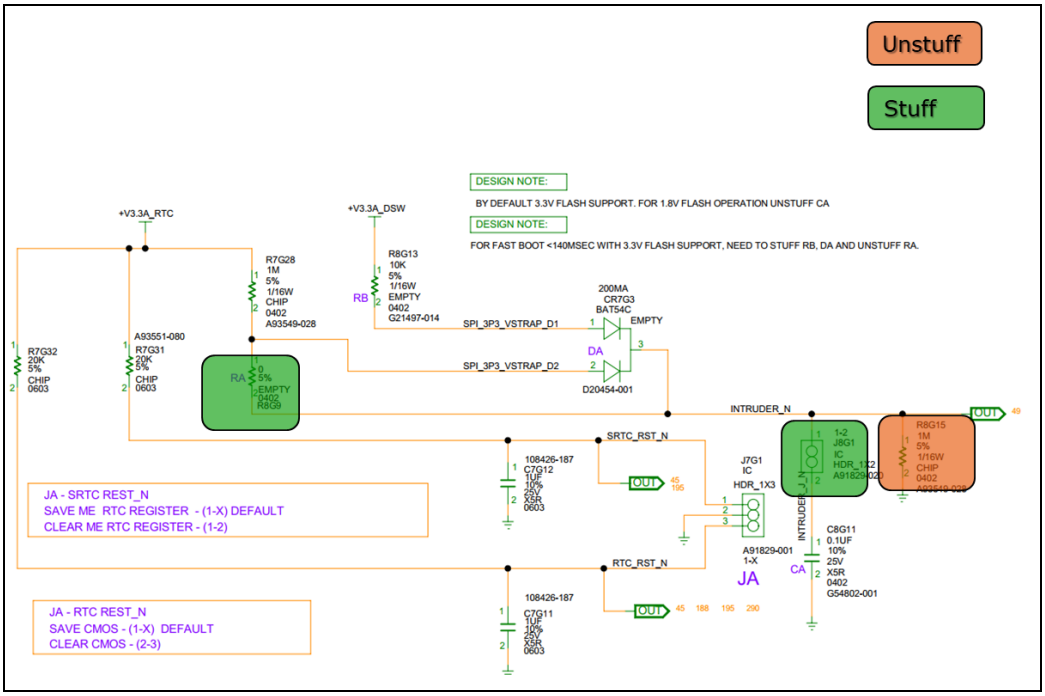


Figure 3-108. Layout Snapshot (Top Layer)

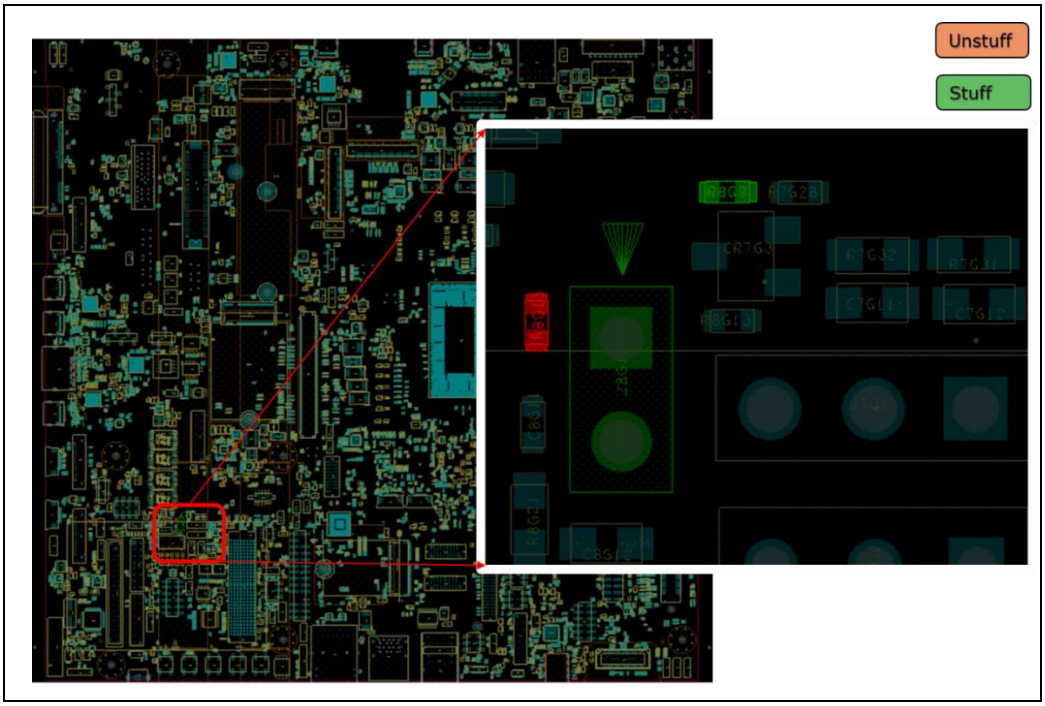
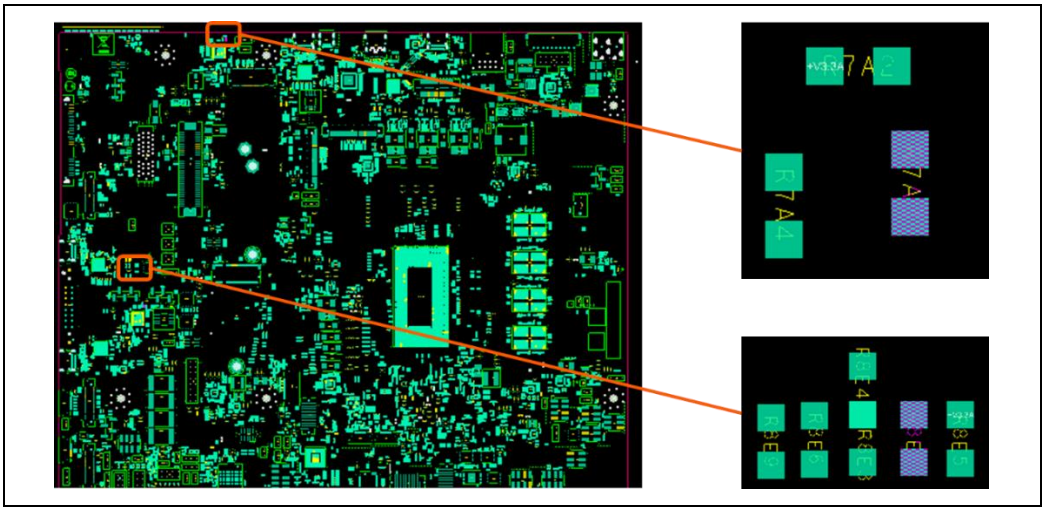


Figure 3-109. Layout Snapshot (Top Layer)



3.2.31 Rework to Enable Mini HDMI on TGL UP3 LP5 Board

Description: Rework instruction to enable mini HDMI port on TGL U LP5.

Impact: By implementing this rework TCP0 port will be disabled.

Rework Details: SMD Resistor rework.

Applicable To: TGL UP3 LP5 RVP

WO# Applicable for this Rework: IPTL203003, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403.

Table 3-59. Rework Details: TGL UP3 LP5 RVP

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Capacitor	C6A33, C6A32, C6A26, C6A27, C6A31, C6A30, C6A29, C6A28	NA	CAP_0402-,X5R,0.1UF,10V,10%,LPDB
Unstuff	Capacitor	C6A21, C6A20, C6A14, C6A15, C6A19, C6A18, C6A17 ,C6A16	CAP_04020.22UF,10V,10%, LPDB, GENERIC	NA

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R5L12, R5L11, R3U2	NA	RES_0402-CHIP,0,5%,1/16W,LPDB,GENERIC
Unstuff	Resistor	R5L15, R5L14	RES_0402,33,5%,1/16 W, LPDB, GENERIC	NA

Figure 3-110. Schematic Snapshot

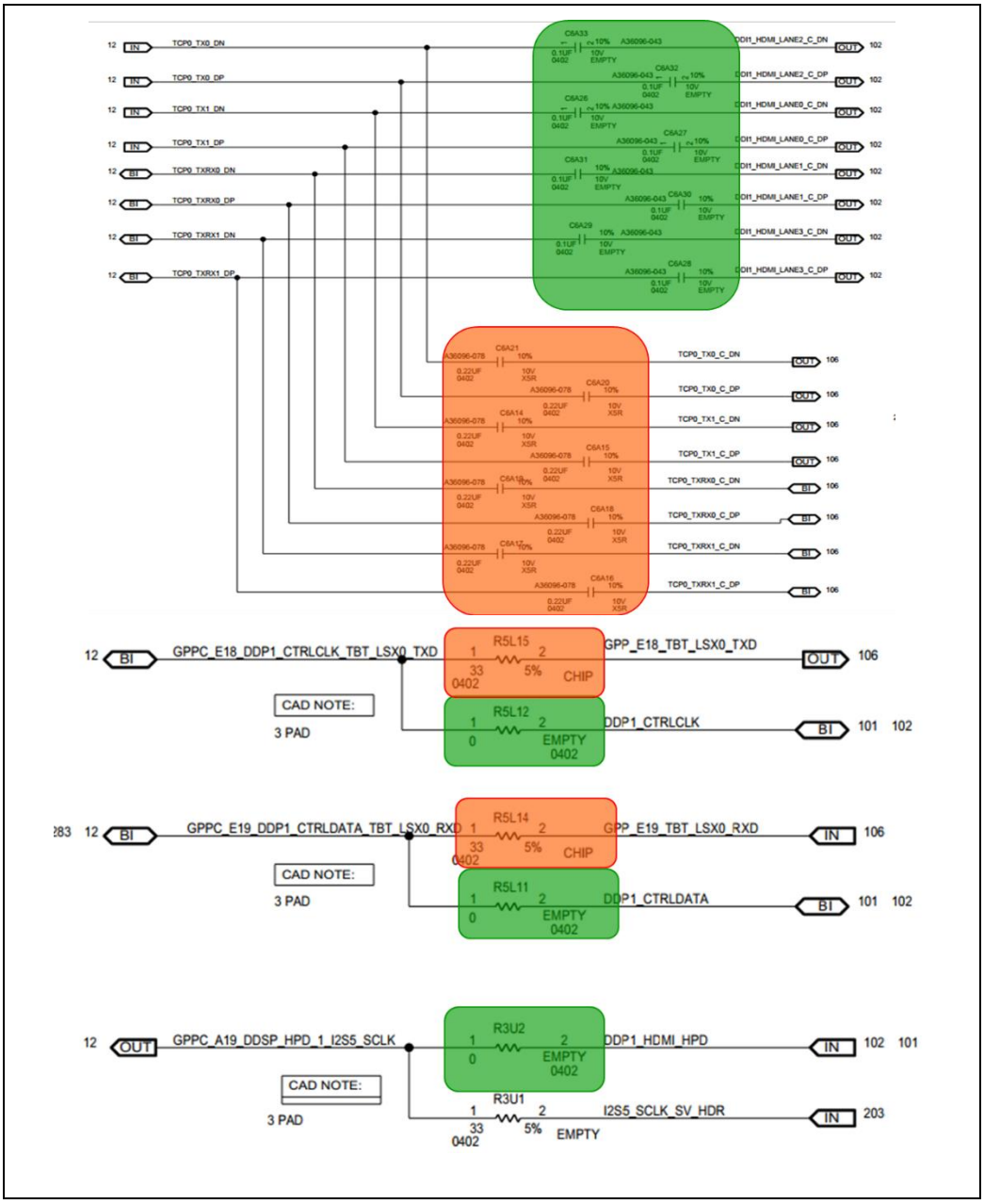


Figure 3-111. Layout Snapshot (Top Layer)

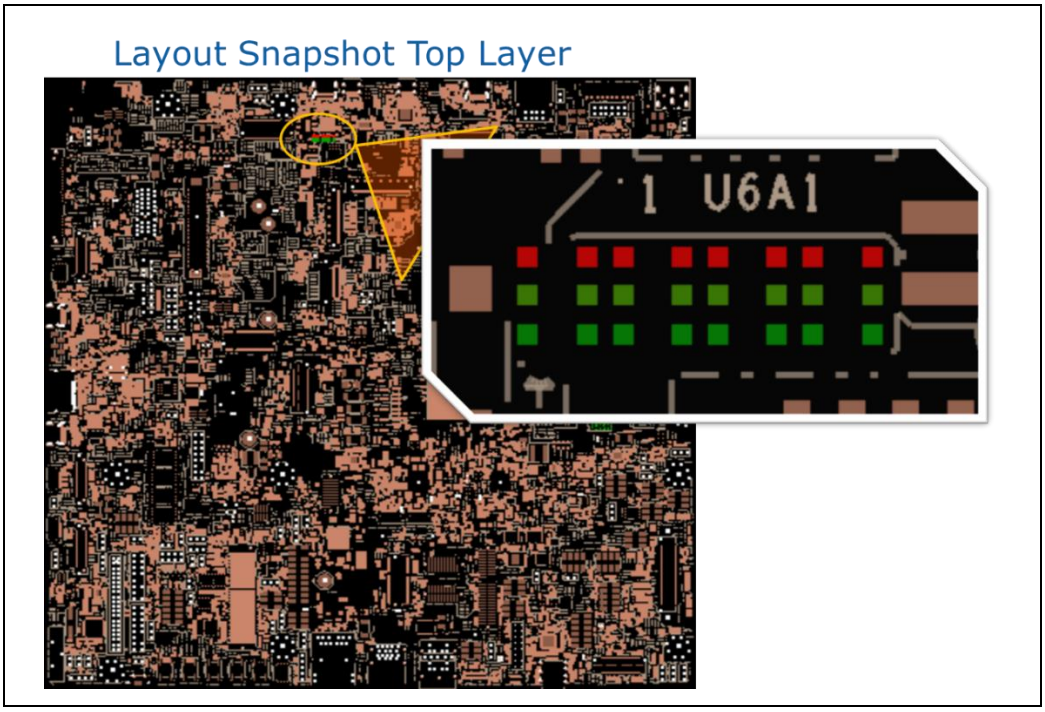
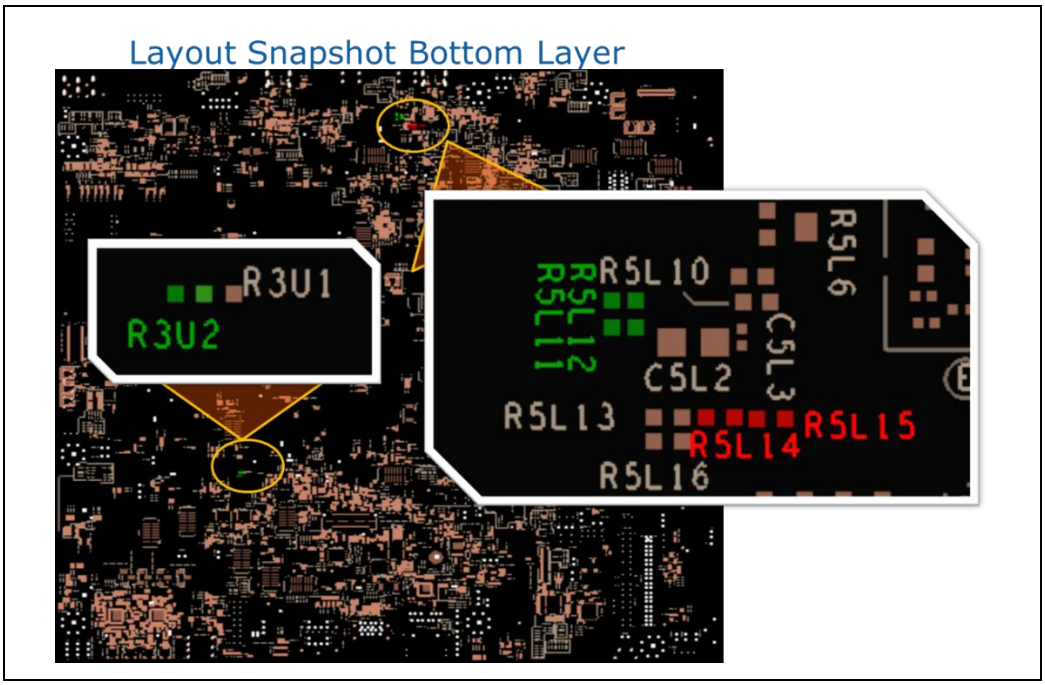


Figure 3-112. Layout Snapshot (Bottom Layer)



3.3 Optional Reworks

3.3.1 Rework to Enable DeepSx Exit Flow in MAF Mode on TGL UP3 RVP

Description: This rework is to enable the PWRBTN path directly to PCH, instead of enabling it through EC.

Impact if not done: This rework enables DeepSx exit flow in MAF mode on TGL UP3 RVP. Without this rework, DeepSx exit does not work.

Details: SMD Stuff/Unstuff.

Applicable To: All TGL UP3 RVPs.

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, and IPTL191001.

Table 3-60. Rework Details

Note: Schematic reference is same across all TGL UP3 RVPs

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R6H4	0E, 5%, 0402	NA
Stuff	Resistor	R6H5	NA	0E, 5%, 0402

Figure 3-113. Schematic Snapshot

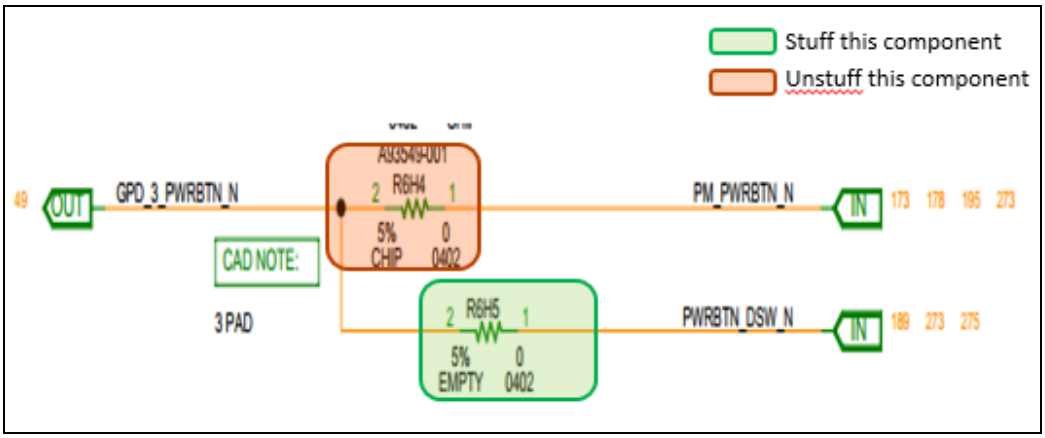
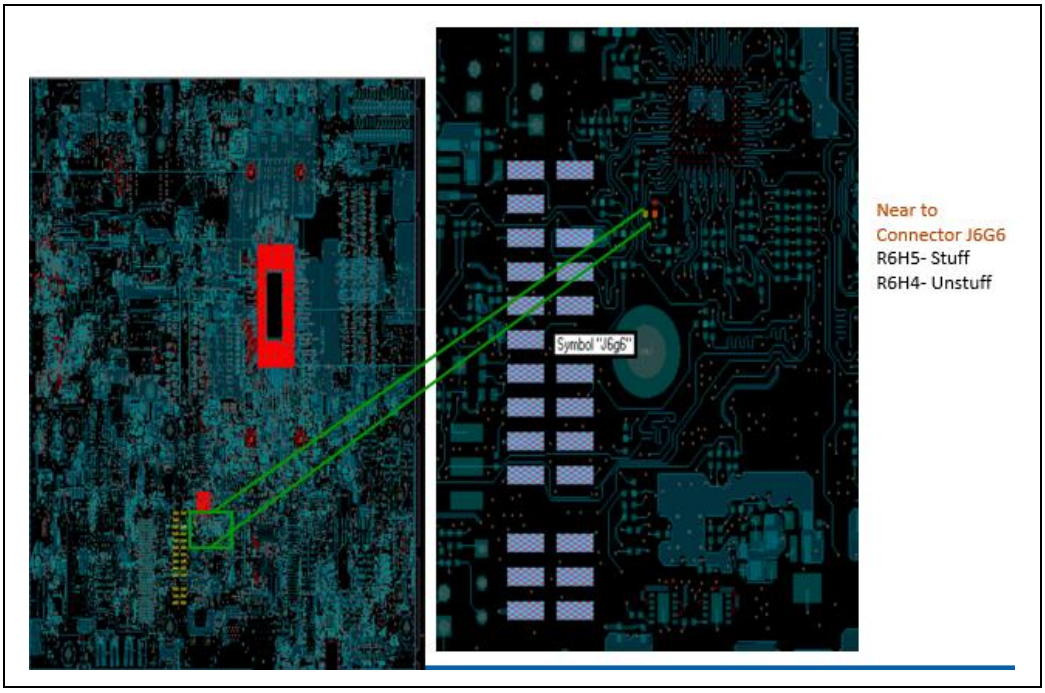


Figure 3-114. Layout Snapshot (Top Layer)



3.3.2 Rework to Enable SPI QUAD MODE Functionality at 50 MHz

Description: This rework is required to increase the isolation resistor value to 3.3K for SPI0_IO2 and increase the drive strength for the SPI IO2.

Impact if not done: ITP Debug consent strap will not functional.

Details: SMD Resistor rework, Dediprog programming to increase the drive strength.

Applicable To: TGL-UP3 RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402 IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192802, IPTL191502, IPTL191701, IPTY190802, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTL193001, IPTY193201, IPTY193102, IPTL193402, IPTL193501, IPTY193301, IPTY193401, IPTY193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTY193901, IPTY193902, IPTL194702, IPTY194703, IPTY194701, IPTY194702, IPTL201201, IPTY201701, IPTL201901, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-61. Rework Details

Action	Item	Reference Description	Description of Existing Part	Description of New Part	Applicable To
Modify	Resistor	R3G88	RES D,0402,1K OHM,5.00%,1/10W	3.3K Ohm, 0402	TGL UP3 DDR4 SODIMM RVP
Modify	Resistor	R3G89	RES D,0402,1K OHM,5.00%,1/10W	3.3K Ohm, 0402	TGL UP3 LP4X RVP
Modify	Resistor	R3G89	RES D,0402,1K OHM,5.00%,1/10W	3.3K Ohm, 0402	TGL UP3 LP5X RVP

Figure 3-115. Schematic Snapshot

TGL UP3 DDR4 SODIMM RVP:

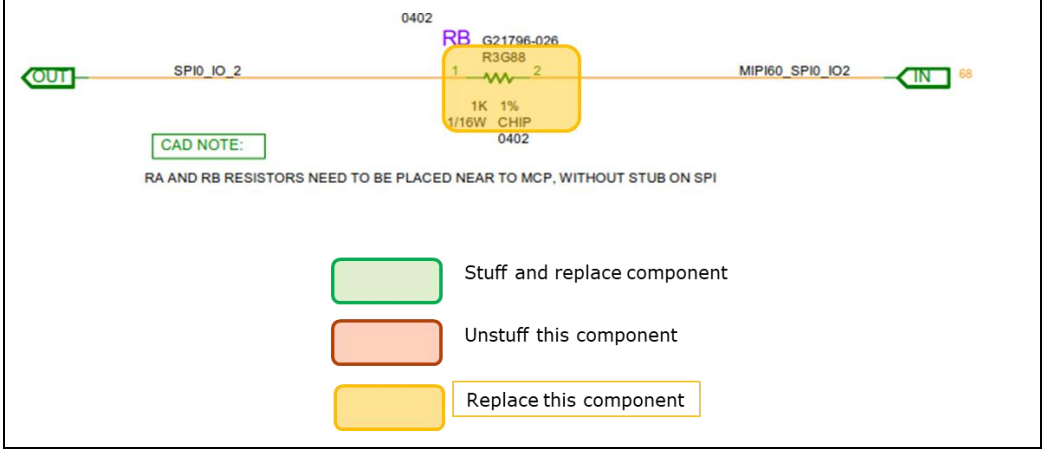
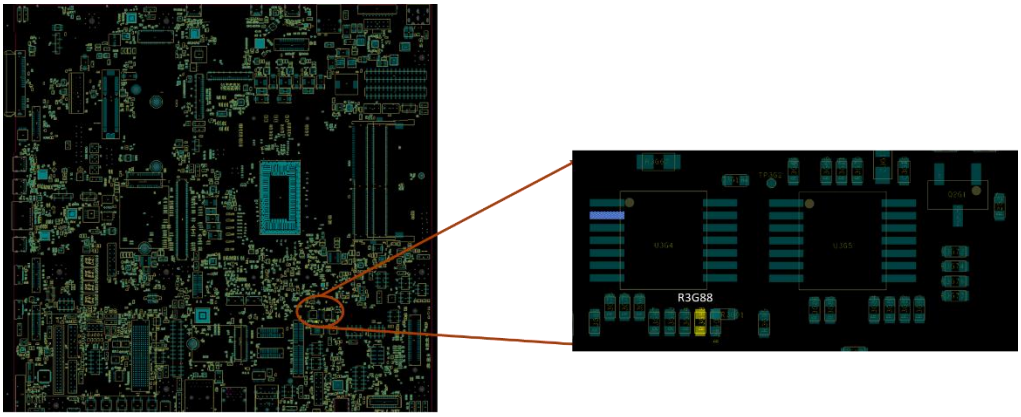


Figure 3-116. Layout Snapshot (Top Layer)

TGL UP3 DDR4 SODIMM RVP:



3.3.3 Rework to Change the VBATA Caps to Higher Voltage Rating

Description: Rework for changing VBATA caps rating to higher voltage of 25V.

Impact if not done: None.

Details: SMD Resistor rework.

Applicable To: TGL-UP3 RVP

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL192101, IPTL192103, IPTL192203, IPTL192604, IPTL192901, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL201901 and IPTL193601

Table 3-62. Rework Details: TGL UP3 DDR4 and TGL UP3 LP4X

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	CAP	C3B3	CAP,100uF,16V,7343	CAP,100uF,25V,7343
Replace	CAP	C3B1	CAP,100uF,16V,7343	CAP,100uF,25V,7343

Figure 3-117. Schematic Snapshot: TGL UP3 DDR4 and TGL UP3 LP4X

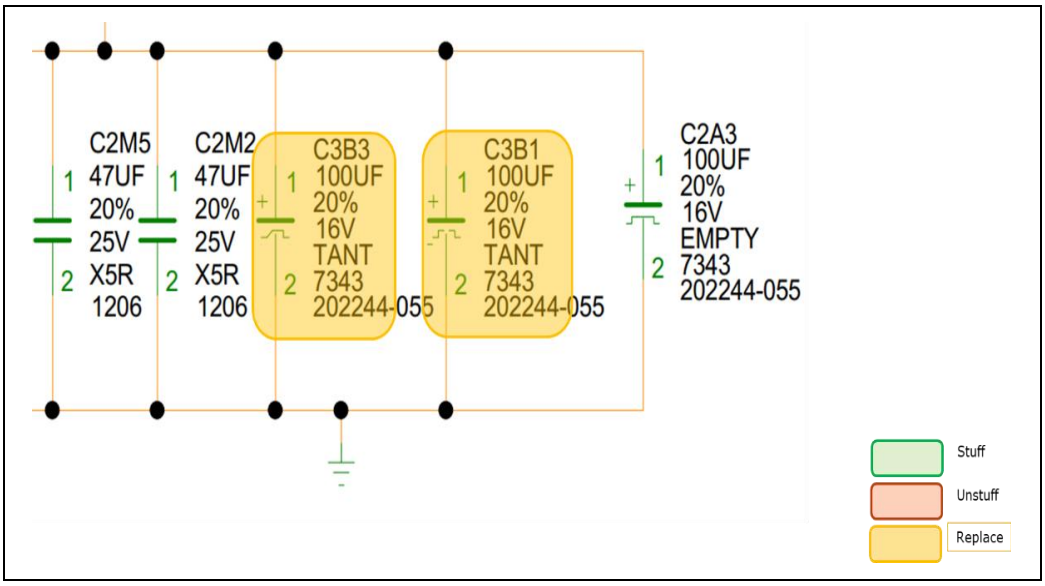


Figure 3-118. Layout Snapshot (Top Layer)

TGL UP3 DDR4 RVP:

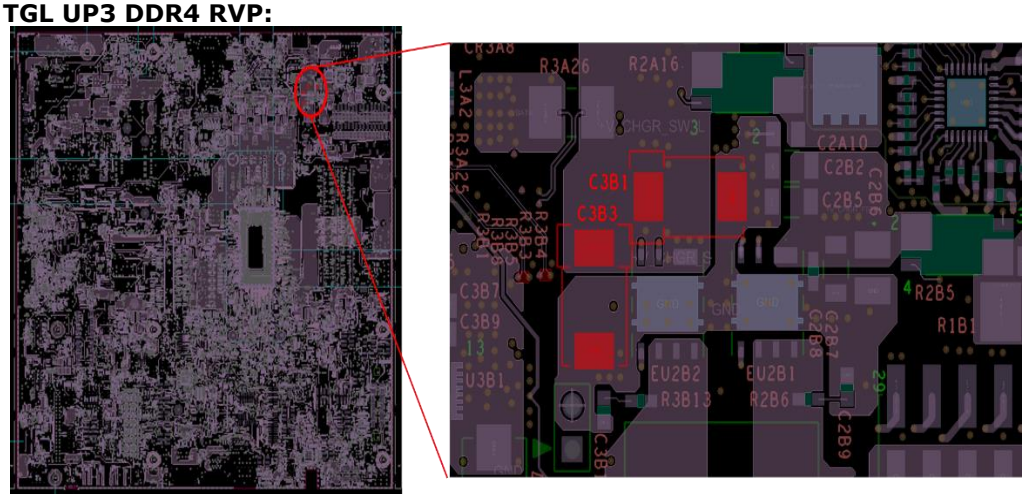
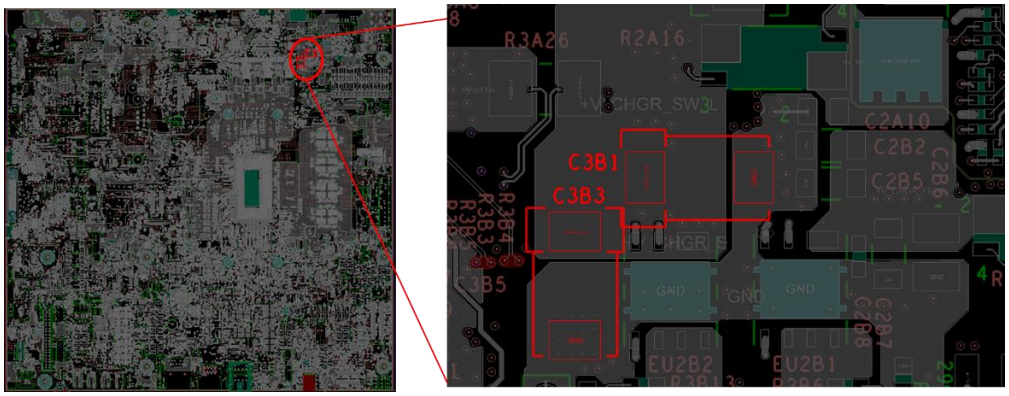


Figure 3-119. Layout Snapshot (Top Layer)

TGL UP3 LP4X RVP:



3.3.4 Rework to Enable TBT™ Compliance on iTBT Ports on RVP

Description: This rework is to unstuff the PD on the LSx voltage level strap to pass the TBT™ compliance on iTBT ports.

Impact if not done: None.

Details: SMD Resistor rework.

Applicable To: TGL-UP3 RVP

WO# Applicable for this Rework: IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701,

IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL194702, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403 IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201 IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTY193102, IPTY201701, IPTL201901, IPTL202001, IPTL202201, IPTL202401, IPTL203002, IPTL203003.

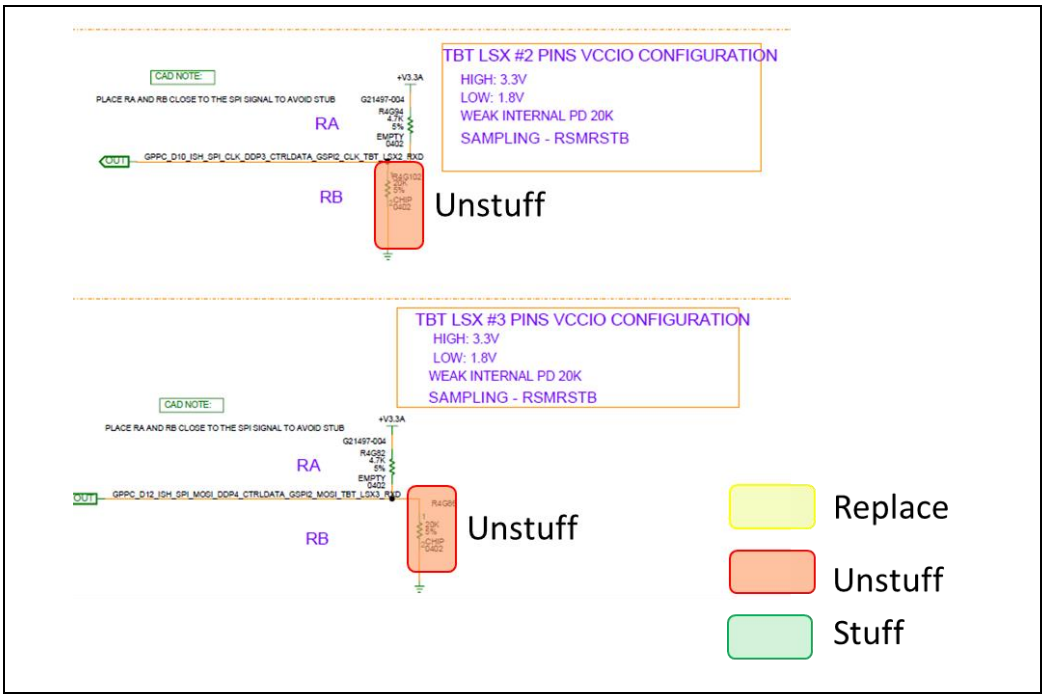
Table 3-63. Rework Details: TGL UP3 DDR4

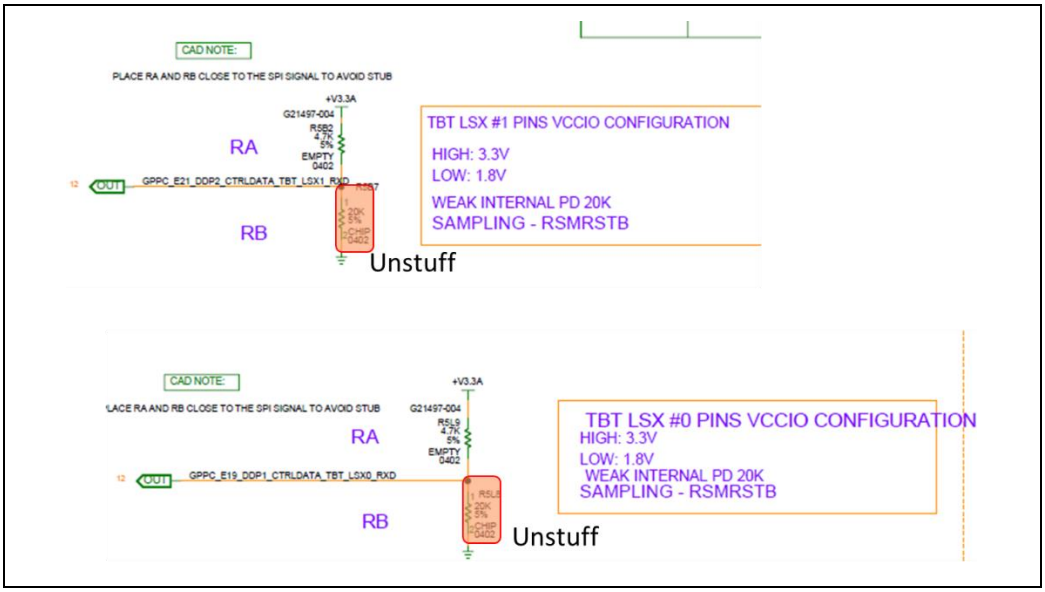
Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R5L8, R5B7, R4G102, R4G86	20K, 5%, 0402	NA

Table 3-64. Rework Details: TGL UP3 LP4X

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R5B9, R5L14, R4G103, R4G88	20K, 5%, 0402	NA

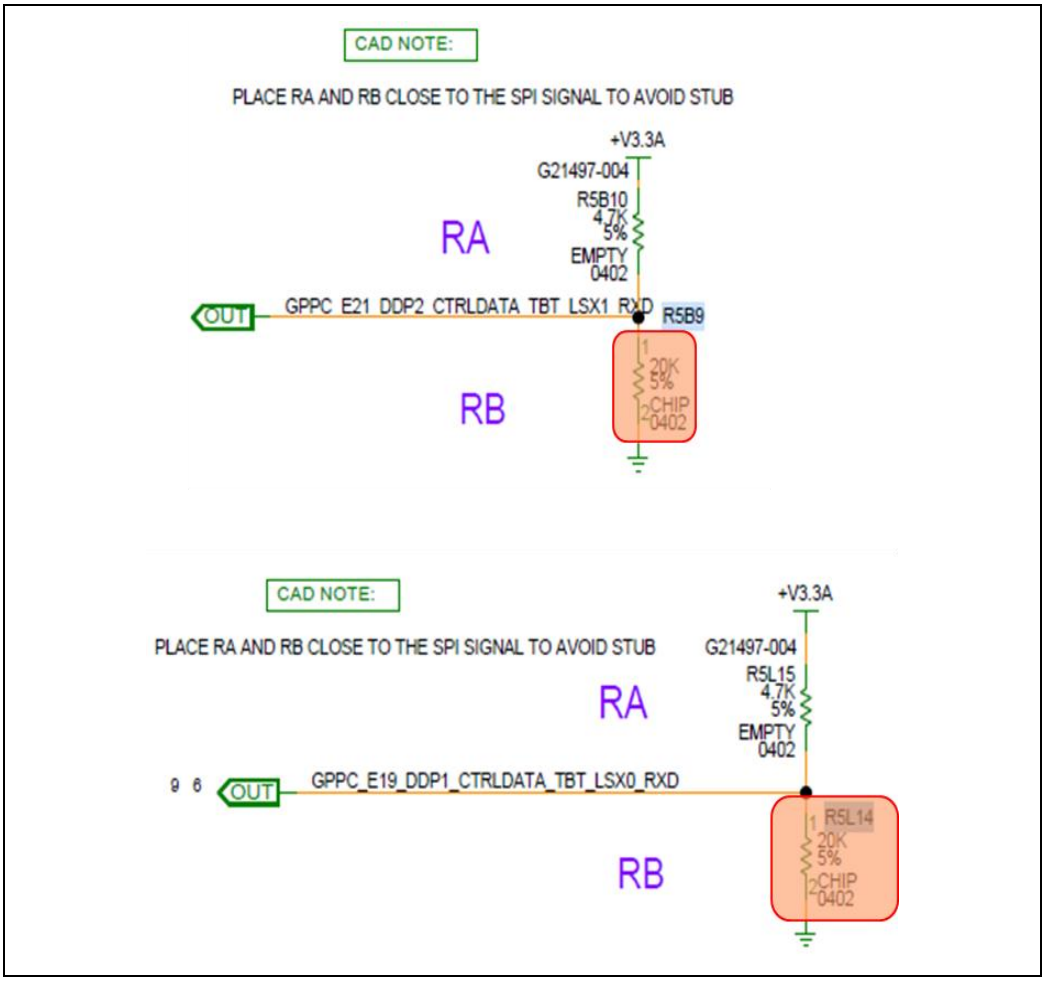
Figure 3-120. Schematic Snapshot: TGL UP3 DDR4




CAD NOTE:
PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB
+V3.3A
G21497-004
R582
4.7K
5%
EMPTY
0402
RA
RB
OUT
GPPC_E21_DDP2_CTRLDATA_TBT_LSX1_RXD
Unstuff
TBT LSX #1 PINS VCCIO CONFIGURATION
HIGH: 3.3V
LOW: 1.8V
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

CAD NOTE:
+V3.3A
G21497-004
R5L9
4.7K
5%
EMPTY
0402
RA
RB
OUT
GPPC_E19_DDP1_CTRLDATA_TBT_LSX0_RXD
Unstuff
TBT LSX #0 PINS VCCIO CONFIGURATION
HIGH: 3.3V
LOW: 1.8V
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

Figure 3-121. Schematic Snapshot: TGL UP3 LP4X



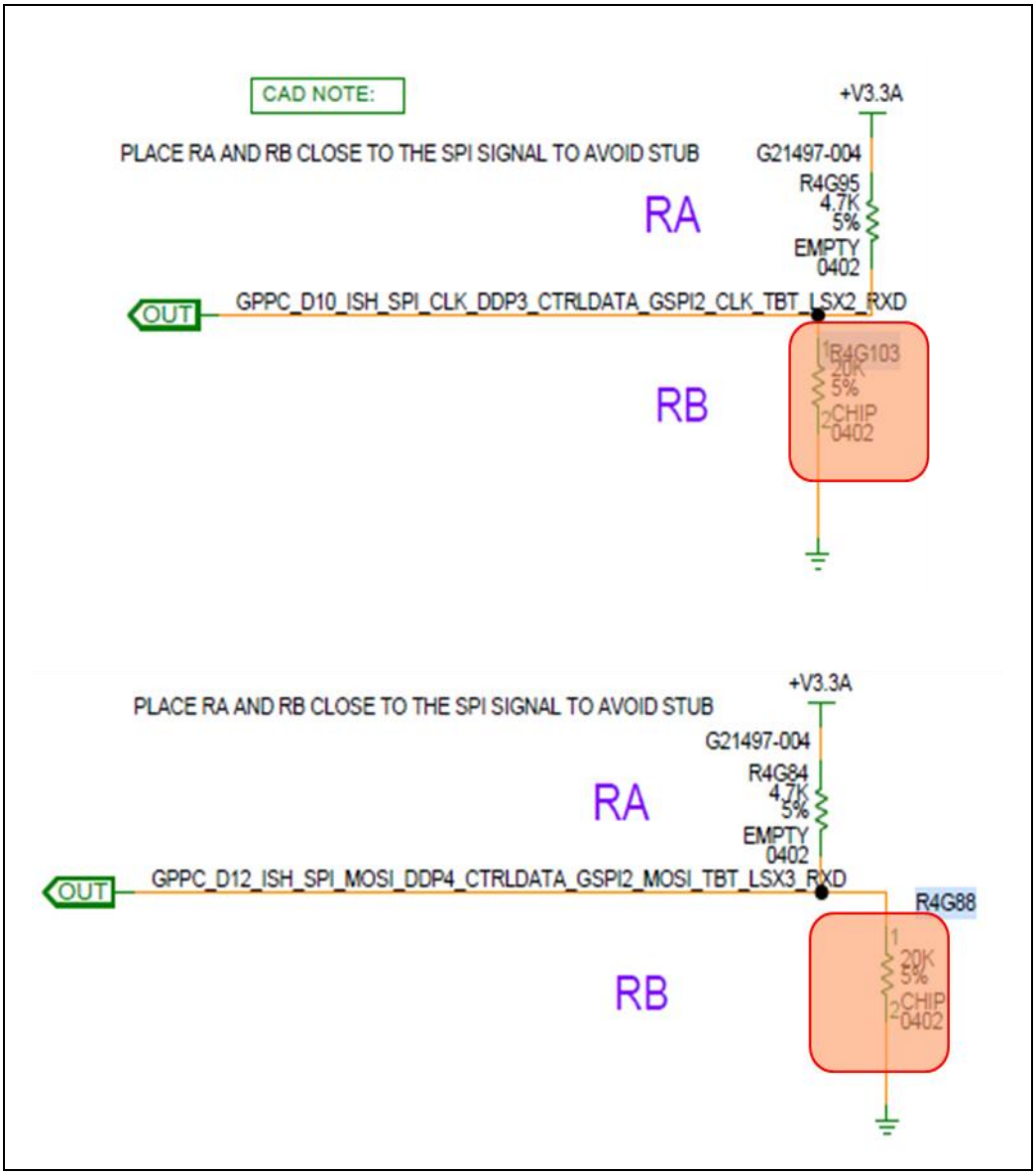

CAD NOTE:
PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB
+V3.3A
G21497-004
R4G95
4.7K
5%
EMPTY
0402
RA
OUT
GPPC_D10_ISH_SPI_CLK_DDP3_CTRLDATA_GSPI2_CLK_TBT_LSX2_RXD
R4G103
20K
5%
CHIP
0402
RB
PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB
+V3.3A
G21497-004
R4G84
4.7K
5%
EMPTY
0402
RA
OUT
GPPC_D12_ISH_SPI_MOSI_DDP4_CTRLDATA_GSPI2_MOSI_TBT_LSX3_RXD
R4G88
20K
5%
CHIP
0402
RB

Figure 3-122. Layout Snapshot (Top Layer)

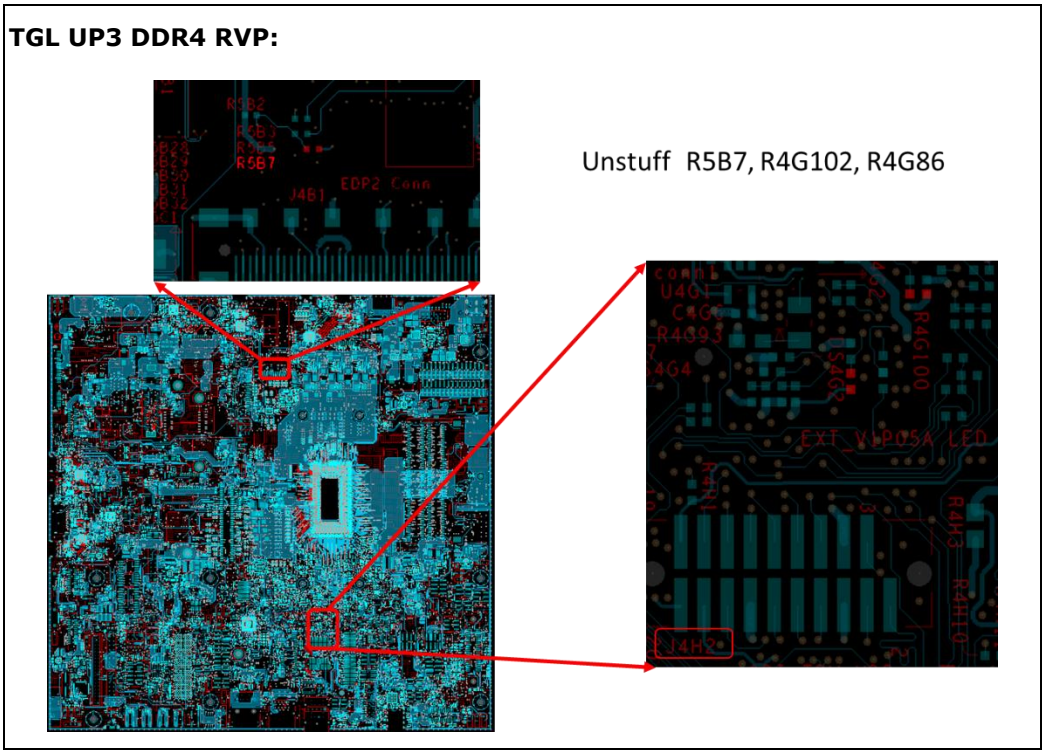


Figure 3-123. Layout Snapshot (Bottom Layer)

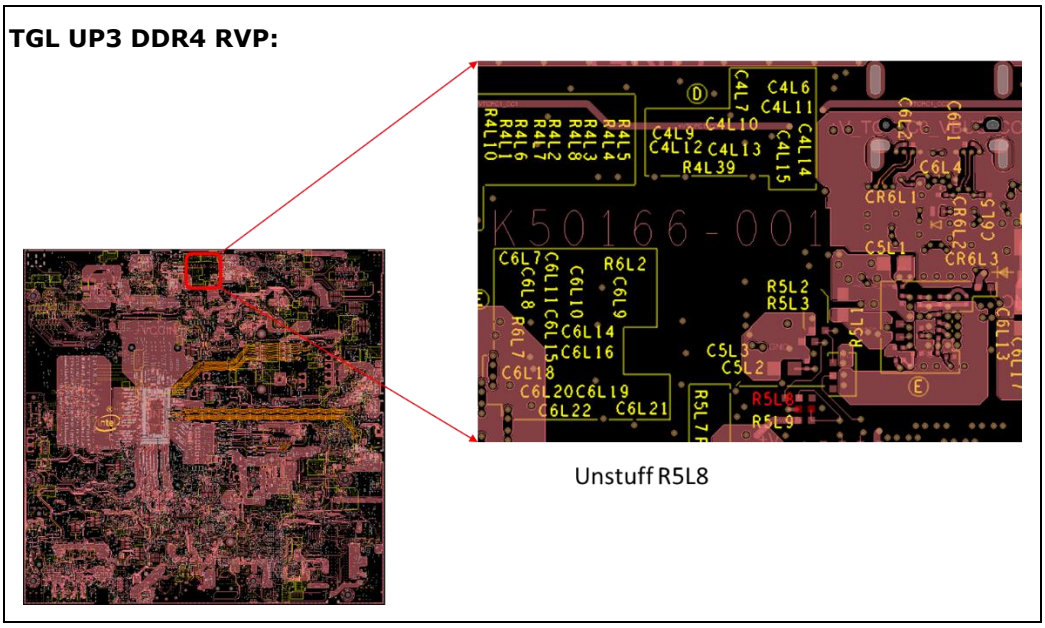


Figure 3-124. Layout Snapshot (Top Layer)

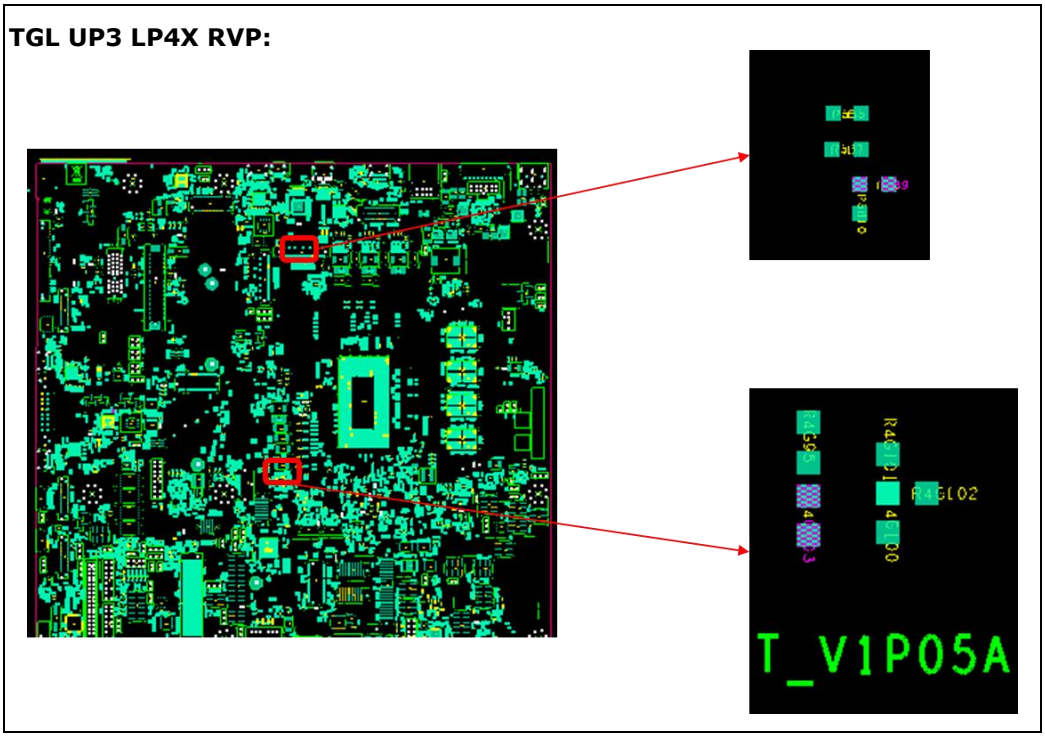
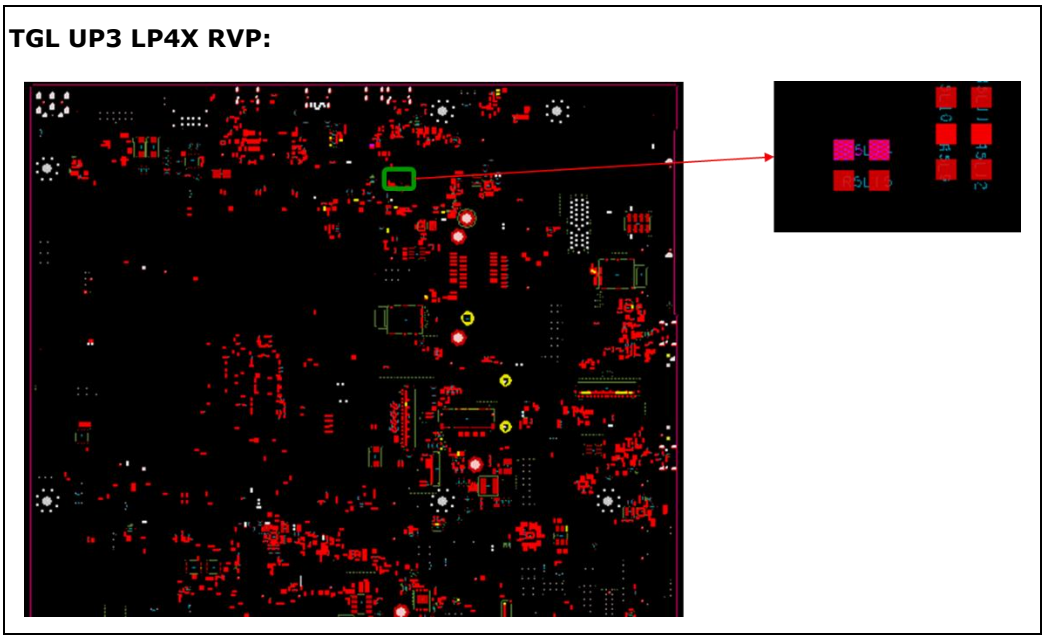


Figure 3-125. Layout Snapshot (Bottom Layer)



3.3.5 Rework to Isolate External VNN and V1.05A VR Power Good

Description: Rework to isolate external VNN and V1.05A VR power good signal from power sequencing tree as existing VNN and V1.05 A part has issue with power good signal implementation.

Impact if not done: No impact.

Details: SMD resistor rework.

Applicable To: TGL UP3 RVPs and TGL UP3 LPDDR4 EXS RVP.

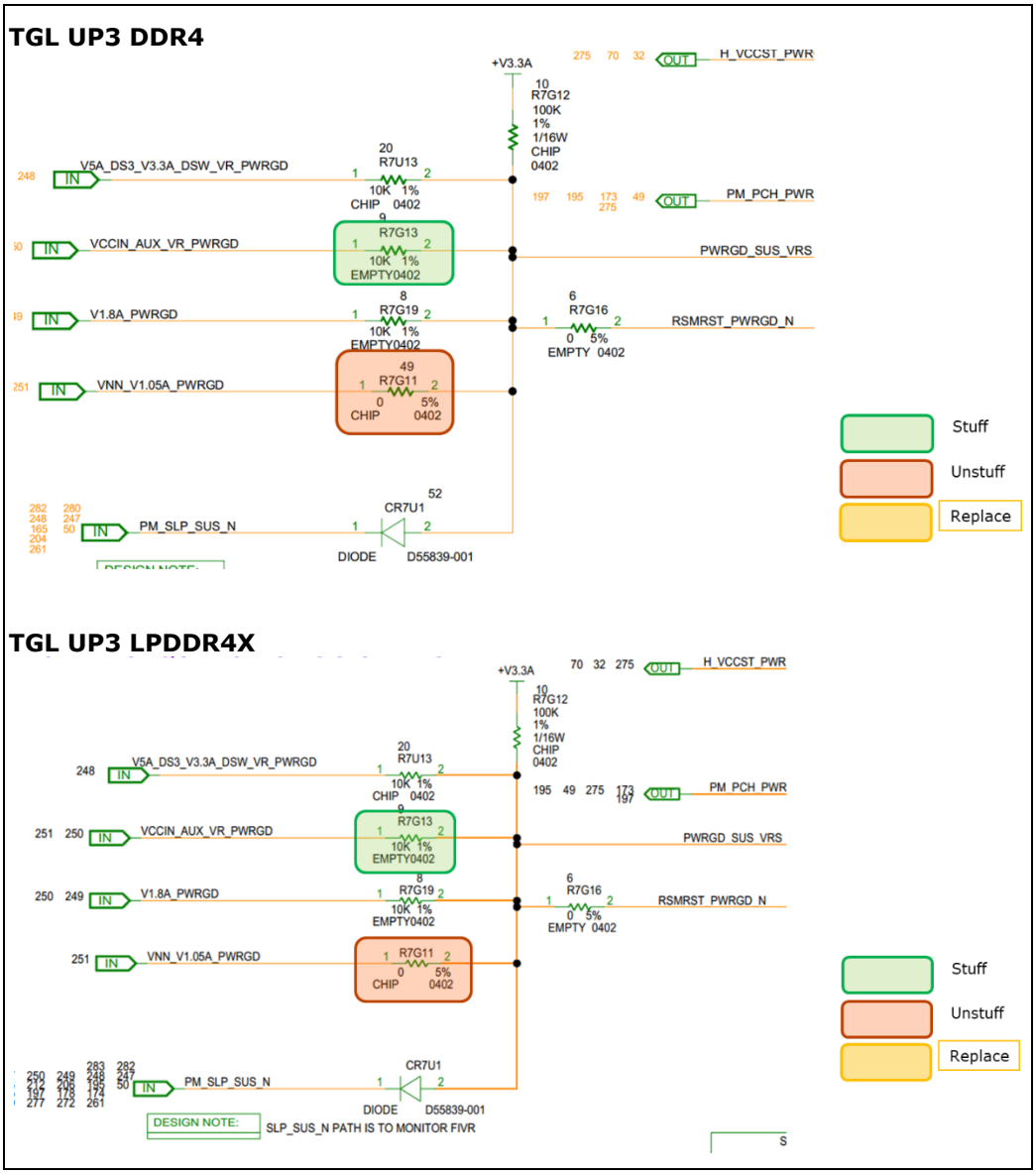
WO# Applicable for this Rework: IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502 IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY201701, IPTY193102, IPTL202001, IPTL202201, IPTL202401, IPTL203002, IPTL203003.

Table 3-65. Rework Details:

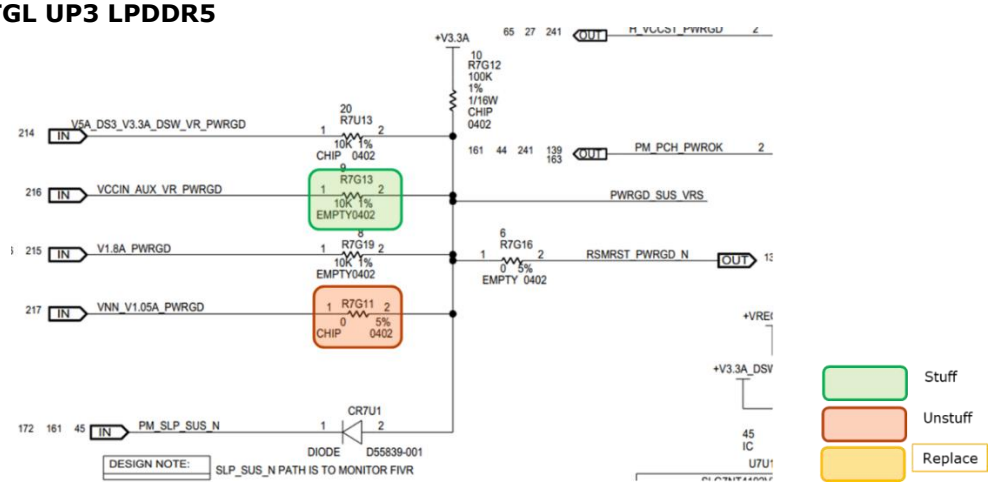
Note: Schematic reference same across all TGL UP3 RVPs

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R7G11	RES D,0402,0 OHM,5.00%,1/16W	NA
Stuff	Resistor	R7G13	NA	RES D,0402,0 OHM,5.00%,1/16W

Figure 3-126. Schematic Snapshot



TGL UP3 LPDDR5



TGL UP3 LPDDR4 EXS RVP

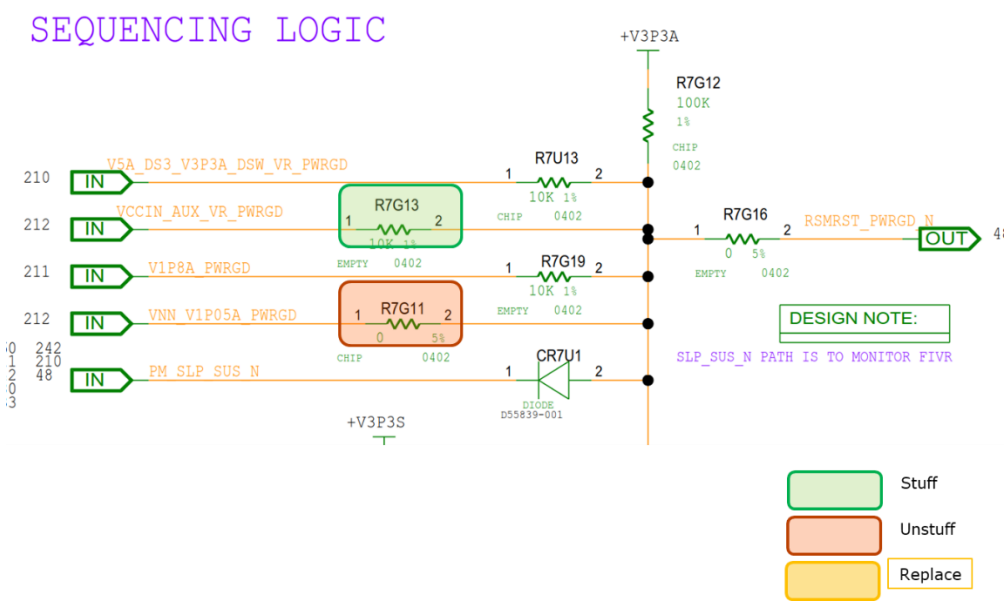
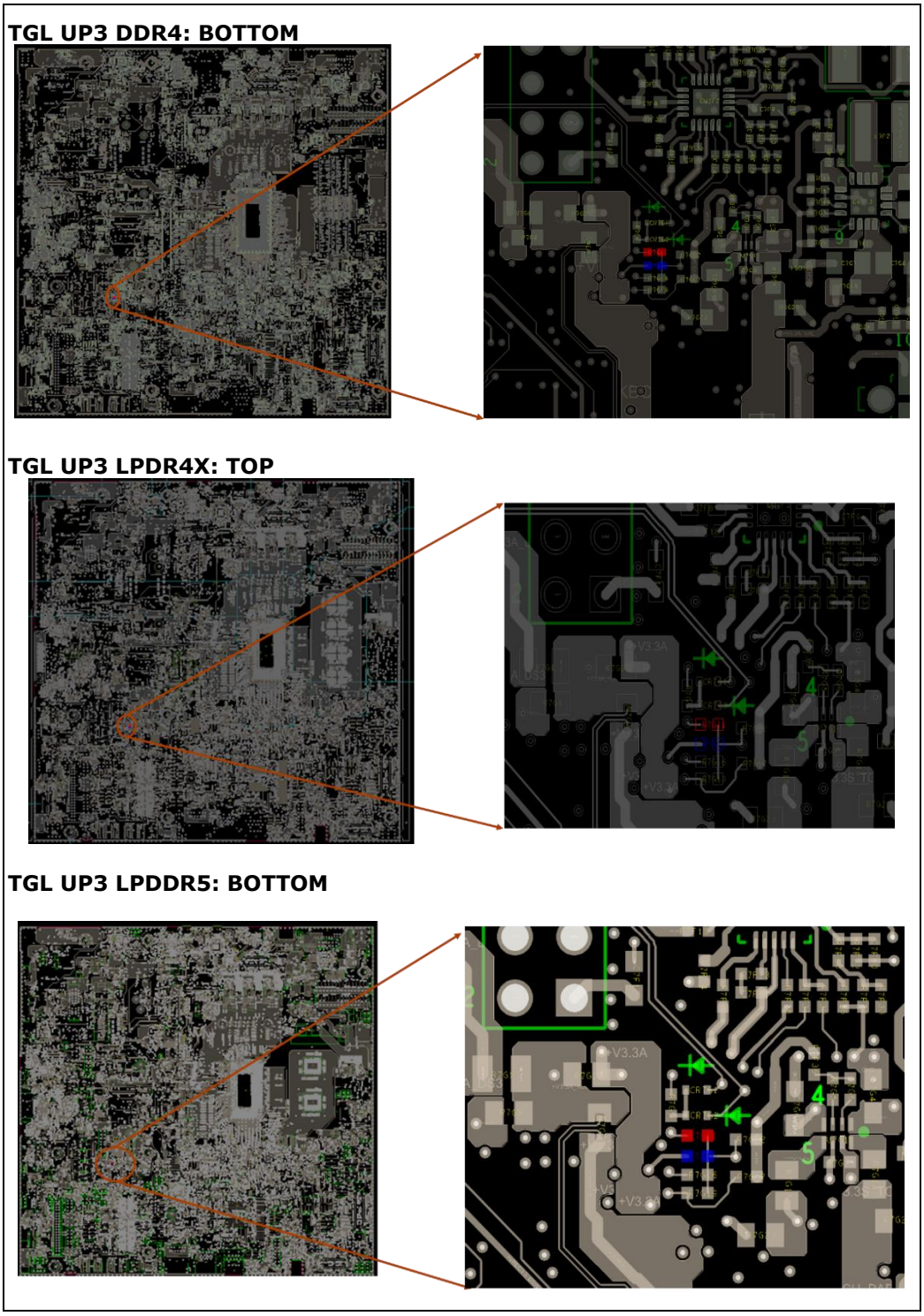
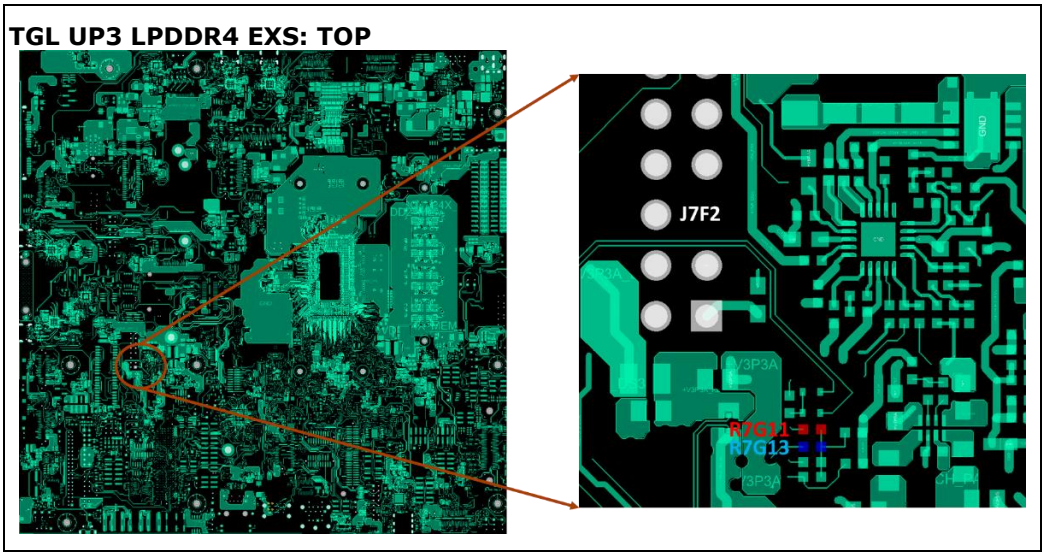


Figure 3-127. Layout Snapshot





3.3.6 Rework to Optimize the EC power in TGL UP3 DDR4

Description: Rework to optimize the EC power in TGL-UP3 DDR4.

Impact if not done: There is no impact of this rework.

Details: SMD Resistor rework.

Applicable To: TGL UP3 DDR4 and LPDDR4x.

WO# Applicable for this Rework: IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901 IPTY193902, PTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901 IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202 IPTL194702, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL201201, IPTL201901, IPTL193601, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

Table 3-66. Rework Details: TGL UP3 DDR4

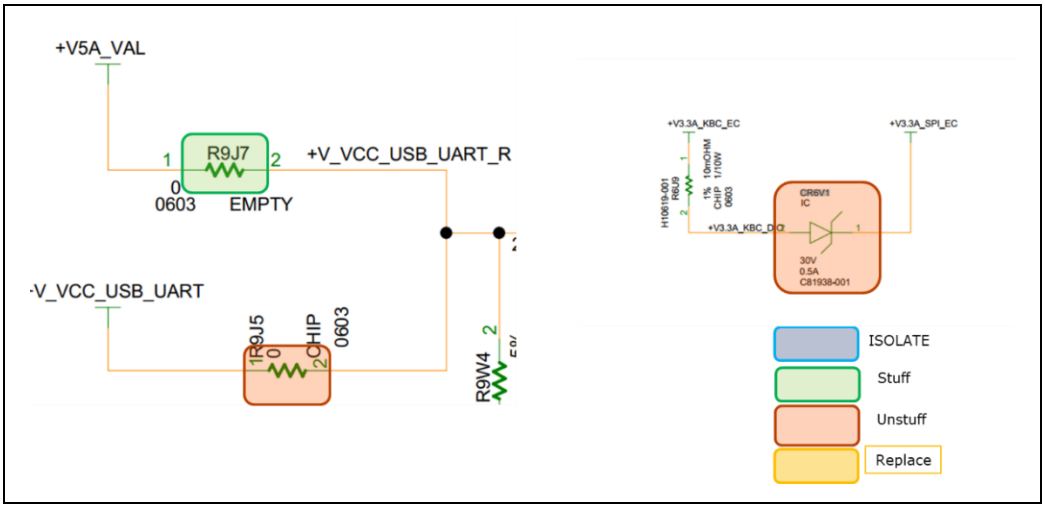
Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Diode	CR6V1	Diode	N/A
Unstuff	Resistor	R9J5	RES D,040, 0 OHM,5.00%,1/1 6W	N/A

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Stuff	Resistor	R9J7	N/A	RES D,040, 0 OHM,5.00%,1/16W
Stuff	Resistor	R6J17	N/A	RES D,040, 20K OHM,5.00%,1/16W
Stuff	Resistor	R6J13	N/A	RES D,040, 20K OHM,5.00%,1/16W

Table 3-67. Rework Details: TGL UP3 LPDDR4X

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Diode	CR6V1	Diode	N/A
Unstuff	Resistor	R9J5	RES D,040, 0 OHM,5.00%,1/16W	N/A
Stuff	Resistor	R9J7	N/A	RES D,040, 0 OHM,5.00%,1/16W
Stuff	Resistor	R6J17	N/A	RES D,040, 20K OHM,5.00%,1/16W
Stuff	Resistor	R6J13	N/A	RES D,040, 20K OHM,5.00%,1/16W

Figure 3-128. Schematic Snapshot: TGL UP3 DDR4



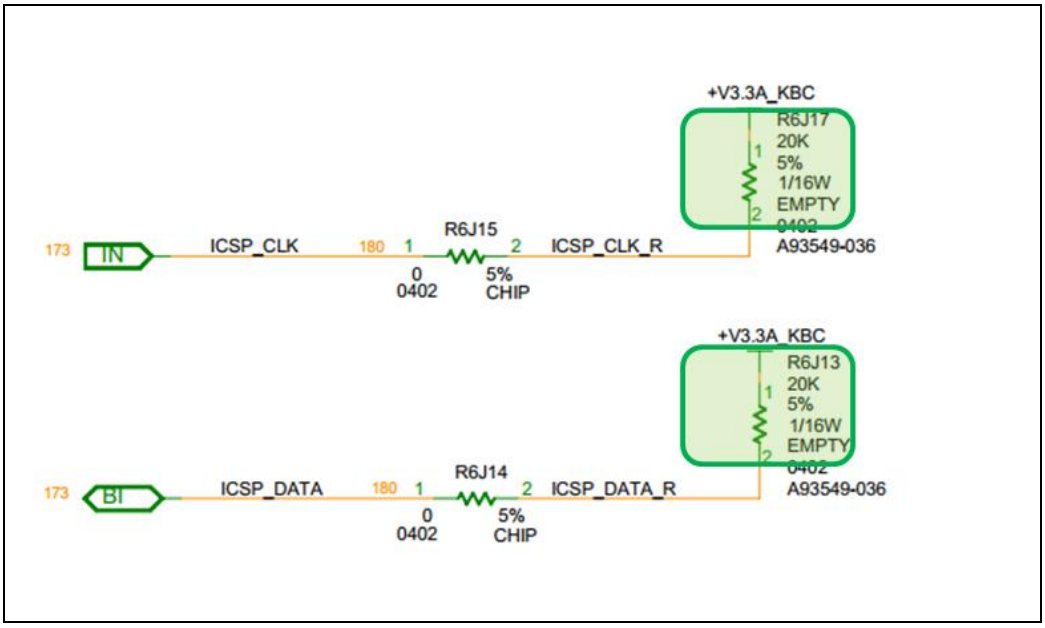
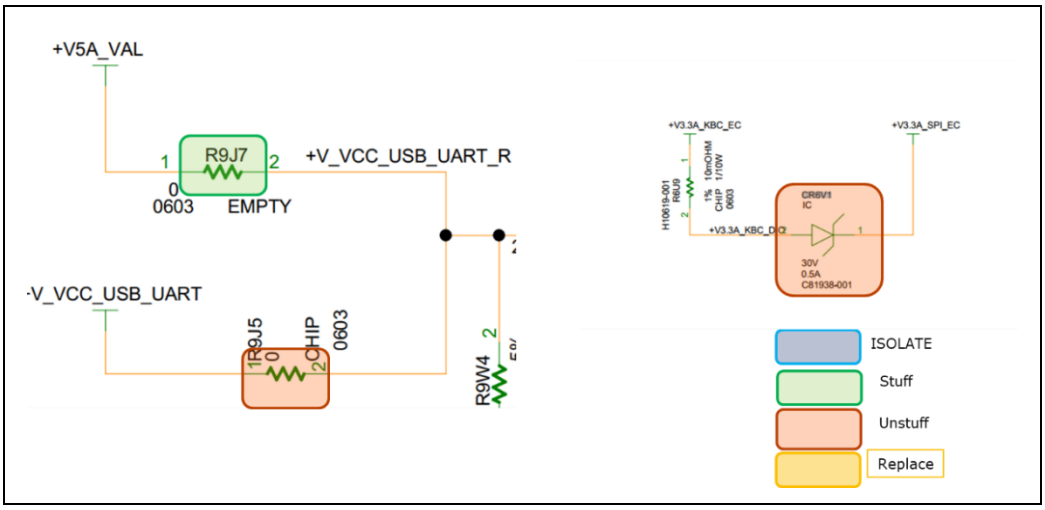


Figure 3-129. Schematic Snapshot: TGL UP3 LPDDR4X



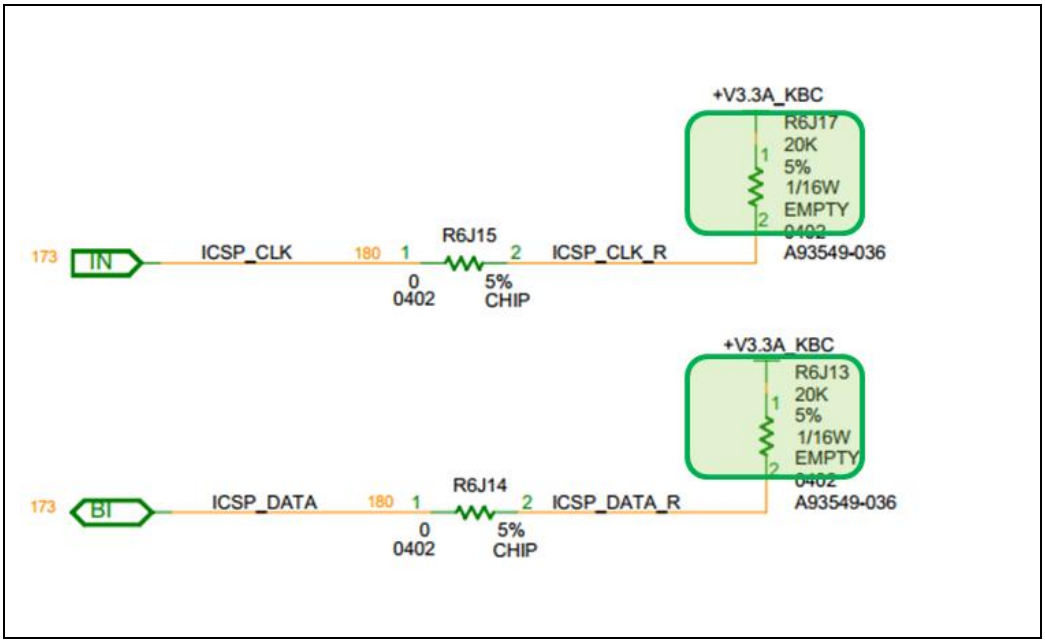
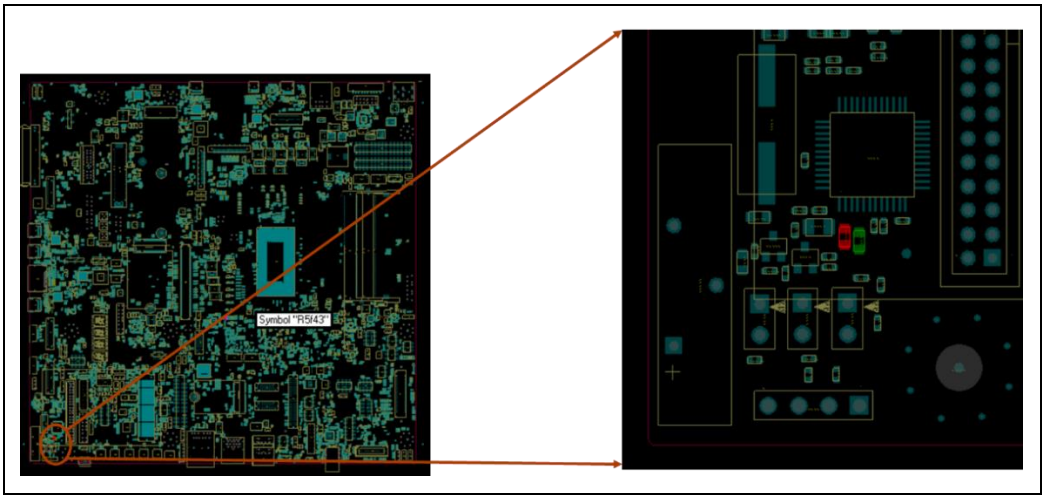


Figure 3-130. Layout Snapshot (Top Layer): TGL UP3 DDR4



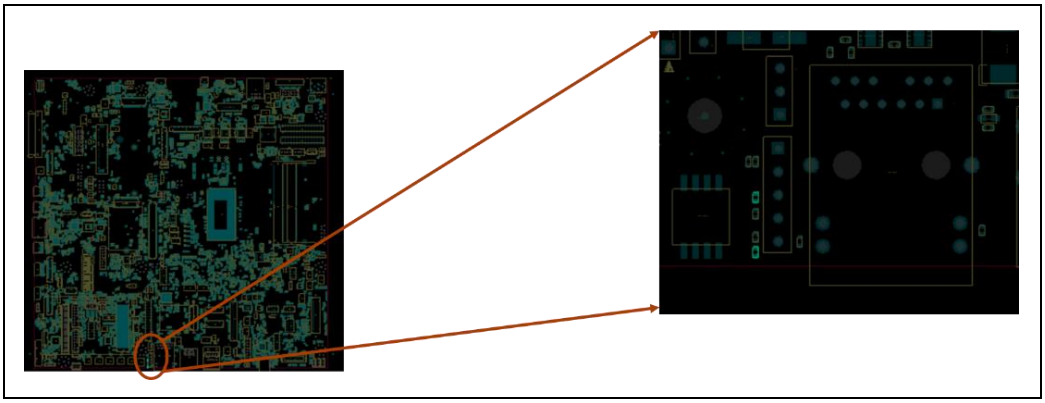


Figure 3-131. Layout Snapshot (Bottom Layer): TGL UP3 DDR4

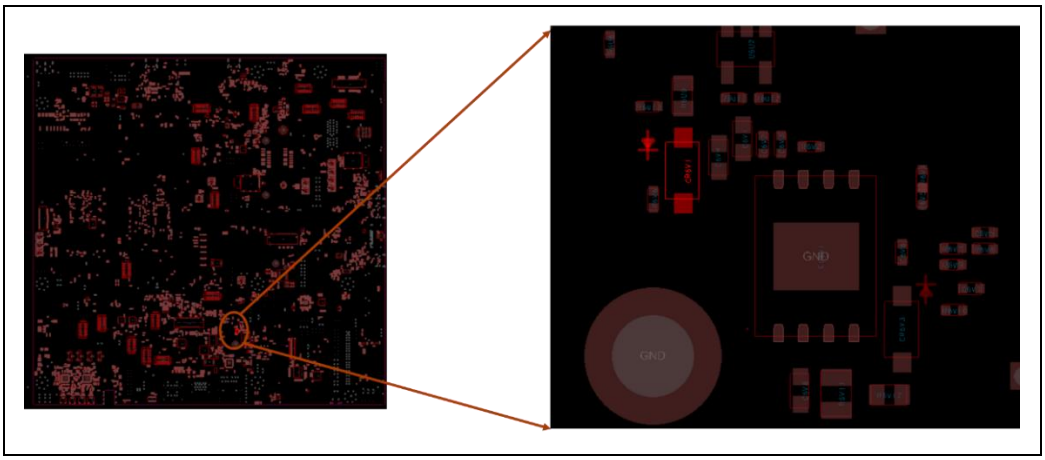


Figure 3-132. Layout Snapshot (Top Layer): TGL UP3 LPDDR4X

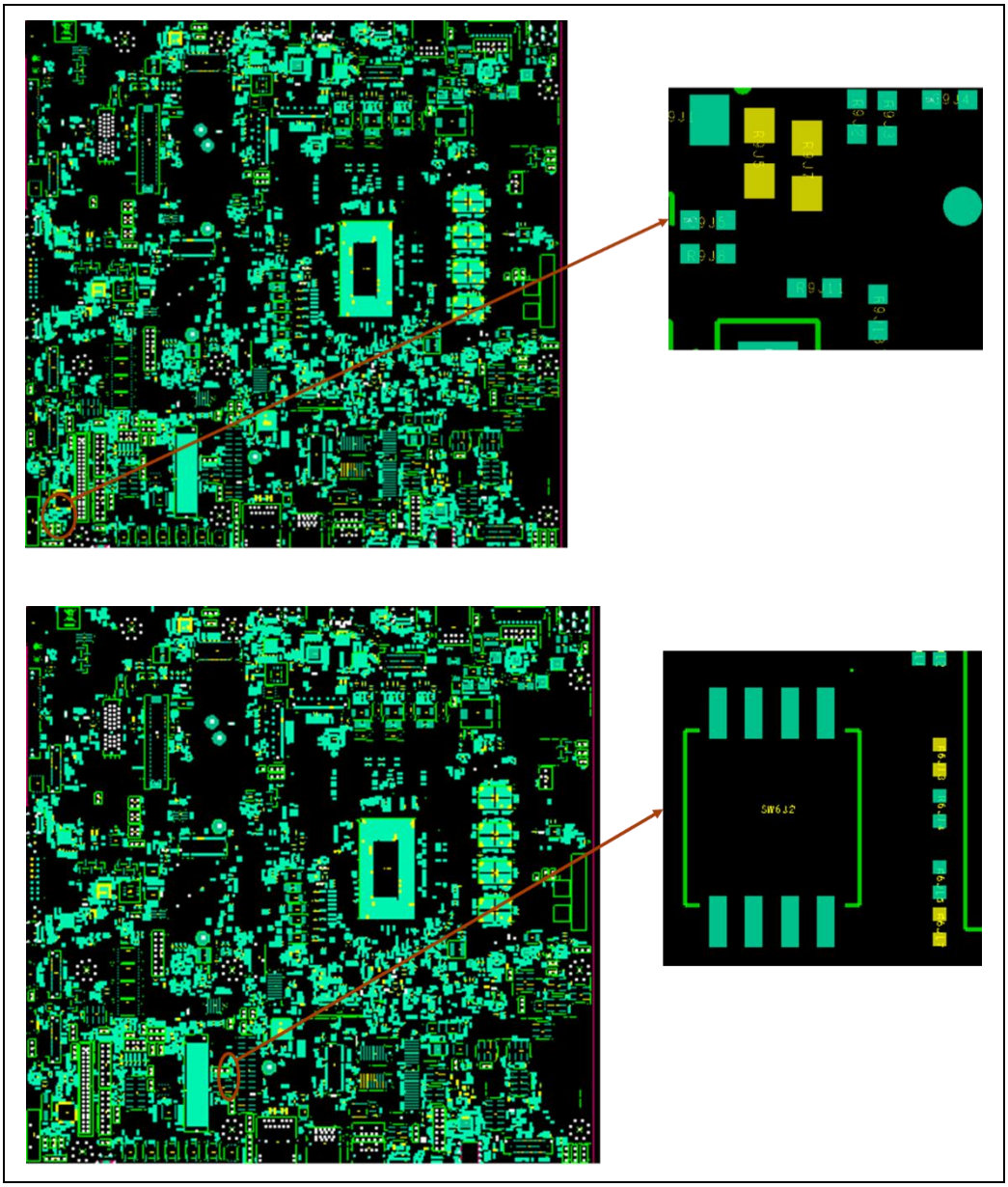
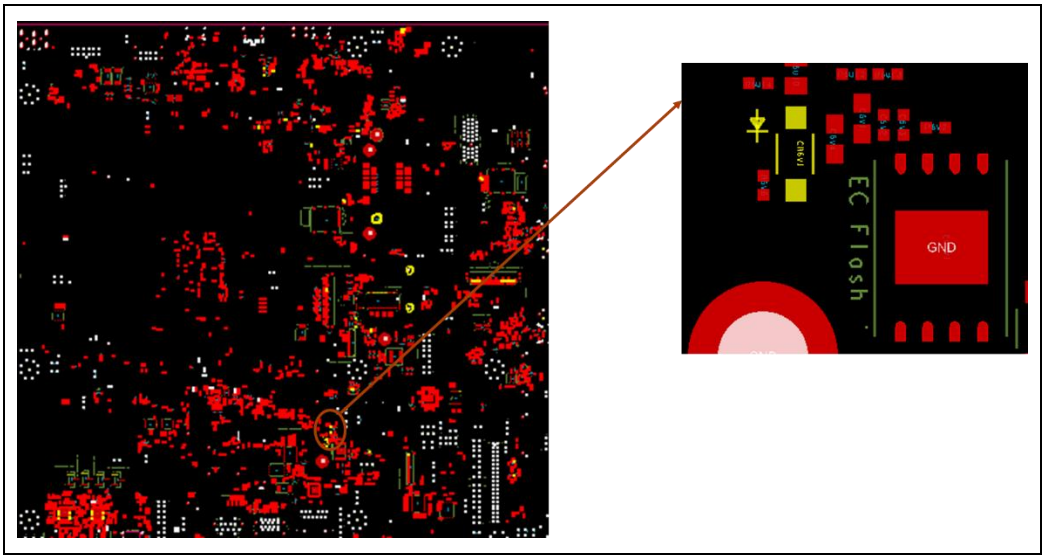


Figure 3-133. Layout Snapshot (Bottom Layer): TGL UP3 LPDDR4X



3.3.7 Rework to Reduce PCH VCCPRIM_1P8 Power from GPPC_B14 GPIO

Description: Rework to reduce PCH VCCPRIM_1P8 power from GPPC_B14 GPIO.

Impact if not done: None.

Details: SMD Resistor rework.

Applicable To: TGL UP3 DDR4 and LPDDR4x.

WO# Applicable for this Rework: IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603 IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL194702, IPTL201201, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTY191801 IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTY201701, IPTL201901, IPTY193102, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002, IPTL203003.

Table 3-68. Rework Details: TGL UP3 DDR4

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R6H7	RES D,0402,0.00 OHM,5.00%,1/1 6W	N/A

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R6W9	RES_D,0402,4.7 kOHM,5.00%,1/ 16W,	N/A

Table 3-69. Rework Details: TGL UP3 LPDDR4X

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R6G25	RES D,0402,0.00 OHM,5.00%,1/1 6W	N/A
Unstuff	Resistor	R6G29	RES_D,0402,4.7 kOHM,5.00%,1/ 16W,	N/A

Figure 3-134. Schematic Snapshot: TGL UP3 DDR4

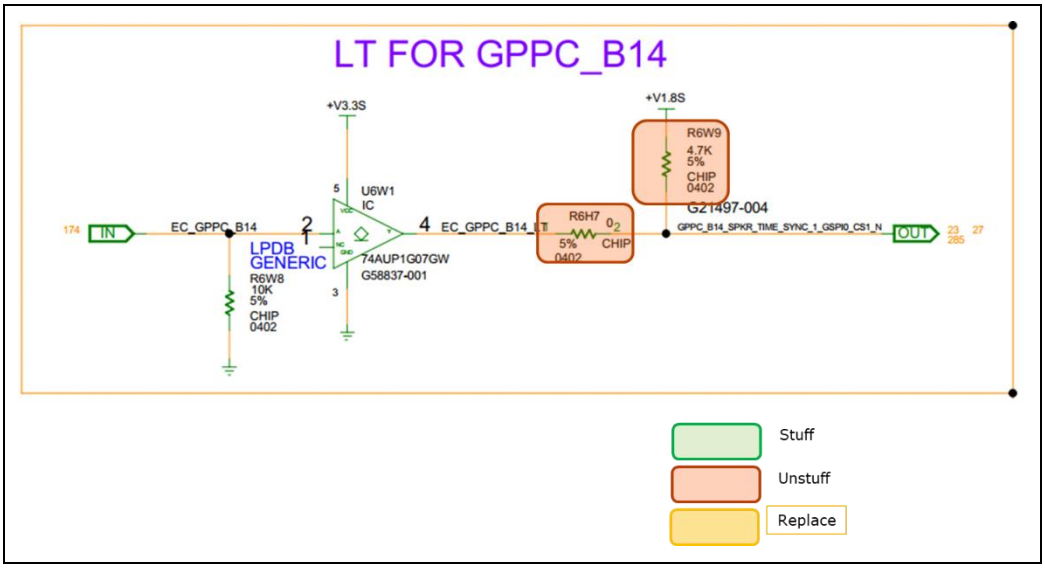


Figure 3-135. Schematic Snapshot: TGL UP3 LPDDR4X

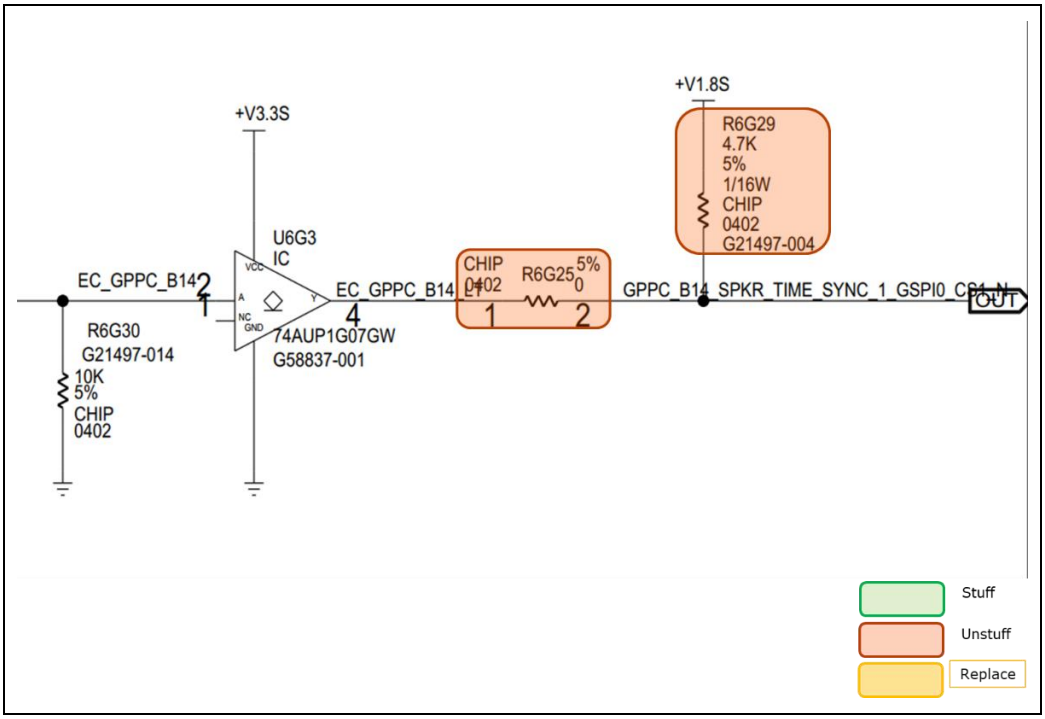


Figure 3-136. Layout Snapshot (Bottom Layer): TGL UP3 DDR4

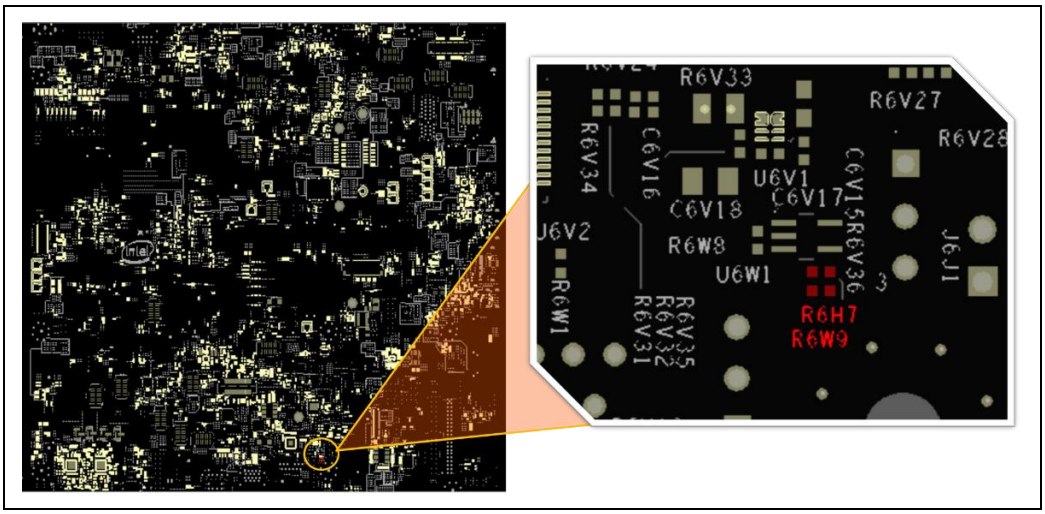
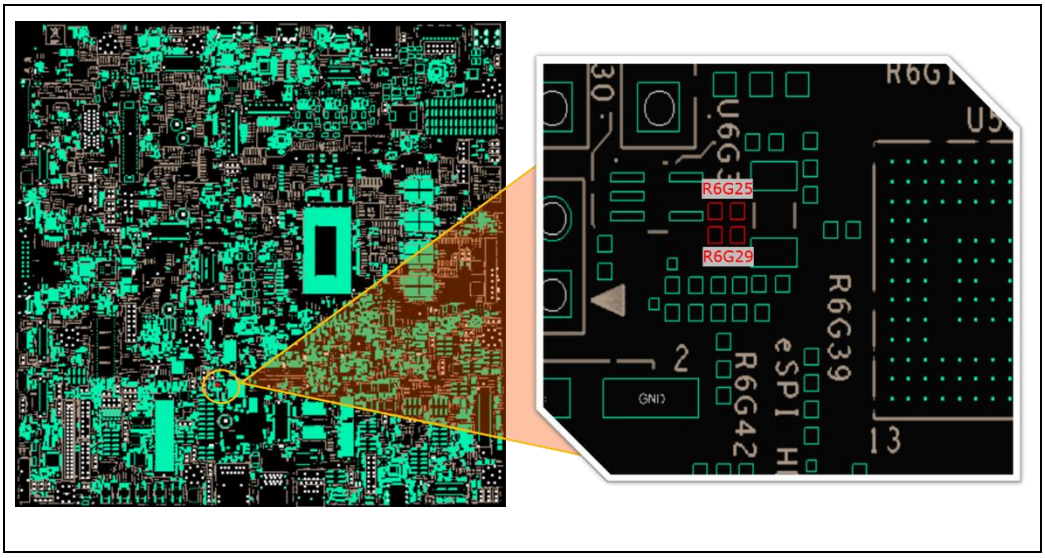


Figure 3-137. Layout Snapshot (Top Layer): TGL UP3 LPDDR4X



3.3.8 Rework to Avoid EYE Diagram Failure on TGL UP3 DDIB HDMI

Description: Rework to avoid HDMI DDIB EYE diagram failure for meeting the HDMI Compliance.

Impact: Without this rework eye diagram failure will be observed on TGL UP3 DDIB HDMI port.

Details: SMD Resistor rework.

Applicable To: TGL UP3 DDR4.

WO# Applicable for this Rework: IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603 IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL194702, IPTL201201, IPTL201901, IPTL202001, IPTL202201, IPTL202401, IPTL203001, IPTL203002.

Table 3-70. Rework Details: TGL UP3 DDR4

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R5N14	RES D,0402,6.04 kOHM,1.00%,1/16W	RES_D,0402,4.3kOHM,1.00%,1/16W

Figure 3-138. Schematic Snapshot: TGL UP3 DDR4

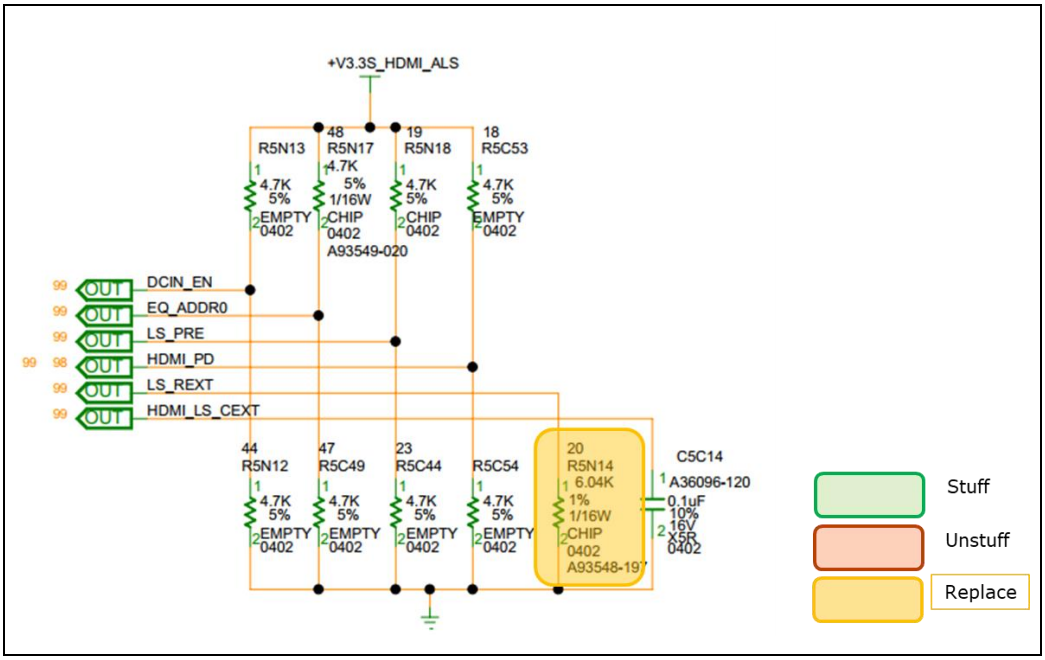
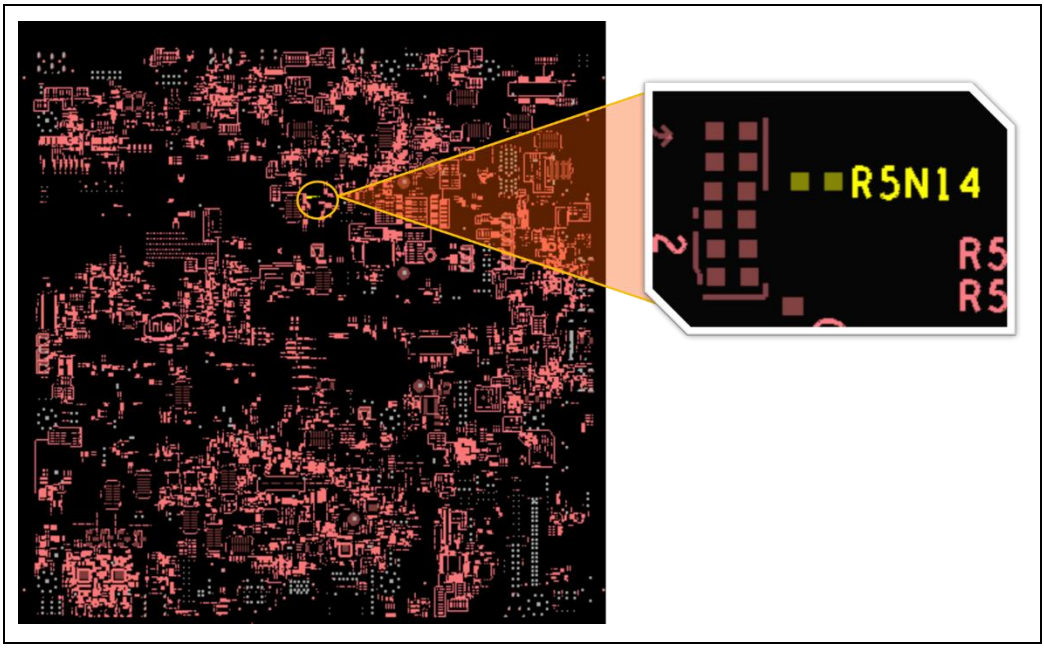


Figure 3-139. Layout Snapshot (Bottom Layer): TGL UP3 DDR4



3.3.9 Rework to Change the ILIM on the USB-C Source Switch for PD Compliance.

Description: The existing ILIM resistor network is not exactly configured for 3A current. Hence, there is a failure seen in the PD compliance. This rework is to change the ILIM resistor to 3A and pass PD compliance.

Impact if not done: Failure in PD compliance

Details: SMD Resistor rework.

Applicable To: TGL UP3 RVPs

WO# Applicable for this Rework: IPTL184901,IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL194702, IPTL201201, IPTL202001, IPTL202201, IPTL202401, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL201901, IPTL202402, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403, IPTY191801, IPTY191802, IPTY191901, IPTY191902, IPTY191903, IPTY193201, IPTY193301, IPTY193401, IPTY193501, IPTY193502, IPTY193601, IPTY193901, IPTY193902, IPTY194401, IPTY194402, IPTY194703, IPTY194701, IPTY194702, IPTY200601, IPTY201501, IPTY201901, IPTY201201, IPTY193102, IPTY201701, IPTL192401, IPTL193101, IPTL193301, IPTL193802, IPTL195001, IPTY202601, IPTL203001, IPTL203002, IPTL203003, IPTL193602, IPTL194801, IPTL200701, IPTL201802, IPTL201801, IPTL200801, IPTL201601, IPTL193603, IPTC203901, IPTC204102, IPTC204103, IPTC204501, IPTC204502, IPTC204503, IPTC205101, IPTU205001.

Table 3-71. Rework Details: TGL UP3 DDR4 RVP

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Replace	Resistor	R6L6, R3A12, R9P22, R9T20	RES D,0402,24.9 KOHM,1.00%	RES D,0402,22.6 KOHM,1.00%

Figure 3-140. Schematic Snapshot: TGL UP3 DDR4 RVP

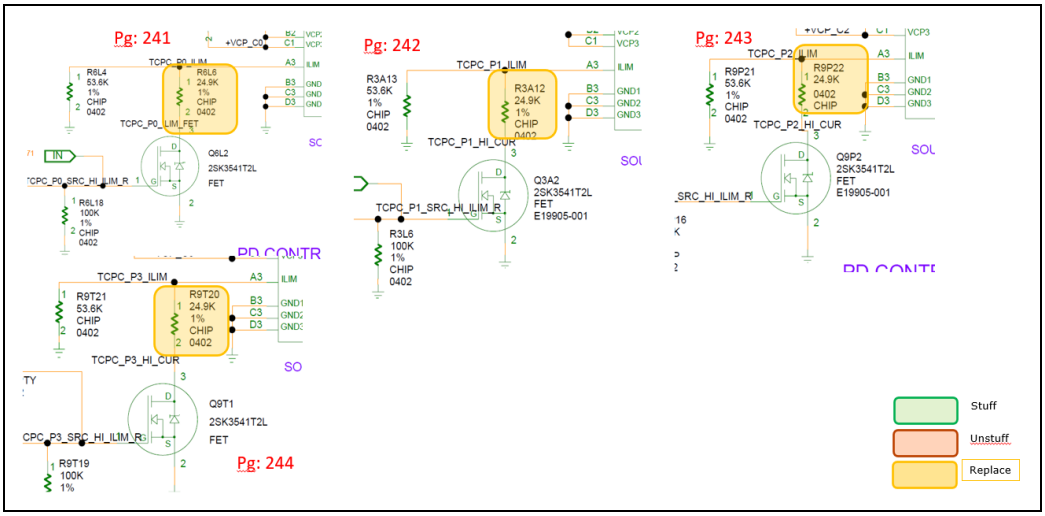


Figure 3-141. Layout Snapshot (Top Layer): TGL UP3 DDR4 RVP

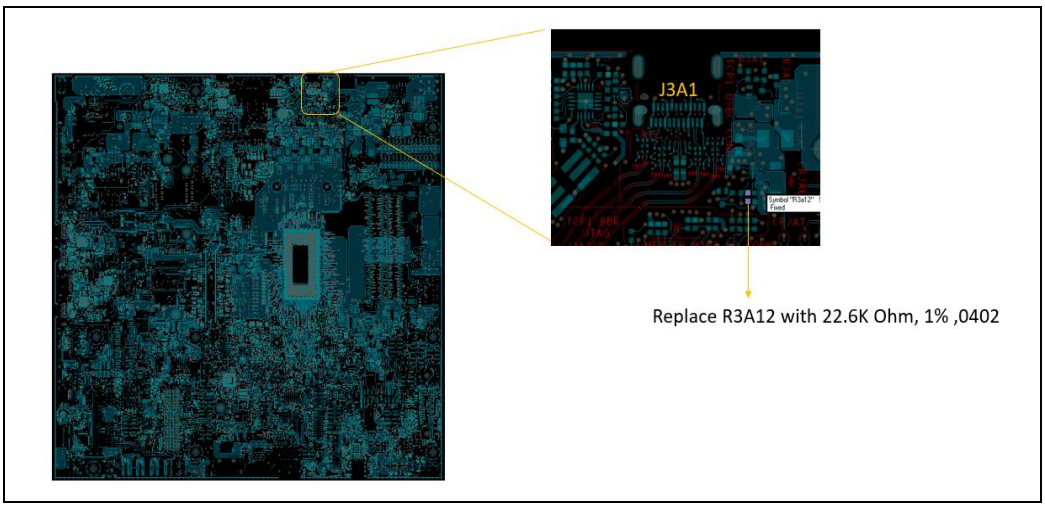


Figure 3-142. Layout Snapshot (Bottom Layer): TGL UP3 DDR4

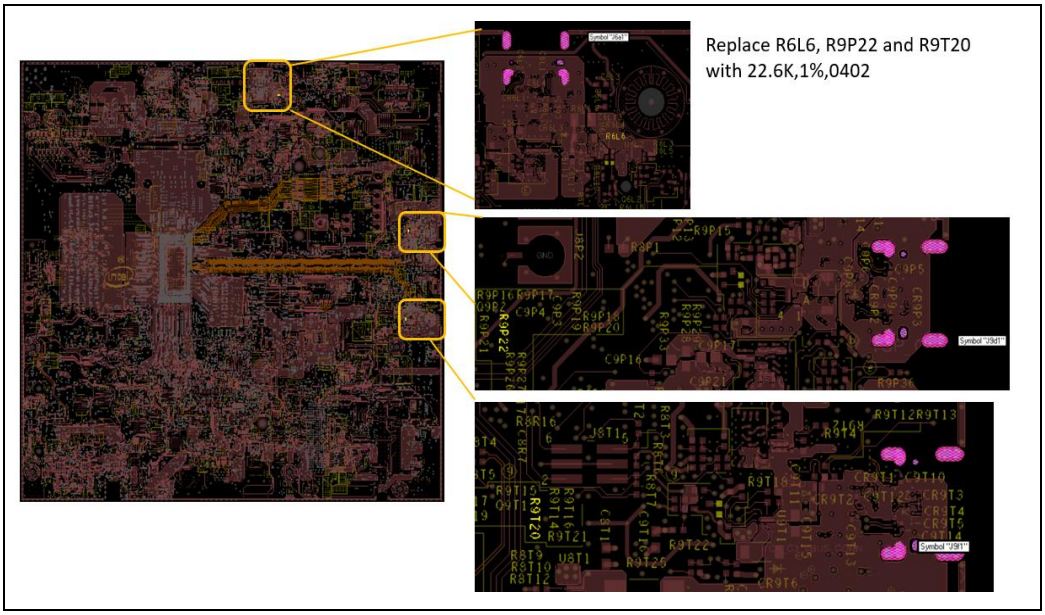


Table 3-72. Reference Designator Comparison

TGL UP3 DDR4 Refdes	TGL UP3 LP4x Refdes	Description of the New Part
R6L6, R3A12, R9P22, R9T20	R6L6, R3A12, R9P21, R9T20	RES D,0402,22.6 KOHM,1.00%

3.3.10 Rework to Enable M.2 WWAN 7560-R+ Module on TGL UP3 Boards.

Description: By default, TGL UP3 WWAN design will support for WWAN M.2 7560 module. Isolating SIM2 path to detect WWAN 7560-R+ module.

Impact: No Impact.

Details: SMD Resistor rework.

Applicable To: TGL UP3 RVPs

WO# Applicable for this Rework: IPTL184901, IPTL185001, IPTL190301, IPTL191001, IPTL191002, IPTL191201, IPTL191203, IPTL191204, IPTL191202, IPTL191901, IPTL191902, IPTL192101, IPTL192102, IPTL192202, IPTL192103, IPTL192203, IPTL192301, IPTL192402, IPTL192501, IPTL192502, IPTL192601, IPTL192603, IPTL192604, IPTL192701, IPTL192901, IPTL192801, IPTL193402, IPTL193501, IPTL193701, IPTL193702, IPTL193801, IPTL193901, IPTL194101, IPTL194202, IPTL194702, IPTL201201, IPTL202001, IPTL202201, IPTL202401, IPTL191101, IPTL191301, IPTL191601, IPTL191702, IPTL192201, IPTL192602, IPTL192702, IPTL192802, IPTL193502, IPTL193601, IPTL201901, IPTL202402, IPTL191502, IPTL191701, IPTL192803, IPTL193001, IPTL193403,, IPTL192401, IPTL193101, IPTL193301, IPTL193802,IPTY193101, IPTY194101, IPTL195001

IPTY202601,IPTL203001, IPTL203002, IPTL203003, IPTY202101, IPTL193602, IPTL194801, IPTL200701, IPTL201802, IPTL201801, IPTL200801, IPTL201601, IPTL193603, IPTC203901, IPTC204101, IPTC204102, IPTC204103, IPTC204501, IPTC204502, IPTC204503, IPTC205101, IPTU205001.

Table 3-73. Rework Details: TGL UP3 DDR4 RVP

Action	Item	Reference Description	Description of Existing Part	Description of New Part
Unstuff	Resistor	R6N37, R6P1, R6N35	RES D,040, 0 OHM,5.00%,1/16 W	NA

Figure 3-143. Schematic Snapshot: TGL UP3 DDR4 RVP

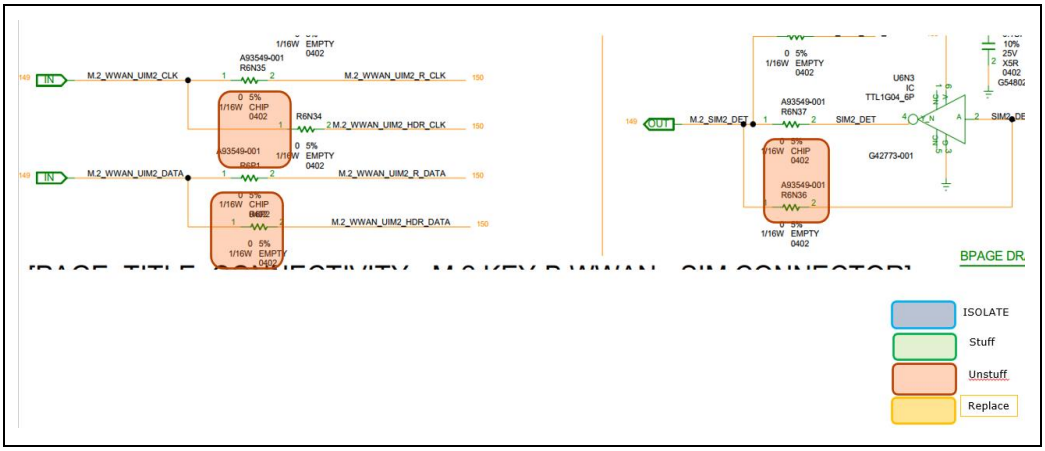


Figure 3-144. Layout Snapshot (Top Layer): TGL UP3 DDR4 RVP

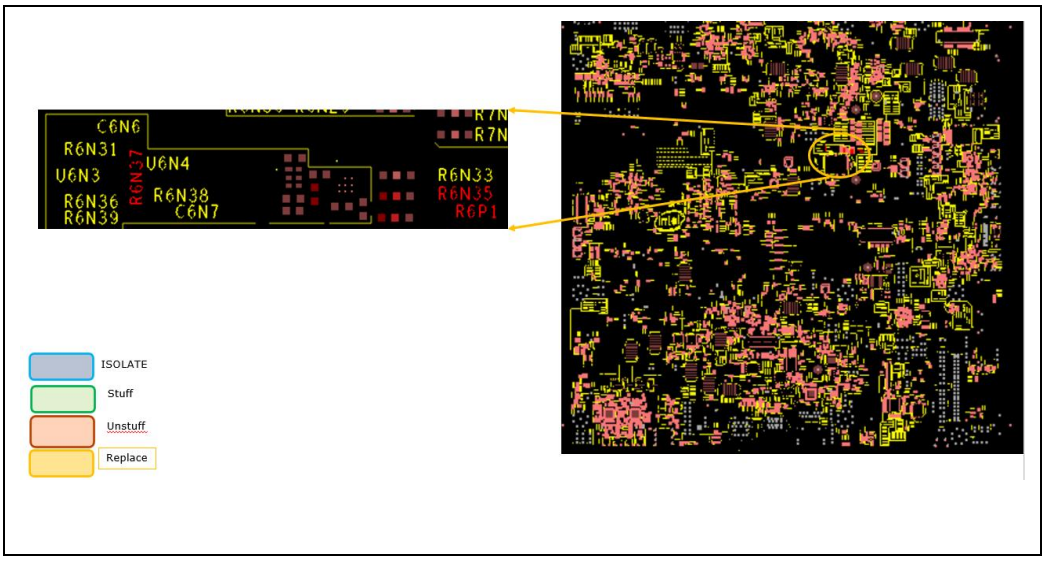


Table 3-74. Reference Designator Comparison

Action	TGL UP3 DDR4	TGL UP3 LPDDR4x RVP
Unstuff	R6N35, R6P1, R6N37	R6N34, R6P1, R6P4

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