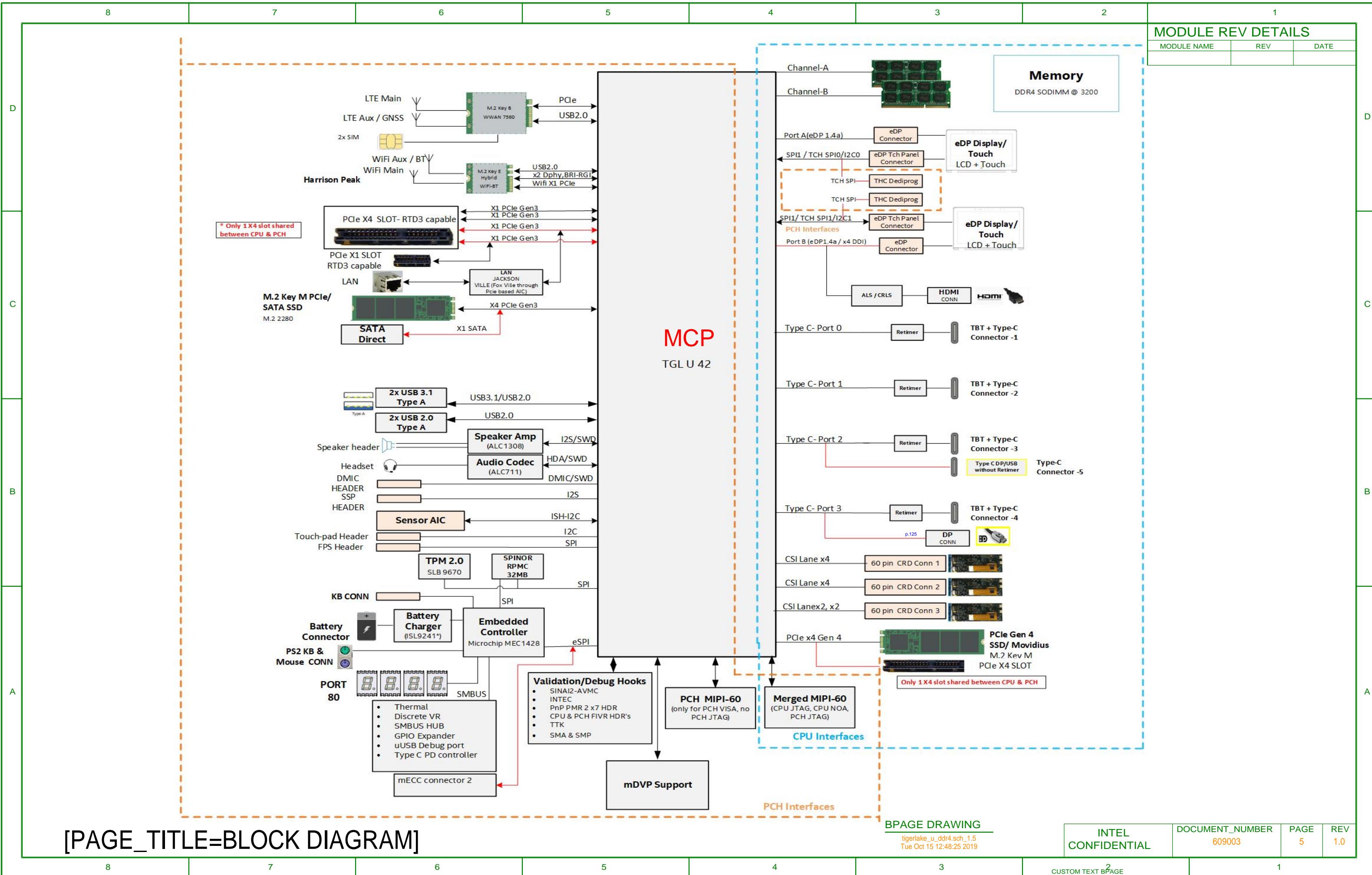


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								MODULE REV DETAILS		
								MODULE NAME	REV	DATE
D	[1. TITLE PAGE] [2. INDEX -1] [3. INDEX -2] [4. INDEX -3] [5. BLOCK DIAGRAM] [6. LED DISCRIPTION] [7. Z0 VS A0 PINLIST] [8. TABLE - MPHYS MAPPING] [9. ALC711 ES1 vs ES2] [10. CLK_SRC MAPPING] [11. JUMPER/SWITCH SETTINGS] [12. TGL-U MCP (1 OF 21) - DISPLAY & TYPE-C (TBT/DISPLAY)] [13. DISPLAY - DDIA - PORT AC CAPS] [14. DISPLAY - DDIB - PORT SHARING, AC CAPS] [15. DISPLAY - TYPE-C PORT 0 SHARING, AC CAPS] [16. DISPLAY - TYPE-C PORT 1 AC CAPS] [17. DISPLAY - TYPE-C PORT 2 AC CAPS] [18. DISPLAY - TYPE-C PORT3 SHARING, AC CAPS] [19. TGL-U MCP (2 OF 21) - MEMORY CHANNEL - A] [20. TGL-U MCP (3 OF 21) - MEMORY CHANNEL - B] [21. TGL-U MCP (4 OF 21) - CPU MISC] [22. TGL-U MCP (5 OF 21) - LSIO - SPI, ESPI, THC, MLINK, SMLINK, SMBUS] [23. TGL-U MCP (6 OF 21) - LPSS - GSPI, UART, I2C, ISH-SPI, ISH UART, ISH I2C, ISH GPIOs] [24. TGL-U MCP (7 OF 21) - AUDIO, SD3.0, DISPLAY MISC] [25. PCH SMBUS EXPANDER, FRU] [26. SHARING OPTIONS - 1 - ESPI, SMLINKS] [27. GPIO - LPSS SHARING OPTIONS - 2 - GSPI, UART] [28. GPIO - LPSS SHARING OPTIONS - 3 - I2C, ISH I2C] [29. GPIO - LPSS SHARING OPTIONS - 4 - I2C] [30. GPIO - SHARING OPTIONS -1 - THC, SPI, UART] [31. GPIO - ISH SHARING OPTIONS -2 - I2C, GPIO] [32. GPIO - OTHER PCH GPIO SHARING OPTIONS - 1] [33. SVID SIGNALS] [34. TGL-U MCP (9 OF 21) - MODPHY] [35. PCIE PORT 0&1 SHARING OPTIONS, AC CAPS] [36. PCIE PORT 2&3 SHARING OPTIONS, AC CAPS] [37. PCIE PORT 4&5 SHARING OPTIONS, AC CAPS] [38. PCIE PORT 6&7 SHARING OPTIONS, AC CAPS] [39. PCIE PORT 8&9 SHARING OPTIONS, AC CAPS] [40. PCIE PORT 10&11 SHARING OPTIONS, AC CAPS] [41. PCIE PORT RESET RTD3 CIRCUIT] [42. PCIE WAKE RTD3] [43. USB2 CMC & SHARING] [44. TGL-U MCP (10 OF 21) - CSI2, CNVI] [45. TGL-U MCP (11 OF 21) - CLOCK SIGNALS] [46. SRC CLOCKS]	[47. CLOCK - CRYSTAL] [48. GPIO - ISH GPIO SHARING OPTIONS - 1] [49. TGL-U MCP (12 OF 21) - SYSTEM POWER MANAGEMENT] [50. SYSTEM POWER MANAGEMENT OPTIONS] [51. PLATFORM RESET BUFFER] [52. TGL-U MCP (13 OF 21) - CPU POWER 1 OF 2] [53. TGL-U MCP (15 OF 21) - CPU POWER 2 OF 2] [54. CPU PDBOM 1 OF 2] [55. CPU PDBOM 2 OF 2] [56. PCH PDBOM 2 OF 2] [57. TGL-U MCP (14 OF 21) - PCH POWER 1 OF 2] [58. RESERVE] [59. PCH PDBOM 1 OF 2] [60. PCH DERIVED RAILS] [61. RESERVED] [62. TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)] [63. TGL-U MCP (19 OF 21) - FIVR DEBUG] [64. CPU FIVR DEBUG HEADER] [65. TGL-U MCP (20 OF 21) - RESERVED SIGNALS] [66. JTAG/CFG - CFG TERMINATIONS] [67. JTAG/CFG - MERGED JTAG OPTIONS] [68. JTAG/CFG - CPU/PCH MERGED MIPI 60 CONNECTOR] [69. JTAG/CFG - PCH DEBUG SHARING OPTIONS] [70. JTAG/CFG - PCH MIPI 60 VISA CONNECTOR] [71. PD AIC CONNECTOR] [72. USBC RSVD]] [73. MECC TRIPAD SHARING] [74. TGL-U MCP(8 OF 21)- RESERVE GENERAL -5] [75. CPU_STRAPS_1] [76. CPU_STRAPS_2]	D							
c										
B									B	
A									A	
	[79. FLEX CONNECTOR] [80. MEMORY - DDR4 SODIMM CHANNEL -A (1 OF 2)] [81. MEMORY - DDR4 SODIMM CHANNEL -A (2 OF 2)] [82. MEMORY - DDR4 SODIMM CHANNEL -B (1 OF 2)] [83. MEMORY - DDR4 SODIMM CHANNEL -B (2 OF 2)] [84. MEMORY - DDR4 SODIMM CHANNEL -A PD BOM] [85. MEMORY - DDR4 SODIMM CHANNEL -BPD BOM] [86. MEMORY - DDR VREF CIRCUITRY -1 - PROCESSOR, OPTIONS] [87. MEMORY - DDR4 SODIMM & LPDIMM CONN PINOUT] [88. MEMORY - DDR VREF CIRCUITRY - 3 - AVMC OPTION] [89. DISPLAY - eDP connector 1 - CMC] [90. DISPLAY - eDP connector 1 - MISC] [91. DISPLAY - eDP connector 1] [92. DISPLAY - EDP CONNECTOR 2 - CMC]									
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8		7	6	5	4	3	CUSTOM TEXT BPAGE	1	1	



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RefDes	LED Description
DS4G1	V1P05_CTRL
DS4G2	VNN_CTRL
DS8H5	S3 STATE
DS8H3	S4 STATE
DS8H4	S5 STATE
DS8H2	DSW STATE
DS8H1	M0/M3 STATE
DS3H1	ME PWR Gate

RefDes	LED Description
DS8H6	CAPS LOCK
DS8H7	NUM LOCK
DS7G1	POWER BUTTON
DS7H1	BAT STATUS LED

RefDes	LED Description
DS8G6	SLP S0 LED
DS8G4	PWRGD
DS8G5	CATERR
DS6G1	C10 GATE
DS6G2	CS INDICATE

RefDes	LED Description
DS9B1	SATA Direct connect DEVSLP
DS9E1	M.2 SSD DEVSLP
DS8G7	SATA ACTIVITY
DS6D1	PCIE LINK DOWN
DS4G4	WLAN
DS4G3	BT
DS7D1	WWAN

Error Type	Error Code	Caps Lock LED (DS9H2)	Scroll Lock LED (DS7G1)	Num Lock LED (DS9J1)
No Error	0	Off	Off	Off
RSMRST_PWRGD_N	1	Off	Off	Flash
PM_SLP_S5_N	2	Off	Flash	Off
PM_SLP_S4_N	3	Off	Flash	Flash
PM_SLP_S3_N	4	Flash	Off	Off
PM_SLP_M_N	5	Flash	Off	Flash
ALL_SYS_PWRGD	6	Flash	Flash	Off
PLT_RST_N	7	Flash	Flash	Flash
DOCK_SYS_PWRGD_N	8	On	On	Flash
SUSWARNB	9	On	Flash	On

Note: KSC Thermal Shutdown is indicated by flashing of Num_Lock and Caps_Lock LEDs alternatively.
DS7G1 acts as led indication for error code in case of any error otherwise works as power button LED

[PAGE_TITLE= LED DISCRIPTION]

BPAGE DRAWING
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

Interface	WHL	TGL
Board ID		
PCIE Gen4 – DEKEL PHY	No	Yes
TYPE C	No	Yes
XTAL_IN	24MHz	38.4MHz
Memory	1 Channel	2 channel
CSI	No	Yes

No.	Changes	WHL	TGL	Status
1	XXDP_COMP	24.9 ohm PU to VCCIO	24.9 ohm PU to VCCIN /+VCC1P05_OUT_FET (default) on extra added pin on one of the spare pins of TGL_A0.	implemented
2	XXDDR_COMP[0]	121 ohm PD	121 ohm PD on Pin DW 49	implemented
3	XXDDR_COMP[1]	80.6 ohm PD	80.6 ohm PD on pin DW47	implemented
STRAP				
4	SVID DISABLE STRAP	J3B1 to 1-2	J3B1 to 1-X	WIP
5	GPPC_F10	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K	WIP
6	GPPC_F0*	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K	WIP

[PAGE_TITLE=Z0 VS A0 PINLIST]

8	7	6	5	4	3	2	1			
							MODULE REV DETAILS			
							MODULE NAME REV DATE			
TGL-U 42 ROW RVP's Mphy Allocation										
PCIe Controller		Lane #	Flex IO		HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 3 (SV SKU)			
x4 Controller 1		Lane 0	PCIE3_1_USB31_1							
		Lane 1	PCIE3_2_USB31_2							
		Lane 2	PCIE3_3_USB31_3							
		Lane 3	PCIE3_4_USB31_4							
x4 Controller 2		Lane 4	PCIE3_5		Lane 0 for x4 PCIe slot		x4 PCIe Slot			
		Lane 5	PCIE3_6		Lane 1 for x4 PCIe slot					
		Lane 6	PCIE3_7_LAN_0A_UFS_00		Jacksonville Gbe LAN					
		Lane 7	PCIE3_8_LAN_0B_UFS_01		x1 PCIe Slot					
x4 Controller 3		Lane 8	PCIE3_9_LAN_0C_UFS_1_00		M.2 Key M x4 SSD(Lane reversal for x4 PCIe)	SATA Direct Connect	HSIO Connector			
		Lane 9	PCIE3_10_UFS_1_01							
		Lane 10	PCIE3_11_SATA_0							
		Lane 11	PCIE3_12_SATA_1							
x4 Controller 4 (Gen 4 North side)		CPU Lane0	CPU_PCIE_0		M.2 Key M x4 SSD	x4 PCIe Slot				
		CPU Lane1	CPU_PCIE_1							
		CPU Lane2	CPU_PCIE_2							
		CPU Lane3	CPU_PCIE_3							

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

D	RefDes	Jumper Description	Default
	J1A3	MIPI60 OVERRIDE N	'1-X'
	J2H3	MIPI60 PRESENT1 N	'1-X'
	J1C1	TYPEC DISABLE	'1-X'
	J1F3	NO REBOOT STRAP	'1-X'
	J1F4	FLASH DESCRIPTOR SECURITY OVERRIDE STRAP	'1-X'
c	J3B1	SVID DISABLE STRAP	'1-X'
	J1F4	A0 PERSONALITY STRAP	'1-X'
	J3H1	DDI3 HPD	'1-X'
	J9J5	BT RF KILL N, WIFI RF KILL N	'1-X,3-X'
	J9J4	CNVI Disable	'1-2'
	J5U1	TOUCH PANEL POWER SUPPLY GENERATION	'1-2'
	J8J3	PROCHOT EC JPR	'1-X'
	J9J3	SMC_RST_N JPR	'1-X'
	J9J2	SMC_LID JPR	'1-X'
	J8D2	SVID CLOCK	'1-2,3-X'
	J8D3	SVID ALERT	'1-2,3-X'
	J8D4	SVID DATA	'1-2,3-X'
	J8G3	PCH GLITCH ISSUE MITIGATION	'1-X'
	J7G1	SRTC/RTC CLEAR CMOS JPR	'1-X'
	J7H2	SPD_PRSNT JPR	'1-2'
	J8H3	FRU SMB CLK S3	'1-2'
	J8H5	FRU SMB DATA S3	'1-2'
	J6J1	PECI_MUX_CTRL_SNI_R	'1-X'
	J8J1	FRU POWER SUPPLY	'1-2'
	J6G4	H_PECI_CPU JPR	'1-X'

D	RefDes	Jumper Description	Default
	SW4V1	MIPI60 FN[0:3]	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
c	SW5V1	1 - VDDQ_VR_PWRGD - IMVP_VR_EN 2 - ALL_SYS_PWRGD - IMVP_VR_EN 3 - SATAXPCIE_0_SATAGP_0_R 4 - BIOS_REC	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
	SW6J2	1 - EC_SHD_CS_SW 2 - NC 3 - RETIMER_BYPASS_STRAP 4 - ESPI_TESTCRD_DET	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
	SW9C1	1 - BUF_PLT_RST_1.8 - WF_CAM_RST_N 2 - WF_CAM_RST_ND - WF_CAM_RST_N 3 +V1.8A - XTAL_SEL1_J 4 +V3.3A - XTAL_IN_J	1-8(OFF); 2-7(ON); 3-6(OFF); 4-5(OFF)
	SW8W1	1 - PNP_NPNP_SKU 2 - VIRTUAL_DOCK_DET_N 3 - VIRTUAL_BATTERY 4 - FLIP_TO_TABLET_MODE	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)

[PAGE_TITLE=JUMPER/SWITCH SETTINGS]

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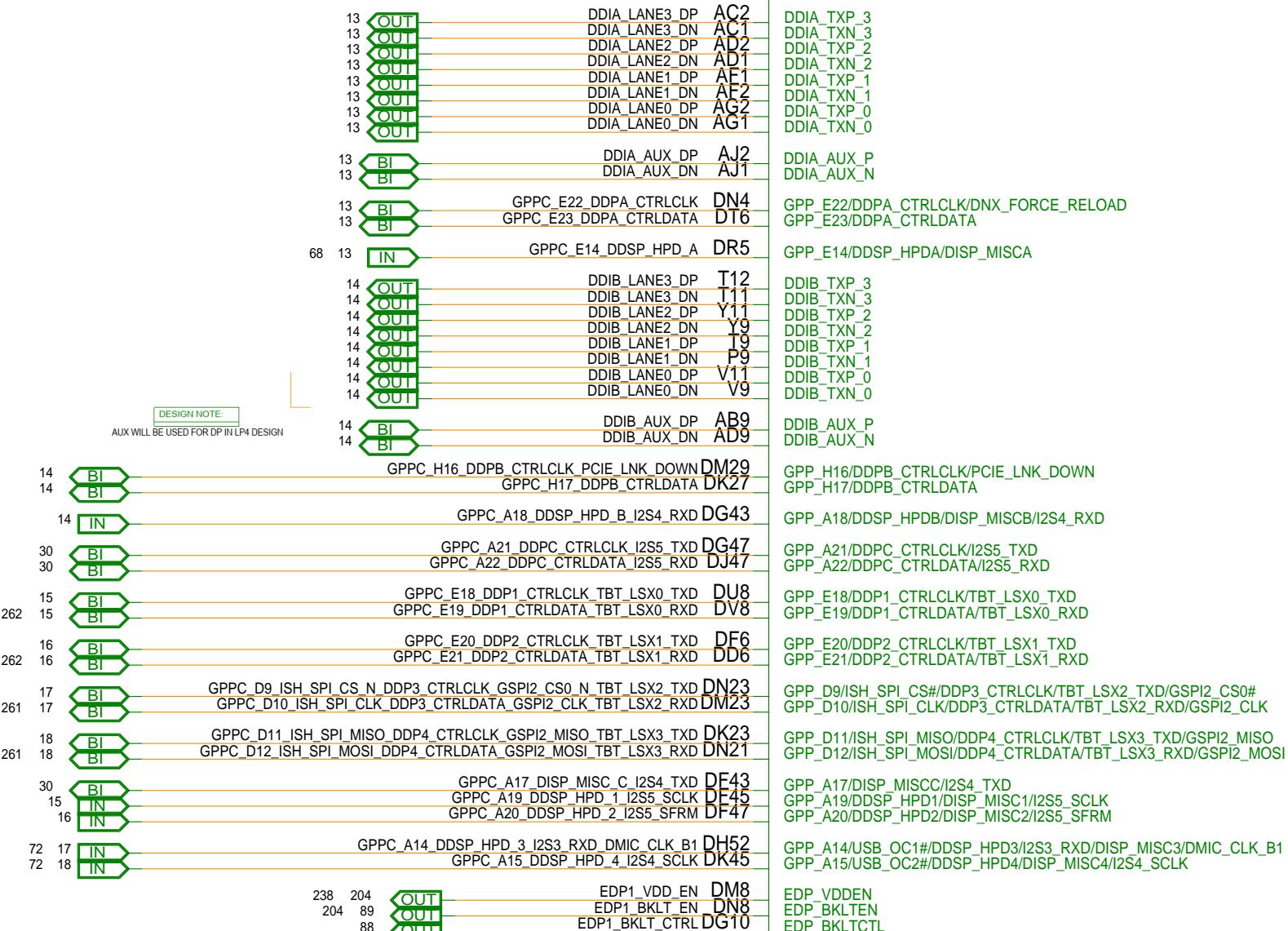
MODULE NAME	REV	DATE

D

D

U4E1
SOC1.6
BGA
TGL_UP3_IP_EXT

1 OF 21

DESIGN NOTE:
AUX WILL BE USED FOR DP IN LP4 DESIGN

DESIGN NOTE:

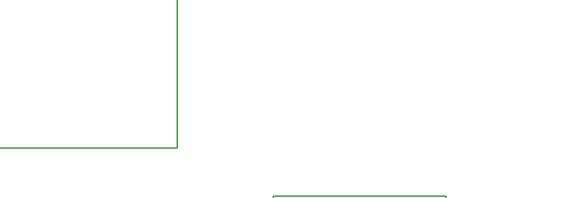
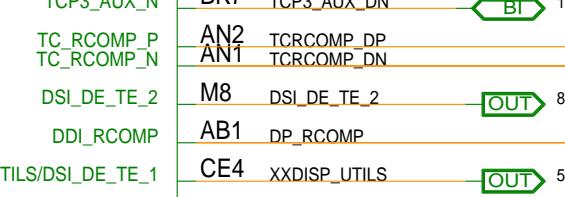
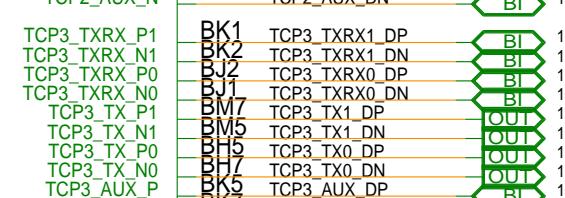
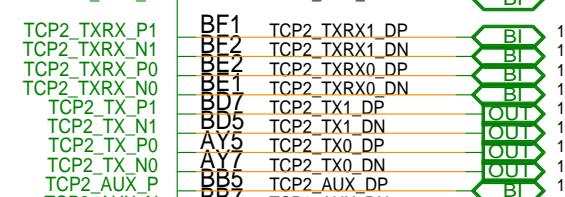
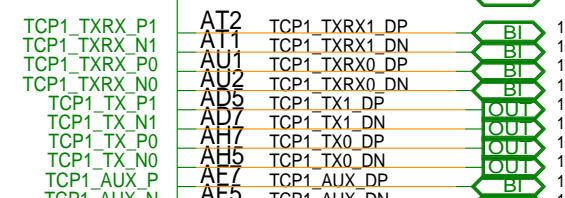
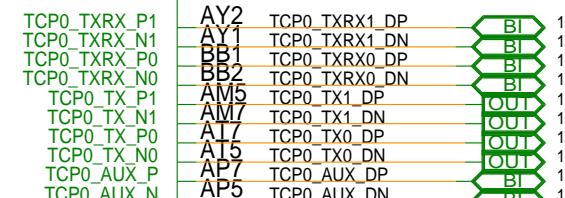
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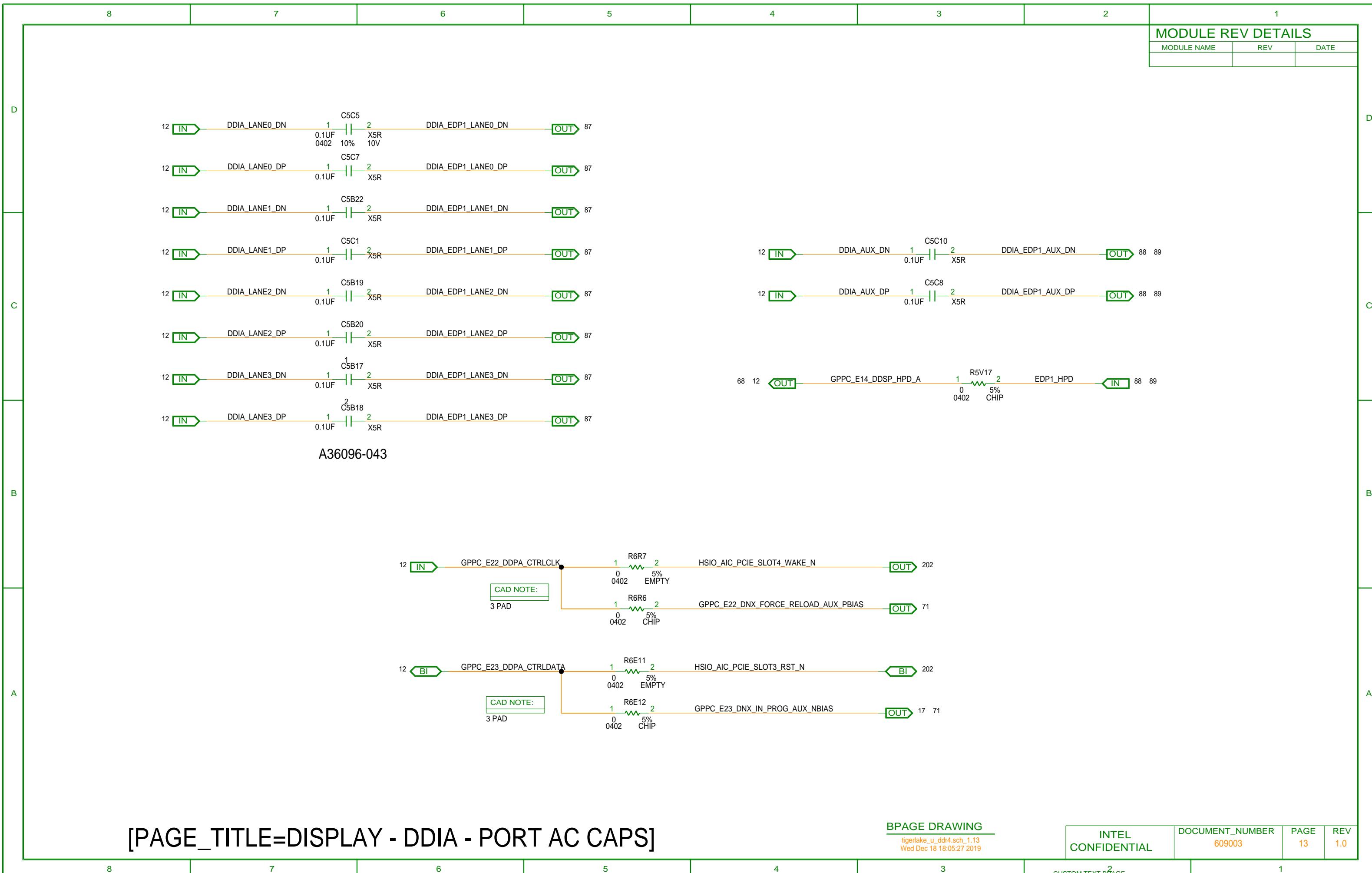
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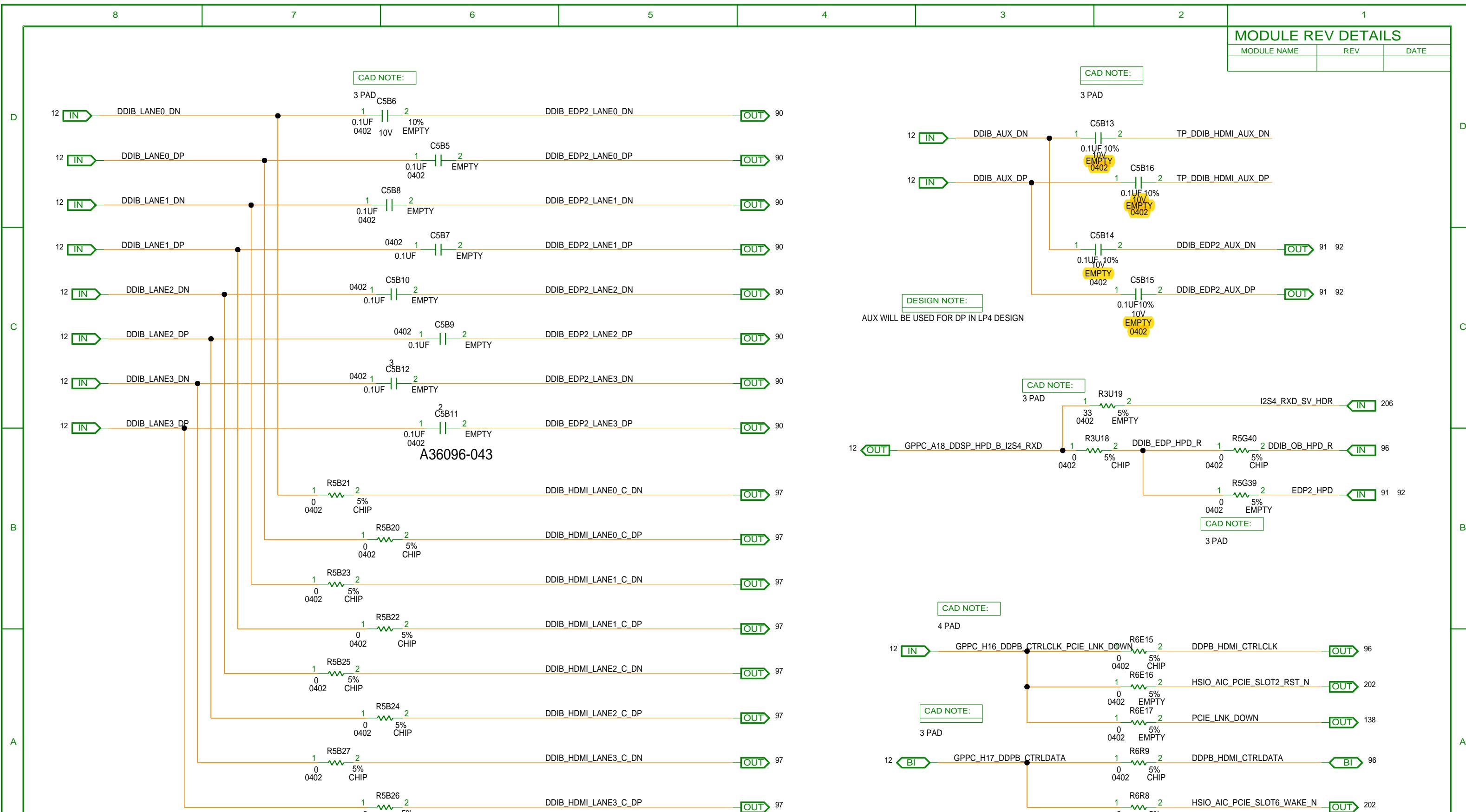
LSX_A:BSSB RXD, LSX_B:BSSB TXD

LPID6529

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

DESIGN NOTE:
GPPC_A17=VDDEN, GPPC_A21=BKLT_EN & GPPC_A22=BKLT_CTRLR4D17
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1%
1/16W
CHIP
A93548-005R4D17
150
1%
1/16W
CHIP
0402
A93548-005

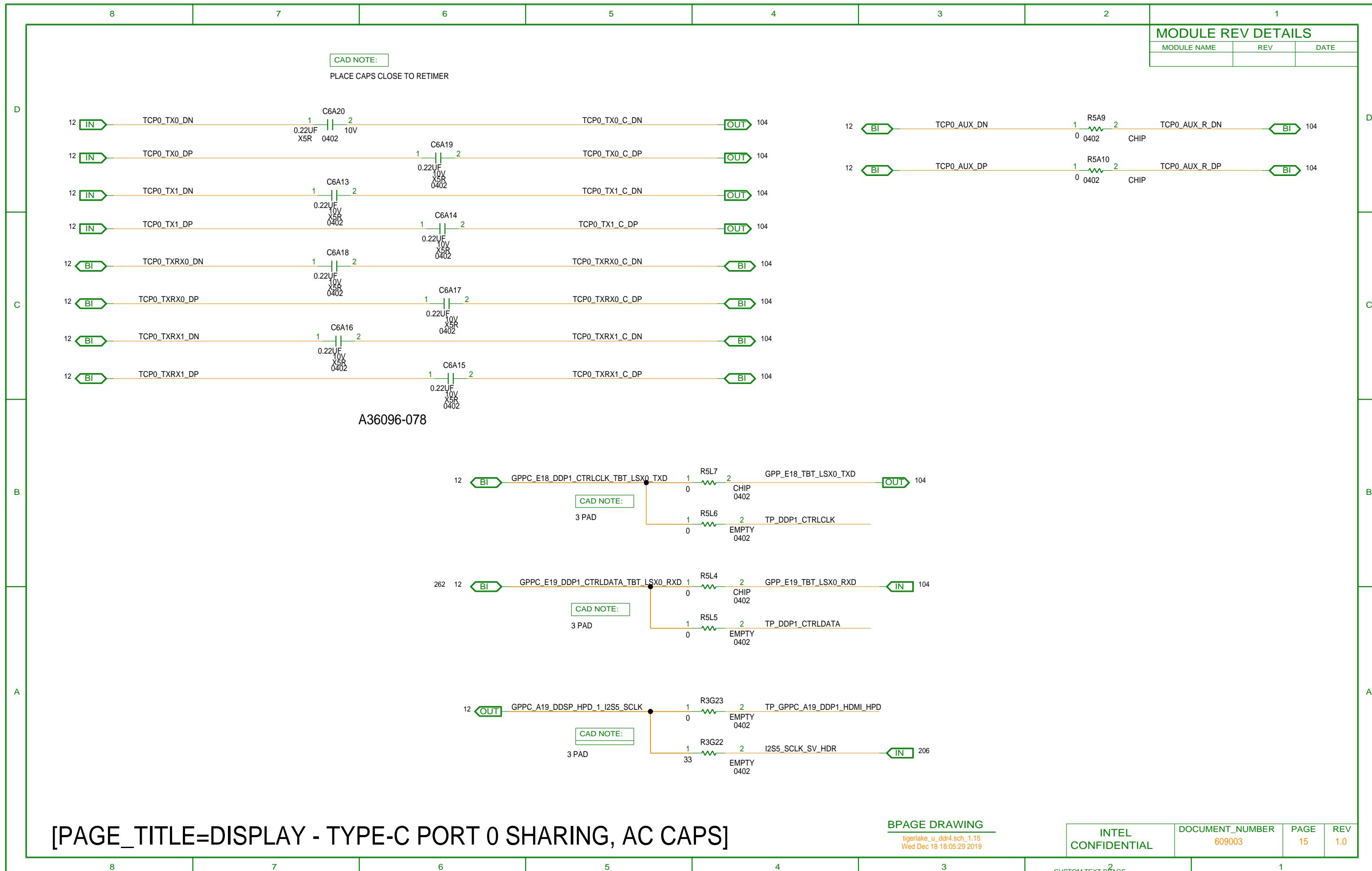


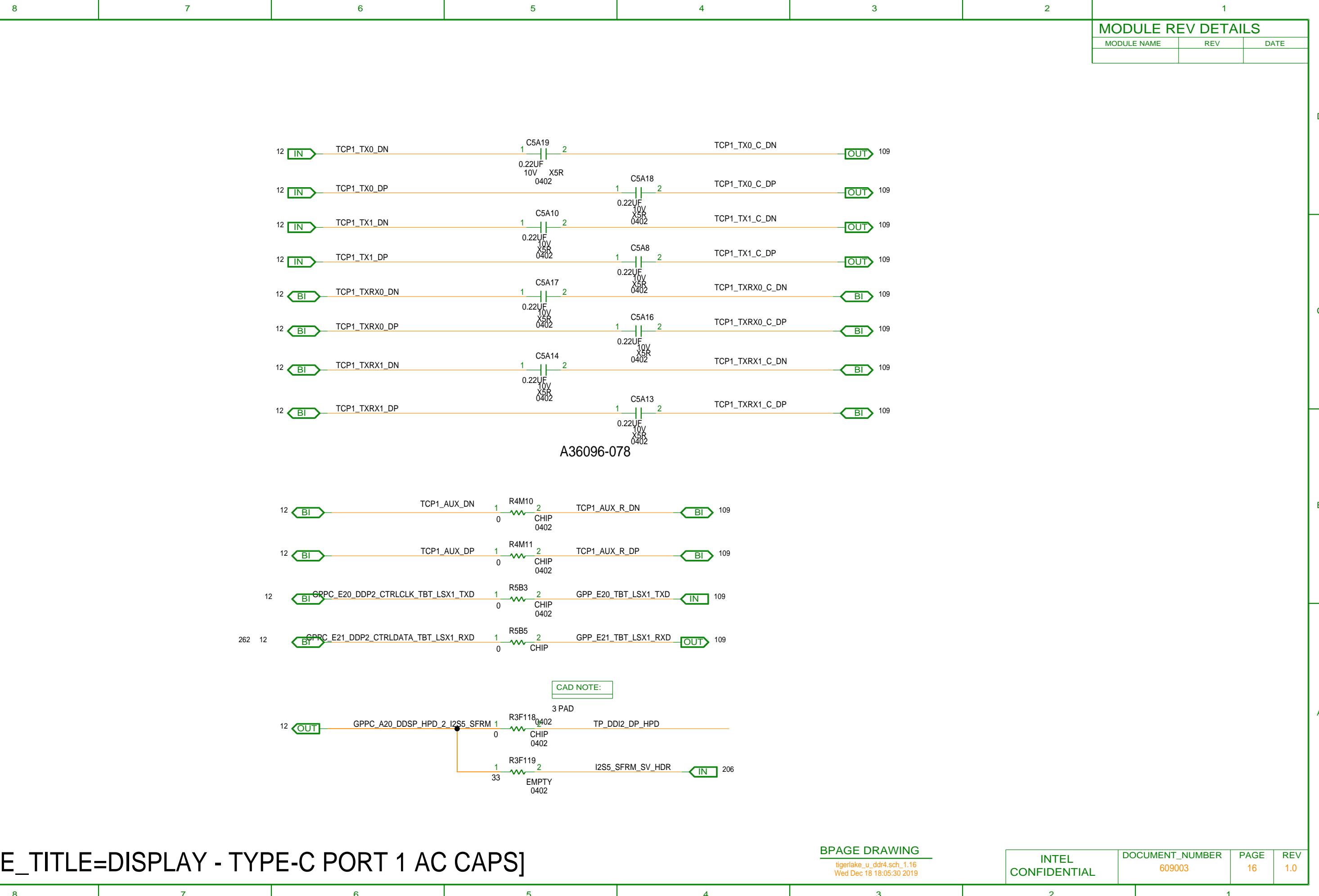


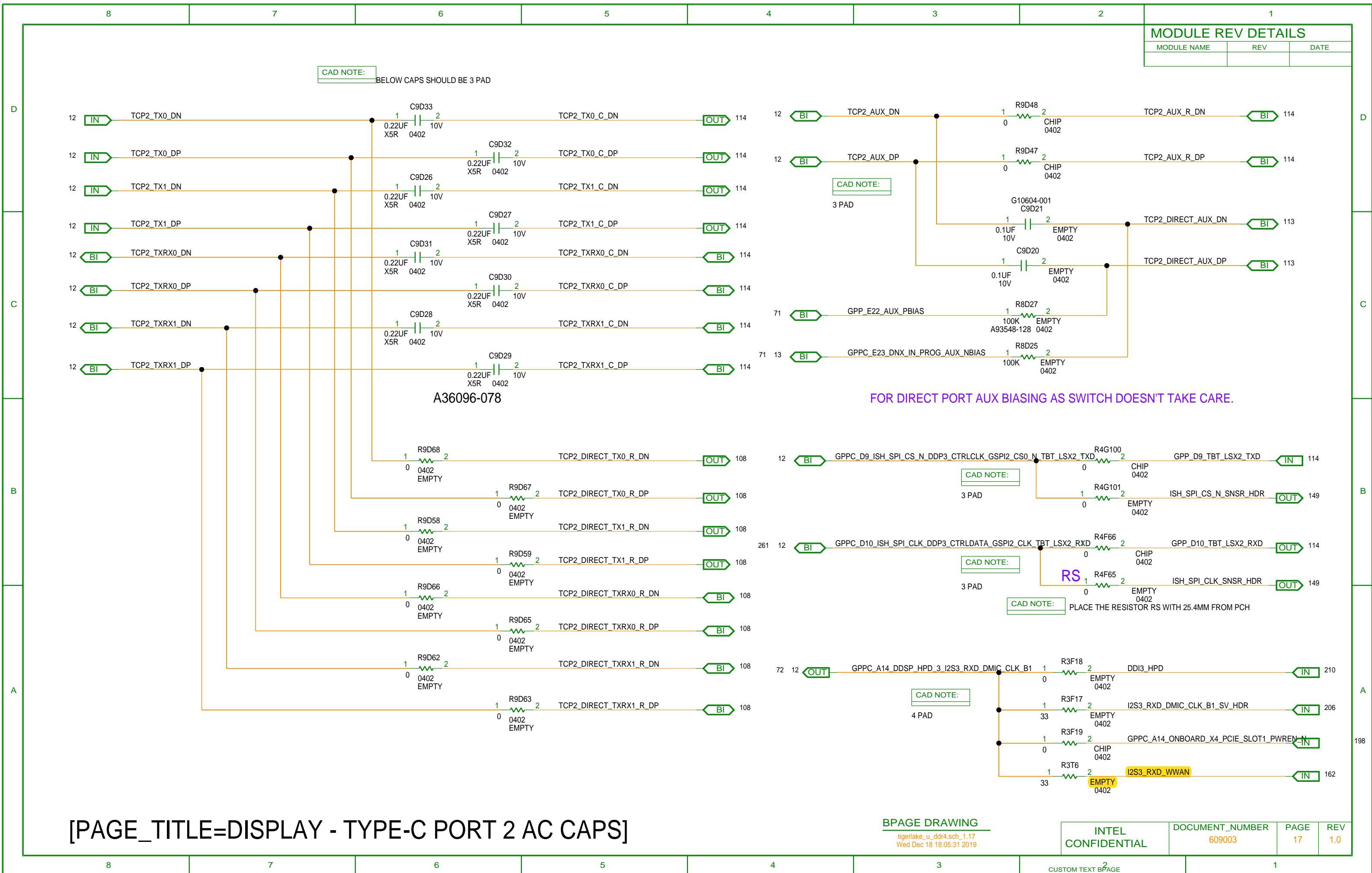
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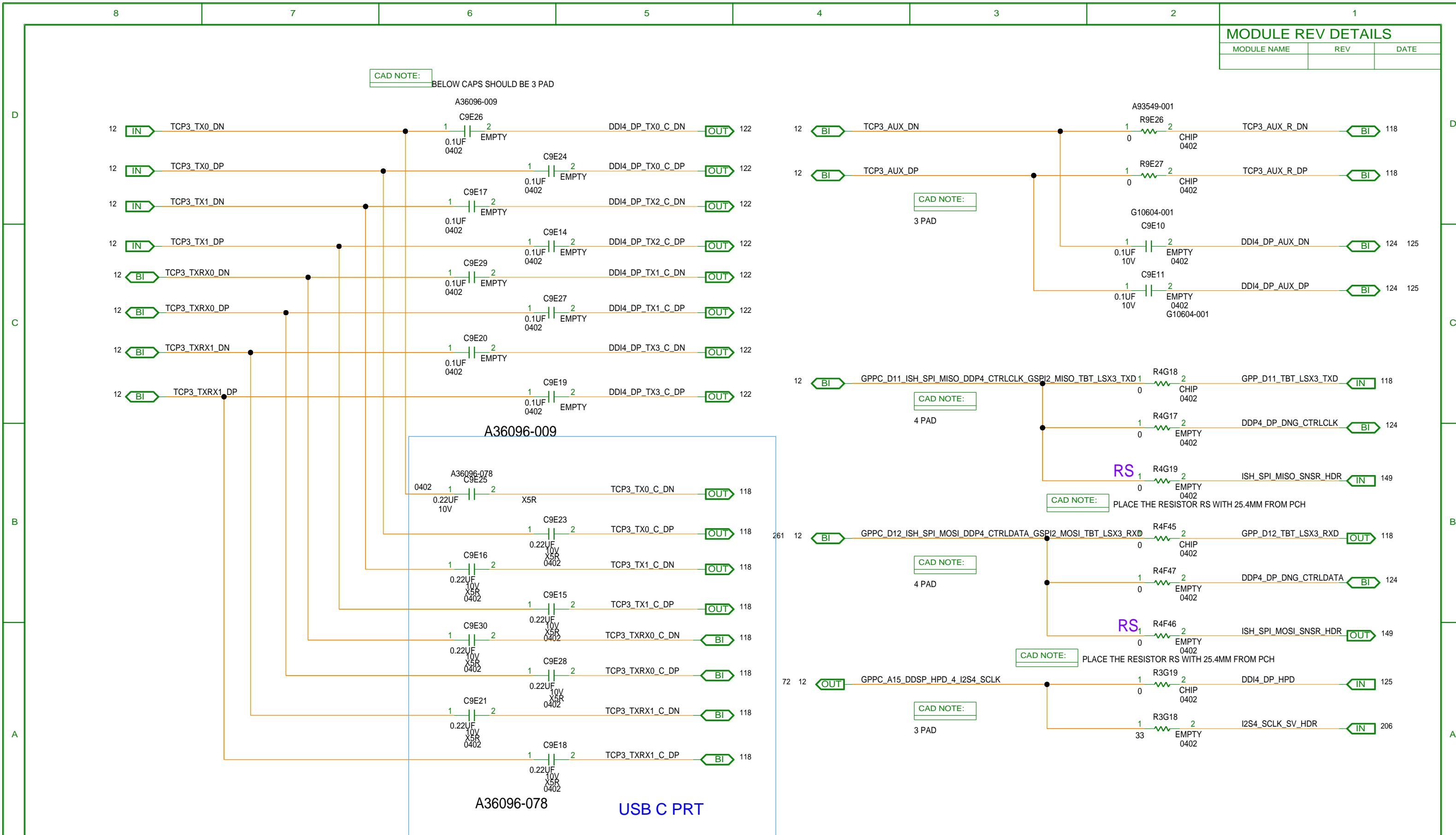
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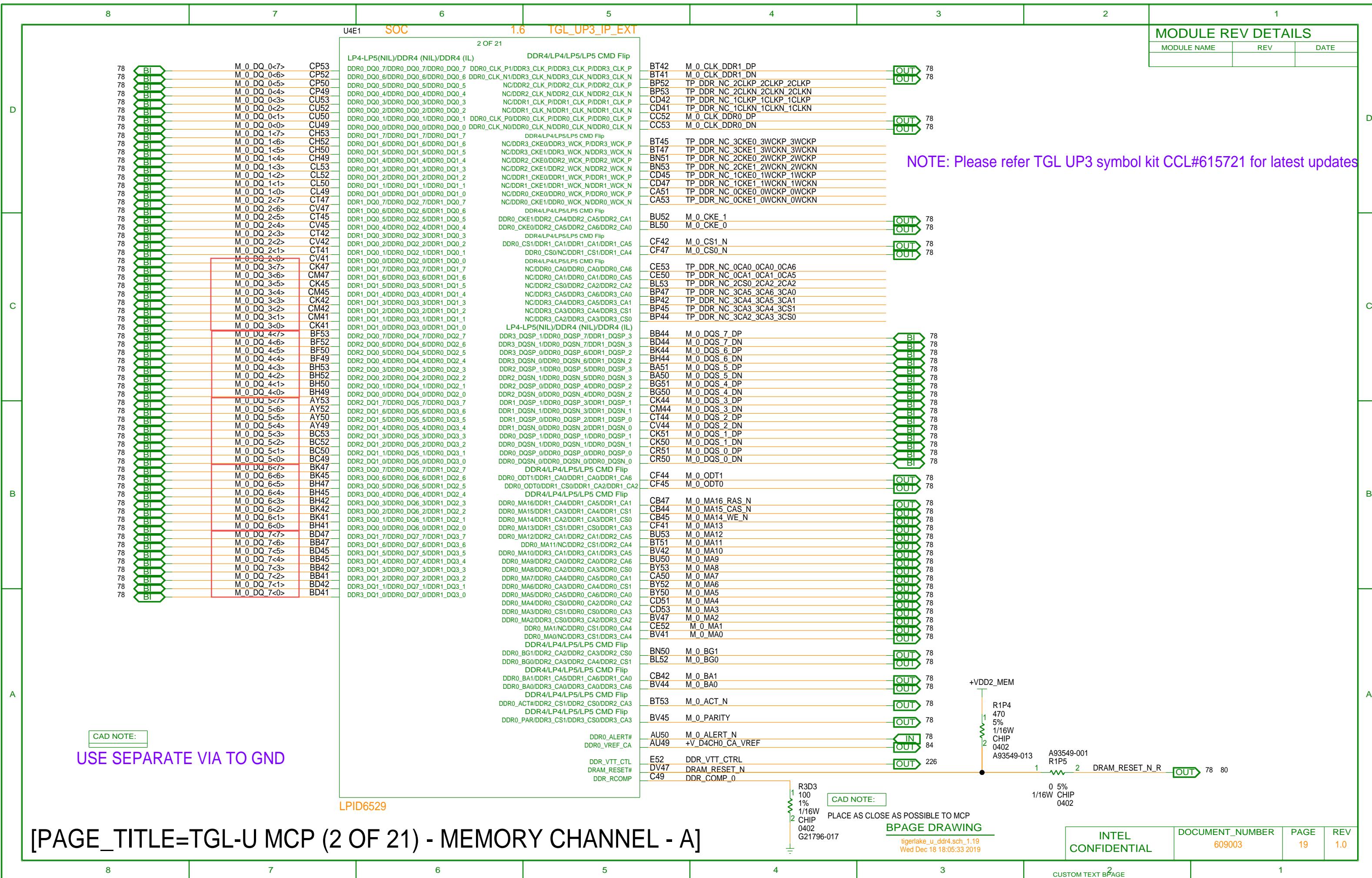
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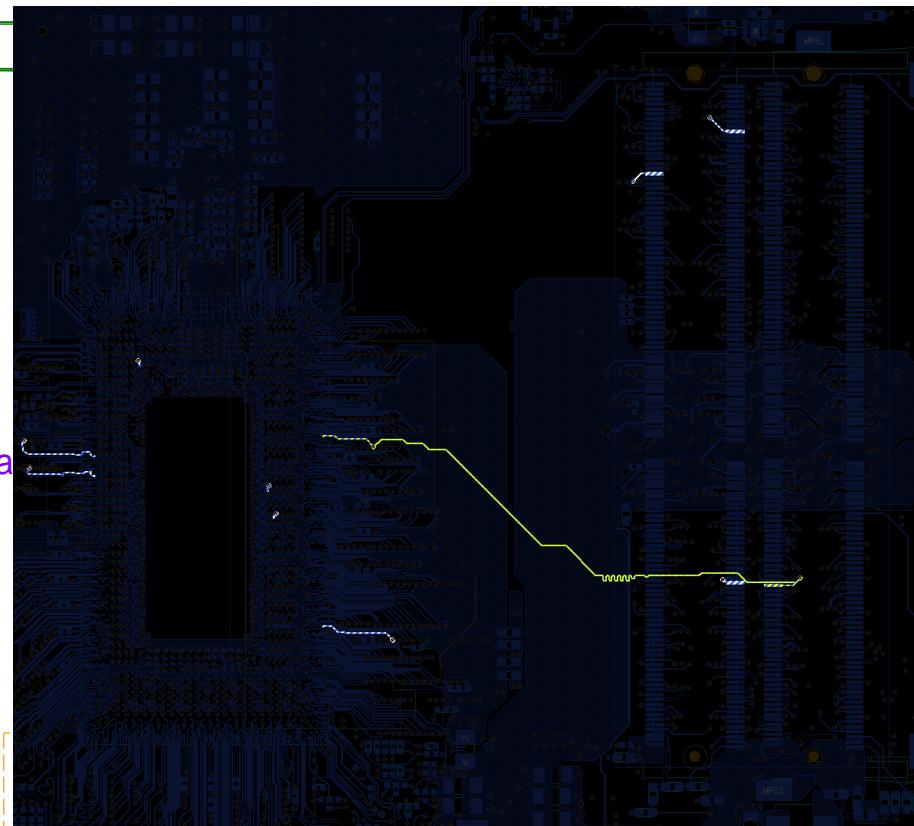
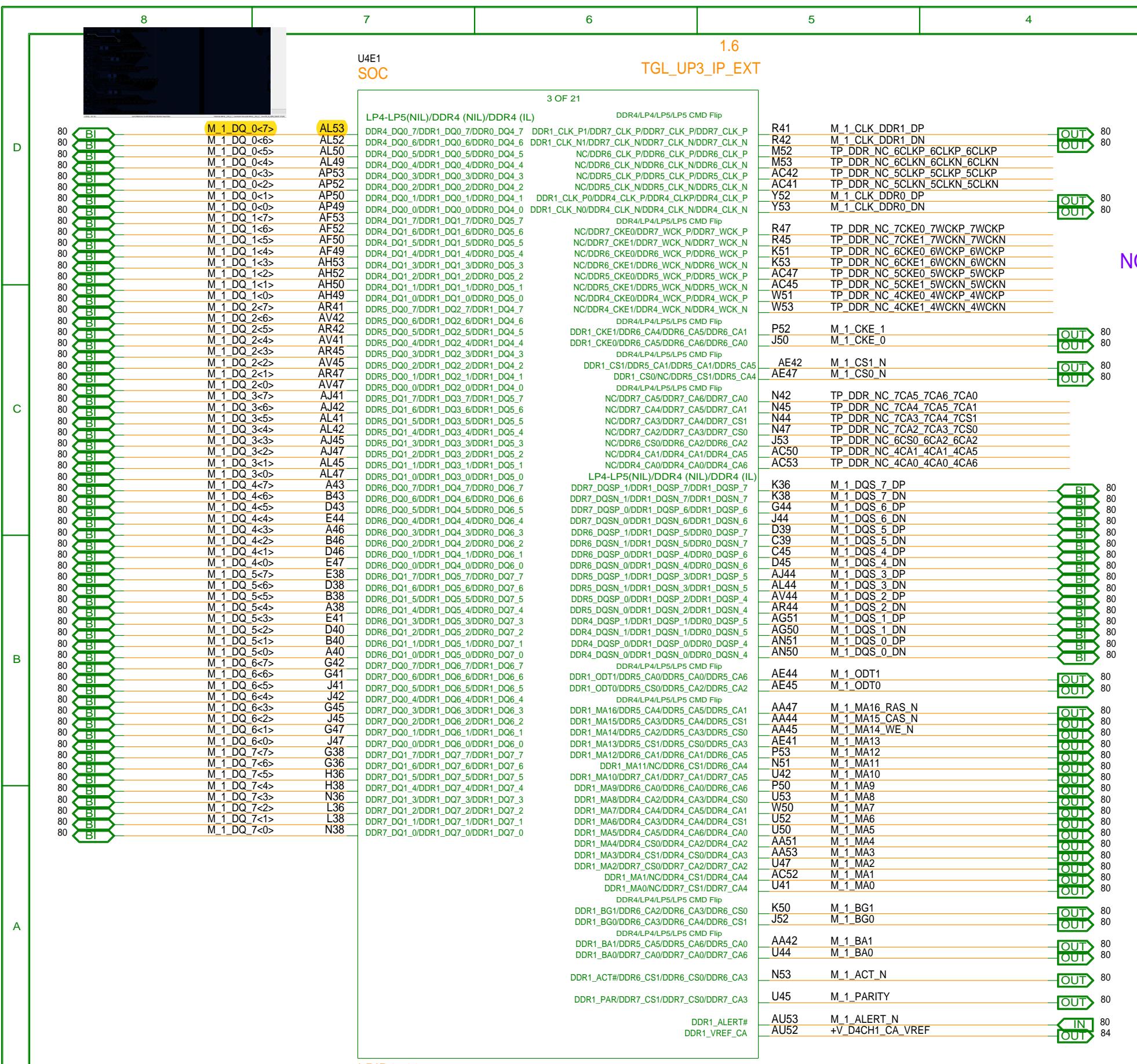






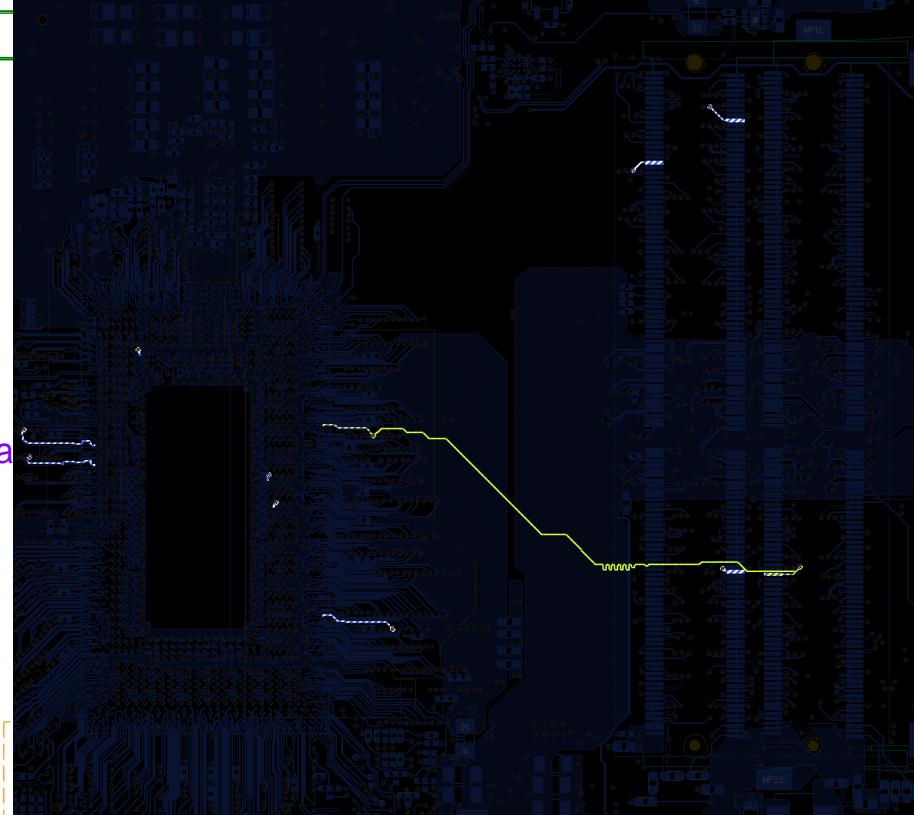




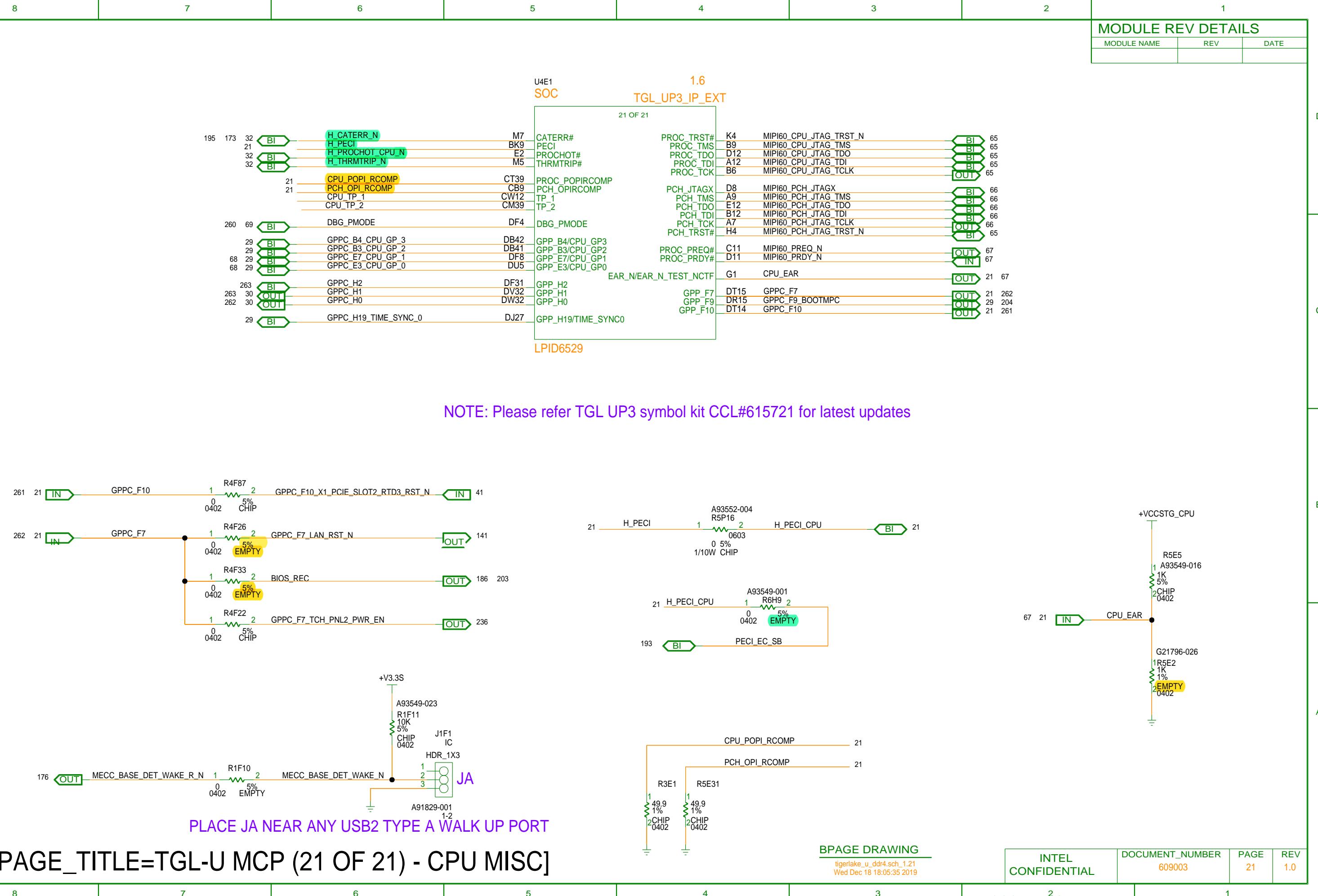


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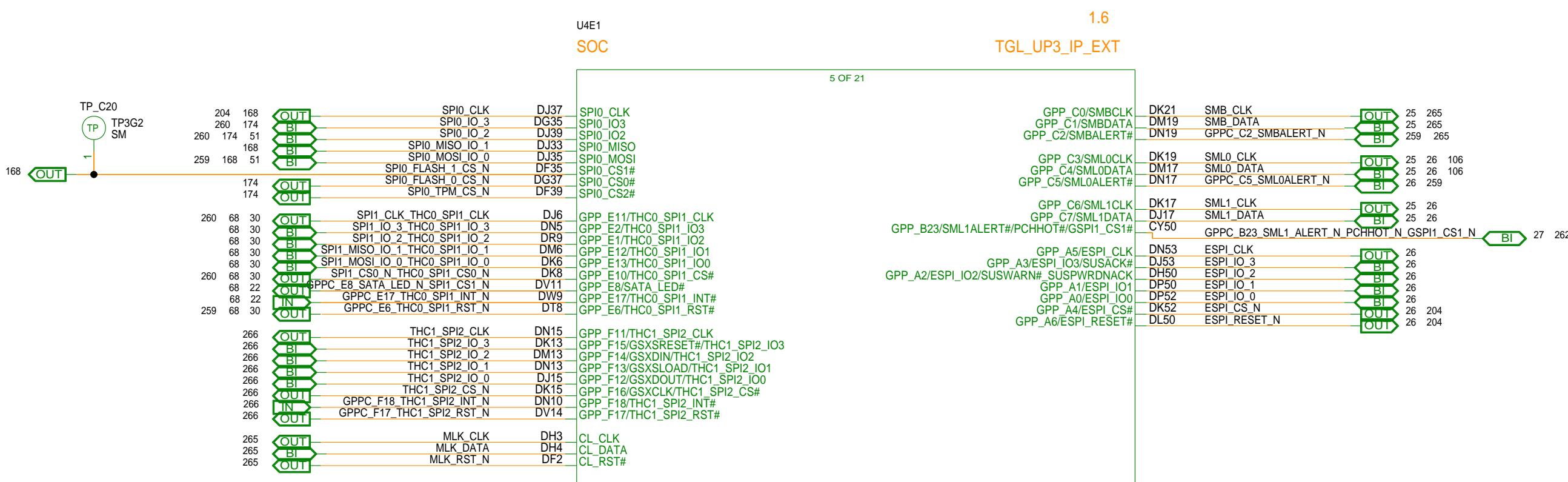
1.6 U4E1
TGL UP3 IP EXT SOC



[PAGE TITLE=TGLU MCP (3 OF 21) - MEMORY CHANNEL - B]



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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

CAD NOTE:
PLACE CLOSE TO J5U2CAD NOTE:
3 PAD WITH R4V4CAD NOTE:
FOR ALL SIGNALS IN THIS PAGE, PLEASE OPEN THE VIA MASKS NEAR TO PCH BREAKOUT FOR PROBING

68 22 IN GPPC_E8_SATA_LED_N SPI1_CS1_N 1 R4V5 2 GPPC_E8_SATA_LED_N SPI1_CS1_R_N OUT 30

0 0402 5% CHIP

68 22 IN GPPC_E17_THCO_SPI1_INT_N 1 R5V27 2 GPPC_E17_THCO_SPI1_INT_R_N OUT 30

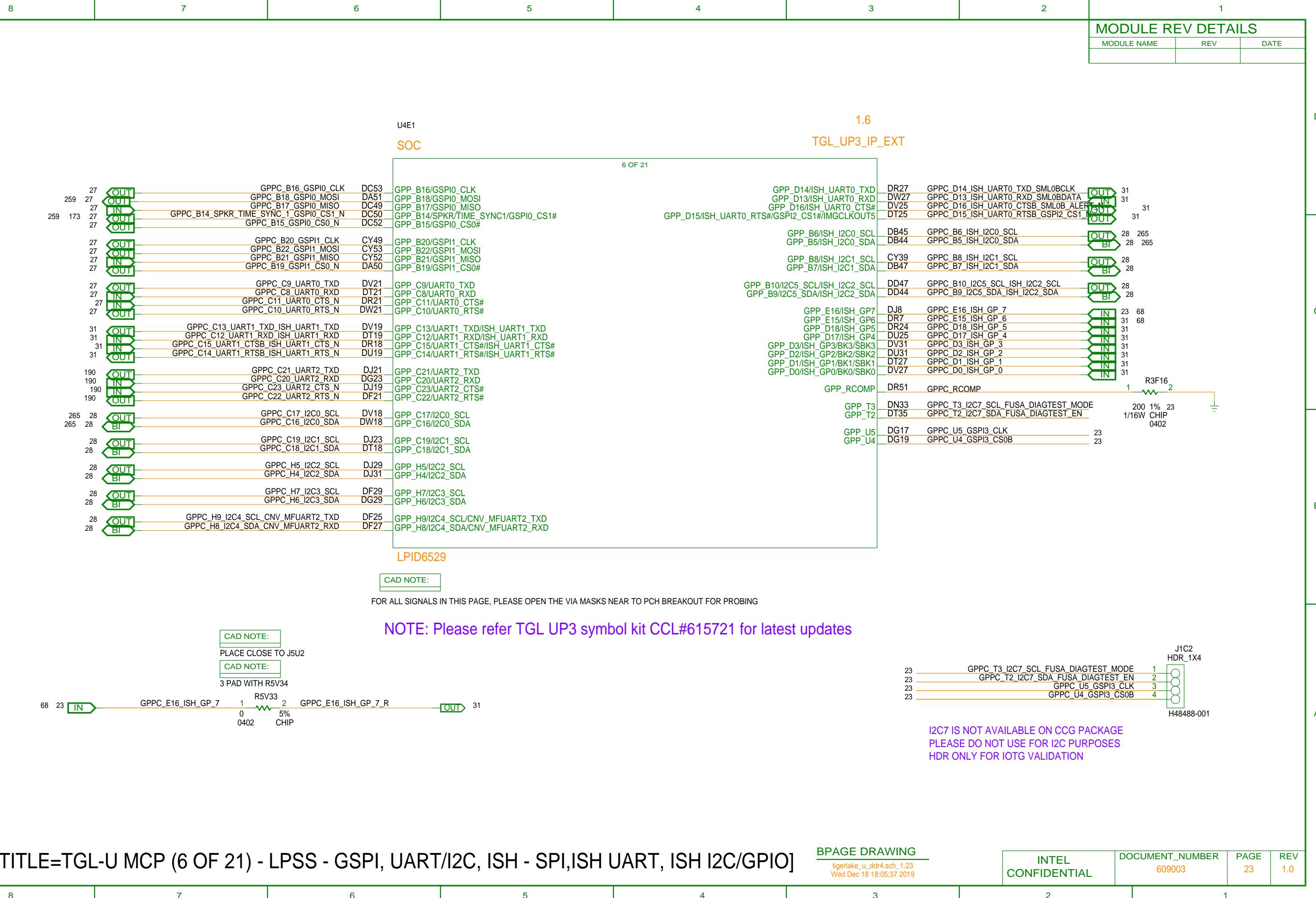
0 0402 5% CHIP

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL-U MCP (5 OF 21) - LSIO - SPI, ESPI, THC, MLINK, SMLINK, SMBUS]

BPAGE DRAWING
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Wed Dec 18 18:05:36 2019

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609003	22	1.0	



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MODULE NAME		REV	DATE				

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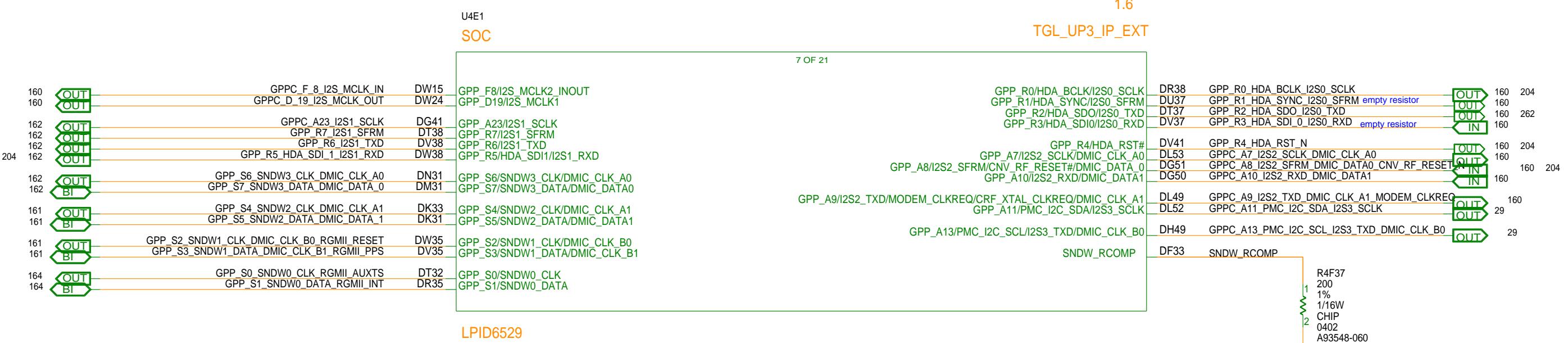
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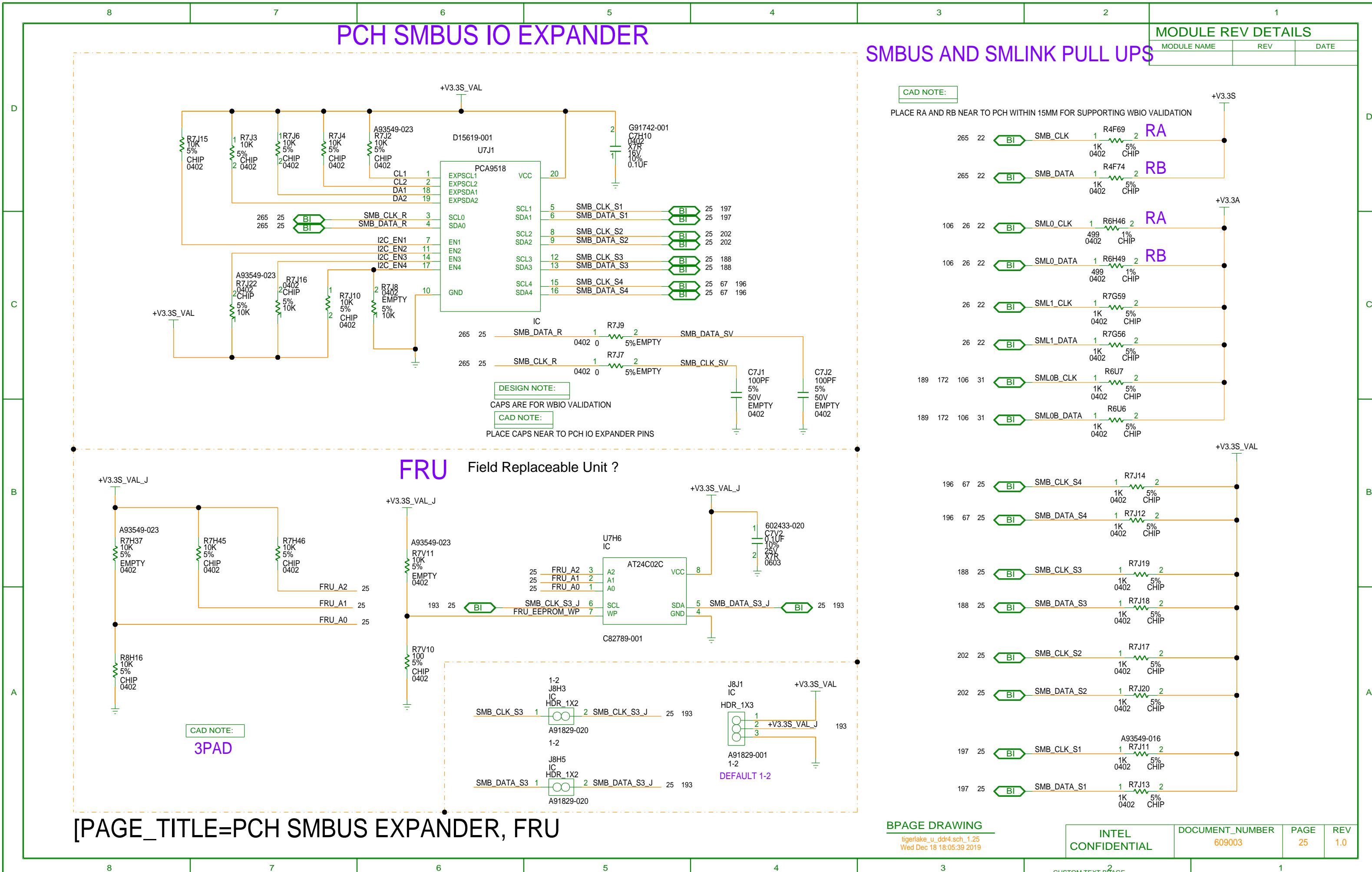
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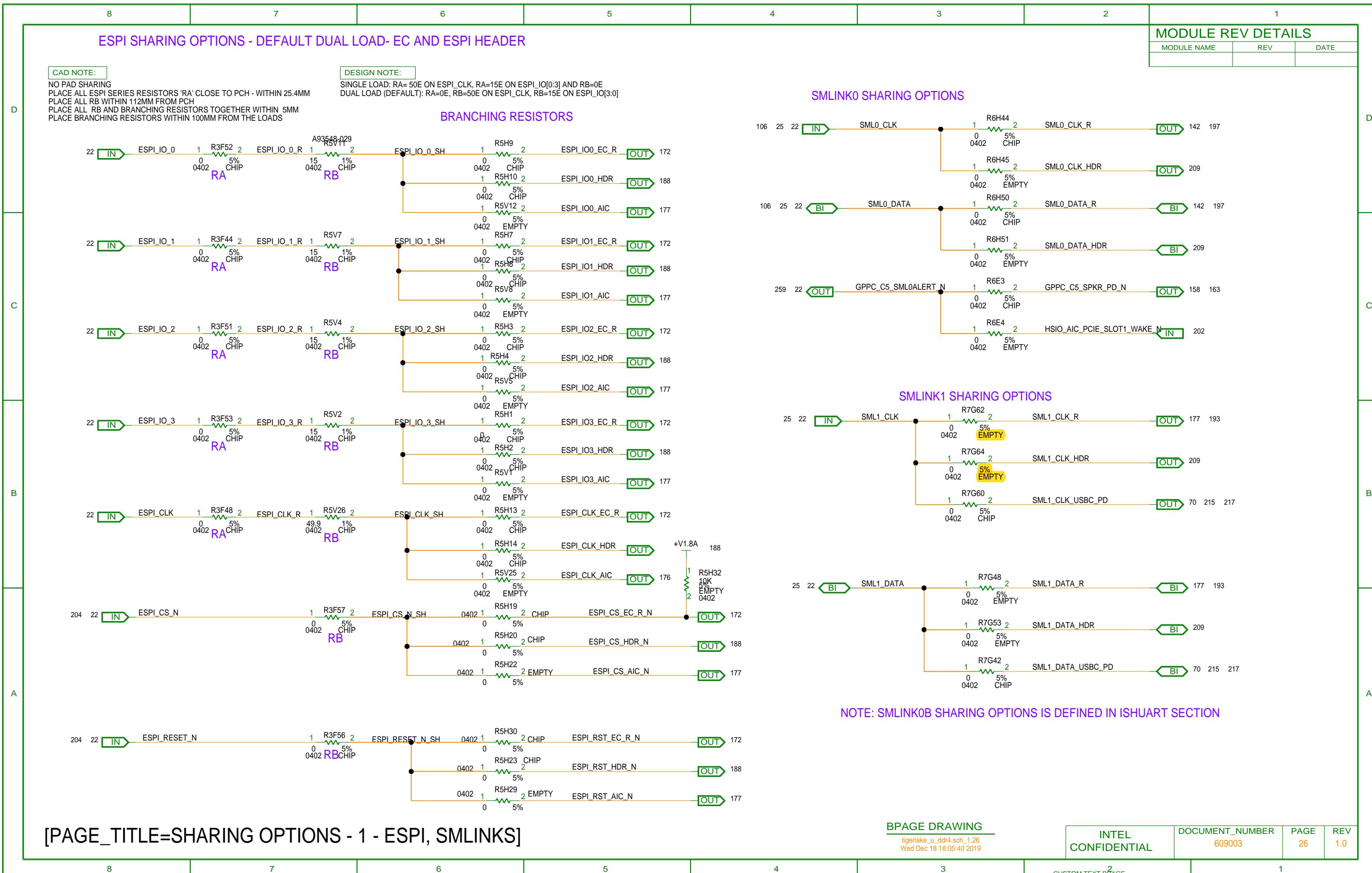
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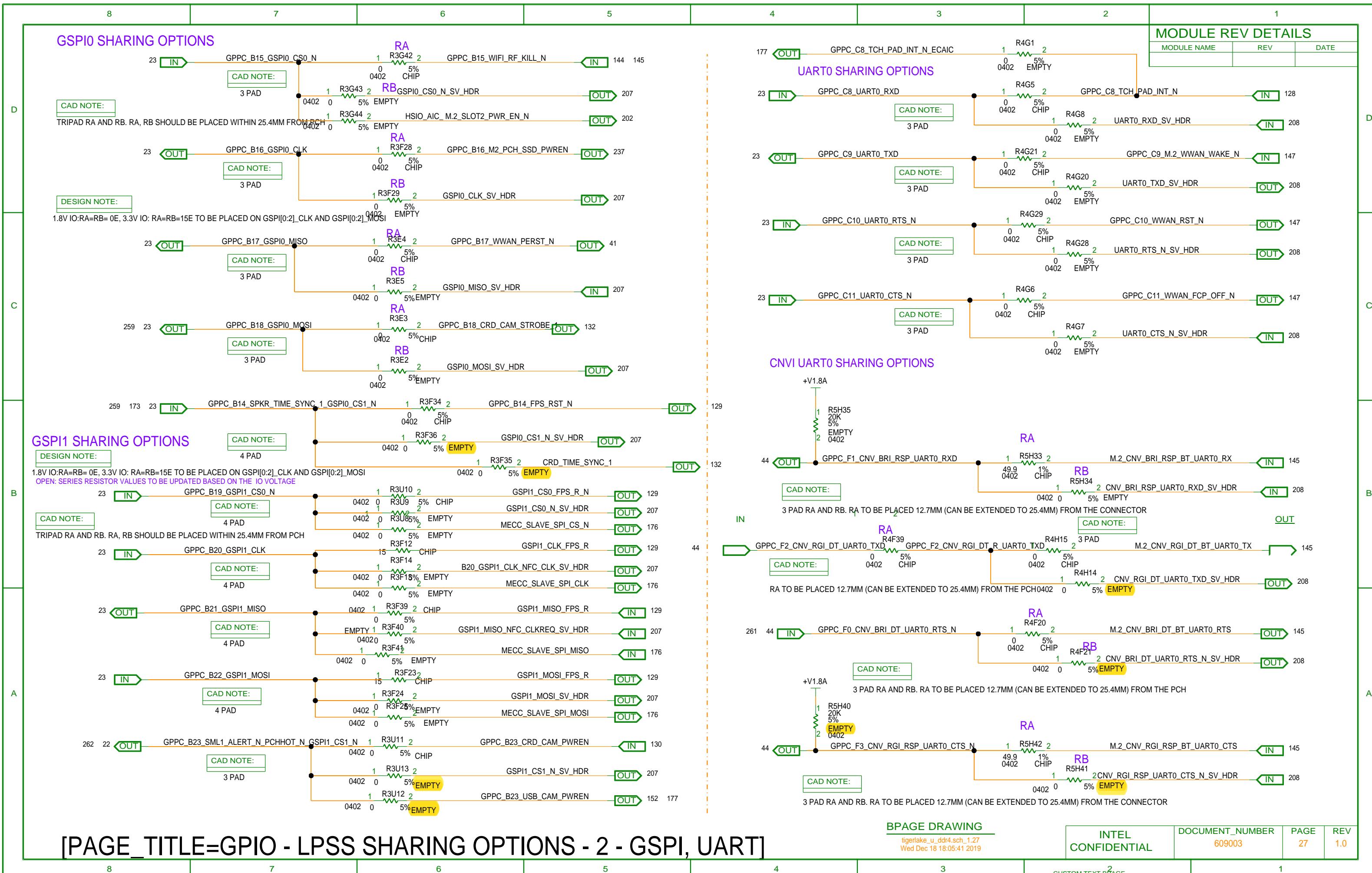
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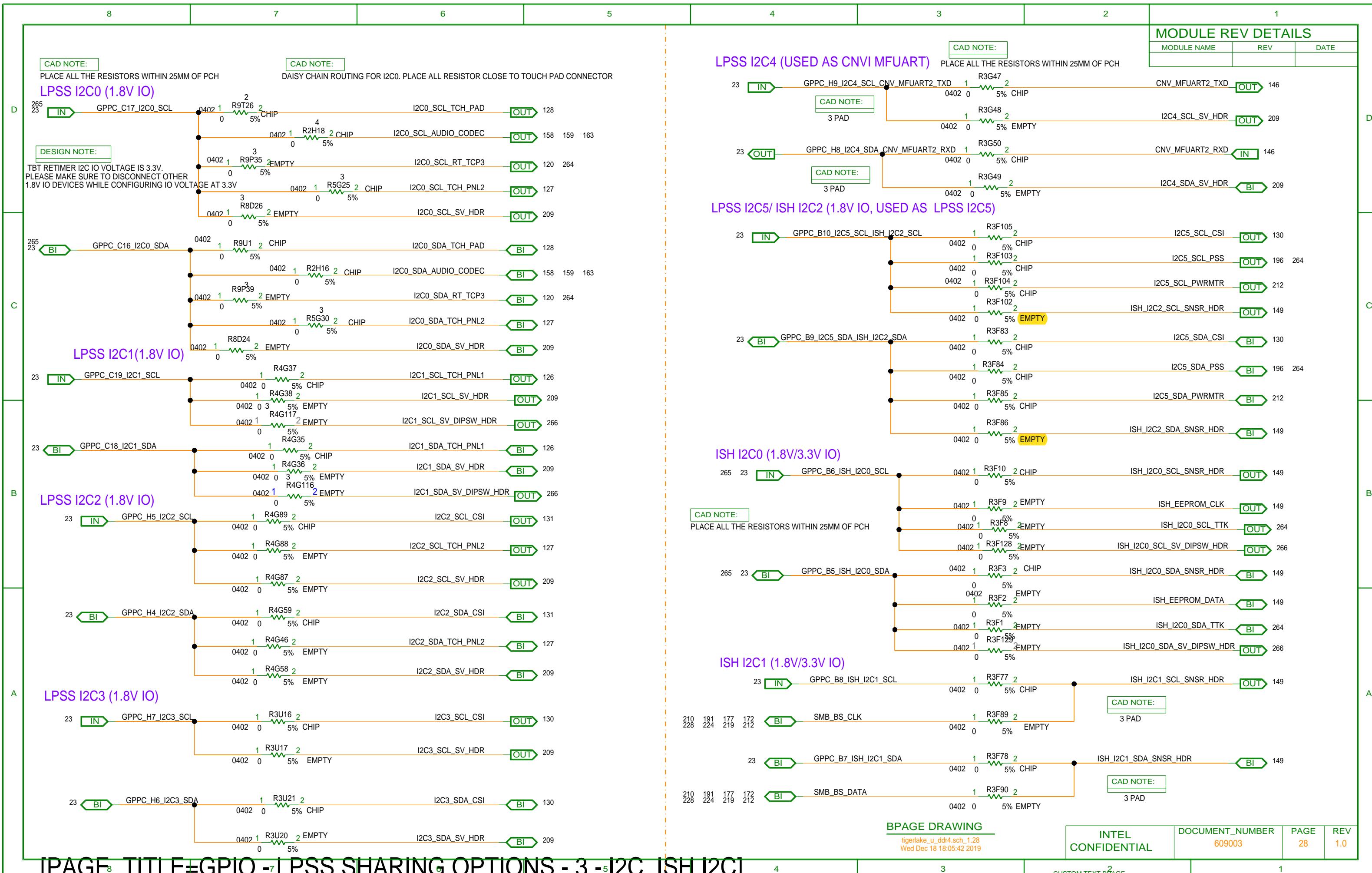


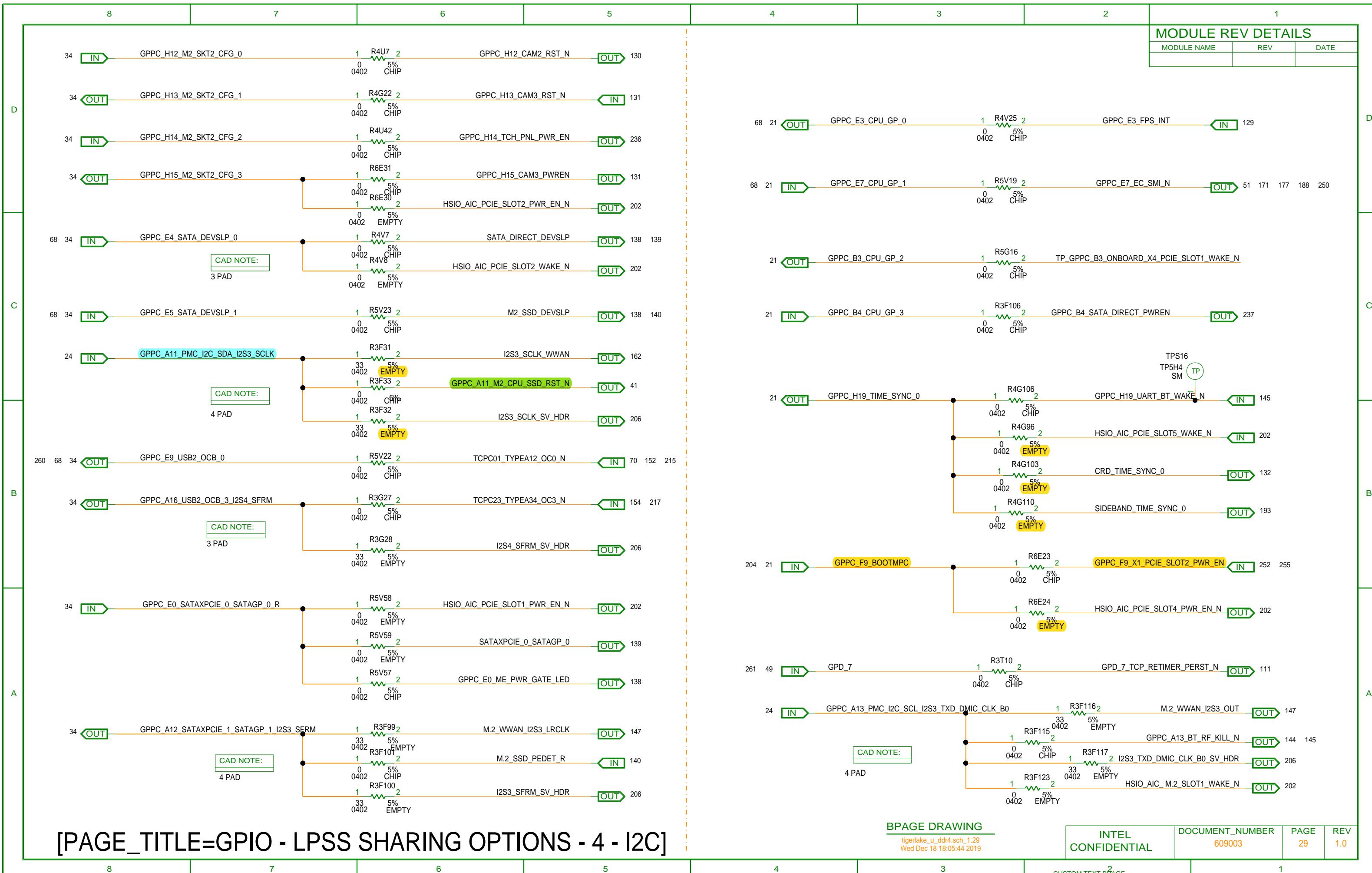
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

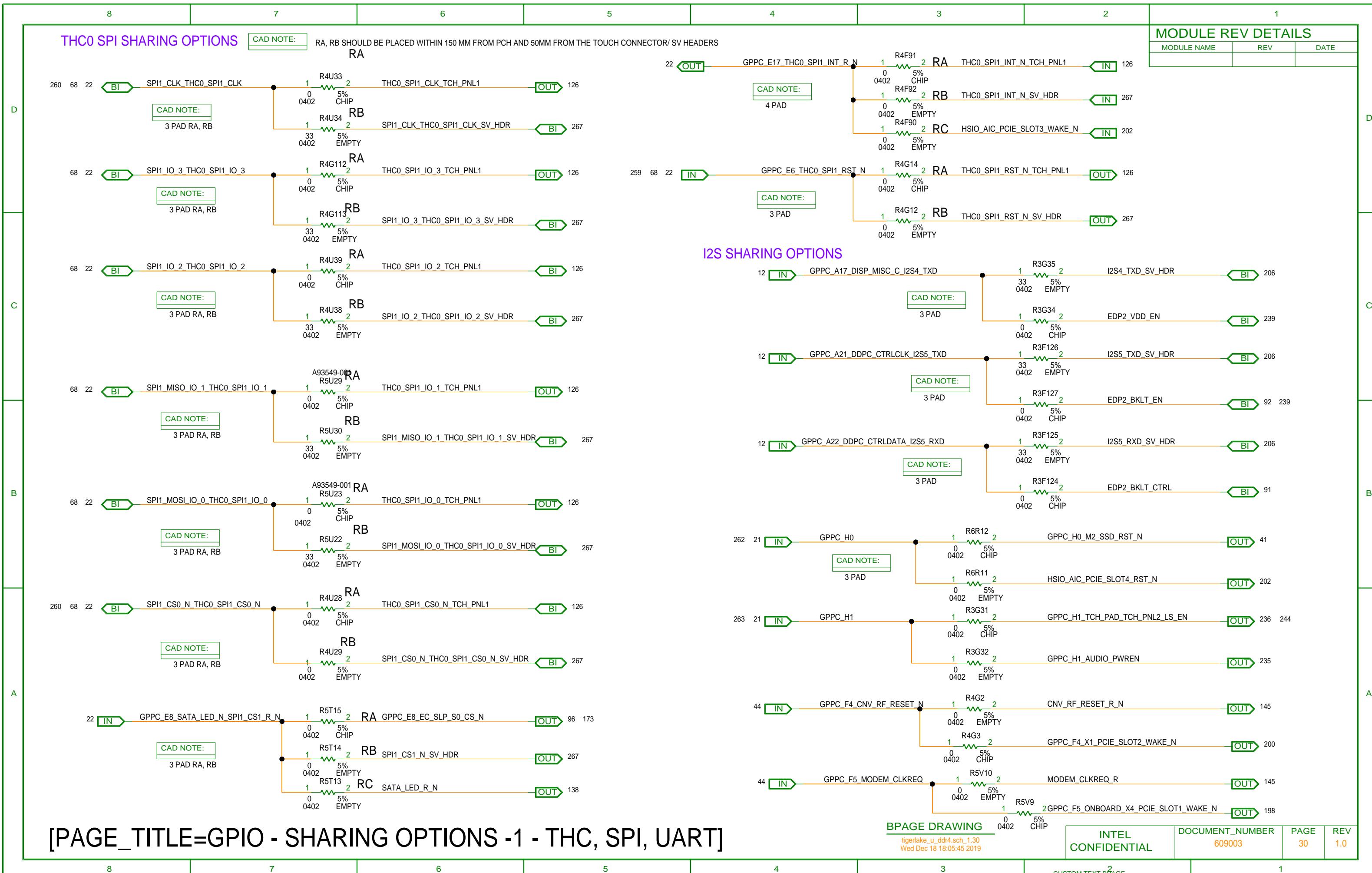


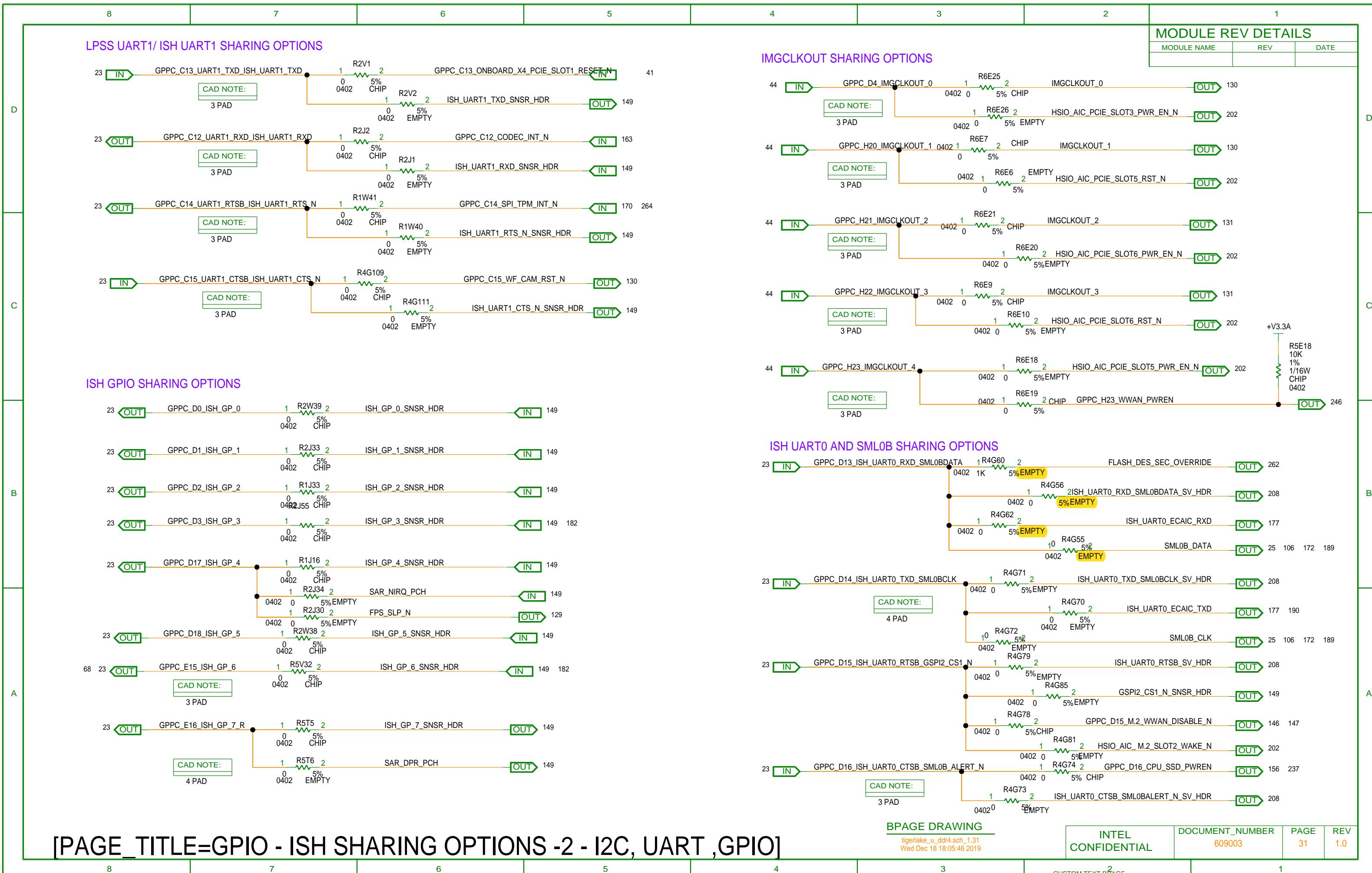






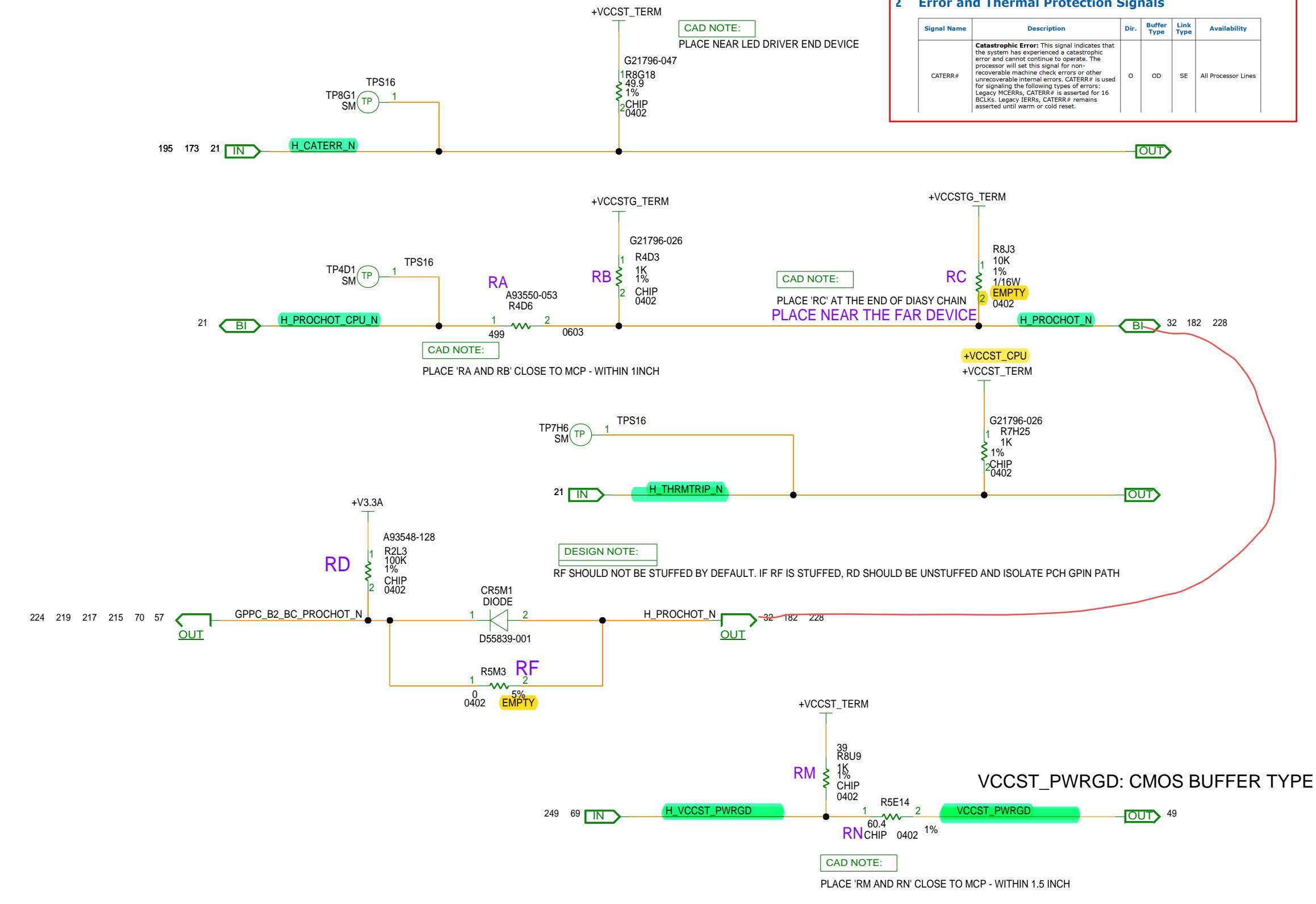






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CPU SIDEBAND SIGNALS

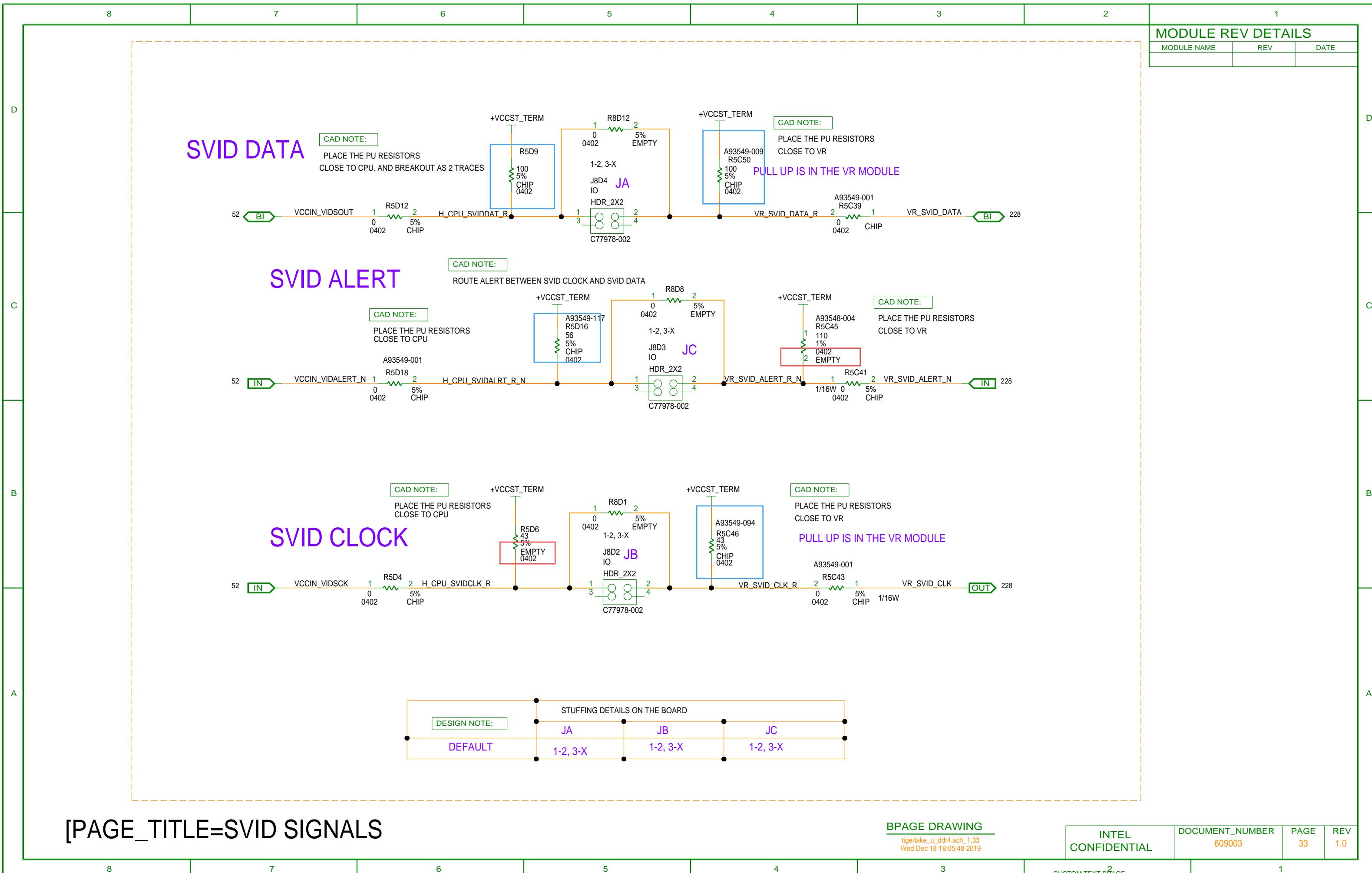


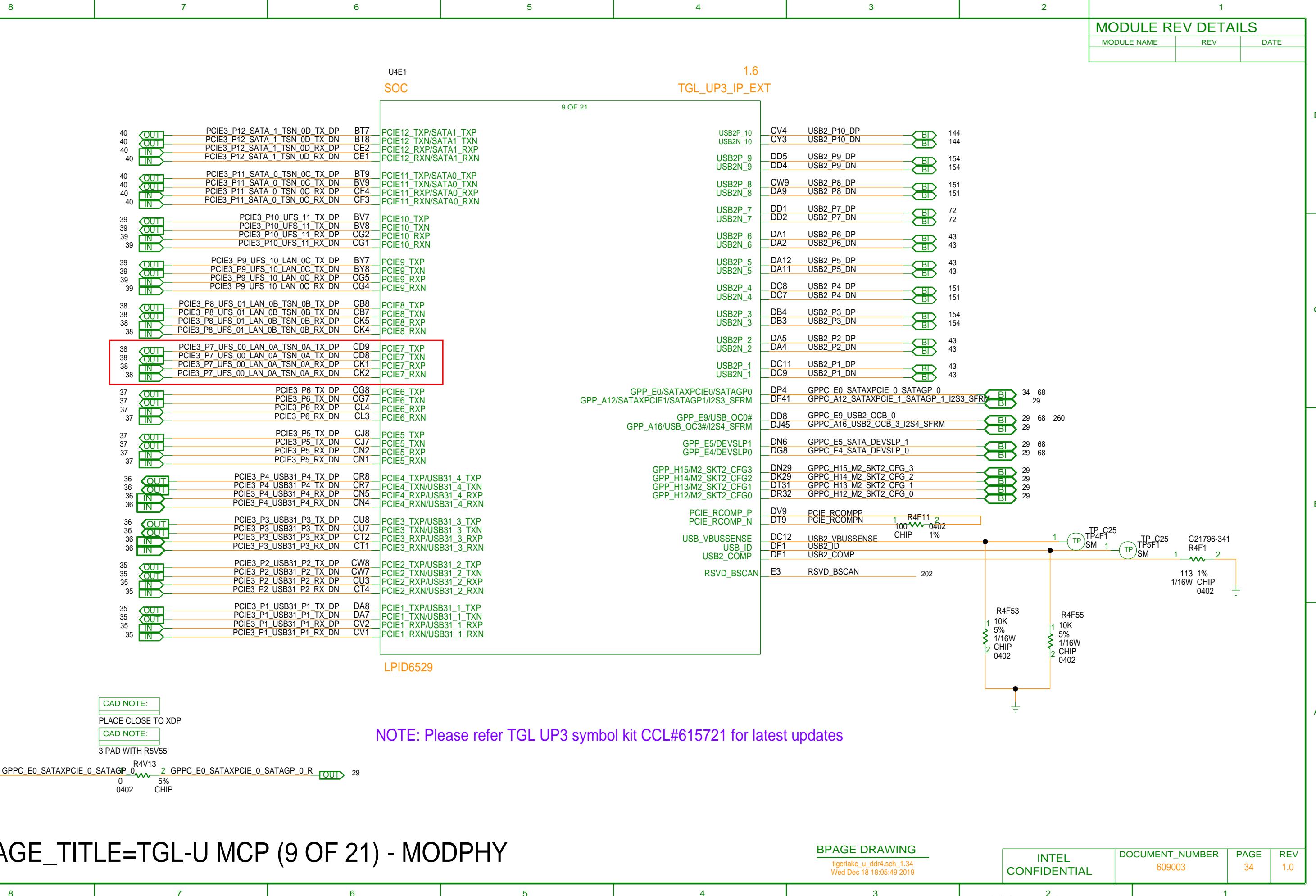
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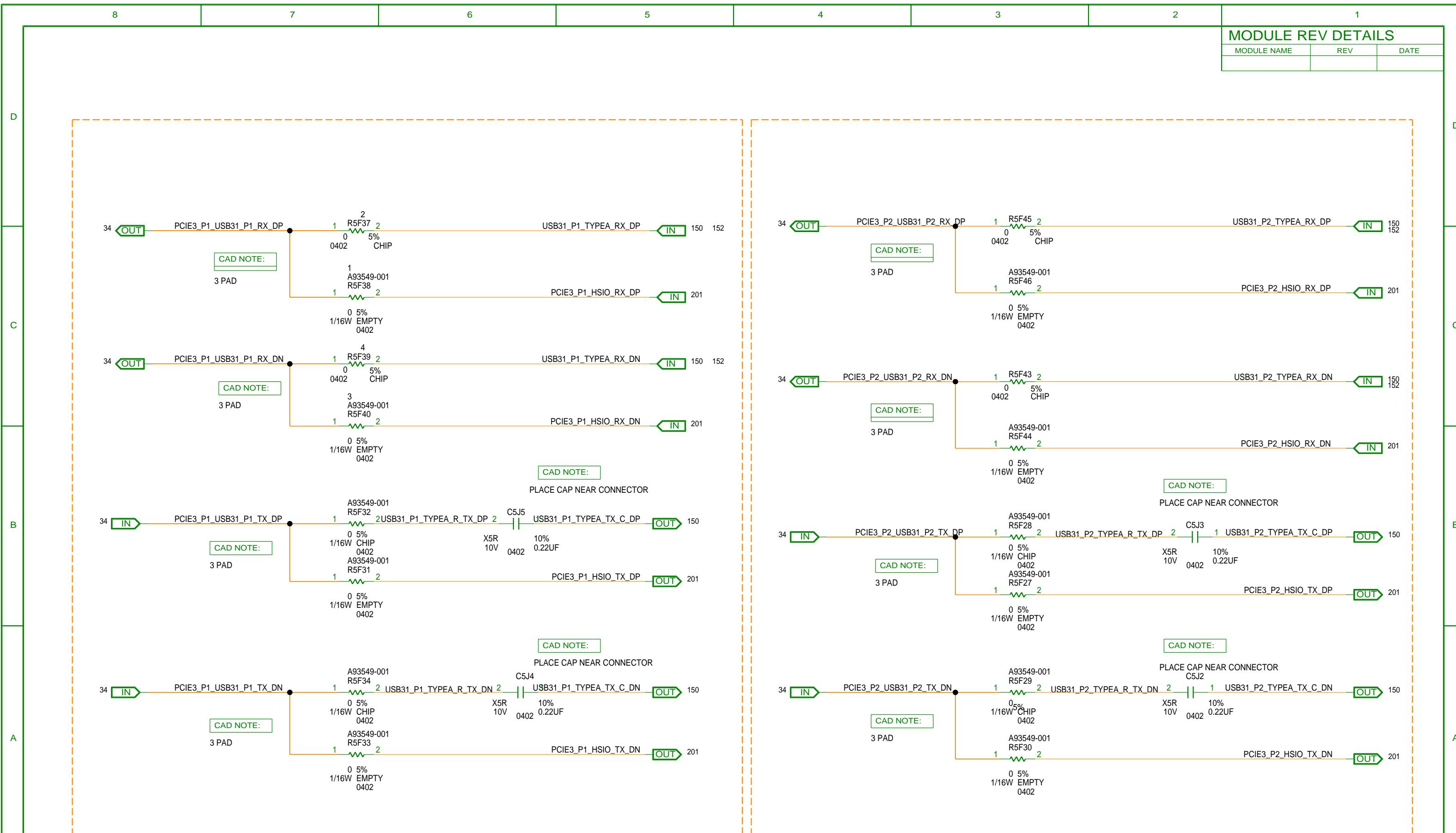
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Wed Dec 18 18:05:47 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 32	REV 1.0
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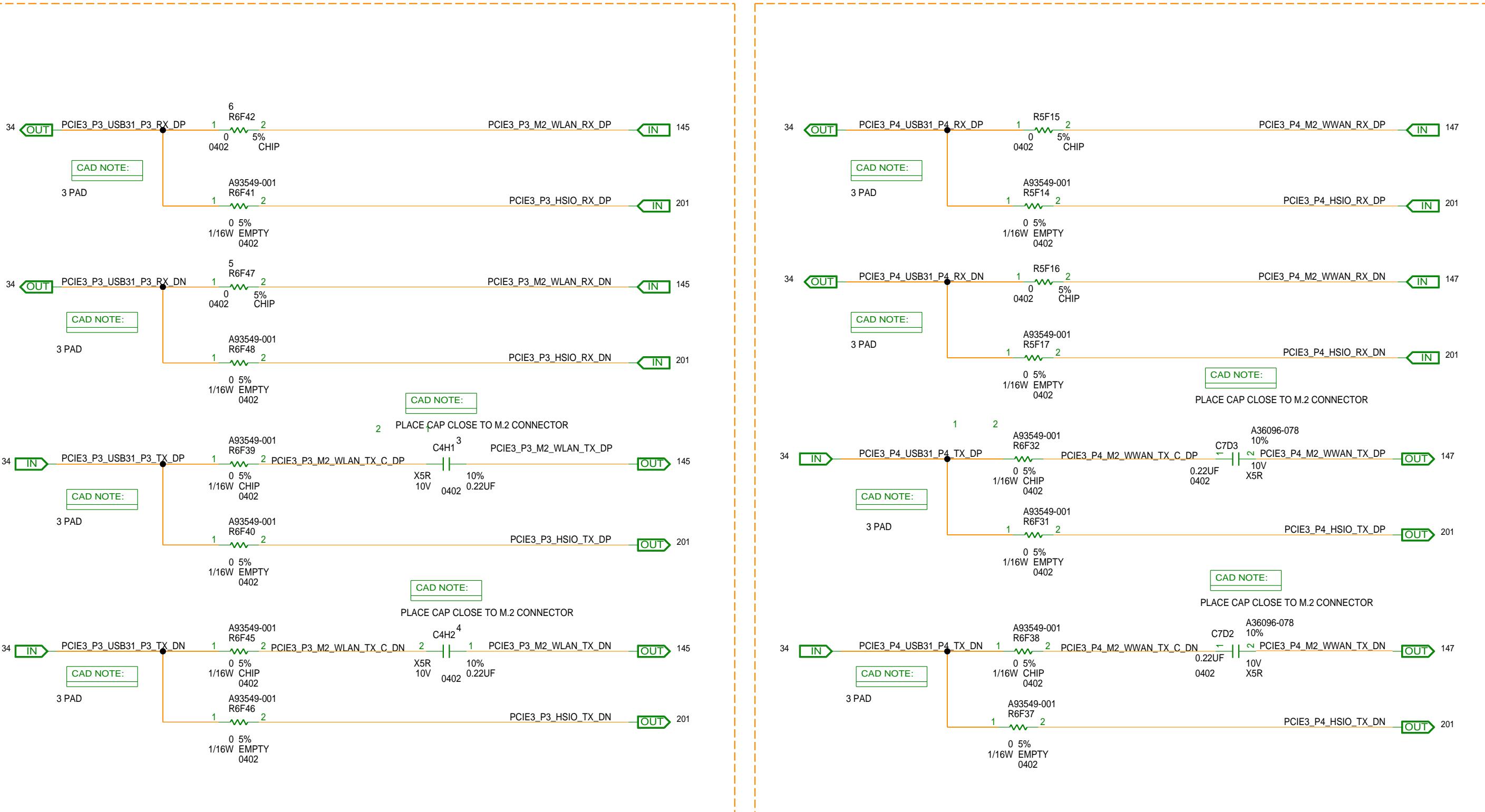


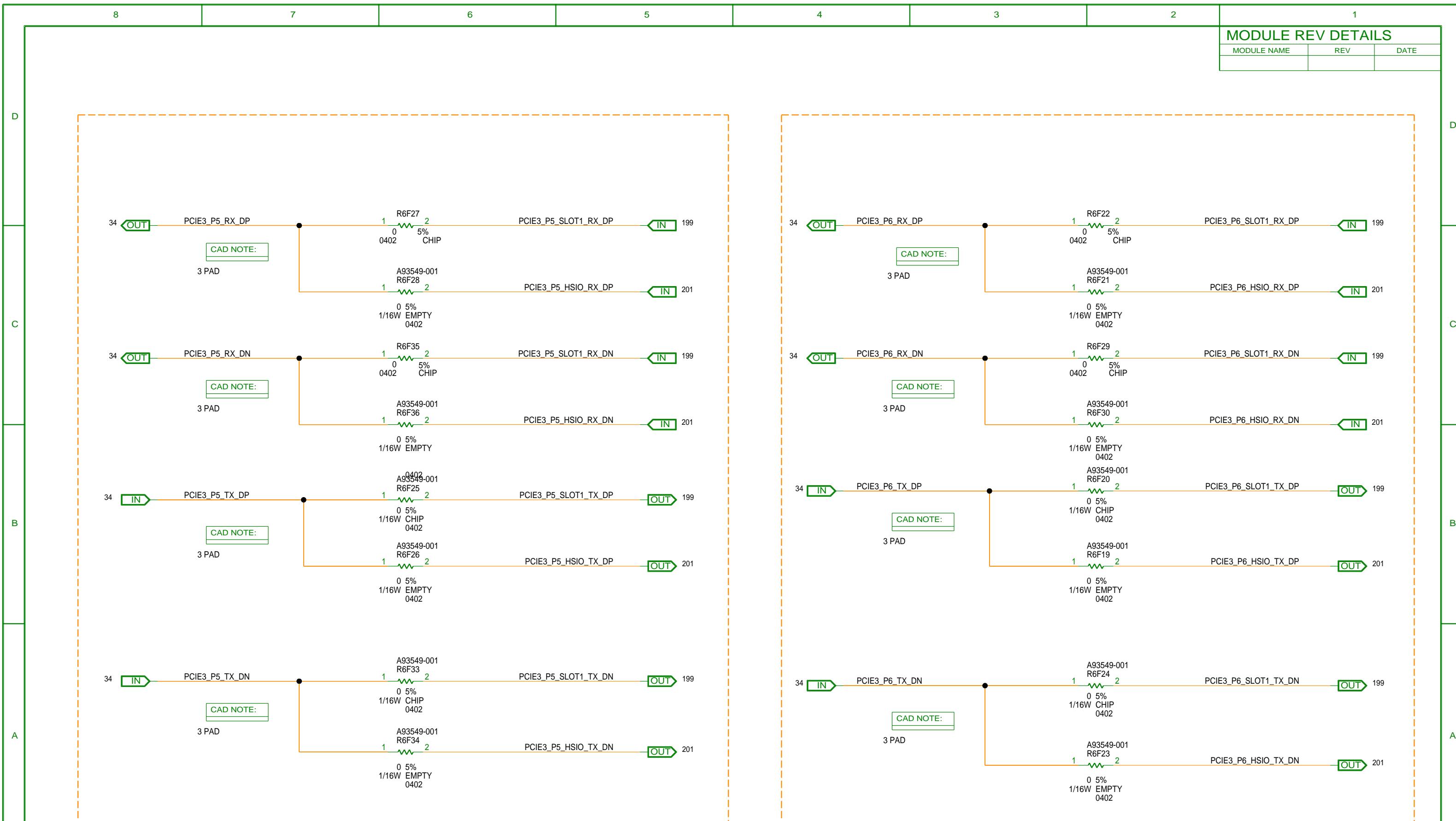
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 35	REV 1.0
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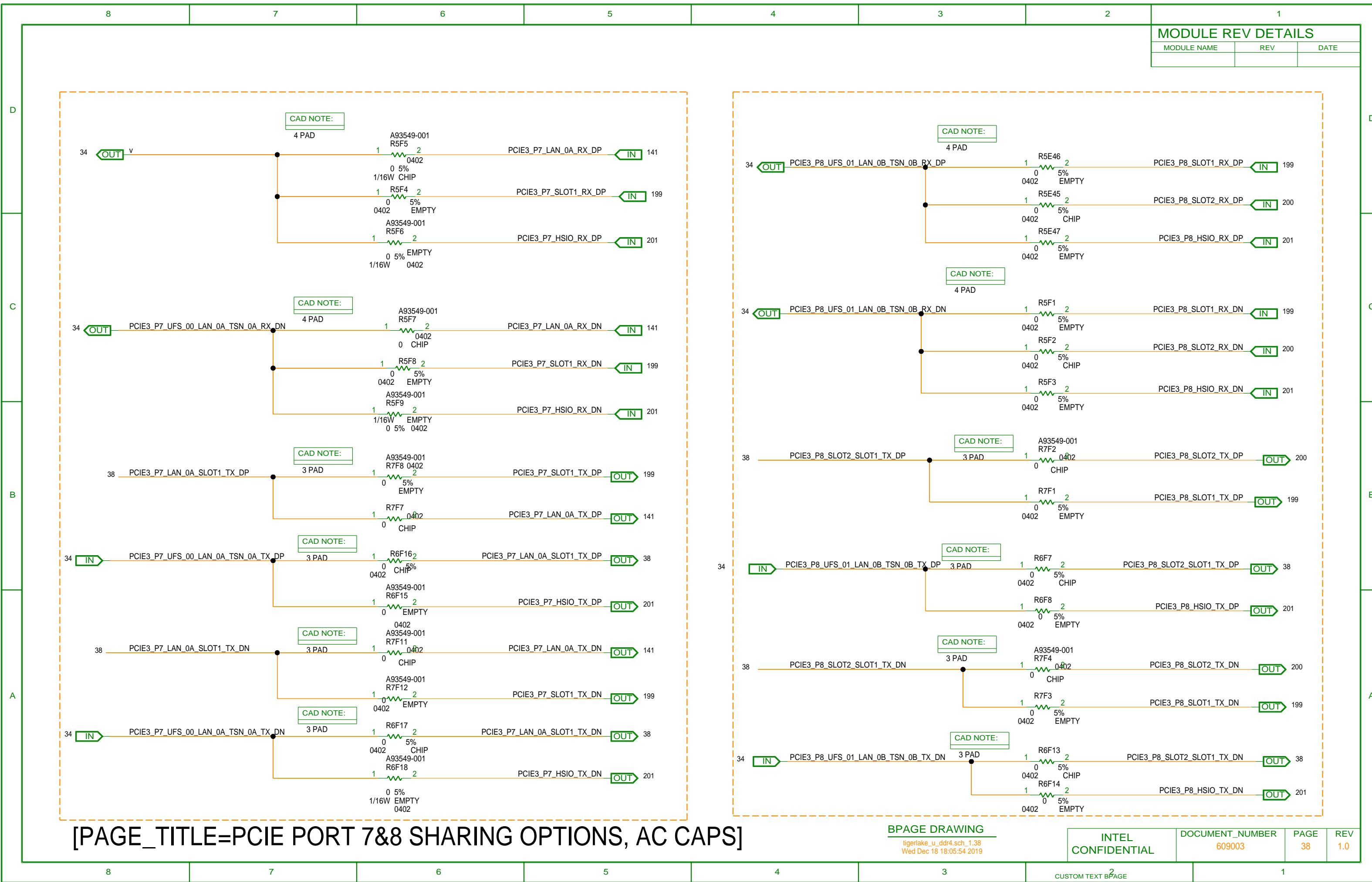




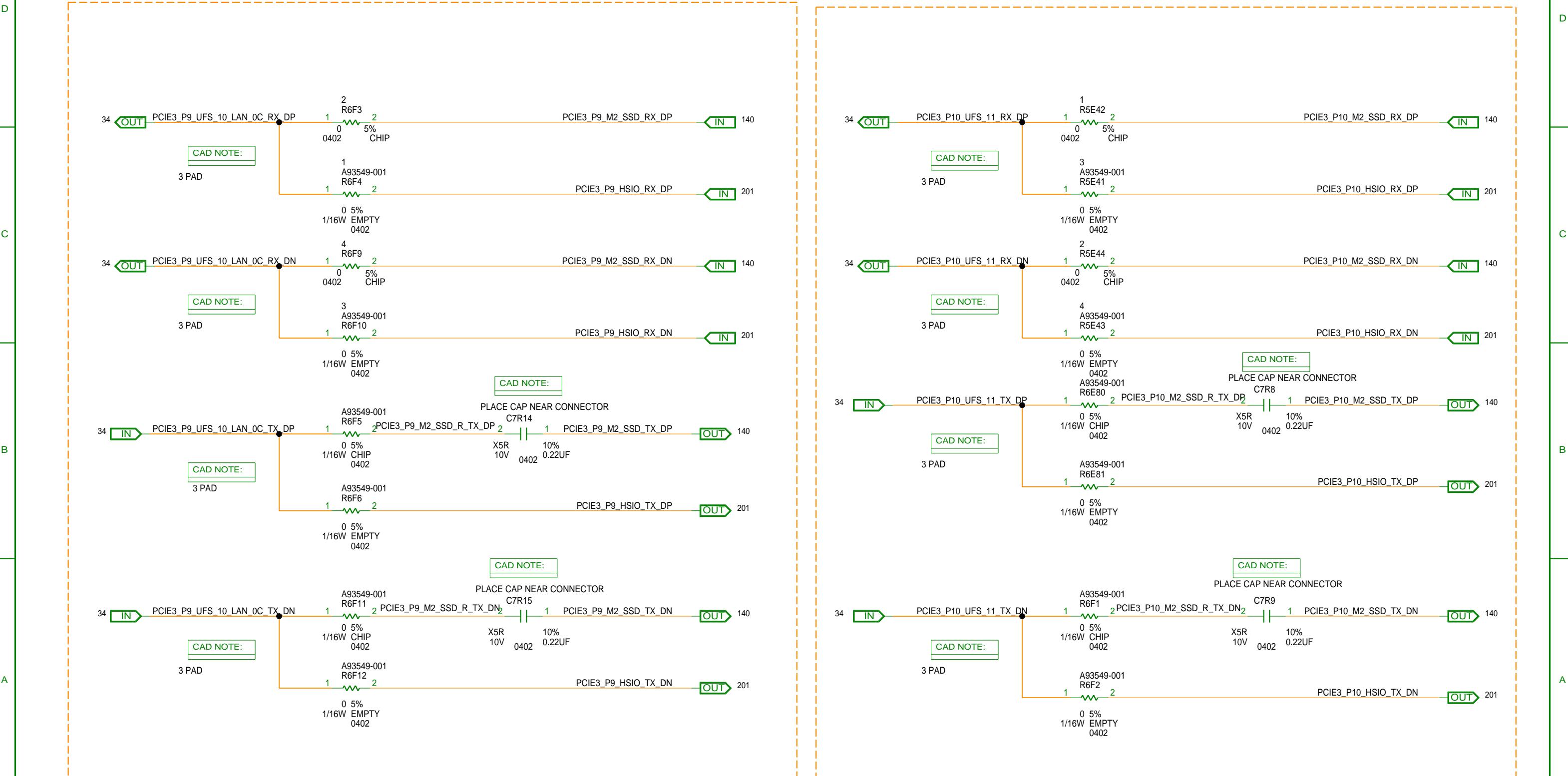
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Wed Dec 18 18:05:52 2019

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MODULE NAME	REV	DATE					

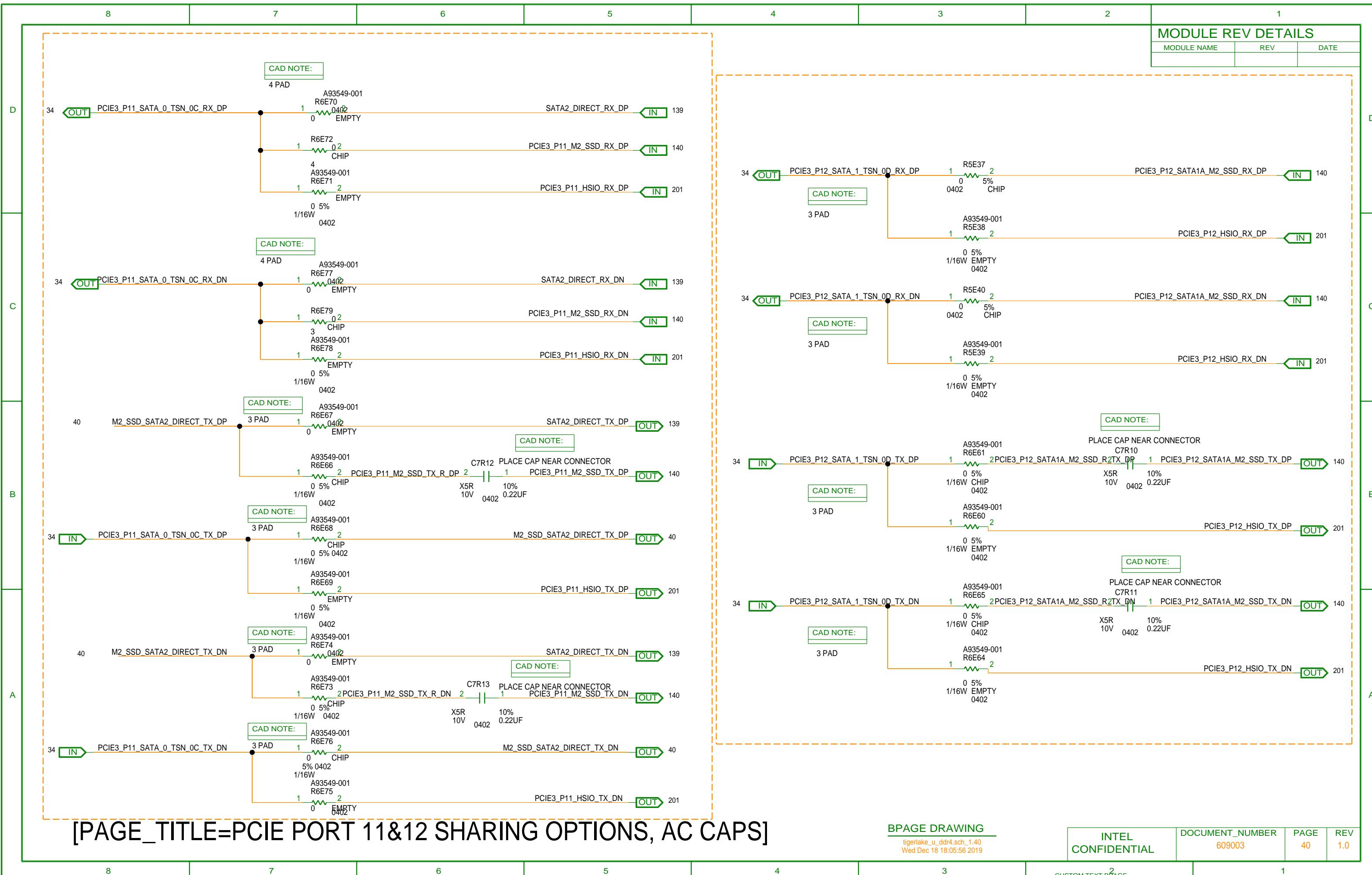


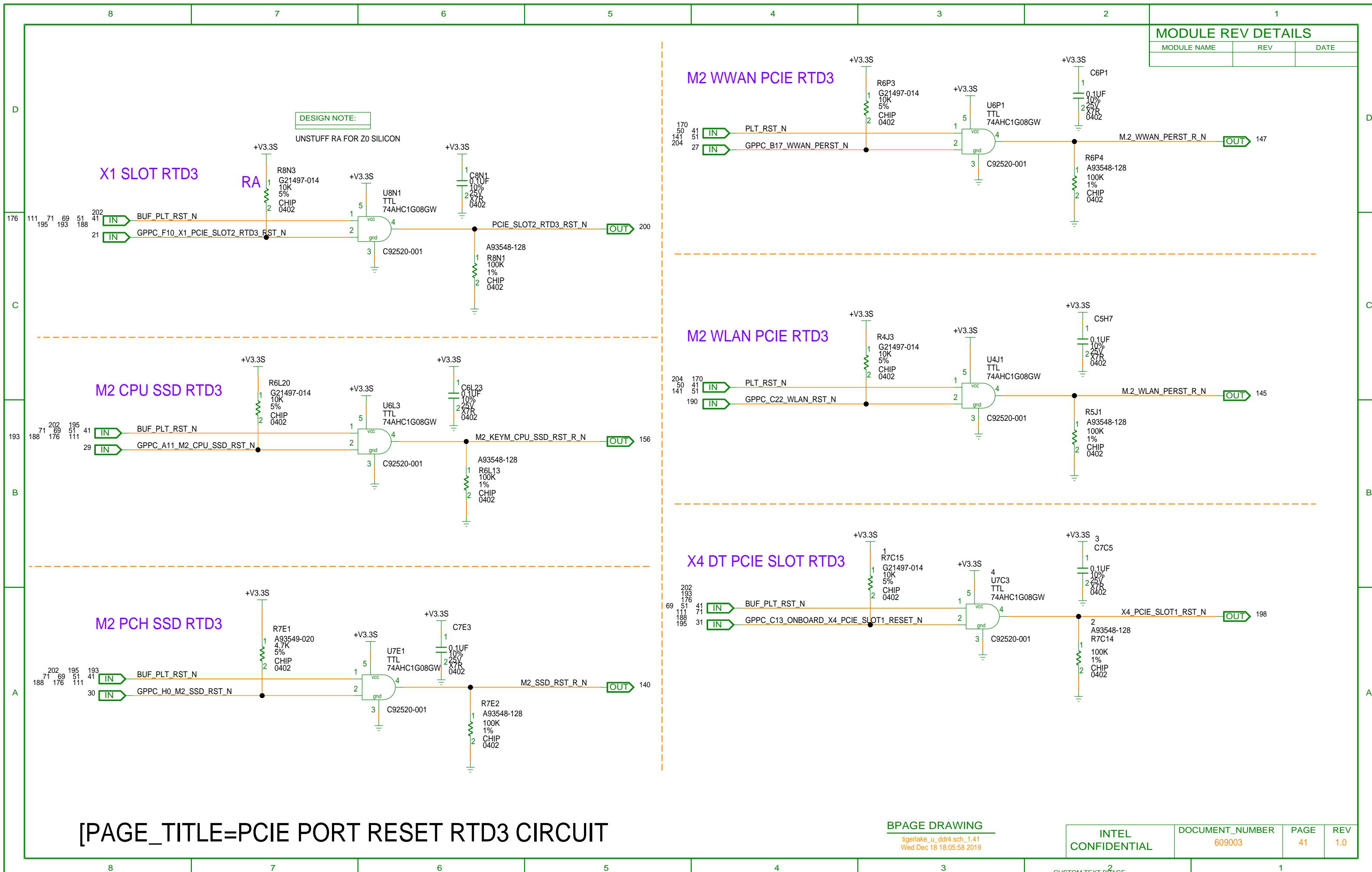
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Wed Dec 18 18:05:55 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 39	REV 1.0

CUSTOM TEXT BPAGE





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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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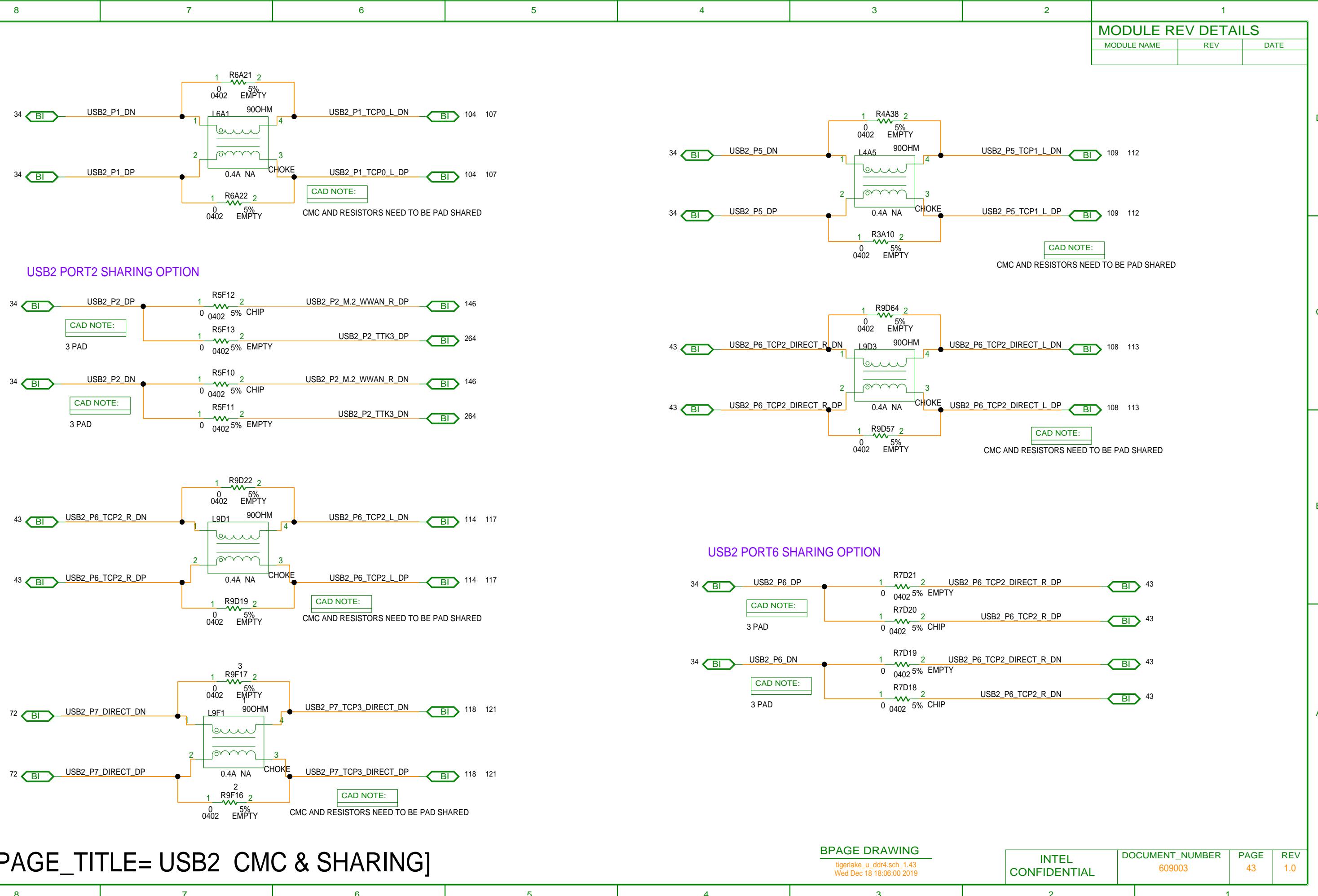
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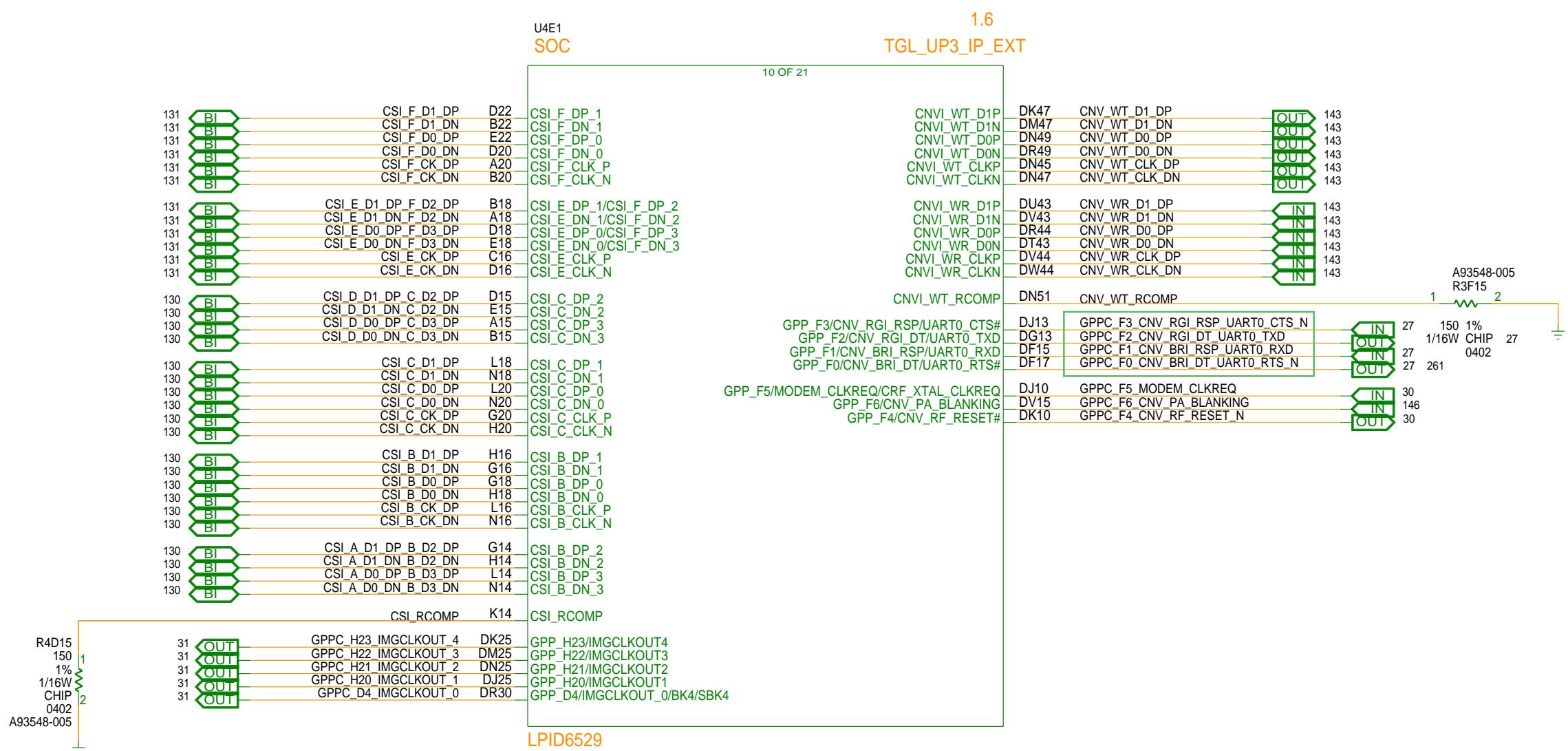
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 42	REV 1.0
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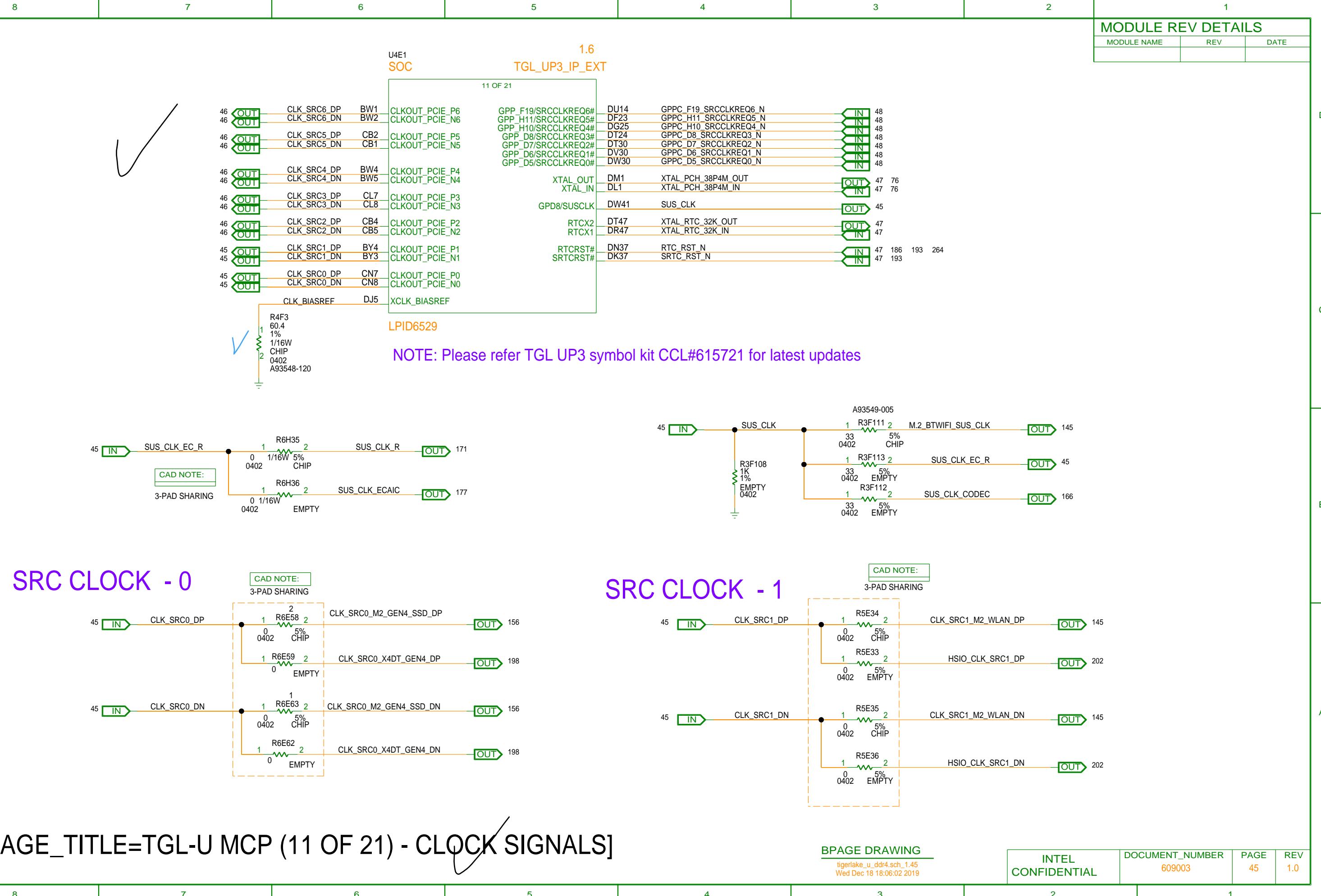


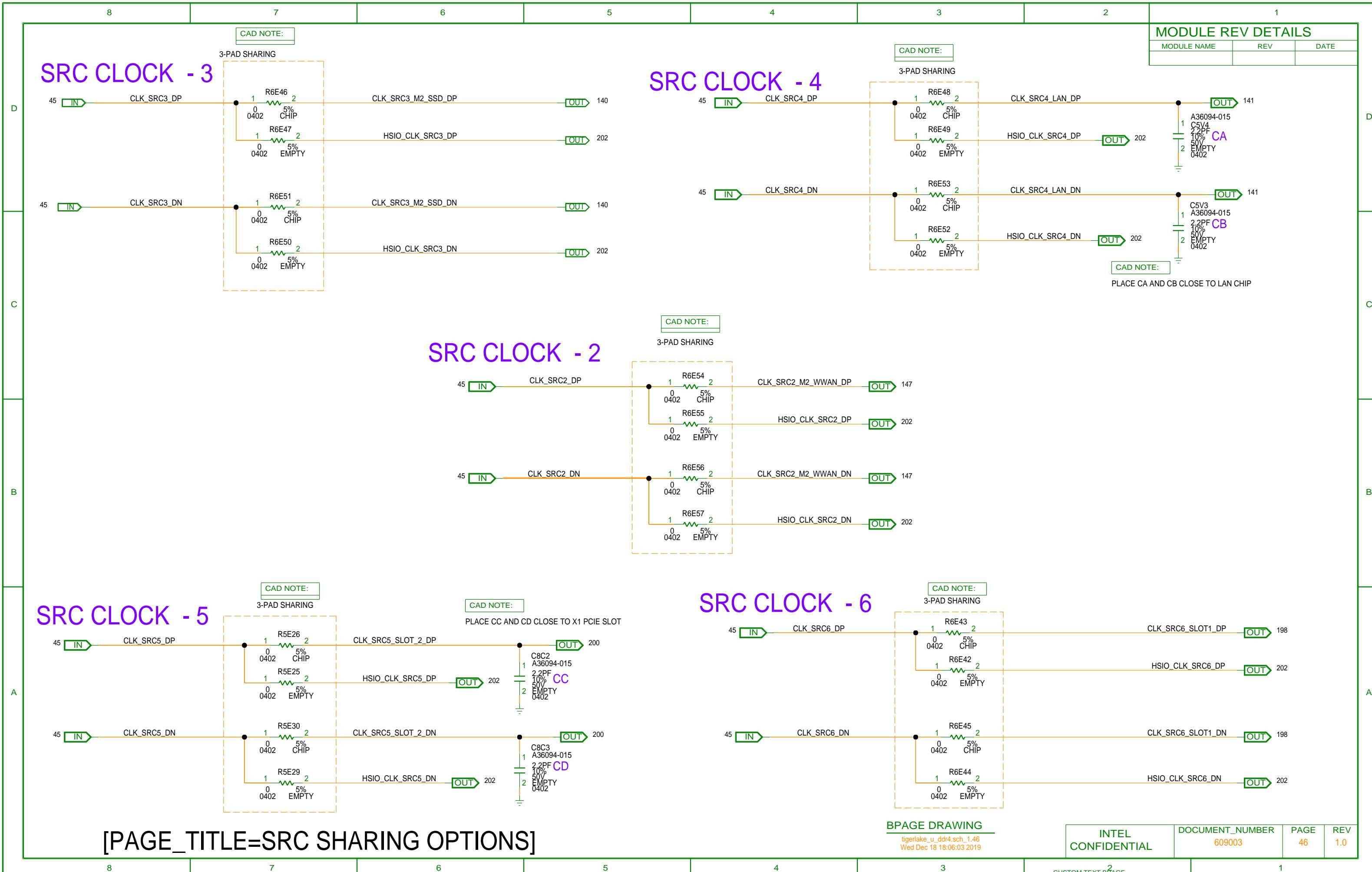
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MODULE REV DETAILS							

DIDNT IMPLEMENT YET



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates





8 7 6 5 4 3 2 1

MODULE REV DETAILS

MODULE NAME	REV	DATE

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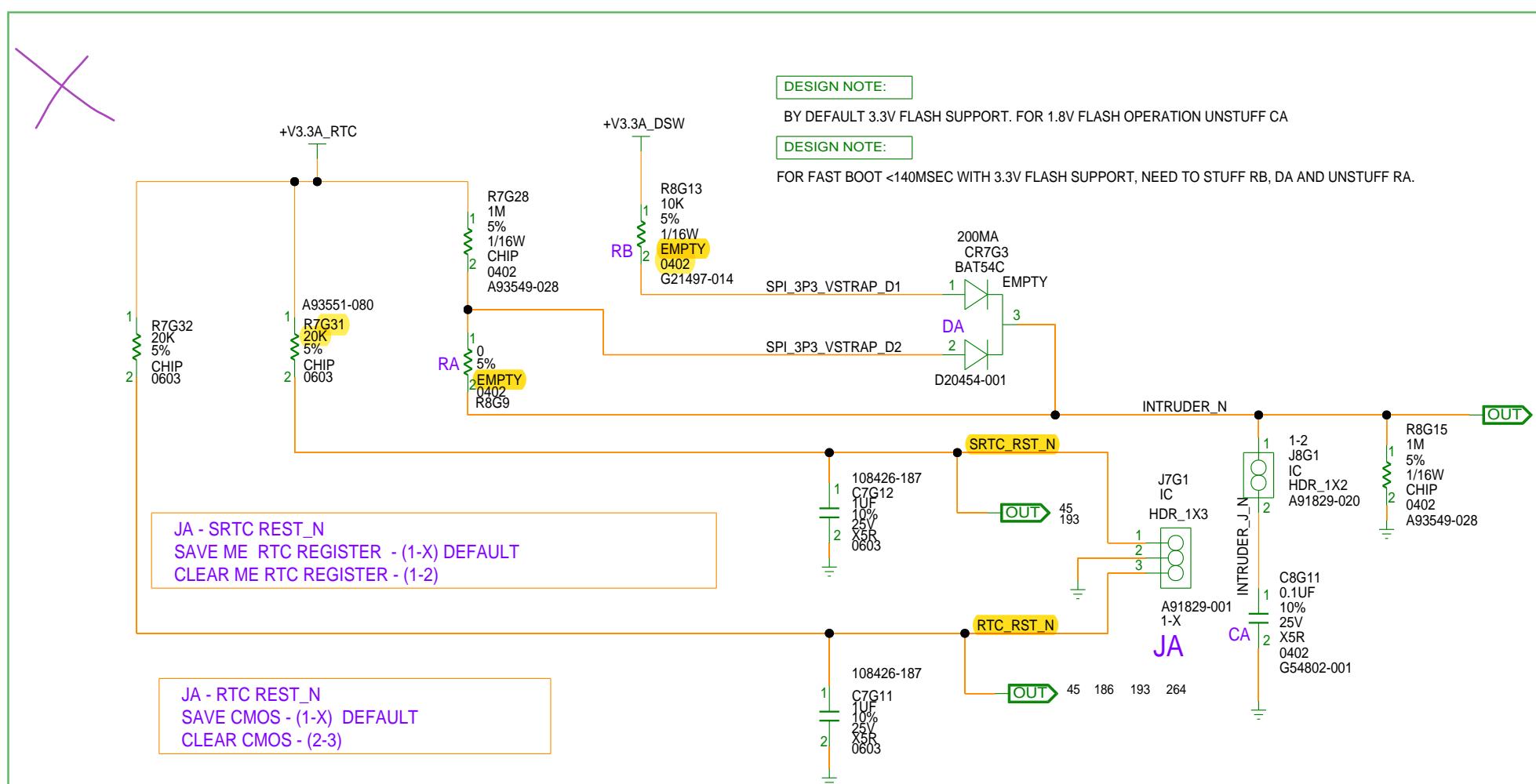
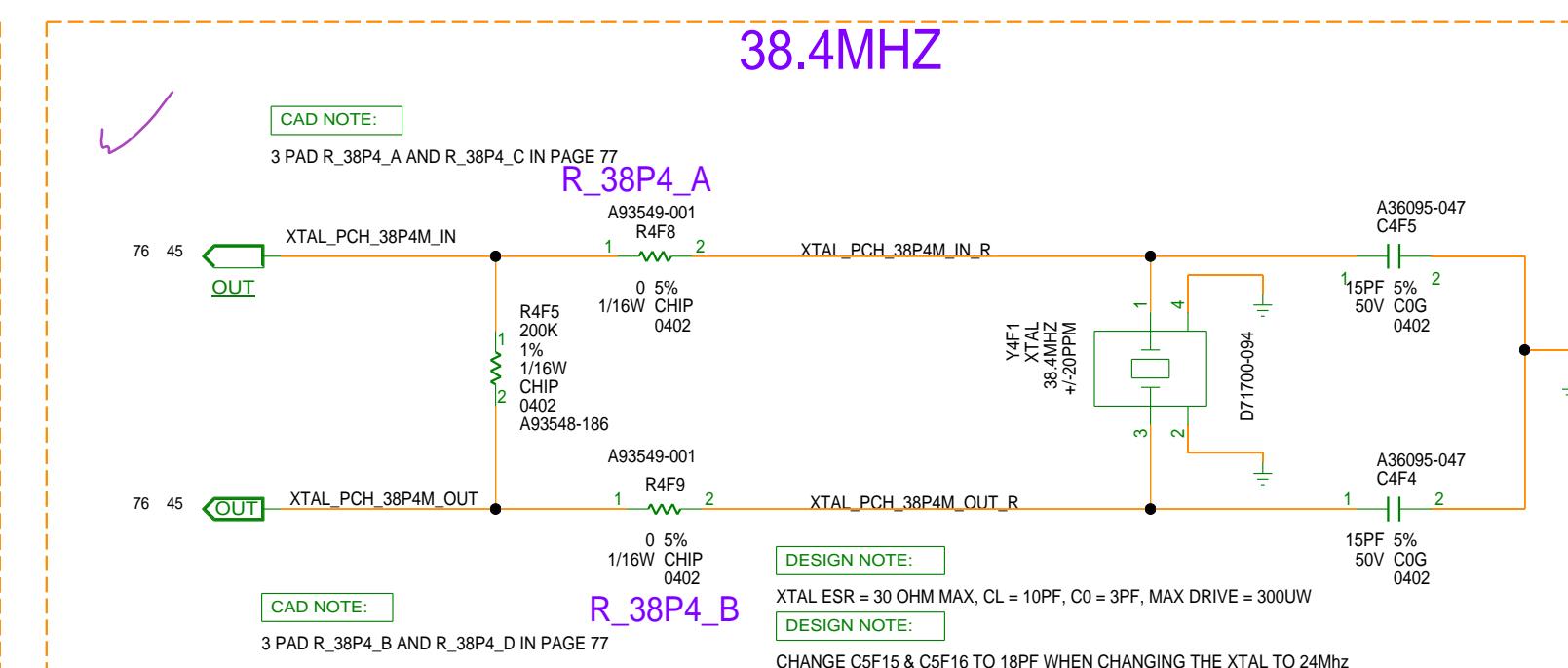
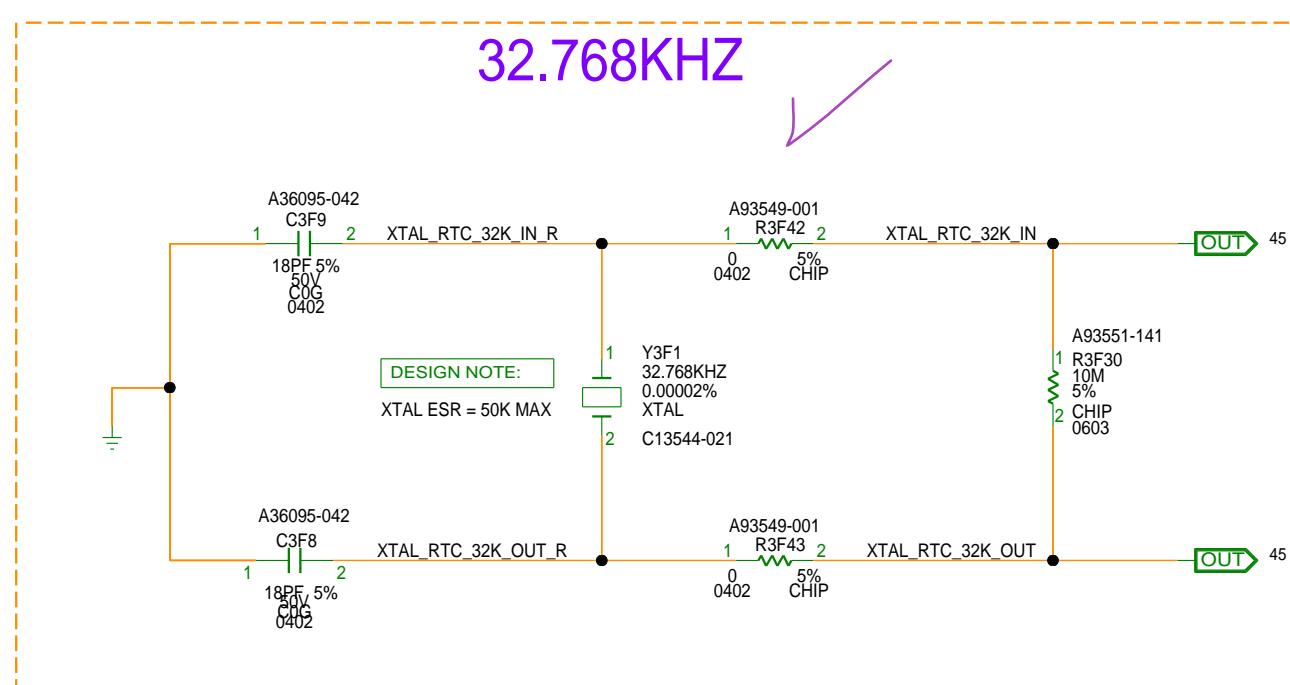
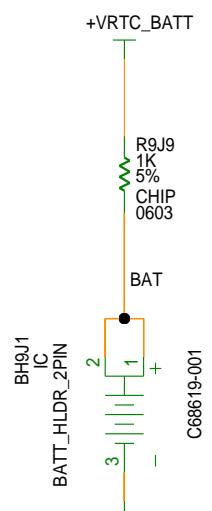
C

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**+V3.3A_RTC GENERATION**

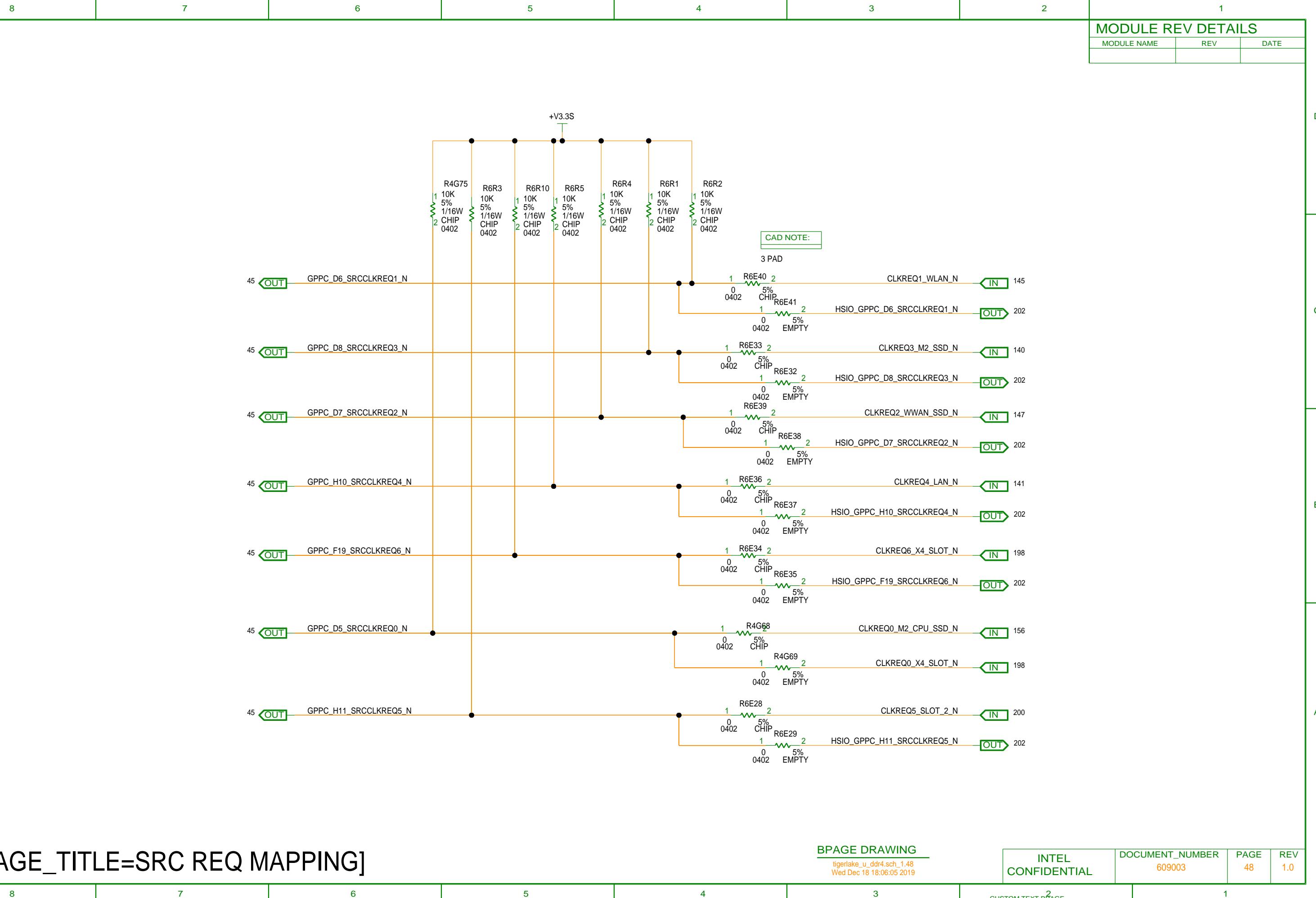
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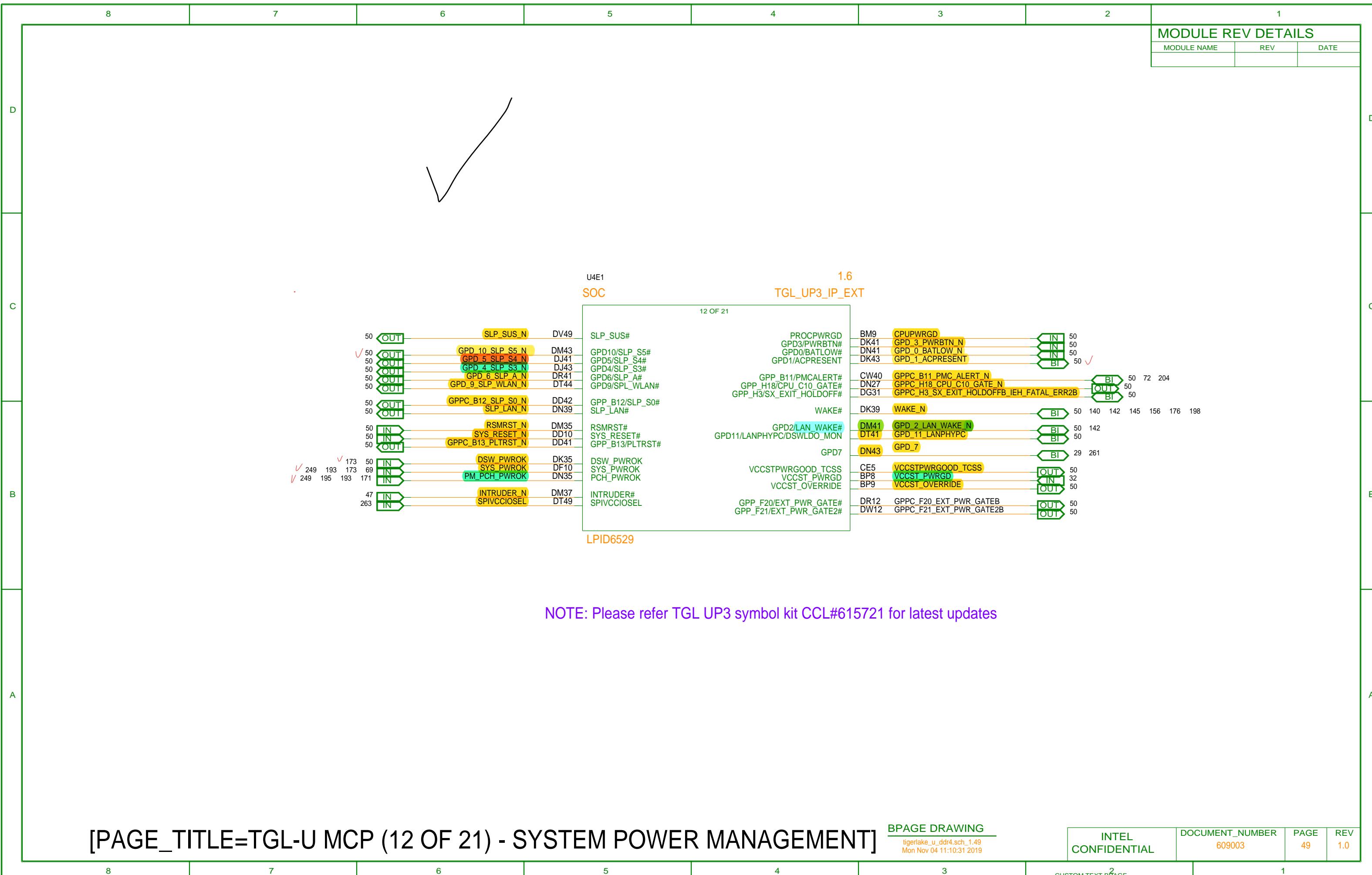
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Wed Dec 18 18:06:04 2019

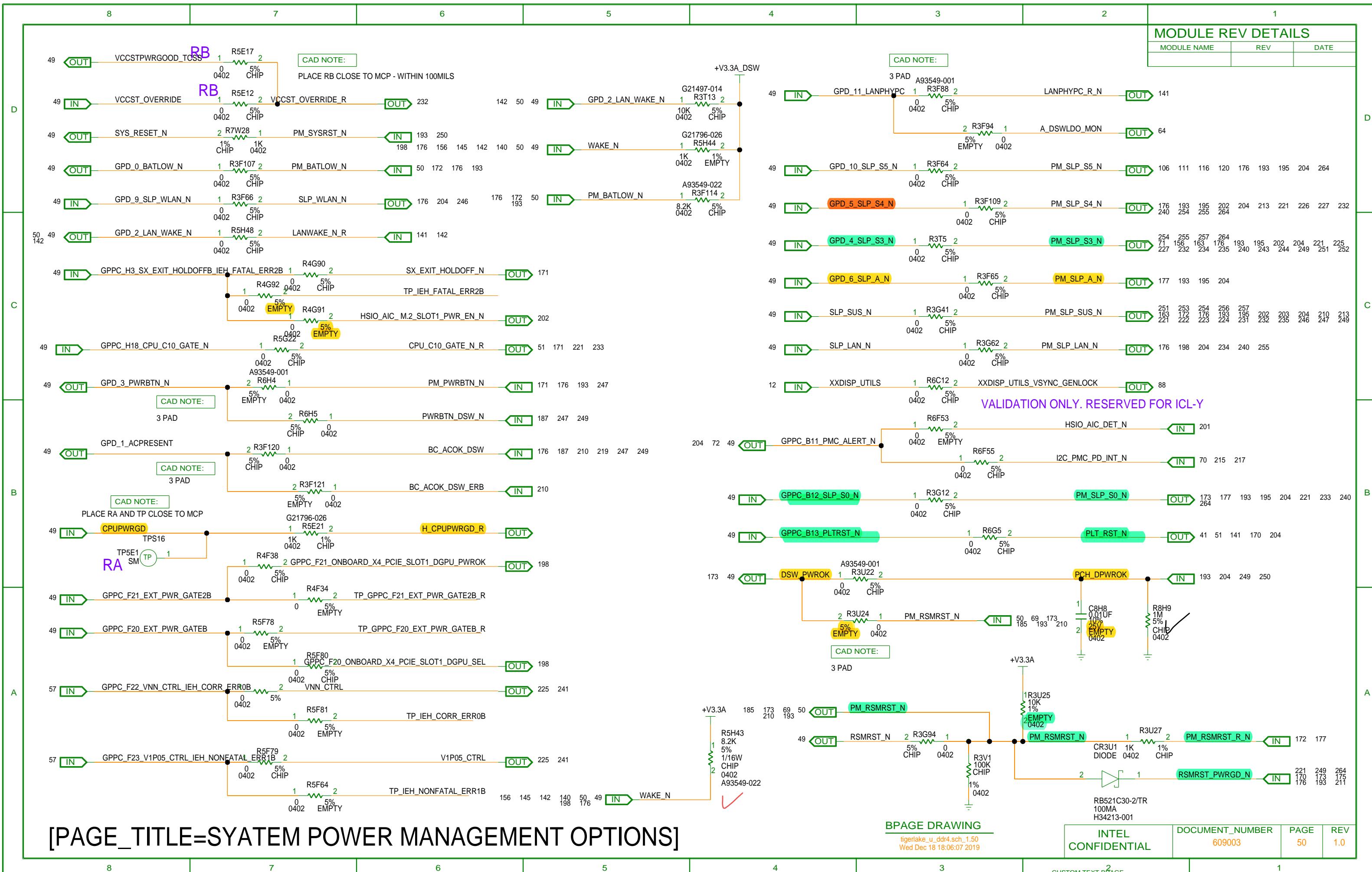
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 47	REV 1.0
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CUSTOM TEXT BPAGE

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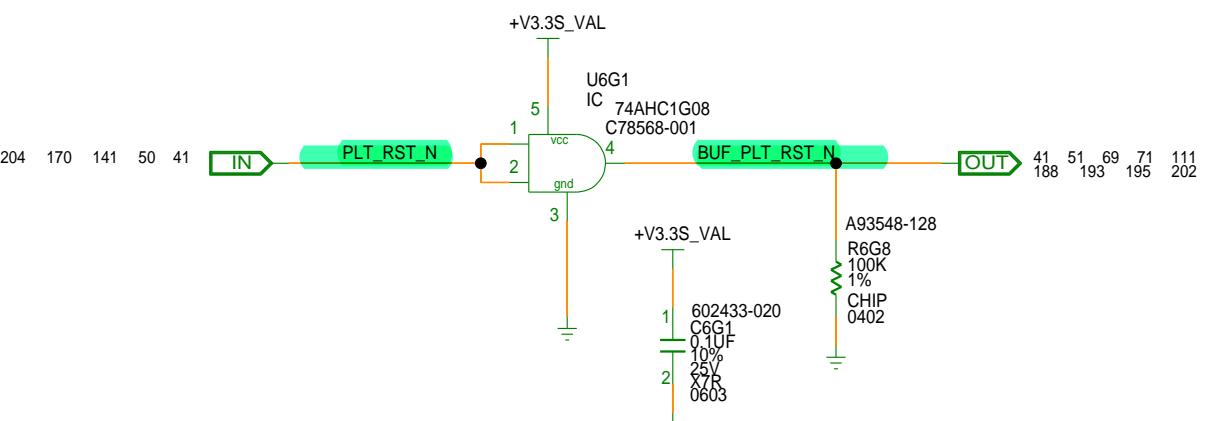
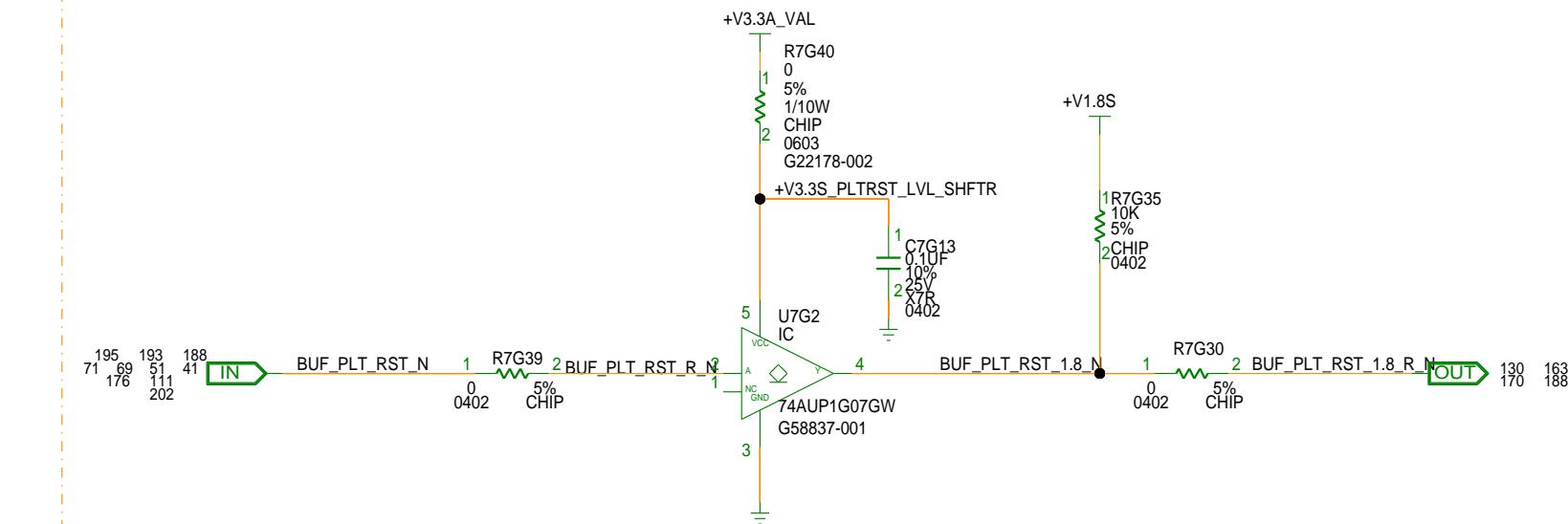






8	7	6	5	4	3	2	1
MODULE REV DETAILS							

D

BUFFER TO REDUCE LOADING ON PLT_RST_N**PLATFORM RESET LEVEL SHIFTER - 3.3V TO 1.8V**

C

B

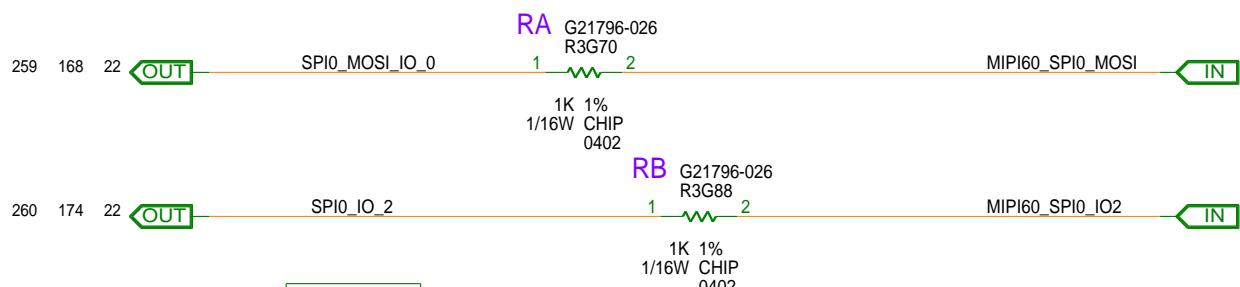
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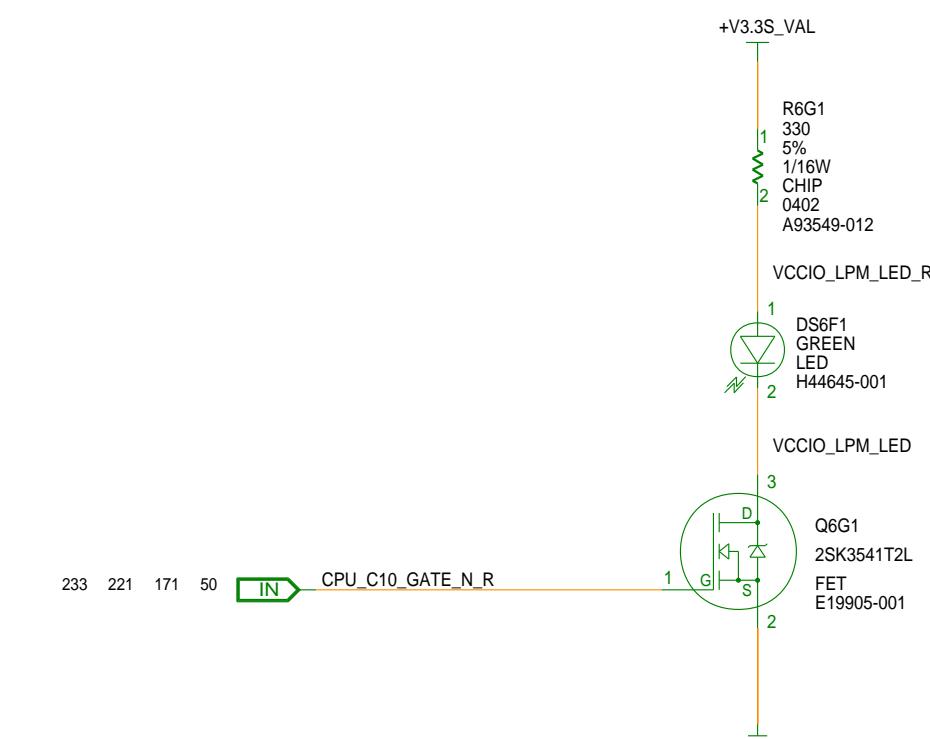
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CAD NOTE:
RA AND RB RESISTORS NEED TO BE PLACED NEAR TO MCP, WITHOUT STUB ON SPI



[PAGE_TITLE=PLATFORM RESET BUFFER]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.51
Wed Dec 18 18:06:08 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 51	REV 1.0
CUSTOM TEXT BPAGE			1

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MODULE REV DETAILS

MODULE NAME	REV	DATE

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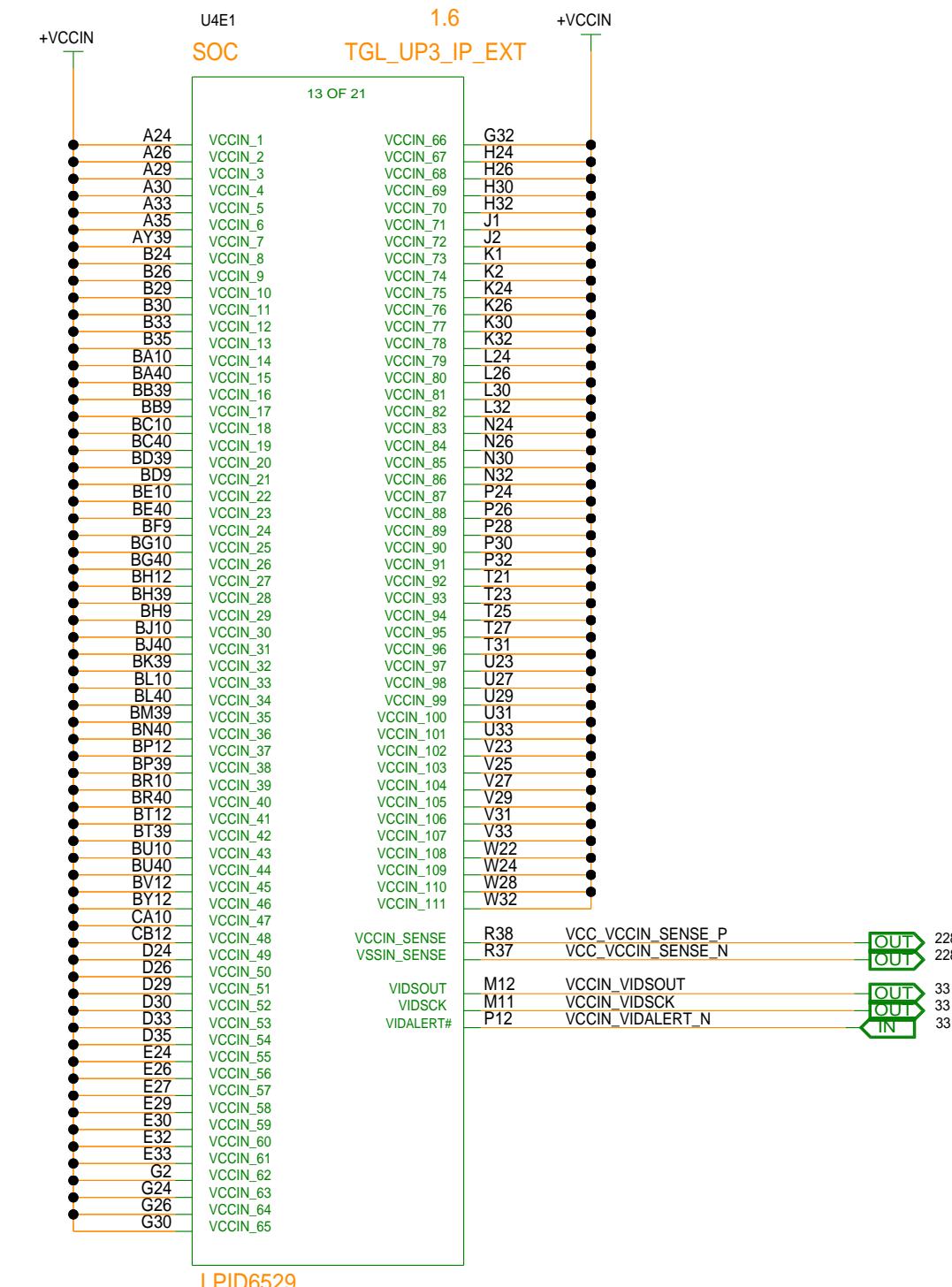
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NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL U MCP (13 OF 21) - CPU POWER 1 OF 2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.52
Wed Dec 18 18:06:09 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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8

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6

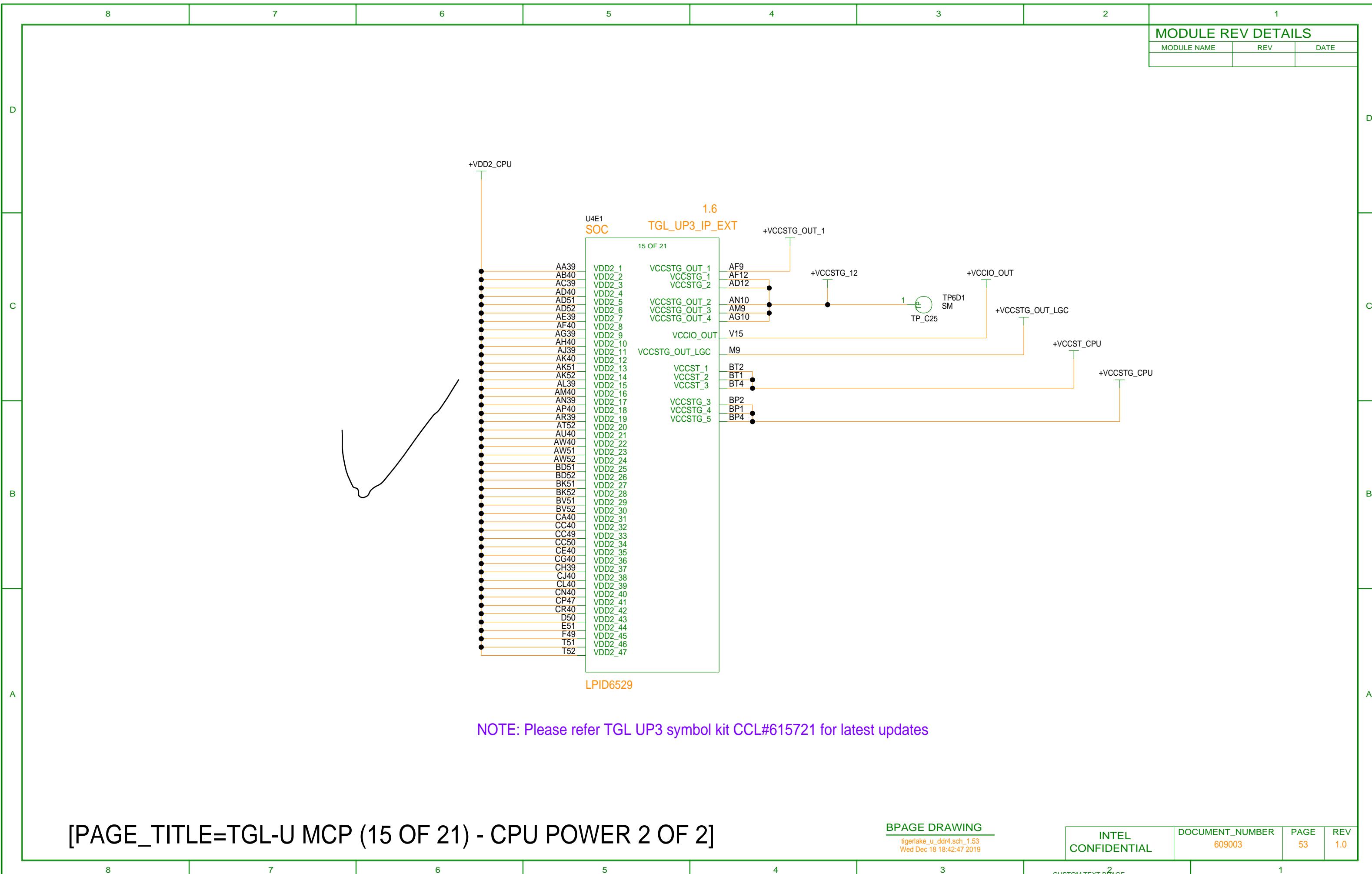
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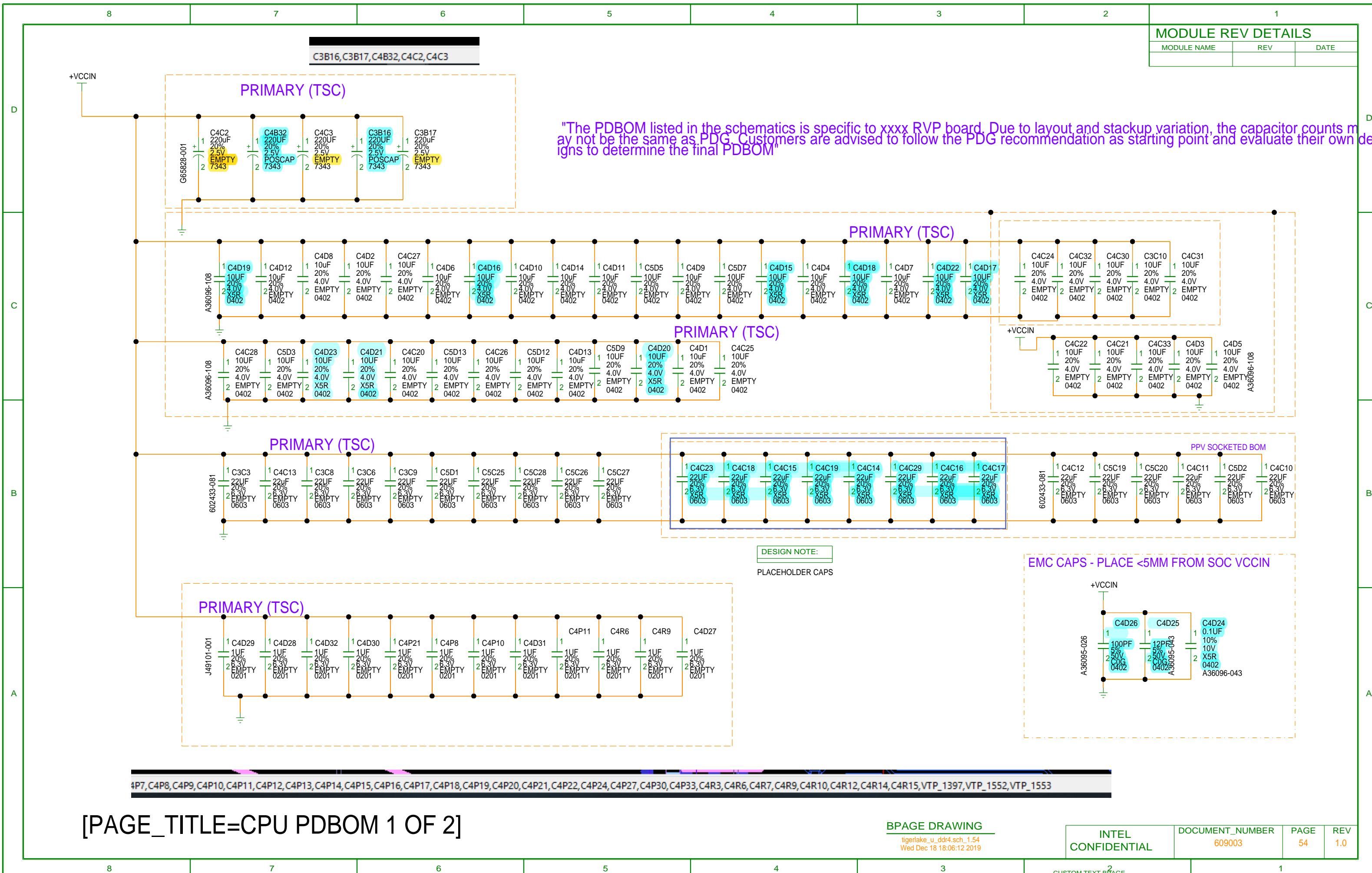
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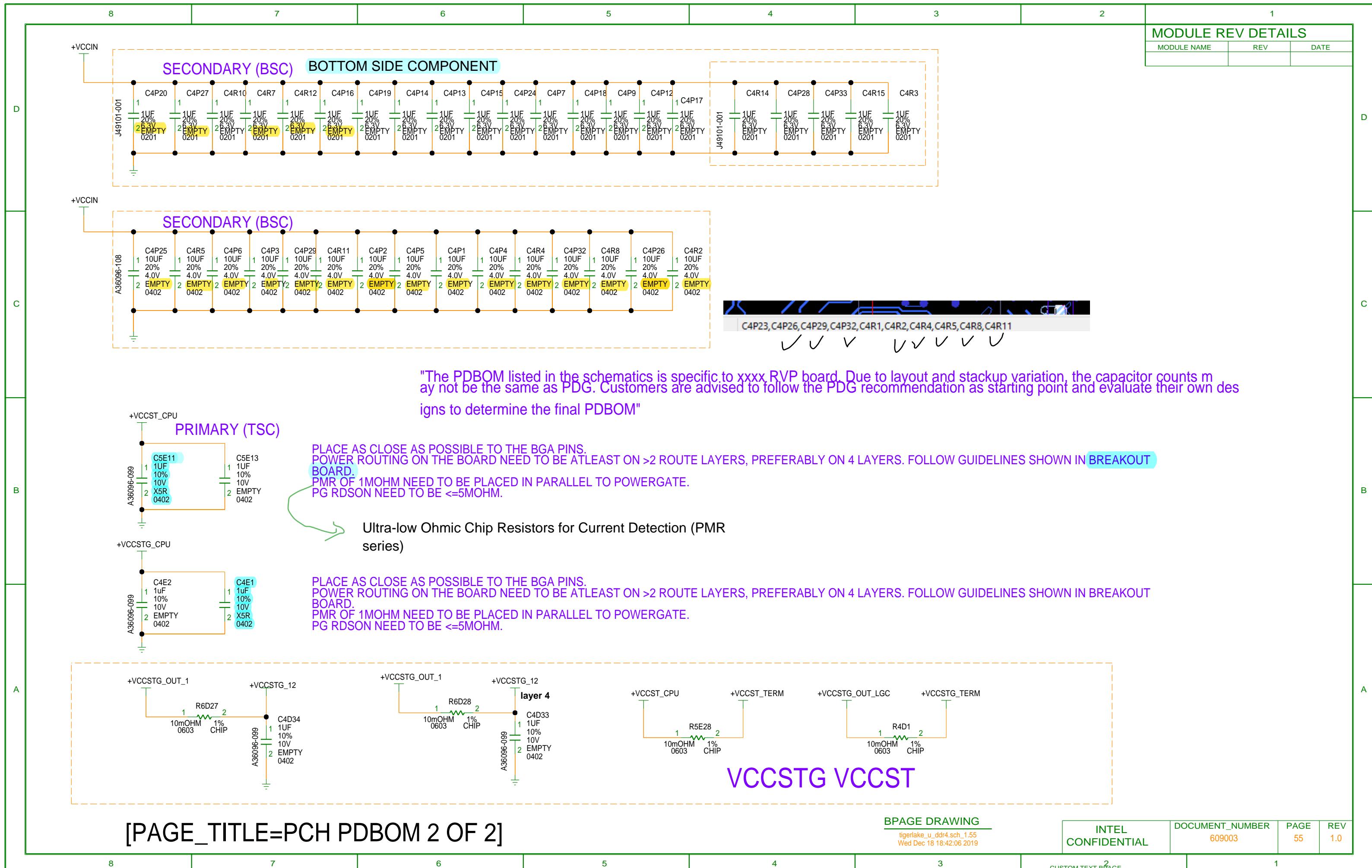
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CUSTOM TEXT BPAGE

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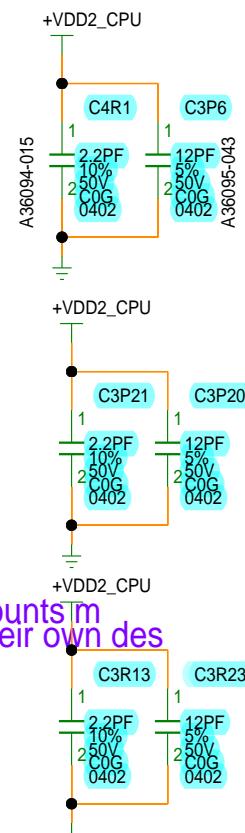




VDD2

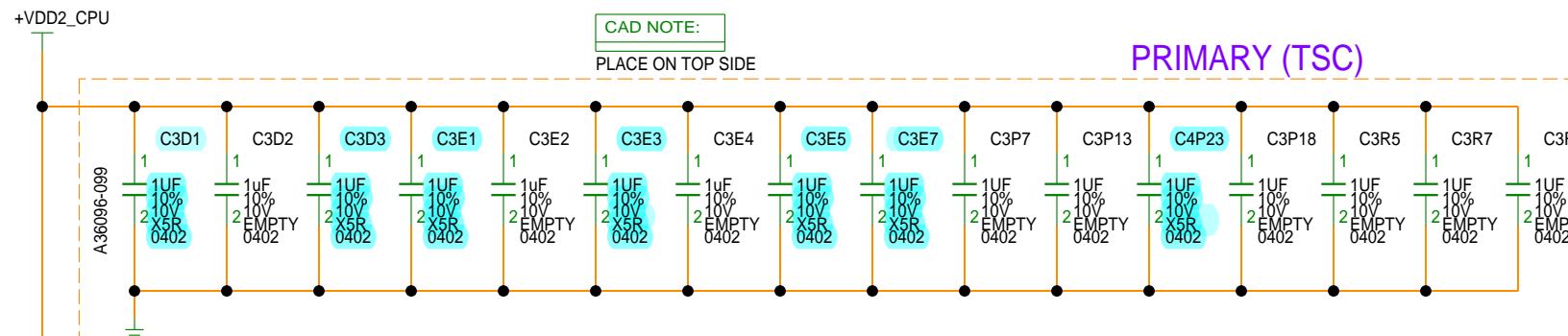
MODULE REV DETAILS		
MODULE NAME	REV	DATE

EMC CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART



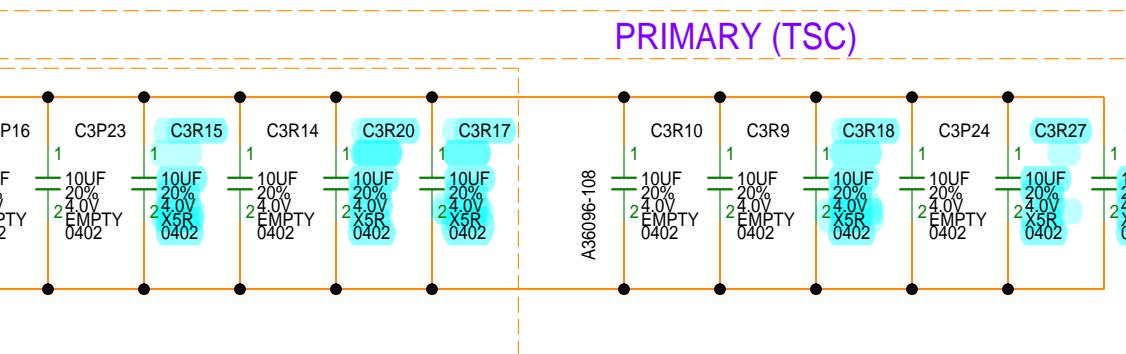
I put 10/16

PRIMARY (TSC)

CAD NOTE:
PLACE ON TOP SIDE

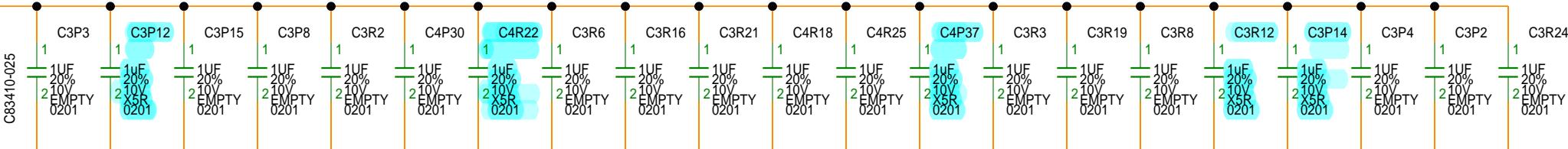
I put 12/16

PRIMARY (TSC)

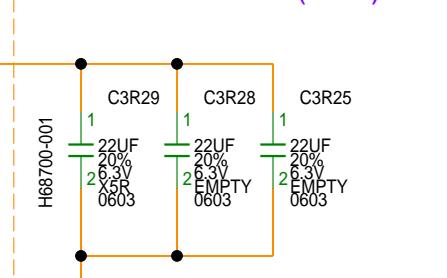
PRIMARY (TSC)
PLACE NEAR BOARD PMIC

The PDBOM listed in the schematics is specific to xxxx RVP board. Due to layout and stackup variation, the capacitor counts may not be the same as PDG. Customers are advised to follow the PDG recommendation as starting point and evaluate their own designs to determine the final PDBOM.

SECONDARY (BSC)

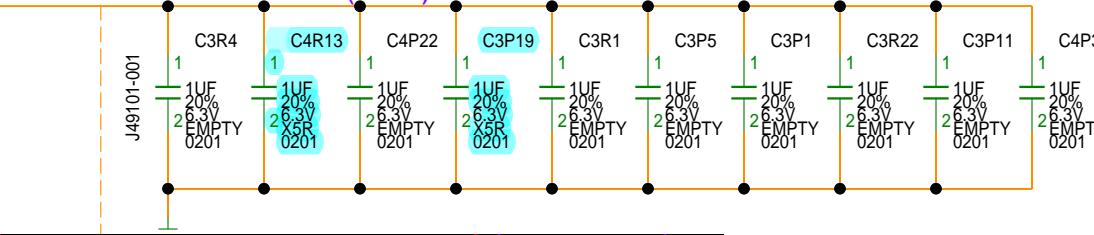


PRIMARY (TSC)



+VDD2_CPU

SECONDARY (BSC)



C3R2,C3R3,C3R6,C3R16,C3R21,C3R22,C4P30,C4P33,C4P34,C4P37,C4R3,C4R13,C4R18,C4R22,C4R25

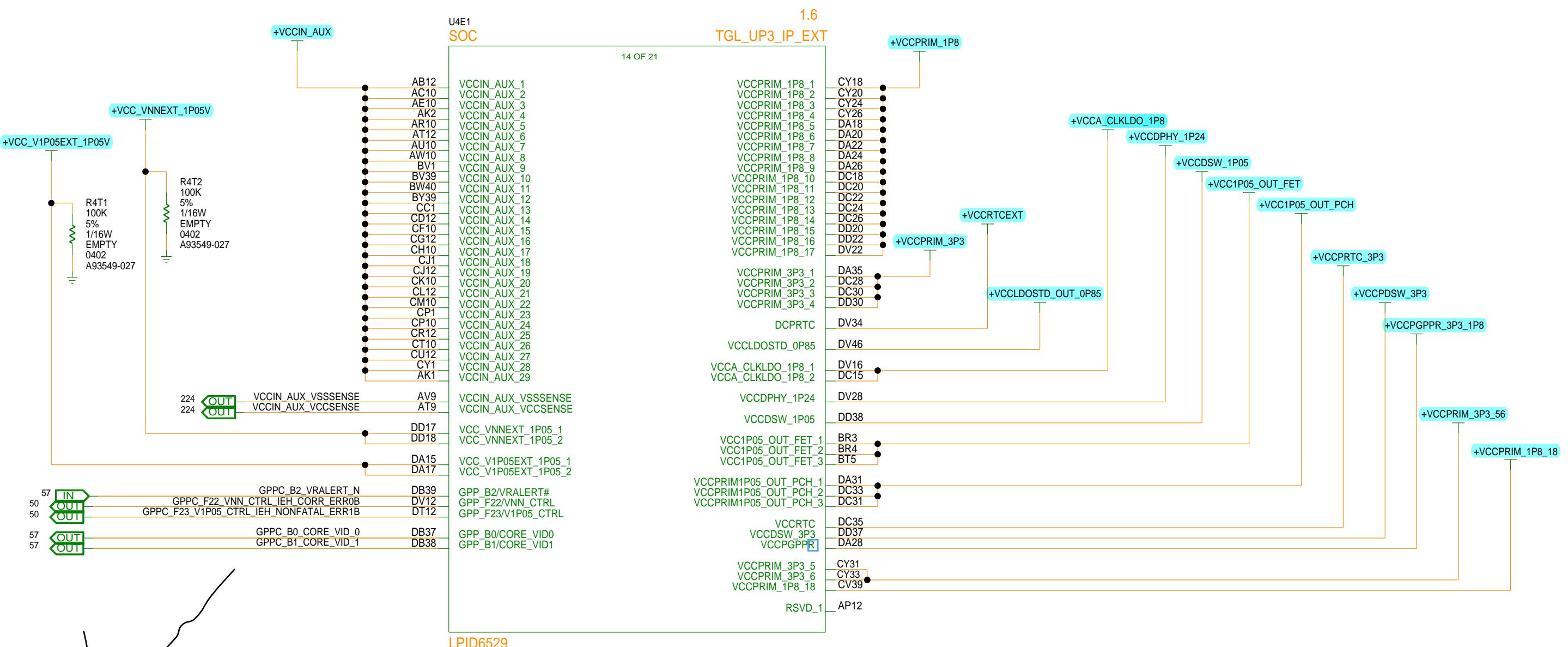
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tigerlake_u_ddr4.sch_156
Wed Dec 18 18:06:14 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	56	1.0

[PAGE_TITLE=CPU PDBOM 2 OF 2]

CUSTOM TEXT BPAGE

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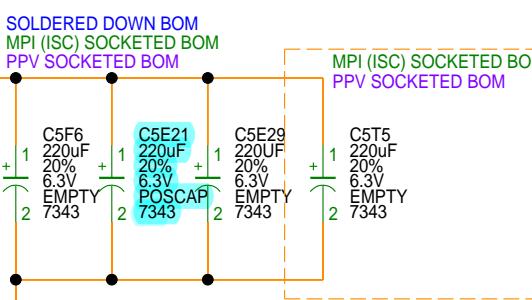


VCCIN_AUX_1P8

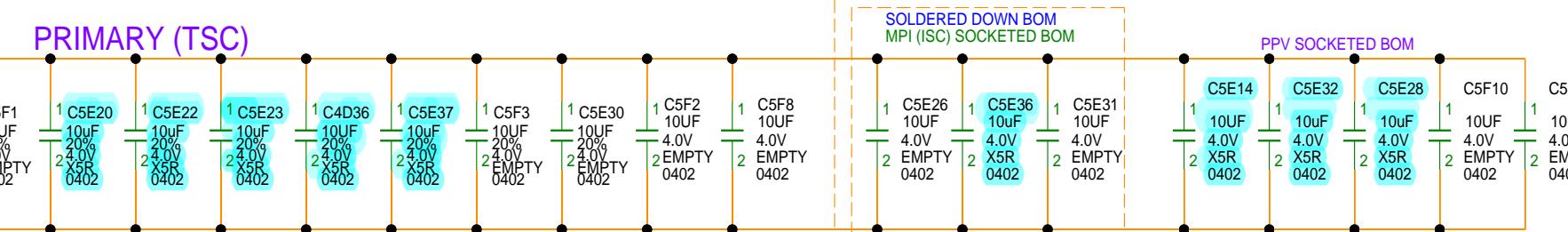
MODULE REV DETAILS

MODULE NAME	REV	DATE

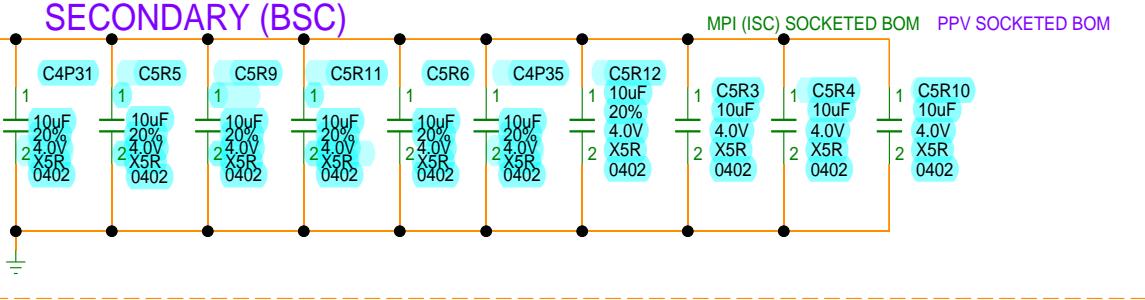
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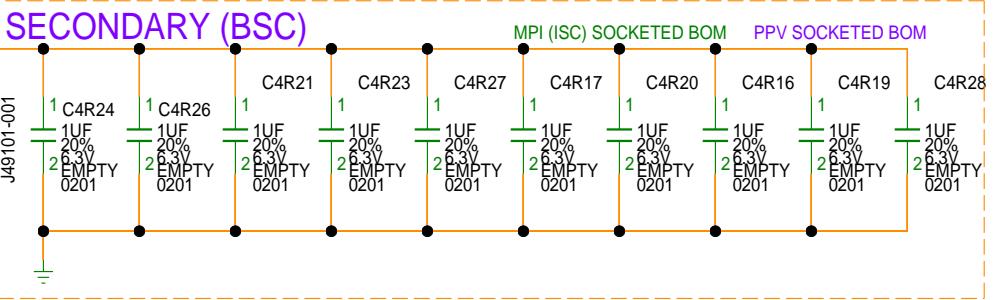
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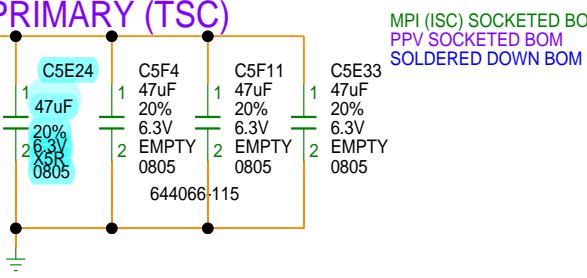
SECONDARY (BSC)



SECONDARY (BSC)

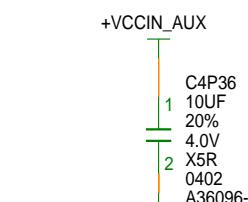


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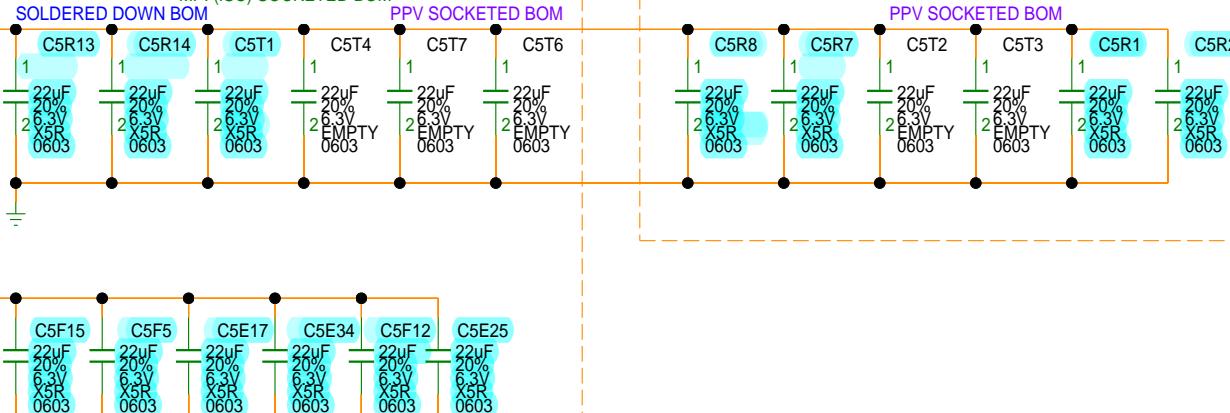


+VCCIN_AUX

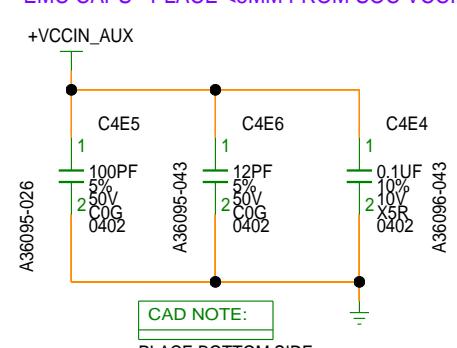
CAP ADDED FOR PI SIMULATION AS PER PI FEEDBACK
PLACE CLOSE TO PIN AK1 of SoC



SOLDERED DOWN BOM



EMC CAPS - PLACE <5MM FROM SOC VCCIN_AUX



[PAGE_TITLE=PDBOM- VCCIN_AUX]

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.58
Wed Dec 18 18:42:42 2019

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CONFIDENTIAL

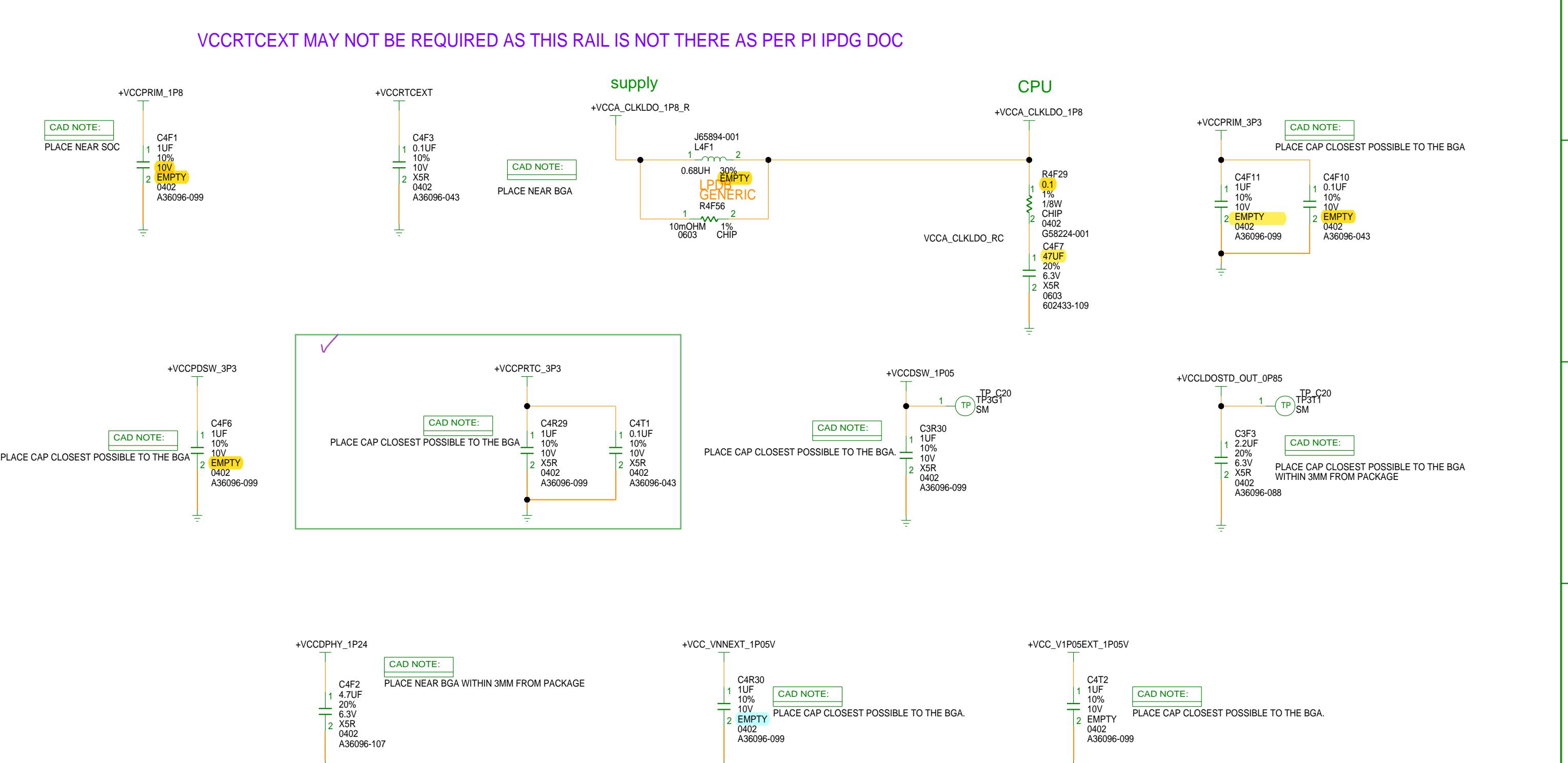
DOCUMENT_NUMBER
609003
PAGE
58
REV
1.0

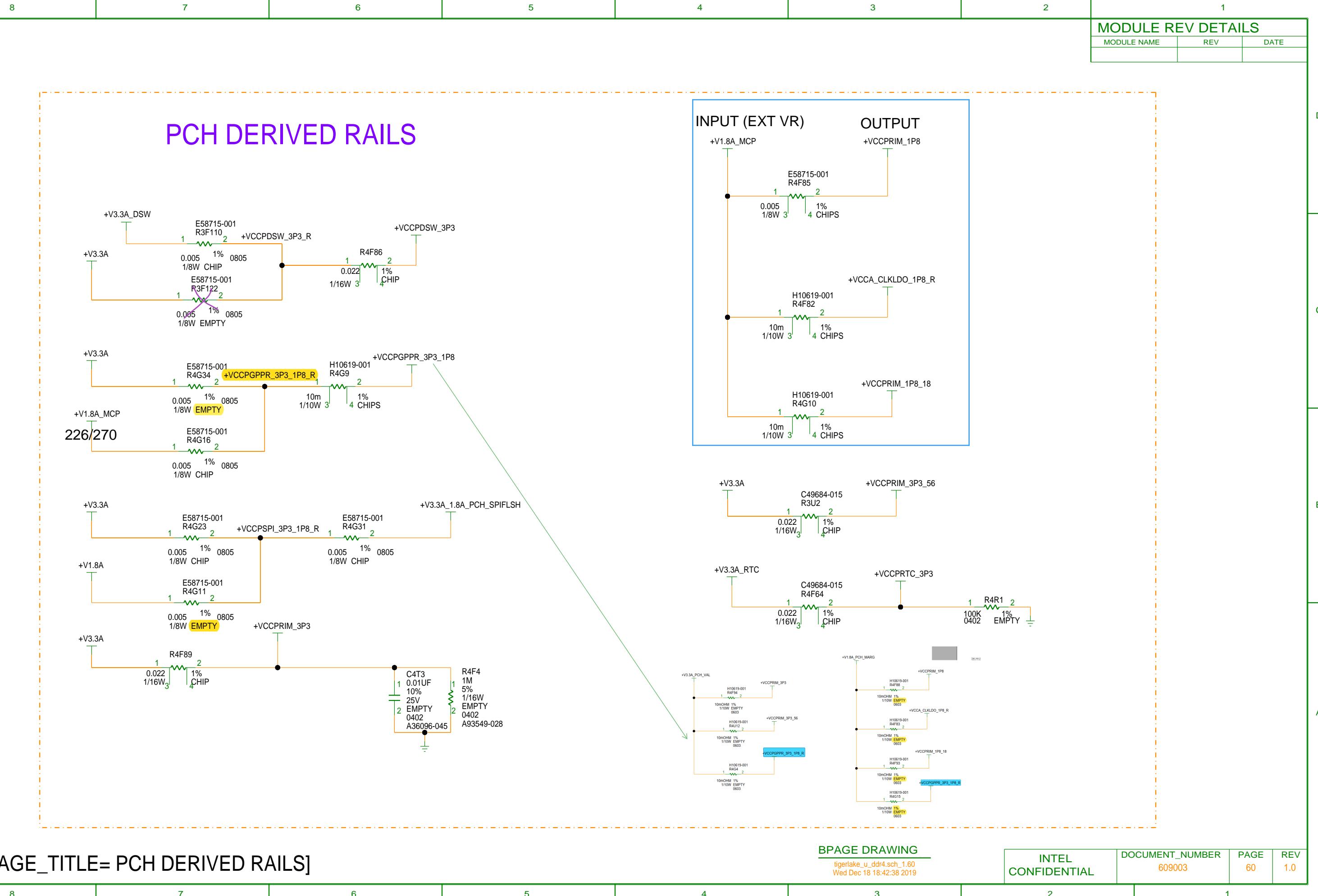
CUSTOM TEXT BPAGE

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8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

VCCRTCEXT MAY NOT BE REQUIRED AS THIS RAIL IS NOT THERE AS PER PI IPDG DOC





8	7	6	5	4	3	2	1
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PCH MARGINING RAILS

MODULE REV DETAILS

MODULE NAME	REV	DATE

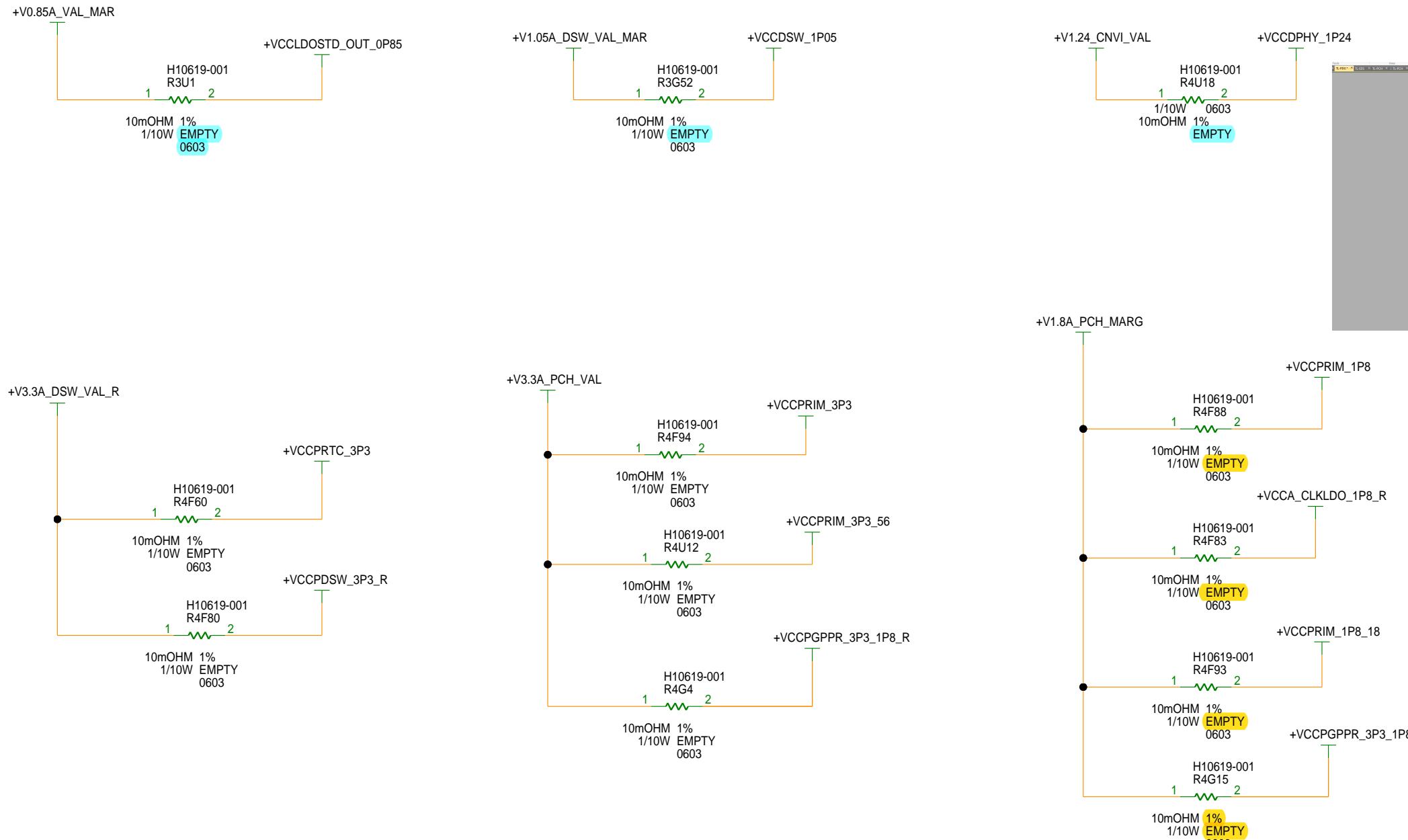


Table 237. No Direct Switching or No External Bypass Supported						
State Enable	Q1 CNVI	Q2 ISH	Q3 Type A	Q4 C-Link	Q5 SMBus	Q6 PHY PG
S02.0	Always Enable	-	-	-	-	-
S02.1	Always Enable	-	-	-	-	-
S02.2	-	-	NO	-	-	YES
S03.0	NO	NO	-	-	-	-
S03.1	NO	NO	-	-	-	-
S03.2	NO	NO	-	-	-	-
S03.3	NO	NO	NO	-	-	YES

Voltage Margining
Voltage margining allows bypass VRs to reduce their voltages depending on S03.x states. To enable this feature, VNN_CTRL and V1P05_CTRL GPIO pins should be configured. This feature can reduce power in Soix states.

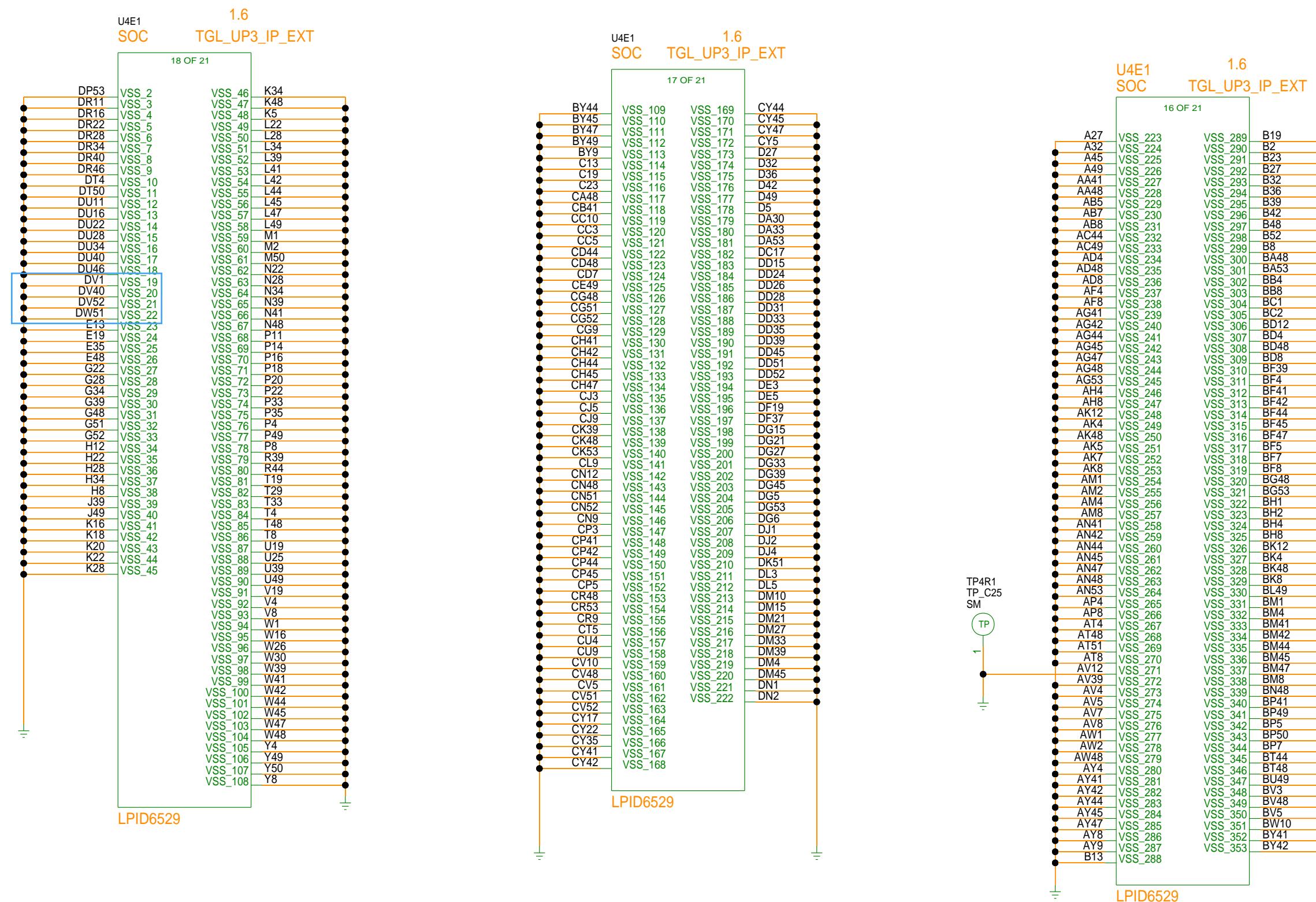
Tiger Lake UP3 UP4 H35 UP3 Refresh Platform

November 2020

8	7	6	5	4	3	2	1
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MODULE REV DETAILS

MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)]

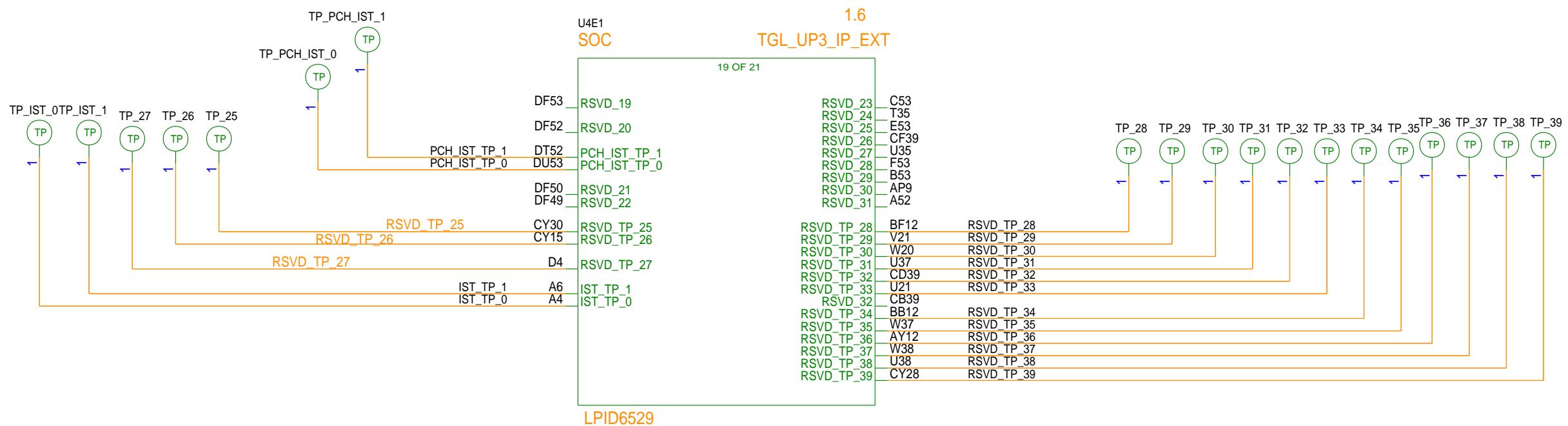
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tigerlake_u_ddr4.sch_1.62
Wed Dec 18 18:06:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 62	REV 1.0
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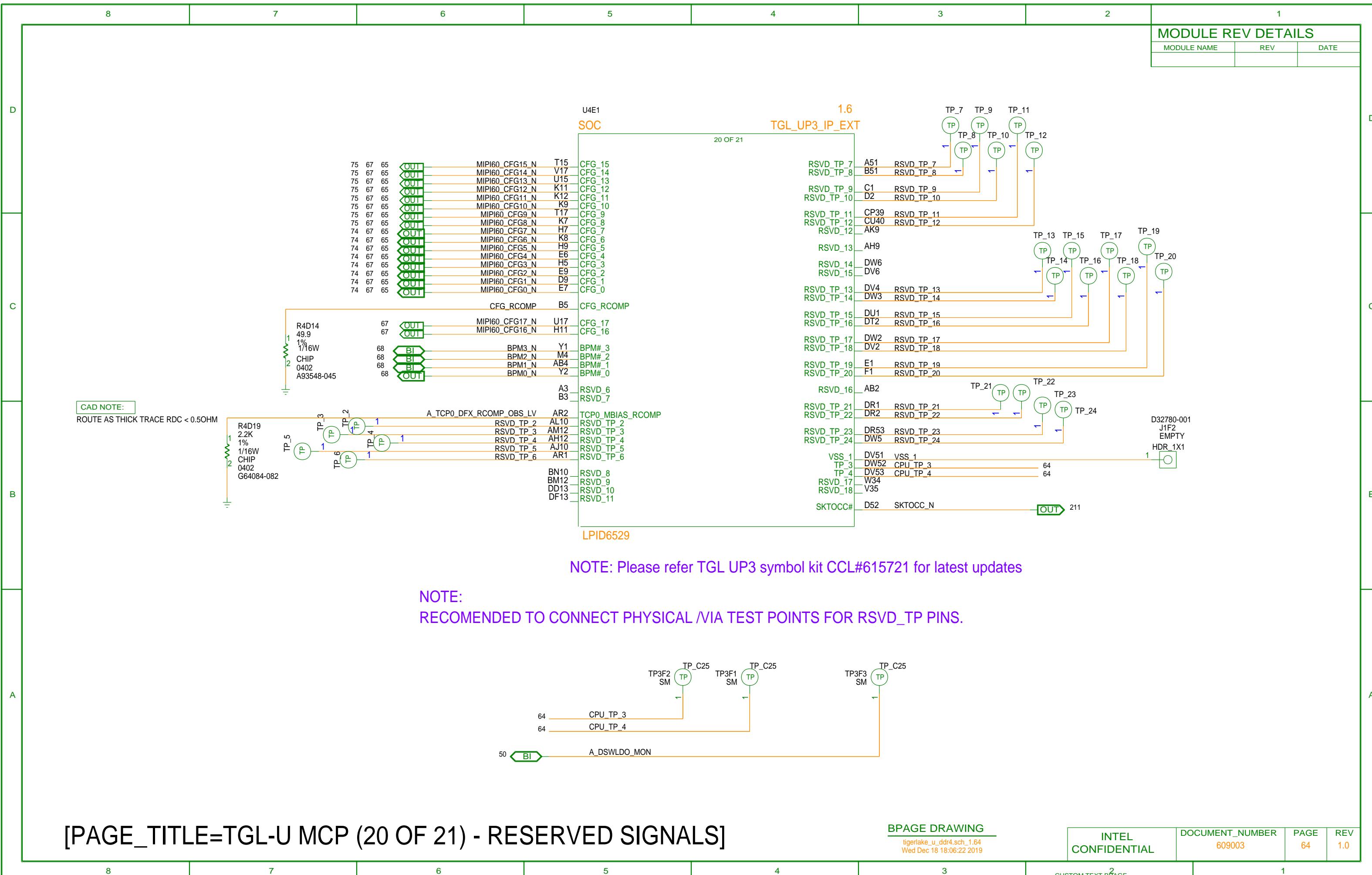
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MODULE REV DETAILS						MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

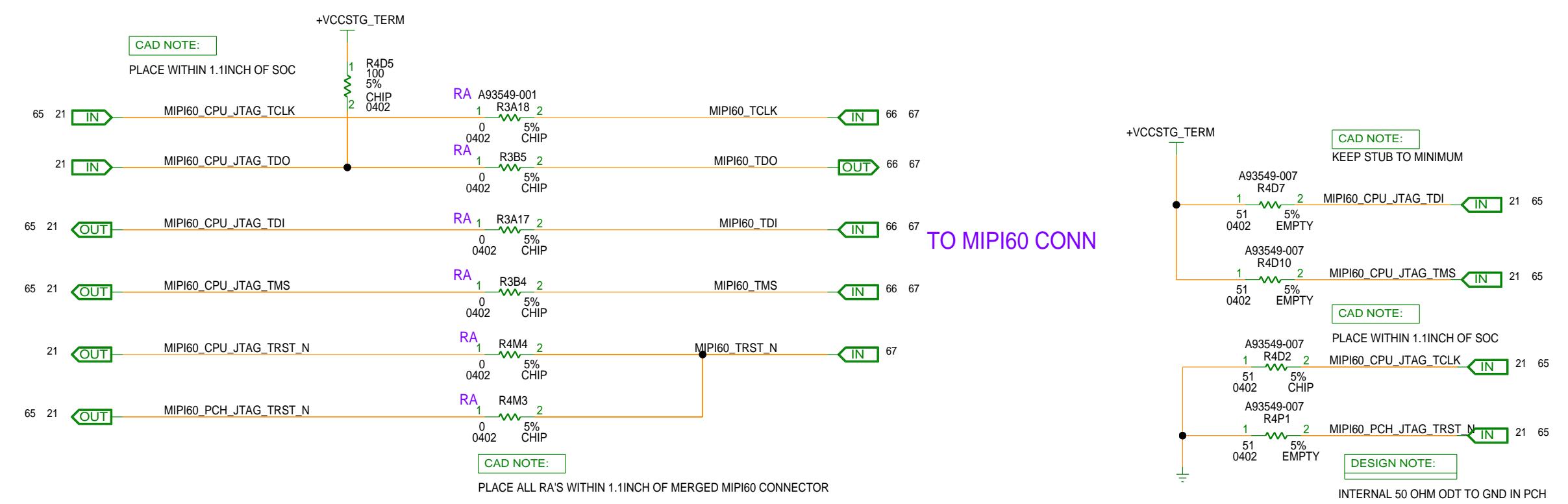
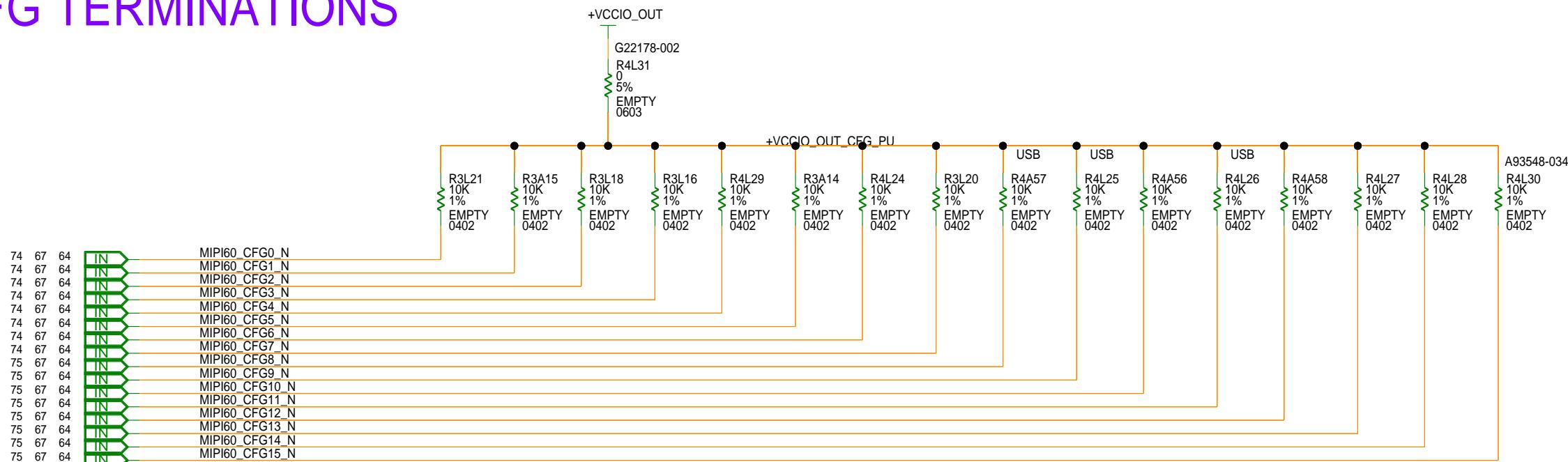
NOTE:

RECOMENDED TO CONNECT PHYSICAL /VIA TEST POINTS FOR RSVD_TP PINS.

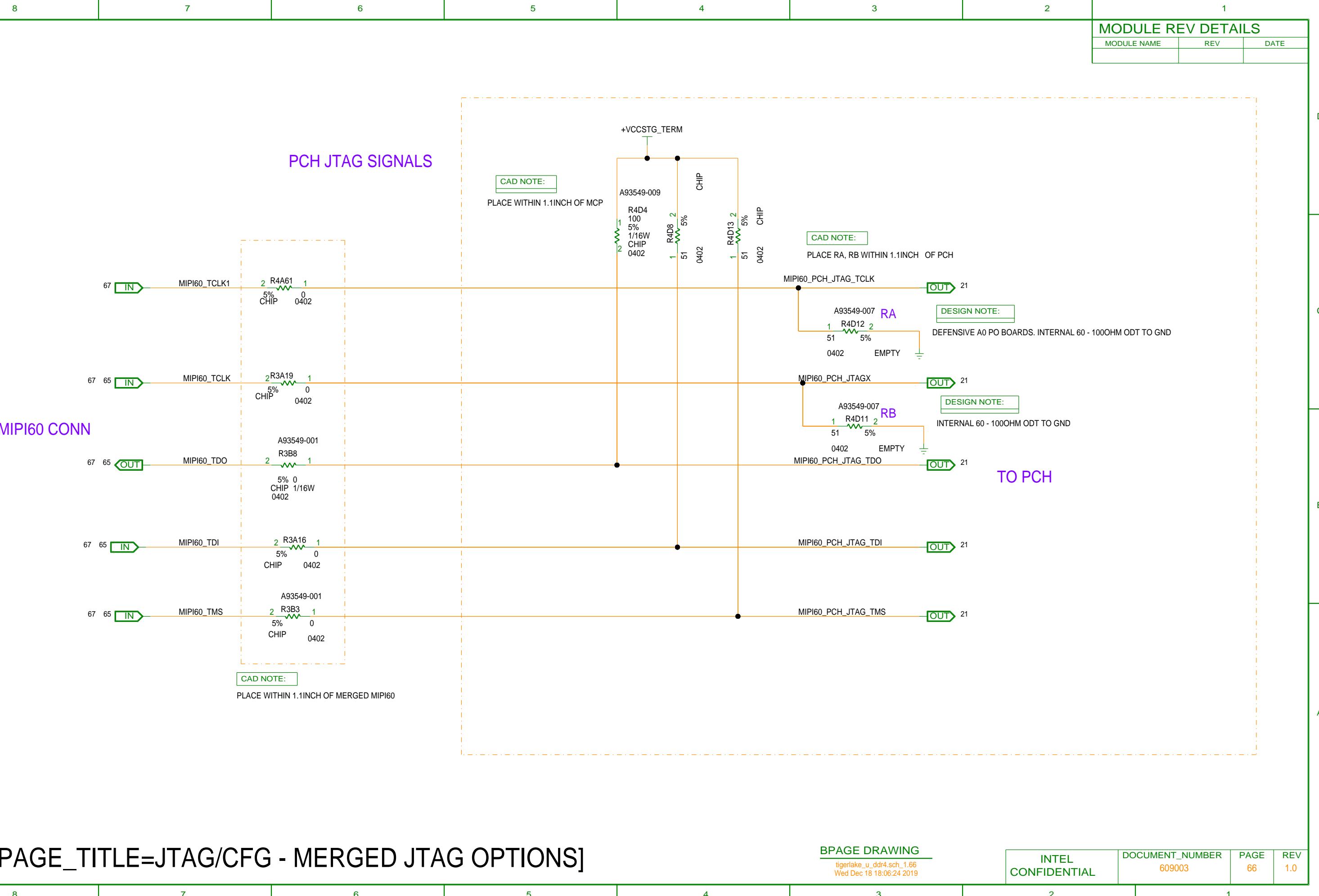


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MODULE REV DETAILS							
MODULE NAME	REV	DATE					

CFG TERMINATIONS



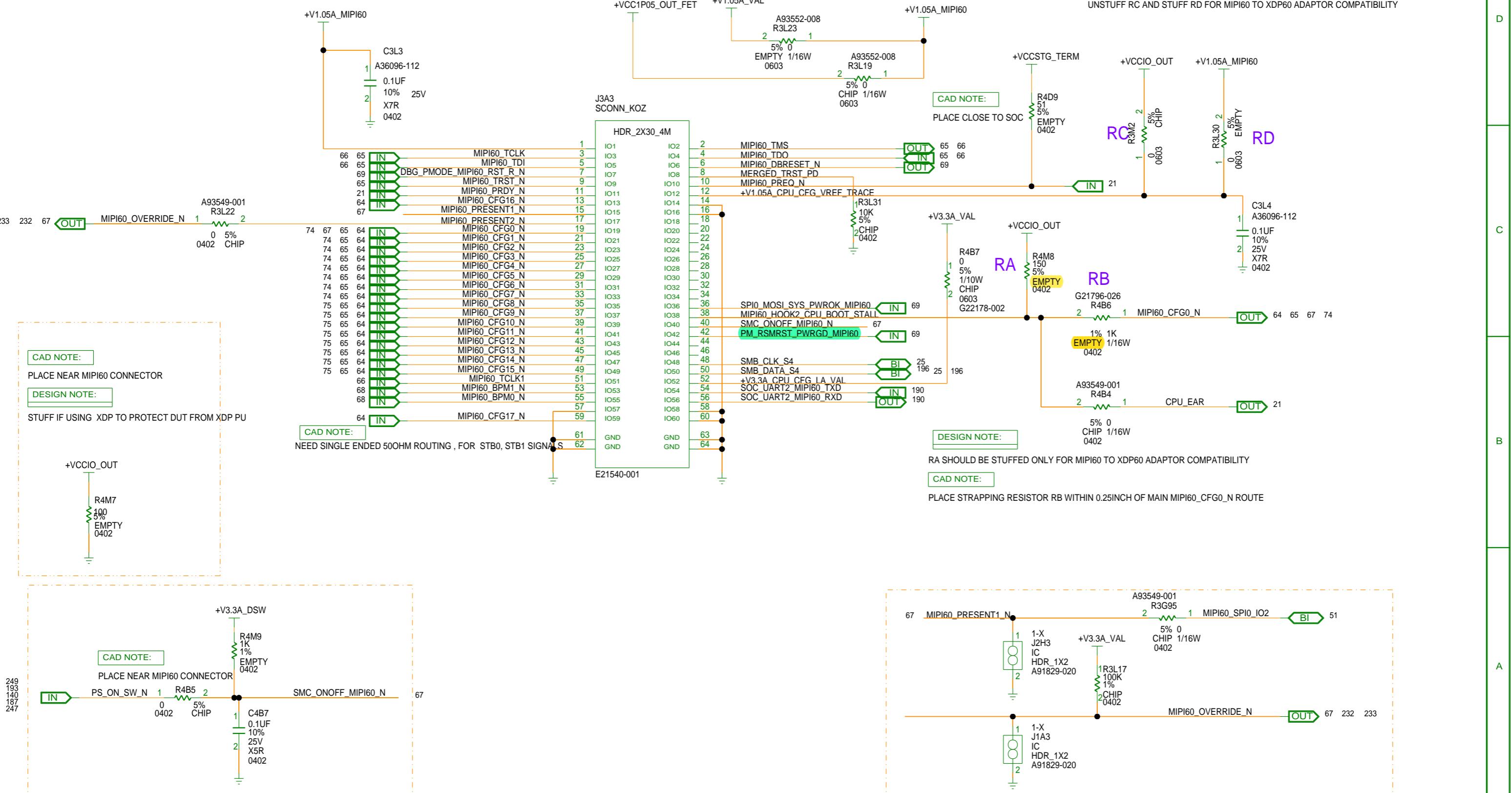
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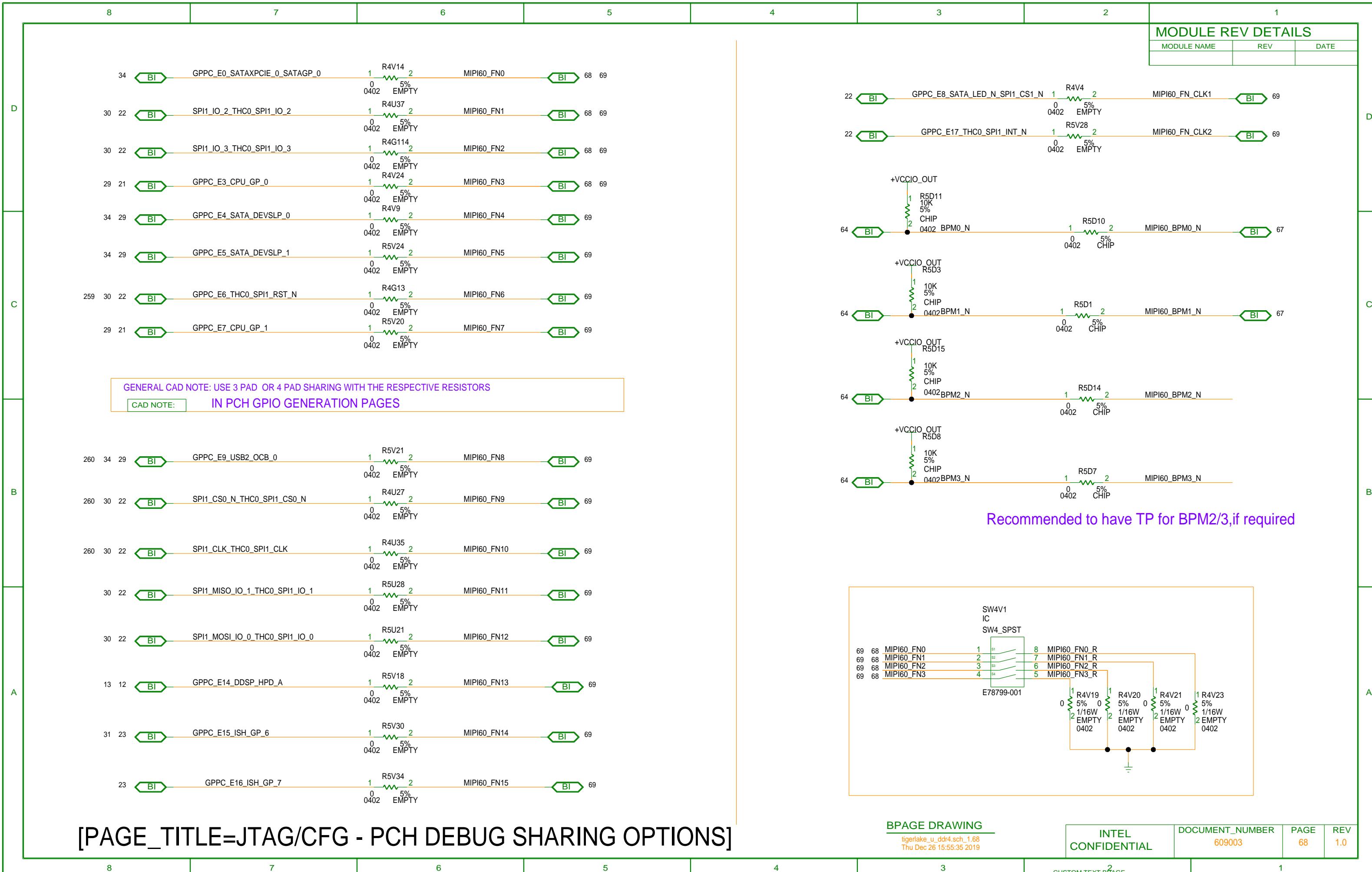


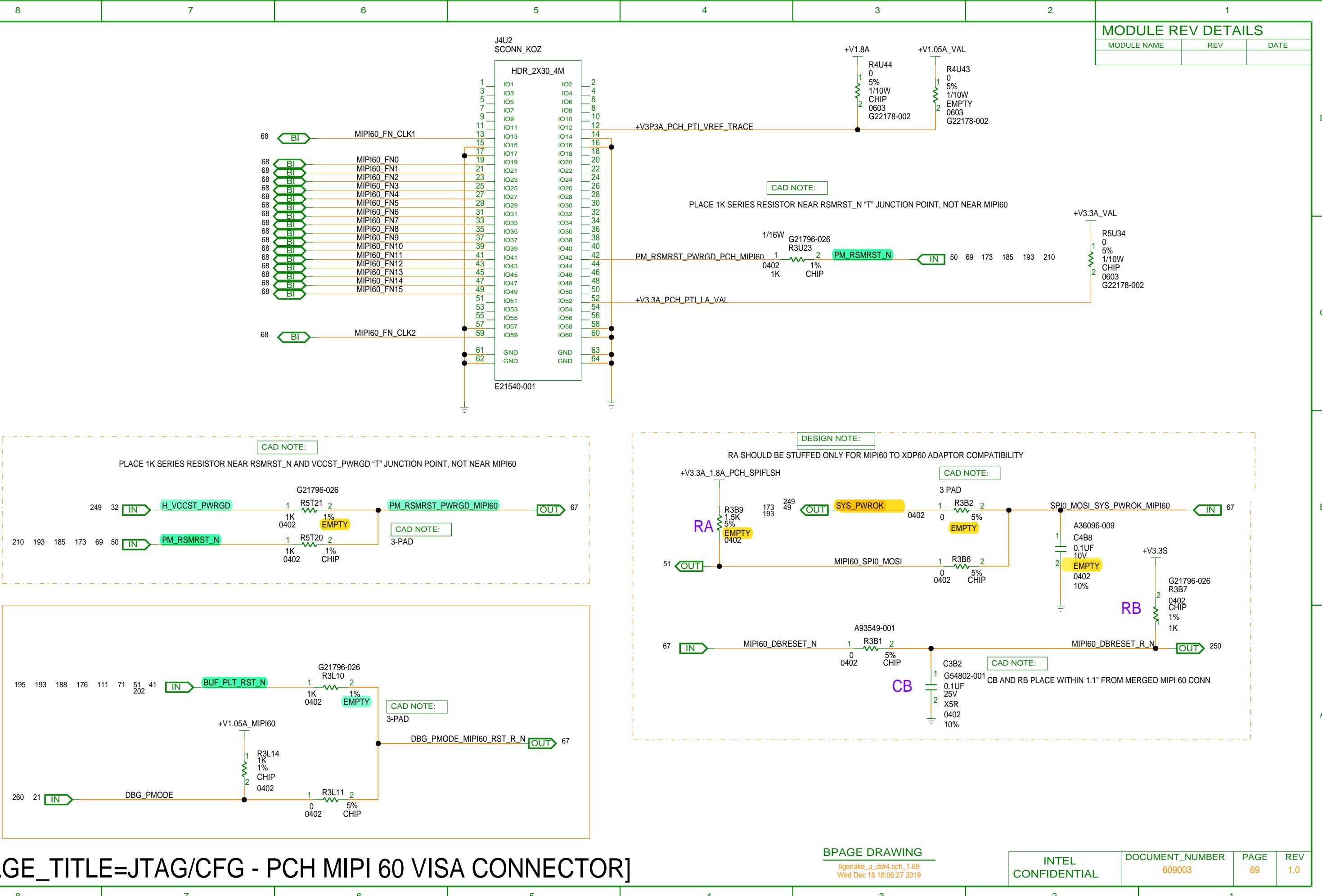
MIPI 60

MODULE REV DETAILS

MODULE NAME	REV	DATE





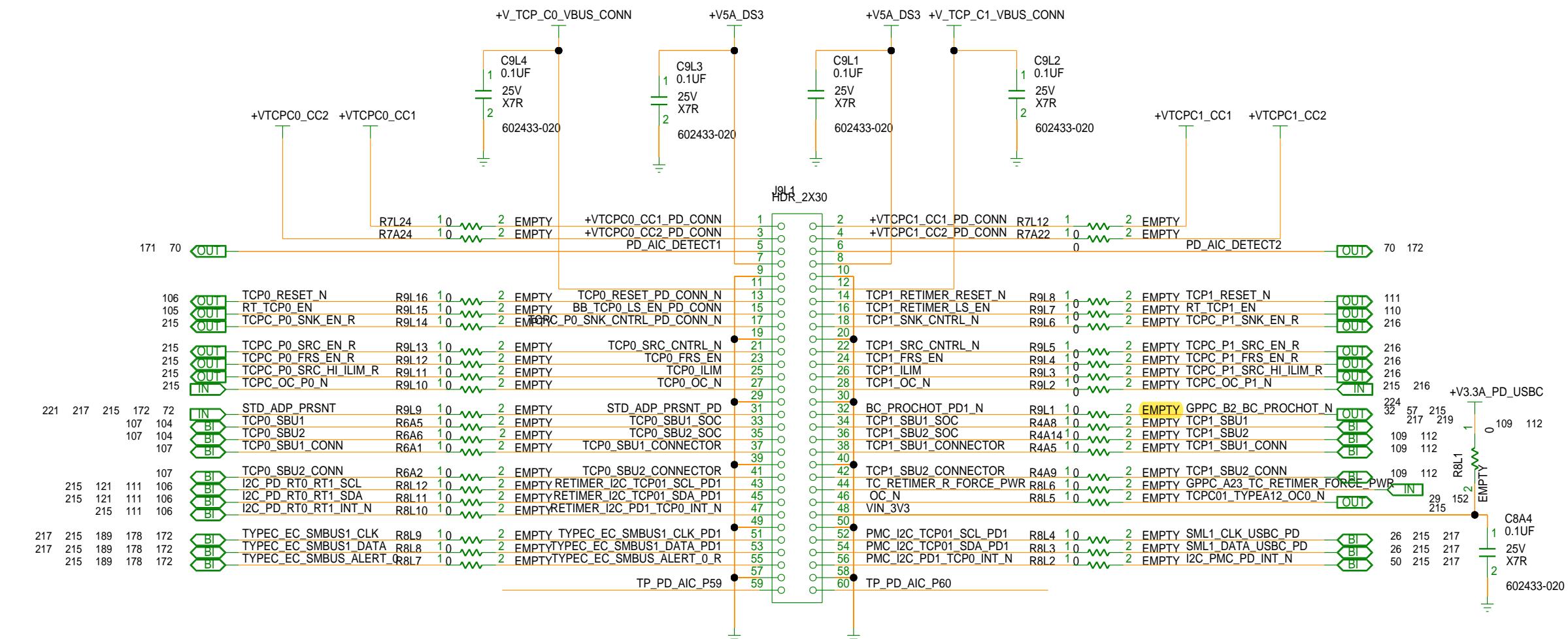


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PD AIC CONTROLLER

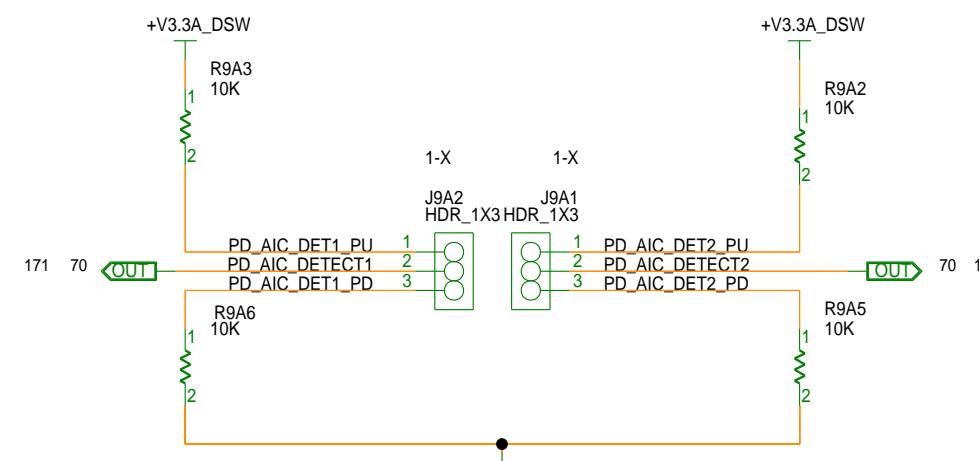
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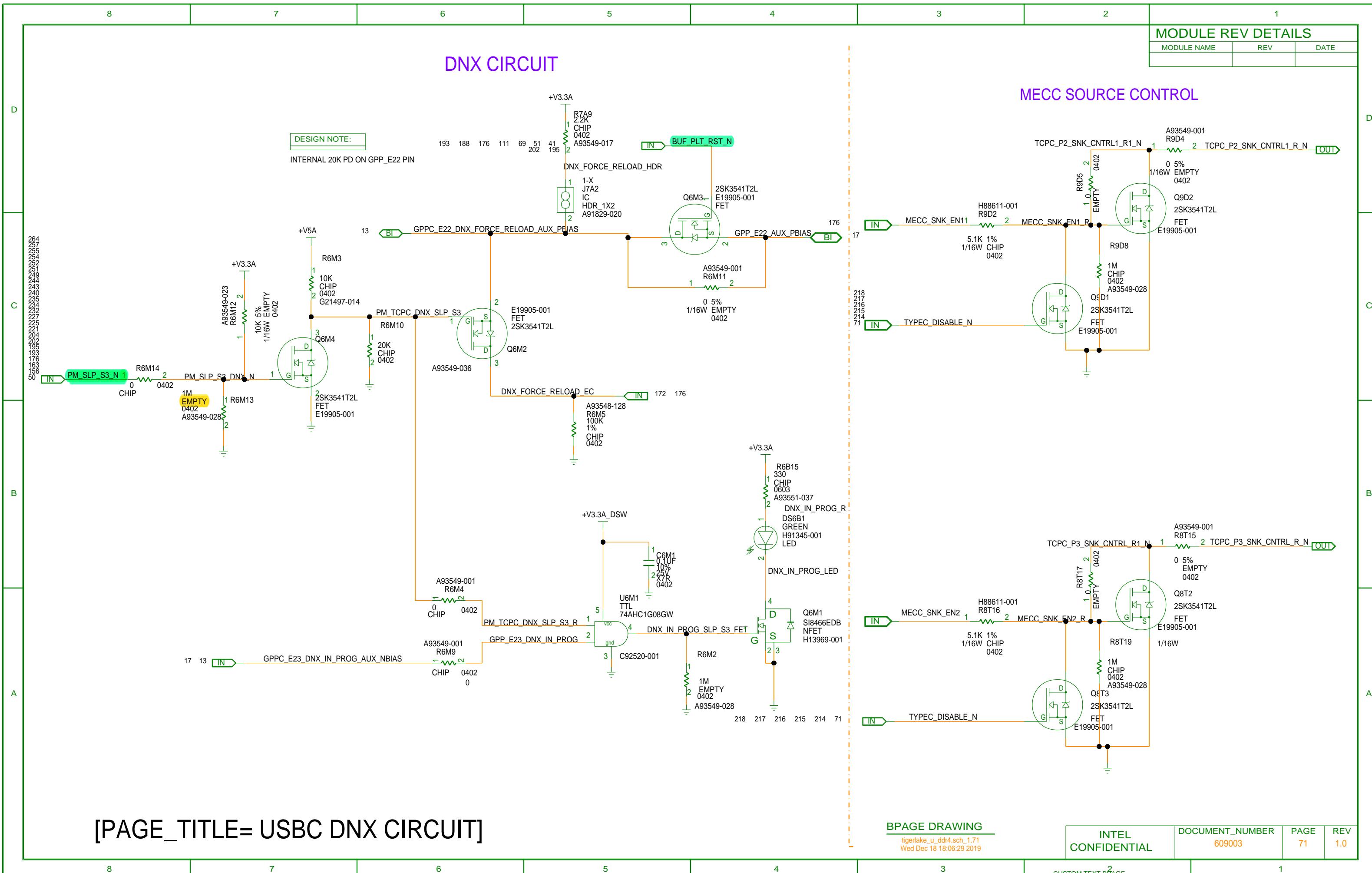
MODULE NAME	REV	DATE

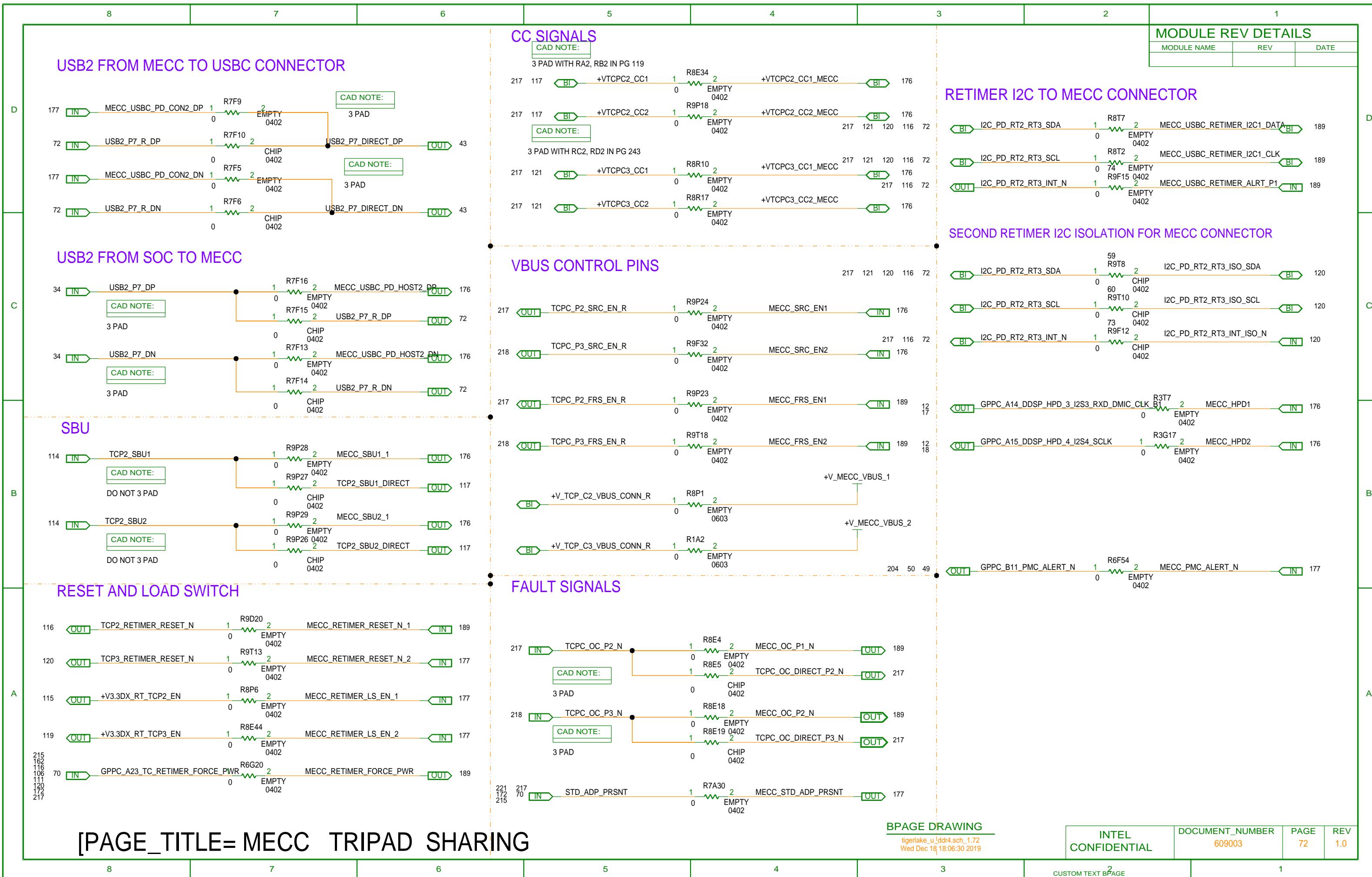


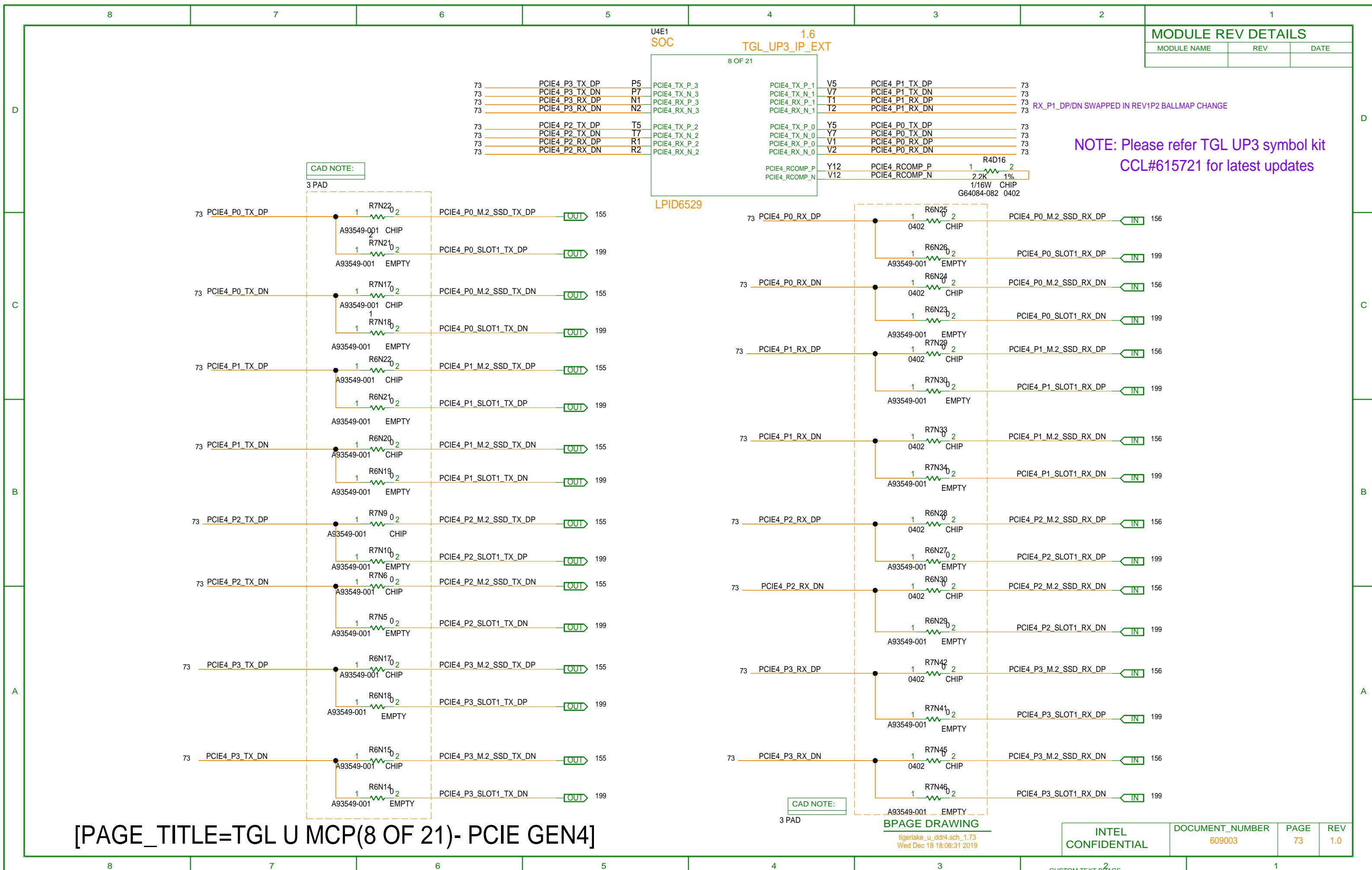
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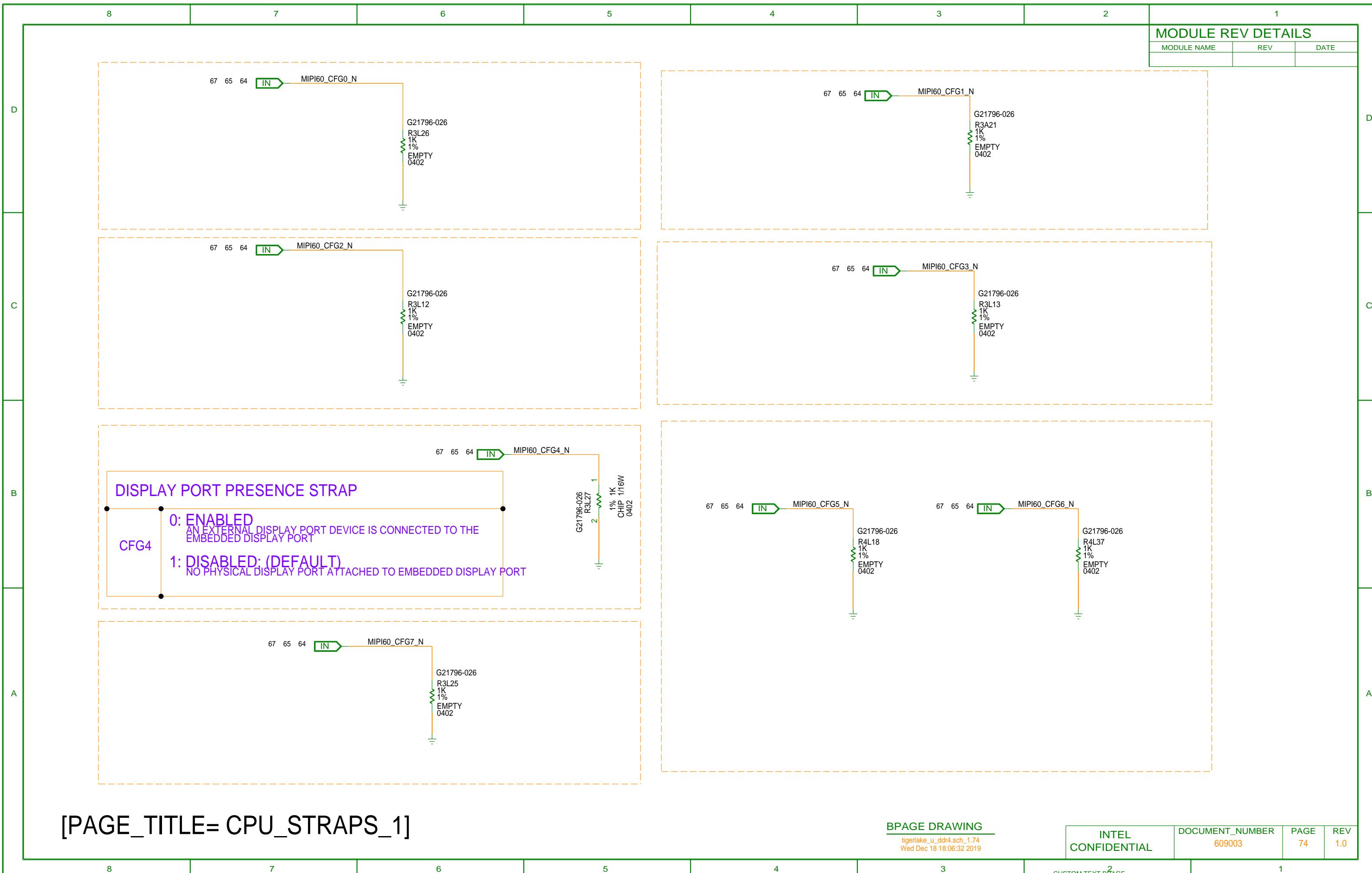
ALL THE RESISTORS IN THIS PAGE SHOULD BE TRIPAD WITH RESPECTIVE RESISTOR IN OTHER SECTION

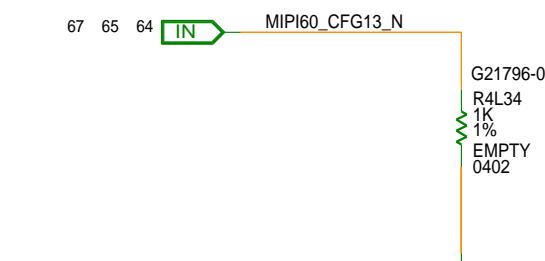
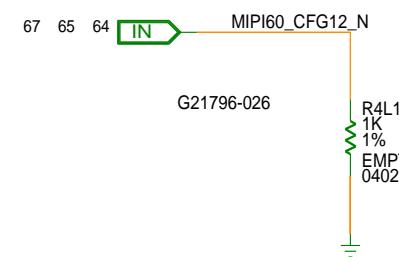
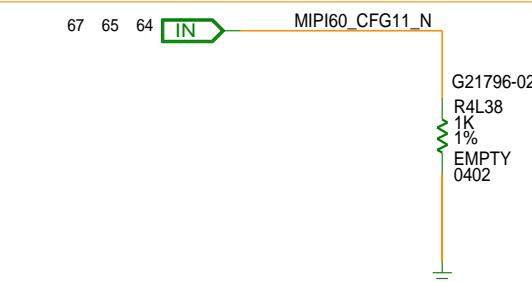
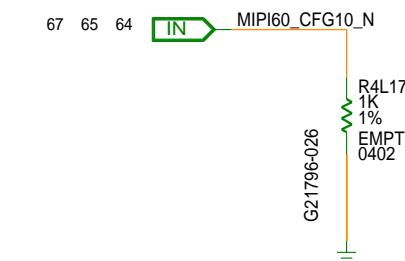
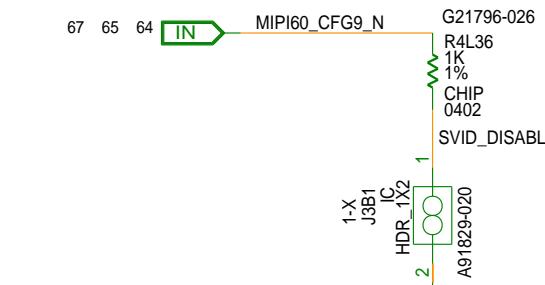
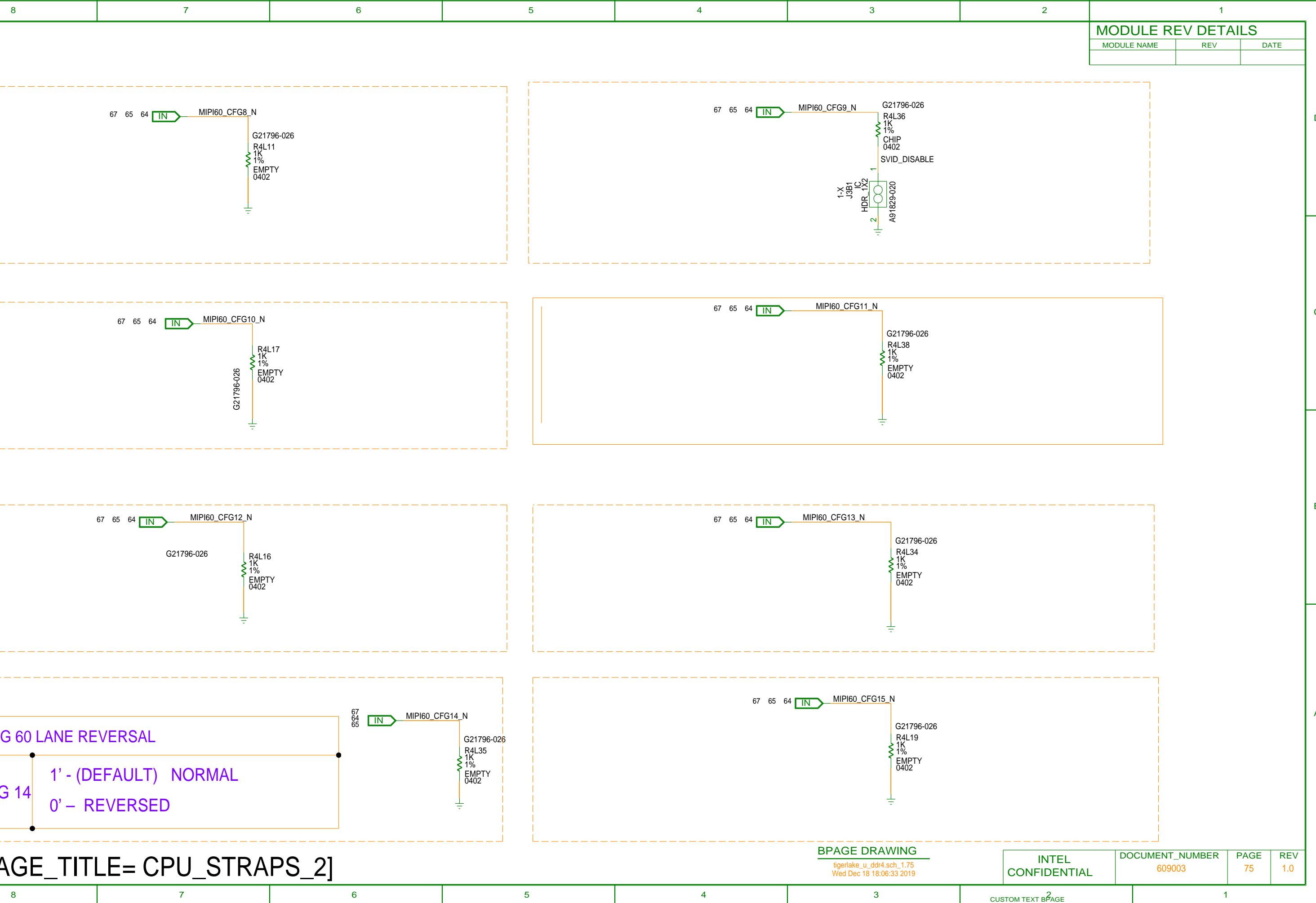












PEG 60 LANE REVERSAL
1' - (DEFAULT) NORMAL
0' – REVERSED
CFG 14

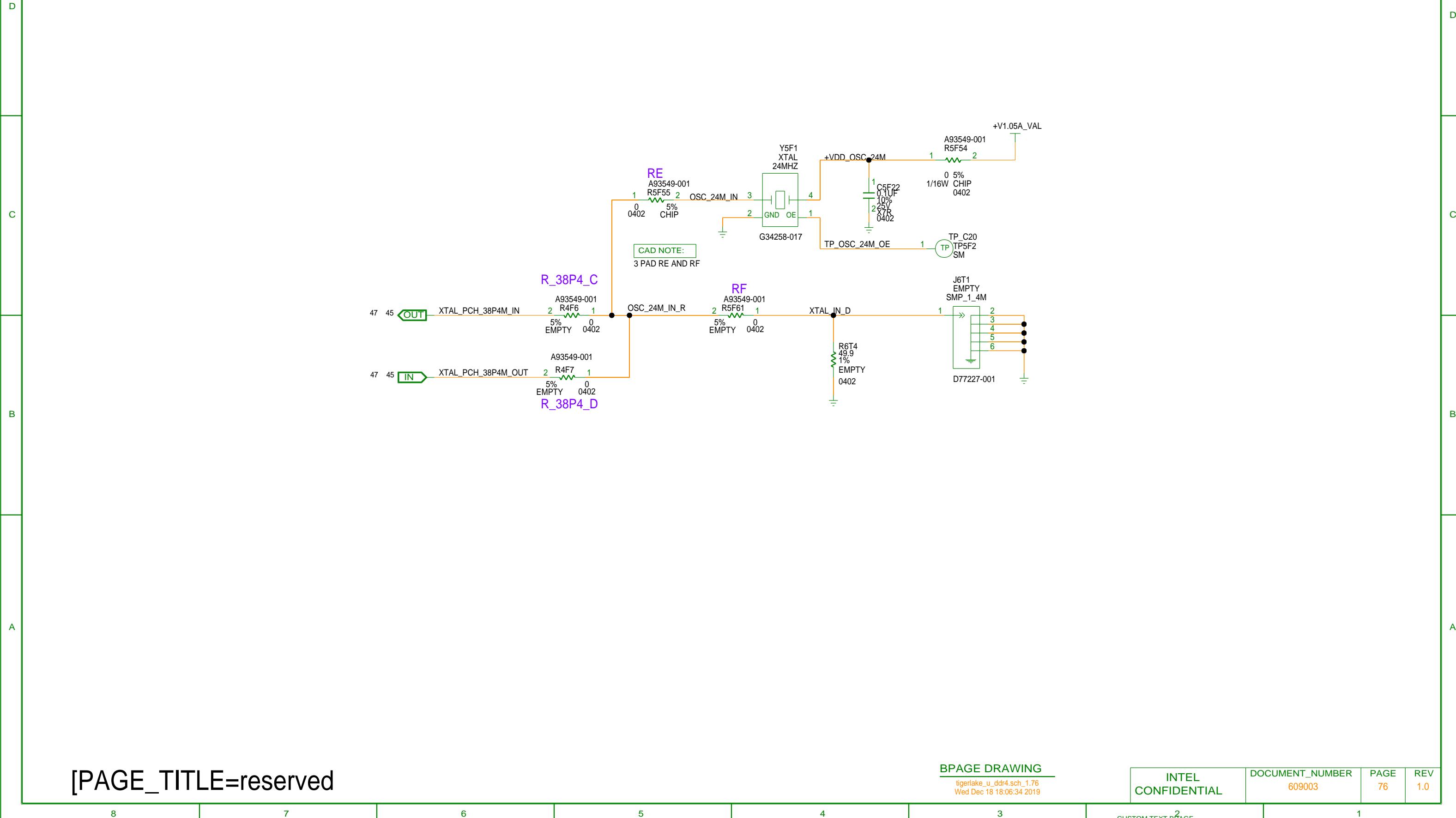
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Wed Dec 18 18:06:33 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 75	REV 1.0

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MODULE REV DETAILS		
MODULE NAME	REV	DATE



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CUSTOM TEXT BPAGE

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MODULE REV DETAILS

MODULE NAME	REV	DATE

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tigerlake_u_ddr4.sch_1.77
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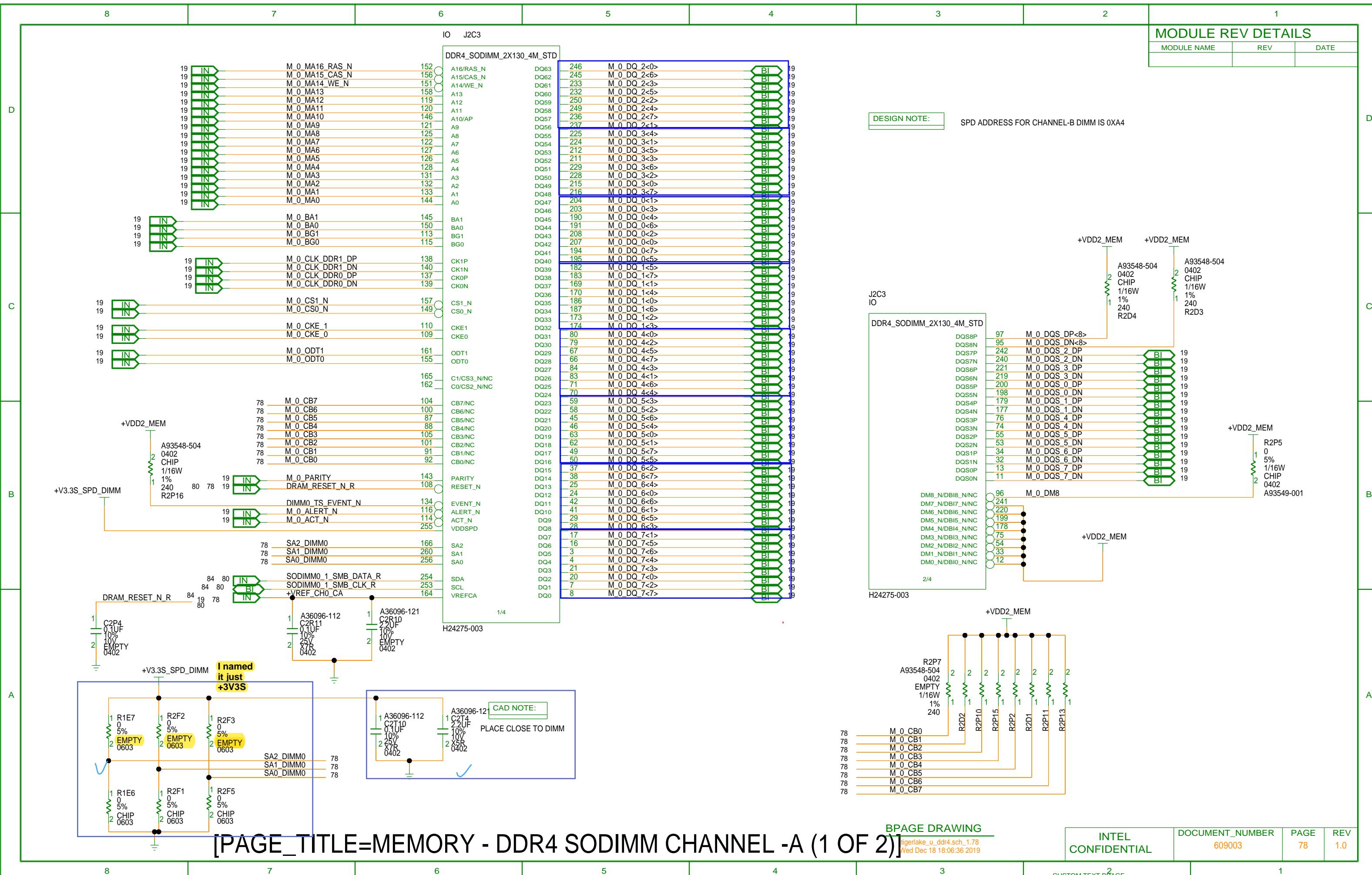
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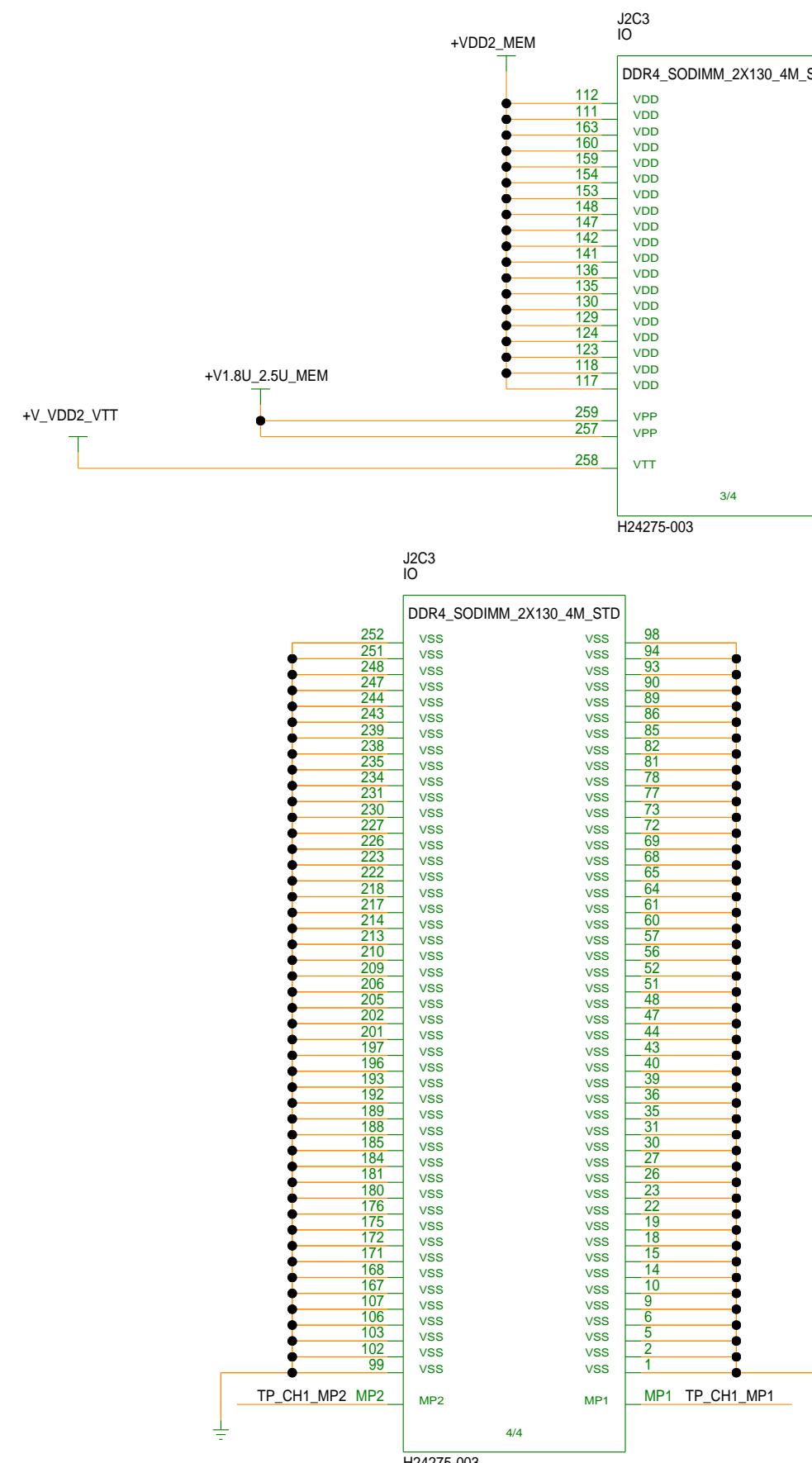
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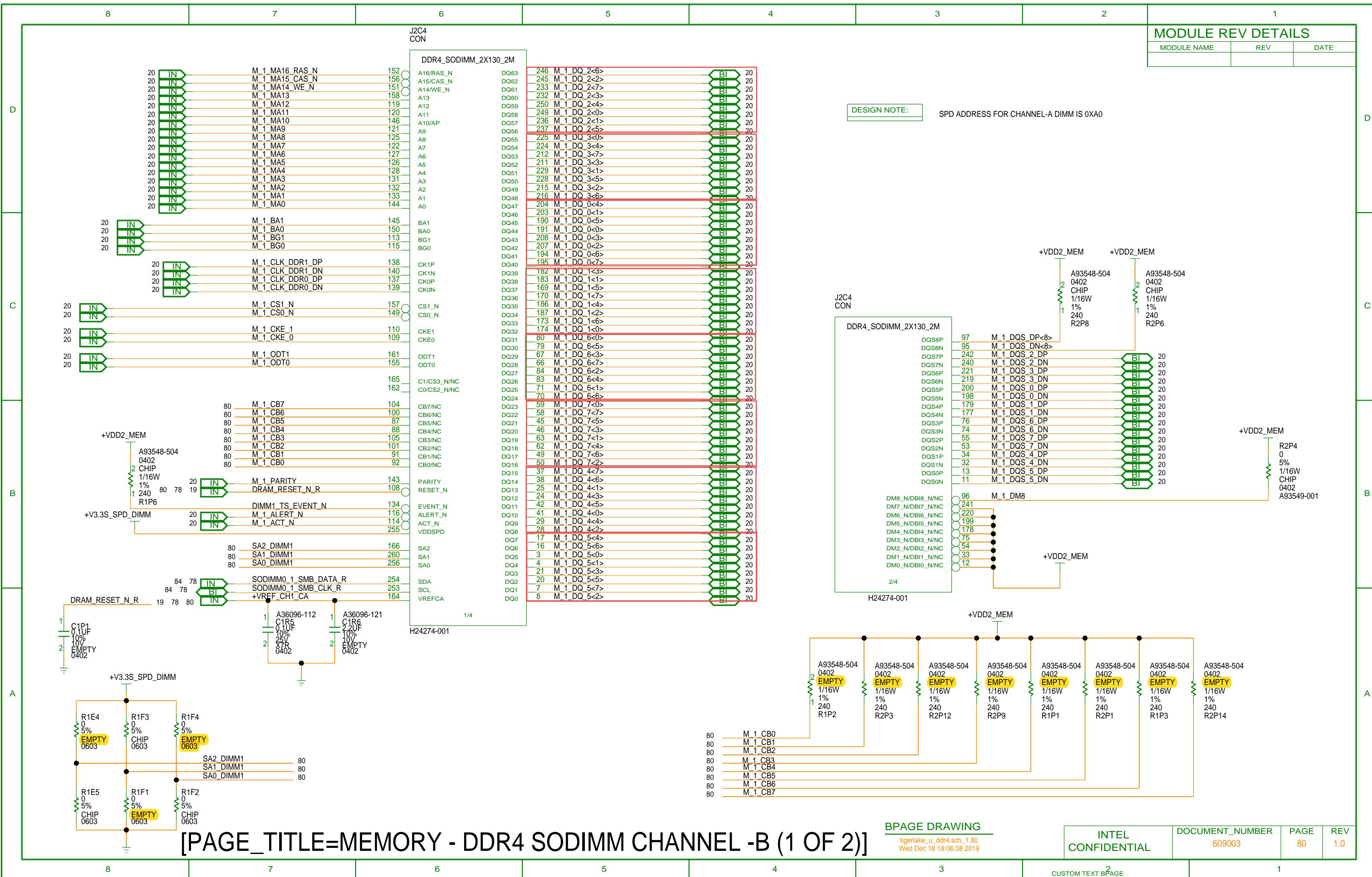
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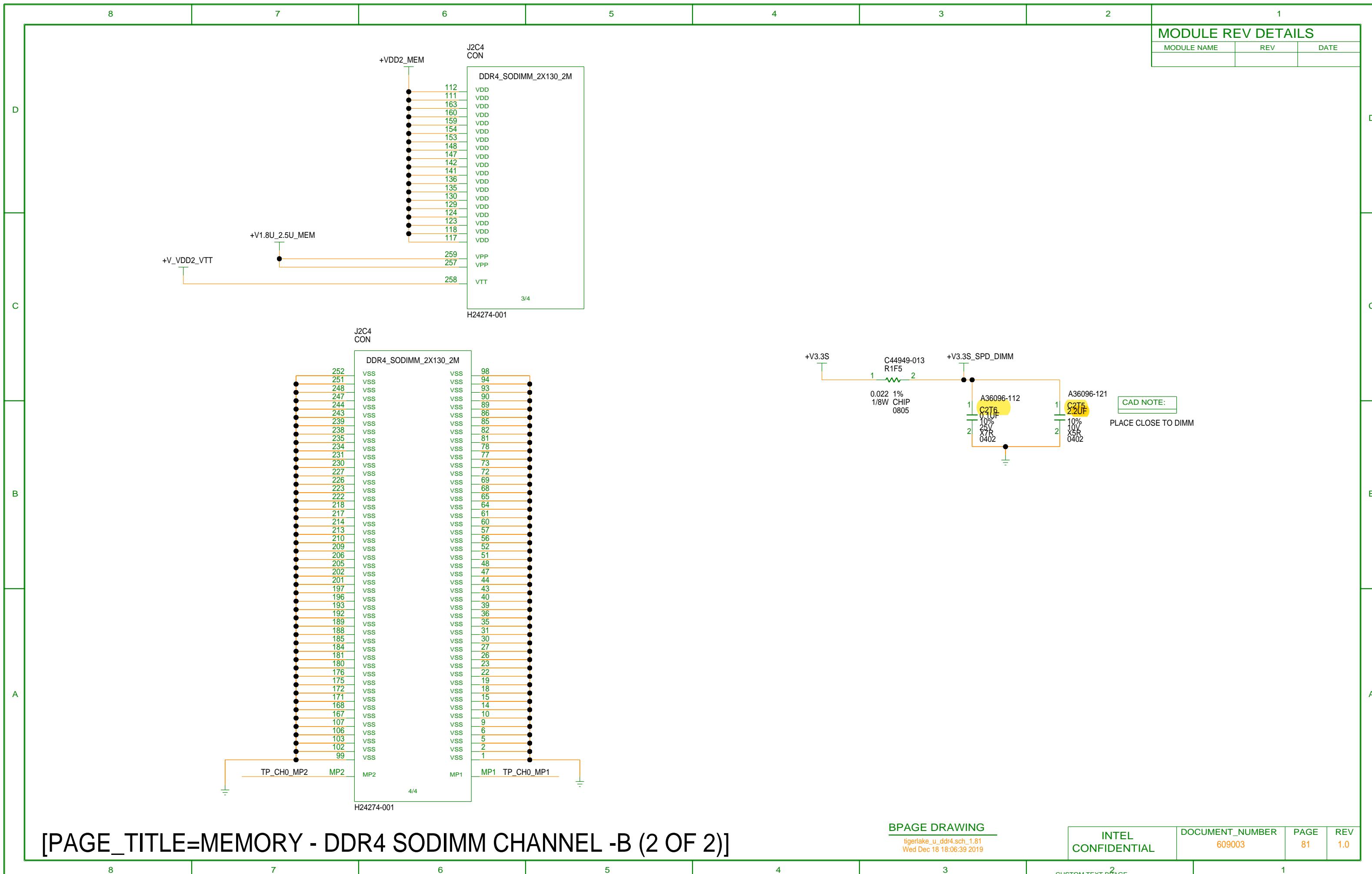
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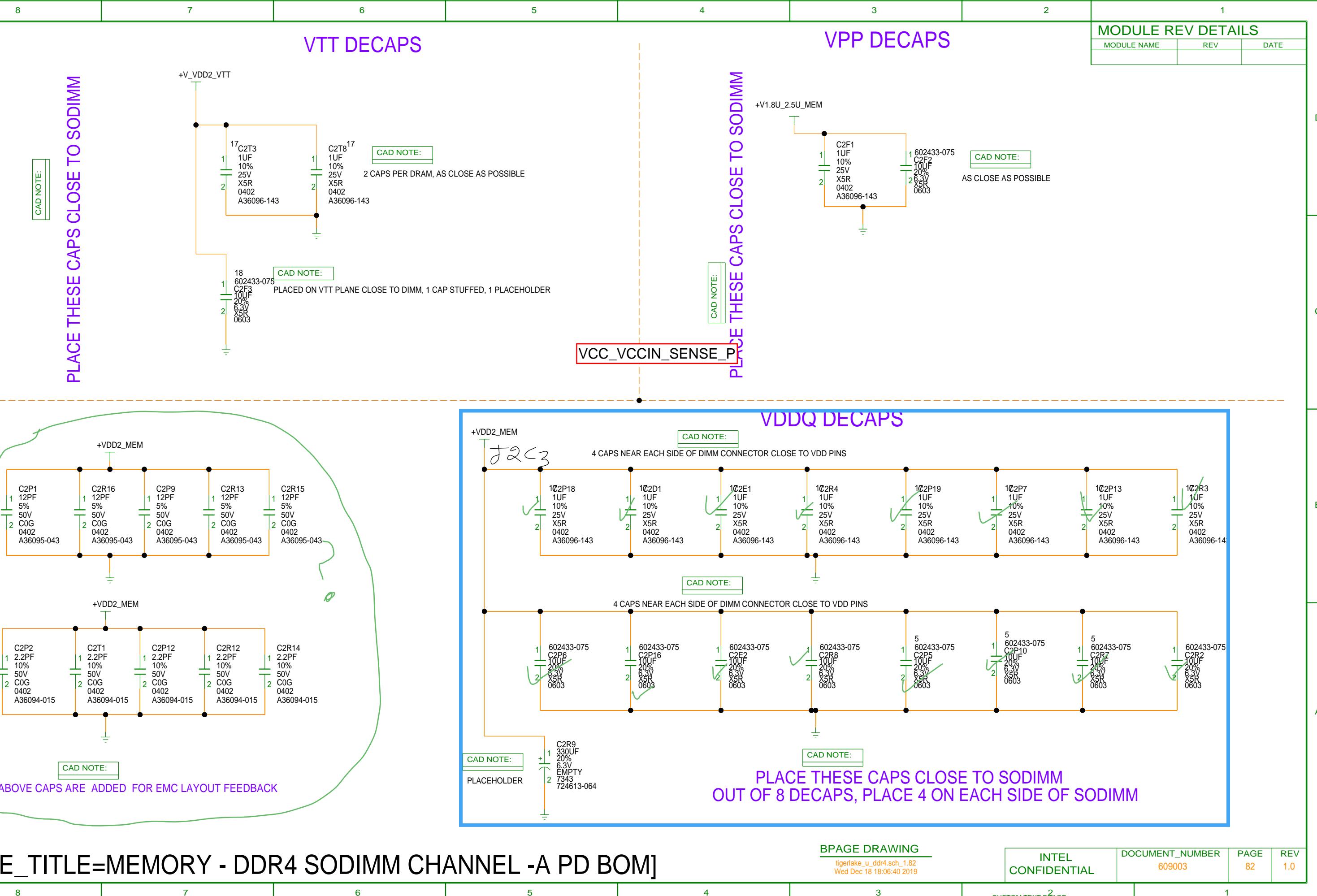
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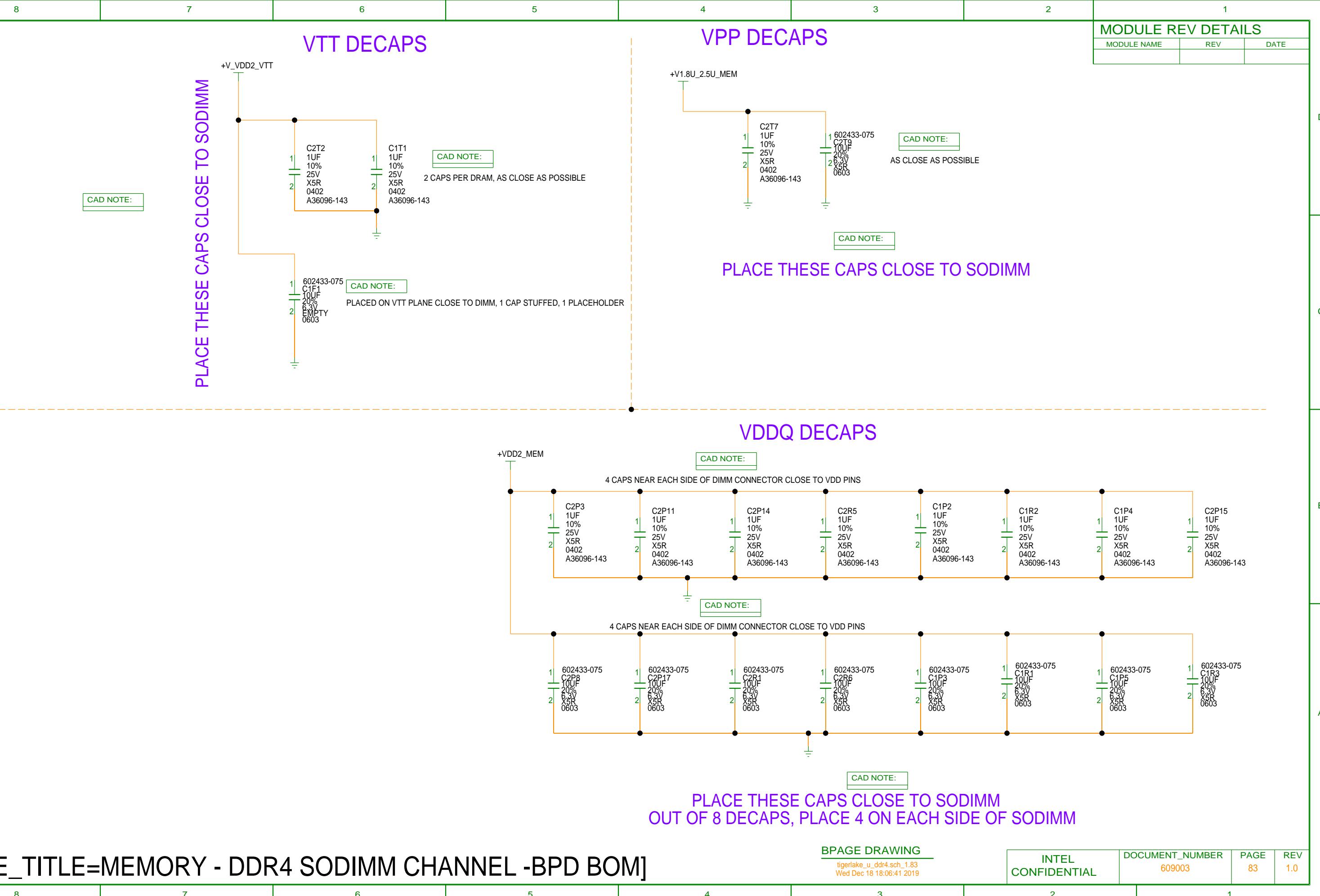
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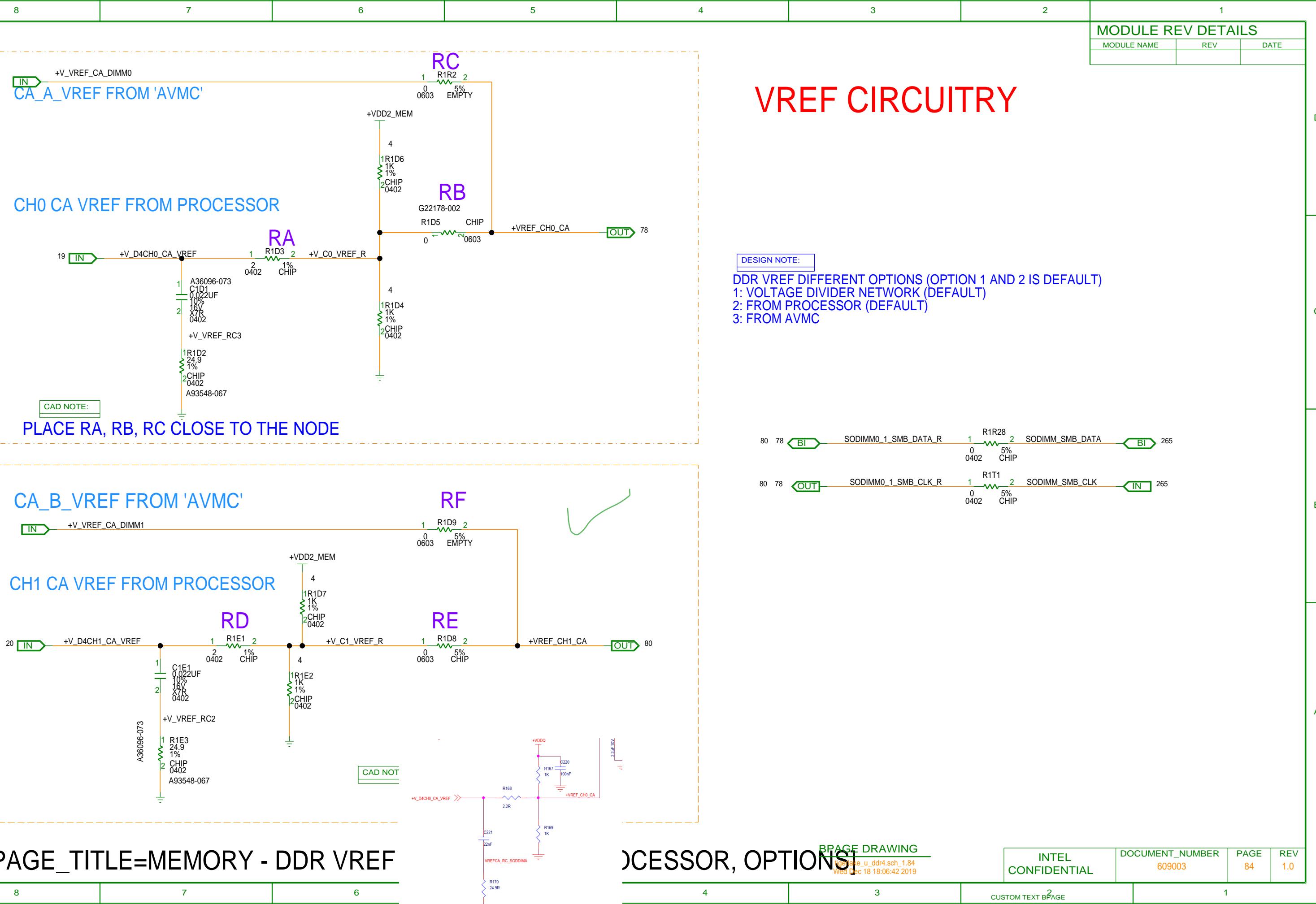












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MODULE REV DETAILS							
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MODULE NAME		REV	DATE				

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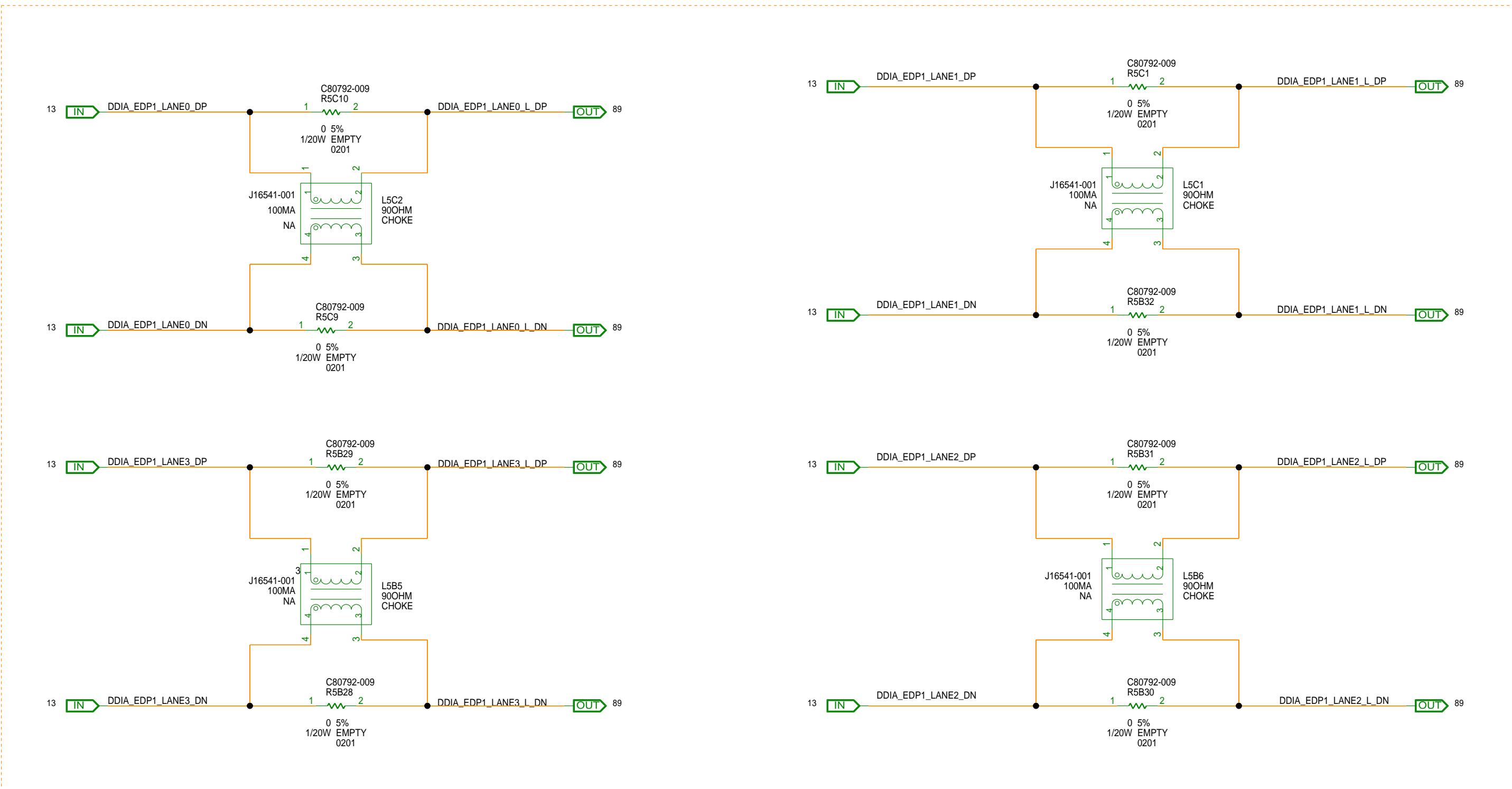
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 86	REV 1.0
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MODULE NAME	REV	DATE					

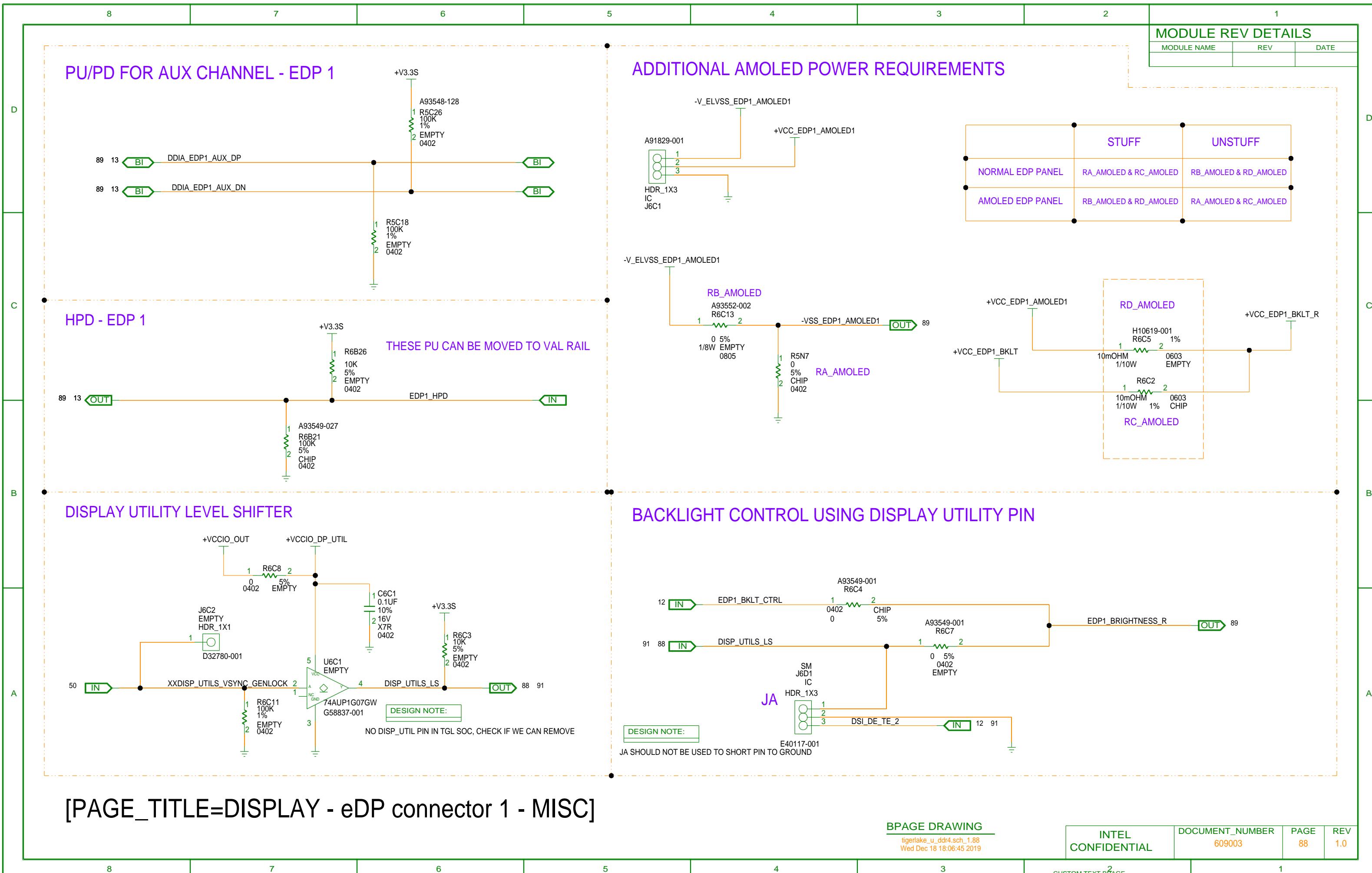
EDP CONNECTOR 1 - CMC



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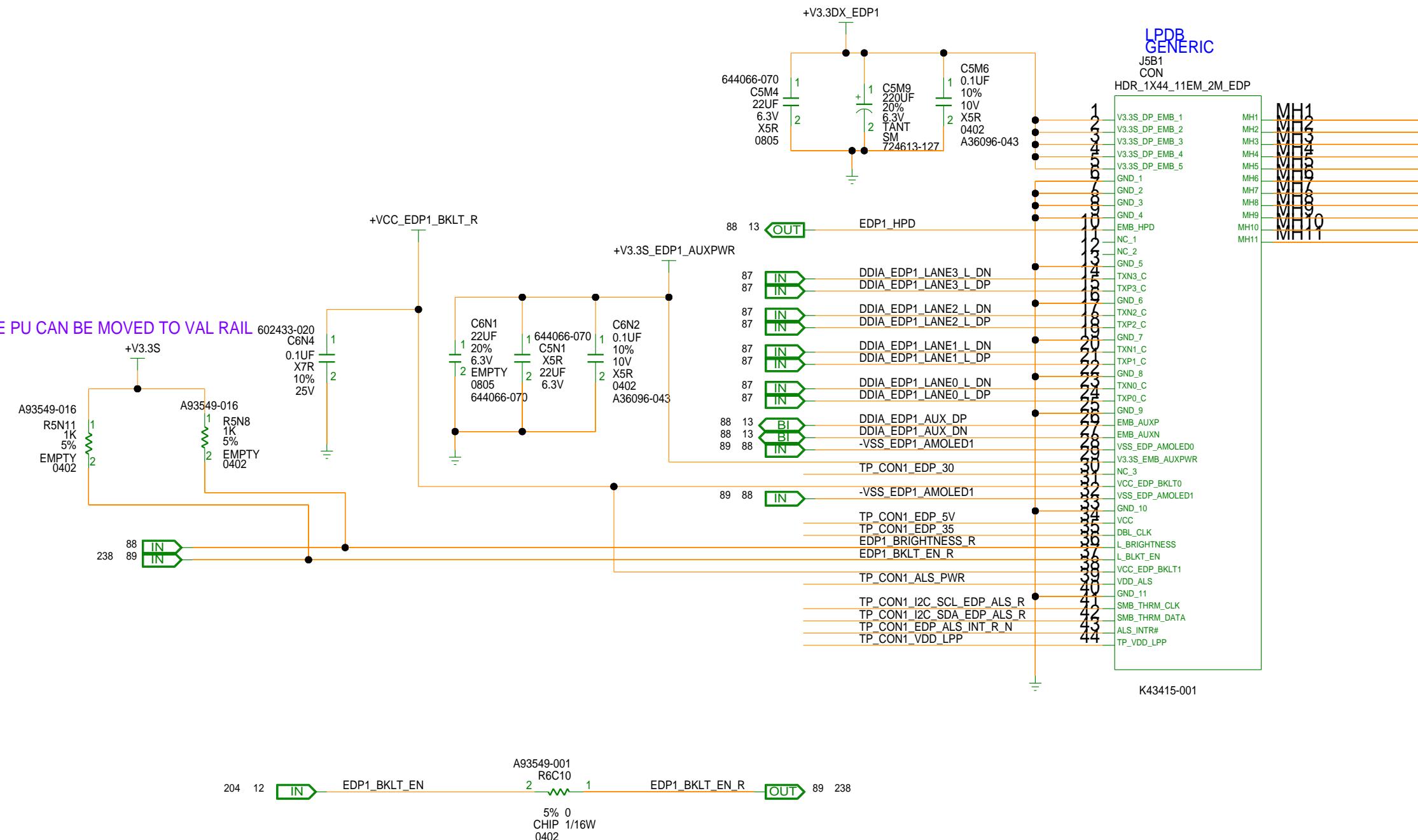
MODULE REV DETAILS

MODULE NAME	REV	DATE

EDP CONNECTOR 1

CHANGE TANT CAP TO LOWER VALUE

THESE PU CAN BE MOVED TO VAL RAIL



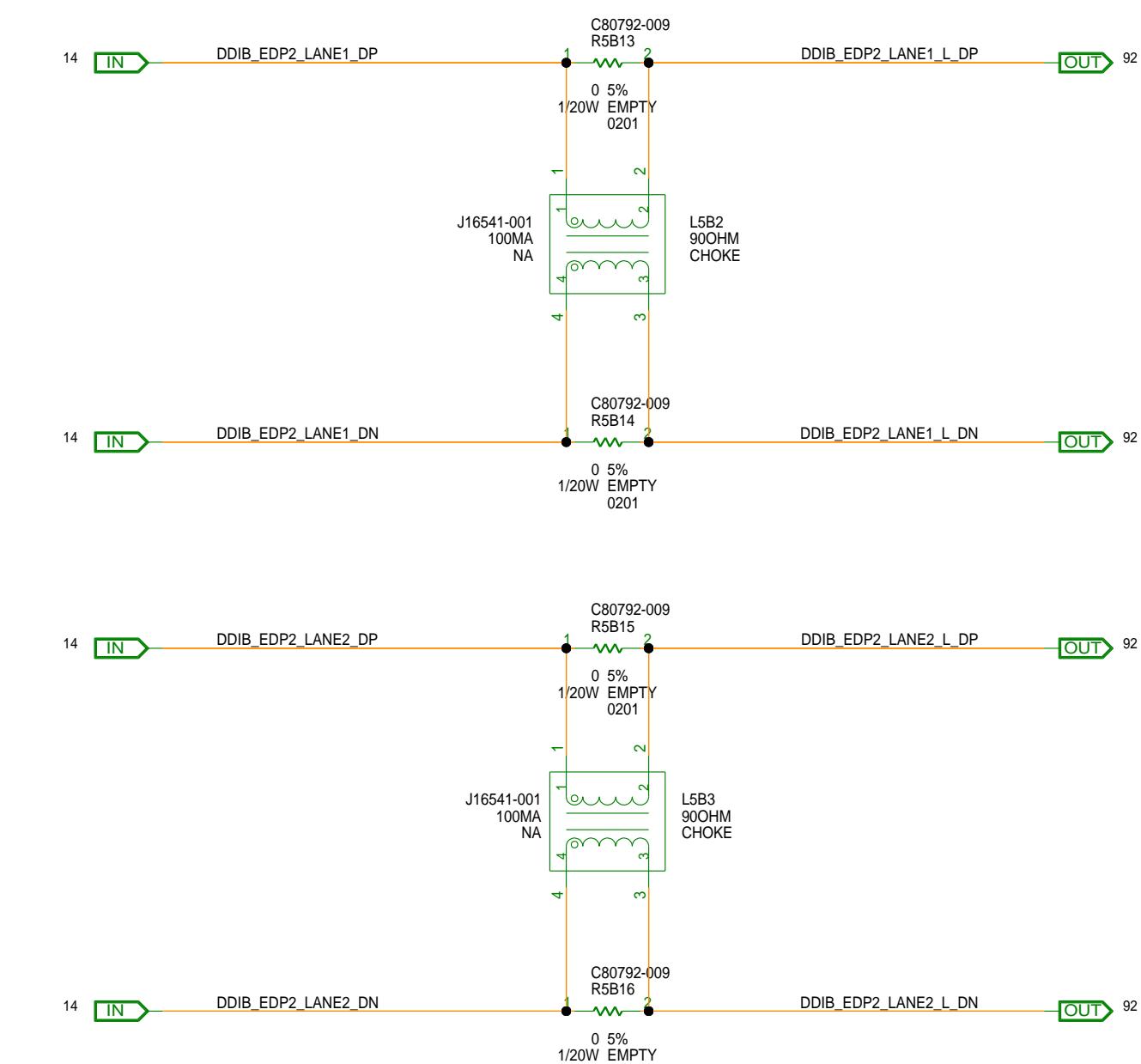
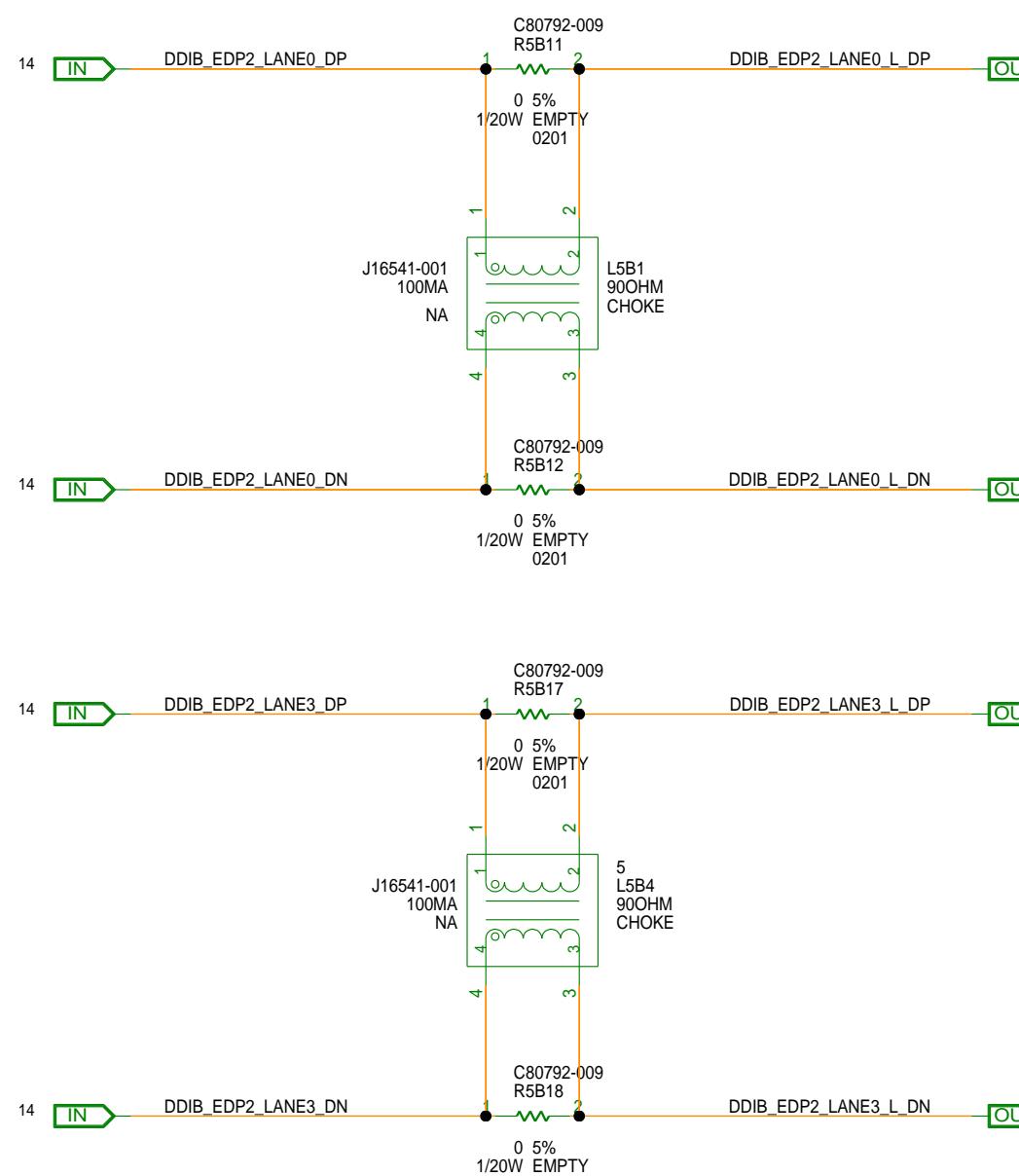
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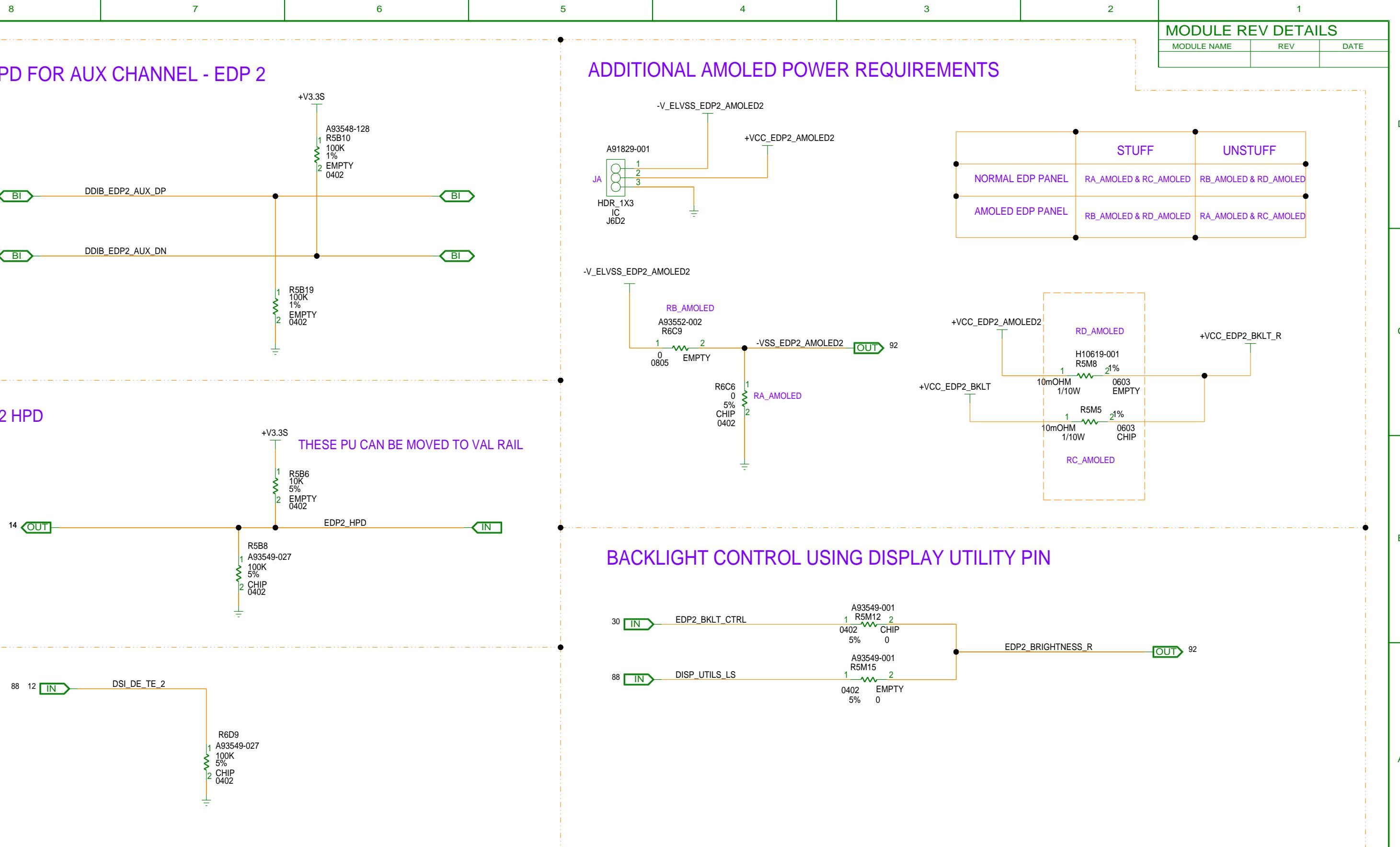
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MODULE NAME				REV	DATE		

EDP CONNECTOR 2 - CMC





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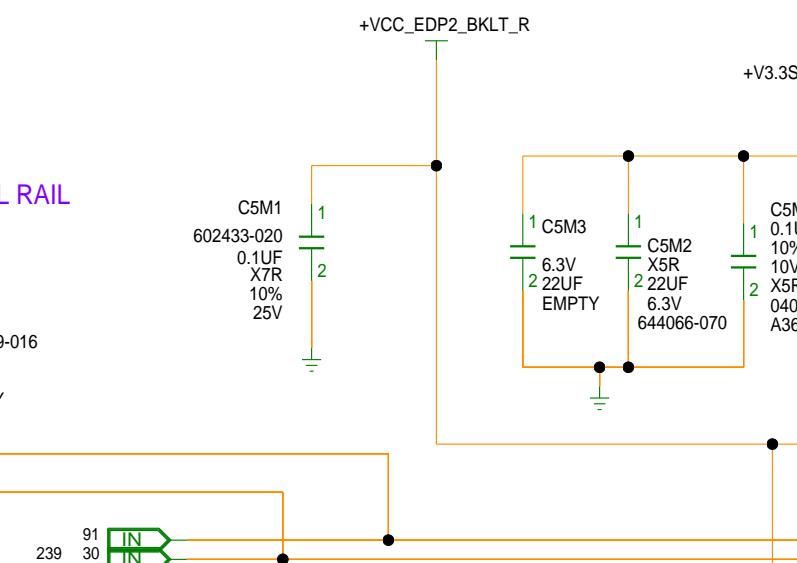
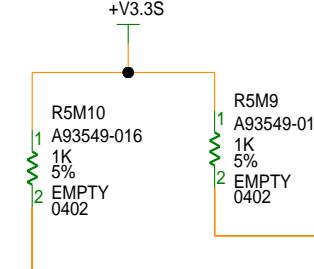
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MODULE REV DETAILS

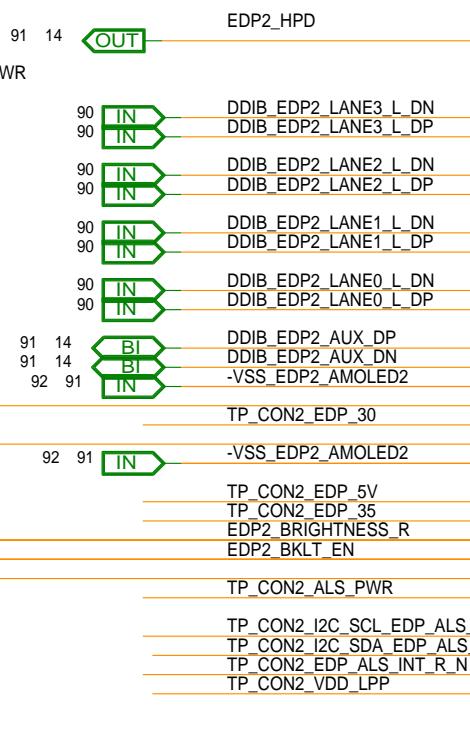
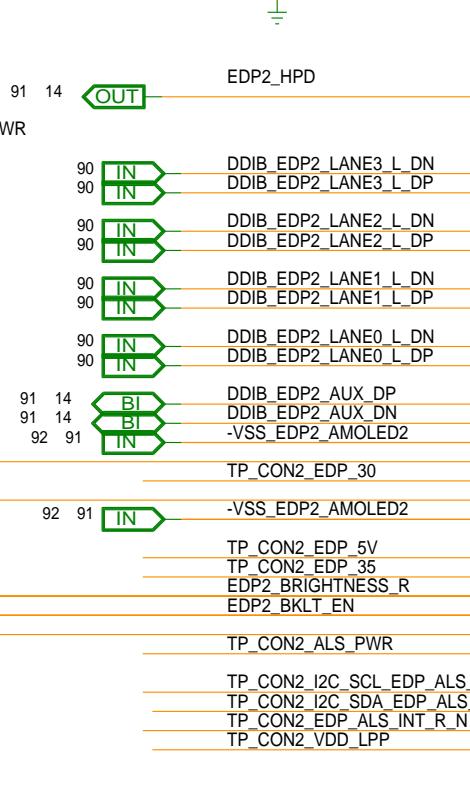
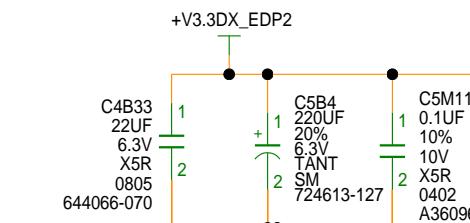
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EDP CONNECTOR 2

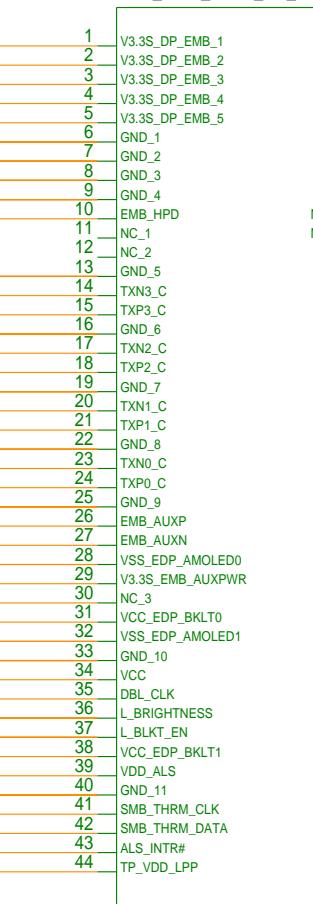
THESE PU CAN BE MOVED TO VAL RAIL



CHANGE TANT CAP TO LOWER VALUE



LPDB GENERIC

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MODULE REV DETAILS

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Tue Oct 15 12:49:48 2019

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MODULE REV DETAILS		
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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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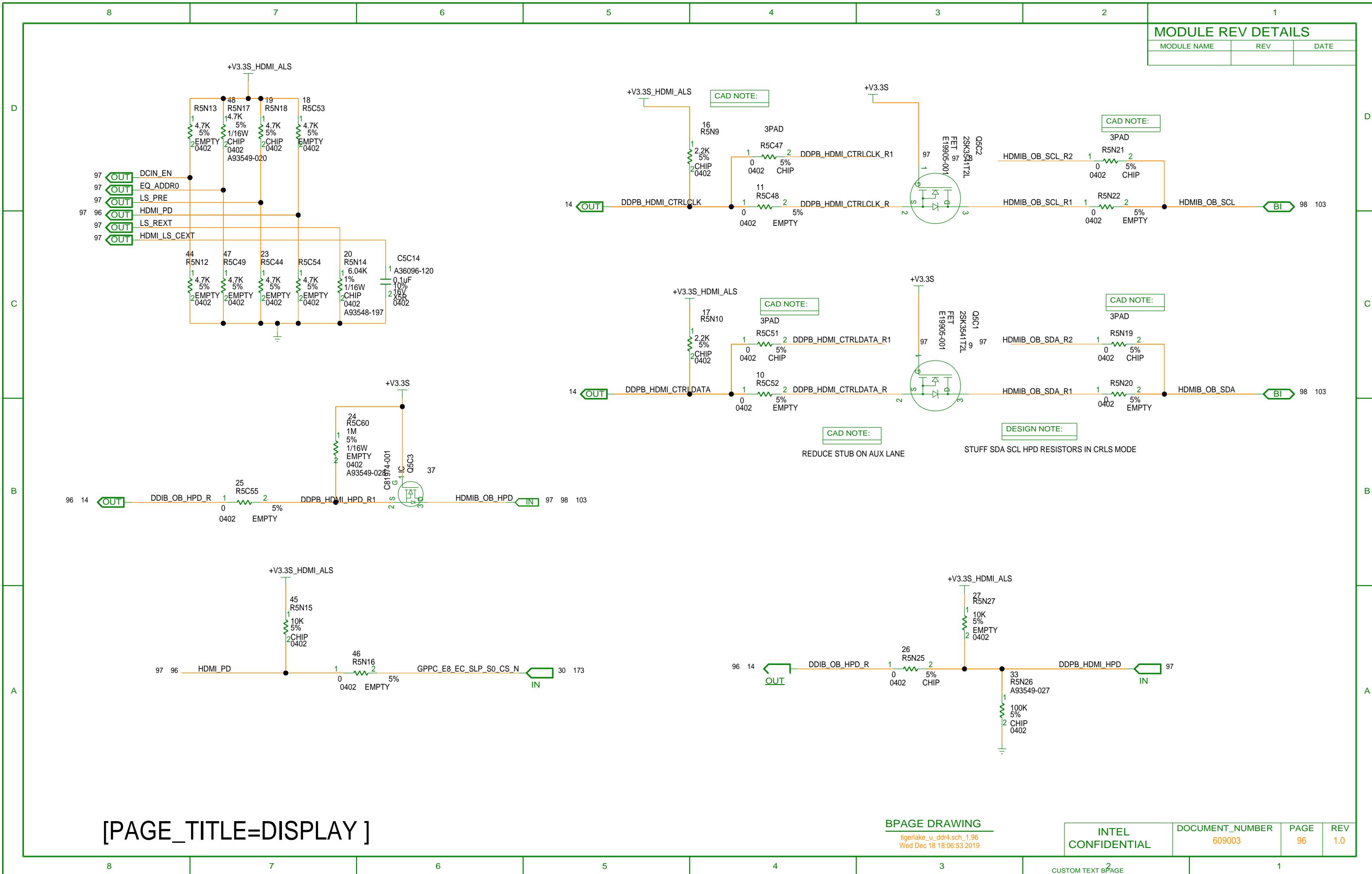
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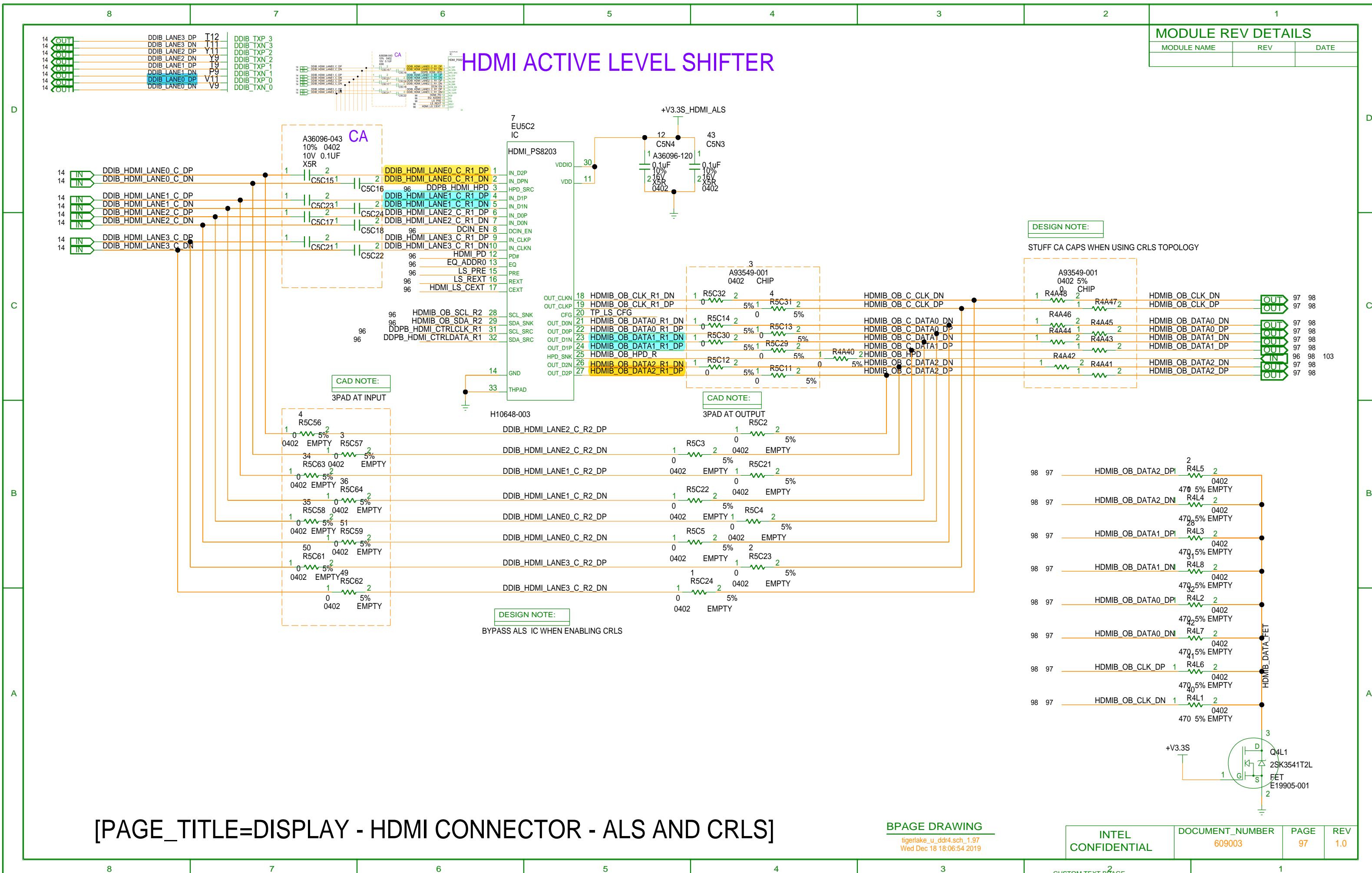
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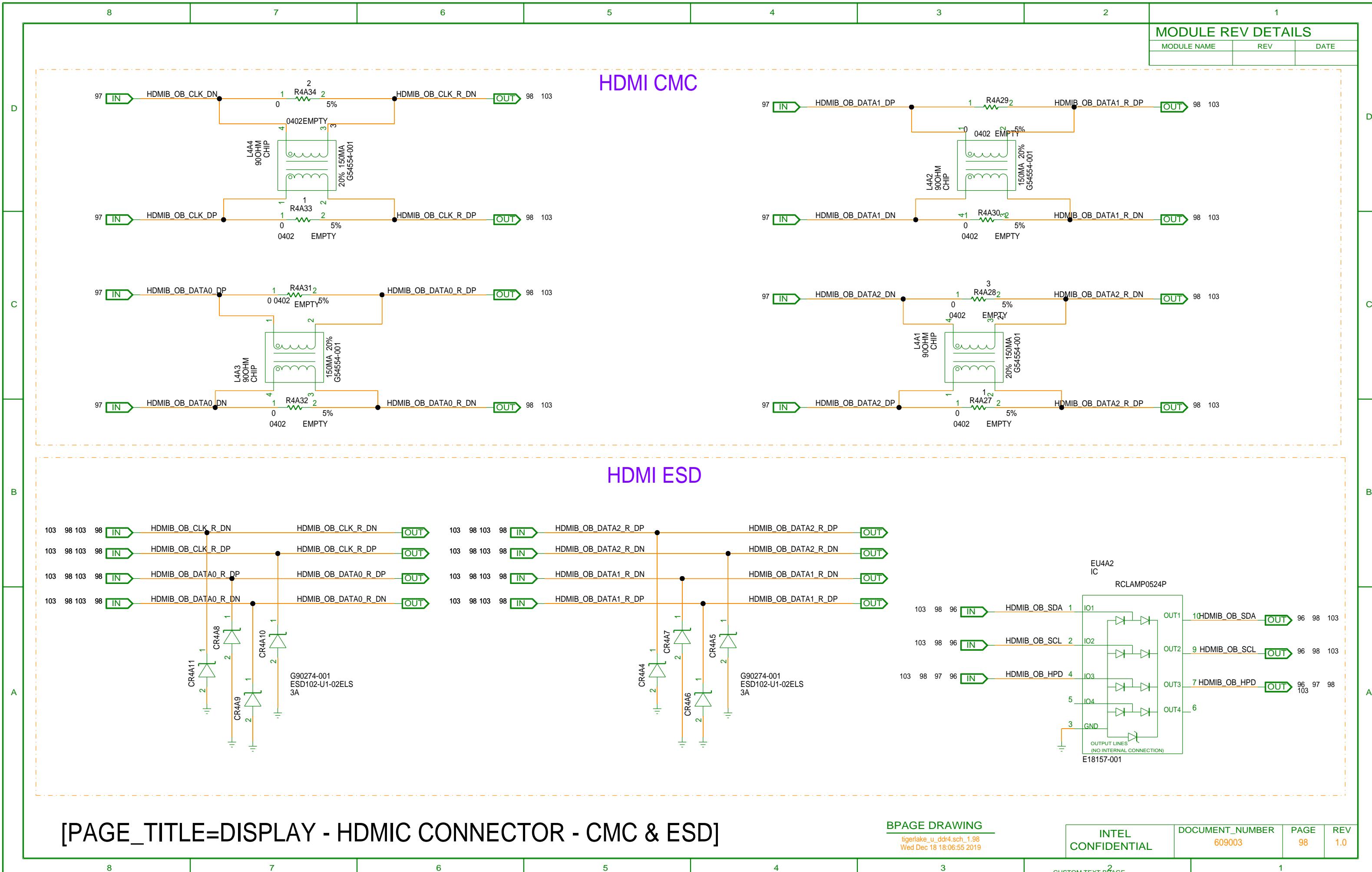
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MODULE REV DETAILS		
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DP CONNECTOR 2 - CMC

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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 99	REV 1.0
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CUSTOM TEXT 2 PAGE

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 101	REV 1.0
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DISPLAY - DDI 1&2 HPD & CONNECTOR

MODULE REV DETAILS

MODULE NAME	REV	DATE

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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 102	REV 1.0
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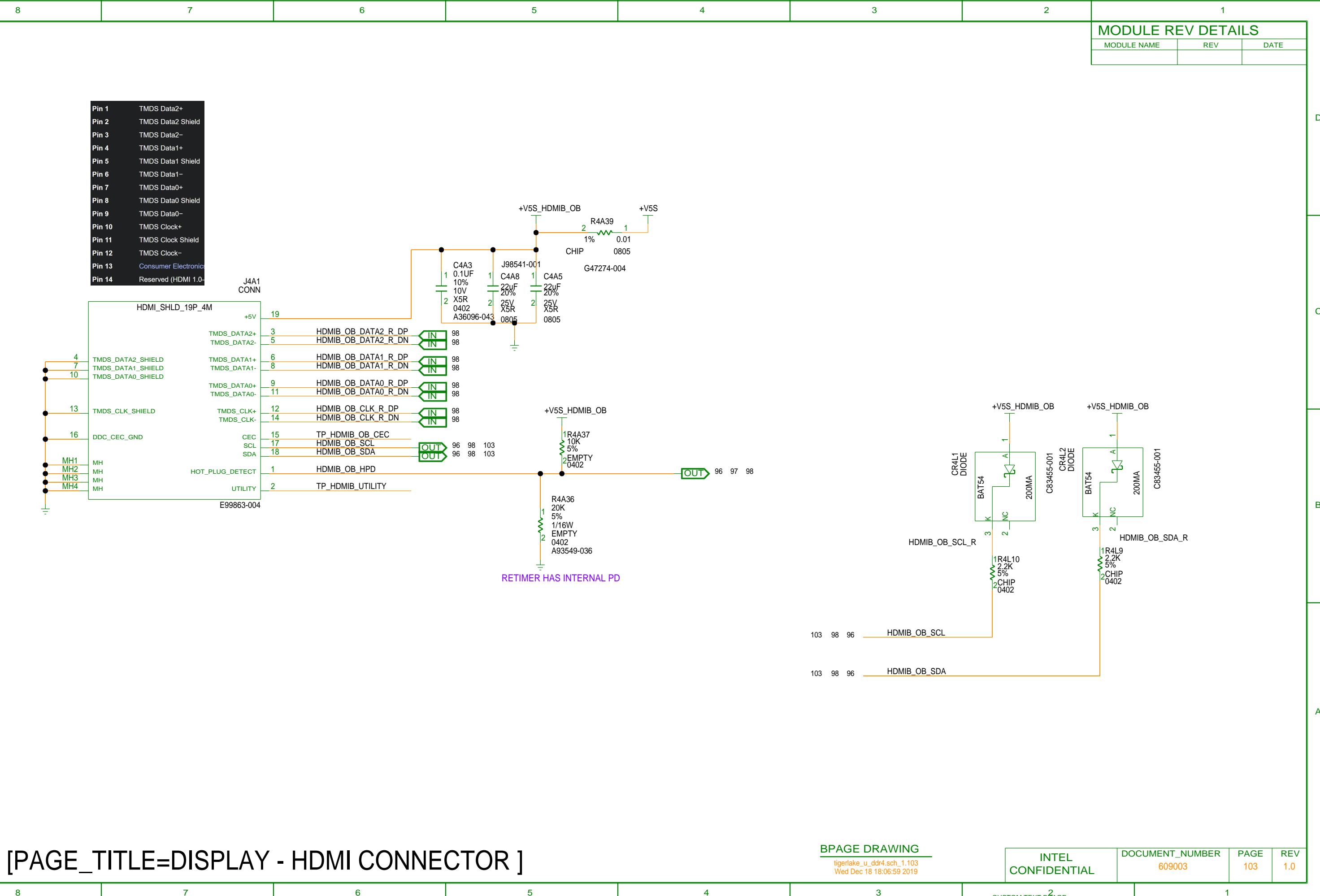
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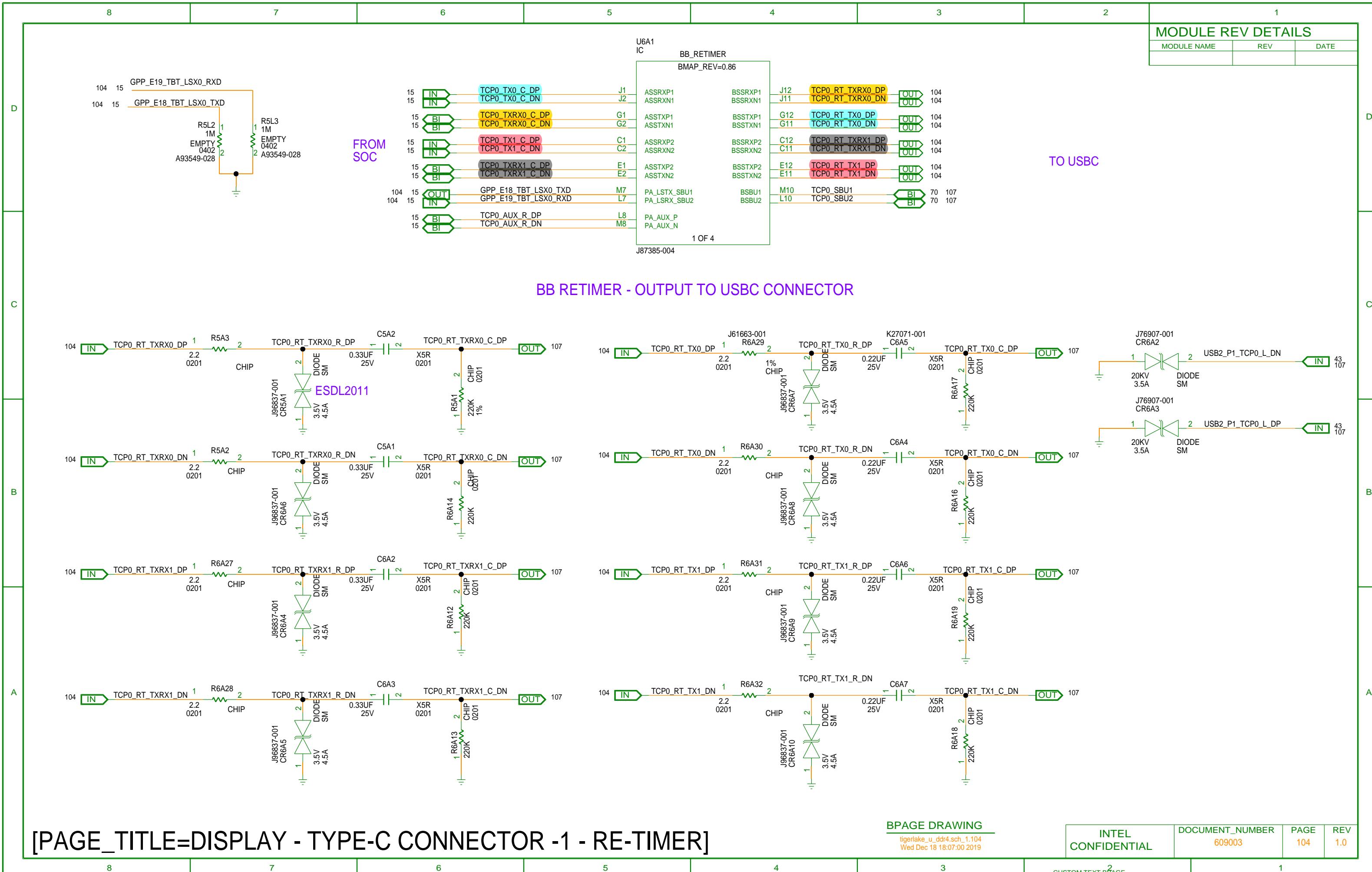
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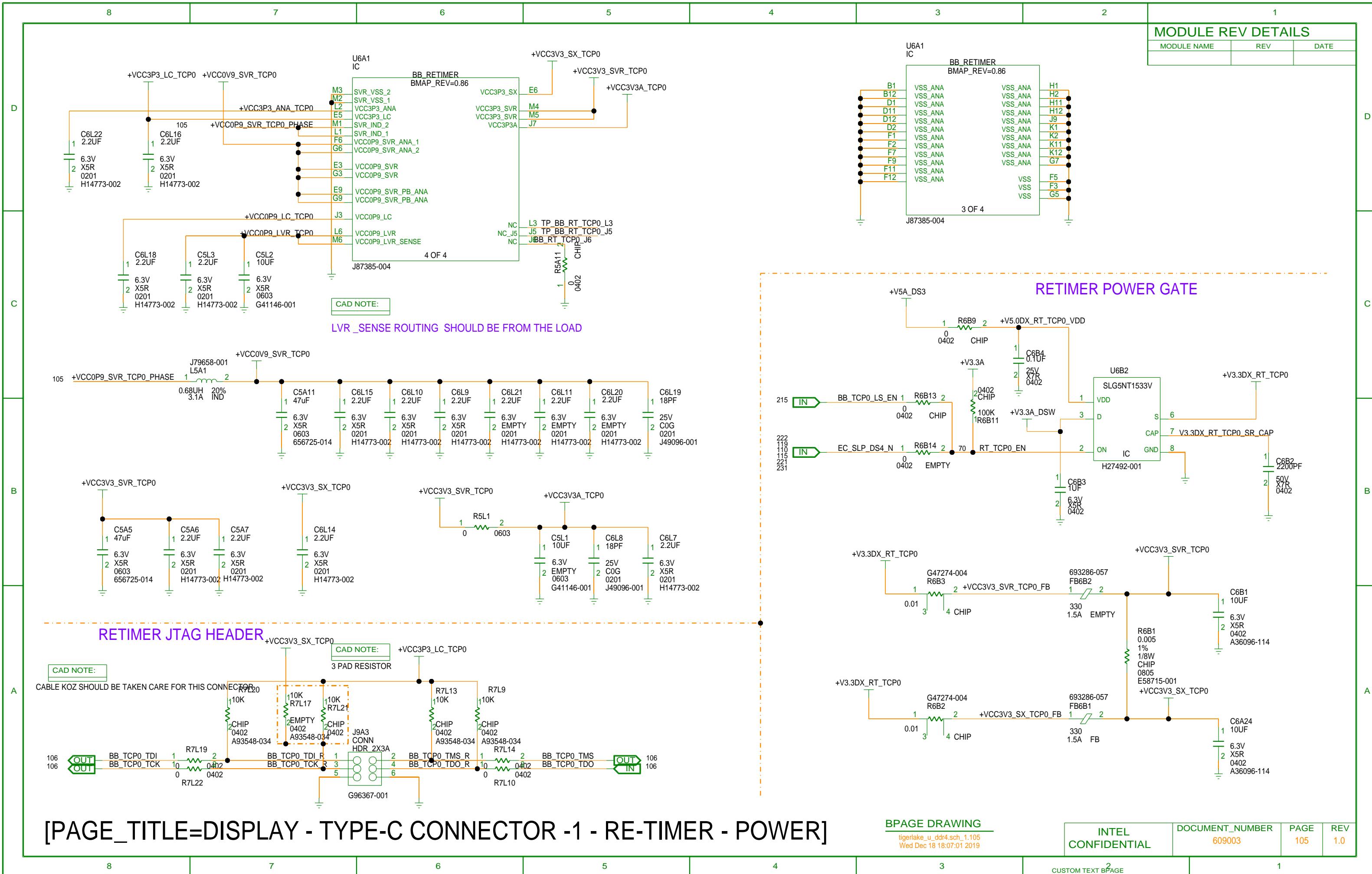
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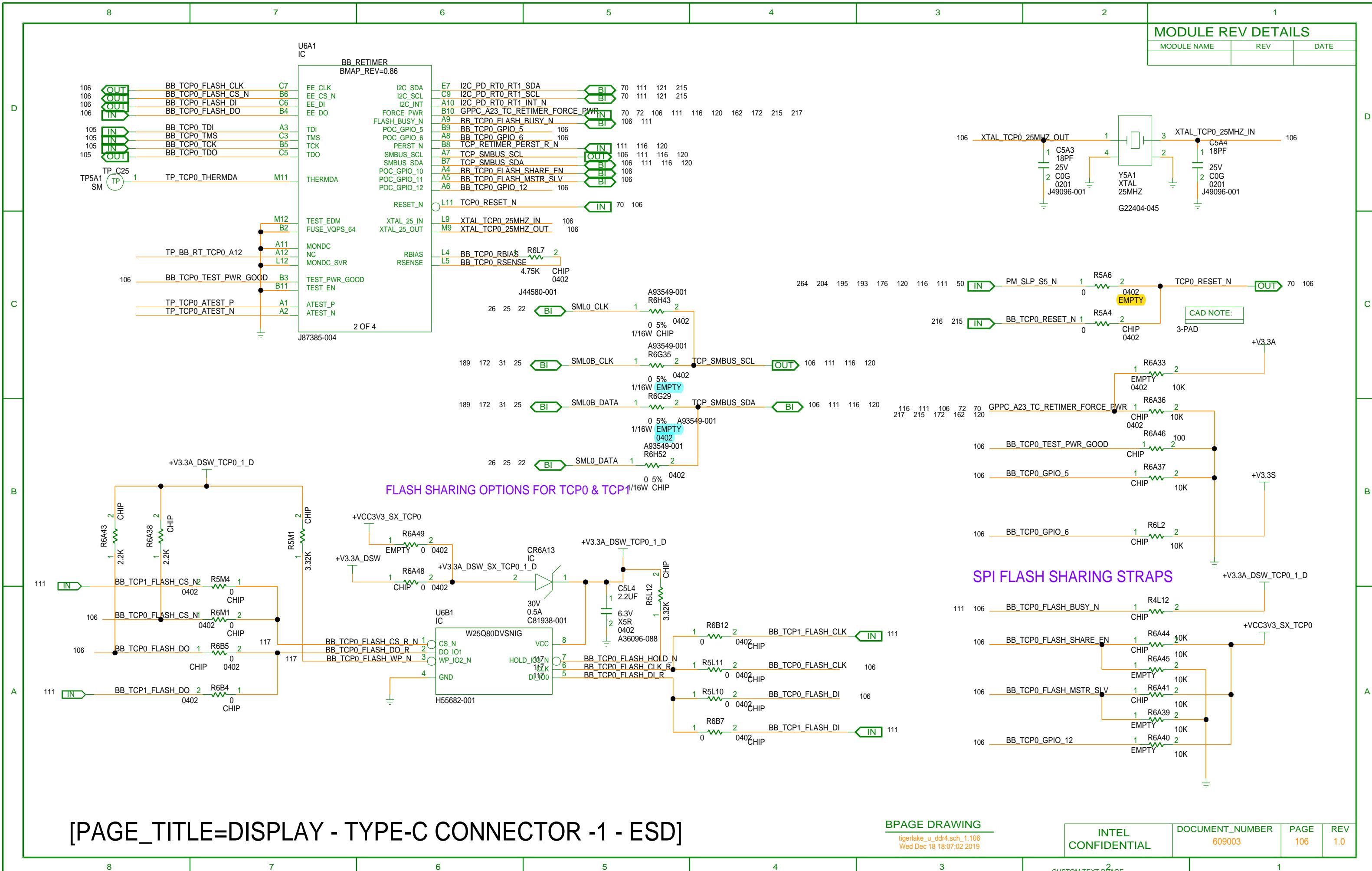
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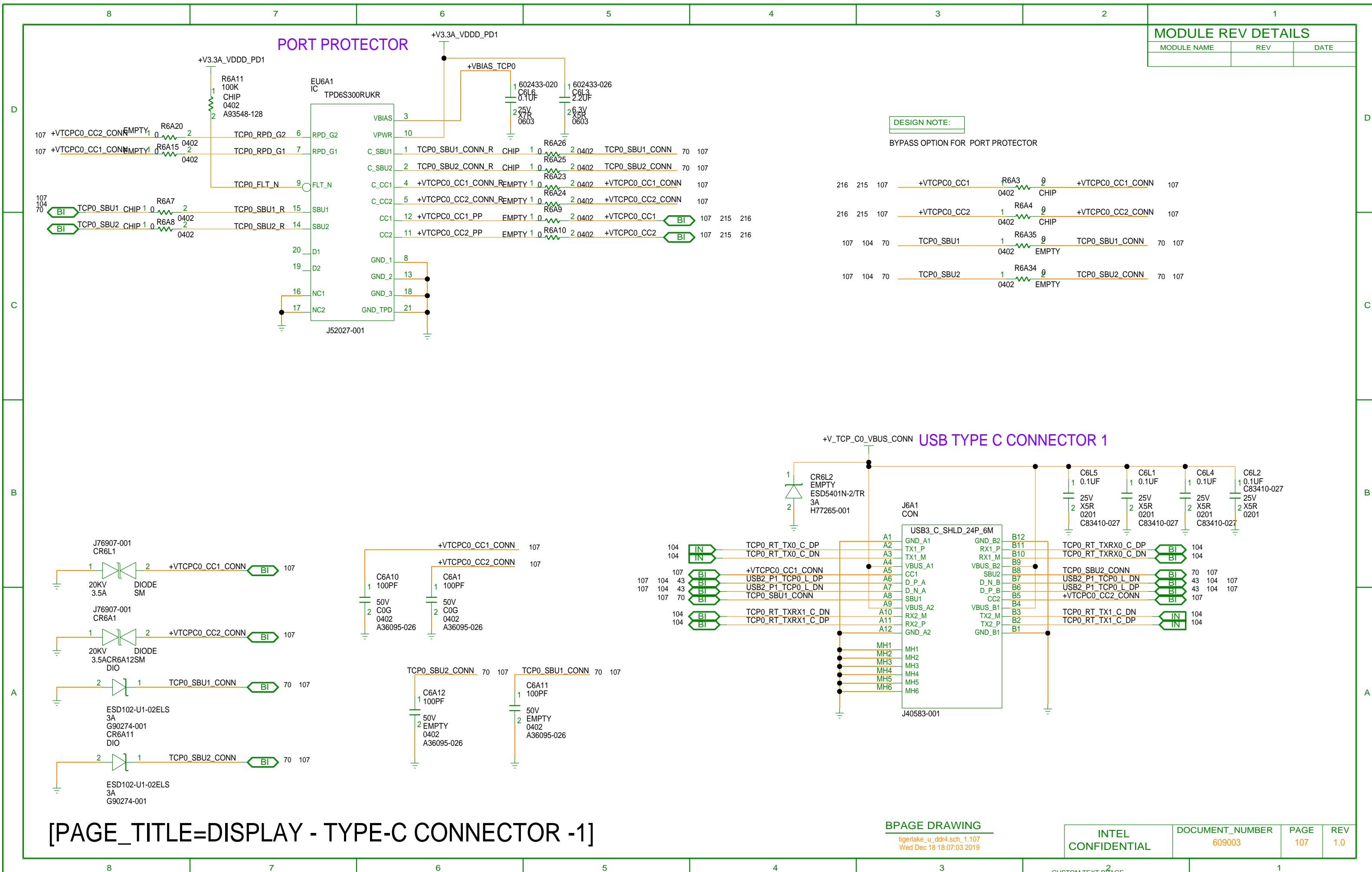
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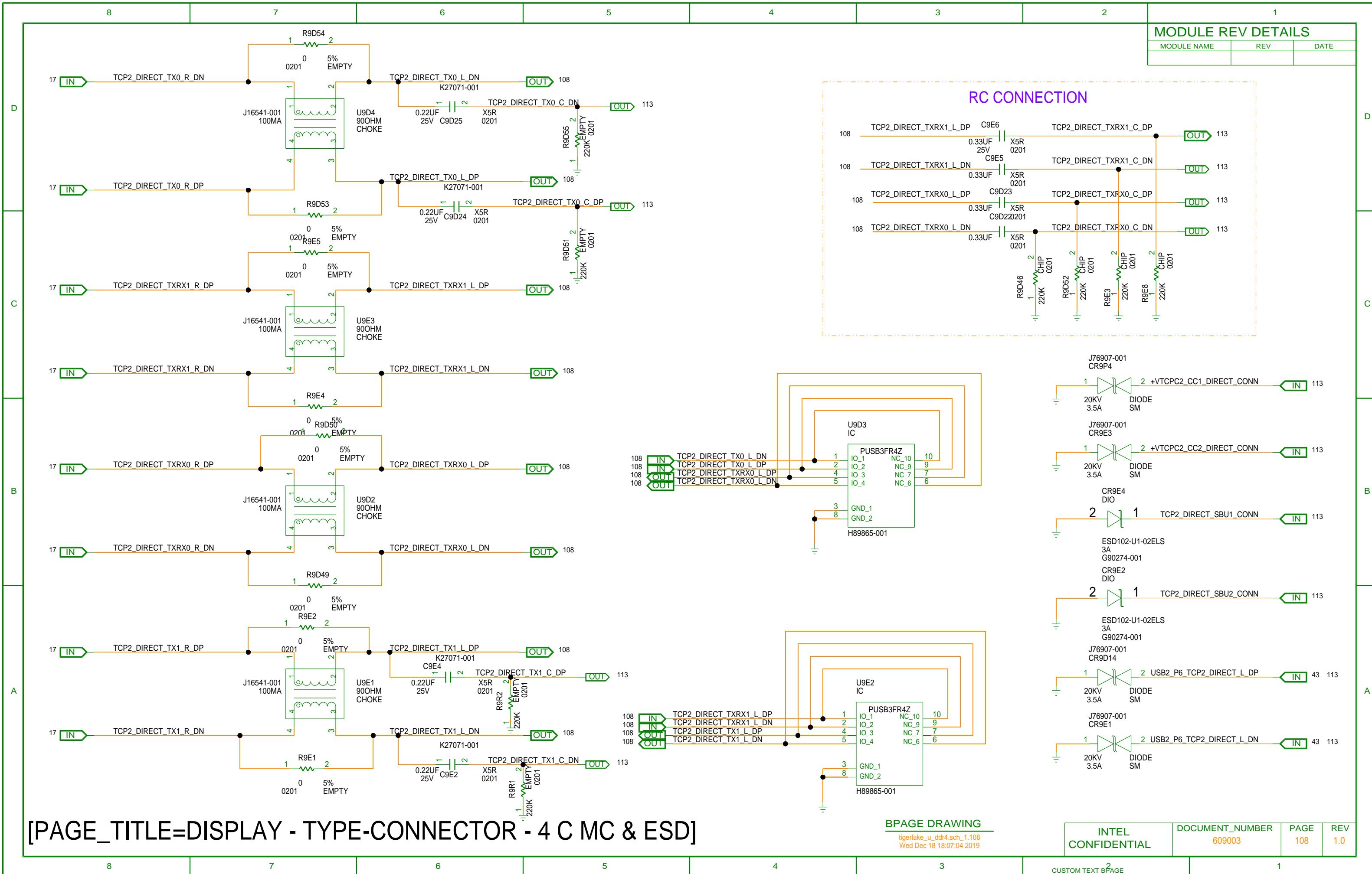


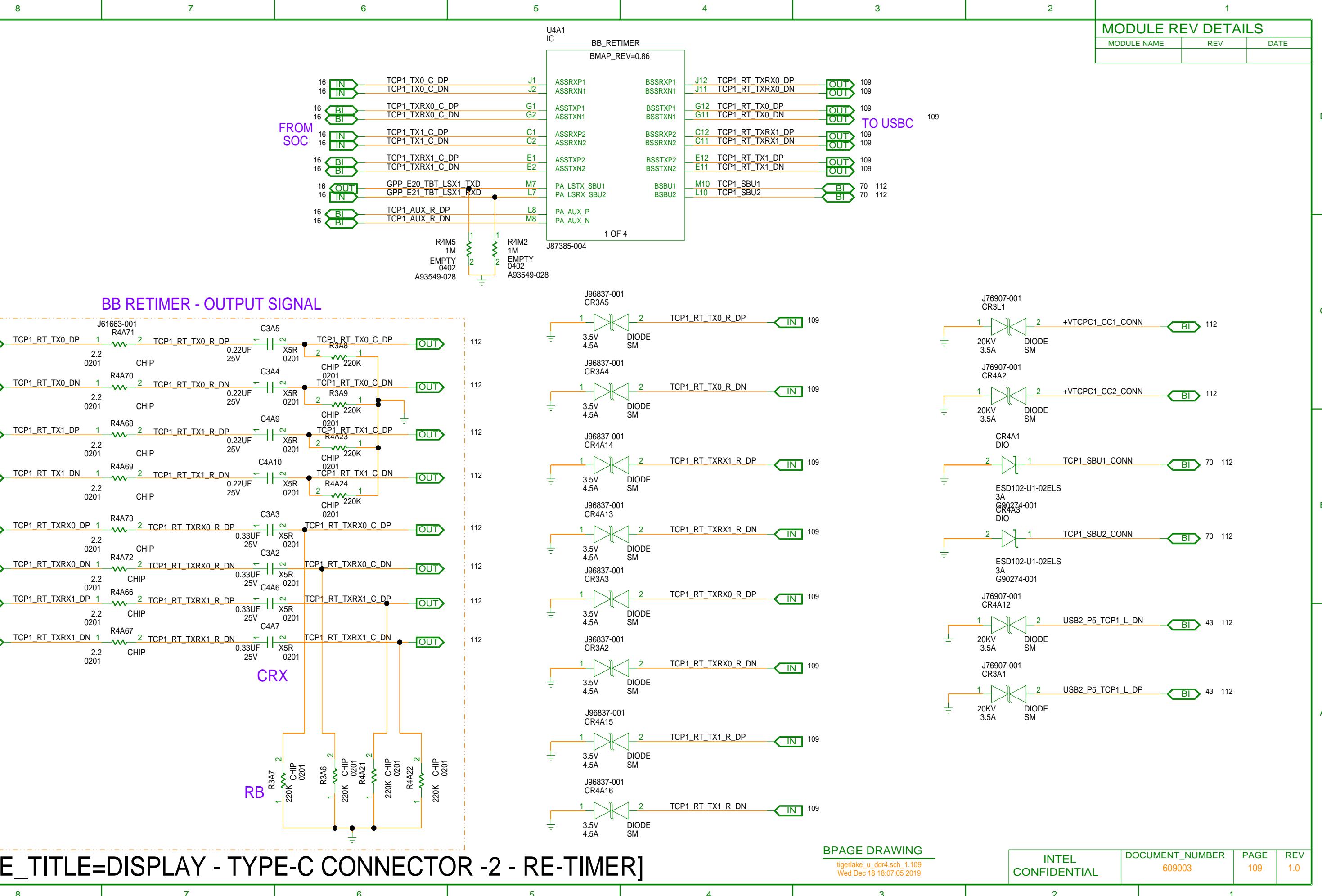


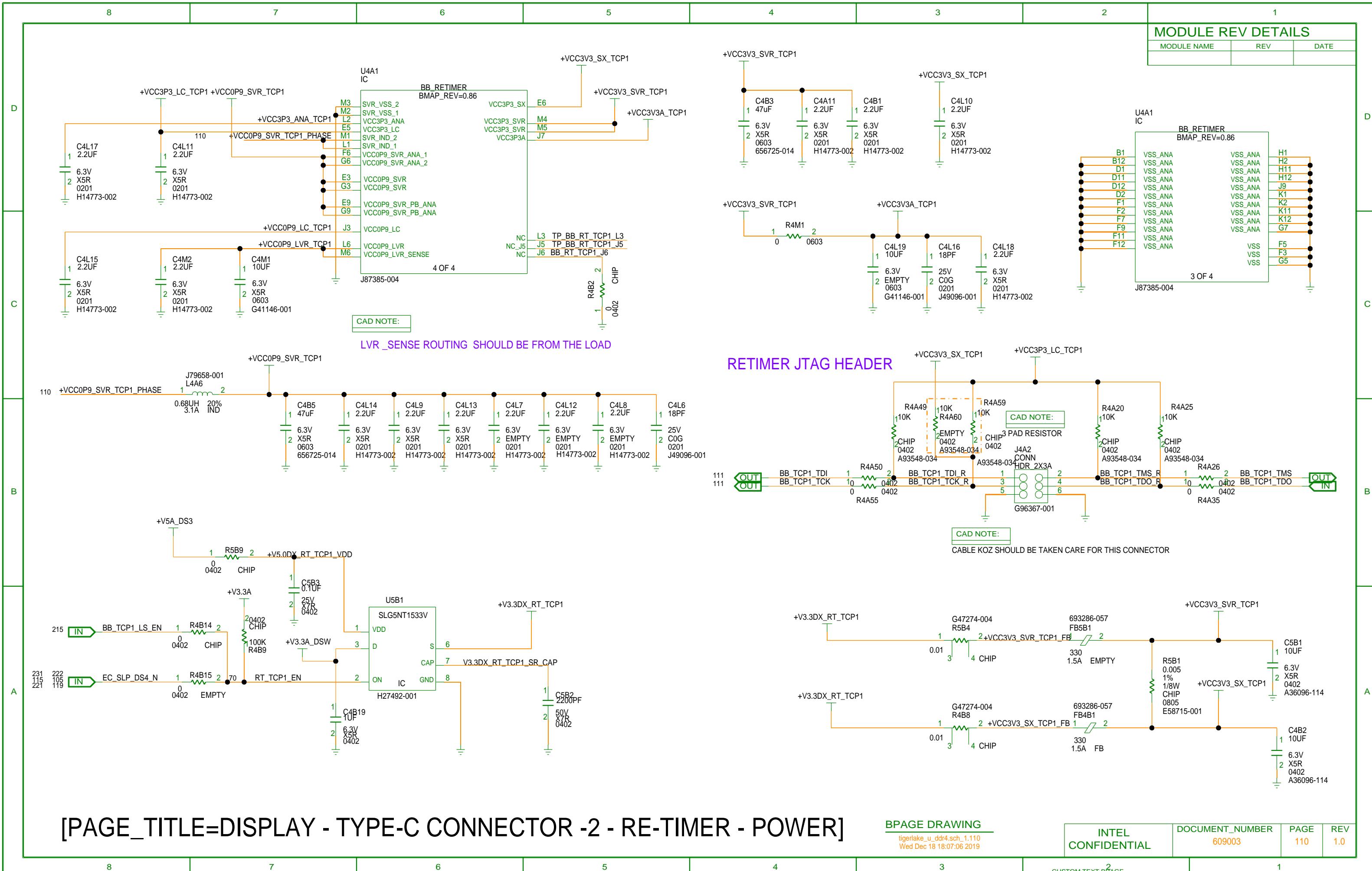


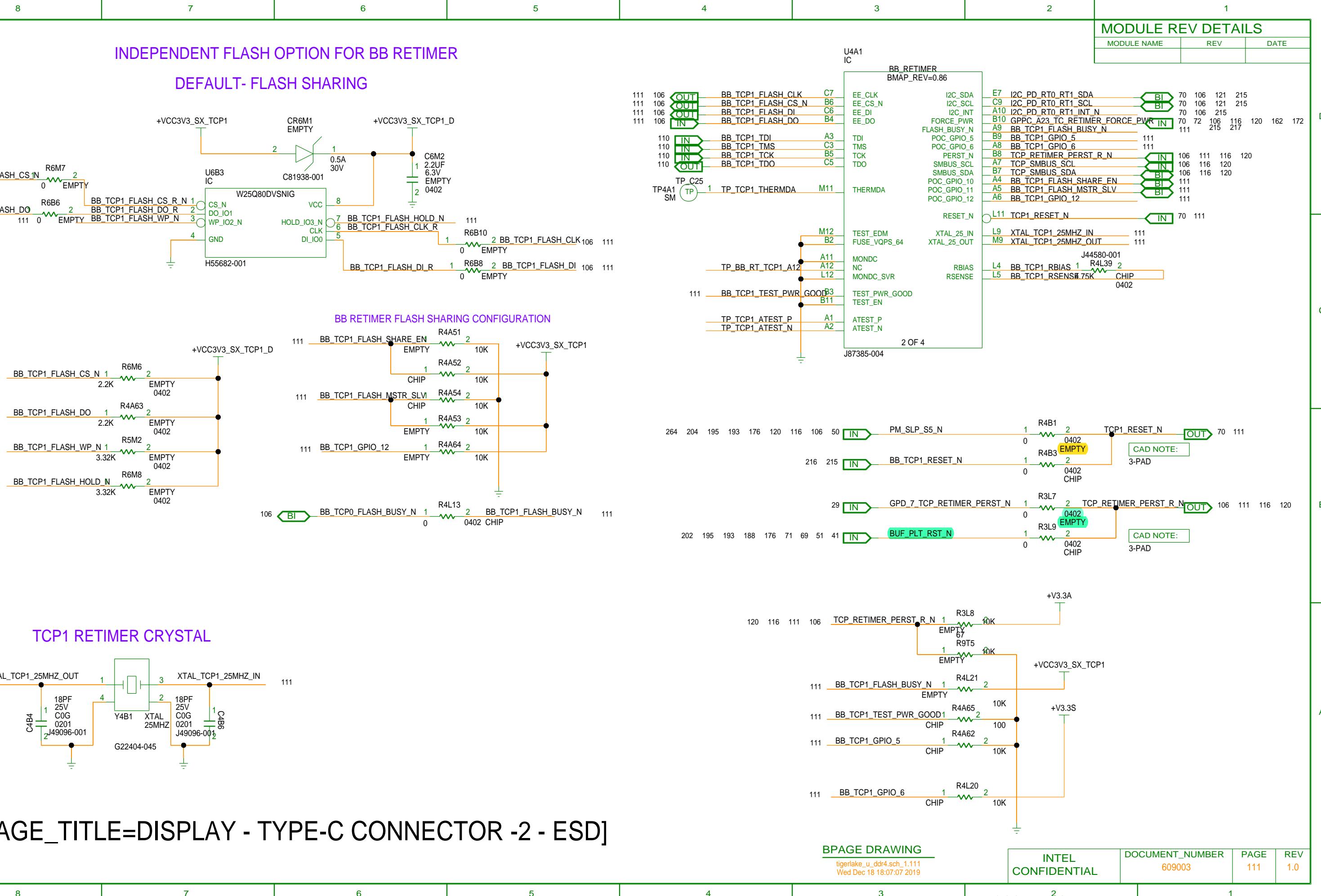


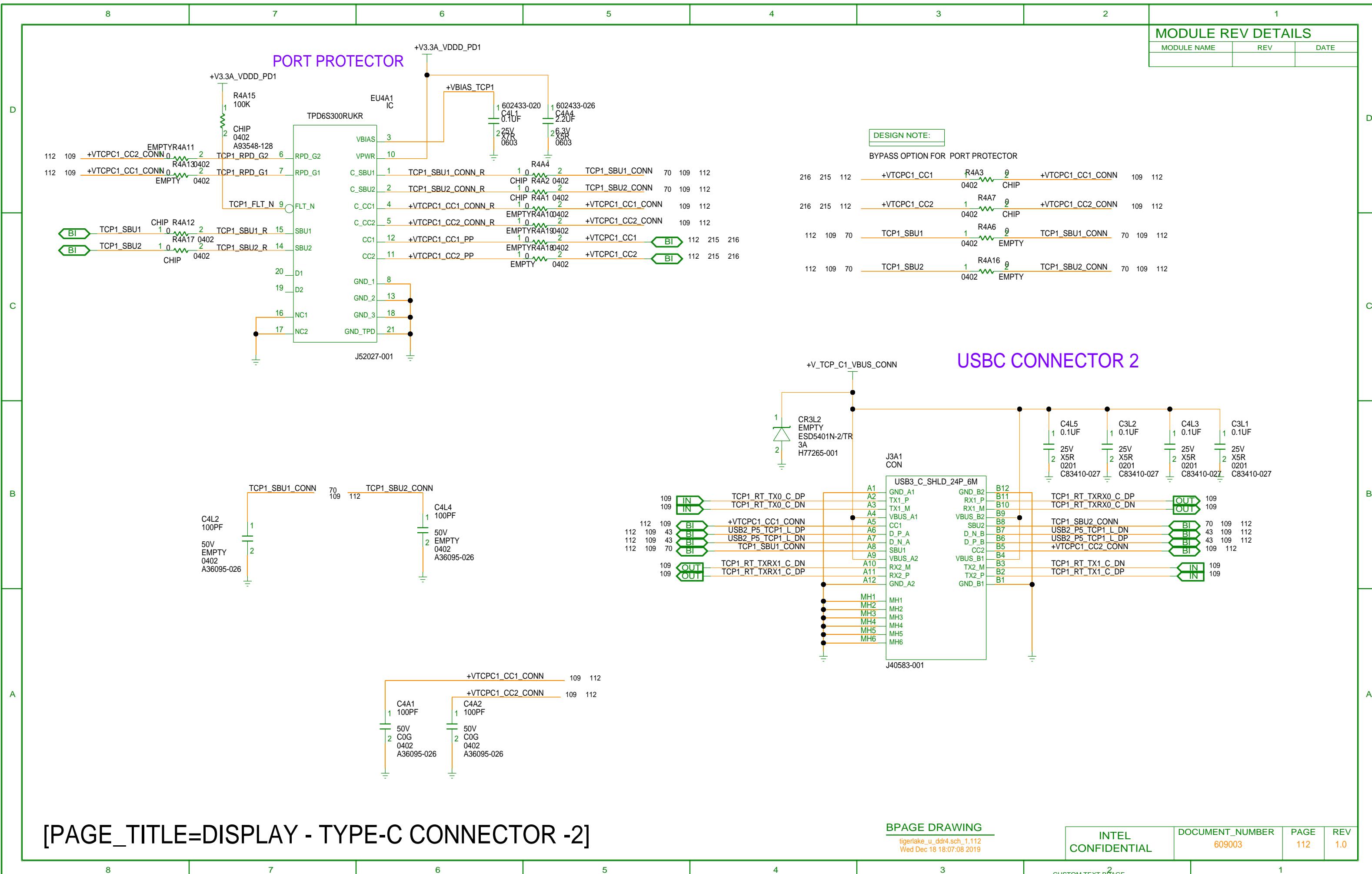


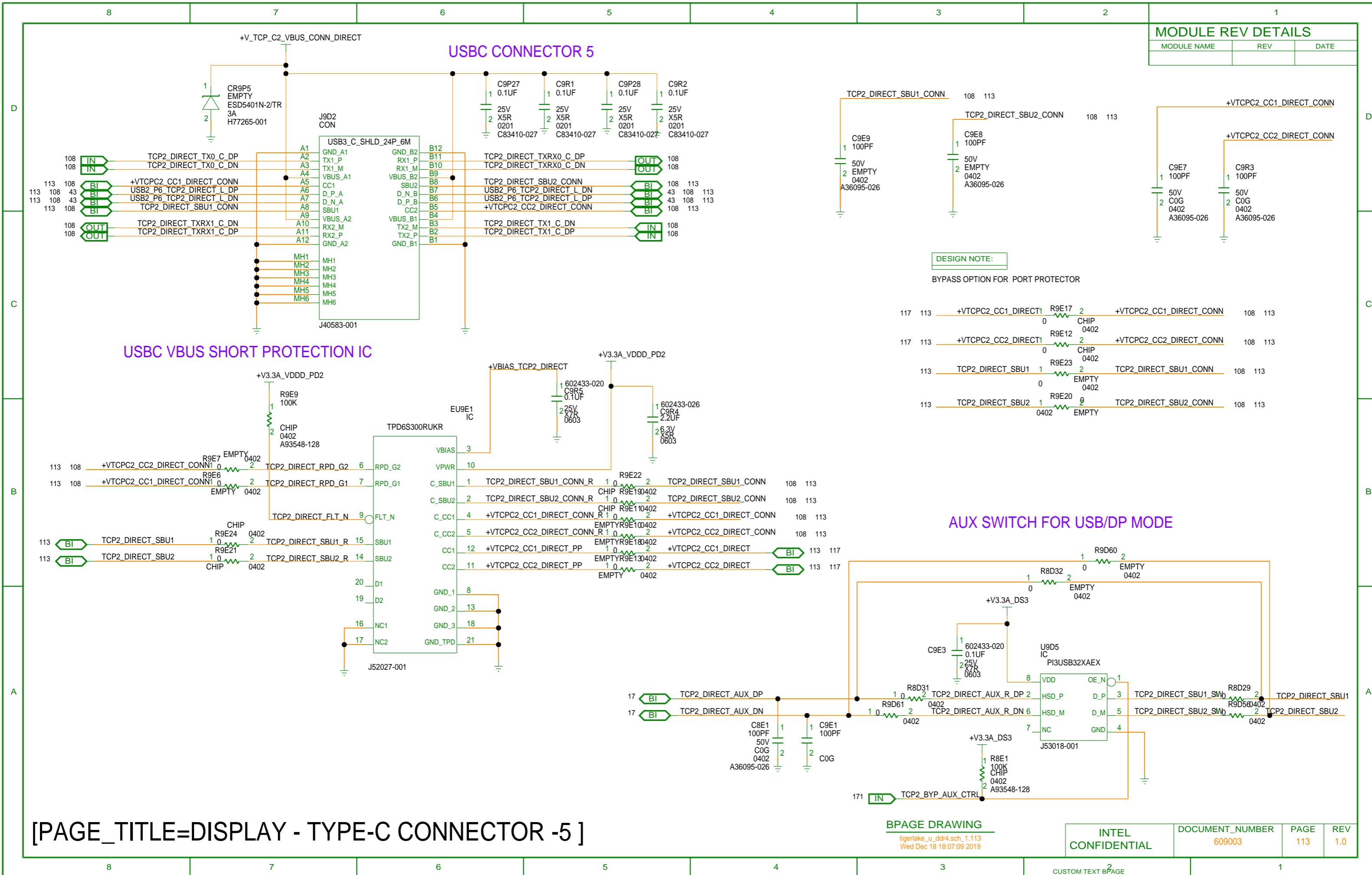


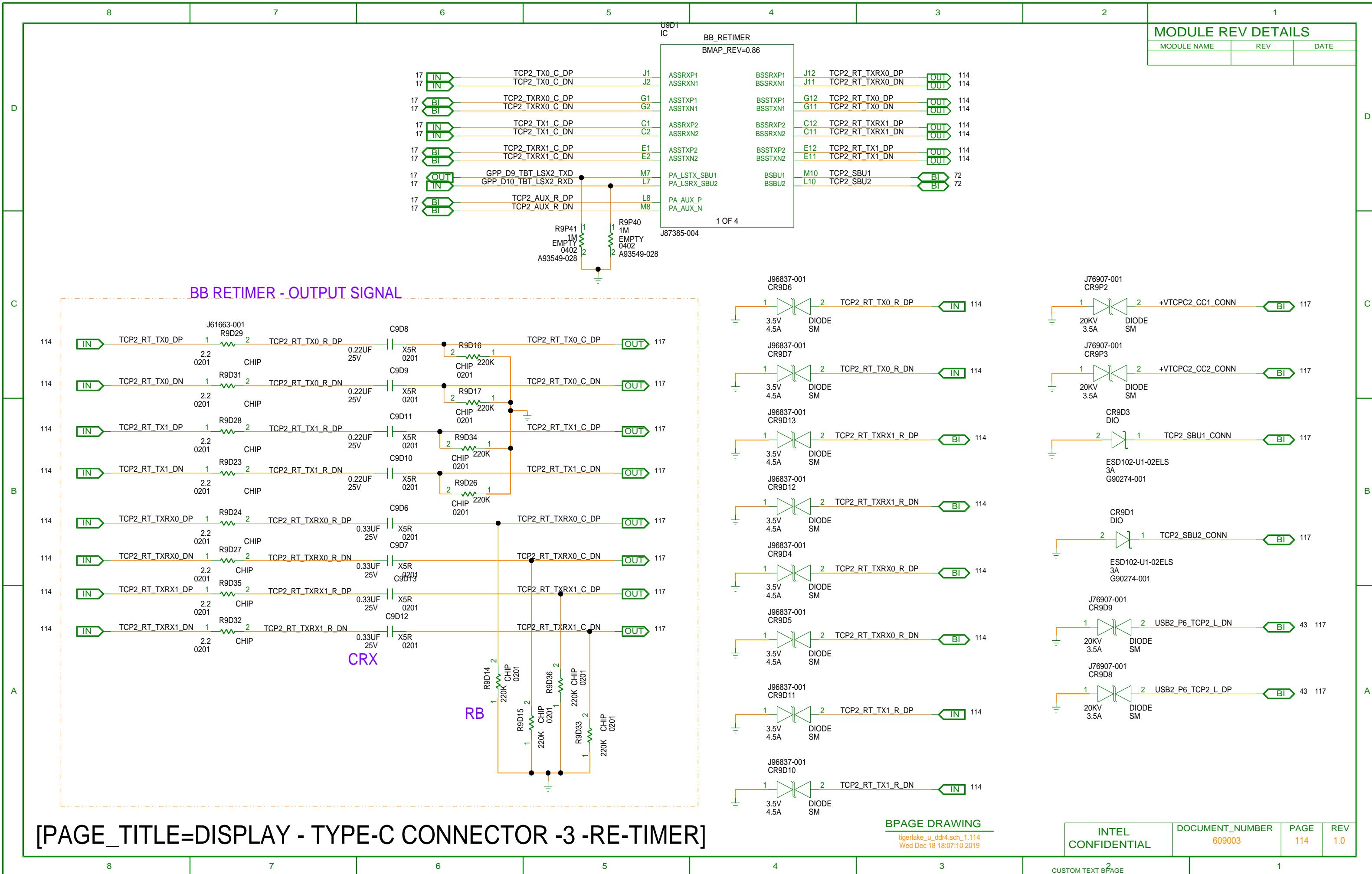


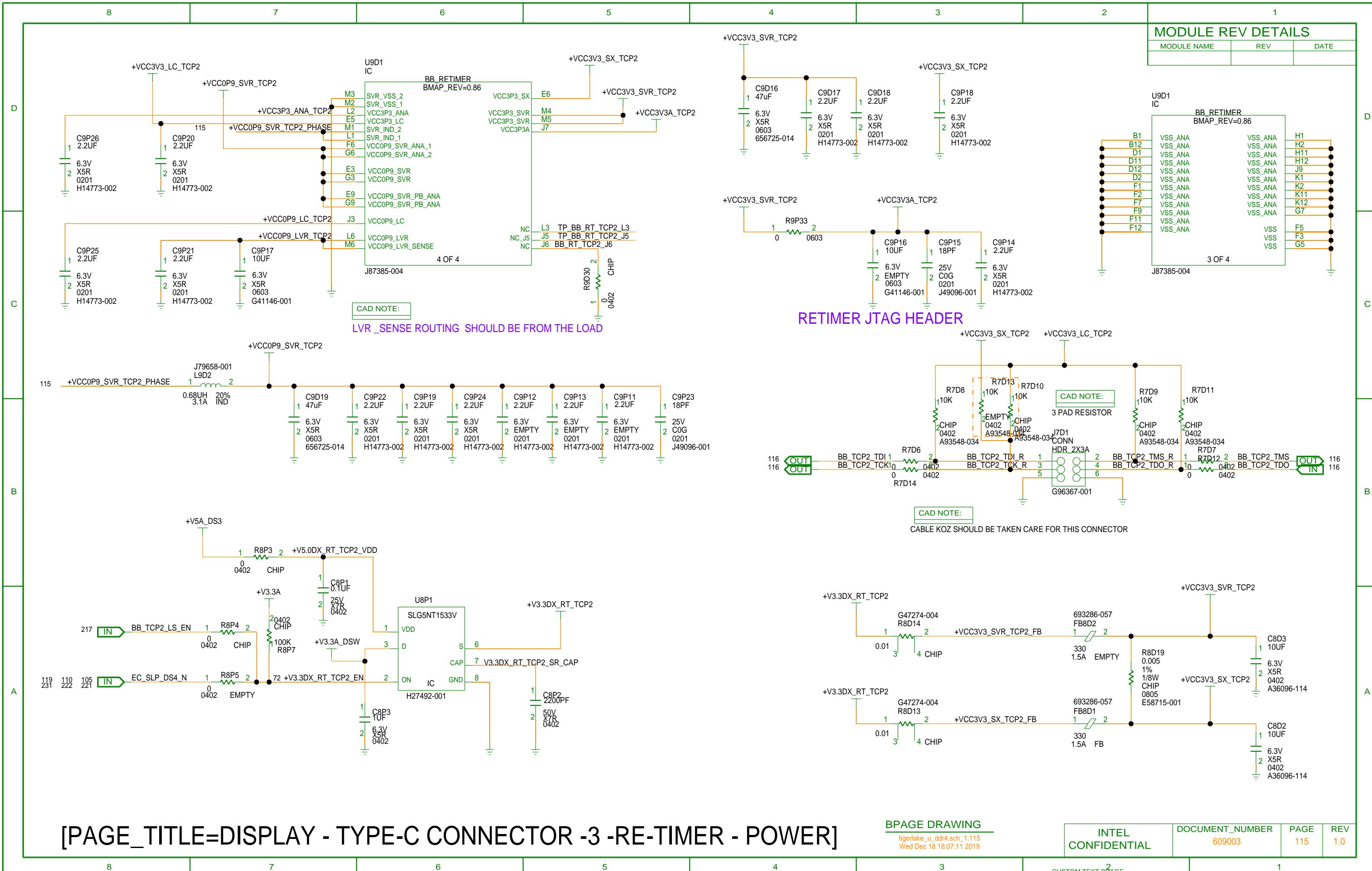


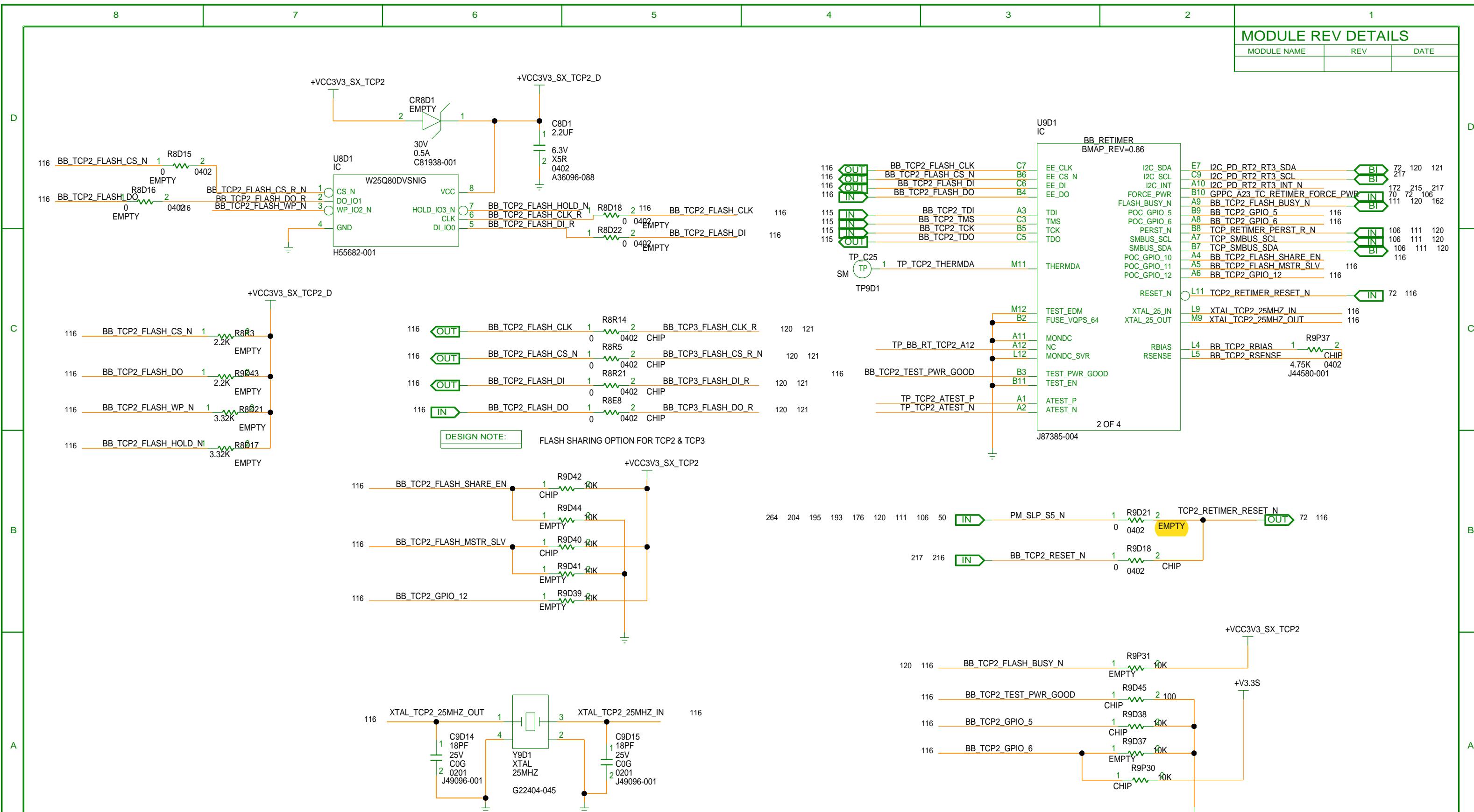










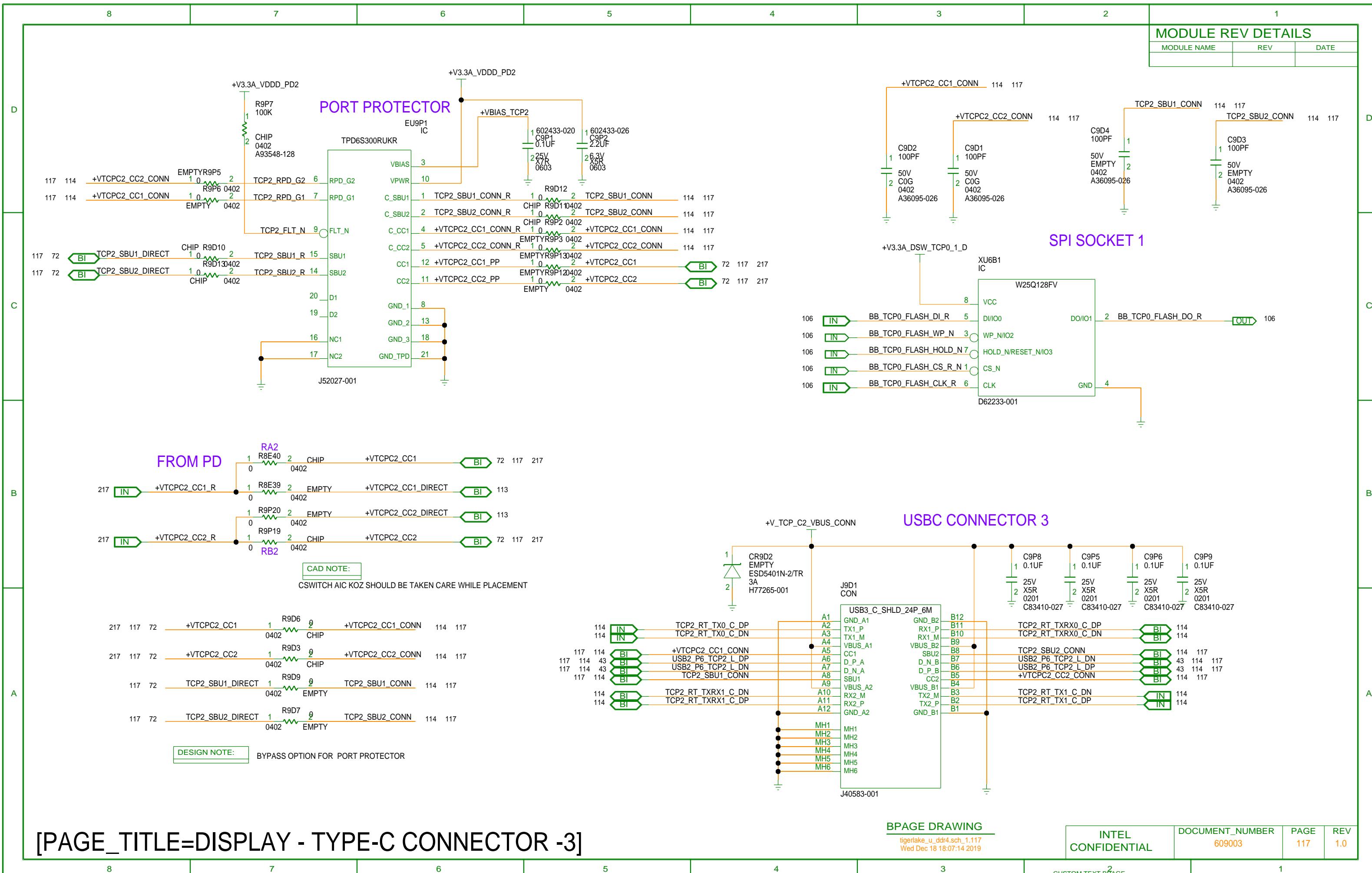


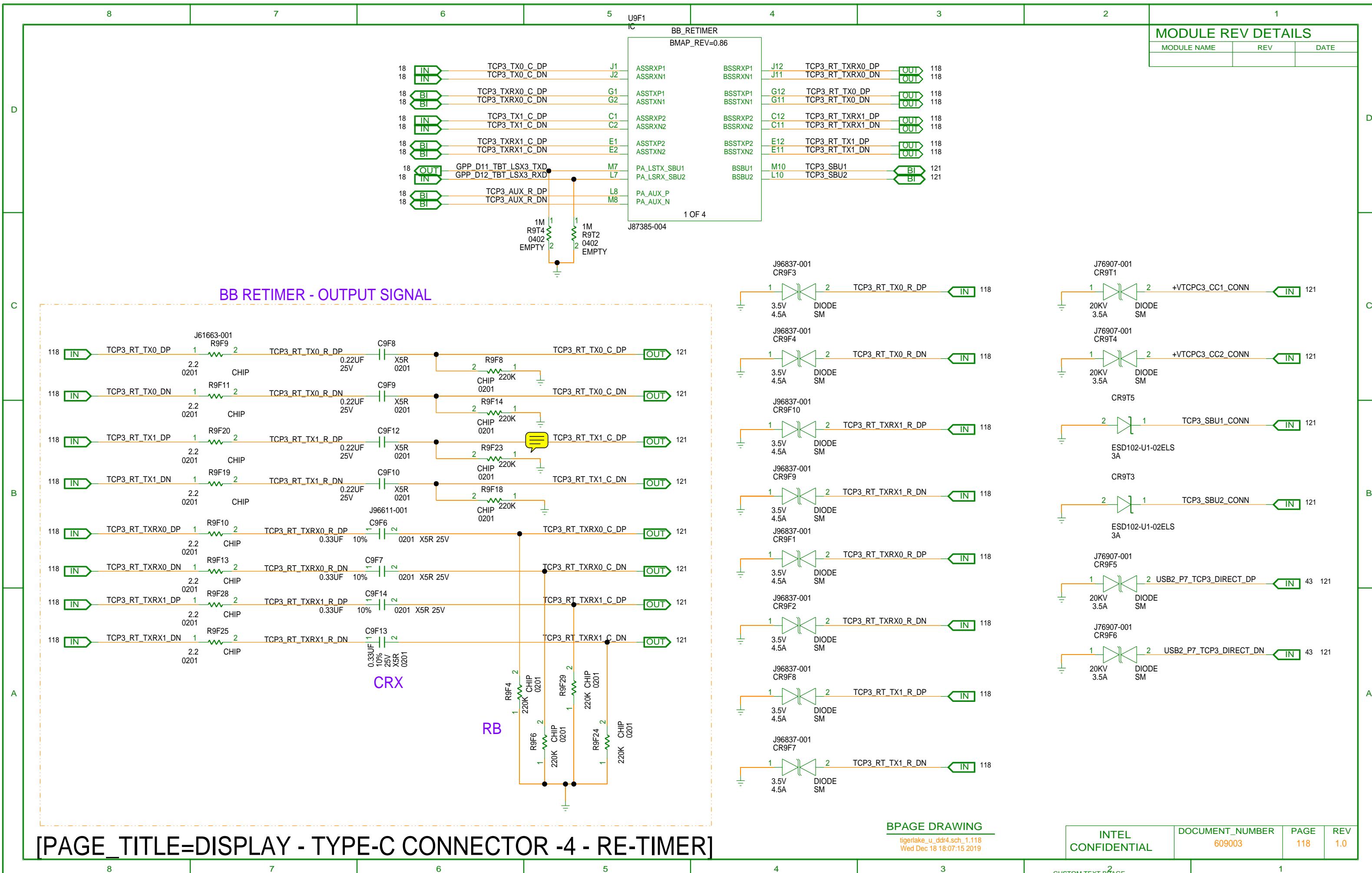
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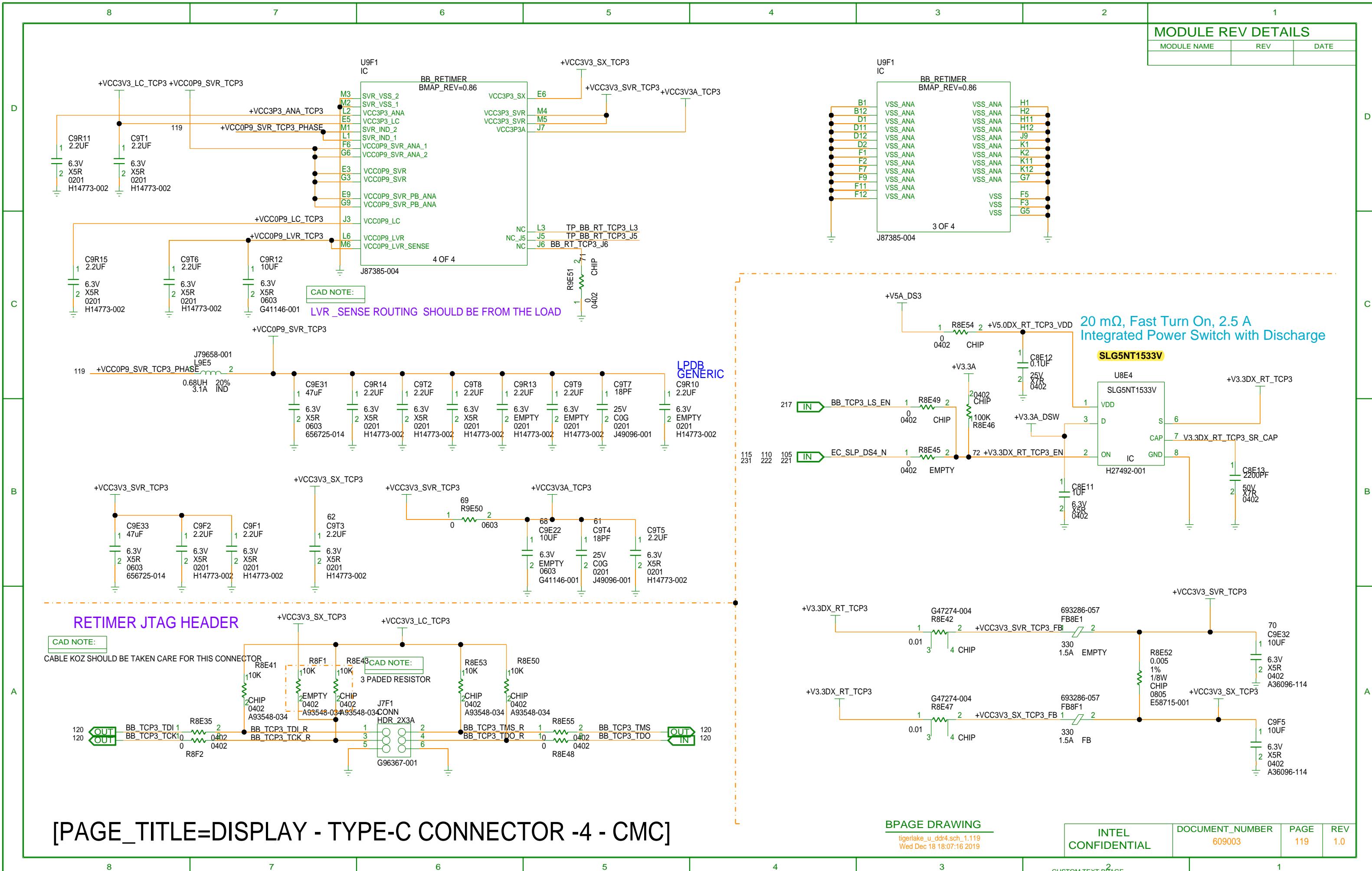
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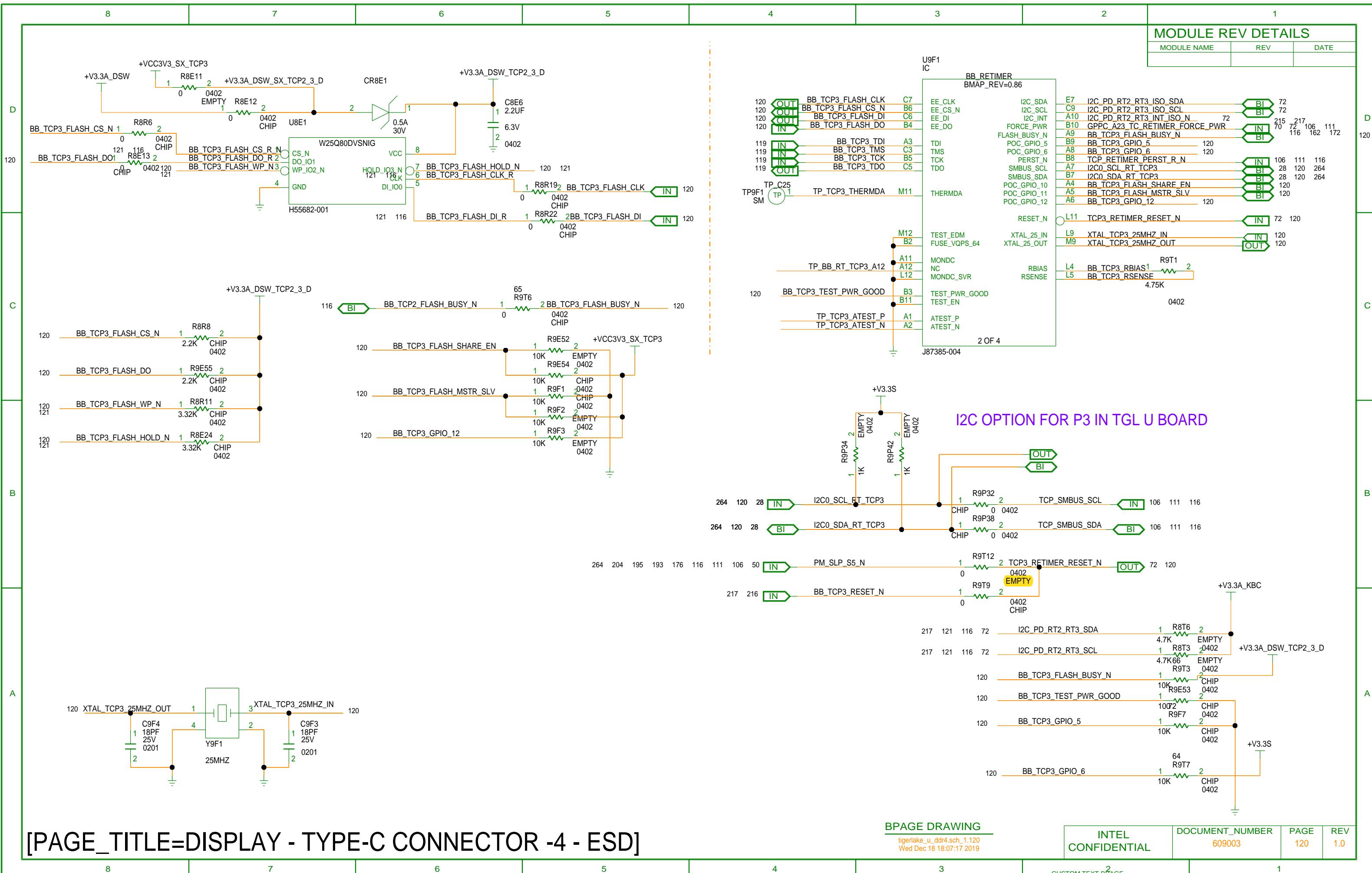
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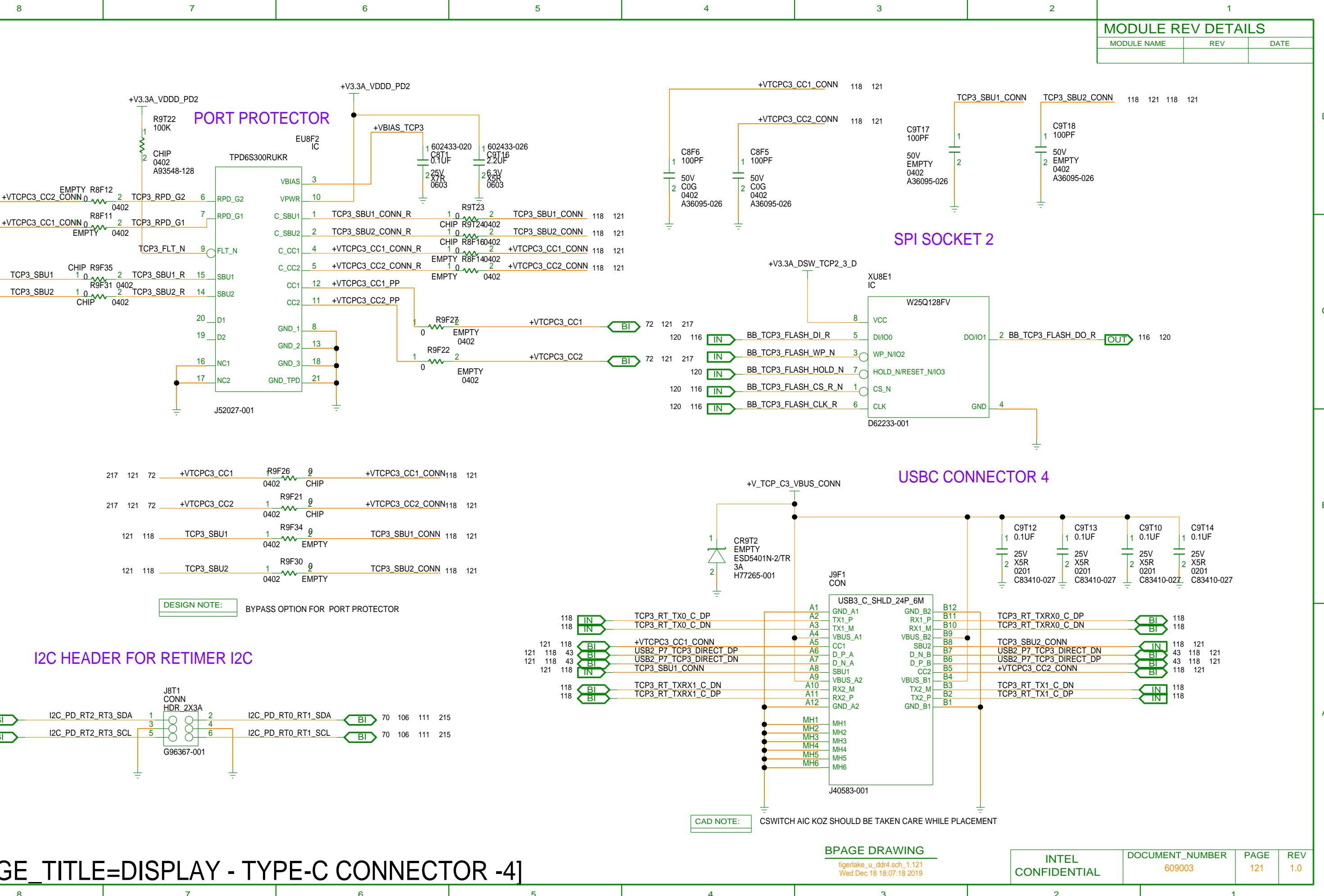
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 116	REV 1.0
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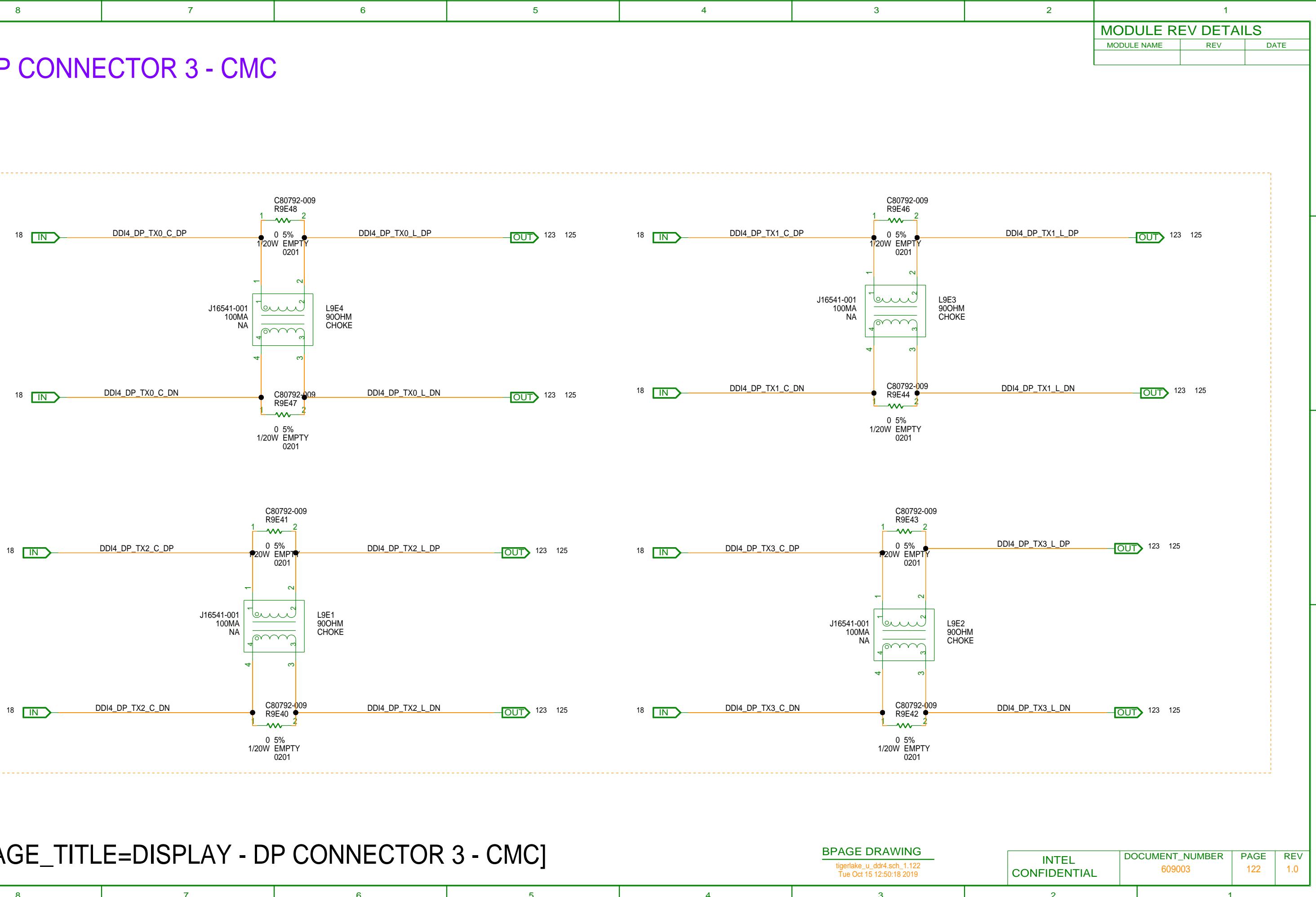








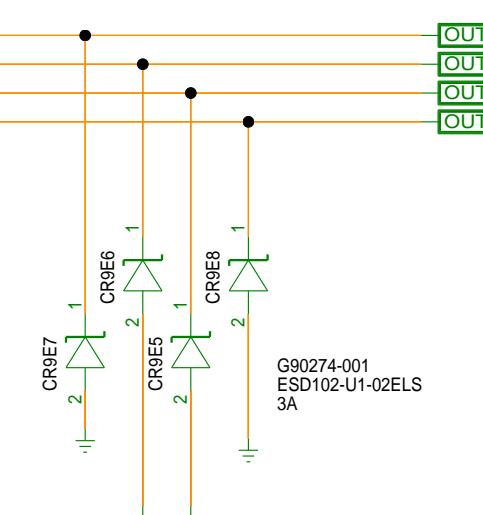
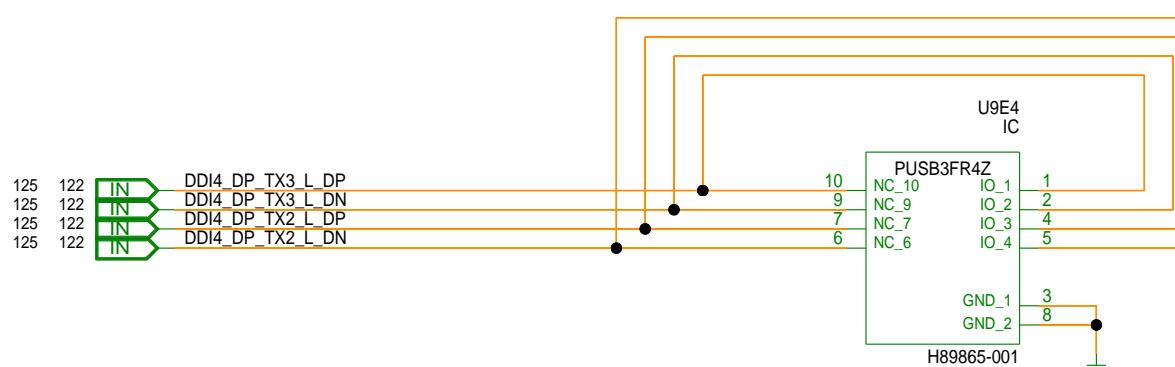
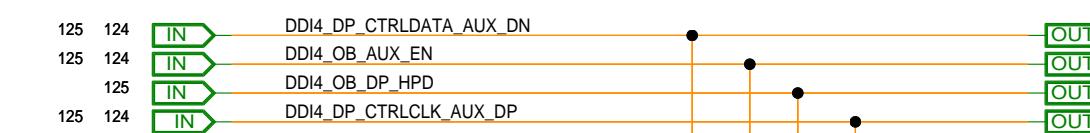
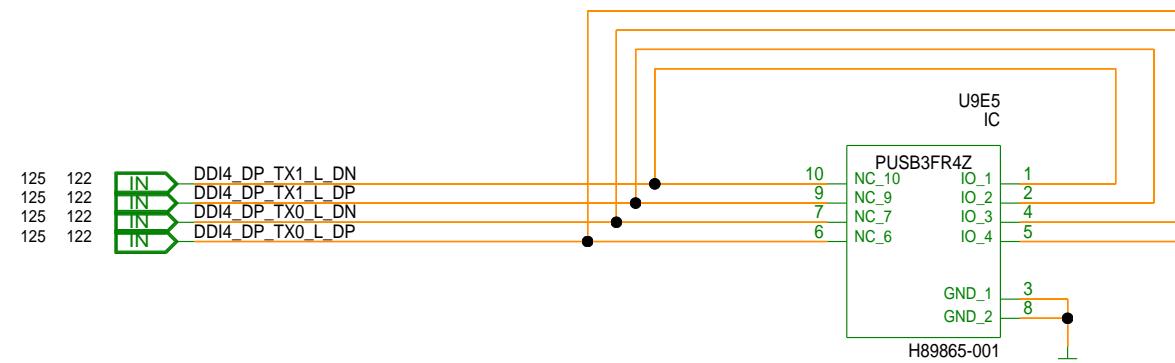




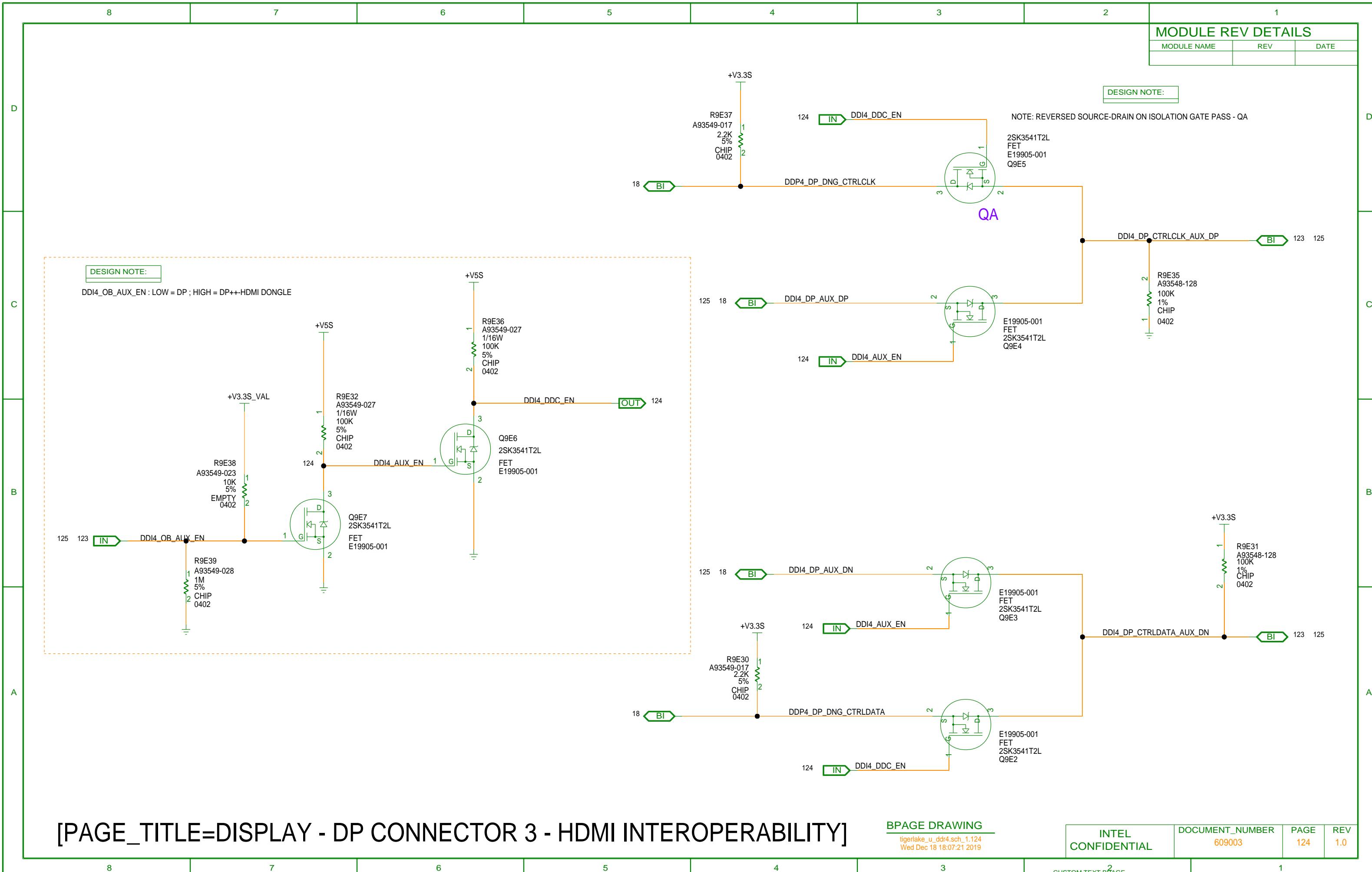
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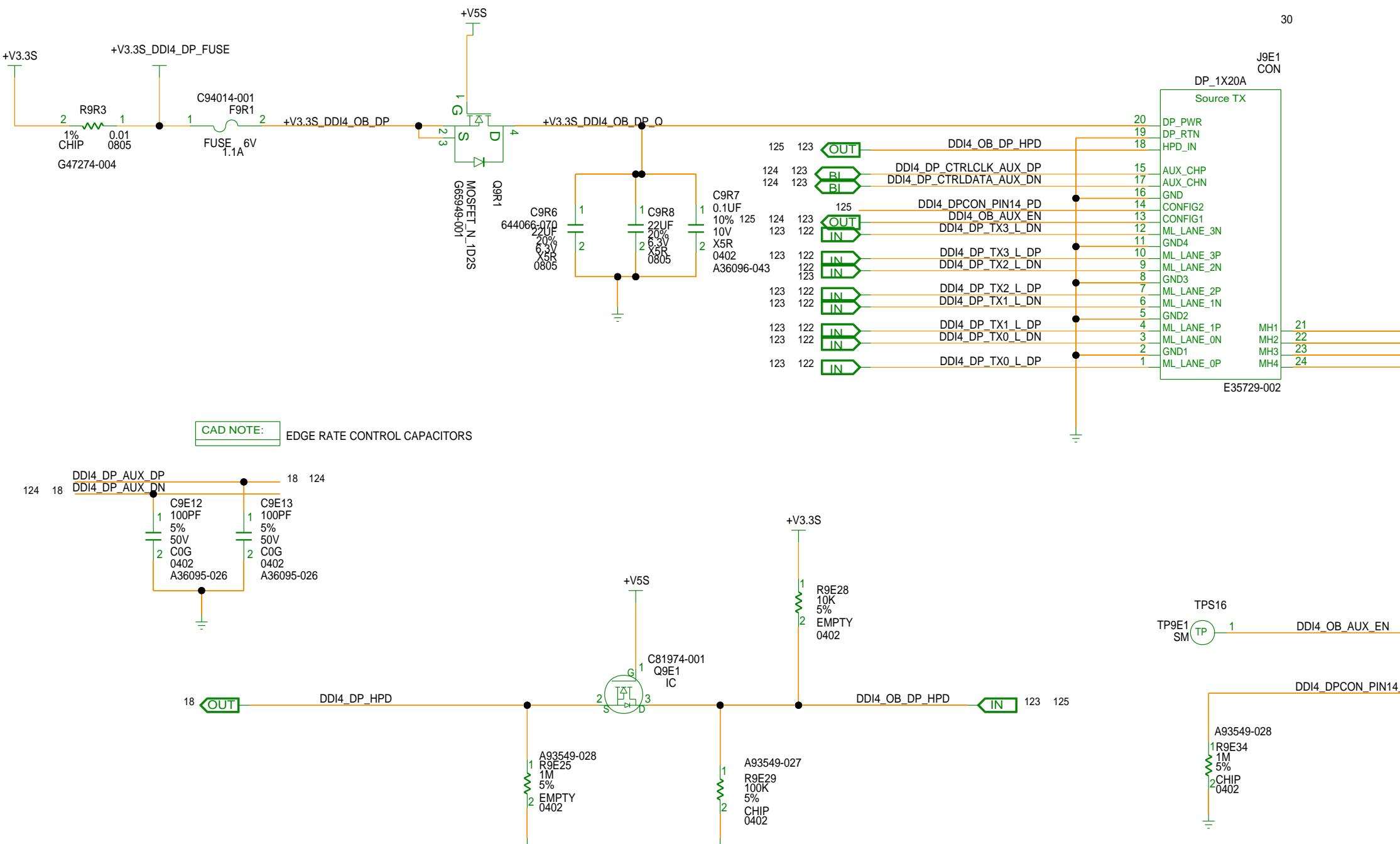


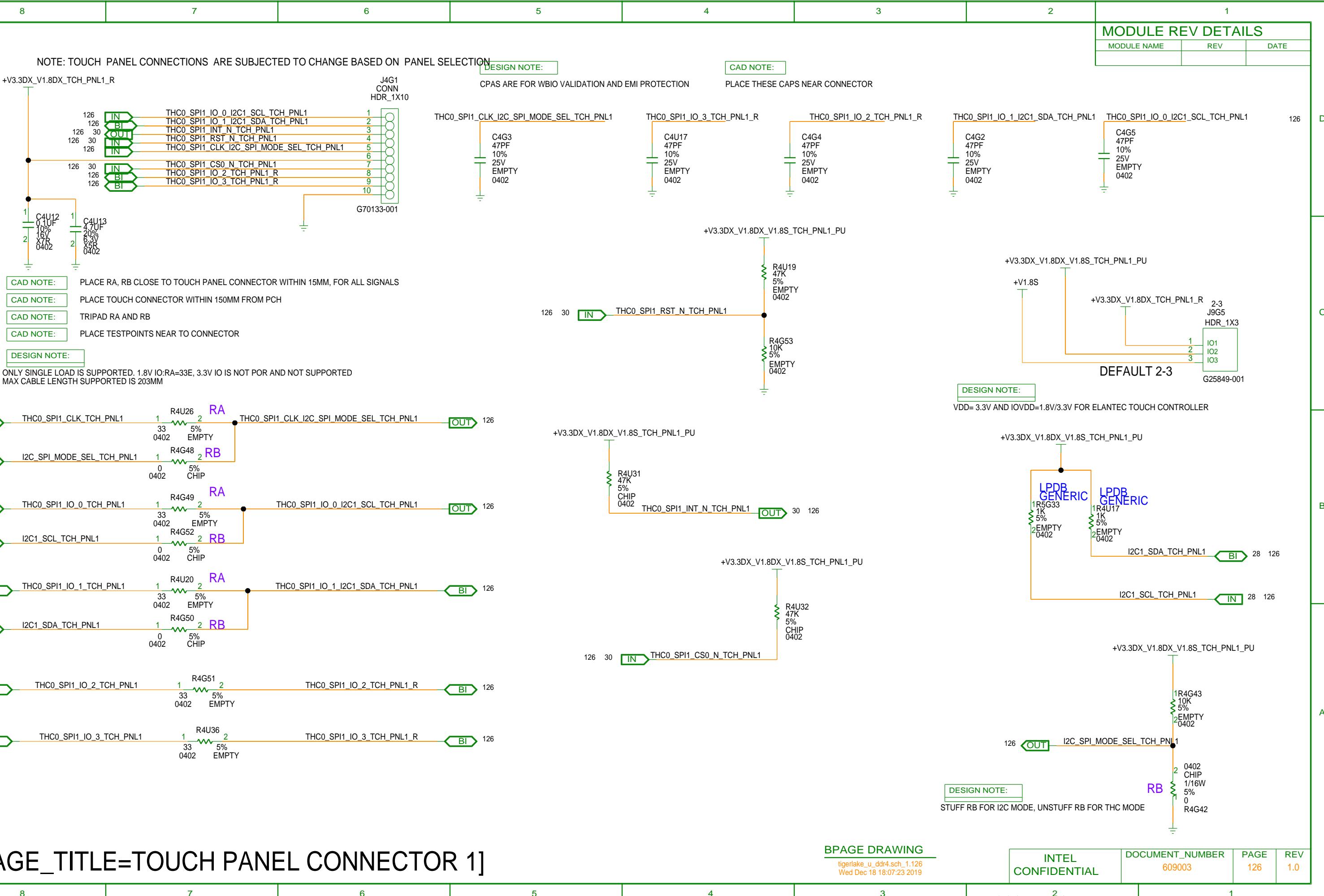
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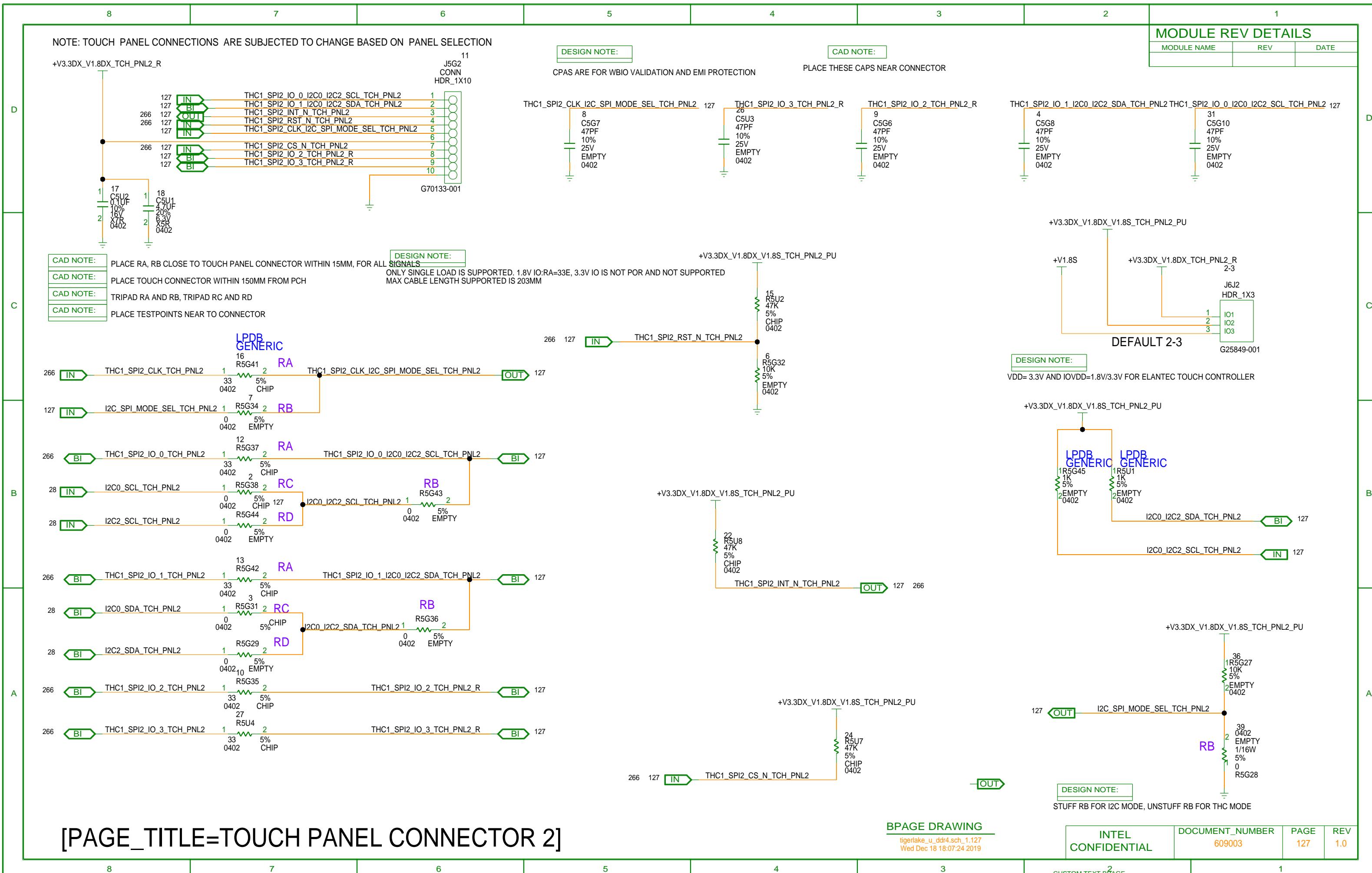


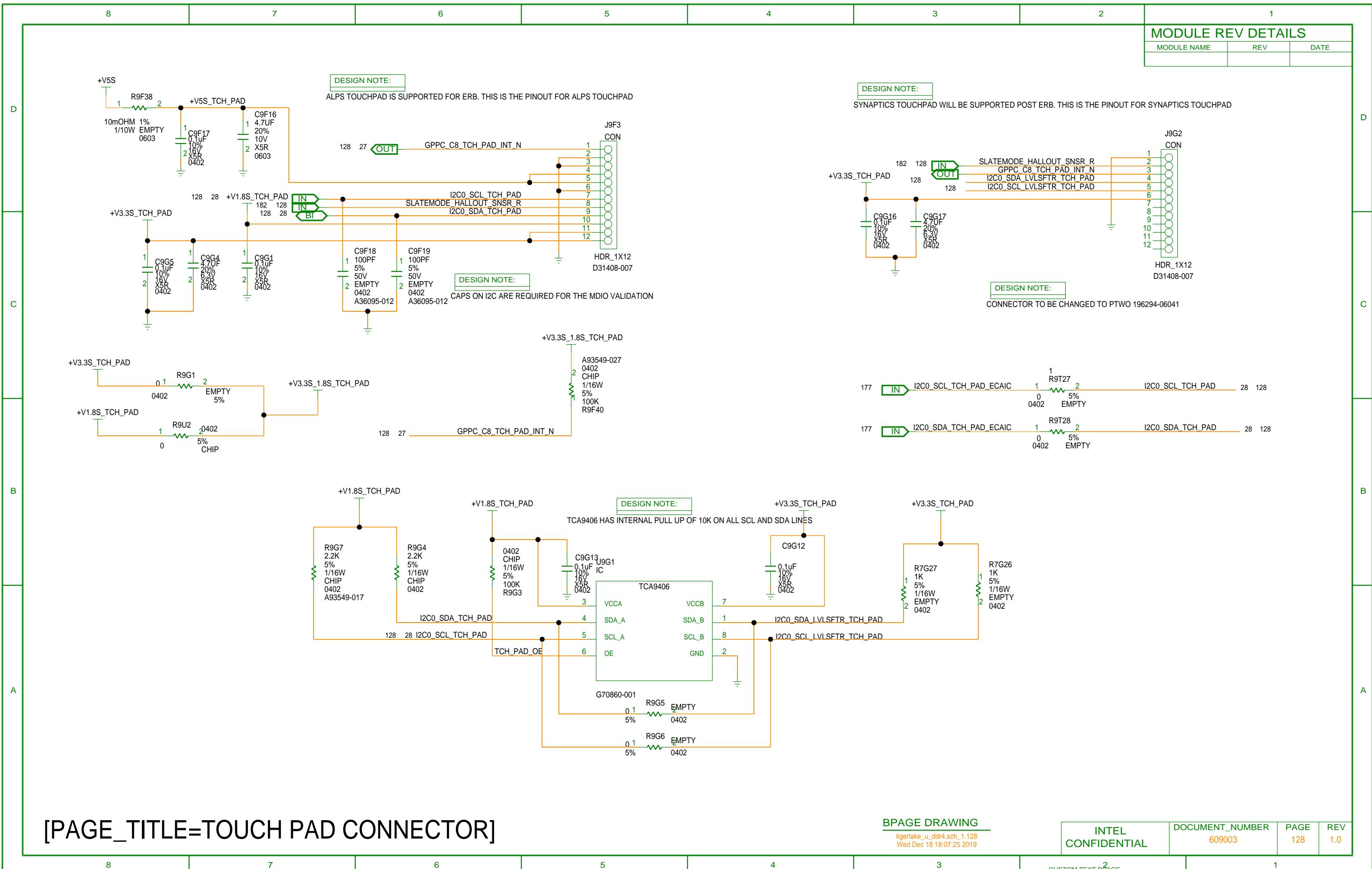
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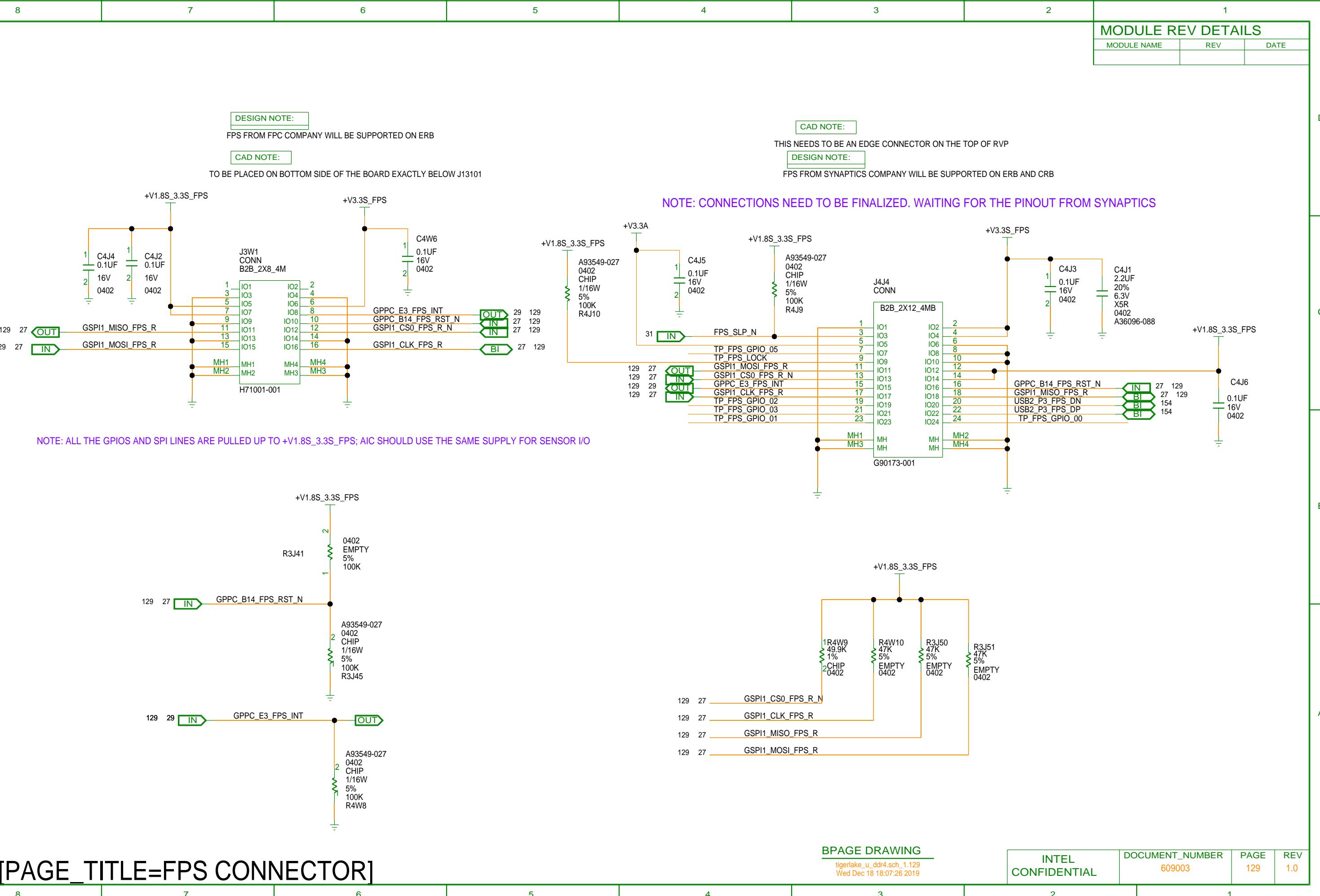
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MODULE NAME	REV	DATE

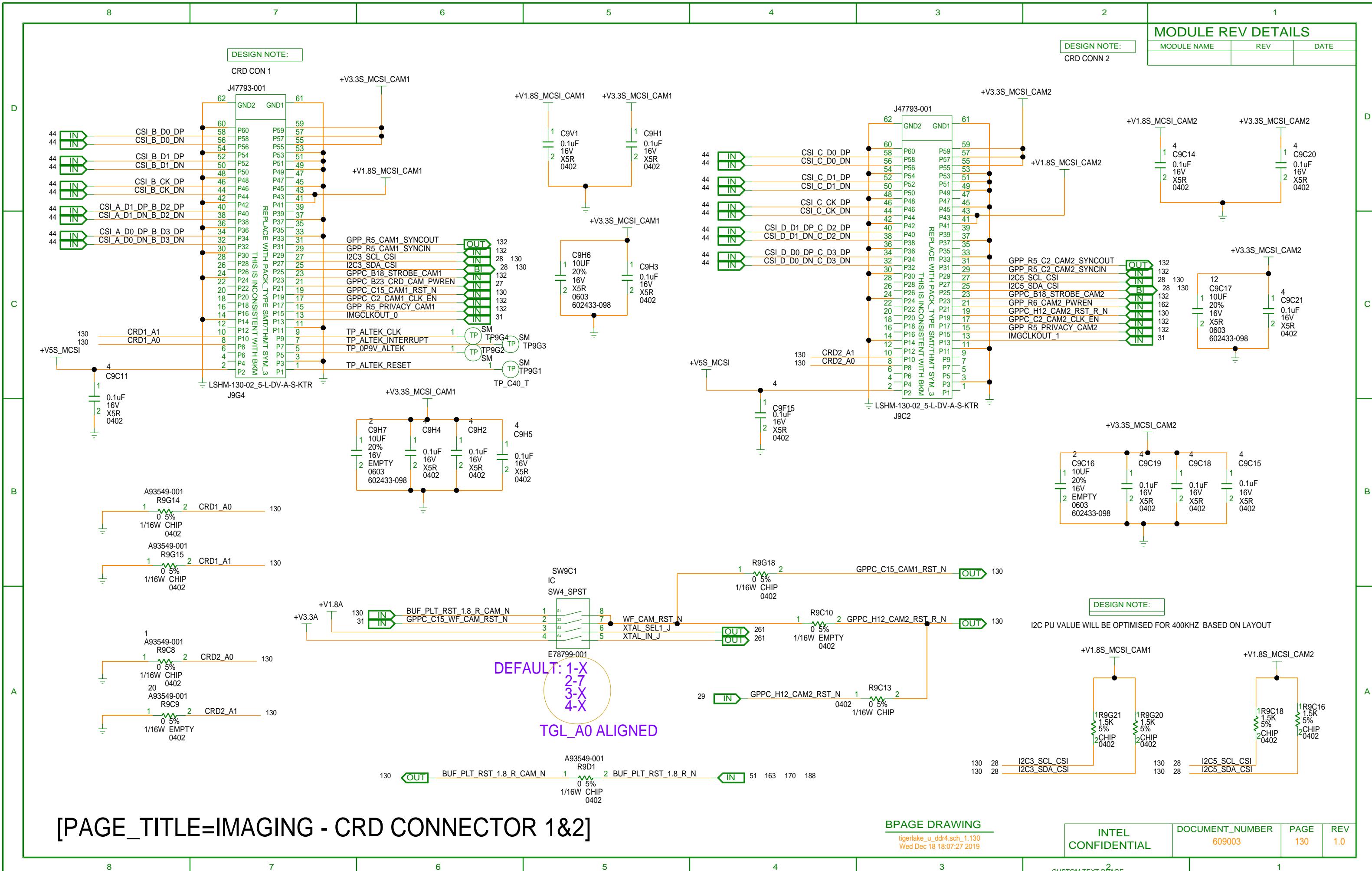








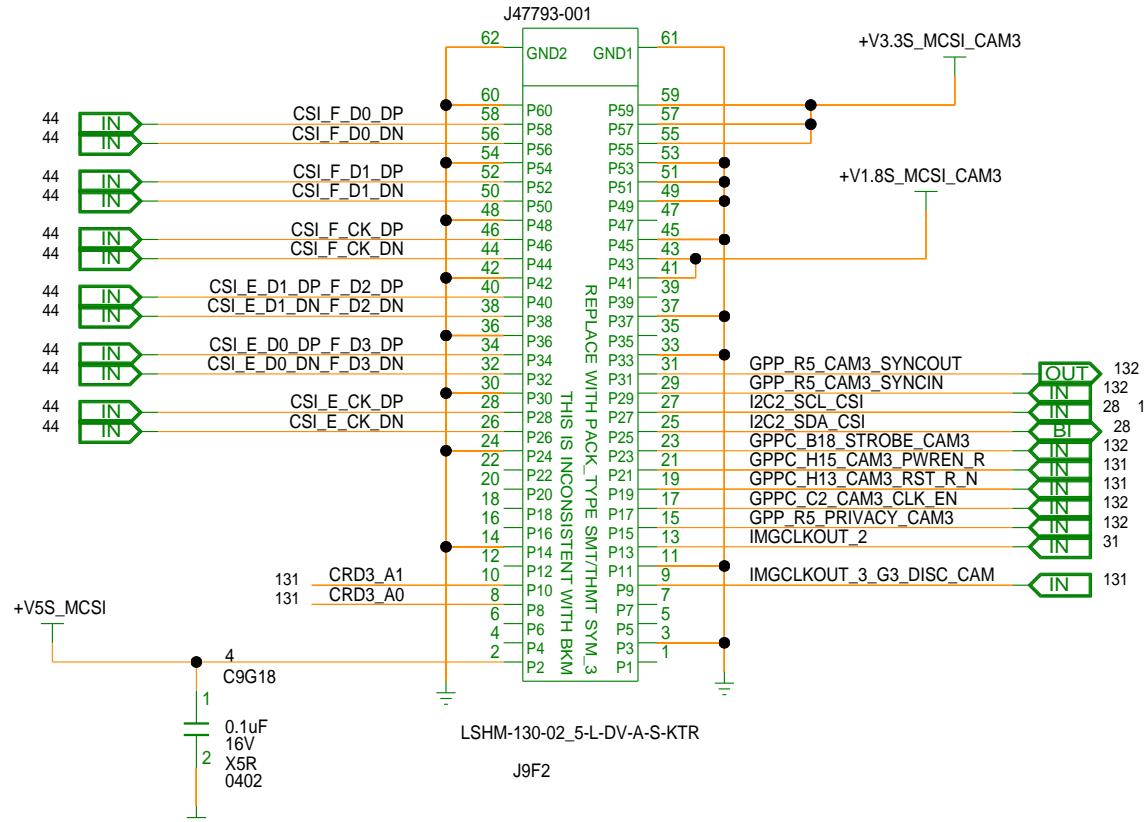




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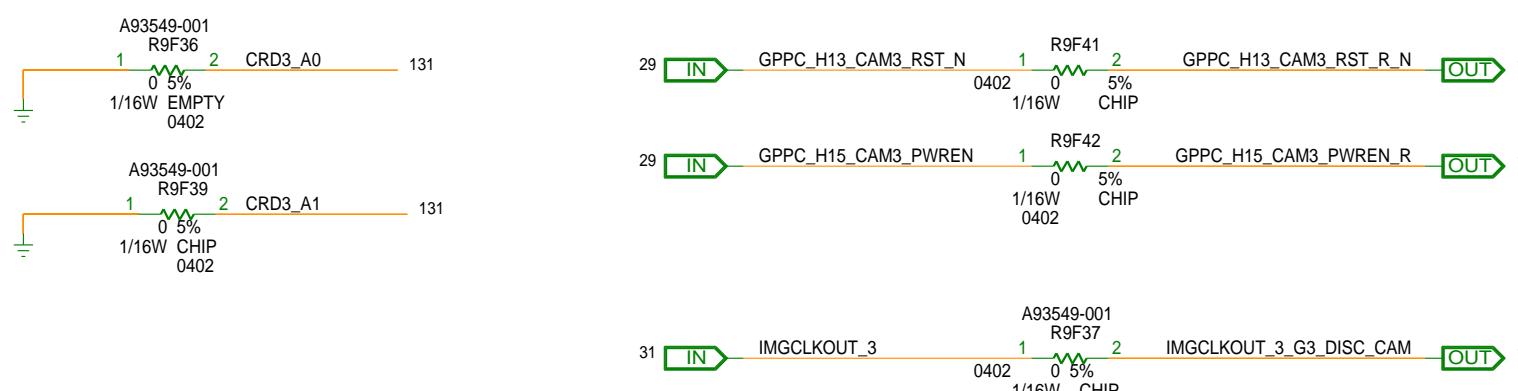
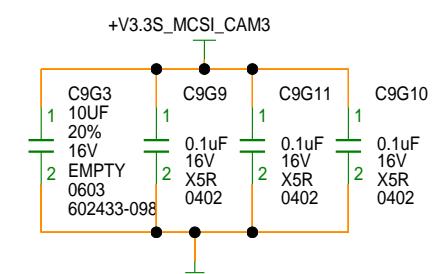
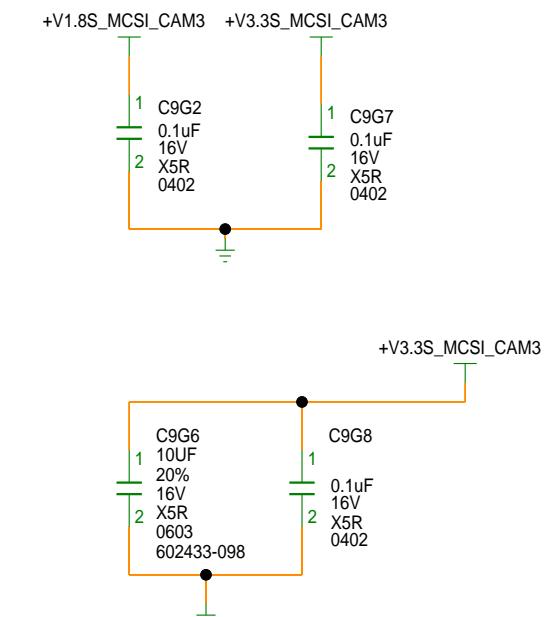
DESIGN NOTE:

CRD CON3

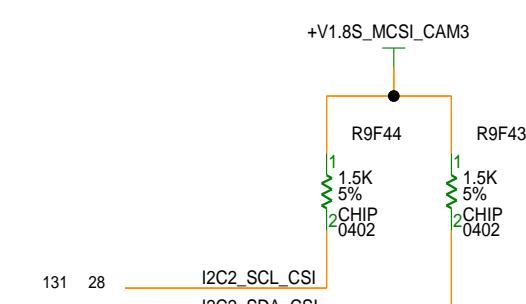


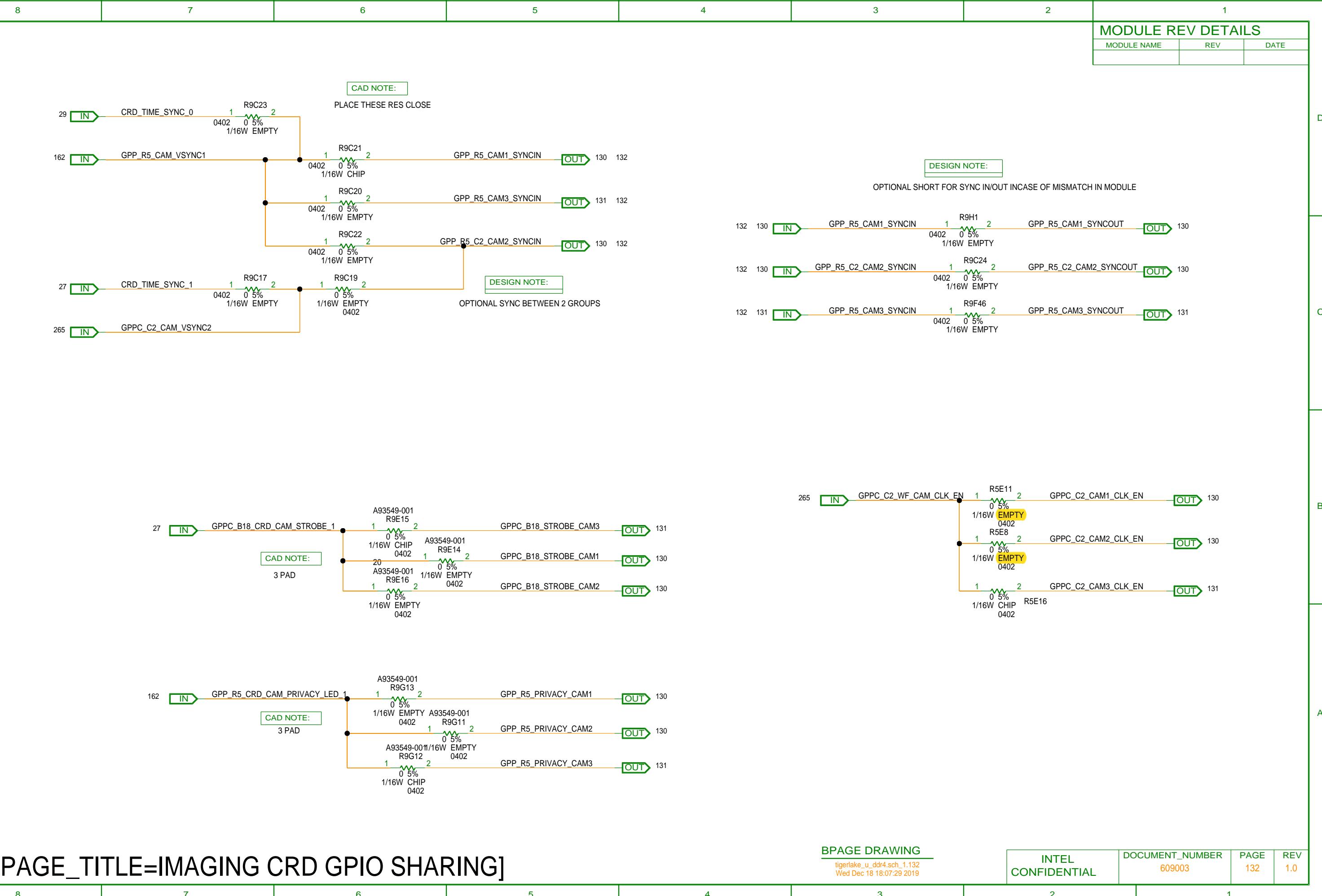
MODULE REV DETAILS

MODULE NAME	REV	DATE



I2C PU VALUE WILL BE OPTIMISED FOR 400KHZ BASED ON LAYOUT





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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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 Tue Oct 15 12:50:30 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 133	REV 1.0
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CUSTOM TEXT 2 PAGE

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MODULE REV DETAILS

MODULE NAME	REV	DATE

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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 135	REV 1.0
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8	7	6	5	4	3	CUSTOM TEXT ² PAGE	1
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MODULE REV DETAILS

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MODULE NAME		REV	DATE				

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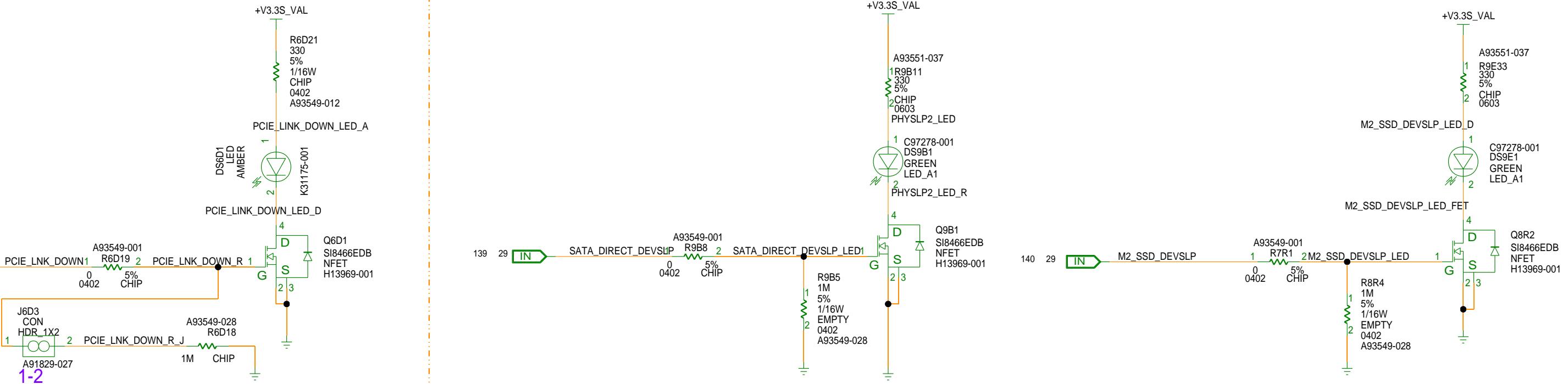
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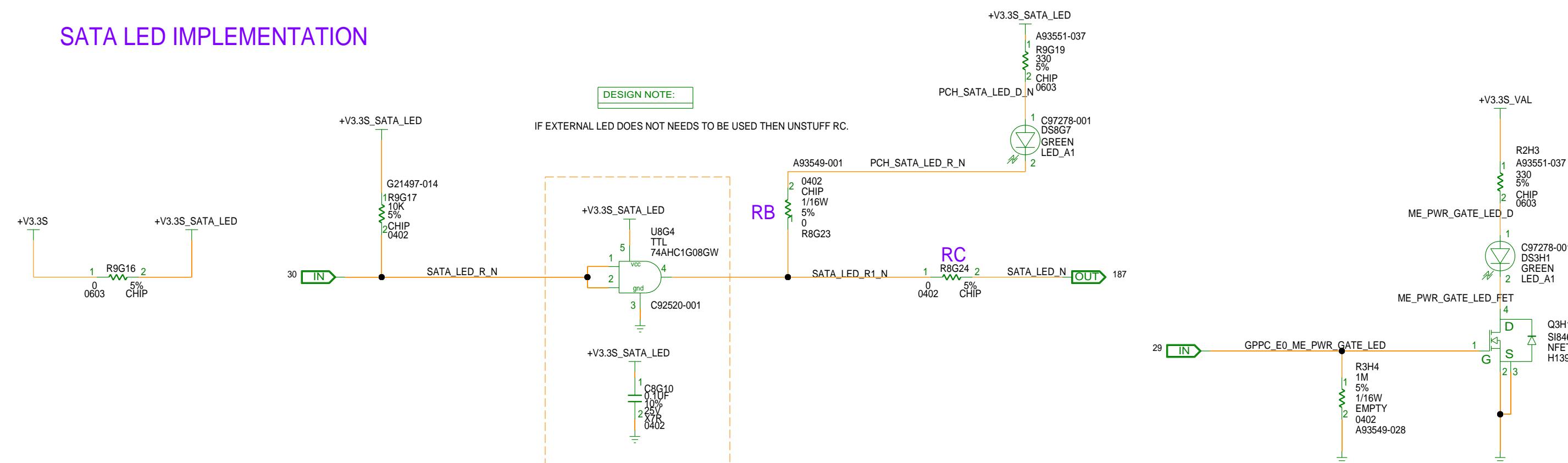
PCIE_LINK_DOWN_LED

SATA DEV SLEEP LED

MODULE REV DETAILS		
MODULE NAME	REV	DATE



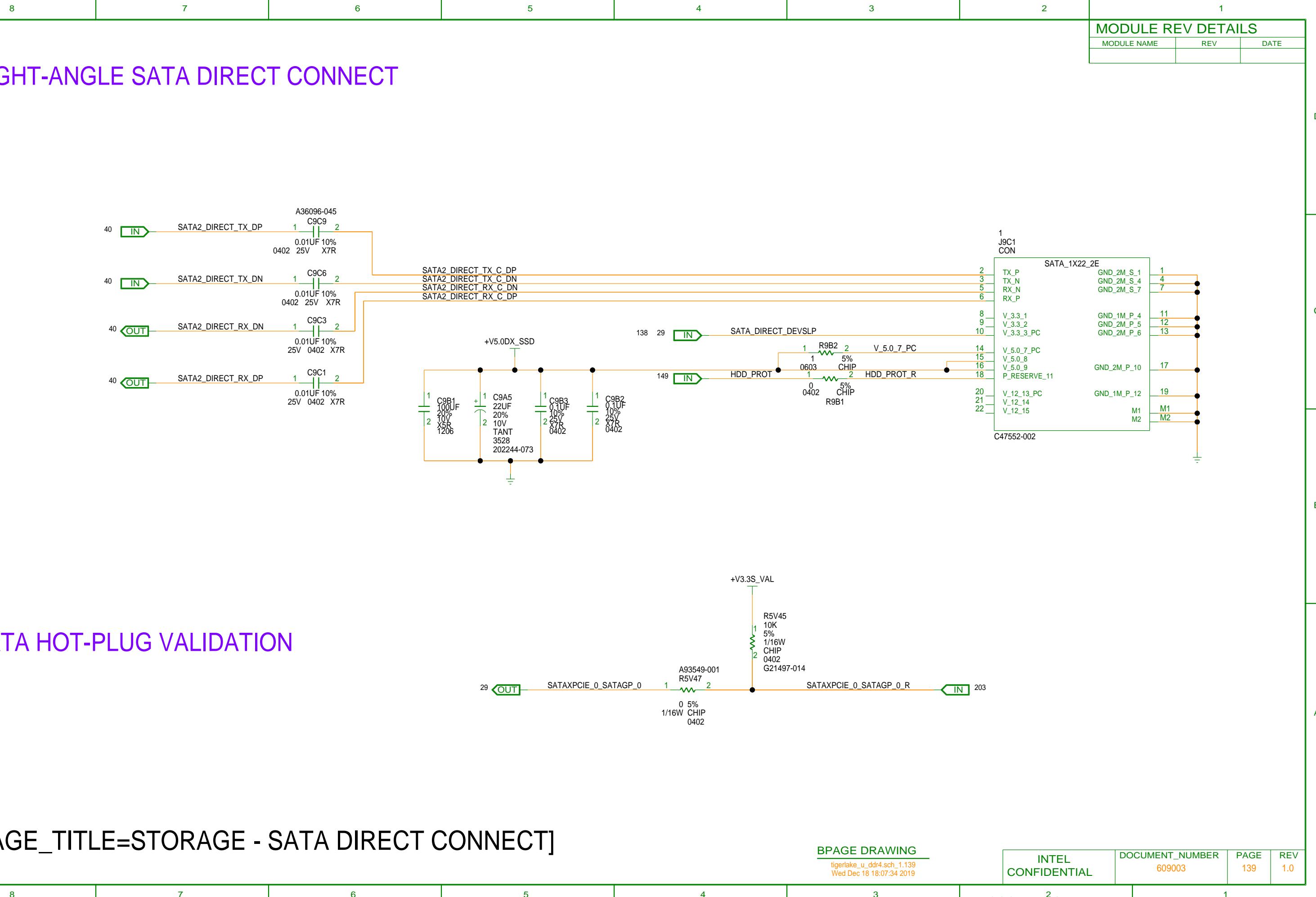
SATA LED IMPLEMENTATION

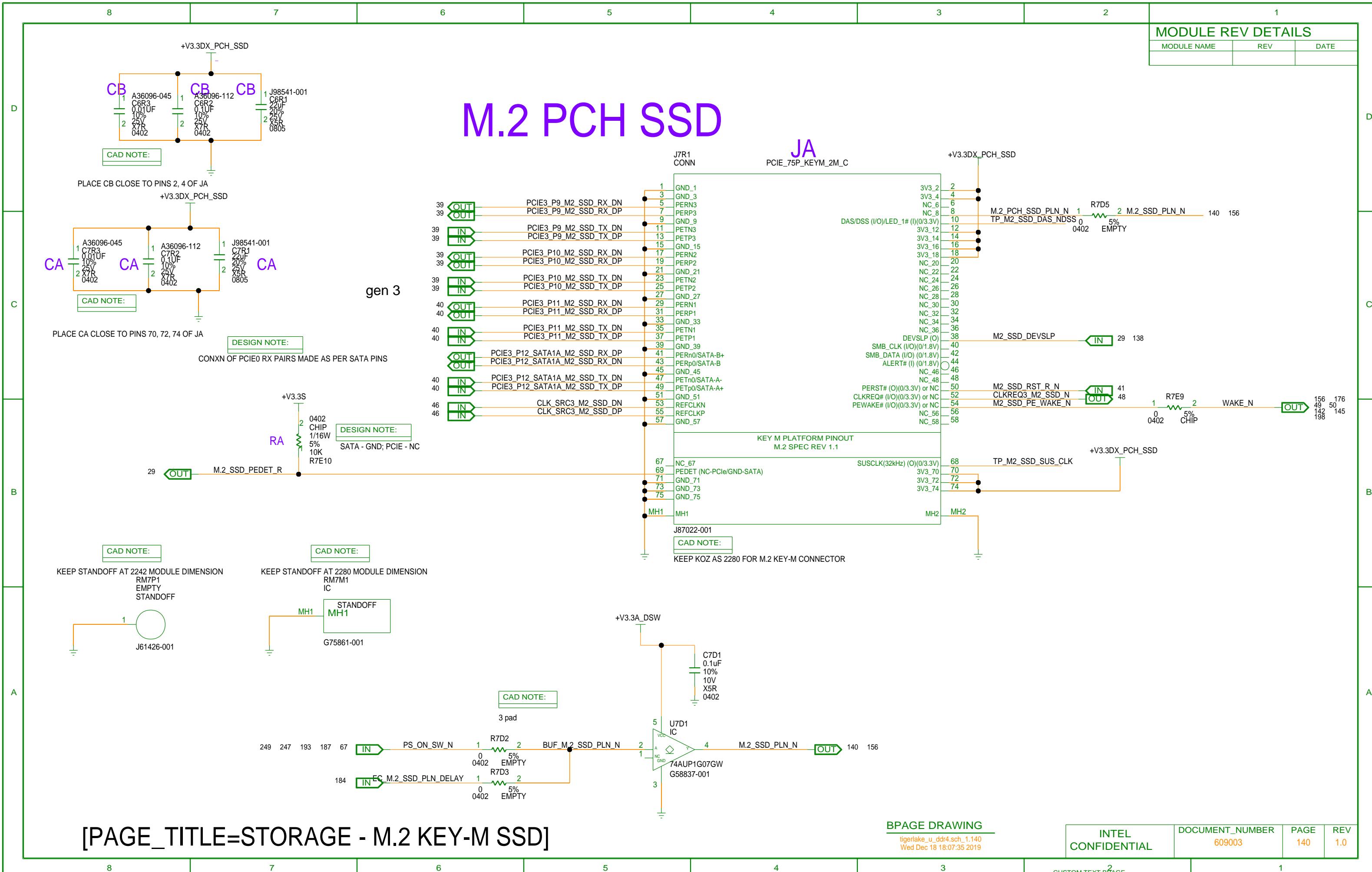


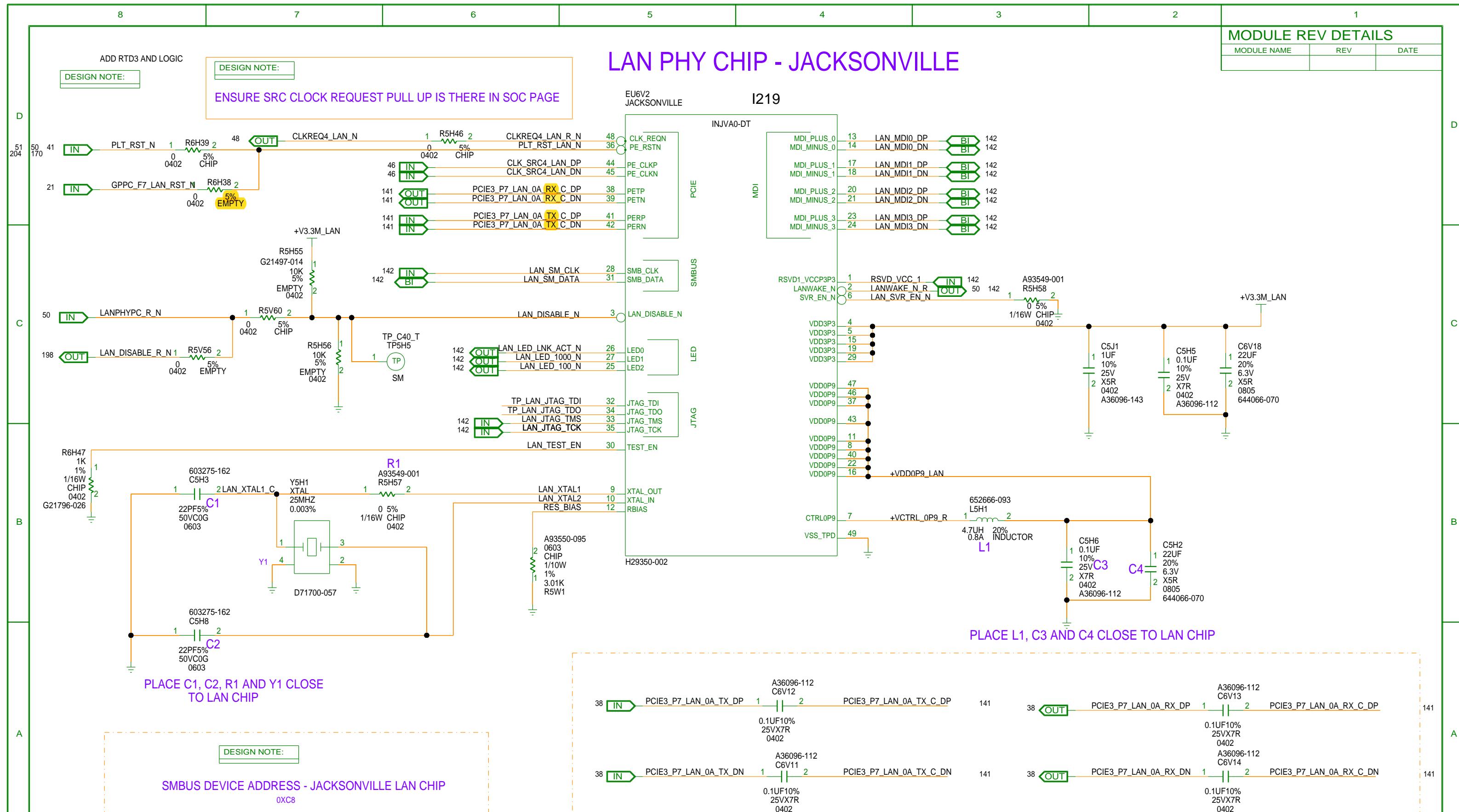
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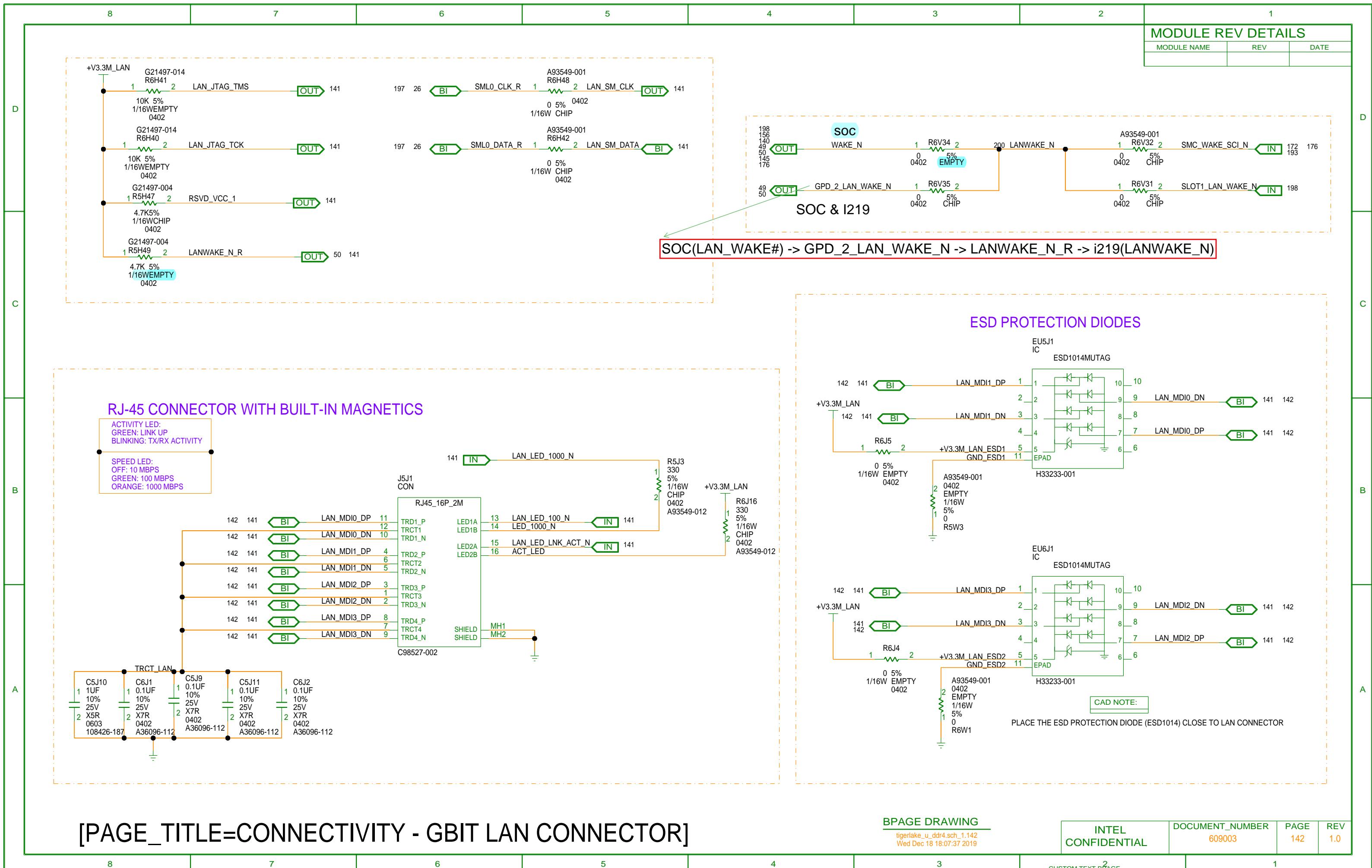
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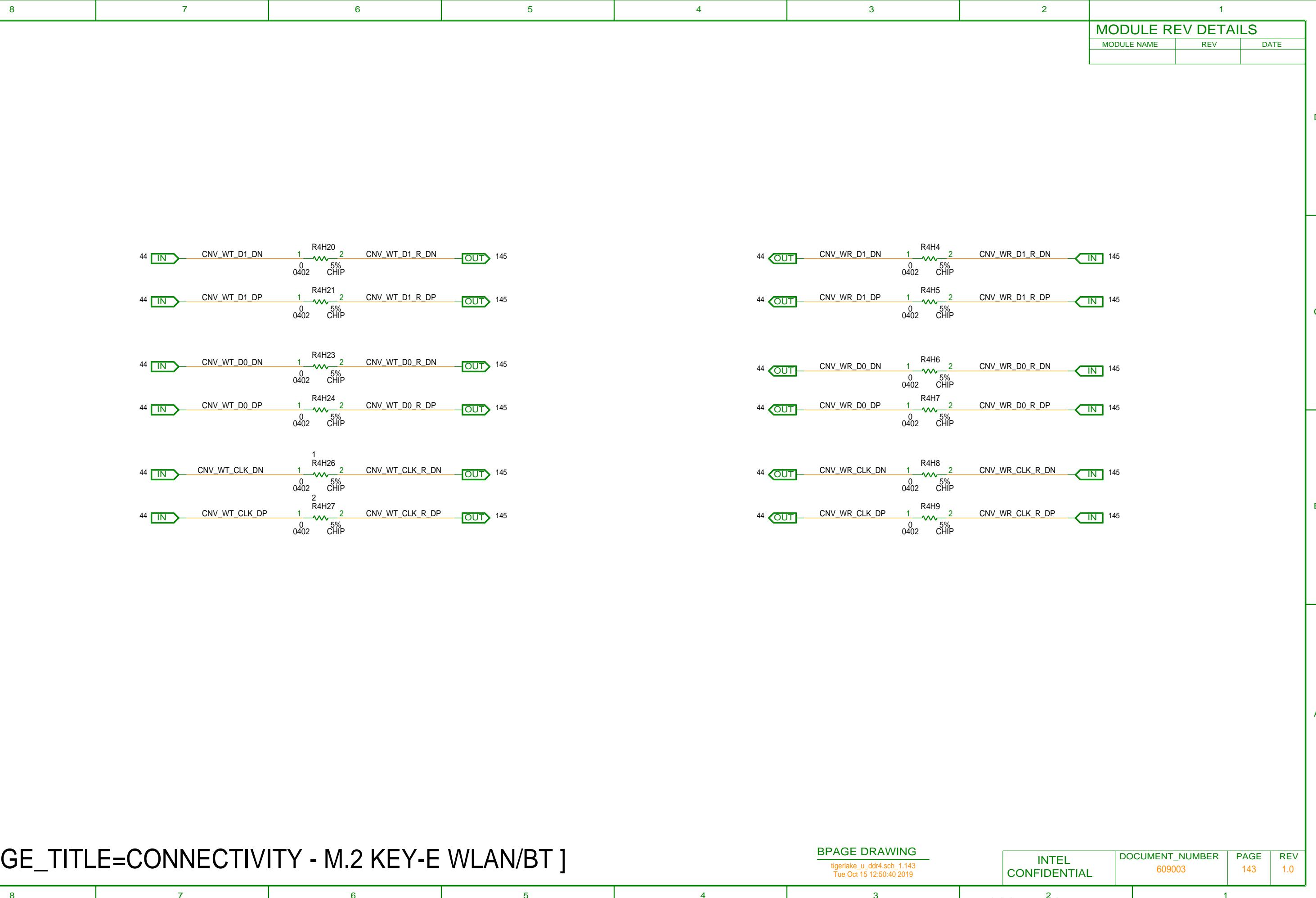
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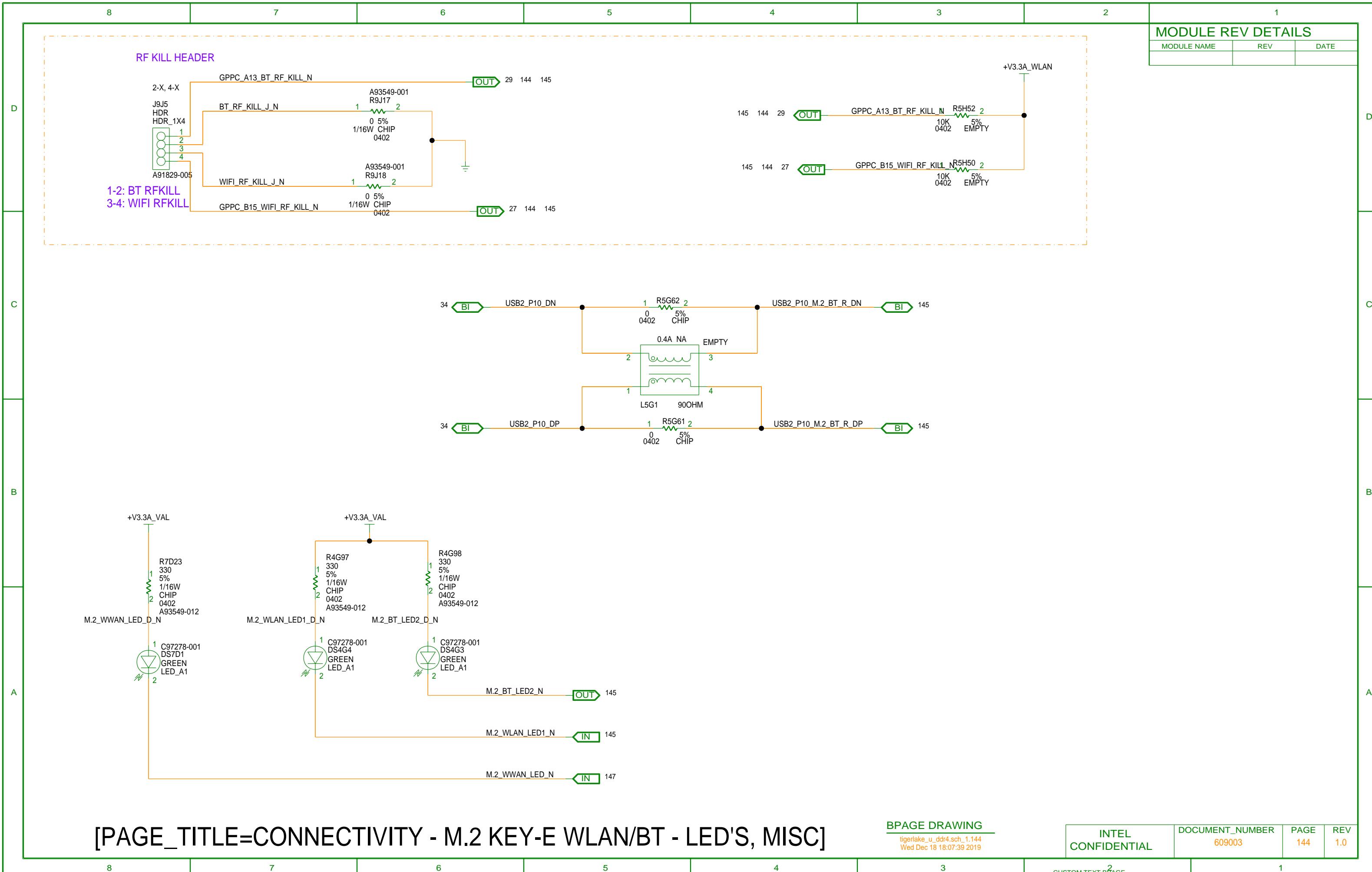


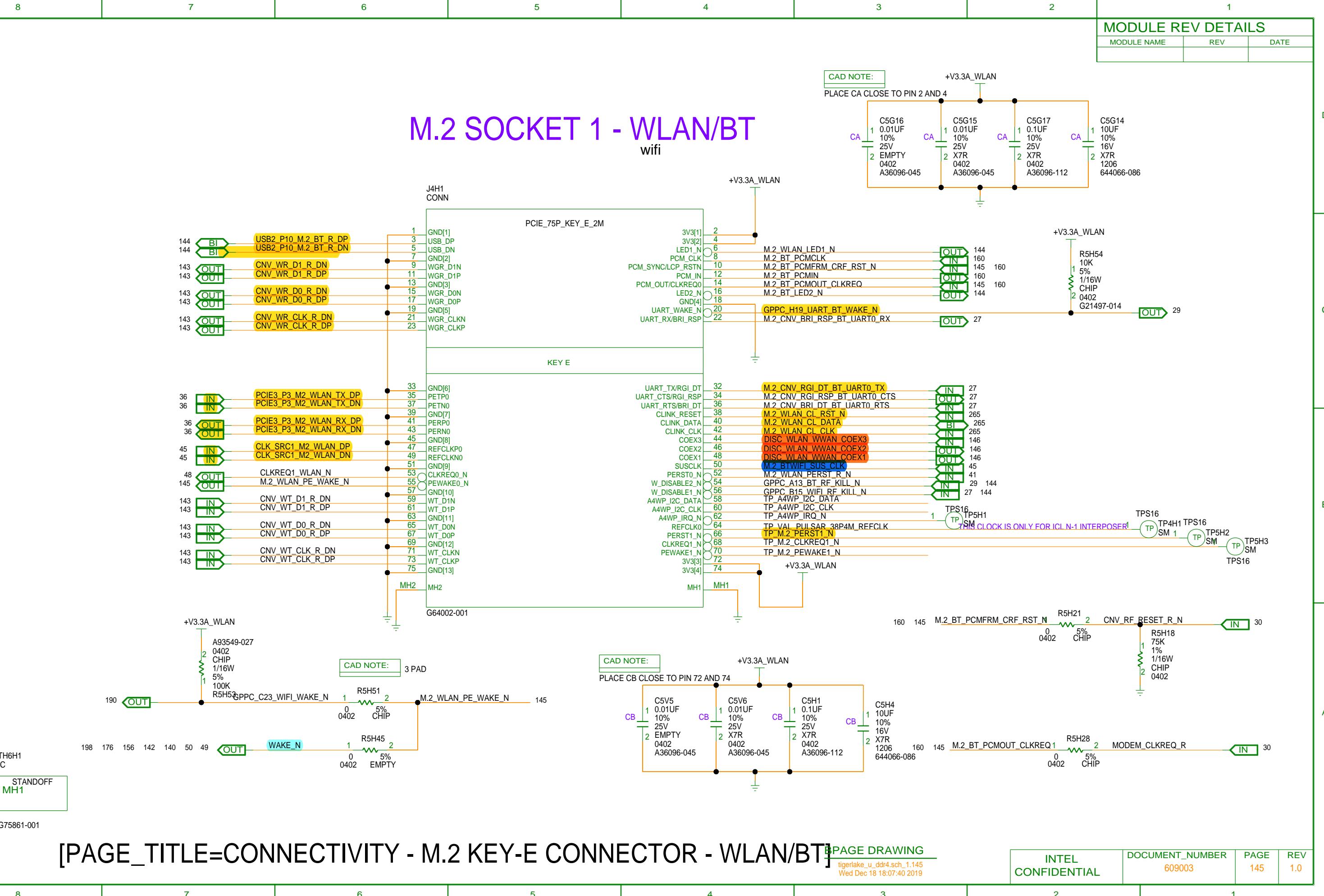


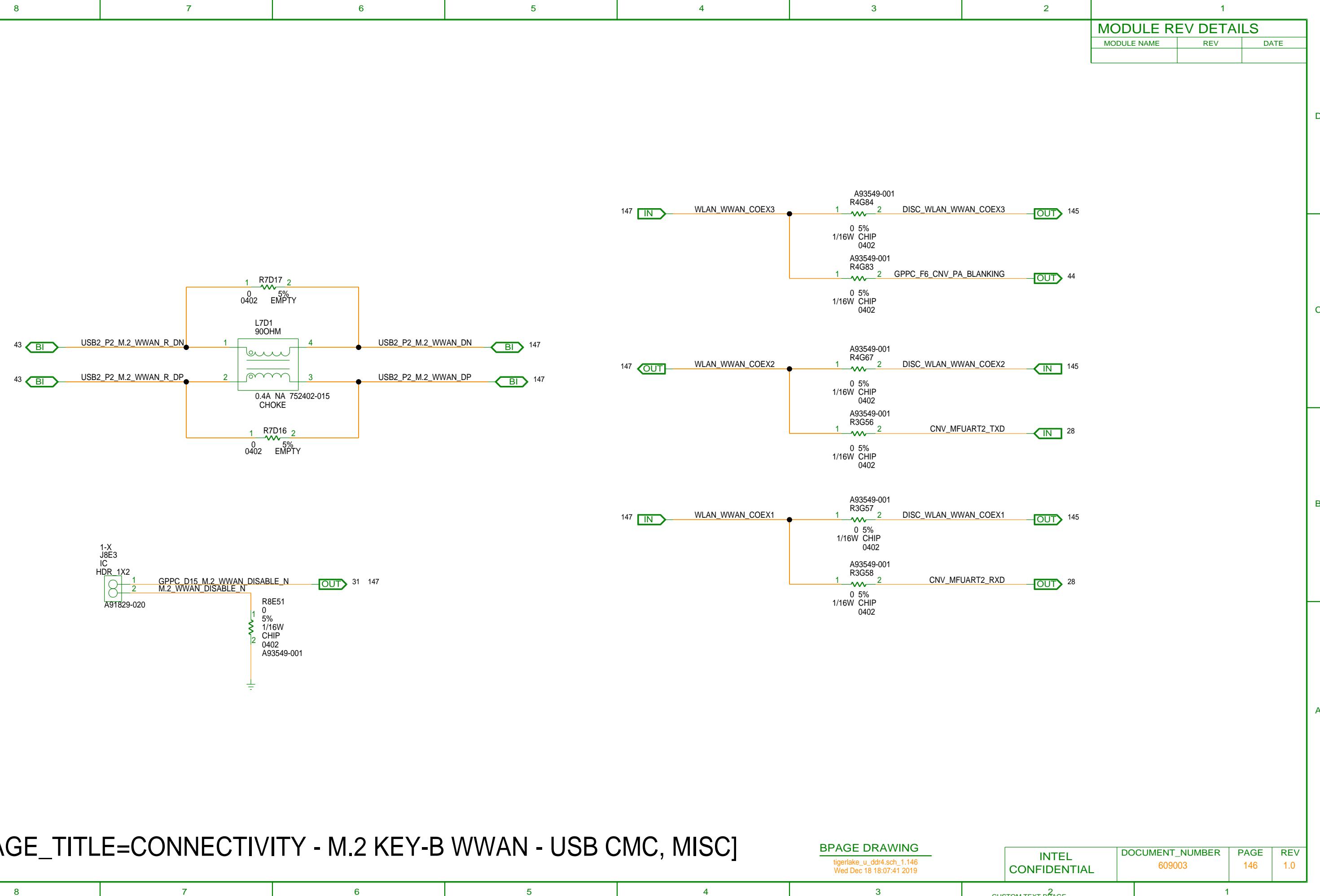


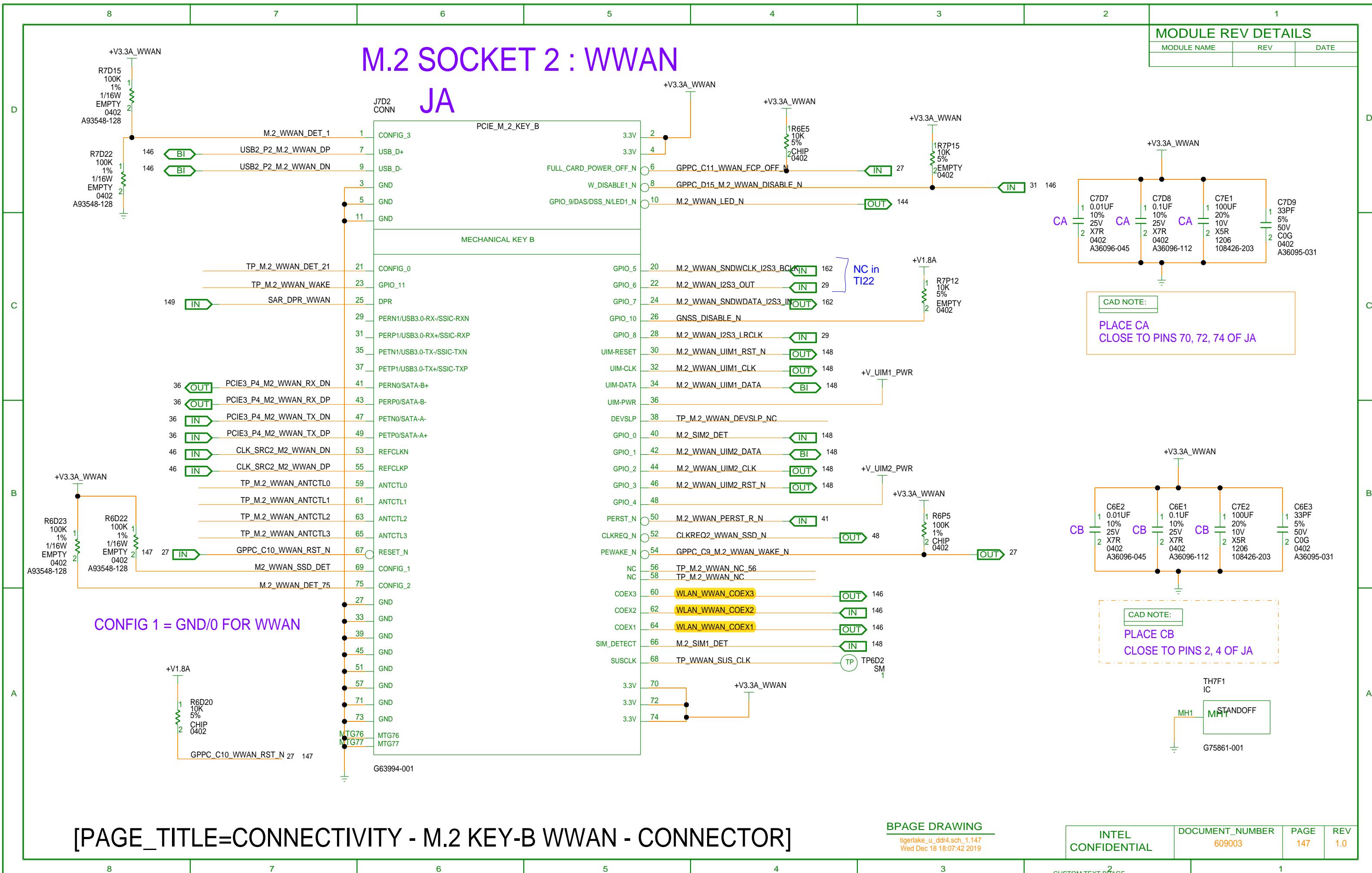


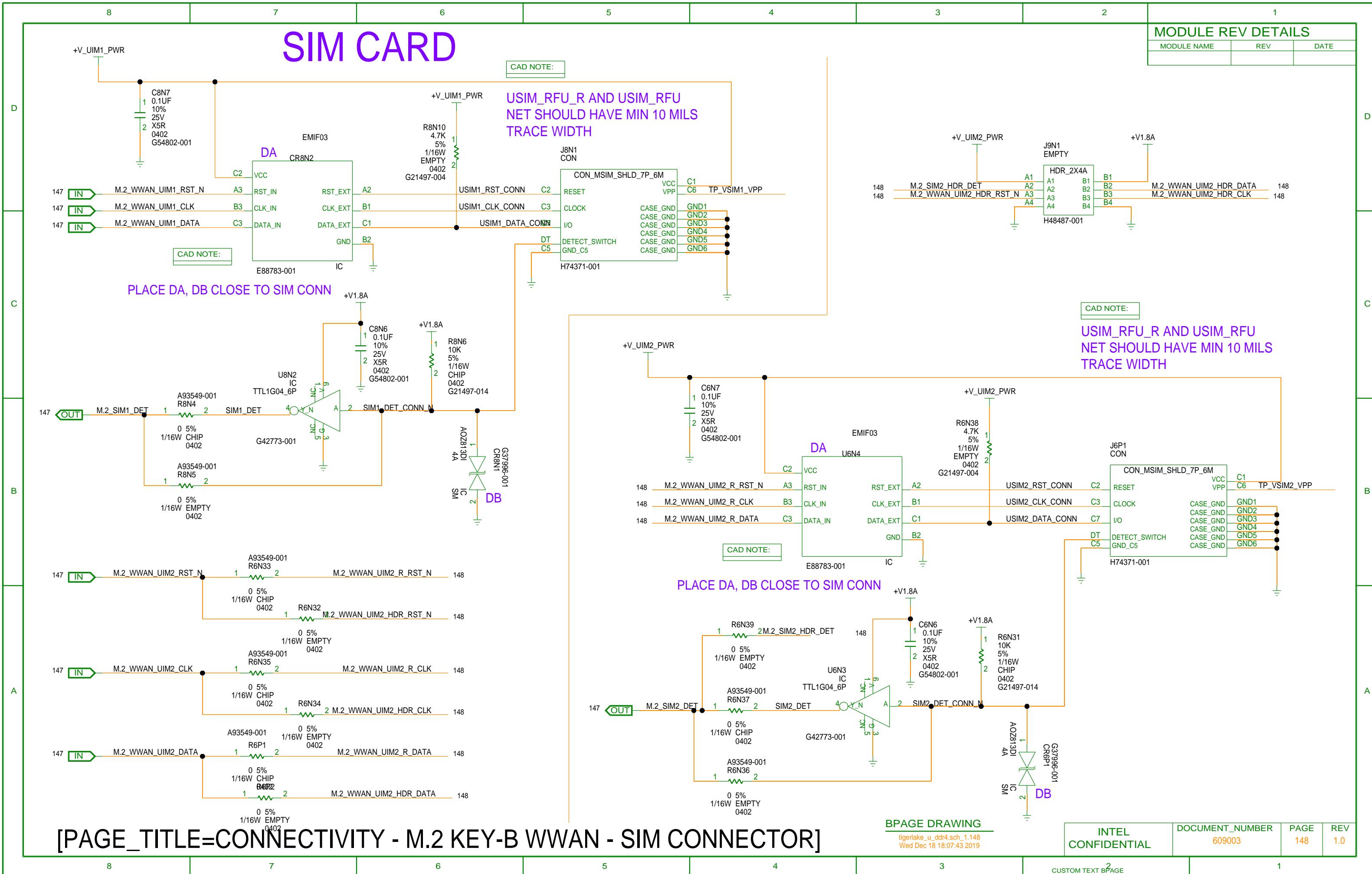


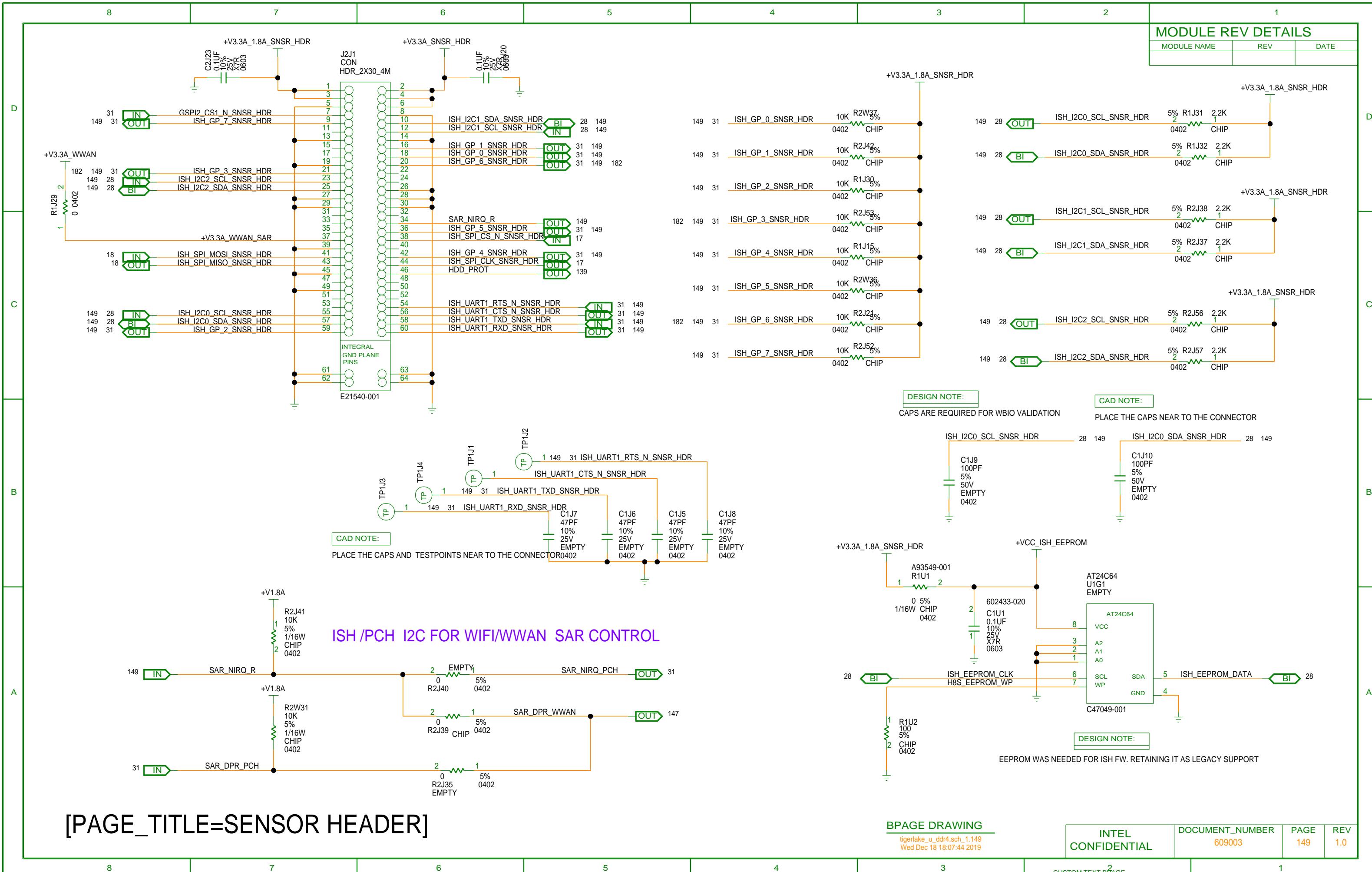






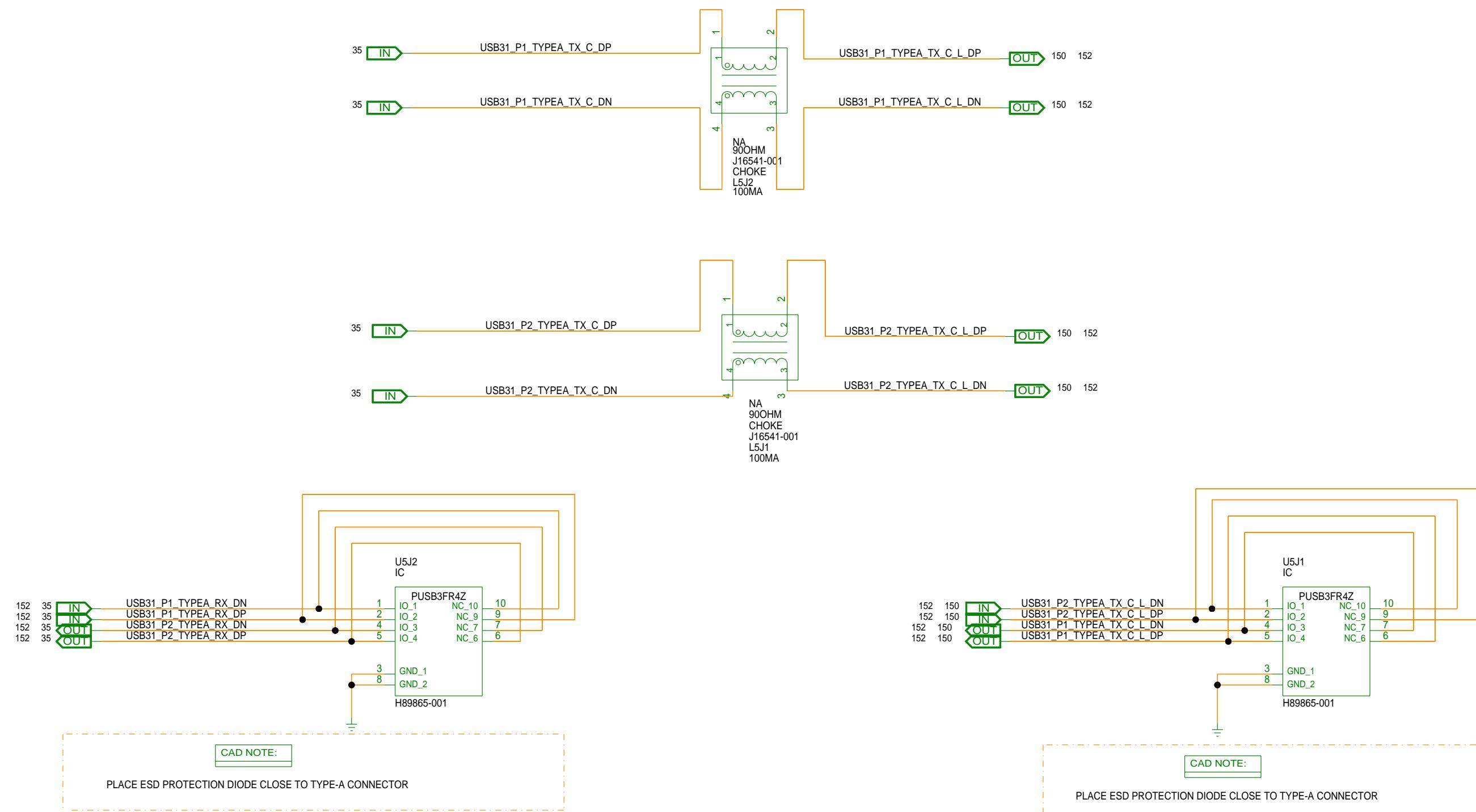






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USB3.1 CMC/ESD

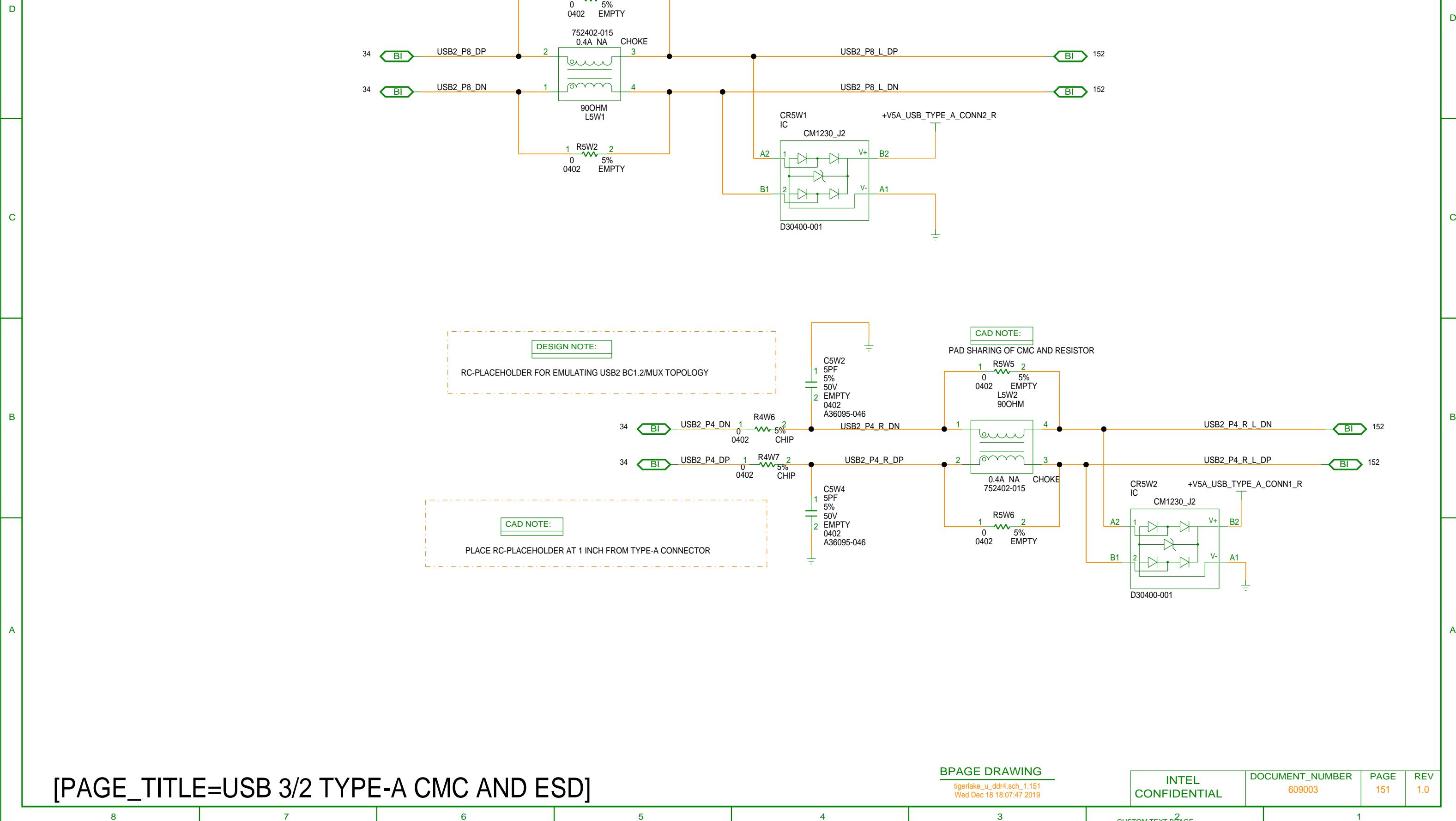


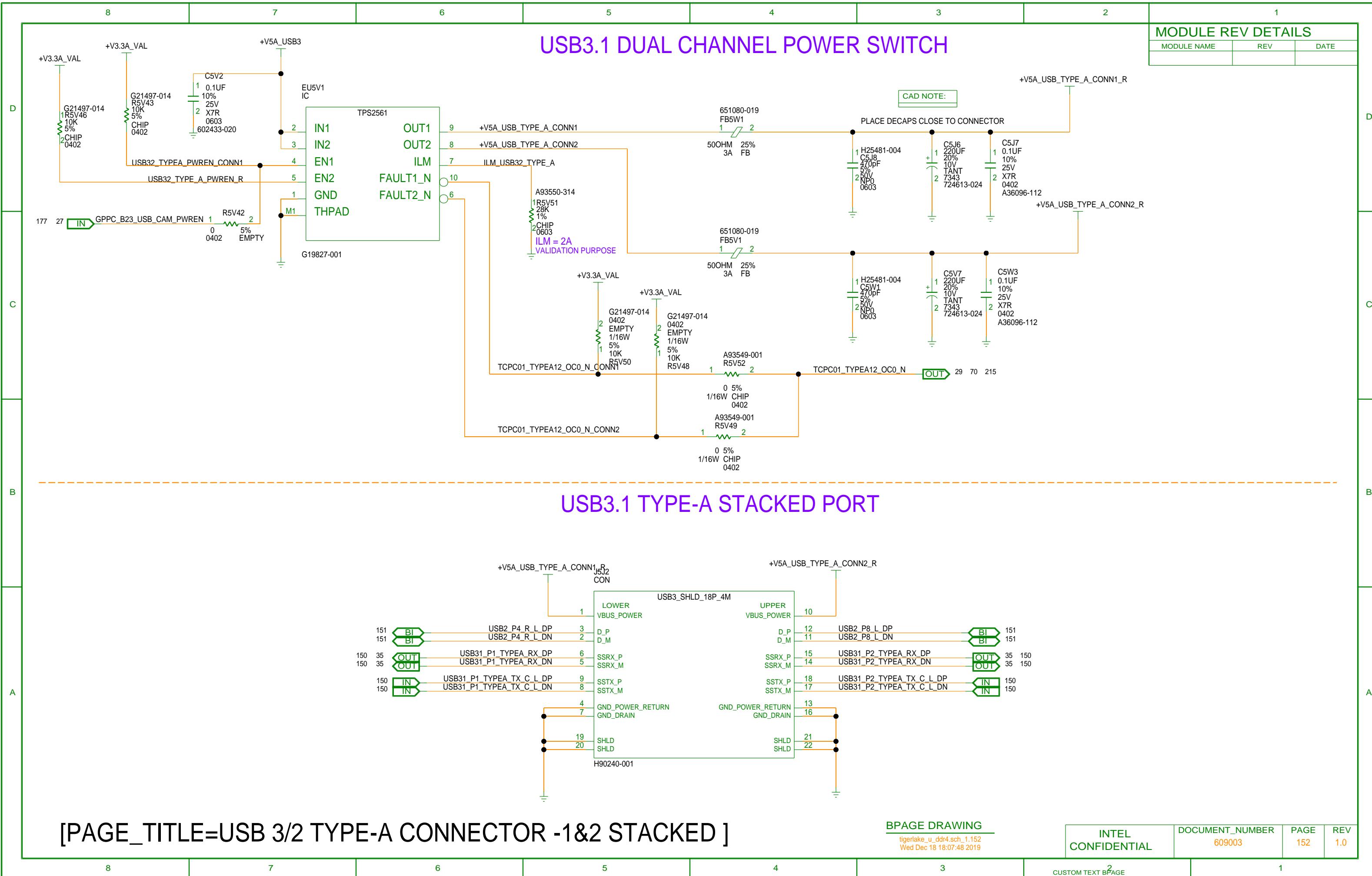
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USB 4 & 8 CMC/ESD

MODULE REV DETAILS

MODULE NAME	REV	DATE





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MODULE REV DETAILS

MODULE NAME	REV	DATE

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tigerlake_u_ddr4.sch_1.153
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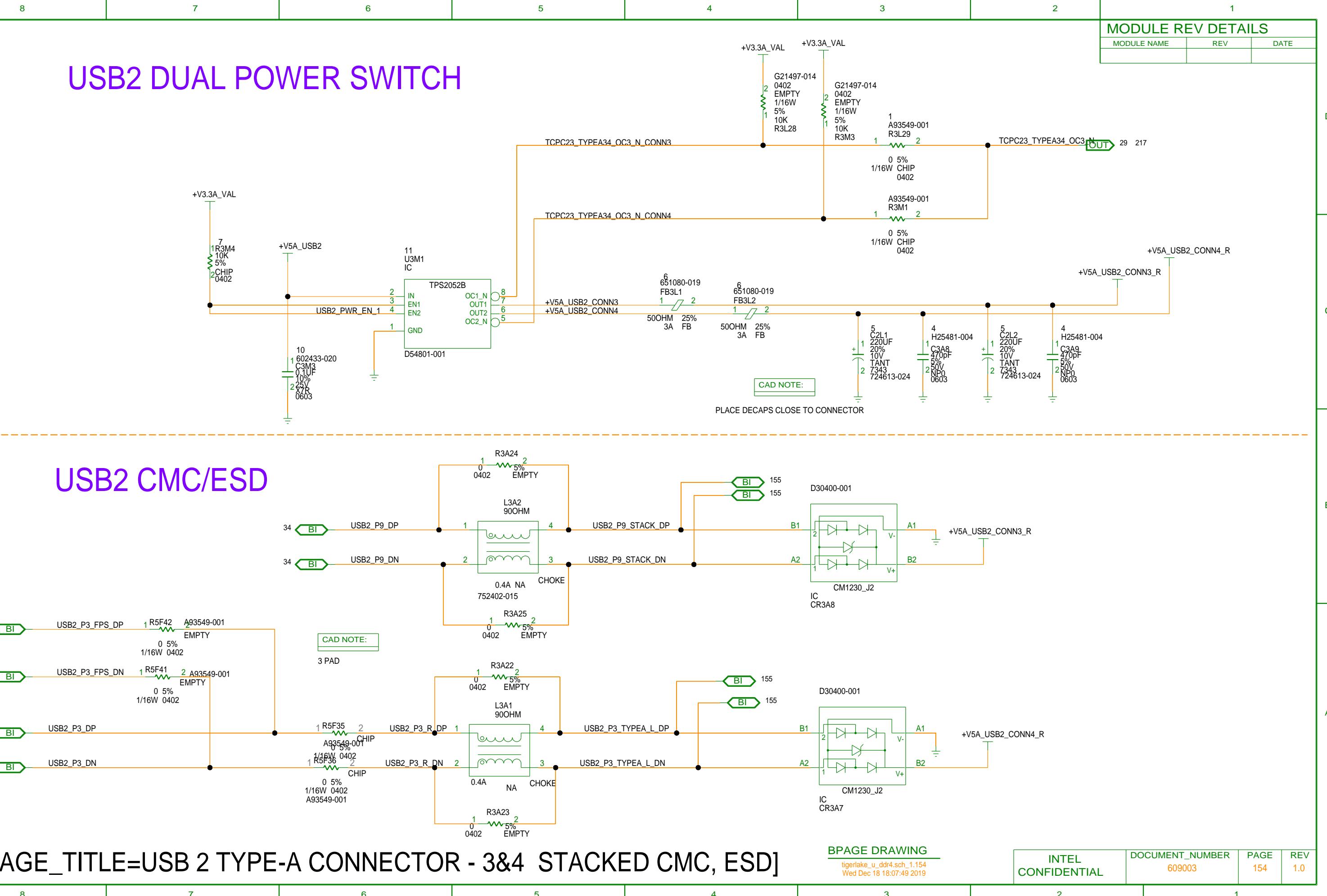
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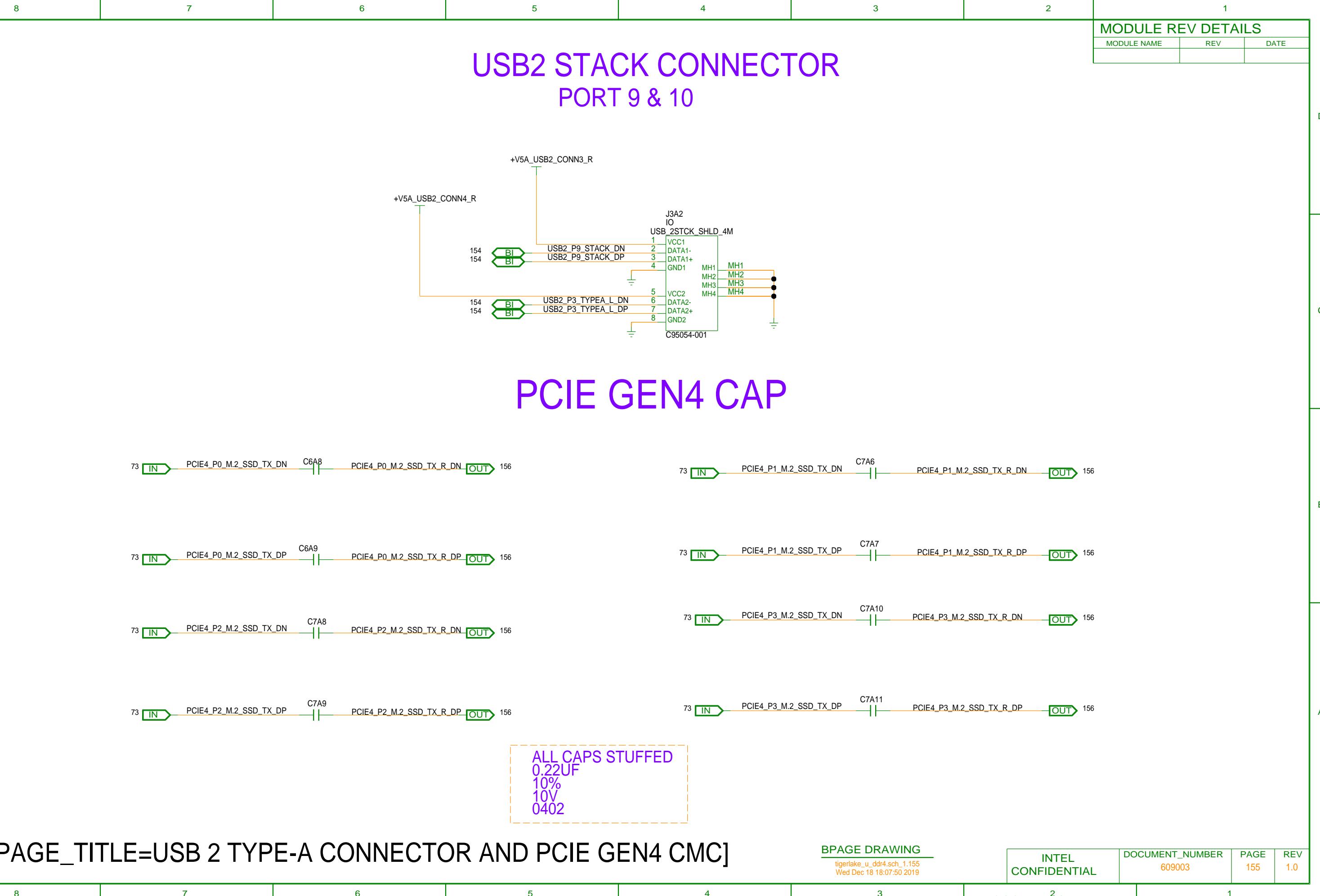
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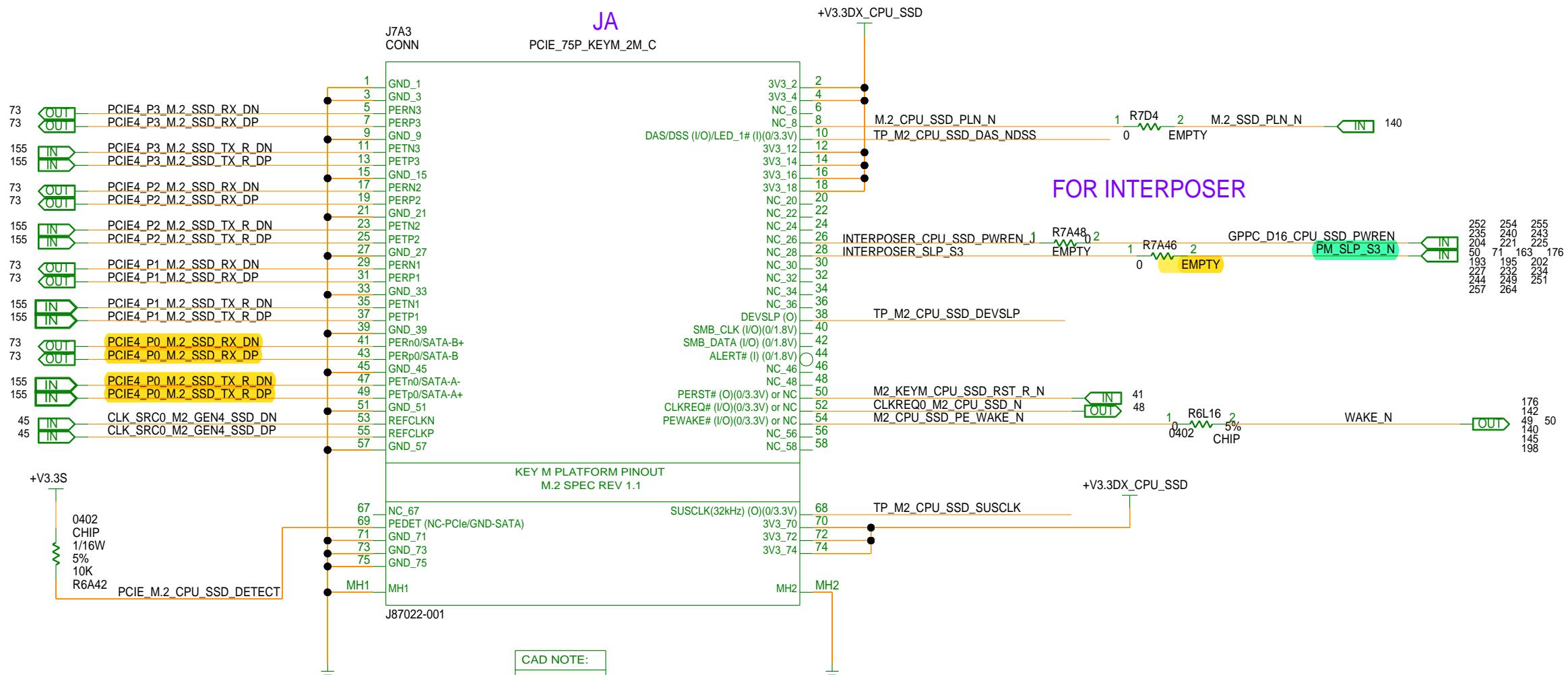


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PCIE GEN4 SSD

MODULE REV DETAILS

MODULE NAME	REV	DATE



CAD NOTE:
KEEP K0Z AS 2280 FOR M.2 KEY-M CONNECTOR

CAD NOTE:
KEEP STANOFF AT 2242 MODULE DIMENSION

RM6N1
EMPTY

STANOFF
MH1

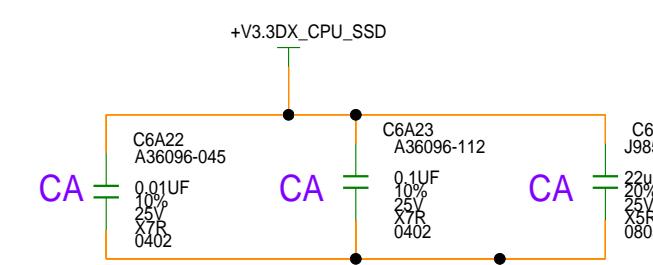
G75861-001

RM6D1
IC

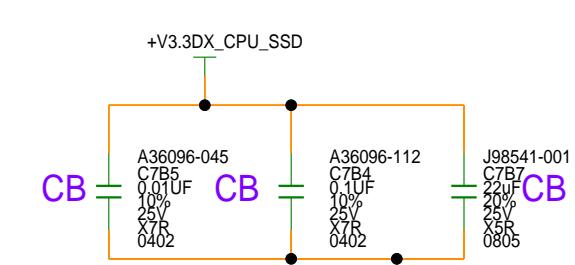
STANOFF
MH1

G75861-001

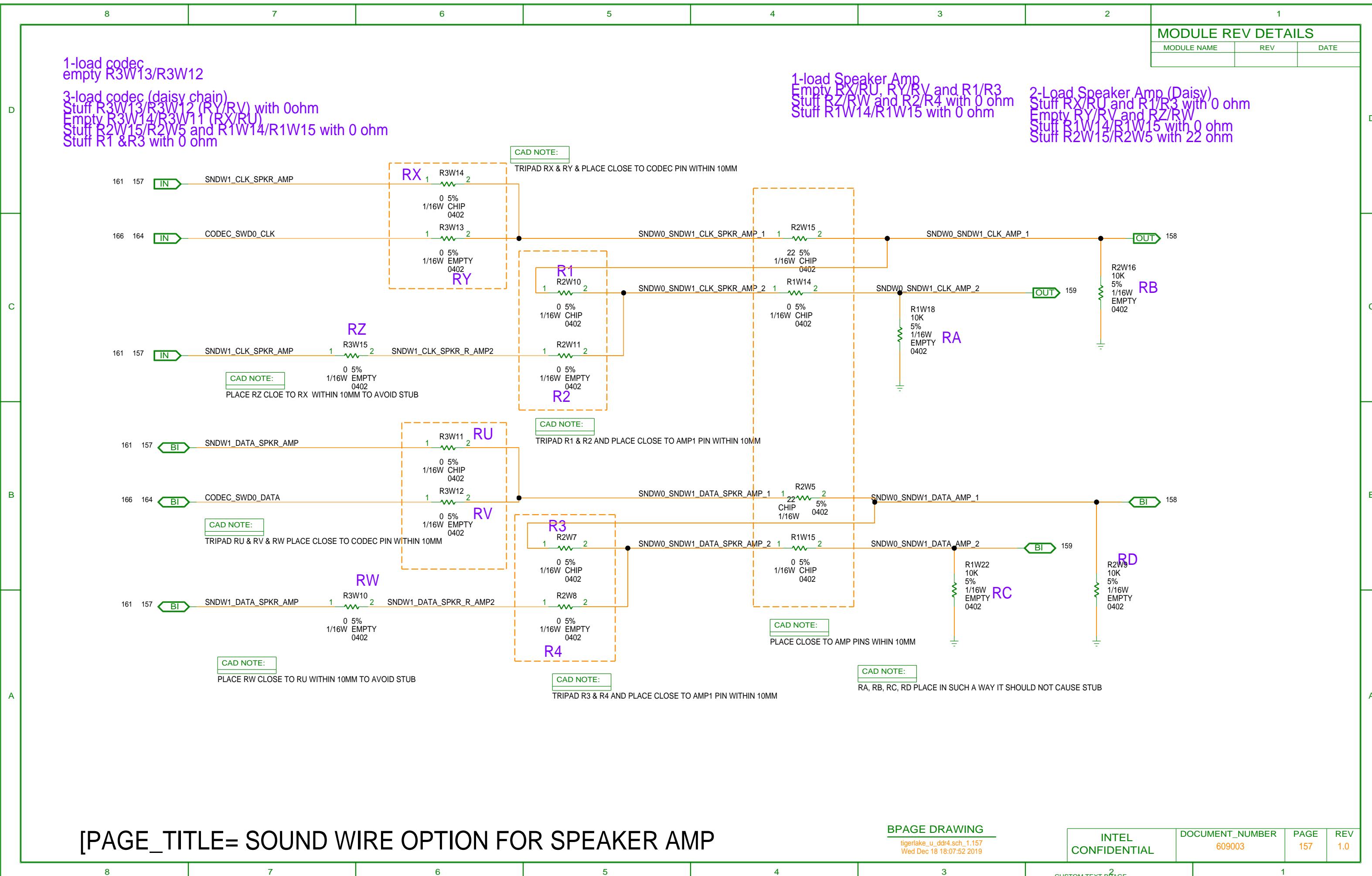
CAD NOTE:
KEEP K0Z AS 2280 FOR M.2 KEY-M CONNECTOR

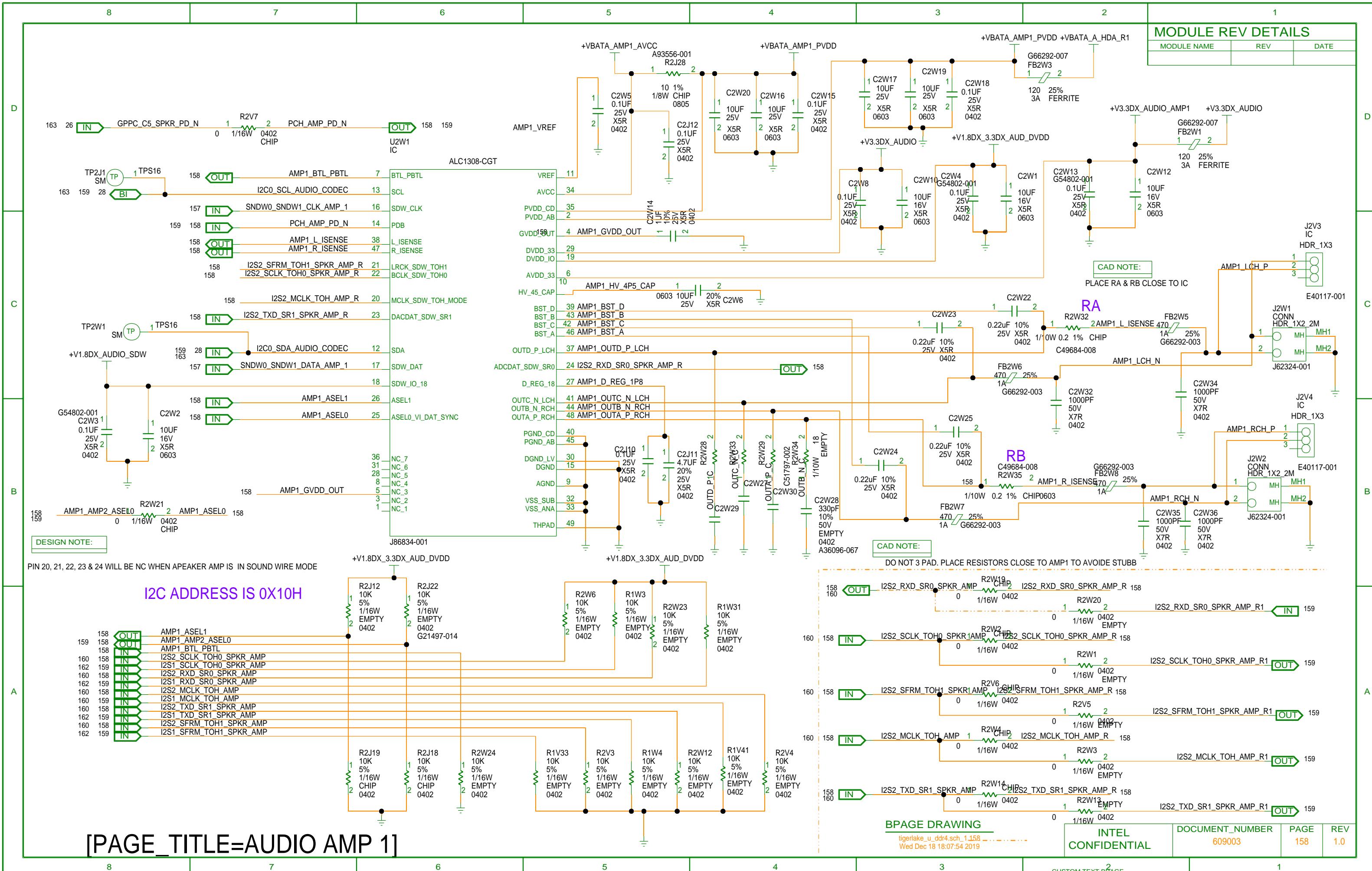


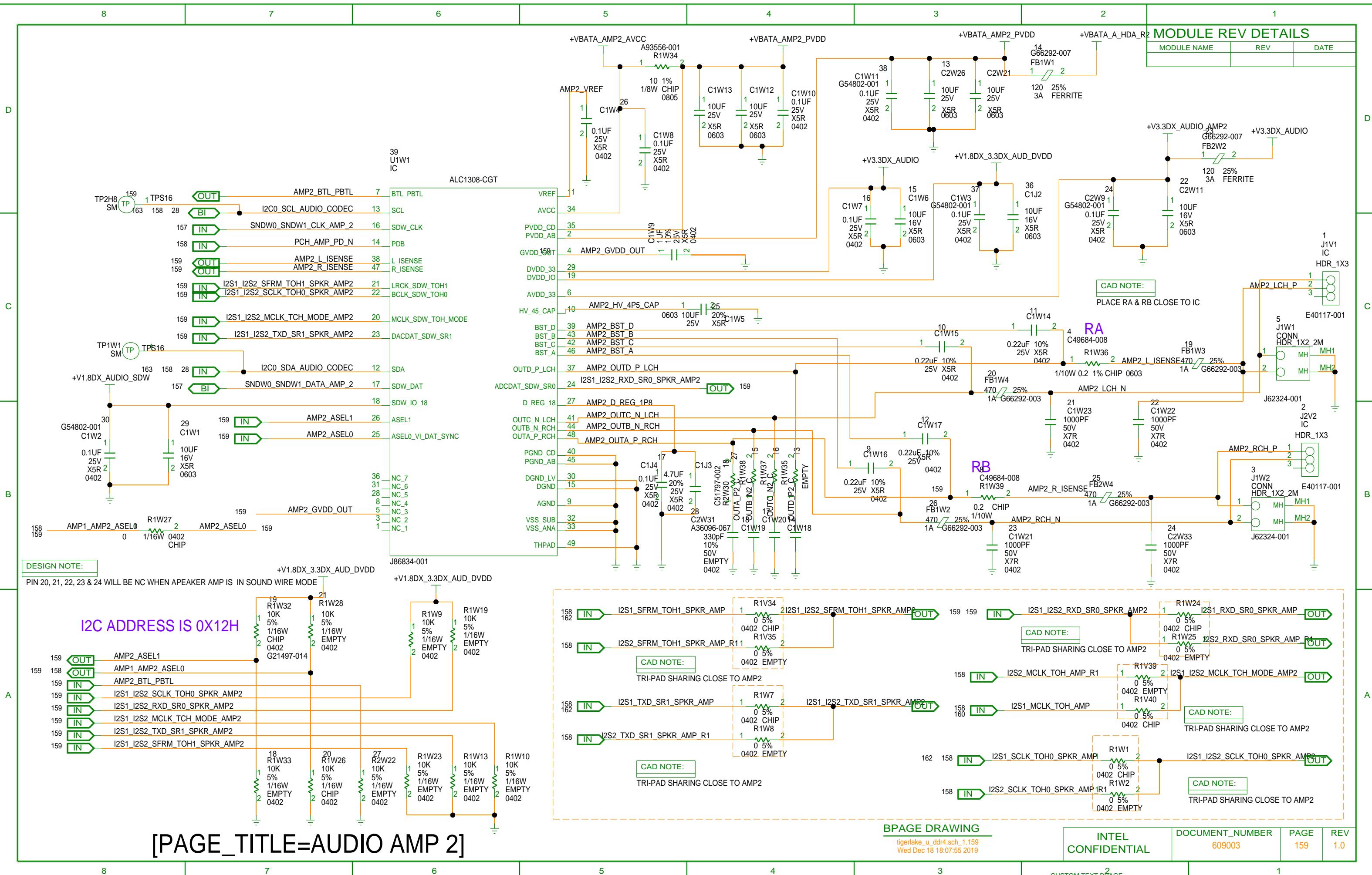
CAD NOTE:
PLACE CA CLOSE TO PINS 70, 72, 74 OF JA

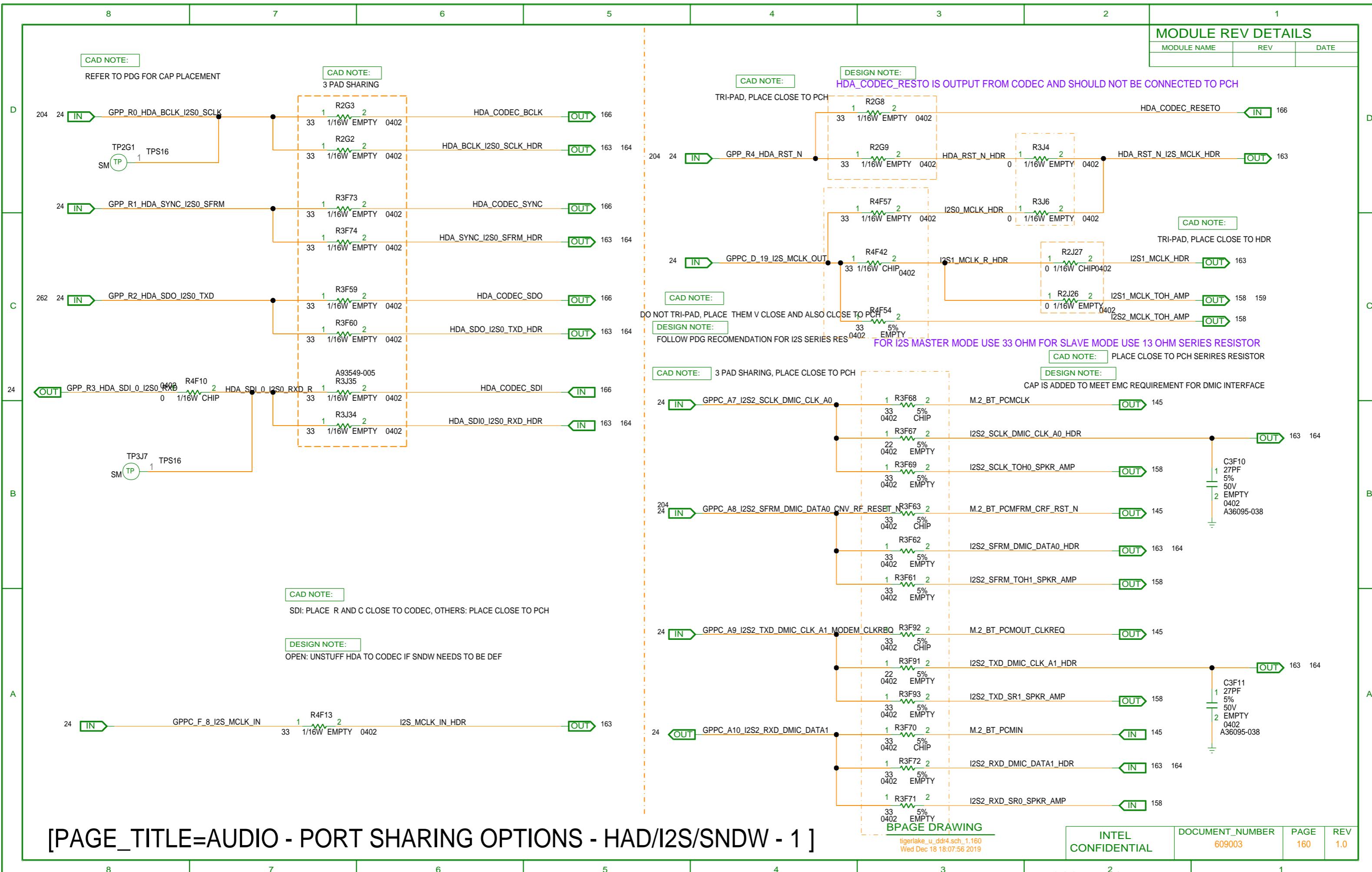


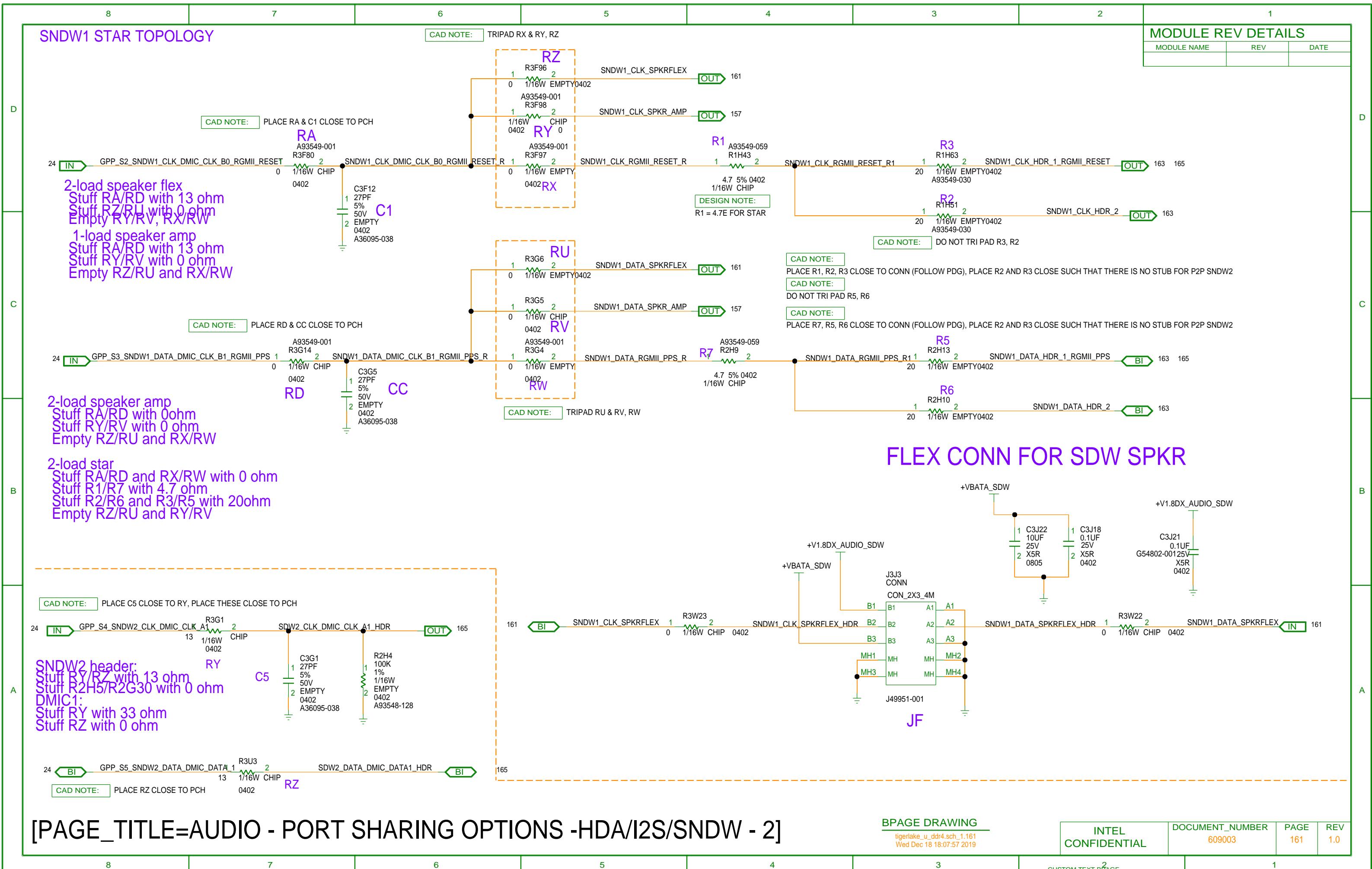
CAD NOTE:
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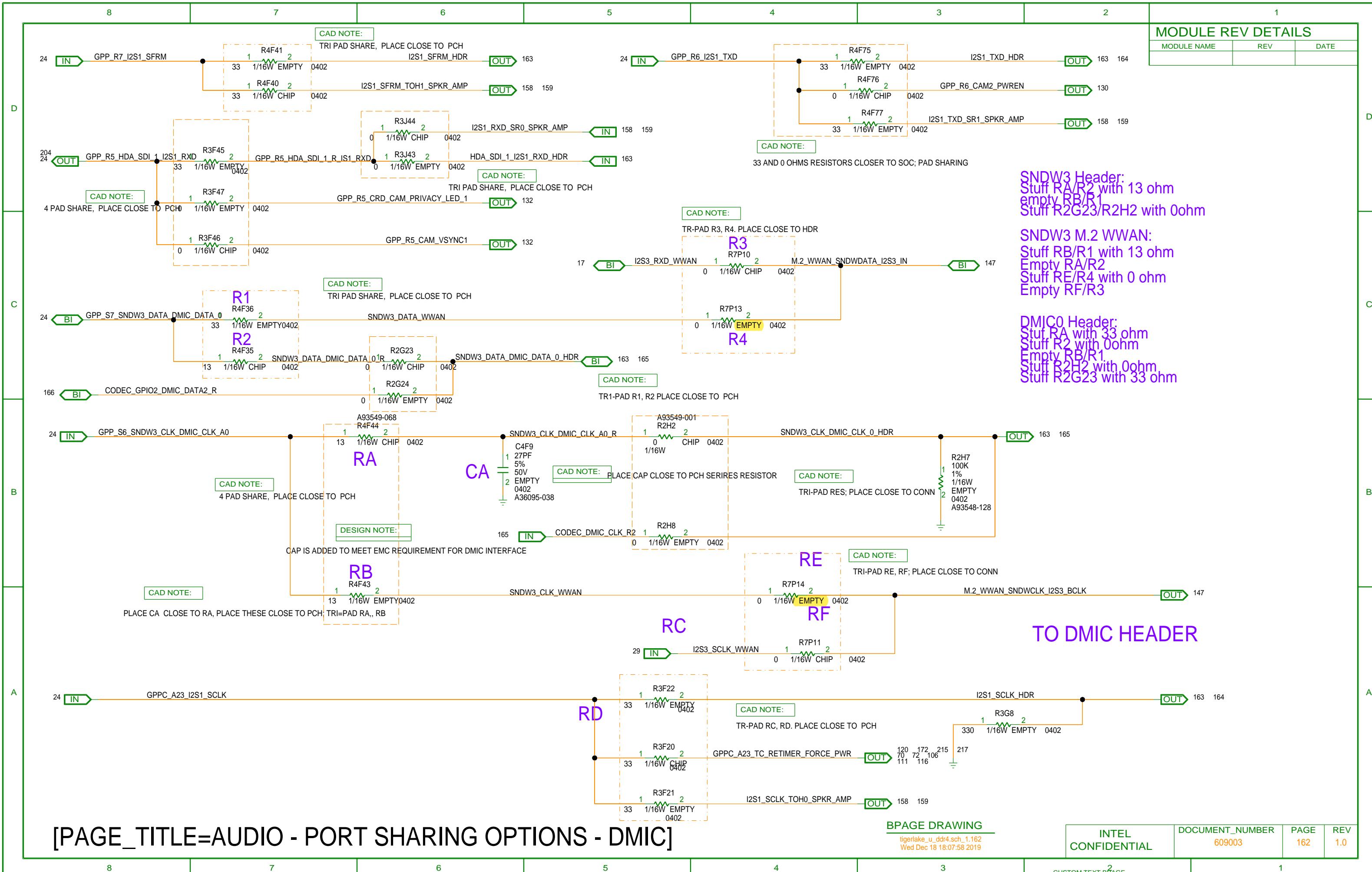


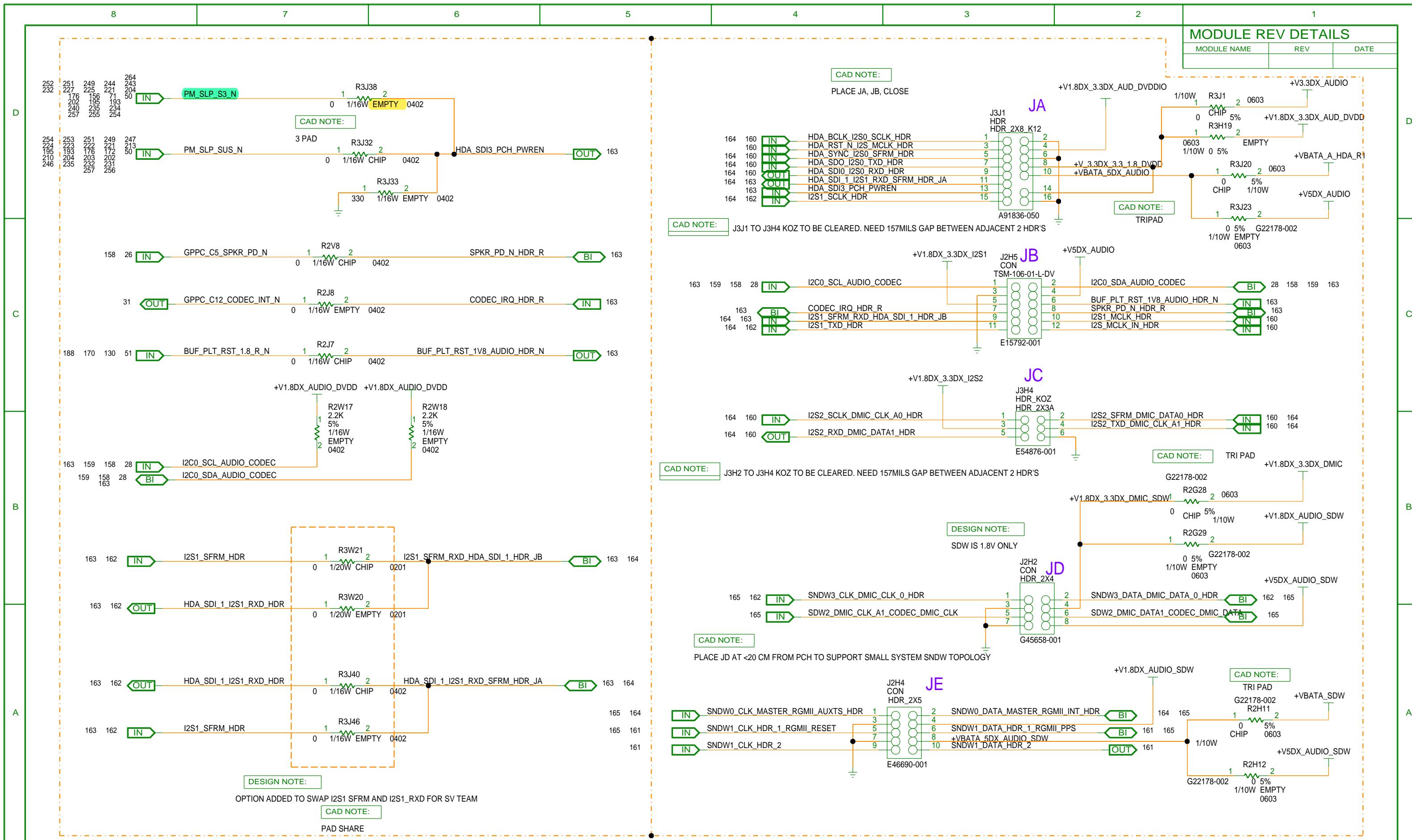








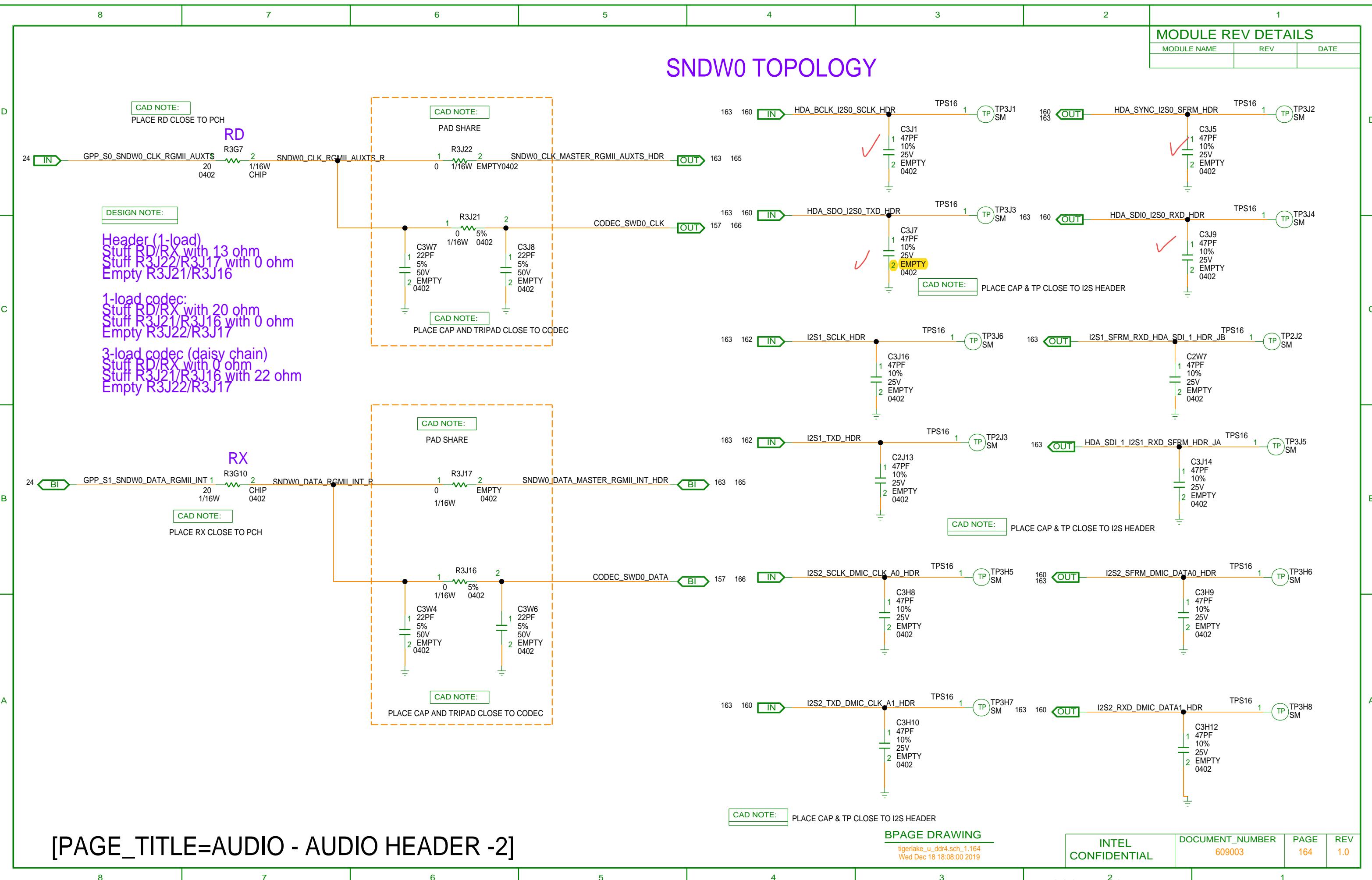


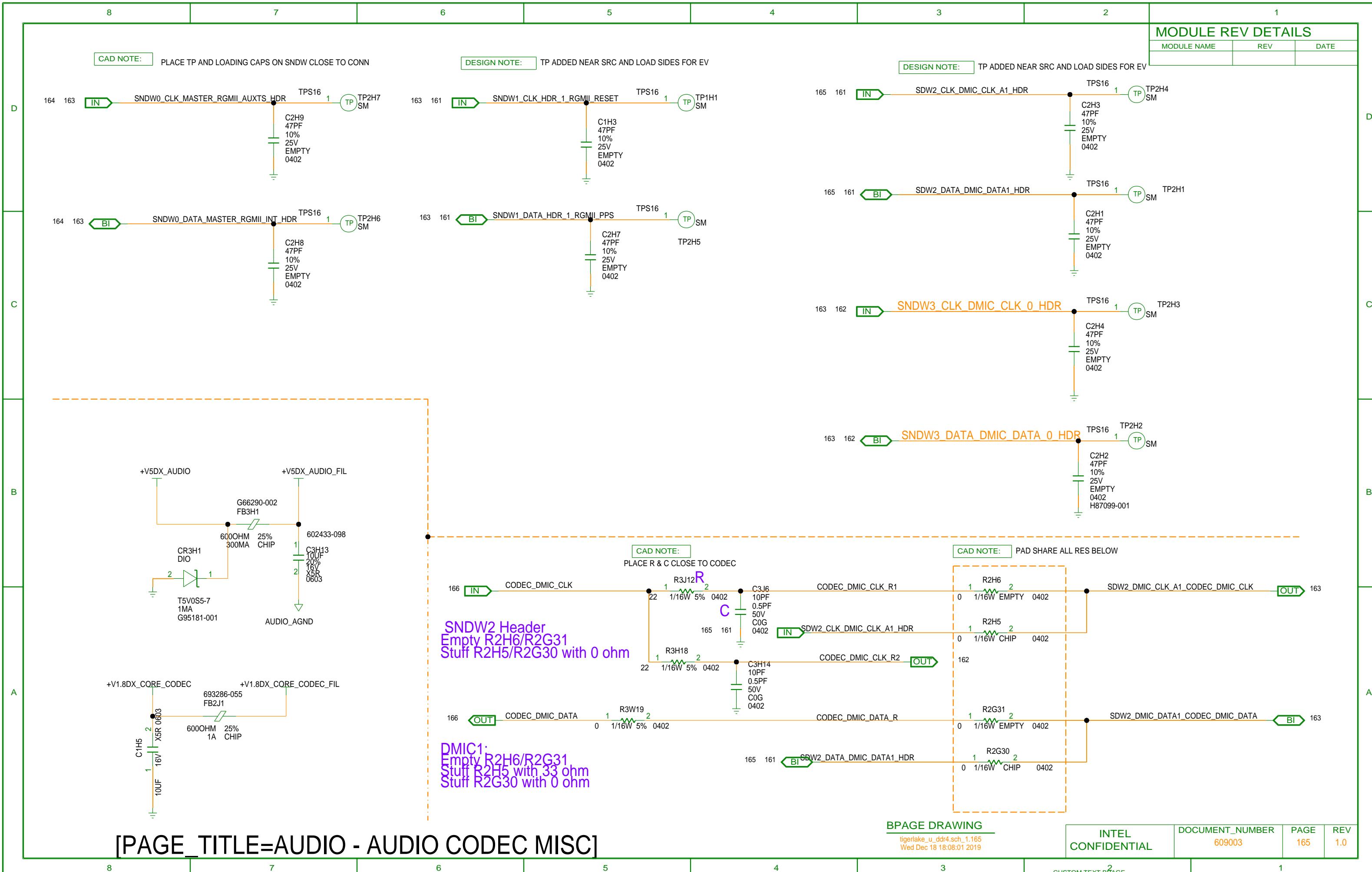


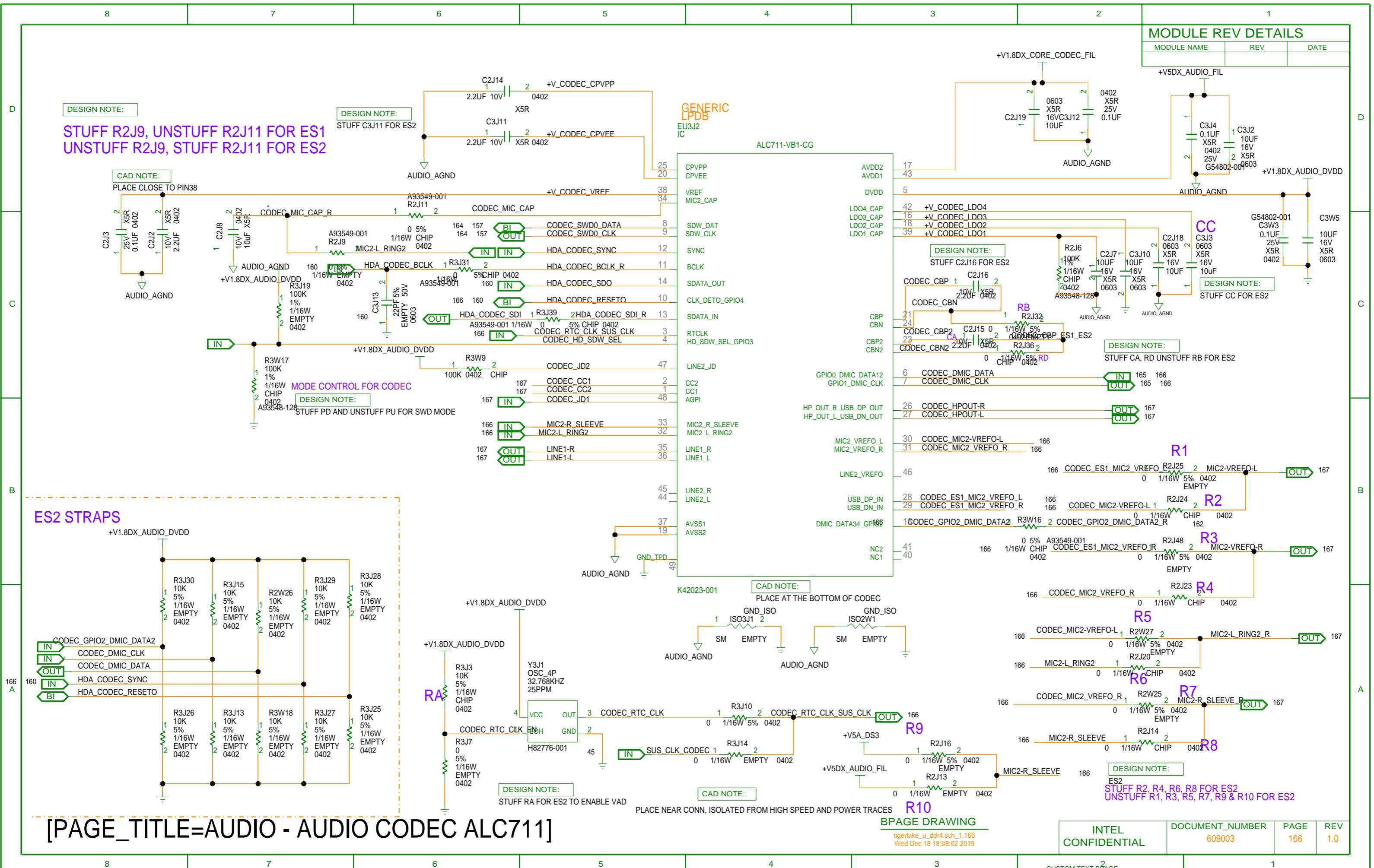
SNDW0 TOPOLOGY

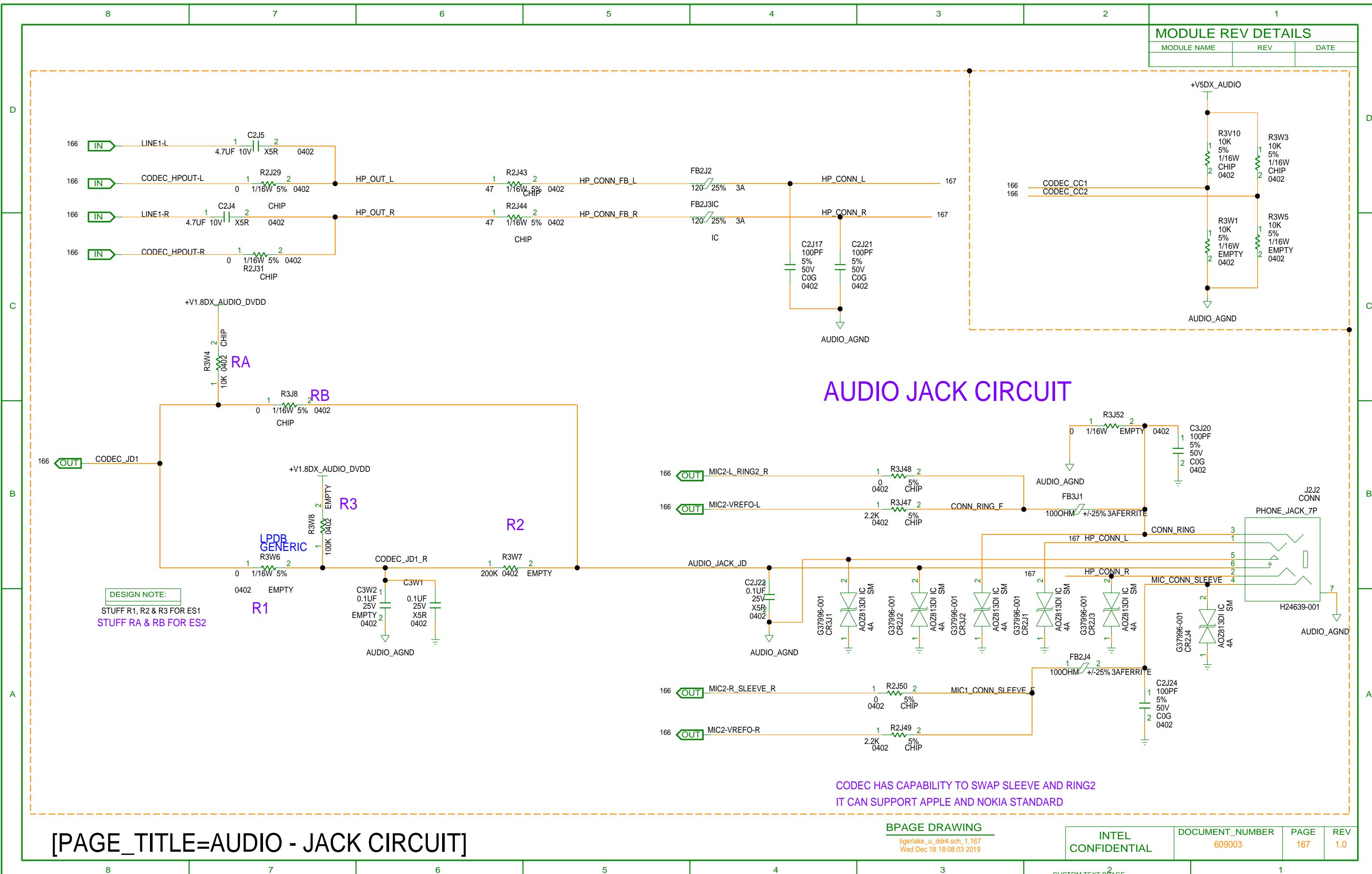
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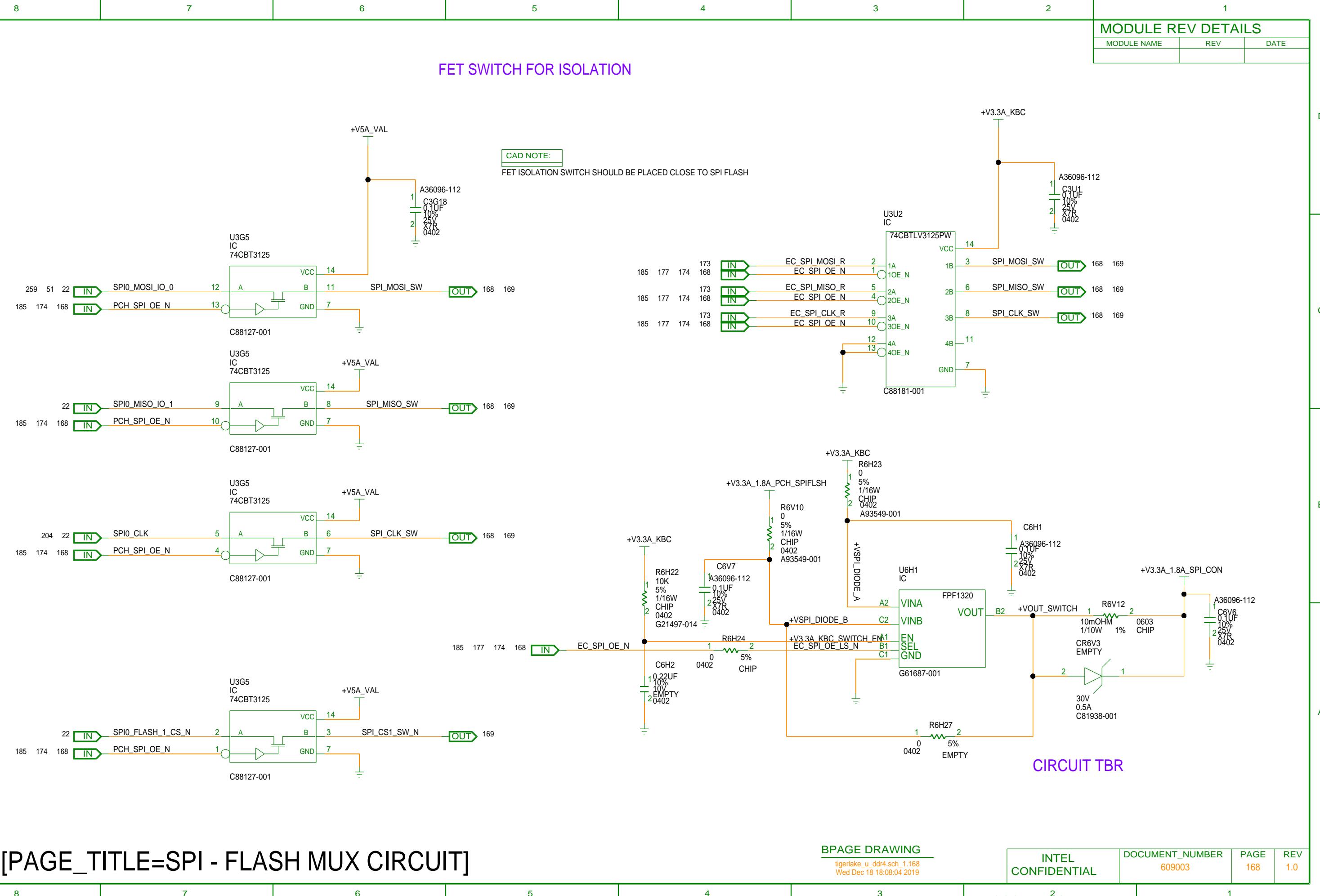
MODULE NAME	REV	DATE

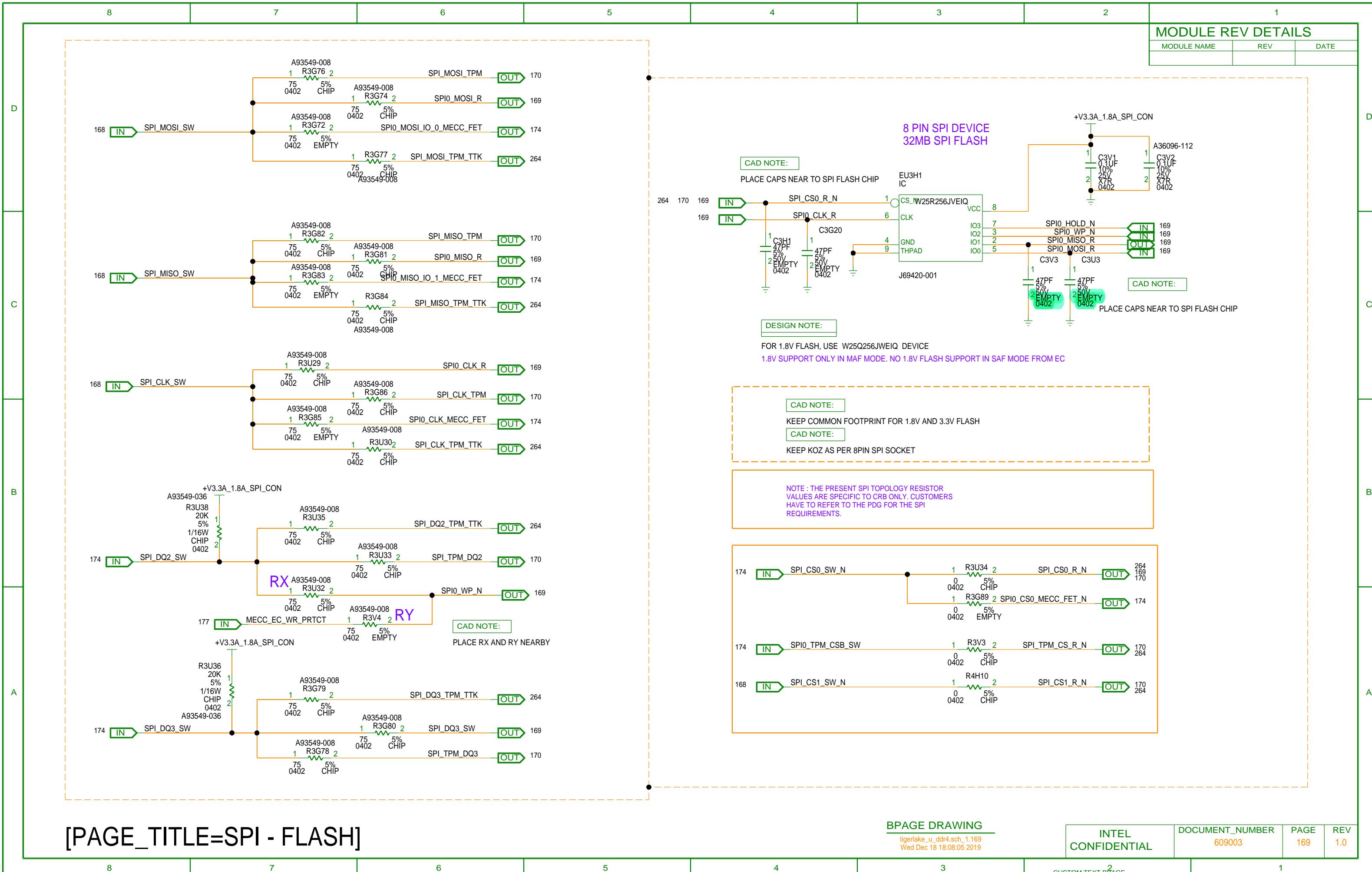












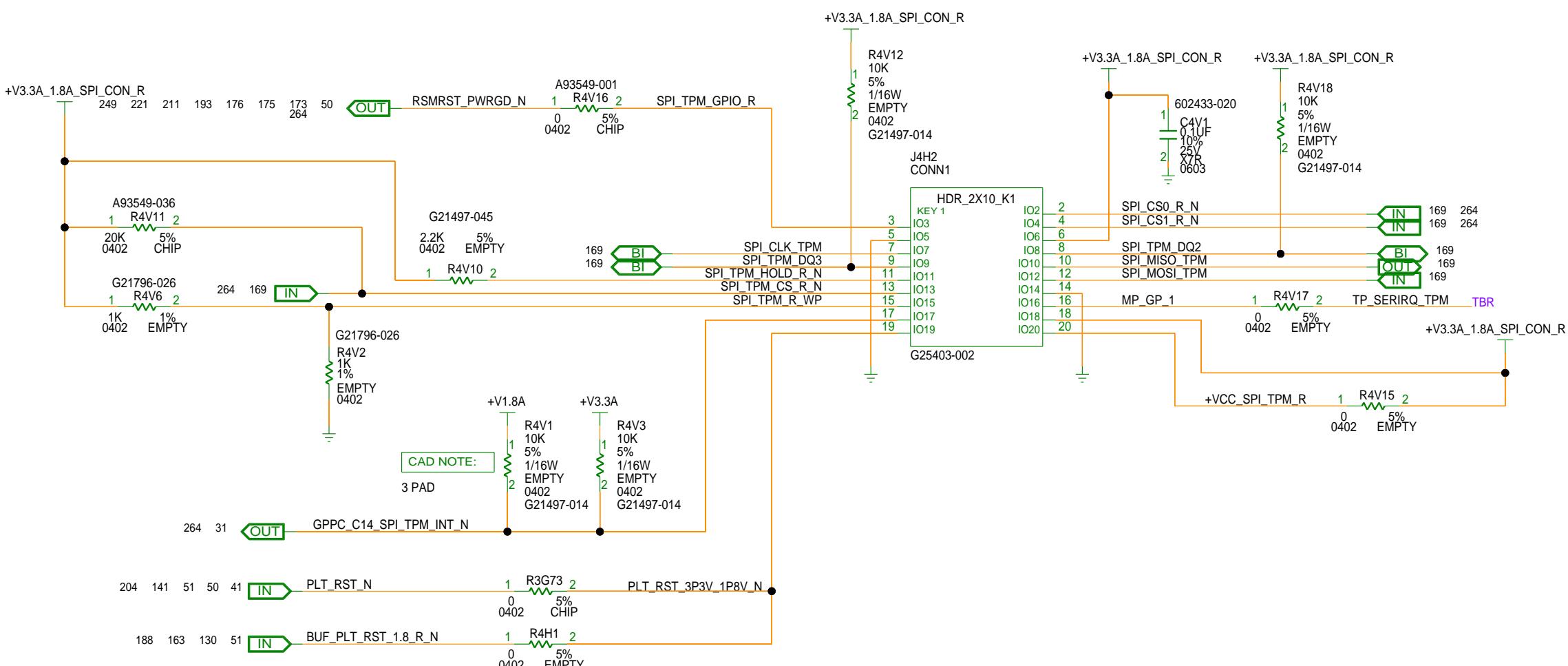
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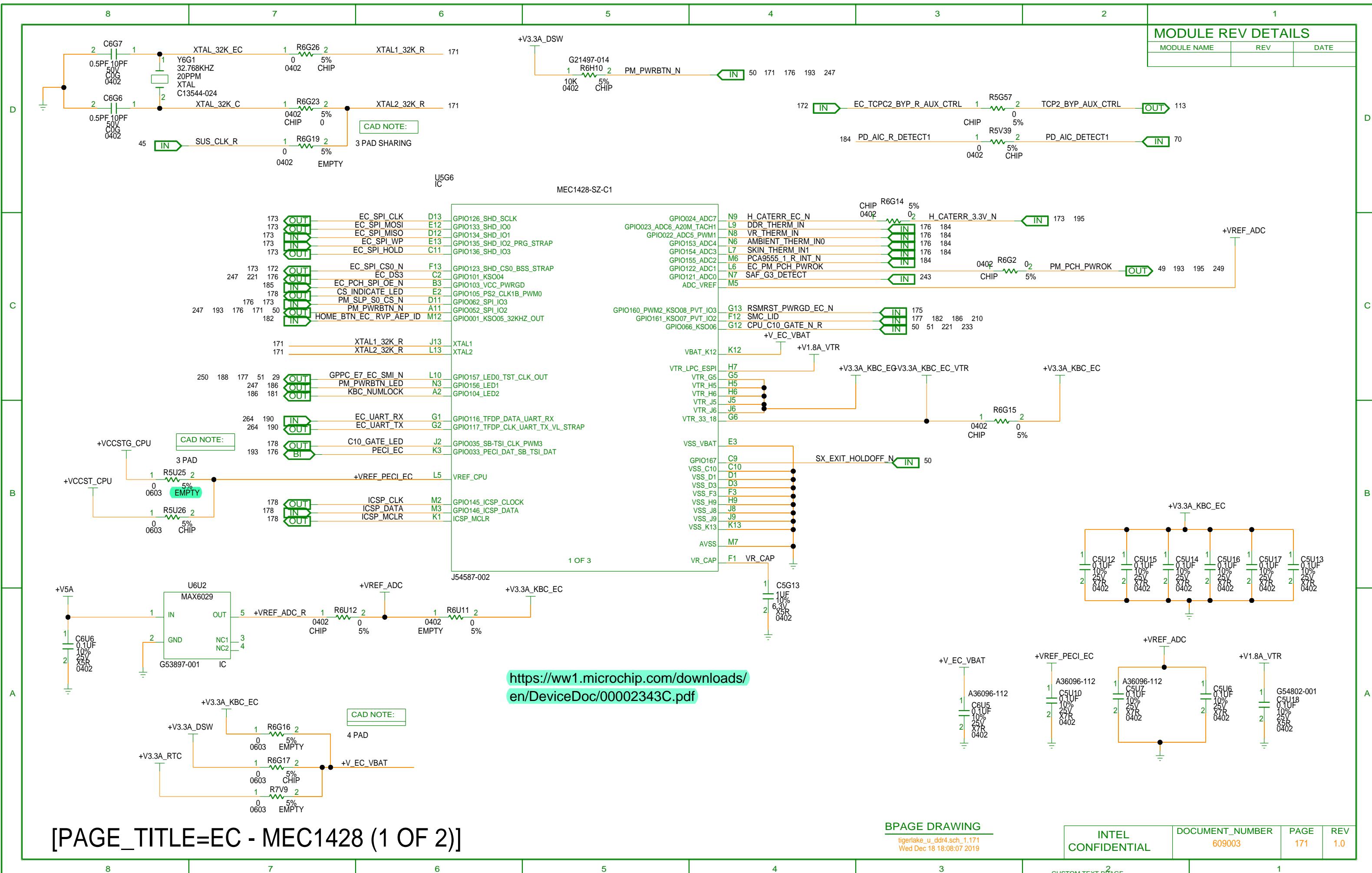
MODULE REV DETAILS		
MODULE NAME	REV	DATE

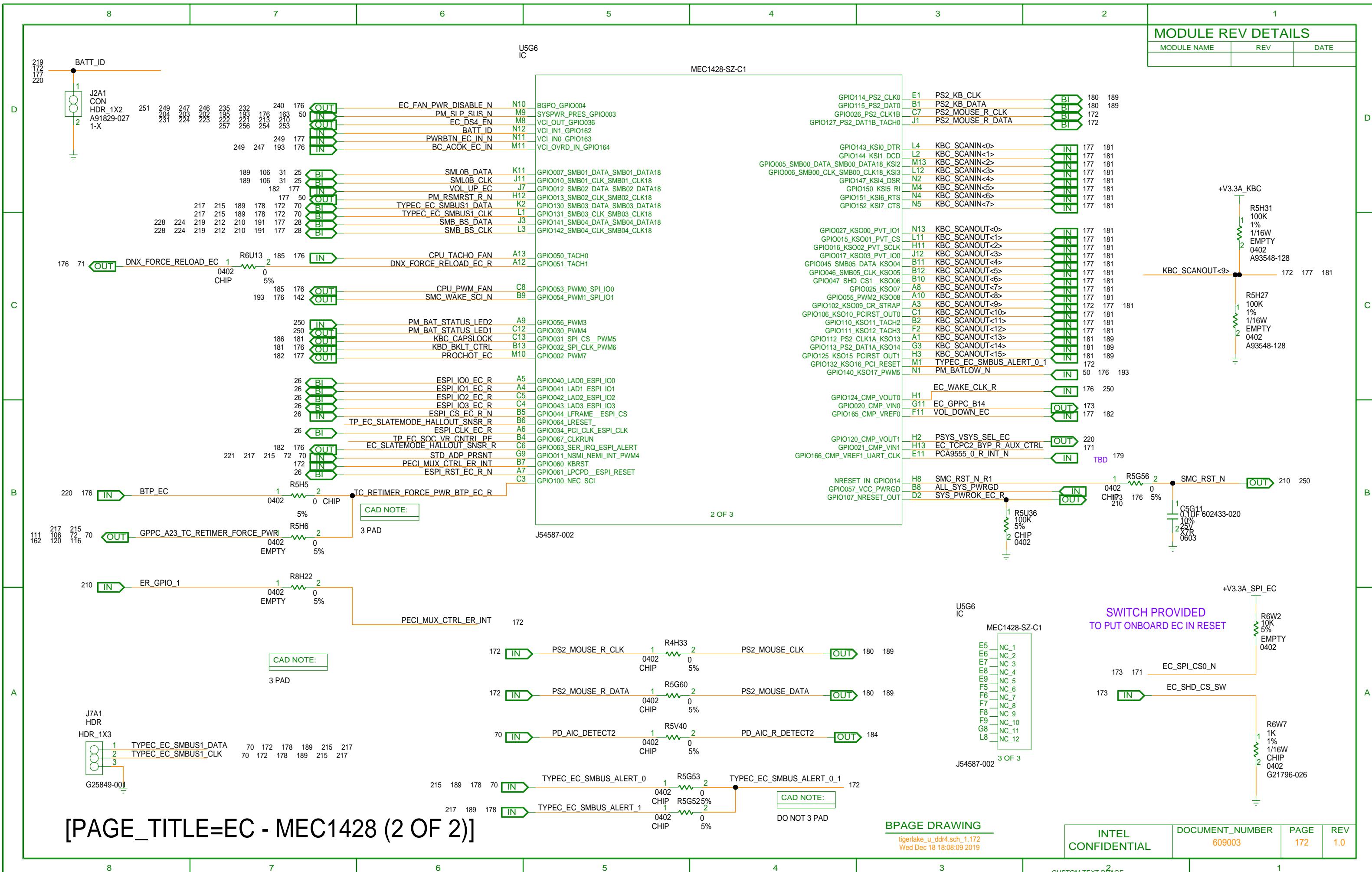
SF600 BASED SPI BASED TPM HEADER

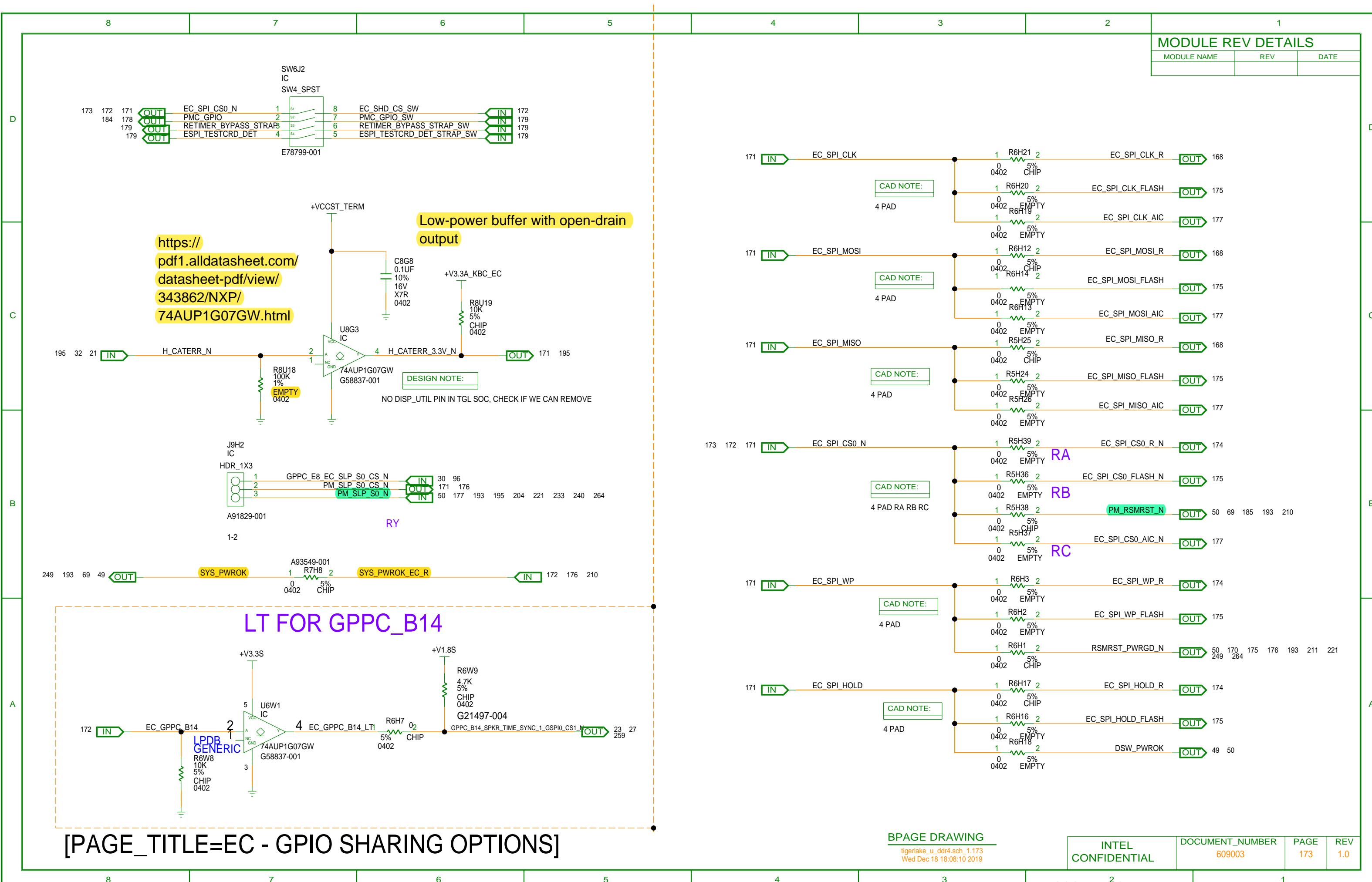
CAD NOTE:

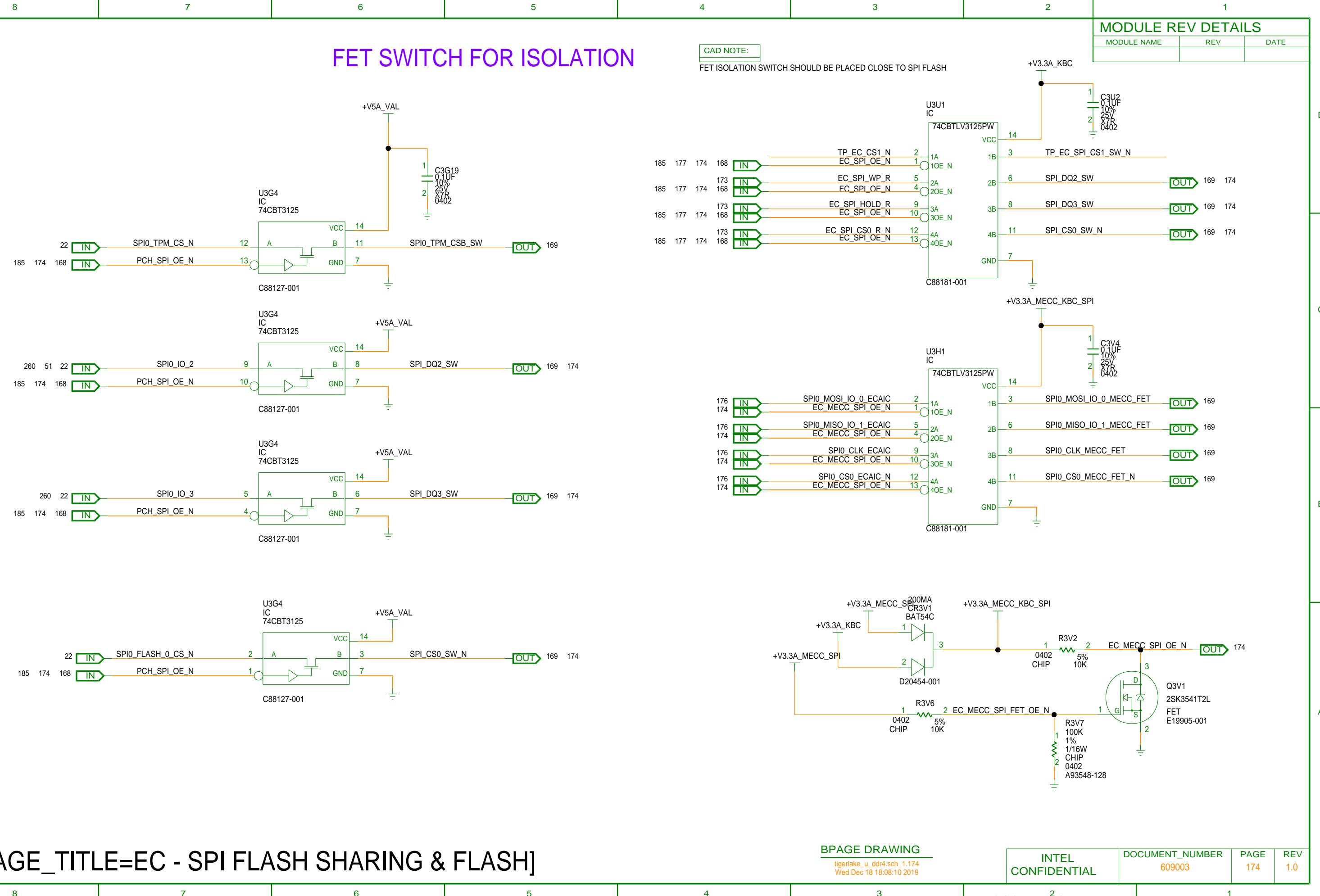
SPI0_FLASH_1_CS_N SIGNAL TO BE ROUTED 1.5 INCH MORE LENGTH THAN OTHER SPI0 SIGNALS





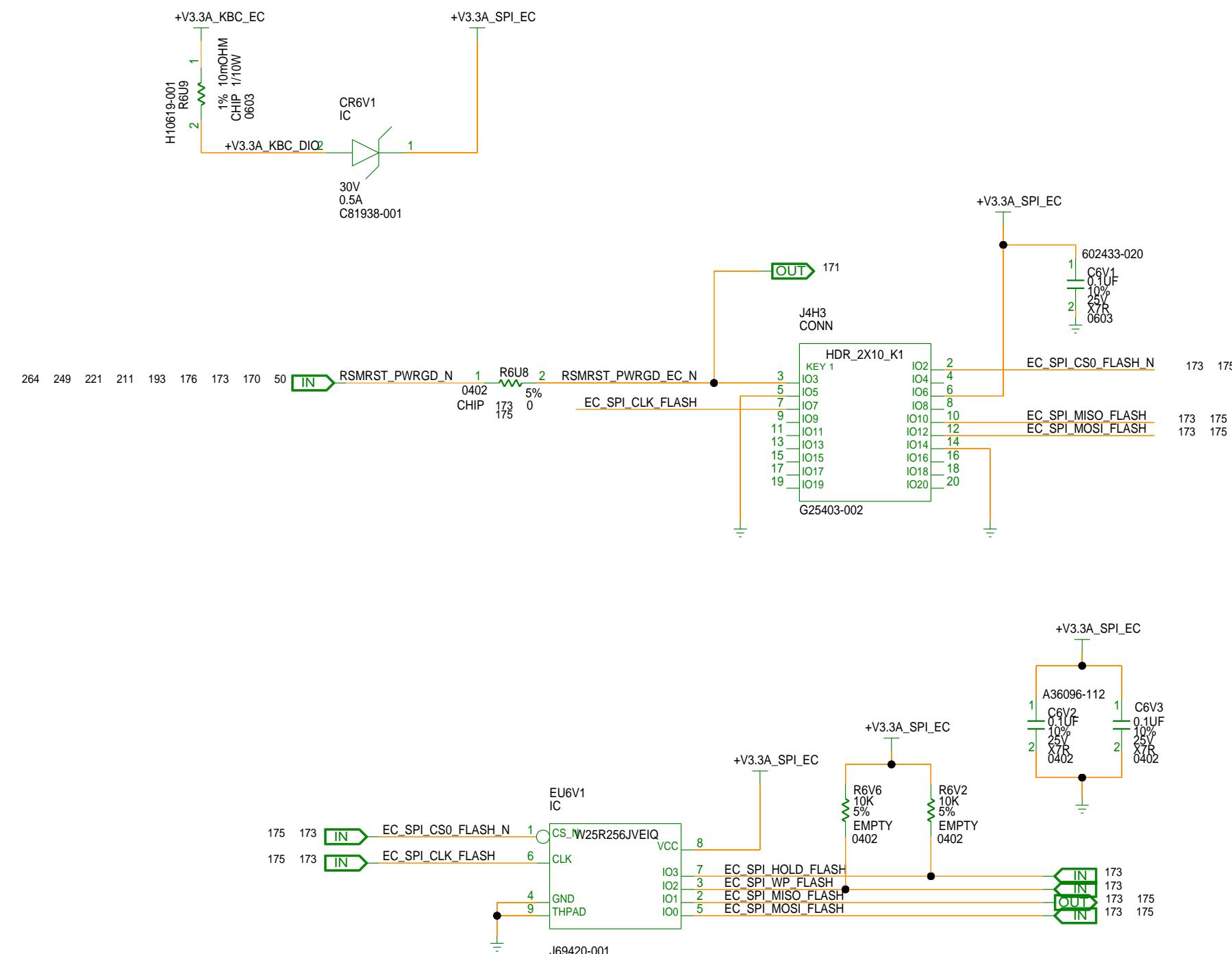






SF600 BASED TPM HEADER (DEDICATED FOR EC)

MODULE REV DETAILS		
MODULE NAME	REV	DATE

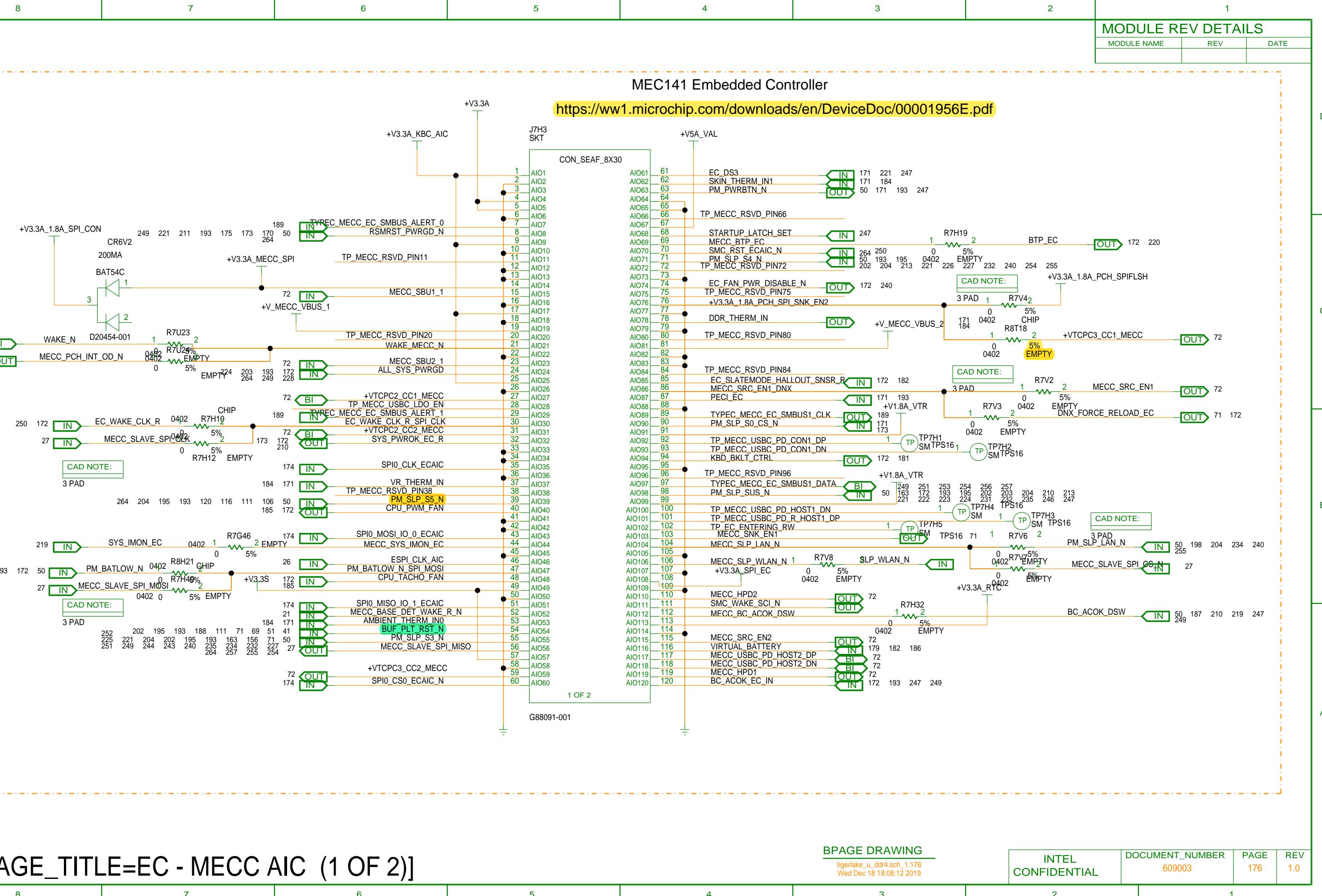


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Wed Dec 18 18:08:11 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 175	REV 1.0
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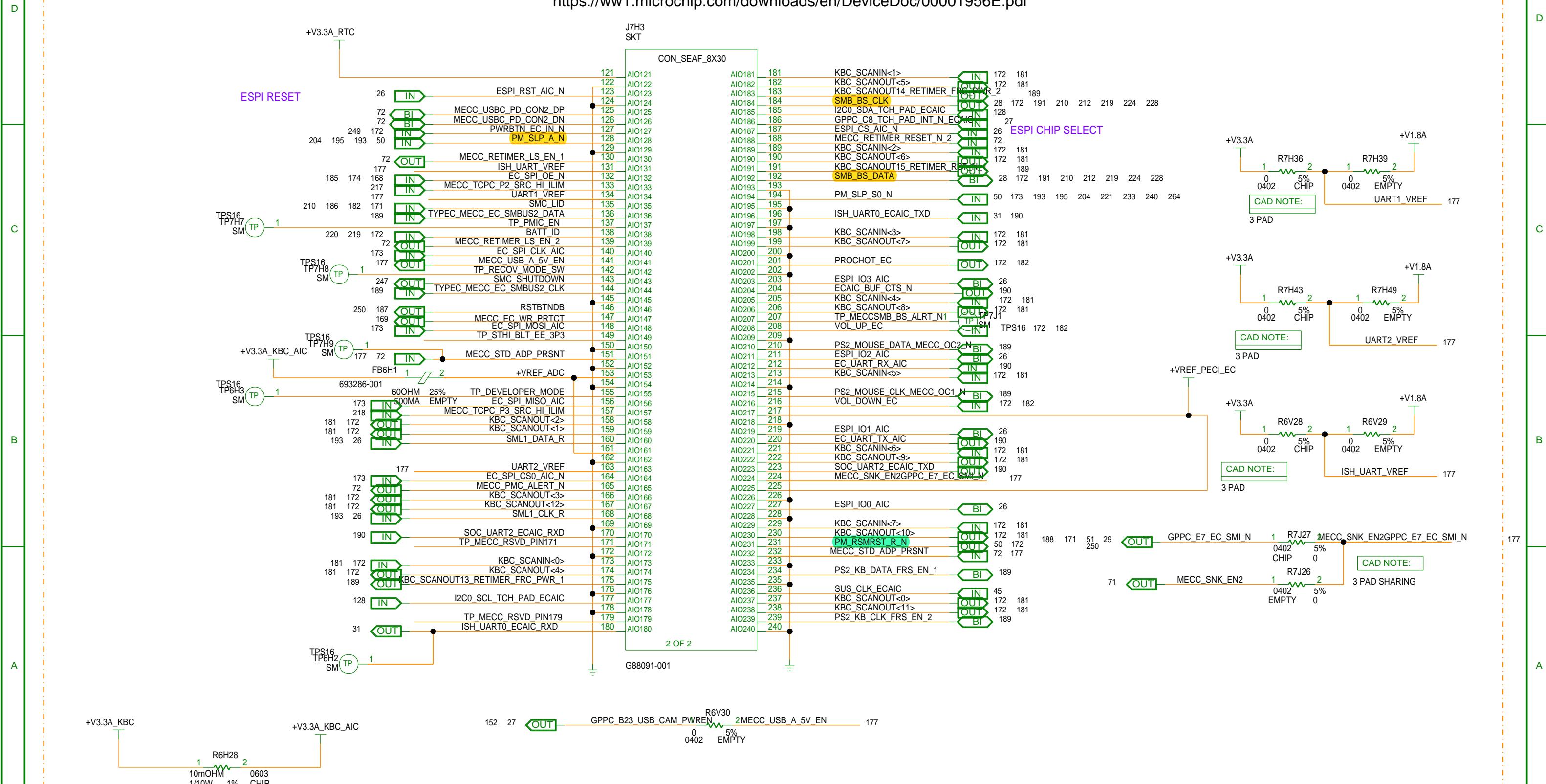
MEC140x/1x embedded

controller

<https://ww1.microchip.com/downloads/en/DeviceDoc/00001956E.pdf>

MODULE REV DETAILS

MODULE NAME	REV	DATE



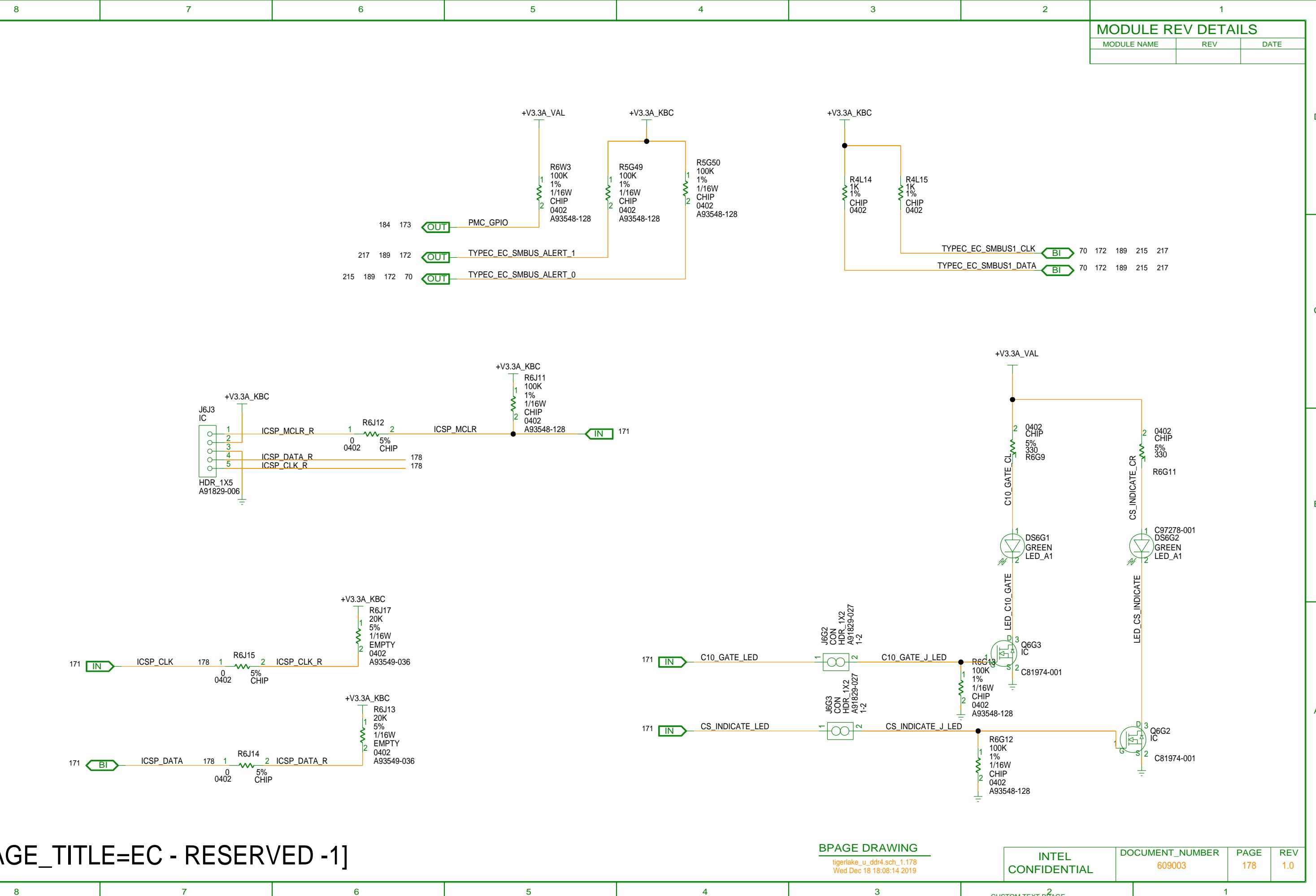
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 178	REV 1.0
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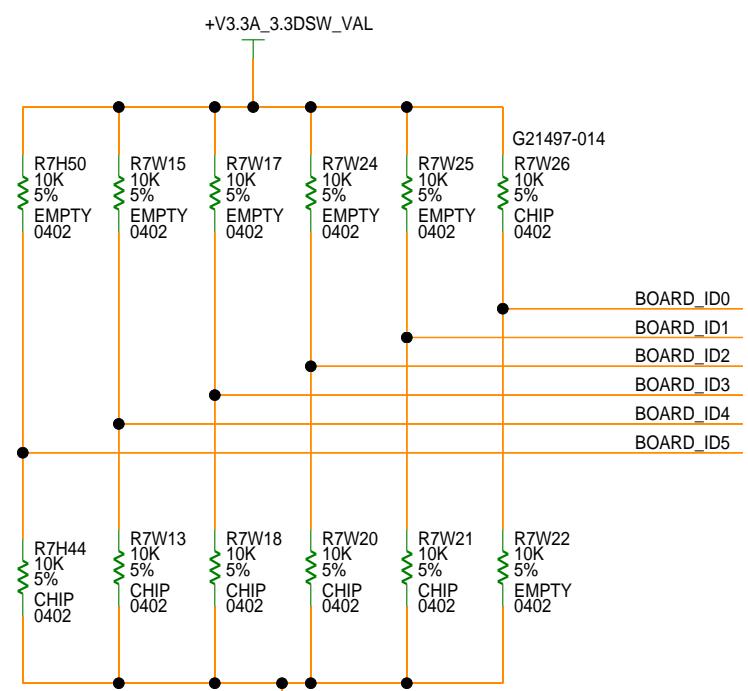
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BOARD ID ,FAB ID & I/O EXPANDER

MODULE REV DETAILS

MODULE NAME	REV	DATE

BOARD REVISION



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R7V21 10K 5% EMPTY 0402

R7V20 10K 5% CHIP 0402

R7W6 10K 5% EMPTY 0402

BRD_ID_A0

BRD_ID_A1

BRD_ID_A2

R7W1 10K 5% CHIP 0402

R7W2 10K 5% EMPTY 0402

R7W4 10K 5% CHIP 0402

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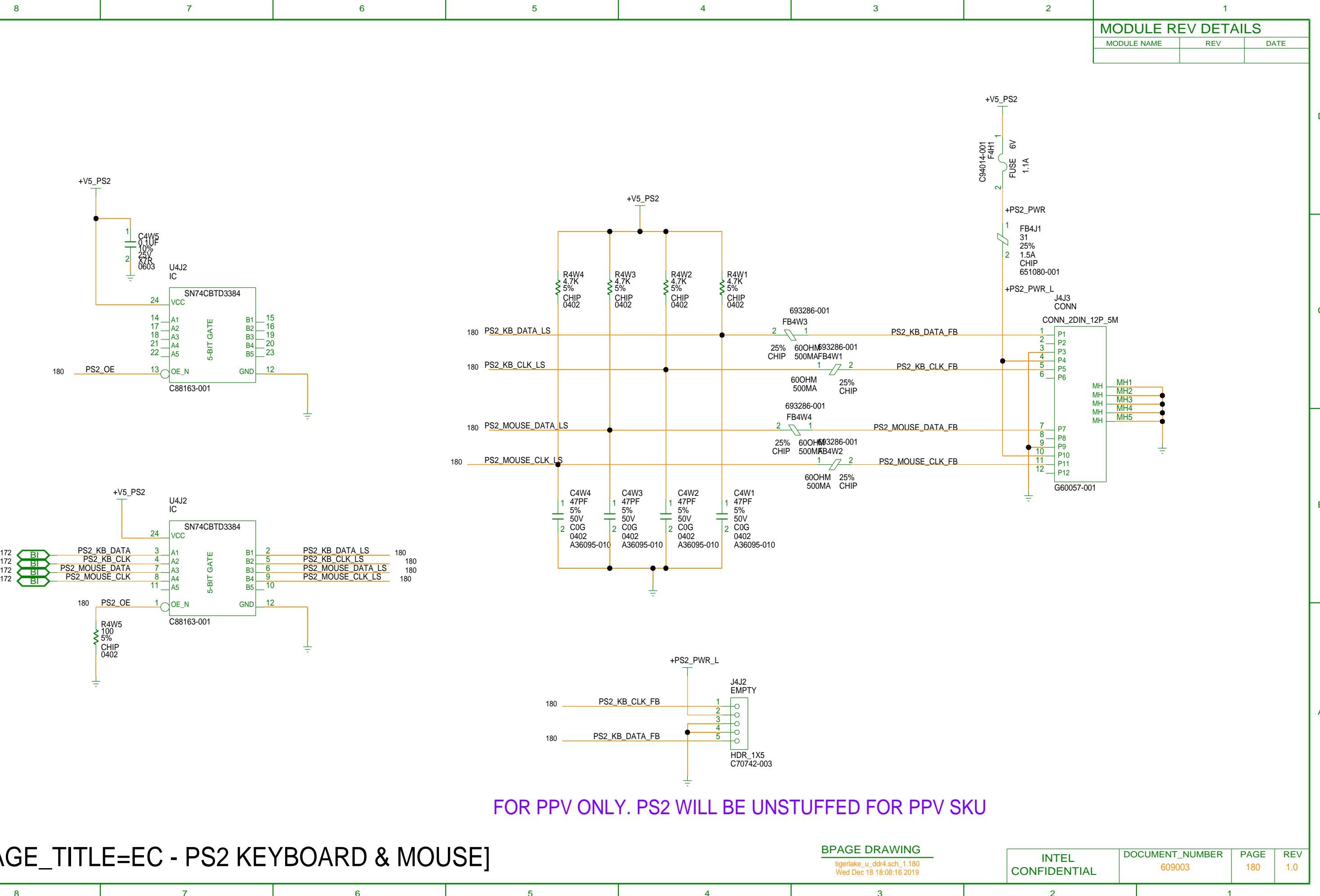
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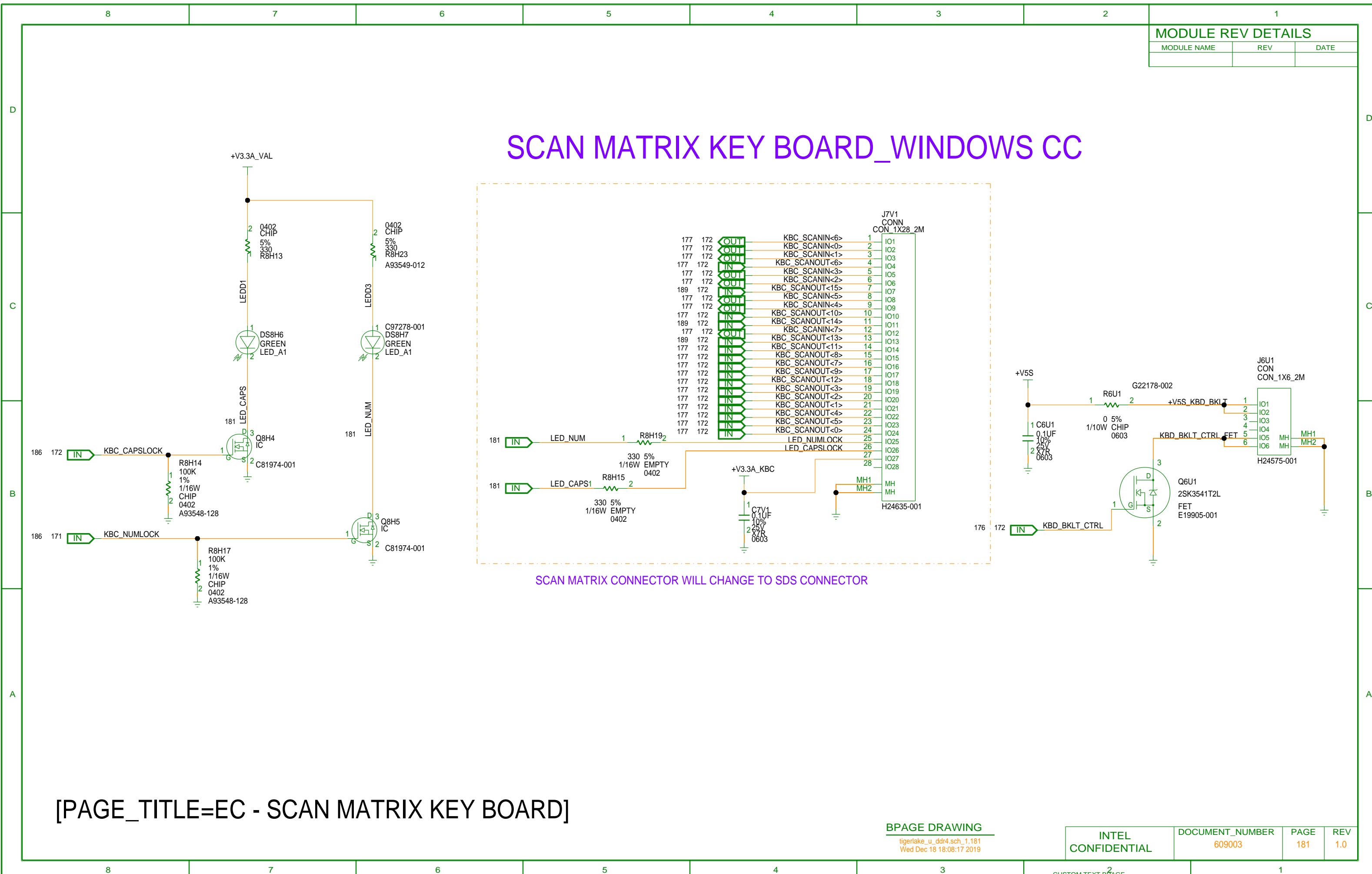
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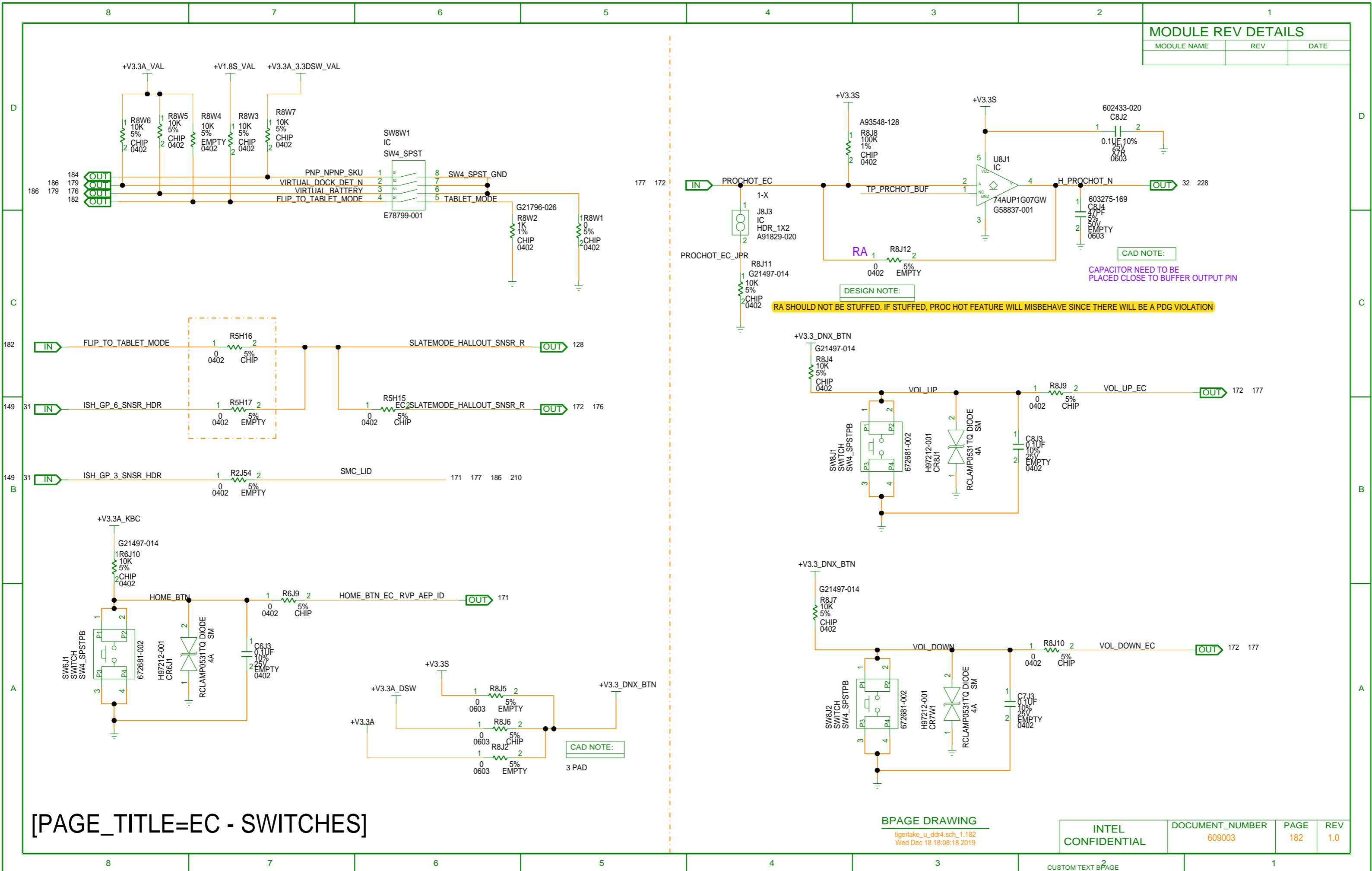
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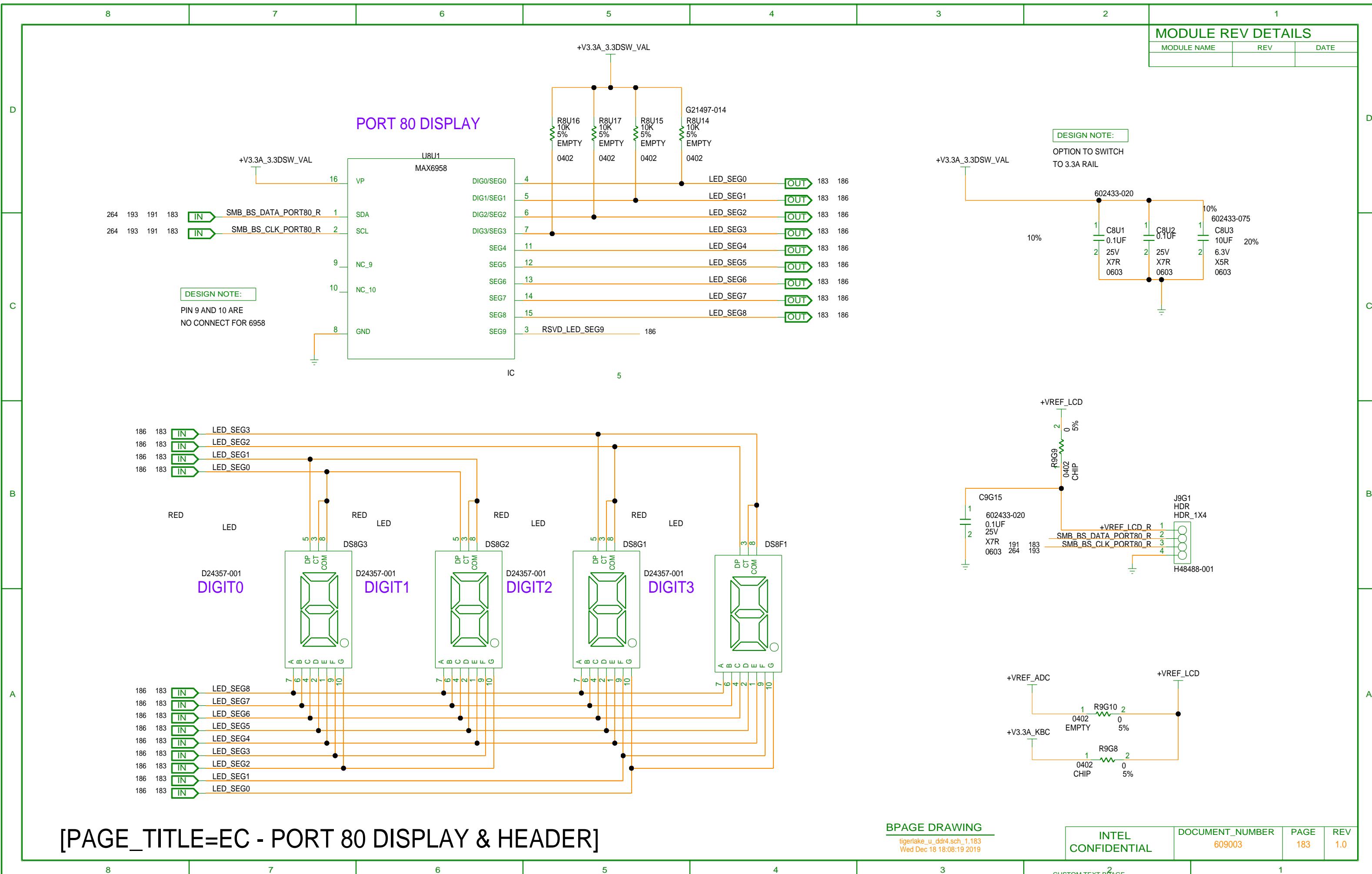
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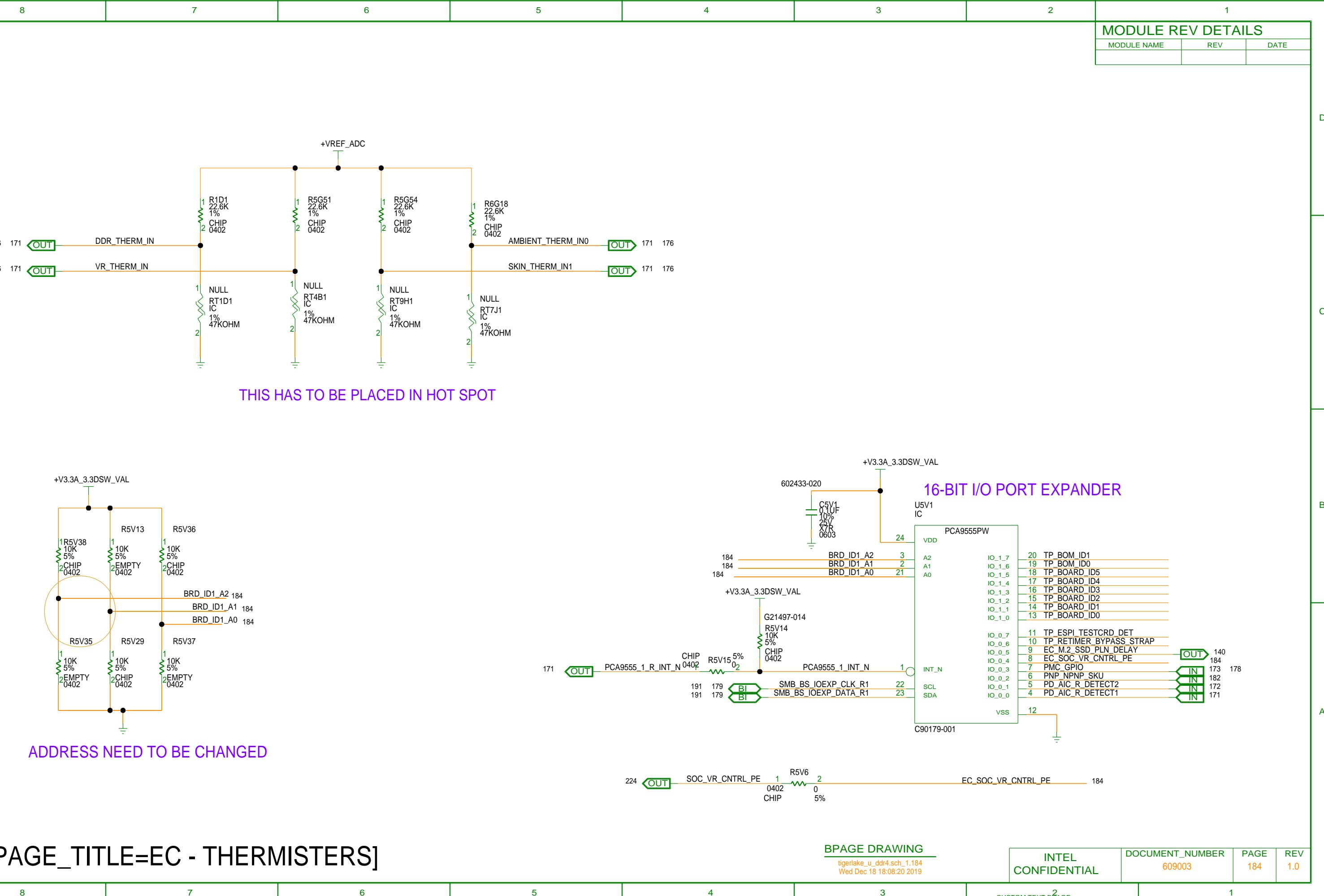
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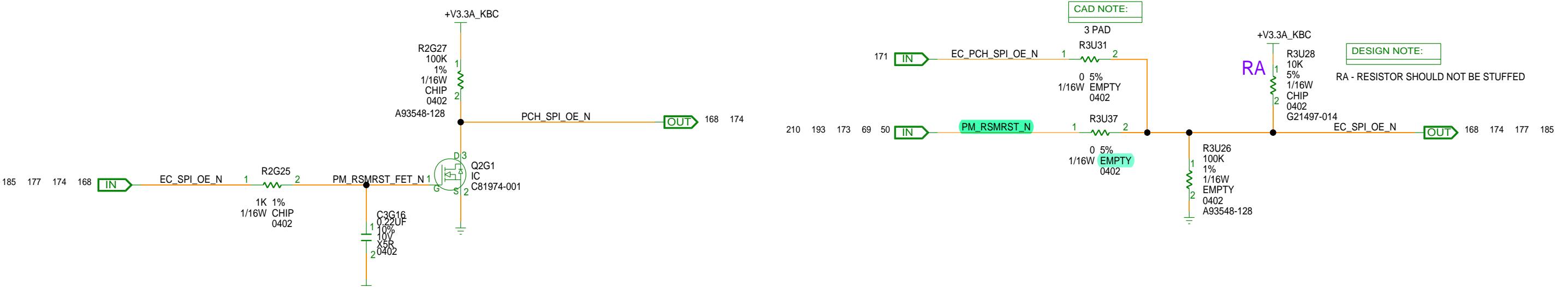
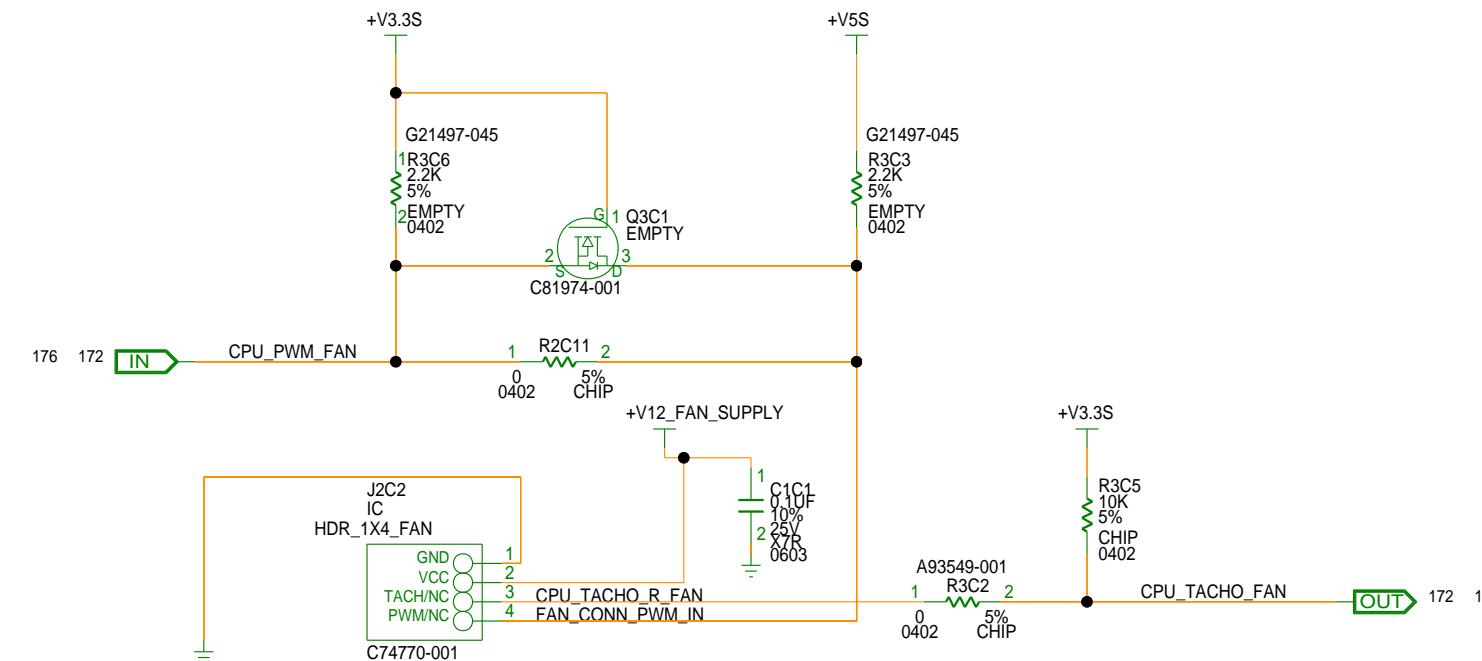




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MODULE REV DETAILS		
MODULE NAME	REV	DATE

PROCESSOR FAN CONTROL



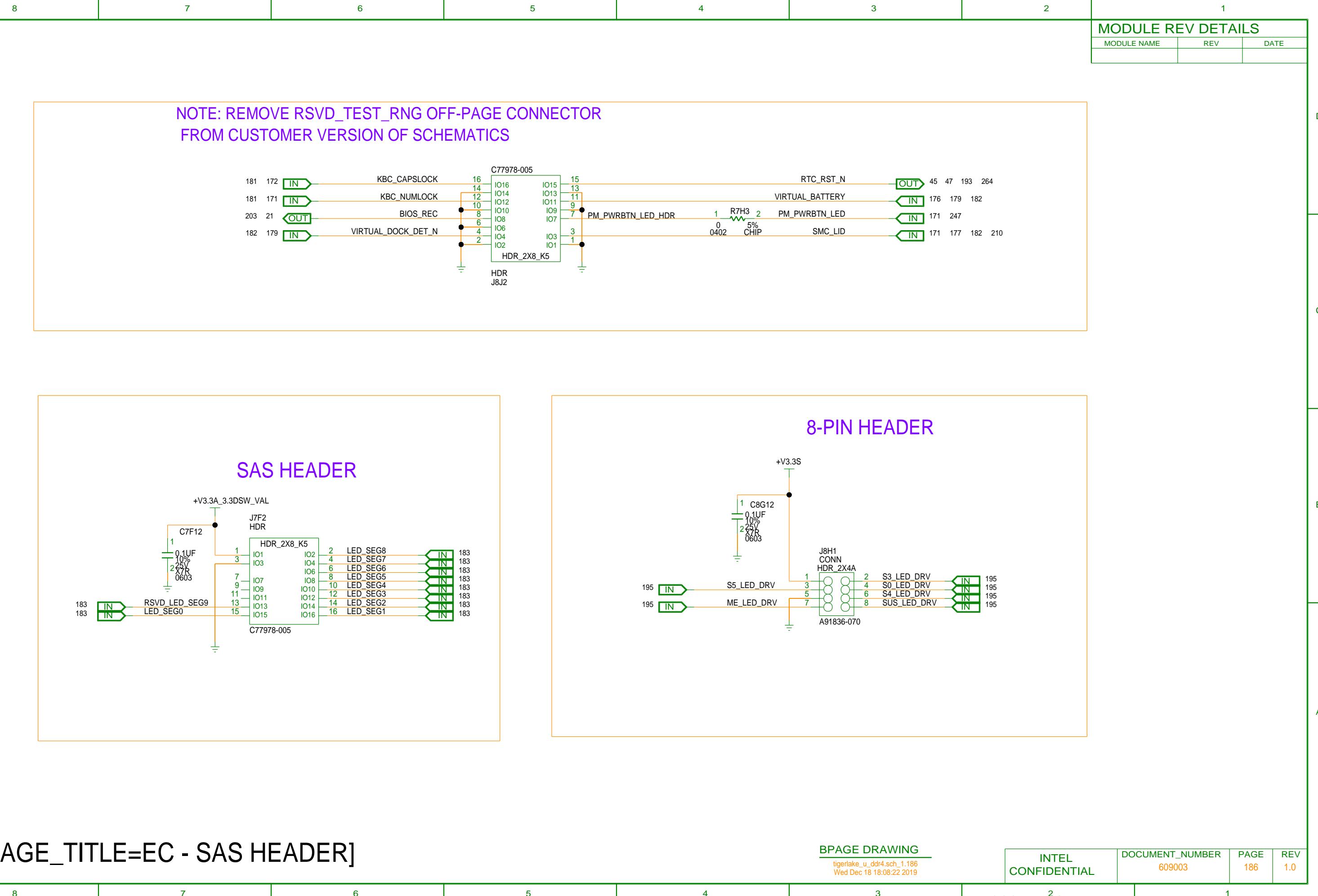
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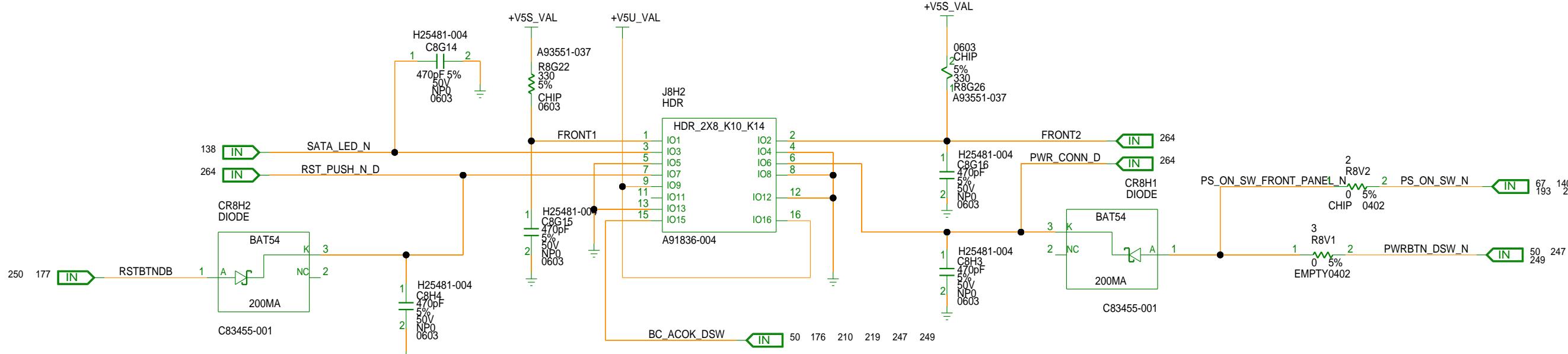
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8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME						REV	DATE

FRONT PANEL HEADER



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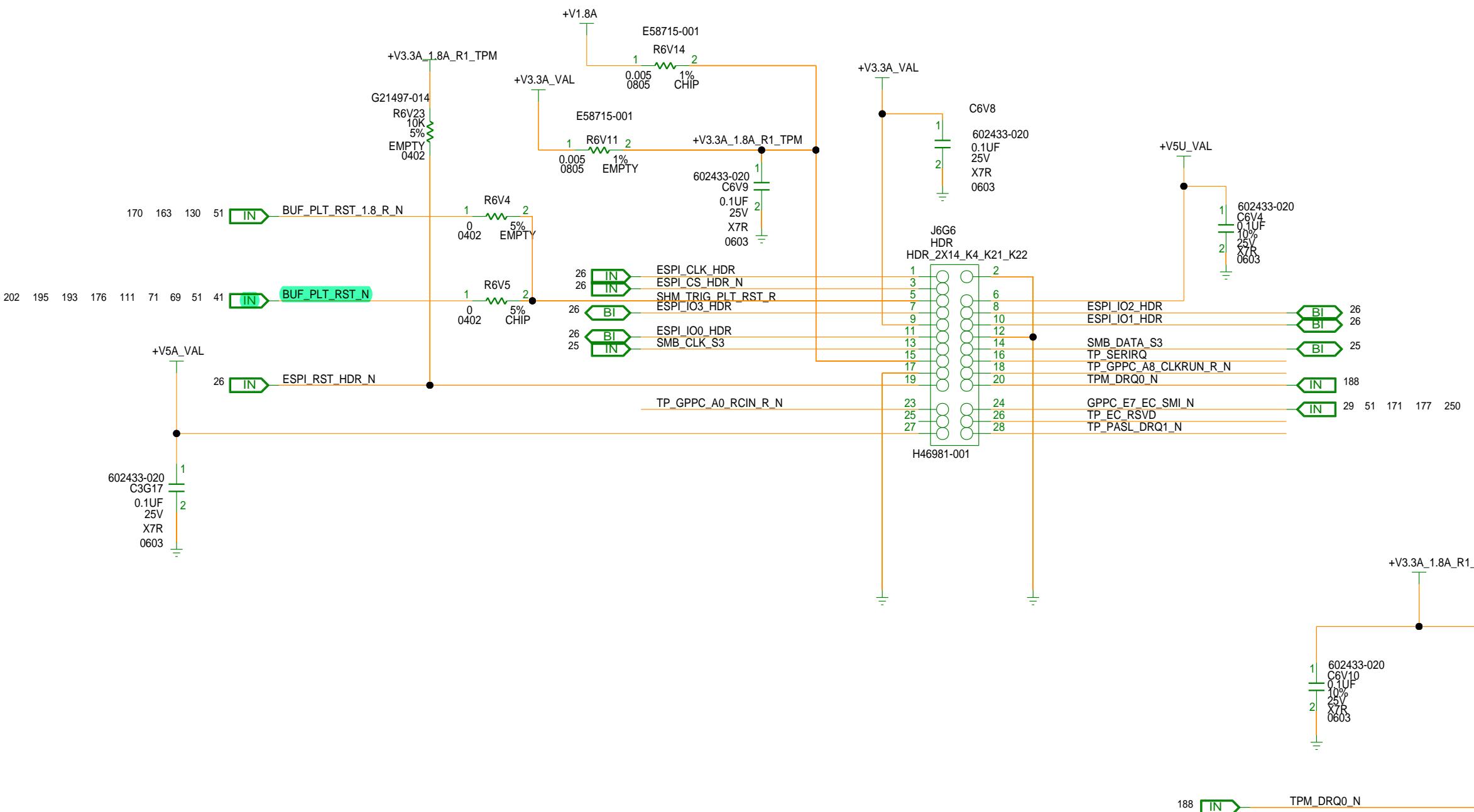
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Wed Dec 18 18:08:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 187	REV 1.0
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MODULE REV DETAILS							

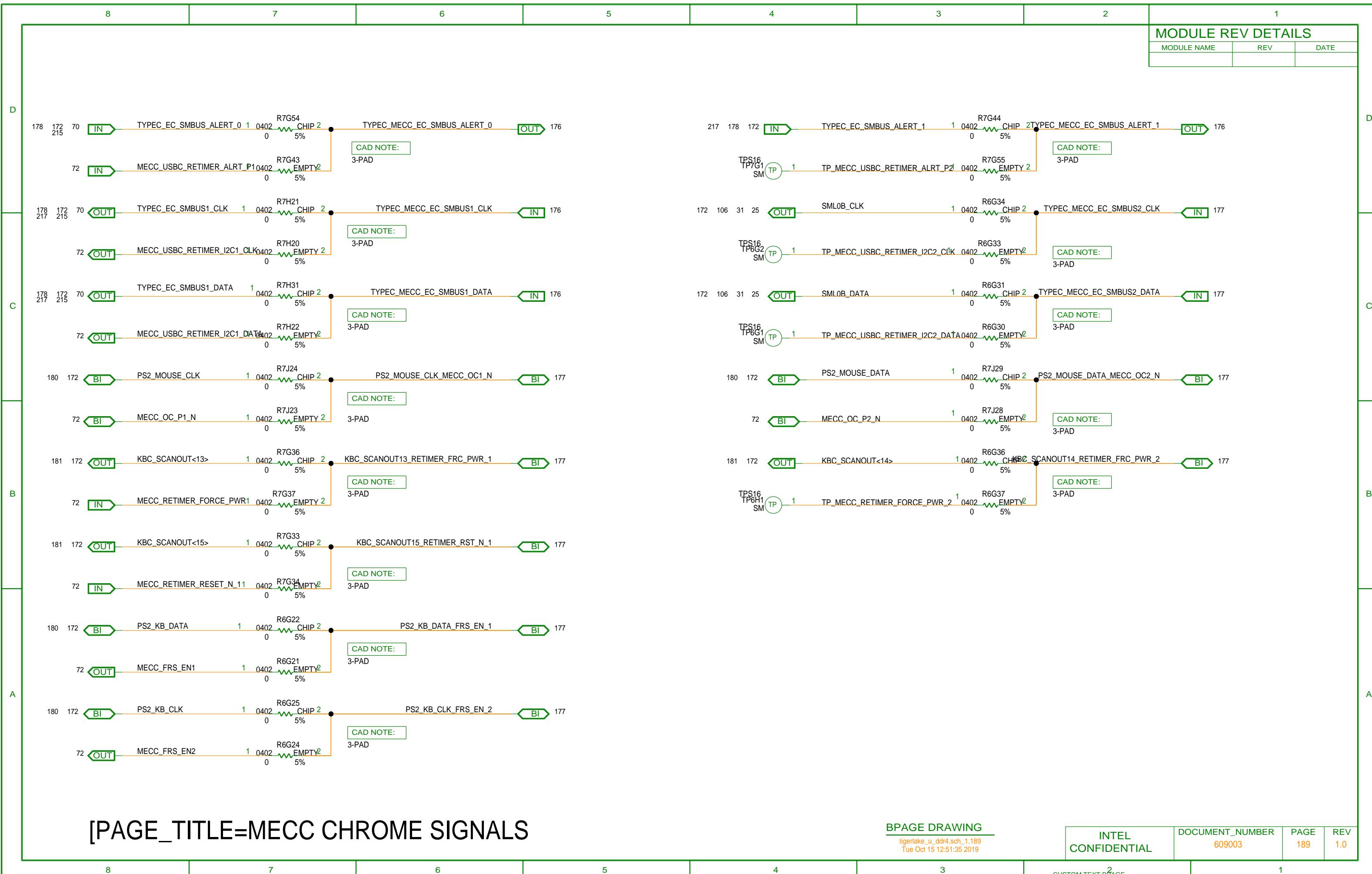
ESPI BUS HEADER

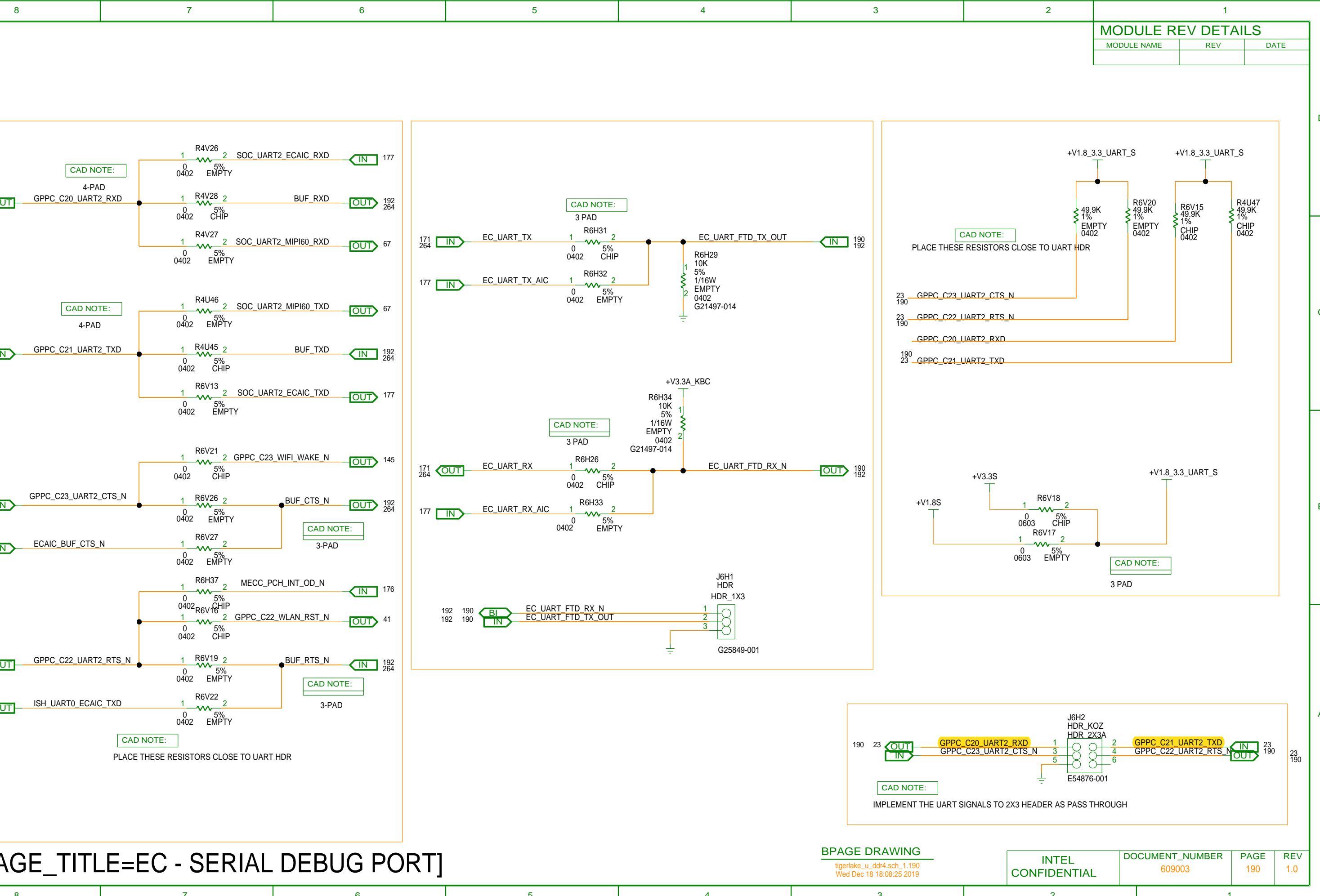


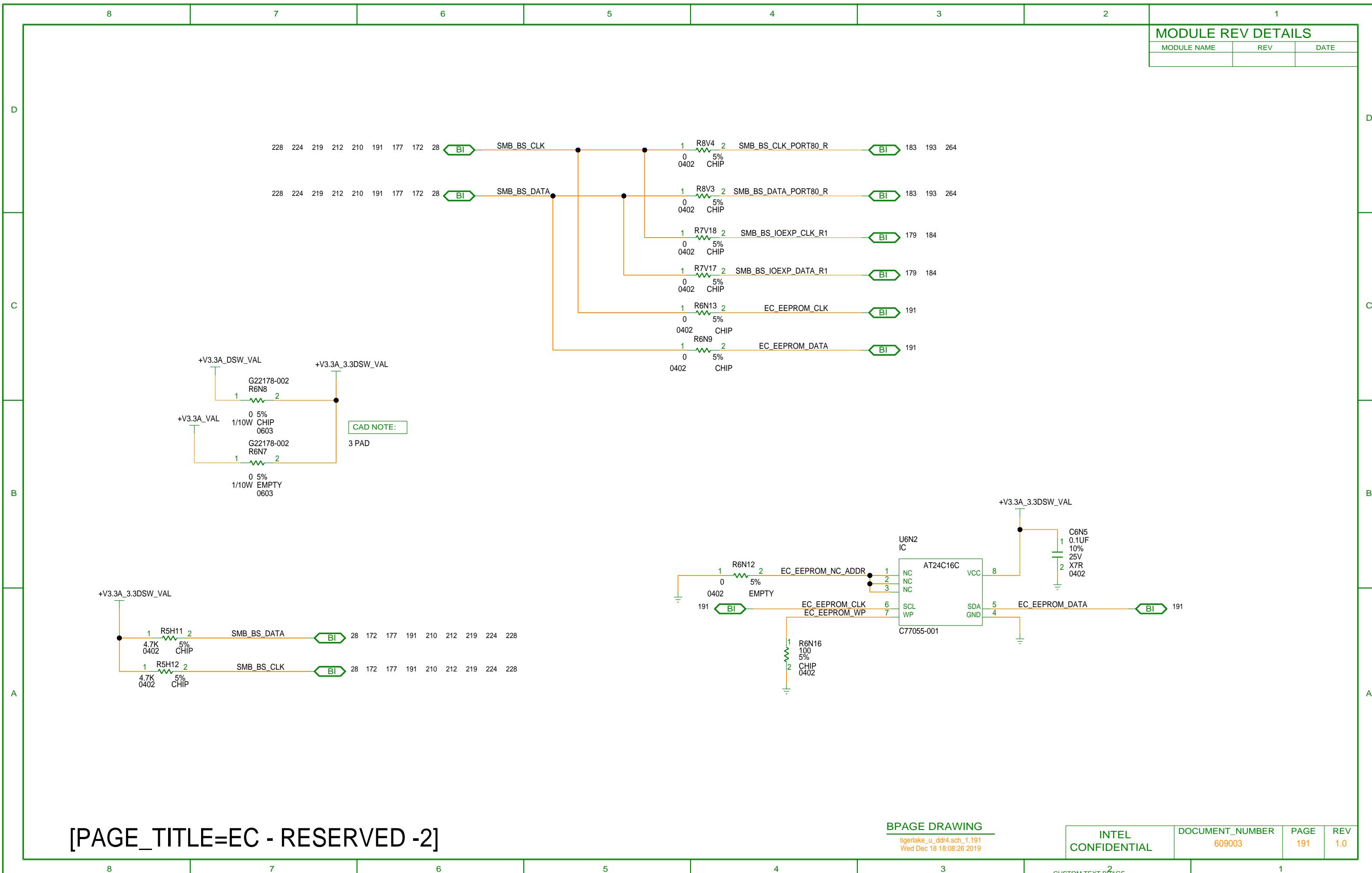
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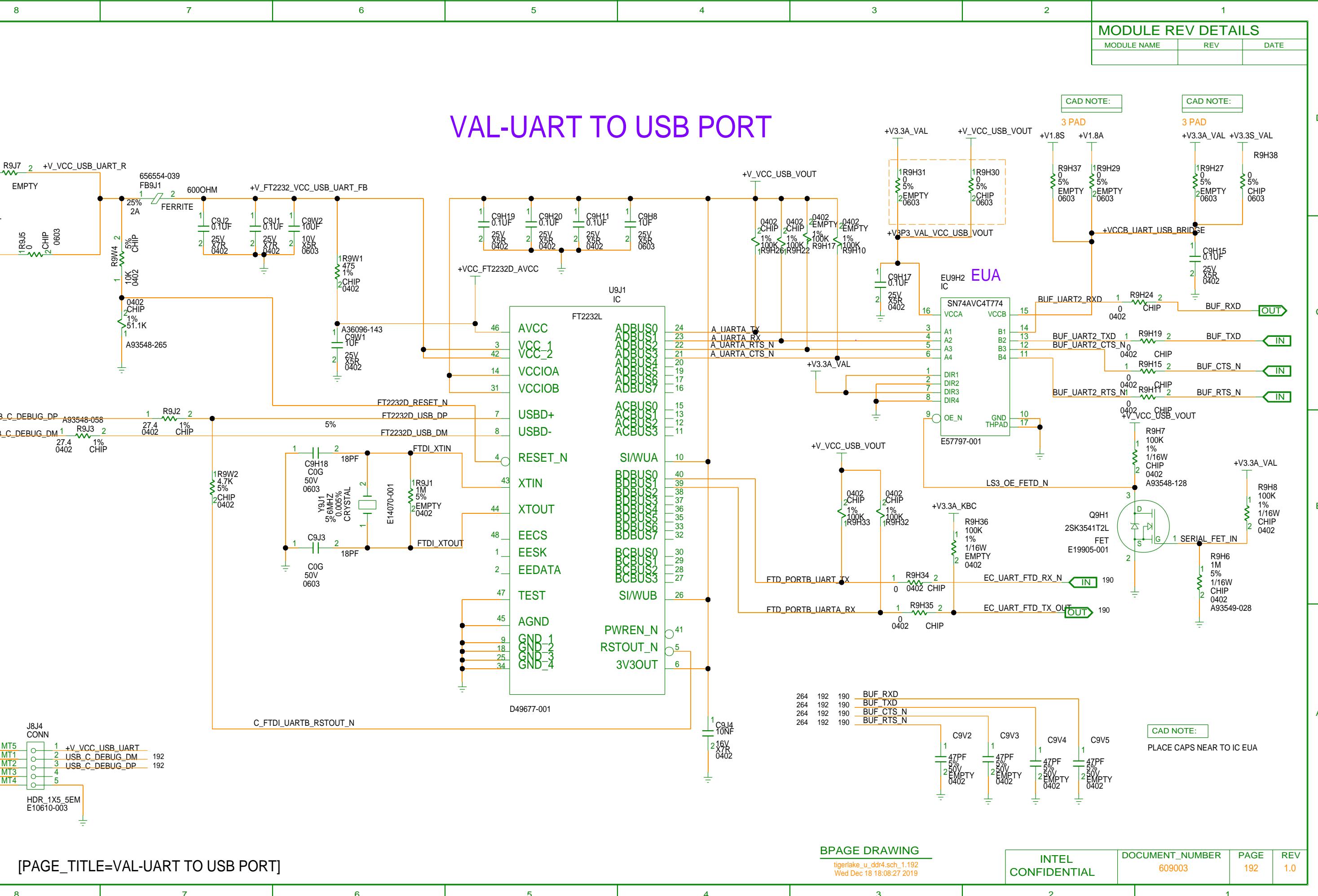
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Wed Dec 18 18:08:24 2019

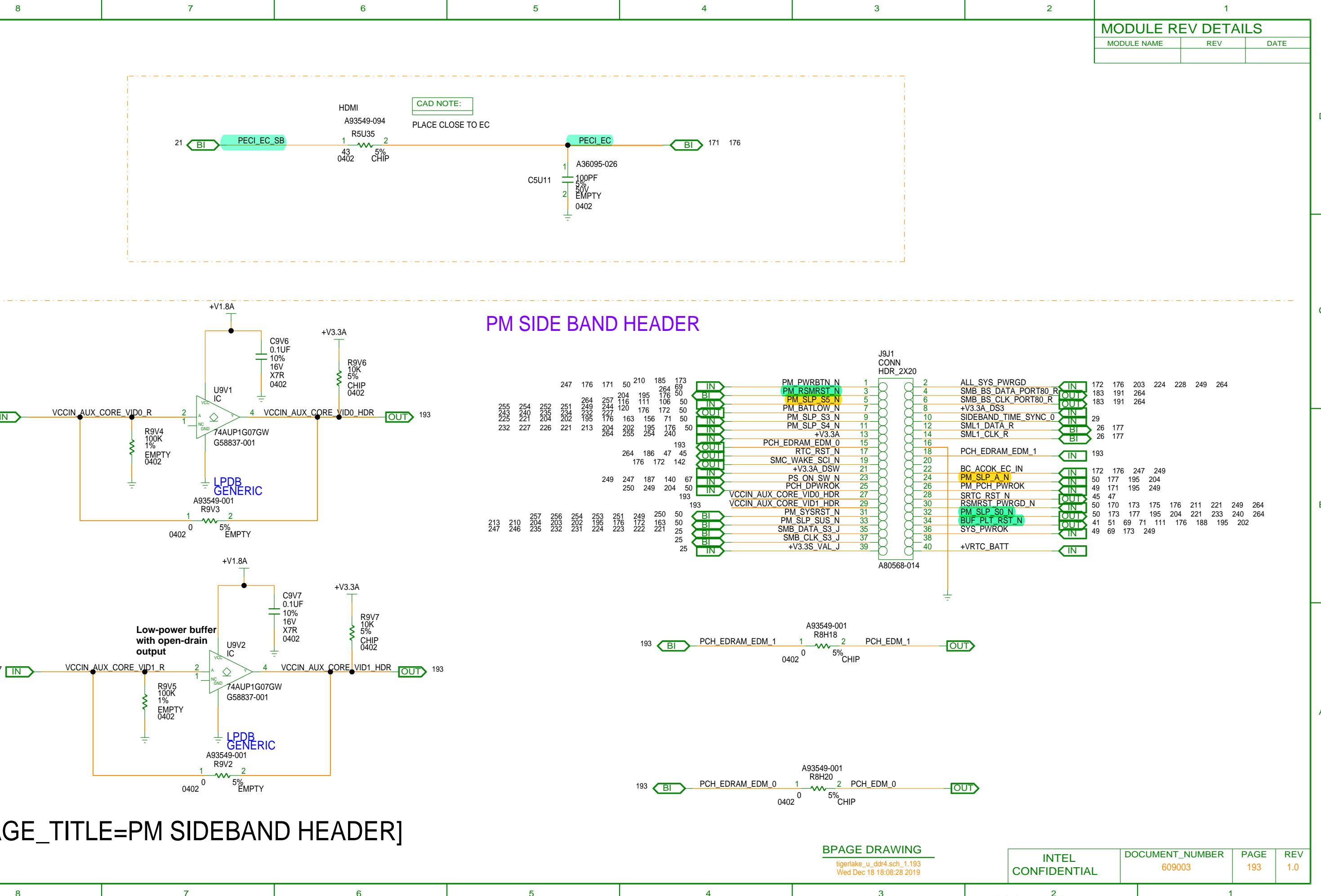
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	188	1.0











8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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Tue Oct 15 12:51:41 2019

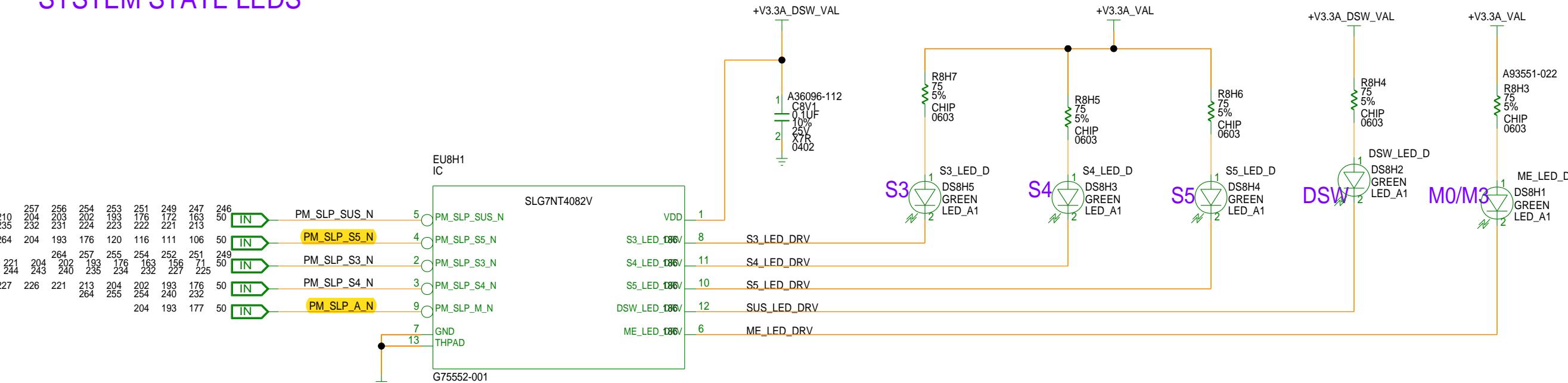
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 194	REV 1.0
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8	7	6	5	4	3	CUSTOM TEXT 2 PAGE	1
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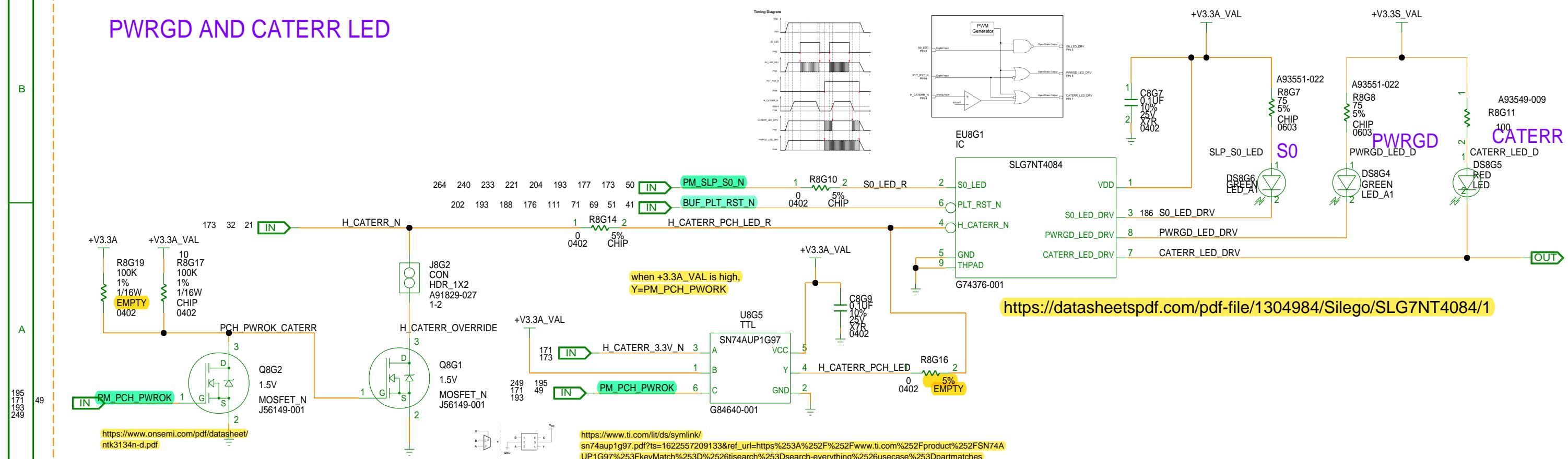
MODULE REV DETAILS

MODULE NAME	REV	DATE

SYSTEM STATE LEDS



PWRGD AND CATERR LED



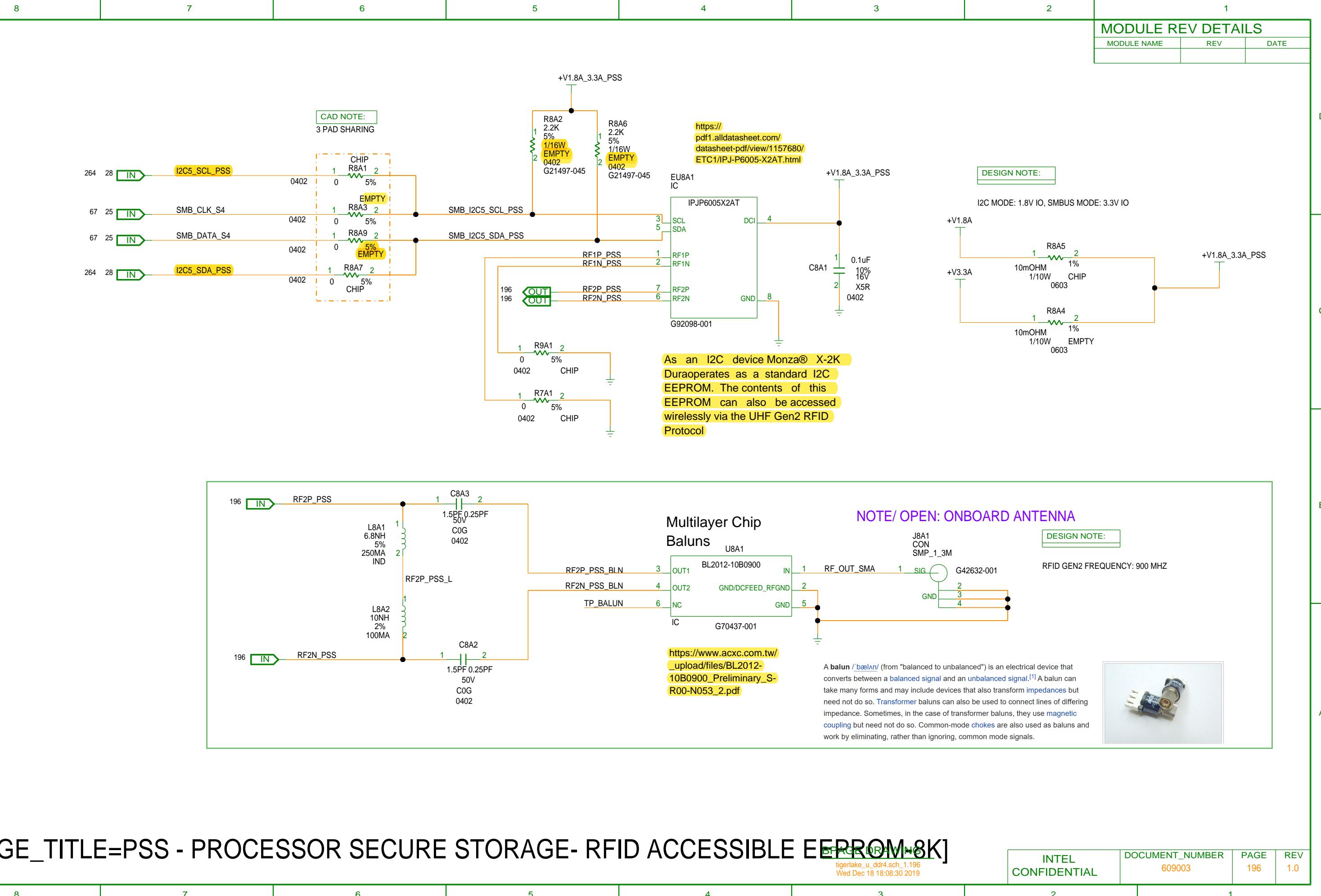
[PAGE_TITLE=SYSTEM STATE LED CIRCUITRY]

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Wed Dec 18 18:08:30 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	195	1.0	

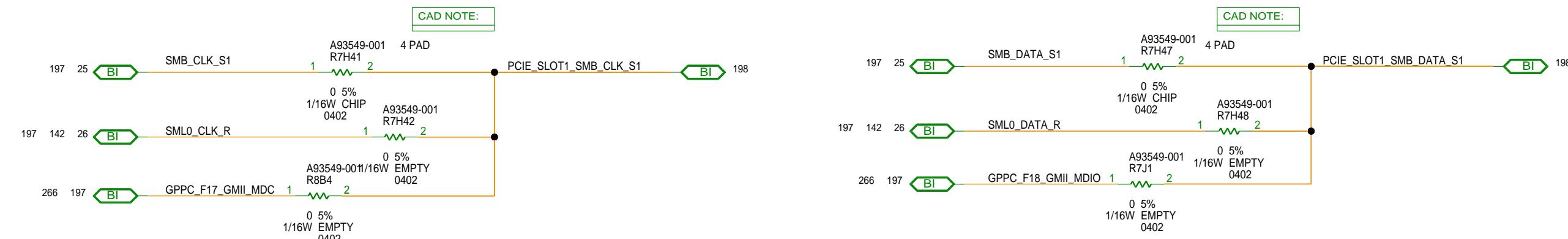
CUSTOM TEXT BPAGE

1

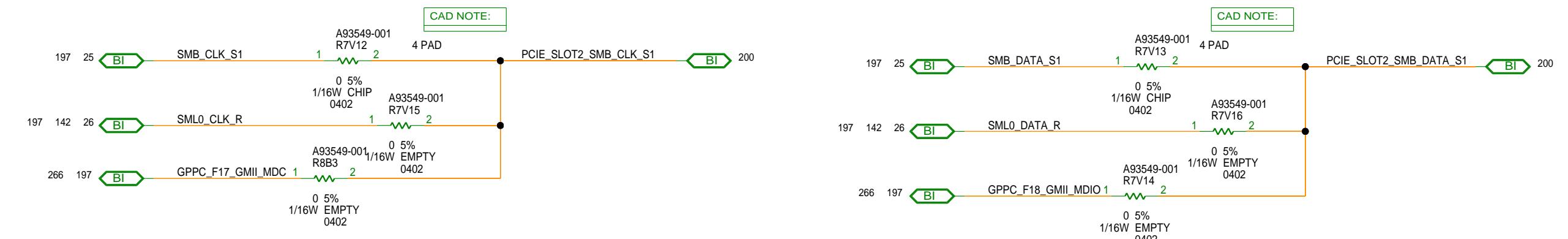


8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME				REV	DATE		

PCIE SLOT 1 SMB SIGNALS



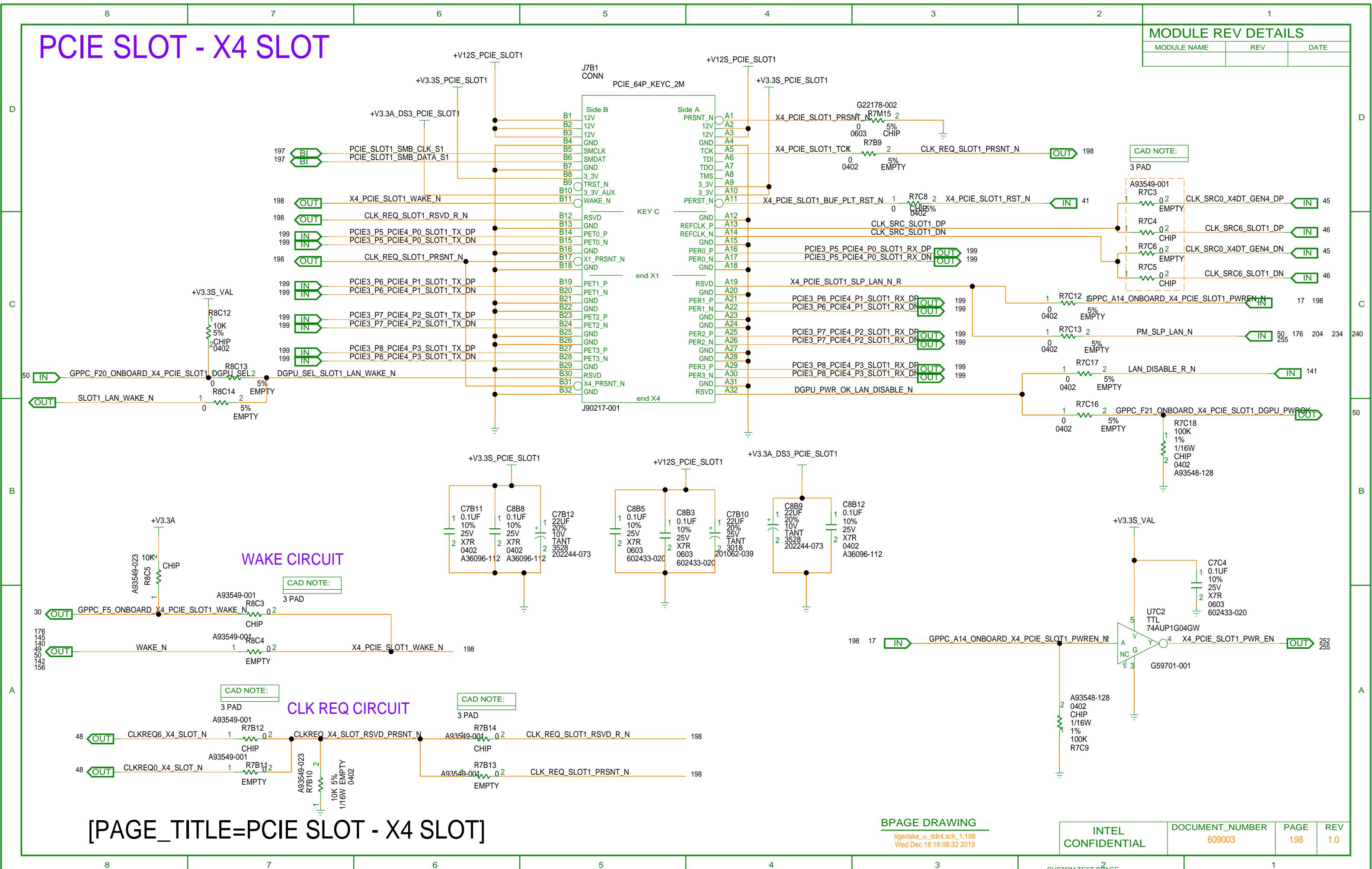
PCIE SLOT 2 SMB SIGNALS

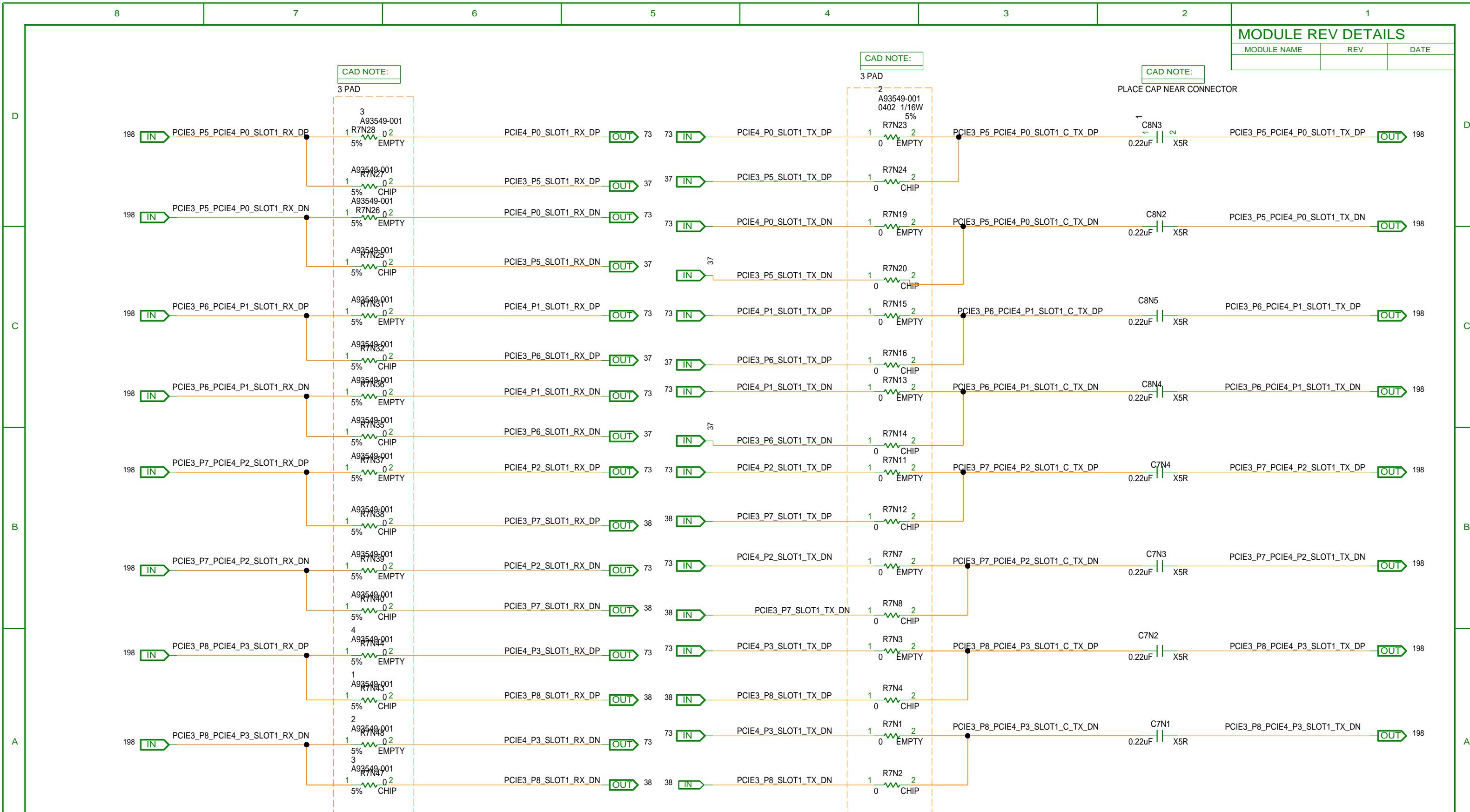


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tigerlake_u_ddr4.sch_1.197
Wed Dec 18 18:08:31 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 197	REV 1.0
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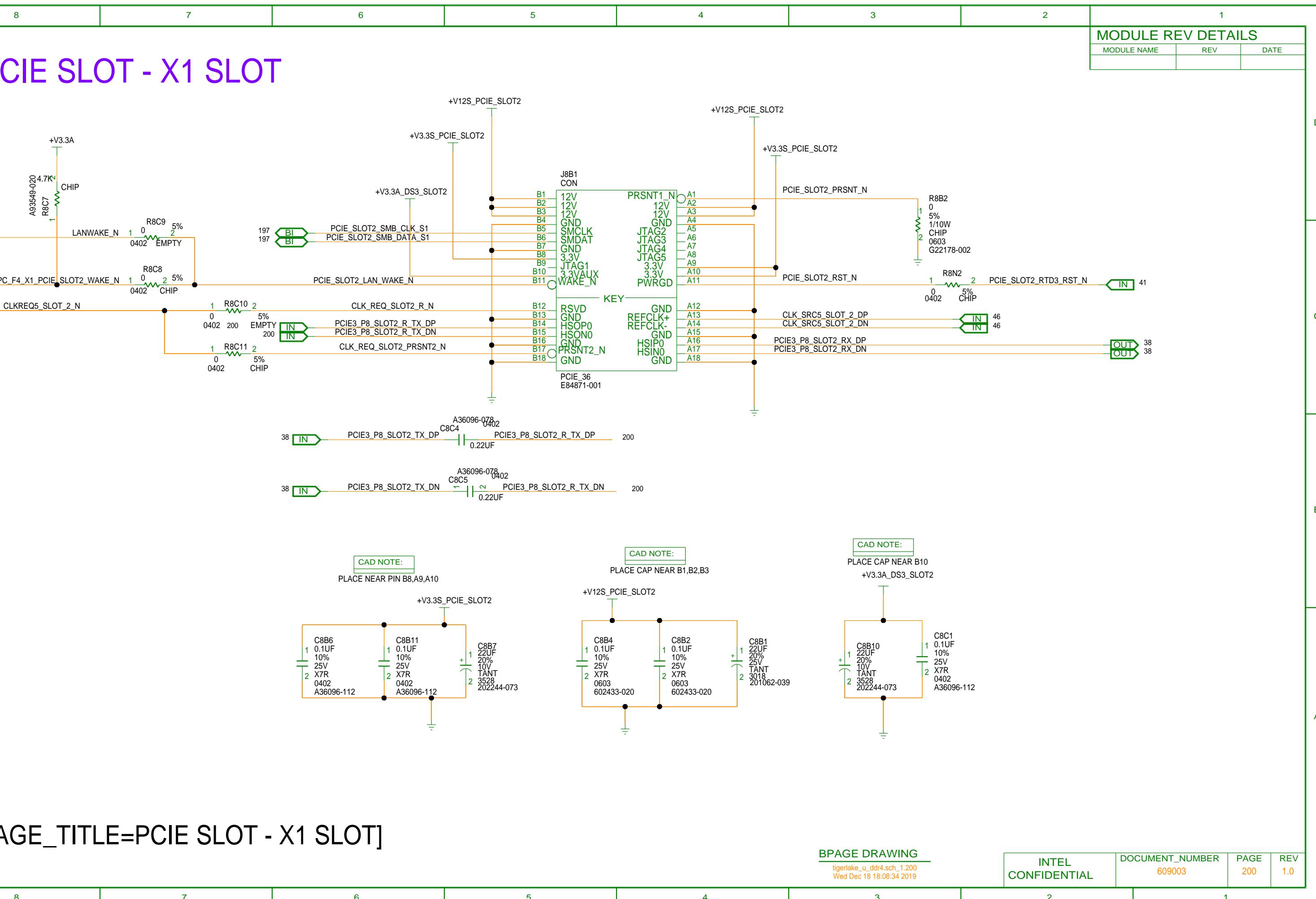


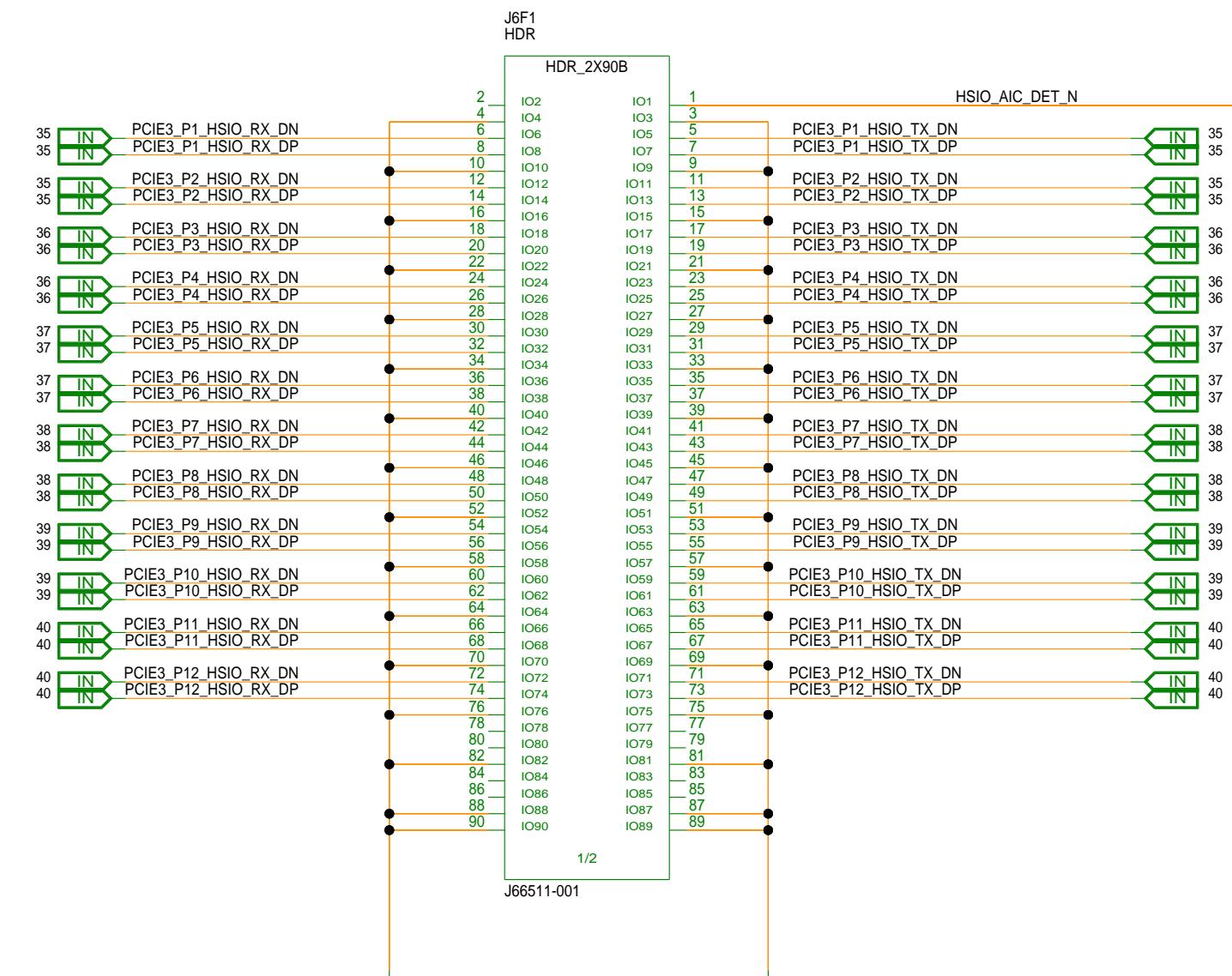
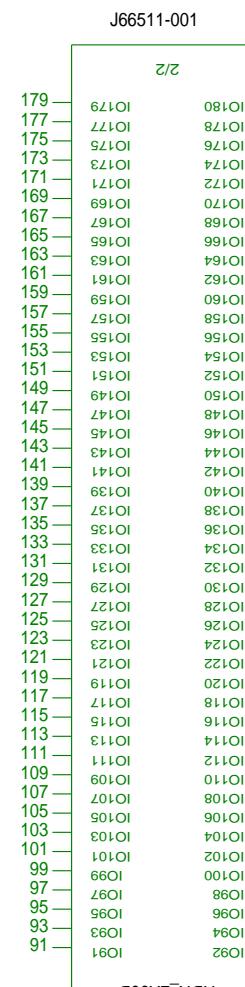


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*tigerlake_u_ddr4.sch_1.199
Wed Dec 18 18:08:33 2019*

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 199	REV 1.0
CUSTOM TEXT BPAGE			





[PAGE_TITLE=HSIO CONNECTOR (1 OF 4)]

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Wed Dec 18 18:08:35 2019

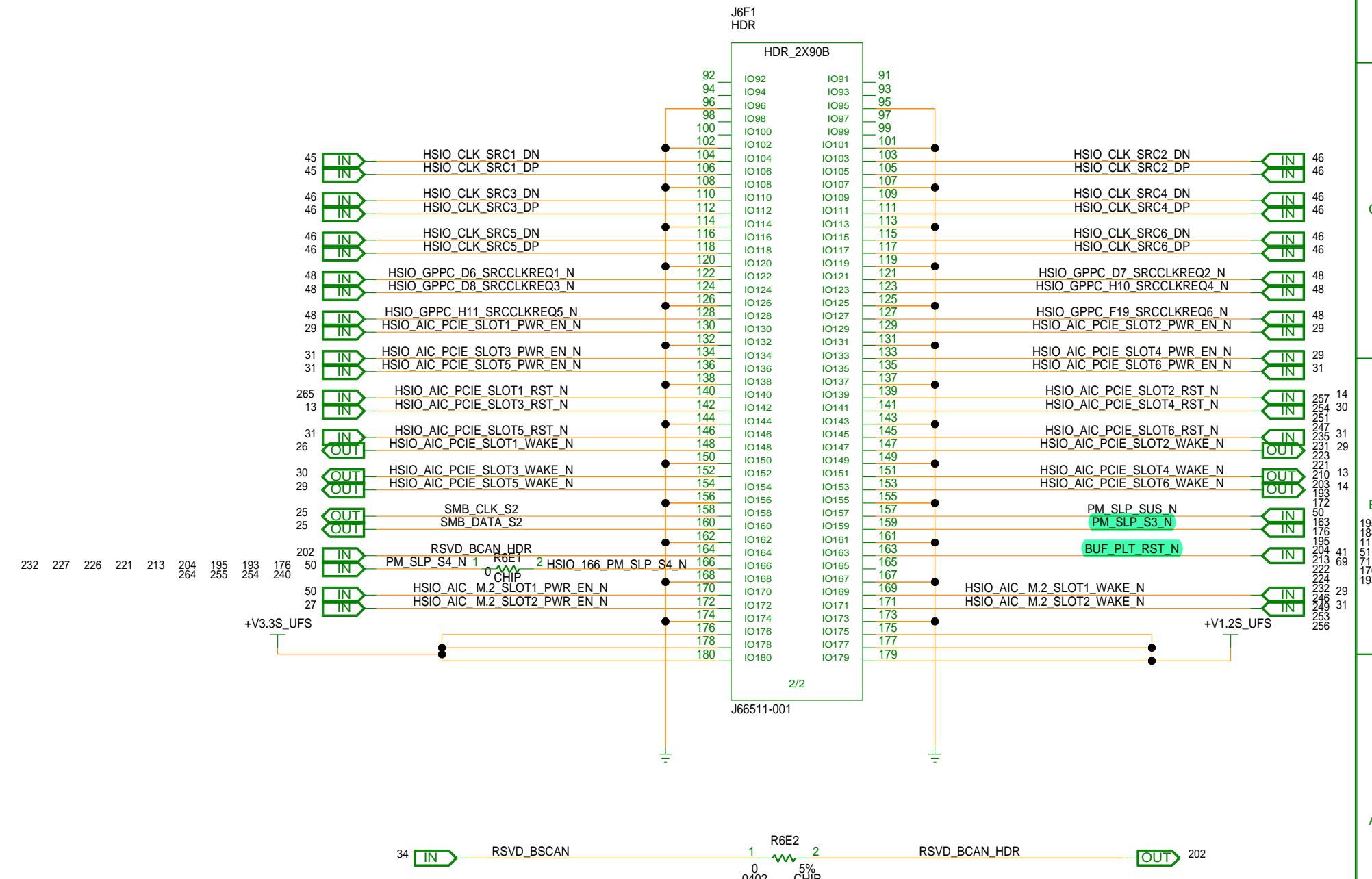
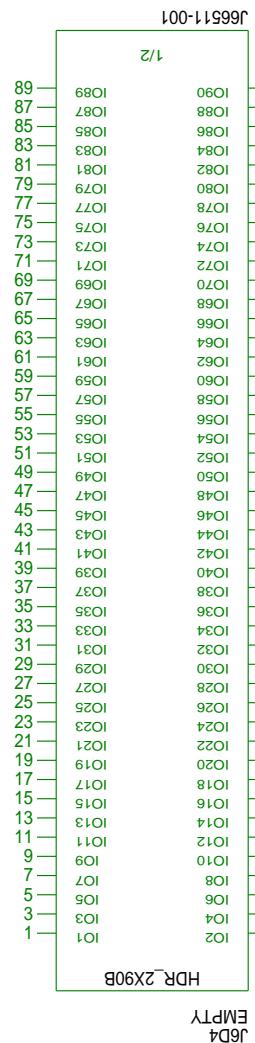
INTEL
CONFIDENTIAL

DOCUMENT_NUMBER 609003	PAGE 201	REV 1.0
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8	7	6	5	4	3	2	1
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



[PAGE_TITLE=HSIO CONNECTOR (2 OF 4)]

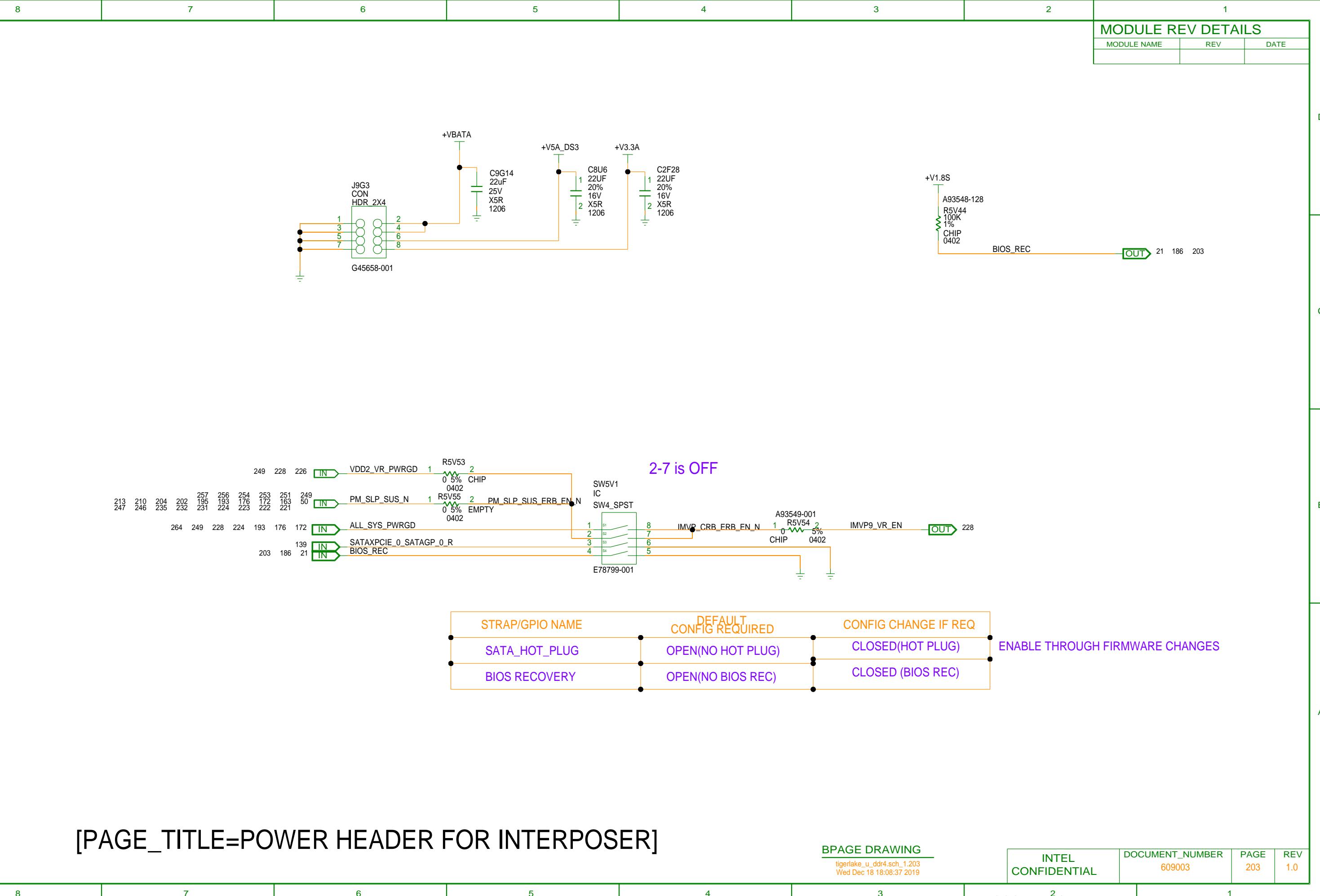
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Wed Dec 18 18:08:36 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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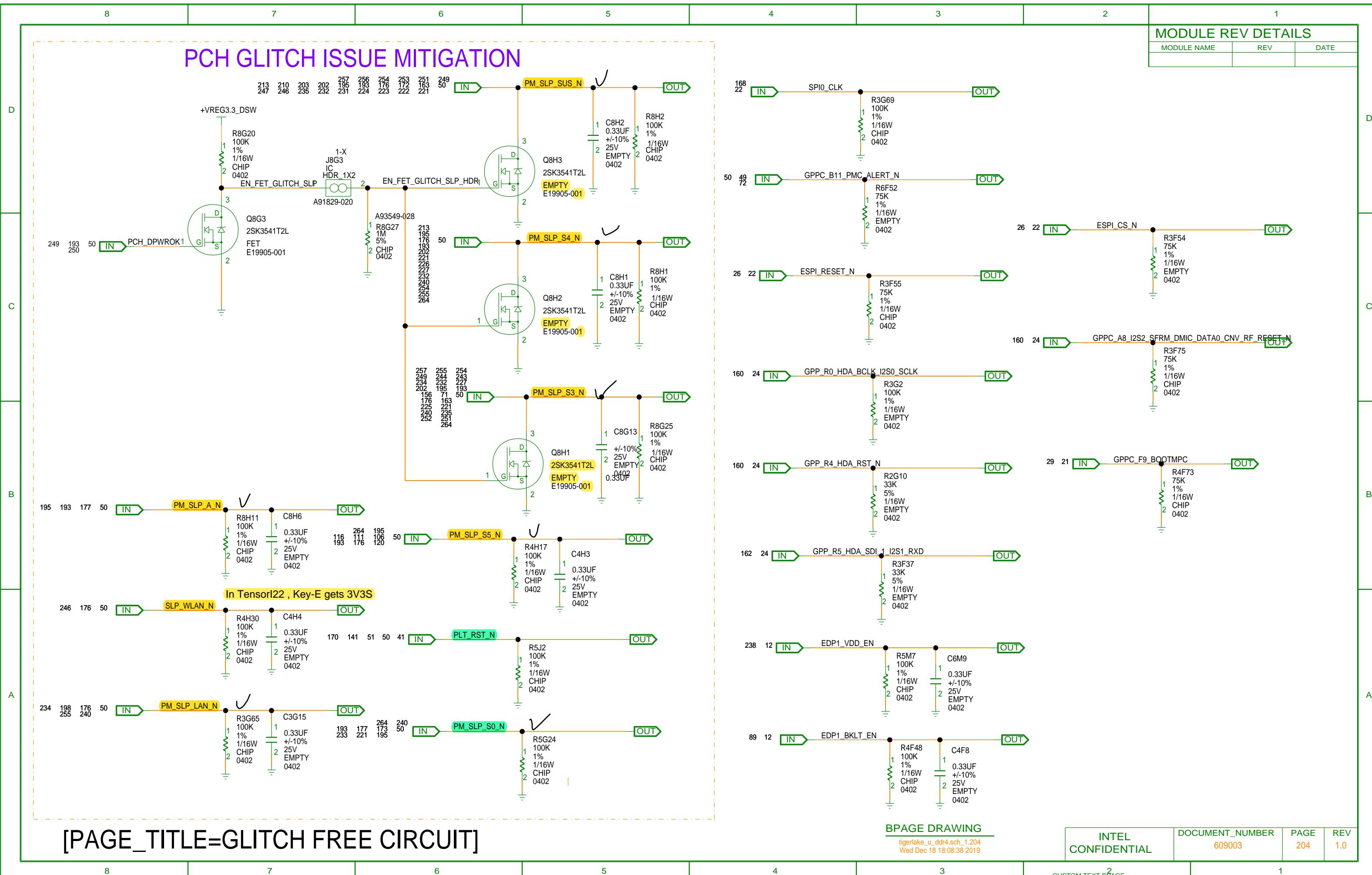
8	7	6	5	4	3	2	1
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CUSTOM TEXT B PAGE

1



PCH GLITCH ISSUE MITIGATION



BPAGE DRAWING
*tigerlake_u_ddr4.sch_1.204
Wed Dec 18 18:08:38 2019*

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 204	REV 1.0
CUSTOM TEXT BPAGE	2	1	1

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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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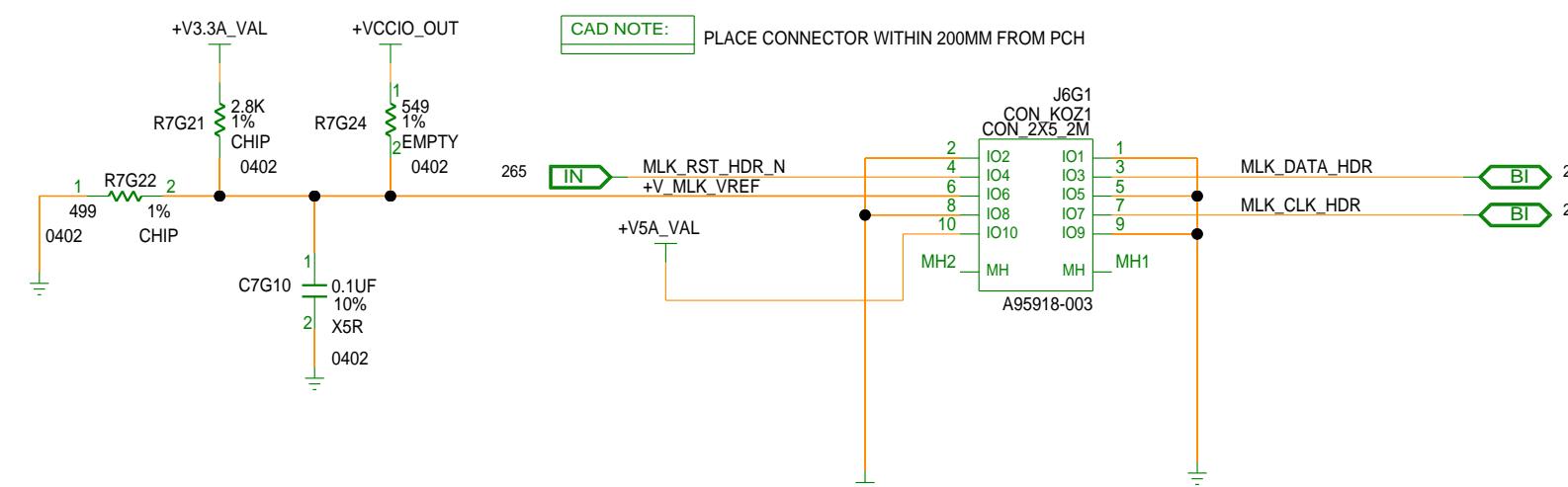
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MLINK HEADER



[PAGE_TITLE=MLX HEADER]

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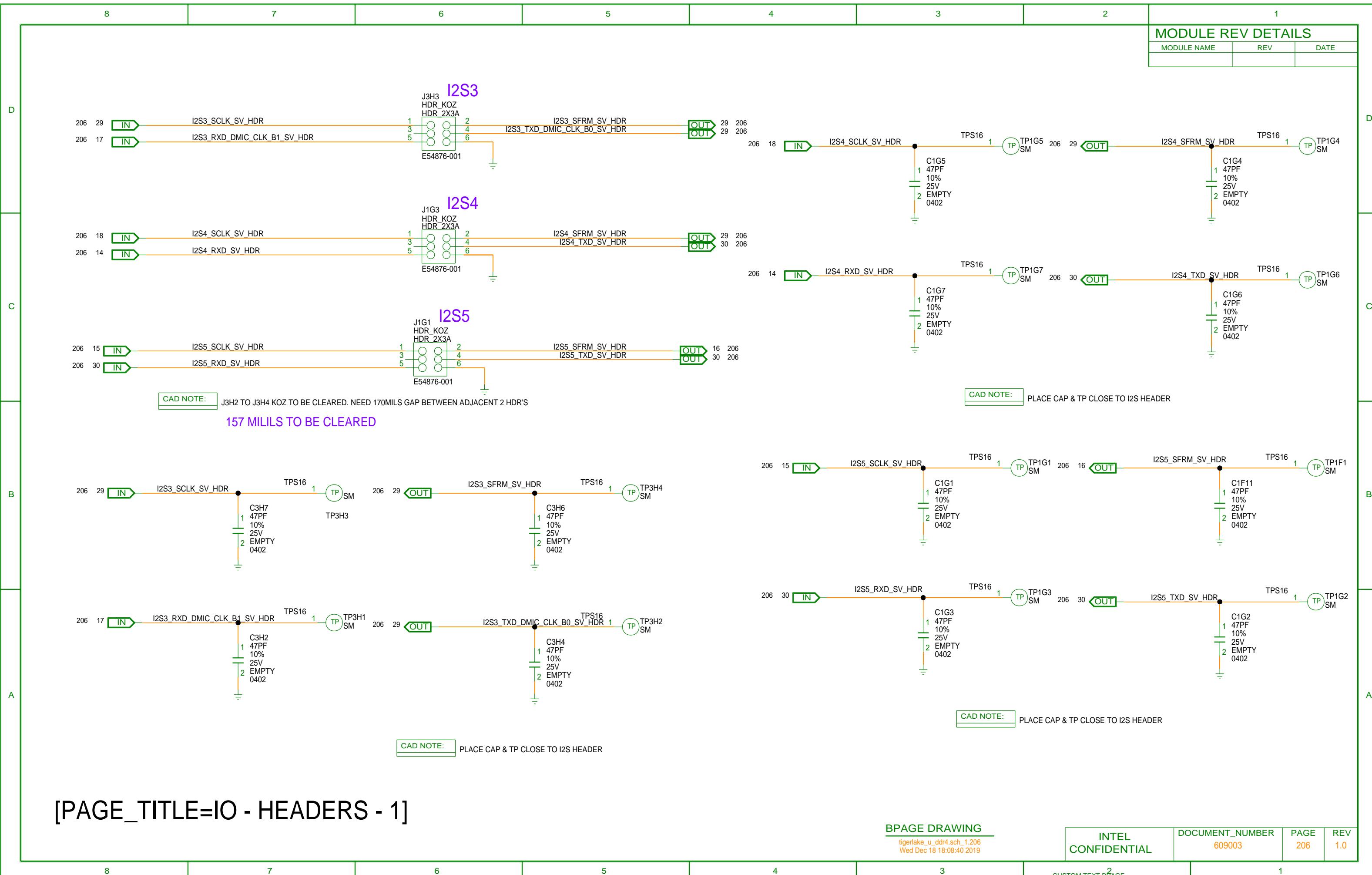
tigerlake_u_ddr4.sch_1.205
Wed Dec 18 18:08:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS

MODULE NAME	REV	DATE



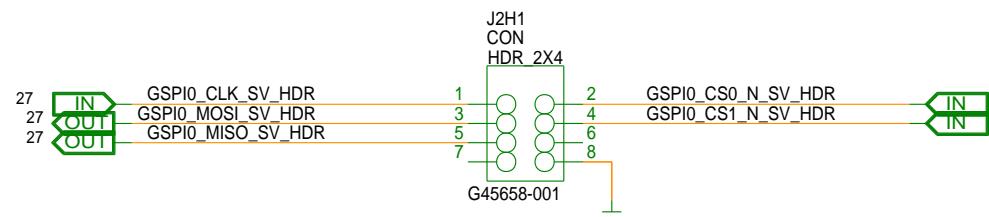
8	7	6	5	4	3	2	1
MODULE REV DETAILS							

CAD NOTE: MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

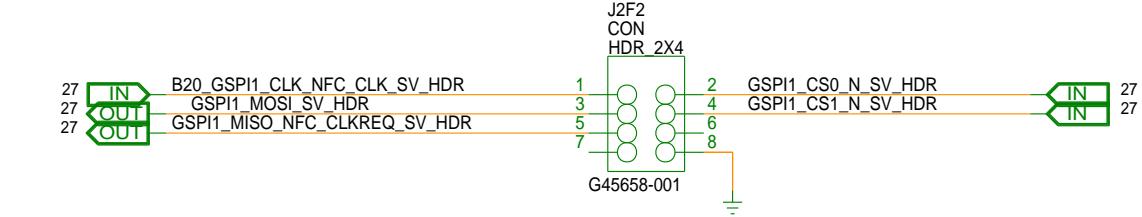
CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

GSPI0 HEADER



GSPI1 HEADER



GSPI2 IS AVAILABLE ON ISH SPI AND ISH UART HEADER
SPI1 IS AVAILABLE ON THC SV HEADER

8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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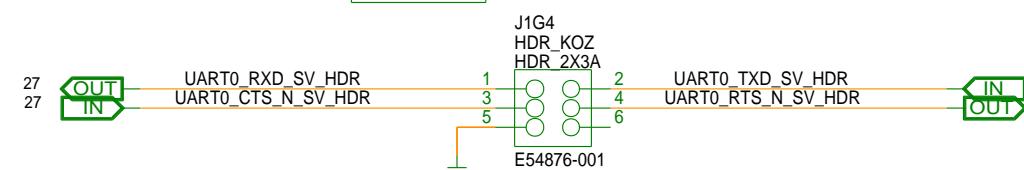
CAD NOTE:

MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

LPSS UART0 HEADER

CAD NOTE:

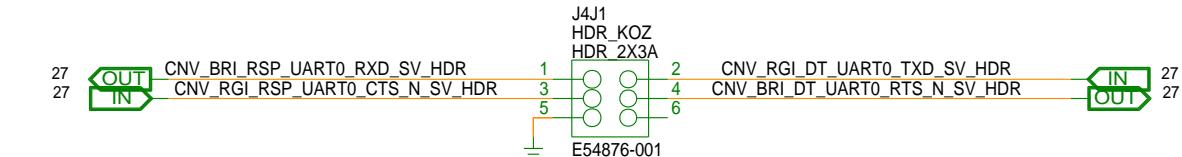
PLACE CONNECTOR WITHIN 300MM FROM PCH



CNV UART0 HEADER

CAD NOTE:

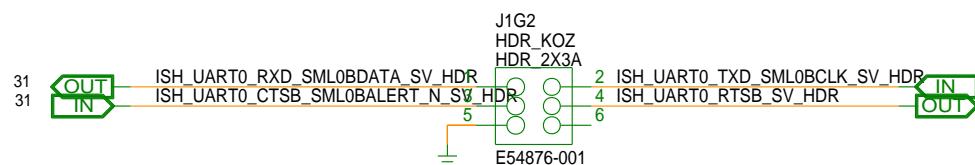
PLACE CONNECTOR WITHIN 300MM FROM PCH



ISH UART0 / SMLINK0B HEADER

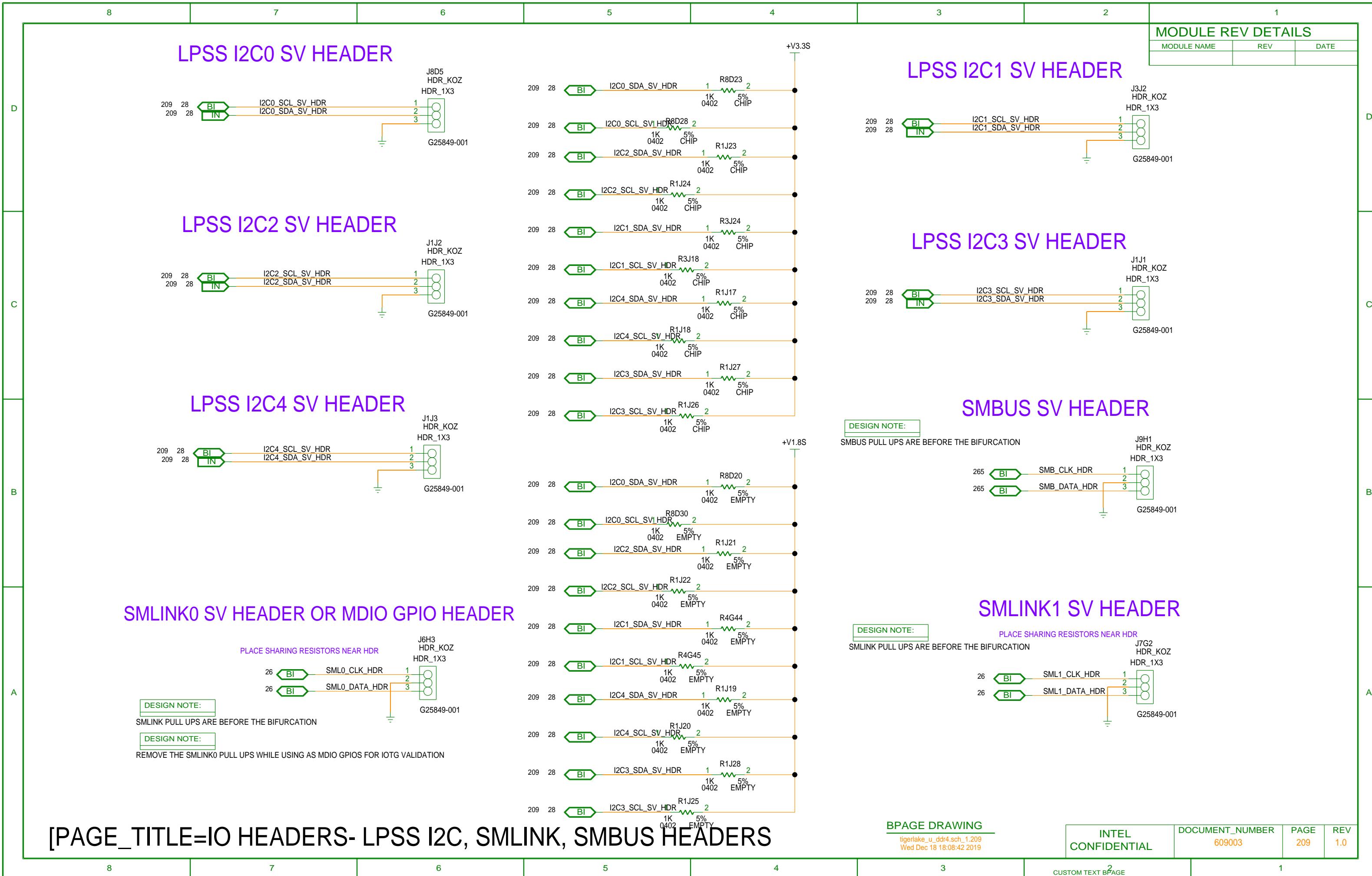
CAD NOTE:

PLACE CONNECTOR WITHIN 300MM FROM PCH



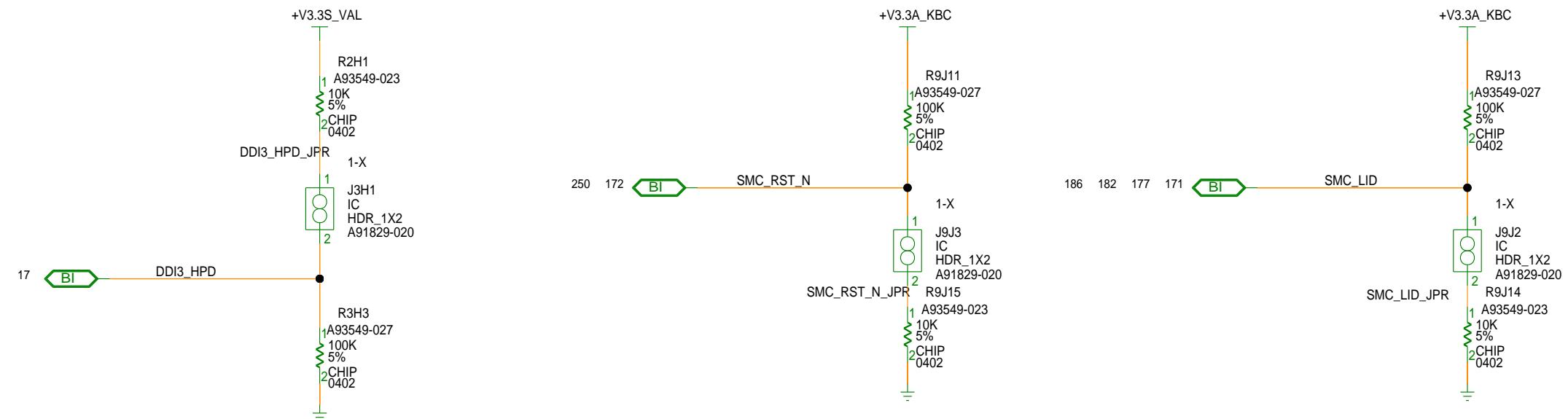
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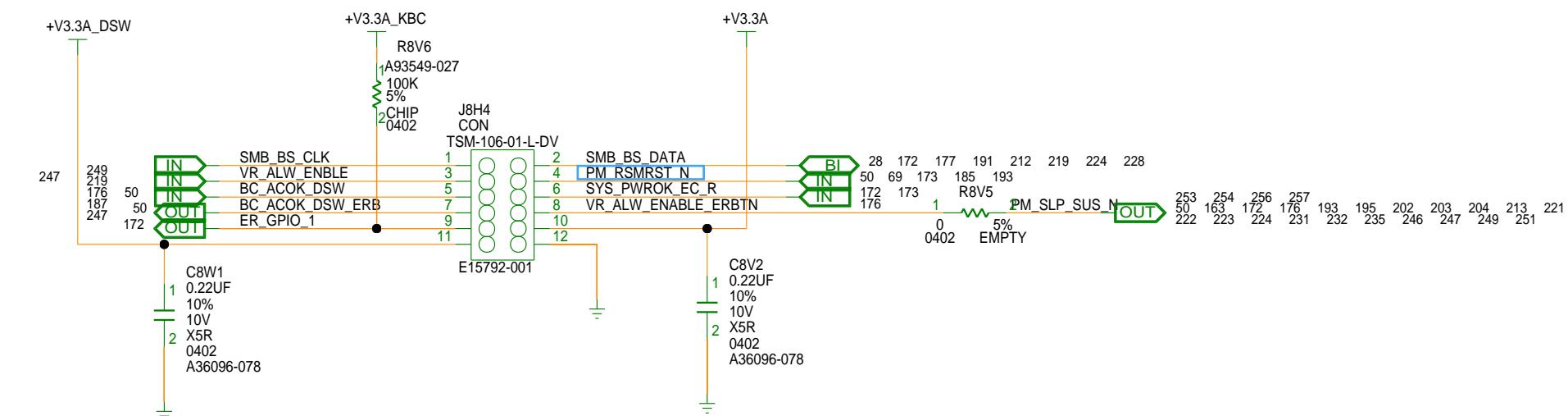


8	7	6	5	4	3	2	1
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JUMPERS FOR VALIDATION



EYE RIVER VALIDATION HEADER



[PAGE_TITLE= IO HEADERS- EYE RIVER HEADER AND OTHER JUMPERS]

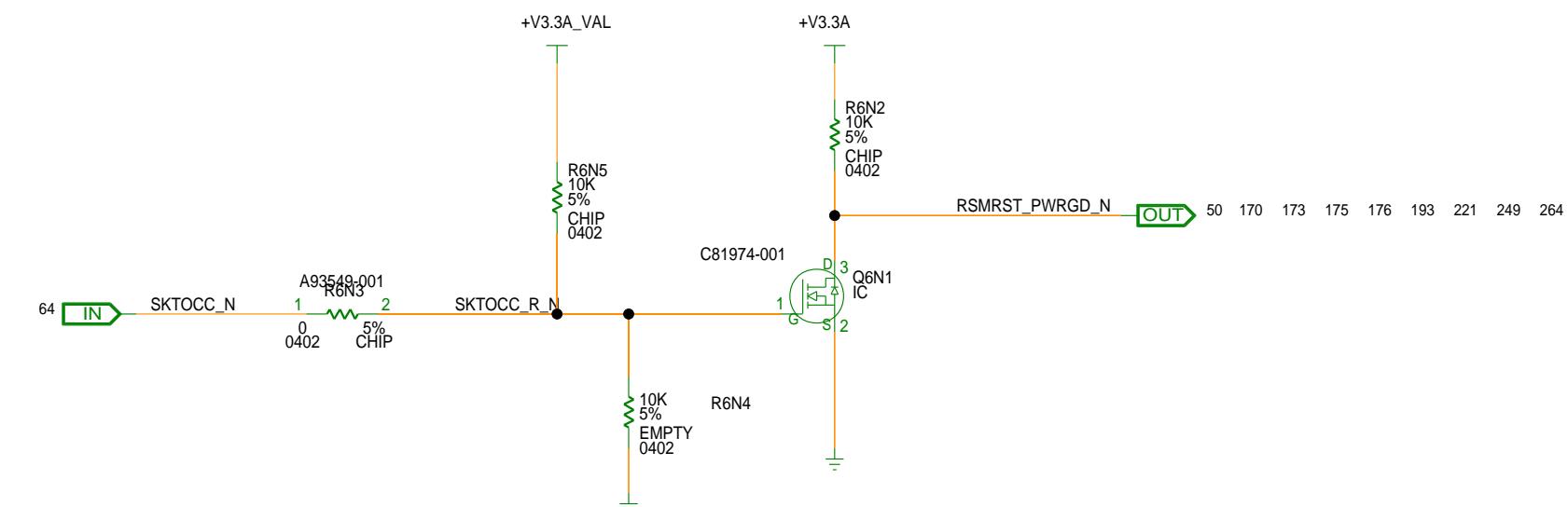
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Wed Dec 18 18:08:43 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 210	REV 1.0
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8	7	6	5	4	3	2	1
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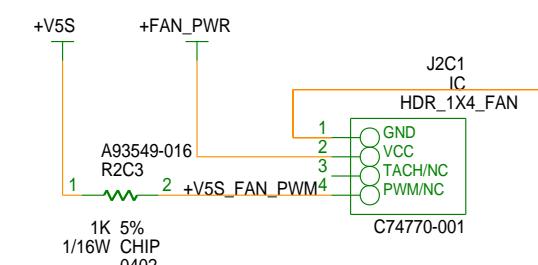
8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

SKTOCC_N -> H_PRESENT_N (CPU DETECT,SKTOCC_N)



CONNECT TO A PROPER VSS PIN OF PCH
PROCESSOR & PCH PART DETECT

FAN HEADER



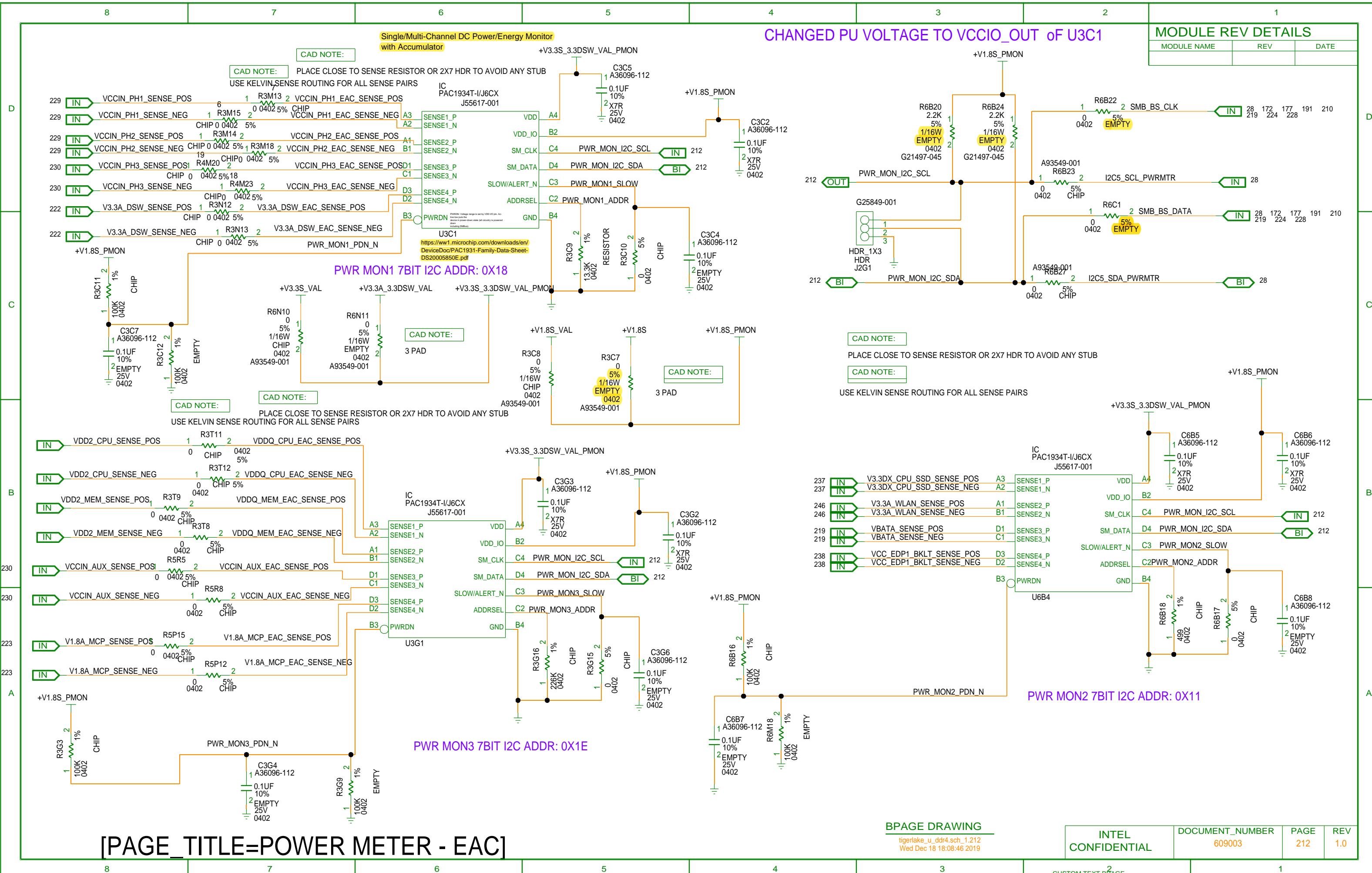
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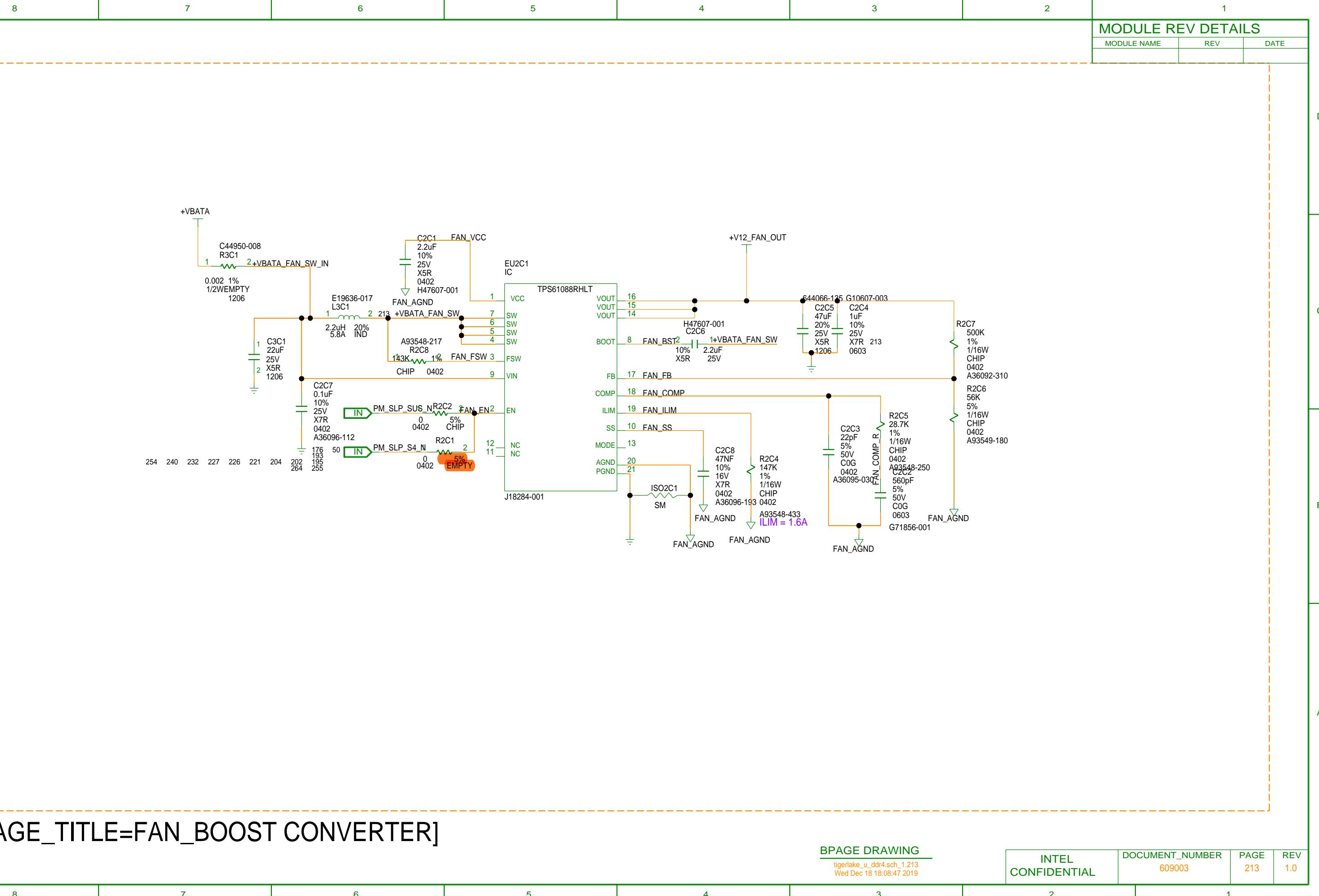
J2A4 FAN CONNECTOR ON & STANDBY(S3)

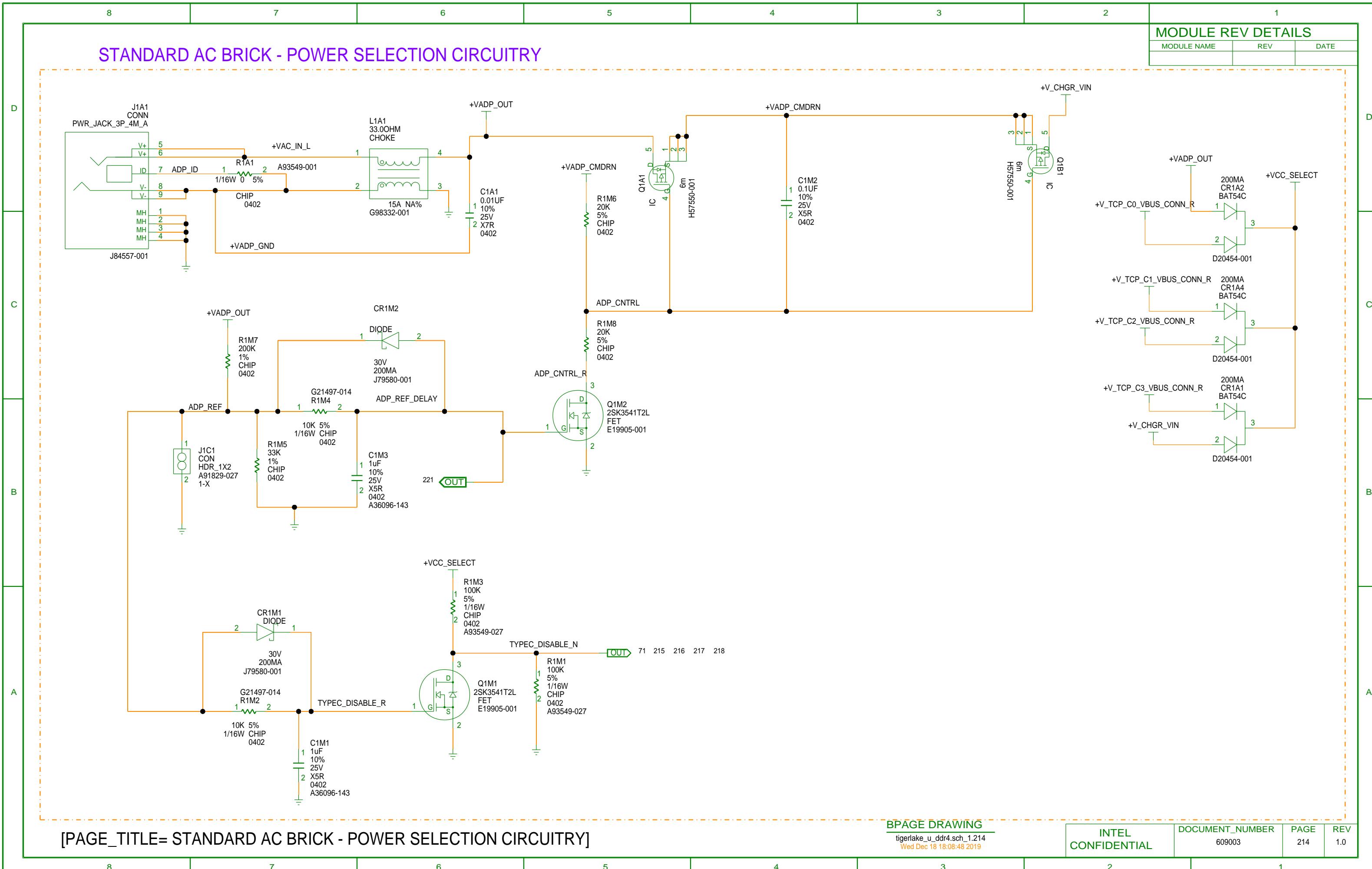
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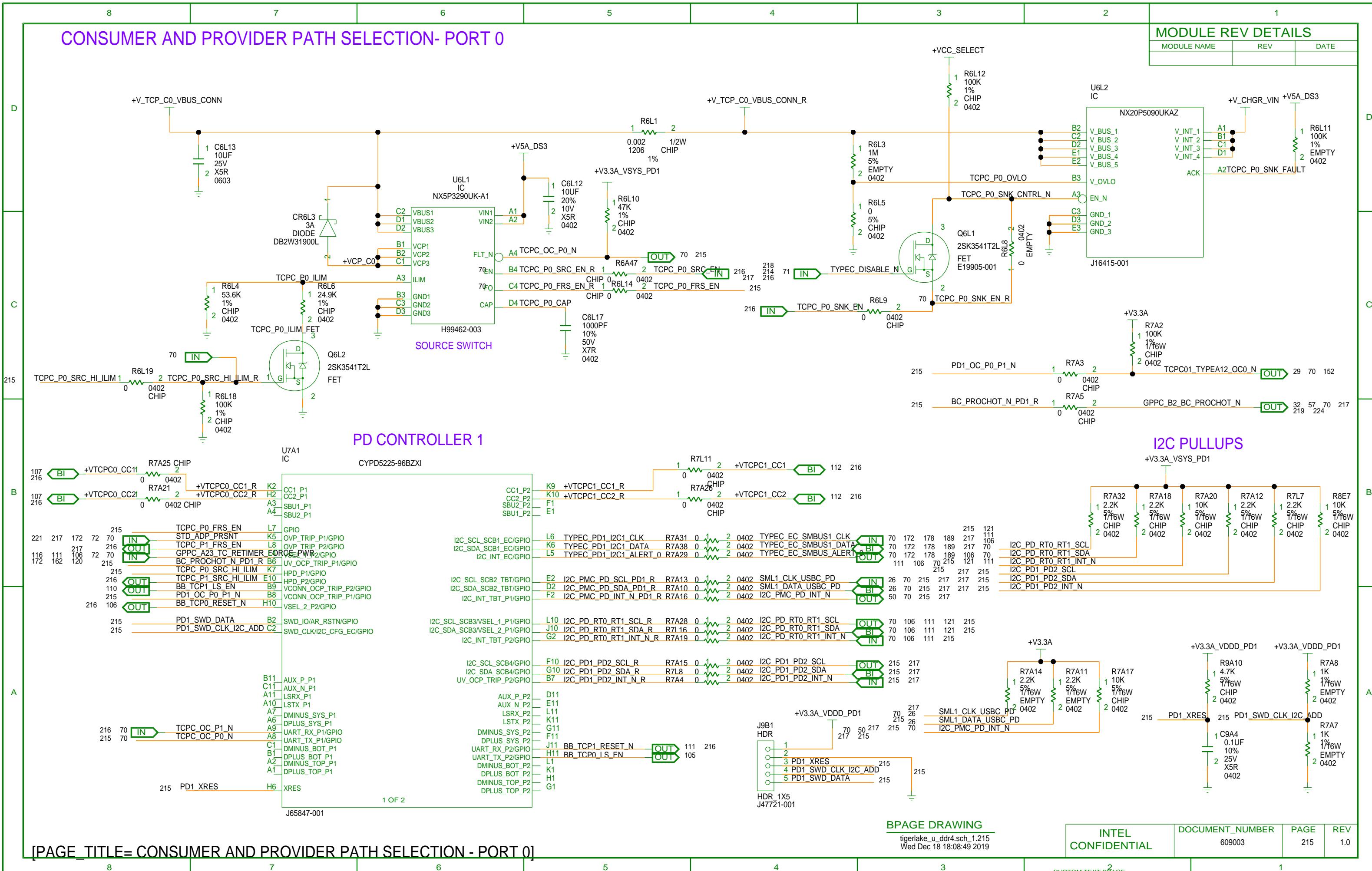
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tigerlake_u_ddr4.sch_1.211
Wed Dec 18 18:08:45 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 211	REV 1.0
CUSTOM TEXT 2 PAGE			1





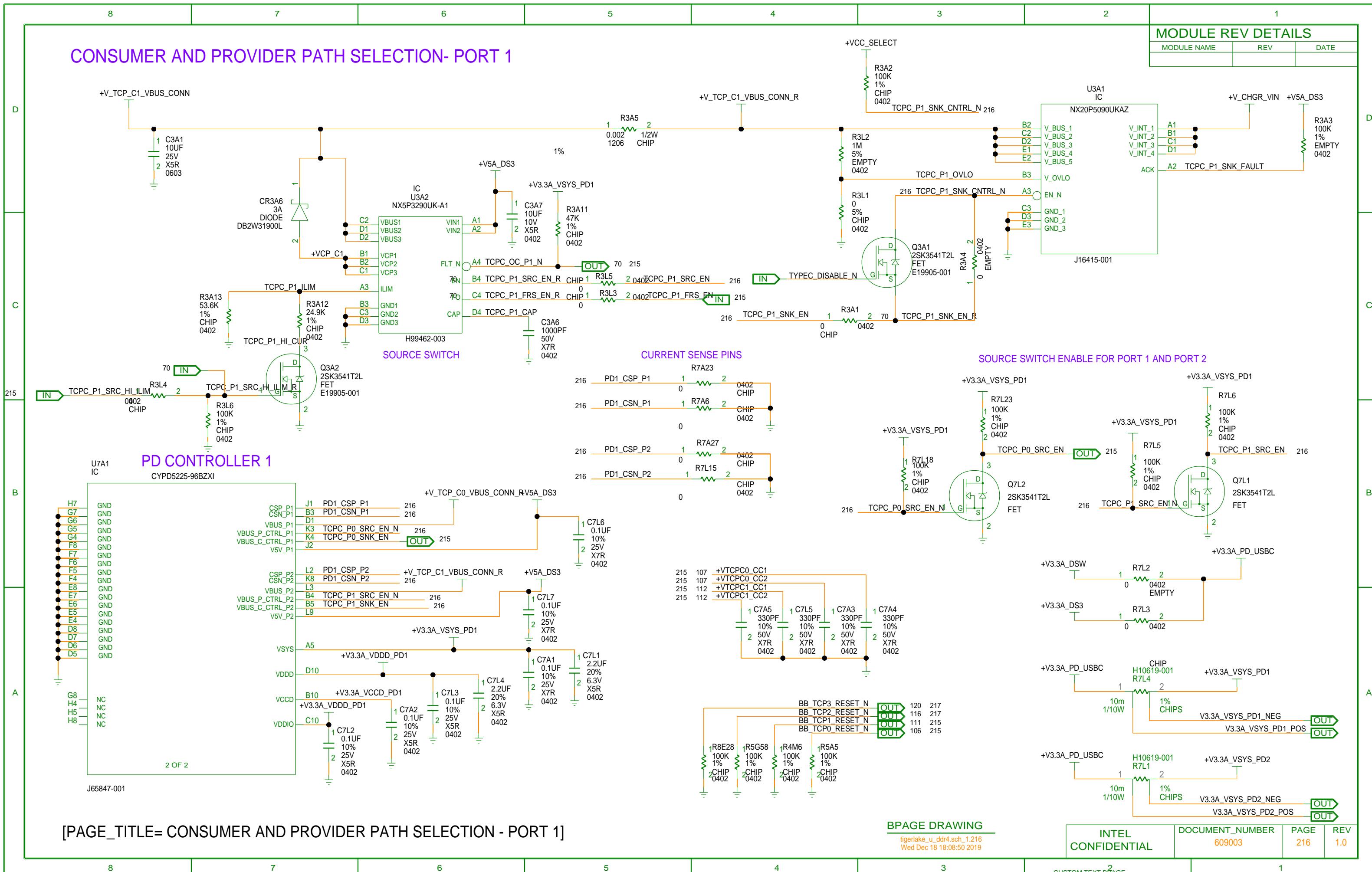


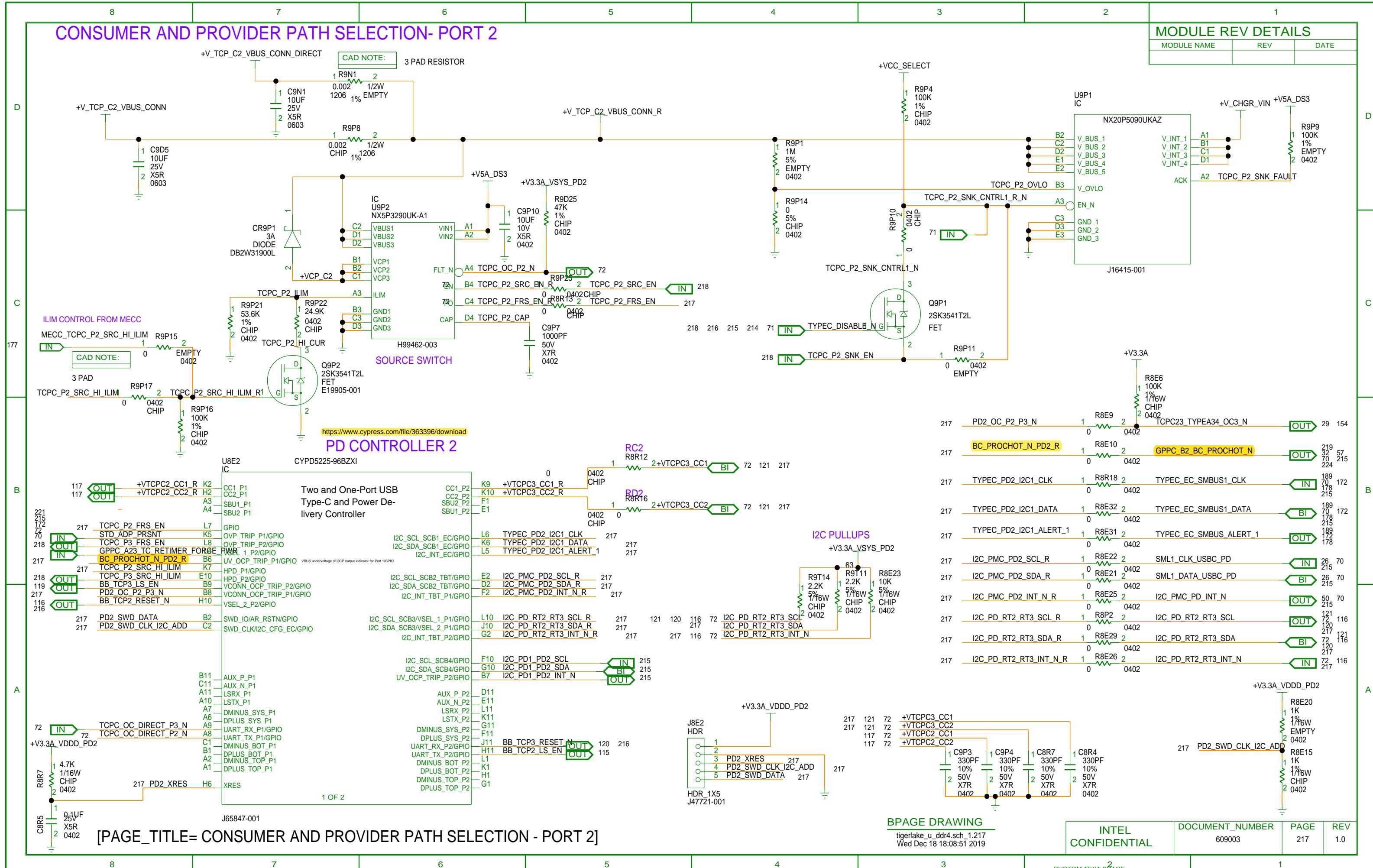


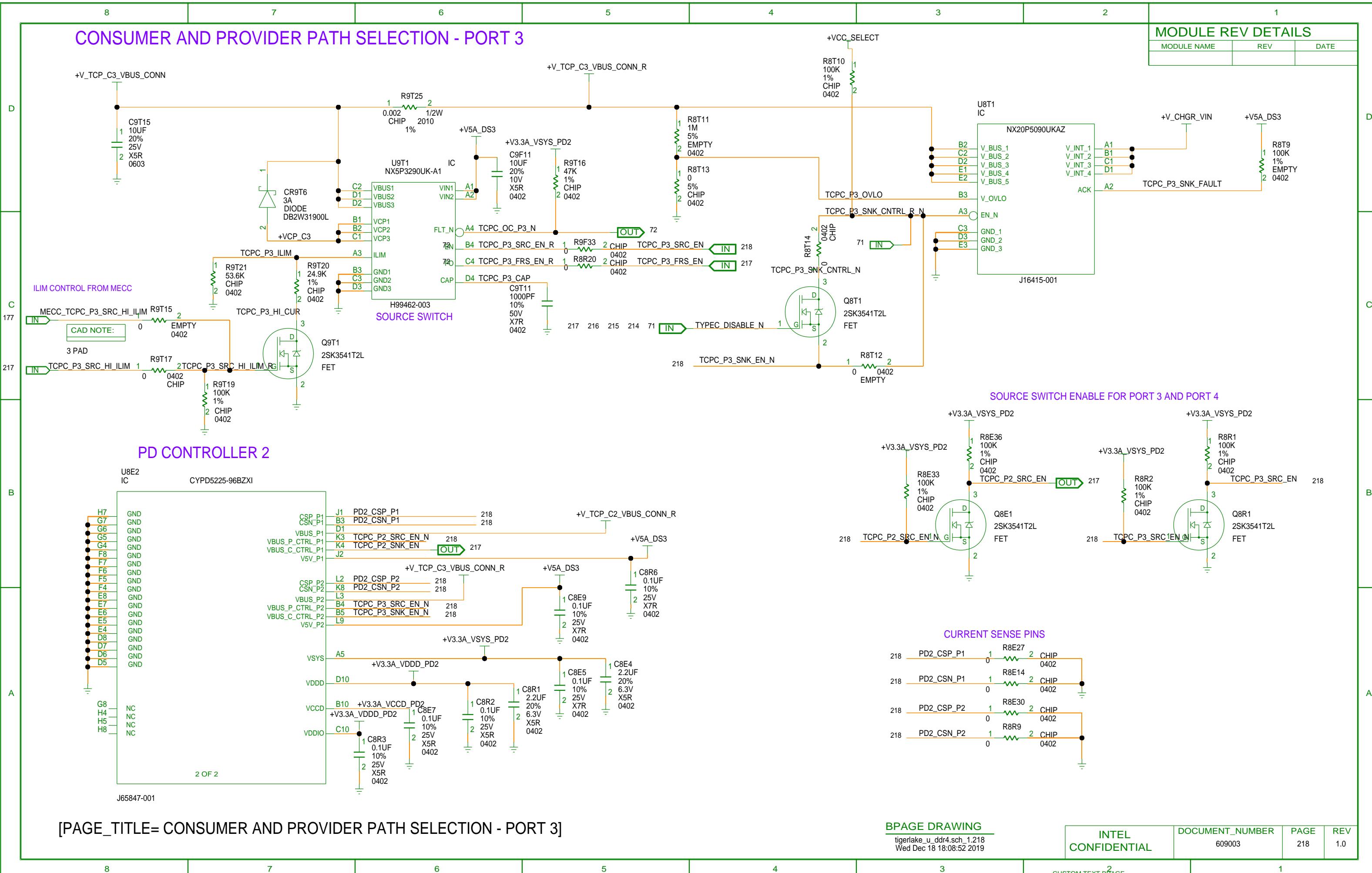
CONSUMER AND PROVIDER PATH SELECTION- PORT 1

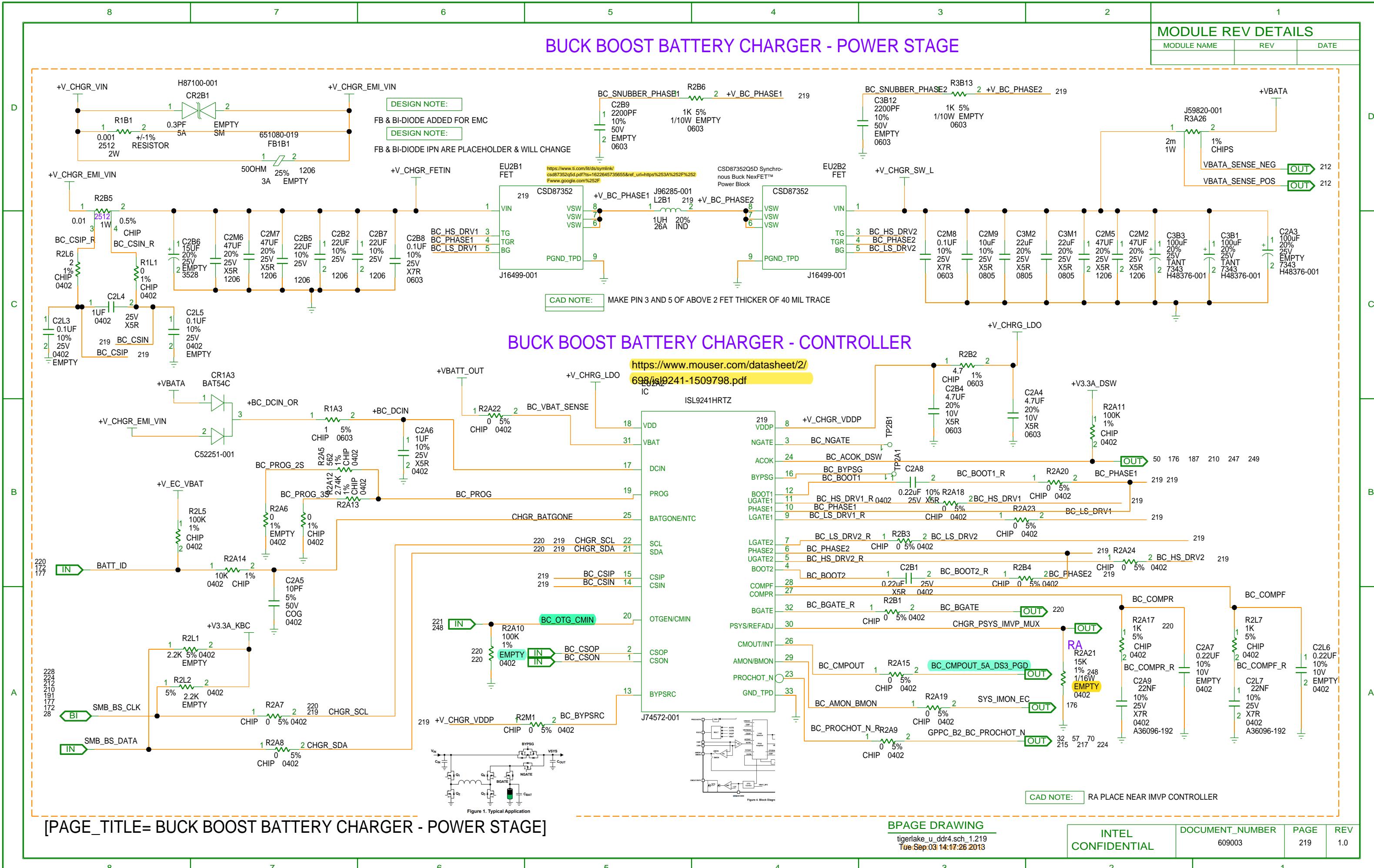
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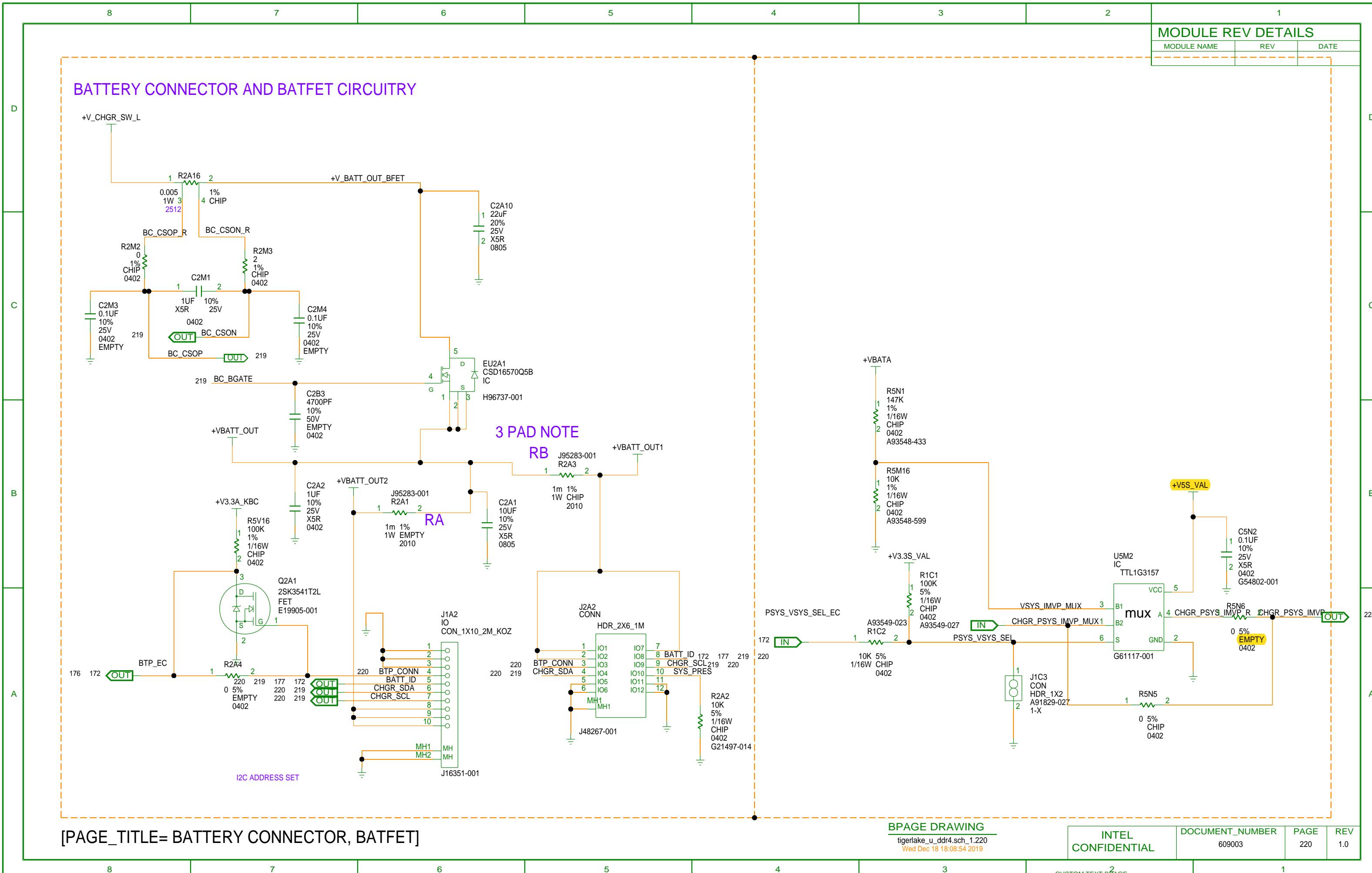
MODULE NAME	REV	DATE

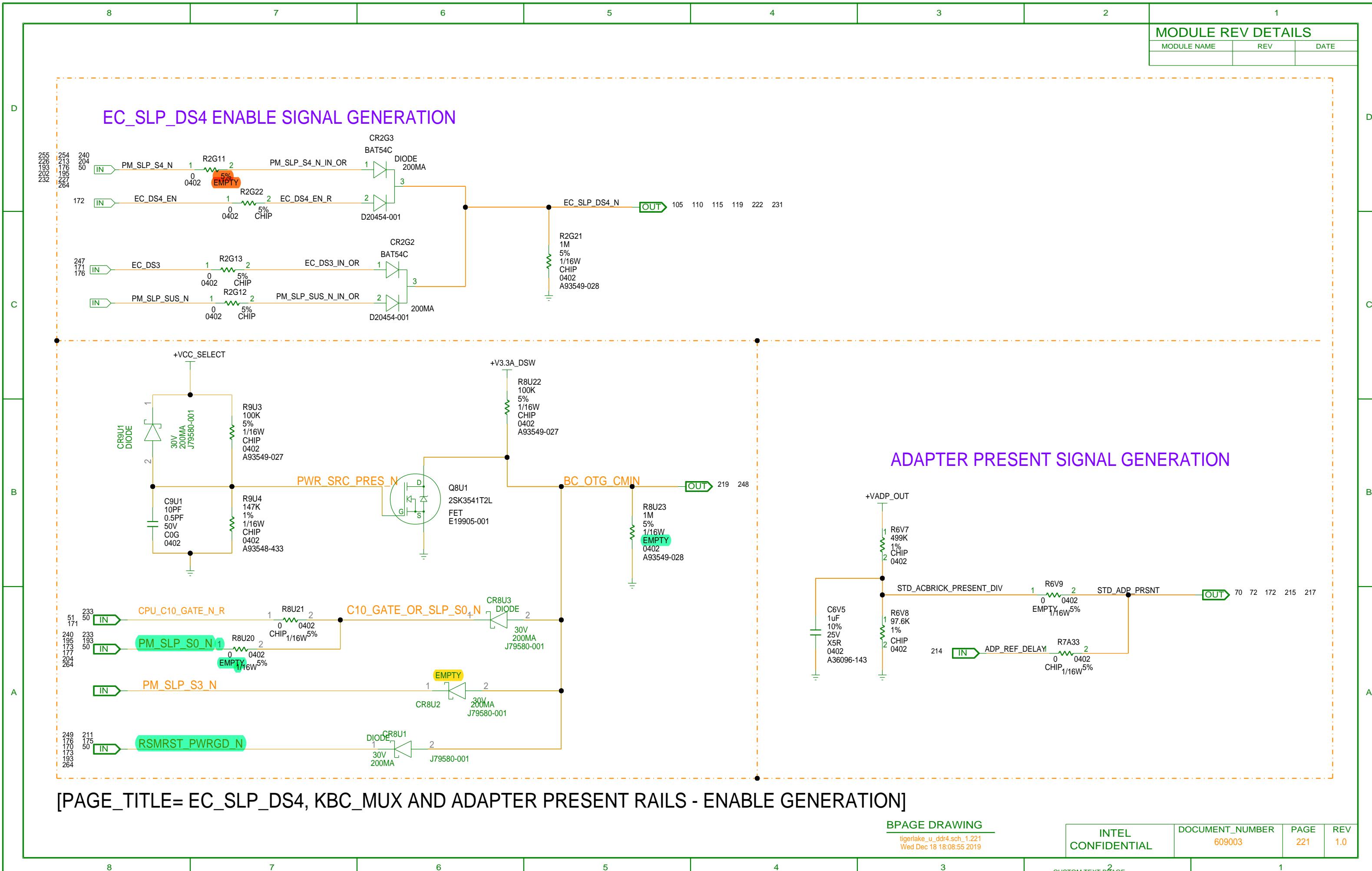


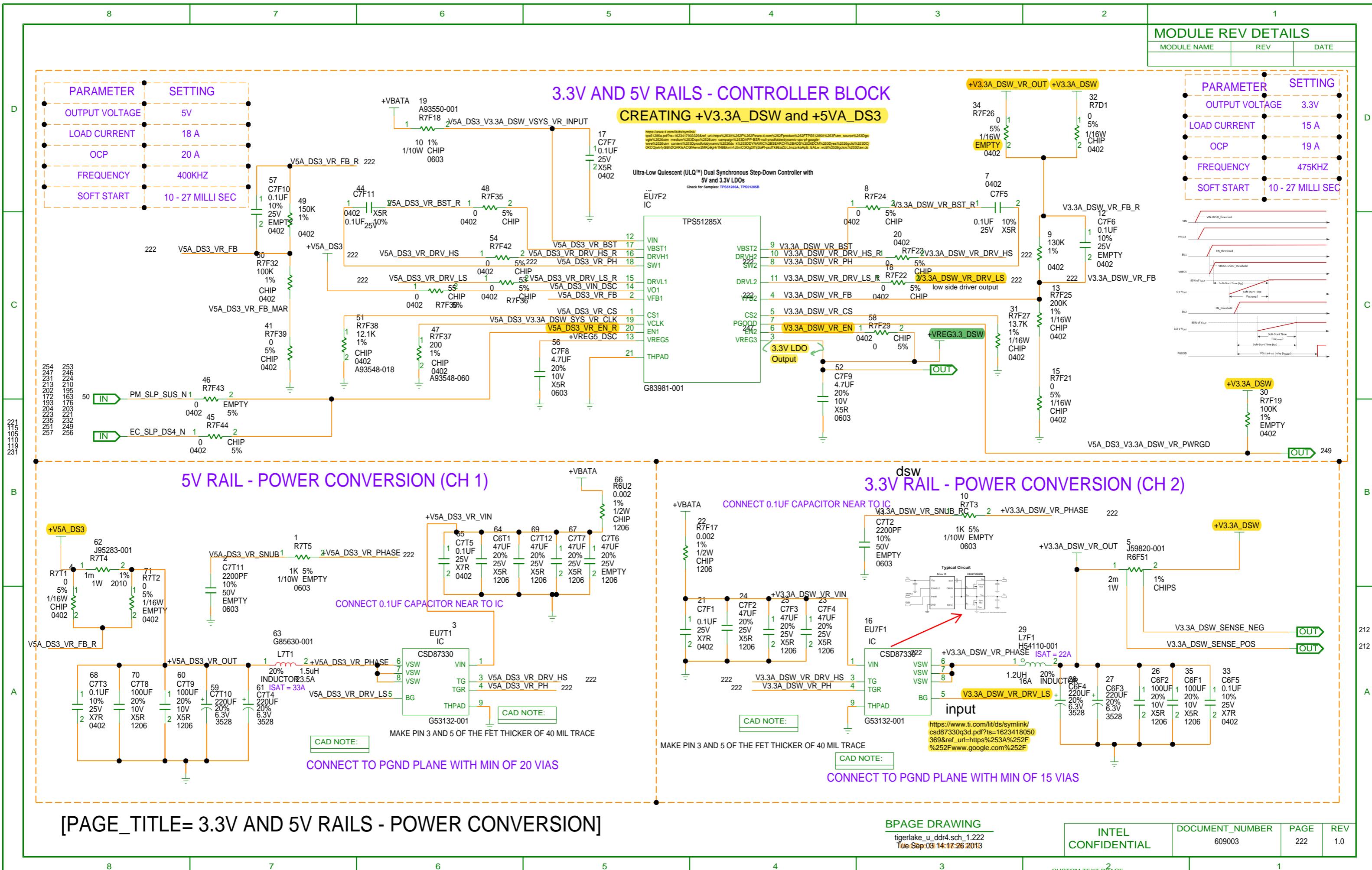


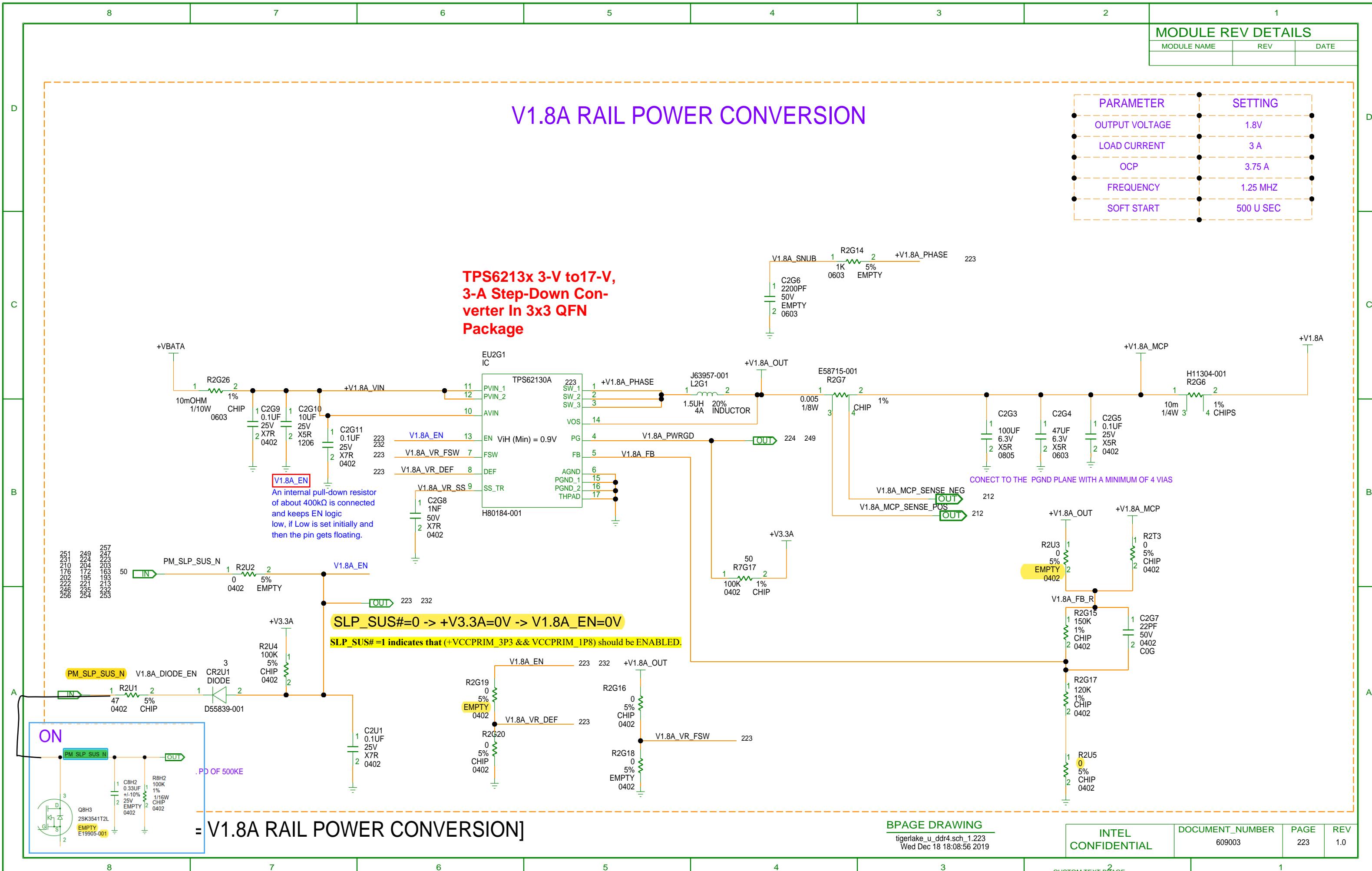


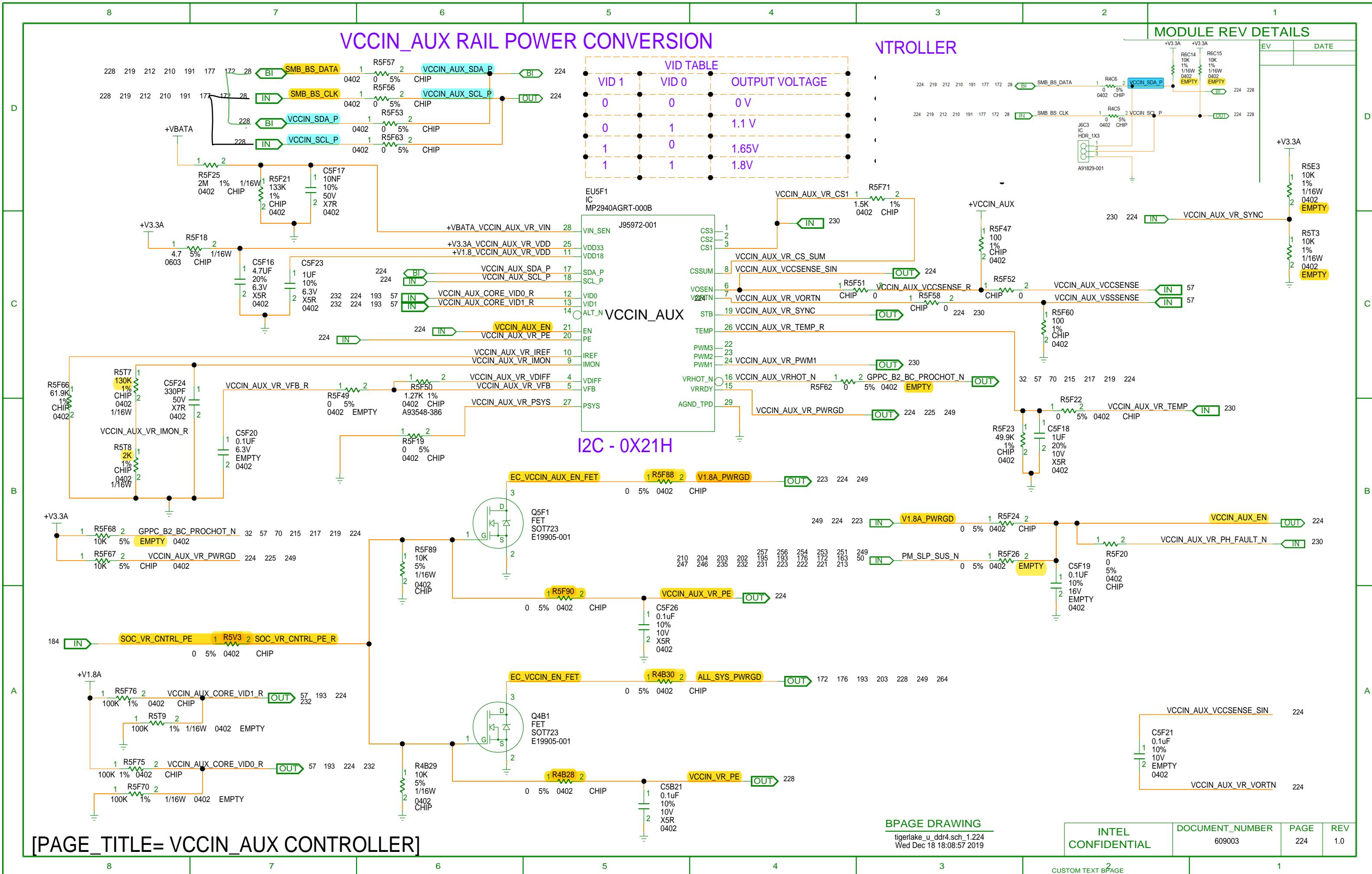


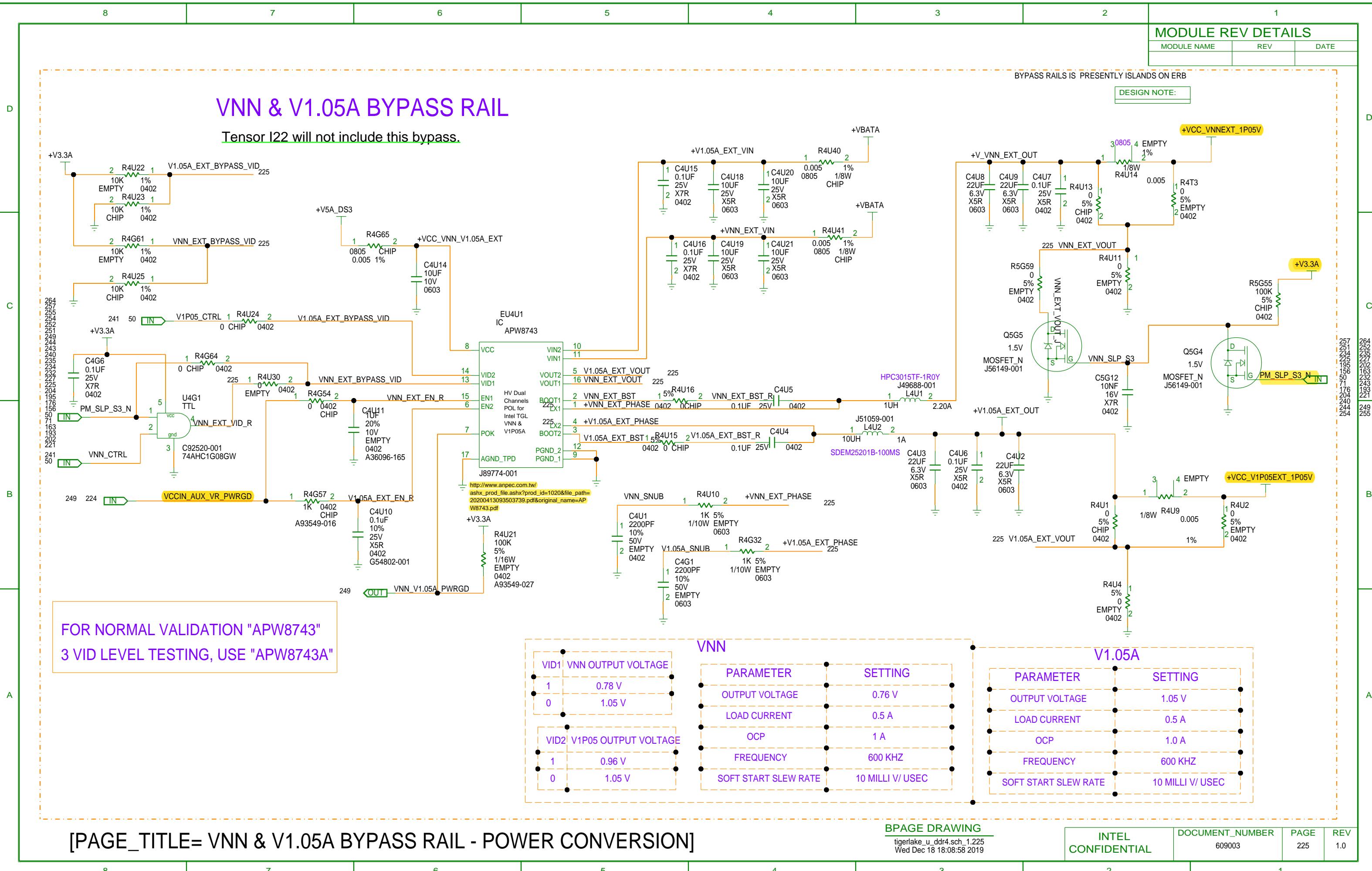


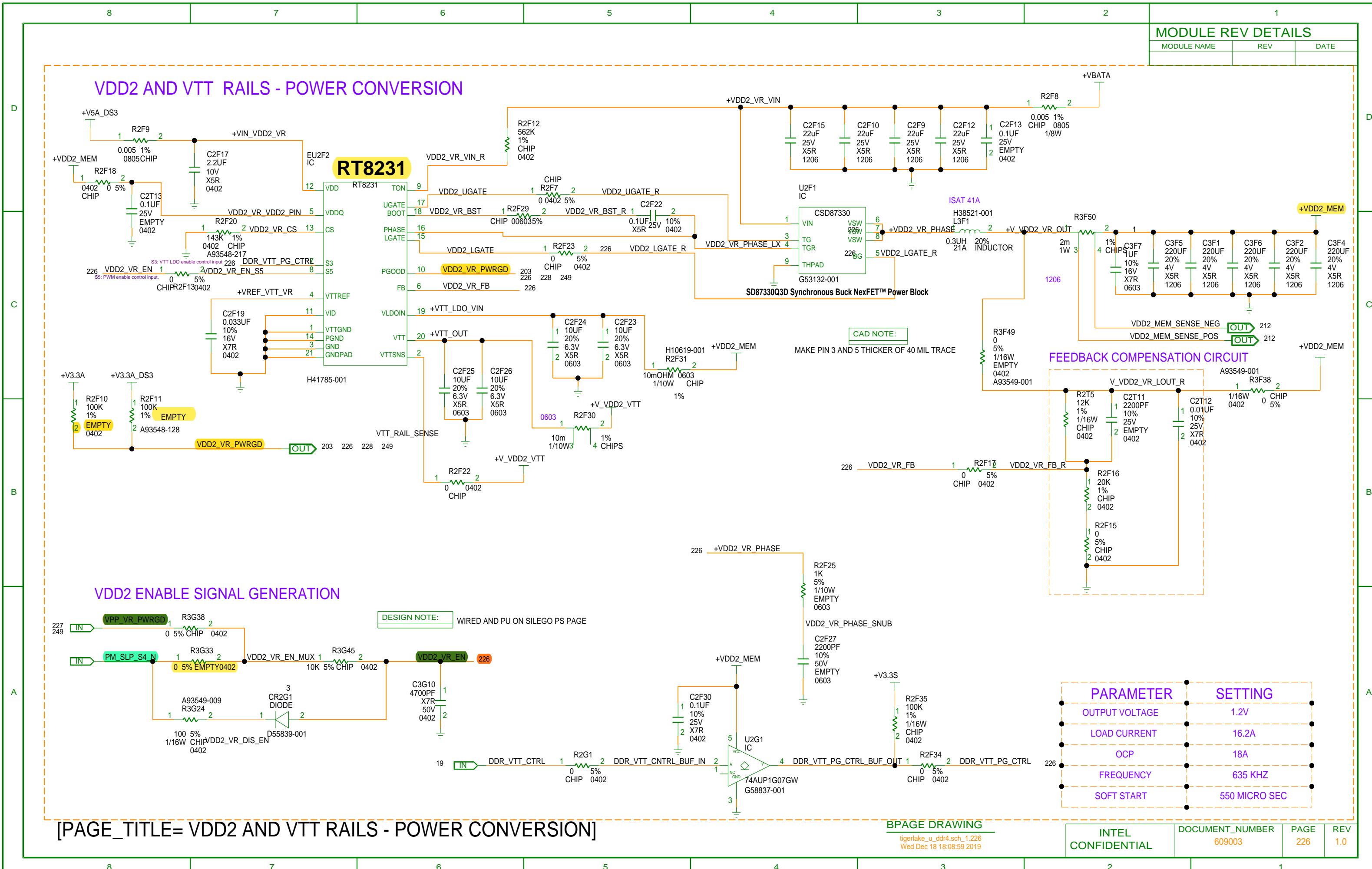


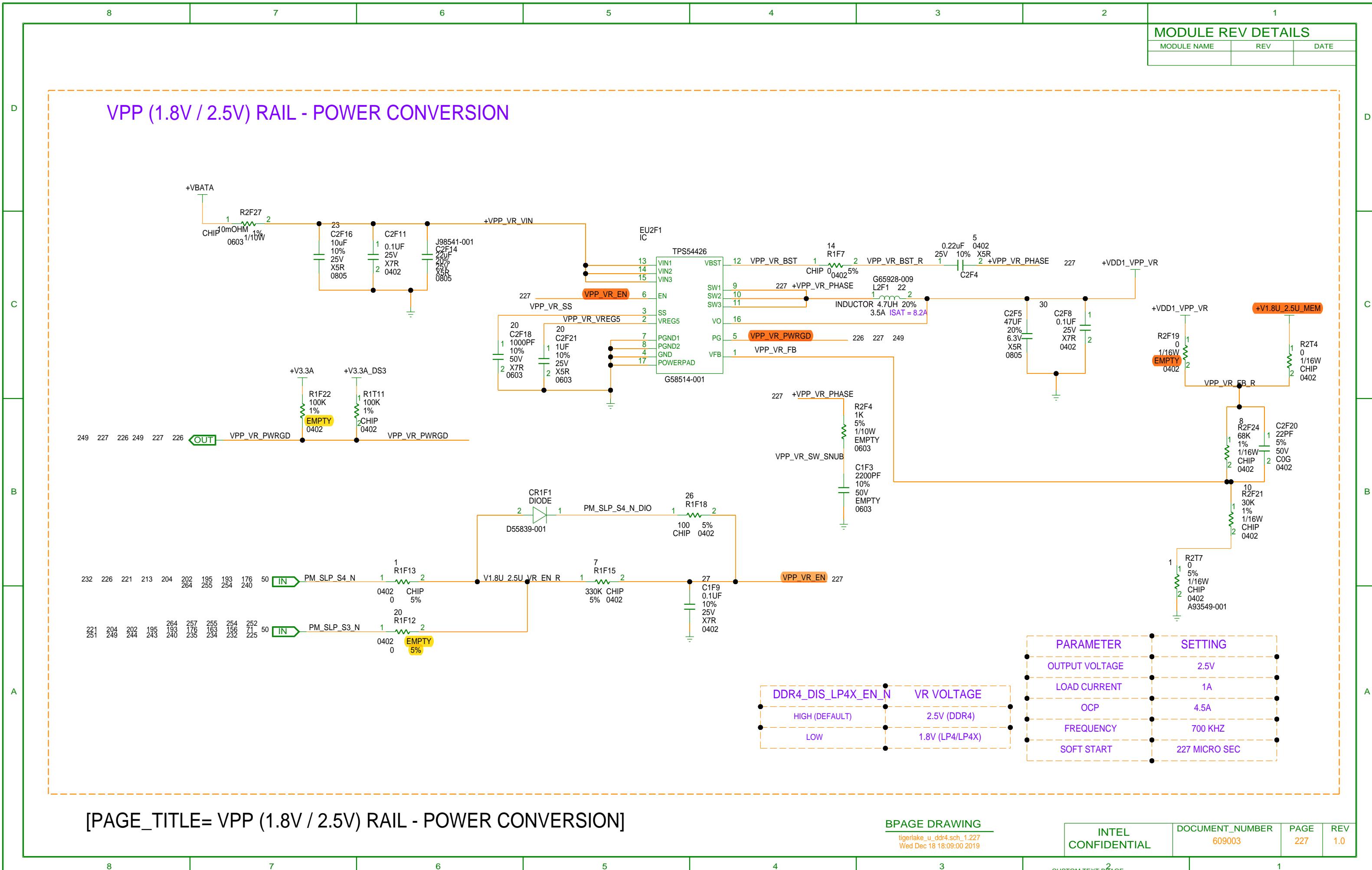


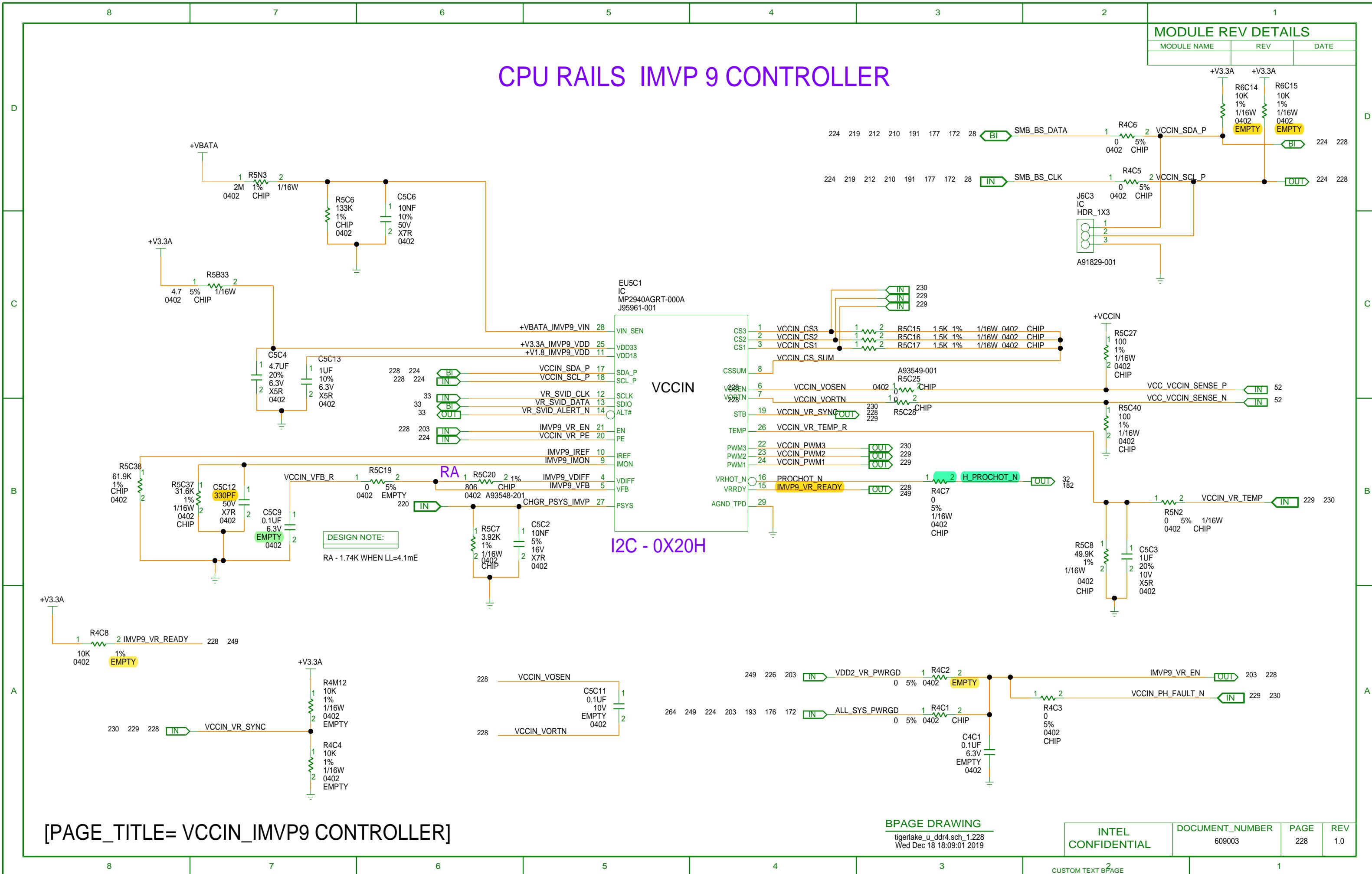


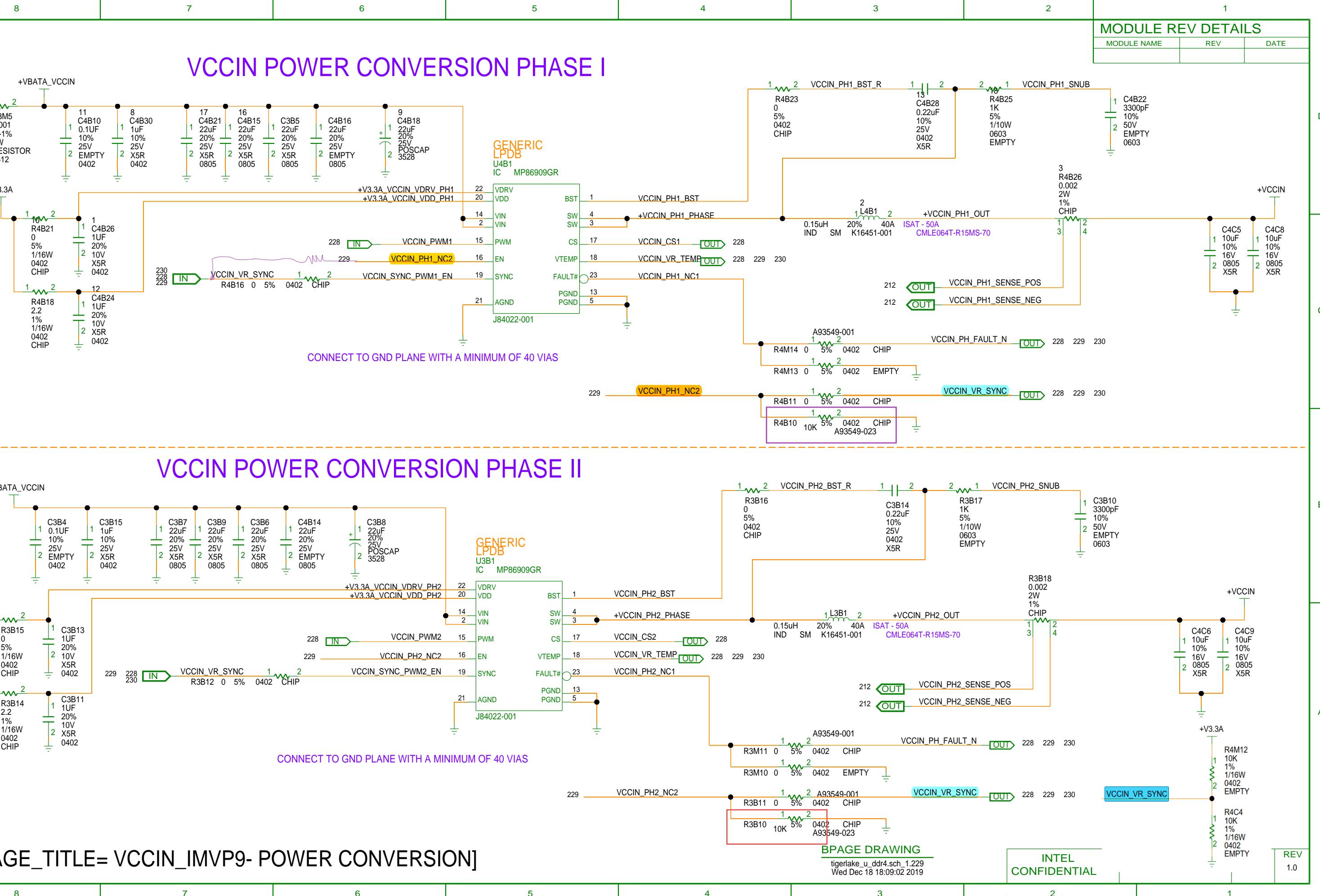








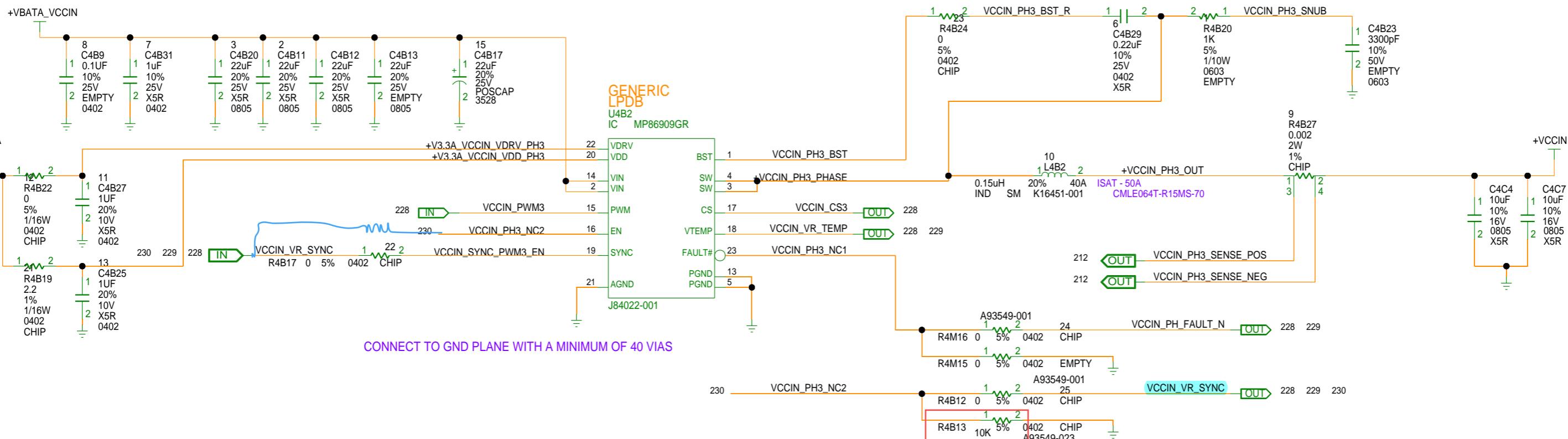




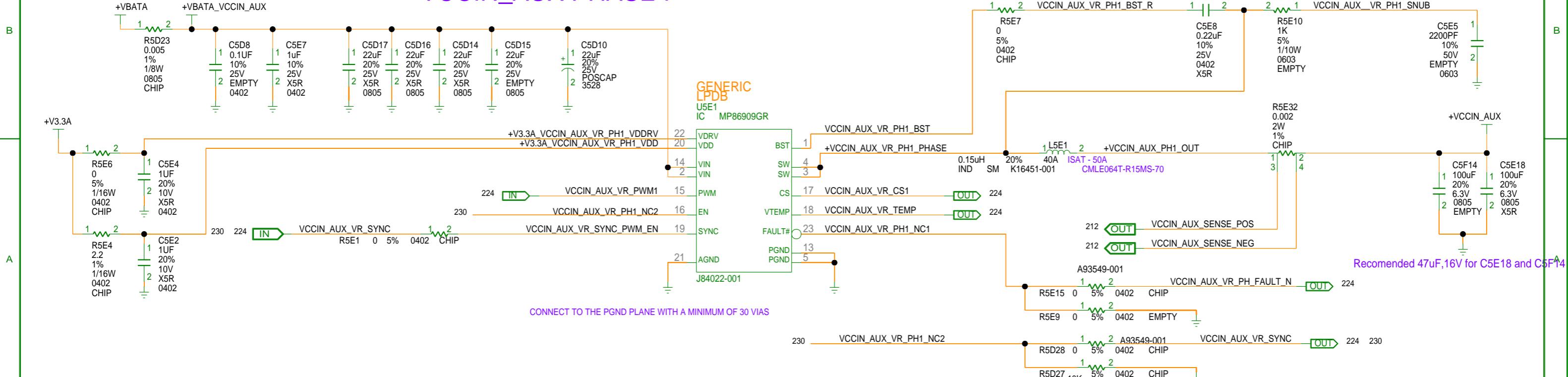
VCCIN POWER CONVERSION PHASE III

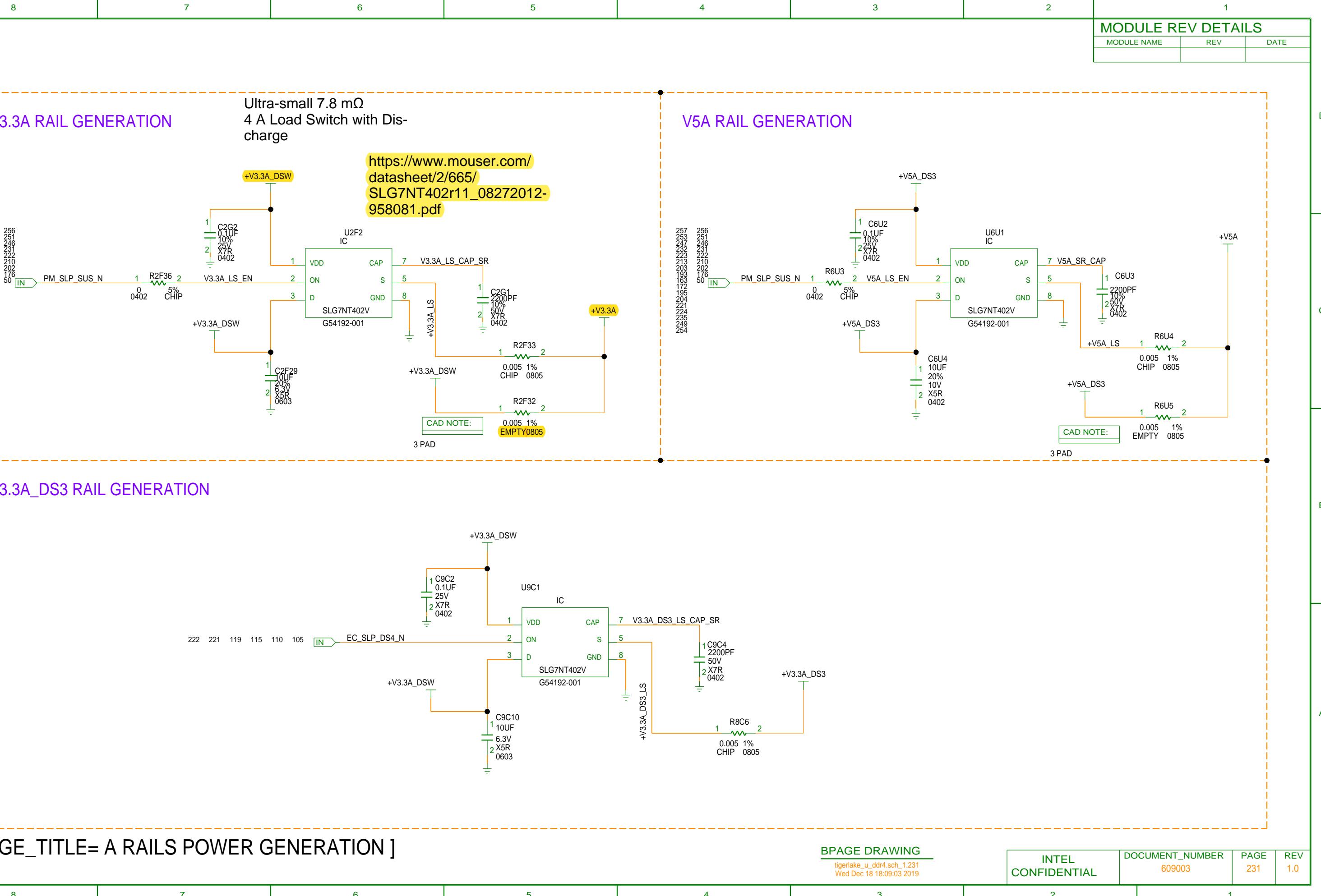
MODULE REV DETAILS

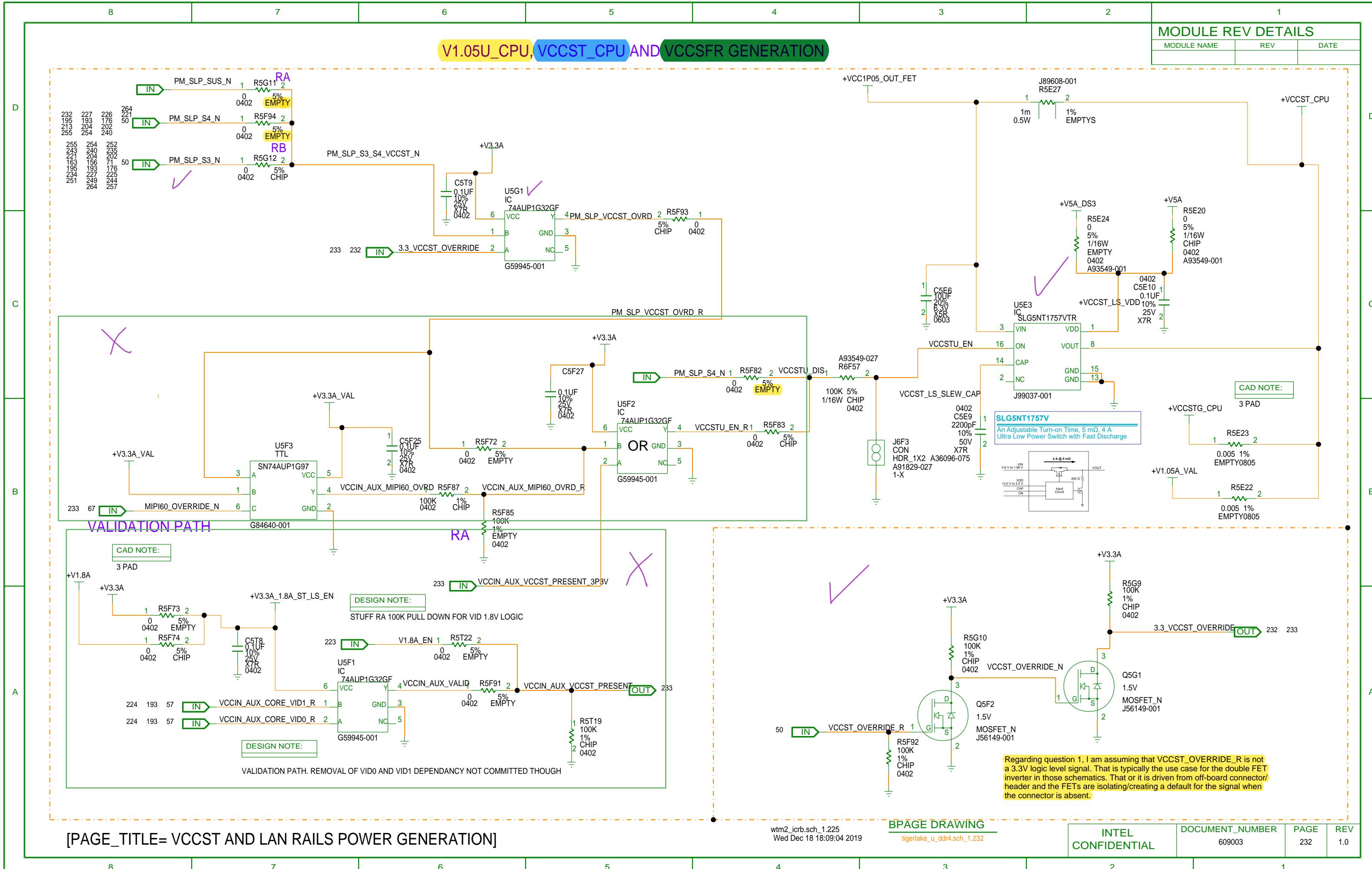
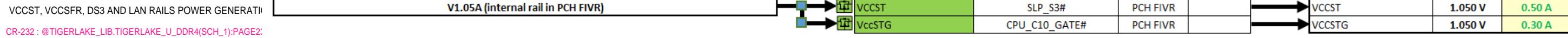
MODULE NAME	REV	DATE

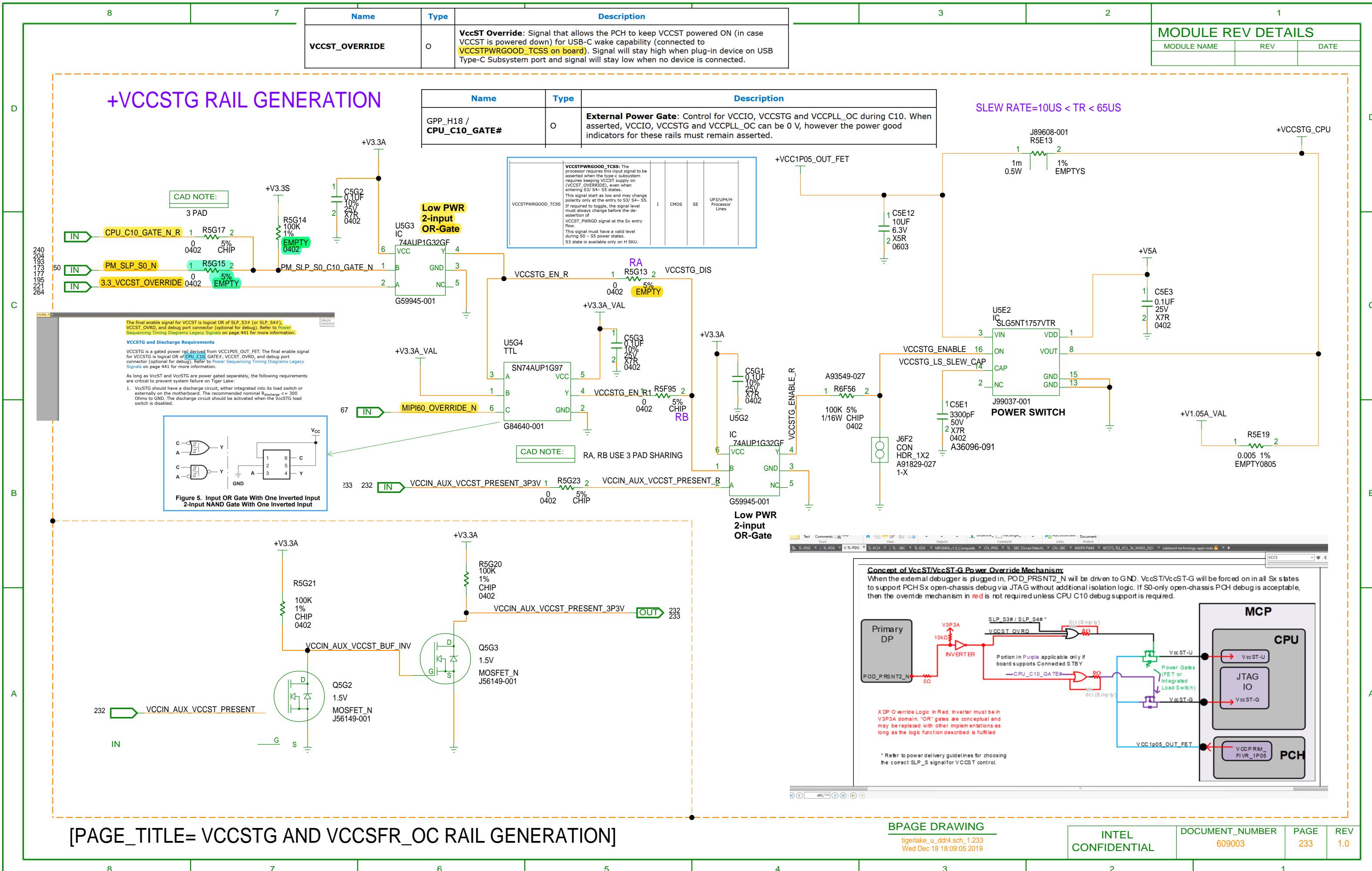


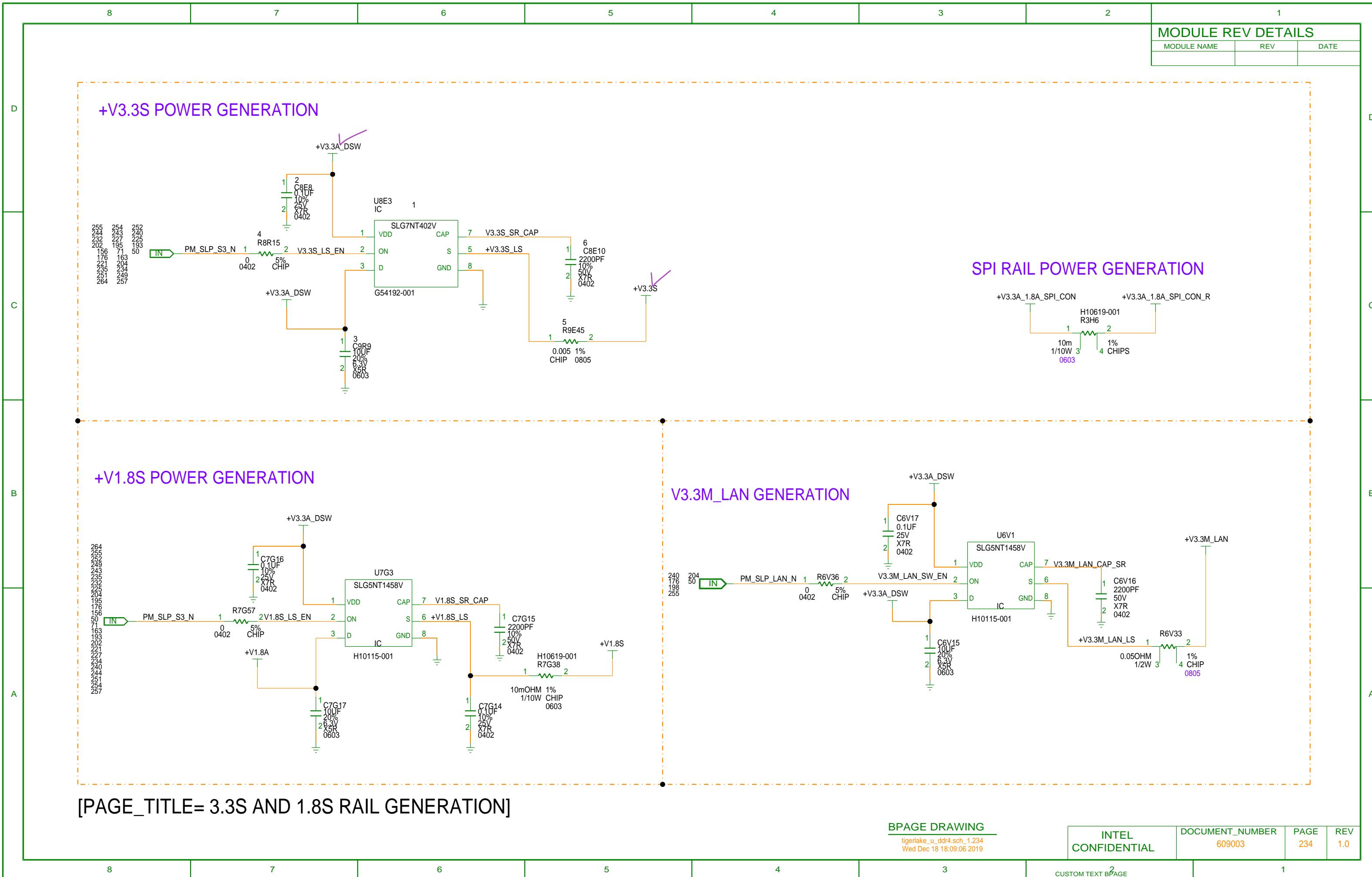
VCCIN_AUX PHASE I







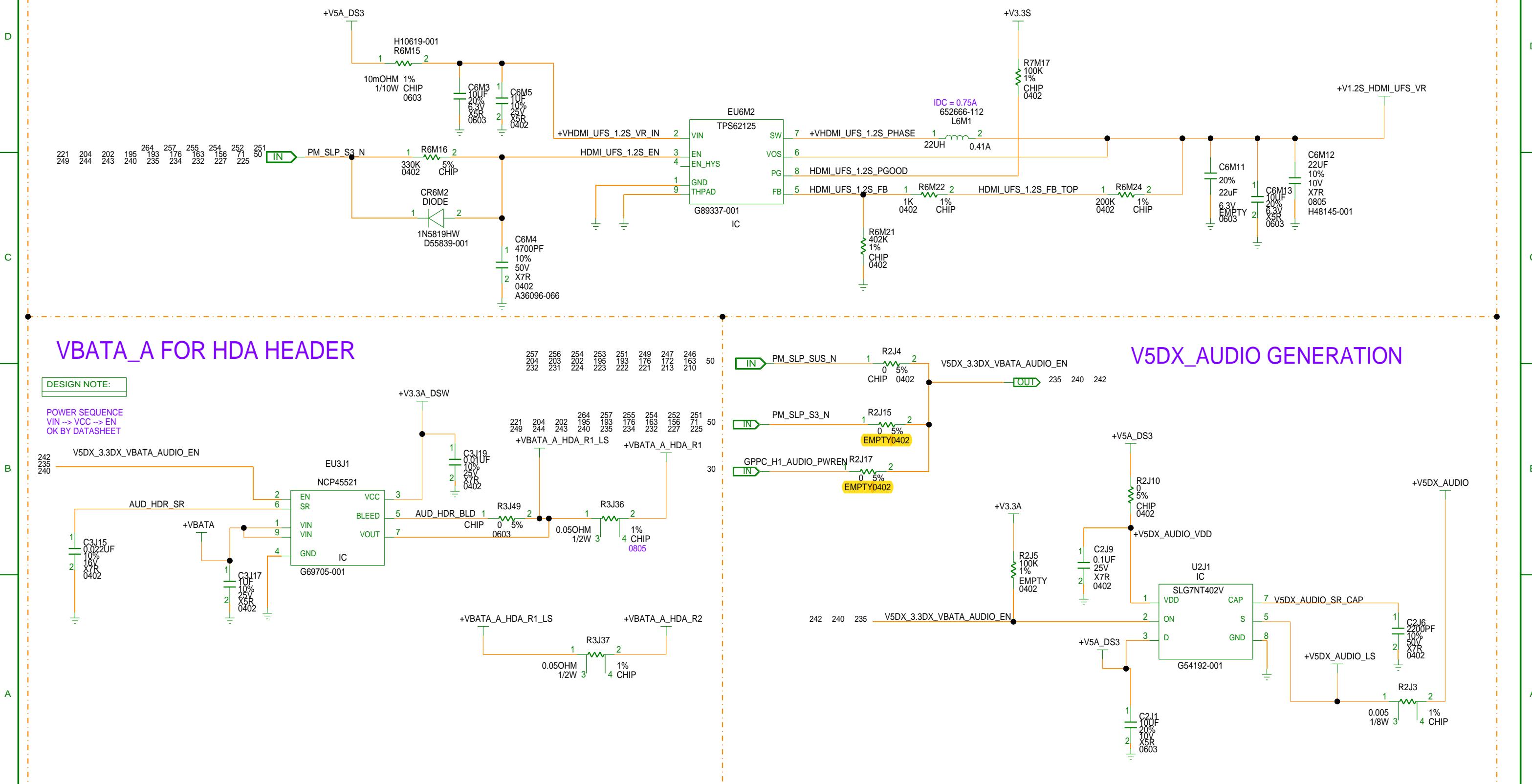




1.2V RAIL FOR HDMI AND UFS - POWER CONVERSION

MODULE REV DETAILS

MODULE NAME	REV	DATE



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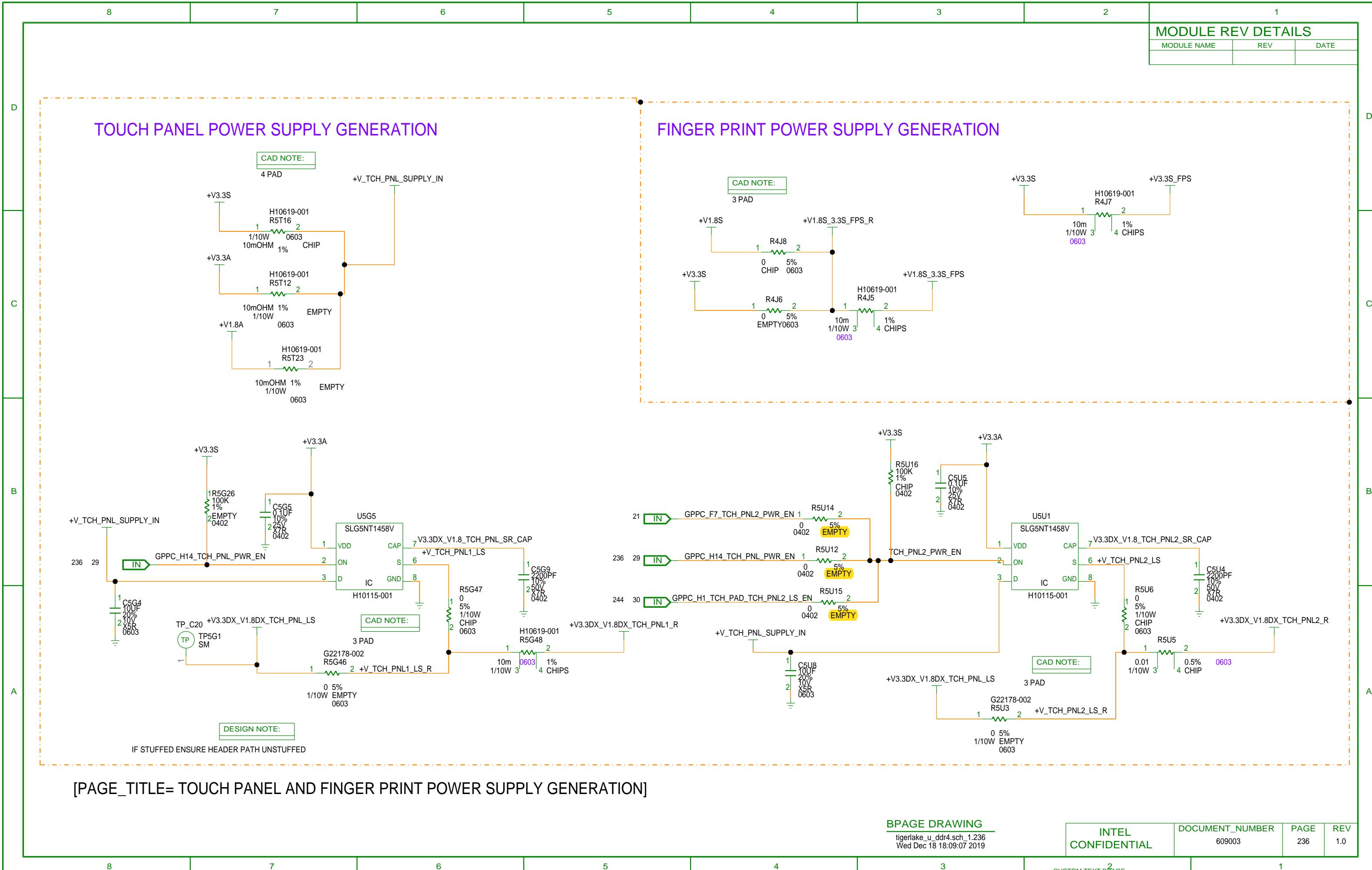
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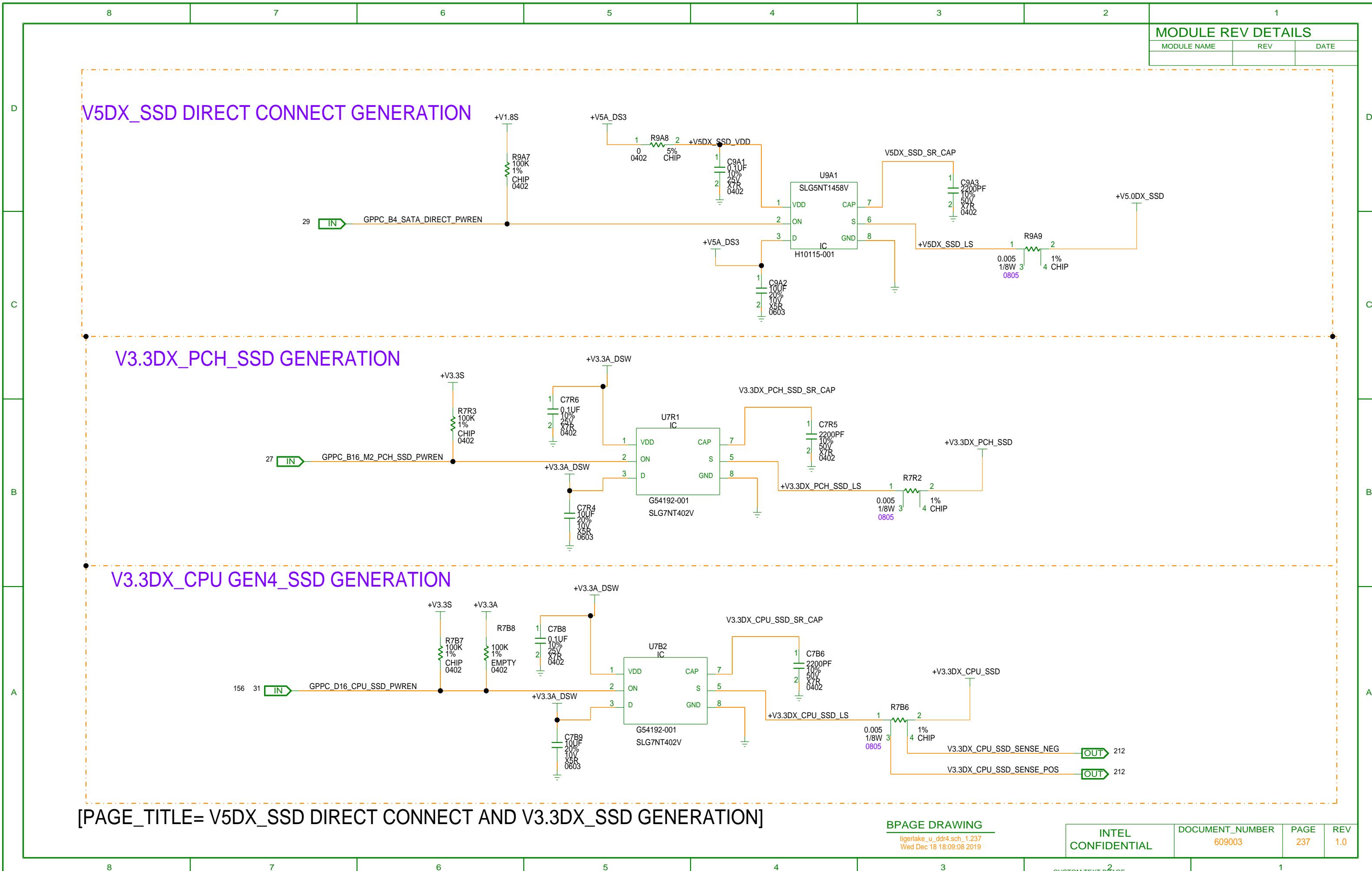
tigerlake_u_ddr4.sch_1235
Wed Dec 18 18:09:07 2019

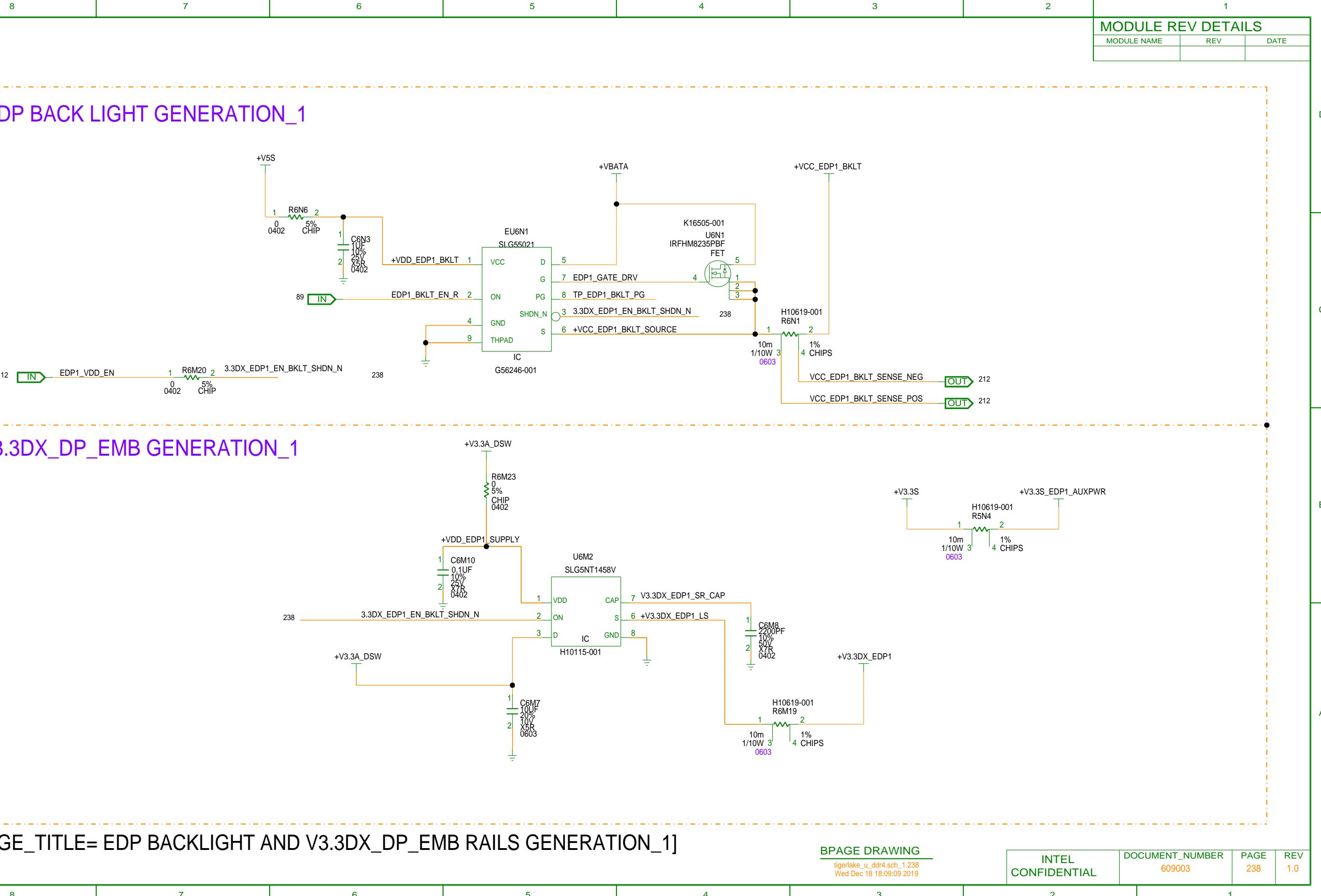
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	235	1.0

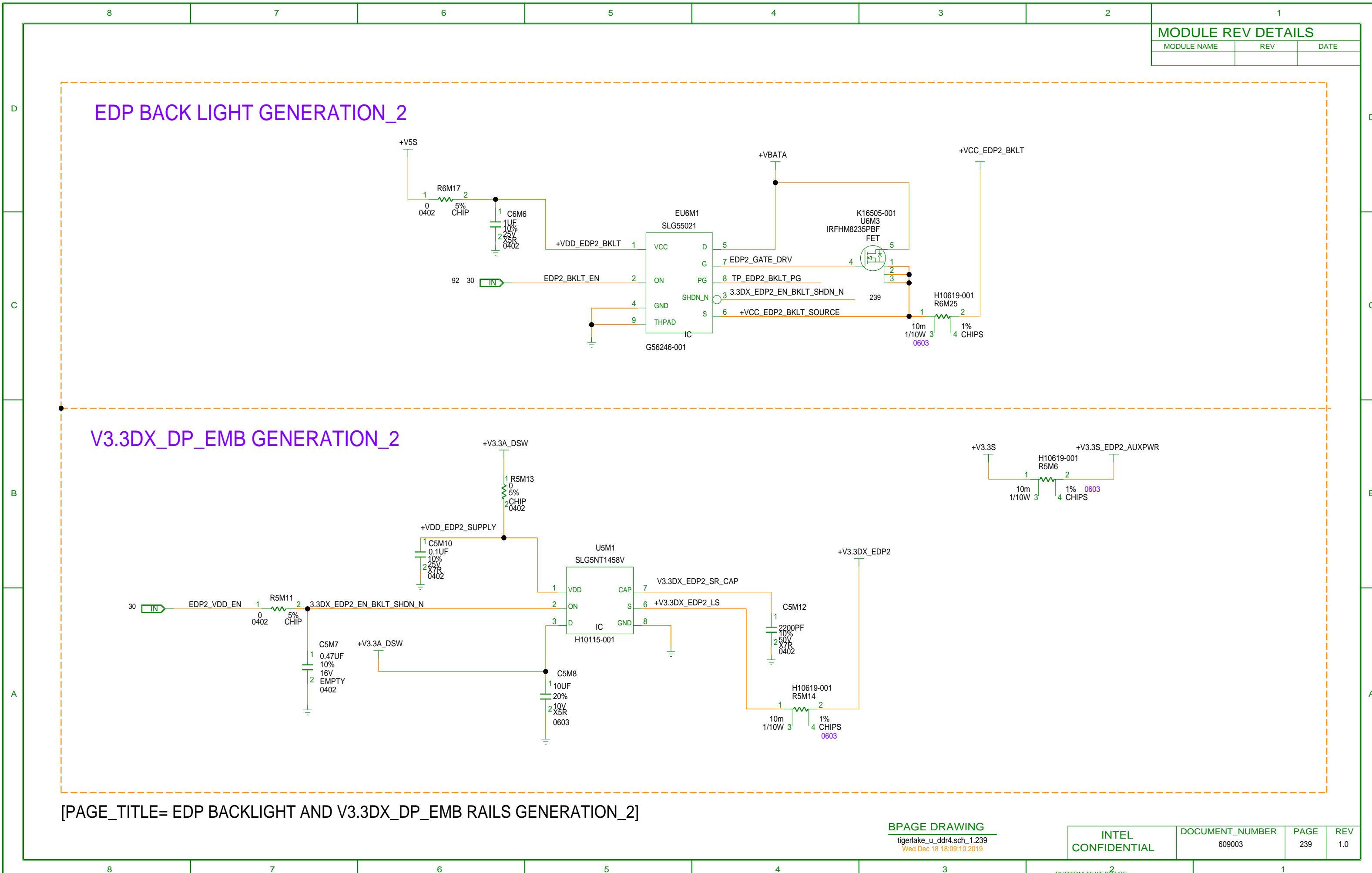
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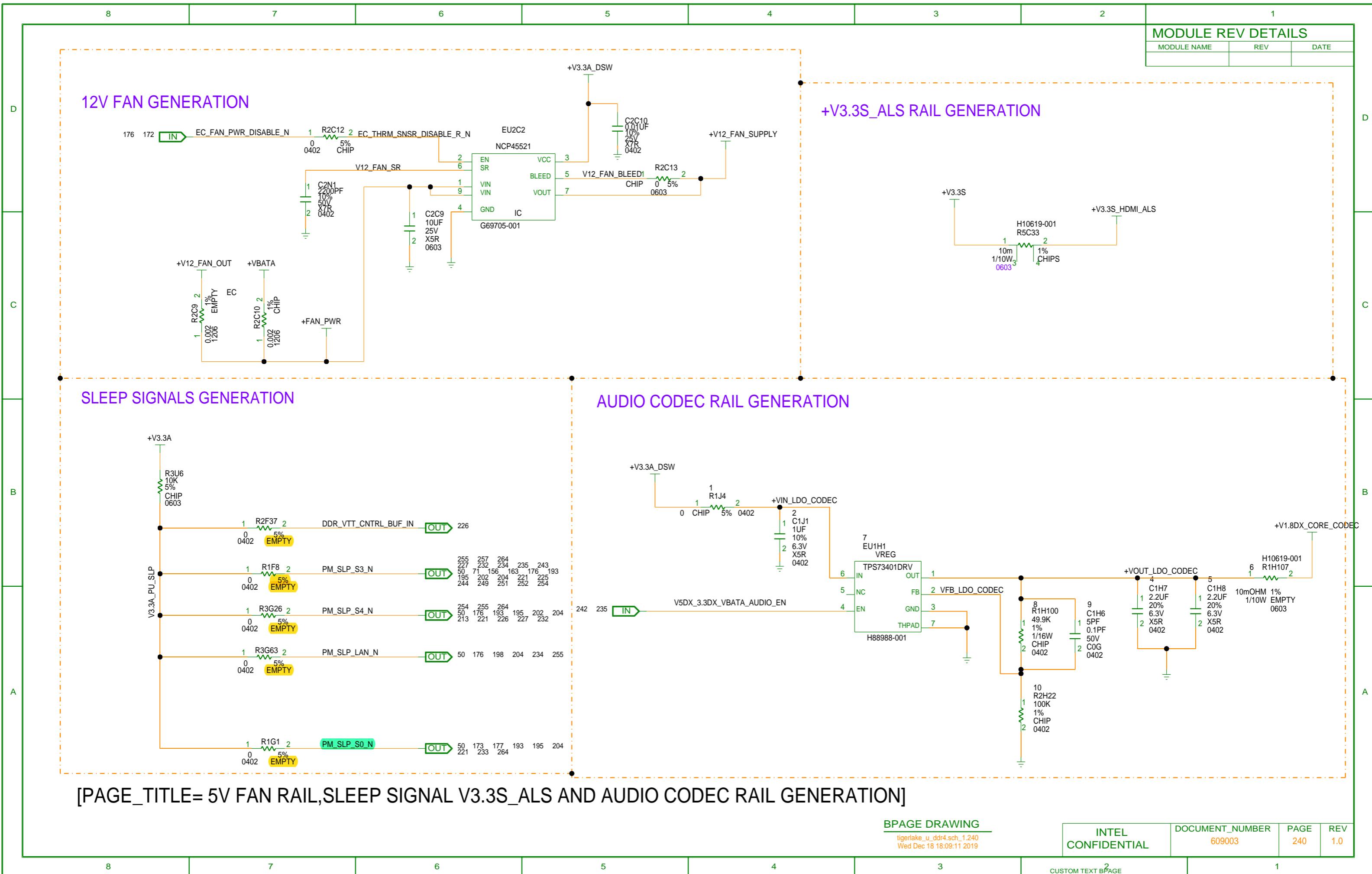
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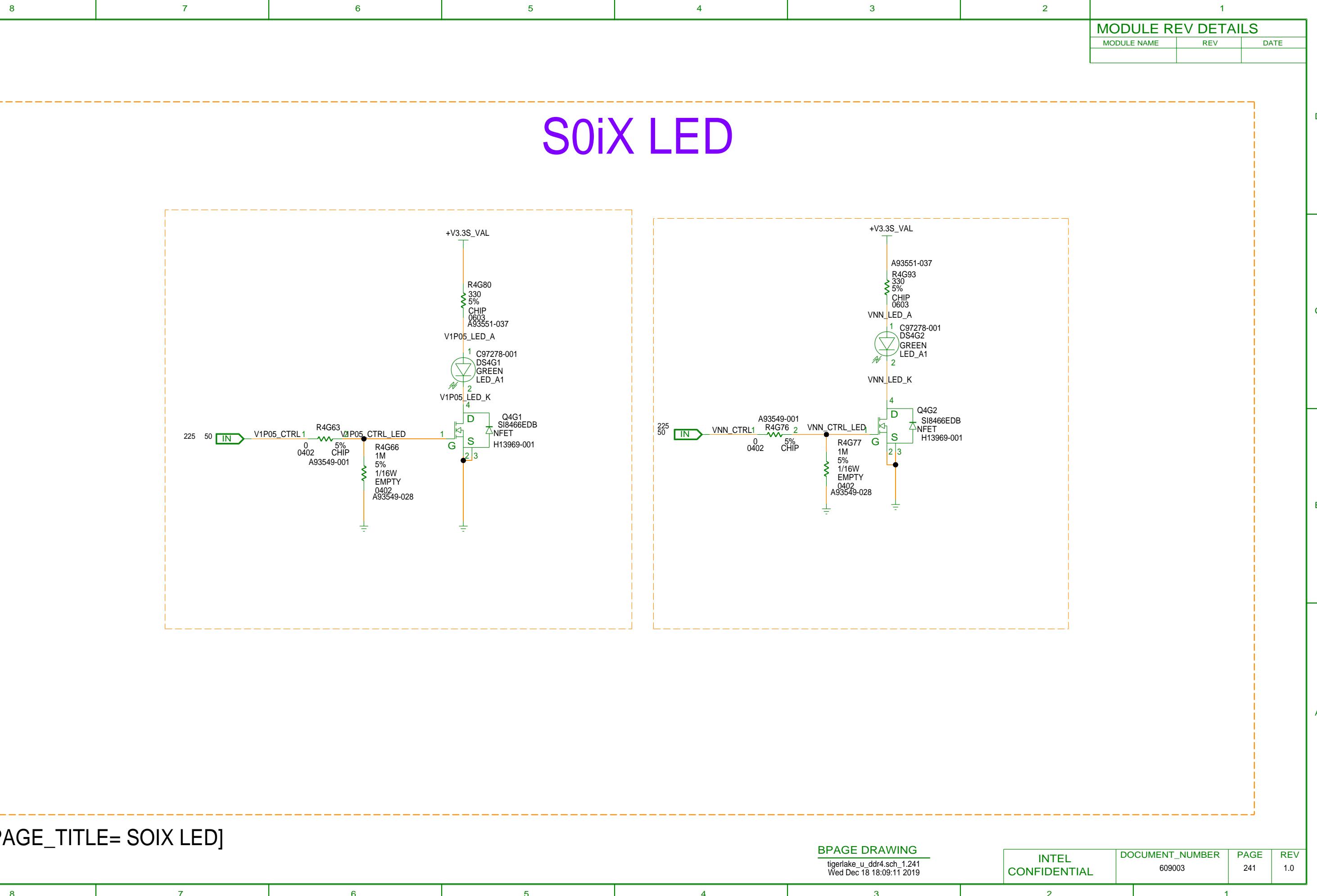


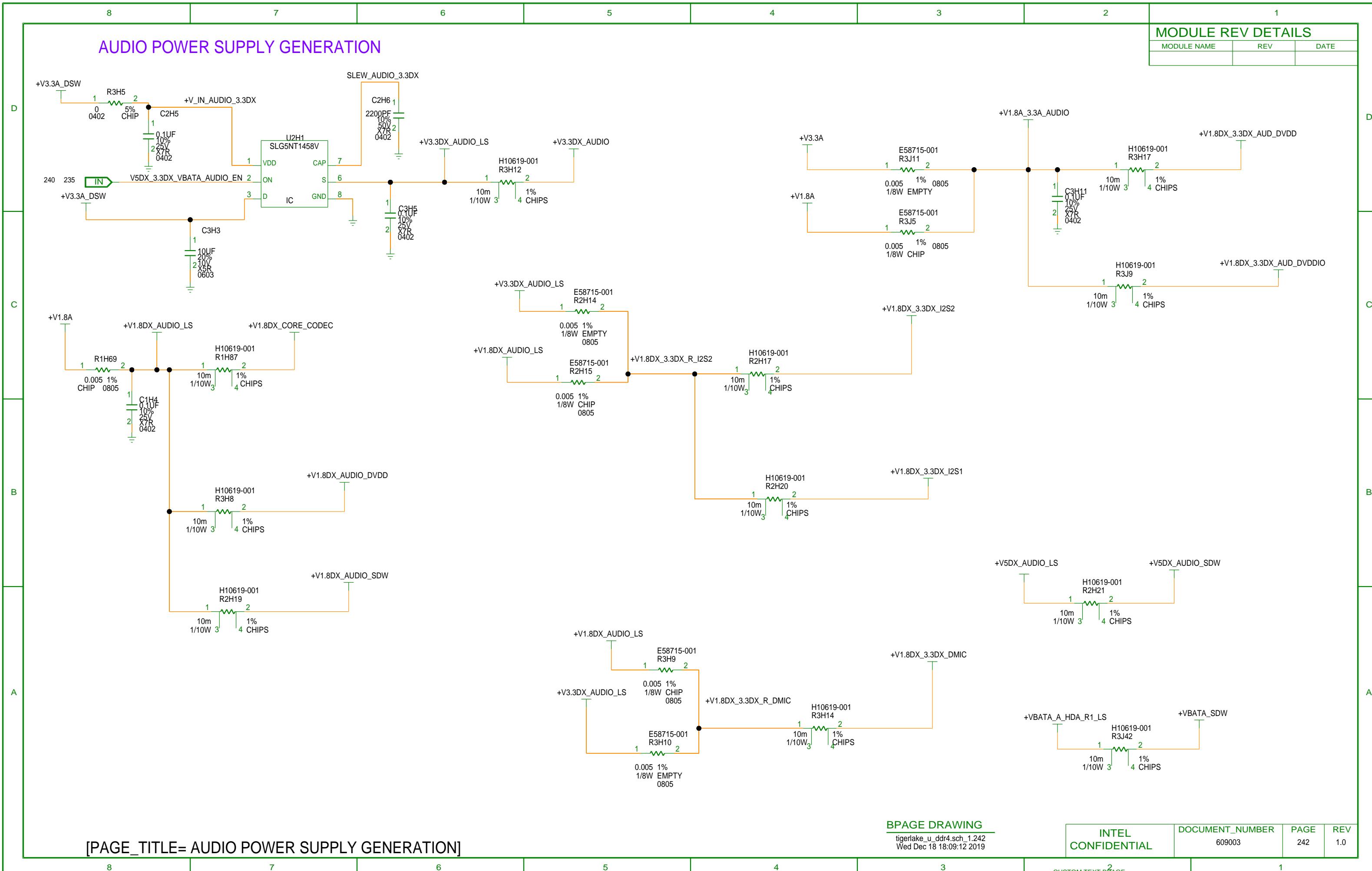


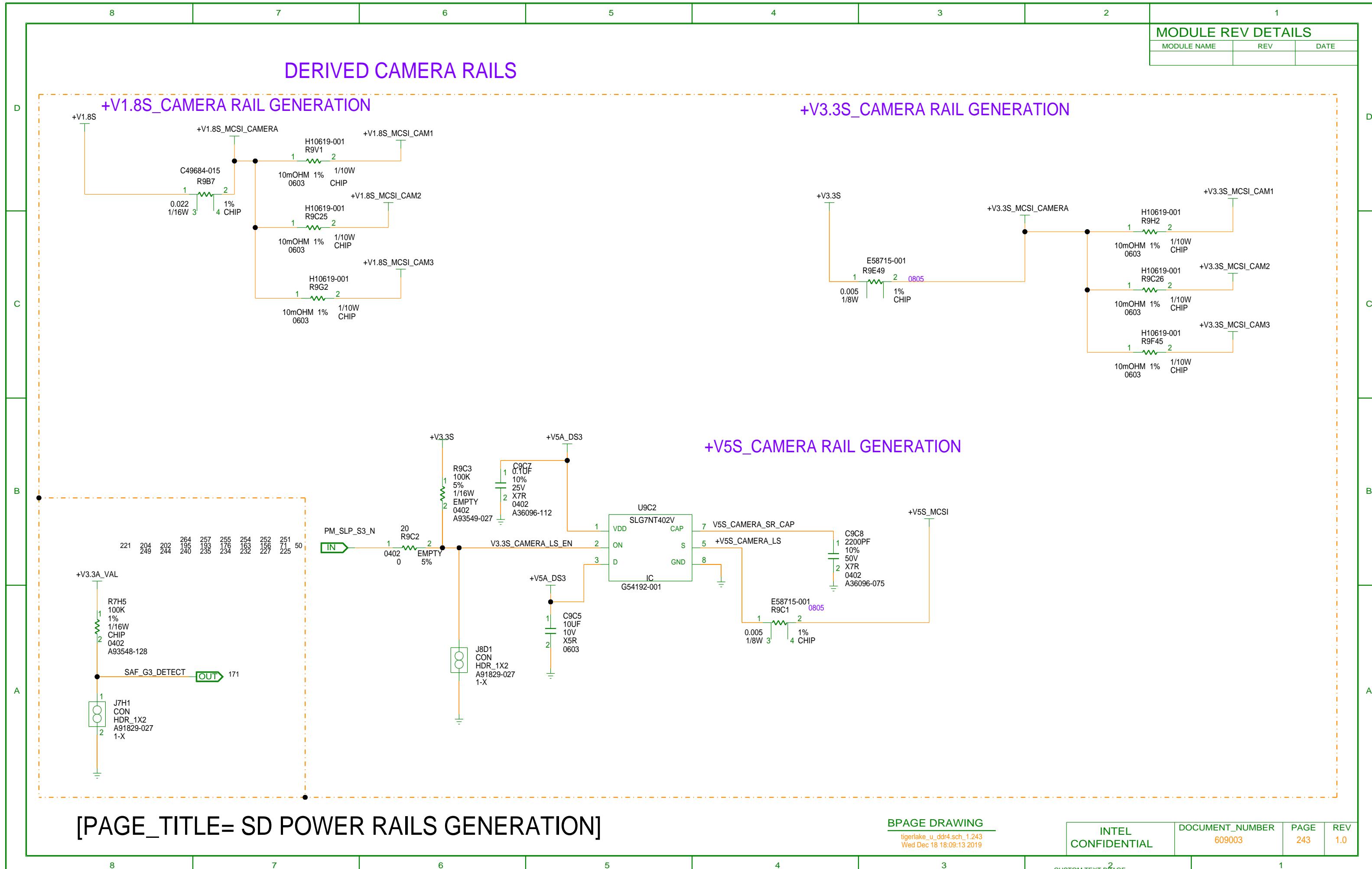


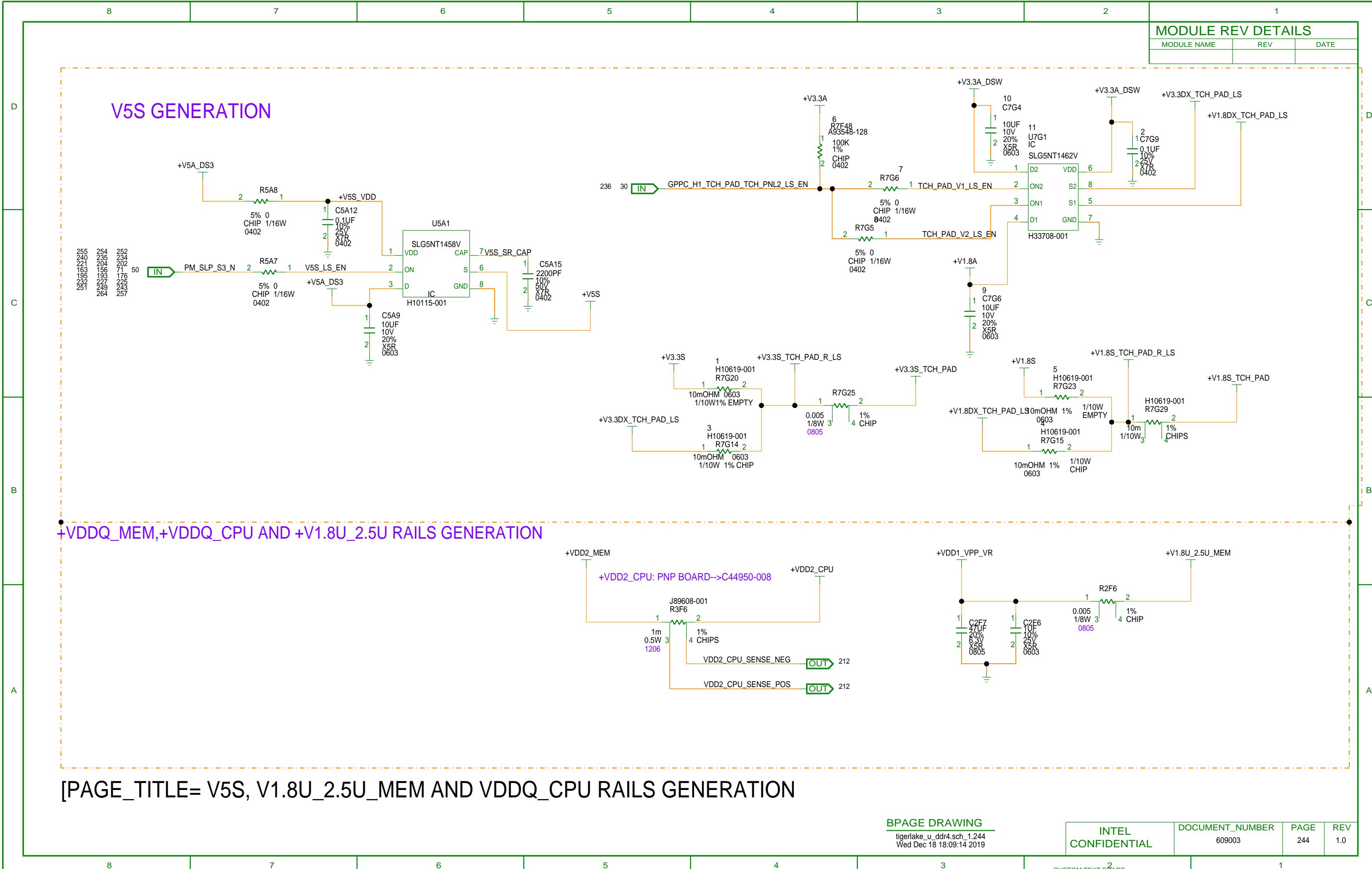






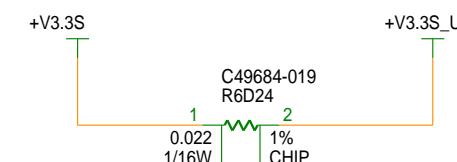
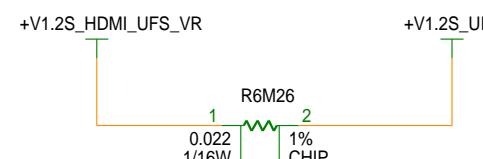
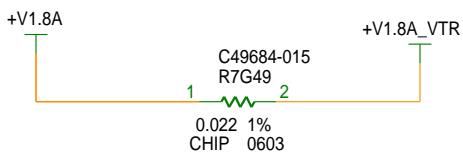
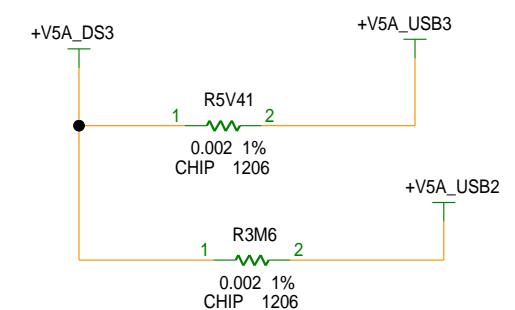
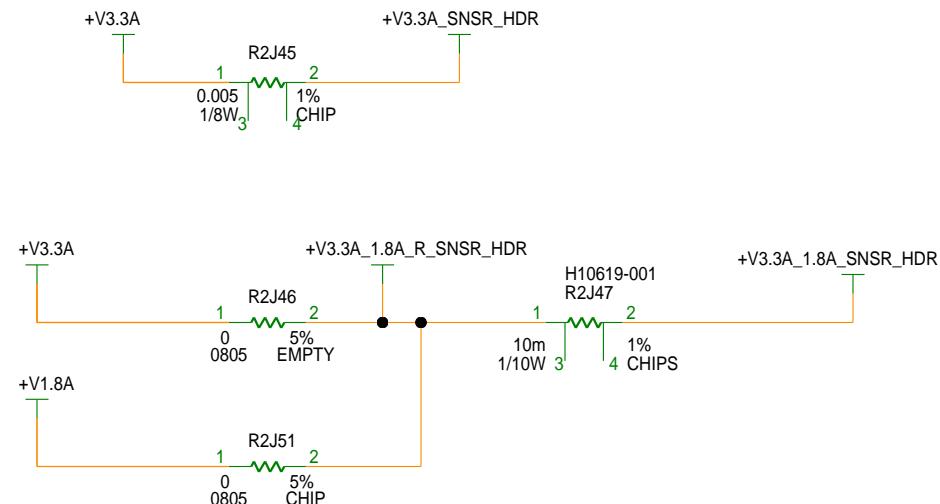
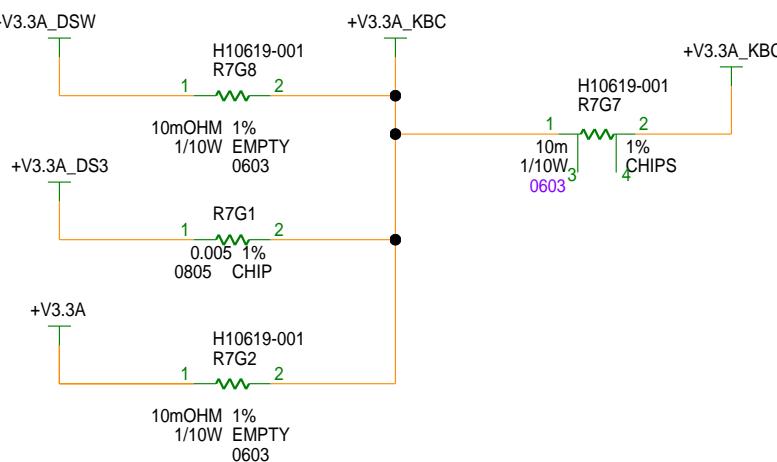


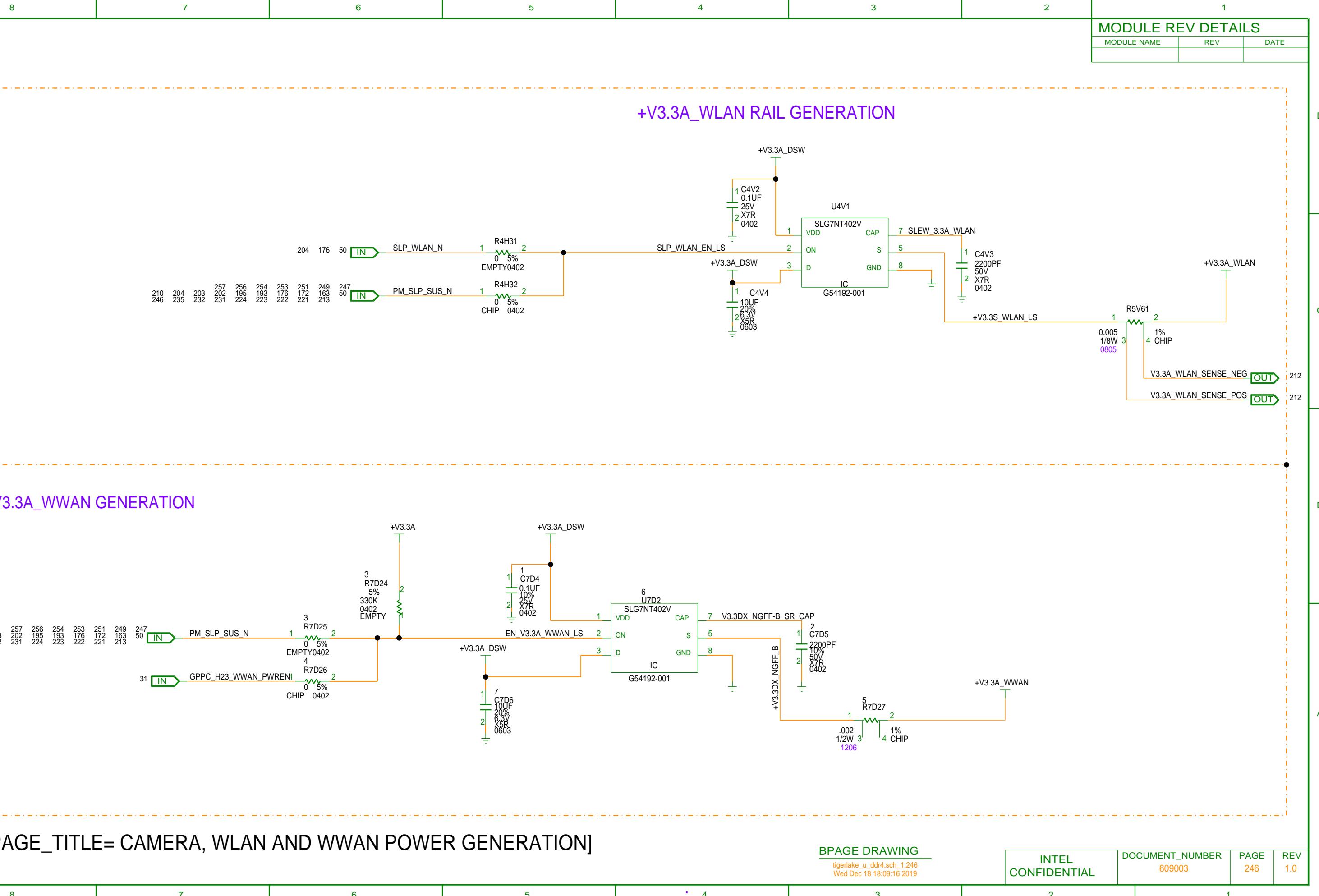


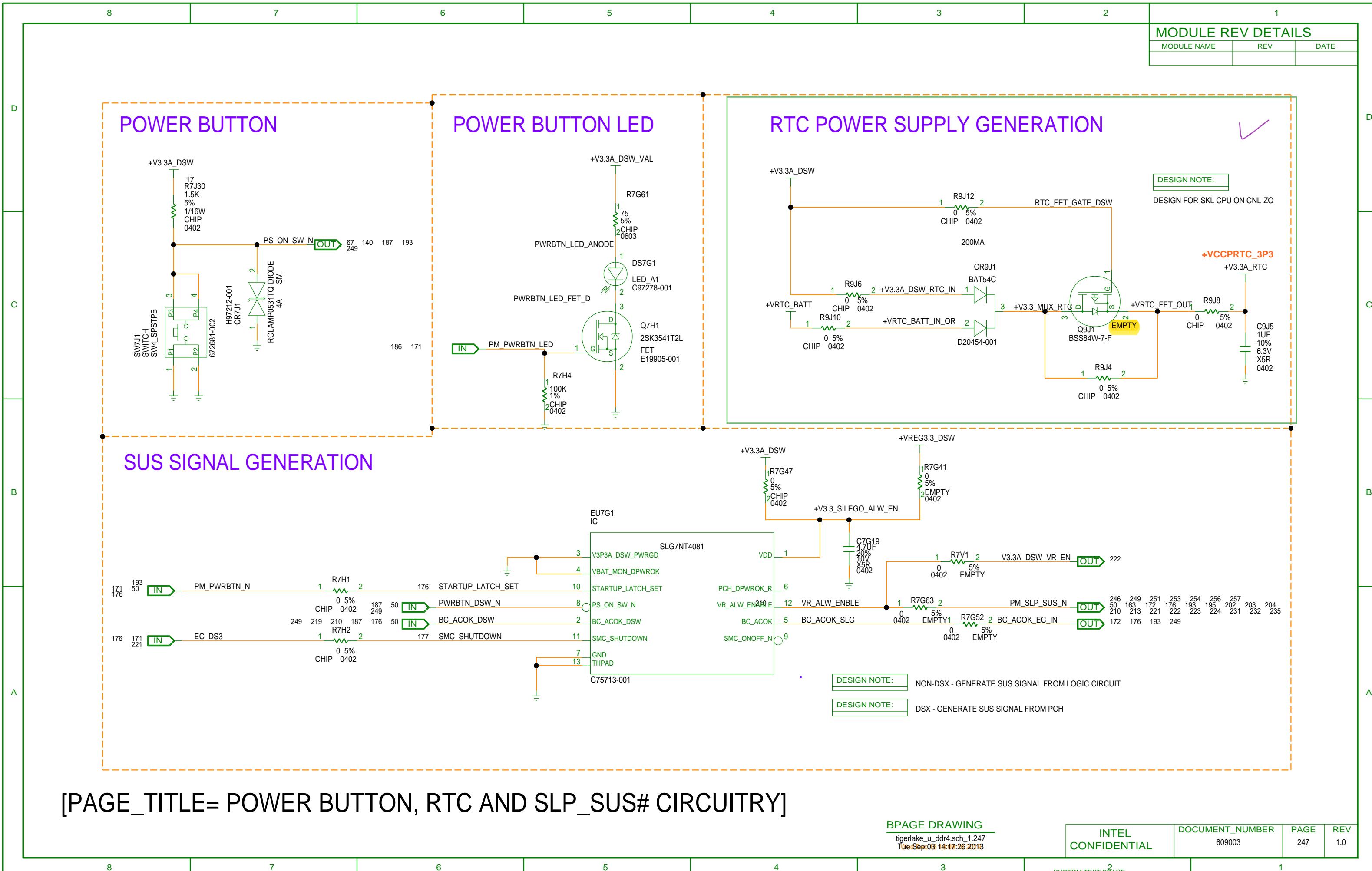


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MODULE REV DETAILS							

DERIVED POWER RAILS

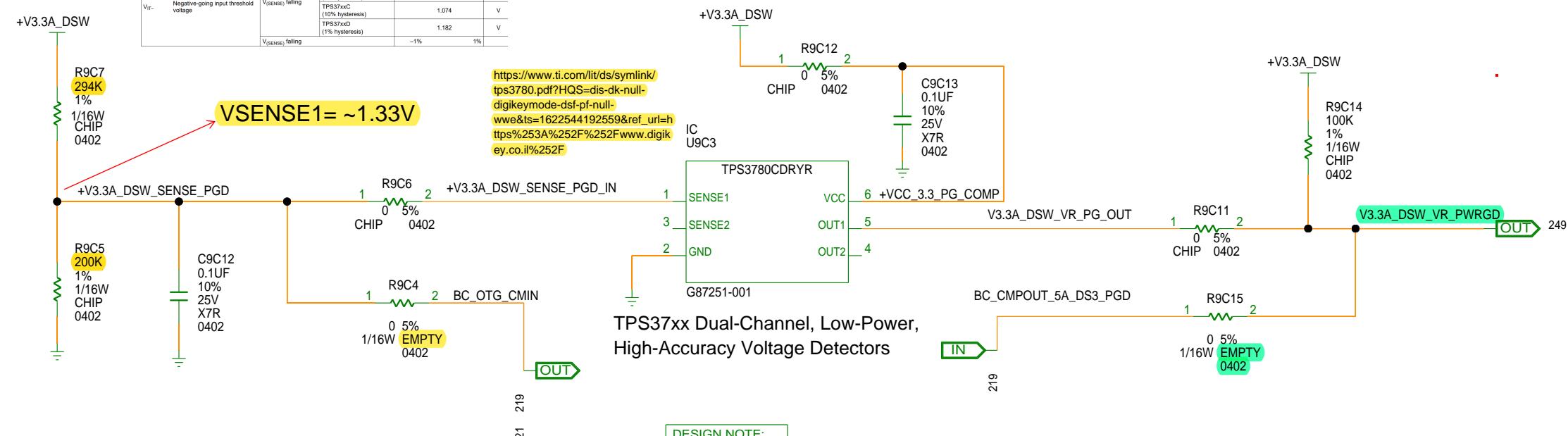
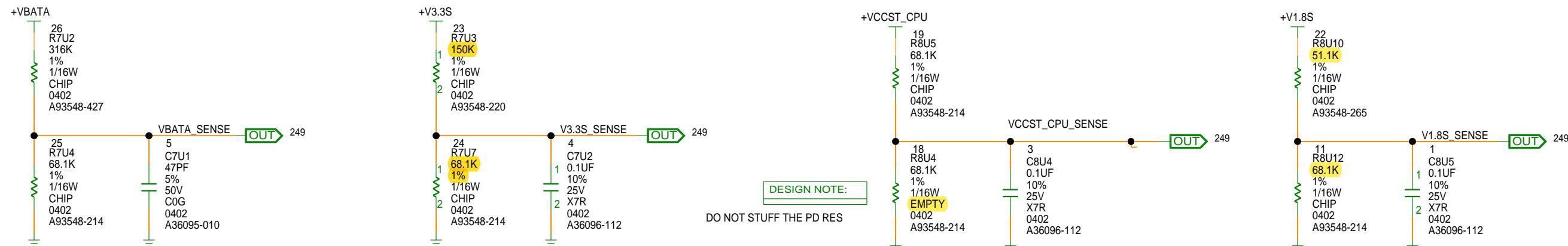






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MODULE REV DETAILS							
MODULE NAME						REV	DATE

POWER SEQUENCING LOGIC - PAGE I

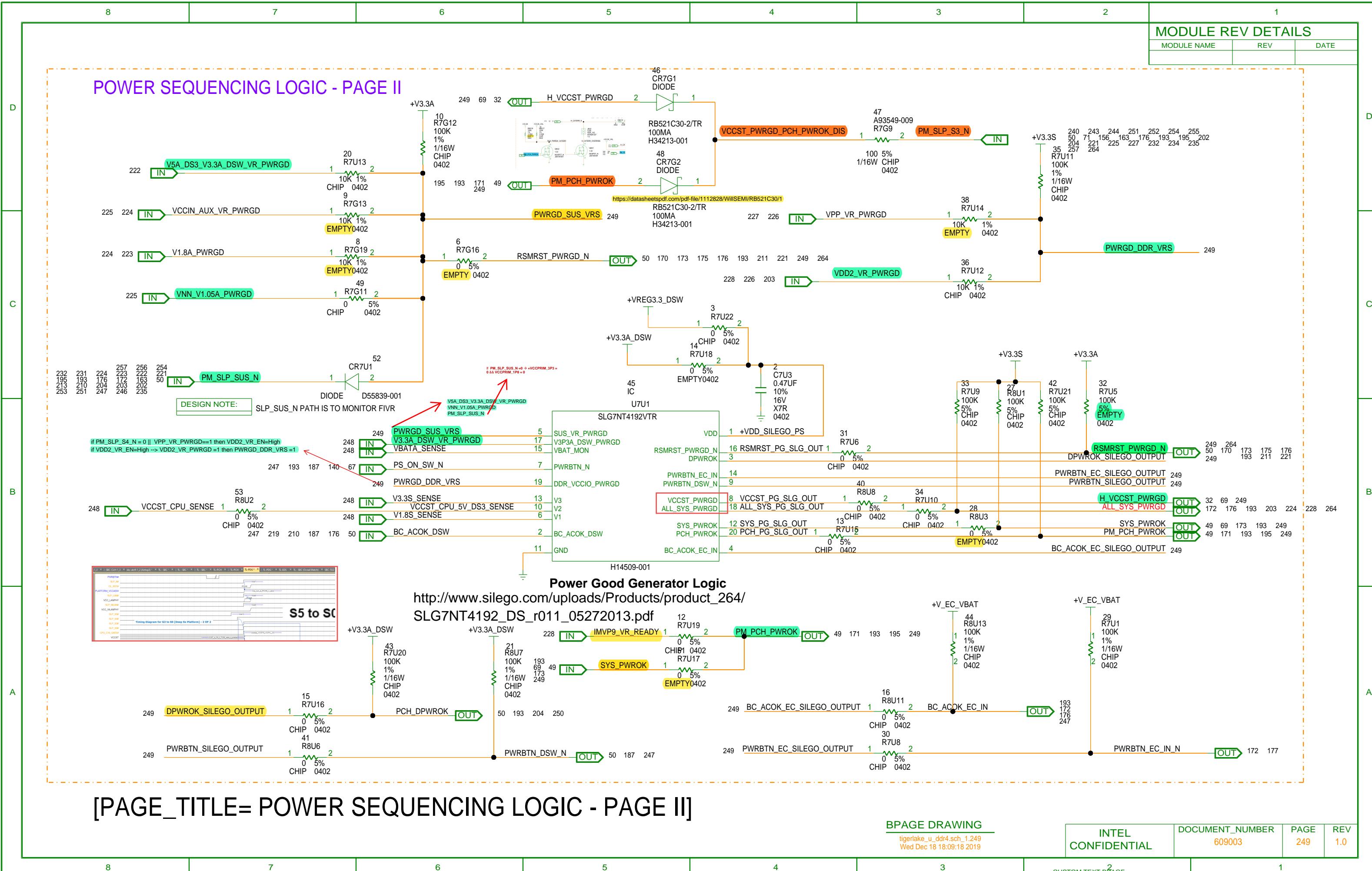


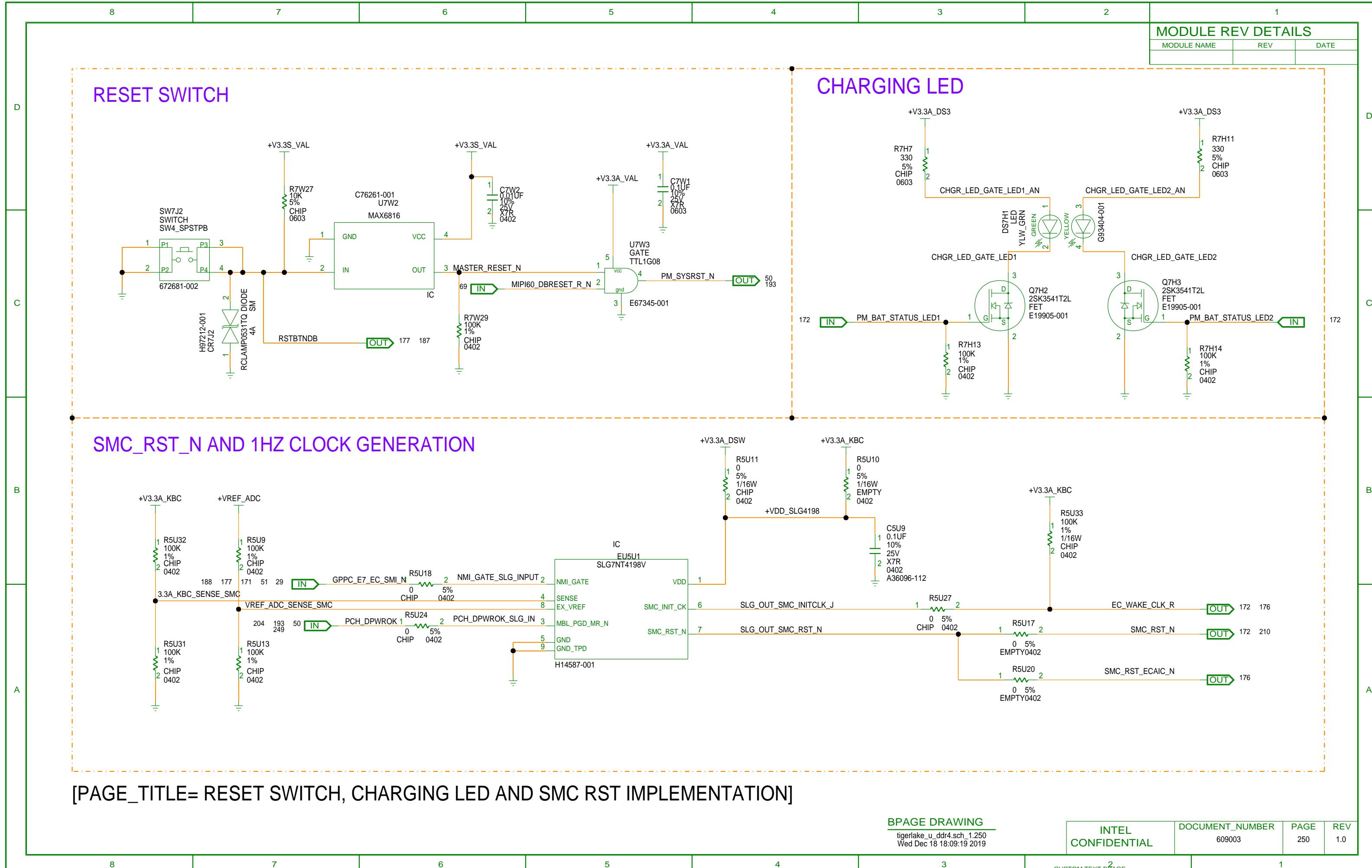
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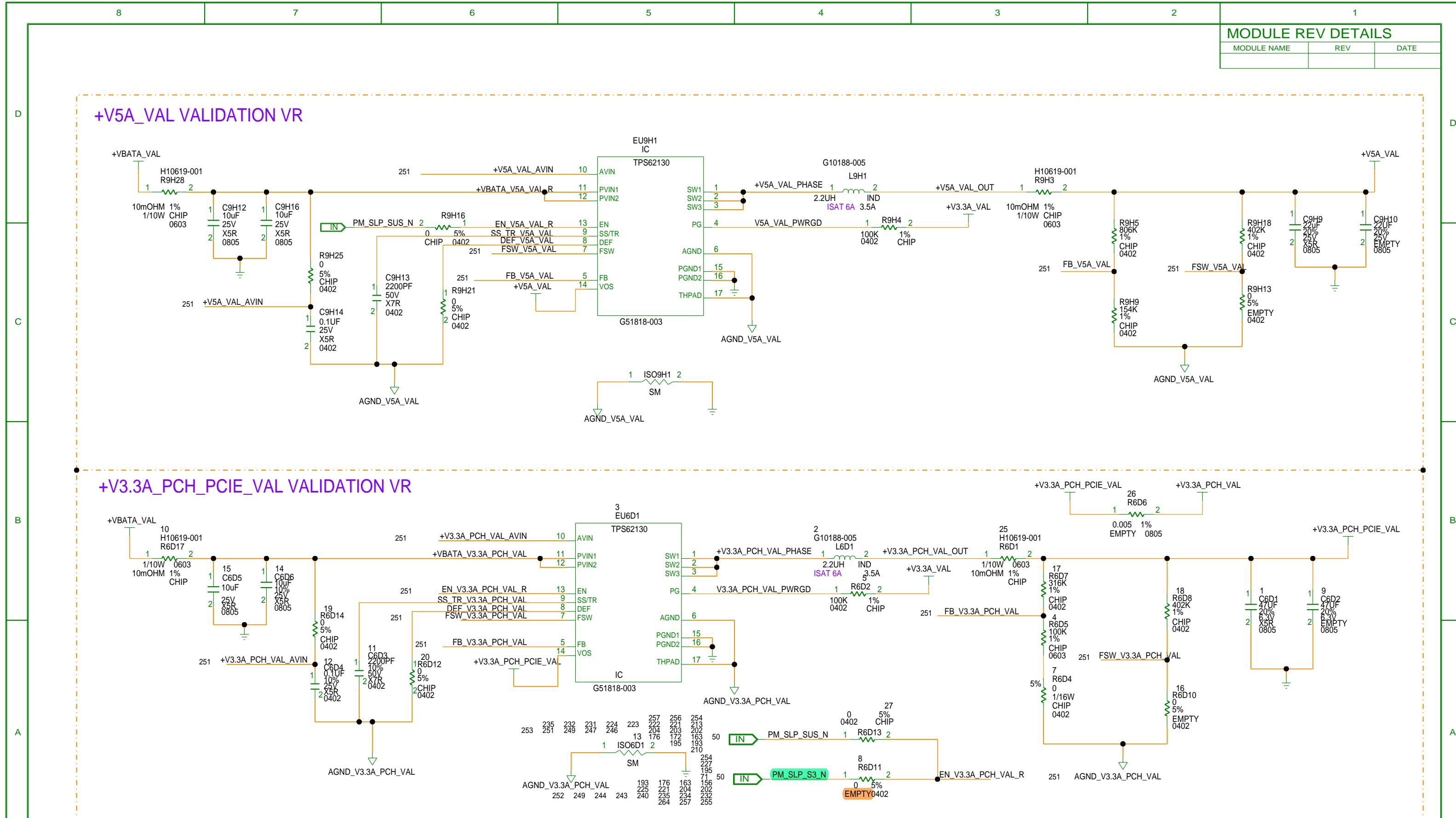
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tigerlake_u_ddr4.sch_1248
Wed Dec 18 18:09:17 2019

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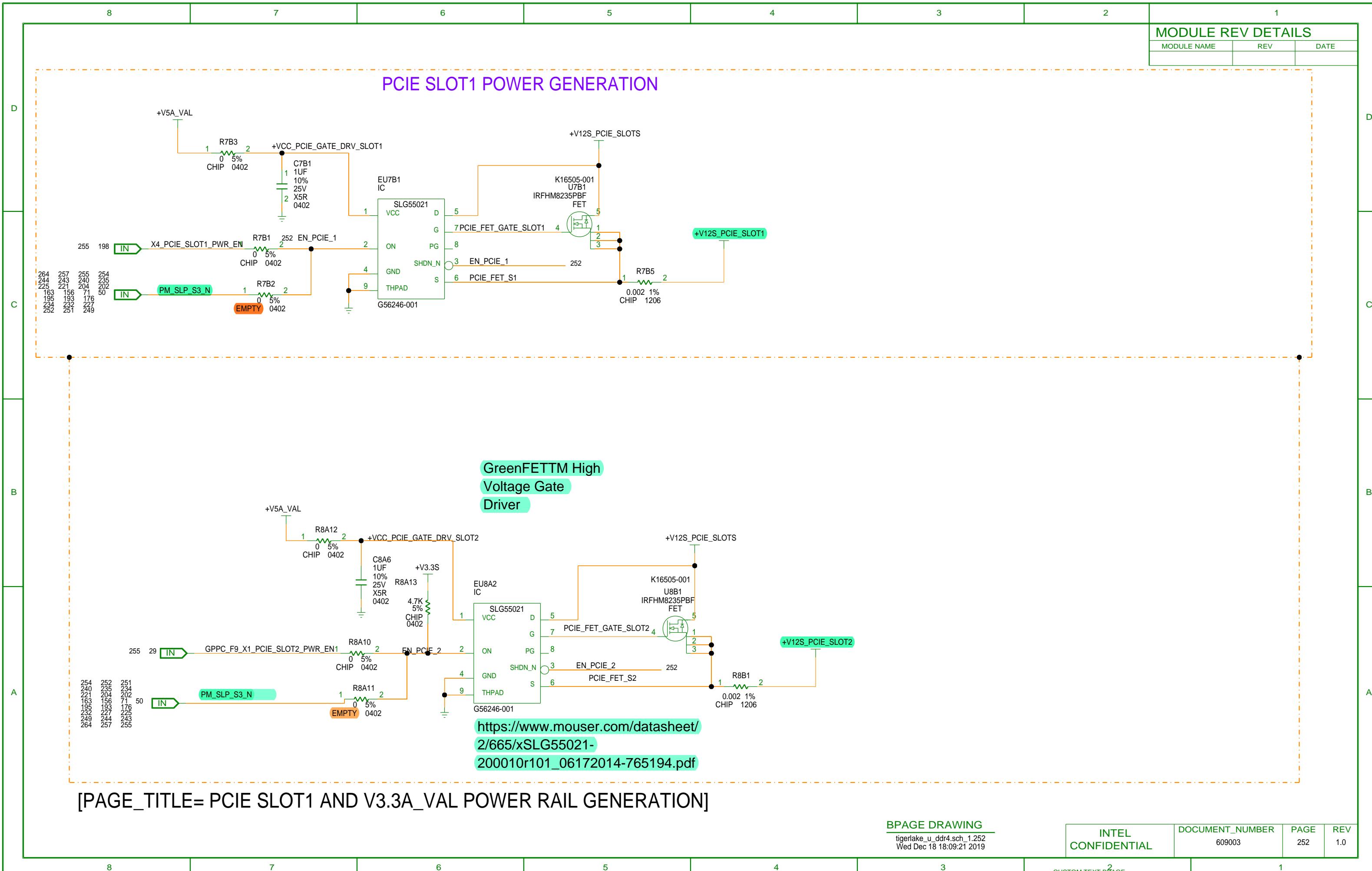


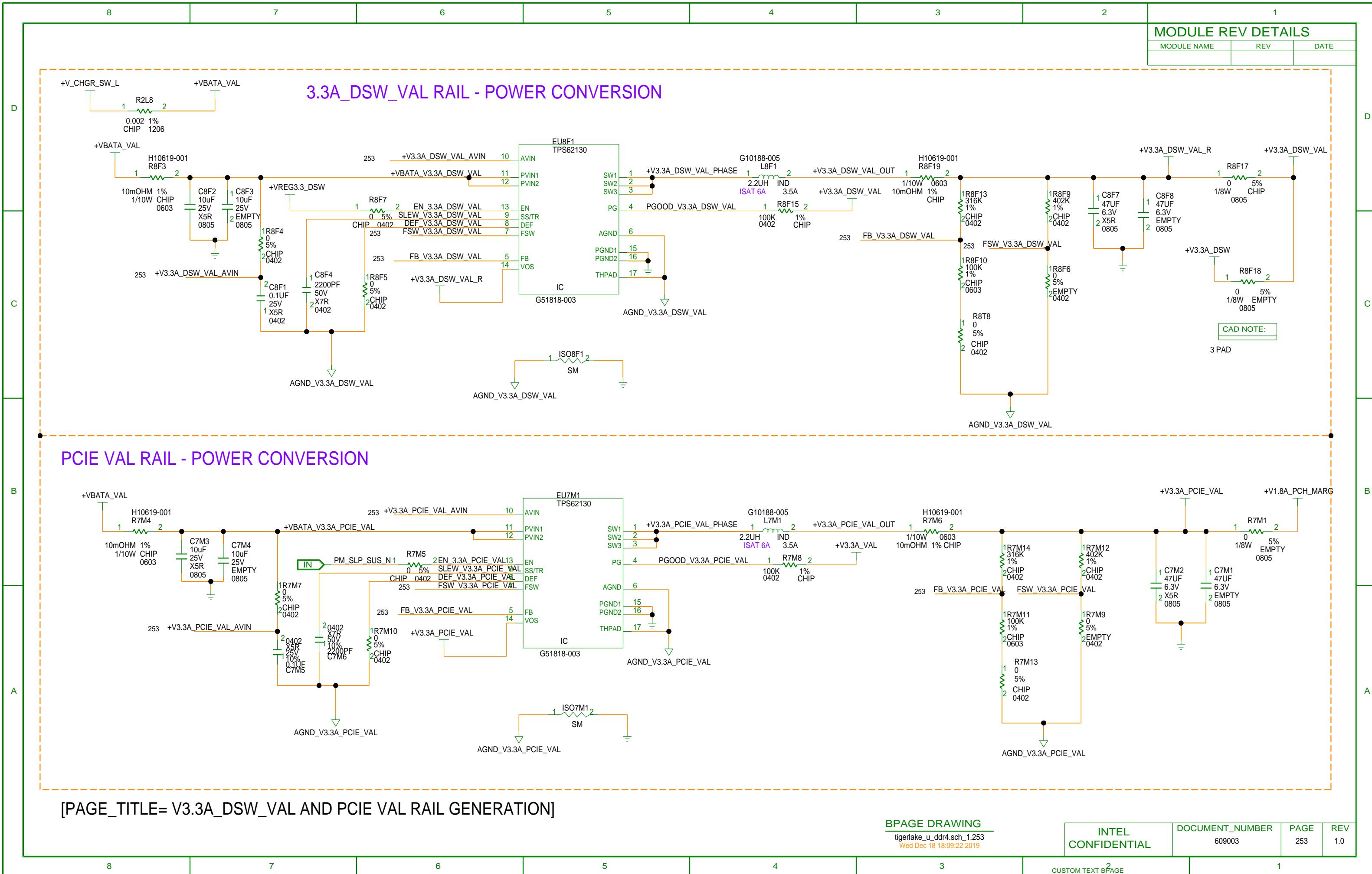
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BPAGE DRAWING

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Wed Dec 18 18:09:20 2019

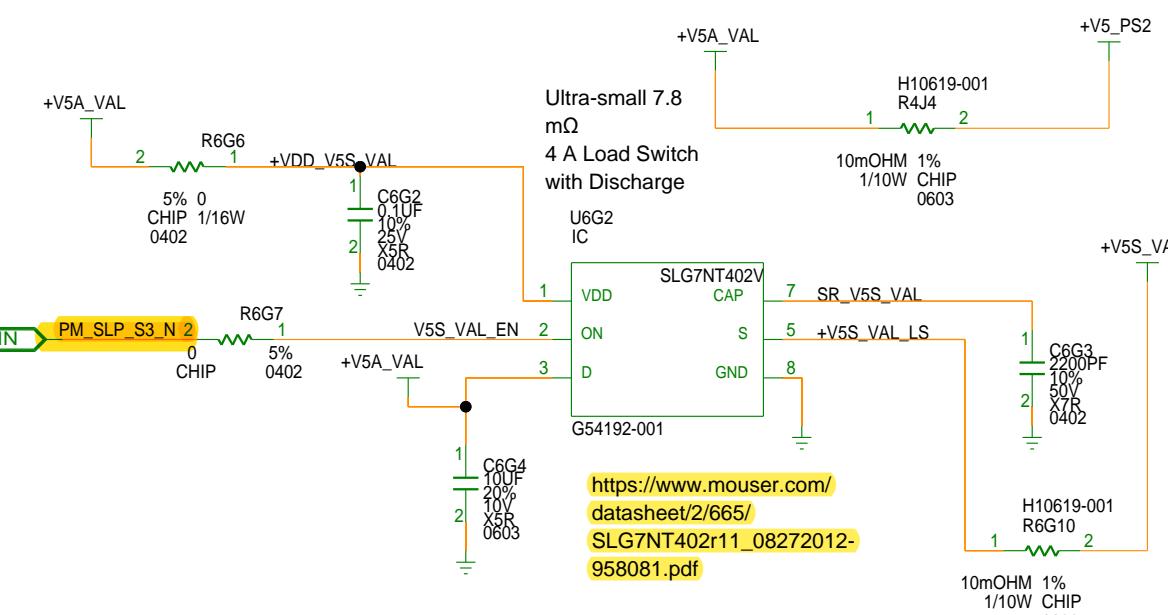
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 251	REV 1.0
CUSTOM TEXT PAGE		1	



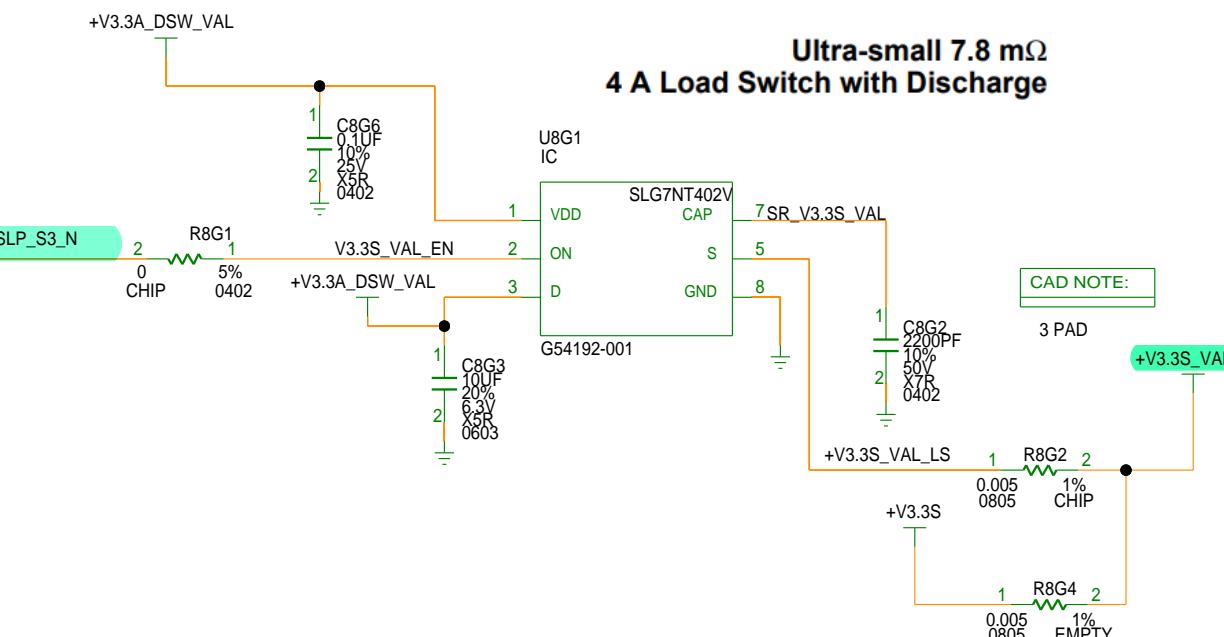


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MODULE REV DETAILS							
MODULE NAME						REV	DATE

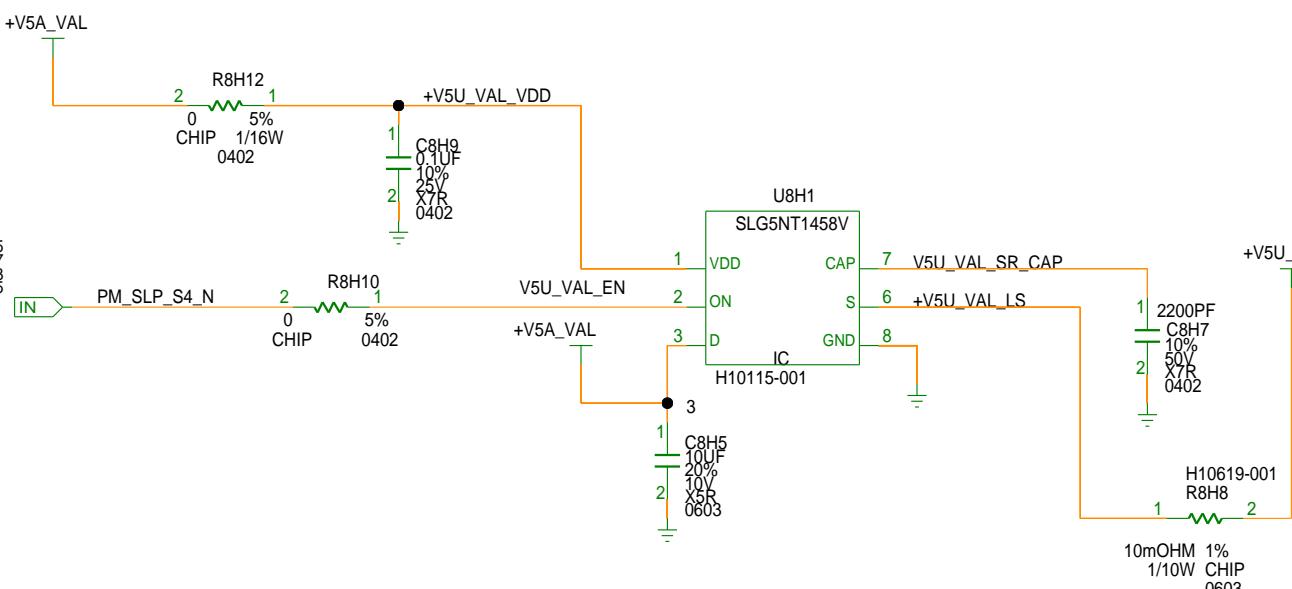
V5S_VAL GENERATION



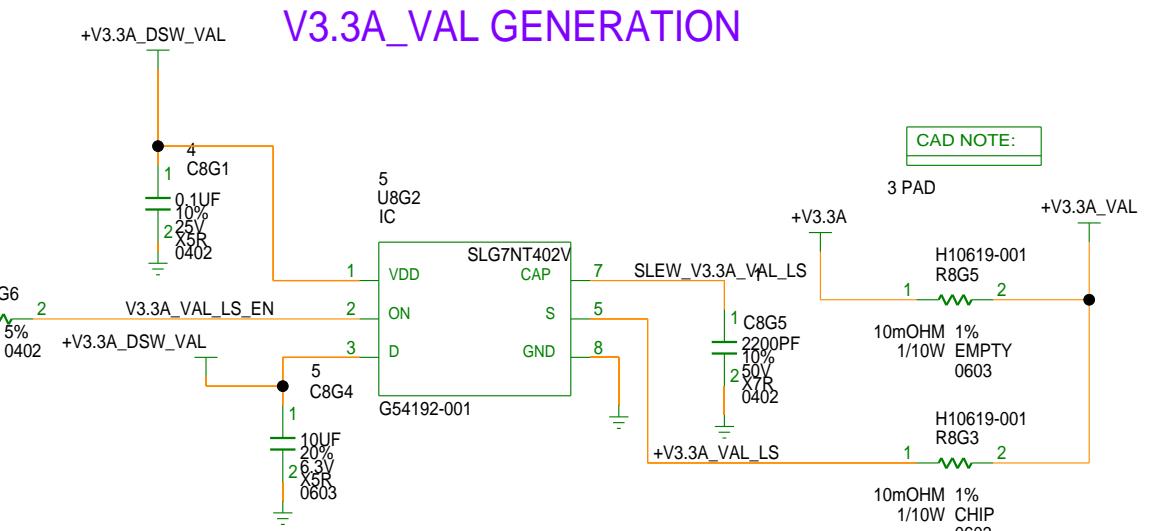
V3.3S_VAL GENERATION



V5U_VAL GENERATION



V3.3A_VAL GENERATION



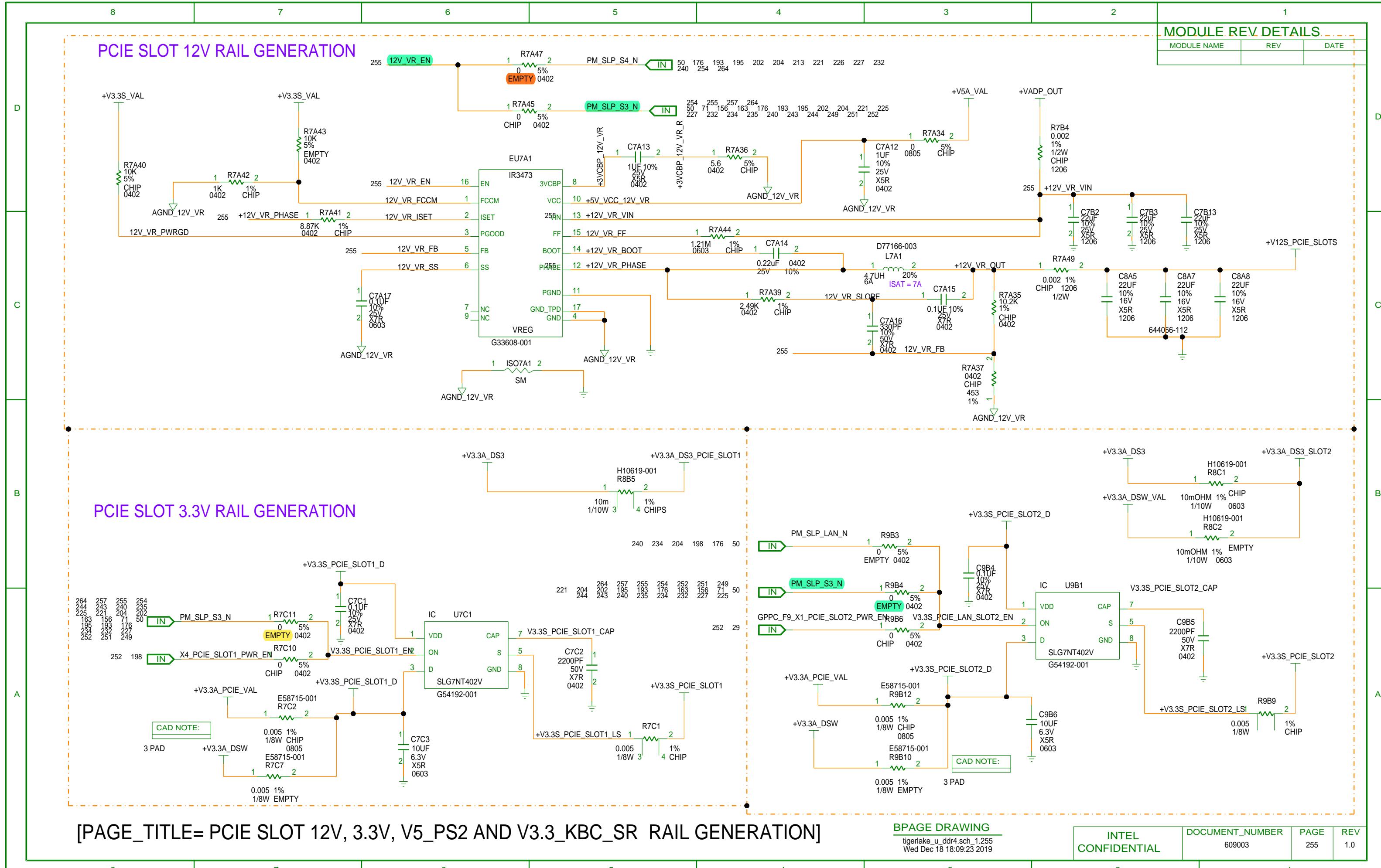
[PAGE_TITLE= U AND S VALIDATION RAILS]

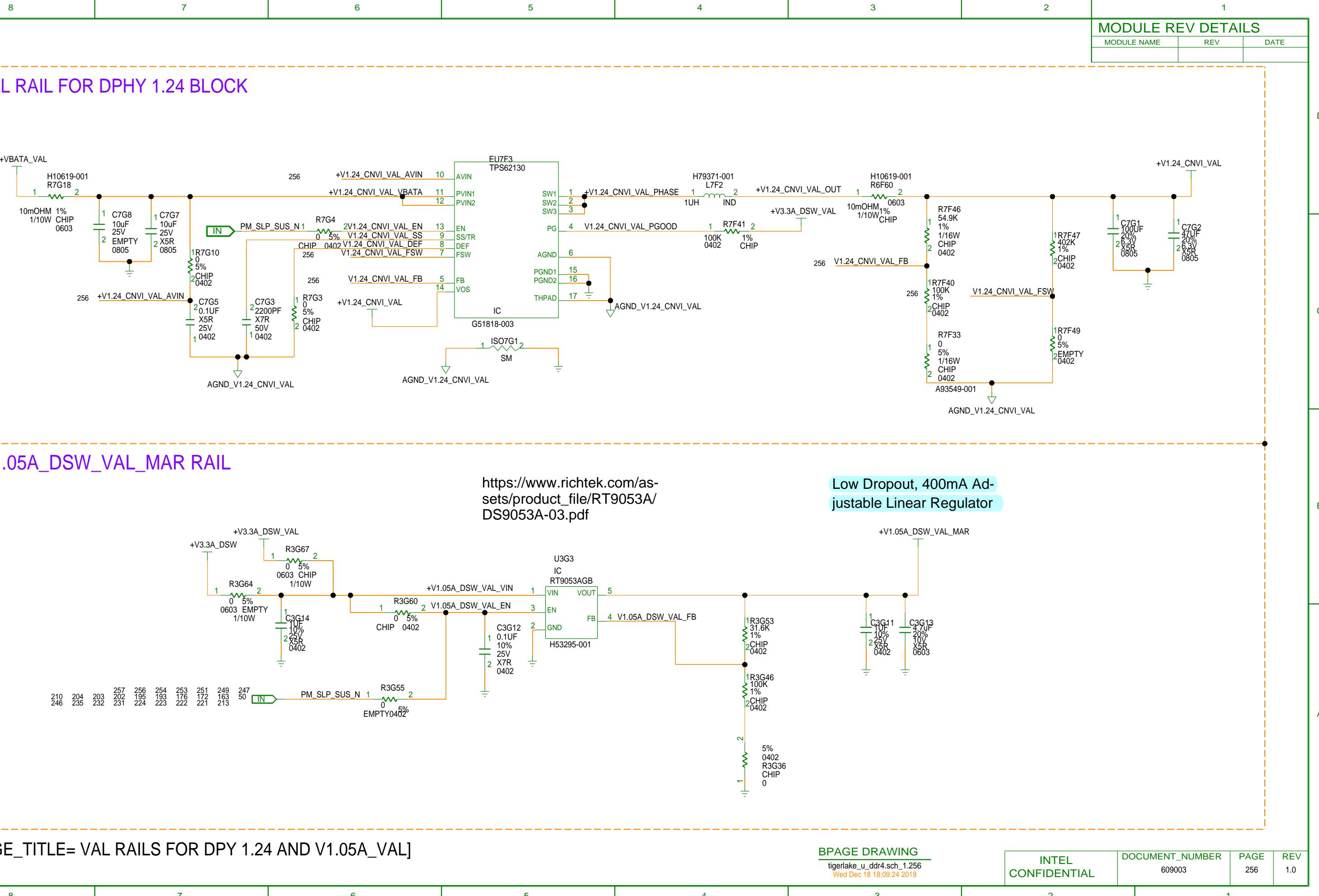
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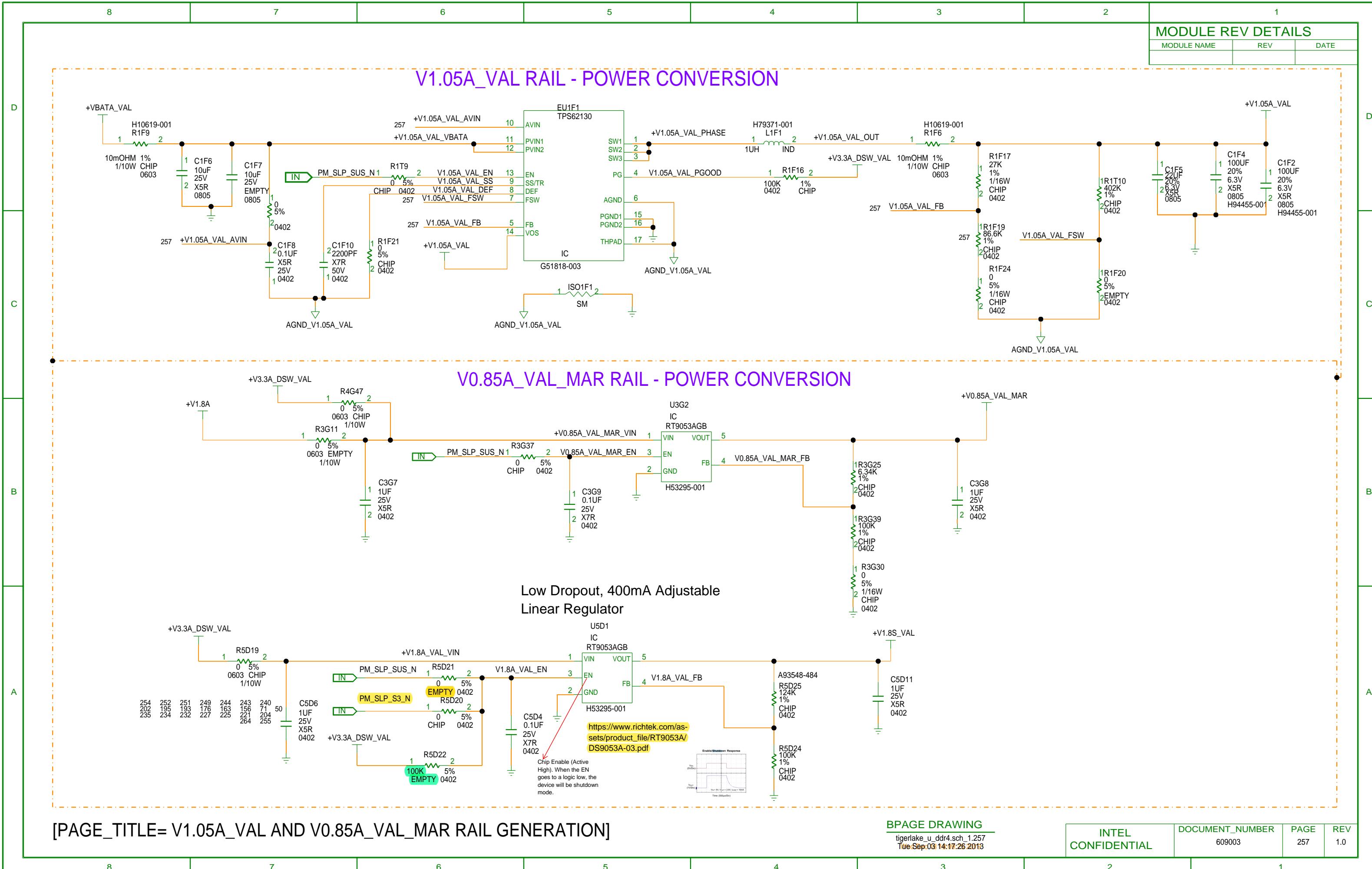
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT 2 PAGE







8	7	6	5	4	3	2	1
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

D

D

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MH6J1
MTG_HOLE
 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
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MH1B1
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GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
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MTG_HOLE
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GND=1,2,3,4,5,6,7,8
G39082-001

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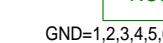
C

C

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G39082-001

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G39082-001

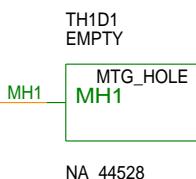
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G39082-001

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MH9J1
MTG_HOLE
 9
GND=1,2,3,4,5,6,7,8
G39082-001

B

B

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MTG_HOLE
 9
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G39082-001



ADDED FOR MEMORY INTERPOSER

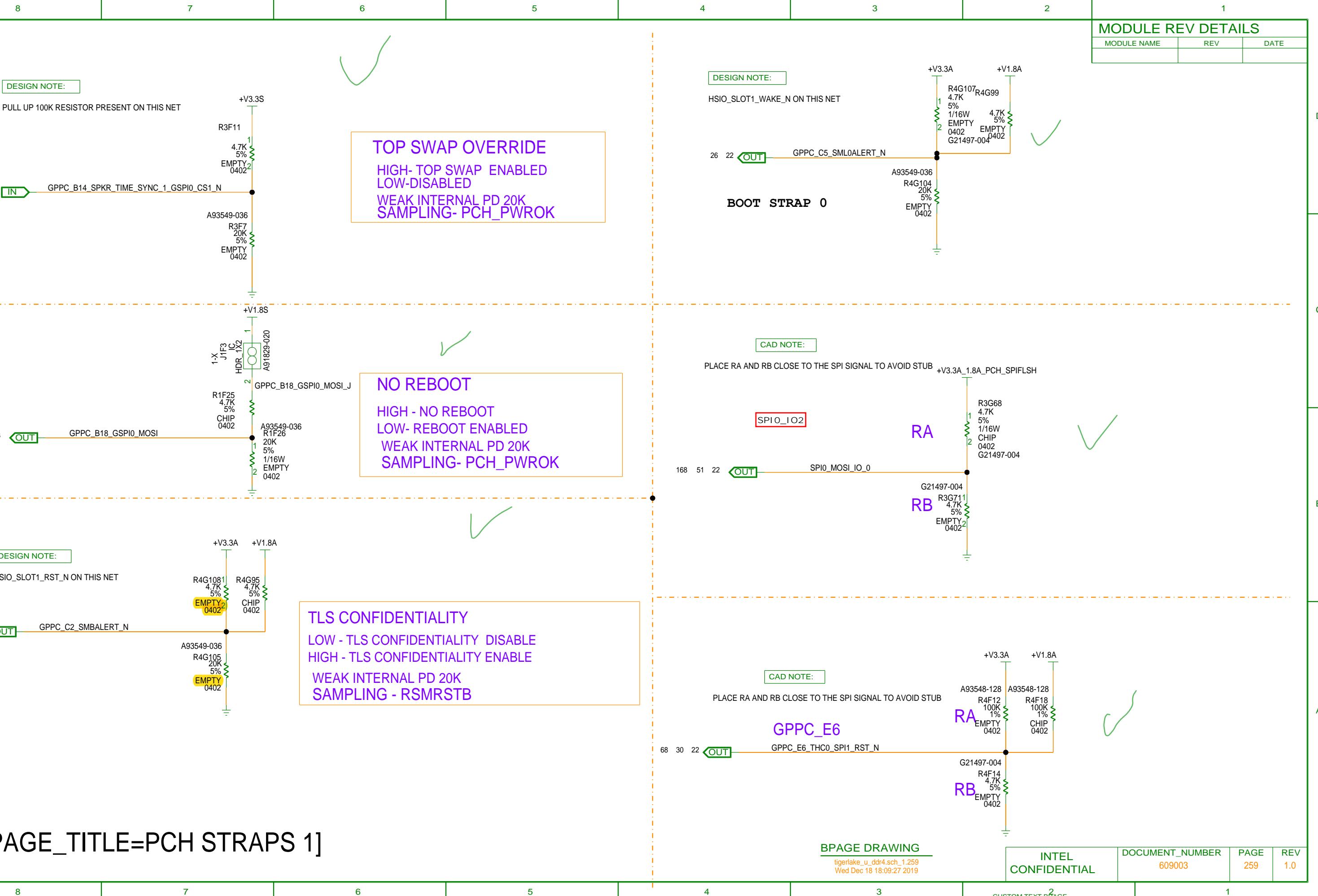
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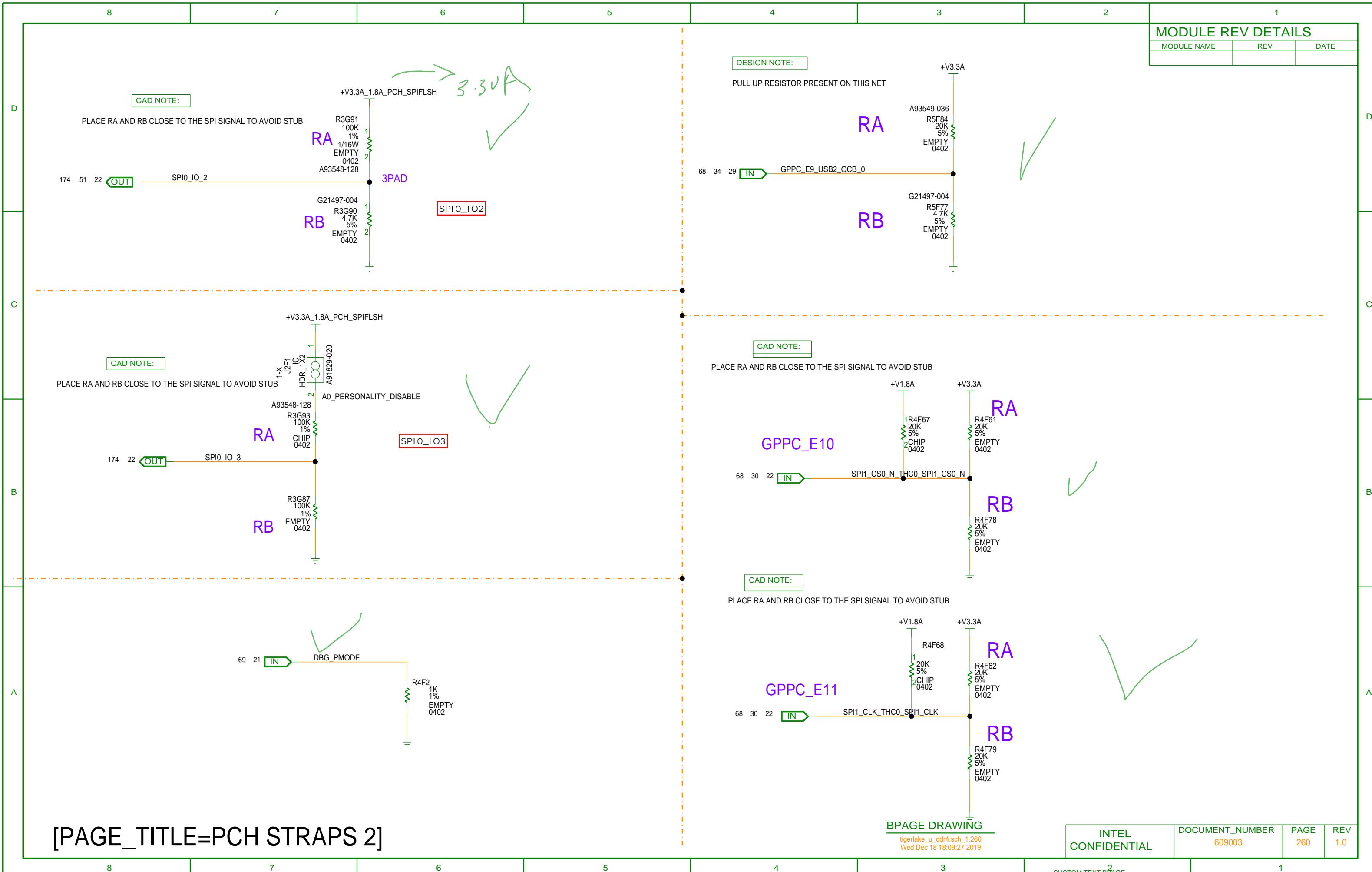
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Wed Dec 18 18:09:26 2019

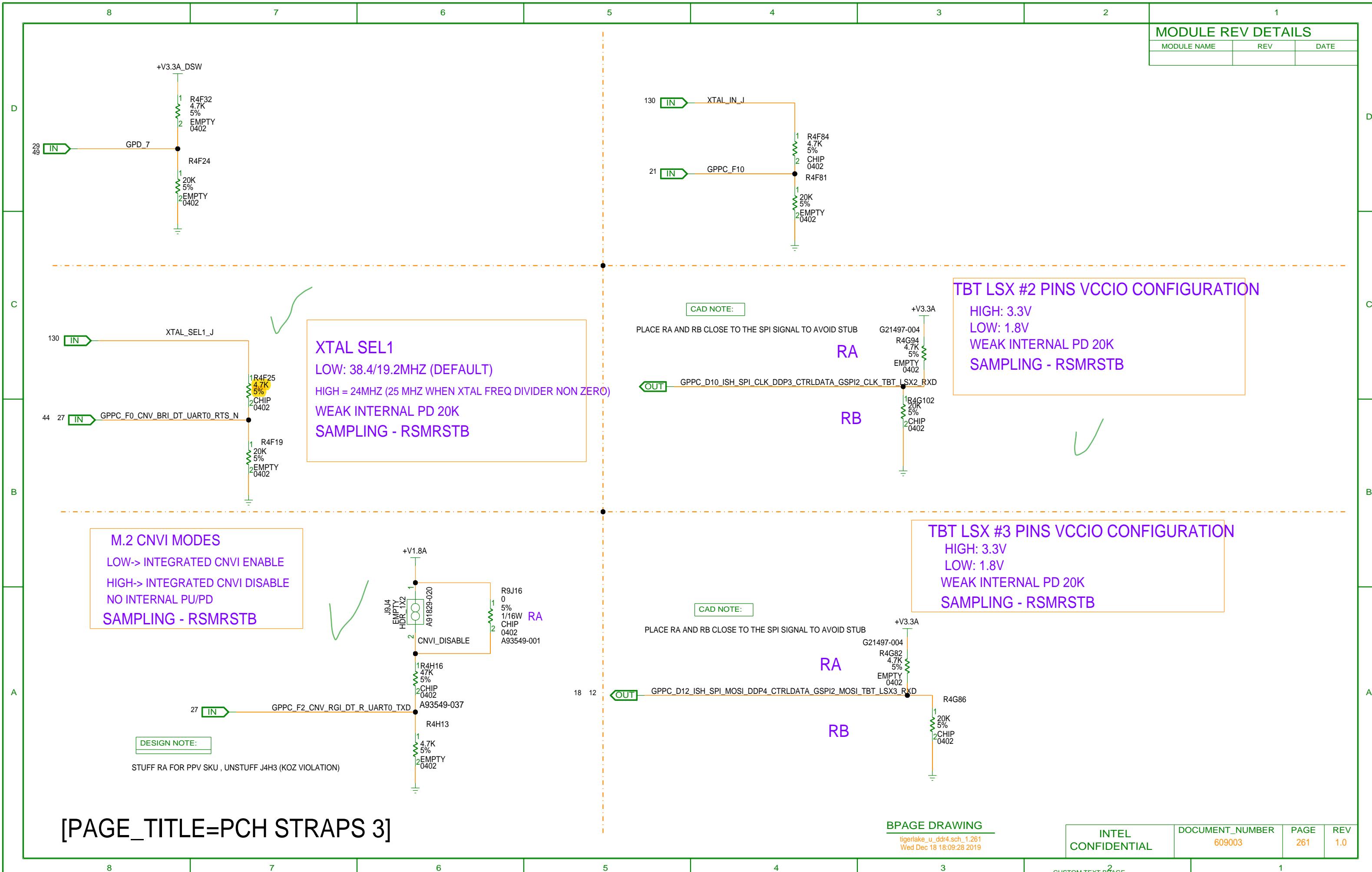
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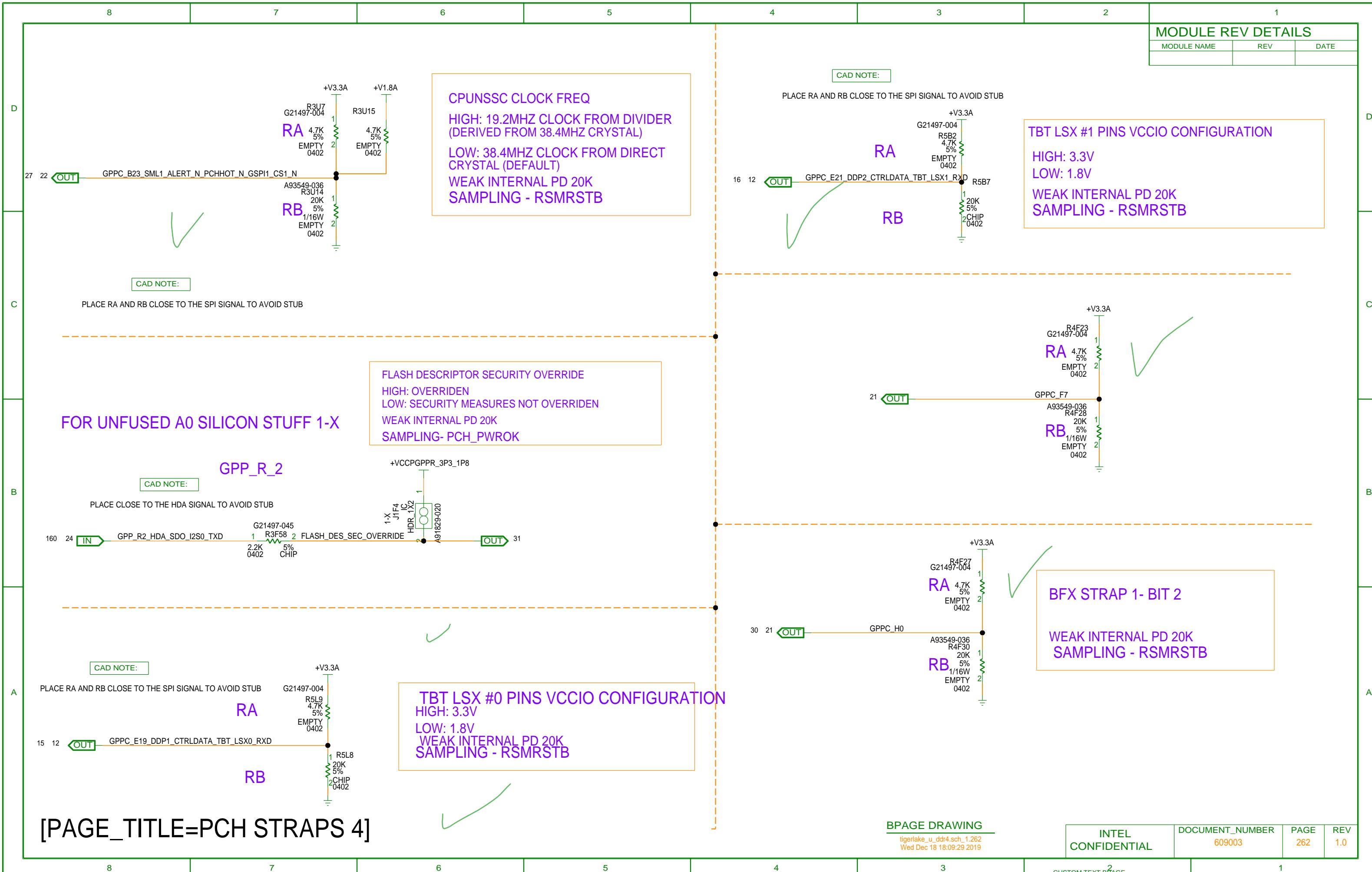
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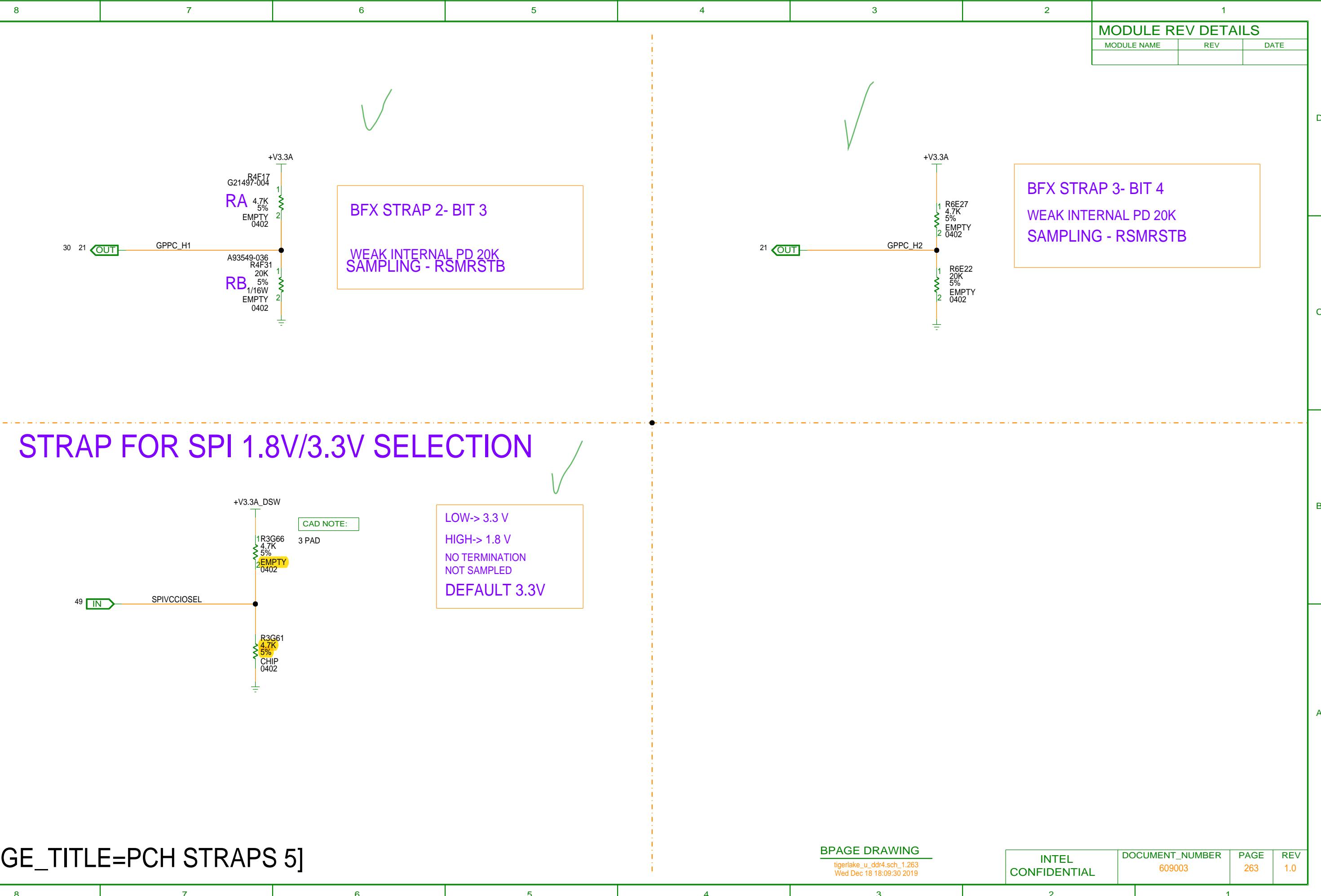
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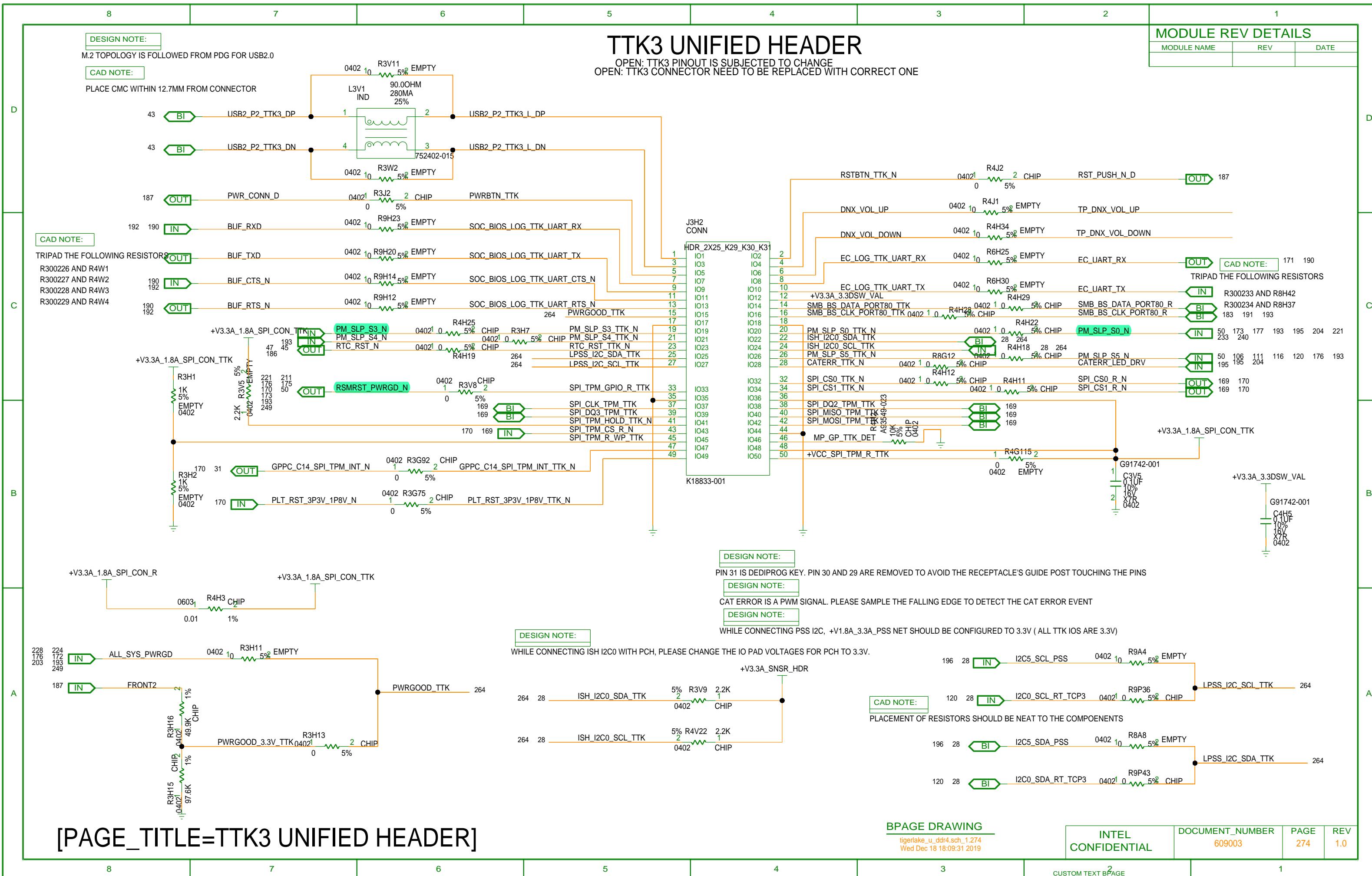


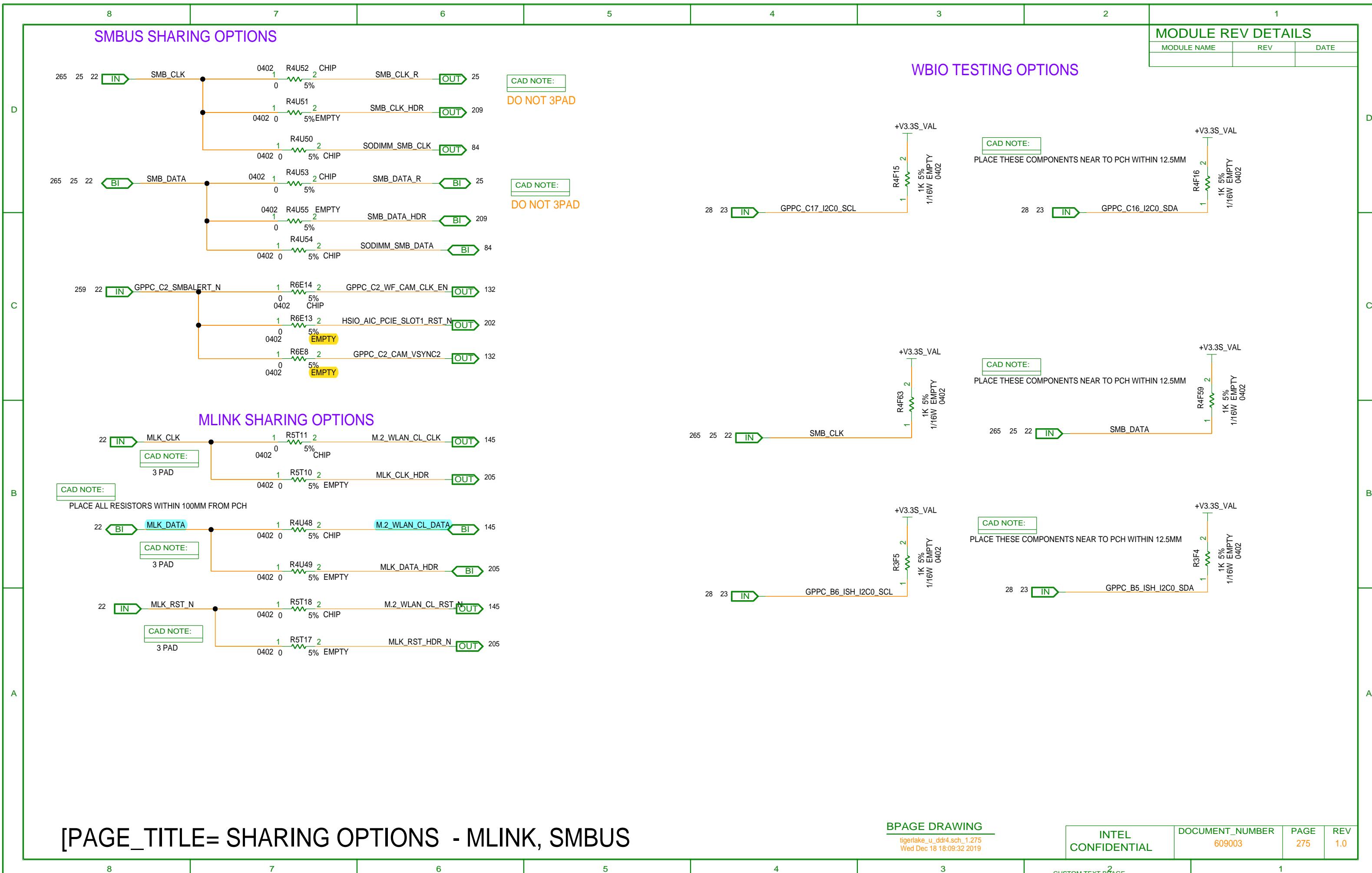


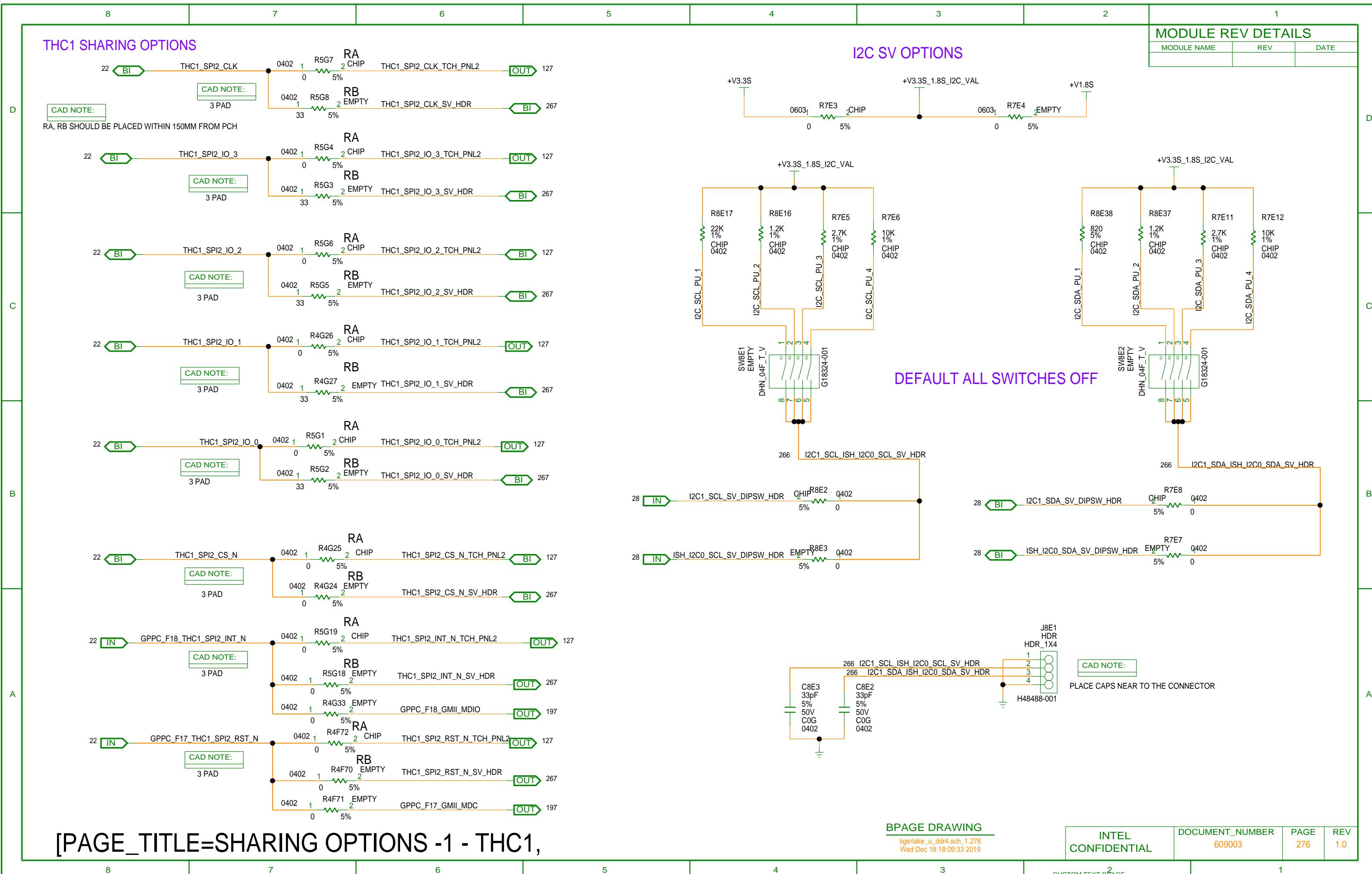












MODULE REV DETAILS		
MODULE NAME	REV	DATE

D

D

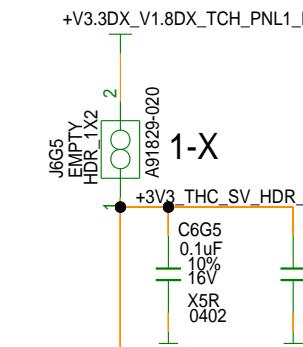
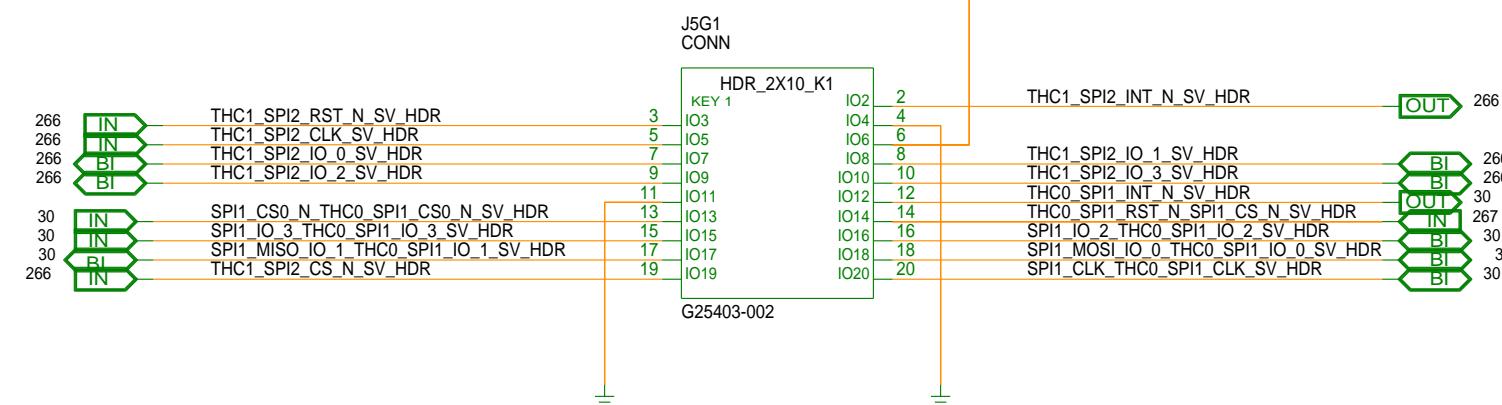
THC0 , THC1 AND SPI1 SV VALIDATION HEADER

DESIGN NOTE:

ONLY SINGLE LOAD IS SUPPORTED. 1.8V IO:RA=33E, 3.3V IO IS NOT POR AND NOT SUPPORTED
MAX CABLE LENGTH SUPPORTED IS 203MM

CAD NOTE:

PLACE RA CLOSE TO CONNECTOR WITHIN 25MM, FOR ALL SIGNALS
PLACE CONNECTOR WITHIN 250MM FROM PCH



DESIGN NOTE:

ON LKF, SPI1 CS1 AND THC0 RESET ARE MULTIPLEXED. HENCE SAME OPTION IS MAINTAINED VIA RESISTOR STUFFING REWORK ON TGL FOR UNIFICATION BETWEEN PLATFORMS

