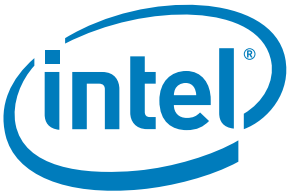


# IMVP9 PWM

## VR Vendor Enabling Specification

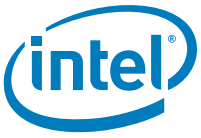
***Revision 1.4***

***July 2017***

**Intel Confidential**

Document Number: 573417

# Contents





## Figures



## Tables

# Revision History

| Document Number | Revision Number | Description | Revision Date |
|---|---|---|---|
| 51061 | 0.5 | • Initial release | November 2015 |
| 51505 | 0.7 | • Changed Slow default to Fast/4<br>• Changed 0Dh PS behavior<br>• Changed Over-Clocking voltage to 3.05V<br>• Changed S-line from fixed voltage to SVID<br>• Added Psys protection and counter features<br>• Added PS4 operation details for S-line support<br>• Vboot values are required, not optional<br>• Changed VID table calculation for clarity (changed the 1 VID subtraction from the VID code to the voltage multiplier) | March 2016 |
| 51594 | 1.0 | • Added clarification to Psys circuitry and registers<br>• Added schedule in Appendix<br>• Clarified T_Alert timing | April 2016 |
| 52117 | 1.1 | • Removed the IMVP8 VccSA rail register reference - refer to the IMVP8 spec if implementing VccSA | November 2016 |
| 52279 | 1.2 | • Updated Section 6.9.2 | January 2017 |
| 573417 | 1.3 | • Updated Table 6-6 section 4D and 4E<br>• Convert document confidentiality from IRS to IC | June 2017 |
| 573417 | 1.4 | • Changed T_ALERT from 1us to 3us<br>• Max time for critical PSYS CRIT to assertion of VR_HOT# is ≤ 2us max | July 2017 |

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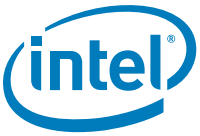


# 1 Introduction

This document defines the PWM control chip features for the IMVP9 DC-DC regulators used in Intel platforms. IMVP9 includes a Serial VID (SVID) interface. Future platform power delivery design guidelines will contain the actual platform DC-DC regulator implementations for mobile and desktop market segments and takes precedence over the targets shown in this document.

## 1.1 Terminology

**Table 1-1. Feature Support Terminology**

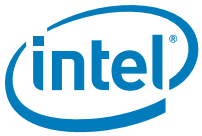
| Categories | Description |
|---|---|
| REQUIRED | An essential feature of the design that must be supported to ensure correct processor and voltage regulator (VR) functionality. Required functions are critical to CPU functions. |
| EXPECTED | A feature to ensure correct VR and processor functionality that can be supported using an alternate solution. The feature is necessary for consistency among system and power designs and is traditionally modified only for custom configurations. The feature may be modified or expanded by system OEMs if the intended functionality is fully supported. |
| PROPOSED | A feature that adds optional functionality to the VR and, therefore, is included as a design target. May be specified or expanded by system OEMs. |
| OPTIONAL | A feature that is not required for processor operation; however, specific platforms or OEMs may request this feature or function. |

**Table 1-2. Glossary (Sheet 1 of 3)**

| Term | Description |
|---|---|
| # | This symbol after a signal name means an active low signal (logic low = asserted) |
| Active high | Signal is asserted when logic is high or a “1” |
| Active low | Signal is asserted when logic is low or zero volts |
| Alert# | SVID Alert line or interrupt line |
| AVP | Adaptive voltage positioning or Load Line (LL) |
| BJT | Bi-Polar Junction Transistor |
| CFM | Cubic feet per minute (airflow). |
| CMRR | Common-mode rejection ratio. |
| CPU | Central Processing Unit, microprocessor |
| CRC-8 | 8-bit Cyclic Redundancy Check |
| DAC | Digital to Analog Converter. |
| DCR | Direct Current Resistance. |
| D-VID | Dynamic Voltage ID. A mode of operation where the output voltage is dynamically changed by changing the VID bits |
| D-VID code | Dynamic Voltage Identification code |
| EMI | Electro-Magnetic Interference |
| EMTS | Electrical, Mechanical, and Thermal Specification |
| ESD | Electrostatic Discharge |

## Table 1-2. Glossary (Sheet 2 of 3)

| | |
|---|---|
| ESL | Equivalent series inductance |
| ESR | Equivalent series resistance |
| FET | Field Effect Transistor |
| FMB | Flexible Motherboard |
| FR4 | A type of printed circuit board (PCB) material |
| GND | Ground (return) |
| HFM | High Frequency Mode |
| HS | Heat Sink |
| HVM | High volume manufacturing |
| $I_{cc}$ | Load current |
| Itt | Bus current associated with the Vtt supply |
| IMON | Analog output (0-900mV) proportional to average output current |
| $I_{OUT}$ | Digitized version of $I_{OUT}$ signal; available over SVID bus |
| LFM | Depending on context: Linear feet per minute (airflow) or Low Frequency Mode |
| Load Line | A mathematical model that describes voltage current relationship given the system impedance ($R_{LL}$). The nominal load-line equation is $V_{cc}$ = VID – I*$R_{LL}$. |
| LV | Low Voltage |
| MLCC | Multi-layer ceramic capacitor |
| Monotonically | A waveform changes from one level to another in a steady fashion, without intermediate retracement or oscillation. |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor. |
| MTBF | Mean Time Between Failures |
| OCP | Over current protection. |
| OTP | Over-Temperature Protection |
| OVP | Over Voltage Protection |
| PEC | Packet Error Correction |
| Processor Datasheet | A document that defines the processor's electrical, mechanical, and thermal specifications |
| PROCHOT# | Under thermal monitoring, the VRD asserts this processor input to indicate an over-temperature condition has occurred. Assertion of this signal places the processor in a low power state, thereby cooling the voltage regulator. |
| PWM | Pulse width modulation. |
| $P_{sys}$ | Input System Power |
| RDSon | MOSFET's Drain Source resistance |
| Ripple & Noise | The periodic or random signals on a voltage rail measured over frequency band of 0 Hz to 20 MHz |
| Rise Time | Rise time is defined as the time it takes any output voltage to rise from 10% to 90% of its nominal voltage |
| $R_{LL}$ | Load line impedance. Defined as the ratio: Voltage droop/current. This is the load-line slope. |
| ROP | Rest of Platform |
| RMS | Root Mean Square |
| RSS | Root Sum Square. A method of adding statistical variables. |
| SerialVID or SVID | Serial Voltage Identification code |



## Table 1-2. Glossary (Sheet 3 of 3)

| | |
|---|---|
| SFF | Small Form Factor |
| Slope | Load line resistance. Refer $R_{LL}$. |
| TDC | Thermal Design Current (continuous current while CPU is drawing thermal design power) |
| TDE | Thermal Design Envelope |
| TDP | Thermal Design Power |
| Thermal Monitor | A feature of the voltage regulator that places the processor in a low power state when critical VRD temperatures are reached, thereby reducing power and VRD temperature |
| Tolerance budget (TOB) | Defines the voltage regulator's 3-σ voltage variation across temperature, manufacturing variation, and age factors. Must be ensured by design through component selection |
| Transient Load Line or AC LL | Equal to dV/di or Vdroop/Istep and is controlled by switching frequency, decoupling capacitor selection, and motherboard layout parasitics |
| ULV | Ultra Low Voltage |
| UVLO | Under-voltage lock-out |
| Vcc | Processor core voltage defined in the processor datasheet. |
| VccP | IO termination voltage |
| VCLK | SVID clock |
| VDIO | SVID Data I/O |
| VID | Voltage Identification: A code supplied by the processor that determines the reference output voltage to be delivered to the processor Vcc lands. At zero amperes and the tolerance band at + 3-σ, VID is the voltage at the processor. |
| VR | Voltage Regulator |
| VRD | Voltage regulator down. A VR circuit resident on the motherboard. |
| VRM | Voltage regulator module that is socketed to a motherboard |
| Vtt | IO termination voltage |
| VR_HOT# | Active low output indicating the VR is over temperature and will be connected on the platform to force thermal throttle to reduce VR load |

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# 2 Required Features

The IMVP9 will cover multiple market segments for Ultrabooks™, Tablets, Notebooks, and Desktop platforms. PWM control ICs for all market segments will implement a common Serial VID interface and command protocol; basic feature sets (VID table, fault response, power states, etc.).

## 2.1 Market Segments

The U/Y-line and H/S-line Platform Power Architecture Guide, and their respective EDS will document required currents, power levels, tolerance band, ripple and loadline information for each platform.

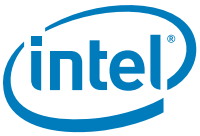
## 2.2 Addressing - Required All Segments

The data packet will contain a 4 bit addressing code for future platform flexibility. 13 address ranges are used for up to 12 distinct voltage rails and 1 Power Domain. The final two addresses, 0Eh, 0Fh are used for all-call instructions. Controllers must respond to the all call 0Fh or 0Eh address commands. The VR vendor is responsible for determining the physical address assignment on their chip. Examples include: single pin with resistor divider to program the unique addresses, binary encoded 3 address pins, OTP programming etc.

**Table 2-1. Address Definitions by Processor Type**

| IMVP9 Domain Address HEX | Y, U and H-line | S-line CPU (Desktop) |
|---|---|---|
| 00h | VccIn | |
| 01h | Reserved | |
| 02h | Reserved | |
| 03h-04h | Available for use | |
| 06h-0Ch | Reserved | |
| 0Dh | Input Power sensor | |
| 0Eh | All Call | |
| 0Fh | All Call | |

***Note:***
1. The VR All-call command functions on either address 0Eh or 0Fh



## 2.3 Required Features and Registers

Table 2-2 lists the required features and registers the IMVP9 controller solution must support.

For a multi-output PWM, the required features are:

- Independent feedback for each rail
- Dual differential remote sense pairs for each rail
- Independent LL or AVP functions for each rail, including setting to zero
- Independent loop compensation for each rail
- Independent, $V_{BOOT}$ levels on each rail
- Independent OVP, OCP functions on each rail
- Independent Icc_MAX settings for each rail
- Independent $I_{OUT}$ reporting for each rail
- Single VR_Hot# output, any rail's thermal sensor can trip VR_Hot#
- Single Temp_Max programming level
- If a rail is disabled or not populated on a multi-output PWM, that SVID address should be disabled and the PWM should reject commands to the disabled rail address.

**Table 2-2. Summary of Required Features (data or X=required, O=optional, NA=Not Applicable) (Sheet 1 of 2)**

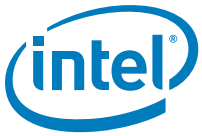
| Feature | Domain Address 00h VccIn | Input Power Domain Address 0Dh | Notes |
|---|---|---|---|
| VID Range | 0-2.74V<br>(3.05V for OC) | NA | |
| SetVID Fast | 48 mV/µs - Min required in Y, U and H-lines.<br>Optional in S-line. | NA | 90mV/us MAX slew rate between any two points during the VID transition |
| | 10 mV/us - Minimum for S-line | | |
| SetVID Slow | Default is 1/4 Fast slew rate<br>Minimum and Target slew rate. Slew rate register must reflect actual slew rate. Slow Slew Rate register 2Ah selects the slew rate. Refer to the SVID protocol for additional slew rate settings. | | |
| SetVID Decay | X | NA | |
| SetPS0 | X | X<br>ACK and do nothing<br>(Follow 1st domain out of PS4) | |
| SetPS1 | X | X<br>ACK and do nothing | |
| SetPS2 | X | X<br>ACK and do nothing | |
| SetPS3 | X | X<br>ACK and do nothing | |
| SetPS4 | X | X<br>ACK and do nothing<br>(Follow last domain into PS4) | |

## Table 2-2. Summary of Required Features (data or X=required, O=optional, NA=Not Applicable) (Sheet 2 of 2)

| Feature | Domain Address 00h VccIn | Input Power Domain Address 0Dh | Notes |
|---|---|---|---|
| SetRegADR | X | | |
| SetRegDAT | X | | |
| GetReg | X | | |
| SetWP (1-4) | O | NA | |
| Temp sensor input | X | NA | Rails that support turbo must have independent Temp sensor inputs (common Temp max, & VR_Hot# output) |
| VR_Hot# | One Active Low Thermal Monitor output, utilizing the temperature sensor input (hottest rail will activate) | NA | |
| Enable | One enable for all rails on multi-output PWM | NA | |
| VR_Ready | One VR_Ready per physical SVID device. | NA | |
| $V_{BOOT}$ | X<br>0V and 1.8V | NA | |

## Summary of Required Registers (data or X=required, O=optional, NA=Not Applicable) (Sheet 1 of 3)

| Register | Domain Address 00h | Input Power Domain Address 0Dh | Notes |
|---|---|---|---|
| 00h-02h (Product info) | X | X | Required in each device of a multi-device configuration |
| 03h-04h | O | O | |
| 05h<br>(Protocol ID) | IMVP9=08h | IMVP9=08h | Required in each device of a multi-device configuration |
| 06h<br>(Capability) | 81h - Default<br>01h - for $J_{OUT}$ in 15h | NA | Support of Joules out is optional. |
| 07h-0Fh | O | O | |
| 10h-11h<br>(Status) | X<br>Includes bit 3, VID DAC High. Refer SVID Protocol Spec for details. | O<br>Not needed. Only optional to prevent conflict with IMVP8 | |
| 12h<br>(Temp zone) | Optional, but thermal Alert & VR_Hot functions must be supported. | NA | |
| 13h<br>(Global Status) | NA | | |
| 14h | NA | | |
| 15h<br>($I_{OUT}$ / $J_{OUT}$) | X | NA | $I_{OUT}$ is Required. $J_{OUT}$ is optional. Refer Section 2.3.1 |
| 16h -1Ah | O | NA | |
| 1Bh<br>(Input Power) | O | X | |



## Summary of Required Registers (data or X=required, O=optional, NA=Not Applicable) (Sheet 2 of 3)

| Register | Domain Address 00h | Input Power Domain Address 0Dh | Notes |
|---|---|---|---|
| 1Ch (Status2_lastread) | X | NA | |
| 21h (Icc_Max) | Must be programmed by platform designer to reflect capability of the relevant voltage output. Default 00h indicates this value it's not programmed and platform won't boot. | NA | |
| 22h (Temp_Max) | O | NA | |
| 23h | O | NA | |
| 24h (Fast slew rate) | X | NA | |
| 25h (Slow slew rate) | X | NA | |
| 26h -29h | O | NA | |
| 2Ah (Slow Slew Rate Setting) | X | NA | |
| 2Bh (PS4 exit latency) | X | NA | |
| 2Ch (PS3 exit latency) | X | NA | |
| 2Dh (Enable to SVID ready) | X | NA | |
| 2Eh (Pin_Max) | O | O | |
| 2Fh | NA | | |
| 30h (Vout Max) | X | NA | |
| 31h (VID setting) | X | NA | |
| 32h (Power state) | X | NA | |
| 33h (Voltage Offset) | X | NA | |
| 34h (Multi VR config) | X Default = 01h | NA | Must also support 00h setting |
| 35h | O | NA | |
| 36h (CPU Status) | NA | | |
| 37h-39h | NA | | |

**Summary of Required Registers (data or X=required, O=optional, NA=Not Applicable) (Sheet 3 of 3)**

| Register | Domain Address 00h | Input Power Domain Address 0Dh | Notes |
|---|---|---|---|
| 3Ah (WP0) | O | NA | Not used. Only listed as optional so there is no conflict with IMVP. |
| 3Bh (WP1) | O | NA | |
| 3Ch (WP2) | O | NA | |
| 3Dh (WP3) | O | NA | |
| 3Eh (WP4) | O | NA | |
| 42h (IVID1-VID)<br>44h (IVID2-VID)<br>46h (IVID3-VID) | O | NA | |
| 43h (IVID1-I)<br>45h (IVID2-I)<br>47h (IVID3-I) | O | NA | |
| 4A (Psys critical level) | NA | X | Required in Y, U, H and S |
| 4B (Psys warning 2 level) | NA | X | |
| 4C (Psys warning 1 level) | NA | X | |
| 4D (Psys warning 2 counter) | NA | X | |
| 4E (Psys warning 1 counter) | NA | X | |
| 4F (Psys critical assertion debounce time) | NA | X | |

## 2.3.1 $I_{OUT}$, Output Current (15h)

Platform Power Management requires the VR to report a digitized value of output current over the SVID bus. The VR must support, the averaging interval of total output current shown in Table 2-3. $I_{OUT}$ support is required in PS0-PS3, and every VID including 0V.

**Figure 2-1. $I_{OUT}$ Update Interval Example**

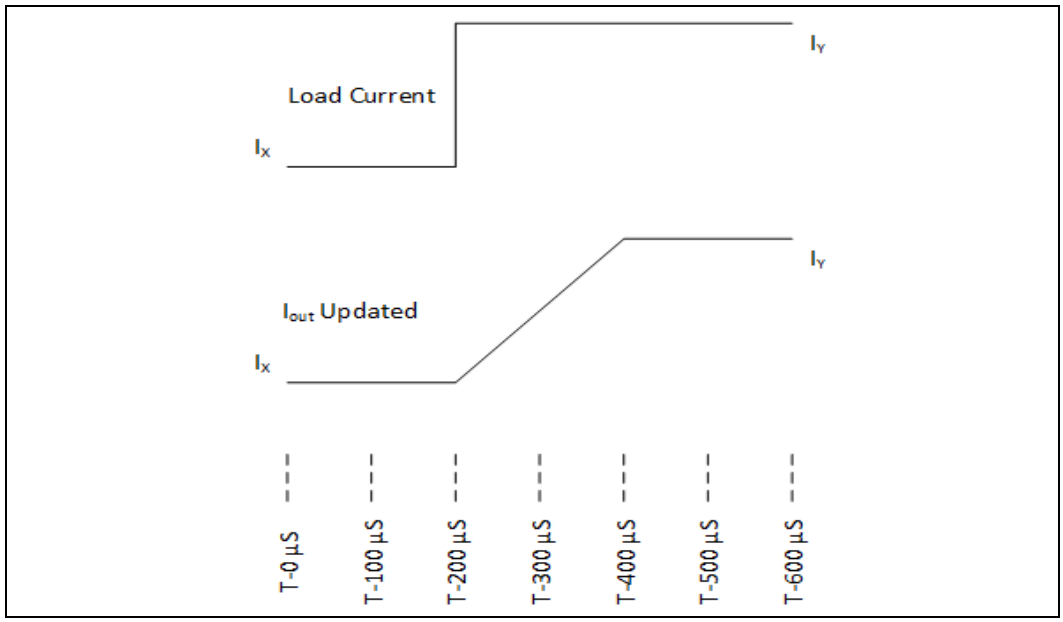



**Table 2-3. Averaging Interval and ADC Conversion Rates**

| Segment | Averaging Interval | ADC Conversion and Register Update |
|---|---|---|
| Client | 200 µs | 100 µs |

Figure 2-1 shows an example of $I_{OUT}$ being updated after a load change. At time T-0, the load and $I_{OUT}$ are at $I_X$. At time T-200, the load changes to $I_Y$. The $I_{OUT}$ register is updated with new data every 100µs, and after 200µs (time T-400µs), the $I_{OUT}$ register also reads $I_Y$.

Testing of $I_{OUT}$ will allow for register updates to occur up to time T-500 to allow for the 100us lag in register updates.

If averaging is done in the analog domain, the PWM vendor may choose the voltage scaling and gain terms for the analog current output pin. The voltage range should be specified in the data sheets to aide in lab testing and board debug.

The ADC should be scaled such that FFh= Icc_MAX for the VR for maximum resolution of the ADC data.

In PS0-PS3, and at every VID including 0V, the $I_{OUT}$ register must continue to reflect the averaged current of the voltage rail.

### 2.3.1.1 $I_{OUT}$ Data Encoding and ADC Resolution

(15h) $I_{OUT}$ register resolution must be ≤1% of ICCMAX per bit. All IMVP9 controllers MUST have 8 bits of ADC resolution.

### 2.3.1.2 VR $I_{OUT}$ Accuracy Targets

Accuracy is typically a function of the PWM internal circuits, external inductor or shunt and NTC temperature coefficient matching network. Below are typical, RSS 3-sigma platform accuracy targets (shown double-sided) for different phase configurations and different inductor and NTC tolerance assumptions**.** 3% or 1% NTC refers to an NTC temperature compensation resistor with a 3% or 1% initial tolerance. Tighter tolerance on current reporting will yield a platform with better 'turbo' performance.

***Note:*** It is strongly recommended that the Iout accuracy targets near TDP (indicated in green) are achieved to ensure that the performance is not compromised.

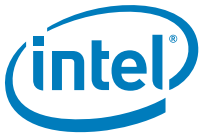
**Table 2-4. IOUT Accuracy Targets**

| VR Load (% of IccMax) | Iout Accuracy | | | |
|---|---|---|---|---|
| | 1 phase | 2 phase | 3 phase | 4 phase |
| 5% | 13% | 16% | 24.5% | 24.4% |
| 10% | 8.1% | 9.6% | 13.2% | 13.1% |
| 20% | 6.3% | 7.2% | 8.2% | 8.0% |
| 30% | 5.9% | 6.7% | 7.0% | 6.7% |
| 40% | 5.8% | 6.5% | 6.4% | 6.1% |
| 50% | 5.7% | 6.4% | 6.2% | 5.8% |
| 60% | 5.7% | 6.3% | 6.0% | 5.7% |
| 70% | 5.6% | 6.3% | 6.0% | 5.6% |
| 80% | 5.6% | 6.3% | 5.9% | 5.5% |
| 90% | 5.6% | 6.3% | 5.9% | 5.5% |
| 100% | 5.6% | 6.2% | 5.8% | 5.5% |
| DCR (mohm) | 5 | 4 | 4 | 4 |

## 2.3.2 JOUT, Output Joules

Register 15h may optionally be configured (selectable in the Compatibility register 06h) to report Joules for the rail.

- Supporting JOUT does not supercede the need for the VR to support $I_{OUT}$
  - Capability register(06h) bit 7 must be configurable to allow for $I_{OUT}$ operation
- Use IccMax (21h) scaled to FFh to represent $J_{OUT}$ in mJ/bit
  - IccMax/255 = mJ per bit
- If using an accumulator larger than 8 bits to provide data to 15h, use the 8 MSBs to populate $J_{OUT}$ (15h) at least every 100us
- Clear $J_{OUT}$ register (15h) when read
  - If using an accumulator larger than 8 bits to provide data to $J_{OUT}$ (15h), clear the 8 MSBs of the accumulator and leave the lower bits in the accumulator to add into the next read
- If register $J_{OUT}$ (15h) reaches the max value of FFh, do *not* roll the register over; leave the FFh value until the register is read, and then clear as normal



## 2.3.3 SVID Clock Behavior

The SVID Clock in IMVP9 has two aspects which are different than previous specifications.

### 2.3.3.1 Support Clock from CMOS Source

The SVID Clock may come from either an open drain, or CMOS source at 1.0-1.05V.

### 2.3.3.2 Move to Rest when SVID Command is Interrupted

The SVID Clock may be run continuously in IMVP9. In addition to the Clock stop requirements listed in the SVID PRotocol spec, the VR must move from the Listening state, to the Rest State when either of the following occurs:

- 36 clocks have elapsed since after the start pattern
- The Clock has halted for 500ns

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# 3 SVID Bus Electrical Features

## 3.1 SerialVID (SVID) Overview

SerialVID bus is a three wire (clock, data, alert) serial source synchronous interface used to transfer power management information between a microprocessor and one or more voltage regulator control ICs. For more information refer the *SVID Protocol Specification* document.

The Serial VID bus is a high speed data bus and bus routing should be done to limit noise coupling from VR phase nodes or MOSFET switching nodes. Do not route traces under any switching MOSFETs or phase nodes. The SVID lines must be ground referenced and each line's width and spacing should be such that they have nominal 50 Ω impedance with the board stackup. The PCB vendor can help with line and spacing recommendations based on the distance to the ground plane to achieve a 50 Ω impedance.

The 0Dh domain is not a VR and has no SVID controlled voltage output. Therefore it will not require support for the ALERT function. If the 0Dh domain SVID interface is supported by a second device, separate from the IMVP9 controller, that device would not require the ALERT output or support.

## 3.2 SVID DC Electrical Parameters

The following table outlines the DC electrical parameters. Note that low voltage operation is essential to avoid level converters to/from the processor. It is optional on the VR controller to bring in the VCCIO/VTT/VCCST voltage from the platform as a reference voltage for improved signal integrity at the receiver.

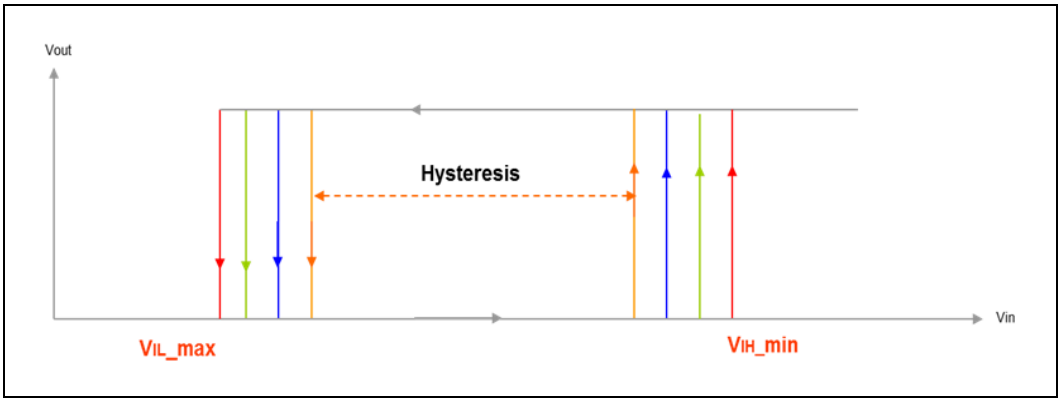
Refer Table 3-1 for voltage definitions.

**Table 3-1. VR DC Electrical Parameters**

| Symbol | Parameter | Min | Type | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{TT}$ | CPU I/O Voltage (also known as VCCIO) | 0.90 | 0.95 - 1.05 | 1.1025 | V | |
| $V_{IL}$ | Input Low Voltage | | | 0.45 | V | 1 |
| $V_{IH}$ | Input High Voltage | 0.65 | | | V | 1 |
| Vhyst | Hysteresis Voltage | 0.05 | | | V | |
| $V_{OH}$ | Output High Voltage | | $V_{TT}$ | | V | 1 |
| $R_{ON}$ | Buffer On Resistance (data line, alert# line, VR_Hot# line) | 4 | | 13 | Ohms | 2 |
| $I_L$ | Leakage Current | -100 | | 100 | µA | 3 |
| $C_{PAD}$ | Pad Capacitance | | | 4.0 | pF | 4 |
| Cpin | Pin capacitance | | | 5.0 | pF | |

***Notes:***
1. $V_{TT}$ refers to instantaneous $V_{TT}$.
2. Measured at 0.31 * $V_{TT}$.
3. VIN between 0V and $V_{TT}$.
4. $C_{PAD}$ includes die capacitance only. No package parasitics are included.

## Figure 3-1. Definition of Vhysteresis




## Table 3-2. VR AC Electrical Parameters

| Symbol | Parameter | Min | Type | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Vmax | VDS Max open drain buffer to accommodate ringing on bus | -1.0 | | 3.3 | volts | |
| SR Fall Data | | 1.2 | | 4.08 | V/ns | Load: Rpu=64.9Ω |
| SR Rise Data | | 1.1 | | 3.62 | V/ns | Load: Rpu=64.9Ω |
| SR Fall Alert/VR_Hot | | 1.25 | | 4.2 | V/ns | Load: Rpu=75Ω |
| SR Rise Alert/VR_Hot | | 1.15 | | 3.33 | V/ns | Load: Rpu=75Ω |

Slew Rate (SR) is measured between 0.735 V and 0.315 V (VccST=1.05 V). SR is measured at the output of the buffer; Rpu is connected to VCCIO as a load with no additional capacitance on the board. The slew rate is defined with the VR buffer capacitance only.

## 3.3 VCLK Timing Parameters

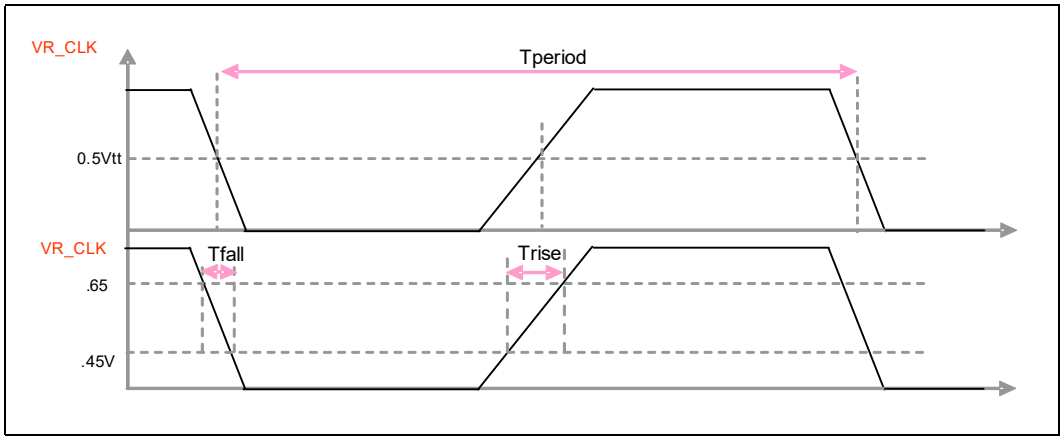
The VCLK AC timing specification is an input specification for SerialVID devices. The VCLK output device must be designed to meet this specification at the clock receiver. The VCLK output device must have a platform design specification that guarantees that its VCLK output meets this AC timing specification at the VCLK receiver. Refer Figure 3-2 The receiver clock should be edge triggered to detect the first falling edge of the clock when it restarts from an idle or high state.

**Table 3-3. VCLK AC Timing Parameters**

| Symbol | Parameter | Min | Type | Max | Units | Notes |
|---|---|---|---|---|---|---|
| | VCLK Frequency (Intel processor POR, different segments will use different Vclk frequency) | 10 | 25 | 26. 25 | MHz | 1, 4, 4 |
| Trise | VCLK Rise Time (@VR Pad) | 0.25 | | 5.5 | ns | 2 |
| Tfall | VCLK Fall Time (@VR Pad) | 0.25 | | 5.5 | ns | 2 |
| | Duty Cycle | 40 | | 60 | % | 1, 4 |

***Notes:***
1. Period and duty cycle are measured with respect to 0.5 * VTT. Refer Figure 3-2
2. High and low time is measured with respect to 0.5 * $V_{TT}$.
3. Rise and Fall times are measured from .45V and .65V. Refer Figure 3-2.
4. Tperiod, Thigh, Tlow and Duty Cycle variation as a result of internal CPU Clock logic only. Additional variation may be introduced as a result of the Clock MB topology (like different Rpu values or MB impedance).

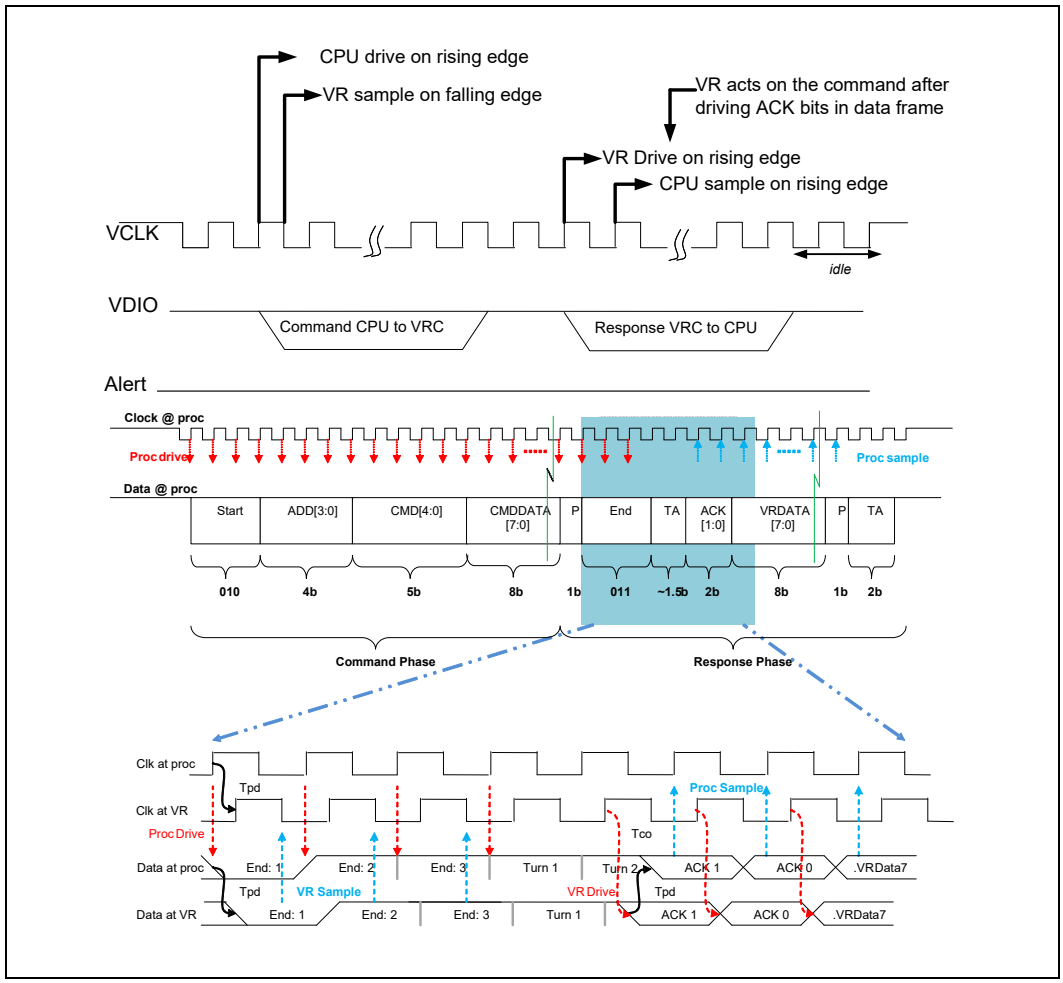
**Figure 3-2. Measurement Points for VCLK High, Low, Rise and Fall Time, Tperiod**




## 3.4 Data Sampling and Timing Analysis

The clock to data delay or skew is different in the CPU or master vs. the VR control IC. To accommodate this and flight time and the process technology differences between the CPU and the VR, the data is sampled on different edges of the clock depending on the CPU or the VR driving data on the bus. Refer Figure 3-3.

## Figure 3-3. Serial VID Bit Transfer Concept

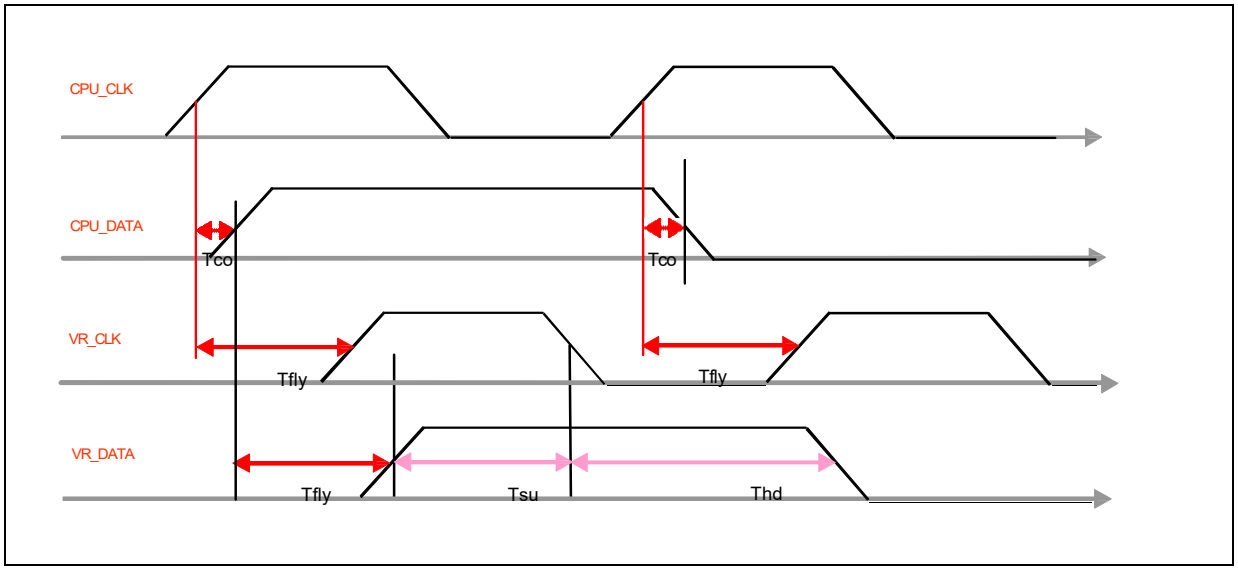



***Notes:***
1. Sampling changes depending on CPU driving data or VR driving data on the bus
2. Refer SVID Protocol for detailed bit timing on data words

## Table 3-4. Platform Bus Timing

| Parameter-Description | Value |
|---|---|
| Tco_max_VR Clock to data delay | 12 ns |
| Tco_min VR clock to data delay | 4 ns |
| Tsu_VR - Setup time of signal VDIO at VR side | 7 ns |
| Thld_VR - hold time of signal VDIO at VR side | 14 ns |
| Tco_max_CPU Clock to data delay @bump | 0.65 ns (measured vs. Rpu of 50 Ω without the channel, this value can change as a result of different Rpu and channel loads) |
| Tco_min_CPU Clock to data delay @bump | -3.6 ns (measured vs. Rpu of 50 Ω without the channel, this value can change as a result of different Rpu and channel loads) |
| Tsu_CPU - Setup time of signal VDIO at CPU side | 1 ns |
| Thld_CPU - hold time of signal VDIO at CPU side | 3 ns |

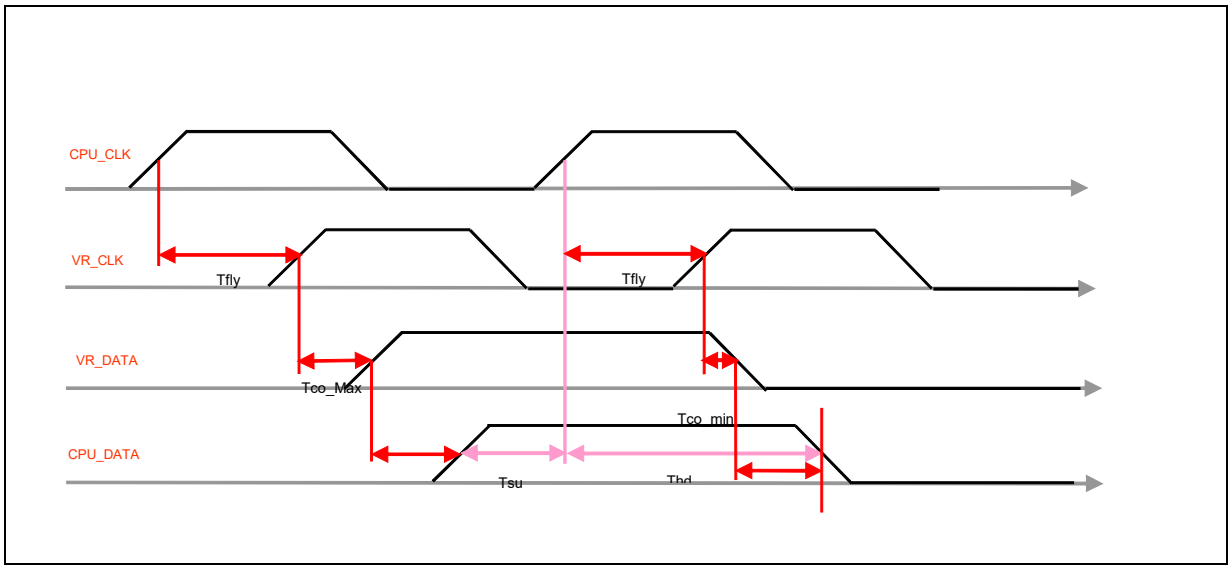
## Figure 3-4. Clock and Data Sample CPU Driving Timing Definitions




***Notes:***

1. All timings shown at VR or CPU pads, not at the pins
2. Tfly = propagation time on the serial VID bus

## Figure 3-5. Clock and Data Sample VR Driving Timing Definitions




***Notes:***

1. All timings shown at VR or CPU pads, not at the pins.
2. Tfly = propagation time on Serial VID bus.

§ §

# 4 VID Table and Operation

IMVP9 uses an 8-bit hex code to identify specific voltage levels for the VR controller to regulate to. Changes between VID levels are done with a SetVID command to the new voltage level identified by VID.

## 4.1 VID Table

Off code = 00h sets output to zero volts, not switching, no active pull down except VR_Ready which is set per the Multi_VR_Config register setting. As long as enable is asserted, the SVID bus is idle waiting on next instruction. The PWM IC should respond to all SVID commands while the output is set to zero volts. SetVID_Slow or SetVID_Fast will be used to turn the VR back on by ramping to a voltage; ACK a SetPS0/1/2/3 command and do nothing since VR is already in low power state for that output voltage and current; ACK and send payload on a GetReg command. PS4 has special conditions and exceptions to these requirements. Refer Section 4.3.5 for more information on PS4 operation.

If the Multi_VR_Config register is set to 01h, then the VR_Ready line will remain asserted when receiving a subsequent 00h VID code. Refer SVID protocol for more information.

- **DAC accuracy is a recommendation only.**
  Total tolerance band must be met, i.e., Ripple + RSS sum of DAC set point + current sense AVP LL droop accuracy. Refer applicable platform design guideline for the tolerance budget.

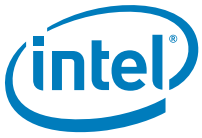
Refer platform power design guidelines for more information on power states and VID ranges.

**Table 4-1. VID Tables**

| VR Domain | Prot ID reg 05h | VID 00h | VID 01h (V) | VID Step Size | VID FFh (V) | Recommended Accuracy | VID Decode Formula |
|---|---|---|---|---|---|---|---|
| VccIn 00h | 08h | Off | 0.20 | 10mV | 2.74 | 0.0 - 0.495V = +/- 10mV<br>0.5 - 0.795 = +/- 8mV<br>>0.795 = +/- 0.5% * VID | =0.19+0.01*<br>HEX2DEC(VID) |

## 4.2 Dynamic Voltage Identification (D-VID)

The SVID bus will be used to send out a new target voltage and slew rate command to the PWM IC. The VR responds by slewing to the new voltage in a controlled manner without false tripping of VR_Ready, over voltage or over current protection circuits. If the VR is in a low power state (PS1, PS2, PS3 or SetVID_Decay) and receives a SetVID_Fast or SetVID_Slow (up or down) the VR should return to power state PS0 enabling all phases to slew the voltage at the commanded slew rate. There should be no delay in the power state exit to PS0 for a SetVID command. The VR will remain in PS0 until the CPU commands it to re-enter a low power state.



During Dynamic VID operation, the VR's OVP circuitry should be designed to prevent false tripping due the output voltage lagging the DAC set point. Examples of this are to have the OVP set at ~400 mV (Max) above highest VID voltage. Do not reset OVP threshold as DVID commands a lower voltage. Another method would be to blank the OVP circuits until the VR has settled to the new DAC value. It is left to the vendor as to the implementation method to avoid false tripping of OVP circuits.

## 4.2.1 Dynamic VID Slew Rates

### 4.2.1.1 SetVID_Fast

The SetVID_Fast slew rates are shown in Table 2-2.

### 4.2.1.2 SetVID_Slow

The SetVID_Slow slew rates are shown in Table 2-2.

### 4.2.1.3 SetVID_Decay

VR_Settled and Alert# functions are required for SetVID_Decay to voltages other than 0V.

- The SetVID_Decay command will put the rail in PS2 unless the rail is already in PS3, then the rail should remain in PS3
- The VR VID/voltage DAC must track the output voltage as it decays
- Alert# will assert when the output voltage has decayed to the target voltage level when the voltage is not 0V.
- SetVID_Decay can be preempted at any time with a target VID higher (by SetVID_Fast or Slow) or lower (by any Set_VID) than the current decay voltage state. The PWM must exit the decay ramp and slew to the new voltage target. T_Alert timing must be met for the new preempted SetVID_Fast or SetVID_Slow command.
- In the case of SetVID_Decay to same VID, VR should ACK the command and assert alert (except at 0V) as the VR is already at the target voltage.
- SetVID_Decay to a higher VID should be rejected.

## 4.2.2 T_Alert and Voltage Settled Function

The VR PWM control IC needs to have a method that detects when the DVID transition is complete. Refer Figure 4-1 and Figure 4-2 for more information. The VR settled function and timings are required on both the multi-phase and single-phase rails. The VR settled function is critical to processor function when moving from a lower VID to a higher VID.

After the VR has ramped, it asserts the VR settled bit in the status register and asserts the Alert# line. The VR Settled bit in the status register is a representation of the actual voltage output. 1= VR is at target VID, 0= VR is slewing to new target. This bit toggles asynchronously with the status of the output voltage changes (settled at VID or slewing). Refer the "SVID Protocol Specification" document for more information on the registers and Alert# line. The final DC-DC design must meet the SetVID slew rate and

final settling time; this will set an upper limit on the value of the inductance and capacitance, particularly on the single-phase rail to meet voltage slew rates and settling to within the tolerance budget.

The VR settled function eliminates the CPU waiting for RC charging time constants for various platform decoupling configurations. A fast response VR with small capacitor banks will settle faster than a slow VR with large capacitor banks and enhance the end user experience. The VR is required to meet the minimum slew rates.

T_Alert is calculated from the last VID the VR asserted the VR_Settled bit at, not the voltage level the VR may presently be at, e.g., starting from a settled voltage of 500mV, a SetVID_Slow to 1.0V that preempts a SetVID_Slow to 800mV will have 500mV/(Slow Slew_rate) to reach 1.0V regardless of the voltage level at the output.

VR_Settled and ALERT# assertion is required after Decay commands to voltages other than 0V, although there is no timing requirement associated with either the slew rate or settle time. Assertion after Decay should be when the voltage output reaches the targeted VID level.

#### 4.2.2.1 Alert# Behavior on SetVID to 0V Commands

The exception to Alert# assertion, is for SetVID commands to 0V. Alert# must NOT be asserted after SetVID_Slow/Fast/Decay commands to 0V.

#### 4.2.2.2 Undershoot Allowance

During PS state changes and SetVID changes to a lower VID, the voltage may be allowed to ‘undershoot’, or go below, the final settled voltage level. The amount of undershoot allowed will be defined in the corresponding platform design guide or power delivery design guide, and may be 0mV. Measurement of undershoot is from the lowest point of the droop to the bottom of the ripple of the final settled voltage.

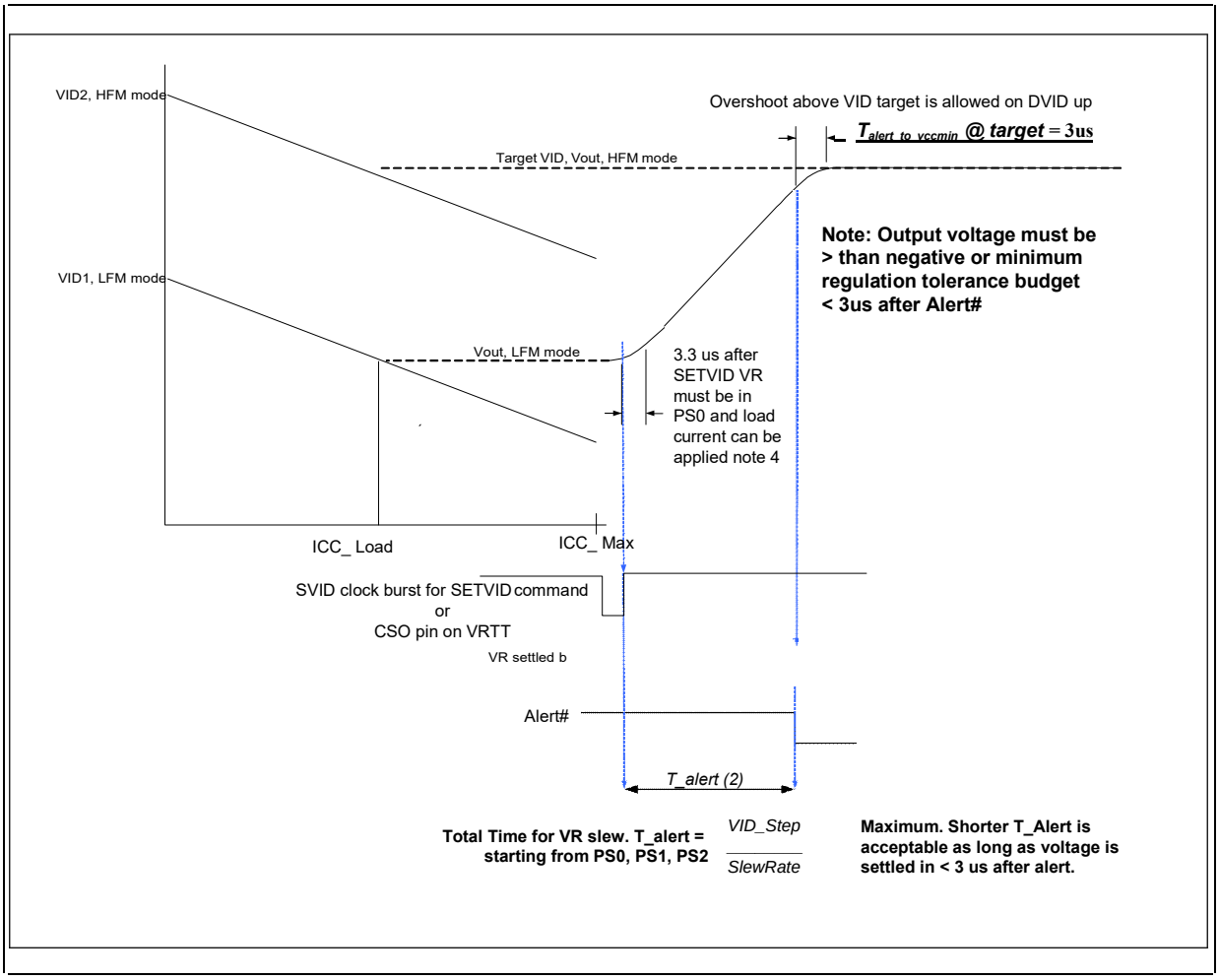
Expect no undershoot allowance for IMVP9.

#### 4.2.2.3 Overshoot Allowances

Overshoot is allowed for a SetVID going up. The overall goal is for the output voltage to reach the new target window in the fastest possible manner as this result in a superior performing platform. Overshoot is above TOB + Ripple.

Load release overshoot is defined separately. Refer to PAG and EDS for specifications.

## Figure 4-1. VR Settled, T_Alert Moving from Lower to Higher, Starting From PS0, PS1, PS2




***Notes:***

1. 20 – 80% is for measuring SetVID Fast, SetVID_Slow for slew rate validation in the test lab. The non-linear regions < 20% and > 80% should be minimized in the PWM control loop. Actual slew rate is not critical as along as T_Alert timing is met.

2. T_Alert <= $\frac{VID\_Step}{SlewRate}$ Maximum. Shortening T_Alert timing improves CPU performance.

3. It is critical that the output voltage be within the TOB within 3µs after T_Alert. VR TOB is defined per platform and is documented in the applicable platform design guidelines.

   The VR must be able to respond to full load step 3µs after T_Alert and not violate Vmin targets as the CPU will re-lock PLL at a higher frequency and may require large current steps.

4. Dynamic loading currents can be applied during voltage ramp. PWM must auto exit PS1, PS2 or PS3 and meet T_Alert timing for any SetVID command up or down.

## Figure 4-2. VR Settle, T_Alert Starting from PS3 with SetVID Command

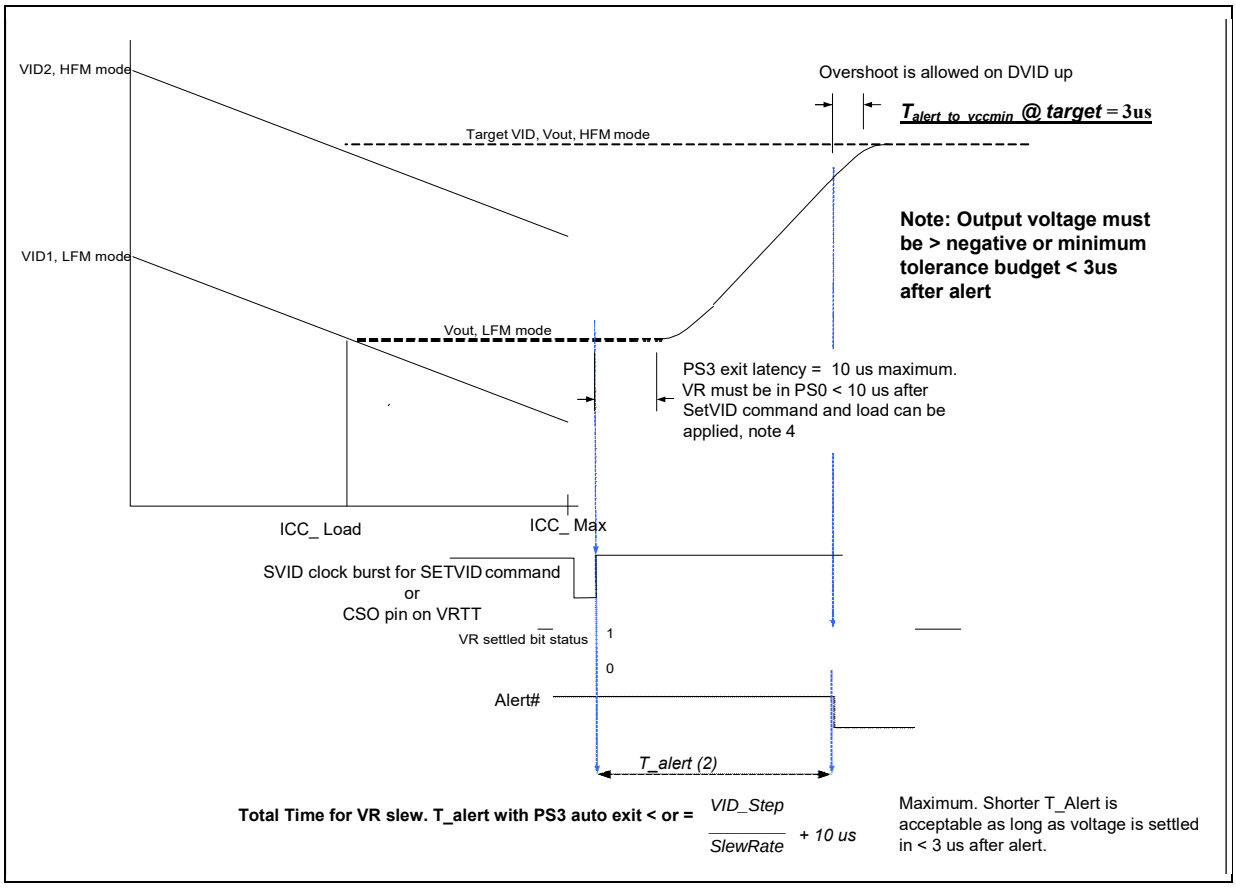
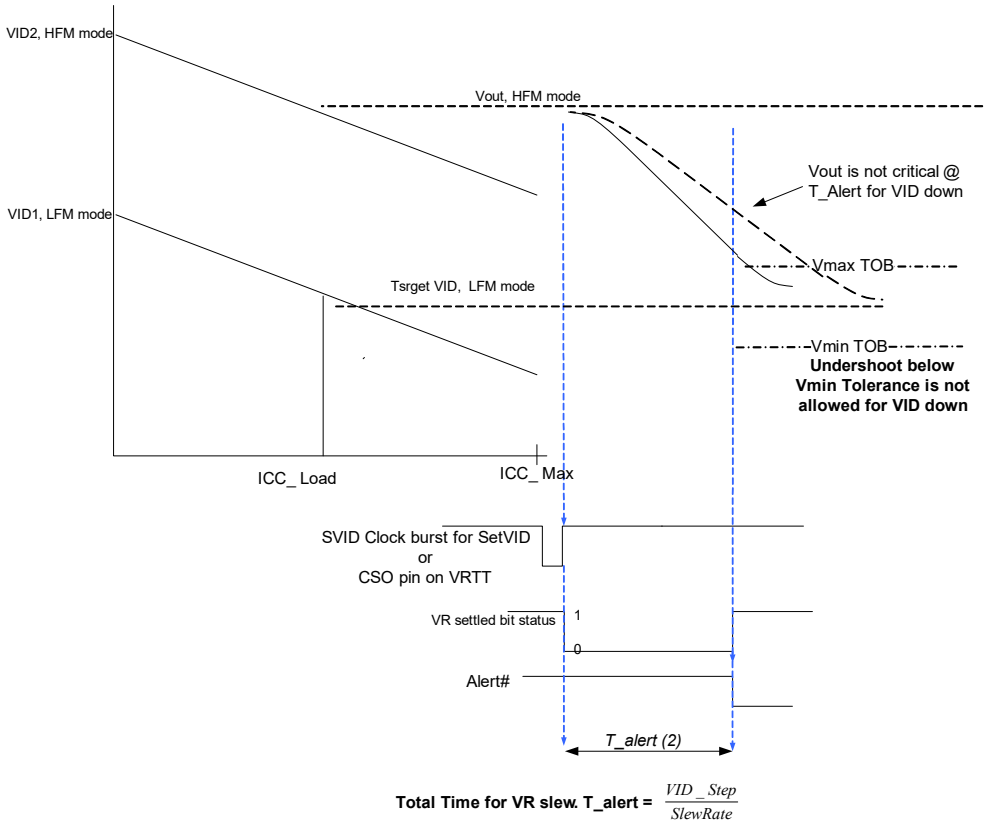


**Figure 4-3. VID Down VR_Settled and T_Alert**

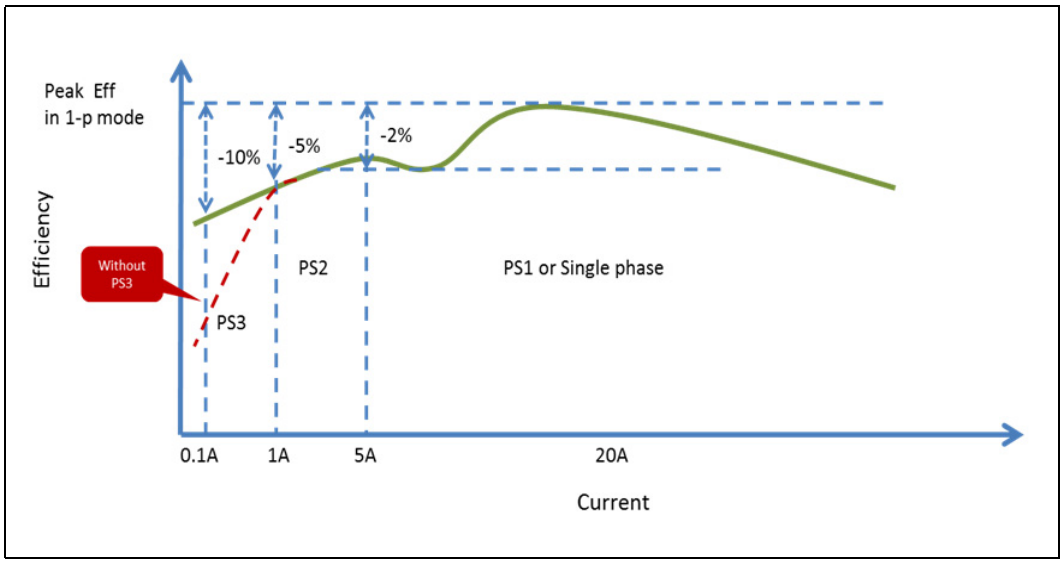



**Note: T_Alert timing must be met regardless of starting power state or back to back SetVID & SetPS and a SetVID_Decay preemption. Preemption can occur at any time and VR must exit low power states or Decay mode to PS0 and ramp to new target and meet T _Alert timing for the preempted VID target command**

## 4.3 VR Power States (PS)

The SVID bus can be used to place the VR into multiple VR states for high efficiency/ light-load conditions. These states are entered by programming the power state register using the SetPS SVID commands. The VR is expected to optimize its power loss to flatten the efficiency curve over the operating current range with the Power State commands that indicate the CPU load current. Actual voltage and current levels in each power state will be detailed in the VR design guidelines and processor EDS specifications, but may be set by customer design. VID and Power states are independent and either one can change at any time as determined by the CPU operating state.While changing power states, overshoot relief is allowed similar to load-line overshoot specification when the load is released. Undershoot allowance may be allowed as shown in Section 4.2.2.2.

**Figure 4-4. Example of Efficiency Targets in Various Power States**




***Note:*** To improve light-load efficiency, ripple will be allowed to increase as the load decreases, regardless of PS states. Platform design guidelines will provide ripple specifications.

The PWM should exit any low power state and return to PS0 for SetVID_Fast or SetVID_Slow up or down command. If after reaching new higher voltage, the CPU is still in a low current state, it will re-issue PS command to enter High Efficiency, Light-Load mode.

### 4.3.1 PS0

The VR is capable of providing the highest power levels demanded by the processor.

***Note:*** The new definition removes the necessity of having all phases 'on' while in PS0. The implication here is that a VR may opt to shed phases if it can still respond to full load current without violating any other specifications.

### 4.3.2 PS1

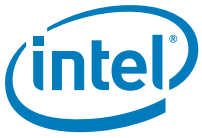
During the PS1 state, the CPU announces to the VR that it is in an active mode that requires limited amount of current; < 20A typical. The VR needs to put itself in a higher efficiency mode to take advantage of the reduced potential current.The platform design guidelines, or customer needs will specify the PS1 threshold.

### 4.3.3 PS2

Used in Sleep Mode and it represents a lower current state than PS1. <5 A typical, may be discontinuous conduction mode, typically used to enable diode emulation mode.

### 4.3.4 PS3

PS3 is an ultra-low current mode lower than PS2; < 1 A typical. PS3 can be used to lower bias power of the PWM IC, change pulse frequency rate, etc.



Support for PS3 is required, even if the VR does not change configuration for PS2 to PS3, it should acknowledge the PS3 command and optimize itself for the low-power state.

For SetVID_Decay followed by SetPS3, the VR can change to PS3 configuration while slewing or at the end of the ramp.

PS3 has a 10µs exit latency applicable to any SVID command requiring the VR to exit the PS3 state.

***Note:*** In PS3 the $I_{OUT}$ register must continue to reflect an averaged current of the voltage rail. The value does not need to be measured. This average is to be maintained so that the next measured (higher current) value is averaged into the low current average rather than starting a new average.

## 4.3.5 PS4

A near "off" condition for the IMVP9 controller. SetPS4 may be sent at any VID (there is no requirement for the VID to be at 0V prior to SetPS4 being sent to the IMVP9 VR controller).

### 4.3.5.1 PS4 Entry

After ACKing the SetPS4 command, the following behavior is expected from the VR:

- Immediately enter PS4, halt regulation, and output switching
- Set VID and DAC to 00h (0V)
- Do not delay PS4 entry while the output decays
- Alert# must remain de-asserted while in PS4
- VR_Ready remains asserted/de-asserted per the Multi-VR Config Register (34h)
- Total VR controller quiescent power for U/Y/H processor applications (S-line processors have no power target)— after all VR outputs have received SetPS4 commands — is **<500 µW** (includes all VR circuitry, including designs using 2 VR or more controllers)
- The Input Power domain at address 0Dh will follow the last voltage rail in the package into PS4. No SetPS4 is required by the 0Dh domain, however if one is received, the VR must respond with ACK.
- In S-line platforms, the VR must support the 12V rail being turned off during PS4. All 3.3V, 5V, and all logic will remain powered. 12V will be stable again before any PS4 exit command is sent.

Any valid GetReg command to a domain in PS4 will be responded to with ACK and a payload of 00h. The VR will consume as little power as possible while responding to GetReg commands.

***Note:*** It is recommended that a domain in PS4 disable all non-SVID circuitry to minimize device power consumption.

#### 4.3.5.2 PS4 Exit

A VR domain in PS4 will exit PS4 when it receives a SetVID (Fast/Slow/Decay) or SetPS0/1/2/3 command addressed to that domain. The Input Power domain at address 0Dh will follow the first VR out of PS4 and go to a PS0 (operational) state. All other VR domains will remain in PS4 until they receive their own SetVID or SetPS0/1/2/3 command.

- The output voltage may NOT be assumed to be 0 V when the next SetVID command is received. Discharging a pre-charge on the output voltage to 0 V prior to ramping to target voltage is NOT allowed.
- $I_{OUT}$ and $I_{OUT}$ value retention or averaging is not required in PS4. The $I_{OUT}$ register (15h) must contain valid data ≤200 µs after asserting ALERT in response to the PS4 exit SetVID command.

### 4.3.6 Power State Exit Latencies

Any SetVID command up or down causes a PS0 auto exit and the VR must ramp to the new voltage target and meet the T_Alert timing. Refer Figure 4-1 VR_Settled/T_Alert timing. The auto exit condition can happen any time during voltage ramp preemption, to a higher or lower voltage target.

- PS1 to PS0, PS2 to PS0 exit due to SetVID up command, exit latency is zero. Refer Figure 4-1 VR_Settled/T_Alert timing is the same starting from PS0, PS1 PS2. The VR should move to PS0 then start ramping the voltage simultaneously with no delay. Any latency performing the auto exit from PS1, PS2 back to PS0 must be compensated by the voltage ramp. T_Alert = VIDstep/Ramp Rate timing must be met regardless of the starting in PS1 or PS2 and applies to small VID steps or large VID steps. Dynamic currents can occur during voltage ramps. Small dynamic load current steps can be applied 3µs after the SetVID command during the voltage ramp.
- PS3 exit latency is 10 µs, added to T_Alert specification, refer Figure 4-2.
- PS1 to PS0 without an accompanying SetVID: < 3.3µs for full load step, note phases must be added in < 500 ns after ACK of SetPS0 command.
- PS2 to PS0 without an accompanying SetVID: < 3.3µs for full load step, note phases must be added in < 500 ns after ACK of SetPS0 command.
- PS2 to PS1 without an accompanying SetVID: is zero, no delay on DCM/CCM mode change
- PS4 exit latency is **≤ 90 µs**. The latency is measured from the ACK of the SetVID or SetPS command to:
  - the beginning of ramp from 0 V for SetVID.
  - being ready to ramp the output (for SetPS).

**Equation 4-1.PS4 Latency Equation**

$$TAlert \leq \frac{VIDstep}{Slewrate} + 90\mu s$$

When exiting PS4, VIDStep of the TAlert calculation is always calculated from 0V, regardless of any pre-charge on the output.

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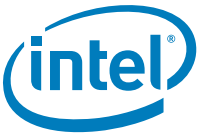


# 5 Start-up Sequence

At power up—after the PWM Vcc is greater than the UVLO voltage and enable is asserted—the VR reads its pin programming values, or NVRAM register default values, during the time period Ta of the VR enabling sequence. The VR is to follow the start-up sequence as called out below for non-zero $V_{BOOT}$ and zero-volt $V_{BOOT}$ cases.

IMVP9 start-up sequence:

1. VR has power and chip VCC is > UVLO voltage.
   Note: V1.00S may not be available at this point; all SVID bus open drain outputs will be floating.
2. VR receives hardware enable.
3. If $V_{BOOT}$ is enabled, $V_{BOOT}$ rails ramps to $V_{BOOT}$ at slow slew rate as set by the default setting in the Slow Slew Rate Selector register (2Ah)
4. If Vboot is enabled,IMVP9 PWM asserts ALERT when target is reached
5. At the end of the $V_{BOOT}$ ramp, VR asserts VR_Ready.
6. If Vboot is set to 0V, VR_Ready should assert when the VR is ready for SVID commands.
7. VR SVID bus is active and idle
8. CPU sends out initial SVID command sequence, reading various SVID ID registers.
9. CPU may program Slew Rate Slow register (2Ah) to non-default value
10. CPU sends out “SetVID_Slow/Fast” command to set the proper output voltage
11. VR acknowledges and ramps to the voltage specified by the SetVID_Slow/Fast command at the slew rate specified by the SetVID command.
12. IMVP9 PWM asserts ALERT when target is reached
13. Start up sequence over.

Refer applicable platform design guidelines for detailed power sequencing of all the platform rails.

Figure 5-1 and Table 5-1 summarize the VR startup timing requirements.

**Figure 5-1. VR Start up Timings**

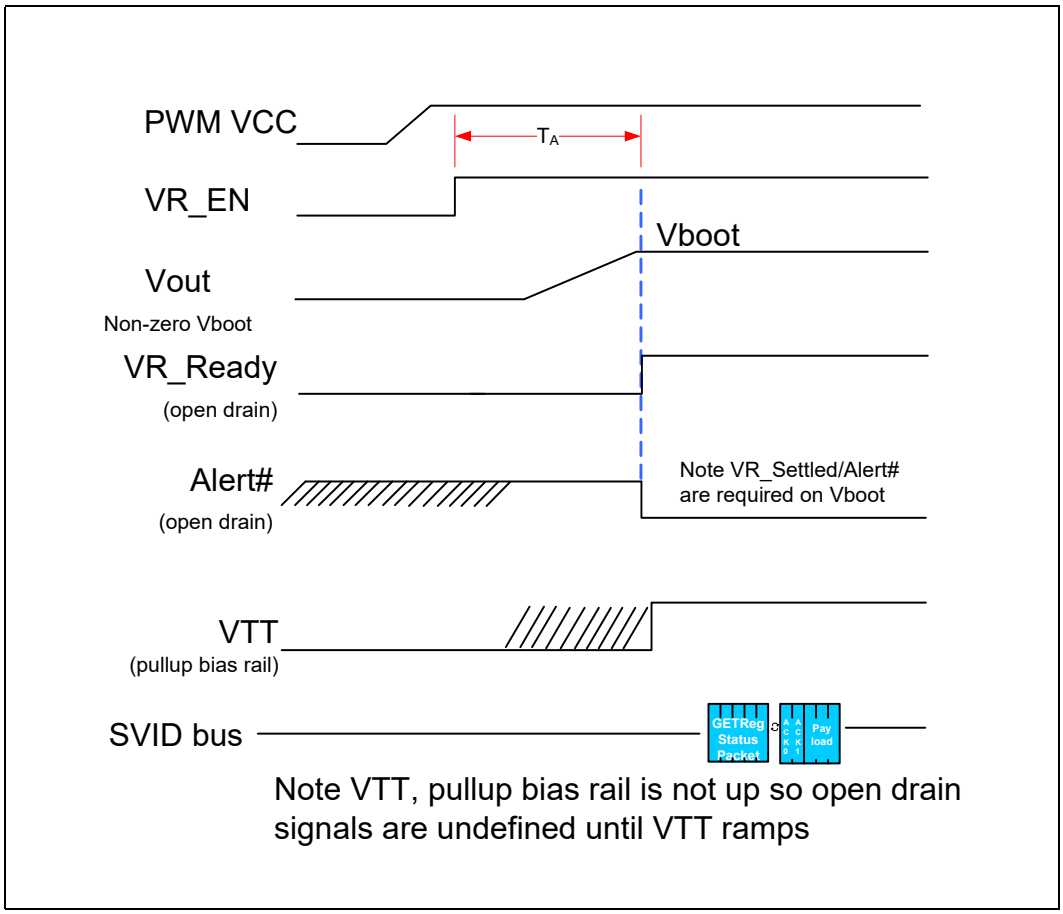



**Table 5-1. VR Start up and Enable Timings**

| Description | | Min | Typ | Max | Note |
|---|---|---|---|---|---|
| $T_A$ | VR_EN to VR_Ready. The later of either $V_{BOOT}$ completing or the PWM IC is ready to accept SVID commands. | | | **2.5 ms** | PWM IC must complete all internal analog and digital configurations and reset protocols during $T_A$. Duration may be disclosed to CPU through register 2Dh. With Multi-VR Config bit 0 set, VR_Ready should only de-assert for faults. |
| $T_D$ | External de-assertion of VR_EN to the internal recognition of VR_EN de-assertion (glitch filter) | **0 µs** | | **1 µs** | Refer Figure 5-2 |
| $T_E$ | VR_EN internal de-assertion to VR_Ready de-assertion | | | **500ns** | When VR_Ready de-asserts, the system may immediately assert VR_EN. Refer Figure 5-2 |

## 5.1 VR-Enable - Required for All Segments

VR_Enable pin is active high and is compatible with 1 V logic (VIH = 0.8 V). A single enable pin controls both outputs on a dual output VR control IC.

When VR_Enable is asserted, SVID bus is active and in an idle state waiting for first commands and initial voltage target. When VR_Enable is pulled low or disabled the DC-DC should shut down in a manner that limits the amplitude of below ground ringing to less than 100 mV. It is permissible to have a small current sink <1 mA when the VR_Enable is de-asserted to bleed off voltage on the output capacitor bank. The VR may reset all register values upon VR_Enable de-assertion.

During the shut down process, no negative voltage below –100 mV may be present at the DC-DC output when loaded with a resistive load or microprocessor in the system.

***Caution:*** Some electronic loads with long leads may cause false readings at turn off.

**Figure 5-2. VR Enable De-assertion Timings**

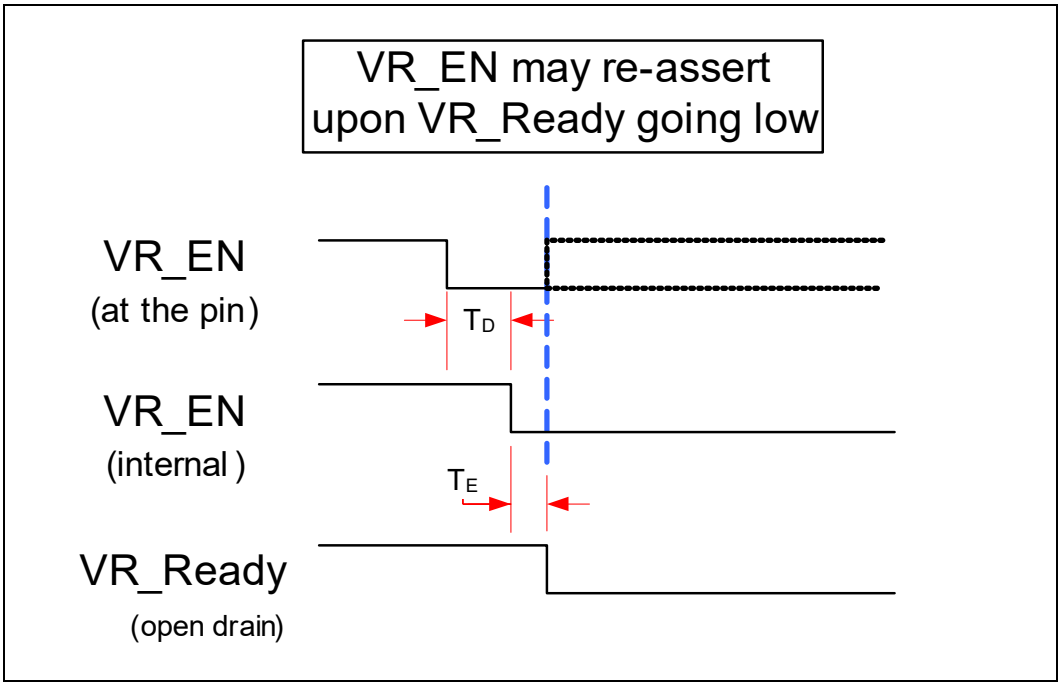



**Table 5-2. Enable Pin Voltage Levels**

| Symbol | Parameter | Min | Nom | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| VR_Enable or VR_On | ON/OFF control signal for voltage regulator. CMOS logic. | 0 | 1.0 | 3.3 | V | Input Signal from Platform Logic.<br>When high, the voltage regulator ramps up to $V_{CC-CORE}$.<br>When low, the voltage regulator is disabled. |

## 5.2 Under Voltage Lock Out (UVLO)

The PWM IC should detect the Vcc input and remain in the disabled state until valid Vcc level is available or reached. Ultimately the PWM vendor should set the level to meet his market segment requirements. However, the PWM and driver chips should coordinate start up such that both the PWM Vcc and power conversion rail (typically 5.6-19 V in mobile platforms) of the buck converter are both up and valid prior to enabling the PWM function. The PWM and Driver combination need to be tolerant of any sequencing combination of 3.3 V, 5 V,12 V, $V_{BAT}$/adapter input rails. If the Vcc rail falls below the UVLO thresholds, the PWM should shutdown in an orderly manner and restart the start-up sequence.

For the desktop segments supporting Modern Standby and newer, lower power regulatory requirements with deeper Cstate support (C10), the input voltage supply may change from 12V to 5V during CS, or go to 0V. UVLO must not shut down the VR for this configuration.

For example when the VR is at 0V (VID=0V in PS3 or in PS4) the VR controller should support the following:

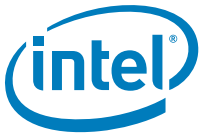
1. The controller power supply VCC will remain powered if powered from 5V. If powered from 12V, the controller will move to 5.0V in Connected Standby.
2. The power stage power will be removed if powered from 12V.

The controller must:

1. Not UVLO or fault in any way.
2. Not pull low or glitch VR_READY in response to loss of power stage voltage or the controller VCC dropping to 5V.
3. Exit 0V VID normally after all rails have been restored and upon receiving a SETVID to a non-zero voltage.
4. Maintain all register settings through entry and exit of this power state with out loss of data in any way.

One method to coordinate driver & PWM start up would be for the driver to actively hold the PWM input low, this way the PWM Control IC could sense if the driver was below its UVLO threshold or there was another fault in the driver.

§ §



# 6 General Operation

## 6.1 Phase Current Sense Input

The type of current sensing is determined by the tolerance band calculations. Common methods for current sensing are shunts, inductor DCR, MOSFET RDSon and silicon based current mirrors. Due to the large variation in RDSon between manufacturers and from lot-to-lot variation, Intel does not recommend RDSon sensing for AVP functions. RDSon sensing is acceptable for phase current balance. Inductor DCR or silicon-based current mirrors are recommended to implement AVP functions to minimize tolerance band.

The current sense amplifier should be able to work with low resistances in the range of 0.3 - 2.0 mΩ for compatibility with low loss-inductors and shunts.

## 6.2 Error Amp Specification

The error amp should be designed with a sufficient gain-bandwidth product to ensure duty-cycle saturation does not occur with large signal current transients. The output of the error amp should also support high slew rates to avoid duty-cycle change delays.

## 6.3 PWM Operating Frequency

Typical per-phase switching frequencies will be from 200 kHz up to 1 MHz with corresponding VR closed-loop gain-bandwidths of 50 kHz to 250 kHz, respectively.

For fixed-frequency PWM topologies, the tolerance of the PWM oscillator should be <+-10%. This applies to power state 0 (PS0) normal operating mode only. In PS2 and PS3, the PWM is allowed to vary its frequency or pulse skip.

Vendors with variable frequency topologies should document the limits of the frequency range over load and VID. Operation at no load and full load should not cause frequency run away.

The design of the VRD and output capacitor technology selection will determine the operating frequency and target closed-loop gain-bandwidths.

## 6.4 Differential Remote Sense Input

The PWM controller must include differential sense inputs (remote sense, remote sense return) for each PWM control loop. The remote sense will be used for “die sensing” and to compensate for output voltage droop due to parasitic resistance in the output power planes, sockets etc. The remote sense lines should draw no more than **<500 µA** to minimize offset errors. The remote sense input needs to have sufficient CMRR to reject high frequency processor noise to the VR output.

In the case of a multi-VR configuration, multi-differential remote sense pairs must be routed to the PWM control IC.

# 6.5 Output Indicators

## 6.5.1 VR_Ready

VR_Ready is an active-high output that indicates the start-up sequence is complete, the VR is ready to accept an SVID command and the VR is operating properly. For a multi-output PWM IC, only one VR_Ready line is required. The signal should remain asserted during normal DC-DC operating conditions and de-assert for any fault (OCP, OVP, etc.) or shutdown conditions on any rail within the multi-output PWM IC. The VR_Ready lines should not false trip during any dynamic VID transitions. Refer Table 6-1 for signal specifications.

**Table 6-1. Open Drain Output Signal Specifications (VR_Ready)**

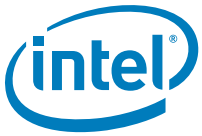
| Signal Type | | Open Collector/Drain Logic output from PWM IC, with external pull-up resistor and reference voltage. | | | |
|---|---|---|---|---|---|
| HIGH | | Active / Asserted | | | |
| LOW | | Not Active / De-Asserted | | | |
| **Symbol** | **Parameter** | **Min** | **Max** | **Units** | **Remarks** |
| VOH | Output Voltage High | 0.8 | 3.3 | Vdc | VCCIO rail is expected; however, some systems may pull-up to a maximum voltage of 3.3 V, with external pull-up resistor; Open Coll. /Drain Trans. OFF, Imp. >100kΩ depending on system implementation |
| VOL | Output Voltage Low | 0 | 0.3 | Vdc | With external pull-up resistor;<br>Open Coll./Drain Trans. ON |
| IOL | Output Low Sink Current | 1.0 | 4.0 | mA dc | Current limit set by external pull-up resistor |
| | Transition Edge Rate | | 150 ns | | From 10-90% rise |

## 6.5.2 Thermal Monitoring (SVID Thermal Alert and VR_Hot# output) Required for all Segments

IMVP9 has thermal monitoring circuits with two trip points for signaling to the CPU that the VR is overheating. The 1st trip point is for the SVID thermal alert communicated through the SVID status1 (10h) register. The 2nd trip point is for VR_Hot# output signal pin. VR_Hot# is required to be routed to the processors PROCHOT# input pin to initiate the thermal throttle low power state of the CPU to protect the VR from overheating. VR_Hot# may also be routed to various system thermal management controllers.

VR_Hot#, is Open-Drain logic, active low and will be used to drive the CPU's force thermal throttle input. VR_Hot# driver needs to be < 13 Ohm resistance to meet the CPU signal integrity requirements, similar to the SVID Alert#. VR_Hot# is typically pulled up to the platform's VCCIO (1.0 - 1.05V) rail. VR_Hot# output buffer should meet the requirements in Table 3-1 and Table 3-2.

The thermal sensor should be external to the PWM control IC since the PWM control IC is normally not located near heat generating components. Thermal sensors need to be implemented in a manner that allows sensing of phase temperature. The trip point needs to be externally programmable by the system designer.



- The hysteresis VR_Hot or SVID Thermal Alert should be approximately 3% or 1 tick in the optional temperature zone register.
- The tolerance on VR_Hot should be +- 4% or approximately +-4 deg C, optimized in the target range of 90 to 120 deg C. Accuracy window can be larger at lower temperatures to accommodate non-linearity of NTC thermistor.
- Spread between SVID thermal Alert and VR_Hot should be approximately 3% or 3 deg C.
- Please reference Fig 6-1.

In addition to the VR_Hot# hardware signal and the SVID thermal alert in status1 (10h), there is an optional Temperature zone register that indicates how close the VR is operating to the VR_Hot trip point. When the VR temperature reaches bit 6 or SVID Thermal alert state, it asserts bit 1 in the Status 1 register and asserts the ALERT# line. This condition is called SVID Therm_Alert. When the VR cools down bit 1 toggles from 1 to 0, the Alert# line is re-asserted to indicate the condition has cleared. SVID Thermal Alert bit is not cleared with a GetReg(status1) command. The data in the temperature zone register should be updated asynchronously with the SVID bus, and update as the temperature changes. As long as there is a VR thermal alert condition, bit 1 in status 1 remains asserted (IE bit 1 is a sticky bit).

### Table 6-2. Thermal Zone and Detection Encoding (Optional)

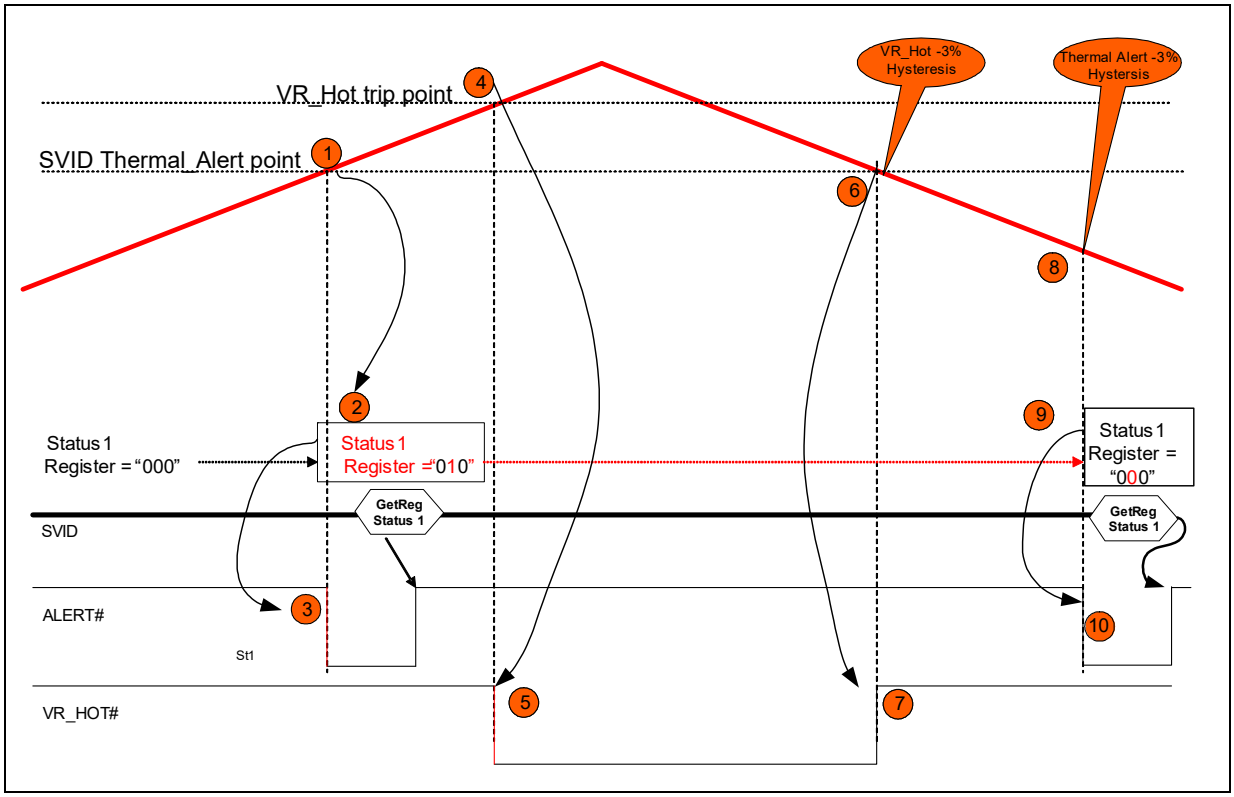
| Temp Max VR_Hot# | SVID Therm Alert | | | | | | |
|---|---|---|---|---|---|---|---|
| **b7** | **b6** | **b5** | **b4** | **b3** | **b2** | **b1** | **b0** |
| 100% | 97% | 94% | 91% | 88% | 85% | 82% | 75% |
| 100C | 97C | 94 | 91 | 88 | 85 | 82 | 75 |
| **Example Register contents for 95C** | | | | | | | |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

***Note:*** Comparator trip points and example shows temperatures scaled to 100C=100%=Temp Max setting

There can be multiple GetReg(status1) commands between when SVID Therm_Alert asserts and de-asserts since the thermal time constants are much longer than the dynamic VID transitions.

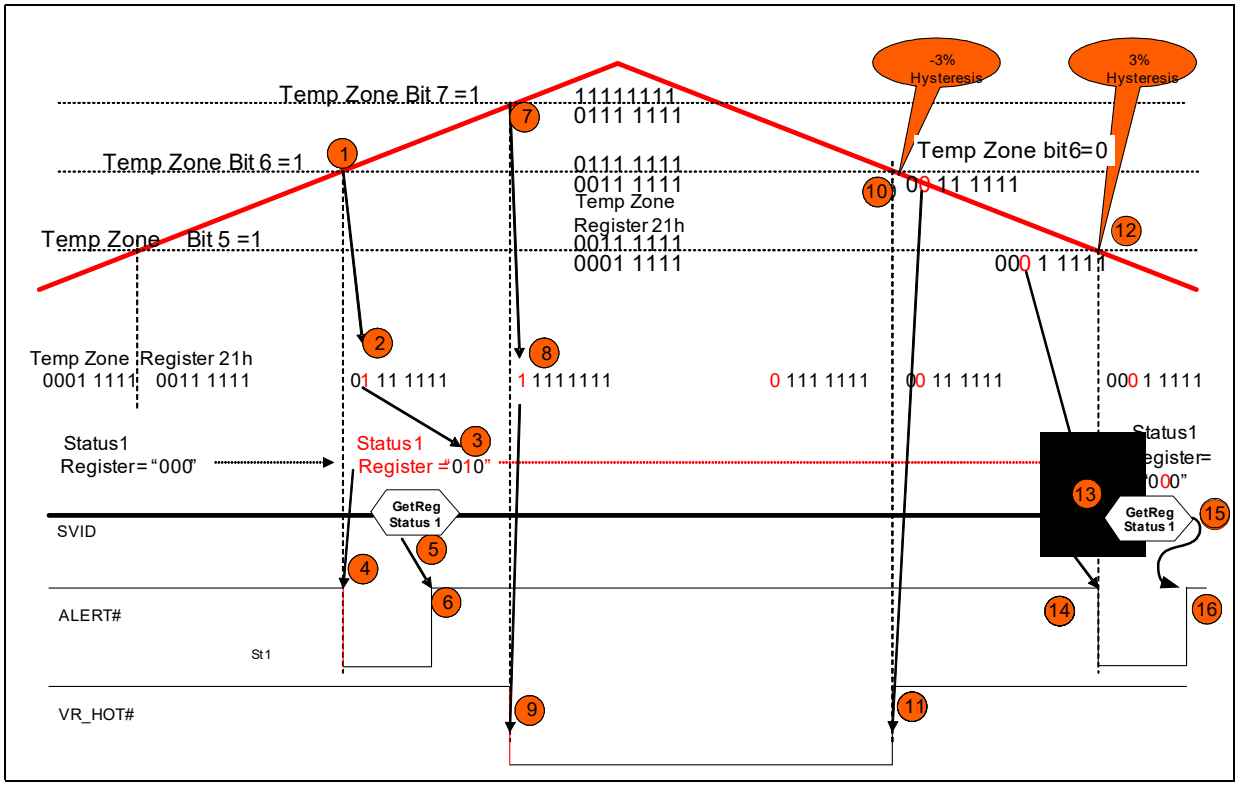
Optional features include digitizing of the temperature sensor and storing that data in the temperature register to be read back over the SVID or PMBUS interface.

**Figure 6-1. VR_Hot#, SVID Thermal Alert Illustration without Thermal Zone Register Support**




1. Temperature rises above Thermal Alert trip point
2. Status1 register bit 1 asserts issuing SVID thermal Alert
3. Alert# asserts indicating change in Status1
4. GetReg(status1) issued to clear the alert but not the status1 thermal alert status. Alert# is cleared. Temperature continues to rise above VR_hot trip point
5. VR_HOT# pin asserts low, CPU reacts enters thermal throttle low power state
6. After some period of time, VR cools down by -3% hysteresis below the VR_Hot trip point
7. VR_HOT# de-asserts
8. VR continues to cool down to -3% hysteresis on Thermal Alert Status1 register bit1 de-asserts
9. Alert# asserts indicating change in Status1
10. GetReg(status1) issued and Alert# is cleared.

**Figure 6-2. VR_Hot#, SVID Thermal Alert Illustration for PWM IC that Support Thermal Zone**




1. Temperature rises above Temp Zone bit 6 trip point
2. Register 12h bit6 asserts
3. Status1 register bit 1 asserts issuing SVID thermal Alert
4. Alert# asserts indicating change in Status1
5. GetReg(status1) issued
6. Alert# is de-asserted in response to GetReg(status1)
7. Temperature continues to rise above bit7 trip point (AKA VR_Hot)
8. Register 12h bit7 asserts
9. VR_HOT# pin asserts low
10. CPU reacts and VR cools down by -3% hysteresis, Bit7 de-asserts
11. VR_HOT# de-asserts
12. VR continues to cool down, Register 12h Bit5 de-asserts with – 3% hysteresis
13. Status1 register bit1 de-asserts
14. Alert# asserts indicating change in Status1
15. GetReg(status1) issued
16. Alert# is de-asserted in response to GetReg(status1)

## 6.6 Output Protection

These are features built into the DC-DC for protection of itself, the processor, and other system components. Intel has left this section vague since these are system level features and we support the VR vendors optimization of their PWM chips to the market segments they service. The main function of OCP or OVP is to prevent damage to the system board in case of component failure. Operating in an OVP condition does not guarantee there will be no damage to the microprocessor.

***Note:*** OVP and OCP are proposed in this document since they are not critical to Intel CPU functions. These are platform level requirements and VR control IC vendors should consult with their customers on how to support these functions.

### 6.6.1 Over-Voltage Protection (OVP)

The main function of OVP is to prevent smoke or fire in a platform from a failed VR circuit or component. An OVP circuit should monitor the output for an over-voltage condition. There are two methods to implement OVP functions:

IMVP9 mode OVP = ~400 mV max above VID

1. Fixed OVP, output voltage can never exceed 400 mV above the Vout_Max program level under any fault condition. Refer Section 3.10.1. This function allows the CPU designer to set the OVP level by changing the Vout_Max level as the CPU silicon technology changes.

2. Tracking OVP, output voltage can never exceed 400mV(max) above programmed VID target+ positive offset. For tracking OVP, OVP can be blanked during dynamic VID events to prevent false trigger. The blanking time should be commensurate with the Dynamic VID settling time.

With either implementation, the VR should not have a false OVP trip due to turn on into a pre-charged capacitor bank or a load release overshoot.

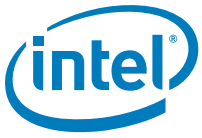
In the event of an OVP condition, the VR should turn off the top MOSFET driver, turn on the low-side MOSFETs, de-assert VR_Ready, and shut down until reset by toggling enable or PWM IC input Vcc (system power supply reset). It is desired that the OVP latch stay active below the standard UVLO for the PWM IC so that the low side MOSFETS clamp if the 12-V rail sags below the PWM control IC's UVLO point.

It is *optional* to support a VR Fault pin that asserts and notifies the platform of a VR fault condition.

### 6.6.2 Over-Current Protection (OCP)

The DC-DC should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the DC-DC. The OCP trip level should be programmable by the DC-DC designer, typically 130% of rated maximum or peak output current. If an OCP fault is detected, the VR should change its mode of operation (fold back, hiccup mode, regulate for X cycles then latch off, etc.) to protect itself against damage, smoke, etc.

OCP shall work on a per-phase basis and be correctly scaled for the remaining phase or phases during low power states such as PS1. OCP shall work with any Load Line or AVP setting including 0 mOhm LL or no LL support.



# 6.7 VR Tolerance

## 6.7.1 Load Line Definitions

The PWM chip should not preclude programming any load-line slope or AVP gain from 0 to 20mΩ. The individual processor or load specifications will set the load line and current level specification. Over current protection and 0 mΩ load lines are required to be independent, e.g., setting a 0mΩ LL will have no effect on OCP trip points.

Load-line settings are platform specific and will not be changed with an SVID command nor will the Master attempt to read the load line setting over the SVID bus.

## 6.7.2 Voltage Tolerance

The voltage tolerance is required over DC input operation conditions, temperature operating conditions, and lot-to-lot variation of PWM IC. The PWM design sets the steady-state or DC load-line accuracy based on DAC set point tolerance and load-line or AVP tolerance.

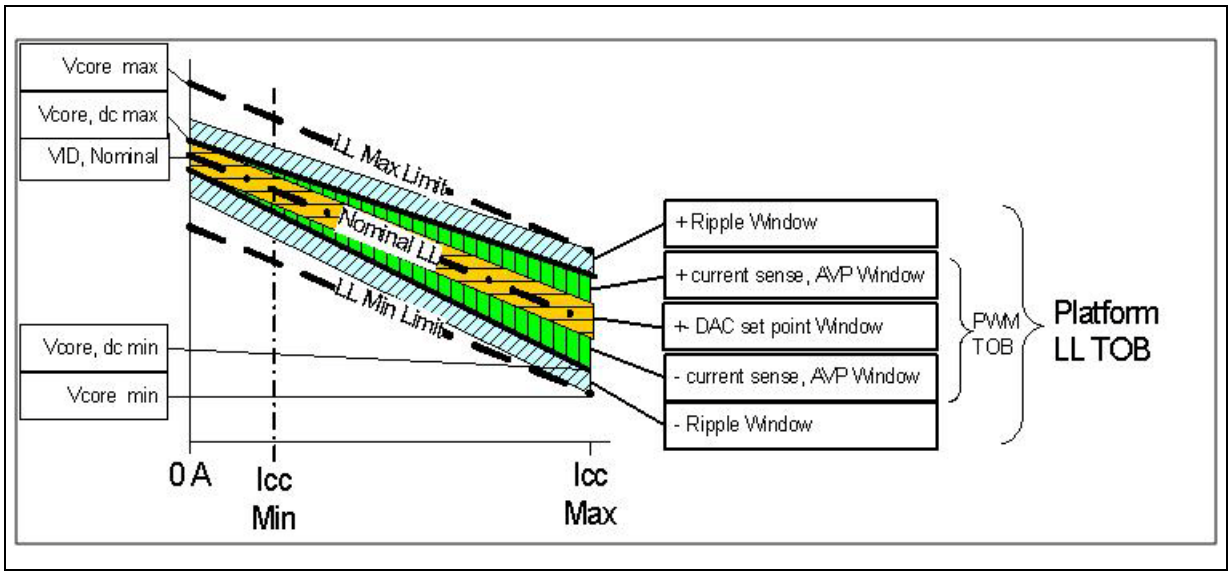
For the total platform loadline tolerance, ripple voltage is added in separately to the VR tolerance window based on platform and market segment requirements. The Electrical Design Specifications (EDS) & Platform Design Guidelines (PDG) will contain a detailed breakdown of the VR tolerance band per market segment and CPU type.

The overall requirement is for the VR to stay within the TOB window, the absolute values of set point, current sense, AVP, and ripple voltages are not important.

Platform Tolerance Budget (TOB) window includes:

- +/- Platform Ripple window
- +/- DAC set point window – Refer VID Table 4-1
- +/- Current sense, AVP window
- Total TOB should be root sum square of the DAC set point window and AVP window with the platform ripple added on top.
- When making tolerance band calculations the individual components that make up the tolerance should be specified as a percentage at the +- 3σ distribution points.
- VR tolerance bands will be documented in Electrical Design Specifications (EDS) and Platform Design Guidelines (PDG) per market segment.

**Figure 6-3. VR Tolerance Definitions (Neglecting Overshoot Relief)**




## 6.7.3 Load Line Thermal Compensation

Thermal compensation allows the microprocessor Vcc voltage regulator to respond to temperature drift in the VRD electrical parameters. It is required to ensure that regulators using inductor current sensing maintain a stable voltage over the full range of load current and system temperatures. Thermal compensation is required on all rails in a multiple output PWM controller.

If thermal compensation is not included, the output voltage of the regulator will droop as the resistance of the sense element increases with temperature. With the increased resistance, the regulator falsely detects an increase in load current and regulates to a lower voltage. Thermal compensation prevents this thermally induced voltage droop by adjusting the feedback path based on the temperature of the regulator. This is accomplished by placing a thermistor in the feedback network, tuned with a resistor network to negate the effects of the increased resistance of the sense element.

The thermal compensation circuit is to be validated by running the regulator at the Voltage Regulator Thermal Design Current (VRTDC) and minimum required air flow for 30 to 45 minutes. This ensures the board is thermally stable and system temperatures have reached the maximum steady-state condition. If the thermal compensation has been properly implemented, the output voltage will only drift 1-2 mV from its coolest temperature condition. If the thermal compensation has not been properly implemented, the voltage can droop in the tens of mV range

### 6.7.4 Input Voltage Range

Each segment will have varying input voltage support requirements.

**Table 6-3. Input Voltage by Segment**

| Segment | Min | TYP | Max | Note |
|---|---|---|---|---|
| Desktop | 4.5V | 12V | 14V | The platform may switch from 4.5V to Max V during runtime. The voltage output must remain within tolerance during this switching period. |
| AIO | 4.5V | | 19V | |
| Mobile | 5.6V | - | 19V | |

## 6.8 No Load Operation

The VR is required to operate at no load or Zero current load without errors or false trip of OVP, or de-asserting VR_Ready.

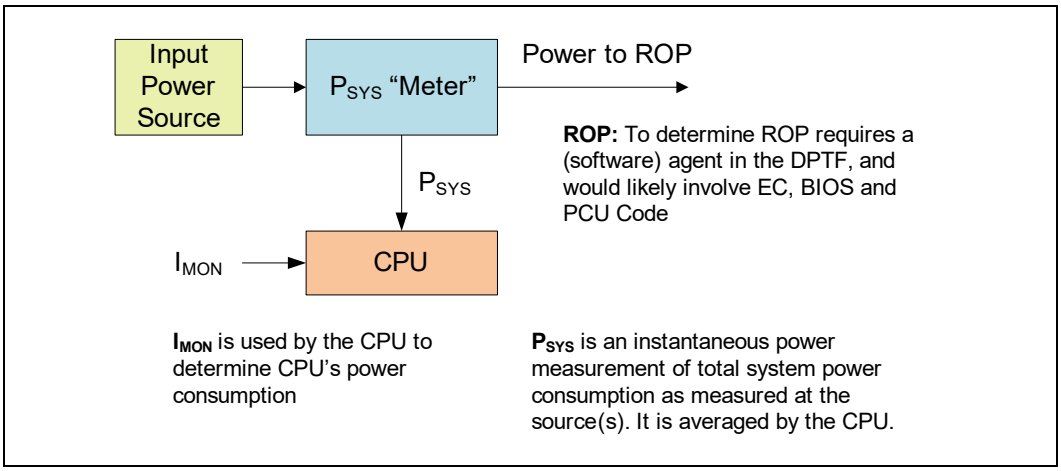
## 6.9 System Input Power Monitor, PSYS [Required Y,U,H and S]

The main functional block is shown in Figure 6-4.

The system input power monitor is the means to measure total platform system power. This information is either sent directly to the IMVP9 PWM as an analog signal proportional to the system power or directly to the CPU via the SVID bus.

PSYS could be implemented by one of two options: internal as part of the charger circuit, or as a stand-alone silicon sensor. Also, within each option are two sub-options: either generating an analog signal that emulates the total platform system power, or directly digitize the analog signal and provide to CPU via the SVID interface. All four options will be described in further detail below.

**Figure 6-4. PSYS Architecture Block Diagram**



### 6.9.1 Functional Block Diagrams

Option1 is the integrated Charger approach, incorporating the power sense function into the charger. Option2 is the Silicon Sensor solution, which requires a dedicated silicon power sensor at the entry of system power. The sub-options for each are differentiated by format, e.g. single-ended current mode analog signal or an SVID based digital representation.

**Figure 6-5. Option 1: PSYS-Integrated NVDC Charger to IMVP9**

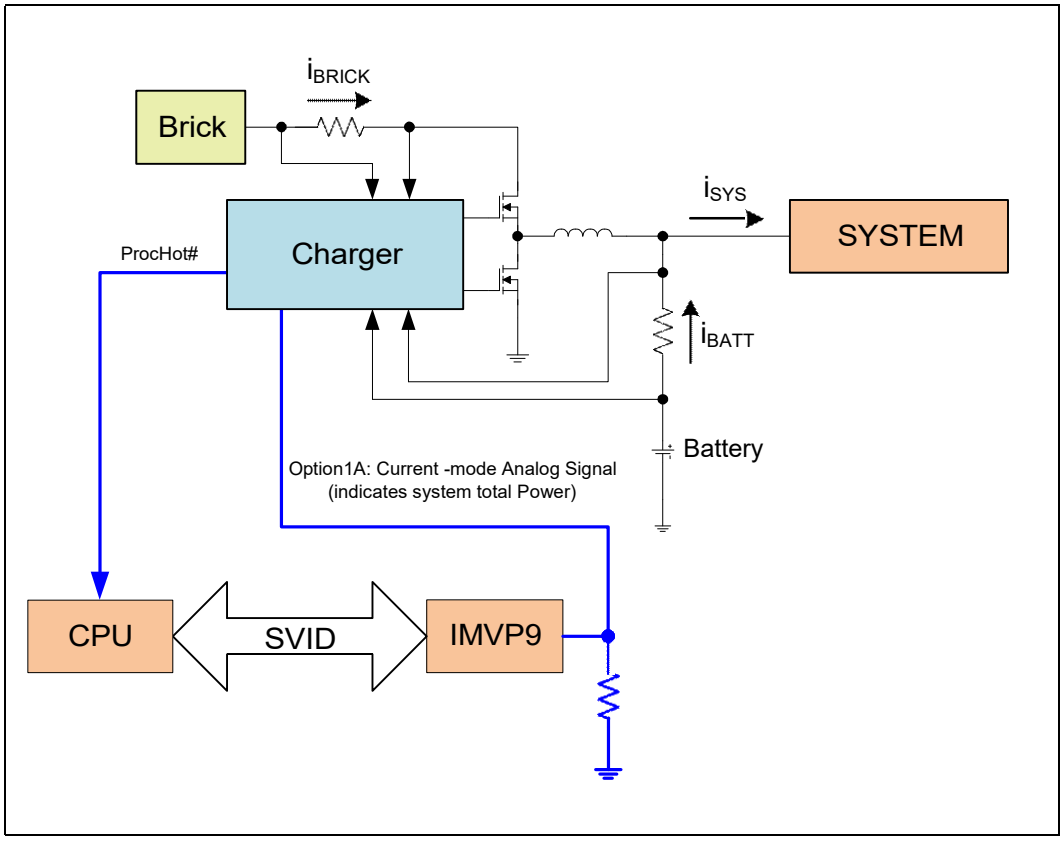
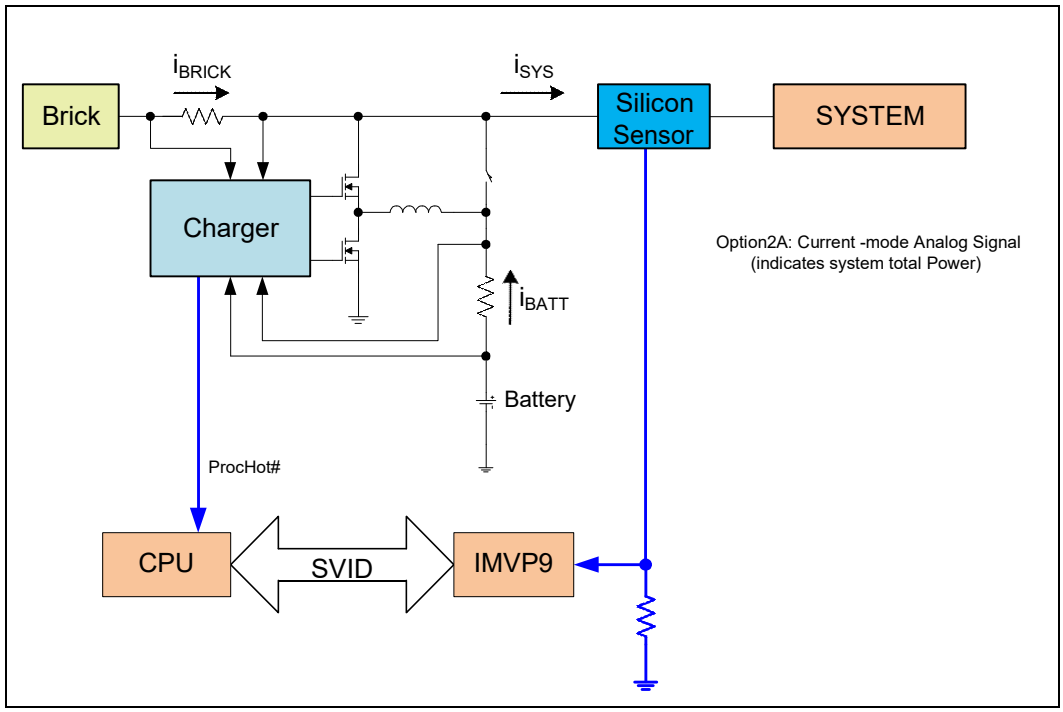


**Figure 6-6. Option 2: Silicon Sensor PSYS to IMVP9**




The preference is for option 1: integrating the PSYS function into the charger circuitry also accounts for the losses of the charger circuit that the stand-alone sensor approach doesn't. The charger sense circuit comprehends both the brick current and the battery current, while the independent, silicon sensor approach comprehends only the system power. The charger's inefficiency is not taken into account in the latter scenario.

Finally, the shunts required for monitoring the adapter (brick) and the battery currents are already a part of the system.

Refer Figure 6-5 for the integrated Charger approach and Figure 6-6 for the Silicon Sensor based approach. The former is thought the most cost-effective solution for the mobile client market segment. Finally, Figure 6-7 and Figure 6-8 visually describe the respective SVID-based approaches, below.

**Figure 6-7. SVID-based, PSYS-Integrated NVDC Charger to CPU Directly**

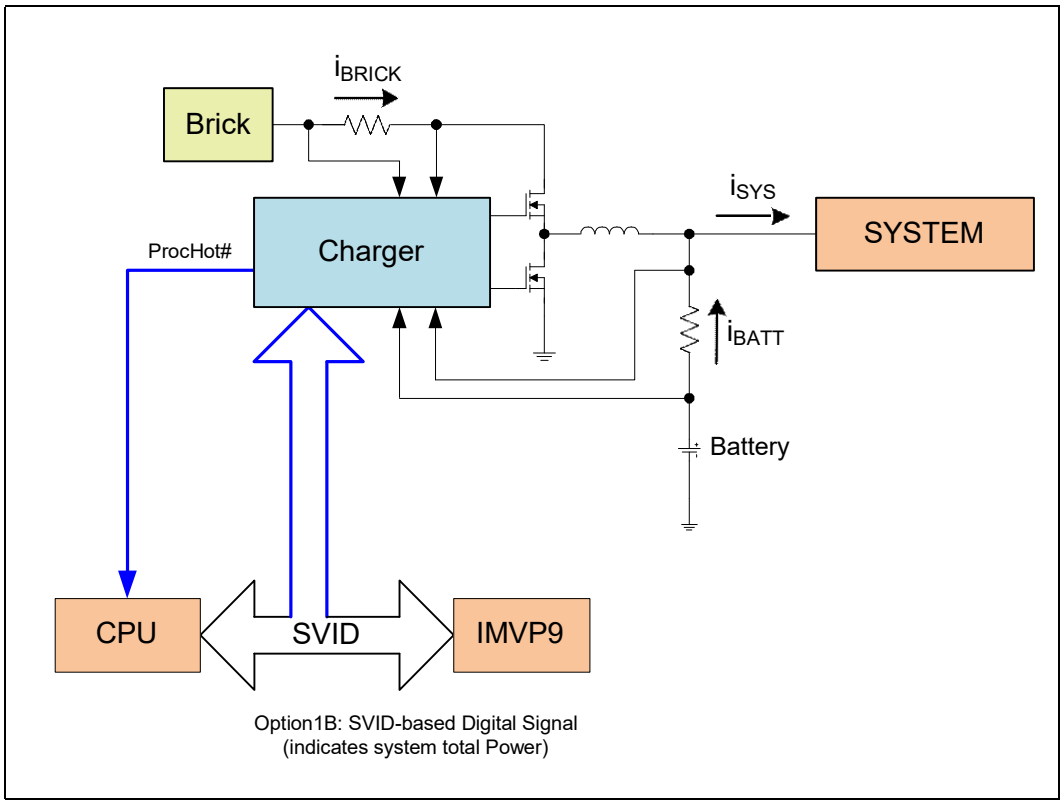
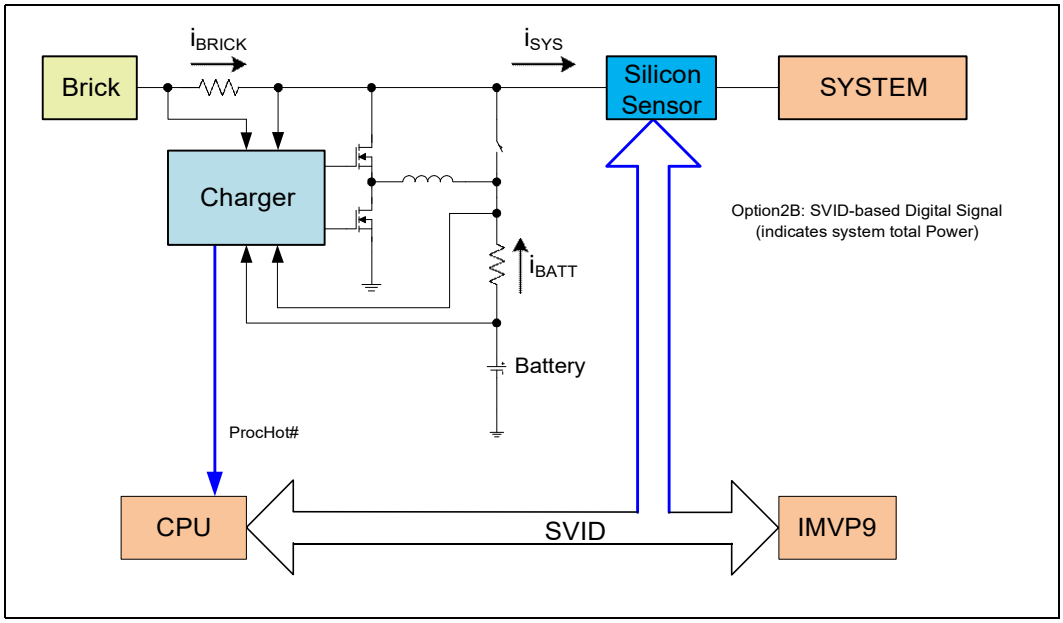


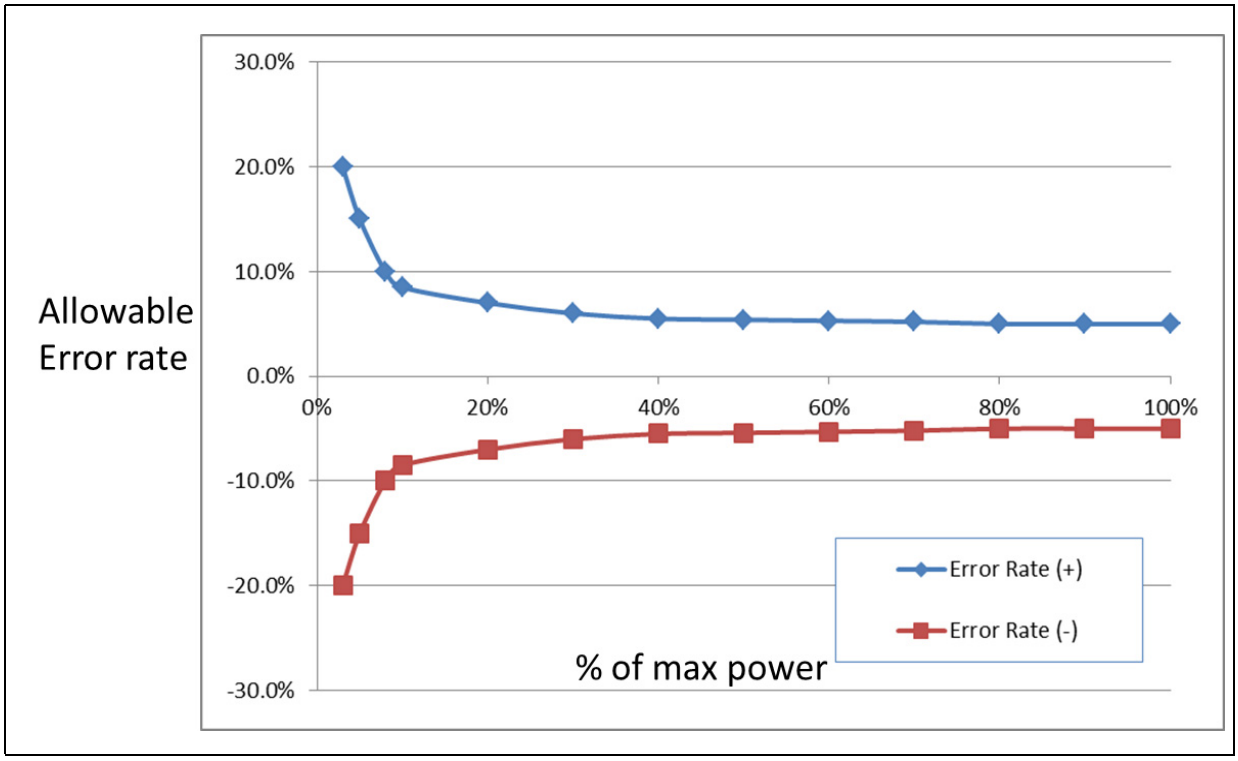

**Figure 6-8. SVID-based Silicon Sensor PSYS to CPU Directly**



### Table 6-4. Input Power Sense and Reporting Specifications

| | Desktop | Mobile | Notes |
|---|---|---|---|
| **Sense node** | Processor Input Power 10-400W range | Platform Input power | |
| **Input pin voltage tolerance** | 3.3V | | |
| **Averaging interval** | 1ms | | |
| **Register update interval** | 500µs | | |

### Figure 6-9. System Input Power Monitor Error Rates




### Table 6-5. System Input Power Monitor Accuracy (Sheet 1 of 2)

| % of Pmax | Error Rate | |
|---|---|---|
| | Pos. | Neg. |
| 100% | 5.0% | -5.0% |
| 90% | 5.0% | -5.0% |
| 80% | 5.0% | -5.0% |
| 70% | 5.2% | -5.2% |
| 60% | 5.3% | -5.3% |
| 50% | 5.4% | -5.4% |
| 40% | 5.5% | -5.5% |
| 30% | 6.0% | -6.0% |
| 20% | 7.0% | -7.0% |

**Table 6-5. System Input Power Monitor Accuracy (Sheet 2 of 2)**

| % of Pmax | Error Rate | |
|---|---|---|
| | Pos. | Neg. |
| 10% | 8.5% | -8.5% |
| 8% | 10.0% | -10.0% |
| 5% | 15.0% | -15.0% |
| 3% | 20.0% | -20.0% |

## 6.9.2 Fast Psys and Psys Event Counters

The following is a high level over view. The reader should refer to section 7.8 of the SVID Protocol Specification v1.8 for detailed information on this feature.

In addition to the standard Psys monitoring called out in Section 6.9, the controller shall support additional facilities for monitoring input power level events and for fast assertion of VR_HOT#. The Psys input pin is to be monitored by three independent peak detecting comparators prior to the ADC low-pass (anti-alias) filter. Two of these comparators are used to trigger independent counters, WARNING1 and WARNING2, that count with 2us resolution when triggered. Each counter will increment whenever its respective threshold is met or exceeded. The third is the Psys Critical Detector comparator, which is used for fast assertion of VR_HOT# whenever the Psys input meets or exceeds its threshold.

Figure 6-10 shows the general architecture for this Fast Psys and Counters architecture. Each comparator has a dedicated threshold register; these threshold registers are located at 0x4Ah, 0X4Bh, and 0x4Ch for the Psys Critical Detector, WARNING2 counter, and WARNING1 counter respectively. Note that the controller may optionally support 16 bit thresholds as called out by the SVID protocol specification for higher resolution threshold settings.

The counter count values are located at 0x4D and 0x4E for WARNING2 and WARNING1 respectively. The Psys Critical detector shall have independent settings for assertion and de-assertion debounce settings; these registers are located at 0x4Fh and 0x49h respectively.

Monitoring system input power, via the Psys input, and detecting when it goes above specific threshold levels is one technique for making sure that system input power supply capability is not exceeded. An alternate method is to use the Psys input to monitor a voltage level provided by the power source for droop, making sure it does not fall below preset levels. This method is applicable to systems that do not have a power telemetry signal available. To enable voltage-level monitoring, the controller shall support the ability to invert the triggers for all the registers above such that the WARNING1, WARNING2, and Psys Critical Detector trigger when the Psys input, fed by a Vsys signal, is at or below the respective thresholds. The polarity of these thresholds is set by the VsysMode bit (0x34[2]) as follows:

- VsysMode bit (0x34[2]) = 0 (default) →Power monitoring
- *VsysMode* bit (0x34[2]) = 1 →Voltage droop monitoring

## Figure 6-10. Fast Psys and Psys Event Counters

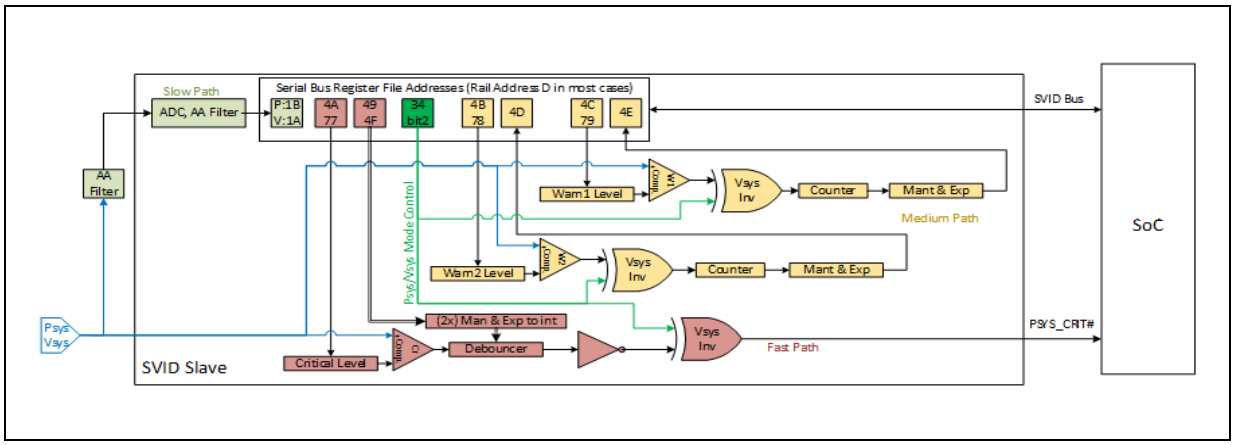


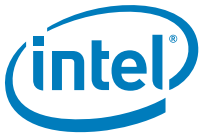

Table below summarizes the registers for the Fast Psys and Psys Event Counter support. For details on this mechanism and its register definitions refer the SVID Protocol Specification v1.8.

## Table 6-6. Fast Psys and Psys Event Counter Registers (Sheet 1 of 3)

| Register | Name | Type | Default | Description |
|---|---|---|---|---|
| | | | | |
| 4A (Required) | PsysCrLvl_H | R/W | 00h | Psys Critical Trigger Threshold most significant byte.<br>This threshold is a linear fractional value of the Psys input full scale voltage.<br>**8 bit resolution:** This register sets the trigger threshold for the Psys critical detector comparator.<br>**9 bit to 16 bit resolution controllers:** This register serves as the Most Significant Byte of the critical comparator trigger threshold. Register 0x77 serves as the least significant byte of the critical comparator threshold.<br>When the Psys input meets or exceeds this threshold (higher or lower as set by 0x34[2] VsysMode) PSYS_CRIT# is asserted. Controllers that do not implement a dedicated pin for PSYS_CRIT# must pull VR_HOT# low in place of PSYS_CRIT# |
| 77 (Optional) | PsysCrLvl_L | R/W | 00h | Psys Critical Trigger Threshold least significant byte.<br>**8 bit resolution:** This register is reserved.<br>**9 bit to 16 bit resolution controllers:** This register serves as the least significant Byte of the critical comparator threshold. This threshold is a linear fractional value of the Psys input full-scale voltage. Bits are left justified (e.g. a 10 bit resolution threshold would put the lower 2 bits of the threshold value (bits 1:0) in bits [7:6] of this register). Unused lower-order bits return 0 on a read.<br>When the Psys input meets or exceeds this threshold (higher or lower as set by 0x34[2] VsysMode) PSYS_CRIT# is asserted. Controllers that do not implement a dedicated pin for PSYS_CRIT# must pull VR_HOT# low in place of PSYS_CRIT#<br>Register 0x4A serves as the most significant byte of the critical comparator threshold. |

## Table 6-6. Fast Psys and Psys Event Counter Registers (Sheet 2 of 3)

| Register | Name | Type | Default | Description |
|---|---|---|---|---|
| 4B<br>(Required) | PsysW2Lvl_H | R/W | 00h | Psys WARNING2 counter trigger threshold most significant byte<br>**8 bit resolution:** This register sets the trigger threshold for the WARNING2 event counter comparator.<br>**9 bit to 16 bit resolution controllers:** This register serves as the Most Significant Byte of the WARNING2 counter threshold. Register 0x78 serves as the least significant byte of the critical comparator threshold.<br>When the Psys input meets or exceeds this threshold (higher or lower as set by 0x34[2] VsysMode) the WARING2 counter increments every 2us for the duration that the Psys input is at or in excess of this threshold. |
| 78<br>(Optional) | PsysW2Lvl_L | R/W | 00h | Psys WARNING2 counter trigger threshold,<br>Least Significant Byte<br>**8 bit resolution:** This register is reserved.<br>**9 bit to 16 bit resolution controllers:** This register serves as the Least Significant Byte of the WARNING2 counter threshold. Register 0x4B serves as the least significant byte of the critical comparator threshold.<br>When the Psys input meets or exceeds this threshold (higher or lower as set by 0x34[2] VsysMode) the WARNING2 counter increments every 2us for the duration that the Psys input is at or in excess of this threshold.<br>Register 0x4B serves as the most significant byte of the WARNING2 counter trigger threshold. |
| 4C<br>(Required) | PsysW1Lvl_H | R/W | 00h | Psys WARNING1 counter trigger threshold.<br>Most Significant Byte<br>**8 bit resolution:** This register sets the trigger threshold for the WARNING1 event-counter comparator.<br>**9 bit to 16 bit resolution controllers:** This register serves as the Most Significant Byte of the WARNING1 counter threshold. Register 0x79 serves as the least significant byte of the critical comparator threshold.<br>When the Psys input meets or exceeds this threshold (higher or lower as set by 0x34[2] VsysMode) the WARNING1 counter increments every 2us for the duration that the Psys input is at or in excess of this threshold. |
| 79<br>(Optional) | PsysW1Lvl_L | R/W | 00h | Psys WARNING1 counter trigger threshold.<br>Least Significant Byte<br>**8 bit resolution:** This register is reserved.<br>**9 bit to 16 bit resolution controllers:** This register serves as the Least Significant Byte of the WARNING1 counter threshold. Register 0x4B serves as the least significant byte of the critical comparator threshold.<br>When the Psys input meets or exceeds this threshold (higher or lower as set by 0x34[2] VsysMode) the WARNING1 counter increments every 2us for the duration that the Psys input is at or in excess of this threshold.<br>Register 0x4C serves as the most significant byte of the WARNING1 counter trigger threshold. |



## Table 6-6. Fast Psys and Psys Event Counter Registers (Sheet 3 of 3)

| Register | Name | Type | Default | Description |
|---|---|---|---|---|
| 4D<br>(Required) | PsysW2Count | R | 00h | Psys WARNING2 counter results register<br>This register contains the WARNGING2 count data. The value in this register is encoded in mantissa exponent format as follows:<br>[7:4] Mantissa<br>[3:0] Exponent<br>$T = 2\mu s \times Mantissa[4bits] \times 2^{Exponent[4bits]}$<br>When triggered this register updates in 2us increments. This register is only cleared when it is read or when its associated threshold value (PsysW2Lvl) is changed.<br>When this counters reaches 0xFF it stops and does not roll over; it and holds its value until it is cleared.<br>The value in the register is persistent through all power states PS0 – PS4. |
| 4E<br>(Required) | PsysW1Count | R | 00h | Psys WARNING1 counter results register<br>This register contains the WARNGING1 count data. The value in this register is encoded in mantissa exponent format as follows:<br>[7:4] Mantissa<br>[3:0] Exponent<br>$T = 2\mu s \times Mantissa[4bits] \times 2^{Exponent[4bits]}$<br>When triggered this register updates in 2us increments. This register is only cleared when it is read or when its associated threshold value (PsysW1Lvl) is changed.<br>When this counters reaches 0xFF it stops and does not roll over; it and holds its value until it is cleared.<br>The value in the register is persistent through all power states PS0 – PS4. |
| 4F<br>(Required) | PsysCritAssert | R/W | 00h | PSYS_CRIT# assertion debounce time.<br>This register sets the Psys Critical detector assertion debounce time.<br>PSYS_CRIT# assertion debounce time. This register sets the Psys Critical detector assertion de-bounce time. The format of this register is mantissa exponent format.<br>[7:4] Assertion debounce time mantissa<br>[3:0] Assertion debounce time exponent<br>Where the assertion debounce time is:<br>$T_{debounce} = 2\mu s \times Mantissa[4bits] \times 2^{Exponent[4bits]}$<br>When this field is set to 0x00h the total time from threshold exceeded to assertion of VR_HOT# is ≤ 2us max. |
| 49<br>(Required) | PsysCritDeassert | R/W | 00h | PSYS_CRIT# de-assertion debounce time. This register sets the Psys Critical detector de-assertion de-bounce time. The format of this register is mantissa exponent format.<br>[7:4] De-assertion debounce time mantissa<br>[3:0] De-assertion debounce time exponent<br>Where the de-assertion debounce time is:<br>$T_{debounce} = 2\mu s \times Mantissa[4bits] \times 2^{Exponent[4bits]}$<br>When this field is set to 0x00h the total time from threshold exceeded to assertion of VR_HOT# is ≤ 2us max. |

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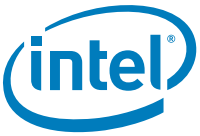

# 7 Design Collateral

## 7.1 Demo, Test Board Requirement (VRTB)

A test board with a socket will be required for evaluation of the PWM controllers submitted to Intel for evaluation.

Each segment will specify the VRTB requirements.

## 7.2 Computer Models

Intel evaluation requires submission of both state averaged and switching computer compatible models of the PWM controller.

IBIS or Spice models of the SVID buffers are required for signal integrity study and simulation on the SVID bus. For more information on IBIS models refer http://www.eigroup.org/ibis/ for more information. In particular, download the "**Ibis Cookbook**" and under "Free Tools", click the "IBIS Golden Parser" to confirm your model formats.

## 7.3 VR Tolerance Band Calculator

As an aid to VR design and component selection, Intel requires the PWM vendor to provide a Load Line tolerance band calculator that allows the OEM/ODM to calculate what tolerance band a particular design will have based on his component selection. This model should contain the parameters within the PWM IC that effect the load line tolerance. The format for the load line calculator should be an MS-Excel* spreadsheet or MathCAD* or web-based design file.

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# 8 PMBUS/SMBUS – Optional

PMBUS/SMBUS can be used to implement VID DAC offset, set an absolute voltage, read back telemetry data, program configuration registers, etc.

It is required by some OEMs on Server Platforms for data collection from the VR, and is commonly used on Client Platforms for over-clocking.

This chapter explains the design considerations for PMBUS/SMBUS support.

## 8.1 PMBUS/SMBUS Data Format and Command Support Recommendation

PWM ICs that supports PMBUS should comply with the PMBus™ Application Profile for Vcore regulators for Compute Market Segment. Refer WWW.PMBUS.org for the latest application profile. PMBUS compliant PWM IC's can also implement the "Vendor Specific Commands" as defined in the PMBUS specifications for additional functionality over the minimum command set in Table 8-1.

When different data formats in the PMBUS protocol are supported, the PWM IC vendor should document which formats are used by their particular IC.

If the PWM IC does not support PMBUS Protocol, but SMBUS or other $I^2C$* protocol, the command protocol must be called out in the VR vendor's data sheets and/or application notes.

The Intel PCH for Client platforms only supports standard SMBUS transaction format. Any transactions involve the extended registers/commands on PMBUS spec can NOT be generated by Intel PCH on Client Platform. Controller with SMBUS support for telemetry and voltage margining must utilize standard SMBUS data format. Some controllers have additional commands such as loadline adjustment, compensation adjustment, boot voltage selection, other special modes, etc. These transactions must also be accessed by standard SMBUS commands.

The table below shows a set of recommended PMBUS commands. Additional vendor specific PMBUS/SMBUS commands are allowed. PWM IC vendors should document the support command set in their data sheets.

**Table 8-1. Minimum Recommended PMBUS Command Set (Sheet 1 of 2)**

| Command code | Command | Description |
|---|---|---|
| 01h | OPERATION | |
| 20h | VOUT_MODE | The VOUT_MODE command, used for commanding and reading output voltage, consists of a three-bit and a five-bit parameter representing the exponent used in output voltage Read/Writes. |
| 21h | VOUT_COMMAND | The VOUT_COMMAND is used to set the output voltage, in volts. |
| 22h | VOUT_TRIM | The VOUT_TRIM command is used to apply a fixed offset voltage to the output voltage command value. |

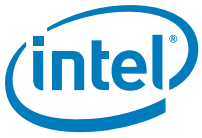

**Table 8-1. Minimum Recommended PMBUS Command Set (Sheet 2 of 2)**

| Command code | Command | Description |
|---|---|---|
| 23h | VOUT_CAL_OFFSET | VOUT_CAL_OFFSET command is used ot applying a fixed offset voltage to the output voltage command value. |
| 24h | VOUT_MAX | |
| 25h | VOUT_MARGIN_HIGH | The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed, in volts, |
| 26h | VOUT_MARGIN_LOW | The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed, in volts, when the command is set to “Margin Low”. |
| 8Bh | READ_VOUT | The READ_VOUT command returns the actual measured output voltage in the same format as set by the VOUT_MODE command In a LL enabled VR; this should be an averaged value. |
| 8Ch | READ_IOUT | The READ_IOUT command returns the output current in amps |
| 8Dh | READ_TEMPERATURE_1 | The READ_TEMPERATURE1 command returns the temperature, in ?C of the external sense element |
| 96h | READ_POUT | Read back Output Power in Watts. |

## 8.2 PMBUS/SMBUS Device Addressing

Multiple IMVP9 controllers may be used on a common PMBUS/SMBUS. VR controllers must support programmable addressing for the respective communications bus that is independent of the SVID bus address.

It is recommended that PMBUS/SMBUS addresses be pin-strapped or resistor programmed so simple manufacturing defect analysis (MDA) or flying probes can verify the address is programmed to the right location when there are multiple VR controllers on the same board.

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# 9 Over Clocking for Extreme Edition Client Platform – Optional

SVID bus is the primary two-way communication channel between the CPU and the IMVP9 controllers. VR controllers are required to communicate VR capability to the CPU through SVID bus, and to handle the power management SVID transitions appropriately during over clocking. This may involve SVID command handling and extended SVID bus frequency support.

Improper SVID register settings may limit the platform ability to over clock. Fail to comply with SVID communication protocol may result in system hang or shut down. The following discusses the design considerations for IMVP9 in over clocking environments.

## 9.1 SVID Bus Frequency and Signal Integrity

### 9.1.1 SVID Clock Frequency

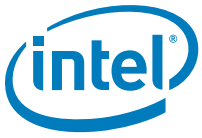
IMVP9 generation CPUs could use BCLK to generate the VR SVID Clock. For instance, SVID CLK = 1/4 * BCLK. During over clocking, if BCLK is increased, SVID CLK will consequently increase. Therefore, PWM controllers that are dedicated to the performance segment should extend their SVID VCLK supported frequency to more than the standard maximum supported frequency of 26.25 MHz. The higher the SVID CLK the VR supports, the higher the BCLK the system can maintain power management function. A recommended target is 43 MHz.

### 9.1.2 SVID Bus Signal Integrity

The typical Power Delivery Design Guide and Validation Plans assume SVID clock frequency is less than 26.25 MHz. As mentioned above, when BCLK is increased, the SVID clock frequency will consequently increase. The SVID bus signal integrity may need to be re-validated up to the maximum supported frequency.

### 9.1.3 SVID VIL and VIH Thresholds

Since SVID bus is an open drain bus, VCCIO/VTT is used to pull up the SVID Bus. In over clocking mode, the VCCIO/VTT voltage can be increased to a higher voltage. SVID Bus Low signal level (VIL) and High signal level (VIH) will be raised as VCCIO/VTT increases. VR controllers should take this increased threshold into consideration when defining VIL and VIH levels.



## 9.2 Voltage Margining

Starting from 2015 (IMVP9) platforms, the CPU will allow voltage margining control using SVID bus. BIOS will have access to CPU voltage control registers (MSRs) that offset the operating VID or set a fixed voltage of the VR. The CPU will adjust the VID setting according to the register settings and issue SetVID commands to the VR. SVID Offset command will not be used in this case.

Using external devices such as digital potentiometers or integrated PMBUS/SMBUS control to margin the voltage is optional for rails with CPU voltage control registers.

### 9.2.1 Extended VID Table

In order for CPU voltage margining to work through SVID bus with the voltage control registers, the PWM IC is recommended to support up to 3.05V in order to provide additional power to the processor.

### 9.2.2 Offset Voltage Margining

Offset voltage margining is commonly used in most over clocking cases. It can provide power saving when processing power is not needed. In this mode, the CPU operating VID is offset by a desired (positive or negative) voltage. When the CPU changes VID, the VR output will be at the level of the sum of the CPU VID and this desired Offset. One exception is when VR receives SetVID to 0V command; the output voltage should be 0 V.

If external devices such as digital potentiometers or integrated PMBUS/SMBUS control are used to create the offset, the VR controller is expected to respond to CPU SVID commands as normal— even if the output voltage may be offset.

SVID clock frequency may be higher due to increased BCLK frequency. The VR must support higher SVID clock frequency as mentioned in previous section in order to keep SVID communication active.

### 9.2.3 Fixed Voltage Margining

Fixed voltage margining is used in extreme over clocking where fixed voltage can provide additional stability. In this mode, a fixed voltage is assigned, and the VR output voltage will be fixed at this voltage in regardless of CPU VID changed.

This mode can only be achieved in two options:

1. Use the CPU built-in voltage control registers mentioned above.
2. Use a special VR controller that provides cheat mode to properly handle the CPU SVID commands while maintaining the output voltage at a fixed VID. For instance, when the CPU issues a SetVID command, the VR will ACK the command, maintain the fixed output voltage and assert ALERT# immediately, while the VR output voltage stay at the fixed VID.

If Option (2) is used, SVID clock frequency may be higher due to increased BCLK frequency. The VR must support higher SVID clock frequency as mentioned in previous section in order to keep the SVID communication active.

# 9.3 Other Performance Tuning and Settings

## 9.3.1 $V_{OUTMAX}$ Register (30h)

In performance segment, $V_{OUTMAX}$ register (30h) is recommended to be user programmable. It can be used to protect the VR components, such as output capacitors, in case the voltage ratings of the components are lower than the maximum VR supported voltage. The CPU respects the Voltage value programmed in the $V_{OUTMAX}$ Register, and does not issue any SetVID command above this defined value.

## 9.3.2 Iccmax Register (21h)

VR's for performance segment are usually designed with higher Iccmax current. VR controller must provide high enough current settings for Iccmax register (21h); otherwise, the CPU may limit the performance up to the VR Iccmax current recorded in this register.

## 9.3.3 $I_{OUT}$ Register (15h)

CPU uses the digital $I_{OUT}$ register (15h) to obtain output current telemetry data from the VR for power management. VR controller may build in current monitor scaling capability to under-report the output current. This will allow for more current margin before the CPU reaches the typical Iccmax threshold.

***Warning:*** Doing so will result in CPU drawing current in excess of the Iccmax value recorded in the Iccmax register and documented in the CPU datasheet. Appropriate over current protection must be applied.

## 9.3.4 Dynamic VID Ramp and Slew Rate Registers (24h and 25h)

The faster the VR can ramp the voltage in dynamic VID event, the sooner the CPU can transition to various frequencies. This will shorten the latency and increase the system performance. If faster slew rate can be achieved, the VR can shorten the T_ALERT timing, and report faster slew rate in the Slew Rate Registers (24h and 25h). The CPU will adjust the latency based on the slew rate register settings. Note that increasing slew rate will increase the inrush current to charge the capacitor and may result in OCP tripping, inductor saturation, etc. It may also cause the VR switch-node spike to increase.

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