PDG:

Sequencing Interface Signals List and Power Rails

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10.3 IMVP9 Voltage and Current Requirements
10.4 AC Adapter Considerations
10.5 Battery Charging System
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10.8 System Peak Power Management (Pmax)
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10.12.3 Sequencing Interface Signals List and Power Rails

Table 227. Tiger Lake Platform Sequencing Signals List

Name	Source	Destination	Description
RTCRST#	Platform	PCH	When asserted, this signal resets the register bits in the RTC well.
SRTCRST#	Platform	PCH	This signal resets the manageability register bits in the RTC well when the RTC battery is removed
DSW_PWROK	Platform	PCH	Indication to the PCH that VCCDSW_3p3V rail is stable. This signal must be asserted no earlier than 10ms after the DSW power wells are valid. *Note:* In TGL generation platforms DSW_PWROK and RSMRST# are always separate power ok signals. Refer DSW/PRIM Rail Architecture in DSx and Non-DSx Designs on page 432
RSMRST#	Platform	PCH	This signal is used for resetting the Primary power plane logic. This signal must be asserted for at least 10 ms after the Primary power wells are valid. When de-asserted, this signal is an indication that the power wells are stable. *Note:* there are special requirements around RSMRST# assertion when NOT entering DSx power states. Refer RSMRST#/DSW_PWROK Special Requirements on page 461 for details.
SUSWARN#	PCH	Platform	This function is only applicable to platforms supporting Deep Sleep

SLP_SUS#:

SLP_SUS#	PCH	Platform	For platforms supporting Deep Sx state, a low on this signal indicates that PCH is in Deep Sx state and that EC/platform logic does not need to keep the Primary Rails ON. If high means EC must keep Primary rails ON. Unlike previous generation platforms, in TGL SLP_SUS# is used in both DSx and Non-DSx platforms. Refer DSW/PRIM Rail Architecture in DSx and Non-DSx Designs on page 432 for details. *Note:* In eSPI mode this signal is a hard wire only and not a virtual wire.

If SLP_SUS#=0 →

Power Up:

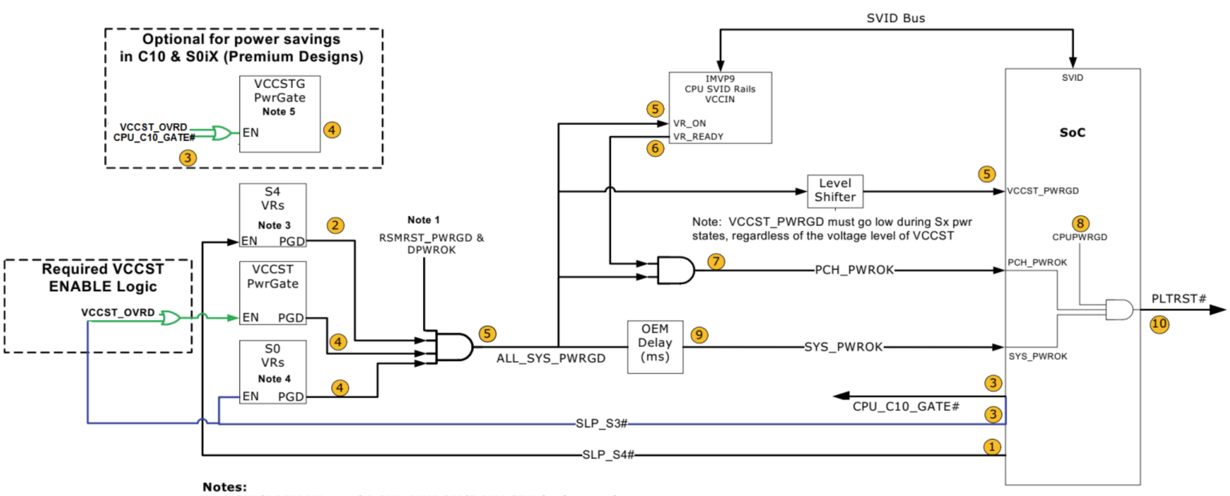
SL. No		Rail Name		Net Name in SCH [Fill up by customer own design]	
1		VCCRTC	1	+VCCPRTC_3P3	2.0-3.3V +5% supplies for PCH RTC Well. This power is not expected to be shut off in any of the sleep states unless the RTC battery is removed or completely drained.
2		RTCRST#		RTC_RST_N	When asserted, this signal resets the register bits in the RTC well.
3		SRTCRST#		SRTC_RST_N	This signal resets the manageability register bits in the RTC well when the RTC battery is removed
4	2	VCCDSW_3P3		**+VCCPDSW_3P3**	3.3-V supply for Deep Sx wells. If Deep Sx is not supported on the platform, tie to **VCCPRIM_3P3.**
5		DSW_PWROK		DSW_PWROK	**Deep Sx Well PWROK**: Power OK Indication for the **+VCCPDSW_3P3** voltage rail. Note: This signal is in the RTC well. This signal cannot tie with RSMRST#. Connected to FPGA
6		SLP_SUS#		PM_SLP_SUS_N	Or platforms supporting Deep Sx state, a low on this signal **(SLP_SUS# =0)** indicates that PCH is in Deep Sx state and that EC/platform logic does not need to keep the Primary Rails ON. (+VCCPRIM_3P3 && VCCPRIM_1P8) should go down. If **SLP_SUS# =0 → +VCCPRIM_3P3 = 0** && **VCCPRIM_1P8 = 0** **If high (SLP_SUS# =1) means EC must keep Primary rails ON.** Unlike previous generation platforms, in TGL SLP_SUS# is used in both DSx and Non-DSx platforms. Refer DSW/PRIM Rail Architecture in DSx and Non-DSx Designs on page 432 for details. Note: In eSPI mode this signal is a hard wire only and not a virtual wire. **SLP_SUS# =1 indicates that** (+VCCPRIM_3P3 && VCCPRIM_1P8) should be ENABLED. In TL-SBC: 226/270 In TL-SBC: 234/270 **SLP_SUS# =1** Enables +V3.3A and +5VA In TL-SBC: 226/270 **SLP_SUS# =1** Enables +V1.8A In TensorI20 FPGA Code: SLP_SUS# wasn't used to enable V33A_ENn, but VCC was used instead (which is high when +3V3DSW is high)
7		V5.0A	3	+V5A	
8		VCCPRIM_3P3		+VCCPRIM_3P3	PCH I/O and Misc rails 3.3V (Primary Well)

9		VCCPRIM_1P8		+VCCPRIM_1P8	PCH I/O and Misc rails 1.8V (Primary Well)
10		VCCIN_AUX		+VCCIN_AUX	PCH FIVR input power supply
~~11~~	4	~~VNN_BYPASS~~	-	~~+VCC_VNNEXT_1P05V~~	~~**Optional** BYPASS rail for PCH Prime Core Well (760mV in S0ix and 1.05V in Sx states) or reduced power consumption in low power states~~
~~12~~		~~V1.05A_BYPASS~~		~~+VCC_V1P05EXT_1P05V~~	~~**Optional** BYPASS rail for PCH Primary Well (1.05V) for reduced power consumption in low power states~~
13		RSMRST#		PM_RSMRST_N	
14		PWRBTN#		PM_PWRBTN_N	
15		SLP_S5#	5	PM_SLP_S5_N	This signal is for power plane control. When asserted (low), it will shutoff power to all non-critical systems in **S5 (Soft Off)** states. Note: In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH.Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.
16	6	SLP_S4#		PM_SLP_S4_N	S4 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S4 (Suspend to Disk) and lower (S5). If SLP_S4# = 0 , Note: In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.
17		**DDR_VPP (DDR4)**		**+V1.8U_2.5U_MEM {VPP}**	
18		SLP_S3#		PM_SLP_S3_N (GOES **HIGH** ON POWER UP)	SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in the **S4, or S5 state.**
19		SLP_S0#		PM_SLP_S0_N	S0 Sleep Control: When PCH is idle and processor is in C10 state, this pin will assert to indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations. If PM_SLP_S0_N = 0,
20	8	CPU_C10_GATE#	7	CPU_C10_GATE_N	Power gating control to turn off VCCSTG in C10 and lower. Note: In eSPI mode this signal is a **hard wire** only and not a virtual wire. External Power Gate: Control for VCCIO, VCCSTG and VCCPLL_OC during C10. When asserted, VCCIO, VCCSTG and VCCPLL_OC can be 0 V, however the power good indicators for these rails must remain asserted.
21		VCCST		+VCCST_CPU	Sustain voltage for processor in Standby modes
22		**DDR_VDD2 (DDR4)**		**+VDD2_CPU**	
23		**DDR_VDDQ (DDR4)**		**+VDD2_MEM (p.229/270)**	
24		VCCSTG	9	+VCCSTG_CPU	
25		ALL_SYS_PWRGD		ALL_SYS_PWRGD	
26	10	VCCST_PWRGD		VCCST_PWRGD	VCCST_PWRGD is a signal on the Tiger Lake processor that indicates both the VCCST power supply and VDDQ power

					supply are within voltage tolerance specifications. TL-PCH: VccST Power Good : When asserted, an indicator to the processor this rail is now supplied by the integrated FIVR in the PCH. During S5 to S0 and DSx to S0 transitions, the platform will need to generate the **VCCST_PWRGD**, **PCH_PWROK** and **SYS_PWROK** signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up.
27		VTT		+V_VDD2_VTT **{VTT}**	
28		PCH_PWROK (from FPGA to Processor)	11	PM_PCH_PWROK	
29		VCCIN		+VCCIN	Processor FIVR input power supply
30		PROCPWRGD		CPUPWRGD	
31	12	VCCIO		+VCCIO_OUT	
32		SYS_PWROK		SYS_PWROK	
33		PLTRST#		PLT_RST_N	

TGL-PDG

Premium PWROK (Power OK) Generation Flow Diagram

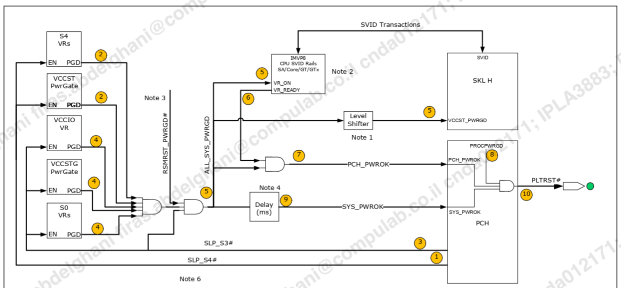


Notes:
1. **DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown.**
2. **NA**
3. **S4 VRs are controlled by SLP_S4# and are on in S3 and higher.**
4. **S0 VRs are controlled by SLP_S3# and are on in S0, C10, and S0iX.**
5. **Turns off in C10 and lower.**

CFL-PDG:

45.2 Sequencing Interface Signals List and Power Rails

Figure 45-1. CFL Flow Diagram for SYS_PWROK/PCH_PWROK Generation



Notes:
1. Enable inputs may be qualified by other signals and factors not shown.
2. Optional configurations. Different configurations may have impact boot latencies differently.
3. This delay is not explicitly required. For systems supporting traditional PCIe add in cards that require up to 100ms delay from pwr stable to PLTRST# deassertion, the PCH can guarantee a 99ms delay by enabling TPCH33 timing thru soft straps. If more or less time is required, then a specific timing delay circuit may be required
4. Voltage Monitor circuit to ensure PSU pwr rails are mostly up and stable before the VR is enabled
5. Circuit is used to monitor PSU for unexpected power down scenarios via falling edge of PSU PWROK output. To improve boot latency, the PSU PWROK rising edge is not used as a qualifier to gate PLTRST# deassertion via SYS_PWROK assertion. PSU power rail stability is inferred on the platform thru other means, such as the VM block shown in the diagram
6. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

Many variations exist on how the various pwrgood signals can be generated on a DT platform to balance system robustness with platform costs constraints. This is just one example of possible logic connections. Components and connections in blue are alternative configurations. Components and connection in black show a baseline configuration.

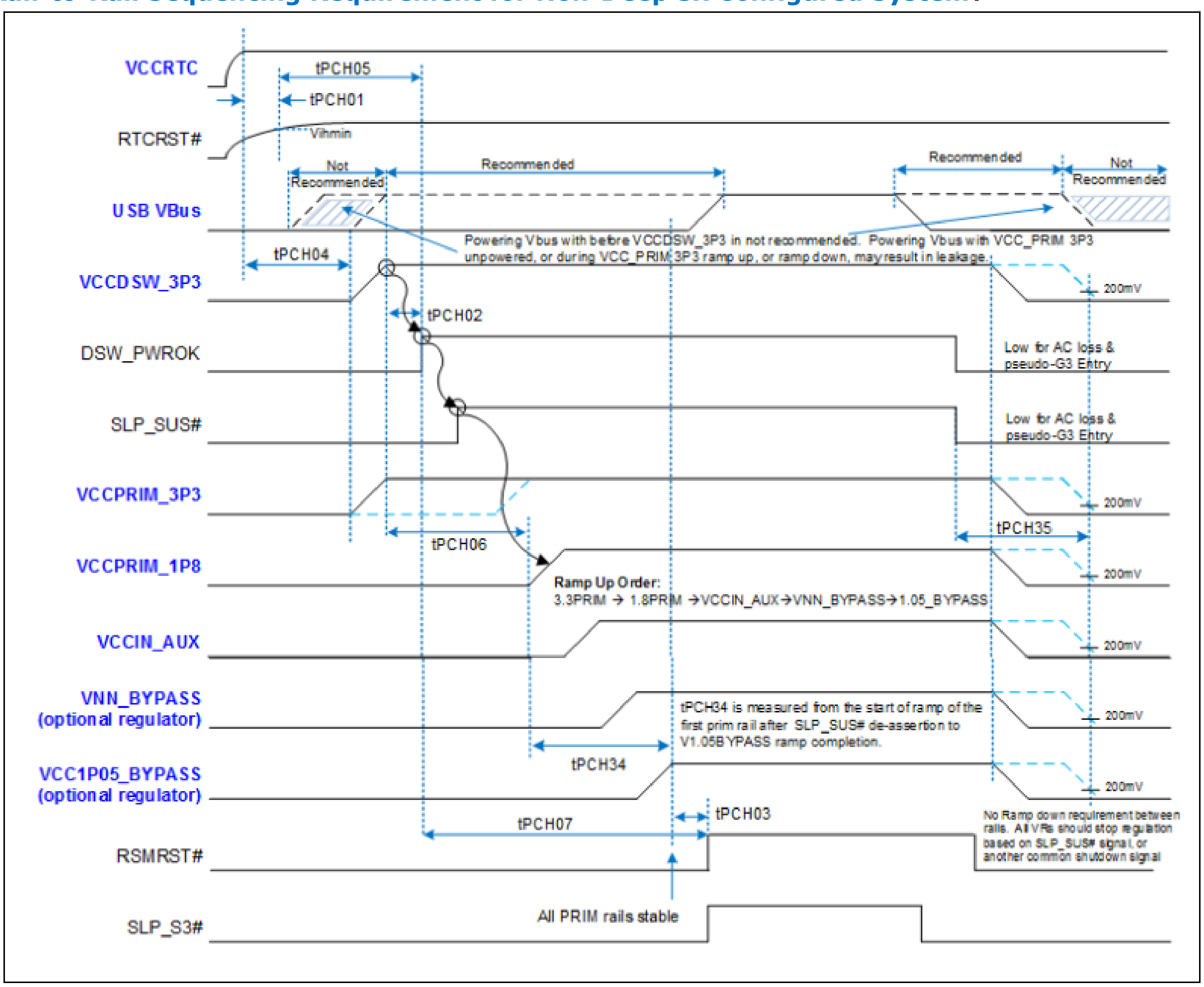
Figure 45-2. CFL Flow Diagram for RSMRST_PWRGD# Generation (Sheet 1 of 2)

10.12.4 Power States

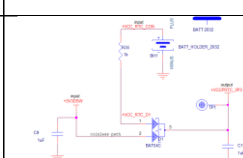
Table 229. System with M3 State Supported

Rails	SKUs	S0/M0[3]	C10[2]	S0ix/M-off[4]	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3[1]
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1P05	All	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P05EXT_1P05	All	ON	ON	ON	ON	ON	OFF	No Power
continued...								
V3.3M[5]	All	ON	ON	OFF	ON[10]	OFF	OFF	No Power
V1.8M[5]	All	ON	ON	OFF	ON[10]	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	OFF[6]	OFF[6]	OFF	No Power
VCCSTG	All	ON	OFF [2]	OFF	OFF	OFF	OFF	No Power
VCC1P8A[15]	H	ON	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON[11]	OFF	OFF	OFF	No Power
VCCIN_AUX[13]	All	ON	ON	ON[11]	OFF[14]	OFF[14]	OFF	No Power

Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System:



Power UP (TL-PDG p.449)

Label	Signal Name	Min	Max	Unit	Description	Controlled by	Chosen in FPGA
tPCH01	VCCRTC [+VCCPRTC_3P3] RTCRST# [RTC_RST_N] SRTCRST# [SRTC_RST_N]	9		ms	VccRTC = 2.0V to the point in time where voltage on the RTC resets equals 0.65 times the voltage present on the VccRTC rail during ramp. This measurement should be made from VccRTC = 2.0V to the first of RTCRST# or SRTCRST# reaching 0.65 * VccRTC	PLT	done
tPCH02	From **VCCDSW_3P3** to **DSW_PWROK**	10	2000	ms	VccDSW stable (@95% of full value) to DSW_PWROK high.	PLT	35 ms (done in dsw_pwrok_block)
tPCH03	VNN_BYPASS [+VCC_VNNEXT_1P05V] V1.05A_BYPASS [+VCC_V1P05EXT_1P05V] RSMRST# [PM_RSMRST_N]	10	2000	ms	VccPrimary stable (@95% of full value) to RSMRST# high	PLT	NA
tPCH04	VCCRTC [+VCCPRTC_3P3] VCCDSW_3P3 [+VCCPDSW_3P3]	9		ms	VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with **coined RTC battery**	PCH	
	Note: how did we take care of this delay in CFL-SBC?	30			VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with **coinless RTC**. Please refer to IBP#549657 for Design considerations technical advisory document without RTC battery. Earlier this timing was referred as tPCH48.(in CLH)		In Tensor I22: In the coinless case when **3V3DSW** is up +**VCCPRTC_3P3** is up.

tPCH05	RTCRST# [RTC_RST_N] DSW_PWROK	1		us	RTCRST# high (voltage above ViH_min) to DSW_PWROK high (when voltage crosses ViL_max such that internally it might be resolved as a logic '1')	PLT	
tPCH06	VCCDSW_3P3 [+VCCPDSW_3P3] VCCPRIM_1P8 [+VCCPRIM_1P8]	200		us	VccDSW 3.3 stable (@95% of full value) to VccPrimary 1.8V starting to ramp (for DSx or nonDSx configurations)	PLT	
tPCH07	DSW_PWROK RSMRST# [PM_RSMRST_N]	0		ms	DSW_PWROK high to RSMRST# high	PLT	
tPCH08	SLP_S3# [PM_SLP_S3_N] PCH_PWROK [PM_PCH_PWROK]	1 32		ms	SLP_S3# de-assertion to PCH_PWROK assertion	PLT	
tPCH32	DSW_PWROK SLP_SUS# [PM_SLP_SUS_N]	95		ms	DSW_PWROK assertion to SLP_SUS# de-assertion	PCH	
tCPU00	VCCST [+VCCST_CPU] VCCSTG [+VCCSTG_CPU] VCCST_PWRGD [VCCST_PWRGD]	2		ms	VCCST, VCCSTG ramped and stable to VccST_PWRGD assertion	PLT	
tCPU01	DDR_VDDQ [+VDD2_MEM] VCCST_PWRGD [VCCST_PWRGD]	1		ms	VDDQ ramped and stable to VccST_PWRGD assertion	PLT	

tPCH34	VCCPRIM_3P3 [+VCCPRIM_3P3] V1.05A_BYPASS [+VCC_V1P05EXT_1P05V]		50	ms	Time from start of ramp of the first prim rail after SLP_SUS# deassertion to completion of primary and bypass rail ramp	PLT	
	VCCPRIM_1P8 [+VCCPRIM_1P8] V1.05A_BYPASS [+VCC_V1P05EXT_1P05V]						

POWER DOWN:

SL. No		Rail Name		Net Name in SCH [Fill up by customer own design]	
1		PLTRST#	1	PLT_RST_N	
2		PROCPWRGD		CPUPWRGD	
3	2	SLP_S3#		PM_SLP_S3_N	USBAB_VBUS=High
4		ALL_SYS_PWRGD		ALL_SYS_PWRGD	
5		VCCST_PWRGD		VCCST_PWRGD VCCST_PWRGD must accurately reflect the state of VCCST and must not glitch when **VCCST**, **VCCSTG** or **VDDQ** power is applied. Additionally, VCCST_PWRGD must track to the state of PCH_PWROK on the platform. When PCH_PWROK de-asserts during S0 --> Sx transitions, then VCCST_PWRGD must also de-assert.	VccST Power Good : When asserted, an indicator to the processor this rail is now supplied by the integrated FIVR in the PCH.
6		PCH_PWROK	3	PM_PCH_PWROK	
7		SYS_PWROK		SYS_PWROK	
8		VCCIN		+VCCIN	
9	4	VTT		+V_VDD2_VTT	
10		VCCSTG		+VCCSTG_CPU	
11		SLP_S4#		PM_SLP_S4_N	In Tensor I22: If SLP_S4#=0 -> USBAB_VBUS=0
12		**DDR_VDDQ (DDR4)**	5	**+VDD2_MEM**	
13		VCCST		+VCCST_CPU	
14		SLP_S5#		PM_SLP_S5_N	
15	6	**DDR_VPP (DDR4)**		**+V1.8U_2.5U_MEM**	
16		SLP_SUS#		PM_SLP_SUS_N	
17		DSW_PWROK	7	DSW_PWROK	
18		RSMRST#		PM_RSMRST_N	
19		SLP_S0#		PM_SLP_S0_N	S0 Sleep Control. When PCH is idle and processor is in C10 state, this Pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.
20	8	CPU_C10_GATE#		CPU_C10_GATE_N	

21		VCCDSW_3P3		+VCCPDSW_3P3	
22		V5.0A		+V5A	
23		VCCPRIM_3P3	9	+VCCPRIM_3P3	
24		VCCPRIM_1P8		+VCCPRIM_1P8	
25		VCC1.05_OUT_PCH		+VCC1P05_OUT_PCH	
26	10	VCCIN_AUX		+VCCIN_AUX	
27		VNN_BYPASS		+VCC_VNNEXT_1P05V	
28		V1.05A_BYPASS		+VCC_V1P05EXT_1P05V	
29		PWRBTN#	11	PM_PWRBTN_N	
30		VCCRTC		+VCCPRTC_3P3	
31		RTCRST#		RTC_RST_N	
32		SRTCRST#		SRTC_RST_N	

SLP_A#:

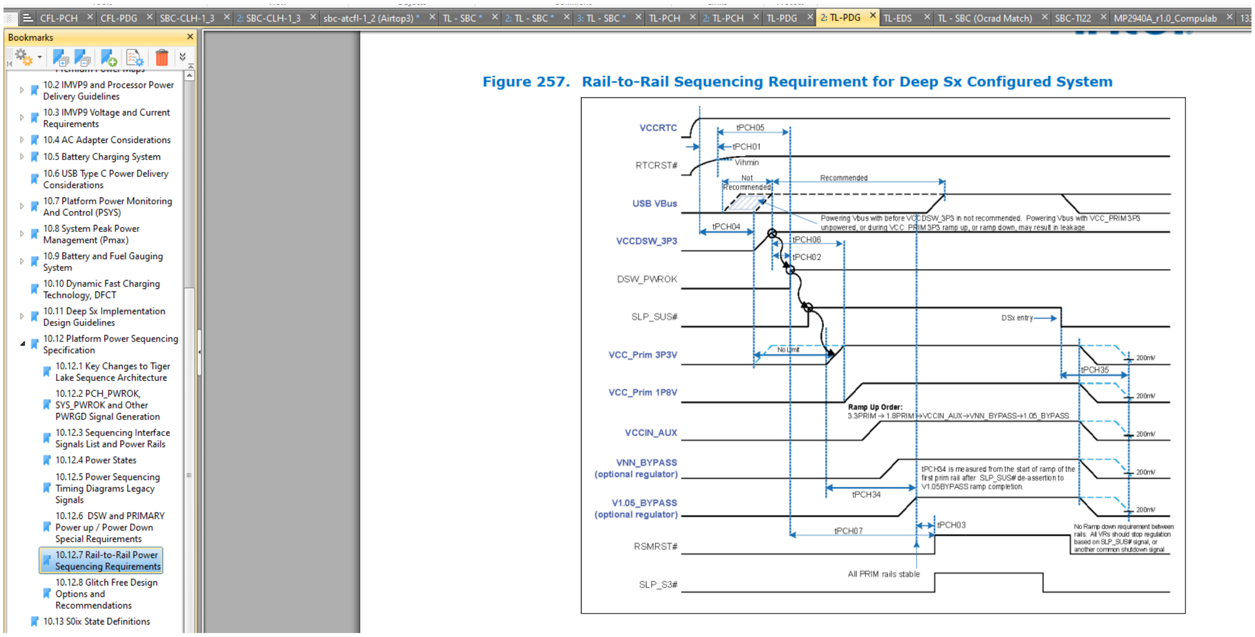
SLP_A# output signal can be used to cut power to the Intel® Converged Security and Management Engine and SPI flash on a platform that supports the M3 state (for example, certain power policies in Intel® AMT).

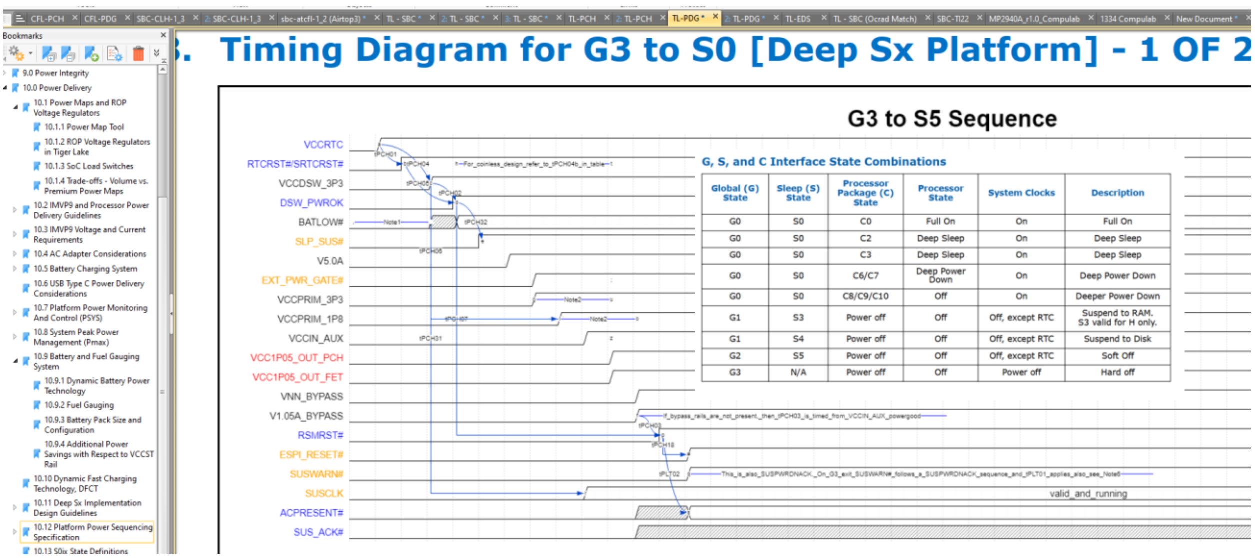
GPD6 / **SLP_A#**		**SLP_A#**: Signal asserted when the Intel CSME platform goes to M-Off or M3-PG. Depending on the platform, this pin may be used to control power to various devices that are part of the Intel CSME sub-system in the platform. If you are not using SLP_A for any functional purposes on your platform, or can tolerate lack of minimum assertion time, program the "SLP_A minimum assertion width" value to the minimum. SLP_A# functionality can be utilized on the platform via either the physical pin or via the SLP_A# virtual wire over eSPI.

Power Down:

Label	Signal Name	Min	Max	Unit	Description	Controlled by
tPCH24	PLTRST# [PLTRST_N] PROCPWRGD [CPUPWRGD]	30		us	PLTRST# assertion to PROCPWRGD de-assertion	PCH
tPCH27	SLP_S4# [PM_SLP_S4_N] SLP_S5# [PM_SLP_S5_N]	30		us	SLP_S4# assertion to SLP_S5# assertion	PCH
tPCH28	SLP_S3# [PM_SLP_S3_N] SLP_S4# [PM_SLP_S4_N]	30		us	SLP_S3# assertion to SLP_S4# assertion	PCH

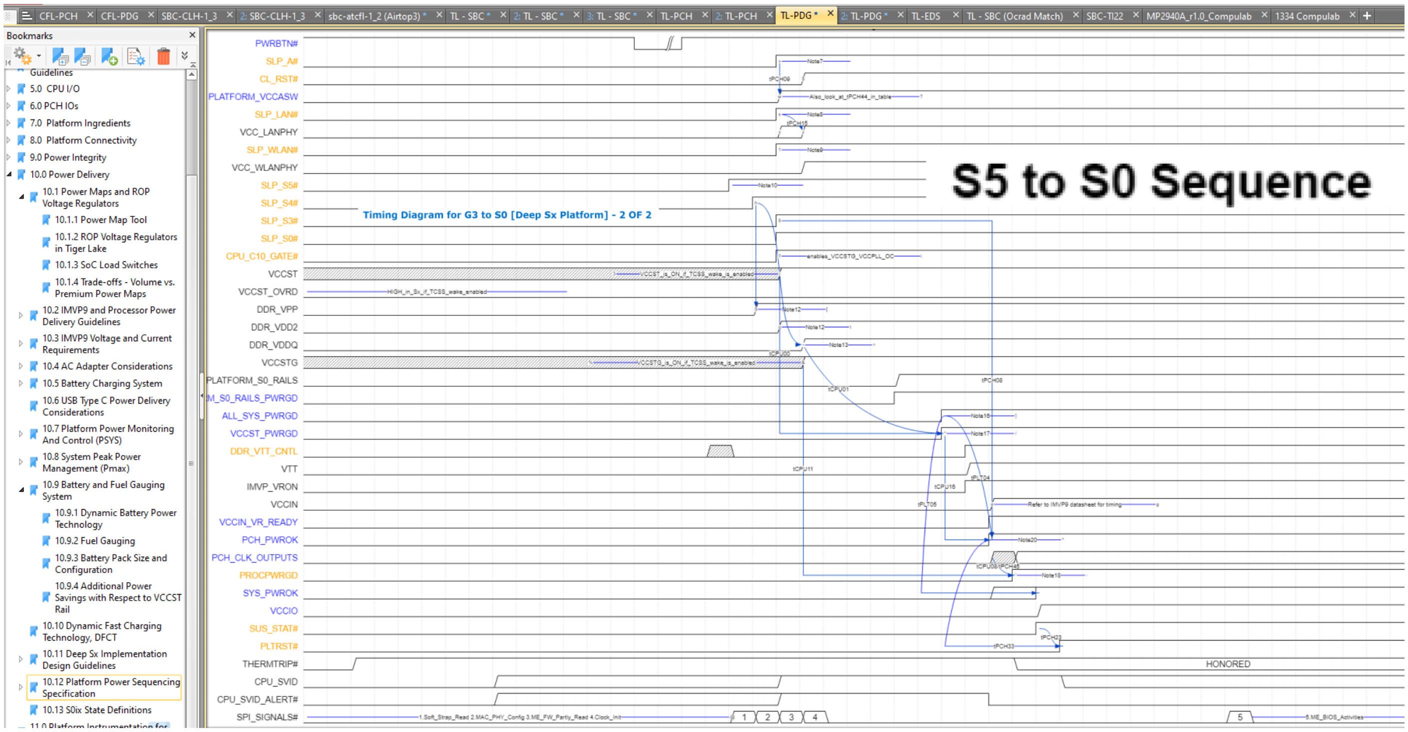
tCPU22	VCCST_PWRGD [VCCST_PWRGD] DDR_VDDQ [+VDD2_MEM]	1		us	VCCST_PWRGD deassertion to either VDDQ, VCCST, VCCSTG below specification for normal S0 to Sx transitions. Recommend VCCST_PWRGD goes low with SLP_S3#	PLT
	VCCST_PWRGD [VCCST_PWRGD] VCCST [+VCCST_CPU]					
	VCCST_PWRGD [VCCST_PWRGD] VCCSTG [+VCCSTG_CPU]					
tPCH29	SLP_S3# [PM_SLP_S3_N] PCH_PWROK [PM_PCH_PWROK]	0		ms	SLP_S3# assertion to PCH_PWROK deassertion	PCH





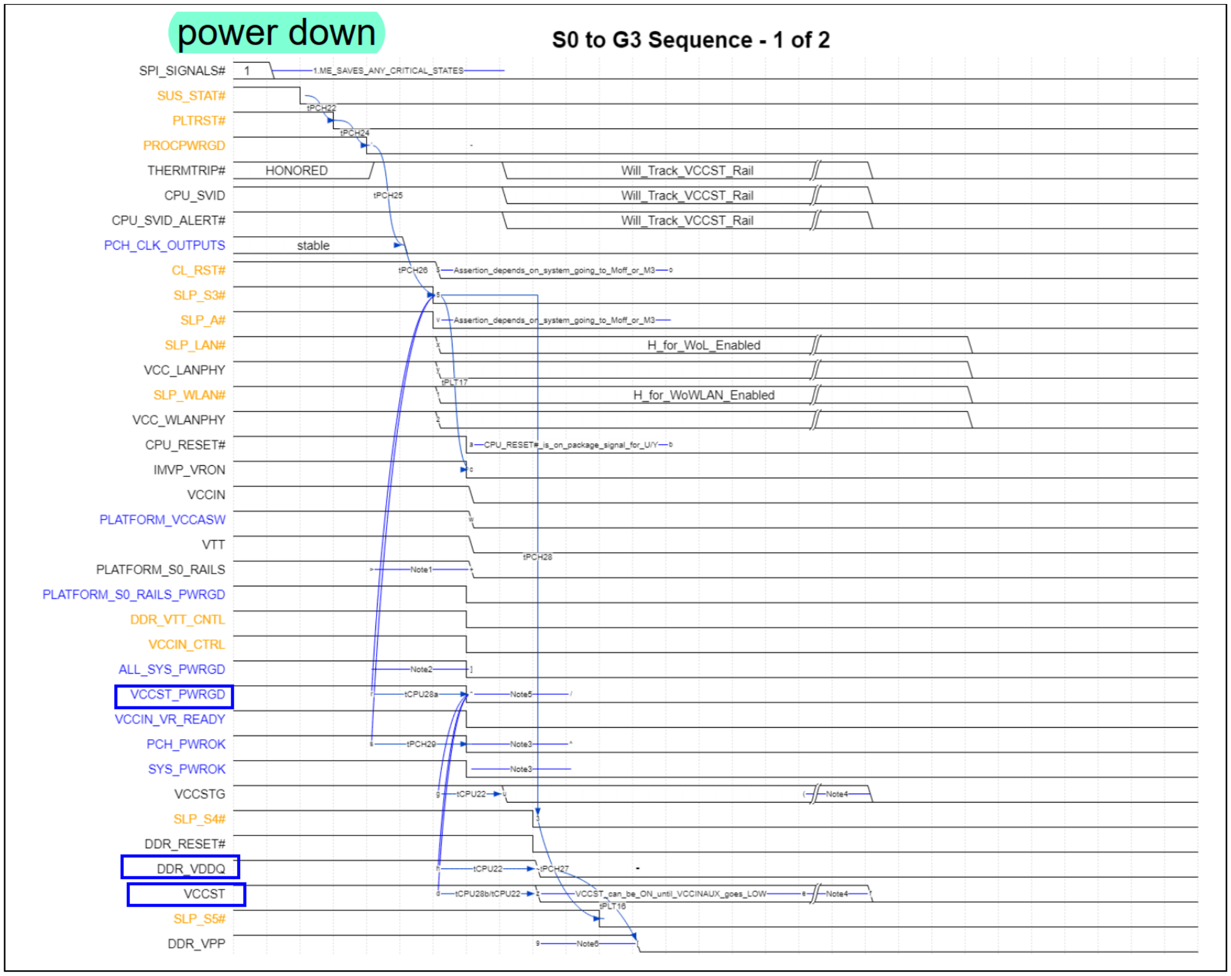
Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C2	Deep Sleep	On	Deep Sleep
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6/C7	Deep Power Down	On	Deep Power Down
G0	S0	C8/C9/C10	Off	On	Deeper Power Down
G1	S3	Power off	Off	Off, except RTC	Suspend to RAM. S3 valid for H only.
G1	S4	Power off	Off	Off, except RTC	Suspend to Disk
G2	S5	Power off	Off	Off, except RTC	Soft Off
G3	N/A	Power off	Off	Power off	Hard off

Power Up:

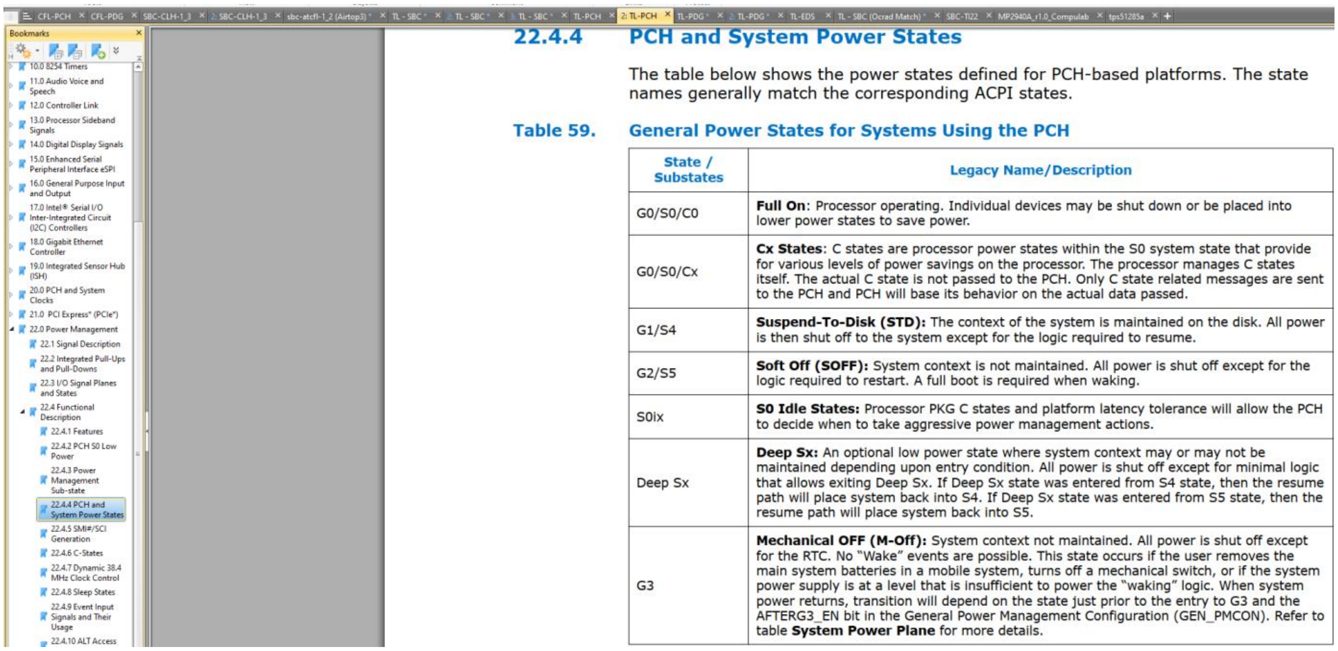


S5 to S0 Sequence
Timing Diagram for G3 to S0 [Deep Sx Platform] - 2 OF 2
Bookmarks
PWRBTN#
SLP_A#
CL_RST#
PLATFORM_VCCASW
SLP_LAN#
VCC_LANPHY
SLP_WLAN#
VCC_WLANPHY
SLP_S5#
SLP_S4#
SLP_S3#
SLP_S0#
CPU_C10_GATE#
VCCST
VCCST_OVRD
DDR_VPP
DDR_VDD2
DDR_VDDQ
VCCSTG
PLATFORM_S0_RAILS
ALL_SYS_PWRGD
VCCST_PWRGD
DDR_VTT_CNTL
VTT
IMVP_VRON
VCCIN
VCCIN_VR_READY
PCH_PWROK
PCH_CLK_OUTPUTS
PROCPWRGD
SYS_PWROK
VCCIO
SUS_STAT#
PLTRST#
THERMTRIP#
CPU_SVID
CPU_SVID_ALERT#
SPI_SIGNALS#
HONORED

Power down:


power down
S0 to G3 Sequence - 1 of 2
SPI_SIGNALS#
SUS_STAT#
PLTRST#
PROCPWRGD
THERMTRIP#
CPU_SVID
CPU_SVID_ALERT#
PCH_CLK_OUTPUTS
CL_RST#
SLP_S3#
SLP_A#
SLP_LAN#
VCC_LANPHY
SLP_WLAN#
VCC_WLANPHY
CPU_RESET#
IMVP_VRON
VCCIN
PLATFORM_VCCASW
VTT
PLATFORM_S0_RAILS
PLATFORM_S0_RAILS_PWRGD
DDR_VTT_CNTL
VCCIN_CTRL
ALL_SYS_PWRGD
VCCST_PWRGD
VCCIN_VR_READY
PCH_PWROK
SYS_PWROK
VCCSTG
SLP_S4#
DDR_RESET#
DDR_VDDQ
VCCST
SLP_S5#
DDR_VPP
HONORED
stable
Will_Track_VCCST_Rail
Will_Track_VCCST_Rail
Will_Track_VCCST_Rail
H_for_WoL_Enabled
H_for_WoWLAN_Enabled
1.ME_SAVES_ANY_CRITICAL_STATES
Assertion_depends_on_system_going_to_Moff_or_M3
Assertion_depends_on_system_going_to_Moff_or_M3
CPU_RESET#_is_on_package_signal_for_U/Y
VCCST_can_be_ON_until_VCCINAUX_goes_LOW
tPCH22
tPCH24
tPCH25
tPCH26
tPLT17
tPCH28
tCPU28a
tPCH29
tCPU22
tCPU22
tPCH27
tCPU28b/tCPU22
tPLT16
Note1
Note2
Note5
Note3
Note3
Note4
Note4
Note6

PCH:



22.4.4 PCH and System Power States

The table below shows the power states defined for PCH-based platforms. The state names generally match the corresponding ACPI states.

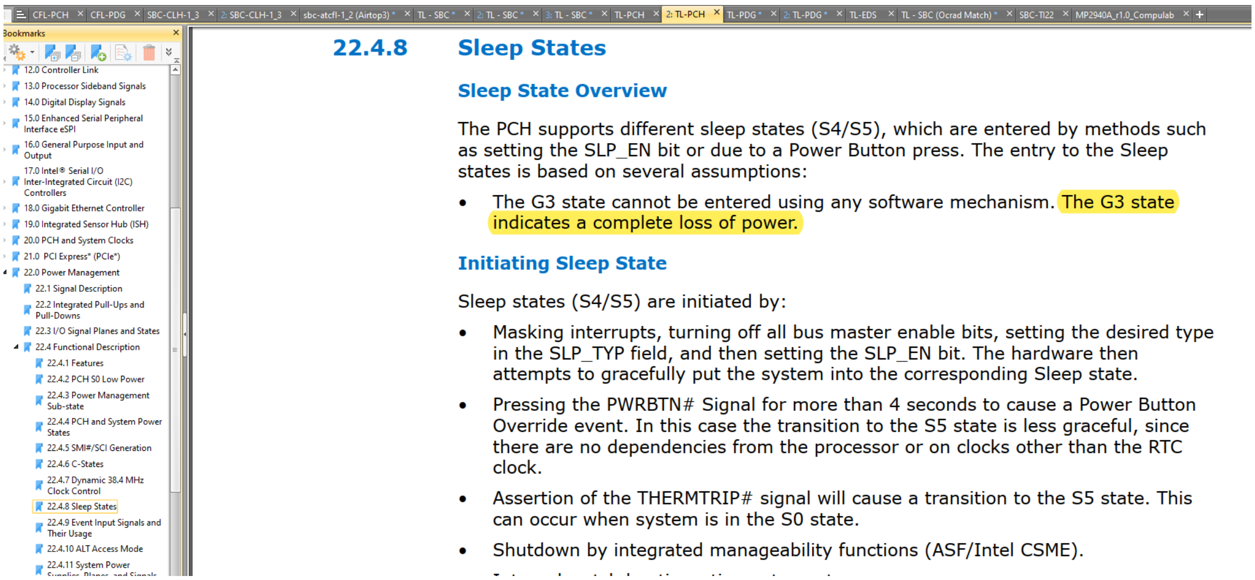
Table 59. General Power States for Systems Using the PCH

State / Substates	Legacy Name/Description
G0/S0/C0	**Full On**: Processor operating. Individual devices may be shut down or be placed into lower power states to save power.
G0/S0/Cx	**Cx States**: C states are processor power states within the S0 system state that provide for various levels of power savings on the processor. The processor manages C states itself. The actual C state is not passed to the PCH. Only C state related messages are sent to the PCH and PCH will base its behavior on the actual data passed.
G1/S4	**Suspend-To-Disk (STD):** The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
G2/S5	**Soft Off (SOFF):** System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.
S0ix	**S0 Idle States:** Processor PKG C states and platform latency tolerance will allow the PCH to decide when to take aggressive power management actions.
Deep Sx	**Deep Sx:** An optional low power state where system context may or may not be maintained depending upon entry condition. All power is shut off except for minimal logic that allows exiting Deep Sx. If Deep Sx state was entered from S4 state, then the resume path will place system back into S4. If Deep Sx state was entered from S5 state, then the resume path will place system back into S5.
G3	**Mechanical OFF (M-Off):** System context not maintained. All power is shut off except for the RTC. No "Wake" events are possible. This state occurs if the user removes the main system batteries in a mobile system, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3 and the AFTERG3_EN bit in the General Power Management Configuration (GEN_PMCON). Refer to table **System Power Plane** for more details.

State / Substates	Legacy Name/Description
G0/S0/C0	**Full On: Processor operating. Individual devices may be shut down or be placed into lower power states to save power.**
G0/S0/Cx	**Cx States: C states are processor power states within the S0 system state that provide for various levels of power savings on the processor. The processor manages C states itself. The actual C state is not passed to the PCH. Only C state related messages are sent to the PCH and PCH will base its behavior on the actual data passed.**
G1/S4	**Suspend-To-Disk (STD): The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.**
G2/S5	**Soft Off (SOFF): System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.**
S0ix	**S0 Idle States: Processor PKG C states and platform latency tolerance will allow the PCH to decide when to take aggressive power management actions.**
Deep Sx	**Deep Sx: An optional low power state where system context may or may not be maintained depending upon entry condition. All power is shut off except for minimal logic that allows exiting Deep Sx. If Deep Sx state was entered from S4 state, then the resume path will place system back into S4. If Deep Sx state was entered from S5 state, then the resume path will place system back into S5.**
G3	**Mechanical OFF (M-Off): System context not maintained. All power is shut off except for the RTC. No "Wake" events are possible. This state occurs if the user removes the main system batteries in a mobile system, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3 and the AFTERG3_EN bit in the General Power Management Configuration (GEN_PMCON). Refer to table System Power**

	Plane for more details.

Sleep States



22.4.8 Sleep States

Sleep State Overview

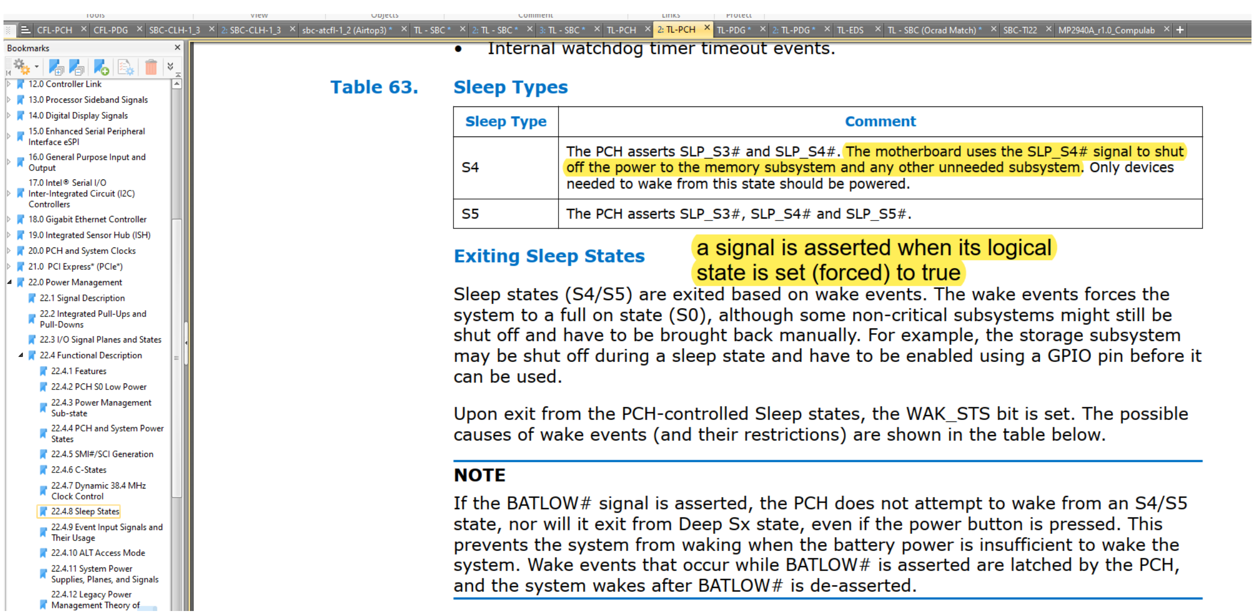
The PCH supports different sleep states (S4/S5), which are entered by methods such as setting the SLP_EN bit or due to a Power Button press. The entry to the Sleep states is based on several assumptions:

- The G3 state cannot be entered using any software mechanism. The G3 state indicates a complete loss of power.

Initiating Sleep State

Sleep states (S4/S5) are initiated by:

- Masking interrupts, turning off all bus master enable bits, setting the desired type in the SLP_TYP field, and then setting the SLP_EN bit. The hardware then attempts to gracefully put the system into the corresponding Sleep state.
- Pressing the PWRBTN# Signal for more than 4 seconds to cause a Power Button Override event. In this case the transition to the S5 state is less graceful, since there are no dependencies from the processor or on clocks other than the RTC clock.
- Assertion of the THERMTRIP# signal will cause a transition to the S5 state. This can occur when system is in the S0 state.
- Shutdown by integrated manageability functions (ASF/Intel CSME).



- Internal watchdog timer timeout events.

Table 63. Sleep Types

Sleep Type	Comment
S4	The PCH asserts SLP_S3# and SLP_S4#. The motherboard uses the SLP_S4# signal to shut off the power to the memory subsystem and any other unneeded subsystem. Only devices needed to wake from this state should be powered.
S5	The PCH asserts SLP_S3#, SLP_S4# and SLP_S5#.

Exiting Sleep States

a signal is asserted when its logical state is set (forced) to true

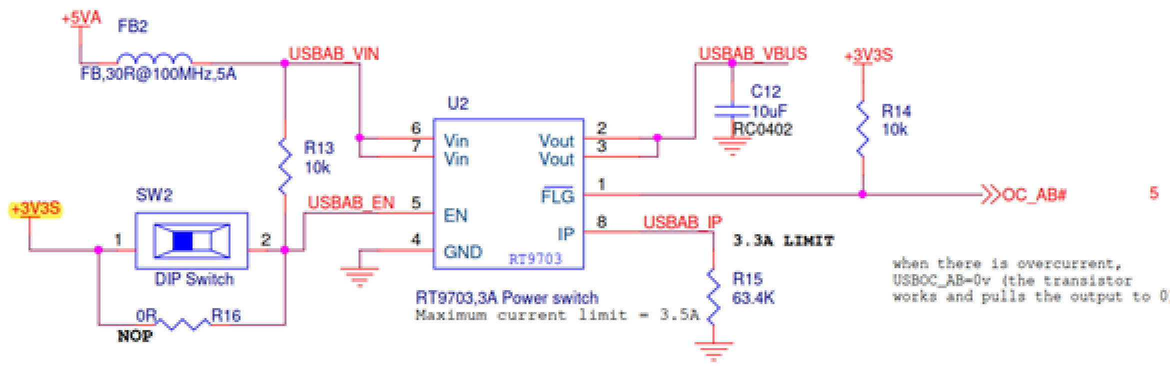
Sleep states (S4/S5) are exited based on wake events. The wake events forces the system to a full on state (S0), although some non-critical subsystems might still be shut off and have to be brought back manually. For example, the storage subsystem may be shut off during a sleep state and have to be enabled using a GPIO pin before it can be used.

Upon exit from the PCH-controlled Sleep states, the WAK_STS bit is set. The possible causes of wake events (and their restrictions) are shown in the table below.

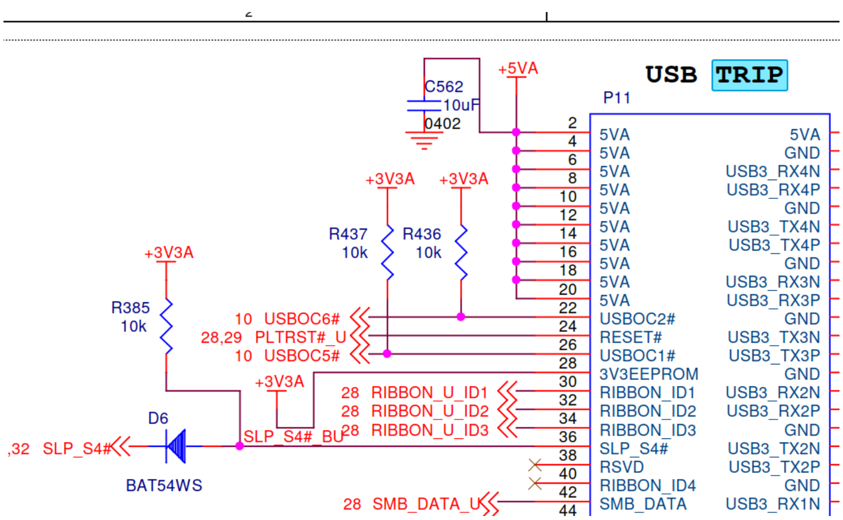
NOTE

If the BATLOW# signal is asserted, the PCH does not attempt to wake from an S4/S5 state, nor will it exit from Deep Sx state, even if the power button is pressed. This prevents the system from waking when the battery power is insufficient to wake the system. Wake events that occur while BATLOW# is asserted are latched by the PCH, and the system wakes after BATLOW# is de-asserted.

USB:



Every USB port must always have VBUS when the system is on S3.
Having that, the wanted status is to turn the VBUS of on S4 and S5, and addition of a switch to change it is a good feature.



When SLP_S4# = 0 (from the CPU) then SLP_S4#=1 inside the TEL.

And if we turn the switch ON, that means SLP_S4#=1 will enable VBUS even when the CPU is in S4 and S5.