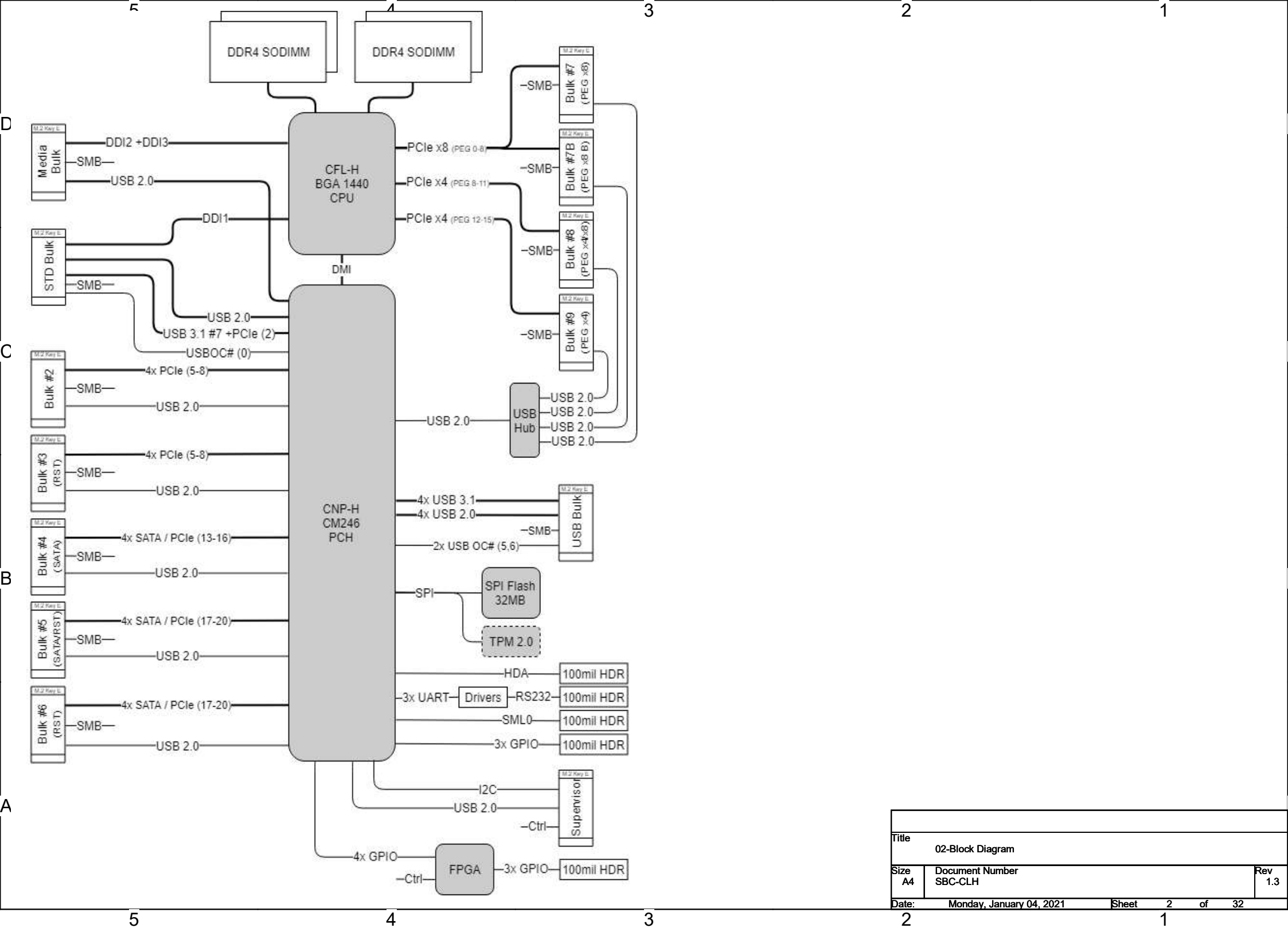


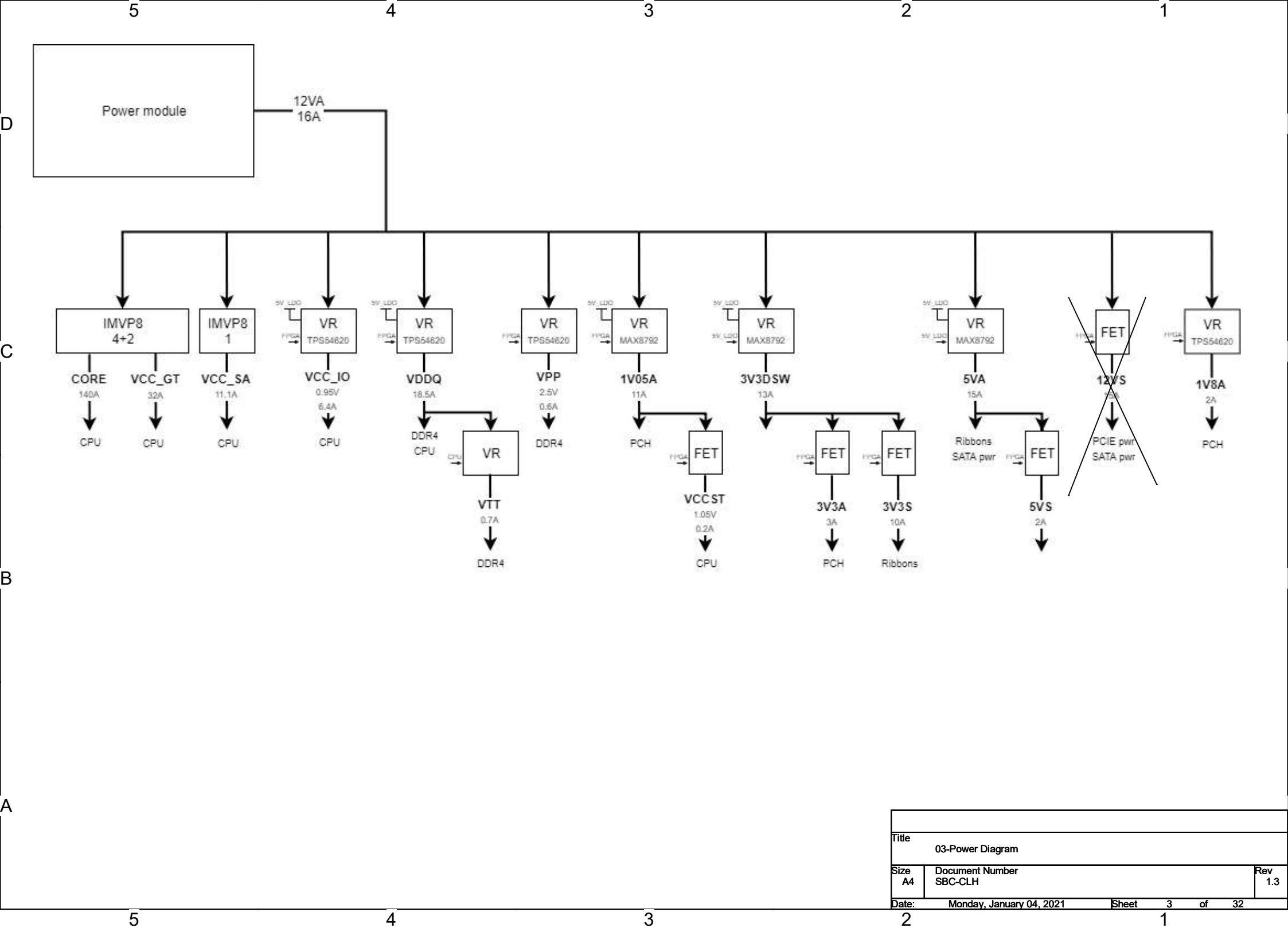
SBC-CLH

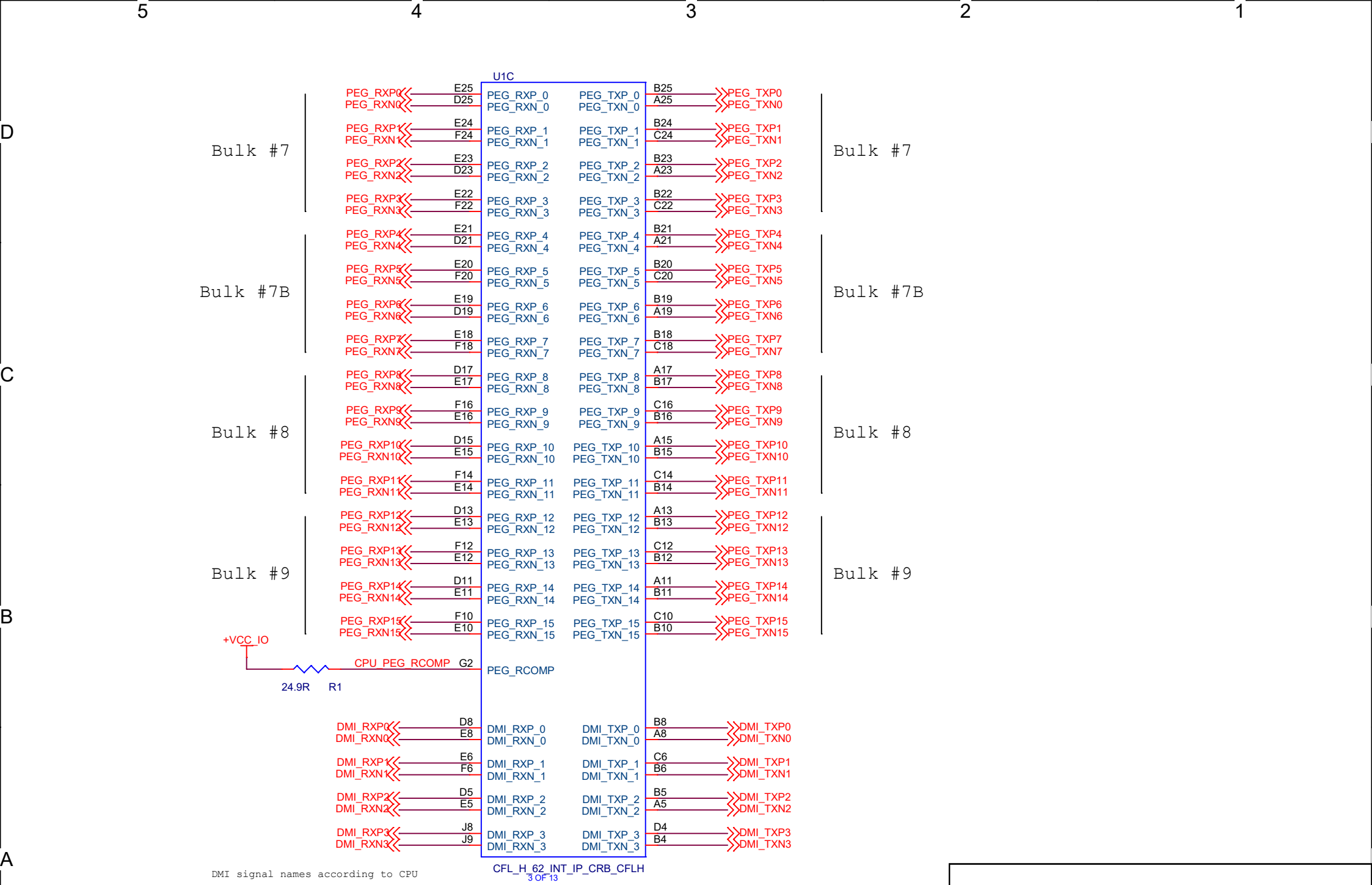
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CM246 PCH Flexible I/O																CPU PEG																CPU Graphics																																																																																																																																																																																																																																																																																																																																																																																																																																																																														
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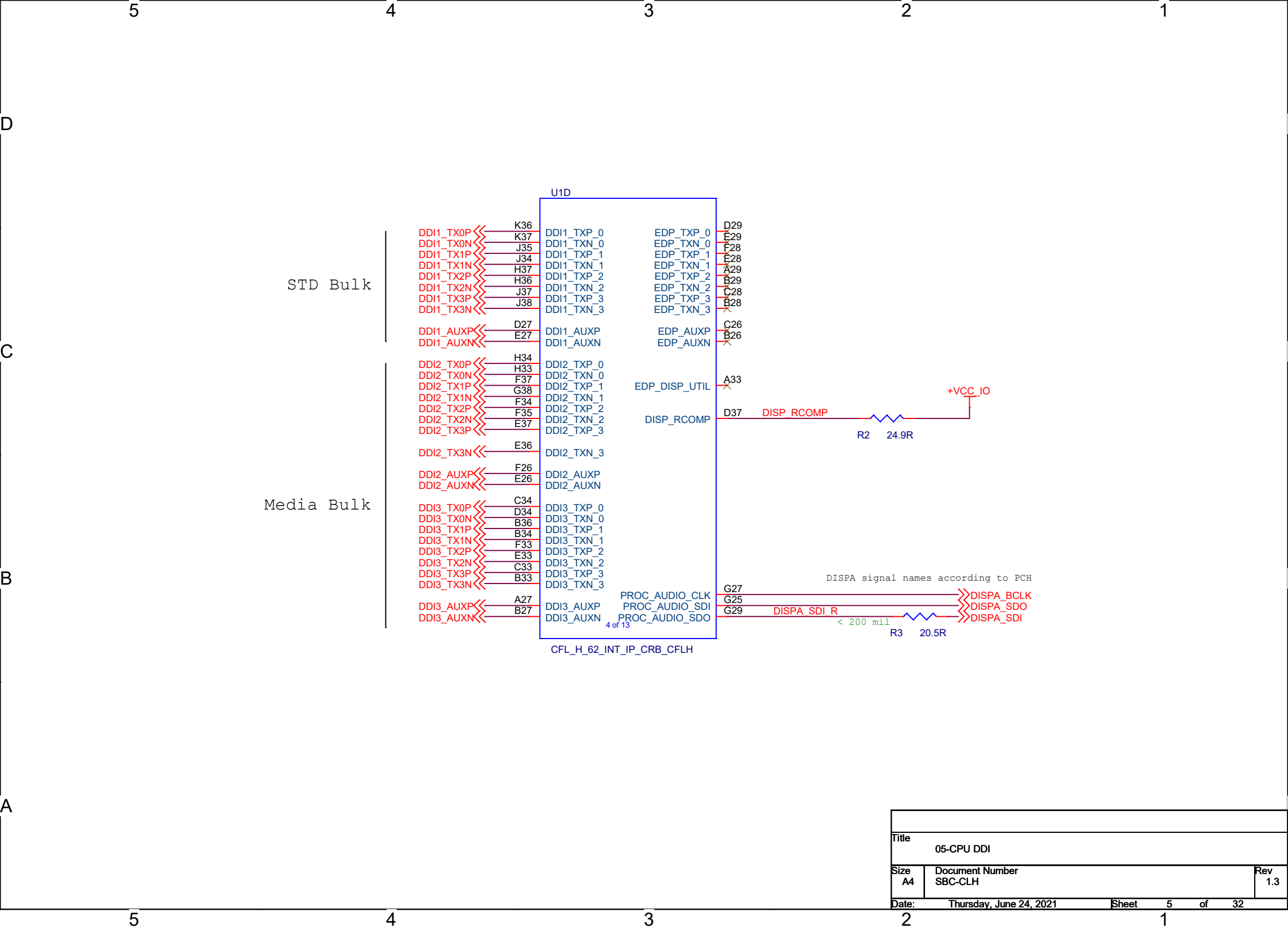


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02-Block Diagram		
Size	Document Number	Rev
A4	SBC-CLH	1.3
Date:	Monday, January 04, 2021	Sheet 2 of 32





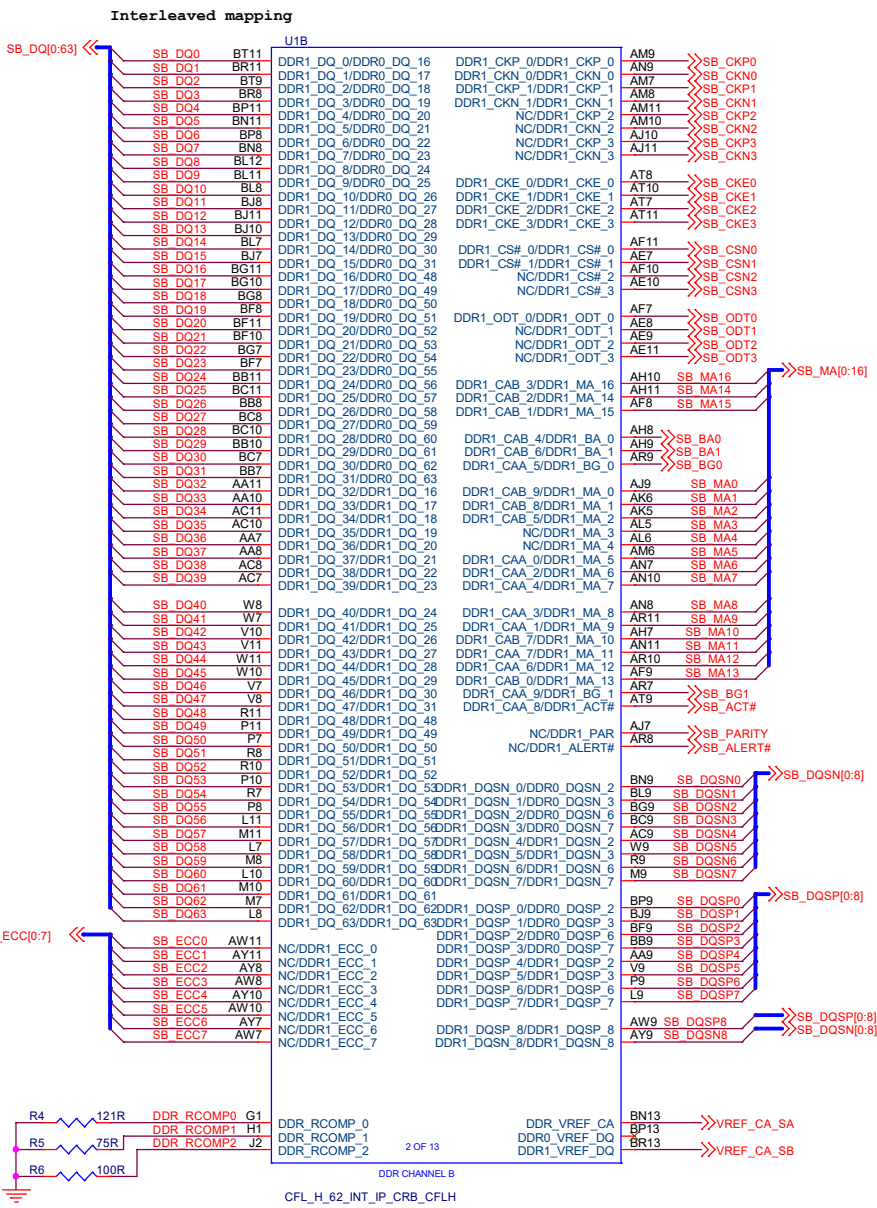
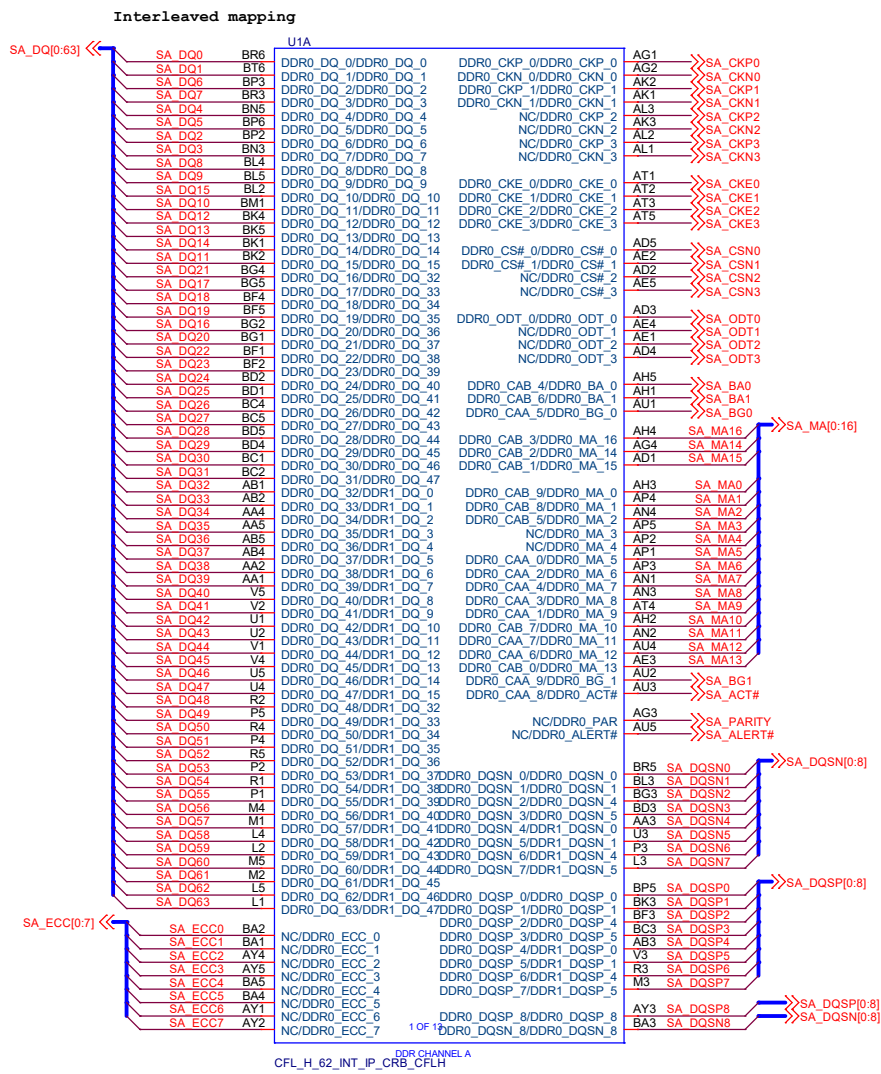
Title 04-CPU PEG/DMI			
Size A4	Document Number SBC-CLH		Rev 1.3
Date:	Thursday, June 24, 2021	Sheet 4 of 32	



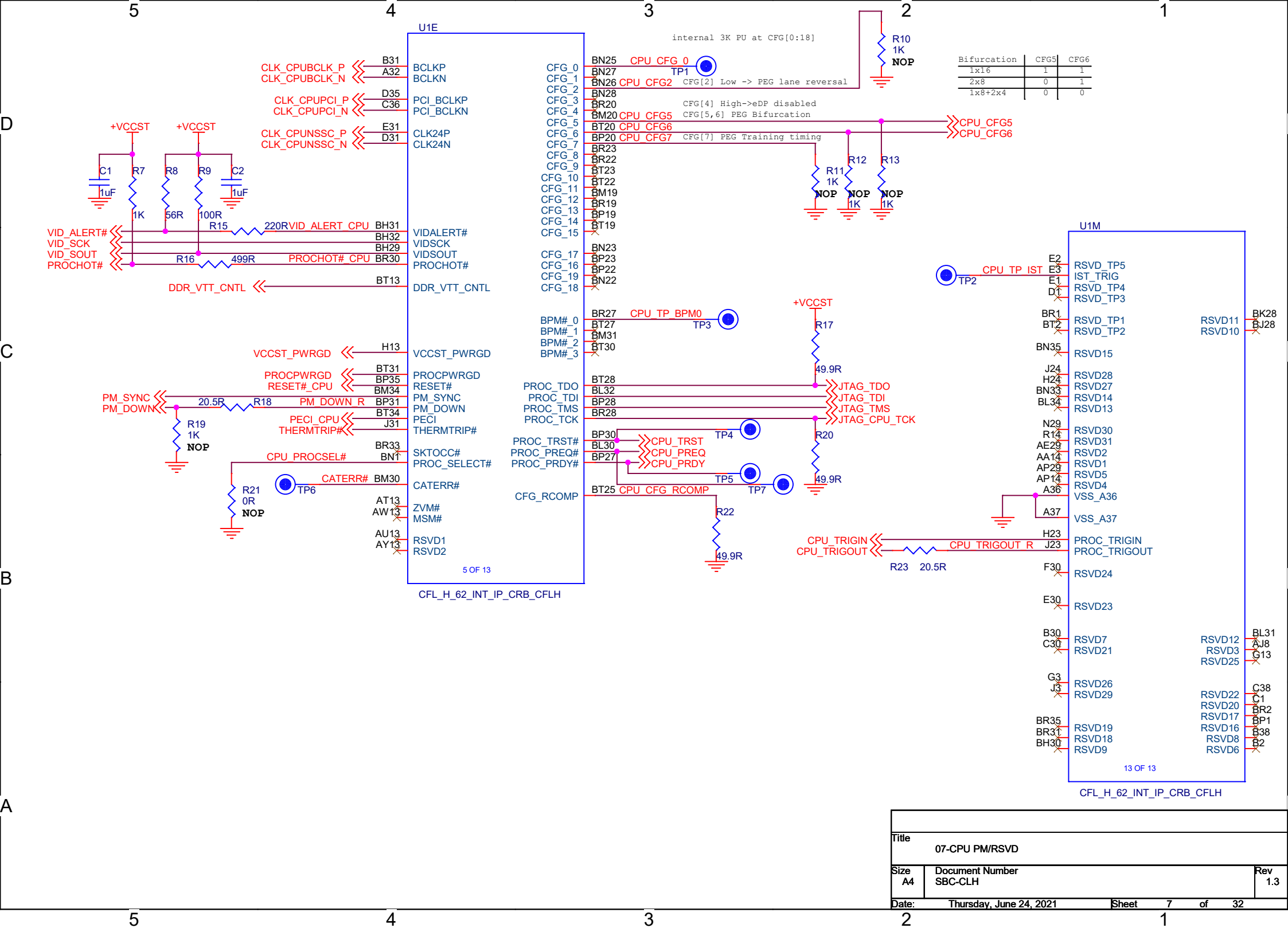
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Size	Document Number	Rev
A4	SBC-CLH	1.3
Date:	Thursday, June 24, 2021	Sheet 5 of 32

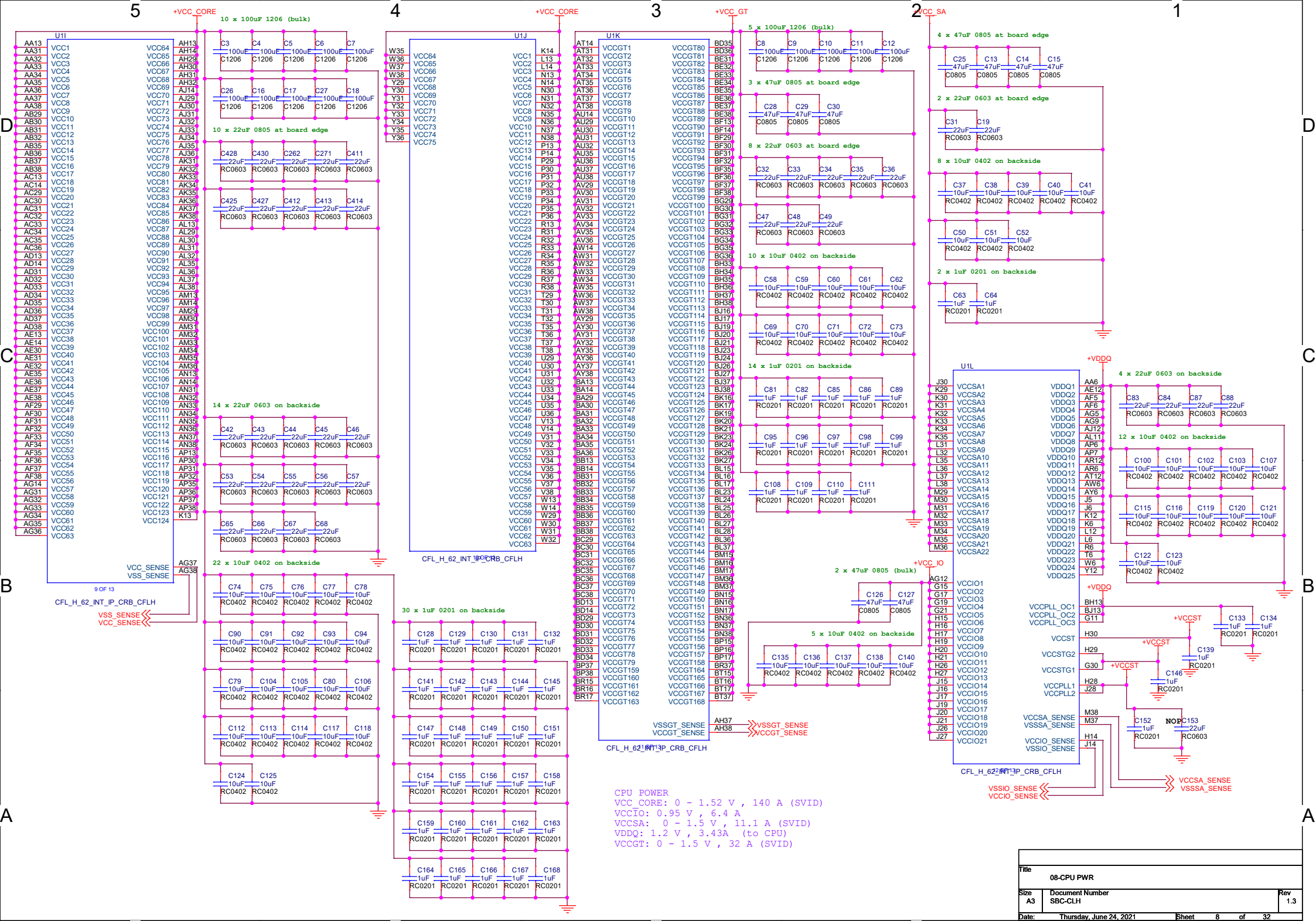
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Data bits can be swapped within a byte

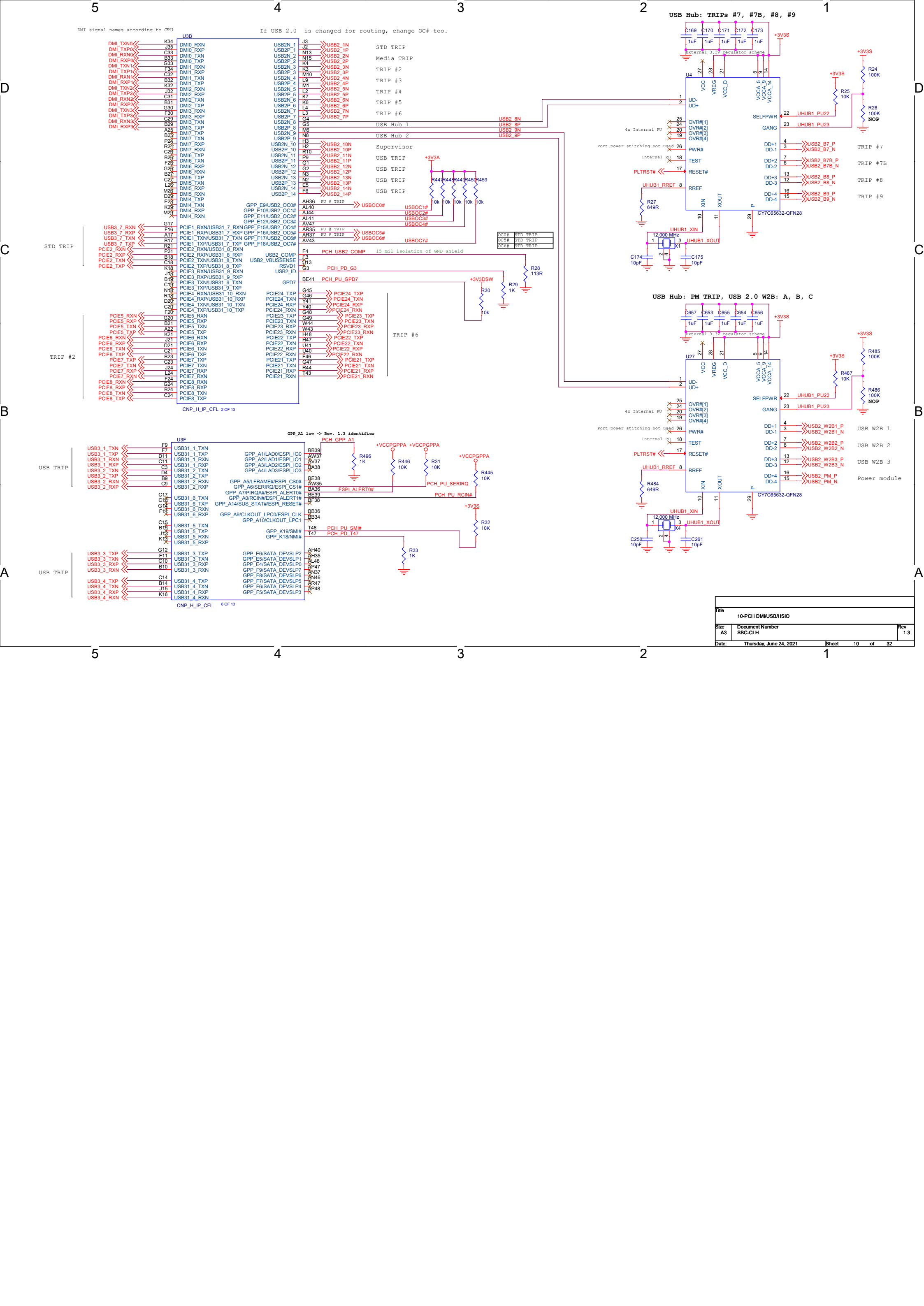


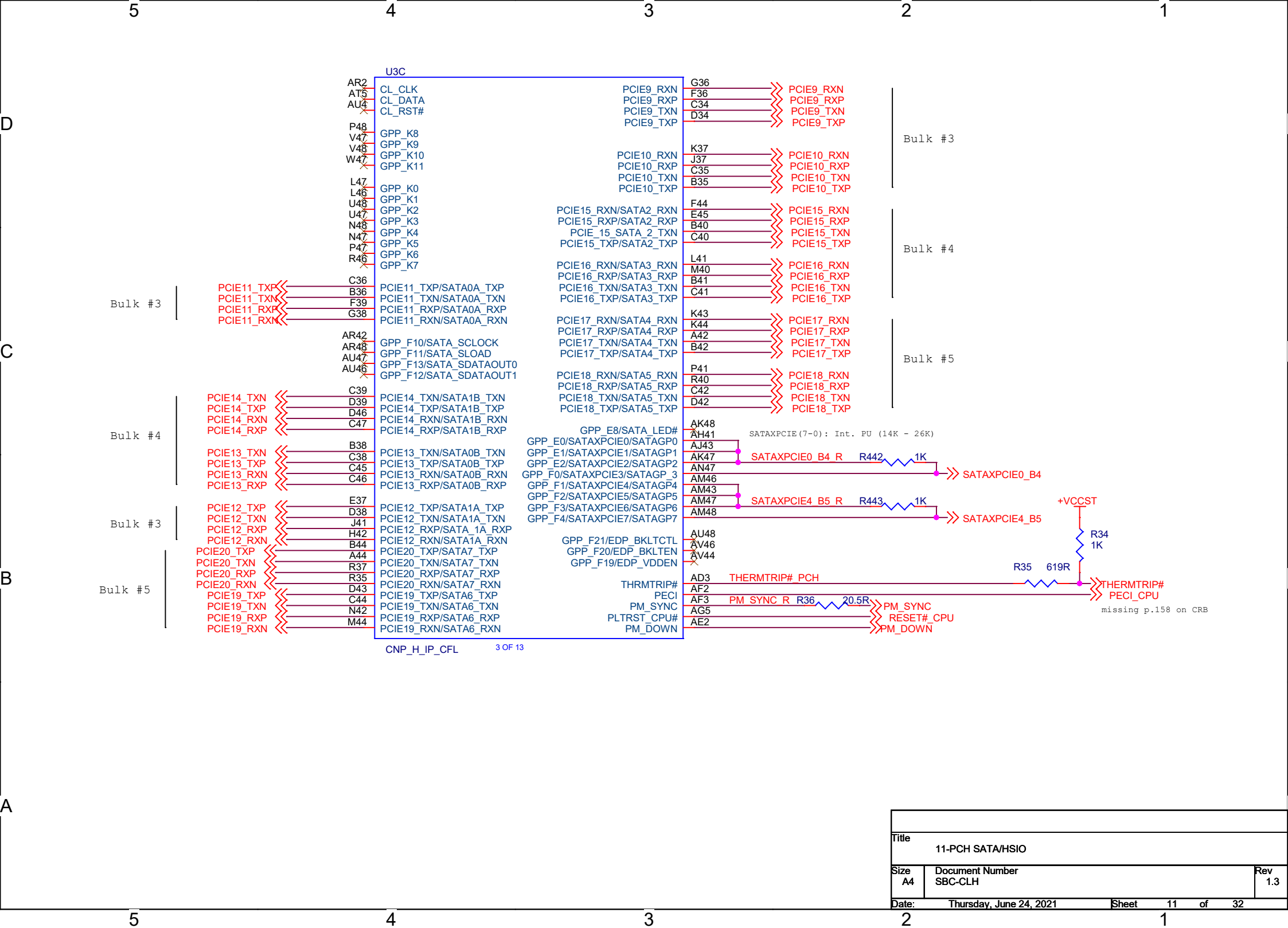
Title		
06-CPU DDR4		
Size	Document Number	Rev
A3	SBC-CLH	1.3
Date:	Thursday, June 24, 2021	Sheet 6 of 32



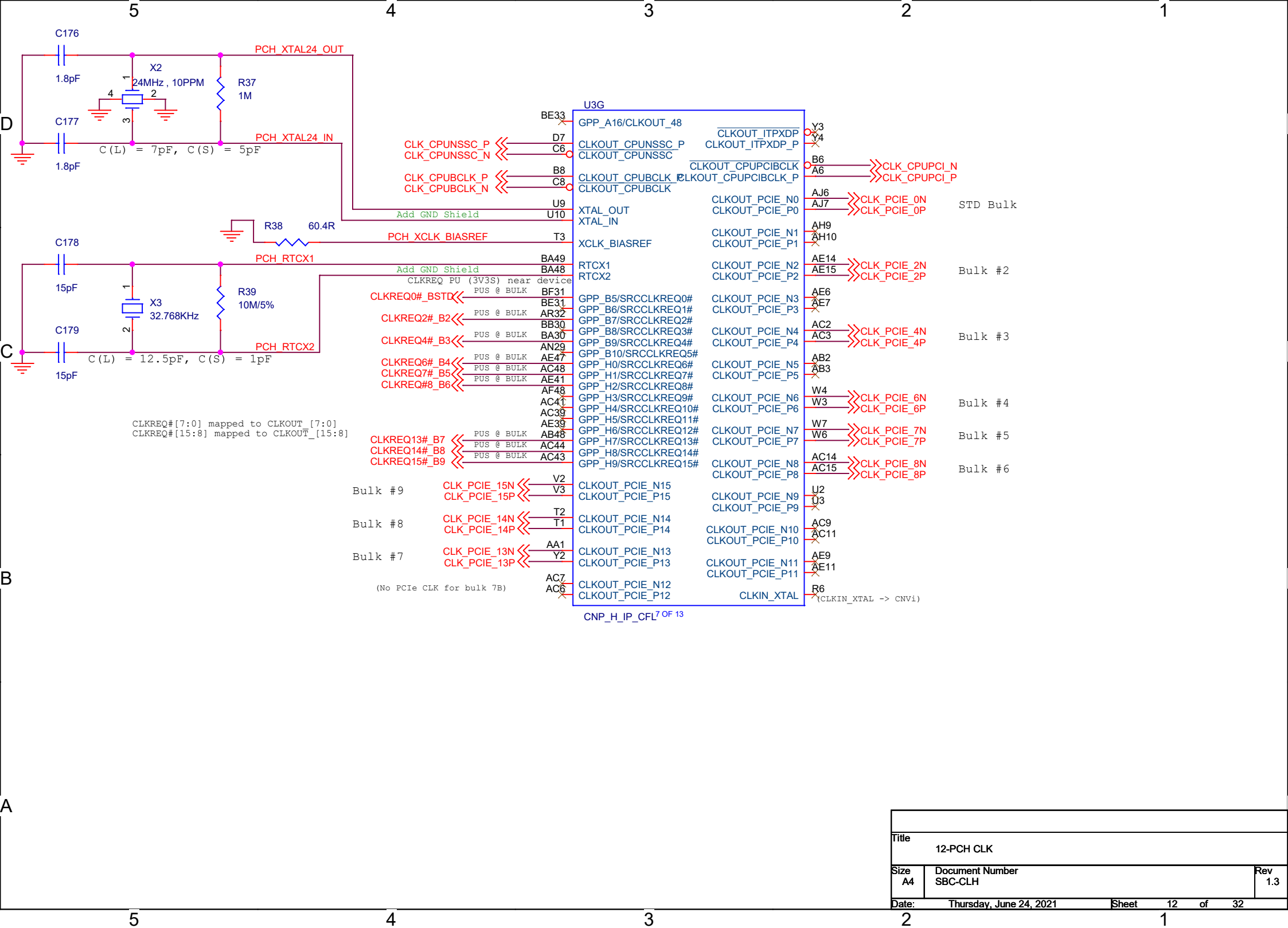


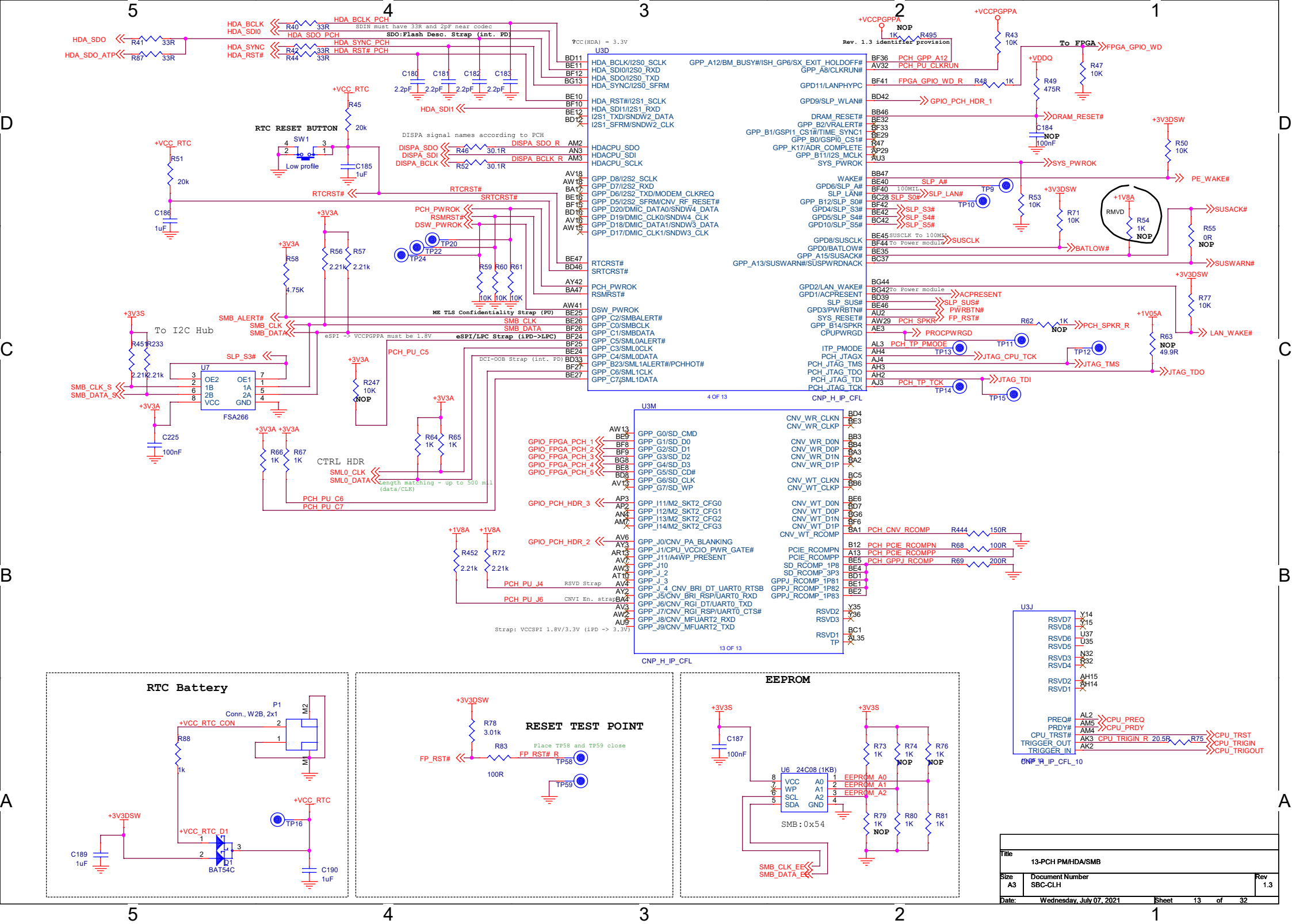
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A12	VSS 2	VSS 83	AL10
A16	VSS 3	VSS 84	AL12
A18	VSS 4	VSS 85	AL14
A20	VSS 5	VSS 86	AL33
A22	VSS 6	VSS 87	AL34
A24	VSS 7	VSS 88	AL4
A26	VSS 8	VSS 89	AL7
A28	VSS 9	VSS 90	AL8
A30	VSS 10	VSS 91	AL9
A6	VSS 11	VSS 92	AM1
A9	VSS 12	VSS 93	AM2
AA12	VSS 13	VSS 94	AM3
AA29	VSS 14	VSS 95	AM37
AA30	VSS 15	VSS 96	AM38
AB33	VSS 16	VSS 97	AM4
AB34	VSS 17	VSS 98	AM5
AB6	VSS 18	VSS 99	AN12
AC1	VSS 19	VSS 100	AN29
AC12	VSS 20	VSS 101	AN30
AC2	VSS 21	VSS 102	AN5
AC37	VSS 22	VSS 103	AN6
AC38	VSS 23	VSS 104	AP10
AC4	VSS 24	VSS 105	AP11
AC5	VSS 25	VSS 106	AP12
AC6	VSS 26	VSS 107	AP18
AD10	VSS 27	VSS 108	AP34
AD11	VSS 28	VSS 109	AP9
AD12	VSS 29	VSS 110	AR1
AD29	VSS 30	VSS 111	AR12
AD30	VSS 31	VSS 112	AR14
AD6	VSS 32	VSS 113	AR2
AD8	VSS 33	VSS 114	AR29
AD9	VSS 34	VSS 115	AR3
AE33	VSS 35	VSS 116	AR37
AE34	VSS 36	VSS 117	AR38
AE6	VSS 37	VSS 118	AR39
AF1	VSS 38	VSS 119	BE1
AF12	VSS 39	VSS 120	BE2
AF13	VSS 40	VSS 121	BE29
AF14	VSS 41	VSS 122	BE3
AF2	VSS 42	VSS 123	BE34
AF3	VSS 43	VSS 124	BE4
AF4	VSS 44	VSS 125	BE5
AG10	VSS 45	VSS 126	BE6
AG11	VSS 46	VSS 127	BE6
AG13	VSS 47	VSS 128	BF12
AG29	VSS 48	VSS 129	BF33
AG30	VSS 49	VSS 130	BF34
AG6	VSS 50	VSS 131	BF6
AG7	VSS 51	VSS 132	BG12
AG8	VSS 52	VSS 133	BG13
AH12	VSS 53	VSS 134	BG14
AH33	VSS 54	VSS 135	BG37
AH34	VSS 55	VSS 136	BG38
AH35	VSS 56	VSS 137	BG6
AH36	VSS 57	VSS 138	BH1
AJ1	VSS 58	VSS 139	BH10
AJ13	VSS 59	VSS 140	BH11
AJ2	VSS 60	VSS 141	BH12
AJ3	VSS 61	VSS 142	BH14
AJ37	VSS 62	VSS 143	AV37
AJ38	VSS 63	VSS 144	BH2
AJ4	VSS 64	VSS 145	BH3
AJ5	VSS 65	VSS 146	BH4
AJ6	VSS 66	VSS 147	BH5
W4	VSS 67	VSS 148	BH7
W5	VSS 68	VSS 149	BH8
Y10	VSS 69	VSS 150	BH9
Y11	VSS 70	VSS 151	I2
Y13	VSS 71	VSS 152	I3
Y14	VSS 72	VSS 153	I33
Y37	VSS 73	VSS 154	I34
Y38	VSS 74	VSS 155	I4
Y7	VSS 75	VSS 156	I5
Y8	VSS 76	VSS 157	I6
Y9	VSS 77	VSS 158	I7
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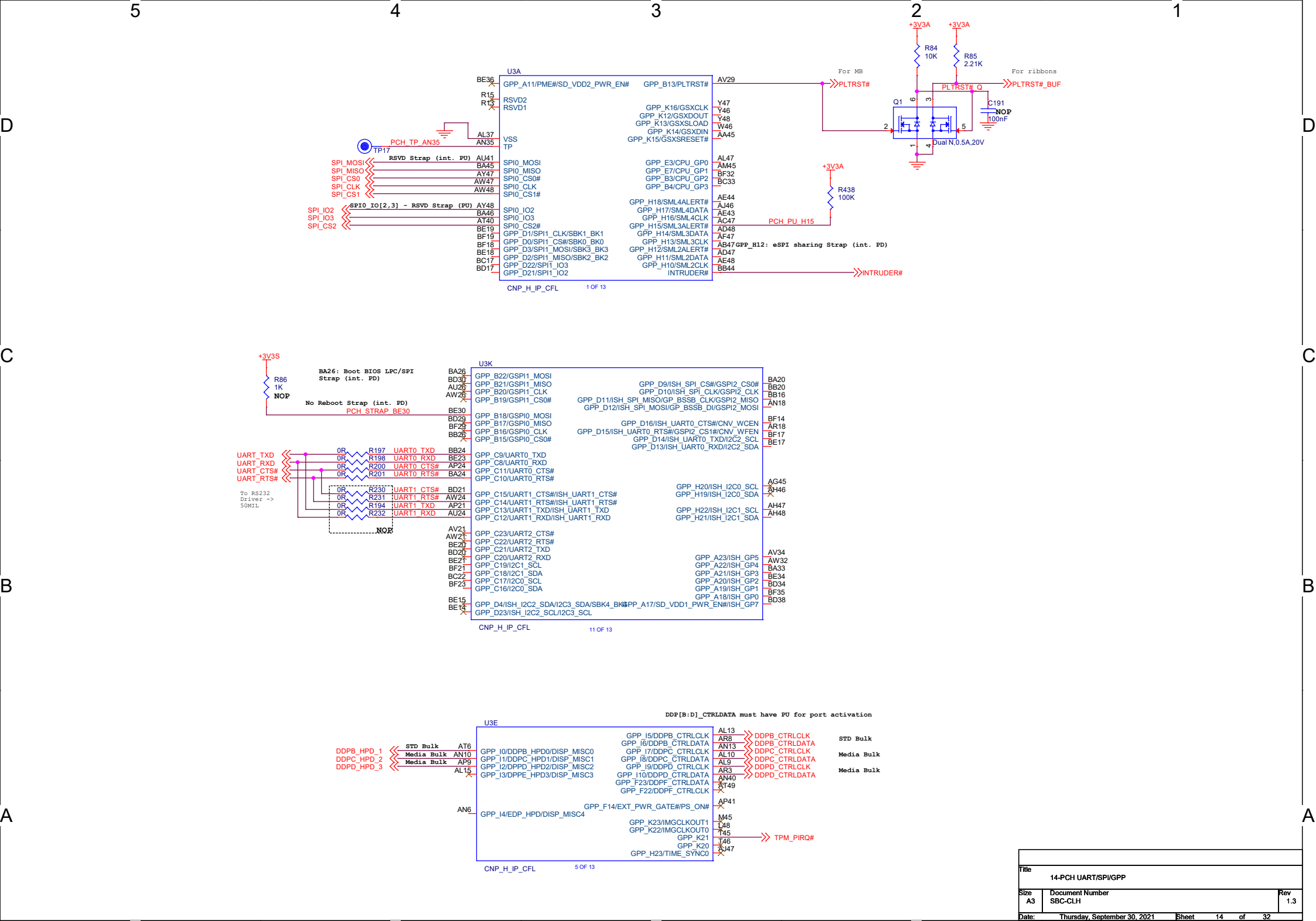


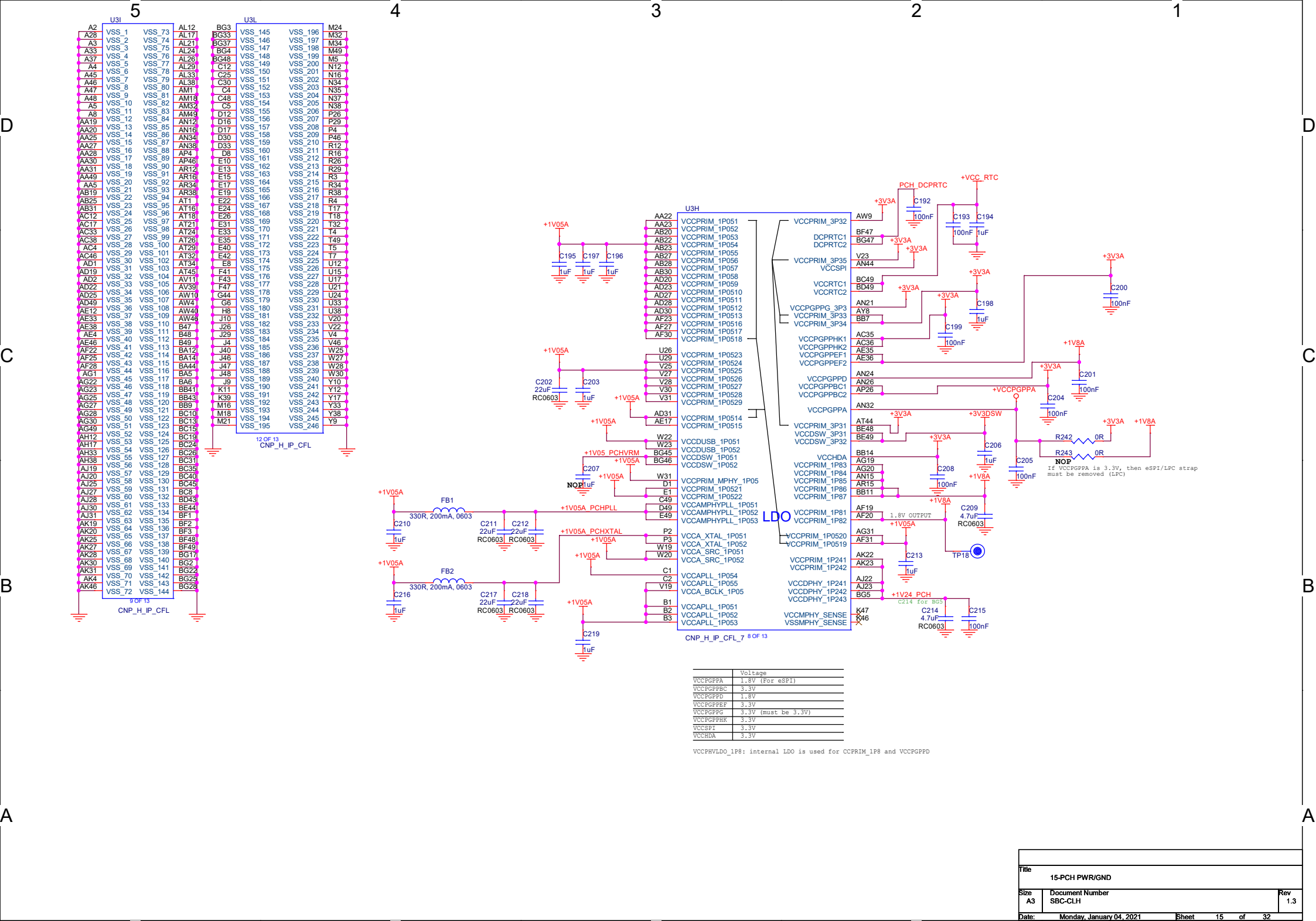


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11-PCH SATA/HSIO		
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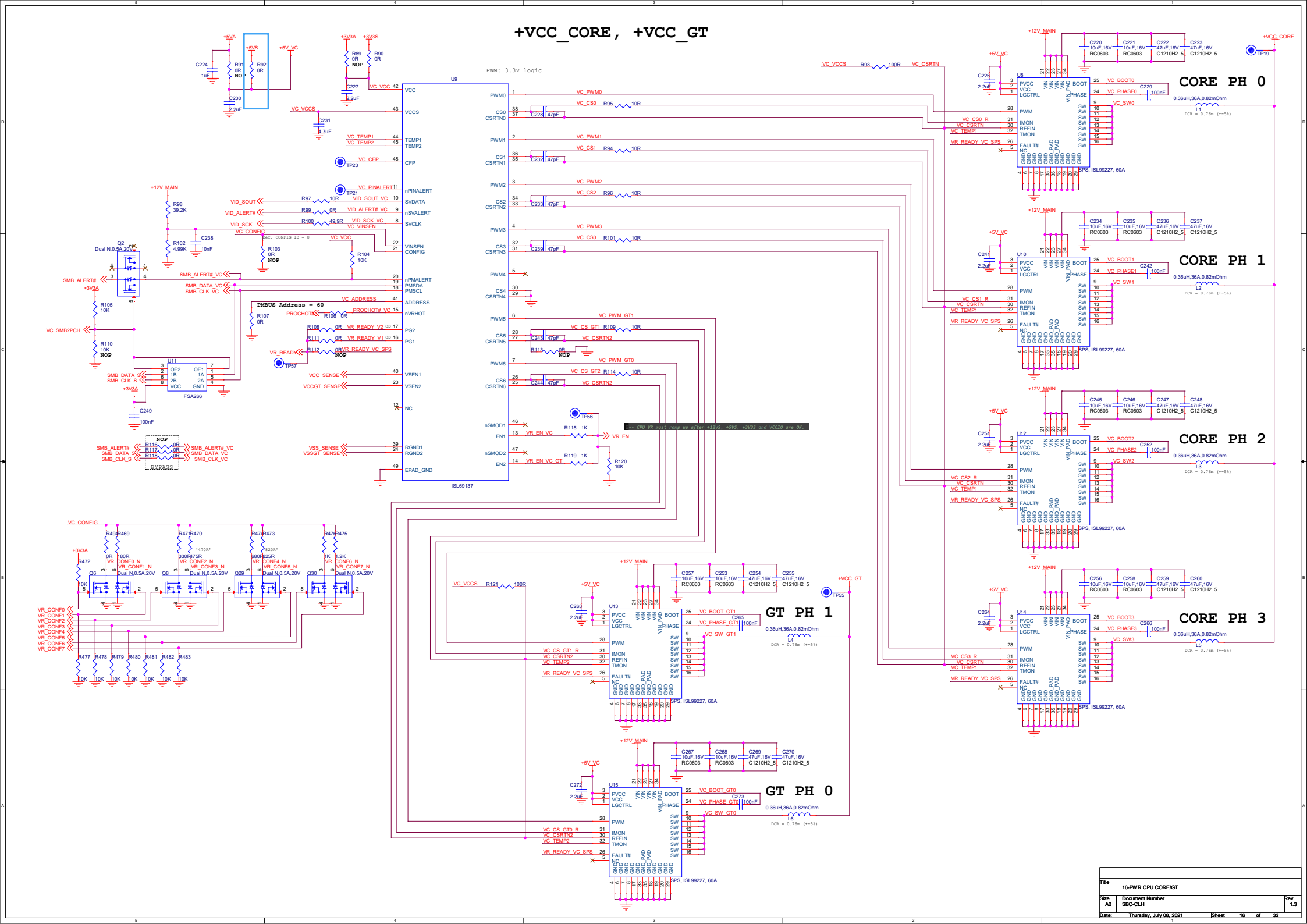




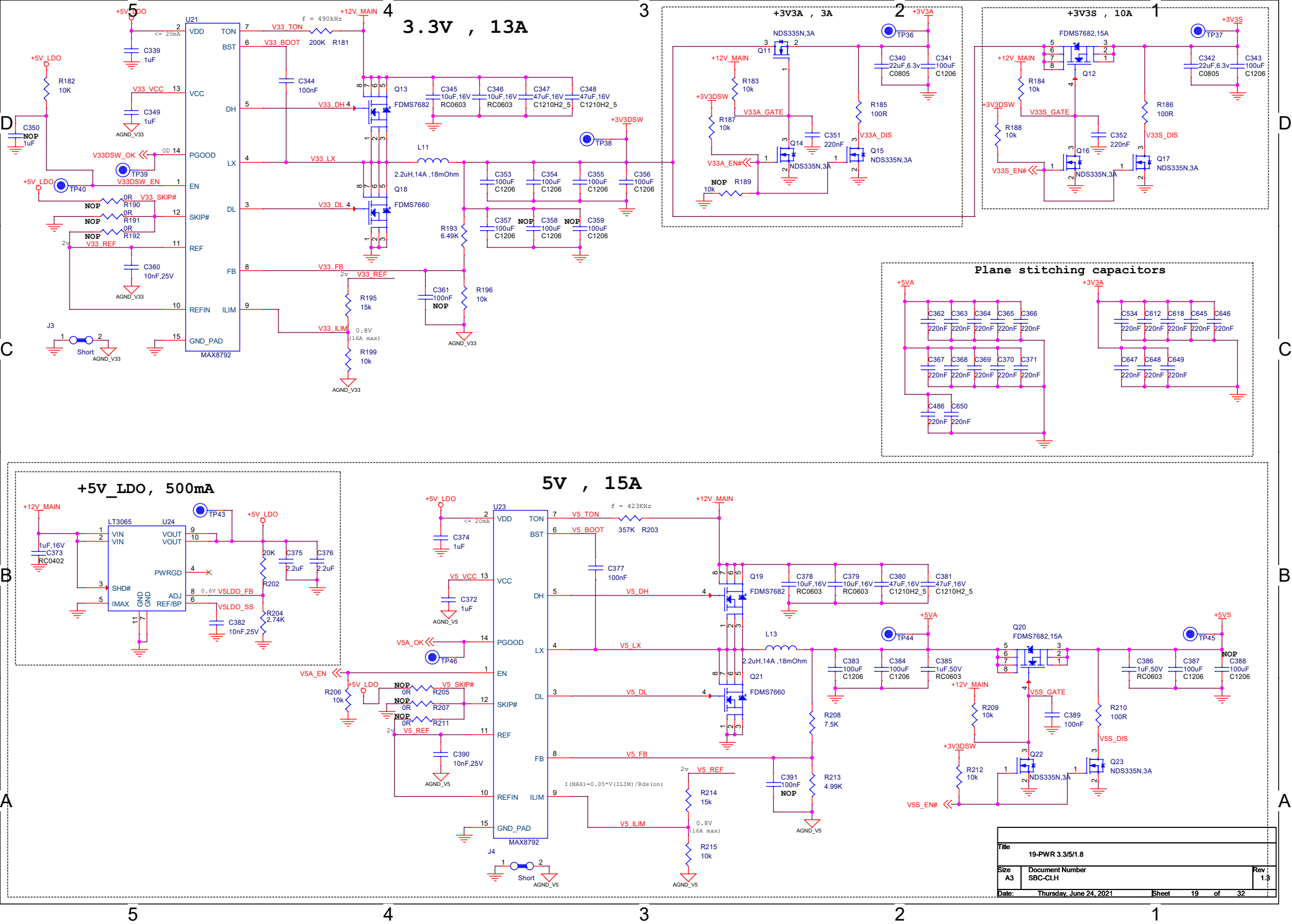


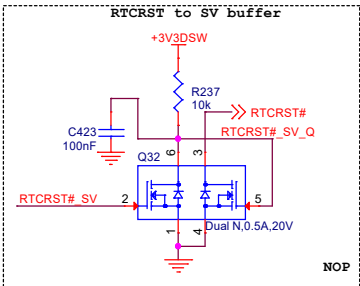
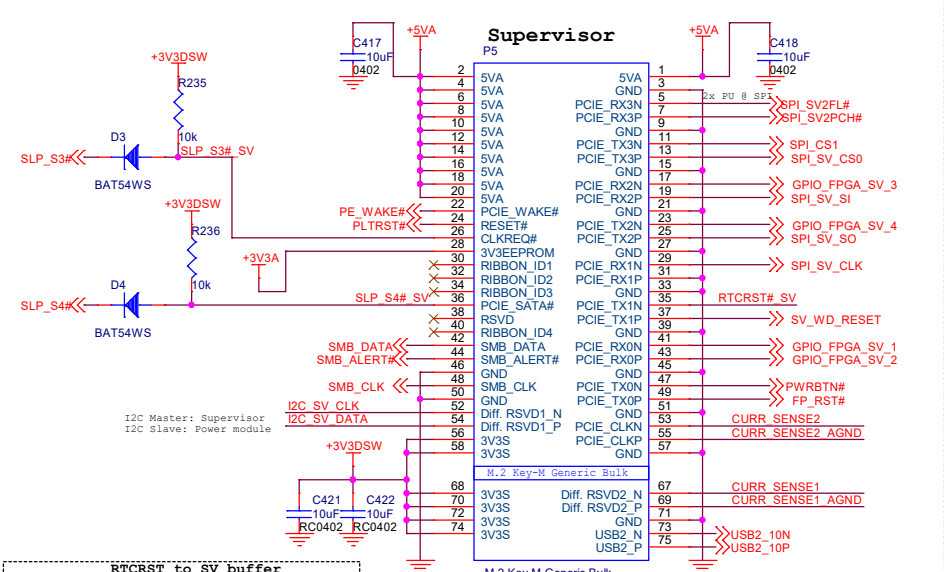
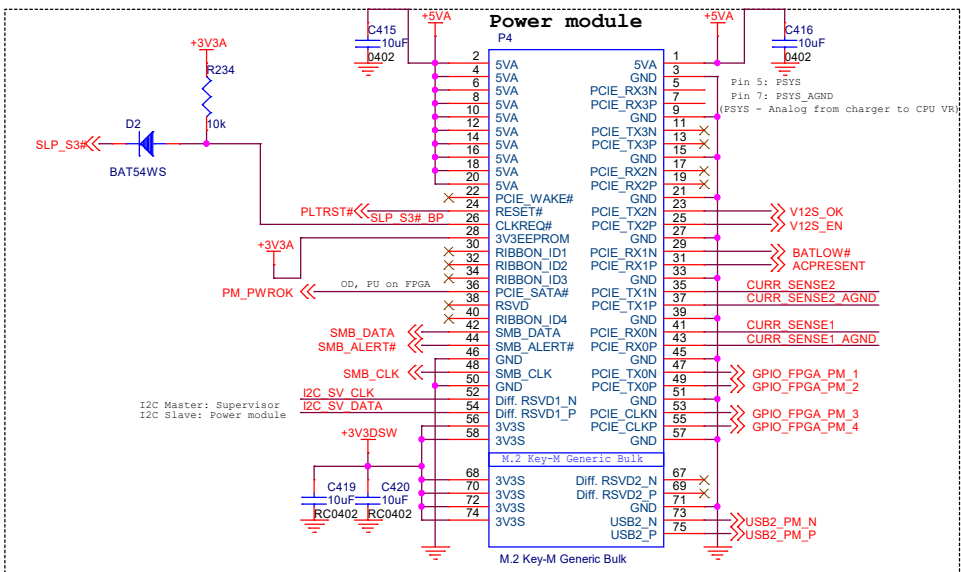


+VCC_CORE, +VCC_GT

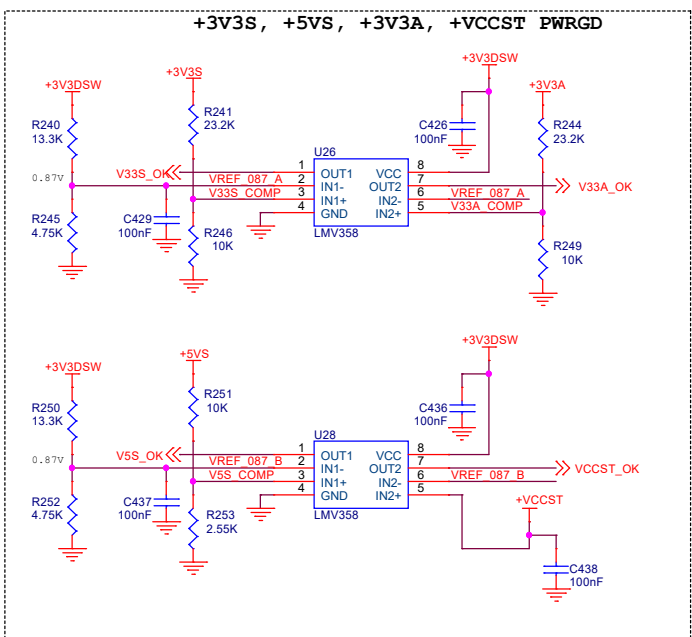


Title			16-PWR CPU CORE/GT
Size	Document Number	Rev	
A2	SRC-CLH	1.3	
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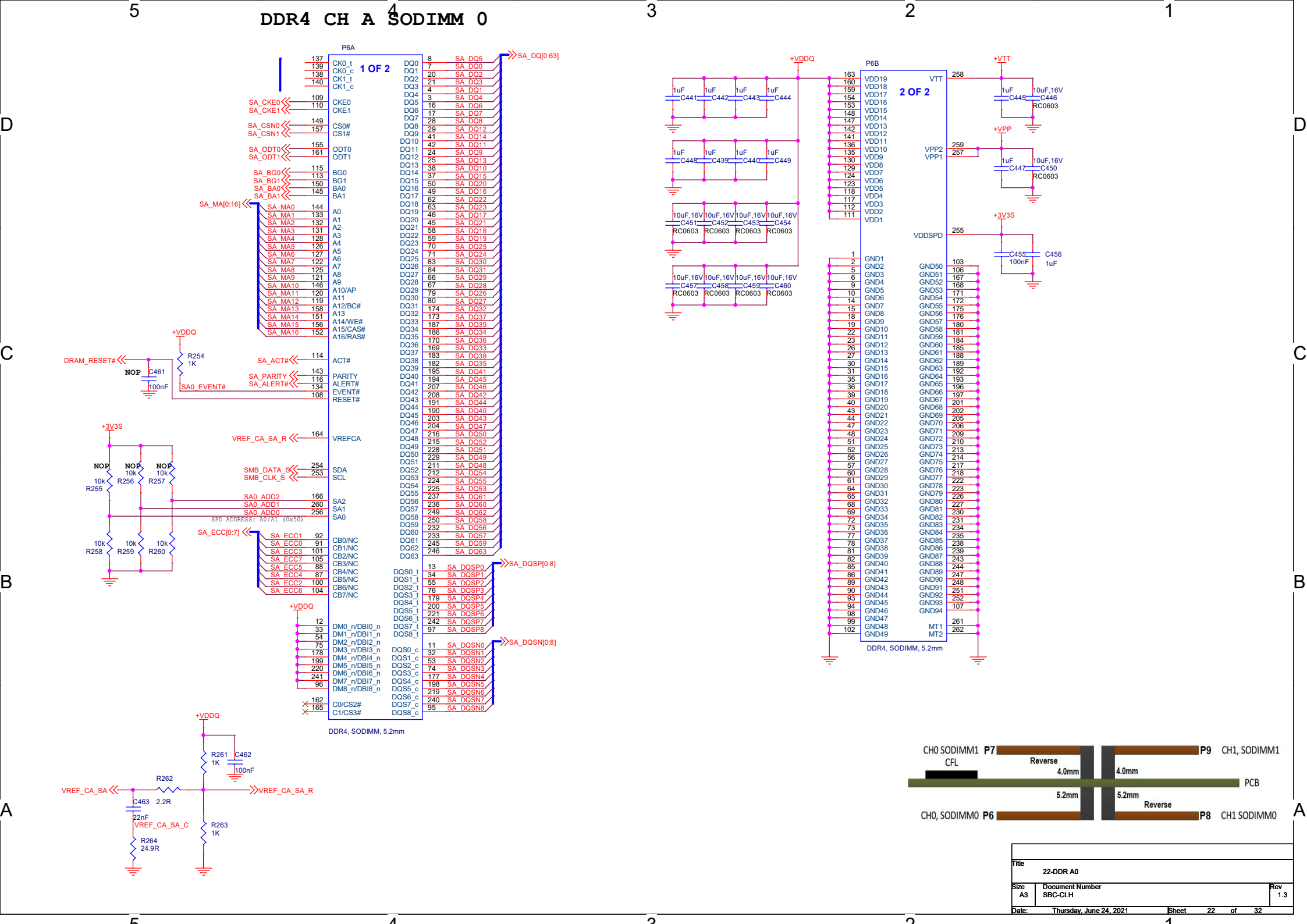


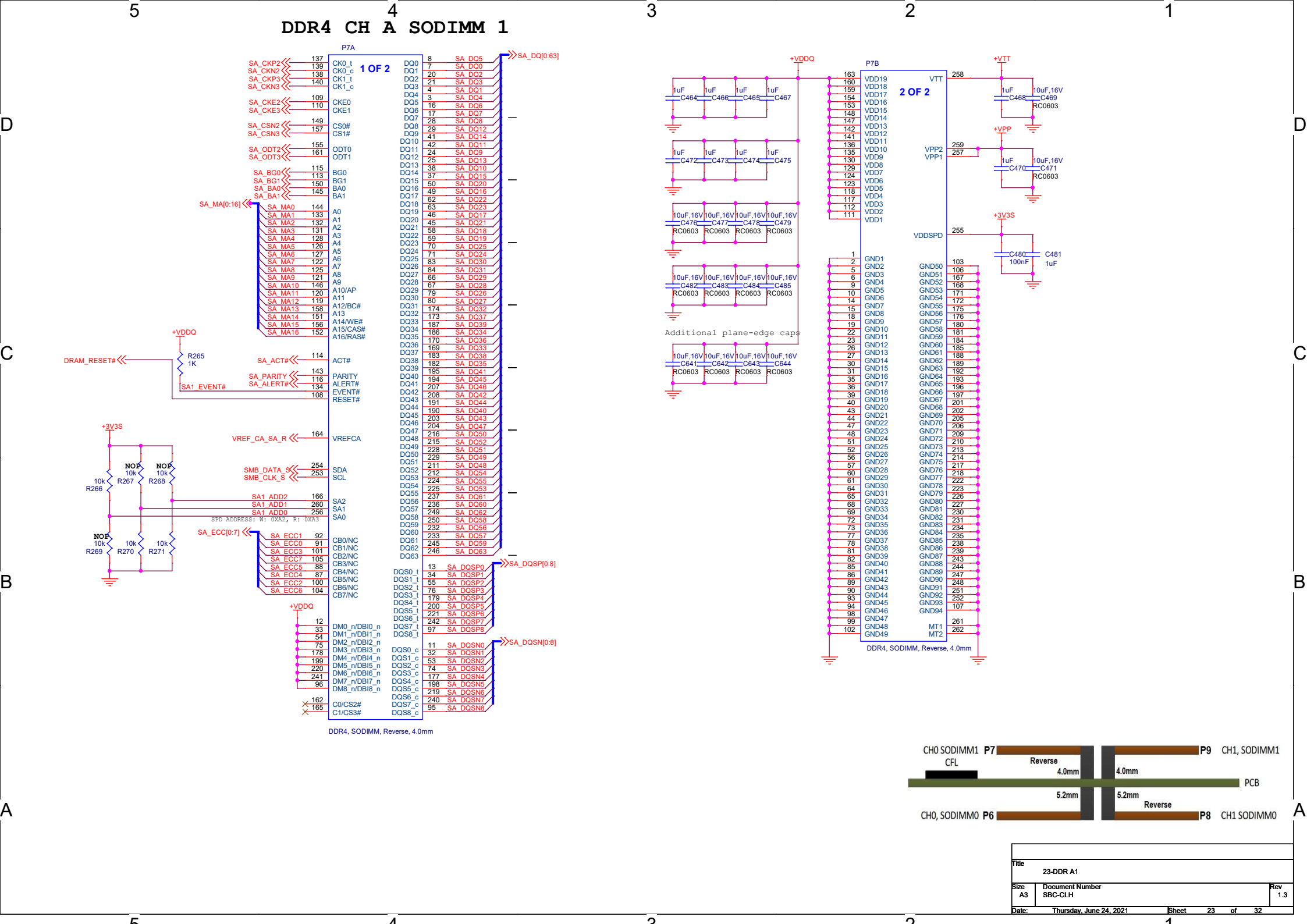


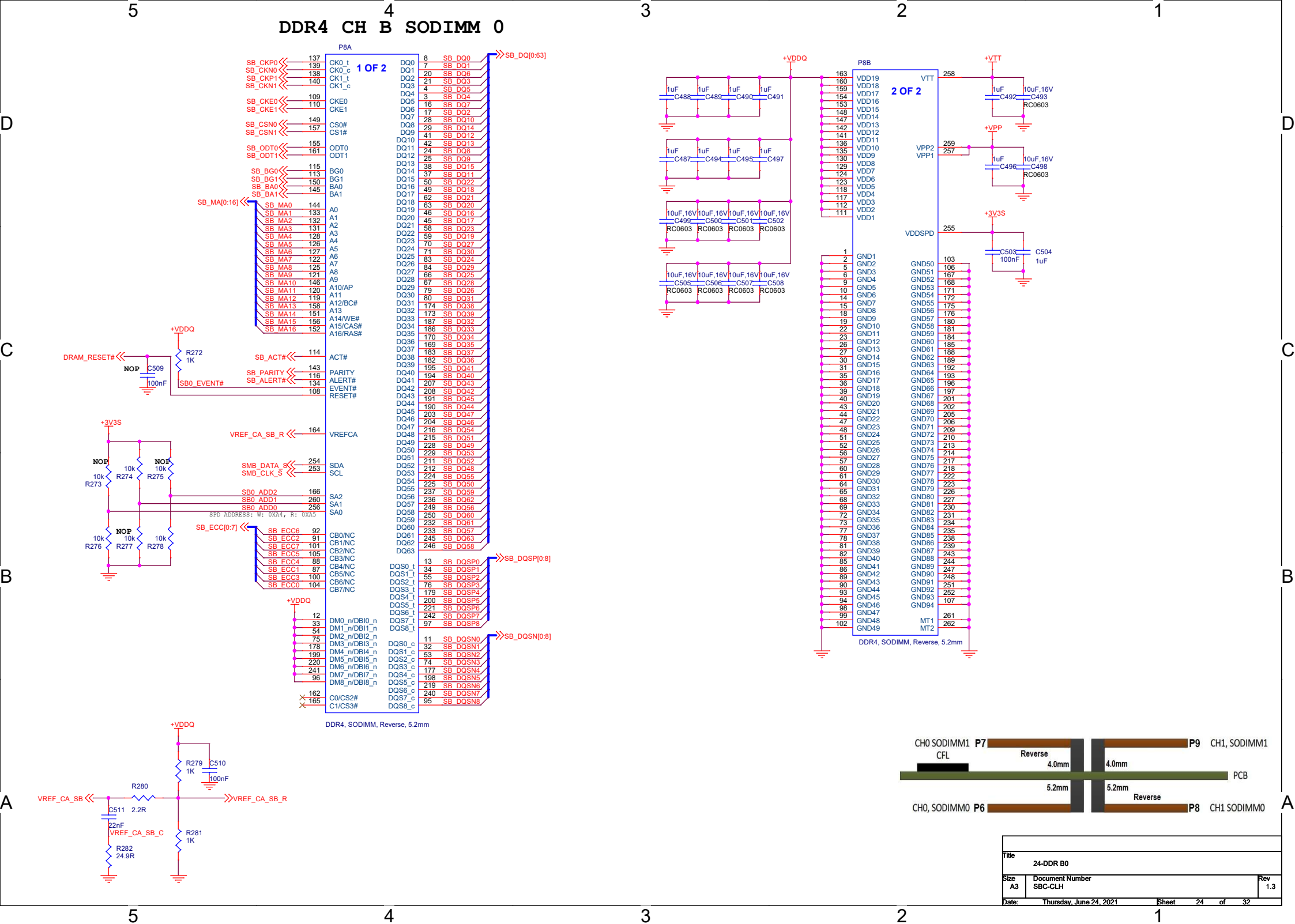
This signal purpose was to enable the supervisor to make a reset for the FPGA. (supervisor is an entity with high credibility).
since the supervisor is a system that could be getting power from battery, or has a MCU that resets it's gone on PWR UP, we want a buffer that makes sure the RTCRST# doesn't change.
when RTCRST#_SV is LOW RTCRST# is LOW.
RTCRST# doesn't go LOW when there is no +3V3DSW, which means after we the SoC has passed all powerup sequence and it's alive, only after that RTCRST# can operate.

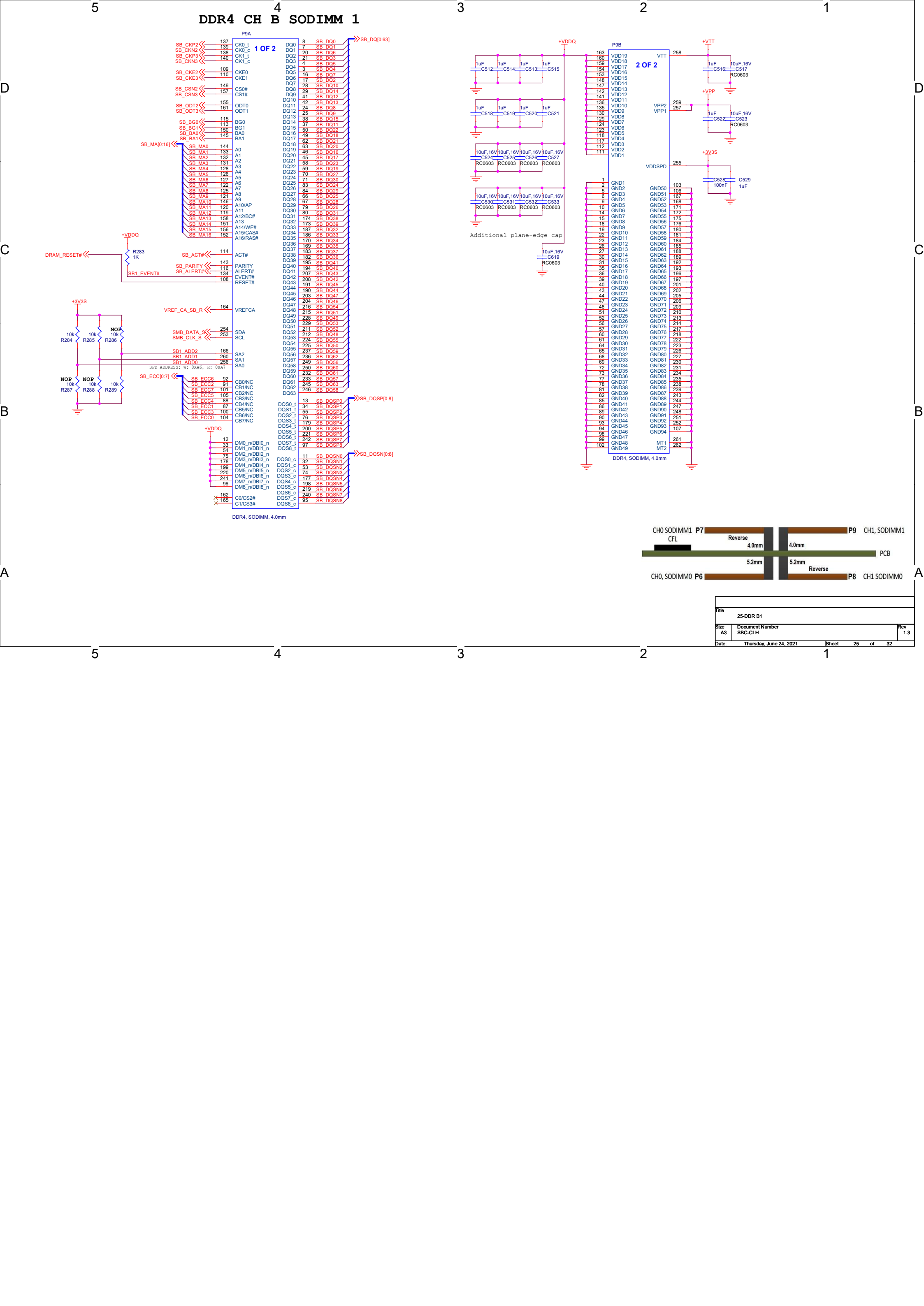


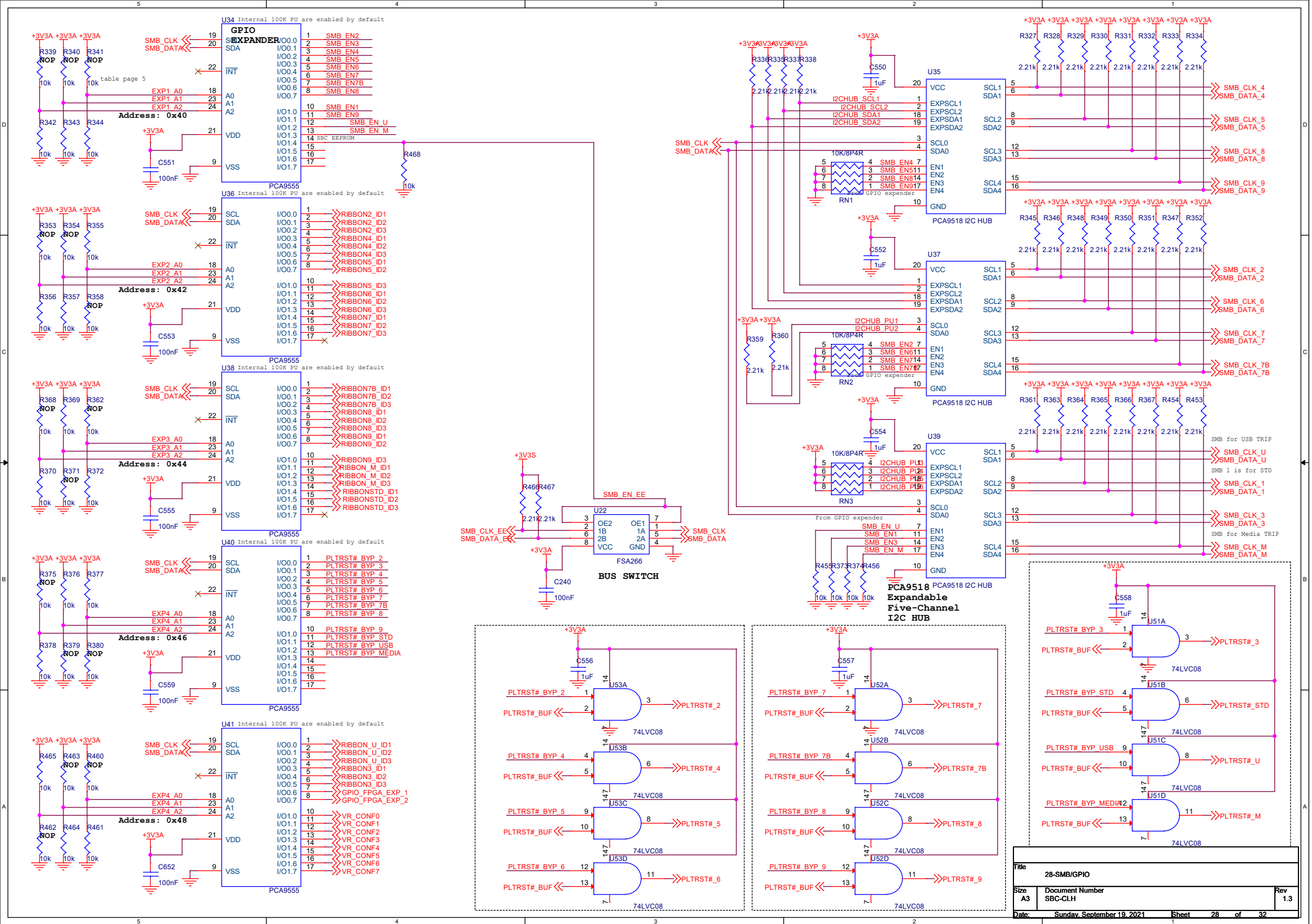
Title			
21-PWROK/PM/SV/LED			
Size	Document Number		Rev
A3	SBC-CLH		1.3
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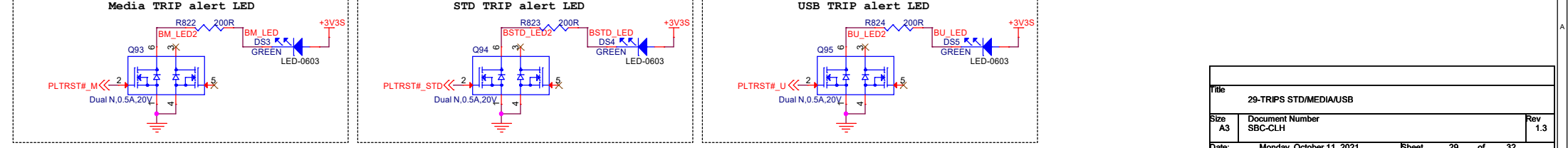
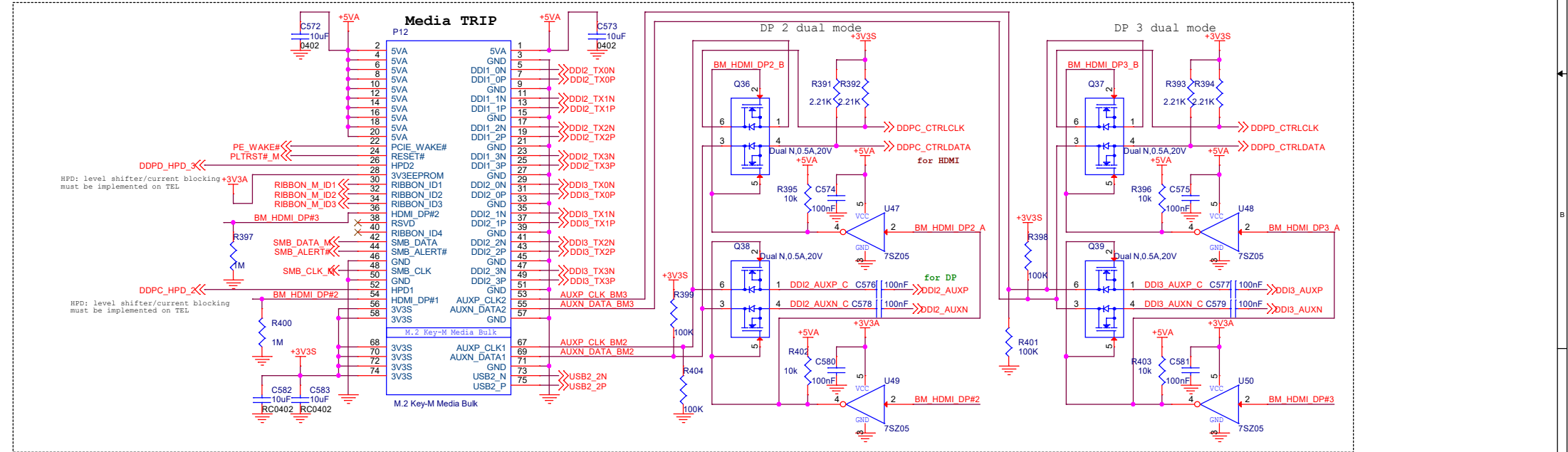
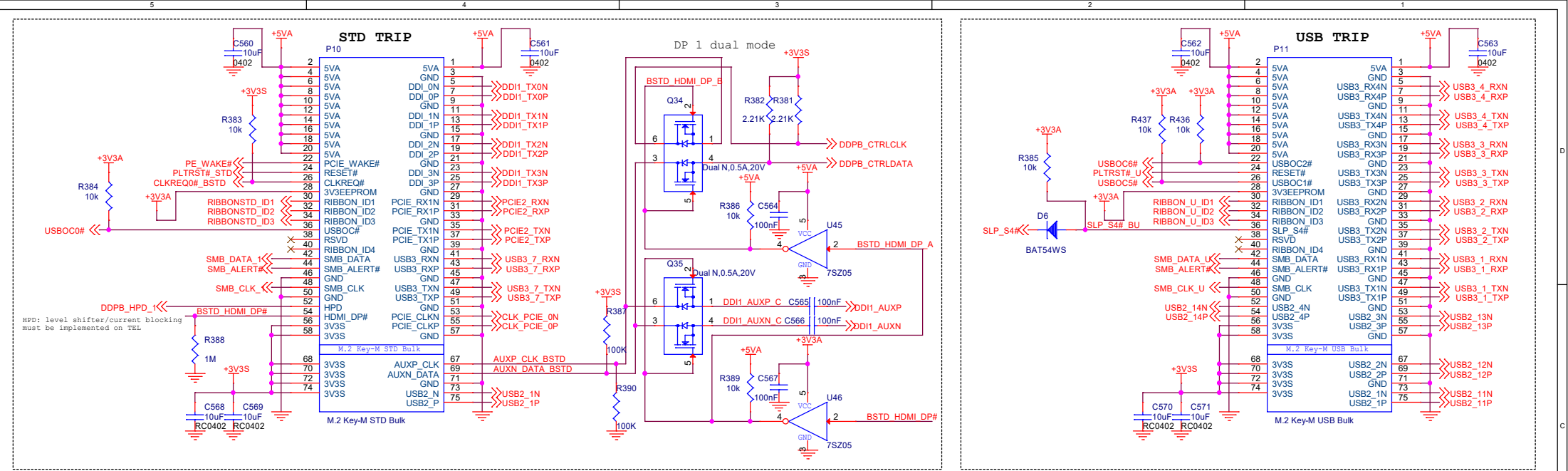




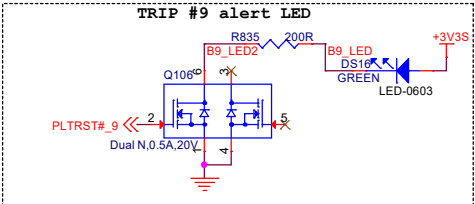
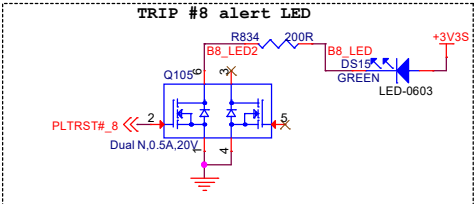
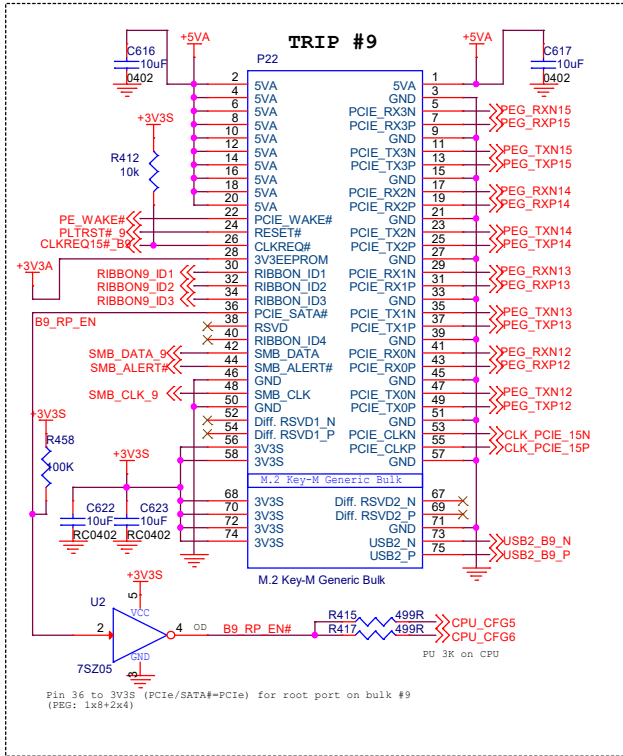
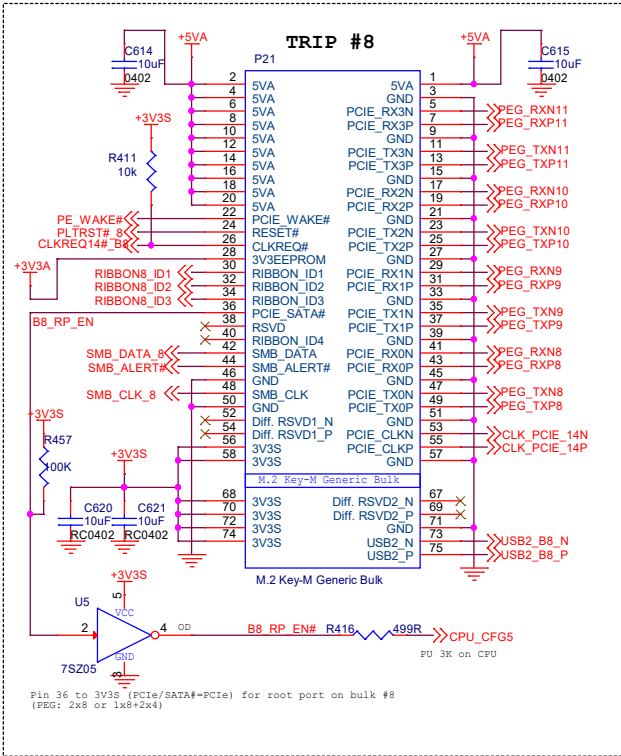
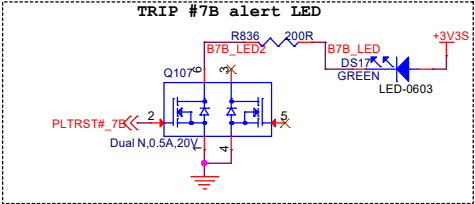
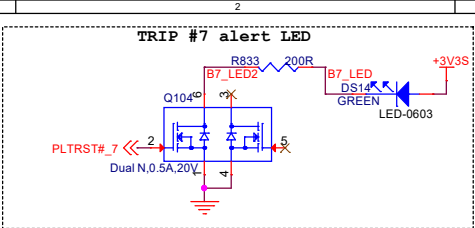
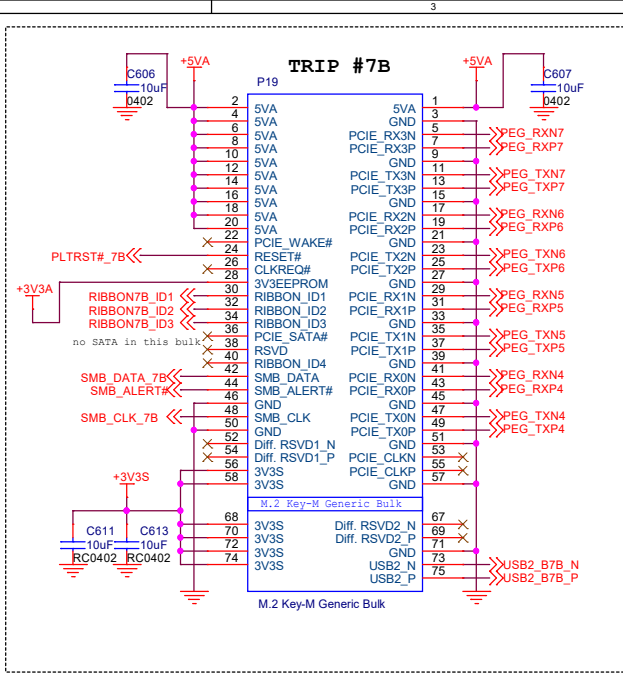
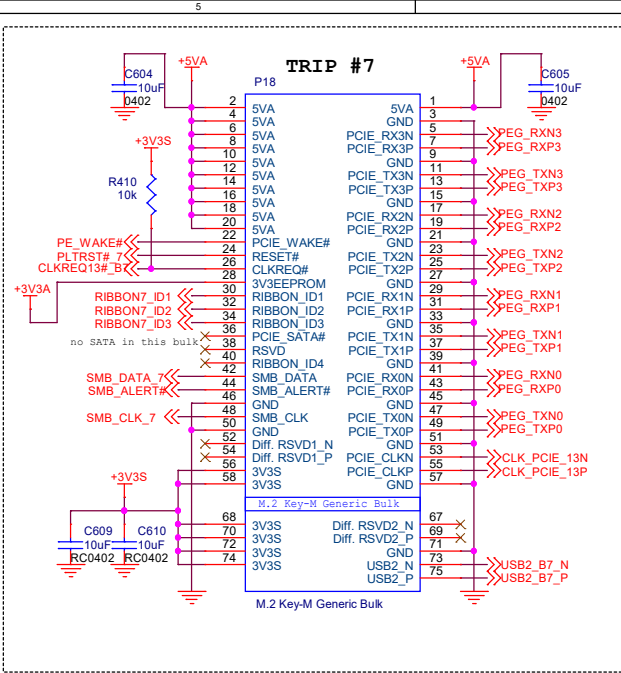




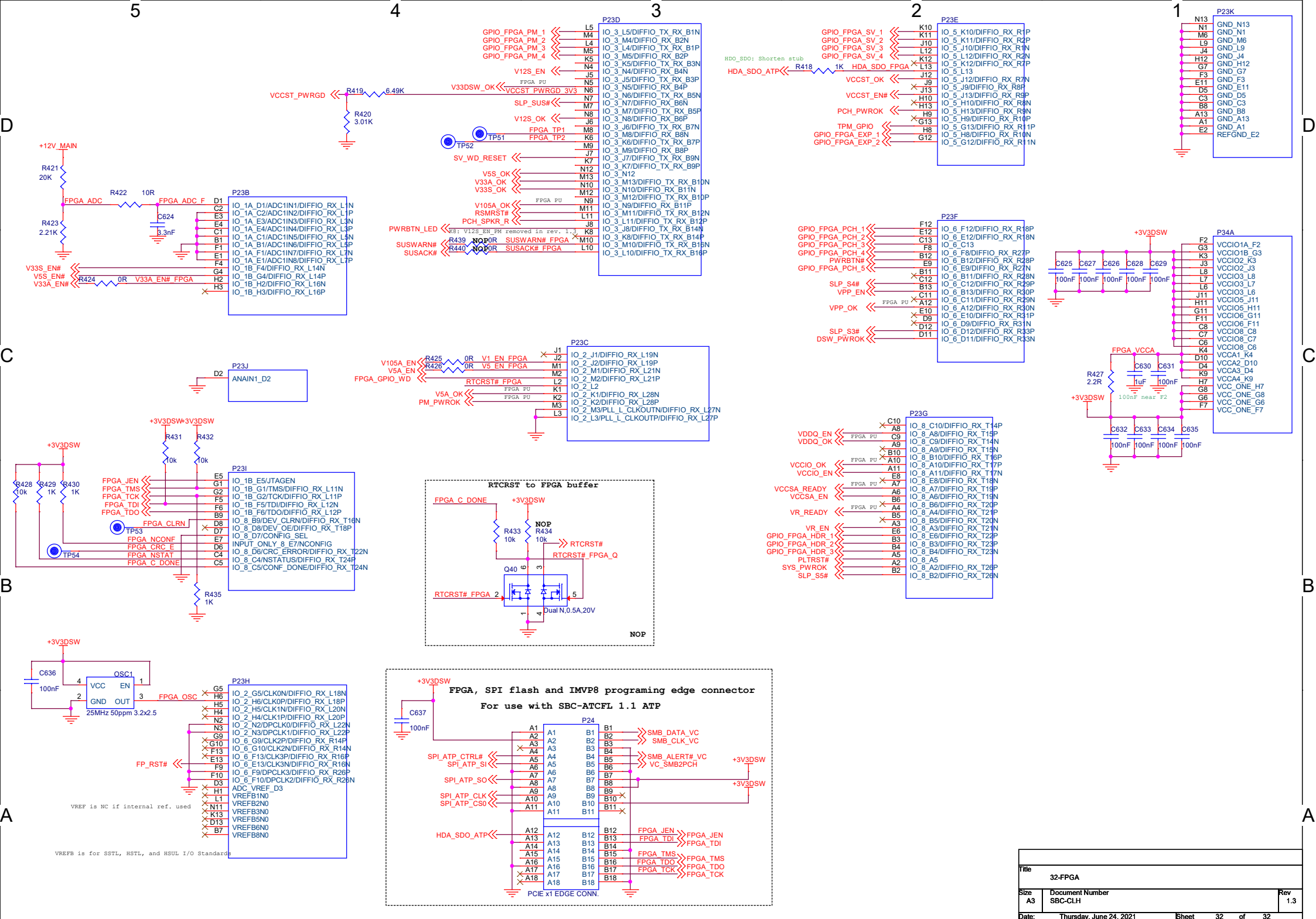




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