Back to main

Notes:

- Please **read the instruction carefully** before you start to fill-in this sheet (click the link below for more information).
- For **DDR_VPP** (TGL-UP3: Row 28 and 64; TGL-H: Row 107 and 144), **DDR_VDD2** (Row 33) and **DDR_VDDQ** (Row 34 and 61) power rails, **please use the drop-down button** to select the right voltage specification based on memory configuration.

Instruction (Click here)

Tiger Lake UP3

Power Up Sequence

SL. No		Rail Name		Net Name in SCH [Fill up by customer own design]	Voltage Check: Voltage (V)	Voltage Check: Tolerence	Voltage Check: Measurement (V)	Timing Check: Recommended Measurement Label				Timing Check: Δt,ms (~80%>~80%)	Timing Check: t,ms (@~80%)	Scope Capture
1		VCCRTC	1	+VCCPRTC_3P3	2.00 - 3.30	+5%	0.00			V3.3A_RTC	1			1
2		RTCRST#		RTC_RST_N	3.00 - 3.30	N/A	0.00			RTC_RST_N			0.00	
3		SRTCRST#		SRTC_RST_N	3.00 - 3.30	N/A	0.00			SRTC_RST_N			0.00	
4	2	VCCDSW_3P3		+VCCPDSW_3P3	3.30	5%	0.00	2	DSW_3P3			0.00	0.00	2
5		DSW_PWROK		DSW_PWROK	3.30	5%	0.00		DSW_OK			32.00	32.00	
6		SLP_SUS#		PM_SLP_SUS_N	3.30	5%	0.00		SLP_SUS			95.85	127.85	
7		V5.0A	3	+V5A	5.00	5%	0.00		V5A	V5A	3	-40.00	87.85	3
8		VCCPRIM_3P3		+VCCPRIM_3P3	3.30	5%	0.00			VCC_3P3			87.85	
9		VCCPRIM_1P8		+VCCPRIM_1P8	1.80	5%	0.00			VCC_1P8			87.85	
10	4	VCCIN_AUX		+VCCIN_AUX	1.80	-10% / +5%	0.00	4	VCCIN_AUX	VCCIN_AUX			87.85	4
11		VNN_BYPASS		+VCC_VNNEXT_1P05V	1.05	5%	0.00		VNN_BYP				87.85	
12		V1.05A_BYPASS		+VCC_V1P05EXT_1P05V	1.05	5%	0.00		V1P05_BYP				87.85	
13		RSMRST# ✓	5	PM_RSMRST_N	3.30	5%	0.00		RSMRST	RSMRST	5		87.85	5
14		PWRBTN#		PM_PWRBTN_N	3.30	5%	0.00			PWRBTN			87.85	
15	6	SLP_S5# ✓		PM_SLP_S5_N	3.30	5%	0.00	6	S5	S5			87.85	6
16		SLP_S4# ✓		PM_SLP_S4_N	3.30	5%	0.00		S4				87.85	
17		**DDR_VPP (DDR4)**		**+V1.8U_2.5U_MEM** VPP_VR_PWRGD comes 880.64 us after SLP_S3#	**2.50**	**5%**	**0.00**		**VPP (DDR4)**				87.85	
18		SLP_S3# ✓	7	PM_SLP_S3_N	3.30	5%	0.00		S3	S3	7		87.85	7
19		SLP_S0# ✓		PMSLP_S0_N	3.30	5%	0.00			S0			87.85	
20	8	CPU_C10_GATE#		CPU_C10_GATE_N	3.30	5%	0.00	8	C10	C10			87.85	8
21		VCCST (VCCST_CPU) ✓		+VCCST_CPU VCCST_EN (7.8 us after SLP_S3#)	1.025	5%	0.00		VCCST				87.85	
22		**DDR_VDD2 (DDR4)** ✓		**+VDD2_CPU**	**1.200**	**5%**	**0.00**		**VDD2 (DDR4)**				87.85	
23		**DDR_VDDQ (DDR4)**		**+VDD2_MEM** VDD2_MEM comes 1.5 ms after SLP_S3# VDD2_MEM ARRIVES 500 MS BEFORE BUF_PLT_RST_N VCCIO_VR_EN comes 880.81 us after SLP_S3#	**1.20**	**5%**	**0.00**		**VDDQ (DDR4)**	**VDDQ (DDR4)**			87.85	9
24													87.85	
25	10	ALL_SYS_PWRGD ✓		ALL_SYS_PWRGD	3.30	5%	0.00	10	ALL_SYS_PWRGD	ALL_SYS_PWRGD			87.85	10
26		VCCST_PWRGD no connection with VCCST		VCCST_PWRGD	1.05	5%	0.00		VCCST_PWRGD				87.85	
27		VTT ✓		+V_VDD2_VTT	0.60	5%	0.00		VTT				87.85	
28		PCH_PWROK ✓	11	PM_PCH_PWROK 32 ms after ALL SYS PWROK	3.30	5%	0.00		PCH_PWROK	PCH_PWROK	11		87.85	11
29		VCCIN ✓		+VCCIN VCCIN ARRIVES 522 us after BUF_PLT_RST_N vccin_en comes exactly with ALL_SYS_PWROK	1.80	±20mV	0.00			VCCIN			87.85	
30		PROCPWRGD ✓		CPUPWRGD 10 ms before PLTRST#	1.00	5%	0.00			PROCPWRGD			87.85	
31	12	VCCIO ✓		+VCCIO_OUT +VCCIO_OUT comes 9.89 ms before PLTRST#	1.05	5%	0.00	12	VCCIO	VCCIO			87.85	12
32		SYS_PWROK ✓		SYS_PWROK	3.30	5%	0.00		SYS_PWROK				87.85	
33		PLTRST# ✓		PLTRST_N	3.30	5%	0.00		PLTRST#				87.85	

VDD2_MEM ARRIVES 500 MS BEFORE BUF_PLT_RST_N

VTT ARRIVES 1200 MS BEFORE BUF_PLT_RST_N

Power Down Sequence

SL. No		Rail Name		Net Name in SCH [Fill up by customer own design]	Voltage Check: Voltage (V)	Voltage Check: Tolerence	Voltage Check: Measurement (V)	Timing Check: Measurement Label				Timing Check: Δt,ms (~80%>~80%)	Timing Check: t,ms (@~80%)	Scope Capture
1		PLTRST#	1	PLTRST_N	3.30	5%	0.00			PLTRST#	1			1
2		PROCPWRGD		CPUPWRGD	1.00	5%	0.00			PROCPWRGD			0.00	
3		SLP_S3#		PM_SLP_S3_N	3.30	5%	0.00	2	S3	S3			0.00	2
4	2	ALL_SYS_PWRGD		ALL_SYS_PWRGD	3.30	5%	0.00		ALL_SYS_PWRGD				0.00	
5		VCCST_PWRGD		VCCST_PWRGD	1.05	5%	0.00		VCCST_PWRGD				0.00	
6		PCH_PWROK	3	PM_PCH_PWROK	3.30	5%	0.00		PCH_PWROK	PCH_PWROK	3		0.00	3
7		SYS_PWROK		SYS_PWROK	3.30	5%	0.00			SYS_PWROK			0.00	
8		VCCIN		+VCCIN	1.80	±20mV	0.00			VCCIN			0.00	
9	4	VTT		+V_VDD2_VTT	0.60	5%	0.00	4	VTT	VTT			0.00	4
10		VCCSTG		+VCCSTG_CPU	1.025	5%	0.00		VCCSTG				0.00	
11		SLP_S4#		PM_SLP_S4_N	3.30	5%	0.00		S4				0.00	
12		**DDR_VDDQ (DDR4)**	5	**+VDD2_MEM**	**1.20**	**5%**	**0.00**		**DDR_VDDQ (DDR4)**	**DDR_VDDQ (DDR4)**	5		0.00	5
13		VCCST		+VCCST_CPU	1.025	5%	0.00			VCCST			0.00	
14		SLP_S5#		PM_SLP_S5_N	3.30	5%	0.00			S5			0.00	
15	6	**DDR_VPP (DDR4)**		**+V1.8U_2.5U_MEM**	**2.50**	**5%**	**0.00**	6	**DDR_VPP (DDR4)**	**DDR_VPP (DDR4)**			0.00	6
16		SLP_SUS#		PM_SLP_SUS_N	3.30	5%	0.00		SLP_SUS#				0.00	
17		DSW_PWROK	7	DSW_PWROK	3.30	5%	0.00		DSW_PWROK	DSW_PWROK	7		0.00	7
18		RSMRST#		PM_RSMRST_N	3.30	5%	0.00			RSMRST#			0.00	
19		SLP_S0#		PM_SLP_S0_N	3.30	5%	0.00			S0			0.00	
20	8	CPU_C10_GATE#		CPU_C10_GATE_N	3.30	5%	0.00	8	C10	C10			0.00	8
21		VCCDSW_3P3		+VCCPDSW_3P3	3.30	5%	0.00		VCCDSW_3P3				0.00	
22		V5.0A		+V5A	5.00	5%	0.00		V5A				0.00	
23		VCCPRIM_3P3	9	+VCCPRIM_3P3	3.30	5%	0.00		VCCPRIM_3P3	VCCPRIM_3P3	9		0.00	9
24		VCCPRIM_1P8		+VCCPRIM_1P8	1.80	5%	0.00			VCCPRIM_1P8			0.00	
25		VCC1.05_OUT_PCH		+VCC1P05_OUT_PCH	1.05	5%	0.00			VCC1P05_OUT_PCH			0.00	
26	10	VCCIN_AUX		+VCCIN_AUX	1.80	-10% / +5%	0.00	10	VCCIN_AUX	VCCIN_AUX			0.00	10
27		VNN_BYPASS		+VCC_VNNEXT_1P05V	1.05	5%	0.00		VNN_BYP				0.00	
28		V1.05A_BYPASS		+VCC_V1P05EXT_1P05V	1.05	5%	0.00		V1.05A_BYP				0.00	
29		PWRBTN#	11	PM_PWRBTN_N	3.30	5%	0.00		PWRBTN#	PWRBTN#	11		0.00	11
30		VCCRTC		+VCCPRTC_3P3	2.00 - 3.30	+5%	0.00			VCCRTC			0.00	
31		RTCRST#		RTC_RST_N	3.00 - 3.30	N/A	0.00			RTCRST#			0.00	
32		SRTCRST#		SRTC_RST_N	3.00 - 3.30	N/A	0.00			SRTCRST#			0.00	

Tiger Lake H

Power Up Sequence

SL. No		Rail Name		Net Name in SCH [Fill up by customer own design]	Voltage Check: Voltage (V)	Voltage Check: Tolerence	Voltage Check: Measurement (V)	Timing Check: Recommended Measurement Label				Timing Check: Δt,ms (~80%>~80%)	Timing Check: t,ms (@~80%)	Scope Capture
1		VCCRTC	1	+VCCPRTC_3P3	2.00 - 3.30	+5%	0.00			V3.3A_RTC	1			1
2		RTCRST#		RTC_RST_N	3.00 - 3.30	N/A	0.00			RTC_RST_N			0.00	
3		SRTCRST#		SRTC_RST_N	3.00 - 3.30	N/A	0.00			SRTC_RST_N			0.00	
4	2	VCCDSW_3P3		+VCCPDSW_3P3	3.30	5%	0.00	2	DSW_3P3				0.00	2
5		DSW_PWROK		DSW_PWROK	3.30	5%	0.00		DSW_OK				0.00	
6		SLP_SUS#		PM_SLP_SUS_N	3.30	5%	0.00		SLP_SUS				0.00	
7		V5.0A	3	+V5A	5.00	5%	0.00		V5A	V5A	3		0.00	3
8		VCCPRIM_3P3		+VCCPRIM_3P3	3.30	5%	0.00			VCC_3P3			0.00	
9		VCCPRIM_1P8		+VCCPRIM_1P8	1.80	5%	0.00			VCC_1P8			0.00	
10	4	VCCIN_AUX		+VCCIN_AUX	1.80	-5% / +10%	0.00	4	VCCIN_AUX	VCCIN_AUX			0.00	4
11		VNN_BYPASS		+VCC_VNNEXT_1P05V	1.05	5%	0.00		VNN_BYP				0.00	
12		V1.05A_BYPASS		+VCC_V1P05EXT_1P05V	1.05	5%	0.00		V1P05_BYP				0.00	
13		RSMRST#	5	PM_RSMRST_N	3.30	5%	0.00		RSMRST	RSMRST	5		0.00	5
14		PWRBTN#		PM_PWRBTN_N	3.30	5%	0.00			PWRBTN			0.00	
15	6	SLP_S5#		PM_SLP_S5_N	3.30	5%	0.00	6	S5	S5			0.00	6
16		SLP_S4#		PM_SLP_S4_N	3.30	5%	0.00		S4				0.00	
17		**DDR_VPP (DDR4)**		**+V1.8U_2.5U_MEM**	**2.50**	**5%**	**0.00**		**VPP (DDR4)**				0.00	
18		SLP_S3#	7	PM_SLP_S3_N	3.30	5%	0.00		S3	S3	7		0.00	7
19		SLP_S0#		PMSLP_S0_N	3.30	5%	0.00			S0			0.00	
20	8	CPU_C10_GATE#		CPU_C10_GATE_N	3.30	5%	0.00	8	C10	C10			0.00	8
21		VCCST		+VCCST_CPU	1.065	5%	0.00		VCCST				0.00	
22		DDR_VDD2		+VDD2_CPU	1.20	5%	0.00		VDD2				0.00	
23		DDR_VDDQ	9	+VDD2_MEM	1.20	5%	0.00		VDDQ	VDDQ	9		0.00	9
24		VCCSTG		+VCCSTG_CPU	1.065	5%	0.00			VCCSTG			0.00	
25	10	VCC1P8A		+VCC1P8A	1.80	5%	0.00	10	VCC1P8A	VCC1P8A			0.00	10
26		ALL_SYS_PWRGD		ALL_SYS_PWRGD	3.30	5%	0.00		ALL_SYS_PWRGD				0.00	
27		VCCST_PWRGD		VCCST_PWRGD	1.05	5%	0.00		VCCST_PWRGD				0.00	
28		VTT	11	+V_VDD2_VTT	0.60	5%	0.00		VTT	VTT	11		0.00	11
29		PCH_PWROK		PM_PCH_PWROK	3.30	5%	0.00			PCH_PWROK			0.00	
30		VCCIN		+VCCIN	1.80	±20mV	0.00			VCCIN			0.00	
31	12	PROCPWRGD		CPUPWRGD	1.00	5%	0.00	12	PROCPWRGD	PROCPWRGD			0.00	12
32		VCCIO		+VCCIO_OUT	1.05	5%	0.00		VCCIO				0.00	

33	12	SYS_PWROK		SYS_PWROK	3.30	5%	0.00	12	SYS_PWROK				0.00	
34		PLTRST#		PLTRST_N	3.30	5%	0.00		PLTRST#				0.00	

Power Down Sequence

					Voltage Check			Timing Check						
SL. No		Rail Name		Net Name in SCH [Fill up by customer own design]	Voltage (V)	Tolerence	Measurement (V)		Measurement Label			Δt,ms (~80%>~80%)	t,ms (@~80%)	Scope Capture
1		PLTRST#		PLTRST_N	3.30	5%	0.00			PLTRST#				1
2		PROCPWRGD	1	CPUPWRGD	1.00	5%	0.00			PROCPWRGD	1		0.00	
3	2	SLP_S3#		PM_SLP_S3_N	3.30	5%	0.00	2	S3	S3			0.00	2
4		VCCSTG		+VCCSTG_CPU	1.065	5%	0.00		VCCSTG				0.00	
5		ALL_SYS_PWRGD		ALL_SYS_PWRGD	3.30	5%	0.00		ALL_SYS_PWRGD				0.00	
6		VCCST_PWRGD	3	VCCST_PWRGD	1.05	5%	0.00		VCCST_PWRGD	VCCST_PWRGD	3		0.00	3
7		PCH_PWROK		PM_PCH_PWROK	3.30	5%	0.00			PCH_PWROK			0.00	
8		SYS_PWROK		SYS_PWROK	3.30	5%	0.00			SYS_PWROK			0.00	
9	4	VCCIN		+VCCIN	1.80	±20mV	0.00	4	VCCIN	VCCIN			0.00	4
10		VTT		+V_VDD2_VTT	0.60	5%	0.00		VTT				0.00	
11		VCCST		+VCCST_CPU	1.065	5%	0.00		VCCST				0.00	
12		SLP_S4#		PM_SLP_S4_N	3.30	5%	0.00		S4	S4			0.00	5
13		DDR_VDDQ	5	+VDD2_MEM	1.20	5%	0.00			DDR_VDDQ	5		0.00	
14		SLP_S5#		PM_SLP_S5_N	3.30	5%	0.00			S5			0.00	
15	6	**DDR_VPP (DDR4)**		**+V1.8U_2.5U_MEM**	**2.50**	**5%**	**0.00**	6	**DDR_VPP (DDR4)**	**DDR_VPP (DDR4)**			0.00	6
16		SLP_SUS#		PM_SLP_SUS_N	3.30	5%	0.00		SLP_SUS#				0.00	
17		DSW_PWROK		DSW_PWROK	3.30	5%	0.00		DSW_PWROK	DSW_PWROK			0.00	7
18		RSMRST#	7	PM_RSMRST_N	3.30	5%	0.00			RSMRST#	7		0.00	
19		SLP_S0#		PM_SLP_S0_N	3.30	5%	0.00			S0			0.00	
20	8	CPU_C10_GATE#		CPU_C10_GATE_N	3.30	5%	0.00	8	C10	C10			0.00	8
21		VCCDSW_3P3		+VCCPDSW_3P3	3.30	5%	0.00		VCCDSW_3P3				0.00	
22		V5.0A		+V5A	5.00	5%	0.00		V5A				0.00	
23		VCCPRIM_3P3		+VCCPRIM_3P3	3.30	5%	0.00		VCCPRIM_3P3	VCCPRIM_3P3			0.00	9
24		VCCPRIM_1P8	9	+VCCPRIM_1P8	1.80	5%	0.00			VCCPRIM_1P8	9		0.00	
25		VCC1.05_OUT_PCH		+VCC1P05_OUT_PCH	1.05	5%	0.00			VCC1P05_OUT_PCH			0.00	
26	10	VCCIN_AUX		+VCCIN_AUX	1.80	-5% / +10%	0.00	10	VCCIN_AUX	VCCIN_AUX			0.00	10
27		VNN_BYPASS		+VCC_VNNEXT_1P05V	1.05	5%	0.00		VNN_BYP				0.00	
28		V1.05A_BYPASS		+VCC_V1P05EXT_1P05V	1.05	5%	0.00		V1.05A_BYP				0.00	
29		PWRBTN#		PM_PWRBTN_N	3.30	5%	0.00		PWRBTN#	PWRBTN#			0.00	11
30		VCCRTC	11	+VCCPRTC_3P3	2.00 - 3.30	+5%	0.00			VCCRTC	11		0.00	
31		RTCRST#		RTC_RST_N	3.00 - 3.30	N/A	0.00			RTCRST#			0.00	
32		SRTCRST#		SRTC_RST_N	3.00 - 3.30	N/A	0.00			SRTCRST#			0.00	