# Coffee Lake H Platform

## Design Guide

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# Revision History

| Document Number | Revision Number | Description | Revision Date |
|---|---|---|---|
| 571391 | 0.5 | • Initial Release | January 2017 |
| 571391 | 0.7 | Chapter 11, "Hybrid Graphics"<br>• Switchable Graphic was removed. Hybrid Graphics content was added.<br>Chapter 16, "PCH PCI Express* Interface Design Guidelines"<br>• Replaced Break-In Max Length segment terminology with Post-AC Capacitor Max Length segment<br>• Correct AC Cap comment in RCOMP section with the correct term Series Resistor<br>Chapter 17, "SATA Interface Guidelines"<br>• Replaced "Breakin Max length" changed to "post-AC capacitor main route length" in topology tables<br>Chapter 20, "USB Type-C"<br>• Updated the diagrams from figures Figure 20-14 to Figure 20-19.<br>• Added general design guidelines in the 'Notes' section at the end of the Section 20.3.2.<br>• Deleted the OC protection diagram, GPIO mapping table, Debug Alternate Mode sub-section and EC-less USB-C sub-section.<br>• Added Figure 20-9 in USB2 sub-section containing component restrictions.<br>• Added reference documents and links in the last sub-section 19.3.10<br>• Updated the platform block diagram in Figure 20-1.<br>• Corrected the mils to mm typo in USB2 DG Table 20-3.<br>Chapter 22, "MIPI SoundWire* Interface Design Guidelines"<br>• In Table 22-2<br>— Updated M-Cable reference in<br>— Updated supported operating frequency to show 6MHz<br>— Added note 2<br>• In Table 22-3<br>— Updated supported operating frequency to show 6MHz<br>— Added note 7<br>• In Table 22-4<br>— Updated supported operating frequency to show 6MHz<br>— Added note 2<br>Chapter 23, "I2C* Interface Design Guidelines"<br>• Updated Section 23.1.2.1, "General Design Considerations"<br>• Updated Table 23-4, "Bus Capacitance Reference Chart":<br>• Updated Table 23-5, "Bus Capacitance / Pull-Up and Current Assist Strength Settings"<br>Chapter 27, "SMBus 2.0/SMLink Interface Design Guidelines"<br>• External Pull-up required for the SMBus and SMLink interfaces<br>Chapter 28, "Secure Digital Card with Extended Capacity (SDXC) Interface Design Guidelines"<br>• Removed SD_VDD2_PWR_EN# signal which is not used<br>• External Pull-up resistor not required on SD_DATA; CLK and CMD.<br>• Updated Figure 28-1, "SDXC Topology" | May 2017 |

| Document Number | Revision Number | Description | Revision Date |
|---|---|---|---|
| 571391 | 0.7 | Chapter 32, "Legacy Audio Interface Design Guidelines"<br>• Corrected trademarks<br>• Added the Embedded Display Audio Interface line to the legacy audio list prior to Section 32.1<br>• Corrected C1 placement in Figure 32-2.<br>• Added note 4 and 5 in Table 32-2.<br>• Added note 5 to Table 32-3.<br>• Updated Figure 32-3 to remove DMIC name as Figure 29-4 is specifically for DMIC.<br>• Updated Table 32-4 and Table 32-5.<br>• Added max length for B0 + M1 Table 32-6.<br>• Simplified Figure 32-4 and Figure 32-5 removing M2 and BI.<br>• Minor adjustments to grammar and readability<br>Chapter 49, "Electromagnetic Compatibility"<br>• Removed CPU/PCH Noise in Section 49.3, "Critical Signals"<br>• Updated Section 49.3.4, "Crystal (Xtal) RF Immunity"<br>Chapter 50, "Processor and PCH Power Integrity Recommendations"<br>• Updated Table 49-3<br>Chapter 52, "Power Delivery"<br>• Power Map excel sheet - part of PDG zip file<br>• Section 52.3<br>• Table 52-2, Table 52-3, and Table 52-4 | May 2017 |
| 571391 | 0.71 | Chapter 4, "System Memory Interface Design Guidelines"<br>•Removed Section 4.5 MD 1Rx16 double-T.<br>•Added Section 4.8, "CFL H DDR4 Mixed SODIMM and MemoryDown x8 Daisy-Chain Topology"<br>•Added Section 4.8, "CFL H DDR4 Mixed SODIMM and MemoryDown x8 Daisy-Chain Topology" | May 2017 |
| 571391 | 1.0 | Chapter 2, "Stack-Up and PCB Considerations"<br>• TMDG document number updated in Table 2-1<br>Chapter 4, "System Memory Interface Design Guidelines"<br>• Table 4-1, Table 4-7, Table 4-9, Table 4-10, Table 4-13, Table 4-16, Table 4-17 - The speed bin increased to 2666 MT/s<br>Chapter 19, "Universal Serial Bus 2.0 Design Guidelines"<br>• CFL H PCH or CFL-S PCH changed to CNP PCH-H.<br>• Topology diagrams are cleaned.<br>• ESD diode recommendation is added in Flex and Docking Topology.<br>Chapter 22, "MIPI SoundWire* Interface Design Guidelines"<br>• Updated Table 22-3 with Resistor minimum and Maximum distance<br>Chapter 42, "Wireless Connectivity Integration (CNVi) Design Considerations"<br>• Requirements for a slow clock (32 KHz) removed from Section 42.3.1.5<br>• Additional note on reference planes added in Section 42.5.1<br>• Cosmetic corrections applied to CNVio Device Down Topology Values table.<br>• Updated Section 42.5.5.1 with separate topology diagrams and routing guidelines table for DT and RSP signals.<br>• Figure 42-8, Figure 42-9 updated with external pull-up resistor of 20K Ohm in the block diagrams.<br>• Table 42-6 - the XTAL_SEL2 description is updated with 20K Ohm pull-up resistor details. | August 2017 |

| Document Number | Revision Number | Description | Revision Date |
|---|---|---|---|
| 571391 | 1.5 | Chapter 2, "Stack-Up and PCB Considerations"<br>• Updated Table 2-9 to Table 2-13<br>Chapter 3, "General Differential Design Guidelines"<br>• Updated Figure 3-32<br>Chapter 4, "System Memory Interface Design Guidelines"<br>• Table 4-1 - 2666 is now supported for DDP x16<br>• Table 4-10 - Both SDP and DDP supports 2666 MT/s<br>• Table 4-11 - RCOMP[0] value fixed<br>Chapter 9, "Direct Media Interface Design Guidelines"<br>• Added Notes in Table 9-1 and Table 9-2<br>Chapter 30, "Serial Peripheral Interface (SPI0) Flash Design Guidelines"<br>• Added Note in Section 30.2.1 and Section 30.2.3<br>Chapter 32, "Legacy Audio Interface Design Guidelines"<br>• Updated Table 32-2, Table 32-3, and Table 32-6 table notes and references<br>• Updated Table 32-3 PCH Buffer values<br>• Added details on Table 32-3 to clarify use of RS2 and RS3 for DMIC usage<br>Chapter 45, "Platform Power Sequencing Specification"<br>• Updated tPLT15/tCPU21 and added tPLT20 | January 2018 |
| 571391 | 1.8 | Chapter 2, "Stack-Up and PCB Considerations"<br>• Updated CFL Signal Integrity Tool Suite Document number<br>Chapter 20, "USB Type-C"<br>• Updated Figure 20-6 and Figure 20-7<br>Chapter 21, "PCH Signal Glitch Free Implementation Requirements"•<br>• Updated Table 21-3<br>Chapter 42, "Wireless Connectivity Integration (CNVi) Design Considerations"<br>• Updated Figure 42-19<br>• Updated CFL Signal Integrity Tool Suite Document number<br>Chapter 50, "Processor and PCH Power Integrity Recommendations"<br>• Added Table 50-5<br>Chapter 51, "Power Delivery"<br>• Updated Table 51-7<br>Added Chapter 52, "Flexible Instrumented Platform (FIP) Design" | May 2018 |
| 571391 | 2.0 | Chapter 45, "Platform Power Sequencing Specification"<br>• Table 45-5<br>— Updated tPCH01 description<br>— Added notes - 47 and 48<br>Chapter 50, "Processor and PCH Power Integrity Recommendations"<br>• Added Figure 50-2 | October 2019 |
| 571391 | 2.1 | Chapter 4, "System Memory Interface Design Guidelines"<br>• Table 4-1 - Updated frequency of SODIMM 2DPC/1DPC with/ without ECC topology | August 2020 |
| 571391 | 2.2 | Chapter 23, "I2C* Interface Design Guidelines"<br>• Updated section 23.1.2.1 General Design Considerations<br>• Updated table 23-5. Bus Capacitance / Pull-Up and Current Assist Strength Settings | September 2020 |
| 571391 | 2.3 | Chapter 9, "Direct Media Interface Design Guidelines"<br>• Added Table 9-2 | December 2020 |

# 1 Introduction

This Design Guide provides motherboard implementation recommendations for the Coffee Lake platform, based on the Coffee Lake processor. This document includes design guides for platforms.

The Coffee Lake platform consists of CFL H 2-Chip Platform Series and CFL S 2-Chip Platform Series. Cannon Lake PCH, also known as CNP PCH, refers to the PCH portion of the Coffee Lake platform. The Coffee Lake H and S 2-Chip platform consists of CFL processor package with Cannon Lake PCH package.

CFL H will be based out of CNP PCH H.

CNP PCH-H can be paired with CFL S CPU

***Note:*** For CFL platform PCH sku details, refer to *Cannon Lake Platform Controller Hub-H (PCH-H) – External Design Specification (EDS)* (# 566439).

***Note:*** For Mehlow Server Platform Design Guide (PDG), refer to (# 571518).

The Coffee Lake Platform Design Guide has been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. Design recommendations are based on Intel's simulations and lab experience and are strongly recommended, if not necessary, to meet the timing and signal quality specifications. Design recommendations are based on the reference platforms designed by Intel. They should be used as an example but may not be applicable to particular designs.

The guidelines recommended in this document are based on experience, simulation, and preliminary validation work done at Intel while developing the Coffee Lake processor-based platform. This work is ongoing, and these recommendations are subject to change. Metric units are used in some sections in addition to the standard use of U.S. customary system of units (USCS). If there is a discrepancy between the metric and USCS units, assume the USCS unit is most accurate. The conversion factor used is 1 inch (1000 mils) = 25.4 mm.

## Figure 1-1. Coffee Lake H Platform Block Diagram

***Notes:***
1. For further information on total number of ports for USB 3.0, PCIe 2.0, SATA 3.0, refer Chapter 14, "Flexible I/O"
2. GbE programmable on PCIe ports 3, 4 or 5.
3. PCIe Ports 5 and 6 can be configured up to x4.

## Table 1-1. CFL H Platform Windows* OS Support

| H | OS Support |
|---|---|
| **OS POR** | Windows* 10 |
| **Consumer (ME 1.5M)** | Yes |
| **Corporate (ME 5M)** | Yes |

## 1.1 Terminology

| Term | Description |
|---|---|
| AOAC | Always On, Always Connected |
| DPTF | Dynamic Platform and Thermal Framework; includes configurable TDP and Low Power Mode. |
| DPPM | Dynamic Power Performance Management |
| MCP | Multi-Chip Package. A single package with multiple dies (processor and PCH) with interconnects between them, which fits into a single socket. |

## 1.2 Reference Documents

| Document | Document Number |
|---|---|
| Coffee Lake Processor Families External Design Specification Volume 1 of 2 | 570805 |
| Coffee Lake Processor Families External Design Specification Volume 2 of 2 | 570806 |
| Coffee Lake Processor High Speed Interface Spice models | 570865 |
| Coffee Lake H Processor Line BGA Package Ballout Mechanical Specification | 570699 |
| Coffee Lake Turbo and Thermal Power Management Guide for Intel Core-based Processors | 571040 |
| Coffee Lake Platform Mobile Thermal and Mechanical Design Guide | 571296 |

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# 2 Stack-Up and PCB Considerations

If the guidelines are not followed, complete signal integrity and timing simulations for each design is required. If the guidelines are followed, simulate critical signals to ensure proper signal integrity and flight timing.

Refer to *Coffee Lake Platform Mobile Thermal Mechanical Design Guide (TMDG)* for thermal and mechanical design guidelines, such as component PCB pad design recommendations and NCTF corner ball routing guidelines.

***Note:*** Metric units are used in some sections in addition to the standard use of U.S. customary system of units (USCS). If there is a discrepancy between the metric and USCS units, assume the USCS unit is most accurate. The conversion factor used is 1 inch (1000 mils) = 25.4 mm.

**Table 2-1. Stack-Up and PCB Considerations Reference Documents**

| Title | Location / Document Number |
|---|---|
| *Coffee Lake Platform Mobile Thermal Mechanical Design Guide* | *566757* |

## 2.1 Printed Circuit Board Considerations

Several layer count configurations may be implemented on the platform, provided the trace geometries of the individual microstrip and stripline routing layers fall within the parameter value ranges and the impedance specifications are met. It is important to note that variations in the stack-up of a motherboard, such as changes in the dielectric height, trace widths, and spacing, can impact the impedance, loss, and jitter characteristics of all the interfaces. Such changes may either be intentional or the result of variations encountered during the PCB manufacturing process. In either case, they must be properly considered when designing interconnects.

The following diagrams and tables depict the typical values and tolerances Intel assumes for microstrip, stripline, and dual-stripline routing layers for single-ended and differential signals.

- Design tolerances account for adjustments intentionally included in their design.
- Material tolerances account for any natural variation in the materials being used.
- Manufacturing tolerance considers variations that may occur during the manufacturing process.
- Use the design tolerance to re-center stack-up impedance, but consider the manufacturing tolerance impact when comparing the chosen stack-up to the given recommendation.

The following general stack-up recommendations should be followed:

- For power and ground planes, it is preferred to use 1 oz. copper where possible.

- All high-speed signals should reference solid planes over the length of their routing and should not cross plane splits. Ground referencing is preferred.
- Reference plane stitching vias must be used in conjunction with high-speed signal layer transitions that include a reference plane change. Refer to each signal group section for more specification.
- High-speed routing on external layers should be minimized to avoid the possibility of EMI. Routing on external layers also introduces different delays compared to internal layers. In general, interfaces that have length matching requirements also restrict routing for groups of signals to be on the same layer to avoid this situation.
- The parameter values for internal and external traces are the final thickness and width.
- Signals must not be routed directly under the processor cavity without at least one solid metal plane above it. Without a "shield" there could be excessive noise coupling from the package to the signal layer. This a requirement for all motherboards.

**Figure 2-1. Single-Ended Microstrip Diagram**

**Figure 2-2. Differential-Microstrip Diagram**

## Table 2-2. CFL H Type 3 PCB Stack-Up Parameter Values (Microstrip)

| Microstrip | Units | Min Value | Negative Manufac-turing Tolerance | Negative Design/ Material Tolerance | Typical Value | Positive Design/ Material Tolerance | Positive Manufac-turing Tolerance | Max Value |
|---|---|---|---|---|---|---|---|---|
| D1 | mils | 2 | 0.3 | 0.4 | 2.7 | 0.2 | 0.3 | 3.2 |
| D2 | mils | 0.1 | 0.3 | 0.25 | 0.65 | 0.25 | 0.30 | 1.20 |
| $\varepsilon_{r1}$ | NA | 3.45 | 0.15 | 0.3 | 3.9 | 0.3 | 0.15 | 4.35 |
| $\varepsilon_{r2}$ | NA | 3.20 | 0.2 | 0 | 3.40 | 0 | 0.2 | 3.60 |
| Trace Thickness (½ oz. Plated) | mils | 1.3 | 0.28 | 0.32 | 1.9 | 0.32 | 0.28 | 2.5 |
| Trace Width Top = Trace Width Bottom - 1mil<br>Refer to Figure 2-1 and Figure 2-2<br>EDW=0.5 | | | | | | | | |

## Table 2-3. CFL H Type 4 PCB Stack-Up Parameter Values (Microstrip)

| Microstrip | Units | Min Value | Negative Manufac-turing Tolerance | Negative Design/ Material Tolerance | Typical Value | Positive Design/ Material Tolerance | Positive Manufac-turing Tolerance | Max Value |
|---|---|---|---|---|---|---|---|---|
| D1 | mils | 1.8 | 0.3 | 0.4 | 2.5 | 0.2 | 0.3 | 3.0 |
| D2 | mils | 0.1 | 0.3 | 0.25 | 0.65 | 0.25 | 0.30 | 1.20 |
| $\varepsilon_{r1}$ | NA | 3.45 | 0.15 | 0.3 | 3.9 | 0.3 | 0.15 | 4.35 |
| $\varepsilon_{r2}$ | NA | 3.20 | 0.2 | 0 | 3.40 | 0 | 0.2 | 3.60 |
| Trace Thickness (1/2 oz. Plated) | mils | 0.8 | 0.28 | 0.32 | 1.4 | 0.32 | 0.28 | 2.0 |
| Trace Width Top = Trace Width Bottom - 1mil<br>Refer to Figure 2-1 and Figure 2-2<br>EDW=0.5 | | | | | | | | |

## Table 2-4. CFL H Type 3 PCB Stack-Up Parameter Values (Dual-Stripline)

| 8-layer/10-layer Dual-Stripline | Units | Min Value | Negative Manufac-turing Tolerance | Negative Design/ Material Tolerance | Typical Value | Positive Design/ Material Tolerance | Positive Manufac-turing Tolerance | Max Value |
|---|---|---|---|---|---|---|---|---|
| D1 | mils | 3.375 | 0.375 | 0.25 | 4.00 | 0.35 | 0.375 | 4.725 |
| D2 | mils | 4.375 | 0.375 | 0.25 | 5.00 | 0.35 | 0.375 | 5.725 |
| D3 | mils | 3.375 | 0.375 | 0.25 | 4.00 | 0.35 | 0.375 | 4.725 |
| $\varepsilon_{r1}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| $\varepsilon_{r2}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| $\varepsilon_{r3}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| Trace Thickness (1/2 oz plated) | mils | 0.50 | 0.05 | 0.05 | 0.60 | 0.05 | 0.05 | 0.70 |
| Refer to Figure 2-3 and Figure 2-4.<br>EDW=0 | | | | | | | | |

## Table 2-5. CFL H Type 4 PCB Stack-Up Parameter Values (2 x 2+ 1 Oz Dual-Stripline)

| 8-layer/10-layer Dual-Stripline | Units | Min Value | Negative Manufac-turing Tolerance | Negative Design/ Material Tolerance | Typical Value | Positive Design/ Material Tolerance | Positive Manufac-turing Tolerance | Max Value |
|---|---|---|---|---|---|---|---|---|
| D1 | mils | 2.375 | 0.375 | 0.25 | 3.00 | 0.35 | 0.375 | 3.725 |
| D2 | mils | 1.875 | 0.375 | 0.25 | 2.50 | 0.35 | 0.375 | 3.225 |
| D3 | mils | 1.875 | 0.375 | 0.25 | 2.50 | 0.35 | 0.375 | 3.225 |
| $\varepsilon_{r1}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| $\varepsilon_{r2}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| $\varepsilon_{r3}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| Trace Thickness (1/3 oz plated) | mils | 0.6 | 0.28 | 0.32 | 1.20 | 0.32 | 0.28 | 1.8 |
| Refer to Figure 2-3 and Figure 2-4.<br>EDW=0.25 | | | | | | | | |

***Note:*** Dual stripline of L3/L4 and L7/L8 has dielectric thickness of 2.5 mils, signal parallelism should be avoided to eliminate potential crosstalk between L3/L4 and L7/L8.

## Table 2-6. CFL H Type 4 PCB Stack-Up Parameter Values for (2 x 2+ 0.5 Oz Dual-Stripline)

| 8-layer/10-layer Dual-Stripline | Units | Min Value | Negative Manufac-turing Tolerance | Negative Design/ Material Tolerance | Typical Value | Positive Design/ Material Tolerance | Positive Manufac-turing Tolerance | Max Value |
|---|---|---|---|---|---|---|---|---|
| D1 | mils | 1.875 | 0.375 | 0.25 | 2.50 | 0.35 | 0.375 | 3.225 |
| D2 | mils | 1.875 | 0.375 | 0.25 | 2.50 | 0.35 | 0.375 | 3.225 |
| D3 | mils | 2.375 | 0.375 | 0.25 | 3.00 | 0.35 | 0.375 | 3.725 |
| $\varepsilon_{r1}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| $\varepsilon_{r2}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| $\varepsilon_{r3}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| Trace Thickness (1/3 oz plated) | mils | 0.5 | 0.05 | 0.50 | 0.60 | 0.050 | 0.050 | 0.70 |
| Refer to Figure 2-3 and Figure 2-4.<br>EDW=0 | | | | | | | | |

**Figure 2-3. Single-Ended Dual-Stripline Diagram**

**Figure 2-4. Differential Dual-Stripline Diagram**

**Figure 2-5. Single-Ended Stripline Diagram**

### Figure 2-6. Differential Stripline Diagram

### Table 2-7. CFL H Type 4 PCB Stack-Up Parameter Values (Stripline 1-x-1/1-x-1+)

| Stripline | Units | Min Value | Negative Manufac-turing Tolerance | Negative Design/ Material Tolerance | Typical Value | Positive Design/ Material Tolerance | Positive Manufac-turing Tolerance | Max Value |
|---|---|---|---|---|---|---|---|---|
| D1 | mils | 3.375 | 0.375 | 0.25 | 4 | 0.35 | 0.375 | 4.725 |
| D2 | mils | 4.375 | 0.375 | 0.25 | 5.0 | 0.35 | 0.375 | 5.725 |
| $\varepsilon_{r1}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| $\varepsilon_{r2}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| Trace Thickness (0.5 oz Plated) | mils | 0.5 | 0.05 | 0.05 | 0.6 | 0.05 | 0.05 | 0.7 |
| Refer to Figure 2-5 and Figure 2-6. EDW=0 | | | | | | | | |

### Table 2-8. CFL H Type 3 PCB Stack-Up Parameter Values (Stripline 8/10 Layer)

| Stripline | Units | Min Value | Negative Manufac-turing Tolerance | Negative Design/ Material Tolerance | Typical Value | Positive Design/ Material Tolerance | Positive Manufac-turing Tolerance | Max Value |
|---|---|---|---|---|---|---|---|---|
| D1 | mils | 3.375 | 0.375 | 0.25 | 4.0 | 0.35 | 0.375 | 4.725 |
| D2 | mils | 4.375 | 0.375 | 0.25 | 5.0 | 0.35 | 0.375 | 5.725 |
| $\varepsilon_{r1}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| $\varepsilon_{r2}$ | NA | 3.70 | 0.15 | 0.275 | 4.125 | 0.275 | 0.15 | 4.55 |
| Trace Thickness (1/2 oz Plated) | mils | 0.5 | 0.05 | 0.05 | 0.6 | 0.05 | 0.05 | 0.7 |
| Refer to Figure 2-5 and Figure 2-6. EDW=0 | | | | | | | | |

## 2.2 Generalized 8-Layer Motherboard Example

An example of a typical 8-layer type 3 PCB stack-up with stripline routing is shown in Figure 2-8. An example of a typical 8-layer type 3 PCB stack-up with dual-stripline routing is shown in Figure 2-7. These sample stack-ups are provided as a reference only.

**Figure 2-7. CFL H Dual-Stripline 8-Layer Type 3 PCB Stack-Up**

| Type-3 8-Layer | Thickness (mils) | Thickness (um) |
|---|---|---|
| Top Surface | 0.65 | 16.51 |
| Layer 1 - Signal | 1.90 | 48.26 |
| Prepreg | 2.70 | 68.58 |
| Layer 2 - GND | 1.20 | 30.48 |
| Core | 4.00 | 101.60 |
| Layer 3 - Signal | 0.60 | 15.24 |
| Prepreg | 5.00 | 127.00 |
| Layer 4 - Signal | 0.60 | 15.24 |
| Core | 4.00 | 101.60 |
| Layer 5 - GND/PWR | 1.20 | 30.48 |
| Prepreg | 5.00 | 127.00 |
| Layer 6 - Signal | 0.60 | 15.24 |
| Core | 4.00 | 101.60 |
| Layer 7 - GND | 1.20 | 30.48 |
| Prepreg | 2.70 | 68.58 |
| Layer 8 - Signal | 1.90 | 48.26 |
| Bottom Surface | 0.65 | 16.51 |
| | 37.90 | 962.66 |

***Note:*** If there are concerns with warpage due to unbalanced center core, use 1/2 oz copper on L5.

## 2.3 Generalized 10-Layer Motherboard Example

An example of a typical, 10-layer type 3 PCB stack-up is shown in Figure 2-8. These sample stack-ups are provided as a reference when routing the different interfaces.

**Figure 2-8. CFL H 10 Layer Type 3 PCB Stack-Up**

| Type-3 10-Layer | Thickness (mils) | Thickness (um) |
|---|---|---|
| Top Surface | 0.65 | 16.51 |
| Layer 1 - Signal | 1.90 | 48.26 |
| Prepreg | 2.70 | 68.58 |
| Layer 2 - GND | 1.20 | 30.48 |
| Core | 4.00 | 101.60 |
| Layer 3 - Signal | 0.60 | 15.24 |
| Prepreg | 5.00 | 127.00 |
| Layer 4 - Signal | 0.60 | 15.24 |
| Core | 4.00 | 101.60 |
| Layer 5 - GND/PWR | 1.20 | 30.48 |
| Prepreg | 3.00 | 76.20 |
| Layer 6 - GND/PWR | 1.20 | 30.48 |
| Core | 4.00 | 101.60 |
| Layer 7 - Signal | 0.60 | 15.24 |
| Prepreg | 5.00 | 127.00 |
| Layer 8 - Signal | 0.60 | 15.24 |
| Core | 4.00 | 101.60 |
| Layer 9 - GND | 1.20 | 30.48 |
| Prepreg | 2.70 | 68.58 |
| Layer 10 - Signal | 1.90 | 48.26 |
| Bottom Surface | 0.65 | 16.51 |
| | 46.70 | 1186.18 |

An example of a typical, 10-layer type 4 PCB stack-up is shown in Figure 2-9. These sample stack-ups are provided as a reference when routing the different interfaces.

Dual stripline of L3/L4 and L7/L8 has dielectric thickness of 2.5 mils, signal parallelism should be avoided to eliminate potential crosstalk between L3/L4 and L7/L8.

**Figure 2-9. CFL H 10-Layer Type 4 PCB Stack-Up 2-x-2+ (L5, L6 is 1 oz. copper)**

| 2-x-2+ 10-Layer (L5, L6 - 1Oz Cu) | Thickness (mils) | Thickness (um) |
|---|---|---|
| Top Surface | 0.65 | 16.51 |
| Layer 1 - Signal | 1.40 | 35.56 |
| Prepreg | 2.50 | 63.50 |
| Layer 2 - GND | 1.20 | 30.48 |
| Prepreg | 2.50 | 63.50 |
| Layer 3 - Signal | 1.20 | 30.48 |
| Prepreg | 2.50 | 63.50 |
| Layer 4 - Signal | 0.60 | 15.24 |
| Core | 3.00 | 76.20 |
| Layer 5 - GND/PWR | 1.20 | 30.48 |
| Prepreg | 2.50 | 63.50 |
| Layer 6 - GND/PWR | 1.20 | 30.48 |
| Core | 3.00 | 76.20 |
| Layer 7 - Signal | 0.60 | 15.24 |
| Prepreg | 2.50 | 63.50 |
| Layer 8 - Signal | 1.20 | 30.48 |
| Prepreg | 2.50 | 63.50 |
| Layer 9 - GND | 1.20 | 30.48 |
| Prepreg | 2.50 | 63.50 |
| Layer 10 - Signal | 1.40 | 35.56 |
| Bottom Surface | 0.65 | 16.51 |
| | 36.00 | 914.40 |

Dual stripline of L3/L4 and L7/L8 has dielectric thickness of 2.5 mils, signal parallelism should be avoided to eliminate potential crosstalk between L3/L4 and L7/L8.

**Figure 2-10. CFL H 10-Layer Type 4 PCB Stack-Up 1-x-1**

| 1-x-1 10-Layer | Thickness (mils) | Thickness (um) |
|---|---|---|
| Top Surface | 0.65 | 16.51 |
| Layer 1 - Signal | 1.40 | 35.56 |
| Prepreg | 2.50 | 63.50 |
| Layer 2 - GND | 1.20 | 30.48 |
| Core | 4.00 | 101.60 |
| Layer 3 - Signal | 0.60 | 15.24 |
| Prepreg | 5.00 | 127.00 |
| Layer 4 - Signal | 0.60 | 15.24 |
| Core | 4.00 | 101.60 |
| Layer 5 - GND/PWR | 1.20 | 30.48 |
| Prepreg | 3.00 | 76.20 |
| Layer 6 - GND/PWR | 1.20 | 30.48 |
| Core | 4.00 | 101.60 |
| Layer 7 - Signal | 0.60 | 15.24 |
| Prepreg | 5.00 | 127.00 |
| Layer 8 - Signal | 0.60 | 15.24 |
| Core | 4.00 | 101.60 |
| Layer 9 - GND | 1.20 | 30.48 |
| Prepreg | 2.50 | 63.50 |
| Layer 10 - Signal | 1.40 | 35.56 |
| Bottom Surface | 0.65 | 16.51 |
| | 45.30 | 1150.62 |

## 2.4 Single-Ended and Differential-Impedance Transmission Line Specifications

### 2.4.1 Breakout Geometries

Breakout topologies are mainly decided by package ballout patterns and pitches. So similar geometries may be used for various stack-ups. Refer to interface chapters for the breakout maximum length allowed and signals not listed.

**Table 2-9. CFL H Breakout Geometries for Type 3 and Type 4 PCB**

| I/O Interfaces | Stack-Up | Units | Trace Width | Minimum Trace Spacing | Minimum Pair-to-Equivalent Pair Spacing[1] | Minimum Pair-to-Non-Equivalent Pair Spacing[1] |
|---|---|---|---|---|---|---|
| DP/HDMI/eDP/PEG/DMI | MS | mils | 3 | 3 | 9 | 15 |
| | SL/DSL | mils | 3 | 3.5 | 10 | 15 |
| SATA/PCH PCIe/Platform Clocks/USB3.x | MS | mils | 3.5 | 4.0 | 8 | 15 |
| | SL/DSL | mils | 3 | 3.5 | 8 | 15 |
| USB 2.0 | MS | mils | 3.5 | 4.0 | 8 | 15 |
| | SL/DSL | mils | 3 | 3.5 | 8 | 15 |
| UART/SDIO/$I^2C$/SPI | MS | mils | 3 | 3.5 | NA | NA |
| | SL/DSL | mils | 3 | 3.5 | NA | NA |
| Others [2] | MS | mils | 4.0 | 4.0 | NA | NA |
| | SL/DSL | mils | 3 | 3.5 | NA | NA |

***Notes:***
1. Equivalent pairs mean both pairs have equal swing and signal propagation direction. Non-equivalent pairs mean both pairs have different swing or propagation direction. Signal within the same interface and direction is considered as equivalent pair. Example DDI1 and DDI2 are non-equivalent. When different interface signal routed side by side, always refer to the larger spacing requirement.
2. Other refers to legacy signals which are not listed in the table, that is, low speed non-critical signals.
3. MS refers to microstrip; SL refers to stripline; DSL refers to dual stripline

### 2.4.2 Routing Geometries

The following tables list examples of single-ended and differential impedances specified for each interface. The microstrip single-ended impedance and differential impedance tolerance is ±15%. The stripline and dual-stripline single-ended impedance and differential impedance tolerance is ±10% for type 3 PCB, ±12% for type 4 PCB.

***Note:*** *The table notes below apply to the following four tables.*

1. For Type 4, trace width recommended is 4mils to achieve the target impedance.
2. For differential interfaces, Zo is listed as a reference to provide a complete picture of electrical performance. There is no requirement for PCB vendors to measure this impedance.
3. All width/spacing/Kb values are given for reference based on reference stackup. In case of any change in stack up, these values need to be recalculated and priority should be given to meet Z values.

4. Refer to Memory Chapter for all routing geometries and impedance recommendations.
5. Equivalent pairs mean both pairs have equal swing and signal propagation direction. Non-equivalent pairs mean both pairs have different swing or propagation direction. Signal within the same interface and direction is considered as equivalent pair. Example DDI1 and DDI2 are non-equivalent. When different interface signal routed side by side, always refer to the larger spacing requirement.

### Table 2-10. CFL H Microstrip Routing Geometries for Type 3 & Type 4 PCB

| I/O Interfaces | Electrical Target | | | Layout Geometries | | | | |
|---|---|---|---|---|---|---|---|---|
| | Target Zo (Ω) | Kb (%) | Attenuation | Units | Trace Width | Intra pair Trace Spacing | Minimum Pair-to-Equivalent Pair Spacing (Note 5) | Minimum Pair-to-Non-Equivalent Pair Spacing (Note 5) |
| Differential Clock | 85 | 0.37 | -0.27 | mils | 3.5[1] | 4.0 | 12.0 | 15.0 |
| DP/eDP/HDMI/PCIe/ USB3.1 Gen1/SATA/ USB2/CNVi DPHY | 85 | 0.37 | -0.27 | mils | 3.5[1] | 4.0 | 12.0 | 12.0 |
| USB 3.1 Gen2 | 80 | 0.17 | -0.96 | mils | 5.0 | 5.0 | 18.0 | 20.0 |
| Single ended IO (clock, except SoundWire Star Topology M1 Segment) / SVID | 50 | 1.23 | -0.25 | mils | 4.0 | N/A | 15.0 | 15.0 |
| Single ended IO (non clock, except SoundWire Star Topology M1 Segment) / PCH Sideband | | 5.98 | -0.26 | mils | | | 5.0 | 5.0 |
| CPU asynchronous and Sideband signals | | 1.77 | -0.25 | mils | | | 12 | 12 |
| PECI | | 0.90 | -0.25 | mils | | | 18 | 18 |
| SD card/ SPI0 flash (non-clock) | | 2.36 | -0.25 | mils | | | 10 | 10 |
| XTAL / RTC | | 0.75 | -0.25 | mils | | | 20 | 70 |
| CLKIN_LPC | | N/A | N/A | mils | | | N/A | 70 |
| SoundWire Star Topology (M1 Segment for clock) | 35 | 1.68 | -0.25 | mils | 8.0 | N/A | 12.0 | 24.0 |
| SoundWire Star Topology (M1 Segment for non clock) | 35 | 1.68 | -0.25 | mils | 8.0 | N/A | 12.0 | 16.0 |

## Table 2-11. CFL H Stripline routing geometry for Type-3 PCB

| I/O Interfaces | Electrical Target | | | Layout Geometries | | | | |
|---|---|---|---|---|---|---|---|---|
| | Target Zo (Ω) | Kb (%) | Attenuation | Units | Trace Width | Intra pair Trace Spacing | Minimum Pair-to-Equivalent Pair Spacing (Note 5) | Minimum Pair-to-Non-Equivalent Pair Spacing (Note 5) |
| Differential Clock | 85 | 0.015 | -0.25 | mils | 4.0 | 4.0 | 12.0 | 15.0 |
| DP/eDP/HDMI/PCIe/ USB3.1 Gen1/SATA/ USB2/CNVi DPHY | 85 | 0.07 | -0.25 | mils | 4.0 | 4.0 | 12.0 | 12.0 |
| USB 3.1 Gen2 | 80 | 0.03 | -1.04 | mils | 5.0 | 5.0 | 18.0 | 20.0 |
| Single ended IO (clock, except SoundWire Star Topology M1 Segment) / SVID | 50 | 0.16 | -0.25 | mils | 4.0 | N/A | 15.0 | 15.0 |
| Single ended IO (non clock, except SoundWire Star Topology M1 Segment) / PCH Sideband | | 2.22 | -0.26 | mils | | | 5.0 | 5.0 |
| CPU asynchronous and Sideband signals | | 0.42 | -0.25 | mils | | | 12 | 12 |
| PECI | | 0.16 | -0.25 | mils | | | 18 | 18 |
| SD card/ SPI0 flash (non-clock) | | 2.36 | -0.25 | mils | | | 10 | 10 |
| XTAL / RTC | | 0.75 | -0.25 | mils | | | 20 | 70 |
| CLKIN_LPC | | N/A | N/A | mils | | | N/A | 70 |
| SoundWire Star Topology (M1 Segment for clock) | 35 | 1.68 | -0.25 | mils | 7.0 | N/A | 12.0 | 24.0 |
| SoundWire Star Topology (M1 Segment for non clock) | 35 | 1.68 | -0.25 | mils | 7.0 | N/A | 12.0 | 16.0 |

## Table 2-12. CFL H Dual Stripline routing geometry for Type-3 PCB (Sheet 1 of 2)

| I/O Interfaces | Electrical Target | | | Layout Geometries | | | | |
|---|---|---|---|---|---|---|---|---|
| | Target Zo (Ω) | Kb (%) | Attenuation | Units | Trace Width | Intra pair Trace Spacing | Minimum Pair-to-Equivalent Pair Spacing (Note 5) | Minimum Pair-to-Non-Equivalent Pair Spacing (Note 5) |
| Differential Clock | 85 | 0.080 | -0.25 | mils | 4.5 | 4.0 | 12.0 | 15.0 |
| DP/eDP/HDMI/PCIe/ USB3.1 Gen1/SATA/ USB2/CNVi DPHY | 85 | 0.44 | -0.25 | mils | 4.5 | 4.0 | 12.0 | 12.0 |
| USB 3.1 Gen2 | 80 | 0.03 | -1.04 | mils | 5.5 | 5.0 | 18.0 | 20.0 |

## Table 2-12. CFL H Dual Stripline routing geometry for Type-3 PCB (Sheet 2 of 2)

| I/O Interfaces | Electrical Target | | | Layout Geometries | | | | |
|---|---|---|---|---|---|---|---|---|
| | Target Zo (Ω) | Kb (%) | Attenuation | Units | Trace Width | Intra pair Trace Spacing | Minimum Pair-to-Equivalent Pair Spacing (Note 5) | Minimum Pair-to-Non-Equivalent Pair Spacing (Note 5) |
| Single ended IO (clock, except SoundWire Star Topology M1 Segment) / SVID | 50 | 0.63 | -0.25 | mils | 4.5 | N/A | 15.0 | 15.0 |
| Single ended IO (non clock, except SoundWire Star Topology M1 Segment) / PCH Sideband | | 2.22 | -0.26 | mils | | | 5.0 | 5.0 |
| CPU asynchronous and Sideband signals | | 0.42 | -0.25 | mils | | | 12 | 12 |
| PECI | | 0.16 | -0.25 | mils | | | 18 | 18 |
| SD card/ SPI0 flash (non-clock) | | 2.36 | -0.25 | mils | | | 10 | 10 |
| XTAL / RTC | | 0.75 | -0.25 | mils | | | 20 | 70 |
| CLKIN_LPC | | N/A | N/A | mils | | | N/A | 70 |
| SoundWire Star Topology (M1 Segment for clock) | 35 | 1.68 | -0.25 | mils | 8.5 | N/A | 12.0 | 24.0 |
| SoundWire Star Topology (M1 Segment for non clock) | 35 | 1.68 | -0.25 | mils | 8.5 | N/A | 12.0 | 16.0 |

## Table 2-13. CFL H Dual Stripline routing geometry for Type-4 (2-x-2+ 1Oz.)PCB (Sheet 1 of 2)

| I/O Interfaces | Electrical Target | | | Layout Geometries | | | | |
|---|---|---|---|---|---|---|---|---|
| | Target Zo (Ω) | Kb (%) | Attenuation | Units | Trace Width | Intra pair Trace Spacing | Minimum Pair-to-Equivalent Pair Spacing (Note 5) | Minimum Pair-to-Non-Equivalent Pair Spacing (Note 5) |
| Differential Clock | 85 | 0.080 | -0.25 | mils | 2.5 | 3.5 | 12.0 | 15.0 |
| DP/eDP/HDMI/PCIe/ USB3.1 Gen1/SATA/ USB2/CNVi DPHY | 85 | 0.44 | -0.25 | mils | 2.5 | 3.5 | 12.0 | 12.0 |
| USB 3.1 Gen2 | 80 | 0.03 | -1.04 | mils | 3.0 | 3.5 | 18.0 | 20.0 |

**Table 2-13. CFL H Dual Stripline routing geometry for Type-4 (2-x-2+ 1Oz.)PCB (Sheet 2 of 2)**

| I/O Interfaces | Electrical Target | | | Layout Geometries | | | | |
|---|---|---|---|---|---|---|---|---|
| | Target Zo (Ω) | Kb (%) | Attenuation | Units | Trace Width | Intra pair Trace Spacing | Minimum Pair-to-Equivalent Pair Spacing (Note 5) | Minimum Pair-to-Non-Equivalent Pair Spacing (Note 5) |
| Single ended IO (clock, except SoundWire Star Topology M1 Segment) / SVID | 50 | 0.63 | -0.25 | mils | 4.5 | N/A | 15.0 | 15.0 |
| Single ended IO (non clock, except SoundWire Star Topology M1 Segment) / PCH Sideband | | 2.22 | -0.26 | mils | | | 5.0 | 5.0 |
| CPU asynchronous and Sideband signals | | 0.42 | -0.25 | mils | | | 12 | 12 |
| PECI | | 0.16 | -0.25 | mils | | | 18 | 18 |
| SD card/ SPI0 flash (non-clock) | | 2.36 | -0.25 | mils | | | 10 | 10 |
| XTAL / RTC | | 0.75 | -0.25 | mils | | | 20 | 70 |
| CLKIN_LPC | | N/A | N/A | mils | | | N/A | 70 |
| SoundWire Star Topology (M1 Segment for clock) | 35 | 1.68 | -0.25 | mils | 6.0 | N/A | 12.0 | 24.0 |
| SoundWire Star Topology (M1 Segment for non clock) | 35 | 1.68 | -0.25 | mils | 6.0 | N/A | 12.0 | 16.0 |

## 2.5 Low Halogen Flame Retardant Stack-Up Considerations

FR4 epoxy has been used in the construction of PCBs for decades. Consequently, its electrical properties, which are influenced by brominated flame retardants integrated into the molecular structure of the resin, have been studied extensively. As an environmentally friendly alternative to the halogenated flame retardants in FR4, several new low halogen (LH) formulations were developed by different material suppliers. Unfortunately, each new formulation has a unique electrical performance that differs from FR4. This leads to the current problem: The critical electrical properties of many LH dielectrics currently on the market make it difficult to design high-speed busses without increasing the cost of the system. The range of supported Er values therefore limits the amount of cost added.

The most apparent problem lies with the increased permittivity of the LH dielectric materials compared to FR4. Measurements show that several LH PCB materials on the market can have permittivity values around 5 at 1 GHz (using 1080 glass), while FR4 has permittivity values in the 3.6 - 3.9 range. Increased permittivity requires thicker dielectric layers to achieve the equivalent impedance as FR4. In turn, the thicker

dielectric layers lead to an increase in crosstalk which reduces bus performance. If the trace-trace spacing and line widths remain constant (consequently board area consumed remains constant), and the dielectric thickness is adjusted to maintain constant characteristic impedance, the bus performance is reduced for high permittivity values due to increased crosstalk.

Conventional means of reducing crosstalk is to isolate traces as much as practical to reduce the electromagnetic coupling of energy. Unfortunately, modern motherboard designs are often real-estate constrained, requiring extra layers (and therefore cost) to provide additional space for crosstalk compensation when using high permittivity dielectrics.

### 2.5.1 Choosing a Low Halogen Material

Choosing an LH dielectric material for a specific design requires a compromise between performance and cost, especially when a single design is required to work with both LH and FR4 PCB materials. Consequently, it is impossible to define universal requirements for LH dielectrics that will be adequate for all products on the market. Generally speaking however, the dielectric materials used to design printed circuit boards (PCBs) with high-speed digital interfaces perform better with low permittivity and low losses. Low permitivity tends to reduce crosstalk noise for given impedance and low loss tangents reduce signal attenuation.

### 2.5.2 Electrical Limits of Low Halogen Material Properties

Although it is impossible to define electrical limits to universally select “good” materials versus “bad” materials because each design is unique in its implementation, general limits can be chosen that will be adequate for most applications. Simulations were performed on several high-speed buses and validation platforms were built to help identify electrical limits of LH materials that will help ensure:

- Adequate bus performance;
- Interchangeability between FR4 and LH material.

The layout constraints listed in this document have been designed to function with both standard FR4 and LH materials if the electrical properties of the LH materials fall within the envelope defined by the table below.

**Table 2-14. Electrical Limits of LH Material Properties**

| Parameter | Approximate LH Electrical Limits | Environmental Condition |
|---|---|---|
| **Permittivity (Er)** | <4.2 (1080, RC~61%) <4.3 (RC~50%) <4.5 (2116, RC~45%) | Any environmental conditions |
| **Loss Tangent (tanδ)** | <0.018 (1080, RC~61%) <0.014 (1080, RC~50%) <0.013 (2116, RC~45%) | 50% RH & 75$^{o}$F |
| **Moisture Impact on Loss (tanδ)** | <0.024(1080, RC~61%) <0.019(RC=50%) <0.017 (2116, RC~45%) | 95% RH & 95$^{o}$F |

***Note:*** Approximate limits of desired electrical performance of LH dielectric materials; RC =% Resin Content, RH = Relative Humidity; 1080 stack-ups have between ~ 60-65% resin content depending on the layer thickness; Limits established using buses implemented on 1080 material. 2116 (RC=45%) and RC=50% limits extrapolated from the 1080

data points using the volume ratio of resin to glass and average values of resin density, glass density, glass permittivity, glass tan and glass weight basis.

Although the limits listed in the table above are generally lower performance than standard FR4, simulated and measured data indicate that they are sufficient to ensure proper functionality of the buses listed in this design guide. Since the volume of LH materials on the market is small compared to FR4, the performance envelope was made as large as practical to maximize the number of LH materials that comply without significantly sacrificing signal integrity. Table 2-14 does not ensure equal performance to FR4. However, if the limits are adhered to, then the risk of signal integrity problems due to the LH material is greatly reduced. Intel bases signal integrity analysis and validation on these ranges.

Designers should also ensure the LH dielectric materials chosen meet all applicable thermal, mechanical and UL flammability requirements.

## 2.6 Reference Planes

Reference all signal routing layers to a solid ground plane that is continuous over the length of the interconnect. Specific requirements may be defined within the interface design guideline chapters.

Using a power layer as a reference plane is allowed if the power layer is low noise and there is proper decoupling stitching at reference planes transitions to ensure high frequency return path continuity. However, this should only be considered as the secondary reference plane on internal layers where a solid continuous ground reference is already present. Even in this case the power plane must be low noise due to the possibility of noise being coupled into the associated signal planes.

Route noisy power planes on the same layers as signals to minimize fringe coupling by proper spacing separation.

## 2.7 Type 4 PCB Vias

### 2.7.1 Plated Through Hole, Buried Via, and Microvia Dimensions

Various combinations of plated through hole (PTH), buried via, and microvia dimensions when implementing type 4 PCB, as shown in the table below. Selection of one of these combinations depends on what works best for your design, and your PCB vendor. Cost and reliability are considerations in selecting one of these via combinations.

Combination #3 in the table below requires an overlap between buried via and microvia. Some PCB vendors may require the buried via to be capped. It is recommended use of this combination be reviewed with the PCB vendor, to thoroughly understand cost and reliability factors.

**Table 2-15. Type 4 PCB Via Combinations**

| # | PTH Drill/Pad/ Antipad | Buried Via Drill/ Pad/Antipad | Microvia Drill/ Pad/Antipad | Comments |
|---|---|---|---|---|
| 1 | 10/20/28 | 8/18/26 | 5/12/20 | No overlap between microvia and buried via |
| 2 | 10/20/28 | 10/20/28 | 4/10/18 | No overlap between microvia and buried via |
| 3 | 10/20/28 | 10/20/28 | 5/12/20 | 1 mil overlap between microvia and buried via. Consult PCB reliability rules. |

## 2.7.2 Staggered versus Stacked Microvias

The Coffee Lake processor reference design with LPDDR3 memory down uses type 4 PCB with stacked microvias. This is especially important in the package breakout and LPDDR3 down breakout areas, where there is routing congestion and a desire to minimize voiding on the L2 ground reference plane.

**Figure 2-11. Staggered vs. Stacked Microvias**

***Note:*** Staggered microvias are shown the left and Stacked microvias are shown on the right

Stacked vias are used to minimize voiding of a high-speed signal's ground reference plane.

## 2.7.3 Buried Via to Microvia Keep-Out

In type 4 PCB, buried vias and microvia combinations create voids in the L2 GND layer. The size of these voids is primarily dependent on how large the distance is between the buried via and microvia on L2, also called the buried via to microvia keep-out.

Large keep outs can lead to significant L2 GND plane perforation and L3 signal return path discontinuities. Large keep-outs also require longer routing between vias on L2. These signals can suffer from severe impedance discontinuities as this trace segment may not find any proper reference on L1 or L3. We strongly recommend limiting the voiding on L2, by minimizing the buried via to microvia keep-out distance. If possible, use a keep-out of 0 mils.

**Figure 2-12. Type 4 PCB PTH to Microvia Keep Out**

## 2.8 Backward and Forward Coupling Coefficient Calculation

Some designs require a stack-up build that is outside of the ranges provided. In this case, compare the routing electrical characteristics versus the Intel recommendation.

Comparing the single-ended and differential-impedances is important. However, crosstalk level, which is governed by trace spacing, is not implied by the impedance target. Calculating and comparing backward coupling coefficients is recommended to choose proper trace spacing in cases where the selected stack-up varies from the Intel recommendation.

The coupling coefficients represent the source voltage percentage that is coupled to victim lines. As shown in Figure 2-13, $K_b$ is defined as the backward coupling coefficient. For backward (near-end) crosstalk, inductive and capacitive coupling are of the same polarity and the noise magnitude is not a function of trace length. The backward coupling coefficient ($K_b$) values can be used to decide trace spacing.

For forward (far-end) crosstalk, $K_f$ inductive and capacitive coupling are of opposite polarity and the crosstalk magnitude (Vfe) is proportional to both trace length and edge rate. $K_f$ is typically a very small value in most practical designs. Therefore, Intel has not included the $K_f$ values in this design guide. However, the equation for calculating $K_f$ is provided in Figure 2-14, "Forward Coupling Coefficient" if the value is desired.

$K_b$ values for all interfaces for all routing layers can be found in figures below. They were calculated assuming a nominal or typical stack-up configuration based on the values in Table 2-10 through Table 2-14. For single-ended interfaces, the $K_b$ values reflect the crosstalk seen between each single-ended signal based on typical spacing. For differential interfaces, the $K_b$ values reflect the crosstalk seen between each differential pair based on the typical pair-to-pair spacing.

**Figure 2-13. Backward Coupling Coefficient**

$$K_b = \frac{1}{4}\left(\frac{|C_{ij}|}{\sqrt{C_{ii}C_{jj}}} + \frac{|L_{ij}|}{\sqrt{L_{ii}L_{jj}}}\right),$$

$$V_{NE} = K_b \bullet V_0$$

**Figure 2-14. Forward Coupling Coefficient**

$$K_f = \frac{1}{2}\left(\frac{|C_{ij}|}{\sqrt{C_{ii}C_{jj}}} - \frac{|L_{ij}|}{\sqrt{L_{ii}L_{jj}}}\right)\left(L_{ii}C_{ii}L_{jj}C_{jj}\right)^{1/4}$$

$$V_{FE} = K_f \bullet Length * \frac{dV}{dt}$$

**Figure 2-15. Single Ended Kb Diagram**

**Figure 2-16. Differential Kb Diagram**

## 2.9 Minimizing the Effect of Fiber Weave

### 2.9.1 Overview of Fiber Weave

Fiber weave in the PCB material impacts the routing of high-speed traces. The PCB material is made up of a composite of fiber and resin. The strands of fiber run perpendicular to each other. Depending on the orientation of the weave relative to the trace, there could be either resin or a fiber bundle beneath the trace. Due to the differing dielectric constants of these two materials, a phase skew could be introduced among signals that comprise a differential pair. This phase skew manifests itself as an AC common mode noise at the receiver, affecting both voltage and timing margin at the receiver. The layout recommendations in this section will minimize the effect of the PCB fiber weave on the routing of differential signals. The choice of a particular mitigation technique is dependent on the configuration and layout of the platform and, hence, this choice is left to the platform designer. Typical printed circuit boards, due to their basic construction consisting of woven fiberglass fabric (Er~6) strengthened and bound together with epoxy resin (Er~3.5), present a non-homogeneous medium for signal propagation of differential pairs. As shown in Figure 2-17, there are several weave types, with the weave strands running horizontal and vertical relative to the board edges. For differential pairs with trace width and spacing comparable to the dimensions of the fiberglass cloth, the PCB's non-uniform dielectric can give rise to substantial propagation differences between the conductors of the pair, refer Figure 2-18.

**Figure 2-17. Common Glass Cloths Used in PCB Manufacture**

***Note:*** Weave types above are for illustration purposes only

**Figure 2-18. Inhomogeneous Nature of a PCB as Shown in this Cross-Section**

***Note:*** Fiberglass weave bundle and epoxy regions are shown in this figure.

At high data rates this skew can amount to a substantial fraction of the transmission unit interval, resulting in an increased common mode voltage and a correspondingly degraded differential signal (Figure 2-19). In addition, the resulting common mode signal (ACCM) can become a source of increased crosstalk and EMI in the system, or violate receiver ACCM specifications.

**Figure 2-19. Effect of Skew on Differential and Common Mode Signals**

**Figure 2-20. Cross-Section of PCB Indicating Effect of PCB Fiber Weave**

Fiber weave effect is noticeable for routing lengths greater than 2” and this effect gets more pronounced for longer trace lengths. There are many approaches to minimize this effect and the next three sections suggest some methods to mitigate this effect. The AC common mode noise causes considerable degradation of the signal for trace lengths in the range of 5” to 15” for a typical PCB stack-up on FR4 material.

## 2.9.2 Fiber Weave Effect versus Transfer Rate and Trace Length

**Table 2-16. Max Root Square Sum (RSS) Length versus Transfer Speed**

| Transfer Speed | Max RSS length (See note 1) |
|---|---|
| 2.5 GT/s | 5" |
| 4 GT/s | 4" |
| 5 GT/s | 3" |
| 6.4 GT/s | 2.5" |
| 8 GT/s | 2" |

***Notes:***

1. The lengths in the table represent total trace lengths that are aligned to the weave (that is, parallel to the manufacturing panel's edge). Actual routing may have a significant portion of the length at angles to the edge of the board- those lengths should not be considered in this analysis.
   The total length is the Root Square Sum of total vertical and horizontal lengths that run parallel to the weave:

   $$Length = (H_1)^2 + (H_2)^2 + (H_3)^2 + (V_1)^2 + (V_2)^2 + (V_3)^2 + \ldots$$

   where:
   a. Hx = length of each segment routed horizontally, and
   b. Vx=length of each segment routed vertically

2. The table represents an approximation only, based on simulations of "representative" topology. The exact fiber weave may vary, depending on the exact topology.

## 2.9.3 Specific Routing Configurations

Some platforms might have their components laid out in a manner that requires non-orthogonal (to the PCB board edge) routing for their high-speed busses. Orthogonal routing up to a maximum length of 2" does not result in a noticeable impact on the differential signals. However, there could be a significant amount of AC Common-Mode voltage introduced between the differential pair that the platform designer will need to consider.

## 2.9.4 Offset Routing

This involves routing the trace in a straight line with offset in the middle equal to a glass bundle pitch. The glass bundle pitch differs by materials and direction and is dependent on the particular manufacturing process. An example is shown in figure below. For this technique to be applied, a PCB layout tool with this capability would be required.

**Figure 2-21. An Example of Offset Routing**

## 2.9.5 Zig-Zag or Slanted Routing

If the weave is aligned to the PCB edges, follow a zig-zag or slanted routing of differential traces. Maintain a minimum angle of 10 degrees between the trace and fiber weave. This will lead to traces that are angled relative to the PCB edge. Figure 2-22 is an example of zig-zag routing. Figure 2-23 shows slanted routing. For this technique to be applied, a PCB layout tool with this capability would be required.

**Figure 2-22. An Example of Zig-Zag Routing**

**Figure 2-23. An Example of Slanted Routing**

## 2.9.6 Image Rotation

Another solution is to maintain an angle between the trace and the fiber weave pattern is to rotate the weave relative to the edge of the PCB, thereby maintaining differential trace routes aligned with edges of the PCB (refer to Figure 2-24). It is recommended the rotation be such that the traces are at a 10 degree angle relative to the fiber weave. The rotation can be achieved by cutting the PCB board at an angle, as shown in Figure 2-24, or by rotating the layout database relative to the edge of the PCB board. The latter requires the use of an appropriate PCB routing software that has this capability.

### 2.9.7 Using Alternate PCB Materials

**Figure 2-24. An Example of a PCB Cut Such That Its Edges are Rotated Relative to the Fiber Weave Pattern**

The fiber weave effect can also be minimized by using PCB material that exhibits less variation in the dielectric coefficient $E_r$ between the epoxy and glass materials.

## 2.10 Flexible Printed Circuit Consideration

Internal cables are widely used inside computing devices, ranging from phone, camera, tablet, and notebook. They are usually non-standard or customized and may include regular cables such as discrete wires, twisted pairs, twin-axial and coaxial wires, as well as FFC (Flexible Flat Cable) and FPC (Flexible Printed Circuit).

With the usages becoming more common, designers are gaining awareness on the importance of cable selection. Flexibility, impedance, crosstalk, EMI and RFI, have always been the factors in cable selection. Refer to RDC#550502 on "Flexible Printed Circuit Electrical Characterization and Recommendation"

## 2.11 Coffee Lake Client Signal Integrity Tool Suite

Coffee Lake Client Signal Integrity Tool Suite RDC#572252 is pre-silicon signal integrity tools targeted for Coffee Lake based design. The tool Suites includes Electrical Channel Simulator (ECS), TlineCalc, and freqMasterEx.

ECS provides customers with an advanced post processing simulation tool to assess the risk level and evaluate voltage and timing margins for any design that falls inside and outside of the PDG, as well as white papers. FreqMasterEX is a toolbox, mainly used to perform evaluation of S-parameter and create equivalent models to be used in ECS. Tline calc, as snapshot in Figure 2-30, is a tool in assisting customer in PCB board stack-up electrical characteristics calculation, to ease customer to compare these electrical characteristics to Intel's assumptions listed in the PDG.

## Figure 2-25. Snapshot of Electrical Channel Simulator (ECS)

## Figure 2-26. Snapshot of freqMasterEx Toolbox

**Figure 2-27. Snapshot of TlineCalc**

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# 3 General Differential Design Guidelines

## 3.1 General Differential Stackup Guidelines

### 3.1.1 Stackup and Layer Utilization Guidelines

#### 3.1.1.1 General Dual-Stripline Support

In cases where high speed differential signals (PEG, DMI, or eDP, etc) are routed in an 8- or 10- layers dual-stripline stack-up, follow the guidelines in Table 3-1. Figure 3-1 illustrates the meaning of Tx-over-Tx, Rx-over-Rx, and Tx-over-Rx.

**Table 3-1. General Dual-Stripline Support**

| Tx -over-Rx Parallel Routing | Tx-over-Tx or Rx-over-Rx Parallel Routing | Tx-over-Rx or Tx-over-Tx or Rx-over-Rx Routing Orthogonal or with Angle |
|---|---|---|
| • Parallel routing not allowed<br>• Route with an offset of 15mil or greater as shown in Figure 3-3. | • A maximum of 2 inches of parallel routing is allowed | • Routing at an angle of at least 30 degrees significantly reduces layer-to-layer crosstalk. Route differential pairs at a 30, 45, 60, 90 etc degree angle. Figure 3-2 shows orthogonal routing. Figure 3-4 shows angled routing at less than 90 degrees.<br>• Allow maximum of 10 aggressor pairs to route over 1 DSL routing victim pair. |

**Figure 3-1. Tx-over-Tx, Rx-over-Rx, and Tx-over-Rx**

**Figure 3-2. Dual-Stripline Orthogonal Routing Recommendation**

**Figure 3-3. Dual-Stripline High Speed Signal Dual Layer Routing Recommendation**

**Figure 3-4. Recommended Routing Angle to Reduce Layer-to-Layer Crosstalk**

## 3.2 General Differential Routing Guidelines

### 3.2.1 Breakout Example and Guidelines

Maintain differential routing rules in package breakout areas.

**Figure 3-5. Board Breakout Example**

**Figure 3-6. Board Breakout Example**

Guidelines are as follows:

- **Differential-pair pitch** is measured from the center of each trace in the differential-pair. The distance from the center of either trace in a differential-pair to the same point of reference on an adjacent differential-pair is described as **interpair pitch (IPP)**. Refer Figure 3-7 for the illustration of differential-pair pitch and IPP.

- **Differential-pair space** is measured from the edge of each trace in the differential-pair. The distance from the edge of one trace in a differential-pair to the near edge of an adjacent differential-pair is described as pair-to-pair space. Refer Figure 3-7 for the illustration of differential-pair space and pair-to-pair space.
- Maintain the best possible **lateral routing symmetry** between the two signals of a differential-pair. (refer Figure 3-8).
- Breakout routing geometries can be found in the PCB Considerations section.

***Caution:*** Maintain routing symmetry between the two signals of a differential-pair. Failure to maintain symmetry introduces an AC common mode voltage.

***Caution:*** Reduced trace width will increase losses due to skin effects and reduced spacing will increase crosstalk. Therefore, it is recommended to keep breakout routing as short as possible.

**Figure 3-7. Differential-Pair Spacing Diagram**

**Figure 3-8. Symmetrical and Non-Symmetrical Routing Example**

## 3.2.2 Differential I/O Routing Scheme Guidelines

Simulation results show that the receiving margin is severely degraded by near-end crosstalk (NEXT) from adjacent Transmit signals. Thus, non-interleaved breakout is required to mitigate concerns on near-end crosstalk.

The Cannon Lake PCH-H package ballmap has most of Tx signals on outer balls and Rx signals on inner balls to help facilitate non-interleaved breakout.

The recommended implementation is illustrated in Figure 3-9, HSIO Tx and HSIO Rx signals are breakout on different board layers or have TX and RX lane at least 15 mils spacing separations.

**Figure 3-9. HSIO Non-interleaved Breakout Guidelines**

**Figure 3-10. Non-interleaved versus Interleaved Routing**

In further suppressing the far-end crosstalk (FEXT), interleaved or semi-interleaved routing is recommended in main routing region.

As illustrated in Figure 3-11, routing scheme changed from non-interleaved in breakout region into interleaved or semi-interleaved in main routing region.

**Figure 3-11. HSIO Interleaved or Semi-Interleaved Main Routing**

Figure 3-12 illustrates the full board routing recommendation, from package ball to device.

**Figure 3-12. Differential Routing Guidelines**

## 3.3 General Differential Optimization Guidelines

### 3.3.1 Via Placement and Via Usage Optimization

- Vias impact the overall loss and jitter budget. Routing signals with a minimal number of vias.
- The via count can be reduced but not increased from the maximum interface via requirement.
- Long via stub degrades overall signal integrity margin. Specific via stub length requirements may be defined within the interface design guideline chapters. For MS to SL/DSL routing recommendation on CFL H platform, routing recommendation has covered via stub length as below.
  - PEG <=10 mils
  - DMI /DP/PCH IO <=25 mils
- Remove pads from unused internal layers to minimize excess via capacitance.
- The differential-pair via placement must be symmetrical. Vias on the differential-pair should not only match in number but also in relative location.

**Figure 3-13. Via Pair Example**

***Note:*** The via placement examples below apply to all high speed interfaces such as PEG, DMI, eDP, and PCH PCIe3.

**Figure 3-14. Example - Via Placement 1**

- The symmetric via pattern in Figure 3-15 below minimizes crosstalk between 2 differential pair, therefore the recommendation is to implement the pattern according to area availability.

**Figure 3-15. Example - Via Placement 2**

- For differential interfaces it is recommended 1:1 ratio of signal to GND via everywhere it is possible (Figure 3-16).

**Figure 3-16. Board Breakout Example - Via Placement 3**

### 3.3.1.1 Differential Transitional Via Recommendations

Transitional vias will use oval-shapes anti-pads on all plane layers. This can be created using a rectangular-shaped void to overlap with the usual round-shaped via anti-pad. The vias must also have a symmetrical trace entry.

Figure 3-17 and Table 3-2 provides the transitional differential via pad stack details.

**Figure 3-17. Differential Transitional Via Layout**

**Table 3-2. Differential Transitional Via Layout Recommendations**

| Parameter | Units | Recommendation |
|---|---|---|
| Via Diameter | mils | 10 |
| Via Pad Size | mils | 22 |
| Oval-Shaped Anti-Pad Size | mils | 32 |
| Via-to-via Distance (centered) | mils | 35 |

## 3.3.2 Bend Optimization Guidelines

Bends are a necessary component in routing differential signals. Guidelines for bends are as follows:

- Keep bends to a minimum. Bends can introduce common mode noise into the system, which can affect the signal integrity of the differential signal pair.
- If bends are required, they should be at a 135-degree angle or greater; there should be no 90-degree bends or turns. An adequate air gap should be maintained between the inside traces of a bend. The gap should be 4 times the trace width or greater. The lengths of the segments in a bend should be 1.5 times the trace width or greater. Refer Figure 3-18 and Figure 3-19 for examples.
- Match the number of left bends to the number of right bends to minimize skew due to length differences between each signal of the differential-pair.
- Alternate between left and right bends.

Matching the number of right and left turns and alternating bends helps to minimize the amount of skew between rising or falling edges, which minimizes the differential to common mode conversion.

**Figure 3-18. Acceptable Bends vs. Tight Bends Example**

**Figure 3-19. Maximum Bend Angle**

## 3.3.3 Component Footprint Optimization Guidelines

Voiding the Ground/Power plane on the layer directly underneath SMT signal pads can help to minimize impedance mismatch caused by the SMT pads. This is recommended for large SMT pads of components such as ESD protection devices, Common Mode Chokes (CMC) and connectors. In general, the reference plane should be voided with the same size as the SMT pad. Voiding is only required on the layer directly underneath SMT signal pads and not required on any other internal layers. Voiding is not required for small components pads such as 0402 components and AC capacitors.

## 3.3.4 General Routing Guidelines

- DO NOT route traces under power connectors, power delivery inductors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks. DO NOT place stubs, test points, test vias on the route to minimize reflection. Utilize vias and connector pads as test points instead. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- It can be helpful for testability to route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.

- Separate signal traces into similar categories, and route similar signal traces together (such as routing differential pairs together).
- Keep signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.

## 3.4 General Differential Length Matching Guidelines

### 3.4.1 Length Matching and Length Formulas

Follow the specific interface length matching guidelines if provided. If not provided, use the below as a general guideline. This guidelines is to minimize signal integrity, EMI and RFI problems.

**Table 3-3. General Differential Pair Length Matching**

| Description | Units | Routing Recommendation |
|---|---|---|
| Within Layer Max Mismatch | mils | +/- 10 |
| Total Length Max Mismatch | mils | +/- 5 |
| ***Note:***<br>1. Preferred to keep both "within layer max mismatch" and "total length max mismatch" within 5 mils | | |

The following are the length matching guidelines for differential-pairs:

- Each signal and its complement in a differential-pair should be length matched whenever possible on a layer-by-layer basis at the point of discontinuity. 'Within-layer' matching means that differential pairs should be matched within 10 mils before transitioning to a different layer. At any via transition the n/p mismatch for the entire route preceding the via cannot exceed 10 mils.
- When trace length matching, the matching should be made as close as possible to the point where the length variation occurs, as shown in Figure 3-20, so the discontinuity won't propagate across the channel. For example, length matching in a chipset breakout area or connector pin field should occur within first 125 mils (3.175 mm) of the structure that causes mismatch.
- Serpentine layout introduces discontinuity to the channel and should be minimized so as to make it transparent to the signal. This is done by making its electrical length shorter than the signal rise time. In general, keeping serpentine routing length <100 mils is adequate. Trace spacing should not become greater than two times the original spacing. Refer Figure 3-21.
- In determining the overall length of a given signal in a differential-pair, use pad or pin edge-to-edge distances rather than the total etch present, unless the amount of trace routing inside each pad is identical. The amount of etch within a given pad is electrically part of the pad itself. In other words, only the etch outside of the pad edge is relevant to the overall length of a differential-pair. For example:
  - If the P signal of the differential-pair has an extra 5 mils (0.127 mm) of etch length compared to the N signal, and the extra 5 mils (0.127 mm) occurs due to extra etch extending into a component pad, the two signals should be considered identical length.

— Similarly, trying to length match signals by adding etch inside a pad boundary (such as extra bends inside the pad itself) does not produce the intended length matching effect on the interconnection (refer Figure 3-22).

**Figure 3-20. Example - Length Matching**

**Figure 3-21. Example - Serpentining**

**Figure 3-22. Example - Etch Located within a Pad**

**Figure 3-23. Example - Good Length Matching**

**Figure 3-24. Example - Poor Length Matching**

## 3.5 General Differential Compensation and Voltage Reference Guidelines

### 3.5.1 RCOMP Signal Guidelines

Cannon Lake PCH-H uses a global Resistance compensation. The calculated values are used across all lanes for adjustment for termination values. Voltage across RCOMPP and RCOMNN is measured differentially and hence matching is very critical. The RCOMP signals should be referenced to Vss and noisy or switching references should be avoided. As board space allows, recommend to add a VSS shield at least 4 mils wide placed between RCOMP and adjacent IO. It is important that these signals maintain low DC resistance routing (<0.1 Ω), so they should be routed with wide and short traces. For the breakout from the PCH, a minimum trace width of 4 mils is allowed with a maximum of 100 mils. All other RCOMP and IREF should be routed with a minimum or 4 mils.

Avoid routing these signals next to clock pins or noisy signals, but a partial VSS shield (defined as a 4 mil VSS shield routed in between the IREF/COMP signals and any adjacent high speed IO) is recommended for RCOMP and IREF. There is no shielding required between RCOMP and IREF. In order to meet these requirements a minimum spacing of 12 mils is required between the IREF/COMP signals to any adjacent high speed IO.

### 3.5.2 Reference Planes

Guidelines for reference planes are as follows:

***Note:*** Reference all signal routing layers to a solid ground plane that is continuous over the length of the interconnect. This is an important requirement especially on high speed differential signal e.g. DMI, PEG, DDI, PCIe3, etc. Specific requirements may be defined within the interface design guideline chapters.

***Note:*** Using a power layer as a reference plane is allowed if the power layer is low noise and there is proper decoupling stitching at reference planes transitions to ensure high frequency return path continuity. However, this is only be allowed as the secondary reference plane on internal layers where a solid continuous ground reference is already present. Even in this case the power plane must be low noise due to the possibility of noise being coupled into the associated signal planes (referencing to noisy power planes that are used by switching VRs are not allowed).

***Note:*** Route noisy power planes on the same layers as signals to minimize fringe coupling by proper spacing separation.

***Note:*** Even when routed as coupled differential-pairs, one trace can experience more coupling to its reference plane than to its routing pair.

- Traces should avoid discontinuities in the reference plane, such as splits and other voids.
  - A good plane reference helps to minimize any AC common mode voltage found on the differential-pair as well as benefiting signal quality and minimizing EMI.
- When routing near the edge of their reference plane, traces should maintain at least a 40-mil (1.016-mm) space keepout from the edge of the plane.

***Note:*** Referencing signals going over a board-to-board connector must be considered and stitching capacitors should be added at the connector as appropriate. For example, if a differential-pair is GND-referenced on the motherboard and the pair is $V_{CC}$ referenced on the daughter card, then stitching capacitors must be added at the connector between $V_{CC}$ and GND.

- One reference plane should be used for the entire length of the trace route.
  - In a traditional 8-layer stack-up, there are two microstrip/stripline routing channel pairs that each share a common reference layer. It is preferred that any layer transitions switch between these two layers, within this layer pair. For example, Layer 1 and Layer 3 are tightly coupled to Layer 2 and form one layer pair; Layer 8 and Layer 6 are tightly coupled to Layer 7 and from another layer pair.
  - In a traditional 6-layer stack-up, there are two microstrip/stripline routing channel pairs that each share a common reference layer. It is preferred that any layer transitions switch between these two layers, within this layer pair. For example, Layer 1 and Layer 3 are tightly coupled to Layer 2 and form one layer pair; Layer 4 and Layer 6 are tightly coupled to Layer 5 and from another layer pair.
  - If this cannot be accomplished, stitching vias must be used to tie the two planes together. The vias should be located within 200 mils (5.08 mm) and in symmetry with the two signal vias to minimize return path discontinuities.
- Differential signals should not cross any plane splits or voids. However, it may be necessary for a trace to be partially routed over a via anti-pad void in the chipset escape area. The amount of the trace that is over the void should be minimized in the length and percentage of the width of the trace. At worst, no more than half of the trace width should be over the via anti-pad at any given time.
  - If crossing a plane split is necessary, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high-speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers.
  - As an example of bridging plane splits, a plane split that separates $V_{5REF}$ and $V_{CC3_3}$ planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to $V_{5REF}$ and the other side should tie to $V_{CC3_3}$. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates. *Do avoid this scenario, as capacitors stitching on bridging plane splits may only help if both the power planes are not noisy. It is harmful if one of or both the power planes is noisy.*

### 3.5.2.1 Option 1

This is the most preferred Design option:

- Reference all signals routing to a solid ground plane that is continuous over the length of the interconnect. This is important especially for high speed differential signals e.g. DMI, PEG, DDI, PCIe3, etc. Specific requirements may be defined within the interface design guideline chapters.
- Differential signals should not cross any plane splits or voids. However, it may be necessary for a trace to be partially routed over a via anti-pad void in the chipset escape area. The amount of the trace that is over the void should be minimized in the length and percentage of the width of the trace. At worst, not more than half of the trace width should be over the via anti-pad at any given time.

- A good plane reference helps to minimize any AC common mode voltage found on the differential-pair as well as benefiting signal quality and minimizing EMI.
- Referencing for signals going over a board-to-board connector must be considered and stitching capacitors should be added at the connector as appropriate. For example, if a differential-pair is GND-referenced on the motherboard and the pair is VCC referenced on the daughter card, then stitching capacitors must be added at the connector between VCC and GND.

### 3.5.2.2 Option 2

The second preferred design option is for signals to have a solid reference plane (be it VCC or GND) that is continuous over the length of the interconnect. This means that the signals do not route over multiple splits referencing planes in a single layer. An example is shown in Figure 3-25 below.

**Figure 3-25. Example - Solid Reference Plane Option**

Low ESL stitching capacitor of 1uF should be included to provide a sufficient return path for high speed signals up to 200 mils away. Additional stitching capacitors should be added for additional signals that do not fall within 200 mils of the first stitching capacitor. This is shown in Figure 3-26.

**Figure 3-26. Example with Low ESL Stitching Capacitor**

Using a continuous power layer as a reference plane is allowed only if the power layer is low noise. This is to avoid the possibility of noise coupling from power to signals.

Signals referencing noisy power planes that are used by switching VRs are not allowed. Route noisy power planes on the same layer as signals to minimize fringe coupling. Do note to implement proper spacing in this case.

### 3.5.2.3 Option 3

If continuous solid plane referencing is unable to be implemented and routing over split planes are unavoidable, the third preferred option is to consider inserting GND planes in between the power planes.

This is to allow for stitching capacitors to be inserted in between the power and ground planes. This option will enable a proper return path for the signals without a significant impact on power integrity.

This option however comes at the cost of a potential added BOM cost.

An example is shown in below figures.

**Figure 3-27. Example - Routing over Split Plane**

**Figure 3-28. Example - Routing Over Split Plane With Low ESL Stitching Capacitor**

### 3.5.2.4 Option 4

The least preferred option is when all the following occurs:

- A solid GND referencing is unavailable.
- A continuous solid plane referencing is unable to be implemented.

- Routing over split planes are unavoidable.
- GND planes are unable to be inserted in between the power planes.

During this case, it is preferable that the power planes crossed by the signals to be of similar voltage levels so as to minimize inter-power plane noise. Stitching capacitors are needed. The capacitor ends should tie to each plane separated by the split.

If the cross plane split occurred between planes of different voltages, then sufficient board decoupling capacitors need to be added to the planes to minimize power integrity noise. Initial recommendation is to include 4 additional capacitors of 1 uF that should be placed within 10mm from the package edge. These should be added in addition to the stitching capacitors requirement.

This option will also come at the cost of a potential added BOM cost.

Examples are shown in below figures.

**Figure 3-29. Example - Routing Over Split Plane and GND Planes are Unable to be Inserted**

**Figure 3-30. Example - Routing Over Split Plane and GND Planes are unable to be Inserted With Low ESL Stitching Capacitor**

## 3.6 General Docking Connector Recommendations for Differential Interfaces

Although various types and suppliers of docking connectors can be used, Intel recommends following the electrical characteristics in Table 3-3. This table lists the differential insertion loss, return loss, crosstalk, and impedance that Intel assumes

when doing docking topology analysis for all differential interfaces. These are the docking connector electrical characteristics that customers should reference to if customers have routing done within PDG routing guidelines.

**Figure 3-31. Example Port A Assignment for Docking Connector**

## 3.7 RCOMP

The RCOMP recommendation for various interfaces provided below

**Figure 3-32. RCOMP recommendations**

| | DDR_RCOMP | PEG_RCOMP | DISP_RCOMP | CFG_RCOMP | PCIE_RCOMP_P/N | USB2_COMP | SD_RCOMP_1P8 | SD_RCOMP_3P3 | GPPJ_RCOMP_1P8 | XCLK_BIASREF | CNV_WT_RCOMP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Board Rterm (ohm) | n/a | 24.9Ω +/-1% to VCCIO | 24.9Ω +/-1% to VCCIO | 49.9Ω +/-1% to GND | 100Ω +/-1% Differential | 113Ω +/-1% to GND | 200Ω +/-1% to GND<br>Notes: SD_RCOMP_1P8, SD_RCOMP_3P3 and GPPJ_RCOMP_1P8 can have merged 200Ω +/-1% to GND resistor. | 200Ω +/-1% to GND | 200Ω +/-1% to GND | 60Ω +/-1% to GND | 150Ω +/-1% to GND |
| Board Rdc (ohm) | n/a | <0.1 | <0.1 | <0.5 | <0.1 | <0.5 | <0.1 | <0.1 | <0.1 | <0.5 | <0.5 |
| Package Rterm (ohm) | DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS<br>DDR_RCOMP[1]: 75 Ω ± 1% on pkg to VSS<br>DDR_RCOMP[2]: 100Ω ± 1% on pkg to VSS | n/a | n/a | n/a | n/a | n/a | n/a | n/a | n/a | n/a | n/a |
| DDR | X | | | | | | | | | | |
| PEG (CPU) | | X | | | | | | | | | |
| DMI | | X | | | | | | | | | |
| HDMI | | | X | | | | | | | | |
| DP | | | X | | | | | | | | |
| eDP | | | X | | | | | | | | |
| CFG | | | | X | | | | | | | |
| ModPHY | | | | | X | | | | | | |
| USB2 | | | | | | X | | | | | |
| SD3 | | | | | | | X | X | | | |
| 1.8 GPIO | | | | | | | | | X | | |
| Differential Clock | | | | | | | | | | X | |
| CNV_DPHY | | | | | | | | | | | X |

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# 4 System Memory Interface Design Guidelines

The Coffee Lake platform supports multiple memory technologies. This chapter covers the guidelines to design a Coffee Lake platform with the following Plan of Record (POR) supported system memory interface configurations and features.

***Notes:***

1. For schematic level and additional system memory signal connection details not covered in this chapter reference the schematic check list chapter.

2. For complete Coffee Lake processor system memory interface POR feature support details see the latest release of the CFL Processor External Design Specification (EDS).

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## Table 4-1. System Memory Configurations Supported by Guidelines in this Chapter

| Platform | Config #/ Chapter | Tech | Topology | Freq | Memory Device | Device Ballout | PCB Stackup | IL/ NIL |
|---|---|---|---|---|---|---|---|---|
| CFL-H | Chapter 4.1 | DDR4 | SODIMM + ECC 2DPC | 2400 | ECC DIMMs:<br>RC-D(1Rx8),RC-G(2Rx8),<br>RC-F(2Rx8),RC-H(2Rx8)<br>Non-ECC DIMMs:<br>RC-A(1Rx8),RC-B(2Rx8),<br>RC-E(2Rx8),RC-C(1Rx16) | 260 | Type3 - 10L | IL |
| | Chapter 4.2 | DDR4 | SODIMM 2DPC | 2400 | RC-A(1Rx8), RC-B(2Rx8),<br>RC-E(2Rx8),RC-C(1Rx16) | 260 | Type3 - 8L | IL |
| | Chapter 4.3 | DDR4 | SODIMM 1DPC | 2400/ 2666 | 2666:<br>RC-A(1Rx8),RC- E(2Rx8),<br>RC-C(1Rx16)<br>2400:<br>RC-B(2Rx8) | 260 | Type3 - 8L | IL |
| | Chapter 4.4 | DDR4 | SODIMM + ECC 1DPC | 2400/ 2666 | ECC DIMMs:<br>2666:<br>RC-D(1Rx8),RC-G(2Rx8)<br>2400:<br>RC-H(2Rx8)<br><br>Non-ECC DIMMs:<br>2666:<br>RC-A(1Rx8),RC-E(2Rx8),RC-C(1Rx16)<br>2400:<br>RC-B(2Rx8) | 260 | Type3 - 10L | IL |
| | Chapter 4.5 | DDR4 | MD 1R x16<br>(4 per ch)<br>Daisy Chain | 2666 | SDP x16<br>DDP x16 | 96 | Type3 - 10L | NIL |
| | Chapter 4.6 | DDR4 | MD 2R x8 | 2666 | SDP x8 | 78 | Type3 - 10L | NIL |
| | Chapter 4.7 | DDR4 | Mixed<br>SODIMM and<br>MD x16 Daisy-Chain (4 per ch) | 2400/ 2666 | SODIMM:<br>2666:<br>RC-A(1Rx8),RC-E(2Rx8),RC-C(1Rx16)<br>2400:<br>RC-B(2Rx8)<br><br>Memory Down:<br>2666:SPD x16<br>2400:DDP x16 | SODIMM :260<br><br>MDx16: 96 | Type3-8L | IL |
| | Chapter 4.8 | DDR4 | Mixed<br>SODIMM & MD 1Rx8 Daisy Chain (8 per ch) | 2400/ 2666 | SODIMM:<br>2666:<br>RC-A(1Rx8),RC-E(2Rx8),RC-C(1Rx16)<br>2400:<br>RC-B(2Rx8)<br><br>Memory Down:<br>2666:SPD x 8 | SODIMM :260<br><br>MDx8: 78 | Type3-8L | IL |
| | Chapter 4.9 | LPDDR3 | MD 2R x32 | 2133 | SDP (1 x 32 die)<br>DDP (2 x 32 dies)<br>QDP (4 x 16 dies) | 178 | HDI 10L (3-x-3+) | NIL |

## Table 4-2. System Memory Interface Guideline Terminology and Descriptions

| CFL Processor and Memory Type | CFL-H | | | |
|---|---|---|---|---|
| | DDR4 SO-DIMM+ECC | DDR4 SO-DIMM no ECC | DDR4 Memory Down | LPDDR3 Memory Down |
| **Signal Group Details** | | | | |
| Clock (CLK) | CKN[3:0], CKP[3:0] | CKN[3:0], CKP[3:0] | CKN[1:0], CKP[1:0] | CKP[1:0], CKN[1:0] |
| Control (CTRL) | CS#[3:0], ODT[3:0] | CS#[3:0], ODT[3:0] | CS#[1:0], ODT[1:0] | CS#[1:0], ODT[0] |
| Clock Enable (CKE) | CKE[3:0] | CKE[3:0] | CKE[1:0] | CKE[3:0] |
| Command (CMD) | MA[16:0], BG[1:0], BA[1:0], ACT#, PAR | MA[16:0], BG[1:0], BA[1:0],ACT#, PAR | MA[16:0], BG[1:0], BA[1:0], ACT#, PAR | CAA[9:0], CAB[9:0] |
| Strobe | DQSP[7:0], DQSN[7:0] | DQSP[7:0], DQSN[7:0] | DQSP[7:0], DQSN[7:0] | DQS[7:0], DQS#[7:0] |
| ECC strobe | DQSP[8], DQSN[8] | N/A | N/A | N/A |
| Data | DQ[63:0] | DQ[63:0] | DQ[63:0] | DQ[63:0] |
| ECC Data | DQ[71:64] | N/A | N/A | N/A |
| Alert | ALERT# | ALERT# | ALERT# | N/A |
| Reset | DRAM_RESET# | DRAM_RESET# | DRAM_RESET# | N/A |
| RCOMP | DDR_RCOMP[2:0] | DDR_RCOMP[2:0] | DDR_RCOMP[2:0] | DDR_RCOMP[2:0] |
| **Guideline Terminology Descriptions** | | | | |
| Via Count | Motherboard Layer Signal Transition Via Placement Locations. At least one ground stitching via must be placed from every signal transition via when ever they change signal layers. | | | |
| Diff Spacing | Differential spacing between CK and CK# and between DQS and DQS# | | | |
| Group Spacing | Min self spacing and spacing between signals within the same signal group | | | |
| Group to Group Spacing | Min spacing between signals from the following different signal groups:<br>[1] CLK-CTRL, CLK-CKE, CLK-CMD, CLK-Reset CTRL-CKE, CTRL-CMD, CTRL-Reset, CKE-CMD, CKE-Reset<br>[2] CLK-Strobe, CLK-Data, CTRL-Strobe, CTRL-Data, CKE-Strobe, CKE-Data, CMD-Strobe, CMD-Data, Reset-Strobe, Reset-Data | | | |
| Byte Spacing | [1] Min spacing between strobe and data group signals within the same byte<br>[2] Min spacing between bytes within the same channel and between different channels | | | |
| DDR to Other Interfaces/Signals | The minimum spacing requirement for DDR to other signal/interfaces is 25mils. | | | |
| DDR Trace impedance and trace geometries | Impedance numbers are calculated according to the stack-up layers thickness, the material conductivity, traces spacing, width and dielectric constant and thickness.The controlling specification is the target trace impedance. It is allowed to change the signal trace width within design tolerance. It is strictly not recommended to reduce spacing between signals. Any spacing reduction can cause to performance degradation. | | | |
| Total max length | Total length refers to the signal trace length calculated from Processor die pad to each DRAM ball or each DIMM connector pin Which include Processor inner PKG trace length, Break-out, Main and Break-in trace segments of each DRAM | | | |

# 4.1 CFL-H DDR4 ECC SO-DIMM 2DPC Guidelines

## Table 4-3. System Memory Configuration Details Covered in this Section

| Parameter | Details |
|---|---|
| Processor | CFL-H |
| Memory Type | DDR4 |
| Configuration | Channel A = Two SO-DIMMs with ECC<br>Channel B = Two SO-DIMMs with ECC |
| Speed (MT/s) | 2400 |
| Channels | 1 and 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | 4 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | 64 |
| SO-DIMM Raw-Card Types | ECC DIMMs: RC-D(1Rx8),RC-G(2Rx8),RC-F(2Rx8),RC-H(2Rx8)<br>Non-ECC DIMMs: RC-A(1Rx8),RC-B(2Rx8),RC-E(2Rx8) |
| PCB Layers / Type [1] | 10L/T3 |
| DRAM Device Placement | Top & Bottom layers, each channel is dual sided, channels DIMMs placed back-to-back. |
| Processor Memory Ball Map [2] | Interleaved |
| DRAM Device ODT Capability [3] | Enable |
| Total Max Length | Strobe/Data/CTRL/CLK/CKE/CMD = PKG+BO1+BO2+M+BI<br>RCOMP = M |

***Notes:***

1. Type 3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias.
   Type 4 (T4) (1-x-1+) = PCB with one build-up layer and two layers of Micro-vias.
   Type 4 (T4) (2-x-2+) = PCB with two build-up layer and three layers of Micro-vias.
   See "Stack-Up and PCB Considerations" chapter for more details in this document.
2. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-by-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.
3. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

**Figure 4-1. CFL-H DDR4 ECC SO-DIMM 2DPC Block Diagram**

**Figure 4-2. CFL-H DDR4 ECC SO-DIMM 2DPC Block Placement**

## Figure 4-3. CFL-H DDR4 ECC SO-DIMM 2DPC Signals Topology

***Note:*** DRAM_RST CAP should no stuffed.

## Table 4-4. CFL-H DDR4 ECC SO-DIMM 2DPC Signal Routing Guidelines (Sheet 1 of 4)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max Length (mils) | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group [1]/[2] | Byte [1]/[2] | Region | Breakout [1,2] | Total | | |
| **CLK** Channel 0 | BO1 | MS | VSS/VCC | 1 | 3 | | | | 3 | 8 | 8/ | | 400 | [1] 500 | 4600 | | 1,2, 3,6 |
| | BO2 | SL | VSS | 0 | 3 | | | | 3 | 8 | 8/ | | 400 | | | | |
| | M | SL | VSS | 0 | 3.5 | 88 | | ±10 | 3.5 | 16 | 20/ | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | 4 | 10 | 10/ | | 300 | | | | |
| **CLK** Channel 1 | BO1 | MS | VSS/VCC | 1 | 3 | | | | 3 | 5 | 5/ | | 25 | [2] 700 | 4600 | | 1,2, 3,6 |
| | BO2a | SL | VSS | 0 | 3 | | | | 3 | 5 | 5/ | | 150 | | | | |
| | BO2b | SL | VSS | 0 | 3 | | | | 3 | 8 | 8/ | | 600 | | | | |
| | M | SL | VSS | 0 | 3.5 | 88 | | ±10 | 3.5 | 16 | 20/ | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | 4 | 10 | 10/ | | 300 | | | | |
| **CTRL CKE** Channel 0 | BO1 | MS | VSS/VCC | 1 | 3 | | | | | 3 | 5/10 | | 500 | [1] 600 | 4600 | | 1,2, 3 |
| | BO2 | SL | VSS | 0 | 3 | | | | | 5 | 5/10 | | 500 | | | | |
| | M | SL | VSS | 0 | 6 | | 40 | ±10 | | 12 | 12/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | | 4 | 12/25 | | 300 | | | | |

## Table 4-4. CFL-H DDR4 ECC SO-DIMM 2DPC Signal Routing Guidelines (Sheet 2 of 4)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max Length (mils) | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group [1]/[2] | Byte [1]/[2] | Region | Breakout [1,2] | Total | | |
| **CTRL CKE** Channel 1 | BO1 | MS | VSS/VCC | 1 | 3 | | | | | 3 | 5/10 | | 25 | [2] 700 | 4600 | | 1,2, 3 |
| | BO2a | SL | VSS | 0 | 3 | | | | | 3 | 5/10 | | 150 | | | | |
| | BO2b | SL | VSS | 0 | 3 | | | | | 4 | 5/10 | | 600 | | | | |
| | M | SL | VSS | 0 | 6 | | 40 | ±10 | | 12 | 12/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | | 4 | 12/25 | | 300 | | | | |
| **CMD** Channel 0 | BO1 | MS | VSS/VCC | 1 | 3 | | | | | 3 | 5/10 | | 500 | [1] 600 | 4600 | | 1,2, 3,10 |
| | BO2 | SL | VSS | 0 | 3 | | | | | 5 | 5/10 | | 500 | | | | |
| | M | SL | VSS | 0 | 7.5 | | 35 | ±10 | | 13.5 | 12/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | | 4 | 12/25 | | 300 | | | | |
| **CMD** Channel 1 | BO1 | MS | VSS/VCC | 1 | 3 | | | | | 3 | 5/10 | | 25 | [2] 700 | 4600 | | 1,2, 3,10 |
| | BO2a | SL | VSS | 0 | 3 | | | | | 3 | 5/10 | | 150 | | | | |
| | BO2b | SL | VSS | 0 | 3 | | | | | 4 | 5/10 | | 600 | | | | |
| | M | SL | VSS | 0 | 7.5 | | 35 | ±10 | | 13.5 | 12/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | | 4 | 12/25 | | 300 | | | | |
| **Strobe** Ch0 [7:0] | BO1 | MS | VSS | 1 | 3 | | | | 3 | | /10 | 4/25 | 300 | [1] 700 | 4600 | | 1,2, 3,4, 5,6, 10,1 1 |
| | BO2 | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 650 | | | | |
| | M | SL | VSS | 0 | 5.5 | 75 | | ±10 | 3.5 | | /25 | 12/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | 4 | | /25 | 8/25 | 300 | | | | |
| **Strobe** Ch1 [0] | BO1 | MS | VSS | 1 | 3 | | | | 3 | | /10 | 4/25 | 200 | [1] 450 | 4600 | | 1,2, 3,4, 5,6, 10,1 1 |
| | BO2 | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 350 | | | | |
| | M | SL | VSS | 0 | 5.5 | 75 | | ±10 | 3.5 | | /25 | 12/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | 4 | | /25 | 8/25 | 300 | | | | |
| **Strobe** Ch1[7:1] | BO1 | MS | VSS | 1 | 3 | | | | 3 | | /10 | 4/25 | 25 | [2] 750 | 4600 | | 1,2, 3,4, 5,6, 10,1 1 |
| | BO2a | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 600 | | | | |
| | BO2b | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 300 | | | | |
| | M | SL | VSS | 0 | 5.5 | 75 | | ±10 | 3.5 | | /25 | 12/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | 4 | | /25 | 8/25 | 300 | | | | |
| **Data** Ch0 Byte [7:0] | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | /10 | 4/25 | 300 | [1] 700 | 4600 | | 1,2, 3,4, 5,10 ,11 |
| | BO2 | SL | VSS | 0 | 3 | | | | | 3 | /10 | 5/25 | 650 | | | | |
| | M | SL | VSS | 0 | 5.5 | | 42 | ±10 | | 9 | /25 | 12/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | | 4 | /25 | 5/25 | 150 | | | | |
| **Data** Ch1 Byte [0] | BO1 | MS | VSS | 1 | 3 | | | | | 3 | /10 | 4/25 | 200 | [1] 450 | 4600 | | 1,2, 3,4, 5,10 ,11 |
| | BO2 | SL | VSS | 0 | 3 | | | | | 4.5 | /10 | 5/25 | 350 | | | | |
| | M | SL | VSS | 0 | 5.5 | | 42 | ±10 | | 9 | /25 | 12/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | | 4 | /25 | 8/25 | 150 | | | | |

## Table 4-4. CFL-H DDR4 ECC SO-DIMM 2DPC Signal Routing Guidelines (Sheet 3 of 4)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max Length (mils) | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group [1]/[2] | Byte [1]/[2] | Region | Breakout [1,2] | Total | | |
| **Data** Ch1 Byte [7:1] | BO1 | MS | VSS | 1 | 3 | | | | | 3 | /10 | 4/25 | 30 | [2] 550 | 4600 | | 1,2, 3,4, 5,10 ,11 |
| | BO2a | SL | VSS | 0 | 3 | | | | | 3 | /10 | 5/25 | 150 | | | | |
| | BO2b | SL | VSS | 0 | 3 | | | | | 5.5 | /10 | 5.5/ 25 | 500 | | | | |
| | M | SL | VSS | 0 | 5.5 | | 42 | ±10 | | 9 | /25 | 12/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | | 4 | /25 | 8/25 | 150 | | | | |
| **Strobe** Ch0 & Ch1 [8] | BO1 | MS | VSS | 1 | 3 | | | | 3 | | /10 | 4/25 | 200 | [1] 450 | 4600 | | 2,3, 4,5, 6,7, 8,10 ,11 |
| | BO2 | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 350 | | | | |
| | M | SL | VSS | 0 | 6.5 | 75 | | ±10 | 3.5 | | | 12/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | 4 | | /25 | 8/25 | 300 | | | | |
| **ECC** Ch0 & Ch1 | BO1 | MS | VSS | 1 | 3 | | | | | 3 | /10 | 4/25 | 200 | [1] 450 | 4600 | | 1,2, 3,4, 5,7, 8,10 ,11 |
| | BO2 | SL | VSS | 0 | 3 | | | | | 4.5 | /10 | 5/25 | 350 | | | | |
| | M | SL | VSS | 0 | 6.5 | | 42 | ±10 | | 9 | | 12/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | | 4 | /25 | 8/25 | 300 | | | | |
| **Alert** | BO1 | MS | VSS/VCC | 1 | 3 | | | | | 3.5 | 5/10 | | 350 | [1] 600 | 4600 | | 1,2, 3 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4.5 | 5/10 | | 500 | | | | |
| | M | SL | VSS | 0 | 7.5 | | 35 | ±10 | | 13.5 | 12/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | | 4 | 12/25 | | 300 | | | | |
| **Reset** | BO1 | MS | VSS/VCC | 1 | 4 | | 50 | ±10 | | | 4/4 | | 30 | | 8000 | (R1) 470 (R2) 0 (C1) 0.1 | 3,9 |
| | BO2 | MS | VSS/VCC | 0 | 4 | | 50 | ±10 | | | 4/4 | | 1000 | | | | |
| | | SL | VSS | 0 | 3.5 | | 50 | ±10 | | | 4/4 | | | | | | |
| | M | MS | VSS/VCC | 0 | 4 | | 50 | ±10 | | | 4/4 | | | | | | |
| | | SL | VSS | 0 | 3.5 | | 50 | ±10 | | | 4/4 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | 50 | ±10 | | | 4/4 | | | | | | |
| **RCOMP [0]** | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25/25 | | | | 500 | 121 | |
| **RCOMP [1]** | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25/25 | | | | 500 | 75 | |
| **RCOMP [2]** | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25/25 | | | | 500 | 100 | |

## Table 4-4. CFL-H DDR4 ECC SO-DIMM 2DPC Signal Routing Guidelines (Sheet 4 of 4)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max Length (mils) | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group [1]/[2] | Byte [1]/[2] | Region | Breakout [1,2] | Total | | |

***Note:***

2. The Channel A CLK/CTRL/CKE/CMD/Strobe/Data/Alert signals all should route on the same inner layer together and they should not route on the same inner layer or an adjacent layer as any of the Channel B CLK/CTRL/CKE/CMD/Strobe/Data/Alert signals. The Channel B CLK/CTRL/CKE/CMD/Strobe/Data/Alert signals all should route on the same inner layer together and they should not route on the same inner layer or an adjacent layer as any of the Channel A CLK/CTRL/CKE/CMD/Strobe/Data/Alert signals. It is possible to spread the routing to another layer as long as the customer meets all impedance and crosstalk parameters in line with other signals which are routed in alternate layers. Within byte signals should be routed in the same layer and channels should be routed in separate layers. Propagation delay matching within groups/bytes should be kept.
3. The Max Breakout Length = BO1+BO2 [1] or BO1+(BO2a + BO2b) [2] where specified
4. Signals while routed on inner PCB layers must be ground referenced with solid ground floods on both sides.
5. The Strobe and Data Group Signals within the same byte must route together for their entire route from CPU Ball to DIMM Pin.
6. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Utilizing this capability enables a modified SO-DIMM pin map and places common SO-DIMM pins in overlapping positions on the top and bottom layers of the motherboard. It also reduces the Data and Strobe signal T-Topology Break-In (BI) segment lengths, it helps eliminate serpentine routing, and creates more room for ground vias next to every Data and Strobe signal transition via in the SO-DIMM pin field area.
7. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.
8. ECC signals should be routed in separate layer than other DDR (DQ/Strobe/CLK/CTRL/CKE/CMD) signals.
9. Parallel routing over ECC signals within DSL layers is not allowed. Vertical routing of low frequency over ECC signals is allowed.
10. Capacitor C1 is a defensive design and should be NO STUFF by default.
11. Although BI max length is 300 mils, the recommendation is to reduce BI length as possible.
12. DQ and DQS signals must route at the same layer and have same width

## Table 4-5. CFL-H DDR4 ECC SO-DIMM Length and Matching Guidelines

| Signal Group | Rule Details | Length Matching (mils) | | Notes |
|---|---|---|---|---|
| | | Min | Max | |
| **CLK** | CK[X] - CK#[X], where X = 0 or 1 | -5 | 5 | 1,2 |
| | CK/CK#[1:0] (max - min) | 0 | 40 | 1,2 |
| **CTRL/CKE** | CTRL/CKE (max - min) | 0 | 200 | 1,2 |
| | CK/CK#[1:0] - CTRL/CKE | 0 | 100 | 1,2 |
| **CMD** | CMD (max - min) | 0 | 200 | 1,2 |
| | CK/CK#[1:0] - CMD | -500 | 500 | 1,2 |
| **Strobe** | DQS[X] - DQS#[X], where X = 0 to 8 | -5 | 5 | 1,2 |
| | CK/CK#[1:0] - DQS/DQS#[X], where X = 0 to 8 | -1500 | 2500 | 1,2 |
| **Data** | DQ(Byte[X]) - DQS/DQS#[X], where X 0 to 7<br>ECC(7:0) - DQS/DQS#[8] | -20 | 20 | 1,2,3 |

***Notes:***

1. Length Matching = CPU Die to SO-DIMM Pin (PKG + BO1 + BO2 + M + BI, PKG + BO1 +BO2a + BO2b + M + BI); where a conversion factor of 0.9 must be used on Micro-Strip Segments to convert Micro-Strip lengths to Strip-Line equivalent lengths
2. To help facilitate and check the Length and Matching relationships on a design please reference the Coffee Lake Platform System Memory Automated Trace Lengths Calculator (ATLC) -#568458
3. Byte[0] = DQ[7:0], DQS/DQS#[0], Byte[1] = DQ[15:8], DQS/DQS#[1], Byte[2] = DQ[23:16], DQS/DQS#[2], Byte[3] = DQ[31:24], DQS/DQS#[3], Byte[4] = DQ[39:32], DQS/DQS#[4], Byte[5] = DQ[47:40], DQS/DQS#[5], Byte[6] = DQ[55:48], DQS/DQS#[6], Byte[7] = DQ[63:56], DQS/DQS#[7]

### 4.1.1 Stub Reduction and Alternative Pin Map

Current SO-DIMM pin assignments are defined by JEDEC spec, same pin assignment is used for both DIMMs. This combination creates stubs of up to 300 mils on the surface routing layers. (See Figure 4-10).

DDR interface allows for data bits to be swizzled within a byte group. Utilizing this capability enables a modified pin map for the second SO-DIMM on each channel that places common pins in overlapping positions on the top and bottom layers of the motherboard. The modified DIMM pin map reduces surface layers stubs on data signals stubs from up to 300 mils to less than 60 mils, resulting in an Eye Width/Eye Height improvement. This modified DIMM pin map also eliminates the need for complex length matching of surface stub lengths and reduces overall routing length of data and strobe signals. This new Pin map allows the data vias to be spaced wider apart, creating space for extra VSS stitching vias and reduction of 3D crosstalk.

**Figure 4-4. Stubs on 2 DIMMs Per Channel Configurations**

## 4.2 CFL-H DDR4 SO-DIMM 2DPC Guidelines

**Table 4-6. System Memory Configuration Details Covered in this Section (Sheet 1 of 2)**

| Parameter | Details |
|---|---|
| Processor | CFL-H |
| Memory Type | DDR4 |
| Configuration | Channel A = Two SO-DIMMs<br>Channel B = Two SO-DIMMs |
| Speed (MT/s) | 2400 |
| Channels | 1 and 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | 4 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | 64 |
| SO-DIMM Raw-Card Types | RC-A (1Rx8), RC-B (2Rx8), RC-E(2Rx8) |
| PCB Layers / Type [1] | 8L/T3 |
| DRAM Device Placement | 2DPC using T-Topology.<br>SODIMMs connectors on Top & Bottom layers, each channel is dual sided,<br>Channels DIMMs placed back-to-back. |

## Table 4-6. System Memory Configuration Details Covered in this Section (Sheet 2 of 2)

| Parameter | Details |
|---|---|
| Processor Memory Ball Map [2] | Interleaved |
| DRAM Device ODT Capability [3] | Enable |
| Total Max Length | Strobe/Data/CTRL/CLK/CKE/CMD = PKG+BO1+BO2+M+BI<br>RCOMP = M |

***Notes:***

1. Type 3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias.
   Type 4 (T4) (1-x-1+) = PCB with one build-up layer and two layers of Micro-vias.
   Type 4 (T4) (2-x-2+) = PCB with two build-up layer and three layers of Micro-vias.
   See "Stack-Up and PCB Considerations" chapter for more details in this document.
2. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-by-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.
3. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

## Figure 4-5. CFL-H DDR4 SO-DIMM 2DPC Block Diagram

**Figure 4-6. CFL-H DDR4 SO-DIMM 2DPC Block Placement**

**Figure 4-7. CFL-H DDR4 SO-DIMM 2DPC Signals Topology**

***Note:*** DRAM_RST CAP should no stuffed.

For CFL-H DDR4 2DPC SODIMM Signals Routing Guidelines table refer to Table 4-4, "CFL-H DDR4 ECC SO-DIMM 2DPC Signal Routing Guidelines", Please ignore ECC guidelines.

For CFL-H DDR4 2DPC SODIMM Lengths and Matching Guidelines Table refer to Table 4-5, "CFL-H DDR4 ECC SO-DIMM Length and Matching Guidelines", Please ignore ECC guidelines.

## 4.3 CFL-H DDR4 SO-DIMM 1DPC Guidelines

### Table 4-7. System Memory Configuration Details Covered in this Section

| Parameter | Details |
|---|---|
| Processor | CFL-H |
| Memory Type | DDR4 |
| Configuration | Channel A = One SO-DIMMs<br>Channel B = One SO-DIMMs |
| Speed (MT/s) | 2400/2666 |
| Channels | 1 and 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | 2 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | 32 |
| SO-DIMM Raw-Card Types | 2666:<br>RC-A (1Rx8), RC-E(2Rx8),RC-C (1Rx16)<br>2400:<br>RC-B (2Rx8) |
| PCB Layers / Type [1] | 8L/T3 |
| DRAM Device Placement | Single side Top layer, OR dual side placement |
| Processor Memory Ball Map [2] | Interleaved |
| DRAM Device ODT Capability [3] | Enable |
| Total Max Length | Strobe/Data/CTRL/CLK/CKE/CMD = PKG+BO1+BO2+M+BI<br>RCOMP = M |

***Notes:***

1. Type 3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias.
   Type 4 (T4) (1-x-1+) = PCB with one build-up layer and two layers of Micro-vias.
   Type 4 (T4) (2-x-2+) = PCB with two build-up layer and three layers of Micro-vias.
   See "Stack-Up and PCB Considerations" chapter for more details in this document.
2. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-by-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.
3. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

**Figure 4-8. CFL-H DDR4 SO-DIMM 1DPC Block Diagram**

**Figure 4-9. CFL-H DDR4 SO-DIMM 1DPC Block Placement**

For CFL H DDR4 SO-DIMM 1DPC Signal Topology refer to Figure 4-7, "CFL-H DDR4 SO-DIMM 2DPC Signals Topology".

## Table 4-8. CFL-H DDR4 SO-DIMM 1DPC Signal Routing Guidelines (Sheet 1 of 2)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max Length (mils) | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group [1]/[2] | Byte [1]/[2] | Region | Breakout [1,2] | Total | | |
| **CLK** Channel 0 | BO1 | MS | VSS/VCC | 1 | 3 | | | | 3.5 | 8 | 8/10 | | 400 | [1] 500 | 4600 | | 1,2, 3,6 |
| | BO2 | SL | VSS | 0 | 3 | | | | 3 | 8 | 8/10 | | 200 | | | | |
| | M | SL | VSS | 0 | 3.5 | 88 | | ±10 | 3.5 | 16 | 16/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | 4 | 16 | 16/25 | | 300 | | | | |
| **CLK** Channel 1 | BO1 | MS | VSS/VCC | 1 | 3 | | | | 3.5 | 8 | 8/10 | | 25 | [1] 620 | 4600 | | 1,2, 3,6 |
| | BO2 | SL | VSS | 0 | 3 | | | | 3 | 8 | 8/10 | | 610 | | | | |
| | M | SL | VSS | 0 | 3.5 | 88 | | ±10 | 3.5 | 16 | 16/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | 4 | 16 | 16/25 | | 300 | | | | |
| **CTRL CKE CMD** Channel 0 | BO1 | MS | VSS/VCC | 1 | 3 | | | | | 3.5 | 5/10 | | 350 | [1] 600 | 4600 | | 1,2, 3 |
| | BO2 | SL | VSS | 0 | 3 | | | | | 5 | 5/10 | | 500 | | | | |
| | M | SL | VSS | 0 | 6 | | 40 | ±10 | | 12 | 16/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | | 4 | 16/25 | | 300 | | | | |
| **CTRL CKE CMD** Channel 1 | BO1 | MS | VSS/VCC | 1 | 3 | | | | | 3.5 | 5/10 | | 25 | [2] 700 | 4600 | | 1,2, 3 |
| | BO2a | SL | VSS | 0 | 3 | | | | | 3 | 5/10 | | 150 | | | | |
| | BO2b | SL | VSS | 0 | 3 | | | | | 5.5 | 5/10 | | 600 | | | | |
| | M | SL | VSS | 0 | 6 | | 40 | ±10 | | 12 | 16/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | | 4 | 16/25 | | 300 | | | | |
| **Strobe** Ch0 [7:0] | BO1 | MS | VSS | 1 | 3 | | | | 3.5 | | /10 | 4/25 | 300 | [1] 700 | 4600 | | 1,2, 3,4, 5,,8 6 |
| | BO2 | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 650 | | | | |
| | M | SL | VSS | 0 | 3.5 | 88 | | ±10 | 3.5 | | /25 | 16/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | 4 | | /25 | 5/25 | 300 | | | | |
| **Strobe** Ch1 [0] | BO1 | MS | VSS | 1 | 3 | | | | 3.5 | | /10 | 4/25 | 300 | [1] 450 | 4600 | | 1,2, 3,4, 5,6, 8 |
| | BO2 | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 350 | | | | |
| | M | SL | VSS | 0 | 3.5 | 88 | | ±10 | 3.5 | | /25 | 16/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | 4 | | /25 | 5/25 | 300 | | | | |
| **Strobe** Ch1 [7:1] | BO1 | MS | VSS | 1 | 3 | | | | 3.5 | | /10 | 4/25 | 25 | [2] 750 | 4600 | | 1,2, 3,4, 5,6, 8 |
| | BO2a | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 600 | | | | |
| | BO2b | SL | VSS | 0 | 3 | | | | 3 | | /10 | 5/25 | 300 | | | | |
| | M | SL | VSS | 0 | 3.5 | 88 | | ±10 | 3.5 | | /25 | 16/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | 4 | | /25 | 5/25 | 300 | | | | |
| **Data** Ch0 Byte [7:0] | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | /10 | 4/25 | 300 | [1] 700 | 4600 | | 1,2, 3,4, 5,8 |
| | BO2 | SL | VSS | 0 | 3 | | | | | 3 | /10 | 5/25 | 650 | | | | |
| | M | SL | VSS | 0 | 3.5 | | 50 | ±10 | | 8 | /25 | 16/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | | 4 | /25 | 5/25 | 300 | | | | |
| **Data** Ch1 Byte [0] | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | /10 | 4/25 | 300 | [1] 450 | 4600 | | 1,2, 3,4, 5,8 |
| | BO2 | SL | VSS | 0 | 3 | | | | | 4.5 | /10 | 5/25 | 350 | | | | |
| | M | SL | VSS | 0 | 3.5 | | 50 | ±10 | | 8 | /25 | 16/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | | 4 | /25 | 5/25 | 300 | | | | |

## Table 4-8. CFL-H DDR4 SO-DIMM 1DPC Signal Routing Guidelines (Sheet 2 of 2)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max Length (mils) | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group [1]/[2] | Byte [1]/[2] | Region | Breakout [1,2] | Total | | |
| **Data** Ch1 Byte [7:1] | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | /10 | 4/25 | 25 | [2] 750 | 4600 | | 1,2, 3,4, 5,8 |
| | BO2a | SL | VSS | 0 | 3 | | | | | 3 | /10 | 5/25 | 600 | | | | |
| | BO2b | SL | VSS | 0 | 3 | | | | | 5.5 | /10 | 5.5/25 | 300 | | | | |
| | M | SL | VSS | 0 | 3.5 | | 50 | ±10 | | 8 | /25 | 16/25 | | | | | |
| | BI | MS | VSS | 1 | 4 | | | | | 4 | /25 | 5/25 | 300 | | | | |
| **Alert** | BO1 | MS | VSS/VCC | 1 | 3 | | | | | 3.5 | 5/10 | | 30 | [2] 750 | 4600 | | 1,2, 3, |
| | BO2a | SL | VSS | 0 | 3 | | | | | 3 | 5/10 | | 500 | | | | |
| | BO2b | SL | VSS | 0 | 3.5 | | | | | 5 | 5/10 | | 200 | | | | |
| | M | SL | VSS | 0 | 6 | | 40 | ±10 | | 12 | 16/25 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | | | | 4 | 16/25 | | 300 | | | | |
| **Reset** | BO1 | MS | VSS/VCC | 1 | 4 | | 50 | ±10 | | | 4/4 | | 30 | | 8000 | (R1) 470 (R2) 0 (C1) 0.1 | 3,7 |
| | BO2 | MS | VSS/VCC | 0 | 4 | | 50 | ±10 | | | 4/4 | | 1000 | | | | |
| | | SL | VSS | 0 | 3.5 | | 50 | ±10 | | | 4/4 | | | | | | |
| | M | MS | VSS/VCC | 0 | 4 | | 50 | ±10 | | | 4/4 | | | | | | |
| | | SL | VSS | 0 | 3.5 | | 50 | ±10 | | | 4/4 | | | | | | |
| | BI | MS | VSS/VCC | 1 | 4 | | 50 | ±10 | | | 4/4 | | | | | | |
| **RCOMP [0]** | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25/25 | | | | 500 | 121 | |
| **RCOMP [1]** | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25/25 | | | | 500 | 75 | |
| **RCOMP [2]** | M | MS | VSS | 2 | 12-15 | | | | | 20 | 25/25 | | | | 500 | 100 | |

***Notes:***

1. The Channel A CLK/CTRL/CKE/CMD/Strobe/Data signals all must route on the same inner layer together and they must not route on the same inner layer or an adjacent layer as any of the Channel B CLK/CTRL/CKE/CMD/Strobe/Data signals. The Channel B CLK/CTRL/CKE/CMD/Strobe/Data signals all must route on the same inner layer together and they must not route on the same inner layer or an adjacent layer as any of the Channel A CLK/CTRL/CKE/CMD/Strobe/Data signals.
2. The Max Breakout Length = BO1+BO2 [1] or BO1+(BO2a + BO2b) [2] where specified
3. Signals while routed on inner PCB layers must be ground referenced with solid ground floods on both sides.
4. The Strobe and Data Group Signals within the same byte must route together for their entire route from CPU Ball to DIMM Pin.
5. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Utilizing this capability enables a modified SO-DIMM pin map and places common SO-DIMM pins in overlapping positions on the top and bottom layers of the motherboard. It also reduces the Data and Strobe signal T-Topology Break-In (BI) segment lengths, it helps eliminate serpentine routing, and creates more room for ground vias next to every Data and Strobe signal transition via in the SO-DIMM pin field area.
6. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

7. Capacitor C1 is a defensive design and should be NO STUFF by default
8. DQ and DQS signals must route at the same layer and have same width

For CFL-H DDR4 SO-DIMM Length and Matching Guidelines refer to Table 4-5, "CFL-H DDR4 ECC SO-DIMM Length and Matching Guidelines".

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## 4.4 CFL H DDR4 ECC SO-DIMM 1DPC guidelines

### Table 4-9. System Memory Configuration Details Covered in this Section

| Parameter | Details |
|---|---|
| Processor | CFL-H |
| Memory Type | DDR4 |
| Configuration | Channel A = One SO-DIMMs<br>Channel B = One SO-DIMMs |
| Speed (MT/s) | 2400/2666 |
| Channels | 1 and 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | 2 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | 32 |
| SO-DIMM Raw-Card Types | ECC DIMMs:<br>2666:<br>RC-D(1Rx8),RC-G(2Rx8),RC-F(2Rx8)<br>2400:<br>RC-H(2Rx8)<br><br>Non-ECC DIMMs:<br>2666:<br>RC-A(1Rx8), RC-E(2Rx8),RC-C (1Rx16)<br>2400:<br>RC-B(2Rx8) |
| PCB Layers / Type [1] | 10L/T3 |
| DRAM Device Placement | Single side Top layer, OR dual side placement |
| Processor Memory Ball Map [2] | Interleaved |
| DRAM Device ODT Capability [3] | Enable |
| Total Max Length | Strobe/Data/CTRL/CLK/CKE/CMD = PKG+BO1+BO2+M+BI<br>RCOMP = M |

***Notes:***

1. Type 3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias.
   Type 4 (T4) (1-x-1+) = PCB with one build-up layer and two layers of Micro-vias.
   Type 4 (T4) (2-x-2+) = PCB with two build-up layer and three layers of Micro-vias.
   See "Stack-Up and PCB Considerations" chapter for more details in this document.
2. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-by-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.
3. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

For all signals, exclude ECC, please follow Chapter 4, "CFL-H DDR4 SO-DIMM 1DPC Guidelines".

ECC guidelines are similar to DQ/DQS in Chapter 4, "CFL-H DDR4 SO-DIMM 1DPC Guidelines".

ECC signals to be routed at separated layer than other DDR signals.

For CFL-H DDR4 1DPC ECC SODIMM Lengths and Matching Guidelines Table refer to Table 4-5, "CFL-H DDR4 ECC SO-DIMM Length and Matching Guidelines", Please ignore ECC guidelines.

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## 4.5 CFL-H DDR4 1R x16 Memory Down Guidelines

### Table 4-10. System Memory Configuration Details Covered in this Section

| Parameter | Details |
|---|---|
| Processor | CFL-H |
| Memory Type | DDR4 |
| Configuration | Channel A = x16 Memory Down (4 DRAM Devices)<br>Channel B = x16 Memory Down (4 DRAM Devices) |
| Speed (MT/s) | 2666 |
| Channels | 1 and 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | 1 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | SDP - 8<br>DDP - 16 |
| Memory Down Types [1] [2]<br>(Pkg Ranks - Die Bits - Pkg bits) | 96-Ball BGA<br>SDP 1-16-16<br>DDP 1-8-16<br>Not for a common SDP/DDP board |
| PCB Layers / Type [3] | 10L/T3 |
| DRAM Device Placement | Each Channel is Single Sided, Channels are Side by Side Placement |
| CPU System Memory Ball Map [4] | Non-Interleaved |
| DRAM Device ODT Capability [5] | Enabled |
| Total Max Length | Strobe/Data/Reset = PKG+BO+M+BI<br>CLK/CTRL/CKE/CMD= PKG+BO+M+BI1+BI2<br>RCOMP = M |

***Notes:***

1. SDP: Single Die Package, DDP: Dual Die Package
2. No mixed vendor support within a channel or channel to channel and No mixed memory DRAM down type support (SDP, DDP) within a channel or channel to channel
3. Type 3 = PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias. See "Stack-Up and PCB Considerations" chapter for more details.
4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-By-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.
5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

**Figure 4-10. CFL-H DDR4 1Rx16 Memory Down Placement and Block Diagram**

**Figure 4-11. CFL-H DDR4 1Rx16 Memory Down Strobe/Data/RCOMP Signal Topologies**

## Figure 4-12. CFL-H DDR4 1Rx16 Memory Down CLK/CTRL/CKE/CMD/Reset Signal Topology

***Notes:***

1. The alert signal must be routed in the opposite direction to the address/command bus. For example, the alert signal must first connect to the last device that the address/command bus is connected to.
2. DRAM_RST CAP should no stuffed.
3. For SDP BG1 should be left open
4. For DDP BG1 Should be connected to the DRAM.

## Table 4-11. CFL-H DDR4 1Rx16 Memory Down Routing Guideline (Sheet 1 of 3)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Breakout | Total | | |
| CLK | BO1 | MS | VSS | 1 | 3 | | | | 3.5 | 3.5 | 3.5 | | 450 | 800 | [1st] 6000 [Last] 8000 | (R1) 36 (C1-no stuff) 0.0033 (C2) 0.01 | 1,2, 3, 7,8 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | 4 | 16 | 16 | | 700 | | | | |
| | M1 | SL | VSS | 0 | 6/6.5 | 72 | 40 | ±10 | 4.5 | 16 | 16 | | | | | | |
| | M2 | SL | VSS | 0 | 5/5.5 | | | | 4.5/ 4 | 16 | 16 | | 1000 | | | | |
| | BI1 | SL | VSS | 8 | 3 | | | | 3.5 | 16 | 16 | | 150 | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | 85 | | ±10 | 4.5 | 16 | 16 | | 700 | | | | |
| | T1 | MS | VSS | 1 | 3 | | | | 3.5 | 16 | 16 | | 200 | | | | |
| | T2 | SL | VSS | 0 | 4.5 | 85 | | ±10 | 4.5 | 16 | 16 | | 300 | | | | |
| | T3 | MS | VSS | 1 | 3 | | | | 3.5 | 16 | 16 | | 50 | | | | |
| CTRL/ CKE | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | 3.5 | | 450 | 800 | [1st] 6000 [Last] 8000 | 36 | 1,2, 3 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4 | 16 | | 700 | | | | |
| | M | SL | VSS | 0 | 5.5/7 | | 40 | ±10 | | 5/6 | 16 | | | | | | |
| | BI1 | MS | VSS | 8 | 3 | | | | | 3.5 | 16 | | 150 | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 700 | | | | |
| | T2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 300 | | | | |
| | T3 | MS | VSS | 1 | 3 | | | | | 3.5 | 16 | | 50 | | | | |
| CMD | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | 3.5 | | 450 | 800 | [1st] 6000 [Last] 8000 | 36 | 1,2, 3 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4 | 16 | | 700 | | | | |
| | M | SL | VSS | 0 | 5.5/7 | | 40 | ±10 | | 4.5/ 5.5 | 16 | | | | | | |
| | BI1 | MS | VSS | 8 | 3 | | | | | 3.5 | 16 | | 150 | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 700 | | | | |
| | T2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 300 | | | | |
| | T3 | MS | VSS | 1 | 3 | | | | | 3.5 | 16 | | 50 | | | | |

## Table 4-11. CFL-H DDR4 1Rx16 Memory Down Routing Guideline (Sheet 2 of 3)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Breakout | Total | | |
| Strobe | BO1 | MS | VSS | 1 | 3 | | | | 3.5 | | 3.5 | 3.5 | 450 | 800 | 4500 | | 1,2, 4,5, 6,7, 9,10 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | 4 | | 16 | 25 | 700 | | | | |
| | M | SL | VSS | 0 | 4/4.5 | 85 | | ±10 | 4.5 | | 16 | 25 | | | | | |
| | BI1 | SL | VSS | 1 | 3 | | | | 3.5 | | 16 | 25 | 150 | | | | |
| Data | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | 3.5 | 3.5 | 450 | 800 | 4500 | | 1,2, 4,5, 6,9, 10 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4 | 16 | 25 | 700 | | | | |
| | M | SL | VSS | 0 | 4/4.5 | | 50 | ±10 | | 4.5/ 5.5 | 16 | 25 | | | | | |
| | BI1 | SL | VSS | 1 | 3 | | | | | 3.5 | 16 | 25 | 150 | | | | |
| Alert | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | 3.5 | | 450 | 800 | [1st] 6000 [Last] 8000 | (R1 connected to VDDQ) 50 | 1,2, 3 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4 | 16 | | 700 | | | | |
| | M | SL | VSS | 0 | 4/4.5 | | 50 | ±10 | | 4.5/ 5.5 | 16 | | | | | | |
| | BI1 | MS | VSS | 0 | 3 | | | | | 3.5 | 16 | | 150 | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 700 | | | | |
| | T2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 300 | | | | |
| | T3 | MS | VSS | 1 | 3 | | | | | 3.5 | 16 | | 50 | | | | |
| Reset | BO1 | MS | VSS | 1 | 3 | | | | | | 3.5 | | 30 | 1000 | 8000 | (R1) 470 (R2) 0 (C1) 0.1 | 3,8 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | | 20 | | 1000 | | | | |
| | M | SL | VSS | 1 | 4/4.5 | | 50 | ±10 | | | 20 | | | | | | |
| | BI1 | MS | VSS | 8 | 3 | | | | | | 20 | | | | | | |
| | BI2 | MS | VSS | 0 | 4.5 | | 50 | ±10 | | | 20 | | | | | | |
| RCOMP [0] | M | MS | VSS | 4 | 12-15 | | | | | 13 | 13 | | 500 | | 500 | 121 | 12 |
| RCOMP [1] | M | MS | VSS | 4 | 12-15 | | | | | 13 | 13 | | 500 | | 500 | 121 | 13 |
| RCOMP [2] | M | MS | VSS | 4 | 12-15 | | | | | 13 | 13 | | 500 | | 500 | 100 | |

## Table 4-11. CFL-H DDR4 1Rx16 Memory Down Routing Guideline (Sheet 3 of 3)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Breakout | Total | | |

***Notes:***

1. Avoid any parallel routing between two adjacent layers. When parallel routing can not be avoided in the CPU Break Out, it is recommended to offset the signals from two adjacent layers so no direct overlap occurs. If needed, the total parallel routing length in the CPU Break Out, which includes both overlapped and offset parallel routing, must be 300 mils or less.
2. Signals while routed on inner PCB layers must be ground referenced with solid ground floods on both sides.
3. Use individual termination resistors (R1) for each signal. Don't use Rpacks
4. For Option #1 (Single Rank) configuration there are only 8 DRAM Devices connected to each CMD Group Signal and only 1 DRAM Device connected to each Strobe/Data Group Signal. For these designs DRAM Devices [15:8] and their corresponding BI1 routing segments need to be removed for each CMD Group Signal and the second DRAM Device and corresponding BI routing segment needs to be removed for each Strobe/Data Group Signal.
5. The Strobe and Data Group Signals within the same byte must always route together on the same layers for their entire route
6. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel
7. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed
8. Capacitor C1 is a defensive design and should be NO STUFF by default
9. DQ and DQS signals must route at the same layer and have same width
10. Route 2 adjacent bytes to same DRAM device - like DRAM0(BYTE0,1) DRAM1 (BYTE 2,3),,, for better VREF training per DRAM device.
11. Impedance numbers are for reference only, it is calculating according to the stackup layers thickness, the material conductivity, traces spacing and width. The recommendation is to follow stackup and traces geometries.
12. RCOMP[1] value for Mix SoDIMM and MD topology should be 75 Ohm

## Table 4-12. CFL-H DDR4 1Rx16 Memory Down Length Matching Guidelines (Sheet 1 of 2)

| Signal Group | Rule Details | Length Matching (mils) | | Notes |
|---|---|---|---|---|
| | | Min | Max | |
| **CLK** | BI1 (max - min) | 0 | 50 | 2 |
| | CK[X] - CK#[X]; where X = 0 or 1 | -5 | 5 | 1,2 |
| | CK/CK#[1:0] (max - min) | 0 | 10 | 1,2 |
| **CTRL/CKE** | BI1 (max - min) | 0 | 0 | 2,4 |
| | CTRL/CKE (max - min) | 0 | 100 | 1,2 |
| | CK/CK#[X] - CTRL/CKE; where X = 0 or 1 | 0 | 100 | 1,2,6 |
| **CMD** | BI1 (max - min) | 0 | 0 | 2,4 |
| | CMD (max - min) | 0 | 100 | 1,2 |
| | CK/CK#[0] - CMD; where X = 0 or 1 | -500 | 500 | 1,2,6 |
| **Strobe** | BI1 (max – min) | 0 | 0 | 2,5 |
| | DQS[X] - DQS#[X], where X = 0 to 7 | -5 | 5 | 1,2 |
| | CK/CK#[X] - DQS/DQS#[Y], where X = 0 or 1 and Y = 0 to 7 | -500 | 3500 | 1,2 |
| **Data** | BI(max-min) | 0 | 0 | 2,5 |
| | DQ(Byte[X]) - DQS/DQS#[X], where X = 0 to 7 | -20 | 20 | 1,2,3 |

### Table 4-12. CFL-H DDR4 1Rx16 Memory Down Length Matching Guidelines (Sheet 2 of 2)

***Notes:***

1. Length Matching = CPU Die to DRAM Ball of every DRAM Device (CLK = PKG+BO1+BO2+M1+M2+BI1+BI2, CTRL/CKE/CMD = PKG+BO1+BO2+M+BI1+BI2, Strobe/Data = PKG+BO1+BO2+M+BI1); where a conversion factor of 0.9 must be used on Micro-Strip Segments to convert Micro-Strip lengths to Strip-Line equivalent lengths
2. To help facilitate and check the Length and Matching relationships on a design please reference the Coffee Lake Platform System Memory Automated Trace Lengths Calculator (ATLC) -#568458
3. Byte[0] = DQ[7:0], DQS/DQS#[0], Byte[1] = DQ[15:8], DQS/DQS#[1], Byte[2] = DQ[23:16], DQS/DQS#[2], Byte[3] = DQ[31:24], DQS/DQS#[3], Byte[4] = DQ[39:32], DQS/DQS#[4], Byte[5] = DQ[47:40], DQS/DQS#[5], Byte[6] = DQ[55:48], DQS/DQS#[6], Byte[7] = DQ[63:56], DQS/DQS#[7]
4. CMD/CTRL BI matching:this matching rule refer to all BI (Break-ins) sections that routed within each signal.For example:ADDR[0]/[1] BI1 shoudl be equal in all DRAMs.ADDR[0] BI1 may be equal to ADDR[1] BI1.
5. DQ/DQS matching rules:DQ - BI should be matched within all bytes and not only within byte (max-min=0). DQ[63..0] BI section should be equal. DQS - BI should be matched within all bytes and not only within bytes (max-min=0).DQS[7..0][P/N] BI section should be equal.DQ and DQS BI does not need to be matched.
6. The delta between CLK signals to CMD/CTRL/CKE, between DRAMs should be kept < 20mils. For exp: |DRAM[x] (CK[i]-Addr[j]) - DRAM[y](CK[i]-Addr[j])| < 20mils.

## 4.6 CFL-H DDR4 2R x8 Memory Down Guidelines

### Table 4-13. System Memory Configuration Details Covered in this Section

| Parameter | Details |
|---|---|
| Processor | CFL-H |
| Memory Type | DDR4 |
| Configuration | Channel A = x8 Memory Down (16 DRAM Devices for 2Ranks)<br>Channel B = x8 Memory Down (16 DRAM Devices for 2Ranks) |
| Speed (MT/s) | 2666 |
| Channels | 1 and 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | 2 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | 32 |
| Memory Down Types [1] [2]<br>(Pkg Ranks - Die Bits - Pkg bits) | 78-Ball BGA<br>SDP 1-8-8 |
| PCB Layers / Type [3] | 10L/T3 |
| DRAM Device Placement | Each Channel is Dual Sided,<br>Channels are Side by Side Placement |
| CPU System Memory Ball Map [4] | Non-Interleaved |
| DRAM Device ODT Capability [5] | Enabled |
| Total Max Length | Strobe/Data = PKG+BO1+BO2+M+BI1<br>Reset = PKG+BO1+BO2+M+BI1+BI2<br>CLK = PKG+BO1+BO2+M1+M2+BI1+BI2<br>CTRL/CKE/CMD= PKG+BO1+BO2+M+BI1+BI2<br>RCOMP = M |

***Notes:***

1. SDP: Single Die Package, DDP: Dual Die Package
2. No mixed vendor support within a channel or channel to channel and No mixed memory DRAM down type support (SDP, DDP) within a channel or channel to channel
3. Type 3 = PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias. See "Stack-Up and PCB Considerations" chapter for more details.

4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-By-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.
5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

## Figure 4-13. CFL-H DDR4 x8 Memory Down Placement and Block Diagram

## Figure 4-14. CFL-H DDR4 x8 Memory Down CLK/CKE/CMD/CTRL/ALERT/Reset Signals Topologies

***Notes:***

1. The alert signal must be routed in the opposite direction to the address/command bus. For example, the alert signal must first connect to the last device that the address/command bus is connected to.
2. DRAM_RST CAP should no stuffed

## Figure 4-15. CFL-H DDR4 x8 Memory Down DQ/DQS/RCOMP Signals

## Table 4-14. CFL-H DDR4 x8 Memory Down Routing Guideline (Sheet 1 of 3)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Breakout | Total | | |
| CLK | BO1 | MS | VSS | 1 | 3 | | | | 3.5 | 3.5 | 3.5 | | 450 | 800 | [1st] 6000 [Last] 10300 | (R1) 36 (C1-no stuff) 0.0033 (C2) 0.01 | 1,2, 3, 7,8 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | 4 | 16 | 16 | | 700 | | | | |
| | M1 | SL | VSS | 0 | 6/6.5 | 72 | | ±10 | 4.5 | 16 | 16 | | | | | | |
| | M2 | SL | VSS | 0 | 5/5.5 | | | | 4.5/4 | 16 | 16 | | 1000 | | | | |
| | BI1 | SL | VSS | 8 | 3 | | | | 3.5 | 16 | 16 | | 150 | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | 85 | | ±10 | 4.5 | 16 | 16 | | 700 | | | | |
| | T1 | MS | VSS | 1 | 3 | | | | 3.5 | 16 | 16 | | 200 | | | | |
| | T2 | SL | VSS | 0 | 4.5 | 85 | | ±10 | 4.5 | 16 | 16 | | 300 | | | | |
| | T3 | MS | VSS | 1 | 3 | | | | 3.5 | 16 | 16 | | 50 | | | | |
| CTRL/ CKE | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | 3.5 | | 450 | 800 | [1st] 6000 [Last] 10300 | 36 | 1,2, 3 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4 | 16 | | 700 | | | | |
| | M | SL | VSS | 0 | 5.5/7 | | 40 | ±10 | | 5/6 | 16 | | | | | | |
| | BI1 | MS | VSS | 8 | 3 | | | | | 3.5 | 16 | | 150 | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 700 | | | | |
| | T2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 300 | | | | |
| | T3 | MS | VSS | 1 | 3 | | | | | 3.5 | 16 | | 50 | | | | |
| CMD | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | 3.5 | | 450 | 800 | [1st] 6000 [Last] 10300 | 36 | 1,2, 3 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4 | 16 | | 700 | | | | |
| | M | SL | VSS | 0 | 5.5/7 | | 40 | ±10 | | 4.5/ 5.5 | 16 | | | | | | |
| | BI1 | MS | VSS | 8 | 3 | | | | | 3.5 | 16 | | 150 | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 700 | | | | |
| | T2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 300 | | | | |
| | T3 | MS | VSS | 1 | 3 | | | | | 3.5 | 16 | | 50 | | | | |

## Table 4-14. CFL-H DDR4 x8 Memory Down Routing Guideline (Sheet 2 of 3)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Breakout | Total | | |
| Alert | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | 3.5 | | 450 | 800 | [1st] 6000 [Last] 10300 | (R1 connected to VDDQ) 50 | 1,2,3 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4 | 16 | | 700 | | | | |
| | M | SL | VSS | 0 | 5.5/7 | | 40 | ±10 | | 4.5/5.5 | 16 | | | | | | |
| | BI1 | MS | VSS | 8 | 3 | | | | | 3.5 | 16 | | 150 | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 700 | | | | |
| | T2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | 6.5 | 16 | | 300 | | | | |
| | T3 | MS | VSS | 1 | 3 | | | | | 3.5 | 16 | | 50 | | | | |
| Strobe | BO1 | MS | VSS | 1 | 3 | | | | 3.5 | | 3.5 | 3.5 | 450 | 800 | 4500 | | 1,2,4,5,6,7,9 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | 4 | | 16 | 25 | 700 | | | | |
| | M | SL | VSS | 0 | 4/4.5 | 85 | 50 | ±10 | 4.5 | | 16 | 25 | | | | | |
| | BI1 | SL | VSS | 1 | 3 | | | | 3.5 | | 16 | 25 | 150 | | | | |
| Data | BO1 | MS | VSS | 1 | 3 | | | | | 3.5 | 3.5 | 3.5 | 450 | 800 | 4500 | | 1,2,4,5,6,9 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | 4 | 16 | 25 | 700 | | | | |
| | M | SL | VSS | 0 | 4/4.5 | | 50 | ±10 | | 4.5/5.5 | 16 | 25 | | | | | |
| | BI1 | SL | VSS | 1 | 3 | | | | | 3.5 | 16 | 25 | 150 | | | | |
| Reset | BO1 | MS | VSS | 1 | 3 | | | | | | 3.5 | | 30 | 1000 | 10300 | (R1) 470 (R2) 0 (C1) 0.1 | 3,8 |
| | BO2 | SL | VSS | 0 | 3.5 | | | | | | 20 | | 1000 | | | | |
| | M | SL | VSS | 1 | 4/4.5 | | 50 | ±10 | | | 20 | | | | | | |
| | BI1 | MS | VSS | 8 | 3 | | | | | | 20 | | | | | | |
| | BI2 | SL | VSS | 0 | 4.5 | | 50 | ±10 | | | 20 | | | | | | |
| RCOMP [0] | M | MS/SL | VSS | 4 | 12-15 | | | | | 13 | 13 | | 500 | | 500 | 121 | |
| RCOMP [1] | M | MS/SL | VSS | 4 | 12-15 | | | | | 13 | 13 | | 500 | | 500 | 121 | 10 |
| RCOMP [2] | M | MS/SL | VSS | 4 | 12-15 | | | | | 13 | 13 | | 500 | | 500 | 100 | |

## Table 4-14. CFL-H DDR4 x8 Memory Down Routing Guideline (Sheet 3 of 3)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | | R (Ω±1%) C(uF) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance (%) | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Breakout | Total | | |

***Notes:***
1. Avoid any parallel routing between two adjacent layers. When parallel routing can not be avoided in the CPU Break Out, it is recommended to offset the signals from two adjacent layers so no direct overlap occurs. If needed, the total parallel routing length in the CPU Break Out, which includes both overlapped and offset parallel routing, must be 300 mils or less.
2. Signals while routed on inner PCB layers must be ground referenced with solid ground floods on both sides.
3. Use individual termination resistors (R1) for each signal. Don't use Rpacks
4. For Option #1 (Single Rank) configuration there are only 8 DRAM Devices connected to each CMD Group Signal and only 1 DRAM Device connected to each Strobe/Data Group Signal. For these designs DRAM Devices [15:8] and their corresponding BI1 routing segments need to be removed for each CMD Group Signal and the second DRAM Device and corresponding BI routing segment needs to be removed for each Strobe/Data Group Signal.
5. The Strobe and Data Group Signals within the same byte must always route together on the same layers for their entire route
6. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel
7. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed
8. Capacitor C1 is a defensive design and should be NO STUFF by default
9. DQ and DQS signals must route at the same layer and have same width
10. RCOMP[1] value for Mix SoDIMM and MD topology should be 75 Ohm

## Table 4-15. CFL-H DDR4 x8 Memory Down Length Matching Guidelines (Sheet 1 of 2)

| Signal Group | Rule Details | Length Matching (mils) | | Notes |
|---|---|---|---|---|
| | | Min | Max | |
| **CLK** | BI1 (max - min) | 0 | 50 | 2 |
| | CK[X] - CK#[X]; where X = 0 or 1 | -5 | 5 | 1,2 |
| | CK/CK#[1:0] (max - min) | 0 | 10 | 1,2 |
| **CTRL/CKE** | BI1 (max - min) | 0 | 0 | 2,4 |
| | CTRL/CKE (max - min) | 0 | 100 | 1,2 |
| | CK/CK#[X] - CTRL/CKE; where X = 0 or 1 | 0 | 100 | 1,2,6 |
| **CMD** | BI1 (max - min) | 0 | 0 | 2,4 |
| | CMD (max - min) | 0 | 100 | 1,2,6 |
| | CK/CK#[0] - CMD; where X = 0 or 1 | -500 | 500 | 1,2 |
| **Strobe** | BI1 (max – min) | 0 | 0 | 2,5 |
| | DQS[X] - DQS#[X], where X = 0 to 7 | -5 | 5 | 1,2 |
| | CK/CK#[X] - DQS/DQS#[Y], where X = 0 or 1 and Y = 0 to 7 | -500 | 5500 | 1,2 |
| **Data** | BI(max-min) | 0 | 0 | 2,5 |
| | DQ(Byte[X]) - DQS/DQS#[X], where X = 0 to 7 | -20 | 20 | 1,2,3 |

### Table 4-15. CFL-H DDR4 x8 Memory Down Length Matching Guidelines (Sheet 2 of 2)

***Notes:***

1. Length Matching = CPU Die to DRAM Ball of every DRAM Device (CLK = PKG+BO1+BO2+M1+M2+BI1+BI2, CTRL/CKE/CMD = PKG+BO1+BO2+M+BI1+BI2, Strobe/Data = PKG+BO1+BO2+M+BI1); where a conversion factor of 0.9 must be used on Micro-Strip Segments to convert Micro-Strip lengths to Strip-Line equivalent lengths
2. To help facilitate and check the Length and Matching relationships on a design please reference the Coffee Lake Platform System Memory Automated Trace Lengths Calculator (ATLC) #568458
3. Byte[0] = DQ[7:0], DQS/DQS#[0], Byte[1] = DQ[15:8], DQS/DQS#[1], Byte[2] = DQ[23:16], DQS/DQS#[2], Byte[3] = DQ[31:24], DQS/DQS#[3], Byte[4] = DQ[39:32], DQS/DQS#[4], Byte[5] = DQ[47:40], DQS/DQS#[5], Byte[6] = DQ[55:48], DQS/DQS#[6], Byte[7] = DQ[63:56], DQS/DQS#[7]
4. CMD/CTRL BI matching:this matching rule refer to all BI (Break-ins) sections that routed within each signal.For example:ADDR[0]/[1] BI1 shoudl be equal in all DRAMs.ADDR[0] BI1 may be equal to ADDR[1] BI1.
5. DQ/DQS matching rules:DQ - BI should be matched within all bytes and not only within byte (max-min=0). DQ[63..0] BI section should be equal. DQS - BI should be matched within all bytes and not only within bytes (max-min=0).DQS[7..0][P/N] BI section should be equal.DQ and DQS BI does not need to be matched.
6. The delta between CLK signals to CMD/CTRL/CKE, between DRAMs should be kept < 20mils. For exp: |DRAM[x] (CK[i]-Addr[j]) - DRAM[y](CK[i]-Addr[j])| < 20mils.

## 4.7 CFL-H DDR4 Mixed SODIMM and Memory Down x16 Daisy-Chain Topology

### Table 4-16. System Memory Configuration Details Covered in this Section (Sheet 1 of 2)

| Parameter | Details |
|---|---|
| Processor | CFL-H |
| Memory Type | DDR4 |
| Configuration | SoDIMM Channel = One SODIMM<br>MD Channel = x16 Memory Down (Four DRAM Devices) |
| Speed (MT/s) | 2400/2666 |
| Channels | 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | SoDIMM Channel:2<br>Memory Down Channel:1 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | Mix with SDP:20GB,SODIMM 16GB+Memory Down 4 Devices of 1GB<br>Mix with DDP:24GB,SODIMM 16GB+Memory Down 4 Devices of 2GB |
| SODIMM Raw-CARD Types | 2666:<br>RC-A(1Rx8),RC-E(2Rx8),RC-C(1Rx16)<br>2400:<br>RC-B(2Rx8) |
| Memory Down Types [1] [2]<br>(Pkg Ranks - Die Bits - Pkg bits) | 96-Ball BGA<br>2666:SDP 1-16-16<br>2400:DDP 1-8-16 |
| PCB Layers / Type [3] | 8L/T3 |
| DRAM Device Placement | Top Motherboard Layer, Single Sided, Back-to-Back Placement<br>Memory Down x16 Daisy-Chain Topology |
| Processor Memory Ball Map [4] | Interleaved |

**Table 4-16. System Memory Configuration Details Covered in this Section (Sheet 2 of 2)**

| Parameter | Details |
|---|---|
| DRAM Device ODT Capability [5] | Enabled |
| Total Max Length | SoDIMM Channel:<br>Strobe/Data/CTRL/CLK/CKE/CMD=PKG+BO1+BO2+M+BI<br>RCOMP=M<br>Memory Down Channel:<br>Strobe/Data/Reset = PKG+BO+M+BI<br>CLK/CTRL/CKE/CMD= PKG+BO+M+BI1+BI2<br>RCOMP = M |

***Notes:***

1. SDP: Single Die Package, DDP: Dual Die Package, QDP: Quad Die Package
2. No mixed vendor support within a channel and No mixed memory DRAM down type support (SDP, DDP, QDP) within a channel
3. Type 3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias.
   Type 4 (T4) (1-x-1+) = PCB with one build-up layer and two layers of Micro-vias.
   Type 4 (T4) (2-x-2+) = PCB with two build-up layer and three layers of Micro-vias.
   Type 4 (T4) (3-x-3+) = PCB with three build-up layer and four layers of Micro-vias.
   See "Stack-Up and PCB Considerations" chapter for more details in this document.
4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-by-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.
5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

For CFL-H DDR4 SO-DIMM Channel-Signals topology refer to Figure 4-7, "CFL-H DDR4 SO-DIMM 2DPC Signals Topology".

For CFL-H DDR4 SO-DIMM Channel - Signals Routing Guidelines refer to Table 4-8, "CFL-H DDR4 SO-DIMM 1DPC Signal Routing Guidelines"

For CFL-H DDR4 SO-DIMM Channel - Length Matching Guidelines refer to Table 4-5, "CFL-H DDR4 ECC SO-DIMM Length and Matching Guidelines",Please ignore ECC guidelines

For CFL-H DDR4 Memory Down x16 Channel-CLK/CTRL/CKE/CMD/Reset signals topology refer to Figure 4-12, "CFL-H DDR4 1Rx16 Memory Down CLK/CTRL/CKE/CMD/Reset Signal Topology"

For CFL-H DDR4 Memory Down x16 Channel-Strobe/Data/RCOMP signals topology refer to Figure 4-11, "CFL-H DDR4 1Rx16 Memory Down Strobe/Data/RCOMP Signal Topologies"

For CFL-H DDR4 Memory Down x16 Channel- signals routing topology refer to Table 4-11, "CFL-H DDR4 1Rx16 Memory Down Routing Guideline"

For CFL-H DDR4 Memory Down x16 Channel- Length Matching Guidelines refer to Table 4-12, "CFL-H DDR4 1Rx16 Memory Down Length Matching Guidelines"

***Note:*** Avoid any parallel routing for Memory down x16 Channel and SoDIMM Channel.

***Note:*** For Mix Topology-SoDIMM with Memory down please use SoDIMM RCOMP [0],[1] and [2] value

## 4.8 CFL-H DDR4 Mixed SODIMM and Memory Down x8 Daisy-Chain Topology

### Table 4-17. System Memory Configuration Details Covered in this Section

| Parameter | Details |
|---|---|
| Processor | CFL-H |
| Memory Type | DDR4 |
| Configuration | SoDIMM Channel = One SODIMM<br>MD Channel = x8 Memory Down (Eight DRAM Devices) |
| Speed (MT/s) | 2400/2666 |
| Channels | 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | SoDIMM Channel:2<br>Memory Down Channel:1 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | 24GB,SODIMM 16GB+Memory Down 8 Devices of 1GB |
| SODIMM Raw-CARD Types | 2666:RC-A(1Rx8),RC-E(2Rx8),RC-C(1Rx16)<br>2400:RC-B(2Rx8) |
| Memory Down Types [1 2]<br>(Pkg Ranks - Die Bits - Pkg bits) | 78-Ball BGA<br>SDP 1-8-8 |
| PCB Layers / Type [3] | 8L/T3 |
| DRAM Device Placement | Top Motherboard Layer, Single Sided, Back-to-Back Placement<br>Memory Down x8 Daisy-Chain Topology |
| Processor Memory Ball Map [4] | Interleaved |
| DRAM Device ODT Capability [5] | Enabled |
| Total Max Length | SoDIMM Channel:<br>Strobe/Data/CTRL/CLK/CKE/CMD=PKG+BO1+BO2+M+BI<br>RCOMP=M<br>Memory Down Channel:<br>Strobe/Data = PKG+BO1+BO2+M+BI1<br>Reset = PKG+BO1+BO2+M+BI1+BI2<br>CLK = PKG+BO1+BO2+M1+M2+BI1+BI2<br>CTRL/CKE/CMD= PKG+BO1+BO2+M+BI1+BI2<br>RCOMP = M |

***Notes:***

1. SDP: Single Die Package, DDP: Dual Die Package, QDP: Quad Die Package
2. No mixed vendor support within a channel and No mixed memory DRAM down type support (SDP, DDP, QDP) within a channel.
3. Type 3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias.
   Type 4 (T4) (1-x-1+) = PCB with one build-up layer and two layers of Micro-vias.
   Type 4 (T4) (2-x-2+) = PCB with two build-up layer and three layers of Micro-vias.
   Type 4 (T4) (3-x-3+) = PCB with three build-up layer and four layers of Micro-vias.
   See "Stack-Up and PCB Considerations" chapter for more details in this document.
4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-by-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.

5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

### Figure 4-16. CFL-H DDR4 x8 Memory Down Placement and Block Diagram

For CFL-H DDR4 SO-DIMM Channel-Signals topology refer to Figure 4-7, "CFL-H DDR4 SO-DIMM 2DPC Signals Topology".

For CFL-H DDR4 SO-DIMM Channel - Signals Routing Guidelines refer to Table 4-8, "CFL-H DDR4 SO-DIMM 1DPC Signal Routing Guidelines"

For CFL-H DDR4 SO-DIMM Channel - Length Matching Guidelines refer to Table 4-5, "CFL-H DDR4 ECC SO-DIMM Length and Matching Guidelines",Please ignore ECC guidelines

For CFL-H DDR4 Memory Down x8 Channel-CLK/CTRL/CKE/CMD/Reset signals topology refer to Figure 4-14, "CFL-H DDR4 x8 Memory Down CLK/CKE/CMD/CTRL/Reset Signals Topologies"

For CFL-H DDR4 Memory Down x8 Channel-Strobe/Data/RCOMP signals topology refer to Figure 4-15, "CFL-H DDR4 x8 Memory Down DQ/DQS/RCOMP Signals"

For CFL-H DDR4 Memory Down x8 Channel- signals routing topology refer to Table 4-14, "CFL-H DDR4 x8 Memory Down Routing Guideline"

For CFL-H DDR4 Memory Down x8 Channel- Length Matching Guidelines refer to Table 4-15, "CFL-H DDR4 x8 Memory Down Length Matching Guidelines"

***Note:*** Avoid any parallel routing for Memory down x8 Channel and SoDIMM Channel.

***Note:*** For Mix Topology-SoDIMM with Memory down please use SoDIMM RCOMP [0],[1] and [2] value

## 4.9 CFL-H LPDDR3 x32 Memory Down

### Table 4-18. System Memory Configuration Details Covered in this Section

| Parameter | Details |
|---|---|
| Processor | CFL-H62 |
| Memory Type | LPDDR3 |
| Configuration | Channel A = x32 Memory Down (Two DRAM Devices)<br>Channel B = x32 Memory Down (Two DRAM Devices) |
| Speed (MT/s) | 2133 |
| Channels | 1 and 2 |
| System Memory Voltage | 1.2V |
| Max Ranks Per Channel | 2 |
| DRAM Die Density (Gb) | 4 and 8 |
| Max Capacity (GB) | 16 |
| Memory Down Types [1] [2]<br>(Pkg Ranks - Die Bits - Pkg bits) | 178-Ball BGA<br>SDP 1-32-32, DDP 2-32-32, and QDP 2-16-32 |
| PCB Layers / Type [3] | 10L/T4 (3-x-3+) |
| DRAM Device Placement | Top Motherboard Layer, Single Sided, Side by Side Placement |
| Processor Memory Ball Map [4] | Non-Interleaved |
| DRAM Device ODT Capability [5] | Disabled |
| Total Max Length | Strobe/Data/CNTL = PKG+BO+M+BI<br>CLK/CKE/CMD = PKG+BO+M<br>RCOMP = M |

***Notes:***

1. SDP: Single Die Package, DDP: Dual Die Package, QDP: Quad Die Package
2. No mixed vendor support within a channel or channel to channel and No mixed memory DRAM down type support (SDP, DDP, QDP) within a channel or channel to channel
3. Type 3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias.
   Type 4 (T4) (1-x-1+) = PCB with one build-up layer and two layers of Micro-vias.
   Type 4 (T4) (2-x-2+) = PCB with two build-up layer and three layers of Micro-vias.
   Type 4 (T4) (3-x-3+) = PCB with three build-up layer and four layers of Micro-vias.
   See "Stack-Up and PCB Considerations" chapter for more details in this document.
4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-by-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.
   Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.
5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to Table 4-21, "ODT Signals Connectivity Table".

**Figure 4-17. CFL-H LPDDR3 x32 Memory Down Placement and Block Diagram**

**Figure 4-18. CFL-H LPDDR3 x32 Memory Down Strobe/Data/RCOMP Signal Topologies**

**Figure 4-19. CFL-H LPDDR3 x32 Memory Down CLK/CKE/CMD Signal Topologies**

## Figure 4-20. CFL-H LPDDR3 x32 Memory Down CTRL Signal Topologies

## Table 4-19. CFL-H LPDDR3 x32 Memory Down Routing Guidelines (Sheet 1 of 2)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | R (Ω±1%) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Total | | |
| CLK | BO | SL | VSS | 1 | 3 | | | | 3 | 6 | 6 | | 300 | 4000 | 38 | 1,2,3,4,7 |
| | M | SL | VSS | 1 | 3 | 70 | | ±10 | 4 | 12 | 12 | | | | | |
| | T | SL/MS | VSS | 1 | 3 | | | | 3 | 12 | 12 | | 400 | | | |
| CTRL | BO | SL | VSS | 1 | 3 | | | | | 4.5 | 6 | | 300 | 4000 | 80 | 1,2,3,4 |
| | M | SL | VSS | 0 | 3 | | 40 | ±10 | | 8 | 12 | | | | | |
| | BI | SL | VSS | 1 | 3 | | | | | 8.5 | 12 | | 400 | | | |
| | T | MS | VSS | 1 | 3 | | | | | 10 | 12 | | 500 | | | |
| CKE | BO | SL | VSS | 1 | 3 | | | | | 4.5 | 6 | | 300 | 4000 | 80 | 1,2,3,4 |
| | M | SL | VSS | 1 | 3 | | 40 | ±10 | | 8 | 12 | | | | | |
| | T | MS | VSS | 1 | 3 | | | | | 10 | 12 | | 500 | | | |
| CMD | BO | SL | VSS | 1 | 3 | | | | | 4.5 | 6 | | 300 | 4000 | 68 | 1,2,3,4 |
| | M | SL | VSS | 1 | 3 | | 40 | ±10 | | 8 | 12 | | | | | |
| | T | SL/MS | VSS | 1 | 3 | | | | | 10 | 12 | | 500 | | | |
| Strobe | BO | SL | VSS | 1 | 3 | | | | 3 | | 6 | 6 | 300 | 3000 | | 1,2,3,5,6,7,8 |
| | M | SL | VSS | 0 | 3 | 70 | | ±10 | 3.5 | | 25 | 16 | | | | |
| | BI | SL | VSS | 1 | 3 | | | | 3.5 | | 12 | 10 | 300 | | | |
| Data | BO | SL | VSS | 1 | 3 | | | | | 4.5 | 6 | 6 | 300 | 3000 | | 1,2,3,5,6,8 |
| | M | SL | VSS | 0 | 3 | | 40 | ±10 | | 9 | 25 | 16 | | | | |
| | BI | SL | VSS | 1 | 3 | | | | | 4.5 | 12 | 10 | 300 | | | |
| RCOMP[0] | M | SL/MS | VSS | 5 | 12-15 | | | | | 20 | 25 | | 500 | 500 | 200 | |
| RCOMP[1] | M | SL/MS | VSS | 5 | 12-15 | | | | | 20 | 25 | | 500 | 500 | 121 | |

## Table 4-19. CFL-H LPDDR3 x32 Memory Down Routing Guidelines (Sheet 2 of 2)

| Signal Group | Region | Layer Route | Reference | Via Count | Trace Width (mils) | Target Impedance (Ω) | | | Min Trace Spacing (mils) | | | | Max (mils) Length | | R (Ω±1%) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Diff | Single Ended | Tolerance | Diff | Group | Group to Group[1&2] | Byte [1&2] | Region | Total | | |
| **RCOMP[2]** | M | SL/MS | VSS | 5 | 12-15 | | | | | 20 | 25 | | 500 | 500 | 162 | |

***Notes:***
1. Avoid any parallel routing between two adjacent layers.
2. With Type 4 PCB there must not be any microstrip routing for pin escapes at the CPU or DRAM sides (via-in-pad technology)
3. Signals while routed on inner PCB layers must be ground referenced with solid ground floods on both sides.
4. Use individual termination resistors (RTT) for each signal. Don't use R-packs
5. Strobe and Data Group Signals within the same byte must route together.
6. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel
7. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed
8. DQ and DQS signals must route at the same layer and have same width.

## Table 4-20. CFL-H LPDDR3 x32 Memory Down Length Matching Guidelines

| Signal Group | Rule Details | Min | Max | Notes |
|---|---|---|---|---|
| CLK | CK[X] - CK#[X]; where X = 0 or 1 | -5 | 5 | 1,2 |
| CTRL/CKE | BI (max - min) | 0 | 24 | 1 |
| | CTRL/CKE (max - min) | 0 | 100 | 1,2 |
| | CK/CK#[1:0] - CTRL/CKE | -250 | 250 | 1,2 |
| CMD | CMD (max - min) | 0 | 100 | 1,2,3 |
| | CK/CK#[1:0] - CMD | -500 | 500 | 1,2 |
| Strobe | DQS[X] - DQS#[X]; where X = 0 to 7 | -5 | 5 | 1,2 |
| | CK/CK#[1:0] - DQS/DQS#[X]; where X = 0 to 7 | -1500 | 2500 | 1,2 |
| Data | Byte[X](DQmax - DQmin), X = 0 to 7 | 0 | 250 | 1,2 |
| | DQ(Byte[X]) - DQS/DQS#[X], where X = 0 to 7 | -400 | 100 | 1,2,4 |

***Notes:***
1. Length Matching = CPU Die to DRAM Ball (PKG + BO + M, PKG + BO + M + BI); where a conversion factor of 0.9 must be used on Micro-Strip Segments to convert Micro-Strip lengths to Strip-Line equivalent lengths
2. To help facilitate and check the Length and Matching relationships on a design please reference the Coffee Lake Platform System Memory Automated Trace Lengths Calculator (ATLC) #568458
3. The CFL H documented Clock to CTRL/CKE Length Matching rule is considered the "Absolute Minimum Requirement." If possible it is strongly recommended to length match the CLK and CTRL/CKE signals with the following relationship for optimal timing margins. CK/CK#[0] - CTRL/CKE: Min = 0 mils, Max = 200 mils
4. Byte[0] = DQ[7:0], DQS/DQS#[0], Byte[1] = DQ[15:8], DQS/DQS#[1], Byte[2] = DQ[23:16], DQS/DQS#[2], Byte[3] = DQ[31:24], DQS/DQS#[3], Byte[4] = DQ[39:32], DQS/DQS#[4], Byte[5] = DQ[47:40], DQS/DQS#[5], Byte[6] = DQ[55:48], DQS/DQS#[6], Byte[7] = DQ[63:56], DQS/DQS#[7]. Two Byte Clusters are grouped as Bytes[1:2], Bytes[3:2], Bytes[5:4] and Bytes[7:6]

## 4.10 CFL-H System Memory ODT Signal Connectivity Details

### Table 4-21. ODT Signals Connectivity Table

| Processor | Memory type | Side | Signal | Rule | Notes |
|---|---|---|---|---|---|
| **CFL-H** | DDR4 Memory Down | Processor | DDR0_ODT[3:0]<br>DDR1_ODT[3:0] | Processor's ODT[1:0] balls connected to DRAMs' ODT balls.<br>Processor's ODT[3:2] balls not connected. | |
| | | DRAMs | ODT[1:0] for two Ranks per channel | | |
| | DDR4 SO-DIMM 1DPC | Processor | DDR0_ODT[3:0]<br>DDR1_ODT[3:0] | Processor's ODT[1:0] balls connected to DRAMs' ODT balls.<br>Processor's ODT[3:2] balls not connected. | 1 |
| | | DRAMs | ODT[1:0] | | |
| | DDR4 SO-DIMM 2DPC | Processor | DDR0_ODT[3:0]<br>DDR1_ODT[3:0] | Processor's ODT[3:0] balls connected to DRAMs' ODT balls. | 1 |
| | | DRAMs | ODT[3:0] | | |
| | LPDDR3 Memory Down | Processor | DDR0_ODT[3:0]<br>DDR1_ODT[3:0] | Processor's ODT[0] balls connected to DRAMs' ODT balls. T-topology connection.<br>Processor's ODT[3:1] balls not connected. | 1 |
| | | DRAMs | ODT[0] | | |

***Notes:***
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP11 -CFL -H DDR4 SODIMM, RVP16 - CFL-H LPDDR3)

## 4.11 Memory Data Mask (DM) Signals Connectivity Details

### Table 4-22. DIMMs/DRAMs DM Signals Connectivity Table

| Memory type | DM signals | Connect to |
|---|---|---|
| **LPDDR3 Memory Down** | DRAMs DM[7:0] | Tied to GND |
| **DDR4 Memory Down** | DRAMs DM[7:0] | Tied to VDDQ |
| **DDR4 DIMMs** | DIMMs DM[8:0] | Tied to VDDQ |

## 4.12 CFL H System Memory Via Placement and Pad Optimization Guidelines

### 4.12.1 Via Placement at CPU Side

Ensure reference plane stitching vias are placed in close proximity of every system memory signal transition via at the CPU side

- Follow the Customer Reference Board (CRB) via placement at CPU side as much as possible for all Signal Groups.
- At least one ground stitching via must be placed from every signal transition via when ever they change signal layers.
- When a signal transitions to a layer in between two reference planes, make sure the stitching via connects to the plane closest to the signal layer.
- When a signal transitions to another routing layer, but the referencing plane still kept the same, no stitching via is required.
- GND/PWR vias should be placed between signals from different signal groups and channels.
- Where possible Data and Strobe vias from different byte lanes should be separated by GND vias.
- For Type 4 (2-x-2+) memory down PCB designs use Stacked Micro Vias from layer 1 to layer 2 or 4 under the processor rather than using Staggered Micro Vias to help minimize voiding on layers 1,3 and 5 reference planes.
- Remove via pads from layers that are not connected to traces (Figure 4-21).

**Figure 4-21. Remove PADs from Layers that Do Not Connect to Trace**

## 4.12.2 Via Placement at SO-DIMM and DRAM Device Side

Ensure reference plane transition vias are placed in close proximity of every system memory signal transition via at the SO-DIMM or DRAM Device side.

- Follow the Customer Reference Board (CRB) via placement at SO-DIMM or Memory DRAM Down side as much as possible for all Signal Groups.
- At least one ground stitching via must be placed from every signal transition via when ever they change signal layers.
- For Type 4 (2-x-2+) memory down PCB designs use Stacked Micro Vias from layer 1 to layer 2 or 4 under the DRAM Devices rather than using Staggered Micro Vias to help minimize voiding on layers 1,3 and 5 reference planes.
- Follow the via spacing guidelines covered in Table 4-23
- Remove via pads from layers that are not connected to traces (Figure 4-21).

### Table 4-23. CFL H Guidelines for Vias Separation

| CPU | Memory Type | Signal Group | Rule | Pitch (mils) | Notes |
|---|---|---|---|---|---|
| CFL H | SO-DIMM | DQ/DQS/DQS# to GND | >= 1 GND via | 30 | 1 |
| | | CLK/CTRL/CKE/CMD to GND | >= 1 GND via | 30 | 1 |
| | | 1 DIMM Per Channel | Pitch between DQ vias from different byte lanes > | 60 | |
| | | | Pitch between CMD to CTRL vias > | 60 | |
| | Memory Down | DQ/DQS/DQS# | >= 1 GND via | 70 | 1 |
| | | CLK/CTRL/CKE/CMD | >= 1 PWR/GND via | 70 | 1 |
| | | DQ to DQ from different byte lanes | Pitch between DQ vias from different byte lanes > | 37 | 2 |

***Notes:***

1. Due to space constrains, it is acceptable to have one GND via for every two transition signal vias.
2. This via-to-via separation is between Micro Vias, not PTH Vias.

## 4.13 CFL H System Memory Reference Voltage (VREF) Guidelines

System memory reference voltages, VREF_DQ_A, VREF_DQ_B, VREF_CA must meet the following guidelines:

- Follow the Customer Reference Board (CRB) board file and schematic implementation as closely as possible.
- The figures at this section show the VREF implementation block diagrams for all supported platform configurations.
- Place the VREF voltage dividers as close as possible to the SO-DIMMs or memory down DRAM devices.
- All VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/ planes. Short violations are acceptable if required due to tight routing constraints.

**Figure 4-22. CFL-H DDR4 SO-DIMM $V_{REF-CA}$ Overview**

**Figure 4-23. CFL-H DDR4 x16 Memory Down $V_{REF-CA}$ Overview**

## Figure 4-24. CFL-H DDR4 x8 Memory Down $V_{REF-CA}$ Overview

***Note:*** For 2Rx8 each DRAM should have its own cap (47nF) – 16 caps per channel. In overall 32 caps.

**Figure 4-25. CFL-H LPDDR3 x32 Memory Down $V_{REF-DQ}$ and $V_{REF-CA}$ Overview**

## 4.14 CFL-H DDR Power Delivery - Memory side

The guidelines here are to support a single sided component assembly.

The expectation is that the decoupling caps will be placed as close as possible to the DRAM devices or SODIMMs to minimize the loop inductance of the caps. A placement of farther than 5mm is not recommended.

The decoupling capacitor to DRAM/SODIMM inductance loop is better with single sided assembly, if the power and ground planes are strongly coupled, and cap placement and connection by common power integrity practices.

Dual sided designs may prove to be a superior solution for certain board technologies, thickness of the stackup and placement location of the caps under the memory devices. This document does not cover the dual sided assembly guidelines.

### 4.14.1 CFL-H DDR4 SODIMM Decoupling

**Table 4-24. DDR4 SODIMM Power Plane Decoupling**

| Memory Configuration | Power Domain | Decoupling Location | Qty x µF (size) | Note |
|---|---|---|---|---|
| DDR4 2 Channels SODIMM **1DPC** | VDDQ | 4 near each side of the DIMM connector close to VDD pins | 16x 10µF (0603) | |
| | | 4 near each side of the DIMM connector close to VDD pins | 16x 1µF (0402) | |
| | | 1 placeholder | 1x 330µF (7343) | |
| | VTT | Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder | 2x 10µF (0603) | |
| | | Placed on VTT plane close to DIMM | 4x 1µF (0402) | |
| | VPP | DIMM Pin side, 1 per DIMM | 2x 10µF (0603) | |
| | | DIMM Pin side, 1 per DIMM | 2x 1µF (0402) | |
| | VDDSPD | Place close to DIMM | 2x 0.1µF (0402) | |
| | | Place close to DIMM | 2x 2.2µF (0402) | |
| DDR4 2 Channels SODIMM **2DPC** | VDDQ | 4 near each side of the DIMM connector close to VDD pins | 32 x 10µF (0603) | |
| | | 4 near each side of the DIMM connector close to VDD pins | 32 x 1µF (0402) | |
| | | Placeholder | 2x 330µF (7343) | |
| | VTT | Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder | 4x 10µF (0603) | |
| | | Placed on VTT plane close to DIMM | 8x 1µF (0402) | |
| | VPP | DIMM Pin side, 1 per DIMM | 4x 10µF (0603) | |
| | | DIMM Pin side, 1 per DIMM | 4 x 1µF (0402) | |
| | VDDSPD | Place close to DIMM | 4x 0.1µF (0402) | |
| | | Place close to DIMM | 4x 2.2µF (0603) | |

***Notes:***
1. Total quantity is referring to 2 channels.

## 4.14.2 CFL-H DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

**Table 4-25. DDR4 Memory Down Power Plane Decoupling**

| Memory Configuration | Power Domain | Decoupling Location | Qty x µF (size) | Note |
|---|---|---|---|---|
| DDR4 Memory Down x16 - 4 Devices per Channel | VDDQ/VDD (shorted) | 4 per dram,as close as possible | 32x 1µF (0402) (All stuffed) | |
| | | Distributed evenly across domain,close by Drams | 10x 10µF (0603) (All stuffed) | |
| | VPP | 2 per dram,as close as possible | 16x 1µF (0402) | |
| | | Distributed evenly across domain,close by Drams | 5x 10µF (0603) | |
| | VTT | Distributed along termination resistors | 16x 1µF (0402) | |
| | | Distributed evenly across domain | 4x 10µF (0603) | |
| DDR4 Memory Down x8- 8 Devices per Channel | VDDQ/VDD (shorted) | 4 as near each x8 DRAM device as possible | 64x 1µF (0402) (min of 48 stuffed) | |
| | | Distributed around the DRAM devices | 20x 10µF (0603) (min of 12 stuffed) | |
| | VPP | 2 as near each x8 DRAM device as possible | 32x 1µF (0402) | |
| | | Distributed around the DRAM devices | 10x 10µF (0603) | |
| | VTT | Distributed along termination resistors | 32x 1µF (0402) | |
| | | Distributed evenly across domain | 8x 10µF (0603) | |
| DDR4 Memory Down x8- 16 Devices per Channel | VDDQ/VDD (shorted) | 4 as near each x8 DRAM device as possible | 128x 1µF (0402) (min of 96 stuffed) | |
| | | Distributed around the DRAM devices | 40x 10µF (0603) (min of 24 stuffed) | |
| | VPP | 2 as near each x8 DRAM device as possible | 64x 1µF (0402) | |
| | | Distributed around the DRAM devices | 20x 10µF (0603) | |
| | VTT | Distributed along termination resistors | 64x 1µF (0402) | |
| | | Distributed evenly across domain | 16x 10µF (0603) | |

***Notes:***
1. Total quantity is referring to 2 channels.

### 4.14.3 CFL-H LPDDR3 x32 Memory Down Decoupling

This decoupling solution assumes a memory down implementation of four x32bit DRAM devices.

The isolation requirement of the DRAM power domains reduces cap sharing resulting in higher cap counts than DDR3L memory down. The power domains are VDD1, VDD2, VDDCA, and VDDQ.

**Figure 4-26. Decoupling Connections at the LPDDR3 Device**

***Note:*** The VDDQ plane can be connected to the DRAM VDDQ inputs directly on L1 or other layers. Isolate VDD2 & VDDCA from VDDQ at DRAM end with PTHs.

## Table 4-26. LPDDR3 x32 Power Plane Decoupling (Sheet 1 of 2)

| Memory Configuration | Power Domain | Decoupling Location | Qty x µF (size) | Note |
|---|---|---|---|---|
| **Config 1**<br>LPDDR3 Memory Down<br>x32 - 2 Devices per Channel | VDDQ | Distributed evenly across domain, close by DRAMs, VDDQ red circles Figure 4-28 | 5x 10µF (0603) | 2 |
| | | 4 caps per DRAM, Figure 4-27 VDDQ red circles | 16x 1µF (0402) | 2 |
| | VDDCA | 2 caps per DRAM, Figure 4-27 VDDCA yellow circles | 8x 1µF (0402) | 2 |
| | | Distributed evenly across domain, close by DRAMs, VDDCA yellow circles Figure 4-28 | 2x 10µF (0603) | 2 |
| | VDD2 | Distributed evenly across domain, close by DRAMs, VDD2 blue circles Figure 4-28 | 5x 10µF (0603) | 2 |
| | | 3 caps per DRAM, Figure 4-27 VDD2 blue circles | 12x 1µF (0402) | 2 |
| | VDD1 | 2 caps per DRAM,Figure 4-27 VDD1 pink circles | 8x 1µF (0402) | 2 |
| | | Distributed evenly across domain, close by DRAMs, VDD2 blue circles Figure 4-28 | 5x 10µF (0603) | 2 |
| | VTT | Distributed along termination resistors.Caps shown in blue Figure 4-29 | 8x 1µF (0402) | |
| | | Distributed evenly across domain, close by terminations | 4x 10µF (0603) | |
| **Config 2**<br>LPDDR3 Memory Down<br>x32 - 2 Devices per Channel | VDDQ | Distributed evenly across domain, close by DRAMs, VDDQ red circles Figure 4-28 | 5x 10µF (0603) | 2 |
| | | 2 caps per DRAM, Figure 4-27 VDDQ red circles | 8x 1µF (0402) | 2 |
| | VDDCA | 2 caps per DRAM, Figure 4-27 VDDCA yellow circles | 8x 1µF (0402) | 2 |
| | | Distributed evenly across domain, close by DRAMs, VDDCA yellow circles Figure 4-28 | 2x 10µF (0603) | 2 |
| | VDD2 | 1 cap for northern VDD2 pins on each DRAM (total 4), 3 caps between DRAMs | 5x 10µF (0603) | 2 |
| | | 3 caps per DRAM, Figure 4-27 VDD2 blue circles | 7x 1µF (0402) | 2 |
| | VDD1 | 1 caps per DRAM,Figure 4-27 VDD1 pink circles | 4x 1µF (0402) | 2 |
| | | Distributed evenly across domain, close by DRAMs, VDD2 blue circles Figure 4-28 | 5x 10µF (0603) | 2 |
| | VTT | Distributed along termination resistors.Caps shown in blue Figure 4-29 | 4x 1µF (0402) | |
| | | Distributed along termination resistors. | 4x 10µF (0603) | |

## Table 4-26. LPDDR3 x32 Power Plane Decoupling (Sheet 2 of 2)

| Memory Configuration | Power Domain | Decoupling Location | Qty x µF (size) | Note |
|---|---|---|---|---|
| ***Notes:***<br>1. Total quantity is referring to 2 channels.<br>2. Distributed among the 4 LPDDR3 Devices | | | | |

## Figure 4-27. Decoupling at the LPDDR3 device

**Figure 4-28. Decoupling at the LPDDR3 Device**

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# 5 DisplayPort* Design Guidelines

## 5.1 Introduction

DisplayPort* uses differential signaling to achieve a high-bandwidth bus interface to support both embedded chip-to-chip and external box-to-box digital display connections from the Coffee Lake processor and PCH. A DisplayPort link consists of:

**Main link:** Unidirectional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio.

**Auxiliary Channel (AUX CH):** A half-duplex, bi-directional channel used for link and device control.

**Hot Plug Detect (HPD) signal:** Serves as an interrupt request for the sink device.

**Figure 5-1. DisplayPort* Channels**

### 5.1.1 DisplayPort* Link Bit Rates

DisplayPort* Main link uses a scrambled 8b/10b encoding scheme for the data stream being transmitted. It allows the clock to be embedded in the data stream.

**Table 5-1. DisplayPort* Bit Rates**

| Bit Rate | Supports (in # of lanes) | Peak Bandwidth |
|---|---|---|
| 1.62 Gb/s | 4 | 4 x 162 MB/s = 648 MB/s |
| 2.7 Gb/s | 4 | 4 x 270 MB/s = 1080 MB/s |
| 5.4 Gb/s | 4 | 4 x 540 MB/s = 2160 MB/s |

### 5.1.2 DisplayPort* Main Link Buffer Type

The AC coupled External DisplayPort* (from the Coffee Lake processor) buffers are capable of driving the following voltage and pre-emphasis levels:

**Table 5-2. Supported Voltage and Pre-emphasis Levels**

| Nominal Voltage | Voltage Level | 0 db | 3.5 db | 6 db | 9.5 db |
|---|---|---|---|---|---|
| 0.4V | 0 | YES | YES | YES | YES |
| 0.6V | 1 | YES | YES | YES | |
| 0.8V | 2 | YES | YES | | |
| 1.2V | 3 | NOT SUPPORTED | | | |

The transmitter driver strength is optimized during the link training for Ext-DP. Pre-emphasis is an effective way to open the data eye of a high-loss channel. The longer trace length increase the channel interconnect loss and therefore require pre-emphasis. For more details on multiple pre-emphasis levels, refer to the DisplayPort* specifications.

### 5.1.3 Reference Documents

| Title | Document Number/Location |
|---|---|
| DisplayPort Standard Version 1.2 Electrical Specification | http://www.vesa.org |
| VESA DisplayPort Dual-Mode Standard | |
| High speed internal connector and cable specification | 549136 |

## 5.2 DisplayPort* Signal Descriptions

### 5.2.1 Signal Groups

**Table 5-3. DisplayPort* Signals**

| Description | Signal Mapping | | |
|---|---|---|---|
| | Coffee Lake Processor | Cannon Lake PCH | CRB DisplayPort Mapping |
| Main Link (Tx) | DDIx_TXP[3:0] and DDIx_TXN[3:0] | N/A | DDIx_OB_LANE[3:0]_DP and DDIx_OB_LANE[3:0]_DN |
| Aux Channel | DDIx_AUXP and DDIx_AUXN | N/A | DDIX_OB_AUX_DP and DDIX_OB_AUX_DN |
| Hot Plug Detect | N/A | DDPx_HPD[3:0] | DDIx_HPD_Q |
| Topology | Differential-Pair Point-to-Point<br>Single Ended Point-to-Point | | |
| Reference Plane | Ground Referenced | | |

## 5.3 DisplayPort* Topology Guidelines

For all topologies, the sink connects to the source via a cable. It is useful to partition the system budgets across the platform components, source, cable assembly and sink to allow different design teams a working budget. The design guide and resulting recommendations were designed to comply with the requirements for DisplayPort* mid bus probe point TP2 for HBR (High Bit Rate =2.7 Gbps) and RBR (Reduced Bit Rate =1.62Gbps). The compliance point for HBR2 (High Bit rate 2 =5.4Gbps) is TP3_EQ.

DisplayPort* Main and Aux Link Topologies:

- CFL DisplayPort* Main Link on Motherboard Topology
- CFL DisplayPort* Main Link Muxed Port Sharing on Motherboard Topology
- CFL DisplayPort* Main Link on Dock Topology with Re-driver
- CFL DisplayPort* Main Link Muxed Port Sharing on Dock Topology
- CFL DisplayPort* Main Link Internal Cable Topology

***Note:*** In addition to the routing design details mentioned below, refer to the DisplayPort external cable requirement in the VESA DisplayPort Standard.

### 5.3.1 Optimizations

**Table 5-4. Optimization Table for all Topologies**

| Description | Recommendation | Value (Units) |
|---|---|---|
| BO/M1 | The traces BO/M1 constitute a breakout and a main route segment pairing. The segments of this pair must be routed on the same layer. | |
| AC Capacitor | Select the AC Capacitor values as per DisplayPort 1.3 Electrical specifications | nominal 100 nF recommended (tolerance 75 nF to 200 nF) |
| ESD/CMC | Recommended PCB CMC or Murata NFP0QHB372HS2. Refer to Section 49.6, "PCB CMC Technology" for more information. | |
| DP_PWR | DP_PWR provides power to the dongle. It is a 3.3-V rail on pin 20 of the DP connector. | |
| CFL H PTPS | CFL H uses 12mils Pair to Pair Spacing for equivalent main routing, and 15 mils for Non-Equivalent main routing. (For Equivalent & Non-Equivalent pairs see Ch.2) | |
| Inter-pair length mismatch | maximum length mismatch between the shortest and longest DP differential pairs for each port is 2" | |
| Inter-pair skew requirement | For Display Port signals is +/-1" | |
| CMC | All DP topologies in this chapter support CMC. CMC is optional and depends on the EMI testing results. It is recommended to leave the footprints in layout.<br>Adding CMC will not reduce the supported length.<br>If populated, reduce total route length by 1". | |
| **Docking Topologies Only** | | |
| AC Cap1 | AC Cap1 may be required based on the input requirements of your Re-driver. AC Cap1 can also be placed on motherboard. | |
| Re-driver | Re-driver assumed to consist of an ideal CTLE. | |

## 5.3.2 DisplayPort* Main Link Motherboard Topologies

**Figure 5-2. CFL DisplayPort* Main Link Direct Motherboard Topology**

**Table 5-6. CFL H Display Port Main Link Topologies Guidelines**

| Segment | Via Count | Stack-up | Max Length [mils] |
|---|---|---|---|
| B0 | Max 2 vias are allowed | MS/SL | 500 |
| M1 + C_I | | MS/SL/DSL | 6500 |
| Esdl | | MS | 300 |
| Cn | | MS | 700 |
| **Total Length** | | **6900** | |

***Notes:***
1. Reference plane will be Continues GND or Power. GND is preferred.
2. CMC is optional. If populated, reduce total route length by 1".

**Figure 5-3. CFL H DisplayPort* Main Link Muxed Port Sharing Topology**

## 5.3.3 Display Port* Main Link on Dock Topology with Redriver Topologies

### Table 5-8. CFL H DisplayPort* Main Link Muxed Port Sharing Topology Guidelines

| Segment | Stack-up | Via Count | Max Length [mils] |
|---|---|---|---|
| B0 | MS/SL | Max 2 vias are allowed | 500 |
| M1 | MS/SL/DSL | | 2200 |
| Muxl | MS | | 300 |
| C_I | MS | | 700 |
| Esdl | MS | | 300 |
| Cn | MS | | 700 |
| **Total Length** | | | **4100** |

***Notes:***
1. DP to VGA converter must meet DP spec
2. Converter to connector must follow Vendor application note.

### Figure 5-4. CFL H DisplayPort* Docking Topology with Re-driver

### Table 5-9. CFL H DisplayPort* Docking Topology with Re-driver Guidelines (Sheet 1 of 2)

| Segment | Stack-up | Max Length [mils] |
|---|---|---|
| BO | MS/SL | 500 |
| M1+M2 | MS/SL/DSL | 4000 |
| DKL | MS | 700 |
| DKR | MS | 3000 |
| RDL | MS | 300 |
| RDR | MS | 1500 |
| CN | MS | 500 |
| **Total Length** | | **10800** |
| Total Length --> BO to RDL | | 8800 |
| Total Length --> DKR to CN | | 5300 |

## Table 5-9. CFL H DisplayPort* Docking Topology with Re-driver Guidelines (Sheet 2 of 2)

| Segment | Stack-up | Max Length [mils] |
|---|---|---|

***Notes:***
1. AC Cap1 may be required based on the input requirements of your Re-driver
2. Re-driver assumed to consist of ideal CTLE, re-timing not necessary.
3. Docking topology does not require retimed redriver (jitter cleaning redriver).

## Figure 5-5. CFL H DisplayPort* Main Link Multiplexed Port Sharing on Dock Topology

## Table 5-10. CFL H DisplayPort* Multiplexed Docking Topology with Re-driver Guidelines

| Segment | Stack-up | Max Length [mils] |
|---|---|---|
| BO | MS/SL | 500 |
| M1 | MS/SL/DSL | 4000 |
| MUXL | MS | 300 |
| DKL | MS | 700 |
| DKR | MS | 3000 |
| RDL | MS | 300 |
| RDR | MS | 1500 |
| CN | MS | 500 |
| **Total Length** | | **10800** |
| Total Length --> BO to RDL | | 8800 |
| Total Length --> DKR to CN | | 5300 |

***Notes:***
1. AC Cap1 may be required based on the input requirements of your Re-driver
2. Re-driver assumed to consist of ideal CTLE, re-timing not necessary.
3. Docking topology does not require retimed redriver (jitter cleaning redriver).

## 5.3.4 Display Port* Main Link Internal Cable Topology

### Figure 5-6. CFL H DisplayPort* Main Link Internal Cable Topology

### Table 5-11. CFL H DisplayPort* Main Link Internal Cable Topology Guidelines

| Segment | Stack-up | Max Length [mils] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| BO | MS/SL | 400 | 400 | 400 | 400 | 400 | 400 | 400 | 400 |
| M1 | MS/SL/DSL | 5500 | 5000 | 4500 | 4000 | 3500 | 3000 | 2500 | 2000 |
| M2 | MS | 500 | 500 | 500 | 500 | 500 | 500 | 500 | 500 |
| BO+M1+M2 | - | 5500 | 5000 | 4500 | 4000 | 3500 | 3000 | 2500 | 2000 |
| Esdl | MS | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| C_I+Esdl+Cn | MS | 800 | 800 | 800 | 800 | 800 | 800 | 800 | 800 |
| Cable Loss @ 2.7GHz | - | <=1.3dB | <=1.8dB | <=2.2dB | <=2.5dB | <=2.7dB | <=2.9dB | <=3.2dB | <=3.4dB |
| Informative AWG38 100W Microcoax | - | 2000 | 5800 | 8900 | 11200 | 12800 | 14300 | 16700 | 17700 |

***Notes:***
1. Internal Cable far end crosstalk should be <=-54dB @ 2.7GHz
2. Pair to pair spacing for motherboard and daughter card is 15 mils.

## 5.3.5 DisplayPort* Auxiliary Channel Topologies

DisplayPort auxiliary channel is a sideband bidirectional differential communication channel. The channel is used by the Source to Discover Sink Capabilities and to determine the multi stream topology during link training. During normal operation, the channel is used to maintain the link, to transport auxiliary data, and control the Display.

Refer the respective stack-up sections for corresponding trace geometries.

***Note:*** Refer the latest VESA DisplayPort Standard for any updates to the specification and topologies.

**Figure 5-7. CFH H DisplayPort* Auxiliary Channel External (Topology A)**

**Figure 5-8. CFH H DisplayPort* Auxiliary Channel Multiplexed Port Sharing on Motherboard (Topology B)**

**Figure 5-9. CFH H DisplayPort* Auxiliary Channel Docking with Re-driver Aux Sampling (Topology C)**

## Figure 5-10. CFH H DisplayPort* Auxiliary Channel Docking with Re-driver Aux Buffer (Topology D)

## Figure 5-11. CFL H DisplayPort* Auxiliary Channel Internal Cable

## Table 5-13. CFL H DisplayPort* Auxiliary Channel Routing Guidelines (Sheet 1 of 2)

| Parameters | Segment | Stackup | Units | Topology A and B | Topology C and D | Internal Cable |
|---|---|---|---|---|---|---|
| Coffee Lake Processor Breakout1 Max | BO | MS/SL | mils | 800 | 700 | NA |
| Main Route Segment Length Max | M1 | MS/SL/DSL | mils | 7000 | 5000 | NA |
| ESD to DP Connector Length Max | CN | MS/SL/DSL | mils | 7000 | 4000 | NA |
| Total Motherboard Trace Length | Sum (BO to CN) | NA | mils | 13000 | NA | NA |
| Total Motherboard Trace Length | Sum (BO to $DK_L$) | NA | mils | NA | 8000 | NA |
| Docking Connector to Re-Driver Input | $DK_R$ | MS | mils | NA | 4000 | NA |
| Total Route on the Dock Length Max | $DK_R$ + CN | NA | mils | NA | 7000 | NA |
| Total Route from Coffee Lake Processor to DP Connector | Sum (BO to CN) | NA | mils | 13000 | 14000 | 13000 |
| Via usage Max (Dock Connector to DP Connector) | DKR+CN (including breakout) | NA | vias | NA | 3 | NA |

**Table 5-13. CFL H DisplayPort* Auxiliary Channel Routing Guidelines (Sheet 2 of 2)**

| Parameters | Segment | Stackup | Units | Topology A and B | Topology C and D | Internal Cable |
|---|---|---|---|---|---|---|

***Notes:***
1. ESD is recommended to protect the silicon host and devices from electrostatic discharges. Refer to Optimization Table for specific passive devices and other common topology requirements.
2. If total length of Aux signals is less than max allowed length of DP main link signals, then Aux main route can use 12 mils Pair To Pair Spacing, otherwise Aux Pair To Pair Spacing needs to be 15mils

# 5.4 DisplayPort* General Considerations and Optimization

## 5.4.1 DisplayPort* HPD General Considerations and Optimization

The hot-plug detect output from DisplayPort sink device is a 3.3-V active high signal. Since the input on Coffee Lake processor is also 3.3-V tolerant, no inverting level shifter is required on the motherboard. However, a current blocking circuit (for example using a FET) is required to prevent the back drive current damaging Coffee Lake processor when the source is powered off and sink device is powered on. The following figure shows an example of this implementation.

***Note:*** If the display connector is on the docking station, the hot-plug circuitry should remain on main motherboard and not on the docking station in order to prevent display detection failures related to hot-plug and S-state resume. HPD signal should not be allowed to float anytime.

**Figure 5-12. DisplayPort* HPD Passgate Design Recommendation**

***Note:*** Select the pass-gate FET which has $VGS_{TH}$ (Gate Threshold voltage) less than 1.5V.

The 5V supply must turn off when CPU power is turned off.

## 5.4.2 DP_PWR Pin Back Drive Protection

DP_PWR pin 20 of DP Connector provides power to the connected dongle from the platform (source) and monitor (sink). As per specification, Normal DP to DP monitor cable assembly should not connect this across the cable. There are non-compliant cables in the market have them as direct connection. This results in Display monitor back driving current to motherboard and causing system malfunction during power on or when waking-up from sleep state.

To prevent this, add a back driver protection circuit (FET) as shown below for DP_PWR pin 20 of DP connector. FUSE is also provided to provide current protection as required by DP spec. Select MOSFET such that sum of Fuse and MOSFET 's ON resistance is less than 0.35 ohms to meet spec requirement of minimum 2.98Volts at DP_PWR pin with 0.5A current.

**Figure 5-13. DisplayPort* DP_PWR pin 20 Back Drive Protection**

***Note:*** Connect Gate of n-MOSFET to a power supply which will turn off during sleep state and is higher than 3.3V like +V12S or +V5S.

***Note:*** Customer can have alternate back drive protection circuit provided they can meet minimum Voltage requirement of 2.98Volts considering 3.3Volts power supply design also have some voltage tolerance(+/-5%).

### 5.4.3 DisplayPort* Main Link Differential-Pair Width and Spacing

Type 3 and Type 4 stack-up geometries will be different. For a summary of general routing guidelines for the width and spacing of the differential-pair traces, refer Chapter 2 “Stack-up and PCB Considerations”.

### 5.4.4 DisplayPort* Auxiliary Channel (AUX CH) General Design Considerations and Optimization

AUX CH consists of an AC-coupled, bi-directional differential-pair, providing a data rate of 1 Mbps. It is used for link management and device control, that is, for transmitting control and status information.

AUX CH is half-duplex and bi-directional. The source device is the master and Sink device is the slave. Manchester II coding is used as the channel coding for AUX CH. Like the Main link the Aux Channel clock is embedded in the data stream.

The sink device may toggle the HPD signal to interrupt the source device.

To support dual mode (DP++) over DisplayPort through Dongle for HDMI, the circuit shown below is required to be implemented on the motherboard.

## Figure 5-14. DisplayPort* Auxiliary Channel Dual Mode Support Protection Circuit

***Notes:***

1. The voltage rails specified on the pull up resistors in this circuit should be switched rails that are on during S0 only. However, the two inverters in this circuit should be powered from suspend rails.
2. Devices such as a TTL compatible FET multiplexer/demultiplexer can be used in place of passgate FETs.
3. The leakage current out of the inverter that is close to the DP connector should be minimized since it may affect voltage level to the input of the inverter due to the 1-MΩ pull down resistor.
4. If FETs are used for the passgate circuit, take care to ensure the body diode of the FETs are connected as shown in the figure above. Failure to do so will cause incorrect functionality of the circuit.

## 5.5 DisplayPort* Length Matching Guidelines

For matching methodology, refer Chapter 3, "General Differential Design Guidelines".

## 5.6 Digital Display Interface Disabling and Termination Guidelines

All the digital display ports on the Coffee Lake processor have a strap associated with it. The port strap needs to be set to configure each digital port irrespective of the digital display technology HDMI/DP. The following table lists all the digital display straps and guidelines to enable/disable a respective port on the platform. All the straps are sampled on the rising edge of the PWROK signal.

**Table 5-14. DDI Disabling and Termination Guidelines**

| Port | Strap | How to Enable Port | How to Disable Port |
|---|---|---|---|
| Port 1 | DDPB_CTRLDATA | Pull up to 3.3V with 2.2K ohm ±5% resistor | No Connect |
| Port 2 | DDPC_CTRLDATA | Pull up to 3.3V with 2.2K ohm ±5% resistor | No Connect |
| Port 3 | DDPD_CTRLDATA | Pull up to 3.3V with 2.2K ohm ±5% resistor | No Connect |

The following table lists connection details for the digital display signals when Coffee Lake processor graphics is disabled. When Coffee Lake processor graphics is not implemented on the platform, the digital display interface must also be disabled in BIOS. Refer to the BIOS specification on how to disable the respective display interfaces.

**Table 5-15. DDI Disabling and Termination Connections**

| Pin Name | Recommendation |
|---|---|
| DDPB_AUXP / DDPC_AUXP / DDPD_AUXP | No Connect |
| DDPB_AUXN / DDPC_AUXN / DDPD_AUXN | No Connect |
| DDPB_HPD / DDPC_HPD / DDPD_HPD | No Connect |
| DDI1_TXP[3:0] / DDI2_TXP[3:0] / DDI3_TXP[3:0] | No Connect |
| DDI1_TXN[3:0] / DDI2_TXN[3:0] / DDI3_TXN[3:0] | No Connect |
| DDPB_CTRLCLK / DDPB_CTRLDATA | No Connect |
| DDPC_CTRLCLK / DDPC_CTRLDATA | No Connect |
| DDPD_CTRLCLK / DDPD_CTRLDATA | No Connect |

## 5.7 Display Compensation Guidelines

Refer to Section 5.5, "DisplayPort* Length Matching Guidelines" for details.

***Note:*** There is one comp pin that is shared among all display ports.

***Note:*** Type-C DP implementation is covered under "18.4 Alternate Modes Configuration"

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# 6 Embedded DisplayPort* (eDP*) Design Guidelines

The Embedded DisplayPort* (eDP*) channel is used to transport digital display data from the Coffee Lake processor to an embedded DisplayPort Panel. Embedded DisplayPort (eDP) utilizes differential signaling to achieve a high bandwidth bus interface that supports embedded chip-to-chip connections from the Coffee Lake processor. Potential embedded chip-to-chip applications include usage within a laptop PC for driving a panel.

The Embedded DisplayPort utilizes DisplayPort 1.62 Gbps, 2.7 Gbps and 5.4 Gbps differential signaling. It is recommended that the eDP/DP standard TP3 EYE mask requirements as are met at the panel side of the mated connector.

**Table 6-1. eDP* Reference Specification**

| Title | Location |
|---|---|
| VESA Embedded DisplayPort Standard - Revision 1.4 | *http://www.DisplayPort.org* |

**Table 6-2. eDP* Compliance Specification**

| Title | Location |
|---|---|
| VESA Embedded DisplayPort Source PHY Compliance Test Guideline - Version 1.0 | *http://www.vesa.org* |

## 6.1 Signal Descriptions

**Table 6-3. eDP* Signal Groups**

| Parameters | Signal Mapping | | |
|---|---|---|---|
| | Processor | PCH | CRB eDP* Connector |
| Main Link (Tx) | eDP_TXN/P[3:0] | N/A | EDP_TX[3:0]_DN/DP |
| Aux | EDP_AUXN/P | N/A | EDP_AUX_DN/DP |
| HPD | N/A | eDP_HPD | EDP_HPD_Q |
| RCOMP | DISP_RCOMP | N/A | DISP_COMP |
| Topology | Differential-Pair Point-to-Point.<br>Single ended Point to Point | | |
| Reference Plane | Ground Referenced | | |

## 6.2 Topology Guidelines

**Table 6-4. eDP* Cable Parameters (Sheet 1 of 2)**

| Cable | Cable Length | Connector Pitch | Cable AWG | Diff Impedance | Diff Insertion Loss | Diff Return Loss | Diff FEXT | EMI/ RFI | HBR2/HBR |
|---|---|---|---|---|---|---|---|---|---|
| Micro-Coax | 1″ | 1 mm | 40 | 85-110 Ω | -0.8db/-1db/ -1.7db/-5.4db | -12.8db/-16.5db/-26db/ -4db | -47.2db/-39db/-30db/ -36db | LOW | HBR2/HBR recommended |

### Table 6-4. eDP* Cable Parameters (Sheet 2 of 2)

| Cable | Cable Length | Connector Pitch | Cable AWG | Diff Impedance | Diff Insertion Loss | Diff Return Loss | Diff FEXT | EMI/ RFI | HBR2/HBR |
|---|---|---|---|---|---|---|---|---|---|
| Micro-Coax | 3″ | 1 mm | 40 | 85-110 Ω | -1.15db/-2.2db/-3.1db/-7.3db | -16.5db/-9.4db/-15.6db/-4.8db | -49.5db/-41.5db/-32db/-36.8db | LOW | HBR2/HBR recommended |
| Micro-Coax | 4″ | 1 mm | 40 | 85-110 Ω | -1.5db/-2.55db/-3.8db/-7.1db | -12.8db/-10.1db/-22db/-9.1db | -45.5db/-42.5db/-33db/-34.5db | LOW | HBR2/HBR recommended |
| Micro-Coax | 5″ | 1 mm | 40 | 85-110 Ω | -1.57db/-2.75db/-4.5db/-9.1db | -22.7db/-13.5db/-16.5db/-5.5db | -48db/-42.5db/-33.5db/-38db | LOW | HBR2/HBR recommended |
| Micro-Coax | 6″ | 1 mm | 40 | 85-110 Ω | -1.97db/-3db/-5.2db/-9.1db | -12.7db/-20.5db/-17.5db/-9db | -47.3db/-42.5db/-34db/-37.4db | LOW | HBR2/HBR recommended |
| Micro-Coax | 8″ | 1 mm | 40 | 85-110 Ω | -2.35db/-4db/-6.6db/-11.25db | -14.6db/-12.5db/-17db/-8.4db | -50db/-42.5db/-35db/-40db | LOW | HBR2/HBR recommended |
| Micro-Coax | 12″ | 1 mm | 40 | 85-110 Ω | -3.2db/-5.4db/-9.4db/-15.3db | -20.25db/-17db/-18.25db/-7.6db | -49db/-45db/-40db/-44.5db | LOW | HBR2/HBR recommended |
| Micro-Coax | 18″ | 1 mm | 40 | 85-110 Ω | -4.5db/-7.5db/-13.6db/-21db | -23.6db/-17.8/-20.5/-6.5db | -47.2db/-45db/-39db/-43db | LOW | HBR2/HBR recommended |

***Notes:***
1. Differential Insertion Loss, return loss and FEXT values are based on current eDP* channel electrical analysis.
2. Differential Insertion Loss, return loss and FEXT parameters above are for 1.35 GHz / 2.7 GHz / 5.4 GHz / 8.1 GHz respectively

## 6.3 Optimizations

### Table 6-5. Optimization Table for all Topologies

| Description | Recommendation | Value (Units) |
|---|---|---|
| BO/M1 | The traces BO/M1 constitute a breakout and a main route segment pairing. The segments of this pair must be routed on the same layer. | |
| Vias | Use of less number of vias is allowed provided the routing layer guideline for MS/SL/DSL is met | |
| CMC | Recommended PCB CMC or Murata NFP0QHB372HS2. Refer to Section 49.6, "PCB CMC Technology" for more information. | |
| AC CAP | AC caps are required to be placed before the motherboard eDP* connector | **Main Link**<br>nominal 100nF recommended (tolerance 75–265 nF) |
| | | **Aux Channel**<br>nominal 100nF recommended (tolerance 75–200 nF) |
| CFL H PTPS | CFL H uses 12mils Pair to Pair Spacing for equivalent main routing, and 15 mils for Non-Equivalent main routing. (For Equivalent & Non-Equivalent pairs see Ch.2) | |
| Board type | For SL Breakout implementation please place the first via to the left of Breakout (BO) segment. Via BO is allowed to appear inside the BO main route but total length must meet PDG requirements. | |
| SL Breakout implementation | | |
| Inter-pair length mismatch | Maximum length mismatch between the shortest and longest eDP* differential pairs for each port is +/-1″ | |

## 6.3.1 Coffee Lake Processor Graphics Embedded DisplayPort* Main Link Topology for HBR and HBR2

### 6.3.1.1 Main Link

**Figure 6-1. CFL eDP* Main Link Direct Topology**

**Table 6-6. CFL eDP* Main Link Topology for HBR and HBR2**

| Segment | Stack-up | Via Count | Max Length [mils] |
|---|---|---|---|
| B0 | MS/SL | Max 2 vias are allowed | 500 |
| M1 | MS/SL/DSL | | 1000 - 8000 |
| C_I | MS | | 100 |
| Cml | MS | | 1000 |
| Cn | MS | | 500 |
| **Total Length** | | | **2000 - 10000** |
| **eDP* Cable Length** | | | **4000 - 15000** |

***Note:***
1. Reference plane will be Continues GND or Power. GND is preferred.

### 6.3.1.2 Auxiliary Channel

**Figure 6-2. CFL eDP* Auxiliary Channel Topology**

**Table 6-7. CFL eDP* Main Link Auxiliary Channel Topology**

| Segment | Stack-up | Via Count | Max Length [mils] |
|---|---|---|---|
| B0 | MS/SL | Max 2 vias are allowed | 700 |
| M1 | MS/SL/DSL | | 10000 |
| CI | MS | | 10000 |
| CN | MS | | 750 |
| **Total Length** | | | **10000** |
| **eDP* Cable Length** | | | **4000 - 15000** |

***Note:***
1. Reference plane will be Continues GND or Power. GND is preferred.

***Note:*** Reference plane will be Continues GND or Power. GND is preferred.

## 6.3.2 Embedded DisplayPort* to VGA Main Link Topology

### 6.3.2.1 Main Link

**Figure 6-3. CFL eDP* Main Link Direct DP to VGA Topology**

**Table 6-8. CFL H Display Port Main Link Direct DP to VGA Topology**

| Segment | Stack-up | Via Count | Max Length [mils] |
|---|---|---|---|
| B0 | MS/SL | Max 2 vias are allowed | 500 |
| M1 + C_I | MS/SL/DSL | | 6500 |
| Cn | MS | | 1000 |
| **Total Length** | | | **6900** |

***Notes:***
1. DP to VGA converter must meet DP spec
2. Converter to connector must follow Vendor application note.

### 6.3.2.2 Auxiliary Channel

**Figure 6-4. CFL eDP* Aux Channel DP to VGA Converter Topology A**

**Table 6-9. CFL eDP* Aux Channel DP to VGA Converter Topology**

| Segment | Stack-up | Via count | Max Length [mils] |
|---|---|---|---|
| B0 | MS/SL | Max 2 vias are allowed | 700 |
| M1 + C_I | MS/SL/DSL | | 7000 |
| Cn | MS | | 7000 |
| **Total Length** | | | 13000 |

***Notes:***
1. DP to VGA converter must meet DP spec
2. Converter to connector must follow Vendor application note.

## 6.3.3 Embedded DisplayPort* Hot-Plug Detect Implementation

Hot-plug detect (HPD) is an output from eDP* sink device and it is a active high signal.

***Note:*** When using eDP bifurcation for DP-VGA Topology, need to use HPD for DDIE (DDPE_HPD) for HPD connectivity.

**Figure 6-5. Embedded DisplayPort* HPD Signal**

## 6.4 Length Matching Guidelines

For matching methodology, refer to General Differential Design Guidelines chapterChapter 3, "General Differential Design Guidelines".

## 6.5 Digital Display Interface Compensation Guidelines

The compensation input is used by the circuitry to determine, check and adjust the system buffer output strength and characteristic impedance over temperature, process and voltage variations. This is done by comparing its buffer impedance against a standard reference resistor, RCOMP.

***Note:*** The RCOMP signals should be referenced to Vss and noisy or switching references should be avoided. As board space allows, recommend to add a VSS shield at least 4 mils wide placed between RCOMP and adjacent IO.

Coffee Lake processor signal DISP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor. DISP_RCOMP is DDI I/O compensation resistor which supports DP, eDP* and HDMI* channels.

**Figure 6-6. Embedded DisplayPort* Compensation Signal Routing Topology**

### 6.5.1 Compensation Signal Routing Guidelines

**Table 6-10. DISP_RCOMP Guideline**

| Signal | Min Trace Width | Isolation Spacing | Resistor Value | Max Length |
|---|---|---|---|---|
| DISP_RCOMP | 5 mils | 20 mils | 24.9 Ω ±1% | 600 mils |
| ***Note:*** Must maintain low DC resistance routing (<0.1Ω) | | | | |

### 6.5.2 Disabling and Termination Guidelines

**Table 6-11. eDP* Disabling and Termination Guidelines**

| Pin name | Recommendation |
|---|---|
| eDP_TXN/P[3:0] | No connect |
| EDP_AUXN/P | No connect |
| eDP_HPD | Pull down to ground via 100k Ω resistor |
| DISP_RCOMP | Pull up to VCCIO via 24.9 Ω resistor |
| eDP_DISP_UTIL | No connect |

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# 7 High-Definition Multimedia Interface* (HDMI*) Design Guidelines

The Integrated High-Definition Multimedia Interface* (HDMI*) transmits digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays.

HDMI* is a display interface connecting the Coffee Lake processor and PCH with display devices that utilizes transition minimized differential signaling (TMDS) to carry audio-visual information through the same HDMI* cable.

## 7.1 Overview

HDMI* includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) however CEC is not supported. The data and clock channels are used to carry video, audio and auxiliary data. In addition, HDMI* carries a VESA display data channel (DDC). The DDC channel is used by an HDMI* source to determine the capabilities and characteristics of the sink.

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels.

**Figure 7-1. HDMI* Overview**

There are three digital display interface channels or ports available that can be configured as HDMI. Each channel or port of HDMI* is comprised of three differential data lanes, and an associated differential-clock, Hot Plug Detect signal (HPD) and two Display Data Channel (DDC) signals. The maximum data rate supported for HDMI* is 2.97 Gb/s for specific configurations.

In order to support HDMI* 2.0, we are adding an external DP-HDMI* 2.0 Level-Shifter/ Protocol Converter (LS-PCon) device. The LS-PCon device contains two functions:

1. A DisplayPort* Dual-mode Type 2 Adaptor Function that supports HDMI* 1.4b up to 3.4 Gbps.
2. A DP Branch Device with a DP-to-HDMI2.0 Protocol Converter Function that supports HDMI* 2.0 up to 5.94 Gbps through protocol conversion from DP (HBR2) to HDMI* 2.0

This scheme is also backward compatible with HDMI* 1.4b spec with up to 2.97 Gb/s. The detailed protocol and electrical properties of this device can be found at Intel LSPCON specification.

**Figure 7-2. HDMI* 2.0 Overview**

## Table 7-1. Mapping of HDMI* Signals for DDI Ports

| Port | Digital Display Interface Pins | CRB Digital Display Interface Signals | HDMI* Signals |
|---|---|---|---|
| Port 1 | DDI1_TXP[0] | DDI1_LANE0_DP | HDMIx_TX2_DP |
| | DDI1_TXN[0] | DDI1_LANE0_DN | HDMIx_TX2_DN |
| | DDI1_TXP[1] | DDI1_LANE1_DP | HDMIx_TX1_DP |
| | DDI1_TXN[1] | DDI1_LANE1_DN | HDMIx_TX1_DN |
| | DDI1_TXP[2] | DDI1_LANE2_DP | HDMIx_TX0_DP |
| | DDI1_TXN[2] | DDI1_LANE2_DN | HDMIx_TX0_DN |
| | DDI1_TXP[3] | DDI1_LANE3_DP | HDMIx_CLK_DP |
| | DDI1_TXN[3] | DDI1_LANE3_DN | HDMIx_CLK_DN |
| | Hot plug detect used by HDMI Port 1 | DDPB_HPD | DDI1_HPD_Q |
| | HDMI DDC lines for Port 1 | DDPB_CTRLCLK | DDI1_CTRL_CK |
| | | DDPB_CTRLDATA | DDI1_CTRL_DATA |
| Port 2 | DDI2_TXP[0] | DDI2_LANE0_DP | HDMIx_TX2_DP |
| | DDI2_TXN[0] | DDI2_LANE0_DN | HDMIx_TX2_DN |
| | DDI2_TXP[1] | DDI2_LANE1_DP | HDMIx_TX1_DP |
| | DDI2_TXN[1] | DDI2_LANE1_DN | HDMIx_TX1_DN |
| | DDI2_TXP[2] | DDI2_LANE2_DP | HDMIx_TX0_DP |
| | DDI2_TXN[2] | DDI2_LANE2_DN | HDMIx_TX0_DN |
| | DDI2_TXP[3] | DDI2_LANE3_DP | HDMIx_CLK_DP |
| | DDI2_TXN[3] | DDI2_LANE3_DN | HDMIx_CLK_DN |
| | Hot plug detect used by HDMI Port 2 | DDPC_HPD | DDI2_HPD_Q |
| | HDMI DDC lines for Port 2 | DDPC_CTRLCLK | DDI2_CTRL_CK |
| | | DDPC_CTRLDATA | DDI2_CTRL_DATA |
| Port 3 | DDI3_TXP[0] | DDI3_LANE0_DP | HDMIx_TX2_DP |
| | DDI3_TXN[0] | DDI3_LANE0_DN | HDMIx_TX2_DN |
| | DDI3_TXP[1] | DDI3_LANE1_DP | HDMIx_TX1_DP |
| | DDI3_TXN[1] | DDI3_LANE1_DN | HDMIx_TX1_DN |
| | DDI3_TXP[2] | DDI3_LANE2_DP | HDMIx_TX0_DP |
| | DDI3_TXN[2] | DDI3_LANE2_DN | HDMIx_TX0_DN |
| | DDI3_TXP[3] | DDI3_LANE3_DP | HDMIx_CLK_DP |
| | DDI3_TXN[3] | DDI3_LANE3_DN | HDMIx_CLK_DN |
| | Hot plug detect used by HDMI Port 3 | DDPD_HPD | DDI3_HPD_Q |
| | HDMI DDC lines for Port 3 | DDPD_CTRLCLK | DDI3_CTRL_CK |
| | | DDPD_CTRLDATA | DDI3_CTRL_DATA |

## Table 7-2. HDMI* Interface Reference Documents

| Title | Document Number/Location |
|---|---|
| High-Definition Multimedia Interface Specification Version 1.4b | *http://www.hdmi.org* |
| High speed internal Connector and Cable Specification | 549136 |

### Table 7-3. HDMI* Interface Compliance Documents

| Title | Location |
|---|---|
| High-Definition Multimedia Interface Compliance Test Specification 1.4b | *http://www.hdmi.org* |

## 7.2 Signal Description

### Table 7-4. HDMI* Signals

| Description | Signal Mapping | | |
|---|---|---|---|
| | Processor | PCH | CRB HDMI* Connector |
| Main Link (Tx) | DDIx_TXP[3:0] and DDIx_TXN[3:0] | N/A | HDMIx_OB_DATA[2:0]_DP and HDMIx_OB_CK_DP<br>HDMIx_OB_DATA[2:0]_DN and HDMIx_CK_DN |
| DDC | DDPx_CTRLCLK/ CTRLDATA | N/A | DDIx_CTRL_CK/CTRL_DATA |
| Hot Plug Detect | N/A | DDPx_HPD | DDIx_HPD_Q |

## 7.3 HDMI 1.4* Topology Guidelines

The following are the topologies supported for HDMI* Data and Clock:

- Cost Reduced Level Shifter Motherboard Topology for max data rate of 1.65Gb/s
- Active Level Shifter Motherboard Topology for max data rate of 2.97 Gb/s
- Active Level Shifter Docking Topology
- Active Level Shifter Docking Multiplexed Topology Internal Cabled Solution

### 7.3.1 Differential-Pair Width and Spacing

HDMI* supports MS/SL/DSL. Follow the guidelines in “Printed Circuit Board (PCB) Considerations”.

### 7.3.2 Optimizations

### Table 7-5. Optimization Table for all Topologies (Sheet 1 of 2)

| Description | Recommendation | |
|---|---|---|
| AC CAP | AC caps are required to be placed before the motherboard HDMI* connector | nominal 100nF recommended (tolerance 75-200 nF) |
| CN Via | The via before the CN segment is to enable backside entry of the connector. Intended to eliminate a stub on the through hole HDMI* connector. | |
| BO/M1 | The traces BO/M1 constitute a breakout and a main route segment pairing. The segments of this pair must be routed on the same layer. | |
| Active Level Shifter (Tx/Rx) | Select the optimized receive and transmit equalization settings for the active level shifter to meet the compliance at the HDMI* connector. | |
| CMC | Recommended PCB CMC or Murata NFP0QHB372HS2. Refer to Section 49.6, “PCB CMC Technology” for more information. | |
| ESD | | |
| DSL Routing | No broadside/parallel routing on the adjacent DSL layer on 8/10 layer stack-up | |

**Table 7-5. Optimization Table for all Topologies (Sheet 2 of 2)**

| Description | Recommendation |
|---|---|
| CFL H PTPS | CFL H uses 12mils Pair to Pair Spacing for equivalent main routing, and 15 mils for Non-Equivalent main routing. (For Equivalent & Non-Equivalent pairs see Ch.2) |
| SL Breakout (BO) implementation | For SL Breakout implementation please place the first via to the left of Breakout (BO) segment. Via BO is allowed to appear inside the BO main route but total length must meet PDG requirements. |
| Inter-pair length mismatch | maximum length mismatch between the shortest and longest HDMI* differential pairs for each port is 2” |
| Inter-pair skew requirement | For HDMI* signals is +/-1” |

## 7.3.3 HDMI 1.4* Main Link Cost-reduced Level Shifter Topology

**Figure 7-3. CFL HDMI 1.4* Main Link Cost-reduced Level Shifter Motherboard Topology**

**Table 7-6. CFL HDMI 1.4* Main Link Cost-reduced Level Shifter Motherboard Topology Guidelines**

| Segment | Via Count | CFL H | |
|---|---|---|---|
| | | Stack-up | Max Length [mils] |
| B0 | Max 3 vias are allowed | MS/SL | 400 |
| M1 | | MS/SL/DSL | constrained by total length |
| Capl | | MS | 100 |
| Cml | | MS | 600 |
| Esdl | | MS | 600 |
| Cn | | MS | 600 |
| Cml+Esdl+Cn | | MS | 600 |
| Rt-R | | MS | 500 |
| **Total Length** | | **6500** | |

***Notes:***
1. Rt = 470ohm
2. ESD is recommended. CMC is optional (recommended to leave footprint on platform)
3. Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).

## 7.3.4 HDMI 1.4* Main Link Active Level Shifter Topology

**Figure 7-4. CFL HDMI 1.4* Main Link Active Level shifter Motherboard Topology**

**Table 7-7. CFL H HDMI 1.4* Main Link Active Level shifter Motherboard Topology Guidelines**

| Segment | Via Count | Stack-up | Max Length [mils] |
|---|---|---|---|
| B0 | Max 3 vias are allowed | MS/SL | 400 |
| M1 | | MS/SL/DSL | 5500 |
| C_I | | MS | 5500 |
| LSL | | MS | 500 |
| M1+C_I+LSL | | MS | 6000 |
| LSR+Cn | | MS | 1000 |
| **Total Length** | | **6500** | |

***Notes:***
1. Topology supports Non Re-time Active Level Shifter
2. Max 3 Vias are allowed.
3. Must use appropriate level shifter for maximum desired data rate.
4. ESD is recommended. CMC is optional (recommended to leave footprint on platform)
5. Retimer Sideband Communication - Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT)

**Figure 7-5. CFL H HDMI 1.4* Main Link Active Level shifter Multiplexed Topology**

### Table 7-8. CFL H HDMI 1.4* Main Link Active Level shifter Multiplexed Topology Guidelines

| Segment | Via Count | Stack-up | Max Length [mils] |
|---|---|---|---|
| B0 | Max 3 vias are allowed | MS/SL | 500 |
| M1 | | MS/SL/DSL | 6000 |
| Muxl | | MS | 500 |
| LSL | | MS | 6000 |
| LSR + Cn | | MS | 800 |
| **Total Length** | | **6000** | |

***Notes:***
1. Must use appropriate level shifter for maximum desired data rate.
2. ESD is recommended. CMC is optional (recommended to leave footprint on platform)
3. Assumed Passive Mux
4. Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).

## 7.3.5 HDMI 1.4* Docking Active Level Shifter Docking Topology

**Figure 7-6. CFL H HDMI 1.4* Main Link Active Level shifter Docking Topology**

**Table 7-9. CFL H HDMI 1.4* Main Link Active Level shifter Docking Topology Guidelines**

| Segment | Stack-up | Max Length [mils] |
|---|---|---|
| B0 | MS/SL | 400 |
| M1 | MS/SL/DSL | 7100 |
| DKL | MS | 1000 |
| DKR | MS | 500 |
| LSL | MS | 2000 |
| LSR+Cn | | 1000 |
| **Total Length** | **11000** | |

***Notes:***
1. Must use appropriate level shifter for maximum desired data rate.
2. ESD is recommended. CMC is optional (recommended to leave footprint on platform)
3. Retimer Active Level Shifter.

**Figure 7-7. CFL H HDMI 1.4* Main Link Active Level shifter Docking Multiplexed Topology**

**Table 7-10. CFL H HDMI 1.4* Main Link Active Level shifter Docking Multiplexed Topology Guidelines (Sheet 1 of 2)**

| Segment | Stack-up | Max Length [mils] |
|---|---|---|
| B0 | MS/SL | 400 |
| M1+Muxl | MS/SL/DSL | 7100 |

### Table 7-10. CFL H HDMI 1.4* Main Link Active Level shifter Docking Multiplexed Topology Guidelines (Sheet 2 of 2)

| Segment | Stack-up | Max Length [mils] |
|---|---|---|
| DKL | MS | 1000 |
| DKR | MS | 500 |
| LSL | MS | 2000 |
| LSr + Cn | MS | 1000 |
| **Total Length** | **11000** | |

***Notes:***
1. Must use appropriate level shifter for maximum desired data rate.
2. ESD is recommended. CMC is optional (recommended to leave footprint on platform)
3. Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).
4. Docking topology assumes Re-time Active level Shifter.
5. ALS may contain integrated ESD devices not shown in the diagram
6. Retimer Active Level Shifter.

## 7.3.6 HDMI 1.4* Internal Cabled Solution

### Figure 7-8. CFL HDMI 1.4* Internal Cabled Solution Topology

### Table 7-11. CFL H HDMI 1.4* Internal Cabled Solution Topology Routing Guidelines (Sheet 1 of 2)

| Segment | Via Count | Stack-up | Max Length [mils] | | | |
|---|---|---|---|---|---|---|
| Internal Cable Assembly Insertion Loss recommendation up to 1.5 GHz | | dB | **<=0.5** | **<=0.9** | **<=1.3** | **<=1.7** |
| Reference Cable length (AWG38 100 ohm uCoax) | | | 5000 | 10000 | 15000 | 20000 |

**Table 7-11. CFL H HDMI 1.4* Internal Cabled Solution Topology Routing Guidelines (Sheet 2 of 2)**

| Segment | Via Count | Stack-up | Max Length [mils] | | | |
|---|---|---|---|---|---|---|
| BOL+BOR | Max 3 vias are allowed | MS/SL | 400 | 400 | 400 | 400 |
| M1+M2 | | MS/SL/DSL | 4000 | 3500 | 3000 | 2500 |
| BOL+BOR+M1+M2 | | MS/SL/DSL | 4000 | 3500 | 3000 | 2500 |
| Cap_L+LS_L | | MS | 1000 | 1000 | 1000 | 1000 |
| LS_R | | MS | 1000 | 1000 | 1000 | 1000 |
| CN | | MS | 1000 | 1000 | 1000 | 1000 |
| LS_R+CN | | MS | 1000 | 1000 | 1000 | 1000 |
| Cap_L+LS_L+LS_R+CN | | MS | 2000 | 2000 | 2000 | 2000 |

***Notes:***
1. Must use appropriate level shifter for maximum desired data rate.
2. ESD is recommended. CMC is optional (recommended to leave footprint on platform)
3. Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT)
4. Far-end crosstalk for cable assembly is assumed to be <=-50dB up to 4.5GHz
5. Beyond the fundamental frequency (1.5GHz), the insertion loss curve is assumed to be reasonably smooth up to 4.5GHz

## 7.3.7 HDMI 1.4* (DDC) Signals Design Guidelines

CRTLDATA and CRTLCLK are single ended signals used for communications between the PCH, add-in card and a panel device (Sink). These two signals follow $I^2C$ specifications and HDMI DDC load (750 pF) when they operate in the standard mode of frequency of 100-kHz. Any port configured to support HDMI must implement sideband communications via the DDC channel associated with that HDMI port as defined in the Video BIOS Table (VBT). Sideband communion using I2C over AUX is not supported.

### 7.3.7.1 HDMI 1.4* DDC Signals on Motherboard Topologies with Cost-reduced Level Shifter, Active Level Shifter and Docking Active Level Shifter

**Figure 7-9. CFL HDMI 1.4* DDC Graphics Active Level Shifter Docking Topology**

***Notes:***
1. 3.3V and 5V should be core rail which will turn off in sleep states.
2. If Level Shifter has integrated resistors, Schottky diode and corresponding integrated resistors are not required.
3. If total length of DDC signals is less than max allowed length of HDMI main link signals, then DDC main route can use 12 mils Pair To Pair Spacing, otherwise DDC Pair To Pair Spacing needs to be 15 mils.

**Figure 7-10. CFL HDMI 1.4* DDC Graphics Active Level Shifter Topology**

***Notes:***
1. 3.3V and 5V should be core rail which will turn off in sleep states.
2. If Level Shifter has integrated resistors, Schottky diode and corresponding integrated resistors are not required.

## Figure 7-11. CFL HDMI 1.4* DDC Cost-reduced Level Shifter Design Recommendation

## Table 7-12. CFL H HDMI 1.4* DDC Routing Guidelines (Sheet 1 of 2)

| Description | Parameter | Stackup | Units | Cost Reduced Level Shifter | Active Level Shifter | Docking Active Level Shifter |
|---|---|---|---|---|---|---|
| | | | | Routing Recommendations | | |
| Coffee Lake Processor Breakout Max | BO | MS/SL/ DSL | mils | 500 | 500 | 500 |
| Main Route | M1 | MS/SL/ DSL | mils | Constrained by Total Motherboard Length Max from Coffee Lake processor to HDMI connector | | |
| M1 to R1 | Rt-L | MS | mils | 1000 | 1000 | 1000 |
| Routing from MB to Docking connector | DK-L | MS | mils | Constrained by Total Motherboard Length Max from Coffee Lake processor to HDMI connector | | |
| Routing on the docking connector | DK-R | MS | mils | Constrained by Total Motherboard Length Max from Coffee Lake processor to HDMI connector | | |
| Routing to Level Shifter Length Max | LS-L | MS/SL/ DSL | mils | Constrained by Total Motherboard Length Max from Coffee Lake processor to HDMI connector | | |
| Level shifter to RT-L Length Max | LS-R | MS/SL/ DSL | mils | Constrained by Total Level Shifter to HDMI connector Length Max | | |
| RT-L to HDMI Conn Length Max | CN | MS | mils | Constrained by Total Level Shifter to HDMI connector Length Max | | |
| Docking connector to Level Shifter Total Length max | DK-R+LS-L | MS | mils | NA | NA | 500 |
| **Total Level Shifter to HDMI connector Length Max** | LS-R+CN | MS | mils | 1500 | 1500 | 1500 |
| **Total Motherboard Length Max** | Sum (BO to CN) | Refer Topology | mils | 10000 | 10000 | 10000 |
| **Passive / Active Devices** | | | | | | |
| Max Capacitance (Backdrive I Protection) | Schottky Diode | NA | pF | 10 | 10 | 10 |
| Resistor Value (+/- 5%) | R1 | NA | Ω | 2.2K | 2.2K[2] | 2.2K[2] |
| Resistor Value (+/- 5%) | R2 | NA | Ω | 2.2K | 2.2K[3] | 2.2K[3] |

**Table 7-12. CFL H HDMI 1.4* DDC Routing Guidelines (Sheet 2 of 2)**

| Description | Parameter | Stackup | Units | Cost Reduced Level Shifter | Active Level Shifter | Docking Active Level Shifter |
|---|---|---|---|---|---|---|
| | | | | Routing Recommendations | | |
| ESD Protection | ESD | NA | NA | Required | Assumed to be contained within level shifter | Assumed to be contained within level shifter |

***Notes:*** |
1. DDC signals follow I2C guidelines. Refer to chapter 20.
2. Stuff R1 on motherboard if no equivalent internal Pull-up inside Active Level Shifter
3. Stuff R2 on motherboard if no equivalent internal Pull-up inside Active Level Shifter
4. Total length from driver to HDMI connector is limited by Spec Capacitance limit of 50pF including trace capacitance and discrete. Refer Chapter 23, "I2C* Interface Design Guidelines" Refer for calculation details.
5. nFET Ron should be <3ohms and Cout < 10pF
6. ESD protection is recommended. However, if ALS chip have sufficient inbuilt ESD protection and trace length from Als to connector is <1", diodes may not be required.

## 7.3.8 HDMI 1.4* HPD Implementation

The hot-plug detect output from HDMI* sink is a 5V active high signal. The hot-plug detect input at the Coffee Lake processor is a 3.3V active high signal (refer to the EDS for DC specifications). A level shifter is required on the motherboard to convert the 5V signal from HDMI* sink device to 3.3V signals for the Coffee Lake processor. However, logic inversion is not required for this signal. Also, make sure necessary protection circuitry is in place to prevent back-drive current from damaging the Coffee Lake processor when the sink device is powered off.

Ensure HDMI* connector HPD is not directly connected to the Coffee Lake processor. Level shifter should have pass-gate circuit, if not then it is recommended to use pass-gate circuit for HPD. Refer figures below for implementation of an Active Level Shifter or a Cost Reduced Level Shifter HPD topology.

***Note:*** If the display connector is on the docking station, the hot-plug circuitry should remain on main motherboard and not on the docking station in order to prevent display detection failures related to hot-plug and S-state resume. HPD signal should not be allowed to float anytime.

**Figure 7-12. HDMI 1.4* HPD Active Level Shifter Design Recommendation**

**Figure 7-13. HDMI 1.4* HPD Cost Reduced Level Shifter Design Recommendation**

***Note:*** 3.3V transistor gate supply must turn off when CPU power is turned off.

## 7.4 HDMI* 2.0 Topology Guidelines

### Figure 7-14. CFL H LSPCON Main Link Direct MB Topology

### Table 7-13. CFL H LSPCON Main Link Direct MB Topology Guidelines

| Segment | Via Count | Stack-up | Max Length [mils] |
|---|---|---|---|
| B0 | Max 3 vias are allowed | MS | 500 |
| M1 | | MS | 5500 |
| M1+C_I | | MS | 6000 |
| LSPCON | | MS | 1000 |
| LS-R+Cn | | MS | LSPCON Spec |
| **Total Length** | | **6500** | |

***Notes:***
1. ESD should be integrated in LSPCON.
2. CMC is optional (recommended to leave footprint on platform)
3. Recommend to have reserve probing locations for LSPCON input link and testing pins.
4. reserve probing locations for LSPCON input link and testing pins.

### Figure 7-15. CFL H Type 3 HDMI 2.0 DDC Topology

### Table 7-14. CFL H Type 3 HDMI 2.0 DDC Topology

| Description | Parameter | CFL H | Units | CFL H LSPCON DDC Routing Recommendations |
|---|---|---|---|---|
| Coffee Lake Processor Breakout Max | BO | MS/SL/DSL | mils | 500 |
| Main Route | M1 | MS/SL/DSL | mils | Constrained by Total Motherboard Length Max |
| Cap to LSPCON length Max | C_l+ Lspconl | MS/SL/DSL | mils | Constrained by Total Motherboard Length Max |
| LSPCON to via length max | Lspconr | MS/SL/DSL | mils | Constrained by Total Motherboard Length Max |
| Via to connector Length Max | Cn | MS | mils | Constrained by Total Motherboard Length Max |
| LSPCON to HDMI connector length Max | Lspconr+Cn | MS | mils | 1500 |
| **Total Motherboard Length Max** | Sum (BO to CN) | - | mils | 13000 |
| **Passive / Active Devices** | | | | |
| Max Capacitance (Backdrive I Protection) | Schottky Diode | NA | pF | 10 |
| Resistor Value (+/- 5%) | R2 $_t$ | NA | Ω | 2.2K* |
| ESD Protection | ESD | NA | NA | assumed to be contained within LSPCON |
| Max nFET Ron/Cout | NA | NA | Ω /pF | 3Ω/10pF |
| ***Notes:***<br>1. Stuff R2 on motherboard if no equivalent internal Pull-up inside Active Level Shifter.<br>2. AC caps range is 75 to 200nF (nominal 100nF). | | | | |

## 7.4.1 HDMI 2.0* HPD Implementation

### Figure 7-16. HDMI 2.0* HPD Implementation

***Note:*** Follow vendors' recommendation to protection against non-compliance HDMI sink which provide low impedance 5V connection to HPD pin and back drive from during off state

## 7.5 Digital Display Interface Disabling and Termination Guidelines

Refer to Section 5.6, "Digital Display Interface Disabling and Termination Guidelines" for HDMI* disabling and termination guidelines

## 7.6 Display Compensation Guidelines

Refer to Section 5.7, "Display Compensation Guidelines" for details.

***Note:*** There is one comp pin (eDP_RCOMP) that is shared among all display ports.

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# 8 Processor - PCI Express* Design Guidelines

## 8.1 Introduction

PCI Express* is a 16-lane interface. The guidelines in the chapter cover PCI Express operation at 2.5-GT/s,5-GT/s and 8GT/s.

### 8.1.1 Compliance Documents

| Title | Doc #/Location |
|---|---|
| PCI Express Base Specification Rev 3.0 | www.pcisig.com |

## 8.2 Signal Description

**Table 8-1. PCI Express* Signal Groups**

| Signal Group | Signal Name | Description |
|---|---|---|
| Input PCI Express* | PEG_RX#[15:0]<br>PEG_RX[15:0] | PCI Express* Receive Differential Pair |
| Output PCI Express* | PEG_TX#[15:0]<br>PEG_TX[15:0] | PCI Express* Transmit Differential Pair |
| COMP | PEG_RCOMP | PCI Express* and DMI Compensation |

## 8.3 Topologies Guidelines

***Note:*** The length difference between lanes (longest to shortest lane) within a PCIe port should not be bigger than 2".

**Figure 8-1. CFL H - PCI Express* Device Down Topology**

**Figure 8-2. CFL H - PCI Express* Add-In Card Topology**

## Table 8-2. Coffee Lake H Design Topologies (Add-In Card and Device Down)

| Description | Parameter | Stackup | Units | Halo AIC Topology | Halo Device Down (DD) Topology |
|---|---|---|---|---|---|
| | | | | Routing | Routing |
| Data Rate | NA | NA | Gbps | 2.5/5/8 | 2.5/5/8 |
| CFL Processor Breakout | BO | uS/SL/DSL | mils | 500 | 500 |
| Main Route Segment Max | M1 | uS/SL/DSL | mils | 7000 | 7000 |
| Cap to Connector | BI | uS | mils | 300 | 300 |
| Total Route Length | Sum BO to BI | per segment | mils | 2000-7000 | 3000-8000 [3] / 3000-9000 [4] |
| **Passive Devices** | | | | | |
| ac cap value Gen1 or Gen2 | Min=75nf Max=265nf | | | | |
| ac cap value Gen3 | Min=180nf Max=265nf | | | | |

***Notes:***
1. Halo use 12mil PTPS
2. Non Interleave route is recommended for Xtalk reduction
3. For 4 via topology
4. For 2 via topology

Add-In Card topology assumptions:

- In the RVP topology, the add-in card is assumed to have up to 3.5 inches of max length for DT form factor designs.
- The add-in card is assumed to have up to 2.0 inches of max length for AIO form factor designs.

**Add-In Card Topology Assumptions:**

1. The topologies in this section assume that AC-caps are placed on the platform for both Rx and Tx lanes. Such topologies are commonly required when using low-profile, horizontally mounted (with surface mounted connectors) Add-in cards, which require AC-caps to be placed on the platform.
2. The recommendations detailed in this section are for a non-interleaved routed add-in card solution only, i.e., Tx and Rx lanes are routed on different layers. If different routing implemented in add-in card, simulations are required to validate interoperability. When implementing an add-in card design based on an industry specification outside of Intel, one should consult with those design specifications and recommendations to ensure an operational and interoperable design.
3. The add-in card is assumed to have up to 2.0 inches of max length for AIO form factor designs.

## 8.4 General Routing Guidelines

### 8.4.1 Reference Planes

Referencing signals going over a board-to-board connector must be considered and stitching capacitors added at the connector as appropriate. For example, if a differential-pair is GND-referenced on the motherboard and the pair is $V_{CC}$ referenced on the daughter card, then stitching capacitors must be added at the connector between $V_{CC}$ and GND.

### 8.4.2 Lane to Controller Allocation

The PCI Express has 16 physical lanes that can be configured in several ways, it can be configured by a single controller as a 16-lane interface, or with two controllers to form a two 8-lane interfaces. It can be configured to be 1 x 8 lane and 2 x 4 lanes interfaces with three controllers. These types of configurations are determined statically by BIOS prior to initialization of the port(s). BIOS may look at card "presence detect" pins to change this setting.

The 16 lanes are associated with root port of device 1
Function 0 refers to the controller of the x16
Function 1 refers to the controller of the x8
Function 2 refers to the controller of the x4

Figure 8-3 shows the x16 lanes port split for the three controller connection to the physical lanes. Note that the external switches in the diagram may not be possible in GEN2 and GEN3 rates.

**Figure 8-3. x16 Lanes Port Splitting**

### 8.4.2.1 Static Lane Reversal Support

The Processor has two strap pins that will be driven by card detect of port B and C. This will allow the platform to enable the second and third controllers and control the external switches for GEN 1 rates. The root port supports static lane reversal. BIOS reference code may not fully support preset search algorithm on systems with lane reversal on PCIe ports. BIOS will fully support GEN 3 by use of presets programmed at customer discretion with Intel guidance. The target for the lane reversal support is to ease mother board layout. Card layout is not supported and should be handled by downstream device.

For the shared 16 lanes only one reversal option is supported regardless of the port split. This allows to design motherboard with straight or rotated processor relative to the PCI Express* slots or to rotate all the slots together. There is no support for different slots having different orientation.

**Figure 8-4. Card Presence Detect Pin Connections**

**Figure 8-5. x16 Configuration with Flipped Processor**

Figure 8-5 shows the configuration on how to connect the x16 lanes with a flipped processor die connection.

## Figure 8-6. x16 Configuration with Flipped Socket

### Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

| x16 Controller Negotiated Width | x8 Controller Negotiated Width | x4 Controller Negotiated Width | Processor | Physical Lanes | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| x16 | Off | Off | Direct | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| x8 | x8 | Off | Direct | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| x8 | x4 | x4 | Direct | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 |
| x16 | Off | Off | Reverse | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| x8 | x8 | Off | Reverse | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| x8 | x4 | x4 | Reverse | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

***Notes:***
1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

### Table 8-4. PCIe* Configurations

| Configuration | PCIe Slot Clock |
|---|---|
| 1x16 | Customer can use any of the available clock out signals. For example CLKOUT_PCIE_8 was used on RVP. |
| 2x8 | Customer can use any of the two available clock signals. For example CLKOUT_PCIE_10 and CLKOUT_PCIE_14 |
| 1x8+2x4 | Customer can use any of the three available clock signals. For example CLKOUT_PCIE_11, CLKOUT_PCIE_12 and CLKOUT_PCIE_13 |

## 8.5 Slot Reset Implementation

AND gate implementation (with inputs –PLTRST# and PCH GPP_F22) should be used for resetting PEG slots. This circuit provides an option to reset PEG slots using BIOS-controlled GPP_F22 during debug, without resetting the entire platform.

A jumper should be added near the PEG slots to select between the PLTRST# directly OR the ANDed output of PLTRST# and GPP_F22. GPP_F22 should follow same routing guidelines as platform reset.

The BIOS needs to ensure that GPP_F22 is configured as output high for normal operation. This circuit will take effect and reset PEG slots only when GPP_F22 is driven low.

PCIe Gen3 margining and functional link training can occasionally hang PEG devices (slots or down). To ensure proper system functionality, Intel recommends implementing a circuit that allows the BIOS to reset the PEG device, independent of PLTRST#. The reference circuit on the Coffee Lake H RVP uses GPP_F22 to control the

auxiliary reset circuit, but the BIOS Reference Code allows a different GPIO to be used, if necessary for the system design flexibility. Unless necessary, customers are advised to use the default GPIO selection. Equivalent reset circuits are also acceptable. The auxiliary reset circuit is only required for PCIe Gen3 implementations.

## 8.6 Debug Guidelines

The inclusion of test points and probing structures may impact the loss and jitter budgets of a PCI Express interconnect. In general, test points and probe structures should not introduce stubs on the differential pairs or cause significant deviation from the recommendations given throughout this chapter. Existing vias, pads or pins should be used wherever possible to accommodate such structures. Careful consideration must be taken whenever additional probing structures are used.

### 8.6.1 Probe Points for Testing Soldered Down PCI Express* Devices

In order to actively characterize the transmit path signal quality for a soldered down PCI Express* device, there must be a terminated probing point on the motherboard very near the soldered down device. This probing point may affect the overall signal quality of the system during normal operation due to the effects of stubs and impedance mismatches of the traces themselves.

The probing point requires populating a resistor stuffing option that can be used to break the path to the device very near the device pins and ideally terminate each line (TX+/TX-) to ground through a 50 Ω 1% resistor. Also, an AC coupling capacitor is required near the device pins. The resistor package/footprint must be as small as possible, preferably size 0402. The population of a 50-Ω resistor, as shown in Figure 8-7, will force the transmitting silicon (host or add-in card) to enter the compliance mode and begin transmitting the compliance packet. The population of two 0-Ω resistors will allow normal operation of the device. One replace the AC coupling cap, the other connects the channel.

**Figure 8-7. Board Preparation Example**

## 8.6.2 Desktop Form Factor Passive Components and Connectors

### 8.6.2.1 Desktop Form Factor AC Coupling Capacitor Placement Guidelines

The *PCI Express* Specification* requires that each lane of a PCI Express* link be AC coupled between the driver and receiver. The specification allows for the actual AC coupling capacitors to be located either on or off the die. However, it is anticipated that in most cases the AC coupling will be separate from the die and in the form of discrete capacitors on the PCB board itself. Use the following guidelines for AC coupling capacitors:

- For add-in cards, the AC coupling capacitors are located on the card itself for each of the TX pairs originating from the add-in card PCI Express* device and going to a RX pair on the motherboard. For the motherboard, the AC coupling capacitors are required on the motherboard itself for the TX pairs originating from the motherboard PCI Express* device and going to the add-in card's RX pairs.
- Dielectric properties are not a major consideration for PCI Express* AC coupling capacitors. It is anticipated that any type from COG capacitors to X7R is acceptable as long as the capacitors meet all other requirements.

**Table 8-5. Desktop Form Factor AC Coupling Capacitor Guidelines**

| Parameter (For AC Coupling Capacitors) | Requirement |
|---|---|
| Cap size | • 0402<br>• C-packs are **not** allowed |
| Cap Value | • 180 nF min<br>• 265 nF max<br>• Cap values must be the same for each signal in a differential pair<br>• Recommend using a nominal Cap Value of 220 nF |
| Cap Value Tolerance | • Not applicable as long as specified min/max range is met when the tolerance is considered. |
| Cap Placement—Coupled Pair | • Must be placed at same exact location within the two signal lines<br>• Symmetric routing into the caps and matched line lengths on either side of the caps for each line of the diff pair. |

Each lane of a PCI Express link must be AC coupled between the driver and receiver. The PCIe specification allows for the AC coupling capacitors to be located either on or off the die. However, in most cases the AC coupling is separated from the die and is in the form of discrete capacitors on the motherboard. Use the following guidelines for AC coupling capacitors.

For Tx pairs originating from the processor, and going to the add-in card Rx pairs, the AC coupling capacitors are located on the motherboard.

For newer low profile graphic cards, which require the AC coupling capacitors be placed on the motherboard, the AC coupling capacitors must be placed on the motherboard for Tx pairs originating from the AIC PCI Express device and going to Rx pairs on the motherboard.

#### 8.6.2.2 Desktop Form Factor Connectors

The *PCI Express* Card Electro-Mechanical Specification* defines the connector to use in conjunction with edge finger add-in cards. However, several items worth mentioning with respect to the connector are listed below:

- For through-hole connectors, the pins of a differential pair are offset from each other. This delta of mismatch between the pins should be directly accounted for by the PCB trace on the system board. Refer to the Length Matching section of this chapter for more details on length matching requirements.
- The two traces of a differential pair should both route into a connector pin field from the same layer.
- The connectors and the add-in cards are keyed such that smaller cards can be put in larger connectors. For example, an x1 card can be inserted into the x4, x8, and x16 connectors. This is referred to as up-plugging. No known layout adjustments need to be made in order to accommodate up-plugging.

### 8.6.3 AIO Form Factor Passive Components and Connectors

#### 8.6.3.1 AIO Form Factor AC Coupling Capacitor Placement Guidelines

Adjacent differential pairs on the connector are separated by two ground pins to manage the connector crosstalk. Ground pins should directly tie to the ground plane on the system board.

Each lane of a PCI Express link must be AC coupled between the driver and receiver. The PCIe specification allows for the AC coupling capacitors to be located either on or off the die. However, in most cases the AC coupling is separated from the die and is in the form of discrete capacitors on the motherboard. Use the following guidelines for AC coupling capacitors.

For Tx pairs originating from the processor, and going to the add-in card Rx pairs, the AC coupling capacitors are located on the motherboard.

For newer low profile graphic cards, which require the AC coupling capacitors be placed on the motherboard, the AC coupling capacitors must be placed on the motherboard for Tx pairs originating from the AIC PCI Express device and going to Rx pairs on the motherboard.

**Table 8-6. AIO Form Factor AC Coupling Capacitor Guidelines (Sheet 1 of 2)**

| Parameter | Recommendation |
|---|---|
| Cap size | • 0402 strongly encouraged (1)<br>• C-packs are not allowed (2) |
| Cap Value (3) | • 180 nF min<br>• 265 nF max<br>• Recommend using a nominal Cap Value of 220 nF<br>• Cap values **must** be the same for each signal in a differential pair<br>• Cap values do not need to be matched among different differential pairs. |

**Table 8-6. AIO Form Factor AC Coupling Capacitor Guidelines (Sheet 2 of 2)**

| Parameter | Recommendation |
|---|---|
| Cap Placement — within a pair | • Place caps at the same linear location along the signals of a given differential-pair.<br>• The breakout into and out of the capacitors should be symmetrical for both signal lines in a differential-pair.(5)<br>• For each differential pair, place the capacitors as close to each other as possible per DFM rules. |
| Cap Separation – within a pair | • Place the capacitors as close to each other as possible per DFM rules for size 0402 caps. |
| Cap Placement - pair-to-pair | • No requirements to length match the routing from the processor to AC coupling caps among the differential pairs. |

***Notes:***

1. While the size 0603 capacitors are acceptable, size 0402 capacitors are strongly encouraged since the smaller package size reduces the series inductance and smaller package size reduces the overall board area needed to place the capacitors. Customers are encouraged to use smaller package size if available for example 0201.
2. C-packs are not recommended for PCI Express AC coupling capacitor. VNA measurements have shown that the loss across the channel due to crosstalk is significant and causes a severe decrease in margin. Also, layout studies show only a small decrease in board area for the placement of the 0504, x2, C-packs compared with 0402 discrete capacitors (less than 10%.).
3. Capacitance value tolerance is not applicable as long as specified min/max range is met when the tolerance is taken into account.
4. Routing studies have shown that the AC coupling capacitors can be place in less than 0.3-square inch (194-square mm). This placement strategy completely utilizes the routing channels in between processor and the graphics controller.
5. The breakout into and out of the capacitors should be symmetrical for both signal lines in a differential-pair. Minimize this trace route to maximize the amount of coupling between the signals within the pair; this helps minimize the common mode noise introduced.

### 8.6.3.2 AIO Form Factor Connectors

Adjacent differential pairs on the connector are separated by ground pins to manage the connector crosstalk. Ground pins should directly tie to the ground plane on the system board.

The topologies in this section assume that AC-caps are placed on the platform for both Rx and Tx lanes. Such topologies are commonly required when using low-profile, horizontally mounted (with surface mounted connectors) Add-in cards, which require AC-caps to be placed on the platform.

## 8.6.4 Passive Components

**Table 8-7. AC Coupling Capacitor Guidelines (Sheet 1 of 2)**

| Parameter (For AC Coupling Capacitors) | Requirement |
|---|---|
| Cap size | • 0402<br>• C-packs are **not** allowed |
| Cap Value | • 180 nF min<br>• 265 nF max<br>• Cap values must be the same for each signal in a differential pair<br>• Recommend using a nominal Cap Value of 220 nF |
| Cap Value Tolerance | • Not applicable as long as specified min/max range is met when the tolerance is considered. |

### Table 8-7. AC Coupling Capacitor Guidelines (Sheet 2 of 2)

| Parameter (For AC Coupling Capacitors) | Requirement |
|---|---|
| Cap Placement—Coupled Pair | • Must be placed at same exact location within the two signal lines<br>• Symmetric routing into the caps and matched line lengths on either side of the caps for each line of the diff pair. |
| Cap Location—Chip to Connector Routing | • Capacitors should be generally placed within 450 mils of the connector no matter what the configuration is i.e. (x16, x8, x4, x2, x1) or form factor. |

Each lane of a PCI Express link must be AC coupled between the driver and receiver. The PCIe specification allows for the AC coupling capacitors to be located either on or off the die. However, in most cases the AC coupling is separated from the die and is in the form of discrete capacitors on the motherboard. Use the following guidelines for AC coupling capacitors.

### Table 8-8. AC Coupling Capacitor Guidelines

| Description | Recommendation |
|---|---|
| Intra pair Placement Mismatch | Max = 5 mil |
| Intra pair Cap Separation | DFM minimum for size 0402 capacitors |
| Pair-to-Pair Cap Matching | Not required |

***Notes:***
1. Locate capacitors at the same linear location along the signals of a given differential-pair.
2. No more than a 5-mil (0.127-mm) delta should exist between the differential signals on the trace segments on either side of the AC coupling capacitor.
3. There is no requirement to length match the routing from processor to the AC coupling capacitors between the differential-pairs.
4. Place the capacitors as close to each other as possible per DFM rules for each differential pair.
5. While the size 0603 capacitors are acceptable, size 0402 capacitors are strongly encouraged since the smaller package size reduces the series inductance and smaller package size reduces the overall board area needed to place the capacitors.Customers are encouraged to use smaller package size if available for example 0201.
6. Pad sizes for each of the capacitors should be the minimum allowed per DFM to minimize parasitics.
7. The same capacitor package size should be used for each signal in a differential-pair.
8. C-packs are not recommended for PCI Express AC coupling capacitor. VNA measurements have shown that the loss across the channel due to crosstalk is significant and causes a severe decrease in margin. Also, layout studies show only a small decrease in board area for the placement of the 0504, x2, C-packs compared with 0402 discrete capacitors (less than 10%).
9. The breakout into and out of the capacitors should be symmetrical for both signal lines in a differential-pair. Minimize this trace route to maximize the amount of coupling between the signals within the pair; this helps minimize the common mode noise introduced.
10. Routing studies have shown that the AC coupling capacitors can be place in less than 0.3-square inch (194-square mm). This placement strategy completely utilizes the routing channels in between processor and the graphics controller.

## 8.7 Compensation Guidelines

The signal PEG_RCOMP should be connected to the VCCIO via a single 24.9 Ω ±1% resistor. Refer to the figure below for details on routing.

**Figure 8-8. Processor PCI Express Compensation Signal Routing Topology**

**Table 8-9. Processor PCI Express* Compensation Signal Routing Guidelines**

| Parameter | Segment | Units | Min Trace Width | Trace Spacing to Other Signals | Max Routing Length | Resistance |
|---|---|---|---|---|---|---|
| PEG_RCOMP [1] | L1 | mils | 5 | 15 | 600 | NA |
| Resistor | R1 | Ω | NA | NA | NA | 24.9 ± 1% |
| ***Note:*** Must maintain low DC resistance routing (<0.1 Ω) | | | | | | |

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# 9 Direct Media Interface Design Guidelines

## 9.1 Introduction

Direct Media Interface (DMI) connects the Coffee Lake Processor and PCH components via a high-bandwidth bus and maintains a low pin count.

### 9.1.1 Compliance Specification

| Title | Location |
|---|---|
| *PCI Express Base Specification* | *http://www.pci.org* |

## 9.2 Signal Descriptions

**Table 9-1. DMI Signal Groups**

| Signal Name | Description |
|---|---|
| DMI_TXN[3:0], DMI_TXP[3:0]<br>DMI_RXN[3:0], DMI_RXP[3:0] | DMI Receive/Transmit Differential Pair |
| PEG_RCOMP | Processor DMI compensation Signal |

## 9.3 Topology Guidelines

DMI interface is composed of eight differential signal pairs or four lanes. Trace lengths greatly impact the loss and jitter budgets of the interconnect and the resulting bus margin. Variations in these design rules are possible, but require simulation to ensure compliance is maintained. Avoid routing Legacy signals adjacent to DMI high-speed differential signals.

### 9.3.1 Differential-Pair Width and Spacing

DMI supports MS/SL/DSL. Follow the guidelines in “Printed Circuit Board (PCB) Considerations”.

### 9.3.2 DMI 2-Via Topology

***Note:*** DMI differential trace pairs may be routed on any layer as long as the max total length, max via count, inter-pair length matching design rules are not violated.

***Note:*** The length difference between lanes (longest to shortest lane) within a DMI port should not be bigger than 2"

## Figure 9-1. DMI 2-Via Topology

***Notes:***

1. DSL Routing - No broadside/parallel routing on the adjacent DSL.
2. The number of vias in use may be less than the number of vias specified in the topology.However, routing layer guideline (MS/SL/DSL) must be met.
3. Coffee Lake H PTPS - uses 12 mils PTPS for main route sections.
4. Coffee Lake H supports board Type 3 only.
5. Non Interleave route is recommended for Xtalk reduction.
6. For SL Breakout implementation please place the first via to the left of Breakout (BO) segment. Via BO is allowed to appear inside the BO main route but total length must meet PDG requirements.
7. DMI differential trace pairs may be routed on any layer as long as the maximum total length, maximum via count and inter-pair length matching design rules are not violated.
8. Maximum number of Via supported is 2, if 3rd via is absolutely necessary, in order to reduce the risk, the via near PCH must be without stub (between top and bottom, from uS to uS).
9. Length Matching between P and N within a differential pair is ±10 mils

## Table 9-2. DMI 2-Via Topology Routing Guidelines (Sheet 1 of 2)

| Description | Parameter | Stackup | | Routing Topology | | Units |
|---|---|---|---|---|---|---|
| | | Coffee Lake S DT Tower | Coffee Lake S DT AIO | Coffee Lake S DT Tower | Coffee Lake S DT AIO | |
| Data Rate | N/A | N/A | N/A | 8 | 8 | Gbps |
| CFL Processor Breakout | BO | MS | MS/SL/DSL | 300 | 300 | mils |
| Main Route Segment Max | M1 | MS | MS/SL/DSL | 1500 | 1500 | mils |
| Main Route Segment Max | M2 | MS | MS/SL/DSL | 7000 | 7000 | mils |
| Route on MB (Mux left) | BI | MS | MS | 300 | 300 | mils |
| Total Route Length Min-Max[3, 4] | Sum BO to BI | per segment | per segment | 1000-7000 | 1000-7000 | mils |

**Table 9-2. DMI 2-Via Topology Routing Guidelines (Sheet 2 of 2)**

| Description | Parameter | Stackup | | Routing Topology | | Units |
|---|---|---|---|---|---|---|
| | | Coffee Lake S DT Tower | Coffee Lake S DT AIO | Coffee Lake S DT Tower | Coffee Lake S DT AIO | |
| Notes:<br>1. Differential-Pair length matching should be maintained segment-to-segment.<br>2. Non - Interleaved routing is recommended.<br>3. Total Length Min-Max limit requirements should not be violated. | | | | | | |

# 9.4 Configuration

## 9.4.1 Lane Reversal and Polarity Inversion Support

Lane Reversal is only supported in PCH DMI Link. OEM can enable this feature in PCH to ease the DMI Link routing (between CPU and PCH) on the board. PCH DMI Lane Reversal is enabled or disabled through SoftStrap.

Polarity inversion is supported on all the Receiver Lanes in PCH DM. PCH DMI will autonomously detects the polarity inversion (Rxp and Rxn is connected reversed) based on the Training Sequence received and enabled it during Link Training.

***Note:*** For more information refer Processor and PCH EDS Vol.1

**Figure 9-2. DMI Lane Reversal Example**

***Notes:***
1. DMI Lane reversal is supported only on CNP PCH-H and not on the Processor.
2. L[7:0] - Processor and PCH DMI Controller Logical Lane Numbers.
3. P[7:0] - Processor and PCH DMI Package Pin Lane Numbers.

## 9.5 Compensation Guidelines

Resistance Compensation for DMI is same for PEG. Refer to PEG chapter for the guidelines.

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# 10 Hybrid Graphics

## 10.1 Introduction

Microsoft* Hybrid Graphics definition includes the following:

- The system contains a single integrated GPU and a single discrete GPU.
- It is a design assumption that the discrete GPU has a significantly higher performance than the integrated GPU.
- Both GPUs shall be physically enclosed as part of the system.
  - MS Hybrid DOES NOT support hot-plugging of GPUs
  - OEMS should seek further guidance from MS before designing systems with the concept of hot-plugging
- Starting with Th1 (WDDM 2.0), a previous restriction that the discrete GPU is a render-only device, with no displays connected to it, has been removed. A render-only configuration with NO outputs is still allowed, just NOT required.

  It must be noted that systems that have outputs available off of the discrete GPU will NOT support previous versions of the OS (Windows 8.1 and Older).

Microsoft Windows 10 operating system enables the Win10 Hybrid graphics framework wherein the GPUs and their drivers can be simultaneously utilized to provide users with the benefits of both performance capability of discrete GPU (dGPU) and low-power display capability of the processor GPU (iGPU). For instance, when there is a high-end 3D gaming workload in progress, the dGPU will process and render the game frames using its graphics performance, while iGPU continues to perform the display operations by compositing the frames rendered by dGPU.

Each vendor [Intel as the vendor of integrated GPU / 3rd Party Graphics Vendor / Microsoft] is responsible for their own component, and Microsoft owns the overall implementation including all Hybrid Graphics related documentation and guidance.

Hybrid Graphics has requirements which determine support on different platforms and these requirements may be different between versions of OS. See Microsoft documentation for detailed requirements per OS version.

The iGPU device is configured as the primary display adapter driving the embedded or local flat panel of the device. If dGPU is designated to drive the internal display, it gets configured as primary display adapter. In this scenario, and when there is no external display driven by iGPU, the system ceases to qualify as a hybrid graphics, and it rather behaves like any discrete graphics system where the capabilities of iGPU is not utilized.

Having a system configured where both iGPU and dGPU are driving displays needs to be carefully evaluated especially if there is difference in display capabilities of the two graphics adapters that would lead to user confusion or bad UX.

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# 11 Thunderbolt™ Design Guidelines

Thunderbolt™ technology (TBT) is a transformational high-speed, dual protocol I/O, and it provides flexibility and simplicity by encapsulating both data (PCIe*) and video (DisplayPort*) on a single cable connection that can daisy-chain up to six devices.

Alpine/Titan Ridge are Thunderbolt controllers that acts as a point of entry or a point of exit in the Thunderbolt domain. The Thunderbolt domain is built as a daisy chain of Thunderbolt enabled products for the encapsulated protocols - PCIe and DisplayPort. These protocols are encapsulated into the Thunderbolt fabric and can be tunneled across the Thunderbolt domain. Alpine/Titan Ridge Thunderbolt controller also acts as a flexible re-driver for DP protocol and a source for xHCI controller.

Alpine/Titan Ridge can be implemented in various systems such as PCs, laptops and tablets, or devices such as storage, docks, displays, home entertainment, cameras, computer peripherals, high end video editing systems, and any other PCIe based device that can be used to extend system capabilities outside of the system's box.

Alpine/Titan Ridge Thunderbolt connection data rate is 20Gbps per lane and is compatible with Thunderbolt 3 specification enabling a Thunderbolt link at up to 2x20Gbps, as well as backward compatible with Thunderbolt 1 (10Gbps) and Thunderbolt 2 (2x10Gbps) specifications.

Alpine/Titan Ridge port connectivity is through USB Type-C connector supporting the following modes:

| Connection Type | Mode | USB-C Port Details |
|---|---|---|
| USB | Native | Single SSP/SS + Single HS/FS/LS USB connection |
| Thunderbolt | Alternate | Dual Thunderbolt lanes running at 10Gpbs/20Gbps |
| Display Port | Alternate | x1/x2/x4 Display Port running at 1.62Gbps/2.7Gbps/5.4Gbps/ 8.1Gbps[1] signaling rate |
| Multi Function Mode | Alternate | Single SSP/SS + Single HS/FS/LS USB connection + x2 Display Port running at 1.62Gbps/2.7Gbps/5.4Gbps/8.1Gbps[1] signaling rate |
| **Note**: 1. 8.1Gbps is only supported on Titan Ridge | | |

**Table 11-1. Acronyms**

| Acronyms | Description |
|---|---|
| TBT | Thunderbolt™ Technology |
| SSP | Super Speed Plus |
| SP | Super Speed |
| AR | Alpine Ridge |
| TR | Titan Ridge |

## 11.1 Supported Thunderbolt™ Configuration Options

### Table 11-2. Supported Thunderbolt™ Configuration - Inputs

| Thunderbolt Connector Number | PCIe* Configuration | DisplayPort* Sink |
|---|---|---|
| 1 USB Type-C Connector | x2 or x4(recommend) | 1 x4 or 2 x4 (recommend) |
| 2 USB Type-C Connectors | x4 | 2 x4 |

### Table 11-3. Supported Thunderbolt™ Configuration - Outputs (Sheet 1 of 2)

| Thunderbolt Controller | Thunderbolt Link Connection | Side Port Connection |
|---|---|---|
| Alpine Ridge DP | 2 high speed ports can be configured as:<br>• Two USB Type-C connectors:<br>— Thunderbolt (40G)<br>— or Native DP1.2<br>— or Native USB 3.1<br>• One USB Type-C connector (as described) and One of the high speed ports can be configured as DP only:<br>— could be mDP or DP<br>• One USB Type-C connector (as described) and One of the high speed ports can be configured as USB Type-A connector:<br>— Native USB3.1 | • 1 Display connector:<br>— HDMI connector - Native HDMI1.4<br>— or DP connector - Native DP1.2 |
| Alpine Ridge SP | 1 high speed port can be configured as:<br>• One USB Type-C connectors:<br>— Thunderbolt (40G)<br>— or Native DP1.2<br>— or Native USB 3.1<br>• One USB Type-A connector:<br>— Native USB3.1 | • 1 Display connector:<br>— HDMI connector - Native HDMI1.4<br>— or DP connector - Native DP1.2 |
| Alpine Ridge LP | 1 high speed port can be configured as:<br>• One USB Type-C connectors:<br>— Thunderbolt (40G)<br>— or Native DP<br>— or Native USB 3.1<br>• One USB Type-A connector:<br>— Native USB3.1 | • No side port supported |
| Titan Ridge DP | 2 high speed ports can be configured as:<br>• Two USB Type-C connectors:<br>— Thunderbolt (40G)<br>— or Native DP1.4[1]<br>— or Native USB 3.1<br>• One USB Type-C connector (as described) and One of the high speed ports can be configured as DP only:<br>— could be mDP or DP<br>• One USB Type-C connector (as described) and One of the high speed ports can be configured as USB Type-A connector:<br>— Native USB3.1 | • 1 Display connector:<br>— DP connector - Native DP1.4[1] |
| Titan Ridge SP | 1 high speed port can be configured as:<br>• One USB Type-C connectors:<br>— Thunderbolt (40G)<br>— or Native DP1.4[1]<br>— or Native USB 3.1<br>• One USB Type-A connector:<br>— Native USB3.1 | • 1 Display connector:<br>— DP connector - Native DP1.4[1] |



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**Table 11-3. Supported Thunderbolt™ Configuration - Outputs (Sheet 2 of 2)**

| Thunderbolt Controller | Thunderbolt Link Connection | Side Port Connection |
|---|---|---|
| **Note**: 1. DP1.4 support will depend on GPU capability | | |

# 11.2 Thunderbolt™ Port Power Requirements

## 11.2.1 Host Source Requirements

Single Port Hosts are required to minimally support 3A/5V on VBUS in Thunderbolt Mode.

Hosts with more than one port are required to provide power per Table 11-4. All Thunderbolt ports shall be capable of providing Full VBUS power on a first-come, first-served basis up to the minimum number of required ports. Tablet PCs with screen sizes less that 13.x" shall provide a minimum of 4.5W on all Thunderbolt ports.

Thunderbolt Hosts shall provide 1.5W to the VCONN pin on all Thunderbolt ports. The VCONN voltage is required to be between 4.75V and 5.5V per USB Type-C r1.0. Note that 1.5W power from VCONN is higher than the 1.0W required by USB Type-C r1.0.

All Ports shall use the termination defined in Table 4-10 in USB Type-C r1.0 to broadcast their available Source current. The DFP/Source shall modify its termination to reflect any changes in Source current availability. Thunderbolt Ports shall use the 3.0A/5V pull-up.

Hosts must be DRPs to be able to support peer-to-peer communication.

**Table 11-4. VBUS Power Provisioning with Number of Thunderbolt™ Ports**

| Power Standard | Voltage/Current | Port 1 | Port 2 | Port 3 | Port 4 |
|---|---|---|---|---|---|
| First Port VBUS Power | 5V/3A | 1 | 1 | 2 | 2 |
| Second Port VBUS Power | 5V/900mA | NA | 1 | 1 | 2 |
| VCONN Power | 1.5W TBT | 1 | 2 | 3 | 4 |

# 11.3 Power Delivery

Refer to **USB PD r2.0** power compliance document for the compliance measurements. The document can be downloaded from http://www.usb.org.

## 11.3.1 Thunderbolt™ Power Provider VBUS Electrical Requirements

The VBUS Source Electrical Parameters are specified in Table 7-22 and Table 7-24 of the USB PD r2.0 Specification. The VCONN Source requirements are specified in Table 4-2 and Table 4-3 of the USB Type-C r1.0 Specification. The only specifications defined here are those which differ from or are in addition to the USB PD r2.0 and the USB Type-C r1.0 Specifications. This specification assumes compliance with USB Type-C r1.0 specification with additional conditions specifically required for Thunderbolt.

Thunderbolt Power Providers must supply 5V and shall use the Fixed Voltage PDO. The current has been chosen to yield 10.5W worst-case for a bus powered device after the switching regulator assuming 88% efficiency at 5V. The requirements for Power Provides is shown in table below.

Optional VBUS sources can provide 9V, 15V and 20V following the USB PD r2.0 Specification.

USB Type-C and USB PD specification can be downloaded from http://www.usb.org.

**Table 11-5. Thunderbolt™ VBUS Source Electrical Parameters**

| Parameter | Description | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| VSrc_BPD5[1] | Minimum voltage provided to port in Active when connected to a BPD | 4.75 | 5 | 5.5 | V | 3A min current |
| ***Note:*** 1. Thunderbolt Specific Requirement | | | | | | |

## 11.3.2 Thunderbolt™ VCONN Source Electrical Requirements

The Thunderbolt Power Provider VCONN Electrical Parameters are specified in table below.

**Table 11-6. Thunderbolt VCONN Source Electrical Requirements**

| Parameter | Description | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| VSrc_Susp | Minimum voltage provided to port in suspend | 4.75 | 5 | 5.5 | V | 7.5mA min |
| VSrc_Active | Minimum power provided to port in Active | 4.75 | 5 | 5.5 | V | 1.5W min |

## 11.3.3 Thunderbolt™ BIOS

Thunderbolt™ introduces multilevel PCIe* trees with multiple bridges and endpoint devices. Windows* 10 RedStone2 and the versions before do not have fully built-in support for Thunderbolt™. Thunderbolt™ uses the native PCIe* driver in the OS, and supports hot plug/unplug via the BIOS.

For Windows* 10 RedStone3 and later versions, Thunderbolt™ hot plug/unplug are supported by native PCIe* driver.

Thunderbolt™ BIOS includes three main aspect,

**1. Thunderbolt™ Hot Plug/unplug**

Hot plug is a standard PCIe* feature and current Windows* OS only supports simple PCIe topologies. In general case, Thunderbolt™ introduces multilevel PCIe trees with multiples bridge and endpoint device. Current Windows* OS does not have built-in support for Thunderbolt™. In order to prevent PCIe* wrong resource allocation and misconfiguration, Thunderbolt™ BIOS uses ACPI issues software SMI and upon completion Notify (RP01,0) to trigger OS rescan of the underlying PCIe* sub-tree.

**2. Security Levels**

Alpine/Titan Ridge supports different levels of security for device connection and PCIe* tunneling. Table below defines Alpine/Titan Ridge support security level, and default security level is Security Level 1 (SL1).

**Table 11-7. Supported Alpine/Titan Ridge Security Level**

| SL# | Security Level | Description |
|---|---|---|
| SL0 | No Security | Allow legacy Thunderbolt devices auto connect - the connection manager auto connects to a new device plugged in |
| SL1 | User Authorization | Allow User Notification devices - the connection manager requests connection approval from the host SW, auto approval may be given based on the Unique ID of the connecting device |
| SL2 | Secure Connect | Allow One time saved key devices - the connection manager requests connection approval from the host SW, auto approval is only given if the host challenge to the device is acceptable |
| SL3 | DisplayPort only | Allow only DP sinks to be connected (re-driver or DP tunnel, no PCIe* tunneling) - at this mode no tunneling is done for PCIe devices |

### 3. Sx Handling

Tables below lists Alpine/Titan Ridge wake support enabled and disabled configuration. If mobile platform wants to enable wake support on some power state only, BIOS should know the host is at what power state, and then follow WakeEnabled flow or WakeDisabled flow. For System For systems that provide Alpine/Titan Ridge power from two separate rails (VCC3P3_SX from a sustain rail while VCC3P3_S0 from S0 rail) the system must perform a pre-notice Sx entry procedure through the TBT2PCIe mailbox. For the case Alpine/Titan Ridge is not powering the CIO domain the BIOS needs to force Alpine/Titan Ridge power using POC_GPIO_3 to enable the mailbox functionality.

**Table 11-8. Alpine/Titan Ridge S3/S4 Wake Support Enabled**

| | S3/S4 WakeEnabled | S5 |
|---|---|---|
| HW requirement | • Connect SLP_S3# to AR/TR GPIO<br>• Keep AR Power VCC3P3_S0 and VCC3P3_SX power rails similar to S0 | Power off AR |
| Sx Entry | SLP_S3: asserted (high->low) | RESET_N: asserted (high->low) |
| Sx (expected behavior) | CM shutdown “CIO”, “RDV”, “LC” power domains | 0 mW |
| If Batlow# asserted during Sx | Wake feature will be disabled | N/A |
| Sx Exit | • SLP_S3#: deasserted<br>• Wake from TBT device - AR/TR will assert PCIE_WAKE_N until PERST_N is deasserted. PCIE_WAKE_N will not be asserted if AR/TR Host woke up due to SLP_S3# deassertion | Same as TBT power on sequence |

**Table 11-9. Alpine/Titan Ridge S3/S4 Wake Support Disabled**

| | S3/S4 WakeDisabled | S5 |
|---|---|---|
| HW requirement | Power off AR(Vcc3v3) | Power off AR(Vcc3v3) |
| Sx Entry | • RESET_N: asserted (high->low)<br>• Power off AR/TR | • RESET_N: asserted (high->low) |
| Sx (expected behavior) | 0 mW | 0 mW |
| If Batlow# asserted during Sx | N/A | N/A |
| Sx Exit | Check if TBT device is connected or not before Sx Entry<br>— Write PCIE2TBT mailbox | Same as TBT power on sequence |

For detailed Thunderbolt BIOS specification and reference code, refer to “Alpine/Titan Ridge - Thunderbolt BIOS Implementation Guide” and “Alpine/Titan Ridge - Thunderbolt BIOS Additions”.

## 11.3.4 Reference Documents

| Title | Document # |
|---|---|
| Alpine Ridge DP Collateral | 563553 |
| Alpine Ridge SP Collateral | 549740 |
| Alpine Ridge LP Collateral | 560284 |
| Titan Ridge DP Collateral | 567677 |
| Titan Ridge SP Collateral | 573973 |
| Thunderbolt - Alpine Ridge C0 NVM image | 565187 |
| Thunderbolt - Titan Ridge B0 NVM image | 573500 |
| Thunderbolt TenLira Tool | 559533 |
| Imaginarium 2- For Alpine Ridge Thunderbolt products | 559314 |
| Manufacturing Test with Intel® Thunderbolt™ Technology Premium IO Controller Host | 559414 |

## 11.3.5 Compliance Specification

### Table 11-10. Thunderbolt™ Compliance Specification

| Title | Document # |
|---|---|
| Thunderbolt - USB Type-C TBT Specification | 557111 |
| Thunderbolt - Host Electrical Validation Test Specification | 567664 |
| Thunderbolt 3 Based PC Host Functional Compliance Test Specification | 557133 |

## 11.3.6 Thunderbolt™ Signal Descriptions

### Table 11-11. Thunderbolt™ High Speed Interface

| Interface | Description | Bit Rate |
|---|---|---|
| TBT | Thunderbolt™ 20Gbps channel | 20.625 Gb/s |
| USB3.1 | USB3.1 10Gbps channel | 10 Gb/s |
| PCIe* Gen3 | Used for PCIe root complex connection | 8 GT/s |
| DisplayPort* 1.2a | Used for DP Sink connection | 5.4 Gb/s |
| DisplayPort* 1.4[1] | Used for DP Sink connection | 8.1 Gb/s |
| USB* 2 | Used for USB 2.0connection | 480 Mb/s |
| **Note**: 1. 8.1Gbps is only supported on Titan Ridge | | |



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### 11.3.6.1 Thunderbolt™ Controller Signal Groups

**Table 11-12. Alpine/Titan Ridge High Speed Signals**

| Group | Signal Name | Description |
|---|---|---|
| TBT Tx | • Alpine Ridge<br>TBTA_HD2CA_0_P, TBTA_HD2CA_0_N<br>TBTA_HD2CA_1_P, TBTA_HD2CA_1_N<br>TBTB_HD2CA_0_P, TBTB_HD2CA_0_N<br>TBTB_HD2CA_1_P, TBTB_HD2CA_1_N | TBT Transmitter Differential Pair |
| | • Titan Ridge<br>TBTA_TX1_P, TBTA_TX1_N<br>TBTA_TX2_P, TBTA_TX2_N<br>TBTB_TX1_P, TBTB_TX1_N<br>TBTB_TX2_P, TBTB_TX2_N | |
| TBT Rx | • Alpine Ridge<br>TBTA_CA2HD_0_P, TBTA_CA2HD_0_N<br>TBTA_CA2HD_1_P, TBTA_CA2HD_1_N<br>TBTB_CA2HD_0_P, TBTB_CA2HD_0_N<br>TBTB_CA2HD_1_P, TBTB_CA2HD_1_N | TBT Receiver Differential Pair |
| | • Titan Ridge<br>TBTA_RX1_P, TBTA_RX1_N<br>TBTA_RX2_P, TBTA_RX2_N<br>TBTB_RX1_P, TBTB_RX1_N<br>TBTB_RX2_P, TBTB_RX2_N | |
| PCIe* Tx | PCIE_TX[3:0]_P, PCIE_TX[3:0]_N | PCIe* Transmitter Differential Pair |
| PCIe* Rx | PCIE_RX[3:0]_P, PCIE_RX[3:0]_N | PCIe Receiver Differential Pair |
| DP Sink | DPSNK0_ML[3:0]_N, DPSNK0_ML[3:0]_P, DPSNK1_ML[3:0]_N, DPSNK1_ML[3:0]_P | DP Sink Main Link Receiver Differential Pair |
| USB 2 | PA_USB2_D_N, PA_USB2_D_P. PB_USB2_D_N, PB_USB2_D_P. | USB 2.0 Differential Pair |

## 11.4 Thunderbolt™ Topology Guidelines

### 11.4.1 Motherboard Down Topology

Thunderbolt™ I/O is a virtual wire from PC point of view that tunnels PCIe* and DisplayPort* stream. Considering PCIe*/DisplayPort* connection and few GPIOs for BIOS implementation, Thunderbolt controller onboard design is highly recommended. External DisplayPort* cable and GPIO cable may cause bad user experience, for example, no video or no Hot Plug support.

## 11.4.2 DisplayPort* to Thunderbolt™ Topology

**Figure 11-1. CFL DisplayPort Main link Direct Motherboard Topology for TBT**

**Table 11-13. CFL DisplayPort to TBT Main Link Routing Guideline**

**Figure 11-2. CFL DisplayPort for TBT Aux link Direct topology**

***Note:***
1. No need Pull UP and Pull Down resistors

**Table 11-14. CFL DisplayPort to TBT AUX Link Routing Guidelines**

| Segment | Stack-up | Via Count | Max Length [mils] |
|---|---|---|---|
| B0 | MS/SL | No explicit limit, use best known routing practices | 700 |
| M1 | MS/SL/DSL | | 7000 |
| CN | MS/SL/DSL | | 7000 |
| **Total Length** | | | **13000** |

## 11.4.3 Add-In Card Topology

**Table 11-15. Thunderbolt™-ready Motherboard Requirement (Sheet 1 of 2)**

| | |
|---|---|
| PCIe* Slot | PCIe x4 or wider slot from the PCH<br>• Recommend 4 PCIe lanes are routed to the PCIe slot<br>• If only 2 PCIe lanes are routed to the PCIe slot the board must state support for only 10Gbps of data, this must be shown on the compatible motherboard list |
| Pre-loaded BIOS | Refer to Thunderbolt BIOS implementation |

**Table 11-15. Thunderbolt™-ready Motherboard Requirement (Sheet 2 of 2)**

| | |
|---|---|
| GPIO Header | • Pin1: Force Power - Output pin from PCH/EC/SIO GPIO for security level and debug purpose<br>• Pin2: No Connect<br>• Pin3: CIO Plug Event - Input pin from PCH GPIO which support SMI/SCI event for hot-plug and surprising removal<br>• Pin4: I2C_MASTER_DATA<br>• Pin5: SLP_S3# - SLP_S3# from PCH for S3 control<br>• Pin6: I2C_MATSTER_CLK<br>• Pin7: SLP_S5_S4# - SLP_S5# from PCH for S4/S5 control<br>• Pin8: PA_PPS_INT#<br>• Pin9: GND<br>• Pin10: GND |
| DP output | • For Z, H and Q chipset boards a standard DP out connector (from processor graphics) must be available on the board<br>• For X chipset boards the DP must come from the graphics add-in card |

### 11.4.4 Thunderbolt™ Connector Guideline

Refer to USB Type-C specification. The document can be downloaded from http://www.usb.org.

## 11.5 Thunderbolt™ Length Matching Guidelines

**Figure 11-3. Thunderbolt™ Host Reference Design Block Diagram**

| Group | Segment | Max Length | | Differential Impedance | Length Matching within Diff Pair |
|---|---|---|---|---|---|
| | | mm (max) | mils (max) | | |
| TBT Tx | • Alpine Ridge<br>TBTA_HD2CA_0_P,<br>TBTA_HD2CA_0_N<br>TBTA_HD2CA_1_P,<br>TBTA_HD2CA_1_N<br>TBTB_HD2CA_0_P,<br>TBTB_HD2CA_0_N<br>TBTB_HD2CA_1_P,<br>TBTB_HD2CA_1_N | 50.8 | 2000 | 90 Ohm ± 5% | N/A |
| | • Titan Ridge<br>TBTA_TX1_P,<br>TBTA_TX1_N,<br>TBTA_TX2_P,<br>TBTA_TX2_N,<br>TBTB_TX1_P,<br>TBTB_TX1_N,<br>TBTB_TX2_P,<br>TBTB_TX2_N, | | | 85 Ohm ± 10% | |
| TBT Rx | • Alpine Ridge<br>TBTA_CA2HD_0_P,<br>TBTA_CA2HD_0_N<br>TBTA_CA2HD_1_P,<br>TBTA_CA2HD_1_N<br>TBTB_CA2HD_0_P,<br>TBTB_CA2HD_0_N<br>TBTB_CA2HD_1_P,<br>TBTB_CA2HD_1_N | 50.8 | 2000 | 90 ohm ± 5% | N/A |
| | • Titan Ridge<br>TBTA_RX1_P,<br>TBTA_RX1_N,<br>TBTA_RX2_P,<br>TBTA_RX2_N,<br>TBTB_RX1_P,<br>TBTB_RX1_N,<br>TBTB_RX2_P,<br>TBTB_RX2_N, | | | 85 Ohm ± 10% | |
| PCIe* | PCIE_TX[3:0]_P,<br>PCIE_TX[3:0]_N<br>PCIE_RX[3:0]_P,<br>PCIE_RX[3:0]_N | For matching methodology, refer to Chapter 16, "PCH PCI Express* Interface Design Guidelines" and Chapter 3, "General Differential Design Guidelines" | | | |
| DisplayPort* | DPSNK0_ML[3:0]_N,<br>DPSNK0_ML[3:0]_P,<br>DPSNK1_ML[3:0]_N,<br>DPSNK1_ML[3:0]_P | For matching methodology, refer to Chapter 5, "DisplayPort* Design Guidelines" and Chapter 3, "General Differential Design Guidelines". | | | |

# 11.6 Thunderbolt™ Stack-up Guidelines

## 11.6.1 Stack-up and Layer Utilization Guidelines

**Table 11-16. Thunderbolt™ Layer Utilization**

| Group | Max Number of Vias Allowed | Routing Layer | Pair-to-Pair Spacing | Pair to other (via, trace, component) spacing |
|---|---|---|---|---|
| TBT Tx | 2 (See Note1) | Top Layer | >3h mil | >3h mil |
| TBT Rx | 2 (See Note1) | Bottom Layer | >3h mil | >3h mil |

***Note:***
1. For mid-mount USB-C connector, PA_TX0, PB_TX0, PA_RX1, PB_RX1 connect to USB-C without Vias, PA_TX1, PB_TX1, PA_RX0, PB_RX0 connect to USB-C with 2 PTH Vias

## 11.6.2 Thunderbolt™ Insertion Loss Spec

| Thunderbolt Link Frequency | Insertion Loss Budget on PCB | Reserved Budget for AR Package and Receptacle | Total Insertion Loss Budget |
|---|---|---|---|
| @5.15625Ghz (10.3125Gbps) | 2dB | 1.5dB | 3.5dB |
| @10.3125Ghz (20.625Gbps) | 4dB | 3.5dB | 7.5dB |

# 11.7 Thunderbolt™ Optimization Guidelines

## 11.7.1 TBT Lane Routing and Component Placement

Refer to “Alpine Ridge Host DP - Layout Guideline” for detailed layout recommendation. Doc. ID: 563553.

## 11.7.2 Via Placement and Via Pad Optimization

TBT lane differential routing makes layer transition, the “Top2Bottom Via” unused via pads and Thunderbolt connector DIP pin pads in the middle layers should be removed. Use the smallest possible Vias on board to optimize the impedance for the CIO interface.

# 11.8 Thunderbolt™ Debug Guidelines

## 11.8.1 PCIe* and DisplayPort* Configuration

For supported PCIe* configuration options, refer to Chapter 15, “PCH PCI Express* interface Design Guidelines”. It is recommended to use any tools and utility to check PCIe link width between Alpine/Titan Ridge and Coffee Lake processor.

For DisplayPort* configuration, refer to Chapter 5, “DisplayPort* Design Guidelines”. VBIOS and 3 independent display configurations are also needed to be taken into consideration.

### 11.8.2 NVM Configuration

Alpine/Titan Ridge support lane reversal mode such that the polarity traces (P/N) of a CIO/DP lane differential pair can be swapped (to N/P) for ease of routing. System developers must modify Alpine/Titan Ridge NVM setting (interface, offset, and value) to match the P/N configuration as used in actual lane trace routing. Refer to "Thunderbolt – Alpine/Titan Ridge NVM Image" for the latest release note about the offset/value setting for specific CIO/DP lanes. Each revision might have different instructions on how to control board-dependent channels lanes N/P swap configuration.

## 11.9 Thunderbolt™ Additional Guidelines

### 11.9.1 Crystal Design Requirement

Refer to 5.4.2 of "Alpine/Titan Ridge datasheet" for detailed XTAL/Clock specification. Doc. ID: 563553/567677

### 11.9.2 NVM

Alpine/Titan Ridge use Flash memory for initialization of various internal parameters, enable/disable bits, analog modules configuration, and internal microcontrollers' ucode patches. Refer to chapter 3 of "Alpine/Titan Ridge datasheet" for more detailed Flash memory map.

**Table 11-17. Supported Flash for Alpine/Titan Ridge**

| Manufacturer | Type | Volume (Mbit) | Supply Voltage (V) |
|---|---|---|---|
| AMIC* | A25L080 | 8.0 | 3.0-3.6 |
| Spansion* | S25FL208K | 8.0 | 2.7-3.6 |
| Winbond* | W25Q80JVNIQ | 8.0 (8pin SOIC150 mil) | 2.7-3.6 |
| Macronix* | MX25L8006EM1I | 8.0 (150mil, 8-SOP) | 2.7-3.6 |
| Micron* | M25PE80-VMN6TP | 8.0 (150mil, SO8N) | 2.7-3.6 |
| Micron* | M25PX80-VMN6TP | 8.0 (150mil, SO8N) | 2.7-3.6 |

### 11.9.3 Thunderbolt Native PCIe* Mode

Thunderbolt native PCIe* mode is supported on Windows* 10 RedStone3 and later versions. Enabling native PCIe* mode on TBT provides benefits including the full support of Modern Standby, less platform BIOS development and validation efforts and shorter device enumeration time.

### 11.9.4 Modern Standby and Runtime D3 Support

Thunderbolt controllers support PCIe link states such as L1 sub-states (Titan Ridge only), L2 and link disconnect to enable SoC to enter low CPU C-States and PCH to assert SLP_S0# to control voltage regulators or embedded controllers to turn off power rails to reduce platform power. If the device, or any other PCIe connected device does not support minimum PCIe low power states, SoC and platform low power states will be blocked and power consumption will be higher.

Refer to Coffee Lake Runtime D3 (RTD3) Hardware and Software Recommendations Design Guide for PCIe* RTD3 implementation details. Doc. ID: 569310.

Modern Standby and RTD3 support with Thunderbolt is supported on Windows* 10 RedStone3 and later versions with native PCIe* mode enabled.

### 11.9.5 Hardware Changes to Support TBT PCIe* RTD3

The following changes are needed to support TBT PCIe* RTD3 in hardware. These pins must be connected to dedicated PCH GPIO pins.

1. TBT_PERST_N: Signal must be isolated to allow a device D3(cold) exit to occur without impacting other endpoints, with facilities to drive the required signal timing (e.g. via ACPI and/or Platform Driver).

2. TBT_PCIE_WAKE_N: Use of the WAKE pin for device-initiated wake during D3(cold) without disrupting other devices.

3. RTD3_PWR_EN: Ability to coordinate/sequence power applied to a D3(cold) domain. This pin must be connected to TBT controller directly instead of connecting to an external MOSFET that controls the power of TBT controller.

4. TBT_CLKREQ_N: Connect to dedicated PCH PCIe* Clock Request pin.

***Note:*** These four signals are named as DG_PERST#, DG_PEWAKE#, DG_RTD3_PWR_EN and DG_CLKREQ# in Titan Ridge Reference Design.

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# 12 Clock and Low Speed I/Os

## 12.1 Platform Clock Design Guidelines

### 12.1.1 Platform Clock Interface Details

**Figure 12-1. Clock Integration Distribution Diagram**

**Figure 12-2. PCH XTAL Input Configuration Diagram**

### 12.1.2 Platform Clock Signal Descriptions

**Table 12-1. Platform Clocks and Associated Signal Details and Descriptions**

| Signal Name | Type | SSC Capable | Description |
|---|---|---|---|
| CLKOUT_CPUNSSC_P<br>CLKOUT_CPUNSSC_N | O | No | **Filtered Crystal Reference Clock to CPU:** 24MHz differential, filtered crystal reference clock to the processor |
| CLKOUT_CPUBCLK_P<br>CLKOUT_CPUBCLK_N | O | Yes | **Differential Clock to CPU:** Reference clock to the processor 100-MHz differential core |
| CLKOUT_CPUPCIBCLK_P<br>CLKOUT_CPUPCIBCLK_N | O | Yes | **Differential PCIe* Reference Clock to CPU:** 100-MHz PCIe* 3.0 specification compliant differential PCIe* reference clock to the processor |
| CLKOUT_ITPXDP_P<br>CLKOUT_ITPXDP_N | O | Yes | **Differential ITP Debug Clock:** 100 MHz differential output to processor XDP/ ITP connector on the platform |
| CLKOUT_PCIE_P[15:0]<br>CLKOUT_PCIE_N[15:0] | O | Yes | **PCI Express* Clock Output:** Serial Reference 100 MHz PCIe* 3.0 specification compliant differential output clocks to PCIe* devices |
| CLKOUT_LPC[1:0] | O | No | **Low Pin Count (LPC) Clock Outputs:** Single-Ended 24-MHz output to various single load connectors/devices |
| SRCCLKREQ#[15:0] | I/O | | **Clock Request:** Serial Reference Clock request signals for PCIe* 100 MHz differential clocks |
| XTAL_IN | I | | **Crystal Input:** Input connection for 24MHz crystal to PCH |
| XTAL_OUT | O | | **Crystal Output:** Output connection for 24 MHz crystal to PCH |
| XCLK_BIASREF | I/O | | **Differential Clock Bias Reference:** Used to set BIAS reference for differential clocks |
| CLKIN_XTAL | I | | **XTAL Clock Input:** Single ended integrated CNV (Connectivity) XTAL clock input |
| XTAL_Freq_Select (GPP_J4) | | | **XTAL Frequency Select:** GPP_J4 Pin Strap for XTAL frequency selection. An external pull-up to VCC (1.8V) is required on this strap for 24 MHz XTAL operation |

***Note:***
1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   — SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   — SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

## 12.2 Platform Clock Guidelines

### 12.2.1 ITP_XDP Differential Clock Routing Guidelines

- Differential Clock Signals:
  — CLKOUT_ITPXDP_P/N

### Figure 12-3. ITP_XDP Differential Clock Topology

### Table 12-2. ITP_XDP Differential Clock Routing Guidelines

| Parameter | Segment | Stack-up | Rule |
|---|---|---|---|
| Reference Plane | BO, M1, M2, M3 | MS/SL/DSL | Ground |
| Max Segment Length | BO | MS/SL/DSL | 12.7mm(500mils) |
| | M3 | MS | 25.4mm(1000mils) |
| Total Motherboard Length | BO+M1+M2+M3 | MS/SL/DSL | 101.6mm(4000mils) to 304.8mm(12000mils) |
| Differential Pair Length Matching | Within Same Layer | MS/SL/DSL | ±0.254mm (±10mils) |
| | Total (B0+M1+M2+M3) | MS/SL/DSL | ± 0.381mm (±15mils) |
| Max Transition Via Count | BO | | 1 |
| | M1, M2 | | 2 |
| | M3 | | 1 |

***Notes:***
1. BO = Motherboard Break Out Segment, M = Motherboard Main Segments
2. MS = Micro-Strip, SL = Strip-Line, DSL = Dual Strip-Line
3. Continuous Ground Referencing is required. If needed power plane referencing to +V1p0 is allowed in the Motherboard Break Out (B0) Segment
4. Clock traces are to be routed in a differential configuration with minimum coupling between the P/N differential signals; where the signals within a differential pair must route together for their entire route.
5. Do not place vias between adjacent complementary clock traces and avoid any differential vias. Vias that are placed in one signal of a differential pair must be matched by a via in the complement signal within a differential pair.
6. At least one ground stitching via must be placed within 30mils(0.762mm) from every signal transition via when ever they change signal layers.
7. If this differential clock pair is not being used it must be left as a no connect
8. Refer to details covered in the "Stack-Up and PCB Considerations" chapter for Trace Impedance, Differential Spacing, Group Spacing, and Isolation Spacing requirements

## 12.2.2 CPU Differential Clock Routing Guidelines

- CPU Differential Clock Signals:
  - CLKOUT_CPUNSSC_P/N
  - CLKOUT_CPUPCIBCLK_P/N
  - CLKOUT_CPUBCLK_P/N

**Figure 12-4. CPU Differential Clock Topology**

**Table 12-3. CPU Differential Clock Routing Guidelines**

| Parameter | Segment | Stack-up | Rule |
|---|---|---|---|
| Reference Plane | BO, M1, M2 | MS/SL/DSL | Ground |
| Max Segment Length | BO | MS/SL/DSL | 12.7mm(500mils) |
| | M2 | MS/SL/DSL | 12.7mm(500mils) |
| Total Motherboard Length | BO+M1+M2 | MS/SL/DSL | 101.6mm(4000mils) to 228.6mm(9000mils) |
| Differential Pair Length Matching | Within Same Layer | MS/SL/DSL | ±0.254mm (±10mils) |
| | Total (B0+M1+M2+M3) | MS/SL/DSL | ± 0.381mm (±15mils) |
| Pair to Pair Length Matching | Total (B0+M1+M2+M3) | MS/SL/DSL | ≤ 12.7mm(500mils) |
| Max Transition Via Count | BO | | 1 |
| | M2 | | 1 |

***Notes:***
1. BO = Motherboard Break Out Segment, M = Motherboard Main Segments
2. MS = Micro-Strip, SL = Strip-Line, DSL = Dual Strip-Line
3. Continuous Ground Referencing is required. If needed power plane referencing to +V1p0 is allowed in the Motherboard Break Out (B0) Segment
4. Clock traces are to be routed in a differential configuration with minimum coupling between the P/N differential signals; where the signals within a differential pair must route together for their entire route.
5. Do not place vias between adjacent complementary clock traces and avoid any differential vias. Vias that are placed in one signal of a differential pair must be matched by a via in the complement signal within a differential pair.
6. At least one ground stitching via must be placed within 30mils(0.762mm) from every signal transition via when ever they change signal layers.
7. Pair to Pair Length Matching = Length Matching between all CPU Differential Clock Signals
8. Refer to details covered in the "Stack-Up and PCB Considerations" chapter for Trace Impedance, Differential Spacing, Group Spacing, and Isolation Spacing requirements
9. For the M1/M1' segment it is recommended to route the CPU Differential Clock Signals on inner layers, SL or DSL, GND Referenced with solid GND Floods on both sides (if applicable) to help mitigate any RFI impacts. If Micro-strip routing is used for the M1/M1' segment it is recommended that it be limited, if possible, to a maximum length of 25.4mm (1000mils). For additional details reference the "Electromagnetic Compatibility" chapter.

## 12.2.3 PCIe* Differential Clock Routing Guidelines to Add-in Card

- Serial Reference Differential Clock Signals:
  - CLKOUT_PCIE_P/N[15:0]

**Figure 12-5. PCIe* Differential Clock to Add-in Card Topology**

**Table 12-4. PCIe* Differential Clock to Add-in Card Routing Guidelines**

| Parameter | Segment | Stack-up | Rule |
|---|---|---|---|
| Reference Plane | BO, M1, M2, M3 | MS/SL/DSL | Ground |
| Max Segment Length | BO | MS/SL/DSL | 12.7mm(500mils) |
| | M3 | MS | 25.4mm(1000mils) |
| | M4 | MS | 50.8mm(2000mils) |
| Total Motherboard Length | BO+M1+M2+M3 | MS/SL/DSL | 101.6 mm(4000mils) to 254mm(10000mils) |
| Differential Pair Length Matching | Within Same Layer | MS/SL/DSL | ±0.254mm (±10mils) |
| | Total (B0+M1+M2+M3) | MS/SL/DSL | ± 0.381mm (±15mils) |
| Max Transition Via Count | BO | | 1 |
| | M1, M2 | | 2 |
| | M3 | | 1 |

***Notes:***
1. BO = Motherboard Break Out Segment, M = Motherboard Main Segments
2. MS = Micro-Strip, SL = Strip-Line, DSL = Dual Strip-Line
3. Continuous Ground Referencing is required. If needed power plane referencing to +V1p0 is allowed in the Motherboard Break Out (B0) Segment
4. Clock traces are to be routed in a differential configuration with minimum coupling between the P/N differential signals; where the signals within a differential pair must route together for their entire route.
5. Do not place vias between adjacent complementary clock traces and avoid any differential vias. Vias that are placed in one signal of a differential pair must be matched by a via in the complement signal within a differential pair.
6. At least one ground stitching via must be placed within 30mils(0.762mm) from every signal transition via when ever they change signal layers.
7. Any differential clock pair not being used must be left as no connects
8. Refer to details covered in the "Stack-Up and PCB Considerations" chapter for Trace Impedance, Differential Spacing, Group Spacing, and Isolation Spacing requirements

## 12.2.4 PCIe* Differential Clock to Down Device Routing Guidelines

- Serial Reference Differential Clock Signals:
  - CLKOUT_PCIE_P/N[15:0]

**Figure 12-6. PCIe* Differential Clock to Down Device Topology**

**Table 12-5. PCIe* Differential Clock to Down Device Routing Guidelines**

| Parameter | Segment | Stack-up | Rule |
|---|---|---|---|
| Reference Plane | BO, M1, M2, M3 | MS/SL/DSL | Ground |
| Max Segment Length | BO | MS/SL/DSL | 12.7mm(500mils) |
| | M3 | MS | 25.4mm(1000mils) |
| Total Motherboard Length | BO+M1+M2+M3 | MS/SL/DSL | 101.6 mm(4000mils) to 304.8mm(12000mils) |
| Differential Pair Length Matching | Within Same Layer | MS/SL/DSL | ±0.254mm (±10mils) |
| | Total (B0+M1+M2+M3) | MS/SL/DSL | ± 0.381mm (±15mils) |
| Max Transition Via Count | BO | | 1 |
| | M1, M2 | | 2 |
| | M3 | | 1 |

***Notes:***
1. BO = Motherboard Break Out Segment, M = Motherboard Main Segments
2. MS = Micro-Strip, SL = Strip-Line, DSL = Dual Strip-Line
3. Continuous Ground Referencing is required. If needed power plane referencing to +V1p0 is allowed in the Motherboard Break Out (B0) Segment
4. Clock traces are to be routed in a differential configuration with minimum coupling between the P/N differential signals; where the signals within a differential pair must route together for their entire route.
5. Do not place vias between adjacent complementary clock traces and avoid any differential vias. Vias that are placed in one signal of a differential pair must be matched by a via in the complement signal within a differential pair.
6. At least one ground stitching via must be placed within 30mils(0.762mm) from every signal transition via when ever they change signal layers.
7. Any differential clock pair not being used must be left as no connects
8. Refer to details covered in the "Stack-Up and PCB Considerations" chapter for Trace Impedance, Differential Spacing, Group Spacing, and Isolation Spacing requirements

### 12.2.5 Single-Ended LPC Clock Routing Guidelines

- Single-Ended Clock Signals:
  - CLKOUT_LPC[1:0]

***Note:*** Refer Chapter 29, "Low Pin Count (LPC) Interface Design Guidelines" for the Single-Ended LPC Clock Routing Guidelines

## 12.3 Platform Clock Associated Signal Guidelines

### 12.3.1 SRC Clock Request Routing Guidelines

- Serial Reference Clock Request Signals:
  - SRCCLKREQ#[15:0]

### Figure 12-7. SRC Request Signal Topology

### Table 12-6. SRC Request Signal Routing Guidelines

| Parameter | Segment | Stack-up | Rule |
|---|---|---|---|
| Reference Plane | BO, M1, M2 | MS/SL/DSL | Ground |
| Max Segment Length | BO | MS/SL/DSL | 100mils(2.54mm) |
| | M2 | MS/SL/DSL | 100mils(2.54mm) |
| Total Motherboard Length | PCH-2-Connector (BO+M1+M2) | MS/SL/DSL | 10000mils(254mm) |
| | PCH-2-Device (BO+M1+M2) | MS/SL/DSL | 12000mils(304.8mm) |
| Resistor (R1) | | | 10k Ohm ±10% |
| Max Transition Via Count | | | Refer Note |

***Note:***
1. BO = Motherboard Break Out Segment, M = Motherboard Main Segments
2. MS = Micro-Strip, SL = Strip-Line, DSL = Dual Strip-Line
3. Ground referencing is preferred. However, single ended clocks can be routed referenced to other planes through the use of stitching capacitors to provide decoupling where the signal crosses planes
4. At least one ground stitching via must be placed within 30mils(0.762mm) from every signal transition via when ever they change signal layers.
5. There are no Max Transition Via Count restrictions but it is recommended to minimize the number of via layer transitions on the SRCCLKREQ# signals.
6. The 10k Ohm pull-up must be pulled up on the rail that the corresponding SRCCLKREQ# pin resides in. PCIe* devices that support the clock request protocol and are powered on only in the S0 state should use core well (S0) powered signals that can be mapped to output any PCI Express* clock as appropriate
7. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
8. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs
9. Any un-used SRCCLKRQ# signal must be left as no connects
10. Refer to details covered in the "Stack-Up and PCB Considerations" chapter for Trace Impedance, Differential Spacing, Group Spacing, and Isolation Spacing requirements

## 12.3.2 24 MHz Input Clock Routing Guidelines

- 24 MHz Signals:
  - XTAL_IN
  - XTAL_Out
  - CLKIN_XTAL

***Notes:***

1. All CFL processor based platforms are required to provide a 24 MHz input to the PCH to enable the PCH to generate all of its internal reference clocks and all of the single-ended and differential platform clock outputs. Refer Figure 12-2, "PCH XTAL Input Configuration Diagram" for the 24 MHz input configuration options.
2. It is strongly recommended that customers designing a Platform pay special attention and follow all of the XTAL_IN/XTAL_OUT/CLKIN_XTAL routing guidelines. The crystal, components, and their XTAL_IN/XTAL_OUT/CLKIN_XTAL signals are very sensitive to board noise and care must be taken when routing and placing these components and signals on the motherboard to provide shielding from any noisy signals or power planes near the components and traces. The details covered in this section provide the guidelines needed to ensure the best environment for these components and signals. Any deviation from these guidelines could result in some platform clock instabilities.

#### 12.3.2.1 24 MHz Crystal External Load Capacitor Requirements

The 24 MHz crystal is physically tuned to operate within the specified frequency range and ppm tolerance with a certain expected capacitive load present. The expected external capacitive load to be used (Ce) consists of the crystal capacitive load plus the pin and trace capacitances. The external load capacitors are important to minimize frequency variations from the crystal by compensating for variable PCB factors related to pin and trace capacitance. Care must be exercised in the selection of the external load capacitors to present the expected capacitive load specified for the crystal in use on the platform.

The appropriate capacitor value for the platform may be determined using the following formula:

**$C_e = 2 * [C_L - (C_s + C_i)]$, where:**

- $C_e$ = External Load Capacitor Value = $C_e1$ = $C_e2$
- $C_L$ = Specified Crystal Capacitive Load = 12pF
  - Found in crystal component data sheet
- $C_s$ = Board Trace Capacitance = < 3pF
  - Includes crystal pad capacitance
- $C_i$ = PCH Pin Capacitance = < 2 to 3pF

Due to vendor variation in crystal characteristics, layout variations and PCB trace capacitance differences, the above calculation should be performed for each design to determine the precise value of $\mathbf{C_e}$ that is optimal for the particular platform.

#### 12.3.2.2 24 MHz Crystal Specification Requirements

**Table 12-7. 24 MHz Crystal Specifications (Sheet 1 of 2)**

| Parameter | Values | Units | Max/Min Range |
|---|---|---|---|
| Frequency | 24 | MHz | |
| Frequency Tolerance | ≤ 100 | PPM | |
| Duty Cycle Variation | +/- 5 | % | |
| Operating Temperature | -40 to 85 | °C | |
| Series Resistance | ≤ 30 | Ω | |

### Table 12-7. 24 MHz Crystal Specifications (Sheet 2 of 2)

| Parameter | Values | Units | Max/Min Range |
|---|---|---|---|
| Aging | ±3 | PPM | |

***Note:***
1. Customers should verify that the vendor's published specifications in the component data sheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance as specified in the respective data sheet.
2. Perform conformance testing and EMC (FCC and EN) testing in real systems
3. Independently measure the component's electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.

## 12.3.2.3 PCH-H Platform Crystal XTAL_IN/OUT Routing Guidelines

### Figure 12-8. PCH-H Platform Crystal XTAL_IN/OUT Topology

### Table 12-8. PCH-H Platform Crystal XTAL_IN/OUT Routing Guidelines (Sheet 1 of 2)

| Parameter | Segment | Stack-up | Rule |
|---|---|---|---|
| Reference Plane | BO1, BO2, M | MS/SL/DSL | Ground |
| Signal Placement | BO1, BO2, M | SL/DSL | • The XTAL_IN/OUT signals **must** be routed on inner layers (SL or DSL) where they **must** be ground referenced with solid ground floods on both sides<br>— If needed the BO1+BO2 segment may be routed on the same single micro-strip layer as the XTAL component |
| Single Ended Trace Impedance | BO1, BO2, M | MS/SL/DSL | 50 Ohms |
| Min Group Spacing | BO1, BO2 | MS/SL/DSL | Signal to Via Void = 5 mils<br>Signal to Signal = 8 mils |
| | M | MS/SL/DSL | Signal to Via Void = 15 mils<br>Signal to Signal = 15 mils |

**Table 12-8. PCH-H Platform Crystal XTAL_IN/OUT Routing Guidelines (Sheet 2 of 2)**

| Parameter | Segment | Stack-up | Rule |
|---|---|---|---|
| Min Isolation Spacing | BO1 (If Needed) | MS/SL/DSL | • XTAL_IN/OUT to non-HSIO Via Void = 8 mils<br>• XTAL_IN/OUT to non-HSIO Signal = 8 mils<br>• XTAL_IN/OUT to HSIO Via Void = 20 mils<br>• XTAL_IN/OUT to HSIO Signal = 20 mils for a max length of 30 mils<br>— Optimized spacing value = 30 mils min |
| | BO2 | MS/SL/DSL | • XTAL_IN/OUT to non-HSIO Via Void = 8 mils<br>• XTAL_IN/OUT to non-HSIO Signal = 8 mils<br>• XTAL_IN/OUT to HSIO Via Void = 50 mils<br>• XTAL_IN/OUT to HSIO Signal = 50 mils for a max length of (100 mils – Break-Out #1 Length) |
| | M | MS/SL/DSL | • XTAL_IN/OUT to non-HSIO Via Void = 20 mils<br>• XTAL_IN/OUT to non-HSIO Signal = 20 mils<br>• XTAL_IN/OUT to HSIO Via Void = 70 mils<br>• XTAL_IN/OUT to HSIO Signal = 70 mils<br>— Optimized spacing value = 100 mils min |
| Max Segment Length | BO1+BO2 | MS/SL/DSL | 100 mils |
| Max Total Length | BO1+BO2+M | MS/SL/DSL | 1000 mils |
| Length Matching | BO1+BO2+M | MS/SL/DSL | ±100 mils |
| Max Transition Via Count | | | 2 |
| External Load Capacitor (Ce1,Ce2) | | | 18pF +/-10% |
| R1 | | | 0 Ohms |
| GND Shield | • 4 mil minimum wide GND shield trace placed evenly between XTAL_IN/OUT to any adjacent VIA Void, power flood, or Signal. If possible this GND shield should also extend around the XTAL crystal components.<br>• GND stitching vias must be placed throughout the GND shield where possible to stitch the GND Shield to ground<br>• Refer GND shield example in Figure 12-10. | | |

***Note:***
1. BO = Motherboard Break Out Segment, M = Motherboard Main Segments
2. MS = Micro-Strip, SL = Strip-Line, DSL = Dual Strip-Line, HSIO = High Speed I/O
3. At least one ground stitching via must be placed within 30mils(0.762mm) from every signal transition via when ever they change signal layers.
4. The oscillator signals are very sensitive to board noise. As a result it is strongly recommended not to route or place any inductive components or high-speed switching signals directly below or above the XTAL_IN/XTAL_OUT signals and the Crystal; including its components (resistors and capacitors).
5. Since these signals are single-ended designers must not route them over or across any voids and they must not route them over any split planes or different reference planes.
6. The documented Ce1/Ce2 external load capacitance value was calculated using the formula in Section 12.3.2.1 and is based off the customer reference design configuration, stack-up, and the crystal characteristics that its using which is defined in the platform design guide. Due to vendor variation in crystal characteristics, layout variations, and PCB trace capacitance differences the formula should be used for each design to determine the value of Ce1/Ce2 that is optimal for the particular platform.
7. If the XTAL_IN or XTAL_OUT signals are routed on inner PCB layers (DSL or SL) they must be ground referenced with solid ground floods on both sides.
8. The crystal input clock can be sensitive to RF power from nearby radios. For more details reference the "Crystal (Xtal) RF Immunity" chapter

## 12.3.3 XCLK_BIASREF Guidelines

- BIAS Reference Signal:

— XCLK_BIASREF

## Figure 12-9. XCLK Bias Reference Topology

## Table 12-9. XCLK Bias Reference Routing Guideline

| Parameter | Segment | Stack-up | Rule |
|---|---|---|---|
| Reference Plane | M1, M2 | MS/SL/DSL | Ground |
| Single Ended Trace Impedance | M1, M2 | MS/SL/DSL | Refer Note |
| Max Total Length | M1+M2 | MS/SL/DSL | 1000mils(25.4mm) |
| Resistor (R1) | | | 60 Ohm ±1.0% |
| Max Transition Via Count | | | 2 |

***Note:***
1. M = Motherboard Main Segments
2. MS = Micro-Strip, SL = Strip-Line, DSL = Dual Strip-Line
3. At least one ground stitching via must be placed within 30mils(0.762mm) from every signal transition via when ever they change signal layers.
4. It is strongly recommended to route the XCLK_BIASREF signal as short as possible where the external series resistor (R1) is placed within 1000 mils from the PCH.
5. No Single Ended Trace Impedance target is identified. Requires low DC resistance routing < 0.5Ω where the max capacitance of the overall net must be <5pf as any extra capacitance can affect pin stability.
6. If desired add a VSS shield, at least 4mil(0.1016mm) wide, between the XCLK signal to any adjacent signal or power flood. If VSS shielding is implemented, then VSS stitching vias must be placed throughout the VSS shield where possible to stitch the VSS Shield to ground. Refer complete details covered in Figure 12-10. Note that the preferred method of isolating the XCLK signals is to follow the Min Isolation Spacing rules.

## Figure 12-10.XCLK Bias Reference VSS Shield Spacing Recommendations

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# 13 Real Time Clock (RTC) Design Guidelines

## 13.1 Real Time Clock (RTC) Design Guidelines

The PCH contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The PCH RTC module requires an external oscillating source 32.768KHz connected on the RTCX1 and RTCX2 balls. Figure below shows the external circuitry that comprises the oscillator of PCH RTC.

The PCH uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to PCH, the RTCX1 signal is amplified to drive internal logic.

**Table 13-1. Reference Specification**

| Title | Location |
|---|---|
| Design Considerations for Platforms Without a Coin Cell Battery - White Paper | RDC#549657 |
| Intel® I/O Controller Hub (Intel® ICH)/ Platform Controller Hub (PCH) Family Real Time Clock (RTC) Electrical, Mechanical, and Thermal Specification (EMTS) - AP-728 | http://www.intel.com/content/www/us/en/chipsets/ich-family-real-time-clock-accuracy-considerations-note.html?wapkw=rtc |

### 13.1.1 RTC Signal Description

| Signals | Description |
|---|---|
| RTCX1 | Crystal Input 1 |
| RTCX2 | Crystal Input 2 |
| SUSCLK | RTC Clock |
| RTCRST# | RTC Reset |
| SRTCRST# | Secured RTC Reset |

### 13.1.2 RTC Topology Guideline

#### 13.1.2.1 VCCRTC External Circuit

On CFL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.46V.

### 13.1.2.2 General RTC Layout Considerations

Since the RTC circuit is very sensitive and requires highly accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Figure and table below provides some general length guidelines for the RTC crystal circuit.

For additional information about RTC Layout Considerations, refer to *Intel® I/O Controller Hub (Intel® ICH)/Platform Controller Hub (PCH) Family Real Time Clock (RTC) Electrical, Mechanical, and Thermal Specification (EMTS) - AP-728* for details layout consideration and fine tuning.

**Figure 13-1. RTC Crystal Input Topology**

**Table 13-2. RTC Routing Guidelines**

| Parameter | Segment / Signal Name | Stack up (MS/SL/DSL) | Units | Recommendation |
|---|---|---|---|---|
| Maximum Length | BO | MS/SL/DSL | mils | 500 |
| Maximum Length | MR | MS/SL/DSL | mils | 500 |
| Maximum Length | BO+MR | MS/SL/DSL | mils | 1000 |
| XTAL_IN and XTAL_OUT length matching maximum | NA | MS/SL/DSL | mils | 50 |
| External Capacitors[7] | C1, C2 | MS | pF | 18+/-10% |
| Resistor | RF | MS | MΩ | 10 |

***Notes:***
7. The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations. Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.

### 13.1.2.3 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while PCH is not powered by the system.

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases.

The battery must be connected to PCH using an isolation Schottky diode circuit. The Schottky diode circuit allows PCH RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. The following figure is an example of a diode circuit that is used.

**Figure 13-2. Schottky Diode Circuit to Connect RTC External Battery**

A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

Using a rechargeable coin battery or a capacitor with a short projected discharged time can increase the risk of:

- an un-provisioned Intel® Active Management Technology (Intel® AMT)
- unusable anti-replay blobs
- Intel® Management Engine (Intel® ME) file system corruption

The first two cases are recoverable: Intel® Active Management Technology (Intel® AMT) can be re-provisioned, and applications using the anti-replay-blobs can be re-enrolled. The third case, the corruption of the Intel® Management Engine (Intel® ME) file system, is irretrievable, but has a very low probability of occurring even when a full discharge occurs.

#### 13.1.2.4 RTC Coin-cell less implementation

Modern implementation of the RTC can also be designed without a coin-cell battery. Details on this implementation is available in the *Design Considerations for Platforms Without a Coin Cell Battery - White Paper*.

### 13.1.3 RTC External RTCRST# Circuit

**Figure 13-3. RTCRST#/SRTCRST# External Circuit for PCH RTC**

The RTCRST# signal is used to reset the RTC well.

***Note:*** RTCRST# should be generated from VBAT with a RC delay of 18–25 ms.

When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

The RTCRST# signal may also be used to detect a low battery voltage. RTCRST# will be asserted during a power up from G3 state if the battery voltage is below 2V. This will set the RTC_PWR_STS bit as described above. If desired, BIOS may request that the user replace the battery.

This RTCRST# circuit is combined with the diode circuit (refer figure above) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. The above figure is an example of this circuitry that is used in conjunction with the external diode circuit.

## 13.1.4 RTC External SRTCRST# Circuit

The SRTCRST# signal is used to reset the RTC registers used for the Intel® Management Engine (Intel® ME) when the on board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18–25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing. Refer to Figure 13-3 external circuit for PCH RTC.

***Notes:***

- RC time delay for SRTCRST# should be the same as RC delay for RTCRST#.
- RTCRST# and SRTCRST# cannot be shorted together.

### 13.1.4.1 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, SRTCRST#, INTRUDER#, PCH_PWROK, DSW_PWROK) must be either pulled up to VccRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in Figure 13-3 meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PCH_PWROK and DSW_PWROK input signal should also be configured with an external weak pull-down.

### 13.1.4.2 RTC Component Selection Guidelines

#### 13.1.4.2.1 External Capacitors

To maintain the RTC accuracy, the external capacitor values C1 and C2 should be chosen to provide the manufacturer's specified load capacitance ($C_{load}$) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package.

$$C_{load} = [(C_1 + C_{in1} + C_{trace1}) \bullet (C_2 + C_{in2} + C_{trace2})] / [(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

For additional information about the External Capacitors, refer to *Intel® I/O Controller Hub (Intel® ICH)/Platform Controller Hub (PCH) Family Real Time Clock (RTC) Electrical, Mechanical, and Thermal Specification (EMTS) - AP-728* for details on fine tuning.

# 14 Asynchronous and Sideband Signals Design Guidelines

This chapter describes the topologies and layout recommendations for the asynchronous signals. Refer to the Coffee Lake processor EDS for more details.

## 14.1 Signal Descriptions

### 14.1.1 Signal Groups

**Table 14-1. Asynchronous and Sideband Legacy Signal Group (Sheet 1 of 2)**

| Signal Name | Description |
|---|---|
| PROCHOT# | PROCHOT# goes active when the Coffee Lake processor temperature monitoring sensor(s) detects that the Coffee Lake processor has reached its maximum safe operating temperature. This indicates that the Coffee Lake processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the Coffee Lake processor to activate the TCC. |
| CATERR# | This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The Coffee Lake processor will set this for non-recoverable machine check errors or other unrecoverable internal errors. On the Coffee Lake processor, CATERR# is used for signaling the following types of errors:<br>Legacy MCERRs - CATERR# is asserted for 16 BCLKs.<br>Legacy IERRs - CATERR# remains asserted until warm or cold reset. |
| PROCPWRGD | Coffee Lake processor input signal Processor Power Good: The processor requires this input signal to be a clean indication that the VCC and VDDQ power supplies and BCLK are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. |
| VCCST_PWRGD | The Coffee Lake processor requires this input signal to be clean indicating that the VCC_ST and VDDQ power supplies. This requirement applies, regardless of the S-state of the Coffee Lake processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. This is connected to the Coffee Lake processor VCCST_PWRGD signal. |
| THERMTRIP# | Coffee Lake processor output signal: Processor Asserted by the Coffee Lake processor to indicate a thermal trip event which may cause processor sever damage, causing the Coffee Lake processor to transition to an S5 state. |
| RESET# | Platform Reset signal is driven by PCH to the Coffee Lake processor. |
| PECI | The PECI interface is a controlled and reliable one-wire, bi-directional signal which is used to communicate the temperature of the Coffee Lake processor digital thermometer to the PECI host controller or to monitor and control Coffee Lake processor information such as energy, power limits, status, and DDR temperature. |
| BPM#[3:0] | Coffee Lake processor bi-directional signal that indicate the status of breakpoints and programmable counters used for monitoring Coffee Lake processor performance |
| PM_SYNC | Coffee Lake processor input signal Power Management Sync:<br>A sideband signal to communicate power management status from the PCH to the processor. |
| PM_DOWN | Coffee Lake processor output signal Power Management Down: A Sideband to PCH.<br>Indicates processor wake up event. |
| PROC_TRIGIN | Coffee Lake processor input signal: A Sideband to PCH. |
| PROC_TRIGOUT | Coffee Lake processor output signal: A Sideband to PCH. |

**Table 14-1. Asynchronous and Sideband Legacy Signal Group (Sheet 2 of 2)**

| Signal Name | Description |
|---|---|
| SVID:<br>VIDSOUT<br>VIDSCK VIDALERT# | VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface (SVID) used to transfer power management information between the Coffee Lake processor and the voltage regulator controllers. Alert signal must be routed between Clk and Data signals to minimize Cross-Talk. |

## 14.2 Topology Guidelines

This section describes topologies and layout recommendations for the legacy signals. Although these signals toggle with relatively low frequency, most of them have very high-edge rates.

***Warning:*** Inappropriate routing or lack of termination can seriously decrease signal quality and lead to electrical specification violations and even logical system failures. The following guidelines apply to all legacy signals described in this section.

- Watch for termination recommendations. If any of the signals that require motherboard termination are pulled-up to a voltage higher than VCCST, the reliability and power consumption of the Coffee Lake processor may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals.
- For Type 3 PCB, routing guidelines allow the asynchronous signals to be routed as either microstrip using 50 Ω ±15% characteristic trace impedance or stripline using 50 Ω ±10% characteristic trace impedance or orthogonal DSL (with only one layer of parallel routing, the routing on the second, adjacent layer, must be orthogonal to the first one) using 50 Ω ±10% characteristic trace impedance.
- For Type 4 PCB, routing guidelines allow the asynchronous signals to be routed as either microstrip using 50 W ±15% characteristic trace impedance or orthogonal dual - stripline using 50 Ω ±12% characteristic trace impedance.
- Changing reference plane is not recommended and may cause signal integrity degradation. In any case, if such routing cannot be avoided, use stitching vias and bypass capacitors between the reference planes near the layer transition.
- General trace spacing requirements (for 50 Ω characteristic impedance traces) specified in the following table. W is trace width and S is the space between 2 adjacent traces.

**Table 14-2. Asynchronous and Sideband Signal General Routing Guideline**

| Trace Type | Stack-up (MS/SL/DSL) | Units | Minimum Spacing (S) |
|---|---|---|---|
| Microstrip | MS | mils | 12 |
| Stripline | SL | mils | 12 |
| Dual-Stripline | DSL | mils | 12 |
| Microstrip PECI | MS[1] | mils | 18 |
| Microstrip SVID | MS[1,3] | mils | 15 |

***Notes:***
1. Parameters for SVID Bus and PECI microstrip routing only.
2. The main route segments (M) of the asynchronous signals listed below are expected to follow the spacings mentioned in the table above while breakin (BI) and breakout (BO) segments are expected to have 4 mils spacing to adjacent signals.
3. Additional spacing guidelines in Section 14.2.13, "SVID Topology".

## 14.2.1 PROCHOT# Topology

The signal can be driven either by the Coffee Lake processor, Embedded Controller (EC) or by VR. If connected from PROCHOT# to particular manufacturer temp sensor and not VR as described in the topology, such PROCHOT# connection must have the drive capabilities as defined in the future available VR specification.

Consider the following:

1. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.
2. If PROCHOT# is not used, then it must be terminated with a 1KΩ ±5% pull-up resistor to VCCSTG.

The EC output DC levels are typically 0 V and 3.3 V, Coffee Lake processor input DC levels are 0 V and 1.0 V. Coffee Lake processor's high voltage level is lower than EC's high voltage level, therefore an onboard voltage level shifter is required. An inverting logic level shifter must be used. EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the Coffee Lake processor side PROCHOT# low.

***Note:*** The Topology demonstrated is designed to be unidirectional, the processor is the receiver.

- An Agent is any (OD) driver that is connected to the PROCHOT# signal, for example VR.
- R1-6 series resistors are needed to keep the PROCHOT# signal at safe level (reduce Under-shoot) if an Agent and/or Inv OD pull-down resistor is too low (driver is too strong). The total pull-down resistance of each agent should be between 75 and 200 Ω. Total pull-down resistance is defined as the sum of internal pull-down resistance of the agent and the series resistor Ri
- Examples:
  — If internal pull-down resistor of Agent1 is 75 Ω, no additional (on board.) series resistor is needed, R1 can be omitted.

— If internal pull-down resistor of Agent2 is 15 Ω, additional (on board) series resistor is needed to increase the total pull-down resistance of Agent2, 60<R2<185 (R2 can be 70 Ω).
— The same applies to the Inv OD driver of the EC.

**Table 14-3. PROCHOT# Routing Guidelines**

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| VCCSTG | NA | NA | V | 1.0 |
| M1,2,3,4,5 | Mi | MS/SL/DSL | inches | <3 |
| M6 | Mi | MS/SL/DSL | inches | 1-11 |
| $M_{CPU}$ | $M_{CPU}$ | MS/SL/DSL | inches | 0.3-1.5 |
| Mt | Mt | MS/SL/DSL | mils | <0.3 |
| Main route (M1+M2+M3+M4+M5+M6+MCPU) | M | MS/SL/DSL | inches | 1-12 |
| Resistor Value (± 5%) | $R_{PU}$ | NA | Ω | 1000 |
| Resistor Value (± 5%) | $R_S$ | NA | Ω | 500 |
| Resistor Value (± 5%) | $R_i+R_{Agenti}$ | NA | Ω | 75-200 |
| Resistor Value (± 5%) | $R_6+R_{INVOD}$ | NA | Ω | 75-200 |
| ***Notes:***<br>1. Add DB (Dog Bone) only as needed as MS.<br>2. All segments are 50 Ω and vias are optional. | | | | |

## 14.2.2 CATERR# Topology

CATERR# indicates system has experienced a catastrophic error and cannot continue to operate. The Coffee Lake processor will set this for non-recoverable machine check errors and other internal unrecoverable errors. CATERR# is an asynchronous open drain driver signal with no on-die termination (ODT). This signal can be connected to a LED if desired. Also, this signal should have an exposed test point for easy debug access.

**Figure 14-1. Routing Illustration for CATERR# Topology**

**Table 14-4. CATERR# Routing Guidelines**

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| VCCST | NA | NA | V | 1.0 |
| Breakout Length Max | Mi | MS/SL/DSL | inches | <0.5 |
| M1 | M1 | MS/SL/DSL | inches | <12 |
| Resistor Value (± 5%) | $R_{PU}$ | NA | Ω | 50 |

### 14.2.3 PROCPWRGD Topology

**Figure 14-2. Routing Illustration for PROCPWRGD Topology**

**Table 14-5. PROCPWRGD Routing Guidelines**

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Breakout Length | BO | MS/SL/DSL | inches | <0.5 |
| M1+M2 | Mi | MS/SL/DSL | inches | 1-11 |
| Breakin Length Max. | BI | MS/SL/DSL | inches | <0.5 |

***Notes:***
1. Add DB (Dog Bone) only as needed as MS.
2. All segments are 50 Ω and vias are optional.

### 14.2.4 VCCST_PWRGOOD Topology

VCCST_PWRGD is a signal on the Coffee Lake processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specifications.

When connecting to the XDP, a series R_xdp resistor of 1 kΩ is required to avoid VR to the Coffee Lake processor line overloading and to reduce signal integrity issues on the receiver. If the driver is CMOS it's supply must not exceed VccST

VCCST_PWRGD is only 1.0 V tolerant. If a dedicated driver is used to drive the VCCST supply, the VCCST_PWRGD should meet the requirements listed below:

- VCCST_PWRGD must be valid (stable at the right level) during all power states when there is a power applied to the VccST power supply.
- VCCST_PWRGD must be de-asserted before VDDQ or VCCST power level goes blow voltage tolerance specification.

**Figure 14-3. Routing Illustration for VCCST_PWRGOOD Topology**

**Table 14-6. VCCST_PWRGOOD Routing Guidelines**

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Driver Ron | $R_{Driver}$ | NA | Ω | <200 |
| M1+M2 | Mi | MS/SL/DSL | inches | 1-11 |
| $M_{CPU}$ | $M_{CPU}$ | MS/SL/DSL | inches | 0.3-1.5 |
| Resistor Value (± 5%) | $R_S$ | NA | Ω | 60 |
| Resistor Value (± 5%) | $R_{PU}$ | NA | Ω | 1000 |

***Notes:***
1. All traces can be MS/SL/DSL as long as above guidelines are met.
2. Add DB (Dog Bone) only as needed on MS.
3. All segments are 50 Ω and vias are optional.

## 14.2.5 THERMTRIP# Topology

**Figure 14-4. Routing Illustration for THERMTRIP# Topology**

RLS series resistor is needed to keep the THERMTRIP# signal at safe level (reduce Under-shoot) if OD LS pull-down resistor is too low (driver is too strong). The total pull-down resistance of OD LS should be between 55 and 200 Ω. Total pull-down resistance is defined as the sum of internal pull-down resistance of the OD LS and the series resistor RLS. Examples:

- If internal pull-down resistor of OD LS is 55 Ω, no additional (on board) series resistor is needed => RLS can be omitted.
- If internal pull-down resistor of OD LS is 15 Ω, additional (on board) series resistor is needed to increase the total pull-down resistance of OD LS in range: $40<R_{LS}<185$, in order to meet the guideline: $55<R_{LS}+R_{ODLS}<200$.

**Table 14-7. THERMTRIP# Routing Guidelines (Sheet 1 of 2)**

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| VccST | NA | NA | V | 1.0 |
| Breakout Length | BO | MS/SL/DSL | inches | <0.5 |
| M1,2 | Mi | MS/SL/DSL | inches | <10 |
| $M_{EC}$ | $M_{EC}$ | MS/SL/DSL | inches | <10 |

**Table 14-7. THERMTRIP# Routing Guidelines (Sheet 2 of 2)**

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Breakin Length | BI | MS/SL/DSL | inches | 0.3-2 |
| Resistor Value (± 5%) | $R_{PCH}$ | NA | Ω | 620 |
| Resistor Value (± 5%) | $R_{PU}$ | NA | Ω | 1000 |
| Resistor Value (± 5%) | $R_{ODLS}+R_{LS}$ | NA | Ω | 55-200 |

***Notes:***
1. THERMTRIP# should be connected to EC or any other monitoring agent.
2. Add DB (Dog Bone) only as needed on MS.
3. All segments are 50 Ω and vias are optional.

## 14.2.6 RESET# (PLTRST#) Topology

**Figure 14-5. Routing Illustration for RESET# (PLTRST#) Topology**

**Table 14-8. RESET# Routing Guidelines**

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Breakout Length | BO | MS/SL/DSL | inches | <0.5 |
| M1+M2 | Mi | MS/SL/DSL | inches | 1-11 |
| Breakin Length Max. | BI | MS/SL/DSL | inches | <0.5 |

***Notes:***
1. Add DB (Dog Bone) only as needed as MS.
2. All segments are 50 Ω and vias are optional.

## 14.2.7 Platform Environmental Control Interface (PECI) Topology

The digital thermometer will be used to communicate Coffee Lake processor core temperature to the platform. Access to the digital thermometer is through the Platform Environmental Control Interface (PECI).

The PECI interface is a controlled and reliable one-wire bi-directional signal which is used to communicate the temperature of the Coffee Lake processor digital thermometer to the PECI host controller or to monitor and control the Coffee Lake processor information such as energy, power limits, status and DDR temperature. Refer to the Platform Environmental Control Interface (PECI) 3 Specification for more architectural details. Also, refer to the *Processor Platform Environment Control Interface Implementation Guide* for commands for firmware coding. If a different PECI topology is implemented or one of the agents does not meet the PECI 3 Specifications, a simulation must be performed to ensure adequate signal quality and maximal operating frequency.

PECI spec has the bus in a L level when there are no transactions happening. The PECI host would normally drive the line H to start transactions, and the PECI clients (aka CPU) respond by over driving and keeping the line H when the Host tried to drive L. Only the PECI host drives the bus L, Clients can only pull up.

If there is no PECI host talking to the CPU and the pin is unused, put a 200-400Ω PD resistor to GND on the CPU pin to make sure it's statically L. it's not recommend to tie the CPU pin directly to GND.

***Note:*** PECI routing guidelines were validated up to a host bandwidth of 1.6 Mbps.

***Note:*** **Intel Recommends using PECI Bus,** If PECI is not used, it should be terminated to GND with 200-400Ω resistor.

***Note:*** The VREF_PECI_EC voltage reference from the processor to the EC should be connected to VccST (PECI reference voltage)

## PECI Routing Guidelines

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Breakout Length | BO | MS/SL/DSL | inches | <0.5 |
| M1 | M1 | MS/SL/DSL | inches | 3-12 |
| M2 | M2 | MS/SL/DSL | inches | 3-8 |
| Breakin Length Max. | BI | MS/SL/DSL | inches | <0.5 |
| Resistor Value (±5%) | $R_{EC}$ | NA | Ω | 33 |
| Resistor Value (±5%) | $R_{PCH}$ | NA | Ω | 13 |

***Notes:***
1. Add DB (Dog Bone) only as needed as MS.
2. All segments are 50 Ohm and vias are optional.
3. If routed MS, PECI requires 18 mils (0.457 mm) spacing to other signals.
4. Adding another agent requires total change of topology.

- If PECI is not used on the CPU, then it should be terminated to GND with 200-400ohm resistor; the PCH-H PECI pin should be terminated to GND with a weak resistor if it is not connected to the CPU PECI pin, or it can be connected to the CPU PECI pin in order the share the same termination resistor.
- If PECI is used on the CPU, and C10 is supported, then PECI bus should also be connected to the PCH-H PECI pin (in addition to the PECI host) to correctly support C10.

- If PECI is used on the CPU, and C10 is not supported, then PECI bus is not required to be connected to the PCH-H PECI pin.

## 14.2.8 BPM#[3:0] Topology

Route the BPM#[3:0] signals point-to-point from the Coffee Lake processor pin to the XDP debug port connector. Adequate termination for these signals is provided within the I/O design of the Coffee Lake processor and on the ITP-XDP hardware. No external components are required. Length match these signals to within ±360 mils (9.1 mm). Stubs on these nets should be limited to less than 1400 mils (35.5 mm) in length.

**Figure 14-6. BPM#[3:0] Topology**

**Table 14-9. BPM#[3:0] Routing Guidelines**

| Parameter | Segment | Routing Layer (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Connector Length | CN | MS/SL | inches | 1 - 6 |
| ***Note:*** All segments are 50 Ω and vias are optional. | | | | |

## 14.2.9 PM_SYNC Topology

**Figure 14-7. Routing Illustration for PM_SYNC Topology**

**Table 14-10. PM_SYNC Routing Guidelines**

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Breakout Length:<br>Short route: M1 + M2 < 3”<br>Long route: M1 + M2 > 3” | BO | MS/SL/DSL | inches | <0.2<br><0.6 |
| M1+M2:<br>Short route<br>Long route | Mi | MS/SL/DSL | inches | 1-3<br>3-11 |
| Breakin Length Max. | BI | MS/SL/DSL | inches | <0.5 |
| Resistor Value (±5%) | Rs | NA | Ω | 30 |
| ***Note:*** All segments are 50 Ω and vias are optional. | | | | |

## 14.2.10 PM_DOWN Topology

### Figure 14-8. Routing Illustration for PM_DOWN Topology

***Note:*** RPD is Un-stuffed

### Table 14-11. PM_DOWN Routing Guidelines

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Breakout Length:<br>Short route: M1 + M2 > 3”<br>Long route: M1 + M2 < 3” | BO | MS/SL/DSL | inches | <0.2<br><0.6 |
| M1+M2:<br>Short route<br>Long route | Mi | MS/SL/DSL | inches | 1-3<br>3-11 |
| Breakin Length Max. | BI | MS/SL/DSL | inches | <0.5 |
| Resistor Value (±5%) | Rs | NA | Ω | 20 |
| Resistor Value (±5%) | $R_{PD}$ | NA | Ω | Unstuffed |
| ***Note:*** All segments are 50 Ω and vias are optional. | | | | |

## 14.2.11 PROC_TRIGIN Topology (PCH to Processor_TRIGIN)

### Figure 14-9. Routing Illustration for PROC_TRIGIN Topology

### Table 14-12. PROC_TRIGIN Routing Guidelines

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Breakout Length | BO | MS/SL/DSL | inches | <0.5 |
| M1+M2: | Mi | MS/SL/DSL | inches | 1-10 |
| Breakin Length Max. | BI | MS/SL/DSL | inches | <0.5 |
| ***Note:*** All segments are 50 Ω and vias are optional. | | | | |

## 14.2.12 PROC_TRIGOUT Topology (Processor to PCH_TRIGIN)

**Figure 14-10.Routing Illustration for PROC_TRIGOUT Topology**

**Table 14-13. PROC_TRIGOUT Routing Guidelines**

| Parameter | Segment | Stackup (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|---|
| Breakout Length | BO | MS/SL/DSL | inches | <0.5 |
| M1+M2 | Mi | MS/SL/DSL | inches | 1-10 |
| Breakin Length Max. | BI | MS/SL/DSL | inches | <0.5 |
| ***Note:*** All segments are 50 Ω and vias are optional. | | | | |

## 14.2.13 SVID Topology

**Figure 14-11.Routing Illustration for SVID Topology**

Figure 14-11 demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

***Notes:***

- If less than 4 VRs are used, remove the first devices from the topology. For example: if 3 VRs are used, remove VR1 from the topology.
- The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
- Route the Alert signal between the Clock and the Data signals.

**Table 14-14. SVID Bus Routing Guidelines**

| Signal | W1 [inches] | W2 [inches] | W3/4/5 [inches] | W2+W3+W4+W5 [inches] | W51 [inches] | W52 [inches] | $R_{PU1}$ [Ω] | $R_{PU2}$ [Ω] | $R_{S1}$ [Ω] | $R_{S2}$ [Ω] | $VCC_{ST}$ [v] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VIDSOUT | 0.5-3 | 1-15 | 0.5-4 | 3-17 | <0.1 | <0.1 | 100 | 100 | 0 | 10 | 1.0 |
| VIDSCK | | | | | | | Empty | 45 | 0 | 50 | |
| VIDALERT # | | | | | | | 56 | Empty | 220 | 0 | |

***Note:*** For additional information regarding SVID and power management refer to *"Power Architecture Guide"* .

**Table 14-15. SVID Minimum Spacing Guidelines**

| Coupling length [inches] | Stripline [mils] | Microstrip [mils] |
|---|---|---|
| <0.5 | 5 | 5 |
| <2.5 | 10 | 10 |
| >2.5 | 12 | 15 |

### 14.2.14 COMP Signals

Refer to Coffee Lake Processor External Design Specification (EDS) Volume 1 of 2 for termination requirements for all COMP signals.

## 14.3 ESD Protection for Asynchronous Signals

Asynchronous signals are not subject to signal integrity issues but could be victims of ESD events resulting in catastrophic system failures. Therefore, some of them deserve extra care during board routing: good referencing from top or bottom layer, placement of noise filters, no exposure to the edges of a board.

Refer to Chapter 49, "Electromagnetic Compatibility" for the detailed info on ESD sensitive nets and their treatments.

§ §

# 15 Flexible I/O

## 15.1 Overview

Flexible Input/Output (I/O) is a technology that allows some of the PCH High Speed I/O (HSIO) lanes to be configured for connection to a Gigabit Ethernet (GbE) Controller, a PCIe* Controller, a Extensible Host Controller Interface (XHCI) USB 3.1 Controller, or a Advanced Host Controller Interface (AHCI) SATA Controller. Flexible I/O enables customers to optimize the allocation of the PCH HSIO interfaces to better meet the I/O needs of their system.

***Note:*** Some Flexible I/O muxing capabilities are not available on all SKUs. Refer to the PCH External Design Specifications (EDS) for specific SKU implementation details.

## 15.2 Flexible I/O Implementation

### 15.2.1 Cannon Lake HPCH-H

**Figure 15-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H**

| Flex I/O Lane | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| High Speed I/O (HSIO) Type and Lane | USB3.1 Gen1/Gen2 #1 | USB3.1 Gen1/Gen2 #2 | USB3.1 Gen1/Gen2 #3 | USB3.1 Gen1/Gen2 #4 | USB3.1 Gen1/Gen2 #5 | USB3.1 Gen1/Gen2 #6 | USB3.1 Gen1 #7 | USB3.1 Gen1 #8 | USB3.1 Gen1 #9 | USB3.1 Gen1 #10 | PCIe* #5 | PCIe* #6 | PCIe* #7 | PCIe* #8 | PCIe* #9 | PCIe* #10 | PCIe* #11 | PCIe* #12 | PCIe* #13 | PCIe* #14 | PCIe* #15 | PCIe* #16 | PCIe* #17 | PCIe* #18 | PCIe* #19 | PCIe* #20 | PCIe* #21 | PCIe* #22 | PCIe* #23 | PCIe* #24 |
| | | | | | | | PCIe* #1 | PCIe* #2 | PCIe* #3 | PCIe* #4 | GbE | | | | GbE | | SATA 0a | GbE | GbE | SATA 1b | SATA 2 | SATA 3 | SATA 4 | SATA 5 | SATA 6 | SATA 7 | | | | |
| | | | | | | | | | | | | | | | | | | SATA 1a | SATA 0b | | | | | | | | | | | |
| Intel® RST Support | | | | | | | No Support | | | | No Support | | | | Yes | | | | | No Support | | | Yes | | | | Yes | | | |

The 30 HSIO lanes on PCH-H supports the following configurations:

1. Up to 24 PCIe* Lanes
   — A maximum of 16 PCIe* Ports (or devices) can be enabled
      - When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:

   Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)

- PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured

2. Up to 10 SATA Lanes
   - A maximum of 8 SATA Ports (or devices) can be enabled
   - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
   - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 6 USB3.1 Gen1/Gen2 Lanes and 4 USB3.1 Gen1 Lanes
   - A maximum of 10 USB3.1 Ports (or devices) can be enabled
   - USB3.1 Gen1 = 5 GT/s
   - USB3.1 Gen2 = 10 GT/s
4. Up to 4 GbE Lanes
   - A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe* storage devices
   - x2 and x4 PCIe* NVMe SSD
   - x2 and x4 Next Generation Intel® Optane™ Memory
   - See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers, configurations, and lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support
6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

# 16 PCH PCI Express* Interface Design Guidelines

## 16.1 PCH PCI Express* Interface Configuration Details

### Figure 16-1. Supported PCH PCI Express* Link Configurations

| PCH-H Details | | PCIe* Controller #1 | | | | PCIe* Controller #2 | | | | PCIe* Controller #3 | | | | PCIe* Controller #4 | | | | PCIe* Controller #5 | | | | PCIe* Controller #6 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | Cycle Router #1 | | | | | | | | Cycle Router #3 | | | | Cycle Router #2 | | | |
| Flex I/O Lane # | | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 |
| PCIe* Lane # | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
| HM370 | 1x4 | | | | | | | | | RP 9 | | | | RP 13 | | | | RP 17 | | | | RP 21 | | | |
| | 1x4 LR | | | | | | | | | RP 9 | | | | RP 13 | | | | RP 17 | | | | RP 21 | | | |
| | 2x2 | | | | | | | | | RP 9 | | RP 11 | | RP 13 | | RP 15 | | RP 17 | | RP 19 | | RP 21 | | RP 23 | |
| | 1x2+2x1 | | | | | | | | | RP 9 | | RP 11 | RP 12 | RP 13 | | RP 15 | RP 16 | RP 17 | | RP 19 | RP 20 | RP 21 | | RP 23 | RP 24 |
| | 2x1+1x2 | | | | | | | | | RP 12 | RP 11 | RP 9 | | RP 16 | RP 15 | RP 13 | | RP 20 | RP 19 | RP 17 | | RP 24 | RP 23 | RP 21 | |
| | 4x1 | | | | | | | | | RP 9 | RP 10 | RP 11 | RP 12 | RP 13 | RP 14 | RP 15 | RP 16 | RP 17 | RP 18 | RP 19 | RP 20 | RP 21 | RP 22 | RP 23 | RP 24 |
| QM370 | 1x4 | | | | | RP 5 | | | | RP 9 | | | | RP 13 | | | | RP 17 | | | | RP 21 | | | |
| | 1x4 LR | | | | | RP 5 | | | | RP 9 | | | | RP 13 | | | | RP 17 | | | | RP 21 | | | |
| | 2x2 | | | | | RP 5 | | RP 7 | | RP 9 | | RP 11 | | RP 13 | | RP 15 | | RP 17 | | RP 19 | | RP 21 | | RP 23 | |
| | 1x2+2x1 | | | | | RP 5 | | RP 7 | RP 8 | RP 9 | | RP 11 | RP 12 | RP 13 | | RP 15 | RP 16 | RP 17 | | RP 19 | RP 20 | RP 21 | | RP 23 | RP 24 |
| | 2x1+1x2 | | | | | RP 8 | RP 7 | RP 5 | | RP 12 | RP 11 | RP 9 | | RP 16 | RP 15 | RP 13 | | RP 20 | RP 19 | RP 17 | | RP 24 | RP 23 | RP 21 | |
| | 4x1 | | | | | RP 5 | RP 6 | RP 7 | RP 8 | RP 9 | RP 10 | RP 11 | RP 12 | RP 13 | RP 14 | RP 15 | RP 16 | RP 17 | RP 18 | RP 19 | RP 20 | RP 21 | RP 22 | RP 23 | RP 24 |
| CM246 | 1x4 | RP 1 | | | | RP 5 | | | | RP 9 | | | | RP 13 | | | | RP 17 | | | | RP 21 | | | |
| | 1x4 LR | RP 1 | | | | RP 5 | | | | RP 9 | | | | RP 13 | | | | RP 17 | | | | RP 21 | | | |
| | 2x2 | RP 1 | | RP 3 | | RP 5 | | RP 7 | | RP 9 | | RP 11 | | RP 13 | | RP 15 | | RP 17 | | RP 19 | | RP 21 | | RP 23 | |
| | 1x2+2x1 | RP 1 | | RP 3 | RP 4 | RP 5 | | RP 7 | RP 8 | RP 9 | | RP 11 | RP 12 | RP 13 | | RP 15 | RP 16 | RP 17 | | RP 19 | RP 20 | RP 21 | | RP 23 | RP 24 |
| | 2x1+1x2 | RP 4 | RP 3 | RP 1 | | RP 8 | RP 7 | RP 5 | | RP 12 | RP 11 | RP 9 | | RP 16 | RP 15 | RP 13 | | RP 20 | RP 19 | RP 17 | | RP 24 | RP 23 | RP 21 | |
| | 4x1 | RP 1 | RP 2 | RP 3 | RP 4 | RP 5 | RP 6 | RP 7 | RP 8 | RP 9 | RP 10 | RP 11 | RP 12 | RP 13 | RP 14 | RP 15 | RP 16 | RP 17 | RP 18 | RP 19 | RP 20 | RP 21 | RP 22 | RP 23 | RP 24 |

***Notes:***

1. RP# refers to a specific PCH PCI Express* Root Port #; for example RP3 = PCH PCI Express* Root Port 3
2. A PCIe* Lane is composed of a single pair of Transmit (TX) and Receive (RX) differential pairs, for a total of four data wires per PCIe* Lane (such as, PCIE[3]_TXP/ PCIE[3]_TXN and PCIE[3]_RXP/ PCIE[3]_RXN make up PCIe Lane 3). A connection between two PCIe* devices is known as a PCIe* Link, and is built up from a collection of one or more PCIe* Lanes which make up the width of the link (such as bundling 2 PCIe* Lanes together would make a x2 PCIe* Link). A PCIe* Link is addressed by the lowest number PCIe* Lane it connects to and is known as the PCIe* Root Port (such as a x2 PCIe* Link connected to PCIe* Lanes 3 and 4 would be called x2 PCIe* Root Port 3).
3. The PCIe* Lanes can be configured independently from one another but the max number of configured Root Ports (Devices) must not be exceeded
   - PCH-H supports a maximum of 16 PCIe* Root Ports (or devices) can be enabled
   - When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
     - PCH-H Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
4. Unidentified lanes within a PCIe* Link Configuration are disabled but their physical lanes are used for the identified Root Port
5. Supports up to Three Remapped (Intel® Rapid Storage Technology) PCIe* Storage Devices
   - Cells highlighted in Green identify controllers, configurations, and lanes that can be used for a x2 or x4 Intel® Rapid Storage Technology Remapped PCIe* NVMe SSD or a x2 or x4 Next Generation Intel® Optane™ Memory Device
6. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCI Express* Root Ports
7. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs
8. Reference and understand the PCIe* High Speed I/O Muxing details covered in the "Flexible I/O" Chapter
9. Lane Reversal Supported Motherboard PCIe* Configurations = 1x4 and 2x1+1x2
   - The 2x1+1x2 configuration is enabled by setting the PCIe* Controller soft straps to 1x2+2x1 with Lane Reversal Enabled
   - 1x4 = 1x4 with Lane Reversal Disabled, 1x4 LR = 1x4 with Lane Reversal Enabled

10. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool. These unused SATA/PCIe* Combo Lanes must not be assigned as polarity based.
    — Refer to the "Flexible I/O" chapter for SATA/PCIe* Combo Lane identification

## 16.2 Intel® Rapid Storage Technology (Intel® RST) for PCH PCIe* Storage

Intel® Rapid Storage Technology for PCIe* Storage includes the PCH PCIe* Controller Remapping Hardware, also referred to as Cycle Routers, and the Intel® RST Driver. The Remapping Hardware is a PCH PCIe* Controller architecture feature that works with the Intel® RST Driver to control and remap PCIe* storage devices to the PCH AHCI SATA Controller.

The PCH has multiple PCIe* Controllers where some, not all, of these Controllers have the Remapping Hardware. These specific PCIe* Controllers along with the Intel® RST Driver handle the remapping for x2 or x4 PCIe* storage devices. Special care must be taken to make sure the correct PCH PCIe* Lanes are used that are associated with these specific PCIe* Controllers. Figure 6-4 describes and identifies all of the Intel® RST PCIe* controller, configuration, and lane support details.

***Note:*** The Intel® RST for PCIe* Storage support details will vary depending on the PCH SKU. Refer to the Platform Controller Hub (PCH) External Design Specification (EDS) Volume 1 for the complete PCH SKU details

## 16.3 PCH PCI Express* Signal Descriptions

### Table 16-1. PCH PCI Express* Signal Groups

| Group | Signal Name | Description |
|---|---|---|
| Data | PCIE[24:1]_TXN & PCIE[24:1]_TXP | PCI Express* Transmit Differential-Pair |
| | PCIE[24:1]_RXN & PCIE[24:1]_RXP | PCI Express* Receive Differential-Pair |
| RCOMP | PCIE_RCOMPN and PCIE_RCOMPP | Impedance Compensation Inputs |

# 16.4 PCH PCI Express* Routing Guidelines

## 16.4.1 PCH PCI Express* Device Down Guidelines

**Figure 16-2. PCH PCI Express* Device Down at 2.5, 5, and 8 GT/s Topology**

**Table 16-2. PCH PCI Express* Device Down Routing Guidelines**

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | 2.5 GT/s Routing | 5GT/s Routing | 8 GT/s Routing |
|---|---|---|---|---|---|---|
| Reference Plane | BO, M1, M2, M3 | MS/SL/DSL | NA | GND | GND | GND |
| Break-Out Max Length | BO | MS/SL/DSL | mm(mils) | 15.2(598.42) | 15.2(598.42) | 15.2(598.42) |
| Post-AC Capacitor Max Length | M3 | MS | mm(mils) | 8(314.96) | 8(314.96) | 8(314.96) |
| Total Motherboard Length Range | BO+M1+M2+M3 | BO=MS/SL/DSL<br>M1=MS/SL/DSL<br>M2=MS/SL/DSL<br>M3=MS | mm(mils) | 64(2519.68) to 356(14015.75) | 64(2519.68) to 279(10984.25) | 64(2519.68) to 229(9015.75) |
| Motherboard Differential Pair Length Matching | BO, M1, M2, M3 | MS/SL/DSL | mm(mils) | Within same layer = ± 0.254mm (± 10mils)<br>BO+M1+M2+M3 = ± 0.127mm (± 5mils) | | |
| AC Coupling Capacitor | BO, M3 | MS | nF | 75 - 265 | 75 - 265 | 176 - 265 |
| Max Via Count | BO, M1, M2, M3 | NA | vias | 6 | 4 | 3 |

***Notes:***
1. For x1 links route the TX and RX signals of each link next to each other on the same layer following interleaved routing
2. For x2 and x4 links route the TX and RX signals non-interleaved or semi-interleaved routing in separate groups. Non-interleaved routing is preferred to reduce the effects of cross talk
3. The Break-Out Segment (BO) if needed, may start with an initial 4mm (157.48 mils) in length of tighter pair-to-pair spacing of 0.11mm to 0.16mm (4 -6 mils)
4. Although min and max capacitor values are shown, 220 nF nominal capacitors are recommended for Gen 3 compliance
5. Although min and max capacitor values are shown, 100 nF nominal capacitors are recommended for Gen 2.
6. AC coupling capacitors on motherboard are recommended to be placed closer to either the connector or processor side. Avoid placing AC caps at the center of the motherboard
7. Micro-Vias within the breakout area are not counted against maximum via total
8. Any PCI Express* Transmit and associated Receive Differential Pair not being used or implemented on the platform must be left as no connects

## 16.4.2 PCH PCI Express* Add-In Card Connector Guidelines

### Figure 16-3. PCH PCI Express* Add-In Card Connector Topology

### Table 16-3. PCH PCI Express* Add-In Card Connector Routing Guidelines

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | 2.5 GT/s Routing | 5 GT/s Routing | 8 GT/s Routing |
|---|---|---|---|---|---|---|
| Reference Plane | BO, M1, M2, M3, M4, M5 | MS/SL/DSL | NA | GND | GND | GND |
| Break-Out Max Length | BO | MS/SL/DSL | mm(mils) | 15.2(598.42) | 15.2(598.42) | 15.2(598.42) |
| Post-AC Capacitor Max Length | M3 | MS | mm(mils) | 8(314.96) | 8(314.96) | 8(314.96) |
| Card Break-In Max Length | M5 | MS | mm(mils) | 8(314.96) | 8(314.96) | 8(314.96) |
| Total Motherboard Length Range | BO+M1+M2+M3 | BO=MS/SL/DSL<br>M1=MS/SL/DSL<br>M2=MS/SL/DSL<br>M3=MS | mm(mils) | 64(2519.68) to 330(12992.13) | 64(2519.68) to 229(9015.75) | 64(2519.68) to 203(7992.13) |
| Add-in-Card Max Length | M4+M5 | MS | mm(mils) | 38(1496.06) | 38(1496.06) | 38(1496.06) |
| Motherboard Differential Pair Length Matching | BO, M1, M2, M3 | MS/SL/DSL | mm(mils) | Within same layer = ± 0.254mm (± 10mils)<br>BO+M1+M2+M3 = ± 0.127mm (± 5mils) | | |
| AC Coupling Capacitor | BO, M3 | MS | nF | 75 - 265 | 75 - 265 | 176 - 265 |
| Motherboard Max Via Count | BO, M1, M2, M3 | NA | vias | RX = 4<br>TX = 4 | RX = 4<br>TX = 4 | RX = 2<br>TX = 3 |
| Add-In Card Max Via Count | M4, M5 | NA | vias | 1 | 1 | 1 |

***Notes:***
1. For x1 links route the TX and RX signals of each link next to each other on the same layer following interleaved routing
2. For x2 and x4 links route the TX and RX signals non-interleaved or semi-interleaved routing in separate groups. Non-interleaved routing is preferred to reduce the effects of cross talk
3. The Break-Out Segment (BO) if needed, may start with an initial 4mm (157.48 mils) in length of tighter pair-to-pair spacing of 0.11mm to 0.16mm (4 -6 mils)
4. Although min and max capacitor values are shown, 220 nF nominal capacitors are recommended for Gen 3 compliance
5. Although min and max capacitor values are shown, 100 nF nominal capacitors are recommended for Gen 2.
6. AC coupling capacitors on motherboard are recommended to be placed closer to the Add-In Card Connector side. Avoid placing AC caps at the center of the motherboard
7. Micro-Vias within the breakout area are not counted against maximum via total
8. Any PCI Express* Transmit and associated Receive Differential Pair not being used or implemented on the platform must be left as no connects

## 16.4.3 PCH PCI Express* with Internal Cable Guidelines

### Figure 16-4. PCH PCI Express* with Internal Cable Topology

### Table 16-4. PCH PCI Express* with Internal Cable Routing Guidelines

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | 2.5 GT/s Routing | 5 GT/s Routing | 8 GT/s Routing |
|---|---|---|---|---|---|---|
| Reference Plane | BO, M1, M2, M3, M4, M5 | MS/SL/DSL | NA | GND | GND | GND |
| Break-Out Max Length | BO | MS/SL/DSL | mm(mils) | 15.2(598.42) | 15.2(598.42) | 15.2(598.42) |
| Post-AC Capacitor Max Length | M2 | MS | mm(mils) | 8(314.96) | 8(314.96) | 8(314.96) |
| Card Break-In Max Length | M5 | MS | mm(mils) | 8(314.96) | 8(314.96) | 8(314.96) |
| Total Length Range | BO+M1+M2+M3 +M4+M5 | BO=MS/SL/DSL<br>M1=MS/SL/DSL<br>M2=MS/SL/DSL<br>M3=MS | mm(mils) | See Table Below | See Table Below | See Table Below |
| Add-in-Card Max Length | M4+M5 | MS | mm(mils) | 38(1496.06) | 38(1496.06) | 38(1496.06) |
| Motherboard Differential Pair Length Matching | BO, M1, M2 | MS/SL/DSL | mm(mils) | Within same layer = ± 0.254mm (± 10mils)<br>BO+M1+M2 = ± 0.127mm (± 5mils) | | |
| AC Coupling Capacitor | M2, M5 | MS | nF | 75 - 265 | 75 - 265 | 176 - 265 |
| Motherboard Max Via Count | BO, M1, M2, M3 | NA | vias | RX = 2<br>TX = 2 | RX = 1<br>TX = 2 | RX = 1<br>TX = 2 |
| Add-In Card Max Via Count | M4, M5 | NA | vias | 1 | 1 | 1 |

***Notes:***
1. For x1 links route the TX and RX signals of each link next to each other on the same layer following interleaved routing
2. For x2 and x4 links route the TX and RX signals non-interleaved or semi-interleaved routing in separate groups. Non-interleaved routing is preferred to reduce the effects of cross talk
3. The Break-Out Segment (BO) if needed, may start with an initial 4mm (157.48 mils) in length of tighter pair-to-pair spacing of 0.11mm to 0.16mm (4 -6 mils)
4. Although min and max capacitor values are shown, 220 nF nominal capacitors are recommended for Gen 3 compliance
5. Although min and max capacitor values are shown, 100 nF nominal capacitors are recommended for Gen 2.
6. AC coupling capacitors on motherboard are recommended to be placed closer to the Connector side. Avoid placing AC caps at the center of the motherboard
7. Micro-Vias within the breakout area are not counted against maximum via total
8. Any PCI Express* Transmit and associated Receive Differential Pair not being used or implemented on the platform must be left as no connects

**Table 16-5. PCH PCI Express* with Internal Cable Routing Length versus Cable Loss**

| Up to 2.5 GHz (Gen2) | | Up to 4.0 GHz (Gen3) | |
|---|---|---|---|
| Total Length B0+M1+M2+M3+M4+M5 | Cable Loss | Total Length B0+M1+M2+M3+M4+M5 | Cable Loss |
| 3000 mils (76.2 mm) | 3.5 dB | 3000 mils (76.2 mm) | 3.0 dB |
| 3500 mils (88.9 mm) | 3 dB | | |
| 4500 mils (114.3 mm) | 2.5 dB | 4000 mils (101.6 mm) | 2.0 dB |
| 5500 mils (139.7 mm) | 2 dB | | |
| 6500 mils (165.1 mm) | 1.5 dB | 5000 mils (127.0 mm) | 1.0 dB |
| 7000 mils (177.8 mm) | 1 dB | | |

## 16.4.4 PCH PCI Express* M.2 Socket Module Guidelines

The routing guidelines for a PCIe* interface used with an M.2 Socket Module are covered in the "M.2 - Next Generation Form Factor (NGFF)" chapter.

***Note:*** Intel® Optane™ Memory Device support requires the following:

- M.2 Socket 2 or a M.2 Socket 3 form factor module connector
- Connect PCH PLTRST# to the M.2 Socket PLTRST# module pin
- Connect a PCH SRCCLKREQ# pin to the M.2 Socket CLKREQ# module pin

## 16.4.5 PCH PCI Express* Impedance Compensation Guidelines

**Figure 16-5. PCH PCIE_RCOMPP and PCIE_RCOMPN Connections**

**Table 16-6. PCH PCI Express* Compensation Routing Guidelines (Sheet 1 of 2)**

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | 2.5 GT/s Routing | 5 GT/s Routing | 8 GT/s Routing |
|---|---|---|---|---|---|---|
| Reference Plane | M1, M2 | MS/SL/DSL | NA | GND | GND | GND |
| Series Resistor | M1, M2 | MS | Ohms | 100 +/-1% | 100 +/-1% | 100 +/-1% |
| Motherboard Max Via Count | M1, M2 | NA | vias | 2 | 2 | 2 |
| Motherboard Length Matching | M1, M2 | MS/SL/DSL | mm(mils) | M1- M2 = ± 0.127mm (± 5mils) | | |

**Table 16-6. PCH PCI Express* Compensation Routing Guidelines (Sheet 2 of 2)**

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | 2.5 GT/s Routing | 5 GT/s Routing | 8 GT/s Routing |
|---|---|---|---|---|---|---|
| ***Notes:***<br>1. Recommended placing a VSS shield of at least 4mils (0.1016mm) wide between the RCOMP signals and any adjacent I/O signal<br>2. Avoid routing close to any clocks<br>3. Micro-Vias within the breakout area are not counted against maximum via total<br>4. Must maintain low DC resistance routing (<0.1 ohm) | | | | | | |

## 16.4.6 PCH PCI Express* Lane Polarity Inversion

The PCI Express* Base Specification requires polarity inversion to be supported independently by all receivers across the Link where each differential pair within each Lane of the PCIe* Link handles its own polarity inversion. Polarity inversion does not imply direction inversion or direction reversal; that is, the Tx differential pair from one device must still connect to the Rx differential pair on the receiving device, per the PCIe* Base Specification.

***Note:*** Polarity Inversion is not the same as "PCI Express* Controller Lane Reversal"

**Figure 16-6. PCH Polarity Inversion on a TX to RX Interconnect**

## 16.4.7 PCH PCI Express* Controller Lane Reversal

For each PCH PCIe* Controller we support end-to-end lane reversal across the four lanes mapped to a controller for the following two motherboard PCIe* configurations

***Notes:***

- Lane Reversal Supported Motherboard PCIe* Configurations = 1x4 and 2x1+1x2
  - The 2x1+1x2 configuration is enabled by setting the PCIe* Controller soft straps to 1x2+2x1 with Lane Reversal Enabled.
- PCH PCI Express* Controller Lane Reversal is not the same as PCI Express* Lane Polarity Inversion

## Table 16-7. PCH PCIe* Configuration Lane Reversal Mapping

| PCIe* Configuration | PCI Express* Lanes | | | | | | PCI Express* Down Device or Connector Lanes |
|---|---|---|---|---|---|---|---|
| | PCIe* Controller #1 | PCIe* Controller #2 | PCIe* Controller #3 | PCIe* Controller #4 | PCIe* Controller #5 | PCIe* Controller #6 | |
| 1x4 | 1 | 5 | 9 | 13 | 17 | 21 | 3 |
| | 2 | 6 | 10 | 14 | 18 | 22 | 2 |
| | 3 | 7 | 11 | 15 | 19 | 23 | 1 |
| | 4 | 8 | 12 | 16 | 20 | 24 | 0 |
| 2x1+1x2 | 1 | 5 | 9 | 13 | 17 | 21 | 0 |
| | 2 | 6 | 10 | 14 | 18 | 22 | 0 |
| | 3 | 7 | 11 | 15 | 19 | 23 | 1 |
| | 4 | 8 | 12 | 16 | 20 | 24 | 0 |

## Figure 16-7. 1x4 Configuration PCH PCI Express* Lane Reversal Example

**Figure 16-8. 2x1+1x2 Configuration PCH PCI Express* Lane Reversal Example**

# 17 SATA Interface Guidelines

## 17.1 Overview

The following sections provides routing requirements and trace guidelines for SATA Gen 1 (1.5 Gb/s), Gen 2 (3 Gb/s), and SATA Gen 3 (6 Gb/s).

The PCH supports up to six SATA ports that is capable of independent DMA operation. The SATA controllers are completely software transparent with an AHCI interface and only supports AHCI mode using memory space (IDE mode is not supported).

**Table 17-1. SATA Reference Documents**

| Title | Document # / Location |
|---|---|
| SATA-IO Certified Test Laboratories | *www.sata-io.org* |
| High Speed Internal Connector and Cable – Specification | 549136 |
| An Electrical Study on the Implementation of 85Ω Nominal Differential Impedance Transmission Lines in High-Speed Serial ATA Interface - Technical White Paper | 549023 |

**Table 17-2. SATA Compliance Documents**

| Title | Document # / Location |
|---|---|
| Serial ATA Specification, Revision 3.2 | *www.sata-io.org* |
| SATA Express Transmitter Test Methodology - Technical White Paper | 548875 |

## 17.2 SATA Signal Description

### 17.2.1 SATA Signal Groups

**Table 17-3. SATA Signal Groups**

| Group | Signal Name | Description |
|---|---|---|
| SATA Receive | SATA0[B:A]_RXP/RXN, SATA1[B:A]_RXP/RXN, SATA[5:2]_RXP/RXN | Differential Receive Pair |
| SATA Transmit | SATA0[B:A]_TXP/TXN, SATA1[B:A]_TXP/TXN, SATA[5:2]_TXP/TXN. | Differential Transmit Pair |
| Power Control | DEVSLP[5:0]. | Host Controlled Power State |
| GPIO | SATAGP[5:0] | General Purpose |
| LED | SATALED# | LED |

### 17.2.2 SATA Signal Considerations

#### 17.2.2.1 SATA General Purpose (SATAGP) Signals

- The PCH provides six SATA general purpose input signals and can be implemented as interlock switch inputs corresponding to a given SATA port.

- When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
- If mechanical presence switches will not be used on the platform, the signals can be used as GPIOs.

#### 17.2.2.2 DEVSLP Implementation

DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.

- When **high**, DEVSLP requests the SATA device to enter into the DEVSLP power state.
- When **low**, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.
- Align DEVSLP pin assignment 1 host pin to 1 device pin as follows:
  - SATA DEVSLP0 to DEVSLP Port0
  - SATA DEVSLP1 to DEVSLP Port1
  - SATA DEVSLP2 to DEVSLP Port2
  - SATA DEVSLP0 to DEVSLP Port3
  - SATA DEVSLP1 to DEVSLP Port4
  - SATA DEVSLP2 to DEVSLP Port5

***Note:*** 1 DEVSLP pin is required to support EACH DEVSLP enabled RAID storage device. (Example: 2 DEVSLP pins are required to support 2 DEVSLP RAID storage devices).

***Important!***

- DEVSLP is an open-drain pin on the PCH side and is not required external pull-up or pull-down. The PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- DEVSLP is supported in direct connect, mSATA/mPCIe, uSSD, M.2.

#### 17.2.2.3 SATALED# Implementation

The processor provides SATALED# to simplify the indication of SATA devices activity. SATALED# is not intended to source high current design implementation. Use current isolation circuitry for implementation beyond driving an LED activity indicator.

- The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.
- When **low**, SATALED# indicates activity on **any** SATA port.

## 17.3 SATA General Guidelines

### 17.3.1 General SATA Routing Guidelines

Refer to Chapter 2, "Stack-Up and PCB Considerations" for more information on common guidelines for HSIO routing.

Use the following general routing and placement guidelines when laying out a new design.

- **DO NOT** route SATA traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- **DO NOT** place stubs, test points, test vias on the route to minimize reflection. Utilize vias and connector pads as test points instead.
- **DO NOT** serpentine to match RX and TX traces; there is **NO** requirement to match RX and TX traces. In addition, **DO NOT** serpentine to meet minimum length guidelines on RX and TX traces.
- Recommend keeping SATA traces 20 mils from any vias on the motherboard whenever possible.

## 17.3.2 SATA Test Points and Probing

DO NOT place stubs, test points, test vias on the route to minimize reflection. Use vias and connector pads as test points instead.

## 17.3.3 SATA Additional Guidelines

### 17.3.3.1 SATA Link Power Management

Intel recommends the following design options to further reduce SATA link power consumption while supporting hot plug on SATA ports. In general, Intel recommends connecting the Mechanical Present detect pin (SATAGP) to topologies supporting SATA slimline connectors, SATA repeaters, and docking connectors in order to detect hot plug events. The usage of the SATAGP pins must correspond to the port that has the mechanical presence switch implemented (such as, the processor SATA port 0 will use SATAGP0 as the mechanical presence pin).

The following figure is an example of how to implement mechanical presence switches on the motherboard. The exact implementation is dependent upon the platform support and implementation.

**Zero Power SATA ODD Guidelines**

Zero Power SATA ODD support provides the capability for host software to power off an idle slimline connector-based SATA optical device with a platform. This feature uses the capabilities of the Manufacturing Diagnostic/Device Attention (MD/DA) pin and the Device Present pin in the SATA slimline connector as defined in the *Serial ATA Specification Revision 3.2*.

The Manufacturing Diagnostic / Device Attention (MD/DA) pin provides the capability for the device to notify the PCH in the processor that the device requires service when power has been removed from the drive. This allows the host system to power off the device and be notified when the device requires attention. Typically, this would be when the front panel button is pressed on a tray-load device or when media is inserted in a slot load optical device. To allow proper voltage bias to the device controller, the processor is required to pull-up the MD/DA pin to 3.3 volts using a 10 kΩ pull-up resistor. The Device Attention pin shall be connected to a level-triggered GPIO Input Pin. This GPIO must be capable of generating an SCI event. An additional GPIO is required to control the circuitry that determines the power state of the device. The implementation of this circuitry is the responsibility of the system designer.

The Device Present pin is routed to the respective SATAGP[2:0][5:0] pin (SATAnGP to SATA Portn where n = SATA Port#) that is connected to the AHCI mechanical presence switch of the SATA port. This notifies the host software that the device has been inserted or removed. If the optical device is not physically removable in the system, this pin does not need to be connected. The 3.3V MD/DA pin must be routed according to the SATA Specification.

The 3.3 V MD/DA pin must be asserted by the host before the 5V rail. This ensures that no manufacturing information is sent from the device.

***Note:*** Support of this feature requires BIOS and AHCI driver support. Refer to the BIOS Specification and/or the ZPODD White paper for additional details.

**Figure 17-1. Zero Power ODD Timing Diagram**

**Figure 17-2. Zero Power ODD - Chipset GPIO Implementation Example**

**Figure 17-3. Zero Power ODD - Embedded Controller GPIO Implementation Example**

## 17.3.4 SATA Disabling and Termination Guidelines

If a SATA port(s) is not implemented, then SATA[x]_RXP/RXN and SATA[x]_TXP/TXN signals may be left unconnected; where 'x' is the port number left as no connect.

SATA compensation circuit is code share with PCIE_RCOMPP/N differential pair.

Refer to **Chapter 8, "Processor - PCI Express* Design Guidelines"**

# 17.4 SATA Topologies and Guidelines

## 17.4.1 mSATA/Direct Connect

The mSATA/direct connect and M.2 topology supports the routing of a SATA port directly to a connector where the SATA device will be connected directly, without any cable in between.

***Note:*** For AC Cap implementation if PCIe/SATA muxed port is utilized for these topologies, refer to the AC Capacitor Guidelines in Table 17-5 below for more details.

### Figure 17-4. mSATA and Direct Connect Topology

### Table 17-4. Routing Guidelines for mSATA and Direct Connect Topology

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | Gen1/2 Routing | Gen 3 Routing |
|---|---|---|---|---|---|
| Reference Plane | BO, M1, M2, M3 | MS/SL/DSL | NA | GND | GND |
| Breakout Max Length | BO | MS/SL/DSL | mm (mils) | 15.2 (598.42) | 15.2 (598.42) |
| Post AC capacitor main route length | M3 | MS | mm (mils) | 10 (393.7) | 10 (393.7) |
| Total Motherboard Length Range | BO+M1+M2 +M3 | BO: MS/SL/DSL<br>M1: MS/SL/DSL<br>M2: MS<br>M3: MS | mm (mils) | 2 Vias: 50.8 (2000) to 203.2 (8000) (Type 4 PCB)<br>3 Vias: 50.8 (2000) to 190.5 (7500) (Type 3 PCB) | 2 Vias: 50.8 (2000) to 203.2 (8000)<br>3 Vias: 50.8 (2000) to 178 (7007.87) |
| Max Via Count | 2 or 3 (assuming add-in card having 1 via) | | | | |

***Notes:***
1. AC capacitor value: 10nF
2. Refer to Chapter 2, "Stack-Up and PCB Considerations" for specific PCB type routing guide.
3. An initial breakout segment of 4mm (157.48 mils) in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm (4 -6 mils) is allowed. The total breakout length is still 15.2mm (598.42 mils)
4. Use a non-interleaved breakout to isolate Tx and Rx.
5. Within the same layer, the mismatch between P and N of a differential pair should be +/- 0.254mm (10 mils), and the total length mismatch should be +/- 0.381mm (15 mils).
6. Continuous GND referencing is preferred. Power plane referencing is allowed. Refer to Chapter 3.5.2 / Power Referencing tab for guidelines and limitations

### 17.4.1.1 AC Capacitor General Guidelines SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports. When SATA and PCIe are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

**Table 17-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values**

| Condition | PCI Express* Gen 2 Only | PCI Express* Gen 3 Only | SATA Only | PCI Express* Gen 2/ SATA | PCI Express* Gen 3/ SATA |
|---|---|---|---|---|---|
| Processor Tx | 100 nF | 220 nF | 10 nF | 100 nF | 220 nF |
| Processor Rx | None | None | 10 nF[1] | None[2] | None[3] |

***Notes:***
1. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
2. For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
3. For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Use a non-interleaved breakout to isolate Tx and Rx.

### 17.4.1.2 Flexible I/O PCIe/SATA Port Selection

The HSIO lanes that have PCIe/SATA port muxing can be statically configured to SATA or PCIe by soft straps.

***Note:*** Refer to the SPI Programming Guide documentation for details on how to configure the HSIO ports via soft straps.

In addition to static configuration via soft straps, the HSIO lanes that have PCIe/SATA port muxing can be configured dynamically to SATA or PCIe via SATAXPCIE signaling to support implementation like SATA Express, M.2 and mSATA, where the port configuration is selected by the type of the add-in card that is used.

Refer to the SPI Programming Guide documentation for details on how to configure the SATAXPCIE for SATA/PCIe port selection

## 17.4.2 SATA Direct Connect with Internal Cable Topology

The direct connect with internal cable topology supports the routing of a SATA Gen 1, Gen 2, and Gen 3 ports directly to a connector using an internal connector.

### 17.4.2.1 Internal Cable Guidelines

The following table provides the guidelines for the internal cable depending on the board trace lengths.

**Table 17-6. Internal Connector and Cable Specification**

| Total Trace Length includes Motherboard and Daughter Card Length (mm or mils) | | Internal Cable Assembly Insertion Loss Recommendation up to 3 GHz |
|---|---|---|
| 50.8 mm | 2000 mils | ≤4.3 dB |
| 76.2 mm | 3000 mils | ≤3.6 dB |
| 101.6 mm | 4000 mils | ≤3.0 dB |
| 127 mm | 5000 mils | ≤2.3 dB |
| 152.4 mm | 6000 mils | ≤2.0 dB |

There are two implementations, with or without a daughter card, as shown in the two following figures.

### 17.4.2.2 Without daughter card and with Internal cable

**Figure 17-5. SATA Direct Connect with Internal Cable Topology**

**Table 17-7. SATA Direct Connect without daughter card and with Internal Cable Guidelines**

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | Routing Guidelines |
|---|---|---|---|---|
| Reference Plane | BO, M1, M2, M3 | MS/SL/DSL | NA | GND |
| Breakout Max Length | BO | MS/SL/DSL | mm (mils) | 15.2 (598.42) |
| Post AC capacitor main route length | M3 | MS | mm (mils) | 10 (393.7) |
| Total Motherboard Length Range | BO+M1+M2+M3 | BO: MS/SL/DSL<br>M1: MS/SL/DSL<br>M2: MS<br>M3: MS | mm (mils) | 50.8 (2000)<br>to<br>152 (5984.25) |
| Max Via Count | 2 | | | |

***Notes:***
1. AC capacitor value: 10nF
2. Refer to Chapter 2, "Stack-Up and PCB Considerations" for specific PCB type routing guide.
3. An initial breakout segment of 4mm (157.48 mils) in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm (4 -6 mils) is allowed. The total breakout length is still 15.2mm (598.42 mils)
4. Use a non-interleaved breakout to isolate Tx and Rx.
5. Within the same layer, the mismatch between P and N of a differential pair should be +/- 0.254mm (10 mils), and the total length mismatch should be +/- 0.381mm (15 mils).
6. Continuous GND referencing is preferred. Power plane referencing is allowed. Refer to Chapter 3.5.2 / Power Referencing tab for guidelines and limitations

### 17.4.2.3 With daughter card and with internal cable

**Figure 17-6. SATA Direct Connect with Internal Cable**

**Table 17-8. SATA Direct Connect with Internal Cable Guidelines**

| Parameter | Segment | Stack-up (MS/SL/DSL) | Units | Routing Guidelines |
|---|---|---|---|---|
| Reference Plane | BO, M1, M2, M3 | MS/SL/DSL | NA | GND |
| Breakout Max Length | BO | MS/SL/DSL | mm (mils) | 15.2 (598.42) |
| Post AC capacitor main route length | M3 | MS | mm (mils) | 10 (393.7) |
| Total Motherboard Length Range | BO+M1+M2+M3 | BO: MS/SL/DSL<br>M1: MS/SL/DSL<br>M2: MS<br>M3: MS | mm (mils) | 50.8 (2000)<br>to<br>152 (5984.25) |
| Max Via Count | 2 | | | |

***Notes:***
1. AC capacitor value: 10nF
2. Refer to Chapter 2, "Stack-Up and PCB Considerations" for specific PCB type routing guide.
3. An initial breakout segment of 4mm (157.48 mils) in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm (4 -6 mils) is allowed. The total breakout length is still 15.2mm (598.42 mils)
4. Use a non-interleaved breakout to isolate Tx and Rx.
5. Within the same layer, the mismatch between P and N of a differential pair should be +/- 0.254mm (10 mils), and the total length mismatch should be +/- 0.381mm (15 mils).
6. Continuous GND referencing is preferred. Power plane referencing is allowed. Refer to Chapter 3.5.2 / Power Referencing tab for guidelines and limitations

## 17.4.3 Internal SATA (Cable Connect) Topology

### Figure 17-7. Internal SATA Topology

### Table 17-9. Routing Guidelines for Internal SATA Topology

| Parameter | Segment | Stack-up (MS/ SL/DSL) | Units | Routing Guidelines |
|---|---|---|---|---|
| Reference Plane | BO, M1, M2, M3 | MS/SL/DSL | NA | GND |
| Breakout Max Length | BO | MS/SL/DSL | mm (mils) | 15.2 (598.42) |
| Post AC capacitor main route length | M3 | MS | mm (mils) | 12.7 (500) |
| Total Motherboard Length | BO+M1+M2+M3 | BO: MS/SL/DSL<br>M1: MS/SL/DSL<br>M2: MS/SL/DSL<br>M3: MS | mm (mils) | 50.8 (2000)<br>to<br>152 (5984.25) |
| Max Via Count | 2 | | | |

***Notes:***
1. AC capacitor value: 10nF
2. Refer to Chapter 2, "Stack-Up and PCB Considerations" for specific PCB type routing guide.
3. An initial breakout segment of 4mm (157.48 mils) in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm (4 -6 mils) is allowed. The total breakout length is still 15.2mm (598.42 mils)
4. Use a non-interleaved breakout to isolate Tx and Rx.
5. Within the same layer, the mismatch between P and N of a differential pair should be +/- 0.254mm (10 mils), and the total length mismatch should be +/- 0.381mm (15 mils).
6. Continuous GND referencing is preferred. Power plane referencing is allowed. Refer to Chapter 3.5.2 / Power Referencing tab for guidelines and limitations

## 17.5 Compliance Requirements

Ensure that the SATA system design is validated and tested for compliance to the SATA specifications. This can be done by executing the Signal Quality Test or by having the system tested by a SATA-IO Certified Test Laboratory. Refer to www.sata-io.org for a list of approved facilities.

§ §

# 18 Universal Serial Bus USB 3.1 Design Guidelines

Platform Controller Hub (PCH) has an xHCI controller and device controller implemented in it.

**Table 18-2. USB 3.1 Reference Documents**

| Title | Document Number / Location |
|---|---|
| USB 3.1 Repeater Integration Technical White Paper Rev 0.9 | 571574 |
| Cannon Lake PCH-H I/O Buffer Information Specification IBIS Models | 572079 |

**Table 18-3. USB 3.1 Compliance Documents**

| Title | Document Number / Location |
|---|---|
| USB 3.1 Specification | www.usb.org |
| USB 3.1 Front Panel Cable and Connector Implementation | http://www.usb.org/developers/docs/whitepapers/USB3p1_Front_Panel_CabCon_Implment_Doc_Rev1p0.pdf |
| USB 3.1 Internal Cable and Connector Implementation | 571591 |

## 18.1 USB 3.1 Signal Descriptions

### 18.1.1 Signal Groups

The following table provides a list of the USB 3 interface signals and signal type.

**Table 18-4. USB 3.1 Gen2 Interface Signals**

| Group | Signal Name |
|---|---|
| USB 3 Differential Transmit Data Pairs | USB31_TXP<br>USB31_TXN |
| USB 3 Differential Receive Data Pairs: | USB31_RXP<br>USB31_RXN |
| OverCurrent | USB2_OC# |

### 18.1.2 Overcurrent Protection

The overcurrent signals require a pull-up to the 3.3V Suspend Rail with 8.2–10 KΩ resistor. Additional overcurrent guidance can be found in **Section 19.5, "Overcurrent Protection"**.

## 18.1.3 USB 3.1 Topology Guidelines

The guidelines provided in this chapter apply to both Type 3 and HDI boards.

### 18.1.3.1 USB 3.1 Back Panel Topology

This Topology is defined to be USB 3.1 signals routed directly to a standard and micro-sized Type-A and Type-B connector. Non-interleaved breakout (B0) is required to mitigate concerns on near-end crosstalk. The main route supports interleaved routing and non-interleaved routing for maximum flexibility. However, breakout must be routed using a non-interleaved scheme. Microstrip main route is also recommended albeit with shorter length than Stripline or Dual-Stripline. Routing recommendation is stated in the following table. For additional information refer Chapter 2, "Stack-Up and PCB Considerations".

These guidelines were developed assuming that the USB 3.1 Device has capacitors on its Tx SS lines. A single 0 Ω resistor per signal trace should be available to be used to bypass the CMC content if it is proven that there is no EMI risk on USB3.1 Tx/Rx signals. However, the 0 Ω resistor must be placed near the connector at the same recommended location as the CMC.

**Figure 18-1. USB 3.1 Gen1/2 Back Panel Topology**

**Table 18-5. USB 3.1 Gen1/2 Back Panel Routing Guidelines (Sheet 1 of 2)**

| | Segment | Tline Type | Reference | Via Count | Max Length, Segment (mm) | Max Length, Total (mm) | Maximum Length, Segment (mils) | Max Length, Total (mils) |
|---|---|---|---|---|---|---|---|---|
| **USB3.1 Gen1** | BO | MS/SL/DSL | VSS | 1 | 15.2 | 228.6 | 600 | 9000 |
| | M1 | SL/DSL | VSS | 1 | 188.0 | | 7400 | |
| | M2+M3+M4 or M6 | MS | VSS | 0 | 10.2 | | 400 | |
| | M5 or M7 | MS | VSS | 0 | 15.2 | | 600 | |

### Table 18-5. USB 3.1 Gen1/2 Back Panel Routing Guidelines (Sheet 2 of 2)

| | Segment | Tline Type | Reference | Via Count | Max Length, Segment (mm) | Max Length, Total (mm) | Maximum Length, Segment (mils) | Max Length, Total (mils) |
|---|---|---|---|---|---|---|---|---|
| ***Notes:***<br>1. Max total length is 228.6 mm (9000 mils) for SL/DSL and 177.8 mm (7000 mils) for MS<br>2. Max M1 length is 188.0 mm (7400) for SL/DSL and 137.2 mm (5400 mils) for MS.<br>3. In order to assure adequate EMI and ESD protection, a ESD protection diode should be implemented on each USB data line. | | | | | | | | |
| **USB3.1 Gen2** | BO | MS/SL/DSL | VSS | 1 | 10.2 | 127.0 | 400 | 5000 |
| | M1 | MS/SL/DSL | VSS | 1 | 96.5 | | 3800 | |
| | M2+M3+M4 or M6 | MS | VSS | 0 | 10.2 | | 400 | |
| | M5 or M7 | MS | VSS | 0 | 10.2 | | 400 | |
| ***Note:***<br>1. Minimum PCB length is 50.8 mm (2000 mils).<br>2. In order to assure adequate EMI and ESD protection, a ESD protection diode should be implemented on each USB data line. | | | | | | | | |

### 18.1.3.2 USB 3.1 Front Panel Topology

This topology supports a low profile internal connector, internal cable solution. Non-interleaved breakout is required to mitigate concerns on near-end crosstalk. However the main route supports interleaved routing and non-interleaved routing for maximum flexibility.

For signal integrity considerations it is recommended that the USB 3.1 signals are routed to the A-connector via bottom-entry.

***Note:*** It is recommended that the internal connectors and cables adhere to the *High Speed Internal Connector and Cable Specification*.

A single 0 Ω resistor per signal trace should be available to be used to bypass the CMC content if it is proven that there is no EMI risk on USB3.1 Tx/Rx signals. However, this component must be placed near the connector at the same recommended location as the CMC.

**Figure 18-2. USB 3.1 Gen1/2 Internal Cable Topology**

### Table 18-6. USB 3.1 Gen1/2 Internal Cable Topology Routing Guidelines

| | Segment | Tline Type | Reference | Via Count | Max Length, Segment (mm) | Max Length, Total (mm) | Maximum Length, Segment (mils) | Max Length, Total (mils) |
|---|---|---|---|---|---|---|---|---|
| **USB3.1 Gen1** | BO | MS/SL/DSL | VSS | 1 | 15.2 | 127.0 | 600 | 5000 |
| | M1 | SL/DSL | VSS | 1 | 106.7 | | 4200 | |
| | M2 | MS | VSS | 0 | 5.1 | | 200 | |
| | M3+M4+M5+M6 or M7+M8 | MS | VSS | 0 | 50.8 | 50.8 | 2000 | 2000 |
| ***Notes:***<br>1. Max total length on main board (BO+M1+M2) is 127.0 mm (5000 mils) for SL/DSL and 101.6 mm (4000 mils) for MS<br>2. Max M1 length is 106.7 mm (4200 mils) for SL/DSL and 81.3 mm (3200 mils) for MS.<br>3. In order to assure adequate EMI and ESD protection, a ESD protection diode should be implemented on each USB data line. | | | | | | | | |
| **USB3.1 Gen2** | BO | MS/SL/DSL | VSS | 1 | 10.2 | 63.5 | 400 | 2500 |
| | M1 | MS/SL/DSL | VSS | 1 | 48.3 | | 1900 | |
| | M2 | MS | VSS | 0 | 5.1 | | 200 | |
| | M3+M4+M5+M6 or M7+M8 | MS | VSS | 0 | 12.5 | 12.5 | 500 | 500 |
| ***Note:***<br>1. Minimum main board length is 25.4 mm (1000 mils)<br>2. In order to assure adequate EMI and ESD protection, a ESD protection diode should be implemented on each USB data line. | | | | | | | | |

### Table 18-7. USB3.1 Gen1 Internal Cable Differential Insertion Loss Requirements

| Motherboard Total Trace Length [SL/DSL;MS] (Inch) | Daughter Card Trace Length (Inch) | Internal Cable Assembly Insertion Loss Recommendation up to 2.5GHz | Internal Cable Assembly Insertion Loss Recommendation up to 5GHz | Internal Cable Assembly Insertion Loss Recommendation up to 7.5GHz |
|---|---|---|---|---|
| 5;4 | 2 | 2.0dB | 3.5dB | 4.8dB |
| 4.5;3.5 | 2 | 2.5dB | 4dB | 6dB |
| 4;3 | 2 | 3.0dB | 5dB | 7dB |
| 3;2 | 2 | 3.5dB | 6dB | 8.5dB |
| 2;1 | 2 | 4.0dB | 7dB | 9.5dB |

### 18.1.3.3 USB 3.1 Re-driver Guidelines

This section provides the necessary guidelines for customers who intend to use re-driver in one of the aforementioned USB 3.1 topologies. Terms such as “re-timer”, “repeater”, and “re-driver” can be used to describe similar devices: active components used to amplify a signal passing through them. The definitions below are not exhaustive and are only applied in this document in the context of serial links.

**Re-driver:** An active component, which may have receiver equalization, transmitter de-emphasis, analog signal amplification, etc., to better "shape" the signals passing through it. Re-drivers do not perform retiming (i.e., the device does not implement any interface protocol and no re-sampling is performed). Because it changes the analog

behavior of the incoming signals, the propagation of jitter, noise and other analog effects from one connected channel to the other must be considered. Note that a re-driver's performance is implementation specific in terms of loss compensation.

**Re-timer:** An active component compliant to the updated Appendix E of the USB 3.1 specification that performs re-sampling of the incoming signal and re-transmitting the recovered signal per specification. A re-timer is protocol aware and compliant to link power management. Note that the delay issue with a re-timer in Gen 1 operation is solved if the implementation follows the updated Appendix E of USB 3.1 Specification document.

For additional details and recommendations regarding the implementation of re-driver in USB3.1 Gen2 channel, refer to the following documents.

| Title | Document Number |
|---|---|
| Intel Channel Checker (ICC) for Client Re-driver CQC Analysis | 556174 |

**Figure 18-3. USB 3.1 Gen1/2 Re-driver Topology**

## Table 18-8. USB 3.1 Gen1/2 Re-Driver Topology Routing Guidelines

| | Segment | Tline Type | Reference | Via Count | Max Length, Segment (mm) | Max Length, Total (mm) |
|---|---|---|---|---|---|---|
| **USB3.1 Gen1** | BO | MS/SL/DSL | VSS | 1 | 12.7 | 266.7 |
| | M1 | MS/SL/DSL | VSS | 1 | 241.3 | |
| | M2+M3 | MS | VSS | 0 | 12.7 | |
| | M4+M5 or M9 | MS | VSS | 1 | 7.6 | 25.4 |
| | M6+M7 or M10 | MS | VSS | 0 | 7.6 | |
| | M8 or M11 | MS | VSS | 0 | 10.2 | |
| ***Notes:*** 1. Minimum length: Pre-channel is 152.4 mm (6000 mils) & post-channel is 12.7 mm (500 mils) 2. In order to assure adequate EMI and ESD protection, a ESD protection diode should be implemented on each USB data line. | | | | | | |
| **USB3.1 Gen2** | BO | MS/SL/DSL | VSS | 1 | Note1* | Note1* |
| | M1 | MS/SL/DSL | VSS | 1 | Note1* | |
| | M2+M3 | MS | VSS | 0 | Note1* | |
| | M4+M5 or M9 | MS | VSS | 1 | 7.6 | 25.4 |
| | M6+M7 or M10 | MS | VSS | 0 | 7.6 | |
| | M8 or M11 | MS | VSS | 0 | 10.2 | |
| ***Note:*** 1. Minimum length: Pre-channel is 152.4 mm (6000 mils) & post-channel is 12.7 mm (500 mils) 2. In order to assure adequate EMI and ESD protection, a ESD protection diode should be implemented on each USB data line. | | | | | | |

***Notes:*** **Important Guidelines on Repeater/Active MUX topologies**

1. *Max pre-channel length at USB3.1 Gen 2 speeds (10Gb/s) depends on what the specific re-driver based active mux/redriver selected can compensate for when used in conjunction with Intel PCH. Work with repeater vendor to ensure that the component being utilized will provide adequate signal integrity at the PCH.
   a. OEMs are recommended to use the CRB/RVP topologies as reference for pre-channel lengths which are achievable and validated by Intel.
2. In addition, it is recommended to refer to the white paper pertaining to the repeater integration (USB 3.1 Repeater Integration Technical White Paper Rev 0.9 with RDC#571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
3. It is recommended that OEMs use active mux/retimer/redriver parts from 3rd party vendors which meet below requirements to avoid Electrical Over Stress (EOS) on USB3.1 receiver lines:
   a. During power on and receive detect phase, recommended transmitter common mode voltage (Vcm) and impedance values:
   - If (Vcm <= 1.2V), Repeater Impedance >= 1K ohm **ELSE**
   - (Vcm+Rx.detect pulse amplitude <= 2.2V) **AND** (Repeater Impedance >= 4.5K ohm).

### 18.1.3.4 USB 3.1 Re-timer Guidelines

**Figure 18-4. USB 3.1 Gen2 Re-timer Topology**

**Table 18-9. USB 3.1 Gen2 Re-timer Topology Routing Guidelines**

| Segment | Tline Type | Reference | Via Count | Max Length, Segment (mm) | Max Length, Total (mm) |
|---|---|---|---|---|---|
| BO | MS/SL/DSL | VSS | 1 | 10.2 | 381 |
| M1+M2 | MS/SL/DSL | VSS | 2 | 358.1 | |
| M3+M4 | MS | VSS | 0 | 12.7 | |
| M5+M6 | MS/SL/DSL | VSS | 2 | 101.6 | 127 |
| M7+M8+M9 or M11 | MS | VSS | 0 | 15.2 | |
| M10 or M12 | MS | VSS | 0 | 10.2 | |

***Note:***

1. Minimum length: Pre-channel & post-channel is 12.7 mm (500 mils)

2. In order to assure adequate EMI and ESD protection, a ESD protection diode should be implemented on each USB data line.

***Notes:***

**Important Guidelines on Repeater/Active MUX topologies**

1. ReferRefer to the white paper pertaining to the repeater integration (USB 3.1 Repeater Integration Technical White Paper Rev 0.9 with RDC#571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
2. It is recommended that OEMs use active mux/retimer/redriver parts from 3rd party vendors which meet below requirements to avoid Electrical Over Stress (EOS) on USB3.1 receiver lines:
   a. During power on and receive detect phase, recommended transmitter common mode voltage (Vcm) and impedance values:
   - If (Vcm <= 1.2V), Repeater Impedance >= 1K ohm **ELSE**
   - (Vcm+Rx.detect pulse amplitude <= 2.2V) **AND** (Repeater Impedance >= 4.5K ohm).

## 18.1.4 USB 3.1 Specific Topology Guidelines

***Note:*** In order to assure adequate EMI and ESD protection, a ESD protection diode should be implemented on each USB data line.

### 18.1.4.1 USB 3.1 Detachable Docking Topology

**Figure 18-5. USB 3.1 Gen1 Detachable Docking Topology**

**Table 18-10. USB 3.1 Gen1 Detachable Docking Topology Routing Guidelines**

| Segment | Tline Type | Reference | Via Count | Max Length, Segment (mm) | Max Length, Total (mm) |
|---|---|---|---|---|---|
| BO | MS/SL/DSL | VSS | 1 | 2.5 | 165.1 |
| M1 | SL/DSL | VSS | 1 | 45.7 | |
| M2+M3 | MS | VSS | 0 | 5.1 | |
| M4 | SL/DSL | VSS | 0 | 11.7 | |
| M5 | SL/DSL | VSS | 0 | 23.9 | |
| M6 | SL/DSL | VSS | 0 | 76.2 | |

***Notes:***

| Segment | Minimum Length |
|---|---|
| M1 | 7.6 mm (300 mils) |
| M5 | 11.7 mm (460 mils) |
| M6 | 24.9 mm (980 mils) |
| Total Length | 63.5 mm (2500 mil) |

### Table 18-11. Trade off of Internal Cable Loss on Margin

| Main Board Total Length (Inches) | Internal Cable Assembly Insertion Loss on Motherboard | Internal Cable Assembly Insertion Loss on Docking |
|---|---|---|
| 2 | 4.0dB;4.5dB | 4.5dB;4.0dB |
| 1.5 | 4.5dB;5.0dB | 5.0dB;4.5dB |
| 1 | 5.0dB;5.5dB | 5.5dB;5.0dB |

## 18.1.4.2 USB 3.1 Traditional Docking Topology

### Figure 18-6. USB 3.1 Gen1 Traditional Docking Topology

### Table 18-12. USB 3.1 Gen1 Traditional Docking Topology Routing Guidelines

| Segment | Tline Type | Reference | Via Count | Max Length, Segment (mm) | Max Length, Total (mm) |
|---|---|---|---|---|---|
| BO | MS/SL/DSL | VSS | 1 | 15.2 | 355.6 |
| M1+M2+M3+M4 | SL/DSL | VSS | 3 | 238.8 | |
| M5+M6 | MS/SL/DSL | VSS | 2 | 88.9 | |
| M7+M8 | MS | VSS | 0 | 12.7 | |

***Notes:***

| Microstrip routing is supported for segments M1+M2+M3+M4 at reduced max length compared to SL/DSL | Max Length |
|---|---|
| M1+M2+M3+M4 | 188.0 mm (7400 mils) |
| Total Length | 304.8 mm (12000 mils) |

### 18.1.4.3 USB 3.1 M.2 Topology

**Figure 18-7. USB 3.1 Gen1 M.2 Topology**

**Table 18-13. USB3.1 Gen1 M.2 Topology**

| Segment | Tline Type | Reference | Via Count | Max Length, Segment (mm) | Max Length, Total (mm) |
|---|---|---|---|---|---|
| BO | MS/SL/DSL | VSS | 1 | 15.2 | 228.6 |
| M1 | SL/DSL | VSS | 1 | 188 | |
| M2+M3+M4 or M6 | MS | VSS | 0 | 10.2 | |
| M5 or M7 | MS | VSS | 0 | 15.2 | |

***Notes:***

| Microstrip routing is supported for segment M1 at reduced max length compared to SL/DSL | Max Length |
|---|---|
| M1 | 137.2 mm (5400 mils) |
| Total Length | 177.8 mm (7000 mils) |

## 18.1.5 USB 3.1 General Guidelines

- Trace length matching requirement - keep both “within layer” mismatches and “total length” mismatches within 0.127mm, especially for Gen2 signaling. For Gen1, “within layer” max mismatch is 0.254mm and “total length” max mismatch is 0.125mm.
- Breakout scheme: TX and RX breakout at different layers (non-interleaved scheme), for better crosstalk shielding performance
- Breakout length and spacing: An initial breakout segment of 4mm (157.48 mils) in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm (4 -6 mils) is allowed. But the total breakout length should still be within the length defined for each topology.
- Trace Geometry: For Gen2, it is recommended to use 80-ohm trace geometry (with larger trace width), primarily to address routing insertion loss at 10Gbps. For Gen1, it is recommended to use 85-ohm trace geometry (narrower trace width), for PCB

real estate saving. It is worth noting that Gen2 with 80-ohm trace geometry is fully functional and backward compatible with Gen1 5Gbps signaling.

- Reference plane: Continuous Ground
- Via stub: For USB3.1 gen 2, via stub length < 15mils
- Via anti-pad: Oval anti-pad size of 40mils is required for better impedance matching.

- AC capacitor value: 100nF nominal (75-265nF range)
- CMC: CMC is not needed for Rx lanes
- ESD: ESD may/may not be required depending on the 3rd party's device. On the removal of discrete ESD, there are two requirements have to be met:
  a) Mux/Re-driver can handle the ESD at least 8kV
  b) Mux/Re-driver to be placed near to USB-C connector (< 1")
  Refer to 3rd party component specification.
- Distance between coils should be greater than 12 mils (recommended is 15 mils).

## 18.1.6 USB 3.1 Optimization Guidelines

## 18.1.7 USB Connector/Receptacle Recommendations

- Proper connector choice is critical to ensure adequate USB signal quality.
- Empirical data has shown that quad-stack USB and DisplayPort*/USB stack connectors may cause Signal quality degradation.
- Proper selection of a motherboard mating connector with USB 3.1 Gen2 support is important to ensure signal quality is not adversely affected due to a poor connector design.
- Refer to usb.org for a list of tested connectors and receptacles.

### 18.1.7.1 A-Connector Recommendations

- Signals should be launched into the connector from the bottom of the board to minimize the through-hole stub effect. The connector footprint shall have the following through-hole dimensions: 28 mil finished hole, 43 mil pad, and 40 mil anti-pad

### 18.1.7.2 USB 3.1 Mobile Internal Connector

- It is possible to define the Mobile internal connector pin list based on individual needs. However, an example connector pin list for 2-port USB3 internal cable connection is shown in the following table.

**Table 18-14. Example of Mobile Internal Connector Pin Assignment and Description for Two-Port USB 3.1 Gen2***

| Pin Number | Signal | Description |
|---|---|---|
| 1 | RSVD | Reserved pin |
| 2 | Vbus | 5 V bus power |
| 3 | Vbus | 5 V bus power |
| 4 | Vbus | 5 V bus power |
| 5 | USB2P_1 | USB2 Port 1 D+ |
| 6 | USB2N_1 | USB2 Port 1 D- |
| 7 | PWR_GND | Power GND return |
| 8 | USB2P_2 | USB2 Port 2 D+ |
| 9 | USB2N_2 | USB2 Port 2 D- |
| 10 | PWR_GND | Power GND return |
| 11 | USB3_1_TXP | USB3 Port 2 SuperSpeed Tx+ |
| 12 | USB3_1_TXN | USB3 Port 2 Super Speed Tx- |
| 13 | SIG_GND | Signal GND return |
| 14 | USB3_1_RXP | USB3 Port 2 SuperSpeed Rx+ |
| 15 | USB3_1_RXN | USB3 Port 2 Super Speed Rx- |
| 16 | SIG_GND | Signal GND return |
| 17 | USB3_2_TXP | USB3 Port 2 SuperSpeed Tx+ |
| 18 | USB3_2_TXN | USB3 Port 2 Super Speed Tx- |
| 19 | SIG_GND | Signal GND return |
| 20 | USB3_2_RXP | USB3 Port 2 SuperSpeed Rx+ |
| 21 | USB3_2_RXN | USB3 Port 2 SuperSpeed Rx- |
| 22 | SIG_GND | Signal GND return |

## 18.1.8 USB 3.1 Disabling and Termination Guidelines

- If some of the USB 3.1 port(s) are not implemented on the platform, USB3Tp/n [x] and USB3Rp/n [x] signals may be left unconnected, where 'x' is the port number left no connect.

### 18.1.8.1 Motherboard-down USB Devices

***Note:*** Intel recommends that USB 2.0 motherboard-down devices be routed to USB 2.0 connectors that are not paired with USB 3.1 signals to allow the USB 3.1 pairs to be used with SuperSpeed devices.

**Figure 18-8. Device-Down**

**Figure 18-9. Device-On-Module**

### 18.1.8.2 External End User Accessible Ports

Designers are recommended to provide a combination of USB 2.0 only ports and USB 3.1 ports for external use on their platforms to provide the greatest amount of flexibility for legacy device support.

### 18.1.8.3 USB Debug Port

The xHCI controller provides a debug port capability on all USB 3.1 ports.

§ §

# 19 Universal Serial Bus 2.0 Design Guidelines

Platform Controller Hub (PCH) has an xHCI controller and device controller implemented in it.

**Table 19-1. USB 2.0 Reference Documents**

| Title | Doc #/Location |
|---|---|
| Front Panel I/O Connectivity Design Guide | *http://www.formfactors.org/developer/specs/A2928604-005.pdf* |

**Table 19-2. USB 2.0 Compliancy Documents**

| Title | Doc #/Location |
|---|---|
| USB 2.0 Specification and Compliancy Requirements | *www.usb.org* |

## 19.1 USB 2.0 Signal Groups

**Table 19-3. USB 2.0 Signal Groups**

| Group | Signal Name | Description |
|---|---|---|
| DATA | USB2P<br>USB2N | Universal Serial Bus Port Differential Pairs. |
| OVERCURRENT | USB2_OC [7:0]# | Overcurrent Indicators |
| BIAS | USB2_COMP | Resistor Bias |
| ***Note:*** The supported connectors are Type A Dual Stack and Type A Single Stack. The connectors must meet the USB2.0 Connector Specification. | | |

## 19.2 USB2_COMP Topology

- The compensation input is used by the circuitry to determine, check and adjust the system buffer output strength and characteristic impedance over temperature, process and voltage variations. This is done comparing its buffer impedance against a standard reference resistor, RCOMP.

***Note:*** The USB2_COMP signals should be referenced to VSS, avoiding noisy or switching references. As board space allows, recommend to add a VSS shield at least 4 mils wide placed between USB2_COMP and adjacent IO

**Figure 19-1. USB2_COMP Connection**

## 19.3 USB2_COMP Routing Guidelines

**Table 19-4. USB2_COMP Routing Guidelines**

| Signal | Trace Width (W) and Isolation Spacing (S) | Resistor Value | Length |
|---|---|---|---|
| USB2_COMP | No hard value for trace width and isolation spacing as long as DCR is met<br>Though a baseline of using a 50Ω single ended channel is recommended.<br>**Note**: must maintain low DC resistance routing (< 0.5Ω)<br>**Note**: a recommendation is to route the signal between 4-8 mils trace width for <1000 mils to meet DCR | 113 Ω ± 1% connected to GND | M1/M1' + M2<br><br>No hard value for max length as long as DCR is met. However it is recommended to route these signals to a maximum of <1000 mils |

***Note:***
1. Although there is no hard value for max topology length as long as the DC resistance routing spec is met, although it is recommended to route the USB2_COMP as short as possible; a general recommendation is to maintain a length of <1000 mils, which will make it easier to hit the targeted DCR.

## 19.4 USB2_COMP to Other Interfaces

If unable to implement a Vss shield for USB2_COMP, the minimum spacing between USB2_COMP and other traces should be at least 15 mils to provide proper isolation.

If Vss shielding is implemented, then the spacing guideline in the figure below should be followed:

**Figure 19-2. Spacing Guideline for USB2_COMP**

## 19.5 Overcurrent Protection

Platform Controller Hub (PCH) has implemented programmable USB Overcurrent signals. The 7 overcurrent pins are to be shared across the USB 2.0 ports and USB 3.1 ports. This allows the platform designer flexibility in routing of the OC pins and allows for unused pins to be configured as GPIOs.

When configured for overcurrent protection, each of the OC pins needs to be connected to an external over current protection circuit. It is important to choose the correct current rating for the thermistor. Each USB port may draw up to 500 mA. The overcurrent protection circuitry needs to be able to support at least 2 A to ensure proper functionality of USB compliant devices. However, if a fault device is plugged into the USB port, it should trigger an overcurrent when current is more than 500 mA is drawn. Designer must balance between optimum cost and protection level.

***Notes:***

1. When the current rating of the protection circuit has been decided, it is crucial to ensure that the overcurrent layout is designed to support the amount of current expected.
2. The overcurrent circuit should be designed to support up to 2 A, the overcurrent trace layout should be using a big fat trace or plane that can sustain at least 2 A.

***Warning:***

1. Failure to design the trace to support high current may cause the trace on motherboard to burn out and cause permanent damage to the protection circuit.
2. The overcurrent signals require a pull-up to the 3.3 V Suspend Rail with 8.2–10 KΩ resistor (refer figure below).

**Figure 19-3. Sample Overcurrent Protection Circuit**

The default configuration of the OC pins is in the table below. Each overcurrent pin is configured to protect one or more USB ports by setting bits in the U2OCM1 register in the xHCI controller.

***Note:*** It is the responsibility of system software (BIOS) to program the overcurrent registers of the given USB controller correctly and to make sure that each USB port is protected

by only one overcurrent pin. Operation with more than one overcurrent pin mapped to a port is undefined.

### 19.5.1 Overcurrent Pin Mapping

It is not recommended that customers map more than four USB ports to a single OC pin. Refer to PCH EDS for more details. Please follow PCH EDS on how to map OC pins to USB ports.

## 19.6 Integrated Bluetooth* and USB 2.0 Design Considerations

Due to the USB 2.0 port requirement for integrated Bluetooth* functionality with the Intel® Wireless-AC (CNVi) solution, Cannon Lake PCH-H USB 2.0 port # 14 will be available for the following platforms:

- **Coffee Lake H Platform**
  - USB 2.0 port 14 will be available for BT functionality only if Integrated Wireless solution is desired on CFL S Platform

If integrated Bluetooth* functionality is not desired, Cannon Lake PCH-H USB 2.0 port 14 may be used for USB functionality.

## 19.7 USB 2.0 Topology Guidelines

### 19.7.1 Back Panel/External Topology

The external topology refers to the routing of USB signals to a standard USB A connector. It is recommended that each USB data line be routed with a common mode choke and ESD protection.

**Figure 19-4. USB 2.0 External Topology**

### Table 19-5. USB 2.0 External Topology

| Parameter | Segment | Stackup (MS/SL/DSL) | Via Count | Reference | Routing Recommendations | |
|---|---|---|---|---|---|---|
| | | | | | Segment (mm) | Segment (mils) |
| Trace Length (MCP Breakout) Max | BO | MS /SL /DSL | 1 | VSS | 15.2 | 598.42 |
| Trace Length (Main route) Max | M1+M2 | MS /SL /DSL | 1 | VSS | N/A | N/A |
| Trace Length (To Choke) Max | M3 | MS | 1 | VSS | 3.8 | 149.6 |
| Trace Length (To ESD Diode) Max | M4 | MS | 0 | VSS | 3.8 | 149.6 |
| Trace Length (To Connector) Max | M5 | MS | 0 | | 12.7 | 500 |
| Total Motherboard Trace Length | BO+ M1 + M2 + M3 + M4 + M5 | | | NA | Max = 304.8<br>Min = 76.2 | Max = 12000<br>Min = 3000 |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 3.
3. Continuous GND referencing plane is preferred.
4. In order to assure adequate EMI and ESD protection, a common mode choke and ESD protection diode should be implemented on each USB data line.

## 19.7.2 On-The-Go Topology

The On-The-Go topology refers to the routing of USB signals to a uAB connector. It is recommended that each USB data line be routed with a common mode choke and ESD protection.

### Figure 19-5. USB On-The-Go Topology

### Table 19-6. USB 2.0 On-The-Go Topology

| Parameter | Segment | Stackup (MS/SL/DSL) | Via Count | Reference | Routing Recommendations | |
|---|---|---|---|---|---|---|
| | | | | | Segment (mm) | Segment (mils) |
| Trace Length (MCP Breakout) Max | BO | MS /SL /DSL | 1 | VSS | 15.2 | 598.42 |
| Trace Length (Main route) Max | M1+M2 | MS /SL /DSL | 1 | VSS | N/A | N/A |
| Trace Length (To Choke) Max | M3 | MS | 1 | VSS | 3.8 | 149.6 |
| Trace Length (To ESD Diode) Max | M4 | MS | 0 | VSS | 3.8 | 149.6 |
| Trace Length (To Connector) Max | M5 | MS | 0 | | 12.7 | 500 |
| Total Motherboard Trace Length | BO+ M1 + M2 + M3 + M4 + M5 | | | NA | Max = 304.8<br>Min = 76.2 | Max = 12000<br>Min = 3000 |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 3.
3. Continuous GND referencing plane is preferred.
4. In order to assure adequate EMI and ESD protection, a common mode choke and ESD protection diode should be implemented on each USB data line.

## 19.7.3 USB 2.0 with M.2 Topology

The USB 2.0 with M.2 topology refers to the routing of USB signals to a standard M.2 connector. It is recommended that each USB data line be routed with a common mode choke.

### Figure 19-6. USB 2.0 with M.2 Topology

**Table 19-7. USB 2.0 with M.2 Topology**

| Parameter | Segment | Stackup (MS/SL/DSL) | Via Count | Reference | Routing Recommendations | |
|---|---|---|---|---|---|---|
| | | | | | Segment (mm) | Segment (mils) |
| Trace Length (MCP Breakout) Max | BO | MS /SL /DSL | 1 | VSS | 15.2 | 598.42 |
| Trace Length (Main route) Max | M1+M2 | MS /SL /DSL | 1 | VSS | N/A | N/A |
| Trace Length (To Choke) Max | M3 | MS | 1 | VSS | 3.8 | 149.6 |
| Trace Length (To ESD Diode) Max | M4 | MS | 0 | VSS | 12.7 | 500 |
| Total Motherboard Trace Length | BO+ M1 + M2 + M3 + M4 | | | NA | Max = 304.8<br>Min = 76.2 | Max = 12000<br>Min = 3000 |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 3.
3. Continuous GND referencing plane is preferred

## 19.7.4 USB 2.0 Flex/Internal Cable Topology

This topology supports a low profile internal connector, internal cable solution and a daughter card. It is recommended that each USB data line be routed with a common mode choke and ESD diode.

***Note:*** The Internal cable guidelines will be defined using insertion loss budget rather than cable length where a recommended mobile internal cable has a loss of 2 dB @ 2.5 GHz.

**Figure 19-7. USB 2.0 Flex/Internal Cable Topology with Daughter Card**

Design Constraint: Differential vias, CMC, ESD and connector voiding (strongly recommended) are required to optimize impedance mismatch in the channel.

## Table 19-8. USB 2.0 Flex/Internal Cable Topology with Daughter Card

| Parameter | Segment | Stackup (MS/ SL/ DSL) | Reference | Via Count | Routing Recommendations | |
|---|---|---|---|---|---|---|
| | | | | | Segment (mm) | Segment (mils) |
| Trace Length (MCP Breakout) Max | BO | MS /SL / DSL | VSS | 1 | 15.2 | 598.42 |
| Trace Length (Main route) Max | M1+M2 | MS /SL / DSL | VSS | 1 | N/A | N/A |
| Trace Length (To Connector) Max | M3 | MS | VSS | 0 | 12.7 | 500 |
| Trace Length (To Choke) Max | M4 | MS | VSS | 0 | N/A | N/A |
| Trace Length (To Diode) Max | M5 | MS | VSS | 0 | 3.8 | 149.6 |
| Trace Length (To Ext. Connector) Max | M6 | MS | VSS | 0 | 12.7 | 500 |
| Total Motherboard Trace Length | BO+ M1 + M2 + M3 | NA | | | Max = 152.4<br>Min = 76.2 | Max = 6000<br>Min = 3000 |
| Total Daughter Card Trace Length | M4 +M5 + M6 | NA | | | Max = 50.8 | Max = 2000 |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 3.
3. Continuous GND referencing plane is preferred.
4. In order to assure adequate EMI and ESD protection, a common mode choke and ESD protection diode should be implemented on each USB data line.

## Table 19-9. USB 2.0 Internal Cable Differential Insertion Loss Restrictions

| Motherboard Total Trace Length (mm) | Motherboard Total Trace Length (Inches) | Maximum Daughter Card Trace Length (mm) | Motherboard Total Trace Length (Inches) | Internal Cable Assembly Insertion Loss Recommendation up to 2.5 GHz (dB) |
|---|---|---|---|---|
| 152.4 | 6.0 | 50.8 | 2 | 2.0 |
| 139.7 | 5.5 | 50.8 | 2 | 2.0 |
| 127 | 5.0 | 50.8 | 2 | 2.5 |
| 114.3 | 4.5 | 50.8 | 2 | 3.0 |
| 101.6 | 4.0 | 50.8 | 2 | 3.5 |
| 89 | 3.5 | 50.8 | 2 | 3.5 |
| 76.2 | 3.0 | 50.8 | 2 | 4.0 |

## Figure 19-8. USB 2.0 Flex/Internal Cable Topology without Daughter Card

## Table 19-10. USB 2.0 Flex/Internal Cable Topology without Daughter Card

| Parameter | Segment | Stackup (MS/ SL/ DSL) | Reference | Via Count | Routing Recommendations | |
|---|---|---|---|---|---|---|
| | | | | | mm | mils |
| Trace Length (MCP Breakout) Max | BO | MS /SL / DSL | VSS | 1 | 15.2 | 598.42 |
| Trace Length (Main route) Max | M1+M2 | MS /SL / DSL | VSS | 1 | N/A | N/A |
| Trace Length (To Connector) Max | M3 | MS | VSS | 1 | 3.8 | 149.6 |
| Trace Length (To Choke) Max | M4 | MS | VSS | 0 | 3.8 | 149.6 |
| Trace Length (To Diode) Max | M5 | MS | VSS | 0 | 12.7 | 500 |
| Total Motherboard Trace Length | BO+ M1 + M2 + M3+M4+M5 | NA | | | Max = 177.8<br>Min = 76.2 | Max = 7000<br>Min = 3000 |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 3.
3. Continuous GND referencing plane is preferred.
4. In order to assure adequate EMI and ESD protection, a common mode choke and ESD protection diode should be implemented on each USB data line.

## Table 19-11. USB 2.0 Internal Cable Differential Insertion Loss Restrictions (Sheet 1 of 2)

| Motherboard Total Trace Length (mm) | Motherboard Total Trace Length (Inches) | Internal Cable Assembly Insertion Loss Recommendation up to 2.5 GHz (dB) |
|---|---|---|
| 177.8 | 7.0 | 2.0 |

### Table 19-11. USB 2.0 Internal Cable Differential Insertion Loss Restrictions (Sheet 2 of 2)

| Motherboard Total Trace Length (mm) | Motherboard Total Trace Length (Inches) | Internal Cable Assembly Insertion Loss Recommendation up to 2.5 GHz (dB) |
|---|---|---|
| 165.1 | 6.5 | 2.0 |
| 152.4 | 6.0 | 2.5 |
| 139.7 | 5.5 | 3.0 |
| 127 | 5.0 | 3.5 |
| 114.3 | 4.5 | 3.5 |
| 101.6 | 4.0 | 4.0 |
| 76.2 | 3.0 | 4.0 |

## 19.7.5 USB 2.0 Device Down Topology

### Figure 19-9. USB 2.0 Device Down Topology

### Table 19-12. Routing Guidelines for USB 2.0 Device Down Topology

| Parameter | Segment | Stackup (MS/SL/ DSL) | Via Count | Reference | Routing Recommendations | |
|---|---|---|---|---|---|---|
| | | | | | Segment (mm) | Segment (mils) |
| Trace Length (MCP Breakout) Max | BO | MS /SL /DSL | 1 | VSS | 15.2 | 598.42 |
| Trace Length (Main route) Max | M1+M2 | MS /SL /DSL | 1 | VSS | N/A | N/A |
| Trace Length (To Choke) Max | M3 | MS | 1 | VSS | 3.8 | 149.6 |
| Trace Length (To ESD Diode) Max | M4 | MS | 0 | VSS | 12.7 | 500 |
| Total Motherboard Trace Length | BO+ M1 + M2 + M3 + M4 + M5 | | | NA | Max = 304.8<br>Min = 76.2 | Max = 12000<br>Min = 3000 |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 3.
3. Continuous GND referencing plane is preferred.
4. In order to assure adequate EMI and ESD protection, a common mode choke and ESD protection diode should be implemented on each USB data line.

## 19.7.6 USB 2.0 External / Back Panel with Power Switch / BC1.2 Charger Module / MUX Topology

The external topology refers to the routing of USB 2.0 signals to a standard USB A connector. It is recommended that each USB data line be routed with a common mode choke and ESD protection. A Power switch / BC1.2 charger controller/ MUX /USB PD (BC1.2 detection) module is present in the topology.

***Notes:***

1. Current electrical characteristic recommendation on Power switch/controller/MUX for charging is to have on-state resistance and on-state capacitance of no greater than 6 Ω and 6pF respectively.
2. Current electrical characteristic limitation on Power switch/controller/MUX for charging is insertion loss of no greater than -0.6 dB and return loss of no greater than -13 dB.
3. For a maximum length channel of 6” – it is recommended that the length of M8_Charger_Length be 1” (1000 mils) for a 6”channel. But, typically as short as possible.
4. The total channel (including the MUX/BC1.2 charger/power switch module) insertion loss should not exceed -2.95 dB and return loss should not exceed -8.5 dB.
5. The length of the main board channel can be increased by trading-off the insertion loss (at 240 MHz) and equivalent on-state resistance and on-state capacitance of the BC1.2 charger module/power switch/MUX. The maximum on-state resistance and on-state capacitance as well as insertion loss allowable for the module is dependent on the total board routing as shown in USB2.0 BC1.2 / MUX/ Power switch Component Restrictions.

**Figure 19-10.USB 2.0 External / Back Panel with Power Switch/ BC1.2 Charger Module/ MUX Topology**

**Table 19-13. USB 2.0 External / Back Panel with Power Switch / BC1.2 Charger Module / Mux Topology Routing Guidelines**

| Parameter | Segment | Stackup (MS/SL/ DSL) | Reference | Via Count | Routing Recommendations | |
|---|---|---|---|---|---|---|
| | | | | | Segment (mm) | Segment (mils) |
| Trace Length (MCP Breakout) Max | BO | MS /SL / DSL | VSS | 1 | 15.2 | 598.42 |
| Trace Length (Main route) Max | M1+M2 | MS /SL / DSL | VSS | 1 | N/A | N/A |
| Trace Length (To BC1.2 Charger/ Mux) Max | M3 | MS | VSS | 1 | 3.8 | 149.6 |
| Trace Length (To Choke) Max | M5 | MS | VSS | | N/A | N/A |
| Trace Length (To ESD Diode) Max | M6 | MS | VSS | 1 | 3.8 | 149.6 |
| Trace Length (To Ext. Connector) Max | M7 | MS | VSS | 0 | 12.7 | 500 |
| M8_chareger_Length Max | M5 + M6 + M7 (M8_charger_len) | MS | VSS | 0 | 25.4 | 1000 |
| Total Motherboard Trace Length | BO+ M1 + M2 + M3 + M4 | NA | | | Max = 152.4<br>Min = 76.2 | Max = 6000<br>Min = 3000 |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 3.
3. Continuous GND referencing plane is preferred
4. Typical component R/C:ON-state resistance and capacitance of 6ohm and 6pF, Insertion Loss <= -0.6dB ; Return Loss <= -13dB
5. Total channel insertion and return loss: Insertion Loss <= -3dB ; Return Loss <= -8.5dB.
6. In order to assure adequate EMI and ESD protection, a common mode choke and ESD protection diode should be implemented on each USB data line.

**Table 19-14. BC1.2 Charger Controller/MUX/Power switch/USB PD (with BC1.2 detection) Module Component Restrictions**

| Motherboard Total Trace Length (mm) | Motherboard Total Trace Length (Inches) | Max charger module on-state resistance, Ron (Ω); on-state capacitance, Con (pF) | Equivalent charger module insertion loss (dB) at 240 MHz |
|---|---|---|---|
| 177.8 | 7.0 | 4 Ω 4 pF | -0.45 to 0.46 dB |
| 152.4 | 6.0 | 5 Ω 5 pF | -0.57 to 0.58 dB |
| 127 | 5.0 | 6 Ω 6 pF | -0.74 to 0.75 dB |
| 101.6 | 4.0 | 6 Ω 6 pF | -0.74 to 0.75 dB |
| 76.2 | 3.0 | 7 Ω 7pF | -0.88 to 0.89 dB |

## 19.7.7 USB 2.0 Docking Topology

- Total trace length will influence the USB transmit amplitude setting. USB Initialization Registers can be set according to recommendations available in Cannon Lake PCH-H External Design Specification.
- This topology meets USB 2.0 specifications if a trace length on the motherboard (M_MB_LEN) is >4” and the length of M1 ≠ M2. At very short motherboard lengths of 3-4” with M1 = M2 is this topology may not meet the USB 2.0 electrical

specifications. Using a dock with integrated USB Hub may increase the routability of this topology.

- It is recommended that each USB data line be routed with a common mode choke and ESD diode

***Note:*** Via placement is compensable. If vias are not used on the main motherboard, then additional via can be placed on the docking board and vice versa. However, total number of vias in entire channel is 3.

**Figure 19-11.USB 2.0 Traditional Docking Topology**

**Table 19-15. USB 2.0 Traditional Docking Topology Routing Guidelines**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length,Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | 1 | 15.2 | 76.2 (min)<br>254 (max) | 598.42 | 3000 (min)<br>10000 (max) |
| M3 | MS | VSS | 1 | 3.8 | | 149.6 | |
| M4 | MS | VSS | 0 | 3.8 | | 149.6 | |
| M5 | MS | VSS | 0 | 12.7 | | 500 | |
| M1+M2 | MS/SL/DSL | VSS | 1 | N/A | | N/A | |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 3.
3. Continuous GND referencing plane is preferred
4. General Docking Routing: 0.3 < M_MB_LEN / TOT_LEN < 0.8, M1 =/ = M2 and M_MB_LEN >3".
5. In order to assure adequate EMI and ESD protection, a common mode choke and ESD protection diode should be implemented on each USB data line.

## 19.7.8 USB 2.0 Detachable Docking Topology

The following figure shows and overview of the docking topology which supports routing from the PCH on the motherboard to a USB 2.0 A-connector on a docking board. Careful attention should be given to the docking connector design as well as its associated internal cables and sub/base boards to ensure that signal quality is not degraded. A USB 2.0 Hub is required on the docking board. Since different Hub chips

have different characteristics, contact your Hub Vendor for routing guidelines from the Hub to A-connector. It is recommended that each USB data line be routed with a common mode choke and ESD protection from the Hub to A-connector

### Figure 19-12.USB 2.0 Detachable Docking Topology

***Note:*** Single multiplexer (MUX) on the docking board is optional and is required if a flippable dual-side detachable docking connector is required. Mux component should have an on-state resistance and on-state capacitance of not more than 6 Ω and 6 pF (which translates to an insertion loss of roughly -0.74 dB).

In order to assure adequate EMI and ESD protection, a common mode choke and ESD protection diode should be implemented on each USB data line.

### Table 19-16. USB 2.0 Detachable Docking Routing Guidelines

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length,Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | 0 | 15.2 | 50.8 (min) 101.6 (max) | 598.42 | 2000 (min) 4000 (max) |
| M1 | MS | VSS | 1 | 3.8 | | 149.6 | |
| MR | MS/SL/DSL | VSS | 1 | N/A | | N/A | |
| M_S1 | MS/SL/DSL | VSS | 0 | 25.4 | 25.4 | 1000 | 1000 |
| M_S2 | MS/SL/DSL | VSS | 0 | 25.4 | 25.4 | 1000 | 1000 |
| M_D1 | MS | VSS | 1 | 3.8 | 54.6 (min) 105.4 (max) | 149.6 | 2149.6 (min) 4149.6 (max) |
| M_D2 | MS/SL/DSL | VSS | 1 | 50.8 | | 2000 | |
| M_D3 | MS/SL/DSL | VSS | 0 | 50.8 | | 2000 | |

***Notes:***
1. Length Matching between P and N with in a differential pair with in same layer mismatch is +/-0.254mm (+/-10mils). Total length mismatch is +/-0.381mm (+/-15mils).
2. Number of vias allowed is maximum of 4.
3. Continuous GND referencing plane is preferred

**Table 19-17. USB 2.0 Trade-off on Internal Cable Differential Insertion Loss on Margins**

| Main Board Total Trace Length (mm) | Main Board Total Trace Length (Inch) | Internal Cable Assembly Insertion Loss on Tablet/motherboard | Internal Cable Assembly Insertion Loss on Docking |
|---|---|---|---|
| 101.6 | 4.0 | .43 dB (at 240 MHz)<br>[2.2 dB at 2.5 GHz] | .43 dB (at 240 MHz)<br>[2.2 dB at 2.5 GHz] |
| 88.9 | 3.5 | .52 dB (at 240 MHz)<br>[2.76 dB at 2.5 GHz] | .52 dB (at 240 MHz)<br>[2.76 dB at 2.5 GHz] |
| 76.2 | 3.0 | .61 dB (at 240 MHz)<br>[3.34 dB at 2.5 GHz] | .61 dB (at 240 MHz)<br>[3.34 dB at 2.5 GHz] |
| 63.5 | 2.5 | .69 dB (at 240 MHz)<br>[3.73 dB at 2.5 GHz] | .69 dB (at 240 MHz)<br>[3.73 dB at 2.5 GHz] |
| 50.8 | 2.0 | .76 dB (at 240 MHz)<br>[4.24 dB at 2.5 GHz] | .76 dB (at 240 MHz)<br>[4.24 dB at 2.5 GHz] |

Consider the following guidelines:

- Total trace length will influence the USB transmit amplitude setting. USB Initialization Registers can be set according to recommendations available in the *Cannon Lake PCH-H External Design Specification*.
- This topology meets USB 2.0 specifications if a trace length on the motherboard (M_MB_LEN) is >4” and the length of M1 ≠ M2. At very short motherboard lengths of 3-4” with M1 = M2 is this topology may not meet the USB 2.0 electrical specifications. Using a dock with integrated USB Hub may increase the routability of this topology.

***Notes:***

- Via placement is compensable. If vias are not used on the main motherboard, then additional via can be placed on the docking board and vice versa. However, total number of vias in entire channel is 3.

## 19.7.9 USB Connector Recommendations

Proper connector choice is critical to ensure adequate USB signal quality. Empirical data has shown that quad-stack USB and DisplayPort*/USB stack connectors may add interference causing poor USB signal quality. Refer to usb.org for a list of tested connectors.

### 19.7.9.1 External Connector Recommendations

The cable and PCB mating connector must pass the TDR requirements listed in the USB 2.0 Specification.

**USB 2.0 Mobile Internal Connector**

It is possible to define the internal connector pin list based on individual needs. However, an example connector pin list for 2-port internal cable connection supporting both USB 2.0 and USB 3.1 is shown in the following table.

**Table 19-18. Example of Internal Connector Pin Assignment and Description**

| Pin Number | Signal | Description |
|---|---|---|
| 1 | RSVD | Reserved Pin |
| 2 | Vbus | 5 v bus power |
| 3 | Vbus | 5 V bus power |
| 4 | Vbus | 5 V bus power |
| 5 | USB2_DIP | USB 2.0 Port 1 D- |
| 6 | USB2-DIN | USB 2.0 Port 1 D+ |
| 7 | PWR_GND | Power GND return |
| 8 | USB2_D2P | USB 2.0 Port 2 D+ |
| 9 | USB2_D2N | USB 2.0 Port 2 D- |
| 10 | PWR_GND | Power GND return |
| 11 | USB3_TX1P | USB 3.1 Port 2 SuperSpeed Tx+ |
| 12 | USB3_TX1N | USB 3.1 Port 2 SuperSpeed Tx- |
| 13 | SIG_GND | Signal GND return |
| 14 | USB3_RX1P | USB 3.1 Port 2 SuperSpeed Rx+ |
| 15 | USB3_RX1N | USB 3.1 Port 2 SuperSpeed Rx- |
| 16 | SIG_GND | Signal GND return |
| 17 | USB3_TX2P | USB 3.1 Port 2 SuperSpeed Tx+ |
| 18 | USB3_TX2N | USB 3.1 Port 2 SuperSpeed Tx- |
| 19 | SIG_GND | Signal GND return |
| 20 | USB3_RX2P | USB 3.1 Port 2 SuperSpeed Rx+ |
| 21 | USB3_RX2N | USB 3.1 Port 2 SuperSpeed Rx- |
| 22 | SIG_GND | Signal GND return |

## 19.7.10 Daughter Card

The best way to provide internal support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. The following figure shows the major components associated with a typical USB solution that uses a daughter card.

When designing the motherboard with internal topology support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there are not duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

**Figure 19-13.Daughter Card**

**Daughter Card Design Guidelines**

The followings are recommended when designing a USB 2.0 daughter card:

- Place the VBUS bypass capacitor, CMC, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Use the same mating connector pinout as - USB 3.1 Internal Connector Pinout (Motherboard).
- Minimize the trace length on the daughter card - Less than a 2-inch trace length is recommended.
- Use the same routing guidelines as described in USB 2.0 Stack-up Guidelines.
- Power and ground nets should have double vias. Trace lengths should be kept as short as possible.

## 19.7.11 USB 2.0 Stack-up Guidelines

## 19.7.12 Stack-up and Layer Utilization Guidelines

Refer to Chapter 2, "Stack-Up and PCB Considerations" - Type 3 and Type 4 Stack-up sections for all I/O routing guidelines including USB 2.0.

## 19.7.13 USB 2.0 Configuration, Connectivity, Block Diagram

## 19.7.14 Port Power Delivery

The following is a suggested topology for power distribution of VBUS to USB ports. These circuits provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach flyback protection. These two types require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). Intel recommends the following:

- Minimize the inductance and resistance between the coupling capacitors and the USB ports.
- Place capacitors close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane.

- Make the power-carrying traces wide enough that the system fuse blows on an overcurrent event. If the system fuse is rated at 1 A, then the power-carrying traces should be wide enough to carry at least 1.5 A.

**Figure 19-14.Good Downstream Power Connection**

## 19.7.15 USB 2.0 Length Matching Guidelines

### 19.7.15.1 Length Matching

Refer to the Section 3.4, "General Differential Length Matching Guidelines" for length matching guidelines.

## 19.7.16 EMI and ESD Protection

Refer to **Chapter 49, "Electromagnetic Compatibility"**

## 19.7.17 USB 2.0 Disabling and Termination Guidelines

If a USB port(s) is not implemented on the platform:

- USB P/N [x] signals can be left unconnected

§ §

# 20 USB Type-C

USB Type-C is a cable and connector specification defined by USB-IF. The connector is

defined so that it is capable of supporting ultra thin form factor with z height as low as 3mm and also enhanced user experience by allowing the USB Type-C plug to be plugged into a receptacle either right side up or up side down. Refer to the following figure for the detailed pin map of a USB Type-C receptacle.

Coffee Lake supports device role on all its USB ports. In Coffee Lake, the only way to put a port in device mode is by setting control register bits specific to USB port and not via hardware mechanism as in Kaby Lake (OTG_ID, VBUS _SENSE is used to detect in Kaby Lake).

For USB type-A ports, which are host only ports, there is a strap in PCH to configure specific USB3 ports to be host only and in such cases PCH leaves USB3 ports connected to its internal logic. Since USB-C connector supports both host and device role, we cannot set that strap. When strap is not set, Coffee Lake SoC leaves the USB3 port disconnected from internal logic. This means at every connect/disconnect/role change events for USB-C, we need to explicitly communicate this information to the SoC. In addition to this, alternate mode entry/exit also need to be explicitly communicated to SoC since it has to know when USB3 is getting connected/disconnected vs both USB3/ USB2 getting connected/disconnected.

Coffee Lake SoC supports 2 ways for this communication. This is new requirement for Coffee Lake.

1. eSPI messages between EC and PMC when eSPI EC is used.
2. BIOS to set control register bits when LPC EC is used. Since SoC needs to be in S0 when using BIOS mechanism, some of the low power/early boot scenarios will NOT be supported using LPC ECs.

During system state transitions, when EC remains powered ON but SPR registers inside PCH maybe reset, at that time it’s responsibility for EC to resend connect messages for respective connectors to the PMC.

**Figure 20-1. Coffee Lake Platform USB Type-C Block Diagram**

***Note:*** The figure above is a high level example implementation block diagram for two USB Type-C connectors with Titan Ridge TBT and PD Controller. The red arrows indicate the communication pathways. Actual implementation on schematics may vary.

**Figure 20-2. USB Type-C Receptacle Pin Map**

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | TX1+ | TX1– | VBUS | CC1 | D+ | D– | SBU1 | VBUS | RX2– | RX2+ | GND |
| | | | | | | | | | | | |
| GND | RX1+ | RX1– | VBUS | SBU2 | D– | D+ | CC2 | VBUS | TX2– | TX2+ | GND |
| B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |

USB Type-C connector consists of 24 signal pins designed in a symmetrical way. Refer to Section 20.2, "USB Type-C Signal Group and Descriptions" for description of all the signals on a USB Type-C connector.

There are up to 6 differential pairs available on a USB Type-C connector, with 4 high speed different pairs and 2 low speed pairs. There are 2 configuration channel signals (CC1/CC2) on the connector which is used for:

- Device detection
- Orientation detection
- Establish DFP and UFP roles
- Discover and configure power
- Discover and configure optional alternate/accessory modes

Unused CC pin will be reconfigured as Vconn, which is used to power the active cable.

**Figure 20-3. Anatomy of a USB Type-C Receptacle**

With two configuration channel signals for communication, USB Type-C connector can support not only USB interfaces but also any other vendor specific interface like DisplayPort* in Alternate Mode.

In Alternate Mode, both the high speed and low speed link and both the SBU1/2 pins can be reconfigured to support the intended configuration. See figure below for an example of the pin re-configuration to support a USB + DP x 2 configuration. DP as an Alt Mode will be described in more detail in the later sections.

**Figure 20-4. USB Type-C Connector Pin Map for a USB + DP x 2 Alternate Mode Example**

## 20.1 USB Type-C Platform- Specific Important Information

Coffee Lake platform support USB Type-C implementation using TCPCi based port controller. USB Type-C port can be configured to support Alternate Modes as per the specification such as DisplayPort* by reconfiguring the connector pins.

Coffee Lake platform reference collateral provide sample implementation of various configuration options that the USB Type-C specification offers including USB 2.0/3.1 and Alternate Modes such as DisplayPort*.

Refer to table below for the supported features being enabled for the Coffee Lake platform.

**Table 20-1. USB Type-C Supported Configuration on Coffee Lake**

| Interface 1 | Interface 2 | Interface3 | Description |
|---|---|---|---|
| USB 3.1 SS | | | USB only with no Alternate Mode |
| USB 3.1 SS | DP* x 2 | | USB with DP 1.3. USB 3.1SS and DP x 2 can be active concurrently. |
| USB 3.1 SS | DP * x 4 | | USB with DP 1.3 for DP panel support with higher resolution. DP x 4 and USB 3.1 SS cannot exist concurrently. When DP x4 is active only USB 2.0 signal is available. |
| USB 3.1 SS | DP* x 2 or DP * x 4 | Intel(R) DCI OOB | Intel(R) DCI OOB is supported over active switch |

## 20.2 USB Type-C Signal Group and Descriptions

| Group | Signal Name | Description |
|---|---|---|
| Power | VBUS | VBUS, capable of up to 3A @ 20V with USB PD |
| | VCONN | VCONN is a power source to active cable which is capable of supplying up to 0.2A @ 5V. Unconnected CC pin will be reconfigured to VCONN when a device is plugged in. |
| Ground | GND | Ground |
| High Speed Differential | TX1+ | First USB3.1 Diff TX pair |
| | TX1- | |
| | RX1+ | First USB3.1 Diff RX pair |
| | RX1- | |
| | TX2+ | Second USB3.1 Diff TX pair |
| | TX2- | |
| | RX2+ | Second USB3.1 Diff RX pair |
| | RX2- | |
| Low Speed Differential | D+ | Low Speed Differential Pair, primary for USB 2 connection |
| | D- | |

| Group | Signal Name | Description |
|---|---|---|
| Control | CC1 | Configuration Channel 1. Used for device detection, orientation detection and Alternate Mode configuration. Unconnected pins will be reconfigured to Vconn. |
| | CC2 | Configuration Channel 2.Used for device detection, orientation detection and Alternate Mode configuration. Unconnected pins will be reconfigured to Vconn |
| Side band | SBU1 | Sideband signals for use by alternate mode AUX signals |
| | SBU2 | |

# 20.3 USB Type-C Topology Guidelines

## 20.3.1 USB 2.0 Guidelines

USB Type-C can be configured to support USB signals only (LS,FS,HS,SS) with a minimum requirement of USB 2.0 (LS, FS, HS) support. Below are the options available for implementing a USB only USB Type-C connector with discrete components on a Coffee Lake platform.

- USB 2.0 USB Type-C Topology
- USB 2.0 with BC1.2 charger module / MUX / Power Switch Topology.
- USB2.0 with MUX and Redriver topology

**Figure 20-5. USB 2.0 Only USB Type-C Connector**

***Note:*** The figure above is a high level example implementation block, actual implementation on the schematic may vary.

USB 2.0 is the minimum requirement for implementing a USB Type-C connector. This configuration is achieved by connecting a pair of USB 2.0 signal to DP+/DP- pins on the receptacle and shorting the 2 DP+/DP- on the receptacle together. On Coffee Lake, all ports are capable of supporting dual role but only one port at a time.

CC1/CC2 is no longer required to handle plug orientation detection in this configuration as there is no switching needed. However discrete CC logic is still needed for handling UFP/DFP detection, Vconn switching and VBUS control.

ESD protection devices is required for all signal connecting to Coffee Lake directly. For signals that is connected to 3rd party component like MUX/controller, refer to 3rd Party component specification to decide if platform level ESD device is needed.

CMC may be required to pass EMI test therefore a CMC footprint is recommended.

USB_ID and VBUS_SENSE pins are not needed for USB Type-C implementation with Type-C port controller (TCPC).

**Figure 20-6. USB Type-C Receptacle Pin Map – USB 2.0 Only**

## 20.3.1.1 Layout Guideline

**Figure 20-7. USB 2.0 USB Type-C Topology**

**USB 2.0 USB Type-C Topology Routing Guidelines (Sheet 1 of 2)**

| Parameter | Segment | Stackup | Via Count | Length (mm) | Length (mils) |
|---|---|---|---|---|---|
| Trace Length Maximum | B0 | MS/SL/ DSL | 1 | 15.2 | 598.42 |
| Trace Length Maximum | M3 | MS | 1 | 3.8 | 149.6 |
| Trace Length Maximum | M4 | MS | 0 | 3.8 | 149.6 |
| Trace Length Maximum | M5 | MS | 0 | 14 | 551.18 |
| Trace Length Maximum | M6 | MS | 1 | 3.6 | 141.73 |
| Trace Length Maximum | M7 | SL/DSL | | 3.6 | 141.73 |
| Trace Length Maximum | M1+M2 | MS/SL/ DSL | 1 | NA | NA |
| Total Trace Length Minimum and Maximum | B0+M1+M2+M3+M4+M5+( M6 or M7) | | | 76.2 (min)<br>228.6 (max) | 3000 (min)<br>9000 (max) |

## USB 2.0 USB Type-C Topology Routing Guidelines (Sheet 2 of 2)

| Parameter | Segment | Stackup | Via Count | Length (mm) | Length (mils) |
|---|---|---|---|---|---|
| ***Notes:***<br>1. Length Matching allowed between P and N within a differential pair:<br>a. Within same layer mismatch:± 0.254mm (± 10mils).<br>b. Total length mismatch:± 0.381mm (± 15mils).<br>2. Maximum via count is 4 ((including the one implemented to accommodate stub).<br>3. NA in the table implies that there is no strict trace length requirements for that particular segment.<br>4. Maximum stub length allowed is 3.6mm (141.7 mils)<br>5. Continuous GND referencing is preferred. Power plane referencing is also allowed. | | | | | |

## Figure 20-8. USB 2.0 with BC1.2 Charger Module / MUX / Power Switch Topology

## Table 20-2. USB 2.0 with BC1.2 Charger Module / MUX / Power Switch Topology Routing Guidelines

| Parameter | Segment | Stackup | Via Count | Length (mm) | Length (mils) |
|---|---|---|---|---|---|
| Trace Length Maximum | B0 | MS/SL/ DSL | 1 | 15.2 | 598.42 |
| Trace Length Maximum | M1+M2 | MS/SL/ DS | 1 | NA | NA |
| Trace Length Maximum | M3 or M5 | MS | 1 | 3.8 | 149.6 |
| Trace Length Maximum | M6 | MS | 0 | 14 | 551.18 |
| Trace Length Maximum | M7 | MS | 1 | 3.6 | 141.73 |
| Trace Length Maximum | M8 | SL/DSL | | 3.6 | 141.73 |
| Trace Length Maximum | M4+M5+M6+M7 or M4+M5+M6+M8 (M9 Charger Length) | MS | 0 | 25.4 | 1000 |
| Total trace length (min and max) | | | | 76.2 (min)<br>152.4 (max) | 3000 (min)<br>6000 (max) |
| ***Notes:***<br>1. Length Matching allowed between P and N within a differential pair:<br>a. Within same layer mismatch:± 0.254mm (± 10mils).<br>b. Total length mismatch:± 0.381mm (± 15mils)<br>2. Maximum number of vias allowed is 4 (including one implemented to accommodate stub).<br>3. NA in the table implies that there is no strict trace length requirements for that particular segment.<br>4. Reference plane recommended is continuous ground. Power plane referencing is also allowed.<br>5. Maximum stub length allowed is 3.6mm (141.7 mils).<br>6. Typical component R/C:<br>a. On-state resistance is 6 Ohm and capacitance is 6pF.<br>b. Insertion Loss <= -0.6dB ; Return Loss <= -13dB.<br>7. Total channel insertion and return loss:<br>a. Insertion Loss <= -3dB ; Return Loss <= -8.5dB. | | | | | |

## Figure 20-9. BC1.2 Charger Module / MUX / Power Switch/USB PD (with BC 1.2 detection) Module Component Restrictions

| Motherboard Total Trace Length (mm) | Motherboard Total Trace Length (inches) | Max charger module on-state resistance, Ron (Ω) ; on-state capacitance, Con (pF) | Equivalent charger module insertion loss (dB) at 240 MHz |
|---|---|---|---|
| 177.8 | 7.0 | 4 Ω ; 4 pF | -0.45 to 0.46 dB |
| 152.4 | 6.0 | 5 Ω ; 5 pF | -0.57 to 0.58 dB |
| 127 | 5.0 | 6 Ω ; 6 pF | -0.74 to 0.75 dB |
| 101.6 | 4.0 | 6 Ω ; 6 pF | -0.74 to 0.75 dB |
| 76.2 | 3.0 | 7 Ω ; 7 pF | -0.88 to 0.89 dB |

## Figure 20-10.USB 2.0 USB Type-C Port with MUX and Redriver Topology

## Table 20-3. USB 2.0 to USB Type-C Port Routing Guideline with MUX and Redriver Topology (Sheet 1 of 2)

| Segment | Tline Type | Via Count | Length (mils) | Length (mm) |
|---|---|---|---|---|
| BO | MS/SL/DSL | 1 | 598.42 | 15.2 |
| M1+M2 | MS/SL/DSL | 1 | NA | NA |
| M3 or M6 | MS | 1 | 149.6 | 3.8 |
| M4 | MS | 0 | 1000 | 25.4 |
| M7 | MS | 0 | 551.18 | 14 |
| M8 | MS | 1 | 141.73 | 3.6 |
| M9 | SL/DSL | | 141.73 | 3.6 |
| M5+M6+M7+M8 or M5+M6+M7+M9 (M10_charger_len) | MS | 0 | 1000 | 25.4 |
| **Total Length** | | | 3000 (min)<br>13000 (max) | 76.2 (min)<br>330.2 (max) |

**Table 20-3. USB 2.0 to USB Type-C Port Routing Guideline with MUX and Redriver Topology (Sheet 2 of 2)**

| Segment | Tline Type | Via Count | Length (mils) | Length (mm) |
|---|---|---|---|---|

***Notes:***

1. Length Matching allowed between P and N within a differential pair:
   a. Within same layer mismatch:± 0.254mm (± 10mils).
   b. Total length mismatch:± 0.381mm (± 15mils)
2. Maximum number of vias allowed is 4 (including one implemented to accommodate stub).
3. NA in the table implies that there is no strict trace length requirements for that particular segment.
4. Reference plane recommended is continuous ground. Power plane referencing is also allowed.
5. Maximum stub length allowed is 3.6mm (141.7 mils).
6. Typical component (MUX) R/C:
   a. On-state resistance is 6 Ohm and capacitance is 6pF.
   b. Insertion Loss <= -0.6dB ; Return Loss <= -13dB
7. Redriver component:
   a. Placement of redriver component will be dependent on redriver pre- and post- channel equalization strength. It is recommended that the designer determine the optimum routing through the redriver datasheet and working with the component vendor.

## 20.3.2 USB 3.1 Guidelines

This section describes the USB Type-C implementation details for USB 3.1 Gen1 and Gen2 speeds.

CC1/CC2 signal on the USB Type-C connector is used to detect the plug orientation and a decoding logic is used to decode the CC1/CC2 signal and control the high speed mux/switch to route USB 3.1 SS signals to the right differential pair.

CC1/CC2 has the options to be decoded with:

- Port chip capable of CC logic decoding
- Full Port controller with CC logic decoding (USB PD is optional on USB Type-C)

Any USB 3.1 port can support Dual Role (DRP) Mode on Coffee Lake, but only one at a time.

USB_ID and VBUS_SENSE signals are not needed for USB Type-C implementation with Type-C Port Controller (TCPC).

ESD protection devices is required for all signal connecting to PCH directly. For signals that are connected to 3rd party components like MUX/controller, refer to 3rd Party component specification to decide if platform level ESD device is needed.

CMC may be required to pass EMI test, therefore a CMC footprint is recommended.

This discrete implementation has high level of dependency on the discrete components used. Each discrete component might have slight different connectivity requirements. Refer to the discrete components datasheet and/or design guide to ensure the functionality of the design.

AC Cap might be needed on RX lines depending on the repeater part used. Suggest to follow recommendation from the repeater vendor.

**Figure 20-11.USB Type-C Receptacle Pin Map - USB 3.1**

**Figure 20-12.USB Type-C Connector Connection (when the plug is 'Right Side Up')**

**Figure 20-13.USB Type-C Connector Connection (when the plug is 'Up Side Down')**

The presence of a mux/switch logic in this configuration will impact the signal quality of USB 3.1 SS signal. A repeater may be required to ensure the signal at USB Type-C connector still meet compliance requirement.

The following sub-sections describe the routing guidelines for following topologies

- USB 3.1 without active mux.
- USB 3.1 with active mux.

### 20.3.2.1 USB 3.1 without Active Mux

This section describes the design guidelines for USB 3.1 without active mux.

## Figure 20-14.USB 3.1 Gen1/Gen2 External Topology Without Active Mux

## Table 20-4. Routing Guidelines- USB 3.1 Gen2- External Topology Without Active Mux

| Parameter | Segment | Stackup | Via Count | Gen2 | |
|---|---|---|---|---|---|
| | | | | Length (mm) | Length (mils) |
| Max Trace Length | BO | MS/SL/DSL | 1 | 10.2 | 400 |
| Max Trace Length | M1 | MS/SL/DSL | 1 | 96.5 | 3800 |
| Max Trace Length | M2+M3+M4 | MS | 0 | 10.2 | 400 |
| Max Trace Length | M5 | MS | 0 | 10.2 | 400 |
| **Total Max Trace Length** | | | | 127.0 | 5000 |

***Notes:***
1. Minimum PCB length is 50.8 mm (2000 mils).
2. Reference is VSS for all segments.
3. Crx Cap Value: 297nF to 363nF including tolerance.
4. Rb Resistor Value: 220kΩ ±5%.

## Table 20-5. Routing Guidelines- USB 3.1 Gen1- External Topology Without Active Mux (Sheet 1 of 2) (Sheet 1 of 2)

| Parameter | Segment | Stackup | Via Count | Gen1 | |
|---|---|---|---|---|---|
| | | | | Length (mm) | Length (mils) |
| Max Trace Length | BO | MS/SL/DSL | 1 | 12.7 | 500 |
| Max Trace Length | M1 | MS/SL/DSL | 1 | 104.1 | 4100 |
| Max Trace Length | M2+M3+M4 | MS | 0 | 10.2 | 400 |
| Max Trace Length | M5 | MS | 0 | 12.7 | 500 |
| **Total Max Trace Length** | | | | 139.7 | 5500 |

## Table 20-5. Routing Guidelines- USB 3.1 Gen1- External Topology Without Active Mux (Sheet 2 of 2) (Sheet 2 of 2)

| Parameter | Segment | Stackup | Via Count | Gen1 | |
|---|---|---|---|---|---|
| | | | | Length (mm) | Length (mils) |

***Notes:***
1. Minimum PCB length is 50.8 mm (2000 mils).
2. Reference is VSS for all segments.
3. Crx Cap Value: 297nF to 363nF including tolerance.
4. Rb Resistor Value: 220kΩ ±5%.

## Figure 20-15.USB 3.1 Gen1/Gen2 Internal Cable Topology Without Active Mux

***Notes:***
1. Minimum main board length is 25.4 mm (1000 mils).
2. Reference is VSS for all segments.
3. Assumes DP internal cable loss profile.
4. Crx Cap Value: 297nF to 363nF including tolerance.
5. Rb Resistor Value: 220kΩ ±5%.

## Table 20-6. Routing Guidelines- USB 3.1 Gen2- Internal Cable Topology Without Active Mux

| Parameter | Segment | Stackup | Via Count | Gen2 | |
|---|---|---|---|---|---|
| | | | | Length (mm) | Length (mils) |
| Max Trace Length | BO | MS/SL/DSL | 1 | 10.2 | 400 |
| Max Trace Length | M1 | MS/SL/DSL | 1 | 48.3 | 1900 |
| Max Trace Length | M2 | MS | 0 | 5.1 | 200 |
| Max Trace Length | M3+M4+M5+M6 | MS | 0 | 12.5 | 500 |
| **Total Max Trace Length (BO+M1+M2)** | | | | 63.5 | 2500 |
| **Total Max Trace Length (M3+M4+M5+M6)** | | | | 12.5 | 500 |

### Table 20-7. Routing Guidelines- USB 3.1 Gen1- Internal Cable Topology Without Active Mux

| Parameter | Segment | Stackup | Via Count | Gen1 | |
|---|---|---|---|---|---|
| | | | | Length (mm) | Length (mils) |
| Max Trace Length | BO | MS/SL/DSL | 1 | 15.2 | 600 |
| Max Trace Length | M1 | MS/SL/DSL | 1 | 68.6 | 2700 |
| Max Trace Length | M2 | MS | 0 | 5.1 | 200 |
| Max Trace Length | M3+M4+M5+M6 | MS | 0 | 50.8 | 2000 |
| **Total Max Trace Length (BO+M1+M2)** | | | | 88.9 | 3500 |
| **Total Max Trace Length (M3+M4+M5+M6)** | | | | 50.8 | 2000 |

#### 20.3.2.1.1 USB 3.1 with Active Mux

This section describes the design guidelines for USB 3.1 with active mux. Active mux can be re-driver based or re-timer based. This following sections cover both these topologies.

### Figure 20-16.USB 3.1 Gen1/Gen2 Active Mux External Topology

***Notes:***

- Minimum length: Pre-channel is 152.4 mm (6000 mils) and post-channel is 12.7 mm (500 mils).
- Reference for all segments is VSS.
- Crx Cap Value: 297nF to 363nF including tolerance.
- Rb Resistor Value: 220kΩ ±5%.

## Table 20-8. Routing Guidelines- USB 3.1 Gen2 Active Mux External Topology (With Re-driver Based Active Mux)

| Channel | Parameter | Segment | Stackup | Via Count | Gen2 | |
|---|---|---|---|---|---|---|
| | | | | | Length (mm) | Length (mils) |
| Pre-channel | Max Trace Length | BO | MS/SL/DSL | 1 | Note#1* | Note#1* |
| | Max Trace Length | M1 | MS/SL/DSL | 1 | Note#1* | Note#1* |
| | Max Trace Length | M2+M3 | MS | 0 | Note#1* | Note#1* |
| Post-channel | Max Trace Length | M4 + M5 | MS | 1 | 7.6 | 300 |
| | Max Trace Length | M6+M7 | MS | | 7.6 | 300 |
| | Max Trace Length | M8 | MS | | 10.2 | 400 |
| **Total Max Trace Length (Pre-channel)** | | | | | Note#1* | Note#1* |
| **Total Max Trace Length(Post-channel)** | | | | | 25.4 | 1000 |

***Notes:*** **Important Guidelines on Re-driver based Active Mux/Re-driver Topologies**

1. *Max pre-channel length at USB3.1 Gen 2 speeds (10Gb/s) depends on what the specific re-driver based active mux/re-driver selected can compensate for when used in conjunction with Intel PCH. Work with repeater vendor to ensure that the component being utilized will provide adequate signal integrity at the PCH.
   a. OEMs are recommended to use the CRB/RVP topologies as reference for pre-channel lengths which are achievable and validated by Intel.
2. In addition, it is recommended to refer to the white paper pertaining to the repeater integration (USB 3.1 Repeater Integration Technical White Paper Rev 0.9 with RDC#571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
3. It is recommended that OEMs use re-driver based active mux/re-driver parts from 3rd party vendors which meet below requirements to avoid Electrical Over Stress (EOS) on USB3.1 receiver lines:
   a. During power on and receive detect phase, recommended transmitter common mode voltage (Vcm) and impedance values:
   - If (Vcm <= 1.2V), Repeater Impedance >= 1K ohm **ELSE**
   - (Vcm+Rx.detect pulse amplitude <= 2.2V) **AND** (Repeater Impedance >= 4.5K ohm).

## Table 20-9. Routing Guidelines- USB 3.1 Gen1 Active Mux External Topology (With Re-driver Based Active Mux)

| Channel | Parameter | Segment | Stackup | Via Count | Gen1 | |
|---|---|---|---|---|---|---|
| | | | | | Length (mm) | Length (mils) |
| Pre-channel | Max Trace Length | BO | MS/SL/DSL | 1 | 12.7 | 500 |
| | Max Trace Length | M1 | MS/SL/DSL | 1 | 241.3 | 9400 |
| | Max Trace Length | M2+M3 | MS | 0 | 12.7 | 500 |
| Post-channel | Max Trace Length | M4 + M5 | MS | 1 | 7.6 | 300 |
| | Max Trace Length | M6+M7 | MS | | 7.6 | 300 |
| | Max Trace Length | M8 | MS | | 10.2 | 400 |
| **Total Max Trace Length (Pre-channel)** | | | | | 266.7 | 10500 |
| **Total Max Trace Length(Post-channel)** | | | | | 25.4 | 1000 |

***Notes:*** **Important Guidelines on Re-driver based Active Mux/Re-driver Topologies**

1. Refer to the white paper pertaining to the repeater integration (USB 3.1 Repeater Integration Technical White Paper Rev 0.9 with RDC#571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeaters in customer system designs.
2. It is recommended that OEMs use re-driver based active mux/re-driver parts from 3rd party vendors which meet below requirements to avoid Electrical Over Stress (EOS) on USB3.1 receiver lines:
   a. During power on and receive detect phase, recommended transmitter common mode voltage (Vcm) and impedance values:
   - If (Vcm <= 1.2V), Repeater Impedance >= 1K ohm **ELSE**
   - (Vcm+Rx.detect pulse amplitude <= 2.2V) **AND** (Repeater Impedance >= 4.5K ohm).

## Table 20-10. Routing Guidelines- USB 3.1 Gen2 Active Mux External Topology (With Re-timer Based Active Mux)

| Channel | Parameter | Segment | Stackup | Via Count | Gen2 | |
|---|---|---|---|---|---|---|
| | | | | | Length (mm) | Length (mils) |
| Pre-channel | Max Trace Length | BO | MS/SL/DSL | 1 | 10.2 | 400 |
| | Max Trace Length | M1 | MS/SL/DSL | 1 | 358.1 | 14100 |
| | Max Trace Length | M2+M3 | MS | 0 | 12.7 | 500 |
| Post-channel | Max Trace Length | M4 + M5 | MS | 1 | 101.6 | 4000 |
| | Max Trace Length | M6+M7 | MS | | 15.2 | 600 |
| | Max Trace Length | M8 | MS | | 10.2 | 400 |
| **Total Max Trace Length (Pre-channel)** | | | | | 381.0 | 15000 |
| **Total Max Trace Length(Post-channel)** | | | | | 127.0 | 5000 |

***Notes:*** **Important Guidelines on Re-timer based Active Mux/Re-timer Topologies**

1. Refer to the white paper pertaining to the repeater integration (USB 3.1 Repeater Integration Technical White Paper Rev 0.9 with RDC#571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeaters in customer system designs.
2. It is recommended that OEMs use re-driver based active mux/re-driver parts from 3rd party vendors which meet below requirements to avoid Electrical Over Stress (EOS) on USB3.1 receiver lines:
   a. During power on and receive detect phase, recommended transmitter common mode voltage (Vcm) and impedance values:
   - If (Vcm <= 1.2V), Repeater Impedance >= 1K ohm **ELSE**
   - (Vcm+Rx.detect pulse amplitude <= 2.2V) **AND** (Repeater Impedance >= 4.5K ohm).

## Table 20-11. Routing Guidelines- USB 3.1 Gen1 Active Mux External Topology (With Re-timer Based Active Mux)

| Channel | Parameter | Segment | Stackup | Via Count | Gen1 | |
|---|---|---|---|---|---|---|
| | | | | | Length (mm) | Length (mils) |
| Pre-channel | Max Trace Length | BO | MS/SL/DSL | 1 | 12.7 | 500 |
| | Max Trace Length | M1 | MS/SL/DSL | 1 | 368.3 | 14500 |
| | Max Trace Length | M2+M3 | MS | 0 | 12.7 | 500 |
| Post-channel | Max Trace Length | M4 + M5 | MS | 1 | 53.3 | 2100 |
| | Max Trace Length | M6+M7 | MS | | 53.3 | 2100 |
| | Max Trace Length | M8 | MS | | 71.1 | 2800 |
| **Total Max Trace Length (Pre-channel)** | | | | | 393.7 | 15500 |
| **Total Max Trace Length(Post-channel)** | | | | | 177.8 | 7000 |

***Notes:*** **Important Guidelines on Re-timer based Active Mux/Re-timer Topologies**

1. Refer to the white paper pertaining to the repeater integration (USB 3.1 Repeater Integration Technical White Paper Rev 0.9 with CDI# 571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeaters in customer system designs.
2. It is recommended that OEMs use re-driver based active mux/re-driver parts from 3rd party vendors which meet below requirements to avoid Electrical Over Stress (EOS) on USB3.1 receiver lines:
   a. During power on and receive detect phase, recommended transmitter common mode voltage (Vcm) and impedance values:
   - If (Vcm <= 1.2V), Repeater Impedance >= 1K ohm **ELSE**
   - (Vcm+Rx.detect pulse amplitude <= 2.2V) **AND** (Repeater Impedance >= 4.5K ohm).

## Figure 20-17.USB 3.1 Gen1/Gen2 Active Mux Internal Cable Topology

***Notes:***

- Minimum length: Pre-channel is 50.8 mm (2000 mils) and post-channel is 12.7 mm (500 mils).
- Reference for all segments is VSS.
- Crx Cap Value: 297nF to 363nF including tolerance.
- Rb Resistor Value: 220kΩ ±5%.
- Assumes DP internal cable loss profile.

## Table 20-12. Routing Guidelines- USB 3.1 Gen1/Gen2 Active Mux Internal Cable Topology (With Re-driver Based Active Mux)

| Channel | Parameter | Segment | Stackup | Via Count | Gen1/Gen2 | |
|---|---|---|---|---|---|---|
| | | | | | Length (mm) | Length (mils) |
| Pre-channel | Max Trace Length | BO | MS/SL/DSL | 1 | Note#1* | Note#1* |
| | Max Trace Length | M1 | MS/SL/DSL | 1 | Note#1* | Note#1* |
| | Max Trace Length | M2 | MS | 0 | Note#1* | Note#1* |
| | Max Trace Length | M3 | MS | 0 | Note#1* | Note#1* |
| Post-channel | Max Trace Length | M4 + M5 | MS | 1 | 7.6 | 300 |
| | Max Trace Length | M6+M7 | MS | 0 | 7.6 | 300 |
| | Max Trace Length | M8 | MS | 0 | 10.2 | 400 |
| **Total Max Trace Length (Pre-channel)** | | | | | Note#1* | Note#1* |
| **Total Max Trace Length(Post-channel)** | | | | | 25.4* | 1000* |

***Notes:*** **Important Guidelines on Re-driver based Active Mux/Re-driver Topologies**

1. *Max pre-channel length at USB3.1 Gen 2 speeds (10Gb/s) depends on what the specific re-driver based active mux/re-driver selected can compensate for when used in conjunction with Intel PCH. Work with repeater vendor to ensure that the component being utilized will provide adequate signal integrity at the PCH.
   a. OEMs are recommended to use the CRB/RVP topologies as reference for pre-channel lengths which are achievable and validated by Intel.
2. In addition, it is recommended to refer to the white paper pertaining to the repeater integration (USB 3.1 Repeater Integration Technical White Paper Rev 0.9 with RDC#571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
3. It is recommended that OEMs use re-driver based active mux/re-driver parts from 3rd party vendors which meet below requirements to avoid Electrical Over Stress (EOS) on USB3.1 receiver lines:
   a. During power on and receive detect phase, recommended transmitter common mode voltage (Vcm) and impedance values:
   - If (Vcm <= 1.2V), Repeater Impedance >= 1K ohm **ELSE**
   - (Vcm+Rx.detect pulse amplitude <= 2.2V) **AND** (Repeater Impedance >= 4.5K ohm).

### Table 20-13. Routing Guidelines- USB 3.1 Gen1/Gen2 Active Mux Internal Cable Topology (With Re-timer Based Active Mux)

| Channel | Parameter | Segment | Stackup | Via Count | Gen1/Gen2 | |
|---|---|---|---|---|---|---|
| | | | | | Length (mm) | Length (mils) |
| Pre-channel | Max Trace Length | BO | MS/SL/DSL | 1 | 7.6 | 300 |
| | Max Trace Length | M1 | MS/SL/DSL | 1 | 205.7 | 8100 |
| | Max Trace Length | M2 | MS | 0 | 5.1 | 200 |
| | Max Trace Length | M3 | MS | 0 | 10.2 | 400 |
| Post-channel | Max Trace Length | M4 + M5 | MS | 1 | 7.6 | 300 |
| | Max Trace Length | M6+M7 | MS | 0 | 7.6 | 300 |
| | Max Trace Length | M8 | MS | 0 | 10.2 | 400 |
| **Total Max Trace Length (Pre-channel)** | | | | | 228.6 | 9000 |
| **Total Max Trace Length(Post-channel)** | | | | | 25.4 | 1000 |

***Notes:*** **Important Guidelines on Re-timer based Active Mux/Re-timer Topologies**

1. Refer to the white paper pertaining to the repeater integration (USB 3.1 Repeater Integration Technical White Paper Rev 0.9 with RDC#571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeaters in customer system designs.
2. It is recommended that OEMs use re-driver based active mux/re-driver parts from 3rd party vendors which meet below requirements to avoid Electrical Over Stress (EOS) on USB3.1 receiver lines:
   a. During power on and receive detect phase, recommended transmitter common mode voltage (Vcm) and impedance values:
   - If (Vcm <= 1.2V), Repeater Impedance >= 1K ohm **ELSE**
   - (Vcm+Rx.detect pulse amplitude <= 2.2V) **AND** (Repeater Impedance >= 4.5K ohm).

***Note:*** **General Guidelines (applicable to all USB 3.1 USB Type-C topologies unless specified otherwise)**

- Length matching between P and N should be ±10mils within same layer and ±15mils for total length.
- Breakout Scheme: TX and RX breakout at different layers (non-interleaved scheme), for better crosstalk shielding performance. The main route supports interleaved routing and non-interleaved routing for maximum flexibility. However, breakout must be routed using a non-interleaved scheme.
- Microstrip Routing Support: Microstrip main route is also recommended albeit with shorter length than Stripline or Dual-Stripline.
- Breakout Length and Spacing: An initial breakout segment of 4mm (157.48 mils) in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm (4 -6 mils) is allowed. But the total breakout length should still be within the length defined for each topology.
- Trace Geometry:
  — For Gen2, it is recommended to use 80-ohm trace geometry (with larger trace width), primarily to address routing insertion loss at 10Gbps.
  — For Gen1, it is recommended to use 85-ohm trace geometry (narrower trace width), for PCB real estate saving. It is worth noting that Gen2 with 80-ohm trace geometry is fully functional and backward compatible with Gen1 5Gbps signaling.
- Reference plane is recommended to be continuous ground.
- TX AC Capacitor Value: 220nF nominal (135-265nF range including tolerance).
- CMC Usage:
  — USB3 Only: Place TX CMCs; RX CMCs are optional
  — USB3 and DP: Place both TX and RX CMCs due to emission from DP.
- Recommended Short Protection Circuit (Optional): It is recommended to include the RC circuit (using the Crx and Rb values provided) to comply with USB ECN "RX AC Coupling Capacitor Option" to provide ESD/EOS protection, and set RX bias at the Type-C connector.
  — The current PDG topologies are designed to optimize for ESD protection. For applications where VBUS = 5V, these topologies can address EOS also by using a TVS device on the board, having a breakdown voltage higher than 5V.
  — The USB 3.1 USB-IF ECN "Rx AC Coupling Capacitor Option" implementation to address possible EOS is currently under evaluation. Refer to USB3.1 Type-C USB-IF ECN Update (IBL#:575549) for details.
- CMC Bypass: A single 0 Ω resistor per signal trace should be available to be used to bypass the CMC content if it is proven that there is no EMI risk on USB3.1 TX/RX signals. However, the 0 Ω resistor must be placed near the connector at the same recommended location as the CMC.
- ESD may/may not be required depending on the 3rd party's device. On the removal of discrete ESD, there are two requirements that have to be met:

  - Mux/ Redriver can handle the ESD at least 8kV
  - Mux/ Redriver to be placed near to USB-C connector (< 1")
- USB Type-C Possible Configurations:
  - No dual role (related to cable orientation) where two independent USB3.0 signal are connected to the USB-C connector.
  - Dual role whereby a mux/redriver switch are presented to support right side up/ up side down plug orientation of the USB-C connector.
  - Dual role with Alternate Mode (DP IO).
- Refer to specific active mux vendor for detailed platform design guide and active mux settings.
- For USB3.1Gen2, the via stub length < 15mils.
- Via Anti-pad: Oval anti-pad size of 40mils is required for better impedance matching (see figure below).

**Figure 20-18.Oval Anti-pad**

## 20.3.3 USB Type-C with DP* as Alternate Mode

USB Type-C connector support DP Alternate Mode where you can have:

- Concurrent USB 3.1 (Gen1 or Gen2) data stream with DP x 2 display stream
- Concurrent USB 2.0 (LS/FS/HS) data stream with DP x 4 display stream utilizing all the differential pairs on the connectors

In DP Alternate Mode SBU1/SBU2 will be connected to DP AUX+/DP AUX- signal to support DP functionality. DP HPD signal will leverage CC communication as hot plug detect. HPD is from EC which is connected to CC lines through port controller.

ESD protection devices is required for all signal connecting to Coffee Lake directly. For signals that are connected to 3rd party component like MUX/controller, refer to 3rd Party component specification to decide if platform level ESD device is needed.

CMC may be required to pass EMI test therefore a CMC footprint is recommended.

**Figure 20-19.USB 3.1 and DP x 2 USB Type-C Connector Mapping (Right Side Up)**

**Figure 20-20.USB 3.1 and DP x 2 USB Type-C Connector Mapping (Up Side Down)**

**Figure 20-21.USB 3.1 and DP x 2**

***Note:*** The figure above is a high level example implementation block. The actual implementation on schematic may vary.

AC Cap might be needed on RX lines depending on Redriver/Repeater. Suggest to follow recommendation from Redriver.

## Figure 20-22.USB and DP x 4 USB Type-C Connector Mapping (Right Side Up)

## Figure 20-23.USB and DP x 4 USB Type-C Connector Mapping (Up Side Down)

## Figure 20-24.USB 3.1 and DP x 4 Discrete Solution

***Note:*** The figure above is a high level example implementation block actual implementation on schematic may vary.

AC Cap might be needed on RX lines depending on Redriver/Repeater. Suggest to follow recommendation from Redriver vendor.

An active mux should be used. Intel(R) DCI OOB over passive mux will not be supported.

Post-channel length (total length after active mux) is restricted to 1” (see figure below)

**Figure 20-25.System Design Example with USB Type-C Supporting DP as Alternate Mode**

***Notes:***
1. USB 2.0 PCB length up to 13" (pre- and post-channels)
2. USB 3.1 Gen2 PCB length up to 10" (pre-channel)
3. DisplayPort PCB length up to 8" (pre-channel)

**Figure 20-26.DP over USB-C- External Topology**

## Table 20-14. Routing Guidelines- DP over USB-C External- B Topology

| Parameter | Segment | Stackup | Length (mm) | Length (mils) |
|---|---|---|---|---|
| Trace length maximum | B0 | MS/SL/DSL | 12.7 | 500 |
| Trace length maximum | M1 | MS/SL/DSL | 190.5 | 7500 |
| Trace length maximum | Muxl | MS | 190.5 | 7500 |
| Trace length maximum | LC to LF | MS | 50.8 | 2000 |
| Total trace length maximum | Total | MS | 228.6 | 9000 |
| Maximum number of vias | | | | 2 |

***Notes:***
1. Crx capacitor value 297nF to 363nF, 25v.
2. Rb resistor value 220 kOhm ±5%.

## Figure 20-27. DP over USB-C- Internal Cable Topology

## Table 20-15. Routing Guidelines- DP over USB-C- Internal Cable Topology

| Parameter | Segment | Stackup | Length (mm) | Length (mils) |
|---|---|---|---|---|
| Trace length maximum | B0 | MS/SL | 12.7 | 500 |
| Trace length maximum | M1+M2 | MS/SL/DSL | 177.8 | 7000 |
| Trace length maximum | M3 | MS/SL/DSL | 25.4 | 1000 |
| Trace length maximum | M4+M5+M6+M7 | MS/SL/DSL | 25.4 | 1000 |
| Total trace length maximum | Total | MS | 241.3 | 9500 |
| Maximum vias allowed | | | | 3 |

***Notes:***
- Active Mux Assumption: With embedded mux/switch. Design guidelines may differ across multiple 3rd party devices. Refer to specific 3rd party vendor for details on platform design guideline and the corresponding device's setting.
- AC Capacitor Values: nominal 100 nF recommended (tolerance 75 nF to 265 nF)
- Reference Plane: Continuous Ground Only
- Internal Cable Insertion Loss Assumption: 1.2dB at 2.5GHz, 3.3dB at 5GHz
- Crx capacitor value 297nF to 363nF, 25v.
- Rb resistor value 220 kOhm ±5%.

**Figure 20-28.DP AUX over USB-C- External Topology**

**Table 20-16. Routing Guidelines- DP AUX over USB-C- External Topology**

| Parameter | Segment | Stackup | Length (mm) | Length (mils) |
|---|---|---|---|---|
| Trace length maximum | B0 | MS/SL | 20.3 | 800 |
| Trace length maximum | M1+M2 | MS/SL/DSL | 330 | 13000 |
| Trace length maximum | M3+M4 | MS/SL/DSL | 25 | 984 |
| Total trace length maximum | Total | MS | 330 | 13000 |

**Figure 20-29.DP AUX over USB-C- Internal Cable Topology**

**Table 20-17. Routing Guidelines- DP AUX over USB-C- Internal Cable Topology**

| Parameter | Segment | Stackup | Length (mm) | Length (mils) |
|---|---|---|---|---|
| Trace length maximum | B0 | MS/SL | 20.3 | 800 |
| Trace length maximum | M1+M2+M3+M4 | MS/SL/DSL | 330 | 13000 |
| Trace length maximum | M5+M6 | MS/SL/DSL | 25 | 984 |
| Trace length maximum | Mcable | | 178 | 7007 |
| Total trace length maximum | Total | MS | 330 | 13000 |

# 20.4 USB Type-C Power Delivery

## 20.4.1 USB Type-C VBUS and VCONN Control

Since USB PD may be supported on a USB Type-C connector, VBUS on the connector could be 5V, 9V, 15V or 20V. It is critical not to share VBUS with any other USB connectors as the operating VBUS may be different.

A Buck boost charger will be needed to support charging (Consumer mode) with different voltages (5V to 20V).By default VBUS on a USB Type-C connector shall be off before a DFP or UFP is connected and established. Therefore additional logic will be

needed to control VBUS on a USB Type-C connector to switch on only when needed. As for VCONN, once a valid devices/cable is plugged in the unconnected CC pin will be reconfigured to VCONN.

**Figure 20-30.USB-C PD System Block Diagram for Clamshell Design**

***Note:*** This sample block diagram is for a USB configuration capable of providing up-to 5V@3A VBUS. This also uses buck-boost charger to allow sink 5-20V through VBUS. Actual implementation might vary.

## 20.4.2 USB Type-C VBUS Options

USB Type-C connector supports multiple power options as below:

- Default USB Power
- 1.5A @ 5V
- 3.0A @ 5V
- USB PD

For Default USB Power, USB Type Power Delivery of 1.5A @5 V and 3.0A @5V, a DFP need to advertise the supported power options through pull up on the CC pins.

For USB PD, the power capability is advertised through the USB-C Port/PD Controller.

### 20.4.2.1 PTBB- PD Design Considerations

The PTBB (Powered Through Buck-Boost) charger block diagram is given below:

In this architecture, the TCPM shares the flash memory with the main system. The typical boot sequence is given below:

#0: USB-C port is attached as Sink and VBUS provides power to the TCPC. Source may start to advertise capabilities after VBUS=vSafe5V.

#1: Bypass VR is off.

#2: TCPC initializes and gets ready. TCPC may alert the host through I2C. TCPC sees that VDD is not present which indicates host is not present. TCPC autonomously turns on Sink path as host is not present after ~20ms. Note that TCPC should only turns on Sink path only with condition Rp≥1.5 and above.

#3: Buck-boost charger turns on. V3P3A (VR#1) starts power supply to EC, TCPC and PCH. V1P8A (VR#2) starts supply to PCH. EC initializes and loads FW code from the shared flash memory.

#4: EC decides to negotiate for higher VBUS voltage. EC turns on Bypass VR. EC sends request for higher VBUS voltage.

#5: EC commands TCPC to turn off the Sink path.

#6: EC receives Accept Msg and PS_RDY.

#7: EC may turn on Sink Path based on the negotiation

The power sequence timing diagram (G3 --> S4/S5) is shown below:

**Legend:**
1. VSYS: Output voltage from NVDC charger.
2. VDownstreamVR: Platform Power Rails (3.3V, 5V etc)

***Notes:***

1. While designing downstream VRs, please ensure the downstream VR's inrush power and loading is always lower than 6W. This is to prevent system from not being able to boot with USB-C charger during dead battery condition.

2. Tips to reduce inrush current
   a. Increase downstream VR ramp-up time
   b. Reduce downstream VR output capacitance.
   c. Add load switches to turn off unused downstream VRs.

## 20.5 Overcurrent Protection

Refer to USB 2.0 for OC protection circuit guidelines, and PCH EDS for pin mapping details.

# 20.6 Layout Optimization

## 20.6.1 CC Pins Layout

CC signals on USB Type-C is both a signal and a power depends on its connection, as the unconnected CC signal will become Vconn which is a power supply that can supply up to 0.3A @ 5V. It is recommended to have at least 10 mils trace width to reduce trace DC resistance and ensure a smooth power delivery when acting as Vconn. DC resistance need to be kept low so that Vconn does not fall below 4.75V which is the minimum voltage allow under USB Type-C specification. With 10 mils trace width, it is possible to route up-to 10 inch on a 1 oz copper layer while keeping the voltage >4.75V. On 1/2 oz copper layer, trace width will need to be >15 mils to achieve same result.

**Table 20-18. CC Signals Routing Guide**

| Trace Width | Copper thickness | Max Length |
|---|---|---|
| 0.254 mm | 1oz | 254 mm |
| 0.381 mm | 1/2 oz | 254 mm |

# 20.7 Type-C Connector Footprint Voiding Guideline

In order to minimize the impedance discontinuity at the connector connection to board, it is recommended to cut void at the connecting pins. Refer to figure below for sample of ground void in PTH or SMT pins.

**Figure 20-31. USB Type-C PTH Ground Void**

| | | |
|---|---|---|
| a | Finished hole radius | 0.40mm |
| b | Annular ring radius | 0.65mm |
| R | Antipad radius to PTH center | 1.00mm |
| P | Antipad center to center distance | 0.8mm |

**Figure 20-32.USB Type-C SMT Pins Ground Void**

## 20.8 USB Type-C Component Selection Guidelines

Refer to PCL for Intel recommended parts. The below figure shows the USB Type-C component considerations for the connector.

**Figure 20-33.USB Type-C Component Considerations**

## 20.9 Reference Documents

USB 3.1 Type-C USB-IF ECN Update: 575549

High Speed Internal Connector and Cable Specification (Intel Technical White-paper): 549136

Intel Channel Checker (ICC) for Client Re-driver CQC Analysis (Intel Software for Redriver Topology Analysis): 556174

USB 3.1 Specification (Industrial Specification): www.usb.org

USB 3.1 Internal Cable and Connector Implementation (Industrial Specification): www.usb.org

Compliance (Industrial Specification): www.usb.org

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# 21 PCH Signal Glitch Free Implementation Requirements

## 21.1 Overview

Certain PCH signals require special board implementation to ensure glitch free operation during boot process. Failure to meet the requirements may cause the signals to glitch during power sequencing and negatively impact the PCH behavior as well as external devices.

## 21.2 Implementation Details

Table 21-1, Table 21-2, and Table 21-3 below summarize the requirements.

Different options (implementing pull-down resistors or capacitors) are provided to meet the requirements. The options are intended for board implementation flexibility. For some signals, a cap or resistor site is recommended for board prototype designs and the site can be removed later on if not needed.

For the cap implementation option, the cap value depends on the 3.3V ramp rate of the VR on the motherboard, regardless of the signals being in 3.3V or 1.8V signaling mode.

For the pull-down resistor option, the resistor value depends on the signaling mode of the signal (3.3V or 1.8V).

**Table 21-1. Signals Required Cap or Pull-Down Resistor**

| Signal Name | Option 1 (Cap Implementation) | | Option 2 (Pull-down Resistor Implementation) | | Note |
|---|---|---|---|---|---|
| | 3.3v Ramp Rate from 5-50ms | 3.3V Ramp Rate Less than 5ms | 3.3V Signaling Mode | 1.8V Signaling Mode | |
| GPD4 / SLP_S3#<br>GPD5 / SLP_S4#<br>GPD6 / SLP_A#<br>GPD9 / SLP_WLAN#<br>SLP_SUS#<br>SLP_LAN# | 330 nF | 33 nF | 100 K | 75K | Cap or pull-down resistor is required |
| SPI0_CLK | N/A | N/A | 100K | 75K | Pull-down resistor is required. |

## Table 21-2. Signals Recommended with Cap or Pull-down Resistor Sites

| Signal Name | Option 1 (Cap Implementation) | Option 2 (Pull-down Resistor Implementation) | Note |
|---|---|---|---|
| GPD10 / SLP_S5#<br>GPP_A14 / SUS_STAT# / ESPI_RESET | Cap site | Pull-down resistor site | Site for cap or pull-down resistor only. |
| GPP_B13 / PLTRST#<br>HDA_BCLK / I2S0_SCLK<br>HDA_RST# / I2S1_SCLK<br>I2S1_SFRM / SNDW2_CLK | N/A | Pull-down resistor site | Site for pull-down resistor only. |

## Table 21-3. Signals Required Pull-up Resistor

| Signal Name | Pull-Up Resistor Value | Note |
|---|---|---|
| GPP_A7 / **PIRQA#** / ESPI_ALERT0# | An external Pull-up 8.2 KΩ ~10 KΩ to V3.3S power rail is required. | Pull-up resistor is required. |
| GPP_B12/SLP_S0# | 3.3V Signaling Mode - 100K<br>1.8V Signaling Mode - 75K | Pull-up resistor is required if a device is monitoring SLP_S0# before RSMRST# de-assertion |

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# 22 MIPI SoundWire* Interface Design Guidelines

For Coffee Lake platform, the SoundWire interface is a new emerging interface targeting (but not limited to) the phone, mobile, and desktop market as an alternative to Slimbus. Its main advantage is the connection simplicity with a 2 wire multi-drop topology + PDM streaming capabilities. For the Cannon Lake PCH there are 4 separate SoundWire* interfaces that can be used.

## 22.1 SoundWire Platform Specific Important Information

On Coffee Lake platform the SoundWire interface pins are partially multiplexed with legacy DMIC, I2S, and HD-A audio interfaces. The SoundWire interface and other audio can be configured as either (and in some cases simultaneously) for connection to end devices. See the Cannon Lake PCH EDS for specific sku pins assignments and multiplexing details.

## 22.2 SoundWire Signal Description

**Table 22-1. SoundWire Signals**

| Signal Name | Description |
|---|---|
| SNDW1_DATA | SoundWire Data 1: Serialized data line containing frame and data being transmitted /Received |
| SNDW1_CLK | SoundWire Clock 1: Serial bit clock used to control the timing of a transfer. |
| SNDW2_DATA | SoundWire Data 2: Serialized data line containing frame and data being transmitted /Received |
| SNDW2_CLK | SoundWire Clock 2: Serial bit clock used to control the timing of a transfer. |
| SNDW3_DATA | SoundWire Data 3: Serialized data line containing frame and data being transmitted /Received |
| SNDW3_CLK | SoundWire Clock 3: Serial bit clock used to control the timing of a transfer. |
| SNDW4_DATA | SoundWire Data 4: Serialized data line containing frame and data being transmitted /Received |
| SNDW4_CLK | SoundWire Clock 4: Serial bit clock used to control the timing of a transfer. |

## 22.3 SoundWire Topology Guidelines

There are several topologies supported in Coffee Lake for SoundWire:

- Large System Topology - Single Load Configuration Using Cables.
- Large System Topology - Single Load Configuration with Device Down.

The following subsections outlines the routing requirements for each topology

### 22.3.1 Large System Topology - Single Load Configuration Using Cables

**Figure 22-1. SNDW1_DATA to SNDW4_DATA/ SNDW1_CLK to SNDW4_CLK Single Cabled Load Configuration Diagram**

**Table 22-2. SNDW1_DATA to SNDW4_DATA/ SNDW1_CLK to SNDW4_CLK Single Cabled Load Routing Guidelines**

| Parameter[1] | Segment | Stack-up | Units | Recommendation |
|---|---|---|---|---|
| Maximum Trace Length | BO | MS/SL/DSL | mils | 500 |
| Maximum Trace Length | M1 | MS/SL/DSL | mils | 7480.31 |
| Maximum Trace Length | M2 | MS/SL/DSL | mils | 5905.51 |
| Cable Length Maximum | M-Cable[3] | NA | mils | 13779.53 |
| Overall Length Maximum | B0+M1+M-Cable+M2 | MS/SL/DSL | mils | 27665.35 |
| Resistor Minimum Distance from PCH | R1 | MS/SL/DSL | mils | 500 |
| Trace Length Mismatch Maximum between Clock and Data | NA | NA | mils | 200 |
| Resistor Value | R1 | NA | Ω | 22 |
| Max Vias Single Load | NA | NA | count | 4 |
| Maximum Operating Frequency Single Load | NA | NA | MHz | 6 |
| Port# supported in this configuration | NA | NA | # | 1, 2, 3, and 4 |
| End Device Buffer Impedance Target | NA | NA | Ω | 90 |
| PCH Buffer | NA | NA | Type | HDA and GPPD |
| PCH Buffer Impedance Target[2] | NA | NA | Ω | 50 |

1. Routes should be referenced to GND for entire route.
2. The buffer impedance target should be 50ohm, slew 00. Refer to the EDS/BIOS programming guide for more details.
3. Cable characteristic impedance target to 50 Ω ±5%. Simulation analysis covers characteristic impedance of 45-60 Ω including cable manufacturing tolerance.

### 22.3.2 Large System Topology - Single Load Configuration with Device Down

**Figure 22-2. SNDW1_DATA to SNDW4_DATA/ SNDW1_CLK to SNDW4_CLK Single Load Device Down Configuration Diagram**

**Table 22-3. SNDW1_DATA to SNDW4_DATA/ SNDW1_CLK to SNDW4_CLK Single Load Down Device Routing Guidelines**

| Parameter[1] | Segment | Stack-up | Units | Recommendation |
|---|---|---|---|---|
| Maximum Trace Length | BO | MS/SL/DSL | mils | 500 |
| Maximum Trace Length | M1 | MS/SL/DSL | mils | 18897.60 |
| Overall Length Maximum | B0+M1 | MS/SL/DSL | mils | 19397.60 |
| Resistor Minimum Distance from PCH | R1 | MS/SL/DSL | mils | 500 |
| Trace Length Mismatch Maximum between Clock and Data | NA | NA | mils | 200 |
| Resistor Value | R1 | NA | Ω | 22 |
| Max Vias Single Load | NA | NA | count | 4 |
| Maximum Operating Frequency Single Load | NA | NA | MHz | 6 |
| Port# supported in this configuration | NA | NA | # | 1, 2, 3, and 4 |
| End Device Buffer Impedance Target | NA | NA | Ω | 90 |
| PCH Buffer | NA | NA | Type | HDA and GPPD |
| PCH Buffer Impedance Target[2] | NA | NA | Ω | 50 |

1. Routes should be referenced to GND for entire route.
2. The buffer impedance target should be 50ohm, slew 00. Refer to the EDS/BIOS programming guide for more details.

# 22.4 Additional Guidelines

## 22.4.1 Adjusting Drive Impedance for Down Devices

In the topology section device buffer strength target recommendations are different depending on the Topology and its configuration. If devices used do not have buffer strengths that match the target recommendations and do not have the ability to adjust the buffer strengths through software you can adjust the impedance via an external resistor as shown in Figure 22-3. To determine R1 the formula is: R1=Device Buffer Impedance Target - Actual Device Buffer Impedance.

Example:

- Device Drive Impedance Target = 80ohms
- Device Buffer Impedance = 45ohm
- R1 = 80ohm - 45ohm = 35ohm

**Figure 22-3. SoundWire Device Drive Impedance Adjustment**

**Table 22-4. SoundWire Device Drive Impedance Guidelines**

| Parameter[1] | Segment | Stack-up | Units | Recommendation |
|---|---|---|---|---|
| Trace Length Maximum | M1 | MS | mils | 393.7 |
| 1. Routes should be referenced to GND for entire route. | | | | |

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# 23 I²C* Interface Design Guidelines

PCH includes four I²C* controllers, providing four independent I²C interfaces. Each interface is a two-wire I²C serial interface consisting of a serial data line and a serial clock.

Each I²C interface supports standard mode (up to 100 Kb/s), fast mode (up to 400 Kb/s), fast mode plus (up to 1 Mb/s) and High speed mode (up to 3.2 Mb/s). Devices supporting standard mode and/or fast mode cannot be connected to the same I²C bus where devices supporting fast mode plus and/or High speed mode are connected.

The I²C interface can support 1.8 V or 3.3 V depending on devices connected to it.

For information on what OS the I²C interface supports, refer to the Intel® Serial I/O Driver PRD documentation.

## 23.1 I²C Platform Specific Important Information

**Table 23-1. Reference Specifications**

| Title |
|---|
| I²C Specification Version 5 |

### 23.1.1 I²C Signal Descriptions

#### 23.1.1.1 Signal Groups

**Table 23-2. I²C* Signals**

| Group | Signal Name | Description |
|---|---|---|
| Clock | I2C[3:0]_SCL | I²C clock signals |
| Data | I2C[3:0]_SDA | I²C data signals |

### 23.1.2 I2C Topology Guidelines

#### 23.1.2.1 General Design Considerations

I²C bus is a multi-device bus (i.e. more than one device can be connected to an I²C bus). The total number of devices connected to the bus is determined by the total capacitive load on the bus. The maximum bus capacitive load for each I²C bus is 400 pF and cannot be exceeded.

I²C clock and data signals require pull-up resistors. There is an internal pull-down resistor, and current assist which can be selected through registers based on the bus capacitive load including devices leakage currents (refer EDS for leakage current). See Table 23-5 for recommendations on pull-up / pull-down resistors and current assist depending on bus capacitance and I²C speed mode.

Do not mix and match devices supporting 100 kHz / 400 kHz speed with the one supporting 1 MHz/3.2 MHz on the same I²C bus.

I²C signals are multiplexed with GPIOs and default to GPIO functionality (as input). If I²C interfaces are not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

### 23.1.2.2 Detailed Routing Requirements

The table below shows detailed routing requirement for I²C bus. Since I²C trace length is dependent on total capacitance of the bus, the designer needs to consider the number and types of I²C devices on each I²C bus. See table below for guidance on trace capacitance.

**Table 23-3. I²C* Signal Routing Summary**

| Parameter | Routing Recommendation (in mils) | Routing Recommendation (in mm) |
|---|---|---|
| Trace Spacing between SCL and other signal (>1GHz) | 15 | 0.381 |
| Trace Spacing between SCL and other signal (>100MHz) | 10 | 0.254 |
| Trace Spacing between SCL and other signal (<1MHz) | 5 | 0.127 |
| Trace Spacing between SDA and other signal | 5 | 0.127 |
| Characteristic Impedance | 30 to 70Ω | |
| Maximum number of Vias allowed | 7 | |

Refer to Chapter 2, "Stack-Up and PCB Considerations" for other details like Trace Width, Trace Spacing, Breakout Width, Breakout Spacing etc.

I²C clock and data signals must be length matched within 1000 mils (25.4 mm).

System designers must consider the total bus capacitance which includes both package and device pin capacitance and board trace length capacitance when designing I²C bus. The total bus capacitance must not exceed 100 pF for High Speed Mode and 400pF for other modes (Standard/Fast/Fast mode plus). Tables below provides information to help determine total bus capacitance and proper internal pull-down resistor/current assist on the I²C buses.

**Table 23-4. Bus Capacitance Reference Chart**

| Device | Capacitance Includes | Units | Capacitance |
|---|---|---|---|
| PCH Pin Capacitance | Pin Capacitance | pF | 8 to 10 |
| Device Pin Capacitance | Pin Capacitance | pF | 5 to 10 |
| Board Trace per Inch | per inch of trace length | pF | 2 to 5 |

Trace Capacitance per inch is approximately equal to 85√ϵr / Zo (in pF) where, ϵr is Dielectric constant of material, Zo is Trace impedance

## Table 23-5. Bus Capacitance / Pull-Up and Current Assist Strength Settings

| I2C Standard Mode (100kHz) - Mode Pull-up / Pull-down /Pull down and Current Assist Strength Settings | | | | |
|---|---|---|---|---|
| **Total Bus Capacitance ($C_b$)** | **Internal Pull -up (Refer EDS)** | **External Pull-up** | **PCH Pull Down Strength (Refer EDS)** | **Current Assist** |
| Upto 50pF | None | 18kΩ | 100Ω | None |
| Upto 100pF | None | 10kΩ | | None |
| Upto 200pF | None | 4.7kΩ | | None |
| Upto 300pF | None | 3.3kΩ | | None |
| Upto 400 pF | None | 2.2KΩ | | None |
| **I2C Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings** | | | | |
| **Total Bus Capacitance ($C_b$)** | **Internal Pull -up (Refer EDS)** | **External Pull-up** | **PCH Pull Down Strength (Refer EDS)** | **Current Assist** |
| Upto 50pF | None | 5.6kΩ | 100Ω | None |
| Upto 100pF | None | 2.7KΩ | | None |
| Upto 200pF | None | 1.5KΩ | | None |
| 50pF to 300pF | None | 1KΩ | | None |
| 50pF to 400pF | None | 680Ω | | None |
| **I2C Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings** | | | | |
| **Total Bus Capacitance ($C_b$)** | **Internal Pull -up (Refer EDS)** | **External Pull-up** | **PCH Pull Down Strength (Refer EDS)** | **Current Assist** |
| Upto 50pF | None | 2.2kΩ | 100Ω | None |
| Upto 100pF | None | 1.2kΩ | | None |
| Upto 200pF | None | 560Ω | | None |
| Upto 300pF | None | 390Ω | 67Ω | None |
| Upto 400 pF | None | 270Ω | 50Ω | None |
| **I2C High Speed mode -SDA (1.7MHz) Pull-up/Pull down and Current Assist strength Settings** | | | | |
| **Total Bus Capacitance ($C_b$)** | **Internal Pull -up (Refer EDS)** | **External Pull-up** | **PCH Pull Down Strength (Refer EDS)** | **Current Assist** |
| Upto 50pF | None | 2.2kΩ | 100Ω | None |
| 50pF to 100pF | None | 1.2kΩ | | None |
| 50pF to 200pF | None | 560Ω | | None |
| 100pF to 300pF | None | 330Ω | | None |
| 100pF to 400pF | None | 270Ω | 50Ω | None |

## Table 23-5. Bus Capacitance / Pull-Up and Current Assist Strength Settings

| I2C High Speed mode -SCL (1.7MHz) at 1.8V Pull-up /Pull down and Current Assist strength Settings | | | | |
|---|---|---|---|---|
| **Total Bus Capacitance ($C_b$)** | **Internal Pull -up (Refer EDS)** | **External Pull-up** | **PCH Pull Down Strength (Refer EDS)** | **Current Assist** |
| Upto 55pF | None | 1.5kΩ | 100Ω | 000 |
| 45pF to 150pF | None | 560Ω | | 000 |
| 100pF to 200pF | None | 330Ω | 50Ω | 000 |
| 150pF to 325pF | None | 330Ω | | 001 |
| 300pF to 400pF | None | 330Ω | | 010 |
| **I2C High Speed mode -SCL(1.7MHz) at 3.3V Pull-up/Pull-down and Current Assist strength Settings** | | | | |
| **Total Bus Capacitance ($C_b$)** | **Internal Pull -up (Refer EDS)** | **External Pull-up** | **PCH Pull Down Strength (Refer EDS)** | **Current Assist** |
| Upto 55pF | None | 1.5kΩ | 100Ω | 000 |
| 45pF to 150pF | None | 560Ω | | 000 |
| 100pF to 200pF | None | 330Ω | 50Ω | 000 |
| 150pF to 275pF | None | 330Ω | | 001 |
| 200pF to 400pF | None | 330Ω | | 010 |
| **I2C High Speed mode -SDA (3.2 MHz) Pull-up /Pull down and Current Assist strength Settings** | | | | |
| **Total Bus Capacitance ($C_b$)** | **Internal Pull -up (Refer EDS)** | **External Pull-up** | **PCH Pull Down Strength (Refer EDS)** | **Current Assist** |
| Upto 20pF | None | 3.9kΩ | 100Ω | None |
| 20pF to 40pF | None | 1.5kΩ | | None |
| 25pF to 60pF | None | 1.2kΩ | | None |
| 30pF to 80pF | None | 1kΩ | | None |
| 35pF to 100 pF | None | 820Ω | | None |
| **I2C High Speed mode -SCL (3.2 MHz) at 1.8V Pull-up /Pull down and Current Assist strength Settings** | | | | |
| **Total Bus Capacitance ($C_b$)** | **Internal Pull -up (Refer EDS)** | **External Pull-up (Refer EDS)** | **PCH Pull Down Strength** | **Current Assist** |
| Upto 35pF | None | 1.2kΩ | 100Ω | 000 |
| 30pF to 50pF | None | 820Ω | | 000 |
| 45pF to 85pF | None | 820Ω | | 001 |
| 80pF to 100pF | None | 820Ω | | 010 |

**Table 23-5. Bus Capacitance / Pull-Up and Current Assist Strength Settings**

| I2C High Speed mode -SCL (3.2 MHz) at 3.3V Pull-up /Pull down and Current Assist strength Settings | | | | |
|---|---|---|---|---|
| Total Bus Capacitance ($C_b$) | Internal Pull -up (Refer EDS) | External Pull-up (Refer EDS) | PCH Pull Down Strength | Current Assist |
| Upto 35pF | None | 1.2kΩ | 100Ω | 000 |
| 30pF to 50pF | None | 820Ω | | 000 |
| 40pF to 70pF | None | 820Ω | | 001 |
| 60pF to 100pF | None | 820Ω | | 010 |

***Note:*** Multiple options for Pull-up/pull-down and current assist strengths are provided for a particular Total bus capacitance. Choose the optimal value for system based on design considerations like power, BOM cost.

## 23.1.3 Tools

Intel does not promote any specific tool for this interface.

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# 24 Universal Asynchronous Receiver Transmitter (UART) Interface Design Guidelines

## 24.1 UART Platform Specific Important Information

The platform integrates three Universal Asynchronous Receiver Transmitter (UART) controllers. Each supports up to 3.8 Mbit/s. The controllers can be used in the low-speed, full-speed, and high-speed modes. The controllers are based on the 16550 industry standard and communicates with serial data ports that conform to the RS-232 interface protocol.

For information on what OS the UART interface supports, refer to the Intel® Serial I/O Driver PRD documentation.

***Note:*** Bluetooth* devices are not supported on the PCH UART interfaces.

### 24.1.1 UART Signal Descriptions

**Table 24-1. UART Signals**

| Group | Signal Name | Description |
|---|---|---|
| Data | UART[2:0]_RXD | Receive Data Input signals |
| | UART[2:0]_TXD | Transmit Data Output signals |
| Control | UART[2:0]_RTS# | Request to Send signals |
| | UART[2:0]_CTS# | Clear to Send signals |

### 24.1.2 UART Topology Guidelines

This section contains information and details for layout and routing guidelines for the UART interfaces.

**Figure 24-1. UART Topology**

**Table 24-2. UART Routing Guideline for Motherboard**

| Parameter | Stack-up | Routing Recommendation (in mm) | Routing Recommendation (in mils) |
|---|---|---|---|
| M1 - Trace Length | MS/DSL | 25-165 | 1000-6500 |
| BO - Max Breakout Length | MS/DSL | 12.7 | 500 |
| Trace spacing between DATA and DATA | - | 0.127 | 5 |
| Maximum number of Vias | | 7 | |

Refer to Chapter 2, "Stack-Up and PCB Considerations" for other details like Trace Width, Trace Spacing, Breakout Width, Breakout Spacing etc.

## 24.1.3 Tools

Intel does not promote any specific tool for this interface.

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# 25 Generic Serial Peripheral Interface (GSPI)

## 25.1 GSPI Platform- Specific Important Information

The PCH's three generic SPI (GSPI) interfaces support devices which use SPI serial protocols for transferring data.

Each interface consists of 4 wires: a clock (CLK), two chip select (CS) and 2 data lines (MOSI and MISO).

The PCH generic SPI is full-duplex synchronous serial interface. The interface operates in master mode only, and supports serial bit rate up to 25Mb/s. Serial data formats may range from 4 to 32 bits in length.

Note that the GSPI is not the same as the PCH SPI interface for flash devices. This GSPI is used mainly for sensor support on the platform.

### 25.1.1 GSPI Signal Descriptions

#### 25.1.1.1 Signal Groups

**Table 25-1. GSPI Signals**

| Group | Signal Name | Description |
|---|---|---|
| Clock | GSPI0_CLK<br>GSPI1_CLK<br>GSPI2_CLK | Clock signals |
| Data | GSPI0_MISO<br>GSPI1_MISO<br>GSPI2_MISO | Master In Slave Out signals |
| | GSPI0_MOSI<br>GSPI1_MOSI<br>GSPI2_MOSI | Master Out Slave In signals |
| Chip Select | GSPI0_CS0#<br>GSPI0_CS1#<br>GSPI1_CS0#<br>GSPI1_CS1#<br>GSPI2_CS0#<br>GSPI2_CS1# | Chip select signals |

### 25.1.2 GSPI Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for the generic SPI interfaces.

**Figure 25-1. GSPI Topology**

Series Resistor R1 mentioned in the above GSPI topology should have recommended value of 33 ohm if operated in 3.3V mode, else 0 ohm if operated in 1.8V mode.

R1 is recommended to be placed 12.7 mm (500 mils) from the PCH, but can be extended to 50.8mm (2000 mils) maximum if required. The length of breakout section BO is still 12.7 mm (500 mils) maximum

**Table 25-2. GSPI Routing Guideline for CFL PCB**

| Parameter | Stack-up | Routing Recommendation (in mm) | Routing Recommendation (in mils) |
|---|---|---|---|
| M1 - Max Trace Length | MS/SL/DSL | 203 | 8000 |
| M1 - Trace Spacing between | MS/SL/DSL | Clock and others:0.381<br>Data and Data: 0.127 | Clock and others:15<br>Data and Data: 5 |
| BO - Max Breakout Length | MS/SL/DSL | 12.7 | 500 |
| Clock and Data Signal Length Mismatch | MS/SL/DSL | <12.7 | < 500 |
| R - Pull-up Resistor | | - 50Kohms on GSPI[2:0]_CS[1:0]#, GSPI[2:0]_CLK and GSPI[2:0]_MISO<br>- 150Kohms on GSPI[2:0]_MOSI if the default functional strap on the signal is desired (low), or 4.7Kohms pull-up resistor if the functional strap needs to be high. | |
| Maximum number of Vias allowed | | 7 | |
| Reference Plane | | Continuous Ground | |

## 25.1.3 Debug Guidelines/Recommendations

GSPI signals are multiplexed with GPIOs and default to GPIO functionality. If GSPI interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

## 25.1.4 Tools

Intel does not promote any specific tool for this interface.

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# 26 Enhanced Serial Peripheral Interface (eSPI)

## 26.1 Introduction

The Enhanced Serial Peripheral Interface (eSPI) provides an alternative for connecting an EC to the platform (besides the LPC interface). Note that LPC and eSPI co-exist on the platform but only one interface can be enabled at a time via a hardware strap.

eSPI operates at 1.8V only and supports one slave device. This interface is not shared and distinct from the SPI interface used for flash device and TPM. The eSPI interface supports 20 MHz, 24MHz, 30 MHz, 48 MHz, and 60 MHz and up to Quad Mode.

**Table 26-1. eSPI Signals**

| Signal Name | Group | Description |
|---|---|---|
| ESPI_IO[3:0] | Data | Bi-directional data signals used to transfer data between CFL and eSPI slave device |
| ESPI_CLK | Clock | eSPI Clock output from PCH |
| ESPI_CS0# | Control | eSPI chip selects |
| ESPI_RESET# | Control | eSPI reset signal |

## 26.2 Topology and Guidelines

### 26.2.1 Topology

The eSPI interface supports single load topology or dual load as illustrated below.

**Figure 26-1. eSPI Single Load Topology**

## 26.2.2 Routing Guidelines

### 26.2.2.1 Single Load Topology Guidelines

Single load topology supports up to 60 MHz.

CS# and Reset signals do not require series resistors.

**Figure 26-2. eSPI Single Load Topology**

**Table 26-2. eSPI Single Load Routing Guidelines**

| Segment / Parameter | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL | VSS | 1 | 12.7 | 165.6 | 500 | 6519.69 |
| M1 | MS | VSS | 1 | 12.7 | | 500 | |
| M2 | MS | VSS | 0 | 0.5 | | 19.69 | |
| M3 | MS/SL/DSL | VSS | 1 | 127 | | 5000 | |
| M4 | MS | VSS | 1 | 12.7 | | 500 | |
| | | | | | | | |
| R1 | For DATA lines: If B0+M1+M2+M3+M4 are full microstrip routing, R1 = 15 Ohm. Otherwise, R1 = 0 Ohm<br>For Clock line: R1 = 33 Ohm<br>R1 is recommended to be placed 12.7mm (500mils) from the PCH, but can be extended to 25.4mm (1000mils)if required | | | | | | |
| Max Via Allowed | 7 | | | | | | |
| Reference plan | Continuous ground only | | | | | | |

### 26.2.2.2 eSPI Length Matching and Spacing Requirement

- eSPI clock and eSPI data must be length matched to within 500 mils (12.7mm).
- eSPI clock and eSPI CS# must be length matched to within 1000 mils (25.4mm).
- Trace spacing between DATA and DATA is 5 mils (0.127mm)
- Trace spacing between CLK and other signals is 15 mils (0.381mm)

### 26.2.2.3 Other Design Considerations

#### 26.2.2.3.1 Voltage Supply

The eSPI signals are multiplexed with Group A GPIOs (GPP_A). This signal group is powered by VCCPGPPA power pin. Since eSPI interface only supports 1.8V, the VCCPGPPA power pin must be connected to 1.8V when eSPI is utilized on the platform. Note that, in this case, all the signals in Group A GPIO (both as GPIO and native functionality) will operate at 1.8V. Designer should take this into account when designing the motherboard.

#### 26.2.2.3.2 eSPI Design with 2 Chip Selects

On platforms designed with eSPI enabled and PCH SKU that supports 2 eSPI CS# (i.e. Intel® Z390 chipset), the following behavior needs to be taken into account:

- GPP_A7 / ESPI_ALERT0# and GPP_A0 / ESPI_ALERT1# pins default to ESPI_ALERT0# and ESPI_ALERT1# (native functions) with ~20K internal pull-ups.
- GPP_A6 / ESPI_CS1# pin defaults to ESPI_CS1# with ~20K internal pull-up before ESPI_RESET# deassertion and driven to logic high after ESPI_RESET# deassertion.

Depending on the number of chip select signals required, designers must follow the guidelines below:

1) If ESPI_CS1# is utilized to support 2 eSPI devices (i.e. ESPI_CS0#, ESPI_CS1#, ESPI_ALERT0#, and ESPI_ALERT1# are all used):

- The eSPI/ EC Slave Device Enable soft strap needs to be configured to 1 (ESPI_CS1# is enabled)
- No external termination is required on the pins

2) If ESPI_CS1# is NOT utilized (i.e. only ESPI_CS0# is used; ESPI_CS1#, ESPI_ALERT0#, and ESPI_ALERT1# are not used):

- The eSPI / EC Slave Device Enable soft strap needs to be configured to 0 (ESPI_CS1# is disabled)
- If GPP_A6 / ESPI_CS1#, GPP_A7 / ESPI_ALERT0# and GPP_A0 / ESPI_ALERT1# pins are not used, they can be left as no-connect.
- If GPP_A6 / ESPI_CS1#, GPP_A7 / ESPI_ALERT0# and GPP_A0 / ESPI_ALERT1# pins are used as GPIO function:
  - For GPP_A7 / ESPI_ALERT0# and GPP_A0 / ESPI_ALERT1#, take into consideration that the internal pull-ups (~20K) on the pins are ON until they are programmed to GPIO function.
  - For GPP_A6 / ESPI_CS1#, there must NOT be any on-board device driving the pin to opposite value (low) before the signal is programmed to GPIO function. Also take into consideration that the internal pull-up (~20K) is ON until the signal is programmed to GPIO function.

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# 27 SMBus 2.0/SMLink Interface Design Guidelines

## 27.1 SMBus 2.0/SMLink Platform Specific Important Information

### 27.1.0.1 SMBus Description

PCH integrates an SMBus 2.0 controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RAM, thermal sensors, PCI cards, etc. The slave interface allows an external micro controller to access system resources.

The SMBus interface on PCH uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used by the SMBus Host, SMBus Slave, and TCO Controllers. These controllers reside inside PCH.

### 27.1.0.2 SMLink Description

PCH incorporates two SMLink interfaces, SMLink0 and SMLink1. When the integrated LAN controller is used, the SMLink0 is a dedicated bus between PCH's LAN controller and the PHY to improve performance and reliability. The SMLink1 is dedicated for an external controller (EC) or a Baseboard Management Controller (BMC). The BMC may communicate with PCH via SMLink1 and to the TCO logic through the Host SMBus signals.

SMBus and SMlink connectivity recommendations are described in **Figure 27-1** and Figure 27-4 below.

***Note:*** The requirement to tie both SMLink and SMBus signals externally is not needed, as slave functionality is available on the SMBus pins.

## 27.1.1 SMBus 2.0/SMLink Signal Descriptions

### 27.1.1.1 Signal Groups

**Table 27-1. SMBus and SMLink Signals**

| Group | Signal Names | Description |
|---|---|---|
| Clock | SMBCLK<br>SML[1:0]CLK | SMBus/SM Link Clock signals |
| Data | SMBDATA<br>SML[1:0]DATA | SMBus/SMLink Data lines |
| ALERT | SMBALERT#<br>SML[1:0]ALERT# | SMBus/SMLink ALERT signals |

## 27.1.2 SMBus 2.0/SMLink Topology Guidelines

### 27.1.2.1 General Design Considerations

- The maximum bus capacitance is 400 pF.
- SMBus devices that can operate in S3 must be powered by the suspend power supply.
- It is recommended that $I^2C$ devices (used on SMBus in $I^2C$ enabled mode) be powered by the core power supply. During an SMBus transaction in which the device is sending information to PCH, the device may not release the SMBus if PCH receives an asynchronous reset. Core well power is used to allow BIOS to reset the device if necessary. SMBus 2.0-compliant devices have a timeout capability which makes them insusceptible to this $I^2C$ issue, allowing flexibility in choosing a voltage supply.
- If SMBus is connected to PCI, it must be connected to all PCI slots.
- If SMBus is connected to PCI Express*, it must be connected to all PCI Express slots.

## 27.1.3 Detailed Routing Requirements

The following table shows detailed routing requirement for SMBus and SMlink signal. However since SMBus and SMLink trace length is dependent on total capacitance of the system bus, designer need to take into consideration the number and types of SMBus devices/slots on the motherboards.

External pull up is required which is also based on the load capacitance and bus speed. Details are captured in the following tables.

Designer need to calculate the total capacitance for trace routing and the pins of each device connected on the bus.

### 27.1.3.1 Length Matching Requirements

Data and clock signal for SMBus and SMlink signal to each device needs to be length matched to 1000 mils (25.4 mm).

### Table 27-2. SMBus Length Matching Summary

| Parameter | Routing Recommendation (in mils) | Routing Recommendation (in mm) |
|---|---|---|
| Trace Spacing between SCL and other signal (>1GHz) | 15 | 0.381 |
| Trace Spacing between SCL and other signal (>100MHz) | 10 | 0.254 |
| Trace Spacing between SCL and other signal (<1MHz) | 5 | 0.127 |
| Trace Spacing between SDA and other signal | 5 | 0.127 |
| Characteristic Impedance | 30 to 70Ω | |
| Maximum number of Vias allowed | 7 | |

## 27.1.4 SMBus and SMLink Connectivity Recommendation

### Figure 27-1. SMBus / SMLink (TCO Legacy Mode)

**Figure 27-2. SMBus / SMlink Connectivity (Advanced TCO Mode)**

### 27.1.4.1 Monitoring Integrated Sensors Over SMLink1

SMBus protocol is defined to allow compatible devices, e.g., SIO or Embedded Controller (EC), to monitor the integrated sensors in the chipset. This solution provides system thermal data to external controller such as the Embedded Controller (EC) or SIO, which can be used for fan speed control, chipsets temperature monitoring and/or managing other cooling elements. The EC or SIO can also get an alert when a device has gone out of its temperature limits.

To implement this thermal monitoring over SMBus capability, the platform is required to have appropriate Intel® ME firmware and a compatible SIO/EC that supports the SMBus protocol.

The following figure illustrates the on board connectivity to support this capability.

**Figure 27-3. Connectivity for Thermal Monitoring over SMBus**

### 27.1.4.2 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate while in S3. Suspend power well leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a "FET" to isolate the devices powered by the core and suspend supplies. See Figure below:

**Figure 27-4. High Power/Low Power Mixed Vcc_SUSPEND / Vcc_CORE_ Architecture**

Added Considerations for Mixed Architecture:

- The bus bridge must be powered by suspend power well.
- Devices that are powered by the suspend power well must not drive into other devices that are powered off. This is accomplished with the "bus switch".
- The bus bridge can be a device like the Philips* PCA9515.

## 27.1.5 Additional Guidelines

### 27.1.5.1 SMBus Design Considerations

No single SMBus design solution will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add a significant amount of capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Device class (High/Low power). Most designs use primarily High Power Devices.
- Devices which must run in S3.
- Amount of suspend well current available, i.e., minimizing load of suspend power wells.

### 27.1.5.2 Calculating Physical Segment Pull-Up Resistor

The following tables are provided as a reference for deciding the value of the external pull-up resistor that should be used for a physical bus segment. If any physical bus segment exceeds maximum bus capacitance of 400 pF, then a bus bridge device like the Philips* PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than the maximum bus capacitance.

**Table 27-3. Bus Capacitance Reference Chart**

Trace Capacitance per inch is approximately equal to 85√єr / Zo (in pF) where, єr is Dielectric constant of material, Zo is Trace impedance.

| Device | Capacitance Includes | Units | Capacitance |
|---|---|---|---|
| PCH Pin Capacitance | Pin Capacitance | pF | 8 to 10 |
| Device Pin Capacitance | Pin Capacitance | pF | 5 to 10 |
| Board Trace per Inch | per inch of trace length | pF | 2 to 5 |

### Table 27-4. Bus Capacitance/Pull-Up Resistor Relationship

| Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings | | |
|---|---|---|
| **Total Bus Capacitance ($C_b$)** | **External Pull-up** | **PCH Pull Down Strength (Refer EDS)** |
| Upto 50 pF | 18KΩ | 100Ω |
| Upto 100 pF | 10KΩ | |
| Upto 200 pF | 4.7KΩ | |
| Upto 300 pF | 3.3KΩ | |
| Upto 400 pF | 2.2KΩ | |
| **Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings** | | |
| **Total Bus Capacitance ($C_b$)** | **External Pull-up** | **PCH Pull Down Strength** |
| Upto 50pF | 5.6KΩ | 100Ω |
| Upto 100pF | 2.7KΩ | |
| Upto 200pF | 1.5KΩ | |
| 50pF to 300pF | 1KΩ | |
| 50pF to 400pF | 680Ω | |
| **Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings** | | |
| **Total Bus Capacitance ($C_b$)** | **External Pull-up** | **PCH Pull Down Strength** |
| Upto 50pF | 2.2KΩ | 100Ω |
| Upto 100pF | 1.2KΩ | |
| Upto 200pF | 560Ω | |
| Upto 300pF | 390Ω | 67Ω |
| Upto 400 pF | 270Ω | 50Ω |

### 27.1.5.3 Intel® Trace Hub Backup: SMBus Test Points

Background: Intel Trace Hub is a new concept/mechanism, used to transport messages from the SoC to external monitor through a USB connector. This concept is defined as "Closed Chassis" message transport, without the need to open the chassis.

The Intel® ME is one of the entities using the Intel Trace Hub to provide debug data to the external monitor. However, since the Intel Trace Hub is a new technology, the following design guidelines act as a **backup** solution to route the debug information to an external SMBus Sniffer. **It is highly recommended that the SMBus Test Points are implemented**, so the customer or Intel debug team will be able to collect debug data from the system.

To quickly attach the SMBus sniffer to the platform, the following items should be added:

- Clearly marked (Silk-screen) SMBus test points, preferably, holes for 0.1" header (3 pins: SMBDATA, SMBCLK and GND), connected directly to the **SoC SMBus pins**.

  **Note:** These Test points will be used to hook up to a SMBus sniffer that will impose an additional 60 pF load capacitance. The value of the SMBus external pull up resistor should be calculated with this additional 60 pF load to ensure that the sniffer and the SMBus will continue to operate normally when the sniffer is plugged in. If the total SMBus section capacitance is equal to or less than 400 pF after adding this 60 pF, no other change is required. In case the final SMBus section capacitance is larger than 400 pF, the SMBus will need a bridge to separate the bus into 2 sections with <400 pF capacitance each.

- Accessing the Test Points to hook the sniffer should be simple. It is recommended that the SMBus Test points be easily accessed when lifting the keyboard, or within the SSD or DDR compartments, or by removing existing battery, wireless or other available easy access panels on the chassis.

## 27.1.6 Compliance Requirements

**Table 27-5. Compliance Documents**

| Title | Location |
|---|---|
| *System Management Bus (SMBus) Specification, version 2* | *http://smbus.org/specs* |

## 27.1.7 Tools

Intel does not promote any specific tool for this interface.

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# 28 Secure Digital Card with Extended Capacity (SDXC) Interface Design Guidelines

## 28.1 SDXC Signal Descriptions

**Table 28-1. SDXC Signals**

| Group | Signal Name | Description |
|---|---|---|
| Clock | SD_CLK | SDXC Clock signal |
| Data | SD_DATA[3:0] | SDXC Data signals |
| Command | SD_CMD | SDXC Command signal |
| Control | SD_CD# | SD Card detect |
| | SD_WP | SD card write protect |
| Power Enable | SD_VDD1_PWR_EN# | SD card power enable 3.3V |
| Reference | SD_3P3_RCOMP | External Reference (200 Ohm+/- 1% pull down to ground) |
| | SD_1P8_RCOMP | External Reference (200 Ohm+/- 1% pull down to ground) |

### 28.1.1 SDXC Topology Guideline

If the interface is used, external pull-up/pull-down resistors are not required on SD_DATA[3:0]; SD_CMD; SD_CD and SD_CLK.

***Notes:***

1. The topology and guidelines below apply to down device as well as M.2 connector.
2. Design guideline applies for 3.3V at 50MHz and 1.8V at 200MHz.
3. Transient Voltage Suppressor (TVS) may be required on SD_CMD, SD_DATA[0:3], SD_CLK and SD_CD#. Refer Section 49, “Electromagnetic Compatibility” for the same.

#### 28.1.1.1 SDXC Topology Guidelines

The PCH implements a SDXC controller that supports SDXC 3.01 specifications.

The interface supports either 1.8V or 3.3V.

Resistor R1 (22 ohms) in the below topology diagram to be placed on SD_DATA[3:0] and SD_CMD not more than 12.7 mm away from the device.

**Figure 28-1. SDXC Topology**

**Table 28-2. SDXC Routing Guidelines for CFL Motherboard**

| Parameter | Stack-up | Routing Recommendation (in mm) | Routing Recommendation (in mils) |
|---|---|---|---|
| BO - Max Breakout Length | MS/SL/DSL | 12.7 | 500 |
| M1 - Trace Length | SL/DSL | 50-177 | 1968.5-6968.5 |
| M2 - Max Breakin Length | MS | 12.7 | 500 |
| M - Trace Spacing for Clock Signal | NA | 0.381 | 15 |
| M - Trace Spacing between Data Signals | MS/SL | 0.254 | 10 |
| SD Card Clock and SD Card Data /CMD Signal Length Mismatch | MS/SL/DSL | <2.54 (Note 1) | <100 (Note 1) |
| Max Via Count for BO and M | | 4 | |

***Notes:***
1. Including package length is not required.
2. Break-in length must not have any via.
3. Reference should be continuous Ground plane only.

Refer Chapter 2, "Stack-Up and PCB Considerations" for other details like Trace Width, Trace Spacing, Breakout Width, Breakout Spacing, etc.

***Note:*** SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

***Warning:*** SD_3P3_RCOMP and SD_1P8_RCOMP are Impedance Compensation for 3.3V and 1.8V operation of SDXC and GPIO buffers. External reference resistor is required (200 Ohm +/- 1% pull down to ground) regardless of SDXC being used or not. SD3_1P8_RCOMP and SD3_3P3_RCOMP can share a common RCOMP resistor of 200 Ohm, 1%. SD3_1P8_RCOMP and SD3_3P3_RCOMP can share a common RCOMP resistor of 200 Ohm, 1%.

### 28.1.1.2 SD_VDD1_PWR_EN Polarity

Signal SD card power enable (SD_VDD1_PWR_EN#) assertion logic can be changed by BIOS. In default BIOS implementation this signal has an Active High assertion logic.

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# 29 Low Pin Count (LPC) Interface Design Guidelines

## 29.1 Overview

This document contains a design guidelines for a Low Pin Count bus interface, called LPC. The SoC contains LPC interfaces for legacy device support. LPC provides accesses to the BIOS Firmware Memory, Embedded Controller or Super I/O (Keyboard Controller, GamePort, Parallel Port, etc) and TPM (Trusted Platform Module).

## 29.2 LPC Signal Description

### Table 29-1. LPC Signal Descriptions (Sheet 1 of 2)

| Signal Names | Group | Description |
|---|---|---|
| GPP_A1 / **LAD0** / ESPI_IO0 | Multiplexed Command, Address, Data (I/O) | This multiplexed signal line communicate address, control, and data information over the LPC bus between a host and a peripheral. Internal pull-ups are provided for these signals. |
| GPP_A2 / **LAD1** / ESPI_IO1 | Multiplexed Command, Address, Data (I/O) | This multiplexed signal line communicate address, control, and data information over the LPC bus between a host and a peripheral. Internal pull-ups are provided for these signals. |
| GPP_A3 / **LAD2** / ESPI_IO2 | Multiplexed Command, Address, Data (I/O) | This multiplexed signal line communicate address, control, and data information over the LPC bus between a host and a peripheral. Internal pull-ups are provided for these signals. |
| GPP_A4 / **LAD3** / ESPI_IO3 | Multiplexed Command, Address, Data (I/O) | This multiplexed signal line communicate address, control, and data information over the LPC bus between a host and a peripheral. Internal pull-ups are provided for these signals. |
| GPP_A5 / **LFRAME#** / ESPI_CS0# | Frame (O) | Indicates start of a new cycle and termination of a broken cycle |
| GPP_A0 / **RCIN#** / ESPI_ALERT1# | Input (I) | **Keyboard Controller Reset Processor:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the PCH's other sources of INIT#. When the PCH detects the assertion of this signal, INIT# is generated to the processor. ***Note: An external Pull-up 10 KΩ to V3.3S power rail is required.*** |
| GPP_A9 / **CLKOUT_LPC0** / ESPI_CLK | Clock (O) | **Low Pin Count (LPC) Clock Outputs:** Single-Ended **24-MHz** output to various single load connectors/ devices. |
| GPP_A10 / **CLKOUT_LPC1** | Clock (O) | **Low Pin Count (LPC) Clock Outputs:** Single-Ended **24-MHz** output to various single load connectors/ devices. |

**Table 29-1. LPC Signal Descriptions (Sheet 2 of 2)**

| Signal Names | Group | Description |
|---|---|---|
| GPP_A8 / **CLKRUN#** | Clock Run (I/O) | Input to determine the status of ILB_LPC_CLK and an open drain output used to request starting or speeding up ILB_LPC_CLK. This is a sustained tri-state signal used by the central resource to request permission to stop or slow ILB_LPC_CLK. The central resource is responsible for maintaining the signal in the asserted state when ILB_LPC_CLK is running and de-asserts the signal to request permission to stop or slow ILB_LPC_CLK. An internal pull-up is provided for this signal. |
| GPP_A6 / **SERIRQ** / ESPI_CS1# | Serial Interrupt Request (I/O) | This signal implements the serial interrupt protocol. ***Note: An external Pull-up 8.2 KΩ ~10 KΩ to V3.3S power rail is required.*** |
| GPP_A14 / **SUS_STAT#** / ESPI_RESET# | Output (O) | **LPC Mode - Suspend Status:** This signal is asserted by the PCH to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. |

## 29.2.1 LPC Topology Guidelines

## 29.2.2 LPC DATA 3 Load Daisy Chain Topology Guidelines

**Figure 29-1. LPC DATA 3 Load Daisy Chain Topology**

**Table 29-2. Routing Guidelines for LPC DATA 3 Load Daisy Chain Topology (Sheet 1 of 2)**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | N/A | 12.7 | 432.70 | 500 | 17035.44 |
| M1 | MS/SL/DSL | VSS | N/A | 330 | | 12992.13 | |
| M2 | MS/SL/DSL | VSS | N/A | 64 | | 2519.69 | |
| M3 | MS/SL/DSL | VSS | N/A | 13 | | 511.81 | |
| M4 | MS/SL/DSL | VSS | N/A | 26 | | 1023.62 | |
| Cable | N/A | VSS | N/A | 177.8 | | 7000.00 | |

**Table 29-2. Routing Guidelines for LPC DATA 3 Load Daisy Chain Topology (Sheet 2 of 2)**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |

***Notes:***
1. R1 is 0 ohm by default, can be up to 22 ohm if there is EMI issue.To be placed for all LPC DATA pins. EMI RC filter placeholder, refer to EMC section for details. R1 is recommended to be placed 12.7mm (500 mils) from the PCH, but can be extended to 25.4 mm (1000 mils) maximum if required. The length of breakout section BO is still 12.7mm (500 mils) maximum
2. C to be unstuffed by default, can be up to 27pF if there is EMI issue. EMI RC filter placeholder, refer to EMC section for details. C To be placed for all LPC DATA pins. C is recommended to be placed 12.7mm (500 mils) from the PCH, but can be extended to 25.4 mm (1000 mils) maximum if required. The length of breakout section BO is still 12.7mm (500 mils) maximum
3. Maximum 7 number of vias can be allowed.
4. Reference plane should be Continuous Ground Plane.

## 29.2.3 LPC CLK Single Load Topology

**Figure 29-2. LPC CLK Single Load Topology**

**Table 29-3. Routing Guidelines for LPC CLK Single Load Topology**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | N/A | 12.7 | 432.7 | 500 | 17035.43 |
| M1 | MS/SL/DSL | VSS | N/A | 420 | | 16535.43 | |

***Notes:***
1. R1 is 0 ohm by default, can be up to 22 ohm if there is EMI issue. EMI RC filter placeholder, refer to EMC section for details. R1 to be placed for LPC CLK pins. R1 is recommended to be placed 12.7mm (500 mils) from the PCH, but can be extended to 25.4 mm (1000 mils) maximum if required. The length of breakout section BO is still 12.7mm (500 mils) maximum.
2. C To be unstuffed by default, can be up to 27pF if there is EMI issue. C to be placed for LPC CLK pins. C is recommended to be placed 12.7mm (500 mils) from the PCH, but can be extended to 25.4 mm (1000 mils) maximum if required. The length of breakout section BO is still 12.7mm (500 mils) maximum
3. 7 number of vias can be allowed.
4. Reference plane should be only Continuous Ground Plane.

## 29.2.4 Disable Guidelines

If the LPC pins are not implemented on the platform, all the pins can be left as unconnected.

### 29.2.5 General Guidelines for Length Matching Requirements

1. For both P2P and branch topology, CLK length need to be matched with data length within 500 mils (12.7mm)
2. Trace spacing between DATA and DATA must be with in 5 mils (0.127mm).
3. Trace spacing between CLK and other signals must be with in 15 mils (0.381mm).

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# 30 Serial Peripheral Interface (SPI0) Flash Design Guidelines

## 30.1 Overview

The Serial Peripheral Interface (SPI0) supports 2 SPI0 flash devices via 2 chip select (SPI0_CS0# and SPI0_CS1#). The maximum size of flash supported is determined by the SFDP-discovered addressing capability of each device. Each component can be up to 16 MB (32 MB total addressable) using 3-byte addressing. Each component can be up to 64 MB (128 MB total addressable) using 4-byte addressing. Another chip select (SPI0_CS2#) is also available and only used for TPM on SPI0 support.

PCH drives the SPI0 interface clock at either 20 MHz, 33 MHz, or 50 MHz and it will function with SPI0 flash devices that support at least one of these frequencies.

The SPI0 interface supports either 3.3V or 1.8V.Descriptor mode is required for all platforms with PCH.

A SPI0 flash device which supporting SFDP (Serial Flash Discovery Parameter) is required for all PCH design. A SPI0 flash device on SPI0_CS0# with a valid descriptor must be attached directly to the PCH.

**Table 30-1. Acronyms**

| Acronyms | Description |
|---|---|
| CS | Chip Select |
| CLK | Clock |
| EC | Embedded Controller |
| FET | Field Effect Transistor |
| MISO | Master In Slave Out |
| MOSI | Master Out Slave In |
| SPI0 | Serial Peripheral Interface |
| TPM | Trusted Platform Module |

**Table 30-2. SPI0 Signals (Sheet 1 of 2)**

| Signal Name | Group | Description |
|---|---|---|
| SPI0_MOSI | Data | SPI0 serial output data from PCH to the SPI0 flash device. This Pin will also function as Input during Dual and Quad I/O operation |
| SPI0_MISO | Data | SPI0 serial input data from the SPI0 flash device to PCH. This Pin will also function as Output during Dual and Quad I/O operation |
| SPI0_IO2 | Data | SPI0 I/O to comprehend the support for the Quad I/O operation |
| SPI0_IO3 | Data | SPI0 I/O to comprehend the support for the Quad I/O operation |
| SPI0_CLK | Clock | SPI0 Clock output from PCH |
| SPI0_CS0# | Chip Select0 | SPI0 chip select 0 |
| SPI0_CS1# | Chip Select1 | SPI0 chip select 1 signal is used as the second chip select when 2 flash devices are used. Do not use when only one SPI0 flash is used |

**Table 30-2. SPI0 Signals (Sheet 2 of 2)**

| Signal Name | Group | Description |
|---|---|---|
| SPI0_CS2# | Chip Select2 | Chip Select 2 is dedicated to support TPM on SPI0. |

## 30.2 Serial Peripheral Interface (SPI0) Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for PCH SPI0 interface. SPI0 flash must be directly connected to the PCH SPI0 bus. Also, refer to the Serial Flash vendor documentation for additional Serial Flash specific design considerations.

### 30.2.0.1 SPI0 Single Load Topology Guidelines

**Figure 30-1. SPI0 Single Load Topology**

**Table 30-3. Single Flash Topology Routing Guidelines**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | N/A | 12.7 | 177.7 | 500.00 | 6996.06 |
| M1 | MS/SL/DSL | VSS | N/A | 165 | | 6496.06 | |

***Notes:***
1. R1 resistor should be stuffed with 33 ohm for 3.3V and 15 ohm for 1.8V. R1 is recommended to be placed 12.7mm (500 mils) from the PCH, but can be extended to 25.4 mm (1000 mils) maximum if required. The length of breakout section BO is still 12.7mm (500 mils) maximum. R1 is not required for CS# signal.
2. 5 number of vias can be allowed.
3. Continuous ground referencing plane
4. Design guidelines are applies for SPI0_IO_2 to 3, SPI0_MOSI, SPI0_MISO, SPI0_CLK, SPI0_FLASH_0_CS#, SPI0_FLASH_1_CS# and SPI0_TPM_CS#
5. Design guideline support up to 50MHz.

## 30.2.1 SPI0 2 Load Topology Guidelines

**Figure 30-2. SPI0 2 Load Topology**

The system can be configured with 1 SPI0 Flash and 1 TPM device.

**Table 30-4. Routing Guidelines for SPI0 2 Load Topology Routing Guidelines**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| B0 | MS/SL/DSL | VSS | N/A | 12.7 | 177.7 | 500.00 | 6996.06 |
| M1 | MS/SL/DSL | VSS | N/A | 124.46 | | 4900.00 | |
| M2 | MS/SL/DSL | VSS | N/A | 2.54 | | 100.00 | |
| M3 | MS/SL/DSL | VSS | N/A | 38 | | 1496.06 | |

***Notes:***
1. R1 resistor should be stuffed with 33 ohm for 3.3V and 15 ohm for 1.8V. R1 is not required for CS# signal.
2. 5 number of vias can be allowed.
3. Continuous ground referencing plane
4. Design guidelines are applies for SPI0_IO_2 to 3, SPI0_MOSI, SPI0_MISO, SPI0_CLK, SPI0_FLASH_0_CS#, SPI0_FLASH_1_CS# and SPI0_TPM_CS#
5. Design guideline support up to 50MHz
6. R2 resistor should be stuffed with 5 ohm for 3.3V and 1.8V. R2 resistor is not required for CS# signal.

## 30.2.2 SPI0 2 Load with EC Flash sharing Topology

**Figure 30-3. SPI0 2 Load with EC Flash sharing Topology**

**Table 30-5. Routing Guidelines for SPI0 2 Load with EC Flash Sharing Topology**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| B0 | MS/SL/DSL | VSS | N/A | 12.7 | 177.7 | 500.00 | 6996.06 |
| M1 | MS/SL/DSL | VSS | N/A | 124.46 | | 4900.00 | |
| M2 | MS/SL/DSL | VSS | N/A | 2.54 | | 100.00 | |
| M3 | MS/SL/DSL | VSS | N/A | 38 | | 1496.06 | |

***Notes:***
1. R1 resistor should be stuffed with 33 ohm for 3.3V and 15 ohm for 1.8V. R1 is not required for CS# signal.
2. 5 number of vias can be allowed.
3. Continuous ground referencing plane
4. Design guideline support up to 50MHz
5. Design guidelines applies for SPI0_IO_2 to 3, SPI0_MOSI, SPI0_MISO, SPI0_CLK, SPI0_FLASH_0_CS#, SPI0_FLASH_1_CS# and SPI0_TPM_CS#
6. FET component criteria: Ron <5 ohm, Cin <3pF

## 30.2.3 SPI0 3 Load Topology Guidelines

The PCH supports TPM through SPI0 bus. The topology below was a full configuration which consist of 2 SPI0 Flash and 1 TPM device.

**Figure 30-4. SPI0 3 Load Topology**

**Table 30-6. SPI0 3 Load Topology Routing Guidelines**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| B0 | MS/SL/DSL | VSS | N/A | 12.7 | 189.70 | 500.00 | 7468.50 |
| M1 | MS/SL/DSL | VSS | N/A | 124.46 | | 4900.00 | |
| M2 | MS/SL/DSL | VSS | N/A | 2.54 | | 100.00 | |
| M3 | MS/SL/DSL | VSS | N/A | 38 | | 1496.06 | |
| M4 | MS/SL/DSL | VSS | N/A | 50 | | 1968.50 | |

***Notes:***
1. R1 resistor should be stuffed with 33 ohm for 3.3V and 10 ohm for 1.8V. R1 is not required for CS# signal.
2. 5 number of vias can be allowed.
3. Continuous ground referencing plane
4. Design guidelines are applies for SPI0_IO_2 to 3, SPI0_MOSI, SPI0_MISO, SPI0_CLK, SPI0_FLASH_0_CS#, SPI0_FLASH_1_CS# and SPI0_TPM_CS#
5. Design guideline support up to 50MHz
6. R2 resistor should be stuffed with 10 ohm for 3.3V and 1.8V. R2 resistor is not required for CS# signal.

## 30.2.4 SPI0 3 Load with EC Flash Sharing Topology

The PCH and Embedded Controller (EC) shares 2 SPI0 Flash device and TPM through FET switch. The topology below was a full configuration which consist of PCH, Embedded Controller (EC), 2 SPI0 Flash and 1 TPM device.

**Figure 30-5. SPI0 3 Load with EC Flash Sharing Topology**

### 30.2.4.1 SPI0 with Embedded Controller (EC) Flash Sharing Routing Guidelines

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| B0 | MS/SL/DSL | VSS | N/A | 12.7 | 189.70 | 500.00 | 7468.50 |
| M1 | MS/SL/DSL | VSS | N/A | 124.46 | | 4900.00 | |
| M2 | MS/SL/DSL | VSS | N/A | 2.54 | | 100.00 | |
| M3 | MS/SL/DSL | VSS | N/A | 38 | | 1496.06 | |
| M4 | MS/SL/DSL | VSS | N/A | 50 | | 1968.50 | |

***Notes:***
1. R1 Resistor should be 33 ohm for 3.3V and 10 ohm for 1.8V. R1 is not required for CS# signal.
2. 5 number of vias can be allowed.
3. Continuous ground referencing plane
4. FET switch component criteria should be Ron <10 ohm, Cin <5pF
5. Design guidelines are applies for SPI0_IO_2 to 3, SPI0_MOSI, SPI0_MISO, SPI0_CLK, SPI0_FLASH_0_CS#, SPI0_FLASH_1_CS# and SPI0_TPM_CS#
6. Design guideline support up to 50MHz

### 30.2.4.2 General guidelines for SPI0 Flash Device Interface

1. Length Matching between DATA and CLK should be maximum of 500 mils (12.7mm).
2. Trace spacing between DATA and DATA should be 10 mils (0.254mm)
3. Trace spacing between CLK and other signals should be 15 mils (0.381mm).

***Notes:***

1. SPI0 branches of segment M2 need to have length matching of 100 mils
2. SPI0_CLK and SPI0_MOSI (including all the Master Output Pins during Dual and Quad I/O Operation) must be length matched to within 500 mils
3. SPI0_CLK and SPI0_CSn# should be length matched by 500 mils, but can extend to 1000 mils.
4. SPI0_CLK must be 20 mils spacing from any other high frequency (>1GHz) signal

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# 31 Serial Peripheral Interface (SPI1) Touch Design Guidelines

## 31.1 SPI1 Touch Platform Specific Important Information

The Serial Peripheral Interface (SPI1) supports 1 SPI1 Touch device via 1 chip select (SPI1_CS#) with Quad IO. PCH drives the SPI1 interface clock at 30 MHz and will function with SPI1 Touch device that support at this frequency.

The SPI1 interface supports either 3.3V or 1.8V. Descriptor mode is required for all platforms with PCH. A SPI1 Touch device on SPI1_CS# with a valid descriptor must be attached directly to the PCH.

## 31.2 SPI1 Touch Signal Descriptions

| Signal Name Group Description | Signal Name Group Description | Signal Name Group Description |
|---|---|---|
| SPI1_CLK | Clock | SPI1 Clock output from PCH |
| SPI1_MISO_IO_1 | Data | SPI1 serial input data from the SPI1 Touch Screen device to PCH. This Pin will also function as Output during Dual and Quad I/O operation |
| SPI1_MOSI_IO_0 | Data | SPI1 serial output data from PCH to the SPI1 Touch Screen device. This Pin will also function as Input during Dual and Quad I/O operation |
| SPI1_IO_2 | Data | SPI1 I/O to comprehend the support for the Quad I/O operation |
| SPI1_IO_3 | Data | SPI1 I/O to comprehend the support for the Quad I/O operation |
| SPI1_CS# | Chip Select | SPI1 chip select |

## 31.3 SPI1 Touch Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for PCH SPI interface. Touch device must be directly connected to the PCH SPI1 bus. Also, refer to the Serial Touch device vendor documentation for additional Serial Touch specific design considerations.

## 31.3.1 SPI1 Single Load Touch Topology

### 31.3.1.1 SPI1 Single Load Touch Length Matching Requirement

**Table 31-1. SPI1 Single Load Touch Routing Guideline**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | N/A | 12.7 | 462.7 | 500.00 | 18216.54 |
| M1 | MS/SL/DSL | VSS | N/A | 300 | | 11811.02 | |
| M_Cable | Shielded cable | VSS | N/A | 150 | | 5905.51 | |

***Notes:***
1. Resistor R1 should be 10 ohm for 1.8V, 50 ohm for 3.3V. R1 is recommended to be placed 12.7mm (500 mils) from the connector. R1 recommendation for SPI1_CLK, SPI1_MOSI, SPI1_MISO, SPI1_IO_2 and SPI1_IO_3 signals
2. Design guideline support up to 30MHz.
3. 7 number of vias can be allowed.
4. Reference plane should be Continuous Ground Plane.
5. SPI1 Touch single load topology applies to SPI_CS#, SPI1_CLK, SPI1_MOSI, SPI1_MISO, SPI1_IO_2 and SPI1_IO_3

## 31.3.2 SPI1 Touch Length Matching Requirement

1. Length Matching between DATA and CLK should be maximum of 500 mils (12.7mm)
2. Trace spacing between DATA and DATA should be 5 mils (0.127mm).
3. Trace spacing between CLK and other signals should be 15 mils (0.381mm).

***Notes:***

1. SPI1_CLK and SPI1_MOSI (including all the Master Output Pins during Dual and Quad I/O Operation) must be length matched to within 500 mils.
2. SPI1_CLK and SPI1_CSn# must be length matched to within 500 mils.
3. SPI1_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.

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# 32 Legacy Audio Interface Design Guidelines

Coffee Lake platform is a next-generation architecture for audio that allows audio output and input streams to be processed by the host IA processor or for processing to be offloaded from IA processing via the next generation Intel® Smart Sound Technology (Intel® SST) DSP.

This design guideline chapter includes the routing details for different legacy audio interfaces that connect to the Coffee Lake platform PCH. These are as follows:

- Intel® High Definition Audio (HD-A) Interface
- Digital Microphone (DMIC) Interface
- Integrated Interchip Sound ($I^2S$) Interface

Intel® Display Audio Interface In this chapter th HD-A interface is compliant with Microsoft* Universal Audio Architecture (UAA). Contact your IHV (Independent Hardware Vendor) for information on HD-A, I2S, and DMIC based products.

## 32.1 Legacy Audio Interface Platform Specific Important Information

On the Coffee Lake platform the Intel HD Audio interface pins are partially multiplexed with $I^2S$ interface, and the MIPI SoundWire* interface and they can be configured as either (and in some cases simultaneously) for connection to end devices. The DMIC interface is multiplexed with various GPP signals. See the Coffee Lake PCH EDS for specific sku pins assignments and multiplexing details.

### 32.1.1 Legacy Audio Interface - Signal Description

**Table 32-1. Audio Signals (Sheet 1 of 2)**

| Signal Name | Description |
|---|---|
| **Intel HD Audio Interface** | |
| HDA_RST# | Master hardware reset to external codec(s) |
| HDA_SYNC | 48 KHz fixed rate sample sync to the codec(s) |
| HDA_BCLK | 24.000 MHz serial data clock generated by the Intel® HD Audio controller. |
| HDA_SDO | Serial TDM data output to the codec(s) |
| HDA_SDIN [1:0] | Serial TDM data inputs from the codecs |
| **I2S Interface** | |
| I2S_SCLK | $I^2S$ Serial Bit Clocks for connection to $I^2S$ devices. |
| I2S_TXD | $I^2S$ Transmit Data (Serial data out) for connection to $I^2S$ devices. |
| I2S_RXD | $I^2S$ Receive Data (Serial data in) for connection to $I^2S$ devices. |
| I2S_SFRM | $I^2S$ Serial Frame for connection to I2S devices. |
| **Intel® Display Audio Interface** | |

**Table 32-1. Audio Signals (Sheet 2 of 2)**

| Signal Name | Description |
|---|---|
| HDACPU_SDI | Serial TDM data inputs from the integrated codec |
| HDACPU_SDO | Serial TDM data output to the integrated codec |
| HDACPU_SCLK | dedicated 24.000 MHz serial data clock to the integrated codec |
| **DMIC Interface** | |
| DMIC_CLK[1:0] | Serial data clock generated by the PCH to the digital microphone module |
| DMIC_DATA[1:0] | Serial data input from the digital microphone module |

## 32.1.2 Intel High Definition Audio (Intel HD Audio) and DMIC Topology Guidelines

### 32.1.2.1 Intel HD Audio Single Load Audio Device Down Topology

**Figure 32-1. HDA_SDI Single Load Audio Down Topology**

**Figure 32-2. HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST# Audio Down Topology**

**Table 32-2. HDA_SDIN/HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST# Audio Down Routing Guidelines (Sheet 1 of 2)**

| Parameter[3] | Segment | Stack-up | Units | Recommendation |
|---|---|---|---|---|
| Trace Length Maximum | BO | MS/SL/DSL | mils | 500 |
| Trace Length Maximum | M1 | MS/SL/DSL | mils | 13976.38 |
| Trace length Maximum | B0+M1 | MS/SL/DSL | mils | 14476.38 |
| Trace Length Matching for HDA_BCLK and HDA_SDO | NA | NA | mils | 500 |
| Trace Spacing Between Data and Data | B0, M1 | NA | mils | 5 |
| Trace Spacing Between Clk and other Signals | B0, M1 | NA | mils | 15 |
| Rs Resistor Value[1] | RS1 | NA | Ω | 33 |

### Table 32-2. HDA_SDIN/HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST# Audio Down Routing Guidelines (Sheet 2 of 2)

| Parameter[3] | Segment | Stack-up | Units | Recommendation |
|---|---|---|---|---|
| Rs Resistor Value[1,4] | RS2 | NA | Ω | 33 |
| RS2 Resistor and C2 Capacitor Minimum Distance from PCH | M1 | MS/SL/DSL | mils | 500 |
| RS2 Resistor Maximum Distance from PCH | M1 | MS/SL/DSL | mils | 3000 |
| C1 Capacitor Max Distance from Codec | M1 | MS | mils | 500 |
| C2 Capacitor Maximum Distance from PCH | M1 | MS | mils | 1000 |
| C2 Capacitor Maximum Distance from PCH | M1 | SL/DSL | mils | 2000 |
| Capacitor Recommended Value[2] | C1, C2 | MS | pF | 2 |
| Max Vias | NA | NA | count | 7 |
| PCH Buffer Impedance Target for Intel HD Audio[5] | NA | NA | Ω | 50 |

***Note:***
1. This is Intel's general series resistor requirements from PCH to a typical end device. Please consult your codec vendor if any specific series resistor requirements for the end device is needed as it may vary from device to device.
2. Capacitor to only be used for HDA_SDO, HDA_RST#, and HDA_SDI for EMI purposes and should be a close as possible to the PCH.
3. Routes should be referenced to GND for entire route.
4. Resistor values should be 33 ohms for both 3.3v and 1.8v signaling.
5. PCH buffer strength should be 50ohm, slew 11. Refer to EDS/BIOS programming guide for further details.

## 32.1.2.2 Intel High Definition Audio (Intel HD Audio) and DMIC Branched Device Topology

### Figure 32-3. HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST# Branched Topology

***Note:*** Any combination of above topology for the Intel HD Audio bus are valid but only up to 2 codec(s) are supported.

## Figure 32-4. DMIC_CLK and DMIC_DATA Branched Topology

*C2 placeholder is for DMIC_CLK only.
**RS2 is for use on DMIC_CLK and RS3 is for use on DMIC_DATA. Do not use both series resistors on the same signal.

## Table 32-3. HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST#/DMIC_CLK/DMIC_DATA Branched Routing Guidelines (Sheet 1 of 2)

| Parameter[3] | Segment | Stack-up | Units | Recommendation |
|---|---|---|---|---|
| Trace Length Max | B0 | SL | mils | 500 |
| Trace Length Max | M1, M3 | MS/SL/DSL | mils | 5000 |
| Trace Length Max | M2 | MS/SL/DSL | mils | 8976.38 |
| Trace Length Max | M4 | MS | mils | 3976.38 |
| Trace Length Max | M5 | MS/SL/DSL | mils | 10000 |
| Trace Length Max | M6 | MS/SL/DSL | mils | 5000 |
| Trace Length Matching both Branch Lengths | M6 | NA | mils | 100 |
| Trace Length Max | M-Cable | NA | mils | 20000 |
| Trace Length Max | B0+M1+M2 or B0+M1+M3+M4 | MS/SL/DSL | mils | 14476.38 |
| Trace Length Max | B0+M5+M-Cable+M6 | MS/SL/DSL | mils | 35500 |
| Trace Length Matching (HDA_BCLK and HDA_SDO) | NA | NA | mils | 500 |
| Trace Spacing Between Data and Data | B0, M1 | NA | mils | 5 |
| Trace Spacing Between Clk and other Signals | B0, M1 | NA | mils | 15 |
| HDA Resistor Value Max[2] | RS1 | NA | Ω | 15 |
| DMIC Resistor Value Max[7] | RS2, RS3 | NA | Ω | 33 |
| DMIC_CLK RS2 recommended distance from PCH[6] | M5 | MS | mils | 500 |
| DMIC_CLK RS2 max distance from PCH[6] | M5 | MS | mils | 1000 |
| DMIC_DATA RS3 recommended distance from DMIC | M6 | MS | mils | 500 |
| C1 and C2 Recommended Distance from Output Device[6] | M1, M5 | MS/SL/DSL | mils | 500 |
| C1 and C2 Maximum Distance from PCH[6] | M1, M5 | MS | mils | 1000 |

**Table 32-3. HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST#/DMIC_CLK/DMIC_DATA Branched Routing Guidelines (Sheet 2 of 2)**

| Parameter[3] | Segment | Stack-up | Units | Recommendation |
|---|---|---|---|---|
| C1 Maximum Distance from Output Device[6] | M1, M5 | SL/DSL | mils | 2000 |
| DMIC spacing between DATA and DATA | NA | MS/SL/DSL | mils | 5 |
| DMIC spacing between CLK and other signals | NA | MS/SL/DSL | mils | 15 |
| Capacitor Value | C1 | NA | pF | 2 |
| Capacitor Value[4] | C2 | NA | pF | 27 |
| Max Vias | NA | NA | count | 7 |
| PCH Buffer Impedance Target for HDA[5] | NA | NA | Ω | 33 |

***Notes:***
1. HDA_SDO and HDA_BCLK as well as DMIC_CLK and DMIC_DATA must be length matched to within 500 mils.
2. This is Intel's general series resistor requirements from PCH to a typical end device. Please consult your codec vendor if any specific series resistor requirements for the end device is needed as it may vary from device to device.
3. Routes should be referenced to GND for entire route.
4. DMIC_CLK cap can be just a placeholder and stuffed only when needed.
5. PCH buffer strength should be 40ohm, slew 11. Refer to EDS/BIOS programming guide for further details.
6. If M5 is routed on MS, EMI RC filter should be placed at the beginning of MS routing.
7. RS2 is for use on DMIC_CLK and RS3 is for use on DMIC_DATA. Do not use both series resistors on the same signal.

## 32.1.3 Integrated CODEC for Intel Display Audio

The processor has an integrated CODEC to provide Audio through HDMI/DP. The Intel Display Audio interface from the processor needs to be connected to the PCH as the audio communication is handled by Intel High Definition Audio controller in the PCH.

**Figure 32-5. PROC_AUDIO_SDO to HDACPU_SDI (CPU Out, PCH In) Topology**

**Table 32-4. HDACPU_SDI Audio Down Routing Guidelines (Sheet 1 of 2)**

| Parameter | Segment | Stackup | Units | Routing Recommendation |
|---|---|---|---|---|
| Trace Length Maximum | BI/BO | MS/SL/DSL | mils | 500 |
| Trace Length Maximum | M1 | MS/SL/DSL | mils | 7500 |
| Trace Length Maximum | M1+BI | MS/SL/DSL | mils | 8000 |
| Trace Length Matching with respect to HDACPU_SCLK | NA | NA | mils | 500 |
| Resistor Value | Rs | NA | Ω | 20 |

**Table 32-4. HDACPU_SDI Audio Down Routing Guidelines (Sheet 2 of 2)**

| Parameter | Segment | Stackup | Units | Routing Recommendation |
|---|---|---|---|---|
| PCH Buffer Impedance Target | NA | NA | Ω | 50 |
| Max Vias | NA | NA | Count | 5 |

**Figure 32-6. HDACPU_SDO to PROC_AUDIO_SDI/HDACPU_SCLK to PROC_AUDIO_CLK (PCH Out, CPU In) Topology**

**Table 32-5. HDACPU_SDO/HDACPU_SCLK Routing Guidelines**

| Parameter | Segment | Stackup | Units | Routing Recommendation |
|---|---|---|---|---|
| Trace Length Maximum | BI, B0 | MS/SL/DSL | mils | 500 |
| Trace Length Maximum | M1 | MS/SL/DSL | mils | 7500 |
| Trace Length Maximum | BO+M1 | MS/SL/DSL | mils | 8000 |
| Trace Length Matching with respect to HDACPU_SCLK | NA | NA | mils | 500 |
| Resistor Value | Rs | NA | Ω | 30 |
| PCH Buffer Impedance Target | NA | NA | Ω | 50 |
| Max Vias | NA | NA | Count | 5 |

## 32.1.4 Disabling and Termination Guidelines for the Intel High Definition Audio Interface

When HDA_SDIN[1:0] is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI on the CPU need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected. The Intel Display Audio pins on the PCH may be left disconnected.

## 32.1.5 $I^2S$* Device Connection Topology

When the PCH Intel® HD Audio bus/$I^2S$ multiplexed pins are configured as $I^2S$, the following topology and guidelines should be used for routing to end devices.

### Figure 32-7. PCH to I²S* Device Topology - I2S_MCLK/ I2Sx_SFRM/ I2Sx_TXD/ I2Sx_RXD

### Table 32-6. I²S* Audio Down Routing Guidelines

| Parameter[1] | Segment | Stack-up | Units | Recommendation |
|---|---|---|---|---|
| Trace Length Max | BO | MS/SL/DSL | mils | 500 |
| Trace Length Max | M1 | MS/SL/DSL | mils | 13066.9 |
| Trace Length Max | M2 | MS/SL/DSL | mils | 1500 |
| Trace Length Max | B0 + M1 + M2 | MS/SL/DSL | mils | 15066.93 |
| Parallel Route Length | M1 | DSL | mils | 3000 |
| RS Resistor Minimum Distance from PCH | M1 | MS/SL/DSL | mils | 500 |
| RS Resistor Maximum Distance from PCH | M1 | MS/SL/DSL | mils | 1000 |
| RS Series Resistor Max | RS | NA | ohms | 33 |
| Max number of Vias | NA | NA | count | 7 |
| PCH Buffer Impedance Target for I2S[2] | NA | NA | Ω | 50 |

***Note:***
1. Parameters applies to I2S_MCLK, I2Sx_SFRM, I2Sx_SCLK, I2Sx_TXD, and I2Sx_RXD signals.
2. PCH buffer strength should be 50ohm, slew 00. Refer to EDS/BIOS programming guide for further details.

§ §

# 33 Intel® Management Engine (Intel® ME)

## 33.1 Acronyms

| Acronyms | Description |
|---|---|
| C-Link, CLink | Controller Link |
| CFL | Coffee Lake |
| CNP | Cannon Lake PCH |
| DSW | Deep Sx Well |
| EC | Embedded Controller |
| FW | Firmware |
| LAN | Local Area Network |
| Intel® AMT | Intel® Active Management Technology |
| Intel® APS | Intel® Automatic Power Switch |
| Intel® ME | Intel® Management Engine |
| M0 | Intel® ME power state. The host CPU is in S0 and Intel® ME is operational. |
| M3 | Intel® ME power state. The host CPU is in Sx and Intel® ME is operational. |
| Moff | Intel® ME power state. The host CPU is in Sx and Intel® ME is not operational. |
| NIC | Network Interface Controller |
| SoC | System on Chip, the platform main processor. |
| SPI | Serial Peripheral Interface used for the Flash device interface, also name of the PCH interface to the real SPI flash |
| SUT | System Under Test |
| Sx | System state S3 or S4 or S5 |
| TBD | To Be Defined |
| WLAN | Wireless LAN |
| WoL | Wake on LAN |
| WoWLAN | Wake on Wireless LAN |

## 33.2 Preface

Intel® Management Engine (Intel® ME) is the SoC internal MinuteIA processor, running the Intel® ME firmware, to deal with platform management. It is connected to the Flash, loading Intel® ME and Intel® ISH FW, run the Intel® AMT section (where applicable), may control EC for power states transition and more. The following is the platform design guidelines, to support hardware design.

Unless otherwise indicated, this content pertains to Coffee Lake H platform.

## 33.3 Reference Documents

| Document | Document Number |
|---|---|
| Converged Security and Manageability Engine (CSME) and Embedded Controller (EC) Interaction | 573615 |

## 33.4 Introduction

The following list of components compose the Intel® ME hardware infrastructure:

- Intel® ME is the general purpose controller, operating in parallel to, and is resource-isolated from the host processor and resides within the CNP-H (which is Cannon Lake PCH-H).
- The SPI Flash device stores firmware code for the Intel® ME and others.
- Intel® ME code is executed from system DRAM in S0 state. This code resides in UMA memory allocated by BIOS, which can be taken from any rank or channel. To interface with DRAM, the Intel® ME uses the main memory controller present in the processor. In S3 through S5 states, if the Intel® ME is active in those states (meaning, it is in M3), it uses internal RAM to the CNP-H (which is Cannon Lake PCH-H).
- The Intel® ME clock is provided by an internal ring oscillator in Sx/M3 states.
- It provide several sideband power sequencing signals, that should be used in conjunction with an EC for platform power flows.

Enabling Intel® ME on the Coffee Lake platform requires the following:

— Intel® ME to EC interface (at least minimal requirements)

— SPI flash

**Figure 33-1. Intel® ME Architecture**

## 33.5 Intel® ME Signal Descriptions

Intel® ME interacts with the on-board EC, to control system power state transitions.

### 33.5.1 Intel® ME to Embedded Controller Interface Signals

The Intel® ME subsystem in the CNP-LP must communicate with the EC to indicate when the Sx and DeepSx power wells needs to remain on, to indicate when LAN and/or WLAN power are/is needed and to know the system power source (AC or battery) to make proper policy decisions. To allow this communication, several sideband signals are required between CNP-H and EC.

***Note:*** There is no on-board logic controlled by SLP_A# signal to power the Intel® ME. This signal is still provided externally to indicate whether Intel® ME is in Moff or not (so that the external devices may be powered accordingly)

## 33.6 Optimization Guidelines

### 33.6.1 Intel® ME Guidelines

In addition to basic component level support (CNP and SPI flash), there are two additional areas of board support that should be considered when designing with Intel® ME and Intel® ME applications. These two areas are the ability to access Intel® ME remotely (via LAN, Wireless LAN) and the ability for Intel® ME to support the M3 power state.

The hardware components for Intel® ME remote access are as following:

- Intel LAN (including SLP_LAN# signal support) is required for LAN connectivity for Intel® ME and supported applications.
- Intel Wireless LAN products (including SLP_WLAN# signal support) is required for wireless network connectivity for Intel® ME and supported applications.
  - The C-Link (Controller Link) is used to manage the wireless devices. C-Link is a 3-pin, 60-MHz, bi-directional, low-power bus that allows the CNP and WLAN subsystems to talk to each other. Refer to "Cannon Lake Platform Controller Hub (PCH-H) - External Design Specification (EDS) - Volume 1 of 2", RDC#571182 for full C-Link details.

To support the M3 power state:

- Support for power sequencing signals is described in the "Platform Power Sequencing Specification" chapter in this document.

Given different considerations, it is possible to design three different types of platforms:

- Platforms that support M3 power states **and** use the Intel LAN PHY or Intel wireless LAN solutions.
- Platforms that do not support M3 power states **and** use Intel LAN PHY or Intel wireless LAN PHY solutions.
- Platforms that do not support M3 power states **and** use a third-party LAN PHY solution.

The notes below in the following table summarize the power rails, enabling signals, and power state-by-state behavior that is common, or specifically relevant to M3 power state support and/or Intel LAN PHY / Wireless LAN usage.

### Table 33-1. Power Delivery Summary for Intel® ME SubSystem

| What It Powers | Rail | Sx /M3 | Sx /Moff | Sx/Moff/ WoL | Enabled By | Power OK Indicator |
|---|---|---|---|---|---|---|
| **Common** | | | | | | |
| Platform 5V rail | V5.0A | On | On | On | NA | NA |
| DRAM VDD | V1.35/V1.2 | On in S3 | On in S3 | On in S3 | SLP_S4# | NA |
| DRAM VTT | VDDQ/2 | Off | Off | Off | SLP_S3# | NA |
| Coffee Lake processor | V1.0 VCC | Off | Off | Off | SLP_S3# | PCH_PWROK |
| **M3 Support without Intel® LAN PHY/Wireless LAN Solution** | | | | | | |
| SPI interface | V1.8 or V3.3 VCCSPI | On | On | On | SLP_SUS# | RSMRST# |
| **M3 Support + Intel® LAN PHY / Wireless LAN Solution** | | | | | | |
| LAN PHY | Power to the LAN PHY | On | Off | On | SLP_LAN# | NA |
| Wireless LAN Device | Power to the Wireless LAN Device | On | Off | On | SLP_WLAN# | NA |
| SPI interface | V1.8 or V3.3 VCCSPI | On | On | On | SLP_SUS# | RSMRST# |
| **No M3 Support + Intel® LAN PHY / Wireless LAN Solution** | | | | | | |
| LAN PHY | Power to the LAN PHY | NA | Off | On | SLP_LAN# | NA |
| Wireless LAN | Power to the Wireless LAN Device | NA | Off | On | SLP_WLAN# | NA |
| SPI interface | V1.8 or V3.3 VCCSPI | On | On | On | SLP_SUS# | RSMRST# |
| ***Note:*** In Coffee Lake, Intel® ME Local RAM is powered by VCCSRAM_1P0 which is controlled by the platform. VCCSRAM_1P0 should be On in Sx/M3 and OFF in Sx/M-off | | | | | | |

### 33.6.1.1 Intel® ME Wireless Controller Link

C-Link interface is the management communication link between the CNP-H and Intel Wireless cards. Correct operation of this bus is required for wireless network communication and wake up events.

CNP is designed for either an internal CLINK connection (for CNVi) or an external bus, as described in the rest of this section (also called "discrete connectivity"). The selection between these two configurations does not require any hardware changes at the board level. The Intel® ME configure its own C-Link multiplexer as to select the C-LINK configuration (internal/external). This feature allows another level of automation by allowing the Intel® ME controller to read a SoC/PCH internal bit, indicating if CNVi or discrete is currently connected.

For implementing the discrete connectivity, refer to "Connon Lake Platform Controller Hub (PCH-H) - External Design Specification (EDS) - Volume 1 of 2", RDC#566439 for full C-Link details.

### Table 33-2. Intel® ME C-Link Signals and Signal-Integrity Design Guidelines

| Group | Signal Name | Description |
|---|---|---|
| Clock | CL_CLK | Controller Link Clock: Bi-directional clock that connects to a Wireless LAN Device supporting Intel® Active Management Technology. |
| Data | CL_DATA | Controller Link Data: Bi-directional data that connects to a Wireless LAN Device supporting Intel® Active Management Technology. |
| Reset | CL_RST# | Controller Link Reset: Controller Link reset that connects to a Wireless LAN Device supporting Intel® Active Management Technology. |

### Figure 33-2. C-Link Topology - To WLAN (CL_CLK1, CL_DATA1, CL_RST#)

### Table 33-3. C-Link Topology Guidelines

| Segment | Tline Type | Reference | Via Count | Max Length, mm | |
|---|---|---|---|---|---|
| | | | | Segment | Total |
| BO | MS/SL/DSL | VSS | N/A | 12.7 | 291.7 |
| M1 | MS/SL/DSL | VSS | N/A | 241 | |
| M2 | MS/SL/DSL | VSS | N/A | 38 | |

### Table 33-4. C-Link General Guidelines

| General Guidelines | |
|---|---|
| Length Matching between DATA and CLK | 25.4mm |
| Trace spacing between DATA and DATA | 0.127mm |
| Trace spacing between CLK and other signals | N/A |
| Max MLK_RSTB length | 228 mm (~9") |
| **Vias and Planes** | |
| Number of vias allowed | 5 |
| Reference plane | Continuous Ground Only |

LAN Considerations with or without Intel® Active Management (Intel® AMT) Support

## 33.6.2 For Intel® AMT support, Intel® ME Wake on LAN is a requirement.

### 33.6.2.1 Wake On LAN (WOL)

SLP_LAN# is used to indicate when power to the LAN PHY is needed. If Host Wake On LAN or Intel® ME Wake on LAN is enabled, the SLP_LAN# signal will remain high to keep power on to the LAN PHY.

The Integrated LAN (VccLAN) rail does not need to be powered in Sx/M-Off state unless they are needed as indicated by the CNP-H signals like SLP_S3# and SUSPWRDNACK.

### 33.6.2.2 Wake On Wireless LAN (WoWLAN)

SLP_WLAN# is used to indicate when power to the wireless LAN device is needed. If Host Wake on Wireless LAN is required in S3/S4/S5 or DeepSx states, the host BIOS must set HOST_WLAN_PP_EN. Refer to the "Cannon Lake Platform Controller Hub (PCH-LP) - External Design Specification (EDS) - Volume 2 of 2" document, RDC#565870, to the section discussing initialization of the HOST_WLAN_PP_EN bit. The SLP_WLAN# signal will remain high to keep power on to the wireless LAN device.

***Note:*** Unless controlled by system User, RF-Kill (W_DISABLE#) should not be asserted by the EC when power is provided to the WLAN card as this will block communication with the Intel® ME during M3 state.

## 33.6.3 WLAN Considerations with Intel® Active Management (Intel® AMT) Support

In designs where Corporate or Consumer Intel® ME are supported and wireless power management is supported, WLAN NIC power must be preserved in S0 and all its sub states (S0, S0ix, Connected standby and modern Standby).

## 33.6.4 SPI Flash Descriptor Security Override

To support Intel® ME, a SPI flash is required on the platform with sufficient space to hold system BIOS, Intel® ME firmware, Coffee Lake Intel® Integrated Sensor Solution firmware and any additional third party data storage. The SPI flash needs to be powered in states S0 through S5, independent of Intel® ME power state.

HDA_SDO_SSP0_TXD signal is used for Flash Descriptor Security Override (which is Intel® ME Debug Mode). This signal input should be tied to a jumper which connects the input to power through an external pull-up (1 KΩ ±5%) ONLY. When this signal is asserted, the Flash Security gets overridden for ease of image programming.

Customers are encouraged to implement this jumper - only on pre-productions designs, to be able to re-flash the SPI Flash device by customers technicians and/or by Intel Debug teams, when asking for their help. This jumper may be removed from the board design before final production.

# 33.7 Intel® APS

The Intel® APS is a tool that is used by the Intel® Platform Enablement Test Suite (Intel® PETS) tool. The Intel® PETS tool is used to test compliancy to Intel® ME requirements and is a validation vehicle to assist with the reproduction of power

management and power sequencing issues. The Intel® APS signals are required to be present at an accessible location on the board. Routing these signals to a connector is strongly recommended and will contribute significantly to accelerating debug and system validation. If an Intel® PETS run is fully done on pre-production SUT, the Intel® APS connector may be removed from the production system board layout.

An Intel® APS header allows for easy connection to a platform without extensive rework and/or intrusion by grouping signals required by the Intel® APS to a common connector. It is strongly recommended to use one of the two proposed connector options described below.

The first option is to use a 18-pin Flat Flex Cable (FFC)/Flexible Printed Circuitry (FPC) connector, such as the 10051922-1810elf. It's a Lower Side Contact, Side Entry, Surface Mount ZIF Connector with 0.5 mm pitch. The pinout of the ZIF connector is shown in Table 33-5. This ZIF connector should be placed in an accessible location for accessing it without opening the chassis. It could be somewhere under the mobile system keyboard or inside the SSD/DDR module compartment. The keyboard or the SSD/DDR back cover could be lifted and the FFC/FPC could be plugged into the proposed ZIF connector, as shown in Figure 33-3, Figure 33-4 and Figure 33-5. After well placing the Intel® APS adapter, all the necessary Intel® APS signal lines can be connected to the 18-pin 0.1" (2.54 mm) header of Intel® APS Adapter, as shown in Figure 33-6. Please contact Intel representative for information of the Intel® APS Adapter and the FFC/FPC.

**Figure 33-3. Location of ZIF connector, FFC/FPC and Intel® APS Adapter**

**Figure 33-4. An Intel® Automatic Power Switcher (Intel® APS) Adapter with a FFC**

**Figure 33-5. An Intel® Automatic Power Switcher (Intel® APS) Adapter**

**Figure 33-6. Intel® Automatic Power Switcher (Intel® APS) Adapter connected**

The second connector option is to use a single 18-pin (2 rows of 9 pins) male header with pin width of 0.64 mm, pin height of 5.84 mm and a 2.54 mm distance (pitch) between pins, as shown in Figure 33-7. The pin-out of the 18-pin male header is shown in the Table 33-5. These pins can be connected directly to Intel® APS. The Intel® APS Adapter is not necessary.

When system gets to the production stage, and if the Intel® ME subsystem is fully functional and is fully validated on pre-production systems, the Intel® APS connector may become “UN_STUFF” (meaning, not being placed on the board). It is recommended to leave the footprint of Intel® APS connector with 'APS' label on silk screen next to the footprint on the system board. Please be noted to solder down the Intel® APS connector to the footprint if the system is going to be sent to Intel for Intel® ME sub-system debugging.

**Figure 33-7. Intel® APS Connector**

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### Table 33-5. Intel® Automatic Power Switcher (Intel® APS) Connector

| Pin | Signal Name | Description | Intel® APS Signal Name |
|---|---|---|---|
| 1 | VCCPRIM_3P3 | 3.3V Primary Power Well | SUS |
| 2 | GPD_4_SLP_S3# | When asserted (0) system is in S3 | S3 |
| 3 | NC | No Connection | |
| 4 | GPD_10_SLP_S5# | When asserted (0) system is in S5 | S5 |
| 5 | GPD_5_SLP_S4# | When asserted (0) system is in S4 | S4 |
| 6 | GPD_6_SLP_A# | When asserted (0) Intel® ME is in Moff | M1/OFF |
| 7 | VCCDSW_3P3 | Used to determine if the system is in Deep S4/S5 | INEX1 |
| 8 | GND | Ground | GND |
| 9 | RTCRST# | When asserted (0) CMOS is cleared | |
| 10 | GND | Ground for RTCRST# | |
| 11 | PWRBTN# | When asserted (0) Power Button pushed | PWR B |
| 12 | GND | Ground for PWRBTN# | PWR B GND |
| 13 | SYS_RESET# | When asserted (0) Reset Button pushed | RST B |
| 14 | GND | Ground for SYS_RESET# | RST B GND |
| 15 | GPP_B12_SLP_S0# | When asserted (0) system is in deterministic idle state | |
| 16 | NC | No Connection | |
| 17 | NC | No Connection | |
| 18 | NC | No Connection | |

### Table 33-6. Pin Location for Dual-in-Line Connector

| Signal Name | Pin | Header | Pin | Signal Name |
|---|---|---|---|---|
| VCCPRIM_3P3 | 1 | | 2 | GPD_4_SLP_S3# |
| NC | 3 | | 4 | GPD_10_SLP_S5# |
| GPD_5_SLP_S4# | 5 | | 6 | GPD_6_SLP_A# |
| VCCDSW_3P3 | 7 | | 8 | GND |
| RTCRST# | 9 | | 10 | GND for RTCRST# |
| PWRBTN# | 11 | | 12 | GND for PWRBTN# |
| SYS_RESET# | 13 | | 14 | GND for SYS_RESET# |
| GPP_B12_SLP_S0# | 15 | | 16 | NC |
| NC | 17 | | 18 | NC |

***Notes:***

1. The unused or unconnected signal sampling lines which are INEX3 to INEX5 from the Intel® APS are better to be connected to GND for preventing unexpected measurement results or risk. Without connecting these unused lines to GND, it is possible to damage the Intel® APS hardware. Because of this, it is strongly recommended to provide additional GND pins for the unused INEX sampling lines. For systems that do not implement Deep Sx, five additional GND pins are needed. For systems that do implement Deep Sx, only three additional GND pins are needed.
2. If neither of the two options above is applicable, the Intel® APS signals should be routed to solder pads located near the memory or SSD slots. Therefore the

required signals on a laptop form factor can be easily accessed through the self-service door on the bottom of the platform.

3. It is strongly recommended that the name 'APS' should be labeled on silk screen next to the Intel® APS connector or Intel® APS test pads, and each pin name clearly marked on silk screen on the PCB.

## 33.8 Intel® ME Firmware behavior in Coffee Lake

The power management flow of consumer firmware is the same as Kaby Lake one. Table 33-7 shows the behavior of corporate firmware.

**Table 33-7. Corporate Firmware behavior**

| Power Policy | Power flow changes in Coffee Lake |
|---|---|
| PP1<br>Intel ® ME is on in S0 Only | Intel ® ME will be ON after G3-exit, Deep Sx exit, Type 8 GRST (which is Power Button Override) and will be OFF after reaching its destined Sx State. |
| PP2<br>Intel ® ME is on in Sx State | None |

Refer Intel® Management Engine 12.0 Delta Doc (RDC#570744) or Intel® ME FW documents for more detail.

## 33.9 Schematics Design Checklists

This section provide schematics, PCB and System checklists for Intel® ME Coffee Lake design to help the design review. It should not be used as a substitute for the Design Guidelines. We recommend that customer will make the best design according the design guidelines provided, and will consult with Intel Application Engineer if there is any violation to the Intel® ME Design Guidelines.

### 33.9.1 Overview

Below is a checklist of items containing hardware and EC firmware requirements to support various Intel® ME technologies. If there are any questions to fill out the checklist below please work with an Intel® ME Application Engineer for assistant.

## 33.9.2 Intel® ME Checklists

### Table 33-8. Hardware and EC firmware Requirements Checklist

| Hardware Requirement | Expected Configuration | Verified (Y/N) | Issues/Next Steps |
|---|---|---|---|
| **Intel® ME Requirements – All Platforms Supporting Intel® ME** | | | |
| Intel® ME-EC: Intel® ME-EC connections according to the latest revision of Intel® ME-EC Interaction Specification | | | |
| Intel® ME-EC: Specific focus - SLP_S3# line between EC and PCH | Optional for platforms with M3 support.<br>Required for platforms without M3 support. If SLP_A# is routed from PCH to EC, then SLP_S3# can be optional from Intel® ME-EC perspective. | | |
| Intel® ME-EC: Specific focus - SLP_A# line between EC and PCH | Required for platforms with M3 support.<br>SLP_A# should be routed from the PCH to the EC. SLP_A# asserted low informs the EC when Intel® ME is in an M-Off state. Depending on the platform, this pin may be used to control power to various devices that are part of the Intel® ME sub-system in the platform. | | |
| Intel® ME-EC: Specific focus – ACPRESENT line between EC and PCH | Required for systems with and without M3. The ACPRESENT pin is used by EC to indicate to the Intel® ME the current power source of the system. When asserted, it indicates that the platform is connected to an AC source. | | |
| Intel® ME-EC: Specific focus – SUSPWRDNACK/ SUSWARN# line between EC and PCH | This signal is called GPPC_A_13_SUSWARNB_SUSPWRDNACK in the PCH documentation.<br>This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (using SLP_SUS#). The EC/motherboard controlling logic must observe edges on this pin, preparing for SUS well power loss on a falling edge and preparing for Primary well related activity (host/Intel® ME wakes and runtime events) on a rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#. This pin is multiplexed with SUSPWRDNACK since it is not needed in Deep Sx supported platforms. | | |
| SLP_SUS# | Deep Sx Indication: When asserted (driven low), this signal indicates PCH is in Deep Sx state where Primary Well is shut off for enhanced power saving. When de-asserted (driven high), this signal indicates exit from Deep Sx state and Primary Well can be applied to PCH. If Deep Sx is not supported, then this pin can be left unconnected.<br>**Note**: This pin is in the DSW power well. | | |
| SUSACK#/GPP_A15 | This signal is called GPPC_A_15_SUSACKB in the PCH documentation. Active low signal is an input to the PCH (driven by the EC) and is involved in Deep Sx entry and exit flows. For more information about SUSACK#, refer to the "Cannon Lake Platform Controller Hub (PCH-H) - External Design Specification (EDS) - Volume 1 of 2" RDC#571182. For platforms that do not support DeepSx mode, this signal can be left unconnected. | | |

| Hardware Requirement | Expected Configuration | Verified (Y/N) | Issues/Next Steps |
|---|---|---|---|
| Intel® ME Power | Intel® ME is powered by two power wells: the vccprim_core Power well and VCCSPI power supply wells. Intel® ME controls its own internal power states. | | |
| SPI Write-Protect Pin | Must be pulled up to one of the following rails: A rail enabled by of SLP_LAN# or SLP_A#. | | |
| SPI Flash Connectivity | SPI flash must be directly connected to the PCH if the ME FW boots from SPI. | | |
| Timing Parameters and hardware Sequences | Customers should ensure their platform follows the timing constraints spelled out in the "Platform Power Sequencing Specification" chapter in this document. | | |
| Manufacturing Mode Jumper (HDA_SDO/ I2S0_TXD, previously known as HDA_SDO) | Flash Descriptor Security Override/Intel® ME Debug Mode If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default) If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up to 3.3A rail in manufacturing/debug environments ONLY.<br>Note: Asserting the HDA_SDO/I2S0_TXD high on the rising edge of PCH_PWROK will also halt the Intel® ME firmware after PCH bring up and disable runtime Intel® ME features. This enables debug mode system operation and must not be asserted after manufacturing/debug are complete. | | |
| PCH Intel® ME XDP Debug port | Connect the PCH JTAG signals directly to PCH XDP debug port connector as described in the "Platform Debug and Test Hooks" chapter in this document. | | |
| **Intel® ME Requirements – All Platforms Supporting Intel® ME in Sx States (M3)** | | | |
| Intel® ME-EC: Specific focus - SLP_A# line between EC and PCH | Required if platform supports M3, otherwise optional. | | |
| Controller Link: Did you verify that the Controller Link design conforms to the design guidelines? | For Controller Link design guidelines, refer to Section 33.6.1.1, "Intel® ME Wireless Controller Link". | | |
| **Intel® ME Requirements – All Platforms Supporting Intel® Active Management Technology (Intel® AMT)** | | | |
| Power to LAN – hardware connections | LAN must be powered by a rail enabled by SLP_LAN#. | | |
| Power to LAN – Behavior of hardware/ EC firmware | Power to LAN while powered must not be interrupted by either hardware or EC firmware, on any event (including warm reset, power-cycle reset). | | |
| Power to WLAN – hardware connections | To support WLAN out-of-band in both S0 and Sx/AC states, the WLAN device must be powered by WLAN supply well" which is derived by ORing between SLP_A# being high and SUSPWRDNACK being low. To support WLAN out-of-band in S0 state only, the WLAN device must be powered by Core well that is on in S0. | | |
| Power to WLAN - Behavior of hardware/ EC firmware | Power to WLAN, while it's powered due to previous item, must not be interrupted by either hardware or EC firmware, on any event (including warm reset, power-cycle reset). | | |

| Hardware Requirement | Expected Configuration | Verified (Y/N) | Issues/Next Steps |
|---|---|---|---|
| Implement one of the 2 proposed 18-pin Intel® APS connectors | Customers are expected to follow the PDG and implement one of the two Intel® APS connectors recommended in the Section 33.7, "Intel® APS". | | |
| Was CLink layout designed to conform to design guidelines | Customers are expected to follow the PDG and design the CLink according to Section 33.6.1.1, "Intel® ME Wireless Controller Link" | | |

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# 34 Intel® Integrated Sensor Solution

## 34.1 Acronyms

| Acronyms | Description |
|---|---|
| AE | Application Engineer |
| AIO | All In One |
| ALS | Ambient Light Sensor |
| AVL | Approved Vendor List |
| BOM | Bill Of Material |
| CFL | Coffee Lake |
| EC | Embedded Controller |
| FDK | Firmware Development Kit |
| FW | Firmware |
| GPIO | General Purpose Input/Output |
| $I^2C$ | IIC - Inter-Integrated Circuit bus |
| IISS | Intel® Integrated Sensor Solution |
| Intel® ISH | Intel® Integrated Sensors Hub |
| Intel® ME, ME | Intel® Management Engine |
| OxM | ODM or OEM |
| pAIO | personal All In One |
| PCB | Printed Circuit Board |
| POR | Plan Of Record |
| SAR | Specific Absorption Rate |
| SUT | System Under Test |
| uDriver | Micro Driver |
| ZIF | Zero Insertion Force (connector) |

## 34.2 Reference Documents

| Document | Document Number |
|---|---|
| Ultrabook™ Platform - Magnetometer Design Integration - Technical White Paper | RDC#535305 |
| Cannon Lake PCH-H External Design Specification - Volume 1 of 2 | RDC#571182 |
| Cannon Lake PCH-LP External Design Specification - Volume 2 of 2 | RDC#565870 |
| Intel® Integrated Sensor Solution (IISS) POR BOM | RDC#570092 |
| Integrating Motion and Orientation Sensors (by Microsoft*) | https://msdn.microsoft.com/en-us/library/windows/hardware/dn642102(v=vs.85).aspx |



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## 34.3 Introduction

Coffee Lake Platform uses an Intel® Integrated Sensor Hub (Intel® ISH), bearing the name "Coffee Lake Intel® Integrated Sensor Solution" (Coffee Lake IISS). This section provide the implementation recommendations for the Intel® Sensor Solution for 2-in-1 (Detachable), 360 clamshell, pAIO (personal All In One) and AIO (All In One) systems design. The intent of this document is to assist the usage of Coffee Lake IISS and sensor devices in hardware design to meet the Microsoft Windows* 10 Operating Systems sensor recommendations.

It is highly recommended to follow all of the design guidelines and perform all checklists and to not deviate from any of the recommendations outlined in this document to prevent or minimize any functionality or responsiveness risks.

## 34.4 Overview

Coffee Lake IISS is to be used on the Coffee Lake platform with Windows 10* Operating Systems (OS) with the combination of sensors, Integrated sensor hub and Intel® sensor firmware and software. Figure 34-1 shows the sensor solution block diagram including the interconnection between Coffee Lake processor and the sensors.

**Figure 34-1. Intel® Coffee Lake IISS Diagram**

***Notes:***
1. Optional to use on 360° hinge designs
2. More sensors are optional, as described in Section 34.6.3, "BOM Innovation"

Also, refer to Section 34.7.1.1 and Section 34.7.1.2 for example of actually connecting Sensors to the SoC.

## 34.5 Sensors

Intel defined a list of sensors, hereinafter defined as BOM, to support customers with different needs. Intel fully supports sensors defined in the BOM, did full validation cycle on them and now supports it as a turn-key solution.

IISS firmware algorithms support only unprocessed and unfiltered raw data, coming directly from the sensors. The use of firmware with the built-in processor that is available on some sensor devices to pre-process the sensor data is not supported by Intel® ISS Firmware.

In previous IISS generations, it was proposed to use a second magnetometer to be located on the base of a 360 degrees hinge swivel designs, used to detect if the lid was facing up/down. However, this option was eliminated and customers requested to use a simple Hall effect sensor. This Hall Effect solution is now Intel's POR, instead of the second magnetometer.

**Table 34-1. Sensor Types and Supported Form Factors**

| Device | Type | 2-in-1 | Clamshell |
|---|---|---|---|
| 3-Axis Sensors | Accelerometer | POR | POR |
| 3-Axis Sensors | Magnetometer | POR | POR |
| 3-Axis Sensors | Gyroscope | POR | POR |
| 6-Axis Sensors | Accelerometer + Magnetometer | POR | POR |
| 6-Axis Sensors | Accelerometer + Gyroscope | POR | POR |
| 9-Axis Sensors | Accelerometer + Gyroscope + Magnetometer | POR | POR |
| Ambient Light Sensor | Ambient Light Sensor | POR | POR |
| Pressure | Pressure | POR | POR |
| SAR Sensor | Specific Absorption Rate sensor | POR | POR |

***Notes:***
1. IISS firmware algorithms support only unprocessed and unfiltered RAW data, coming directly from the sensors. The use of built-in firmware for the built-in processor that is available on some sensor devices to pre-process the sensor data is not supported by IISS Firmware.
2. However, it is on their own discretion to provide the full chain of components such as the uDriver, validate and resolve all issues in house, as sensor not in the BOM list were not validated by Intel.

## 34.6 Sensors Extensibility Options

One of the most important IISS program objectives is Sensor Extensibility. It refers to the ability for the customer to change the sensor - the flexibility to choose different vendor for the sensor types that are included in the proposed Intel BOM or the option to innovate by selecting a totally new sensor type. Intel has developed the IISS Firmware Development Kit (FDK) to enable the extensibility. Please contact your local IISS AE for a FDK release. Following are the implementation highlights:

### 34.6.1 Baseline

- Sensors BOM can be found in "Intel® Integrated Sensor Solution (IISS) POR BOM".
- Basic: Windows* HCK support.
- Intel differentiated: pressure sensor.
- Advanced algorithms: activity context, device context and gesture.
- Support: Full support (Fully validated on Intel systems, with Intel supported BOM).

### 34.6.2 BOM Flexibility

- Feature Set: Intel baseline.
- BOM: OxMs can choose to replace sensor vendor for supported sensor types.
- Support: Intel provides FW and FDK, OxM integrates customer uDriver.
- uDriver: OxM owns FW integration, calibration, and validation.
- Intel will provide a FDK development toolkit for OxM use.

### 34.6.3 BOM Innovation

- Feature Set: Not validated, but Intel base-line functionality supported.
- BOM: OxMs can choose to add new types of sensors and/or algorithms.
- Support: Intel provides FW and FDK, OxM integrates custom uDriver and algorithms.
- uDriver: OxM owns FW integration, calibration, and validation.

***Note:*** Based on the definitions above, customer may choose any sensor from the market. It is important to be noted that sensors are characterize also by the voltage they use for the $I^2C$ interface and interrupts (defined as Vio), which may be either 1.8V or 3.3V. This means that the Intel® ISH, the sensors and the pull-up resistors all should use the same Vio voltage, either 1.8V or 3.3V. If customer's BOM calls for use of sensors which do not support the same Vio voltage, customer should use a voltage level shifter where appropriate.

## 34.7 Design Integration

Intel highly recommends thoroughly understanding and implementing all of the design requirements outlined in the device data sheet, and following all the requirements specified in this chapter for design integration. Failure to do so may result in sensor malfunctioning and support problem.

The physical locations of the sensors on the motherboard or daughter board, or in the system depend on board placement, system placement, and the form factor. Intel firmware has the flexibility to accommodate for orientation of 0°,90°, 180° and 270° with reference to the recommended orientation in the followed subsections. It's required that the edges of the sensor with directivity or used for fusion are in parallel with the system edge, and they must be placed in a fixed orientation relative to each other. It is recommended to place them on the same board. Selection of individual sensors is based on the operating system requirements and usage models planned for the system.

### 34.7.1 Electrical Design

All manufacturers' data sheets and application notes need to be followed. It is recommended to include signal or function description, trace length and air gap information in schematics where ever possible. Refer to the data sheets for the pin definitions and the reference schematics for the detail interconnections.

### 34.7.1.1 Sensors - I²C Bus Considerations

The sensors may be connected to Intel® ISH through Intel® ISH I²C interface and Intel® ISH GPIO. Sensors can be connected to ISH_I2C0 or ISH_I2C1, but it is recommended not to use ISH_I2C2 as it may be used for other functions.

I²C interface is used for data transmission. It is important to note that Intel® ISH I²C interfaces support I/O voltage with either 1.8V or 3.3V voltage, and sensors are characterized also by the voltage they use. If customer's BOM calls for use of sensors which do not support the same voltage, customer should use a voltage level shifter where appropriate. It is recommended, however, to use sensors which support the same I/O voltage. The I²C interface may run at speeds up to 1Mbps and due to the relatively low speed there are few signal integrity issues to worry about. It is required to ensure the total loading does not exceed the maximum bus capacitive load. There is no specified location for ISH_I2C pull-up resistors, but it is recommended to place the pull-up resistors on motherboard if sensors are on daughter board.

Connecting I²C debug device that has build in I²C pull-up resistors will change the final value of pull-up resistors, and the wrong pull-up resistors can cause Intel® ISH I²C bus not to work. Refer Chapter 23, "I²C* Interface Design Guidelines" in this Design Guide.

Refer to the sensor data sheets for selecting the correct power voltage (3.3V or 1.8V) for the sensor components. For the component that have a separated I/O power supply, please select the corresponding voltage (Vio) level according to the voltage level of I²C bus. For 1.8V I²C, an 1.8V I/O power supply is needed. For 3.3V I²C, a 3.3V I/O power supply is needed.

***Note:*** Please be noticed on your early designs. It is strongly recommended to reserve pads of series resistor and stuff with 0 Ohm resistors on Intel® ISH I²C clock and Intel® ISH I²C data lines. Designers could separate sensor components onto ISH_I2C0 and ISH_I2C1. By doing this, it can keep flexibility of circuits if an adjustment is needed on your PCB.

### 34.7.1.2 Sensors - GPIO Considerations

For sensor interrupt, the Intel® ISH GPIO pin is configured as an input and connect to the interrupt output of a sensor. **Intel strong recommend that sensor components should not share one or more interrupt line(s). Intel® ISH FW does not support it.**

For Lid-close sensor (as-known-as hall sensor), it is strongly recommended to add an additional route of Lid-close interrupt output to the Intel® ISH GPIO if the Lid-close sensor interrupt is already connected to EC. It is must in a 360-degree clamshell design. By doing this, it can help Intel® ISH FW to distinguish and calculate the correct angle between the lid and the base. For example, the angle of 0 and 360 degrees in a 360-clamshell design.

For a 360-degree clamshell design which needs a 2nd accelerometer on the base, and other sensors are on th lid. In this case, some of Intel® ISH GPIO pins are configured as output. With Intel® ISH virtual sensor support, Intel® ISH FW can trigger outputs to EC via these GPIO pins. One pin can represent two modes, two pins can represent four modes and so on. Usually two pins are enough. For example, if we divide the angel between the lid and the base into 4 regions, 0~5 degrees means lid close, 355~360 degrees means tablet mode, 15~185 means clamshell mode, 195~345 means book mode. Two GPIO pins can represent 4 modes and so on. The EC can read these two pins to know which mode it is now. Based on this information, The EC can control on/off

to keyboard, touchpad and more.

Figure 34-2 is an example of I²C bus and interrupt connection. All interrupts should have its owned pull-up resistors for supporting Open Drain configuration in Intel® ISH FW. Please also refer the sensor vendor datasheet for the corresponding interrupt connections.

**Figure 34-2. An example of ISH_I2C and ISH_GP connection**

As can be seen in Figure 34-2, interrupt connections of Gyroscope, Magnetometer, Human Proximity and Barometer sensors to the Intel® ISH are not required although the sensors offer this capability. The Intel Basic BOM uDrivers are not utilizing these interrupt requests from these sensors. If designer wishes to use interrupts from these sensors, a new sensor uDriver is needed to be developed to each sensor with IISS FDK.

### 34.7.1.3 Sensors - Configurable Voltage Considerations

Refer to "Cannon Lake Platform Controller Hub (PCH-H) - External Design Specification (EDS) - Volume 1 of 2", RDC#571182, section 17.4.1. Except Group F and GDD, configurable voltage selection per pad is supported in most of GPIO groups since CNP (which is CNL PCH). The configuration is done via soft straps during booting. Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.

- Input: 1.8V level with 3.3V tolerant.
- Output: the pin drives 3.3V via a ~20K pull-up. With this, any 1.8V device must be capable of taking 20K pull-up to 3.3V.

***Warning:*** GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

## 34.7.2 Layout and Assembly

All manufacturers' datasheet, application notes and design recommendations for mechanical placement, soldering and assembly must be followed. **For the combo parts that have more than one sensor in it, the guidances for all the built-in sensors need be followed.**

The general rules:

- **Please make the sensor placement to be the first step when outlining a new PCB layout. Plan accordingly accommodating to both of board and system level.**
- Please understand and follow all the layout and design rule requirements from the sensor vendors and manufacturers.
- Please place sensor 2 or 3 cm away from hot devices to avoid large temperature gradient.
- Please place sensors at interference-free locations on the board in the system for all usage models.
  - Place motion sensors in a stable position and isolated from any vibration.
  - Place magnetometer away from magnetic interference.
  - Place the ambient light sensor away from any unwanted lighting sources (for example: a LED indicator) in the system. Also make sure that the ambient light is not blocked.
- Please Do NOT place the sensor in a region of PCB that can warp as it can cause package stress which causes shift.
- Please Do NOT place the sensor at the position which has unsymmetrical stress coming from PCB deformation as it will cause drift.
- Please design for manufacturing: Design a system that the board is easy to be assembled in and ensure the board is fixed firmly and there is no flex after the assembly.
- It is strongly recommended on the top metal layer, the area just below the sensor component, not to place any metal structure such as via, trace, plane and etc., meaning no metal entity under the sensor component on the PCB.

## 34.7.3 Form Factor Considerations

This section illustrates the sensor placement for form factors such as Ultrabook™ 2-in-1 (Slider, Twist, Ferris Wheel, 360 hinge, dual Screen, etc.), Ultrabook Detachable, Ultrabook Clamshell and pAIO (portable All In One).

For all the form factors, it is recommended to place the main motion sensors behind screen or in the LID, and place the 2$^{nd}$ accelerometer for 360-Hinge design in the base.

For low-cost clamshell design which only supports screen rotation, the accelerometer sensor can be placed in the base.

**System/Chassis Integration Options:**

- Clamshell: Main sensors behind the screen or in the Lid. For low-cost design, the accelerator sensor can be in the base.

**Figure 34-3. System/Chassis Integration Options: Clamshell**

- Detachable: Main sensors behind the screen or in the Lid.

**Figure 34-4. System/Chassis Integration Options: Detachable**

- 2-in-1 with 360 hinge: Main sensors behind the screen (LID) while the 2nd sensor in base.

**Figure 34-5. System/Chassis Integration Options: 2-in-1 with 360 Hinge**

- Other 2-in-1: Main sensors behind the screen (LID) or in the LID.

**Figure 34-6. Other 2-in-1: Main A, G, M sensors behind the screen or in the Lid**

- pAIO: Main sensors behind the screen (LID)

**Figure 34-7. System/Chassis Integration Options: pAIO**

### 34.7.3.1 Ambient Light Sensor (ALS)

The ALS must be placed in the lid as close as possible to the camera module (if present), in order to allow effective control of screen brightness based on ambient light. The performance of the display brightening is ultimately defined by the performance of ambient light sensor and dimming to specified LCD luminance levels in response to lighting changes. While the firmware has the ability to control the ALS signal gain and the LCD luminance response, proper mechanical design is still required to ensure the right user experience. Several hardware features must be considered when integrating ambient light sensors into PCs.

- **ALS Characteristics:**

**Table 34-2. ALS Characteristics**

| Characteristic | Specification | Notes |
|---|---|---|
| Illuminance Range | 5-100k lux | As output through sensor module which includes optics, surfaces, calibration data and etc. It's not only related to the bare sensor. |
| Accuracy | +/- 10% | As output through sensor module which includes optics, surfaces, calibration data and etc. It's not only related to the bare sensor. |
| Type | Digital | 16-bit resolution |
| ALS IR/UV rejection | Supported | Important for consistent measurement |

- **Aperture Placement:**

The light sensor aperture is required to be located on the same plane as the display which is facing the user. This is necessary because the sensor measures the lighting conditions facing the user for supporting adaptive brightness and light-aware applications that display their content on the screen.

  — Please avoid placing the light sensor in areas of the computer that are likely to be obscured from the light source or sources by shadows.

  — Figure 34-8 illustrates an example of user scenario in which a direct light source is behind the user. A shadow is cast over the lower half of the screen and the base of the computer. This scenario suggests that the optimal light sensor placement is near the top of the screen and facing the user.

### Figure 34-8. Ambient Light Sensor Cross Section

- **Aperture Size:**

The aperture must be wide enough to detect light without significant attenuation when the light source is at an angle to the device or from a diffused source. A hole too small or too deep could cause a "Shadow Effect" which reduces the usability of the ALS sensor.

OEM should work with their sensor manufacturer to determine the minimal and optimal aperture size.

### Figure 34-9. Ambient Light Sensor Cross Section

- **Optical filter**:

In some instances, an optical film or ink coating may be applied to hide the ALS optical cavity. **The filter must be designed to allow at least 80% of visible wavelength light to pass.** That is, a light meter placed behind the film must register at least 80% of the LUX value from a direct light source that it registers with the film removed.

- **Light pipe**:

A light pipe constructed from a light-conducting material may optionally be deployed to increase the light-gathering ability of the optical cavity. This may be required in cases where the ALS optical cavity is excessively deep, inhibiting light gathering from off-axis (i.e., angled) and diffused light sources.

- **Cover Consistency of Glass/Cover**:
  - The glass or plastic covering material must be consistent across the units of the same SKU/Model. Failure to follow this recommendation will result in inaccurate readings from the ALS based on the per Model-Calibration parameters.
  - Care must be taken when placing the Glass/Cover; a misalignment would mask out some of the light and produce unexpected readings from the ALS.

### 34.7.3.2 Gyroscope

- The X, Y and Z axes of the sensor chip orientation is recommended to match the diagram below.

**Figure 34-10.Gyroscope X, Y and Z Orientation**

- Gyroscope must be mounted securely, near a screwed standoff point, and can not move independently.
- Gyroscope must be placed in a stable position and isolated from any vibration including transmitted vibration, air pressure change vibration and etc.
- It is recommended that gyroscope is kept a distance of 30 mm from audio speakers, fans and haptic vibration motors.

### 34.7.3.3 Accelerometer

- The X, Y and Z axes of the sensor chip orientation is recommended to match the diagram below.

**Figure 34-11.Accelerometer X, Y and Z Orientation**

- Accelerometer must be mounted securely, near a screwed standoff point and can not move independently.
- Accelerometer must be placed in a stable position and isolated from any vibration including transmitted vibration, air pressure change vibration and etc. It is recommended that accelerometer is kept a distance of 30 mm from audio speakers, fans, and haptic vibration motors.
- Many modern electronic accelerometers have the ability to perform on-board filtering e.g., the purpose of removing DC gravity components in the signal. All accelerometer signal conditioning and signal thresholding are performed within the integrated sensor hub firmware.

### 34.7.3.4 Magnetometer

- The X, Y and Z axes of the sensor chip orientation is recommended to match the diagram below.

**Figure 34-12.Magnetometer X Y and Z Orientation**

- **Please make the magnetometer placement the first step when outlining a new PCB layout.** The ideal location for the magnetometer is to be as far away as possible from magnetized components, high current components or traces. The best locations are often to be found on an edge or at a corner of the PCB.
- Please must be placed at least 40 mm from any rare earth magnets (speaker magnets, LID magnets, etc.), and inductors.
- Please must be placed at least 30 mm from any large/thick (structural) ferrous metals, the components which includes the magnet of a hard disk, digitizer, the components with the magnetism of 100 Gauss.
- Please keep a minimum distance of 10 mm from the components which include microphone, vibration motor, magnetic switch, transformer, camera module, beeper, battery, SAW filter, antenna, power amplifier, choke, LCD rear case and the components with the magnetism of 5 Gauss.
- Please keep a minimum distance of 5 mm from the components which include Memory/SIM card socket, USB connector, other connectors, screw, nut, spring, EMI

shielding part, the components with the magnet-conductive material (Iron, Cobalt, Nickel).

- 2 mm away from the surrounding resistor and capacitor since nickel plating is usually present on solder end caps of surface mount components.
- **Please keep away from the power trace (including power or ground plane) on all the PCB layers or component on both PCB sides or out of the board with the variable current higher than 10 mA. For instance: keep a minimum distance of 20 mm from the trace that carries the variable current of 100 mA or keep a minimum distance of 25 mm from the trace that carries the variable current of 200 mA.**
- **Constant current has the interference as magnet. The magnet field created by it is found using the following equation. Please make sure the interference does not cause the output of the magnetometer over the measurement range of the magnetometer.**

$$B = \frac{m_0 * I * L}{2\pi R \sqrt{(L^2 + 4R^2)}}$$

B = magnetic field strength in Teslas

$m_0$ = permittivity of free space ($4\pi * E^{-7}$ T*m/A)

I = current in Amps

L = Conductor length in Meters

R = Radius in Meters

- Please Do NOT cover the magnetic sensor with any material that can block the static magnetic field from magnet and earth.
- As far as possible from mechanical based HDDs, vibrators, hearing aid coils and battery connector which contain ferromagnetism, high frequency circuits and power circuits.
- Please make sure LCD back shell, shield (for RF, BT…) and mechanical part (key, screw, connector) do not contain ferromagnetism material (Fe, Co, Ni).
- The same rules apply to the opposite side of the board.
- The same rules apply to any daughter boards or other components sandwiched in proximity to the magnetometer.
- Please make sure the rules are followed in all the usage models. (Example: with magnetometer in the lid, consider components on the base in tablet mode.)

***Note:*** For the means to calculate the possible interference, refer to Magnetometer Design Integration Challenges - White Paper, RDC#535305.

All digitizer solutions that employ a ferrous-based shield are unsuited for deployment with the magnetometer. Digitizers that require a ferrous-based shield are not supported by Intel due to the excessive soft iron distortion induced on the e-Compass. Other platforms possessing digitizer solutions that do not require a ferrous-based shield must conform to the general platform guidance for deploying magnetometer.

### 34.7.3.5 Pressure Sensor

In order to achieve the specified performance for your design, the following recommendations when mounting a pressure sensor on a printed-circuit board (PCB):

- The clearance above the sensor package shall be 0.1mm at minimum.
- For the device housing appropriate venting needs to be provided in case the ambient pressure shall be measured.
- Liquids shall not come into direct contact with the device.
- During operation Pressure sensor is sensitive to air pressure variation, fast heating and light heating which can influence the accuracy of the measurement.
- The pressure sensor should not be placed at the position where has unwanted fast air pressure variation caused by fans, speaker etc.
- The pressure sensor shall not be placed close the fast heating parts in case of gradients > 3°C/sec. it is recommended to follow the vendor's application note and contact the vendor representative for details.
- The area below the sensor (on the same side of the board) must be defined as keep-out area. It is strongly recommended not to place any structure in top metal layer underneath the sensor.

### 34.7.3.6 SAR (Specific Absorption Rate) Sensor

SAR sensor is used as a proximity sensor to identify conductive objects (human body parts such as ear, head, lap and torso) presence near the transmitting system antenna. The purpose of the SAR sensor is to allow a device to transmit at higher powers when not located in close proximity to a body and operate at lower powers when close to the body. Many regulatory bodies globally are aligning to International RF exposure guidelines or the FCC limits, as defined below. Examples are when the user brings the transmitting system close to his head (mobile phone) or when the system is used on the person's lap.

Relevant systems are those mobile systems that use wireless communication (transmission) of voice and/or data, including wearables, mobile phones, tablets, phablets, ultrabooks, laptops, some personal AIO (All In One) systems and more.

SAR needs to be evaluated for transmitters operating anywhere in the RF spectrum (9KHz - 300GHz) and so it is relevant to cellular technologies, Wireless LAN technologies and many other wireless technologies supporting data and/or voice.

SAR requirements limit the levels of transmitted RF power to ensure that the power absorbed by a human body is below certain limits established by regulatory bodies around the world. This may require that a device reduce its RF transmitting power when it is in close proximity to the human body. In these systems, the SAR sensor activation is used to allow the device to operate at a higher power (and increased operating range) when the antennas are not close to a body but then reduce the transmission power of the relevant antenna to ensure compliance with the RF exposure requirements.

Transmission power control was simple when there was WWAN (3G/4G/LTE) modem only, SAR output was connected directly to the WWAN modem, directly controlling the Cellular transmitter. The problem started when smart phone with IP phone emerged, so now there may be a need to control the output power from both WWAN and Wi-Fi. Co-SAR section below describes it.

### Regulation Sources

The following are the 2 RF exposure requirements for devices that are used in close proximity to the body (within 20cm). As this can be a changing field, the data published in this section is as it was known in the time of publishing of this document:

- United States: The relevant FCC requirements for the FCC requires that devices used in close proximity to the body have a SAR level below 1.6 watts per kilogram (W/kg) measured over the volume containing a mass of 1 gram of tissue that is absorbing the RF energy.
- European Union: CENELEC specify SAR limits within the EU, following IEC standards (IEC 62209-2:2010). For devices used in close proximity to the body, the SAR limit is 2.0 W/kg measured over the volume containing a mass of 10 grams of tissue that is absorbing the RF energy.

### Co-SAR

A simple SAR sensor control over Antenna power is described in Figure 34-13. In this way, the SAR sensor directly controls the WWAN transmitter power. This is the most efficient way remain compliant with the RF exposure requirements without any additional logic.

**Figure 34-13.Simple SAR Sensor Control over WWAN Antenna Power**

In more sophisticated systems, where system support both WWAN phone and IP phone (Such as WWAN and Wi-Fi).

Figure 34-14 shows a recommended way to control antenna power using an algorithm that runs on the Operating system (OS). In this way the OS has control over each antenna, to control the transmitted power, to ensure compliance with RF exposure requirements.

**Figure 34-14.Co-SAR Sensor Control over WWAN Antenna and Wi-Fi Antenna Power**

### Design Guidelines

There are 2 main relevant usage models that should be covered by SAR sensors, used to reduce antenna transmission power:

- When bringing the system to the users' ear, so phone speaker (and RF antennas) is closed to the users' ear and head. This is mainly relevant to "Mobile Phone" systems, such as handsets and phablets.
- When placing the system on or close to other human body parts, such as the lap or torso. This is mainly relevant to laptop/clamshell, tablets, phablets and similar types of devices.

1. The sensor electrode may be a simple copper area on a PCB or FPC (Flexible PCB) for example with an adjacent reference ground area. Sensor electrode capacitance (to ground) will vary when a conductive object is moving in its proximity.
2. The sensor electrode needs to be located close to the antenna, or antennas, that it is controlling. Having the sensor be away from the antenna makes trigger distances unreliable. The size, shape and position of the sensor electrode are largely dependent on the system usage model. Typically, the sensing area (position) for on ear detection is around the speaker, at the top of the (for example) mobile phone, near the camera etc.
3. Conductive tape (copper tape) works well for prototypes, while FPC is suggested for mass production.
4. Keep the SAR sensor area away from area that human finger touches, such as a touch screen, systems' buttons, keyboard etc. There is no need to throttle antenna power in such a case as the extremity SAR requirements are 2.0 W/kg over 10g of tissue mass.
5. Robust electrode design is the one that minimizes environmental (parasitic) capacitance noise value and variation of it.
6. Power reduction values need to consider both the stand-alone use of a transmitting antenna and simultaneous transmissions from multiple antennas, where supported. The combined SAR value from these antennas needs to meet the relevant limits.
7. System design considerations need to ensure that the default power state is always the reduced power state such that if the SAR proximity sensor circuitry is failed.

8. The software controls need to be robust and must not be user accessible (i.e. the user must not be able to modify the power reduction settings or disable the sensor). Firmware and software updates need to be carefully tested to ensure that the proximity sensor functions are not bypassed.
9. Where the proximity sensor enables large power reduction regulatory bodies such as the FCC may expect to see a description of how the sensor performance is verified across production units. This may necessitate the use of test software and test fixtures and sampling at the production floor. Large power reduction values can trigger device surveillance testing by regulatory agencies so quality control at the production level is important.
10. In general, wherever possible, place the transmitting antennas in areas not accessible to human body parts, so eliminate the need for SAR sensor circuits and the need to lower transmission power. This is difficult in tablets, 2-in-1 and phones which are small and difficult to have an antenna that would not be in close proximity. For tablets it makes sense to keep the antennas toward the front (screen side) of the device to maximize separation from person. Other items to suggest here might be the ability to keep antennas that might operate simultaneous (Wi-Fi and WWAN in hot spot mode, for example) as far apart as possible to reduce the need for power reduction in those modes.

**Device Requirements**

The device selection, electrode and circuit design need to meet the following minimum requirements:

1. The sensor electrode needs to be placed on the inner side of the back cover, close to the transmission antenna, and properly shielded with ground to minimize the interference from the surrounding electronics. The shield needs to be tied to the platform ground to remove the ground bouncing noise and false proximity detection from the platform ground traces.
2. Sensor should be placed very close to the electrode to reduce noise. Routing from sensor electrode to sensor needs to be co-ax cable with ground shielding.
3. Sensor proximity range requirement needs to be determined after SAR testing, but can start with 10mm from the back and side close to where the transmission antennae are placed in the form factor system.
4. Sensor detect range should be 0-60pF with distance of 20mm from a human body part.
5. SAR sensor circuit power needs to be less than 0.1 mW.
6. SAR sensor proximity range for human body and other non-conductive material (such as tablet top) should have big enough delta so that it can be programmed/ tuned to detect only the human body proximity and not other non-conductive material.

## 34.7.4 PCB and Cable Routing

For the $I^2C$, and other signals routing between Intel® ISH and the sensors, refer to the corresponding sections in the PDG. **Please do not route the cables that have power wire close to the magnetometer.** For other partitions, please follow the manufacturers' requirements.

#### 34.7.4.1 Soldering Recommendations

For soldering guidelines refer to the corresponding documents from the sensor vendors or consult the sensor vendor.

### 34.7.5 Sensor Problem Areas

#### 34.7.5.1 Ambient Light Sensors (ALS)

The ability of the ALS to gather light is almost completely determined by the glass/cover, the size and depth of the optical aperture, the use of optical pipes and the quality of the ALS sensor. Inconsistent coating with the glass/cover can cause inconsistent light transmittance. The light transmittance consistency must be with 5% tolerance to avoid per-system calibration.

#### 34.7.5.2 Gyroscope

Measurement of Gyroscope output from several instances of the STM L3GD20H Gyroscope show approximately +-5% variation from the actual rotation rate when measured on Table 34-3. The table shows the cumulative probability distribution of readings from the Gyroscope when rotating at 200 dps.

The measurements show that there is a wide variation in the performance of individual parts. A perfect set of measurements would show a collection of straight vertical lines clustered at 200 dps.

**Table 34-3. Rate Table: The cumulative distribution of Gyroscope output at 200 dps**

The amount of error was examined at three different speeds which are 60 dps, 200 dps, and 300 dps. The percentage of error remains almost constant with changes in speed. This means that the absolute value of the error observed in gyro measurements will increase with speed. For example, there is almost 8dps variation at 200dps rotation and almost 12dps variation at 300dps rotation.

**Table 34-4. Variations of Gyroscope output at different mDPS**

| Ref. value in mDPS | Max/Min/Low M./High M. | Real value in mDPS | Delta | Percent of Error |
|---|---|---|---|---|
| 60,000 | Max | 64,827 | 4,827 | 8% |
| | Min | 55,488 | 4,512 | 8% |
| | Low Median | 57,896 | 2,104 | 4% |
| | High Median | 62,673 | 2,673 | 4% |
| 200,000 | Max | 210,597 | 10,597 | 5% |
| | Min | 191,234 | 8,766 | 4% |
| | Low Median | 193,211 | 6,789 | 3% |
| | High Median | 207,911 | 7,911 | 4% |
| 300,000 | Max | 314,836 | 14,836 | 5% |
| | Min | 286,172 | 13,828 | 5% |
| | Low Median | 288,828 | 11,172 | 4% |
| | High Median | 311,637 | 11,637 | 4% |

The variation could be compensated with a simple multiplier. However, finding the amount of variation would require running each instance on a rate table at a known speed and computing scaling terms for each axis. It is difficult and time consuming to perform this procedure on the factory floor.

The sensor fusion core that produces the Orientation, Inclinometer, and Compass virtual sensors uses Gyroscope as the primary input for orientation changes. The fusion algorithms continually crosscheck the Gyroscope against the accelerometer and magnetometer readings to compensate for Gyroscope error. However, if the device enters an area where the magnetometer confidence is low, the error in the Gyroscope may accumulate and result in heading error.

Applications directly using the Gyroscope through the Windows* APIs must anticipate error in the Gyroscope readings.

### 34.7.5.3 Accelerometer

Inconsistent assembly can cause different accelerometer data offset.

Issue Replication Steps:

- System laid flat on leveled surface and Microsoft Sensor Diagnostic Tool showed system appeared to be moving (For example, XYZ accelerometer values are non-zeroes).
- Output from Gyroscope device showed system appeared to be rotating.

Root Cause 1: Sensor device was placed near screw holes.

EFFECT: Board bends when screwed to chassis causes the sensor to skew, not leveled in referenced to the chassis.

WORKAROUND:

1. Relocate sensor device away from screw hole.
2. Per-System Calibration.

Root Cause 2: Assembly house SMT machines inconsistent placements

EFFECT: Sensors soldered on the board are skewed in referenced to the main board/ daughter card.

WORKAROUND:

1. Provide tighter SMT machine tolerance level.
2. Per-System Calibration.

#### 34.7.5.4 Pressure Sensors

Pressure sensor is sensitive to air pressure variation, fast heating and light. Please do not place pressure sensor close to fan, speaker and etc that can cause air pressure variation and fast heating part. Please do not expose pressure sensor to light heating.

#### 34.7.5.5 Magnetometer

For the magnetometer enabling challenges refer to Magnetometer Design Integration Challenges - White Paper, RDC#535305.

## 34.8 System Debug

System debuggability is an important part of the HW design, providing the ability to access the internal parts of the system without harming the system chassis too much. Intel embeds several debug features into its components that requires hardware debug

hooks to be available on the system. This chapter is the design guideline to help the designer to implement Coffee Lake IISS debug hooks on customer's systems. It's for customer's team to be able to debug their systems, if needed.

Also, there are certain issues that customer can not resolve them, and require Intel's assistance to debug it. When system is sent to Intel for debugging, Intel expect these debug hooks to be implemented on customer's system. Otherwise, it will be difficult for Intel to assist within the stipulated time frame.

Debugging Coffee Lake IISS may be divided into two main areas:

- Firmware debug
- Sensor debug

These issues are discussed in the following sections.

## 34.8.1 Firmware Debug Hooks

The Firmware debug and its debug hooks are fully defined in Chapter 46, "Platform Debug and Test Hooks".

***Note:*** The Firmware Debug Hook is used to support multiple components on the system, such as the CPU, Intel® ME and etc. It is not specific to Intel® ISH.

## 34.8.2 Sensors Debug Hooks

Coffee Lake IISS is composed of the embedded Intel® ISH, its communication lines (which are $I^2C$ and GPIOs as in below table) to the sensors and the sensors themselves. Accessing sensors traces is required in order to test and/or debug the Coffee Lake IISS system.

Coffee Lake IISS debug is based on connecting debug equipment to the following traces, to resolve issues with sensors.

| Connection | Function |
|---|---|
| ISH_I2C[1:0] | $I^2C$ port [1:0] |
| ISH_GPIO[15:0] | Up to 4 Interrupt GPIOs due to predefined pins on Intel® ISH Debug Adaptor. The rest of 6 pins are Intel reversed on the same adaptor. |
| Vio | Sensors Reference Voltage |

IISS requires the above traces to be routed to a connector which should be mounted on the system board in an easy accessible location.

For the dense PCB systems, such as is the 2-in-1 (Detachable) and clamshell systems, a solution involving an adaptor that is proposed, as defined in Section 34.8.2.1.

For a less dense PCB systems, as are the pAIO and AIO systems, the customer may select if to adopt the adaptor solution as in Section 34.8.2.1 or a solution of placing a simple 0.1" header on the pAIO or AIO PCB, as described in Section 34.8.2.2.

Not implementing one of the debug connectors as proposed above will limit the customer in debugging system and will limit Intel debug team in supporting the customer when brought it to Intel for assistance. When system is sent to IISS debug team, a debug connector is expected to be available and accessible.

The debug connector may be eliminated from production systems. Therefore, customer is proposed to replace it with test pads.For easy blue wire soldering, in case more validation or debug will be required. It is proposed to clearly mark these test pads with silk screen writing on the PCB for easy identification.

### 34.8.2.1 Sensors Debug Hooks for 2-in-1 (Detachable) and Clamshell Systems

All the 2-in-1 (Detachable) and clamshell systems (and some pAIO systems too) are dense systems, enclosed inside a chassis which is very delicate and may be damaged when opening chassis for accessing internal traces on debugging.

To overcome this problem, Intel recommend customer placing a small connector on the PCB, to provide all the sensor debug traces located in an easily accessible location, such as under the keyboard(Figure 34-16), inside the DDR compartment, the WLAN module compartment or the SSD compartment.

In order to access this connector to share the traces on the connector with external test/debug equipment, Intel developed an adapter (Figure 34-15), providing the ability for the external test/debug equipment to connected the connector on the main board. To obtain such adaptor, please contact local Intel® ISH AE.

**Figure 34-15.Adapter and Ribbon Cable**

When the system gets to the production stage, and if the Coffee Lake IISS is fully functional and was fully validated on pre-production systems, the debug connector may become “UN_STUFF” (meaning, not being placed on the board). It is, however, recommended to leave connectors’ footprint on the system board layout without being populated, in case future debug is required.

***Note:*** Solder the debug connector to the footprint, if the system is going to be sent to Intel, for IISS debug support.

The connector to use on the main board is a 18-pin FPC/FFC Lower Side Contact, Side Entry, Surface Mount ZIF Connector with a 0.5 mm pitch, such as the 10051922-1810elf, and using the pinout shown in Table 34-5. This connector should be placed in an easy accessible location as described above.

### Optional Locations of the ZIF Connector

The ZIF connector may be placed on the system in location where it will be easy to connect the adapter and hopefully will not require opening the chassis to access it. The adapter will then be extend out of the chassis, so the connection of test/debug equipment will be direct to the 0.1” spacing header which is part of the adapter. Figure 34-16 through Figure 34-19 propose optional locations and connecting technologies.

**Figure 34-16.Proposed Location for ZIF Connector - under the keyboard**

**Figure 34-17.Proposed Location for ZIF Connector - under the keyboard**

**Figure 34-18.Connecting Debug Adaptor to an I²C sniffer**

**Figure 34-19.Proposed Usage of ZIF Connector Inside SST Compartment**

Once the 0.1" header part of the adapter is out of the chassis, it is now easy to hook debug equipment (Such as an I²C sniffer or an oscilloscope channel) to it, as in Figure 34-20, for a debug session.

**Figure 34-20.Connecting Test/Debug Equipment to the Adapter**

Table 34-5 defines the pin configuration of the external 2x9 pin 0.1” spacing header.

### Table 34-5. Pin Location for Dual-in-Line Connector

| Signal Name | Pin | Header | Pin | Signal Name |
|---|---|---|---|---|
| ISH_I2C0_SCL | 1 | | 2 | ISH_I2C0_SDA |
| ISH_I2C1_SCL | 3 | | 4 | ISH_I2C1_SDA |
| GND | 5 | | 6 | GPIOa |
| GPIOb | 7 | | 8 | GPIOc |
| GPIOd | 9 | | 10 | GND |
| Reserved by Intel | 11 | | 12 | Reserved by Intel |
| Reserved by Intel | 13 | | 14 | Reserved by Intel |
| Reserved by Intel | 15 | | 16 | Reserved by Intel |
| GND | 17 | | 18 | Vio |

Table 34-6 defines the pin configuration of the internal 18 pins ZIP connector.

### Table 34-6. 18-pin ZIF Connector Pinout

| Pin | Pin function | Description |
|---|---|---|
| 1 | ISH_I2C0_SCL | Clock line for the I2C0 |
| 2 | ISH_I2C0_SDA | Data line for the I2C0 |
| 3 | ISH_I2C1_SCL | Clock line for the I2C1 |
| 4 | ISH_I2C1_SDA | Data line for the I2C1 |
| 5 | GND | System Ground |
| 6 | GPIOa (1) | Connect here one of the GPIOs in use |
| 7 | GPIOb (1) | Connect here one of the GPIOs in use |
| 8 | GPIOc (1) | Connect here one of the GPIOs in use |
| 9 | GPIOd (1) | Connect here one of the GPIOs in use |
| 10 | GND | System Ground |
| 11 | Reserved by Intel | Do not use |
| 12 | Reserved by Intel | Do not use |
| 13 | Reserved by Intel | Do not use |
| 14 | Reserved by Intel | Do not use |
| 15 | Reserved by Intel | Do not use |
| 16 | Reserved by Intel | Do not use |
| 17 | GND | System Ground |
| 18 | Vio | Sensors Reference Voltage |

***Notes:***

1. GPIOa, GPIOb, GPIOc and GPIOd are place holders for customer design GPIOs. Customer should connect to these pins his Intel® ISH GPIOs, to be able to connect them to a debug equipment, at the time of need.
2. It is strongly recommended that the name 'Coffee Lake Intel® Integrated Sensor Solution' be labeled in silk screen next to the ZIF connector and/or pads, and each pin name clearly marked in silk screen on the board.

### 34.8.2.2 Sensors Debug Hooks for pAIO and AIO Systems

pAIO and AIO form factors are less dense so the adaptor solution that was proposed for the 2-in-1 (Detachable) and clamshell systems may be too complicated and not needed.

It is recommended to use a single 18-pin (2 rows of 9 pins) male 0.1" header with pin width of 64 mm, pin height of 5.84 mm and a 2.54 mm distance (pitch) between pins, as shown in Figure 34-21, using the pinout shown in Table 34-7. These pins connect directly to the Sensor debug equipment, such as sniffer or a scope. The Intel® ISH Debug Adapter is not necessary.

**Figure 34-21.Dual-in-Line Header Example**

**Table 34-7. Pin Location for Dual-in-Line 0.1” Header**

| Signal Name | Pin | Header | Pin | Signal Name |
|---|---|---|---|---|
| ISH_I2C0_SCL | 1 | | 2 | ISH_I2C0_SDA |
| ISH_I2C1_SCL | 3 | | 4 | ISH_I2C1_SDA |
| GND | 5 | | 6 | GPIOa |
| GPIOb | 7 | | 8 | GPIOc |
| GPIOd | 9 | | 10 | GND |
| Reserved by Intel | 11 | | 12 | Reserved by Intel |
| Reserved by Intel | 13 | | 14 | Reserved by Intel |
| Reserved by Intel | 15 | | 16 | Reserved by Intel |
| GND | 17 | | 18 | Vio |

## 34.9 Intel® ISS Checklists

This section provide schematics, PCB Layout and System checklists for the Coffee Lake IISS design to support in the design review and provide additional filter to catch design errors. Intel recommends that customer will make the best design according to the design guidelines provided, will run over the following checklist and will consult with Intel Field Application Engineers if there is any violation to the IISS Design Guidelines.

When to use this Checklist?

- Schematics: to be performed after schematics is done before PCB Layout design.
- PCB Layout: to be performed after chassis and PCB layout are done before Gerber.
- System: to be performed after system is fully assembled and powered.

***Notes:***

1. Please be noticed on your early designs. It is strongly recommended to reserve pads of series resistor and stuff with 0 Ohm resistors on Intel® ISH $I^2C$ clock and Intel® ISH $I^2C$ data lines. Designers could separate sensor components onto ISH_I2C0 and ISH_I2C1. By doing this, it can keep flexibility of circuits if an adjustment is needed on your PCB.
2. For the Magnetometer, a special white paper was composed, to support Magnetometer integration. Refer to RDC#535305.

## 34.9.1 Schematics Design Checklists

All labels may be prefixed with ISH_ if needed to differentiate them from other system schematic labels.

### 34.9.1.1 General Schematics Checklists

This section is used to record the actual sensors that the designer selected to use on his/her design. Based on the sensor used, the following tables should be filled by the designer with the specific selected sensors data.

**Table 34-8. Ambient Light Sensor (ALS) Details**

| Ambient Light Sensor (ALS) | Data | Comments |
|---|---|---|
| Sensor Part number? | | |
| $I^2C$ bus the Sensor is connected to? | | |
| $I^2C$ address on the i2C bus? | | |
| Is there an option to use alternative $I^2C$ Address? If so, what is the alternative $I^2C$ Address? | | |
| Interrupt function? (such as Wake or free-fall or Motion detection, etc.) | | |
| Interrupt polarity? (Active high or active low) | | |
| Interrupt I/O buffer type? (Totem Pole or Open drain) | | |
| Is the same interrupt line shared with other component(s)? Intel strongly do not recommend it and support it. | | |
| VDD voltage? (Typically 3.3V) | | |
| VDDIO voltage? Either 1.8V or 3.3V should be same for all sensors connected to the same $I^2C$. | | |

**Table 34-9. Gyroscope Details**

| Gyroscope | Data | Comments |
|---|---|---|
| Sensor Part number? | | |
| $I^2C$ bus the Sensor is connected to? | | |
| $I^2C$ address on the i2C bus? | | |
| Is there an option to use alternative $I^2C$ Address? If so, what is the alternative $I^2C$ Address? | | |
| VDD voltage? (Typically 3.3V) | | |
| VDDIO voltage? Either 1.8V or 3.3V should be same for all sensors connected to the same $I^2C$. | | |

**Table 34-10. Magnetometer Details (Sheet 1 of 2)**

| Magnetometer | Data | Comments |
|---|---|---|
| Sensor Part number? | | |
| $I^2C$ bus the Sensor is connected to? | | |
| $I^2C$ address on the i2C bus? | | |
| Is there an option to use alternative $I^2C$ Address? If so, what is the alternative $I^2C$ Address? | | |
| VDD voltage? (Typically 3.3V) | | |

## Table 34-10. Magnetometer Details (Sheet 2 of 2)

| Magnetometer | Data | Comments |
|---|---|---|
| VDDIO voltage? Either 1.8V or 3.3V should be same for all sensors connected to the same $I^2C$. | | |

## Table 34-11. Accelerometer Details

| Accelerometer | Data | Comments |
|---|---|---|
| Sensor Part number? | | |
| $I^2C$ bus the Sensor is connected to? | | |
| $I^2C$ address on the i2C bus? | | |
| Is there an option to use alternative $I^2C$ Address? If so, what is the alternative $I^2C$ Address? | | |
| Interrupt function? (such as Wake or free-fall or Motion detection, etc.) | | |
| Interrupt polarity? (Active high or active low) | | |
| Interrupt I/O buffer type? (Totem Pole or Open drain) | | |
| Is the same interrupt line shared with other component(s)? Intel strongly do not recommend it and support it. | | |
| VDD voltage? (Typically 3.3V) | | |
| VDDIO voltage? Either 1.8V or 3.3V should be same for all sensors connected to the same $I^2C$? | | |

## Table 34-12. Pressure Sensor Details

| Pressure Sensor | Data | Comments |
|---|---|---|
| Sensor Part number? | | |
| $I^2C$ bus the Sensor is connected to? | | |
| $I^2C$ address on the $I^2C$ bus? | | |
| Is there an option to use alternative v Address? If so, what is the alternative $I^2C$ Address? | | |
| VDD voltage? (Typically 3.3V) | | |
| VDDIO voltage? Either 1.8V or 3.3V should be same for all sensors connected to the same $I^2C$? | | |

## Table 34-13. Optional 2nd Accelerometer (for 360° hinge designs) (Sheet 1 of 2)

| 2nd Accelerometer | Data | Comments |
|---|---|---|
| Sensor Part number? | | |
| $I^2C$ bus the Sensor is connected to? | | |
| $I^2C$ address on the i2C bus? | | |
| Is there an option to use alternative $I^2C$ Address? If so, what is the alternative $I^2C$ Address? | | |
| Interrupt function? (such as Wake or free-fall or Motion detection, etc.) | | |
| Interrupt polarity? (Active high or active low) | | |
| Interrupt I/O buffer type? (Totem Pole or Open drain) | | |



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### Table 34-13. Optional 2nd Accelerometer (for 360° hinge designs) (Sheet 2 of 2)

| 2nd Accelerometer | Data | Comments |
|---|---|---|
| Is the same interrupt line shared with other component(s)? Intel strongly do not recommend it and support it. | | |
| VDD voltage? (Typically 3.3V) | | |
| VDDIO voltage? Either 1.8V or 3.3V should be same for all sensors connected to the same $I^2C$ | | |

### Table 34-14. Intel Sensor Solution BOM Checklist

| Schematic Notes | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Are all the Intel® ISH managed sensors supported in Intel POR BOM on specific platform (ex: KBL, CNL, etc.)? | | | |
| Did you make sure you or your vendor will provide support to you with Intel® ISH FDK if your selected sensor/sensors is/are not in Intel POR BOM? | | | |
| Did you make sure there are no 2 sensors using the same $I^2C$ address on the same Intel® ISH $I^2C$ bus? | | | |
| Did you review the $I^2C$ design and make sure it conforms to the $I^2C$ Design Guidelines as in the "$I^2C$ Interface Design Guidelines" in Coffee Lake PDG? | | | |

### Table 34-15. Sensors Debug Connector Checklist

| Schematic Notes | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Was one of the 2 Sensors debug connectors options implemented in this design? Refer to "Sensors Debug Hooks" in Coffee Lake PDG. | | | |

### Table 34-16. FW Debug connector Checklist

| Schematic Notes | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Was the XDP or the Primary CMC Debug Solution implemented? Refer to "Platform Debug and Test Hooks" for details in Coffee Lake PDG. | | | |

## 34.9.1.2 Detailed Schematics Checklists

### Table 34-17. General Checklist

| Schematic Notes | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Did you read, understood and followed all your sensors manufacturers design guidelines? | | | |
| Did you add Layout instructions to the schematics, for the layout designer to implement, such as keep-out zones for sensors, as mentioned in "System Debug" in Coffee Lake PDG? | | | |
| Did you check that all the sensors that are located on the same $I^2C$ bus, can they operate in the selected frequency? | | | |

**Table 34-17. General Checklist**

| Schematic Notes | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Did you correctly set the Address Selection pin on each of the sensors, to the correct level, to be accessible on its selected address? | | | |

**Table 34-18. Power Rails Checklist**

| Schematic Notes | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Intel® ISH $I^2C$ interfaces support either 1.8V or 3.3V voltage, but not mixing. Did you check that all sensors support the same voltage, or you have provided voltage level shifter? | | | |
| Did you understand and follow all the layout and design rules requirements from the sensor manufacturers? | | | |

**Table 34-19. Coffee Lake Sensors Interrupt/GPIO Checklist**

| Schematic Notes | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Are all sensors' INT pins configured correctly, as mentioned in "Electrical Characteristics" in Coffee Lake Platform PDG? | | | |
| Optional, are all Sensors INT pins on the same GPIO using the same I/O type (Totem Pole, Open Drain), polarity (Active High or Active Low) and voltage (1.8V or 3.3V)? | | | |

## 34.9.2 PCB Layout and System Design Checklists

The PCB Layout and System design checklist is documented to provide our customer's PCB Layout and System design assistance to verify that the customer will produce the best accuracy reading sensor data, by followed the IISS system design guidelines. We recommend that customer will make the best design according to the design guidelines provided and will consult with Intel Application Engineer, if this PCB Layout and System check results violates IISS design guidelines. Not following design guidelines will result in a system with **less** then best performance possible.

When using sensors package that contains 2 or more sensors, this package should conform to the design guidelines for both sensors, so both sensors checklists should be used for that package.

### 34.9.2.1 When to Use this Checklist?

Use this checklist as follows:

- After board's components are placed (according to the design guidelines), before PCB Layout starts.
- After PCB Layout was done, before closing the PCB design for gerber files.
- During and after system's chassis design, for LID magnets, hinges, speakers, microphone, fan, cooling system, hot spots location, wireless charger and digitizers, that may impact sensors accuracy.
- On any PCB Layout change.
- On any Chassis re-design.

***Note:*** For the Magnetometer, a special white paper was composed, to support Magnetometer integration. It provides a concept on how and when to use the MLOT tool/Concept. Refer to RDC#535305.

### 34.9.2.2 Sources to this PCB Layout and System Checklist:

This System and PCB Layout checklist is based on the following sources:

- Schematics checklist.
- Sensor vendors documentation.
- Accumulated knowledge and experience gathered by Intel Application Engineers.

Intel Application Engineers will be more then happy to hear customer's inputs on any aspect of sensors, to better serve customers in the next platform.

### 34.9.2.3 PCB Layout and System Checklists:

**General Mechanical Sensor Placement and Assembly Checklist**

| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| **PCB Layout** | | | |
| Did you read, understand and follow all the layout and design rules requirements from your sensor manufacturers? | | | |
| Did you read and understand the "Magnetometer Design Integration - Technical White Paper", RDC#535305? | | | |
| **Did you make sure that the sensor placement was the first step when outlining a new PCB layout and system Chassis? You need to plan accordingly, accommodating both board and system level.** | | | |
| In the Chassis level, did you place sensors at an interference-free location, in the system in **all its usage models**? | | | |
| Did you avoid placing the sensors in a long and narrow region of PCB? From our learning shows that doing this can warp and cause sensor package stress which may cause drift. | | | |
| Did you avoid placing the sensor near a connector and screw hole? Doing it will cause unsymmetrical stress coming from PCB deformation when screw is inserted will cause drift. | | | |
| Did you avoid placing the sensor in a region of PCB that can warp? Doing it might cause sensor package stress which may cause shift. | | | |
| **System Layout** | | | |
| Were all sensors placed 2 or 3 cm away from any hot devices? This helps to avoid large temperature gradient. | | | |
| Did you make sure that sensors are not placed in a region of PCB that can warp? It can cause package stress which may cause shift. | | | |

| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Did you make sure that sensors are not placed near a connector or screw hole? It can cause an unsymmetrical stress coming from PCB deformation and may cause drift. | | | |
| For a 360° system, checklist defined in the PCB Layout above should be run for all usage models, meaning Lid is in 0°, 180° and 360° etc. | | | |
| For a Detachable (2-in-1) system, checklist defined in the PCB Layout above should be run for all usage models, meaning Tablet mode, Laptop mode where Lid is at 0° (Lid closed), 90° and the maximum. | | | |

### 34.9.2.3.1 Ambient Light Sensor - ALS

| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| **System Layout** | | | |
| Is the ALS placed in the lid or display module, close to the camera (if present) and facing the user? This will allow effective control of screen brightness based on ambient light. | | | |
| Are the view angle and the lens meeting the spec of the ALS? | | | |
| Is the glass or plastic covering material consistent across the units of the same SKU/Model? | | | |
| Is the aperture wide enough to detect light without significant attenuation when the light source is at an angle to the device or from a diffused source? | | | |
| Are the glass/cover and the sensor aligned? (a misalignment would mask out some of the light and produce unexpected readings from the ALS) | | | |
| If optical film or ink coating are applied to hide the ALS optical cavity, is the filter designed to allow at least 80% of visible wavelength light to pass? | | | |

### 34.9.2.3.2 Gyroscope

| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| **PCB Layout** | | | |
| Is the Gyroscope mounted securely, so it can not move independently? | | | |
| **System Layout** | | | |
| Are the Gyroscope X, Y and Z axes orientated as described in the PDG? | | | |
| Is the Gyroscope placed in a stable position, isolated from any vibration, including transmitted vibration, air pressure change vibration, etc.? | | | |
| Is the Gyroscope place at least 30 mm away from audio speakers, fans, and haptic vibration motors? | | | |

### Accelerometer

| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| **PCB Layout** | | | |
| Is the Accelerometer mounted securely, so it can not move independently? | | | |
| **System Layout** | | | |
| Are the Accelerometer X, Y and Z axes orientated as described in the PDG? | | | |
| Is the Accelerometer placed in a stable position, isolated from any vibration, including transmitted vibration, air pressure change vibration, etc.? | | | |
| Is the Accelerometer place at least 30 mm away from audio speakers, fans, and haptic vibration motors? | | | |

### 34.9.2.3.3 Magnetometer

| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| **PCB Layout** | | | |
| **Have you read and understood the Magnetometer Design Integration - Technical White Paper, RDC#535305?** | | | |
| **The Magnetometer can easily become an issue if the design guidelines are not followed. Did you follow all of the Design Guidelines provided in the PDG?** | | | |
| **Was the magnetometer placement the first step when outlining a new PCB layout?** | | | |
| **Was the magnetometer placed at least 40 mm away from any rare earth magnets (Hard Iron such as speaker magnets, LID magnets, fan, Hall Effect magnet etc.)?** | | | |
| **Was the Magnetometer placed at least 30 mm away from any large/thick (structural) ferrous metals, the components which includes the magnet of a hard disk, digitizer, and any components with the magnetism of 100 Gauss?** | | | |
| Was the Magnetometer placed at least 10 mm away from the components which include microphone, vibration motor, magnetic switch, transformer, camera module, beeper, battery, SAW filter, antenna, power amplifier, choke, LCD rear case and any components with the magnetism of 5 Gauss? | | | |
| Was the Magnetometer placed at least 5 mm away from the components which include Memory/SIM card socket, USB connector, other connectors, screw, nut, spring, EMI shielding part, and any components with the magnet-conductive material (Iron, Cobalt, Nickel)? | | | |
| Was the Magnetometer placed at least 2 mm away from the surrounding resistor and capacitor? This, since nickel plating is usually present on solder end caps of surface mount components? | | | |



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| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| Was the Magnetometer placed at least 10 mm away from the power trace (including power plane) on all the PCB layers, components on both PCB sides or out of the board with the variable current higher than 10 mA? | | | |
| Was the Magnetometer placed at least 20 mm away from the power trace (including power plane) on all the PCB layers, components on both PCB sides or out of the board with the variable current higher than 100 mA? | | | |
| Was the Magnetometer placed at least 25 mm away from the power trace (including power plane) on all the PCB layers, components on both PCB sides or out of the board with the variable current higher than 200 mA? | | | |
| **Is there any power or ground plane under or nearby the Magnetometer? (There should be none)** | | | |
| **Make sure the Magnetometer is not covered with any material that can block the static magnetic field from the earth.** | | | |
| **System Layout** | | | |
| **Did you make sure that the LCD screen back shell, shield (for RF, BT…), mechanical part (key, screw, connector) do not contain ferromagnetism material (Fe, Co, Ni)? (correct answer is no)** | | | |
| **Did you perform the same test as in the PCB layout when the PCB is inside the final chassis, when system is powered?** | | | |
| **All the above tests must be checked in all usage models, such as a 360° system, interference for the Lid located Magnetometer should be checked with Lid in 0°, 180° and 360°.** | | | |

### 34.9.2.3.4 Pressure Sensor

| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| **System Layout** | | | |
| Is the clearance above the metal lid less then 0.1mm? | | | |
| Is the sensor located in a section where appropriate venting exists? | | | |
| Is the sensor located in an area where liquids may come into direct contact with the device? | | | |
| Is there a direct light heating the sensor? Direct light can influence the accuracy of the measurement (photo-current of silicon). | | | |
| Is the sensor located near a source of fast air pressure variation, such as fans, speaker etc.? | | | |
| Is the sensor located near a source of fast heating parts with gradients higher than 3°C/sec? | | | |
| Is the PCB area below the sensor defined as keep-out area? | | | |

#### 34.9.2.3.5 Debug Connector (10051922-1810elf)

| Checklist | ✓ | Customer Feedback | Intel Feedback |
|---|---|---|---|
| **PCB Layout** | | | |
| Was the connector implemented on the PCB? | | | |
| **System Layout** | | | |
| Was the connector placed in an area where accessing it does not require opening the chassis? | | | |

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# 35 Discrete Trusted Platform Module (TPM) Design Guidelines

Trusted Platform Module (TPM) is a Trusted Computing Group (TCG) low cost security solution to increase confidence on system security. The Trusted Platform Module (TPM) is a device that resides on the motherboard and is connected to PCH using the Low Pin Count (LPC) bus to communicate with the rest of the platform.

Today most protection against computer viruses and unauthorized intrusions consists of adding and updating software that installs outer barriers and surveillance tools. The goal of Safer Computing is to go much deeper, integrating a level of trust into the actual hardware and pre-operating system environments. Applications intended for e-business are based on trust in the communication partner and the reliability of the connection.

The objective of the TPM is to establish a baseline of platform integrity and enhance system security. TPMs are available from several integrated circuit vendors in the form of a silicon component and accompanying software. When integrated into the PC, a Trusted Platform Module provides protected storage of platform data allowing for platform-level authentication toward the goal of making data files, transactions and communication more trustworthy.

For more information on trusted platform modules and Safer Computing, refer to the trusted computing group web site: http://www.trustedcomputinggroup.org.

**Table 35-1. TPM Reference Documents**

| Title | Location |
|---|---|
| TCG Architecture Overview, Version 1.4 | http://www.trustedcomputinggroup.org |
| TCG Design, Implementation, and Usage Principles (Best Practices) | http://www.trustedcomputinggroup.org |

**Table 35-2. TPM Compliance Documents**

| Title | Location |
|---|---|
| TPM Main Specification | http://www.trustedcomputinggroup.org |

# 35.1 Signal Description

## 35.1.1 Signal Groups

### Table 35-3. Trusted Platform Module (TPM) Signals

| Section | Group | Signal Name | Description |
|---|---|---|---|
| Refer figure below | Address data | LAD[3:0] | Address/Data lines |
| | Clock | LCLK | Clock |
| | Reset | LRESET | Reset |
| | Control | LFRAME# | Cycle termination |
| | | SERIRQ | Serialized IRQ |
| | | LPCPD# | Suspend status and LPC power down |

### Figure 35-1. Trusted Platform Module (TPM) / PCH Block Diagram

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# 36 Platform Reset Considerations

Platform reset signals is a group of reset signal that control power on sequence, power management and provide proper reset to all components on the platform. This chapter provide detailed guideline on how to generate and use platform reset signal to ensure functionality of the platform.

## 36.1 Signal Description

### 36.1.1 Signal Groups

Signals listed in the following table are identified as platform reset signals from the PCH.

**Table 36-1. Platform Reset Signals**

| Group | Signal Name | Description |
|---|---|---|
| Reset | RSMRST# | Resume Well Reset: This signal resets the Primary Well |
| | SYS_RESET# | System Reset |
| | PLTRST# | Platform Reset |
| | DRAM_RESET# | DRAM Reset |
| Power Management | ACPRESENT | ACPRESENT |
| | BATLOW# | Battery Low |
| | PCH_PWROK | PCH Power OK |
| | DSW_PWROK | Deep Sleep Well Power OK |
| | SYS_PWROK | System Power OK |
| | SLP_A# | ASW Sleep Control |
| | SLP_S0# | S0 Sleep Control |
| | SLP_S3# | S3 Sleep Control |
| | SLP_S4# | S4 Sleep Control |
| | SLP_S5# | S5 Sleep Control |
| | SLP_LAN# | LAN Sub-System Sleep Control |
| | SLP_WLAN# | WLAN Sub-System Sleep Control |
| | SLP_SUS# | Deep S3/S4/S5 Indication. Primary Well power control on Deep Sx enabled platform. |
| | PWRBTN# | Power Button |
| | SUSACK# | Deep S3/S4/S5 entry Acknowledge |
| | SUSPWRDNACK/ SUSWARN# | Deep S3/S4/S5 Power Down Warning to EC. |
| | SUSCLK | This clock is an output of the RTC generator circuit for use by other platform devices for clock refresh. |

## 36.2 Additional Guidelines

### 36.2.1 SYS_RESET# Usage Model

Designers can connect the System Reset signal (SYS_RESET#) on PCH directly to the reset button on the system, provided that there is a weak 8.2 KΩ -10 KΩ pull-up resistor to Primary 3.3 V (VCCPRIM_3p3) or pull-up to any 3.3V rails that is controlled by SLP_S3# or SLP_S4# or SLP_S5# signals. PCH will de-bounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system; thus helping prevent a slave device on the SMBus from "hanging" due to the PCH being reset in the middle of a cycle.

When SYS_RESET# is connected to a XDP header, it will require a stronger pull up to work with ITP hardware. Use 100 Ω - 3 KΩ pull-up whenever it is connected to a XDP header. Recommend to use 3 KΩ to minimize leakage.

### 36.2.2 SLP_A# Usage Model

SLP_A# is a PCH signal that may be used to control the overall power to Intel® Management Engine (Intel® ME) components during ACPI S3 through S5 states when Intel ME is enabled. When asserted, it indicates platform level devices on the Active Sleep Well (ASW) maybe powered off.

***Note:*** The PCH no longer have a dedicated ASW rail. Refer to Chapter 33, "Intel® Management Engine (Intel® ME)" for details regarding SLP_A# connection.

### 36.2.3 SLP_S0# Usage Model

SLP_S0# is a PCH signal which indicates the system is in the S0ix state. It is used primarily to control platform VR so that it will enter a more power efficient mode during S0ix. It may also be used to power off all non-critical components during the S0ix state. This signal should be connected to an VR controller to enter low power mode.

### 36.2.4 SLP_S3# Usage Model

SLP_S3# is a PCH signal which indicates the system is in the ACPI S3 State. It is used to power off all non-critical components during the S3 state. This pin may be connected to an SIO to indicate the S3 state. Refer to PCH EDS for additional information.

### 36.2.5 SLP_S4# Usage Model

SLP_S4# is a PCH signal which indicates the system is in the ACPI S4 State. It is used to power off the DRAM and other non-critical components during the S4 state. This pin can be connected to an SIO to indicate the S4 state. Refer to PCH EDS for additional information.

### 36.2.6 SLP_S5# Usage Model

SLP_S5# is a PCH signal which indicates the system is in the ACPI S5 State. It maybe used to power off non-critical components during the S5 state. This pin can be connected to an SIO to indicate the S5 state. If S5 state indication is not required this pin may be left as no connect or configured as GPIO. Refer to PCH EDS for additional information.

### 36.2.7 SLP_LAN# Usage Model

SLP_LAN# is a PCH signal which indicates when the Intel LAN PHY device must be powered. This pin should be connected to a power switch to control the 3.3V and any other externally supplied voltages to the external Intel LAN PHY. SLP_LAN# is always de-asserted when SLP_S3# and/or SLP_A# is de-asserted. SLP_LAN# can also be configured by Intel ME FW or host BIOS to indicate when the Intel LAN PHY should be powered in S3-S5 to support WOL (Host or Intel ME).

### 36.2.8 SLP_WLAN# Usage Model

SLP_WLAN# is a PCH signal which indicates when the Wireless LAN device must be powered. This pin should be connected to a power switch to control the 3.3V and any other externally supplied voltages to the external Wireless LAN. SLP_WLAN# is always de-asserted when SLP_S3# and/or SLP_A# is de-asserted. SLP_LAN# can also be configured by Intel ME FW or host BIOS to indicate when the Wireless LAN should be powered in S3-S5 to support Wake on Wireless LAN (Host or Intel ME).

### 36.2.9 SLP_SUS# Usage Model

SLP_SUS# is a PCH signal which indicates that the system is in Deep Sx state. The Deep Sx state is a lower power, limited wake capability supported state where the Primary well is powered off and only the DSW well in the PCH remains powered. This pin can be used to power off Primary power during the Deep Sx state. If Deep Sx is not implemented on the platform, this signal may be left as no connect. Refer to PCH EDS for additional information.

### 36.2.10 SUSWARN# / SUSPWRDNACK Usage Model

SUSWARN# is a PCH signal which indicates the PCH is planning to enter into Deep Sx state and power off the Primary well. The Embedded Controller (EC) monitors this signal and appropriately controls power to the Primary rails. This signal is only used on platforms that support the Deep Sx state.

This signal is multiplexed with SUSPWRDNACK, since SUSPWRDNACK is not needed in Deep Sx supported platforms.

### 36.2.11 SUSACK# Usage Model

SUSACK# is an input signal to the PCH from the Embedded Controller (EC), acknowledging that the EC has completed preparations as signaled by SUSWARN#. This signal is only used on platforms that support the Deep Sx rate.

***Note:*** SUSACK# and SUSWARN# can be tied together if EC does not want to be involved in the handshake mechanism for the Deep Sx state entry and exit.

### 36.2.12 PWRBTN# Usage Model

The Power Button signal (PWRBTN#) on PCH can be connected directly to the power button on the system. When system power button is pressed, PWRBTN# should be pulled low. This signal is internally pulled-up in PCH to VCCDSW_3p3 through a weak pull-up resistor (15 kΩ to 40 kΩ). PCH has 16 ms of internal de-bounce logic on this pin, external debouncing circuit is not required.

### 36.2.13 PLTRST# Usage Model

The Platform Reset signal (PLTRST#) is a signal on the PCH that should be connected to devices on the motherboard which require a reset. For designs with large fan out on PLTRST#, proper validation should be carried out to ensure the output driving capability of PLTRST# is not exceeded. A buffer will be needed if PLTRST# driving capability is exceeded.

***Note:*** Some devices may utilize GPIOs to control the resets during RTD3.

### 36.2.14 SUSCLK Usage Model

On CFL, the SUSCLK signal has moved to the DSW well and is generated from the RTC. For platforms supporting Deep Sx and utilizing this signal, proper isolation must be taken to ensure SUSCLK is not driven into a device that might be powered off in Deep Sx state.

### 36.2.15 RSMRST# Generation

RSMRST# is an input signal to the PCH generated by EC. This signal is used for resetting the Primary power plane logic. It must be asserted for at least 10ms after Primary power wells are stable.

### 36.2.16 DSW_PWROK Generation

DSW_PWROK is an input signal to the PCH generated by EC to indicate that DSW rail, is stable on the platform. For platforms not supporting Deep Sx, connect directly to RSMRST#. The DSW rails must be stable for at least 10 ms before DSW_PWROK is asserted to PCH.

### 36.2.17 PCH_PWROK Generation

PCH_PWROK is an input signal to the PCH generated by EC based on VR power good signal. Assertion of this signal indicates that all the PCH Primary rails are up and all the main CPU rails (excluding GT and core) are up.

### 36.2.18 SYS_PWROK Generation

This is an input signal to the PCH and provides a platform/EC a mechanism to stall the PCH de-assertion of PLTRST# to the platform. While PCH_PWROK always indicates that the Primary well of the PCH and CPU rails (excluding core and GT) are stable, SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset. The particular component(s) associated with SYS_PWROK can vary across platform. Depending on the platform, the PCH may expect (and wait) for SYS_PWROK at different stages of the boot flow before continuing.

***Note:*** PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. PCH does not monitor SYS_PWROK until after PCH_PWROK is asserted. Refer to the Chapter 45, "Platform Power Sequencing Specification" for details.

## 36.2.19 Legacy Requirements

- Legacy APWROK implementation has been replaced internally by a timer. PCH will assume any device whose power is controlled by SLP_A#, will ramp within 16ms of SLP_A# de-assertion.
- Legacy timing requirements for DSW_PWROK and RSMRST# based on DSW or Suspend well falling have been removed. Refer to Chapter 45, "Platform Power Sequencing Specification", Rail to Rail Sequencing Requirements on new guidelines for CFL.

## 36.2.20 Additional Power Sequencing Considerations

It is possible that on rare occasions, wake events can cause the system to immediately wake after entering in S3 or S4 or other power states. Additionally, similar wake events can occur and cause a system to wake immediately out of Intel ME Mx states (such as Moff).

In such circumstances it is possible that the PCH will generate short duration pulse widths on SLP_S3#, SLP_S4#, SLP_A#, or SLP_SUS#, depending on which system state was being entered. Care should be taken during the platform design to evaluate and account for such events in terms of VR design, power good circuitry design, and overall platform power sequencing in order to ensure timing specifications related to power sequencing are not violated.

To help minimize the impact of such events to platform design and complexity, the PCH has the capability to "stretch" the minimum assertion time on SLP_S3#, SLP_S4#, SLP_A#, and SLP_SUS# signals. Options provided by PCH are shown below.

**Table 36-2. Minimum Assertion Time Stretching Options**

| Signal Name | Units | Minimum Assertion Time Stretching Options |
|---|---|---|
| SLP_S3# | seconds | 60u, 1m, 50m, 2 |
| SLP_S4# | seconds | 1, 2, 3, 4 |
| SLP_A# | seconds | 0, 98m, 2, 4 |
| SLP_SUS# | seconds | 0, 500m, 1, 4 |

By default, the stretching capabilities are not enabled by hardware defaults and require the BIOS to set up the features.

A typical configuration recommended by Intel is SLP_S3#= 50 ms, SLP_S4#=1 s, SLP_A#=2 s, SLP_SUS#=4 s. Differences in customer platforms may require or allow for adjustments to these recommendations.

Refer BIOS writer's guide for further details and requirements on programming of these features.

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# 37 Interrupt Interface Design Guidelines

The interrupt capabilities of the PCH platform maintain support for up to eight PCI interrupt pins and PCI 2.3 Message-Based Interrupts. In addition, the PCH supports system bus interrupt delivery.

## 37.1 Signal Description

**Table 37-1. IOAPIC Interrupt Inputs 16 Through 23 Usage**

| Number | IOAPIC INTIN PIN | Function in Intel® PCH using the PCI IRQ in IOAPIC |
|---|---|---|
| 1 | IOAPIC INTIN PIN 16 (PIRQA) | USB UHCI Controller 1; USB UHCI Controller 4 |
| 2 | IOAPIC INTIN PIN 17 (PIRQB) | Option for SMBus |
| 3 | IOAPIC INTIN PIN 18 (PIRQC) | USB UHCI Controller 3; SATA Mode |
| 4 | IOAPIC INTIN PIN 19 (PIRQD) | USB UHCI Controller 2 |
| 5 | IOAPIC INTIN PIN 20 (PIRQE) | Internal LAN; option for SCI, TCO, HPET 0,1,2 |
| 6 | IOAPIC INTIN PIN 21 (PIRQF) | Option for SCI, TCO, HPET 0,1,2 |
| 7 | IOAPIC INTIN PIN 22 (PIRQG) | Option for SCI, TCO, HPET 0,1,2 |
| 8 | IOAPIC INTIN PIN 23 (PIRQH) | USB EHCI Controller; option for SCI, TCO, HPET 0,1,2 |

## 37.2 Additional Guidelines

### 37.2.1 PIRQ Routing Example

The following figure shows how PCH uses the PCI IRQ when the I/O APIC is active.

Due to different system configurations, IRQ line routing to the PCI slots (“swizzling”) should be made to minimize the sharing of interrupts between both internal Intel PCH functions and PCI functions. The following shows an example of IRQ line routing to the PCI slots.

**Figure 37-1. Example PIRQ Routing**

***Note:*** Figure 37-1 is an example. It is up to each board designer to route these signals in a way that will prove the most efficient for a particular system. A PCI slot can be routed to share interrupts with any of the PCH internal device/functions (but at a higher latency cost).

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# 38 Critical Low Speed Signals Design Guidelines

Critical Low Speed Signals are identified as critical input signals from the PCH that are low frequency but have huge impact to system functionality or stability. Glitches on these signals may cause the system to behave in and unpredicted manner or cause an unpredicted system shutdown or reset. Although these are low speed signals in nature, glitches may be induced or coupled from nearby high speed signals. Therefore, it is important to keep these signals clean from any potential sources of glitches on the platform.

## 38.1 Signal Description

### 38.1.1 Signals Group

Signals listed in Table 38-1 are identified as critical input signals from the PCH that need to be guaranteed glitch free all the time.

**Table 38-1. Signals Group (Sheet 1 of 2)**

| Group | Signal Name | Description |
|---|---|---|
| System Management | INTRUDER# | Intruder Detect: This signal can be set to disable system if box detected open. |
| RTC | SRTCRST# | Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed. |
| RTC | RTCRST# | RTC Reset: When asserted, this signal resets register bits in the RTC well. |
| Power Management | RSMRST# | Resume Well Reset: This signal is used for resetting the resume power plane logic. This signal must be asserted for at least 10 ms after the suspend power wells are valid. When deasserted, this signal is an indication that the suspend power wells are stable. |
| Power Management | SYS_RESET# | System Reset: This pin forces an internal reset after being debounced. |
| Power Management | PWROK | Power OK: When asserted, PWROK is an indication to the PCH that all of its core power rails have been stable for 10 ms. PWROK can be driven asynchronously. When PWROK is negated, the PCH asserts PLTRST#. |
| Power Management | APWROK | Active Sleep Well Power OK: When asserted, this signal indicates that power to the Intel ME subsystem and integrated LAN are stable. |
| Power Management | DPWROK | Deep Sleep Well Power OK: When asserted, this signal indicates that power to the DSW are stable. |
| Power Management | SYS_PWROK | System Power OK: This generic power good input to the PCH is driven and used in a platform-specific manner. SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset. |
| Power Management | PWRBTN# | Power Button: The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input. |

**Table 38-1. Signals Group (Sheet 2 of 2)**

| Group | Signal Name | Description |
|---|---|---|
| Power Management | THRMTRIP# | Thermal Trip: When low, this signal indicates that a thermal trip from the processor occurred, and the PCH will immediately transition to a S5 state. PCH will drive SLP_S3#, SLP_S4# and SLP_S5# low within 1us after sampling THRMTRIP# active. |
| Power Management | WAKE# | PCI Express* Wake Event: Sideband wake signal on PCI Express asserted by components requesting wake up. |
| Processor Interface | RCIN# | Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks. |

## 38.2 Additional Guidelines

All critical signals must stay away from potential glitch or noise sources on the platform. It is recommended to keep all critical signal traces a minimum of 15 mils away from any clock or high speed differential signals with > 4 V/ns edge rate to avoid glitches from crosstalk.

**Table 38-2. Critical Signals Routing Summary**

| Parameter | Stack-up (MS/SL/DSL) | Units | Routing Recommendation |
|---|---|---|---|
| Spacing | MS/SL/DSL | mils | 15 mils |

Experiment data shows that certain signals have shown high sensitivity to specific frequencies. Routing those signals near to the frequency source will increase the glitches due crosstalk. The relationship of each signal with the frequency it is sensitive to is listed in the following table. The designer should try to avoid routing a signal next to the sensitive frequency and the harmonics of its sensitive frequency. If this cannot be avoided, it should be kept a minimal of 15 mils from the respective signal trace.

**Table 38-3. Frequency Sensitivity**

| Signal Name | Frequency to Avoid |
|---|---|
| INTRUDER# | 32 KHz |
| THRMTRIP# | 125 MHz |
| RCIN# | 33 MHz |
| APWROK | 12.5 MHz |
| PWRBTN# | 32.768 KHz |
| SYS_RESET# | 1 KHz |
| SYS_PWROK | 12.5 MHz |
| WAKE# | 12.5 MHz |

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# 39 M.2 Module

## 39.1 Overview

M.2 is a versatile form factor that meets the power and thermal needs of add-in cards for ultra-thin profile products like Ultra books™ and Tablets. Further, M.2 also enables the co-existence of multiple I/O technologies on the same module, which is a big benefit for customers that other embedded (small) form factors, like mini PCIe* or mini SATA, are not able to provide.

### 39.1.1 Reference Specifications

**Table 39-1. References**

| Title | Location |
|---|---|
| PCI Express* M.2 Specification rev 1.0 | *http://www.pcisig.com* |
| M.2 Specification in Serial ATA Specification, Revision 3.2 | *http://www.sata-io.org* |

## 39.2 Supported M.2 Features

### 39.2.1 Connector Keys

Connector keys serve two primary purposes: safety and proper matting guidance.

- **Safety:** A 1:1 definition of the pinout between motherboard and modules to prevent the wrongful insertion of an incompatible module into a wrong slot on the motherboard, including the potential module inversion (i.e. mirroring).
- **Guidance:** Ensures that the pins between the motherboard connector and the module's gold fingers are properly aligned as the module is inserted or extracted. This is especially important when plugging a 1630 Wireless module into the 2230 Socket 1 connector on the motherboard.

### 39.2.2 Module Stand-off

The location of the stand-off on the motherboard depends on the length of the M.2 modules that the system plans to support. Since the stand-off sub-assembly is meant to be removable (i.e. not soldered down, riveted, etc) it is possible to have multiple holes in the motherboard to accommodate the various modules that may plug into the sockets. CFL supports the following module lengths: 30 mm (Socket 1 applications), 42 mm (Socket 2 applications) and 60 mm (Socket 2 or 3 SSD).

The module stand-off must be connected to ground on the motherboard and module.

The module stand-off serves two primary purposes: Retention and thermal dissipation.

- **Retention:** The retention screw ensures the module is properly secured in place.
- **Thermal dissipation:** With a minimum conductivity requirement of 50 W/m*K (Watts per meter per Kelvin), the retention screw/module stand-off sub-assembly acts as a heat transfer conduit away from the M.2 module. This is particularly important for tight applications where airflow is extremely limited.

## 39.2.3 Schematics Connector Symbol - Design Considerations

It is recommended, as a good schematics design practice, for the schematics symbol to match the physical connector shape and attributes. The schematics should clearly convey the design intention and should avoid ambiguous symbols. The M.2 specification includes a pinout for the platform and a matching pinout for M.2 modules. Motherboard designers shall use the platform pinout and should document this in the schematics, as a good design practice. The following are examples of bad M.2 connector symbol choices and a well-done M.2 connector schematics symbol.

Refer M.2 specification for pinouts for different interfaces.

**Figure 39-1. Poorly-Documented M.2 Connector Schematics Symbols**

## Figure 39-2. Well-Documented M.2 Connector Schematics Symbol

# 39.3 Design Guidelines for M.2 Interfaces

## 39.3.1 PCI Express* Interface

**Figure 39-3. PCI Express* Interface - Topology**

**Table 39-2. TX and RX - PCIe Gen1 Layout Guidelines**

| Segment | T line Type | Reference | Via count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | 4 | 15.2 | 64 (min) 330 (max) | 598.42 | 2519.68 (min) 12992.13 (max) |
| M1+M2 | MS/SL/DSL | VSS | | NA | | NA | |
| M3/M5 | MS | VSS | | 8 | | 314.96 | |
| M4+M5 | NA | VSS | 1 | 38 | 38 | 1496.06 | 1496.06 |

**Table 39-3. TX and RX - PCIe Gen2 Layout Guidelines**

| Segment | T line Type | Reference | Via count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | 4 | 15.2 | 64 (min) 229 (max) | 598.42 | 2519.68 (min) 9015.75 (max) |
| M1+M2 | MS/SL/DSL | VSS | | NA | | NA | |
| M3/M5 | MS | VSS | | 8 | | 314.96 | |
| M4+M5 | NA | VSS | 1 | 38 | 38 | 1496.06 | 1496.06 |

**Table 39-4. TX and RX - PCIe Gen3 Layout Guidelines (Sheet 1 of 2)**

| Segment | T line Type | Reference | Via Count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | 3 (for TX) 2 (for RX) | 15.2 | 64 (min) 203 (max) | 598.42 | 2519.68 (min) 7992.13 (max) |
| M1+M2 | MS/SL/DSL | VSS | | NA | | NA | |
| M3/M5 | MS | VSS | | 8 | | 314.96 | |

**Table 39-4. TX and RX - PCIe Gen3 Layout Guidelines (Sheet 2 of 2)**

| Segment | T line Type | Reference | Via Count | Max Length, mm | | Max Length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| M4+M5 | NA | VSS | 1 | 38 | 38 | 1496.06 | 1496.06 |

***Notes:***

- AC Capacitor value
  - Gen1 and Gen2: 75nF --> 265 nF and Gen 2 nominal is 100nF
  - Gen3: 176 --> 265 nF and nominal is 220nF
- Number of Via allowed
  - TX: Gen1 and Gen2 -->4 and Gen3 -->3 (not counting via under package)
  - RX: Gen1 and Gen2 -->4 and Gen3 -->2 (not counting via under package)
  - Express card/Add-in card vias allowed: 1 (for Tx / Rx lanes)
- Breakout length and spacing: An initial breakout segment of 4mm (157.48 mils) in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm (4 -6 mils) is allowed. The total breakout length is still 15.2mm (598.42 mils)
- Reference plane: Continuous Ground Only and Power plane referencing is allowed. Refer to Chapter 3.5.2, Power Referencing tab for guidelines and limitations
- Length Matching between P and N within a differential pair
  - Within same layer mismatch:± 0.254mm (± 10mils)
  - Total length mismatch: ± 0.127mm (±5mils)
- Length matching between Tx pairs of multiple lanes - If PCIe signals are routed to the same connector (eg a x4 connector), the total delta length between all the TX signals should be within 2". Assuming @ a X4 connector, where TXp/n_0 is shortest length @ 3", while TXp/n_3 is the longest trace, then the longest routing length TXp/n_3 allowed will be 3"+ delta 2" = 5"
- Length matching between Rx pairs of multiple lanes - If PCIe signals are routed to the same connector (eg a x4 connector), the total delta length between all the RX signals should be within 2". Assuming @ a X4 connector, where RXp/n_0 is shortest length @ 3", while RXp/n_3 is the longest trace, then the longest routing length RXp/n_3 allowed will be 3"+ delta 2" = 5"
- Length matching between TX and Rx pairs - If PCIe signals are routed to the same connector (eg a x4 connector), the TX and RX pairs should be length match to be within 2" (see above for length matching TX and RX)
- Include package length in length matching- Not required

## 39.3.2 SATA Interface

**Figure 39-4. SATA Interface - Topology**

**Table 39-5. SATA M.2 Layout Guidelines**

| Segment | T line Type | Reference | Via count | Max length, mm | | Max length, mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | 3/2 * | 15.2 | 50.8(min) 178/203.2* (max) | 598.42 | 2000(min) 7007.87/ 8000* (max) |
| M1 | MS/SL/DSL | VSS | | NA | | NA | |
| M2 | MS | VSS | | NA | | NA | |
| M3 | MS | VSS | | 10 | | 393.7 | |
| M4 | MS | VSS | | M2+M3 | | M2+M3 | |

***Notes:***

- AC Capacitor value: 10nF
- Number of Via allowed
  - 3 vias for 7007.87 mils max length and 2 vias for 8000 mils max length
  - Assumes 1 via in the device M.2 card
- Breakout length and spacing: An initial breakout segment of 4mm (157.48 mils) in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm (4 -6 mils) is allowed. The total breakout length is still 15.2mm (598.42 mils)
- Reference plane: Continuous ground only and Power plane referencing is allowed. Refer to Chapter 3.5.2, Power Referencing tab for guidelines and limitations
- Length Matching between P and N within a differential pair
  - Within same layer mismatch:± 0.254mm (± 10mils)
  - Total length mismatch: ± 0.127mm (±15mils)
- Length matching between TX and Rx pairs - Not required
- Include package length in length matching- Not required

#### 39.3.2.1 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

***Note:*** When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

**Table 39-6. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values**

| Condition | PCI Express* Gen 2 Only | PCI Express* Gen 3 Only | SATA Only | PCI Express* Gen 2/ SATA | PCI Express* Gen 3/ SATA |
|---|---|---|---|---|---|
| Processor Tx | 100 nF | 220 nF | 10 nF | 100 nF | 220 nF |
| Processor Rx | None | None | 10 nF[2] | None | None[3] |

***Notes:***
1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

### 39.3.3 USB 3.0 Interface (USB3.1 Gen1)

Refer guidelines from **Section 18.1.4.2, "USB 3.1 Gen1 M.2 Topology"**

### 39.3.4 USB 2.0 Interface

Refer guidelines from **Section 19.7.3, "USB 2.0 with M.2 Topology"**

### 39.3.5 SMBus and I$^2$C Topology Guidelines

SMBus: Refer guidelines from **Chapter 27, "SMBus 2.0/SMLink Interface Design Guidelines"**

I2C: Refer guidelines from **Chapter 23, "I$^2$C* Interface Design Guidelines,"**

### 39.3.6 UART and SPI Topology Guidelines

UART: Refer guidelines from Chapter 24, "Universal Asynchronous Receiver Transmitter (UART) Interface Design Guidelines"

SPI: Refer guidelines from Chapter 25, "Generic Serial Peripheral Interface (GSPI)"

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# 40 Front Facing HD/FHD Webcam Design Guidelines

Intel requires 720p cameras in the Ultrabook™ for High Definition Video Conferencing. 720p camera is baseline, but 1080p is recommended by Intel. The guidelines in this chapter are design considerations for designing a Front Facing High Definition (HD) or Full High Definition (FHD) Webcam module. Vendors should reference the *(Platform Product Requirements Document)* for designing the webcam interface in accordance with Intel recommendations.

## 40.1 Design Considerations

- Customers are recommended to use "Unified" mechanical dimension to enable HD/FHD webcam modules. Use 50 mm (or 100 mm) DMiC spacing for speech/voice program per architecture recommendation.

**Figure 40-1. Unified Module Component Placement/Dimension**

| Module Dimension and Mounting | | |
|---|---|---|
| Length (L) | ~ 70.0mm | |
| Width (W) | ~ 7.5mm | |
| Z-Height (H) | <= 3.0mm | Required |
| **Mounting** | | |
| Alignment Hole (p) | = 2.65mm | Required |
| Screw hole (s) | = 51.0mm | Required |

| Component Placement | | | |
|---|---|---|---|
| LED (e) | = | 14.0mm | Required |
| Camera (c) | = | 22.0mm | Required |
| ALS (a) | = | 30.0mm | Required |
| DMIC (m) | = | 47.0mm | Required |
| MIC Spacing (d) | = | 50.0mm | Required |

***Note:*** OEM/ODM should contact module IHV for the exact dimension to design the system ID.

**Table 40-1. HD/FHD Webcam Module Connector/Pinout (Sheet 1 of 2)**

| Normal Cam Pin Description | | | |
|---|---|---|---|
| **Pin Number** | **Name** | **Pin Type** | **Function Description** |
| 1 | DMIC/ALS VCC | Power | Power supply DC +3.3V for DMiC, ALS |
| 2 | USB VCC | Power | Power supply DC +3.3V for Camera |

**Table 40-1. HD/FHD Webcam Module Connector/Pinout (Sheet 2 of 2)**

| Normal Cam Pin Description | | | |
|---|---|---|---|
| **Pin Number** | **Name** | **Pin Type** | **Function Description** |
| 3 | D- | Data | USB data transmission |
| 4 | D+ | Data | USB data transmission |
| 5 | DGND | Ground | Common Ground |
| 6 | MDATA | Output | Microphone Data |
| 7 | MCLK | Input | Microphone Clock |
| 8 | DGND | Ground | Digital Ground |
| 9 | ALS DATA | Output | Ambient Light Sensor Data |
| 10 | ALS CLK | Input | Ambient Light Sensor Clock |
| 11 | ALS Interrupt | Input | Ambient Light Sensor Interrupt |
| 12 | SH GND | Ground | Shielding Ground |

Power rail option: Camera has two power sources, one for Camera and second for DMiC and ALS.

- Separated Power rail:
  - Reference design comes with separated power rail option. Camera can be turned on while DMiC and ALS can be turned off for power saving.
- Combined Power rail:
  - Having two separate power rails is not a requirement. OEM/ODM can have a single power rail if they want.
  - If OEMs/ODMs want to merge power for Camera and DMiC and ALS then add a 0-Ω resistor on R17 (Refer Figure 40-2).

## Figure 40-2. USB Connector

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# 41 LAN Design Considerations and Guidelines

The PCH incorporates an integrated 10/100/1000 Mb/s Media Access Controller (MAC) that can be used with an external Intel® Ethernet Connection I219 Physical Layer Transceiver (PHY). Its bus master capabilities enables the component to process high-level commands and perform multiple operations. This can decrease processor use by off loading communication tasks from the processor.

For specific design and implementation information about the I219 Physical Layer Transceiver (PHY), refer the following reference documents.

**Table 41-1. Reference Documents**

| Document | Document Number |
|---|---|
| Intel® Ethernet Connection I219 (Jacksonville) - Reference Schematic - Rev. 1.0 | 544767 |
| Intel® Ethernet Connection I219 (Jacksonville) - Cadence Files | NA |
| Intel® Ethernet Connection I219 (Jacksonville) - Schematic and Layout Checklist - Rev. 1.2 | 544506 |
| Intel® Ethernet Connection I219 (Jacksonville) - Datasheet - Rev. 2.02 | 544486 |
| Intel® Network Connections LAN Software Production Version 20.2 v2 | 560726 |
| Intel® Ethernet Connection I219 [Jacksonville] - Message of the Week (MOW) - 11-Feb-2015 | 546335 |
| Intel® Ethernet Connection I218/I219 [Clarkville/Jacksonville] - Specification Update - Public - Rev. 1.1 | 558625 |

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# 42 Wireless Connectivity Integration (CNVi) Design Considerations

## 42.1 Connectivity Integration (CNVi)

| | |
|---|---|
| CFL-S Rev1.8 | • In section "**Jefferson Peak Crystal Input to CNL Topology Routing Guidelines**"<br>• Updated the block diagram "**Jefferson Peak Crystal Input to CNL Topology Diagram**" |
| CFL-H Rev1.6 | • In section "**Jefferson Peak Crystal Input to CNL Topology Routing Guidelines**"<br>• Updated the block diagram "**Jefferson Peak Crystal Input to CNL Topology Diagram**" |
| CFL-H Rev 1.8 | • Updated the figure "**CNVi Power up Sequence**" |
| CFL-S Rev 1.8 | • Updated the figure "**CNVi Power up Sequence**" |
| CFL-H Rev 1.9 | • Updated the table "**CNVio M.2 Topology Values"** |
| CFL-S Rev 1.9 | • Updated the table "**CNVio M.2 Topology Values"** |
| CFL-S/H date 27/7/18 | • Updated table 42-9<br>• Updated the section "**CLKREQ# Timing**" |
| CFL-S/H date 3/7/18 | • Updated table "**General guidelines**" for BRI/RGI routing guideline section |
| CFL-S/H date 3/27/19 | • Updated the table "**PERST# timing**" |

Connectivity integration (CNVi) is a general term referring to a family of connectivity solutions which are based on the Pulsar family for CFL. The common component of all these solutions is the Pulsar IP, which is a hard macro embedded in various Intel SoC chips.

The CNVi solution also contains an external RF companion module (CRF) and RF antennas. This module can be implemented in the following variations:

1. M.2 (2230)
2. Soldered-down M.2 (1216) or
3. Chip-on board (COB).

## 42.2 Platform High-level Description

Figure below shows the Platform-level view of CNVi, including all related system components.

**Figure 42-1. CNVi Platform Block Diagram**

The CNVi platform system includes the following blocks:

## 42.2.1 System-on-Chip (SoC)

Pulsar IP is integrated with PCH (CNP-LP and CNP-H) part of Multi-chip module (MCM).

## 42.2.2 Platform Crystal

The platform crystal provides reference clock to the SoC. The frequency of this clock varies according to the platform. Possible frequencies for CFL- 24MHz.

## 42.2.3 WWAN Co-existence

This is a Cellular modem module, typically an M.2 card which provides cellular connectivity to the platform. The WWAN modem interacts with the CNVi through two different interfaces:

- UART- a bus used to exchange Real-Time Co-Existence data between Wi-Fi*/ Bluetooth and the cellular modem.
- Aiding- signals driven by the modem, which are used to assist in improving performance.

### 42.2.4 Platform VRs

Provides a single 3.3V rail to the external connectivity circuitry.

### 42.2.5 CNVi Related Straps

These are pin-straps used on SoC pins. These straps control SoC initialization functions related to CNVi implementation.

### 42.2.6 Connectivity

The connectivity block can have different mechanical implementations depending on the form factor and functionality. Connectivity modules are characterized by the following properties:

- Integration level: Intel RF companion chip or Discrete (Intel or TPV)
- Form factor: M.2 2230 or 1216 or Chip-on-board (COB)
- Wi-Fi* streams: 1x1 or 2x2 802.11ac

### 42.2.7 Connectivity Antennas

2x2 Configuration include:

- Wi-Fi* Main Antenna
- Shared Wi-Fi*/Bluetooth Antenna (combining Wi-Fi* chain-1 and Bluetooth signals together)

1x1 Configuration include:

- Wi-Fi*/Bluetooth Antenna with Diversity option.

## 42.3 CNVi Form Factors

The modules described in this section are:

- RF Companion M.2 (2230)
- RF Companion Solder-down M.2 (1216)
- RF Companion COB

### 42.3.1 RF Companion M.2 (2230)

The RF Companion 2230 module has the same mechanical outline as the standard M.2 connectivity Type 2230-S3-E card.

The standard M.2 Key E connector pin-out is modified to accommodate the proprietary RF companion signals, hence called “Hybrid Key-E”. This unique design allows inserting the RF Companion module into a standard M.2 Key E socket.

This feature is only possible when the Motherboard design follows specific guidelines described here.

### 42.3.1.1 Module Pinout

The RF Companion 2230 module Pinout is shown in Table below.

**Table 42-1. RF Companion Module 2230 Pin List (Sheet 1 of 3)**

| M.2 Pin# | Hybrid Key E M.2 2230 Pin Name | CNVi RF Companion Pin Description | Standard WLAN Solution Pin Description |
|---|---|---|---|
| 1 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 2 | +V3P3A | Connect all +V3P3A pins to Platform 3.3V supply. | Connect all +V3P3A pins to Platform 3.3V supply. |
| 3 | USB D+ | Unused | USB |
| 4 | +V3P3A | Connect all +V3P3A pins to Platform 3.3V supply. | Connect all +V3P3A pins to Platform 3.3V supply. |
| 5 | USB D- | Unused | USB |
| 6 | LED1# | Open-drain output capable of driving a platform LED. Optional to connect to Platform LED 1 (if needed). | Open-drain output capable of driving a platform LED. Optional to connect to Platform LED 1 (if needed). |
| 7 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 8 | PCM_CLK | Unused | Optional Bluetooth I2S bus clock |
| 9 | WGR_D1N | CNVio lane 1 to Pulsar (Negative). Connect to SoC CNVio input D1- pin | Unused |
| 10 | PCM_SYNC/LCP_RSTN | RF companion reset signal, active low. Connect to SoC output. | Optional Bluetooth I2S bus sync |
| 11 | WGR_D1P | CNVio lane 1 to Pulsar (Positive) Connect to SoC CNVio input D1+ pin | Unused |
| 12 | PCM_IN | Unused | Optional Bluetooth I2S bus din |
| 13 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 14 | PCM_OUT/CLKREQ0 | Clock request signal. Used by the SoC to request the RF companion clock (38.4M Ref clock) for Pulsar and SoC. | Optional Bluetooth I2S bus dout |
| 15 | WGR_D0N | CNVio lane 0 to Pulsar (Negative) Connect to SoC CNVio input D0- pin | Unused |
| 16 | LED2# | Open-drain output capable of driving a platform LED. Optional to connect to Platform LED 2 (if needed). | Open-drain output capable of driving a platform LED. Optional to connect to Platform LED 1 (if needed). |
| 17 | WGR_D0P | CNVio lane 0 to Pulsar (Positive) Connect to SoC CNVio input D0+ pin | Unused |
| 18 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 19 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 20 | UART_WAKE# | Unused | Optional host wake for Bluetooth |

## Table 42-1. RF Companion Module 2230 Pin List (Sheet 2 of 3)

| M.2 Pin# | Hybrid Key E M.2 2230 Pin Name | CNVi RF Companion Pin Description | Standard WLAN Solution Pin Description |
|---|---|---|---|
| 21 | WGR_CLKN | CNVio clock to Pulsar (Negative). Connect to SoC CNVio input CLK- pin | Unused |
| 22 | UART_RX/BRI_RSP | BRI bus output to SoC. Used for Bluetooth data and control between pulsar and the RF companion. Connect to SoC BRI input. | Optional Bluetooth UART bus rx |
| 23 | WGR_CLKP | CNVio clock to Pulsar (Positive) Connect to SoC CNVio input CLK+ pin | Unused |
| 32 | UART_TX/RGI_DT | RGI bus input from SoC. Used for general control between pulsar and the RF companion. Connect to SoC RGI output | Optional Bluetooth UART bus tx |
| 33 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 34 | UART_CTS/RGI_RSP | RGI bus output to SoC. Used for general control between pulsar and the RF companion. Connect to SoC RGI input | Optional Bluetooth UART bus cts |
| 35 | PETP0 | Unused | Wi-Fi* PCIe tx lane 0 |
| 36 | UART_RTS/BRI_DT | BRI bus input from SoC. Used for Bluetooth data and control between pulsar and the RF companion. Connect to SoC BRI output | Optional Bluetooth UART bus rts |
| 37 | PETN0 | Unused | Wi-Fi* PCIe tx lane 0 |
| 38 | CLINK_RESET | Unused | CLINK bus reset |
| 39 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 40 | CLINK_DATA | Unused | CLINK bus data |
| 41 | PERP0 | Unused | Wi-Fi* PCIe rx lane 0 |
| 42 | CLINK_CLK | Unused | CLINK bus clock |
| 43 | PERN0 | Unused | Wi-Fi* PCIe rx lane 0 |
| 44 | COEX3 | Unused | LTE coex standard pin |
| 45 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 46 | COEX2 | Unused | LTE coex UART rx |
| 47 | REFCLKP0 | Unused | Wi-Fi* PCIe clock lane 0 |
| 48 | COEX1 | Unused | LTE coex UART tx |
| 49 | REFCLKN0 | Unused | Wi-Fi* PCIe clock lane 0 |
| 50 | SUSCLK | Slow clock input for low power logic. Connect to a 32Khz clock from the Platform or SoC. | Optional Slow clock input for low power logic. Connect to a 32Khz clock from the Platform or SoC. This clock may not be required- depending on the M.2 module specific requirements |
| 51 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 52 | PERST0# | Unused | Wi-Fi* PCIe reset lane 0 |

## Table 42-1. RF Companion Module 2230 Pin List (Sheet 3 of 3)

| M.2 Pin# | Hybrid Key E M.2 2230 Pin Name | CNVi RF Companion Pin Description | Standard WLAN Solution Pin Description |
|---|---|---|---|
| 53 | CLKREQ0# | Unused | Wi-Fi* PCIe clock request lane 0 |
| 54 | W_DISABLE2# | BT_KILL input. Optional to connect to a Bluetooth KILL signal from the SoC or from the platform | BT_KILL input. Optional to connect to a Bluetooth KILL signal from the SoC or from the platform |
| 55 | PEWAKE0# | Unused | Wi-Fi* PCIe host wake lane 0 |
| 56 | W_DISABLE1# | WLAN_KILL input. Optional to connect to a Wi-Fi* KILL signal from the SoC or from the platform | WLAN_KILL input. Optional to connect to a Wi-Fi* KILL signal from the SoC or from the platform |
| 57 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 58 | A4WP_I2C_DATA | Unused | Unused |
| 59 | WT_D1N | CNVio lane 1 from Pulsar (Negative). Connect to SoC CNVio output D1- pin | Unused |
| 60 | A4WP_I2C_CLK | Unused | Unused |
| 61 | WT_D1P | CNVio lane 1 from Pulsar (Positive) Connect to SoC CNVio output D1+ pin | Unused |
| 62 | A4WP_IRQ# | Unused | Unused |
| 63 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 64 | REFCLK0 | Clock signal. Used The 38.4M ref clock for Pulsar. | Unused |
| 65 | WT_D0N | CNVio lane 0 from Pulsar (Negative) Connect to SoC CNVio output D0- pin | Unused |
| 66 | PERST1# | Unused | Unused |
| 67 | WT_D0P | CNVio lane 0 from Pulsar (Positive) Connect to SoC CNVio output D0+ pin | Unused |
| 68 | CLKREQ1# | Unused | Unused |
| 69 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |
| 70 | PEWAKE1# | Unused | Unused |
| 71 | WT_CLKN | CNVio clock from Pulsar (Negative). Connect to SoC CNVio output CLK- pin | Unused |
| 72 | +V3P3A | Connect all +V3P3A pins to Platform 3.3V supply. | Connect all +V3P3A pins to Platform 3.3V supply. |
| 73 | WT_CLKP | CNVio clock from Pulsar (Positive) Connect to SoC CNVio output CLK+ pin | Unused |
| 74 | +V3P3A | Connect all +V3P3A pins to Platform 3.3V supply. | Connect all +V3P3A pins to Platform 3.3V supply. |
| 75 | GND | Connect all GND pins to Platform ground | Connect all GND pins to Platform ground |

### 42.3.1.2 Module Mechanical Dimensions

The M.2 2230 CRF Module mechanical diagram is shown in figure below.

**Figure 42-2. Module Mechanical Diagram - Source is PCI-SIG M.2 Spec Rev 1.0**

### 42.3.1.3 Hybrid Key-E (2230) Pin-Out

The RF Companion M.2 2230 module is intended to be used with a proprietary pin out "Hybrid Key-E" scheme due to the mechanical similarity to a Key-E connector.

The pinout for "Hybrid Key-E" socket on MB is shown in figure below. The CRF signals listed with the prefix "/" signify that they are electrically MUX'd inside the PCH/SoC and are shared.

**Figure 42-3. Hybrid Key E'Pinout- Platform Side View**

| | Standard M.2 Key E | LcP Signals | LcP Signals | Standard M.2 Key E | |
|---|---|---|---|---|---|
| | | | GND | | 75 |
| 74 | +V3P3A | | WT_CLKP | REFCLKN1 | 73 |
| 72 | +V3P3A | | WT_CLKN | REFCLKP1 | 71 |
| 70 | PEWake1# (IO)(0/3.3V) | | GND | | 69 |
| 68 | CLKREQ1# (IO)(0/3.3V) | | WT_D0P | PERn1 | 67 |
| 66 | PERST1# (O)(0/3.3V) | | WT_D0N | PERp1 | 65 |
| 64 | RESERVED | REFCLK0 (I)(1V@38.4MHz) | GND | | 63 |
| 62 | ALERT# (I)(0/1.8) | A4WP_IRQ# | WT_D1P | PETn1 | 61 |
| 60 | I2C_CLK (O)(0/1.8V) | A4WP_I2C_CLK | WT_D1N | PETp1 | 59 |
| 58 | I2C_DATA (IO)(0/1.8) | A4WP_I2C_DATA | GND | | 57 |
| 56 | W_DISABLE1# (O)(0/3.3V) | | PEWake0# (IO)(0/3.3V) | | 55 |
| 54 | W_DISABLE2# (O)(0/3.3V) | | CLKREQ0# (IO)(0/3.3V) | | 53 |
| 52 | PERST0# (O)(0/3.3V) | | GND | | 51 |
| 50 | SUSCLK(32kHz) (O)(0/3.3V) | C_P32K (3.3V Tolerant) | REFCLKN0 | | 49 |
| 48 | COEX_TXD (O)(0/1.8V) | | REFCLKP0 | | 47 |
| 46 | COEX_RXD (O)(0/1.8V) | | GND | | 45 |
| 44 | COEX3 (IO)(0/1.8V) | | PERn0 | | 43 |
| 42 | CLink CLK | | PERp0 | | 41 |
| 40 | CLink DATA | | GND | | 39 |
| 38 | CLink RESET (O)(0/3.3V) | | PETn0 | | 37 |
| 36 | LPSS UART RTS (O)(0/1.8V) | / BRI_DT (MUX'd in PCH/SoC) | PETp0 | | 35 |
| 34 | LPSS UART CTS (I)(0/1.8V) | / RGI_RSP (MUX'd in PCH/SoC) | GND | | 33 |
| 32 | LPSS UART Tx (O)(0/1.8V) | / RGI_DT (MUX'd in PCH/SoC) | Connector Key | | E |
| E | Connector Key | | Connector Key | | |
| | Connector Key | | Connector Key | | |
| | Connector Key | | Connector Key | | |
| | Connector Key | | WGR_CLKP | SDIO Reset#(O)(0/1.8V) | 23 |
| 22 | LPSS UART Rx (I)(0/1.8V) | / BRI_RSP (MUX'd in PCH/SoC) | WGR_CLKN | SDIO Wake#(I)(0/1.8V) | 21 |
| 20 | UART Wake# (I)(0/3.3V) | | GND | SDIO DAT3(IO)(0/1.8V) | 19 |
| 18 | GND | GND/LNA_EN (LcP Production) | WGR_D0P | SDIO DAT2(IO)(0/1.8V) | 17 |
| 16 | LED2# (I)(OD) | | WGR_D0N | SDIO DAT1(IO)(0/1.8V) | 15 |
| 14 | PCM_OUT (O)(0/1.8V) | / CLKREQ0 (MUX'd in PCH/SoC) | GND | SDIO DAT0(IO)(0/1.8V) | 13 |
| 12 | PCM_IN (I)(0/1.8V) | | WGR_D1P | SDIO CMD(IO)(0/1.8V) | 11 |
| 10 | PCM_SYNC (OI)(0/1.8V) | /RF_RESET_B (MUX'd in PCH/SoC) | WGR_D1N | SDIO CLK(O)(0/1.8V) | 9 |
| 8 | PCM_CLK (OI)(0/1.8V) | | GND | | 7 |
| 6 | LED1# (I)(OD) | | USB_D- | | 5 |
| 4 | +V3P3A | | USB_D+ | | 3 |
| 2 | +V3P3A | | GND | | 1 |

### 42.3.1.4 Special Considerations for Hybrid Key-E Scheme

The "Hybrid Key-E" scheme relies on assigning multiple functions to M.2 connector pins and to PCH pins. This causes a significant reduction in the amount of signals that needs to be routed between the SoC and the M.2 module.

### 42.3.1.5 Shared M.2 Socket Pins

The following M.2 pins are shared between different functions:

- **PCIe-1/CNVio**

These are 6 pins which are assigned to the PCIe-1 bus in the M.2 standard pinout. This bus has 3 differential pairs, two for the PCIe data lanes (one per direction) and one for the PCIe clock. In the "Hybrid Key-E" scheme these signals are used for CNVio interface from Pulsar to the RF companion chip. Due to this sharing, the "Hybrid Key-E" scheme does not support PCIe-1.

- **SDIO/CNVio**

These are 8 pins which are assigned to the SDIO bus in the M.2 standard pinout. This bus has 8 signals, 4 bi-directional for the SDIO data, one be-directional command signal, one clock (SoC to M.2) and 2 control (Reset SoC to M.2, Wake M.2 to SoC). In the "Hybrid Key-E" scheme these signals are used for CNVio interface the RF companion chip to Pulsar (6 for CNVio and 2 for ground). Due to this sharing, the "Hybrid Key-E" scheme does not support SDIO.

- **PCM/ClockReq and Reset**

The standard M.2 defines 4 pins for a dedicated PCM audio serial bus for Bluetooth. In the "Hybrid Key-E" scheme, two of these signals are used for CNVi Clock (from RF companion to SoC) and Reset (For SoC to RF companion). Since the PCM serial bus is connected to PCH GPIO pins, and the CNVi clock request and reset pins are also connected to PCH GPIO pins, it is possible to have support for both PCM bus and CNVi signals by changing the PCH GPIO multiplexing function select. Due to this sharing, the "Hybrid Key-E" scheme can still support PCM (for discrete Bluetooth connectivity with PCM support).

- **UART (Bluetooth) / BRI and RGI**

The standard M.2 defines 4 pins for a dedicated UART serial bus for Bluetooth. In the "Hybrid Key-E" scheme, all these signals are used for CNVi BRI (Bluetooth Radio Interface) and RGI (Radio Generic interface), each comprising of 2 signals (one per direction). Since the UART serial bus is connected to PCH GPIO pins, and the CNVi BRI, RGI are also connected to PCH GPIO pins, it is possible to have support for both UART bus and CNVi signals by changing the PCH GPIO multiplexing function select. Due to this sharing, the "Hybrid Key-E" scheme can still support Bluetooth UART (for discrete connectivity with BT-UART support).

- **SUSCLK/P_32K**

These signals are both functionally similar. In the M.2 standard this pin is optionally connected to a 32 KHz RTC clock.

- **GND/LNA_EN**

This signal is used for different purposes in CNVi and discrete but in both cases should be connected to ground, therefore it does not affect functionality.

- **A4WP+Ref clock**

In the "Hybrid Key-E" scheme only one of these 4 signals used. This REFCLK0 signal connects the reference clock (single ended, 1V p-p, 38.4MHz) from the RF companion to the SoC. The remaining 3 signals are not used.

- **Non-shared M.2 socket pins**

The functions of these pins impacted by the "Hybrid Key-E" scheme as will be described below:

- **V3P3A, GND**

These are the M.2 card power supply (3.3V) and Ground pins. These pins have the same purpose in either discrete or CNVi implementations and therefore are not affected by the "Hybrid Key-E" scheme.

- **PEWake1#, CLKREQ1#, PERST1#**

These are 3 control signals used by the PCIe-1 bus in standard M.2 cards. Although these signals are not shared with any other function, they have no usage in a "Hybrid Key-E" scheme design. This is because the PCIe-1 bus by itself is not usable (see PCIe-1/CNVio sharing above).

- **PCIe-0 Bus**

This consists of 6 signals (3 differential pairs) used for PCIe data to and from the SoC, and a single pair used for the PCIe bus clock. In a CNVi RF companion these signals are left unused. In standard discrete these signals are being used as the Wi-Fi* bus interface.

- **W_DISABLE1#, W_DISABLE2#,**

These are used for Wi-Fi* and Bluetooth RF-Kill control respectively. Asserting these signals effectively shuts off the RF transmission or the relevant core.

- **PEWake0#, CLKREQ0#, PERST0#**

These are 3 control signals used by the PCIe-0 bus in standard M.2 cards. They should be routed to SoC pins which are assigned to GPIOs in Discrete or Combo modes.

- **Coex UART Interface**

This consist of 3 signals (two UART bus signals and one GPIO) used for Wi-Fi* - LTE coexistence signaling in the M.2 standard definition.

Since these pins are left unused in the RF companion, they can still be used with a discrete M.2 card even when designing with the "Hybrid Key-E" scheme.

In platforms that are designed to support a WWAN modem and "Hybrid Key-E" there should be 3 pins connected to each signal, to allow the modem to connect to the M.2 pin (in the discrete connectivity case) or to the PCH (in the CNVi case). See Section 42.5.6, "Modem Coexistence 3-way UART Connection" for more details on the UART connection between WWAN, PCH and CNVi.

- **CLINK Interface**

This consist of 3 signals (clock, data and reset). This bus in an Intel proprietary bus. Since these pins are left unused in the RF companion, they can still be used with a discrete M.2 card even when designing with the "Hybrid Key-E" scheme.

- **LED1, LED2**

These are optional pins that are assigned to drive LEDs on the platform in the standard M.2 cards. They are used for the same function when using CNVi and therefore are not affected by the "Hybrid Key-E" scheme.

- **USB Bus**

The standard M.2 defines 2 pins for a differential USB bus. This has no usage in the RF companion.

When using a standard M.2 discrete card, the pins will have the standard functionality and are not affected by the "Hybrid Key-E" scheme. The different connectivity interfaces as used by a discrete connectivity (Standard M.2, Intel connectivity or TPV), CNVi RF companion card are summarized in table below.

**Table 42-2. Connectivity Interfaces for Different M.2 2230 Cards**

| M.2 interface | CNVi | Discrete |
|---|---|---|
| PCIe-1 | M.2 pins are not connected to the CRF. Wi-Fi* uses internal IOSF to interface the host. | Used for Wi-Fi* host interface |
| PCIe-2 | Not functional<br>Pins are connected to CRF and Pulsar CNVio and can't be used as PCIe. | Not functional<br>Pins are connected to Pulsar CNVio and can't be used as PCIe. |
| Wi-Fi* SDIO | Not functional<br>Pins are connected to CRF and Pulsar CNVio and can't be used as SDIO. | Not functional<br>Pins are connected to Pulsar CNVio and can't be used as SDIO. |
| Wi-Fi* CLINK | M.2 pins are not connected to the CRF. Wi-Fi* uses internal CLINK to interface the ME. | Used for Wi-Fi* ME interface |
| Wi-Fi* RF-Kill | Used (optional) | Used (optional) |
| Bluetooth USB | M.2 pins are not connected to the CRF. Bluetooth uses internal U2U to interface the host. | Used for Bluetooth USB interface |
| Bluetooth UART | M.2 pins are not connected to the CRF. Bluetooth uses internal UART to interface the host. | Used for Bluetooth UART interface |
| Bluetooth I2S (Audio) | M.2 pins are not connected to the CRF. Bluetooth uses internal I2S to interface the host. | Used for Bluetooth I2S interface |
| Bluetooth wake | M.2 pin is not connected to the CRF. Bluetooth uses internal vGPIO. | Used for Bluetooth wake signal |
| Bluetooth RF-Kill | Used (optional) | Used (optional) |
| UART bus to ISH | Pins are connected to Refclock (38.4M system clock). An internal UART is used to connect Pulsar to ISH | Pins are connected to Refclock (38.4M system clock). Can be used for ISH UART connection. |
| I2C bus to A4WP | Unused. | Unused. |
| Power supply | Used per M.2 standard | Used per M.2 standard |
| GND | Used per M.2 standard | Used per M.2 standard |

## 42.3.2 Soldered Down M.2 (SD-1216)

The RF Companion SD-1216 module has the same mechanical outline as the standard M.2 connectivity type 1216-S3. The standard M.2 land pattern is modified to accommodate the proprietary RF Companion Module signals. As opposed to the Connectorized module, the SD-1216 module is not sharing the standard M.2 pads for the RF companion functions. Instead, it has an additional set of solder pads which don't overlap with the standard solder pads. This allows having a single motherboard design that can accommodate either a standard M.2 1216 card or an RF companion 1216 card. However unlike the connectorized case, swapping cards requires removing a soldered

down module and can't be done by a simple socket card exchange. Additionally the assembly tooling and BOM should change between a discrete and CNVi motherboards assembly.

#### 42.3.2.1 Soldered Down 1216 Module Pinout

As explained above, the RF companion module M.2 1216 card has a proprietary set of pads and does no reuse the standard M.2 pads. The special pad-out required for supporting CNVi and discrete on the same motherboard real-estate is shown in Figure below. The corresponding pin-description and CRF signals are shown in Figure 42-5 and Table 42-3 respectively.

**Figure 42-4. SD-1216 Module Pad-out for Supporting CNVi and Discrete 1216 Modules**

## Figure 42-5. Pin Out Scheme for Dual CNVi/Discrete 1216 Footprint

## Table 42-3. RF Companion Module 1216 Pin List (CNVi only) (Sheet 1 of 5)

| Pin # | Pin Name | Function When CNVi is used | Function when Standard M.2 is Used |
|---|---|---|---|
| 1 | UIM_POWER_SRC/ GPIO1 | Not used | UIM_POWER_SRC/ GPIO1 |
| 2 | UIM_POWER_SNK | Not used | UIM_POWER_SNK |
| 3 | UIM_SWP | Not used | UIM_SWP |
| 4 | 3.3V | 3.3V | 3.3V |
| 5 | 3.3V | 3.3V | 3.3V |
| 6 | GND | GND | GND |
| 7 | RESERVED | Not used | RESERVED |
| 8 | ALERT# | Not used | ALERT# |
| 9 | I2C_CLK | Not used | I2C_CLK |
| 10 | I2C_DATA | Not used | I2C_DATA |

## Table 42-3. RF Companion Module 1216 Pin List (CNVi only) (Sheet 2 of 5)

| Pin # | Pin Name | Function When CNVi is used | Function when Standard M.2 is Used |
|---|---|---|---|
| 11 | COEX_TXD | Not used | COEX_TXD |
| 12 | COEX_RXD | Not used | COEX_RXD |
| 13 | COEX3 | Not used | COEX3 |
| 14 | SYSCLK/GNSS0 | Not used | SYSCLK/GNSS0 |
| 15 | TX_BLANKING/GNSS1 | Not used | TX_BLANKING/GNSS1 |
| 16 | RESERVED | Not used | RESERVED |
| 17 | GND | GND | GND |
| 18 | RESERVED | Not used | Not used |
| 19 | RESERVED | Not used | Not used |
| 20 | GND | GND | GND |
| 21 | RESERVED | Not used | Not used |
| 22 | RESERVED | Not used | Not used |
| 23 | GND | GND | GND |
| 24 | RESERVED | Not used | Not used |
| 25 | RESERVED | Not used | Not used |
| 26 | GND | GND | GND |
| 27 | SUSCLK(32kHz)(3.3V) | Not used | SUSCLK(32kHz)(3.3V) |
| 28 | W_DISABLE1# | W_DISABLE1# | W_DISABLE1# |
| 29 | PEWAKE# | Not used | PEWAKE# |
| 30 | CLKREQ# | Not used | CLKREQ# |
| 31 | PERST# | Not used | PERST# |
| 32 | GND | GND | GND |
| 33 | REFCLKN0 | Not used | REFCLKN0 |
| 34 | REFCLKP0 | Not used | REFCLKP0 |
| 35 | GND | GND | GND |
| 36 | PERn0 | Not used | PERn0 |
| 37 | PERp0 | Not used | PERp0 |
| 38 | GND | GND | GND |
| 39 | PETn0 | Not used | PETn0 |
| 40 | PETp0 | Not used | PETp0 |
| 41 | GND | GND | GND |
| 42 | CLink_CLK | Not used | CLink_CLK |
| 43 | CLink_DATA | Not used | CLink_DATA |
| 44 | CLink_RESET | Not used | CLink_RESET |
| 45 | SDIO_RESET# | Not used | Not used |
| 46 | SDIO_WAKE# | Not used | Not used |
| 47 | SDIO_DATA3 | Not used | Not used |
| 48 | SDIO_DATA2 | Not used | Not used |
| 49 | SDIO_DATA1 | Not used | Not used |

## Table 42-3. RF Companion Module 1216 Pin List (CNVi only) (Sheet 3 of 5)

| Pin # | Pin Name | Function When CNVi is used | Function when Standard M.2 is Used |
|---|---|---|---|
| 50 | SDIO_DATA0 | Not used | Not used |
| 51 | SDIO_CMD | Not used | Not used |
| 52 | SDIO_CLK | Not used | Not used |
| 53 | UART_WAKE# (3.3V) | Not used | UART_WAKE# (3.3V) |
| 54 | LPSS_UART_RTS/bri_dt | Not used | LPSS_UART_RTS/ bri_dt |
| 55 | LPSS_UART_RXD/ bri_rsp | Not used | LPSS_UART_RXD/ bri_rsp |
| 56 | LPSS_UART_TXD/rgi_dt | Not used | LPSS_UART_TXD/ rgi_dt |
| 57 | LPSS_UART_CTS/rgi_rsp | Not used | LPSS_UART_CTS/ rgi_rsp |
| 58 | PCM_SYNC/I2S_WS | Not used | PCM_SYNC/I2S_WS |
| 59 | PCM_OUT/I2S_SD_OUT | Not used | PCM_OUT/ I2S_SD_OUT |
| 60 | PCM_IN/I2S_SD_IN | Not used | PCM_IN/I2S_SD_IN |
| 61 | PCM_CLK/I2S_SCK | Not used | PCM_CLK/I2S_SCK |
| 62 | GND | GND | GND |
| 63 | W_DISABLE2# | W_DISABLE2# | W_DISABLE2# |
| 64 | LED2# | LED2# | LED2# |
| 65 | LED1# | LED1# | LED1# |
| 66 | RESERVED | Not used | RESERVED |
| 67 | RESERVED | Not used | RESERVED |
| 68 | GND | GND | GND |
| 69 | USB_D- | Not used | USB_D- |
| 70 | USB_D+ | Not used | USB_D+ |
| 71 | GND | GND | GND |
| 72 | 3.3V | 3.3V | 3.3V |
| 73 | 3.3V | 3.3V | 3.3V |
| 74 | GND | GND | GND |
| 75 | GND | GND | GND |
| 76 | GND | GND | GND |
| 77 | GND | GND | GND |
| 78 | GND | GND | GND |
| 79 | GND | GND | GND |
| 80 | GND | GND | GND |
| 81 | GND | GND | GND |
| 82 | GND | GND | GND |
| 83 | GND | GND | GND |
| 84 | GND | GND | GND |
| 85 | GND | GND | GND |

## Table 42-3. RF Companion Module 1216 Pin List (CNVi only) (Sheet 4 of 5)

| Pin # | Pin Name | Function When CNVi is used | Function when Standard M.2 is Used |
|---|---|---|---|
| 86 | GND | GND | GND |
| 87 | GND | GND | GND |
| 88 | GND | GND | GND |
| 89 | GND | GND | GND |
| 90 | GND | GND | GND |
| 91 | GND | GND | GND |
| 92 | GND | GND | GND |
| 93 | GND | GND | GND |
| 94 | GND | GND | GND |
| 95 | GND | GND | GND |
| 96 | GND | GND | GND |
| G1 | GND | GND | GND |
| G2 | GND | GND | GND |
| G3 | GND | GND | GND |
| G4 | GND | GND | GND |
| G5 | GND | GND | GND |
| G6 | GND | GND | GND |
| G7 | GND | GND | GND |
| G8 | GND | GND | GND |
| G9 | GND | GND | GND |
| G10 | GND | GND | GND |
| G11 | GND | GND | GND |
| G12 | GND | GND | GND |
| | | | |
| A07 | GND | GND | Not Applicable |
| A08 | A4WP_IRQ# | A4WP_IRQ# | Not Applicable |
| A09 | A4WP_CLK | A4WP_CLK | Not Applicable |
| A10 | A4WP_DATA | A4WP_DATA | Not Applicable |
| A11 | RESERVED | RESERVED | Not Applicable |
| A12 | RESERVED | RESERVED | Not Applicable |
| A13 | RESERVED | RESERVED | Not Applicable |
| A14 | RESERVED | RESERVED | Not Applicable |
| A15 | LNA_EN | GND | Not Applicable |
| A16 | RESERVED | RESERVED | Not Applicable |
| A17 | RESERVED | RESERVED | Not Applicable |
| A18 | RESERVED | RESERVED | Not Applicable |
| A19 | WT_CLKP | WT_CLKP | Not Applicable |
| A20 | WT_CLKN | WT_CLKN | Not Applicable |
| A21 | WT_D0P | WT_D0P | Not Applicable |

## Table 42-3. RF Companion Module 1216 Pin List (CNVi only) (Sheet 5 of 5)

| Pin # | Pin Name | Function When CNVi is used | Function when Standard M.2 is Used |
|---|---|---|---|
| A22 | WT_D0N | WT_D0N | Not Applicable |
| A23 | WT_D1P | WT_D1P | Not Applicable |
| A24 | WT_D1N | WT_D1N | Not Applicable |
| A25 | C_P32K | C_P32K | Not Applicable |
| A26 | GND | GND | Not Applicable |
| A27 | RESERVED | RESERVED | Not Applicable |
| A28 | RESERVED | RESERVED | Not Applicable |
| A29 | RESERVED | RESERVED | Not Applicable |
| A30 | RESERVED | RESERVED | Not Applicable |
| A31 | GND | GND | Not Applicable |
| A32 | WGR_CLKP | WGR_CLKP | Not Applicable |
| A33 | WGR_CLKN | WGR_CLKN | Not Applicable |
| A34 | WGR_D0P | WGR_D0P | Not Applicable |
| A35 | WGR_D0N | WGR_D0N | Not Applicable |
| A36 | WGR_D1P | WGR_D1P | Not Applicable |
| A37 | WGR_D1N | WGR_D1N | Not Applicable |
| A38 | BRI_DT | BRI_DT | Not Applicable |
| A39 | BRI_RSP | BRI_RSP | Not Applicable |
| A40 | RGI_DT | RGI_DT | Not Applicable |
| A41 | RGI_RSP | RGI_RSP | Not Applicable |
| A42 | RF_RESET_B | RF_RESET_B | Not Applicable |
| A43 | CLKREQ0 | CLKREQ0 | Not Applicable |
| A44 | REFCLK0 | REFCLK0 | Not Applicable |
| A45 | NO CONNECT | NO CONNECT | Not Applicable |
| A46 | RESERVED | RESERVED | Not Applicable |
| A47 | RESERVED | RESERVED | Not Applicable |
| A48 | 3.3V | 3.3V | Not Applicable |
| A49 | 3.3V | 3.3V | Not Applicable |
| A50 | GND | GND | Not Applicable |

### 42.3.2.2 Soldered Down 1216 Module Mechanical Dimensions

**Figure 42-6. 1216 Module Mechanical Diagram**

### 42.3.2.3 Breakout Example for JfP Soldered Down Module

The soldered down JfP module has a special pad shape which combines the standard M.2 pad ring on the outside with the new inner ring of the CNVi pads. It is recommended to consider all signal properties when designing the motherboard for dual discrete/CNVi design supporting Jefferson Peak 1216. An example for the breakout layout for a type-3 board (with no micro-via) is shown in the figure below**.**

***Note:*** In order to keep the picture clear, this example shows only 2 signal layers (top layer and 3’rd layer) while the other layers are not shown. Also there is an assumption that the second layer shall be ground.

**Figure 42-7. Board Layout Example Showing Breakout from JfP 1216 pads**

## 42.4 Platform Considerations

### 42.4.1 Selecting Connectivity Solution

The platform motherboard can be designed to support discrete connectivity (either Intel or TPV), integrated connectivity (CNVi).

***Note:*** All CNVi 2230 SKUs can support a "Hybrid Key-E" routing with no jumpers. When considering a TPV module one should only use a Key-E module if the motherboard design is "Hybrid Key-E". A Key-A module will not fit into this scheme.

**Table 42-4. CNVi Module SKUs (Sheet 1 of 2)**

| SKU | M.2 type | Wi-Fi* chains | LTE coex (on-module BAW filter) | Comments |
|---|---|---|---|---|
| JfP1 2230 | 2230 | 1x1 | No | Basic 1x1 |
| JfP1 2230 diversity | 2230 | 1x1 | No | Basic 1x1 with diversity |
| JfP1-SD | 1216 | 1x1 | No | Solder-down 1x1 |

**Table 42-4. CNVi Module SKUs (Sheet 2 of 2)**

| SKU | M.2 type | Wi-Fi* chains | LTE coex (on-module BAW filter) | Comments |
|---|---|---|---|---|
| JfP1-SD diversity | 1216 | 1x1 | No | Solder-down 1x1 with diversity |
| JfP2 2230 | 2230 | 2x2 | No | Basic 2x2 |
| JfP2 2230 vPro | 2230 | 2x2 | No | vPro 2x2 |
| JfP2 2230 vPro Coex | 2230 | 2x2 | Yes | vPro 2x2 with Coex |
| JfP2 SD | 1216 | 2x2 | No | Solder-down 2x2 |
| JfP2 SD Coex | 1216 | 2x2 | Yes | Solder-down 2x2 with LTE Coex |
| JfP2 SD vPro | 1216 | 2x2 | No | Solder-down vPro 2x2 |

**Table 42-5. Intel Discrete Module SKUs**

| SKU | M.2 type | Wi-Fi* chains | LTE coex (on-module BAW filter) | Comments |
|---|---|---|---|---|
| ThP2 2230 | 2230 | 2x2 | No | Basic 2x2 module |
| ThP2 2230 vPro | 2230 | 2x2 | No | vPro 2x2 module |

## 42.4.2 CNVi Reference Clock

The two configurations related to having a M.2 discrete or CNVi (with no clock sharing) is shown in Figure 42-8, “CNVi Clock Connections” and Figure 42-9, “Discrete Clock Connections” respectively.

## Figure 42-8. CNVi Clock Connections

**Figure 42-9. Discrete Clock Connections**

### 42.4.2.1 SoC Pin-straps Configurations Related to CNVi and Clock Sharing

An SoC that supports CNVi has special interfaces and configurations that needs to be set properly even if the platform is not using integrated connectivity (CNVi).

**Pin Straps**

These are SoC pins which are used at power-up to determine whether an RF companion exists or not. Based on this information the PCH will determine how to run the boot flow and how to configure internal logic that has different behavior when using M.2 discrete versus CNVi.

For CFL platform with CNP PCH, the SoC uses the RGI_DT signal to drive this pin strap. The property of this signal is that it is connected to a strong pull-down resistor at the time of CRF power up. Based on this property, with an additional SoC pull-up resistor on this GPIO pin, the CNVi/discrete option can be resolved. Refer to Table 42-6 for the details of the SoC straps for PCH.

***Note:*** CNVi RGI_DT pin gets the pull-down resistor (1K ohm) from the internal CRF module when CNVi is enabled. There must not be any pull-down resistor connected on the board.

**PCH Main Clock Source**

Alternatively, the CFL SoC shall be configured to have 2 clocks: One for the Pulsar IP and another one for the rest of the PCH circuitry. When CNVi is not used, the main clock source for the PCH is the PCH main crystal clock.

**Table 42-6. SoC Straps Related to CNVi and Clock Sharing**

| SoC | Configuration | XTAL input mode | XTAL input freq (XTAL_SEL1) | XTAL_SEL2 | SoC clock source |
|---|---|---|---|---|---|
| CNL (CNP PCH) | CNVi Mode | Disconnected<br>Pulled up internally | Pulled up for 24M | Pulled down by an internal resistor (1K ohm) within the CRF module via CNVi RGI_DT pin | SoC crystal oscillator.<br>A 24M XTAL_IN and XTAL_OUT |
| | Discrete Mode | Disconnected<br>Pulled up internally | | Pulled up by an external resistor (20K ohm) and by Discrete UART0_TXD pin | |

## 42.4.3 SoC RCOMP Pin Connection

The RCOMP pin is a SoC pin which is connected to a calibration resistor. This pin is used for interfacing an internal calibration circuit used for the CNVio bus. When the CNVio bus goes out of power up, Pulsar will run a self-calibration sequence which will result in calibrating the CNVio ports to the desired impedance. The RCOM resistance value shall be set to 150 ohm within 1% accuracy.

## 42.4.4 RF-Kill and LED Support

In legacy platforms, the RF-Kill and LED features are used to control the Wi-Fi* and Bluetooth operation (RF-Kill) and indicate Wireless link status (LED).

The traditional motherboard design has both functions built with direct connection between the connectivity card (M.2 pins) and discrete platform components (e.g. Laser Emitting Diodes for LED and pushbutton switches for RF-Kill).

In newer platforms these functions can be supported in various different methods including SW control. To maintain compatibility to legacy motherboard designs, the CRF is designed with RF-Kill and LED support.

The following limitations should be considered if RF-Kill or LED legacy support is required for a specific platform design:

- RF-Kill and LED pins for a JfP(2x2) and ThP (Discrete) modules (either 2230 or 1216) use dedicated pins of the CRF chip and are connected to the standard M.2 pins dedicated to these functions namely:
  - W_DISABLE2# for Bluetooth RF-Kill
  - W_DISABLE1# for Wi-Fi* RF-Kill

In some cases the platform design is required to have an explicit Wi-Fi* and Bluetooth disable function in BIOS to completely shut down Wi-Fi* and Bluetooth even when the connectivity module HW is connected on the board. To support this design, the M.2 W_DISABLE# pins should be routed to SoC GPIOs and forced to a logical zero by BIOS for disabling the Wi-Fi* and Bluetooth completely.

### 42.4.5 CLINK Support

For CNVi CLINK is internal to the PCH and does not need an connection. In order to support CLINK with discrete M.2 modules (such as Thunder Peak) connect the CLINK to the CLINK pins of the M.2 connector.

### 42.4.6 CNVi Power Supply Connections

Integrated connectivity (CNVi) power delivery has two parts:

- The integrated part- which is directly connected to the SoC power delivery
- The external part- which is similar to the standard M.2 power supply scheme

The integrated part of CNVi relays on the PCH power rails and therefore no additional routing or power budgeting is required beyond the PCH recommended design. Figure 42-10 provides information on the pin connections which control power delivery to CNVi IP inside PCH. To complete the picture this figure also shows the M.2 module power supply pins (Note: These are the same for either a standard M.2 module or a CRF).

Note that the PCH-H contains an internal 1.8V linear regulator that is capable of powering the VCCPRIM1P8 rail without adding a 1.8V voltage regulator to the platform. Therefore there are 2 optional configurations:

- Platform supplies the 1.8V rail directly
- 1.8V rail is power by the PCH internal 1.8V LDO

The two options has different connection scheme at the platform level which is shown in Figure 42-10 and Figure 42-11 below.

The power delivery is the same for a CNVi only design and for a CNVi/Discrete (dual) design.

In some designs, the connectivity solution is powered by a power switch which allows the PCH to dynamically control the 3.3V supply to the M.2 card. This is done in the PCH by using a signal called SLP_WLAN# (active low) to control a power switch on the motherboard which feeds the M.2 supply pins.

When designing the platform for CNVi, it is recommended to either not have this switch in the design, or hardware it to be always-on by following PCH. This is because the operation of the RF companion module does not allow switching off its main power in any system state that the PCH is powered on, in order to keeping synchronization with PCH all the time.

Refer to the technical white-paper (RDC#573970) related to the correct usage of Load Switch.

Note that the power supply to the M.2 module is connected directly to the platform V3.3A rail without having any controlled power switch on the line. This ensures that the CNVi will be powered early in the platform power up process as required by the CNVi power up sequencing. Note that CNVi does not support wake on WLAN/BT during deep system sleep states (DSx). Connecting the CRF to 3.3V_DSW rail is not recommended since the PCH rails needed for CNVi will be powered off in deep system sleep state, getting out of DSx requires the CNVi, in the PCH, to Boot, Cold-Boot, in any case so no real value to have the CRF on 3.3V_DSW.

**Figure 42-10.CNVi Power Connections with 1.8V Platform VR**

**Figure 42-11.CNVi Power Connections with Internal 1.8V LDO**

***Note:*** When CNVi is not used in the design:

- VCCDPHY_1P24 (balls AK22, AK23) pin shall be disconnected from the VCCDPHY_1P24 (AJ22, AJ23, BG5) pin.
- The decoupling capacitor shall remain connected to the VCCDPHY_1P24 (AJ22, AJ23, BG5) pin.

***Notes:***

1. Refer to the technical advisory (RDC#574860) related to the usage of internal LDO

2. Refer to the technical white-paper (RDC#573970) related to the usage of Load Switch

## 42.4.7 Electrical Specifications for CNVi 1.8V Signals

For using GPP_D bank signals for CNVi, the input voltage to the VCCPGPPD pin must be set to 1.8V.

The below diagrams illustrate the detailed electrical requirements for the 1.8V CNVi signals:

**Table 42-7. Input/Output Electrical Specifications**

| I/O Type | Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| 1.8V I/O<br><br>RF_RESET_B | $V_{IH}$ | Input High Voltage | 1.26 | 2.1 | V | |
| | $V_{IL}$ | Input Low Voltage | -0.3 | 0.54 | V | |
| | $R_{PU/PD}$ | Weak Pull-Up or Pull-Down | 70 | 150 | Kohm | |
| | $I_{IN}$ | Input Leakage Current | | 10 | uA | No Pull Up/ Down |
| | $V_{OH}$ | Output High Voltage | 1.62 | 1.8 | V | Io = 2mA<br>Load = 20pF |
| | $V_{OL}$ | Output Low Voltage | 0 | 0.18 | | Io = 2mA<br>Load = 20pF |
| | $T_R$, $T_F$ | Rise, Fall Time | | 6 | ns | Load = 20pF |
| | $C_{IO}$ | IO Pin Capacitance | | 2 | pF | |
| 1.8V FS I/O<br><br>A4WP_IRQ#<br>A4WP_I2C_CLK<br>A4WP_I2C_CLK<br>(Note 1) | $V_{IH}$ | Input High Voltage | 1.26 | 2.1 | V | |
| | $V_{IL}$ | Input Low Voltage | -0.3 | 0.54 | V | |
| | $R_{PU/PD}$ | Weak Pull-Up or Pull-Down | 100 | 180 | Kohm | |
| | $I_{IN}$ | Input Leakage Current | | 10 | uA | No Pulls |
| | $V_{OL}$<br>Push-Pull | Output Low Voltage<br>Push-pull | 0 | 0.36 | | Io = 2mA<br>Load = 50pF |
| | $V_{OH}$<br>Push-Pull | Output Low Voltage<br>Push-pull | 1.62 | 1.8 | | Io = 2mA<br>Load = 50pF |
| | $T_R$, $T_F$<br>Push-Pull | Rise, Fall Time<br>Push-pull | | 18.5 | ns | Load = 50pF |
| | $V_{OL}$<br>Open Drain | Output Low Voltage | 0 | 0.36 | | Io = 2mA<br>Load = 64pF<br>RPU = 1Kohm |
| | $C_{IO}$ | IO Pin Capacitance | | 2 | pF | |
| 1.8V FS_CR<br><br>CLKREQ0<br>(Note 2) | $V_{IH}$ | Input High Voltage | 1.26 | 2.1 | V | |
| | $V_{IL}$ | Input Low Voltage | -0.3 | 0.54 | V | |
| | $R_{PU/PD}$ | Weak Pull-Up or Pull-Down | 100 | 180 | Kohm | |
| | $I_{IN}$ | Input Leakage Current | | 10 | uA | No Pulls |
| | $V_{OH}$ | Output High Voltage | 1.62 | 1.8 | V | Io = 2mA<br>Load = 20pF |
| | $V_{OL}$ | Output Low Voltage | 0 | 0.18 | | Io = 2mA<br>Load = 20pF |
| | $T_R$, $T_F$ | Rise, Fall Time | | 18.5 | ns | Load = 20pF |
| | $C_{IO}$ | IO Pin Capacitance | | 2 | pF | |

| I/O Type | Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| 1.8V FS_3VT<br><br>C_P32K<br>(Note 3) | $V_{IH}$ | Input High Voltage | 1.26 | 2.1 | V | |
| | $V_{IL}$ | Input Low Voltage | -0.3 | 0.54 | V | |
| | $R_{PU/PD}$ | Weak Pull-Up or Pull-Down | 150 (typical) | | Kohm | |
| | $I_{IN}$ | Input Leakage Current | | 10 | uA | No Pulls |
| | $V_{OH}$ | Output High Voltage | 1.62 | 1.8 | V | Io = 1mA<br>Load = 30pF |
| | $V_{OL}$ | Output Low Voltage | 0 | 0.18 | | Io = 1mA<br>Load = 30pF |
| | $T_R$, $T_F$ | Rise, Fall Time | | 20 | ns | Load = 30pF |
| | $C_{IO}$ | IO Pin Capacitance | | 2 | pF | |
| BRI and RGI 1.8V I/O<br><br>BRI_DT<br>BRI_RSP<br>RGI_DT<br>RGI_RSP<br>(Note 4) | $V_{IH}$ | Input High Voltage | 1.26 | TBD | V | |
| | $V_{IL}$ | Input Low Voltage | TBD | 0.54 | V | |
| | $R_{PU/PD}$ | | | | | |
| | $I_{IN}$ | | | | | |
| | $V_{OH}$ | Output High Voltage | 1.62 | 1.8 | V | 50ohm driver impedance<br>Load = 35pF |
| | $V_{OL}$ | Output Low Voltage | 0 | 0.18 | | |
| | $T_R$, $T_F$ | Rise, Fall Time | 1.5 | 4.5 | ns | |
| | $R_b$ | Baud rate | 4.8 | 76.8 | Mbaud | Tolerance +/- 5% |
| | $C_{IO}$ | IO Pin Capacitance | | 2 | pF | |
| CNVio<br>(Note 5) | Signal parameters follow the MIPI D-PHY Specifications Rev1.1 | | | | | |

***Notes:***

1. I2C max speed will be 1MHz (Fast plus Mode). I2C SDA & SCL I/Os must comply with 120ns max rise/fall time. I/O are protected against back-bias up to 1.8V and can withstand I/O voltage when the power supply is off.
2. I/O are protected against back-bias up to 1.98V and can withstand I/O voltage when the power supply is off.
3. Input is 3.6V tolerant. I/O are protected against back-bias up to 3.6V and can withstand I/O voltage when the power supply is off.
4. I/O are protected against back-bias up to 1.98V and can withstand I/O voltage when the power supply is off.
5. The D-PHY I/O pins must comply with the DC electrical specifications in "MIPI Alliance Specification for D-PHY Rev1.1." Specifically, the D-PHY JfP transmitter (JfP to Pulsar) DC characteristics are found in Section 9.1, Table 16. The D-PHY JfP receiver (Pulsar to JfP) DC characteristics are found in Section 9.2, Table 20.

### 42.4.8 CNVi Power Rails Table

| Voltage (V) | Source | Input | Comments |
|---|---|---|---|
| 3.3V (M.2 Supply) | Platform VR | 3.3V supply pin on Connectivity M.2 | Must be always on for CNVi<br>Power gating not allowed |
| 1.8 | Platform VR or PCH internal H-LDO PCH pins VCCPHVLDO_1P8[2] | VCCPRIM_1P8[5] | Depends on the presence of a 1.8V platform VR or PCH internal 1.8V LDO. For internal LDO configuration short VCCPHVLDO_1P8[2] to VCCPRIM_1P8[5] |
| 1.05 | Platform VR | VCCPRIM_1P05[16]<br>VCCPRIM_CNV_HVLDO_1P05 | |
| 1.24 | VCCDPHY_1P24[3] | VCCLDOSRAM_IN_1P24[2] | Pins are used for decap only. Connect a 4.7uF cap close to VCCDPHY_1P24 pins and short between VCCLDOSRAM_IN_1P24[2]<br>and VCCDPHY_1P24[3] |
| 3.3 (PCH) | Platform VR | VCCPHVLDO_3P3[1] | For the internal 1.8V configuration only. |

### 42.4.9 CNVi Power-up Sequence

During platform power up the PCH performs a hardware auto-detect handshake to detect the presence of a CRF in the system. From PCH perspective there can be a CRF in the system, or there can be no CRF, in which case Wi-Fi* and Bluetooth are supported by a discrete connectivity module.

The following signals are involved in the CNVi auto detect sequence:

- CRF power supply- 3.3V power pin of the connectivity module (either CRF or discrete)
- RSMRST#- platform global resume reset signal
- CNV_RF_RESET#- GPIO used as a reset for CRF modules (output from PCH)
- CNV_RGI_DT- GPIO used as a strap to detect the CRF present and as a control bus for CNVi (PCH strap and output from PCH)
- MODEM_CLKREQ- GPIO used to activate/deactivate the CRF reference clock (output of PCH)
- 38.4 MHz clock- the CRF reference clock (input to PCH)

The auto-detect is based on the CNV_RGI_DT signal which is initially controlled by the CRF and sampled as a PCH strap during power up.

Inside the CRF chip, the CNV_RGI_DT is actively pulled low (with an approximate strength of 1K ohm to ground). This pull-down is only valid when the CRF power is up and stable therefore it is required that the 3.3V power to the connectivity module will ramp up before any auto-detect sequence starts.

The PCH straps are sampled immediately after the de-assertion of RSMRSET#.

- If the system has a CRF, the value sampled into the strap will be the CNV_RGI_DT pulled to zero. In this case once the straps are sampled they are locked and the PCH HW will be configured for CNVi mode until it is shut down.
- Once CNVi HW is configured in the PCH the CNV_RF_RESET# is de-asserted which causes the CRF to de-activate the 1K pull down of CNV_RGI_DT. The CNV_RGI_DT

GPIO pin defaults to an output of the PCH to become the RGI bus and is set to logical high (which is the CNV_RGI_DT value at rest).

- As part of the CNVi internal boot, the clock request is asserted by the PCH and the CRF clock starts toggling at a frequency of 38.4Mhz. At this point the CNVi initial handshake completes.

During the first point above, if the CRF does not exist, the CNV_RGI_DT value will be driven by on-die or platform pull up resistors (typical 20K). In this case the strap will sample a logical high and the rest of the handshake process will not be performed.

**Figure 42-12.CNVi Power up Sequence**

## 42.4.10 CNVi Platform Connections

### 42.4.10.1 Jumper-less Hybrid Key-E Routing on Motherboard

**Figure 42-13.Jumper-less Hybrid Key-E Routing Scheme**

### 42.4.10.2 Connectivity Integration (CNVi) BRI/RGI

The BRI and RGI can operate at Slow speed (4.8Mbps) and at Full Speed (76.8Mbps). Only at power up the bus will operate at 4.8Mbits/sec, and after very short time it switches to full speed. The switching is self-configured by the CNVi hardware.

The BRI and RGI data is over-sampled by a factor of 8 in Slow speed (De-serializer runs at 38.4MHz clock) and by a factor of 8.125 in Full Speed (De-serializer runs at 624MHz clock) in the CNVi CRF module side, and 8.333 in the PCH (Pulsar) side. Both interfaces operate either in Slow or Full Speed at any given time (no mixed mode).

#### 42.4.10.3 Tools for Analysis

BRI and RGI design can be simulated using single-ended trace model to ensure proper signal integrity for the maximum signal bandwidth.

#### 42.4.10.4 Tools for Debug

BRI and RGI can be tested with the CNVio tool or with the EMT tool. This tool will test the design margins and can detect bus errors as well as very marginal signal integrity.

### 42.4.11 USB 2.0 Port for Bluetooth

The USB port used for Bluetooth is the same whether CNVi or discrete connectivity is used. For CNVi the USB connection is internal to the SoC and there is no USB PHY or external bus required. For discrete connectivity the Bluetooth is connected through the USB pins. In both cases, the same USB port number is used. The USB port number used for Bluetooth in PCH-LP is port 10 and in PCH-H it is port 14.

## 42.5 CNVio Bus

The CNVio signals connects between the CRF RF companion module and the SoC. They are used as the main data bus for Wi-Fi* to transfer data between the PCH (Pulsar) and the RF companion chip. The CNVio signals electrical characteristics are similar to the DPHY standard. The CNVio protocol used for this bus is proprietary.

CNVio signal specifications are documented in the MIPI-DPHY rev1.1 standard specification (see chapter 7 of the MIPI-DPHY rev1.1 standard revision 1.1: Interconnect and Lane Configuration

The CNVio bus is source synchronous where each lane has data carried over a differential pair, and each direction may have multiple lanes and a single clock driven by the source.

The CNVio has 2 lanes in each direction, which supports the following bit rates: (per lane)

- 1.28Gbits/sec (with a clock rate of 640Mhz)

### 42.5.1 Routing Guidelines for CNVio

The CNVio signals connects between the RF companion module and the SoC. They are used as the main data bus for Wi-Fi* to transfer data between the Pulsar and the RF companion chip. The CNVio signals are physically compliant to MIPI-DPHY rev1.1 standard, but have a different (and Intel proprietary) protocol.

We recommend that the design be fully comply with the CNVio routing signal requirements. These requirements are well documented in the CNVio standard specification (see chapter 7 of the MIPI-DPHY rev1.1 standard: Interconnect and Lane Configuration)

The CNVio bus is source synchronous where each lane has data carried over a differential pair, and each direction may have multiple lanes and a single clock driven by the source.

### 42.5.1.1 Routing

The 2 traces of each lane must be routed as matched as possible. Moreover, since the CNVio uses one clock signal for 2 lanes in each direction, there should also be a good delay matching between the two data lanes and the clock. There are no special delay matching requirements between lanes on opposite directions.

**Table 42-8. CNVio Recommended Routing Parameters**

| Parameter | Value | Comment |
|---|---|---|
| Differential pair length matching: | • Within same layer mismatch:± 10mils (0.254mm)<br>• Total length mismatch:±15mils (0.381mm) | This parameters may effect EMI and RFI |
| Characteristic impedance | 85 ohm differential | 50 Ohm to ground for each trace |
| Maximum length | 10 inch | ***Notes:*** The "Maximum Length" considerations for different CNVi solution:<br>• Connector based M.2 – (M1+M2+M3+M4)<br>• Solder down M.2 – (M1+M2+M3) |
| Maximum resistance | 5 ohm | 50 ohm to ground for each trace |
| Shielding | Stripline | Recommended for minimizing EMI/RFI |
| Delay matching between pairs of the same direction | Better than 80 mil | Including the 2 lanes and the clock in every direction |
| Vias | Avoid | Recommended to avoid Via connections as much as possible |
| BER | 1E-12 | Standard PHY bit error rate for a CNVio lane |

### 42.5.1.2 CNVio M.2 Topology

**Figure 42-14.CNVio M.2 Topology Diagram**

## Table 42-9. CNVio M.2 Topology Values

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | 3 | 12.7 | 254.00 | 500.00 | 10000.00 |
| M1 | MS/SL/DSL | VSS | | 213 | | 8385.80 | |
| M2 | MS/SL/DSL | VSS | | | | | |
| M3 | MS | VSS | | 2.5 | | 98.20 | |
| M4 | MS | VSS | | 25.4 | | 1000.00 | |

***Notes:***
1. Number of vias: 2 vias from BO to main Route to device and 1 via underneath the BGA to breakout.
2. Reference Plane: Continuous Ground.

## Figure 42-15.CNVio Device down Topology Diagram

## Table 42-10. CNVio Device Down Topology Values

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | 3 | 12.7 | 254.00 | 500.00 | 10000.00 |
| M1 | MS/SL/DSL | VSS | | 215.9 | | 8500.00 | |
| M2 | MS/SL/DSL | VSS | | | | | |
| M3 | MS | VSS | | 25.4 | | 1000.00 | |

***Notes:***

1. RCOMP Rdc on motherboard is < 0.5ohm.

2. 150 ohm +/-1 % RCOMP on motherboard. The RCOMP signals should be referenced to VSS. Noisy or switching references should be avoided. As board space allows, it is recommended to add a VSS shield at least 4 mils wide placed between RCOMP and adjacent I/O.

3. Continuous GND referencing is preferred for both the topologies. Power plane referencing is also allowed.

**Table 42-11. Topology Guidelines**

| General Guidelines | Value |
|---|---|
| Number of vias allowed | 3 |
| Reference Plane | Continuous Ground Only |

**Table 42-12. General Guidelines**

| General Guidelines | Value |
|---|---|
| Length Matching between P and N within a diff. pair | Within same layer mismatch:± 10mils (0.254mm)<br>Total length mismatch:±15mils (0.381mm) |
| Length matching between Data to CLK lane (board) | < 50 mils (1.27mm) |

## 42.5.2 Tools for Analysis

CNVio design can be simulated using differential trace model to ensure proper signal integrity for the maximum signal bandwidth.

## 42.5.3 Tools for Debug

CNVio can be tested with the CNVio test tool or with the EMT tool. This tool will test the design marginality and can detect bus errors as well as very marginal signal integrity.

## 42.5.4 CNVio Probing

It is recommended to avoid adding any probing pads or test points to the CNVio traces. However in cases where probing the CNVio bus is needed it is recommended to use a special soft touch probe. A special CNVio analyzer U4421A from Agilent (Keysight) can be used with a special cable and retention module. When designing for using this probing set, the probe footprint is inserted within the CNVio traces while allowing the traces to maintain good impedance characteristics. An illustration of the probe and cable setup is shown in figure below.

**Figure 42-16.CNVio Probing Components**

## 42.5.5 Routing Guidelines for BRI/RGI

These are GPIO signals (1.8V) running between the SoC and the RF companion module. The BRI and RGI signals share the same traces as UART signals (for discrete). Since the UART baud rate is expected to be lower than the BRI/RGI toggle rate it can be assumed the BRI/RGI sets the requirements for this bus.

BRI and RGI are 2 bi-directional busses. These signals have slew-rate controlled I/O's on both ends (SoC and RF companion) which should be optimized to minimize EMI/RFI while maintaining good signal waveform. No special control impedance is needed.

The BRI and RGI packets are ECC protected and with standard routing and signal integrity practices applied, no errors are expected to be noticed on the busses.

### 42.5.5.1 CNVi BRI & RGI Single Load

**Figure 42-17.CNVi BRI & RGI Single Load (DT) Topology Diagram**

## Table 42-13. CNVi BRI & RGI Single Load (DT) Topology Values

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | N/A | 12.7 | 253.7 | 500.00 | 9988.19 |
| M1 | MS | VSS | N/A | 12.7 | | 500.00 | |
| M2 | MS/SL/DSL | VSS | N/A | 228.3 | | 8988.19 | |

***Notes:***
1. This topology relates to CNV_BRI/RGI_DT signal.
2. Frequency Support: The design guidelines support up to 38.4MHz.
3. Resistor R1 Spec: 33 Ohm, to be placed close to the PCH.
4. Number of vias allowed: 7.

## Figure 42-18. CNVi BRI & RGI Single Load (RSP) Topology Diagram

## Table 42-14. CNVi BRI & RGI Single Load (RSP) Topology Values

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO | MS/SL/DSL | VSS | N/A | 12.7 | 253.7 | 500.00 | 9988.19 |
| M1 | MS/SL/DSL | VSS | N/A | 228.3 | | 8988.19 | |
| M2 | MS | VSS | N/A | 12.7 | | 500.00 | |

***Notes:***
1. This topology relates to CNV_BRI/RGI_RSP signal.
2. Frequency Support: The design guidelines support up to 38.4MHz.
3. Resistor R1 Spec: 22 Ohm, to be placed close to the connector.
4. Number of vias allowed: 7.

## Table 42-15. General Guidelines

| General Guidelines | Value |
|---|---|
| Trace spacing between DATA and DATA | 5 mils (0.127mm) |

| General Guidelines | Value |
|---|---|
| Trace spacing between DATA and other signals | 20 mils (0.508mm) |

### 42.5.5.2 Routing Guidelines for RefClk

RefCLK is a 38.4MHz clock signal which is generated by the RF companion module and sent to the SoC. This clock can be used as the SoC main clock (in clock sharing configuration) or as the Pulsar clock (in non-clock sharing configuration). When using the latter option, the SoC should have another clock for its operation, but Pulsar (within the SoC) will always get the 38.4MHz clock coming from the CRF.

The clock signal is 1V nominal, 10Kohm typical resistive load with 35pF load capacitance.

It is recommended to rout the clock with special care while maintaining clock routing practices, preferably as a microstrip to minimize EMI/RFI and susceptibility to noise.

### 42.5.5.3 Jefferson Peak Crystal Input to CFL Topology Routing Guidelines

**Figure 42-19. Jefferson Peak Crystal Input to CFL Topology Diagram**

**Table 42-16. Jefferson Peak Crystal Input to CFL Topology Values**

| Segment | Tline Type | Reference | Via Count | Max Length, mm | | Max Length, Mils | |
|---|---|---|---|---|---|---|---|
| | | | | Segment | Total | Segment | Total |
| BO or BI | MS/SL/DSL | VSS | 1* | 12.7 | 254 | 500 | 10000 |
| MR | MS/SL/DSL | VSS | 1* | NA | | NA | |

**Table 42-17. External Topology Guidelines**

| External Topology Guidelines | Value |
|---|---|
| GND shielding | GND shielding to adjacent signals (especially high speed IO) is recommended |
| Number of vias allowed | Max 2 vias - recommended to minimize number of vias |
| Reference plane | Continuous Ground Only; may not reference power planes if routing in stripline or dual stripline, both top and/or bottom reference / adjacent planes MUST be solid continuous ground. Avoid routing directly parallel (under /over) to high current power planes. If unavoidable route signal orthogonal to power plane |

## 42.5.6 Modem Coexistence 3-way UART Connection

In order to allow a "Hybrid Key-E" scheme supporting both connectivity and a cellular modem, there is a need to connect the modem coexistence bus in a configuration that will allow the modem to connect to the connectivity coexistence control logic.

In Intel connectivity modules this logic may reside in the M.2 module or in the SoC, depending on whether CNVi or discrete solutions are used:

- For CNVi, the logic resides in Pulsar
- For discrete M.2 cards, this logic resides in the module

As a result, when a motherboard design contains a modem, and it is desired to be able to support CNVi and discrete on the same M.2 socket, there is a need to have a 3-way connection of the board as shown in figure 17.

One can simplify the routing by adding a jumper resistor to select between the two configurations however this will result in losing the option to swap between CNVi and Discrete on the board. Any such swapping will then require board HW change for changing the jumper resistor position.

Note that when doing this 3-way connection between SoC, M.2 and the Modem there will always be an unused signal which is not optimally terminated for that connection. This signal is shown in red in figure below. The effect of this signal is similar to a stub which adds undesired impedance change to the trace. The effect of this stub on the UART bus depends on several system parameters, distance between the different UART pins, UART bus speed and electrical characteristics of the UART drivers and receivers (referenced to the signal pins). This effect must be considered and analyzed through design practices or simulations to ensure signal integrity is not compromised. For this analysis, the UART baud rate shall be assumed not higher than 4Mbaud.

**Figure 42-20.Coex UART for Connectivity/Modem in 3-way Configuration**

## 42.5.7 SoC Termination Requirements

Due to special power up sequencing of the CRF and I/O requirements the SoC I/O shall be terminated according to the following considerations:

The 38.4 MHz clock from CRF to the SoC has an I/O buffer which is not powered when the CRF is initially powered up. The supply to this buffer will only come up following the first clock request from the SoC. To avoid floating input at the SoC clock pin it is recommended to add a weak **pull down** resistor to the SoC pin. The resistor value shall be 10K ohm and it should be located close to the SoC pin. When adding this resistor the design should be checked to ensure it does not distort the clock signal.

The BRI_RSP and RGI_RSP signals from CRF to the SoC have I/O buffers which are not powered when the CRF is initially powered up. The supply to these buffers will only come up following the first clock request from the SoC. To avoid floating input at the I/O pin it is recommended to add a weak **pull up** resistor to the SoC pin with a recommended value of 20K ohm.

The **CNV_RF_RESET#** signal from the SoC to CRF is used as the main reset signal to the CRF during boot. This signal must have a stable value starting from initial power up of the platform and before the CRF power comes up. To ensure that the CNV_RF_RESET# signal is glitch free it is recommended that a **pull down** resistor be connected between the SoC pin and ground. A 75K ohm resistor to ground will ensure the stability of the signal. Since CNV_RF_RESET# is normally held at 1.8V it is expected to consume negligible amount of power (about 43uW continuously).

## 42.5.8 RF Companion Specifications

The electrical specifications of the JfP chip can be found in the JfP Electrical Spec document (RDC#567240)

# 42.6 Standard M.2 Connectivity Design Considerations

## 42.6.1 Standard (Discrete) Connectivity Guidelines

The Coffee Lake platform supports both Integrated (CNVi) and Discrete (Standard M.2) connectivity modules on the M.2 socket. These are the guidelines for using the standard M.2 Wi-Fi*/Bluetooth combo modules.

#### 42.6.1.1 PCIe

- PCIe is the standard M.2 interface for Wi-Fi*.
- PESRT# and PEWAKE# are used for D3 flows it is possible to share these signal with other system components.
  - PEWAKE # signal cannot be shared with other PCIe devices since it is used by a specific device.
  - PERST# signal can be shared. As example Wi-Fi* PERST# can be connected to a platform global PCIe reset signal.
  - Connected standby flows are using RTD3hot. RTD3hot is not using PERST#, and not using PEWAKE#
  - Non-connected standby flows are using D3cold. D3cold is using PERST# and PEWAKE#.
- In S3-5 the platform puts all the devices to D3cold, and will assert PERST# to all of them, as a result PERST# can be shared.
- Wi-Fi* core can still be kept active in D3, but in that case, since it is D3cold, Wi-Fi* will ignore PERST# even if it puts Wi-Fi* into PCIe reset.
- Wi-Fi* core can wake the system using PEWAKE# and there is added value in non-CS platforms to have dedicated PEWAKE# signals, but it is not mandatory.
- To conclude, even in non-connected standby flows the signals can be shared.

#### 42.6.1.2 Connectivity Module Power Control

The platform designer has the following options to control the power rail of the connectivity module:

- **Recommended option (and a must for CNVi support):** Connect directly to a non-switched 3.3V rail. This is the only possible option when the design should also support CNVi.
  - The device will be on as long as the rail provides power.
  - The OEM can save the need to use power switch, but keep connectivity module leakage in the relevant platform states.
- **Optional (not valid for CNVi or dual discrete/CNVi support):** Connect to a 3.3V rail through power switch.
  - Control the switch using SLP_WLAN controlling signal.
  - The SLP_WLAN signal will keep the connectivity awake when needed, and turn it off when not needed.
  - For example, if ME in Sx is not used, and wake on WLAN in Sx is not used, then connectivity can be turned off.

#### 42.6.1.3 Power Feed

It is required to have decoupling caps on the power feeds in each end of the connector.

10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.

10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

## 42.6.2 PCIe Host Interface Errata

This section includes several important implementation aspects about PCIe host interface. The platform designer should take these items into account as part of the platform design.

### 42.6.2.1 Squelch Detect Mechanism

The Squelch (SQ) detect mechanism may not consistently identify PCH wake signaling (TS1 symbols) as valid above SQ Max threshold of 175 mV, as defined in the PCIe spec.

It is important to follow proper platform design and layout guidelines as defined in the PCIe CEM specification to ensure PCH wake signaling (Electrical Idle Detect Threshold - *Vrx-idle-det-diff-p-p* parameter) in the range of:

- 65 mV to 280 mV

Customers should design/plan appropriately for all adapters that may be used in a given platform.

### 42.6.2.2 Common Clock Configuration

PCIe on both platform side (PCH) and WLAN side must operate using common clock configuration. Both PCH and WLAN are configured for this by default (bit 6 is set in registers 0x50 and 0xF0). From hardware perspective, the same reference clock (Refclk) must be used for both PCH and Wi-Fi* card, as shown in Figure below.

**Figure 42-21.PCIe Common Clock Configuration**

**Source**: *PCI Express* Rev 2.0 spec (PCI_Express_Base_Rev_2.0_20Dec06a, figure 4-50)

### 42.6.2.3 Enabling PCIe Controllers with ASPM

ASPM defines the L states of the PCIe connections, L0, L0s, L1 and L2.

The device supports L1 state, and does not support L0s. This is in order to benefit from the power saving that is achieved with L1 state, while avoiding platform integration complexity which is involved with using L0s state.

The device supports ASPM optionality ECN, allowing support of L1 without L0s. Therefore, there is no need for special BIOS actions as with previous Intel's wireless products.

### 42.6.2.4 CLKREQ# Timing

Latest PCIe M.2 Specification does not specify a constraint on when PCIe device should assert CLKREQ# after Power Valid (which is a point where the V3.3 rail reached nominal level).

Refer to the below timing diagram and timing tables taken from PCIe M.2 specification and as can be seen, CLKREQ# assertion timing is not defined.

**Figure 42-22.PCIe CLKREQ# Timing**

**Source:** M.2 specification

**Table 42-18.Power-up CLKREQ# Timing**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{PVPGL}$ | Power valid to PERST# Input active | Implementation specific | | ms |
| $T_{PERST\#-CLK}$ | REFCLK stable before PERST# inactive | 100 | | µs |

Cyclone peak, Thunder Peak and Windstorm peak asserts CLKREQ# within 12ms from Power valid as shown in below figure, these devices complies with the requirement to enter DETECT within 20ms of PERST# de-assertion.

***Note:*** Refer to M.2 device specification to meet the POWER rail to PERST# timing requirements

The PERST# signal rise time needs to meet the limitations listed in below table. This guarantees robust out-of-reset flow of the device and better immunity to noise that can be carried by this signal. In addition, it is required that this signal rise in a monotonic way and avoid a step-like rise.

### Table 42-19. Power-up PERST# Timing

| PERST# Rise Time | | |
|---|---|---|
| Parameter | Intel® Wireless Devices | |
| | Stone Peak<br>Sandy Peak | Snowfield Peak<br>Windstorm Peak<br>Thunder Peak<br>Cyclone Peak |
| PERST# Rise Time | < 20 nSec Monotonic rise | < 150 nSec Monotonic rise |
| PERST# Ripple/Glitch During Rise Time | < 50 mV glitch during the rise rime phase | < 100 mV glitch during the rise rime phase |

§ §

# 43 Wireless Modules and Antenna Design Guidelines

## 43.1 Antenna Design Guidelines

A broad range of wireless modules are available suited to different regulatory, performance, and user requirements. This chapter shall discuss the considerations for antenna integration in Coffee Lake processor designs including, but not limited to, antenna performance, placement options, and RF system-level integration.

The Coffee Lake processor may support radios for:

- Wi-Fi (WLAN)
- Bluetooth* (BT)
- GNSS
- WWAN

### 43.1.1 Antenna Integration

The successful antenna integration on the system is determined through three prime objectives:

1. Ensure good individual antenna efficiency in the frequency bands supported by the respective modem, for all antennas and all modes of operation.
2. Ensure adequate isolation between antennas to:
   a. Minimize the spatial correlation and mutual coupling between antennas for radios supporting MIMO or diversity, and maximize the benefit that can be derived from the additional transceiver chain.
   b. Enable the simultaneous operation use-case scenario of multiple radios (co-existence) to be supported without any potential performance degradation. Co-existence of multiple wireless modules and their antennas can become a major problem if not considered in the initial stages of design.
3. Minimize the platform noise coupling into each antenna (in-band noise) which may potentially impact the radio's receiver performance.

### 43.1.2 Antenna Performance

The individual antenna performance can be characterized by the frequency coverage, efficiency, and peak gain. The isolation between antennas is defined by the $S_{21}$ as measured from the antenna ports on a network analyzer. For radios supporting MIMO or diversity, the MIMO antennas will need to meet the recommended gain imbalance and envelope correlation coefficient limits.

The envelope correlation coefficient can be expressed in the following methods depending on the available figures of merit:

1. With the far-field complex antenna radiation patterns, which can be measured in antenna test chambers, the envelope correlation coefficient can be evaluated with the following formula:

$$\rho_e = \frac{\left|\int_0^{2\pi}\int_0^{\pi}\left(XPR\bullet F_{\theta 1}(\theta,\phi)F^*_{\theta 2}(\theta,\phi)P_\theta(\theta,\phi)+F_{\phi 1}(\theta,\phi)F^*_{\phi 2}(\theta,\phi)P_\phi(\theta,\phi)\right)\sin(\theta)\,d\theta d\phi\right|^2}{\int_0^{2\pi}\int_0^{\pi}\left(XPR\bullet\left|F_{\theta 1}(\theta,\phi)\right|^2 P_\theta(\theta,\phi)+\left|F_{\phi 1}(\theta,\phi)\right|^2 P_\phi(\theta,\phi)\right)\sin(\theta)\,d\theta d\phi\bullet\left|\int_0^{2\pi}\int_0^{\pi}\left(XPR\bullet\left|F_{\theta 2}(\theta,\phi)\right|^2 P_\theta(\theta,\phi)+\left|F_{\phi 2}(\theta,\phi)\right|^2 P_\phi(\theta,\phi)\right)\sin(\theta)\,d\theta d\phi\right|}$$

   where $\rho_e$ is the envelope correlation coefficient, $F_1$ and $F_2$ are the complex vector field strengths of antenna 1 and 2 respectively, *XPR* is the cross-polarization ratio, and *P* is the incident field distribution function.

2. In the case where the complex antenna radiation pattern cannot be obtained, an alternative method, which requires the S-parameters and the individual radiation efficiencies, can be utilized to determine the correlation coefficient in the following formula:

$$\rho = \frac{-S_{11}S^*_{12} - S_{21}S^*_{22}}{\sqrt{(1-|S_{11}|^2-|S_{21}|^2)(1-|S_{22}|^2-|S_{12}|^2)\eta_1\eta_2}}.$$

   where $\rho$ is the envelope correlation coefficient, $S_{11}$, $S_{12}$, $S_{21}$, $S_{22}$ are the S-parameters of the two port antenna system measured on a network analyzer, $S_{12}$* is the complex conjugate of $S_{12}$, and $\eta_1$ and $\eta_2$ are the antenna radiation efficiencies measured with the unused antenna port terminated with a 50 ohm load.

3. In the case where only the S-parameters are available, the envelope correlation coefficient can be estimated with the following formula:

$$\rho_e = \frac{\left|S^*_{11}S_{12}+S^*_{21}S_{22}\right|^2}{(1-|S_{11}|^2-|S_{21}|^2)(1-|S_{22}|^2-|S_{12}|^2)}$$

The envelope correlation coefficient calculation methods shown above are described in the following papers:

- *Ying et al.; "Characterization of multi-channel antenna performance for mobile terminal by using near field and far field parameters," COST 273 TD(04)(095), Goteborg, Sweden, 2004.*
- *Hallbjorner, P.; "The significance of radiation efficiencies when using S-parameters to calculate the received signal correlation from two antennas," Antennas and Wireless Propagation Letters, IEEE, vol.4, no., pp. 97- 99, 2005*

The following tables summarize the antenna performance recommendations for each wireless system, the isolation recommendations, and the recommendations for different modes of operation.

## Table 43-1. Antenna Performance Recommendations

| Antenna | Frequency GHz | Type | Max Size of Antenna Element mm | Efficiency[1] dB | Peak Gain dBi | MIMO Metrics |
|---|---|---|---|---|---|---|
| WLAN | 2.40-2.49<br>5.15-5.85 | PIFA/ Slot | 35x8x1 | -3.9 (2.4G)<br>-4.4 (5G) | <2 (2.4G)<br><3.5 (5G) | Correlation Coefficient < 0.3,<br>Gain imbalance < 1 dB |
| Bluetooth* | 2.40-2.49 | PIFA/ Chip | 35x8x1 | -3.9 | <3 | N/A |
| GNSS[2] | 1.56-1.61 | PIFA | 15x5x2 | -3.5 | <2 | N/A |
| WWAN M.2 HSPA (2G, 3G) | 0.82-0.96<br>1.71-2.17 | PIFA | 75x13x2 | -4 (f<1GHz)<br>-3 (f>1GHz) | <2 | Correlation Coefficient:<br>-> ecc < 0.5 (f < 1GHz)<br>-> ecc < 0.4 (f > 1GHz)<br>Gain imbalance < 1 dB |
| WWAN M.2 LTE (2G, 3G, LTE) | 0.70-0.96<br>1.42-1.51<br>1.71-2.17<br>2.30-2.36<br>2.50-2.70<br>GNSS[2] | PIFA | 75x13x2 | -3.5 (f<1.6GHz)<br>-3 (f>1.6GHz) | <2 | Correlation Coefficient:<br>-> ecc < 0.5 (f < 1.6GHz)<br>-> ecc < 0.4 (f > 1.6GHz)<br>Gain imbalance < 1 dB |

[1] Cable length is assumed to be 600 mm (1.13 mm OD coax) for the antenna efficiency targets. Actual cable length will vary based upon the chassis.

[2] GNSS (i.e. GPS, GLONASS) antenna is usually expected to be shared with WWAN Aux antenna. It is also possible that GNSS antenna for non WWAN SKUs is either discrete or shared with WLAN antenna. In either case, the efficiency numbers listed above are recommended.

## Table 43-2. Isolation Recommendations

| Antenna Ports | Wi-Fi | Bluetooth* | GNSS | WWAN/LTE |
|---|---|---|---|---|
| **Wi-Fi** | 25 dB nominal | 25 dB nominal[1]<br>(15 dB min) | 25 dB | 25 dB[2]<br>(15 dB LTE Band7[3]) |
| **Bluetooth*** | 25 dB nominal[1]<br>(15 dB min) | N/A | 25 dB | 25 dB<br>(20 dB LTE Band7[3]) |
| **GNSS** | 25 dB | 25 dB | N/A | shared |
| **WWAN/LTE** | 25 dB<br>(15 dB LTE Band7) | 25 dB<br>(20 dB LTE Band7[3]) | (shared) | 25 dB |

[1] BT-Wi-Fi isolation translates to Wi-Fi main to Wi-Fi Aux isolation for the case where BT antenna is shared with Wi-Fi. For best performance, recommended isolation > 35 dB. Nominal performance with limited degradation can be seen with isolation > 25dB. Co-existence solution allows functionality down to 15 dB isolation with reduced performance.

[2]Without LTE band 7 and without a co-existence mechanism between Wi-Fi and WWAN modules, 30 dB isolation is the best, but 25 dB is acceptable as indicated shown above

[3]Without a coexistence scheme between WLAN and WWAN, additional filtering at both WWAN and WLAN modules is required to operate at 15 dB isolation. Careful consideration of the total system solution is required for this case

## Table 43-3. Recommendations for Different Modes of Operation

| Description of Lid Mode | Clamshell (Open Lid) | Tablet | Closed Lid |
|---|---|---|---|
| Antenna performance recommendations | As in Table 43-1 | As in Table 43-1 | 3 dB lower than values in Table 43-1 |

### 43.1.3 Antenna Placement

The following must be considered when deciding the placement of antennas:

- **Modes of Operation:** For devices which enable different modes of operation (i.e. Clamshell, Tablet, and Closed Lid), careful consideration of the environment around the antenna in each configuration while deciding the antenna placement is necessary to deliver the desired user experience in all modes of operation.
- **Keep-Out-Zone (KOZ):** A metal-free KOZ is typically required to integrate the antenna in traditional designs. The physical size of the antenna will depend on the target frequencies, bandwidth, and performance requirements of the antenna. Antennas with larger geometric footprints tend to provide better performance. The non-metallic materials (i.e. plastics) also need to be assessed since different materials properties may have different effects to the antenna characteristics.
- **Lossy Structures:** Separation of the antenna radiation elements from lossy structures, such as the LCD enclosure, will provide better bandwidth. The separation required for WWAN is higher than that required for Wi-Fi. In general, lower operational frequencies require larger separation compared to higher operational frequencies. Also, larger bandwidth considerations require larger separation from nearby metallic structures. For WiGig, this separation is crucial and more details can be obtained from Section 9.5 WIGIG Product Guidelines.
- **Grounding:** Unbalanced antennas require a ground reference, which is typically the chassis or the back of the display. The size of the ground reference needs to be considered as part of the antenna design.
- **Cable Routing:** Each antenna will require a coaxial cable to connect to the radio module's RF port. Cable routing that avoids regions with noise and minimizes cable lengths is recommended to minimize the platform noise impact and cable loss. In the case where the module is in the base and the antenna is in the display, the coaxial cable will need to be fed through the hinges. The size of the mechanical hinge places a restriction on the number of cables that can be fed through and the diameter of the cables. Typical RF coax cables can range in outer diameter (OD) from 0.81 mm to 1.37 mm; however, the RF connector receptacle defined by the M.2 module specification will only accept mated plugs with either 0.81 mm OD cables or 1.13 mm OD cables. Refer the respective radio module's product description for the RF connector type.
- **Cable Loss:** Coaxial cables will introduce an insertion loss depending on the diameter, length, and frequency of interest. Thicker coaxial cables tends to be less lossy while being more expensive compared to thinner cables. Lower loss cables are also available from vendors which will reduce the total cable loss especially for long cables. Double shielded cables are useful in ensuring that radio module sensitivity degradation is limited due to the cable picking up platform noise when routed through the platform.
- **RF Exposure (SAR):** Regulatory bodies, such as FCC and CE, define detailed requirements for the allowable RF exposure for devices which generate RF electromagnetic fields. Specific Absorption Rate (SAR) is a measure of the rate in which energy is absorbed in body tissue due to EM energy from an antenna. and is a prime consideration for placement of antennas, especially for higher power radios such as WWAN. For WiGig, the Maximum Permissible Exposure (MPE) is used to determine the RF exposure limit of the radio implementation. In general, the antennas should be located in areas which will not be in close proximity to the human body in any mode of operation. Refer to the published guidance from FCC for more details on the RF exposure requirements.

- **Isolation between antenna ports:** To improve the isolation between antennas, the following methods can be employed which include, but is not limited to:
  i. Spatial diversity - larger spatial separation between antennas is one way of increasing the isolation between ports of radio modules that operate in bands that are close to one another.
  ii. Polarization diversity - in some instances where the antennas have polarization discrimination, the relative orientation of the antennas can be used to improve isolation and enhance performance.
- **Platform Noise:** Various components in the system, such as display/touch circuits, memory, PLLs, cameras, clocks, USB/HDMI ports, and other high speed IO, may generate noise which can couple to the antennas and/or coax cables and thus degrade the wireless radio's receiver performance. Careful consideration needs to be employed with respect to antenna placement and cable routing to avoid these noise sources and minimize the platform noise impact to the receivers. With detachable tablets and convertible notebooks, the proximity of the antenna to the base components needs to be especially considered during the initial floor planning.
  — Internal studies have found that 3D cameras, which utilize the USB3 interface to communicate with the motherboard, is a source of broadband RF noise which may impact the antennas in the vicinity. The camera noise may impact the radio's receiver performance through the antenna in two ways:
  i. Conducted noise which flows from the camera through the shared ground plane (chassis) and in to the antenna through the antenna ground connection. To reduce the noise coupled in to antenna, the ground plane should be manipulated to re-direct the current flow from the camera away from the antenna.
  ii. Radiated noise from the 3D camera interface (especially the USB3 connector), may couple to the antenna and hence desensitize the radio receiver. In general, the antennas should be separated from the 3D camera and USB3 bus to avoid any degradation to the radio's receiver performance. Studies have shown that the antenna should be at least 15 mm away from the USB3 connector for minimal impact to WWAN and Wi-Fi radios. Shielding of the camera and USB3 connector is also recommended.

#### 43.1.3.1 Antenna Placement Options for Multi-Mode Devices

Two potential antenna placement options are shown in the figures below for clamshells or multi-mode devices such convertibles and detachable Ultrabook™. The target form factor is a 14.1 inch (3581.4 mm) notebook, but it is not limited to this size. Additional consideration will need to be applied to the RF clearance in the base around the antennas for multi-mode devices when in Tablet or Lid-Closed modes.

The module selection includes support for 2x2 MIMO Wi-Fi/BT, and 1x2 WWAN. GNSS is assumed to be combined with WWAN Aux antenna (AGPS/GPS).

**Figure 43-1. Antenna Placement Option 1**

**Figure 43-2. Antenna Placement Option 2**

### 43.1.3.2 Antenna Placement in Metallic Chassis

Many platforms with the U-processor design utilize metal materials for the surface covers, commonly referred to as metallic chassis. The antenna must be placed such that there is sufficient clearance from metal to enable good wireless performance. When there are metal surfaces surrounding the antenna, it is recommended to have plastic sections or insert molded plastic in the metal covers to provide an RF transparent window which will not degrade the antenna performance and thus enable good wireless connectivity in all modes of operation. Other potential options include integrating the antenna on the base (keyboard side) of the platform or utilizing the hinge area. Care should be taken to ensure potential EMI from adjacent I/O connectors do not interfere with the antenna reception.

The following placement options may be considered for Closed Lid mode:

1. **Non-Metallic Chassis/ Metal Chassis with cutouts**: A non-metallic chassis will not cause issues in Closed Lid mode. In the case of a metallic chassis, cutouts may be employed to provide required clearance for the antenna on the A and B-covers. When the lid is closed, the antenna must not rest closer than 5 mm to the EMI coating (or metal) on the C-surface. A suitable plastic cutout, with a recessed EMI shield maybe required to achieve both ESD and EMI protection and good closed lid performance.
2. **Metallic chassis with no cutout on C-surface**: A dielectric loaded antenna maybe placed for Wi-Fi operation on the B-surface, with a cutout on the A-surface. Such a dielectric loaded antenna can operate with a metallic B-surface, which also shields the antenna from the changes introduced by closing the lid. The figure below depicts this solution.

**Figure 43-3. Potential Solution for Metallic Chassis with Lid-Closed Operation**

— Due to the Tent Mode test configuration for convertible notebooks defined by Intel Regulatory, or in the case of a detachable tablet, the antenna on the A-cover is the worst-case for the body SAR requirement in touch condition and will result in significant transmit power reduction for WWAN and possibly even Wi-Fi. (Same applies for detachable tablet notebooks)

3. **Base mounted Wi-Fi antennas:** Antennas can be placed in the hinge area on the base of a metallic chassis notebook, with a plastic cutout near the hinge. The hinge must be such that when the lid closes, the area in the base where the antennas are housed is not shielded completely by the lid. Special consideration must be given to maximizing the separation between the antenna and the human body below the D-surface to pass SAR requirements with low-risk. Platform noise pickup from base mounted antennas needs to be measured before committing to a particular location as there is a higher risk of impact from platform noise due to the closer proximity of the antennas to the motherboard.
4. **Slot antennas cut into the chassis:** Slots can be cut into the A-surface of the antenna, near the apex of the lid and the cutout can be covered with plastic inserts. Such an antenna would be integrated into the chassis and special care must be given to the feeding mechanism, especially when materials not amenable to soldering such as aluminum are used. Multiple antenna SKUs and/or revisions will imply multiple chassis SKUs and/or revisions, so this option will need to be considered very early in the design cycle.

## 43.1.4 RF System-Level Integration Recommendations

### 43.1.4.1 Wi-Fi

Platforms typically support 2x2 (and some 3x3) MIMO configurations for Wi-Fi. In addition to meeting the efficiency requirements set forth in Table 43-1, some additional system level recommendations are listed in Table 43-4 below.

**Table 43-4. Additional Recommendations for Wi-Fi MIMO Operation**

| | | |
|---|---|---|
| 1 | Difference in Noise coupling into Main and Aux antennas | < 1 dB |
| 2 | Absolute value of noise coupling into Main and Aux antennas | < 3dB de-sense from noise floor |

In addition the antenna specs, the following considerations are brought to attention:

- Modern Standby Support (previously Connected Standby or InstantGo)
  - The platform may need to maintain the Wi-Fi connection while in standby and in any mode of operation such as clamshell, tablet, closed lid, detached, and/or convertible modes. SAR requirements will need to be met and active states must be achievable in each of the above operation modes.
- Specific Absorption Rate (SAR)
  - In situations where the platform cannot meet regulatory RF exposure requirements, the radio module's RF transmit power may need to be reduced.
- In-Device Co-Existence Interface
  - Refer to the WWAN section below for more details on the IDC interface.

### 43.1.4.2 Bluetooth*

A majority of platforms are expected to use the combo Wi-Fi–BT modules. The combo modules implement co-existence schemes which allow for simultaneous operation of Wi-Fi and Bluetooth* with isolation down to 15 dB; however, higher isolation offers better performance and robustness and is recommended as shown in Table 43-2.

If a discrete Bluetooth* module is implemented, the isolation between the BT antenna and each Wi-Fi antenna will need to meet the isolation recommendations in Table 43-2. In platforms where Wi-FI Aux antenna is also shared as the BT antenna, the Wi-Fi to BT isolation becomes the same as Wi-Fi Main to Wi-Fi Aux isolation.

### 43.1.4.3 GNSS

Global Navigation Satellite System (GNSS) includes GPS, GLONASS, Galileo, Beidou, and other regional systems. Two potential integration options (and corresponding antenna choices) are supported for GNSS:

1. GNSS on the WWAN module. The WWAN Aux antenna will be required to support GPS and GLONASS frequency bands as defined in Table 43-1. The module will filter the GNSS signal to the GNSS modem integrated in the module.
2. Discrete GNSS solution: A standalone GNSS antenna is required, which will be connected to the RF front end of the discrete GNSS modem implementation.

### 43.1.4.4 WWAN

Antenna efficiency requirements for WWAN (HSPA or LTE) antennas are listed in Table 43-1. WWAN modules support two antennas (Main and Aux). The WWAN-Main antenna is capable of transmit and receive functions. The WWAN-Aux antenna is a receive-only antenna and is expected to also support the GNSS frequencies.

In addition the antenna specs, the following considerations are brought to attention:

- Modern Standby Support (previously Connected Standby or InstantGo)
  - The platform may need to maintain the WWAN connection while in standby and in any mode of operation such as clamshell, tablet, closed lid, detached, and/or

convertible modes. SAR requirements will need to be met and active states must be achievable in each of the above operation modes.

- Specific Absorption Rate (SAR)
  - In situations where the platform cannot meet regulatory RF exposure requirements, the radio module's RF transmit power may need to be reduced. The WWAN modem has the capability of implementing dynamic power reduction (DPR) with the co-integration of a SAR proximity sensor. SAR proximity sensor pads will need to be implemented around the WWAN transmit antennas (WWAN-Main) and trigger the SAR sensor controller upon detection of the human body to send a signal through GPIO on PCH via SW or directly to the module's DPR pin. Upon receiving the trigger signal, the module will be responsible for reducing the radio's transmit power to levels required to pass the SAR limit.
  - Refer to FCC's documentation for details on RF exposure requirements.
- Tuner and Tunable Antennas:
  - It is recommended that there should be provisions to support antenna tuners with specific antenna and tuner type provided by Intel. Several antenna vendors are offering both tunable and non-tunable (passive) WWAN antennas. The passive antennas are typically easier to integrate but are larger (75 mm x 13 mm x 2 mm for global coverage LTE). The tunable antennas can be potentially smaller in size but require traces from the motherboard/module to be routed to the antenna tuning circuitry, as well as modem support to implement and verify the active tuning intelligence.
  - The Intel WWAN module can control a tuner module by means of 4 GPIO lines from the M.2 module as shown in Table 43-5. Board space for the tuner and additional tuning components and routing space for the power and control signals will need to be taken into account.

### Table 43-5. Intel WWAN Antenna Tuning GPIO Description

| Signal Name | SMARTi Signal | M.2 Connector Pin | Direction (WWAN) |
|---|---|---|---|
| ANTCTL0 | GPO8 | 59 | O |
| ANTCTL1 | REFE_SDATA/GPO13 | 61 | IO |
| ANTCTL2 | REFE_SCLK/GPO14 | 63 | O |
| ANTCTL3 | REFE_VIO/GPO12 | 65 | O |

  - Selection of tuning components is implementation specific and the recommended values are not hard requirements. See table Table 43-6 and Table 43-7 below for M.2 module specifications and recommendations with respect to tuners. Please contact Intel RF support team for additional options.

### Table 43-6. M.2 Module Specifications

| Parameter | Value | Comments |
|---|---|---|
| Voltage | 1.8 V | Applied to both GPO and REFE |
| max source/sink current | -/+ 5 mA | For GPO operation. At max current up to 0.5 V output voltage drop can occur |
| REFE_VIO | 20 mA | Shared between up to 8 slaves at 1.25 mA per slave plus capacitive load |
| REFE version | 1.1 | |
| Maximum REFE frequency | 26 MHz | 13 MHz optional |
| Number of supported tuners | configurable | Please contact Intel RF support team for details |

### Table 43-7. M.2 Module Recommended values for Tuners

| Parameter | Value | Comments |
|---|---|---|
| Switching Time | <50 uS | Switching between states - REFE or GPO controlled switches |
| Tuner boot time | <50 uS | Time between VIO goes high and tuner is ready |
| REFE bus length | REFE 1.1 | According to MIPI specification and depending on capacitive load |

- In-Device Co-Existence Interface
  - It is recommended that platform designs implement two key mechanisms to improve coexistence when integrating Intel Connectivity and WWAN modules with the potential for simultaneous operation.
    i. Maximize the isolation between Wi-Fi and WWAN antennas beyond 15 dB which will ease simultaneous operation (see Table 43-2).
    ii. Implement the In-Device Coexistence interface connection on the system between the Connectivity and WWAN modules to enable the use of the smart co-existence solution. Table 43-8 is an example of how the 3 coexistence signals for the IDC interface should be connected when the Intel Connectivity and WWAN solutions are implemented as modules plugged into M.2 compatible sockets on the platform.

### Table 43-8. In-Device Coexistence Interface

| Intel Coexistence Signal description (Signal Name) | Pin# in Connectivity socket | Signal Direction | Pin# in WWAN socket |
|---|---|---|---|
| IDC_UART_TXD (COEX1) | 48 | ← | 64 |
| IDC_UART_RXD (COEX2) | 46 | → | 62 |
| GNSS_EXT_FTA (COEX3) | 44 | ← | 60 |

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# 44 Platform Telecom Design Guidelines

## 44.1 Safety Rules

Ensure safety compatibility by meeting regulatory requirements. The two standards that are commonly used to evaluate Safety are:

- United States Federal Communication Commission/ Canada UL/CSA 60950-1 Edition (2003)
- European Union, and Mutually Recognizing Countries, International Electro technical Commission's IEC 60950-1 - 1st Edition (2001-10) (with CB certificate) or EN 60950-1: 2001 (with CB certificate) (or 60950-1: 2006) (2006 version required after 1/12/2010)

## 44.2 EMC Rules and Regulations

Ensure Electromagnetic Compatibility (EMC) by meeting regulatory requirements. The two standards that are commonly used to evaluate emissions are:

- United States Federal Communication Commission (FCC) Title 47 CFR, Part 15, Subpart B §15.107, §15.109.
- European Union, and Mutually Recognizing Countries, International Electro technical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 class B limits also known as CISPR22 or EN 55022. The seven standards that are commonly used to evaluate immunity for the European Union and Mutually Recognizing Countries IEC 61000-n-n are described in Chapter 49, “Electromagnetic Compatibility”.

## 44.3 Telecom Safety Considerations

To pass the FCC (Federal Communication Commission) and other regulating agency's Telecom standards, digital system designers have to consider the specific Telecom safety isolation between the TNV (DAA side) and the SELV areas. This isolation is measured under 1000 Volts 1 Amp during 1 minute in USA FCC, 1500 Volts 1 Amp during 1 minute in Europe and 2500 Volts 1 Amp during 1 minute in Australia for specific finger tip detection design.

**Figure 44-1. Telecom Safety Considerations-Generic Block Diagram and Isolation**

To pass the FCC (Federal Communication Commission) and other regulating agency's Telecom standards, digital system designers have to consider the specific Telecom surge test between Tip, ring and Ground (metallic between Tip and Ring and longitudinal between Tip/Ring tied together and Ground). The surge tests are applied up to 1500 Volts for USA FCC, 4000 Volts for International K21 and up to 6000 Volts for some OEM recommendations. The modem/circuit traces must survive after these surges.

**Figure 44-2. Telecom Safety Considerations-Stringent Test in Metallic Mode**

## 44.4 Configuration

The following sections discuss PCB design techniques which must be applied to fulfill the isolation and surge test limits.

### 44.4.1 Isolation

A minimum distance of 106.3 mils (2.7 mm) must be respected between all components of the TNV/DAA area and the SELV area (126 mils (3.2 mm) for the medical equipment and 157.48 mils (4 mm) for Australia for specific finger tip detection design).

**Figure 44-3. Board Level Design Considerations-Isolation**

### 44.4.2 Surge

In the TNV/DAA area a minimum distance of 20.08 mils (0.51 mm) must be respected between the Tip and Ring tracks, the circuit traces connecting the sidactor to the RJ11 shall not be less than 25.2 mil (0.64-mm) wide, no VIA and no tracks in the other intermediate layers can be installed in this area.

**For the following figure, keep in mind that Intel is no longer developing such devices. The use of the following configuration is at the risk of designer (mainly at the OEM level).**

**Figure 44-4. Board Level Design Considerations-Surge (Distances inside TNV)**

## 44.4.3 Example of Wrong Implementation

**Figure 44-5. Board Level Design Considerations-Example of Wrong Implementation**

## 44.5 Additional Guidelines

### Table 44-1. Component Placement Review Checklist

| Item NO. | Description | Y/N |
|---|---|---|
| 1 | Tip and ring EMI/EMC capacitors must be placed as close as possible to the phone connector RJ11. | |
| 2 | Ferrite beads must be placed as close as possible to the phone connector RJ11, must be after the surge protection device (commonly a sidactor). | |
| 3 | All TNV circuits must have a minimum of 106.3 mils (2.7 mm), 126 mils (3.2 mm) for medical, separation from all SELV circuits to meet international safety regulations with some margin (98.43 mils (2.5 mm) is absolute min). However for increased lightning surge protection to greater than 6 kV this clearance should be increased to 157.48 mils (4 mm) or 196.85 mils (5 mm). | |
| 4 | All PCB traces and pads connected to TIP shall have a minimum separation from all traces and pads connected to RING by a minimum distance of 20.08 mils (0.51 mm). This rule represents an absolute minimum requirement applicable to mobile designs such as MDC (very constrained PCB area). Of course, a larger clearance is acceptable and desirable, if the PCB area permits it. | |

### Table 44-2. General Routing Review Checklist

| Item NO. | Description | Y/N |
|---|---|---|
| 1 | Sidactor shall be placed close to the telephone connector RJ11. The circuit traces connecting sidactor to RJ11 shall not be less than 25.2 mils (0.64 mm) wide. This minimum trace width ensures that the traces will survive lightning surge currents during metallic surge events. | |
| 2 | No VIA and no tracks in the other intermediate layers must be installed in the area between the RJ11 and the sidactor. | |

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# 45 Platform Power Sequencing Specification

This chapter provides the following information:

- Platform Power Sequence requirements for the Coffee Lake platforms
- Platform Voltage Rails Status in the different S-States/M-States
- Voltage Rail Sequencing Requirements

## 45.1 PCH_PWROK, SYS_PWROK and Other PWRGD Signal Generation

The power sequencing consists of multiple stages of power state transitions. During each stage, different VRs will be turned on through various control signals from the processor such as the SLP_SUS#, SLP_S4#, and SLP_S3#. In response, the platform will ramp the required voltage rails in the required order and then asserted the various powergood signals required by the processor and other platform components after the necessarily timing requirements have been met.

During G3/DSx-S5 transitions, the platform will need to generate the DSW_PWROK and RSMRST# signals. In this phase of the power up sequence, the DSW and Primary power well voltage rails are ramped to the processor.

During S5-S0 and DSx-S0 transitions, the platform will need to generate the PCH_PWROK and SYS_PWROK signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up. Figure 45-7 shows a high-level representative control signal and the powergood logic diagram for generating the PCH_PWROK and SYS_PWROK signals. This figure shows the recommended power-on sequencing flow steps from SLP_S4# de-assertion until PLTRST# de-assertion for the Coffee Lake platform.

The PCH_PWROK signal is expected to be asserted by the platform to indicate to the processor that all required CPU voltage rails are up and stable and that the processor may continue the boot sequence leading up to PLTRST# de-assertion, such as starting to turn on clocks and ffexecuting other internal pre-reset activities. Not all CPU ails are required to be ramped up by the time PCH_PWROK is asserted, such as some of the IMVP8 based rails like VCC, VCCGT, and VCCGTx, which will be ramped later on in the power sequence. SYS_PWROK is expected to be asserted by the platform to indicate that the system and all of its non-CPU components are ready for PLTRST# de-assertion. During power state transition to S0, the SYS_PWROK signal is the final platform controlled hardware gate before PLTRST# de-assertion. Platform designers may optimize when the SYS_PWROK signal is asserted with respect to the PCH_PWROK signal to help optimize overall boot latency, depending on system and component timing requirements.

## 45.2 Sequencing Interface Signals List and Power Rails

### Figure 45-1. CFL Flow Diagram for SYS_PWROK/PCH_PWROK Generation

***Notes:***

1. Enable inputs may be qualified by other signals and factors not shown.
2. Optional configurations. Different configurations may have impact boot latencies differently.
3. This delay is not explicitly required. For systems supporting traditional PCIe add in cards that require up to 100ms delay from pwr stable to PLTRST# deassertion, the PCH can guarantee a 99ms delay by enabling TPCH33 timing thru soft straps. If more or less time is required, then a specific timing delay circuit may be required
4. Voltage Monitor circuit to ensure PSU pwr rails are mostly up and stable before the VR is enabled
5. Circuit is used to monitor PSU for unexpected power down scenarios via falling edge of PSU PWROK output. To improve boot latency, the PSU PWROK rising edge is not used as a qualifier to gate PLTRST# deassertion via SYS_PWROK assertion. PSU power rail stability is inferred on the platform thru other means, such as the VM block shown in the diagram
6. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

Many variations exist on how the various pwrgood signals can be generated on a DT platform to balance system robustness with platform costs constraints. This is just one example of possible logic connections. Components and connections in blue are alternative configurations. Components and connection in black show a baseline configuration.

### Figure 45-2. CFL Flow Diagram for RSMRST_PWRGD# Generation (Sheet 1 of 2)

## Figure 45-2. CFL Flow Diagram for RSMRST_PWRGD# Generation (Sheet 2 of 2)

***Notes:***

1. This circuit is for early detection of surprise power loss to support proper RTC isolation. By monitoring the main input supply for abnormal behavior, DSW_PWROK can be de-asserted before VRs sourced from the main input supply start to shutdown or fallout of regulation.
2. NA
3. NA
4. Optional. Added for addition system robustness.
5. The reference configuration shown does not use EC. The system may or may not use SUSWARN and SUSACK# for handshaking with the PCH before exit from DSx.
6. Depending on response time of VR logic to assertion of SLP_SUS#, this may be optional. Refer to RSMRST# timing requirement (tPCH12).

Many variations exist on how the various pwrgood signals can be generated on a MB platform to balance system robustness with platform costs constraints and area constraints. This is just one example of possible logic connections. Components and connection in black show a baseline configuration, and components and connections in blue are alternative configurations. DSx configuration is shown.

## Table 45-1. CFL Interface Signals List (Sheet 1 of 4)

| Name | Source | Destination | Description |
|---|---|---|---|
| RTCRST# | Platform | PCH | When asserted, the signal resets the register bits in the RTC well. |
| SRTCRST# | Platform | PCH | The signal resets the manageability register bits in the RTC well when the RTC battery is removed |
| DSW_PWROK | Platform | PCH | Indication to the PCH that VCCDSW_3p3V rail is stable.<br>For platforms NOT supporting Deep Sx this pin can be tied to RSMRST#. |
| RSMRST# | Platform | PCH | This signal is used for resetting the Primary power plane logic. This signal must be asserted for at least 10 ms after the Primary power wells are valid. When de-asserted, this signal is an indication that the power wells are stable. |
| SUSWARN# | PCH | Platform | This function is only applicable to platforms supporting Deep Sleep Wells<br>This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (using SLP_SUS#). The EC/ motherboard controlling logic must observe edges on this pin, preparing for Primary well power loss on a falling edge and preparing for Prim well related activity (host/Intel ME wakes and runtime events) on a rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#. |

## Table 45-1. CFL Interface Signals List (Sheet 2 of 4)

| Name | Source | Destination | Description |
|---|---|---|---|
| SUSPWRDNACK | PCH | Platform | This function is only applicable to platforms NOT supporting Deep Sleep Wells<br>Asserted high by PCH when it does not require Primary well to be powered. No longer requires a 10-K pull-up to VCCSUS (3.3 V).<br>This signal is required to be connected to EC for platforms with or without M3 support that do not support Deep Sx.<br>This signal gives an added flexibility for the EC to turn OFF the Prim Rails when not needed by the PCH.<br>SUSPWRDNACK can be High/Low in Sx/Moff based on the ME power policy selected.<br>If platform doesn't support both Deep Sx and M3:<br>EC must keep Prim rails powered ON if:<br>SUSPWRDNACK is de-asserted low OR<br>System state is S3<br>Else, EC has the option to turn-off the Prim rails<br>If platform doesn't support Deep Sx, but supports M3:<br>EC must keep Prim rails powered ON if:<br>SUSPWRDNACK is de-asserted low OR<br>System state is S3 OR<br>SLP_A# is de-asserted high OR<br>It's the first 200 ms after Prim rails power has been applied<br>Else, EC has the option to turn-off the Prim rails.<br>**Note:** The polarity of SUSPWRDNACK is the opposite of SUS_WARN#. SUS_WARN# will assert low when Primary well power will be turning off, however SUSPWRDNACK will assert high when Primary well power can be turned off. |
| SUSCLK | PCH | Platform | This clock is an output of the RTC generator circuit for use by other chips for refresh clock. SUSCLK is now moved to DSW (new on CFL). |
| ACPRESENT | Platform | PCH | Used on mobile systems to determine presence of AC power or battery power. In addition to previous Intel® ME to EC communication, PCH uses this signal to implement Deep Sx policies. For example, the platform may be configured to enter Deep Sx only on battery and not AC. |
| SUS_ACK# | Platform | PCH | For platform supporting Deep Sx state, this signal is driven from the platform EC to PCH to acknowledge that EC has received the SUSWARN# signals and it is preparing to go into DeepSx mode.<br>For non-DSW platforms, this signal can be left unconnected. Due to the internal pull-up on this signal it will be pulled high in order for the boot sequence to proceed. It does not matter if this assertion happens before or after SUSPWRDNACK assertion. |
| SLP_SUS# | PCH | Platform | For platforms supporting Deep Sx state, a low on this signal indicates that PCH is in Deep Sx state and that EC/platform logic does not need to keep the Primary Rails ON.<br>If high means EC must keep Primary rails ON.<br>If Deep Sx is not supported, then this pin can be left unconnected. |
| PWRBTN# | Platform | PCH | Signal driven from EC to PCH indicating a system request to go into Sleep State OR if the system is already in the Sleep State then it will cause a wake event. |
| SLP_A# | PCH | Platform | This signal is used to control power to devices on the platform in conjunction with the Intel® ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timings as SLP_S3#. |
| SLP_LAN# | PCH | Platform | LAN Sub-System Sleep Control. Controls power to the LAN PHY. When "low", indicates that power can be shut off to the external wired LAN (GbE) PHY. SLP_LAN# will always be de-asserted in S0 and Sx/M3. |
| SLP_S5# | PCH | Platform | This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S5 (Soft Off) states. |

## Table 45-1. CFL Interface Signals List (Sheet 3 of 4)

| Name | Source | Destination | Description |
|---|---|---|---|
| SLP_S4# | PCH | Platform | S4 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S4 (Suspend to Disk) or S5 (Soft Off) states. |
| SLP_S3# | PCH | Platform | S3 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S3 (Suspend to RAM), S4 (Suspend to Disk) or S5 (Soft Off) states. |
| CL_RST# | PCH | Platform | This signal connects to the Wireless LAN device supporting Intel® AMT. |
| VDDQPWRGD | Platform VR | Platform Logic | Indicates that the DRAM power supply is stable and within specification. |
| Platform S0 Rails | Platform | Processor/PCH | These are all the non-core platform rails. |
| RSMRST_PWRGD# | Platform | Platform | The signal represents power good for VCCPRIM rails, 3.3V_DSW, and other S5 rails. |
| ALL_SYS_PWRGD | Platform | Platform | This signal represents the power good for all the non-core and non-graphics power rails. |
| IMVP VR_READY | Platform | CPU VR power circuitry | IMVP VR_READY is an active-high output that indicates the start-up sequence is complete, and the VR is ready to accept an SVID command and is operating properly. Refer to the VR_READY definition in the IMVP8 spec for additional details. |
| PCH_PWROK | Platform | PCH | When asserted, it indicates that all the main PCH Primary rails are up and all the main CPU rails (excluding VCC, VCCGT, VCCGTx, VCCOPC and VCCEOPIO) are up. |
| SYS_PWROK | Platform | PCH | Generic power good input to the PCH is driven and utilized in a platform-specific manner. Informs PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset (de-asserts PLT_RST# to the processor).<br>**Note:** PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. PCH does not monitor SYS_PWROK until after PCH_PWROK is asserted. |
| DRAM_RESET# | PCH | Processor | Controls reset to the memory subsystems, and is used on DDR3L, DDR4 (not applicable to LPDDR3). |
| PROCPWRGD | PCH | Processor | Indicates that VCCST, VCCSTG, VCCPLL, VCCPLL_OC, VCCIO, VCCSA, VDDQ (and for OPC SKUs, VCCOPC_1p8) power supplies and clocks are stable. This signal will be asserted only after PCH_PWROK assertion. |
| SUS_STAT# | PCH | Platform | This signal is asserted by the PCH to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. |
| PLTRST# | PCH | Processor | The PCH asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN etc.). Asserted during power-up and when S/W initiates a hard reset sequence through the Reset Control register. |
| SPI | PCH | Flash Device | **S**erial **P**eripheral **I**nterface between PCH and BIOS Flash Device. |
| DMI | PCH | Processor | **D**irect **M**edia **I**nterface transactions between PCH and Processor. |
| SLP_WLAN# | PCH | WLAN | WLAN Sub-System Sleep Control: When SLP_WLAN# is asserted, power can be shut off to the external wireless LAN device. SLP_WLAN# will always be de-asserted in S0. |
| LAN_WAKE# | PHY | PCH | Can be used by the LAN PHY as a wake signal. |
| ESPI_RESET# | PCH | Platform | Controls reset to eSPI |
| VCCST_PWRGD | Platform | Processor | Indication that the VCCST\VDDQ power supplies are stable and within specification |
| DDR_VTT_CNTL | CPU | VTT VR | Enable signal for the DDR VTT VR |
| SLP_S0# | PCH | Platform | S0 Sleep Control. When PCH is idle and processor is in C10 state, this pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations. |

### Table 45-1. CFL Interface Signals List (Sheet 4 of 4)

| Name | Source | Destination | Description |
|---|---|---|---|
| CPU_C10_GATE# | CPU | Platform | Power gating control to turn off VCCSTG, VCCIO and VCCPLL_OC in C10 |

### Table 45-2. CFL Power Sequence Related Power Rails

| Name | Source | Destination | Description |
|---|---|---|---|
| VCCRTC | Platform | PCH | 3.05-V supplies for PCH RTC Well. This power is not expected to be shut off in any of the sleep states unless the RTC battery is removed or completely drained. |
| VCCDSW_3p3 | Platform | PCH | 3.3-V supply for Deep Sx wells. If Deep Sx is not supported on the platform, tie to VCCPRIM_3p3 |
| VCCPRIM_1p0/1p8/3p3 | Platform | PCH | PCH I/O and Misc rails 1.0/1.8/3.3V (Primary Well) |
| VCCSPI | Platform | PCH | 1.8V/3.3-V supply for the SPI IO. This rail must be powered when VCCPRIM is powered. |
| VCC | Platform | Processor | Processor core rail |
| VCCST | Platform | Processor | Sustain voltage for processor in Standby modes |
| VCCPLL | Platform | Processor | CPU PLL power rails |
| VCCPLL_OC | Platform | Processor | CPU digital PLL power rails |
| VCCGT | Platform | Processor | Sliced graphics power rail |
| VCCGTx[1] | Platform | Processor | Unsliced graphics power rail |
| VCCIO | Platform | Processor | IO power rail |
| VDDQ | Platform | Processor | CPU Memory power rail, voltage dependent on memory technology |
| VPP | Platform | Processor | CPU Memory power rail, voltage dependent on memory technology |
| VCCSA | Platform | Processor | System Agent power rail |

## 45.3 Power States

### Table 45-3. System with M3 State Supported (Sheet 1 of 2)

| Rails | S0/M0 | S0ix/ M-off[16] | S3/M3 | S3/M-off | S4 & S5/M3 | S4 & S5/ M-off | Deep S3 | Deep S4/ S5 | G3[1] |
|---|---|---|---|---|---|---|---|---|---|
| RTC Well | ON | ON | ON | ON | ON | ON | ON | ON | ON |
| 3.3V_DSW | ON | ON | ON | ON | ON | ON | ON | ON | No Power |
| VBATA (VDC) | ON | ON | ON | ON | ON | ON | ON | ON | No Power |
| V5.0A | ON | ON | ON | ON | ON | ON | OFF | OFF | No Power |
| V3.3A | ON | ON | ON | ON | ON | ON | OFF | OFF | No Power |
| V1.8A | ON | ON | ON | ON | ON | ON | OFF | OFF | No Power |
| V1.0A | ON | ON | ON | ON | ON | ON | OFF | OFF | No Power |
| V3.3M[3] | ON | OFF | ON[11] | OFF | ON[11] | OFF | OFF | OFF | No Power |
| V1.8M[3] | ON | OFF | ON[11] | OFF | ON[11] | OFF | OFF | OFF | No Power |
| VDDQ | ON | ON | ON | ON | OFF | OFF | ON | OFF | No Power |
| V2.5U | ON | ON | ON | ON | OFF | OFF | ON | OFF | No Power |
| VCCST[13] | ON | ON | ON [19] | ON [19] | OFF[5] | OFF[5] | OFF | OFF | No Power |
| VCCPLL | ON | ON | ON[7, 19] | ON[7, 19] | OFF[5] | OFF[5] | OFF[5] | OFF | No Power |

### Table 45-3. System with M3 State Supported (Sheet 2 of 2)

For Devices that should be turned off completely when entering sleeping mode

| Rails | S0/M0 | S0ix/ M-off[16] | S3/M3 | S3/M-off | S4 & S5/M3 | S4 & S5/ M-off | Deep S3 | Deep S4/ S5 | G3[1] |
|---|---|---|---|---|---|---|---|---|---|
| V3.3S | ON | ON | OFF | OFF | OFF | OFF | OFF | OFF | No Power |
| VCCPLL_OC[13] | ON | OFF[17] | ON[8, 19] | ON[8, 19] | OFF | OFF | OFF[8] | OFF | No Power |
| VCC | ON | OFF | OFF | OFF | OFF | OFF | OFF | OFF | No Power |
| VCCGT/VCCGTx | ON | OFF | OFF | OFF | OFF | OFF | OFF | OFF | No Power |
| VCCIO | ON | OFF[17] | OFF | OFF | OFF | OFF | OFF | OFF | No Power |
| VCCSA | ON | OFF[17] | OFF | OFF | OFF | OFF | OFF | OFF | No Power |

***Notes:***
1. The state of the system without RTC well powered can also be considered G3.
2. NA
3. V3.3M and V1.8M are platform rails used by external devices which ME operates during Sx/M3 states. These rails are not use directly by the CPU/PCH, and are not present on non-M3 supported systems
4. NA
5. VCCST, VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 46, "Platform Debug and Test Hooks".
6. NA
7. VCCPLL is allowed to be OFF in this power state, but it is generally assumed to be ON since it is powered from the same source as VCCST. VCCPLL should never be ON while VCCST is OFF
8. VCCPLL_OC is allowed to be turned off during S3 if it is not powered directly from VDDQ
9. NA
10. For no M3 support on external devices, V3.3M/V1.8M will be OFF in Sx/M3
11. VCCOPC_1p8 may be left on in Sx with minimal leakage.
12. NA
13. Assume SLP_S0# and CPU_C10_GATE# have asserted from the PCHThis supply is expected to be OFF during states where SLP_S0# is asserted. It may be left on during this condition, but the SoC will not achieve it's lowest power consumption. Specific power up latencies apply when exiting this stateVCCST should be "on whenever VCCPLL_OC is "on". VCCPLL_OC must be "off" whenever VCCST is "off", pay special attention particularly for systems supporting DS3.
14. For additional power savings in S3, refer Section 45.5, "Additional Power Optimizations with Respect to VCCST Rail in S3"

## 45.4 Power Sequencing Timing Diagrams—Legacy Signals

### Table 45-4. Legend for Signals in Transition Waveforms

| Color/Legend | Comments |
|---|---|
| *Signal Names* | Timing of these signals is set by PCH or processor |
| **Signal Names** | Timing of these signals should be met by the platform |
| Signal Names | Voltage rails or chip-to-chip buses |
| Grey Highlight | Indicates unstable state |

## Figure 45-3. Timing Diagram for G3 to S0/M0 [Deep Sx Platform] (Sheet 1 of 2)

## Figure 45-3. Timing Diagram for G3 to S0/M0 [Deep Sx Platform] (Sheet 2 of 2)

***Notes:***

1. PCH will sample BATLOW# on the rising edge of DSW_PWROK for DSx Systems
2. Refer section TBD details on PCH prime rail-to-rail power and power down dependencies
3. For a DSx system, PCH will ignore SUSACK# until after SUSWARN# is valid
4. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
5. On first exit from G3, SLP_A# de-asserts with SLP_S3# de-assertion
6. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#
7. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
8. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
9. VCCST and VCCPLL can remain powered during S4 and S5 pwr states for board VR optimization. VCCST may also remain powered in S4 and S5 for debug purposes. Refer to debug port design guide for more details.
10. Only required with LPDDR3 and DDR4 memory configurations
11. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
12. VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps.
13. IMVP VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
14. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
15. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD and / or SLP_S3# in their generation. This ensures during failure events, both signals de-assert at the same time
16. NA
17. When "Power Button" is the trigger for wake or sleep event for the system
18. The Platform should ensure that PCH_PWROK does not glitch when RSMRST# is de-asserted
19. PS has a wide range of specifications, which may affect boot latency
20. Use of DDR_VTT_CNTL to control VTT power gate is optional for additional power savings in Idle power states. If not used, VTT should be controlled by SLP_S3#

power up

## Figure 45-4. Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)

## Figure 45-4. Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 2 of 2)

***Notes:***

1. SLP_SUS# is ignored in Non-DSx systems
2. Refer section TBD for details on PCH prime rail-to-rail power and power down dependencies
3. For a non-DeepSx system DSW_PWROK and RSMRST# go high at the same time (connected on board)
4. For a non-DeepSx system SUS_ACK# will rise with prime voltage rail powering the VCCPGPPA power pin due to weak internal pull-up.
5. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
6. On first exit from G3, SLP_A# de-asserts with SLP_S3# de-assertion
7. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#
8. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
9. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
10. VCCST and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST may also remain powered in S4 and S5 for debug purposes. Refer to debug port design guide for more details.
11. Only required with LPDDR3 and DDR4 memory configurations
12. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
13. VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps
14. IMVP VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
15. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
16. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD and / or SLP_S3# in their generation. This ensures during failure events, both signals de-assert at the same time
17. NA
18. When "Power Button" is the trigger for wake or sleep event for the system
19. The Platform should ensure that PCH_PWROK does not glitch when RSMRST# is de-asserted
20. PS has a wide range of specifications, which may affect boot latency
21. Use of DDR_VTT_CNTL to control VTT power gate is optional for additional power savings in Idle power states. If not used, VTT should be controlled by SLP_S3#

***Additional Notes:***

The state of the SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.

- SUSPWRDNACK
  - *Platform not supporting M3* - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3. Else, EC has an option to do whatever it wants with the SUS Rails
  - *Platform supporting M3* - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3 **OR** SLP_A# is de-asserted **OR** it is the first 200mS after SUS Rails power has been applied. Else, EC has an option to do whatever it wants with the SUS Rails
- Primary rails and Deep Sx Rails should **never** be active while VccRTC rail is inactive.

## Figure 45-5. Timing Diagram for S0/M0 to G3 [Deep Sx Platform]

***Notes:***

1. These are all the processor S0 non-Core rails. Includes the rails like 3.3-V/5-V platform rails, etc.
2. This represents the overall Power-Good signal including the platform rails mentioned in Note (1)
3. Signal may drop before or after SLP _S4# / SLP_S5 # / DDR_RESET# assertion
4. VCCST and VCCPLL may remain powered during Sx power states for Debug support and platform VR optimization. Platform designers will need to account for proper power rail management with external devices and circuity to avoid leakage path scenarios.
5. VCCST_PWRGD signal must deassert in all Sx / DSx states, regardless of the status of the VCCST rail
6. PCH waits for SUS _ACK# to deassert before proceeding with Deep S4/S5 flow. If SUSWARN#/SUS_ACK # handshake is not used, these signals are tied on the board
7. High for WoL=1, Low forWoL=0
8. High for WoWLAN =1, Low for WoWLAN = 0
9. Present on LPDDR3 and DDR4 systems only. Must ramp down ***AFTER*** VDDQ has ramped down
10. Refer to Section 45.6.2, "RSMRST#/DSW_PWROK Special Considerations"

## Figure 45-6. Timing Diagram for S0/M0 to G3 [Non-Deep Sx Platform]

***Notes:***

1. These are all the processor S0 non-Core rails. Includes the rails like 3.3-V/5-V platform rails, etc.
2. This represents the overall Power-Good signal including the platform rails mentioned in Note (1)
3. Signal may drop before or after SLP _S4# / SLP_S5 # / DDR_RESET# assertion
4. VCCST and VCCPLL may remain powered during Sx power states for Debug support and platform VR optimization. Platform designers will need to account for proper power rail management with external devices and circuity to avoid leakage path scenarios.
5. VCCST_PWRGD signal must de-assert in all Sx / DSx states, regardless of the status of the VCCST rail
6. PCH waits for SUS _ACK# to deassert before proceeding with Deep S4/S5 flow. If SUSWARN#/SUS_ACK # handshake is not used, these signals are tied on the board
7. High for WoL=1, Low forWoL=0
8. High for WoWLAN =1, Low for WoWLAN = 0
9. Present on LPDDR3 and DDR4 systems only. Must ramp down ***AFTER*** VDDQ has ramped down

## Figure 45-7. Timing Diagram for Warm Reset (Host Partition Reset w/o Power Cycle)

## Figure 45-8. Timing Diagram for Cold Reset (Host Partition Reset w/ Power Cycle) and Global Reset [Non-Deep Sx Platform]

***Notes:***

1. Present on LPDDR3 and DDR4 systems only. Must ramp down AFTER VDDQ has ramped down
2. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
3. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may end up after SLP_S3# de-assertion due to VR ramp timing and configuration
4. VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps
5. IMVP VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
6. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
7. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time

### 45.4.1 Power Sequencing Timing Requirements

The following table defines the timing parameters used in the timing diagrams in previous sections. The timing parameters are put into three categories: tCPU, tPCH, and tPLT. tCPU parameters are mostly required by the processor, tPCH parameters are required or controlled by the PCH, and tPLT parameters are mostly controlled by the platform.

**Table 45-5. Platform Sequencing Timing Parameters (Sheet 1 of 7)**

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|
| tCPU00 | CPU | PLT | 1 | | ms | 6, 7, 26 | VCCST ramped and stable to VccST_PWRGD assertion |
| tCPU01 | CPU | PLT | 1 | | ms | 6, 7 | VDDQ ramped and stable to VccST_PWRGD assertion |
| tCPU02 | CPU | PLT | | No limit | ms | 26, 43 | VCCST ramped and stable before VDDQ stable<br>**Note**: tCPU02 and tCPU03 are mutually exclusive, and only one of the parameters needs to be met depending on the rail order of VCCST/VCCSTG and VDDQ. |
| tCPU03 | CPU | PLT | | 25 | ms | 26, 43 | VDDQ ramped and stable before VCCST stable<br>**Note**: tCPU02 and tCPU03 are mutually exclusive, and only one of the parameters needs to be met depending on the rail order of VCCST/VCCSTG and VDDQ. |
| tCPU04 | CPU | PLT | 0 | | ns | 26, 31 | VCCST must always ramp with or earlier then VCCSTG. VCCST >= VCCSTG at all times during ramp. |
| tCPU05 | CPU | PLT | 100 | | ns | | VDDQ ramped and stable before VCCSA/ VCCIO ramps |
| tCPU06 | CPU | PLT | 100 | | ns | 27 | VCCST ramped and stable before VCCSA/ VCCIO ramps. |
| tCPU07 | CPU | PLT | No Req | No Req | ns | | VCCSA ramped and stable before VCCIO stable<br>**Note:** this timing is to explicitly call out that there is no timing requirement between VCCSA and VCCIO. |
| tCPU08 | CPU | PCH | 1 | | ms | 8 | PCH CLK outputs stable and CPU VRs stable/ ready to PROCPWRGD assertion |
| tCPU09 | CPU | PLT | 1 | | ms | 23 | VCCSA stable before PROCPWRGD |
| tCPU10 | CPU | PLT | 1 | | ms | 23 | VCCIO stable before PROCPWRGD |
| tCPU11 | CPU | PLT | 1 | | ms | 23 | VCCPLL stable before PROCPWRGD |
| tCPU12 | CPU | PLT | 1 | | ms | 23 | VCCPLL_OC stable before PROCPWRGD |
| tCPU16 | CPU | PLT | 0 | | ns | 32 | VCCST_PWRGD assertion to PCH_PWROK assertion |
| tCPU18 | CPU | PLT | 0 | 35 | us | 34 | DDR_VTT_CNTL (was DDR_PG_CTL) assertion to DDR VTT supplied ramped and stable while PLTRST = H (de-asserted). |
| tCPU19 | | CPU | 0 | 100 | ns | 9 | VccST_PWRGD assertion to DDR_VTT_CNTL (was DDR_PG_CTL) asserted. |
| tCPU20 | CPU | PLT + PCH | | 500 | ms | 10 | THERMTRIP# assertion until VCC, VCCGT, VCCSA, VCCIO VRs are disabled and not sourcing power. |
| tCPU21 | CPU | PCH | | 1 | ms | | THERMTRIP# assertion until PCH issues global reset and assertion of SLP_SX signals |

## Table 45-5. Platform Sequencing Timing Parameters (Sheet 2 of 7)

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|
| tCPU22 | CPU | PLT | 1 | | us | | VCCST_PWRGD de-assertion to either VDDQ, VCCST below specification for normal S0 to Sx transitions. Recommend VCCST_PWRGD goes low with SLP_S3#. |
| tCPU23 | CPU | PCH | TBD | | us | 45 | PROCPWRGD de-assertion to either VCC* below specification for normal S0 to Sx transitions |
| tCPU26 | CPU | PLT | 10 | 65 | us | 11 | CPU_C10_GATE# de-assertion to VCCSTG stable<br>Note: CPU_C10_GATE# de-assertion to VCCST also needs to meet max 65us on cold boot |
| tCPU27 | CPU | PLT | 10 | 240 | us | 11 | CPU_C10_GATE# de-assertion to VCCIO stable |
| tCPU28a | CPU | PLT | | 200 | us | 36 | SLP_S3# assertion to VCCST_PWRGD de-assertion |
| tCPU28b | CPU | PLT | 0 | | us | 37, 38 | VCCST_PWRGD low to VCCST dropping 5% of nominal value |
| tCPU29 | CPU | PLT | | 100 | mV/us | 13, 25 | Processor power rail instantaneous slew rate. |
| tCPU33 | CPU | PLT | | 240 | us | 11 | CPU_C10_GATE# de-assertion to VCCPLL_OC stable |
| tPCH01 | PCH | PLT | 9 | | ms | 1, 47, 48 | VccRTC = 2.0V to the point in time where voltage on the RTC resets equals 0.65 times the voltage present on the VccRTC rail during ramp. This measurement should be made from VccRTC = 2.0V to the first of RTCRST# or SRTCRST# reaching 0.65 * VccRTC |
| tPCH02 | PCH | PLT | 10 | | ms | | VccDSW stable (@95% of full value) to DSW_PWROK high |
| tPCH03 | PCH | PLT | 10 | | ms | | VccPrimary stable (@95% of full value) to RSMRST# high |
| tPCH04 | | PCH | 9 | | ms | 29, 42 | VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with coined RTC battery |
| tPCH48 | | PCH | 30 | | ms | 29, 42 | VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with coinless RTC |
| tPCH05 | PCH | PLT | 1 | | us | 42 | RTCRST# high (voltage above ViH_min) to DSW_PWROK high (when voltage crosses ViL_max such that internally it might be resolved as a logic '1') |
| tPCH06 | PCH | PLT | 200 | | us | | VccDSW 3.3 stable (@95% of full value) to VccPrimary 1.05V starting to ramp (for DSx or nonDSx configurations) |
| tPCH07 | PCH | PLT | 0 | | ms | | DSW_PWROK high to RSMRST# high |
| tPCH08 | PCH | PLT | 1 | | ms | | SLP_S3# de-assertion to PCH_PWROK assertion |

## Table 45-5. Platform Sequencing Timing Parameters (Sheet 3 of 7)

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|
| tPCH09 | PCH | PLT | 2, 4, 8, 16 | | ms | | SLP_A# high to PCH assuming ASW rails are stable (95% of full value) |
| tPCH10 | PCH | PLT | 400 | | ns | 4, 5 | PCH_PWROK low to VCCIO dropping 5% of nominal value |
| tPCH11 | PCH | PLT | 100 | | ns | | SLP_SUS# asserting to VccPRIM dropping 5% of nominal value |
| tPCH12 | PCH | PLT | 400 | | ns | 5, 24 | RSMRST# asserting to VccPRIM dropping 5% of nominal value |
| tPCH13 | PCH | | 0 | | ms | 14 | RTCRST# asserting to VccRTC dropping 5% of nominal value (this applies only when RTC battery is removed) |
| tPCH14 | PCH | PLT | 400 | | ns | 4, 5 | DSW_PWROK falling to any of VccDSW, VccPrimary dropping 5% of nominal value |
| tPCH15 | PCH | PLT | | 20 | ms | | SLP_LAN# (or LANPHYPC) rising to VccLANPHY high and stable |
| tPCH18 | | PCH | 90 | | us | | De-assertion of RSMRST# to De-assertion of eSPI_RESET# on exit from G3 (DSx platforms only), or exit from DSx |
| | | PCH | 95 | | ms | | De-assertion of RSMRST# to De-assertion of eSPI_RESET# on exit from G3 (Non-DSx platforms only) |
| tPCH20 | PLT | PCH | -100 | | ns | | DDR_RESET# assertion to SLP_S4# assertion (*The negative minimum timing implies that* DDR_RESET# *must either fall before SLP_S4# or within 100 nS after it*). |
| tPCH21 | | PCH | Note 39 | | ms | 39 | Warm Reset PLTRST# assertion duration time |
| tPCH22 | | PCH | 210 | | us | | SUS_STAT# active to PLTRST# active |
| tPCH23 | | PCH | 60 | | us | | SUS_STAT# de-assertion to PLTRST# de-assertion |
| tPCH24 | | PCH | 30 | | us | | PLTRST# assertion to PROCPWRGD de-assertion |
| tPCH25 | | PCH | 10 | | us | | PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF. This timing is programmable (Range = 10us, 100us, 1ms, 10ms). Default is set to 10 us. |
| tPCH26 | | PCH | 1 | | us | | CLKOUT_BCLK turning OFF to SLP_S3# assertion |
| tPCH27 | | PCH | 30 | | us | 33 | SLP_S4# assertion to SLP_S5# assertion |
| tPCH28 | | PCH | 30 | | us | 33 | SLP_S3# assertion to SLP_S4# assertion |
| tPCH29 | | PCH | 0 | | ms | | SLP_S3# assertion to PCH_PWROK deassertion |
| tPCH31 | | PCH | | tPCH02 + tPCH32 | ms | 15, 44 | VccDSW3p3 ramped and stable until SUSCLK is stable. SUSCLK will start before the max timing, but will not be guaranteed valid until max timing is met |
| tPCH32 | | PCH | 95 | | ms | | DSW_PWROK assertion to SLP_SUS# de-assertion (only applicable to Deep Sx supported platforms). |

## Table 45-5. Platform Sequencing Timing Parameters (Sheet 4 of 7)

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|
| tPCH33 | | PCH | 0, 99 | | ms | 16 | PCH_PWROK high to PLTRST# de-assertion. This timing is set by the PCH via Soft strap settings. |
| tPCH34 | PCH | PLT | | 50 | ms | | All PCH Primary Rails should ramp up within this window. |
| tPCH35 | PCH | PLT | | 100 | ms | 20 | All PCH Rails should ramp down within this window. |
| tPCH36 | PCH | PLT | | 100 | mV/us | | PCH Power rails instantaneous slew rate |
| tPCH37 | PCH | PLT | 5 | | mV/us | 21 | MPHY / SRAM Supply instantaneous slew rate |
| tPCH41 | PCH | PCH | 1 | | ms | | PCH_PWROK high to PCH clock outputs stable |
| tPCH42 | PCH | PLT | | 10 | mV/us | | VCCPRIM_Core slew rate during VID change |
| tPCH43 | PCH | PLT | 95 | | ms | 28 | DSW_PWROK assertion to PWRBTN# monitored |
| tPCH44 | PCH | PLT | 500 | | us | | tPCH09 expiring to CL_RST# high |
| tPCH45 | | PCH | 1, 5, 50, 100 | | ms | 41 | Clock outputs stable to PROCPWRGD assertion to processor. Timing set by PCH via Soft Strap settings |
| tPCH46 | | PCH | 1, 2, 5 | | ms | 41 | PROCPWRGD and SYS_PWROK High to SUS_STAT# de-assertion. **NOTE:** Timing can be adjusted through the FIT tool |
| tPCH47 | PCH | PLT | 0 | | ms | 46 | RCIN# de-asserted to PCH_PWROK assertion |
| tPLT01 | | PCH | 200 | | ms | 2 | RSMRST# de-assertion to SUSPWRDNACK valid. Timing set by PCH. |
| tPLT02 | | | 0 | 90 | ms | | RSMRST# de-assertion to ACPRESENT valid (not floating). **NOTE:** This is only for platforms not supporting Deep Sx state |
| | | | | 0 | ms | | RSMRST# de-assertion to ACPRESENT valid (not floating) [For platforms supporting Deep Sx state]. **NOTE:** ACPRESENT is a powered input to the PCH while in the Deep Sx state (that is, when DSW_PWROK=1 and RSMRST#=0). The PCH implements a weak pull-down on ACPRESENT while RSMRST#=0 such that the input is observed as 0 if not driven actively by the board during this time. If driven actively by the board to 1 while in Deep Sx and if the PCH is enabled to treat the ACPRESENT indication as a wake event from Deep Sx, then the PCH will power up the Primary well. |
| tPLT04 | CPU/PCH | PLT | 1 | | ms | 3, 19 | ALL_SYS_PWRGD assertion to PCH_PWROK. This timing must be controlled on the platform. |
| tPLT05 | | PLT | Platform dependent | No limit | | 18 | ALL_SYS_PWRGD assertion to SYS_PWROK. This timing must be controlled on the platform. SYS_PWROK provides a platform/EC mechanism to stall the PCH de-assertion of PLTRST# to the platform. Different platform components may have difference timing requirements from when their power rails are stable until their respective reset signal can de-assert. Platform designer should adjust this timing based on their specific platform requirements. |

## Table 45-5. Platform Sequencing Timing Parameters (Sheet 5 of 7)

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|
| tPLT11 | CPU | PLT | | 500 | ms | | SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA <100mV. |
| tPLT14 | | PCH | 4 | | s | | Power cycle duration time; programmable via PM_CFG.PWR_CYC_DUR bit. |
| tPLT15 | PLT (MEM) | PLT | | 200 | us | 40 | SLP_S4# assertion to VDDQ EN Low (VDDQ VR disabled). Memory dependent, refer JEDEC requirements |
| tPLT16 | PLT (MEM) | PLT | 30 | | ms | 30 | VDDQ ramp down to start of VPP ramp down when entering S4 and lower. This is not SOC requirement but a recommended timing to help meet the JEDEC sequencing requirements. Platform designers are responsible for making sure their designs meet the power sequencing requirements for the memory technology used in their designs. |
| tPLT20 | PLT (MEM) | PLT | 2.5 | | ms | 30 | VPP ramped to VDDQ start of ramp when entering S0 at power up. This is not SOC requirement but a recommended timing to help meet the JEDEC sequencing requirements. Platform designers are responsible for making sure their designs meet the power sequencing requirements for the memory technology used in their designs. |
| tPLT17 | CPU | PLT | | 200 | us | 35 | SLP_S3# assertion to IMVP VR_ON de-assertion |
| tPLT18 | CPU | PLT | | 200 | us | 35 | SLP_S3# assertion to VCCIO VR disabled |
| tPLT19 | PLT | PLT | | 10 | us | 22 | RSMRST_PWRGD# or SLP_SUS# assertion to RSMRST# assertion |

## Table 45-5. Platform Sequencing Timing Parameters (Sheet 6 of 7)

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|

***Notes:***

1. PCH Primary Rails must never be active while VCCRTC is OFF
2. RSMRST# should be de-asserted for at least 200ms before PCH will consider SUSPWRDNACK valid.
3. PCH can delay de-assertion of PLTRST# with a soft strap setting. Refer tPCH08 and tPCH09 and the SPI Programming Guide for more details.
4. For catastrophic/surprise power failures only.
5. For surprise power down cases, if DSW_PWROK is de-asserted (tPCH14) before DSW3.3 **and** any other Prim rails droop out of spec, there is no risk of RTC corruption (assuming VCCRTC was previously powered and VCCRTC# is de-asserted) and this spec can be ignored
6. VCCST_PWRGD has no edge rate requirement, but edges must be monotonic.
7. VCCST_PWRGD must accurately reflect the state of VCCST and must not glitch when VCCST, or VDDQ power is applied. Additionally, VCCST_PWRGD must track to the state of PCH_PWROK on the platform. When PCH_PWROK de-asserts during S0 --> Sx transitions, then VCCST_PWRGD must also de-assert.
8. Processor's PROCPWRGD is not expected to be used externally on the platform, but is available for monitoring.
9. CPU will assert DDR_VTT_CNTL after VCCST_PWRGD crosses its threshold point on rising edge, which will typically be around 0.5*VccST but can be anywhere between Vil to Vih levels.
10. It is strongly recommended that the SLP_S3# be a qualifying input signal to ALL_SYS_PWRGD logic, which drives IMVP VR_ON inputs. Additionally, it is recommended that SLP_S3# also qualify the EN control to the VCCIO power supply
11. NA
12. NA
13. Applies to all CPU power supply rails
14. There are no perceived functional failures if this minimum is violated since all data is lost anyway when VccRTC drops. The only real requirement is to avoid driving a high signal level into the powered down device for an extended period of time, assuming an external device(s) on a different power supply then VCCRTC is driving RTCRST# or any other RTC well input signal.
15. SUSCLK is now powered in DSW well.
16. PCH can delay de-assertion of PLTRST# with a soft strap setting. If tPCH33 is not enabled, the platform is responsible for controlling the assertion timing of PCH_PWROK and SYS_PWROK in such a way that it satisfies platform component timing requirements of power stable to reset de-assertion. Refer SPI Programming Guide for more details. On a platform level this timing doesn't necessarily need to meet 99ms, PCH soft straps guarantees a min of 99ms.
17. NA
18. Example, if the platform only has mini-PCIe* devices requiring a 1 ms delay from power rails stable to PCIe* reset de-assertion, then the minimum value for ALL_SYS_PWRGD assertion to SYS_PWROK can be reduced to 1 ms. If SYS_PWROK asserts before PCH_PWROK, no additional delay will be added by the PCH to delay PLTRST# de-assertion and the final timing value will be subject to internal PCH timing parameters.
19. PCH_PWROK assertion assumes all the following CPU and PCH voltage rails are ramped and stable **except** for: VCC, VCCGT, VCCGTx, VCCOPC, VCCEOPIO
20. No Ramp down requirement between rails. All VRs should stop regulation based on SLP_SUS# signal, or another common shutdown signal
21. NA
22. 10us max limit is an estimation and will vary based on platform VR and EC implementation details. Platform designers are responsible for ensuring that tPCH12 is not violated during normal DSx entries based on EC and VR response times to assertion of SLP_SUS# and/or RSMRST_PWRGD#
23. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD. Therefore, the platform is only responsible to have these rails ready a minimum of 0ms before PCH_PWROK assertion
24. Applicable to all power down sequences where Prime well rails are turned off and to emergency power loss. Refer RSMRST#/DSW_PWROK Special Considerations section for more details.
25. Only applicable to SKUs with OPC support
26. If VCCSTG and VCCIO supplies are merged together as a single supply, then VCCSTG/VCCIO supply must also satisfy this requirement
27. If VCCSTG and VCCIO supplies are merged together as a single supply, then the timing requirement is between VCCST/ VCCSTG/VCCIO and VCCSA

## Table 45-5. Platform Sequencing Timing Parameters (Sheet 7 of 7)

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|

***Notes:*** (cont)

28. Applicable to all G3 exits where GEN_PMCON_B.AG3E=1. The PWRBTN# must assert for at least 16ms after the minimum tPCH43 timing before PCH will detect PWRBTN# as a wake event
29. For scenarios where the coin-cell is dead or missing, the PCH can electrically tolerate the VCCRTC and VCCDSW/VCCPRIM 3.3V supplies ramping simultaneously with VCCDSW/VCCPRIM 3.3V leading VCCRTC by ~0.2 – 0.3V (i.e. voltage drop associated with the coin cell Schottky diode circuit). These scenarios are not allowed as typical power sequencing scenarios, and are expected to be very infrequent. In these scenarios, glitch-free signal operation on DSW signals can not be guaranteed when the platform is configured for DSx mode. Likewise, glitch-free signal operation on DSW and PRIM well signals can not be guaranteed when the platform is configured for non-DSx mode
30. Generally, JEDEC specifications require VPP >= VDDQ for both power up and power down sequences. This timing parameter is a suggested value as ensure this requirement is met on power down, but systems designer must account for other platform level considerations such as output decoupling, discharge circuits, etc that can alter this relationship.
31. VCCST supply is typically controlled by SLP_S4#, and VCCSTG supply is typically controlled by SLP_S0# AND SLP_S3#. Since the timing delay between SLP_S3# and SLP_S4# deassertion during a S4/S5 à S0 transition can be small (defined by tPCH28), OEMs may need to take extra steps to ensure this timing is met. Example, power gates of equivalent slew rate may be required on both VCCST and VCCSTG supplies. Alternatively, a small timing delay path might be required on the SLP_S3# path of the VCCSTG power gate enable
32. VCCST_PWRGD should start to assert no later than when PCH_PWROK asserts; however, VCCST_PWRGD may lag completing its ramp with respect to PCH_PWROK by up to 20us
33. Not applicable to eSPI mode, refer to the eSPI Compatibility Specification (RDC#508740) for eSPI implementations
34. Only applies to configurations that use DDR_VTT_VCTRL signal to enable/disable VTT VR and only applies after PLTRST# has de-asserted (ie, S0). VTT must be completely ramped and ready for full load at or before the de-assertion of PLTRST# on Sx -> S0 transitions.
35. Timing to VR being disabled, not until the VR is fully ramped down
36. S0 to S3 transition with VCCST powered in S3 state
37. S0 to Sx transition with VCCST unpowered in Sx
38. Recommend not to exceed 200us delay with respect to SLP_S3#
39. During a warm reset sequence, the PCH sequencing flows will internally re-execute several timing parameters and tpch45 and tpch46 are two of the parameters that are re-executed. tPCH45 and tPCH46 are primarily for G3/DSx/Sx -->S0 flows, but they are executed for cold boot, cold reset, and warm reset. The nominal setting for these timings is partially controlled by the setting of SPI soft straps associated with tPCH45 and tPCH46. The minimum possible PLTRST# assertion time will be equal to the soft strap settings for tPCH45 + tPCH46. The maximum PLTRST# assertion time is not guaranteed across all warm reset cycles, but the typical worst case assertion time is approximately equal to (tPCH45 soft strap setting) + (tPCH46 soft strap setting) + 20ms.
40. This is a platform timing recommendation to help ensure that memory device power down sequencing requirements between VDDQ and VPP are likely to be met (refer tPLT16). This is not a requirement for the CFL SoC itself. Refer to the JEDEC LPDDR3 and DDR4 power down sequencing requirements for more details
41. This parameter is programmable, refer to the Flash Descriptor Record in the SPI Programming Guide in the ME firmware package
42. For the dead RTC coin cell and coin cell-less with depleted main battery RTC cases where the 3.3DSW ramps and powers the RTC well, the board designer should set the 3.3DSW rail stable to DPWROK assertion delay (tPCH02) for = 30ms. This is required to ensure that SRTCRST# and RTCRST# de-assert after VCCRTC is stable, but before DPWROK assertion. Failure to meet this requirement may result in DPWROK asserting with, or before, SRTCRST# and RTCRST# reach VIH, which is a sequencing violation and can result in a non-booting system scenario. Refer Section 30.2 (Real Time Clock Topology Guidelines) and Section 59.3.13 (RTC Circuit) for SRTCRST# and RTCRST# RC timing network details
43. tCPU02 and tCPU03 are mutually exclusive, only tCPU02 or tCPU03 needs to be met
44. SUSCLK stable means the clock is toggling and is within it's defined parameters. This timing spec is applicable to all G3 exits, excluding the G3 exit immediately following the ramp of VCCRTC, which may have a longer delay
45. This does not concern platform design, this is internal to SOC.
46. RCIN# is expected to be low in S3 and lower, but can be kept high in S3 through S5 without issue. RCIN# low in S3 and lower will not cause an INIT#. This requirement does not preclude the platform for asserting RCIN# after PLTRST# de-assertion when entering S0.
47. C3 and C4 Capacitors used in the RTC external circuit should be evaluated with regards to aging, voltage and temperature characteristics to ensure reliable operation in the intended operating environment. See section 13.1.3 RTC External RTCRST# Circuit.
48. For measurement details, reference RTC Reset Timing Technical Advisory - RDC#610459.

***Additional Notes:***

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- DDR_RESET# behavior does not directly track the state of VDDQ rail. For DDR_RESET# to assert properly on surprise power failure, the VDDQ VR pwrgood output should be an input into the logic generating PCH_PWROK

## 45.5 Additional Power Optimizations with Respect to VCCST Rail in S3

Throughout the PDG, it is generally noted that the VCCST rail should be ON during S3 power states, and is thus generally shown as being controlled directly or indirectly by the SLP_S4# signal. To save additional power during S3 power state, it is allowable to turn the VCCST rail OFF during S3 given that the following requirements and considerations are met. First, the following table below must be met. To support this table, an additional power gate would be required on the VCCPLL_OC in order to isolate this supply and turn it off during S3. Second, VCCPLL_OC must meet all the same timing requirements and rail-to-rail ramp requirements as VDDQ relative to all other rails of interest, specifically tCPU01, tCPU02, tCPU03 and tCPU05. All various figures and tables throughout the PDG such as in this chapter and other associated documents such as the Debug Port Design Guide and Coffee Lake Platform Power Design Guidelines will not be updated to explicitly reflect this option of turning VCCST off during S3. Also, it is assumed that VCCST and VCCPLL are supplied from the same power gate on the platform as documented in the Platform Architecture Guide, thus references VCCST in this description also include VCCPLL.

**Table 45-6. Allowed VCCST and VCCPLL_OC Power State Combinations**

| VCCST | VCCPLL_OC | State |
|---|---|---|
| OFF | OFF | - VALID |
| OFF | ON | - INVALID |
| ON | OFF | - VALID |
| ON | ON | - VALID |
| ***Note:*** this table reflects valid and invalid power states for static, steady state conditions for leakage and long term reliability considerations | | |

## 45.6 Rail-to-Rail Power Sequencing Requirements

### 45.6.1 Rail-to-Rail Sequencing For Various Supplies

The following diagrams show the recommended rail-to-rail sequencing requirement for Deep Sx configuration (Figure 45-3) and Non-Deep Sx configuration (Figure 45-4).

In general, Cannon Lake PCH architecture implements new capability to help minimize rail-to-rail sequencing related problems. As long as the RTC 3.3 V supply is powered up properly in advance of DSW and Primary rails, new isolation logic is active and will help achieve proper isolation between power rails during power up and power down sequences. The I/O interfaces will achieve proper isolation between the Primary 1.0 V supply and the higher 1.8 V and 3.3 V Primary / DSW supplies as well as achieving glitch-less I/O behavior for signals that support this capability.

During scenarios where the RTC supply is not powered such as a dead coin cell scenario and it is instead ramping along the Primary/DSW supplies through external platform circuitry, proper isolation between the Primary 1.0 V supply and the higher 1.8 V and 3.3 V Primary / DSW supplies cannot be guaranteed. It is thus possible that current inrush/back drive events could exist in these cases, but these scenarios are not a reliability risk to the PCH. It is, however, assumed that for general operation of Cannon Lake PCH, the RTC supply should be ramped and valid before the DSW and Primary rails ramp. Ramping the RTC supply simultaneously with the VCCDSW_3p3 rail for

Deep Sx systems and VCCPRIM_3p3/VCCDSW_3p3 rails for Non-Deep Sx systems as a standard power up sequence for every G3 exit is not a valid configuration and is not allowed.

**Figure 45-9. CFL H Rail to Rail Sequencing Requirement for Deep Sx Configured System**

***Notes:***

1. VCCPRIM 1.8 V may include VCCPGPPA, VCCPGPPBCH, VCCPGPPD, VCCPGPPEF, VCCPGPPG, VCCHDA and/or VCCSPI if the rails are 1.8 V.
2. VCCPRIM 3.3 V includes VCCPRIM_3p3, VCCRTCPRIM_3p3 and may include VCCPGPPA, VCCPGPPBCH, VCCPGPPD, VCCPGPPEF, VCCPGPPG, VCCHDA, and/or VCCSPI if the rails are 3.3V.
3. VCCPRIM 1.0 V may include the following rails: VCCPRIM_1p0, VCCMPHY_1p0, VCCPCIEPLL_1p0, VCCAPLLEBB_1p0, VCCUSB2PLL_1p0, VCCHDAPLL_1p0, VCCMPHYPLL_1p0, VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6.

## Figure 45-10.CFL H Rail to Rail Sequencing Requirement for Non-Deep Sx Configured System

***Notes:***

1. VCCPRIM 1.8 V may include VCCPGPPA, VCCPGPPBCH, VCCPGPPD, VCCPGPPEF, VCCPGPPG, VCCHDA and/or VCCSPI if the rails are 1.8 V.
2. VCCPRIM 3.3 V includes VCCPRIM_3p3, VCCRTCPRIM_3p3 and may include VCCPGPPA, VCCPGPPBCH, VCCPGPPD, VCCPGPPEF, VCCPGPPG, VCCHDA, and/or VCCSPI if the rails are 3.3V.
3. VCCPRIM 1.0 V may include the following rails: VCCPRIM_1p0, VCCMPHY_1p0, VCCPCIEPLL_1p0, VCCAPLLEBB_1p0, VCCUSB2PLL_1p0, VCCHDAPLL_1p0, VCCMPHYPLL_1p0, VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6.

### 45.6.1.1 General Rail-to-Rail Sequencing

For power up, all Primary rails should ramp within 50 ms of each other

For power down, there are no explicit timing requirements/relationships between the various Primary Well voltages on power down, but it is required that all Primary Well voltage regulators stop regulation simultaneously based on SLP_SUS# assertion. The power down sequencing should not be staggered from one VR to the next. Natural variance between VRs disabling due to differences in voltage regulator disable time is acceptable on the order of tens of microseconds. It is required that all rails ramp down within ~100 ms.

For surprise power down requirements, refer Section 45.6.3 for assumptions.

**Table 45-7. Rail-to-Rail Seque[1]ncing Requirements**

| Rail 1 | Rail 2 | Ramp Up | Ramp Down |
|---|---|---|---|
| VCC_PRIM 3.3 V/ VCC_PRIM 1.8 V | VPRIM_CORE/ VCC_PRIM 1.0 V | 3.3 V Primary/1.8 V Primary rails ramp in advance of the 1.0 V Primary and VCCPRIM_Core rails | All rails must ramp down within 100 ms. Refer Section 45.6.1.1. |
| VCC_PRIM 3p3/VCC_PRIM 1.0V | Vbus | Vbus ramp after VCC_PRIM 3.3V and VCC_PRIM1.0V have both reached 95% of their final nominal voltage. | Vbus must ramp down with or before the PRIM rails. |

***Notes:***

1. VCC_PRIM 1.0V may include the following rails: VCCPRIM_1p0, VCCSRAM_1p0, VCCMPHYAON_1p0, VCCMPHYGT_1p0, VCCMPHYPLL_1p0, VCCAPLL_1p0, VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK%, VCCCLK6

### 45.6.1.2 Primary Rails and External USB Vbus Power Sequencing

The Vbus provided to external USB ports can be used by USB devices to power their USB speed detect pull-up resistors. Some devices generate a local 3.3V power supply and pull up the D+ / D- lines with a 1.5k resistor. Other devices, per more recent USB ECRs, are allowed to pull up the D+/D- lines with Vbus voltage directly using ~7.5k resistor; implementation varies with device design.

If Vbus is powered while VCCPRIM_3p3 is not powered, and a device pulls either data line to 3.3V via its speed select pull-up resistor, the PCH will be exposed to leakage current through its un-powered USB 2.0 buffers. These leakage paths potentially impact both Non-Deep Sx and Deep Sx board designs alike.

The leakage paths exist only when Vbus is powered while VCCPRIM_3p3 and VCCPRIM_1.0V are both unpowered.

Powering Vbus while the PRIM rails are not powered is permitted, but designers should be aware that leakage through the PCH may occur.

## 45.6.2 RSMRST#/DSW_PWROK Special Considerations

When the system is powered off (G3), DSW_PWROK and RSMRST# must not glitch from their Low states while the corresponding PCH rails are not powered or are below normal operating voltage specifications to ensure RTC corruption does not happen.

When a system is in S0-S5 state and not entering a Deep Sx or G3 state, the RSMRST# may only be driven low if the DSW_PWROK is also driven low (by an external controller such as EC). Failure to meet this requirement may result in unexpected PCH behavior, including failure to boot, which may only be recovered through a G3 cycling. This requirement does not apply to systems that tie the DSW_PWROK and RSMRST# together.

RSMRST# must always be driven low before any of the PRIMARY rails fall below the lower end of their tolerance band (Taking RSMRST low without taking DSW_PWROK low is not permitted when not entering DSx states). This is true for all power states transitions including emergency power loss.

### 45.6.3 Surprise Power Down Sequencing Considerations

Surprise power down events will be treated slightly differently on Cannon Lake PCH compared to past generation platforms. The main goal of the various power down timing specification such as tPCH10, tPCH12, tPCH14, etc., is to ensure proper isolation between the associated power well and the RTC well to guarantee that RTC contents are not accidentally corrupted. There are many events that could cause a surprise power down. The following is a short list of some events, but is not exhaustive:

- VR failure (over current, overvoltage, IC failure, etc.)
- AC removal with no DC Battery present
- Removal of the primary battery

Properly designed platforms generally should not be experiencing VR failures of any kind; therefore the focus of this section is on the unexpected power removal caused by user interaction, which could be an end user, factory technicians, etc.

To ensure RTC is not corrupted, the platform must de-assert the appropriate power good signals BEFORE the rails go out of their defined tolerance range. This implies that the platform should monitor the highest voltage available which is usually the main power supply like the battery voltage to determine when it has dropped too low and VR failure/shutdown is eminent. At that point, the PCH power good signals (PCH_PWROK, RSMRST#, DSW_PWROK) should be driven Low before their associated rails turn off and droop below the defined tolerance. Note, for these cases, de-assertion of just the DSW_PWROK signal is sufficient to activate isolation logic for ALL power wells, thus guaranteeing RTC corruption cannot happen.

Refer Figure 45-7 below for more details.

**Figure 45-11.DSW_PWROK Requirement for Power Loss**

### 45.6.4 eSPI Considerations for Sequencing

In general, eSPI support does not have any major impact to power sequencing requirements. However, there are a few behavioral differences worth noting that could have side effects to platform behavior that should be considered.

With eSPI, the EC may or may not take in or drive physical pins that historically would have been supported by the PCH. The values of these signals (ex. SLP_S4#) are tunneled over the eSPI interface between the PCH / EC like virtual wires. If the EC is driving the physical version of these virtual wire signals instead of the PCH driving the signal natively, the PCH cannot guarantee the timing relationships between various tunneled sequencing signals is maintained due to inherent bus latencies.

Only the physical signals directly on the PCH are guaranteed to refer the PCH-defined timing relationships. Example, SLP_S4# de-assertion → SLP_S3# de-assertion relationship is defined as 30 us for the physical pins but could be shorter for the virtual wire relationship on the EC.

### 45.6.5 Virtual wire SUSWARN deassertion delay during global reset

1. For eSPI enabled platforms, the platform SUS_WARN# de-assertion can occur much later compared to LPC based previous platforms.
2. Hence it is recommended that eSPI based platforms should account for at least 5-6 seconds of delay between eSPI_RESET# de-assertion and SUSWARN# eSPI VW de-assertion from SoC/PCH to EC.
3. This additional delay between above mentioned PCH signals is applicable for Global reset flows only but not for G3 exit flows (or) Sx cycles which do not have the long delay between eSPI_RESET# and SUSWARN.
4. Note that the behavior above does not change the total time for Global reset exit.

§ §

# 46 Platform Debug and Test Hooks

Intel is committed to reducing debug time and cost for OEMs and system integrators. Many debug features and test hooks have been designed into the platform to help reduce these factors. The following section provides implementation details of the processor debug and test hooks specifically to this platform only and takes priority over any discrepancies existing between this document and any previous Debug Port Design Guide.

The details of this chapter are requirements for run control (XDP) debug-port design and Intel Direct Connect Interface (DCI), unless the text explicitly states that a design rule or connection is optional. Note that while this content provides design solutions to allow both run control tool and boundary scan test JTAG tool to utilize the same JTAG scan chain for debug and manufacturing testing respectively, it does not contain all of the routing and design requirements for use with a boundary scan JTAG tool. Please contact your Intel Field Representative if additional information on manufacturing boundary scan testing is needed.

***Note:*** The resistor values used for the JTAG signals in this content are meant for ITP or Run control JTAG debugger only and are subject to change according to test/debug tool condition. For example, some third party JTAG test tools may not have enough drive strength to meet the input-threshold requirements of the Intel Silicon with the strong 50-Ω terminations required for the ITP debugger.

The Coffee Lake JTAG (TAP) ports are compatible with the IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1 and 1149.6 Specification, as detailed per device in each BSDL file.

In this chapter, the term ITP and ITP-XDP can be interchanged with run-control tool or halt-mode debugger. Intel works with several run-control vendors to create tools that can be used if the guidelines within this document are followed. Please contact your Intel representative to obtain the list of tool vendors.

## 46.1 Platform Debug Port Options

Table 46-1 describes the two connector options and Table 46-2 describes the two JTAG based debug hook routing options for Coffee Lake platforms:

**Table 46-1. Coffee Lake Run Control Tool Debug Port Options (Sheet 1 of 2)**

| Debug Port Connectors | Figure/Diagram |
|---|---|
| **60-pin eXtended Debug Port (XDP) connector**<br>The XDP target system connector is a Samtec* 60-pin BSH-030-01 series connector. Specific plating types, locking clips, and alignment pins versions of this connector can be obtained from Samtec™. No specific plating types, locking clips or alignment pins are required for the XDP tool.<br><br>Refer Section 46.1.4 for 60-pin XDP Mechanical Specification | |

## Table 46-1. Coffee Lake Run Control Tool Debug Port Options (Sheet 2 of 2)

| Debug Port Connectors | Figure/Diagram |
|---|---|
| **Chassis Mount Connector (CMC)**<br>CMC is a compact connecting solution developed by Intel for Coffee Lake platform debug. CMC has a much smaller keep-out than the standard 60 pin XDP connector. It utilizes a motherboard through-hole for mounting and makes contact with pads located and routed around the mounting hole via the CMC connector. There are two versions of CMC adapters: the CMC Merged adapter (primary CMC) offers the same DFX accessibility (with the exception of SMBus), HOOK[2,3,4,5,7]) as the standard 60-pin XDP connector and the CMC OBS adapter (secondary CMC) provide access to PCH OBS signals via paddleboard.<br><br>Refer Section 46.1.5 for CMC Mechanical Specifications | **Primary CMC Debug Solution**:<br> <br><br>**Secondary CMC Solution**:<br> <br> |
| **Intel Direct Connect Interface (DCI)**<br>Intel® Direct Connect Interface (DCI) is a new Intel debug tool-transport technology that connects the host system to the System-Under-Test (SUT) using the USB3 port. The advantage is debug functions and trace features can be connected using existing USB3 ports, rather than the usual additional connectors. This enables easy connections to production systems where debug connectors have been removed. | |

## Table 46-2. Run Control Debug Hooks Routing Options

| Routing Options | Links to Guidelines | Use Cases |
|---|---|---|
| **Option 1** (preferred/ recommended):<br><br>One primary debug port (either a 60-pin XDP or a CMC) for Coffee Lake's JTAG, CFG[0:19], System control, power and ground signals:<br><br>• Support only dual TCK scan chain (aka Shared JTAG) design for the CPU and PCH components.<br><br>and,<br><br>One secondary debug port (either a 60-pin XDP or a CMC) for PCH Chipset Test Interface signals. | • Refer Section 46.1.1.1for detail routing guidelines for the Dual TCKs scan chain only topology.<br><br>• Refer Section 46.1.1.2 for CFG[19:0], PROC_PREQ#, PROC_PRDY# rand BPM#[1:0] routing guidelines.<br><br>• Refer Section 46.1.1.3 for Primary XDP System Control signals, Power and Ground pins routing guidelines.<br><br>• Refer Section 46.1.2 for detail routing guideline of Secondary Debug Port connector.<br><br>• Refer Section 46.1.4 for 60-pin XDP Mechanical Specification<br><br>• Refer Section 46.1.5 for CMC Mechanical Specifications | • Used for closed chassis debug through the USB port using an Intel® SVT Closed Chassis Adapter (CCA):<br>— support processor run control<br>— support Intel® AET/IOT tracing<br>— support Sx state/ME debug<br>— source level debug<br>— Might support Intel® Silicon View Technology (Intel® SVT) based HVM manufacturing test solution. Refer with your HVM test tool vendor.<br><br>• Used for open chassis debug using an ITP or similar JTAG debugger,<br>— support processor run control<br>— support Intel® AET/IOT tracing<br>— support Sx state/ME debug<br>— source level debug<br>— support Intel® Silicon View Technology (Intel® SVT) based HVM manufacturing test solution. Refer with your HVM test tool vendor for the exact tool usage model.<br><br>• Used for Intel® Silicon View Technology (Intel® SVT) based HVM and boundary scan manufacturing testing.<br><br>***Note:*** This is the preferred debug port routing options on most boards.<br><br>CMC is recommended for use as secondary debug port because it requires less routing onboard and takes up less board space.<br><br>Refer with your Intel representative if your HVM test tool required a Single Scan Chain (aka Common JTAG) support. Most Intel enabled JTAG test tool can support dual scan chain topology. |
| **Option 2:**<br><br>Intel Direct Connect Interface (DCI) over existing USB port<br>Bare minimum routing with no connector on board. | Refer Section 46.1.3 for connector less routing requirement. and specification<br><br>(Add in reference to Intel DCI section) | • Can only support closed chassis debug through the USB port using an Intel® SVT Closed Chassis Adapter. (Refer above for features)<br><br>• Used for Intel® Silicon View Technology (Intel® SVT) based HVM and boundary scan manufacturing testing<br><br>***Note:*** Intel does not recommend this option for development board. It should only be considered for board that does not have board space to route traces to a primary CMC connector or for a production board when debug is no longer needed.<br>Intel strongly recommends placing at least a primary CMC on the board. |

## 46.1.1 Primary Debug Port Debug Port Routing Guidelines

Unless otherwise indicated, routing guidelines in this section apply to both primary XDP and primary CMC connectors.

### 46.1.1.1 Primary Debug Port: Dual JTAG Scan Chain Only Topology

JTAG Topology in this section supports only Dual TCKs Scan Chain (aka Shared JTAG) covering the CPU and PCH components. This is a typical JTAG routing for Coffee Lake Platforms. This topology can not support HVM test tool or any JTAG debugger that requires both processor and PCH JTAG in a single scan chain that is controlled by the same TCK.

Refer with your Intel representative and your HVM tool vendor if your HVM test tool required a Single Scan Chain (aka Common JTAG) support.

***Note:*** The resistor values used for the JTAG signals in this content are meant for ITP or Run control JTAG debugger only and are subject to change according to test/debug tool condition. For example, some third party JTAG test tools may not have enough drive strength to meet the input-threshold requirements of the Intel Silicon with the strong 50-Ω terminations required for the ITP debugger. Consult with your test tool vendor for the appropriate resistor value to use.

**Figure 46-1. Primary Debug Port-JTAG Topology for Dual Scan Chain Only Design**

## Figure 46-2. Primary Debug Port-JTAG Topology for Dual Scan Chain Only Design

## Table 46-3. Primary Debug Port - Dual Scan Chain Only Routing Guidelines (Sheet 1 of 3)

| Pin/Signal | Routing Rules |
|---|---|
| XDP_TCK0 | •Route from XDP_TCK0 to Coffee Lake PROC_TCK and JTAGX as shown in Figure 46-6.<br>— Make sure to fork the traces no more than 200ps (approx 1100 mil or 28mm) from XDP_TCK0 pin.<br>• Test Point Placement<br>— Must placed on secondary side<br>— Place to within 250ps of Coffee Lake PROC_TCK pin and within 200ps of termination.<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br>**PROC_TCK Termination: 51 Ω ±5% pull down to GND**<br>•Placed to within 200ps (approx 1100 min or 28mm) of Coffee Lake pins.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>•Any stub length on TCK trace can not be more than 200ps. The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: 3 x Trace Width<br>**Maximum Via count**: 4<br>**Maximum Trace length:** 1ns (roughly 6000 mil or 154 mm) [per segment, measure from XDP pin -> Coffee Lake pin]<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>• Ideally, TCK should be routed directly to the socket pin of each processor and then exit the via array to continue on to the termination resistor on the trace.<br>*Suggestion:* Provide a scope test point at Coffee Lake breakout via to verify signal integrity of the first platforms.<br>**Refer to Section 46.1.8 for debug port depopulation rule.**<br>***Note:*** Note that some of the Intel reference designs might still have the JTAGX pull up. These pull up is only used to support Intel power-on, can be removed from the design. |
| XDP_TCK1 | •Route from XDP_TCK1 to Coffee Lake PCH_JTAG_TCK as shown in Figure 46-6.<br>• Test Point Placement<br>— Must placed on secondary side<br>— Place to within 250ps of Coffee Lake pin and within 200ps of termination.<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br>**Termination: 51 Ω ±5% pull down to GND**<br>•Placed to within 200ps (approx 1100 min or 28mm) of Coffee Lake pins.<br>•Leave EMPTY.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>•Any stub length on TCK trace can not be more than 200ps. The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: 3 x Trace Width<br>**Maximum Via count: 4**<br>**Maximum Trace length: 1ns (roughly 6000 mil or 154mm)**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>• Ideally, TCK should be routed directly to the socket pin of each processor and then exit the via array to continue on to the termination resistor on the trace.<br>•*Suggestion:* Provide a scope test point at Coffee Lake breakout via to verify signal integrity of the first platforms.<br>**Refer to Section 46.1.8 for debug port depopulation rule.** |

## Table 46-3. Primary Debug Port - Dual Scan Chain Only Routing Guidelines (Sheet 2 of 3)

| Pin/Signal | Routing Rules |
|---|---|
| XDP_TMS | •Route from XDP_TMS to Coffee Lake PROC_TMS and PCH_JTAG_TMS as shown in Figure 46-6.<br>— Make sure to fork the traces no more than 200ps (approx 1100 mil or 28mm) from XDP_TMS pin.<br>• Test Point Placement<br>— Must placed on secondary side<br>— Place to within 250ps of Coffee Lake pin and within 200ps of termination.<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br>**Termination: 51 Ω ±5% pull up to VCCSTG or equivalent**<br>•Placed to within 200ps (approx. 1100 min or 28mm) of Coffee Lake PCH_JTAG_TMS pin [note: PROC_TMS has on-die termination].<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>•Any stub length on this trace can not be more than 200ps. The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: No limit, but at least 2x trace width when possible<br>**Maximum Via count**: No limit, but should minimize whenever possible<br>**Maximum Trace length: 1ns (roughly 6000 mil or 154mm)** [for each segment, measures from XDP->Coffee Lake pin]<br>**Length Matching: matching to +/- 270 mil (6.85mm) of TCK**<br>— Match PROC_TMS net to PROC_TCK net<br>— Match PCH_JTAG_TMS to PCH_JTAG_TCK net<br>— Length matching is recommended but it is optional [Note: Length matching to TCK might allow operating at higher TCK frequency]<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>• Ideally, TMS will be routed directly to the socket pin of each processor and then exit the via array to continue on to the termination resistor on the trace.<br>*Suggestion:* Provide a scope test point at Coffee Lake breakout via to verify signal integrity of the first platforms.<br>**Refer to Section 46.1.8 for debug port depopulation rule.** |
| XDP_TRSTn | •Route daisy chain from XDP_TRSTn to Coffee Lake PROC_TRST# and PCH_TRST# as shown in Figure 46-6.<br>• Test Point Placement<br>— Must placed on secondary side<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br>**Termination: None**<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>**Trace-to-Trace spacing**: No limit. At least 1x trace width when possible<br>**Maximum Via count**: No limit. Should minimize whenever possible<br>**Maximum Trace length: 2.5ns (roughly 15000 mil or 381mm)**<br>**Length Matching: None**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.**<br>***Note:*** Note that some of the Intel reference designs might still have the XDP_TRSTn pull down. These pull down is only used to support Intel power-on, can be removed from the design. |

## Table 46-3. Primary Debug Port - Dual Scan Chain Only Routing Guidelines (Sheet 3 of 3)

| Pin/Signal | Routing Rules |
|---|---|
| XDP_TDI | •Route from XDP_TDI to Coffee Lake PROC_TDI and PCH_JTAG_TDI as shown in Figure 46-6.<br>— Make sure to fork the traces no more than 200ps (approx 1100 mil or 28mm) from XDP_TDI pin.<br>• Test Point Placement<br>— Must placed on secondary side<br>— Place to within 250ps of Coffee Lake pin and within 200ps of termination.<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br>**Termination: 51 Ω ±5% pull up to VCCSTG or equivalent**<br>•Placed to within 200ps (approx 1100 min or 28mm) of PCH_JTAG_TDI pin [Note: PROC_TDI has on-die termination].<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>•The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: No limit, At least 1x trace width when possible<br>**Maximum Via count**: No limit, Should minimize whenever possible<br>**Maximum Trace length: 1ns (roughly 6000 mil or 154mm)** [For each segment, measures from XDP->Coffee Lake pin]<br>**Length Matching: matching to +/- 270 mil (6.85mm) of TCK**<br>— Match PROC_TDI net to PROC_TCK net<br>— Match PCH_JTAG_TDI to PCH_JTAG_TCK net<br>— Length matching is recommended but it is optional [Note: Length matching to TCK might allow operating at higher TCK frequency]<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** |
| XDP_TDO | •Route from XDP_TDO to Coffee Lake PROC_TDO and PCH_JTAG_TDO as shown in Figure 46-6.<br>— Make sure to fork the traces no more than 200ps (approx 1100 mil or 28mm) from XDP_TDO pin.<br>• Test Point Placement<br>— Must placed on secondary side<br>— Place to within 250ps of Coffee Lake pin and within 200ps of termination.<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br>**Termination: 100 Ω ±5% pull up to VCCSTG or equivalent**<br>•Placed to within 200ps (approx 1100 min or 28mm) of each Coffee Lake pin.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>•Any stub length on this trace can not be more than 200ps. The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: No limit. At least 1x trace width when possible<br>**Maximum Via count**: No limit. Should minimize whenever possible<br>**Maximum Trace length: 1ns (roughly 6000 mil or 154mm)** [For each segment, measures from XDP->Coffee Lake pin]<br>**Length Matching: matching to +/- 270 mil (6.85mm) of TCK**<br>— Match PROC_TDO net to PROC_TCK net<br>— Match PCH_JTAG_TDO to PCH_JTAG_TCK net<br>— Length matching is recommended but it is optional [Note: Length matching to TCK might allow operating at higher TCK frequency]<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** |

### 46.1.1.2 Primary Debug Port: Observation Ports (CFG[0:19]) and PREQ#/ PRDY# pins Routing Guidelines

Both XDP and CMC connector has defined 16 observation data signals (OBSDATA ports) and specialized signal ports (4 pairs OBS_FN for XDP or 2 pairs OBS_CLK for CMC).

**Figure 46-3. Primary Debug Port: Observation Ports routing**

** A value of 1.5kohm has worked in Intel designs.*
*** BPM1:0]# can be left as Non Connect (NC) on OxM board with CMC connector. It is used by Intel to debug when need to*

*-TP = Test Point Pad (size - 18 mil min, 25 mil preferred)*

## Figure 46-4. Primary Debug Port: Observation Ports Routing

** A value of 1.5kohm has worked in Intel designs.*
*** BPM1:0]# can be connected to a Test point or test resistor pad on OxM board with CMC connector. It is used by Intel to debug.*

*-PREQ# and PRDY# stub length (S) should be less than 200ps (1100mil or 28mm)*

*-TP = Test Point Pad (size - 18 mil min, 25 mil preferred)*

## Table 46-4. Primary Debug Port - Observation Pins Routing Guidelines (Sheet 1 of 3)

| Pin/Signal | Routing Rules |
|---|---|
| XDP:<br>OBSFN_A[0]<br>OBSFN_A[1]<br><br>CMC:<br>XDP_PREQ#<br>XDP_PRDY# | • Route these signals to Coffee Lake Signals point-to-point according to Figure 46-8:<br>— Route XDP OBSFN_A[0] or CMC XDP_PREQ# to Coffee Lake PROC_PREQ#<br>— Route XDP OBSFN_A[1] or CMC XDP_PRDY# to Coffee Lake PROC_PRDY#<br>—<br>• Test Point Placement<br>— Must placed on secondary side<br>— Place to within 250ps of each Coffee Lake pin.<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br><br>**Termination: None**<br>**Stub length: 200ps (approx. 1100 mil or 28mm).** The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: No limit. At least 1xTrace Width when possible<br>**Maximum Via count**: No limit. Should minimize whenever possible<br>**Maximum Trace length: 2ns (roughly 12000 mil or 308mm)**<br>**Length Matching: None**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** |

## Table 46-4. Primary Debug Port - Observation Pins Routing Guidelines (Sheet 2 of 3)

| Pin/Signal | Routing Rules |
|---|---|
| XDP:<br>OBSDATA_A[2:0],<br>OBSDATA_B[3:0]<br>OBSDATA_C[3:0]<br>OBSDATA_D[3:0]<br><br>or<br><br>CMC:<br>OBSDATA_[15:0] | • Route these signals to Coffee Lake Signals point-to-point according to Figure 46-9:<br>**XDP:**<br>— Route OBSDATA_A[0] to Coffee Lake CFG[0].<br>— Route OBSDATA_A[1] to Coffee Lake CFG[1].<br>— Route OBSDATA_A[2] to Coffee Lake CFG[2].<br>— Route OBSDATA_A[3] to Coffee Lake CFG[3].<br>— Route OBSDATA_B[0] to Coffee Lake CFG[4].<br>— Route OBSDATA_B[1] to Coffee Lake CFG[5].<br>— Route OBSDATA_B[2] to Coffee Lake CFG[6].<br>— Route OBSDATA_B[3] to Coffee Lake CFG[7].<br>— Route OBSDATA_C[0] to Coffee Lake CFG[8].<br>— Route OBSDATA_C[1] to Coffee Lake CFG[9].<br>— Route OBSDATA_C[2] to Coffee Lake CFG[10].<br>— Route OBSDATA_C[3] to Coffee Lake CFG[11].<br>— Route OBSDATA_D[0] to Coffee Lake CFG[12].<br>— Route OBSDATA_D[1] to Coffee Lake CFG[13].<br>— Route OBSDATA_D[2] to Coffee Lake CFG[14].<br>— Route OBSDATA_D[3] to Coffee Lake CFG[15].<br>**CMC:**<br>— Route pin1/OBSDATA_0 to Coffee Lake CFG[0].<br>— Route pin3/OBSDATA_1 to Coffee Lake CFG[1].<br>— Route pin5/OBSDATA_2 to Coffee Lake CFG[2].<br>— Route pin7/OBSDATA_3 to Coffee Lake CFG[3].<br>— Route pin9/OBSDATA_4 to Coffee Lake CFG[4].<br>— Route pin11/OBSDATA_5 to Coffee Lake CFG[5].<br>— Route pin13/OBSDATA_6 to Coffee Lake CFG[6].<br>— Route pin15/OBSDATA_7 to Coffee Lake CFG[7].<br>— Route pin2/OBSDATA_8 to Coffee Lake CFG[8].<br>— Route pin4/OBSDATA_9 to Coffee Lake CFG[9].<br>— Route pin6/OBSDATA_10 to Coffee Lake CFG[10].<br>— Route pin8/OBSDATA_11 to Coffee Lake CFG[11].<br>— Route pin10/OBSDATA_12 to Coffee Lake CFG[12].<br>— Route pin12/OBSDATA_13 to Coffee Lake CFG[13].<br>— Route pin14/OBSDATA_14 to Coffee Lake CFG[14].<br>— Route pin16/OBSDATA_15 to Coffee Lake CFG[15].<br><br>• Test Point Placement (CFG[3])<br>— Must placed on secondary side<br>— Place to within 250ps of each Coffee Lake pin.<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br><br>CFG[3] also needs to refer to Section 46.1.1.3.1 for additional routing guidelines.<br>**Termination: None**<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**. The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: No limit, but 2x trace width when possible<br>**Maximum Via count**: No limit, but should minimize whenever possible<br>**Maximum Trace length: 2ns (roughly 12000 mil or 305mm)** [For each segment, measures from XDP OBS pin ->Coffee Lake pin]<br>**Length Matching: within +/- 270 mil (6.85mm) of CFG[17]**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.**<br>***Note:*** Note that some of the Intel reference designs might connect CFG[0] to HOOK[2]. This route is not needed on OxM board. |

## Table 46-4. Primary Debug Port - Observation Pins Routing Guidelines (Sheet 3 of 3)

| Pin/Signal | Routing Rules |
|---|---|
| XDP:<br>OBSFN_C[0]<br>OBSFN_C[1]<br>OBSFN_D[0]<br>OBSFN_D[1]<br><br>CMC:<br>OBS_CLK_1P<br>OBS_CLK_1N<br>OBS_CLK_2P<br>OBS_CLK_2N | • Route these signals to Coffee Lake Signals point-to-point according to Figure 46-8:<br>— Route XDP OBSFN_C0 or CMC OBS_CLK_1P to Coffee Lake CFG[17].<br>— Route XDP OBSFN_C1 or CMC OBS_CLK_1N to Coffee Lake CFG[16].<br>— Route XDP OBSFN_D0 or CMC OBS_CLK_2P to Coffee Lake CFG[19].<br>— Route XDP OBSFN_D1 or CMC OBS_CLK_2N to Coffee Lake CFG[18].<br><br>**Termination: None**<br>**Stub length: 200ps (approx. 1100 mil or 28mm).** The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: 3 x Trace Width<br>**Maximum Via count**: 4<br>**Maximum Trace length: 2ns (roughly 12000 mil or 305mm)**<br>**Length Matching: within +/- 270 mil (6.85mm) of CFG[17]**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** |
| XDP Only:<br>OBSFN_B[1:0] | • Route these signals to Coffee Lake Signals according to Figure 46-8:<br>— Route OBSFN_B0 to Coffee Lake BPM#[0].<br>— Route OBSFN_B1 to Coffee Lake BPM#[1].<br><br>**Termination: None**<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>•Any stub length on this trace can not be more than 200ps. The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: No limit, but at least 1x trace width when possible<br>**Maximum Via count**: No limit, but should minimize whenever possible<br>**Maximum Trace length: 2ns (roughly 12000 mil or 305mm)**<br>**Length Matching: within +/- 270 mil (6.85mm) of each other**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** |
| XDP<br>Coffee Lake<br>BPM#[3:2]#<br><br>CMC:<br>Coffee Lake BPM#[3:0] | • Routed as test points or resistor pads on the platform.<br><br>***Note:*** The test points or pads must be placed in a location that is probe accessible (avoid location that is blocked by thermal solutions) so that Intel would be able to access them when debug by Intel is required.<br><br>**Refer to Section 46.1.8 for debug port depopulation rule.** |

### 46.1.1.3 Primary Debug Port HOOKs, SMBus, XDP_PRESENT_N, VCC_OBS and Ground Signals Routing Guidelines

This section describes Primary Debug port's HOOK/system control signals routing guidelines. Unless otherwise indicated, routing guidelines in this section apply to both primary XDP and primary CMC connectors.

**Figure 46-5. Primary Debug Port-HOOK, VCC_OBS signals Route Map**

**Figure 46-6. Primary Debug Port-HOOK, VCC_OBS signals Route Map**

## Table 46-5. Primary Debug Port - HOOK, VCC_OBS, SCL/SDA, Ground signals Routing (Sheet 1 of 4)

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| XDP Ground pins#2, 7, 8, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 49, 50, 59<br><br>CMC: Pin#19 | • Connect all of the XDP connector GND pins (except of XDP pin#1) directly to a GND plane through individual vias. Keep trace lengths on these connections to a minimum.<br>• Refer Section 46.1.1.3.1 for XDP pin# 1 routing Guidelines | |
| XDP:<br>VCC_OBS_AB<br>VCC_OBS_CD<br><br>CMC: VccOBS_AB | • Connect VCC_OBS_AB/ VccOBS_AB and VCC_OBS_CD to the PCH_1.0V A Rail or equivalent<br>• Minimum Trace Width: 10 mil (0.254mm)<br><br>***Note:*** The ITP probe will have an internal 220uF capacitor on each VCC_OBS rail. It is required to take this into account in the design of the Power Delivery Network in order to minimize voltage droops when hot-plugging the ITP. These droops are caused mainly by the in-rush currents needed to charge the two 220uF capacitors | |
| XDP/CMC:<br><br>HOOK[0] | • Route these signals to Coffee Lake Signals according to Figure 46-9:<br>— Route HOOK[0] to Coffee Lake RSMRST#.<br>— Places a 1K Ω 5% series resistor on the trace between processor XDP HOOK[0] and RSMRST# trace<br>— Consult RSMRST# topology and guidelines sections in this Platform Design Guide (PDG) for termination information and additional routing guidelines.<br><br>**Termination:** Consult RSMRST# topology and guidelines sections in this Platform Design Guide (PDG) for termination information and additional RSMRST# routing guidelines.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>**Trace-to-Trace spacing**: No limit for XDP. Consult RSMRST# routing guidelines for additional routing requirement.<br>**Maximum Via count**: No limit for XDP. Consult RSMRST# routing guidelines for additional routing requirement.<br>**Maximum Trace length: 2.5ns (roughly 15000 mil or 381mm)** [from XDP to Coffee Lake RSMRST# pin]<br>**Length Matching: None**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** | |

## Table 46-5. Primary Debug Port - HOOK, VCC_OBS, SCL/SDA, Ground signals Routing (Sheet 2 of 4)

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| XDP/CMC:<br><br>HOOK[3] | • Route these signals to Coffee Lake Signals according to Figure 46-9:<br>— Route HOOK[3] to the strapping resistor (Rstrap) connecting to Coffee Lake SPIO_MOSI pin and other device (if any) SPIO_MOSI.<br>— Rstrap need to be place to within 200ps (1100 mil or 28mm) of the T-point connection to main SPI0_MOSI trace.<br>— Resistor RStrap value is platform dependent. A value of 1.5kΩ has worked in Intel designs. Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for the SPIO_MOSI Rstrap value and additional routing guidelines.<br>**Termination:** Resistor can be value from 1K to 3K Ω pull up to voltage value from 0.8V-3.3V.<br>• Place termination between XDP/CMC and Rstrap. it should be within 200ps of debug port HOOK[3] pin.<br>• Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for the SPIO_MOSI termination value and additional routing guidelines.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>•Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_MOSI routing guidelines.<br>**Trace-to-Trace spacing**: No limit for XDP. Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_MOSI routing guidelines.<br>**Maximum Via count**: No limit for XDP. Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_MOSI routing guidelines.<br>**Maximum Trace length:** Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_MOSI routing guidelines.<br>**Length Matching:** Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for the SPIO_MOSI termination value and additional routing guidelines<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** | |
| HOOK[6] | • Route these signals to Coffee Lake Signals according to Figure 46-9:<br>— Route HOOK[6] to Coffee Lake ITP_PMODE.<br>**Termination:** Resistor value from 1K Ω to 3K Ω pull up to PCH_V1.0A Rail.<br>— Place termination to within 200ps (approx 1100 or 28mm) of XDP/CMC HOOK[6] pin.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>•Any stub length on this trace can not be more than 200ps. The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: No limit.<br>**Maximum Via count**: No limit, should be minimize whenever possible.<br>**Maximum Trace length: 2ns (roughly 12000 mil or 305mm)** [from XDP to Coffee Lake pin]<br>**Length Matching: None**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** | |

## Table 46-5. Primary Debug Port - HOOK, VCC_OBS, SCL/SDA, Ground signals Routing (Sheet 3 of 4)

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| XDP:<br>HOOK[1] | • Route these signals to Coffee Lake Signals according to Figure 46-9:<br>— Route HOOK[1] to Coffee Lake PWRBTN# or board Reset Logic controlling the system power button.<br>— Provide a pull up (resistor range from 150 to 3K Ω and pull up voltage range from 0.8V to 3.3V can be driven by ITP) on this connection<br>- Note that only one pull up is needed when there are multiple XDP HOOK[1] connections.<br>— Place a capacitor (value can be range from 2.2nF to 0.1uF) pull down to ground to within 200ps (approx 1100 or 28mm) of XDP HOOK[1] pin.<br>**Termination:** consult PWRBTN# routing guidelines for exact termination values and additional routing requirement.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>**Trace-to-Trace spacing**: No limit for XDP. Consult PWRBTN# routing guidelines for additional routing requirement.<br>**Maximum Via count**: No limit for XDP. Consult PWRBTN# routing guidelines for additional routing requirement.<br>**Maximum Trace length: 2.7ns (roughly 16100 mil or 409mm)**<br>**Length Matching: None**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** | |
| XDP:<br>HOOK[2] | • This XDP pin should be left as No Connect (NC)<br>***Note:*** Some Intel Reference Design might connect HOOK[2] to CFG[0]. HOOK[2] routing is only required for Intel debug, its routing is OPTIONAL. | |
| XDP only:<br>HOOK[4],<br>HOOK[5] | • Route these signals to Coffee Lake Signals according to Figure 46-9:<br>— Route HOOK[4] point-to-point to Coffee Lake CLKOUT_ITPXDP_P.<br>— Route HOOK[5] point-to-point to Coffee Lake CLKOUT_ITPXDP_N.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>**Trace-to-Trace spacing**: No limit. At least 1 x Trace Width when possible.<br>**Maximum Via count**: No limit. Should be minimize whenever possible.<br>**Maximum Trace length: 2.5ns (roughly 15000 mil or 381mm)**<br>**Length Matching: within +/- 10 mil (0.25mm) of each other**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.**<br>***Note:*** Route of HOOK[4] and HOOK[5] is Optional. They can be left No Connect (NC) on a OxM board. | |

## Table 46-5. Primary Debug Port - HOOK, VCC_OBS, SCL/SDA, Ground signals Routing (Sheet 4 of 4)

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| XDP:<br>HOOK[7] | • Route these signals to Coffee Lake Signals according to Figure 46-9:<br>— Route HOOK[7] to Coffee Lake SYS_RESET# or board Reset Logic capable of initiating a warm Reset cycle.<br>— Provide a pull up (resistor range from 150 to 3K Ω and pull up voltage range from 0.8V to 3.3V can be driven by ITP) on this connection<br>- Note that only one pull up is needed when there are multiple XDP HOOK[7] connections.<br>— Place a capacitor (value can be range from 2.2nF to 0.1uF) pull down to ground to within 200ps (approx 1100 or 28mm) of XDP HOOK[7] pin.<br>**Termination:** Consult Section 30.2.1, "SYS_RESET# Usage Model" for termination values and additional routing requirement.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**. The stub length should be minimized whenever possible.<br>**Trace-to-Trace spacing**: No limit for XDP. Consult SYS_RESET# routing guidelines for additional routing requirement.<br>**Maximum Via count**: No limit for XDP. Consult SYS_RESET# routing guidelines for additional routing requirement.<br>**Maximum Trace length: 2.7ns (roughly 16100 mil or 409mm)**<br>**Length Matching: None**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** | |
| XDP:<br>SCL/SDA | • $I^2C$*/SMBus is Optional connection for XDP.<br>• If connected;<br>— Route the debug-port SDA pin to the SDA signal of the SMBus on the system.<br>— Route the debug port SCL pin to the SCL signal of the SMBus on the system.<br>— provide the pull ups and follow the routing guidelines according to Section 33.3.5, "SMBus and $I^2C$ Topology Guidelines" in this guide. | |

#### 46.1.1.3.1 Primary Debug Port XDP_PRESENT# Routing Guidelines

This section describes XDP_PRESENT# connectivity of primary debug port.

**Figure 46-7. Primary Debug Port-XDP_PRESENT# Connectivity**

***Note:*** Refer to Section 46.1.8 for debug port depopulation rule.

## Figure 46-8. Primary Debug Port-XDP_PRESENT# Connectivity

***Note:*** Refer to Section 46.1.8 for debug port depopulation rule.

## Table 46-6. Primary Debug Port - XDP_PRESENT Routing Guidelines (Sheet 1 of 2)

| Signal (pin#) | Routing Rules | Notes |
|---|---|---|
| XDP:<br>XDP_pin# 1 (pin# 1)<br><br>CMC:<br>XDP_PRESENT_CPU (pin# 23) | • Route these signals to Coffee Lake pin according to Figure 46-11:<br>— Route XDP pin# 1 or CMC XDP_PRESENT_CPU pin to Coffee Lake CFG[3]<br>— Places Rstrap resistor on the trace between debug port pin and CFG[3].<br>— Rstrap should be placed to within 100ps (500 mil or 12.5 mm) of the T-point connection to main CFG[3] trace.<br>— Check Section 49.3.27, "Processor Strapping" for CFG[3] Rstrap value.<br>— NOTE: Consult Section 46.1.1.2, "Primary Debug Port: Observation Ports (CFG[0:19]) and PREQ#/PRDY# pins Routing Guidelines" for additional CFG[3] routing guidelines.<br>**Stub length: 200ps (approx. 1100 mil or 28mm)**<br>**Trace-to-Trace spacing**: No limit for XDP_PRESENT signals.<br>**Maximum Via count**: No limit for XDP. should be minimized whenever possible.<br>**Maximum Trace length: 2ns (roughly 12000 mil or 305mm)** [measure from debug Port pin#1 to CFG[3]].<br>**Length Matching:** None for XDP_PRESENT_CPU or XDP pin#1. Refer Section 46.1.1.2 for CFG[3] length matching rule.<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br>**Refer to Section 46.1.8 for debug port depopulation rule.** | |

### Table 46-6. Primary Debug Port - XDP_PRESENT Routing Guidelines (Sheet 2 of 2)

| Signal (pin#) | Routing Rules | Notes |
|---|---|---|
| XDP:<br>XDP_PRESENT#<br>(pin# 60)<br><br>CMC:<br>XDP_PRESENT_PCH<br>(pin#24) | • Route these signals to Coffee Lake Signals according to Figure 46-11:<br>— Route XDP XDP_PRESENT# or CMC XDP_PRESENT_PCH pin to Coffee Lake SPIO_IO2 pin.<br>— Rstrap should be placed to within 100ps (500 mil or 12.5 mm) of the T-point connection to main SPI0_IO2 trace.<br>— Consult section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for the SPIO_IO2 Rstrap value and additional SPIO_IO2 routing guidelines.<br><br>• Test Point Placement (SPIO_IO2)<br>— Must be placed on secondary side<br>— Place to within 250ps of Coffee Lake pin.<br>— Pad size: Minimum 18mil, Preferred pad size 25 mil<br>— Refer section Section 46.1.7 for additional routing requirement to support Intel® Silicon View Technology DFM HVM solution<br><br>**Stub length: 200ps (approx. 1100 mil or 28mm).** Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_IO2 routing guidelines.<br><br>**Trace-to-Trace spacing**: No limit for debug port. Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_IO2 routing guidelines<br><br>**Maximum Via count**: No limit for debug port. Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_IO2 routing guidelines<br><br>**Maximum Trace length:** Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_IO2 routing guidelines<br><br>**Length Matching:** Consult Section 24.2, "Serial Peripheral Interface (SPI) Topology Guidelines" for additional SPIO_IO2 routing guidelines.<br><br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.**<br><br>**Refer to Section 46.1.8 for debug port depopulation rule.** | |

### 46.1.1.4 Primary XDP Connector Pin Out

Table 46-7 documents the pinout of Primary XDP connector.

### Table 46-7. Primary XDP Connector Pinout (Sheet 1 of 2)

| Pin | XDP Signal Name | Target Signal | I/O | Device | Pin | XDP Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 1 | XDP Pin#1[2] | Refer XDP_PRESENT# routing guidelines | NA | Coffee Lake | 2 | GND | GND | NA | |
| 3 | OBSFN_A0 | PROC_PREQ# | O | Coffee Lake | 4 | OBSFN_C0 | CFG(17) | I | Coffee Lake |
| 5 | OBSFN_A1 | PROC_PRDY# | I | Coffee Lake | 6 | OBSFN_C1 | CFG(16) | I | Coffee Lake |
| 7 | GND | GND | NA | | 8 | GND | GND | NA | |
| 9 | OBSDATA_A0 | CFG[0] | I/O | Coffee Lake | 10 | OBSDATA_C0 | CFG[8] | I/O | Coffee Lake |
| 11 | OBSDATA_A1 | CFG[1] | I/O | Coffee Lake | 12 | OBSDATA_C1 | CFG[9] | I/O | Coffee Lake |
| 13 | GND | GND | NA | | 14 | GND | GND | NA | |
| 15 | OBSDATA_A2 | CFG[2] | I/O | Coffee Lake | 16 | OBSDATA_C2 | CFG[10] | I/O | Coffee Lake |
| 17 | OBSDATA_A3 | CFG[3] | I/O | Coffee Lake | 18 | OBSDATA_C3 | CFG[11] | I/O | Coffee Lake |
| 19 | GND | GND | NA | | 20 | GND | GND | NA | |
| 21 | OBSFN_B0 | BPM#[0] | I/O | Coffee Lake | 22 | OBSFN_D0 | CFG(19) | I | Coffee Lake |

## Table 46-7. Primary XDP Connector Pinout (Sheet 2 of 2)

| Pin | XDP Signal Name | Target Signal | I/O | Device | Pin | XDP Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 23 | OBSFN_B1 | BPM#[1] | I/O | Coffee Lake | 24 | OBSFN_D1 | CFG(18) | I | Coffee Lake |
| 25 | GND | GND | NA | | 26 | GND | GND | NA | |
| 27 | OBSDATA_B0 | CFG[4] | I/O | Coffee Lake | 28 | OBSDATA_D0 | CFG[12] | I/O | Coffee Lake |
| 29 | OBSDATA_B1 | CFG[5] | I/O | Coffee Lake | 30 | OBSDATA_D1 | CFG[13] | I/O | Coffee Lake |
| 31 | GND | GND | NA | | 32 | GND | GND | NA | |
| 33 | OBSDATA_B2 | CFG[6] | I/O | Coffee Lake | 34 | OBSDATA_D2 | CFG[14] | I/O | Coffee Lake |
| 35 | OBSDATA_B3 | CFG[7] | I/O | Coffee Lake | 36 | OBSDATA_D3 | CFG[15] | I/O | Coffee Lake |
| 37 | GND | GND | NA | | 38 | GND | GND | NA | |
| 39 | HOOK0 | RSMRST# | I | Coffee Lake | 40 | ITPCLK/HOOK4[1] | CLKOUT_ITPXDP_P | I | Coffee Lake |
| 41 | HOOK1 | PWRBTN# | O | Coffee Lake | 42 | ITPCLK#/HOOK5 | CLKOUT_ITPXDP_N | I | Coffee Lake |
| 43 | VCC_OBS_AB | PCH V1.0A | NA | | 44 | VCC_OBS_CD | PCH V1.0A | NA | |
| 45 | HOOK2[3] | Open | NA | | 46 | HOOK6/RESET# | ITP_PMODE | I | Coffee Lake |
| 47 | HOOK3[1] | SPIO_MOSI | O | Coffee Lake | 48 | HOOK7/DBR# | SYS_RESET# | O | Coffee Lake |
| 49 | GND | GND | NA | | 50 | GND | GND | NA | |
| 51 | XDP_SDA[1] | SDA | I/O | system | 52 | XDP_TDO | PROC_TDO / PCH_JTAG_TDO | I | Coffee Lake |
| 53 | XDP_SCL[1] | SCL | I/O | system | 54 | XDP_TRSTn | PROC_TRST#/ PCH_TRST# | O | Coffee Lake |
| 55 | XDP_TCK1 | PCH_JTAG_TCK | O | Coffee Lake | 56 | XDP_TDI | PROC_TDI / PCH_JTAG_TDI | O | Coffee Lake |
| 57 | XDP_TCK0 | PROC_TCK / JTAGX | O | Coffee Lake | 58 | XDP_TMS | PROC_TMS / PCH_JTAG_TMS | O | Coffee Lake |
| 59 | GND | GND | NA | | 60 | GND[2] (XDP_PRESENT#) | Refer XDP_PRESENT# routing guidelines | NA | system |

***Notes:***
1. These signals are optional, can be left as OPEN/No-Connect.
2. Refer XDP_PRESENT# section for additional routing guidelines.
3. Routing of this signal to CFG[0] is OPTIONAL.



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#### 46.1.1.5 Primary CMC Pin Out

Table 46-8 documents the pinout of Primary CMC connector.

**Table 46-8. Primary CMC Connector Pinout**

| Pin | CMC Signal Name | Target Signal | I/O | Device | Pin | CMC Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 1 | OBSDATA_0 | CFG[0] | I/O | Coffee Lake | 2 | OBSDATA_8 | CFG[8] | I/O | Coffee Lake |
| 3 | OBSDATA_1 | CFG[1] | I/O | Coffee Lake | 4 | OBSDATA_9 | CFG[9] | I/O | Coffee Lake |
| 5 | OBSDATA_2 | CFG[2] | I/O | Coffee Lake | 6 | OBSDATA_10 | CFG[10] | I/O | Coffee Lake |
| 7 | OBSDATA_3 | CFG[3] | I/O | Coffee Lake | 8 | OBSDATA_11 | CFG[11] | I/O | Coffee Lake |
| 9 | OBSDATA_4 | CFG[4] | I/O | Coffee Lake | 10 | OBSDATA_12 | CFG[12] | I/O | Coffee Lake |
| 11 | OBSDATA_5 | CFG[5] | I/O | Coffee Lake | 12 | OBSDATA_13 | CFG[13] | I/O | Coffee Lake |
| 13 | OBSDATA_6 | CFG[6] | I/O | Coffee Lake | 14 | OBSDATA_14 | CFG[14] | I/O | Coffee Lake |
| 15 | OBSDATA_7 | CFG[7] | I/O | Coffee Lake | 16 | OBSDATA_15 | CFG[15] | I/O | Coffee Lake |
| 17 | OBS_CLK_1P | CFG[17] | I | Coffee Lake | 18 | OBS_CLK_2P | CFG[19] | I | Coffee Lake |
| 19 | GND | GND | NA | | 20 | OBS_CLK_2N | CFG[18] | I | Coffee Lake |
| 21 | OBS_CLK_1N | CFG[16] | I | Coffee Lake | 22 | VCCOBS_AB | PCH V1.0 A | NA | |
| 23 | XDP_PRESENT_CPU# | Refer XDP_PRESEN# section | NA | system | 24 | XDP_PRESENT_PCH# | Refer XDP_PRESENT # section | NA | System |
| 25 | HOOK[3] | SPI_MOSI | O | Coffee Lake | 26 | HOOK[6] | ITP_PMODE | I | Coffee Lake |
| 27 | HOOK[0] | RSMRST# | I | Coffee Lake | 28 | XDP_TRSTn | PROC_TRST# / PCH_TRST# | O | Coffee Lake |
| 29 | XDP_TDI | PROC_TDI / PCH_JTAG_TDI | O | Coffee Lake | 30 | XDP_TMS | PROC_TMS / PCH_JTAG_TMS | O | Coffee Lake |
| 31 | XDP_TCK1 | PCH_JTAG_TCK | O | Coffee Lake | 32 | XDP_TCK0 | PROC_TCK / JTAGX | O | Coffee Lake |
| 33 | XDP_PREQ# | PROC_PREQ# | O | Coffee Lake | 34 | XDP_PRDY# | PROC_PRDY# | I | Coffee Lake |
| 35 | XDP_TDO | PROC_TDO / PCH_JTAG_TDO | I | Coffee Lake | | | | | |

## 46.1.2 Secondary Debug Port Routing Guidelines

Unless otherwise indicated, routing guidelines in this section apply to both secondary XDP and secondary CMC connectors.

JTAG pins, HOOK pins, XDP_PRESENT#, VCCOBS pins, SCL/SDA pins of this secondary debug port can be left as No connect (NC) unless indicated otherwise.

#### 46.1.2.1 Secondary Debug Port Observation Ports Routing Guidelines

The XDP connector has defined four separate observation ports (OBS ports) named A through D. Each port contains four data signals (OBS_DATA), and two specialized signals (OBS_FN). Likewise, CMC has defined 16 OBS data pins (OBSDATA) and 2 set of OBS Clock pins (OBS_CLK_[1:2]P/N).

The Coffee Lake Chipset Test Interface signals are used by Intel when debugging customer platforms. There are 18 PCH Chipset Test Interface signals; Those signals need to be routed to secondary XDP or CMC OBS pins according to Figure 46-9 and Table 46-9.

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## Table 46-9. Secondary Debug Port- OBS Pins Routing Requirements (Sheet 1 of 2)

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| XDP pins:<br>OBSDATA_A[3:0], OBSDATA_B[3:0],<br>OBSFN_C[1:0], OBSDATA_C[3:0], OBSDATA_D[3:0]<br><br>CMC: pins<br>OBSDATA _[0:18]<br>OBS_CLK_1P<br>OBS_CLK_2P | XDP:<br><br>•Route these OBS pins to Coffee Lake according to Figure 46-4:<br><br>**XDP:**<br>— Route OBSDATA_A[0] to PCH GPP_E1 / SATAXPCIE1 / SATAGP1<br>— Route OBSDATA_A[1] to PCH GPP_E2 / SATAXPCIE2 / SATAGP2<br>— Route OBSDATA_A[2] to PCH GPP_E3 / CPU_GP0<br>— Route OBSDATA_A[3] to PCH GPP_E4 / DEVSLP0<br>— Route OBSDATA_B[0] to PCH GPP_E5 / DEVSLP1<br>— Route OBSDATA_B[1] to PCH GPP_E6 / DEVSLP2<br>— Route OBSDATA_B[2] to PCH GPP_E7 / CPU_GP1<br>— Route OBSDATA_B[3] to PCH GPP_E8 / SATALED#<br>— Route OBSFN_C[0] to PCH GPP_E0 / SATAXPCIE0 / SATAGP0<br>— Route OBSFN_C[1] to PCH GPP_F4 / SATAXPCIE7 / SATAGP7<br>— Route OBSDATA_C[0] to PCH GPP_E9 / USB2_OC0#<br>— Route OBSDATA_C[1] to PCH GPP_E10 / USB2_OC1#<br>— Route OBSDATA_C[2] to PCH GPP_E11 / USB2_OC2#<br>— Route OBSDATA_C[3] to PCH GPP_E12 / USB2_OC3#<br>— Route OBSDATA_D[0] to PCH GPP_F0 / SATAXPCIE3 / SATAGP3<br>— Route OBSDATA_D[1] to PCH GPP_F1 / SATAXPCIE4 / SATAGP4<br>— Route OBSDATA_D[2] to PCH GPP_F2 / SATAXPCIE5 / SATAGP5<br>— Route OBSDATA_D[3] to PCH GPP_F3 / SATAXPCIE6 / SATAGP6<br>**CMC:**<br>— Route pin1/OBSDATA_0 to PCH GPP_E1 / SATAXPCIE1 / SATAGP1.<br>— Route pin3/OBSDATA_1 to PCH GPP_E2 / SATAXPCIE2 / SATAGP2<br>— Route pin5/OBSDATA_2 to PCH GPP_E3 / CPU_GP0<br>— Route pin7/OBSDATA_3 to PCH GPP_E4 / DEVSLP0<br>— Route pin9/OBSDATA_4 to PCH GPP_E5 / DEVSLP1<br>— Route pin11/OBSDATA_5 to PCH GPP_E6 / DEVSLP2<br>— Route pin13/OBSDATA_6 to PCH GPP_E7 / CPU_GP1<br>— Route pin15/OBSDATA_7 to PCH GPP_E8 / SATALED#<br>— Route pin17/OBS_CLK_1P to PCH GPP_E0 / SATAXPCIE0 / SATAGP0<br>— Route pin2/OBSDATA_8 to PCH GPP_E9 / USB2_OC0#<br>— Route pin4/OBSDATA_9 to PCH GPP_E10 / USB2_OC1#<br>— Route pin6/OBSDATA_10 to PCH GPP_E11 / USB2_OC2#<br>— Route pin8/OBSDATA_11 to PCH GPP_E12 / USB2_OC3#<br>— Route pin10/OBSDATA_12 to PCH GPP_F0 / SATAXPCIE3 / SATAGP3<br>— Route pin12/OBSDATA_13 to PCH GPP_F1 / SATAXPCIE4 / SATAGP4<br>— Route pin14/OBSDATA_14 to PCH GPP_F2 / SATAXPCIE5 / SATAGP5<br>— Route pin16/OBSDATA_15 to PCH GPP_F3 / SATAXPCIE6 / SATAGP6<br>— Route pin18/OBS_CLK_2P to PCH GPP_F4 / SATAXPCIE7 / SATAGP7<br><br>**Stub length: 200ps (approx. 1100mil or 28mm).** The stub length should be minimized whenever possible.<br>**Maximum Via count**: 4 for OBS_C[1:0]/OBS_CLK_[2,1]P signals, No limit of others.<br>**Length Matching: ±50ps (roughly 270mil or 6.85mm)**<br>•These group of signal must be length matched to ±50ps of flight time with respect to OBSFN_C[1] for XDP or OBSCLK_2P for CMC.<br>**Trace-To-Trace Spacing:**<br>•XDP: OBSFN_C[0:1]: 3 x Trace Width<br>•CMC: OBS_CLK_1P and OBS_CLK_2P: 3xTrace Width<br>•Others OBS signals have no trace spacing restriction. It is recommended; however, to keep at least 2xTrace Width when possible.<br>**Maximum Trace length: 2ns (roughly 12000mil or 305mm)**<br>**Refer to Section 46.1.6 for additional debug port PCB layout rules.** | |

**Table 46-9. Secondary Debug Port- OBS Pins Routing Requirements (Sheet 2 of 2)**

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| XDP pins:<br>OBSFN_A[1:0]<br>OBSFN_D[1:0]<br>OBSFN_B[1:0]<br><br>CMC: pins<br>OBS_CLK_1N,<br>OBS_CLK_2N | Leave these secondary debug port OBS pins as NO CONNECT (NC) | |

**Figure 46-9. Secondary Debug Port - PCH Chipset Test Interfaces**

Normal Operation: Stuff Rs 0 ohm resistor and unstuff Rd for standard usage of the signal.
Debug Usage: Stuff Rd 0 ohm, Unstuff Rs resistor when used as chipset test Interface signal with XDP/CMC.

**Note:** No need to provide 0 ohm resistor stuffing (Rs and Rd) or isolation mechanism on the trace between XDP/CMC OBS pin and Chipset Test Interface signal, if the PCH Chipset Test Interface signal will ONLY connect point-to-point to XDP OBS pin.

### 46.1.2.2 Secondary XDP HOOK0 Routing Guidelines

This routing guidelines apply only to Secondary XDP. For Secondary CMC, HOOK0 can be left as No Connect (NC).

Route XDP HOOK[0] to Coffee Lake RSMRST# pin as shown in Figure 46-9.

Follow the HOOK[0] routing rules in Table 46-5.

### 46.1.2.3 Secondary XDP VCCOBS_AB and VCCOBS_CD Routing Guidelines

This routing guidelines apply only to Secondary XDP. For Secondary CMC, VCCOBS_AB can be left as No Connect (NC).

Route point to point from XDP VCCOBS_AB and VCCOBS_CD to PCH_V1.0A rail or equivalent as shown in Figure 46-9.

Follow the routing rules of VCC_OBS_AB and VCC_OBS_CD in Table 46-5.

### 46.1.2.4 Secondary XDP Connector PinOut

Table below documents the pinout of Secondary XDP connector.

**Table 46-10. Secondary XDP Connector Pinout (Sheet 1 of 2)**

| Pin | XDP Signal Name | Target Signal | I/O | Device | Pin | XDP Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | GND | NA | | 2 | GND | GND | NA | |
| 3 | OBSFN_A0 | Open | NA | | 4 | OBSFN_C0 | GPP_E0 / SATAXPCIE0 / SATAGP0 | I | PCH |
| 5 | OBSFN_A1 | Open | NA | | 6 | OBSFN_C1 | GPP_F4 / SATAXPCIE7 / SATAGP7 | I | PCH |
| 7 | GND | GND | NA | | 8 | GND | GND | NA | |
| 9 | OBSDATA_A0 | GPP_E1 / SATAXPCIE1 / SATAGP1 | I | PCH | 10 | OBSDATA_C0 | GPP_E9 / USB2_OC0# | I | PCH |
| 11 | OBSDATA_A1 | GPP_E2 / SATAXPCIE2 / SATAGP2 | I | PCH | 12 | OBSDATA_C1 | GPP_E10 / USB2_OC1# | I | PCH |
| 13 | GND | GND | NA | | 14 | GND | GND | NA | |
| 15 | OBSDATA_A2 | GPP_E3 / CPU_GP0 | I | PCH | 16 | OBSDATA_C2 | GPP_E11 / USB2_OC2# | I | PCH |
| 17 | OBSDATA_A3 | GPP_E4 / DEVSLP0 | I | PCH | 18 | OBSDATA_C3 | GPP_E12 / USB2_OC3# | I | PCH |
| 19 | GND | GND | NA | | 20 | GND | GND | NA | |
| 21 | OBSFN_B0 | Open | NA | | 22 | OBSFN_D0 | Open | NA | |
| 23 | OBSFN_B1 | Open | NA | | 24 | OBSFN_D1 | Open | NA | |
| 25 | GND | GND | NA | | 26 | GND | GND | NA | |
| 27 | OBSDATA_B0 | GPP_E5 / DEVSLP1 | I | PCH | 28 | OBSDATA_D0 | GPP_F0 / SATAXPCIE3 / SATAGP3 | I | PCH |
| 29 | OBSDATA_B1 | GPP_E6 / DEVSLP2 | I | PCH | 30 | OBSDATA_D1 | GPP_F1 / SATAXPCIE4 / SATAGP4 | I | PCH |
| 31 | GND | GND | NA | | 32 | GND | GND | NA | |
| 33 | OBSDATA_B2 | GPP_E7 / CPU_GP1 | I | PCH | 34 | OBSDATA_D2 | GPP_F2 / SATAXPCIE5 / SATAGP5 | I | PCH |
| 35 | OBSDATA_B3 | GPP_E8 / SATALED# | I | PCH | 36 | OBSDATA_D3 | GPP_F3 / SATAXPCIE6 / SATAGP6 | I | PCH |
| 37 | GND | GND | NA | | 38 | GND | GND | NA | |

## Table 46-10. Secondary XDP Connector Pinout (Sheet 2 of 2)

| Pin | XDP Signal Name | Target Signal | I/O | Device | Pin | XDP Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 39 | HOOK0 | RSMRST# | I | PCH | 40 | ITPCLK/HOOK4[1] | Open | NA | |
| 41 | HOOK1 | Open | NA | | 42 | ITPCLK#/HOOK5 | Open | NA | |
| 43 | VCC_OBS_AB | PCH v1.0A | NA | system | 44 | VCC_OBS_CD | PCH v1.0A | NA | system |
| 45 | HOOK2 | Open | NA | | 46 | HOOK6/RESET# | Open | NA | |
| 47 | HOOK3[1] | Open | NA | | 48 | HOOK7/DBR# | Open | NA | |
| 49 | GND | GND | NA | | 50 | GND | GND | NA | |
| 51 | SDA[1] | Open | NA | | 52 | TDO | Open | NA | |
| 53 | SCL[1] | Open | NA | | 54 | TRSTn | Open | NA | |
| 55 | TCK1 | Open | NA | | 56 | TDI | Open | NA | |
| 57 | TCK0 | Open | I | | 58 | TMS | Open | NA | |
| 59 | GND | GND | NA | | 60 | GND[2] (XDP_PRESENT#) | GND | NA | |

***Notes:***
1. These signals are optional, can be left as OPEN/No-Connect.
2. Connect pin 60 to GND when it is not used to indicate the presence of ITP-XDP style tool.

## Table 46-11. Secondary XDP Connector Pinout (Sheet 1 of 2)

| Pin | XDP Signal Name | Target Signal | I/O | Device | Pin | XDP Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | GND | NA | | 2 | GND | GND | NA | |
| 3 | OBSFN_A0 | Open | NA | | 4 | OBSFN_C0 | GPP_E12 / USB2_OC3# | I | Coffee Lake |
| 5 | OBSFN_A1 | Open | NA | | 6 | OBSFN_C1 | GPP_E3 / CPU_GP0 | I | Coffee Lake |
| 7 | GND | GND | NA | | 8 | GND | GND | NA | |
| 9 | OBSDATA_A0 | GPP_E4 / DEVSLP0 | I | Coffee Lake | 10 | OBSDATA_C0 | GPP_D17 / DMIC_CLK1 | I | Coffee Lake |
| 11 | OBSDATA_A1 | GPP E5 / DEVSLP1 | I | Coffee Lake | 12 | OBSDATA_C1 | GPP_D18 / DMIC_DATA1 | I | Coffee Lake |
| 13 | GND | GND | NA | | 14 | GND | GND | NA | |
| 15 | OBSDATA_A2 | GPP_E6 / DEVSLP2 | I | Coffee Lake | 16 | OBSDATA_C2 | GPP_D19 / DMIC_CLK0 | I | Coffee Lake |
| 17 | OBSDATA_A3 | GPP_E7 / CPU_GP1 | I | Coffee Lake | 18 | OBSDATA_C3 | GPP_D20 / DMIC_DATA0 | I | Coffee Lake |
| 19 | GND | GND | NA | | 20 | GND | GND | NA | |
| 21 | OBSFN_B0 | Open | NA | | 22 | OBSFN_D0 | Open | NA | |
| 23 | OBSFN_B1 | Open | NA | | 24 | OBSFN_D1 | Open | NA | |
| 25 | GND | GND | NA | | 26 | GND | GND | NA | |
| 27 | OBSDATA_B0 | GPP_E8 / SATALED# | I | Coffee Lake | 28 | OBSDATA_D0 | GPP_D23 / I2S_MCLK | I | Coffee Lake |
| 29 | OBSDATA_B1 | GPP_E9 / USB2_OC0# | I | Coffee Lake | 30 | OBSDATA_D1 | GPP_E0 / SATAXPCIE0 / SATAGP0 | I | Coffee Lake |

### Table 46-11. Secondary XDP Connector Pinout (Sheet 2 of 2)

| Pin | XDP Signal Name | Target Signal | I/O | Device | Pin | XDP Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 31 | GND | GND | NA | | 32 | GND | GND | NA | |
| 33 | OBSDATA_B2 | GPP_E10 / USB2_OC1# | I | Coffee Lake | 34 | OBSDATA_D2 | GPP_E1 / SATAXPCIE1 / SATAGP1 | I | Coffee Lake |
| 35 | OBSDATA_B3 | GPP_E11 / USB2_OC2# | I | Coffee Lake | 36 | OBSDATA_D3 | GPP_E2 / SATAXPCIE2 / SATAGP2 | I | Coffee Lake |
| 37 | GND | GND | NA | | 38 | GND | GND | NA | |
| 39 | HOOK0 | RSMRST# | I | Coffee Lake | 40 | ITPCLK/HOOK4[1] | Open | NA | |
| 41 | HOOK1 | Open | NA | | 42 | ITPCLK#/HOOK5 | Open | NA | |
| 43 | VCC_OBS_AB | PCH v1.0A | NA | system | 44 | VCC_OBS_CD | PCH v1.0A | NA | system |
| 45 | HOOK2 | Open | NA | | 46 | HOOK6/RESET# | Open | NA | |
| 47 | HOOK3[1] | Open | NA | | 48 | HOOK7/DBR# | Open | NA | |
| 49 | GND | GND | NA | | 50 | GND | GND | NA | |
| 51 | SDA[1] | Open | NA | | 52 | TDO | Open | NA | |
| 53 | SCL[1] | Open | NA | | 54 | TRSTn | Open | NA | |
| 55 | TCK1 | Open | NA | | 56 | TDI | Open | NA | |
| 57 | TCK0 | Open | I | | 58 | TMS | Open | NA | |
| 59 | GND | GND | NA | | 60 | GND[2] (XDP_PRESENT#) | GND | NA | |

***Notes:***
1. These signals are optional, can be left as OPEN/No-Connect.
2. Connect pin 60 to GND when it is not used to indicate the presence of ITP-XDP style tool.

### 46.1.2.5 Secondary CMC PinOut

Table 46-12 documents the pinout of Secondary CMC connector.

### Table 46-12. Secondary CMC Connector Pinout (Sheet 1 of 2)

| Pin | CMC Signal Name | Target Signal | I/O | Device | Pin | CMC Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 1 | OBSDATA_0 | GPP_E1 / SATAXPCIE1 / SATAGP1 | I | PCH | 2 | OBSDATA_8 | GPP_E9 / USB2_OC0# | I | PCH |
| 3 | OBSDATA_1 | GPP_E2 / SATAXPCIE2 / SATAGP2 | I | PCH | 4 | OBSDATA_9 | GPP_E10 / USB2_OC1# | I | PCH |
| 5 | OBSDATA_2 | GPP_E3 / CPU_GP0 | I | PCH | 6 | OBSDATA_10 | GPP_E11 / USB2_OC2# | I | PCH |
| 7 | OBSDATA_3 | GPP_E4 / DEVSLP0 | I | PCH | 8 | OBSDATA_11 | GPP_E12 / USB2_OC3# | I | PCH |
| 9 | OBSDATA_4 | GPP_E5 / DEVSLP1 | I | PCH | 10 | OBSDATA_12 | GPP_F0 / SATAXPCIE3 / SATAGP3 | I | PCH |
| 11 | OBSDATA_5 | GPP_E6 / DEVSLP2 | I | PCH | 12 | OBSDATA_13 | GPP_F1 / SATAXPCIE4 / SATAGP4 | I | PCH |

**Table 46-12. Secondary CMC Connector Pinout (Sheet 2 of 2)**

| Pin | CMC Signal Name | Target Signal | I/O | Device | Pin | CMC Signal Name | Target Signal | I/O | Device |
|---|---|---|---|---|---|---|---|---|---|
| 13 | OBSDATA_6 | GPP_E7 / CPU_GP1 | I | PCH | 14 | OBSDATA_14 | GPP_F2 / SATAXPCIE5 / SATAGP5 | I | PCH |
| 15 | OBSDATA_7 | GPP_E8 / SATALED# | I | PCH | 16 | OBSDATA_15 | GPP_F3 / SATAXPCIE6 / SATAGP6 | I | PCH |
| 17 | OBS_CLK_1P | GPP_E0 / SATAXPCIE0 / SATAGP0 | I | PCH | 18 | OBS_CLK_2P | GPP_F4 / SATAXPCIE7 / SATAGP7 | I | PCH |
| 19 | GND | GND | NA | | 20 | OBS_CLK_2N | Open | NA | |
| 21 | OBS_CLK_1N | Open | NA | | 22 | VCCOBS_AB | Open | NA | |
| 23 | XDP_PRESENT_CPU | Open | NA | | 24 | XDP_PRESENT_PCH | Open | NA | |
| 25 | HOOK[3] | Open | NA | | 26 | HOOK[6] | Open | NA | |
| 27 | HOOK[0] | Open | NA | | 28 | XDP_TRST# | Open | NA | |
| 29 | XDP_TDI | Open | NA | | 30 | XDP_TMS | Open | NA | |
| 31 | XDP_TCK1 | Open | NA | | 32 | XDP_TCK0 | Open | NA | |
| 33 | XDP_PREQ# | Open | NA | | 34 | XDP_PRDY# | Open | NA | |
| 35 | XDP_TDO | Open | NA | | | | | | |

## 46.1.3 Intel® DCI Implementation

Intel® DCI (Direct Connect Interface) is an Intel Technology that allows debug access by re-purposing a USB 3.0 port. The advantage is debug functions and trace features can be connected using existing USB3 ports, rather than the usual additional connectors. If properly supported, many debug functions can be implemented "closed chassis". The DCI connection supports run-control debug, validation, trace, DMA, OS Debug and scripting.

DCI is implemented using two primary transport topologies: Intel® DCI-OOB (formerly BSSB), and Intel® DCI-Debug Class (formerly DbC).

The following sub sections cover the requirements to implement Intel® DCI for supporting closed-chassis debug on the platform.

All USB3 ports support Intel DCI. USB3 Port 1 additionally supports OTG. If the OTG function is not used, please pull down the USB2_ID pin to program the function properly.

This sections describes the debug hook routing requirement for platforms using Intel DCI without an XDP60 or CMC connector.

It is important to maintain the merged JTAG circuitry for proper Intel DCI functionality. Route the JTAG pins, HOOK pins according to the Table 46-10 and Figure 46-14:

## Figure 46-10.Connector Less Routing Topology

***Note:*** Connect JTAG pull-ups to VccST on S designs and VccST-G on H designs.

## Figure 46-11.Connector Less Routing Topology

## Table 46-13. Connector Less Debug Hooks Routing Guidelines

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| PROC_TDI,<br>PROC_TDO,<br>PROC_TMS,<br>PROC_TCK,<br>PROC_TRST#,<br>PCH_JTAG_TCK<br>PCH_JTAG_TDI<br>PCH_JTAG_TDO,<br>PCH_JTAG_TMS,<br>JTAGX,<br>PCH_TRST# | • Route these signals to Test Points according to Figure 46-13:<br>• **Stub Length**: 200ps (approx 1100 mil or 28mm)<br>• **Maximum Trace length**: 1ns (approx 6000 mil or 154mm)<br>• **PROC_TCK Termination**:<br>— 51 ohm +/- 5% pull down to GNG (Ground)<br>— Placed to within 200ps (1100 mil) or PROC_TCK pin<br>• **PCH_JTAG_TDO Termination**:<br>— 51ohm +/- 5% pull up to VccSTG or equivalent.<br>— Placed to within 200ps (1100 mil) or PCH_JTAG_TDO pin<br>• Test Point Pad Size: 18 mil minimum, preferred 25 mil maximum<br>• Test Points Placement: placed to within 250ps of the repetitive Coffee Lake pins, and the distance between TP and termination (if any) must be within 200ps.<br>•Refer Section 46.1.7 for additional routing guidelines on Test Points requirement for Intel® Silicon View Technology DFM HVM Test Solution.<br>**•Refer to Section 46.1.6 for additional PCB layout rules.** | |
| RSMRST#,<br>PROC_PREQ#,<br>PROC_PRDY#,<br>CFG[3],<br>SPIO_IO2,<br>SYS_RESET#,<br>ITP_PMODE | • Route these signals to Test Points according to Figure 46-13<br>• Test Point Pad Size: Minimum 18mil, preferred 28 mil<br>• Refer RSMRST#, CFG[3], SPI_IO2, SYS_RESET# in their respective sections for additional routing guidelines and termination or strapping requirement.<br>•Refer Section 46.1.7 for additional routing guidelines on Test Points requirement for Intel® Silicon View Technology DFM HVM Test Solution. | |
| GND,<br>VCCOBS_AB | •Route PCH V1.0 A Rail or equivalent voltage rail to a test point pad.<br>•Route two ground (GND) pins directly to a GND plane through individual vias.<br>•Test Point Pad Size: Minimum 18mil, preferred 28 mil<br>•Refer Section 46.1.7 for additional routing guidelines on Test Points requirement for Intel® Silicon View Technology DFM HVM Test Solution. | |
| JTAG_ODT_Disable | • Let Float | |
| SML1ALERT#/<br>PCHHOT#/GPP_B23 | •If USB 3.0 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.<br>•If USB 3.0 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float.<br>•If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor. | |

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| CPU:<br>PROC_TDI,<br>PROC_TDO,<br>PROC_TMS,<br>PROC_TCK,<br>PROC_TRST#,<br><br>PCH-H:<br>JTAG_TCK,<br>JTAG_TDI,<br>JTAG_TDO,<br>JTAG_TMS,<br>JTAGX,<br>CPU_TRST# | • Route these signals according to Figure 46-13<br>• **Stub Length:** 200ps (approx 1100mil or 28mm)<br>• **Maximum Trace length:** 1ns (approx 6000mil or 154mm))<br>• **PROC_TCK Termination:**<br>— 51 Ω +/- 5% pull down to GND (Ground)<br>— Placed to within 200ps (1100 mil) or PROC_TCK pin<br>• **PCH-H JTAG_TDO Termination:**<br>— 51Ω +/- 5% pull up to VccST rail or equivalent.<br>— Placed to within 200ps (1100 mil) or PCH-H JTAG_TDO pin<br>• Test Point Pad Size: 18 mil minimum, preferred 25 mil maximum<br>• Test Points Placement: placed to within 250ps of the repetitive Coffee Lake pins, and the distance between TP and termination (if any) must be within 200ps.<br>•Refer Section 46.1.7 for additional routing guidelines on Test Points requirement for Intel® Silicon View Technology DFM HVM Test Solution.<br>**•Refer to Section 46.1.6 for additional PCB layout rules.** | |

| Pin/Signal | Routing Rules | Notes |
|---|---|---|
| CPU<br>PROC_PREQ#<br>PROC_PRDY#<br><br>PCH<br>PREQ#<br>PRDY# | • Route these signals according to Figure 46-13.<br>• **Stub Length:** 200ps (approx 1100mil or 28mm)<br>• **Maximum Trace length:** 2.5ns (approx 15000mil or 381mm), should minimize the trace length whenever possible.<br>• Test Point Pad Size: 18 mil minimum, preferred 25 mil maximum<br>• Test Points Placement: placed to within 250ps of the repetitive Coffee Lake pins, and the distance between TP and termination (if any) must be within 200ps.<br>•Refer Section 46.1.7 for additional routing guidelines on Test Points requirement for Intel® Silicon View Technology DFM HVM Test Solution.<br>•**Refer to Section 46.1.6 for additional PCB layout rules.** | |
| PCH-H:<br>RSMRST#,<br>SPIO_IO2,<br>SYS_RESET#,<br>ITP_PMODE<br><br>CPU:<br>CFG[3] | • Route these signals to Test Points according to Figure 46-13<br>• Test Point Pad Size: Minimum 18mil, preferred 28 mil<br>• Refer RSMRST#, CFG[3], SPI_IO2, SYS_RESET# in their respective sections for additional routing guidelines and termination or strapping requirement.<br>•Refer Section 46.1.7 for additional routing guidelines on Test Points requirement for Intel® Silicon View Technology DFM HVM Test Solution. | |
| GND,<br>VCCOBS_AB | •Route PCH V1.0 A Rail or equivalent voltage rail to a test point pad.<br>•Route two ground (GND) pins directly to a GND plane through individual vias.<br>•Test Point Pad Size: Minimum 18mil, preferred 28 mil<br>•Refer Section 46.1.7 for additional routing guidelines on Test Points requirement for Intel® Silicon View Technology DFM HVM Test Solution. | |
| JTAG_ODT_Disable | • Let Float | |
| SML1ALERT#/<br>PCHHOT#/GPP_B23 | •If USB 3.0 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.<br>•If USB 3.0 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float.<br>• | |

### 46.1.3.1 Intel® DCI OOB Overview

Intel® DCI-OOB is implemented using a proprietary electrical transport over the USB3 port. The USB3 pins are used, but do not use USB3 electrical signaling. The following sections describe tool considerations and board schematic considerations.

It is only required to support Intel® DCI-OOB on one external connector. The least complex and least expensive solution is to use an existing USB3 Type A connector which does not use any retimer solution. If only USB Type C is available, then the section describes configurations appropriate to make Intel® DCI-OOB operate properly.

**Advantage:** Intel® DCI-OOB is used when debug connections need to survive power transitions to S0iX and Sx states. Starts operation almost immediately upon boot start. Additionally, if Intel® DCI-OOB is connected from a cold boot, no BIOS enabling is needed.

**Disadvantage:** Transport operates at a considerably lower frequency than Intel® DCI-Debug class.

#### 46.1.3.1.1 Interface Tool Considerations for Intel® DCI OOB Support over USB3

Intel® DCI-OOB requires a special debug adaptor called the Closed Chassis Adapter (CCA). From a user perspective, the software automatically configures to use the new Intel® DCI-OOB interface.

#### 46.1.3.1.2 Signaling Considerations for Intel® DCI OOB Support over USB3

For Intel® DCI-OOB Hosting DCI functionality to work properly in the system, the following signaling requirements must be met by the platform design:

- Any external pull-down resistor on the SoC TRST_N trace must be depopulated. This is especially important in systems migrating from open-chassis MIPI60 operation
- All the devices in Intel® DCI-OOB Hosting signal path must be designed to support Intel® DCI-OOB signaling. The proprietary Intel® DCI-OOB signaling is single-ended CMOS which must be preserved for this debug technology to operate properly.
  - Any components placed in this path must allow the CMOS single ended like signaling to pass.
  - In general, this can rule out any active switches, re-timers, and re-drivers in this path.
  - CMCs, EMI inductors/ferrite beads (Common Mode Chokes), negatively impact Intel® DCI-OOB performance. If not needed for EMI suppression, remove or short out. These filters aren't needed for USB functionality but are used to reduce radio interference.
    CMCs may interfere with OOB signal integrity by changing the maximum effective operating frequency of the data channel. Remove from the SSRx signals and replace with 0 Ω resistors (or wires/solder bridges) if higher OOB transport frequencies are needed.
  - RX Coupling capacitors: Some designs implement AC coupling caps on the inbound RX SS pin. This breaks Intel® DCI-OOB and violates the USB standards specification. Capacitors are placed only on the TX SS signals.
  - Signaling for Intel® DCI-OOB operates at maximum of 1.0V.

#### 46.1.3.1.3 Intel® DCI OOB Configurations Supporting USB3 Type A

For Intel® DCI-OOB Hosting DCI functionality to work properly in the system, proper signaling as described in previous section must be preserved. For many USB3 Type A implementations, no re-timer device is required. If a re-timer is required, it will stop OOB operation.

#### 46.1.3.1.4 Intel® DCI OOB Configurations Supporting USB Type-C Implementations

Support for alternate functions such as Display Port and plug reverse require an external MUX device which complicates the Intel® DCI-OOB design. Additionally, re-timer devices, which improve signal fidelity, block OOB signaling and special devices are needed to remedy the situation. Try to use Type A for DCI as much as possible. For design without Type-C, please reserve an unused USB3 port and route it to test points for soldering a type A connector when DCI.OOB is necessary. DCI.OOB usage will be reduced because of the introduction of DCI.USB2. So the rework should be minimal.

### 46.1.3.2 DCI.USB2/DCI.USB3

Intel® DCI-Debug Class is implemented using standard USB3 Super Speed/ USB2 High Speed electrical and transport protocol. There are no additional electrical channel or connection requirements for using DCI-USB as the standard USB3 Super Speed/USB2

High Speed channel is used. A standard USB3/USB2 cable can be used for connecting the Host PC and the SUT. No special interface box is required. Bear in mind that only designs paired with Cannon Lake PCH will have DCI.USB2 feature

**USB3 Advantage:** Much higher transport speeds.

**USB3 Disadvantage:** Starts later in boot process so some early messages and unlock capabilities are not available. Does not operate through power sequences.

**USB2 Advantage:** Higher speed than DCI-OOB. No special interface box is required. Can even trace in S5.

**USB2 Disadvantage:** There are some usages that DCI-USB2 cannot handle. Those cases will be handled by Intel using DCI-OOB

#### 46.1.3.2.1 Signaling Considerations for Intel® DCI Direct Connect Support over USB3/USB2

The controllers and multiplexers in the signal path of the USB3/USB2 pins must be powered when Intel DCI "Direct Connect" is in use for the signals to pass. Standard USB3/USB2 signaling is utilized.

### 46.1.3.3 Thunderbolt™ Configurations

Alpine Ridge does not directly support Intel.DCI.OOB. Refer Chapter 11, "Thunderbolt™ Design Guidelines" in this document supporting Thunderbolt Solutions for proper implementation.

## 46.1.4 eXtended Debug Port (XDP) Mechanical Specifications

Figure 46-12 illustrates the target system volume that must be reserved for the ITP-XDP to attach to the target system. It is recommended that the main ITP-XDP enclosure be securely attached to the target system to avoid damage to the ITP-XDP and the target system. Four 1/8 inch mounting holes are provided on the ITP-XDP to facilitate attachment with screws or cable ties.

The Intel ITP-XDP3 hardware unit has four half-inch by 1/16th inch slots for cable tie or velcro straps to secure the body of the ITP-XDP3 hardware unit to the chassis. Third party vendors run control tools would have different keepout volumes and securing features.

## Figure 46-12.60-pin XDP Connector System Keep-Out Diagram

The placement of the XDP connector on the 2nd side should be avoided if possible. Among other reasons, it should be avoided due to the complexity of hand placing and soldering the device. Cap all vias near the XDP-connector pads in compliance with the Intel DFM Guidelines for capped vias. vias need to be capped not only around the XDP connector pads, but also specifically under the XDP connector body. Open vias under the XDP connector can cause shorts.

Contact your Intel representative for a formal review of the mechanical placement and layout of the system.

## 46.1.5 Chassis Mount Connector (CMC) Mechanical Specifications

Chassis Mount Connector (CMC) is a compact connecting solution developed by Intel for Coffee Lake platform debug. CMC has a much smaller keep-out than the standard 60 pin XDP connector. It utilizes a motherboard through-hole for mounting and makes contact with pads located and routed around the mounting hole via the CMC connector. There are two versions of CMC adapters: the CMC Merged adapter (primary CMC) offers the same DFX accessibility (with the exception of SMBus)) as the standard 60-pin XDP connector and the CMC OBS adapter (secondary CMC) provide access to OBS signals via paddle-board.

### 46.1.5.1 Primary Chassis Mount Connector (CMC) Mechanical Drawings and Keep Out

The following diagrams illustrate the KOZ and KOV must be reserved for the Primary (Merged) CMC adapter on a Coffee Lake platform.

Note that an adapter (ITPCMCMERGEADAP1, MM#933664) to connect Primary CMC to XDP connector on the ITP hardware is required. This adapter can be ordered from https://designIntools.intel.com/.

## Figure 46-13.Primary (Merged) CMC Gen 1 Keep out Specification

## Figure 46-14.Primary (Merged) CMC Pads Layout (Primary Side)

## Figure 46-15.CMC Gen 1 - Captive Screw

**Figure 46-16.CMC Gen 1- Retention Nut**

## 46.1.5.2 Secondary Chassis Mount Connector (CMC) Mechanical Drawings and Keep Out

The following diagrams illustrate the KOZ and KOV must be reserved for the Secondary (OBS) CMC attachment on a Coffee Lake platform.

## Figure 46-17.Secondary CMC Keep Out Specification

## Figure 46-18.Secondary (OBS) CMC Pads Layout

Refers to Figure 46-15 and Figure 46-16 for the mechanical drawings of CMC Captive Screw and Retention Nut.

Note that An adapter (ITPCMCOBSADAP1, MM#933663) to connect Secondary OBS CMC to Logic Analyzer Interface connector is required. This adapter can be ordered from https://designIntools.intel.com/.

### 46.1.6 Additional Debug Port PCB Layout Guidelines

This section describes the general high speed layout guidelines must be followed for the debug port:

Electrical lengths of XDP traces are provided in units of flight time. Conversion of flight time to board-trace lengths is dependent on what layer routing occurs on, and the dielectric constant of the board materials for a specific design. Rule-of-thumb numbers can be derived by using 140 to 180ps/inch for outer layers of an FR4 product and 180ps/inch for inner layers

**Trace Nominal Impedance for Debug Port** JTAG signals, OBS pins, HOOK[3:0], HOOK[7:6], XDP_PRESENT#, $I^2C$ pins: 50 Ω ±17% nominal impedance. HOOK[5:4]: 100Ω (differential pair).

Unless indicated otherwise, Signals on the debug port should be routed with this in mind:

- Minimize the number of layer transitions and avoid plane split crossings imposed on each trace (ideally this will be zero). If return paths are well kept then the number of vias are nearly immaterial.
  - Clock signals (TCK, OBSFN_CD/OBS_CLK) are allowed maximum of 4 vias.
  - Clock signals are not allowed to route across splits or over voids.
- All signals except VCCOBS, GND and HOOK[5:4] pins must be referenced to ground (GND) plane.
- All signals except GND, VccOBS, and HOOK[0,1, 2, 3, 6, 7] pins must include ground-stitching/return vias near every layer transition. ground-stitching/return vias should be placed to within 0.1 inches (2.54mm) of the signal via.

**Figure 46-19.Ground Stitching/Return Vias Example**

- For situations where these signals are routed referenced to one or more power planes, include a bypass capacitor near every layer transition or plane split between the two referenced planes. bypass capacitor pads should be placed to within 0.5 inches (12.7mm) from the trace.

**Figure 46-20.Bypass Capacitor**

- Avoid sharing XDP bypass capacitors with other high-speed signals.
- For all signals, pull-up termination resistors should be located above a solid-power plane. If a solid-power plane does not exist at the required termination location, add a 0.1µF ceramic capacitor to GND on the pull-up voltage within 0.5 inches of termination resistor.

The length of any un-terminated stub on any TCK (1:0) or observation-port pin nets must be less than 200ps (1100 mil or 28mm) unless otherwise stated. The 51 ±5% Ω recommendation in this document for signal termination has been proven to work on all recommended board impedances. JTAG and observation-port signals my optionally be terminated using the nominal-board impedance.

### 46.1.6.1 Termination Resistor Placement

Termination resistances are given, with tolerances, whenever appropriate. Tolerances are documented as within ± of the percentage.

With few exceptions (noted specifically in their description), termination resistors must be close to the receiver. The topology, at the end of the chain, must be terminated in one of the following ways (in all cases) except those noted in their specific description.

**Preferred Debug Port termination Method:** In the case of Figure 46-21, where there is a termination after the last receiver, (A) must be smaller than any noted maximum routing length. There is no restriction for the length of (B) unless otherwise noted.

**Figure 46-21.Termination after Last Receiver**

Option 2 for XDP termination Method: Figure 46-22 shows another method for termination that is equally valid. This is a termination prior to the end receiver where the maximum routing length of the signal must be less than the length of (D) + (C). (C) must be less than 200ps or noted stub length whichever is smaller.

**Figure 46-22.Termination Prior to Last Receiver**

In both figures above, note that there may be other devices on the (A) or (D) routing of the signal if called for within this document.

### 46.1.7 Additional Routing Guidelines to support Intel® Silicon View Technology (Intel® SVT) based DFM HVM Test Solution

Intel enabled several third party JTAG vendors to design high volume manufacturing (HVM) test solution based on Intel® SVT architecture. With this test solution, the test points are placed on the JTAG pins of the processor and PCH and other required signals, and the Intel enabled test tool will make contact to the test point pads on the secondary side of the board via dual end probes. The figure below illustrates the typical setup of the Intel enabled DFM HVM test solution.

**Figure 46-23.Intel DFM HVM Test Solution High Level View**

Besides routing test point pads to JTAGs and PROC_PREQ# and PROC_PRDY#, CFG[3], SPIO_IO2 signals of processor and PCH as outlined in Section 46.1.1, Several others signals must also be routed to test point pads. these signals are:

- **PowerGood (HOOK0)** - Route RSMRST# to a test point pad to use as HOOK0 signal.
- **RESET_N (HOOK6)** - Route ITP_PMODE to a test point pad as HOOK6 signal for both processor and PCH.
- **DBR# (HOOK7)** - Route SYS_RESET# to a test point pad as HOOK7 signal.
- **Power (VccOBS_AB)** and **Ground (GND) Pins** - Route PCH_V1.0A Rail or equivalent voltage rail to a test point pad as the VccOBS_AB pin and route two ground (GND) pins directly to a GND plane through individual vias.

There is no trace length limitation on these signals, but it is recommended to optimize when routing between each signal to its test point pad and keep trace length to minimum whenever possible.

To reduce the GND affect and improve signal integrity, the following are recommended for supporting the manufacturing testing of the motherboard:

- Test point pads must be used on the secondary side of the motherboard for tester accessibility via pogo pins.
- Prefer pad size is 25 mil, but 18 mil is acceptable. The pad size must meet the industry standard for boundary scan test.
- The pads are not required to be arranged into a particular pad pattern. However, TCK signals must be routed with GND pads nearby.

### 46.1.8 Depopulation Guidelines for Debug Port

At some point there may be a desire to remove the debug port from the board especially when the debug is no longer needed. It is recommended that the debug-port real estate and pads remain in place if they need to be populated for a future problem.

Coffee Lake has adequate internal bias resistance on JTAG, PROC_PREQ# and PROC_PRDY# signals to keep the devices in an idle state without the external pull up resistors.

It is acceptable to replace the standard resistor values with any resistor value between 51 Ω to 3k Ω to reduce bill-of-material items when the debug is no longer needed.

Processor BPM#[3:0] nets can be left floated when not use for debug. Processor CFG[19:0] and PCH chipset test interfaces might have dual purpose usage. From XDP debug perspective, external components (resistor, jumper, or FET switch) between XDP connector and chipset test interfaces can be removed when debug is no longer needed; however, there might be a need to keep the strap resistor and the external components in place for the non debug usage of the interfaces; for example the "OR" gates associated with the VCCST/VCCSTG XDP Power Override Mechanism in Figure 44-4.

Refer other relevant chapters in Platform Design Guide (PDG), External Design Specifications (EDS) and your Intel representative for addition information on these signals.

From XDP perspective, it is fine to remove the isolation resistors of HOOK pins on the XDP side of the routing when debug is no longer needed. Refer relevant sections in PDG, EDS and your Intel representative before removing the external pull up resistor that tie to XDP HOOK pins.

***Note:*** Intel recommends at least route the JTAG signals according to Section 46.1.3 on the production board to support closed chassis debug after production.

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# 47 Platform Thermal Management Design Guidelines

Thermal management consists of a way to sense temperature and a means of reducing the temperature if it is above a specified limit. For each major component of the platform, thermal management is available for the user to implement into their system design to ensure sufficient platform cooling.

**Table 47-1. Platform Thermal Management Reference Documents**

| Title | Location |
|---|---|
| Coffee Lake Client Platform Thermal Management Design Guide | 571296 |

## 47.1 Platform Thermal Management Signal Descriptions

### 47.1.1 Signal Groups

The following signals must be connected for proper Intel® Turbo Boost Technology and overall platform thermal management behavior.

**Table 47-2. Signal Groups**

| Signal [4] Name | Routing Guideline | Description |
|---|---|---|
| PECI | Connect PECI directly from EC to the processor | PECI allows EC read / write access to registers to control thermal management |
| PROCHOT# [1] | | |
| AC_PRESENT# | | Senses whether AC is present on the platform |
| ADAPTER_ICC [2] | Connect from System Charger to EC | Senses Icc for the power adapter. Allow EC to monitor total platform power. |
| BRICK_ID [3] | Connect from AC Adapter to EC | Detect power limit for the AC Adapter |

***Notes:***
1. Platform needs to enable bi-directional PROCHOT# through Processor MSRs.
2. The GPIO on EC should be capable of A/D conversion.
3. Implementation of this signal is optional.
4. All Signals: Refer Section 14.2.7, "Platform Environmental Control Interface (PECI) Topology", and Table 14-4.

## 47.2 Platform Thermal Management Configuration, Connectivity, Block Diagram

Intel recommends that the system EC owns all platform thermal management buses and events. All platform components report their temperature to the EC so that platform software can provide an appropriate response. EC connects to the processor using PECI signal (EC is PECI Host). EC that supports PECI 3.0 is capable of getting per core or full processor package temperature data during turbo operation and also

temperatures in low power Cstates. EC connects to PCH through SMLink1 which can be used to report the direct PCH DTS temperature. Other platform thermal sensors can be connected to the EC directly through the SMBus.

**Figure 47-1. Thermal Management Option 1**

**Figure 47-2. Thermal Management Option 2**

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# 48 Acoustic Noise Mitigation

## 48.1 Introduction

Audible acoustic noise can be generated by electronic components, such as capacitors or inductors, when they vibrate due to large, fast and periodic voltage or current changes. Since platform power management techniques (e.g., processor C-state management) can cause such voltage transitions, it is important to address and minimize the acoustic risk.

These vibrations are transferred through the rigid mounting of the electronic components to the board. Multi-layered ceramic capacitors (MLCC) are most prone to this, because they are of rigid construction and rigidly mounted to the board. The circuit board acts as a sounding board, and audible acoustic noise is radiated.

This acoustic noise generation scenario is demonstrated in Figure 48-1. In such a scenario, there are a few architectural design guidelines that should be followed in order to minimize the risk of generating audible acoustic noise.

**Figure 48-1. Flow Chart of Acoustic Noise Generation**

To illustrate some of the complexity involved, the vibration pattern generated by a single capacitor when mounted in the center of an otherwise unpopulated board is shown in Figure 48-2.

The left-hand pattern shows “peak” and “valley” deflections throughout the board. The right-hand pattern shows the acoustic response generated by the board vibrations due to the capacitor vibration.

In this example, the acoustic maxima are symmetrically located on the left side and the right side of the board, because that is the orientation of the mounting pads that transmit the vibration. That the acoustic maxima locations do not correspond to the vibration source (i.e. capacitor) creates an added complexity for troubleshooting the acoustic issue. Therefore, it is not advised to use microphone scanning to identify the vibrating source component.

**Figure 48-2. Example Vibration (Left) and Acoustic Radiation (Right) Pattern Generated by One Capacitor Mounted in the Center of Test Board**

***Note:*** Capacitor Location Denoted by Red Square

# 48.2 Noise Mitigation

## 48.2.1 Mechanical Mitigation

It is good mechanical design practice, if board layout and space allows, mounting capacitors that are driven by the same electrical signal on both sides of the board directly opposite each other. This symmetrical mounting cancels out a large part of the vibrations generated by the capacitors, and therefore the acoustic noise. An example of this is shown in Figure 48-3, where two capacitors with symmetric mounting generate a significantly lower acoustic level than a single-sided mounted capacitor. The example is an idealized test case, and the amount of reduction seen in a real system might be less.

**Figure 48-3. Example: Single-sided Mounted Capacitor Generates 49 dB Sound Pressure Level (SPL) while Symmetrically Mounted Capacitor Generate 25 dB**

***Note:*** SPL Measured Just Above Capacitor

Even though mechanical precautions have been taken, acoustic noise at lower levels can still be generated. Therefore, architectural guidelines also need to be adhered to for minimizing the acoustic noise.

## 48.2.2 Architectural Mitigation

### 48.2.2.1 Signal Parameters

The acoustic noise generated depends upon the voltage swing and frequency of the voltage changes. The acoustic noise decreases with decreasing voltage swing. However, reducing the voltage swing could have a negative effect on the potential power savings. In addition, the frequency of the voltage swing is a parameter to consider in reducing the perceived impact of the acoustic noise. The audible frequency range is 20 Hz - 20 kHz, and this frequency range is divided into three different regions (low, mid and high) in this text. It is acoustically beneficial to employ specific frequencies for periodic processor interrupts in each of these three regions as described below.

1. Low frequency (20 Hz - 200 Hz) range; the extreme ends of this range are recommended for reducing the perceived noise. The 70 Hz frequency is technically the worst to use, due to the human perception of this frequency (called roughness). However, the acoustic noise level is lower for interrupts across this range, and therefore generally not noticed.
2. Mid frequency (200 Hz - 1 kHz) range; 200 Hz - 300 Hz is preferred.
3. High frequency (1 kHz - 20 kHz) range; higher frequency is preferred to reduce the number of harmonics in the audible range. If there is a need to operate at lower frequencies in this range, it should be done with caution. The human ear is most sensitive in the frequency range of 1 - 6 kHz. Hence, interrupt frequencies in this range, especially 1 kHz, should be avoided if possible.

Another parameter to consider is the ramp rate of the voltage changes. The ramp rate is defined as the voltage change over unit time and describes how fast and/or slow electronic components experience voltage level changes. Different ramp rates can impact the strength of the harmonics; however, there is an interaction with the duty cycle of the transition. Therefore, different ramp rates must be tested on a case-by-case basis for their acoustic benefit.

#### 48.2.2.2 Software and Settings

BIOS/UEFI settings should be used to synchronize the EHCI controllers, and USB selective suspend should be enabled, because these settings can reduce the likelihood of voltage or current changes that may trigger acoustic noise. Refer to BIOS Writers Guide for details.

#### 48.2.2.3 Dynamic Periodicity Alteration

An architectural mitigation methodology that addresses the acoustic issue directly at the source by disrupting/altering the periodicity of the electrical signal is called Dynamic Periodicity Alteration (DPA). A requirement for audible acoustic noise is periodic voltage/current transitions. The most common scenario when such transitions occur is during an Operating System (OS) or application-scheduled timer event. When there are no applications to execute in the near future, the CPU enters in to a sleep state (C-state). When the timer expires, an interrupt occurs and wakes the CPU from the sleep state. This sleep-wake sequence can result in periodic voltage transitions that can cause audible noise. By disrupting the periodicity, the acoustic levels can be reduced and can become less audible to the user.

Without a DPA implementation, the processor pursues a “just-in-time” wake-up strategy. This involves ramping the input VR and waking a core just before the timer event expires. Immediately after the timer event is serviced, the processor ramps the input VR back down to the lower voltage. The result is high power efficiency, but periodic timer ticks result in periodic power actions and the potential for unacceptable acoustic noise.

The DPA implementation pseudo-randomizes the scheduling of these three power actions: ramping the input VR from 1.6V to 1.8V (first introduced on 4th Generation Intel® Core™ Processor), waking the bootstrap thread (essentially waking a core), and then ramping the input VR down from 1.8V to 1.6V. BIOS can program the maximum range of the randomization of each event. For each event, a different pseudo-random number is chosen to alter the timing of these three actions.

Figure 48-4 shows a pictorial representation of the resulting behavior. The diagram depicts time advancing from top to bottom and left to right, with each segment representing a 1 ms time interval. The left side of the diagram shows an example of what the behavior is without DPA. A timer tick at a 1 ms interval causes the three power actions (ramp input VR from 1.6V to 1.8V, wake a core, and ramp input VR from 1.8V to 1.6V) to occur at regular intervals. The diagram shows how these power actions align between subsequent time intervals. The diagram on the right shows the result of the architectural mitigation of periodic power events with DPA. The regular interval between power events is disrupted by the introduction of pseudo-randomness in the scheduling of power actions. The amount of time off-set is adjustable.

**Figure 48-4. Before (Top) and After (Bottom) the Implementation of Dynamic Periodicity Alteration**

It is up to the OEM to set the appropriate randomization ranges depending upon the severity of the acoustic noise generated. If the OEM needs to enable the DPA feature, two features should be employed before employing the full three-feature DPA. The two features to activate first are either pre-wake or ramp-up, which should be combined with ramp-down. The OEM should start with a low randomization range and increase the range until the acoustic noise is mitigated. The range is between 0 (no DPA) to the maximum value of max 255 us [0xff]. This staged approach will ensure the lowest power penalty of the DPA feature. If the noise is still not mitigated, the full three-feature DPA should be employed (pre-wake, ramp-up, and ramp-down), and the OEM should again start with a low randomization range and increase the range until the noise is mitigated.

Refer the appropriate BIOS Writers Guide for details of register settings and implementations.

#### 48.2.2.4 Constant Voltage Regulator (VR) Voltage

If periodic excitations are not due to scheduled timer events, DPA does not apply. In this case, the recommendation is to keep C-states enabled, but reducing the min VID so there is either no or a reduced voltage delta between the sleep states. This approach can also be used in conjunction with or in place of DPA even for timer driven events, if further acoustic mitigation is required. Refer CPU dependent VR guidelines for details.

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# 49 Electromagnetic Compatibility

## 49.1 General Considerations

### 49.1.1 Ground Ring/ PTH

- Ground rings on all layers and ground PTHs are recommended on the edge of the board.
- Ground ring should be a continuous and solid shape with no splits and minimum shape neck width is 0.75mils.
- At least 0.5mm gap between ground ring and other signal traces/shapes.
- The ground shape should connect to multiple mounting holes electrically. This connects the PCB ground to chassis ground. The mounting holes need to be evenly distributed.
- The ground shape is useless without proper vertical stitching to the ground layer. Connector holes can be considered stitching vias. Add vias throughout the length of the ground shape, no more than 2.5mm apart, close to the board's edge. Refer figure below.

**Figure 49-1. Ground Ring/ PTH**

The following example shows the impact of adding the ground ring. Below figure (FIG (A)) shows a PCB board with a differential trace routed as stripline. The trace length routed was 50mm. A Wi-Fi Antenna is included in the model and is placed 50 mm away from the differential trace. The differential trace is excited with a common mode signal. The impact of the ground ring is assessed by comparing the noise coupled to the antenna with and without a ground ring in use. Below figure (FIG (B)) shows the noise coupling comparison with and without the ground ring. The noise coupling can reduce by 27dB when a ground ring is used.

**Figure 49-2. Example - Ground ring**

## 49.1.2 Power Plane Decoupling

Power planes on top and bottom layers longer than 50 mm may have significant emission. Decoupling capacitors (0.1 uF, 0402 or smaller) need to be placed along the edge of such power plane with spacing <50 mm. The decoupling capacitors need to be within 10 mm from the edge of power planes. Decoupling may be skipped when there already existing similar capacitors (0.1 uF, 0402 or smaller) within 10 mm. Refer figure below.

**Figure 49-3. Power Plane Decoupling**

## 49.1.3 Connector Decoupling

Decoupling capacitor placed on power pins of internal and external connectors to reduce the noise on power rails and recommended capacitor value is 0.1uF 0402 or smaller. Refer figure below for example.

**Figure 49-4. Example for Connector Decoupling**

## 49.1.4 Crossing Split planes

Crossing split planes increases the emissions from the signal traces. Recommended to avoid crossing split planes by moving the traces or reshape the power planes. Refer figure below for example.

**Figure 49-5. Example for Traces Crossing Planes**

### 49.1.5 Reference Discontinuity

- Changing reference plane from GND to power plane, or from power plane A to power plane B, may significantly increase noise emission.
- It is recommended to have stitching capacitors (0.1 uF, 0402 or smaller) to bridge the two reference planes and provide current return path. Refer figure below for stitching capacitors placement.

**Figure 49-6. Stitching Capacitors Placement**

## 49.2 Power Supply

### 49.2.1 Voltage Regulator

- Switching mode regulators (including battery charger) have EMI/RFI noise caused by parasitic resonance.
- A filter at voltage input may reduce the noise. The filter consists of a ferrite bead, diode and a resistor.
- The selection of the components depends on the VR design. An example of ferrite bead BLM18SG121TN1, diode ESD300-B1-02LRH, and 2-ohm resistor shows 3-10 dB EMI reduction in 3-m chamber. It is recommended resistor to be no larger than 2 ohm. Refer figure below for input filtering circuit.
- Place the decoupling capacitors very close to the top transistor. The ground pin of the capacitors should be connected to the solid ground plane right underneath.
- Use at least two decoupling capacitors to reduce overall parasitic inductance from the capacitors themselves.
- Have a solid ground plane immediately underneath the VRM circuit and connect the VRM ground to the solid ground plane through vias.

**Figure 49-7. VRM Input Filter**

**Figure 49-8. Measurement Results**

## 49.2.2 AC Jack

Ferrite Bead on both power and GND pins of the AC jack to reduce EMI emissions. Refer figure below.

**Figure 49-9. Filtering Circuit for AC Jack**

## 49.3 Critical Signals

### 49.3.1 Audio

- DMIC clock may have EMI/RFI risk due to its high-order harmonics.
- Recommend to have strip line routing and a RC filter before being routed in microstrip/cable to reduce high-frequency harmonics.
- The RC value may vary according to the board design. Refer figure below.

**Figure 49-10.Filter for DMIC_CLK**

### 49.3.2 LPC

- LPC clock and signals may have EMI/RFI risk due to its high-order harmonics.
- Recommend to have stripline routing and a RC filter before being routed in microstrip/cable to reduce high-frequency harmonics.
- The RC value may vary according to the board design. Refer figure below.

**Figure 49-11.Filter for LPC_CLK**

### 49.3.3 Integrated Touch (SPI)

- The SPI interface used in integrated touch may have EMI concerns.
- Recommend to use shielded cable for both clock and signal. Refer figure below for noise comparison.

## Figure 49-12.Noise Comparison - With Shield and Without Shield

## Figure 49-13.SPI Cable Shielding

## 49.3.4 Crystal (Xtal) RF Immunity

- The 24 MHz crystal that provides the input clock to the PCH Integrated Clock Controller has been identified to be very sensitive to RF power from nearby radios.
- Radiated power from internal WWAN and WLAN antennas as well as from external WWAN devices placed near the platform can couple to the crystal and corrupt the clock signal causing issues such as screen flickering and system hang.
- Similarly the crystal used with the Thunderbolt Interface Controller is very sensitive to RF power and noise from nearby antennas can result in connection loss with the device plugged into the Thunderbolt port.
- Refer to Thunderbolt design collateral for xtal spec and recommended xtal part. (Document #563553)

The following RF Immunity Guideline applies to both the 24MHz crystal as well as the Thunderbolt/retimer crystal.

### 49.3.4.1 RF Immunity Guidelines

- For 24MHz nssc differential clock: Ideally, for RF immunity, the traces between PCH and CPU should be covered by GND plane.
- Ensure that external HSIO (SATA, USB3.1, DP) and internal HSIO (PCIe) traces are not routed in close proximity to the crystal components and traces (XTAL_IN/OUT)
- Follow crystal routing guidelines very carefully. (Refer to Platform Clock Design Guidelines section)
- Add a series 0-Ohm resistor stuffing option on XTAL_IN and XTAL_OUT traces as a reserved option for possible debug and mitigation to unintended RF power effects, refer to below figure. Intel has only done limited validation of mitigation options and recommends customers to do additional testing.
- Add a ground ring surrounding crystal part, related components and routing may help to reduce the EMI risk. Refer to below figure. Do not connect external load caps to GND ring, but rather directly to GND plane on adjacent layer.
- Use a shielded crystal component.
- Place crystal far away from antennas and potential RF power coupling paths such as unshielded/ungrounded cables. Exact distance needed depends on platform design.
- Platforms without board shield have higher risk.
- WWAN antennas pose higher risk than WLAN antennas because of WWAN's higher transmit power.

**Figure 49-14. 0-Ohm Series Resistors for Crystal Signals**

## 49.3.5 EMC Sensitive Nets

The following nets may be sensitive to ESD injection based on measurement on KBL platform. Similar trends are expected on CFL platform.

**Table 49-1. Sensitive Nets**

| Net Name |
|---|
| PROCHOT_N |
| XTAL_IN |
| XTAL_OUT |
| VCCST_PWRGD |
| GPP_E_9_USB2_OCB_0 |
| VCCAPLLEBB |
| VCCDUSB_1P0 |
| VCCAPLL_1P0 |
| DRAM_RESETB |
| VCCDTS_1P0 |

System-level ESD issue may be mitigated by,

- Routing sensitive nets as stripline.
- Adding decoupling capacitors on the sensitive nets to reduce the ESD level injected into the victim ICs (excluding crystal oscillator). The value of capacitor varies on different nets and systems. The recommended value is 1-100 nF. Refer figure below.

**Figure 49-15. De-coupling Capacitor for Sensitive Net**

- Follow specific guideline of crystal layout (Refer to document #564413).

# 49.4 Connectors

## 49.4.1 General Guidelines

- Proper ground shielding for the connector can reduce the radiation.
- Proper contact to the chassis of host platform can reduce the radiation.
- Recommend to have multiple ground points between receptacle and plug.

## 49.4.2 USB

- Radio antennas (Wi-Fi, WWAN, GNSS, etc) need to be placed away from USB3.1 type-A connector to avoid radio-frequency interference (RFI).
- Wi-Fi antennas need to be at least 3" away to avoid significant Wi-Fi performance degradation.

**Figure 49-16.Measurement Results**

### 49.4.2.1 USB Type-C Connector Considerations

Following are the recommendations for Type C receptacle connector selection.

**Figure 49-17.Improper Shielding for USB Connectors**

## Figure 49-18.Proper Shielding For Connectors

## Figure 49-19.USB3 Type-A Connector Shielding

### 49.4.3 Audio Jack

- Audio jack needs to have EMI/ESD protections composed of ferrite beads and decoupling capacitors.
- The decoupling capacitors need to connect the digital/chassis ground. Refer figure below.

**Figure 49-20.Filter Circuit for Audio Jack**

## 49.5 Cables/ Shielding

### 49.5.1 Shielded FFC

- Internal Cables are frequently used to carry high speed signals such as USB3, eDP, MIPI CSI etc. Noise from such high speed interfaces can radiate and cause EMI, RFI issues.
- A shielded FFC cable may be used as an alternate to expensive three-layer FPC cables. The method by which the shield layers of a flexible cable are contacted to ground has a significant impact on the RFI performance and noise radiation reduction.
- In order to make the shielding effective, the shield layer cannot be floating. A floating shield does not provide a return current path and may even make the noise radiation worse.
- When the shield ground connection is through the ground pins as in below figure (A) the return path inductance could still be high when compared to the PCB ground connection. This results in higher noise radiation.
- To improve the ground contact of the shield, a direct PCB connection of the shield, shown in below figure (B) is recommended. Using conductive tape or an EMI gasket, the shield of the cable is made to directly contact a ground pad on the PCB.
- The near-field scanning plots in below figure (C), (D) and (E) show the comparison of the RFI from an unshielded cable, shielded FFC with ground pin connection and shielded FFC with the recommended direct PCB ground contact.
- As can be seen in below figure (E), the RFI is significantly reduced even half inch away from the cable.

**Figure 49-21.Shielded FFC Cable Design Recommendations**

## 49.6 PCB CMC Technology

- To provide a low-cost alternative to using discrete CMCs, Intel has developed a PCB embedded common-mode filter solution to mitigate radio frequency interference (RFI). Compared to conventional discrete CMC solutions, the PCB-CMC only consumes slightly larger PCB space but without the extra cost.
- PCB-CMC technology is designed specifically for RFI mitigation, and it can be applied to high speed differential data interfaces such as USB 3.1, eDP, and HDMI.

- For access to Intel PCB-CMC technology, a legal agreement is required. To proceed or check status of License/Evaluation Agreement with Intel for the PCB-CMC Technology, please contact your Intel field representative. For the latest and most complete information on PCB-CMC technology refer to the Intel White Paper# 546122.

**Figure 49-22.PCB CMC**

| | 4-layer PCB-CMC | 6-layer PCB-CMC | 6-layer-X PCB-CMC 5mm | 6-layer-X PCB-CMC 3mm |
|---|---|---|---|---|
| Layout | | | | |
| Stack-ups supported | Type 3 & 4; 4-layer | Type 3 & 4; 6,8&10-layer | Type 3 & 4; 6,8&10-layer | Type 3 & 4; 6,8&10-layer |
| Typical application | Desktop, AIO, daughter card | Notebook, Ultrabook, tablet | Notebook, Ultrabook, tablet | Notebook, Ultrabook, tablet |
| Signal speed supported | Up to ~5 Gbps | Up to ~5 Gbps | Up to ~10 Gbps | Up to ~10 Gbps |
| RFI mitigation | WLAN, WWAN | WLAN 2.4GHz, WWAN | WLAN, WWAN | WLAN |
| Common-mode filter BW | 1.8GHz – 6GHz | 1.8GHz – 3.7GHz | 1.8GHz – 6GHz | 2.4-2.5GHz & 5-6GHz |
| Differential Insertion Loss | -3dB @ 7.5GHz | -3dB @ 7.5GHz | -3dB @ 10GHz | -3dB @ 10GHz |

## 49.7 Components Selection

Below components are used for internal reference design. Intel does not recommend a specific part/device or circuit because each solution is board/chassis/usage model specific. Customers should choose the components on their own based on the recommended components specifications. Refer below tables for some examples of CMC and ESD components for different interfaces.

***Note:*** Due to routing limitations, full stripline routing may not be possible. Recommend <25.4mm microstrip routing at break-out region and <25.4 mm microstrip routing at connector region to reduce EMI/RFI risk.

**Table 49-2. Examples for CMC Components Selection (Sheet 1 of 2)**

| Interface | Routing | Cable | Placement | Cutoff Frequency (3-dB Band width) | Insertion Loss | CM Rejection (10-dB Band) | Reference part |
|---|---|---|---|---|---|---|---|
| USB 2.0 | Stripline | Shielded FPC/FFC/ Coax | <25.4mm from connector | - | <0.2 dB @240 MHz | 0.5-2.0 GHz | DLW21SN900SQ2L ACM2012-900-2P-T002 |
| USB 3.1 Gen1 | Stripline | Shielded FPC/FFC/ Coax | <25.4mm from connector | >7.5 GHz | <1.5 dB @2.5 GHz | 1.8-3.8 GHz | PCB CMC: MCF06052G120 |
| USB 3.1 Gen2 | Stripline | Shielded FPC/FFC/ Coax | <25.4mm from connector | >10 GHz | <1.2 dB @ 5 GHz | 1.8-3.8 GHz | PCB CMC: NFP0QHB372HS2 |

## Table 49-2. Examples for CMC Components Selection (Sheet 2 of 2)

| Interface | Routing | Cable | Placement | Cutoff Frequency (3-dB Band width) | Insertion Loss | CM Rejection (10-dB Band) | Reference part |
|---|---|---|---|---|---|---|---|
| HDMI | Stripline | Shielded FPC/FFC/ Coax | <25.4mm from connector | >6 GHz | <0.8 dB @1.5 GHz <1.3 dB @3 GHz | 0.3-3.8 GHz | DLP11SA900HL2 |
| DP | Stripline | Shielded FPC/FFC/ Coax | <25.4mm from connector | >10 GHz | <1.2 dB @ 5 GHz | 1.8-3.8 GHz | PCB CMC NFP0QHB372HS2 |
| eDP | Stripline | Shielded FPC/FFC/ Coax | <25.4mm from connector | >10 GHz | <1.2 dB @ 5 GHz | 1.8-3.8 GHz | PCB CMC NFP0QHB372HS2 |
| SATA | Stripline | Shielded FPC/FFC/ Coax | <25.4mm from connector | >7.5 GHz | <1.5 dB @ 5 GHz | 1.8-3.8 GHz | PCB CMC MCF06052G120 |

## Table 49-3. Filter requirements for other interfaces

| Interface | Routing | Cable Shielding | Placement |
|---|---|---|---|
| SPI | Stripline | Shielded FPC/FFC/Coax | Placeholder for shunt capacitor |
| DMIC | Stripline | - | 22 Ω + 27 pF (Placeholder) |

## Table 49-4. Examples for ESD Components Selection

| Interface | Routing | Cable | Placement | Shunt Capacitance | Rdyn | Reverse working voltage | Reference part |
|---|---|---|---|---|---|---|---|
| USB 2.0 | Stripline | Shielded FPC/ FFC/Coax | <25.4mm from connector | <1.5 pF | <0.8 Ohm | <6 V | ESD105-B1-02ELS CM1230 |
| USB 3.1 Gen1 | Stripline | Shielded FPC/ FFC/Coax | <25.4mm from connector | <0.5 pF | <0.5 Ohm | <6 V | ESD102-U4-05L |
| USB 3.1 Gen2 | Stripline | Shielded FPC/ FFC/Coax | <25.4mm from connector | <0.35 pF | <0.5 Ohm | <6 V | PUSB3FR4 |
| HDMI | Stripline | Shielded FPC/ FFC/Coax | <25.4mm from connector | <0.4 pF | <0.5 Ohm | <6 V | ESD102-U4-05L |
| DP | Stripline | Shielded FPC/ FFC/Coax | <25.4mm from connector | <0.4 pF | <0.5 Ohm | <6 V | ESD102-U4-05L |
| SD CARD | Stripline | Shielded FPC/ FFC/Coax | <25.4mm from connector | <0.4 pF | <0.5 Ohm | <6 V | ESD102-U4-05L |
| Thunderbolt | Stripline | - | <25.4mm from connector | <0.35 pF | <0.5 Ohm | <6V | PESD5V0H1B |

**Table 49-5. Other Critical Decoupling Capacitors and EMI Filtering Components**

| Interface | Component Requirement | Recommended Part Number/ Part Value |
|---|---|---|
| AC JACK | Ferrite Bead on power and ground pins of AC JACK | BLM18SG121TN1 |
| Voltage Regulator | EMI filter at the voltage input (ferrite, diode, resistor) | Refer **Section 49.2** |
| XTAL | Series 0-ohm resistors | Refer **Section 49.3.4** |
| VCC_IN, VCC_AUX | Decoupling caps | Refer **Chapter 50** |
| Type C Connector | Decoupling caps on VBUS signal pins (x4) | 0.1uF |
| | Decoupling capacitor on CC1 and CC2 pins | 100pF |
| | Ferrite Bead on VBUS | refer below section, TYPE C EMI and ESD consideration |

## 49.7.1 Type C EMI and ESD Components

**Figure 49-23.Type C ESD Protection**

For CMC placement on Type C signals, refer below table according to the usage scenario.

**Table 49-6. TYPE C CMC guidelines**

| Port Usage | CMC Guideline |
|---|---|
| USB3 Only | Place Tx CMCs and RX CMCs are optional |
| USB3 and DP | Place both Tx and Rx CMCs due to emission from DP |
| USB3 and TBT | Do not place either Tx and Rx CMCs |

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# 50 Processor and PCH Power Integrity Recommendations

This chapter details the decoupling and layout recommendations for the processor and PCH.

**Table 50-1. Reference Documents**

| Title | Document Number / Location |
|---|---|
| Coffee Lake Platform Device Power Targets and Related Recommendations | 571086 |
| Coffee Lake Turbo and Thermal Power Management Guide for Intel® Core™-based Processors | 571040 |

## 50.1 Processor Decoupling and Layout Recommendations

Follow processor decoupling capacitor requirements in the following table to ensure component maintains stable supply voltage. The capacitors should be placed as close to the package as possible (100 mils or 2.54 mm nominal) in a location that would effectively decouple the interfaces listed under 'Domain'. All decoupling capacitors need to have at least X5R rating. Intel recommends including pads for extra power plane decoupling capacitors for prototype board designs.

The decoupling requirements in this document are based on a 150-kHz Unity Gain-Bandwidth VR. As a rule of thumb, the assumption of Unity Gain-Bandwidth of a VR is $1/4^{th}$ of the switching frequency ($F_{sw}$). In this case, we're using 600-kHz as the switching frequency in our simulation and the requirements here are based on these assumptions. As for decoupling in CRB reference design, these are based on 150-kHz Unity Gain-Bandwidth VR and hence, the difference in decoupling requirements.

XTAL signals are sensitive to noise. If the XTAL is placed near a noisy power plane and the signal lines are routed without proper isolation, the noise can be coupled from the power planes to the signals and cause issues.

### 50.1.1 Coffee Lake H Processor Layout Recommendation

In order to prevent manufacturing yield loss (open solder joint defects), the surface layer under the package cavity should be voided. This is to avoid package land side capacitors interacting with the board surface model inside package cavity area and ensure SMT yield.

The copper shape and plane inside the cavity are required to be removed. Ideally, PTHs/vias and pads inside the cavity should be avoided. The cavity keepout zone recommendation is shown below.

To account for manufacturing process variations, the optimal design will maintain a distance of 150um from any PTH/via to the package landside capacitors (as measured from the via edge to LSC body outline) inside the cavity.

In the case that PTHs/vias has to be placed inside the cavity area, it is recommended to place them strategically to avoid overlapping with package landside capacitors. Clp/dxf files for landside capacitor locations are also provided in the collateral RDC#572464 Coffee Lake Package Landside Capacitor dxf and clp files. which can be imported into the CAD tool to aid the design.

**Figure 50-1. CFL H 6+2 CPU Cavity Keep Out Zone Recommendation**

**Figure 50-2. CFL H 8+2 Refresh CPU Cavity Keep Out Zone Recommendation**

## 50.1.2 Coffee Lake Decoupling Requirement

### Table 50-2. CFL H 6+2 Bulk Decoupling Example

| Bulk Decoupling Locations | EXAMPLE | Notes |
|---|---|---|
| Vcc Power Plane at VR output | 3x 330uF | Place on top of board, near processor edge |
| $Vcc_{GT}$ Power Plane at VR output | 2x 220uF | Place on top of board, near processor edge |
| $Vcc_{IO}$ Power Plane at VR output | 2x 47uF 0805 | Place close to VR output |
| $Vcc_{SA}$ Power Plane at VR output | 2x 47uF 0805 | Place on top of board, near processor edge |

***Note:*** 220uF aluminium polymer bulk cap listed above should have ESR @ 5m ohm and ESL @ 1.9nH each. These are the values used in power distribution simulations used by Intel. They are not vendor specifications.

### Table 50-3. Decoupling Requirements for CFL H 6+2 Processor (Sheet 1 of 2)

| Domain | Board Edge cap | Backside cap | Notes |
|---|---|---|---|
| Vcc | 5x 47uF 0805 | | |
| | | 12x 22uF 0603 | |
| | | 21x 10uF 0402 | |
| | | 24x 1uF 0201/0402 | |
| | | 24x 0201/0402 (placeholder) | |
| $Vcc_{GT}$ | 3x 47uF 0805 | | Place as close to the BGA as possible |
| | 7x 22uF 0603 | | |
| | | 10x 10uF 0402 | |
| | | 12x 1uF 0201/0402 | |
| $Vcc_{SA}$ | 2x 47uF 0805 | | |
| | 2x 22uF 0603 | | |
| | | 7x 10uF 0402 | |
| | | 1x 1uF 0201/0402 | |
| $V_{DDQ}$ | | 4x 22uF 0603 | |
| | | 11x 10uF 0402 | |
| $Vcc_{IO}$ | | 3x 10uF 0402 | |
| | | 3x 0402 (placeholder) | Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate. |
| $Vcc_{ST}$ | | 1x 1uF 0201/0402 | Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm.<br>Do not route $Vcc_{ST}$ closest adjacent layer over any power net other than ground. |
| $Vcc_{STG}$ | | 1x 1uF 0201/0402 | Must be Ground referenced. Share with 1.0V PCH rail |

## Table 50-3. Decoupling Requirements for CFL H 6+2 Processor (Sheet 2 of 2)

| Domain | Board Edge cap | Backside cap | Notes |
|---|---|---|---|
| $Vcc_{PLL}$ | | 1x 1uF 0201/0402 | Must be Ground referenced. Share with 1.0V PCH rail.<br>Board resistance from BGA to Power gate should be less than 130mOhm. |
| | 1x 22uF/47uF 0805 (placeholder) | | **Placeholder not stuffed.*<br>To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside. |
| $Vcc_{PLL_OC}$ | | 2x 1uF 0201/0402 | Must be Ground referenced. Share with $V_{DDQ}$.<br>Board resistance from BGA to Power gate should be less than 86mOhm. |

***Note:*** High Current Rail assuming 600KHz for VR bandwidth. Higher VR bandwidth assumptions results in lower quantity of MLCC (0805/0603) to meet the same AC loadline.

***Note:*** It is important to make sure that the noise on VCCPLL rail must be limited to the +/-5% VR specification below 150KHz - as this will potentially impact the PLL failing to phase lock. Where necessary, the 0805 placeholder can be stuffed with a 22uF or 47uF to assist noise reduction. While stuffing the 0805 cap may reduce noise coupling, one should still route the PLL rail carefully (i.e. to avoid noisy and high current rail) to mitigate any potential issue.

## Table 50-4. CFL H 8+2 Bulk Decoupling Example

| Bulk Decoupling Locations | EXAMPLE | Notes |
|---|---|---|
| Vcc Power Plane at VR output | 2x 220uF 7343 | Place on top of board, near processor edge |
| | 2x 220uF 7343 | Place on the backside. |
| $Vcc_{GT}$ Power Plane at VR output | 2x 220uF | Place on top of board, near processor edge |
| $Vcc_{IO}$ Power Plane at VR output | 2x 47uF 0805 | Place close to VR output |
| $Vcc_{SA}$ Power Plane at VR output | 2x 47uF 0805 | Place on top of board, near processor edge |

***Note:*** 220uF aluminium polymer bulk cap listed above should have ESR @ 5m ohm and ESL @ 1.9nH each. These are the values used in power distribution simulations used by Intel. They are not vendor specifications.

## Table 50-5. Decoupling Requirements for CFL H 8+2 Processor (Sheet 1 of 2)

| Domain | Board Edge cap | Backside cap | Notes |
|---|---|---|---|
| Vcc | 2x 22uF 0603 | | |
| | 8x 47uF 0805 | | |
| | | 48x 1uF 0201/0402 | |
| | | 42x 10uF 0402 | |
| | | 10x 22uF 0603 | |
| $Vcc_{GT}$ | 3x 47uF 0805 | | Place as close to the BGA as possible |
| | 7x 22uF 0603 | | |
| | | 10x 10uF 0402 | |
| | | 12x 1uF 0201/0402 | |

## Table 50-5. Decoupling Requirements for CFL H 8+2 Processor (Sheet 2 of 2)

| Domain | Board Edge cap | Backside cap | Notes |
|---|---|---|---|
| $Vcc_{SA}$ | 2x 47uF 0805 | | |
| | 2x 22uF 0603 | | |
| | | 7x 10uF 0402 | |
| | | 1x 1uF 0201/0402 | |
| $V_{DDQ}$ | | 4x 22uF 0603 | |
| | | 11x 10uF 0402 | |
| $Vcc_{IO}$ | | 3x 10uF 0402 | |
| | | 3x 0402 (placeholder) | Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate. |
| $Vcc_{ST}$ | | 1x 1uF 0201/0402 | Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm.<br>Do not route $Vcc_{ST}$ closest adjacent layer over any power net other than ground. |
| $Vcc_{STG}$ | | 1x 1uF 0201/0402 | Must be Ground referenced. Share with 1.0V PCH rail |
| $Vcc_{PLL}$ | | 1x 1uF 0201/0402 | Must be Ground referenced. Share with 1.0V PCH rail.<br>Board resistance from BGA to Power gate should be less than 130mOhm. |
| | 1x 22uF/47uF 0805 (placeholder) | | **Placeholder not stuffed.*<br>To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside. |
| $Vcc_{PLL_OC}$ | | 2x 1uF 0201/0402 | Must be Ground referenced. Share with $V_{DDQ}$.<br>Board resistance from BGA to Power gate should be less than 86mOhm. |

***Note:*** High Current Rail assuming 600KHz for VR bandwidth. Higher VR bandwidth assumptions results in lower quantity of MLCC (0805/0603) to meet the same AC loadline.

***Note:*** It is important to make sure that the noise on VCCPLL rail must be limited to the +/-5% VR specification below 150KHz - as this will potentially impact the PLL failing to phase lock. Where necessary, the 0805 placeholder can be stuffed with a 22uF or 47uF to assist noise reduction. While stuffing the 0805 cap may reduce noise coupling, one should still route the PLL rail carefully (i.e. to avoid noisy and high current rail) to mitigate any potential issue.

### 50.1.3 VCCST PLL Jitter Recommendation

VCCST PLL jitter issue was found during Intel internal validation and it was causing by power rail overlapping between VCCSA/VCCST on RVP.

Figure 50-3 below shows the example of PLL jitter from VCCSA/VCCST overlapping on RVP.

**Figure 50-3. VCCSA Ripple (Yellow) vs PLL Phase Error (TIE)**

***Note:*** Phase error is around 80ps while it is preferred to be 40ps or less
***Note:*** Phase error is 100% in sync with VCCSA Voltage ripple

As to avoid this PLL jitter issue, Intel recommend to have a layout oversight with VCCST_VCCPLL routing over other power rails on Coffee Lake RVP #571506 and 573546.

***Note:*** *Intel RVP does not follow the current PDG recommendations for VCCST, VCCPLL and VCCSTG*

Customers should take care to only GND reference VCCST and VCCPLL from beginning to CPU.

### 50.1.3.1 CPU VCCST, VCCSTG, VCCPLL Power Routing Recommendation

**CFL H CPU VCCST, VCCSTG, VCCPLL Power Routing Recommendation**

1. Ideally both 2 & 1 routing channels will have VCCST GND referenced and avoid routing over other power.
2. Routing channel 1 is a must have for VCCST to be GND referenced & not overlap any power planes.

***Note:*** Routing channel 1: VCCST routing between large decoupling capacitor and CPU.
***Note:*** Routing channel 2: VCCST origin to CPU decoupling capacitor.

## 50.1.4 Impedance Spectrum Tool (IST/IFDIM) Testing Requirements and Recommendations

Impedance Spectrum Tool testing requirements and recommendations are shown below.

***Note:*** IST/IFDIM is not directly available to customers, Intel will need these trigger points to support debug of customer issues at Intel validation labs. Intel recommends customers implement the IST tool requirements from this section.

**Table 50-6. IST (IFDIM) Testing Requirements and Recommendations (Sheet 1 of 2)**

| Power Rail Sense Line | Feature | As Shown In | Required or Recommended | Notes |
|---|---|---|---|---|
| Vcc_SENSE / Vss_SENSE | Trigger signals | Table 50-7 and Figure 50-4 | Required | Route to un-stuffed header as shown in Figure 50-4 |
| | Current sense resistors | Figure 50-5 | Recommended | One sense resistor per phase. VRTT loadline data is required if sense resistors are not provided |
| $Vcc_{GT}$_SENSE / $Vss_{GT}$_SENSE | Trigger signals | Table 50-7 and Figure 50-4 | Required | Route to un-stuffed header as shown in Figure 50-4 |
| | Current sense resistors | Figure 50-5 | Recommended | One sense resistor per phase. VRTT loadline data is required if sense resistors are not provided |

### Table 50-6. IST (IFDIM) Testing Requirements and Recommendations (Sheet 2 of 2)

| Power Rail Sense Line | Feature | As Shown In | Required or Recommended | Notes |
|---|---|---|---|---|
| $Vcc_{SA}$_SENSE / $Vss_{SA}$_SENSE | Trigger signals | Table 50-7 and Figure 50-4 | Required | Route to un-stuffed header as shown in Figure 50-4 |
| | Current sense resistors | Figure 50-5 | Recommended | One sense resistor per phase. VRTT loadline data is required if sense resistors are not provided |

***Note:*** ITP/XDP uses the same MBP0 (xdp_bpm<0>) line. Recommend using steering resistors for trigger signal.

### Table 50-7. Coffee Lake SKU IFDIM/IST Ballout Pins on Processor

| | Coffee Lake SKU | Ballout Pin #'s and Names |
|---|---|---|
| 1 | CFL H BGA | BR27 or BPM#[0] |
| | | E3 or IST_TRIG |

### Figure 50-4. IST Trigger Point Implementation Requirement

**Figure 50-5. Current Sense Resistor Recommendation**

## 50.2 PCH Decoupling / Filter and Sense Point Recommendations

Follow decoupling capacitor requirements in the following table to ensure component maintains stable supply voltage. The capacitors should be placed as close to the package as possible in a location that would effectively decouple the pins listed under 'Place capacitors near balls'. Also, all decoupling capacitors need to have at least X5R rating. Pins listed under 'PCH Pins sharing power rail' are recommendations for pin group isolation and power plane routing. Intel recommends including pads for extra power plane decoupling capacitors for prototype board designs.

### 50.2.1 Power Plane Decoupling Recommendations

Refer to vendor's recommendation for exact VR output capacitor to meet the VR output target stated in Chapter 52, "Power Delivery"

## Table 50-8. Decoupling and Power Connection Requirements for CNL PCH-H (Sheet 1 of 2)

| Voltage Supply | Power Rails Pin Name | Pin Number | Edge Cap |
|---|---|---|---|
| V1.05A | VCCAPLL_1P05 | B1, B2, B3, C1, C2 | 1x 1uF, 0402, 5mm |
| | VCCPRIM_1P05 | E1, D1 | 1x 4.7uF, 0402, 5mm |
| | VCCA_BCLK_1P05 | V19 | |
| | VCCA_SRC_1P05 | W19, W20 | |
| | VCCA_XTAL_1P05 | P2, P3 | |
| | VCCPRIM_1P05 | U26, U29, V25, V27, V28, V30, V31 | 1x 1uF 0402, 3mm<br>1x 22uF 0805, 5mm |
| | VCCAMPHYPLL_1P05 | C49, D49, E49 | 1x 1uF 0402, 3mm |
| | VCCPRIM_MPHY_1P05 | W31 | |
| | VCCDUSB_1P05 | W22, W23 | |
| | VCCDSW_1P05 | BG45, BG46 | |
| | VCCPRIM_1P05 | AF31, AG31, AD31, AA22, AA23, AB20, AB22, AB23, AB27, AB28, AB30, AD20, AD23, AD27, AD28, AD30, AF23, AF27, AF30, AE17 | 1x 1uF 0402, 3mm |
| V1.8A/ PCH Integrated 1.8V VRM<br>Note 3,5 | VCCPRIM_1P8 | AG19, AG20, AR15, AN15, BB11 | 1x 4.7uF 0603, 3mm<br>when PCH Integrated 1.8V VRM is used<br>**or**<br>1x 1uF 0402, 3mm<br>when PCH Integrated 1.8V VRM is not used |
| N/A(PCH Integrated 1.8V VRM Output pin)<br>Note 3 | VCCPHVLDO_1P8 | AF19, AF20 | |
| V1.8A/PCH Integrated 1.8V VRM<br>Note3 | VCCPGPPD | AN24 | |
| V1.8A/V3.3A | VCCPGPPA | AN32 | |
| | VCCPGPPBC | AN26, AP26 | |
| | VCCPGPPEF | AE35, AE36 | 1x 0.1uF 0402, 3mm<br>(*placeholder*) |
| | VCCPGPPHK | AC35, AC36 | 1x 0.1uF 0402 3mm<br>(*placeholder*) |
| | VCCPSPI | AN44 | |
| V1.5A/V1.8A/3.3A | VCCHDA | BB14 | |
| V3.3A | VCCPRIM_3P3 | AW9, AY8, BB7, V23, AT44 | 1x 1uF 0603, 3mm<br>Place close to AY8, BB7 pins. |
| | VCCPGPPG_3P3 | AN21 | |
| | VCCPDSW_3P3 | BE48, BE49 | 1x 0.1uF 0402, 3mm<br>(*placeholder*) |
| | VCCRTC | BC49,BD49 | 1x 0.1uF 0402, 3mm<br>1x 1uF 0402, 5mm |
| V0.7-2.0V | DCPRTC | BG47, BF47 | |
| N/A (Internal 1.24V LDO)<br>Note 4 | VCCDPHY_1P24 | AJ22, AJ23, AK22, AK23 | |
| | | BG5 | 1x 4.7uF 0603, 5mm |

### Table 50-8. Decoupling and Power Connection Requirements for CNL PCH-H (Sheet 2 of 2)

| Voltage Supply | Power Rails Pin Name | Pin Number | Edge Cap |
|---|---|---|---|
| V1.05 | VCCMPHY_SENSE | K47 | |
| 0 | VSSMPHY_SENSE | K46 | |

***Notes:***
1. All the edge caps need to be placed close to the power rails pin.
2. Refer Chapter 41 "Electromagnetic Compatibility" for recommended placement.
3. Refer to Section 50.4.1.1 for CNL PCH-H Integrated 1.8V VRM usage guidelines.
4. Make sure AJ22, AJ23, AK22, AK23 are all shorted together on motherboard. Refer to Figure 50-9 for implementation information.
5. Only 1 edge cap is required depending on the PCH Integrated 1.8V VRM implementation. Use 1x 4.7uF 0603 cap when PCH Integrated 1.8V VRM is used; Use 1x 1uF 0402 cap when PCH Integrated 1.8V VRM is not used.

### Table 50-9. Filter Requirements for CNL PCH-H

| Supply | Value | Quantity | Type | Notes |
|---|---|---|---|---|
| VCCA_XTAL_1P05<br>(Pin P2, P3)<br>Note 1, 3 | 2.2 uH | 1 | Series Inductor 0603 | Rated at least 100 mA<br>DCR = 0.33Ω +/- 30% |
| | 22 uF | 2 | Filter Capacitor 0805 | X5R rating |
| VccAMPHYPLL_1P05<br>(Pin C49, D49, E49)<br>Note 1, 3 | 2.2 uH | 1 | Series Inductor 0603 | Rated at least 100 mA<br>DCR = 0.33Ω +/- 30% |
| | 22 uF | 2 | Filter Capacitor 0805 | X5R rating |

***Note:***
1. Placeholder only. Does not need to be stuffed.
2. All capacitors are edge capacitors unless labeled otherwise.
3. 2x 22uF 0603 caps can optionally be used instead of 1x 47uF 0603 caps. Caps should be with X5R temperature characteristics.
4. For LC Filter placeholder, the inductor should be replaced by a 0 ohm resistor.
5. Refer to Figure 50-11 for routing information.

### 50.2.1.1 Alternate Capacitor Selection Considerations:

The MLCC decoupling recommendation listed in the PDG assumes 6.3V rated capacitors. It is recommended to use the capacitors with rated voltage at least 2 times the nominal voltage of the power rails.

When replacing the capacitors recommended in the PDG with different form factor/ value capacitors, one needs to consider the capacitance derating, ESR and ESL difference from the original recommendation. Capacitor derating depends on many different factors, including temperature, DC bias, AC noise, voltage rating, etc. Smaller capacitors tend to have lower capacitance value after derating while in general the ESL is lower as well. Table [1] below shows an example of motherboard capacitor models (ESR/ESL and derated capacitance) used for 1V rails with 6.3V rated capacitors.

**Table 50-10. A capacitor Derating example**

| Form Factor | Rated Capacitance | ESR (mW) | ESL (pH) | Derated Capacitance (uF) |
|---|---|---|---|---|
| 0201 | 0.1uF | 41.2 | 185.6 | 0.064 |
| 0201 | 1uF | 13.1 | 158.0 | 0.601 |
| 0402 | 1uF | 14.7 | 213.9 | 0.575 |
| 0402 | 10uF | 8.4 | 237.9 | 6.057 |
| 0603 | 22uF | 3.9 | 286.9 | 13.946 |
| 0603 | 47uF | 3.2 | 279.4 | 28.901 |
| 0805 | 47uF | 3.0 | 359.0 | 29.915 |

It is critical to understand the design constraints/limitation and ensure the alternative capacitor choice meets the same electrical requirement as the PDG recommendation.

Even though most of the rails can use 1 to 1 replacement ratio (i.e., using 1x 0201 to replace 1x 0402 capacitor with the same value), some sensitive rails may require 2 to 1 ratio.

## 50.2.2 VR Sense Requirements for PCH Rails

### 50.2.2.1 Sense Requirements for V1.05A

The sense point should be placed at the maximum 13 mm - 17 mm away from the MPHY pins. The width of this shape should be at least 15mils. This is required to meet the Vmin at the bumps.

# 50.3 Loop Inductance Reduction Decoupling

To reduce loop inductance and return path of for the decoupling capacitors, it is important to adhere to the (R)unway, and (E)dge decoupling capacitor placement recommended in Figure 50-6 and Figure 50-7.

The idea is to rotate capacitors that set over power planes so that the loop inductance is minimized. The basic theory for minimizing loop inductance is to consider which voltage is on layer two (power or ground) and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance.

The first figure below is an example of (R)unway decoupling capacitor placement, and the second figure is an example of (E)dge decoupling capacitor placement.

**Figure 50-6. Minimized Loop Inductance Example (R)unway**

**Figure 50-7. (E)dge Decoupling Capacitor Placement**

## 50.4 Power Plane Isolation

Customers must adhere to the following board design practices to address noise coupling concerns:

On the same layer, power plane isolation is required for different interfaces on the same power-rail (Example: Clock integration, mPHY, Core, PLLs). Minimum isolation-distance required is until the package edge.

- Avoid overlapping power planes on board stack-up, such as 3.3V referencing 1.05V plane. Reference GND as much as possible.

Power rail isolation is critical in power delivery design in order for proper noise isolation between interfaces. Proper grouping of ball pins and plane isolation for each interfaces is necessary even though they are sharing same voltage supply rail. Refer to Section 50.4.1, "CNL PCH-H Power Rail Isolation and Routing Recommendations" for more information.

## 50.4.1 CNL PCH-H Power Rail Isolation and Routing Recommendations

**Figure 50-8. CNL PCH-H Power Rail Isolation Example**

***Note:*** Figure above shows the example of power plane isolation between VCC plane layer (L2) and some miscellaneous routing on layer 4 (L4) for a 4L board design.

## Figure 50-9. CNL PCH-H Power Rail Isolation Example

**CNL PCH-H VCCDPHY_1P24 Routing**

1. Connect pin BG5 to edgecap with lowest loop inductance possible.
   — Power rails route on surface layer.
   — Ground reference on next layer.
2. Short pins below together at surface layer:
   — AJ22, AJ23, AK22, AK23.
   — It is optional to short pins BG5 to AJ22 and AJ23 together to have improved DC drop performance.

## Figure 50-10.CNL PCH-H 1.05V VRM Senseline Isolation Example

**CNL PCH-H 1.05V VRM Senseline Routing**

- PCH 1.05V VR sense is recommended to be placed close to VCCMPHY_1P05 power plane under package region.

**Figure 50-11.CNL PCH-H Sensitive Rail Filtering and Routing Recommendation**

**CNL PCH-H Sensitive Rail Filtering and Routing Recommendation**

- LC Filter Placeholder needed for jitter sensitive rails: VCCA_XTAL_1P05 and VCCAMPHYPLL_1P05
- Ground shielding is recommended to minimize coupling risk from USB2 signal to VCCA_XTAL_1P05 rail.

### 50.4.1.1 Cannon Lake PCH-H Integrated 1.8V VRM Usage Guidelines

The Cannon Lake PCH-H has an integrated 1.8V VRM using an integrated high voltage low dropout voltage regulator (HVLDO) which may be enabled to output 1.8V for use by the PCH as specified below.

- VCCPHVLDO_1P8 may be used to power VCCPRIM_1P8 if:
  - Platform does not implement 1.8V external VR connected to PCH.
- VCCPHVLDO_1P8 may be used to power both VCCPRIM_1P8 and VCCPGPPD if:
  - Platform does not implement a 1.8V external VR connected to PCH.
  - GPIO Primary Well Group D (GPP_D) is operating at 1.8V.
  - All GPP_D signals are operating in Native mode (instead of GPIO mode).
- Other usage requirements:
  - VCCPHVLDO_1P8 pin may not be connected to any other PCH or platform rail.
  - Platforms that implement a 1.8V external VR powering any of the 1.8V rails of PCH should leave the VCCPHVLDO_1P8 as No Connect. All PCH 1.8V rails should be powered by the external VR.

## Figure 50-12.Scenario 1: Platforms without 1.8V External VR Connected to PCH Recommendation

**Configuration 1: GPP_D operating at 1.8V**

***Note:***

1. Integrated 1.8V VRM connected to VCCPRIM_1P8 and VCCPGPPD.

## Figure 50-12.Scenario 1: Platforms without 1.8V External VR Connected to PCH Recommendation

**Configuration 2: GPP_D operating at 3.3V**

***Note:***

1. Integrated 1.8V VRM connected only to VCCPRIM_1P8.

**Figure 50-13.Scenario 2: Platforms with 1.8V External VR Connected to PCH Recommendation**

**Platforms with 1.8V external VR connected to PCH**

***Notes:***

1. Whenever there is 1.8V external VR, all PCH 1.8V should be coming from the external 1.8V VR.
2. PCH Integrated 1.8V VRM output pins (AF19, AF20) need to be NC when PCH Integrated 1.8V VRM is not used.
3. Using two different source of 1.8V is not recommended, there is potential power sequencing problem and eventually functional issue.

## 50.5 Coffee Lake H Land Pattern Recommendations

Intel's land pattern guidance applies to PCB pad size and pad type design and is developed to maximize solder joint reliability mechanical performance and solder joint quality or SMT/manufacturing while still taking into consideration power delivery and power integrity requirements.

**Table 50-11. Land Pattern Reference Document**

| Title | Document Number |
|---|---|
| Customer Knowledge Sharing: Land Pattern Design Best Known Methods | 516635 |

## Table 50-12. PCB Pad Definitions

| Pad Type | Definition | Description | Illustration |
|---|---|---|---|
| MD | Metal Defined | Traditional dog bone via to BGA-pad. IO driven, trace width usually determined by impedance. | |
| SMD | Solder Mask Defined | Pad 100% defined by solder mask, flood and/or metal trace > pad diameter. | |
| ½ MD | Half Metal Defined | 50% pad is metal defined and the other 50% pad is solder mask defined. | |
| Spoke (X or +) | Spoke pad | Multiple traces connecting pad to nearby flood plane. Used for improved reliability or manufacturability where flood plane is needed. | |
| WTMD | Wide Trace Metal Defined | Trace = pad diameter or less.<br>1WTMD = 1 wide trace to BGA pad. | |
| | | 2WTMD = 2 wide trace to BGA pad.<br>Total thickness of traces should not cover more than 50% of pad circumference (T1 width + T2 width < 50% circumference. | |

## Figure 50-14.Coffee Lake H-Processor Land Pattern Guidance

Total number of balls: 1440

| Legend | Pad Size (microns/mils) ; SRO Size (microns/mils) | Function | # of Balls |
|---|---|---|---|
| ● | MD or Spoked Pad : 305um (12mil)Pad, 406um (16mil) SRO ; SMD Pad: 406um (16mil) Pad, 305um (12mil) SRO | CTF | 1229 |
| ◀ | MD or Spoked Pad : 305um (12mil)Pad, 406um (16mil) SRO | CTF | 108 |
| ▶ | MD or Spoked Pad : 305um (12mil)Pad, 406um (16mil) SRO | NCTF | 30 |
| ■ | MD or Spoked Pad : 330um (13mil)Pad, 430um (17mil) SRO ; SMD Pad: 430um (17mil) Pad, 330um (13mil) SRO | CTF | 26 |
| ◆ | MD or Spoked Pad : 356um (14mil)Pad, 455um (18mil) SRO ; SMD Pad: 455um (18mil) Pad, 356um (14mil) SRO | CTF | 19 |
| ▼ | MD or Spoked Pad : 381um (15mil)Pad, 480um (19mil) SRO ; SMD Pad: 480um (19mil) Pad, 381um (15mil) SRO | NCTF | 19 |
| ▲ | MD or Spoked Pad : 406um (16mil)Pad, 506um (20mil) SRO ; SMD Pad: 506um (20mil) Pad, 406um (16mil) SRO | NCTF | 9 |

**Figure 50-15.Cannon Lake PCH-H Land Pattern Guidance**

Total number of balls: 874

| Legend | Pad Size (microns/mils) ; SRO Size (microns/mils) | # of Balls |
|---|---|---|
| ● | 203.2 X 254um (8 X 10mil) SMD allowed CTF | 248 |
| ▲ | 203.2 X 304.8um (8 X 12mil) SMD allowed CTF | 36 |
| ▼ | 254um (10mil) SMD allowed CTF | 120 |
| ■ | 279.4um (11mil) SMD allowed CTF | 8 |
| ◆ | 304.8um (12mil) SMD allowed CTF | 434 |
| ◀ | 304.8um (12mil) SMD allowed nCTF | 28 |

§ §

# 51 Power Delivery

This chapter provides guidelines for the Coffee Lake platform power delivery solution. The platform power delivery is comprised of an IMVP8 voltage regulator (VR), Rest of Platform (ROP) VRs, load switches, battery charger, battery and fuel gauge, AC/DC adapter, power and current monitors, USB Type C power delivery and Power Sequencing.

- IMVP8 VR(s) regulate power to the CPU and graphics core of the processor. Details are provided in Section 51.2.
- Rest of Platform (ROP) VRs regulate power to the PCH and rest of the system components. Discrete VRs or a PMIC can be used to supply ROP rails. Details are provided in the Power Map Section 51.1.
- Load Switches gate power to various SoC and ROP blocks to save power. Details are also provided in the Power Map Section 51.1.2.
- Battery Charger considerations are discussed in Section 51.6.
- Battery Fuel Gauge considerations are discussed in Section 51.8.
- AC/DC Adapter considerations are discussed in Section 51.5.
- $P_{SYS}$, the System Input Power Monitor is discussed in Section 51.7.
- USB Type C Power Delivery is covered in **Chapter 20**
- Power Sequencing is covered in **Chapter 45**

## 51.1 Power Maps

### 51.1.1 Power Map Tool

The Platform Power Map diagrams key specifications of the voltage regulators (IMVP8 and ROP VRs), load switches and the loads. To provide more flexibility in power design, power maps are now provided as a separate configurable tool. This tool is also where Default and Extreme power limits (PL2, PL4) are provided. Refer to Coffee Lake H Platform Power Map Design tool to generate a power map that accompanies this section. The Power Map tool will be in the same collateral list as this document on www.intel.com.

***Note:*** **The processor and PCH EDS specification documents take precedence and will override any conflicts with what is being stated herein.**

### 51.1.2 Load Switch Sizing

For SoC power rails requiring load switches, platform designers will need to select a load switch with an appropriate resistance/$R_{dson}$ target to ensure that the voltage specifications at the SoC are met. As a general rule of thumb, the IR drop across the load switch should not exceed more than 1% of the voltage supply value under Iccmax conditions. Platform designers can adjust this target higher or lower to optimize the

load switch selection for a specific motherboard design based on parameters such as the tolerance of the sourcing VR design, the resistance of the layout path from the VR to the load switch and finally to the CPU, VR sense location, etc.

### 51.1.3 Trade-offs - Volume vs. Premium Power Maps

Power maps are broken into two tiers: Volume and Premium. Volume focuses on cost savings with the fewest VRs and Premium focuses on the smallest solution size with the lowest power consumption. For a design focused on S0ix or Modern Standby* power, the Premium power map is recommended. The designer may choose to implement a hybrid between Volume and Premium as long as guidelines are followed.

**Table 51-1. Differences between Power Maps**

| Volume | Premium |
|---|---|
| VccST gated by SLP_S4# | VccST gated by SLP_S3# |
| Various system devices share load switches | Various system devices have their own independent load switches |
| VccPLL_OC is supplied directly from VDDQ | VccPLL_OC is supplied from VDDQ through a load switch |
| ***Note:*** Other changes may be present. Refer to the Power Map tool for details. | |

Estimated power deltas of each SoC load between different configurations is shown in table below.

**Table 51-2. Estimated Power Deltas between Different Configurations**

| Configuration | | Estimated SoC Power Delta from Config #1 to #2 |
|---|---|---|
| **Config #1 (Premium)** | **Config #2 (Volume)** | **CFL H** |
| VccST off in S3 | On in S3 | +25-30mW |
| VccPLL_OC off in S0/C10 | On in S0/C10 | +3-10mW |
| VccPLL_OC off in S0ix | On in S0ix | +3-10mW |

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

**CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (CFL H) in the S0/C10 system state in order to save power.**

Ensure fast ramp-up timing requirements can be met as described in Section 45.4.1, "Power Sequencing Timing Requirements"

To save power in S0 idle (for example Windows* idle), it is recommended to power gate VccSTG in the S0/C10 state even in "Volume" designs. VccSTG should be gated by {SLP_S3# AND CPU_C10_GATE#}.

VccPLL_OC must powered off whenever VccST is off.

**Table 51-3. Enable Signal Implementations for VccST and VccPLL_OC**

| VccST Load Switch Enable | Supported VccPLL_OC Load Switch Enables |
|---|---|
| SLP_S3# | SLP_S3#, or<br>{SLP_S3# AND CPU_C10_GATE#} |
| SLP_S4# | No gating required (tied to VDDQ), or<br>SLP_S3#<br>, or<br>{SLP_S3# AND CPU_C10_GATE#} |

Both Premium and Volume configurations can be used for systems that support the S0ix / Modern Standby state however power may be higher in that state with the Volume configuration.

Platform/silicon debug functionality may require that some platform rails be powered up in states where they would normally be unpowered under a normal usage scenario. Platforms that require the ability to use this debug functionality must support powering the proper rails in the proper power states.

### 51.1.4 VccSTG Rail Discharge Requirements

As long as VccST and VccSTG are power gated separately, the following requirements are critical to prevent system failure on Coffee Lake:

1. VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal $R_{discharge}$ <= 300Ω to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.
2. If VccST/VccPLL has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal $R_{discharge}$ <= VccST/VccPLL $R_{discharge}$.
3. The total capacitance on VccSTG <= total capacitance on VccST/VccPLL.

## 51.2 Processor Power Delivery Guidelines

This section provides the general processor voltage rail design guidelines.

### 51.2.1 General Processor Power Delivery Considerations

An IMVP8 VR regulates power to the processor core. The IMVP8 Pulse Width Modulation (PWM) Specifications define the DC-DC VR electrical requirements.

CFL H uses IMVP8 to power the processor, graphics, and system agent.

Figure 51-1 is a generic representation of the IMVP8 VR. Other features and implementations are definitely possible.

**Figure 51-1. IMVP8 VR Block Diagram**

Important points to note in these block diagrams are:

- IMVP8 requires differential remote sensing. Differential sense inputs for a given rail must be the ONLY feedback point back to controller. Refer to Table 51-4.
- VR_Ready is a required controller output signal. It indicates that VR is operational. VR_Ready signal is also used for appropriate power up sequencing during a platform boot.
- IMVP8 compliant controller is required to provide VR_HOT# (VR Thermal Throttling) output signal to indicate operation close to regulator maximum thermal limit. It is used by the system to prevent catastrophic thermal damage.
- VR_ENABLE (IMVP8) is required signal provided by platform logic. It enables the outputs of IMVP8 regulators.

## 51.2.2 Testing and Validation

The nominal processor voltage is determined by an SVID code provided to the VR. The VID nominal value indicates the reference point that the VID provides for the static and ripple voltage tolerance. Due to VR tolerances, PCB parasitic and current draw variations, the average voltage seen at the processor may be slightly higher or lower than the reference value according to the loadline spec or tolerances.

The VR must meet the static, ripple, and loadline tolerance limits for the entire range of processor load. Loadline, static and ripple tolerance window specifications must be met as measured differentially at Vcc_SENSE/Vss_SENSE pins.

Frequency Domain Impedance Measurement (FDIM) testing is also expected to be completed up to 1MHz on every IMVP8 power rail.

Refer to *Coffee Lake Platform Power Validation Plan* for guidance on validating power delivery and FDIM test requirements.

### 51.2.3 Audible Noise Reduction

At least three conditions need to be simultaneously present for acoustic noise. They are periodic dv/dt in the audible range, sufficient dv magnitude, and insufficient damping, e.g. typical of a heavily-reliant or all-MLCC decoupling solution. The noise amplitude increases with current in I = C * dv / dt.

Ways to minimize the acoustic noise are:

- Control the in-rush current by sizing the output capacitor to just meet the transient requirement without excess
- Proper selection of inductors; taking core material, construction, mechanicals, and mounting into account to mitigate any potential inductor-induced “buzz” noise.
- Low-ESR MLCC's are notorious for potential audible noise, especially when exposed to large dv/dt events. This is due to the Piezo effect. The noise magnitude is proportional to the number of MLCC's used. Potential steps to take are:
  - Buck Regulator Input Filter. The highest peak-to-peak voltage/current stresses (dV/dt, dI/dt) of a Buck regulator are handled by the input filter caps
    - The input filter MLCC's should be (2) 4.7µF X5R per phase
    - Avoid Y5V dielectric MLCC's, as experience shows them more susceptible to the Piezo effect
    - Physical placement is important, e.g. co-locate MLCC pairs either side of the input FET, not side-by-side
    - Increase the capacitance to 10uF if needed to minimize the noise
    - Where possible, large input bulk capacitors should be used-(2) 680 µF or larger-to minimize the dv/dt events
  - Buck Regulator Output Decoupling
    - For output high frequency decoupling, use 22µF or higher valued MLCC's to reduce the number of needed capacitors
    - Use polymer chip capacitors in conjunction with MLCC's, when possible
  - Placing MLCC's symmetrically on the top- and bottom-sides of the motherboard introduces mechanically-opposed forces, helping mitigate any vibration, and reducing the noise magnitude

**Figure 51-2. Input Voltage Droop Caused by dv/dt Event at Output**

## 51.2.4 Vcc_SENSE/Vss_SENSE Package Sensing

Motherboards are subject to layout area constraints that could significantly compromise a VR's placement on the motherboard and its connection to the processor pins. To ensure that the power delivery network's (PDN) impedance profile stays at/below the maximum loadline target for frequencies above the VR's Gain-Bandwidth (G-BW), the placement and connection of the decoupling capacitors as well the shapes of the power plane(s) is critical. At frequencies within the VR's G-BW control, the VR layout placement may be compensated using remote sensing of the voltage at the die through Vcc_SENSE/Vss_SENSE signals.

The processor implements the concept of “package sensing” for IMVP8 voltage rails; the following examples use Vcc/Vss as general labels. Note: for optimal performance and noise rejection, the feedback signals for the IMVP8 controller should be routed as if they are a differential pair connecting the Vcc and Vss bumps of the processor to the IMVP8 controller Vcc_SENSE and Vss_SENSE pins respectively. This is true for non-IMVP8 rails too. This implementation extends the VR controller's regulation range, enclosing the motherboard parasitics within its feedback loop minimizing the impact on voltage regulation. The conceptual implementation of Vcc_SENSE/Vss_SENSE package sensing is illustrated in Figure 51-3 with recommendations in Table 51-4.

## Table 51-4. Package Sensing Recommendations

| Power Rail Sense Line | R1,R2 | Trace Impedance | Trace Length Match |
|---|---|---|---|
| | 100Ω | 50Ω | <25 mils |
| Vcc_SENSE /Vss_SENSE | | | |
| $Vcc_{GT}$_SENSE / $Vss_{GT}$_SENSE | | | |
| $Vcc_{SA}$_SENSE / $Vss_{SA}$_SENSE | | | |
| $Vcc_{IO}$_SENSE / $Vss_{IO}$_SENSE[1] | | NA | |

***Note:***
1. Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/ Vss_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain 25-mil separation distance away from any other dynamic signals

## Figure 51-3. Example of Processor Vcc_SENSE/Vss_SENSE Package Sensing

- Figure above demonstrates the purpose/function of the feedback "catch" resistors. As discussed above package sensing effectively encloses the board parasitics within the feedback loop of the VR; however, a problem arises when the DUT is not present; the feedback loop is open and the VR does not have any feedback. Aberrant or unstable VR behavior may result, including overvoltage, errant/ sporadic VR operation, etc. This may potentially damage motherboard components like the bulk decoupling capacitors. The "catch" resistors serve to close this feedback path, "bypassing" the Vcc_SENSE/Vss_SENSE connections through the processor and providing the necessary closed-loop feedback to the VR.
- Operation: The processor Vcc_SENSE/Vss_SENSE package traces are shunted to the motherboard Vccx and Vssx planes via the catch resistors R1 and R2. R1 and R2 are sized large in relation to the sense lines impedance so not to cause error when the DUT is present.
- Some additional guidelines:

— R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

— Preserve the transmission line integrity of Vcc_SENSE/Vss_SENSE lines by avoiding stub routing to R1, R2 catch resistors.

— Note: For systems using a BGA packaged processor catch resistors are optional.

## 51.3 IMVP8 Voltage and Current Requirements- H-Line

An IMVP8 compliant VR supplies the required voltage and current to the processor's IMVP8 based voltage rails of a single processor. The VID nominal value indicates the reference point for the static and ripple voltage tolerance.

Each IMVP8 VR output must meet the specifications in the processor EDS at remote sense processor pins.

Due to VR tolerances, PCB parasitic and current draw variations, the average voltage at the processor may be slightly higher or lower than the reference value. However, the VR must meet processor static and ripple tolerance limits over the entire range of processor load. The following conditions apply to the specifications:

- Applies to all frequencies unless specific frequencies are listed
- Applies to full temperature range
- Icc is measured at the nominal VID Vcc value under maximum signal loading conditions such as running a power virus program.
- Applies to full input power rail range
- The nominal VID voltage, voltage tolerance, and maximum current values are for reference only. Refer to the appropriate component documentation for the most current specifications.

An IMVP8 compliant VR must be designed to:

- Temporarily support “IPL2”currents during a PL2 event for the respective tau duration their VR can thermally support.
- Momentarily support the processor’s maximum current (VR’s electrical design constraint)
- Operate within spec under the worst-case dynamic/loaf transient events

**Refer to the processor’s EDS for detailed processor specifications. Values shown in this document represent voltage plane design guidelines, not processor specifications.**

### Table 51-5. General Processor VR Parameters for CFL H62, CFL H42 and CFL H82 (Sheet 1 of 2)

| Symbol | Description | Parameter Values | Notes |
|---|---|---|---|
| VCC,VCCGT, VCCSA,VID | VID Range | 0 V-1.52 V | |
| VCC, VCCGT VBoot | VBoot Setting | 0V | |

## Table 51-5. General Processor VR Parameters for CFL H62, CFL H42 and CFL H82 (Sheet 2 of 2)

| Symbol | Description | Parameter Values | | Notes |
|---|---|---|---|---|
| VCCSA VBoot | VBoot Setting | 1.05V | | |
| VID1 | Test VID | 0.9V | | |
| VID2 | Test VID in Low Freq Mode | 0.6V | | |
| VID3 | Test VID in PS3 | 0.3V | | |
| Icc_PS1 | Max Current in PS1 state | 20 A | | |
| Icc_PS2 | Max Current in PS2 state | 5 A (4A max transient) | | Transient loads will be from 1A to 5A |
| Icc_PS3 | Max Current in PS3 state | 1 A | | Transient loads are not expected |
| +/- ripple (mV) | PS0, PS1, PS2, PS3 | 0 A< Load ≤ 0.5 A | +30mV/ -10mV | |
| | PS0 | 0.5A < Load ≤ $I_{TDC}$ | +/- 10mV | |
| | | $I_{TDC}$ < Load≤ IccMax | +/- 15mV | |
| | PS1 | Load > 0.5 A | +/- 15mV | |
| | PS2 | Load > 0.5 A | +30mV/ -10mV | |
| | PS3 | Load > 0.5 A | +30mV/ -10mV | |
| V_TOB_Imin (mV) | VID1 | +/- 5 | | See Note 3 and 4 |
| | VID2 | +/- 8 | | |
| | VID3 | +/- 8 | | |
| V_TOB_Imax (mV) | PS0 | +/- 20 | | |
| | PS1 | +/- 20 | | |
| | PS2/ PS3 | +/- 20 | | |
| Max Slew rate | For VID changes <= 50mV | 200 mV/us | | |
| | For VID changes > 50mV | 90 mV/us | | |
| R_DC_LL (mV/A) MAX | Loadline slope within the VR regulation loop capability 0-1kHz | VCC | 1.8 | Load line slope within the VR regulation loop capability 0-1kHz |
| | | VCCGT | 2.7 | |
| | | VCCSA | 10.3 | |
| R_AC_LL (mV/A) MAX | Loadline slope in response to dynamic load increase events 1kHz-1MHz | VCC | 1.8 | Load line slope in response to dynamic load increase events 1kHz-1MHz |
| | | VCCGT | 2.7 | |
| | | VCCSA | 10.3 | |

***Notes:***
1. Refer to applicable processor Electrical Design Specification (EDS) for latest electrical parameters.
2. Processors will spend more time operating at thermal design point. VR should be designed to efficiently deliver power at TDC and beyond.
3. These are Intel default values and are used in the calculation of Min and Max LL slope tolerances in this table. Values obtained from the VR vendor based on the VR design may be used here as well, but they will change the calculation results.

4. Icc_PS1, Icc_PS2 and Icc_PS3 values are default settings. Consult BIOS Writers Guide (Chapter 1, "Introduction") for possible methods to overwrite them. Icc PS1 max current should not exceed the domain

## Table 51-6. Processor VR Overshoot values

| Parameter | Vcc | | $Vcc_{GT}$ | $Vcc_{SA}$ |
|---|---|---|---|---|
| | IccMAX_App transients | IccMAX transients | IccMAX transients | IccMAX transients |
| VOvS_Max (Max overshoot voltage) [mV] | 70 | 200 | 70 | 200 |
| tOvS_Max (Max Overshoot time duration) [us] | 10 | 30 | 10 | 30 |

## Table 51-7. Processor VR Design Values

| Parameter | Vcc | $Vcc_{GT}$ | VCCSA |
|---|---|---|---|
| **CFL H 42 45W** | | | |
| IPL2 [A] | 60 | 25 | 10 |
| IccMax current 10 ms max | Refer to the EDS for the IccMax numbers | | |
| IccMax_App current | 85% of IccMax | NA | |
| di (IccMax transient) [A] | 69 | 26 | 3 |
| di (IccMax_App transient) | IccMax_App di = IccMax_App - (IccMax - IccMax di) | NA | |
| dt (ns) (Slew time for the di step) (Note 3) | 65 | 65 | 200 |
| **CFL H 62 45W** | | | |
| IPL2 [A] | 80 | 25 | 10 |
| IccMax current 10 ms max | Refer to the EDS for the IccMax numbers | | |
| IccMax_App current | 85% of IccMax | NA | |
| di (IccMax transient) [A] | 91 | 24 | 3 |
| di (IccMax_App transient) | IccMax_App di = IccMax_App - (IccMax - IccMax di) | NA | |

### Table 51-7. Processor VR Design Values

| Parameter | Vcc | $Vcc_{GT}$ | VCCSA |
|---|---|---|---|
| dt (ns)<br>(Slew time for the di step) (Note 3) | 65 | 65 | 200 |
| CFL H 82 45W | | | |
| IPL2 [A] | 86 | 25 | 10 |
| IccMax current<br>10 ms max | Refer to the EDS for the IccMax numbers | | |
| IccMax_App current | 85% of IccMax | NA | |
| di<br>(IccMax transient)<br>[A] | 110 | 24 | 3 |
| di<br>(IccMax_App transient) | IccMax_App di = IccMax_App - (IccMax - IccMax di) | NA | |
| dt (ns)<br>(Slew time for the di step) (Note 3) | 65 | 65 | 200 |

1. All references to "TDC" in this document refer to PL2 current events. PL2 is a temporary event whose duration will be determined by the thermal capability of both the platform thermal solution and VR design.
2. IccMax_APP is not a spec. It is a characterization of limited samples using limited set of benchmarks under default PL1 and PL2 conditions. It aims to show more realistic current envelope that can be exceeded.
3. Simulated at processor motherboard pads. This parameter is not tested.
4. The time durations given here are for VR design only.
5. If using Psys, Intel recommends sizing the VR's thermal solution to support the domain's equivalent PL2 max TDC currents. By continually monitoring the platform's total power dissipation, Psys optimizes the AC adapter's PsysPL2 power capability, maximizing PL2 power delivered to the CPU(e.g. PL2 max operation) when rest-of-platform power headroom exists allows. Note: PsysPL2 is the sum of PL2 and ROP as measured at the power input. As ROP is reduced PL2 may increase, PsysPL2 remaining constant.
6. The SET VR TDC CONFIG mailbox register in the BIOS assumes a default tau of 1ms.

## 51.4 Voltage Regulator Requirements

***Notes:***

1. The Tolerance requirements have to be met at the package ball if the sense location is not on package. Additional decoupling may have to be added to meet the tolerance if the sense location is far away from the ball.

2. For VRs that implement Low Power mode (LPM) through a dedicated pin, the $T_{LPM_EXIT}$ defines the minimum and maximum time allowed from LPM exit as measured from LPM L' H transition to the active voltage reached, regardless of the duration of the LPM signal L pulse width.

3. For VRs that implement Low Power Mode (LPM) through the ENABLE pin, the $T_{EN}$ defines the maximum time allowed from IC_ENABLE to Vout (nom), regardless of the duration of the ENABLE (low) pulse width.

4. The Platform Power Sequencing Specification (PSS) Chapter in the Platform Design Guide (PDG) has additional requirements and the PSS specs supersede any requirements listed in the PDG.

### Table 51-8. Electrical Requirements for VCCIO VR

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| $V_{NOM}$ | Default voltage | | 0.95 LPM-0 V | | V | Output voltage fixed on platform Refer to EDS for the required voltage level for a given CPU SKU. |
| Tolerance | Output Voltage Tolerance | -50 | | 50 | mV | DC+AC+ripple, DC to 1MHz For all VSEL settings in VCCIOCNT. |
| $T_{LPM_EXIT}$ | Low Power Mode exit Latency | 10 | | 240 | us | If VCCIO is turn off in C10(either through controller LPM pin or ENABLE pin. Time from CPU C10 GATE# de-assertion to VCCIO voltage stable |
| $T_{EN}$ | Turn on delay | 0.0085 | 3 | 5 | ms | For start-up |
| SR | Voltage ramp slew rate | | | 90 | mV/us | |
| $I_{STDBY}$ | Standby Current | | 1 | | mA | |

### Table 51-9. Electrical Requirements for V1.05A VR

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| **Output Requirement** | | | | | | |
| $V_{NOM}$ | Default voltage | | 1.05 | | V | |
| Tolerance | Output Voltage Tolerance | -5 | | 5 | % | DC+AC+ripple, DC to 1MHz |
| $I_{STDBY}$ | Standby Current | | 2 | | mA | |

### Table 51-10. Electrical Requirements for VTT VR

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| **Output Requirement** | | | | | | |
| $V_{NOM}$ | Default voltage | | VDDQ/2 | | V | VTT output voltage must track VDDQ |
| Tolerance | Output Voltage Tolerance | -5 | | 5 | % | DC+AC+ripple, DC to 1MHz |
| $I_{Trasient}$ | Trasient Load Step | | | 1.2 | A | -600mA to 600mA for decoupling design |

***Note:*** The voltage specification requirements are measured on VTT line as near as possible to the termination resistor with an oscilloscope with 3 x CLK bandwidth, 1.5pF maximum probe capacitance, and 1MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5mm. Ensure external noise from the system is not coupled into the oscilloscope probe. Or use differential probe between VTT and GND. All VTT net need to be measured separately.

### Table 51-11. Electrical Requirements for VDDQ VR

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| **Output Requirement** | | | | | | |
| $V_{NOM}$ | Default voltage | | 1.2 | | V | For DDR4 |
| Tolerance | Output Voltage Tolerance | -5 | | 5 | % | DC+AC+ripple, DC to 1MHz |
| $I_{STDBY}$ | Standby Current | | 8 | | mA | |

### Table 51-12. Electrical Requirements for V3.3_DSWVR

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| **Output Requirement** | | | | | | |
| $V_{NOM}$ | Default voltage | | 3.3 | | V | |
| Tolerance | Output Voltage Tolerance | -5 | | 5 | % | DC+AC+ripple, DC to 1MHz |
| $I_{STDBY}$ | Standby Current | | 5.3 | | mA | |

### Table 51-13. Electrical Requirements for V5A VR

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| **Output Requirement** | | | | | | |
| $V_{NOM}$ | Default voltage | | 5.0 | | V | |
| Tolerance | Output Voltage Tolerance | -5 | | 5 | % | DC+AC+ripple, DC to 1MHz |
| $I_{STDBY}$ | Standby Current | | 1 | | mA | |

### Table 51-14. Electrical Requirements for V1.8A VR

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| **Output Requirement** | | | | | | |
| $V_{NOM}$ | Default voltage | | 1.8 | | V | |
| Tolerance | Output Voltage Tolerance | -5 | | 5 | % | DC+AC+ripple, DC to 1MHz |
| $I_{STDBY}$ | Standby Current | | 1 | | mA | |

### Table 51-15. Electrical Requirements for V2.5U VR

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| **Output Requirement** | | | | | | |
| $V_{NOM}$ | Default voltage | | 2.5 | | V | |

**Table 51-15. Electrical Requirements for V2.5U VR**

| Symbol | Parameter | Min | Typ | Max | Unit | Notes/Conditions |
|---|---|---|---|---|---|---|
| Tolerance | Output Voltage Tolerance | -5 | | 5 | % | DC+AC+ripple, DC to 1MHz |
| $I_{STDBY}$ | Standby Current | | 1 | | mA | |

# 51.5 AC Adapter Considerations

To support Turbo performance as well as to provide more flexibility on the size and cost of the AC adapter, this section will cover the important aspects of adapter requirements and trade-offs.

## 51.5.1 Power Budgeting for AC Adapter

The adapter power rating is divided into the sustained power level and transient power level. The sustained power level is the maximum constant power that the adapter can supply to system. The transient power level is the maximum peak power that the adapter can supply within a given duration of time, usually in milliseconds.

The adapter power rating has to meet the power demand of system, which can be divided in to SoC power and rest-of-platform (ROP) power. For the system with Turbo, the sustained SoC power is PL2 and the peak SoC power is PL4.

Default and Extreme Power Limits (PL2, PL4) are now provided in the Coffee Lake H Platform Power Map Design Guide.

The ROP power is determined by the components other than SoC. The number of USB ports, the display module, the memory module, etc., significantly impact on the ROP power level. As described in the $P_{SYS}$ Section 51.7, the $P_{SYS}$ feature can monitor the ROP power in real-time. If $P_{SYS}$ is not available, the designer has to estimate the typical ROP power level ($P_{ROP_typ}$) and the worst case maximum ROP power level ($P_{ROP_MAX}$) in order to size the adapter.

## 51.5.2 Transient Power Requirement for Turbo

The selection of charger PD architecture is going to affect the transient power requirements on the AC adapter in order to adequately support Turbo operation. The duration of transient power level depends on how long the battery takes to start providing power.

## 51.5.3 Sustained Power Requirement at Dead Battery Level

For the system with either Hybrid Power Boost (HPB) or NVDC charger, the sustained power requirement of the adapter can be estimated based on the scenario of a dead battery when the battery doesn't have enough charge to power the system and the AC adapter has to provide all the power. Intel recommends the Dynamic Battery Power Technology (DBPT) to better determine the battery power capability in real-time. See Section 51.8 on battery and fuel gauge system for details.

$P_{SYS}$, the platform power monitoring and control feature on Coffee Lake can be used to maintain a desired $P_{SYS}PL2$ level where the overly conservative estimation of ROP power can be reduced. Instead of using the worst case maximum ROP power level to estimate the sustained power level for AC adapter, the pre-defined $P_{SYS}PL2$ can be used.

**Table 51-16. Sustained and Transient Power Levels with different PD Architectures**

| Charger Type | Adapter Supplemented by Battery | Sustained Power Level with Dead Battery | Transient Power Level | Transient Power Level with Dead Battery Level |
|---|---|---|---|---|
| Traditional | No | Without $P_{SYS}$: PL2 + $P_{ROP_MAX}$<br>With $P_{SYS}$: $P_{SYS}PL2$ | Up to 10ms: PL4+$P_{ROP_MAX}$ | Up to 10ms: PL4+$P_{ROP_MAX}$ |
| Hybrid Power Boost (HPB) | Yes | | Up to 1.5ms: PL4+$P_{ROP_MAX}$ | |
| NVDC | Yes | | Same as sustained power level | |

***Note:*** The above power loading levels have to be divided by the conversion efficiency to get the final adapter output power levels. The $P_{SYS}PL$ and PL values need to be updated regularly as the power capability of adapter and battery changes. In "CFL Turbo and Thermal Power Management Guide for Core™ based Processors", the flow chart and equations are provided to calculate $P_{SYS}PL$ and PL values based on adapter power capability and battery power capability (DBPT) for 4 design options; NVDC with $P_{SYS}$, NVDC without $P_{SYS}$, HPB with $P_{SYS}$, and HPB without $P_{SYS}$.

## 51.5.4 Psys and Other Considerations for Using Smaller AC Adapter

There are some cases where a smaller adapter with lower sustained power level can be used for better portability or lower adapter cost. However, there will be impacts on the dead battery operation, Turbo performance, and charging time.

If an AC adapter with sustained power level less than PL2 + $P_{ROP_MAX}$, it is recommended to have $P_{SYS}PL2$ enabled and set $P_{SYS}PL2$ to the sustained power rating of AC adapter. However, there could be performance impact if the sustained power of adapter is much less than the PL2 + $P_{ROP_MAX}$ and user loaded the ROP power close to the worst case maximum. Here is an example.

For example, in a system with PL2 of 25W, PL4 of 46W, $P_{ROP_MAX}$ of 15W, and conversion efficiency of 90%, the sustained power level of adapter can be calculated with the following equation. An adapter with a sustained power rating of 45W is recommended for this system.

$$P_{sustained}=(PL2+P_{ROP_MAX})/Efficiency$$

However, if a smaller adapter with 30W sustained power rating is used with this system, without $P_{SYS}$, the PL2 will have to be reduced down to 12W, which is even less than PL1 of 15W. In this scenario, both PL2 and PL1 have to be reduced to 12W when the battery is dead. If the system has a traditional charger, the PL2 and PL1 have to be reduced to 12W no matter if the battery is dead or not as long as the adapter is connected.

On the other hand, if the system has $P_{SYS}$ enabled, the performance will be managed to keep the $P_{SYS}PL2$ at 30W. If the rest of platform power is lowered to 10W, the SoC will have 17W of power budget and the performance should be better than the case without $P_{SYS}$.

With a smaller adapter, the charging time from 0% to 80% state of charge will likely be impacted. However, the actual charging time impacts depends on many other factors besides the sustained power rating of adapter, such as the power state of system, battery size, constant current charging rate. As the sustained power rating is reduced, the power available for charging is going to be reduced first.

### 51.5.5 Protection Mechanisms

The electrical protection mechanisms cover the following two scenarios: the magnitude of system peak power exceeds the adapter transient power limit, and the duration of system peak power event exceeds the duration of adapter transient capability.

In the event when system peak power might exceed the adapter transient power limit, the over-current-protection (OCP) is designed to sense the adapter current and trigger PROCHOT# if the over-current condition is met. For the discrete implementation, refer to "Battery Voltage Droop & Brick Over Current Protection Circuit Design" doc# 509511. There are chargers with integrated PROCHOT# circuit available as well.

However, after PROCHOT# is triggered, the SoC frequency is going to be reduced to the minimum causing significant performance loss. So instead of hitting PROCHOT#, the system EC may reduce PL4 as a preemptive measure if an under-sized adapter is connected.

## 51.6 Battery Charging System

This section reviews battery charger topologies used in mobile system designs.

During CPU Turbo Boost periods, the system may overload the input power source. The battery charge controller shall be capable of operating in hybrid power mode where the battery discharges to supplement the DC input power. There are two types of charger topologies capable of doing this:

1. Hybrid Power Boost (HPB) battery charger
2. Narrow VDC (NVDC) battery charger

### 51.6.1 Hybrid Power Boost (HPB) Battery Charger

In the Hybrid Power Boost configuration, the synchronous buck converter runs as a normal buck converter when the adapter provides power to the system and is charging the battery. When the adapter power is not sufficient, the synchronous buck converter runs in reverse to boost the battery voltage to around 20V. Thus the battery supplements the adapter whenever the adapter power is not sufficient. This requires no circuit changes from a traditional adapter. The change is required in the control circuit (the Battery charger controller).

The advantage of this system over a traditional charger is that the battery is able to assist the adapter during turbo workloads. This system has the disadvantage that the light load efficiency is pretty low as it is difficult to achieve high light load efficiency at high input voltage.

**Figure 51-4. Hybrid Power Boost (HPB) Battery Charger**

## 51.6.2 Narrow VDC (NVDC) Battery Charger

**Figure 51-5. Narrow VDC (NVDC) Battery Charger**

Figure above shows the Narrow VDC (NVDC) topology. Here, the system bus ($V_{SYS}$) is not connected directly to the adapter. It is connected to the output of the buck converter. Hence, NVDC operates only as a buck converter, both when NVDC charges the battery and when the battery supplements the adapter and provides power to the system. NVDC implementation reduces the switch-over period between the charging

mode and the hybrid power mode. NVDC implementation allows the system to minimize the period of overloading the input power source when CPU is in Turbo Boost mode.

The advantage of using the NVDC system is that the overall system efficiency is better compared to the Hybrid Power Boost charger. The system can be designed for a smaller voltage rating since the system has a lower Vin. The disadvantage is that the charger components' size and power dissipation increases.

## 51.6.3 Benefits and Trade-Offs

**Table 51-17. Benefits and Trade-offs of the Different Chargers**

| PD Architecture | Turbo support | Advantages | Limits |
|---|---|---|---|
| Traditional charger | No. Rely on adapter or battery | More common for system with less dynamic load. | VRs with large range of input voltage are less efficient at light load.<br>Adapter has to be sized to supply peak system power for 10ms. |
| Hybrid power boost | Yes | Higher input voltage is more suitable to larger system with large power consumption. | VRs with large range of input voltage are less efficient at light load.<br>Adapter has to supply peak system power for 1ms. |
| NVDC with 2S battery | Yes | Design optimized with Lower input voltage has better light load efficiency. | Charger's components (FET/ Inductor) size increase (small for Ultrabook™)<br>Additional power dissipation localized to charger area |
| | | FETs can be optimized for lower input voltage and VRs can be smaller and faster. | |

Section 51.7 describes $P_{SYS}$, the protection mechanism for the input power sources.

## 51.6.4 Chargers Supporting 5V-20V USB Charging

USB Power Delivery usage models suggest the following operating modes on the USB charging port:

1. System battery providing power to USB ports (5V, up to 3A OUT)
2. 5V USB adapter providing power to the system(5V, up to 3A IN)
3. USB PD Charger to provide power to the system and battery (9V, 15V, 20V up to 3A or 5A IN)

In order to support all of these charging modes, the Buck Boost charger provides a simple, cost effective and space saving solution.

## Figure 51-6. Detailed View of USB-PD Subsystem

## Figure 51-7. Modes of Operation

| | OPERATION | | | | | | |
|---|---|---|---|---|---|---|---|
| | Mode | Power Flow | Topology | Q1 | Q2 | Q3 | Q4 |
| 1 | **Battery Powering USB** (e.g. mouse, KB, HD, charging phone/tablet; Vbatt>Vusb) | Batt→USB | Buck CV | Control FET | Sync Diode | ON | OFF |
| 2 | **Generic USB Charging Battery** (Vusb<Vbatt, i.e. Vusb=5V) | Batt←USB | Boost CC/CV | Sync Diode | Control FET | ON | OFF |
| 3 | **USB PD Charging Battery + Sourcing System** (Vusb>Vbatt, i.e. Vusb=12V/20V) | Batt←USB | Buck CC/CV | ON | OFF | Control FET | Sync Diode |
| 4 | **Battery Operation w/ No USB** (No adapter or USB plugged in) | None | Short Protection | OFF | OFF | OFF | OFF |

### 51.6.4.1 Features Desired in Buck Boost Charger

1. Adapter voltages to be supported: 3.8V - 20V sustained
2. Battery configurations to supported: 2S - 4S (5.6V - 17.4V)
3. Two level programmable input current limit (sustained and peak)
4. Default input current limit programmable by hardware pin
5. Platform power monitoring ($P_{SYS}$)
6. PROCHOT# - System voltage, Input current, Battery discharge current (and input voltage)
7. Low power mode during battery only Sx/ S0ix mode (consume <1.5mW)
8. SMBus or I2C compatible

For detailed Buck Boost charger requirements, refer to Buck Boost Charger Specification – Power Supply Design Guide RDC#561998

### 51.6.4.2 Design Considerations for 5V VBUS Operation

It is important to consider the following factors when using a buck boost charger on the platform:

1. With a 5V USB input, the inrush current on the system bus should be limited when the charger and system rails are enabled. This is especially important under a dead battery power on scenario.

2. The maximum resistance from the USB VBUS to the input of the charger should be <50-60mΩ in order to operate at 5V.

3. Dead battery power on sequence with a port controller needs to take into account a way to power on the TCPM/ EC and meeting the pSnkStdby requirement. If the TCPM is powered using the V3.3A rail, care should be taken to ensure that inrush current does not exceed the default current limit set on the charger.

## 51.7 Platform Power Monitoring And Control ($P_{SYS}$)

For thermal control, previous platforms had the ability to throttle the processor speed to reduce SoC power consumption and keep the average power dissipation of the SoC package within defined limits. Coffee Lake Platform has added the ability to monitor and control the average power the platform is consuming and throttle the SoC to keep the overall platform power dissipation within defined limits. The new platform power level limits are useful to keep the average power of the platform within the power ratings of input power sources, voltage regulators and batteries. The feature of measuring total platform system power is termed $P_{SYS}$ or System Input Power Monitor.

### 51.7.1 Benefits

The $P_{SYS}$ function provides a measure of the instantaneous power consumption of the entire platform. The PCode in the SoC uses the measured platform power to adjust SoC performance to keep the average platform power within desired limits. The measured platform power is also available to the Embedded Controller (EC) via the PECI interface and to software and firmware applications via MSR registers. Some systems may also have the EC sample the analog $P_{SYS}$ signal after the resistor to avoid latency. The following is a list of benefits and features available with the SoC varying performance to keep the average platform power within limits and the ability of other software agents to read the platform power:

1. Real time monitoring of the platform power enhances the ability to support turbo mode when the platform is being powered by the battery only.
2. The average power of the platform can be kept within the average power rating of the input power source even if peak platform power temporarily exceeds the rated power of the input power source. This allows smaller wattage input power sources (battery and AC adapter) to power a platform that has high peak power requirements by keeping the average power demand within limits of the input power sources.
3. The platform power demand can also be adjusted to keep the average platform power and thus the average platform temperature under desired levels.
4. Previous thermal solutions measured the power to the SoC and used an estimate of the power the rest of the platform (ROP) was consuming to determine power budgets. Some potential performance gains are not realized in the cases where the actual ROP power consumption is less than the estimate. For these circumstances,

using the actual platform power consumption ($P_{SYS}$) will provide an increase in turbo performance.

5. The platform instantaneous power consumption can be monitored by firmware and software to provide applications that provide power monitoring and feedback to the user.

## 51.7.2 Theory Of Operation

The $P_{SYS}$ feature function parallels the package level power monitoring features. Registers hold defined power limits for the platform. The new power limits are defined as $P_{SYS}PL1$, Tau, $P_{SYS}PL2$ and $P_{SYS}PL3$. Figure below shows the relationship between the different power levels.

**Figure 51-8. Relationship Between Platform Power Levels**

The $P_{SYS}PL1$ level is the long term sustainable power limit of the platform. This can be the rated power of the adapter, the discharge rate of a battery, the power capability of the platform or a combination of all of these. $P_{SYS}PL1$ has a time constant (Tau) associated with it. $P_{SYS}PL2$ is a power level that the platform is allowed to have for a temporary time. For example, a battery can be discharged at a higher rate for a short period of time as long as the average discharge is equal to $P_{SYS}PL1$. Shorter period but higher power limits can also be supported up to the $P_{SYS}PL3$ level, for example, discharging the battery at 4C for less than 10ms and a 9% duty cycle. The SoC will adjust power consumption to drive the average power consumption to the $P_{SYS}PL1$ level over a long period of time which is greater than Tau.

## 51.7.3 Hardware Ingredients

The $P_{SYS}$ feature requires some hardware components for implementation in order for the platform to measure the power it is consuming. Figure 51-9 and Figure 51-10 show typical implementations of the $P_{SYS}$ feature. The platform must be able to monitor the

power going to the platform. In a battery powered device, the power going to the system is the power coming from the input adapter, plus any power the battery is providing. Using a battery charger with a power monitoring function makes the most sense since the battery charger monitors both of these pieces of information already. Several battery chargers with a power monitoring feature have been enabled to support $P_{SYS}$ on Coffee Lake platforms.

**Figure 51-9. HPB Battery Charger with $P_{SYS}$ Implementation**

**Figure 51-10.NVDC Battery Charger with $P_{SYS}$ Implementation**

The battery charger provides a current output that is proportional to the power being delivered to the platform (from the brick, battery or both). A shunt resistor is used to convert this current output to a voltage output and to scale the voltage to the full scale input voltage range of an analog to digital converter. The platform uses the SVID interface to read the power data. The measured platform power is provided in SVID register 0Dh, location 1Bh. An 8 bit A/D converter in the IMVP8 controller is used to convert the power monitoring information. The processor then reads the power measurements via SVID from SVID address 0Dh, location 1Bh. See the 'Serial VID (SVID) Protocol' specification and the 'IMPV8 PWM VR' specification for specifics on the IMVP8 and SVID.

The PROCHOT# signal shown in Figure 51-9 is a signal that indicates to the CPU that a platform event has occurred that requires the immediate power reduction by the processor. The PROCHOT# signal provides a faster mechanism for power reduction than $P_{SYS}$ and is used to protect the input sources against instantaneous power events rather than the average power.

PROCHOT# can be triggered by multiple sources in the platform. PROCHOT# typically is asserted by the battery charger under the following conditions:

1. The amount of adapter current exceeds an upper threshold.
2. The amount of battery discharge current exceeds an upper threshold.
3. The battery voltage falls below a lower threshold.

If the PROCHOT# levels are programmable then the levels should be set to protect the input source. For example, the PROCHOT# for the adapter current level should be programmed to at the current the adapter can provide without damage such as a fuse blowing.

If $P_{SYS}$ is used to protect the input power source then specific information about the input power source must be relayed to the platform. The platform must know the power capability of the input power source which can be a wall adapter, wireless system charger, battery, USB-PD port, USB-BC port or any other of a variety of sources. Typically, the input power source capability will be determined by the EC on the platform.

### 51.7.4 Software/Firmware Ingredients

The new PSYS Monitoring and Control Parameters are:

**$P_{SYS}$** is the value provided to the processor PCU from the platform through SVID quantifying the total platform power load. This value shares the name of the feature.

**$P_{SYS}P_{MAX}$** is the maximum power the platform is capable of drawing. It is the sum of PL4 plus the Rest of Platform power.

**$P_{SYS}$PL1** is the targeted total platform power level to which the PCU's platform power monitoring and control will manage over time. The value is provided by the system.

**$P_{SYS}$PL2** is the highest power level to which $P_{SYS}$ will be allowed to go on a temporary basis while there is budget to do so (analogous to RAPL's PL2). The value is provided by the system.

**Tau** is the time window which roughly characterizes the time scale under which $P_{SYS}$ monitoring and control manage to the target $P_{SYS}$PL1 value. The value is provided by the system.

**$P_{SYS}$PL3** is the same limit value/feature as the legacy PL3. $P_{SYS}$PL3 triggers control such that $P_{SYS}$ power level events exceeding it are limited to a small duty-cycle percent on time; e.g., 10%; notwithstanding power spiking events caused by another component on the platform. No change in function. $P_{SYS}$PL3 limit value uses the platform level power ($P_{SYS}$) as a basis for decisions instead of package power.

The MSR registers and bit definitions pertinent to $P_{SYS}$ functionality can be found in the Coffee Lake BIOS Guide (Refer to table below).

**Table 51-18. Access Availability of the Various $P_{SYS}$ Configuration Parameters**

| Parameter | Description | Access (Addresses Defined in HAS) | | | |
|---|---|---|---|---|---|
| Name | | MSR | MMIO | PECI | BIOSMB |
| $P_{SYS}PL1$ | Platform average power target | RW | N | RW | N/A |
| $P_{SYS}PL2$ | Turbo/Momentary average platform power target | RW | N | RW | N/A |
| $P_{SYS}PL3$ | Duty cycle controlled average platform power target | RW | N | RW | N/A |
| $P_{SYS}Tau$ | PL1/PL2 Time Scale | RW | N | RW | N/A |
| Enable | PC Monitor/Control On/Off | RW | N | RW | N/A |
| $P_{SYS}Value$ | Actual value of $P_{SYS}$ | RO | N | RO | N/A |

**Figure 51-11. Information Sources and Flow Diagram**

## 51.7.5 Configuration

The $P_{SYS}$ feature can co-exist with other thermal and power management features found on the platform.

At power on, BIOS must initialize the $P_{SYS}$ power limit registers ($P_{SYS}_P_{MAX}$ and $P_{SYS}PLx$) to reflect the basic configuration of the platform. During run-time, the EC or other software/firmware agents can update the $P_{SYS}PLx$ values as platform conditions change such as a new input power source being plugged in.

## 51.7.6 Implementation of $P_{SYS}$

$P_{SYS}$ is enabled by:

1. Clearing bits: **[30]** SVID Presence, and **[31]** Platform IMON ($P_{SYS}$) Disable. Clear these at Flash Address FCPUSBA + 004h (default Flash Address 304h). Refer to the SPI Programming Guide.
2. Enable $P_{SYS}$ functionality in your charger. Usually done through your EC.
3. Program the $P_{SYS}_P_{MAX}$ value to PL4+$ROP_{MAX}$ (Rest Of Platform) power. Refer to the BIOS Specification.
4. Select a value for $R_{PSYS}$ as shown in Section 51.7.6.1.

The $P_{SYS_}P_{MAX}$ value is the scale that the processor uses to interpret the $P_{SYS}$ values read from the IMVP8 controller. There is no specific $P_{SYS_}P_{MAX}$ which is correct.

1. Use a $P_{SYS_}P_{MAX}$ value that is large enough to cover the most power the platform could possibly draw.
2. Use a $P_{SYS_}P_{MAX}$ value which is small enough to provide the granularity appropriate for the platform.

### 51.7.6.1 Determining the value of $R_{PSYS}$

$R_{PSYS}$ is sized to develop the $P_{SYS}$ current from the charger so the voltage input to the IMVP8 ADC will reflect the value of $P_{SYS_}P_{MAX}$ as FFh.

$R_{PSYS}$ should be placed near the IMVP controller.

Figure 51-9, here are some examples where:

**$P_{SYS_}P_{MAX}$** = the max power for a platform, PL4 + $ROP_{MAX}$. Programmed as above.

**ADC $V_{REF}$** = the full-scale voltage on the IMVP8 $P_{SYS}$ pin. An ADC converts this voltage level to FFh. Different for each IMVP8 controller.

**$I_{PSYS}$** = the µAmps/Watt of the $P_{SYS}$ signal from the charger. A typical value is 1µA/W, but your charger may vary.

The formula for determining the value of $R_{PSYS}$ is:

$$R_{PSYS} = ADC\ V_{REF} / (I_{PSYS} * P_{SYS_}P_{MAX})$$

**Table 51-19. $R_{PSYS}$ Examples**

| $P_{SYS_}P_{MAX}$ | $I_{PSYS}$ | ADC $V_{REF}$ | $R_{PSYS}$ |
|---|---|---|---|
| 35W | 1 µA/W | 1.2V | 34.3KΩ |
| 95W | 2 µA/W | 3.3V | 17.4KΩ |
| 175W | 1 µA/W | 1.6V | 9.1KΩ |

## 51.8 Battery and Fuel Gauging System

This section suggests system architecture for the U-Line battery and fuel gauging systems. Section 51.8.1 on Dynamic Battery Power Technology provides information on how Turbo can be performed during discharge, given a two series Li pack configuration, providing for maximum performance.

We have adopted a cost / functionality strategy for the U-line. We see the market being divided into three segments (shown below) which can be identified by differences in their battery and fuel gauging system.

1. Volume Segment: Battery and fuel gauging system designed to meet nominal battery runtime at nominal cost targets. Fuel gauging system provides nominal accuracy. Approaching full SoC performance.

2. Premium Segment: Battery and fuel gauging system designed to meet maximum battery life. Fuel gauging system provides best accuracy, and supports Dynamic Battery Power Technology. Full SoC performance

3. Value Segment: Reduced battery life to meet cost target. Fuel gauging system may sacrifice accuracy to save cost. Nominal SoC performance.

## 51.8.1 Dynamic Battery Power Technology

Figure below shows the top level architecture of Intel DBPT version 2 (Dynamic Battery Power Technology). The input voltage of system regulator, $V_{input}$, is lower than the open circuit voltage of battery cells, $V_{batt}$. The voltage drop depends on the load current, $I_{input}$, and the total parasitic resistance from cells to regulator, $R_{batt}$ and $R_{sys}$.

**Figure 51-12.DBPT Top Level Block Diagram**

Where $R_{batt}$ includes both cell resistance and parasitic resistance due to the cell interconnect, sense resistor, FET, fuse, connector of battery pack. $R_{sys}$ includes the resistance of power/ground metal, sense resistor, FET, and other parasitic resistance on the system main board.

In order to prevent $V_{input}$ from violating the required minimum system input voltage, $V_{min}$, $I_{input}$ has to be adjusted according to the level of $V_{batt}$ as the battery is discharged, as the impedance of the battery changes with state of charge, temperature, and age.

DBPT adds commands to the SMBus command set, so that the fuel gauge reports the maximum power the pack can support for a Turbo pulse. The pack takes into account, $R_{sys}$, $R_{batt}$, and $V_{min}$ when reporting what maximum power the pack can support. The system is then able to implement an algorithm so that the combination of SoC and other power sources stay within this allowed power envelope, so that an under-voltage condition does not occur.

There are two versions of DBPT. The first version defines an SMBus command MaxPeakPower() that reports the ability of a battery pack to deliver power for up to 10ms. This is useful for setting the maximum PL4 value for the SoC, while making sure the battery voltage droop, combined with losses between the cells and voltage regulator are allowed for. DBPT version 2 implements all the features of DBPT, and adds

the additional SMBus command SusPeakPower() which reports the ability of a battery pack to deliver power for up to 10s. This is useful for setting the maximum PL2 value for the SoC, while again allowing for voltage droop and power loss between the battery and voltage regulator.

For further information on DBPT, refer to the following documents:

- Intel Dynamic Battery Power Technology v2, SMBus Implementation Specification RDC#498853
- Intel Dynamic Battery Power Technology (Intel DBPT and DBPT v2) Implementation Considerations RDC#564428.

Without DBPT, the pack voltage must be chosen so that under load the pack voltage cannot fall below Vmin. Ways to achieve this are to choose cell counts of 3 or more series Li cells. An alternative is to allow Turbo events on discharge, only to a predetermined critical threshold based on state of charge of the pack. The issue with this approach is that the impedance of the battery changes based on age and temperature, and the solution involves reducing SoC performance in an overly conservative way. DBPT allows for the SoC to perform optimally, at any given battery impedance.

## 51.8.2 Fuel Gauging

By choosing between the following fuel gauging types, it is possible to tailor the fuel gauging solution cost, by trading off functionality. The following choices of fuel gauging solution are ordered below, starting with the most accurate, highest featured. As the list continues the features are reduced, along with the cost.

### 51.8.2.1 In-Pack SMBus Fuel Gauge with DBPT

This solution for in-pack fuel gauging which supports DBPT provides for greatest runtime by providing the greatest fuel gauging accuracy. This solution also provides the greatest performance, as it allows for Turbo operation over the entire discharge cycle. Solutions which provide support for 2-4 series connected Li based cells are present in the market, from the two premier fuel gauging suppliers.

**Figure 51-13.Block Diagram of In-Pack Fuel Gauge with DBPT**

### 51.8.2.2 In-Pack SMBus Fuel Gauge without DBPT

This solution for in-pack fuel gauging provides for greatest runtime by providing the greatest fuel gauging accuracy. As this solution lacks support for DBPT, this solution is well suited to configurations of 3-4 series connected Li based cells, which support Turbo during discharge. With the higher cell count, typically the dropout concerns that might impact a two series configuration are not present. This solution is also a viable choice for a Li two series system, which will not Turbo during discharge. The block diagram of this system is identical to the In-pack SMBus Fuel Gauge with DBPT, as the only change is a fuel gauge that lacks the DBPT support, typically available at a lower price point.

### 51.8.2.3 In-system Fuel Gauge without DBPT

This solution for In-system fuel gauging provides for adequate fuel gauging accuracy. This solution also foregoes support for DBPT. The solution utilizes the selection of fuel gauging parts aimed at the cost competitive one cell fuel gauging market. As the SoC solutions require 5V rails, this solution uses an Op-Amp to divide the pack voltage of a 2 series Li pack configuration in half, and supply this precision divided voltage to the fuel gauge solution designed to handle one series cell. A typical block diagram of such a system is shown below.

**Figure 51-14. Block Diagram of 1S Fuel Gauge with 2S Pack**

***Note:*** In such a system the Op-Amp and the divider resistors should be chosen to provide a very accurate division ratio, as inaccuracy in this division will directly affect fuel gauging accuracy. This means selection of an Op-Amp with a very low input offset voltage. In addition a matched set of divider resistors, or high precision resistors should be evaluated for their effect upon accuracy. Note that the Op-Amp will not be required to swing to the power or ground rails if powered by a 5V rail, so cost can be saved by choosing a low power, low input offset amplifier, which does not provide rail to rail output swing. The bandwidth of the amplifier is of some concern, but a bandwidth of 200kHz should be adequate to give good results. It is suggested to consult the fuel gauge manufacturer to determine what bandwidth their gauging solution requires.

In Windows* solutions, a reporting of current is required by the operating system, so be sure to choose a single cell gauging solution which reports current for such systems. Other operating systems may not require reporting of current. Single cell gauging solutions which monitor only voltage, can provide a bit lower price point while typically giving up a couple percent of accuracy.

## 51.8.3 Battery Pack Size and Configuration

The battery pack is typically size to meet goals for runtime and peak power. In order to achieve the highest performance for the processor, please specify the battery based on guidelines for power capability of the pack from Table 51-20.

**Table 51-20. Battery Discharge Capability Recommendations**

| Recommended peak duration | 10ms | 100 sec | Constant discharge |
|---|---|---|---|
| Recommended Max Discharging Power Level if $P_{SYS}$ is not used | PL4 + $P_{ROP_MAX}$ | PL2 + $P_{ROP_MAX}$ | PL1 + $P_{ROP_MAX}$ |
| Recommended Max Discharging Power Level if $P_{SYS}$ is used | PL4 + $P_{ROP_MAX}$ | $P_{SYS}$PL2 | $P_{SYS}$PL1 |
| Peak Duration with PL3/$P_{SYS}$PL3 | configurable down to 2ms[1] | NA | NA |
| Duty Cycle with PL3/$P_{SYS}$PL3 | configurable down to 4%[1] | NA | NA |

***Note:***
1. Refer to *CFL Turbo and Thermal Power Management Guide for Core™ based processors* RDC#566828

Once the power capabilities to support a performance level are decided, a choice of pack configuration remains.

The choice is often between two series and three series configurations of Li based cells. Two series configurations result in higher currents, when compared to a three series configuration, for equivalent system power consumption. This would normally tend toward choosing the higher voltage solution, as power losses increase with the square of the current. The other factor is that with a lower voltage range, the DC/DC converter can typically be optimized for a better overall efficiency, which tends to favor the two series solution. Another factor to consider, is that a three series configuration will likely not have issues with reaching low voltages during Turbo events, where a two series configuration may reach low voltages under load, and require support of DBPT to manage this. For the lower power consumption systems in this line, an NVDC charger configured for two series cells seems to achieve the greatest system efficiency. For higher power consumption systems in this line, a three series cell configuration will achieve the greatest system efficiency. The tradeoff between the two approaches can be gauged, by looking at the $I^2R$ losses throughout the power system in the two approaches.

A trade-off that is often overlooked is that of fuel gauging accuracy, and pack cost. If we think of battery pack cost in terms of $/Wh (dollars per watt-hour), then any inaccuracy in the fuel gauge can be expressed as a cost in dollars, for a given pack size. For example, given a 50Wh pack, and a cell cost of $0.40/Wh, the cost of cells would be $20. When choosing between a 6% accurate fuel gauge, and a 1% accurate fuel gauge, it makes sense to look at the cost of that potentially lost capacity, when looking at the price difference between the gauges. With a difference of 5% in accuracy, and a cell cost of $20, the 1% accurate gauge could be $1 more expensive ($20*5% =$1), and still offer better performance. The 6% accurate gauge would need to increase the cell cost by $1 to allow for the potentially decreased runtime due to gauge performance. In addition the more accurate gauge will offer a solution that is smaller and lighter, as the pack capacity that is purchased is fully used, rather than just sized up to allow for fuel gauge inaccuracy.

## 51.9 Dynamic Fast Charging Technology-DFCT

Fast charging is becoming a feature sought out by many customers. There are several challenges to providing fast charging within a system.

First is the potential impact to the size of the AC Adapter needed to provide this fast charge capability. To charge faster requires more power during at least a portion of the charge cycle. If the requirement is to provide faster charging while the system is in a lightly loaded or off state, it may be possible to fast charge without increasing the AC Adapter wattage. If fast charge is required under all power states, then more AC adapter wattage is likely required.

The cells in the battery must be capable of fast charging. There is increased power dissipation in the charger circuitry while fast charging, so either additional thermal handling capability must be present, or the charge rate must be controlled based upon the thermal environment.

There are several vendors that provide algorithms designed to fast charge "standard" cells, while promising to preserve the cycle life. Previously the method used to report and control fast charging was proprietary to each vendor, which made implementation of solutions complex, and limits reuse when moving between vendors.

DFCT addresses many of these concerns. It provides a standardized set of SMBus commands that are used to define the fast charge. The algorithm resides within the battery pack or fuel gauge in the system, as this subsystem has the best understanding of the cells. Allowing for multiple vendors with the same commands stimulates innovation, and allows for moving between different vendors with various algorithms, without needing new code for the embedded controller. DFCT can be used with Dynamic Platform Thermal Framework, DPTF, to provide fast charging in a way that allows control of the thermal issues within the system.

For further information on DFCT, refer to the following documents:

- Intel Dynamic Fast Charging Technology, SMBus Implementation Specification RDC#564466
- Implementing Fast Charging with Intel Dynamic Fast Charging Technology (Intel DFCT) RDC#564842.

# 52 Flexible Instrumented Platform (FIP) Design

Power instrumentation is vital in measuring and analyzing sub-subsystem power to enable full-system power optimization; Power Sequencing and Low speed signal test for system functionality test/verification and debug. Current system instrumentation technique involves connecting sense resistors on the board to the Data Acquisition Device (DAQ) manually for system power optimization and system functionality verification/debug. This method has several pitfalls and carries risks such as tedious manual re-work, quality concerns, and potential board damage. In this paper we introduce a new technique of power instrumentation called the Flexible Instrumentation Platform (FIP) design. The FIP design offers many advantages over existing methods such as one-time effort requiring no manual rework, no risk of shipping damage and shorter setup time.

## 52.1 Background

Sense resistors and Power/Electrical test access are typically not part of the production design. Hence power instrumentation and low speed electrical signal test access technique involve manually connecting sense resistors on the board and using wires connected to a pod on the DAQ for measuring current, voltage and power consumption as well as to use a Scope/Digital multi-meter for low speed signal test.

As depicted in Figure 52-1 and Figure 52-2, existing instrumentation introduces several challenges:

- Manual rework time: instrumentation takes three days best case for the whole board with one dedicated labor. Also this rework has to be done for each board.
- Quality concern: potential lack of quality in soldering can affect power measurement accuracy.
- Potential risk: Board damage caused by rework at limited board and SOC sample stages that may be gating product launch without tuning to extend battery life to meet/exceed target
- Portability Issues: the instrumented platforms connected to pods are sensitive to damage such as wires pulling pads off. This affects ability to move or transport instrumented boards without damage.
- Setup time: connecting individual wires to DAQ takes time and depending on the number of rails/ channels, it can take half a day or more.

Additionally, customers that do take the time to add power instrumentation to their designs do not include consistent accurate labeling to the wires. Also they tend to hot glue the sense resistor location making identification very difficult, sometimes impossible. The FIP implementation proposed here reduces the requirement for power measurement teams to become intimately familiar with the customer design for setup, therefore enabling full focus on software power optimization.

**Figure 52-1. System Instrumentation Block Diagram**

**Figure 52-2. Power Instrumentation Setup**

## 52.2 Overview

This section introduces a new instrumentation design proposal. FIP design minimizes the risk introduced by the current instrumentation techniques by adding extra sense layers on the PCB and routing the instrumented wires to an extended PCB space with a Flexible male DuPont connector. The board can then be connected via a Flexible DuPont cable to the DAQ for power measurements and scope for low speed electrical signal measurements. Figure below shows an overview of the FIP design.

FIP involves adding the following components:

- Four extra PCB layers
- Industry flexible DuPont header connector
- Flexible extended PCB space sense resistors
- FIP trace routing to the edge
- FIP (Via in Pad) sense resistors
- FIP Vias
- Inner layer impedance coupon (be added for power rail <900mA)

Figure 52-4 shows the difference between FIP and non-FIP boards and Figure 52-5 and Figure 52-6 show the layout for top/bottom and inner layers' current sense resistors calibration (for power consumption measurement accuracy) FIP design.

**Figure 52-3. Flexible Instrumentation Overview**

**Figure 52-4. FIP Board versus Non-FIP Board**

**Figure 52-5. Layout for Inner Layout Current Sense Resistors (impedance coupon) Calibration**

**Figure 52-6. Layout for Current Sense Resistors Calibration for Top and Bottom Layers**

## 52.3 FIP Design Details

This solution is FIP a design with detachable layout solution with all test trace layout to connector for connection to the DAQ/ scope including below. Total setup time is approximately less than one day for complete system power measurements and risk of damaging the board via reworks or setup is eliminated.

1. Complete system power rail instrumentation.
2. Low speed electrical signal test access.

### 52.3.1 FIP Details and Steps

The solution design involves a detachable PCB layout and Gerber method. This package involves designing one PCB layout and generating 2 Gerber files for manufacturing 2 PCBs, one as non-FIP, and the other as a FIP design. The non-FIP design will not have any current sense resistors, and can be ~1USD/piece saving. The FIP PCB can be attached/ removed to the board at any design stage without impact to the original board design. There are no additional design costs nor any rework resource costs associated with addition of power instrumentation to the non-FIP designs. We also avoid the risk of damaging boards by manual rework at limited sample stages and risk of not able to fully debug/fine-tune system low power to extend battery life before product launch schedule.

The PCB design for the two different PCB types is given below:

1. Type3 PCB
2. HDI PCB

Both recommend to have VIP (Via in Pad) sense resistors: N Layer stackup vs. N+4 L (bigger board size to hold a connector). If the number of boards needed is within manufacturer's sample quantity, then there is a potential to not incur any additional costs as some manufacturer do not charge for samples.

1. The design steps for the FIP are:
2. Add 4x layer to core of the original design
3. Define the FIP symbol (Connectors, Current Sense Resistors, Impedance Coupon for inner layer)
4. PCB placement
5. Route System Traces and FIP traces
6. Generate FIP Gerber and Non-FIP Gerber

#### 52.3.1.1 STEP 1: Add 4x Layer to Core of Original Design

The PCB stack-up solution is defined by consulting with the project SI and PI engineers. The FIP layers design should have the least impact to the system base design in terms of impedance control, signal ground/ power referencing especially on high speed I/O signals and should avoid cross talk. A PCB stack-up design proposal adding the 4x layer to the original design in Table 52-1 shows a base design example and Table 52-2 shows the SIP proposal for that base design.

**Table 52-1. Base Design Proposal**

| Base Design | | | |
|---|---|---|---|
| Layer | Layer Thickness (in mm) | | Signal |
| | Layer | Insulator | |
| L1 | 1.55 | 2.7 | Signal |
| L2 | 0.6 | 4 | GND |
| L3 | 0.6 | 4 | Signal |
| L4 | 0.6 | 4 | VCC |
| L5 | 0.6 | 4 | Signal (only low speed signals will be routed here)/GND |
| L6 | 0.6 | 4 | Signal |
| L7 | 0.6 | 2.7 | GND |
| L8 | 1.55 | - | Signal |

### Table 52-1. Base Design Proposal

| Base Design | | | |
|---|---|---|---|
| | Total Thickness | 32.1mm | |

### Table 52-2. FIP Design Proposal (with 4x Layer Addition)

| SIP Design | | | |
|---|---|---|---|
| Layer | Layer Thickness (in mm) | | Signal |
| | Layer | Insulator | |
| L1 | 1.55 | 2.7 | Signal |
| L2 | 0.6 | 4 | GND |
| L3 | 0.6 | 4 | Signal |
| L4 | 0.6 | 4 | VCC |
| L5 | 0.6 | 4 | FIP -GND (connect to system ground as defined by the layout rules) |
| L6 | 0.6 | 4 | FIP-S1 |
| L7 | 0.6 | 4 | FIP-S2 |
| L8 | 1 | - | FIP-GND (connect to the system ground as defined by the layout rules) |
| L9 | 0.6 | 4 | Signal (only low speed signals will be routed here) |
| L10 | 0.6 | 4 | Signal |
| L11 | 0.6 | 4 | GND |
| L12 | 1.55 | 2.7 | Signal |
| | Total Thickness | 46.25mm | |



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### 52.3.1.2 STEP 2: Define FIP Symbols

Establish a layout symbol library for the FIP and define the FIP resistor symbol and non-FIP resistor symbol options. Figures below shows the FIP/ non-FIP symbol design.

**Figure 52-7. FIP/non-FIP Symbol Design Examples-1**

**Figure 52-8. FIP/non-FIP Symbol Design Examples-2**

### 52.3.1.3 STEP 3: PCB Placement

Secure the sense resistors with via in the PCB placement stage. Via creates a precise contact point between the wire and the sense resistor. The placement of any via on the FIP board is critical since a variation of via placement from one site to next will result in marginal variations in the total resistance used to measure the IR drop and current. This in turn results in discrepancies in the power measurement data that impacts the power data quality as shown in Figure below. Conclusion is, VIP sense resistors should be used as described in Table 52-1 for library generation. Test vias alternative symbols should be generated for low speed signals for FIP and Non-FIP Gerbers.

**Figure 52-9. Variations in IR Drop due to Via Placement**

### 52.3.1.4 STEP 4: Route System and FIP Traces

Place the FIP resistors with VIP type and FIP Vias at placement stage and secure the space with VIAs (through Vias and/or Blind/Buried Vias), Route and complete the system traces prior routing the FIP traces. Figure below shows the steps.

**Figure 52-10.PCB Placement**

### 52.3.1.5 STEP 5: Generate FIP Gerber and Non-FIP Gerber

After routing the system traces and the FIP traces, the next step is to generate the FIP and non-FIP gerber. In the non-FIP gerber, remove all the FIP layers, FIP vias, FIP connector, F/IP traces, and replace the sense resistor symbol with the alternative symbol for short trace (refer Figure below) and remove the test vias for the non-FIP.

**Figure 52-11.FIP and Non-FIP Gerber/PCB**

## 52.4 DuPont Header Connector

A DuPont header on the flexible PCB layout space is a 2.54mm pitch connector. The pin count is not fixed but is determined by the FIP layout flexibility. If there is adequate layout space, a Flexible connector with clear pin map assignments can be placed on the board, and a Flexible cable can be used for saving time and effort during test setup. Flexible cable will also reduce the cost and will be easier for mass adoption across different engineering teams. Figure 52-12 shows an example of DuPont header connector.

**Figure 52-12.DuPont Header Connector**

## 52.5 General Guidance for the FIP Solution

- Prepare schematics to generate two sets of net lists for layout to allow one PCB design and two sets of Gerber file generation.
- FIP schematics should include FIP attributes such as:
  - Current Sense resistors (using Via-in-Pad types with both vias connecting to the test pins of 2.54mm pitch DuPont Header connector), power logic test pads of 2.54mm pitch DuPont Head connector, and a GND-FIP (with short pairs of pads connecting to platform GND). The non-FIP schematics do not have FIP attributes included.Current sense resistors are defined as FIP resistors.
  - FIP resistor value/size need to consider the max current/wattage of the resistor can handle, and with high accuracy (1% tolerance or better) and recommend sense resistors remain on same layer with power delivery path from source to receiver
  - Define test signal with POS-FIP_PowerNetName for the power input side of sense resistor and Neg-FIP_PowerNetName and connect to FIP connector measurement pins.
  - Add FIP attribute to all the FIP traces.
  - Define all FIP resistors to have “No_Shape_Connect” property on via-inpad.
  - Define power logic signal test traces as FIP and route to the FIP connector defined PINs for Power Logic test.
  - Define the connector that power test points with positive signals on one side and negative signals on the other side.
- The PCB layout guidance are given below:
  - Add 4 extra layers to the center, use PCB copper weight recommendations: 1oz and define FIP layer (GND-Signal-Signal-GND) to be added to the layout placement stage, ensure system signals not falsely referenced to FIP ground. Have your PI/SI review to ensure no SI/PI concerns specifically on the defined stack-up with FIP, do SI/PI simulation as needed (such as if adding a capacitor is needed)

  - Define power logic signal test traces as FIP and route to the FIP connector
  - Define VIAs and Traces for Power Logic test with FIP attributes
  - Define the DuPont headers that power test points with positive signals on one side and negative signals on the other side
  - If there is no board space to hold DuPont header consult with mechanical designer to make two board outlines for FIP and non-FIP support, one for FIP (bigger one that holds DuPont header, while ensuring SMT process is compliant) and one for non-FIP
  - If enlarging board size is a concern to go in chassis at design stage, set V-Cut from the extending edge or separate different PCB design with two sets of Gerber files for two sets of PCB (while impedance control is considered)
  - Implement current sense resistors on both input and output of each VR. If impedance Coupons used in inner layer, used only on rails <900mA (consult with your SI/PI engineer ensure no SIP/PI concerns)
  - All FIP measurements reference to FIP ground (all rails' ground connected together then connect to system ground), so only 2 points of voltages across sense resistors and 2 source signals (if calibration needs to be done) need to be laid out to the FIP connector (pin headers) unless your data acquisition has different requirements
- FIP traces for the power rails should be routed in a differential fashion, and the following rules apply:
  - FIP Voltage sense line layout rule (i.e. 1oz copper weight, if different, please recalculate below accordingly)
  - For power consumption test: routing on 2 inner layers between FIP_GND: Differential pair from VIP FIP sense resistors
  - For both power consumption and logic test: 5mm trace/4mmspace/10mm between pairs min spacing, keep 15mm minimum spacing to other signal traces/vias; for any clock, high speed signals, keep away as far as possible, or recommend 20mm+ space
  - For impedance coupon FIP trace layout, as recommend only <900mA rails to use impedance coupon, use 10mm/4mm (if space allows, enlarge the distance) and 20mm+ space to other signals, if different copper weight is used, trace width should be calculated accordingly
  - NO || routing on adjacent layers (max allowed || routing less than 100mm)—NO routing under INDUCTORS /avoid switching node on Vreg)
  - FIP traces should avoid Hi-Speed Signal Routing areas
  - The FIP_GND reference planes should extend to the FIP Connector area, while other PWR/GND planes (from pre-existing layers) should be relieved at the GND areas so as not to reference the FIP connections
  - Use different net name for FIP ground and connect FIP ground to system ground with 3x Ohm resistors and 3x capacitors (place on 4 different places, such as 4 corners of PCB, and far from power switching source) to avoid other system signal faulty GND referencing as place holders and choose the best location for short
- Ensure the silkscreen indicates the test points with clear power rail and logic names. As well as the source for resistor calibration (refer to Section 52.6, routing suggestions for current sense resistor calibration)

## 52.6 Routing Overview for Current Sense Resistor Calibration

Current sense resistor calibration can help test accuracy. Figures below provide a routing overview. The Sense+/- and Source+/- can be laid out to the test pins of Dupont header connectors

**Figure 52-13.FIP Top/Bottom Side Current Sense Resistor Calibration - Routing Overview**

**Figure 52-14.FIP Inner Layer Impedance Coupon Calibration - Routing Overview**

## 52.7 General PCB Via/Trace Calculator Routing Guidelines

- http://circuitcalculator.com/wordpress/2006/03/12/pcb-via-calculator/
- http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator/
- Other tools preferred by the ODMs/ OEMs

## 52.8 Summary

The FIP board could save up-to 3-7 days of effort when compared to manual instrumentation and setup for one test. The FIP layout solution will have minimum impact to layout engineers if it is planned at the beginning of the layout component placing and routing. One-layout-2-Gerber file method supports flexible FIP/Non-FIP PCB manufacturing and SMT assembly. It also saves cost and effort for Non-FIP as no extra layout effort or current sense resistors costs are needed at any product design stage.

# 53 Designing for Power Optimized S0ix Platforms (Connected Standby/Modern Standby)

## 53.1 Overview

Intel® S0 idle low power mode (S0ix) IA hardware features and Microsoft® Modern Standby operating system software features (MS, previously known as 'Connected Standby' or CS) work together as key power optimization capabilities that enable power efficient SoC platform designs.

The power efficient platform ecosystem (hardware, software, firmware) that integrates hardware S0ix and operating system Modern Standby power efficient architectures require that all independent hardware design features (SoC, PCIe, USB, SATA, GPIO, clocks, clock control, power delivery and control, PMIC, EC, VR, FETs, glue logic, level-shifters, repeaters, signal routing and termination, etc.) to be integrated accurately, completely and functionally robust according to all individual platform feature specifications listed in the Product Design Guide (PDG), External Design Specification (EDS), Firmware Architecture Specification/BIOS Writer's Guide (FAS/BWG respectively), Runtime D3 (RTD3) Guidelines, Device Power Recommendations Guide as well as industry specification requirements.

**This is a critical design step to enabling S0 idle low power mode:** BOM devices and software stack must support RTD3 requirements fully to enable the SoC power management architecture to enter the most power efficient states. Displays must support power efficient "Active" display states such as Panel Self-Refresh, or PSR to enable deep SoC core and package C-States. Devices and software stacks that do not have "clocks off" or "offloading" capability in addition to power efficient functionality will block SoC power efficient states and result with increased SoC and platform power consumption.

Any one or more features, components or devices that do <u>not</u> meet individual functional design specifications including device sleep and individual component or device power efficiency requirements block SoC, platform and OS deep sleep and have a negative impact on power and performance.

BOM and platform design choices also have a platform power efficiency where regulatory requirements are concerned including new California Energy Commission (CEC) regulatory requirements that are expected to impact all products manufactured on and after January 1, 2019. More information about new CEC regulatory requirement are available in the Coffee Lake Desktop / AIO S0 idle (S0ix) Design Recommendations Technical White Paper (RDC#571210). Regulatory resources outside the scope of this design reference must also be considered based on country and international regulatory requirements for products used in those specific regions.

S0ix power efficient design specification references are distributed throughout individual SoC Platform Design Guide (PDG) chapters and other hardware and software design guidance discussed above, therefore additional guidance will not be listed in this chapter to avoid duplication and associated synchronization issues. Refer to the specific

SoC PDG, EDS, RVP, industry feature specifications (PCIe, USB, SATA, etc.) and the key design references listed in the table below for the most up-to-date design specification and guidance to design for a power optimized S0ix SoC and platform ecosystem.

Additionally, S0 idle low power mode (S0ix) hardware designs require stable, fully functional legacy Sx design capabilities since BIOS FADT table can be disabled on S0ix platforms making the system default to an Sx only design. Sx flows must be fully functional and stable to support the additional power efficient capabilities available from RTD3 and S0ix platform design ecosystems.

In summary, final design power and performance capability is determined by board design, OS, drivers, power policies, BOM device and component capabilities choices. SoC and software stack can't workaround device and component lack of capability with the only resolution is to remove or replace devices and components that reduce or block low power efficiency. S0ix designs that integrate RTD3 capabilities continue to require support for Sx (S0, S3, S4, S5) design capabilities since legacy power sequence flows provide the design baseline for platform sleep states--even though S3 support and S0ix support are mutually exclusive capabilities: Either S3 is enabled and S0 idle low power mode (S0ix) is disabled, or S3 is disabled and S0ix is enabled.

### 53.1.1 S0 Idle (S0ix) SoC Design References

The low power S0 idle (S0ix) / Modern Standby ecosystem must consider many external design considerations beyond this hardware product design guide (PDG) since SoC connected devices, drivers, operating system, application software and firmware play significant roles to enable S0ix. The information will not be consolidated here to avoid duplication, missing detailed design requirements listed in the complete reference and to avoid out-of-sync confusion.

Refer to individual PDG feature sections and implement to specification. Designs must continue to meet Intel® Architecture (IA) platform design Sx requirements (Sleep States: S0, S3, S4, S5) since Sx functionality continues to provide the design capability base and power delivery flow controls for S0ix designs. Platform design choices are key factors that determine the final platform design capability that enable the design to meet power efficiency and regulatory targets.

For Coffee Lake, Microsoft* Windows 10 will be the only Windows client OS supported. As such, refer to Microsoft* Windows 10 MSDN for OS specific design recommendations that impact power management and power optimized performance.

California Energy Commission (CEC) has updated California regulatory requirements that intercept Coffee Lake product production time frame. Although the "Coffee Lake Desktop / AIO S0 idle (S0ix) Design Recommendations" White Paper (RDC#571210) is intended for CFL desktops and AIO designs, mobile hardware designers need to be aware of CEC regulatory impacts to overall CFL design implementation. Access the white paper and refer to section 4, entitled "2019 California Energy Commission (CEC) Computers impact" for details and direct references to CEC resources.

The following Key Design References for Power Optimization Designs below in the table are a partial list and is provided as a convenience. Work with your Intel Field AE and known power and performance AE team members and refine Intel collateral RDC, Validation Internet Portal (VIP), industry standards organizations, operating system manufacture, endpoint device and component vendors for product specific feature design recommendation and requirements.

***Note:*** SoC signal "SLP_S0_B" (SLP_S0#) replaces the power control capability for S3 since S3 and S0ix (SLP_S0_B) power control are mutually exclusive. However, S3 must continue to be routed since software is capable to disable low power S0 idle (SLP_S0_B). This user setting is set at boot. Sx signals and states all continue to be required for S0ix platform designs. Refer to this product's S0ix reference design (SDS or RVP) for guidance. Confirm that all SLP_* signals are routed according to PDG recommendations. Plan platform power maps for sufficient isolated device FET power control according to PDG and reference design recommendations and specific target design requirements.

### Table 53-1. [1]Key Design References for Power Optimized Designs

| Reference title | Reference Type: HW, SW, FW, etc. | Reference location, ID |
|---|---|---|
| System Energy Calculator for California Energy Commission (CEC) - Computer Regulation | Interactive CEC Calculator to confirm design decision feature impact on CEC Expandability Score (ES) | RDC#571644* |
| Cannon Lake Rest-of-Platform (ROP) Power Management Integrated Circuit (PMIC) for Premium Segment with Volume Segment Information (CFL leverages CNL SoC architecture) | Requirements Specification | RDC#560460* |
| Coffee Lake Runtime D3 Hardware and Software Recommendations | Design Guide | RDC#569310* |
| 2017 Coffee Lake Platform Device Power Targets and Related Recommendations | Device Power Specification | RDC#571086* |
| 2017 Coffee Lake Platform Firmware Architecture Specification | Firmware Architecture Specification (FAS) | RDC#570050* |
| Coffee Lake H DDR4 RVP Schematic<br><br>Coffee Lake S CRB Schematic<br><br>Coffee Lake S SODIMM RVP Schematic | Schematic, Board, Symbol references | RDC#571483*<br><br>RDC#572913*<br><br>RDC#573546* |
| Coffee Lake Desktop / AIO S0 idle (S0ix) Design Recommendations | S0ix design recommendations; California Energy Commission (CEC) regulatory resources | RDC#571210* |
| Battery Life: Debugging Power Problems with Standby | External to Intel - Microsoft Channel9 MSDN | https://channel9.msdn.com/Events/WinHEC/2015/OWD200 * |
| Modern Standby Design Decisions | External to Intel - Microsoft MSDN | MSDN page ID: "modern-standby-design-decisions" * |
| Modern Standby Power/ Performance targets | External to Intel - Microsoft MSDN | MSDN page ID: "power-performance-targets" * |
| Modern Standby Tools available | External to Intel - Microsoft MSDN | MSDN page ID: "using-windows-performance-analyzer-to-analyze-modern-standby-issues" * |
| Powerhouse Mountain (PHM) - Intel Hardware Power optimization tool (available only with NDA) | Intel Software Tool: Power Optimization and Enabling | Validation Internet Portal (VIP): Product Documentation and Other software->Access Test software files. Accept terms of use. Search for "Mountain" then download and install the latest version. A PHM video walk-through may also be available in a separate VIP download. |

***Notes:***

1. References and links confirmed as working on 5/25/2018

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# 54 Compatibility with Other Platforms

## 54.1 Compatibility with Legacy Platforms

Coffee Lake H Processor is not forward or backward compatible with Kaby Lake H or Sky Lake H Processors.

There is a compatibility option between Coffee Lake H processor sku i.e., It is possible to mount CFL H 82 45W processor on CFL H 62 45W board and to mount CFL H 62 45W processor on CFL H 82 board. In order to implement this correctly the BIOS should be configured to the right processor capability. Refer to “CFL-H boards compatible and BIOS configuration Technical Advisory RDC#599797”, “BIOS Writer Guide Rev 3.1.0 RDC#550049”.

And also, it is possible to mount CFL H 82 45W processor on CFL H 62 65W RVP Board with minor reworks on RVP - Refer to “CFL H RVP User Guide RDC#572461”. Please note that the proper BIOS configuration is required.

CNP PCH-H is not forward or backward compatible with KBP PCH-H or SPT PCH-H.

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