



# Tiger Lake UP3 UP4 H35 UP3 Refresh Platform

**Design Guide**

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## Revision History

Document Number	Revision Number	Revision Description	Release Date								
607872	0.5	Initial Release	December 2018								
607872	0.7	<p><i>Note:</i> In this revision, this document contains only related information. For Stack up, Tline, Topology Guidelines for all interfaces and Power Integrity, refer 607872_TGL_UY_PDG_Rev0p7.xlsx.</p> <p><b>Introduction on page 29</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Table 1</a> on page 29</li> <li>— <a href="#">Table 2</a> on page 31</li> <li>— <a href="#">Table 3</a> on page 32</li> </ul> </li> <p><b>PCB Stackup and Design Considerations on page 34</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Figure 5</a> on page 35</li> </ul> </li> <p><b>System Memory Interface Design Guidelines on page 64</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Table 12</a> on page 69</li> <li>— <a href="#">Table 13</a> on page 70</li> <li>— <a href="#">Table 14</a> on page 71</li> <li>— <a href="#">Table 15</a> on page 72</li> </ul> </li> <p><b>PCH IOs on page 121</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">RTC Component Selection Guidelines</a> on page 127</li> <li>— <a href="#">Figure 63</a> on page 126</li> <li>— <a href="#">Table 65</a> on page 124</li> <li>— <a href="#">Table 86</a> on page 159</li> <li>— <a href="#">Figure 64</a> on page 129</li> <li>— <a href="#">Figure 63</a> on page 126</li> <li>— <a href="#">Figure 84</a> on page 167</li> </ul> </li> <p><b>Power Delivery on page 376</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— Notes 46, 47 and modified tPCH01 description only in <a href="#">Table 231</a> on page 449</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— Note 7 in <a href="#">Figure 248</a> on page 442</li> </ul> </li> </ul> </ul></ul></ul></ul>	April 2019								
607872	0.9	<p><b>Replaced the below in the entire document</b></p> <table border="1"> <tr> <td>USB 3.1 Gen1</td> <td>USB 3.2 Gen 1x1 (5 Gb/s)</td> </tr> <tr> <td>USB 3.1 Gen2</td> <td>USB 3.2 Gen 2x1 (10 Gb/s)</td> </tr> <tr> <td>Tiger Lake U/TGL U</td> <td>Tiger Lake UP3/TGL UP3</td> </tr> <tr> <td>Tiger Lake Y/TGL Y</td> <td>Tiger Lake UP4/TGL UP4</td> </tr> </table> <p><b>PCB Stackup and Design Considerations on page 34</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b></li> </ul>	USB 3.1 Gen1	USB 3.2 Gen 1x1 (5 Gb/s)	USB 3.1 Gen2	USB 3.2 Gen 2x1 (10 Gb/s)	Tiger Lake U/TGL U	Tiger Lake UP3/TGL UP3	Tiger Lake Y/TGL Y	Tiger Lake UP4/TGL UP4	August 2019 <i>continued...</i>
USB 3.1 Gen1	USB 3.2 Gen 1x1 (5 Gb/s)										
USB 3.1 Gen2	USB 3.2 Gen 2x1 (10 Gb/s)										
Tiger Lake U/TGL U	Tiger Lake UP3/TGL UP3										
Tiger Lake Y/TGL Y	Tiger Lake UP4/TGL UP4										

Document Number	Revision Number	Revision Description	Release Date
		<ul style="list-style-type: none"> <li>— UPM Calculator document number in <a href="#">Tiger Lake UP4 RIMB Z-Stack Tolerance Components</a> on page 36</li> <li>— Updated <a href="#">Tiger Lake UP4 Land Pattern and Corner NCTF PCB Routing Guidance</a> on page 48 on latest LPID</li> </ul> <p><b>General Design Considerations on page 51</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— <a href="#">TCP0_MBIAS_RCOMP</a></li> </ul> </li> <li>• <b>CPU I/O on page 79</b></li> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— "The re-timer SMBUS connected to PCH via I2C" above <a href="#">Figure 46</a> on page 85</li> <li>— <a href="#">CFG Signals Functionality and Termination</a> on page 120</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— Re-timer SMBUS signal to PCH new name "I<sup>2</sup>C" in <a href="#">Figure 46</a> on page 85</li> <li>— <a href="#">CATERR# Topology</a> on page 117 with PU information</li> </ul> </li> </ul> <p><b>PCH IOs on page 121</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">I<sup>2</sup>C Interface Design Guidelines</a> on page 185</li> <li>— <a href="#">SMLink Description</a> on page 187</li> <li>— <a href="#">Integrated Bluetooth* and USB 2.0 Design Considerations</a> on page 152</li> </ul> </li> <li>• <b>Removed</b> Monitoring Integrated Sensors Over SMLink1</li> </ul> <p><b>Removed Electromagnetic Compatibility.</b> Refer Platform Design Guide Excelsheet for the same from this revision onwards.</p> <p><b>Platform Ingredients on page 206</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— GPIO names of Non-per-pad-configurable group <a href="#">Sensors - Configurable Voltage Considerations</a> on page 220</li> </ul> </li> </ul> <p><b>Power Delivery on page 376</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> Bypass and Aux Configuration Registers</li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Audible Noise Reduction</a> on page 389</li> <li>— <a href="#">Figure 243</a> on page 431, <a href="#">Figure 244</a> on page 432, <a href="#">Figure 245</a> on page 433, <a href="#">Figure 246</a> on page 434, <a href="#">Figure 247</a> on page 435</li> <li>— <a href="#">TCSS Power Adders Guidance</a> on page 397</li> <li>— Critical requirements to prevent system failure in <a href="#">VCCSTG and Discharge Requirements</a> on page 385</li> <li>— <a href="#">Table 218</a> on page 394 and table notes</li> <li>— SLP_A# and CPU_C10_GATE# descriptions in <a href="#">Table 227</a> on page 436</li> </ul> </li> </ul> <p><b>Platform Instrumentation for Power Measurement and Correlation on page 470</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Table 241</a> on page 482</li> </ul> </li> </ul> <p><b>Platform Debug and Test Hooks on page 488</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— <a href="#">Figure 271</a> on page 496</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— CFG[0] to EAR_N in <a href="#">Table 246</a> on page 493</li> </ul> </li> </ul>	
607872	1.0	<p><b>Introduction on page 29</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Table 1</a> on page 29</li> <li>— <a href="#">Table 2</a> on page 31</li> </ul> </li> </ul>	October 2019

*continued...*

Document Number	Revision Number	Revision Description	Release Date
		<ul style="list-style-type: none"> <li>— <a href="#">Table 3</a> on page 32</li> </ul> <p><b>System Memory Interface Design Guidelines on page 64</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> RCOMP [1] and RCOMP [2] data from all memory topology. There is only one RCOMP device.</li> </ul> <p><b>CPU I/O on page 79</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> eDP to DDIA only</li> </ul> <p><b>PCH IOs on page 121</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> PCH PCIe* UP4 port numbers in <a href="#">Table 63</a> on page 121</li> </ul> <p><b>Power Integrity on page 368</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <a href="#">Figure 206</a> on page 370</li> </ul> <p><b>Power Delivery on page 376</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— <a href="#">Figure 218</a> on page 399, <a href="#">Figure 219</a> on page 400, <a href="#">Figure 220</a> on page 401, and <a href="#">Figure 221</a> on page 401</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">SoC Load Switches</a> on page 385</li> <li>— Descriptions of tPCH32 in <a href="#">Table 231</a> on page 449</li> <li>— <a href="#">Table 229</a> on page 440</li> <li>— <a href="#">Additional Power Savings with Respect to VCCST Rail</a> on page 429</li> </ul> </li> <li>• <b>Removed</b> tCPU30, tCPU31, tCPU32.</li> </ul> <p><b>Platform Debug and Test Hooks on page 488</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— Directions for hook pins in <a href="#">Table 246</a> on page 493</li> <li>— 2 wire descriptions in <a href="#">Intel® DCI Implementation</a> on page 500</li> </ul> </li> </ul>	
607872	1.1	<p><b>CPU I/O on page 79</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— Thunderbolt™4 in <a href="#">Thunderbolt™ Design Guidelines</a> on page 79</li> <li>— USB 4 in <a href="#">USB Type C Power Delivery Considerations</a> on page 407</li> <li>— Dual eDP support in <a href="#">Table 33</a> on page 93 <a href="#">Table 44</a> on page 101</li> </ul> </li> </ul> <p><b>Power Delivery on page 376</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <a href="#">Figure 252</a> on page 446 with VDD2 for LP4/4x and IMVP VR sequence as per IMVP9</li> </ul> <p><b>Platform Debug and Test Hooks on page 488</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> Hook3 note moved from hook[0] to hook[3] row in <a href="#">Table 246</a> on page 493</li> </ul>	December 2019
607872	1.2	<p><b>Introduction on page 29</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <a href="#">Table 1</a> on page 29 with MIPI DSI in Internal Display</li> </ul> <p><b>PCB Stackup and Design Considerations on page 34</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Figure 19</a> on page 44, <a href="#">Figure 20</a> on page 45, and <a href="#">Figure 21</a> on page 47</li> <li>— <a href="#">Figure 22</a> on page 48, <a href="#">Figure 23</a> on page 49 and <a href="#">Figure 24</a> on page 50</li> </ul> </li> </ul> <p><b>General Design Considerations on page 51</b></p> <ul style="list-style-type: none"> <li>• <b>Removed</b> RCOMP in this document and made available in the respective excel sheet</li> </ul> <p><b>System Memory Interface Design Guidelines on page 64</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b></li> </ul>	April 2020

*continued...*

Document Number	Revision Number	Revision Description	Release Date
		<ul style="list-style-type: none"> <li>— DDL Support in Memory Down Types in <a href="#">Table 14</a> on page 71 and <a href="#">Table 15</a> on page 72</li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— DRAM Die Density in <a href="#">Table 10</a> on page 67</li> <li>— PCB Layers to 10L in <a href="#">Table 12</a> on page 69 and <a href="#">Table 13</a> on page 70</li> <li>— SDP Max Capacity in <a href="#">Table 13</a> on page 70 and <a href="#">Table 14</a> on page 71</li> </ul> </li> <li>• <b>Removed</b> ECC in <a href="#">DDR Byte Swapping</a> on page 73</li> <li><b>CPU I/O on page 79</b></li> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— Note for <a href="#">Figure 49</a> on page 88</li> <li>— <a href="#">General Routing Guidelines</a> on page 113, <a href="#">Slot Reset Implementation</a> on page 114, and <a href="#">Debug Guidelines</a> on page 115</li> </ul> </li> <li>• <b>Updated</b> <a href="#">Figure 44</a> on page 83</li> <li><b>PCH IOs on page 121</b></li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Platform Clock Design Guidelines</a> on page 121</li> <li>— SATALED# -&gt; SATA_LED# in <a href="#">Table 72</a> on page 134</li> <li>— DMIC_CLK_A and DMIC_CLK_A in <a href="#">Table 86</a> on page 159</li> <li>— SM Link description in <a href="#">SMBus 2.0/SMLink Platform Specific Important Information</a> on page 187</li> </ul> </li> <li><b>Platform Ingredients on page 206</b></li> <li>• <b>Added</b> <a href="#">Download and Execute (DnX)</a> on page 210</li> <li><b>Platform Connectivity on page 247</b></li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Table 182</a> on page 318 and also its notes</li> <li>— <a href="#">Figure 185</a> on page 323, <a href="#">Figure 186</a> on page 324, <a href="#">Figure 187</a> on page 325, and <a href="#">Figure 188</a> on page 326</li> </ul> </li> <li><b>Power Delivery on page 376</b></li> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— <a href="#">Table 226</a> on page 429</li> <li>— <a href="#">TCSS Power Adders Guidance</a> on page 397</li> <li>— <a href="#">DSW and PRIMARY Power up / Power Down Special Requirements</a> on page 455</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">VCCIN_AUX Requirements</a> on page 381</li> <li>— <a href="#">Bypass Rails (Optional)</a> on page 383</li> <li>— <a href="#">UP3 Line Requirement</a> on page 394</li> <li>— tPCH02a, tPCH02b, tPCH03a, tPCH03b, tPCH35 parameters of with notes 48 and 49 in <a href="#">Table 231</a> on page 449</li> </ul> </li> <li>• <b>Removed</b> <ul style="list-style-type: none"> <li>— Bypass and Aux Configuration Registers. Refer to Intel® 500 Series Chipset Family Platform Controller Hub (PCH) EDS Vol 2 (#619207)</li> <li>— S3 column in <a href="#">Power States</a> on page 440</li> </ul> </li> <li><b>Platform Debug and Test Hooks on page 488</b></li> <li>• <b>Added</b> <a href="#">Intel® Small Form Factor Debug Connector</a> on page 496</li> <li>• <b>Removed</b> Additional Routing Guidelines to Support Intel® Silicon View Technology (Intel® SVT) based DFM HVM Test Solution section</li> </ul>	
607872	1.5	<b>Introduction on page 29</b> <ul style="list-style-type: none"> <li>• <b>Updated</b> <a href="#">Reference Documents</a> on page 33</li> <li><b>System Memory Interface Design Guidelines on page 64</b></li> </ul>	June 2020

*continued...*

Document Number	Revision Number	Revision Description	Release Date
		<ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— PCB Layer row in <a href="#">Table 13</a> on page 70 and <a href="#">Table 12</a> on page 69</li> <li>— <a href="#">DDR Byte Swapping</a> on page 73</li> </ul> </li> <li><b>CPU I/O on page 79</b></li> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— Note under <a href="#">Table 34</a> on page 93</li> <li>— <a href="#">Table 28</a> on page 91</li> <li>— <a href="#">Hybrid Intel® Optane™ Memory Support</a> on page 112</li> </ul> </li> <li>• <b>Updated</b> <a href="#">Table 55</a> on page 108</li> <li><b>PCH IOs on page 121</b></li> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— Note in <a href="#">Touch Host Controller (THC) Design Guidelines</a> on page 184</li> <li>— <a href="#">General Purpose I/Os Design Guidelines</a> on page 194</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Table 66</a> on page 128</li> <li>— Notes 7 and 8 in <a href="#">PCH PCI Express* Interface Configuration Details</a> on page 129</li> <li>— VCCSPI to SPI in <a href="#">Serial Peripheral Interface (SPI0) Guidelines</a> on page 167</li> <li>— <a href="#">Table 125</a> on page 195 and <a href="#">Table 126</a> on page 196</li> <li>— <a href="#">Table 86</a> on page 159</li> <li>— <a href="#">Table 89</a> on page 163</li> </ul> </li> <li><b>Platform Ingredients on page 206</b></li> <li>• <b>Updated</b> VCCSPI to SPI in and <a href="#">Optimization Guidelines</a> on page 208</li> <li><b>Power Delivery on page 376</b></li> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— HU3 Processor note in <a href="#">Power Delivery</a> on page 376</li> <li>— Note about cTDP PD specification in <a href="#">Power Map Tool</a> on page 377</li> <li>— Note for external bypass benefit per scenario in <a href="#">Trade-offs - Volume vs. Premium Power Maps</a> on page 386</li> <li>— Notes under <a href="#">Table 215</a> on page 386</li> <li>— Reference document in <a href="#">General Processor Power Delivery Considerations</a> on page 388</li> <li>— <a href="#">SOI State Definitions</a> on page 465</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— VCCST in <a href="#">VCCST Requirements</a> on page 385</li> <li>— V_TOB voltage tolerance range in <a href="#">Table 208</a> on page 382</li> <li>— VID2 and VID3 in <a href="#">Table 218</a> on page 394</li> </ul> </li> <li>• <b>Removed</b> S3 in <a href="#">Additional Power Savings with Respect to VCCST Rail</a> on page 429</li> <li><b>Platform Debug and Test Hooks on page 488</b></li> <li>• <b>Updated</b> <a href="#">Intel® DCI Implementation</a> on page 500</li> </ul>	
607872	2.0	<b>System Memory Interface Design Guidelines on page 64</b> <ul style="list-style-type: none"> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— Note 6 and referenced for DDP Memory Down Types in <a href="#">Table 13</a> on page 70</li> <li>— Note 7 and referenced for DDP Memory Down Types in <a href="#">Table 14</a> on page 71</li> </ul> </li> <li><b>CPU I/O on page 79</b></li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— Last 3 rows of <a href="#">Table 28</a> on page 91</li> </ul> </li> </ul>	August 2020

*continued...*

Document Number	Revision Number	Revision Description	Release Date
		<ul style="list-style-type: none"> <li>— CFG 5 6 and 7 details in <a href="#">Table 62</a> on page 120</li> <li><b>PCH IOs on page 121</b></li> <li>• <b>Added</b> note in <a href="#">UART Interface</a> on page 193</li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Table 66</a> on page 128</li> <li>— SATADEVSLP0 and SATADEVSLP1 with DEVSLP0 and DEVSLP1 respectively in <a href="#">SATA Signal Description</a> on page 134</li> <li>— Break-out Length guideline in <a href="#">USB 3.2 Gen 1x1 (5 Gb/s) and Gen 2x1 (10 Gb/s) Topology Guidelines</a> on page 143</li> <li>— Via Stub length with recommendation to USB 3.2 <b>Tx</b> and <b>Rx signal pair</b> and CMC choke recommendation points in <a href="#">USB 3.2 General Guidelines</a> on page 145</li> <li>— Replaced Intel® ME with Intel® CSME in <a href="#">Controller Link</a> on page 192</li> </ul> </li> <li>• <b>Removed</b> Intel HD Audio 2-Load Topology (Device Down and Add-In Card)</li> </ul> <p><b>Power Delivery on page 376</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— TVOS in <a href="#">Table 207</a> on page 381 and <a href="#">Figure 214</a> on page 383</li> <li>— <a href="#">UP4-Line Requirement</a> on page 393 back.</li> <li>— Note 11 in <a href="#">Table 217</a> on page 393</li> <li>— Note 11 and referenced in V_OVS Max and T_OVS Max in <a href="#">Table 218</a> on page 394</li> <li>— Note 51 under <a href="#">Table 231</a> on page 449</li> <li>— Note and <a href="#">Table 235</a> on page 466 in <a href="#">S0ix State Definitions</a> on page 465</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— HU3 to H35 in Note of <a href="#">Power Delivery</a> on page 376</li> <li>— V_TOB values in <a href="#">Table 207</a> on page 381, <a href="#">Table 207</a> on page 381</li> <li>— Replaced VCC_1P05OUT_FET with VCC1P05_OUT_FET in <a href="#">SoC Load Switches</a> on page 385</li> <li>— Replaced VPU_C10_GATE# with CPU_C10_GATE# in Note 15 of <a href="#">Table 229</a> on page 440</li> <li>— <a href="#">Figure 257</a> on page 459 and <a href="#">Figure 258</a> on page 460</li> <li>— <a href="#">DSW_PWROK Min LOW Time during Cycling</a></li> <li>— <a href="#">Figure 260</a> on page 465</li> </ul> </li> <li>• <b>Removed</b> tPCH47,tPCH48 and tPCH49 in <a href="#">Table 231</a> on page 449</li> </ul>	
607872	2.1	<p><b>CPU I/O on page 79</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> Processor PCIe TX EQ Tuning on page 113</li> <li>• <b>Updated</b> CFG 5 6 and 7 details in <a href="#">Table 62</a> on page 120</li> </ul> <p><b>Platform Ingredients on page 206</b></p> <ul style="list-style-type: none"> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— Connection values in <a href="#">Sensors Debug Hooks</a> on page 235</li> <li>— ISH_I2C0_SDA and ISH_I2C1_SCL - Pin Function and Description in <a href="#">Table 143</a> on page 236</li> <li>— Pin 11 and 12 Signal Name in <a href="#">Table 144</a> on page 237</li> </ul> </li> </ul> <p><b>Power Delivery on page 376</b></p> <ul style="list-style-type: none"> <li>• <b>Added</b> <ul style="list-style-type: none"> <li>— V_Undershoot and T_UDS MAX in <a href="#">Table 217</a> on page 393 and <a href="#">Table 218</a> on page 394</li> </ul> </li> <li>• <b>Updated</b> <ul style="list-style-type: none"> <li>— <a href="#">Figure 245</a> on page 433 and <a href="#">Figure 246</a> on page 434</li> </ul> </li> </ul>	September 2020

*continued...*



Document Number	Revision Number	Revision Description	Release Date
		<ul style="list-style-type: none"><li>— Note 13 of <a href="#">Table 229</a> on page 440</li><li>— <a href="#">Surprise Power Down Sequencing Considerations</a> on page 462</li><li>• <b>Removed</b> S0i3.4 in <a href="#">S0ix State Definitions</a> on page 465</li></ul>	
607872	2.2	<p><b>CPU I/O on page 79</b></p> <ul style="list-style-type: none"><li>• <b>Added</b> note in <a href="#">CSI Signal Descriptions</a> on page 110</li><p><b>Power Delivery on page 376</b></p><ul style="list-style-type: none"><li>• <b>Added</b> <a href="#">Figure 249</a> on page 442</li><li>• <b>Updated</b><ul style="list-style-type: none"><li>— XDP to debug port connector in <a href="#">SoC Load Switches</a> on page 385</li><li>— Title of <a href="#">Figure 248</a> on page 442</li></ul></li><li>• <b>Removed</b> 1.1V VCCIN_Aux retention lines in <a href="#">Table 205</a> on page 378</li></ul><p><b>Platform Debug and Test Hooks on page 488</b></p><ul style="list-style-type: none"><li>• <b>Added</b> Note in <a href="#">Intel® Small Form Factor Debug Connector</a> on page 496</li><li>• <b>Updated</b> MB SFF Header of MIPI60_CFG1_N in <a href="#">Intel® Small Form Factor Debug Connector</a> on page 496</li></ul></ul>	November 2020

## 1.0 Introduction

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This Design Guide provides motherboard implementation recommendations for the Tiger Lake UP3 and UP4 platforms, based on the Tiger Lake processor.

### **NOTE**

The Tiger Lake U processor line is now named Tiger Lake UP3 or TGL UP3.

The Tiger Lake Y processor line is now named Tiger Lake UP4 or TGL UP4.

The Tiger Lake UP3/UP4 platform consists of an Tiger Lake UP3 42 /UP4 42 processor plus an Tiger Lake Platform Controller Hub (PCH) in the same Multi Chip Package (MCP). In the rest of the document, TGL PCH will be referred to as "PCH" and TGL CPU will be referred to as "CPU".

## 1.1 Tiger Lake UP3 Platform

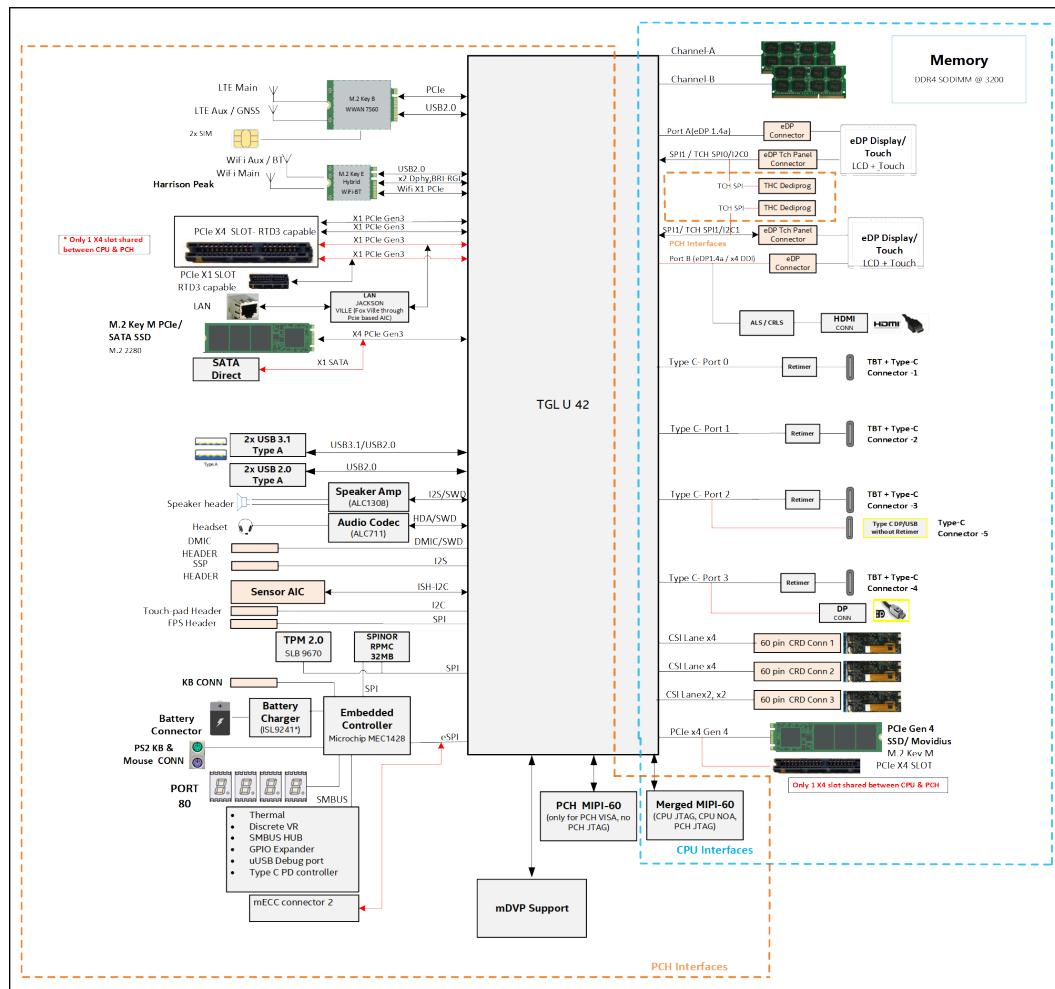
**Table 1. Tiger Lake UP3 Key Feature Summary**

Feature	Description
Thermal (SoC)	UP3 4+2: 15W
SoC	TGL UP3 CPU (4+2) PCH – LP
CPU IO	PCIe Gen4, 4x Type-C (TBT, USB 4.0, DP), DDR4,LPDDR4x, LPDDR5, CSI, DSi, DDI, eDP
PCH-LP	12 lanes HSIO, USB2, USB 3.2, eSPI, SPI, LPSS, I2C, SMBus
Power Delivery	CPU FIVR/PCH FIVR w/discrete VR ROP USB-C PD Controller
Memory	DDR4 - Max 64GB @ 3200MT/s LPDDR4x - Max 32GB @ 4266MT/s
Storage	PCIe/SATA
Boot	SPI NOR
Discrete Graphics	Optional x4 PCIe – Hybrid Graphics support w/Hot Plug
Internal Display	eDP , MIPI DSI
External displays	4 Wired Type-C (DP/TBT) Wireless (Miracast2.0 r2) (Wi-Fi) DDI(DP, HDMI)
Wireless	Quasar CNVi w/Harrison Peak (Wi-Fi/BT) module WWAN – XMM 7560
Clocking	38.4MHz Platform Xtal
Wired COMMs	Integrated GbE w/ discrete Gbit Lan Phy

*continued...*

Feature	Description
Imaging	4x WF/UF 2D Camera – (13MP WF, 2MP UF, 2MP Others) Other Cameras: AutoFocus, Face Tracking, Image Biometrics
Docking/Walk-up-Port	4x Ports Max: Type-C/Type-A
Audio	3.5mm Headphone Jack, Integrated Speakers/Mic, Docking Soundwire, Intel HD Audio, I2S, USB
Sensors	Ambient Light Sensor, Gyroscope, Accelerometer, Compass, Proximity, Pressure
Misc, GPIO's	Power/Vol button/Indicator LEDs/Keyboard/Touchpad/etc

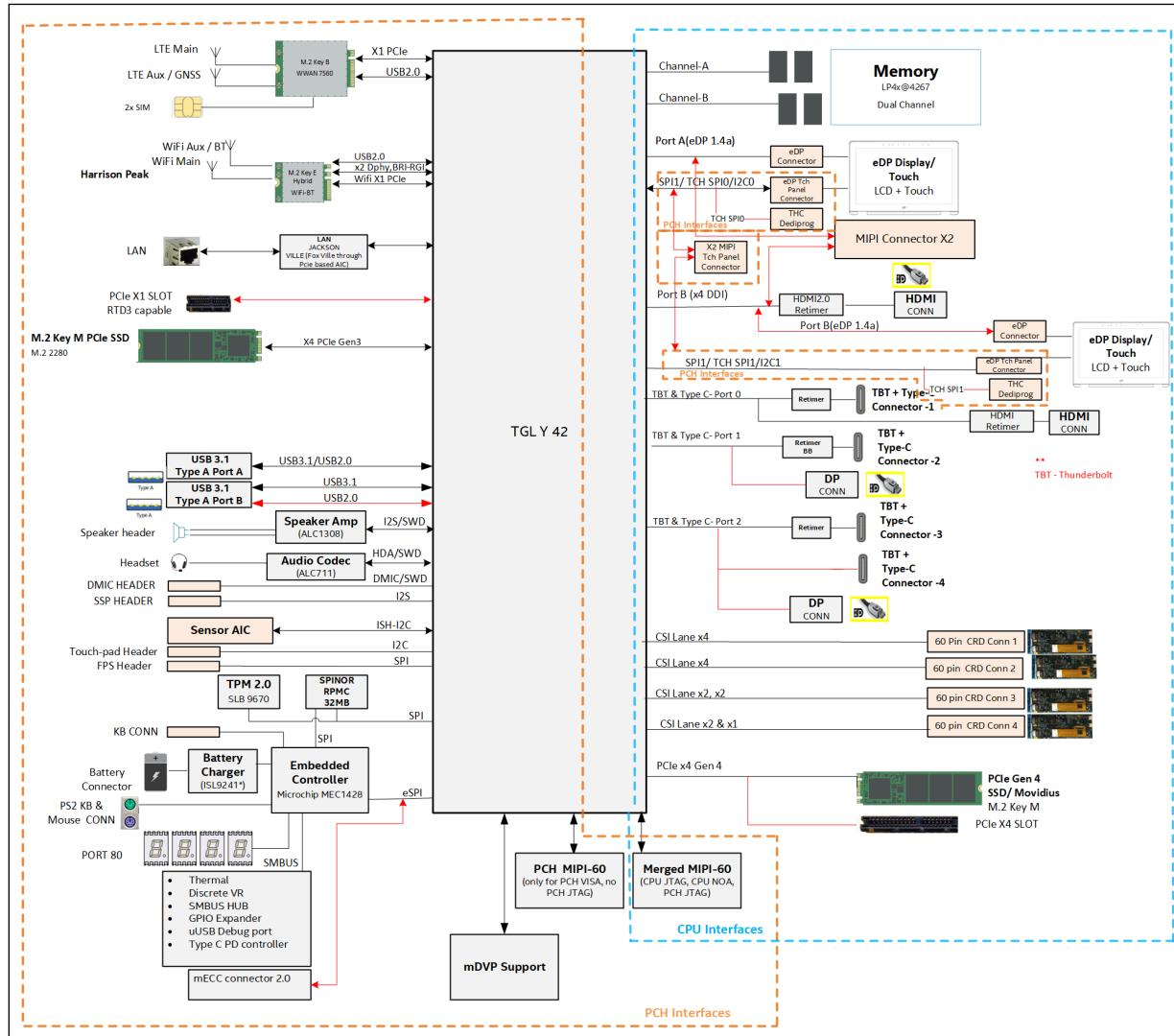
**Figure 1.** Tiger Lake UP3 Platform Block Diagram



## 1.2 Tiger Lake UP4 Platform

**Table 2.** Tiger Lake UP4 Key Feature Summary

Feature	Description
SoC	UP4 CPU (4+2) PCH – LP
CPU I/O PCH-LP I/O	3x Type-C (TBT, USB 4.0, DP), LPDDRx, LPDDR5, CSI2, DSI, DDI, eDP 1.4b HSIO, USB 3.2, PCIe Gen4, USB2,eSPI, SPI, LPSS, I2C/I3C, SMBus
Power Delivery	CPU FIVR/PCH FIVR w/discrete VR ROP USB-C PD controller
Memory	LPDDR4x - Max 32GB @ 4266MT/s
Storage	PCIe
Boot	SPI NOR
Internal Display	MIPI-DSI 1.3/eDP 1.4b
External displays	3 Wired Type-C(DP/TBT) Wireless (Miracast2.0* r2) (Wi-Fi) DDI(DP/HDMI)
Wireless	Quasar CNVi w/ Harrison Peak (Wi-Fi/BT) WWAN – XMM 7560
Clocking	38.4MHz Platform Xtal
Imaging	6x WF/UF 2D Camera – (23MP WF, 8MP UF, 2x 2MP Others) Other Cameras: Auto-Focus, Face Tracking, Image Biometrics
Walk up ports	3x Type-C w/Charging
Audio	3.5mm Headphone Jack, Integrated Speakers/Mic, Docking Soundwire, Intel HD Audio, I2S, USB2
Sensors	Ambient Light Sensor, Gyroscope, Accelerometer, Compass, Proximity, Barometer
Misc	Power/Vol button/Indicator LEDs/etc via. discrete EC.

**Figure 2.** Tiger Lake UP4 Platform Block Diagram

**Table 3.** High Level Comparison Between Ice Lake and Tiger Lake Platform Features

Platform Feature	Ice Lake	Tiger Lake
Memory	DDR4 (3200 MT/s) LPDDR4x (3733 MT/s)	DDR4 (3200 MT/s) LPDDR4x (4266 MT/s)
Display	eDP 1.4b, MIPI-DSI 1.3, DP1.4, HDMI2.0, DP tunneling mode, DP-TBT	eDP 1.4b, MIPI-DSI 1.3, DP1.4, HDMI2.0, DP tunneling mode, DP-TBT

**Table 4.** OS Support

Segment	OS Support
Consumer	Windows* 10 with RSx (in-market OS) Linux* (Refer Note1)

*continued...*

Segment	OS Support
	Chrome* (Refer Note2)
Corporate	Windows* 10 with RSx (in-market OS)
<p>Notes:</p> <ol style="list-style-type: none"> <li>1. Linux* supported by Intel via the up-streaming of Intel Linux* drivers to the Linux Open Source Community. Adoption into individual Linux distributions is dependent upon the OS vendor.</li> <li>2. Chrome* OS features and support are dependent upon Google* and an approved reference design.</li> </ol>	

## 1.3

## Reference Documents

Document Title	Document Number
Tiger Lake Processor External Design Specification (EDS) Volume 1 of 2	608190
Tiger Lake Processor External Design Specification (EDS) Volume 2 of 2	575681
Tiger Lake PCH-LP External Design Specification, Volume 1 of 2	576591
Tiger Lake PCH-LP External Design Specification, Volume 2 of 2	575857
Tiger Lake Platform Memory Interface I/O Package Trace Length Calculator	605928
Tiger Lake Platform Mobile Thermal and Mechanical Design Guide	607873
Tiger Lake UP3 Platform DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit	609003
Tiger Lake UP4 Platform LP4x Reference Validation Platform (RVP) Technical Documentation Kit	610815
Fiber weave Effect: Practical Impact Analysis and Mitigation Strategies	406926
Tiger Lake UP3 Processor Line BGA Package Ballout Mechanical Specification	604917
Tiger Lake UP4 Processor Line BGA Package Ballout Mechanical Specification	607754
Tiger Lake Platform Runtime D3 (RTD3) Hardware and Software Recommendations Design Guide	576056
Tiger Lake Processor Family Core and Uncore BIOS Specification	611569
Reading and Overriding Power Delivery via BIOS Technical Advisory	626935
New BIOS Debug Log Technical Advisory	614453
Tiger Lake VCCIN Shutdown Demotion Threshold Tuning for Power Optimization Technical Advisory	626886

## 2.0 PCB Stackup and Design Considerations

Refer to *Tiger Lake Platform Mobile Thermal Mechanical Design Guide (TMDG, #607873)* for thermal and mechanical design guidelines, such as component PCB pad design recommendations and NCTF corner ball routing guidelines.

### NOTES

1. Metric units um and mm are used as the primary unit in this PDG.
2. Dielectric thickness for each layer is measured as the coating above trace.

### 2.1

#### Motherboard RIMB/HIMB for Tiger Lake UP4 Platforms

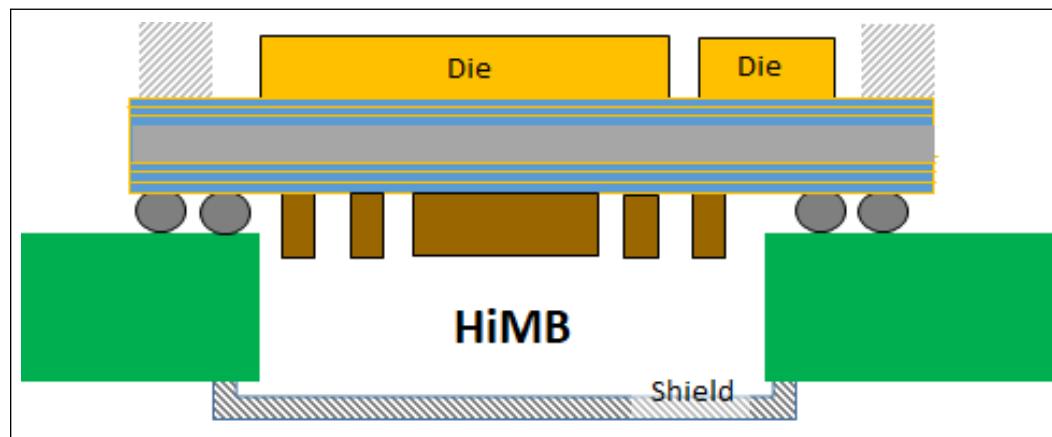
This section is intended for motherboard designs for platforms using the Tiger Lake UP4 processor. Platforms using the Tiger Lake UP4 processor are required to have Hole in Motherboard (HIMB) or Recess in Motherboard (RIMB) to accommodate the landside components (LSC). The HIMB or RIMB is required for Tiger Lake UP4 processor SKU only.

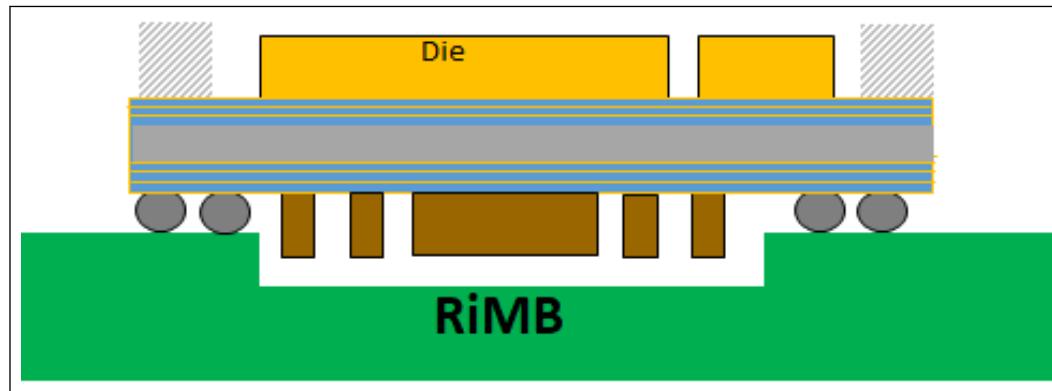
Intel recommends Any layer stack-up @ 0.8 mm thickness for TGL UP4 generation:

- Enables high speed IO margin
- Enables low UPM RIMB

RIMB designs can be double sided. HIMB designs need additional EMI shielding.

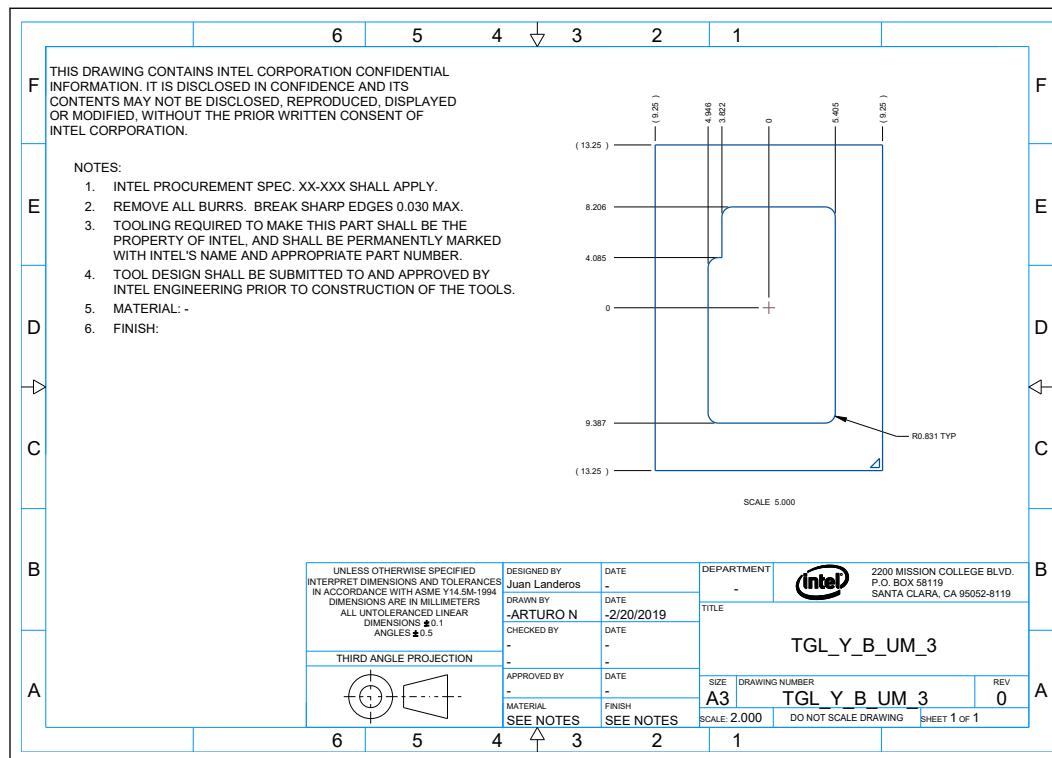
**Figure 3.** **Tiger Lake UP4 HIMB**



**Figure 4.** Tiger Lake UP4 RIMB**Table 5.** Tiger Lake UP4 RIMB Considerations

PCB Design	RIMB Optional Depths			UPM Risk
3-4-3+, 0.916mm	Laser process to Layer 3	220um (+/- 50u)		1052 UPM
	Mech process	240um (+/- 75u)		384 UPM
	Laser process to Layer 4	220um (+/- 50u)		0 UPM

Note: 1. Please refer to UPM calculator for your specific design

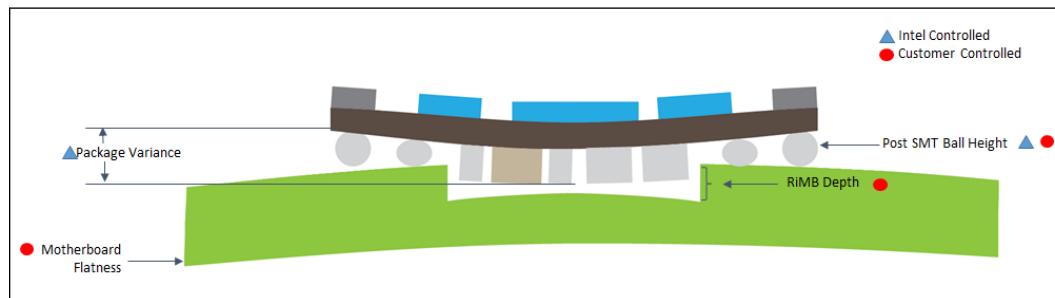
**Figure 5.** Tiger Lake UP4 Recess Dimensions

## 2.1.1 Tiger Lake UP4 RIMB Z-Stack Tolerance Components

Package and board materials dynamically flex/warp during the SMT Reflow process: Room Temperature > Reflow Temperature > Room Temperature

The warpage of the different components combine to create potential interference between the RIMB (cavity) and Package Components. The following illustration describes the different variables.

**Figure 6. Warpage of Components Creating Interference between RIMB and Package Components**



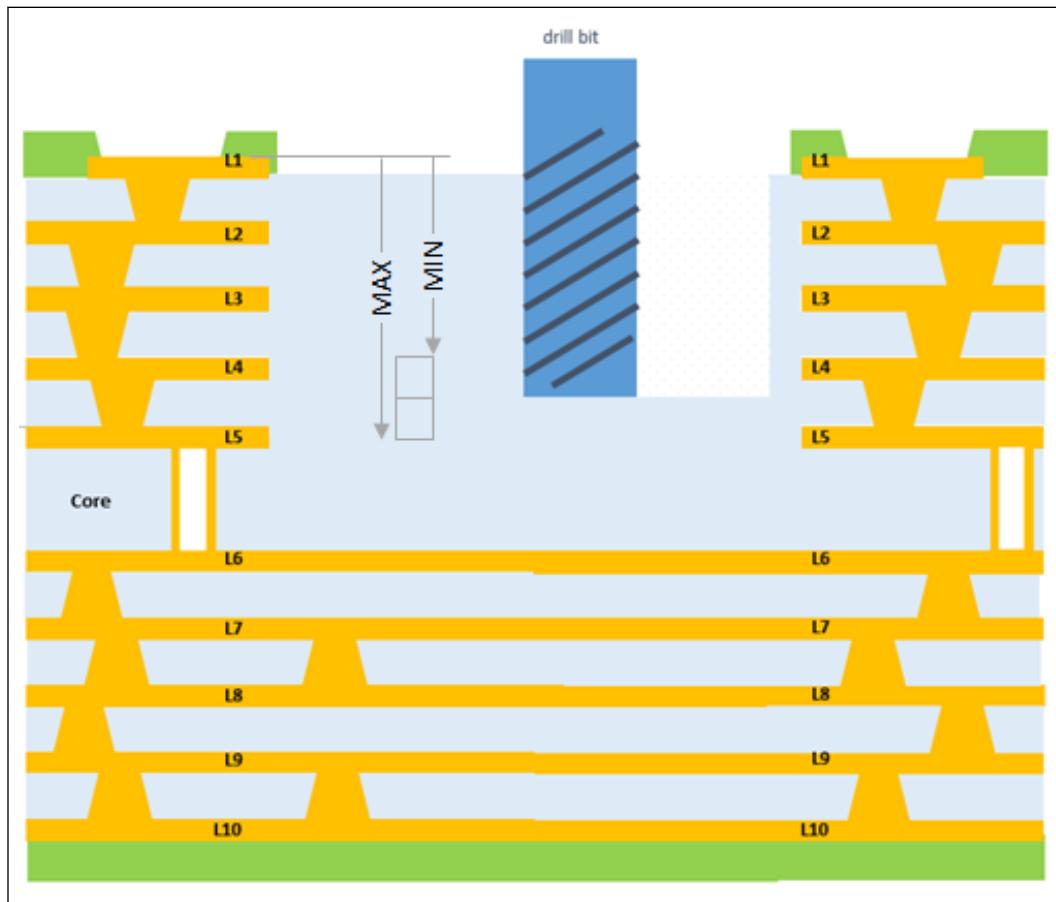
In order to determine the potential risk for RIMB and Component interference, Intel has developed a model to calculate the UPM (Units per Million) of boards that may have component-RIMB interference. Refer to the Tiger Lake UP4 UPM calculator(# 614089) for RIMB and UPM calculation..

**Figure 7. Component - RIMB Interference Calculation Example**

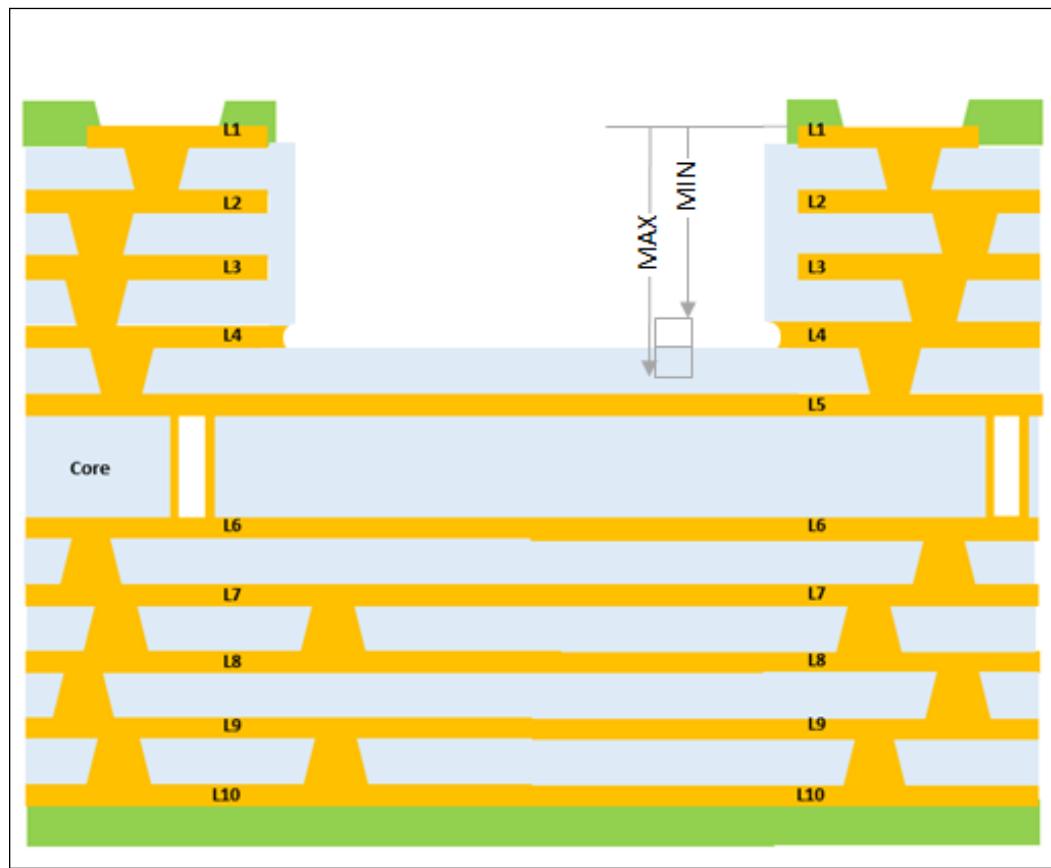
UPM Calculation		SAC Solder					
		Nominal (mm)	Range (mm)	(%)			
Package + LSC variance		-0.322	± 0.050	30%	Nominal = typical value or "as designed" value Range = typical range/spread of variable	Intel provided Customer owned Intel-customer co-owned Customer owned Sum of squares of ranges. Ranges assumed to be 4 sigma 1 sigma tolerance of all contributing tolerances Worst case tolerance sum; used to calculate % contribution	
Motherboard flatness		0.000	± 0.050	30%			
Post SMT BGA ball height		0.170	± 0.018	11%			
Recess depth		0.232	± 0.050	30%			
Distance between LSC and bottom of recess = Air Gap between LSCs and MB		0.080	0.088 0.022 0.168				
UPM based on normal distribution function for 0um LSC to PCB recess interference		<b>UPM</b>		<b>149</b>			

## 2.1.2 Common Manufacturing Methods

Figure 8. Mechanically Milling



**Figure 9.** Laser Stop Process



### 2.1.3 Tiger Lake UP4 RIMB Considerations for Any Layer, 10 Layer Stackup with 0.8mm Thickness

**Figure 10.** Any layer, 10 Layer Stackup, 0.8mm Thickness

Routing Layer	Memory		Non-Memory		Thickness (um)	EDW um	Dielectric Constant	Loss Tangent
	Layer Description	Tline Type	Layer Description	Tline Type				
1	S/M		S/M		13		3.7	0.031
	Power, GND	GND/PWR	BO, Power, GND	MS	30	9.6		
2	PP		PP		60		3.5	0.011
	GND	GND/PWR	GND	GND/PWR	25			
3	PP		PP		60		3.5	0.011
	BO, Main Route	SL	BO, Main Route	SL	15	5.3		
4	PP		PP		60		3.5	0.011
	GND	GND/PWR	GND	GND/PWR	25			
5	PP		PP		60		3.5	0.011
	BO, Main Route	SL	BO, Main Route	SL	15	5.3		
6	CORE		CORE		70		3.6	0.011
	GND	GND/PWR	GND	GND/PWR	15			
7	PP		PP		60		3.5	0.011
	Power	GND/PWR	Power	GND/PWR	25			
8	PP		PP		60		3.5	0.011
	Power, GND	GND/PWR	Main Route	SL	15	5.3		
9	PP		PP		60		3.5	0.011
	GND	GND/PWR	GND	GND/PWR	25			
10	PP		PP		60		3.5	0.011
	Power	GND/PWR	Main Route, Power, GND	MS	30	9.6		
	S/M		S/M		13		3.7	0.031
				TOTAL:	796.0			

### RIMB Design Considerations

**Figure 11. Laser Recess to Layer 3; Depth = 220um +/- 50 um**

UPM Calculation					
	(mm)	(mm)	(%)		
Package+LSC variance	-0.325	$\pm$	0.050	30%	Intel provided
Motherboard flatness	0.000	$\pm$	0.050	30%	Customer owned
Post SMT BGA ball height (0.43)	0.170	$\pm$	0.018	11%	Intel-customer co-owned
Recess Depth	0.220	$\pm$	0.050	30%	Customer owned
Distance between LSC and bottom of cavity	0.065	$\pm$	0.088	4 sigma tolerance combining all contributing tolerances	
		$\pm$	0.022	1 sigma tolerance of all contributing tolerances	
		$\pm$	0.168	Worst Case Tolerance Linear Sum: Used to calculate % Contribution	
UPM based on normal distribution function for 0um LSC to PCB Cavity interference		<b>UPM = 1644</b>			

**Figure 12. Laser Recess to Layer 4; Depth = 320um +/- 50 um**

UPM Calculation					
	(mm)	(mm)	(%)		
Package+LSC variance	-0.325	$\pm$	0.050	30%	Intel provided
Motherboard flatness	0.000	$\pm$	0.050	30%	Customer owned
Post SMT BGA ball height (0.43)	0.170	$\pm$	0.018	11%	Intel-customer co-owned
Recess Depth	0.320	$\pm$	0.050	30%	Customer owned
Distance between LSC and bottom of cavity	0.165	$\pm$	0.088	4 sigma tolerance combining all contributing tolerances	
		$\pm$	0.022	1 sigma tolerance of all contributing tolerances	
		$\pm$	0.168	Worst Case Tolerance Linear Sum: Used to calculate % Contribution	
UPM based on normal distribution function for 0um LSC to PCB Cavity interference		<b>UPM = 0</b>			

**Figure 13. Controlled Depth Milling to 260um +/- 100um**

10L, 0.916mm, 3-4-3+					
UPM Calculation					
	(mm)	(mm)	(%)		
Package+LSC variance	-0.325	± 0.050	28%	Intel provided	
Motherboard flatness	0.000	± 0.050	28%	Customer owned	
Post SMT BGA ball height (0.43)	0.170	± 0.018	9%	Intel-customer co-owned	
Cavity Depth	0.260	± 0.075	38%	Customer owned	
Distance between LSC and bottom of cavity	0.105	± 0.105	4 sigma tolerance combining all contributing tolerances		
		± 0.026	1 sigma tolerance of all contributing tolerances		
		± 0.193	Worst Case Tolerance Linear Sum: Used to calculate % Contribution		
UPM based on normal distribution function for 0um LSC to PCB Cavity interference		<b>UPM = 30</b>			

**Figure 14. Recess with Controlled Drilling; Depth = 260 um; Assume +/- 100 um Tolerance**

UPM Calculation					
	(mm)	(mm)	(%)		
Package+LSC variance	-0.325	± 0.050	23%	Intel provided	
Motherboard flatness	0.000	± 0.050	23%	Customer owned	
Post SMT BGA ball height (0.43)	0.170	± 0.018	8%	Intel-customer co-owned	
Recess Depth	0.260	± 0.100	46%	Customer owned	
Distance between LSC and bottom of cavity	0.105	± 0.124	4 sigma tolerance combining all contributing tolerances		
		± 0.031	1 sigma tolerance of all contributing tolerances		
		± 0.218	Worst Case Tolerance Linear Sum: Used to calculate % Contribution		
UPM based on normal distribution function for 0um LSC to PCB Cavity interference		<b>UPM = 346</b>			

**Figure 15. Recess with Controlled Drilling; Depth = 260 um; Assume +/- 75 um Tolerance**

UPM Calculation					
	(mm)	(mm)	(mm)	(%)	
Package+LSC variance	-0.325	±	0.050	26%	Intel provided
Motherboard flatness	0.000	±	0.050	26%	Customer owned
Post SMT BGA ball height (0.43)	0.170	±	0.018	9%	Intel-customer co-owned
Recess Depth	0.260	±	0.075	39%	Customer owned
Distance between LSC and bottom of cavity	0.105	±	0.105	4 sigma tolerance combining all contributing tolerances	
		±	0.026	1 sigma tolerance of all contributing tolerances	
		±	0.193	Worst Case Tolerance Linear Sum: Used to calculate % Contribution	
UPM based on normal distribution function for 0um LSC to PCB Cavity interference			<b>UPM = 30</b>		

## 2.2

### Non Critical To Function (NCTF) Solder Balls and Testability Recommendation

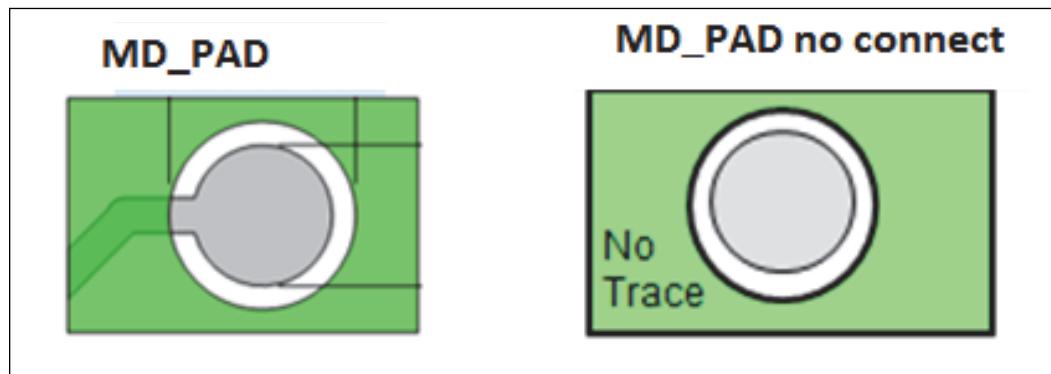
As we shift to thinner system designs, SMT is becoming more challenging with the corners being more susceptible to solder joint defects. Testing the corner NCTF Solder Joints (SJ's) is a good way to screen potential solder joint defects and check health of process. UP3/UP4 Processor corner NCTF SJ's have some pins connected to the package POWER/VCC or GROUND/VSS planes which can be used to test connectivity.

#### 2.2.1 Pad Definitions

##### Metal Defined (MD) Pad: (Traditional dog bone Via to BGA-Pad)

- Pad is defined as MD when 40% - 100% of the pad circumference is defined by metal.
- I/O Driven, trace width usually determined by Impedance matching.
- No connect is metal pad with "NO" trace connected (e.g. uvia in pad).
- MD pad type preferred for T/C performance.

**Figure 16. Metal Defined (MD) Pad**



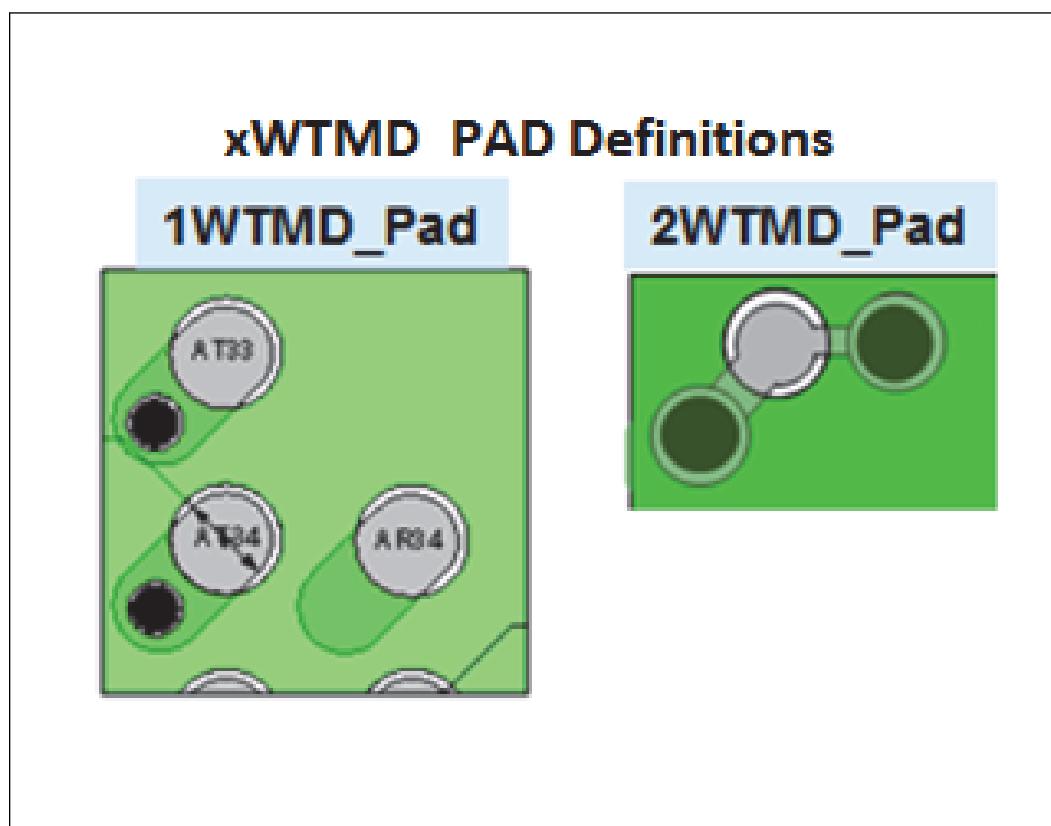
#### Spoked MD

Metal Defined pad with up to 4 traces branching off it such that at least 40% of pad periphery is still defined by metal. Used to improve solder joint reliability where a surface plane is present.

#### Wide Trace Defined (WTMD) Pad (Trace = Pad Diameter or Less)

- $xWTMD >> 1WTMD = 1$  Wide Trace,  $2WTMD = 2$  Wide Traces going to BGA Pad.
- Multiple "Wide Traces", can look/behave as a Spoke design.

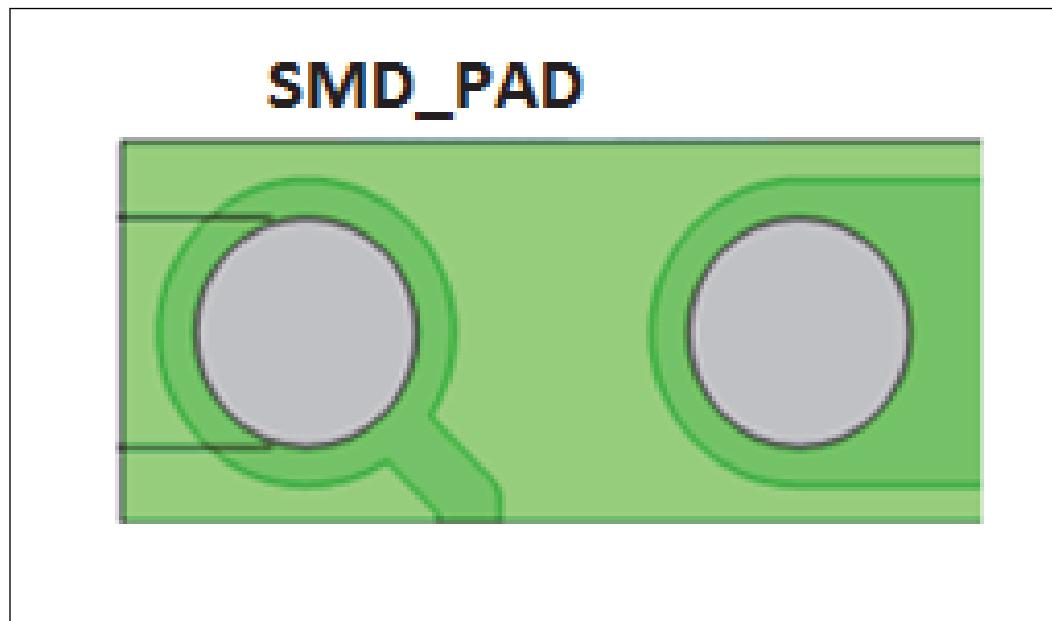
**Figure 17. Wide Trace Defined (WTMD) Pad**



### Soldermask Defined (SMD)

60% - 100% of the pad circumference is defined by Soldermask, pads in flood areas and/or Larger metal pad.

**Figure 18. Soldermask Defined Pad**



#### 2.2.2

### NCTF Implementation – Continuity/Resistance Test Threshold

- Continuity or resistance tests are developed using a pass/fail resistance threshold.
- The pass/fail threshold would be determined by the accuracy of the test equipment and measurement data obtained from boards with known good solder joints.
- For boards under test, a measurement below the pass/fail threshold may indicate a good package electrical solder joint (pass), and a measurement above the pass/fail threshold may indicate a bad package electrical solder joint (fail).

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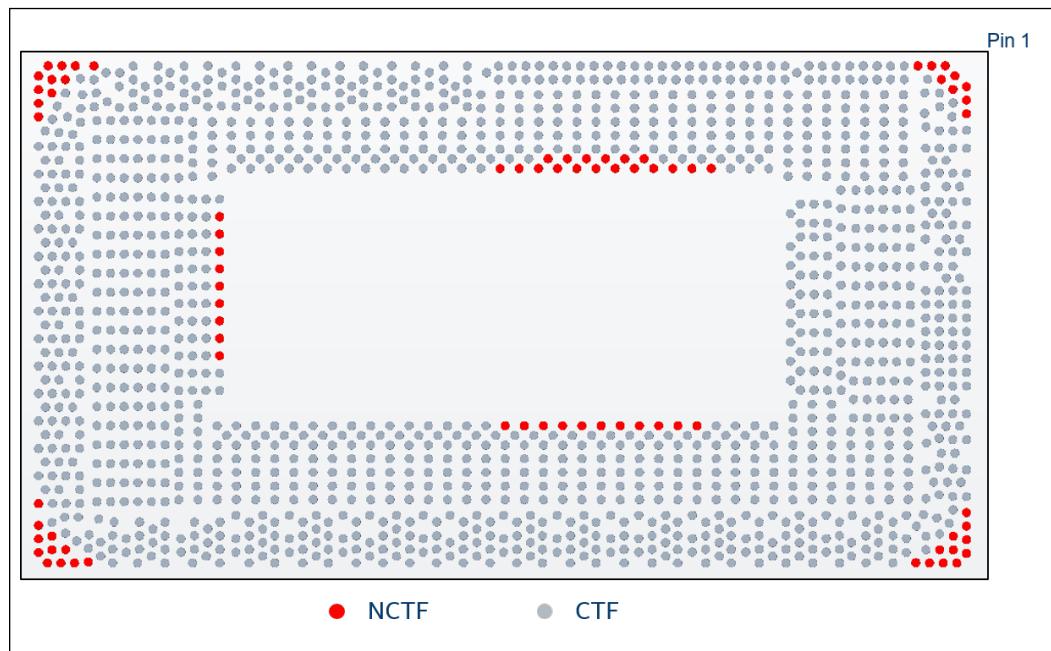
#### NOTE

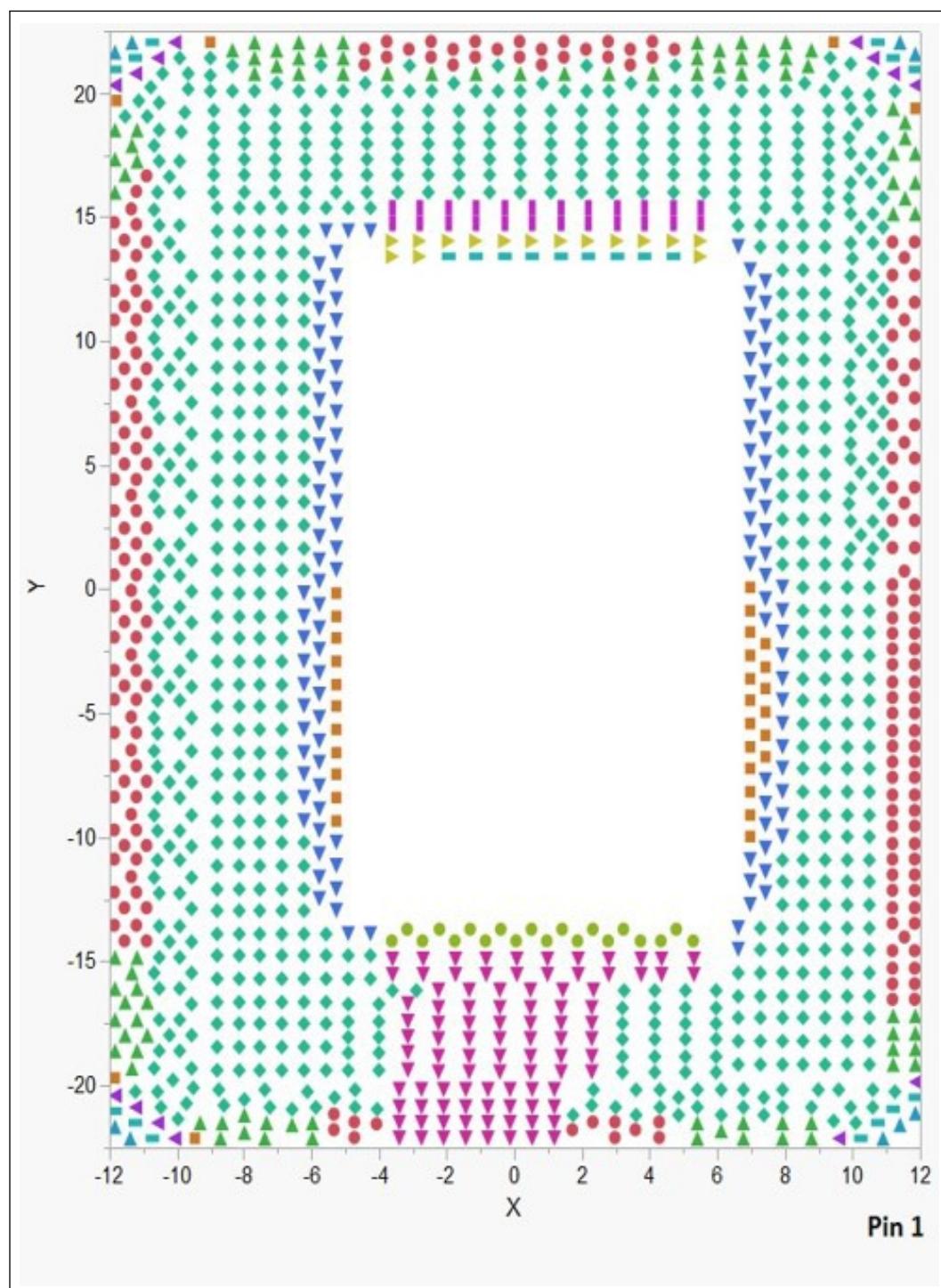
This type of electrical resistance test can detect a completely open solder joint between the package and board, but can be ineffective in detecting marginal solder joint connectivity (SJ that may not be mechanically sound).

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### 2.2.3 Tiger Lake UP3 Land Pattern and Corner NCTF PCB Routing Guidance

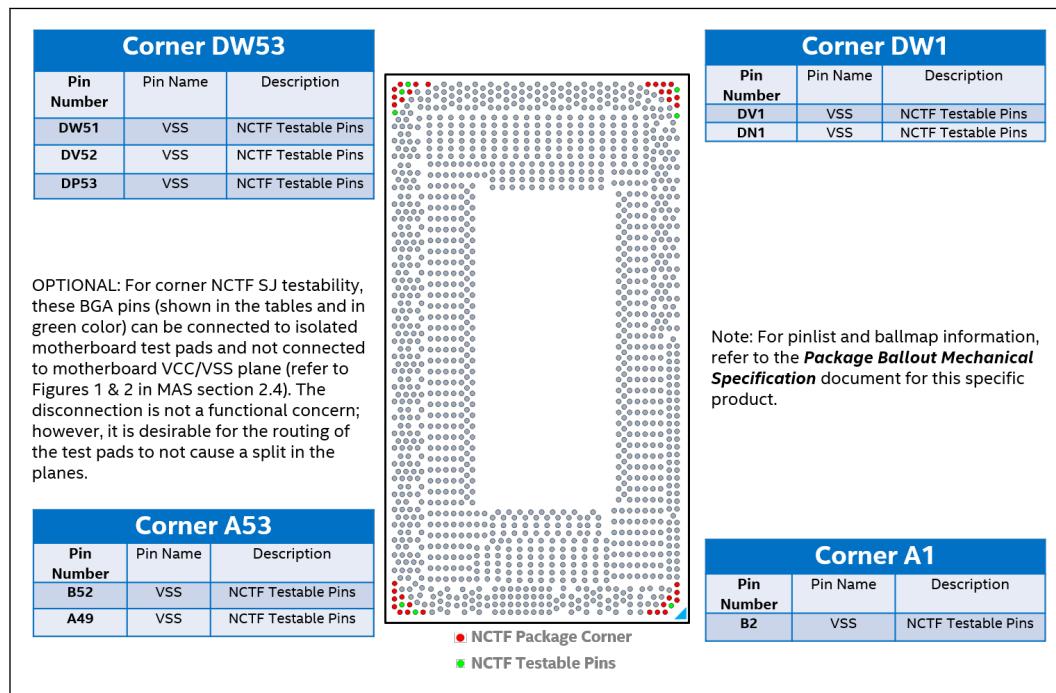
Figure 19. UP3 Package Non-Critical to Function (NCTF) Overview



**Figure 20. UP3 Land Pattern Guidance**

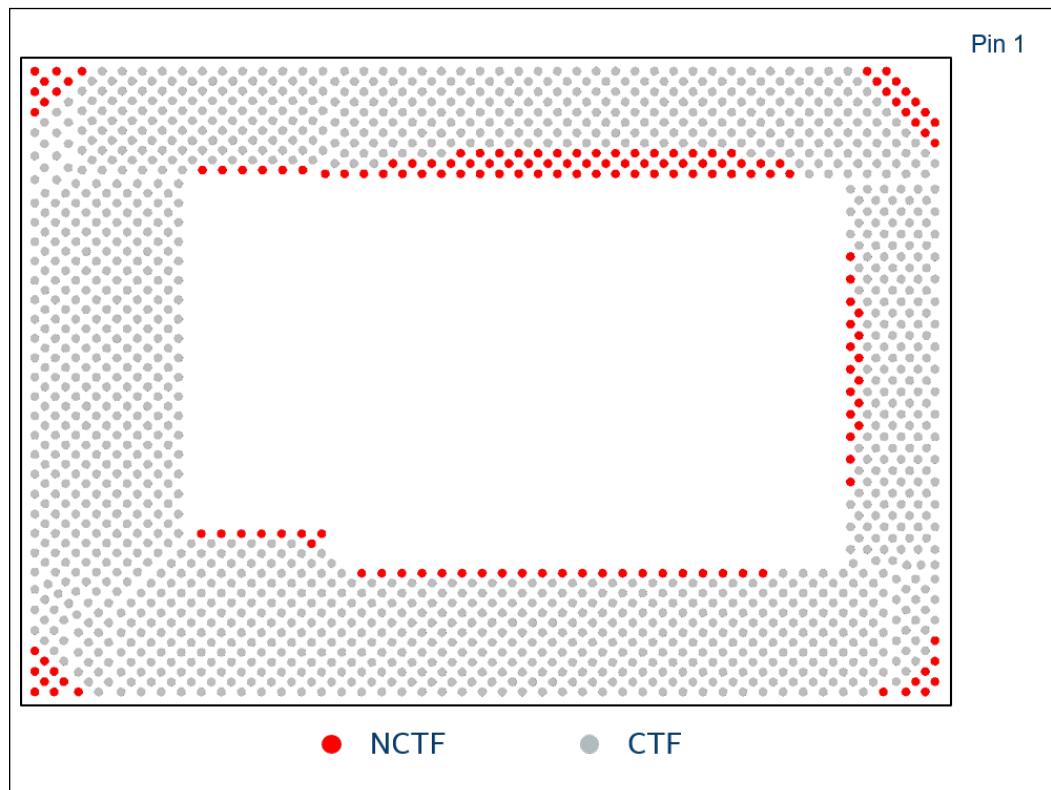
Legend	Pad Size (microns/mils) ; SRO Size (microns/mils)	Function	# of Balls
●	MD or Spoked Pad Diameter: 200x300um, SRO 300x400um; SMD Pad Diameter: 300x400um, SRO: 200x300um	CTF	204
▲	MD or Spoked Pad Diameter: 250x350um, SRO 350x450um; SMD Pad Diameter: 350x450um, SRO: 250x350um	CTF	92
▼	MD or Spoked Pad Diameter: 300um, SRO 400um	CTF	118
■	MD or Spoked Pad Diameter: 300um, SRO 400um	NCTF	35
◆	MD or Spoked Pad Diameter: 300um, SRO 400um; SMD Pad Diameter: 400um, SRO: 300um	CTF	801
◀	MD or Spoked Pad Diameter: 300um, SRO 400um; SMD Pad Diameter: 400um, SRO: 300um	NCTF	14
▶	MD or Spoked Pad Diameter: 330um, SRO 430um;	CTF	15
▬	MD or Spoked Pad Diameter: 330um, SRO 430um;	NCTF	22
▀	MD or Spoked Pad Diameter: 330um, SRO 430um; SMD Pad Diameter: 430um, SRO: 330um	CTF	24
●	MD or Spoked Pad Diameter: 355um, SRO 455um	CTF	20
▲	MD or Spoked Pad Diameter: 355um, SRO 455um	NCTF	9
▼	MD or Spoked Pad Diameter: 355um, SRO 455um; SMD Pad Diameter: 455um, SRO: 355um	CTF	95
Total number of balls: 1449			

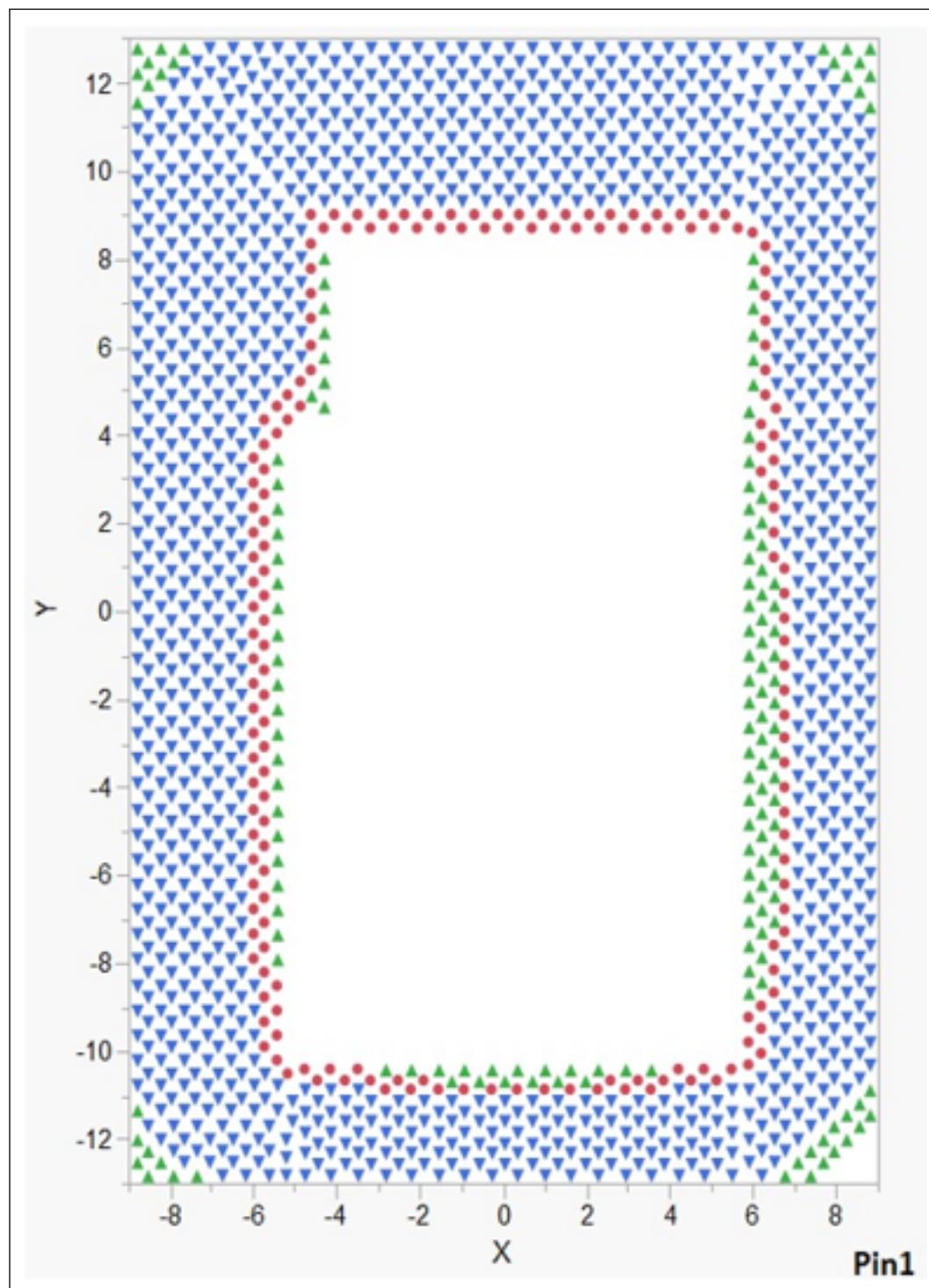
Figure 21. UP3 Corner NCTF Test- PCB Routing Example



## 2.2.4 Tiger Lake UP4 Land Pattern and Corner NCTF PCB Routing Guidance

Figure 22. UP4 Package Non-Critical to Function (NCTF) Overview



**Figure 23. UP4 Land Pattern Guidance**

Legend	Pad Size (microns/mils) ; SRO Size (microns/mils)	Function	# of Balls
●	MD or Spoked Pad : Pad 250um (10 mils), SRO 325um (13 mils)	CTF	172
▲	MD or Spoked Pad : Pad 250um (10 mils), SRO 325um (13 mils)	NCTF	153
▼	MD or Spoked Pad : Pad 250um (10 mils), SRO 325um (13 mils) SMD Pad : Pad 325um (13 mils), SRO 250um (10 mils)	CTF	1273

Total number of balls: 1598

Figure 24. UP4 Corner NCTF Test- PCB Routing Example

Corner DR67			Corner DR1		
Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
DR67	VSS	NCTF Testable Pins	DPS	VSS	NCTF Testable Pins
DR65	VSS	NCTF Testable Pins	DN4	VSS	NCTF Testable Pins
DP66	VSS	NCTF Testable Pins	DM2	VSS	NCTF Testable Pins
DN67	VSS	NCTF Testable Pins	DK1	VSS	NCTF Testable Pins
DR63	VSS	NCTF Testable Pins			
DP64	VSS	NCTF Testable Pins			
DN65	VSS	NCTF Testable Pins			
DM66	VSS	NCTF Testable Pins			
DK67	VSS	NCTF Testable Pins			

OPTIONAL: For corner NCTF SJ testability, these BGA pins (shown in the tables and in green color) can be connected to isolated motherboard test pads and not connected to motherboard VCC/VSS plane (refer to Figures 1 & 2 in MAS section 2.4). The disconnection is not a functional concern; however, it is desirable for the routing of the test pads to not cause a split in the planes.

Corner A67			Corner A1		
Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
D67	VSS	NCTF Testable Pins	C4	VSS	NCTF Testable Pins
C66	VSS	NCTF Testable Pins	F1	VSS	NCTF Testable Pins
B64	VSS	NCTF Testable Pins	C6	VSS	NCTF Testable Pins
A63	VSS	NCTF Testable Pins	F3	VSS	NCTF Testable Pins
A61	VSS	NCTF Testable Pins			
H67	VSS	NCTF Testable Pins			

● NCTF Package Corner  
● NCTF Testable Pins

Note: For pinlist and ballmap information, refer to the **Package Ballout Mechanical Specification** document for this specific product.

## 3.0 General Design Considerations

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### 3.1 Fiberweave Impact for HSIOs Operating at $\geq 8$ GT/s Speeds

Owing to negative signal integrity effects of fiberglass weave in the materials of which circuit boards are made, the Fiberweave impact to HSIO (High Speed I/O) running at  $\geq 8$  GT/s is significant, thus the need for mitigation to ensure robust system design.

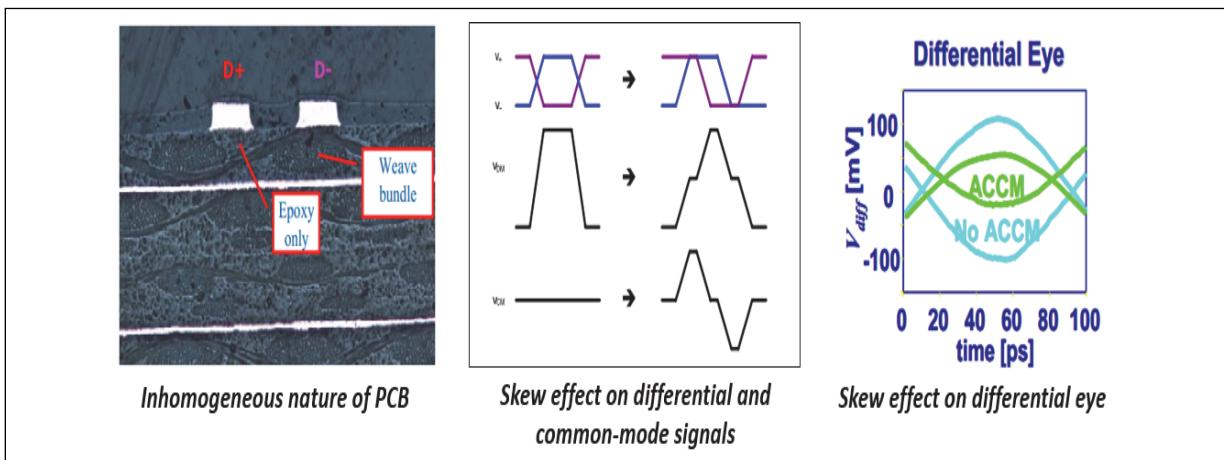
- The Fiberweave whitepaper (# 406926) discusses 17 options used to quantify the impact of Fiberweave and strategies studied to mitigate it.
- 10-degree PCB panel tilting is not the most cost-effective mitigation solution (among 17 options proposed), due to the low panel utilization and higher PCB cost.
- It is, therefore, Intel's advocacy for board routing efforts to address the cost concern. Examples of such routings, i.e. angled and zig-zag routing (minimum 10-degrees) are recommended.
- Customers are requested to prioritize floor planning on the board in such a way that the routing ends up being at an angle rather than orthogonal.

Tiger Lake SoC has Integrated Thunderbolt (TBT) controller, thus 20GT/s signal routing length can be as long as 205mm prior to connection to re-timer. Orthogonal routing with such length would result in adverse effect to channel margin, as described in Fiberweave White Paper (# 406926)

This is different from Cannon Lake platforms, where discrete TBT controllers are used. 20Gbps signal routing length from discrete controller to connector is only 38.1mm. Signal from SoC to re-timer is running at sub-10Gbps speed.

Impact to channel margin can be shown below. This is ascribed to the difference in propagation velocities leading to skew between D+ and D- signals, therefore resulting in an increased of common mode noise.

**Figure 25. Fiberweave Effects**



### 3.1.1 Maximum Parallel Routing Restrictions

For 20GT/s TBT4 signals, maximum allowable parallel RSS routing length is 12.7mm. Due to such restrictions, zig-zag or angled routing (both need minimum 10 degrees) is recommended.

Below Figure specifies the maximum allowed routing parallel to the board edge for each transfer rate. It is given as a "Root Sum Square" (RSS, root of the sums squared) value. The given maximum RSS length is based on the assumption that weave type of PCB construction is not specified. In the cases that specific weaves with better skew control are used, the maximum RSS length can be relaxed, but quantification of the benefit is beyond the scope of this document.

**Figure 26. Max Root Square Sum (RSS) Length versus Transfer Speed**

Transfer Speed	Max RSS length in mm (See note 1)
2.5 GT/s	127
4 GT/s	101.6
5 GT/s	76.2
6.4 GT/s	63.5
8 GT/s	50.8
10 GT/s	50.8
16 GT/s	25.4
20 GT/s	12.7

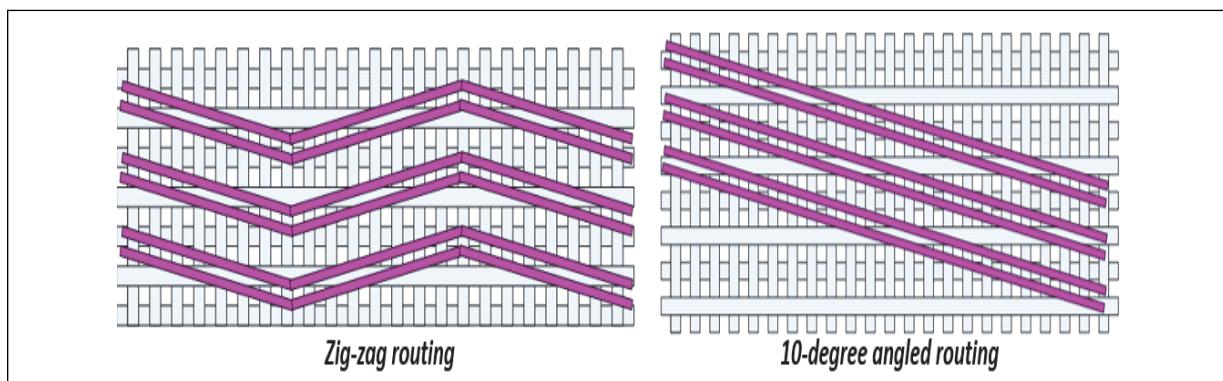
**Notes:**

- 1) The lengths in the table represent total trace lengths that are aligned to the weave (that is, parallel to the manufacturing panel's edge). Actual routing may have a significant portion of the length at angles to the edge of the board – those lengths should not be considered in this analysis.  
The total length is the Root Square Sum of total vertical and horizontal lengths that run parallel to the weave:  

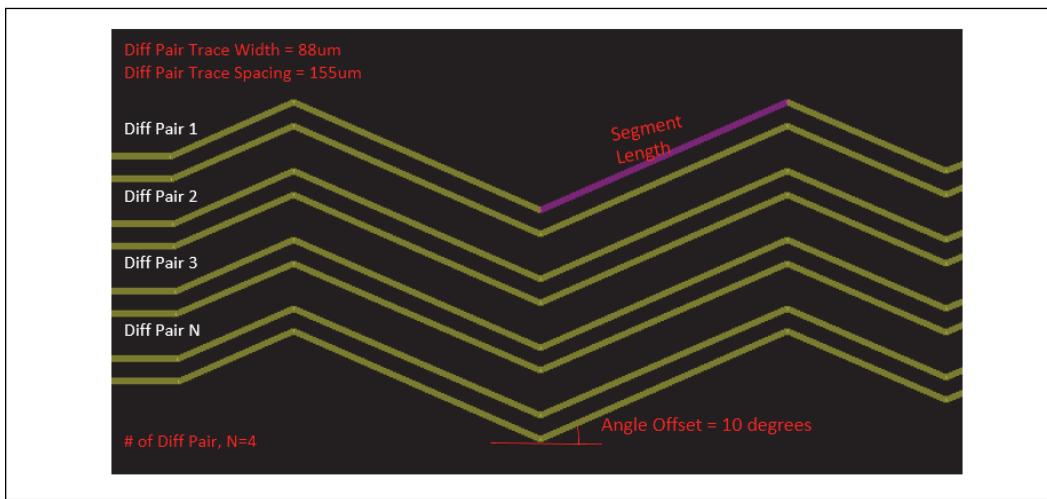
$$\text{Length} = \sqrt{(H_1)^2 + (H_2)^2 + (H_3)^2 + (V_1)^2 + (V_2)^2 + (V_3)^2 + \dots}$$
where:
  - a.  $H_X$  = length of each segment routed horizontally, and
  - b.  $V_X$  = length of each segment routed vertically
- 2) The table represents an approximation only, based on simulations of "representative" topology. The exact fiber weave may vary, depending on the exact topology.

### 3.1.2 Recommended Routing Guidelines

- Zig-zag or angled routing (both need minimum 10 degrees) is recommended after allowable RSS length.
- For angled routing, total length increases with angle of the segment.
- Customers are required to check their glass fabric material used related to weave pitch. Segment trace length needed to cross 2 weave bundles along its length.
- Each segment length can be independent segments of length.

**Figure 27. Recommended Routing Illustrations**

**Figure 28. Zig-zag Routing Layout Example**



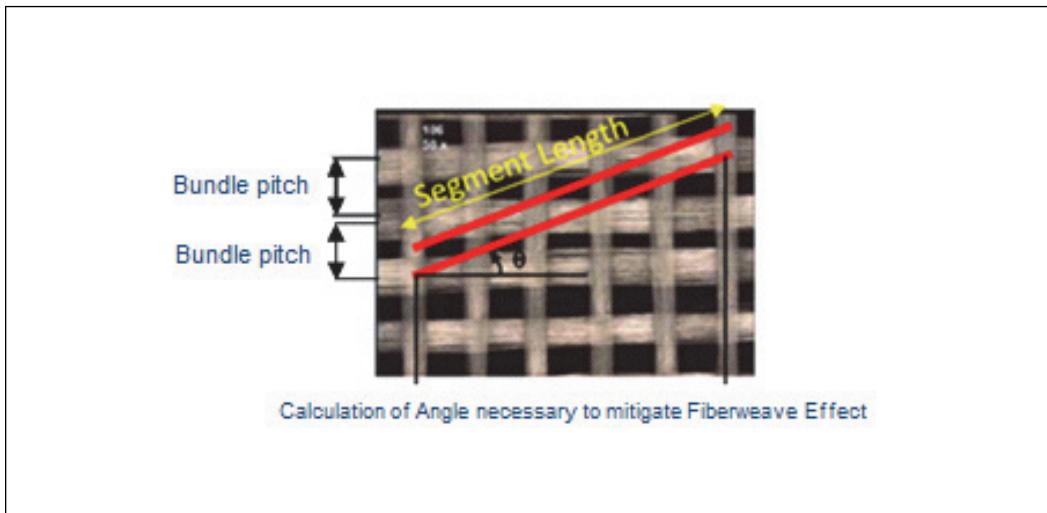
#### NOTES

1. 10-degree routing angle: Length increases ~1-2%.
2. 20-degree routing angle: Length increases ~6%.

### 3.1.3 Zig-zag Segment Length Calculation Example For Improving Fabric

Customers can interchange the glass fabric with the same thickness for reduced Fiberweave effect. E.g., from 2113 to 2313, 1080 to 1078\1086, 106 to 1067. Work directly with your PCB vendor to evaluate options.

**Figure 29. Calculation of Angle Necessary to Mitigate Fiberweave Effect**



#### Typical case glass fabric material 106:

Fiber bundle pitch: 469.9um

2X pitch: 939.8um

Zig-zag segment length to cross 2 pitches calculated as:

$$\text{Segment Length} = 2 \times \text{pitch} / \sin \theta = 939.8 / \sin 10^\circ = 5412\text{um}$$

#### **Replacement glass fabric material 1067:**

Fiber bundle pitch : 363.2um

2X pitch: 726.4um

Zig-zag segment length to cross 2 pitches calculated as:

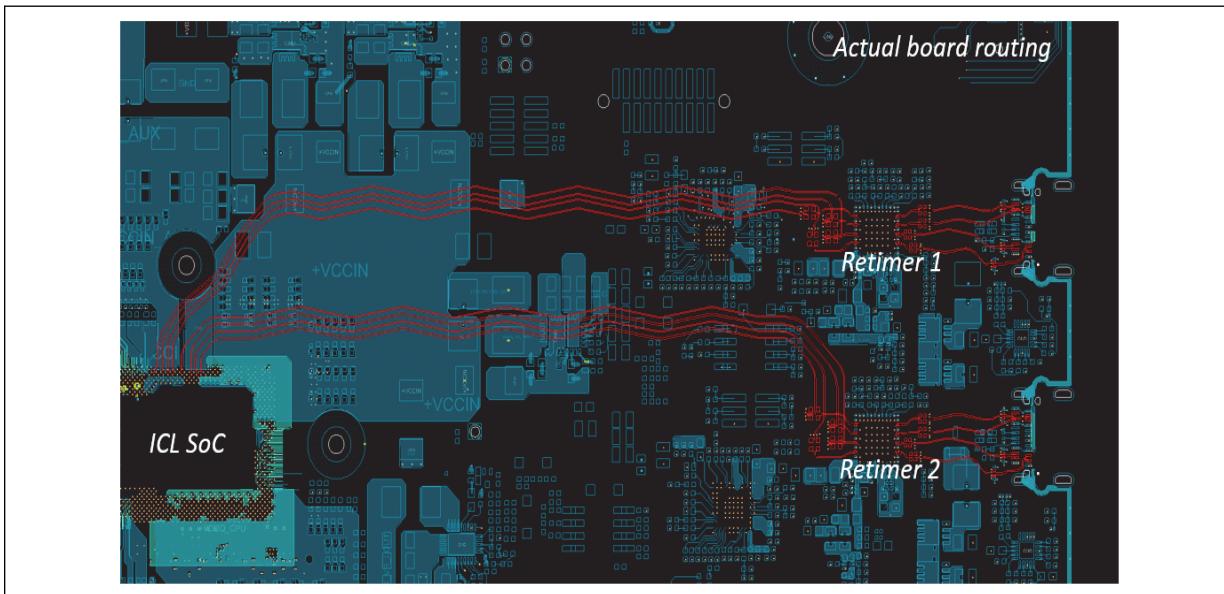
$$\text{Segment Length} = 2 \times \text{pitch} / \sin \theta = 726.4 / \sin 10^\circ = 4183\text{um}$$

In this example calculation, 1067 glass fabric has a much finer fiber bundle pitch than 106. This helps reduce the overall trace length adder from using zig-zag or angled routing at a minimum of 10 degrees.

#### **Example Layout Implementation**

Below is an example of which zig-zag routing is implemented in Intel reference design

**Figure 30. Layout Implementation Example**



## 3.2

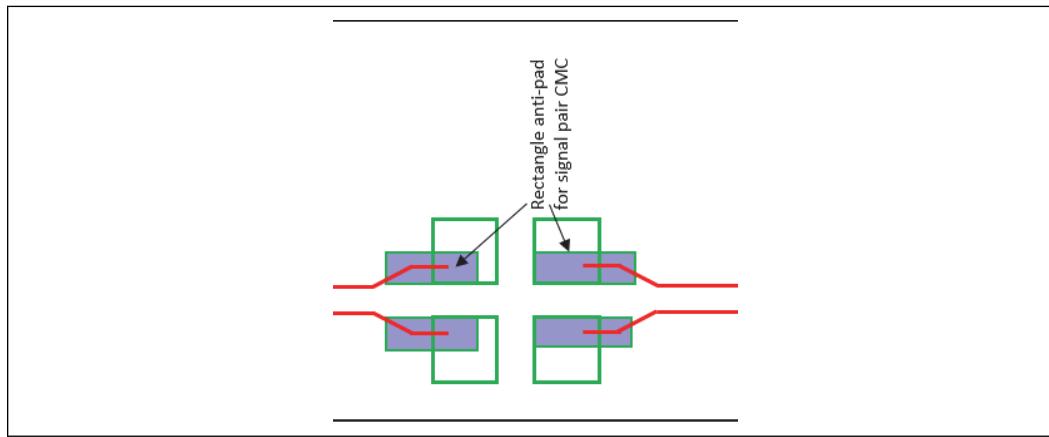
### **Component Footprint Plane Voiding Recommendation**

Voiding the Ground/Power plane on the layer directly underneath SMT signal pads is necessary to minimize impedance mismatch caused by the SMT pads. This is recommended for large SMT pads of components such as ESD protection devices, Common Mode Chokes (CMC) and connectors. In general, the reference plane should be voided with the same size as the SMT pad. Voiding is only required on the layer directly underneath SMT signal pads and not required on any other internal layers.

Voiding is not required for small component pads such as 0402 components and AC capacitors (unless explicitly mentioned for certain high-speed IO such as Thunderbolt and PCIe4).

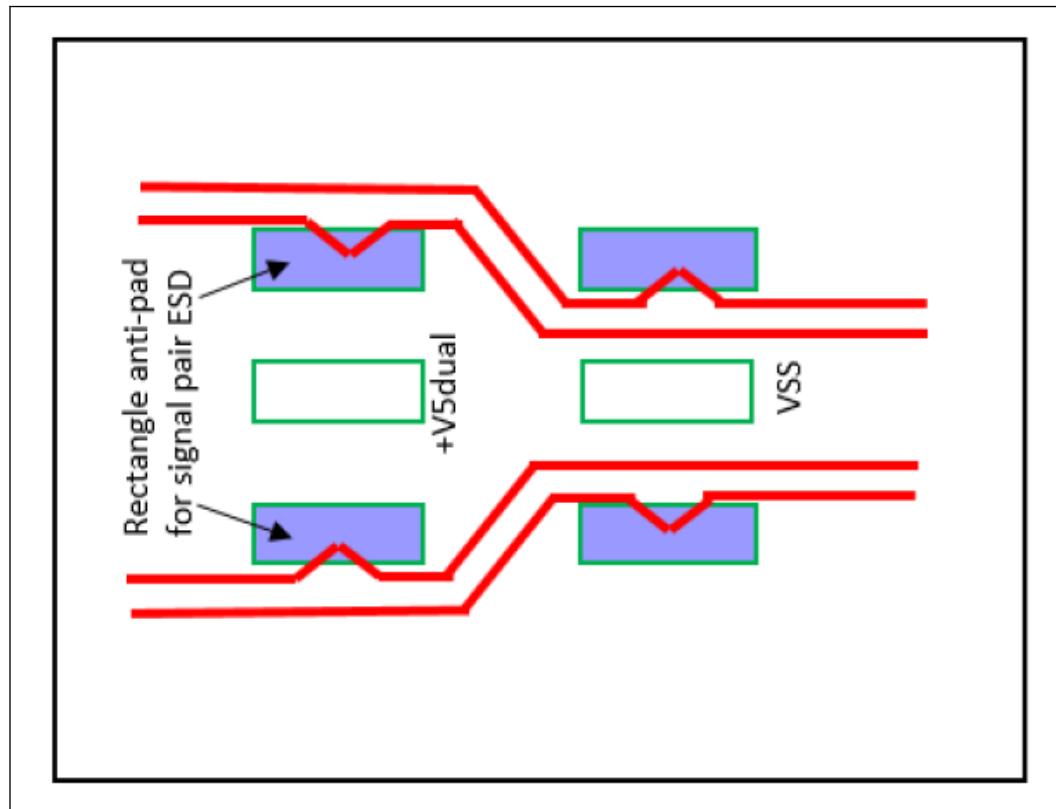
### 3.2.1 USB 2.0/3.X/4 SMT Common-mode Choke Footprint and Ground Plane

**Figure 31. USB2.0, USB 3.X and USB 4 Common-mode Choke (CMC) Voiding Recommendation**



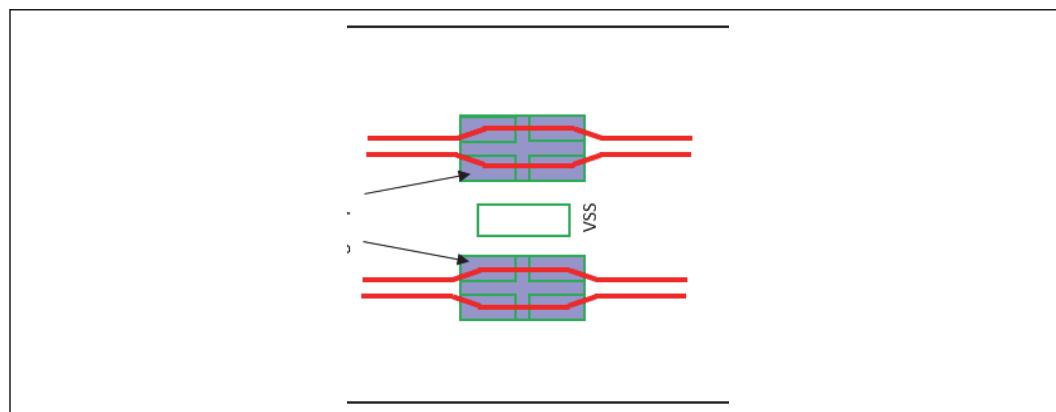
### 3.2.2 USB2.0 SMT Electrostatic Diode Footprint, Power and Ground Plane

Figure 32. USB2.0 Electrostatic Diode (ESD) Voiding Recommendation



### 3.2.3 USB3.X SMT Electrostatic Diode Footprint, Power and Ground Plane

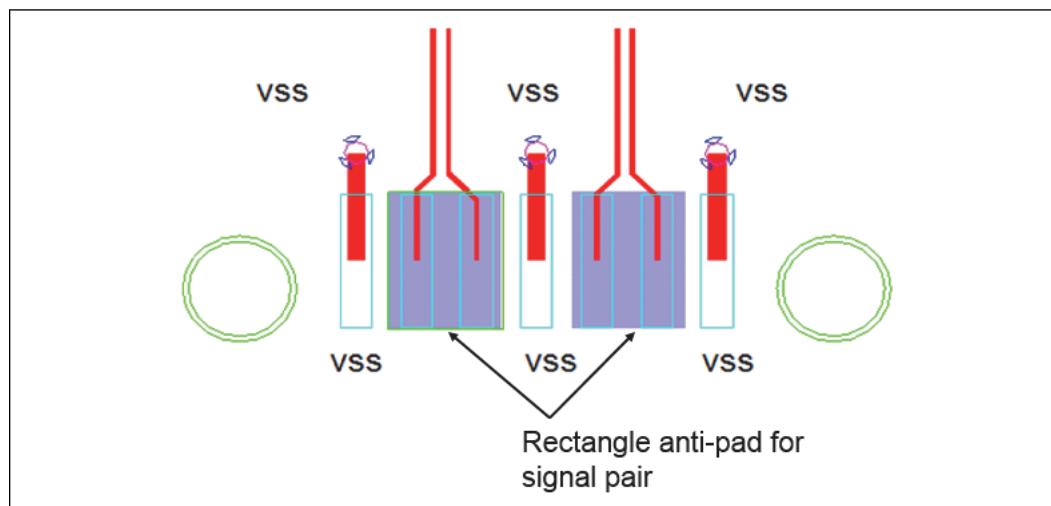
Figure 33. USB3.X Electrostatic Diode (ESD) Voiding Recommendation



### 3.2.4 SATA Connector Footprint Voiding

The shaded areas shown in the Figure below (rectangle shape anti-pad) illustrate the GND/power plane under the SMT pads have been voided.

**Figure 34. SATA 6 Gb/s SMT Connector Footprint, Power and Ground Plane**

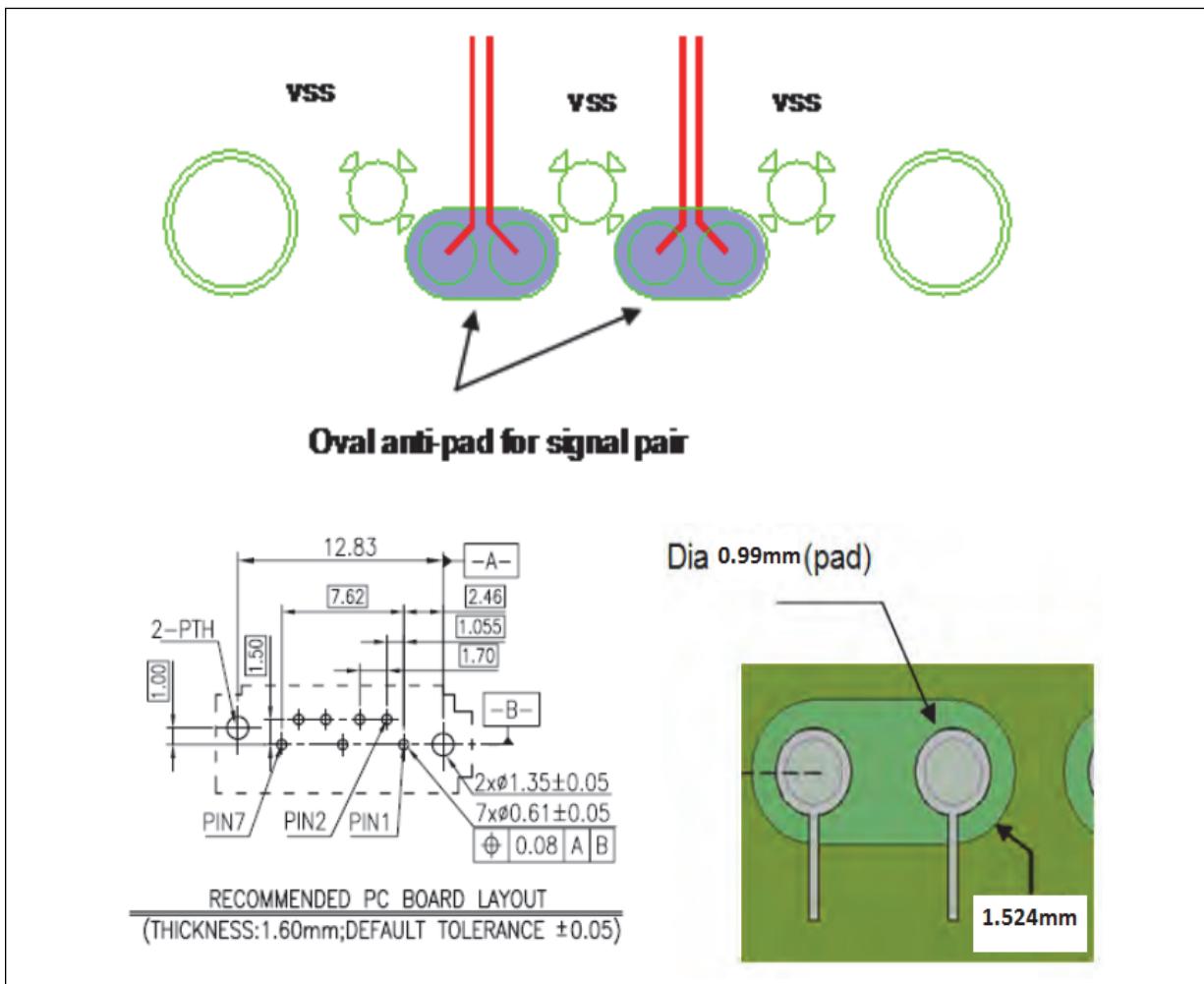


#### PCH Differential Through-Hole Connector Footprint Recommendations

Figure below shows the recommended 7-pin through-hole SATA 6 Gb/s connector footprint, as well as the pad and anti-pad dimension. The following points should be noted about the through-hole connector footprint:

- The SATA 6 Gb/s connector footprint is different from the one for the existing SATA Gen 2x1 (10 Gb/s) connector. This is done to ensure that high performance SATA connectors are used with the SATA 6 Gb/s interface.
- The through-hole, pad, and anti-pad sizes are chosen to prevent the through-hole impedance from being too low. The finished through-hole diameter is 0.61 mm; the pad diameter is 0.99 mm; and the anti-pad diameter is 1.52 mm.
- The oval shape anti-pad (GND void), shown in figure below, should be used to reduce the through-hole capacitance when the traces enter the connector on the top of the PCB (maximum through-hole stub length). However, when the traces enter the connector on the bottom of the PCB (minimum through-hole stub length), the regular circular anti-pad or diameter of 1.524mm should be used.

**Figure 35. SATA 6 Gb/s Through-hole Connector Footprint, Pad/Anti-pad Size**



#### SATA 6 Gb/s Surface-Mount Connector Footprint Recommendations

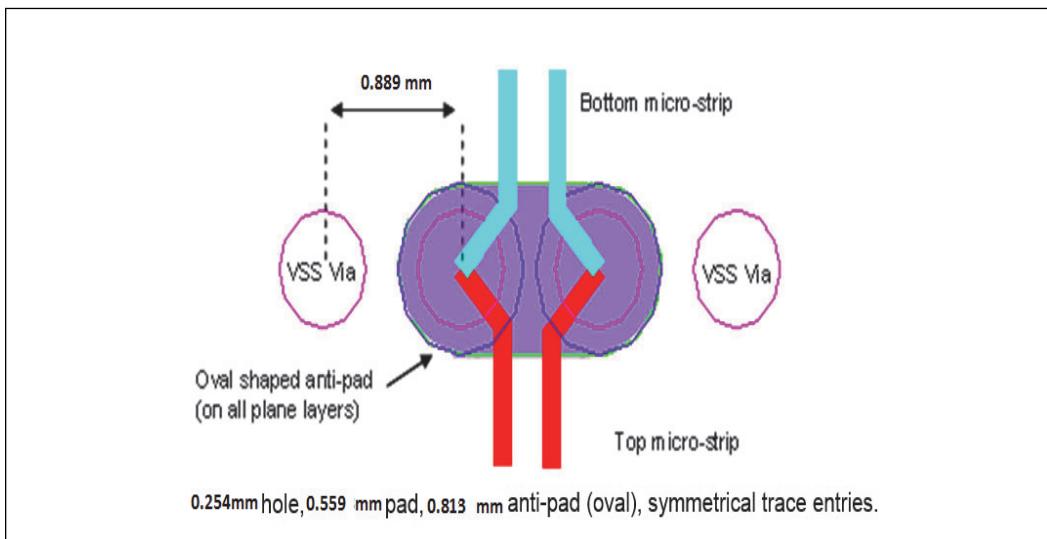
The SATA 6 Gb/s surface-mount (SMT) connector footprint may have the same footprint as the SATA Gen 2x1 (10 Gb/s) connector, but voiding the Ground/Power plane underneath the SMT signal pads is necessary to minimize the impedance mismatch caused by the SMT pads. The shaded areas shown in the Figure 34 on page 58, illustrate the GND/power plane under the SMT pads that have been voided.

### 3.3

#### Differential Transitional Via Recommendations

Transitional vias will use oval-shapes anti-pads on all plane layers. This can be created using a rectangular-shaped void to overlap with the usual round-shaped via anti-pad. The vias must also have a symmetrical trace entry. Furthermore, Vss stitching vias must be placed at a symmetrical distance to the signal vias and must connect the reference planes above and below the incoming and outgoing traces.

Figure and Table below provides the transitional differential via pad stack details.

**Figure 36. Differential Transitional Via Layout**

**Table 6. Differential Transitional Via Layout Recommendations**

Parameter	Units	Recommendation
Via Diameter	mm	0.254
Via Pad Size	mm	0.559
Oval-Shaped Anti-Pad Size	mm	0.813
Via-to-via Distance (centered)	mm	0.889

### 3.4 General Dual-Stripline Support

In cases where high speed differential signals are routed in an 8- or 10- layer dual-stripline stack-up, follow the guidelines in table below. Figure below illustrates the meaning of Tx-over-Tx, Rx-over-Rx, and Tx-over-Rx.

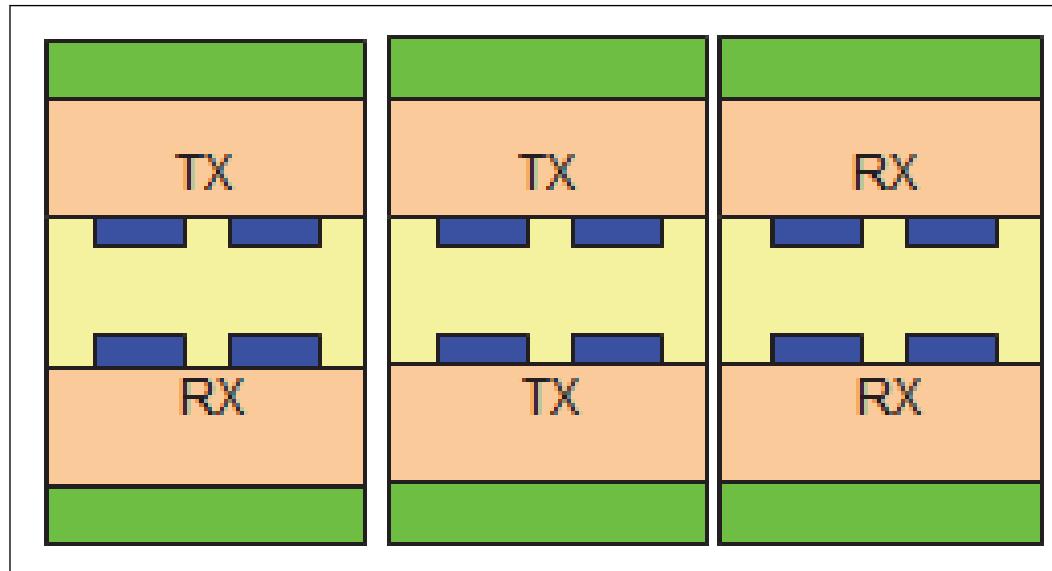
For additional details and recommendations regarding dual-stripline routing, refer to Dual Stripline Crosstalk Behavior and Cross-Interface Coupling technical white paper (#575518).

**Table 7. General Dual-Stripline Support**

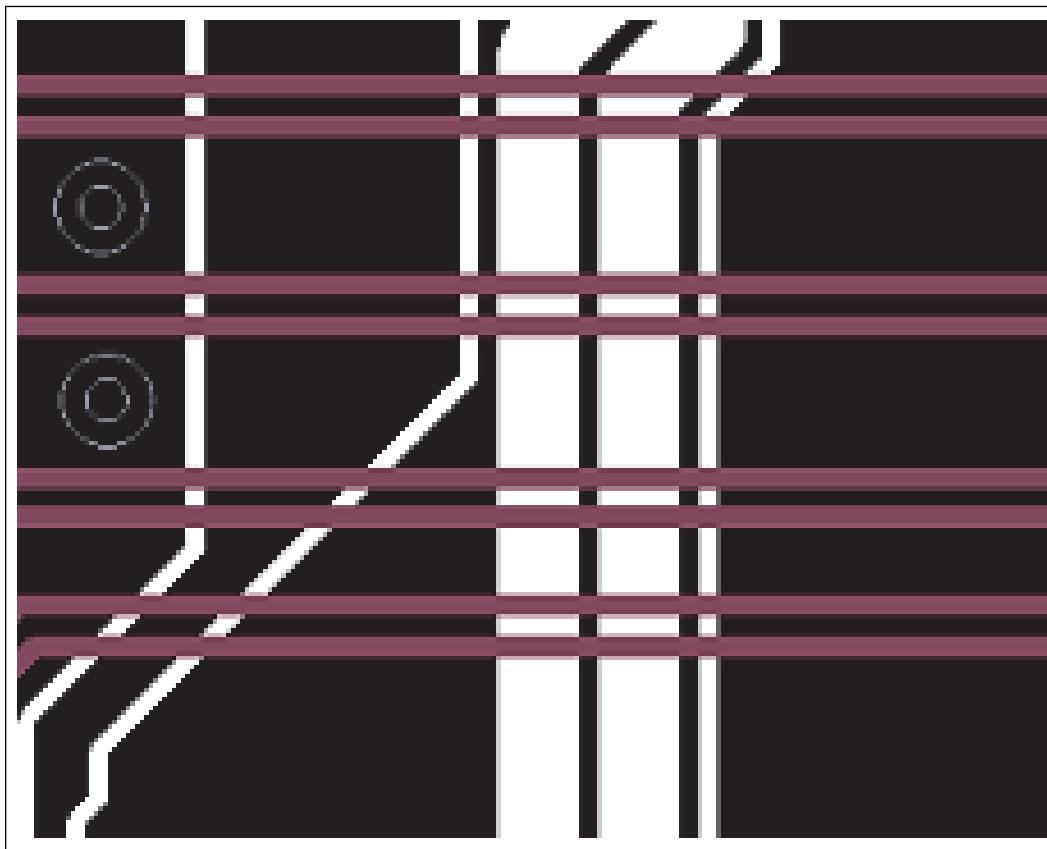
Tx -over-Rx Parallel Routing	Tx-over-Tx or Rx-over-Rx Parallel Routing	Tx-over-Rx or Tx-over-Tx or Rx-over-Rx Routing Orthogonal or with Angle
<ul style="list-style-type: none"> <li>For CPU HSIOs, parallel routing is allowed if the offset is at least equal to the Signal-to-Non Equivalent-Signal spacing defined in the Tline specification sheet (attached with the PDG).</li> <li>For other IOs, route with an offset of 0.381mm or greater</li> </ul>	<ul style="list-style-type: none"> <li>For CPU HSIOs, parallel routing is allowed if the offset is at least equal to the Signal-to-Equivalent-Signal spacing defined in the Tline specification sheet (attached with the PDG)</li> <li>For other IOs, a maximum of 50.8mm of parallel routing is allowed</li> </ul>	<ul style="list-style-type: none"> <li>Routing at an angle of at least 30 degrees significantly reduces layer-to-layer crosstalk.</li> <li>Route differential pairs at a 30,45, 60, 90 etc degree angle.</li> <li>Allow maximum of 10 aggressor pairs to route over 1 DSL routing victim pair.</li> <li><a href="#">Figure 38</a> on page 62 shows orthogonal routing.</li> <li><a href="#">Figure 39</a> on page 62 shows angled routing at less than 90 degrees.</li> </ul>

**NOTE**

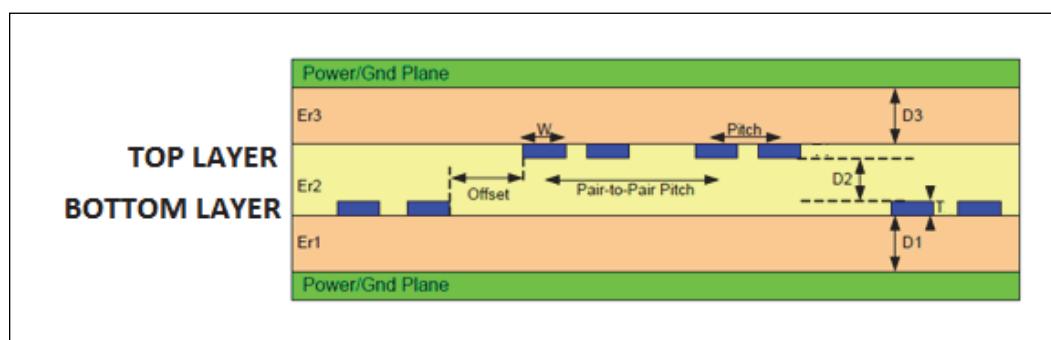
Signal-to-Equivalent-Signal: Same interface AND direction of propagation AND swing.  
Signal-to-Non Equivalent-Signal: Different interface OR direction of propagation OR swing.

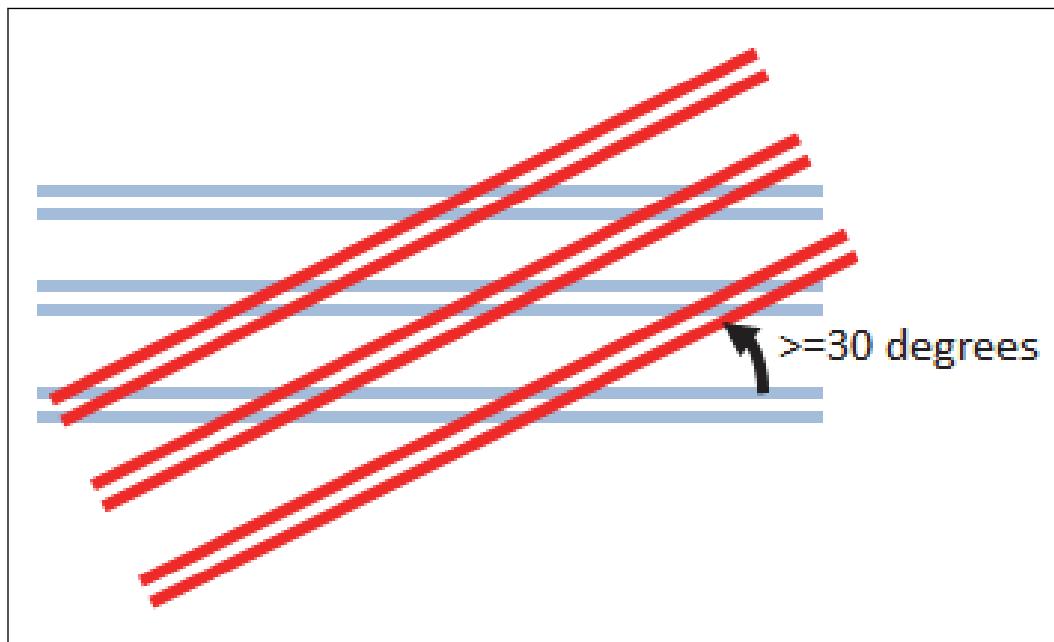
**Figure 37. Tx-over-Tx, Rx-over-Rx, and Tx-over-Rx**

**Figure 38. Dual-Stripline Orthogonal Routing Recommendation**



**Figure 39. Dual-Stripline High Speed Signal Dual Layer Routing Recommendation**



**Figure 40. Recommended Routing Angle to Reduce Layer-to-Layer Crosstalk**

### 3.5

### Trace Length Matching Requirements

Follow the specific interface length matching guidelines if provided. If not provided, use the following as a general guideline.

**Table 8.****General Differential Pair Length Matching**

Description	Routing Recommendation (mm)
Within Layer Max Mismatch	0.254
Total Length Max Mismatch	0.127

*Note:* Preferred to keep both 'within layer' mismatches and 'total length' mismatches within 0.127mm.

### 3.6

### General Differential Routing Guidelines

Do not route traces under power connectors, other interface connectors, inductors, crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks. To minimize reflection, do not place stubs, test points, test vias on the route. Use vias and connector pads as test points instead. If a stub is unavoidable in the design, the total stub lengths on the particular trace should not be greater than 5.08 mm.

- It can be helpful for testability to route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
- Keep signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.

## 4.0 System Memory Interface Design Guidelines

The Tiger Lake platform supports multiple memory technologies. This chapter covers the guidelines to design an Tiger Lake platform with the following **Plan of Record (POR)** supported system memory interface configurations and features.

### NOTE

For complete Tiger Lake processor system memory interface POR feature support details refer the latest release of the Tiger Lake Processor External Design Specification (EDS).

## 4.1 POR Memory Configurations

Platform	Config#	Transfer rate (MT/s)	Topology	Memory Device	Device Ballout	PCB Stack-up	IL/NIL
TGL UP4 LPDDR4x x64	4.2.1	4266	1R x64 2R x64 Single Sided	QDP (4 x 16 die) ODP (8 x16 die)	556	Type-4 10L (Any layer)	NIL
TGL UP3 LPDDR4x x32	4.2.2	4266	1R x32, 2R x32 Single Sided	DDP (2 x 16 die) QDP (4 x 16 die) ODP (8 x 16 die)	200	Type-4 8L (1-x-1+)	NIL
TGL UP3 DDR4	4.4.1	3200	SoDIMM SBS/B2B channel Single Sided	A(1Rx8) C(1Rx16) E(2Rx8)	260	Type-3/8L	NIL
	4.4.2	3200	MD 1R x8 Daisy Chain SBS/B2B channel Single/dual Sided	SDP (1 x 8 die) 1R, 4 Bank Groups, 4Banks	78	Type-3/10L	NIL
	4.4.3	3200	MD 1R x16 Daisy Chain SBS/B2B channel Single/dual Sided	SDP (1 x 16 die), DDP (2 x 8 die) 1R, 2 Bank Groups, 4Banks	96	Type-3 /10L	NIL
	4.4.4	3200	Mixed SoDIMM and MDx16 (4 DRAMs per channel) SBS/B2B channel	MDx16: SDP (1 x 16 die) DDP (2 X 8 die) 1R, 2 Bank Groups, 4Banks <u>SODIMM:</u>	MDx16: 96 <u>SODIMM:</u> 260	Type-3 /8L	NIL

*continued...*

Platform	Config#	Transfer rate (MT/s)	Topology	Memory Device	Device Ballout	PCB Stack-up	IL/NIL
			Single/dual Sided	A(1Rx8),C(1Rx16),E(2Rx8)			
	4.4.5	3200	Mixed SoDIMM and MDx8 (8 DRAMs per channel) SBS/B2B channel Single/dual Sided	MDx8: SDP (1 x 8 die) 1R,4 Bank Groups, 4Banks SODIMM: A(1Rx8),C(1Rx16),E(2Rx8)	MDx16: 78 SODIMM: 260	Type-3 /8L	NIL

Notes:

- 1. NIL - Non-interleave ballmap
- 2. IL - Interleave ballmap (Not supported at TGL UP3/UP4)
- 3. SBS - Side by side, DIMMs placed is side by side, in line placement.
- 4. B2B - Back to Back, DIMMs placed in parallel one to other.
- 5. SDP: Single Die Package, DDP: Dual Die Package , QDP: Quad Die Package, ODP: Octal Die Package



TGL Processor and Memory Type	TGL UP3	TGL UP3 and TGL UP4
	DDR4 SODIMM and Memory Down (per Channel)	LPDDR4x Memory Down (All channels)
<b>Signal details</b>		
Clock (CLK)	DDR[1:0]_CLK_P[1:0], DDR[1:0]_CLK_N[1:0]	DDR[7:0]_CLK_N DDR[7:0]_CLK_P
Control (CTRL)	DDR[1:0]_CS[1:0], DDR[1:0]_ODT[1:0]	DDR[7:0]_CS[1:0]
Clock Enable (CKE)	DDR[1:0]_CKE[1:0]	DDR[7:0]_CKE[1:0]
Command (CMD)	DDR[1:0]_MA[16:0], DDR[1:0]_BG[1:0], DDR[1:0]_BA[1:0], DDR[1:0]_ACT#, DDR[1:0]_PAR	DDR[7:0]_CA[5:0]
Alert	DDR[1:0]_ALERT#	N/A
Strobe	DDR[1:0]_DQSN[7:0] DDR[1:0]_DQSP[7:0]	DDR[7:0]_DQSN[1:0] DDR[7:0]_DQSP[1:0]
Data	DDR[1:0]_DQ[7:0][7:0]	DDR[7:0]_DQ[1:0][7:0]
Reset	DRAM_RESET#	DRAM_RESET#
RCOMP	DDR_RCOMP	DDR_RCOMP
Vref	DDR[1:0]_VREF_CA	N/A
VTT	DDR_VTT_CTL	N/A
<b>Guideline Terminology Descriptions</b>		
Diff Spacing	Differential spacing between CK and CK# and between DQS and DQS#	
Within Group Spacing	Min self spacing and spacing between signals within the same signal group	
Group to Group Spacing	Min spacing between signals from the following different signal groups: [1] CLK-CLK [2] CMD-CMD, CMD-CTRL, CMD-CKE, CTRL-CTRL, CTRL-CKE, CKE-CKE	

continued...

TGL Processor and Memory Type	TGL UP3	TGL UP3 and TGL UP4
	DDR4 SODIMM and Memory Down (per Channel)	LPDDR4x Memory Down (All channels)
	[3] Data-Data, Strobe-Strobe, WCK-WCK, RCOMP-RCOMP, Reset-Reset	
Byte to Byte Spacing	Min spacing between bytes within the same channel	
DQS pair to DQ spacing	Min spacing between strobe and data group signals within the same byte	
DDR to Other signals/interfaces	Minimum required spacing to other signals/interfaces is 0.635 mm.	
DDR Trace impedance and trace geometries	Impedance numbers are calculated according to the stack-up layers thickness, the material conductivity, traces spacing, width, dielectric constant and thickness. The controlling specification is the target trace impedance. It is allowed to change the signal trace width within design tolerance. It is strictly not recommended to reduce spacing between signals. Any spacing reduction can cause to performance degradation.	
Type-3/Type-4	Type-3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias. Type-4 (T4) (1-x-1+) = PCB with one build-up layer and two layers of Micro-vias. Type-4 (T4) (3-x-3+) = PCB with three build-up layer and four layers of Micro-vias. Refer PCB Stack-Up and Design Considerations.	
Non-Interleave	Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-by-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.	
ODT Capability	The DRAM Device ODT Capability can be enabled or disabled dynamically through the MRC for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins.	

## 4.2 LPDDR4x Memory Down Topologies

This section describes the following topologies

- UP3 LPDDR4x x32 Type-4
- UP4 LPDDR4x x64 Type-4

### 4.2.1 Tiger Lake UP3 LPDDR4x x32 Type-4

**Table 9. System Memory Configuration Details Covered in this Section**

Parameter	Details
Processor	TGL UP3 42
Memory Type	LPDDR4x
Speed (MT/s)	DDP, QDP, ODP - 4266
Channels	Channels: 0-7
Population Rules	<u>1 Dram</u> - N/A <u>2 Drams</u> - DRAM 0 is connected to channel 0 and 1 <sup>6</sup> DRAM 1 is connected to channel 2 and 3 <sup>6</sup> <u>3 Drams</u> - N/A <u>4 Drams</u> -

*continued...*

Parameter	Details
	DRAM 0 is connected to channel 0 and 1 DRAM 1 is connected to channel 2 and 3 DRAM 2 is connected to channel 4 and 5 DRAM 3 is connected to channel 6 and 7
System Memory Voltage	LPDDR4x Processor VDD2 is 1.1v. LPDDR4x DRAM VDDQ voltage is 0.6v, VDD2 is 1.1v
Max Ranks Per Channel	2
DRAM Die Density (Gb)	8, 16
Max Capacity (GB)	8Gb die-32GB 16Gb die-32GB <sup>8</sup>
Memory Down Types <sup>1,2</sup> (Pkg Ranks - Die Bits - Pkg bits)	200 balls DDP:1-16-32 QDP:2-16-32 ODP:2-8-32 (byte mode) <sup>7</sup>
PCB Layers / Type <sup>3</sup>	TGL UP3: Type-4 8L (1-x-1+)
DRAM Device Placement	Top Motherboard Layer, Single Sided, Side by Side Placement
Processor Memory Ball Map <sup>4</sup>	Non-Interleaved
DRAM Device ODT Capability <sup>5,6</sup>	MRC trained
<p>Notes:</p> <ol style="list-style-type: none"> <li>1. DDP: Dual Die Package, QDP: Quad Die Package, ODP: Octal Die Package</li> <li>2. No mixed vendor support within a channel or channel to channel and No mixed memory DRAM down type support (SDP, DDP, QDP) within a channel or channel to channel</li> <li>3. Type-4 (T4) (1-x-1+) = PCB with one build-up layer and x layers of Micro-vias. Refer "Stack-Up and PCB Considerations" chapter for more details in this document.</li> <li>4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices placement. Each memory channel's signals are grouped together on one side of the processor packages.</li> <li>5. The DRAM Device ODT will be trained by the MRC.</li> <li>6. For LPDDR4x, to avoid excessive latency due to ZQ topology, Intel specifies that each ZQ pin must have a unique ZQ resistor.</li> <li>7. 16Gb ODP 2-16-32 pending sample availability.</li> <li>8. 16Gb die-64GB Pending DRAM samples availability.</li> </ol>	

#### 4.2.2 Tiger Lake UP4 LPDDR4x x64 Type-4

**Table 10. System Memory Configuration Details Covered in this Section**

Parameter	Details
Processor	TGL UP4 4+2
Memory Type	LPDDR4x
Speed (MT/s)	QDP ,ODP- 4266
Channels	Channels: 0-7
Population Rules	<u>1 Dram</u> - DRAM 0 is connected to channels 0,1,2 and 3 <sup>6</sup> <u>2 Drams</u> - DRAM 0 is connected to channels 0,1,2 and 3 DRAM 1 is connected to channels 4,5,6 and 7
System Memory Voltage	LPDDR4x Processor VDD2 is 1.1v.

*continued...*

Parameter	Details
	LPDDR4x DRAM VDDQ is 0.6v, VDD2 is 1.1v
Max Ranks Per Channel	2
DRAM Die Density (Gb)	8, 16
Max Capacity Per System(GB) <sup>7</sup>	8 die-16GB 16 die-16GB
Memory Down Types <sup>1,2</sup> (Pkg Ranks - Die Bits - Pkg bits)	556 balls QDP:1-16-64 ODP:2-16-64
PCB Layers / Type <sup>3</sup>	TGL UP4: Type-4 10L (Any Layer)
DRAM Device Placement	Top Motherboard Layer, Single Sided, Side by Side Placement
Processor Memory Ball Map <sup>4</sup>	Non-Interleaved
DRAM Device ODT Capability <sup>5,6</sup>	MRC trained
Notes:	
1. QDP: Quad Die Package, ODP :Octal Die Package	
2. No mixed vendor support within a channel or channel to channel and No mixed memory DRAM down type support (SDP, DDP, QDP) within a channel or channel to channel	
3. Type-4 (T4) (3-x-3+) = PCB with three build-up layers and x layers of Micro-vias. Refer "Stack-Up and PCB Considerations" chapter for more details in this document.	
4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices placement. Each memory channel's signals are grouped together on one side of the processor packages.	
5. The DRAM Device ODT will be trained by the MRC.	
6. For LPDDR4x, to avoid excessive latency due to ZQ topology, Intel specifies that each ZQ pin must have a unique ZQ resistor.	
7. Maximum system capacity refers to system with all 8 sub-channels populated.	

## 4.3

### DDR4 Topologies

This section describes the following topologies

- UP3 DDR4 SODIMM Type3
- UP3 DDR4 1Rx8 Daisy-Chain
- UP3 DDR4 1Rx16
- UP3 DDR4 Mixed SODIMM and Memory Down x16
- UP3 DDR4 Mixed SODIMM and Memory Down x8

#### 4.3.1

##### Tiger Lake UP3 DDR4 SODIMM Type3

**Table 11. Tiger Lake UP3 DDR4 SODIMM Type-3/8L Topology Guidelines**

Parameter	Details
Processor	TGL UP3 4+2
Memory Type	DDR4
Configuration	Channel A = One SODIMM Channel B = One SODIMM
Speed (MT/s)	3200
<i>continued...</i>	

Parameter	Details
Channels	1 and 2
System Memory Voltage	1.2V
Max Ranks Per Channel	2
DRAM Die Density (Gb)	8,16
Max Capacity (GB)	64
Memory Types	RC-A (1Rx8), RC-C(1Rx16), RC-E (2Rx8)
PCB Layers / Type <sup>1</sup>	Type-3/8L
DRAM Device Placement	Board can be single sided or dual sided, Channels are Side by Side or Back to Back Placement
Processor Memory Ball Map <sup>2</sup>	Non-Interleaved
DRAM Device ODT Capability <sup>3</sup>	Enabled

Notes: 1. Type-3 (T3)= PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias.  
 2. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices placement. Each memory channel's signals are grouped together on one side of the processor packages.  
 3. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to [Table 16](#) on page 73

#### 4.3.2 Tiger Lake UP3 DDR4 1Rx8 Daisy-Chain Topology Memory Down Guidelines

1Rx means it is a single rank module and 2Rx means it is a dual-rank module module. Rank is a data block which is 64 bits wide without Error Correction Code (ECC) created using some, or all of the memory chips on a module. The 8 in them specifies the number of banks in the memory module. Higher the number of banks, the fewer the chips in the memory module, the better the reliability and power consumption.

**Table 12. System Memory Configuration Details Covered in this Section**

Parameter	Details
Processor	TGL UP3 4+2
Memory Type	DDR4
Configuration	Channel A = x8 Memory Down (8 DRAM Devices for 1 Rank) Channel B = x8 Memory Down (8 DRAM Devices for 1 Rank)
Speed (MT/s)	3200
Channels	1 and 2
System Memory Voltage	1.2V
Max Ranks Per Channel	1
DRAM Die Density (Gb)	8,16
Max Capacity (GB)	32
Memory Down Types <sup>1,2</sup> (Pkg Ranks - Die Bits - Pkg bits)	78-Ball BGA SDP 1-8-8
PCB Layers / Type <sup>3</sup>	Type-3/8L
CPU System Memory Ball Map <sup>4</sup>	Non-Interleaved for Side by Side (Inline) Placement
DRAM Device Placement	Each Channel is single sided or dual sided,

*continued...*

Parameter	Details
	Channels are Side by Side or Back to Back Placement
DRAM Device ODT Capability <sup>5</sup>	Enabled
<p>Notes:</p> <ol style="list-style-type: none"> <li>1. SDP: Single Die Package</li> <li>2. No mixed vendor support within a channel or channel to channel and No mixed memory DRAM down type support within a channel or channel to channel</li> <li>3. Type-3 = PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias. Refer "Stack-Up and PCB Considerations" chapter for more details.</li> <li>4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or <b>DIMM Side-By-Side (inline)</b> placement. Each memory channel's signals are grouped together on one side of the processor packages.</li> <li>5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to <a href="#">Table 16</a> on page 73.</li> </ol>	

### 4.3.3

### Tiger Lake UP3 DDR4 1Rx16 Memory Down Guidelines

**Table 13.**

**System Memory Configuration Details Covered in this Section**

Parameter	Details
Processor	TGL UP3 4+2
Memory Type	DDR4
Configuration	One Channel = x16 Memory Down (4 DRAM Devices) One Channel = x16 Memory Down (4 DRAM Devices)
Speed (MT/s)	3200
Channels	1 and 2
System Memory Voltage	1.2V
Max Ranks Per Channel	1
DRAM Die Density (Gb)	8,16
Max Capacity (GB)	SDP: 16 DDP: 32
Memory Down Types <sup>1,2</sup> (Pkg Ranks - Die Bits - Pkg bits)	96-Ball BGA SDP 1-16-16 DDP 1-8-16 <sup>6</sup>
PCB Layers / Type <sup>3</sup>	Type-3/8L
DRAM Device Placement	Each channel is single sided or dual sided Channels are Side by Side or Back-to-Back Placement

*continued...*

Parameter	Details
CPU System Memory Ball Map <sup>4</sup>	Non-Interleaved
DRAM Device ODT Capability <sup>5</sup>	Enabled
<p>Notes:</p> <ol style="list-style-type: none"> <li>1. SDP: Single Die Package, DDP: Dual Die Package</li> <li>2. No mixed vendor support within a channel or channel to channel and No mixed memory DRAM down type support (SDP, DDP) within a channel or channel to channel</li> <li>3. Type-3 = PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias. Refer "Stack-Up and PCB Considerations" chapter for more details.</li> <li>4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-By-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages. Interleave = the processor is optimized for a back-to-back ball map and placement of the DIMMs. Each memory channel's signals are grouped together on front or back side of the processor packages.</li> <li>5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to <a href="#">Table 16 on page 73</a></li> <li>6. For BG1 compatibility across SDP and DDP x16 devices, please refer to the excel sheet portion of the PDG</li> </ol>	

#### 4.3.4 Tiger Lake UP3 DDR4 Mixed SODIMM and Memory Down x16

**Table 14. System Memory Configuration Details Covered in this Section**

Parameter	Details
Processor	TGL UP3 4+2
Memory Type	DDR4
Configuration	MD Channel = x4 Memory Down (4 DRAM Devices) SoDIMM Channel = One SODIMM
Speed (MT/s)	3200
Channels	1 and 2
System Memory Voltage	1.2V
Max Ranks Per Channel	SoDIMM Channel - 2 Ranks Memory down channel - 1 Rank
DRAM Die Density (Gb)	8,16
Max Capacity (GB)	40GB, SODIMM 32GB + SDP Memory Down 4 DRAMs of 2GB. 48GB, SODIMM 32GB + DDP Memory Down 4 DRAMs of 4GB.
SO-DIMM Raw-Card Types	RC-A (1Rx8), RC-C(1Rx16), RC-E (2Rx8)
Memory Down Types <sup>1,2</sup> (Pkg Ranks - Die Bits - Pkg bits)	96-Ball BGA SDP 1-16-16, DDP 1-8-16 <sup>6</sup>
PCB Layers / Type <sup>3</sup>	Type-3/8L
DRAM Device Placement	Top Motherboard Layer, Single Sided, Channels are Back-to-Back Placement, Memory Down x16 Daisy-Chain Topology

*continued...*

Parameter	Details
CPU System Memory Ball Map <sup>4</sup>	Non-Interleaved
DRAM Device ODT Capability <sup>5</sup>	Enabled

*Notes:* 1. SDP: Single Die Package  
2. No mixed vendor support within a channel and No mixed memory DRAM down type support (SDP, DDP) within a channel.  
3. Type-3 = PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias. Refer PCB Stack-Up and Design Considerations for more details.  
4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-By-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.  
5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to [Table 16](#) on page 73  
6. For BG1 compatibility across SDP and DDP x16 devices, please refer to the excel sheet portion of the PDG

#### 4.3.5 Tiger Lake UP3 DDR4 Mixed SODIMM and Memory Down x8

**Table 15.** System Memory Configuration Details Covered in this Section

Parameter	Details
Processor	TGL UP3 4+2
Memory Type	DDR4
Configuration	MD Channel = x8 Memory Down (8 DRAM Devices) SoDIMM Channel = One SODIMM
Speed (MT/s)	3200
Channels	1 and 2
System Memory Voltage	1.2V
Max Ranks Per Channel	SoDIMM Channel - 2 Ranks Memory down channel - 1 Rank
DRAM Die Density (Gb)	8,16
Max Capacity (GB)	48GB, SODIMM 32GB + Memory Down 8 Devices of 2GB
SO-DIMM Raw-Card Types	RC-A (1Rx8), RC-C(1Rx16), RC-E (2Rx8)
Memory Down Types <sup>1,2</sup> (Pkg Ranks - Die Bits - Pkg bits)	78-Ball BGA SDP 1-8-8
PCB Layers / Type <sup>3</sup>	Type-3/8L
DRAM Device Placement	Top Motherboard Layer, Single Sided, Channels are Back-to-Back Placement, Memory Down x16 Daisy-Chain Topology

*continued...*

Parameter	Details
CPU System Memory Ball Map <sup>4</sup>	Non-Interleaved
DRAM Device ODT Capability <sup>5</sup>	Enabled
<p>Notes:</p> <ol style="list-style-type: none"> <li>1. SDP: Single Die Package</li> <li>2. No mixed vendor support within a channel and No mixed memory DRAM down type support (SDP, DDP) within a channel.</li> <li>3. Type-3 = PCB with zero build-up layers using Plated Through-hole (PTH) Vias with no Micro-vias. Refer "Stack-Up and PCB Considerations" chapter for more details.</li> <li>4. Non-Interleave = The processor is optimized for a side-by-side ball map and placement of the DRAM memory down devices or DIMM Side-By-Side (inline) placement. Each memory channel's signals are grouped together on one side of the processor packages.</li> <li>5. The DRAM Device ODT Capability can be enabled or disabled for reads and writes depending on the system memory interface margins. Enabling the DRAM device ODT increases the memory interface power and improves signal integrity/margins while disabling the DRAM device ODT decreases the memory interface power but degrades signal integrity/margins. For ODT implementation recommendation for this topology refer to <a href="#">Table 16</a> on page 73</li> </ol>	

## 4.4 DDR Byte Swapping

- LPDDR4x - Byte swapping is allowed within each x16 sub channel
- DDR4 - Byte swapping is allowed within each x64 channel.
- Bit swapping is allowed within each Byte for all DDR technologies.
- ECC bits swap is allowed within DDR4 ECC[7..0]

## 4.5 ODT Connectivity

**Table 16. ODT Signals Connectivity Table**

Processor	Memory Type	Side	Signal	Rule
<b>TGL UP4</b>	<b>LPDDR4x Memory Down</b>	Processor	Not connected	N/A
		DRAMs	in- band	
<b>TGL UP3</b>	<b>LPDDR4x Memory Down</b>	Processor	Not connected	N/A <b>ODT: On die Termination</b>
	<b>DDR4 Memory Down</b>	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	
		DRAMs	ODT[1:0]	
	<b>DDR4 SODIMM</b>	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	
		DIMMs	ODT[1:0]	

*Note:* For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

## 4.6 Data Mask (DM) Connectivity

**Table 17. DIMMs/DRAMs DM Signals Connectivity Table**

Memory Type	DM signals	Connect to
<b>LPDDR4x Memory Down</b>	DRAMs DM[7:0]	Tied to GND
<b>DDR4 Memory Down</b>	DRAMs DM[7:0]	Tied to VDDQ
<b>DIMMs</b>	DIMMs DM[8:0]	Tied to VDDQ

## 4.7 Via Placement and Pad Optimization

This section describes the following:

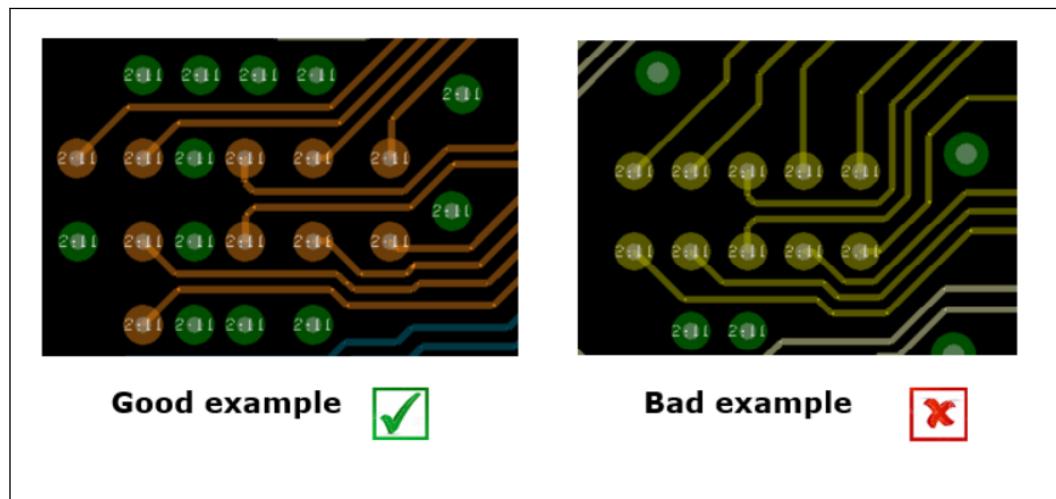
- System Memory Via Placement and Pad Optimization Guidelines
- Via Placement at SoDIMM and DRAM Device Side

### 4.7.1 Via Placement and Pad Optimization Guidelines

#### Via Placement at CPU Side

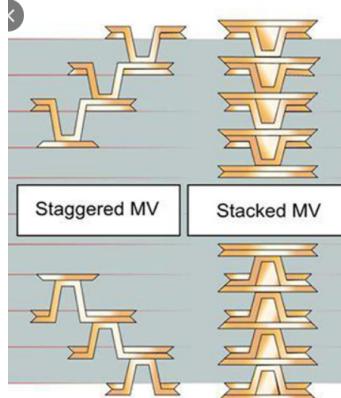
The following via stitching guidelines on the CPU-side are critical to follow to meet memory performance

- Improper or insufficient ground vias for any given signal can cause a significant impact at higher data rates. For single-ended signaling, if a properly stitched return path via is not placed in close proximity to every signal via, a nonideal return path is created.
- In a symmetrical stripline, the return current is shared equally between both reference planes. So, ensuring a ground stitching via which connects to both the reference planes of a signal layer is important.
- Follow the Reference Validation Platform (RVP) via placement at Processor side as much as possible for all Signal Groups.
- When a signal transitions to another routing layer, but the referencing plane is still kept the same, no stitching via is required.
- GND vias must be placed between signals from different signal groups and channels.
- Data and Strobe vias from different byte lanes must be separated by GND vias.
- For HDI or Type-4 memory down system designs, use GND Micro Vias from surface pin/pad (Top/Bottom) layer to connect to respective signal routing reference plane layers.
- A good example of CPU-side ground via stitching has sufficient ground coverage for every signal in a byte lane Figure below.
- Remove via pads from layers that are not connected to traces in [Figure 43](#) on page 76

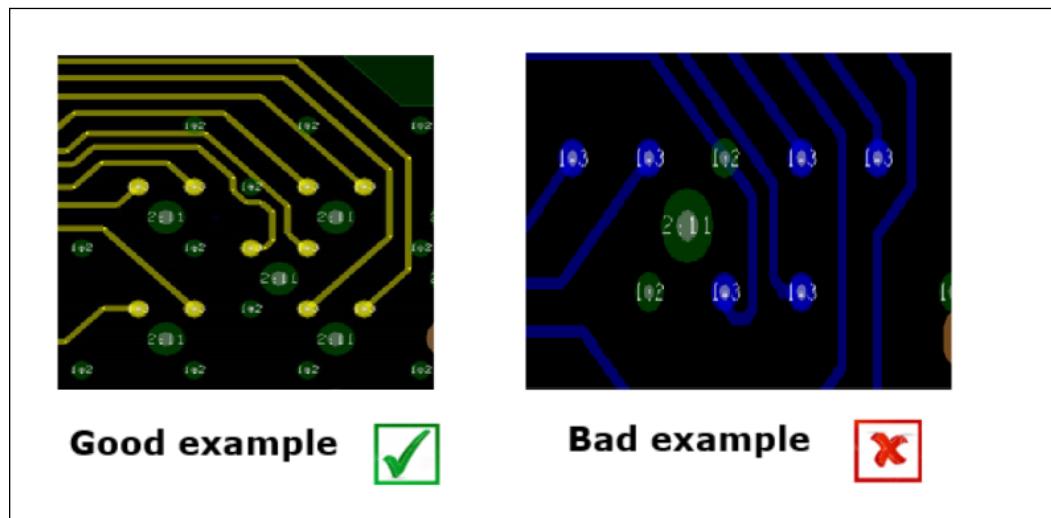
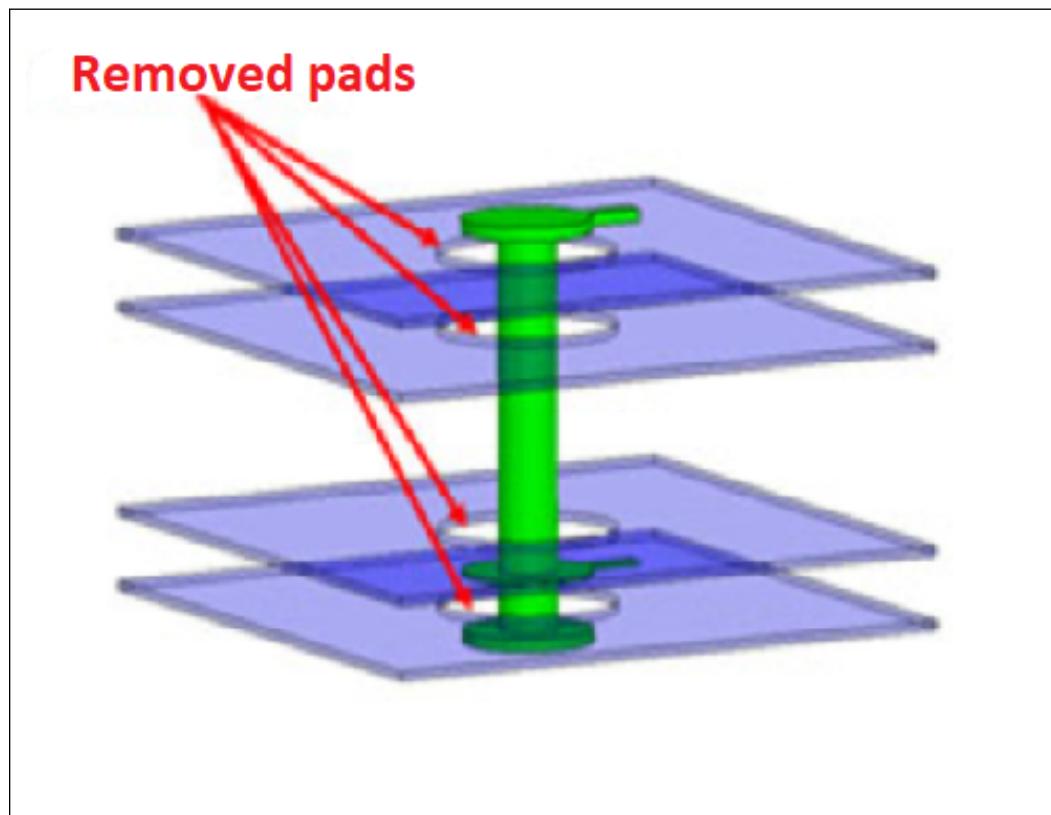
**Figure 41. CPU-side GND via Stitching Examples (GND vias in Green)**

#### 4.7.2 Via Placement at SoDIMM and DRAM Device Side

Similar to the via placement guidelines on the CPU-side, the following via placement guidelines on the DRAM-side ensure design robustness at high memory frequencies.



- Follow the Reference Validation Platform (RVP) via placement at SoDIMM or Memory DRAM Down side as much as possible for all Signal Groups.
- For Type-4 (any layer) memory down PCB designs use **Stacked Micro Vias** from layer 1 to layer 3 or 5 under the DRAM Devices and SOC rather than using **Staggered Micro Vias** to help minimize voiding on adjacent layer reference planes
- For Type-4 (1x1+) memory down PCB designs use Stacked Micro Vias from layer 1 to layer 3 under the DRAM Devices and SOC rather than using Staggered Micro Vias to help minimize voiding on adjacent layer reference planes and Micro Vias from layer 1 to layer 2 then transition to PTH from layer 2 to layer 5 under the DRAM Devices and SOC rather than using Staggered Micro Vias to help minimize voiding on adjacent layer reference planes
- GND/PWR vias must be placed between signals from different signal groups and channels.
- Data and Strobe vias from different byte lanes must be separated by GND vias.
- A good example of DRAM-side ground via stitching has sufficient ground coverage for every signal in a byte lane Figure below
- Follow the via spacing guidelines covered in table below.
- Remove via pads from layers that are not connected to traces in [Figure 43](#) on page 76

**Figure 42. DRAM-side GND via Stitching Examples (GND vias in Green)****Figure 43. Remove PADs from Layers that Do Not Connect to Trace**

**Table 18. Guidelines for Vias Separation**

CPU	Memory Type	Signal Group	Signal:GND Rule	Pitch (mm)
UP3 4+2	SODIMM	DQ/DQS/DQS#	1:1 (microvia) 1:1-2:1 (PTH/Buried via)	≤0.65
		CLK/CTRL/CKE/CMD	1:1 (microvia) 1:1-2:1 (PTH/Buried via)	≤0.65
		1 DIMM Per Channel	Pitch between DQ vias from different byte lanes	>1.524 (PTH/Buried pitch)
			Pitch between CMD to CTRL vias	>1.524 (PTH/Buried pitch)
	Memory Down	DQ/DQS/DQS#	1:1 (microvia) 1:1-2:1 (PTH/Buried via)	≤0.65
		CLK/CTRL/CKE/CMD	1:1 (microvia) 1:1-2:1 (PTH/Buried via)	≤0.65
		DQ to DQ from different byte lanes	Pitch between DQ vias from different byte lanes>	≥0.607 (microvia) ≥0.915 (PTH/ Buried)

Note: 1. Via-to-via pitch is measures between via centers

## 4.8 Reference Voltage (VREF)

This section describes the following:

- UP3 System Memory Reference Voltage (VREF) Guidelines
- UP4 System Memory Reference Voltage (VREF) Guidelines

### 4.8.1 Tiger Lake UP3 System Memory Reference Voltage (VREF) Guidelines

System memory reference voltages:

DDR4: DDR0\_VREF\_CA, DDR1\_VREF\_CA for DDR4 must meet the following guidelines

- Follow the Customer Reference Board (CRB) board file and schematic implementation as closely as possible.
- Place the VREF voltage dividers as close as possible to the SODIMMs or memory down DRAM devices.
- All VREF traces should be at least 0.5mm wide with 0.5 mm spacing to other signals/planes. Short violations are acceptable if required due to tight routing constraints.

LPDDR4x has all Vref Internal inside the DRAMS

## 4.8.2 Tiger Lake UP4 System Memory Reference Voltage (VREF) Guidelines

LPDDR4x has all Vref Internal inside the DRAMS

## 4.9 Memory Side Power Delivery

This section describes the following:

- DDR Power Delivery Memory Side

### 4.9.1 Tiger Lake DDR Power Delivery Memory Side

The guidelines here are to support a single sided component assembly.

The expectation is that the DRAM decoupling caps will be placed as close as possible to the DRAM devices to minimize the loop inductance of the caps. A distance of greater than 5mm from the device is not recommended.

The decoupling capacitor to DRAM device inductance loop is improved with single sided assembly, if the power and ground planes are strongly coupled, and cap placement and connection by common power integrity practices.

Dual sided designs may prove to be a superior solution for certain board technologies, thickness of the stack up and placement location of the caps under the memory devices. This document does not cover the dual sided assembly guidelines.

## 5.0 CPU I/O

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### 5.1 Thunderbolt™ Design Guidelines

Thunderbolt™ technology (TBT) is a transformational high-speed, dual protocol I/O, and it provides flexibility and simplicity by encapsulating both data (PCIe\*) and video (DisplayPort\*) on a single cable connection that can daisy-chain up to six devices.

Thunderbolt controllers act as a point of entry or a point of exit in the Thunderbolt domain. The Thunderbolt domain is built as a daisy chain of Thunderbolt enabled products for the encapsulated protocols - PCIe and DisplayPort. These protocols are encapsulated into the Thunderbolt fabric and can be tunneled across the Thunderbolt domain.

Thunderbolt controllers can be implemented in various systems such as PCs, laptops and tablets, or devices such as storage, docks, displays, home entertainment, cameras, computer peripherals, high end video editing systems, and any other PCIe based device that can be used to extend system capabilities outside of the system's box.

Thunderbolt™ 4 connection data rate is 20Gbps per lane and is compatible with Thunderbolt™ 4 specification enabling a Thunderbolt link at up to 2x20Gbps, as well as backward compatible with Thunderbolt 1 (10Gbps) and Thunderbolt 2 (2x10Gbps) specifications.

Note: Thunderbolt™ 4 is a USB-C solution Intel brand which requires the following elements:

USB2, USB3 (10G), USB3/DP implemented at the connector

In addition, it requires USB4 implemented up to 40G, including TBT3 compatibility as defined by USB4/USB-PD specs

Thunderbolt 4 solutions use (and prioritize) the USB4 PD entry mode (while still supporting TBT3 alt mode)

#### 5.1.1 Thunderbolt™ Port Power Requirements

##### Host Source Requirements

Single Port Hosts are required to minimally support 3A/5V on VBUS in Thunderbolt Mode.

Hosts with more than one port are required to provide power per the table below. All Thunderbolt ports shall be capable of providing Full VBUS power on a first-come, first-served basis up to the minimum number of required ports. Tablet PCs with screen sizes less than 14" shall provide a minimum of 4.5W on all Thunderbolt ports.

Thunderbolt Hosts shall provide 1.5W to the VCONN pin on all Thunderbolt ports. The VCONN voltage is required to be between 4.75V and 5.5V per USB Type-C r1.0. Note that 1.5W power from VCONN is higher than the 1.0W required by USB Type-C r1.0.

All Ports shall use the termination defined in Table 4-10 in USB Type-C r1.0 to broadcast their available Source current. The DFP/Source shall modify its termination to reflect any changes in Source current availability. Thunderbolt Ports shall use the 3.0A/5V pull-up.

Hosts must be DRPs to be able to support peer-to-peer communication.

**Table 19.**
**VBUS Power Provisioning with Number of Thunderbolt™ Ports**

Power Standard	Voltage/Current	1 Port	2 Port	3 Port	4 Port
First Port VBUS Power	5V/3A <sup>1,3</sup>	1	1	1	1
Second Port VBUS Power	5V/1.5A or 5V/900mA <sup>2,3,4</sup>	NA	1	2	3
VCONN Power	1.5W TBT	1	2	3	4

*Notes:*

1. 5V/3A is required for one of every four ports. It is recommended that 5V/3A be provided per every two ports if possible. The power rules defined in USB PD shall be followed if power greater than 15W is provided.
2. 5V/900mA minimum is required for the second, third, and fourth ports.
3. Power should be allocated on a first-come first-serve basis between the first, second, third and fourth ports. If the first port only consumes 5V/900mA, then second port shall make 5V/3A available. If the first and second ports only consume 5V/900mA each, the third port shall make 5V/3A available. If the first, second, and third ports only consume 5V/900mA each, the fourth port shall make 5V/3A available.
4. Most Thunderbolt Bus Powered Devices have no functionality with Half of minimum power.

### Power Delivery

Refer to **USB PD r2.0** power compliance document for the compliance measurements. The document can be downloaded from <http://www.usb.org>.

### Thunderbolt™ Power Provider VBUS Electrical Requirements

The VBUS Source Electrical Parameters are specified in Table 7-22 and Table 7-24 of the USB PD r2.0 Specification. The VCONN Source requirements are specified in Table 4-2 and Table 4-3 of the USB Type-C r1.0 Specification. The only specifications defined here are those which differ from or are in addition to the USB PD r2.0 and the USB Type-C r1.0 Specifications. This specification assumes compliance with USB Type-C r1.0 specification with additional conditions specifically required for Thunderbolt.

Thunderbolt Power Providers must supply 5V and shall use the Fixed Voltage PDO. The current has been chosen to yield 10.5W worst-case for a bus powered device after the switching regulator assuming 88% efficiency at 5V. The requirements for Power Provides is shown in table below.

Optional VBUS sources can provide 9V, 15V and 20V following the USB PD r2.0 Specification.

USB Type-C and USB PD specification can be downloaded from <http://www.usb.org>.

**Table 20.** **Thunderbolt™ VBUS Source Electrical Parameters**

Parameter	Description	Min	Typ	Max	Units	Note
VSrc_BPD5 <sup>1</sup>	Minimum voltage provided to port in Active when connected to a BPD	4.75	5	5.5	V	3A min current
<i>Note:</i> 1. Thunderbolt Specific Requirement						

### Thunderbolt™ VCONN Source Electrical Requirements

The Thunderbolt Power Provider VCONN Electrical Parameters are specified in table below.

**Table 21.** **Thunderbolt VCONN Source Electrical Requirements**

Parameter	Description	Min	Typ	Max	Units	Note
VSrc_Susp	Minimum voltage provided to port in suspend	4.25	5	5.5	V	70mW min
VSrc_Active	Minimum power provided to port in Active	4.25	5	5.5	V	1.5W min

## 5.1.2 Reference Documents

**Table 22.** **Reference Documents**

Title	Document #
Fiberweave Effect: Practical Impact Analysis and Mitigation Strategies	406926

### Compliance Specification

**Table 23.** **Thunderbolt™ Compliance Specification**

Title	Document #
Thunderbolt - USB Type-C TBT Specification	557111
Thunderbolt - Host Electrical Validation Test Specification	567664
Thunderbolt 3 Based PC Host Functional Compliance Test Specification	557133

## 5.1.3 Thunderbolt™ 3 Connector Guideline

Refer to <https://thunderbolttechnology.net/developers> for Thunderbolt 3 certified USB Type-C connectors.

## 5.2 USB-C\* Sub-System

USB-C\* is a cable and connector specification defined by USB-IF.

The USB -C\* protocol in TGL supports USB2, USB3, DPoC, and USB4 protocols.

USB4 is a Standard architecture (formerly known as CIO), but with the addition of USB3 (10G) tunneling, and rounded frequencies. USB4 adds a new USB4 PD entry mode, but fully documents the mode entry, and negotiation elements of Thunderbolt™ 3.

Below are functional block diagrams for TGL USB-C for different SKUs. There are 4 main components needed to support USB-C\* features POR for Intel platforms.

- **PD Controller:** PD Controller is a 3<sup>rd</sup> party discrete IC supporting various type-C\* features such as detecting attach/orientation of cable, connecting VCONN/VBUS to connector, providing UFP/DFP roles and USB Power delivery protocol. It also has all the control logic needed to communicate with type-C\* port partner.
- **EC:** EC can make decisions on USB PD policy along with help of OS and also helps support UCSI spec.
- **Re-driver/Re-timers:** These are discrete ICs needed on the motherboard to boost signal strength/condition the high speed signals. Requirements are based on different speeds the IC has to support.

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**NOTE**

2 re-timers in series per USB-C\* connector not supported on TGL UP3/UP4 processors.

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**NOTE**

Intel supports only Burnside Bridge re-timers, there is no POR to support or validate re-timers from 3<sup>rd</sup> party vendors

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- **Miscellaneous Logic:** This is miscellaneous logic needed on the motherboard such as FETs for controlling power to/from VBUS, AC caps, discrete resistors/CMC/ESD etc. Depending on features integrated on PD Controller, the amount of misc. logic needed on the board will vary.

Details about these components is listed in next section.

**PDG Documentation:** All the discrete components (PD Controller, retimers, VBUS load switches) in the block diagrams below are suggested to be powered using "A" rail (i.e. rail active in Sx & S0 but off in DSx) to support wakes in Sx and also to avoid any electrical leakage issues. EC could be on "A" rail or DSW rail.

Figures below are high level example implementation block diagram, actual implementation on schematic may vary.

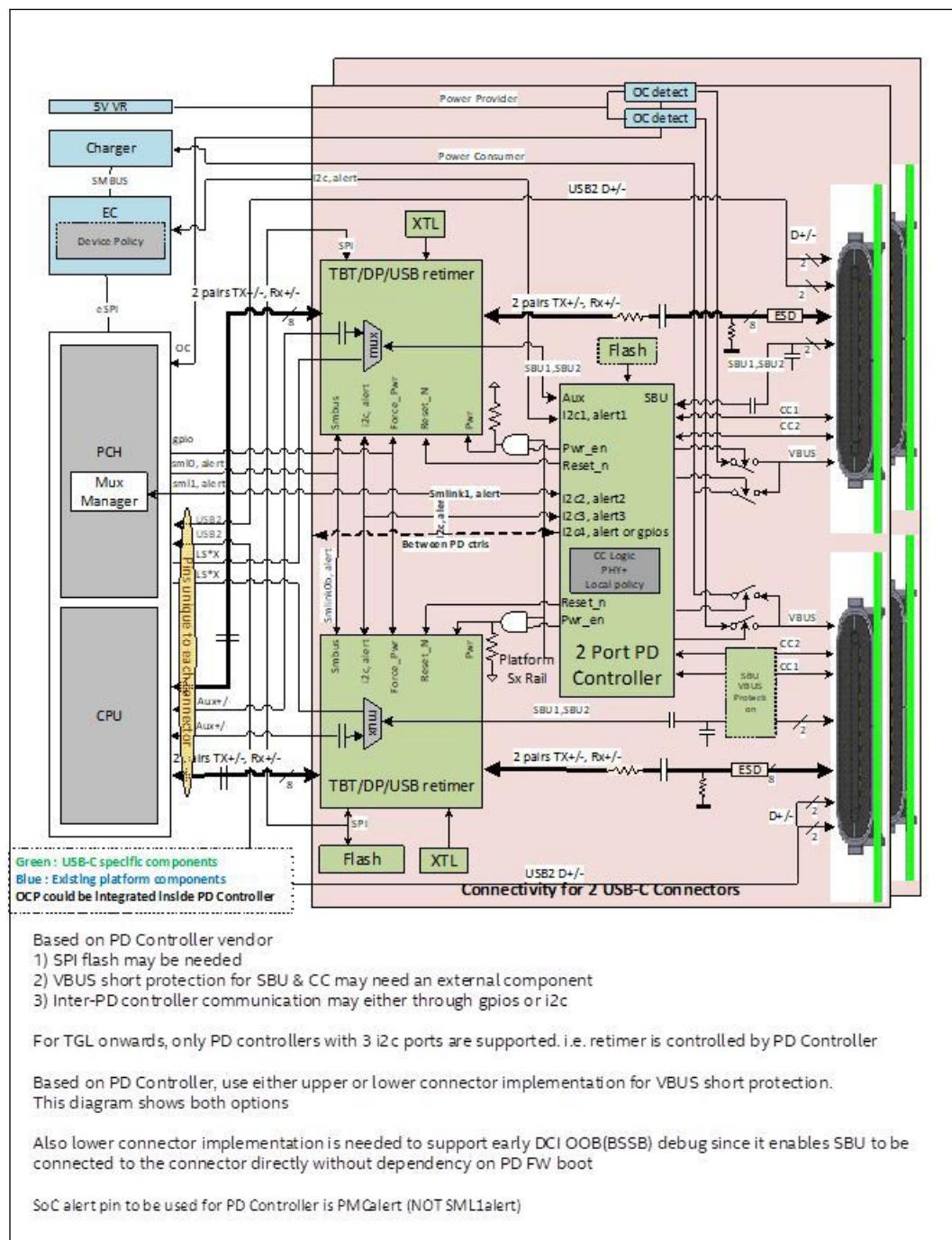
**Figure 44. USB - C\* Block Diagram**

Figure 45. USB3/DP w/ re-timer on USB - C\* Block Diagram

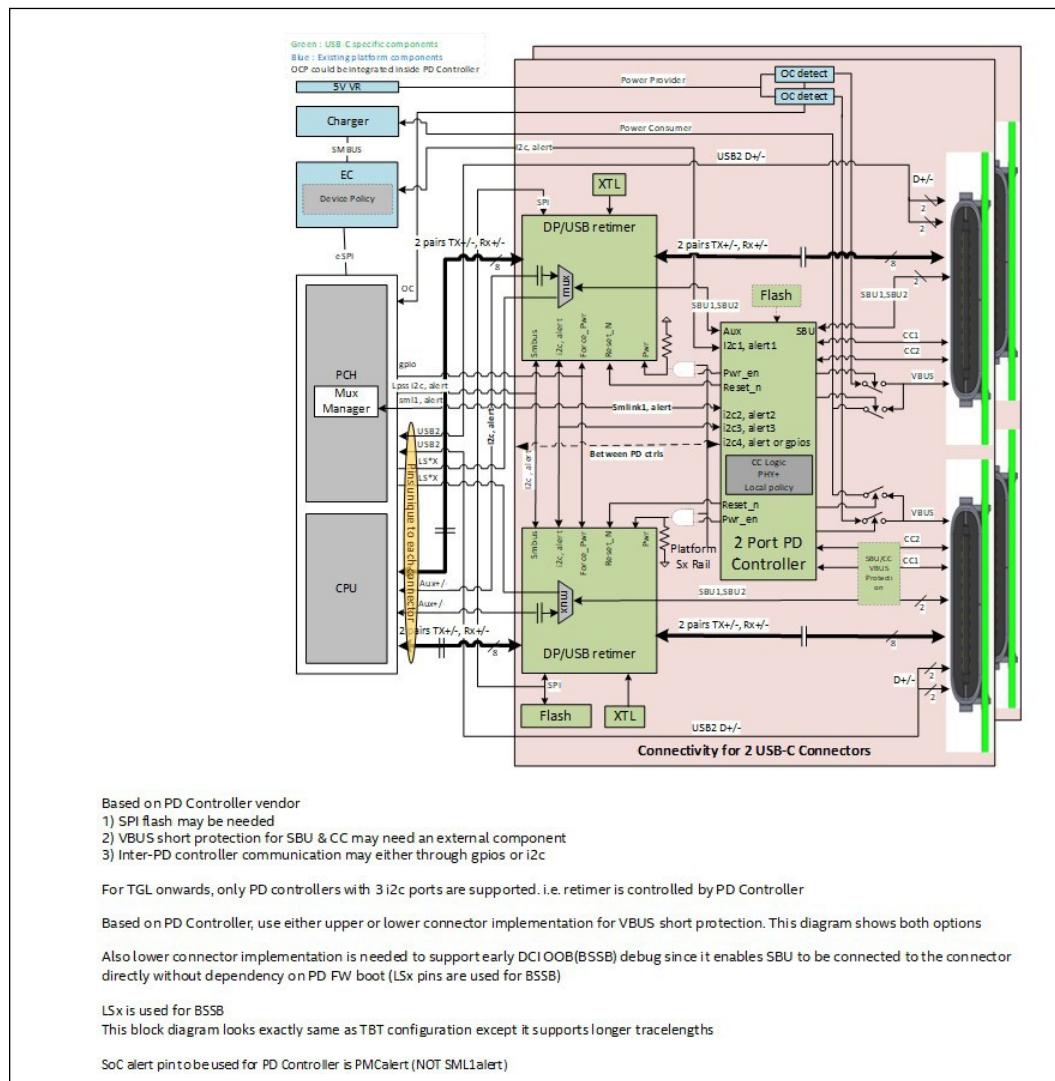
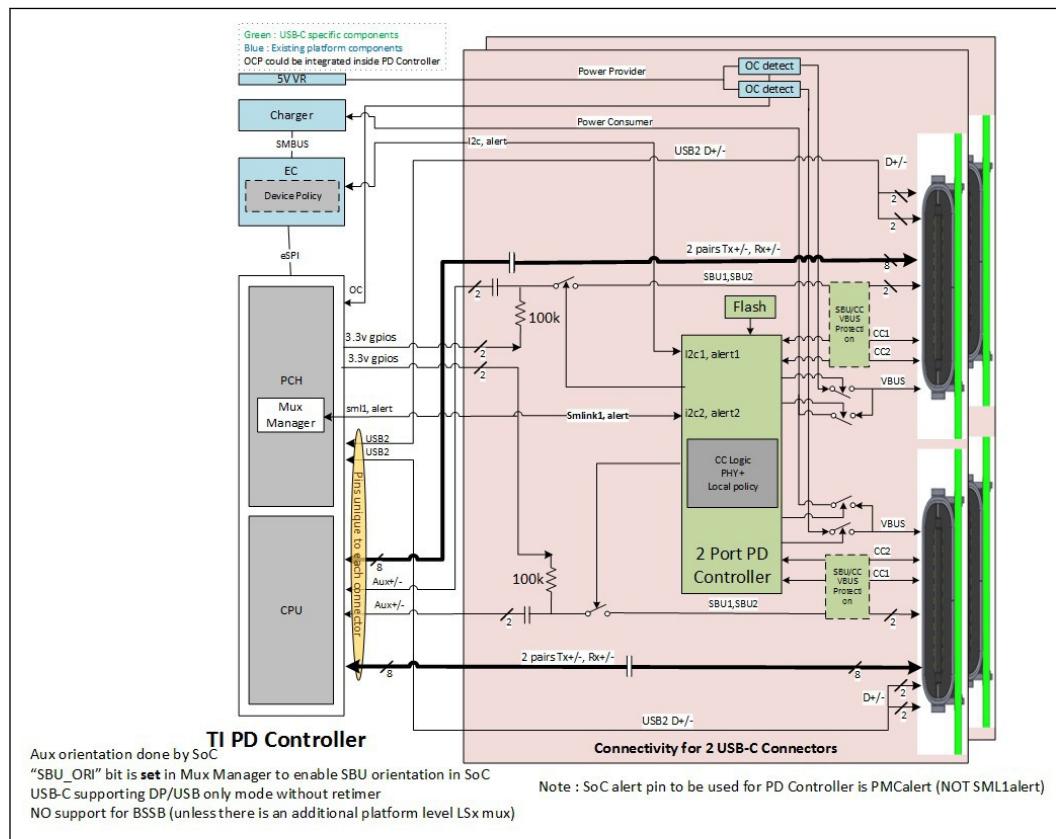
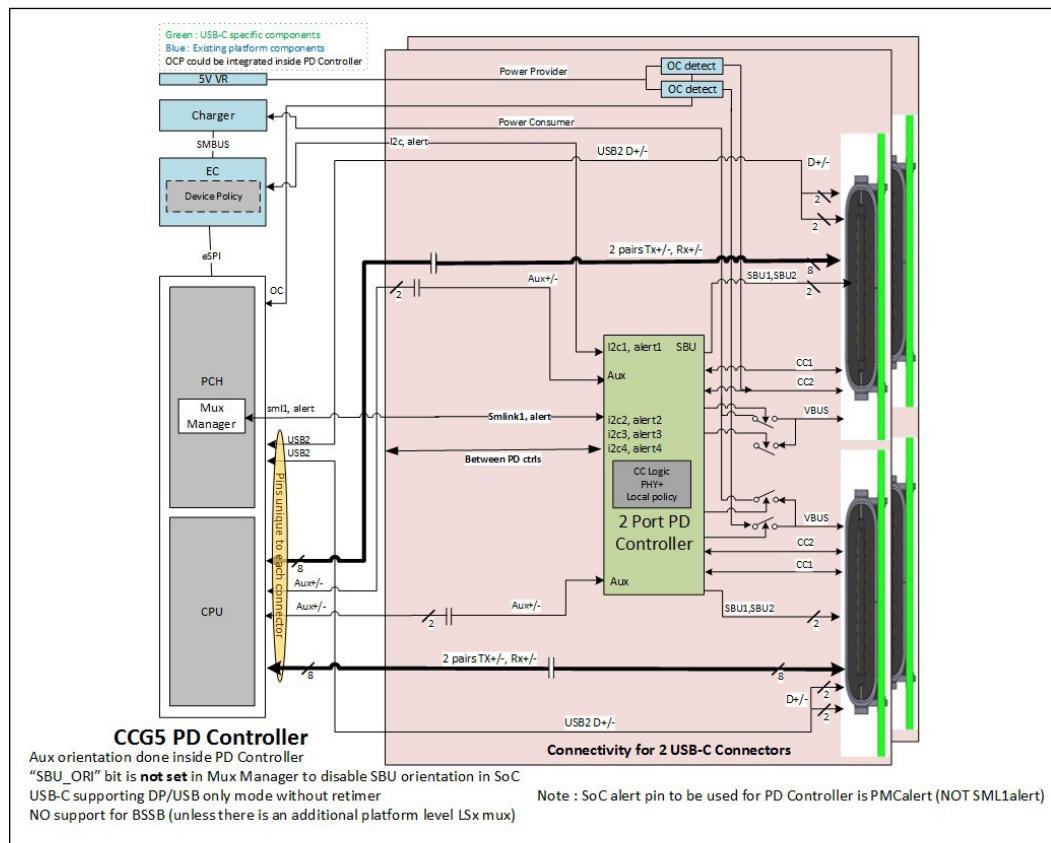


Figure 46. USB3/DP w/o re-timer USB - C\* Block Diagram with TI65994



**Figure 47. USB3/DP w/o re-timer USB-C\* Block Diagram with CCG5**



#### NOTE

It is possible to use integrated orientation muxes inside CCG5 PD Controller for Aux orientation for w/o re-timer configuration but there is no POR to support or validate this configuration

### 5.2.1

#### Aux/LSx Muxing

Aux and LSx are sideband signals used for DisplayPort and Thunderbolt Alternate modes respectively. Aux is driven from processor, is low voltage & uses AC coupled differential pair signaling. LSx is driven from PCH, is 3.3v & uses DC coupled UART signaling. Due to this, it is not possible to mux them internally inside SoC - platform level mux is required. Burnside Bridge re-timer has integrated this mux and orientation capability since all USB 4 capable connectors will have Burnside Bridge re-timer on the board, no additional consideration is needed for OEM's.

The LSx GPIOs in PCH are mapped to specific USB-C\* port in processor, so while routing LSx for a given USB-C\* connector, this important mapping needs to be considered.

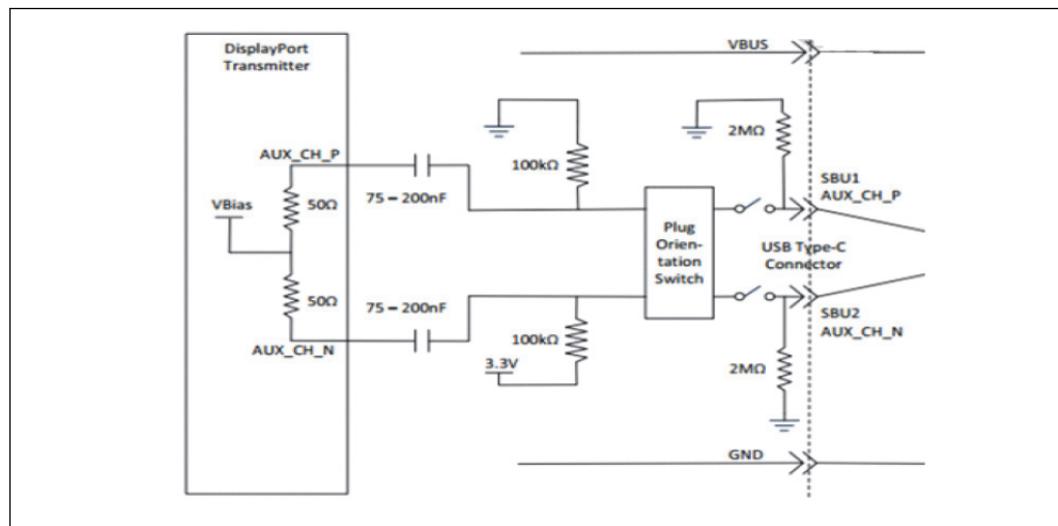
## 5.2.2 Aux Bias/Orientation/Isolation Control

Below considerations for configurations w/o re-timer and USB/DP only capable connectors.

As part of USB-C\* integration support, in addition to supporting orientation muxing of data signals, need to support orientation muxing of aux signals with requirements shown below from VESA DP alt mode spec. There are pulldown and pullups on Aux signals **after** the capacitor and before the orientation mux. This aux orientation muxing was done in discrete USB/DP muxes **after** the resistors & capacitors on the motherboard.

Example is shown in the figure below

**Figure 48. DP Alternate Mode Specification for Aux Orientation Muxing**



In TGL, since SoC cannot integrate capacitors and resistors, the orientation can happen only before capacitors and resistors.

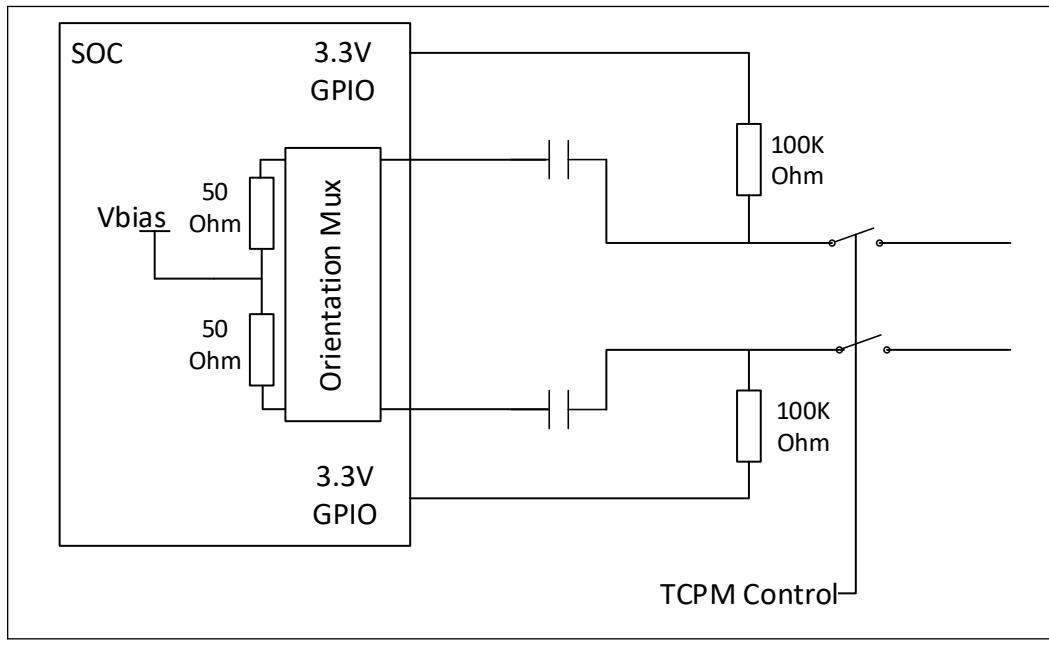
TGL SoC has support for integrated Aux orientation, since the biasing resistors and AC Caps are going to be after the orientation mux, special considerations are needed.

Default TGL implementation is to use 2 PCH GPIOs per USB-C\* connector and drive them in accordance with plug orientation in addition to controlling the orientation mux inside the SoC. The GPIOs are managed by SoC HW and no action needed by TCPM for controlling those GPIOs. In addition, TCPM also controls a platform level switch to make sure Aux is isolated from SBU pins when the system not in alternate mode.

The topology below behaves functionally similar to the VESA requirements described earlier even though location of orientation mux is different in VESA diagram.

Below diagram shows the default case, based on specific platform configuration. In addition, there is a need to communicate to SoC about need of Aux orientation, so SoC does aux orientation in desired selective cases.

**Figure 49. Tiger Lake SoC USB-C Aux Muxing Proposal**



#### NOTE

GPP E22, and GPP E23 can be used for AUX Bias.

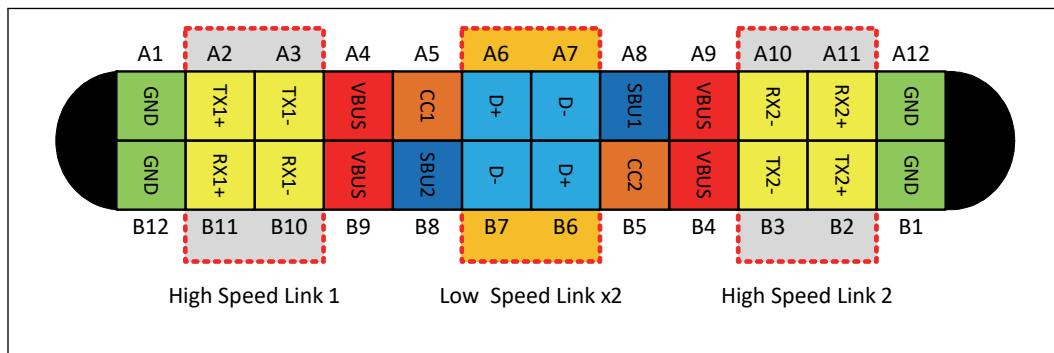
### 5.2.3 USB-C\* Connector

USB-C\* connector consists of 24 signal pins designed in a symmetrical way. Refer to figure below.

There are up to six differential pairs available on a USB-C\* connector, with 4 high speed different pairs and two low speed pairs. There are two configuration channel signals (CC1/CC2) on the connector which is used for:

- Device detection
- Orientation detection
- Establish DFP and UFP roles
- Discover and configure power
- Discover and configure optional alternate/accessory modes

Unused CC pin will be reconfigured as Vconn, which is used to power the active cable.

**Figure 50. USB-C\* Receptacle Anatomy**

With two configuration channel signals for communication, USB-C\* connector can support USB3/USB2 interfaces and any other vendor specific interfaces like DisplayPort and TBT in Alternate Mode.

In Alternate Mode, both the high speed and low speed link and both the SBU1/2 pins can be reconfigured to support the intended configuration. Refer table below for an examples of the lane configuration.

**Table 24. USB-C\* Connector Signal Group and Description**

Group	Signal Name	Description
Power	VBUS	VBUS, capable of up to 5A @ 20V with USB PD
	VCONN	VCONN is a power source to active cable which is capable of supplying up to 0.2A @ 5V. Unconnected CC pin will be reconfigured to VCONN when a device is plugged in.
Ground	GND	Ground
High Speed Differential	TX1+	First USB3.2 or Display Alt Mode or USB 4 Alt Mode Diff TX pair
	TX1-	
	RX1+	First USB3.2 Diff or USB 4 Alt Mode RX pair or Display Alt Mode Diff TX pair
	RX1-	
	TX2+	Second USB3.2 or Display Alt Mode or USB 4 Alt Mode Diff TX pair
	TX2-	
	RX2+	Second USB3.2 Diff or USB 4 Alt Mode RX pair Display Alt Mode Diff TX pair
	RX2-	
Low Speed Differential	D+	Low Speed Differential Pair, primary for USB 2 connection
	D-	
Control	CC1	Configuration Channel 1. Used for device detection, orientation detection and Alternate Mode configuration. Unconnected pins will be reconfigured to Vconn.
	CC2	Configuration Channel 2.Used for device detection, orientation detection and Alternate Mode configuration. Unconnected pins will be reconfigured to Vconn
Side band	SBU1/SBU2	Sideband signals for use by alternate: <ul style="list-style-type: none"> <li>• DP mode -AUX signals</li> <li>• USB 4 mode - LSx signals</li> </ul>

**NOTE**

Refer PCH-Low Speed Link (LSx) chapter for details on LSx layout guidelines.

**Table 25. USB-C\* Supported Configuration**

<b>Lane1</b>	<b>Lane2</b>	<b>Comments</b>
USB4	USB4	Both lanes operate at Gen 2 (10G) or Gen 3 (20G) and also support non-rounded frequencies (10.3125G / 20.625G) for TBT3 compatibility.
USB3.2	No connect	Any combination of: USB3.2 Gen 1x1 (5Gb/s) USB3.2 Gen 2x1 (10Gb/s)
No connect	USB3.2	Any combination of: • USB3.2 Gen 1x1 (5Gb/s) • USB3.2 Gen 2x1 (10Gb/s)
USB3.2	DPx2	Any of HBR3/HBR2/HBR1/RBR for DP and USB3.2
DPx2	USB3.2	Any of HBR3/HBR2/HBR1/RBR for DP and USB3.2
DPx4		Both lanes @same DP rate - no support for 2x DPx2 USB-C connector

**Table 26. USB-C\* Non-Supported Configuration**

<b>Lane1</b>	<b>Lane2</b>	<b>Comments</b>
#	PCIe	No PCIe native support
USB 4	#	No support for USB 4 with any other protocol
USB3.2	USB3.2	No support for Multi-lane USB

**Table 27. Interchangeable DDI and USB-C\* Connectors**

<b>Port group</b>	<b>Package/Pin port Name</b>	<b>TGL UP4</b>	<b>TGL UP3</b>
Group A	TCP0	USB-C/DP/HDMI	USB-C/DP/HDMI
	TCP1	USB-C/DP/HDMI	USB-C/DP/HDMI
Group B	TCP2	USB-C/DP/HDMI	USB-C/DP/HDMI
	TCP3	N/A	USB-C/DP/HDMI

*Note:*

- USB-C\* connector may support USB4/DP/USB3 capability or USB3/DP only capability.
- TCP\* pins can be routed to USB-C\* connector or DP/HDMI native connector (for DP/HDMI connector support refer to chapter 5.3)
- Port group is defined as two ports sharing the same USB4 router, each router supports up to two display interfaces.
- Display interface can be connected directly to a DP/HDMI/Type-C port or thru USB 4 router (Tunneled) on a Type-C connector.
- If two ports in the same group are configured to one as USB4 and the other as DP/HDMI fixed connection each port will support single display interface.

**Table 28. TCSS Port Allocation Recommendations**

<b>Port Allocation options</b>	<b>Port Group A TCP 0/1</b>	<b>Port Group B TCP 2/3</b>
1x Type-C + 1x DP/ HDMI	1xTCP 1x N.C	1xDP/HDMI 1x N.C
2x Type-C Note 4	1xTCP 1x N.C	1xTCP 1x N.C
2x Type-C + 1x DP/ HDMI	2xTCP	1xDP/HDMI 1x N.C
1x Type-C + 2x DP/ HDMI	1xTCP 1x N.C	2x DP/HDMI
2x Type-C +2x DP/ HDMI	2xTCP	2x DP/HDMI
3x Type-C + 1x DP/ HDMI	Any option	
1x Type-C + 3x DP/ HDMI		
4x Type-C		
4x DP/HDMI		
<p><i>Notes:</i></p> <ul style="list-style-type: none"> <li>• DP/HDMI implementation can also be referred as fixed connections.</li> <li>• N.C is referring to a port which is not routed.</li> <li>• Implementing Type-C + HDMI/DP in the same group will limit the Type-C (direct and tunneled modes) to support only one display interface.</li> <li>• Display interface can be connected directly to a DP/HDMI/Type-C port or thru USB 4 router (Tunneled) on a Type-C connector.</li> <li>• DP/HDMI can also be implemented on DDIB to optimize port allocations - Please refer to display chapter for more information.</li> </ul>		

**Table 29. TCSS Data, Sideband and Comp Signals**

<b>Signals</b>	<b>Values</b>
TC_RCOMP_N / TC_RCOMP_P	150Ω +/-1% between TC_RCOMP_N and TC_RCOMP_P. Provide good noise isolation. Platform Rdc < 0.5Ω for the sum of both signals. TCSS RCOMP has a capacitance requirement: capacitance on RCOMP nets cannot exceed 1.9pF each. This includes routing and via caps.
TCP[3-0]_AUXPAD_N TCP[3-0]_AUXPAD_P	Common Lane: AUX N/P - pad
TCP[3-0]_TXRX_P[1-0] TCP[3-0]_TXRX_N[1-0]	Data Lane, RX, complementary signals N/P. Also serves as the secondary TX for display modes.
TCP[3-0]_TX_P[1-0] TCP[3-0]_TX_N[1-0]	Data Lane, TX, complementary signals P/N
<p><i>Note:</i></p> <ul style="list-style-type: none"> <li>• Unused data and AUX signals should be left no connected at the BGA ball</li> </ul>	

**Table 30. USB3/USB2 Port Pairing for USB-C\* Connectors**

	<b>Connector C0</b>	<b>Connector C1</b>	<b>Connector C2</b>	<b>Connector C3</b>
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C\* connectors with increasing port numbers (TCP0\_\*, TCP1\_\*, TCP2\_\*, TCP3\_\*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C\* connectors, but it is not strictly required.

**Table 31. USB-C\* Signals Mapping**

<b>Port<sup>(1)</sup></b>	<b>Processor to Re-timer</b>	<b>Re-timer to USB-C* Connector</b>	<b>Processor to USB-C* Connector w/o re-timer</b>
Port 0	TCP0_TX0	TCP0_RT_TX0	TCP0_DIRECT_TX0
	TCP0_TX1	TCP0_RT_TX1	TCP0_DIRECT_TX1
	TCP0_RX0	TCP0_RT_RX0	TCP0_DIRECT_RX0
	TCP0_RX1	TCP0_RT_RX1	TCP0_DIRECT_RX1
Port 1	TCP1_TX0	TCP1_RT_TX0	TCP1_DIRECT_TX0
	TCP1_TX1	TCP1_RT_TX1	TCP1_DIRECT_TX1
	TCP1_RX0	TCP1_RT_RX0	TCP1_DIRECT_RX0
	TCP1_RX1	TCP1_RT_RX1	TCP1_DIRECT_RX1
Port 2	TCP2_TX0	TCP2_RT_TX0	TCP2_DIRECT_TX0
	TCP2_TX1	TCP2_RT_TX1	TCP2_DIRECT_TX1
	TCP2_RX0	TCP2_RT_RX0	TCP2_DIRECT_RX0
	TCP2_RX1	TCP2_RT_RX1	TCP2_DIRECT_RX1
Port 3 <sup>(2)</sup>	TCP3_TX0	TCP3_RT_TX0	TCP3_DIRECT_TX0
	TCP3_TX1	TCP3_RT_TX1	TCP3_DIRECT_TX1
	TCP3_RX0	TCP3_RT_RX0	TCP3_DIRECT_RX0
	TCP3_RX1	TCP3_RT_RX1	TCP3_DIRECT_RX1
<p><i>Notes:</i> 1. Each port can be connected either USB-C* directly (w/o re-timer) or through re-timer to connector.  2. Port 3 configurations are valid for TGL UP3 SKU only  3. For Burnside Bridge re-timer pin information refer #572046.</p>			

### TCSS General Guidelines

**Table 32. Length Matching Rules**

<b>Rules</b>	<b>Values</b>	<b>Topology</b>
Length Matching between P and N within a differential pair	Within Layer Max Mismatch: 125um Total Length Max Mismatch: 125um	USB3/USB3/DP
	Within Layer Max Mismatch: 250um Total Length Max Mismatch: 125um	USB3/DP
Length matching between Pair to Pair (inter Pair)	Within 25mm	All
Short Protection circuit	It is recommended to include this circuit to comply with USB ECN " RX AC Coupling Capacitor Option" to provide ESD/EOS protection and set RX bias at the USB-C*	All
<i>continued...</i>		

Rules	Values	Topology
	connector. Intel's recommendation on DC rating of the Crx is 25V. The customer should consider short event to VBUS that can be up to 20V.	
TCRCOMPN / TCRCOMPP	150Ω +/-1% between TCRCOMPN and TCRCOMPP. Provide good noise isolation. Platform Rdc <0.5Ω for the sum of both signals.	USB4/USB3/DP
RCOMP capacitance	Capacitance on RCOMP nets (TCRCOMP/N and TCP0_MBIAS_RCOMP) cannot exceed 1.9pF each. This includes routing and via caps. Assumption: Parasitic cap of the RCOMP resistor is 5pF max.	USB4/USB3/DP
<p><b>Note:</b></p> <ul style="list-style-type: none"> <li>It is recommended to void unused pads for differential vias, and pin pads for CMCs, ESDs, AC Cap, and connectors to optimize the impedance matching in the channel.</li> <li>For optimal performance it is recommended to begin layout with USB4, use arc routing and maintain 3H spacing vias/void/splits. It is also recommended that return loss specification of routing from Re-timer to USB-C* connector is met. Refer to section 5.5.11 of USB-C* specification (#557111)</li> <li>It is recommended to use 0201 between re-timer and USB-C* connector</li> <li>Routing and return via requirement near vertical transition - for all vertical transitions, the differential Tlines should be connected to the two vias symmetrically. Moreover, Vss return vias should be placed near the signal vias in an equidistant symmetrical manner, and all signal vias should have identical Vss return vias around each of them.</li> </ul>		

## 5.3 Display Interfaces

**Table 33.** DDI Ports Availability

SKU	UP4 Processor Line	UP3 Processor Line
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	eDP*/DP*/HDMI*/MIPI_1	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*

*Note:* HBR3 supported on TCP ports only.  
Each of the TCP port can support DPoC\* (DisplayPort\* over Type-C)

**Table 34.** Display Topology Summary

Interface	Topology
DisplayPort* (DP*)	Direct (All Ports)
	Re-timer (TCP ports only)
	Internal Cable (All Ports)
	Internal Cable with Re-timer (TCP ports only)
	HPD
Embedded DisplayPort* (eDP*)	Direct Topology (DDI A/B port)
	HPD

*continued...*

Interface	Topology
HDMI*	Re-timing Level Shifter (All ports)
	Linear Re-Driver Level Shifter (TCP ports only)
	Active Level Shifter (All ports)
	Internal Cable Active Level Shifter (All ports)
	Cost Reduced Level Shifter 2.97GT/s (TCP ports only)
	Cost Reduced Level Shifter 1.65GT/s (All ports)
	DDC signals design guidelines
	HPD
MIPI DSI	Direct (DDI A/B ports only)
Note: HDMI Active Level shifter driven from TCP are supported but not fully validated.	

### Reference Documents

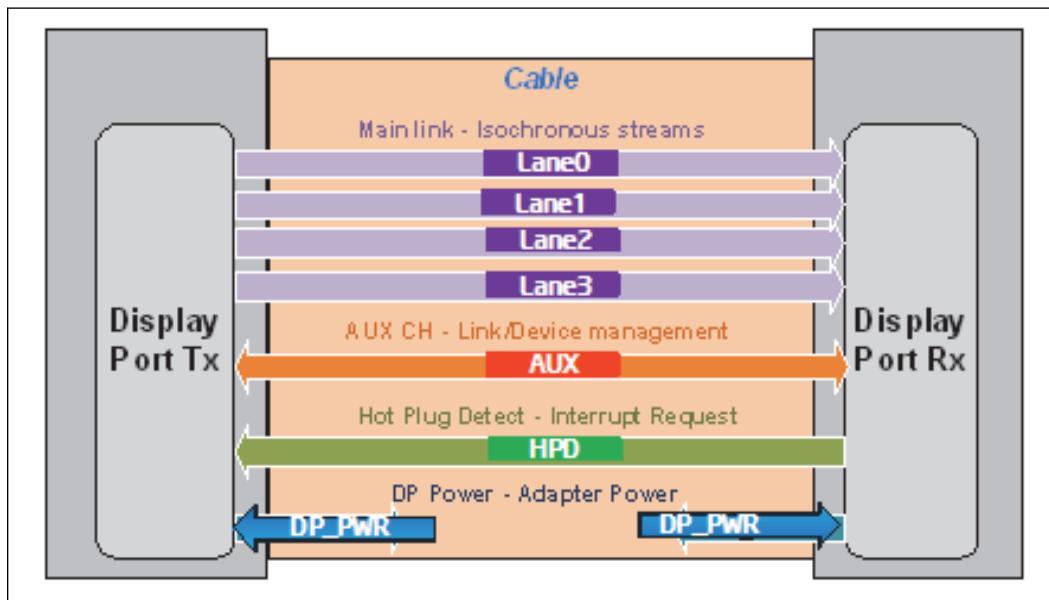
**Table 35. Digital Display Interface Reference Documents**

Title	Document Number/Location
DisplayPort* Standard Version 1.4 Electrical Specification	<a href="http://www.vesa.org">http://www.vesa.org</a>
VESA DisplayPort* Dual-Mode Standard	
High speed internal connector and cable specification	549136

### 5.3.1 DisplayPort\* (DP\*)

#### DisplayPort\* Platform Information

**Figure 51. DisplayPort\* Channels**



**Table 36.** DisplayPort\* Bit Rates

Bit Rate	Lane Supports (Max # of Lanes)	Peak Bandwidth
1.62 Gb/s (RBR)	4	4 x 162 MB/s = 648 MB/s
2.7 Gb/s (HBR)	4	4 x 270 MB/s = 1080 MB/s
5.4 Gb/s (HBR2)	4	4 x 540 MB/s = 2160 MB/s
8.1 Gb/s (HBR3)	4	4 x 810 MB/s = 3240 MB/s

### DisplayPort\* Bit Rates

**Table 37.** Digital Display Interface Reference Documents

Title	Document Number/Location
DisplayPort* Standard Version 1.4 Electrical Specification	<a href="http://www.vesa.org">http://www.vesa.org</a>
VESA DisplayPort* Dual-Mode Standard	
High speed internal connector and cable specification	549136

### DisplayPort\* Signal Descriptions

**Table 38.** DisplayPort\* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx)	DDIx_TXP/N[3:0]	N/A	N/A	1
	TCPx_TX_P/N[1:0] and TCPx_TXRX_P/N[1:0]	N/A	N/A	2
Aux Channel	DDIx_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4
<p><i>Note:</i></p> <ol style="list-style-type: none"> <li>1. Signals names apply for DDI A/B ports.</li> <li>2. Signals names apply for TCP ports.</li> <li>3. Provide good noise isolation, Platform Rdc&lt;0.2 Ohm, require if any DDI implemented.</li> <li>4. Provide good noise isolation, Platform Rdc&lt;0.2 Ohm, require if any TCP implemented.</li> </ol>				

**Table 39. TCP Port Signal Mapping For DisplayPort\***

Description	Signal Mapping	
	DDI	DP++
Main Link (Tx)	TCP_TX0	DP Lane_0
	TCP_TX1	DP Lane_2
	TCP_TXRX0	DP Lane_1
	TCP_TXRX1	DP Lane_3

*Note:* Apply to TCP ports only.

### DisplayPort\* Topology Guidelines

For all topologies, the sink connects to the source via a cable. It is useful to partition the system budgets across the platform components, source, cable assembly and sink to allow different design teams a working budget. The design guide and resulting recommendations were designed to comply with the requirements for DisplayPort\* mid bus probe point TP2 for RBR/HBR. The compliance point for HBR3/HBR2 is TP3\_EQ.

**Table 40. General Guidance for all Topologies**

Description	Recommendation	Value (Units)
AC Capacitor	Select the AC Capacitor values as per DisplayPort* 1.4 Electrical specifications	<b>Main Link:</b> Nominal 100nF recommended (75nF to 265nF including tolerance)  <b>Aux Channel:</b> Nominal 100nF recommended (75nF to 200nF including tolerance)
CMC	Optional. Can use PCB CMC or discrete CMC (e.g., Murata NFP0QHB372HS2).	
ESD	Infineon* ESD102-U4-05L (I/O-to-GND Capacitance <=0.65pF) unless other ESD is specified.	
DP_PWR	DP_PWR provides power to the dongle. It is a 3.3-V rail on pin 20 of the DP connector.	
Inter-pair length mismatch	Maximum length mismatch between the shortest and longest DP* differential pairs for each port is 25mm	
Length Matching between P and N within a diff. pair	Within Layer Max Mismatch: 250um Total Length Max Mismatch: 125um	
Reference Plane (micro-strip)	Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.	
Reference Plane (strip and dual strip line)	Both side can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.	
<i>Note:</i> It is recommended to void unused pads for differential vias, pin pads for CMC, ESD and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.		

### DisplayPort\* HPD General Considerations and Optimization

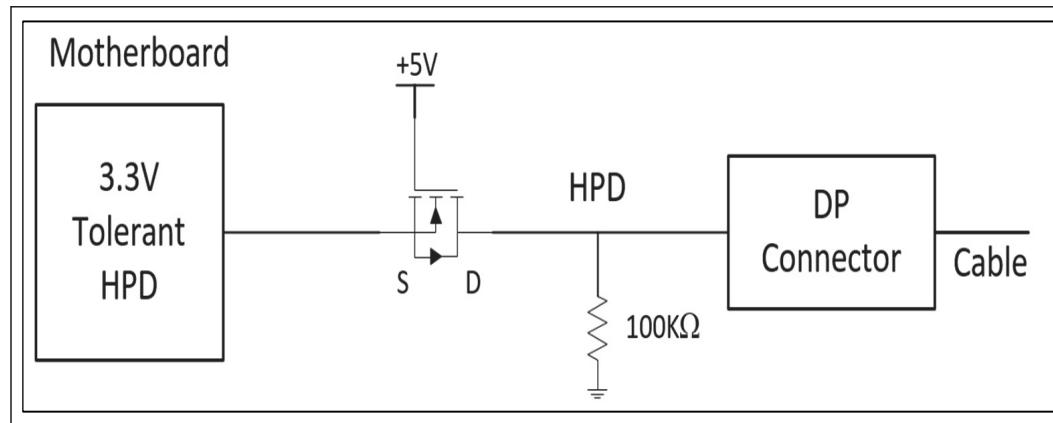
The hot-plug detect output from DisplayPort\* sink device is a 3.3-V active high signal. Since the input on Tiger Lake processor is also 3.3-V tolerant, no inverting level shifter is required on the motherboard. However, a current blocking circuit (for example using

a FET) is required to prevent the back drive current damaging Tiger Lake processor when the source is powered off and sink device is powered on. The following figure shows an example of this implementation.

#### **NOTE**

If the display connector is on the docking station, the hot-plug circuitry should remain on main motherboard and not on the docking station in order to prevent display detection failures related to hot-plug and S-state resume. HPD signal should not be allowed to float anytime.

**Figure 52. DisplayPort\* HPD Pass-gate Design Recommendation**



#### **NOTE**

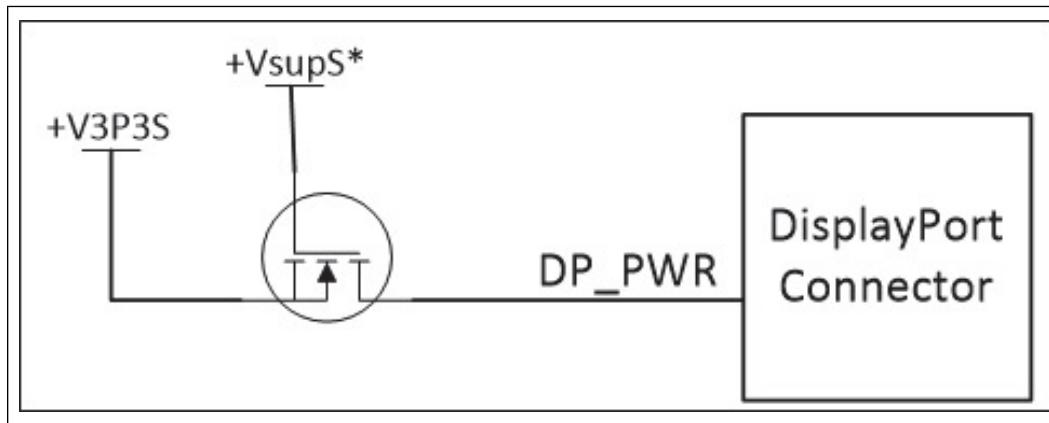
- Select the pass-gate FET which has VGSTH (Gate Threshold voltage) less than 1.5V.
- The 5V supply must turn off when CPU power is turned off.
- On Docking Topology, need to place the HPD circuit on the main motherboard and not in Docking Board.
- Recommend 50 ohm nominal trace impedance with reasonable noise isolation.

#### **DP\_PWR Pin Back Drive Protection**

DP\_PWR pin 20 of DP Connector provides power to the dongle from the platform. Normal DP to DP monitor cable should have this pin as no connect. There are non-compliant cables in the market have them as direct connection. This results in Display monitor back driving current to motherboard and causing system malfunction during power on or when waking-up from sleep state.

To prevent this, add a back driver protection circuit (FET) as shown below for DP\_PWR pin 20 of DP connector.

**Figure 53. DisplayPort\* DP\_PWR pin 20 Back Drive Protection**



#### NOTE

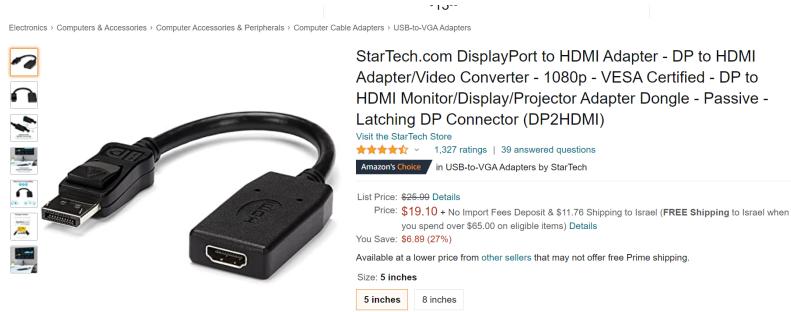
- Connect Gate of n-MOSFET to a power supply which will turn off during sleep state and is higher than 3.3V like +V12S or +V5S.
- Select MOSFET with on resistance less than 0.35 Ohms to meet spec requirement of minimum 2.98V at DP\_PWR pin with 0.5A current.
  - DisplayPort\* Auxiliary Channel (AUX CH) General Design Considerations and Optimization

AUX CH consists of an AC-coupled, bi-directional differential-pair, providing a data rate of 1 Mbps. It is used for link management and device control, that is, for transmitting control and status information.

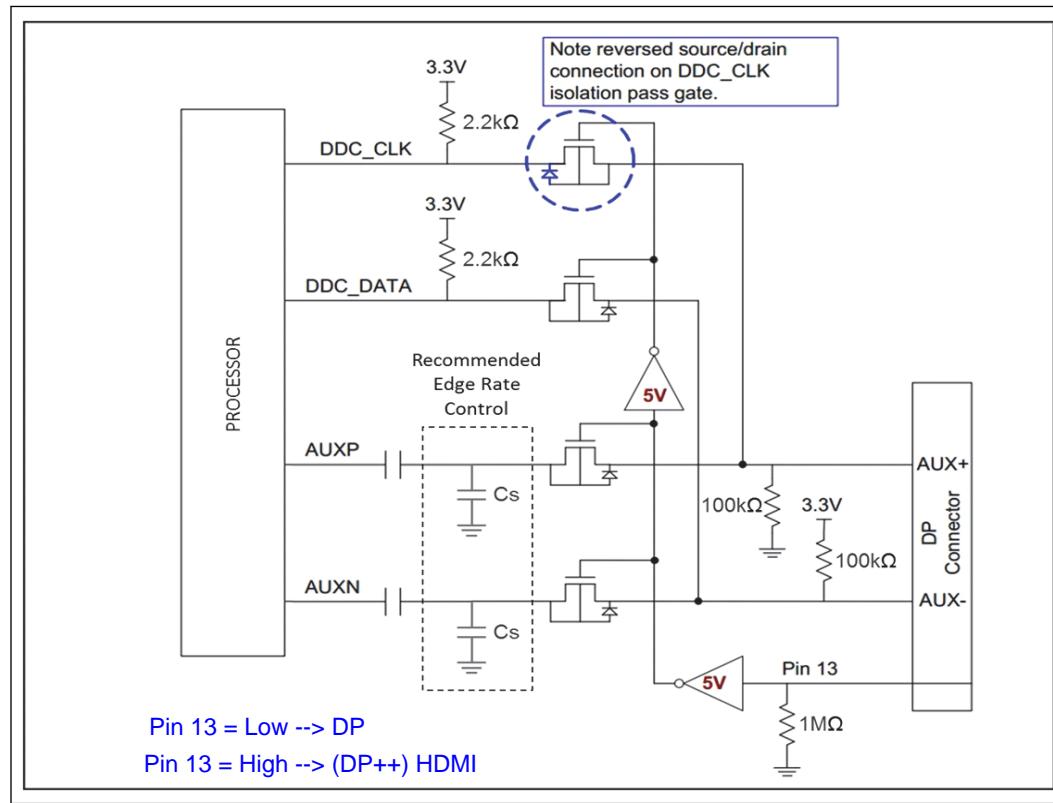
AUX CH is half-duplex and bi-directional. The source device is the master and Sink device is the slave. Manchester II coding is used as the channel coding for AUX CH. Like the Main link the Aux Channel clock is embedded in the data stream.

The sink device may toggle the HPD signal to interrupt the source device.

To support dual mode (DP++) over DisplayPort\* through Dongle for HDMI\*, the circuit shown below is required to be implemented on the motherboard.



Great Adapter. Be aware that this is a PASSIVE adapter. To use this, your device will need to have a dual-mode displayport. Your port MUST be labeled with a "++DP". If you do not see the "++", it is not dual-mode. If you only see "DP", you need an active adapter, which will be a little more expensive. See the attached image of the correct symbol you should see to use this adapter.

**Figure 54. DisplayPort\* Auxiliary Channel Dual Mode Support Protection Circuit****NOTE**

1. The voltage rails specified on the pull up resistors in this circuit should be switched rails that are on during S0 only. However, the two inverters in this circuit should be powered from suspend rails.
2. Devices such as a TTL compatible FET multiplexer/demultiplexer can be used in place of passgate FETs.
3. The leakage current out of the inverter that is close to the DP connector should be minimized since it may affect voltage level to the input of the inverter due to the 1-MΩ pull down resistor.
4. If FETs are used for the passgate circuit, take care to ensure the body diode of the FETs are connected as shown in the figure above. Failure to do so will cause incorrect functionality of the circuit.
5. Recommended edge rate control, a circuit to control crosstalk on SBU for frequencies above 100 MHz and to comply with DP AUX edge rate requirements.
6. Cs Cap Value 100pF.

### 5.3.2 Embedded DisplayPort\* (eDP\*)

#### eDP\* Platform - Specific Important Information

The Embedded DisplayPort\* (eDP\*) channel is used to transport digital display data from the Tiger Lake processor to an embedded DisplayPort\* Panel. Embedded DisplayPort\* (eDP\*) utilizes differential signaling to achieve a high bandwidth bus interface that supports embedded chip-to-chip connections from the Tiger Lake processor. Potential embedded chip-to-chip applications include usage within a laptop PC for driving a panel.

It is recommended that the eDP\*/DP\* standard TP3\_EQ Eye mask requirements are met at the panel side of the mated connector.

eDP\* Main link uses a scrambled 8b/10b encoding scheme for the data stream being transmitted. It allows the clock to be embedded in the data stream.

**Table 41.** eDP\* Bit Rates

Bit Rate	Lane Supports (Max # of Lanes)	Peak Bandwidth
1.62 Gb/s (RBR)	4	4 x 162 MB/s = 648 MB/s
2.7 Gb/s (HBR)	4	4 x 270 MB/s = 1080 MB/s
5.4 Gb/s (HBR2)	4	4 x 540 MB/s = 2160 MB/s
8.1 Gb/s (HBR3)	4	4 x 810 MB/s = 3240 MB/s

**Table 42.** eDP\* Reference Specification

Title	Location
VESA Embedded DisplayPort* Standard - Revision 1.4b	<a href="http://www.DisplayPort.org">http://www.DisplayPort.org</a>

#### eDP\* Signal Descriptions

**Table 43.** eDP\* Signal Groups

Parameters	Signal Mapping		
	Processor	PCH	CRB eDP* Connector
Main Link (Tx)	DDIx_TXP/N_[3:0]	N/A	N/A
Aux	DDIx_AUX_P/N	N/A	N/A
HPD	N/A	DDSP_HPD_x	N/A
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		
DISP_UTILS	Recommend 50Ω nominal trace impedance. Requires level shifting on the platform.		
<b>Note:</b>	x Can be DDIA and/or DDIB.		

**Table 44.** eDP\* Back light Control Signal Mapping

Parameters	PCH Signal Mapping	
	Primary eDP*	Secondary eDP*
VDDEN - Main Power Enable	EDP1_VDD_EN	DISP_MISC_C
BKLT_EN - Backlight Enable	EDP1_BKLT_EN	DDPC_CTRLCLK
BKLT_CTRL - Backlight Control	EDP1_BKLT_CTRL	DDPC_CTRLDATA

### eDP\* Topology Guidelines

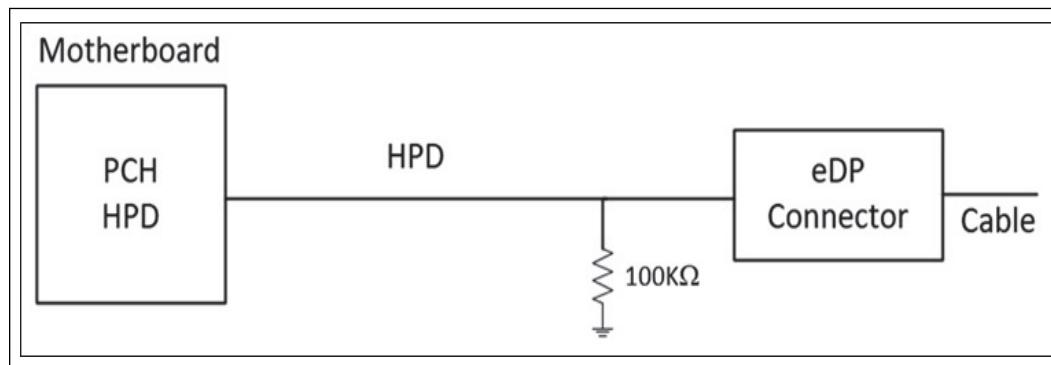
**Table 45.** General Guidance for all Topologies

Description	Recommendation	Value (Units)
AC CAP	AC caps are required to be placed before the motherboard eDP* connector	<b>Main Link:</b> Nominal 100nF recommended (75nF to 265nF including tolerance)  <b>Auxiliary Channel:</b> Nominal 100nF recommended (75nF to 200nF including tolerance)
CMC	Optional. Can use PCB CMC or discrete CMC (e.g., Murata NFP0QHB372HS2).	
Inter-pair length mismatch	maximum length mismatch between the shortest and longest eDP* differential pairs for each port is 25mm	
Length Matching between P and N within a diff. pair	Within Layer Max Mismatch: 250um Total Length Max Mismatch: 125um	
Reference Plane (micro-strip)	Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.	
Reference Plane (strip and dual strip line)	Both side can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.	
<i>Note:</i> It is recommended to void unused pads for differential vias, pin pads for CMC, ESD and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.		

### Embedded DisplayPort\* Hot-Plug Detect Implementation

Hot-plug detect (HPD) is an output from eDP\* sink device and it is an active high signal.

**Figure 55. Embedded DisplayPort\* HPD Signal**



**NOTE**

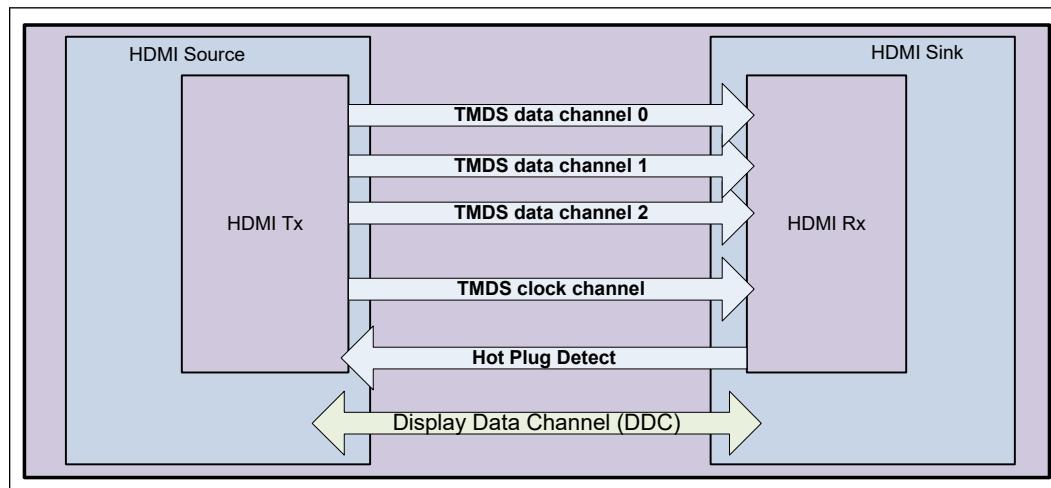
Recommend 50 ohm nominal trace impedance with reasonable noise isolation.

### 5.3.3 HDMI\*

#### HDMI\* Platform-specific Important Information

HDMI\* includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) however CEC is not supported.

**Figure 56. HDMI\* Overview**



## Reference Documents

**Table 46. HDMI\* Reference Documents**

Title	Document Number/Location
High-Definition Multimedia Interface Specification version 2.0a	
High-Definition Multimedia Interface Specification version 1.4b	<a href="http://www.hDMI.org">http://www.hDMI.org</a>
High speed internal connector and cable specification	549136

## HDMI\* Signal Descriptions

**Table 47. HDMI\* Signals**

Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx)	DDIx_TXP/N[3:0]	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	2
DDC	N/A	DDPx_CTRLCLK and DDPx_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

*Note:*

1. Signal names apply for DDI A/B ports.
2. Signal names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

**Table 48. TCP Port Signal Mapping for HDMI\***

Description	Signal Mapping	
	TCP	HDMI
Main Link (Tx)	TCP_TX0	HDMI Data_2
	TCP_TX1	HDMI Data_0
	TCP_TXRX0	HDMI Data_1
	TCP_TXRX1	HDMI CLK

*Note:* Apply to TCP ports only.

**Table 49. DDI Port Signal Mapping for HDMI\***

Description	Signal Mapping	
	DDI	HDMI
Main Link (Tx)	DDI_TX0	HDMI Data_2
	DDI_TX1	HDMI Data_1
	DDI_TX2	HDMI Data_0
	DDI_TX3	HDMI CLK
<i>Note:</i> Apply to DDIA/B ports only		

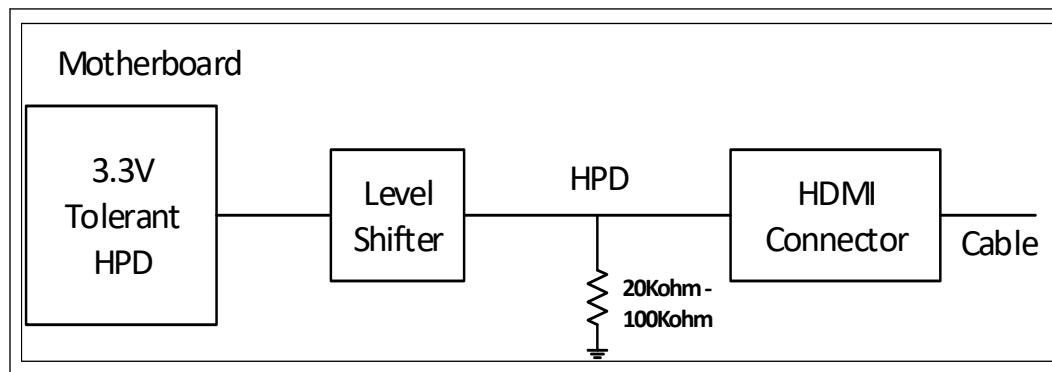
### HDMI\* Topology Guidelines

**Table 50. General Guidance for all Topologies**

Description	Recommendation	
AC CAP	AC caps are required to be placed before the motherboard HDMI* connector	Nominal 100nF recommended (75nF to 200nF including tolerance)
Re-timing Level Shifter	TI SN75DP159 or Parade PS8409A	Disclaimer: The Component guidelines are based on the reference solution used to develop the Platform Design Guide and are provided as a reference only. Intel does not endorse any particular Vendor or component model.
Re-timer Sideband Communication	Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT)	
CMC	Optional. Can use PCB CMC or discrete CMC (e.g., Murata DLP11SA900HL2 with IL<=0.54dB@0.85GHz; 0.8dB@1.5GHz; 1.3dB@3GHz; 3.82dB@6GHz). Populating will not reduce the supported length.	
ESD	Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ≤0.65pF).	
Inter-pair length mismatch	For HDMI*1.4 signals is 25mm For HDMI*2.0 signals is 13mm	
Diff-pair length mismatch	Within Layer Max Mismatch: 250um Total Length Max Mismatch: 125um	
Reference Plane for micro-strip route	Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.	
Reference Plane for strip-line and dual strip-line route	Both side can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.	
<i>Note:</i> It is recommended to void unused pads for differential vias, pin pads for CMC, ESD and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.		

### HDMI\* Hot Plug Detect Topology

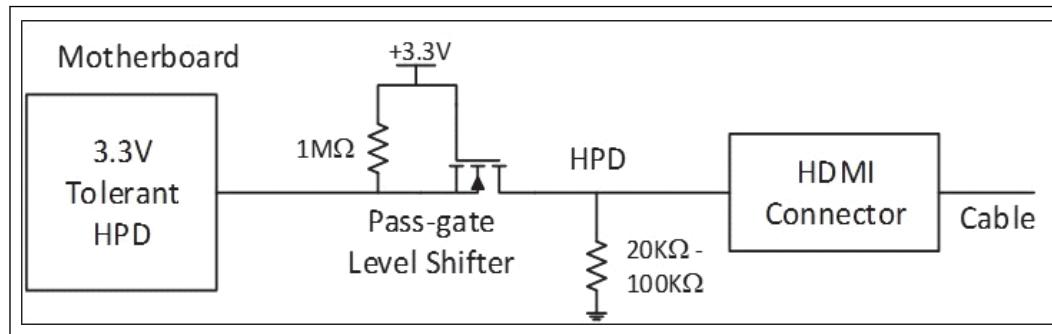
**Figure 57.** HDMI\* Hot Plug Detect Topology



#### NOTE

- Recommend 50 ohm nominal trace impedance with reasonable noise isolation.
- Ensure necessary protection circuitry is in place to prevent back-drive current from damaging the processor when the sink device is powered off.

**Figure 58.** HDMI\* Cost Reduced Hot Plug Detect Topology



#### NOTE

Recommend 50 ohm nominal trace impedance with reasonable noise isolation.

3.3v power supply must be turned off when the CPU power is off.

Ensure necessary protection circuitry is in place to prevent back-drive current from damaging the processor when the sink device is powered off.

### 5.3.4 MIPI DSI (TGL UP3 Port A, TGL UP4 Ports A and B)

#### Signal Descriptions

**Table 51.** MIPI DSI Signal Groups

Parameters	Signal Mapping		
	Processor	PCH	CRB MIPI* Connector
Main Link (Tx) and Aux	DDIA_TXP/N[3]	N/A	DSI0_DATA_P/N[3]
	DDIA_TXP/N[2]		DSI0_Clock_P/N
	DDIA_TXP/N[1]		DSI0_DATA_P/N[2]
	DDIA_TXP/N[0]		DSI0_DATA_P/N[1]
	DDIA_AUXP/N		DSI0_DATA_P/N[0]
	DDIB_TXP/N[3]		DSI1_DATA_P/N[3]
	DDIB_TXP/N[2]		DSI1_Clock_P/N
	DDIB_TXP/N[1]		DSI1_DATA_P/N[2]
	DDIB_TXP/N[0]		DSI1_DATA_P/N[1]
	DDIB_AUXP/N		DSI1_DATA_P/N[0]
Panel 1 Tearing Effect <sup>1</sup>	DISP_UTILS	-	DSI_DE_TE_1
Panel 2 Tearing Effect <sup>1</sup>	DSI_DE_TE_2	-	DSI_DE_TE_2
Panel 1 Reset	-	DDIA_HPD	MIP1_DSI_RST
Panel 2 Reset	-	DDIB_HPD	MIP2_DSI_RST
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, provide good noise isolation, Platform Rdc<0.2 Ohm		
<i>Note:</i>			
1. Recommend 50Ω nominal trace impedance with reasonable noise isolation. Requires level shifting on the platform.			

#### NOTE

MIPI DSI can function as x4 or x8 lanes.

#### Topology Guidelines

**Table 52.** Optimization Table for all Topologies

Description	Recommendation	Value (Units)
CMC	Optional. Can use PCB CMC or discrete CMC (e.g., TDK* TCM0605T, Taiyo Yuden* MCF06052G350-T or equivalent). Refer PCB CMC Technology in Platform Design Guide excelsheet.	
Length Matching between P and N within a diff. pair	Within Layer Max Mismatch: 250um Total Length Max Mismatch: 125um	
Length Matching between DPHY clock and data	MB: Within 1000um CRD + X'fer + Cable + Connectors: Within 1000um	

*continued...*

Description	Recommendation	Value (Units)
Reference Plane for micro-strip route	Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.	
Reference Plane for strip-line and dual strip-line route	Both side can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.	
<i>Note:</i> Recommend that each DPHY configuration (for example: x4) will be routed on the same layer.		

**Table 53. DSI\* Back light Control Signal Mapping**

Parameters	PCH Signal Mapping	
	1st DSI*	2nd DSI*
VDDEN - Main Power Enable	EDP1_VDD_EN	GPPC_A17_DISP_MISC_C
BKLT_EN - Backlight Enable	EDP1_BKLT_EN	GPPC_A21_DDPC_CTRLCLK
BKLT_CTRL - Backlight Control	EDP1_BKLT_CTRL	GPPC_A22_DDPC_CTRLDATA
MIPI secondary power enable AVEE	DDPA_CTRLCLK	DDPB_CTRLCLK
MIPI Secondary power enable AVDD	DDPA_CTRLDATA	DDPB_CTRLDATA

### 5.3.5 Digital Display Interface Termination Guidelines

#### Disabling and Termination Guidelines

**Table 54. Disabling and Termination Guidelines**

Pin name	Recommendation
DDIx_TXN/P[3:0]	No connect
DDIx_AUXN/P	No connect
DDIx_HPD	Pull down to ground via 100k Ω resistor
DDIA_RCOMP	Pull Down to VSS via 150 Ohm resistor.
DISP_UTIL / DSI_DE_TE_1	No connect
DSI_DE_TE_2	100K Ohm to ground.

### 5.3.6 Hybrid Graphics

Microsoft\* Hybrid Graphics definition includes the following:

- The system contains a single integrated GPU and a single discrete GPU.
- It is a design assumption that the discrete GPU has a significantly higher performance than the integrated GPU.
- Both GPUs shall be physically enclosed as part of the system.
  - MS Hybrid DOES NOT support hot-plugging of GPUs
  - OEMS should seek further guidance from MS before designing systems with the concept of hot-plugging
- Starting with Th1 (WDDM 2.0), a previous restriction that the discrete GPU is a render-only device, with no displays connected to it, has been removed. A render-only configuration with NO outputs is still allowed, just NOT required.

It must be noted that systems that have outputs available off of the discrete GPU will NOT support previous versions of the OS (Windows 8.1 and Older).

Microsoft\* Windows 10 operating system enables the Windows 10 Hybrid graphics framework wherein the GPUs and their drivers can be simultaneously utilized to provide users with the benefits of both performance capability of discrete GPU (dGPU) and low-power display capability of the processor GPU (iGPU). For instance, when there is a high-end 3D gaming workload in progress, the dGPU will process and render the game frames using its graphics performance, while iGPU continues to perform the display operations by compositing the frames rendered by dGPU.

Each vendor [Intel as the vendor of integrated GPU / 3rd Party Graphics Vendor / Microsoft] is responsible for their own component, and Microsoft owns the overall implementation including all Hybrid Graphics related documentation and guidance.

Hybrid Graphics has requirements which determine support on different platforms and these requirements may be different between versions of OS. Refer Microsoft documentation for detailed requirements per OS version.

The iGPU device is configured as the primary display adapter driving the embedded or local flat panel of the device. If dGPU is designated to drive the internal display, it gets configured as primary display adapter. In this scenario, and when there is no external display driven by iGPU, the system ceases to qualify as a hybrid graphics, and it rather behaves like any discrete graphics system where the capabilities of iGPU is not utilized.

Having a system configured where both iGPU and dGPU are driving displays needs to be carefully evaluated especially if there is difference in display capabilities of the two graphics adapters that would lead to user confusion or bad UX.

## 5.4

### MIPI CSI-2

MIPI\* CSI-2 is the primary Camera data interface. TGL UP4 supports up to 6 concurrently connected cameras over CSI, TGL UP3 supports up to 4 concurrently connected cameras over CSI, each camera may have a different lane width (x1, x2 or x4 DPHY lanes).

**Table 55.**

**Reference Specification**

Title	Location
MIPI* CSI-2 Specifications	<a href="http://www.mipi.org/specifications/camera-interface">http://www.mipi.org/specifications/camera-interface</a>
I2C Specifications	<a href="http://www.i2c-bus.org/">http://www.i2c-bus.org/</a>
Camera IPU6 Software Integration Guide	613944
IPU6 System Design Guide	619820

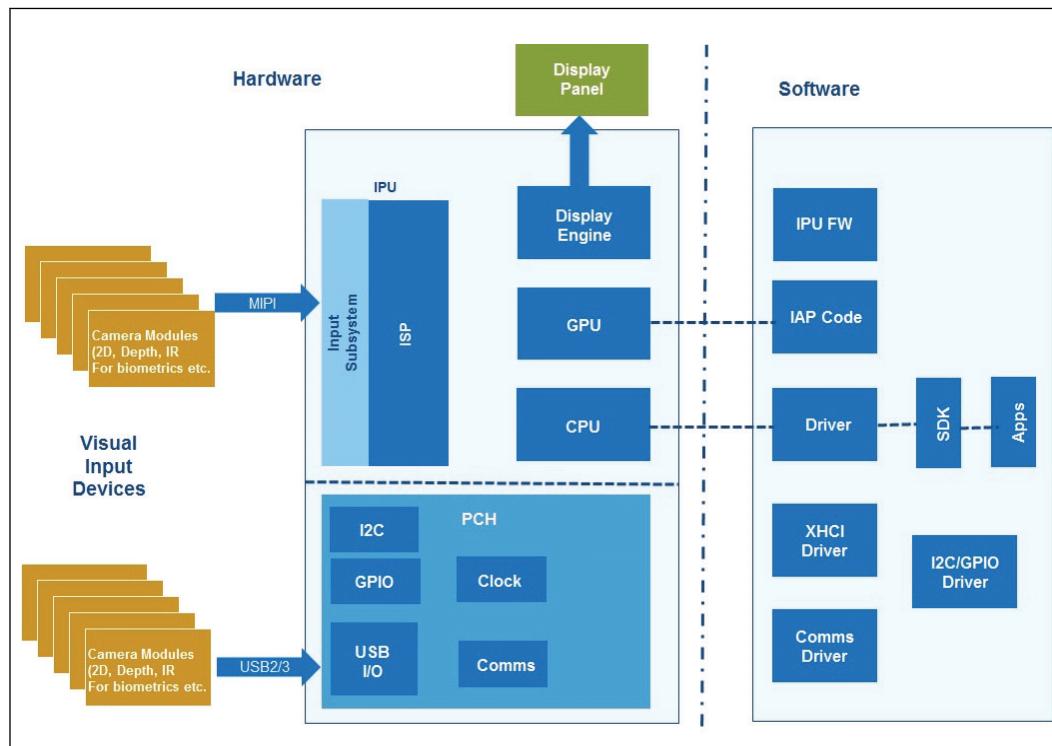
#### 5.4.1

#### CSI-2 Platform Specific Information

For TGL UP4 the platform only has 42 DPHY (Data + Clocks) pins.

For TGL UP3 the platform only has 32 DPHY (Data + Clocks) pins.

The below diagram illustrates the different possible cameras and solutions to be supported on Tiger Lake along with the connection to SoC.

**Figure 59. Visual Computing System Components Block Diagram**

#### 5.4.2 CSI-2 Lane Configurations

**Table 56. CSI-2 Lane Allocation Table**

Ball Name	Main Configuration	Cfg	Second Configuration	Cfg
CSI_B_DP[3]	B_DP[3]	X4	B_DP[3]	X4
CSI_B_DN[3]	B_DN[3]		B_DN[3]	
CSI_B_DP[2]	B_DP[2]		B_DP[2]	
CSI_B_DN[2]	B_DN[2]		B_DN[2]	
CSI_B_DP[1]	B_DP[1]		B_DP[1]	
CSI_B_DN[1]	B_DN[1]		B_DN[1]	
CSI_B_DP[0]	B_DP[1]		B_DP[1]	
CSI_B_DN[0]	B_DN[1]		B_DN[1]	
CSI_B_CLK_P	B_CLK_P		B_CLK_P	
CSI_B_CLK_N	B_CLK_N		B_CLK_N	
CSI_C_DP[3]	C_DP[3]	X4	C_DP[3]	X4
CSI_C_DN[3]	C_DN[3]		C_DN[3]	
CSI_C_DP[2]	C_DP[2]		C_DP[2]	
CSI_C_DN[2]	C_DN[2]		C_DN[2]	

*continued...*

Ball Name	Main Configuration	Cfg	Second Configuration	Cfg
CSI_C_DP[1]	C_DP[1]		C_DP[1]	
CSI_C_DN[1]	C_DN[1]		C_DN[1]	
CSI_C_DP[0]	C_DP[0]		C_DP[0]	
CSI_C_DN[0]	C_DN[0]		C_DN[0]	
CSI_C_CLK_P	C_CLK_P		C_CLK_P	
CSI_C_CLK_N	C_CLK_N		C_CLK_N	
CSI_E_CLK_P	Not Used	-	E_CLK_P	X2
CSI_E_CLK_N		-	E_CLK_N	
CSI_E_DP[1]	E_DP[1]	X4	E_DP[1]	X2
CSI_E_DN[1]	E_DN[1]		E_DN[1]	
CSI_E_DP[0]	E_DP[0]		E_DP[0]	
CSI_E_DN[0]	E_DN[0]		E_DN[0]	
CSI_F_DP[1]	F_DP[1]	X4	F_DP[1]	X2
CSI_F_DN[1]	F_DN[1]		F_DN[1]	
CSI_F_DP[0]	F_DP[0]		F_DP[0]	
CSI_F_DN[0]	F_DN[0]		F_DN[0]	
CSI_F_CLK_P	F_CLK_P		F_CLK_P	X2
CSI_F_CLK_N	F_CLK_N		F_CLK_N	

**Table 57. Additional CSI-2 Lane Allocation Table (TGL UP4 Only)**

Ball Name	Main Configuration	Cfg	Second Configuration	Cfg
CSI_G_DP[1]	G_DP[1]	X2	G_DP[1]	X2
CSI_G_DN[1]	G_DN[1]		G_DN[1]	
CSI_G_DP[0]	G_DP[0]		G_DP[0]	
CSI_G_DN[0]	G_DN[0]		G_DN[0]	
CSI_G_CLK_P	G_CLK_P		G_CLK_P	
CSI_G_CLK_N	G_CLK_N		G_CLK_N	
CSI_H_DP[0]	Not Used	-	H_DP[0]	X1
CSI_H_DN[0]		-	H_DN[0]	
CSI_H_CLK_P		-	H_CLK_P	
CSI_H_CLK_N		-	H_CLK_N	

### 5.4.3 CSI Signal Descriptions

Name	Type	Description
CSI_B_DP]3[ CSI_B_DN[3] CSI_B_DP[2]	I	MIPI* CSI-2 Data
<i>continued...</i>		

Name	Type	Description
CSI_B_DN[2] CSI_B_DP[1] CSI_B_DN[1] CSI_B_DP[0] CSI_B_DN[0] CSI_C_DP[3] CSI_C_DN[3] CSI_C_DP[2] CSI_C_DN[2] CSI_C_DP[1] CSI_C_DN[1] CSI_C_DP[0] CSI_C_DN[0] CSI_E_DP[1] CSI_E_DN[1] CSI_E_DP[0] CSI_E_DN[0] CSI_F_DP[1] CSI_F_DN[1] CSI_F_DP[0] CSI_F_DN[0]		
CSI_F_CLK_P CSI_F_CLK_N CSI_B_CLK_P CSI_B_CLK_N CSI_C_CLK_P CSI_C_CLK_N CSI_E_CLK_P CSI_E_CLK_N	I	MIPI* CSI-2 Clock
CSI_G_DP[1] CSI_G_DN[1] CSI_G_DP[0] CSI_G_DN[0] CSI_H_DP[0] CSI_H_DN[0]	I	MIPI* CSI-2 Data (TGL UP4 Only)
CSI_H_CLK_P CSI_H_CLK_N CSI_G_CLK_P CSI_G_CLK_N	I	MIPI* CSI-2 Clock (TGL UP4 Only)
CSI_RCOMP	I	External Reference (150Ohm +/- 1% to GND)
<i>Note:</i> Polarity (P/N) cannot be reversed.		

## 5.4.4 CSI DPHY Topology Guidelines

### General Topology Guidelines:

1. CSI\_RCOMP  $150\Omega \pm 1\%$  pull down to GND to provide good noise isolation.  
assuming platform  $R_{dc} < 0.5\Omega$ .

2. Each DPHY configuration (ex: X4) should be routed on same layer.
3. Length Matching between P and N within a DPHY diff. pair:
  - a. Within Layer Max Mismatch: 0.25mm
  - b. Total Length Max Mismatch: 0.125mm.
4. Length matching between DPHY clock and data:
  - a. Board: within 1mm
  - b. Board: within 1mm
    - For Cable + Connectors: within 1mm
5. It is recommended to use Common Mode Choke (CMC) and it should be located near the sensor, however simulation results don't include CMC.
6. Mcable can be either coax or FPC cable (Flexible Printed Circuit Board)
7. Refer to the IPU4P Design guide for more information.

## 5.5

### Processor PCIe Interface

The TGL UP3/UP4 processor PCI Express\* interface is a 4-lane (x4) port. The interconnect between the TGL UP3/UP4 processor and NVMe storage or dGFX provided through the M.2 connector or device down.

#### Hybrid Intel® Optane™ Memory Support

Hybrid Intel® Optane™ memory devices such as Teton Glacier, are required to be supported by the platform as a PCIe 2x2 device. The Tiger Lake processor does not support PCIe 2x2 configurations. M.2 connectors that are intended for use with hybrid Intel® Optane™ memory devices, should be connected to PCH ports that support a PCIe 2x2 configuration. Please refer to the appropriate *PCH External Design Specification (EDS)* for more details of how the PCIe ports are configured.

Additional design guidelines and other system integration information about hybrid Intel® Optane™ memory can be found in the *Intel® Optane™ Memory H10 Teton Glacier System Integration Guide* (# 596835) and well as in the *Intel Teton Glacier Storage Support with Multiplexed CPU PEG and PCH PCIe3\*on Single M.2* whitepaper (# 626037).

**Table 58.**

#### Compliance Documents

Title	Doc# / Location
PCIe Base Specification Rev 4.0	<a href="http://www.pcisig.com">www.pcisig.com</a>

#### Signals Description

**Table 59.**

#### PCI Express\* Signal Groups

Signal Group	Signal Name	Description
Input PCI Express*	PCIE4_RX_P[3-0] PCIE4_RX_N[3-0]	PCI Express* Receive Differential Pair
Output PCI Express*	PCIE4_TX_P[3-0] PCIE4_TX_N[3-0]	PCI Express* Transmit Differential Pair
COMP	PCIE4_RCOMP_P	PCI Express* Compensation

*continued...*

Signal Group	Signal Name	Description
	PCIE4_RCOMP_N	

Note: Customer can use PCH CLKOUT\_SRC\_P [4, 3, 0] clock out signals for PCIe gen4.

## 5.5.1 General Routing Guidelines

### Reference Planes

Referencing signals going over a board-to-board connector must be considered and stitching capacitors added at the connector as appropriate. For example, if a differential-pair is GND-referenced on the motherboard and the pair is  $V_{CC}$  referenced on the daughter card, then stitching capacitors must be added at the connector between  $V_{CC}$  and GND.

### Lane to Controller Allocation

The PCIe x4 has 4 physical lanes that cannot be configured.

### PCI Express Lane Polarity Inversion

The PCI Express\* Base Specification requires polarity inversion to be supported independently by all receivers across a Link where each differential pair within each Lane of a PCIe Link handles its own polarity inversion. Polarity inversion eliminates the need to untangle a trace route to reverse a signal polarity difference within a differential pair and no special configuration settings are necessary to enable it.

---

#### NOTE

The polarity inversion does not imply direction inversion or direction reversal; that is, the Tx differential pair from one device must still connect to the Rx differential pair on the receiving device, per the PCIe Base Specification.

---

### Static Lane Reversal Support

The Processor has a strap pin that allow the root port supports static lane reversal. BIOS reference code may not fully support preset search algorithm on systems with lane reversal on PCIe\* ports. BIOS will fully support GEN 3 and GEN4 by use of presets programmed at customer discretion with Intel guidance. The target for the lane reversal support is to ease mother board layout. Card layout is not supported and should be handled by downstream device. Please check EDS for the configuration.

**Table 60. PCIe\* Configurations**

Interface	Configuration	PCIe* Slot Clock
PCIe x4	1x4	Customer can use any of the available clock out signals. For example, CLKOUT_SRC_P/N was used on RVP.

## 5.5.2 Processor PCIe TX EQ Tuning

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#### NOTE

Latest version (Rev 1.2.010) of the IOMT tool has the new capability to tune end-point Cp/Cm parameters.

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Outcome of this tool are Cp/Cm parameters. These parameters will be asked by the endpoint during Phase 3 of the training that needs to be updated in the BIOS for the far end Tx (End point Tx) which will improve PCIe Rx margins. This tool primarily needs to be run for a specific platform as channel is the major contributor and end point is the minor contributor for the far end Tx preset to change. For example: If a customer has three platform designs with 4 inch /6 inch/8 inch routing length, we highly recommend them to run this tool on 3 platforms independently but if each platform has several end point configurations and the combination turns out to be a large number in that case it is ok to run any one end point per platform design.

### 5.5.3

#### Modern Standby - PCIe D3cold Enabling

Each PCIe end point device link state should be at L2 or deeper to enable platform S0 idle states deeper than S0i2.0 or S0i3.0. Implementing PCIe end point device D3cold is required to enable its link state to enter L2 or deeper. PCIe Device Power Management D3cold state is where all core power is removed from end point device, and any auxiliary power is only supplied if the device is enabled to generate a wake event. Core power removal is controlled by the platform via external power controls, typically power FETs, and may be required to limit power consumption of PCIe NVMe Storage Devices; otherwise higher than expected device power could be observed with D3cold.

For complete D3cold hardware, software, and motherboard (PERST#, Wake#, device VDD\_Core, and device VDD\_Aux) recommendations reference the following material and consult your PCIe device vendor(s) for their D3cold required implementation and power consumption:

1. Tiger Lake Platform Runtime D3 (RTD3) Hardware and Software Recommendations Design Guide (Document 576056)
2. SLPS0 Design and Debug Checklist (#570300)

### 5.5.4

#### Slot Reset Implementation

AND gate implementation (with inputs –PLTRST# and PCH GPP) should be used for resetting PEG slots. This circuit provides an option to reset PEG slots using BIOS-controlled GPP\_F22 during debug, without resetting the entire platform.

A jumper should be added near the PEG slots to select between the PLTRST# directly OR the ANDed output of PLTRST# and GPP. GPP should follow same routing guidelines as platform reset.

The BIOS needs to ensure that GPP is configured as output high for normal operation. This circuit will take effect and reset PEG slots only when GPP is driven low.

PCIe\* Gen4 margining and functional link training can occasionally hang PEG devices (slots or down). To ensure proper system functionality, Intel recommends implementing a circuit that allows the BIOS to reset the PEG device, independent of PLTRST#. The reference circuit on the RVP uses GPP to control the auxiliary reset circuit, but the BIOS Reference Code allows a different GPIO to be used, if necessary for the system design flexibility. Unless necessary, customers are advised to use the default GPIO selection. Equivalent reset circuits are also acceptable. The auxiliary reset circuit is only required for PCIe\* Gen4 implementations.

### 5.5.5 Debug Guidelines

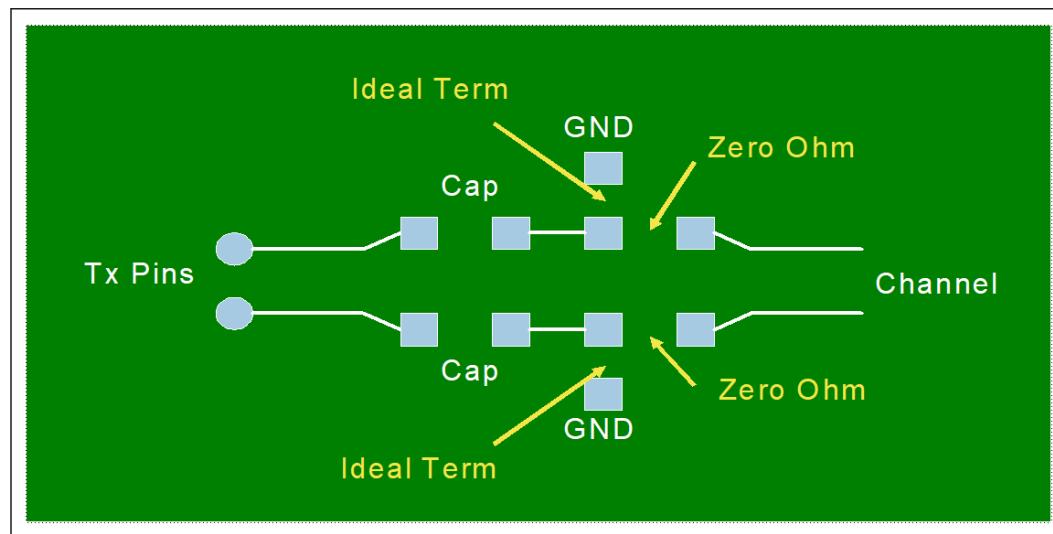
The inclusion of test points and probing structures may impact the loss and jitter budgets of a PCI Express\* interconnect. In general, test points and probe structures should not introduce stubs on the differential pairs or cause significant deviation from the recommendations given throughout this chapter. Existing vias, pads or pins should be used wherever possible to accommodate such structures. Careful consideration must be taken whenever additional probing structures are used.

#### Probe Points for Testing Soldered Down PCI Express\* Devices

In order to actively characterize the transmit path signal quality for a soldered down PCI Express\* device, there must be a terminated probing point on the motherboard very near the soldered down device. This probing point may affect the overall signal quality of the system during normal operation due to the effects of stubs and impedance mismatches of the traces themselves.

The probing point requires populating a resistor stuffing option that can be used to break the path to the device very near the device pins and ideally terminate each line (TX+/TX-) to ground through a  $50\ \Omega$  1% resistor. Also, an AC coupling capacitor is required near the device pins. The resistor package/footprint must be as small as possible, preferably size 0402. The population of a  $50\text{-}\Omega$  resistor, as shown in the figure below, will force the transmitting silicon (host or add-in card) to enter the compliance mode and begin transmitting the compliance packet. The population of two  $0\text{-}\Omega$  resistors will allow normal operation of the device. One replace the AC coupling cap, the other connects the channel.

**Figure 60. Board Preparation Example**



### 5.6 Asynchronous and Sideband Signals

This section describes the topologies and layout recommendations for the asynchronous signals. Refer to the Tiger Lake processor EDS for more details.

---

**NOTE**

If a section/paragraph/table/figure/- Note is applicable to both UP3 and UP4 platforms, it is not explicitly called out. If a section/paragraph/table/figure/- Note is specific to UP3 or UP4 platform only, it will be called out.

---

**5.6.1****Asynchronous and Sideband Signals Topology Guidelines**

This section describes topologies and layout recommendations for the legacy signals. Although these signals toggle with relatively low frequency, most of them have very high-edge rates.

Inappropriate routing or lack of termination can seriously decrease signal quality and lead to electrical specification violations and even logical system failures. The following guidelines apply to all legacy signals described in this section.

- Watch for termination recommendations. If any of the signals that require motherboard termination are pulled-up to a voltage higher than VCCST, the reliability and power consumption of the Tiger Lake processor may be affected. Therefore, it is very important to follow the recommended pull-up voltage for these signals.
- For Type 3 PCB, routing guidelines allow the asynchronous signals to be routed as either microstrip using  $50 \Omega \pm 15\%$  characteristic trace impedance or stripline using  $50 \Omega \pm 10\%$  characteristic trace impedance or orthogonal DSL (with only one layer of parallel routing, the routing on the second, adjacent layer, must be orthogonal to the first one) using  $50 \Omega \pm 10\%$  characteristic trace impedance.
- For Type 4 PCB, routing guidelines allow the asynchronous signals to be routed as either microstrip using  $50 \Omega \pm 15\%$  characteristic trace impedance or orthogonal dual - stripline using  $50 \Omega \pm 12\%$  characteristic trace impedance.
- Changing reference plane is not recommended and may cause signal integrity degradation. In any case, if such routing cannot be avoided, use stitching vias and bypass capacitors between the reference planes near the layer transition.
- General trace spacing requirements (for  $50 \Omega$  characteristic impedance traces) specified in the following table. W is trace width and S is the space between 2 adjacent traces.

**Table 61. Asynchronous and Sideband Signal General Routing Guideline**

Trace Type	Stack-up (MS/SL/DSL)	Minimum Spacing (S)	
		Value	Units
Microstrip	MS	300	μm
Stripline	SL	300	μm
Dual-Stripline	DSL	300	μm
Microstrip PECI	MS1	450	μm
Microstrip SVID	MS1,3	380	μm

*Note:*

1. Parameters for SVID Bus and PECI microstrip routing only.

*continued...*

Trace Type	Stack-up (MS/SL/DSL)	Minimum Spacing (S)	
		Value	Units
2.	The main route segments (M) of the asynchronous signals listed below are expected to follow the spacings mentioned in the table above while breakin (BI) and breakout (BO) segments are expected to have 0.1mm spacing to adjacent signals.		
3.	Additional spacing guidelines in SVID Protocol Specification Doc # 456098.		

## 5.6.2 PROCHOT# Topology

The signal can be driven either by the Tiger Lake processor, Embedded Controller (EC) or by VR. If connected from PROCHOT# to particular manufacturer temp sensor and not VR as described in the topology, such PROCHOT# connection must have the drive capabilities as defined in the future available VR specification.

Consider the following:

1. PROCHOT# is capable of toggling hundreds of times per second to signal a hot temperature condition.
2. If PROCHOT# is not used, then it must be terminated with a  $1\text{K}\Omega \pm 5\%$  pull-up resistor to VCCSTG.

The EC output DC levels are typically 0 V and 3.3 V, Tiger Lake processor input DC levels are 0 V and 1.0 V. Tiger Lake processor's high voltage level is lower than EC's high voltage level, therefore an onboard voltage level shifter is required. An inverting logic level shifter must be used. EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the Tiger Lake processor side PROCHOT# low.

- An Agent is any (OD) driver that is connected to the PROCHOT# signal, for example VR.
- R1-6 series resistors are needed to keep the PROCHOT# signal at safe level (reduce Under-shoot) if an Agent and/or Inv OD pull-down resistor is too low (driver is too strong). The total pull-down resistance of each agent should be between 75 and  $200\Omega$ . Total pull-down resistance is defined as the sum of internal pull-down resistance of the agent and the series resistor  $R_i$
- Examples:
  - If internal pull-down resistor of Agent1 is  $75\Omega$ , no additional (on board.) series resistor is needed,  $R_1$  can be omitted.
  - If internal pull-down resistor of Agent2 is  $15\Omega$ , additional (on board) series resistor is needed to increase the total pull-down resistance of Agent2,  $60 < R_2 < 185$  ( $R_2$  can be  $70\Omega$ ).
  - The same applies to the Inv OD driver of the EC.

## 5.6.3 CATERR# Topology

CATERR# indicates system has experienced a catastrophic error and cannot continue to operate. The Tiger Lake processor will set this for non-recoverable machine check errors and other internal unrecoverable errors. CATERR# is an asynchronous open drain driver signal with no on-die termination (ODT). This signal can be connected to a LED if desired. Also, this signal should have an exposed test point for easy debug access and have a  $1\text{K}$  ohm pull-up to VCCST.

## 5.6.4 VCCST\_PWRGD Topology

VCCST\_PWRGD is a signal on the Tiger Lake processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specifications.

VCCST\_PWRGD is only 1.0 V tolerant. If a dedicated driver is used to drive the VCCST supply, the VCCST\_PWRGD should meet the requirements listed below:

- VCCST\_PWRGD must be valid (stable at the right level) during all power states when there is a power applied to the VccST power supply.
- VCCST\_PWRGD must be de-asserted before VDDQ or VCCST power level goes below voltage tolerance specification.

## 5.6.5 VCCSTPWRGOOD\_TCSS Topology

VCCSTPWRGOOD\_TCSS is a new input signal on the Tiger Lake processor that is asserted when the USB-C\* Subsystem requires keeping VCCST supply on, even when entering S3-S5 states.

This signal starts low and may change polarity only at the entry to S3-S5 states. If required to toggle, the signal level must always change before de-assertion of VCCST\_PWRGD signal at the Sx entry flow. This signal should have a valid level during S0-S5 power states.

TCSS gets a dedicated power-good signal VCCST\_PWRGOOD\_TCSS that is derived from a PCH signal called VCCST\_OVERRIDE. This is used in S5 state when Complete CPU in Reset but the TCSS logic active.

If a dedicated driver is used to drive the VCCST supply, the VCCSTPWRGOOD\_TCSS should meet the same requirements as VCCST\_PWRGD.

## 5.6.6 THERMTRIP# Topology

RLS series resistor is needed to keep the THERMTRIP# signal at safe level (reduce Under-shoot) if OD LS pull-down resistor is too low (driver is too strong). The total pull-down resistance of OD LS should be between 55 and 200Ω. Total pull-down resistance is defined as the sum of internal pull-down resistance of the OD LS and the series resistor RLS.

Examples:

- If internal pull-down resistor of OD LS is 55Ω, no additional (on board) series resistor is needed => RLS can be omitted.
- If internal pull-down resistor of OD LS is 15Ω, additional (on board) series resistor is needed to increase the total pull-down resistance of OD LS in range: 40 < RLS < 185, in order to meet the guideline: 55 < RLS + RODLS < 200.

## 5.6.7 Platform Environmental Control Interface (PECI) Topology

The digital thermometer will be used to communicate Tiger Lake processor core temperature to the platform. Access to the digital thermometer is through the Platform Environmental Control Interface (PECI).

The PECI interface is a controlled one-wire bi-directional signal which is used to communicate the temperature of the Tiger Lake processor digital thermometer to the PECI host controller or to monitor and control the Tiger Lake processor information.

such as energy, power limits, status and DDR temperature. Refer to the Processor Platform Environment Control Interface (PECI) Implementation Guide Doc#554767 for commands for firmware coding.

If a different PECI topology is implemented or one of the agents does not meet the PECI 3.1 Specifications, a simulation must be performed to ensure adequate signal quality and maximal operating frequency.

PECI specification has the bus in a L level when there are no transactions happening. The PECI host would normally drive the line H to start transactions, and the PECI clients (aka CPU) respond by overdriving and keeping the line H when the Host tried to drive L. Only the PECI host drives the bus L, Clients can only pull up.

If there is no PECI host talking to the CPU and the pin is unused, put a 200-400ohm PD resistor to GND on the CPU pin to make sure it is statically L. it is not recommend to tie the CPU pin directly to GND.

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**NOTE**

PECI routing guidelines were validated up to a host bandwidth of 1.6 Mbps.

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**Intel Recommends using PECI Bus.**


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**NOTE**

If PECI is not used, then it should be terminated to GND with 200-400ohm resistor.

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**NOTE**


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- The VREF\_PECI\_EC voltage reference from the Processor to the EC should be connected to VCCST (PECI reference voltage).
  - For TGL UP4 connect to VCCST\_OUT.
- 

**NOTE**

If PECI is not used on the CPU, then it should be terminated to GND with 200-400ohm resistor;

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## 5.6.8

## BPM#[3:0] Topology

Route the BPM#[3:0] signals point-to-point from the Tiger Lake processor pin to the LTB debug port connector. Adequate termination for these signals is provided within the Tiger Lake processor EDS and on the LTB hardware. No external components are required.

Refer Tiger Lake processor EDS and Primary Debug Port - Observation Pins Routing Guidelines for more information.

## 5.6.9 SVID Topology

### NOTE

For additional information regarding SVID and power management refer to [Power Delivery](#) on page 376 in this document and SVID protocol specification Doc ID #456098.

## 5.6.10 COMP Signals

Refer to Tiger Lake Processor External Design Specification (EDS) Volume 1 of 2 ( 575683) for termination requirements for all COMP signals.

## 5.6.11 ESD Protection for Asynchronous Signals

Asynchronous signals are not subject to signal integrity issues but could be victims of ESD events resulting in catastrophic system failures. Therefore, some of them deserve extra care during board routing: good referencing from top or bottom layer, placement of noise filters, no exposure to the edges of a board.

## 5.7 CFG Signals Functionality and Termination

**Table 62. CFG Signals Functionality and Termination**

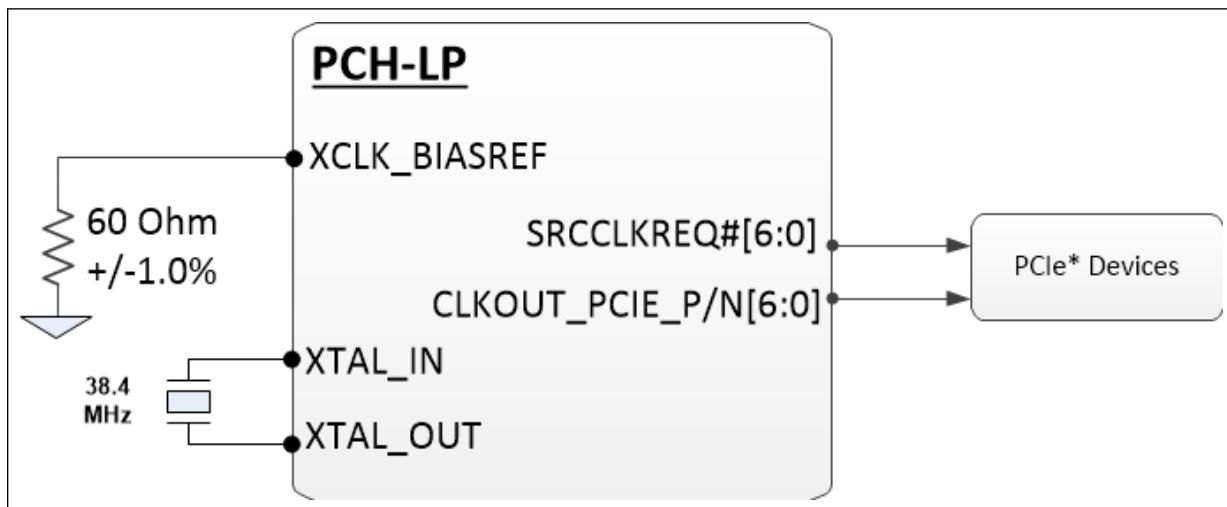
CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	1K ohm
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15 ]	RSVD	None	

## 6.0 PCH IOs

### 6.1 Platform Clock Design Guidelines

#### 6.1.1 Interface Details

**Figure 61. Clock Integration Distribution Diagram**



#### 6.1.2 Signal Descriptions

**Table 63. Platform Clocks and Associated Signal Details and Descriptions**

Signal Name	Type	SSC Capable	Description
PCH-LP (UP3): <ul style="list-style-type: none"> <li>• CLKOUT_PCIE_P [6:0]</li> <li>• CLKOUT_PCIE_N [6:0]</li> </ul> PCH-LP (UP4): <ul style="list-style-type: none"> <li>• CLKOUT_PCIE_P[4:0]</li> <li>• CLKOUT_PCIE_N[4:0]</li> </ul>	O	Yes	PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices <ul style="list-style-type: none"> <li>• CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support</li> <li>• CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support</li> </ul> Any un-used CLKOUT_PCIE_P/N differential pair not being routed on a platform should be configured as "Disabled" through the Intel® Flash Image Tool (FIT) tool. The CLKOUT_PCIE_P/N differential pairs are called out as CLKOUT_SRC differential outputs in FIT as discussed in the SPI Programming Guide.
PCH-LP (UP3): <ul style="list-style-type: none"> <li>• SRCCCLKREQ#[6:0]</li> </ul> PCH-LP (UP4): <ul style="list-style-type: none"> <li>• SRCCCLKREQ#[5:0]</li> </ul>	I/O		Clock Request: Serial Reference Clock request signals for PCIe* 100 MHz differential clocks

*continued...*

Signal Name	Type	SSC Capable	Description
XTAL_IN	I		Crystal Input: Input connection for 38.4 MHz crystal to PCH
XTAL_OUT	O		Crystal Output: Output connection for 38.4 MHz crystal to PCH
XCLK_BIASREF	I/O		Differential Clock Bias Reference: Used to set BIAS reference for differential clocks

*Notes:* 1. SSC = Spread Spectrum Clocking  
2. The SRCCCLKREQ# signals can be configured to map to any of the PCH PCI Express\* Root Ports while using any of the CLKOUT\_PCIE\_P/N differential pairs

### 6.1.3 Platform Clock Associated Signal Guidelines

The guidelines for the following platform clock signals are provided in the excel sheet portion of the PDG.

- SRCCCLKREQ#[6:0] - PCH-LP (UP3)
- SRCCCLKREQ#[5:0] - PCH-LP (UP4)
- 38.4 MHz Input Clock
  - XTAL\_IN
  - XTAL\_Out
- XCLK\_BIASREF

#### 38.4MHz Input Clock Routing Guidelines

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##### NOTES

- All platforms are required to provide a 38.4 MHz input to the PCH to enable the PCH to generate all of its internal reference clocks and all of the single-ended and differential platform clock outputs.
  - It is strongly recommended that customers designing a Platform pay special attention and follow all of the XTAL\_IN/XTAL\_OUT routing guidelines. The crystal, components, and their XTAL\_IN/XTAL\_OUT signals are very sensitive to board noise and care must be taken when routing and placing these components and signals on the motherboard to provide shielding from any noisy signals or power planes near the components and traces. The details covered in this section provide the guidelines needed to ensure the best environment for these components and signals. Any deviation from these guidelines could result in some platform clock instabilities.
- 

#### 38.4 MHz Crystal External Load Capacitor Requirements

The 38.4 MHz crystal is physically tuned to operate within the specified frequency range and ppm tolerance with a certain expected capacitive load present. The expected external capacitive load to be used ( $C_e$ ) consists of the crystal capacitive load plus the pin and trace capacitances. The external load capacitors are important to minimize frequency variations from the crystal by compensating for variable PCB factors related to pin and trace capacitance. Care must be exercised in the selection of the external load capacitors to present the expected capacitive load specified for the crystal in use on the platform.

The appropriate capacitor value for the platform may be determined using the following formula:

$$C_e = 2 * [C_L - (C_s + C_i)], \text{ where:}$$

- $C_e$  = External Load Capacitor Value =  $C_{e1} = C_{e2}$
- $C_L$  = Specified Crystal Capacitive Load = 10pF
  - Found in crystal component data sheet
- $C_s$  = Board Trace Capacitance = < 3pF
  - Includes crystal pad capacitance
- $C_i$  = PCH Pin Capacitance = < 2 to 3pF

Due to vendor variation in crystal characteristics, layout variations and PCB trace capacitance differences, the above calculation should be performed for each design to determine the precise value of  $C_e$  that is optimal for the particular platform.

#### 38.4 MHz Crystal Specification Requirements

**Table 64. 38.4 MHz Crystal Specifications**

Parameter	Values	Units	Max/Min Range
Frequency	38.4	MHz	
Frequency Tolerance	$\leq 100$	PPM	
Duty Cycle Variation	$+/- 5$	%	
Pk to Pk jitter	$\leq 150$	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	
Series Resistance	$\leq 30$	$\Omega$	
Aging	$\pm 3$	PPM	
Notes: 1. Customers should verify that the vendor's published specifications in the component data sheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance as specified in the respective data sheet. 2. Perform conformance testing and EMC (FCC and EN) testing in real systems 3. Independently measure the component's electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.			

## 6.2

### Real Time Clock (RTC) Design Guidelines

The PCH contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The PCH RTC module requires an external oscillating source 32.768KHz connected on the RTCX1 and RTCX2 balls. Figure below shows the external circuitry that comprises the oscillator of PCH RTC.

The PCH uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to PCH, the RTCX1 signal is amplified to drive internal logic.

**Table 65. Reference Specification**

Title	Location
Design Considerations for Platforms Without a Coin Cell Battery - White Paper	#549657
Intel® I/O Controller Hub (Intel® ICH)/Platform Controller Hub (PCH) Family Real Time Clock (RTC) Electrical, Mechanical, and Thermal Specification (EMTS) - AP-728	<a href="http://www.intel.com/content/www/us/en/chipsets/ich-family-real-time-clock-accuracy-considerations-note.html?wapkw=rtc">http://www.intel.com/content/www/us/en/chipsets/ich-family-real-time-clock-accuracy-considerations-note.html?wapkw=rtc</a>
Real Time Clock Reset Timing Technical Advisory	#610459

### 6.2.1 RTC Signal Description

Signals	Description
RTCX1	Crystal Input 1
RTCX2	Crystal Input 2
SUSCLK	RTC Clock
RTCRST#	RTC Reset
SRTCRST#	Secured RTC Reset

### 6.2.2 RTC Topology Guideline

#### VCCRTC External Circuit

On TGL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW\_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.3V.

#### General RTC Layout Considerations

Since the RTC circuit is very sensitive and requires highly accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Figure and table below provides some general length guidelines for the RTC crystal circuit.

For additional information about RTC Layout Considerations, refer to *Intel® I/O Controller Hub (Intel® ICH)/Platform Controller Hub (PCH) Family Real Time Clock (RTC) Electrical, Mechanical, and Thermal Specification (EMTS) - AP-728* for details layout consideration and fine tuning.

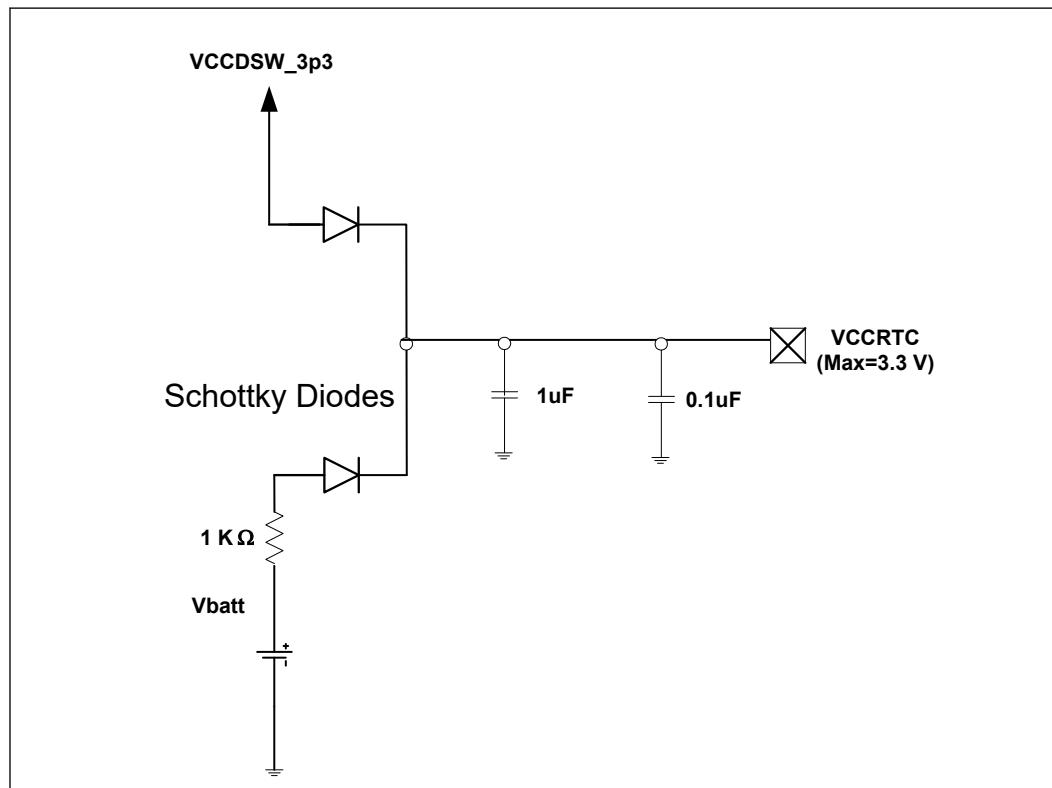
#### RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while PCH is not powered by the system.

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases.

The battery must be connected to PCH using an isolation Schottky diode circuit. The Schottky diode circuit allows PCH RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. The following figure is an example of a diode circuit that is used.

**Figure 62. Schottky Diode Circuit to Connect RTC External Battery**



A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

Using a rechargeable coin battery or a capacitor with a short projected discharged time can increase the risk of:

- an un-provisioned Intel® Active Management Technology (Intel® AMT)
- unusable anti-replay blobs
- Intel® Management Engine (Intel® ME) file system corruption

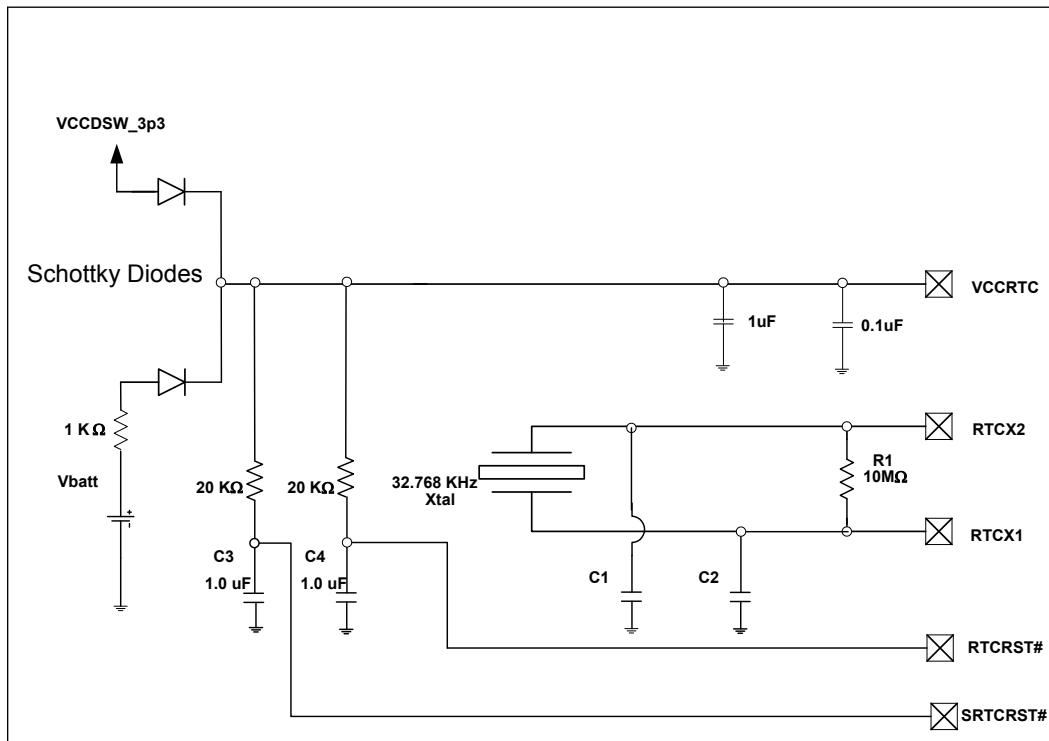
The first two cases are recoverable: Intel® Active Management Technology (Intel® AMT) can be re-provisioned, and applications using the anti-replay-blobs can be re-enrolled. The third case, the corruption of the Intel® Management Engine (Intel® ME) file system, is irretrievable, but has a very low probability of occurring even when a full discharge occurs.

### RTC Coin-cell Less Implementation

Modern implementation of the RTC can also be designed without a coin-cell battery. Details on this implementation is available in the *Design Considerations for Platforms Without a Coin Cell Battery - White Paper*.

#### 6.2.3 RTC External RTCRST# Circuit

**Figure 63.** RTCRST/SRTCRST External Circuit for PCH RTC



The RTCRST# signal is used to reset the RTC well.

---

**NOTE**

RTCRST# should be generated from VBAT with a RC delay of 18–25 ms.

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When RTCRST# is asserted, bit 2 (RTC\_PWR\_STS) in the GEN\_PMCN\_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

The RTCRST# signal may also be used to detect a low battery voltage. RTCRST# will be asserted during a power up from G3 state if the battery voltage is below 2V. This will set the RTC\_PWR\_STS bit as described above. If desired, BIOS may request that the user replace the battery.

This RTCRST# circuit is combined with the diode circuit (refer figure above) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. The above figure is an example of this circuitry that is used in conjunction with the external diode circuit.

## 6.2.4 RTC External SRTCRST# Circuit

The SRTCRST# signal is used to reset the RTC registers used for the Intel® Management Engine (Intel® ME) when the on board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18–25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing. Refer to [Figure 63](#) on page 126 for external circuit for PCH RTC.

### NOTES

- RC time delay for SRTCRST# should be the same as RC delay for RTCRST#.
- RTCRST# and SRTCRST# cannot be shorted together.

## 6.2.5 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, SRTCRST#, INTRUDER#, PCH\_PWROK, DSW\_PWROK) must be either pulled up to VccRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in [Figure 63](#) on page 126 meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PCH\_PWROK and DSW\_PWROK input signal should also be configured with an external weak pull-down.

## 6.2.6 RTC Component Selection Guidelines

- **RTC Clock Crystal Capacitors (C1 and C2)**

To maintain the RTC accuracy, the external capacitor values C1 and C2 should be chosen to provide the manufacturer's specified load capacitance ( $C_{load}$ ) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package.

$$C_{load} = \frac{[(C_1 + C_{in1} + C_{trace1}) \bullet (C_2 + C_{in2} + C_{trace2})]}{[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}}$$

For additional information about the External Capacitors, refer to *Intel® I/O Controller Hub (Intel® ICH)/Platform Controller Hub (PCH) Family Real Time Clock (RTC) Electrical, Mechanical, and Thermal Specification (EMTS) - AP-728* for details on fine tuning.

- **Capacitor Selection Considerations (C3 and C4)**

DC voltage characteristics vary among different types and sizes of capacitor. Capacitance variation with voltage, temperature and age should be taken into account when selecting components for the RTC external circuit to ensure the actual capacitance matches expectations, especially for C3 and C4 shunt capacitors. Over time, as systems have decreased in size, ceramic capacitors have also become smaller for equivalent nominal values of capacitance. Large amounts of nominal capacitance can now be obtained in very small form factors. For

instance, 0201 capacitors with values at or above 1uF are now common (e.g. X5R or X7R 0201, 1uF capacitors). Ceramic capacitors tend to exhibit a loss of capacitance with applied DC voltage. High capacitance, small form factor (0402, 0201, and lower) parts, tend to exhibit more significant capacitance loss due to DC bias than their physically larger counterparts, for the same applied voltage. This phenomenon can result in lower than expected time constants for circuits utilizing small form factor capacitors. The impact may also vary by manufacturer for "equivalent" parts. The data sheet for each capacitor considered should be checked to make sure that, under DC conditions, the effective capacitance works as intended in a given circuit application.

### 6.2.7 SUSCLK Routing Guidelines

The SUSCLK single load(device down), single load(add in card) and dual load topologies are supported in TGL UP3/UP4.

## 6.3 Imaging Clock

### Signal

There are up to six different Imaging Clock out signals from the PCH

**Table 66. Imaging Clock Signal Descriptions**

Name	Type	Description
GPPC_D4 / IMGCLKOUT0	0	Imaging Clock
GPPC_H20 / IMGCLKOUT1	0	Imaging Clock
GPPC_H21 / IMGCLKOUT2	0	Imaging Clock
GPPC_H22 / IMGCLKOUT3	0	Imaging Clock
GPPC_H23 / IMGCLKOUT4	0	Imaging Clock
GPP_D15 / ISH_UART0_RTS# / GSPI2_CS1# / IMGCLKOUT5	0	Imaging Clock

## 6.4 Flexible I/O

Flexible Input/Output (I/O) is a technology that allows some of the PCH High Speed I/O (HSIO) lanes to be configured for connection to a Gigabit Ethernet (GbE) Controller, a PCIe\* Controller, an Extensible Host Controller Interface (xHCI) USB 3.2 Controller, or a Advanced Host Controller Interface (AHCI) SATA Controller. Flexible I/O enables customers to optimize the allocation of the PCH HSIO interfaces to better meet the I/O needs of their system.

---

### NOTE

The PCH Flexible I/O Lane support will vary depending on the PCH SKU. Refer to the associated PCH External Design Specification (EDS) Volume 1 for specific PCH SKU Flexible I/O implementation details.

---

## 6.5 PCH PCI Express\* Interface Design Guidelines

### 6.5.1 PCH PCI Express\* Interface Configuration Details

**Figure 64.** Supported PCH PCI Express\* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
<b>Flex I/O Lanes</b>		<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>	<b>8</b>	<b>9</b>	<b>10</b>	<b>11</b>
<b>PCIe* Lanes</b>		<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>	<b>8</b>	<b>9</b>	<b>10</b>	<b>11</b>	<b>12</b>
Logical Link Lanes	<b>1x4</b>	0	1	2	3	0	1	2	3	0	1	2	3
	<b>1x4 LR</b>	3	2	1	0	3	2	1	0	3	2	1	0
	<b>2x2</b>	0	1	0	1	0	1	0	1	0	1	0	1
	<b>2x2 LR</b>	1	0	1	0	1	0	1	0	1	0	1	0
	<b>1x2+2x1</b>	0	1	0	0	0	1	0	0	0	1	0	0
	<b>2x1+1x2</b>	0	0	1	0	0	0	1	0	0	0	1	0
	<b>4x1</b>	0	0	0	0	0	0	0	0	0	0	0	0
Assigned Root Ports	<b>1x4</b>	RP1				RP5				RP9			
	<b>1x4 LR</b>	RP1				RP5				RP9			
	<b>2x2</b>	RP1		RP3		RP5		RP7		RP9		RP11	
	<b>2x2 LR</b>	RP3		RP1		RP7		RP5		RP11		RP9	
	<b>1x2+2x1</b>	RP1		RP3   RP4		RP5		RP7   RP8		RP9		RP11   RP12	
	<b>2x1+1x2</b>	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	<b>4x1</b>	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12

---

**NOTES**

1. The PCH PCIe\* Link Configuration support will vary depending on the PCH SKU. Refer to the associated PCH External Design Specification (EDS) Volume 1 for specific PCH SKU PCIe\* implementation details.
  2. RP# refers to a specific PCH PCI Express\* Root Port #; for example RP3 = PCH PCI Express\* Root Port 3.
  3. A PCIe\* Lane is composed of a single pair of Transmit (TX) and Receive (RX) differential pairs, for a total of four data wires per PCIe\* Lane (such as, PCIE[3]\_TXP/ PCIE[3]\_TXN and PCIE[3]\_RXP/ PCIE[3]\_RXN make up PCIe Lane 3). A connection between two PCIe\* devices is known as a PCIe\* Link, and is built up from a collection of one or more PCIe\* Lanes which make up the width of the link (such as bundling 2 PCIe\* Lanes together would make a x2 PCIe\* Link). A PCIe\* Link is addressed by the lowest number PCIe\* Lane it connects to and is known as the PCIe\* Root Port (such as a x2 PCIe\* Link connected to PCIe\* Lanes 3 and 4 would be called x2 PCIe\* Root Port 3).
  4. The PCIe\* Lanes can be configured independently from one another but the max number of configured Root Ports (Devices) must not be exceeded
    - PCH-LP (UP3) supports a maximum of 6 PCIe\* Root Ports (or devices) can be enabled
    - PCH-LP (UP4) supports a maximum of 5 PCIe\* Root Ports (or devices) can be enabled
    - When a GbE Port is enabled, the maximum number of PCIe\* Ports (or devices) that can be enabled reduces based off the following:
      - PCH-LP (UP3) Max PCIe\* Ports (or devices) = 6 - GbE (0 or 1)
      - PCH-LP (UP4) Max PCIe\* Ports (or devices) = 5 - GbE (0 or 1)
  5. Unidentified lanes within a PCIe\* Link Configuration are disabled but their physical lanes are used for the identified Root Port
  6. The PCH PCIe\* Root Ports can be configured to map to any of the SRCCLKREQ# PCIe\* clock request signals and the CLKOUT\_PCIE\_P/N PCIe\* differential clock signal pairs covered
  7. Lane Reversal Supported Motherboard PCIe\* Configurations = 1x4, 2x1+1x2, and 2x2
    - The 2x1+1x2 configuration is enabled by setting the PCIe\* Controller soft straps to 1x2+2x1 with Lane Reversal Enabled
    - 1x4 = 1x4 with Lane Reversal Disabled, 1x4 LR = 1x4 with Lane Reversal Enabled
    - 2x2 = 2x2 with Lane Reversal Disabled, 2x2 LR = 2x2 with Lane Reversal Enabled
  8. Un-used USB 3.2/PCIe and SATA/PCIe Combo Port Lanes must be statically assigned to "Disabled" through their Combo Port Soft Straps discussed in the SPI Programming Guide using the Intel Flash Image Tool (FIT).
    - Refer to the associated PCH External Design Specification (EDS) Volume 1 for specific PCH Combo Port Lane implementation details
-

## 6.5.2 PCH PCI Express\* Signal Descriptions

**Table 67.** PCH PCI Express\* Signal Groups

Group	Signal Name	Description
Data	PCH-LP (UP3) <ul style="list-style-type: none"> <li>• PCIE[12:1]_TXN and PCIE[12:1]_TXP</li> </ul> PCH-LP (UP4) <ul style="list-style-type: none"> <li>• PCIE[12:7, 4:1]_TXN and PCIE[12:7, 4:1]_TXP</li> </ul>	PCI Express* Transmit Differential-Pair
	PCH-LP (UP3) <ul style="list-style-type: none"> <li>• PCIE[12:1]_RXN and PCIE[12:1]_RXP</li> </ul> PCH-LP (UP4) <ul style="list-style-type: none"> <li>• PCIE[12:7, 4:1]_RXN and PCIE[12:7, 4:1]_RXP</li> </ul>	PCI Express* Receive Differential-Pair
RCOMP	PCIE_RCOMPN and PCIE_RCOMPP	Impedance Compensation Inputs

## 6.5.3 Modern Standby - PCIe D3cold Enabling

Each PCIe end point device link state should be at L2 or deeper to enable platform S0 idle states deeper than S0i2.0 or S0i3.0. Implementing PCIe end point device D3cold is required to enable its link state to enter L2 or deeper. PCIe Device Power Management D3cold state is where all core power is removed from end point device, and any auxiliary power is only supplied if the device is enabled to generate a wake event. Core power removal is controlled by the platform via external power controls, typically power FETs, and may be required to limit power consumption of PCIe NVMe Storage Devices; otherwise higher than expected device power could be observed with D3cold.

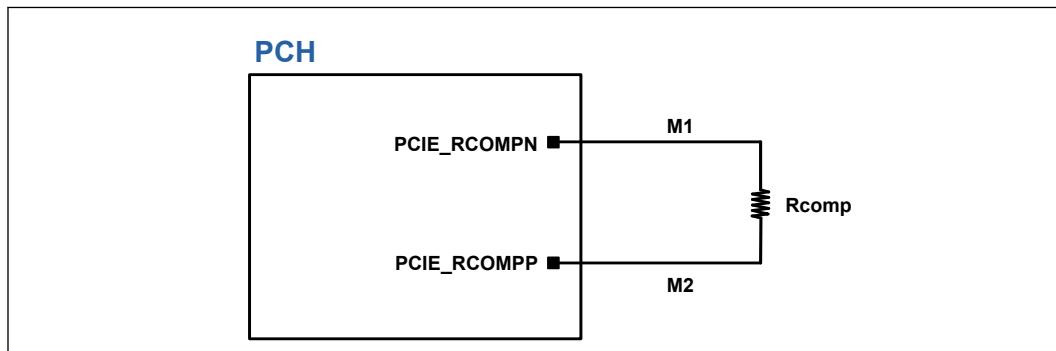
For complete D3cold hardware, software, and motherboard (PERST#, Wake#, device VDD\_Core, and device VDD\_Aux) recommendations reference the following material and consult your PCIe device vendor(s) for their D3cold required implementation and power consumption:

1. Tiger Lake Platform Runtime D3 (RTD3) Hardware and Software Recommendations Design Guide (Document 576056)
2. SLPS0 Design and Debug Checklist (#570300)

## 6.5.4 PCH PCI Express\* Routing Guidelines

### PCH PCI Express\* Impedance Compensation Guidelines

**Figure 65.** PCH PCIE\_RCOMPP and PCIE\_RCOMPN Connections



**Table 68. PCH PCI Express\* Compensation Routing Guidelines**

Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5 GT/s Routing	8 GT/s Routing
Reference Plane	M1, M2	MS/SL/DSL		GND	GND	GND
Compensation resistor	M1, M2	MS	Ohms	100 +/-1%	100 +/-1%	100 +/-1%
Motherboard Max Via Count	M1, M2	NA	vias	2	2	2
Motherboard Length Matching	M1, M2	MS/SL/DSL	mm	M1- M2 = ± 0.127mm		
Notes: 1. Recommended placing a VSS shield of at least 0.1 mm wide between the RCOMP signals and any adjacent I/O signal 2. Avoid routing close to any clocks 3. Micro-Vias within the breakout area are not counted against maximum via total 4. Must maintain low DC resistance routing (<0.1 ohm)						

### PCH PCI Express\* Lane Polarity Inversion

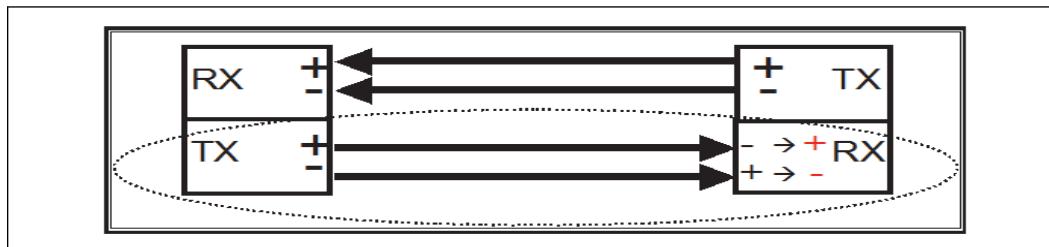
The PCI Express\* Base Specification requires polarity inversion to be supported independently by all receivers across the Link where each differential pair within each Lane of the PCIe\* Link handles its own polarity inversion. Polarity inversion does not imply direction inversion or direction reversal; that is, the Tx differential pair from one device must still connect to the Rx differential pair on the receiving device, per the PCIe\* Base Specification.

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#### NOTE

Polarity Inversion is not the same as "PCI Express\* Controller Lane Reversal"

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**Figure 66. PCH Polarity Inversion on a TX to RX Interconnect**


### PCH PCI Express\* Controller Lane Reversal

For each PCH PCIe\* Controller we support end-to-end lane reversal across the four lanes mapped to a controller for the following two motherboard PCIe\* configurations

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#### NOTES

- Lane Reversal Supported Motherboard PCIe\* Configurations = 1x4, 2x1+1x2, and 2x2
    - The 2x1+1x2 configuration is enabled by setting the PCIe\* Controller soft straps to 1x2+2x1 with Lane Reversal Enabled.
  - PCH PCI Express\* Controller Lane Reversal is not the same as PCI Express\* Lane Polarity Inversion.
-

**Table 69.** PCH PCIe\* Configuration Lane Reversal Mapping

PCIe* Configuration	PCI Express* Lanes				PCI Express* Down Device or Connector Lanes
	PCIe* Controller #1	PCIe* Controller #2 PCH-LP (UP3)	PCIe* Controller #2 PCH-LP (UP4)	PCIe* Controller #3	
1x4	1	5	Not Available	9	3
	2	6	Not Available	10	2
	3	7	Not Available	11	1
	4	8	Not Available	12	0
2x1+1x2	1	5	Not Available	9	0
	2	6	Not Available	10	0
	3	7	Not Available	11	1
	4	8	Not Available	12	0
2x2	1	5	Not Available	9	1
	2	6	Not Available	10	0
	3	7	Not Available	11	1
	4	8	Not Available	12	0

## 6.6 SATA Interface Guidelines

SATA ports are capable of independent DMA operation. The SATA controllers are completely software transparent with an AHCI interface and only supports AHCI mode using memory space (IDE mode is not supported).

**Table 70.** SATA Reference Documents

Title	Document Number/Location
SATA-IO Certified Test Laboratories	<a href="http://www.sata-io.org">www.sata-io.org</a>
High Speed Internal Connector and Cable – Specification	549136
An Electrical Study on the Implementation of 85Ω Nominal Differential Impedance Transmission Lines in High-Speed Serial ATA Interface - Technical White Paper	549023

**Table 71.** SATA Compliance Documents

Title	Document Number/Location
Serial ATA Specification, Revision 3.2	<a href="http://www.sata-io.org">www.sata-io.org</a>

## 6.6.1 SATA Signal Description

**Table 72. SATA Signal Groups**

Group	Signal Name	Description
SATA Receive	SATA0_RXP/RXN, SATA1_RXP/RXN.	Differential Receive Pair
SATA Transmit	SATA0_TXP/TXN, SATA1_TXP/TXN.	Differential Transmit Pair
Power Control	DEVSLP[1:0].	Host Controlled Power State
GPIO	SATAGP[1:0]	General Purpose
LED	SATA_LED#	LED

### SATA Signal Considerations

#### SATA General Purpose (SATAGP[1:0]) Signals

- The PCH provides three SATA general purpose input signals and can be implemented as interlock switch inputs corresponding to a given SATA port.
- When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
- If mechanical presence switches will not be used on the platform, the signals can be used as GPIOs.

#### DEVSLP[1:0] Implementation

- DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs. When **high**, DEVSLP requests the SATA device to enter into the DEVSLP power state.
- When **low**, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.
- Align DEVSLP pin assignment 1 host pin to 1 device pin as follows:
  - DEVSLP0 to DEVSLP Port0
  - DEVSLP1 to DEVSLP Port1

---

#### NOTE

1 DEVSLP pin is required to support EACH DEVSLP enabled RAID storage device. (Example: 2 DEVSLP pins are required to support 2 DEVSLP RAID storage devices).

- DEVSLP is an open-drain pin on the PCH side and is not required external pull-up or pull-down. The PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
  - DEVSLP is supported in direct connect, mSATA/mPCIe, uSSD, M.2.
-

### SATA\_LED# Implementation

The processor provides SATA\_LED# to simplify the indication of SATA devices activity. SATA\_LED# is not intended to source high current design implementation. Use current isolation circuitry for implementation beyond driving an LED activity indicator.

- The SATA\_LED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3\_3.
- When **low**, SATA\_LED# indicates activity on **any** SATA port.

## 6.6.2 SATA General Guidelines

### SATA Link Power Management

Intel recommends the following design options to further reduce SATA link power consumption while supporting hot plug on SATA ports. In general, Intel recommends connecting the Mechanical Present detect pin (SATAGP[1:0]) to topologies supporting SATA slimline connectors, SATA repeaters, and docking connectors in order to detect hot plug events. The usage of the SATAGP[1:0] pins must correspond to the port that has the mechanical presence switch implemented (such as, the processor SATA port 0 will use SATAGP0 as the mechanical presence pin).

### SATA Disabling and Termination Guidelines

If a SATA port(s) is not implemented, then SATA[x]\_RXP/RXN and SATA[x]\_TXP/TXN signals may be left unconnected; where 'x' is the port number left as no connect.

SATA compensation circuit is shared with PCIE\_RCOMPP/N differential pair.

### Flexible I/O PCIe/SATA Port Selection

The HSIO lanes that have PCIe/SATA port muxing can be statically configured to SATA or PCIe by soft straps.

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#### NOTE

Refer to the SPI Programming Guide documentation for details on how to configure the HSIO ports via soft straps.

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In addition to static configuration via soft straps, the HSIO lanes that have PCIe/SATA port muxing can be configured dynamically to SATA or PCIe via SATAXPCIE signaling to support implementation like SATA Express, M.2 and mSATA, where the port configuration is selected by the type of the add-in card that is used.

Refer to the SPI Programming Guide documentation for details on how to configure the SATAXPCIE for SATA/PCIe port selection.

### AC Capacitor General Guidelines SATA / PCI Express\* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe\* multiplexed ports. SATA does not support signal polarity reversal and does not support lane reversal.

**Table 73. SATA / PCI Express\* Gen 2x1 (10 Gb/s) and Gen 3 Capacitor Values**

Condition	PCI Express* Gen 2x1 (10 Gb/s) Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2x1 (10 Gb/s)/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF1	None2	None3

**Notes:**

1. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
2. For PCIe\* Gen 2x1 (10 Gb/s)/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
3. For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe\* lane that needs to support either **PCIe\* Gen 2x1 (10 Gb/s) devices or PCIe\* Gen3 devices**, follow the PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

### 6.6.3 SATA Topologies and Guidelines

The following SATA topologies are supported on platform. Refer to Tiger Lake UP3/UP4 design guidelines.xlsx document for PCB routing guidelines for each topology. This document is released as part of PDG package.

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#### NOTE

Tiger Lake UP4 platform does not support SATA interface.

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- mSATA/Direct connect and M.2 topology
  - The mSATA/direct connect and M.2 topology supports the routing of a SATA port directly to a connector where the SATA device will be connected directly without any cable.
- Internal SATA (cable connect) topology
- SATA Direct Connect with Internal Cable Topology
  - The direct connect with internal cable topology supports the routing of a SATA Gen 1x1 (5 Gb/s), Gen 2x1 (10 Gb/s), and Gen 3 ports directly to a connector using an internal connector. There are two topology implementations,
    - Without daughter card and with internal cable
    - With daughter card and with internal cable

### 6.6.4 Compliance Requirements - SATA Interface Guidelines

Ensure that the SATA system design is validated and tested for compliance to the SATA specifications. This can be done by executing the Signal Quality Test or by having the system tested by a SATA-IO Certified Test Laboratory. Refer to [www.sata-io.org](http://www.sata-io.org) for a list of approved facilities.

## 6.7

## Intel Storage M.2 Guidelines

PCIe\* M.2 specification contains various key configurations for different functions. For storage the applicable key configurations are Socket 2 Key B, and Socket 3 Key M. Key B is for SSDs that use 2 PCIe\* lanes or SATA SSDs. Key M is for SSDs or NVMe drives that use up to 4 PCIe\* lanes.

M.2 storage devices come in a variety of sizes. Determine which devices your design needs to support in order to determine the location of the standoffs and mounting screw locations.

For detailed routing guidelines (trace length, spacing, etc.), refer to the PCIe\* design guidelines for M.2 topologies.

### 6.7.1

### Power Delivery

Socket 2 has 5 power pins and supports up to 2.5 A. Socket 3 has 9 power pins and supports up to 2.5 A. The 4 extra power pins in Socket 3 are to reduce IR drop.

The power supply for the M.2 module is 3.3 V ±5%.

### 6.7.2

### Power Loss Notification (PLN) Feature for M.2 NVMe SSD

#### Problem

A sudden loss of power caused by long power button press may cause minimal data loss and subsequent boot delays.

#### Solution

To prevent this problem, a new optional pin in M.2 pinout, called PLN, was defined as a part of an ECR, refer to reference document section 6.x.x.x, to provide the NVMe SSD an early warning that power will be lost. This allows the SSD to prepare as if a graceful shutdown and avoid unexpected power loss. If PLN# is de-asserted before the override time, the device shall return to normal operations. Currently, the PLN# feature will be used to cover long power button press power only.

To support sudden power loss from long power button press, the following system requirements must be met:

1. NVMe SSD with PLN support
2. A Discrete IC or EC to recognize that the power button was held down for the allotted time. It also connects to the PLN signal on the M.2 connector.
3. BIOS support to determine if the feature is available and to override if necessary.

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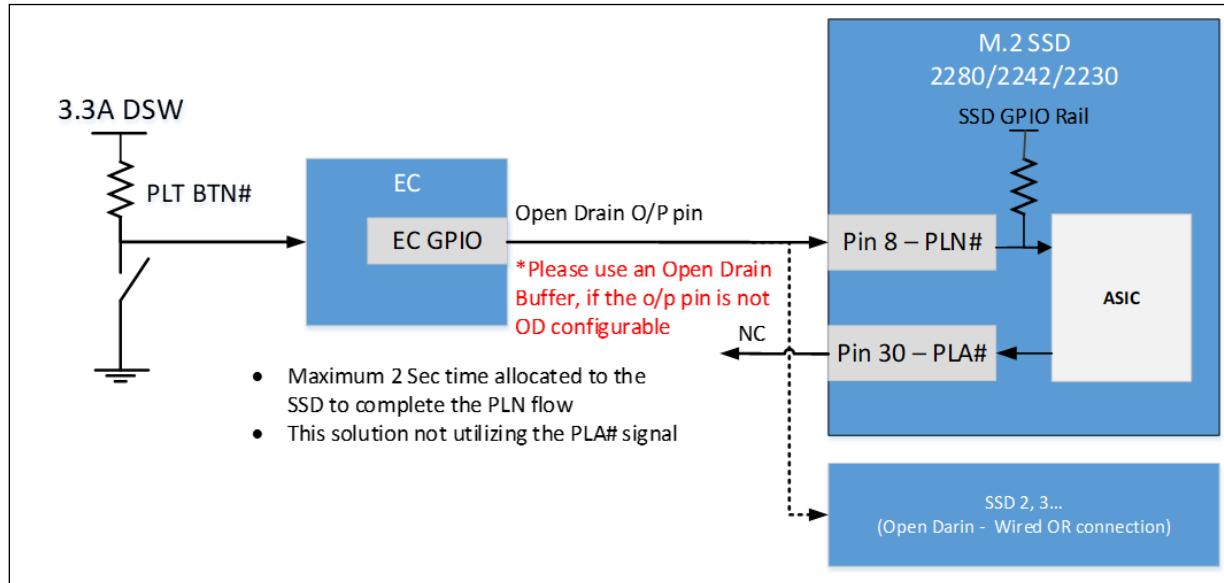
#### NOTE

All other power loss scenarios such as AC power loss or battery removal is not supported by the PLN feature. The PLA pin is currently not used as part of this PLN feature implementation.

### 6.7.2.1 Platform Design Implementation

If system design is using EC Controller, the power button is routed to EC Controller and EC Controller GPIO is routed to Pin 8 of M.2 connector. Refer figure below for example on block diagram of connection.

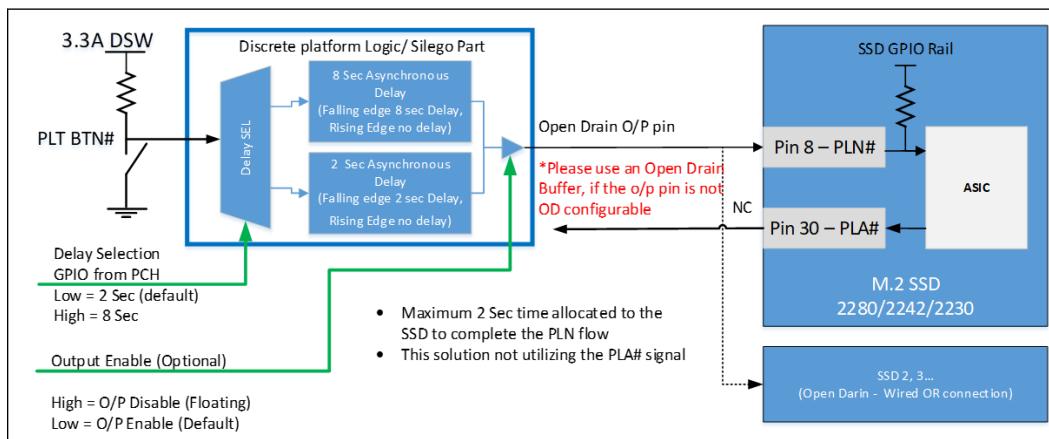
**Figure 67. PLN# with Embedded Controller**



If the system design is using a discrete solution, the power button should route to a logic controller with the output going into Pin 8 of the M.2. An additional GPIO from PCH to the discrete controller is needed to output a low or high depending on button press length.

The 2 and 8 seconds delays are asynchronous delays and follow the falling edge of the PWRBTN# signal. There is no delay at the rising edge of the PWRBTN# signal. This ensures NVMe SSD PLN# signal de-assertion is coincident with de-assertion of PWRBTN#. Refer Figure below for example on block diagram of connection.

**Figure 68. PLN# without Embedded Controller**



The Power Loss Notification feature requires an additional pin on the M.2 connector. This is pin #8 on the Key M M.2 module and connector.

### 6.7.2.2 BIOS and Discrete Solution or EC Support

BIOS configuration of a PCH GPIO is required, if a discrete solution is used. If EC is used to control the PLN# pin, it must have a programmed GPIO to handle the flow.

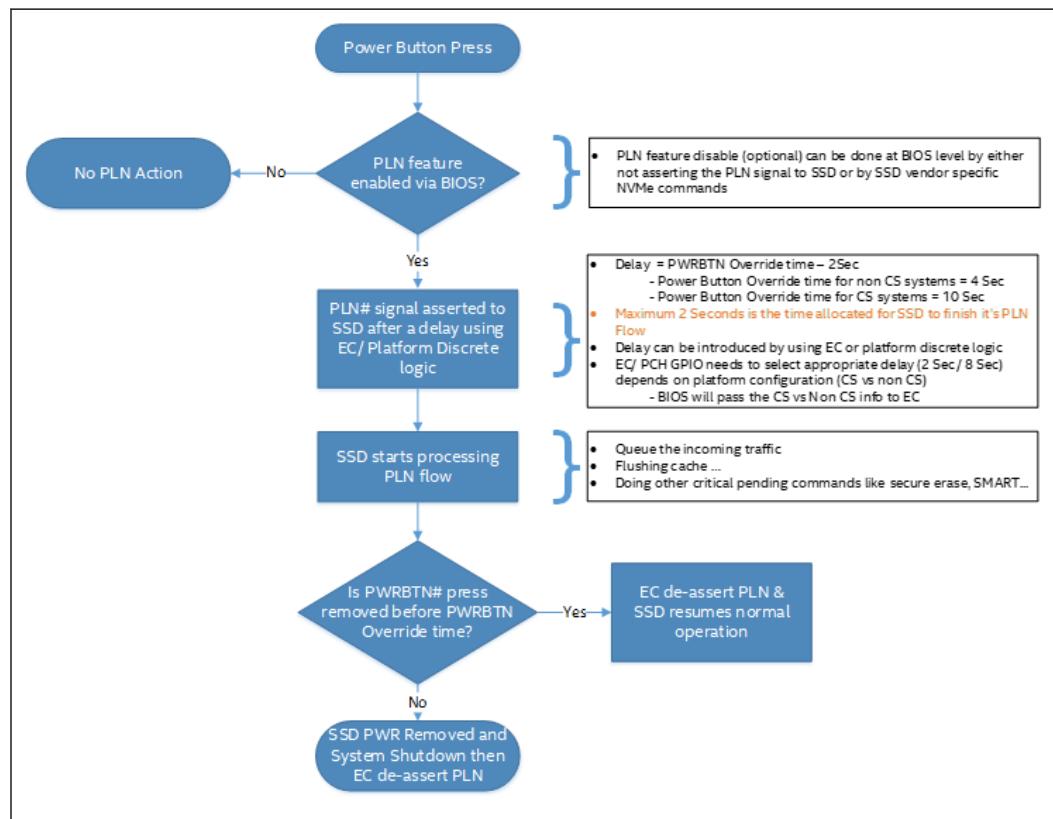
- Drive is allocated Maximum 2 seconds to finish the PLN flow.
- CS is 10 seconds power button press for system shutdown
- Non-CS is 4 seconds power button press for system shutdown

#### NOTE

These Connected Standby (CS) times are programmable

Figure below is an example flow diagram of the PLN process. When a user presses and holds the power button, PLN# will assert and the NVMe SSD will start preparing for shutdown. If the button is released before the programmed override time, the drive will go back to normal operation.

**Figure 69. Flow Diagram for PLN**



### 6.7.2.3 PLN Reference

<https://members.pcisig.com/wg/PCI-SIG/document/previewpdf/11942>

**NOTE**

This ECR is for PLN from PCI SIG and will be updated after it is incorporated in the M.2 Module section.

### 6.7.2.4 RTD3 Implementation

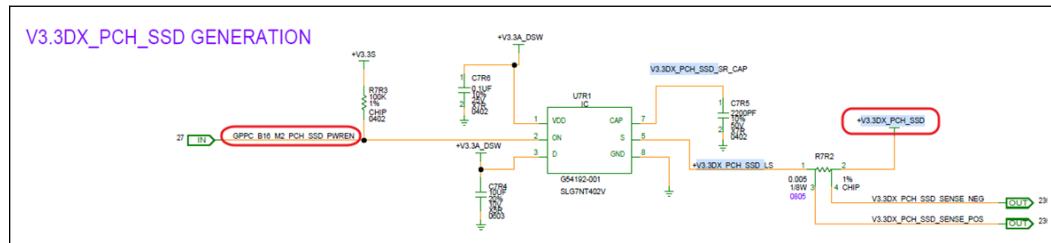
Runtime D3 is used to describe a device state whereby power is removed or drastically reduced while the system is in the S0 or operational state. Only device managed power and/or clock gating is engaged in D3(hot). D3(hot) is a low-power, non-operational state. D3(cold) is where all core power is removed, and any auxiliary power is only supplied if the device is enabled to generate a wake event. Power removal is controlled by the platform via external power controls, typically power FETs. The policy controlling device runtime power management is typically owned by the running operating system.

**NOTE**

Intel only supports Bitlocker for D3 cold. Drive password, example: Pyrite, OPAL and so on is not supported. D3hot does not have the same limitation and thus drive password, example: Pyrite, OPAL and so on or Bitlocker may be implemented.

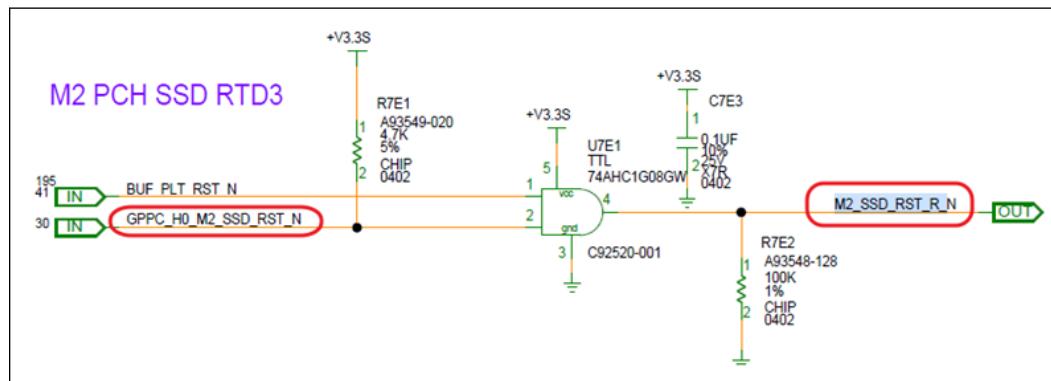
The external power control or power gate for M.2 storage RTD3 support is shown in below.

**Figure 70. RTD3 Power Gate Implementation**



In addition to the power gate, the reset signal for the M.2 slot needs to have PCH GPIO control as shown in below.

**Figure 71. RTD3 Reset Implementation**



### 6.7.2.5 Motherboard Flexibility Options

The processor PCIe\* interfaces have only x4 configuration to support PCIe\* (1x4) SSDs. But, Intel hybrid Optane drives need a 2x2 configuration which is not compatible with the processor PCIe\* port.

If your design can only accommodate a single storage M.2 socket, and you want to have flexibility to support hybrid drives from the PCH as well as SSDs from the processor, there are two design options shown below.

#### Zero Ohm Resistor Stuffing Option

Refer *Intel Teton Glacier Storage Support with Multiplexed CPU PEG and PCH PCIe3\*on Single M.2 Technical Whitepaper (# 626037)*.

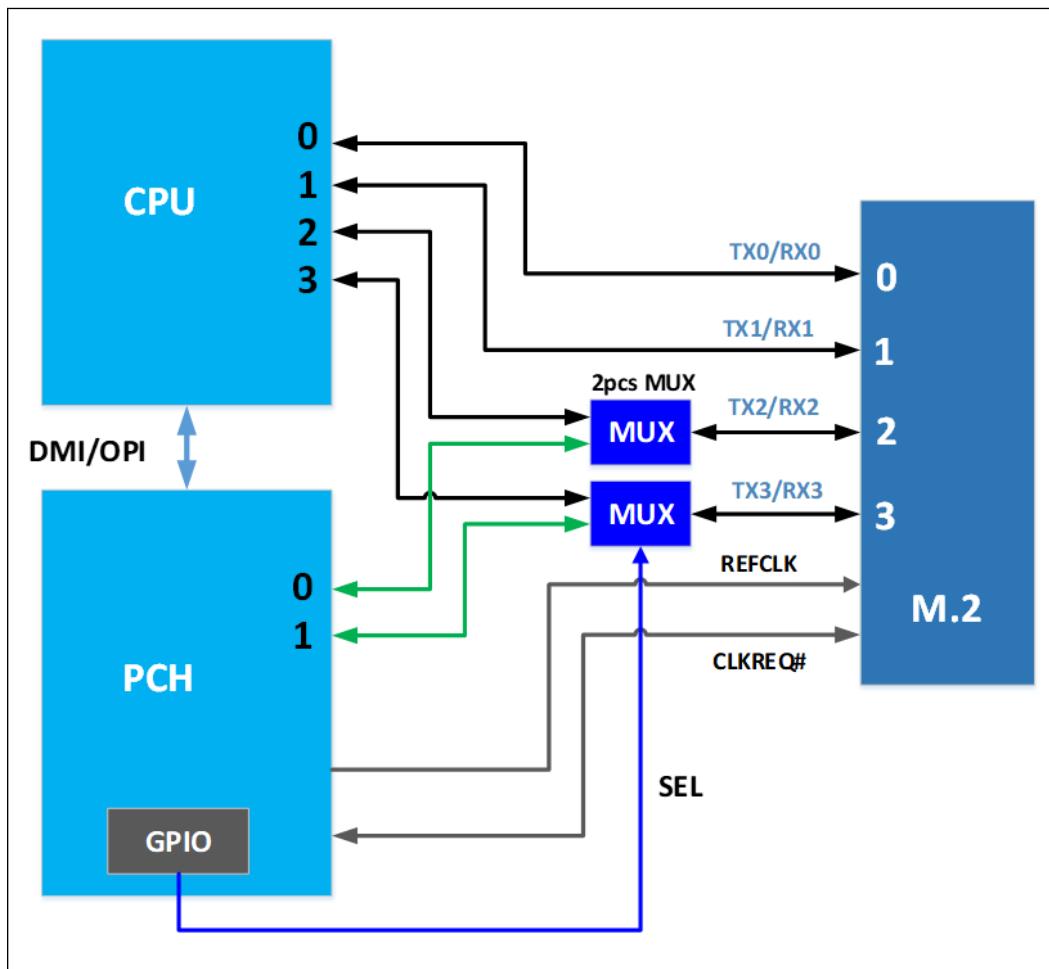
Even though the above guidelines are for Teton Glacier, they can also be applied to Pyramid Glacier.

#### Passive Multiplexer Option

A passive mux can also be used to support a single storage M.2 socket. In this example, in order to save some cost and motherboard space, two PCIe\* lanes from the processor are used and two PCIe\* lanes from the PCH are used. In this way, only two mux components are needed. This option is shown in Figure below.

A GPIO from the PCH can be used to switch between processor attached storage and PCH attached storage.

The routing guidelines for this option can be found in the PCIE Gen 3 M.2 with Passive Mux and CPU PCIe Gen4 - Hybrid with Passive MUX sections in this document.

**Figure 72. Passive Mux Options**


## 6.8

## Universal Serial Bus USB 3.2 Design Guidelines

Platform Controller Hub (PCH) has an xHCI controller and device controller implemented in it.

**Table 74.**
**Tiger Lake Processor USB Overcurrent Pins**

Processor	Overcurrent Pins
TGL UP3/UP4	USB2_OC[3:0]
TGL UP3/UP4	USB_OC[3:0]#

**Table 75.**
**USB 3.2 Reference Documents**

Title	Document Number / Location
USB 3.2 Repeater Integration Technical White Paper Rev 0.9	571574

**Table 76. USB 3.2 Compliance Documents**

Title	Document Number / Location
USB 3.2 Specification	<a href="http://www.usb.org">www.usb.org</a>
USB 3.2 Front Panel Cable and Connector Implementation	<a href="http://www.usb.org/developers/docs/whitepapers/USB3p1_Front_Panel_CabCon_Implment_Doc_Rev1p0.pdf">http://www.usb.org/developers/docs/whitepapers/USB3p1_Front_Panel_CabCon_Implment_Doc_Rev1p0.pdf</a>

## 6.8.1 USB 3.2 Signal Descriptions

### Signal Groups

The following table provides a list of the USB 3 interface signals and signal type.

**Table 77. USB 3.2 Gen 2x1 (10 Gb/s) Interface Signals**

Group	Signal Name
USB 3 Differential Transmit Data Pairs	USB31_TXP USB31_TXN
USB 3 Differential Receive Data Pairs:	USB31_RXP USB31_RXN
Overcurrent	USB2_OC#

## 6.8.2 Overcurrent Protection

The overcurrent signals require a pull-up to the 3.3V Suspend Rail with 8.2–10 KΩ resistor. Additional overcurrent guidance can be found in this section.

---

### NOTE

It's not recommended to route the USB 3.2 signals to the USB connector for USB ports that is USB 2.0 capable only.

---

## 6.8.3 USB 3.2 Gen 1x1 (5 Gb/s) and Gen 2x1 (10 Gb/s) Topology Guidelines

The guidelines provided in this chapter apply to both Type-3 and Type-4 boards.

### USB 3.2 External Topology

This Topology is defined to be USB 3.2 signals routed directly to a standard and micro-sized Type-A and Type-B connector. Non-interleaved breakout (B0) is required to mitigate concerns on near-end crosstalk. The main route supports interleaved routing and non-interleaved routing for maximum flexibility. However, breakout must be routed using a non-interleaved scheme. Microstrip main route is also recommended albeit with shorter length than Stripline or Dual-Stripline. Routing recommendation is stated in the following table. For additional information refer PCB Stack-Up and Design Considerations.

These guidelines were developed assuming that the USB 3.2 Device has capacitors on its Tx SS lines. A single  $0\ \Omega$  resistor per signal trace should be available to be used to bypass the CMC content if it is proven that there is no EMI risk on USB 3.2 Tx/Rx signals. However, the  $0\ \Omega$  resistor must be placed near the connector at the same recommended location as the CMC.

### USB 3.2 Internal Cable Topology

This topology supports a low profile internal connector, internal cable solution. Non-interleaved breakout is required to mitigate concerns on near-end crosstalk. However the main route supports interleaved routing and non-interleaved routing for maximum flexibility.

For signal integrity considerations it is recommended that the USB 3.2 signals are routed to the A-connector via bottom-entry.

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#### NOTE

It is recommended that the internal connectors and cables adhere to the *High Speed Internal Connector and Cable Specification*.

---

A single  $0\ \Omega$  resistor per signal trace should be available to be used to bypass the CMC content if it is proven that there is no EMI risk on USB 3.2 Tx/Rx signals. However, this component must be placed near the connector at the same recommended location as the CMC.

**Table 78. USB 3.2 Gen 1x1 (5 Gb/s) Internal Cable Differential Insertion Loss Requirements**

Motherboard Total Trace Length [SL/DSL;MS] (mm)	Add-in-Card Trace Length (mm)	Internal Cable Assembly Insertion Loss Recommendation up to 2.5GHz	Internal Cable Assembly Insertion Loss Recommendation up to 5GHz	Internal Cable Assembly Insertion Loss Recommendation up to 7.5GHz
127;101.6	50.8	2.0dB	3.5dB	4.8dB
114.3;88.9	50.8	2.5dB	4dB	6dB
101.6;76.2	50.8	3.0dB	5dB	7dB
76.2;50.8	50.8	3.5dB	6dB	8.5dB
50.8;25.4	50.8	4.0dB	7dB	9.5dB

### USB 3.2 Re-driver Guidelines

This section provides the necessary guidelines for customers who intend to use re-driver in one of the aforementioned USB 3.2 topologies. Terms such as "re-timer", "repeater", and "re-driver" can be used to describe similar devices: active components used to amplify a signal passing through them. The definitions below are not exhaustive and are only applied in this document in the context of serial links.

**Re-driver:** An active component, which may have receiver equalization, transmitter de-emphasis, analog signal amplification, etc., to better "shape" the signals passing through it. Re-drivers do not perform retiming (i.e., the device does not implement any interface protocol and no re-sampling is performed). Because it changes the analog behavior of the incoming signals, the propagation of jitter, noise and other analog effects from one connected channel to the other must be considered. Note that a re-driver's performance is implementation specific in terms of loss compensation.

**Re-timer:** An active component compliant to the updated Appendix E of the USB 3.2 specification that performs re-sampling of the incoming signal and re-transmitting the recovered signal per specification. A re-timer is protocol aware and compliant to link power management. Note that the delay issue with a re-timer in Gen 1x1 (5 Gb/s) operation is solved if the implementation follows the updated Appendix E of USB 3.2 Specification document.

For additional details and recommendations regarding the implementation of re-driver in USB 3.2 Gen 2x1 (10 Gb/s) channel, refer to the following documents.

Title	Document Number
Intel Channel Checker (ICC) for Client Re-driver CQC Analysis	556174

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#### NOTE

Important Guidelines on Repeater/Active MUX topologies

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1. Max pre-channel length depends on what the specific repeater selected can compensate for at both 5G and 10G speeds when used in conjunction with Intel PCH. Work with Repeater vendor for specific routing recommendations. The aforementioned DG is preliminary and superseded by vendor recommendations.
2. In addition, it is recommended to refer to the white paper pertaining to the repeater integration (USB 3.2 Repeater Integration Technical White Paper # 571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
3. It is strongly recommended that OEMs use active mux/retimer/redriver parts from 3rd party vendors which meet below requirement to avoid EOS on Rx lines for USB3.

#### 6.8.4 USB 3.2 Specific Topology Guidelines

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#### NOTE

It is strongly recommended to include the use of ESD protection devices on each USB data signals.

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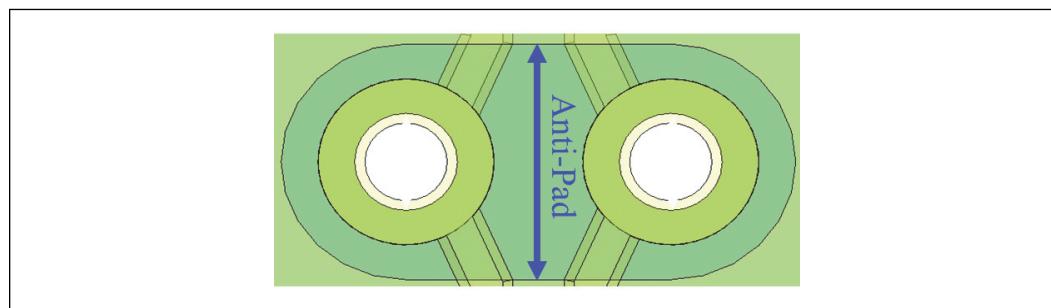
**Table 79. Trade off of Internal Cable Loss on Margin**

Main Board Total Length (mm)	Internal Cable Assembly Insertion Loss on Motherboard	Internal Cable Assembly Insertion Loss on Docking
50.8	4.0dB;4.5dB	4.5dB;4.0dB
38.1	4.5dB;5.0dB	5.0dB;4.5dB
25.4	5.0dB;5.5dB	5.5dB;5.0dB

#### 6.8.5 USB 3.2 General Guidelines

- **Length Matching between P and N within a diff. pair for Gen 1x1 (5 Gb/s) and Gen 2x1 (10 Gb/s):** Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm

- **Length Matching between P and N within a diff. pair for Gen 1x1 (5 Gb/s) and Gen 2x1 (10 Gb/s):** Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm
- **MODPHY\_RCOMP P/N sideband/Comp signals:** 100 Ohm +/-1% differential routing between RCOMP\_P and RCOMP\_N. length matching and closely coupled routing as per standard differential pair. DC-resistance onf <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88um at breakout and 200um at main route (currently to low-speed I/O) required
- **Stub Requirement:** Channel and Via stub requirement must meet <381um for both Tx and Rx signal pairs
- **Reference plane:** continuous GND is recommended. if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- Breakout scheme: TX and RX breakout at different layers (non-interleaved scheme), for better crosstalk shielding performance
- Breakout length and spacing: An initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. But the total breakout length should still be within the length defined for each topology.
- Trace Geometry: For Gen 2x1 (10 Gb/s), it is recommended to use 80-ohm trace geometry (with larger trace width), primarily to address routing insertion loss at 10Gbps. For Gen 1x1 (5 Gb/s), it is recommended to use 85-ohm trace geometry (narrower trace width), for PCB real estate saving. It is worth noting that Gen 2x1 (10 Gb/s) with 80-ohm trace geometry is fully functional and backward compatible with Gen 1x1 (5 Gb/s) 5Gbps signaling.
- Via stub: Channel and Via stub requirement must meet <381um for both Tx and Rx signal pairs
- Via anti-pad: Oval anti-pad size of 1.016mm is required for better impedance matching



- AC capacitor value: 100nF nominal (75-265nF range)
  - CMC: CMC is optional for RX lanes on Type A Connector.
  - ESD: ESD may/may not be required depending on the 3rd party's device. On the removal of discrete ESD, there are two requirements have to be met:
    - a) Mux/Re-driver can handle the ESD at least 8kV
    - b) Mux/Re-driver to be placed near to USB-C connector (< 25.4mm)
- Refer to 3rd party component specification.

## 6.8.6 USB 3.2 Optimization Guidelines

### USB Connector/Receptacle Recommendations

- Proper connector choice is critical to ensure adequate USB signal quality.
- Empirical data has shown that quad-stack USB and DisplayPort\*/USB stack connectors may cause Signal quality degradation.
- Proper selection of a motherboard mating connector with USB 3.2 Gen 2x1 (10 Gb/s) support is important to ensure signal quality is not adversely affected due to a poor connector design.
- Refer to [usb.org](http://usb.org) for a list of tested connectors and receptacles.

### A-Connector Recommendations

- Signals should be launched into the connector from the bottom of the board to minimize the through-hole stub effect. The connector footprint shall have the following through-hole dimensions: 0.7112mm finished hole, 1.0922mm pad, and 1.016mm anti-pad

### USB 3.2 Mobile Internal Connector

- It is possible to define the Mobile internal connector pin list based on individual needs. However, an example connector pin list for 2-port USB3 internal cable connection is shown in the following table.

**Table 80. Example of Mobile Internal Connector Pin Assignment and Description for Two-Port USB 3.2 Gen 2x1 (10 Gb/s)**

Pin Number	Signal	Description
1	RSVD	Reserved pin
2	Vbus	5 V bus power
3	Vbus	5 V bus power
4	Vbus	5 V bus power
5	USB2P_1	USB2 Port 1 D+
6	USB2N_1	USB2 Port 1 D-
7	PWR_GND	Power GND return
8	USB2P_2	USB2 Port 2 D+
9	USB2N_2	USB2 Port 2 D-
10	PWR_GND	Power GND return
11	USB3_1_TXP	USB3 Port 2 SuperSpeed Tx+
12	USB3_1_TXN	USB3 Port 2 Super Speed Tx-
13	SIG_GND	Signal GND return
14	USB3_1_RXP	USB3 Port 2 SuperSpeed Rx+
15	USB3_1_RXN	USB3 Port 2 Super Speed Rx-
16	SIG_GND	Signal GND return
17	USB3_2_TXP	USB3 Port 2 SuperSpeed Tx+
18	USB3_2_TXN	USB3 Port 2 Super Speed Tx-

*continued...*

Pin Number	Signal	Description
19	SIG_GND	Signal GND return
20	USB3_2_RXP	USB3 Port 2 SuperSpeed Rx+
21	USB3_2_RXN	USB3 Port 2 SuperSpeed Rx-
22	SIG_GND	Signal GND return

## 6.8.7 USB 3.2 Disabling and Termination Guidelines

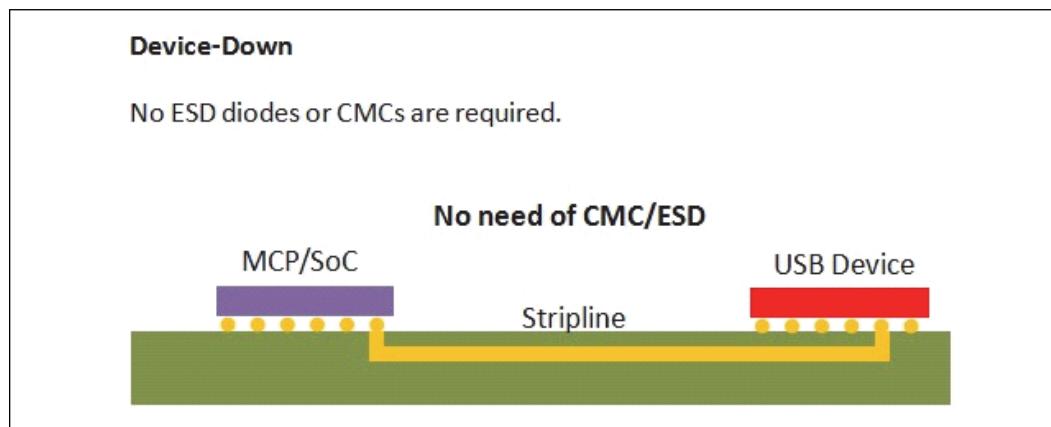
If some of the USB 3.2 port(s) are not implemented on the platform, USB3Tp/n [x] and USB3Rp/n [x] signals may be left unconnected, where 'x' is the port number left no connect.

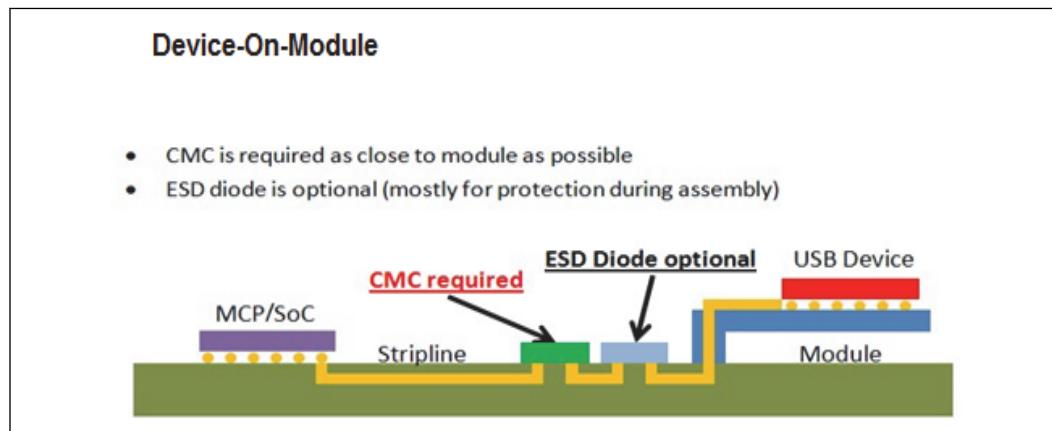
## 6.8.8 Motherboard Down USB Devices

### NOTE

Intel recommends that USB 2.0 motherboard-down devices be routed to USB 2.0 connectors that are not paired with USB 3.2 signals to allow the USB 3.2 pairs to be used with SuperSpeed devices.

**Figure 73. Device-Down**



**Figure 74. Device-On-Module****6.8.9 External End User Accessible Ports**

Designers are recommended to provide a combination of USB 2.0 only ports and USB 3.2 ports for external use on their platforms to provide the greatest amount of flexibility for legacy device support.

**6.8.10 USB Debug Port**

The xHCI controller provides a debug port capability on all USB 3.2 ports

**6.9 Universal Serial Bus 2.0 Design Guidelines**

Platform Controller Hub (PCH) has an xHCI controller and device controller implemented in it.

**Table 81. USB 2.0 Reference Documents**

Title	Doc #/Location
Front Panel I/O Connectivity Design Guide	<a href="http://www.formfactors.org/developer/specs/A2928604-005.pdf">http://www.formfactors.org/developer/specs/A2928604-005.pdf</a>

**Table 82. USB 2.0 Compliancy Documents**

Title	Doc #/Location
USB 2.0 Specification and Compliancy Requirements	<a href="http://www.usb.org">www.usb.org</a>

**6.9.1 USB 2.0 Signal Groups****Table 83. USB 2.0 Signal Groups (Sheet 1 of 2)**

Group	Signal Name	Description
DATA	USB2P USB2N	Universal Serial Bus Port Differential Pairs. Cannon Lake-H 14 USB 2.0 ports. Tiger Lake UP3 have 10 USB 2.0 ports

*continued...*

Group	Signal Name	Description
		Tiger Lake UP4 have 6 USB 2.0 ports
OVERCURRENT	<b>USB_OC0#/GPP_E9</b> <b>USB_OC1#/ GPP_A14 / DDSP_HPD3 / I2S3_RXD / DISP_MISC3 / DMIC_CLK_B1</b> <b>USB_OC2#/ GPP_A15 / DDSP_HPD4 / DISP_MISC4 / I2S4_SCLK</b> <b>USB_OC3#/ GPP_A16 / I2S4_SFRM</b>	Overcurrent Indicators
BIAS	<b>USB2_COMP</b>	Resistor Bias
<p><b>Note:</b> The supported connectors are Type A Dual Stack and Type A Single Stack. The connectors must meet the USB2.0 Connector Specification.</p>		

## 6.9.2 USBCOMP Connection Guidelines

- Short the USB2\_COMP pins at the package and then route on the top layer to one end of a  $113\ \Omega \pm 1\%$  resistor to ground.
- Route signal using  $50\ \Omega$  single-ended impedance and 12.7-mm max trace length and no longer than 11.43mm to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 0.381mm.

## 6.9.3 USBCOMP Routing Guidelines

**Table 84. USBCOMP Routing Guidelines**

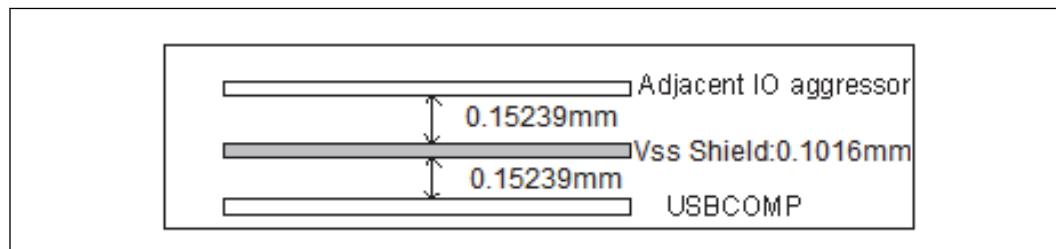
Signal	Trace Width (W) and Isolation Spacing (S)	Resistor Value	Length
USB2_COMP	No hard value for trace width and isolation spacing as long as DCR is met <i>Note:</i> : Must maintain low DC resistance routing ( $< 0.5\Omega$ )	$113\ \Omega \pm 1\%$ connected to GND	M1/M1' + M2
<p><i>Notes:</i> 1. Although there is no hard value for max topology length as long as the DC resistance routing spec is met, although it is recommended to route the USB2_COMP using 50 single-ended impedance and as short as possible; a general recommendation is to maintain a length of &lt;25.4mm, which will make it easier to hit the targeted DCR.</p> <p>2. Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 0.381mm</p>			

## 6.9.4 USB2\_COMP to Other Interfaces

If unable to implement a Vss shield for USB2\_COMP, the minimum spacing between USB2\_COMP and other traces should be at least 0.381mm to provide proper isolation.

If Vss shielding is implemented, then the spacing guideline in the figure below should be followed:

**Figure 75. Spacing Guideline for USBCOMP**



### 6.9.5 Overcurrent Protection

Tiger Lake processor has implemented programmable USB Overcurrent signals. The 74 overcurrent pins are to be shared across the USB 2.0 ports and USB 3.2 ports. This allows the platform designer flexibility in routing of the OC pins and allows for unused pins to be configured as GPIOs.

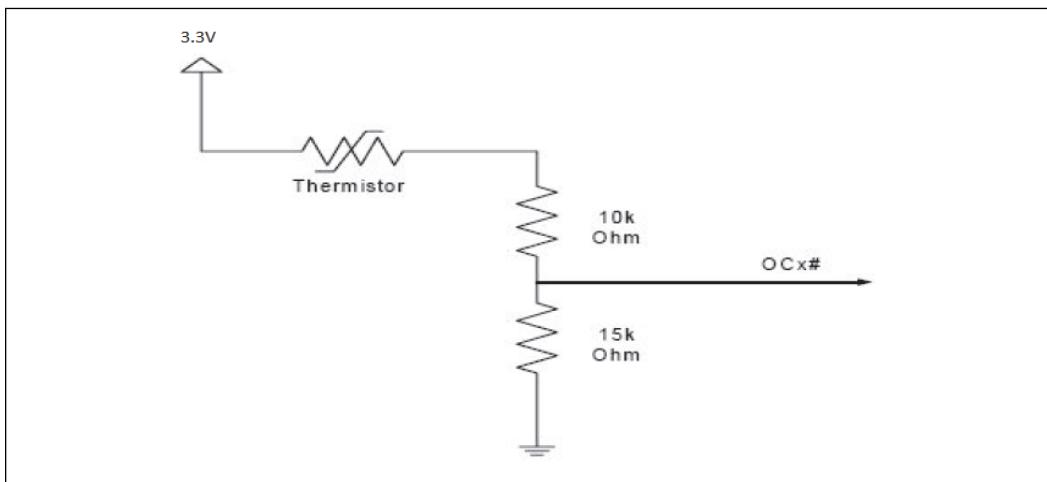
When configured for overcurrent protection, each of the OC pins needs to be connected to an external over current protection circuit. It is important to choose the correct current rating for the thermistor. Each USB port may draw up to 500 mA. The overcurrent protection circuitry needs to be able to support at least 2 A to ensure proper functionality of USB compliant devices. However, if a fault device is plugged into the USB port, it should trigger an overcurrent when current is more than 500 mA is drawn. Designer must balance between optimum cost and protection level.

#### NOTES

1. When the current rating of the protection circuit has been decided, it is crucial to ensure that the overcurrent layout is designed to support the amount of current expected.
2. The overcurrent circuit should be designed to support up to 2 A, the overcurrent trace layout should be using a big fat trace or plane that can sustain at least 2 A.

#### Warning:

1. Failure to design the trace to support high current may cause the trace on motherboard to burn out and cause permanent damage to the protection circuit.
2. The overcurrent signals require a pull-up to the 3.3 V Suspend Rail with 8.2–10 KΩ resistor (refer figure below).

**Figure 76. Sample Overcurrent Protection Circuit**

Each overcurrent pin is configured to protect one or more USB ports by setting bits in the U2OCM1 register in the xHCI controller.

**NOTE**

It is the responsibility of system software (BIOS) to program the overcurrent registers of the given USB controller correctly and to make sure that each USB port is protected by only one overcurrent pin. Operation with more than one overcurrent pin mapped to a port is undefined.

**Overcurrent Pin Mapping**

It is not recommended that customers map more than four USB ports to a single OC pin. Refer Tiger Lake PCH-LP External Design Specification (576591) for more details on how to map OC pins to USB ports.

## 6.9.6 Integrated Bluetooth\* and USB 2.0 Design Considerations

**Tiger Lake UP3**

For integrated Bluetooth\* functionality with the Intel® Wireless-AC (CNVi) solution, Tiger Lake PCH-LP USB 2.0 port # 10 must be used.

If integrated Bluetooth\* functionality is not desired, Tiger Lake UP3 USB 2.0 port 10 may be used for USB functionality.

**Tiger Lake UP4**

Please refer to TGL PCH LP EDS Vol-1 for TGL UP4 USB 2.0 port mapping

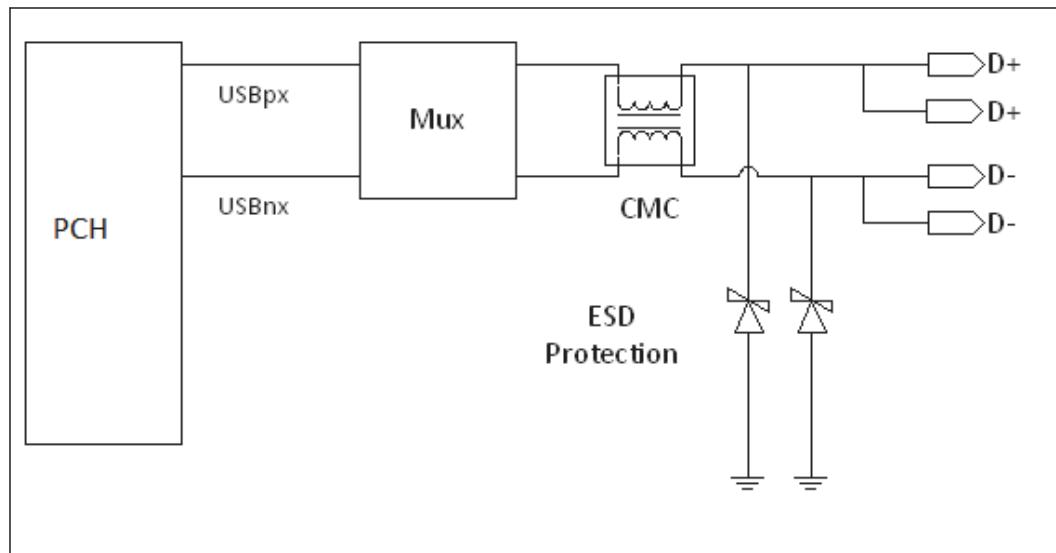
## 6.9.7 USB 2.0 Type-C Topology Guidelines

**USB 2.0 Guidelines**

USB Type-C can be configured to support USB signals only (LS,FS,HS,SS) with a minimum requirement of USB 2.0 (LS, FS, HS) support. Below are the options available for implementing USB2 topologies

- USB 2.0 Only
- USB 2.0 Only to USB Type-C Connector with BC1.2 Charger Module/MUX/Power Switch
- USB 2.0 Only with MUX and Re-driver topology

**Figure 77. USB 2.0 Only USB Type-C Connector**



#### NOTE

The figure above is a high level example implementation block, actual implementation on schematic may vary.

USB 2.0 is the minimum requirement for implementing a USB Type-C connector. This configuration is achieved by connecting a pair of USB 2.0 signal to DP+/DP- pins on the receptacle and shorting the 2 DP+/DP- on the receptacle together. On Tiger Lake, all ports are capable of supporting dual role but only one port at a time.

CC1/CC2 is no longer required to handle plug orientation detection in this configuration as there is no switching needed. However discrete CC logic is still needed for handling UFP/DFP detection, Vconn switching and VBUS control.

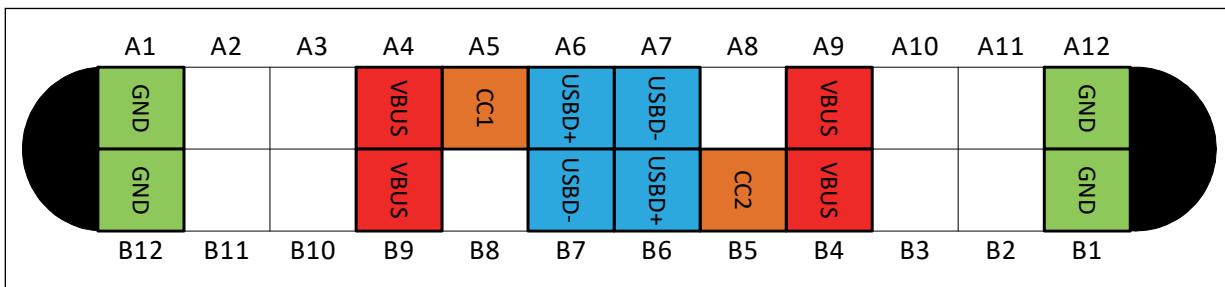
ESD protection devices is required for all signal connecting to Tiger Lake directly. For signals that is connected to 3rd party component like MUX/controller, refer to 3rd Party component specification to decide if platform level ESD device is needed.

CMC may be required to pass EMI test therefore a CMC footprint is recommended.

USB\_ID and VBUS\_SENSE pins are not needed for USB Type-C implementation with Type-C port controller (TCPC).

It is strongly recommended to include the use of ESD protection devices on each USB data signals.

**Figure 78. USB Type-C Receptacle Pin Map – USB 2.0 Only**



#### Notes or Re-Driver Component:

This section provides the necessary guidelines for customers who intend to use re-driver in one of the aforementioned USB 2.0 topologies. Terms such as "re-timer", "repeater", and "re-driver" can be used to describe similar devices: active components used to amplify a signal passing through them. The definitions below are not exhaustive and are only applied in this document in the context of serial links.

**Re-driver:** An active component, which may have receiver equalization, transmitter de-emphasis, analog signal amplification, etc., to better "shape" the signals passing through it. Re-drivers do not perform retiming (i.e., the device does not implement any interface protocol and no re-sampling is performed). Because it changes the analog behavior of the incoming signals, the propagation of jitter, noise and other analog effects from one connected channel to the other must be considered.

**Re-timer:** An active component that performs re-sampling of the incoming signal. Because no analog effects are propagated from its' inputs to its outputs, the transmitter and receiver portions of the device can be treated as independent endpoints devices.

## 6.9.8 USB 2.0 Supported Topologies

### Back Panel/External Topology

The external topology refers to the routing of USB signals to a standard USB A connector. It is recommended that each USB data line be routed with a common mode choke and ESD protection.

### USB2.0 On-the-go Topology

### USB2.0 M.2 Topology

### USB 2.0 Internal Cable Topology/Front Panel Topology

This topology supports a low profile internal connector, internal cable solution and a daughter card.

---

#### NOTE

The Internal cable guidelines will be defined using insertion loss budget rather than cable length where a recommended mobile internal cable has a loss of 2 dB @ 2.5 GHz.

Design Constraint: Differential vias, CMC, ESD and connector voiding (strongly recommended) are required to optimize impedance mismatch in the channel.

It is strongly recommended to include the use of ESD protection devices on each USB data signals.

### **USB 2.0 Docking Topology**

Consider the following guideline:

- Total trace length will influence the USB transmit amplitude setting. USB Initialization Registers can be set according to recommendations available in *Tiger Lake PCH-LP External Design Specification*.
- This topology meets USB 2.0 specifications if a trace length on the motherboard (M\_MB\_LEN) is >101.6mm and the length of M1 ≠ M2. At very short motherboard lengths of 76.2-101.6mm with M1 = M2 is this topology may not meet the USB 2.0 electrical specifications. Using a dock with integrated USB Hub may increase the routability of this topology.

#### **NOTE**

Via placement is compensable. If vias are not used on the main motherboard, then additional via can be placed on the docking board and vice versa. However, total number of vias in entire channel is 3.

### **USB 2.0 Device Down Topology**

#### **USB 2.0 External / Back Panel or On-The-Go with Power Switch / BC1.2 Charger Module / MUX Topology**

The external topology refers to the routing of USB 2.0 signals to a standard USB A connector. It is recommended that each USB data line be routed with a common mode choke and ESD protection. A Power switch / BC1.2 charger controller/ MUX /USB PD (BC1.2 detection) module is present in the topology.

- Current electrical characteristic recommendation on Power switch/controller/MUX for charging is to have on-state resistance and on-state capacitance of no greater than 6 Ω and 6pF respectively.
- Current electrical characteristic limitation on Power switch/controller/MUX for charging is insertion loss of no greater than -0.6 dB and return loss of no greater than -13 dB.
- For a maximum length channel of 127mm – it is recommended that the length of M8\_Charger\_Length be 50.8mm and a minimum of 38.1mm.
- The total channel (including the MUX/BC1.2 charger/power switch module) insertion loss should not exceed -2.95 dB and return loss should not exceed -8.5 dB.
- The length of the main board channel can be increased by trading-off the insertion loss (at 240 MHz) and equivalent on-state resistance and on-state capacitance of the BC1.2 charger module/power switch/MUX. The maximum on-state resistance and on-state capacitance as well as insertion loss allowable for the module is dependent on the total board routing as shown in USB2.0 BC1.2 / MUX/ Power switch Component Restrictions.

## USB 2.0 Detachable Docking Topology

Careful attention should be given to the docking connector design as well as its associated internal cables and sub/base boards to ensure that signal quality is not degraded. A USB 2.0 Hub is required on the docking board. Since different Hub chips have different characteristics, contact your Hub Vendor for routing guidelines from the Hub to A-connector. It is recommended that each USB data line be routed with a common mode choke and ESD protection from the Hub to A-connector.

Docking topologies shown in this document, should only be implemented on Windows\* designs.

### 6.9.9

## USB Connector Recommendations

Proper connector choice is critical to ensure adequate USB signal quality. Empirical data has shown that quad-stack USB and DisplayPort\*/USB stack connectors may add interference causing poor USB signal quality. Refer to [usb.org](http://usb.org) for a list of tested connectors.

### External Connector Recommendations

The cable and PCB mating connector must pass the TDR (Time Domain Reflectometry) requirements listed in the USB 2.0 Specification.

### USB 2.0 Mobile Internal Connector

It is possible to define the internal connector pin list based on individual needs. However, an example connector pin list for 2-port internal cable connection supporting both USB 2.0 and USB 3.2 is shown in the following table.

**Table 85. Example of Internal Connector Pin Assignment and Description**

Pin Number	Signal	Description
1	RSVD	Reserved Pin
2	Vbus	5 V bus power
3	Vbus	5 V bus power
4	Vbus	5 V bus power
5	USB2_DIP	USB 2.0 Port 1 D-
6	USB2-DIN	USB 2.0 Port 1 D+
7	PWR_GND	Power GND return
8	USB2_D2P	USB 2.0 Port 2 D+
9	USB2_D2N	USB 2.0 Port 2 D-
10	PWR_GND	Power GND return
11	USB3_TX1P	USB 3.2 Port 2 SuperSpeed Tx+
12	USB3_TX1N	USB 3.2 Port 2 SuperSpeed Tx-
13	SIG_GND	Signal GND return
14	USB3_RX1P	USB 3.2 Port 2 SuperSpeed Rx+
15	USB3_RX1N	USB 3.2 Port 2 SuperSpeed Rx-

*continued...*

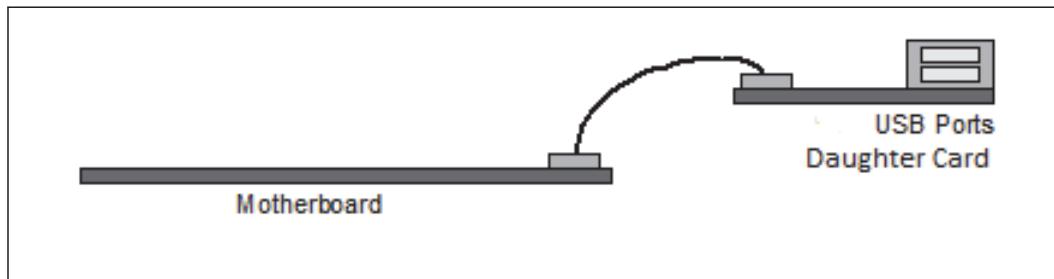
Pin Number	Signal	Description
16	SIG_GND	Signal GND return
17	USB3_TX2P	USB 3.2 Port 2 SuperSpeed Tx+
18	USB3_TX2N	USB 3.2 Port 2 SuperSpeed Tx-
19	SIG_GND	Signal GND return
20	USB3_RX2P	USB 3.2 Port 2 SuperSpeed Rx+
21	USB3_RX2N	USB 3.2 Port 2 SuperSpeed Rx-
22	SIG_GND	Signal GND return

## 6.9.10 Daughter Card

The best way to provide internal support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. The following figure shows the major components associated with a typical USB solution that uses a daughter card.

When designing the motherboard with internal topology support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there are not duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

**Figure 79. Daughter Card**



### Daughter Card Design Guidelines

The followings are recommended when designing a USB 2.0 daughter card:

- Place the VBUS bypass capacitor, CMC, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Use the same mating connector pinout as - USB 3.1 Internal Connector Pinout (Motherboard).
- Minimize the trace length on the daughter card - Less than a 50.8mm trace length is recommended.
- Use the same routing guidelines as described in USB 2.0 Stack-up Guidelines. Refer to PCB Stack-Up and Design Considerations, for specific PCB type routing guide.

- Power and ground nets should have double vias. Trace lengths should be kept as short as possible.

### 6.9.11 Stack-Up and Layer Utilization Guidelines

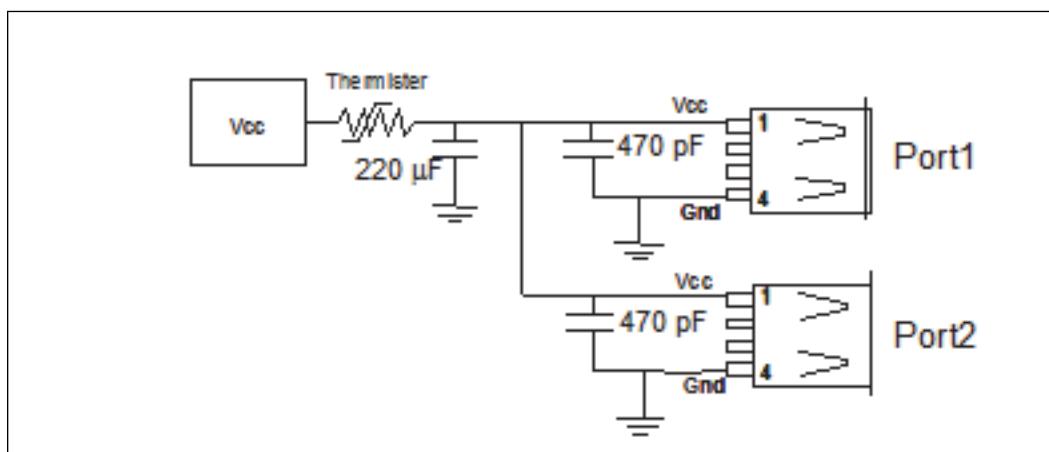
Refer to PCB Stack-Up and Design Considerations - Type 3 and Type 4 Stack-up sections for all I/O routing guidelines including USB 2.0.

### 6.9.12 Port Power Delivery

The following is a suggested topology for power distribution of VBUS to USB ports. These circuits provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach flyback protection. These two types require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). Intel recommends the following:

- Minimize the inductance and resistance between the coupling capacitors and the USB ports.
- Place capacitors close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane.
- Make the power-carrying traces wide enough that the system fuse blows on an overcurrent event. If the system fuse is rated at 1 A, then the power-carrying traces should be wide enough to carry at least 1.5 A.

**Figure 80. Good Downstream Power Connection**



### 6.9.13 USB 2.0 Length Matching Guidelines

Refer Platform Design Guide excel sheet for length matching guidelines.

### 6.9.14 EMI and ESD Protection

Refer Electromagnetic Compatibility in Platform Design Guide excelsheet.

### 6.9.15 USB 2.0 Disabling and Termination Guidelines

If a USB port(s) is not implemented on the platform:

USB P/N [x] signals can be left unconnected.

## 6.10 Legacy Audio Interface Design Guidelines

This platform is a next-generation architecture for audio that allows audio output and input streams to be processed by the host IA processor or for processing to be offloaded from IA processing via the next generation Intel® Smart Sound Technology DSP.

This design guideline chapter includes the routing details for different legacy audio interfaces that connect to the PCH. These are as follows:

- Intel® High Definition Audio ( Intel® HD Audio) Interface
- Digital Microphone (DMIC) Interface
- Integrated Interchip Sound (I<sup>2</sup>S) Interface

### 6.10.1 Legacy Audio Interface Platform Specific Important Information

In this section, Intel HD Audio interface is compliant with Microsoft\* Universal Audio Architecture (UAA). Contact your IHV (Independent Hardware Vendor) for information on Intel HD Audio, I<sup>2</sup>S, and DMIC based products.

On the Tiger Lake platform the Intel HD Audio, I<sup>2</sup>S, and DMIC interfaces are multiplexed with each other as well as other interfaces to allow flexibility in pin usage. Refer Tiger Lake PCH-LP External Design Specification (#576591) for specific sku pins assignments and multiplexing details.

### 6.10.2 Legacy Audio Interface - Signal Description

**Table 86. Legacy Audio Signals**

Signal Name	Description
<b>Intel® High Definition Audio Interface</b>	
HDA_RST#	Master hardware reset to external codec(s)
HDA_SYNC	48 KHz fixed rate sample sync to the codec(s)
HDA_BCLK	24.000 MHz serial data clock generated by the Intel® HD Audio controller.
HDA_SDO	Serial TDM data output to the codec(s)
HDA_SDIN [1:0]	Serial TDM data inputs from the codec(s)
<b>I<sup>2</sup>S Interface</b>	
I2S_MCLK1	I <sup>2</sup> S* Master Clock Output
I2S_MCLK2_INOUT	Second I <sup>2</sup> S* Master Clock Output. Can be configured as input as a reference clock.
I2S[5:0]_SCLK	I <sup>2</sup> S Serial Bit Clocks for connections to I <sup>2</sup> S devices.
I2S[5:0]_TXD	I <sup>2</sup> S Transmit Data (Serial Data Out) for connection to I <sup>2</sup> S devices.
I2S[5:0]_RXD	I <sup>2</sup> S Receive Data (Serial Data In) for connection to I <sup>2</sup> S devices.
I2S[5:0]_SFRM	I <sup>2</sup> S Serial Frame for connection to I <sup>2</sup> S devices.
<b>DMIC Interface</b>	
DMIC_CLK_A[1:0]	Serial data clock to module A (left microphone) DMIC on interface/port 0 or 1.
DMIC_CLK_B[1:0]	Serial data clock to module B (right microphone) DMIC on interface/port 0 or 1.
DMIC_DATA[1:0]	Serial data input from the digital microphone module

Signal Name	Description
DMIC_CLK_A[1:0]	Serial data clock to module A (left microphone) DMIC on interface/port 0 or 1.
DMIC_CLK_B[1:0]	Serial data clock to module B (right microphone) DMIC on interface/port 0 or 1.
DMIC_DATA[1:0]	Serial data input from the digital microphone module

### 6.10.3 Intel® High Definition Audio (Intel HD Audio) and DMIC Topology Guidelines

The PCH supports a single Intel HD Audio Interface that supports up to two devices

The DMIC interface has been changed from previous chipset generations allowing up to 2 clocks for each of the two DMIC interfaces. This allows left and right DMIC modules to have their own unique clocks that can be powered down independently. The PCH will also support DMIC configurations of sharing a single clock to both stereo DMIC modules as was supported in previous chipsets. When using the Intel HDA Audio and DMIC interface the following topologies are supported:

- Intel HD Audio 1-Load Topology (Device Down)
- DMIC 1-Load CLK Topology (For 2-Load Branch Add-In Card) - Separate clock to each DMIC module while Data signal is shared in a branched configuration.
- DMIC 2-Load Branch Topology (Add-In Card) - Shared clock and data signal to each DMIC module branched on the add-in card.
- DMIC 1-Load CLK Topology (For 2-Load Daisy) - Separate clock to each DMIC module while Data signal is shared in a daisy chain configuration.
- DMIC 2-Load Daisy Topology - Shared clock and data signal to each DMIC module in a daisy configuration.

#### Disabling and Termination Guidelines for High Definition Audio Interface

When HDA\_SDIN[1:0] interface is not implemented on the platform the signal pin(s) may be left unconnected.

### 6.10.4 Intel® I2S\* Topology Guidelines

When the I2S interface is used, the following guidelines should be used for routing to end devices. The following topologies are supported:

- 1-Load Topology Master Mode (Device Down)
- 1-Load Topology Slave Mode (Device Down)
- 1-Load Topology Master Mode (Add-In Card)
- 1-Load Topology Slave Mode (Add-In Card)
- 1-Load Topology Master Mode (Cable to Add-In Card)

## 6.11 SoundWire\* Interface Design Guidelines

For the Tiger Lake platform, SoundWire\* is still the newest audio interface targeting (but not limited to) the phone, mobile, and desktop market as an alternative to Slimbus. Its main advantage is the connection simplicity with a 2 wire multi-drop topology + PDM streaming capabilities. For the Tiger Lake PCH there are 4 separate SoundWire interfaces that can be used.

## 6.11 SoundWire\* Interface Design Guidelines

For the Tiger Lake platform, SoundWire\* is still the newest audio interface targeting (but not limited to) the phone, mobile, and desktop market as an alternative to Slimbus. Its main advantage is the connection simplicity with a 2 wire multi-drop topology + PDM streaming capabilities. For the Tiger Lake PCH there are 4 separate SoundWire interfaces that can be used.

### 6.11.1 SoundWire\* Platform Specific Important Information

On the Tiger Lake platform the SoundWire\* interface and other audio interfaces can be configured by itself or at the same time with other interfaces for connection to end devices. Refer Tiger Lake PCH-LP External Design Specification (#576591) for specific sku pins assignments.

### 6.11.2 SoundWire\* Signal Description

**Table 87. SoundWire\* Signals**

Signal Name	Description
SNDW0_DATA	SoundWire Data 0: Serialized data line containing frame and data being transmitted /Received
SNDW0_CLK	SoundWire Clock 0: Serial bit clock used to control the timing of a transfer.
SNDW1_DATA	SoundWire Data 1: Serialized data line containing frame and data being transmitted /Received
SNDW1_CLK	SoundWire Clock 1: Serial bit clock used to control the timing of a transfer.
SNDW2_DATA	SoundWire Data 2: Serialized data line containing frame and data being transmitted /Received
SNDW2_CLK	SoundWire Clock 2: Serial bit clock used to control the timing of a transfer.
SNDW3_DATA	SoundWire Data 3: Serialized data line containing frame and data being transmitted /Received
SNDW3_CLK	SoundWire Clock 3: Serial bit clock used to control the timing of a transfer.

### 6.11.3 SoundWire\* Topology Guidelines

There are several topologies supported in Tiger Lake for SoundWire\*:

- Large System: 1-Load Topology (Add-in Card)
- Large System: 2-Load Star Topology (Add-in Card)
- Large System: 2-Load Daisy Chain Topology (Add-in Card)
- Large System: 4-Load Daisy Chain Topology (Add-in Card)
- Small System: 1-Load Topology (Device Down)
- Small System: 3-Load Daisy Chain Topology (Device Down)
- Small System: 4-Load Daisy Chain Topology (Device Down)

### 6.11.4 Additional Guidelines - SoundWire\* Interface Design Guidelines

#### Adjusting Drive Impedance for Down Devices

In the topology section the device buffer strength target recommendations are different depending on the Topology and its configuration. If devices used do not have buffer strengths that match the target recommendations and do not have the ability to adjust the buffer strengths through software you can adjust the impedance via an external resistor (R1) in series near the device, between the device and PCH. To determine R1 the formula is:  $R1 = \text{Device Buffer Impedance Target} - \text{Actual Device Buffer Impedance}$ .

Example:

- Device Drive Impedance Target = 80ohms
- Device Buffer Impedance = 45ohm
- $R1 = 80\text{ohm} - 45\text{ohm} = 35\text{ohm}$

## 6.12 Generic Serial Peripheral Interface (GSPI)

### 6.12.1 GSPI Platform- Specific Important Information

The PCH's three generic SPI (GSPI) interfaces support devices which use SPI serial protocols for transferring data.

Each interface consists of 4 wires: a clock (CLK), two chip select (CS) and 2 data lines (MOSI and MISO).

The PCH generic SPI is full-duplex synchronous serial interface. The interface operates in master mode only, and supports serial bit rate up to 25 Mb/s. Serial data formats may range from 4 to 32 bits in length.

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#### NOTE

The GSPI is not the same as the PCH SPI interface for flash devices. This GSPI is used mainly for sensor support on the platform.

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### 6.12.2 GSPI Signal Descriptions

#### Signal Groups

**Table 88.** GSPI Signals

Group	Signal Name	Description
Clock	GSPI0_CLK GSPI1_CLK GSPI2_CLK	Clock signals
Data	GSPI0_MISO GSPI1_MISO GSPI2_MISO	Master In Slave Out signals
	GSPI0_MOSI GSPI1_MOSI GSPI2_MOSI	Master Out Slave In signals
Chip Select	GSPI0_CS0# GSPI1_CS0# GSPI2_CS0#	Chip select signals

### 6.12.3 Debug Guidelines/Recommendations

GSPI signals are multiplexed with GPIOs and default to GPIO functionality. If GSPI interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

## 6.12.4 Tools

Intel does not promote any specific tool for this interface.

## 6.13 eSPI Interface Guidelines

The Enhanced Serial Peripheral Interface (eSPI) is intended for connecting an EC to the platform.

eSPI operates at 1.8V only. This interface is not shared and distinct from the SPI interface used for flash device and TPM. The eSPI interface supports up to 50MHz and up to Quad Mode.

The interface supports both MAF (Master Attached Flash) and SAF (Slave Attached Flash).

### **6.13.1 eSPI Signal Description**

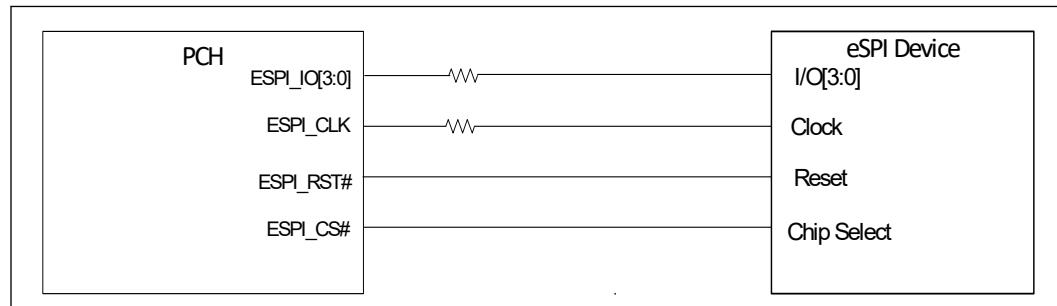
**Table 89.** eSPI Signals

Signal Name	Group	Description
ESPI_IO[3:0]	Data	Bi-directional data signals used to transfer data between PCH and eSPI slave device
ESPI_CLK	Clock	eSPI Clock output from PCH
ESPI_CS#	Control	eSPI chip select
ESPI_RESET#	Control	eSPI reset signal

eSPI Guidelines

- eSPI Single Load Topology

**Figure 81.** eSPI Topology



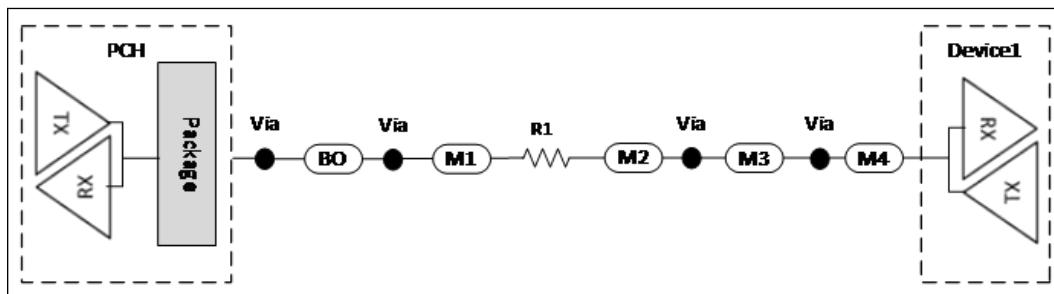
### **6.13.1.1 eSPI**

### **6.13.1.1.1 1-Load Topology (Device Down)**

Pcb Type: None

Pcb Thickness: None

**Figure 82. eSPI 1-Load Topology (Device Down) Diagram**



**Table 90. 1-Load Topology (Device Down) Notes**

Note	Detail
Number of vias allowed	7
Reference plane	Continuous ground only
Max Frequency	50MHz
Device assumption	Compliant to Intel ESPI Base Specification 1.0 (66MHz and above)
R1	33Ω on ESPI_CLK, ESPI_IO[0:3]
Minimum length	[1] M3: 12.7mm [2] M1, M2 and M4: 2.54mm
Length matching between CLK and DATA signals	12.7mm
Trace spacing between DATA and DATA signals	0.125mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	ESPI_CLK, ESPI_IO[0:3], ESPI_CS0#

### Segment Lengths

Max Length Total (mm): 165.6

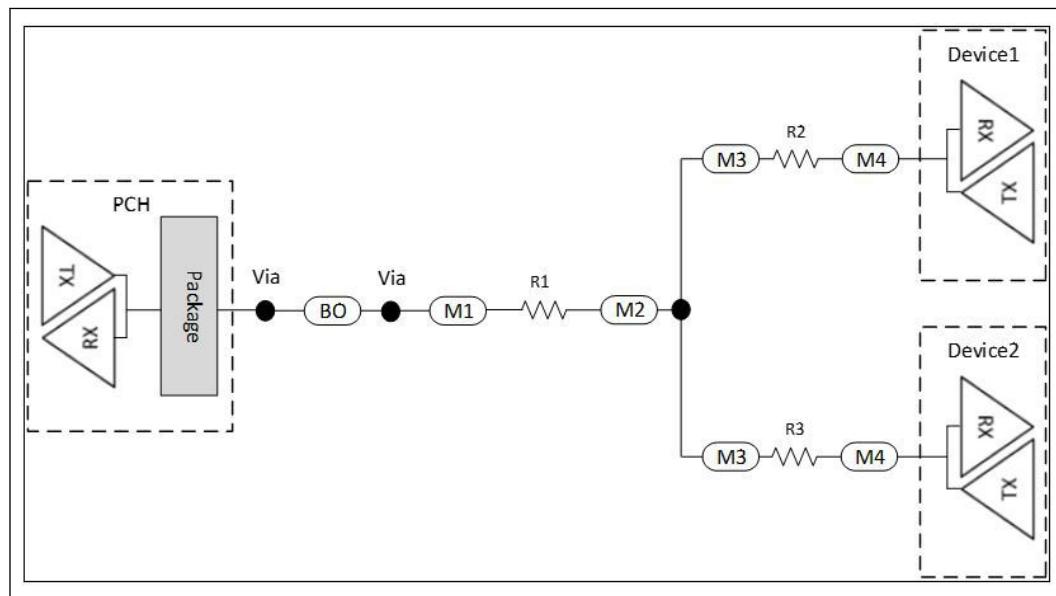
**Table 91. 1-Load Topology (Device Down) Routing Guidelines**

Segment	Tline Type	Max Length (mm)
BO	MS, SL	12.7
M1	MS	12.7
M2	MS	0.5
M3	DSL, MS, SL	127
M4	MS	12.7

### 6.13.1.1.2 2-Load Branch Topology (Device Down)

Pcb Type: None

Pcb Thickness: None

**Figure 83. eSPI 2-Load Branch Topology (Device Down) Diagram****Table 92. 2-Load Branch Topology (Device Down) Notes**

Note	Detail
Number of vias allowed	6
Reference plane	Continuous ground only
Max Frequency	[1] Device1: EC @50MHz [2] Device2: SIO/TPM @33MHz
Device assumption	Compliant to Intel eSPI Base Specification 1.0 (66MHz and above)
R1	0Ω for eSPI_CLK and eSPI_IO[0:3]
R2	22Ω for eSPI_CLK and eSPI_IO[0:3]
R3	100Ω for eSPI_CLK and eSPI_IO[0:3]
Minimum length	50.8mm
Length matching between CLK and DATA signals	12.7mm
Trace spacing between DATA and DATA signals	0.125mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	eSPI_CLK, eSPI_IO[0:3], eSPI_CS[0:1]#

### Segment Lengths

Max Length Total (mm): 215.9

**Table 93. 2-Load Branch Topology (Device Down) Routing Guidelines**

Segment	Tline Type	Max Length (mm)
BO	MS, SL	12.7
M1	DSL, MS, SL	127
M2	MS	12.7
M3	MS	12.7
M4	MS	50.8

## 6.14 Serial Peripheral Interface (SPI0) Flash Design Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting flash devices.

The Serial Peripheral Interface (SPI0) supports 2 SPI0 flash devices via 2 chip select (SPI0\_CS0# and SPI0\_CS1#). The maximum size of flash supported is determined by the SDFD-discovered addressing capability of each device. Each component can be up to 16 MB (32 MB total addressable) using 3-byte addressing. Each component can be up to 64 MB (128 MB total addressable) using 4-byte addressing. Another chip select (SPI0\_CS2#) is also available and only used for TPM on SPI0 support.

PCH drives the SPI0 interface clock at either 20 MHz, 33 MHz, or 50 MHz and will function with SPI0 flash devices that support at least one of these frequencies.

The SPI0 interface supports either 3.3V or 1.8V. Descriptor mode is required for all platforms with PCH.

A SPI0 flash device supporting SDFP (Serial Flash Discovery Parameter) is required for all PCH design. A SPI0 flash device on SPI0\_CS0# with a valid descriptor MUST be attached directly to the PCH.

**Table 94. SPI0 Signals**

Signal Name	Group	Description
SPI0_MOSI	Data	SPI0 serial output data from PCH to the SPI0 flash device. This Pin will also function as Input during Dual and Quad I/O operation
SPI0_MISO	Data	SPI0 serial input data from the SPI0 flash device to PCH. This Pin will also function as Output during Dual and Quad I/O operation
SPI0_IO2	Data	SPI0 I/O to comprehend the support for the Quad I/O operation
SPI0_IO3	Data	SPI0 I/O to comprehend the support for the Quad I/O operation
SPI0_CLK	Clock	SPI0 Clock output from PCH
SPI0_CS0#	Chip Select0	SPI0 chip select 0
SPI0_CS1#	Chip Select1	SPI0 chip select 1 signal is used as the second chip select when 2 flash devices are used. Do not use when only one SPI0 flash is used
SPI0_CS2#	Chip Select2	Chip Select is dedicated to support TPM on SPI0.

### 6.14.1 Serial Peripheral Interface (SPI0) Guidelines

SPI0 flash must be directly connected to the PCH SPI0 bus. Also, refer to the Serial Flash vendor documentation for additional Serial Flash specific design considerations.

#### NOTE

For SPI0 topology with PCH and EC G3 Flash sharing in Wire-OR Configuration, it is recommended that when VCC\_SPI is on, all primary wells (1.8 V, 3.3 V and 1.05 V) must be ON before accessing the SPI bus.

#### SPI Voltage (3.3V or 1.8V) Selection

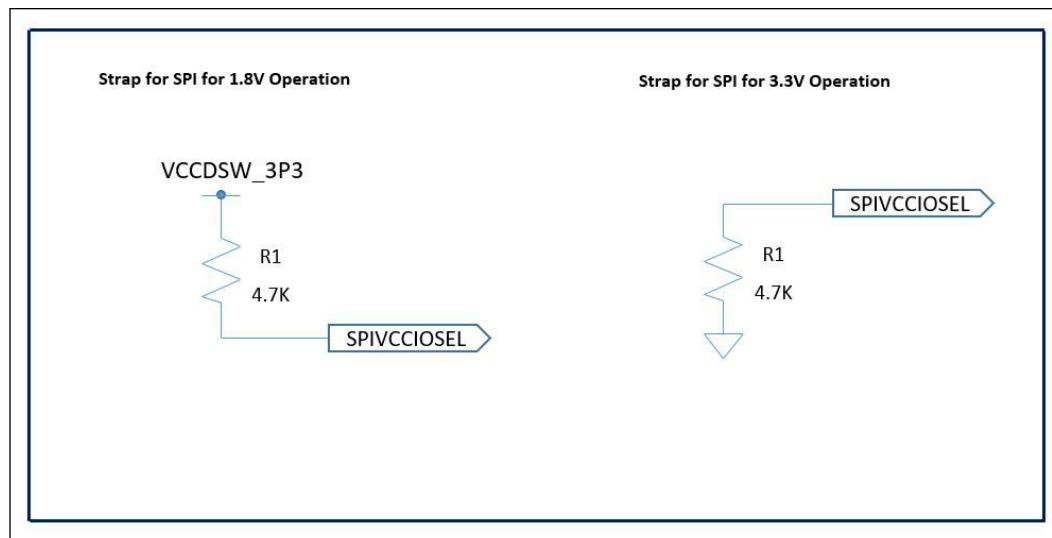
The SPI voltage (3.3V or 1.8V) is selected via a strap on **SPIVCCIOSEL**.

This strap sets the SPI interface signaling voltage at the rising edge of DSW\_PWROK. Designers should strap this pin to match the expected interface operational voltage for their target SPI device as follows.

0 = SPI voltage is 3.3V (4.7K ohm pull-down to GND)

1 = SPI voltage is 1.8V (4.7K ohm pull-up to VCCDSW\_3P3)

**Figure 84. SPI Voltage (3.3V or 1.8V) Selection**



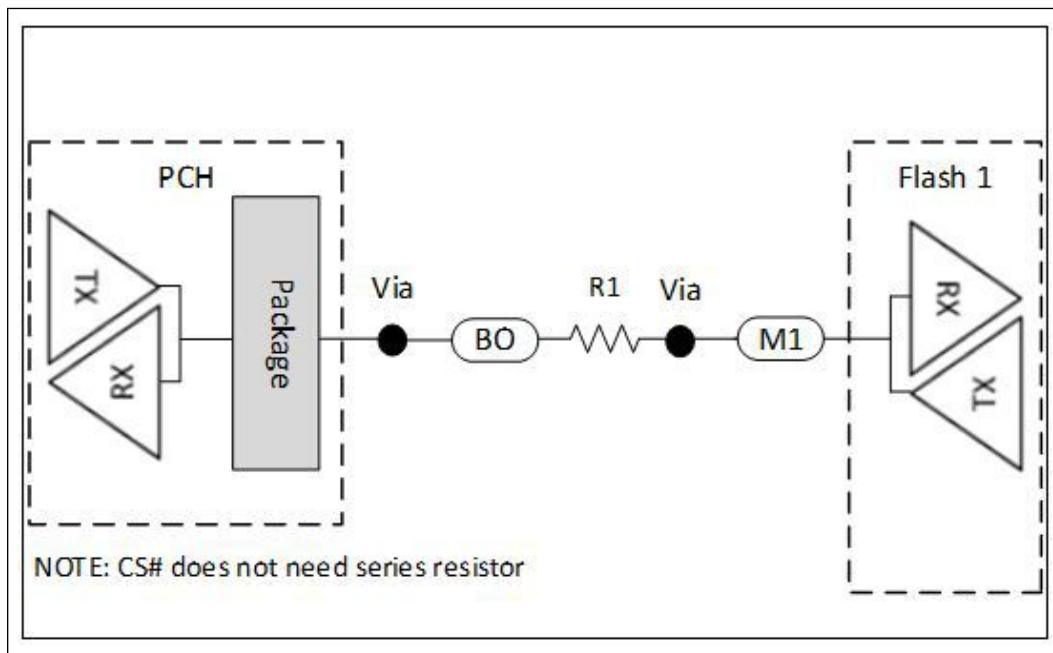
### 6.14.1.1 SPI0 Flash

#### 6.14.1.1.1 1-Load Topology (Device Down) MAF

Pcb Type: None

Pcb Thickness: None

**Figure 85. SPI0 1-Load MAF Topology Diagram**



**Table 95. 1-Load Topology (Device Down) MAF Notes**

Note	Detail
Number of vias allowed	7
Reference plane	Continuous ground only
Max Frequency	50MHz
R1	$75\Omega \pm 5\%$ for 1.8V, $62\Omega \pm 5\%$ for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3
Minimum length	M1: 50.8mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS0#

### Segment Lengths

Max Length Total (mm): 177.8

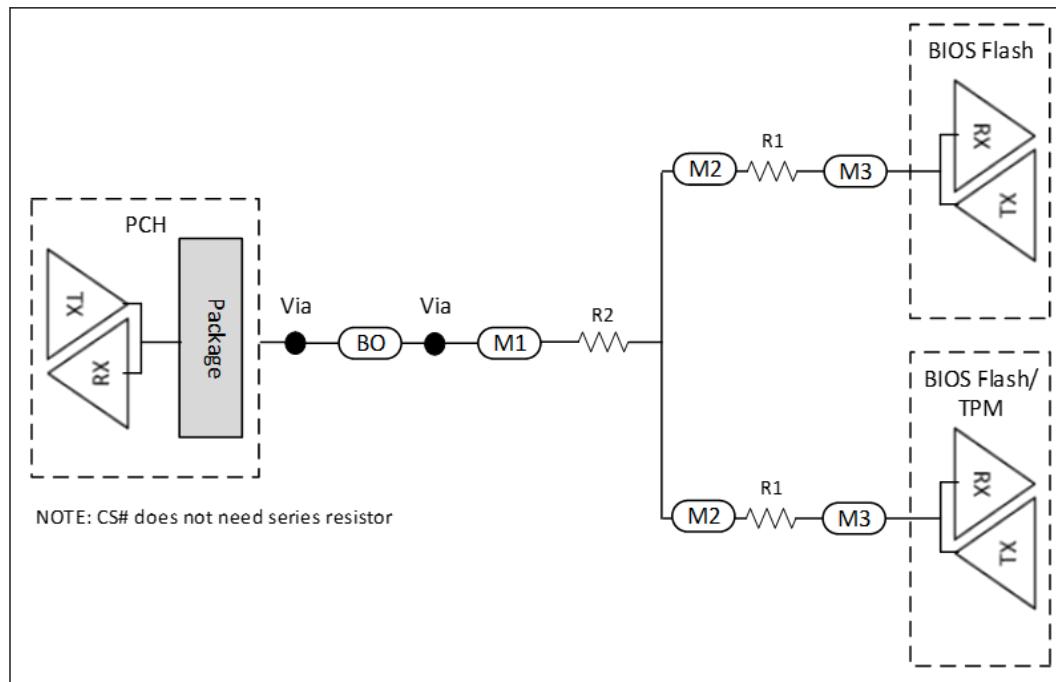
**Table 96. 1-Load Topology (Device Down) MAF Routing Guidelines**

Segment	Tline Type	Max Length (mm)
BO	MS, SL	12.7
M1	DSL, MS, SL	165.1

**6.14.1.1.2 2-Load Branch Topology (Device Down) MAF**

Pcb Type: None

Pcb Thickness: None

**Figure 86. SPI0 2-Load Branch MAF Topology Diagram****Table 97. 2-Load Branch Topology (Device Down) MAF Notes**

Note	Detail
Number of vias allowed	6
Reference plane	Continuous ground only
Max Frequency	50MHz
R1	$33\Omega \pm 5\%$ for 1.8V, $56\Omega \pm 5\%$ for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0莫斯I, SPI0_IO2 and SPI0_IO3.
R2	$5\Omega$ for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0莫斯I, SPI0_IO2 and SPI0_IO3. It is an optional to have R2 on the channel. It can be removed to reduce BOM cost.
M3	SPI branches of segment M3 need to have length matching of 2.54mm
Minimum length	M1 and M3: 25.4mm

*continued...*

Note	Detail
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Stuffing resistor	If one of devices are unstuff (rework), treat it as point-to-point topology thus place stuffing resistor as close as possible to the branch to avoid long stub length
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS0#, SPI0_CS2#

### Segment Lengths

Max Length Total (mm): 177.8

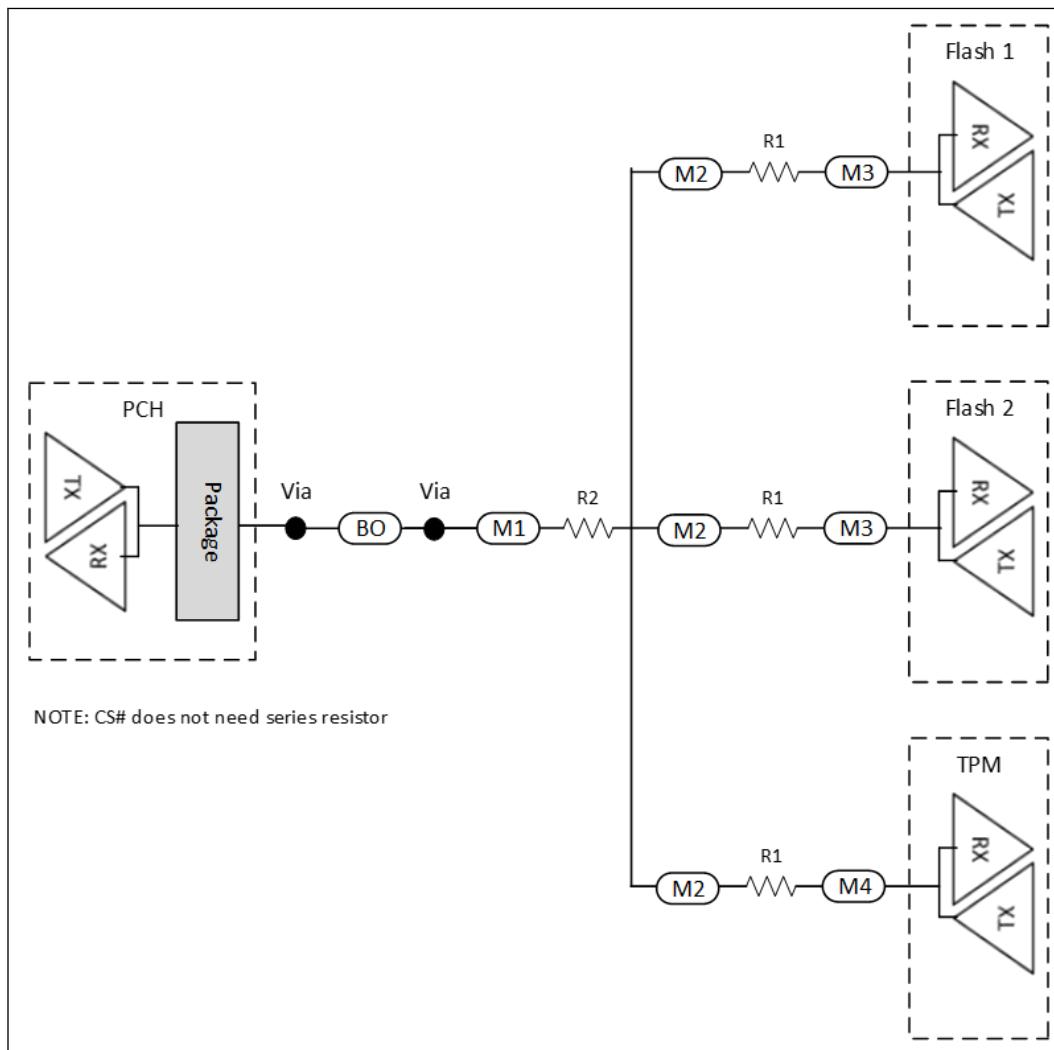
**Table 98. 2-Load Branch Topology (Device Down) MAF Routing Guidelines**

Segment	Tline Type	Max Length (mm)
BO	MS, SL	12.7
M1	DSL, MS, SL	111.8
M2	MS	2.54
M3	MS	50.8

### 6.14.1.1.3 3-Load Branch Topology (Device Down) MAF

Pcb Type: None

Pcb Thickness: None

**Figure 87. SPI0 3-Load Branch MAF Topology Diagram****Table 99. 3-Load Branch Topology (Device Down) MAF Notes**

Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Max Frequency	50MHz
R1	$27\Omega \pm 5\%$ for 1.8V, $33\Omega \pm 5\%$ for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3
R2	10Ω for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3. It is an optional to have R2 on the channel. It can be removed to reduce BOM cost.
M3	SPI branches of segment M3 need to have length matching of 2.54mm

*continued...*

Note	Detail
Minimum length	M1, M3 and M4: 25.4mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Stuffing resistor	If one of devices are unstuff (rework), treat it as point-to-point topology thus place stuffing resistor as close as possible to the branch to avoid long stub length
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA/signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS[0:1]#, SPI0_CS2#

### Segment Lengths

Max Length Total (mm): 189.7

**Table 100. 3-Load Branch Topology (Device Down) MAF Routing Guidelines**

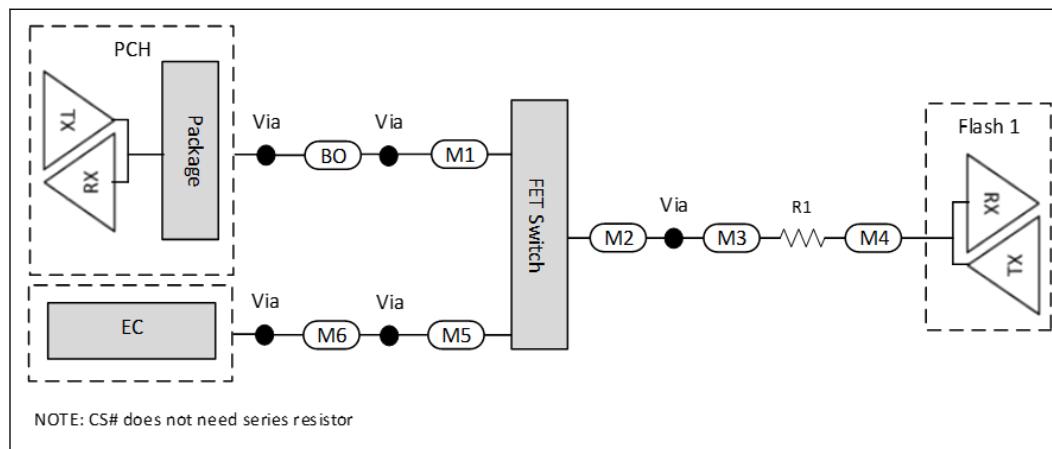
Segment	Tline Type	Max Length (mm)
BO	MS, SL	12.7
M1	DSL, MS, SL	124.46
M2	MS	2.54
M3	MS	38
M4	MS	50

#### 6.14.1.1.4 1-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing

Pcb Type: None

Pcb Thickness: None

**Figure 88. SPI0 1-Load Branch (Device Down) with EC Isolation FET Flash Sharing Topology Diagram**



**Table 101. 1-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing Notes**

Note	Detail
Number of vias allowed	7
Reference plane	Continuous ground only
Max Frequency	50MHz
R1	$33\Omega \pm 5\%$ for 1.8V, $33\Omega \pm 5\%$ for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
Minimum length	[1] M1, M4 and M5: 12.7mm [2] M2: 2.54mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
FET component criteria	$R_{on} < 8\text{ ohm}$ , $C_{in} < 14.3\text{pF}$
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS0#

### Segment Lengths

Max Length Total (mm): 177.8

**Table 102. 1-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing Routing Guidelines**

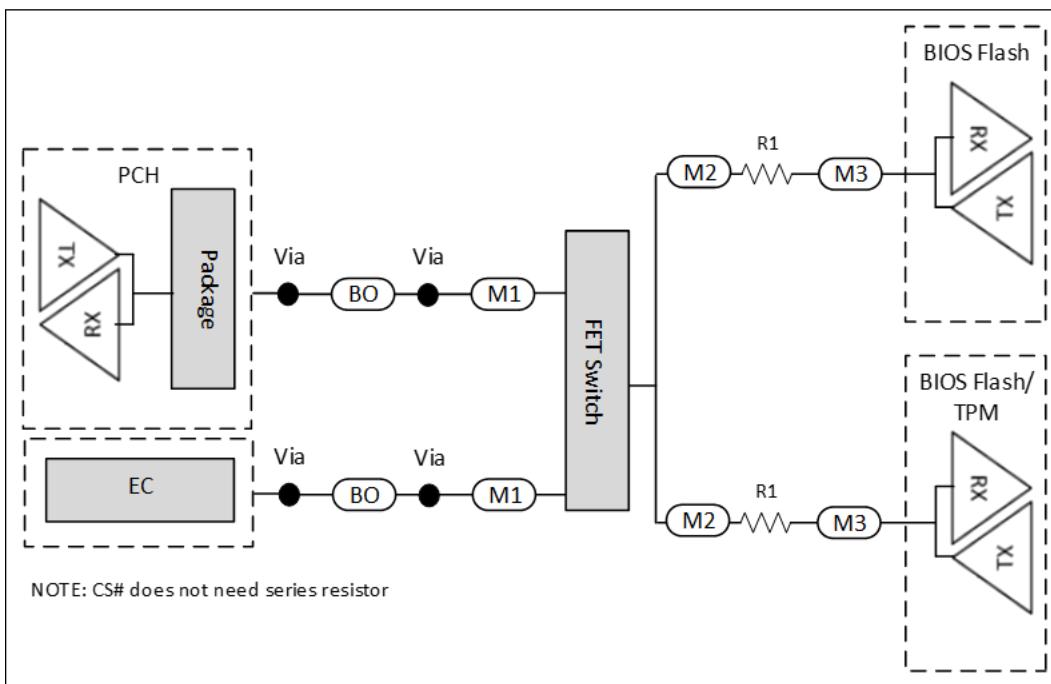
Segment	Tline Type	Max Length (mm)
BO/M6	MS, SL	12.7
M1/M5	DSL, MS, SL	50.8
M2	MS	12.7
M3	MS	2.54
M4	MS	101.6

#### 6.14.1.1.5 2-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing

Pcb Type: None

Pcb Thickness: None

**Figure 89. SPIO 2-Load Topology with EC Isolation FET Flash Diagram**



**Table 103. 2-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing Notes**

Note	Detail
Number of vias allowed	6
Reference plane	Continuous ground only
Max Frequency	50MHz
R1	$33\Omega \pm 5\%$ for 1.8V, $56\Omega \pm 5\%$ for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0莫斯I, SPI0_IO2 and SPI0_IO3.
<i>continued...</i>	

Note	Detail
M3	SPI branches of segment M3 need to have length matching of 2.54mm
Minimum length	M1 and M3: 25.4mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Stuffing resistor	If one of devices are unstuff (rework), treat it as point-to-point topology thus place stuffing resistor as close as possible to the branch to avoid long stub length
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
FET component criteria	Ron <5 ohm, Cin <3pF
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS[0:1]#, SPI0_CS2#

### Segment Lengths

Max Length Total (mm): 177.8

**Table 104. 2-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing Routing Guidelines**

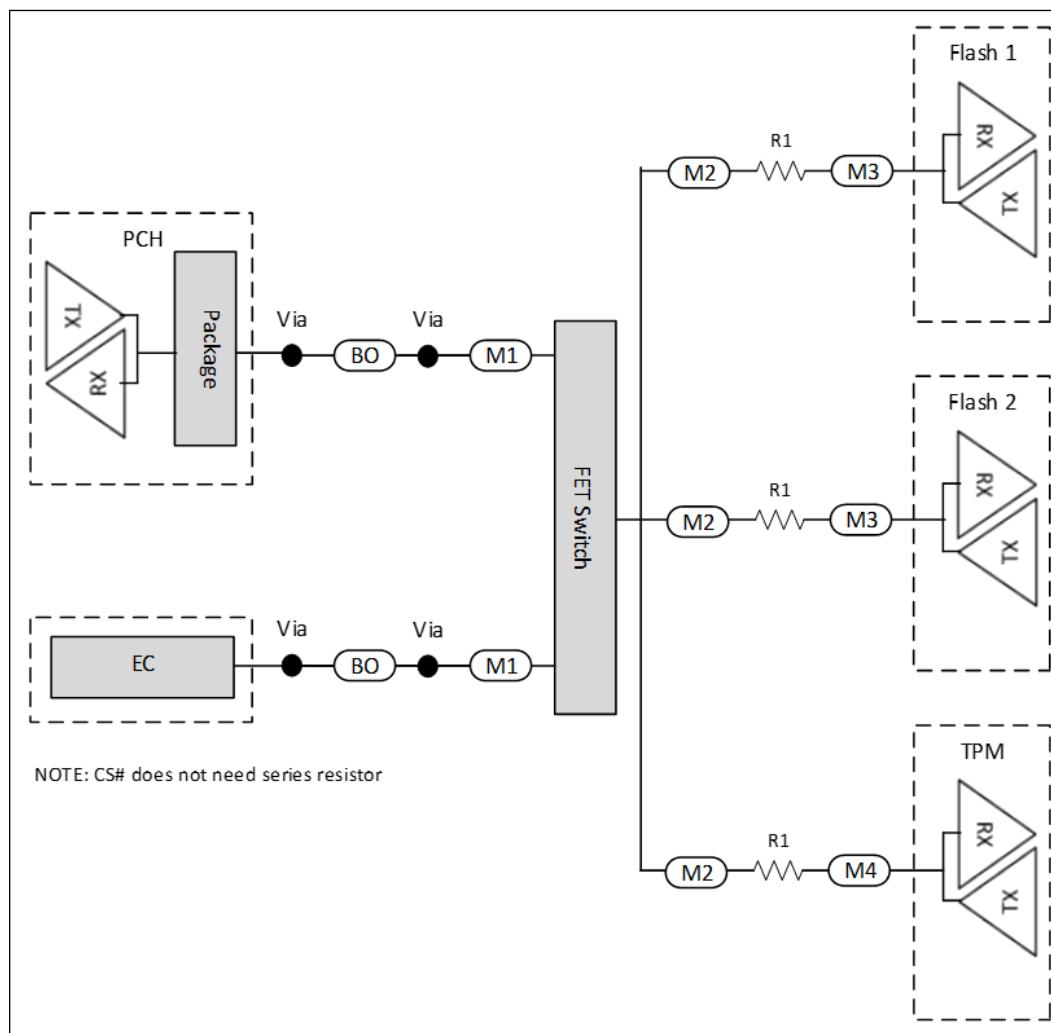
Segment	Tline Type	Max Length (mm)
BO	MS, SL	12.7
M1	DSL, MS, SL	111.8
M2	MS	2.54
M3	MS	50.8

### 6.14.1.1.6 3-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing

Pcb Type: None

Pcb Thickness: None

**Figure 90. SPI0 3-Load Branch with EC Isolation FET Flash Sharing Diagram**



**Table 105. 3-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing Notes**

Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Max Frequency	50MHz
R1	$27\Omega \pm 5\%$ for 1.8V, $33\Omega \pm 5\%$ for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0莫斯I, SPI0_IO2 and SPI0_IO3.
M3	SPI branches of segment M3 need to have length matching of 2.54mm
Minimum length	M1, M3 and M4: 25.4mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V

*continued...*

Note	Detail
	1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Stuffing resistor	If one of devices are unstuff (rework), treat it as point-to-point topology thus place stuffing resistor as close as possible to the branch to avoid long stub length
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
FET component criteria	Ron < 10 ohm, Cin < 5pF
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS[0:1]#, SPI0_CS2#

### Segment Lengths

Max Length Total (mm): 189.7

**Table 106. 3-Load Branch Topology (Device Down) with EC Isolation FET Flash Sharing Routing Guidelines**

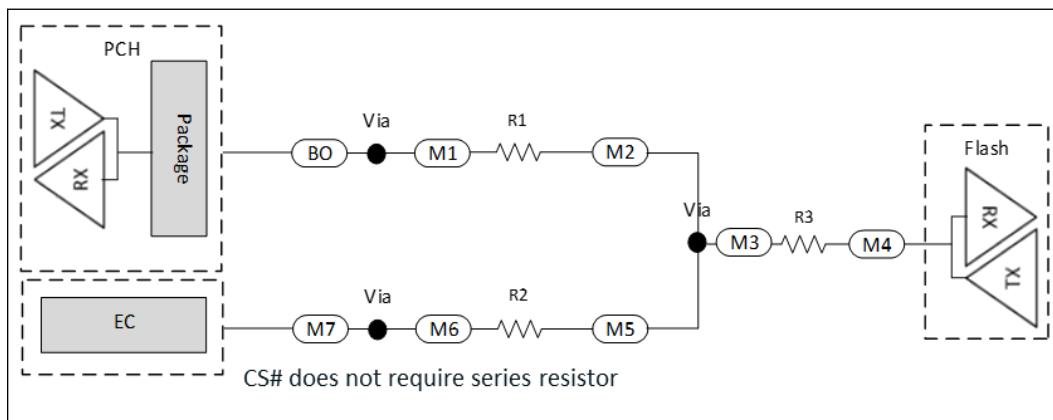
Segment	Tline Type	Max Length (mm)
BO	MS, SL	12.7
M1	DSL, MS, SL	124.46
M2	MS	2.54
M3	MS	38
M4	MS	50

### 6.14.1.1.7 1-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing

Pcb Type: None

Pcb Thickness: None

**Figure 91. SPI0 1-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Diagram**



**Table 107. 1-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Notes**

Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Max Frequency	50MHz
EC and PCH branch requirement	Delta between M1+M2 and M5+M6 shall not exceed 25.4mm (1inch)
R1	0Ω placeholder for 1.8V and 15Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
R2	50Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
R3	33Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3
Minimum length	[1] M1, M3, M4 and M6: 12.7mm [2] M2 and M5: 2.54mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS[0:1]#, SPI0_CS2#

### Segment Lengths

Max Length Total (mm): 177.8

**Table 108. 1-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Routing Guidelines**

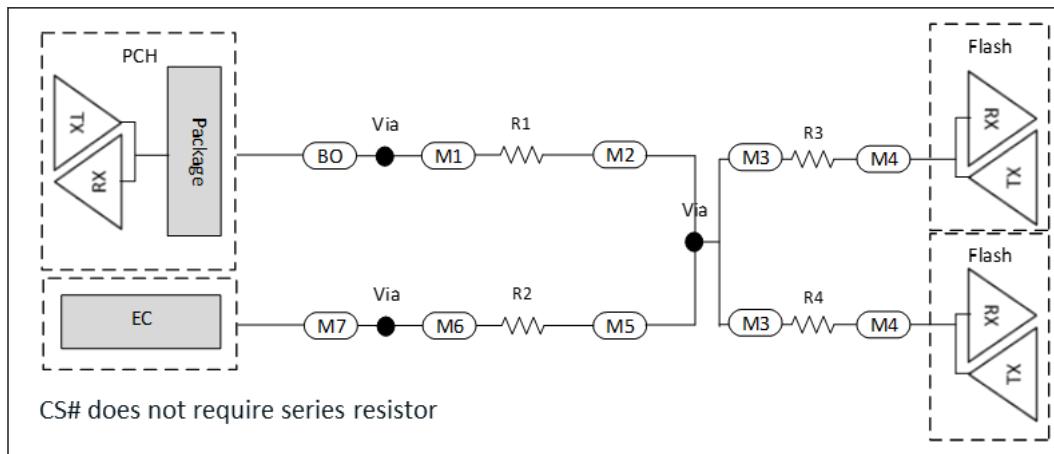
Segment	Tline Type	Max Length (mm)
BO/M7	MS, SL	12.7
M1/M6	DSL, MS, SL	88.9
M2/M5	MS	25.4
M3	MS	25.4
M4	MS	25.4

#### 6.14.1.1.8 2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing

Pcb Type: None

Pcb Thickness: None

**Figure 92. SPI0 2-Load Branch Topology with EC Wired-OR Flash Sharing Diagram**



**Table 109. 2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Notes**

Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Max Frequency	50MHz
EC and PCH branch requirement	Delta between M1+M2 and M5+M6 shall not exceed 25.4mm (1inch)
R1	0Ω placeholder for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0莫斯I, SPI0_IO2 and SPI0_IO3
R2	50Ω for 1.8V and 100Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0莫斯I, SPI0_IO2 and SPI0_IO3
R3	15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0莫斯I, SPI0_IO2 and SPI0_IO3
R4	15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0莫斯I, SPI0_IO2 and SPI0_IO3

*continued...*

Note	Detail
Minimum length	[1] M1, M3, M4 and M6: 12.7mm [2] M2 and M5: 2.54mm
M3 + M4	SPI branches of segment M3+M4 need to have length matching of 2.54mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS[0:1]#, SPI0_CS2#

### Segment Lengths

Max Length Total (mm): 165.1

**Table 110. 2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Routing Guidelines**

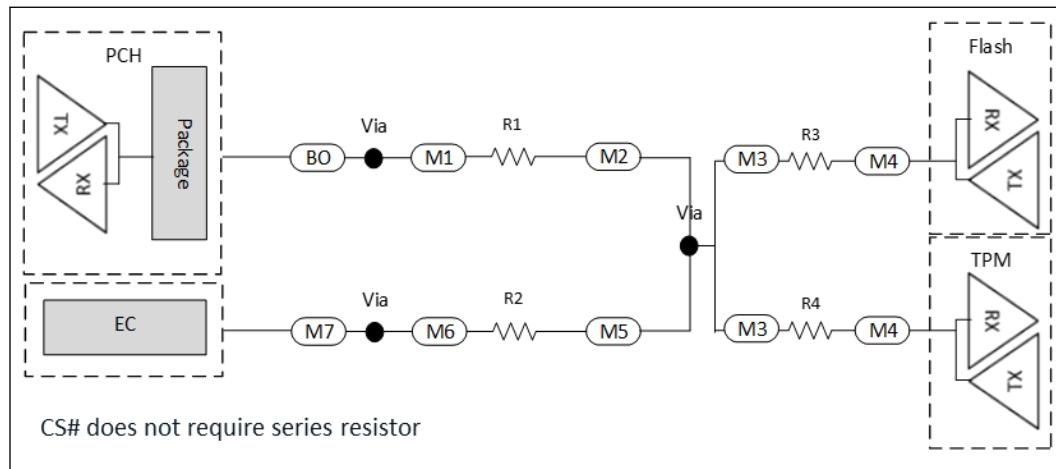
Segment	Tline Type	Max Length (mm)
BO/M7	MS, SL	12.7
M1/M6	DSL, MS, SL	76.2
M2/M5	MS	25.4
M3	MS	25.4
M4	MS	25.4

#### 6.14.1.1.9 2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing and TPM

Pcb Type: None

Pcb Thickness: None

**Figure 93. SPI0 2-Load Branch Topology with EC Wired-OR Flash Sharing and TPM Diagram**



**Table 111. 2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing and TPM Notes**

Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Max Frequency	50MHz
EC and PCH branch requirement	Delta between M1+M2 and M5+M6 shall not exceed 25.4mm (1inch)
R1	0Ω placeholder for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3
R2	[1] 50Ω for 1.8V and 100Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. [2] 50Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0_IO2 and SPI0_IO3. If TPM use this signal, R3 value shall follow MISO and MOSI recommendation.
R3	[1] 15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. [2] 33Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0_IO2 and SPI0_IO3. If TPM use this signal, R3 value shall follow MISO and MOSI recommendation.
R4	15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If TPM use SPI0_IO2 and SPI0_IO3, R4 value shall follow MISO and MOSI recommendation.
Minimum length	[1] M1, M3, M4 and M6: 12.7mm [2] M2 and M5: 2.54mm
M3 + M4	SPI branches of segment M3+M4 need to have length matching of 2.54mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V

*continued...*

Note	Detail
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS[0:1]#, SPI0_CS2#

### Segment Lengths

Max Length Total (mm): 165.1

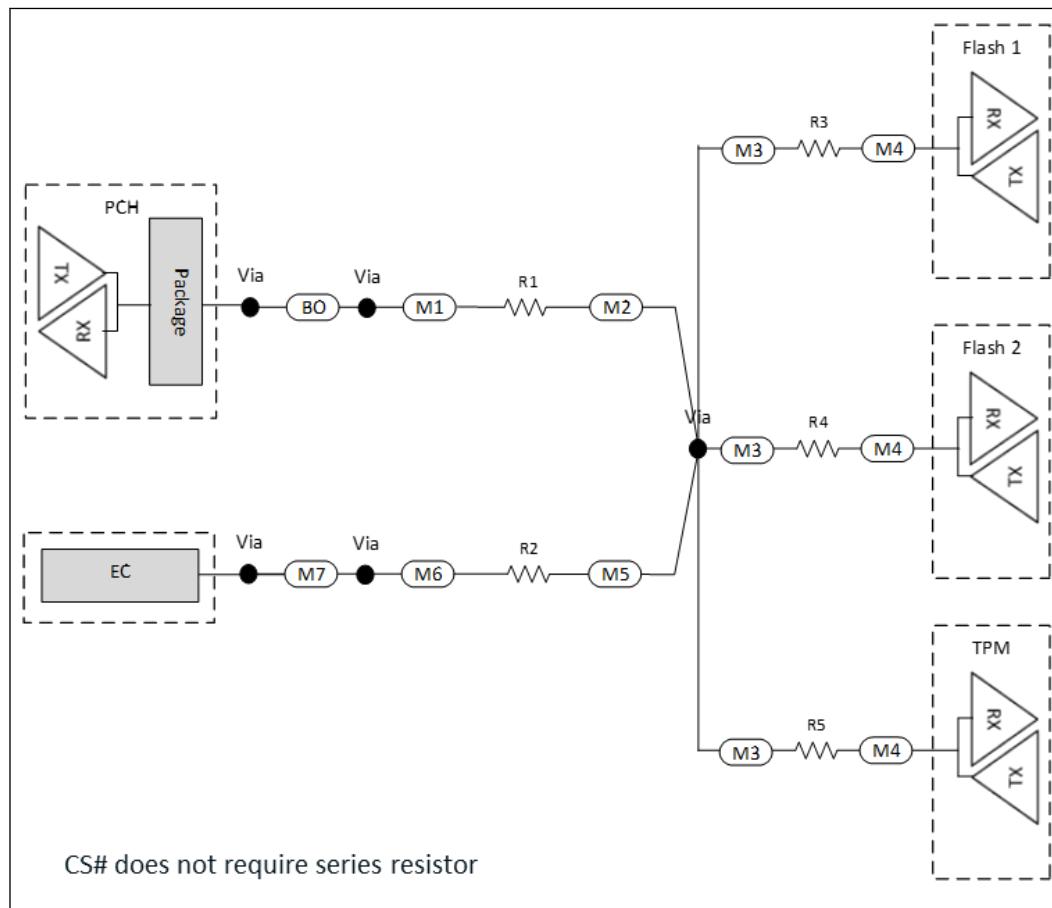
**Table 112. 2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing and TPM Routing Guidelines**

Segment	Tline Type	Max Length (mm)
BO/M7	MS, SL	12.7
M1/M6	DSL, MS, SL	76.2
M2/M5	MS	25.4
M3	MS	25.4
M4	MS	25.4

### 6.14.1.1.10 3-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing

Pcb Type: None

Pcb Thickness: None

**Figure 94. SPI0 3-Load Branch Topology with EC Wired-OR Flash Sharing Diagram****Table 113. 3-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Notes**

Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Max Frequency	50MHz
EC and PCH branch requirement	Delta between M1+M2 and M5+M6 shall not exceed 25.4mm (1inch)
M1/M6	It can be extended up to 76.2mm for 1.8V ONLY
R1	0Ω placeholder for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
R2	[1] 15Ω for 1.8V and 100Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. [2] 50Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0_IO2 and SPI0_IO3. If TPM use this signal, R2 value shall follow MISO and MOSI recommendation.
R3	15Ω for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.

*continued...*

Note	Detail
R4	15Ω for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
R5	15Ω for 1.8V and 3.3V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If TPM use SPI0_IO2 and SPI0_IO3, R5 value shall follow MISO and MOSI recommendation.
Minimum length	[1] M1, M3, M4 and M6: 12.7mm [2] M2 and M5: 2.54mm
M3 + M4	SPI branches of segment M3+M4 need to have length matching of 2.54mm
Device AC Timing Characteristics	Data Input Setup time < 2ns for 1.8V and 3.3V Data Input Hold time < 3ns for 1.8V and 3.3V 1.5ns < Clock to Data output valid time < 7.5ns for 1.8V 1.5ns < Clock to Data output valid time < 7ns for 3.3V
Length matching between CLK and DATA/CS# signals	12.7mm
Trace spacing between DATA and DATA signals	0.250mm
Trace spacing between CLK and DATA/Other signals	0.375mm
Signal Name/List	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO3, SPI0_IO2, SPI0_CS[0:1]#, SPI0_CS2#

### Segment Lengths

Max Length Total (mm): 139.7

**Table 114. 3-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Routing Guidelines**

Segment	Tline Type	Max Length (mm)
BO/M7	MS, SL	12.7
M1/M6	DSL, MS, SL	63.5
M2/M5	MS	12.7
M3	MS	25.4
M4	MS	25.4

## 6.15

### Touch Host Controller (THC) Design Guidelines

The Touch Host Controller uses standard SPI interface for PCH to connect external touch devices. Two touch ports/devices can be interfaced with THC. THC also supports the GPIO based SPI interrupt from touch IC's.

The SPI bus protocols used for the touch operation are the same as the existing SPI touch interface.

---

#### NOTE

THC Touch is only applicable for Mobile PCH Sku's.

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### 6.15.1 THC Touch Signal Descriptions

Signal Name Group Description	Signal Name Group Description	Signal Name Group Description
GPP_E11 / <b>THC0_SPI1_CLK</b>	Clock	THC0 SPI1 Clock output from PCH
GPP_E13 / <b>THC0_SPI1_IO0</b>	Data	THC0 SPI1 serial output data from PCH to the Touch Screen device. This Pin will also function as Input during Dual and Quad I/O operation
GPP_E12 / <b>THC0_SPI1_IO1</b>	Data	THC0 SPI1 serial input data from the Touch Screen device to PCH. This Pin will also function as Output during Dual and Quad I/O operation
GPP_E1 / <b>THC0_SPI1_IO2</b>	Data	THC0 SPI1 I/O to comprehend the support for the Quad I/O operation
GPP_E2 / <b>THC0_SPI1_IO3</b>	Data	THC0 SPI1 I/O to comprehend the support for the Quad I/O operation
GPP_E10 / <b>THC0_SPI1_CS#</b>	Chip Select	THC0 SPI1 chip select
GPP_E6 / <b>THC0_SPI1_RST#</b>	Reset	THC0 SPI1 reset
GPP_E17 / <b>THC0_SPI1_INT#</b>	Interrupt	THC0 SPI1 interrupt
GPP_F11 / <b>THC1_SPI2_CLK</b>	Clock	THC1 SPI2 Clock output from PCH
GPP_F12 / GSXDOOUT / <b>THC1_SPI2_IO0</b>	Data	THC1 SPI2 serial output data from PCH to the Touch Screen device. This Pin will also function as Input during Dual and Quad I/O operation
GPP_F13 / GSXSLOAD / <b>THC1_SPI2_IO1</b>	Data	THC1 SPI2 serial input data from the Touch Screen device to PCH. This Pin will also function as Output during Dual and Quad I/O operation
GPP_F14 / GSXDIN / <b>THC1_SPI2_IO2</b>	Data	THC1 SPI2 I/O to comprehend the support for the Quad I/O operation
GPP_F15 / GSXSRESET# / <b>THC1_SPI2_IO3</b>	Data	THC1 SPI2 I/O to comprehend the support for the Quad I/O operation
GPP_F16 / GSXCLK / <b>THC1_SPI2_CS#</b>	Chip Select	THC1 SPI2 chip select
GPP_F17 / <b>THC1_SPI2_RST#</b>	Reset	THC1 SPI2 reset
GPP_F18 / <b>THC1_SPI2_INT#</b>	Interrupt	THC1 SPI2 interrupt

### 6.15.2 THC Touch Guidelines

Touch device must be directly connected to the THC SPI bus. Also, refer to the Serial Touch device vendor documentation for additional Serial Touch specific design considerations.

## 6.16 I<sup>2</sup>C Interface Design Guidelines

PCH includes six I<sup>2</sup>C controllers, providing six independent I<sup>2</sup>C interfaces. Each interface is a two-wire I<sup>2</sup>C serial interface consisting of a serial data line and a serial clock.

Each I<sup>2</sup>C interface supports standard mode (up to 100 Kb/s), fast mode (up to 400 Kb/s), fast mode plus (up to 1 Mb/s) and High speed mode (up to 3.2 Mb/s). Devices supporting standard mode and/or fast mode cannot be connected to the same I<sup>2</sup>C bus where devices supporting fast mode plus and/or High speed mode are connected.

The I<sup>2</sup>C interface can support 1.8 V or 3.3 V depending on devices connected to it.

I<sup>2</sup>C bus from PCH is recommended to connect SMBus of USB/DP Re-Timer for USB Type-C interface. When Burnside bridge Re-timer (BBR) is only used for USB/DP mode on any system, LSX interface cannot be used for Re-Timer SPI Flash image update, in this case I<sup>2</sup>C bus from PCH is required to connect to BBR Re-Timer SMBus for updating the Re-Timer SPI flash image. Refer [USB-C\\* Sub-System](#) on page 81

## 6.16.1 I<sup>2</sup>C Platform Specific Important Information

**Table 115. Reference Specifications**

Title
I <sup>2</sup> C Specification Version 5

## 6.16.2 I<sup>2</sup>C Signal Descriptions

### Signal Groups

**Table 116. I<sup>2</sup>C\* Signals**

Group	Signal Name	Description
Clock	I <sup>2</sup> C[5:0]_SCL	I <sup>2</sup> C clock signals
Data	I <sup>2</sup> C[5:0]_SDA	I <sup>2</sup> C data signals
Clock	I <sup>2</sup> C4B_SCL	I <sup>2</sup> C clock signals
Data	I <sup>2</sup> C4B_SDA	I <sup>2</sup> C data signals

## 6.16.3 I<sup>2</sup>C Guidelines

### General Design Considerations

I<sup>2</sup>C bus is a multi-device bus (i.e. more than one device can be connected to an I<sup>2</sup>C bus). The total number of devices connected to the bus is determined by the total capacitive load on the bus. The maximum bus capacitive load for each I<sup>2</sup>C bus is 400pF and cannot be exceeded.

I<sup>2</sup>C clock and data signals require pull-up resistors. There is an internal pull-down resistor, and current assist which can be selected through register based on the bus capacitive load including devices leakage currents (refer 572795 for details).

Do not mix and match devices supporting 100 kHz / 400 kHz speed with the one supporting 1 MHz/3.2 MHz on the same I<sup>2</sup>C bus.

I<sup>2</sup>C signals are multiplexed with GPIOs and default to GPIO functionality (as input). If I<sup>2</sup>C interfaces are not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

### Detailed Routing Requirements

System designers must consider the total bus capacitance which includes both package and device pin capacitance and board trace length capacitance when designing I<sup>2</sup>C bus. The total bus capacitance must not exceed 100pF for High Speed Mode and 400pF for other modes (Standard/Fast/Fast mode plus).

**Table 117. Bus Capacitance Reference Chart**

Device	Capacitance Includes	Units	Capacitance
PCH Pin Capacitance	Pin Capacitance	pF	8 to 10
Device Pin Capacitance	Pin Capacitance	pF	5 to 10
Board Trace per Inch	per inch of trace length	pF	2 to 5

Trace Capacitance per inch is approximately equal to  $85\sqrt{\epsilon_r} / Z_0$  (in pF) where,  $\epsilon_r$  is Dielectric constant of material,  $Z_0$  is Trace impedance

#### NOTE

Multiple options for Pull-up/pull-down and current assist strengths are provided for a particular total bus capacitance. Choose the optimal value for system based on design considerations like power, BOM and cost.

### 6.16.4 Tools

Intel does not promote any specific tool for this interface.

## 6.17 SMBus 2.0/SMLink Interface Design Guidelines

### 6.17.1 SMBus 2.0/SMLink Platform Specific Important Information

#### SMBus Description

PCH integrates an SMBus 2.0 controller. The SMBus provides an interface to manage peripherals such as Serial Presence Detection (SPD) on RAM, thermal sensors, PCI cards, etc. The slave interface allows an external micro controller to access system resources.

The SMBus interface on PCH uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used by the SMBus Host, SMBus Slave, and TCO Controllers. These controllers reside inside PCH.

#### SMLink Description

PCH incorporates two SMLink interfaces, SMLink0 and SMLink1. SMLink0 is used for Re-timer configuration for USB Type-C interface and between PCH's LAN controller and the PHY. SMLink1 is used for various PD Controllers.

SMBus and SMLink connectivity recommendations are described in [Figure 95](#) on page 189 and [Figure 98](#) on page 190 below.

---

**NOTE**

The requirement to tie both SMLink and SMBus signals externally is not needed, as slave functionality is available on the SMBus pins.

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## 6.17.2 SMBus 2.0/SMLink Signal Descriptions

### Signal Groups

**Table 118. SMBus and SMLink Signals**

Group	Signal Names	Description
Clock	SMBCLK SML[1:0]CLK	SMBus/SM Link Clock signals
Data	SMBDATA SML[1:0]DATA	SMBus/SMLink Data lines
ALERT	SMBALERT# SML[1:0]ALERT# PMCALERT#	SMBus/SMLink ALERT signals /SMLink ALERT signals USB Type-C PD controller / Re-timer Alert.

## 6.17.3 SMBus 2.0/SMLink Guidelines

### General Design Considerations

- The maximum bus capacitance is 400 pF.
- It is recommended that I<sup>2</sup>C devices (used on SMBus in I<sup>2</sup>C enabled mode) be powered by the core power supply. During an SMBus transaction in which the device is sending information to PCH, the device may not release the SMBus if PCH receives an asynchronous reset. Core well power is used to allow BIOS to reset the device if necessary. SMBus 2.0-compliant devices have a timeout capability which makes them **insusceptible** to this I<sup>2</sup>C issue, allowing flexibility in choosing a voltage supply. **not likely to be affected.**
- If SMBus is connected to PCI, it must be connected to all PCI slots.
- If SMBus is connected to PCI Express\*, it must be connected to all PCI Express slots.

**Note 2:** Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of TTIMEOUT,MIN. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than TTIMEOUT,MAX. Typical device examples include the host controller, and embedded controller and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition.

A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for TTIMEOUT,MAX or longer.

## 6.17.4 Detailed Routing Requirements

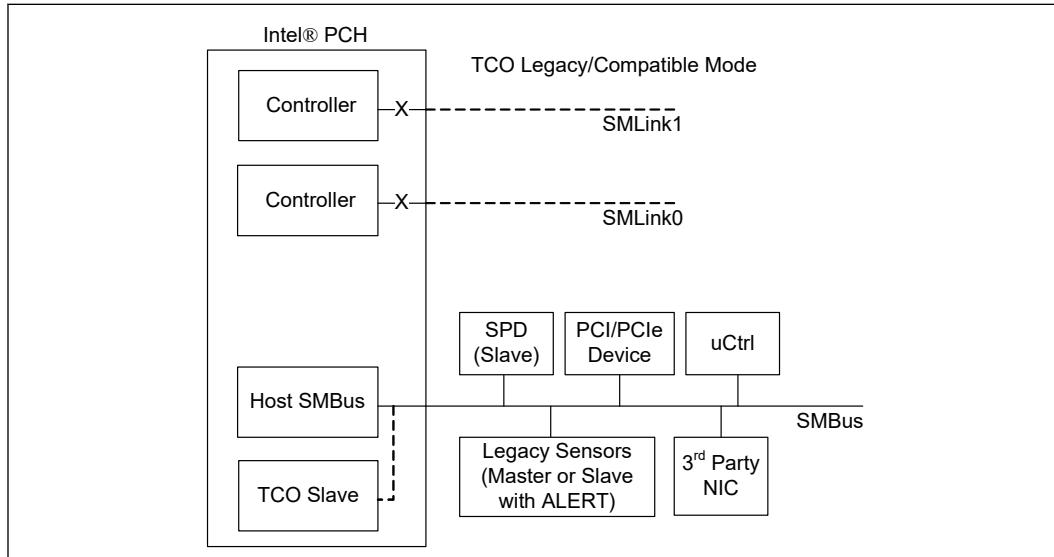
Since SMBus and SMLink trace length is dependent on total capacitance of the system bus, designer needs to take into consideration the number and types of SMBus devices/slots on the motherboards.

External pull up is required which is also based on the load capacitance and bus speed.

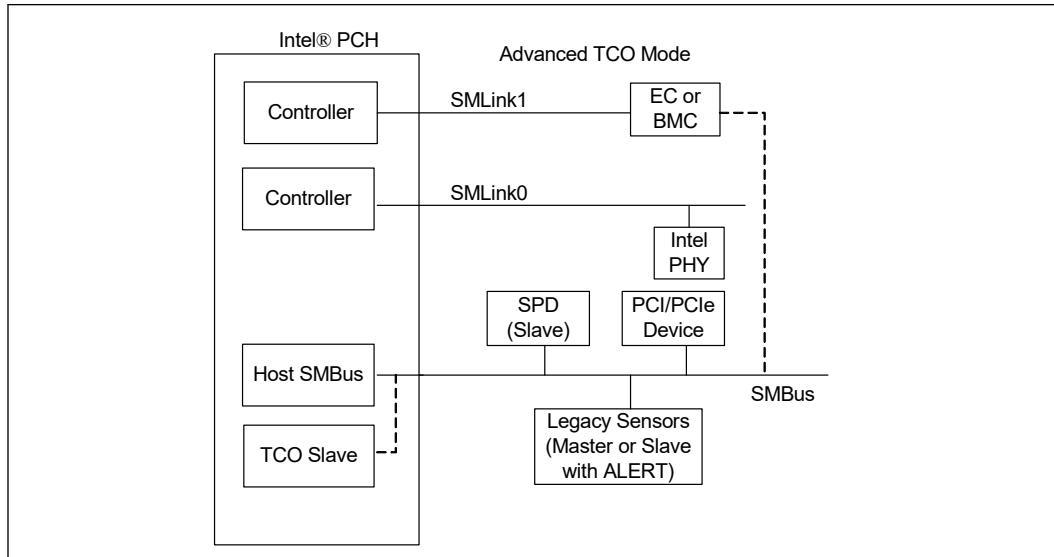
Designer needs to calculate the total capacitance for trace routing and the pins of each device connected on the bus.

## 6.17.5 SMBus and SMLink Connectivity Recommendation

**Figure 95.** SMBus / SMLink (TCO Legacy Mode)



**Figure 96.** SMBus / SMLink Connectivity (Advanced TCO Mode)



## BMC

**Baseboard management controller** [edit]

See also: [Out-of-band management § Implementation](#)

The baseboard management controller (BMC) provides the intelligence in the IPMI architecture. It is a specialized microcontroller embedded on the motherboard of a computer – generally a server. The BMC manages the interface between system-management software and platform hardware. BMC has its own firmware and RAM.

Different types of sensors built into the computer system report to the BMC on parameters such as temperature, cooling fan speeds, power status, operating system (OS) status, etc. The BMC monitors the sensors and can send alerts to a system administrator via the network if any of the parameters do not stay within pre-set limits, indicating a potential failure of the system. The administrator can also remotely communicate with the BMC to take some corrective actions – such as resetting or power cycling the system to get a hung OS running again. These abilities reduce the total cost of ownership of a system.

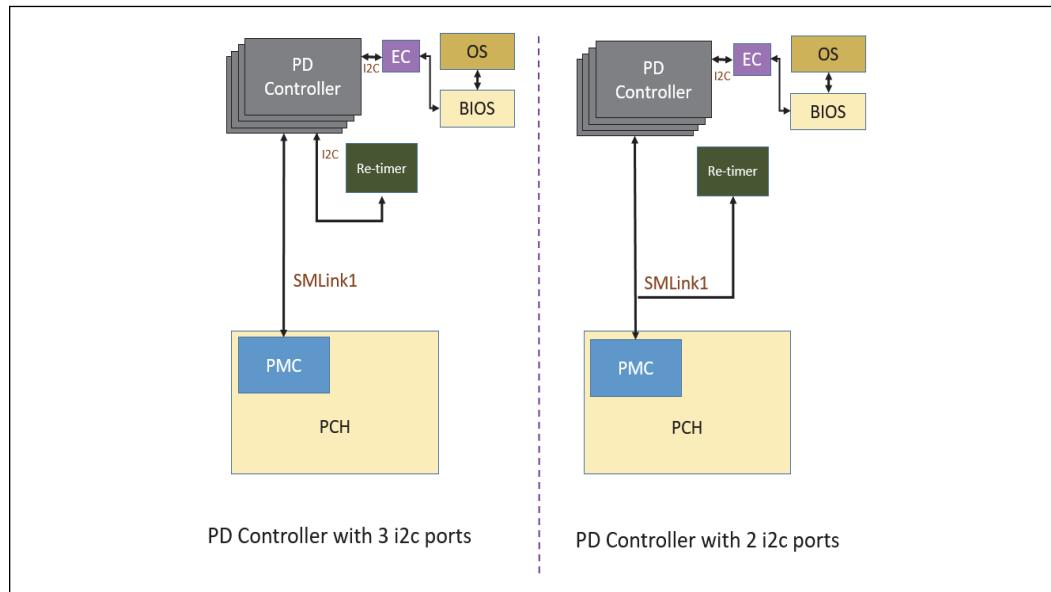
Systems compliant with IPMI version 2.0 can also communicate via serial over LAN, whereby serial console output can be remotely viewed over the LAN. Systems implementing IPMI 2.0 typically also include KVM over IP, remote virtual media and out-of-band embedded web-server interface functionality, although strictly speaking, these lie outside of the scope of the IPMI interface standard.

Physical interfaces to the BMC include SMBuses, an RS-232 serial console, address and data lines and an Intelligent Platform Management Bus (IPMB), that enables the BMC to accept IPMI request messages from other management controllers in the system.

A direct serial connection to the BMC is not encrypted as the connection itself is secure. Connection to the BMC over LAN may or may not use encryption depending on the security concerns of the user.

There are rising concerns about general security regarding BMCs as a closed infrastructure.<sup>[5][6][7][8]</sup> OpenBMC is a Linux Foundation Collaborative open-source BMC project.<sup>[9]</sup>

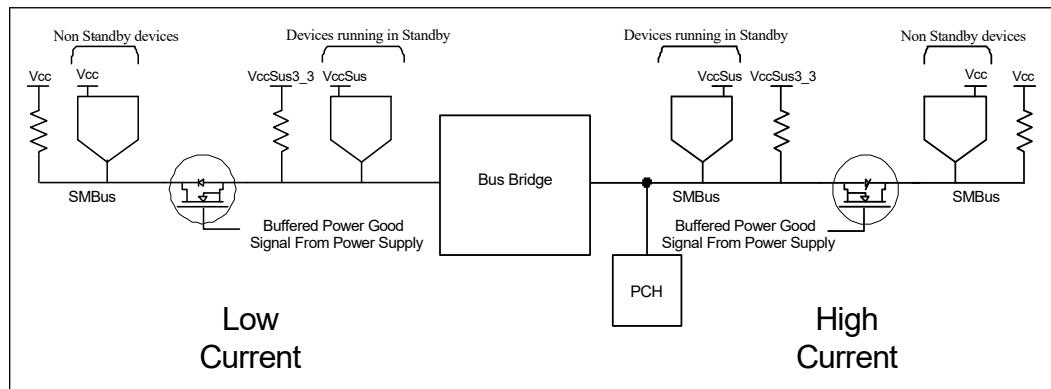
**Figure 97. SMBus / SMLink Connectivity for USB Type-C PD Controller**



### High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices. Suspend power well leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of a "FET" to isolate the devices powered by the core and suspend supplies. Refer Figure below:

**Figure 98. High Power/Low Power Mixed Vcc\_SUSPEND / Vcc\_CORE\_ Architecture**



#### Added Considerations for Mixed Architecture:

- The bus bridge must be powered by suspend power well.
- Devices that are powered by the suspend power well must not drive into other devices that are powered off. This is accomplished with the "bus switch".
- The bus bridge can be a device like the Philips\* PCA9515.

## 6.17.6 Additional Guidelines - SMBus 2.0/SMLink Interface Design Guidelines

### SMBus Design Considerations

No single SMBus design solution will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add a significant amount of capacitance to the bus. This extra capacitance has a large effect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Device class (High/Low power). Most designs use primarily High Power Devices.
- Amount of suspend well current available, i.e., minimizing load of suspend power wells.

### Intel® Trace Hub Backup: SMBus Test Points

Background: Intel Trace Hub is a new concept/mechanism, used to transport messages from the SoC to external monitor through a USB connector. This concept is defined as “Closed Chassis” message transport, without the need to open the chassis.

The Intel® ME is one of the entities using the Intel Trace Hub to provide debug data to the external monitor. However, since the Intel Trace Hub is a new technology, the following design guidelines act as a **backup** solution to route the debug information to an external SMBus Sniffer. **It is highly recommended that the SMBus Test Points are implemented**, so the customer or Intel debug team will be able to collect debug data from the system.

To quickly attach the SMBus sniffer to the platform, the following items should be added:

- Clearly marked (Silk-screen) SMBus test points, preferably, holes for 0.1" header (3 pins: SMBDATA, SMBCLK and GND), connected directly to the SoC SMBus pins.

---

#### NOTE

These Test points will be used to hook up to a SMBus sniffer that will impose an additional 60 pF load capacitance. The value of the SMBus internal pull up resistor should be calculated with this additional 60 pF load to ensure that the sniffer and the SMBus will continue to operate normally when the sniffer is plugged in. If the total SMBus section capacitance is equal to or less than 400 pF after adding this 60 pF, no other change is required. In case the final SMBus section capacitance is larger than 400 pF, the SMBus will need a bridge to separate the bus into 2 sections with <400 pF capacitance each.

- Accessing the Test Points to hook the sniffer should be simple. It is recommended that the SMBus Test points be easily accessed when lifting the keyboard, or within the SSD or DDR compartments, or by removing existing battery, wireless or other available easy access panels on the chassis.

## 6.17.7 Compliance Requirements - SMBus 2.0/SMLink Interface Design Guidelines

**Table 119. Compliance Documents**

Title	Location
System Management Bus (SMBus) Specification, version 2	<a href="http://smbus.org/specs">http://smbus.org/specs</a>

## 6.17.8 Tools

Intel does not promote any specific tool for this interface.

## 6.18 Controller Link

Controller Link interface is the management communication link between the PCH and Intel Wireless cards. Correct operation of this bus is required for wireless network communication and wake up events.

It is designed for either an internal Controller Link connection (for CNVi) or an external bus, as described in the rest of this section (also called “discrete connectivity”). The selection between these two configurations does not require any hardware changes at the board level. The Intel® CSME configure its own Controller Link multiplexer as to select the Controller Link configuration (internal/external). This feature allows another level of automation by allowing the Intel® CSME controller to read a SoC/PCH internal bit, indicating if CNVi or discrete is currently connected.

For implementing the discrete connectivity, refer to “Tiger Lake Platform Controller Hub (PCH-UP4/UP3) - External Design Specification (EDS) - Volume 1 of 2 (#576591)” for full Controller Link details.

**Table 120. Intel® CSME Controller Link Signals and Signal-Integrity Design Guidelines**

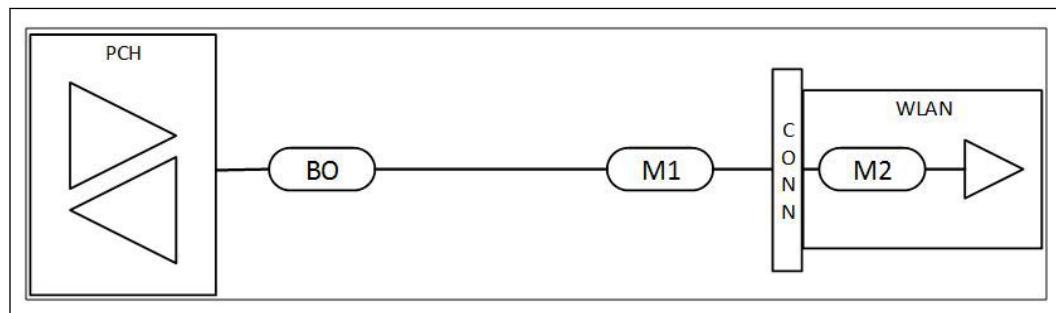
Group	Signal Name	Description
Clock	CL_CLK	Controller Link Clock: Bi-directional clock that connects to a Wireless LAN Device supporting Intel® Active Management Technology.
Data	CL_DATA	Controller Link Data: Bi-directional data that connects to a Wireless LAN Device supporting Intel® Active Management Technology.
Reset	CL_RST#	Controller Link Reset: Controller Link reset that connects to a Wireless LAN Device supporting Intel® Active Management Technology.

## 6.18.1 CLINK

### 6.18.1.1 CLINK 1-Load Topology (Add-In Card)

Pcb Type: None

Pcb Thickness: None

**Figure 99. CLINK 1-Load (Add-In Card) Topology Diagram****Table 121. CLINK 1-Load Topology (Add-In Card) Notes**

Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Length matching between Clock and Data signals	25.4mm
Trace spacing between DATA and DATA signals	0.125mm
Trace spacing between CLK and DATA/Other signals	N/A
Max CL_RST# length	228mm
Signal Name/List	CL_DATA, CL_CLK, CL_RST#

### Segment Lengths

Max Length Total (mm): 291.7

**Table 122. CLINK 1-Load Topology (Add-In Card) Routing Guidelines**

Segment	Tline Type	Max Length (mm)
BO	DSL, MS, SL	12.7
M1	DSL, MS, SL	241
M2	DSL, MS, SL	38

## 6.19 Universal Asynchronous Receiver Transmitter (UART) and LSx Interface Design Guidelines

### 6.19.1 UART Interface

The platform integrates three Universal Asynchronous Receiver Transmitter (UART) controllers. Each supports up to 3.8 Mbit/s. The controllers can be used in the low-speed, full-speed, and high-speed modes. The controllers are based on the 16550 industry standard and communicates with serial data ports that conform to the RS-232 interface protocol.

For information on what OS the UART interface supports, refer to the Intel® Serial I/O Driver PRD documentation.

---

**NOTE**

1. Bluetooth\* devices are not supported on the PCH UART interfaces.

---

2. The pull up resistor requirement is device dependent and not mandatory

## 6.19.2 UART Signal Descriptions

**Table 123. UART Signals**

Group	Signal Name	Description
Data	UART[2:0]_RXD	Receive Data Input signals
	UART[2:0]_TXD	Transmit Data Output signals
Control	UART[2:0]_RTS#	Request to Send signals
	UART[2:0]_CTS#	Clear to Send signals

## 6.19.3 LSx Interface

The PCH LSx interface enables communication between one thunderbolt controller to another. TGL UP3/UP4 supports 4 pairs of LSx signals. The LSx signals use a UART interface. It operates at a 1 MHz baud rate and shares identical electrical characteristics/routing guidelines as UART.

## 6.19.4 LSx Signal Description

**Table 124. LSx Signals**

Group	Signal Name	Description
Data	TBT_LSX[0:3]_RXD	Receive Data Input signals
	TBT_LSX[0:3]_TXD	Transmit Data Output signals

## 6.19.5 Tools

Intel does not promote any specific tool for this interface.

## 6.20 General Purpose I/Os Design Guidelines

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**NOTES**

- For unused GPIO defaulting to GPIO function, there's no termination required.
  - For unused GPIO defaulting to a Native function:
    - Termination may be required depending on the native function operation/requirement or buffer types (e.g. input). This should have been covered in individual native interface. OR
    - The pin can be programmed to GPIO function (if acceptable) and no termination is needed.
-

## 6.21 PCH Signal Glitch Free Implementation Requirements

Certain PCH signals require special board implementation to ensure glitch free operation during boot process. Failure to meet the requirements may cause the signals to glitch during power sequencing and negatively impact the PCH behavior as well as external devices.

### 6.21.1 Implementation Details

Different options (implementing pull-up/pull-down resistors or capacitors) are provided to meet the requirements. The options are intended for board implementation flexibility. For some signals, a cap or resistor site is recommended for board prototype designs and the site can be removed later on if not needed.

For the cap implementation option, the cap value depends on the 3.3V ramp rate of the VR on the motherboard, regardless of the signals being in 3.3V or 1.8V signaling mode.

For the resistor option, the resistor value depends on the signaling mode of the signal (3.3V or 1.8V).

The signal details will be updated in the next revision.

**Table 125. Signals Required Cap or Pull-Down Resistor**

Signal Name	Option 1 (Cap Implementation)		Option 2 (Pull-down Resistor Implementation)		Note
	3.3v Ramp Rate from 5-50ms	3.3V Ramp Rate Less than 5ms	3.3V Signaling Mode	1.8V Signaling Mode	
GPD4 / SLP_S3# GPD5 / SLP_S4# GPD6 / SLP_A# GPD9 / SLP_WLAN#	330 nF	33 nF	100 K	N/A	Cap or pull-down resistor is required
SLP_SUS# SLP_LAN#	330 nF	33 nF	100 K	N/A	
SPI0_CLK GPP_H18 / PROC_C10_GATE#	N/A	N/A	100K	75K	Pull-down resistor is required.
eDP_BKLTEM eDP_VDDEN	330 nF	33 nF	100K	75K	Cap or pull-down resistor is required depending on panel power sequencing spec or power delivery
CNV_RF_RESET#	N/A	N/A	N/A	75K	Pull-down resistor to ensure the stability of the signal during platform bootup

**Table 126. Signals Recommended with Cap or Pull-down Resistor Sites**

Signal Name	Option 1 (Cap Implementation)	Option 2 (Pull-down Resistor Implementation)	Notes
GPD_10 / SLP_S5# GPP_A10 / ESPI_RESET	Cap site	Pull-down resistor site	Site for cap or pull-down resistor only.
GPP_B13 / PLTRST# GPP_R0 / HDA_BCLK / I2S0_SCLK / DMIC_CLK_B0 / HDAPROC_BCLK GPP_R4 / HDA_RST# / I2S2_SCLK / DMIC_CLK_A0 GPP_R5 / HDA_SDII / I2S2_SFRM / DMIC_DATA0	N/A	Pull-down resistor site	Site for pull-down resistor only.

**Table 127. Signals Required Pull-up Resistor**

Signal Name	Pull-Up Resistor Value		Note
	3.3V Signaling Mode	1.8V Signaling Mode	
GPP_B12 / SLP_S0#	100K	75K	Pull-up resistor is required on GPP_B12 / SLP_S0# if a device is monitoring SLP_S0# before RSMRST# de-assertion
GPP_F20 / EXT_PWR_GATE#	100K	75K	
GPP_F21 / EXT_PWR_GATE2#	100K	75K	

## 6.22 CNVio Bus

The CNVio signals connects between the CRF RF companion module and the SoC. For details, refer to Wireless Connectivity Integration (CNVi) Design

They are used as the main data bus for Wi-Fi\* to transfer data between the PCH (Pulsar/Quasar) and the RF companion chip. The CNVio signals electrical characteristics are similar to the DPHY standard. The CNVio protocol used for this bus is proprietary.

This product uses the latest Gen2.0 of the CNVio (supporting higher rates) that is also backward compatible to work with Gen 1 used in JfP.

CNVio signal specifications are documented in the CNVio standard specification (based on MIPI-DPHY refer MIPI-DPHY standard version 2.0 Revision 0.5: Chapter 8 - Interconnect and Lane Configuration)

The CNVio bus is source synchronous where each lane has data carried over a differential pair, and each direction may have multiple lanes and a single clock driven by the source.

The CNVio Gen 2, has 2 lanes in each direction, which supports the following bit rates: (per lane).

- 2.5GBit/Sec Rate with 1250MHz clock rate in Gen 2 Mode
- When working with JfP Gen 1 (based module) the clock rate is ~660MHz

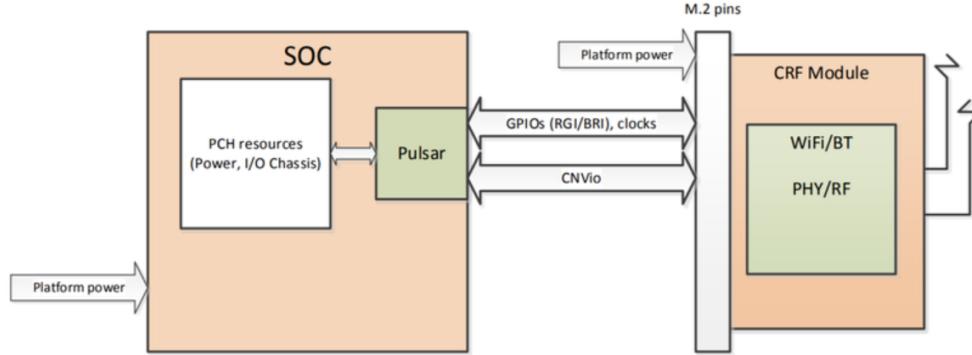
Refer MIPI alliance Draft Specification for D-PHY v2.0\_r0.5 July 5th 2019

Integrated Connectivity (CNVi) is an architecture for wireless connectivity devices designed by Intel for their processors. CNVi was introduced in 2017 with the launch of [Gemini Lake](#) and is also planned for future mobile chipsets starting with [Cannon Lake](#).

## Overview [edit]

CNVi is an architecture for wireless connectivity designed by Intel for their recent mobile devices. Under the CNVi architecture, the large (and typically expensive) functional blocks found on a typical radio chip are moved onto the processor or chipset itself. This includes the processor and associated logic, memory, and the **MAC** components of the Bluetooth and Wi-Fi cores. The remaining parts (i.e., signal processor, analog and RF functions) are left on the Companion RF (CRF) module. This ultimately reduces the **bill of material** size and cost of the product.

The connectivity functionality that was moved to the SoC is incorporated in a block called a **Pulsar**. Pulsar interfaces with the rest of SoC through its internal interfaces and buses. Pulsar interfaces with the CRF module via the CNVi interface.



## 6.22.1 Routing Guidelines for CNVio

The CNVio signals connects between the RF companion module and the SoC. They are used as the main data bus for Wi-Fi to transfer data between the Pulsar/Quasar IP and the RF companion chip. The CNVio signals are physically compliant to MIPI-DPHY standard, but have a different (and Intel® proprietary) protocol.

We recommend that the design be fully comply with the MIPI-DPHY Ver 2.0 Rev 0.5 routing signal requirements. These requirements are well documented in the MIPI-DPHY standard specification (for electrical refer chapter 8 and 9 of the MIPI-DPHY Ver 2.0 Rev 0.5 standard: Interconnect and Lane Configuration)

The CNVio bus is source synchronous where each lane has data carried over a differential pair, and each direction may have multiple lanes and a single clock driven by the source.

The 2 traces of each lane must be routed as matched as possible. Moreover, since the CNVio uses one clock signal for 2 lanes in each direction, there should also be a good delay matching between the two data lanes and the clock. There are no special delay matching requirements between lanes on opposite directions.

**Table 128. CNVio Recommended Routing Parameters**

Parameter	Value	Comment
Characteristic impedance	85 ohm +/- 10% differential	This is a relaxation vs MIPI-DPHY Spec that requires 100 ohm
Maximum length	254 mm	228.6 mm from M.2 connector pins to SoC pins
Maximum resistance	50 ohm	50 ohm to ground for each trace
Shielding	Stripline	Recommended for minimizing EMI/RFI
Delay matching between pairs of the same direction	Better than 2mm	Including the 2 lanes and the clock in every direction
Vias	Avoid	Recommended to avoid Via connections as much as possible
BER	1E-12	Standard PHY bit error rate for a CNVio lane

### 6.22.1.1 CNViO

**Table 129. CNViO General Guidelines**

Note	Detail
Length Matching between P and N within a diff. pair	Within same layer mismatch: 0.254mm Total length mismatch: 0.381mm
Length matching between Data and CLK lane	< 1.27mm
CNV_RCOMP sideband/Comp	(1) 150 ohm +/- 1 % RCOMP on motherboard. The RCOMP signals should be referenced to VSS. (2) Noisy or switching references should be avoided. As board space allows, it is recommended to add a VSS shield (3) RCOMP Rdc on motherboard is < 0.5ohm. (4) Isolation of 88um at breakout and 200um at main route (currently to low-speed I/O) required

*continued...*

Note	Detail
Single-ended equivalent impedance of differential channel	For a differential channel transmission line impedance of 80 - 85Ω, the equivalent required single-ended transmission line impedance should be 45 - 50Ω
Reference plane	(1) Continuous GND is recommended. (2) If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed ( $di/dt$ ). (3) If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed ( $di/dt$ ), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
Voiding recommendation for mainstream stackup	It is recommended to void pads for all components for example AC Caps as well as connector pads to optimize the impedance matching in the channel.
Voiding recommendation for thin stackup	It is recommended to void pads for all components for example AC Caps as well as connector pads to optimize the impedance matching in the channel.
Discrete component part size for mainstream stackup	Recommended to use 0402 or smaller component sizes.
Discrete component part size for thin stackup	Required to use 0201
Max Via Stub Length	< 900 um

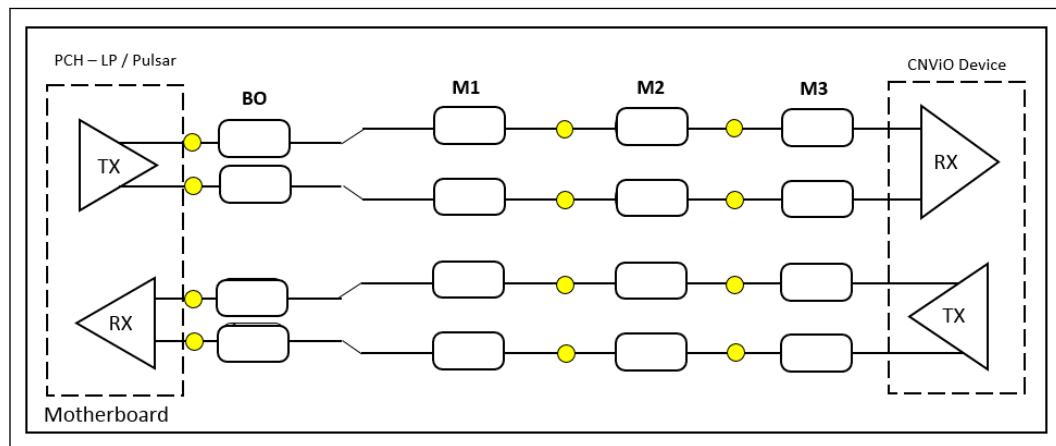
**Table 130. Length Matching**

Matching Group Id	Matching Groups	Required	Maximum Mismatch (mm)
1	Total Length matching between P and N within a Differential Pair	Yes	0.381
2	Within Layer matching between P and N within a Differential Pair	Yes	0.254
3	Total Length matching between TX pairs of multiple lanes	No	0
4	Total Length matching between RX pairs of multiple lanes	No	0
5	Total Length matching between TX and RX pairs of multiple lanes	No	0
6	Total Length matching between DATA pair and CLK pair	Yes	1.27

#### 6.22.1.1.1 Device Down Topology

Pcb Type: None

Pcb Thickness: None

**Figure 100. Device Down Topology****Table 131. Device Down Topology Notes**

Note	Detail
Minimum total length	76mm
Number of vias allowed	Max 3 vias

**Mainstream, Rx, Tx****Table 132. Device Down Topology Mainstream, Rx, Tx Routing Guidelines**

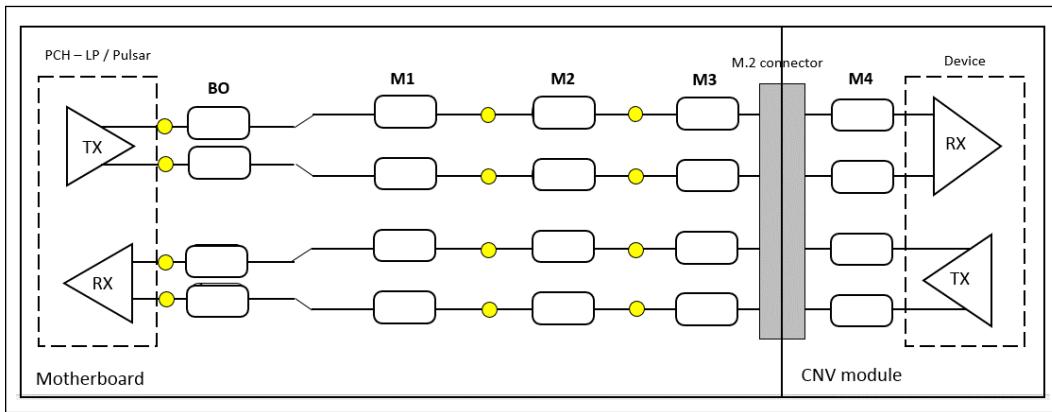
Segment	Tline Type	Max Length (mm)	Max Length Segment Note
BO	DSL, MS, SL	12.7	
M1	DSL, MS, SL	107.95	M1+M2 = 215.9mm
M2	DSL, MS, SL	107.95	M1+M2 = 215.9mm
M3	MS	25.4	

Max Length Total (mm): 254

**6.22.1.1.2 M.2 Topology**

Pcb Type: None

Pcb Thickness: None

**Figure 101. M.2 Topology**

**Table 133. M.2 Topology Notes**

Note	Detail
Minimum total length	76mm
Number of vias allowed	Max 3 vias

#### Mainstream, Rx, Tx

**Table 134. M.2 Topology Mainstream, Rx, Tx Routing Guidelines**

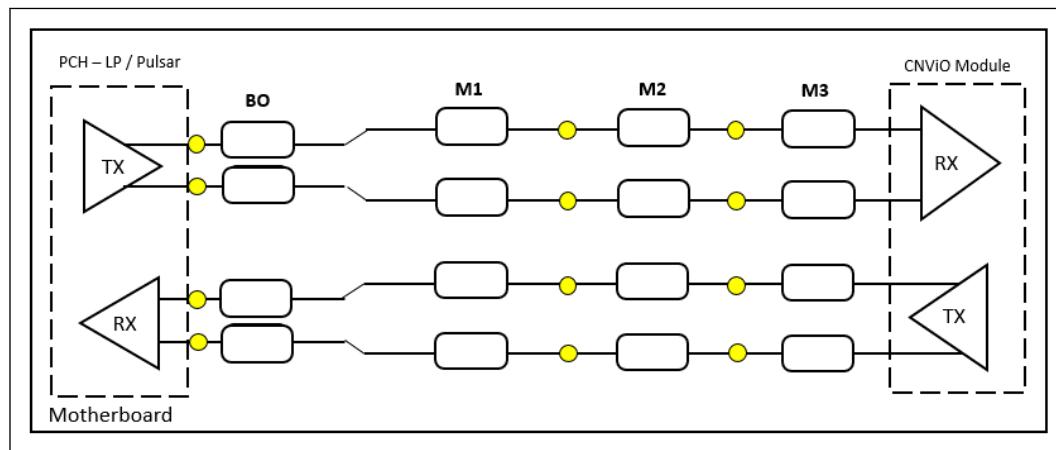
Segment	Tline Type	Max Length (mm)	Max Length Segment Note
BO	DSL, MS, SL	12.7	
M1	DSL, MS, SL	107.95	M1+M2=215.9mm
M2	DSL, MS, SL	107.95	M1+M2=215.9mm
M3	MS	25.4	

Max Length Total (mm): 254

#### 6.22.1.1.3 Module Down Topology

Pcb Type: None

Pcb Thickness: None

**Figure 102. Module Down Topology****Table 135. Module Down Topology Notes**

Note	Detail
Minimum total length	76mm
Number of vias allowed	Max 3 vias

#### Mainstream, Rx, Tx

**Table 136. Module Down Topology Mainstream, Rx, Tx Routing Guidelines**

Segment	Tline Type	Max Length (mm)	Max Length Segment Note
BO	DSL, MS, SL	12.7	
M1	DSL, MS, SL	107.95	M1+M2=215.9mm
M2	DSL, MS, SL	107.95	M1+M2=215.9mm
M3	MS	25.4	

Max Length Total (mm): 254

#### 6.22.2 Tools for Analysis

CNVio design can be simulated using differential trace model to ensure proper signal integrity for the maximum signal bandwidth.

#### 6.22.3 Tools for Debug

CNVio can be tested with the CNVio test tool or with the EMT tool. This tool will test the design marginality and can detect bus errors as well as very marginal signal integrity.

#### 6.22.4 CNVio Probing

It is recommended to avoid adding any probing pads or test points to the CNVio traces. However in cases where probing the CNVio bus is needed it is recommended to use a special soft touch probe. A special CNVio analyzer U4421A from Agilent (Keysight) can be used with a special cable and retention module. When designing for

using this probing set, the probe footprint is inserted within the CNVio traces while allowing the traces to maintain good impedance characteristics. An illustration of the probe and cable setup is shown in figure below.

**Figure 103. CNVio Probing Components**



## 6.22.5

### Routing Guidelines for BRI and RGI

These are GPIO signals (1.8V) running between the SoC and the RF companion module. The BRI and RGI signals share the same traces as UART signals (for discrete). Since the UART baud rate is expected to be lower than the BRI/RGI toggle rate it can be assumed the BRI/RGI sets the requirements for this bus.

BRI and RGI are two bi-directional buses. These signals have slew-rate controlled I/O's on both ends (SoC and RF companion) which should be optimized to minimize EMI/RFI while maintaining good signal waveform. No special control impedance is needed.

The BRI and RGI packets are ECC protected and with standard routing and signal integrity practices applied, no errors are expected to be noticed on the busses.

#### 6.22.5.1

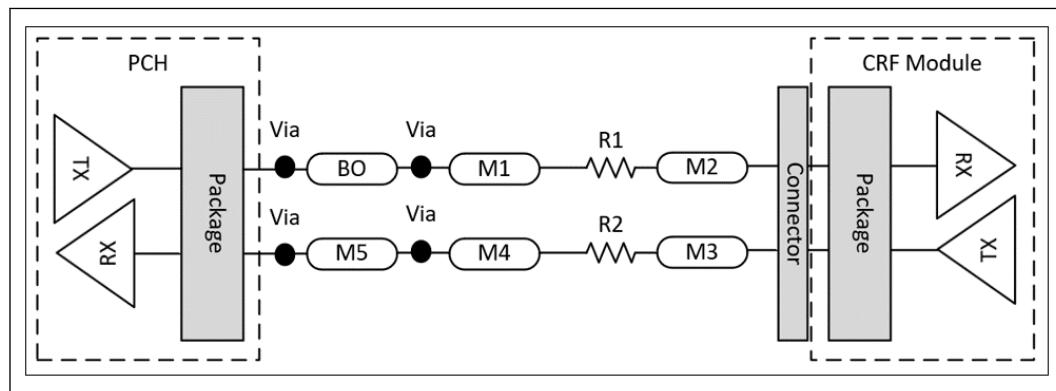
##### CNVi BRI and RGI

###### 6.22.5.1.1

###### 1-Load Topology (Device Down)

Pcb Type: None

Pcb Thickness: None

**Figure 104. BRI/RGI 1-Load Topology (Device Down) Diagram****Table 137. 1-Load Topology (Device Down) Notes**

Note	Detail
Number of vias allowed	4
Max Frequency	40MHz
R1	0Ω Placeholder. To be placed 12.7mm (can be extended to 25.4mm) from the PCH for CNV_BRI_DT and CNV_RGI_DT signal.
R2	39Ω. To be placed 12.7mm (can be extended to 25.4mm) from the connector for CNV_BRI_RSP and CNV_RGI_RSP signal.
Trace spacing between DATA and DATA signals	0.125mm
Signal Name/List	CNV_BRI_DT, CNV_RGI_DT, CNV_BRI_RSP, CNV_RGI_RSP

### Segment Lengths

Max Length Total (mm): 253.7

**Table 138. 1-Load Topology (Device Down) Routing Guidelines**

Segment	Tline Type	Max Length (mm)
BO	DSL, MS, SL	12.7
M1	MS	12.7
M2	DSL, MS, SL	228.3
M3	MS	12.7
M4	DSL, MS, SL	228.3
M5	DSL, MS, SL	12.7

## 6.22.6 Modem Coexistence 3-way UART Connection

In order to allow a “Hybrid Key-E” scheme supporting both connectivity and a cellular modem, there is a need to connect the modem coexistence bus in a configuration that will allow the modem to connect to the connectivity coexistence control logic.

In Intel connectivity modules this logic may reside in the M.2 module or in the SoC, depending on whether CNVi or discrete solutions are used:

- For CNVi, the logic resides in Pulsar/Quasar
- For discrete M.2 cards, this logic resides in the module

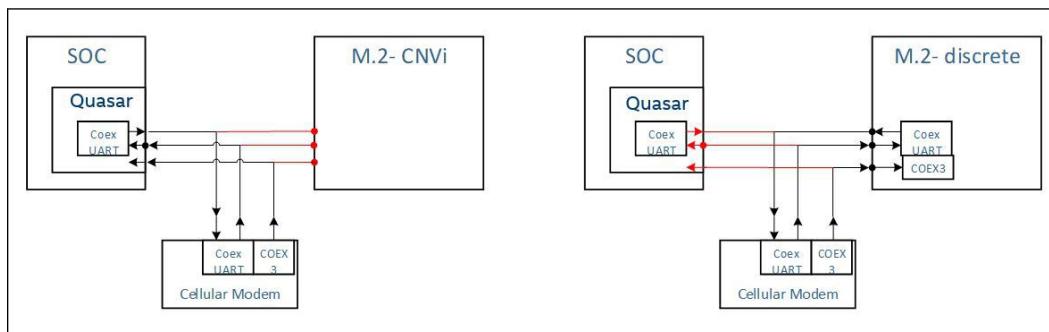
As a result, when a motherboard design contains a modem, and it is desired to be able to support CNVi and discrete on the same M.2 socket, there is a need to have a 3-way connection of the board as shown in figure below.

One can simplify the routing by adding a jumper resistor to select between the two configurations however this will result in losing the option to swap between CNVi and Discrete on the board. Any such swapping will then require board HW change for changing the jumper resistor position.

#### NOTE

when doing this 3-way connection between SoC, M.2 and the Modem there will always be an unused signal which is not optimally terminated for that connection. This signal is shown in red in figure below. The effect of this signal is similar to a stub which adds undesired impedance change to the trace. The effect of this stub on the UART bus depends on several system parameters, distance between the different UART pins, UART bus speed and electrical characteristics of the UART drivers and receivers (referenced to the signal pins). This effect must be considered and analyzed through design practices or simulations to ensure signal integrity is not compromised. For this analysis, the UART baud rate shall be assumed not higher than 4Mbaud.

**Figure 105. Coex UART for Connectivity/Modem in 3-way Configuration**



#### 6.22.7 SoC Termination Requirements

Due to special power up sequencing of the CRF and I/O requirements, the SoC I/O shall be terminated according to the following considerations:

- The 38.4 MHz clock from CRF to the SoC has an I/O buffer which is not powered when the CRF is initially powered up. The supply to this buffer will only come up following the first clock request from the SoC. To avoid floating input at the SoC clock pin it is recommended to add a weak **pull-down** resistor to the SoC pin. The resistor value shall be 10K ohm and it should be located close to the SoC pin. When adding this resistor the design should be checked to ensure it does not distort the clock signal.
- The BRI\_RSP and RGI\_RSP signals from CRF to the SoC have I/O buffers which are not powered when the CRF is initially powered up. The supply to these buffers will only come up following the first clock request from the SoC. To avoid floating input, internal pull-ups of 20K are provided at the SoC I/O pins; **no external pull-ups are required**.

- The **CNV\_RF\_RESET#** signal from the SoC to CRF is used as the main reset signal to the CRF during boot. This signal must have a stable value starting from initial power up of the platform and before the CRF power comes up. To ensure that the CNV\_RF\_RESET# signal is glitch free it is recommended that a **pull down** resistor be connected between the SoC pin and ground. A 75K ohm resistor to ground will ensure the stability of the signal. Since CNV\_RF\_RESET# is normally held at 1.8V it is expected to consume negligible amount of power (about 43uW continuously).

## 6.22.8 RF Companion Specifications

The electrical specifications of CRF can be found in below Electrical Specification document :

- Jefferson Peak 2 (Jfp) Electrical Specification document #567240
- Harrison Peak 2 (Hrp) Electrical Specification document #574370

## 7.0 Platform Ingredients

### 7.1 Intel® Management Engine (Intel® ME)

The following list of components compose Intel® ME hardware infrastructure:

- Intel® ME is the general purpose controller which resides within TGP-LP (which is Tiger Lake PCH-LP). It is resource-isolated from the host processor and operating in parallel to the host processor.
- The FW of Intel® ME is stored on SPI Flash together with other ingredient FWs.
- The Intel® ME code is executed from system DRAM in S0 state. This code resides in IMR. Intel® ME uses the main memory controller present in the processor to interface with DRAM. If Intel® ME is active in Sx state, it uses internal RAM on TGP-LP.
- The Intel® ME clock is provided by an internal ring oscillator in Sx/M3 states.
- It provide several sideband power sequencing signals that should be used in conjunction with an EC for platform power flows.

Enabling Intel® ME on the Tiger Lake platform requires the following:

- SPI flash
- Intel® ME to EC interface (at least minimal requirements)

#### 7.1.1 Acronyms

Acronyms	Description
APS	Automatic Power Switch
C-Link, CLink	Controller Link
DSW	Deep Sx Well
EC	Embedded Controller
M0	Intel® ME power state. The host CPU is in S0 and Intel® ME is operational.
M3	Intel® ME power state. The host CPU is in Sx and Intel® ME is operational.
Moff	Intel® ME power state. The host CPU is in Sx and Intel® ME is not operational.
Sx	System state S3, S4 or S5
TGL	Tiger Lake
TGP	Tiger Lake PCH
TBD	To Be Defined

## 7.1.2 Preface

Intel® Management Engine (Intel® ME) is the internal processor running Intel® ME firmware and dealing with platform management. It is connected to the flash, loading Intel® ME FW and Intel® ISH FW, running Intel® AMT section (where applicable), controlling EC for power states transition, and more.

Unless otherwise indicated, this content pertains to Tiger Lake platforms.

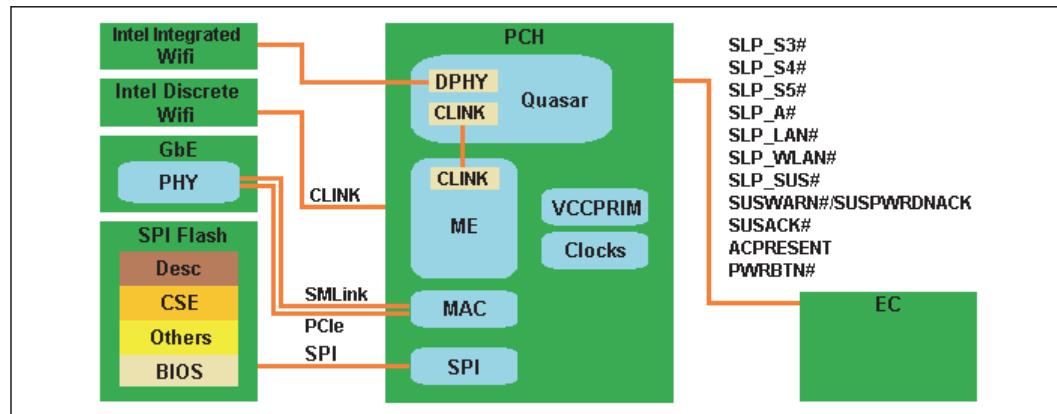
## 7.1.3 Reference Documents

Document	Document Number
Converged Security and Manageability Engine (CSME) and Embedded Controller (EC) Interaction	CCL# 573615

## 7.1.4 Signal Descriptions

Intel® ME interacts with the on-board EC with proper policy decisions during system power state transitions. The below figure illustrating the Sx (or DeepSx) power wells need to remain on for indicating power to LAN, WLAN and more with below sideband signals.

**Figure 106. Intel® ME Architecture**



### NOTES

1. Choose either one from Intel Wi-Fi solution above.
2. There is no on-board logic controlled by SLP\_A#. SLP\_A# is still provided externally to indicate whether Intel® ME is in Moff state or not.

## 7.1.5 Intel® ME to EC Interface Signals

The Intel® ME subsystem in the TGP-LP must communicate with the EC to indicate when the Sx and DeepSx power wells needs to remain on, to indicate when LAN and/or WLAN power are/is needed and to know the system power source (AC or battery) to make proper policy decisions. To allow this communication, several sideband signals are required between TGP-LP and EC.

Please refer to the "Converged Security and Manageability Engine (CSME) and Embedded Controller (EC) Interaction, CCL #573615" document for more information.

#### **NOTE**

There is no on-board logic controlled by SLP\_A# signal to power the Intel® ME. This signal is still provided externally to indicate whether Intel® ME is in Moff or not (so that the external devices may be powered accordingly)

### 7.1.6

### Optimization Guidelines

#### Intel® ME Guidelines on Corporate SKUs

There are two additional areas of board support that should be considered when designing with Intel® ME and Intel® ME applications. These two are the ability to access Intel® ME remotely (via LAN or Wireless LAN) and the ability for Intel® ME to support the M3 power state.

To support Intel® ME remote access:

- Intel® LAN (including SLP\_LAN# signal support) is required for LAN connectivity to Intel® ME and supported applications.
- Intel® Wireless LAN products (including SLP\_WLAN# signal support) is required for wireless network connectivity to Intel® ME and supported applications.
  - The internal Controller Link (CLINK) is used to manage the wireless devices.  
Please refer to "Tiger Lake Platform Controller Hub (PCH-LP) - External Design Specification (EDS) - Volume 1 of 2", CCL# 576591 for more detail on CLINK.

To support the M3 power state:

- Refer to [Platform Power Sequencing Specification](#) on page 430 in this document.

Given different considerations, it is possible to design three different types of platforms:

- Platforms that support M3 power states **and** use Intel® LAN PHY or Intel® Wireless LAN solutions.
- Platforms that do not support M3 power states **and** use Intel® LAN PHY or Intel® Wireless LAN PHY solutions.
- Platforms that support M3 power states **and** use a third-party LAN PHY solution.

Table below summarizes the power rails, power states and signals.

**Table 139. Power Delivery Summary for Intel® ME Subsystem**

What It Powers	Rail	Sx / M3	Sx / Moff	Sx / Moff/ WoL3	Enabled By	Power OK Indicator
<b>Common</b>						
Platform 5V rail	V5.0A	On	On	On	NA	NA
DRAM VDD	V1.35 / V1.2	On in S3	On in S3	On in S3	SLP_S4#	NA
DRAM VTT	VDDQ/2	Off	Off	Off	SLP_S3#	NA

*continued...*

What It Powers	Rail	Sx / M3	Sx / Moff	Sx / Moff/WoL3	Enabled By	Power OK Indicator
Tiger Lake SoC	V1.0 VCC	Off	Off	Off	SLP_S3#	PCH_PWROK
<b>M3 Support + Intel® LAN PHY / Intel® Wireless LAN Solution</b>						
SPI interface	V1.8 or V3.3 SPI voltage	On	On	On	SLP_SUS#	RSMRST#
Wireless LAN Device	Power to the Wireless LAN Device	On	Off	On	SLP_WLAN #	NA
LAN PHY	Power to the LAN PHY	On	Off	On	SLP_LAN#	NA
<b>No M3 Support + Intel® LAN PHY / Intel® Wireless LAN Solution</b>						
SPI interface	V1.8 or V3.3 SPI voltage	On	On	On	SLP_SUS#	RSMRST#
Wireless LAN Device	Power to the Wireless LAN Device	NA	Off	On	SLP_WLAN #	NA
LAN PHY	Power to the LAN PHY	NA	Off	On	SLP_LAN#	NA
<b>M3 Support + A third-party LAN PHY Solution</b>						
SPI interface	V1.8 or V3.3 SPI voltage	On	On	On	SLP_SUS#	RSMRST#
Note: 1. Intel® ME Local RAM is powered by VCCSRAM_1P0						

## LAN Considerations with or without Intel® Active Management (Intel® AMT) Support

For Intel® AMT support, Intel® ME Wake on LAN is a requirement.

### Wake on LAN (WoL)

SLP\_LAN# is used to indicate when power to the LAN PHY is needed. If Host Wake On LAN or Intel® ME Wake on LAN is enabled, the SLP\_LAN# signal will remain high to keep power on to the LAN PHY.

The Integrated LAN (VccLAN) rail does not need to be powered in Sx/M-Off state unless they are needed as indicated by the TGP-LP signals like SLP\_S3# and SUSPWRDNACK.

### Wake on Wireless LAN (WoWLAN)

SLP\_WLAN# is used to indicate when power to the wireless LAN device is needed. If Host Wake on Wireless LAN is required in S3/S4/S5 or DeepSx states, the host BIOS must set HOST\_WLAN\_PP\_EN. Refer to the "Tiger Lake Platform Controller Hub (PCH-LP) - External Design Specification (EDS) - Volume 2 of 2" document, CCL# 575857, to the section discussing initialization of the HOST\_WLAN\_PP\_EN bit. The SLP\_WLAN# signal will remain high to keep power on to the wireless LAN device.

### NOTE

Unless controlled by system User, RF-Kill (W\_DISABLE#) should not be asserted by the EC when power is provided to the WLAN card as this will block communication with the Intel® ME during M3 state.

### WLAN Considerations with Intel® Active Management (Intel® AMT) Support

In designs where Corporate or Consumer Intel® ME are supported and wireless power management is supported, WLAN NIC power must be preserved in S0 and all its sub states (S0, S0ix, Connected standby and Modern Standby).

#### 7.1.7 Download and Execute (DnX)

DnX is Intel's proprietary solution to download FW module to a target machine from a host machine by means of USB cable and execute it. DnX flows are executed over fixed USB 2.0 port. On SPI platforms, this capability allows to access boot media for IFWI write as well as signed Token injection for debug unlock after the platform have completed manufacturing.

There are many advantages in using DnX, one of which is the capability to flash IFWI without opening the chassis to physically reach the flash device. This is especially important in the manufacturing line once the chassis is closed, in debug labs and in post manufacturing scenarios. Other methods such as FWUpdate and Capsule flow can be used on subsequent upgrades/downgrades if the platform can boot to an operating system. DnX is a capability in Intel® CSME ROM, where during the boot ROM can configure the USB port #0 on the PCH to connect to a remote computer to download DnX module which is signed by Intel. This module initiates rest of the Intel® CSME and sets up an environment to accept IFWI binary or secure token from a remote computer.

Following methods can be used to trigger DnX on the platform.

**Table 140. Methods to Trigger DnX**

Method	Description
Pin Strap	GPP_G2 is multiplexed with DNX_FORCE_RELOAD Refer to "Tiger Lake Platform Controller Hub External Design Specification (EDS) - Volume 1 of 2"
Intel® CSME or BIOS Error Handling Flow	If Intel® CSME or BIOS reach a critical error which prevent platform from booting, it can be programmed to enter DnX flow. (e.g Failure to authenticate BIOS signature, CSME detect FW corruption, etc.)
Empty Flash Device	When CSME ROM detects an empty flash device on the platform, it will enter DnX mode
BIOS HECI Call	BIOS can make a HECI call to Intel® CSME during boot to enter DnX after the reset

#### 7.1.8 SPI Flash Descriptor Security Override

To support Intel® ME, a SPI flash is required on the platform with sufficient space to hold system BIOS, Intel® ME firmware, Intel® Integrated Sensor Solution firmware and any additional third party data storage. The SPI flash needs to be powered in states S0 through S5, independent of Intel® ME power state.

GPP\_R2 / HDA\_SDO / I2S0\_TXD signal is used for Flash Descriptor Security Override (which is also known as Intel® ME Debug Mode). This signal input should be tied to a jumper which connects to power through an external pull-up (1 KΩ ±5%) only. When this signal is asserted, the Flash Security gets overridden for ease of image programming.

Customers are encouraged to implement this jumper - only on pre-productions designs, to be able to re-flash the SPI Flash device by customer technicians and/or by Intel Debug teams when asking help from them. This jumper may be removed from the board design before final production.

## 7.1.9 Intel® APS

Intel® APS is a tool for Intel® Platform Enablement Test Suite (Intel® PETS). Intel® PETS tool is used to test **compliance** to Intel® ME requirements and is a validation vehicle to assist with the reproduction of power management and power sequencing issues. The Intel® APS signals are required to be present at an accessible location on the board. Routing these signals to a connector is strongly recommended and will contribute significantly for accelerating debug and system validation.

An Intel® APS header allows for easy connection to a platform without extensive rework and/or intrusion by grouping signals required by Intel® APS to a common connector. It is strongly recommended to use one of the two proposed connector options described below.

The first option is to use a 18-pin Flat Flex Cable (FFC)/Flexible Printed Circuitry (FPC) connector, such as the 10051922-1810elf. It's a Lower Side Contact, Side Entry, Surface Mount ZIF Connector with 0.5 mm pitch. The pinout of the ZIF connector is shown in the figure below. This ZIF connector should be placed in an accessible location for accessing it without opening the chassis. It could be somewhere under the mobile system keyboard or inside the SSD/DDR module compartment. The keyboard or the SSD/DDR back cover could be lifted and the FFC/FPC could be plugged into the proposed ZIF connector, as shown in the below three figures. After well placing the Intel® APS adapter, all the necessary Intel® APS signal lines can be connected to the 18-pin 0.1" (2.54 mm) header of Intel® APS Adapter, as shown in the Figure "Intel® Automatic Power Switcher (Intel® APS) Adapter Connected". Please refer Intel representative for information of the Intel® APS Adapter and the FFC/FPC.

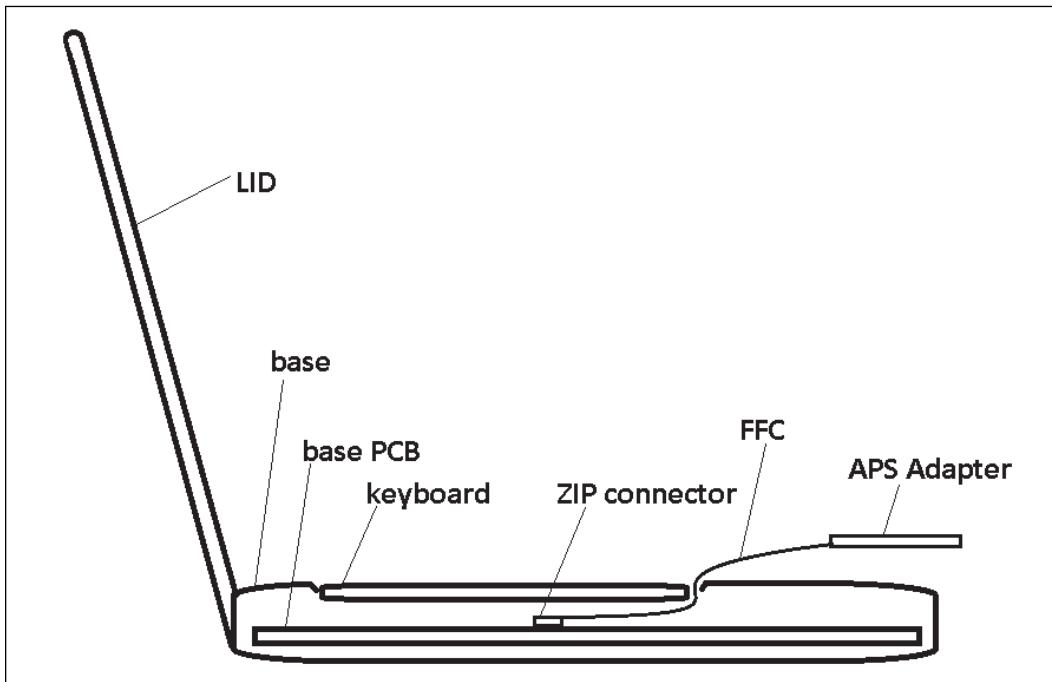
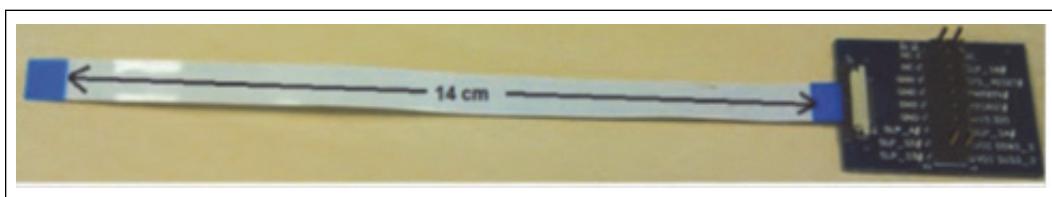
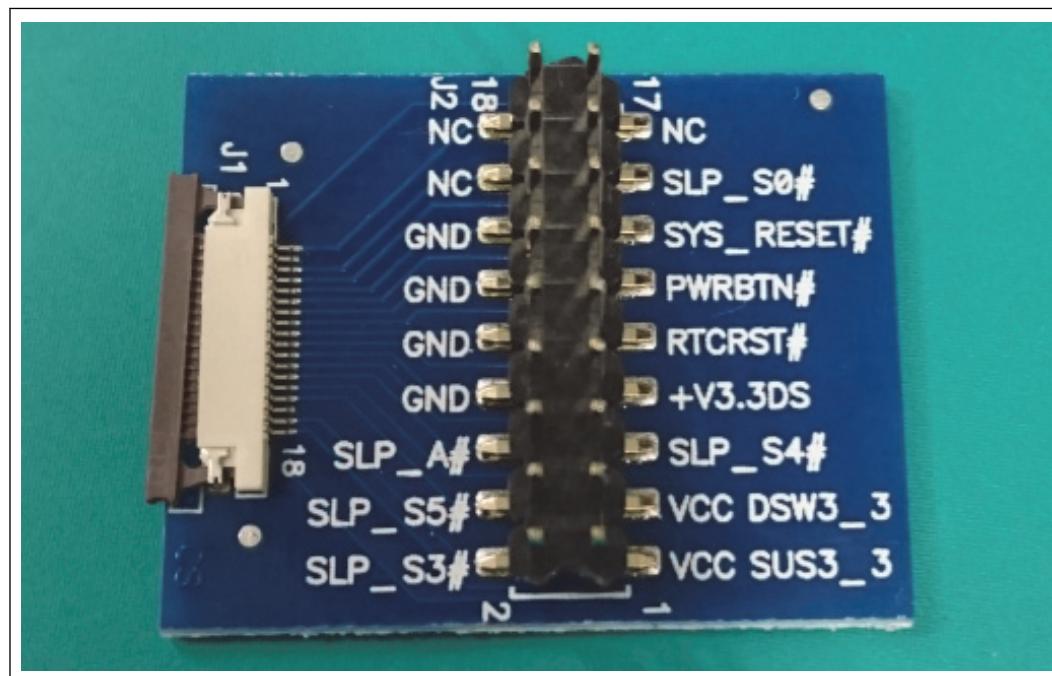
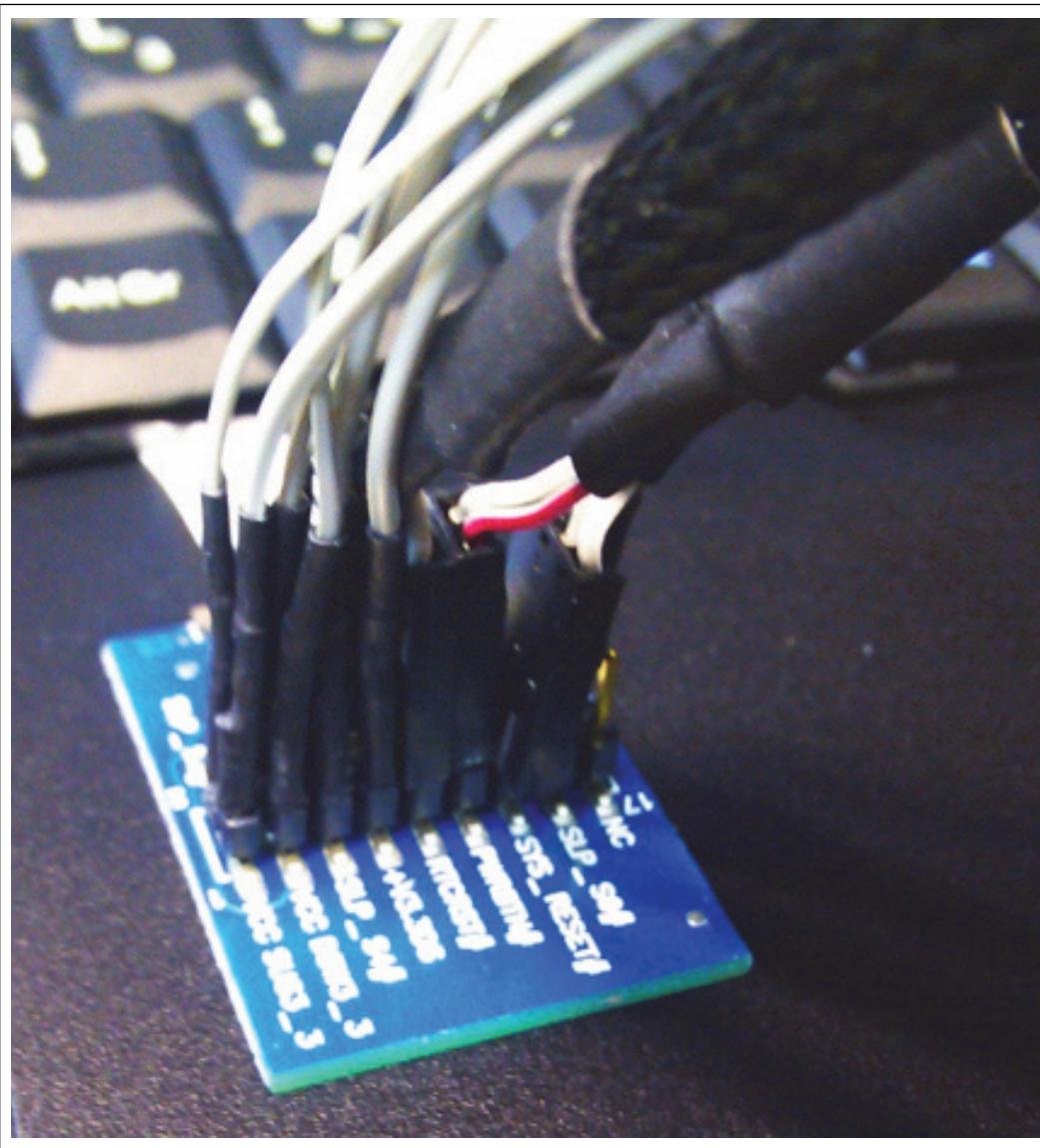
**Figure 107. Location of ZIF connector, FFC/FPC and Intel® APS Adapter****Figure 108. Intel® Automatic Power Switcher (Intel® APS) Adapter with a FFC**

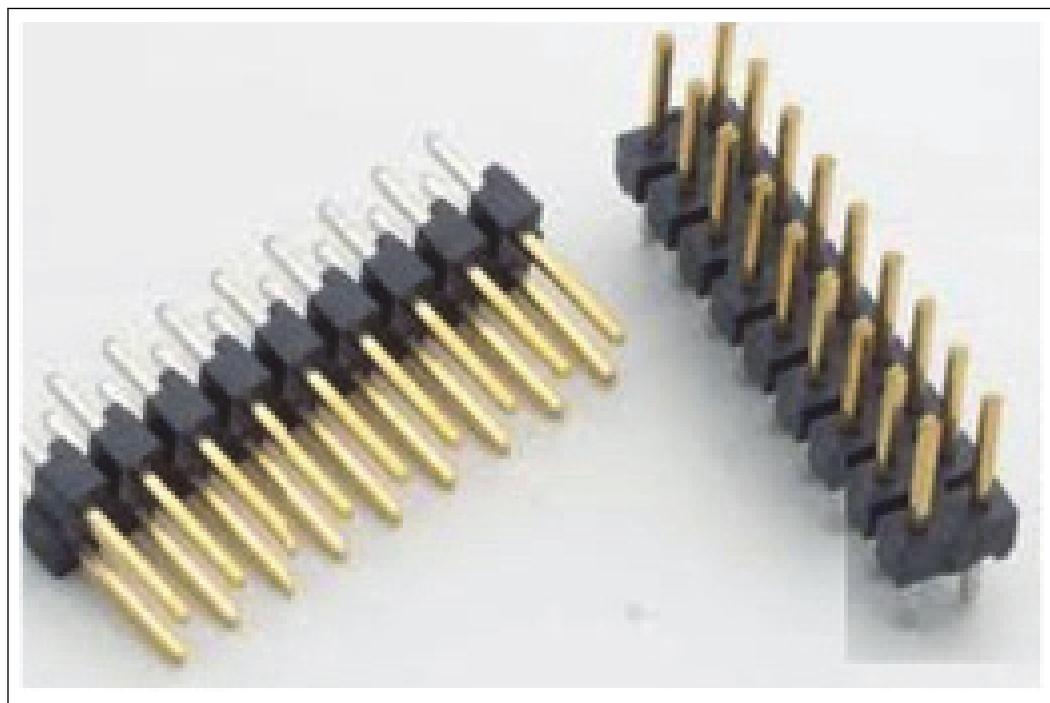
Figure 109. Intel® Automatic Power Switcher (Intel® APS) Adapter



**Figure 110. Intel® Automatic Power Switcher (Intel® APS) Adapter Connected**

The second connector option is to use a single 18-pin (2 rows of 9 pins) male header with pin width of 0.64 mm, pin height of 5.84 mm and a 2.54 mm distance (pitch) between pins, as shown in the figure below. The pin-out of the 18-pin male header is shown in the Table "Intel® Automatic Power Switcher (Intel® APS) Connector". These pins can be connected directly to Intel® APS. The Intel® APS Adapter is not necessary.

When system gets to the production stage, and if the Intel® ME subsystem is fully functional and is fully validated on pre-production systems, the Intel® APS connector may become "UN\_STUFF" (meaning, not being placed on the board). It is recommended to leave the footprint of Intel® APS connector with 'APS' label on silk screen next to the footprint on the system board. Solder down the Intel® APS connector to the footprint if the system is going to be sent to Intel for Intel® ME subsystem debugging.

**Figure 111. Intel® Automatic Power Switcher (Intel® APS) Header****Table 141. Intel® Automatic Power Switcher (Intel® APS) Connector**

<b>Pin</b>	<b>Signal Name</b>	<b>Description</b>	<b>Intel® APS Signal Name</b>
1	VCCPRIM_3P3	3.3V Primary Power Well	SUS
2	GPD_4_SLP_S3#	When asserted (0) system is in S3	S3
3	NC	No Connection	
4	GPD_10_SLP_S5#	When asserted (0) system is in S5	S5
5	GPD_5_SLP_S4#	When asserted (0) system is in S4	S4
6	GPD_6_SLP_A#	When asserted (0) Intel® ME is in Moff	M1/OFF
7	VCCDSW_3P3	Used to determine if the system is in Deep S4/S5	INEX1
8	GND	Ground	GND
9	RTCRST#	When asserted (0) CMOS is cleared	
10	GND	Ground for RTCRST#	
11	GPD_3_PWRBTN#	When asserted (0) Power Button is pushed	PWR B
12	GND	Ground for PWRBTN#	PWR B GND
13	SYS_RESET#	When asserted (0) Reset Button is pushed	RST B
14	GND	Ground for SYS_RESET#	RST B GND
15	GPP_B12_SLP_S0#	When asserted (0) system is in deterministic idle state	

*continued...*

Pin	Signal Name	Description	Intel® APS Signal Name
16	NC	No Connection	
17	NC	No Connection	
18	NC	No Connection	

**Table 142. Pin Location for Dual-in-Line Connector**

Signal Name	Pin	Header	Pin	Signal Name
VCCPRIM_3P3	1		2	GPD_4_SLP_S3#
NC	3		4	GPD_10_SLP_S5#
GPD_5_SLP_S4#	5		6	GPD_6_SLP_A#
VCCDSW_3P3	7		8	GND
RTCRST#	9		10	GND for RTCRST#
PWRBTN#	11		12	GND for PWRBTN#
SYS_RESET#	13		14	GND for SYS_RESET#
GPP_B12_SLP_S0#	15		16	NC
NC	17		18	NC

### NOTE

The unused or unconnected signal sampling lines which are INEX3 to INEX5 from the Intel® APS are better to be connected to GND for preventing from unexpected measurement results or risk. Without connecting these unused lines to GND, it is possible to damage the Intel® APS hardware. Because of this, it is strongly recommended to provide additional GND pins for the unused INEX sampling lines. For systems that do not implement Deep Sx, five additional GND pins are needed. For systems that do implement Deep Sx, only three additional GND pins are needed.

### Firmware Debug Hooks

The Firmware debug and its debug hooks are fully defined in Chapter “Platform Debug and Test Hooks”.

- The Firmware Debug Hook is used to support multiple components on the system, such as the CPU, Intel® ME and etc.

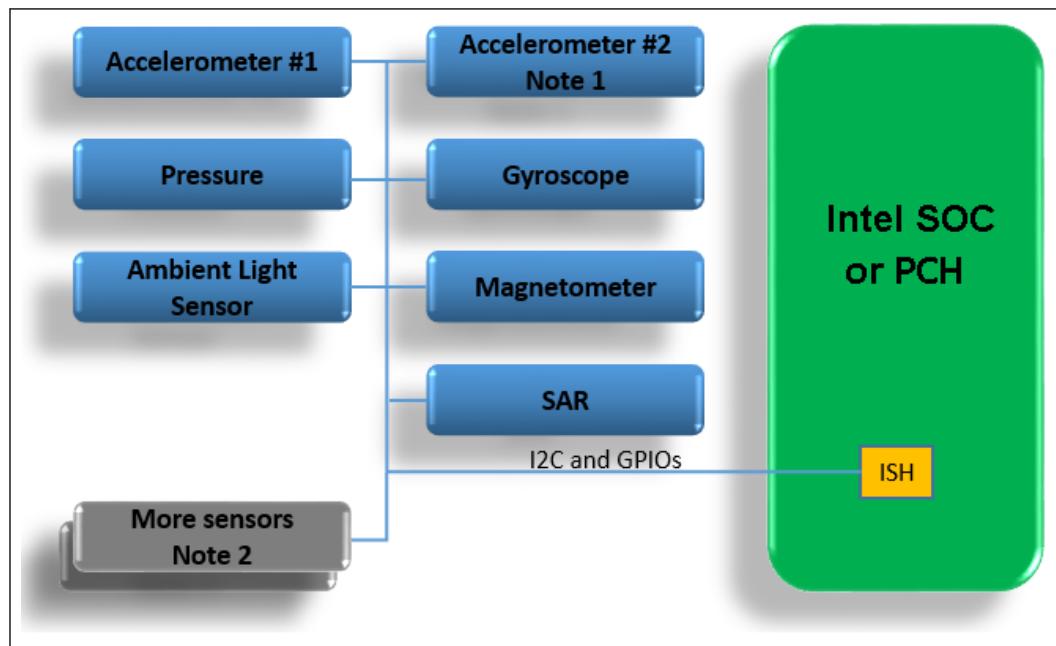
## 7.2

### Intel® Integrated Sensor Solution (IISS)

This platform uses an Intel® Integrated Sensor Hub (Intel® ISH) bearing the Tiger Lake Intel® Integrated Sensor Solution (IISS). This section provides the implementation recommendations of IISS for 2-in-1 (Detachable), 360-Clamshell, pAIO (personal All In One) and AIO (All In One) system designs. The intent of this document assists the usage of this IISS and sensor devices in hardware design to meet the Microsoft Windows\* 10 Operating Systems sensor recommendations. It is highly recommended to follow all of the design guidelines and perform all checklists. Do not deviate from any of the recommendations outlined in this document to prevent or minimize any functionality or responsiveness risks.

Figure below shows the block diagram of the SoC and the sensors.

**Figure 112. IISS Block Diagram**



#### NOTES

1. It is for 360-Clamshell design
2. More sensors are optional, as described in "BOM Innovation" section below

#### Sensors

Intel provide a list of sensors as IISS POR BOM. Intel provide support and perform full validation cycle on these sensors.

IISS firmware algorithms support only unprocessed and unfiltered raw data coming directly from the sensors. Any pre-process of the sensor data with internal FW which is inside a sensor is not support by IISS Firmware.

#### Sensors Extensibility Options

The designer has flexibility to choose different vendor for the sensor types that are not included in the proposed Intel POR BOM. Intel have developed the IISS Firmware Development Kit (FDK) to enable the extensibility. Please contact your local IISS AE for a FDK release. Following are the extensibility of BOM:

- **BOM Baseline**
  - Feature Set: Intel baseline (which is Windows\* HCK Support).
  - BOM: Integrated Sensor Solution (IISS) POR BOM
  - Intel differentiated: pressure sensor, activity context, device context and gesture.
  - uDriver: Intel own FW integration, calibration and validation.

- Support: Intel provide full support which includes validation on Intel systems.
- **BOM Flexibility**
  - Feature Set: Intel baseline.
  - BOM: OxM can replace sensor which is one of IISS supported sensor types from sensor vendor(s).
  - uDriver: OxM owns FW integration, calibration and validation.
  - Support: Intel provide FW and FDK. OxM integrate custom uDriver.
- **BOM Innovation**
  - Feature Set: Custom set with Intel baseline functionality supported.
  - BOM: OxMs can choose to add new types of sensors and/or algorithms.
  - uDriver: OxM owns FW integration, calibration and validation.
  - Support: Intel provide FW and FDK. OxM integrate custom uDriver and algorithms.

### 7.2.1 Acronyms

Acronyms	Description
BOM	Bill Of Material
EC	Embedded Controller
FDK	Firmware Development Kit
Intel® ME	Intel® Management Engine
Intel® ISH	Intel® Integrated Sensors Hub
OxM	ODM or OEM
POR	Plan Of Record
TGL	Tiger Lake
uDriver	Micro Driver
ZIF	Zero Insertion Force (connector)

### 7.2.2 Reference Documents

Document	Document Number
Ultrabook™ Platform - Magnetometer Design Integration Technical White Paper	535305
Intel® Integrated Sensor Solution (IISS) POR BOM	570092
Integrating Motion and Orientation Sensors (by Microsoft*)	<a href="https://msdn.microsoft.com/en-us/library/windows/hardware/dn642102(v=vs.85).aspx">https://msdn.microsoft.com/en-us/library/windows/hardware/dn642102(v=vs.85).aspx</a>
ISH EC Communication for Platform State Update	603384

### 7.2.3 Schematics Design

Intel highly recommend thoroughly understanding and implementing all of the design requirements outlined in the device datasheet avoid from sensor malfunctioning and support problems. The physical locations of the sensors on the main board or daughter board depend on board placement and the form factor.

Intel is not a sensor vendor. Follow manufacturers' datasheet and application notes for sensor design. It is recommended to include signal description, function description, trace length and air gap information in schematics where ever possible. Refer to the datasheet for the pin definitions and the reference schematics for the detail interconnections.

#### Sensors - I<sup>2</sup>C Bus Considerations

- Sensors can be connected to ISH\_I2C0, ISH\_I2C1 or ISH\_I2C2. It is required to ensure the total capacitance loading does not exceed the maximum bus load. There is no specified location for ISH\_I2C pull-up resistors, but it is recommended to place them on main board especially the sensors are on daughter board.
- It is important to note that Intel® ISH I<sup>2</sup>C interfaces support Vio with either 1.8V or 3.3V voltage. If customer's BOM calls for use of sensors which do not support the same voltage, customer should add a voltage level shifter where appropriate.

#### Sensors - GPIO Considerations

- For sensor interrupt output, each of Intel® ISH managed GPIO can be configured as input pin and connects to the output pin of a sensor with proper PU resister to Vio at the same voltage without a level shifter. Intel strong recommend that sensor components should not share interrupt line(s). Intel® ISH FW does not support it.
- For a 360-Clamshell design, it needs a 2<sup>nd</sup> accelerometer on the base and a main accelerometer in the lid. It is strongly recommended to add additional interrupt lines/traces from hall sensors/switches to Intel® ISH GPIO if the lid-close switch and the tablet switch are already connected to EC or other components. By doing this, it can help Intel® ISH FW to distinguish between 0° (which is in lid-close mode) and 360° (which is in tablet-mode) and calculate the correct angle between the lid and the base in a 360-Clamshell design. Some of Intel® ISH managed GPIO pins can be configured as GPIO output pins. Intel® ISH FW can trigger these output pins to EC or other components. One pin can represent two modes, two pins can represent four modes and so on. For example, if the angle between the lid and the base has been divided into 4 regions, 0~10 degrees means lid-close mode, 350~360 degrees means tablet mode, 10~190 means clamshell mode, 190~350 means book mode. The EC or other components can read these GPIO pins to know which mode it is now. Based on this information, the EC or other components can control power on/off to keyboard, touchpad, LED and more.
- For a 360-Clamshell design, this virtual sensor needs ISH managed GPIO as output(s) to EC. The number of ISH managed GPIO is limited. For saving GPIO pin count, please refer to CCL# 603384 for more detail on implementing a custom SW in EC. ISH managed I2C is the bus master. EC managed I2C is the bus slave.
- For a On-Table Detection design, it needs a primary accelerometer placed in the base. One of ISH managed GPIO can be configured as an output to EC as a bridge for noticing to DPTF (Dynamic Power and Thermal framework). This GPIO pin is optional if DPTF is ready to receive the noticing from the Windows framework.

## Sensors - Configurable Voltage Considerations

- Refer "Tiger Lake Platform Controller Hub (PCH) - External Design Specification (EDS) - Volume 1", # 615985. The configuration is done via soft straps during booting. Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.
  - Input: 1.8V level with 3.3V tolerant.
  - Output: the pin drives 3.3V via a ~20K pull-up. With this, any 1.8V device must be capable of taking a 20K pull-up to 3.3V.

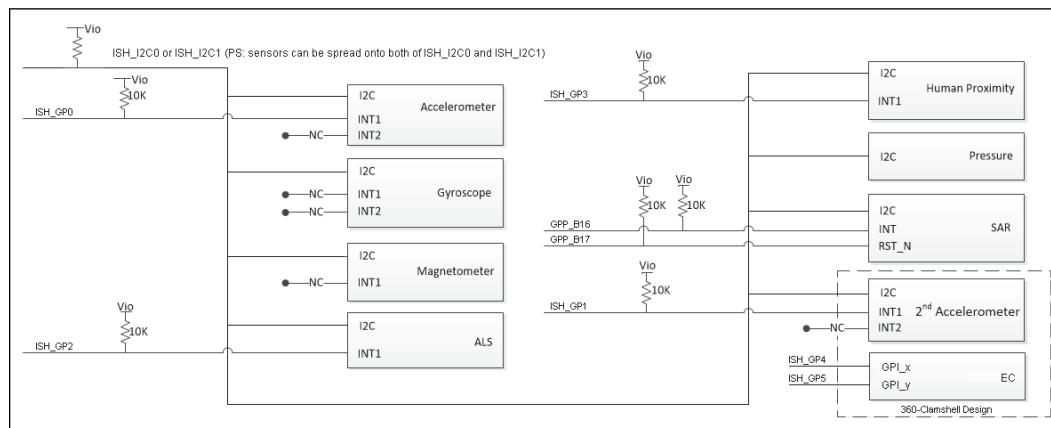
### WARNING

GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

## Sensors - Example of I2C Bus and Interrupt Connection

- Figure below shows an example of interrupt connections to Accelerometer, Gyroscope, Magnetometer and etc. All I2C buses and interrupt lines should have their own pull-up resistors for supporting Open Drain configuration in Intel® ISH FW. Please refer to the datasheet from sensor vendor for more detail.

**Figure 113. I2C Bus and Interrupt Connection Example**



## 7.2.4 Layout and Assembly

### General Rules

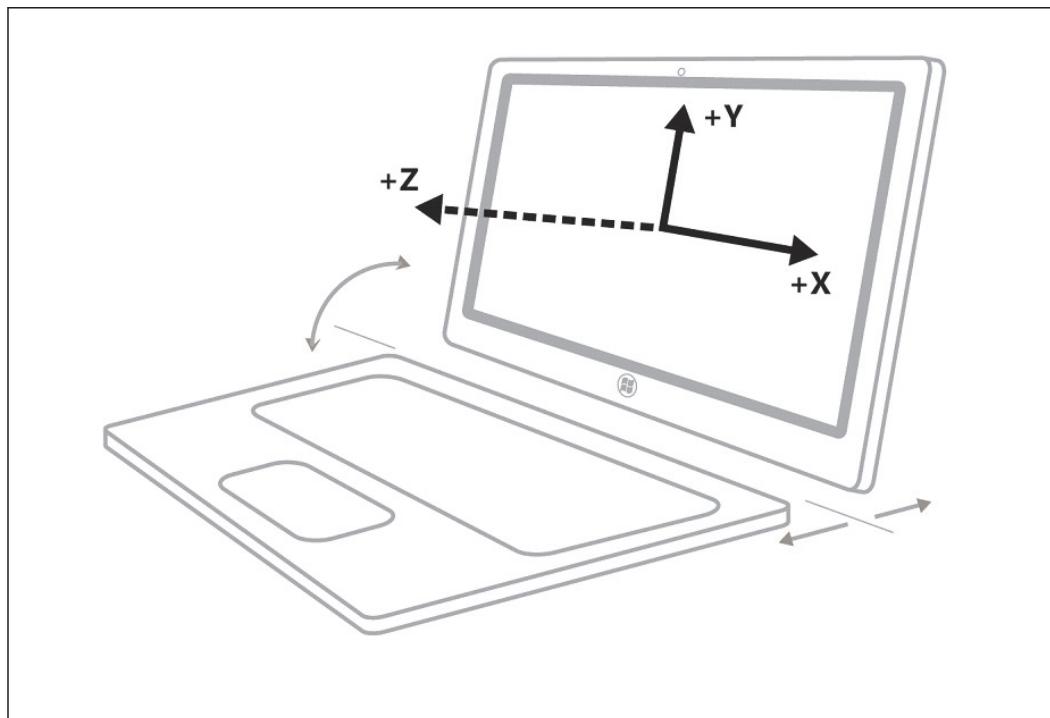
- Make the sensor placement to be the first step when outlining a new PCB layout. Plan accordingly accommodating to both of board and system level.**
- Understand and follow all the layout and design rule requirements from the sensor vendors and manufacturers.
- Place sensor 2 or 3 cm away from hot devices to avoid large temperature gradient.
- Place sensors at interference-free locations on the board in the system for all user scenarios.
  - Place the accelerometer in a stable position and isolated from any vibration.

- Place the magnetometer away from magnetic interferences.
- Place the ambient light sensor away from any unwanted lighting sources (for example: a LED indicator) in the system. Also make sure that the ambient light is not blocked.
- Do NOT place the sensor in a region of PCB that can warp as it can cause package stress which causes shift.
- Do NOT place the sensor at the position which has unsymmetrical stress coming from PCB deformation as it will cause drift.
- Design for manufacturing: Design a system that the board is easy to be assembled and ensure the board is fixed firmly without flex after the assembly.
- It is strongly recommended not to place any metal structure such as via, trace, plane and etc. in the area just below the sensor component on the top metal layer.

### Accelerometer

- The X, Y and Z axes of the sensor chip orientation is recommended to match the diagram below.

**Figure 114. Accelerometer X, Y and Z Orientation**



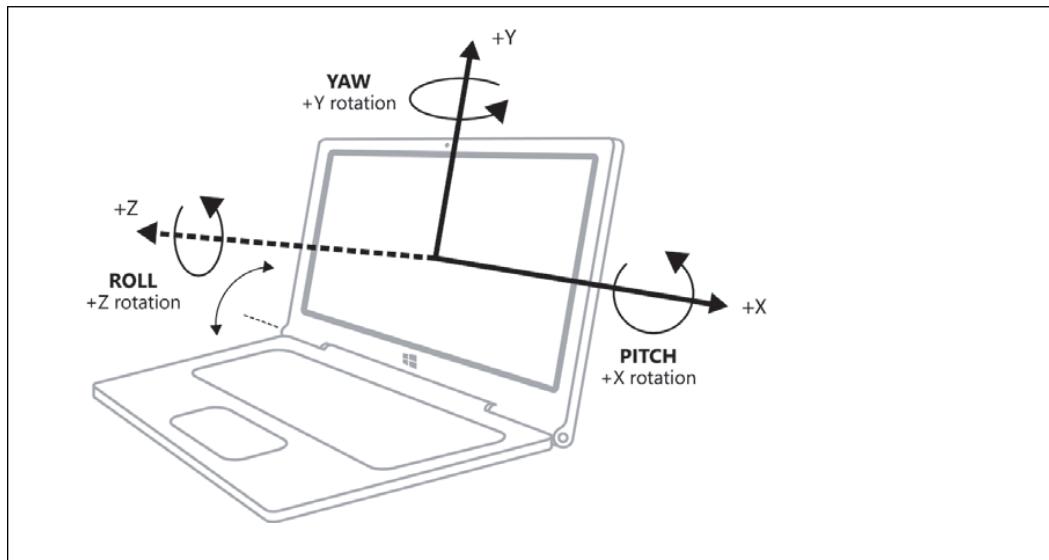
- Accelerometer must be mounted securely, near a screwed standoff point and can not move independently.
- Accelerometer must be placed in a stable position and isolated from any vibration including transmitted vibration, air pressure change vibration and etc.
- It is recommended that accelerometer is kept a distance of 30 mm away from audio speakers, fans and haptic vibration motors.

- Many modern electronic accelerometers have the ability to perform on-board filtering (e.g., removing DC gravity components in the signal). Intel® ISH specifically disables all on-board accelerometer filtering. All signal conditioning and signal thresholding of accelerometer are performed within Intel® ISH FW.

### Gyroscope

- The X, Y and Z axes of the sensor chip orientation is recommended to match the diagram below.

**Figure 115. Gyroscope X, Y and Z Orientation**



- Gyroscope must be mounted securely, near a screwed standoff point and can not move independently.
- Gyroscope must be placed in a stable position and isolated from any vibration including transmitted vibration, air pressure change vibration and etc.
- It is recommended that gyroscope is kept a distance of 30 mm away from audio speakers, fans and haptic vibration motors.

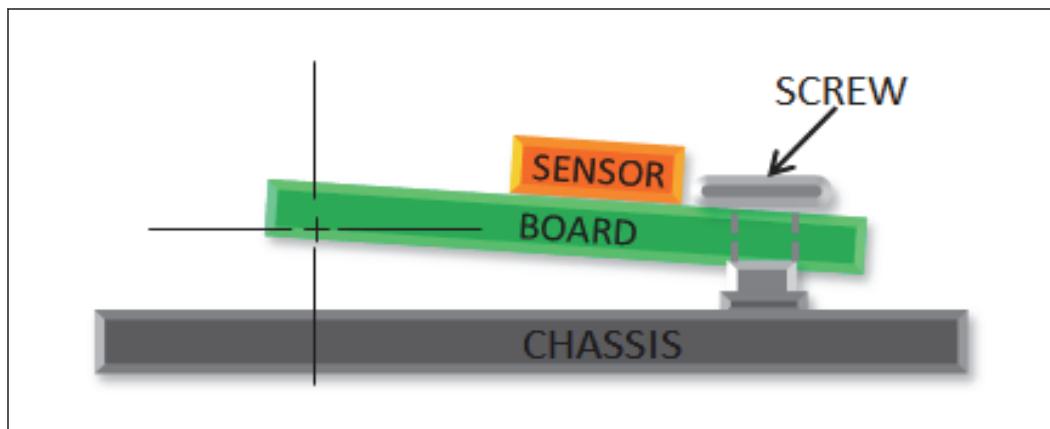
### Inconsistent Assembling of Accelerometer and Gyroscope

- **Issue Replication Steps:**

- System laid flat on leveled surface and Microsoft Sensor Diagnostic Tool showed system appeared to be moving (For example, XYZ accelerometer values are non-zeroes).
- Output from Gyroscope device showed system appeared to be rotating.

- **Possible root cause 1:**

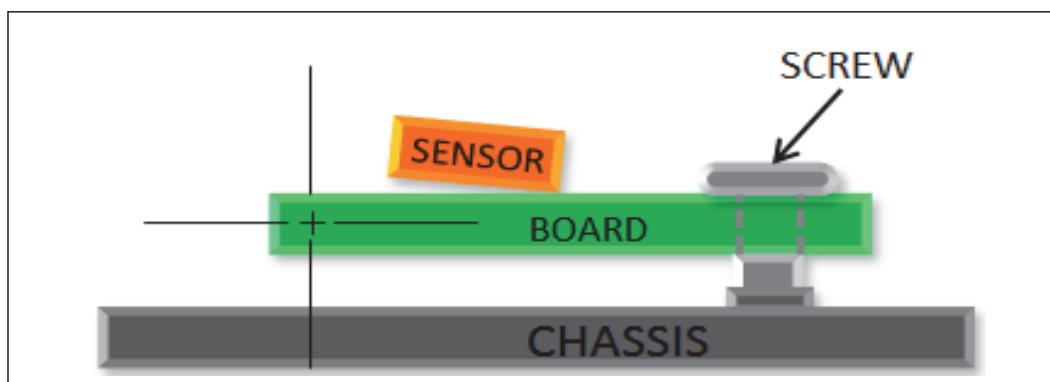
Sensor device was placed near screw holes. Board bends when screwed to chassis causes the sensor to skew, not leveled in referenced to the chassis.

**WORKAROUND:**

1. Relocate sensor device away from screw hole.
2. Perform per-System Calibration.

- **Possible root cause 2:**

Assembly house SMT machines inconsistent placements. Sensors soldered on the board are skewed in referenced to the main board or daughter board.

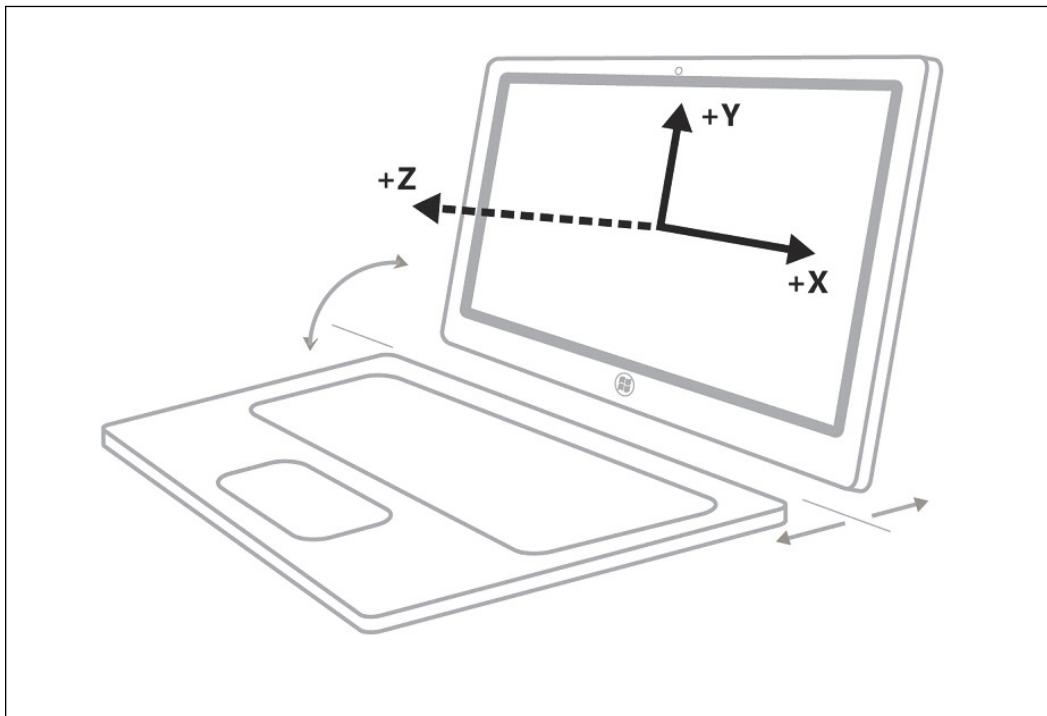
**WORKAROUND:**

1. Provide tighter SMT machine tolerance level.
2. Perform per-System Calibration.

**Magnetometer**

- The X, Y and Z axes of the sensor chip orientation is recommended to match the diagram below.

**Figure 116. Magnetometer X Y and Z Orientation**



- **Make the magnetometer placement be the first step when outlining a new PCB layout.** The ideal location for the magnetometer is to be as far as possible away from magnetized components, high current components and traces. The best locations are often to be found on edges and/or at corners of the PCB.
- Must place it at least 40 mm away from any rare earth magnets (speaker magnets, LID magnets, etc.) and inductors.
- Must place it at least 30 mm away from any large/thick (structural) ferrous metals, the components which includes the magnet of a hard disk, digitizer and the components with the magnetism of 100 Gauss.
- Keep a minimum distance of 10 mm away from the components which includes microphone, vibration motor, magnetic switch, transformer, camera module, beeper, battery, SAW filter, antenna, power amplifier, choke, LCD rear case and the components with the magnetism of 5 Gauss.
- Keep a minimum distance of 5 mm away from the components which includes memory socket, SIM card socket, USB connector, other connectors, screw, nut, spring, EMI shielding part and the components with the magnet-conductive material (which includes **Iron, Cobalt and Nickel**).
- Keep a minimum distance of 2 mm away from the surrounding resistor and capacitor since **Nickel plating** is usually present on solder end caps of surface mount components.
- **Keep it away from the power traces (which include power or ground plane) on all the PCB layers, component on both PCB sides and out of the board with the variable current higher than 10 mA. For instance:**

**keep a minimum distance of 20 mm away from the trace that carries the variable current of 100 mA or keep a minimum distance of 25 mm away from the trace that carries the variable current of 200 mA.**

- **Constant current has the interference as magnet. Make sure the interference does not cause the output of the magnetometer over the measurement range of the magnetometer.**
- Do NOT cover the magnetometer with any material that can block the static magnetic field from magnet and earth.
- As far as possible away from mechanical based HDDs, vibrators, hearing aid coils and battery connector which contain ferromagnetism, high frequency circuits and power circuits.
- Make sure LCD back shell, shield (for RF, BT...) and mechanical part (key, screw, connector) do not contain ferromagnetism material (Fe, Co, Ni).
- The same rules apply to the opposite side of the PCB.
- The same rules apply to any daughter boards or other components sandwiched in proximity to the magnetometer.
- Make sure the rules are followed in all the usage modes. (Example: The magnetometer is in the lid. Consider components on the base when system in tablet mode in a 360-Clamshell design.)

All digitizer solutions that employ a ferrous-based shield are unsuited for deployment with the magnetometer. Digitizers that require a ferrous-based shield are not supported by Intel® ISH FW due to the excessive soft iron distortion induced on the magnetometer. Other platforms possessing digitizer solutions that do not require a ferrous-based shield must conform to the general platform guidance for deploying magnetometer.

### Ambient Light Sensor (ALS)

- The ALS must be placed in the lid as close as possible to the camera module (if it is present). In order to allow effective control of screen brightness based on ambient light. The performance of the display brightening is ultimately defined by the performance of ambient light sensor and dimming to specified LCD luminance levels in response to ambient light changes. While the firmware has the ability to control the ALS signal gain and the LCD luminance response and proper mechanical design is still required to ensure the right user experience. Several hardware features must be considered when integrating ambient light sensors into system.

- **ALS Characteristics:**

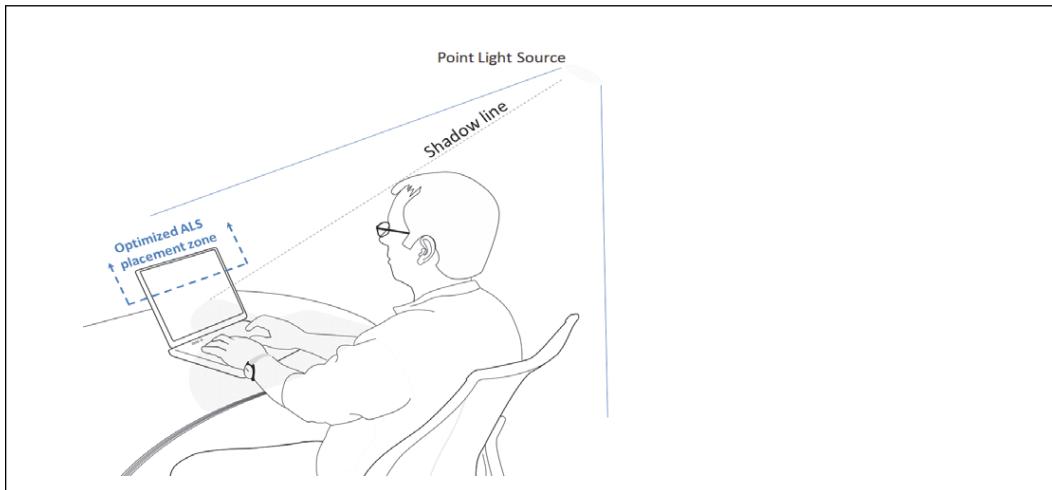
Characteristic	Specification	Notes
Illuminance Range	1-100k Lux	As output through sensor module which includes optics, surfaces, calibration data and etc. It's not only related to the bare sensor.
Accuracy	+/- 10%	As output through sensor module which includes optics, surfaces, calibration data and etc. It's not only related to the bare sensor.
Type	Digital	16-bit resolution.
ALS IR/UV rejection	Supported	Important for consistent measurement.

- **Aperture Placement:**

The light sensor aperture is required to be located on the same plane as the primary display which is facing to the user. This is necessary because the sensor measures the ambient light conditions facing the user for supporting adaptive brightness and light-aware applications that display their content on the screen.

- Avoid placing the light sensor in areas of the computer that are likely to be obscured from the light source or by shadows.
- Figure below illustrates an example of user scenario in which a direct light source is behind the user. A shadow is cast over the lower half of the screen and the base of the computer. The optimal light sensor placement is near the top of the screen and facing the user in this scenario.

**Figure 117. Ambient Light Sensor Cross Section**



- **Aperture Size:**

The aperture must be wide enough to detect light without significant attenuation when the light source is at an angle to the device or from a diffused source. A small hole or deep hole could cause a "Shadow Effect" which reduces the usability of the ALS sensor.

Oxm should work with their sensor vendor or manufacturer to determine the minimal and optimal aperture size.

- **Optical filter:**

In some instances, an optical film or ink coating may be applied to hide the ALS optical cavity. The filter must be designed to allow at least 80% of visible wavelength of light to pass. It means a light meter placed behind the film must register at least 80% of the LUX value from a direct light source that it registers with the film removed.

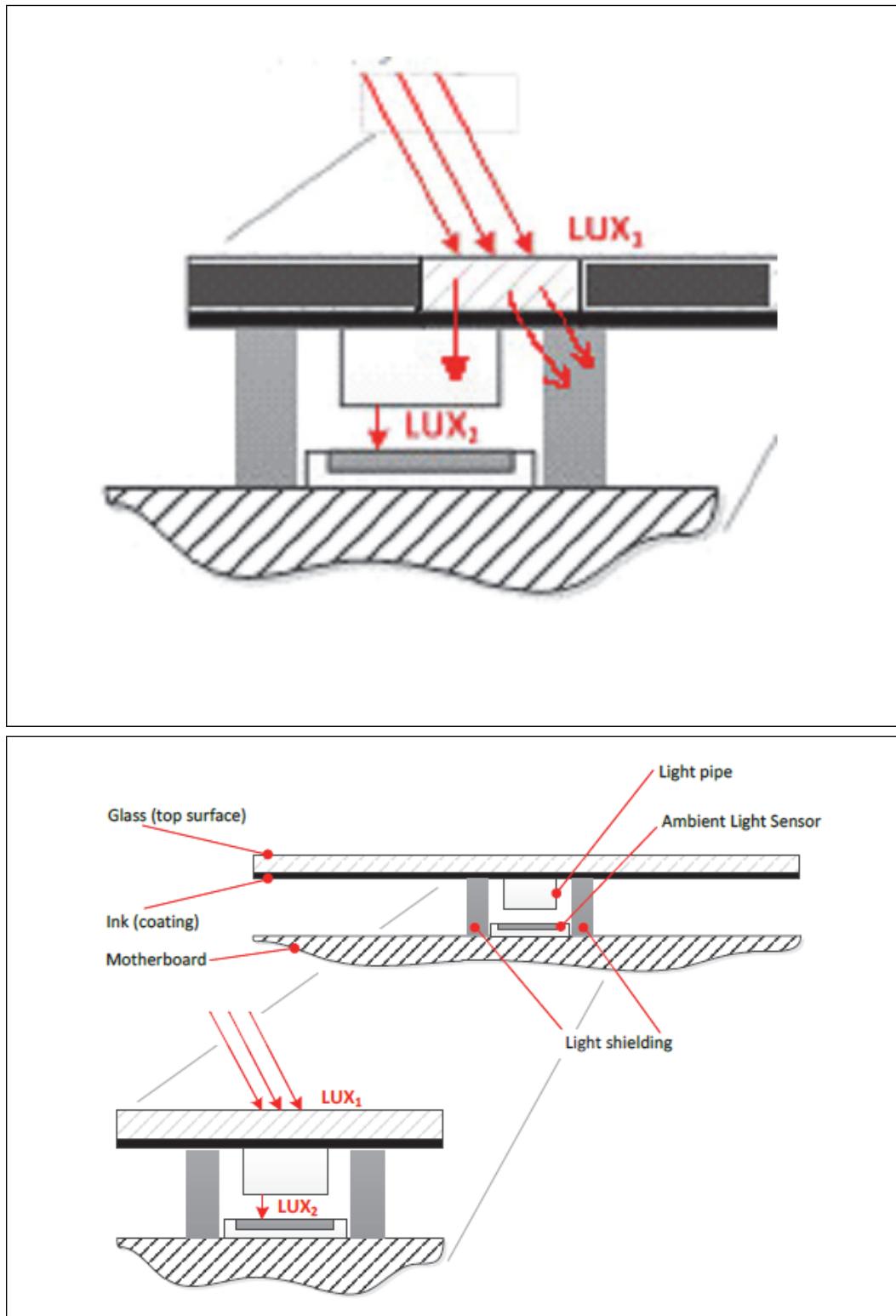
- **Light pipe:**

A light pipe constructed from a light-conducting material may optionally be deployed to increase the light-gathering ability of the optical cavity. This may be required in cases where the ALS optical cavity is excessively deep, inhibiting light gathering from off-axis (i.e., angled) and diffused light sources.

- **Cover Consistency of Glass/Cover**

- The glass or plastic covering material must be consistent across the units of the same model. Failure to follow this recommendation will result in inaccurate readings from the ALS based on the per model calibration parameters.
- Care must be taken when placing the Glass/Cover. A misalignment would mask out some of the light and produce unexpected readings from the ALS.

**Figure 118. Ambient Light Sensor Cross Section**



### Pressure Sensor

- In order to achieve the specified performance for your design, the following recommendations when mounting a pressure sensor on PCB:
  - The clearance above the sensor package shall be 0.1mm at minimum.
  - For the device housing appropriate venting needs to be provided in case the ambient pressure shall be measured.
  - Liquids shall not come into direct contact with the device.
  - During operation pressure sensor is sensitive to air pressure variation, fast heating and light heating which can influence the accuracy of the measurement.
  - The pressure sensor should not be placed at the position where has unwanted fast air pressure variation caused by fans, speaker and etc.
  - The pressure sensor shall not be placed close the fast heating parts in case of gradients > 3°C/sec. It is recommended to follow the vendor's application note and contact the vendor representative for details.
  - The area below the sensor (on the same side of the board) must be defined as keep-out area. It is strongly recommended not to place any structure in top metal layer underneath the sensor.

### Specific Absorption Rate (SAR) Sensor

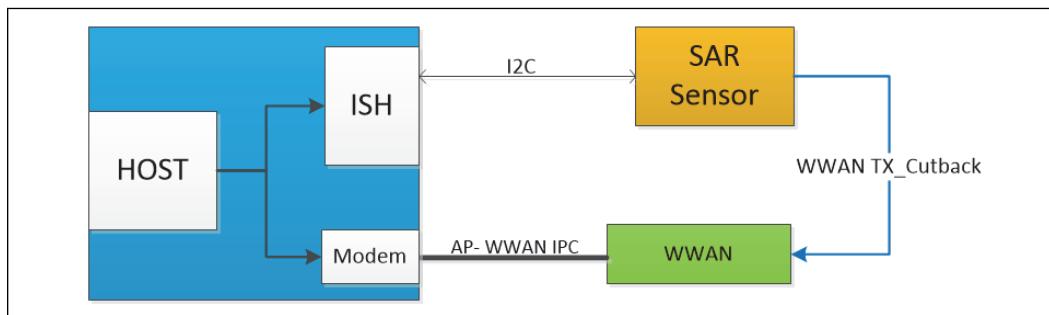
- **SAR**

SAR sensor is used as a proximity sensor to identify conductive objects (human body parts such as ear, head, lap and torso) presence near the transmitting system antenna. SAR requirements limit the levels of transmitted RF power to ensure that the power absorbed by a human body is below certain limits established by regulatory bodies around the world. This may require that a device reduce its RF transmitting power when it is in close proximity to the human body. In these systems, the SAR sensor activation is used to allow the device to operate at a higher power (and increased operating range) when the antennas are not close to a body but then reduce the transmission power of the relevant antenna to ensure compliance with the RF exposure requirements when close to the human body. Many regulatory bodies globally are aligning to International RF exposure guidelines or the FCC limits.

SAR needs to be evaluated for transmitters operating anywhere in the RF spectrum (9KHz - 300GHz) and so it is relevant to cellular technologies, Wireless LAN technologies and many other wireless technologies supporting data and/or voice.

A simple SAR sensor control over Antenna power is described in the figure below. In this way, the SAR sensor directly controls the WWAN transmitter power. This is the most efficient way remain compliant with the RF exposure requirements without any additional logic.

**Figure 119. Simple SAR Sensor Control over WWAN Antenna Power**



- **Regulation Sources**

The following are the 2 RF exposure requirements for devices that are used in close proximity to the body (within 20 cm). As this can be a changing field, the data published in this section is as it was known in the time of publishing of this document:

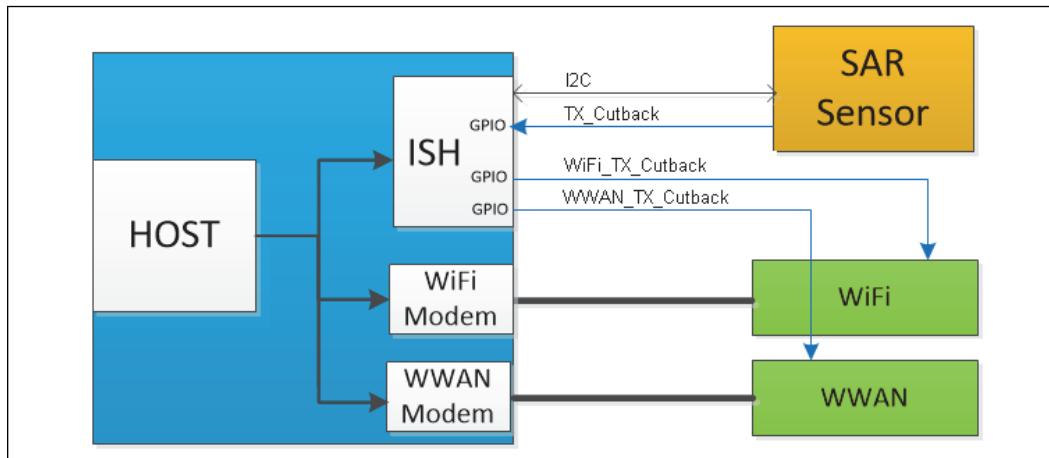
- **United States:** The relevant FCC Requirements for the FCC requires that devices used in close proximity to the body have a SAR level below 1.6 watts per kilogram (W/kg) measured over the volume containing a mass of 1 gram of tissue that is absorbing the RF energy.
- **European Union:** CENELEC specify SAR limits within the EU, following IEC standards (IEC 62209-2:2010). For devices used in close proximity to the body, the SAR limit is 2.0 W/kg measured over the volume containing a mass of 10 grams of tissue that is absorbing the RF energy.

- **Co-SAR**

In more sophisticated systems where the system support both WWAN phone and IP phone (e.g., such as WWAN and Wi-Fi).

Figure below shows a recommended way to control antenna power using an algorithm that runs on the Operating system (OS). In this way, the OS has control over each antenna for controlling the transmitted power to ensure compliance with RF exposure requirements.

**Figure 120. Co-SAR Sensor Control over WWAN Antenna and Wi-Fi Antenna Power**



- **Design Guidelines**

1. There are two main relevant usage models that should be covered by SAR sensors used to reduce transmission power of the antenna:
  - When bringing the system to the users' ear, so phone speaker (and RF antennas) is closed to the users' ear and head. This is mainly relevant to "Mobile Phone" systems, such as handsets and phablets.
  - When placing the system on or close to other human body parts, such as the lap or torso. This is mainly relevant to laptop/clamshell, tablets, phablets and similar types of device.
2. The sensor electrode may be a simple copper area on a PCB or FPC (Flexible PCB) for example with an adjacent reference ground area. Sensor electrode capacitance (to ground) will vary when a conductive object is moving in its proximity.
3. The sensor electrode needs to be located close to the antenna or antennas that it is controlling. Having the sensor be away from the antenna makes trigger distances unreliable. The size, shape and position of the sensor electrode are largely dependent on the system usage model. Typically, the sensing area for on ear detection is around the speaker at the top of the mobile phone and near the camera.
4. Conductive tape (copper tape) works well for prototypes, while FPC is suggested for mass production.
5. Keep the SAR sensor area away from area that human finger touches, such as a touch screen, systems' buttons, keyboard and etc. There is no need to throttle antenna power in such a case as the extremity SAR requirements are 2.0 W/kg over 10g of tissue mass.
6. Robust electrode design is the one that minimizes environmental (parasitic) capacitance noise value and variation of it.
7. Power reduction values need to consider both the stand-alone use of a transmitting antenna and simultaneous transmissions from multiple antennas, where supported. The combined SAR value from these antennas needs to meet the relevant limits.
8. System design considerations need to ensure that the default power state is always the reduced power state such that if the SAR proximity sensor circuitry is failed.
9. The software controls need to be robust and must not be user accessible (i.e. the user must not be able to modify the power reduction settings or disable the sensor). Firmware and software updates need to be carefully tested to ensure that the proximity sensor functions are not bypassed.
10. Where the proximity sensor enables large power reduction regulatory bodies such as the FCC may expect to refer a description of how the sensor performance is verified across production units. This may necessitate the use of test software, test fixtures and sampling at the production floor. Large power reduction values can trigger device surveillance testing by regulatory agencies so quality control at the production level is important.
11. In general, wherever possible, place the transmitting antennas in areas not accessible to human body parts, so eliminate the need for SAR sensor circuits and the need to lower transmission power. This is difficult in tablets, 2-in-1 and phones which are small and difficult to have an antenna that would not be in close proximity. For tablets it makes sense to keep the antennas toward the front (screen side) of the device to maximize separation from person. Other

items to suggest here might be the ability to keep antennas that might operate simultaneous (Wi-Fi and WWAN in hot spot mode, for example) as far apart as possible to reduce the need for power reduction in those modes.

- **Device Requirements**

The electrode and circuit design need to meet the following minimum requirements:

1. The sensor electrode needs to be placed on the inner side of the back cover, close to the transmission antenna, and properly shielded with ground to minimize the interference from the surrounding electronics. The shield needs to be tied to the platform ground to remove the ground bouncing noise and false proximity detection from the platform ground traces.
2. Sensor should be placed very close to the electrode to reduce noise. Routing from sensor electrode to sensor needs to be coaxial cable with ground shielding.
3. Sensor proximity range requirement needs to be determined after SAR testing, but can start with 10 mm from the back and side close to where the transmission antennae are placed in the form factor system.
4. Sensor detect range should be 0-60pF with distance of 20 mm from a human body part.
5. SAR sensor circuit power needs to be less than 0.1 mW.
6. SAR sensor proximity range for human body and other non-conductive material (such as tablet top) should have big enough delta so that it can be programmed/tuned to detect only the human body proximity and not other non-conductive material.

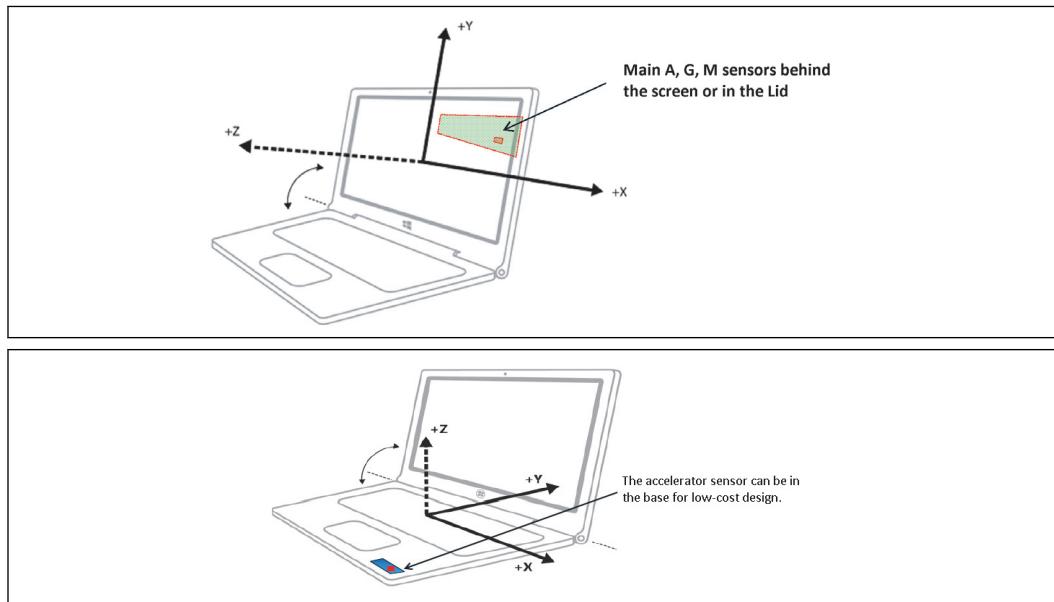
## 7.2.5 Form Factor Considerations

This section illustrates the sensor placement for form factors such as Clamshell, Detachable, 2-in-1 (360 hinge, Twist, Slider, Ferris Wheel, etc.), and pAIO (portable All In One).

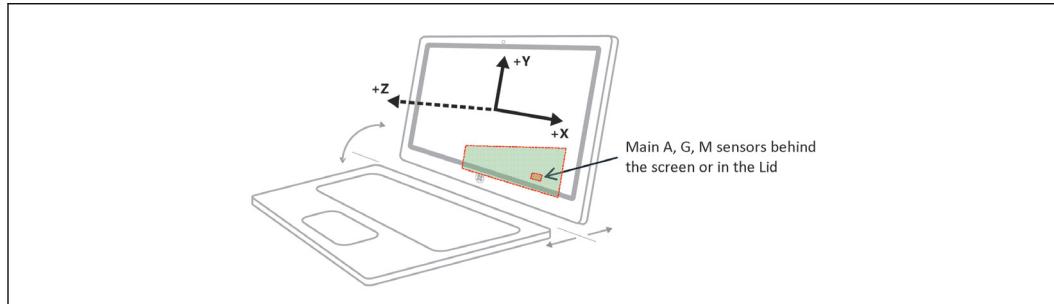
- For all the form factors, it is must to place the primary accelerometer, gyro and magnetometer sensors in the lid or behind the screen.
- For 360-Clamshell designs, please must place the 2<sup>nd</sup> accelerometer in the base.
- For Low-cost Clamshell designs which only support screen rotation, the primary accelerometer is the only available sensor which can be placed in the base. On-Table Detection is supported by the primary accelerometer placed in the lid. Please contact local ISH AE for more detail if On-Table Detection is enabled on Low-cost Clamshell designs.

### System/Chassis Integration Options

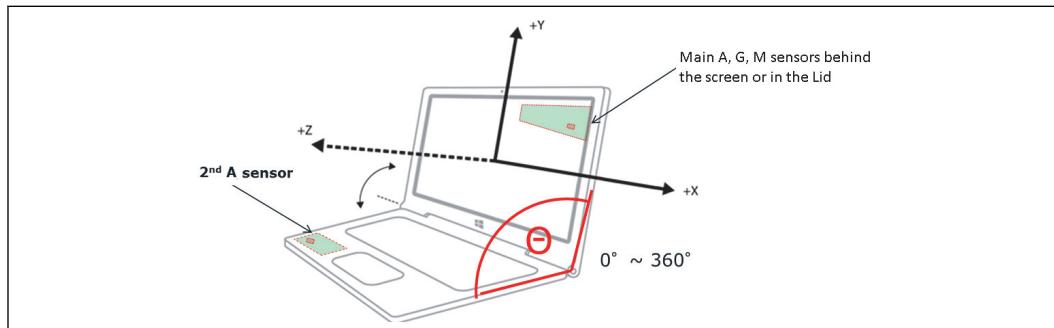
- Clamshell: Main sensors behind the screen or in the lid. For low-cost design, the accelerometer sensor can be placed in the base.

**Figure 121. System/Chassis Integration Options: Clamshell**

- Detachable: Main sensors behind the screen or in the lid.

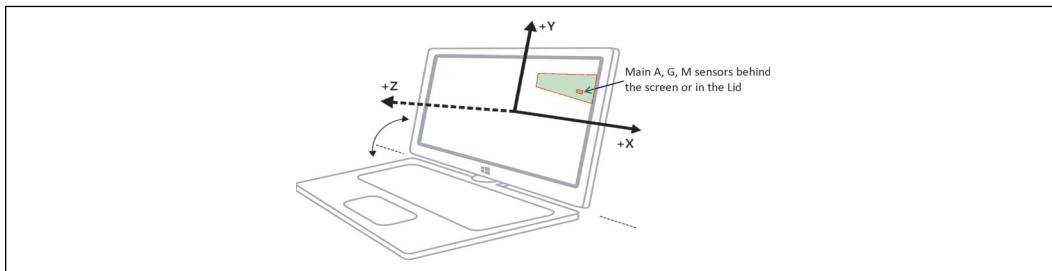
**Figure 122. System/Chassis Integration Options: Detachable**

- 2-in-1 with 360 hinge: Main sensors behind the screen or in the Lid. The 2<sup>nd</sup> accelerometer is in the base.

**Figure 123. System/Chassis Integration Options: 2-in-1 with 360 Hinge**

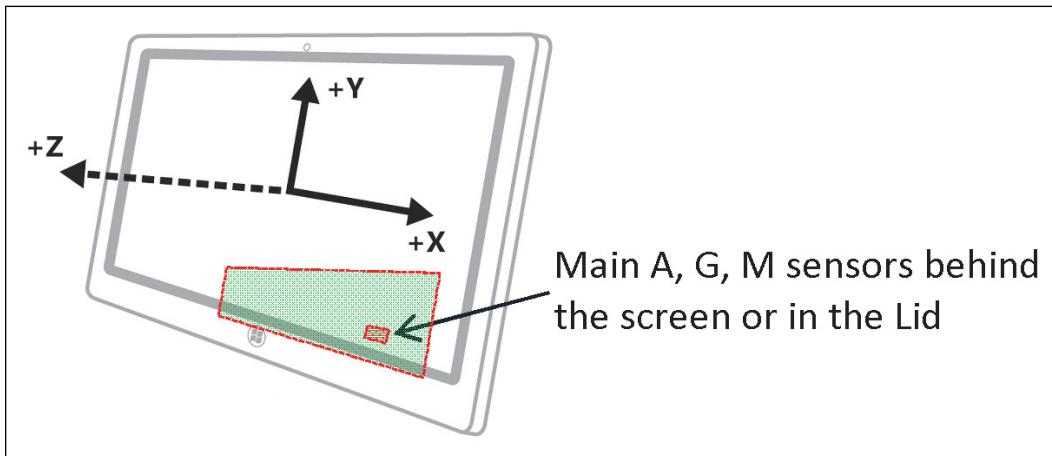
- Other 2-in-1: Main sensors behind the screen or in the lid.

**Figure 124. Other 2-in-1: Twist**



- pAO: Main sensors behind the screen (Lid).

**Figure 125. System/Chassis Integration Options: pAO**



## 7.2.6 System Debug

System debug hook is an important part of the HW design. It provides the ability to access the system without harming the chassis too much. Otherwise, it will be difficult for Intel to assist within the stipulated time frame.

The debug hook may be eliminated from production systems. For high dense designs, customer is proposed to replace it with test pads. Intel expect these debug hooks to be implemented on customer's system.

Debugging Tiger Lake IISS may be divided into two main areas:

- Firmware debug
- Sensor debug

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### NOTE

Connecting I<sup>2</sup>C debug device that has build in I<sup>2</sup>C pull-up resistors will change the final value of pull-up resistors. The wrong pull-up resistors may cause Intel® ISH I<sup>2</sup>C bus not to work. Please refer to Section "I<sup>2</sup>C\* Interface Design Guidelines".

## Firmware Debug Hooks

The Firmware debug and its debug hooks are fully defined in Chapter “Platform Debug and Test Hooks”.

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### NOTE

The Firmware Debug Hook is used to support multiple components on the system, such as the CPU, Intel® ME and etc. It is not specific to Intel® ISH.

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## Sensors Debug Hooks

IISS requires the below signals to be routed to a connector which should be mounted on the system board in an easy accessible location.

Connection	Function
ISH_I2C[0:2]_SDA	Intel® ISH managed I <sup>2</sup> C ports
ISH_I2C[0:2]_SCL	
ISH_GP[0:7]	Intel® ISH managed GPIO pins
Vio	Sensor Reference Voltage

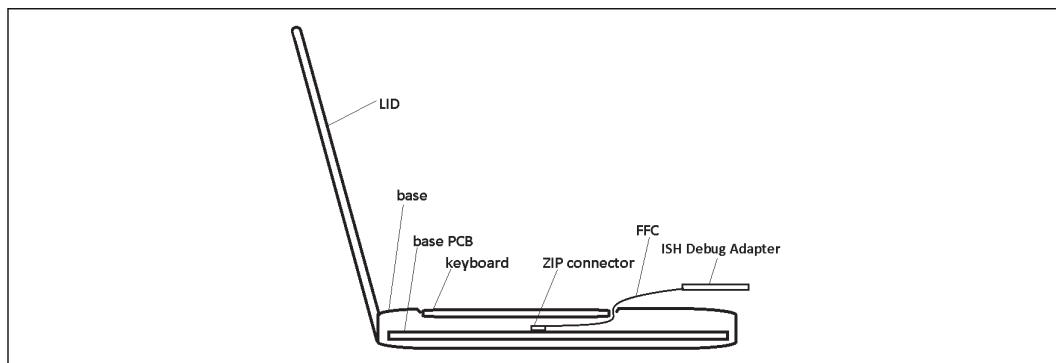
In order to access this connector with external test/debug equipment, Intel developed an adapter in the figure below. To obtain such adaptor, contact to Intel® ISH AE.

**Figure 126. Intel® ISH Debug Adapter and Ribbon Cable**

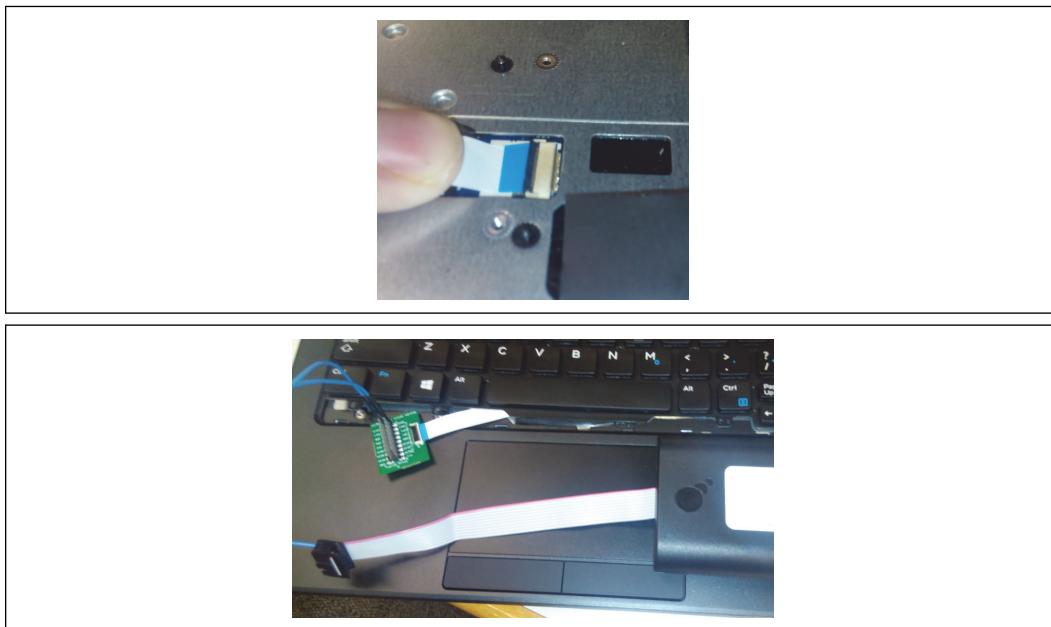


Intel recommend customer placing a small connector on the PCB. It provides all the sensor debug traces located in an easily accessible location such as under the keyboard, inside the DDR compartment, the WLAN module compartment or the SSD compartment. Please refer to the figures below.

**Figure 127. Proposed Location for ZIF Connector - Under the Keyboard**



**Figure 128. Proposed Location for ZIF Connector - Under the keyboard**



The ZIF connector is a 18-pin FPC/FFC Lower Side Contact, Side Entry, Surface Mount connector with 0.5 mm pitch, such as the 10051922-1810elf. The pinout of the ZIF connector is shown in Table below.

**Table 143. 18-pin ZIF Connector Pinout**

Pin	Pin function	Description	Pin	Pin function	Description
1	ISH_I2C0_SCL	Clock line of I2C0	10	GND	System Ground
2	ISH_I2C0_SDA	Data line of I2C0	11	ISH_I2C2_SCL	Clock line of I2C2
3	ISH_I2C1_SCL	Clock line of I2C1	12	ISH_I2C2_SDA	Data line of I2C2
4	ISH_I2C1_SDA	Data line of I2C1	13	Reserved	Reserved
5	GND	System Ground	14	Reserved	Reserved
6	GPIOa <sup>1</sup>	one pin of GPIO	15	Reserved	Reserved
7	GPIOb <sup>1</sup>	one pin of GPIO	16	Reserved	Reserved
8	GPIOc <sup>1</sup>	one pin of GPIO	17	GND	System Ground
9	GPIOd <sup>1</sup>	one pin of GPIO	18	Vio	Sensors IO Voltage

*Notes:* 1. GPIOa, GPIOb, GPIOc and GPIOd are place holders for customer designed GPIOs.  
2. It is strongly recommended that the name 'Tiger Lake IISS' be labeled on silk screen next to the ZIF connector/pads. The pin names are also recommended.

There is another option of the debug hook in high dense design. Test pads of all necessary IISS signals can be reserved on the PCB. Solder them with wires to an external 2x9 pin header for debugging.

Table below defines the pin configuration of the external 2x9 pin, 0.1" spacing header.

**Table 144. Pin Location for Dual-in-Line Connector**

Signal Name	Pin	Header	Pin	Signal Name
ISH_I2C0_SCL	1		2	ISH_I2C0_SDA
ISH_I2C1_SCL	3		4	ISH_I2C1_SDA
GND	5		6	GPIOa
GPIOb	7		8	GPIOc
GPIOd	9		10	GND
ISH_I2C2_SCL	11		12	ISH_I2C2_SDA
Reserved	13		14	Reserved
Reserved	15		16	Reserved
GND	17		18	Vio

After the Tiger Lake IISS is fully functional and fully validated on pre-production systems, the debug connector may be un-stuffed on production stage of systems. It is recommended to leave connector footprint on the PCB without being populated for future debugging.

#### NOTE

Solder the debug connector to the footprint before the system is going to be sent to Intel for IISS debug support.

## 7.3

### Discrete Trusted Platform Module

Trusted Platform Module (TPM) is a Trusted Computing Group (TCG) low cost security solution to increase confidence on system security. The TCG Website with all current specifications and revisions can be found at this link,

<https://trustedcomputinggroup.org/>.

The Trusted Platform Module (TPM) is a device that resides on the motherboard and is connected to PCH using the Serial Peripheral Interface (SPI) bus to communicate with the rest of the platform.

Today most protection against computer viruses and unauthorized intrusions consists of adding and updating software that installs outer barriers and surveillance tools. The goal of Safer Computing is to go much deeper, integrating a level of trust into the actual hardware and pre-operating system environments. Applications intended for e-business are based on trust in the communication partner and the reliability of the connection.

The objective of the TPM is to establish a baseline of platform integrity and enhance system security. TPM's are available from several integrated circuit vendors in the form of a silicon component and accompanying software. When integrated into the PC, a Trusted Platform Module provides protected storage of platform data allowing for platform-level authentication toward the goal of making data files, transactions and communication more trustworthy.

### 7.3.1 Discrete Trusted Platform Module Platform-Specific Important Information

For more information on trusted platform modules and Safer Computing, refer to the trusted computing group web site: <http://www.trustedcomputinggroup.org>.

### 7.3.2 Discrete Trusted Platform Module Signal Descriptions

**Table 145. TSSOP-28 Pin Assignments**

Signal	Pin(s)	Type	Description	SPI Pin-Assignments
PIRQ	20	BI/O	PIRQ#: SPI Interrupt, active low, open collector	M-(Mandatory)
MOSI	23	BI	MOSI: As defined in Section SPI Hardware Protocol in TPM Spec	M
MISO	26	BI		M
LPCPD#	28	I	Implementation of this pin SHALL allow for the pin to be strapped HIGH.	O-(Optional)
SPI_CLK	21	I	SPI_CLK: As defined in Section Clocking	M
SPI_CS#	22	I	SPI_CS#: As defined in SPI Interface Specification	M
LRESET#/SPI_RST#	16	I	SPI_RST#: Active Low	M
SERIRQ	27	BI	As defined in the LPC Interface Specification	O
CLKRUN#/GPIO	15	BI	Same as PCI CLKRUN#. Active Low, internal pull-down. Only needed by peripherals that need DMA or bus mastering in a system that can stop the PCI bus (generally mobile devices). Implementation of CLKRUN# is TPM and chipset vendor specific GPIO will default to low.	O
PP(GPIO	7	I, BI	Physical Presence, active high, internal pull-down. Used to indicate Physical Presence to the TPM. GPIO will default to low	O
XTALOI/32k in	13	I	32 kHz crystal input or 32 kHz clock input	O
XTALO	14	O	32 kHz crystal output	O
GPIO/SM_CLK	2	BI	Defaults as a GPIO. GPIO will default high. Also used as System Management Bus (SMB) Clock signal	O
GPIO/SM_DAT	1	BI	Defaults as a GPIO. GPIO will default high Also used as System Management Bus (SMB)Data signal.	O
GPIO-Express-00	6	BI	GPIO assigned to TPM_NV_INDEX_GPIO_00, internal pull-up	O

*continued...*

Signal	Pin(s)	Type	Description	SPI Pin-Assignments
			Open-Collector output (when configured as output).	
VNC	3		Vendor-controlled No Connect. This pin will be defined by the TPM vendor or can be a GPIO. There is no defined default state for this signal.	O
TESTI	8	I	This pin will be pulled low on the motherboard. Pull high to enable Test mode. Pull low to disable Test mode and enable GPIO/BADD on pin 9(TESTBI).	O
TESTBI/BADD/GPIO	9	8	TESTBI: Test port. Internal pull-up If TESTI is pulled low, TESTBI acts as a GPIO and (optionally) BADD. GPIO will default high. BADD (optional, defaults high, use external pull-down to signal "low") can be used to select the legacy I/O base address. This logic is manufacturer specific, as well as the selected addresses. Setting is read at Startup.	O
<b>POWER</b>				
VDD			This is either a 3.3 volt or 1.8V DC power rail supplied by the motherboard to the module. The maximum power for this interface is 250 mA. Available from S0-S2.	M
GND	4, 11, 18, 25	I	Zero volts. Expected to be connected to main motherboard ground.	M
VBAT	12	I	Battery input, may be 3.3V. Available from S0-S5 and in G3 state.	O
VSB	5	I	Standby DC power rail, may be 3.3V or 1.8V. Available from S0-S5.	O

**Table 146. QFN-32 Pin Assignments**

Signal	Pin(s)	Type	Description	SPI Pin-Assignments
SPI_PIRQ#	18	BI/O	PIRQ#: SPI Interrupt, active low, open collector	M
SPI_CLK	19	I	SPI_CLK:	M
SPI_CS#	20	I	SPI_CS#:	M
SPI_RST#	17	I	SPI_RST#: Active Low	M
GPIO	3, 4	BI	GPIO defaults to low.	O
VNC/GPIO	6, 13, 29, 30	I,BI	Vendor defined no-connect.	
GPIO will default to low	O			
MOSI	21	BI	MOSI - As defined in Section 6.4 SPI Hardware Protocol	M

*continued...*

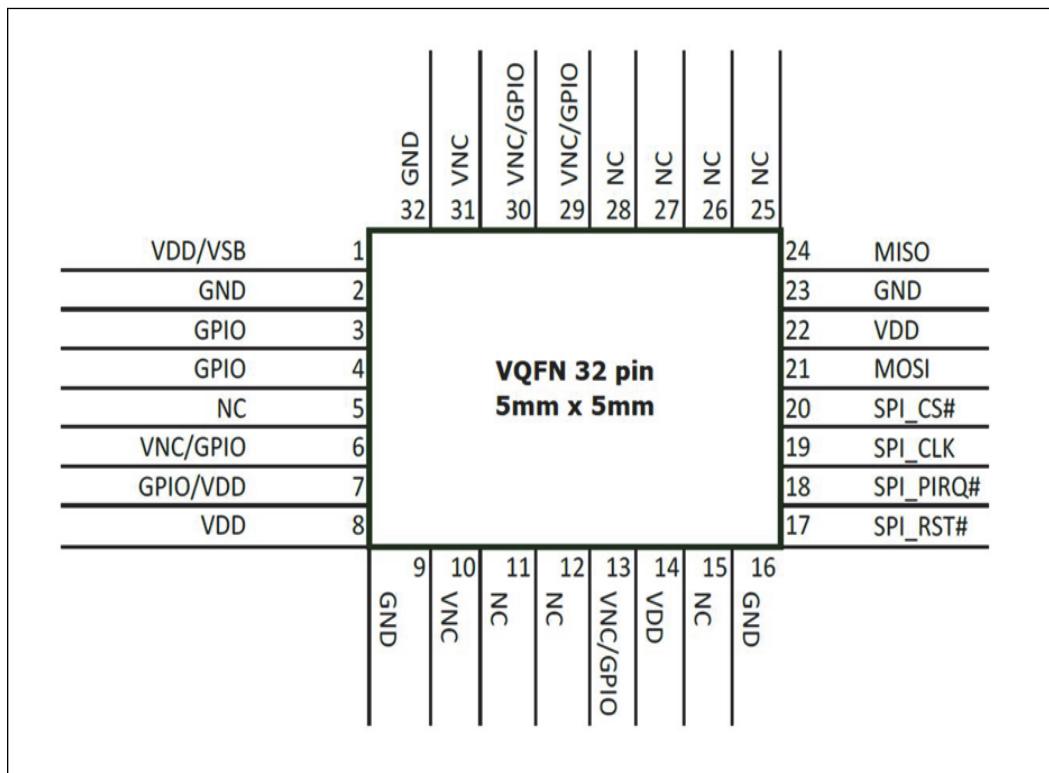
<b>Signal</b>	<b>Pin(s)</b>	<b>Type</b>	<b>Description</b>	<b>SPI Pin-Assignments</b>
MISO	24	BI	MISO -	M
VNC	10, 31		Vendor-controlled No Connect. This pin will be defined by the TPM vendor or can be a GPIO. There is no defined default state for this signal.	O
Power				
VDD	14 22	I	This is either a 3.3 volt or 1.8 volt DC power rail supplied by the motherboard to the module. The maximum power for this interface is 250 mA. Available from S0-S2.	M
VDD/VSB	1	I	This is either a 3.3 volt or 1.8 volt DC power rail supplied by the motherboard to the module. The maximum power for this interface is 250 mA. Available from S0-S2. If defined as VSB, this is a 3.3V supply.	M
GND	2, 9, 16, 23, 32	I	Zero volts. Expected to be connected to main motherboard ground.	M
NC	5, 11, 12, 15, 25, 26, 27, 28		No connect	O
GPIO/Power	7	I	GPIO defaults to low, e.g. Physical Presence	
Power is vendor defined	O			

### 7.3.3 Discrete Trusted Platform Module Topology Guidelines

Figure 129. TPM Combo TSSOP-28 Pin out

GPIO/SM_DAT	1	28	LPCPD#
GPIO/SM_CLK	2	27	SIRQ
VNC	3	26	LAD0/MISO
GND	4	25	GND
VSB	5	24	VDD
GPIO-Express-00	6	23	LAD1/MOSI
PP/GPIO	7	22	LFRAME#/SPI_CS#
TestI	8	21	LCLK/SPI_CLK
TestBI/BADD(GPIO	9	20	LAD2/PIRQ#
VDD	10	19	VDD
GND	11	18	GND
VBAT	12	17	LAD3
xtalI/32k in	13	16	LRESET#/SPI_RST#
xtalO	14	15	CLKRUN#/GPIO

**Figure 130. TPM SPI VQFN-32 Pin out**



#### 7.3.4

#### Discrete Trusted Platform Module Component Selection Guidelines

The TPM in the PC Client platform serves as the Root of Trust. As such, the hardware implementation of the TPM on the motherboard has to account for how the TPM is connected to the other components of the platform which form the trust chain, such as the CPU. It is important that the TPM reset, clock and power signals support the TPM's function as the RTM and RTR and cannot be easily circumvented. Motherboard manufacturers should take care to ensure that the physical connections and routing

- The \_TPM\_INIT (LRESET#/SPI\_RST#) signal SHALL be connected to the platform CPU Reset signal such that it complies with the requirements, specified in Section 1.2.7 of the TPM Profile (PTP) Specification available on TCG website, [HOST Platform Reset](#) in the PC Client Implementation Specification for Conventional BIOS.
- The TPM's main power pins (VDD) SHALL be connected such that the TPM is powered during ACPI states S0-S2 and MAY be powered in S3-S5.
- If a TPM implements the optional VBAT and/or VSB pins, the pins MAY be connected to a battery or auxiliary power source. The motherboard manufacturer SHOULD consult their TPM documentation.

#### Software Interface to SPI-TPM

This section provides guidelines for platform OEM's and ISV's to aid in design of platforms and software using an SPI TPM. The following sections are informative only, as they describe recommended behavior.

The SPI interface has been architected to be transparent to the driver and application layers in a TPM-enabled software stack. There are some SPI properties which will produce different results than LPC in cases where software does not follow good design practice. In these cases, this specification addresses the TPM requirements so that none of the TPM's security is impacted by bad software design, at the risk of a potentially poor user experience. As such, software and drivers should follow these recommendations to ensure a robust implementation.

- SW should continue to use the memory mapped 0xFED4\_xxxx address range to access the SPI-TPM

### 7.3.5 Debug Guidelines/Recommendations

#### Discrete Trusted Platform Module (TPM) Design Considerations

This design guide defines a new software interface to the TPM for TPM 2.0, in addition to the FIFO interface. This interface, the Command Response Buffer Interface, has been defined so that it may be implemented in a TPM which also contains a FIFO interface. The Command Response Buffer (CRB) Interface is intended to be physical-bus agnostic, so that it could be implemented on a SPI interface, as specified in this specification or on another physical interface not specified. In order for a TPM to be compliant with this specification, however, it is required to implement at least one of the interfaces is defined.

Refer to the TPM vendor documentation for additional TPM specific design considerations.

## 7.4 Clover Falls Introduction

Clover Falls (CVF) is a discrete ASIC that provides ultra-low-power [ULP] privacy-protected computer vision capabilities targeting Intel's next-gen mobile platforms, as a part of larger Project Athena effort (<https://newsroom.intel.com/tag/project-athena/>).

CVF is intended to be placed in line between a compatible Intel CPU such as a TGL SoC with Intel IPU Enabled, and a MIPI CSI-2 imaging sensor. It offers robust ULP Vision facilities without the need for an additional sensor with provisions to seamlessly share a user-facing camera with the OS and applications.

The ASIC includes a Privacy and Security Engine [PSE] that gives end-users (and/or IT) full visibility and control of the user-facing camera, while ensuring imaging data that cannot be compromised, while operating in ULP Vision mode. Hardened indicators and controls ensure the current state of imaging pipeline selector - Normal, ULP Vision or Privacy Mode - is always properly reflected by LED indicators.

Following are brief discussions on features, modes of operation and key usages. Further information about CVF, including system design considerations, is available in the document 613151 - *Clover Falls Datasheet*

### 7.4.1 Features

#### Physical and Electrical Properties

- Power Supplies: 0.9 V @ <500 mA and 1.8 V @ <200 mA
- Operating Temperature Range: -0° to 70°C

- Package: Wafer-Level Chip Scale Package @ {X= $\leq$ 6.0 mm, Y= $\leq$ 3.0 mm, Z= $\leq$ 0.6 mm}

#### **Ultra-Low-Power ULP Vision Accelerator**

- Multi-task Cascaded Convolutional Networks (MTCNN) engine.
- Built-in models for Face, Head Orientation and Multi-face detection.
- Detection Range: ~0.3 m up to 2 m.
- Power: Optimized for ultra-low-power operation with  $\leq$ 15 mW typical CVF power and  $\leq$ 20 mW solution power, when paired with a ULP imaging sensor.

#### **Seamless sharing of a MIPI CSI-2 User-Facing Camera**

- MIPI CSI-2 DPHY v2: Up to four lanes at 1.5 Gbps/lane.
  - x1 lane configuration during ULP Vision mode (lowest power).
  - x1, x2 and x4 lane configures supported during pass-through (to the IPU).
- MIPI CSI-2 Repeater with Spread Spectrum Clocking [SSC] support
  - MIPI CSI-2 Rx: Ability to receive a SSC embedded clock from an upstream imaging sensor.
  - MIPI CSI-2 Tx: Ability to drive a SSC embedded clock out of CVF's CSI-2 DPHY to the host; ideally suited when CVF is located on the lid.

---

#### **NOTE**

Spread Spectrum Clocking (SSC) mitigates EMI issues and reduces peak emission considerably (~6-8 dB) and reduces cable and connector cost.

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#### **Secure, Privacy-Protected Operation**

- Hardened Privacy Indicators and Controls
- Secure Firmware Load
- Secure Debug

### **7.4.2 Modes of Operation**

CVF supports four modes of operation:

- Privacy Mode where the MIPI-DPHY is physical disconnected (cut-off), such that no agent can access the user-facing camera without the end-user (or IT) disabling Privacy Mode.
- Pass-Thru Mode where imaging data is passed through the MIPI DPHY mux/selector to the Image Processing Unit [IPU] in the CPU and on to software (Example: Skype\*, Google\* Hangouts).
- ULP Vision Mode for ultra-low-power face, head orientation, and multi-face detection. In this mode imaging sensor data path is connected to CVF's Audio and Contextual Engine [ACE].
- Off (D3) which occurs, whenever the lid is closed (clamshell designs), the system transitions to S5, etc. During D3 CVF resides in a reset/off state and have no FW loaded.

Transitions to Privacy Mode are initiated by the end user (or IT) by asserting one of CVF's Privacy Switch inputs. Logic within CVF ensures a graceful termination of the image data stream, when the Privacy Switch is asserted during an active stream (Example: Midstream within a video call). De-assertion of the Privacy Switch causes CVF to resume ULP Vision Mode.

Transitions to Pass-Thru Mode are initiated, whenever any software entity activates the user-facing camera (Example: End-user launches a video call). The OS's Camera Driver and Clover Falls Driver coordinate the handoff (D3 > D0). Likewise, the user-facing camera transitions to D3 and CVF resumes ULP Vision Mode, when software no longer requires the camera.

### 7.4.3 Key Usages

CVF is intended to facilitate the following five key usages.

- **Camera Privacy:** End-user ability to securely disconnect the user-facing camera's MIPI DPHY connection plus hardened indicators to clearly articulate the state of the camera, which can be used independently or in conjunction with a physical camera shutter.
- **Adaptive Dimming:** Progressively dim the backlight, when user has disengaged and quickly turn off the display, when the user is no longer present.
- **Wake on Face:** Wake the system from S0ix, as the user approaches the system and their face comes into view - without touching a key or moving the mouse. Intended for S0ix lid open / display off scenarios to streamline OS-based face authentication.

---

#### NOTE

Unlike time-of-flight or other motion sensors, CVF only wakes the system, when a human face is present and engaged (at up to 2 meters) to minimize spurious wake events.

- **Lock on Absence:** Lock the system, once the user leaves after powering down the embedded panel (Adaptive Dimming).
- **No Lock on Presence:** Keep the display ON by overriding the OS inactivity timeout, when the user is present and engaged. Example: Reading a document or watching a video.

CVF is also be able to detect and report, when Multiple Faces exist in the field of view. Example: To potentially automate a privacy filter, when the primary user is viewing confidential information.

Several additional usages are currently being explored that leverage CVF's highly-accurate human presence and attentiveness understanding:

- System Responsiveness (Example: Escalate performance bias, when engaged).
- CPU Power and Performance (Example: Only Turbo, when engaged).
- Web Browser Auto-Pause (Example: Stop animation and videos, when disengaged).
- Panel Adaptive Sync and Render Optimizations (Example: Dynamic throttling for non-browser applications).

- OS Background Task Scheduling (Example: Pause, when engaged / run when disengaged).
- Advanced Fan Control (Example: Shift to passive cooling @ lower power limit, when not present).

## 8.0 Platform Connectivity

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### 8.1 Intel® Ethernet 1G LAN Design Considerations and Guidelines

The PCH incorporates an integrated 10/100/1000 Mb/s Media Access Controller (MAC) that can be used with an external Intel® Ethernet Connection I219 Physical Layer Transceiver (PHY). Its bus master capabilities enables the component to process high-level commands and perform multiple operations. This can decrease processor use by off loading communication tasks from the processor.

For specific design and implementation information about the I219 Physical Layer Transceiver (PHY), refer the following reference documents.

**Table 147. LAN Design Reference Documents**

Document	Document Number
Intel® Ethernet Connection I219 Series (Jacksonville)- All Collateral	<a href="https://www.intel.com/content/www/us/en/design/products-and-solutions/networking-and-io/ethernet-connection-i219/technical-library.html?wapkw=i219&amp;grouping=rdc%20Content%20Types">https://www.intel.com/content/www/us/en/design/products-and-solutions/networking-and-io/ethernet-connection-i219/technical-library.html?wapkw=i219&amp;grouping=rdc%20Content%20Types</a>
Intel® Client Ethernet Message of the Week	574707
Intel® Ethernet Connection I219 Datasheet	544486
Intel® Ethernet Connection I219 Reference Schematic	544767
Intel® Ethernet Connection I219 Design Checklist	544506
Intel® Ethernet Connection I218/ I219 Specification Update	571189
Intel® Ethernet Connection I219LM Dear Customer Letter	549358
Intel® Ethernet Connection I219V Dear Customer Letter	558301
Intel® Ethernet Connection I219 Fast Startup Wake-on-LAN Guidance	554465
Intel® Ethernet Connection I219 PXE Software (UEFI and Legacy)	574961
Intel® Ethernet Connection I219 Skylake Production GbE NVM	573993
Intel® Ethernet Connection I219 Kaby Lake Production GbE NVM	574056
Intel® Ethernet Connection I219 Purley & Whitley Production GbE NVM	574055
Intel® Ethernet Connection I219 Whiskey Lake Production GbE NVM	605898

*continued...*

Document	Document Number
Intel® Ethernet Connection I219 Ice Lake Production GbE NVM	613088
Intel® Ethernet Connection I219 Modern Standby PRD	600935
Networking Division Ethernet CNDA Roadmap	564924
Intel® Networking Division - Product Lifecycle Guidance	499897
Intel® Ethernet Network Connections - LAN Tools Guide	489650
Intel® Network Connections Tools	348742
Intel® Network Connections Tools (DOS only)	348743

## 8.2

## Intel® Ethernet 2.5G LAN Design Considerations and Guidelines

This section provides guidelines for connecting interfaces, using special pins, selecting components, and layout guidance. Unused interfaces should be terminated with pull-up or pull-down resistors. There is one reserved pin (pin #8), which should pull-down with 0 Ohm resistor. Please check the I225 collateral package or ask your Intel representative if there is question about schematic or layout designs.

**Table 148. LAN Design Reference Documents**

Document	Document Number
Intel® Ethernet Controller I225 (Foxville) - All Collateral	<a href="https://www.intel.com/content/www/us/en/design/products-and-solutions/networking-and-io/ethernet-controller-i225/technical-library.html?wapkw=i225&amp;grouping=rdc%20Content%20Types">https://www.intel.com/content/www/us/en/design/products-and-solutions/networking-and-io/ethernet-controller-i225/technical-library.html?wapkw=i225&amp;grouping=rdc%20Content%20Types</a>
Intel® Ethernet Controller I225 Datasheet	596659
Intel® Client Ethernet Message of the Week	574707
Intel® Ethernet Controller I225 Reference Schematic	576602
Intel® Ethernet Controller I225 Cadence Symbol Files	576601
Intel® Ethernet Controller I225 Frequently Asked Questions	574703
Intel® Ethernet Controller I225 Design Checklist	576704
Intel® Ethernet Controller I225 Design Considerations	607353
Intel® Ethernet Controller I225 - Dear Customer Letter (DCL) - ES2	613747
Intel® Ethernet Controller I225 Boundary Scan Description Language (BSDL)	613949
Intel® Ethernet Controller I225 Specification Update (External)	615084
Intel® Ethernet Controller I225 NVM	615202
Intel® Ethernet Controller I225 PXE Software (UEFI and Legacy)	615203

*continued...*

Document	Document Number
Intel® Ethernet Controller I225 Technical Highlight	615204
Intel® Ethernet Controller I225 LAN Tools	615722
Intel® Ethernet Controller I225V PRQ NVM	616655

## 8.2.1 Connecting PCIe Interface

The I225 connects to the host system using a PCIe interface. The lane has to be AC-coupled between its corresponding transmitter and receiver, with the AC-coupling capacitor located close to the transmitter side (within 1 inch). Each end of the link is terminated on the die into nominal 100 differential DC impedance. Board termination is not required.

The I225 supports the PCIe Gen 2, v3.1 interface. Refer to PCI Express\* Card Electro mechanical Specification, rev2.0 and the PCI Express\* Gen2 Specification, ver3.1.

### Link Width Configuration

The I225 is a MAC/PHY PCIe device that supports link width x1. During link configuration, the platform and the I225 negotiates on a common link width. The link width result must be x1.

### Polarity Inversion and Lane Reversal

To ease routing, designers have the flexibility to the lane reversal modes supported by the I225. During the link training sequence, the polarity inversion of differential pair is detected and automatically corrected.

### PCIe Reference Clock

The I225 requires a 100 MHz differential reference clock called PE\_CLK\_p and PE\_CLK\_n. This signal is typically generated from a Peripheral Controller Hub (PCH) and provides it to the I225. For Network Interface Cards (NICs), the clock is furnished at the PCIe connector and the signal must be routed to the PCIe connector.

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#### NOTE

The frequency tolerance for the PCIe reference clock is  $\pm 300$  ppm.

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### PCIe Bias Resistor

For proper biasing of the PCIe analog interface, a  $200\ \Omega$  1% pull-down resistor must be connected between the RBIAS (pin #20) pin and ground in order to calibrate the PCIe analog modules. To avoid noise coupled onto this reference signal, place the bias resistor close to the I225 and keep traces as short as possible. Do not change this resistor value.

### Miscellaneous PCIe Signals

The I225 signals power management events to the system by pulling low the PE\_WAKE\_N signal. This signal operates like the LAN WAKE signal. Note that somewhere in the system, this signal has to be pulled high to the auxiliary 3.3 V supply rail.

The PE\_RST# signal, which serves as the familiar reset function for the I225, needs to be connected to the host system's corresponding signal.

### PCIe Layout Recommendations

For information regarding the PCIe signal routing, refer to the Intel PCIe Design Guide.

## 8.2.2 Connecting 2.5GBASE-T MDI Interfaces

The MDI line interface on the I225 is capable of driving up to +100 meters of CAT-5E or CAT-6 unshielded twisted pair ( $100\ \Omega$  differential impedance) on 10 Mb/s, 100 Mb/s, 1 GbE, or 2.5 GbE. It is designed to drive this via a quad,  $50\ \Omega$  center tapped 1:1 transformer connected to an RJ-45 PCBmount jack. Solutions that combine the transformer and RJ-45 jack into a single device are also supported.

The MDI line interface on the I225 supports automatic A/B and C/D pair swaps and inversions (MDI-X). It also supports provisioned ABCD to DCBA pair reversal (called the MDI Lane Swap feature) for ease of routing via a hardware strap. Please see the MDI Lane Swap Configuration Feature section for details.

### PHY Calibration Resistor

For proper biasing of the MDI analog interface, a  $22\ K\Omega$  1% pull-down resistor must be connected between the RCAL pin (pin#42) and ground in order to calibrate the I225 MDI analog front-end. To avoid noise coupled onto this reference signal, place the calibration resistor close to the I225 and keep traces as short as possible. Do not change this resistor value.

### MDI Circuit Guidelines

The MDI discrete design and integrated magnetic components were chosen for inclusion in the reference design and Bill of Material (BOM). These components are capable of delivering the performance required for this demanding application.

For systems with enhanced ESD performance requirements, the additional enhanced ESD parts might be needed. Consult with the ESD part vendors for their latest technology and technique. Also consult with Intel representative for the schematic and layout implementation.

### MDI Layout Guidance

The magnetics can be implemented either as a discrete module or an integrated solution combining the magnetics and the RJ-45 jack.

For the discrete magnetics, the I225 designs consist of an RJ-45 jack, Bob Smith termination and discrete magnetics all separated parts (refer Figure below).

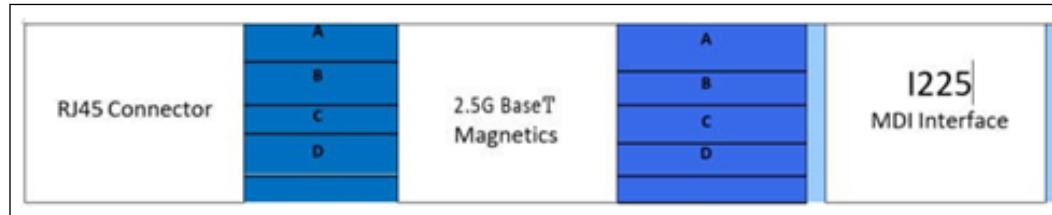
For the integrated magnetics, the I225 designs is simple. The RJ-45 connector has Bob Smith termination and discrete magnetics integrated inside (refer [Figure 135](#) on page 253).

Minimizing the amount of space needed for the PHY is important because other interfaces compete for physical space on the LAN on Motherboard (LOM) near the connector. The PHY circuits need to be as close as possible to the connector.

Figure below illustrates some basic placement distance guidelines. It shows four differential pairs and the layout can be generalized for a 2.5 GbE system with four analog pairs. The ideal placement for the I225 is approximately two inches behind the magnetics module for both the discrete and integrated solutions.

- **Discrete Magnetics**

**Figure 131. Discrete Magnetics**

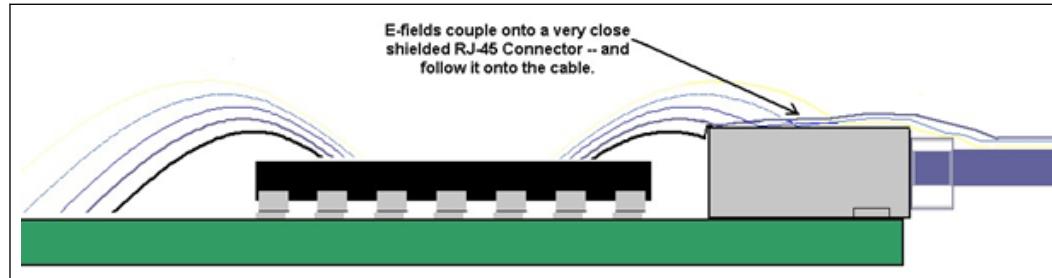


The I225 impedance of the Bob Smith termination is  $75 \Omega$  Channel A, B, C and D, whereas the PHY input impedance is  $100 \Omega$ .

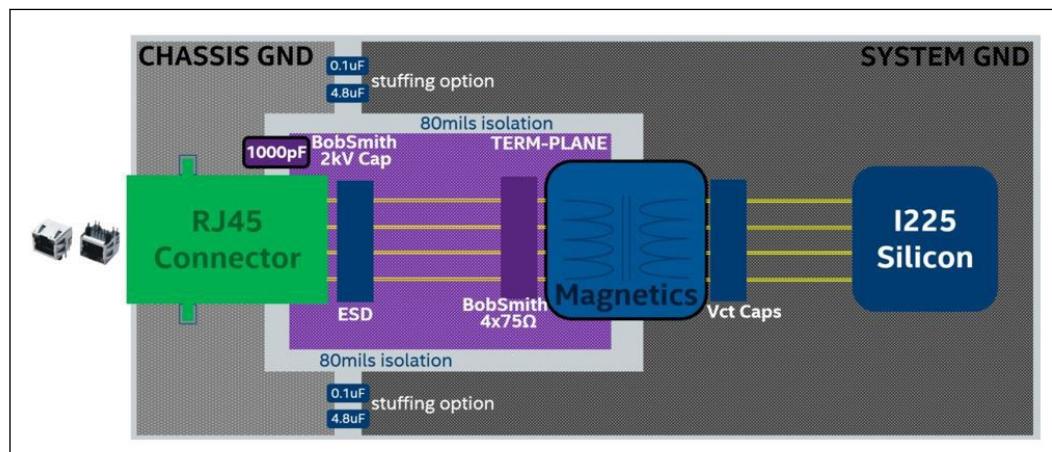
The I225, referred as a LAN silicon in Figure 1-2 and Figure 1-3, must be at least 1.5 inches from the I/O back panel. To help reduce EMI, the following recommendations should be followed:

- Minimize the length of the MDI interface
- Place the MDI traces no closer than 0.5 inch (1.3 cm) from the board edge.

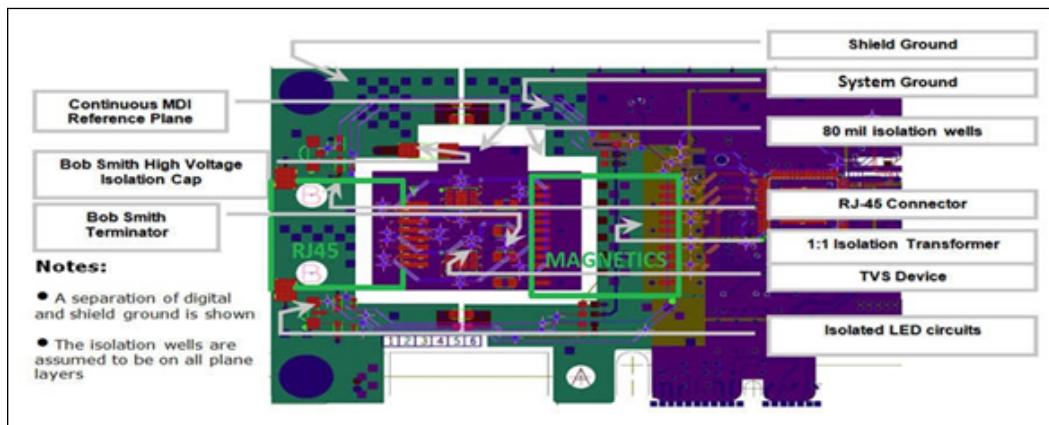
**Figure 132. Device Placed Less Than One Inch from the RJ-45 Connector**



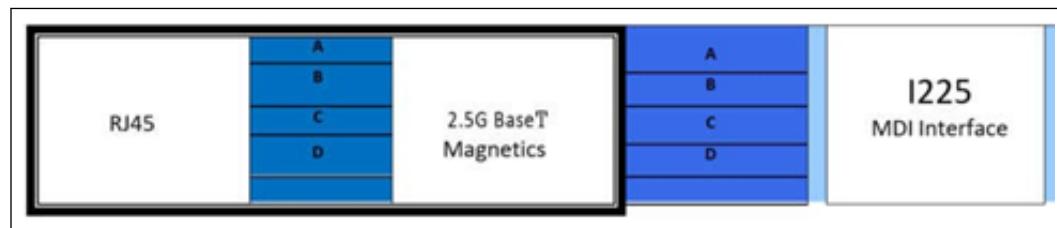
**Figure 133. Discrete Magnetic Connector Layout Topology**



**Figure 134. Discrete Magnetic Layout Example**

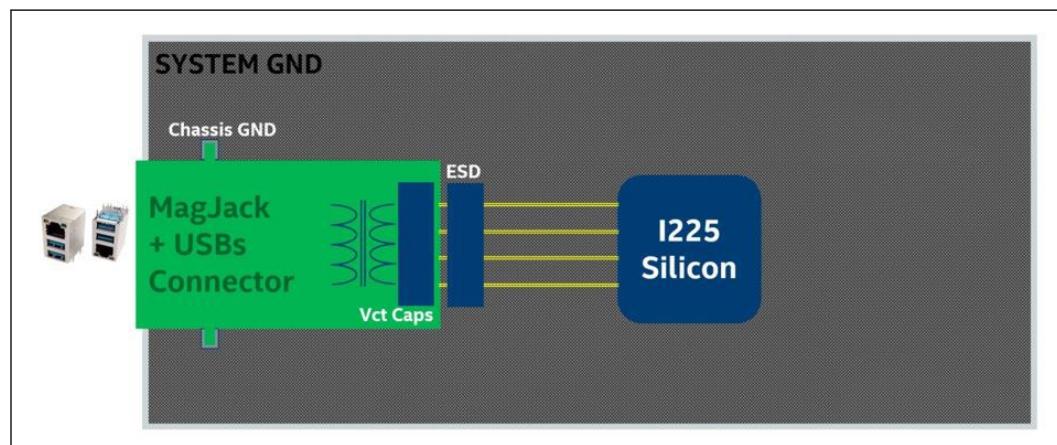


- The ground is split underneath the magnetics, with the MDI Reference Plane GND (the purple island) being present under the front-end (Figure above), and the circuit system ground under the I225 side of the magnetics. The MDI traces on the line side are referenced to the MDI reference plane. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.
- Between the RJ45 connector and the magnetics device, the MDI Reference Plane GND (the purple island) can be voided. When using this voiding technique, this MDI segment (cable side of the magnetics) will have no reference plane. Please make sure using the trace width/separation to target 100-ohm differential impedance. The MDI segment on the silicon side of the magnetics still references to the system ground.
- The Bob Smith termination (4x 75 Ω) to be implemented from the line side transformer center taps to the reference plane.
- Bob Smith termination and the shield of the RJ-45 jack are both connected to chassis ground, which are the two large circular metallization in the MDI (refer [Figure 135](#) on page 253).
- The resistors in the Bob Smith termination are required to be 0805's to handle the cable discharge voltages.
- Similarly, the magnetics should be placed as close as possible to the RJ-45 jack.
- In [Figure 134](#) on page 252, the Hi-POT clearance for cable discharge is shown and designed with ≥2.032 mm of clearance from the ground. Therefore, the MDI reference plan has 2.032 mm clearance away from any other signals (including shield ground and system ground). Note that the breakdown voltage in FR4 is lowest in the x-y axes planar to the PCB and highest in the z-axis between layers.
- The MDI reference plane is coupling to the shield ground via the Bob Smith high voltage isolation capacitor. This helps ESD performance.
- The shield ground can be coupled to the system ground via 2-4 small value capacitors. Spread and distribute these capacitors out. The capacitor value can be tuned for improving the EMI performance.
- **Integrated Magnetics**

**Figure 135. Integrated Magnetic**

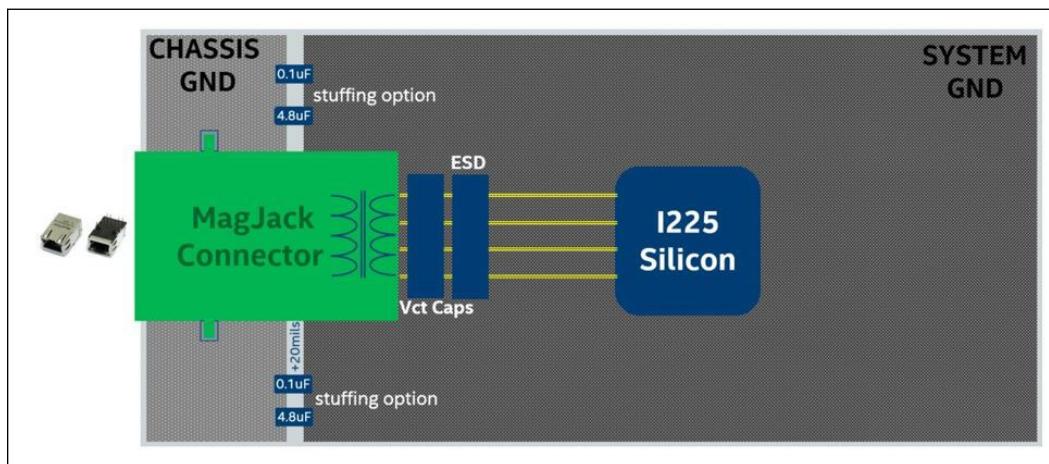
At high level, the guidance on MDI trace implementation between the I225 and the integrated module remains the same as with discrete magnetics, including length requirements and target impedance.

However, the RJ45 connector has the magnetics and the Bob Smith termination network integrated inside. Therefore, no need to take care the high-voltage isolation routing. Do not split the connector shield ground with the system ground. Just connect the RJ45 shield ground directly to the system ground.

**Figure 136. Integrated Magnetic/USB Connector Layout Topology**

The MagJack/ICM integrated magnetics connector can have the slit Ground implementation for the EMI improvement. The stuffing cap values can be adjusted to gain 1-2dBs

**Figure 137. Integrated Magnetic Connector Layout Topology with Ground Slit for EMI Improvement**



- **MDI Differential Pair Trace Routing for LAN Design**

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

- **Signal Trace Geometry**

One of the key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the reference plane. To minimize trace inductance, high-speed signals and signal layers that are close to a reference or power plane should be as short and wide as practical. Ideally, the trace-width to trace-height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the neighboring planes.

Each pair of signals should target a differential impedance of  $100 \Omega \pm 15\%$ .

A set of trace length calculation tools are made available from Intel to aid with MDI topology design. Contact your Intel representative for tool availability.

When designing a board layout, the automatic router feature of the CAD tool must not route the differential pairs without intervention. In most cases, the differential pairs require manual routing.

---

#### NOTE

Measuring trace impedance for layout designs targeting  $100 \Omega$  often results in lower actual impedance due to over-etching. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of  $105 \Omega$  to  $110 \Omega$  should compensate for over-etching.

- **Matching Traces within a Pair (P and N)**

P and N for each MDI pair should be matched to within 0.127 mm on the PCB to prevent common-to-differential and differential-to-common conversion due to the length mismatch.

If in-pair length matching is not possible using bends or small loops, serpentine routing (zig-zag of a shorter trace) is acceptable if only one to three meanders are routed within 5.08 mm of the source of the skew or the end(s) of any otherwise unmatched lengths of a differential trace segment. For example, near device pins and/or at or near the connector pins and possibly at differential signal vias. Refer to the Intel® Ethernet Controller I225 Checklists for more details.

**Table 149. MDI Routing Summary**

Parameter	Main Route Guidelines	Breakout Guidelines <sup>1</sup>	Notes
Signal group	MDI_P[3:0] MDI_N[3:0]		
Microstrip*/Stripline* uncoupled single-ended impedance specification	50 ±10%		
Microstrip/Stripline uncoupled differential impedance specification	100 ±15%		2 , 3
Microstrip nominal trace width	Design dependent	Design dependent	
Microstrip nominal trace space	Design dependent	Design dependent	3
Microstrip/Stripline trace length	< 4 inches		
Microstrip/Stripline pair-to-pair space (edge-to-edge)	7 times the dielectric thickness		
Microstrip/Stripline bus-to-bus spacing	7 times the dielectric thickness		
Matching traces within a pair (P and N)	< 0.127 mm		
Keep pair-to-pair length differences	< 2 inches		
<p>Notes:</p> <ol style="list-style-type: none"> <li>1. Pair-to-pair spacing 7 times the dielectric thickness for a maximum distance of 12.7 mm from the pin. The phase tolerance between MDI_P and MDI_N is &lt;0.127 mm.</li> <li>2. Board designers should ideally target 100 ohms ±10%. If it's not feasible (due to board stackup) it is recommended that board designers use a 95ohms±10% target differential impedance for MDI with the expectation that the center of the impedance is always targeted at 95ohms. The ±10% tolerance is provided to allow for board manufacturing process variations and not lower target impedances. The minimum value of impedance cannot be lower than 90 Ohms.</li> <li>3. Simulation shows 80 differential trace impedances degrade MDI return loss measurements by approximately 1 dB from that of 90 Ohms.</li> </ol>			

**Table 150. Maximum Trace Lengths Based on Trace Geometry and Board Stackup**

Dielectric Thickness (um)	Dielectric Constant (DK) at 1 MHz	Width / Space/ Width (um)	Pair-to-Pair Space (um)	Nominal Impedance (ohms)	Impedance Tolerance (+/-%)	Maximum Trace Length (inches) <sup>1</sup>
68.58	4.05	101.6/254/101.6	482.6	95 <sup>2</sup>	17 <sup>2</sup>	3.5
68.58	4.05	101.6/254/101.6	482.6	95 <sup>2</sup>	15 <sup>2</sup>	4

*continued...*

Dielectric Thickness (um)	Dielectric Constant (DK) at 1 MHz	Width / Space/ Width (um)	Pair-to-Pair Space (um)	Nominal Impedance (ohms)	Impedance Tolerance (+/- %)	Maximum Trace Length (inches) <sup>1</sup>
68.58	4.05	101.6/254/101.6	482.6	95	10	5
83.82	4.1	106.68 / 228.6 / 106.68	584.2	100 <sup>2</sup>	17 <sup>2</sup>	4

*Notes:* 1. Longer MDI trace lengths can be achievable, but might make it more difficult to achieve IEEE conformance. Simulations have shown deviations are possible if traces are kept short. Longer traces are possible; use cost considerations and stack-up tolerance for differential pairs to determine length requirements.  
2. Deviations from 100 □ nominal and/or tolerances greater than 15% decrease the maximum length for IEEE conformance.

### NOTE

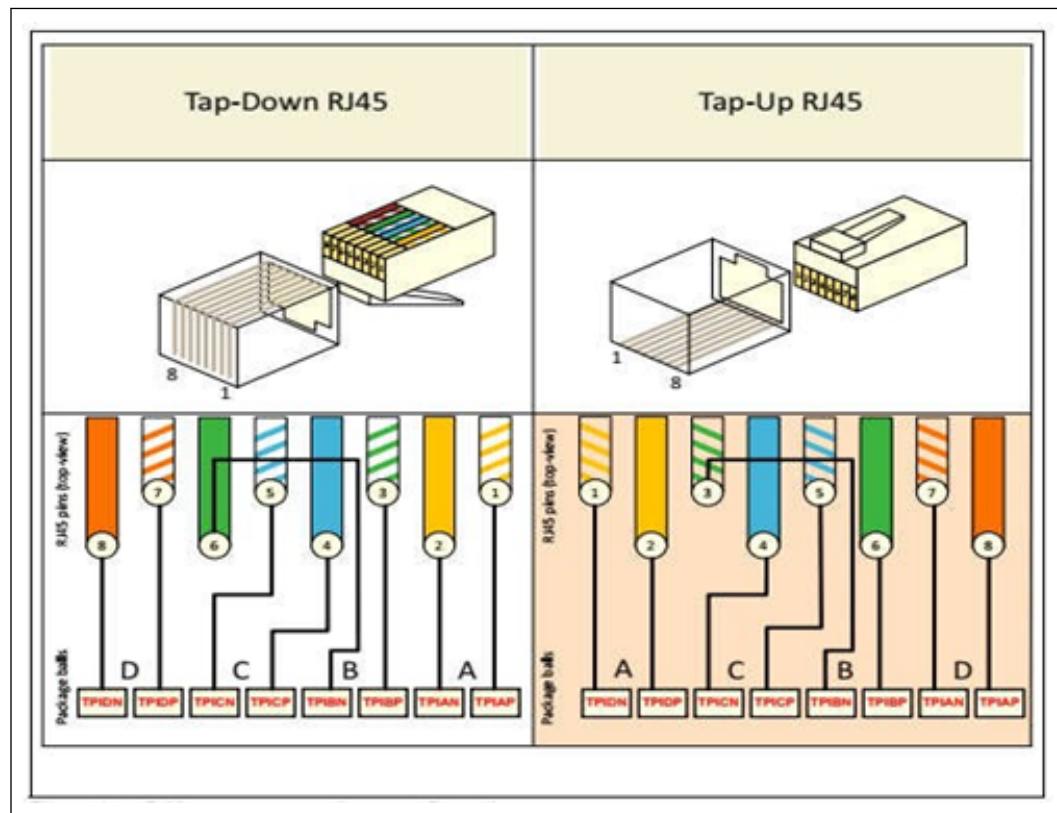
Use the MDI differential trace calculator to determine the maximum MDI trace length for your trace geometry and board stackup. Contact your Intel representative for access.

The following factors can limit the maximum MDI differential trace lengths for IEEE conformance:

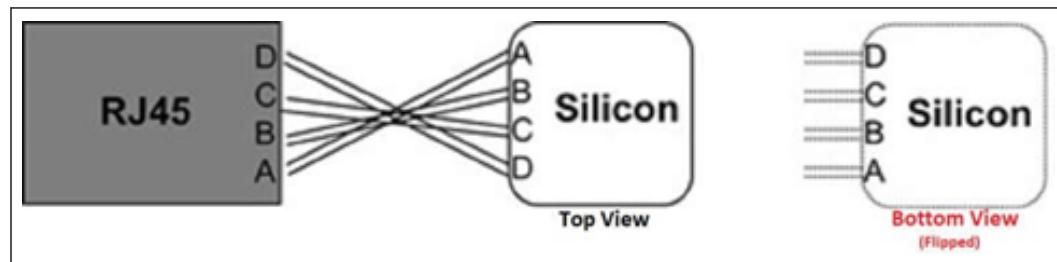
- Dielectric thickness
- Dielectric constant
- Nominal differential trace impedance
- Trace impedance tolerance
- Copper trace losses
- Additional devices, such as switches, in the MDI path might impact IEEE conformance. Board geometry should also be factored in when setting trace length.

### PHY MDI Lane Swap Configuration

In general, the RJ45 connector on the system PCB can have two different structures with the tap up or the tap down as shown in Figure below. The difference between tap-up and tap-down is a swap of positioning ABCD and DCBA orders. The I225 pin#18 strapping allows system designers to perform the MDI lane swap configuration. As a result, a PCB layout can avoid the crossing routing problem.

**Figure 138. MDI Lane Swap Configuration**

**MDI Crossing Issue:** When selecting RJ45 connectors, the RJ45 MDI lanes order might not line up with the Silicon MDI lanes order. This causes the MDI crossing routing problem in layout.

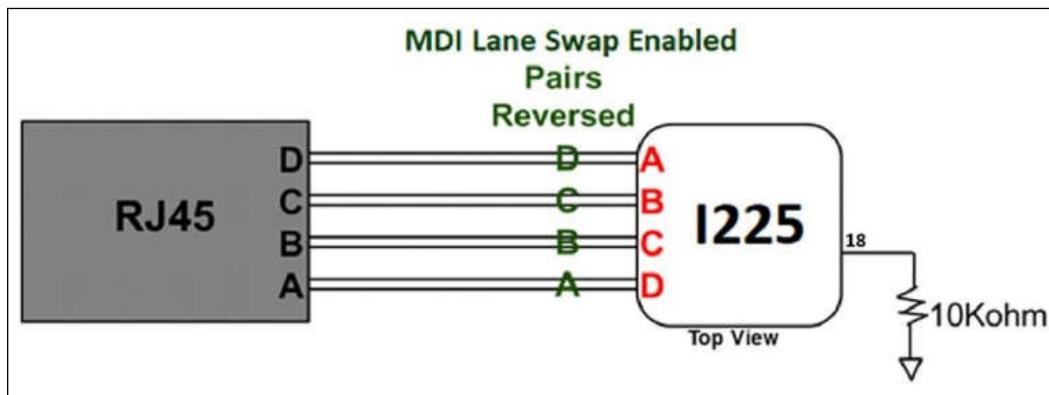
**Figure 139. Crossing Routing Issue Between RJ45 and Silicon**

**Silicon:** Pin#18 allows the MDI lane swap configuration. This is a hardware strap.

**Default Configuration (Unstrap):** Pin#18 has its internal pull-up resistor. The pin can leave unconnected.

**MDI Swap Configuration (Strapped):** Pin#18 needs a 10 K ohms pull-down. This hardware strap activates the MDI lane swap feature. ABCD order are reversed.

**Figure 140. MDI Lane Swap Enabled by Strapping**



#### Center Tap Connection Via Capacitors to Ground

The I225 has a voltage-mode driver. Therefore, it is required that a center tap be decoupled to ground via capacitors.

When using an integrated magnetic, a  $0.1\ \mu F$  capacitor should be connected from each center tap pin to ground. Most of integrated magnetic connector will have  $4 \times 0.1\ \mu F$  capacitor inside. Therefore, the I225 does not need any external capacitor. Please add  $1 \times 0.1\ \mu F$  capacitor (empty) as a place holder.

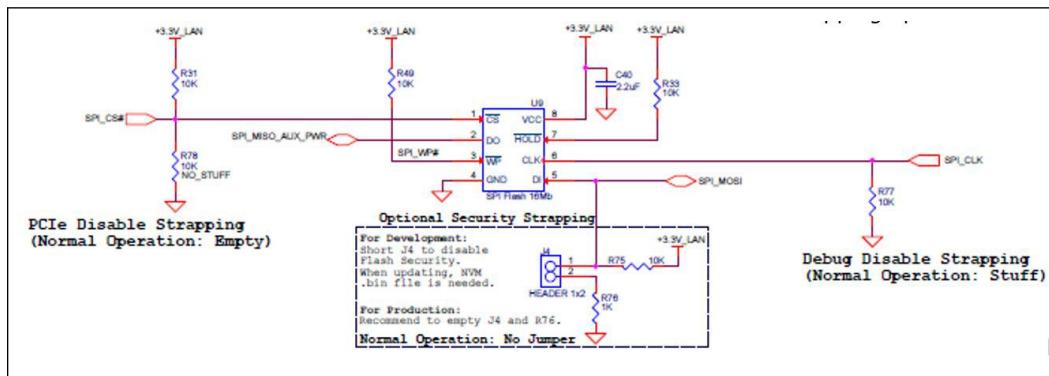
When using a discrete magnetic, add a  $0.1\ \mu F$  capacitor to each center tap pin of the magnetic. The I225 should have a total of  $4 \times 0.1\ \mu F$  capacitors at the magnetic center tap. Please see I225 Reference Schematic for details.

### 8.2.3 Connecting Flash Interface

#### Connecting Flash

Intel recommends having a Flash socket for validation, but it is not required for production releases. Following is a typical SPI connection for the I225. Please see the Datasheet and I225 Reference Schematic for details of the strapping options.

**Figure 141. Typical SPI Flash Connection**



The I225 provides support for a SPI Flash device that is made accessible to the system through the following:

- Flash Base Address register. The PCIe Control register at an offset that will be identified in a later release of this document
- An address range of the IOADDR register, defined by the I/O Base Address register (PCIe Control register at an offset that will be identified in a later release of this document).
- Expansion ROM Base Address register. The PCIe Control register is at an offset that will be identified in a later release of this document.

### Supported Flash Devices

The I225 uses a SPI Flash. Several words of the Flash are accessed automatically by the I225 after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the Flash space is available to software for storing the MAC address, serial numbers, and additional information.

### Connecting SMBus Interface

The I225 SMB\_DATA and SMB\_CLK signals must be connected to the PCH SMLINK0 for supporting vPro. These pins require pull-up resistors to the 3.3V supply rail.

**Note:** If the interface is not used, the previously mentioned pull-up resistors on the SMB\_DATA and SMB\_CLK signals still have to be in place.

Refer to the I225 Reference Schematic and Schematic/Layout Checklist for more details.

### 8.2.3.1 Connecting Miscellaneous Signals

#### LAN Disable

The I225 has the LAN\_DISABLE\_N pin (pin #2) that can be used for disabling Ethernet functions (disable the silicon). For normal operation, pull this pin up with a 10 K  $\Omega$  resistor to 3.3 Vdc.

### 8.2.4 Connecting Light Emitting Diodes (LEDs)

The I225 provides three programmable outputs to directly drive the LEDs for link activity and speed indications. Each of the three LED outputs can be individually configured to select the particular event, state, or activity, which is indicated on that output. In addition, each LED can be individually configured for output polarity, as well as for blinking versus non-blinking (steady-state) indication.

The LED ports are fully programmable through the Flash interface (LEDCTL register). In addition, the hardware-default configuration for all LED outputs can be specified via a Flash field, thus supporting LED displays configurable to a particular OEM preference.

System designers need to provide separate current limiting resistors for each LED connected.

Since the LEDs are likely to be placed close to the board edge and to external interconnect, take care to route the LED traces away from potential sources of EMI noise. In some cases, it might be desirable to attach filter capacitors.

### LED Configuration #1

This configuration has been used widely in Server/Workstation/Desktop/AIC/etc.

#### Expectation:

Speed LED is a dual-color. Link-Activity LED is a single-color.

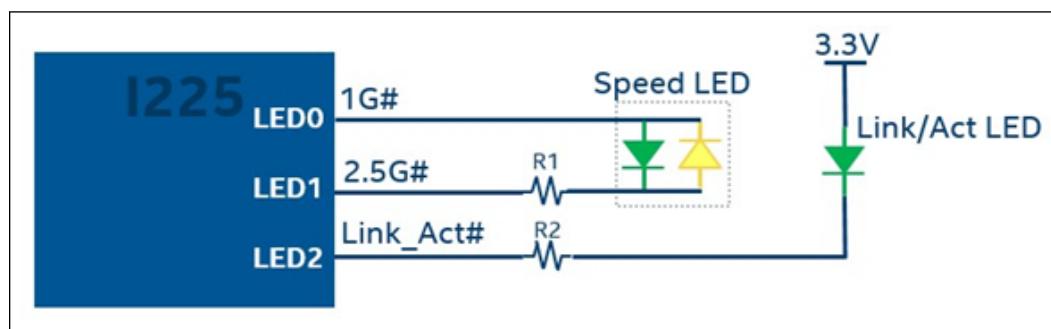
Highest speed LED is Green. Second highest speed LED is Yellow. All other-speed LEDs are OFF.

**Figure 142. LED Configuration #1 Expected Behavior**

Speed LED	
10 Mbps	OFF
100 Mbps	OFF
1000 Mbps	Yellow
2500 Mbps	Green
Link-Activity LED	
Link-up	Green
Tx/Rx Activity	Blinking Green

← 2<sup>nd</sup> Highest Speed  
 ← Highest Speed

**Figure 143. Typical Schematic Setup for LED Configuration #1 Design**



#### NOTES

- All LED pins are active-low signals.
- R1/R2 are current-limit resistors.
- Good practice for server. Just by looking at the back of server racks, IF all LEDs are green, users know all ports are running at the highest speeds.

**Figure 144. I225 NVM Setting for Configuration #1: Offset 0x1C = 0x0508 and Offset 0x1F = 0x8427**

NVM word offset 0x1C = 0x0508 (for LED1 Setting)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0
Reserved				TXAMP				Blink1	Invert1	Reserved				LED1=0x8 (for 2.5G#)	
NVM word offset 0x1F = 0x8427 (for LED0 and LED2 Setting)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1
Blink2	Invert2	Reserved		LED2=0x4 (for Link_Act#)				Blink0	Invert0	Global Blink	Reserved	LED0=0x7 (for 1G#)			

#### Design Notes:

Invert = 0 (LED is an active low signal)

Blink2 = 1 (LED2 is solid = link-up and blinking = Tx/Rx)

Global Blink = 1 (fast blinking mode for all LEDs)

#### LED Configuration #2

This configuration is for the I225 design, which needs individual color for each Ethernet speed.

#### Expectation:

The speed LED can display three different colors. The Link-Activity LED is a single-color.

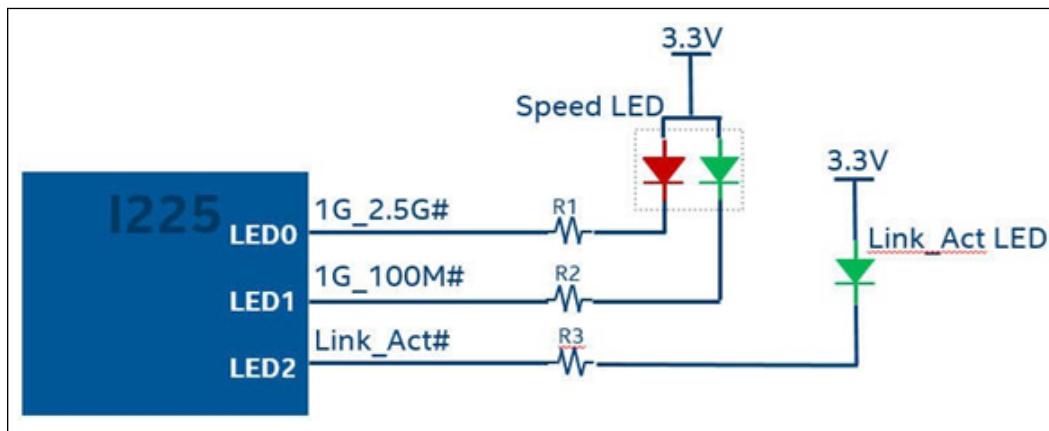
Each speed LED has a different color. This has an advantage for distinct displays of all speeds at assigned colors. The RJ45 cost expected to be higher.

**Figure 145. LED Configuration #2 Expected Behavior**

Speed LED	
10 Mbps	OFF
100 Mbps	Green
1000 Mbps	Yellow
2500 Mbps	Red
Link-Activity LED	
Link-up	Green
Tx/Rx Activity	Blinking Green

← A  
 ← Mixed A+B color, both LEDs turned on at a same time.  
 ← B

**Figure 146. Typical Schematic Setup for LED Configuration #2**



**Design Notes:**

- All LED pins are active-low signals.
- R1/R2/R3 are current-limit resistors.
- Each speed can have its own color by this 3-pin LED. Traditionally, 1 GbE is yellow and 100 Mb/s is green. This setup creates a new red indication for 2.5 GbE.

**Figure 147. Mixed-color Examples for the LED Configuration #2**

Example#	Color A	Color B	Mixed A+B
1	Red	Green	= Yellow
2	Red	Yellow	= Orange
3	Orange	Green	= Yellow

**Figure 148. 225 NVM Setting for Configuration #2: Offset 0x1C = 0x050D and Offset 0x1F = 0x842E**

NVM word offset 0x1C = 0x050D (for LED1 Setting)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1
Reserved				TXAMP				Blink1	Invert1	Reserved			LED1=0xD (for 1G_100M#)		
NVM word offset 0x1F = 0x842E (for LED0 and LED2 Setting)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	0	0	0	0	1	0	1	1	1	0
Blink2	Invert2	Reserved		LED2=0x4 (for Link_Act#)				Blink0	Invert0	Global Blink	Reserved	LED0=0xE (for 1G_2.5G#)			

**Design Notes:**

- Invert = 0 (LED is an active low signal)
- Blink2 = 1 (LED2 is solid = Link-up and blinking = Tx/Rx)

- Global Blink = 1 (fast blinking mode for all LEDs)

## 8.2.5 Connecting JTAG Port

The I225 contains a test access port (3.3 V only) conforming to the IEEE 1149.1-2001 Edition (JTAG) specification. To use the test access port, connect these balls to pads accessible by specific test equipment.

For normal operation, pull-up JTCK, JTDO, JTMS and JTDI signals with 10 K  $\Omega$  resistors to 3.3 Vdc. JRST\_N signals should also be pulled up as well.

## 8.2.6 Crystal Design Considerations

All designs require an external clock. The only option for this clock source is a 25 MHz external crystal. The I225 uses the crystal to generate clocks for the high speed interfaces.

The chosen crystal vendor should be consulted early in the design cycle. Crystal manufacturers familiar with networking equipment clock requirements might provide assistance in selecting an optimum, low- cost solution.

The following parameters are required when selecting the 25 MHz external crystal component for I225.

**Table 151. External Crystal Specifications**

Parameter Name	Symbol	Recommended Value	Max/Min Range	Conditions
Frequency	$f_o$	25 [MHz]		@25 [ $^{\circ}$ C]
Vibration Mode		Fundamental		
Frequency Tolerance @25 $^{\circ}$ C	$Df/f_o$ @25 $^{\circ}$ C	$\pm 30$ [ppm]		@25 [ $^{\circ}$ C]
Temperature Tolerance	$Df/f_o$	$\pm 30$ [ppm]		0 to +70 [ $^{\circ}$ C]
Series Resistance (ESR)	$R_s$		60 [ohms] max	@25 [MHz]
Crystal Load Capacitance	$C_{load}$	18 [pF]		
Shunt Capacitance	$C_o$		5 [pF] max	
Drive Level	$D_L$		100 [milliW] max	
Aging	$Df/f_o$	$\pm 5$ ppm per year	$\pm 5$ ppm per year max	
Calibration Mode		Parallel		
Insulation Resistance			500 [Mohms] min	@ 100 Vdc
<i>Note:</i> The selected Crystal Component must meet or exceed the specified drive Level ( $D_L$ ) The crystal Component datasheet should show 100uW or more.				

## Quartz Crystal

Quartz crystals are the mainstay of frequency components due to low cost and ease of implementation. They are available from numerous vendors in many package types with various specification options.

### Vibrational Mode

Crystals are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals. At any operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

### Frequency Tolerance

The frequency tolerance for an Ethernet Platform LAN Connect is dictated by the IEEE 802.3 specification as  $\pm 50$  parts per million (ppm). This measurement is referenced to a standard temperature of 25 °C. It is recommended that a frequency tolerance of  $\pm 10$  ppm be used.

### Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -10 °C to +70 °C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers can also list temperature stability as 50 ppm in their datasheets.

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### NOTE

Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

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### Calibration Mode

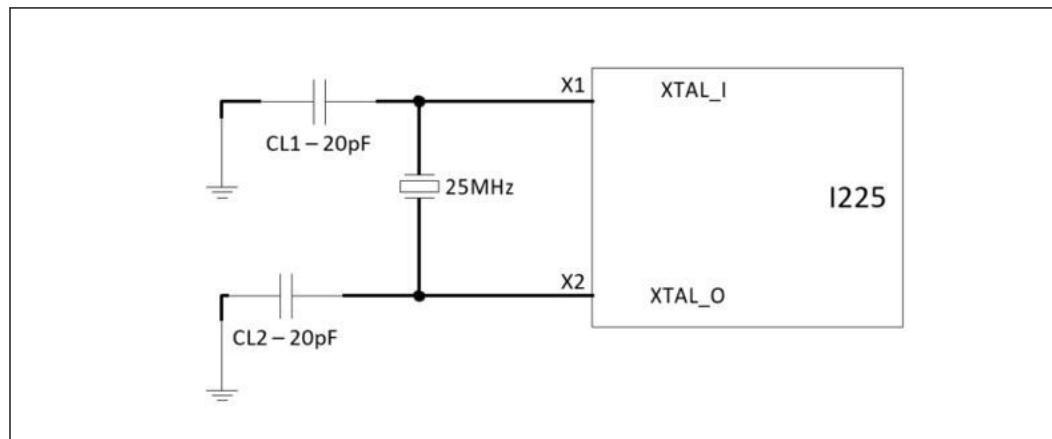
The terms series-resonant and parallel-resonant are used to describe crystal oscillator circuits.

Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory. A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal's inherent series resonant frequency.

### Reference Crystal Circuit

Figure below shows a typical schematic of the I225 oscillating circuit. Pin X1 and X2 refers to XTAL1 and XTAL2 in the I225, respectively. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit.

**Figure 149. Crystal Circuit**



### Crystal Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C_1 \cdot C_2)}{(C_1 + C_2)} + |C_{stray}|$$

where  $C_1 = C_2 = 20\text{ pF}$  and  $C_{stray} = \text{allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet device package}$ . An allowance of 3 pF to 10 pF accounts for lumped stray capacitance.

The calculated crystal load capacitance is 18 pF with  $C_1 = C_2 = 20\text{pF}$  and an estimated stray capacitance of about 8 pF. Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the device. Thin circuit boards generally have higher stray capacitance than thick circuit boards.

The oscillating frequency should be measured with a precision frequency counter where possible. The load specification or values of C1 and C2 should be fine-tuned for the design. As the actual capacitance load increases, the oscillating frequency decreases.

---

#### NOTE

C1 and C2 can vary by as much as 5% (approximately 1 pF) from their nominal values.

---

## Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 5 pF.

## Equivalent Series Resistance (ESR)

ESR is the actual component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 60 Ω or better.

## Driver Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

I225 Ethernet controllers can drive crystals up to 100 mW value. Therefore, the crystal datasheets should support at least of 100 mW. Otherwise, the silicon will over drive the crystal.

## Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

## Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2. Even with a perfect support circuit, most crystals oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal is perfectly centered at the desired target frequency.

## Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal. These are listed below.

- If a Saunders and Associates (S&A) crystal network analyzer is available, discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation is a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.

- If a crystal analyzer is not available, the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It might also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

When choosing a crystal, keep in mind that to comply with IEEE specifications for 100/1000/2.5GBASE-T Ethernet LAN, the transmitter reference frequency must be precise within  $\pm 50$  ppm. Intel recommends using a transmitter reference frequency that is accurate to within  $\pm 10$  ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance

- **Circuit Board**

Since dielectric layers of the circuit board are allowed some reasonable variation in thickness, stray capacitance from the printed board (to the crystal circuit) also vary. If the thickness tolerance for the outer layers of dielectric are controlled within  $\pm 17$  percent of nominal, the circuit board should not cause more than  $\pm 2$  pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards. Alternatively, a larger sample population of circuit boards can be used. A larger population increases the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance. Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board and the LAN reference frequency should be measured on each circuit board. The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

- **Temperature Changes**

Temperature changes can cause crystal frequency to shift. Frequency measurements should be done in the final system chassis across the system's rated operating temperature range.

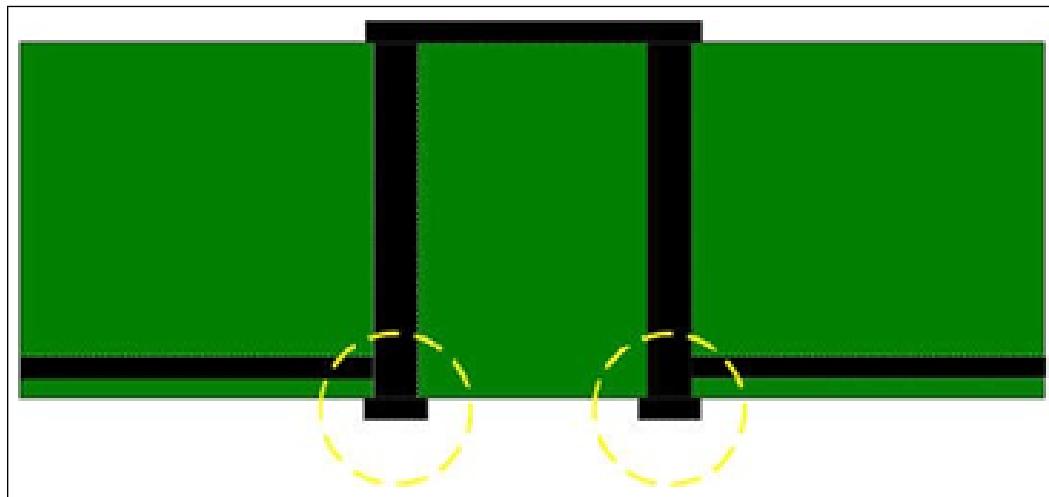
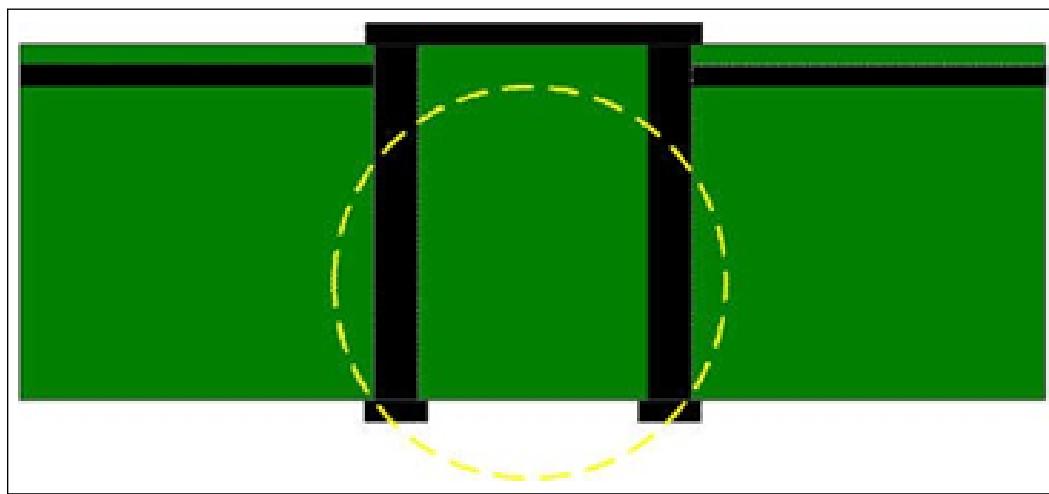
## 8.2.7

### PCB Guidelines

This section describes the general PCB design guidance targeted as supplementary information in addition to the specific requirements and recommendations for individual interfaces. For items not directly covered in the specific interface sections, these guidance recommendations apply to the design.

#### Via Usage

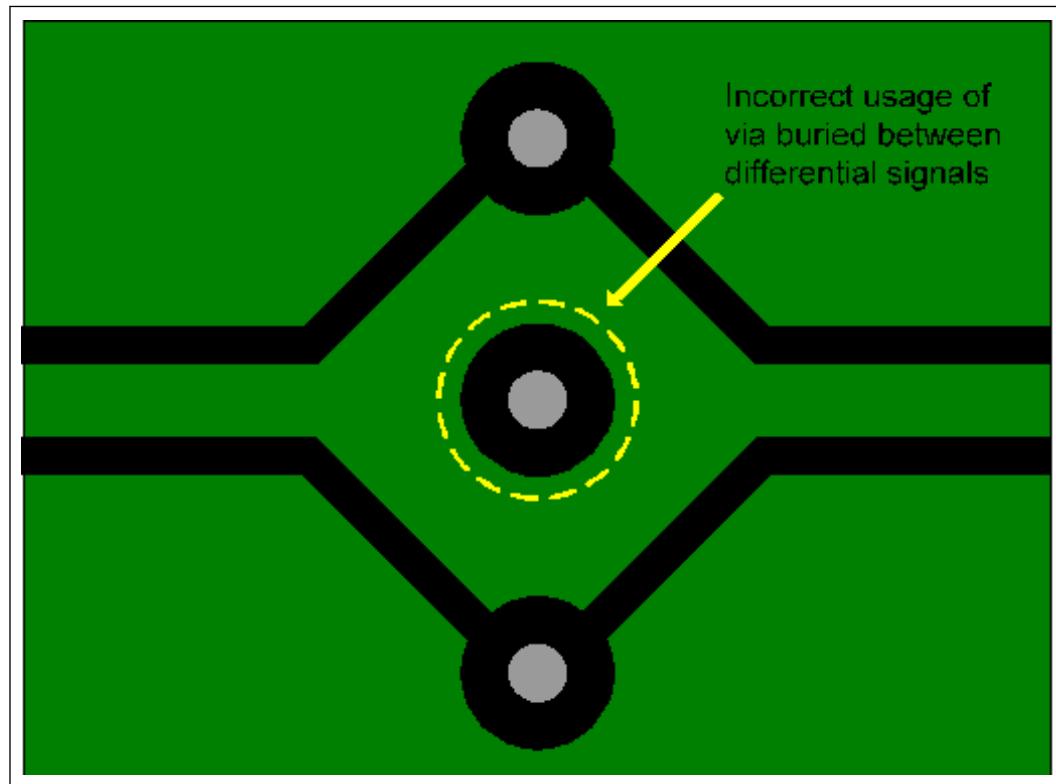
Use vias to optimize signal integrity. Figure below shows correct via usage. Figure below shows the type of topology that should be avoided.

**Figure 150. Correct Via Usage****Figure 151. Incorrect Via Usage**

Any via stubs on the MDI differential signal traces must be less than 0.889 mm in length. Keeping MDI signal via stubs less than or equal to 0.508 mm is preferable.

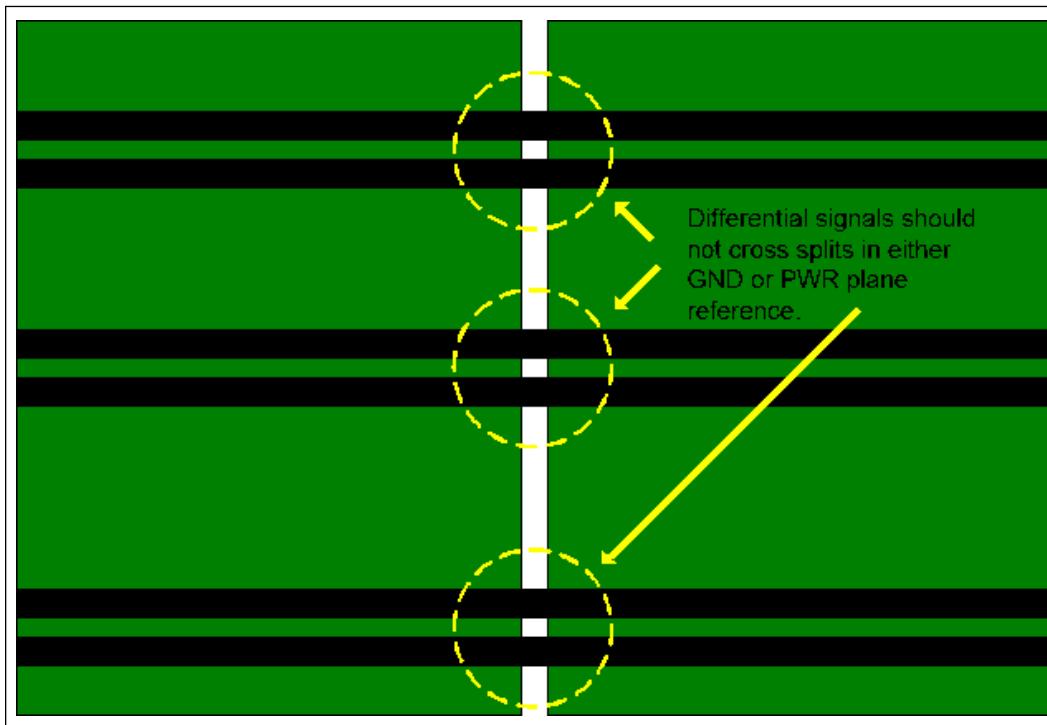
Place ground vias adjacent to signal vias used for the MDI interface. DO NOT embed vias between the high-speed signals, but place them adjacent to the signal vias. This helps to create a better ground path for the return current of the AC signals, which also helps address impedance mismatches and EMC performance.

It is recommended that, in the breakout region between the via and the capacitor pad, target a  $Z_0$  for the via to capacitor trace equal to 50 ohms. This minimizes impedance imbalance.

**Figure 152. Incorrect Via Usage for Differential Pair**

#### Reference Planes

Do not cross plane splits with the MDI high-speed differential signals. This causes impedance mismatches and negatively affects the return current paths for the board design and layout. Refer Figure below.

**Figure 153. Improper Differential Signal Routing - Plane Split**

Traces should not cross power or ground plane splits if at all possible. Traces should stay seven times the dielectric height away from plane splits or voids. If traces must cross splits, capacitive coupling should be added to stitch the two planes together to provide a better AC return path for the high-speed signals. To be effective, the capacitors should have low ESR and low equivalent series inductance

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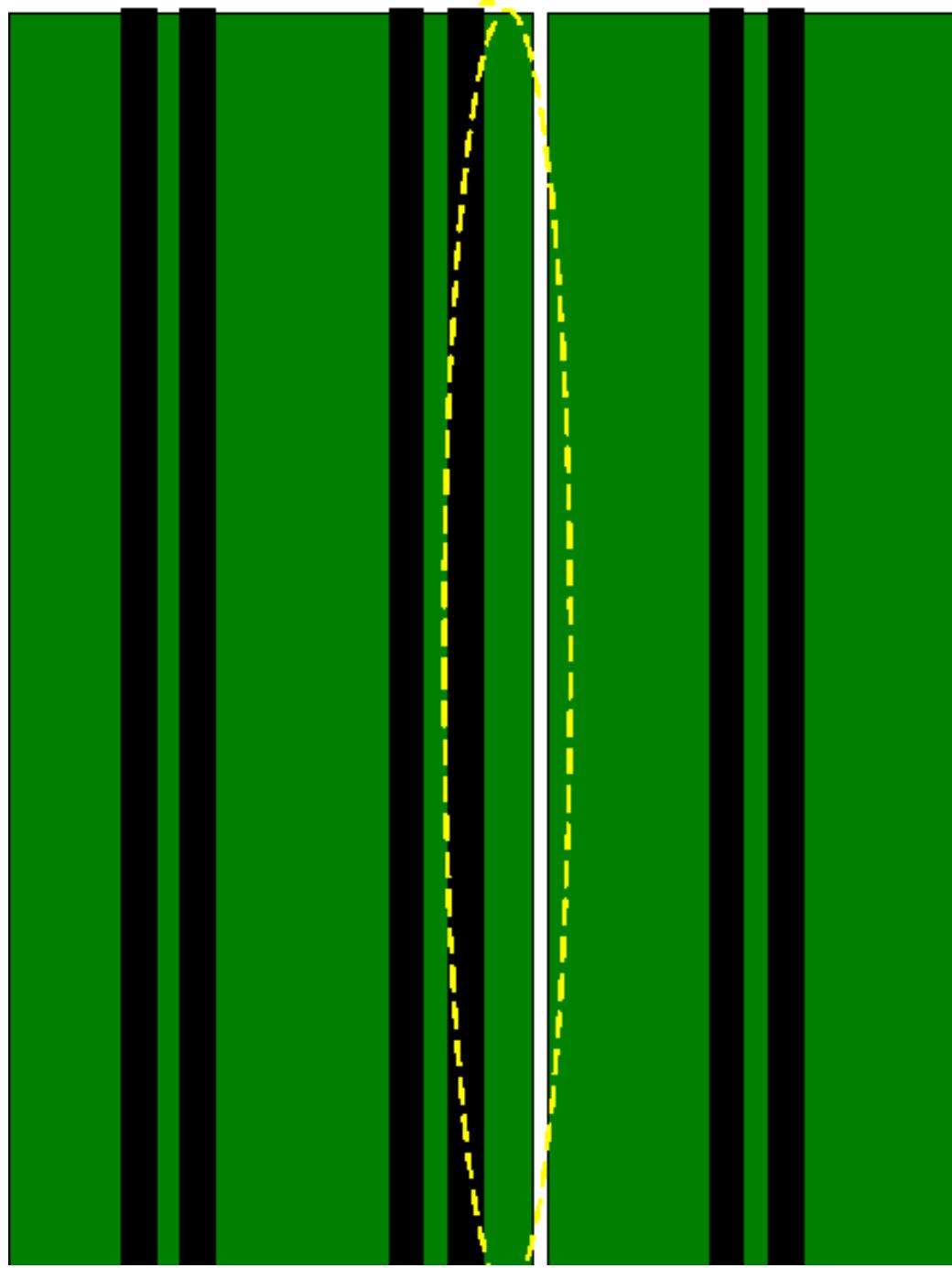
**NOTE**

Even with plane split stitching capacitors, crossing plane splits is extremely high risk for 5GBASE-T designs

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**Figure 154. Differential Signal Routing - Plane Split and Void Proximity**

Differential signals should be  $> 6$   
x dielectric height away from  
PWR and GND plane splits.



It is recommended that the MDI signals stay at least seven times the dielectric height away from any power or ground plane split. This improves impedance balance and return current paths.

If a high-speed signal needs to reference a power plane, ensure that the height of the secondary (power) reference plane is at least 3 x the height of the primary (ground) reference plane.

### Reducing Circuit Inductance

Traces should be routed over a continuous reference plane with no interruptions. If there are vacant areas on a reference or power plane, the signal conductors should not cross the vacant area. Routing over a void in the reference plane causes impedance mismatches and usually increases radiated noise levels. Noisy logic grounds should NOT be located near or under high-speed signals or near sensitive analog pin regions of the LAN silicon. If a noisy ground area must be near these sensitive signals or IC pins, ensure sufficient decoupling and bulk capacitance in these areas. Noisy logic and switching power supply grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc.

All ground vias should be connected to every ground plane; and similarly, every power via should be equally potential power planes. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible while still meeting the relevant electrical requirements because signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling and simulation software.

### Signal Isolation

To maintain the best signal integrity, keep digital signals far away from the analog traces. A good rule to follow is no digital signal should be within 7x to 10x dielectric height of the differential pairs. If digital signals on other board layers cannot be separated by a ground plane, they should be routed at a right angle (90 degrees) to the differential signal traces. If there is another Ethernet controller on the board, take care to keep the differential pairs away from that circuit. The same thing applies to switching regulator traces.

Rules to follow for signal isolation:

- Separate and group signals by function on separate board layers if possible. Maintain a separation that is at least seven times the thinnest adjacent dielectric height between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.
- Over the length of the trace run, each differential pair should be at least seven times the thinnest adjacent dielectric height away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate other I/O signals from high-speed signals to minimize crosstalk. Crosstalk can increase radiated EMI and can also increase susceptibility to EMI from other signals.

- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

### Traces for Decoupling Capacitors

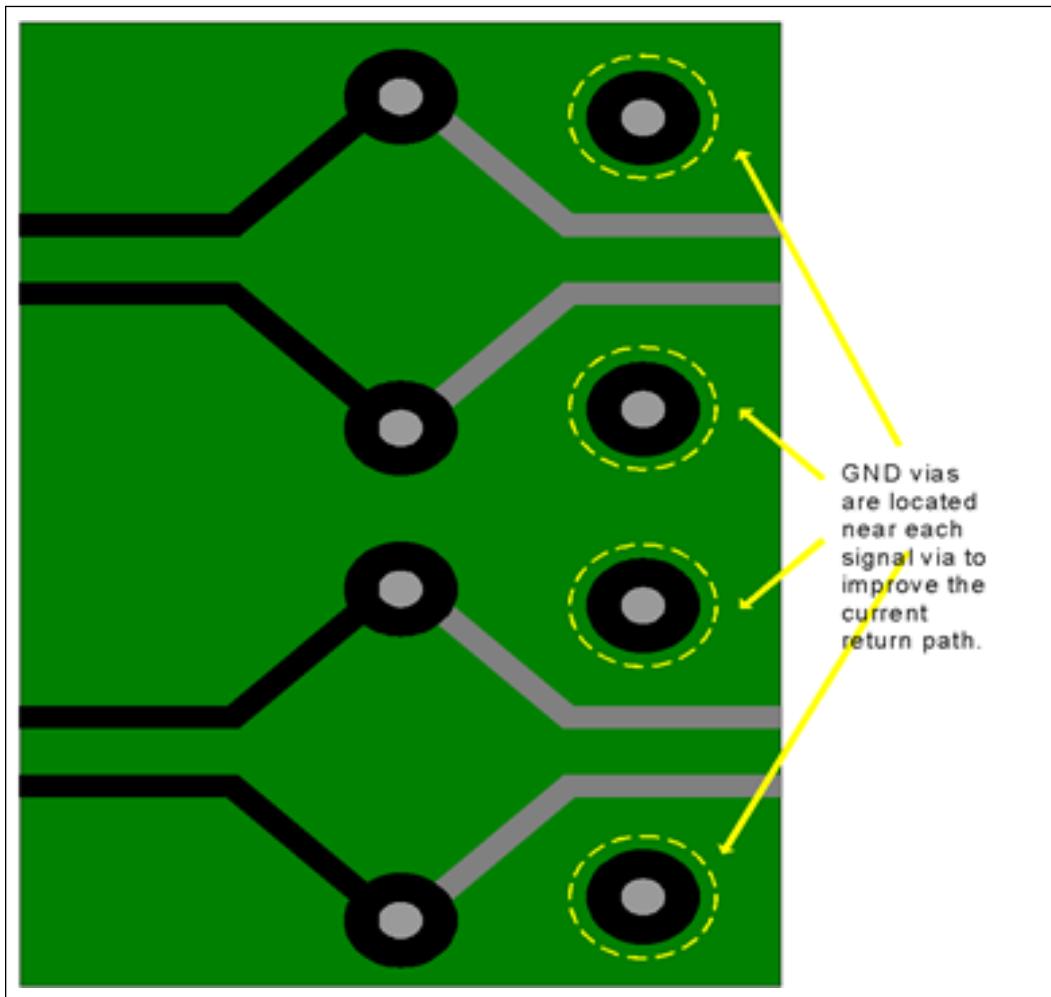
Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and reduce the intended effect of decoupling capacitors. Also, for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

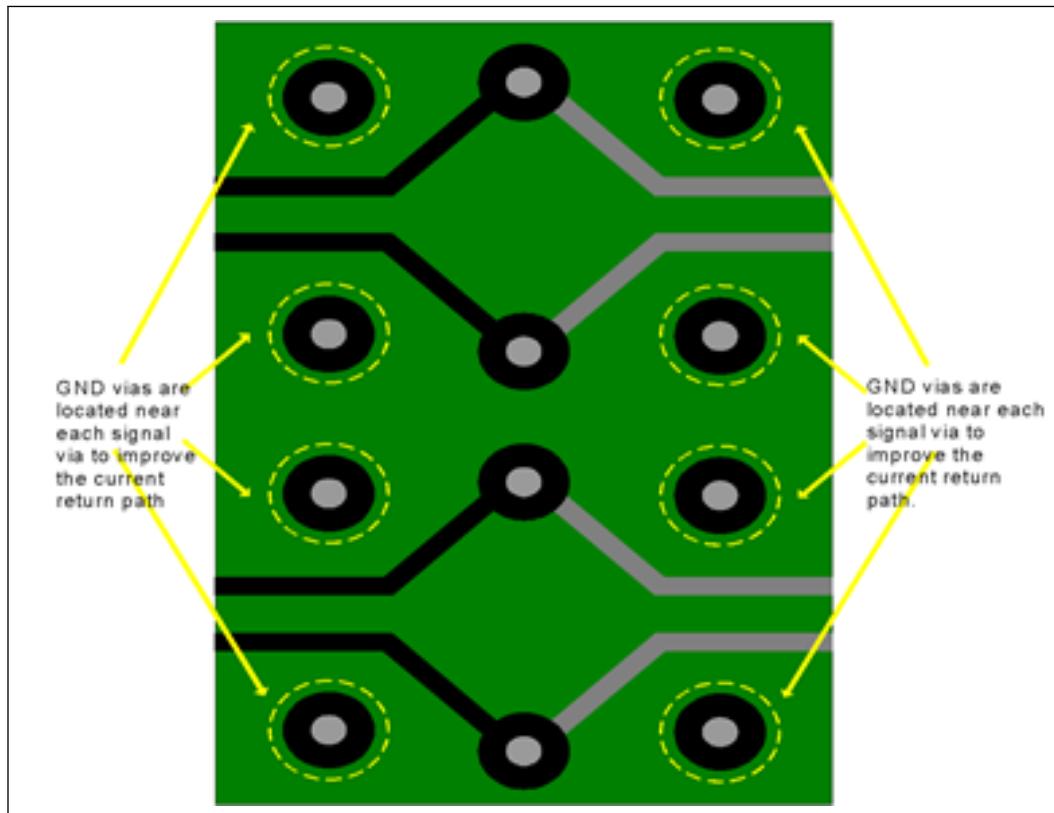
### Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and locating decoupling capacitors at or near power inputs to bypass to the signal return. This significantly reduces EMI radiation.

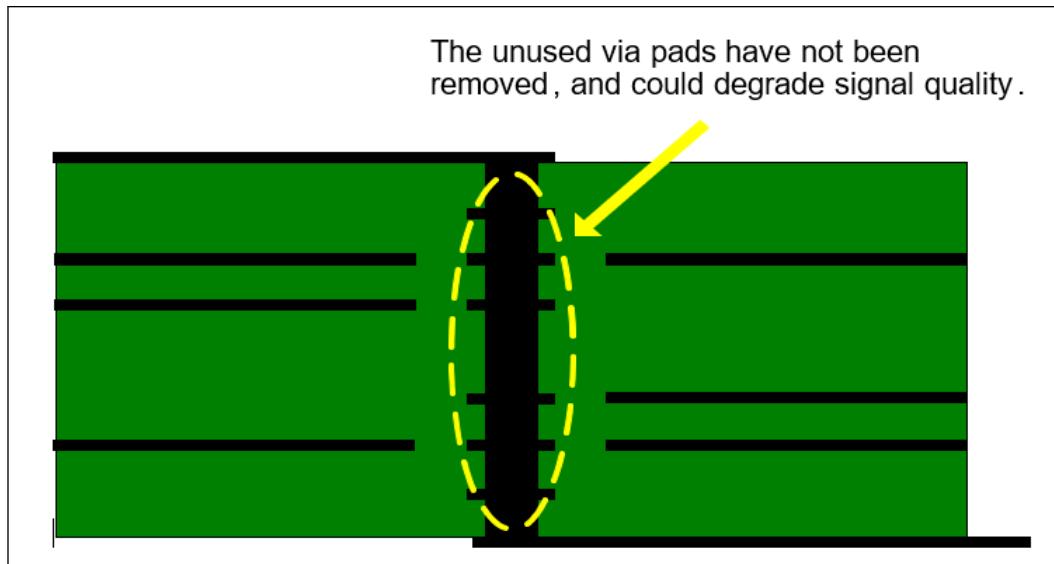
These general following guidelines help reducing circuit inductance:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. Routing signals over power or ground voids increases inductance and increases radiated EMI levels.
- Use distance and/or extra decoupling capacitors to separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds can affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- Do not route high-speed signals near switching regulator circuits.
- It's acceptable to put ground fill or thieving on the trace layers, but preferably not closer than 1.27 mm to the differential traces and the connector pins.
- If differential traces must be routed on another layer, the signal vias should carry the signal to the opposite side of the PCB (to be near the top of the PCB), AND if the high-speed signals are being routed between two connectors on the same board, before the signal traces reach the second connector, they must return to the original signal layer (before reaching the connector pin). This strategy keeps via stubs short without requiring back drilling.
- Each time differential traces make a layer transition (pass through a pair of signal vias), there must be at least one ground via located near each signal via. Two ground vias near each signal via is better. Refer Figures below.

**Figure 155. Return Path Vias for Differential Signals - Acceptable Example**

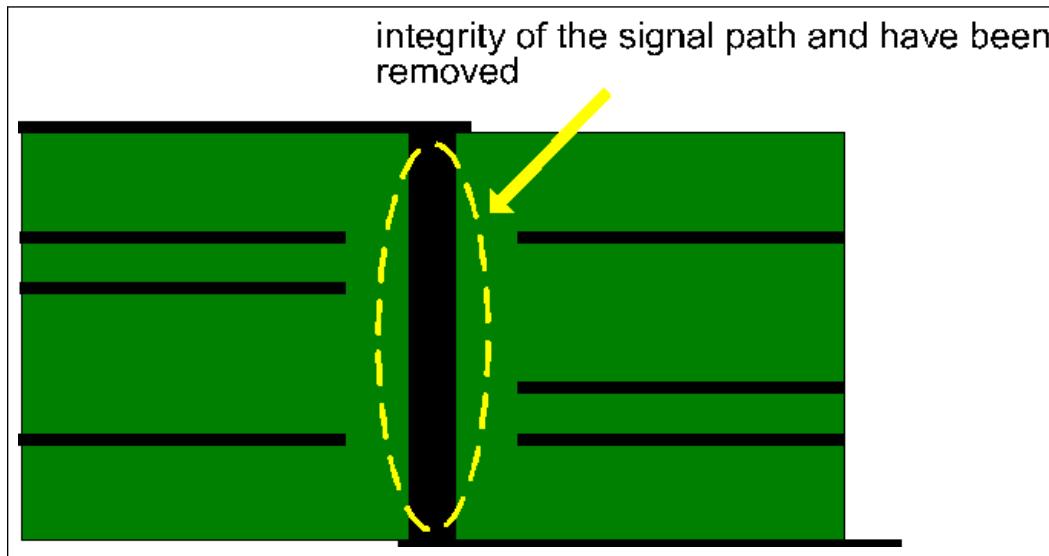
**Figure 156. Return Path Vias for Differential Signals - Optimal Example**

If the PCB fabrication process permits it, it's best to remove signal via pads on unconnected metal layers. Refer Figure below.

**Figure 157. Signal Vias: Improper Padstack Example**

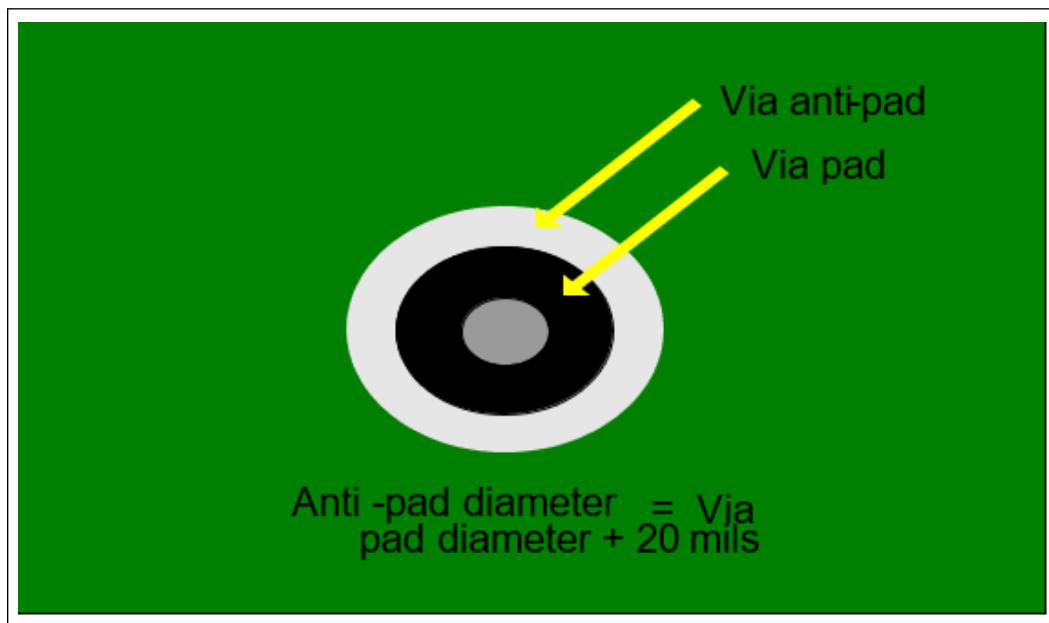
The unused via pads degrade the signal

**Figure 158. Signal Vias: Optimal Padstack**

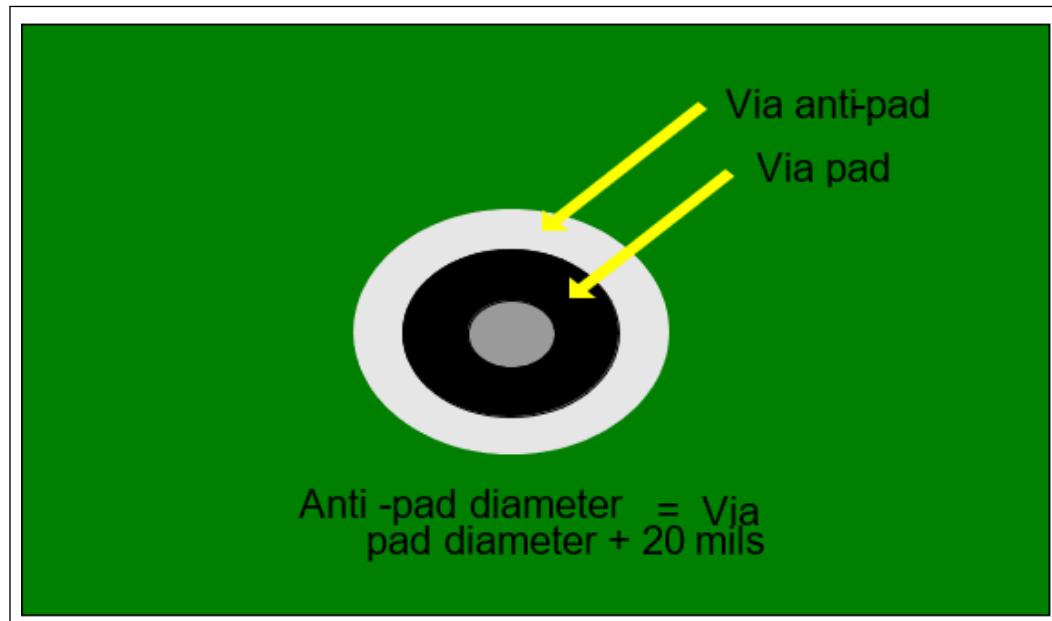
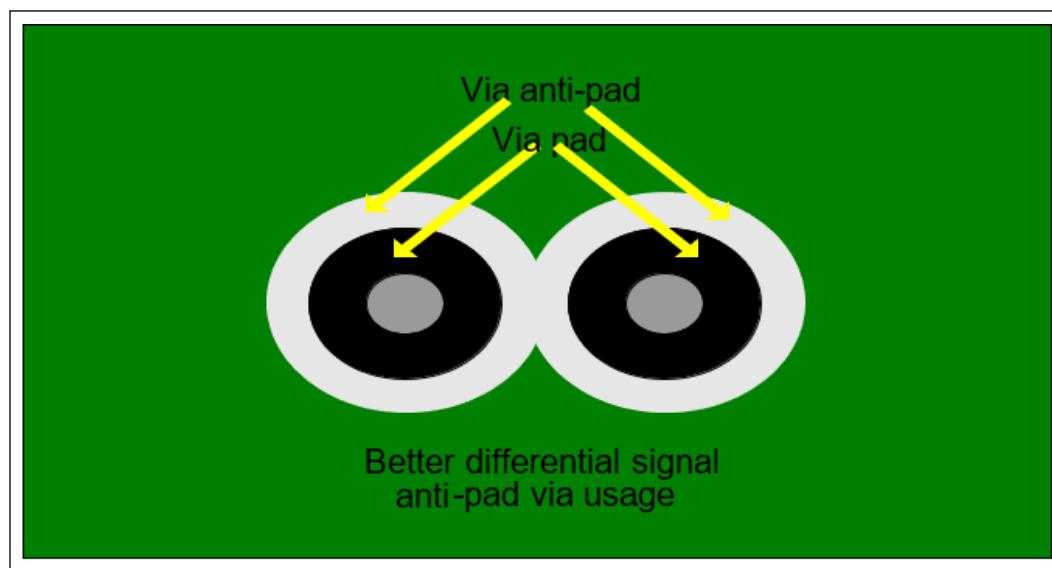


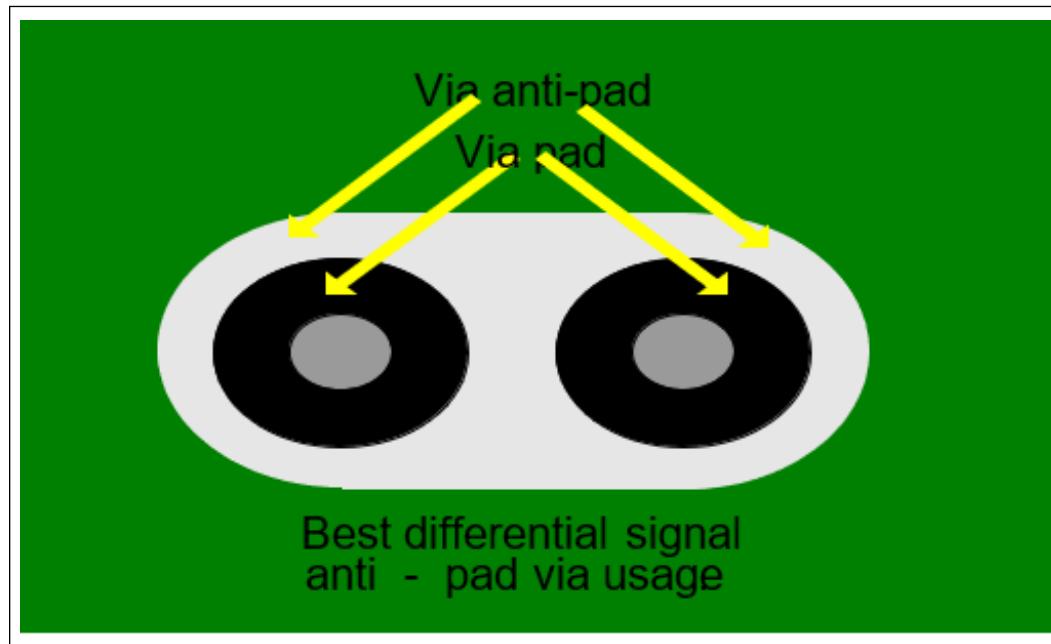
On metal layers where signal vias need to have via pads, it is desirable to reduce capacitance between the signal vias and ground-plane layers. The anti-pad diameters should be up to 0.508 mm larger than the via pad diameters. Refer Figure below. Clearance between the pad and the surrounding metal should be  $\geq 0.254$  mm

**Figure 159. Anti-Pad Geometry**



Each time differential signal vias pass through a plane layer, within each differential pair, the anti-pads should overlap. Refer Figure below.

**Figure 160. Differential Signal Vias: Improper Anti-pad Geometry****Figure 161. Differential Signal Vias: Acceptable Example**

**Figure 162. Differential Signal Vias: Optimal Example****Differential High Speed Layout Guideline**

The following shows the Good vs Bad Practices for typical differential high-speed signals. This guideline should be applied when routing the 4x MDI pairs and PCIe TX/RX pairs of I225.

Figure 163. Differential High Speed Layout Guidelines

<i>Fan-out/ Break-out</i>	✓	✓	!
<i>Balanced routing</i>	✓	✓	❌
<i>Direction change</i>	✓	!	❌
<i>Length matching</i>	✓	!	❌
	✓	!	❌
<i>Keep-outs/ Clearances</i>	✓	!	!
<i>Stubs</i>	✓	✓	❌
<i>Layer change</i>	✓	!	❌
	✓ ! ❌	No layer change Balanced layer change Top-to-bottom layer change Top-to-bottom layer change, with backdrilling or UVia Via short	Unbalanced layer change

## 8.2.8 Component Selection (Bill Of Material)

Listed parts have been used successfully in the past designs. Note that no particular part is required to use with the I225 silicon. It is recommended to start with the known quality parts, which Intel knows that they work. At a high-level, any part within the I225 specifications should work with the silicon.

Any selected parts must go through the validations for production design quality.

### NOTE

Please see the recommended parts list in the I225 Datasheet.

## 8.3 M.2 7360 WWAN Design Guidelines

The WWAN M.2 7360 LTE Advanced module supports 3G, 4G/LTE wireless technologies in a very small M.2 card footprint. The WWAN M.2 module achieves download rates to 450 Mbps through support of 3GPP release 11 LTE Carrier Aggregation.

There is only WW SKU of WWAN M.2 LTE Advanced module to support the various RF frequency bands and band combinations deployed worldwide including North America, Europe, Japan, and Asia Pacific.

The WWAN M.2 module supports several unique Intel features such as Adaptive Clocking, Selective Suspend, Link Power Management, and Dynamic Power Thermal Management in support of an always on/always connected (AOC) user experience.

The M.2 offers single side component mounting, a 75 pin host interface, in a 30 mm x 42 mm compact card size.

### 8.3.1 WWAN M.2 7360 LTE Advanced Module Overview

There is only one WWSKU M.2 7360 LTE Advanced modules available in the M.2 Card of Type 3042 form factor. Details of the features, RF band support, and data rates for the WWAN M.2 modules are shown in below tables.

**Table 152. WWAN M.2 Module - General Features**

Feature	Description	Addition Information
Mechanical	M.2 Card Type 3042 Key B	30 mm x 42 mm Pin count: 75 (67 usable, 8 slot-key)
Operating Voltage	3.3 V +/- 5%	Laptop/ Notebook
Operating Temperature	-10 °C to +55 °C	-
Application Interface (75 pin card)	Interprocessor Communications	PCIe
	USIM w/ Card Detect	SIM_CLK, SIM_RESET, SIM_IO, SIM_PWR, SIM_DETECT
	WWAN M.2 Control	FULL_CARD_POWER_OFF#
		RESET#
		W_DISABLE#
		LED#1

*continued...*

Feature	Description	Addition Information
		DPR (Body SAR)
		WAKE on WWAN
		GNSS Disable
	Global Positioning (GPS/GLONASS)	TX_BLANKING, FINE_TUNE_AIDING (FTA)
	Antenna Tuning	(4) GPO (SMARTi™ RF Transceiver)
	RF Coexistence	UART_RX, UART_TX, GNSS_EXT_FTA UART supports Real-Time Coexistence
	Audio	I2S <sup>1</sup>
RF Antenna	Main and Diversity/ GNSS	Separate coax connectors
Debug	JTAG	-
	ETM11	-
	MIPI PTI	-

**NOTE**

1. Hardware interface available, no software support

**Table 153. WWAN M.2 Module - RF Band Support**

RF Band	Approximate Center Frequency	Duplex Mode	SKU LTE WW SKU	
			UMTS	LTE
001	2100 MHz	FDD	x	x
002	1900 MHz	FDD	x	x
003	1800 MHz	FDD	-	x
004	1700 MHz	FDD	x	x
005	850 MHz	FDD	x	Sub band of 261
006	850 MHz	FDD	Sub band of 51	-
007	2.6 GHz	FDD	-	x
008	900 MHz	FDD	x	x
009	1800 MHz	FDD	-	-
010	1700 MHz	FDD	-	-
011	1500 MHz	FDD	-	x
012	700 MHz	FDD	-	x
013	750 MHz	FDD	-	x
014	750 MHz	FDD	-	-
017	700 MHz	FDD	-	Sub band of 121
018	850 MHz	FDD	-	Sub band of 261

*continued...*

RF Band	Approximate Center Frequency	Duplex Mode	SKU LTE WW SKU	
			UMTS	LTE
019	850 MHz	FDD	-	Sub band of 261
020	800 MHz	FDD	-	x
021	1500 MHz	FDD	-	x
022	3.5 GHz	FDD	-	-
023	2 GHz	FDD	-	-
024	1600 MHz	FDD	-	-
025	1900 MHz	FDD	-	-
026	850 MHz	FDD	-	x
027	850 MHz	FDD	-	-
028	750 MHz	FDD	-	x
029	700 MHz	FDD	-	x
030	2.3 GHz	FDD	-	x
033	2.1 GHz	TDD	-	-
034	2.1 GHz	TDD	-	-
035	1900 MHz	TDD	-	-
036	1900 MHz	TDD	-	-
037	1900 MHz	TDD	-	-
038	2.6 GHz	TDD	-	x
039	1900 MHz	TDD	-	x
040	2.3 GHz	TDD	-	x
041	2.5 GHz	TDD	-	x
042	3.5 GHz	TDD	-	-
043	3.7 GHz	TDD	-	-
044	700 MHz	TDD	-	-

**LTE Advanced Carrier Aggregation (CA)** enables multiple LTE carriers to be used together to provide the high data rates required for LTE Advanced.

Inter-band and intra-band RF band combinations supported by the WWAN M.2 LTE Advanced modules are shown below.

**Table 154. LTE Advanced Carrier Aggregation - Inter-Band Support**

SKU	RF Band Inter-band Combinations
WWAN M.2 LTE Advanced WW	<ul style="list-style-type: none"> <li>• 1+3,5, 7, 8,11,18,19,20,21,26,28</li> <li>• 2+2,4,5,12(17), 13,28,,29,30,66;</li> <li>• 3+3,5,7,8,19,20, 26,28;</li> <li>• 4+4,5,12(17), 13,28,29,30;</li> <li>• 5+ 5,7,30,66;</li> <li>• 7+7,8,12,20,28;</li> </ul>

SKU	RF Band Inter-band Combinations
	<ul style="list-style-type: none"> <li>• 8+11;</li> <li>• 11+18;</li> <li>• 12+30,66;</li> <li>• 13+2,4,66;</li> <li>• 19+21,</li> <li>• 21+28,</li> <li>• 29+30, 66;</li> <li>• 39+39,41;</li> <li>• 40+40;</li> <li>• 41+41;</li> <li>• 66+66</li> </ul>

**Table 155. LTE Advanced 3 Carrier Aggregation**

SKU	2 Contiguous Plus Inter-band
WWAN M.2 LTE Advanced WW	<ul style="list-style-type: none"> <li>• 1+3+5, 1+3+7, 1+3, 8, 1+3+19, 1+3+20, 1+3+28, 1+5+7, 1+7+8, 1+7+20, 1+7+28, , 1+11+18, 1+19+21, 1+8+11;</li> <li>• 2+4+5, 2+4+13, 2+4+29, 2+4+30, 2+5+30, 2+5+66, 2+12+30, 2+12+66, 2+29+30, 2+4+12;</li> <li>• 3+5+7, 3+7+8, , 3+7+20, 3+3+5, 3+3+7, 3+7+7, 3+7+28, 3+3+28;</li> <li>• 4+5+30, 4+12+30, 4+29+30, 4+4+12;</li> <li>• 5+2+2, 5+66+66;</li> <li>• 7+7+28;</li> <li>• 13+2+2, 13+4+4, 13+66+2, 13+66+66;</li> <li>• 39+39+41, 39+41+41;</li> <li>• 40+40+40;</li> <li>• 41+41+41;</li> <li>• 66+66+66;</li> </ul>

**Table 156. LTE Advanced Carrier Aggregation – Intra-band Support**

SKU	RF Band Intra-band Combinations
WWAN M.2 LTE Advanced WW	<ul style="list-style-type: none"> <li>• Band 1, 2, 3, 4, 7, 38, 39, 40, 41</li> </ul>

**Table 157. WWAN M.2 Module – Data Services**

Data Service	M2 7360 LTE WW SKU
WCDMA: DL 384 kbps, UL 384 kbps	x
HSPA+: DL 21 Mbps, UL 5.7 Mbps	x
HSPA+: DL 42 Mbps, UL 5.7 Mbps	x
LTE FDD: DL 100 Mbps, UL 50 Mbps	x
LTE TDD: DL 50 Mbps, UL 50 Mbps	x
LTE FDD: DL 300 Mbps, UL 50 Mbps	x
LTE FDD: DL 450 Mbps, UL 50 Mbps	x

**WWAN M.2 Module – Block Diagram**

- **WWAN M.2 3G/LTE Advanced Module**

The WW LTE Advanced module supports MultiRat (3G, 4G), 3GPP release 11 Compliant Modem providing datacard functionality. The modules are based on Intel's XMM™7360 modem platform.

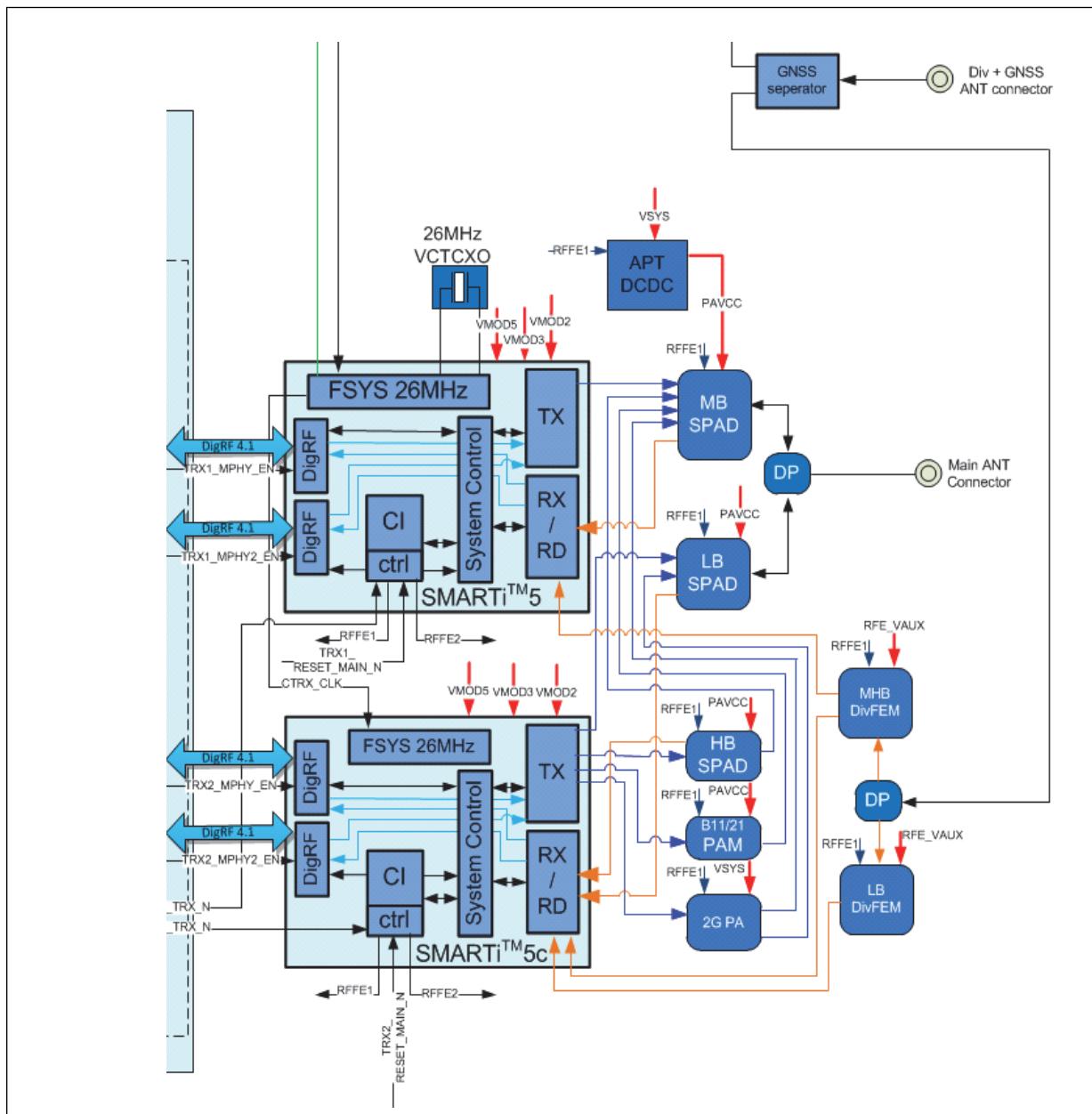
The XMM™7360 modem platform contains Intel's' X-GOLD™ 736G Baseband Controller device accompanied by the multiband multimode RF transceiver chip, SMARTi™ 5. Intel complements the XMM™7360 modem platform Modem Platform with its own worldwide proven triple-mode 3GPP Protocol Stack in its Release 11 version, in order to provide a complete in-house system solutions.

For GNSS support, The M.2 LTE Advanced module integrates Intel's CG2100 device. The CG2100 is a high-performance single-die with fully integrated GPS, GLONASS, Beiduo, Galileo receivers with GPS and GNSS support.

The WWAN M.2 WW LTE Advanced module is targeted towards APAC, North America and Europe and offers 3G, and LTE Advanced data card functionality.

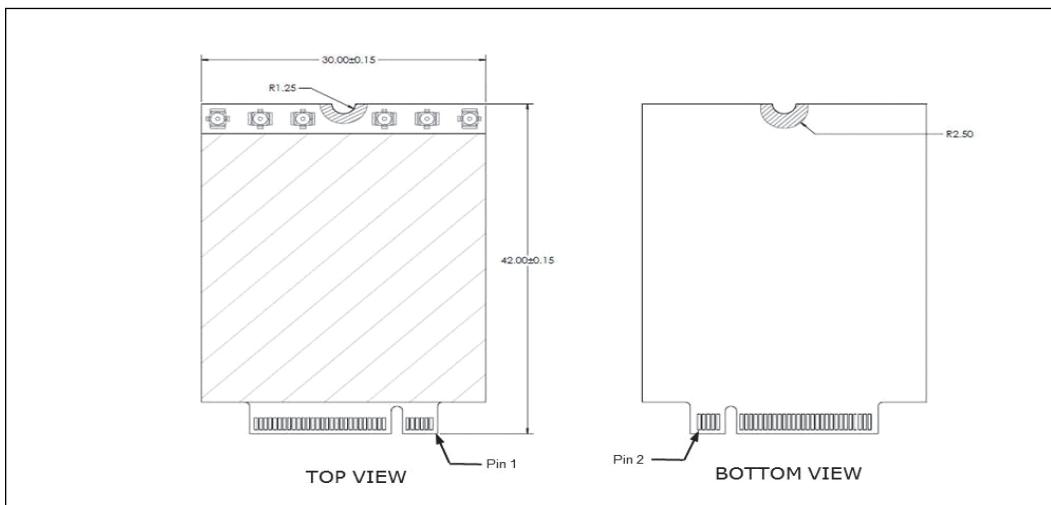
A more detailed view of the RF Engine utilized on the WWAN M.2 LTE Advanced module is shown below.

Figure 164. WWAN Module RF Engine Block Diagram



- **Host Interface Signals**

This section describes the signals available to the host processor at the 75 pin application interface. Eight signals are eliminated by the slot-key on the host connector, leaving 67 usable signals. A diagram of the WWAN M.2 module identifying the 75 pin interface on the WWAN Card Type 3042-S3-B card is shown below. Note that the WWAN M.2 module has all components mounted on the top side. Odd pin numbers are on the top side while even pins on the bottom side.

**Figure 165. M.2 Module Diagram**

**Table 158. Host Interface Signals**

Pin	Signal Name	I/O	Description	Supply
1	CONFIG_3	O	Presence Indication: WWAN M.2 Connects to GND internally	-
2	3.3V	P	WWAN M.2 Supply Pin 3.3 V	3.3 V
3	GND	P	Ground	-
4	3.3V	P	WWAN M.2 Supply Pin 3.3 V	3.3 V
5	GND	P	Ground	-
6	FULL_CARD_POWER_OF_F#	I	Control signal to power On/Off WWAN M.2	3.3 V
7	USB D+	IO	USB 2.0 HS DPLUS Signal	-
8	W_DISABLE#	I	Active low signal to Disable Radio Operation	1.8 V
9	USB D-	IO	USB 2.0 HS DMINUS Signal	-
10	LED#1	O	Open Drain, active low signal used for add-in card to provide status	3.3 V
11	GND	P	Ground	-
12	SLOT KEY			
13	SLOT KEY			
14	SLOT KEY			
15	SLOT KEY			
16	SLOT KEY			
17	SLOT KEY			
18	SLOT KEY			
19	SLOT KEY			
20	AUDIO0	IO	PCM Clock (I2S_CLK)	1.8 V

*continued...*

Pin	Signal Name	I/O	Description	Supply
21	CONFIG_0	O	Configuration Status. Presently not connected on WWAN M.2 module.	-
22	AUDIO1	I	PCM In (I2S_RX)	1.8 V
23	WAKE_WWAN#	O	Wake On WWAN Use by WWAN M.2 to wake up host.	1.8 V
24	AUDIO2	O	PCM Out (I2S_TX)	1.8 V
25	DPR	I	Dynamic Power Reduction - Body SAR control signal	1.8 V/3.3V
26	GNSS_DISABLE#	I	Disable GNSS function	1.8 V
27	GND	P	Ground	-
28	AUDIO3	IO	PCM Sync (I2S_WA0)	1.8 V
29	USB30_RxN	I	USB3.2 SS Receive N(Host RX, WWAN TX)	-
30	UIM_RESET	O	SIM Reset (I)	1.8 V/3.0 V
31	USB30_RxP	I	USB3.2 SS Receive P(Host RX, WWAN TX)	-
32	UIM_CLK	O	SIM Clock (I)	1.8 V/3.0 V
33	GND	-	Ground	-
34	UIM_DATA	IO	SIM Data (I/O)	1.8 V/3.0 V
35	USB30_TxN	O	USB3.2 SS Transmit N(Host TX, WWAN RX)	-
36	UIM_PWR	O	SIM power	1.8 V/3.0 V
37	USB30_TxP	O	USB3.2 SS Transmit P(Host TX, WWAN RX)	-
38	N/C	-	Not connected internally on WWAN M.2	-
39	GND	P	Ground	-
40	I2C_SCL	IO	I2C Clock – GNSS Support	1.8 V
41	PCI_PER_N	I	PCIe Receive N(HOST RX, WWAN TX)	-
42	I2C_SDA	IO	I2C Data – GNSS Support	1.8 V
43	PCI_PER_P	I	PCIe Receive P(HOST RX, WWAN TX)	-
44	I2C_IRQ	O	GNSS Interrupt Request – GNSS Support	1.8 V
45	GND	P	Ground	-
46	SYSCLK	O	26 MHz reference Clock output for external GNSS module	1.8 V
47	PCI_PET_N	O	PCIe Transmit N(HOST TX, WWAN RX)	-
48	TX_BLANKING	O	GNSS Blanking Signal used to indicate 2G Tx burst and LTE band 13 Tx burst.	1.8 V
49	PCI_PET_P	O	PCIe Transmit P(HOST TX, WWAN RX)	-
50	PCIE_PERST_N	I	PCIe reset	3.3V
51	GND	P	Ground	-
52	PCIE_CLKREQ_N	IO	PCIe Clock Request	3.3V
53	PCIE_REFCLK_N	I	PCIe Clock N	-
54	PCIE_WAKE_N	O	PCIe wake up	3.3V

*continued...*

Pin	Signal Name	I/O	Description	Supply
55	PCIE_REFCLK_P	I	PCIe Clock P	-
56	N/C	-	Not connected internally on WWAN M.2	-
57	GND	P	Ground	-
58	N/C	-	Not connected internally on WWAN M.2	-
59	ANTCTL0	O	RF Antenna Tuning Control Signal, GPO0	1.8 V
60	COEX3	O	Wireless Coexistence between WWAN and Wi-Fi/BT modules, GNSS_EXT_FTA	1.8 V
61	ANTCTL1	IO	RF Antenna Tuning Control Signal 1, GPO1	1.8 V
62	COEX2	I	Wireless Coexistence between WWAN and Wi-Fi/BT modules, IDC_UART_RXD	1.8 V
63	ANTCTL2	O	RF Antenna Tuning Control Signal 2, GPO2	1.8 V
64	COEX1	O	Wireless Coexistence between WWAN and Wi-Fi/BT modules, IDC_UART_TXD	1.8 V
65	ANTCTL3	O	RF Antenna Tuning Control Signal 3, GPO3	1.8 V
66	SIM DETECT	I	SIM Card Detection (I) (low active). Pull-up resistor on WWAN M.2 module	1.8 V
67	RESET#	I	Single control to reset WWAN (O)	1.8 V
68	N/C	-	Not connected internally on WWAN M.2	-
69	CONFIG_1	O	Configuration Status WWAN M.2 Connects to GND internally	-
70	3.3V	P	WWAN Supply Pin 3.3 V	-
71	GND	P	Ground	-
72	3.3V	P	WWAN Supply Pin 3.3 V	-
73	GND	P	Ground	-
74	3.3V	P	WWAN Supply Pin 3.3 V	-
75	CONFIG_2	O	Configuration Status WWAN M.2 Connects to GND internally	-

### WWAN M.2 Module Interface Details

This section provides details on the various interfaces available WWAN M.2 modules.

- **Interprocessor Interface (IPC)**

There WWAN M.2 7360 module has three HW interfaces that support interprocessor communications (IPC); Different IPC HW interfaces available on the host interface are:

- USB 2.0 High-speed
- USB 3.2 Super Speed
- PCIe based IPC

The host processor, connected via an IPC interface, has access to the functions of the WWAN card. However on the end M.2 7360 product, PCIe is the only IPC interface that is available for the host.

### USB Features

The USB stack is used as an IPC communication with the Host. It provides the device functionality for CD-ACM and CDC-NCM. M.2 7360 uses two USB IPC interface i.e USB 2.0 and USB3.2. The USB based IPC supports the following features.

- Modem Connection for AT command interface (CDC-ACM)
- Network interface for Ethernet frames (CDC-NCM)
- Suspend /Resume and Remote wake up power saving
- Software download, flashless boot.
- **Modem Connection**

CDC-ACM functions are available to use as an interface for the following functionality:

- AT commands
- 3GPP 27.0101 Multiplexer
- Trace data delivery

#### — **Network Connection**

CDC-NCM functions are available to be used as an interface for network connections. Each CDC\_NCM channel services a single PDN Connections.

The USB 2.0 IPC interface is used only during the production testing and debugging activities. The USB Controller is compliant to the USB 2.0 Specification and with the Link Power Management (LPM) Addendum. LPM introduces a new sleep state (L1) which significantly reduces the transitional latencies between the defined power states; hence, improving the responsiveness of the WWAN platform regarding connecting to the internet (Quick Connect).

**Table 159. USB HS – IPC Interface**

Signal Name	Description	Pin	Direction (WWAN)	Operating Voltage Range
USB_D+	USB Data Plus	7	I, O	Per USB 2.0 Specification
USB_D-	USB Data Minus	9	I, O	

The USB 3.2 solution is based on USB hardware IP that is integrated in the X-GOLD™ 730 baseband chip. The USB Controller is compliant with the USB 3.2 Specification and with the USB 3.2 Super Speed Inter Chip Electrical Specification. This IPC interface is used for M.2 product certification at different operators lab test setup. The ACM / NCM Channels that are available over USB3.2 will be used for issuing the commands for M2 module certification.

**Table 160. USB 3.2 – IPC Interface**

Signal Name	Description	Pin	Direction (WWAN)	Operating Voltage Range
D90_USB30_RXN	USB 3.2 Receiver Signal P	29	O (HOST:TXN)	Per USB 3.2 SS Specification.
D90_USB30_RXP	USB 3.2 Receiver Signal N	31	O (HOST:TXP)	
D90_USB30_TXN	USB 3.2 Transmitter Signal N	35	I (HOST:RXN)	
D90_USB30_TXP	USB 3.2 Transmitter Signal P	37	I (HOST:RXP)	

### PCIe Based IPC

The PCIe solution of the platform is based on a PCIe end point with an integrated PHY supporting

- Compliant to PCIe specification V2.1
- Single Lane with PCIe Gen 1x1 (5 Gb/s) signaling speed(2.5GTps).
- Single functional (Additional PF, VF)
- One Virtual Channel only
- No support for isochrony
- PCIe sideband Wake #
- Additional sideband Device WAKE#
- D0-, D3 hot/cold support
- L1 Substates L1.1 and L1.2
- IPC Protocol according to IMC proprietary specification.

**Table 161. PCIe – IPC Interface**

Signal Name	Description	Pin	Direction (WWAN)	Operating Voltage Range
D100_PCI_PET_N1	PCIe Transmitter Signal N	41	O (HOST:RXN)	Per PCIe Specification
D100_PCI_PET_P1	PCIe Transmitter Signal P	43	O (HOST:RXP)	
D100_PCI_PER_N1	PCIe Receiver Signal N	47	I (HOST:TXN)	
D100_PCI_PER_P1	PCIe Receiver Signal P	49	I (HOST:TXP)	
D100_PCI_REFCLK_N1	PCIe reference clock N	53	I	
D100_PCI_REFCLK_P1	PCIe reference clock P	55	I	

### • USIM Interface

The USIM interface is compatible with the ISO 7816-3 IC Card standard on the issues required by the GSM 11.12 and GSM 11.18 standard.

Both 1.8 V and 3 V SIM Cards are supported.

A few comments on the SIM\_DETECT signal

- An external pull-up resistor is connected to SIM\_DETECT on the WWAN M.2 module.
- When a SIM is inserted, SIM\_DETECT will be high.
- When a SIM is removed or not present, SIM\_DETECT will be low.
- The host does not need to drive this signal. It can be tri-stated.

**Table 162. (U)SIM Interface Signals**

Signal Name	Description	Pin	Direction (WWAN)	Voltage Level
UIM_CLK	Clock SIM Card	32	O	1.8 V/3.0 V
UIM_DATA	Input/ Output SIM Card	34	I, O	1.8 V/3.0 V
UIM_RESET	Reset signal for SIM card	30	O	1.8 V/3.0 V
USIM_PWR	1.8 V/3 V Supply for SIM Card	36	O	1.8 V/3.0 V
SIM Detect	SIM Card Detection	66	I	1.8 V

### SIM Design Recommendations

The following design guidelines are recommended for the SIM card socket mounted on the host system:

- Length of the traces UIM\_CLK, UIM\_DATA, and UIM\_RESET should not exceed 10 cm.
- UIM\_DATA is a sensitive open-drain bi-directional signal. It should not be mounted beside the UIM\_CLK signal for long distances. It is recommended to place the UIM\_RST trace between UIM\_DATA and UIM\_CLK to provide isolation. If the traces are run a long distance, surround the UIM\_DATA with ground to shield from system noise and UIM\_CLK.
- The rise time for UIM\_DATA should not exceed 1  $\mu$ s per the 3GPP specification. High input capacitance may increase rise time and lead to certification failure.
- Keep UIM traces with low capacitance between each other and to GND
- An ESD component with high capacitance may increase rise time.
- The pull-up current cannot be increased to speed up rise time, because the pull-up current must not exceed 1 mA including any crosstalk.
- Pull-up current is defined by the 6.8 k $\Omega$  pull-up resistor (to USIM\_PWR) on the WWAN M.2 module, plus 200  $\mu$ A from the baseband chip is approximately 0.8 mA.
- Place a decoupling capacitor close to the SIM card socket.

- **GNSS Interface**

WWAN M.2 module will provide a GNSS interface for GNSS chip on the WWAN M.2 module.

### Internal GNSS Interface

The WWAN M.2 module incorporates the WCS2100 Single-Chip GNSS Device, which supports GPS, GLONASS, BeiDou and Galileo Constellation GNSS.

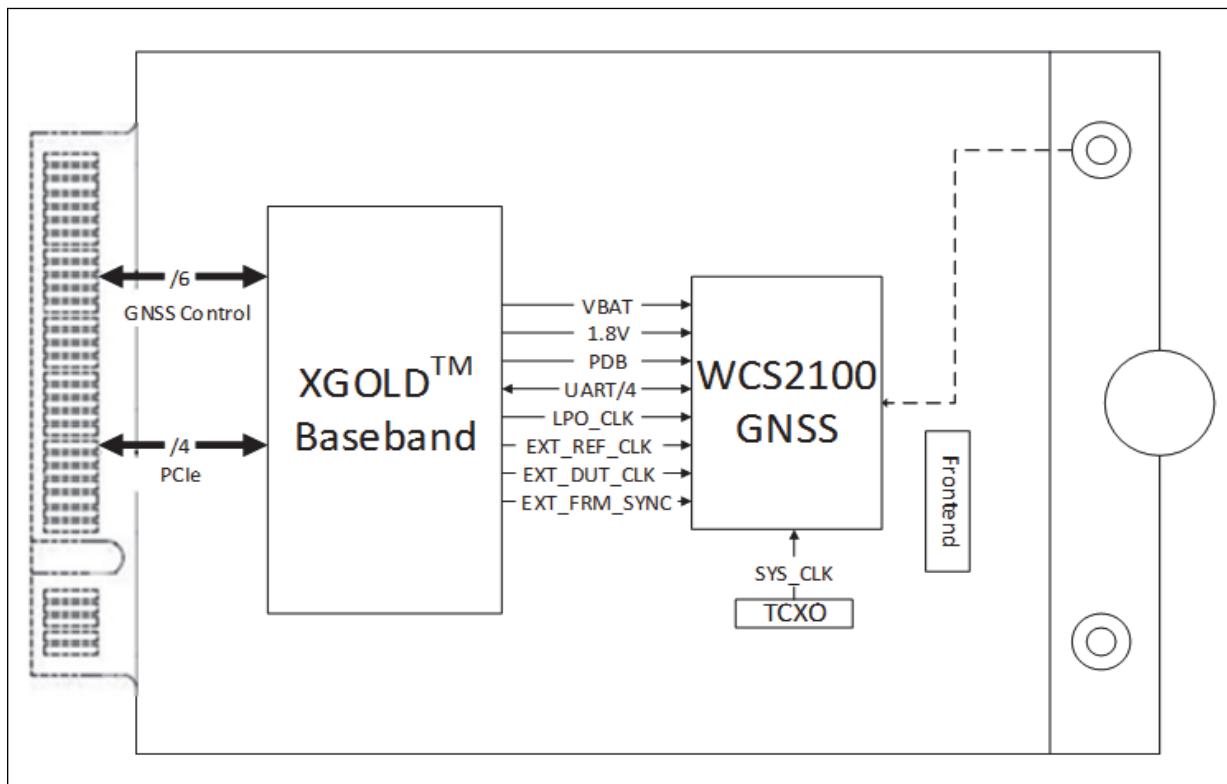
The GNSS receiver covers the GPS L1 C/A and GLONASS L1 bands. GPS L2 is not supported. A UART interface is used by the X-GOLD™ Communications Processor on the WWAN module to communicate with the WCS2100 device. The solution offers best-in-class acquisition and tracking sensitivity, TTFF and accuracy.

The GNSS device supports several different power management modes which gives the lowest possible energy usage per fix. The pre-calculated location data will be sent over the PCIe host interface over AT port.

#### — **GNSS General Features**

- Autonomous GPS / GLONASS / Galileo / Beiduo
- Assisted GNSS Using SUPL 1.0/2.0
  - MS Assisted positioning ( SET Initiated )
  - MS Based positioning ( SET Initiated )
- SUPL 2.0 Feature Sets
  - Version Negotiation
  - Periodic Triggers
  - Area Event Triggers (SET Initiated)
  - Application ID
  - Enhanced Cell Id
  - Multiple Location IDs
  - Location Transfer to 3rd Party
  - Location Request to another SET

A diagram of the GNSS connections on the WWAN M.2 module is shown below. This diagram identifies the signals between the X-GOLD™ baseband and GNSS devices along with the PCIe and GNSS signals available to the host at the card interface.

**Figure 166. GNSS Connections and Interface**

A description of the signals between the X-GOLD™ baseband and the WCS2100 interface are defined in below table.

**Table 163. X-GOLD™ Baseband to GNSS Interface Signals**

Signal	Description
VBAT	Battery Supply
1.8V	1.8 V Supply provided from X-GOLD™ Baseband
UART	The data and control I/F between the X-GOLD™ baseband and the GNSS device is over a 4 wire UART interface which include CTS/RTS handshaking.
PDB	X-GOLD™ baseband uses this signal to control Power-on/reset of the GNSS device
LPO_CLK	X-GOLD™ baseband provides a permanently active 32 kHz clock to the GNSS device
EXT_REF_CLK	X-GOLD™ baseband provides a 26 MHz clock to the GNSS device for frequency aiding.
EXT_DUT_CYCLE	X-GOLD™ baseband provides this signal to notify the GNSS device of that GSM Tx activity (PA Blanking)
EXT_FRM_SYNC	X-GOLD™ baseband provides a strobe signal to the GNSS device to allow fine time assistance based on 3GPP cell timing.

The GNSS signals available to the host at the WWAN module interface to support GNSS operation are shown in below table.

**Table 164. GNSS Module Interface Signals**

Signal Name	Description	Pin	Direction (WWAN)	Voltage Level
SYSCLK	Synchronization Clock	46	O	1.8 V
TX_BLANKING	TX Blanking – Active High when WWAN M.2 is transmitting.	48	O	1.8 V
GNSS_DISABLE#	GNSS Disable <ul style="list-style-type: none"> <li>— High: GNSS function is determined by AT command.</li> <li>— Low: GNSS function is disabled.</li> </ul> GNSS_DISABLE# pin has a pull-up resistor on the WWAN M.2 module	26	I	1.8 V
GNSS_EXT_FTA	GNSS_EXT_FTA – GNSS Fine Tune Aiding. Fine Tune aiding is a single on-off pulse output, and is used to set precise time in order to narrow the satellite search range. This feature will speed up the first satellite acquisition.	60	O	1.8 V

- System Control Interface**

The system control interface is used to control the power-up and reset of the WWAN module. There are additional control signals to disable the radio, drive an LED as a status indicator, an output to wake the host processor, and an input for body SAR.

#### Power On and Reset

The host processor has two signals that can be used to power on and reset the modem. Powering off the modem is accomplished through an AT command.

**Table 165. Power On and Reset Signals**

Signal Name	Description	Pin	Direction (WWAN)	Voltage Level
FULL_CARD_POWER_OFF#	Modem Power-on: For Tablet based designs only; this signal is used for power off control of X-GOLD™ Baseband IC. WWAN M.2 module <ul style="list-style-type: none"> <li>— Logic Low: WWAN M.2 Off</li> <li>— Logic High: WWAN M.2 Power On</li> </ul> This pin has an internal pull-down resistor. Ultrabook Designs: Ultrabook host should deliver a 1.8 V signal to turn on the module. If 1.8 V is not feasible, recommend using a 10 kΩ series resistor connected to 3.3 V.	6	I	3.3 V
RESET#	Reset the WWAN system. This signal is used to reset the module. This signal is part of the modem rigorous power-off procedure. The host will first assert this signal, followed by assertion of: <ul style="list-style-type: none"> <li>— FULL_CARD_POWER_OFF# signal (for Ultrabook/Tablet)</li> <li>— Switch off 3.3V regulator (for Ultrabook)</li> </ul> Asserting RESET first is to trigger Baseband internal state machine to run the reset of the whole modem system. But some blocks like the PMU and PCL are excluded from this reset. Asynchronous, active low signal. When active, the Baseband will be placed in a power-on reset condition.	67	I	1.8 V

### Host Radio Disable Operation

An additional control signal is used to disable the radio on the module.

Signal W\_DISABLE# is provided to allow users to disable, via a system-provided switch, the add-in card's radio operation in order to meet public safety regulations or when otherwise desired. Implementation of this signal is required for systems and all add-in cards that implement radio frequency capabilities.

The W\_DISABLE# signal is an active low signal that when driven low by the system shall disable radio operation. The assertion and de-assertion of the W\_DISABLE# signal is asynchronous to any system clock. All transients resulting from mechanical switches need to be de-bounced by the host system and no further signal conditioning will be required. When the W\_DISABLE# signal is asserted, all radios attached to the add-in card shall be disabled. When the W\_DISABLE# is not asserted or in a high impedance state, the radio may transmit if not disabled by other means such as software.

The operation of the W\_DISABLE# Signal is:

- Enable, ON (1.8 V): The radio transmitter is to be made capable of transmitting.
- Disable, OFF (low): The radio transmitter(s) is to be made incapable of transmitting.

Standard TTL signaling levels shall be used making it compatible with 1.8 V and 3.3 V signaling.

W\_DISABLE# pin has an internal pull-up on the WWAN M.2 module.

**Table 166. Radio Disable Signal**

Signal Name	Detailed Description	Pin	Direction (WWAN)	Voltage Level
W_DISABLE#	<p>Disable Radio. This active low signal allows the host to disable the WWAN M.2 radio operation in order to meet public safety regulations or when otherwise desired.</p> <ul style="list-style-type: none"> <li>— Logic Low: WWAN M.2 RF Off</li> <li>— Logic High: function is determined by Software (AT Command).</li> </ul> <p>If this pin is left un-connected, functionality is controlled by software.</p> <p>Care should be taken not to activate this pin unless there is a critical failure and all other methods of regaining control and/or communication with the WWAN M.2 module have failed.</p>	8	I	Compatible with 1.8 V/3.3 V

Standard TTL signaling levels will be used.

**Table 167. Host Radio Disable Interface (W\_DISABLE#)**

Requirement	Detailed Description
Radio disable duration	<p>On reception of a HW or SW disable signal, the WWAN module will initiate within one second the mandatory cellular procedures (which are dependent on current state) for disconnecting from the cellular network. The time taken to complete the procedures will be dependent on external factors including but not limited to: 3G/4GPP</p> <p><i>continued...</i></p>

Requirement	Detailed Description
	specifications, network implementation, radio conditions, etc. Once those procedures are complete, the WWAN module will switch off the RF.
Radio enable duration	On reception of a hardware or software enable signal the WWAN module will initiate within one second the mandatory cellular procedures for connecting to the cellular network.
Radio enable during selective suspend	If radio is disabled due to W_DISABLE# assertion and WWAN module is in selective suspend, then W_DISABLE# de-assertion shall be detected by WWAN module and the module shall initiate exit from selective suspend.

### LED Interface – Status Indicator

An LED will be used to provide status indications to users via system provided indicators.

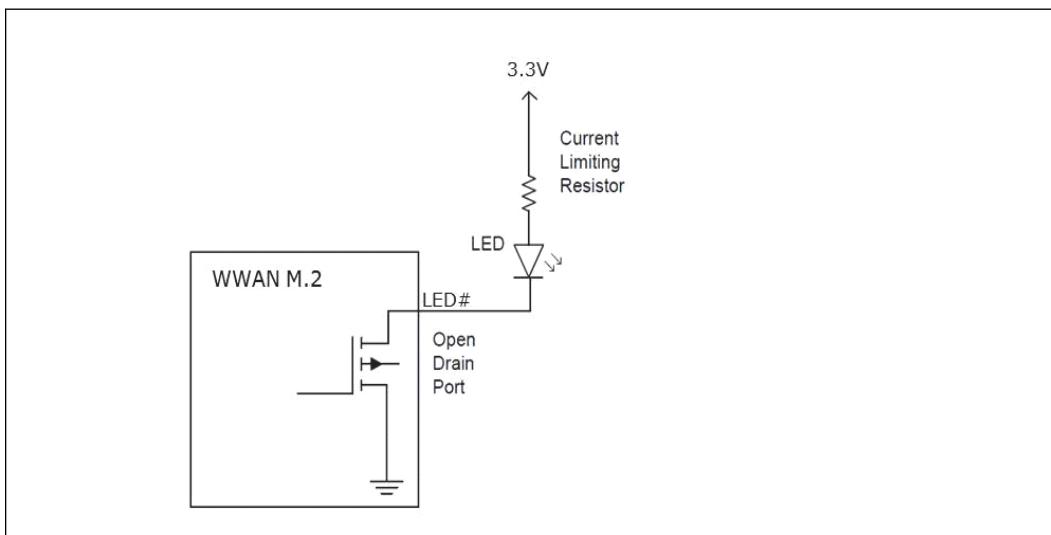
LED#1 (pin 10) is an active low open drain output signal intended to drive system-mounted LED indicators. These signals shall be capable of sinking to ground a minimum of 9.0 mA at up to a maximum VOL of 400 mV. The LED has four defined states.

**Table 168. LED#1 Signal**

Signal Name	Detailed Description	Pin	Direction (WWAN)	Voltage Level
LED#1	LED Status Indicator	10	O (OD)	3.3 V

Below figure is an example of how an LED indicator is typically connected in a platform/system using 3.3 V. The series resistor can be adjusted to obtain the desired brightness.

**Figure 167. Typical LED Connection**



The indication protocol for the LED is shown below.

**Table 169. LED State Indicator**

State	Definition	Characteristics	WWAN State
OFF	The LED is emitting no light	-	Not powered
ON	The LED is emitting light in a stable non-flashing state	-	Powered registered but not transmitting or receiving

### Wake on WWAN Signal

An output signal is available to wake the host system, WAKE\_WWAN#. This is an active low, open-drain output.

This output requires a pull-up resistor on the host system.

Hardware support for WAKE\_WWAN# is available; however, there is no software support.

**Table 170. Wake on WWAN Signal**

Signal Name	Detailed Description	Pin	Direction (WWAN)	Voltage Level
WAKE_WWAN#	Used by WWAN M.2 module to wake the host. Active Low, Open Drain output	23	O (OD)	1.8 V

**Table 171. DPR#/ SAR Support Signal**

Signal Name	Detailed Description	Pin	Direction (WWAN)	Voltage Level
DPR	Dynamic power reduction.	25	I	1.8/3.3 V

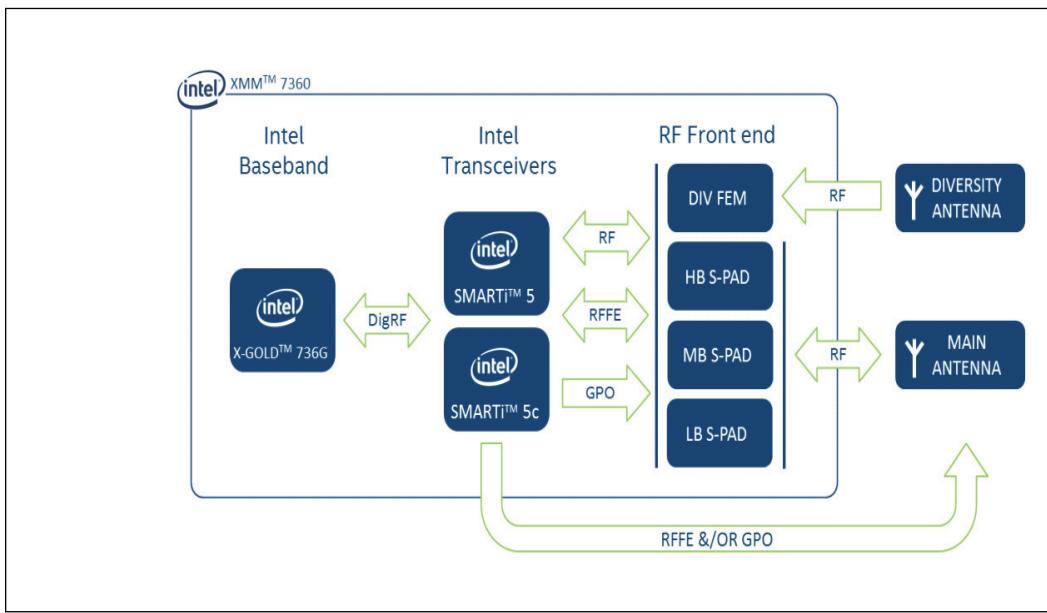
- **Tunable Antenna Control Interface**

In notebook platforms, since the WWAN antennas are usually located on the top of the lid, there is a long RF mini-coax cable that can be up to 60 cm long between the antenna and WWAN module, it is preferred to use switches/tunable components directly on the antenna for antenna band switching/tuning to improve efficiency.

On select WWAN M.2 modules, four (4) GPIOs are available on the host interface that can be connected to an external antenna switch, to load the antenna with different impedances, configuring the different frequency responses for the main antenna. A sample block diagram depicting the antenna control signal connections to the antenna switch is shown in below figure.

Intel's current antenna control solution offers an open loop control solution. The WWAN M.2 modem expects the AP to provide the antenna profile detection and through a pre-defined API, notify the WWAN M.2 modem with the correct antenna profile. The WWAN M.2 modem then applies the proper antenna profile data accordingly.

**Figure 168. Antenna Control – Connections Detail**



The electrical specification for the antenna control GPOs are shown in below table.

**Table 172. Tunable Antenna Control Signals**

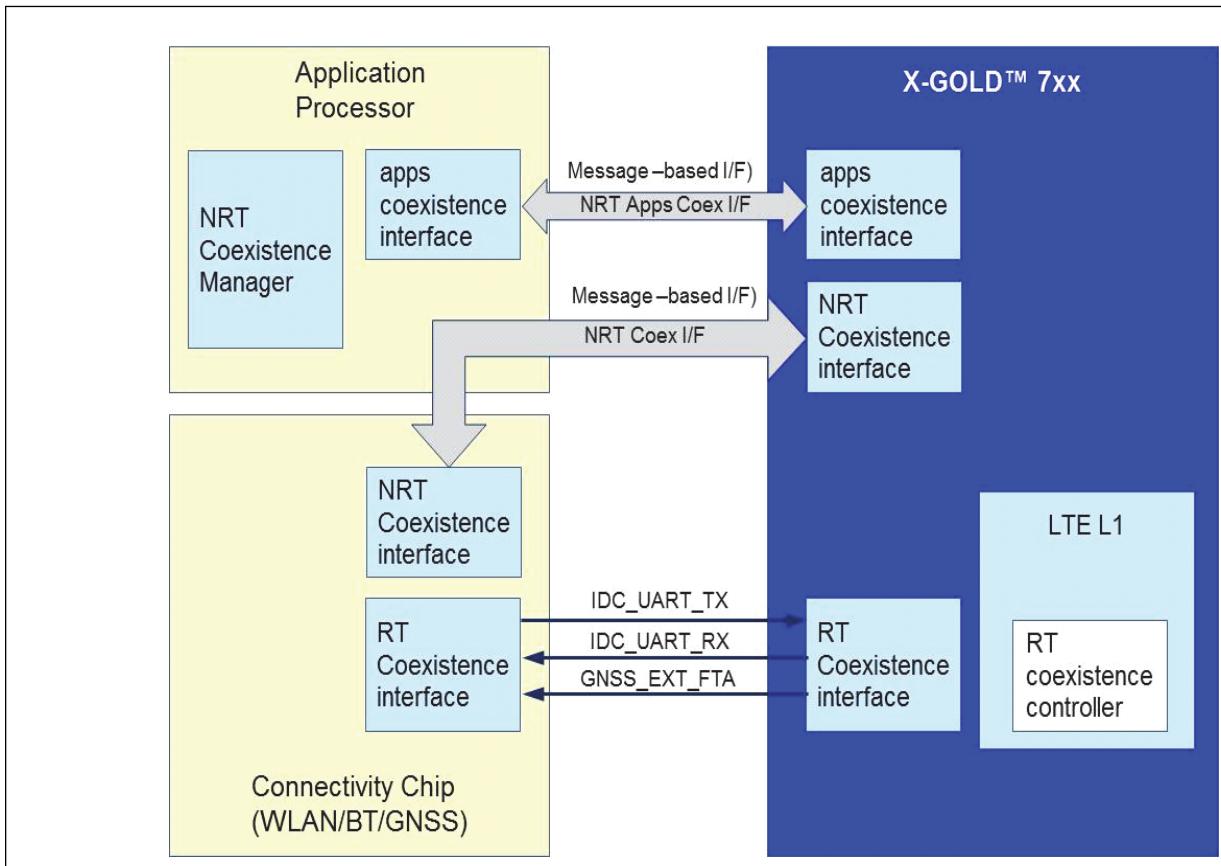
Signal Name	Description	Direction (WWAN)	Voltage Level
ANTCTL0	Antenna Control 0	O	1.8 V
ANTCTL1	Antenna Control 1	O	1.8 V
ANTCTL2	Antenna Control 2	O	1.8 V
ANTCTL3	Antenna Control 3	O	1.8 V

- **In-Device Coexistence Interface**

As more and more radios are added to PC Ultrabook™ and tablet platforms, the sources RF interference increases significantly as multiple radios will have overlapping transmissions and receptions. This problem will increase further as overlapping bands continue to be rolled out; WIFI, BT, WWAN will all use overlapping bands from 2300 MHz to 2600 MHz.

In-Device Coexistence is a feature which improves the user experience and maximizes throughput and Quality of Service of connectivity systems (WLAN, BT and GNSS) when these radios are simultaneously running with the WWAN M.2 modem.

A diagram of the In-Device Coexistence architecture is shown in below figure.

**Figure 169. In-Device Coexistence Architecture**

### Seamless Co-Running

In-Device-Coexistence primarily aims at avoiding interference between radio systems to allow seamless co-running where LTE and WLAN/BT/GNSS ensuring their maximum throughput and performance. To do so, a Non Real Time (NRT) Coexistence Manager is implemented on the AP. The NRT coexistence manager centralizes LTE, WLAN, BT and GNSS information and performs interference avoidance mechanisms, selecting interference-safe frequency configurations whenever possible. The NRT coexistence manager is also in charge of enabling some Real Time (RT) coexistence mechanisms when NRT mechanisms are not sufficient to guarantee seamless co-running of LTE and connectivity systems (WLAN, BT, and GNSS).

### Inter-System Synchronization

For the cases where co-running of LTE and connectivity systems cannot be achieved, a Real Time (RT) coexistence controller is implemented in the LTE Layer-1 subsystem. The RT coexistence controller is in control of the RT coexistence interface, which is exposed to the connectivity chip. The RT coexistence controller exploits real time information received from the LTE Layer-1 subsystem and from the connectivity chip to coordinate LTE and connectivity "in the air" activities. The coordination function protects LTE traffic while optimizing the throughput and availability of WLAN/BT/GNSS. When operating in this mode,

the connectivity systems have reduced capability since they access the medium when LTE is inactive, or when their respective operations do not impact each other significantly.

The Non Real-Time mechanism implements a messaging based interface, formatted as AT commands that are passed to the AP host over the IPC interface (USB). The host software will also be responsible for initializing the Real-Time mechanism.

The Real-Time mechanism consists of 3 signals which allow the synchronization of multiple TX and RX events. The signals to support real Time coexistence are listed in below table.

If the coexistence signals are not used by the host system, they should not be connected.

**Table 173. Coexistence – Hardware Synchronization Signals**

Signal Name	Description	Pin	Direction (WWAN)	Voltage Level
COEX3	<b>GNSS_EXT_FTA</b> – GNSS Fine Tune Aiding. Fine Tune aiding is a single on-off pulse output, and is used to set precise time in order to narrow the satellite search range. This feature will speed up the first satellite acquisition. This signal is also listed in for use by the GNSS solution.	60	O	1.8 V
COEX2	<b>IDC_UART_RXD</b> – UART_RXD_MRST – UART Receive input for Real-time Coexistence support	62	I	1.8 V
COEX1	<b>IDC_UART_TXD</b> – UART_TXD_MTSR - UART Transmit output for Real-time Coexistence support	64	O	1.8 V

- **Power Supply Interface**

The WWAN M.2 modules require the host to provide the 3.3 V power source. The voltage source is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card.

The 3.3 V power and ground pins are listed in below table.

**Table 174. Power and Ground Signals**

Power Pins	Description
2, 4, 70, 72, 74	3.3 V Supply
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	Ground

- **Configuration Pins**

There are four configuration pins on the WWAN M.2 module to assist the host identifying the presence of an Add-In card in the socket.

On the M.2 WWAN module, pins CONFIG\_0...3 are configured as shown in below table.

All configuration pins can be read and decoded by the host platform to recognize the indicated module configuration and host interface supported. On the host side, each of the CONFIG\_0...3 signals needs to be fitted with a pull-up resistor.

**Table 175. WWAN M.2 Configuration Pins**

Signal Name	Description	Pin	Direction (WWAN)	Voltage Level
CONFIG_0	This signal is not connected on the WWAN M.2 module.	21	O	-
CONFIG_1	Tied to Ground on the WWAN M.2 module at the M.2 interface connector.	69	O	0 V
CONFIG_2	Tied to Ground on the WWAN M.2 module at the M.2 interface connector.	75	O	0 V
CONFIG_3	Tied to Ground on the WWAN M.2 module at the M.2 interface connector.	1	O	0 V

- **Audio Pins (Reserved)**

There are four signals on the host interface that are reserved to support a digital audio interface. This is for future development, all existing WWAN M.2 modules do not support audio; therefore, these signals should be left unconnected at the host to avoid any contention.

**Table 176. Audio Signals (Future Development)**

Signal Name	Description	Pin	Direction (WWAN)	Voltage Level
AUDIO0	PCM Clock (I2S_CLK)	20	IO	1.8 V
AUDIO1	PCM In (I2S_RX)	22	I	1.8 V
AUDIO2	PCM Out (I2S_TX)	24	O	1.8 V
AUDIO3	PCM Sync (I2S_WAO)	28	IO	1.8 V

- **No Connect Pins**

The WWAN M.2 has several No Connect pins. The pins are not connected on the WWAN M.2 module.

**Table 177. No Connect Pins**

Pins	Description
38, 56, 58, 68	Do Not Connect Pins
12, 13, 14, 15, 16, 17, 18, 19	Slot-key

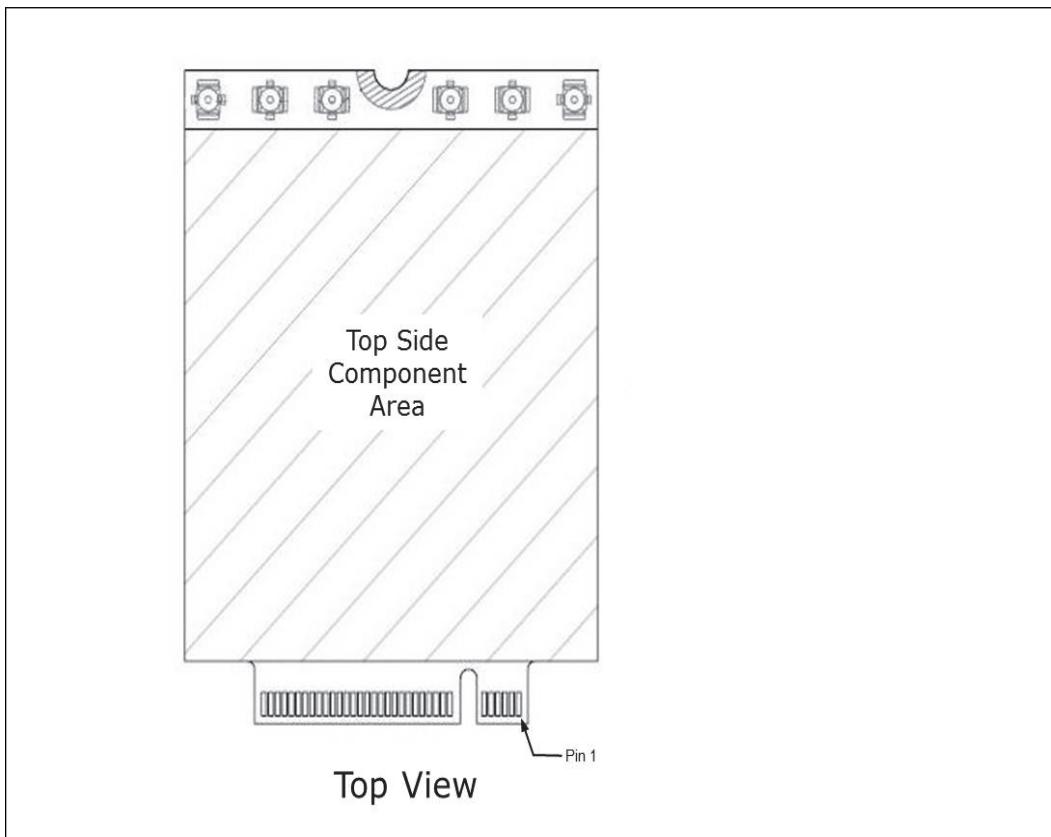
- **Antenna Interface**

The WWAN M.2 module has space for six antenna connectors; yet, as a minimum, only two will be populated to support a main Rx/Tx antenna and a secondary antenna that will be multiplexed between the Diversity receiver and GPS receiver (if applicable).

The antenna signals are not available at the host interface but have their own connectors. A diagram on the WWAN M.2 module with the location of the RF connectors appears in below figure.

**Table 178. Antenna Requirements**

Requirement	Detailed Description
Connection to module	The connector of WWAN antenna cable is Hirose W.FLT or equivalent
Multi-band single antenna	Single antenna has to support all bands of WWAN module specified in the Product Features.
Rx Diversity antenna	Diversity antenna has to support all bands WWAN module specified in the Product Features in addition GPS/GLONASS frequencies.
GPS Antenna	The GPS antenna will share the Diversity antenna (Secondary Antenna) connector.

**Figure 170. RF Antenna – Coaxial Connector Location**


### Power Delivery Requirements

- **Electrical Parameters (3.3 V Power Supply)**

The WWAN M.2 modules utilize a single regulated power rail of 3.3 V provided by the host platform. There is no other VDDIO like pin and the WWAN M.2 module is responsible for generating its own I/O voltage source using the 3.3 V power rail. This 3.3 V voltage rail source on the platform should always be on and available during the system's stand-by/suspend state to support the wake event processing on the communications card.

There are five power pins on the host interface, pins 2, 4, 70, 72, and 74.

The requirements of the regulated 3.3 V power supply provided by the host platform are listed below.

**Table 179. WWAN M.2 Module Power Delivery Requirements – Ultrabook**

Requirement	Detailed Description
Supply Voltage	3.3 V at the Card connector will be within 5% tolerance on the motherboard.
Peak Current	The host board shall provide 2.5 A peak current.
Average Current	Average max current of 1.1 A will be supported.
Max in-rush Current	Max module in-rush current of 5.1 A will be supported.
Power Pin Connections	The power pins specified in WWAN card #'s, 2, 4, 70, 72, and 74 will be connected to 3.3 V supply and WWAN configuration pins 1 and 69 will be connected to ground.

**Electrical Parameters - Host Interface Signals****Table 180. Electrical Parameters – Host Interface Signals**

Signal	Pin	Description	I/O	Voltage Domain (V) (VDD_IO)	DC Characteristics (V)		
					Min	Typical	Max
FULL_CARD_POWER_OFF #	6	Power On/Off WWAN M.2 Module	I	3.3	-0.3	0/3.3	3.465
RESET#	67	Reset WWAN M.2 Module	I	1.8	-0.3	0/1.8	2.3
LED#1	10	WWAN M.2 Status Indicator	O (OD)	3.0	Open-Drain Output, Host requires pull-up resistor		
W_DISABLE#	8	WWAN M.2 Disable	I	1.8	-0.3	1.8	2.1
WAKE_WWAN#	23	WWAN wake Host	O	1.8	-0.3	0/1.8	3.0
DPR	25	Body SAR Detection	I	1.8	-0.3	0/1.8 0/3.3	3.465
USB ( D+/D- )	7, 9	USB D+/D- 2.0 High-speed	I/O	-	Per USB 2.0 Specification		
USB30_TX (N/P)	35, 37	USB3.2 SS Transmit	O	-	Per USB 3.2 SS specification		
USB30_RX (N/P)	29, 31	USB3.2 SS Receive	I	-			
SIM_DETECT	66	SIM Card Detection	I	1.8	-0.3	0/1.8	2.1
UIM_CLK	32	SIM Card Clock	O	1.8/ 3.0	-0.3	0/1.8 0/3.0	3.3 3.3
UIM_RESET	30	SIM Card Reset	O	1.8 / 3.0	-0.3	0/1.8 0/3.0	3.3 3.3
UIM_DATA	34	SIM Card DATA	I/O	1.8/ 3.0	-0.3	0/1.8 0/3.0	3.3 3.3
UIM_PWR	36	SIM Card Power	O	1.8/ 3.0	1.62/2.7	1.8/ 3.0	1.98 3.3
PCI PET (N/P)	47, 49	PCIe Transmit	O	-	Per PCIe G1 specification		
PCI_PER (N/P)	41, 43	PCIe Receive	I	-			
PCI_REFCLK (N/P)	53,	PCIe Reference Clock	I	-			

*continued...*

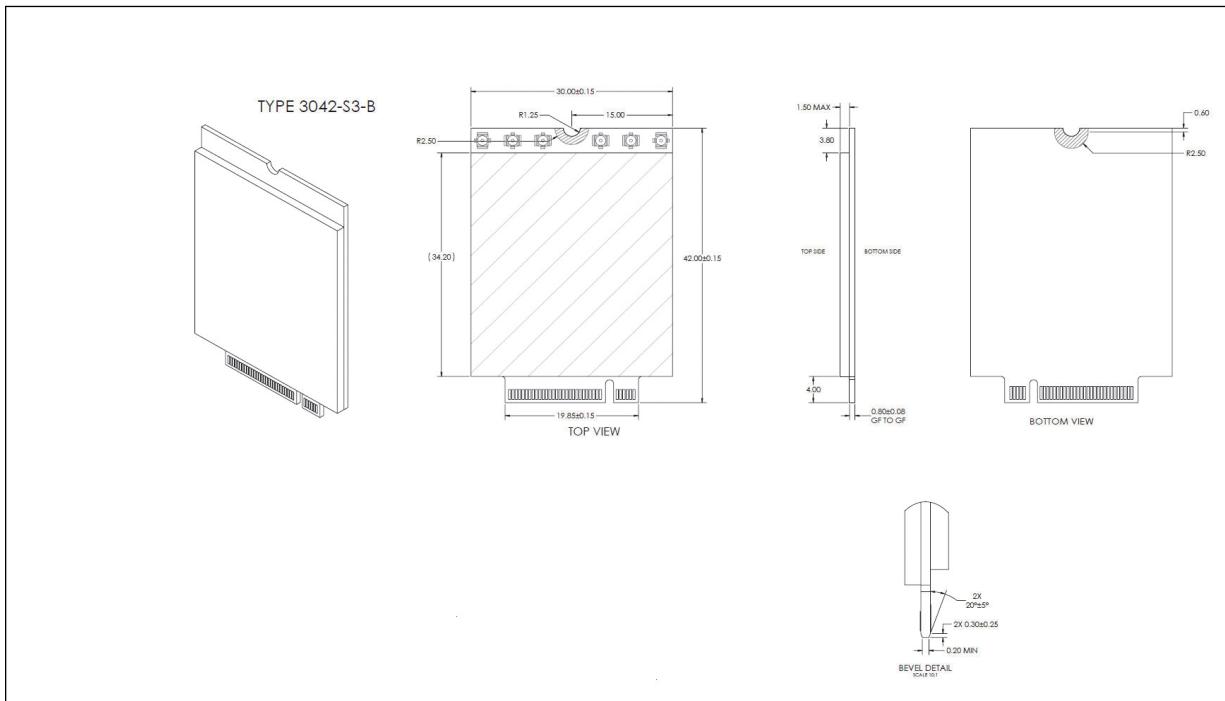
Signal	Pin	Description	I/O	Voltage Domain (V) (VDD_IO)	DC Characteristics (V)		
					Min	Typical	Max
	55						
PCIE_PERST_N	50	PCIe reset	I	3.3	-0.3	0/3.3	3.465
PCIE_CLKREQ_N	52	PCIe clock request	O	3.3	-0.3	0/3.3	3.465
PCIE_WAKE_N	54	PCIe wake up	O	3.3	-0.3	0/3.3	3.465
I2C_SCL	40	GNSS – I2C Clock	I/O	1.8	-0.3	0/1.8	2.1
I2C_SDA	42	GNSS – I2C Data	I/O	1.8	-0.3	0/1.8	2.1
I2C_IRQ	44	GNSS – I2C Interrupt	I	1.8	-0.3	0/1.8	2.1
CLKOUT0	46	GNSS – 26 MHz Clock Synchronization	O	1.8	-0.3	0/1.8	2.1
TX_BLANKING	48	GNSS – TX Blanking	O	1.8	-0.3	0/1.8	2.1
GNSS_DISABLE#	26	Disable GNSS	I	1.8	-0.3	0/1.8	2.1
ANTCTL[3:0]	59, 61, 63, 65	Antenna Tuning Signals – RF Engine	O	2.3	-0.3	0/1.8	2.3
COEX[3:1]	60, 62, 64	RF Coexistence Synchronization	I/O	1.8	-0.3	0/1.8	2.1

### WWAN Card Type 3042-S3-B

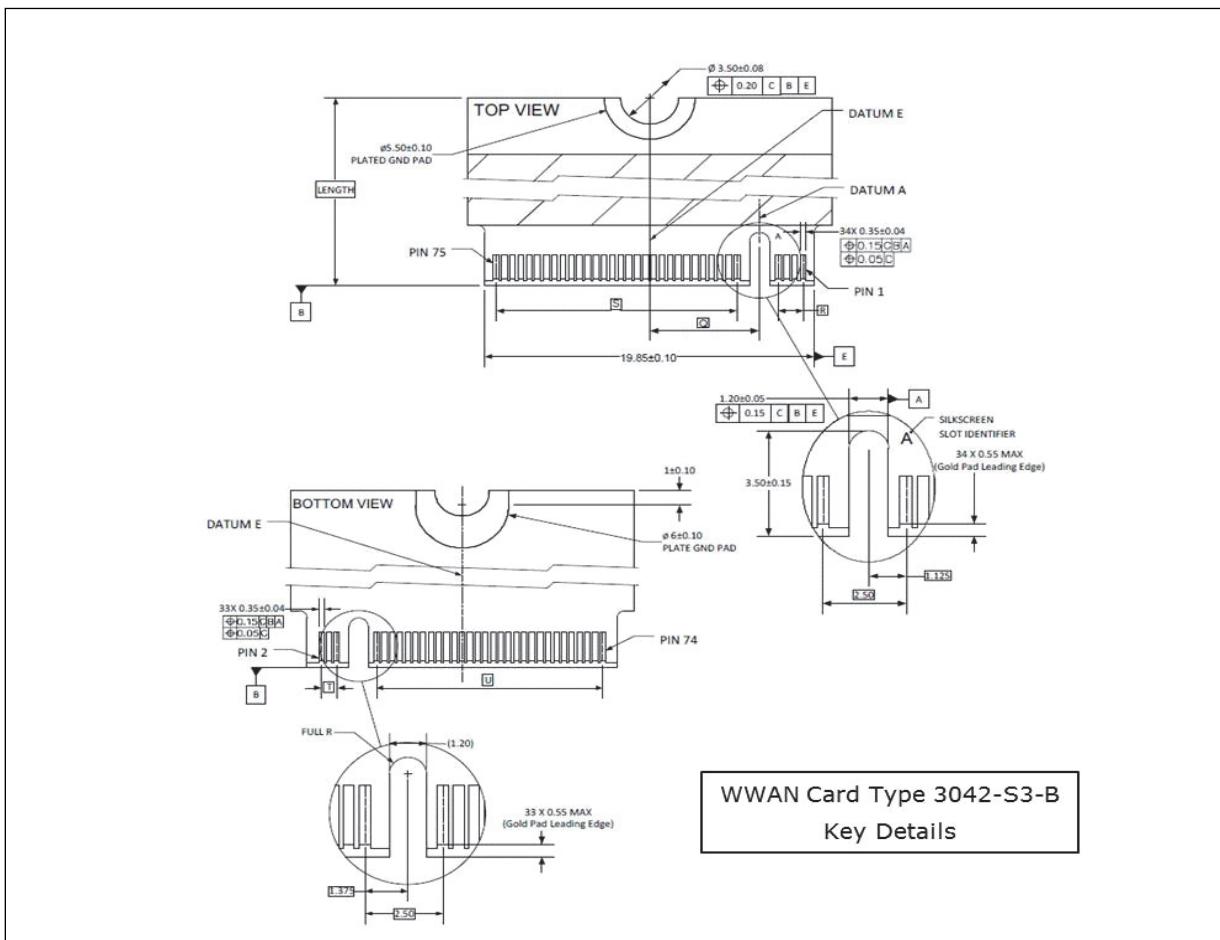
- Mechanical Dimensions**

The mechanical dimensions of WWAN Card Type 3042 are shown in below figures.

The WWAN card is 30 mm x 42 mm. The height is 1.5 mm from the top of the PCB to the top of the outside shield. There are a total of 75 pins; however 8 pins are lost to support the slot-key. All components are mounted on the top side.

**Figure 171. WWAN Card 3042 Mechanical Dimensions**

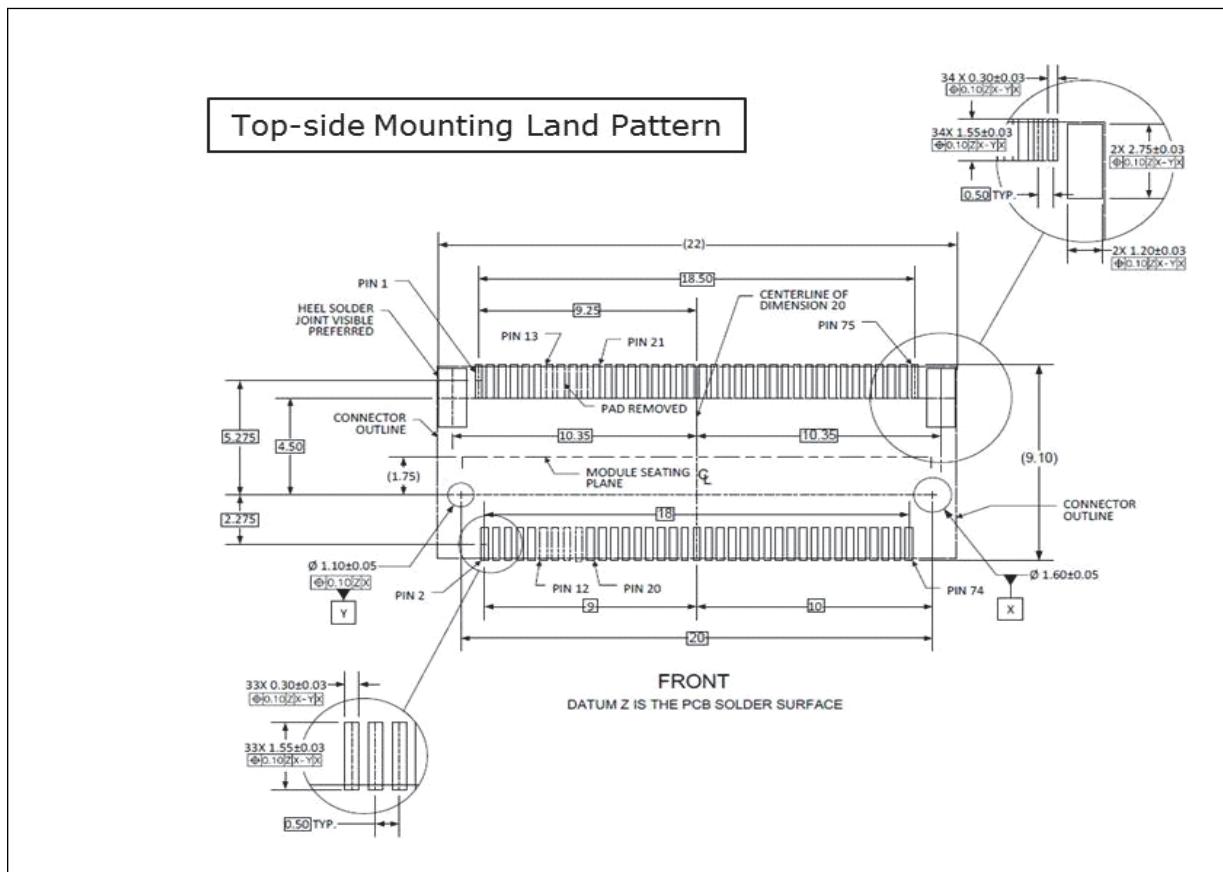
**Figure 172. WWAN Card 3042 Slot-key Details**



- **Land Pattern**

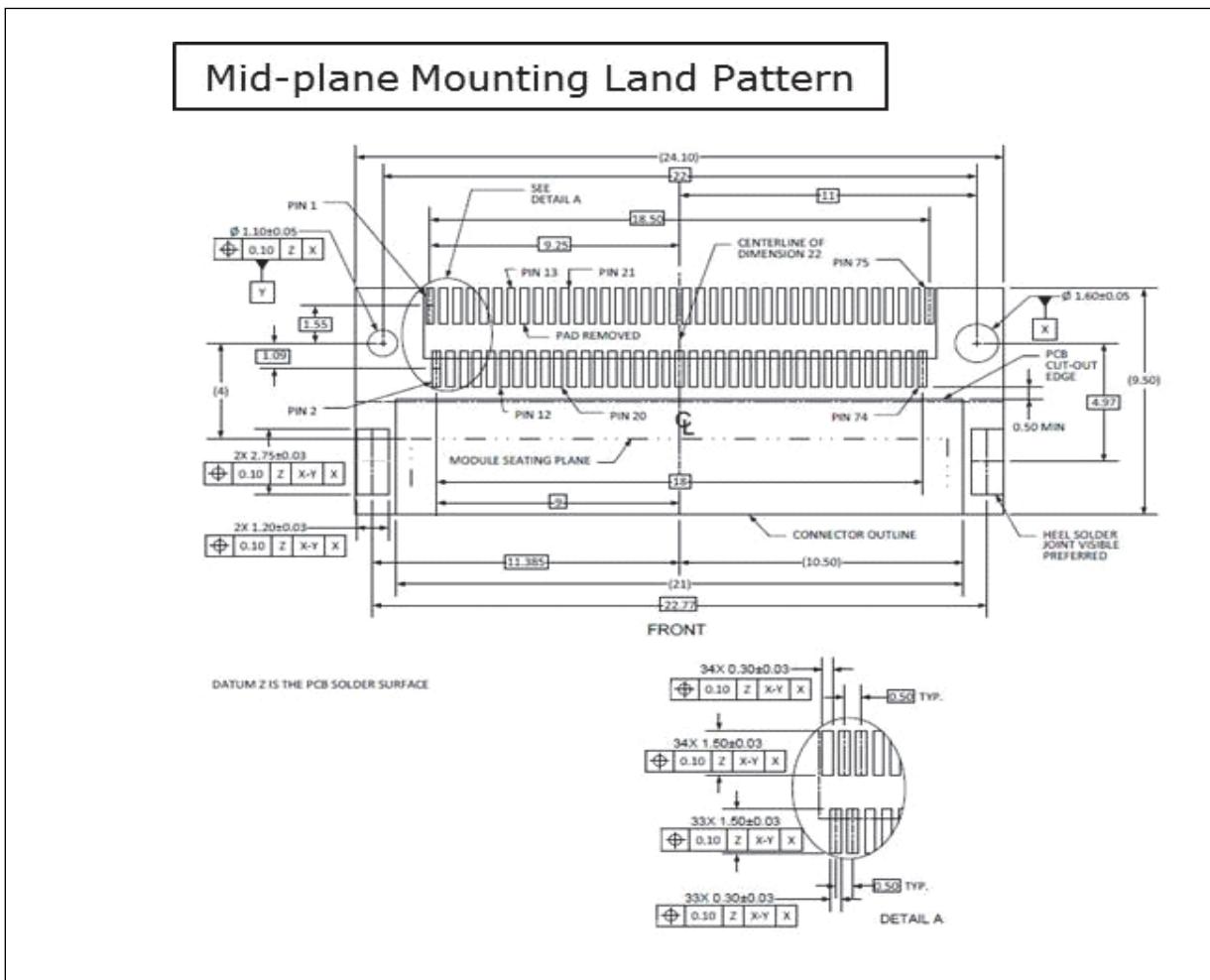
Below figure illustrates a typical land pattern for a top-mount connector with the slot-key removed.

Figure 173. WWAN Card Type 3042 Top-Side Mounting Land Pattern



Below figure illustrates a typical mid-plane (in-line) land pattern with slot-key removed.

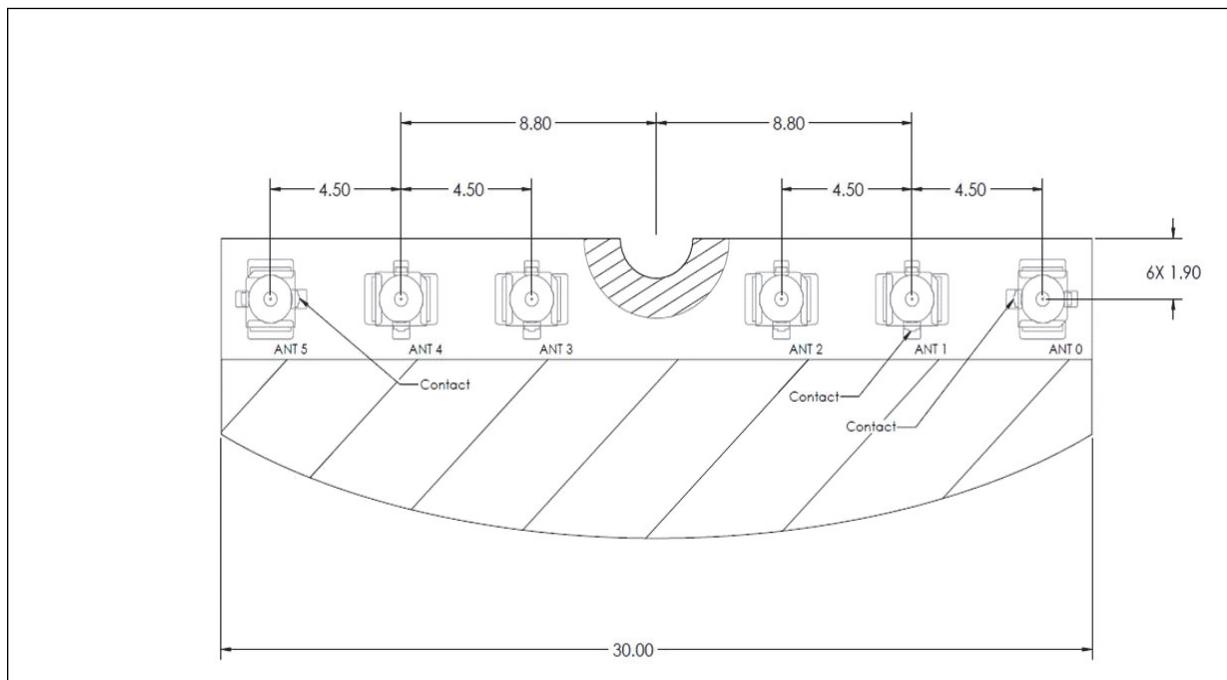
**Figure 174. WWAN Card 3042 Mid-plane Land Pattern with Slot-key Removed**



- **Antenna Connector Locations**

Below figure illustrates the locations for the antenna locations on the M.2 module.

Below table identifies the specific antenna ports utilized on the WWAN M.2 LTE Advanced modules.

**Figure 175. Antenna Connector Location****Table 181. Antenna Connector Assignment**

Antenna	Interface
0	TBD
1	WWAN Main Tx/Rx
2	TBD
3	TBD
4	Diversity/ GPS
5	TBD

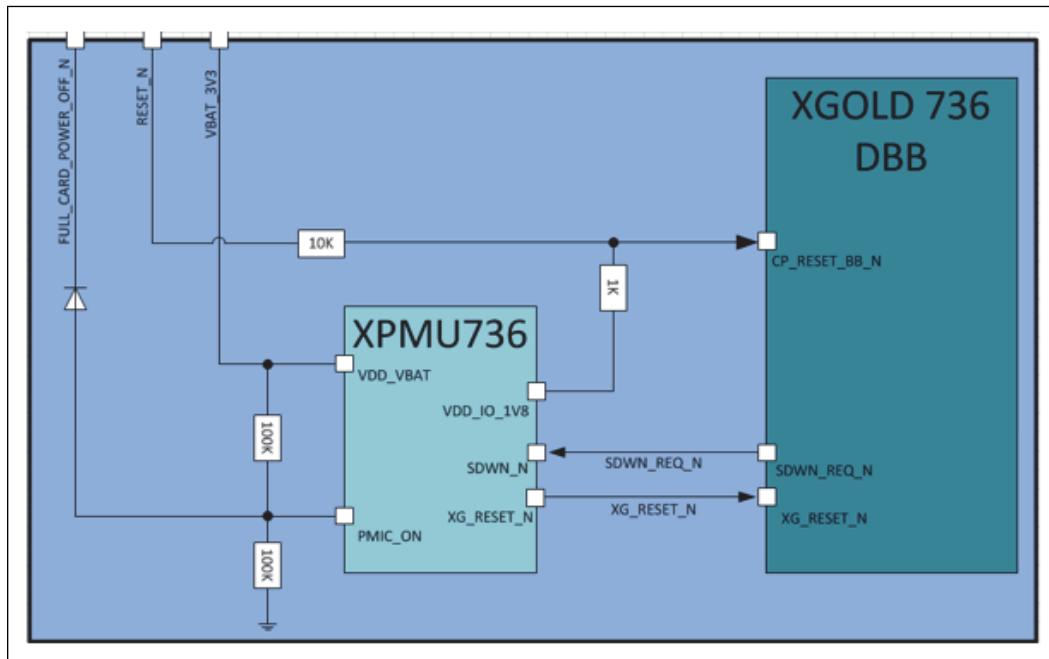
For WWAN M.2 LTE Advanced, only positions 1 and 4 are used. The other antenna connectors are not mounted on the module.

#### Modem Power ON/OFF

- **Auto-Power-On**

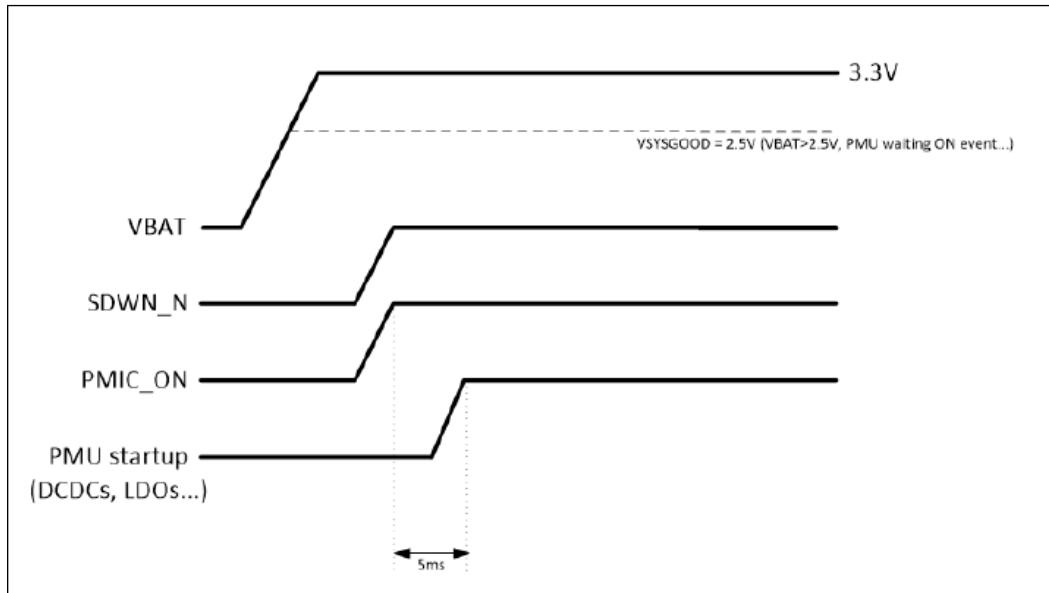
This section provides brief overview of the auto-power-on circuit design inside M2 modules.

**Figure 176. Simplified Circuit (M.2.7360)**



**VSYSGOOD** is the minimum battery voltage required by X-PMU™ 736 to startup.

**Figure 177. Power on Circuitry for XPMU7360**



- The **ON** pin and **RESET\_N** (M2 pin 67) has a pull-up within M2 module to **VBAT\_3V3** and **VDD\_IO\_1V8**.
- The **FULL\_CARD\_POWER\_OFF\_N** (M2 pin 6) is **3.3 V** tolerant. Within M2 module, we have resistors divider and diode circuits to prevent back powering.

- On **products powering by 3.3V regulator**, there is an option to use **47 kΩ** (or lower value) series resistor connected to regulated **3.3V** so that this auto-power-on circuitry will work when VBAT is applied.

#### Conclusion:

- In essence, this auto-power-on implementation is such that if the voltage conditions of **FULL\_CARD\_POWER\_OFF\_N** (M2 pin 6) and **RESET\_N** (M2 pin 67) are **HIGH**, with sufficient **VBAT** voltage ( $>2.5V$ ), this will trigger modem system start-up!

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#### NOTE

For M2 module in meeting 3GPP, the minimum VBAT is 3.135V.

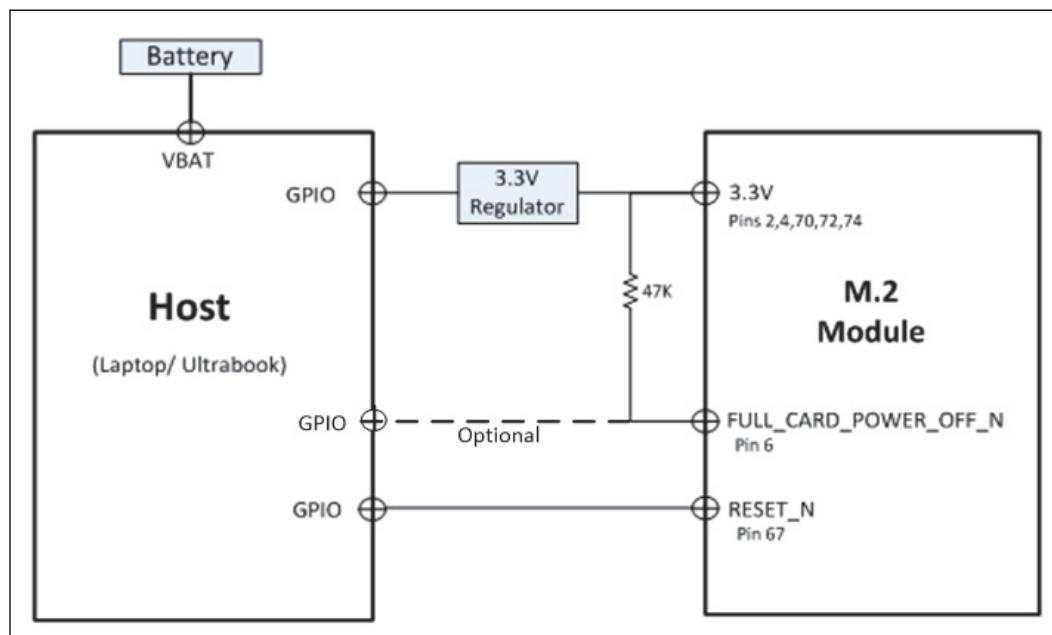
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- **Power Supply to M2 Module**

#### M2 Powering by Regulated 3.3V

If using 3.3V regulator to power M2 module then the **FULL\_CARD\_POWER\_OFF\_N** pin needs a pull-up to VBAT. The recommended pull-up resistor outside M2 module is **47 kΩ** to ensure turning the first NMOS switch ON for auto-power-on.

**Figure 178. Module Powering by Regulated 3.3 V**

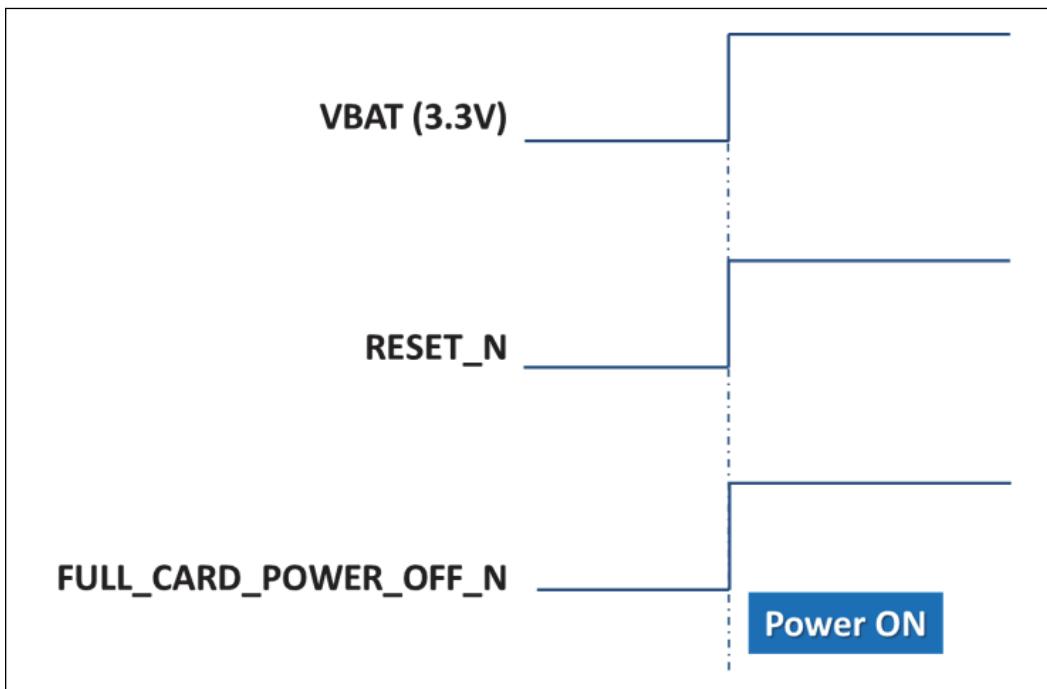


- **Power on Sequence and Timing**

#### Power on for M2 by Regulated 3.3V

As soon as the Host turns on 3.3V regulator, the M2 module will start powering on. The host should assert RESET\_N pin HIGH at the same time when turning on 3.3V regulator.

**Figure 179. Power on Timing for M2 with Regulated 3.3V**



- **Power off Sequence and Timing**

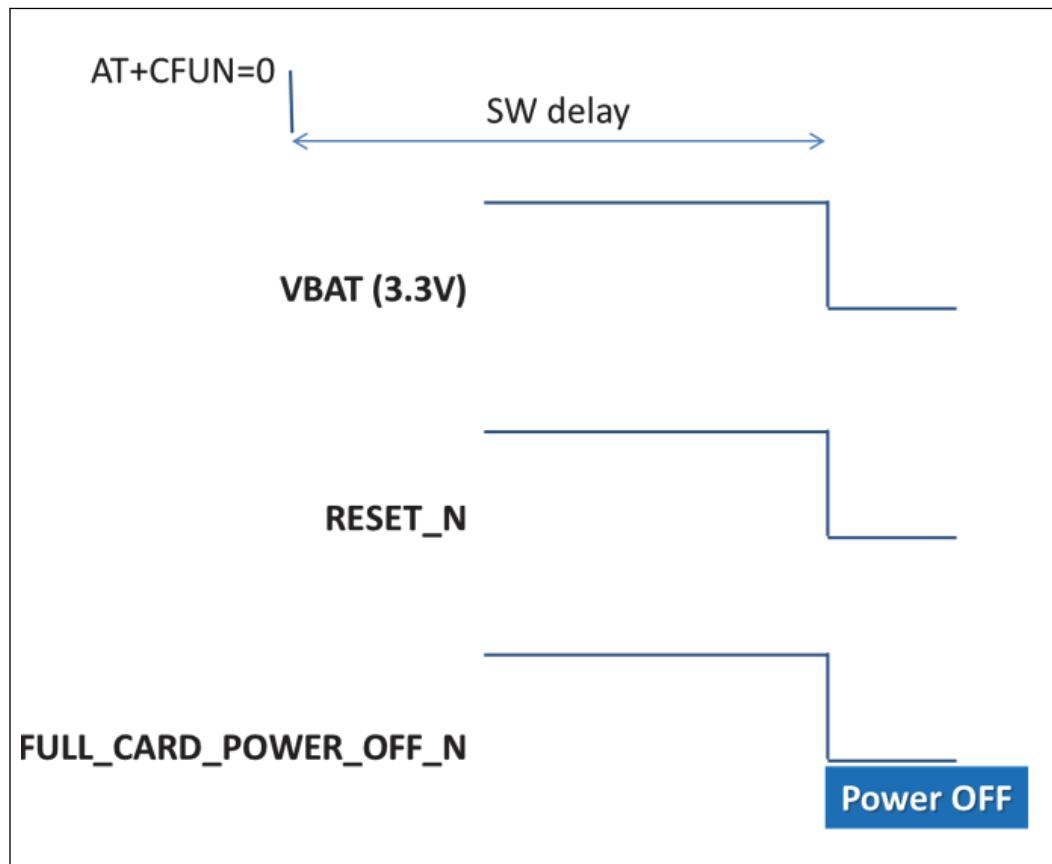
There are two supported modem power off methods, first is **Modem Controlled Shutdown** method and second is **Modem Rigorous Power-Off** method. Each method requires considering for two types of products, namely product powering by **3.3V regulator**.

#### Modem Controlled Shutdown

This method is common on Android\* products.

1. The host will issue modem shutdown AT command to M2 module, examples of modem shutdown AT commands are
2. **AT+CFUN=0, AT+CPWROFF** or customer specific customized AT command.
3. The time requires for network detach depends on network, we have seen it could range from 1 second to 5 seconds or more depending on live network condition.
4. This command triggers modem SW to do shutdown preparations (like detaching from cellular network), and once completed, it will request the actual power-off through X-PMU™ 736 register access.
5. As a consequence, the X-PMU™ 736 will disable all regulators, assert reset signals to X-GOLD™ DBB and RF Engine main reset, release the 26 MHz system clock request signal and finally go into its IDLE state (assuming VBAT > VPOR).
6. For product powering by 3.3V regulator, the host can cut off the 3.3V regulator supply to M2 module.

**Figure 180. Modem Controlled Shutdown Timing for Product with Regulated 3.3V**

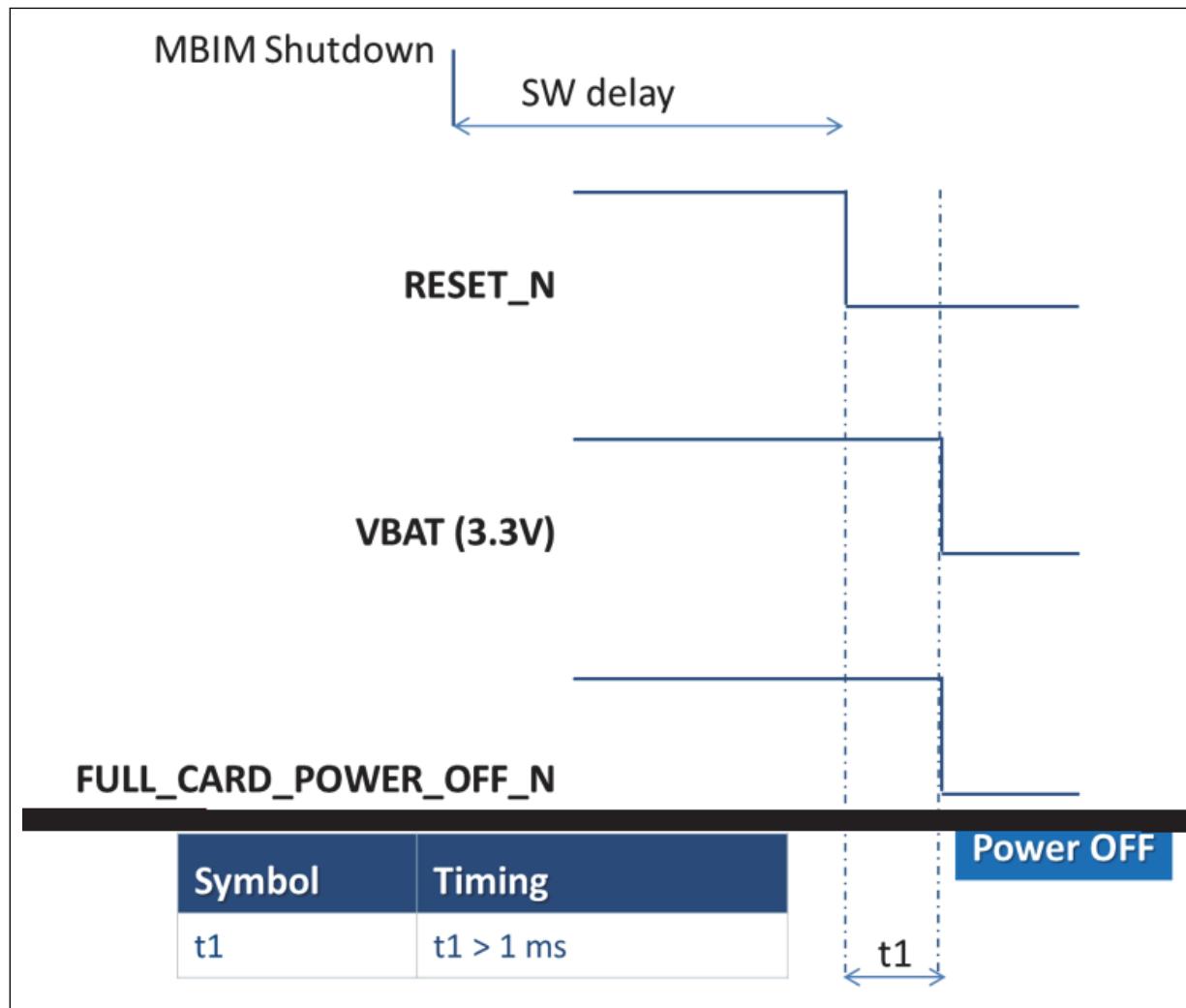


#### Modem Rigorous Power-Off

This method is for MBIM-based Windows\* OS products.

1. The host will issue MBIM shutdown command to M2 module. This command will trigger modem to perform network detached. We have seen network detach could take 1 to 5 seconds or more depend on live network condition.
2. The host will assert the **RESET\_N** pin, reason for asserting **RESET\_N** pin prior to power cut is to trigger X-GOLD™ DBB internal state machine to run shutdown sequences e.g. for SIM and external memory controller (EMIC), before switching off power supplies.
3. For product powering by 3.3V regulator, the host can cut off the 3.3V regulator supply to M2 module.

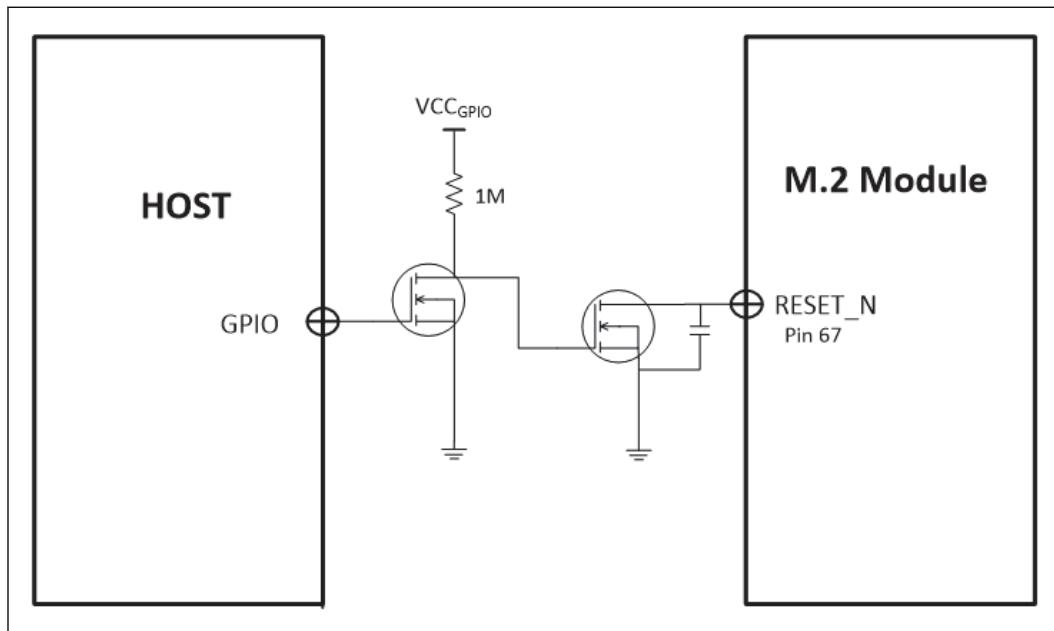
**Figure 181. Modem Rigorous Power-Off Timing for Product with Regulated 3.3V**



- **Modem Reset**

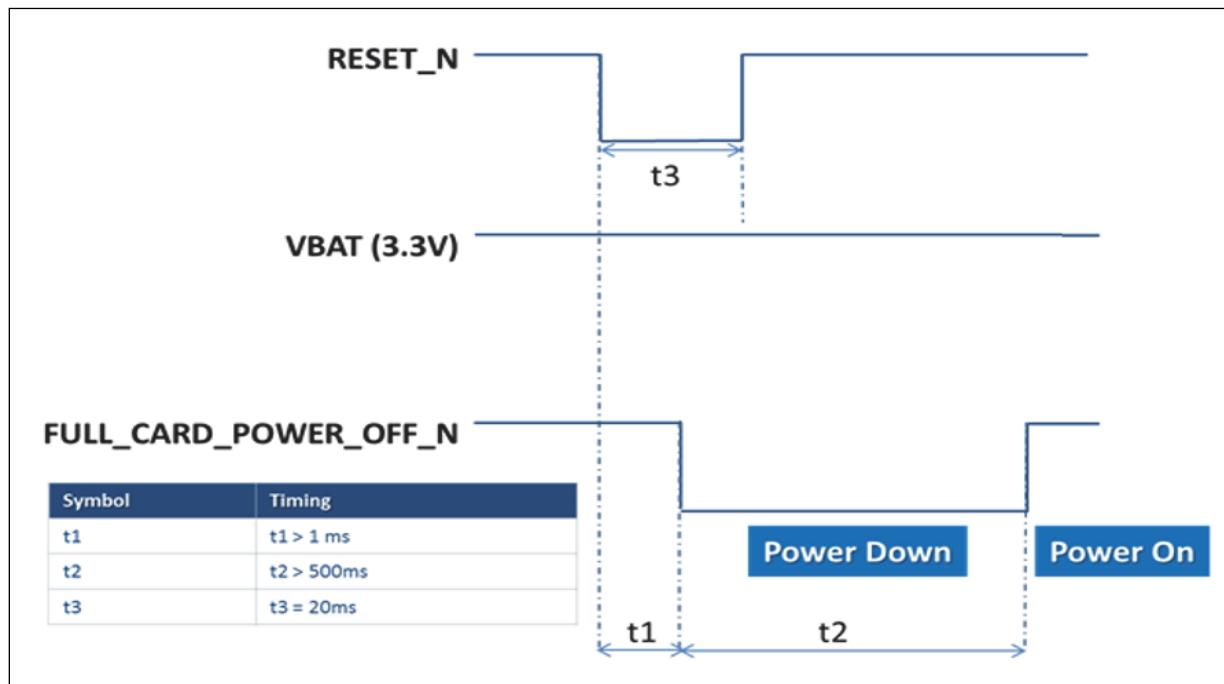
The host can reset modem during critical failure, when all other methods of regaining control or communication with the modem sub-system have failed. The Host GPIO to drive RESET\_N pin needs to be High Impedance when M2 module is power OFF to prevent back driving issue. If this is not the case, then there is a recommended circuit provided here:

**Figure 182. Sample Hardware Circuit for Host GPIO that is not High-impedance when M2 Module is OFF**



1. **RESET\_N**
  - a. Pulling **RESET\_N** low for more than 20ms will reset modem.
  - b. **RESET\_N** pin is internally pull-up to VDD\_IO\_1V8; this IO voltage will turn on when the host provides 3.3V and **FULL\_CARD\_POWER\_OFF\_N** is HIGH.
  - c. **RESET\_N** pin will trigger modem baseband reset cycle in which some modules (like EMIC and SIM) are first safely deactivated before they are forced into the reset state. The reset state is kept as long as **RESET\_N** is asserted.
2. **FULL\_CARD\_POWER\_OFF\_N**
  - In the event if assertion of **RESET\_N** pin unable to recover modem from crashed, then the Host can assert **FULL\_CARD\_POWER\_OFF\_N** low for more than 500ms, follow by pulling it HIGH to reset modem. This should be final resort because this is a force shutdown followed by recovery procedure.
  - Pulling **FULL\_CARD\_POWER\_OFF\_N** low will assert PMIC\_ON pin of modem and this will immediately start a power-off sequence in X-PMU™ 736 and the X-PMU™ 736 will disable all regulators, assert reset signals to X-GOLD™ DBB and RF Engine main reset, release the 26 MHz system clock request signal and finally go into its IDLE state (assuming VBAT > VPOR)
  - Pulling **FULL\_CARD\_POWER\_OFF\_N** back to HIGH is powering back M2 module and the timing will follow the power up sequence documented in previous section.
  - Modem reset timing by using **RESET\_N** and **FULL\_CARD\_POWER\_OFF\_N** pin

**Figure 183. Modem Reset Timing by RESET\_N and FULL\_CARD\_POWER\_OFF\_N Pin**



- **Host Reboot Scenario**

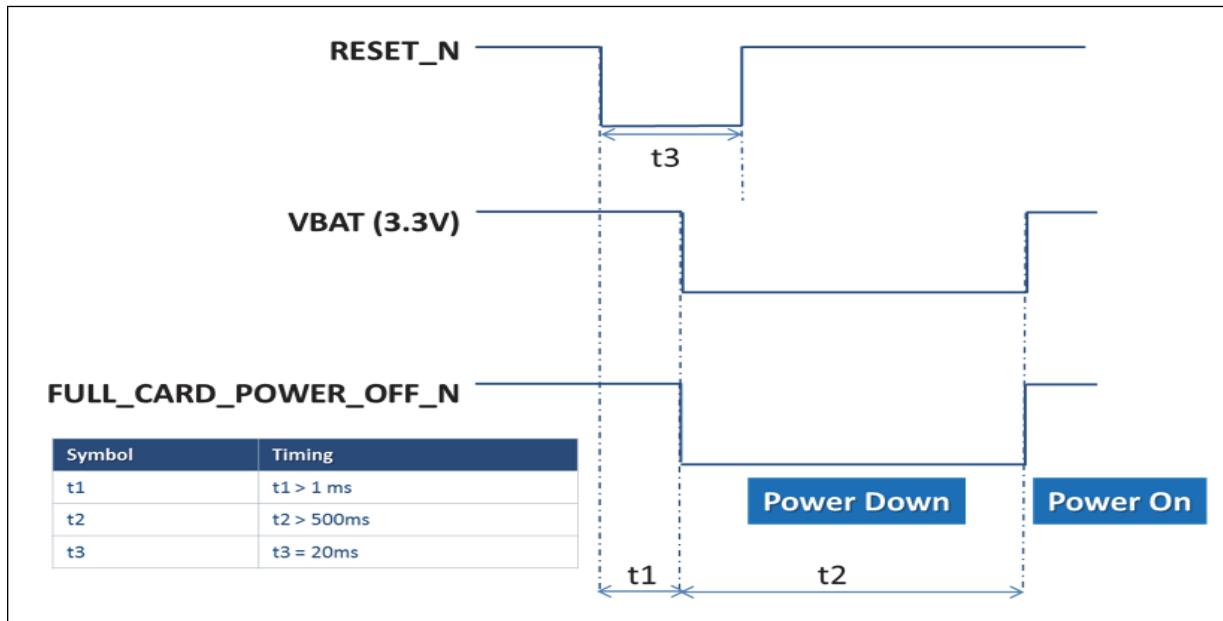
There are two methods to handle M2 module during host reboot:

- The host will assert **RESET\_N** pin to **reset** M2 module. The timing for reset method is the same as described on the above figure.
- The Host GPIO to drive **RESET\_N** pin needs to be High Impedance when M2 module is power OFF to prevent back driving issue.

The host will **power cycle** M2 module by first using **Modem Rigorous Power-Off** method to shutdown modem, and then use the **Power On** method to start up modem again.

There is no change on the sequence and timing as provided in previous sections.

#### **Host Reboot Timing with Power Cycle for Product with Regulated 3.3V**

**Figure 184. Host Reboot Timing for Product with Regulated 3.3V**

## 8.4 Antenna Design Guidelines

A broad range of wireless modules are available suited to different regulatory, performance, and user requirements. This chapter shall discuss the considerations for antenna integration in this processor designs including, but not limited to, antenna performance, placement options, and RF system-level integration.

The processor may support radios for:

- Wi-Fi (WLAN)
- Bluetooth (BT)
- GNSS
- WWAN

### 8.4.1 Antenna Integration

The successful antenna integration on the system is determined through three prime objectives:

1. Ensure good individual antenna efficiency in the frequency bands supported by the respective modem, for all antennas and all modes of operation.
2. Ensure adequate isolation between antennas to:
  - a. Minimize the spatial correlation and mutual coupling between antennas for radios supporting MIMO or diversity, and maximize the benefit that can be derived from the additional transceiver chain.
  - b. Enable the simultaneous operation use-case scenario of multiple radios (co-existence) to be supported without any potential performance degradation. Co-existence of multiple wireless modules and their antennas can become a major problem if not considered in the initial stages of design.

3. Minimize the platform noise coupling into each antenna (in-band noise) which may potentially impact the radio's receiver performance.

## 8.4.2 Antenna Performance

The individual antenna performance can be characterized by the frequency coverage, efficiency, and peak gain. The isolation between antennas is defined by the  $S_{21}$  as measured from the antenna ports on a network analyzer. For radios supporting MIMO or diversity, the MIMO antennas will need to meet the recommended gain imbalance and envelope correlation coefficient limits. These antenna metrics are commonly referred to as passive antenna metrics since the antennas are not connected to their respective modems during the measurement. For WWAN and A-GNSS, most major carriers have defined radiated performance requirements for wireless devices which include the Total Radiated Power (TRP) and Total Isotropic Sensitivity (TIS). Refer to the target carrier(s) radiated performance requirements for details.

The following tables summarize the passive antenna performance recommendations for each wireless system, the isolation recommendations, and the recommendations for different modes of operation.

The envelope correlation coefficient can be expressed in the following methods depending on the available figures of merit:

**Table 182. Antenna Performance Recommendations**

Antenna	Frequency (GHz)	Type	Max Size of Antenna Element (mm)	Efficiency <sup>1</sup> (dB)	Peak Gain <sup>3</sup> (dBi)	VSWR <sup>4</sup>	MIMO Metrics
WLAN	2.40-2.49 5.15-5.85 5.925-7.125	PIFA/Slot <sup>7</sup>	35x8x1	-3.9 (2.4GHz) -4.4 (5GHz) -4.4 (6GHz)	<3 (2.4GHz) <3.5 (5GHz) <3.5 (6GHz)	2:1	Correlation Coefficient < 0.3, Gain imbalance < 1 dB
Bluetooth*	2.40-2.49	PIFA/Chip <sup>7</sup>	35x8x1	-3.9	<3	2:1	N/A
GNSS <sup>2</sup>	1.56-1.61	PIFA	15x5x2	-3.5	<2	2:1	N/A
WWAN M.2 HSPA (2G, 3G)	0.82-0.96 1.71-2.17	PIFA	75x13x2	-4 (f<1GHz) -3 (f>1GHz)	<2	3:1 <1GHz 2:1 >1GHz	Correlation Coefficient: -> ecc < 0.5 (f < 1GHz) -> ecc < 0.4 (f > 1GHz) Gain imbalance < 1 dB
WWAN M.2 LTE (2G, 3G, LTE)	0.70-0.96 1.42-1.51 1.71-2.17 2.30-2.40 2.50-2.70 GNSS <sup>2</sup>	PIFA	75x13x2	-3.5 (f<1.6GHz) -3 (f>1.6GHz)	<2	3:1 <1GHz 2:1 >1GHz	Correlation Coefficient: -> ecc < 0.5 (f < 1.6GHz) -> ecc < 0.4 (f > 1.6GHz) Gain imbalance < 1 dB
WWAN M.2 LTE (2G, 3G, LTE, LTE-LAA)	0.70-0.96 1.42-1.51 1.71-2.17 2.30-2.40 2.50-2.70 3.50-3.70 5.0-6.0 GNSS <sup>2</sup>	PIFA	75x13x2	-3.5 (f<1.6GHz) -3 (f>1.6GHz)	<2	3:1 <1GHz 2:1 >1GHz	Correlation Coefficient: -> ecc < 0.5 (f < 1.6GHz) -> ecc < 0.4 (f > 1.6GHz) Gain imbalance < 1 dB
LTE Sub 6GHz Main & Aux	0.60-0.96 1.42-1.51	PIFA	75x13x2	-3.5 (f<1.6GHz) -3 (f>1.6GHz)	<2	3:1 <1GHz 2:1 >1GHz	Correlation Coefficient:  <i>continued...</i>

Antenna	Frequency (GHz)	Type	Max Size of Antenna Element (mm)	Efficiency <sup>1</sup> (dB)	Peak Gain <sup>3</sup> (dBi)	VSWR <sup>4</sup>	MIMO Metrics
	1.71-2.17 2.30-2.40 2.50-2.70 3.5-3.70 5.0-6.0						-> ecc < 0.5 (f < 1.6GHz) -> ecc < 0.4 (f > 1.6GHz) Gain imbalance < 1 dB
LTE MIMO 3 & 4	1.71-2.17 2.30-2.40 2.50-2.70 3.50-3.70 5.0-6.0	PIFA /Slot 7	45x10x2	-6 (MIMO RX)	<2		Correlation Coefficient: -> ecc < 0.4 Gain imbalance < 1 dB

*Notes:*

- Efficiency targets include the cable loss. Actual cable loss will vary based upon the chassis integration.
- GNSS (i.e. GPS, GLONASS) antenna is usually expected to be shared with WWAN Aux (LTE only) or 5G NR/WWAN MIMO antenna. It is also possible that GNSS antenna for non WWAN SKUs is either discrete or shared with WLAN antenna. In either case, the efficiency target listed above is recommended
- Peak gain targets include the cable loss. Refer to the module's regulatory modular approval for details.
- VSWR = 2:1 represent S<sub>11</sub> (reflection coefficient) = -10 dB and VSWR = 3:1 represents S<sub>11</sub> = -6 dB
- For TRP evaluation refer to module EPS document for actual conducted Tx Power depending on Geo. For TIS evaluation refer to conducted sensitivity
- During the WiFi modular certification, reference antenna uses less than 5 dBi Peak gain requirement at 5GHz and above. Table shows the recommendation mainly targeting to best UX from 3.5 dBi.
- For Regulatory purpose Intel handles modular certification with PIFA antenna only

**Table 183. Isolation Recommendations**

Antenna Ports	Wi-Fi	Bluetooth*	GNSS	LTE Main and Aux	LTE MIMO 3 and 4
<b>Wi-Fi</b>	25 dB nominal	25 dB nominal <sup>1</sup> (15 dB min)	25 dB	25 dB <sup>2</sup> (15 dB LTE Band7, 40, 65, 66 <sup>3</sup> )	25 dB nominal <sup>2</sup> (15 dB min)
<b>Bluetooth*</b>	25 dB nominal <sup>1</sup> (15 dB min)	N/A	25 dB	25 dB (20 dB LTE Band7, 40, 65, 66 <sup>3</sup> )	25 dB nominal <sup>1</sup> (15 dB min)
<b>GNSS</b>	25 dB	25 dB	N/A	25 dB	(Shared)
<b>LTE Main &amp; Aux</b>	25 dB (15 dB LTE Band7, 40, 65, 66 <sup>3</sup> )	25 dB (20 dB LTE Band7, 40, 65, 66 <sup>3</sup> )	25 dB	25 dB	25 dB
<b>LTE MIMO 3 &amp; 4</b>	25 dB nominal <sup>1</sup> (15 dB min)	25 dB nominal <sup>1</sup> (15 dB min)	(Shared)	25 dB	25 dB

*Notes:*

- BT-WiFi isolation translates to Wi-Fi main to Wi-Fi Aux isolation for the case where BT antenna is shared with Wi-Fi. For best performance, recommended isolation > 35 dB. Nominal performance with limited degradation can be seen with isolation > 25dB. Co-existence solution allows functionality down to 15 dB isolation with reduced performance.
- Without LTE band 7 and without a co-existence mechanism between Wi-Fi and WWAN modules, 30 dB isolation is the best, but 25 dB is acceptable as indicated shown above
- Without a coexistence scheme between WLAN and WWAN, additional filtering at both WWAN and WLAN modules is required to operate at 15 dB isolation. Careful consideration of the total system solution is required for this case

**Table 184. Recommendations for Different Modes of Operation**

Description of Lid Mode	Clamshell (open Lid)	Tablet	Closed Lid
Antenna performance recommendations	As in Antenna Performance Recommendations	As in Antenna Performance Recommendations	3 dB lower than values in Antenna Performance Recommendations

- With the far-field complex antenna radiation patterns, which can be measured in antenna test chambers, the envelope correlation coefficient can be evaluated with the following formula:

$$\rho_e = \frac{\left| \int_0^{2\pi} \int_0^{\pi} (XPR \cdot F_{\theta 1}(\theta, \phi) F_{\theta 2}^*(\theta, \phi) P_\theta(\theta, \phi) + F_{\phi 1}(\theta, \phi) F_{\phi 2}^*(\theta, \phi) P_\phi(\theta, \phi)) \sin \theta d\theta d\phi \right|^2}{\left| \int_0^{2\pi} \int_0^{\pi} (XPR \cdot |F_{\theta 1}(\theta, \phi)|^2 P_\theta(\theta, \phi) + |F_{\phi 1}(\theta, \phi)|^2 P_\phi(\theta, \phi)) \sin \theta d\theta d\phi \right| \cdot \left| \int_0^{2\pi} \int_0^{\pi} (XPR \cdot |F_{\theta 2}(\theta, \phi)|^2 P_\theta(\theta, \phi) + |F_{\phi 2}(\theta, \phi)|^2 P_\phi(\theta, \phi)) \sin \theta d\theta d\phi \right|}$$

where  $\rho_e$  is the envelope correlation coefficient,  $F_1$  and  $F_2$  are the complex vector field strengths of antenna 1 and 2 respectively,  $XPR$  is the cross-polarization ratio, and  $P$  is the incident field distribution function.

- In the case where the complex antenna radiation pattern cannot be obtained, an alternative method, which requires the S-parameters and the individual radiation efficiencies, can be utilized to determine the correlation coefficient in the following formula:

$$\rho = \frac{-S_{11}S_{12}^* - S_{21}S_{22}^*}{\sqrt{(1 - |S_{11}|^2 - |S_{21}|^2)(1 - |S_{22}|^2 - |S_{12}|^2)n_1 n_2}}$$

where  $\rho$  is the envelope correlation coefficient,  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ ,  $S_{22}$  are the S-parameters of the two port antenna system measured on a network analyzer,  $S_{12}^*$  is the complex conjugate of  $S_{12}$ , and  $n_1$  and  $n_2$  are the antenna radiation efficiencies measured with the unused antenna port terminated with a 50 Ohm load.

- In the case where only the S-parameters are available, the envelope correlation coefficient can be estimated with the following formula:

$$\rho_e = \frac{|S_{11}^*S_{12} + S_{21}^*S_{22}|^2}{(1 - |S_{11}|^2 - |S_{21}|^2)(1 - |S_{22}|^2 - |S_{12}|^2)}$$

The envelope correlation coefficient calculation methods shown above are described in the following papers:

- Ying et al.; "Characterization of multi-channel antenna performance for mobile terminal by using near field and far field parameters," COST 273 TD(04)(095), Goteborg, Sweden, 2004.*
- Hallbjorner, P.; "The significance of radiation efficiencies when using S-parameters to calculate the received signal correlation from two antennas," Antennas and Wireless Propagation Letters, IEEE, vol.4, no., pp. 97- 99, 2005*

### 8.4.3 Antenna Placement

The following must be considered when deciding the placement of antennas:

- Modes of Operation:** For devices which enable different modes of operation (i.e. Clamshell, Tablet, and Closed Lid), careful consideration of the environment around the antenna in each configuration while deciding the antenna placement is necessary to deliver the desired user experience in all modes of operation.

Furthermore, it should be verified that the antennas are placed in such a manner that the user does not accidentally cover all antennas while in an intended mode of operation. This would result in loss of connectivity or deteriorating of the signal for the affected radios.

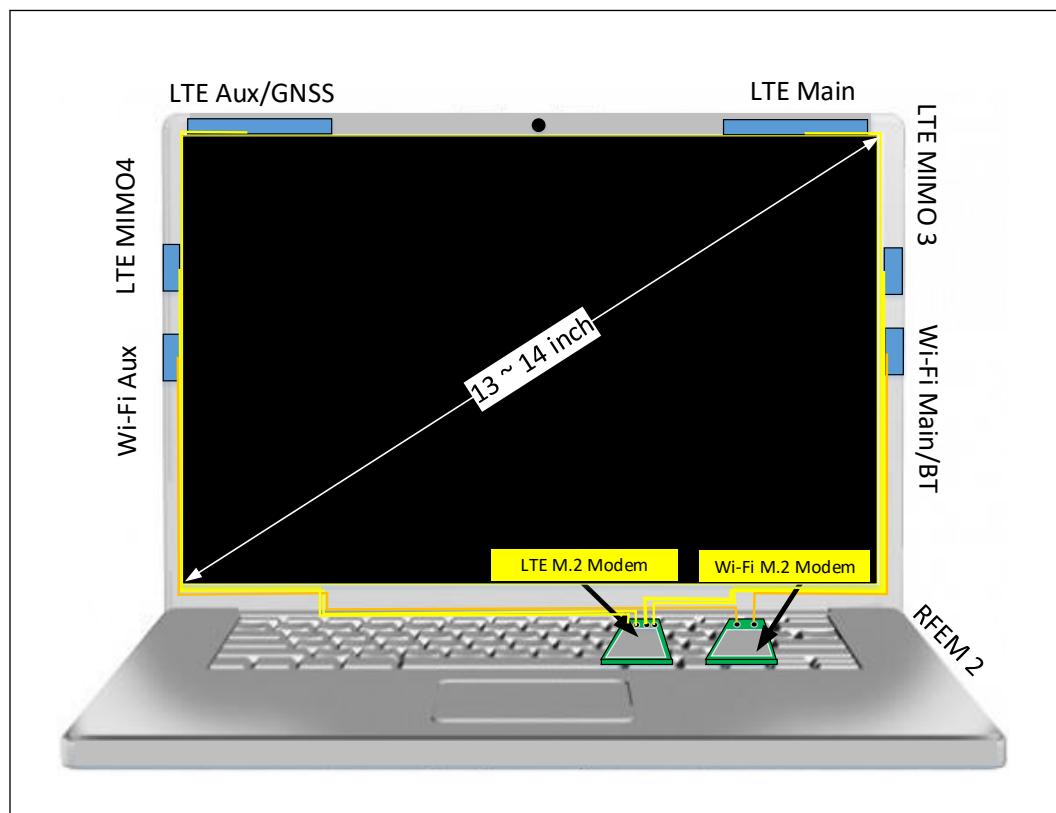
- **Keep-Out-Zone (KOZ):** A metal-free KOZ is typically required to integrate the antenna in traditional designs. The physical size of the antenna will depend on the target frequencies, bandwidth, and performance requirements of the antenna. Antennas with larger geometric footprints tend to provide better performance. The non-metallic materials (i.e. plastics) also need to be assessed since different materials properties may have different effects to the antenna characteristics.
- **Lossy Structures:** Separation of the antenna radiation elements from lossy structures, such as the LCD enclosure, will provide better bandwidth. The separation required for WWAN is higher than that required for Wi-Fi. In general, lower operational frequencies require larger separation compared to higher operational frequencies. Also, larger bandwidth considerations require larger separation from nearby metallic structures.
- **Grounding:** Unbalanced antennas require a ground reference, which is typically the chassis or the back of the display. The size of the ground reference needs to be considered as part of the antenna design.
- **Cable Routing:** Each antenna will require a coaxial cable to connect to the radio module's RF port. Cable routing that avoids regions with noise and minimizes cable lengths is recommended to minimize the platform noise impact and cable loss. In the case where the module is in the base and the antenna is in the display, the coaxial cable will need to be fed through the hinges. The size of the mechanical hinge places a restriction on the number of cables that can be fed through and the diameter of the cables. Typical RF coax cables can range in outer diameter (OD) from 0.81 mm to 1.37 mm; however, the RF connector receptacle defined by the M.2 module specification will only accept mated plugs with either 0.81 mm OD cables or 1.13 mm OD cables. Refer the respective radio module's product description for the RF connector type.
- **Cable Loss:** Coaxial cables will introduce an insertion loss depending on the diameter, length, and frequency of interest. Thicker coaxial cables tends to be less lossy while being more expensive compared to thinner cables. Lower loss cables are also available from vendors which will reduce the total cable loss especially for long cables. Double shielded cables are useful in ensuring that radio module sensitivity degradation is limited due to the cable picking up platform noise when routed through the platform.
- **RF Exposure (SAR):** Regulatory bodies, such as FCC and CE, define detailed requirements for the allowable RF exposure for devices which generate RF electromagnetic fields. Specific Absorption Rate (SAR) is a measure of the rate in which energy is absorbed in body tissue due to EM energy from an antenna. and is a prime consideration for placement of antennas, especially for higher power radios such as WWAN.
- **Isolation between antenna ports:** To improve the isolation between antennas, the following methods can be employed which include, but is not limited to:
  1. Spatial diversity - larger spatial separation between antennas is one way of increasing the isolation between ports of radio modules that operate in bands that are close to one another.
  2. Polarization diversity - in some instances where the antennas have polarization discrimination, the relative orientation of the antennas can be used to improve isolation and enhance performance.

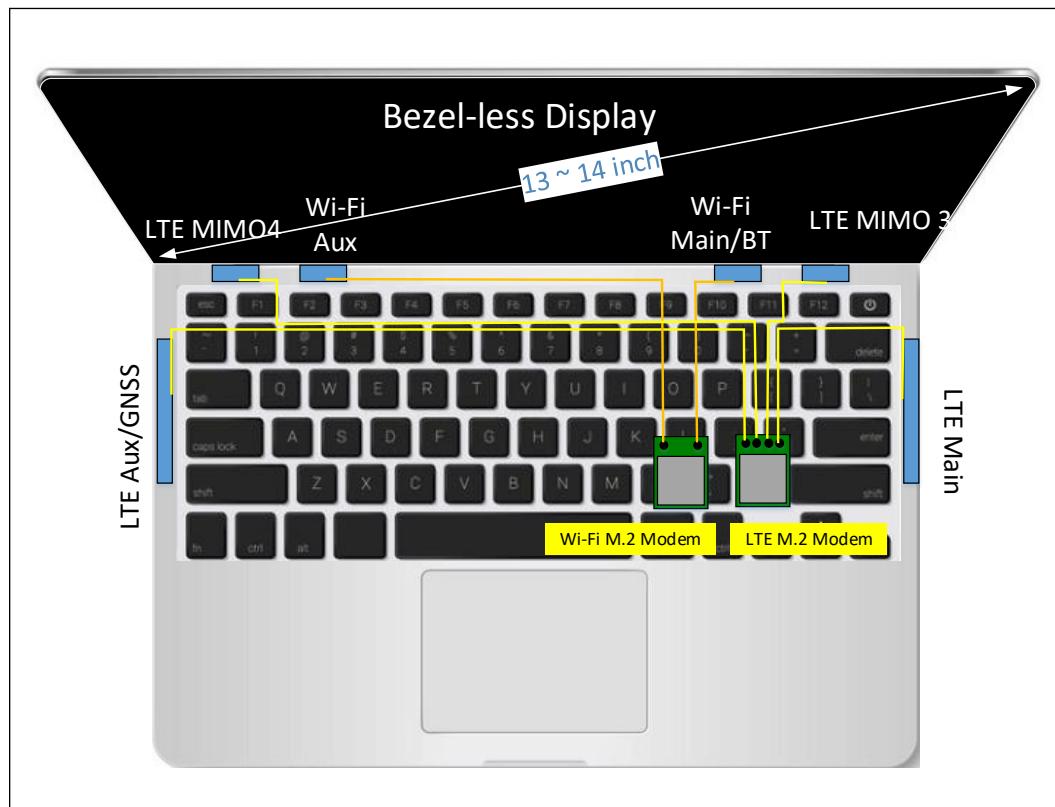
3. Pattern diversity - utilizing antennas with different radiation patterns and orienting the peak gain direction of the antenna in different directions may also improve isolation.
- **Platform Noise:** Various components in the system, such as display/touch circuits, memory, PLLs, cameras, clocks, USB/HDMI ports, and other high speed IO, may generate noise which can couple to the antennas and/or coax cables and thus degrade the wireless radio's receiver performance. Careful consideration needs to be employed with respect to antenna placement and cable routing to avoid these noise sources and minimize the platform noise impact to the receivers. With detachable tablets and convertible notebooks, the proximity of the antenna to the base components needs to be especially considered during the initial floor planning. In addition to antenna placement , the particular component which was highly suspected to be radiation source should require good RF shielding for significant isolation improvement.
    - Internal studies have found that 3D cameras, which utilize the USB3 interface to communicate with the motherboard, is a source of broadband RF noise which may impact the antennas in the vicinity. The camera noise may impact the radio's receiver performance through the antenna in two ways:
      1. Conducted noise which flows from the camera through the shared ground plane (chassis) and in to the antenna through the antenna ground connection. To reduce the noise coupled in to antenna, the ground plane should be manipulated to re-direct the current flow from the camera away from the antenna.
      2. Radiated noise from the 3D camera interface (especially the USB3 connector), may couple to the antenna and hence desensitize the radio receiver. In general, the antennas should be separated from the 3D camera and USB3 bus to avoid any degradation to the radio's receiver performance. Studies have shown that the antenna should be at least 15 mm away from the USB3 connector for minimal impact to WWAN and Wi-Fi radios. Shielding of the camera and USB3 connector is also recommended.

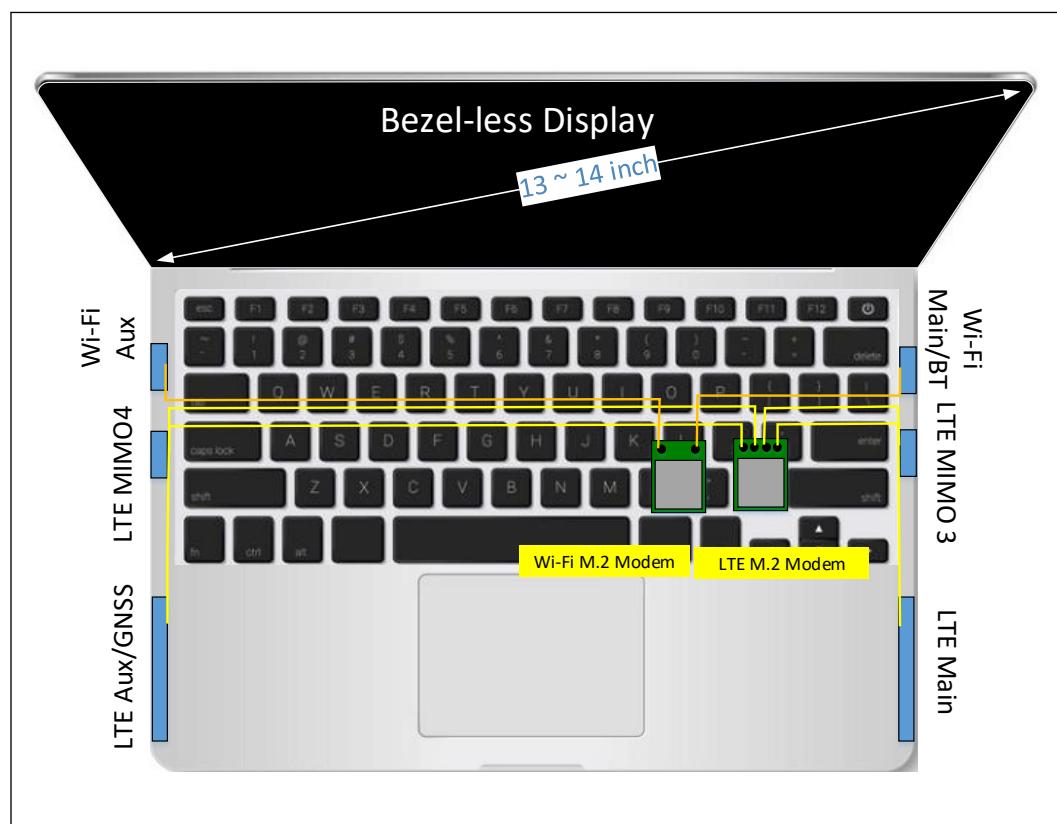
### Antenna Placement Options for Multi-Mode Devices

Four potential antenna placement options are shown in the figures below for clamshells or multi-mode devices such as convertibles and detachable Ultrabook™. The target form factor for the placement options is around 13 to 14 inch notebook, but it is not limited to this size. Recent platform ID trend introduces Bezel-less display platforms and there is no space available in LCD bezel area where could be the prime location for antennas. The module selection includes support for 2x2 MIMO Wi-Fi/BT, and 4X4 WWAN. GNSS is assumed to be combined with WWAN Aux antenna.

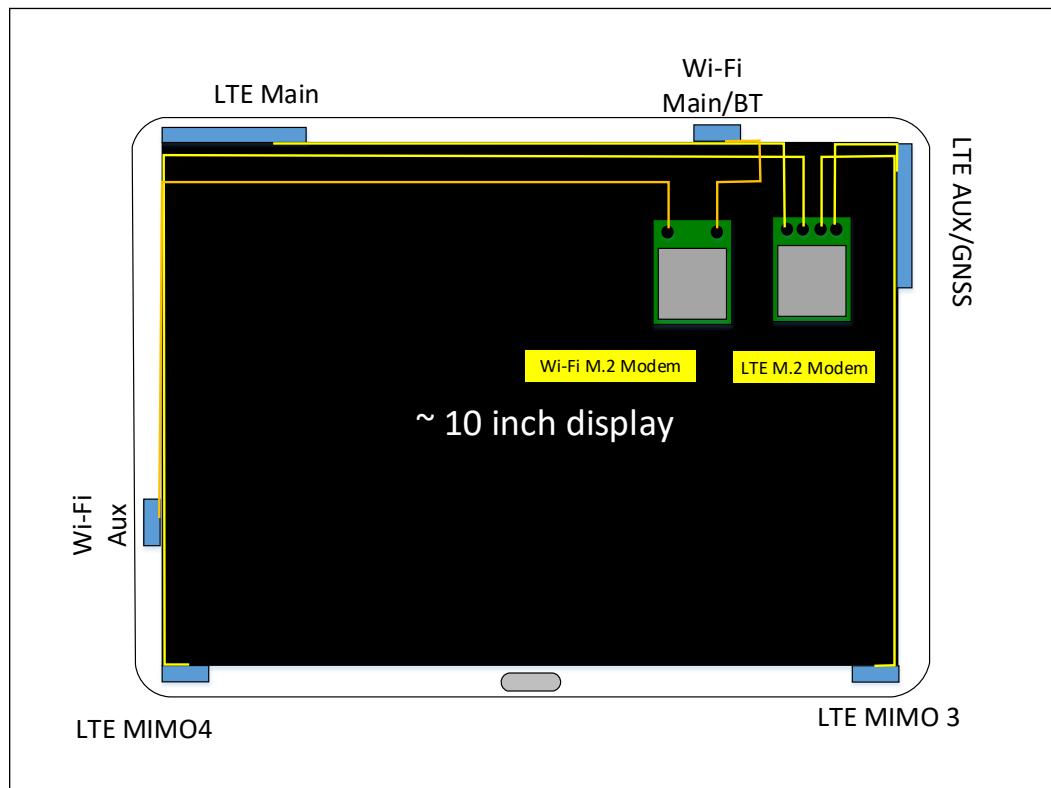
The module selection includes support for 2x2 MIMO Wi-Fi/BT, and 1x2 WWAN. GNSS is assumed to be combined with WWAN Aux antenna (AGPS/GPS).

**Figure 185. Antenna Placement Option 1: Clamshell Mode Bezel Integration**

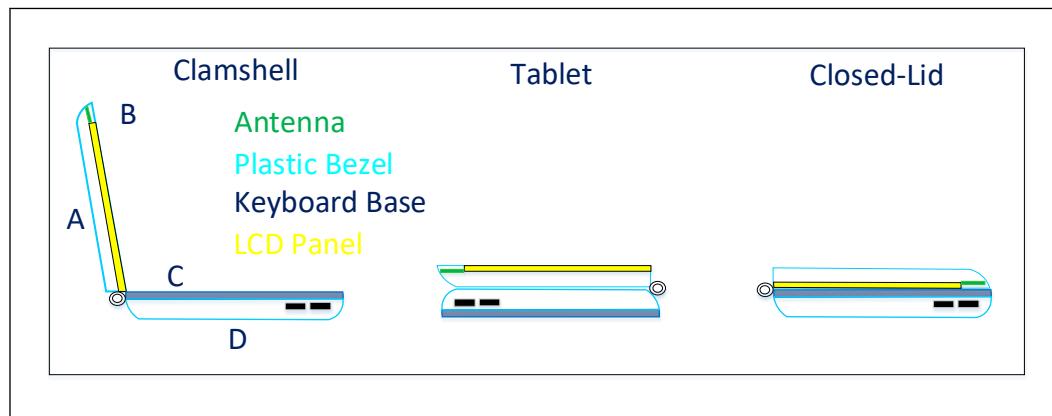
**Figure 186. Antenna Placement Option 2: Clamshell/2in1 Base Integration 1**

**Figure 187. Antenna Placement Option 3: Clamshell/2in1 Base Integration 2**

**Figure 188. Antenna Placement Option 4: Tablet/Detachable Integration**



Previously, most Clamshell-only notebooks have satisfied the SAR exclusion thresholds defined by FCC in which one of the requirements being the antennas are mounted around the display with the minimum antenna-to-user separation distance. In those cases, the SAR testing and transmit power reduction could be potentially avoided. With multi-mode devices, the various modes of operations will require special attention to the impact to SAR due to the antenna placement and may require transmit power reduction to meet regulatory requirements. In general, the antennas in the display should be mounted closer to the B-surface to increase the separation distance from the body and reduce the SAR. The figure below provides recommendations for antenna placement in a non-metallic convertible chassis, with considerations for SAR.

**Figure 189. Placement Recommendation with Regulatory SAR Considerations**

- In the case of a detachable tablet, or the Tent Mode test configuration for convertible notebooks defined by Intel Regulatory, the antenna on the A-surface is the worst-case location for body-SAR and will result in significant transmit power reduction for WWAN and possibly even Wi-Fi.

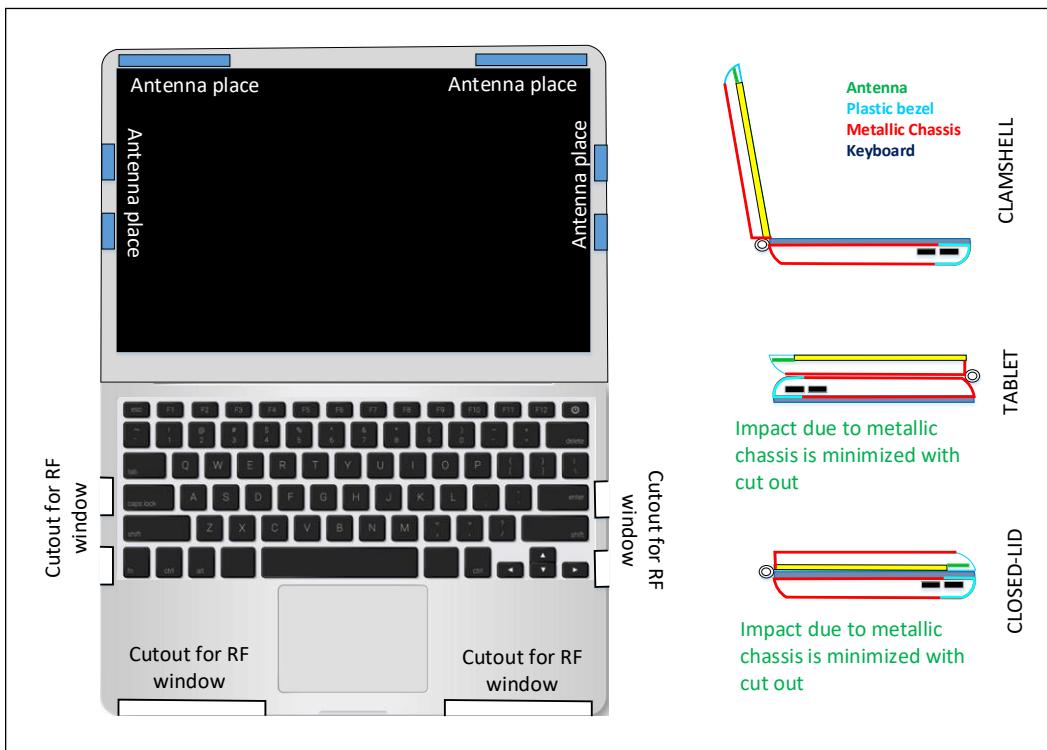
### Antenna Placement in Metallic Chassis

Many platforms with the U-processor design utilize metal materials for the surface covers, commonly referred to as metallic chassis. The antenna must be placed such that there is sufficient clearance from metal to enable good wireless performance. When there are metal surfaces surrounding the antenna, it is recommended to have plastic sections or insert molded plastic in the metal covers to provide an RF transparent window which will not degrade the antenna performance and thus enable good wireless connectivity in all modes of operation. Other potential options include integrating the antenna on the base (keyboard side) of the platform or utilizing the hinge area. Care should be taken to ensure potential EMI from adjacent I/O connectors do not interfere with the antenna reception.

The following placement options may be considered:

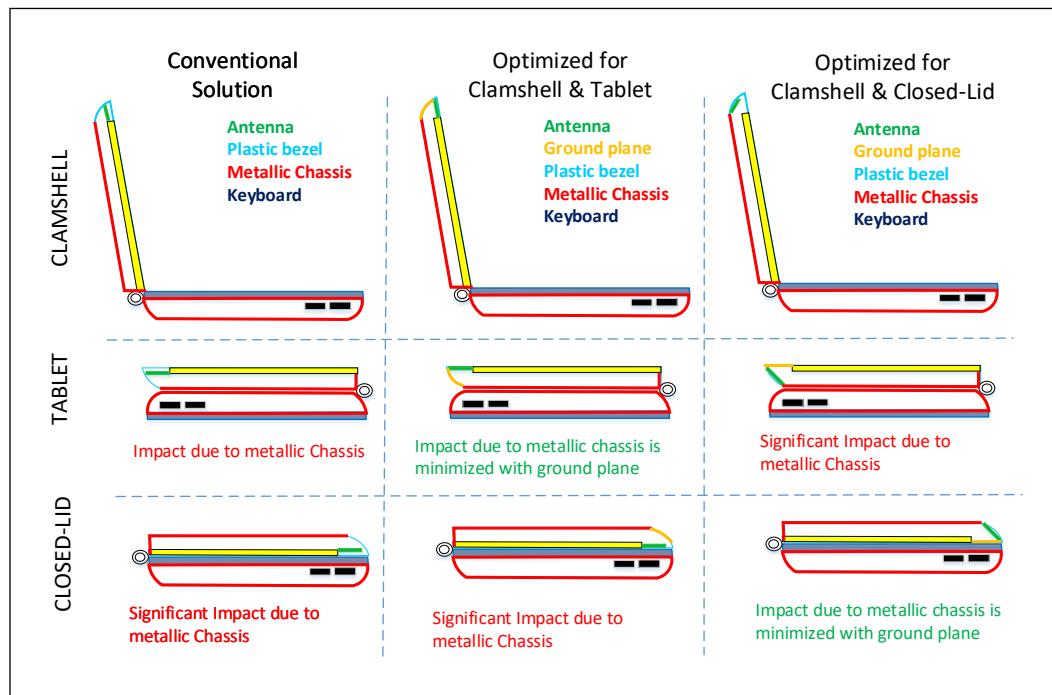
1. **Metal Chassis with cutouts in display and base:** In the case of a metallic chassis, cutouts may be employed to provide required clearance for the antenna on the A and B-surfaces. When in Tablet or Closed-Lid modes, the antenna must not reside closer than 5 mm to metal (or EMI coating) on the D-surface or C-surface, respectively. A suitable plastic cutout, with a recessed EMI shield maybe required to achieve both ESD and EMI protection and good Tablet and Closed-Lid performance. The figure below depicts this solution.

**Figure 190. Placement Options for Metallic Chassis with Cutouts in Display and Base**



2. **Metallic chassis with cutout in the display:** A dielectric loaded antenna maybe placed for Wi-Fi operation on the B-surface, with a cutout on the A-surface. Such a dielectric loaded antenna can operate with a metallic B-surface, which also shields the antenna from the changes introduced by closing the lid. The figure below depicts this solution.

**Figure 191. Placement Options for Metallic Chassis with Cutouts in Display**



- Due to the Tent Mode test configuration for convertible notebooks defined by Intel Regulatory, or in the case of a detachable tablet, the antenna on the A-cover is the worst-case for the body SAR requirement in touch condition and will result in significant transmit power reduction for WWAN and possibly even Wi-Fi. (Same applies for detachable tablet notebooks)
- Base mounted Wi-Fi antennas:** Antennas can be placed in the hinge area on the base of a metallic chassis notebook, with a plastic cutout near the hinge. The hinge must be such that when the lid closes, the area in the base where the antennas are housed is not shielded completely by the lid. Special consideration must be given to maximizing the separation between the antenna and the human body below the D-surface to pass SAR requirements with low-risk. Platform noise pickup from base mounted antennas needs to be measured before committing to a particular location as there is a higher risk of impact from platform noise due to the closer proximity of the antennas to the motherboard.
  - Slot antennas cut into the chassis:** Slots can be cut into the A-surface of the antenna, near the apex of the lid and the cutout can be covered with plastic inserts. Such an antenna would be integrated into the chassis and special care must be given to the feeding mechanism, especially when materials not amenable to soldering such as aluminum are used. Multiple antenna SKUs and/or revisions will imply multiple chassis SKUs and/or revisions, so this option will need to be considered very early in the design cycle.

#### 8.4.4

#### RF System-Level Integration Recommendations

##### Wi-Fi

Platforms typically support 2x2 (and some 3x3) MIMO configurations for Wi-Fi. In addition to meeting the efficiency requirements set forth in [Antenna Performance](#) on page 318, some additional system level recommendations are listed in table below.

**Table 185. Additional Recommendations for Wi-Fi MIMO Operation**

SN	Additional Recommendations for Wi-Fi MIMO Operation	
1	Difference in Noise coupling into Main and Aux antennas	< 1 dB
2	Absolute value of noise coupling into Main and Aux antennas	< 3dB de-sense from noise floor

In addition the antenna specifications, the following considerations are brought to attention:

- Modern Standby Support (previously Connected Standby or InstantGo)
  - The platform may need to maintain the Wi-Fi connection while in standby and in any mode of operation such as clamshell, tablet, closed lid, detached, and/or convertible modes. SAR requirements will need to be met and active states must be achievable in each of the above operation modes.
- Specific Absorption Rate (SAR)
  - In situations where the platform cannot meet regulatory RF exposure requirements, the radio module's RF transmit power may need to be reduced.
- In-Device Co-Existence Interface
  - Refer [WWAN](#) on page 330 for more details on the IDC interface.

## Bluetooth

A majority of platforms are expected to use the combo Wi-Fi-BT modules. The combo modules implement co-existence schemes which allow for simultaneous operation of Wi-Fi and Bluetooth with isolation down to 15 dB; however, higher isolation offers better performance and robustness and is recommended as shown in [Table 183](#) on page 319.

If a discrete Bluetooth\* module is implemented, the isolation between the BT antenna and each Wi-Fi antenna will need to meet the isolation recommendations in [Table 183](#) on page 319. In platforms where Wi-Fi Aux antenna is also shared as the BT antenna, the Wi-Fi to BT isolation becomes the same as Wi-Fi Main to Wi-Fi Aux isolation.

## GNSS

Global Navigation Satellite System (GNSS) includes GPS, GLONASS, Galileo, Beidou, and other regional systems. Two potential integration options (and corresponding antenna choices) are supported for GNSS:

1. GNSS on the WWAN module. The WWAN Aux antenna will be required to support GPS and GLONASS frequency bands as defined in [Table 183](#) on page 319. The module will filter the GNSS signal to the GNSS modem integrated in the module.
2. Discrete GNSS solution: A standalone GNSS antenna is required, which will be connected to the RF front end of the discrete GNSS modem implementation.

## WWAN

Antenna efficiency requirements for WWAN (HSPA or LTE) antennas are listed in [Table 183](#) on page 319. WWAN modules support two antennas (Main and Aux). The WWAN-Main antenna is capable of transmit and receive functions. The WWAN-Aux antenna is a receive-only antenna and is expected to also support the GNSS frequencies.

In addition the antenna specs, the following considerations are brought to attention:

- Modern Standby Support (previously Connected Standby or InstantGo)

- The platform may need to maintain the WWAN connection while in standby and in any mode of operation such as clamshell, tablet, closed lid, detached, and/or convertible modes. SAR requirements will need to be met and active states must be achievable in each of the above operation modes.
- Specific Absorption Rate (SAR)
  - In situations where the platform cannot meet regulatory RF exposure requirements, the radio module's RF transmit power may need to be reduced. The WWAN modem has the capability of implementing dynamic power reduction (DPR) with the co-integration of a SAR proximity sensor. SAR proximity sensor pads will need to be implemented around the WWAN transmit antennas (WWAN-Main) and trigger the SAR sensor controller upon detection of the human body to send a signal through GPIO on PCH via SW or directly to the module's DPR pin. Upon receiving the trigger signal, the module will be responsible for reducing the radio's transmit power to levels required to pass the SAR limit.
  - Refer to FCC's documentation for details on RF exposure requirements.
- Tuner and Tunable Antennas:
  - It is recommended that there should be provisions to support antenna tuners with specific antenna and tuner type provided by Intel. Several antenna vendors are offering both tunable and non-tunable (passive) WWAN antennas. The passive antennas are typically easier to integrate but are larger (75 mm x 13 mm x 2 mm for global coverage LTE). The tunable antennas can be potentially smaller in size but require traces from the motherboard/module to be routed to the antenna tuning circuitry, as well as modem support to implement and verify the active tuning intelligence.
  - The Intel WWAN module can control a tuner module by means of 4 GPIO lines from the M.2 module as shown in table below. Board space for the tuner and additional tuning components and routing space for the power and control signals will need to be taken into account.

**Table 186. Intel WWAN Antenna Tuning GPIO Description**

Signal Name	SMARTi Signal	M.2 Connector Pin	Direction (WWAN)
ANTCTL0	GPO8	59	O
ANTCTL1	REFE_SDATA/GPO13	61	IO
ANTCTL2	REFE_SCLK/GPO14	63	O
ANTCTL3	REFE_VIO/GPO12	65	O

- Selection of tuning components is implementation specific and the recommended values are not hard requirements. Refer tables below for M.2 module specifications and recommendations with respect to tuners. Contact Intel RF support team for additional options.

**Table 187. M.2 Module Specifications**

Parameter	Value	Comments
Voltage	1.8 V	Applied to both GPO and REFE
Max source/sink current	-/+ 5 mA	For GPO operation. At max current up to 0.5 V output voltage drop can occur

*continued...*

Parameter	Value	Comments
REFE_VIO	20 mA	Shared between up to 8 slaves at 1.25 mA per slave plus capacitive load
REFE version	1.1	
Maximum REFE frequency	26 MHz	13 MHz optional
Number of supported tuners	configurable	Please contact Intel RF support team for details

**Table 188. M.2 Module Recommended values for Tuners**

Parameter	Value	Comments
Switching Time	<50 uS	Switching between states - REFE or GPO controlled switches
Tuner boot time	<50 uS	Time between VIO goes high and tuner is ready
REFE bus length	REFE 1.1	According to MIPI specification and depending on capacitive load

- In-Device Co-Existence Interface
  - It is recommended that platform designs implement two key mechanisms to improve coexistence when integrating Intel Connectivity and WWAN modules with the potential for simultaneous operation.
    - Maximize the isolation between Wi-Fi and WWAN antennas beyond 15 dB which will ease simultaneous operation (Refer [Table 183](#) on page 319).
    - Implement the In-Device Coexistence interface connection on the system between the Connectivity and WWAN modules to enable the use of the smart co-existence solution. Below table is an example of how the 3 coexistence signals for the IDC interface should be connected when the Intel Connectivity and WWAN solutions are implemented as modules plugged into M.2 compatible sockets on the platform.

**Table 189. In-Device Coexistence Interface**

Intel Coexistence Signal description (Signal Name)	Pin# in Connectivity socket	Signal Direction	Pin# in WWAN socket
IDC_UART_TXD (COEX1)	48	←	64
IDC_UART_RXD (COEX2)	46	→	62
GNSS_EXT_FTA (COEX3)	44	←	60

## 8.5 Standard M.2 Connectivity Design Considerations

This section describes the following:

- Standard (Discrete) Connectivity Guidelines
- PCIe\* Host Interface Errata

### 8.5.1 Standard (Discrete) Connectivity Guidelines

The platform supports both Integrated (CNVi) and Discrete (Standard M.2) connectivity modules on the M.2 socket. These are the guidelines for using the standard M.2 Wi-Fi/BT combo modules.

This section includes several important implementation aspects the OEM should take into consideration when implementing a platform that would accommodate this product.

### Socket 1 Mechanical Key Options

Socket 1 has two options: Key E and Key A. Each key with different supported list of I/Fs as defined in the M.2 specification.

In general the different Keys should be used in the following cases:

- **Key E** – when UART/I2S for BT is required.

It is possible to have a single-motherboard design that supports either of these options, and select between them using resistor assembly options.

### Signal Connection Pitfalls

- The OEM should make sure to follow the M.2 definitions of signal names and directions (I/O TX/Rx etc.) and avoid confusion between platform side and device side.

---

#### NOTE

Some lines are bidirectional, such as PCIe CLKREQ, PEWAKE.

---

### Pullups and Pulldowns

The OEM should apply pullups and pulldowns in the platform side according to below table.

**Table 190. Socket 1 Pullups and Pulldowns**

I/F	Signals	PU/PD Guidelines	Rationale
W_Disable#	Power valid to PERST# Input active	PU	May be required by M.2 cards; in Intel Wireless products there is already a PU at the silicon level.
PCIe*	PEWAKE#	PU	Open drain, required by M.2
	CLKREQ#	PU	Open drain, required by M.2
	PERST#	PD	Required by Intel platform design guidelines
	Other PCIe* signals	None	PCIe* specification

The OEM must avoid using PU/PD when not needed or when required not to be used. Unless this rule is followed, it would result in a back-bias condition, in which the IO is getting voltage before the device side is ready for it.

### IO Connection Scenarios and Best Practices

The motherboard designer should address the following requirements for the sake of avoiding failsafe problems, reducing unneeded leakage and for following best practice design rules:

- Level-shifter back-bias prevention
  - Level shifter shall not set value in A side when not getting voltage in B side.
    - **Rationale:** Prevent back-bias and wrong logic condition.
  - Level shifters shall be back-bias protected.
    - **Rationale:** The level shifter is often supplied with a different supply than the IO connected to it. During ramp up/down states there might be back-bias scenario.

#### PCIe\*

- PCIe\* is the standard M.2 interface for Wi-Fi.
- PESRT# and PEWAKE# are used for D3 flows it is possible to share these signal with other system components.
  - PERST# signal can be shared. As example Wi-Fi PERST# can be connected to a platform global PCIe reset signal.
  - Connected standby flows are using RTD3hot. RTD3hot is not using PERST#, and not using PEWAKE#
  - Non-connected standby flows are using D3cold. D3cold is using PERST# and PEWAKE#.
- If, in S3-5 the platform puts all the devices to D3cold, and will assert PERST# to all of them, then, as a result PERST# can be shared.
- Wi-Fi core can still be kept active in D3, but in that case, since it is D3cold, Wi-Fi will ignore PERST# even if it puts Wi-Fi into PCIe reset.
- Wi-Fi core can wake the system using PEWAKE# and there is added value in non-CS platforms to have dedicated PEWAKE# signals, but it is not mandatory (depend on Platform decision/needs).
- To conclude, even in non-connected standby flows the signals can be shared.

#### Connectivity Module Power Control

The platform designer has the following options to control the power rail of the connectivity module:

- **Recommended option (and a must for CNVi support):** Connect directly to a non-switched 3.3V rail. This is the only possible option when the design should also support CNVi.
  - The device will be on as long as the rail provides power.
  - The OEM can save the need to use power switch, but keep connectivity module leakage in the relevant platform states.
- **Optional (not valid for CNVi or dual discrete/CNVi support):** Connect to a 3.3V rail through power switch.
  - Control the switch using SLP\_WLAN controlling signal.
  - The SLP\_WLAN signal will keep the connectivity awake when needed, and turn it off when not needed.
  - For example, if ME in Sx is not used, and wake on WLAN in Sx is not used, then connectivity can be turned off.

## Power Feed

It is required to have decoupling caps on the power feeds in each end of the connector.

- 10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
- 10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 72 and 74.

## BIOS

The customer will need to apply the relevant CNV BIOS objects and methods, along with their appropriate settings, according to the device in use. Wrong values in the BIOS will result in unexpected behavior and degraded performance.

### 8.5.2 PCIe\* Host Interface Errata

This section includes several important implementation aspects about PCIe\* host interface. The platform designer should take these items into account as part of the platform design.

#### Squelch Detect Mechanism

The Squelch (SQ) detect mechanism may not consistently identify PCH wake signaling (TS1 symbols) as valid above SQ Maximum threshold of 175 mV, as defined in the PCIe\* specification.

It is important to follow proper platform design and layout guidelines as defined in the PCIe\* CEM specification to ensure PCH wake signaling (Electrical Idle Detect Threshold - *Vrx-idle-det-diff-p-p* parameter) in the range of:

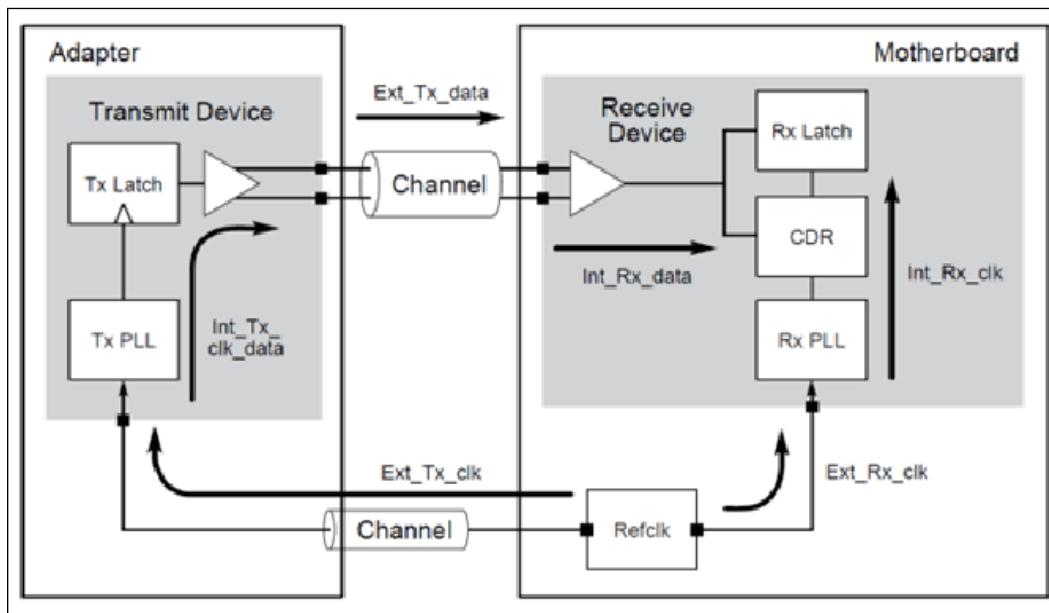
- 65 mV to 280 mV

Customers should design/plan appropriately for all adapters that may be used in a given platform.

#### PCIe\* Common Clock Configuration

PCIe\* on both platform side (PCH) and WLAN side must operate using the PCIe\* common clock configuration. Both PCH and WLAN are configured for this by default (bit 6 is set in registers 0x50). From hardware perspective, the same reference clock (Refclk) must be used for both PCH and Wi-Fi card, as shown in Figure below.

**Figure 192. PCIe\* Common Clock Configuration**



**Source:** PCI Express Rev 2.0 spec (PCI\_Express\_Base\_Rev\_2.0\_20Dec06a, figure 4-50)

#### Enabling PCIe\* Controllers with ASPM

ASPM defines the L states of the PCIe\* connections, L0, L0s, L1 and L2.

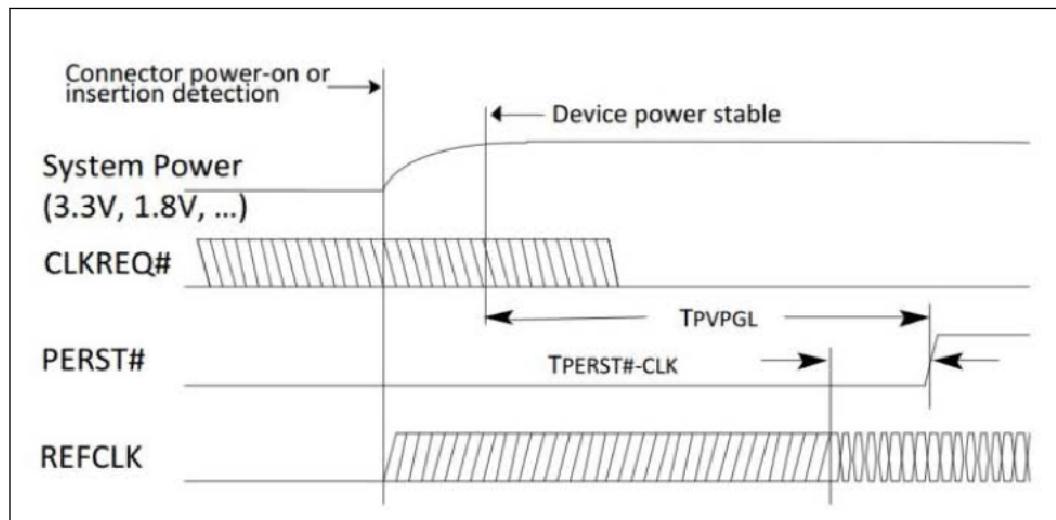
The device does not support L0s. This is in order to benefit from the power saving that is achieved with L1 state, while avoiding platform integration complexity which is involved with using L0s state.

The device supports ASPM optionality ECN, allowing support of L1 without L0s. Therefore, there is no need for special BIOS actions as with previous Intel's wireless products.

#### CLKREQ# Timing

Latest PCIe\* M.2 Specification does not specify a constraint on when PCIe\* device should assert CLKREQ# after Power Valid (which is a point where the V3.3 rail reached nominal level).

Refer to the below timing diagram and timing tables taken from PCIe\* M.2 specification and as can be seen, CLKREQ# assertion timing is not defined.

**Figure 193. PCIe\* CLKREQ# Timing**

**Source:** M.2 specification

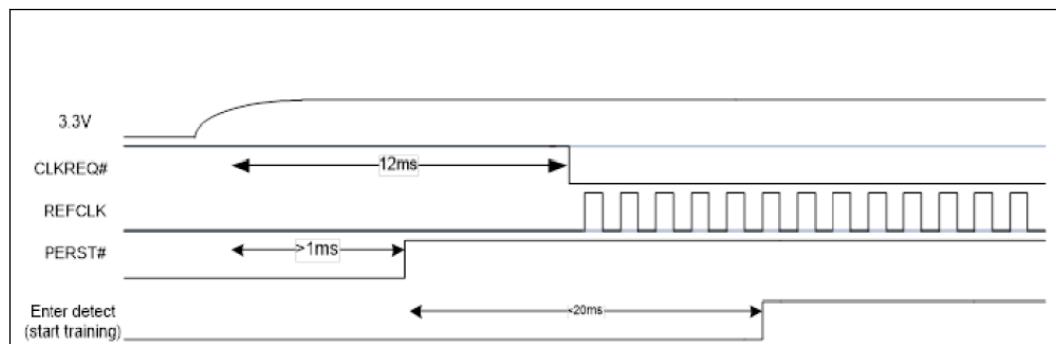
**Table 191. Power-up CLKREQ# Timing**

Symbol	Parameter	Min	Max	Units
$T_{PVPGL}$	Power valid to PERST# Input active	Implementation specific		ms
$T_{PERST\#-CLK}$	REFCLK stable before PERST# inactive	100		$\mu$ s

Cyclone peak, Thunder Peak and Windstorm peak asserts CLKREQ# within 12ms from Power valid as shown in below figure, these devices complies with the requirement to enter DETECT within 20ms of PERST# de-assertion.

#### NOTE

Refer to M.2 device specification to meet the POWER rail to PERST# timing requirements.

**Figure 194. Cold Reset**

KBG said:

Hi,

What is the difference between warm reset & cold reset (OMAP 5912) ?

This is advance,  
Karthik Balaguru

cold reset = complete removal of power and restart.

warm reset = forcing a restart via a reboot with out powering down.

The PERST# signal rise time needs to meet the limitations listed in below table. This guarantees robust out-of-reset flow of the device and better immunity to noise that can be carried by this signal. In addition, it is required that this signal rise in a monotonic way and avoid a step-like rise.

#### Power-up PERST# Timing

**Table 192. Power-up PERST# Timing**

Parameter	PERST# Rise Time			
	Intel® Wireless Devices			
	Stone Peak	Sandy Peak	Snowfield Peak	Windstorm Peak
PERST# Rise Time	< 20 nSec Monotonic rise		< 150 nSec Monotonic rise	
PERST# Ripple/Glitch During Rise Time	< 50 mV glitch during the rise rime phase		< 100 mV glitch during the rise rime phase	

#### PCI Setting for Gen 2x1 (10 Gb/s) and De-emphasis

Some platforms experienced difficulties enumerating the Wi-Fi device after warm boot. The cause of this issue is the ability to choose the right PCI interface speed. A workaround for this issue is to disable the PCI De-emphasis option in the BIOS and set speed to Gen 2x1 (10 Gb/s).

- De-emphasis disabled.
- Speed – AUTO (to allow Gen 2x1 (10 Gb/s) speed).

## 8.6

### Wireless Connectivity Integration (CNVi) Design Considerations

This section describes the following:

- Connectivity Integration (CNVi)
- Integrated Connectivity Concept
- CNVi Form Factors
- Platform Considerations
- Signal Connection Pitfalls
- Internal USB Port used in PCH
- Pull-ups and Pull-downs
- IO Connection Scenarios and Best Practices
- I/F-Specific Guidelines
- Connectivity Module Power Control
- Wi-Fi Wireless Disable and RF-Kill
- M.2 Bluetooth® HW RF-Kill
- Power Supply De-coupling
- A4WP Issues

- BIOS
- CNVi Power up Sequence

### 8.6.1 Connectivity Integration (CNVi)

Connectivity integration (CNVi) is a general term referring to a family of connectivity solutions which started with Pulsar family, and continues with Quasar family for ICL PCH/ CML PCH/ TGL PCH . The common component solution is the CNVi IP , which is a hard macro embedded in various Intel SoC chips.

The CNVi solution also contains an external RF companion module (CRF) and RF antennas. This module can be implemented in the following variations:

1. M.2 (2230)
2. Soldered-down M.2 (1216)
3. Chip-on board (COB)

For Intel® Wifi\* companion RF Symbol kit , refer to #**630287** and for Intel® Wifi\* M.2 1216 Discrete Symbol kit, refer to #**627347**.

### 8.6.2 Integrated Connectivity Concept

Integrated Connectivity (CNVi) is a new architecture for wireless connectivity devices. The concept of CNVi is to move a large part of the functional content of the connectivity chip from the radio chip into the SoC. As a result, a large portion of the chip logic and memory resources is moved out of the radio chip, reducing platform bill of material (BOM) size and cost, and improving accessibility to SoC re-sources (audio, memory, etc.).

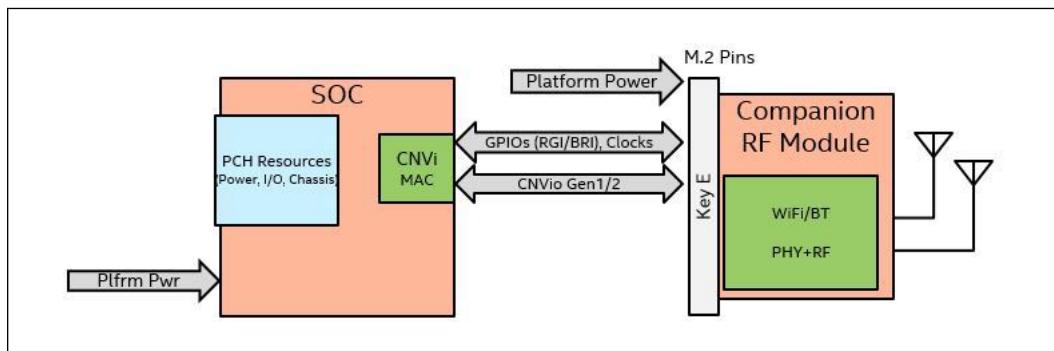
In the CNVi architecture, the MACs of the Wi-Fi and Bluetooth®, including processors, logic and memory are relocated from the radio chip into the SoC chip. Signal processing, Analog and RF func-tions stay in the radio chip, which is called a Companion RF chip (CRF) in CNVi terminology.

The part of the connectivity IP which is ported into the SoC is called Pulsar/Quasar (CNVi is the general name). The Pulsar/Quasar interfaces with the rest of the SoC functions through SoC-internal interfaces and buses, and does not require any host interfaces at the platform level. On the other hand, inter-facing the Pulsar/Quasar and the Companion RF (CRF) chip does require platform signals to be routed between the SoC and the Companion RF chip (Intel-proprietary interfaces, based on existing M.2 signals).

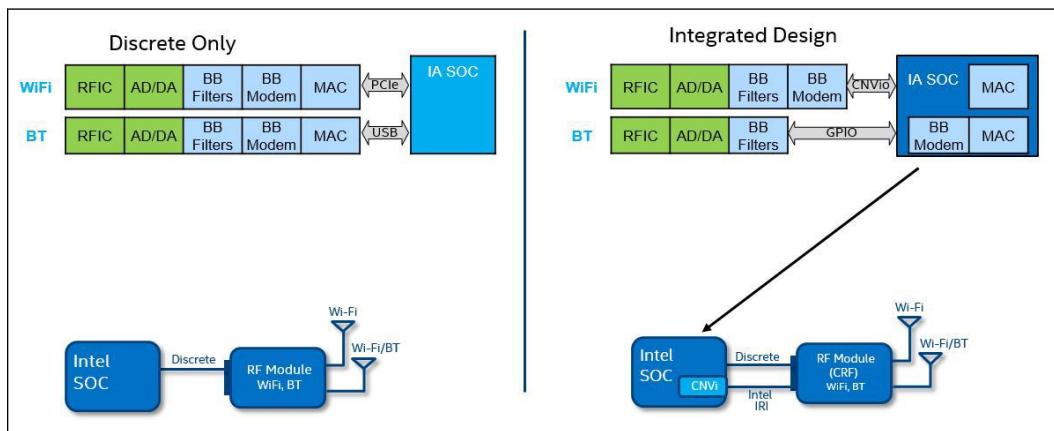
The Integrated Connectivity architecture has the MAC part of the Wi-Fi and BT cores located inside the SoC. As a result, the Host interfaces of Wi-Fi and BT are no longer part of the M.2 module, which is an RF companion module. These Host Interfaces reside in the SoC and are not exposed to the platform.

The figure below shows the Platform-level view of CNVi, including all related system components.

**Figure 195. CNVi Platform Block Diagram**



**Figure 196. CNVi Discrete vs Integrated Architecture**



The CNVi platform system includes the following blocks:

### System-on-Chip (SoC)

Quasar IP is integrated with PCH part of Multi-chip module (MCM).

### Platform Crystal

In **Quasar** generation, The CRF and the platform have, each, its own crystal. There is NO shared clock between the Wireless CRF and the PCH/Platform.

In **Pulsar** generation, The CRF share its 38.4MHz clock with the Pulsar that is in the PCH.

The CRF (code name HrP – Harrison Peak) operate with 60 MHz Crystal. The SoC and the Quasar IP uses the PCH Crystal, either 24MHz (example, CML) or 38.4MHz (example, ICL) one (depend on the Platform/PCH variant).

### WWAN Co-existence

This is a Cellular modem module, typically an M.2 card which provides cellular connectivity to the platform. The WWAN modem interacts with the CNVi through two different interfaces:

- UART- a bus used to exchange Real Time co-existence data between Wi-Fi/BT and the cellular modem.

- Aiding- signals driven by the modem, which are used to assist in improving performance.

### Platform VRs

Provides a single 3.3V rail to the external connectivity circuitry.

### CNVi Related Straps

These are pin-straps used on SoC pins. These straps control SoC initialization functions related to CNVi implementation.

Refer “Power-up sequence” Sections for the signals and power-up flow.

### Connectivity CRF/Discrete

The connectivity block can have different mechanical implementations depending on the form factor and functionality. Connectivity modules are characterized by the following properties:

- Integration level: Intel RF companion chip (CRF) or Discrete (Intel or TPV)
- Form factor: M.2 2230 (Connectorized module) or M.2 1216 or (Solder down module) Chip-on-board (COB)
- Includes both Wi-Fi and BT Cores
- Wi-Fi streams (depending on the used CRF)
- BT Stream is similar for both Previous generation (JfP) and New Generation (HrP).

### Connectivity Antennas

2x2 Configuration include:

- Wi-Fi main antenna
- Shared Wi-Fi/Bluetooth Antenna (combining Wi-Fi chain-1 and Bluetooth signals together)

1x1 Configuration include:

- Wi-Fi/Bluetooth Antenna with Diversity option (can select one of the 2 available antennas).

**Table 193. Antenna Connector Functionality**

Connector	Functionality
Wi-Fi + BT	ANT1
Wi-Fi	ANT2 (M.2-2230) / ANT3 (M.2-1216)

### 8.6.3

### CNVi Form Factors

The modules described in this section are:

- RF Companion M.2 (2230)
- RF Companion Solder-down M.2 (1216)
- RF Companion COB

## RF Companion M.2 (2230)

The RF Companion 2230 module has the same mechanical outline as the standard M.2 connectivity Type 2230-S3-E card.

The standard M.2 Key E connector pin out is modified to accommodate the proprietary RF companion signals, hence called “Hybrid Key-E”. This unique design allows inserting the RF Companion module into a standard M.2 Key E socket.

This feature is only possible when the Motherboard design follows specific guidelines described in this document.

The M.2 socket with the Hybrid Key-E scheme is intended to be used with a proprietary pinout. This scheme is called “Hybrid Key-E” due to the mechanical similarity to a Key-E connector and the ability to support both Companion RF and Discrete modules. When designing a motherboard with this scheme, it is possible to have the same M.2 socket supporting two different connectivity cards:

1. CNVi Companion RF module (CRF)
2. Standard M.2 discrete module (Discrete)

The ability to swap between these cards on the same M.2 socket, while using the same motherboard design, is an important feature desired by PC platform OEMs.

When designing the motherboard M.2 socket and routing according the Hybrid Key-E scheme, and subject to certain assumptions that will be defined later, the following basic properties are guaranteed:

- Inserting either of the optional cards (CRF, Discrete) to the M.2 socket will be safe (meaning no damage to the motherboard or card will occur).
- Both options can be used and will function as desired, subject to the following:
  1. For CNVi: CNVio/RGI/BRI and few of the CNVi-CRF signals are in place.
  2. For Discrete: all external interfaces (PCIe/USB/Controller Link) are available and connected.

The pinout for the Hybrid Key-E socket on the motherboard is shown in next Figure .The inner columns show the Companion RF proprietary signals at their assigned pins. The Companion RF signals, listed with the prefix “/”, signify that they are electrically MUX'd inside the PCH/SoC, and are shared. Due to this internal SoC sharing, these signals do not require any jumpers to select between the two functions.

---

### NOTE

There are six (6) such signals.

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- **Module Pinout**

The RF Companion 2230 module Pinout is shown in Table below.

**Table 194. RF Companion Module 2230 Pin List**

<b>Pin #</b>	<b>Pin Name Platform Pinout</b>	<b>Pin Name Spec (Product side) Pinout</b>	<b>Pin Name Module Pinout</b>	<b>Direction w/ respect to CRF Module</b>	<b>CRF Voltage on Module Side</b>	<b>Connection on Platform/Usage</b>
1	GND		GND			GND
2	3.3 V	3.3 V	3.3 V		3.3 V	3.3 V Supply
3	USB_D+	USB_D+	NC	IO	3.3 V	Not used by CRF Shall be connected to USB for Discrete support
4	3.3 V	3.3 V	3.3 V		3.3 V	3.3 V Supply
5	USB_D-	USB_D-	NC	IO	3.3 V	Not used by CRF Shall be connected to USB for Discrete support
6	LED1#	LED1#	LED1#	O	OD	LED 1 (Main, WiFi)
7	GND		GND			GND
8	PCM_CLK/I2S SCK	PCM_CLK/I2S SCK	NC	IO	1.8 V	Not used by CRF Optional UART+PCM interface when used with Discrete
9	WGR_D1N	SDIO_CLK/ SYSCLK	WGR_D1N	O	CNVio phy	CNVio bus RX lane 1
10	PCM_SYNC/I2S WS/RF_RESET_B	PCM_SYNC/I2S WS	RF_RESET_B	I	1.8 V	The PCM functionality is not used by CRF, but using this signal as RF reset indication (active low, PD) Optional UART+PCM interface when used with Discrete
11	WGR_D1P	SDIO_CMD	WGR_D1P	O	CNVio phy	CNVio bus RX lane 1
12	PCM_IN/I2S SD_IN	PCM_IN/I2S SD_IN	NC	O	1.8 V	Not used by CRF Optional UART+PCM interface when used with Discrete
13	GND	SDIO_DATA0	GND			
14	PCM_OUT/I2S SD_OUT/ CLKREQ0	PCM_OUT/I2S SD_OUT	CLKREQ0	I	1.8 V	CRF: Wake/activity request from SOC side Optional PCM interface when used with Discrete
15	WGR_D0N	SDIO_DATA1	WGR_D0N	O	CNVio phy	CNVio bus RX lane 0
16	LED2#	LED2#	LED2#	O	OD	LED secondary (BT)
17	WGR_D0P	SDIO_DATA2	WGR_D0P	O	CNVio phy	CNVio bus RX lane 0
18	GND		LNA_EN			This a special purpose test pin of the CRF module. Should be connected to Ground on the platform.

*continued...*

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to CRF Module	CRF Voltage on Module Side	Connection on Platform/Usage
19	GND	GND/SDIO DATA3	GND			
20	UART-Wake	UART WAKE#	NC	O	3.3 V	Not used by CRF Optional UART+PCM interface when used with Discrete
21	WGR_CLKN	SDIO_WAKE#	WGR_CLKN	O	CNVio phy	CNVio bus RX clock
22	UART RXD/ BRI_RSP	UART TXD	BRI_RSP	O	1.8 V	BRI bus RX, PD in CRF Optional UART+PCM interface when used with Discrete
23	WGR_CLKP	SDIO_RESET#	WGR_CLKP	O	CNVio phy	CNVio bus RX clock
24	Connector Key	Connector Key	Module Key			
25	Connector Key	Connector Key	Module Key			
26	Connector Key	Connector Key	Module Key			
27	Connector Key	Connector Key	Module Key			
28	Connector Key	Connector Key	Module Key			
29	Connector Key	Connector Key	Module Key			
30	Connector Key	Connector Key	Module Key			
31	Connector Key	Connector Key	Module Key			
32	UART TXD/ RGI_DT	UART RXD	RGI_DT	I	1.8 V	BRI bus TX, PU in CRF Optional UART+PCM interface when used with Discrete
33	GND		GND			GND
34	UART CTS/ RGI_RSP	UART RTS	RGI_RSP	O	1.8 V	RGI bus RX, PD in CRF Optional UART+PCM interface when used with Discrete
35	PETp0	PERp0	NC		PCIe phy	Not used by Harrison Peak Shall be connected to PCIe for Discrete support PCIe phy signals.
36	UART RTS/ BRI_DT	UART CTS	BRI_DT	I	1.8 V	BRI bus TX, PU in CRF
37	PETn0	PERn0	NC		PCIe phy	Not used by CRF Shall be connected to PCIe for Discrete support PCIe phy signals.
38	Controller Link RESET	<Vendor Defined> Controller Link RESET	NC			Not used by CRF Optional Controller Link interface when used with Discrete

*continued...*

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/ respect to CRF Module	CRF Voltage on Module Side	Connection on Platform/Usage
39	GND		GND			GND
40	Controller Link DATA	<Vendor Defined> Controller Link DATA	NC			Not used by CRF Optional Controller Link interface when used with Discrete
41	PERp0	PETp0	NC		PCIe phy	Not used by CRF Shall be connected to PCIe for Discrete support PCIe phy signals.
42	Controller Link CLK	<Vendor Defined> Controller Link CLK	NC			Not used by CRF Optional Controller Link interface when used with Discrete
43	PERn0	PETn0	NC		PCIe phy	Not used by CRF Shall be connected to PCIe for Discrete support PCIe phy signals.
44	COEX3 (I/O)	COEX3 (I/O)	NC			Not used by CRF Optional Coex interface with LTE modem when used with Discrete
45	GND		GND			GND
46	COEX2	COEX2				Not used by CRF Optional Coex interface with LTE modem when used with Discrete
47	REFCLKP0	REFCLKP0	NC		PCIe phy	Not used by CRF Shall be connected to PCIe for Discrete support PCIe phy signals.
48	COEX1	COEX1	NC			Not used by CRF Optional Coex interface with LTE modem when used with Discrete
49	REFCLKN0	REFCLKN0	NC		PCIe phy	Not used by CRF Shall be connected to PCIe for Discrete support PCIe phy signals.
50	SUSCLK (32 kHz)	SUSCLK (32 kHz)	C_P32K (32 kHz)	I	3.3 V	CRF also supports 1.8 V electrical levels on this signal PD in CRF
51	GND		GND			GND
52	PERST0#	PERST0#	NC		3.3 V	Not used by CRF

*continued...*



Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to CRF Module	CRF Voltage on Module Side	Connection on Platform/Usage
						Shall be connected to PCIe for Discrete support
53	CLKREQ0#	CLKREQ0#	NC		3.3 V	PCIe clock request. Not used by CRF Shall be connected to PCIe for Discrete support
54	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	I	3.3 V	CRF also supports 1.8 V electrical levels on this signal PU in CRF
55	PEWAKE0#	PEWAKE0#	NC		3.3 V	Not used by CRF Shall be connected to PCIe for Discrete support
56	W_DISABLE1#	W_DISABLE1#	W_DISABLE1#	I	3.3 V	CRF also supports 1.8 V electrical levels on this signal PU in CRF
57	GND		GND			GND
58	PER1p0	I2C DATA/ UART_TX	NC		1.8 V	Not used by CRF
59	WT_D1N	WT_D1N <PERp1>	WT_D1N		CNVio phy	CNVio bus TX lane 1
60	PER1n0	I2C CLK/ UART_RX	NC		1.8 V	Not used by CRF
61	WT_D1P	WT_D1P <PER1n1>	WT_D1P	I	CNVio phy	CNVio bus TX lane 1
62	GND	ALERT#/ UART_RTS	NC		1.8 V	Not used by CRF
63	GND		GND			GND
64	PET1p0	REFCLK0/ UART_CTS <Reserve>	REFCLK0	O	1 V	Not used by CRF
65	WT_D0N	WT_D0N <PET1p1>	WT_D0N	I	CNVio phy	CNVio bus TX lane 0
66	PET1n0	PERST1#	NC			Not used by CRF
67	WT_D0P	WT_D0P <PET1n1>	WT_D0P	I	CNVio phy	CNVio bus TX lane 0
68	CLKREQ1#	CLKREQ1#	NC			Not used by CRF
69	GND		GND			GND
70	UIM_POWER_ SRC/GPIO1/ PEWAKE1#	UIM_POWER_ SRC/GPIO1/ PEWAKE1#	NA			Not used by CRF

*continued...*

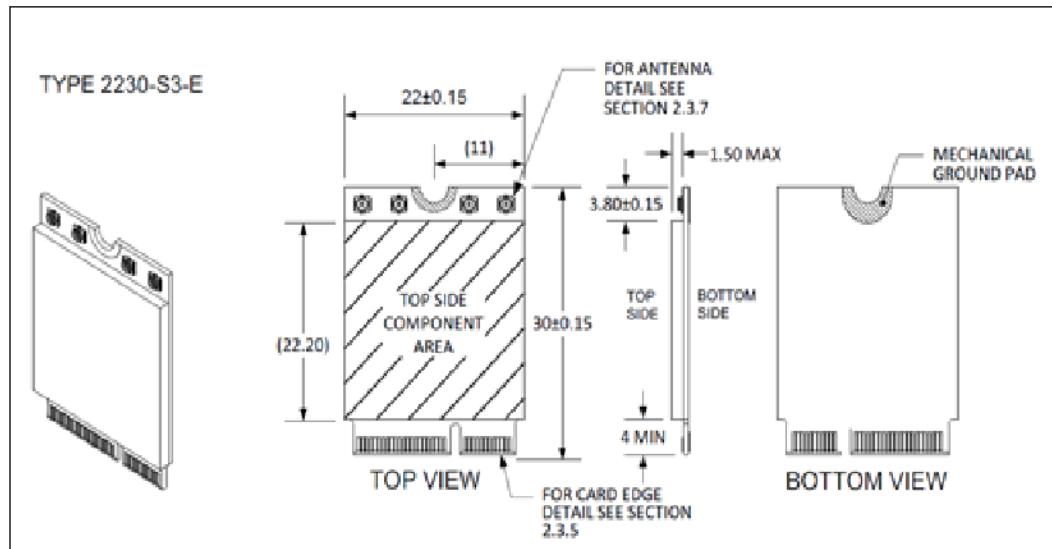
Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/ respect to CRF Module	CRF Voltage on Module Side	Connection on Platform/Usage
71	WT_CLKN	WT_CLKN <REFCLKP1>	WT_CLKN	I	CNVio phy	CNVio bus TX clock
72	3.3 V	3.3 V	3.3 V			3.3 V Supply
73	WT_CLKP	WT_CLKP <REFCLKN1>	WT_CLKP	I	CNVio phy	CNVio bus TX clock
74	3.3 V	3.3 V	3.3 V			3.3 V Supply
75	GND		GND			GND

Note: PU is Pull up and PD is pull down.

- **Module Mechanical Dimensions**

The M.2 2230 CRF Module mechanical diagram is shown in figure below.

**Figure 197. Module Mechanical Diagram**



**NOTE**

Source is PCI-SIG M.2 Specification.

- **Hybrid Key-E (2230) Pin-Out**

The RF Companion M.2 2230 module is intended to be used with a proprietary pin out "Hybrid Key E" scheme due to the mechanical similarity to a Key-E connector.

The pinout for Hybrid Key-E socket on MB is shown in figure below. The CRF signals listed with the prefix "/" signify that they are electrically MUX'd inside the PCH/SoC and are shared.

Figure 198. Hybrid Key E'Pinout- Platform Side View

Single Key Platform Slot Pinout			
PS - Bottom		CS - Top	
	Standard M.2 Key E	Next Gen iCNV Signals	Standard M.2 Key E
74	+V3P3A		GND
72	+V3P3A	WT_CLKP	REFCLKN1
70	PEWake1#(IO)(0/3.3V)	WT_CLKN	REFCLKP1
68	CLKREQ1#(IO)(0/3.3V)		GND
66	PERST1#(O)(0/3.3V)	WT_DOP	PERn1
64	RESERVED	WT_DON	PERp1
62	ALERT#(IO)(1.8)	REFCLK0-(1V@33.4MHz)	GND
60	I2C_CLK (O)(0/1.8V)	A4WP_JRC# Not Used	WT_D1P
58	I2C_DATA (IO)(0/1.8)	A4WP_J2C_Glk Not Used	WT_D1N
56	W_DISABLE1#(O)(0/3.3V)	A4WP_J2C_Data Not Used	GND
54	W_DISABLE2#(O)(0/3.3V)		PEWake0#(IO)(0/3.3V)
52	PERST0#(O)(0/3.3V)		CLKREQ0#(IO)(0/3.3V)
50	SUSCLK(32kHz) (O)(0/3.3V)	C_P32K (3.3V Tolerant)	GND
48	COEX_TXD (O)(0/1.8V)		REFCLKNO
46	COEX_RXD (O)(0/1.8V)		REFCLKPO
44	COEX3 (IO)(0/1.8V)		GND
42	CLink CLK		PERn0
40	CLink DATA		PERp0
38	CLink RESET (O)(0/3.3V)		GND
36	LPSS UART RTS (O)(0/1.8V)	/BRI_DT [MUX'd in PCH/SoC]	PETn0
34	LPSS UART CTS (I)(0/1.8V)	/RGI_RSP [MUX'd in PCH/SoC]	PETp0
32	LPSS UART Tx (O)(0/1.8V)	/RGI_DT [MUX'd in PCH/SoC]	GND
E	Connector Key		Connector Key
	Connector Key		Connector Key
	Connector Key		Connector Key
	Connector Key		Connector Key
22	LPSS UART Rx (I)(0/1.8V)	/BRI_RSP [MUX'd in PCH/SoC]	WGR_CLKP
20	UARTWake#(I)(0/3.3V)		SDIO Reset#(O)(0/1.8V)
18	GND	GND/LNA_EN (LcP Production)	WGR_CLKN
16	LED2#(I)(OD)		SDIO Wake#(I)(0/1.8V)
14	PCM_OUT (O)(0/1.8V)	/CLKREQ0 [MUX'd in PCH/SoC]	GND
12	PCM_IN (I)(0/1.8V)		SDIO DAT3#(IO)(0/1.8V)
10	PCM_SYNC (O)(0/1.8V)	/RF_RESET_B [MUX'd in PCH/SoC]	WGR_DOP
8	PCM_CLK (O)(0/1.8V)		SDIO DAT2#(IO)(0/1.8V)
6	LED1#(I)(OD)		WGR_DON
2	+V3P3A		SDIO DAT1#(IO)(0/1.8V)
			SDIO DATA#(IO)(0/1.8V)
			SDIO CMD#(O)(0/1.8V)
			SDIO CLK#(O)(0/1.8V)
			GND
			USB_D
			E
			1

- Special Considerations for Hybrid Key-E Scheme

The “Hybrid Key-E” scheme relies on assigning multiple functions to M.2 connector pins and to PCH pins. This causes a significant reduction in the amount of signals that needs to be routed between the SoC and the M.2 module, at the expense of additional dependency between modes, and the loss of some functionality. The dependencies between multiple function pins and M.2 card functionality is described in the next Sections.

- Shared M.2 Socket Pins

The following M.2 pins are shared between different functions:

- **V3P3A, GND**

These are the M.2 card power supply (3.3V) and Ground pins, respectively. Both have multiple pins on the connector. These pins have the same purpose in either Discrete or CNVi implementations, and therefore are not affected by the Hybrid Key-E scheme

- **PCIe-1/CNVio**

These are 6 pins which are assigned to the PCIe-1 bus in the M.2 standard pinout. This bus has 3 differential pairs, two for the PCIe data lanes (one per direction) and one for the PCIe clock. In the "Hybrid Key-E" scheme these signals are used for CNVio interface from Pulsar/Quasardo the RF companion chip. Due to this sharing, the "Hybrid Key -E" scheme does not support PCIe-1.

#### — **SDIO/CNVio**

These are 8 pins which are assigned to the SDIO bus in the M.2 standard pinout. This bus has 8 signals, 4 bi-directional for the SDIO data, one bi-directional command signal, one clock (SoC to M.2) and 2 control (Reset SoC to M.2, Wake M.2 to SoC). In the "Hybrid Key-E" scheme these signals are used for CNVio interface the RF companion chip to Pulsar (6 for CNVio and 2 for ground). Due to this sharing, the "Hybrid Key-E" scheme does not support SDIO.

#### — **PCM/ClockReq and Reset**

The standard M.2 defines 4 pins for a dedicated PCM audio serial bus for BT. In the "Hybrid Key-E" scheme, two of these signals are used for CRF Clock Request - a wake indication from SOC to CRF and Reset (For SoC to RF companion). Since the PCM serial bus is connected to PCH GPIO pins, and the CNVi clock request and reset pins are also connected to PCH GPIO pins, it is possible to have support for both PCM bus and CNVi signals by changing the PCH GPIO multiplexing function select. Due to this sharing, the "Hybrid Key-E" scheme can still support PCM (for discrete BT connectivity with PCM support).

#### — **UART (BT) / BRI and RGI**

The standard M.2 defines 4 pins for a dedicated UART serial bus for Bluetooth. In the "Hybrid Key-E" scheme, all these signals are used for CNVi BRI (Bluetooth\* Radio Interface) and RGI (Radio Generic interface), each comprising of 2 signals (one per direction). Since the UART serial bus is connected to PCH GPIO pins, and the CNVi BRI, RGI are also connected to PCH GPIO pins, it is possible to have support for both UART bus and CNVi signals by changing the PCH GPIO multiplexing function select. Due to this sharing, the "Hybrid Key-E" scheme can still support BT UART (for discrete connectivity with BT-UART support).

In the CRF, we have Pull-Up on the RGI/BRI \_DT and Pull Down on the RGI/BRI\_RST signal.

#### — **SUSCLK/P\_32K**

These signals are both functionally similar. In the M.2 standard, this pin is optionally connected to a 32kHz RTC clock.

In the Hybrid Key-E scheme for CNVi, it should be connected to a 32kHz clock. In the CRF, there is an option to use either an internal 32kHz clock or this external clock. The decision can be made by an auto-detect mechanism that checks whether the external 32kHz clock is indeed active (configurable option), and selects it if so, else it will choose the internal clock.

The "price" is additional power consumption in low-power states. If an external clock is used, it MUST be driven by a valid 32kHz clock any time the RF companion module is powered on (no glitches are allowed), and a BIOS/ACPI based indication is needed as well (refer "*Intel Connectivity Platforms BIOS Guidelines*").

The 32kHz clock can come from a PCH pin or from a different source on the platform, depending on the platform used. Note that the External 32kHz accuracy is assumed to be 20ppm.

In HrP this signal is 1.8v based and is tolerant to 3.3v.

#### — **GND/LNA\_EN**

This signal is used for different purposes in CNVi and discrete but in both cases should be connected to ground, therefore it does not affect functionality.

- **NFC I/F, and A4WP+Ref clock (relevant for JfP Only – not used in HrP)**

In the Hybrid Key-E scheme, only one of these four signals is used. The REFCLK0 (in JfP case) signal connects the reference clock (single ended, 1V p-p, 38.4 MHz) from the RF companion to the SoC. The remaining three signals are not used.

- **A4WP+Ref clock (relevant for JfP Only – not used in HrP)**

In the “Hybrid Key-E” scheme only one of these 4 signals used. This REFCLK0 signal connects the reference clock (single ended, 1V p-p, 38.4MHz) from the RF companion to the SoC, but only with JfP \* cases. The remaining 3 signals are not used, the signals were saved for A4WP needs but A4WP is no longer relevant and not supported by the platforms.

- **RF\_RESET\_B**

This is an Intel proprietary signal between the SoC and the CRF, used as internal RESET indication from the SoC to the CRF used during the init flow of the CNVi based modules. This signal has an internal Pull-Down in HrP side.

- **ClkReq0 (Pin14 in M.2-2230, A43 in 1216)**

This is an Intel proprietary signal between the SoC and the CRF , used as Wake indication from the SoC to the CRF

This signal has an internal Pull-Down in HrP side. It is also shared with Optional PCM interface that can be used with Discrete Module solution (Non CRF)

- **Non-shared M.2 Socket Pins**

The functions of these pins impacted by the “Hybrid Key-E” scheme as will be described below:

- **V3P3A, GND**

These are the M.2 card power supply (3.3V) and Ground pins. These pins have the same purpose in either discrete or CNVi implementations and therefore are not affected by the “Hybrid Key-E” scheme.

- **PEWake1#, CLKREQ1#, PERST1#**

These are 3 control signals used by the PCIe-1 bus in standard M.2 cards. Although these signals are not shared with any other function, they have no usage in a “Hybrid Key-E” scheme design. This is because the PCIe-1 bus by itself is not usable (refer PCIe-1/CNVio sharing above).

- **PCIe-0 Bus**

This consists of 6 signals (3 differential pairs) used for PCIe data to and from the SoC, and a single pair used for the PCIe bus clock. In a CNVi RF companion these signals are left unused. In standard discrete these signals are being used as the Wi-Fi bus interface.

- **W\_DISABLE1#, W\_DISABLE2#,**

These are used for Wi-Fi and BT RF-Kill control respectively. Asserting these signals effectively shuts off the RF transmission or the relevant core.

Jefferson/Harrison Peak M.2 modules support receiving a wireless disable (RF-KILL) command through the two RF-KILL pins for turning off Wi-Fi and BT, respectively. These pins can be connected to a platform switch or to SoC GPIOs (recommendation- if possible do not use GPIOs that have Platform impact as "bootstraps" during platform init).

The RF-Kill signals (Wireless disable\*) have an internal Pull-Up in HrP side (they are "Active Low" signals).

- **PEWake0#, CLKREQ0#, PERST0#**

These are 3 control signals used by the PCIe-0 bus in standard M.2 cards. They should be routed to SoC pins which are assigned to GPIOs in Discrete or Combo modes.

- **Coex UART Interface**

This consist of 3 signals (two UART bus signals and one GPIO) used for Wi-Fi - LTE coexistence signaling in the M.2 standard definition.

Since these pins are left unused in the RF companion, they can still be used with a discrete M.2 card even when designing with the "Hybrid Key-E" scheme.

In platforms that are designed to support a WWAN modem and "Hybrid Key-E" there should be 3 pins connected to each signal, to allow the modem to connect to the M.2 pin (in the discrete connectivity case) or to the PCH (in the CNVi case) refer "Modem Coexistence 3-way UART Connection" section below.

- **CLink Interface**

This I/F is relevant, and is a MUST for vPRO based platforms. This consist of 3 signals (clock, data and reset). This bus in an Intel proprietary bus. Since these pins are left unused in the RF companion, but they will still be used with a discrete M.2 card even when designing with the "Hybrid Key-E" scheme on vPRO based platforms.

- **LED1, LED2**

These are optional pins that are assigned to drive LEDs on the platform in the standard M.2 cards. They are used for the same function when using CNVi and therefore are not affected by the "Hybrid Key-E" scheme.

- **USB Bus**

The standard M.2 defines 2 pins for a differential USB bus. This has no usage in the RF companion.

When using a standard M.2 discrete card, the pins will have the standard functionality and are not affected by the "Hybrid Key-E" scheme. The different connectivity interfaces as used by a discrete connectivity (Standard M.2, Intel connectivity or TPV), CNVi RF companion card are summarized in table below.

**Table 195. Connectivity Interfaces for Different M.2 2230 Cards**

M.2 interface	CNVi	Discrete
PCIe-1	M.2 pins are not connected to the CRF. Wi-Fi uses internal IOSF to interface the host.	Used for Wi-Fi host interface
PCIe-2	Not functional Pins are connected to CRF and Pulsar CNVio and can't be used as PCIe.	Not functional Pins are connected to Pulsar CNVio and can't be used as PCIe.
Wi-Fi SDIO	Not functional	Not functional

*continued...*

M.2 interface	CNVi	Discrete
	Pins are connected to CRF and Pulsar CNVi and can't be used as SDIO.	Pins are connected to Pulsar CNVi and can't be used as SDIO.
Wi-Fi Controller Link	M.2 pins are not connected to the CRF. Wi-Fi uses internal Controller Link to interface the ME.	Used for Wi-Fi CSME interface
Wi-Fi RF-Kill	Used (optional)	Used (optional)
BT USB	M.2 pins are not connected to the CRF. BT uses internal U2U to interface the host.	Used for BT USB interface
BT UART	M.2 pins are not connected to the CRF. BT uses internal UART to interface the host.	Used for BT UART interface
BT I2S (Audio)	M.2 pins are not connected to the CRF. BT uses internal I2S to interface the host.	Used for BT I2S interface
BT wake	M.2 pin is not connected to the CRF. BT uses internal vGPIO.	Used for BT wake signal
BT RF-Kill	Used (optional)	Used (optional)
UART bus to ISH	Pins are connected to Refclock (38.4M system clock). An internal UART is used to connect Pulsar to ISH	Pins are connected to Refclock (38.4M system clock). Can be used for ISH UART connection.
I2C bus to A4WP	Unused.	Unused.
Power supply	Used per M.2 standard	Used per M.2 standard
GND	Used per M.2 standard	Used per M.2 standard

- **Other General Recommendations**

The Following Pins are not in use and, at least on the Intel RVPs it is recommended to Not Connect or connect to test points:

- Pins 58,60,62,64, 68, 70 will be TP (or disconnected).
- Pin 66 can be connected to the “platform reset” BUT notice that Intel Wireless Products will not respond to this specific signal and will ignore it.

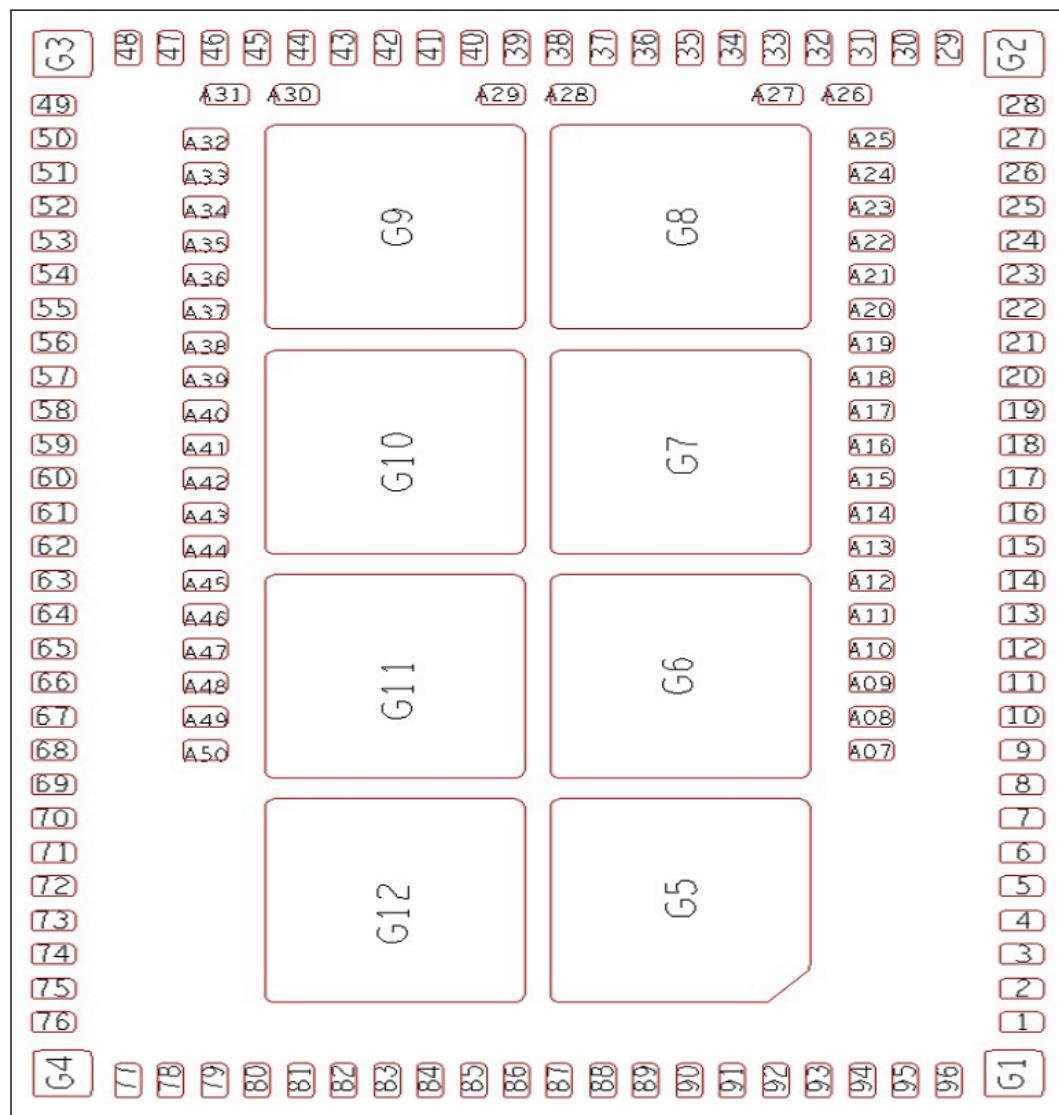
### Soldered Down M.2 (SD-1216)

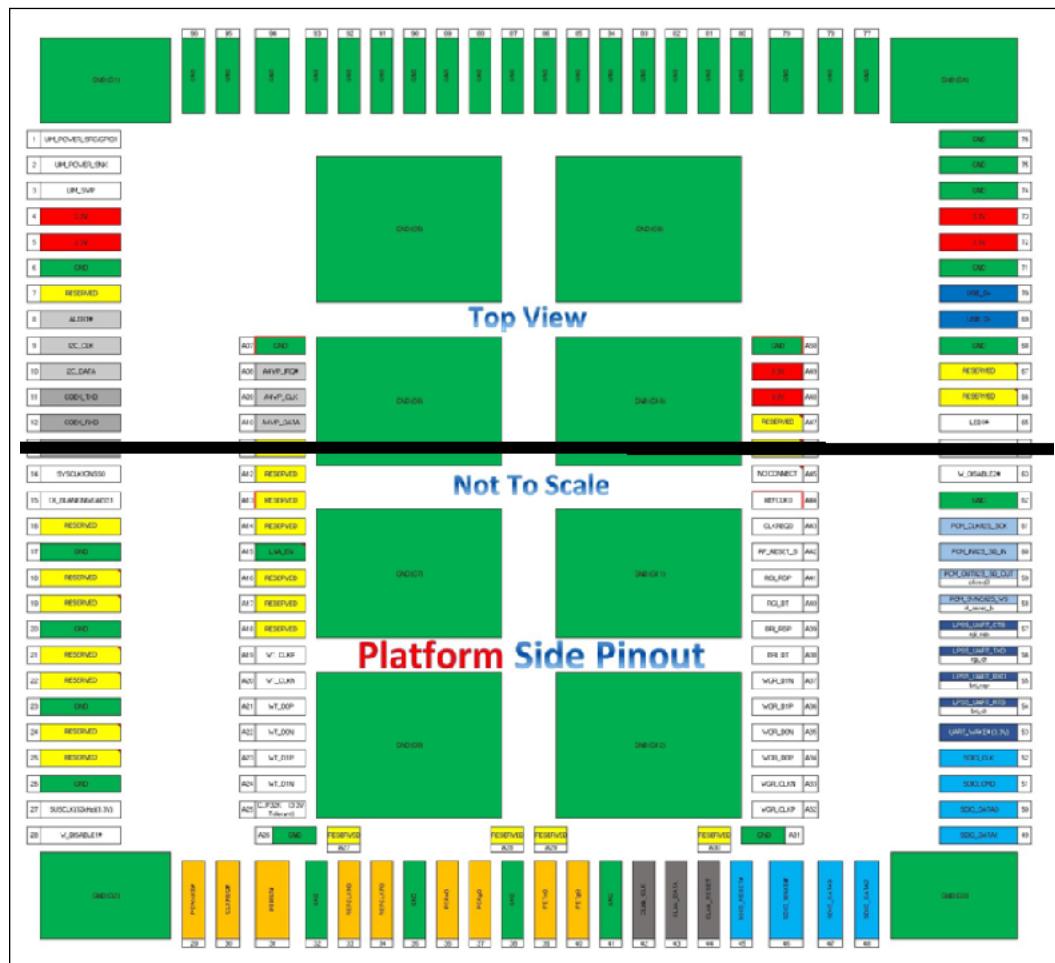
The RF Companion SD-1216 module has the same mechanical outline as the standard M.2 connectivity type 1216-S3. The standard M.2 land pattern is modified to accommodate the proprietary RF Companion Module signals. As opposed to the Connectorized module, the SD-1216 module is not sharing the standard M.2 pads for the RF companion functions. Instead, it has an additional set of solder pads which don't overlap with the standard solder pads. This allows having a single motherboard design that can accommodate either a standard M.2 1216 card or an RF companion 1216 card. However unlike the connectorized case, swapping cards requires removing a soldered down module and can't be done by a simple socket card exchange. Additionally the assembly tooling and BOM should change between a discrete and CNVi motherboards assembly.

- **Soldered Down 1216 Module Pinout**

As explained above, the RF companion module M.2 1216 card has a proprietary set of pads and does no reuse the standard M.2 pads. The special pad-out required for supporting CNVi and discrete on the same motherboard real-estate is shown in figure below. The corresponding pin-description and CRF signals are shown in figure and table below, respectively.

**Figure 199. SD-1216 Module Pad-out for Supporting CNVi and Discrete 1216 Modules**



**Figure 200. Pin Out Scheme for Dual CNVi/Discrete 1216 Footprint**


Please refer document # : 627347 and 630287 for LP pattern guidelines.

**Table 196. RF Companion Module 1216 Pin List (CNVi Only)**

Pin #	Pin Name	Function When CNVi is Used	Function when Standard M.2 is Used
1	UIM_POWER_SRC/GPIO1	Not used	UIM_POWER_SRC/GPIO1
2	UIM_POWER_SNK	Not used	UIM_POWER_SNK
3	UIM_SWP	Not used	UIM_SWP
4	3.3V	3.3V	3.3V
5	3.3V	3.3V	3.3V
6	GND	GND	GND
7	RESERVED	Not used	RESERVED
8	ALERT#	Not used	ALERT#
9	I2C_CLK	Not used	I2C_CLK
10	RESERVED		
11	RESERVED		
12	RESERVED		
13	RESERVED		
14	RESERVED		
15	RESERVED		
16	RESERVED		
17	RESERVED		
18	RESERVED		
19	RESERVED		
20	RESERVED		
21	RESERVED		
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34	RESERVED		
35	RESERVED		
36	RESERVED		
37	RESERVED		
38	RESERVED		
39	RESERVED		
40	RESERVED		
41	RESERVED		
42	RESERVED		
43	RESERVED		
44	RESERVED		
45	RESERVED		
46	RESERVED		
47	RESERVED		
48	RESERVED		

*continued...*

Pin #	Pin Name	Function When CNVi is Used	Function when Standard M.2 is Used
10	I2C_DATA	Not used	I2C_DATA
11	COEX_TXD	Not used	COEX_TXD
12	COEX_RXD	Not used	COEX_RXD
13	COEX3	Not used	COEX3
14	SYSCLK/GNSS0	Not used	SYSCLK/GNSS0
15	TX_BLANKING/GNSS1	Not used	TX_BLANKING/GNSS1
16	RESERVED	Not used	RESERVED
17	GND	GND	GND
18	RESERVED	Not used	Not used
19	RESERVED	Not used	Not used
20	GND	GND	GND
21	RESERVED	Not used	Not used
22	RESERVED	Not used	Not used
23	GND	GND	GND
24	RESERVED	Not used	Not used
25	RESERVED	Not used	Not used
26	GND	GND	GND
27	SUSCLK(32kHz)(3.3V)	Not used	SUSCLK(32kHz)(3.3V)
28	W_DISABLE1#	W_DISABLE1#	W_DISABLE1#
29	PEWAKE#	Not used	PEWAKE#
30	CLKREQ#	Not used	CLKREQ#
31	PERST#	Not used	PERST#
32	GND	GND	GND
33	REFCLKN0	Not used	REFCLKN0
34	REFCLKP0	Not used	REFCLKP0
35	GND	GND	GND
36	PERn0	Not used	PERn0
37	PERp0	Not used	PERp0
38	GND	GND	GND
39	PETn0	Not used	PETn0
40	PETp0	Not used	PETp0
41	GND	GND	GND
42	CLink CLK	Not used	CLink CLK
43	CLink DATA	Not used	CLink DATA
44	CLink RESET	Not used	CLink RESET

*continued...*

Pin #	Pin Name	Function When CNVi is Used	Function when Standard M.2 is Used
45	SDIO_RESET#	Not used	Not used
46	SDIO_WAKE#	Not used	Not used
47	SDIO_DATA3	Not used	Not used
48	SDIO_DATA2	Not used	Not used
49	SDIO_DATA1	Not used	Not used
50	SDIO_DATA0	Not used	Not used
51	SDIO_CMD	Not used	Not used
52	SDIO_CLK	Not used	Not used
53	UART_WAKE# (3.3V)	Not used	UART_WAKE# (3.3V)
54	LPSS_UART_RTS/bri_dt	Not used	LPSS_UART_RTS/bri_dt
55	LPSS_UART_RXD/bri_rsp	Not used	LPSS_UART_RXD/bri_rsp
56	LPSS_UART_TXD/rgi_dt	Not used	LPSS_UART_TXD/rgi_dt
57	LPSS_UART_CTS/rgi_rsp	Not used	LPSS_UART_CTS/rgi_rsp
58	PCM_SYNC/I2S_WS	Not used	PCM_SYNC/I2S_WS
59	PCM_OUT/I2S_SD_OUT	Not used	PCM_OUT/I2S_SD_OUT
60	PCM_IN/I2S_SD_IN	Not used	PCM_IN/I2S_SD_IN
61	PCM_CLK/I2S_SCK	Not used	PCM_CLK/I2S_SCK
62	GND	GND	GND
63	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#
64	LED2#	LED2#	LED2#
65	LED1#	LED1#	LED1#
66	RESERVED	Not used	RESERVED
67	RESERVED	Not used	RESERVED
68	GND	GND	GND
69	USB_D-	Not used	USB_D-
70	USB_D+	Not used	USB_D+
71	GND	GND	GND
72	3.3V	3.3V	3.3V
73	3.3V	3.3V	3.3V
74	GND	GND	GND
75	GND	GND	GND
76	GND	GND	GND
77	GND	GND	GND
78	GND	GND	GND
79	GND	GND	GND

*continued...*

Pin #	Pin Name	Function When CNVi is Used	Function when Standard M.2 is Used
80	GND	GND	GND
81	GND	GND	GND
82	GND	GND	GND
83	GND	GND	GND
84	GND	GND	GND
85	GND	GND	GND
86	GND	GND	GND
87	GND	GND	GND
88	GND	GND	GND
89	GND	GND	GND
90	GND	GND	GND
91	GND	GND	GND
92	GND	GND	GND
93	GND	GND	GND
94	GND	GND	GND
95	GND	GND	GND
96	GND	GND	GND
G1	GND	GND	GND
G2	GND	GND	GND
G3	GND	GND	GND
G4	GND	GND	GND
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	GND	GND	GND
G12	GND	GND	GND
A07	GND	GND	Not Applicable
A08	A4WP_IRQ#	PU – Pull Up PD – Pull Down Not Applicable	Not Applicable
A09	A4WP_CLK	PU – Pull Up PD – Pull Down Not Applicable	Not Applicable
A10	A4WP_DATA	PU – Pull Up	Not Applicable

*continued...*

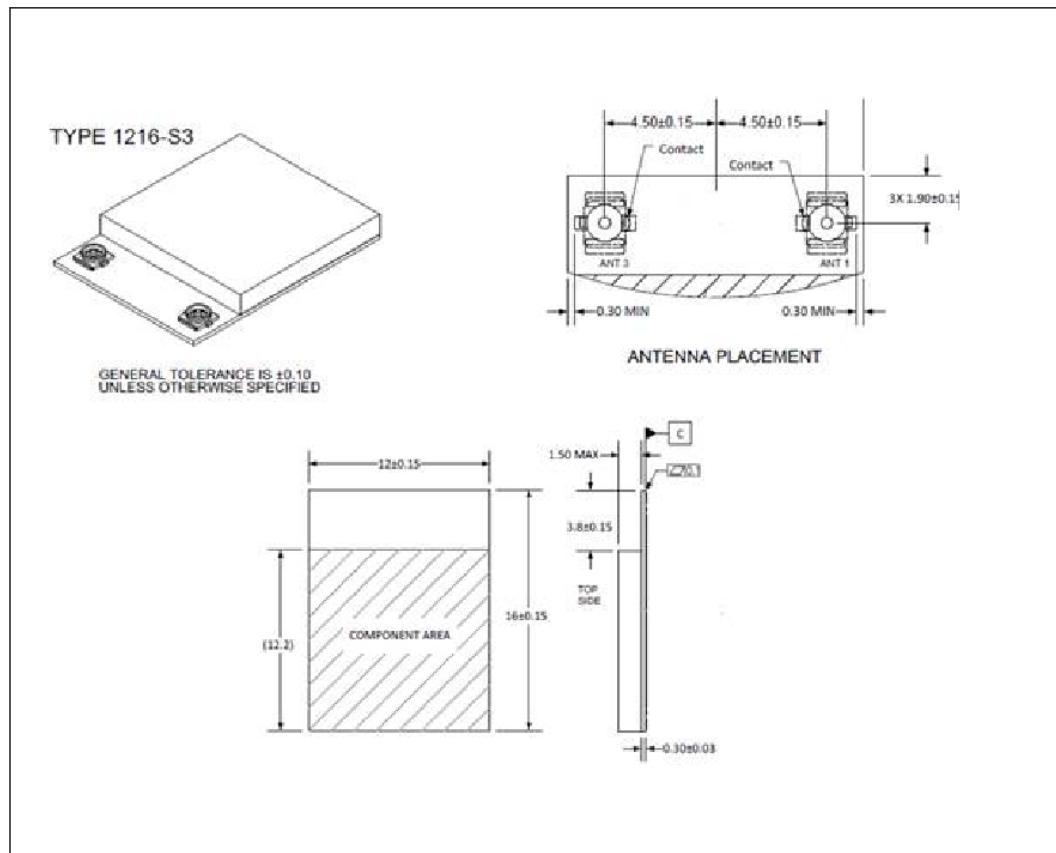
<b>Pin #</b>	<b>Pin Name</b>	<b>Function When CNVi is Used</b>	<b>Function when Standard M.2 is Used</b>
		PD – Pull Down Not Applicable	
A11	RESERVED	RESERVED	Not Applicable
A12	RESERVED	RESERVED	Not Applicable
A13	RESERVED	RESERVED	Not Applicable
A14	RESERVED	RESERVED	Not Applicable
A15	LNA_EN	GND	Not Applicable
A16	RESERVED	RESERVED	Not Applicable
A17	RESERVED	RESERVED	Not Applicable
A18	RESERVED	RESERVED	Not Applicable
A19	WT_CLKP	WT_CLKP	Not Applicable
A20	WT_CLKN	WT_CLKN	Not Applicable
A21	WT_D0P	WT_D0P	Not Applicable
A22	WT_D0N	WT_D0N	Not Applicable
A23	WT_D1P	WT_D1P	Not Applicable
A24	WT_D1N	WT_D1N	Not Applicable
A25	C_P32K	C_P32K	Not Applicable
A26	GND	GND	Not Applicable
A27	RESERVED	RESERVED	Not Applicable
A28	RESERVED	RESERVED	Not Applicable
A29	RESERVED	RESERVED	Not Applicable
A30	RESERVED	RESERVED	Not Applicable
A31	GND	GND	Not Applicable
A32	WGR_CLKP	WGR_CLKP	Not Applicable
A33	WGR_CLKN	WGR_CLKN	Not Applicable
A34	WGR_D0P	WGR_D0P	Not Applicable
A35	WGR_D0N	WGR_D0N	Not Applicable
A36	WGR_D1P	WGR_D1P	Not Applicable
A37	WGR_D1N	WGR_D1N	Not Applicable
A38	BRI_DT	BRI_DT	Not Applicable
A39	BRI_RSP	BRI_RSP	Not Applicable
A40	RGI_DT	RGI_DT	Not Applicable
A41	RGI_RSP	RGI_RSP	Not Applicable
A42	RF_RESET_B	RF_RESET_B	Not Applicable
A43	CLKREQ0	Disconnected/floating on M.2 side	Not Applicable

*continued...*

Pin #	Pin Name	Function When CNVi is Used	Function when Standard M.2 is Used
A44	REFCLK0	REFCLK0	Not Applicable
A45	NO CONNECT	NO CONNECT	Not Applicable
A46	RESERVED	RESERVED	Not Applicable
A47	RESERVED	RESERVED	Not Applicable
A48	3.3V	3.3V	Not Applicable
A49	3.3V	3.3V	Not Applicable
A50	GND	GND	Not Applicable

- **Soldered Down 1216 Module Mechanical Dimensions**

**Figure 201. 1216 Module Mechanical Diagram**



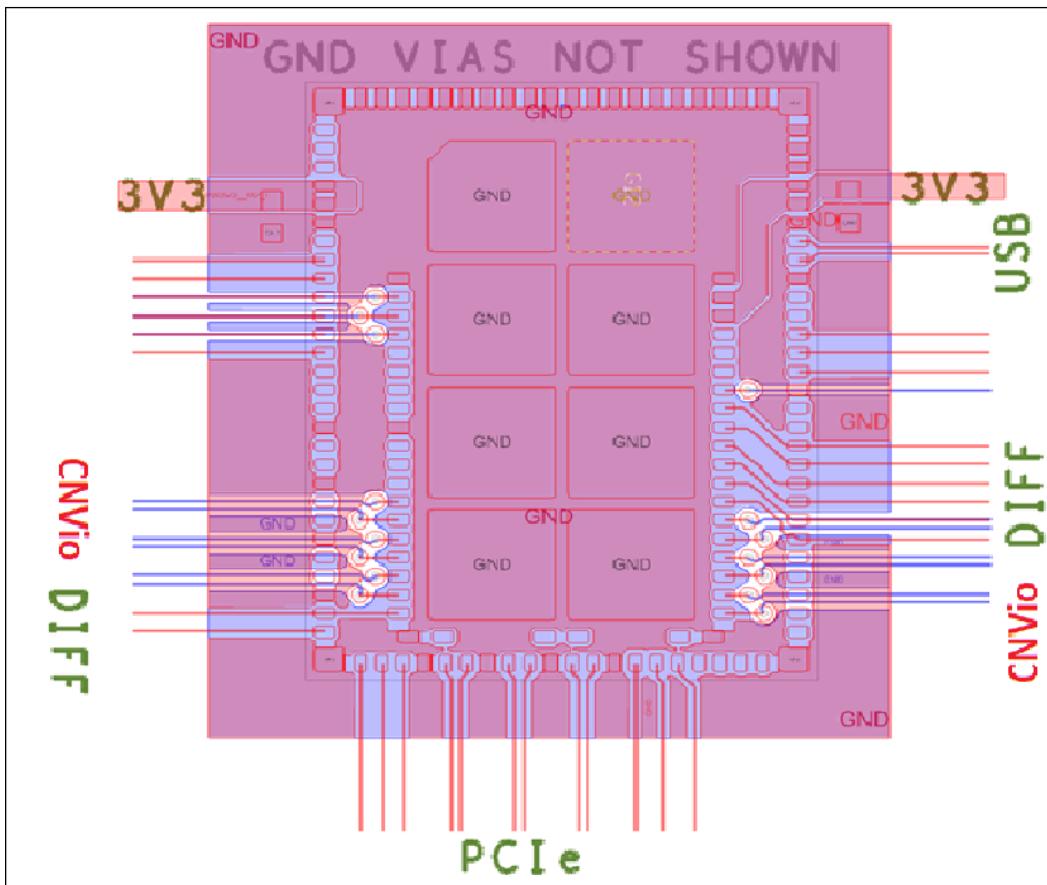
- **Breakout Example for HrP/JfP Soldered Down Module**

The soldered down HrP/JfP modules have a special pad shape which combines the standard M.2 pad ring on the outside with the new inner ring of the CNVi pads. It is recommended to consider all signal properties when designing the motherboard for dual discrete/CNVi design supporting Jefferson/Harrison Peak 1216. An example for the breakout layout for a type-3 board (with no micro-via) is shown in the figure below.

**NOTE**

In order to keep the picture clear, this example shows only two signal layers (top layer and 3rd layer) while the other layers are not shown. Also there is an assumption that the second layer shall be ground.

**Figure 202. Board Layout Example Showing Breakout from JfP 1216 Pads**



## 8.6.4 Platform Considerations

### Selecting Connectivity Solution

The platform motherboard can be designed to support discrete connectivity (either Intel or TPV), integrated connectivity (CNVi).

**NOTE**

All CNVi 2230 SKUs can support a "Hybrid Key-E" routing with no jumpers. When considering a TPV module one should only use a Key-E module if the motherboard design is "Hybrid Key-E". A Key-A module will not fit into this scheme.

**Table 197. CNVi Module New Generation SKU**

<b>SKU</b>	<b>M.2 Type</b>	<b>Wi-Fi Channels</b>	<b>LTE Coex (On-module BAW Filter)</b>	<b>Comments</b>
JfP1 2230	2230	1x1	No	Basic 1x1
JfP1 2230 diversity	2230	1x1	No	Basic 1x1 with diversity
JfP1-SD	1216	1x1	No	Solder-down 1x1
JfP1-SD diversity	1216	1x1	No	Solder-down 1x1 with diversity
HrP1 2230	2230	1x1	No	.11ax 1x1
HrP1 SD Diversity	1216	1x1	No	.11ax Solder-down 1x1
HrP2 2230	2230	2x2	No	.11ax 2x2
HrP2 SD-1216	1216	2x2	No	.11ax Solder-down 2x2
HrP2 SD-1216 LTE	1216	2x2	Yes	.11ax Solder-down 2x2

**Table 198. Intel Discrete Previous Generation SKUs**

<b>SKU Name</b>	<b>M.2 Type</b>	<b>Wi-Fi Channels</b>	<b>LTE coex (On-module BAW Filter)</b>	<b>Comments</b>
ThP2 2230	2230	2x2	No	Basic 2x2 module
ThP2 2230 vPro	2230	2x2	No	vPro 2x2 module
CcP 2230	2230	2x2	No	.11ax 2x2 module
CcP SD-1216	1216	2x2	No	.11ax 2x2 module
CcP SD-1216 LTE	1216	2x2	Yes	.11ax 2x2 module

## 8.6.5 Signal Connection Pitfalls

The OEM should make sure to follow the M.2 definitions of signal names and directions (I/O, Tx/Rx, etc.) and avoid confusion between the platform side and device side.

---

### NOTE

Few lines are bidirectional, such as PCIe CLKREQ, PEWAKE.

---

## 8.6.6 Internal USB Port used in PCH

The CNVi IP that is embedded in the PCH uses an internal IOSF (PCIe like) bus for Wi-Fi and internal USB for BT.

The port used for this internal USB (for BT) can change between different PCH variants, as shown in below table.

---

**NOTE**

The ports are assigned zero-based numbers (example, the 10th port is #9).

---

**NOTE**

In CNVi flexible platform design, the OEM should consider to use the same USB port as the internal USB port assigned to CNVi Bluetooth\* device to Bluetooth\*/WLAN M.2 socket. That is, same USB port will be used for Bluetooth\* device of either CRF module or discrete module.

---

**Table 199. Example Internal USB Port Assignments in PCH**

PCH	USB Port Number (Zero-based) (When starting with "1", example, BIOS)
PCH-LP (ICPLP, TGPLP, CMPLP, CNPLP, ADPLP, MCC)	Port 9 (#10)
PCH-H (ICPH, TGPH, CMPH, CNPH, ADPH)	Port 13 (#14)
PCH-N (JPL)	Port 7 (#8)

*Note:* Can change between PCHs.

## 8.6.7 Pull-ups and Pull-downs

### Internal/Integrated PU/PD Settings

The OEM should consider the pull-ups and pull-downs on the CRF card, as described in below table.

**Table 200. Socket 1 Pull-ups and Pull-downs**

I/F	Signals	PU/PD in CNVr (CRF)	PU/PU in CNVi (SoC)	Comments
BRI/RGI (BT UART)	RGI_DT/ BRI_DT	PU (~120-150Kohm), RGI_DT shall be applied with 1K pull down during power-on Init	-	Shared with BT UART Expected power wasted while active with 100K <32uW at each pin RGI_DT is used by the platform to strap the presence of the CRF, as such it is a strong pull-down by the CRF (1K) as long as RF_RESET_B = 0
	RGI_RSP/ BRI_RSP	none	PU = 20Kohm This can be set by the BIOS after boot-up; needs to be enabled ONLY if CNVi is not used in the platform	BRI_RSP is used by the CNVi to strap the CRF type; i.e., when to apply PLL speed: when BRI_RSP = 0 – PLL at 1280M (JfP), when BRI_RSP =1 – PLL at 1320 (HrP and other future parts)
W_Disable* #	Wi-Fi/BT RF Kill	PU (~110-130Kohm)	-	

*continued...*

I/F	Signals	PU/PD in CNVr (CRF)	PU/PU in CNVi (SoC)	Comments
Slow CLK	SUSCLK (32kHz)	PD (~100Kohm)	-	If available on platform
Init Signals	RF_RESET_B	PD (~100Kohm)	-	Shared with PCM_SYNC
	CLKREQ0	PD (~200Kohm)	-	Shared with PCM_OUT

### Platform PU/PD Requirements

The OEM should apply pull-ups and pull-downs on the platform side according to below table.

**Table 201. Platform Pull-up and Pull-down Requirements**

I/F	Signals	PU/PD in Platform	Comments
BRI/RGI (BT UART)	RGI_DT	PU (20kohm)	This pull is required so that the SoC will be able to reliably detect that the CRF is present at power-up. However, it is possible to increase the resistor to 50K or even to 100K instead of 20K.
Init Signals	RF_RESET_B	PD (75Kohm)	It is highly encouraged to increase this resistor (or allow to switch it off when CNVi is active; not sure this is possible at the platform level). This resistor consumes power (43uW) all the time.
38.4 Ref Clock	RefCLK	PD (10kohm) (for JfP)	Only If used (e.g. Pulsar based platform, a platform-level decision); <b>not supported and not connected by HrP.</b>  Note: Although this signal is not connected from CRF side; there are platforms that use CNL like design and have those line in place - for those there is a recommendation from ESD team (no Wireless related logic on this) to keep the PD to avoid floating signals.
A4WP indication	A4WP_PRESNT	PD (75kohm)	Although not used, it is Recommended to not use this GPIO for other needs, to not toggle it, and to add a PD at the platform level to avoid a floating signal (with a non-deterministic value)

The OEM must avoid using a specific PU/PD when not needed or when required to not be used. Unless this rule is followed, a back-bias condition will result, where the IO is getting voltage before the device side is ready for it.

### 8.6.8 IO Connection Scenarios and Best Practices

The motherboard designer should address the following requirements for the sake of avoiding failsafe problems, reducing unneeded leakage and for following best practice design rules:

- Level-shifter back-bias prevention
  - Level shifter shall not set value in A side when not getting voltage in B side.
    - **Rationale:** Prevent back bias and wrong logic condition.
  - Level shifters shall be back-bias protected.

- **Rationale:** The level shifter is often supplied with a different supply than the IO connected to it. During ramp up/down states there might be back-bias scenario.

## 8.6.9 Connectivity Interface Specific Guidelines

### CNVio Signals

The CNVio signals connect between the RF companion module and the SoC. They are used as the main data bus for Wi-Fi, to transfer data between the CNVi and the RF companion chip. The CNVio signals are physically similar to those in the [MiPi DPHY](#) standard, but have a different (and Intel-proprietary) protocol.

Since the physical layer of the CNVio is similar to the MiPi DPHY standard, the user should follow the MiPi DPHY routing signal requirements. These are well documented in the MiPi DPHY standard specification. (Refer Chapter 7 of the MiPi DPHY standard: Interconnect and Lane Configuration.)

The CNVio bus is source-synchronous, and run at a clock rate of 1280 Mhz. Each lane has data carried over a differential pair, and each direction may have multiple lanes and a single clock driven by the source.

### Routing

The two traces of each lane must be routed together / same-length, as matched as possible (to reduce the signal propagation time difference). Moreover, since the CNVio uses one clock signal for multiple lanes in each direction, there should also be good delay matching between the two data lanes and the clock. There are no special delay matching requirements between lanes on opposite directions.

If needed, there is an option to add test points on those signals, but try to reduce such additional capacitance to a minimum. Refer the recommended parameters in below table.

**Table 202. CNVio DATA vs. CLK Imbalance Budget**

CNVIO Protocol	Platform End2End	Intel Platform with 2230			Intel Platform with 1216		
		M.2 Board	Platform Board	End2End	M.2 Board	Platform Board	End2End
		[mm]	[mm]	[mm]	[mm]	[mm]	[mm]
CNVio USB 3.2 Gen 1x1 (5 Gb/s) (JfP)	2.4	0.3	1	1.3	2	1	3
CNVio USB 3.2 Gen 2x1 (10 Gb/s) (HrP)	6.1	0.3	2	2.3	2	2	4.1

### RGI and BRI Signals

These are GPIO signals (1.8V) running between the SoC and the RF companion module. The BRI and RGI signals share the same traces as UART signals (for Discrete). Since the UART baud rate is expected to be lower than the BRI/RGI toggle rate, it can be assumed the BRI/RGI sets the requirements for this bus. BRI and RGI are two bi-directional buses. These signals have slew-rate controlled I/Os on both

ends (SoC and RF companion), which should be optimized to minimize EMI/RFI while maintaining good signal waveform. No special control impedance is needed. The BRI and RGI packets are protected by error correction coding and with standard routing and signal integrity practices applied, no errors are expected to be noticed on the buses.

- The directions of the signals are set by the CNVi/SoC/PCH side.
- RGI/BRI\_DT is the Tx side from the SoC to the CRF (so it is an Output signal on the SoC and Input signal on the CRF).
- RGI/BRI\_RSP is the Rx side at the SoC from the CRF (so it is an Input signal on the SoC and Output signal on the CRF).
- It is recommended to not use the GPIOs that are mapped to these signals for any Boot-Stepping function without considering the electrical behavior of this signal. (Refer Section 1).
- The RGI-BRI bus frequency is double the Crystal used on the CNVi side. So for current PCH cases, it uses a 38.4MHz Crystal so operates in the frequency of 76.8MHz.
- Notice that the RGI/BRI signals are GPIOs from the PCH, as so they can be impacted by BIOS settings to the GPIOs (e.g. impact the Rise-Fall time of the signals) see the Product EPS for mode details.

#### Wi-Fi/BT/LTE Coexistence Signals

Refer Chapter CNVio Bus for more details.

### 8.6.10

#### Connectivity Module Power Control

When designing the platform for CNVi, it is recommended to either not have this switch in the design, or to hard-wire it to be always-on by following the PCH (ON when the PCH is ON). This is because the operation of the RF companion module does not allow switching off its main power in any system state where the PCH is powered on, in order to maintain synchronization with the at all times.

Refer to “REF 2” for information on the correct usage of Load Switch (#[573970](#) – *Using a Load Switch for Intel CNVi Designs White Paper*).

---

#### NOTES

1. Power supply to the M.2 module is connected directly to the platform V3.3A rail without having any controlled power switch on the line. This ensures that the CNVi will be powered early in the platform power-up process as required by the CNVi power up sequencing. CNVi does not support wake-on-WLAN/BT during deep system sleep states (DSx). Connecting the CRF to 3.3V\_DSW rail is not specifically recommended; since the PCH rails needed for CNVi will be powered off in the deep-system-sleep state, getting out of DSx requires the CNVi, in the PCH, to Boot, Cold-Boot, in any case, so there is no real value in having the CRF on 3.3V\_DSW.
  2. CRF module was designed with low-leakage power, and so therefore does not require any external power control to be used during normal operation.
-

### 8.6.11 Wi-Fi Wireless Disable and RF-Kill

W\_DISABLE1# (pin 56 in M.2 2230 pinout, pin 28 in M.2 1216 SD pinout) serves as HW RF-Kill for the Wi-Fi radio. The pin is recommended to be left unconnected if, and only if, the HW RF-Kill signal is not required.

Asserting the W\_DISABLE#\_1 signal will result in a complete shutdown of the RF of the Wi-Fi part. The result from the user perspective is similar to that of disabling the Wi-Fi device from the laptop. Note that HW RF-Kill is part of the spec of the M.2 modules.

On some platforms this signal is also mapped as a PCH GPIO; if so, it is recommended to not use the GPIO that is mapped to this signal for any Boot-Stepping function without considering the electrical behavior of this signal.

### 8.6.12 M.2 Bluetooth® HW RF-Kill

W\_DISABLE2# (pin 54 in M.2 2230 pinout, pin 63 in M.2 1216 SD pinout) serves as HW RF-Kill for the Bluetooth® radio.

Asserting W\_DISABLE#\_2 signal will result in a complete shutdown of the Bluetooth® part. The result from the user perspective is similar to that of removing the Bluetooth® device from the platform.

It is recommended to not use the GPIO that is mapped to this signal for any Boot-Stepping function without considering the electrical behavior of this signal.

### 8.6.13 Power Supply De-coupling

It is required to have decoupling caps on the power feeds in each end of the connector.

- 10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V pins 2 and 4 (in 2230 modules) or pins 4 and 5 (in 1216 modules)
- 10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V pins 72 and 74 (in 2230 modules) or pin 72 and 73 (in 1216 modules)

### 8.6.14 A4WP Issues

Although A4WP is not supported in ICL/CML/TGL, and the dedicated signals between the PCH and the M.2 are not used, there are still platforms with this internal signal that gets into the PCH, and then to the CNVi IP , that indicates A4WP enablement. Apparently, this GPIO signal functionality was supposed to be fused, and disabled, but it was not. So, this signal might either be used by other means and/or be floating, and therefore sometimes get a value of "1," and thereby impact the BT in our module, keeping it ON.

For this we specifically recommend:

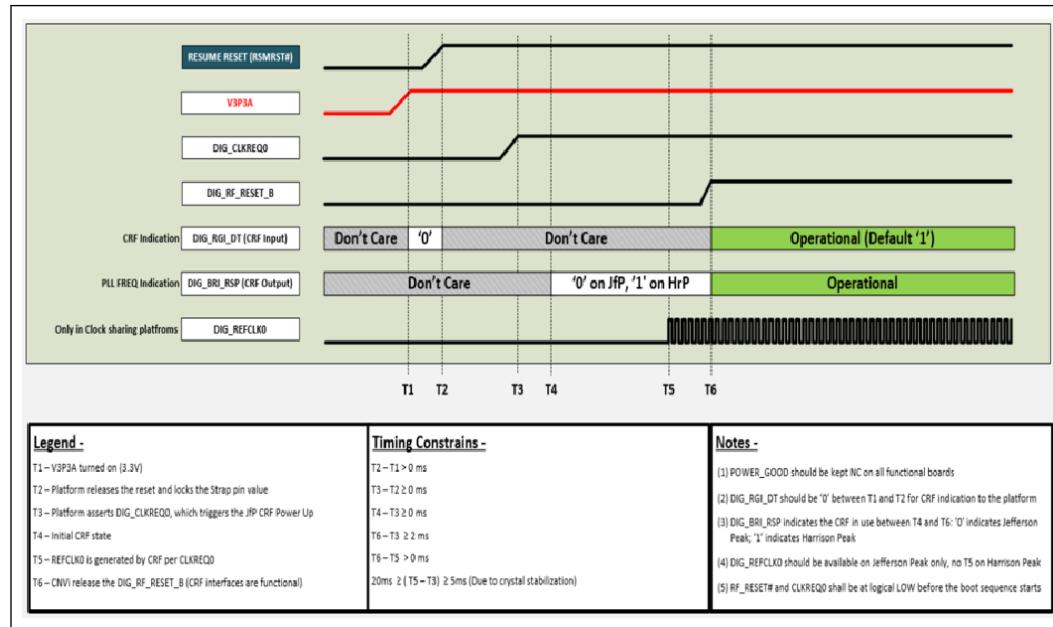
- Not to use this GPIO – assuming starting from TGL it will be removed from the Platform level.
- Add a PD on it at the Platform level for ICL- and CML-based platforms, and as needed in CNL/CFL.

## 8.6.15 BIOS

The CNVi modules (including Jefferson/Harrison Peak require specific BIOS support. A full description of BIOS support needed for platform can be found in the Connectivity BIOS Guide documents.

## 8.6.16 CNVi Power up Sequence

**Figure 203. CNVi Power up Sequence**



### NOTE

BRI\_RSP has a weak PU (CNVi side). When the 3P3A is up, it will get to "1", which means that T4 will be hard to identify (not really required). This also means that prior to T4 the "Don't care" period of the BRI\_RSP will be actually "1" - but still Don't care.

## 9.0 Power Integrity

### 9.1 Power Integrity Design Practice

This section describes the following:

- Capacitor Placement Consideration

#### 9.1.1 Capacitor Placement Consideration

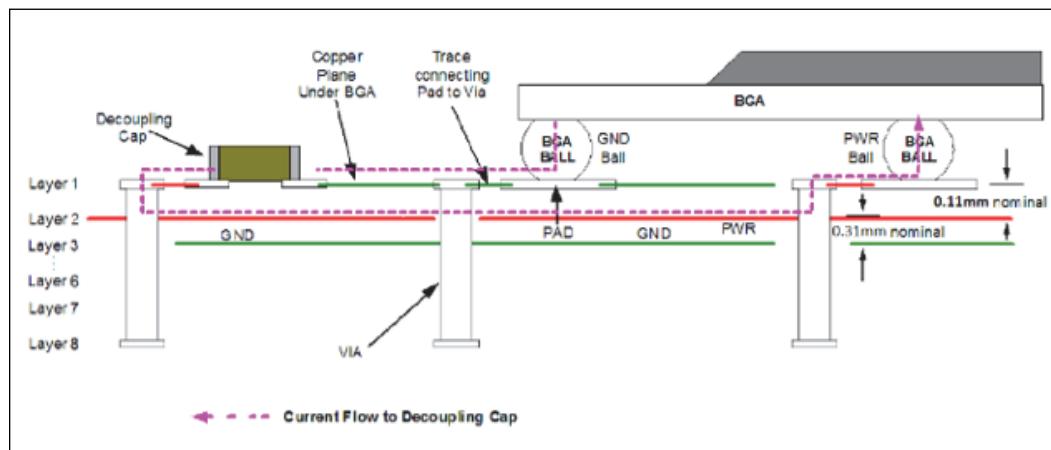
##### Loop Inductance Reduction Decoupling

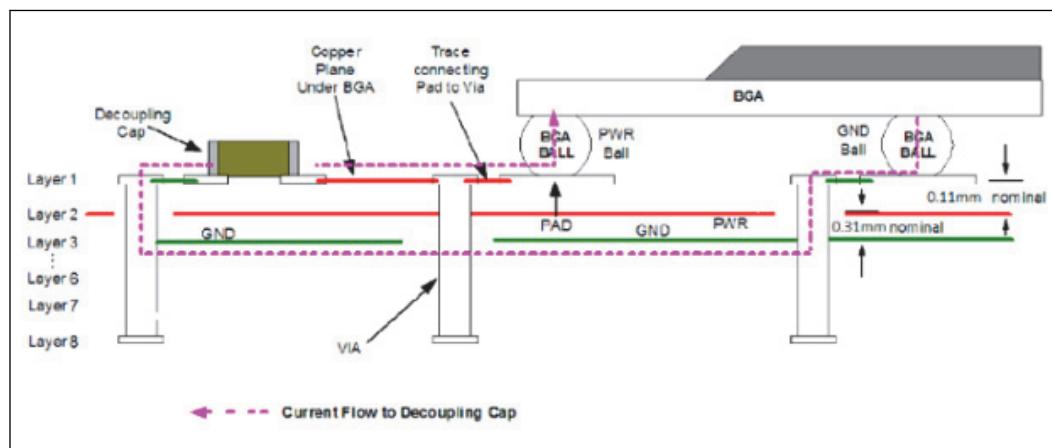
To reduce loop inductance and return path of for the decoupling capacitors, it is important to adhere to the (R)unway, and (E)dge decoupling capacitor placement recommendation mentioned below.

The idea is to rotate capacitors that set over power planes so that the loop inductance is minimized (refer the following figure). The basic theory for minimizing loop inductance is to consider which voltage is on layer two (power or ground) and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance.

The first figure below is an example of (R)unway decoupling capacitor placement, and the second figure is an example of (E)dge decoupling capacitor placement.

**Figure 204. Minimized Loop Inductance Example (R)unway**



**Figure 205. (E)dge Decoupling Capacitor Placement**

## 9.2 Tiger Lake UP3

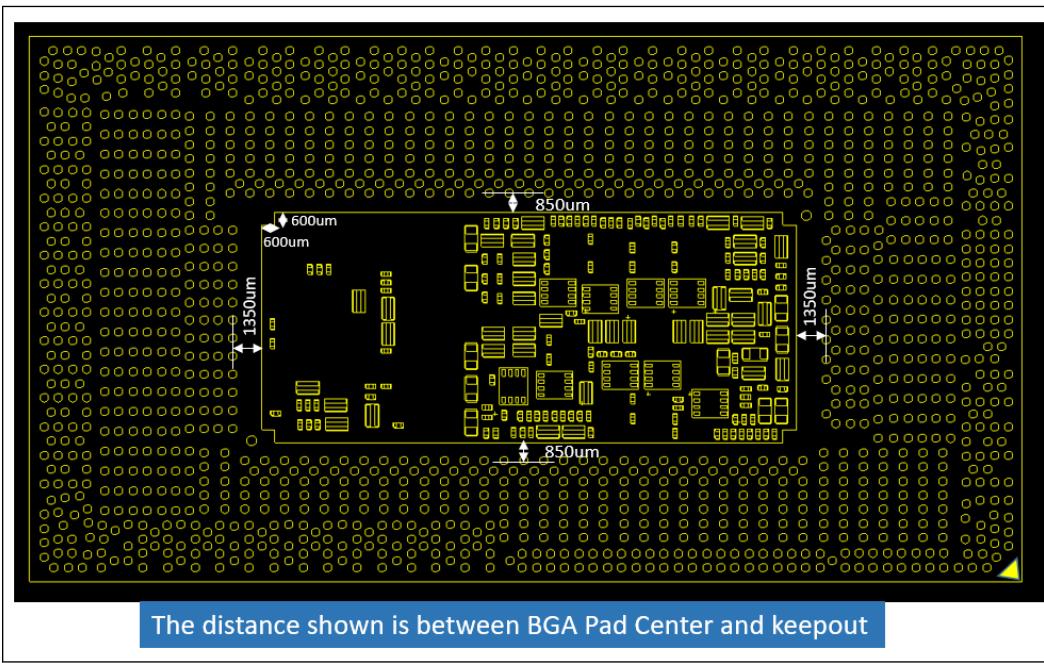
### General Design Consideration

In order to prevent manufacturing yield loss (open solder joint defects), the surface layer under the package cavity should be voided. This is to avoid package land side capacitors interacting with the board surface model inside package cavity area and ensure SMT yield.

To account for manufacturing process variations, the optimal design will maintain a distance of 150um from any PTH/via to the package landside capacitors (as measured from the via edge to LSC body outline) inside the cavity.

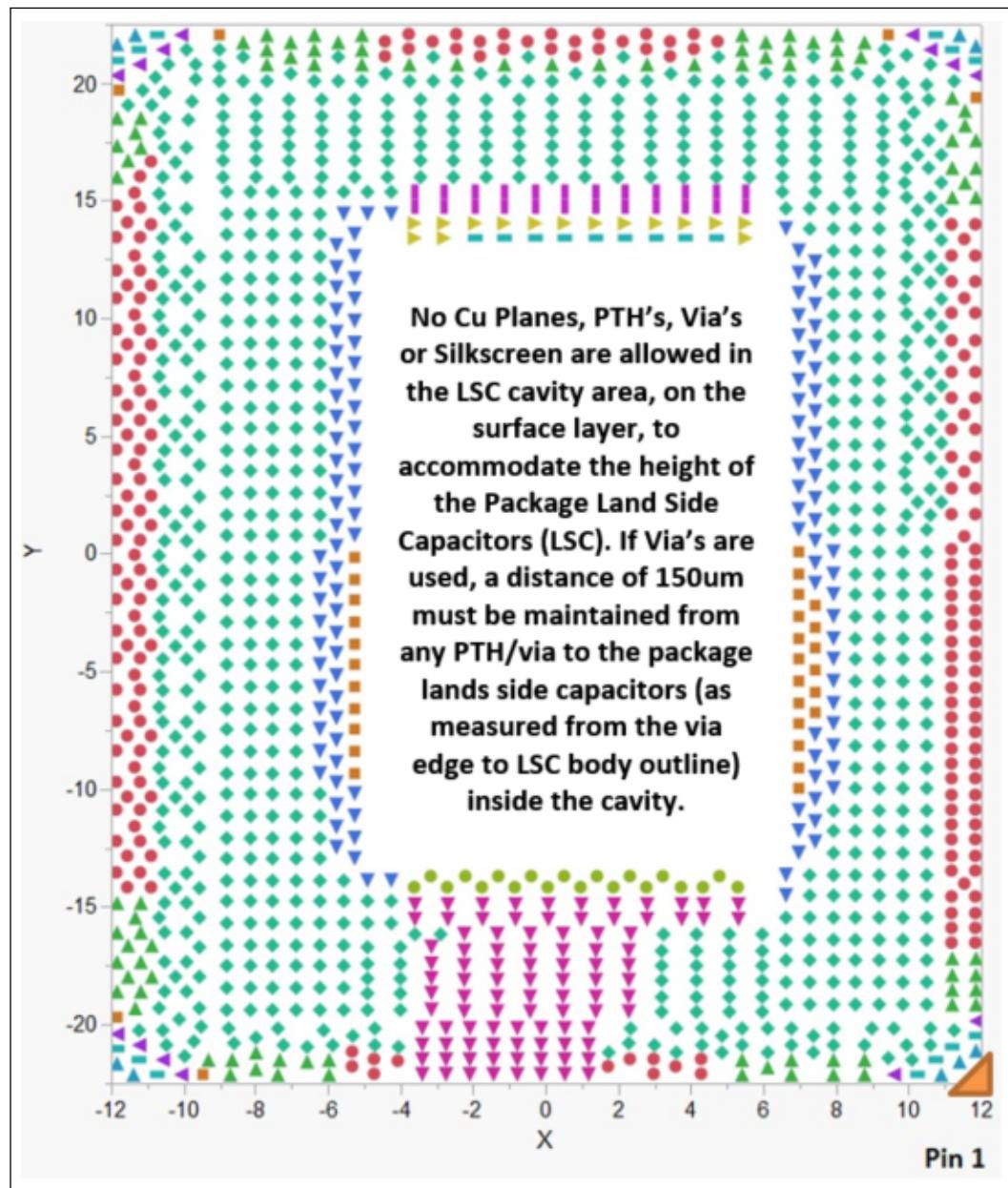
The copper shape and plane inside the cavity are required to be removed. Ideally, PTHs/vias and pads inside the cavity should be avoided. The cavity keepout zone recommendation is shown below.

In the case that PTHs/vias has to be placed inside the cavity area, it is recommended to place them strategically to avoid overlapping with package landside capacitors. Clp/dxf files for landside capacitor locations are also provided in the collateral # 608524 - "Tiger Lake Package Landside Capacitor dxf and clp files" which can be imported into the CAD tool to aid the design.

**Figure 206. Tiger Lake UP3 Package Cavity Keep Out Zone Recommendation****NOTE**

It is recommended not to place any metal features in the cavity keepout zone, including shape, PTHs, via, or pads. Package Landside capacitor may cause interference with these metal features.

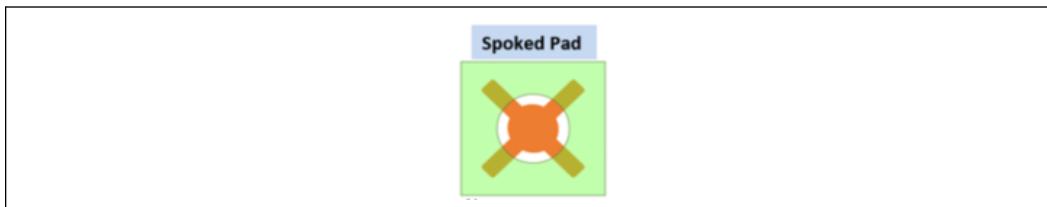
- **Land Pattern Recommendations**

**Figure 207. Tiger Lake UP3 Package Land Pattern Recommendation**

**Figure 208. Tiger Lake UP3 Package Land Pattern Pad Description**

Legend	Pad Size (microns/mils) ; SRO Size (microns/mils)	Function	# of Balls
●	MD or Spoked Pad Diameter: 200x300um, SRO 300x400um; SMD Pad Diameter: 300x400um, SRO: 200x300um	CTF	204
▲	MD or Spoked Pad Diameter: 250x350um, SRO 350x450um; SMD Pad Diameter: 350x450um, SRO: 250x350um	CTF	92
▼	MD or Spoked Pad Diameter: 300um, SRO 400um	CTF	118
■	MD or Spoked Pad Diameter: 300um, SRO 400um	NCTF	35
◆	MD or Spoked Pad Diameter: 300um, SRO 400um; SMD Pad Diameter: 400um, SRO: 300um	CTF	801
◀	MD or Spoked Pad Diameter: 300um, SRO 400um; SMD Pad Diameter: 400um, SRO: 300um	NCTF	14
▶	MD or Spoked Pad Diameter: 330um, SRO 430um;	CTF	15
■	MD or Spoked Pad Diameter: 330um, SRO 430um;	NCTF	22
■	MD or Spoked Pad Diameter: 330um, SRO 430um; SMD Pad Diameter: 430um, SRO: 330um	CTF	24
●	MD or Spoked Pad Diameter: 355um, SRO 455um	CTF	20
▲	MD or Spoked Pad Diameter: 355um, SRO 455um	NCTF	9
▼	MD or Spoked Pad Diameter: 355um, SRO 455um; SMD Pad Diameter: 455um, SRO: 355um	CTF	95

**Figure 209. Tiger Lake UP3 Package Land Pattern Spoked Pad Reference**



- Processor Decoupling and Layout Recommendations**

Follow processor decoupling capacitor requirements in the processor decoupling table to ensure component maintains stable supply voltage. The capacitors should be placed as close to the package as possible (2.54 mm nominal) in a location that would effectively decouple the interfaces listed under 'Domain'. All decoupling capacitors need to have at least X5R rating. Intel recommends including pads for extra power plane decoupling capacitors for prototype board designs.

- PCH Decoupling / Filter and Sense Point Recommendations**

Follow decoupling capacitor requirements in the PCH decoupling table to ensure component maintains stable supply voltage. The capacitors should be placed as close to the package as possible in a location that would effectively decouple the pins listed under 'Place capacitors near balls'. Also, all decoupling capacitors need

to have at least X5R rating. Pins listed under ‘PCH Pins sharing power rail’ are recommendations for pin group isolation and power plane routing. Intel recommends including pads for extra power plane decoupling capacitors for prototype board designs.

## 9.3 Tiger Lake UP4

### General Design Consideration

Follow processor and PCH decoupling capacitor requirements sorted based on power rail basis in the following sections to ensure component maintains stable supply voltage. The capacitors should be placed as close to the package as possible (2.54 mm nominal) in a location that would effectively decouple the interfaces listed under ‘Domain’. All decoupling capacitors need to have at least X5R rating. Intel recommends including pads for extra power plane decoupling capacitors for prototype board designs.

## 9.4 Impedance Spectrum Tool (IST/IFDIM) Testing Requirements and Recommendations

Impedance Spectrum Tool testing requirements and recommendations are shown below.

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#### NOTE

IST/IFDIM is not directly available to customers, Intel will need these trigger points to support debug of customer issues at Intel validation labs. Intel recommends customers implement the IST tool requirements from this section.

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**Table 203. IST (IFDIM) Testing Requirements and Recommendations**

Power Rail Sense Line	Feature	As Shown In	Required or Recommended	Notes
VCCIN	Trigger signals	Table and Figure below	Required	Route to un-stuffed header as shown in Figure below
	Differential Sense Nets	NA	Recommended	VCCIN_SENSE and VSSIN_SENSE VR lines we monitor for IFDIM/IST
	Current sense resistors	Figure below	Recommended	One sense resistor per phase. VR TT loadline data is required if sense resistors are not provided

*continued...*

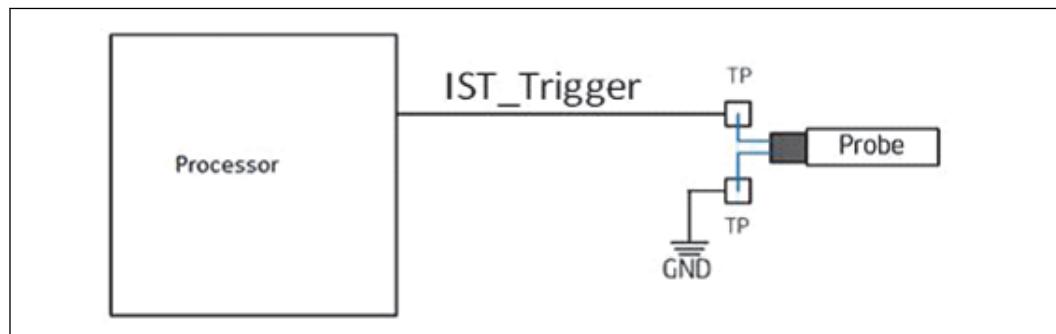
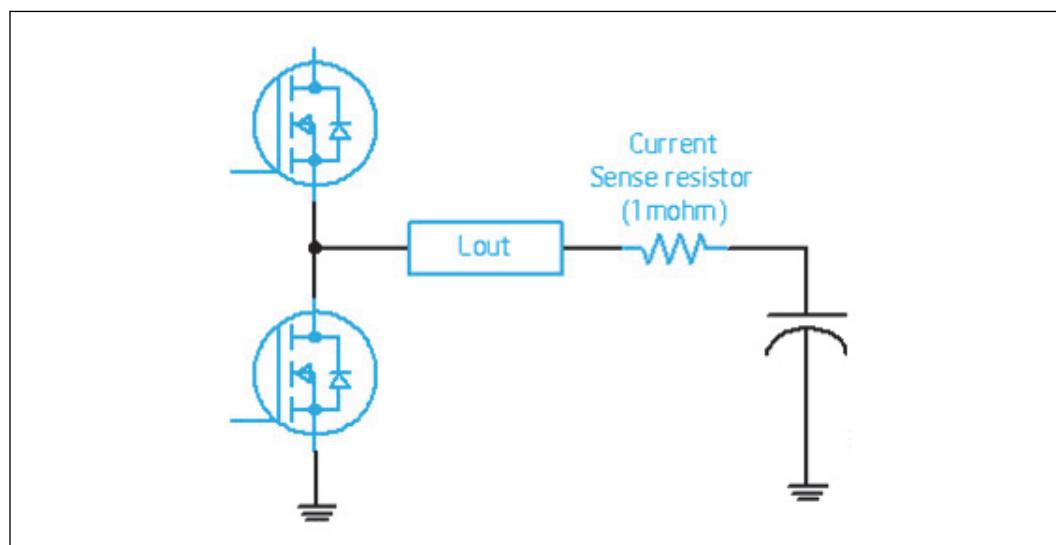
Power Rail Sense Line	Feature	As Shown In	Required or Recommended	Notes
VCCIN_AUX	Trigger signals	Table and Figure below	Required	Route to un-stuffed header as shown in Figure below
	Differential Sense Nets	NA	Recommended	VCCIN_AUX_VCCSENS E and VCCIN_AUX_VSSSENS E VR lines we monitor for IFDIM/IST
	Current sense resistors	Figure below	Recommended	One sense resistor per phase. VR TT loadline data is required if sense resistors are not provided

**NOTE**

ITP/XDP uses the same BPM#[0] line. Recommend using steering resistors for trigger signal.

**Table 204. Signals Required for IFDIM**

SKU	Feature	Required or Recommended	NET Name VIEW Pins	Ballout Pin #'s	
TGL UP3	IST/IFDIM Trigger	Required	BPM#[0]	Y2	
	CPU FIVR digital viewpins	Recommended	RSVD_TP	D2	
			RSVD_TP	C1	
	CPU FIVR analog viewpins	Recommended	IST_TP[0]	A4	
			IST_TP[1]]	A6	
	PCH FIVR analog viewpins	Optional	PCH_IST_TP[0]	DU53	
			PCH_IST_TP[1]	DT52	
TGL UP4	IST/IFDIM Trigger	Required	BPM#[0]	B33	
	CPU FIVR digital viewpins	Required	RSVD_TP	G23	
			RSVD_TP	E23	
	CPU FIVR analog viewpins	Recommended	IST_TP[0]	DA13	
			IST_TP[1]	CC11	
	PCH FIVR analog viewpins	Optional	PCH_IST_TP[0]	CL53	
			PCH_IST_TP[1]	CL51	
<b>Routing Recommendations</b>					
<ul style="list-style-type: none"> <li>ITP/XDP uses same MBPM[0] line. Recommend using 0 Ohm resistor in BPM#[0] net for access to trigger signal.</li> <li>50 Ohm routing is recommended for the following Single-ended analog signals: IST_TP[0], IST_TP[1], PCH_IST_TP[0], PCH_IST_TP[1].</li> <li>50 Ohm characteristic impedance differential routing is required for high frequency digital signals: RSVD_TP.</li> <li>Termination on board can be a regular Test Point or SMP connector.</li> </ul>					

**Figure 210. IST Trigger Point Implementation Requirement****Figure 211. Current Sense Resistor Recommendation**

## 10.0 Power Delivery

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This chapter provides guidelines for the Tiger Lake platform power delivery solution. The platform power delivery is comprised of an IMVP9 voltage regulator (VR), VCCIN\_AUX VR, Rest of Platform (ROP) VRs, load switches, battery charger, battery and fuel gauge, AC/DC adapter, power and current monitors, USB Type C power delivery and Power Sequencing.

- IMVP9 VR regulate power to the CPU processor and graphics FIVR. Details are provided in Section [IMVP9 and Processor Power Delivery Guidelines](#) .
- VccIN\_AUX VR regulate power to the PCH core FIVRs and also the processor system agent and Type C FIVRs. Details are provided in the Power Map Section [Power Maps and ROP Voltage Regulators](#)
- Rest of Platform (ROP) VRs regulate power to the PCH and rest of the system components. Discrete VRs or a PMIC can be used to supply ROP rails. Details are provided in the [Power Map Section Power Maps and ROP Voltage Regulators](#).
- Load Switches gate power to various SoC and ROP blocks to save power. Details are also provided in the Power Map Section [Power Map Tool](#).
- Battery Charger considerations are discussed in Section [Battery Charging System](#).
- Battery Fuel Gauge considerations are discussed in Section [System Peak Power Management \(Pmax\)](#).
- AC/DC Adapter considerations are discussed in Section [AC Adapter Considerations](#) .
- PSYS, the System Input Power Monitor is discussed in Section [Platform Power Monitoring And Control \(PSYS\)](#).
- USB Type C Power Delivery is covered in Section [USB Type C Power Delivery Considerations](#) .

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### NOTE

For the H35 processor line, please refer to UP3 4+2 electrical specifications

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## 10.1 Power Maps and ROP Voltage Regulators

This section describes the following:

- Power Map Tool
- New Power Rails in TGL (ROP Voltage Regulators in Tiger Lake)
- SoC Load Switches
- Trade-offs - Volume vs. Premium Power Maps

### 10.1.1 Power Map Tool

The Platform Power Map diagrams key specifications of the voltage regulators (IMVP9 and ROP VRs), load switches and the loads. To provide more flexibility in power design, power maps are now provided as a separate configurable tool. This tool is also where Default and Extreme power limits (PL2, PL4) are provided. Refer to Tiger Lake UP3/UP4 Platform Power Map Design Guide to generate a power map that accompanies this section.

---

#### NOTE

The processor and PCH EDS specification documents take precedence and will override any conflicts with what is being stated herein.

All cTDP configurations maintain the same power delivery specification as TDP

rest of platform

### 10.1.2 ROP Voltage Regulators in Tiger Lake

New Tiger Lake power rails consist of VCCIN\_AUX and two bypass rails (VCC\_VNNEXT\_1P05 and VCC\_V1P05EXT\_1P05)

#### VCCIN\_AUX

VCCIN\_AUX is a required rest of platform (ROP) power rail for Tiger Lake. It powers up non-core FIVRs in both the CPU and PCH. Differential package sensing is highly recommended for this rail. Differential package sensing is highly recommended for this rail.

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#### NOTE

Merging VCCIN\_AUX with V1.8A is not supported.

#### VID

Dynamic VID is used for this rail where the voltage can be set to the following values: 1.8V, 1.65V, and 0V. The Tiger Lake SoC PCH selects the required voltage via 2-pin VID signals. Both Tiger Lake UP3 and UP4 SKUs are required to support boot up voltage of 1.8V. The PCH will then control the VID pins to function at nominal voltages of 1.65V on TGL-UP3/P4 and 1.8V on TGL-UP3. During idle and power saving states, the voltage may be set to 0V.

---

#### NOTE

Use of VID gives power savings of 30mW and Sx and S0ix states.

To support this, the voltage regulator used must support dynamic changes in voltage set point while the regulator is running according to voltage and timing specifications in [Table 207](#) on page 381 and [Table 208](#) on page 382

Voltage regulators enabled to meet these requirements are detailed in [Rest of Platform \(ROP\) Component Enabling for TGL-UP3 and TGL-UP4](#) on page 387.

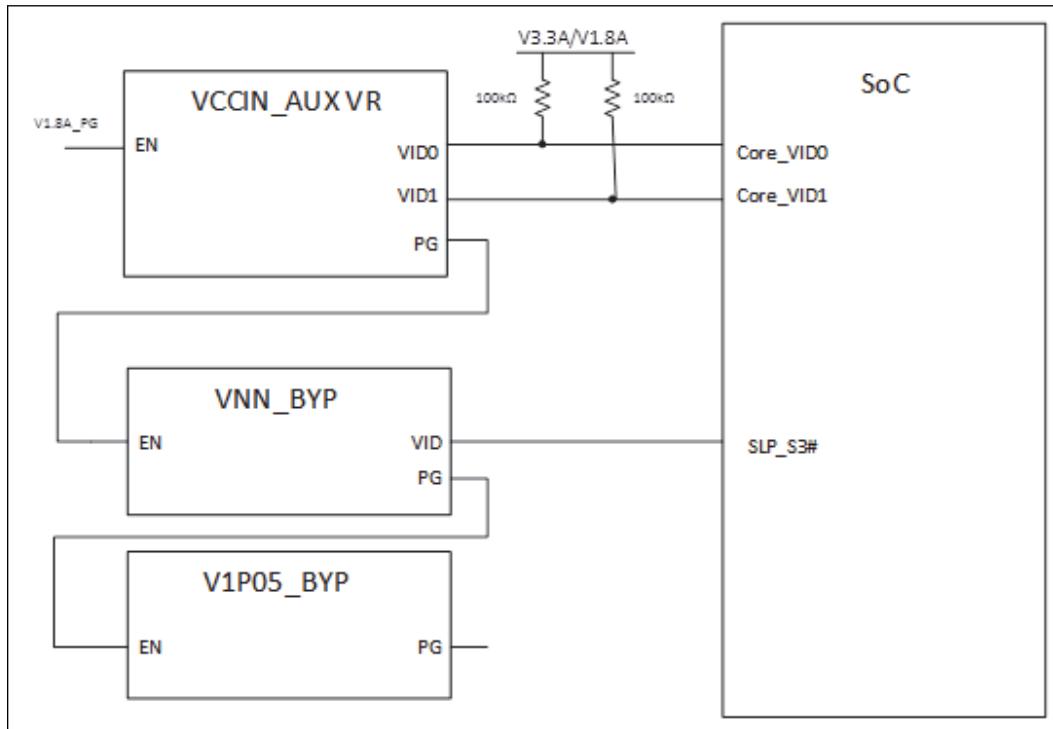
The below figure shows the block diagram of VID functionality. Depending on the GPIO voltage being used, the VID pins need to be pulled up to either V3P3A or V1P8A. Refer to GPIO strap settings.

**Table 205. VCCIN\_AUX VID**

VID[1] Pin State	VID[0] Pin State	VCCIN_AUX Voltage (V)	Usage
0	0	0	Power Saving State
0	1	1.1	Reserved
1	0	1.65	Full Current, TGL-UP4
1	1	1.8	Initial boot for TGL-UP3/UP4 Full current, TGL-UP3

**NOTE**

Logic “0” is 0V and Logic “1” is 1.8V based logic, but the VID pins must be 3.3 V tolerant as well.

**Figure 212. VCCIN\_AUX and BYP Rails Control Block Diagram**


By default PCH sets VCCIN\_AUX to run at 1.8V. In order to enable VID capability for power savings, the BIOS has to program the PCH to use the VID pins on the first transition to S0 out of G3/DSx. Details on the register configurations can be found in the BIOS Specification (#613495).

**Adjustable DC Load Line (Recommended)**

A voltage regulator with adjustable DC load line may be used to save on decoupling solution cost. If this functionality is supported, the regulator chosen must support a user configurable DC load line that ranges from  $0m\Omega$  to  $3.3m\Omega$ . The default DC load

line is  $0\text{m}\Omega$ . The specific implementation used is up to the user's direction as long as the voltage always stays within the tolerance specified in [Table 207](#) on page 381 and [Table 208](#) on page 382.

### **Load Line 3 (LL3) Impedance Guideline (Optional)**

Load Line 3 (LL3) refers to the power delivery network AC impedance peak at frequencies below 1MHz. The VCCIN\_AUX LL3 guideline is published in this document and is intended as a reference for voltage regulator design. It eases design and validation when the impedance can be obtained from simulation or measured on the actual board. The LL3 guideline numbers are specified along with other VCCIN\_AUX requirements in [Table 207](#) on page 381 and [Table 208](#) on page 382.

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#### **NOTE**

The LL3 guideline assumes that the voltage regulator bandwidth is below 1MHz. The load line is defined at sense point. If this guideline is met the voltage regulator is expected to perform within voltage tolerance specifications and meet performance requirements.

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It is important to also note that the voltage tolerance specified in [Table 207](#) on page 381 and [Table 208](#) on page 382 must still be met. The LL3 values specified here are only intended as guidelines. Refer Power Integrity and Customer PI (TBD) for more information about impedance guidelines.

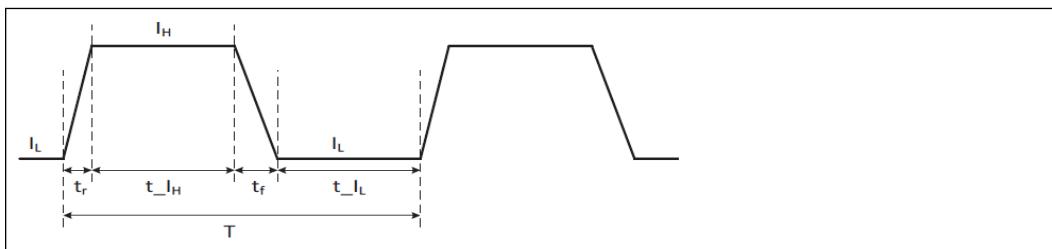
### **Decay Down (Optional)**

The decay down option helps to save power when there are frequent transitions from high to low voltage. It prevents power loss due to the frequent charge and discharge cycles of large output capacitors. When the VID changes to a lower set point, the regulator output stops switching and goes high impedance. The output naturally decays into the load; the regulator does not discharge the residual charge on the output decoupling. When VID changes to a higher value, the output voltage must still meet the ramp up time requirement and must ramp without discharging any residual discharge on the output decoupling.

### **VCCIN\_AUX Power Delivery Capacitors and Transient Requirements**

Power Integrity (PI) capacitor recommendations are itemized in the Power Integrity chapter. If those capacitors are close to the output inductor they are effectively shared with the voltage regulator (VR) and act as decoupling capacitors for transient response as well as being part of the output filter. Because of this, there is an opportunity to reduce cost by reducing the VR caps.

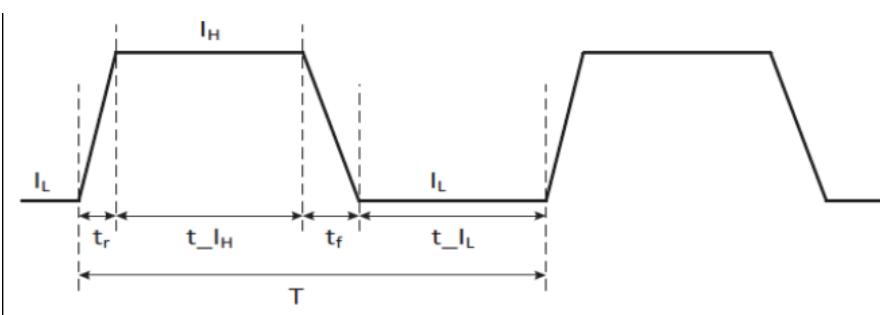
To test for transient performance the load current profile shown in Figure and Table below is used. The measured voltage must meet transient requirements specified in below Figure and Table .The test may be performed using a fast current load such as mini slammer or Voltage Regulator Test Tool (VRTT). The number of decoupling capacitors required for this rail may vary based on the board layout and VR solution chosen.

**Figure 213. Load Current Profile**

**Table 206. Transient Requirements**

Regulator	$I_L$ (mA)	$I_H$ (mA)	$t_r$ (ns)	$t_f$ (ns)	Frequency <sup>2</sup> (1/T)	Duty <sup>1</sup> (%)	Tolerance Spec (DC+AC at Sense point)
VCCIN_AU_X (TGL-UP3)	0	di' from <a href="#">Table 207</a> on page 381	'dt' from <a href="#">Table 207</a> on page 381	DC to 1MHz	50	Refer to <a href="#">Table 207</a> on page 381	
	'di' from <a href="#">Table 207</a> on page 381	'IccMax' from <a href="#">Table 207</a> on page 381					
VCCIN_AU_X (TGL-UP4)	0	di' from <a href="#">Table 208</a> on page 382	'dt' from <a href="#">Table 208</a> on page 382		50	Refer to <a href="#">Table 208</a> on page 382	
	'di' from <a href="#">Table 208</a> on page 382	'IccMax' from <a href="#">Table 208</a> on page 382					

**NOTES**

1. Duty =  $[(t_r + t_{I_H})/T]*100\%$
2. For cases where the transient load profile duty cycle and frequency are slew rate limited by  $t_r$  and  $t_f$ , the high time is set by  $t_r + t_f$ . The highest load frequency is set by  $1/(t_r + t_f)$ .
3. This is an electrical validation to test out corner conditions and is meant as a thermal test. If RMS current load exceeds the TDC of voltage regulator, additional cooling is allowed to prevent thermal issues.



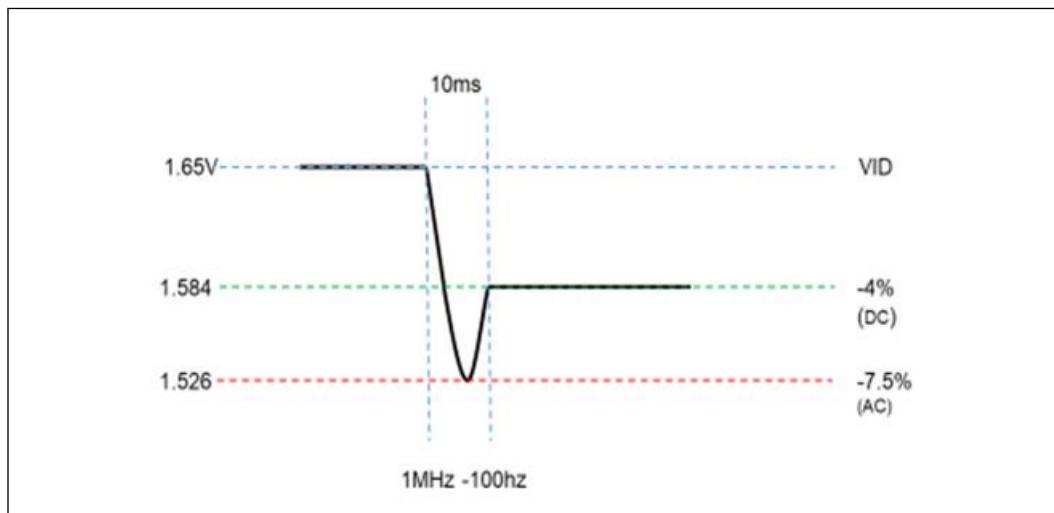
### VCCIN\_AUX Requirements

**Table 207. VCCIN\_AUX Parameters for UP3-Line 4+2 SKU**

Symbol	Description	Value		Notes
t <sub>RAMP_UP</sub>	Time from VID signal ( to higher voltage) to VCCIN_AUX voltage change complete	150µs		Maximum time allowed for VID ramp up
t <sub>RAMP_DOWN</sub> (slew)	Time from VID signal ( to lower voltage) to VCCIN_AUX voltage change complete	150µs		Maximum time allowed for VID ramp down when slewing down (Refer Note 1)
t <sub>RAMP_DOWN</sub> (decay)	Time from VID signal ( to lower voltage) to VCCIN_AUX voltage change complete	Not applicable		Maximum time allowed for VID ramp down for decay down
TDC	Thermal Design Current	Refer Tiger Lake UP3/UP4 Power Map		
I <sub>CCMAX</sub>	I <sub>CCMAX</sub> current	Refer Tiger Lake Processor External Design Specification (#575683)		
DCLL	DC Load Line	Refer Tiger Lake Processor External Design Specification (#575683)		
di	I <sub>CCMAX</sub> transient	70% of I <sub>CCMAX</sub>		Refer Note 2
dt	Duration for di step	250ns		Refer Note 2
V_TOB	Voltage Tolerance	High	+5% (1.8V), +5% (1.1V)	AC + DC + Ripple, DC to 1MHz
		Nominal	1.8V, 1.1V	
		Low	-10% (1.8V), -5% (1.1V)	
VCCIN_AUX_LL3	Load Line (LL3) impedance guideline (1MHz)	Refer to Tiger Lake Processor External Design Specification (#575683)		Refer Note 3 and 5
VOS	Max voltage overshoot	1.95 V		
TVOS	Max voltage overshoot duration	5 µsec		
T_UDS_MAX	Max voltage undershoot duration	200 µsec		
V_Undershoot	Voltage undershoot	15 mV		
ToVs_Max_app	Max app voltage overshoot duration	0 µsec		Refer Note 6
VoVs_Max_app	Max app voltage overshoot	0 mV		Refer Note 6
<p><i>Notes:</i></p> <ol style="list-style-type: none"> <li>Assumption is that the VR ramps up and down with the same slew rate</li> <li>For VR testing, the recommended initial current is 40% of I<sub>CCMAX</sub>.</li> <li>Refer Power Integrity for more information. Impedance at Sense can be validated on actual board or obtained through simulation using Customer PI Model</li> <li>This number may change in future revisions.</li> <li>DCLL targets are merely for FDIM testing guidance and are not specifically tested. Could be additional load up to PKG. Final test criteria are the voltage test specs in VRTT test plan.</li> <li>VRTT testing of this parameter is not required</li> </ol>				

**Table 208. VCCIN\_AUX Parameters for UP4-Line 4+2 SKU**

Symbol	Description	Value		Notes
t <sub>RAMP_UP</sub>	Time from VID signal ( to higher voltage) to VCCIN_AUX voltage change complete	150 $\mu$ s		Maximum time allowed for VID ramp up
t <sub>RAMP_DOWN</sub> (slew)	Time from VID signal ( to lower voltage) to VCCIN_AUX voltage change complete	150 $\mu$ s		Maximum time allowed for VID ramp down when slewing down (refer Note 1)
t <sub>RAMP_DOWN</sub> (decay)	Time from VID signal ( to lower voltage) to VCCIN_AUX voltage change complete	Not applicable		Maximum time allowed for VID ramp down for decay down
TDC	Thermal Design Current	Refer Tiger Lake UP3/UP4 Power Map IPDS		
I <sub>CCMAX</sub>	I <sub>CCMAX</sub> current 10ms max	Refer Tiger Lake Processor External Design Specification (#575683)		
di	I <sub>CCMAX</sub> transient	70% of I <sub>CCMAX</sub>		Refer Note 2
dt	Duration for di step	250ns		Refer Note 2
V_TOB	Voltage Tolerance	Low	-7.5% (1.65V AC), -4% (1.65V DC), +5% (1.1V)	AC + DC +Ripple, DC to 1MHz
		Nominal	1.65V, 1.1V	
		High	+7.5% (1.65V), +5% (1.1V)	
VCCIN_AUX_LL3	Load Line (LL3) impedance guideline (1MHz)	Refer to Tiger Lake Processor External Design Specification (#575683)		Refer Note 3 & 5
VOS	Max voltage during overshoot	1.89 V		
TVOS	Max voltage overshoot duration	10 $\mu$ sec		
T_UDS_MAX	Max voltage undershoot duration	200 $\mu$ sec		
V_Undershoot	Voltage undershoot	15 mV		
Tovs_Max_app	Max app voltage overshoot duration	0 $\mu$ sec		Refer Note 6
Vovs_Max_app	Max app voltage overshoot	0 mV		Refer Note 6
<p>Notes:</p> <ol style="list-style-type: none"> <li>Assumption is that the VR ramps up and down with the same slew rate</li> <li>For VR testing, the recommended initial current is 30% of I<sub>CCMAX</sub>.</li> <li>Refer Power Integrity for more information. Impedance at Sense can be validated on actual board or obtained through simulation using Customer PI Model .</li> <li>This number may change in future revisions.</li> <li>DCLL targets are merely for FDIM testing guidance and are not specifically tested. Could be additional load up to PKG. Final test criteria are the voltage test specs in VRTT test plan.</li> <li>VRTT testing of this parameter is not required</li> </ol>				

**Figure 214. Transient Tolerance for UP4**

#### Bypass Rails (Optional)

VCC\_VNNEXT\_1P05 (VNN\_BYP) and VCC\_V1P05EXT\_1P05 (V1P05\_BYP) are two dedicated voltage regulators that save platform power during low power states (Sx/S0ix).

Both VCC\_V1P05EXT\_1P05 and VCC\_VNNEXT\_1P05 are VIDed rails that operate at two voltage levels each. The VID control for this VR is the SLP\_S3#, V1P05\_CTRL, VNN\_CTRL (optional) signals.

These package pins are to be floated if they are not in use.

**Table 209. VCC\_VNNEXT\_1P05 VR Voltage Configurations**

SLP_S3# State	VNN_CTRL State (Optional)	Output Voltage (V)
0	N/A	1.05
1	0	0.78
1	1	0.70

**Table 210. VCC\_V1P056EXT\_1P05 VR Voltage Configurations**

V1P05_CTRL State	Output Voltage (V)
0	1.05
1	0.96

These voltage regulators need to meet stringent efficiency requirements while operating in low load condition. Efficiency must be met (from battery to Vout) with current in the range of 4mA to 50mA. Buck regulators are recommended for these rails. A 2S (7.4V nominal) battery configuration is recommended.

---

**NOTES**

1. The over voltage protection (OVP) trip level for the bypass rails must be within this range:  $1.155V \leq V_{ovp} \leq 1.365V$ . This is applicable for all VIDs (both 1.05V and 0.76V modes).
  2. Leakage from VCC\_VNNEXT\_1P05 power rail may back drive the external bypass VR when it is not in use, and its output may float up as high as 1.15 V. This is an expected behavior. Designers should make sure they select bypass VR with an OVP threshold that is above 1.15 V for all VNN\_BYPASS voltage settings to avoid false VR shutdown.
- 

**Table 211. Bypass Rails Efficiency Target**

Battery Nominal Voltage	Output Current Range	Efficiency (from Battery to Vout)
7.4V (2S)	4mA - 50mA	75%
11.1V (3S)		65%

---

**NOTE**

Failure to meet this efficiency requirement will result in diminished power savings or even higher power loss compared to not using these rails.

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**Table 212. VCC\_VNNEXT\_1P05 Parameters**

Symbol	Description	Value		Notes
t <sub>RAMP_UP</sub>	Time from VID signal ( to lower voltage) to VCCIN_AUX voltage change complete	200μs		Maximum time allowed for VID ramp up
I <sub>CCMAX</sub>	I <sub>CCMAX</sub> current 10ms max	Refer Tiger Lake External Design Specification (#575683)		
I <sub>CCstep</sub>	I <sub>CCstep</sub> for transient measurement	0 to 70% I <sub>CCMAX</sub> and 30% to 100% I <sub>CCMAX</sub>		
di/dt	I <sub>CCMAX</sub> slew rate for transient measurement	2.5A/μs		
VNN_BYP TOL	Voltage Tolerance, SLP_S3# = High)VID = 0.78V	Low	-40mV	Inclusive of AC +DC Ripple to 1MHz (Refer Note 1)
		Nominal	0.78V	
		High	+50mV	
	Voltage Tolerance, SLP_S3# = Low) VID = 1.05V	Low	-5%	
		Nominal	1.05V	
		High	+5%	
Note: This is measured at the SoC BGA location for VCC_VNNEXT_1P05 rail.				

**Table 213. VCC\_V1P05EXT\_1P05 Parameters**

Symbol	Description	Value		Notes
Icc <sub>MAX</sub>	Icc <sub>MAX</sub> current 10ms max	Refer Tiger Lake External Design Specification (#575683)		
Icc <sub>step</sub>	Icc <sub>step</sub> for transient measurement	0 to 70% Icc <sub>MAX</sub> and 30% to 100% Icc <sub>MAX</sub>		
di/dt	Icc <sub>MAX</sub> slew rate for transient measurement	2.5A/μs		
V1.05_BYP TOL	Voltage Tolerance, (V1.05_CTRL = High) VID = 0.96V	Low	-5%	Inclusive of AC +DC Ripple to 1MHz (Refer Note 1)
		Nominal	0.96V	
		High	+5%	

*Note:* 1. This is measured at the SoC BGA location for VCC\_V1P05EXT\_1P05 rail.

### 10.1.3 SoC Load Switches

For SoC power rails requiring load switches, platform designers will need to select a load switch with an appropriate resistance/R<sub>dson</sub> target to ensure that the voltage specifications at the SoC are met. As a general rule of thumb, the IR drop across the load switch should not exceed more than 1% of the voltage supply value under Iccmax conditions. Platform designers can adjust this target higher or lower to optimize the load switch selection for a specific motherboard design based on parameters such as the tolerance of the sourcing VR design, the resistance of the layout path from the VR to the load switch and finally to the CPU, VR sense location, etc.

#### Load Switch Ramp up Time Requirements

All load switches mentioned in this chapter are required to ramp within 65μs. Not meeting this requirement may result in system failure. Refer to [Power Sequencing Timing Diagrams Legacy Signals](#) on page 441 for more information.

#### VCCST Requirements

VCCST is a gated power rail derived from VCC1P05\_OUT\_FET.

The final enable signal for VCCST is logical OR of SLP\_S3# (or SLP\_S4#), VCCST\_OVRD, and debug port connector (optional for debug). Refer to [Power Sequencing Timing Diagrams Legacy Signals](#) on page 441 for more information.

#### VCCSTG and Discharge Requirements

VCCSTG is a gated power rail derived from VCC1P05\_OUT\_FET. The final enable signal for VCCSTG is logical OR of CPU\_C10\_GATE#, VCCST\_OVRD, and debug port connector (optional for debug). Refer to [Power Sequencing Timing Diagrams Legacy Signals](#) on page 441 for more information.

As long as VccST and VccSTG are power gated separately, the following requirements are critical to prevent system failure on Tiger Lake:

1. VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal R<sub>discharge</sub> <= 300 Ohms to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.

2. If VccST has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal  $R_{\text{discharge}} \leq VccST R_{\text{discharge}}$ .
3. The total capacitance on VccSTG  $\leq$  total capacitance on VccST

#### 10.1.4 Trade-offs - Volume vs. Premium Power Maps

Power maps are broken into two tiers: Volume and Premium. Volume focuses on cost savings with the fewest VRs and Premium focuses on the smallest solution size with the lowest power consumption. For a design focused on S0ix or Modern Standby\* power, the Premium power map is recommended. The designer may choose to implement a hybrid between Volume and Premium as long as guidelines are followed.

**Table 214. Differences between Power Maps**

Volume	Premium
VccSTG gated by SLP_S3#	VccSTG gated by {CPU_C10_GATE#}
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC_V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load
Various system devices share load switches	Various system devices have their own independent load switches
<i>Note:</i>	
1. VCC_VNNEXT_1P05 is also known as VNN BYP	
2. VCC_V1P05EXT_1P05 is also known as VP105 BYP	
3. Other changes may be present. Refer to the Power Map for details.	

From testing on TGL UP4, a 35mW impact has been observed from disabling external bypass in Connected Standby. Power increase is observed on the VCCIN\_Aux and VCCPRIM\_1P8 rails, with a decrease in power on the V1P05A\_Bypass rail. TGL UP3 will see similar impact. Power delta observed on customer platforms is likely lower compared to Intel RVPs due to typically lower quantity of capacitors on the board .

**Table 215. External Bypass Impact on Platform Power**

TGL UP3/UP4 KPI Power Rails	Power (W) CS w/ External Bypass	Power (W) CS w/o External Bypass
<b>VCCPRIM_3P3</b>	0.002	0.002
<b>VCCPRTC_3P3</b>	0.000	0.000
<b>VCCPDSW_3P3A</b>	0.003	0.003
<b>VCCPRIM_3P3_56</b>	0.001	0.001
<b>VCCPGPPR_3P3_1P8</b>	0.000	0.000
<b>VNN_BYPASS</b>	0.003	0.000
<b>VCCPRIM_1P8</b>	0.006	0.034
<b>VCCA_CLKLDO_1P8</b>	0.001	0.001
<b>VCCPRIM_1P8_18</b>	0.000	0.000
<b>V1P05A_BYPASS</b>	0.014	0.001
<b>VDD2_CPU</b>	0.001	0.001

*continued...*

<b>VCCIN_package_reference</b>	0.000	0.000
<b>VCCIN_AUX</b>	0.000	0.023
<b>SoC_total</b>	0.031	0.066

### NOTE

Power number deltas are assuming a 2S(7.4V nominal) battery configuration.

When using the external bypass VR in Config #1, the VR power loss of the external VR needs to be considered

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU\_C10\_GATE# is a signal from the Tiger Lake SoC that can be used for gating off VccSTG in the S0/C10 system state in order to save power.

To save power in S0 idle (for example Windows\* idle), it is recommended to power gate VccSTG in the S0/C10 state even in "Volume" designs. VccSTG should be gated by CPU\_C10\_GATE#.

Both Premium and Volume configurations can be used for systems that support the S0ix / Modern Standby state however power may be significantly higher in that state with the Volume configuration.

Platform/silicon debug functionality may require that some platform rails be powered up in states where they would normally be unpowered under a normal usage scenario. Platforms that require the ability to use this debug functionality must support powering the proper rails in the proper power states.

### Rest of Platform (ROP) Component Enabling for TGL-UP3 and TGL-UP4

Intel has worked together with various vendors to enable both discrete point of load (POL) voltage regulators as well as MOIC (Multi-output Integrated Circuit) that meet the new power delivery requirements in Tiger Lake.

MOIC is a simplified PMIC (Power Management Integrated Circuits) chip where multiple voltage regulators (VR) and power sequencing logic are integrated. The MOIC features adhere to the TGL platform voltage and timing requirements, voltage transient specifications, and power sequencing requirements. From Tiger Lake SoC perspective the MOIC behaves just like discrete VRs by default and requires no additional software enabling for it to work. The I2C interface is optional and helps in debug and tweaking if needed.

The enabled point of load (POL) VRs meet requirements for the new Tiger Lake power delivery rails, VCCIN\_AUX, VCC\_VNNEXT\_1P05 and VCC\_V1.05EXT\_1P05.

List of MOIC and POL vendors working with Intel for Tiger Lake will be updated in the Platform Component List (PCL) as they become available



## 10.2 IMVP9 and Processor Power Delivery Guidelines

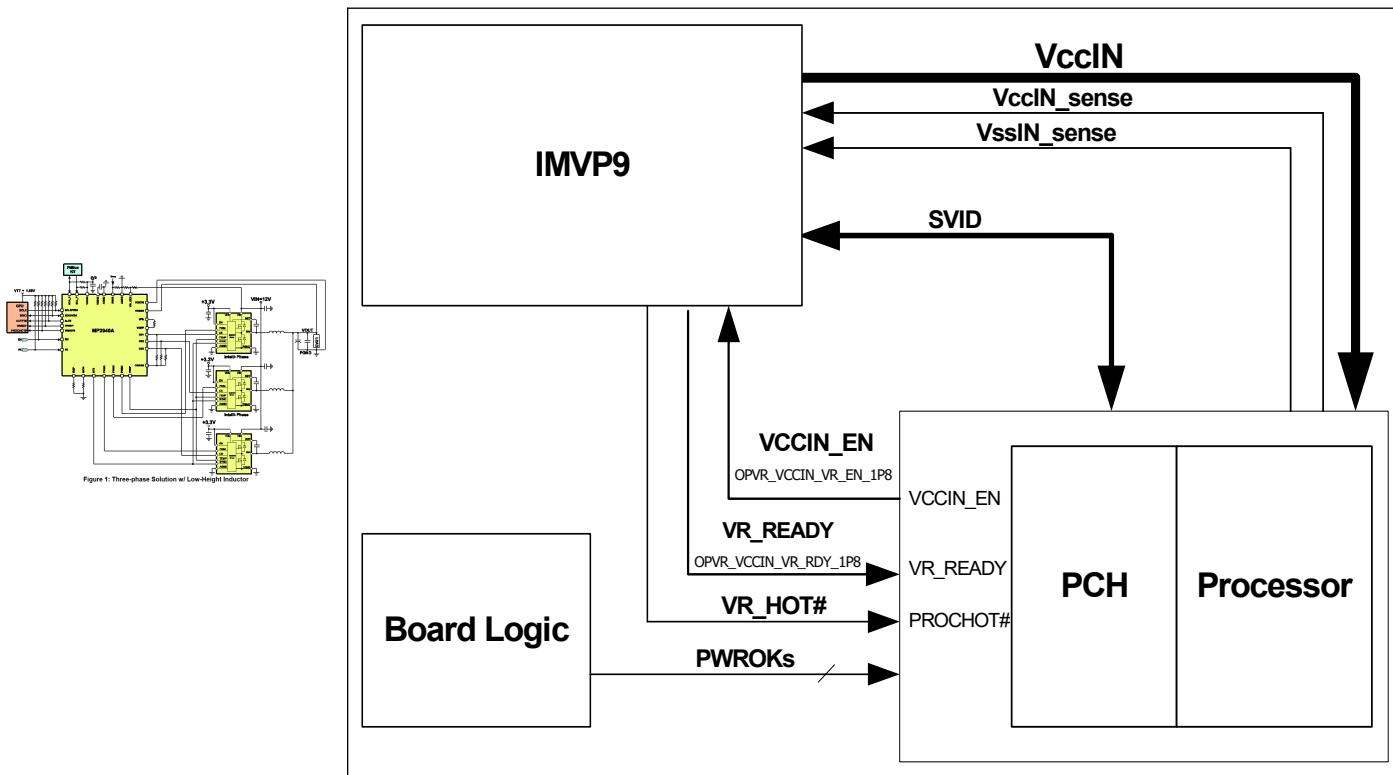
This section provides the general processor voltage rail design guidelines.

### 10.2.1 General Processor Power Delivery Considerations

An IMVP9 VR regulates power to the processor's main input rail, which internally supplies both core and graphics. The IMVP9 Pulse Width Modulation (PWM) Specifications define the DC-DC VR electrical requirements.

Figure below is only a generic representation of the IMVP9 VR. Other features and implementations are definitely possible.

**Figure 215. IMVP9 VR Block Diagram**



Important points to note in these block diagrams are:

- IMVP9 requires differential remote sensing. Differential sense inputs for a given rail must be the ONLY feedback point back to controller. Refer to [Table 216](#) on page 391 .
- VR\_Ready is a required controller output signal. It indicates that VR is operational. VR\_Ready signal is also used for appropriate power up sequencing during a platform boot.
- IMVP9 compliant controller is required to provide VR\_HOT# (VR Thermal Throttling) output signal to indicate operation close to regulator maximum thermal limit. **It is used by the system to prevent catastrophic thermal damage.**

- VCCIN\_EN (IMVP9) are required signals provided by platform logic. It enables the outputs of IMVP9 regulator.

VCCIN demotion is a new feature. Please refer to the VCCIN demotion TA #626886

## 10.2.2 Testing and Validation

The nominal processor voltage is determined by an SVID code provided to the VR. The VID nominal value indicates the reference point that the VID provides for the static and ripple voltage tolerance. Due to VR tolerances, PCB parasitic and current draw variations, the average voltage seen at the processor may be slightly higher or lower than the reference value according to the loadline spec or tolerances.

The VR must meet the static, ripple, and loadline tolerance limits for the entire range of processor load. Loadline, static and ripple tolerance window specifications must be met as measured differentially at Vcc\_SENSE/Vss\_SENSE pins.

Frequency Domain Impedance Measurement (FDIM) testing is also expected to be completed up to 1MHz on every IMVP9 power rail.

Refer to *Tiger Lake Platform Power Validation Plan* for guidance on validating power delivery and FDIM test requirements.

## 10.2.3 Audible Noise Reduction

In case of electrical noise issues, the appropriate Audible Noise Reduction option depends on the noise type. Solving acoustic noise is not:

- To avoid acoustic noise issues, during board design the BOM selection needs to be considered. There are design
- Noise mitigation is best done at the source

At least three conditions need to be simultaneously present for acoustic noise. They are periodic dv/dt in the audible range, sufficient dv magnitude, and insufficient damping, e.g. typical of a heavily-reliant or all-MLCC decoupling solution. The noise amplitude increases with current in  $I = C * dv / dt$ .

Ways to minimize the acoustic noise are:

- Control the in-rush current by sizing the output capacitor to just meet the transient requirement without excess
- Proper selection of inductors; taking core material, construction, mechanicals, and mounting into account to mitigate any potential inductor-induced “buzz” noise.
- Low-ESR MLCC's are notorious for potential audible noise, especially when exposed to large dv/dt events. This is due to the Piezo effect. The noise magnitude is proportional to the number of MLCC's used. Potential steps to take are:
  - Buck Regulator Input Filter. The highest peak-to-peak voltage/current stresses (dV/dt, dI/dt) of a Buck regulator are handled by the input filter caps
    - The input filter MLCC's should be (2) 4.7µF X5R per phase and 0402 or smaller size
    - Avoid Y5V dielectric MLCC's, as experience shows them more susceptible to the Piezo effect

- Physical placement is important, e.g. co-locate MLCC pairs either side of the input FET, not side-by-side
- Increase the capacitance to 10 $\mu$ F if needed to minimize the noise
- Where possible, large input bulk capacitors should be used 100  $\mu$ F or larger-to minimize the dv/dt events with polymer caps preferred.
- Buck Regulator Output Decoupling
  - For output high frequency decoupling, use 22 $\mu$ F or higher valued MLCC's to reduce the number of needed capacitors
  - Use polymer chip capacitors in conjunction with MLCC's, when possible
- Placing MLCC's symmetrically on the top- and bottom-sides of the motherboard introduces mechanically-opposed forces, helping mitigate any vibration, and reducing the noise magnitude

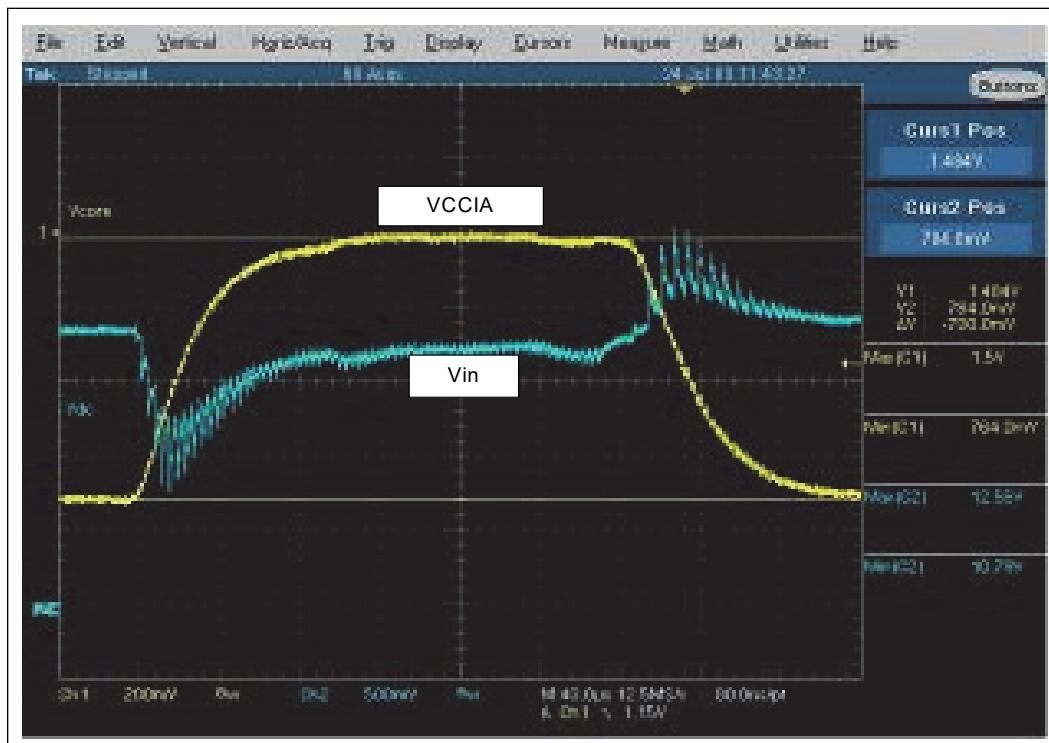
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**NOTE**

**For more acoustic noise solution kindly refer to Acoustic Noise Mitigation document CCL# 575216. Using Software solution to mitigate acoustic noise provided by the Technical advisory option may impact power and performance, interrupt response time, and device latency.**

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**Figure 216. Input Voltage Droop Caused by dv/dt Event at Output**



#### 10.2.4 Vcc\_SENSE/Vss\_SENSE Package Sensing

Motherboards are subject to layout area constraints that could significantly compromise a VR's placement on the motherboard and its connection to the processor pins. To ensure that the power delivery network's (PDN) impedance profile stays at/below the maximum loadline target for frequencies above the VR's Gain-Bandwidth (G-BW), the placement and connection of the decoupling capacitors as well the shapes of the power plane(s) is critical. At frequencies within the VR's G-BW control, the VR layout placement may be compensated using remote sensing of the voltage at the die through Vcc\_SENSE/Vss\_SENSE signals.

The processor implements the concept of "package sensing" for all IMVP9 voltage rails; the following examples use Vcc/Vss as general labels. Note: for optimal performance and noise rejection, the feedback signals for the IMVP9 controller should be routed as if they are a differential pair connecting the Vcc and Vss bumps of the processor to the IMVP9 controller Vcc\_SENSE and Vss\_SENSE pins respectively. This is true for non-IMVP9 rails too. This implementation extends the VR controller's regulation range, enclosing the motherboard parasitic within its feedback loop minimizing the impact on voltage regulation. The conceptual implementation of Vcc\_SENSE/Vss\_SENSE package sensing is illustrated in [Figure 217](#) on page 391 with recommendations in Table below.

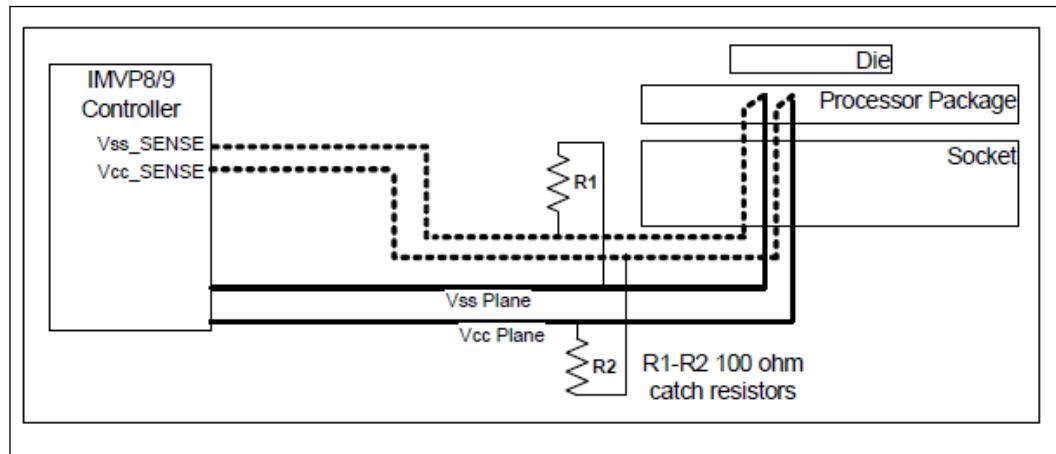
**Table 216. Package Sensing Recommendations**

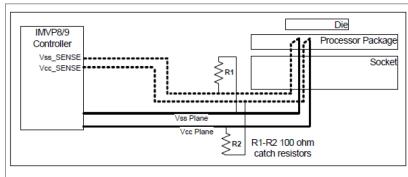
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VccIN_SENSE /VssIN_SENSE	100 ohm	50 ohm	<0.635 mm
<i>Note:</i> Does not apply when rails are merged.			

To minimize any stray noise pickup to the Vcc\_SENSE/ Vss\_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain 0.635 mm separation distance away from any other dynamic signals

**Figure 217. Example - Processor Vcc\_SENSE/Vss\_SENSE Package Sensing**





CPU/Processor?

- Figure above demonstrates the purpose/function of the feedback "catch" resistors. As discussed above package sensing effectively encloses the board parasitics within the feedback loop of the VR; however, a problem arises when the DUT is not present; the feedback loop is open and the VR does not have any feedback. Aberrant or unstable VR behavior may result, including overvoltage, errant/sporadic VR operation, etc. This may potentially damage motherboard components like the bulk decoupling capacitors. The "catch" resistors serve to close this feedback path, "bypassing" the Vcc\_SENSE/Vss\_SENSE connections through the processor and providing the necessary closed-loop feedback to the VR.
- Operation: The processor Vcc\_SENSE/Vss\_SENSE package traces are shunted to the motherboard Vccx and Vssx planes via the catch resistors R1 and R2. R1 and R2 are sized large in relation to the sense lines impedance so not to cause error when the DUT is present.
- Some additional guidelines:
  - R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc\_SENSE/Vss\_SENSE line resistance.
  - Preserve the transmission line integrity of Vcc\_SENSE/Vss\_SENSE lines by avoiding stub routing to R1, R2 catch resistors.

#### NOTE

For systems using a BGA packaged processor catch resistors are optional.

### 10.3 IMVP9 Voltage and Current Requirements

IMVP9 compliant VRs supply the required voltage and current to the processor's IMVP9 based voltage rails. The VID nominal value indicates the reference point for the static and ripple voltage tolerance.

Each IMVP9 VR output must meet the specifications in the processor EDS at remote sense processor pins.

Due to VR tolerances, PCB parasitic and current draw variations, the average voltage at the processor may be slightly higher or lower than the reference value. However, the VR must meet processor static and ripple tolerance limits over the entire range of processor load. The following conditions apply to the specifications:

- Applies to all frequencies unless specific frequencies are listed
- Applies to full temperature range
- I<sub>cc</sub> is measured at the nominal VID Vcc value under maximum signal loading conditions such as running a power virus program.
- Applies to full input power rail range
- The nominal VID voltage, voltage tolerance, and maximum current values are for reference only. Refer to the appropriate component documentation for the most current specifications.

An IMVP9 compliant VR must be designed to:

- Temporarily support IPL2 currents during a PL2 event for the respective tau duration their VR can thermally support
- Momentarily support the processor's maximum current (VR's electrical design constraint)

- Operate within spec under the worst-case dynamic/loaf transient events

#### NOTES

- Platform VRs should be thermally capable to support “IPL2” for ~10-20seconds. DTT or other mechanisms that raise PL1 will trend towards the longer 20 second duration estimate. The “PL1\_tau” is set to 28seconds by default. “IPL2” can be adjusted as needed using the “VR\_TDC” register in the BIOS.
- Refer Tiger Lake Processor External Design Specification, Volume 1 of 2 (#608190) for detailed processor specifications. Values shown in this document represent voltage plane design guidelines, not processor specifications

### 10.3.1 UP4-Line Requirement

**Table 217. VCCIN VR Parameters for UP4-Line 4+2 SKU**

Symbol	Description	Parameter Values by Product Segment		Notes
VID Range	V <sub>CCIN</sub> VID range issued across all operating modes	0 V- 2V		Design your board to handle the max VID plus ripple and tolerance in case of future specification change
VBoot	V <sub>CCIN</sub> VBoot setting	0 V		
VID1	Test VID for high freq mode	1.80 V		
VID2	Test VID in Low Freq Mode	1.60 V		To be used in Power Validation Plan for V <sub>CCIN</sub>
VID3	Test VID in PS3 state	1.20 V		
Icc PS1	Max Current in PS1 State	20A		
Icc PS2	Max Current in PS2 State	5A		Refer Notes 4-6. Transient loads not expected in PS3
Icc PS3	Max Current in PS3 State	1A		
Ripple	Ripple Tolerance	PS0	±15mV	
		PS1	±15mV	
		PS2	±30mV	
		PS3	±30mV	
V_TOB_Imin	Voltage Tolerance at Icc <sub>MIN</sub>	VID1	±13mV	
		VID2	±13mV	Refer Note 4
		VID3	±13mV	
V_TOB_Imax	Voltage Tolerance at Icc <sub>MAX</sub>	PS0	±20mV	
		PS1	±20mV	
		PS2	±35mV	
		PS3	±35mV	
Slew MAX	Maximum VR Slew Rate	For VID changes ≤ 50mV	200 mV/µs	

*continued...*

Symbol	Description	Parameter Values by Product Segment		Notes	
		For VID changes > 50mV	90 mV/μs		
R_DC_LL MAX	Loadline slope within the VR regulation loop capability 0-1kHz	$\leq 2.0\text{m}\Omega$ (mV/A)		Decoupling recommendations and associated VR bandwidth requirements are shown in Power Integrity chapter.	
R_AC_LL MAX	Loadline slope in response to dynamic load increase events 1kHz-1MHz	$4.7\text{m}\Omega$ (mV/A)			
TDC	Thermal Design Current	Refer to the TGL UP3/UP4 Power Map			
IccMAX	IccMAX current 10ms max	Refer to Tiger Lake Processor External Design Specification (575683)			
di	IccMAX transient	75% of IccMax		Refer Note 10	
dt	Duration for di step	150ns		Refer Note 8	
V_OVS MAX	Max Overshoot voltage	200mV		Refer Note 11	
T_OVS MAX	Max Overshoot time duration	500μs		Refer Note 11	
V_Undershoot	Max Undershoot Voltage	15mV		Refer Note 11	
T_UDS MAX	Max Undershoot time duration	200μs		Refer Note 11	
<p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. Refer to applicable processor Electrical Design Specification (EDS) for latest electrical parameters.</li> <li>2. Processors will spend more time operating at thermal design point. VR should be designed to efficiently deliver power at TDC and beyond.</li> <li>3. These are Intel default values and are used in the calculation of Min and Max LL slope tolerances in this table. Values obtained from the VR vendor based on the VR design may be used here as well, but they will change the calculation results. The user should be optimizing these thresholds to balance light load efficiency (impacting battery life) and performance.</li> <li>4. Icc_PS1, Icc_PS2 and Icc_PS3 cutoff thresholds should not be used as OCP values. Please refer to the Over-Current Protection (OCP) section in the IMVP specification for determining OCP threshold.</li> <li>5. Customers are strongly recommended to program the platform BIOS VR power state (PS) cutoff threshold settings to align with system IMVP VR power state and efficiency measurement results.</li> <li>6. For VR Power State Cutoff threshold tuning please refer to the following documentation package, CCL#608715</li> <li>7. Icc PS1 max current setting should not exceed the domain single phase current capability for TDC and IccMax.</li> <li>8. The time durations given here are for the VR design only.</li> <li>9. If using Psys, Intel recommends sizing the VR's thermal solution to support the domain's equivalent PL2 max TDC currents. By continually monitoring the platform's total power dissipation, Psys optimizes the AC adapter's PsysPL2 power capability, maximizing PL2 power delivered to the CPU (e.g. PL2 max operation) when rest-of-platform power headroom exists allows. PsysPL2 is the sum of the PL2 and ROP as measured at the power input. As ROP is reduced PL2 may increase, PsysPL2 remaining constant.</li> <li>10. For VR design testing, the recommended initial current is 25% of IccMax.</li> <li>11. IMAXAPP testing is not needed on TGL</li> <li>12. AUX FDIM is optional. APLL and DPLL are only for FDIM reference and not tested in time domain</li> </ol>					

### 10.3.2 UP3 Line Requirement

**Table 218. Processor VR Parameters for UP3-Line 4+2 SKU**

Symbol	Description	Parameter Values by Product Segment	Notes
VID Range	V <sub>CCIN</sub> VID range issued across all operating modes	0 V- 2V	Design your board to handle the max VID plus ripple and tolerance in case of future specification change
VBoot	V <sub>CCIN</sub> VBoot setting	0 V	

*continued...*

Symbol	Description	Parameter Values by Product Segment		Notes		
VID1	Test VID for high freq mode	1.80 V	1.60 V	To be used in Power Validation Plan for V <sub>CCIN</sub>		
VID2	Test VID in Low Freq Mode					
VID3	Test VID in PS3 state					
Icc PS1	Max Current in PS1 State	20A		Refer Notes 4-6. Transient loads not expected in PS3		
Icc PS2	Max Current in PS2 State	5A				
Icc PS3	Max Current in PS3 State	1A				
Ripple	Ripple Tolerance	PS0	±15mV			
		PS1	±15mV			
		PS2	±30mV			
		PS3	±30mV			
V_TOB_Imin	Voltage Tolerance at Icc <sub>MIN</sub>	VID1	±13mV	Refer Note 4		
		VID2	±13mV			
		VID3	±13mV			
V_TOB_Imax	Voltage Tolerance at Icc <sub>MAX</sub>	PS0	±20mV			
		PS1	±20mV			
		PS2	±35mV			
		PS3	±35mV			
Slew MAX	Maximum VR Slew Rate	For VID changes ≤ 50mV	200 mV/µs			
		For VID changes > 50mV	90 mV/µs			
R_DC_LL MAX	Loadline slope within the VR regulation loop capability 0-1kHz	≤2.0mΩ (mV/A)		Decoupling recommendations and associated VR bandwidth requirements are shown in Power Integrity chapter.		
R_AC_LL MAX	Loadline slope in response to dynamic load increase events 1kHz-1MHz	4.4mΩ (mV/A)				
TDC	Thermal Design Current	Refer to the TGL UP3/UP4 Power Map				
Icc <sub>MAX</sub>	ICC <sub>MAX</sub> current 10ms max	Refer to Tiger Lake Processor External Design Specification (608190)				
di	ICC <sub>MAX</sub> transient	75% of IccMax		Refer Note 10		
dt	Duration for di step	139ns		Refer Note 8		
V_OVS MAX	Max Overshoot voltage	200mV		Refer Note 11		
T_OVS MAX	Max Overshoot time duration	500µs		Refer Note 11		

*continued...*

Symbol	Description	Parameter Values by Product Segment	Notes
V_Undershoot	Max Undershoot Voltage	15mV	Refer Note 11
T_UDS MAX	Max Undershoot time duration	200µs	Refer Note 11

**Notes:**

1. Refer to applicable processor Electrical Design Specification (EDS) for latest electrical parameters.
2. Processors will spend more time operating at thermal design point. VR should be designed to efficiently deliver power at TDC and beyond.
3. These are Intel default values and are used in the calculation of Min and Max LL slope tolerances in this table. Values obtained from the VR vendor based on the VR design may be used here as well, but they will change the calculation results. The user should be optimizing these thresholds to balance light load efficiency (impacting battery life) and performance.
4. Icc\_PS1, Icc\_PS2 and Icc\_PS3 cutoff thresholds should not be used as OCP values. Please refer to the Over-Current Protection (OCP) section in the IMVP specification for determining OCP threshold.
5. Customers are strongly recommended to program the platform BIOS VR power state (PS) cutoff threshold settings to align with system IMVP VR power state and efficiency measurement results.
6. For VR Power State Cutoff threshold tuning please refer to the following documentation package, (#608715).
7. Icc PS1 max current setting should not exceed the domain single phase current capability for TDC and IccMax.
8. The time durations given here are for the VR design only.
9. If using Psys, Intel recommends sizing the VR's thermal solution to support the domain's equivalent PL2 max TDC currents. By continually monitoring the platforms total power dissipation, Psys optimizes the AC adapter's PsysPL2 power capability, maximizing PL2 power delivered to the CPU (e.g. PL2 max operation) when rest-of-platform power headroom exists allows. PsysPL2 is the sum of the PL2 and ROP as measured at the power input. As ROP is reduced PL2 may increase, PsysPL2 remaining constant.
10. For VR design testing, the recommended initial current is 25% of IccMax.
11. IMAXAPP testing is not needed on TGL
12. AUX FDIM is optional. APLL and DPLL are only for FDIM reference and not tested in time domain

## 10.4 AC Adapter Considerations

To support Turbo performance as well as to provide more flexibility on the size and cost of the AC adapter, this section will cover the important aspects of adapter requirements and trade-offs including thermal power considerations.

### 10.4.1 Power Budgeting for AC Adapter

The adapter power rating is divided into the sustained power level and transient power level. The sustained power level is the maximum constant power that the adapter can supply to system. The transient power level is the maximum peak power that the adapter can supply within a given duration of time, usually in milliseconds.

The adapter power rating has to meet the power demand of system, which can be divided into SoC power and rest-of-platform (ROP) power. For the system with Turbo, the sustained SoC power is PL2 and the peak SoC power is PL4.

Default and Extreme Power Limits (PL2, PL4) are now provided in the TGL Platform Power Map Design Guide.

The ROP power is determined by the components other than SoC. The number of USB ports, the display module, the memory module, etc., significantly impact on the ROP power level. As described in the P<sub>SYS</sub> in [Platform Power Monitoring And Control \(Psys\)](#) on page 411 feature can monitor the ROP power in real-time. If P<sub>SYS</sub> is not available, the designer has to estimate the typical ROP power level (P<sub>ROP\_typ</sub>) and the worst case maximum ROP power level (P<sub>ROP\_max</sub>) in order to size the adapter.

## 10.4.2 Transient Power Requirement for Turbo

The selection of charger PD architecture is going to affect the transient power requirements on the AC adapter in order to adequately support Turbo operation. The duration of transient power level depends on how long the battery takes to start providing power.

## 10.4.3 Sustained Power Requirement at Dead Battery Level

For the system with either Hybrid Power Boost (HPB) or NVDC charger, the sustained power requirement of the adapter can be estimated based on the scenario of a dead battery when the battery doesn't have enough charge to power the system and the AC adapter has to provide all the power. Intel recommends the Dynamic Battery Power Technology (DBPT) to better determine the battery power capability in real-time. Refer Section [System Peak Power Management \(Pmax\)](#) on page 417 on battery and fuel gauge system for details.

$P_{sys}$ , the platform power monitoring and control feature on Tiger Lake can be used to maintain a desired  $P_{sysPL2}$  level where the overly conservative estimation of ROP power can be reduced. Instead of using the worst case maximum ROP power level to estimate the sustained power level for AC adapter, the pre-defined  $P_{sysPL2}$  can be used.

**Table 219. Sustained and Transient Power Levels with different PD Architectures**

Charger Type	Adapter Supplemented by Battery	Sustained Power Level with Dead Battery	Transient Power Level	Transient Power Level with Dead Battery Level
Traditional	No	Without $P_{sys}$ : PL2 + $P_{ROP\_max}$ With $P_{sys}$ : $P_{sysPL2}$	Up to 10ms: PL4+ $P_{ROP\_max}$	Up to 10ms: PL4+ $P_{ROP\_max}$
Hybrid Power Boost (HPB)	Yes		Up to 1.5ms: PL4+ $P_{ROP\_max}$	
NVDC	Yes		Same as sustained power level	

---

### NOTE

The above power loading levels have to be divided by the conversion efficiency to get the final adapter output power levels. The  $P_{sysPL}$  and PL values need to be updated regularly as the power capability of adapter and battery changes. In Tiger Lake Platform Turbo and Thermal Power Management Guide for Intel® Core™ Based Processors User Guide (#607378), the flow chart and equations are provided to calculate  $P_{sysPL}$  and PL values based on adapter power capability and battery power capability (DBPT) for 4 design options; NVDC with  $P_{sys}$ , NVDC without  $P_{sys}$ , HPB with  $P_{sys}$ , and HPB without  $P_{sys}$ .

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## 10.4.4 TCSS Power Adders Guidance

This section provides Power Adders Guidance for Integrated TCSS not reflected in the processor baseline workload. Power Adders are sustained thermal power for non-IA IP on the device. Power Adders may be negligible or significant and impact the overall thermal budget for the processor. The recommended SoC PL1 power targets for the scenarios provided below reflect adjustments to the baseline power required to preserve base frequency associated to the sustained long-term thermal capability. The

system designer should consider the power impact of different I/O connections on the processor and platform when determining the thermal budget and associated cooling solution to preserve user experiences or performance. The scenarios shown in table below represents sustained workload situations. Processor cTDP down will still maintain SoC performance without undesired behavior from these Power Adders. In the case of bursty workloads, the impact on processor performance may be negligible and the adders provided may not be needed to be factored into the design.

**Table 220. TGL-UP3 TCSS Scenarios with Integrated Thunderbolt**

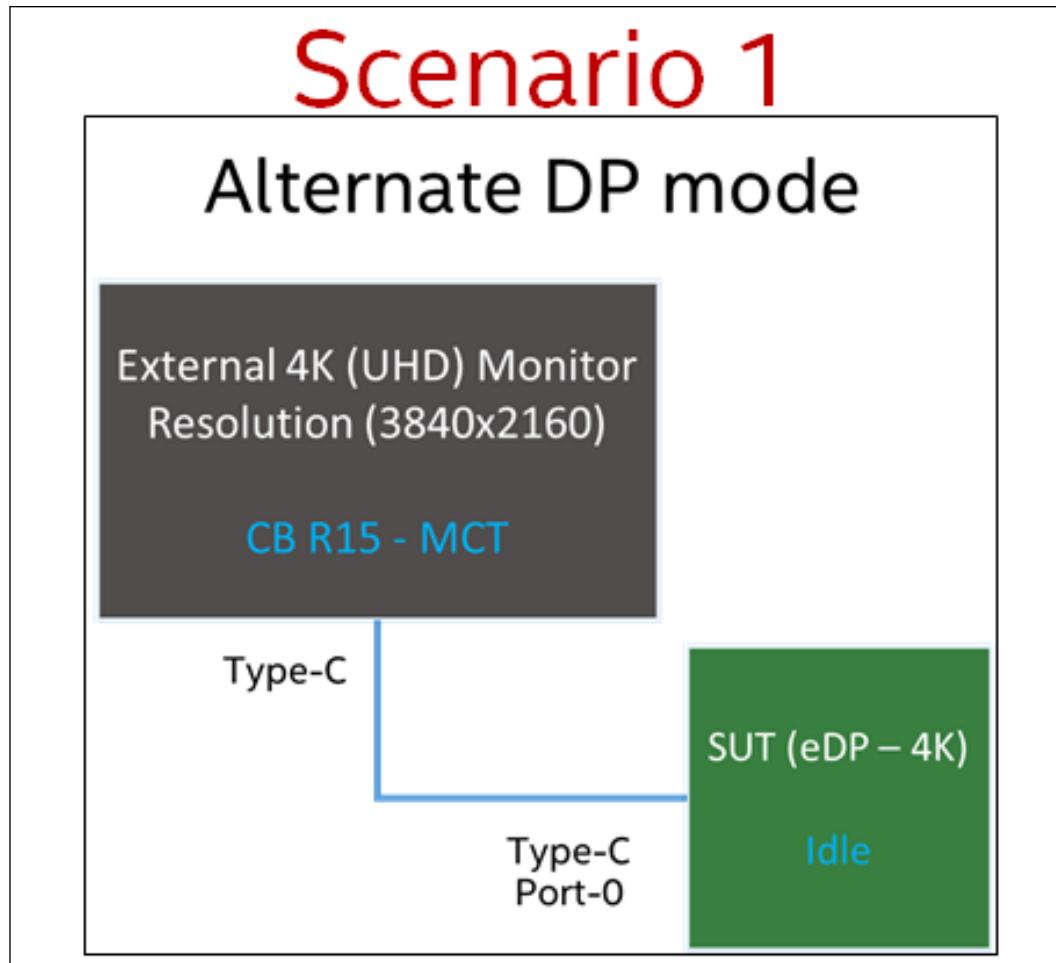
TCSS Scenario	Description	TGL-UP3 TCSS Power Adder (W)	TGL-UP3 SoC Power Target (W)
Baseline	TC-Cold NDA, (Internal Display ( eDP ), 4K resolution (3840x2160)	0	15
DP Alternate Mode	1x4K at 60Hz external display, extended mode	0.8	15.8
Thunderbolt DP Mode	1x4K at 60Hz external display, extended mode	1.0	16
Thunderbolt dual DP Mode	2x4K at 60Hz external display, extended mode	1.9	16.9
Thunderbolt DP Mode, Max IO	1x4K at 60Hz external display, IO power scaled to max to simulate full BW	1.6	16.6

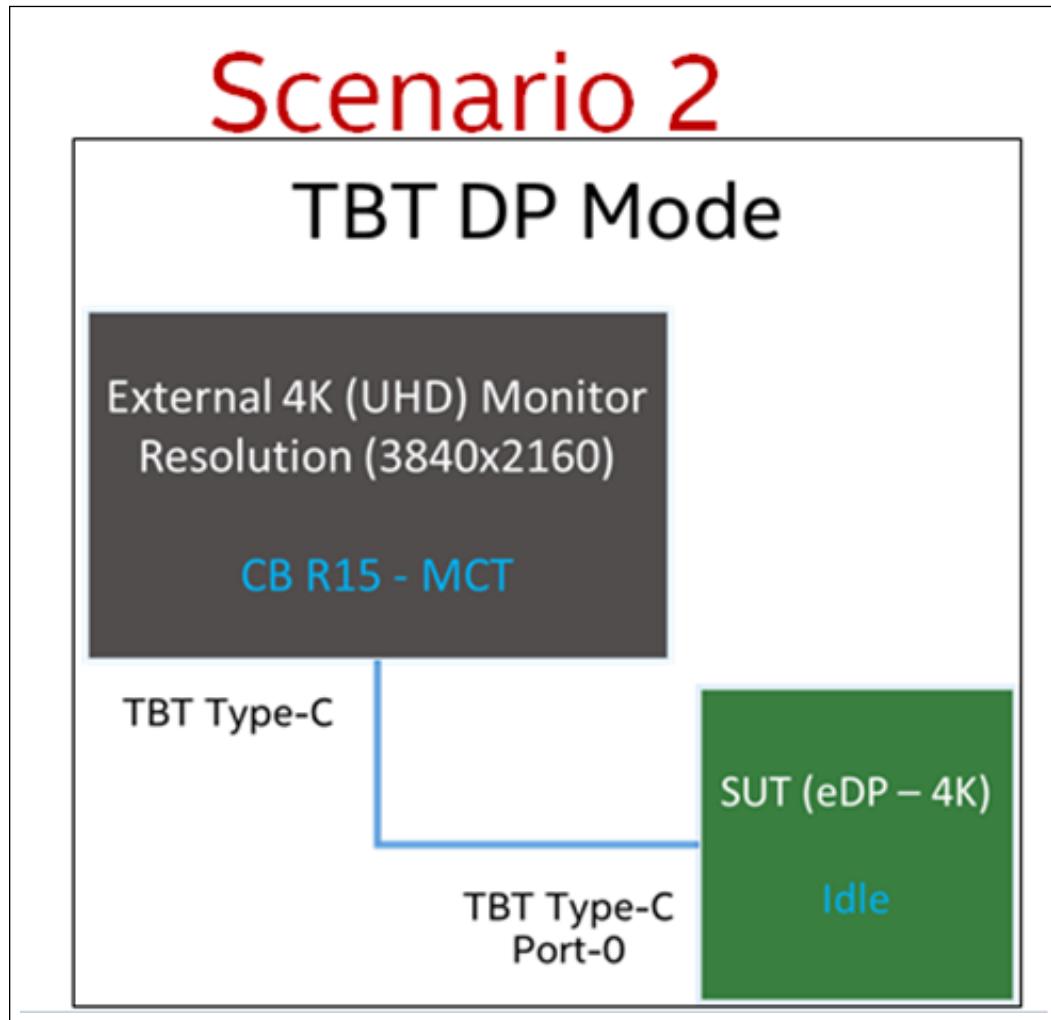
**Table 221. TGL-UP4 TCSS Scenarios with Integrated Thunderbolt**

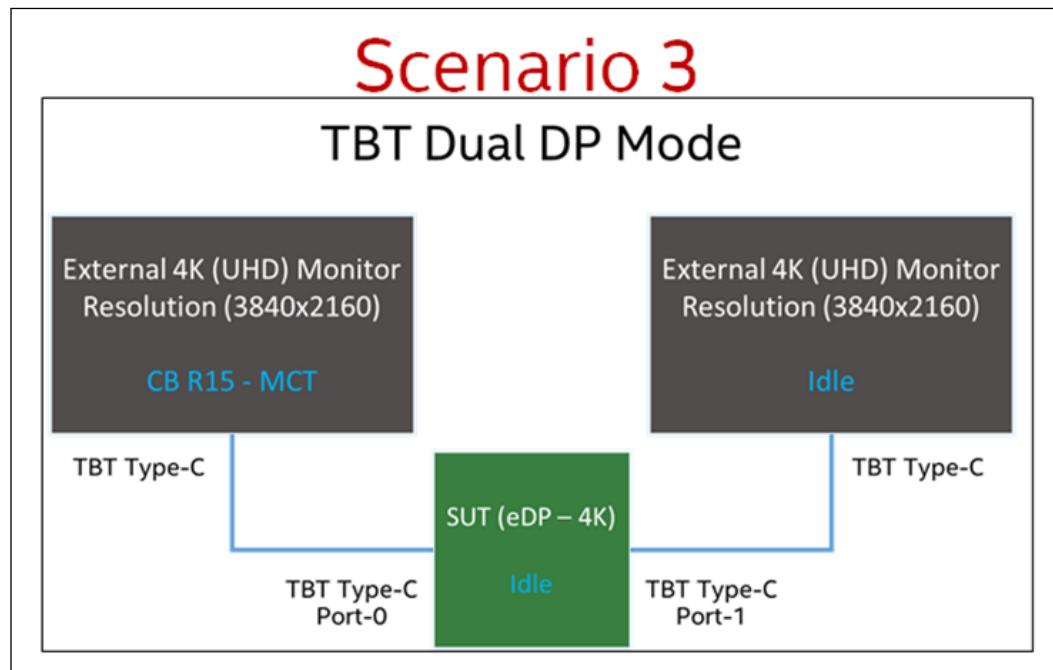
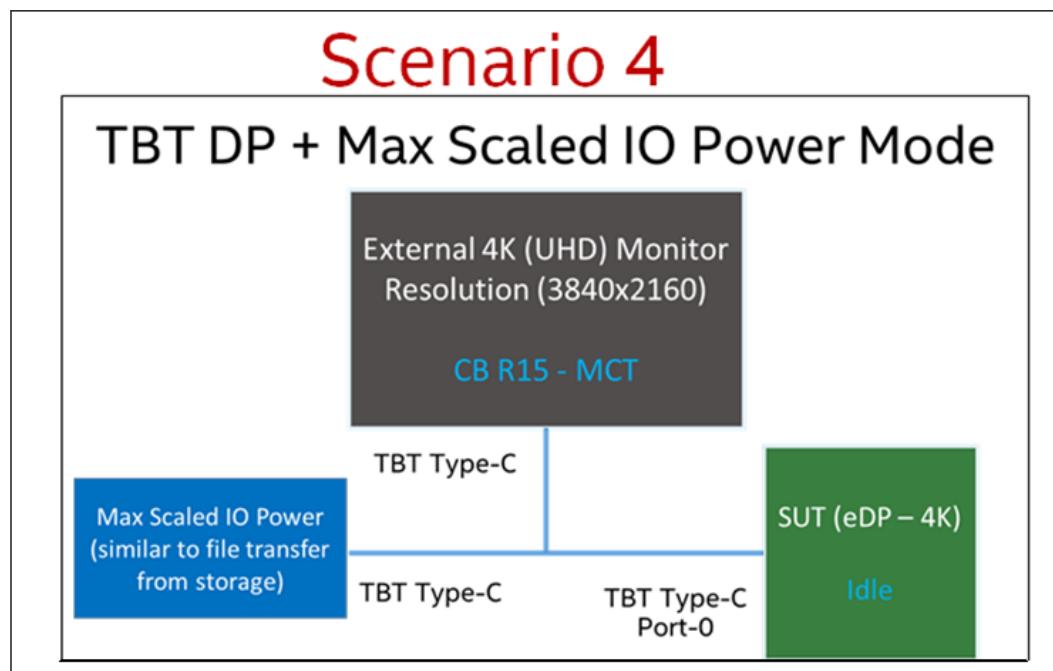
TCSS Scenario	Description	TGL-UP4 TCSS Power Adder (W)	TGL-UP4 SoC Power Target (W)
Baseline	TC-Cold NDA, (Internal Display ( eDP ), 4K resolution (3840x2160)	0	9
DP Alternate Mode	1x4K at 60Hz external display, extended mode	0.7	9.7
Thunderbolt DP Mode	1x4K at 60Hz external display, extended mode	0.9	9.9
Thunderbolt dual DP Mode	2x4K at 60Hz external display, extended mode	1.7	10.7
Thunderbolt DP Mode, Max IO	1x4K at 60Hz external display, IO power scaled to max to simulate full BW	1.4	10.4

**NOTES**

- All values are pre-Si estimates on scaled ICL-U measured data and are subject to change
- Test were performed with top bin with fixed P1 frequency for median UP3 parts at T<sub>j</sub> Max at 100C
- Workload used Cinebench R15 MCT on external display in extended mode with other displays
- SoC power adders will remain at 28W45W nominal TDP level
- ~900mW additional power adder impact per traditional TCSS port with device attached and active
- SoC power increase only; additional system power losses should be factored into system analysis.

**Figure 218. Scenario 1: Alternate DP Mode**

**Figure 219. Scenario 2: TBT DP Mode**

**Figure 220. Scenario 3: TBT Dual DP Mode****Figure 221. Scenario 4: TBT DP + Max Scaled IO Power Mode**

#### 10.4.5 **P<sub>sys</sub>** and Other Considerations for Using Smaller AC Adapter

There are some cases where a smaller adapter with lower sustained power level can be used for better portability or lower adapter cost. However, there will be impacts on the dead battery operation, Turbo performance, and charging time.

If an AC adapter with sustained power level less than PL2 + P<sub>ROP\_max</sub>, it is recommended to have P<sub>sys</sub>PL2 enabled and set P<sub>sys</sub>PL2 to the sustained power rating of AC adapter. However, there could be performance impact if the sustained power of adapter is much less than the PL2 + P<sub>ROP\_max</sub> and user loaded the ROP power close to the worst case maximum. Here is an example.

For example, in a system with PL2 of 25W, PL4 of 46W, P<sub>ROP\_max</sub> of 15W, and conversion efficiency of 90%, the sustained power level of adapter can be calculated with the following equation. An adapter with a sustained power rating of 45W is recommended for this system.

$$P_{\text{sustained}} = (PL2 + P_{\text{ROP\_max}}) / \text{Efficiency}$$

However, if a smaller adapter with 30W sustained power rating is used with this system, without P<sub>sys</sub>, the PL2 will have to be reduced down to 12W, which is even less than PL1 of 15W. In this scenario, both PL2 and PL1 have to be reduced to 12W when the battery is dead. If the system has a traditional charger, the PL2 and PL1 have to be reduced to 12W no matter if the battery is dead or not as long as the adapter is connected.

On the other hand, if the system has P<sub>sys</sub> enabled, the performance will be managed to keep the P<sub>sys</sub>PL2 at 30W. If the rest of platform power is lowered to 10W, the SoC will have 17W of power budget and the performance should be better than the case without P<sub>sys</sub>.

With a smaller adapter, the charging time from 0% to 80% state of charge will likely be impacted. However, the actual charging time impacts depends on many other factors besides the sustained power rating of adapter, such as the power state of system, battery size, constant current charging rate. As the sustained power rating is reduced, the power available for charging is going to be reduced first.

#### 10.4.6 Protection Mechanisms

The electrical protection mechanisms cover the following two scenarios: the magnitude of system peak power exceeds the adapter transient power limit, and the duration of system peak power event exceeds the duration of adapter transient capability.

In the event when system peak power might exceed the adapter transient power limit, the over-current-protection (OCP) is designed to sense the adapter current and trigger PROCHOT# if the over-current condition is met. For the discrete implementation, refer to "Battery Voltage Droop and Brick Over Current Protection Circuit Design" doc# 556361. There are chargers with integrated PROCHOT# circuit available as well.

However, after PROCHOT# is triggered, the SoC frequency is going to be throttled to the absolute minimum causing significant performance loss. Because running at minimum frequency builds up thermal headroom for turbo, it is possible that the processor can cause repeated triggering of PROCHOT#. To prevent this scenario from happening, the system EC may reducePL4 as a preemptive measure if an under-sized adapter is connected.

## 10.5 Battery Charging System

This section reviews battery charger topologies and requirements in mobile system designs.

During CPU Turbo Boost periods, the system may overload the input power source.

It is required that the battery charger has protection mechanisms such as FAST PROCHOT# and Vmin Active Protection (VAP) to mitigate overloading of the power source. There are two types of charger topologies capable of doing this:

1. Hybrid Power Boost (HPB) battery charger
2. Narrow VDC (NVDC) battery charger

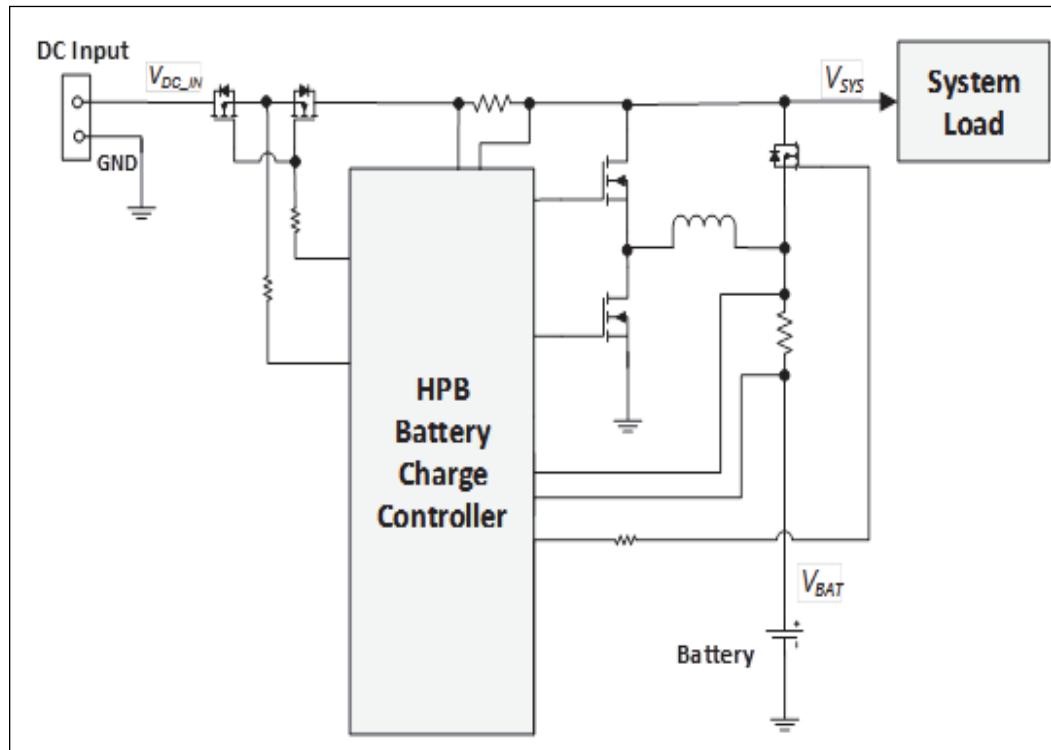
NVDC battery chargers are often capable of operating in both NVDC and HPB modes.

### 10.5.1 Hybrid Power Boost (HPB) Battery Charger

In the Hybrid Power Boost configuration, the synchronous buck converter runs as a normal buck converter when the adapter provides power to the system and is charging the battery. When the adapter power is not sufficient, the synchronous buck converter runs in reverse to boost the battery voltage to around 20V. Thus the battery supplements the adapter whenever the adapter power is not sufficient. This requires no circuit changes from a traditional adapter. The change is required in the control circuit (the Battery charger controller).

The advantage of this system over a traditional charger is that the battery is able to assist the adapter during turbo workloads. This system has the disadvantage that the light load efficiency is pretty low as it is difficult to achieve high light load efficiency at high input voltage.

**Figure 222. Hybrid Power Boost (HPB) Battery Charger**



### 10.5.2 Narrow VDC (NVDC) Battery Charger

**Figure 223. Narrow VDC (NVDC) Battery Charger**

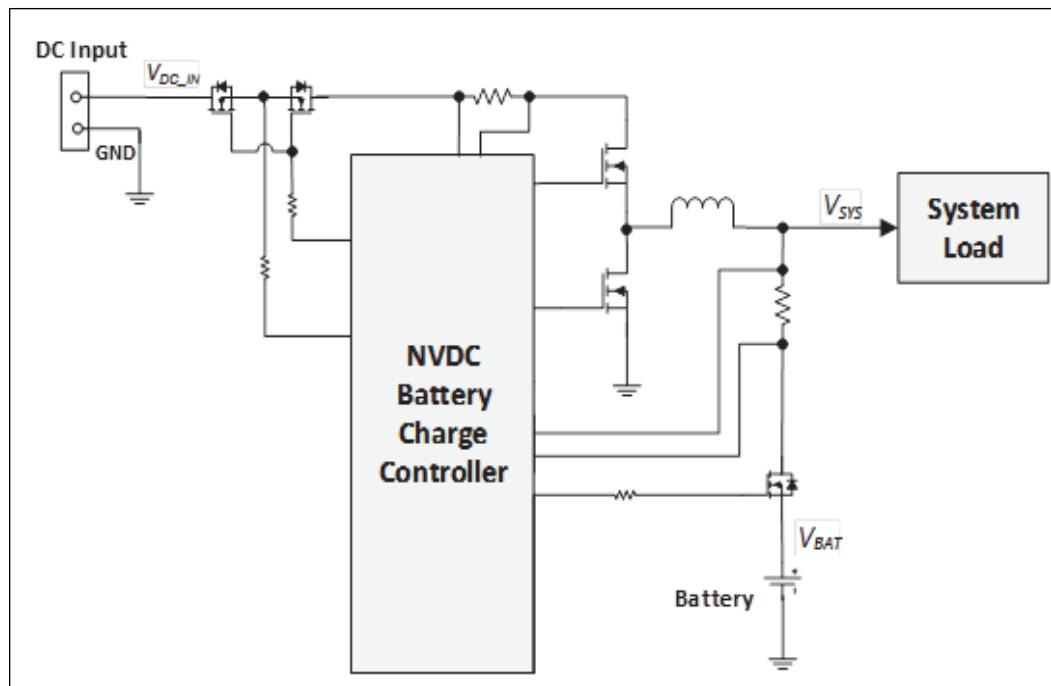


Figure above shows the Narrow VDC (NVDC) topology. Here, the system bus ( $V_{sys}$ ) is not connected directly to the adapter. It is connected to the output of the buck converter. Hence, NVDC operates only as a buck converter, both when NVDC charges the battery and when the battery supplements the adapter and provides power to the system. NVDC implementation reduces the switch-over period between the charging mode and the hybrid power mode. NVDC implementation allows the system to minimize the period of overloading the input power source when CPU is in Turbo Boost mode.

The advantage of using the NVDC system is that the overall system efficiency is better compared to the Hybrid Power Boost charger. The system can be designed for a smaller voltage rating since the system has a lower  $V_{in}$ . The disadvantage is that the charger components' size and power dissipation increases.

### 10.5.3 Benefits and Trade-Offs

**Table 222. Benefits and Trade-offs of the Different Chargers**

PD Architecture	Turbo support	Advantages	Limits
Traditional charger	No. Turbo is limited to the capability of the adapter or Battery (varies widely by state of charge)	A very common for system with less dynamic load.	VRs with large range of input voltage are less efficient at light load. The AC adapter has to be sized to supply peak system power for ~10ms.
Hybrid power boost	Yes	Higher input voltage is more suitable to larger system with large power consumption.	VRs with large range of input voltage are less efficient at light load. The AC Adapter has to supply peak system power for 1ms.
NVDC with 2S battery	Yes	Design optimized with Lower input voltage has better light load efficiency.  FETs can be optimized for lower input voltage and VRs can be smaller and faster.	Charger's components (FET/Inductor) size are often larger and power dissipation is often greater.

[Platform Power Monitoring And Control \( \$P\_{sys}\$ \)](#) on page 411 describes  $P_{sys}$ , the protection mechanism for the input power sources.

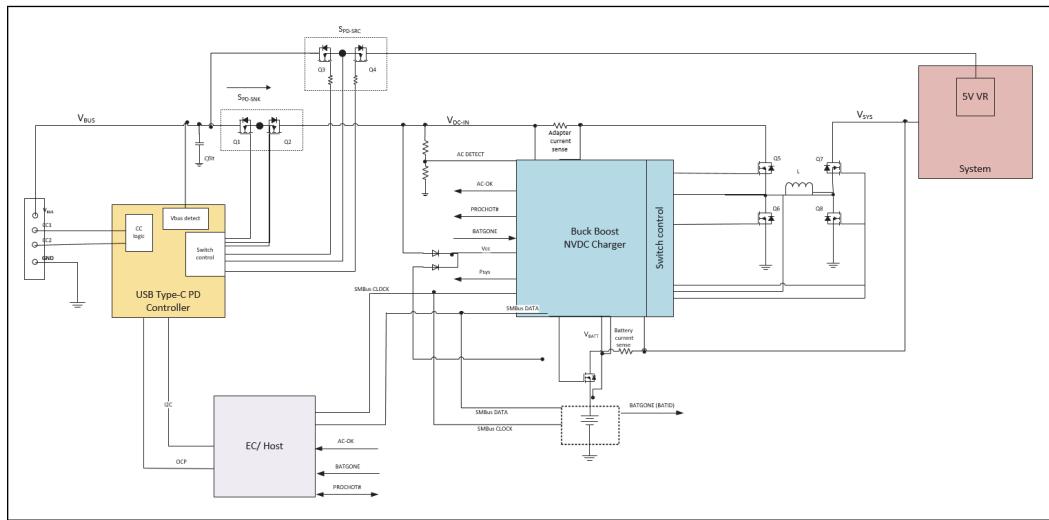
### 10.5.4 Supporting 5V-20V USB Charging

USB-C PD specification suggests the following operating modes for the USB-C PD supported ports:

1. System battery sources power to a sink device connected to a USB- PD port (5V, up to 3A OUT)
2. 5V USB AC Adapter sources power to the system(5V, up to 3A IN)
3. USB PD AC Adapter sources power to the system and battery (9V, 15V, 20V up to 3A or 5A IN)

The Buck Boost charger provides a simple, cost effective and space saving solution that support all of these charging modes.

**Figure 224. Detailed View of USB-PD Subsystem**



**Figure 225. Modes of Operation**

OPERATION							
Mode	Power Flow	Topology	Q1	Q2	Q3	Q4	
1 <b>Battery Powering USB</b> (e.g. mouse, KB, HD, charging phone/tablet; V <sub>batt</sub> >V <sub>usb</sub> )	Batt→USB	Buck CV	Control FET	Sync Diode	ON	OFF	
2 <b>Generic USB Charging Battery</b> (V <sub>usb</sub> <V <sub>batt</sub> , i.e. V <sub>usb</sub> =5V)	Batt←USB	Boost CC/CV	Sync Diode	Control FET	ON	OFF	
3 <b>USB PD Charging Battery + Sourcing System</b> (V <sub>usb</sub> >V <sub>batt</sub> , i.e. V <sub>usb</sub> =12V/20V)	Batt←USB	Buck CC/CV	ON	OFF	Control FET	Sync Diode	
4 <b>Battery Operation w/ No USB</b> (No adapter or USB plugged in)	None	Short Protection	OFF	OFF	OFF	OFF	

#### Features Required in Buck Boost Charger

1. Adapter voltages supported: 3.2V - 21.5V Sustained (recommended)
2. Battery configurations supported: 2S - 4S (5.6V - 18V)
3. Two level programmable input current limit (sustained and peak capability power sources)
4. Default input current limit programmable by hardware pin
5. Platform power monitoring ( $P_{sys}$ )
6. Fast PROCHOT# - System voltage, Input current (and voltage), Battery discharge current
7. Low power mode during battery only Sx/ S0ix mode (consume <1.5mW)
8. SMBus or I2C compatible.

9. Vmin Active Protection (VAP): Use the input decoupling to supplement the system when in battery mode, during peak spikes that cause the system voltage to be close to minimum operating range (recommended).

For detailed Buck Boost charger requirements, refer to Buck Boost Charger Specification – Power Supply Design Guide #571381

#### **Design Considerations for 5V VBUS Operation**

It is important to consider the following factors when using a buck boost charger on the platform:

1. With a 5V USB input, the inrush current on the system bus should be limited when the charger and system rails are enabled. This is especially important under a dead battery power on scenario.
2. The maximum resistance from the USB VBUS to the input of the charger should be <50-60mOhm in order to operate at 5V.
3. Dead battery power on sequence with a port controller needs to take into account a way to power on the TCPM/ EC and meeting the pSnkStdby requirement. If the TCPM is powered using the V3.3A rail, care should be taken to ensure that inrush current does not exceed the default current limit set on the charger.

## **10.6 USB Type C Power Delivery Considerations**

### **PD Controller**

The PD controller is a power management chip that provides detection of cable-plug and orientation, communication with the connected device for power and mode negotiations, and switching of the power delivery current paths.

### **PROCHOT# Assertion Scenarios**

In order to maximize Turbo performance when no AC Adapter is available and to prevent over-stressing the battery capability of the system, the PD Controller must be immediately pull down Alert# and PROCHOT# signals when the following scenarios occur:

New Sink is Connected

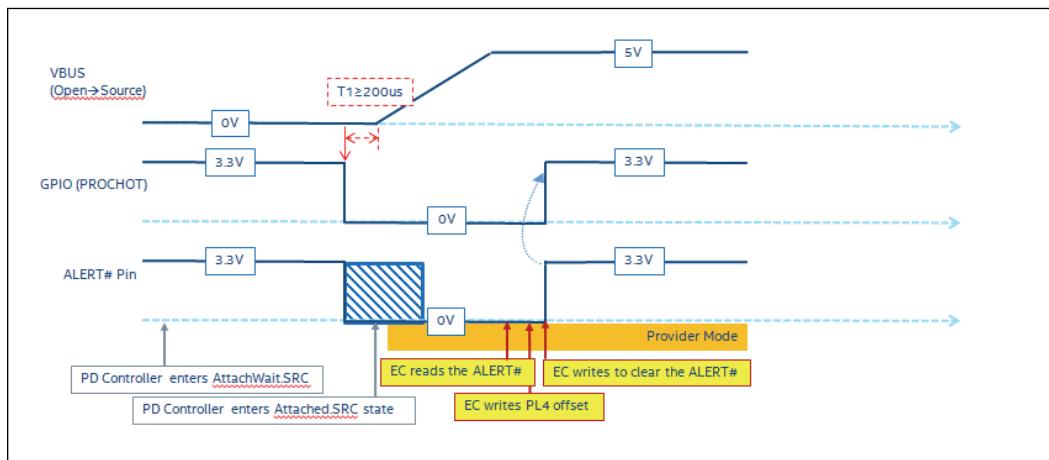
Requirements for PD Controller:

- Assert PROCHOT# and ALERT# at least 200µs before entering Attached\_SRC state (supplying vSafe5V to the Sink)
- De-assert PROCHOT# only after ALERT# is de-asserted.

Requirements for EC:

- Write to PL4 offset
- Write to clear the ALERT#

**Figure 226. Sink Connect Event**



New Source is Connected

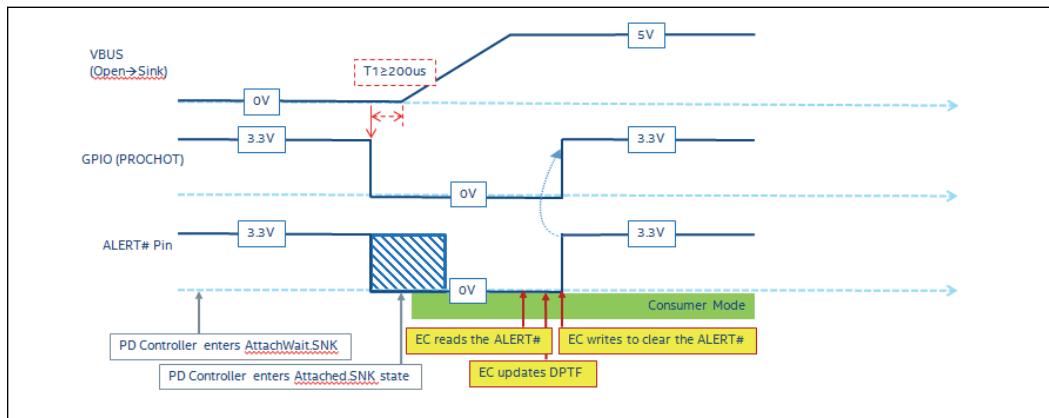
Requirements for PD Controller:

- Assert PROCHOT# and ALERT# at least  $200\mu s$  before entering Attached\_SINK state (vSafe5V is supplied by the source)
- De-assert PROCHOT# only after ALERT# is de-asserted.

Requirements for EC:

- Write to PL4 offset
- Write to clear the ALERT#

**Figure 227. Source Connect Event**



A Source is Disconnected

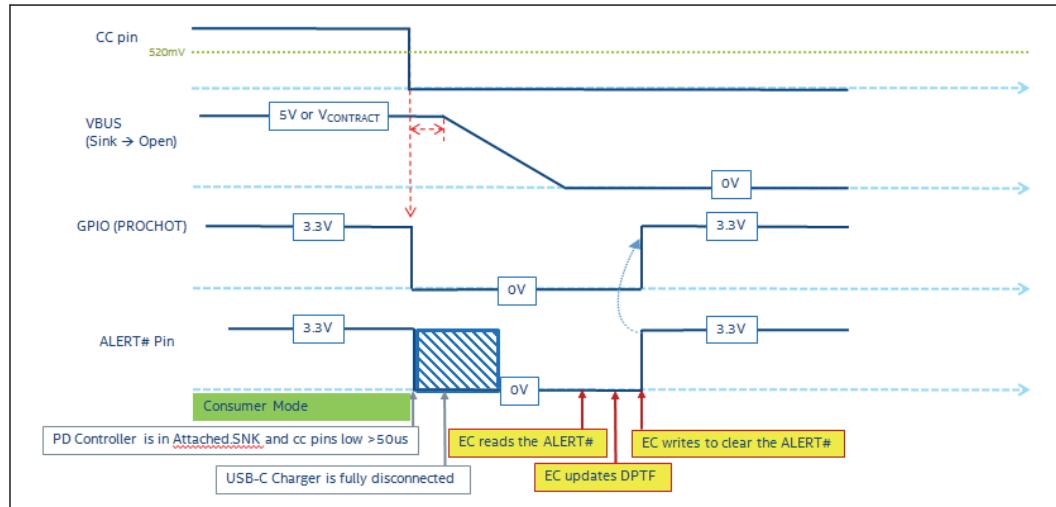
Requirements for PD Controller:

- If the PD controller is in Attached\_SINK state; immediately assert PROCHOT# and ALERT# when the CC pin has been below 520mV for  $50\mu s$  (debounce time)
- De-assert PROCHOT# only after ALERT# is de-asserted.

Requirements for EC:

- Update DPTF with new Vcontract
- Write to clear the ALERT# only after receiving PBOK from DPTF

**Figure 228. Source Disconnect Event**



A Source has Negotiated for Lower Power

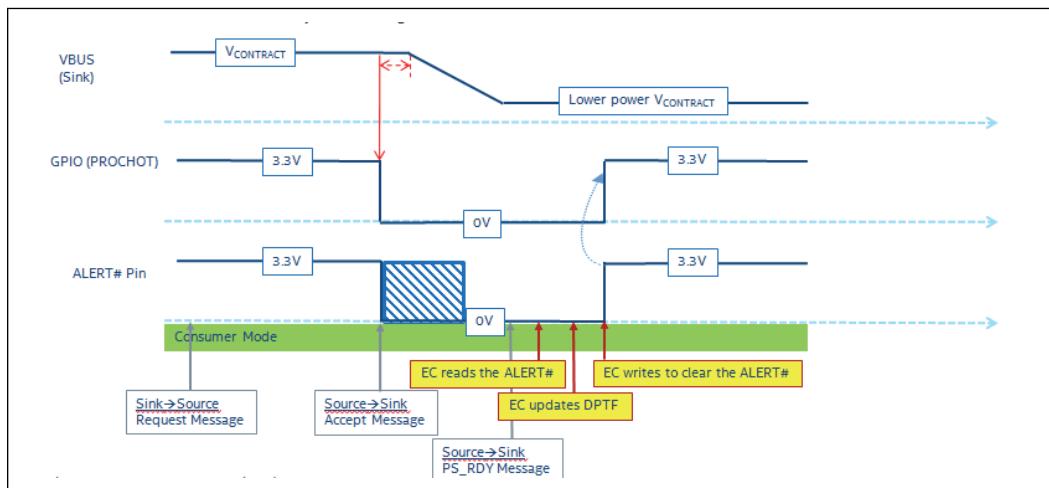
Requirements for PD Controller:

- If the PD controller transitions from PF\_SNK\_Ready to PF\_SNK\_Evaluate Capability state assert PROCHOT# and ALERT# immediately after receiving Source Capabilities message.
- Do not assert PROCHOT# in any other entry to PF\_SNK\_Evaluate Capability state scenario.
- De-assert PROCHOT# only after ALERT# is de-asserted.

Requirements for EC:

- Update DPTF with new Vcontract
- Write to clear the ALERT# only after receiving PDOK from DPTF

**Figure 229. Source Power Reduction Event**



A Source has Negotiated for Lower Power

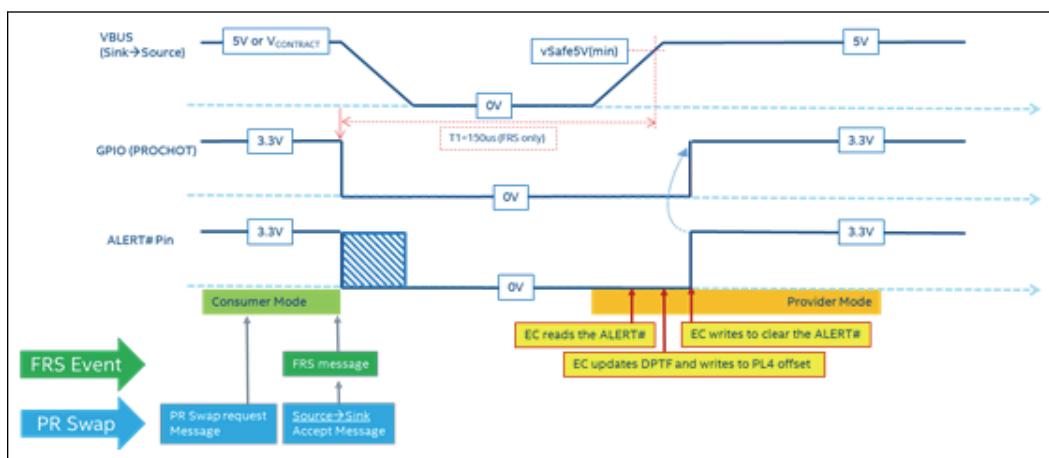
Requirements for PD Controller:

- Assert PROCHOT# and ALERT# based on FRS or PRS scenarios described on the following side.
- De-assert PROCHOT# only after ALERT# is de-asserted.

Requirements for EC:

- Update DPTF with new Vcontract
- Write to PL4 offset
- Write to clear the ALERT# only after receiving PDOK from DPTF

**Figure 230. Power Role Swap Event Sequence**



## 10.7

## Platform Power Monitoring And Control (Psys)

For thermal control, previous platforms had the ability to throttle the processor speed to reduce SoC power consumption and keep the average power dissipation of the SoC package within defined limits. Tiger Lake Platform has added the ability to monitor and control the average power the platform is consuming and throttle the SoC to keep the overall platform power dissipation within defined limits. The new platform power level limits are useful to keep the average power of the platform within the power ratings of input power sources, voltage regulators and batteries. The feature of measuring total platform system power is termed Psys or System Input Power Monitor.

### 10.7.1

#### Benefits

The Psys function provides a measure of the instantaneous power consumption of the entire platform. The PCode in the SoC uses the measured platform power to adjust SoC performance to keep the average platform power within desired limits. The measured platform power is also available to the Embedded Controller (EC) via the PECI interface and to software and firmware applications via MSR registers. Some systems may also have the EC sample the analog Psys signal after the resistor to avoid latency. The following is a list of benefits and features available with the SoC varying performance to keep the average platform power within limits and the ability of other software agents to read the platform power:

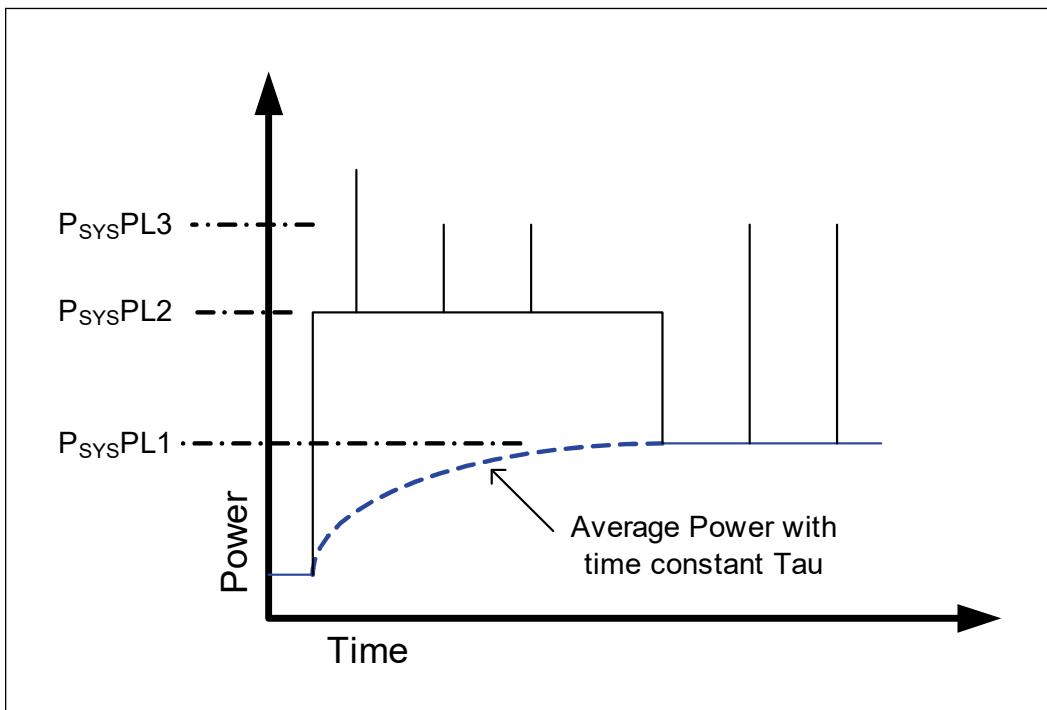
1. Real time monitoring of the platform power enhances the ability to support turbo mode when the platform is being powered by the battery only.
2. The average power of the platform can be kept within the average power rating of the input power source even if peak platform power temporarily exceeds the rated power of the input power source. This allows smaller wattage input power sources (battery and AC adapter) to power a platform that has high peak power requirements by keeping the average power demand within limits of the input power sources.
3. The platform power demand can also be adjusted to keep the average platform power and thus the average platform temperature under desired levels.
4. Previous thermal solutions measured the power to the SoC and used an estimate of the power the rest of the platform (ROP) was consuming to determine power budgets. Some potential performance gains are not realized in the cases where the actual ROP power consumption is less than the estimate. For these circumstances, using the actual platform power consumption (Psys) will provide an increase in turbo performance.
5. The platform instantaneous power consumption can be monitored by firmware and software to provide applications that provide power monitoring and feedback to the user.

### 10.7.2

#### Theory Of Operation

The Psys feature function parallels the package level power monitoring features. Registers hold defined power limits for the platform. The new power limits are defined as PsysPL1, Tau, PsysPL2 and PsysPL3. Figure below shows the relationship between the different power levels.

**Figure 231. Relationship Between Platform Power Levels**



The  $P_{sysPL1}$  level is the long term sustainable power limit of the platform. This can be the rated power of the adapter, the discharge rate of a battery, the power capability of the platform or a combination of all of these.  $P_{sysPL1}$  has a time constant ( $Tau$ ) associated with it.  $P_{sysPL2}$  is a power level that the platform is allowed to have for a temporary time. For example, a battery can be discharged at a higher rate for a short period of time as long as the average discharge is equal to  $P_{sysPL1}$ . Shorter period but higher power limits can also be supported up to the  $P_{sysPL3}$  level, for example, discharging the battery at 4C for less than 10ms and a 9% duty cycle. The SoC will adjust power consumption to drive the average power consumption to the  $P_{sysPL1}$  level over a long period of time which is greater than  $Tau$ .

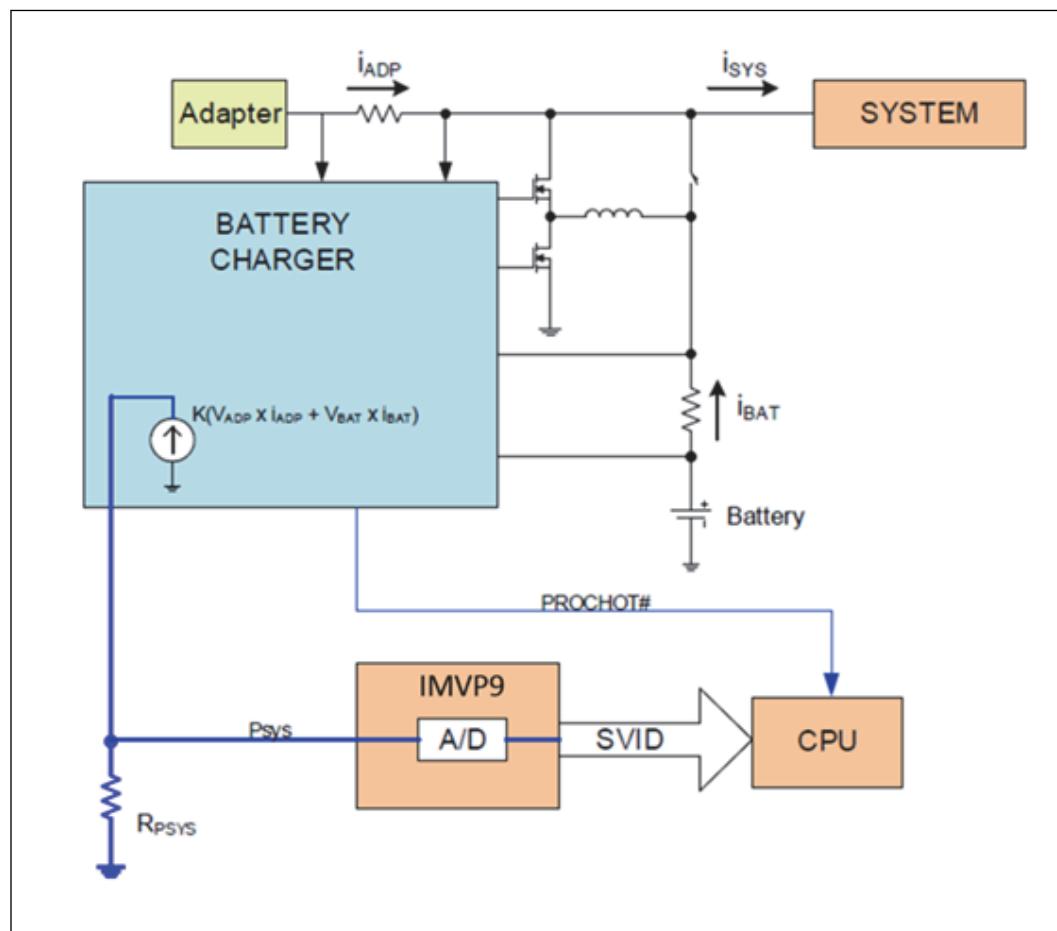
### 10.7.3

### Hardware Ingredients

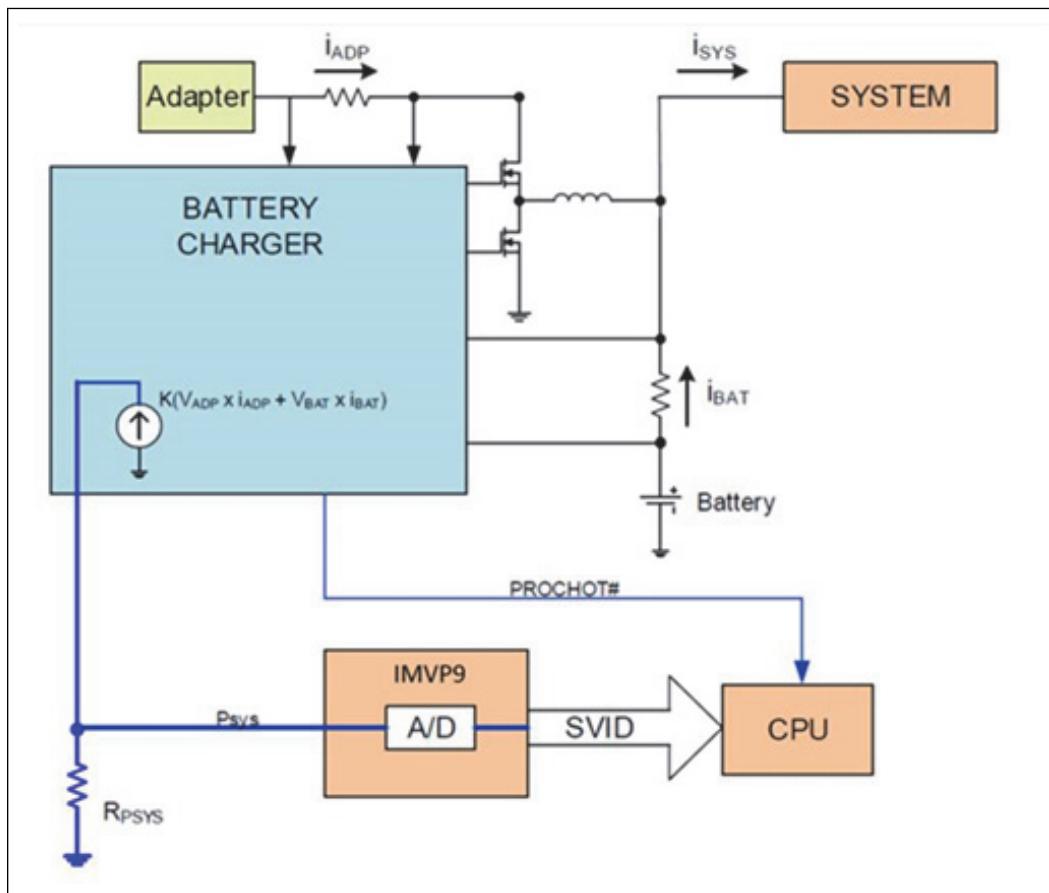
The  $P_{sys}$  feature requires some hardware components for implementation in order for the platform to measure the power it is consuming. Figures below show typical implementations of the  $P_{sys}$  feature. The platform must be able to monitor the power going to the platform. In a battery powered device, the power going to the system is the power coming from the input adapter, plus any power the battery is providing. Using a battery charger with a power monitoring function makes the most sense since the battery charger monitors both of these pieces of information already. Several battery chargers with a power monitoring feature have been enabled to support  $P_{sys}$  on Tiger Lake platforms.

If  $P_{sys}$  is used to protect the input power source then specific information about the input power source must be relayed to the platform. The platform must know the power capability of the input power source which can be a wall adapter, wireless system charger, battery, USB-PD port, USB-BC port or any other of a variety of sources. Typically, the input power source capability will be determined by the EC on the platform.

Figure 232. HPB Battery Charger with Psys Implementation



**Figure 233. NVDC Battery Charger with Psys Implementation**



The battery charger provides a current output that is proportional to the power being delivered to the platform (from the brick, battery or both). A shunt resistor is used to convert this current output to a voltage output and to scale the voltage to the full scale input voltage range of an analog to digital converter. The platform uses the SVID interface to read the power data. The measured platform power is provided in SVID register 0Dh, location 1Bh. An 8 bit A/D converter in the IMVP9 controller is used to convert the power monitoring information. The processor then reads the power measurements via SVID from SVID address 0Dh, location 1Bh. Refer the 'Serial VID (SVID) Protocol' specification and the 'IMVP8 PWM VR' specification for specifics on the IMVP9 and SVID.

#### 10.7.4

#### Software /Firmware Ingredients

The new PSYS Monitoring and Control Parameters are:

**P sys** is the value provided to the processor PCU from the platform through SVID quantifying the total platform power load. This value shares the name of the feature.

**P sys P<sub>max</sub>** is the maximum power the platform is capable of drawing. It is the sum of PL4 plus the Rest of Platform power.

**P sys PL1** is the targeted total platform power level to which the PCU's platform power monitoring and control will manage over time. The value is provided by the system.

**P<sub>SYS</sub> PL2** is the highest power level to which P<sub>SYS</sub> will be allowed to go on a temporary basis while there is budget to do so (analogous to RAPL's PL2). The value is provided by the system.

**Tau** is the time window which roughly characterizes the time scale under which P<sub>SYS</sub> monitoring and control manage to the target P<sub>SYS</sub>PL1 value. The value is provided by the system.

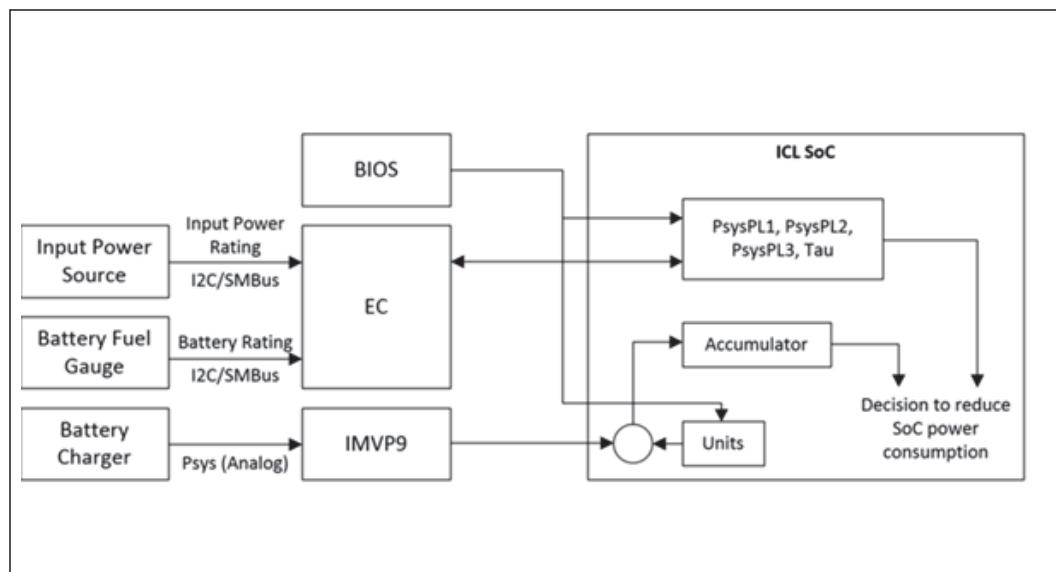
**P<sub>SYS</sub> PL3** is the same limit value/feature as the legacy PL3. P<sub>SYS</sub>PL3 triggers control such that P<sub>SYS</sub> power level events exceeding it are limited to a small duty-cycle percent on time; e.g., 10%; notwithstanding power spiking events caused by another component on the platform. No change in function. P<sub>SYS</sub>PL3 limit value uses the platform level power (P<sub>SYS</sub>) as a basis for decisions instead of package power.

The MSR registers and bit definitions pertinent to P<sub>SYS</sub> functionality can be found in the Tiger Lake BIOS Guide (Refer to table below).

**Table 223. Access Availability of the Various P<sub>SYS</sub> Configuration Parameters**

Parameter Name	Description	Access (Addresses Defined in HAS)			
		MSR	MMIO	PCIE	BIOSMB
P <sub>SYS</sub> PL1	Platform average power target	RW	N	RW	N/A
P <sub>SYS</sub> PL2	Turbo/Momentary average platform power target	RW	N	RW	N/A
P <sub>SYS</sub> PL3	Duty cycle controlled average platform power target	RW	N	RW	N/A
P <sub>SYS</sub> Tau	PL1/PL2 Time Scale	RW	N	RW	N/A
Enable	PC Monitor/Control On/Off	RW	N	RW	N/A
P <sub>SYS</sub> Value	Actual value of P <sub>SYS</sub>	RO	N	RO	N/A

**Figure 234. Information Sources and Flow Diagram**



## 10.7.5 Configuration

The  $P_{sys}$  feature can co-exist with other thermal and power management features found on the platform.

At power on, BIOS must initialize the  $P_{sys}$  power limit registers ( $P_{sys\_P_{max}}$  and  $P_{sysPLx}$ ) to reflect the basic configuration of the platform. During run-time, the EC or other software/firmware agents can update the  $P_{sysPLx}$  values as platform conditions change such as a new input power source being plugged in.

## 10.7.6 Implementation of $P_{sys}$

$P_{sys}$  is enabled by:

1. Clearing bits: [30] SVID Presence, and [31] Platform IMON ( $P_{sys}$ ) Disable. Clear these at Flash Address FCPUSBA + 004h (default Flash Address 304h). Refer to the SPI Programming Guide.
2. Enable  $P_{sys}$  functionality in your charger. Usually done through your EC.
3. Program the  $P_{sys\_P_{max}}$  value to PL4+ROP<sub>MAX</sub> (Rest Of Platform) power. Refer to the BIOS Specification.
4. Select a value for  $R_{P_{sys}}$  as shown in Section below.

The  $P_{sys\_P_{max}}$  value is the scale that the processor uses to interpret the  $P_{sys}$  values read from the IMVP9 controller. There is no specific  $P_{sys\_P_{max}}$  which is correct.

1. Use a  $P_{sys\_P_{max}}$  value that is large enough to cover the most power the platform could possibly draw.
2. Use a  $P_{sys\_P_{max}}$  value which is small enough to provide the granularity appropriate for the platform.

### Determining the Value of $R_{P_{sys}}$

$R_{P_{sys}}$  is sized to develop the  $P_{sys}$  current from the charger so the voltage input to the IMVP9 ADC will reflect the value of  $P_{sys\_P_{max}}$  as FFh.

$R_{P_{sys}}$  should be placed near the IMVP controller.

[Figure 232](#) on page 413, here are some examples where:

**$P_{sys\_P_{max}}$**  = the max power for a platform, PL4 + ROP<sub>MAX</sub>. Programmed as above.

**ADC V<sub>REF</sub>** = the full-scale voltage on the IMVP9  $P_{sys}$  pin. An ADC converts this voltage level to FFh. Different for each IMVP9 controller.

**I<sub>P<sub>sys</sub></sub>** = the  $\mu$ Amps/Watt of the  $P_{sys}$  signal from the charger. A typical value is 1 $\mu$ A/W, but your charger may vary.

The formula for determining the value of  $R_{P_{sys}}$  is:

$$R_{P_{sys}} = \text{ADC } V_{REF} / (I_{P_{sys}} * P_{sys\_P_{max}})$$

**Table 224. RPSYS Examples**

P <sub>SYS_PMAX</sub>	I <sub>PSYS</sub>	ADC V <sub>REF</sub>	R <sub>PSYS</sub>
35W	1 µA/W	1.2V	34.3KΩ
95W	2 µA/W	3.3V	17.4KΩ
175W	1 µA/W	1.6V	9.1KΩ

## 10.8 System Peak Power Management (Pmax)

To achieve improved system performance, Tiger Lake introduces higher PL4 levels compared to the previous platforms. Many customers are using batteries with two cells in series (2s), and may be constrained on how high the peak power can be supported by the platform due to the minimum system voltage of 5.4 -5.6V. Intel proposes a framework with a number of new technologies to allow the system to support higher peak power.

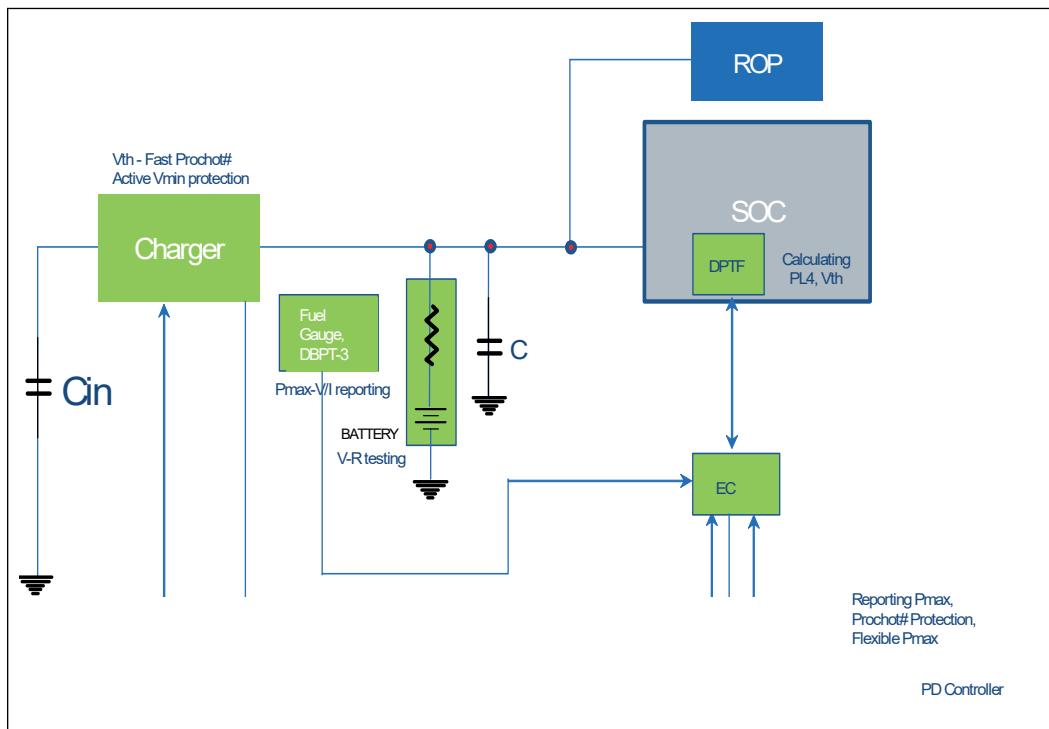
Figure below shows the proposed framework. The operation is expected to be as follows:

The DPTF software (which resides in the Operating system) will be calculating the SOC PL4 and the system threshold level based on the data provided to the DPTF through the EC by the fuel gauge (DBPT-3). DPTF will find the highest possible PL4 level and report it to the SOC, and then will calculate the lowest possible threshold system voltage at which the system minimum voltage Vmin. The EC will be setting this value in the charger.

If the system voltage drops below the Vth, the charger will assert PROCHOT# and start supplementing the battery until the system power drops to the level below the peak power capability of the battery.

The second part of the framework is the Type C, and the PD controller. If a new device is inserted in the Type C, the PD controller will assert PROCHOT# to prevent the system from black screening, and then report the new peak power demand from the device to the EC, which will put this value in the SOC for the calculation of the new PL4 level. This technology is required to allow the SOC PL4 and the threshold voltage to be calculated for the level of the actual system peak power (typical values), and not the worst case scenario.

**Figure 235. Tiger Lake Pmax Framework**



In order to support the Tiger Lake Pmax framework for 2s system, the customers are recommended to use the following hardware, software and firmware solutions:

- Charger
  - Supporting system voltage protection ( $V_{th}$  setting, PROCHOT# assertion)
  - Supporting  $V_{min}$  Active protection
  - Supporting various other protections: battery and adapter currents, input voltage
- Battery Fuel Gauge
  - Supporting DBPT-3
- DPTF v3
- USB PD Controller with PROCHOT# and functionality
- EC firmware to support Pmax framework
- Optional: Barrel adapter protection circuitry (a logic circuit)

### 10.8.1 Fast PROCHOT#

The PROCHOT# signal shown in [Figure 232](#) on page 413 is a signal that could be used to indicate to the CPU that a platform event has occurred that requires the immediate power reduction by the processor. The PROCHOT# signal provides a faster mechanism for power reduction than  $P_{sys}$  and is used to protect the input sources against instantaneous power events rather than the average power.

PROCHOT# can be triggered by multiple sources in the platform. PROCHOT# can be asserted by the battery charger under the following conditions:

1. The adapter current exceeds an upper threshold.
2. The battery discharge current exceeds an upper threshold.
3. The system voltage falls below a lower threshold.
4. The charger input voltage falls below a lower threshold.

If the PROCHOT# levels are programmable then the levels should be set to protect the input source. For example, the PROCHOT# for the adapter current level should be programmed to at the current the adapter can provide without damage or adapter turning off.

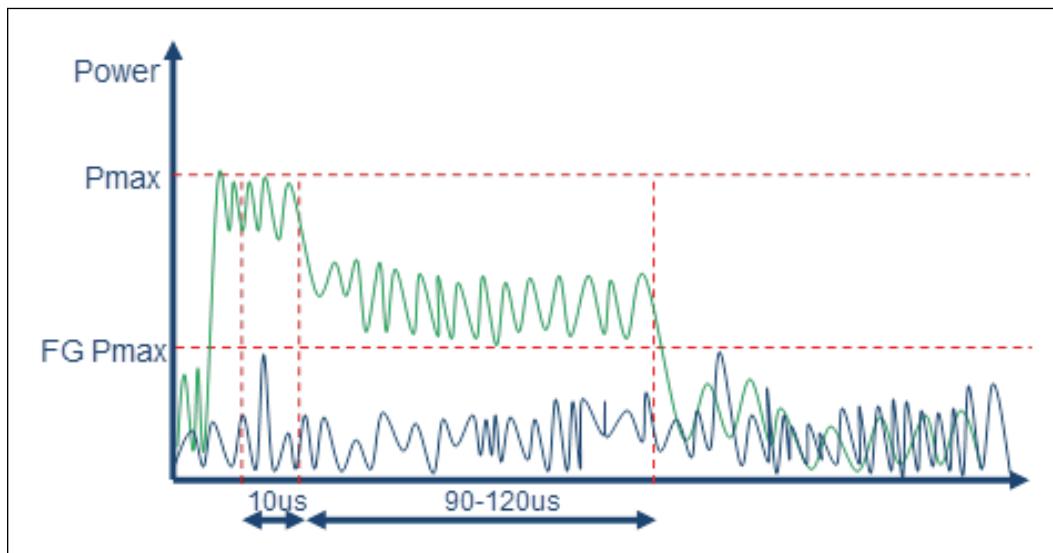
On Tiger Lake, the processor PROCHOT# response time has been reduced to 10µs. However total system power can still be above minimum supported limit for 300µs after PROCHOT# asserts. In battery-only case (where no adapter is connected), active V<sub>min</sub> protection is recommended so that the charger can still provide the necessary power and prevent unintended system shutdown. Because PROCHOT# holds processor frequency low for at least 10ms (the time duration is adjustable in the charger setting), the charger must take advantage of the time between power spikes to ensure that the input decoupling capacitors are charged to predetermined value (if there is no adapter present).

The fast response to the PROCHOT# assertion allows the DPTF to set the PL4 level potentially above the capability to the battery (or system V<sub>min</sub>). [Figure 236](#) on page 420 below contrast the allowed system power spike for the Tiger Lake platform (green curve) versus the previous platforms (blue curve). It is assumed that the maximum power that the system, can consume from the battery (limited by the system minimum voltage) is FG Pmax (reported by the Fuel Gauge through the DBPT), and today's system cannot exceed this level without potentially black screening. On the Tiger Lake Platform, with the advance of the fast PROCHOT# and active V<sub>min</sub> protection, the system is allowed to exceed the maximum system peak power for a limited duration. This allows the SOC PL4 levels to be set higher, and thus provide better performance. The system protection, including the fast SOC reaction time to the PROCHOT# assertion will guarantee that the system voltage does not drop below the pre-determined level.

The charger will assert PROCHOT# if the system voltage drops below the V<sub>th</sub>, a limit set by the DPTF in the charger. The charger is also expected to supplement the battery for a short duration (100-200µs, up to 300µs), if needed. As can be seen in the figure, the peak power drops after 10µs of the PROCHOT# assertion, and goes below the FG Pmax in another 90-200µs (TBD). With this technology in Tiger Lake, the SOC PL4 can be set to the levels far exceeding the capability of the battery without the risk of the system black screening.

For more details on the Tiger Lake Pmax operation, including the description on charger, fuel gauge, DPTF, EC, and the PD controller, refer to the Pmax White Paper (TBD).

**Figure 236. Comparison of System Pmax Scenarios**



## 10.8.2 Active Minimum Voltage Protection (Active V<sub>min</sub>)

Although fast PROCHOT# may be effective at protecting the system from an under-voltage condition, at some states of battery charge or at higher level of PL4, the SOC power drop 10 $\mu$ s after the PROCHOT# assertion may not be sufficient to protect the system against the black screening.

Given that the higher power requirements of Tiger Lake processor are running against the limits of the battery, there is potentially much performance that is left behind because of the necessary guardband against peak power events. Active V<sub>min</sub> protection feature was introduced to take advantage of the fact that these peak power events are rare and likely short in duration, and most importantly, that the SOC can go into the LFM mode a few hundred microsecond after the PROCHOT# assertion, and thus decrease it is power consumption even further.

Figure below shows the schematic for the today's Type C charging system. FETs Q1 and Q2 are used to block the voltage when the connector is not used, while FETs Q3-Q6 are used for the buck-boost charger. This configuration is used for the Type C system, which can be charged from the input voltage source of 5V to 20V, and where the system itself can be a voltage source.

**Figure 237. Traditional Type-C Buck Boost Charger Implementation**

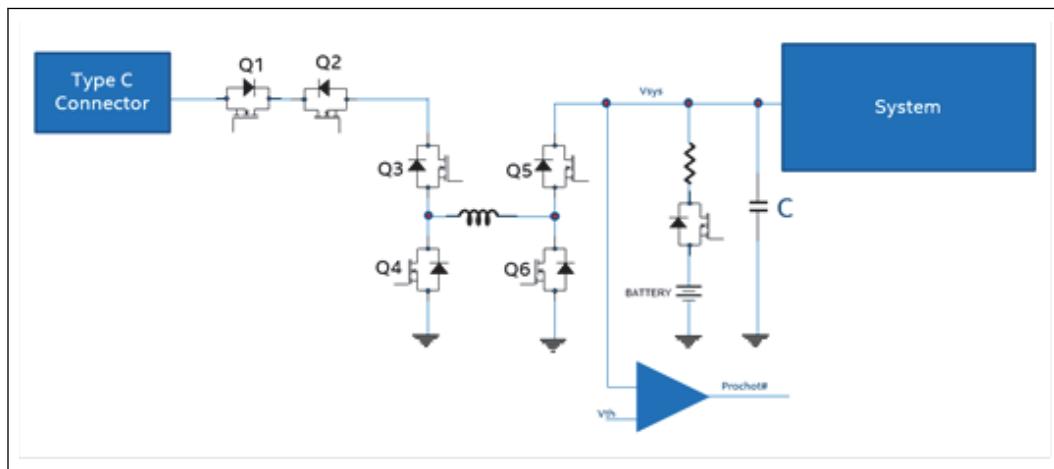
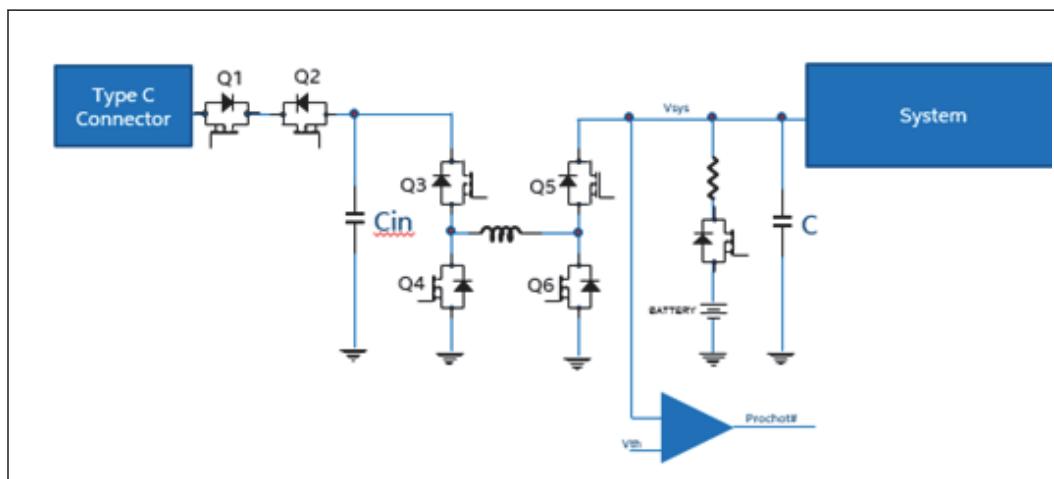


Figure below shows the proposed circuit, which would substitute this system and will allow much higher peak power than possible today. Note that the circuit looks identical to the existing circuit- and it is with a small change of an added capacitor  $C_{in}$ . The main difference is that the charger is used now very differently when in battery mode – compared to today's circuit. The added capacitor  $C_{in}$  becomes an energy storage component for this operation off the battery, and the total system power is below the capacity of the battery, and the system voltage is at high level (well above 5.4V for a 2S system and 2.5V for a 1S system). It is expected that the capacitor will be charged to 20V, a normal voltage of an ultrabook adapter, and a spec'd voltage of a Type C adapter.

**Figure 238. Buck-Boost Charger Implementation with Active  $V_{min}$  Protection**



When the system starts drawing sufficiently high power for sufficiently long time, the charger will compensate some of that draw by discharging the storage capacitor  $C_{in}$ , and supplementing the battery, and protecting the system voltage from drooping below the minimum voltage level (5.4 - 5.6V for a 2S system and 2.5V for a 1S system). It will also assert a PROCHOT# signal to throttle the SOC power. After PROCHOT# is asserted, the system must be guaranteed to be in the low power mode for sufficient amount of time to recharge the capacitor  $C_{in}$  (~1-2ms).

A charger that explicitly supports active Vmin protection must be used to enable this feature. The changes are mostly transparent to the designer and handled internally by the charger, with the exception of the additional capacitor  $C_{in}$  that plays a crucial role of the energy storage component. The capacitance proposed for the charger input decoupling strongly depends on the amount of time needed to supplement the battery and the amount of power which must be delivered. The expected value of this decoupling is lower than 50uF (effective value) for Y and U skus.

Active minimum voltage protection works in conjunction with fast PROCHOT# to allow system power to temporarily exceed what can be provided by battery alone, since the charger input capacitors on the unused adapter side provide the “reserve” power while fast PROCHOT# works to reduce processor power to a sustainable level until the charger input capacitors can be re-charged again. Because processor PL4 can now be set higher with these technologies implemented, the system can maintain better performance down to an even lower battery state of charge.

## 10.9 Battery and Fuel Gauging System

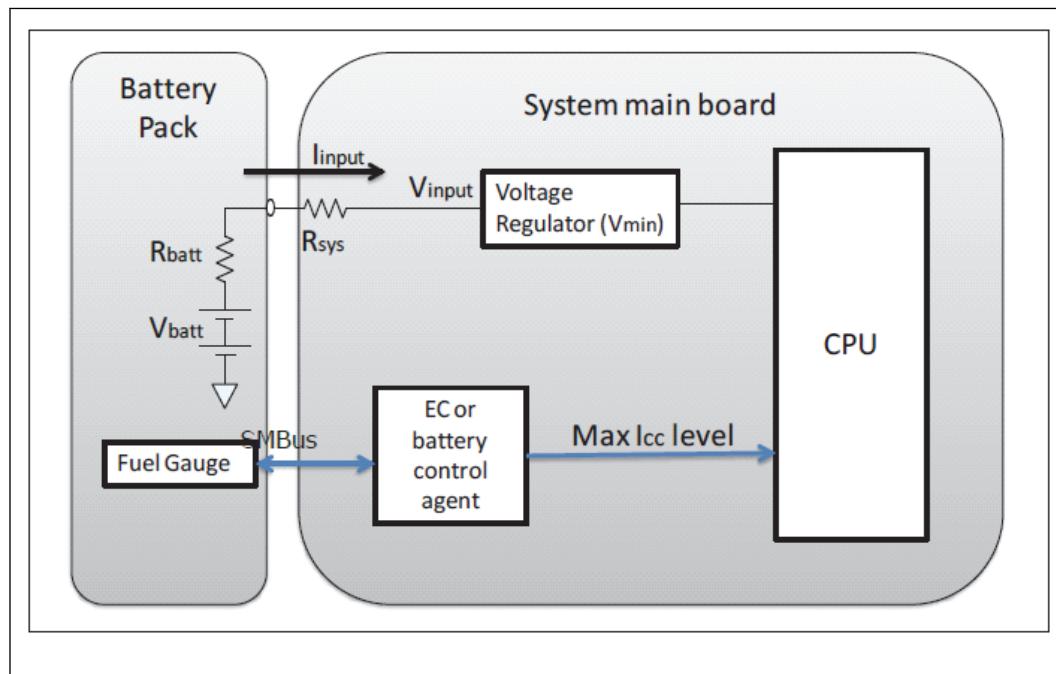
This section suggests system architecture for the UP3-Line battery and fuel gauging systems. [Dynamic Battery Power Technology](#) on page 422 provides information on how Turbo can be performed during discharge, given a two series Li pack configuration, providing for maximum performance.

We have adopted a cost / functionality strategy for UP3 -line. We refer the market being divided into three segments (shown below) which can be identified by differences in their battery and fuel gauging system.

1. **Volume Segment:** Battery and fuel gauging system designed to meet nominal battery runtime at nominal cost targets. Fuel gauging system provides nominal accuracy. Approaching full SoC performance.
2. **Premium Segment:** Battery and fuel gauging system designed to meet maximum battery life. Fuel gauging system provides best accuracy, and supports Dynamic Battery Power Technology. Full SoC performance.
3. **Value Segment:** Reduced battery life to meet cost target. Fuel gauging system may sacrifice accuracy to save cost. Nominal SoC performance.

### 10.9.1 Dynamic Battery Power Technology

[Figure 239](#) on page 423 below shows the top level architecture of Intel DBPT version 3(Dynamic Battery Power Technology). The input voltage of system regulator,  $V_{input}$ , is lower than the open circuit voltage of battery cells,  $V_{batt}$ . The voltage drop depends on the load current,  $I_{input}$ , and the total parasitic resistance from cells to regulator,  $R_{batt}$  and  $R_{sys}$ .

**Figure 239. DBPT Top Level Block Diagram**

Where  $R_{batt}$  includes both cell resistance and parasitic resistance due to the cell interconnect, sense resistor, FET, fuse, connector of battery pack.  $R_{sys}$  includes the resistance of power/ground metal, sense resistor, FET, and other parasitic resistance on the system main board.

In order to prevent  $V_{input}$  from violating the required minimum system input voltage,  $V_{min}$ ,  $I_{input}$  has to be adjusted according to the level of  $V_{batt}$  as the battery is discharged, as the impedance of the battery changes with state of charge, temperature, and age.

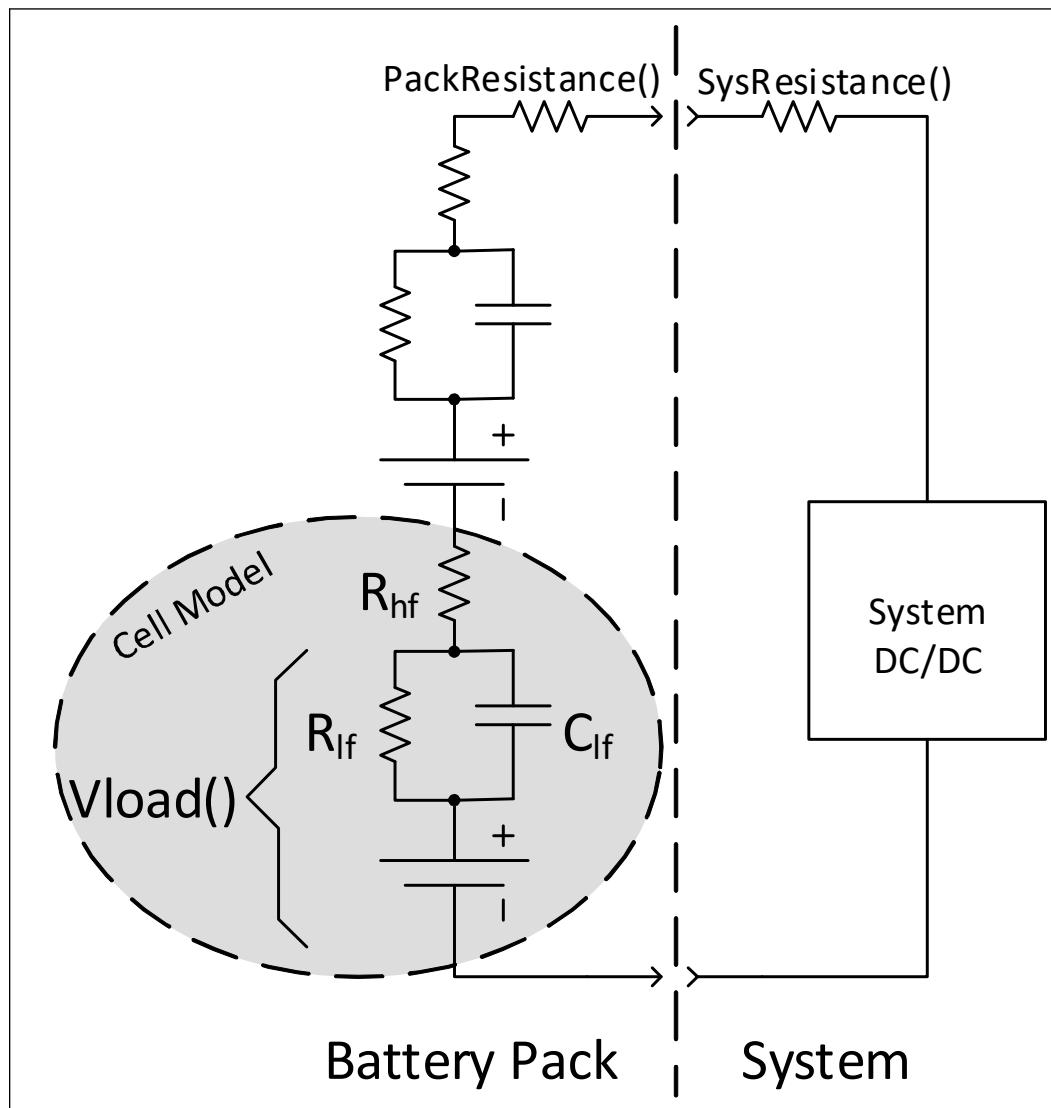
DBPT adds commands to the SMBus command set, so that the fuel gauge reports the maximum power the pack can support for a Turbo pulse. The pack takes into account,  $R_{sys}$ ,  $R_{batt}$ , and  $V_{min}$  when reporting what maximum power the pack can support. The system is then able to implement an algorithm so that the combination of SoC and other power sources stay within this allowed power envelope, so that an under-voltage condition does not occur.

There are three versions of DBPT.

1. The first version defines an SMBus command `MaxPeakPower()` that reports the ability of a battery pack to deliver power for up to 10ms. This is useful for setting the maximum PL4 value for the SoC, while making sure the battery voltage droop, combined with losses between the cells and voltage regulator are allowed for.
2. The DBPT version 2 implements all the features of DBPT, and adds the additional SMBus command `SusPeakPower()` which reports the ability of a battery pack to deliver power for up to 10s. This is useful for setting the maximum PL2 value for the SoC, while again allowing for voltage droop and power loss between the battery and voltage regulator.
3. The DBPT v3 was designed to assist the Pmax framework for the platform, and is targeting the system with 2s batteries.

As processors Turbo, there is a need to support higher power levels for short duration power events. To assist in supporting these power spikes for a short duration, the following model allows for determining the pack's behavior during these events, so that the system can determine what additional power it can get from the motherboard capacitance, AC adapters, etc. The model we have chosen is commonly used to model the behavior of the cells, and is shown in Figure below .

**Figure 240. Cell Model and Battery System Diagram**



The model of a single cell is shown within the greyed circle. The model consists of an internal cell voltage, which is closely tied to the state of charge of the cell. The low frequency resistance and capacitance,  $R_{if}$  and  $C_{if}$  respectively, have a very long time constant and model the behavior the cells shows to take 10's of minutes to settle to a final terminal voltage. The final component of the model is the high frequency resistance of the cell  $R_{hf}$ .

The first quantity from the model that version 3 of Dynamic Battery Power Technology utilizes is the loaded voltage `Vload()`. As the time constants of  $R_{lf}$  and  $C_{lf}$  are so long, the value for `Vload()` would be the voltage shown at the cell terminals, immediately after providing power for minutes, and then having all power consumption stopped. The voltage would be that observed about one ms after all current draw stops. This value is scaled appropriately for the number of cells in the pack, and reported via the `Vload()` command.

The other command added for DBPTv3 is `RhfEffective()`. This command gives the effective value of the impedance shown for a high frequency pulse. So this would consist of  $R_{hf}$  in the cell model, scaled appropriately for the number of cells in the pack, and includes other impedances such as `PackResistance()` and `SysResistance()`.

Together these values can be used to set a threshold voltage for a `PROCHOT#`, so that higher values of `PL4` can be supported for the system.

For further information on DBPT, refer to Intel Dynamic Battery Power Technology v3.

Without DBPT, the pack voltage must be chosen so that under load the pack voltage cannot fall below  $V_{min}$ . Ways to achieve this are to choose cell counts of 3 or more series Li cells. An alternative is to allow Turbo events on discharge, only to a predetermined critical threshold based on state of charge of the pack. The issue with this approach is that the impedance of the battery changes based on age and temperature, and the solution involves reducing SoC performance in an overly conservative way. DBPT allows for the SoC to perform optimally, at any given battery impedance.

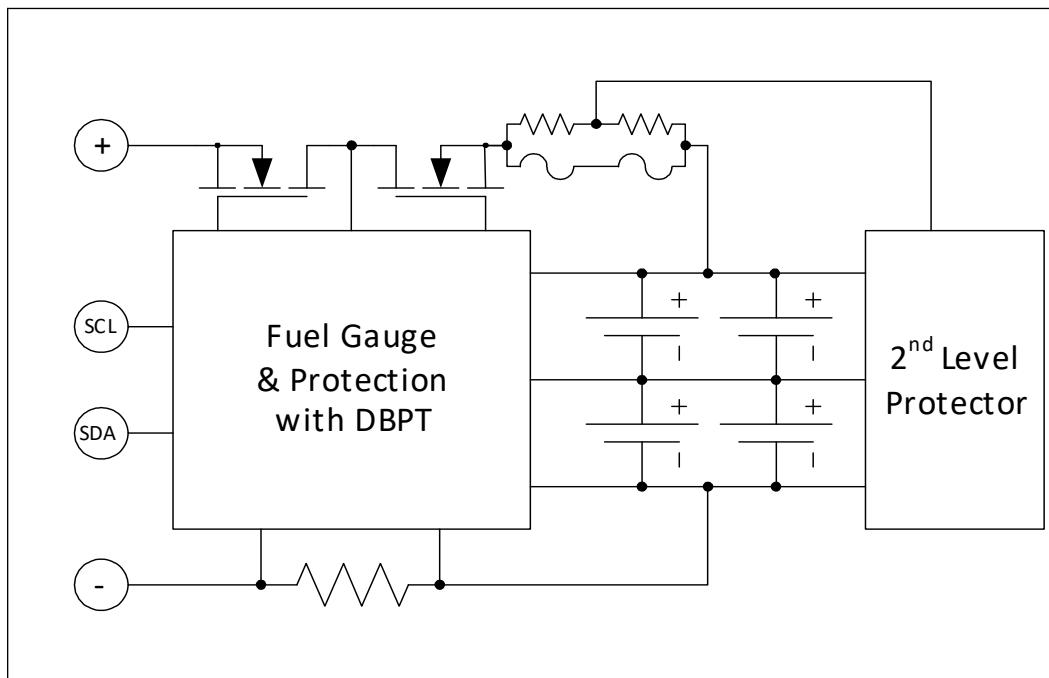
## 10.9.2 Fuel Gauging

By choosing between the following fuel gauging types, it is possible to tailor the fuel gauging solution cost, by trading off functionality. The following choices of fuel gauging solution are ordered below, starting with the most accurate, highest featured. As the list continues the features are reduced, along with the cost.

### In-Pack SMBus Fuel Gauge with DBPT

This solution for in-pack fuel gauging which supports DBPT provides for greatest runtime by providing the greatest fuel gauging accuracy. This solution also provides the greatest performance, as it allows for Turbo operation over the entire discharge cycle. Solutions which provide support for 2-4 series connected Li based cells are present in the market, from the two premier fuel gauging suppliers.

**Figure 241. Block Diagram of In-Pack Fuel Gauge with DBPT**



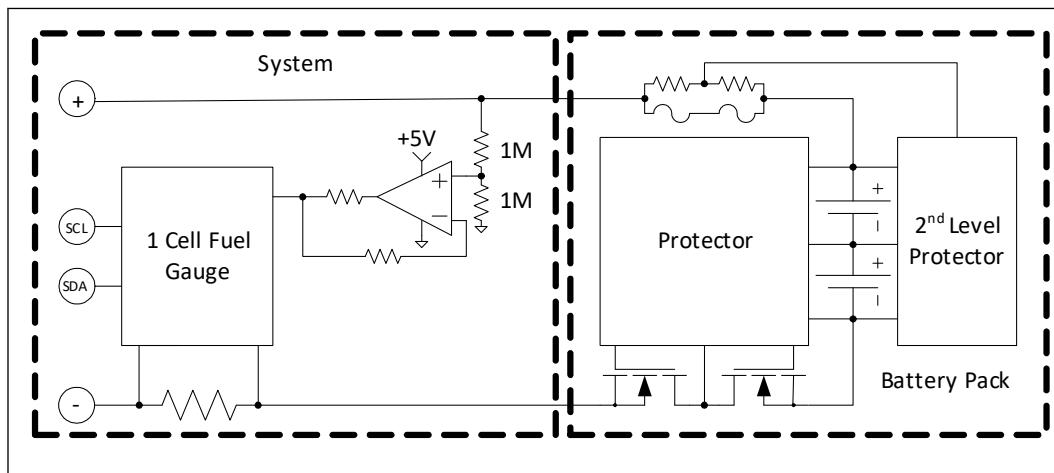
#### In-Pack SMBus Fuel Gauge without DBPT

This solution for in-pack fuel gauging provides for greatest runtime by providing the greatest fuel gauging accuracy. As this solution lacks support for DBPT, this solution is well suited to configurations of 3-4 series connected Li based cells, which support Turbo during discharge. With the higher cell count, typically the dropout concerns that might impact a two series configuration are not present. This solution is also a viable choice for a Li two series system, which will not Turbo during discharge. The block diagram of this system is identical to the In-pack SMBus Fuel Gauge with DBPT, as the only change is a fuel gauge that lacks the DBPT support, typically available at a lower price point.

#### In-system Fuel Gauge without DBPT

This solution for In-system fuel gauging provides for adequate fuel gauging accuracy. This solution also foregoes support for DBPT. The solution utilizes the selection of fuel gauging parts aimed at the cost competitive one cell fuel gauging market. As the SoC solutions require 5V rails, this solution uses an Op-Amp to divide the pack voltage of a 2 series Li pack configuration in half, and supply this precision divided voltage to the fuel gauge solution designed to handle one series cell. A typical block diagram of such a system is shown below.

**Figure 242. Block Diagram of 1S Fuel Gauge with 2S Pack**



#### NOTE

In such a system the Op-Amp and the divider resistors should be chosen to provide a very accurate division ratio, as inaccuracy in this division will directly affect fuel gauging accuracy. This means selection of an Op-Amp with a very low input offset voltage. In addition a matched set of divider resistors, or high precision resistors should be evaluated for their effect upon accuracy. Note that the Op-Amp will not be required to swing to the power or ground rails if powered by a 5V rail, so cost can be saved by choosing a low power, low input offset amplifier, which does not provide rail to rail output swing. The bandwidth of the amplifier is of some concern, but a bandwidth of 200kHz should be adequate to give good results. It is suggested to consult the fuel gauge manufacturer to determine what bandwidth their gauging solution requires.

In Windows\* solutions, a reporting of current is required by the operating system, so be sure to choose a single cell gauging solution which reports current for such systems. Other operating systems may not require reporting of current. Single cell gauging solutions which monitor only voltage, can provide a bit lower price point while typically giving up a couple percent of accuracy.

### 10.9.3 Battery Pack Size and Configuration

The battery pack is typically size to meet goals for runtime and peak power. In order to achieve the highest performance for the processor, please specify the battery based on guidelines for power capability of the pack from the Table below.

**Table 225. Battery Discharge Capability Recommendations**

<b>Recommended Peak Duration</b>	<b>10ms</b>	<b>100 sec</b>	<b>Constant Discharge</b>
Recommended Max Discharging Power Level if $P_{SYS}$ is not used	$PL4 + P_{ROP\_MAX}$	$PL2 + P_{ROP\_MAX}$	$PL1 + P_{ROP\_MAX}$
Recommended Max Discharging Power Level if $P_{SYS}$ is used	$PL4 + P_{ROP\_MAX}$	$P_{SYS}PL2$	$P_{SYS}PL1$
Peak Duration with PL3/ $P_{SYS}PL3$	configurable down to 2ms <sup>1</sup>	NA	NA
Duty Cycle with PL3/ $P_{SYS}PL3$	configurable down to 4%	NA	NA

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**NOTE**

Refer to Tiger Lake Platform Turbo and Thermal Power Management Guide for Intel® Core™ Based Processors User Guide (#607378).

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Once the power capabilities to support a performance level are decided, a choice of pack configuration remains.

The choice is often between two series and three series configurations of Li based cells. Two series configurations result in higher currents, when compared to a three series configuration, for equivalent system power consumption. This would normally tend toward choosing the higher voltage solution, as power losses increase with the square of the current. The other factor is that with a lower voltage range, the DC/DC converter can typically be optimized for a better overall efficiency, which tends to favor the two series solution. Another factor to consider, is that a three series configuration will likely not have issues with reaching low voltages during Turbo events, where a two series configuration may reach low voltages under load, and require support of DBPT to manage this. For the lower power consumption systems in this line, an NVDC charger configured for two series cells seems to achieve the greatest system efficiency. For higher power consumption systems in this line, a three series cell configuration will achieve the greatest system efficiency. The tradeoff between the two approaches can be gauged, by looking at the  $I^2R$  losses throughout the power system in the two approaches.

A trade-off that is often overlooked is that of fuel gauging accuracy, and pack cost. If we think of battery pack cost in terms of \$/Wh (dollars per watt-hour), then any inaccuracy in the fuel gauge can be expressed as a cost in dollars, for a given pack size. For example, given a 50Wh pack, and a cell cost of \$0.40/Wh, the cost of cells would be \$20. When choosing between a 6% accurate fuel gauge, and a 1% accurate fuel gauge, it makes sense to look at the cost of that potentially lost capacity, when looking at the price difference between the gauges. With a difference of 5% in accuracy, and a cell cost of \$20, the 1% accurate gauge could be \$1 less expensive ( $\$20 * 5\% = \$1$ ), and still offer better performance. The 6% accurate gauge would need to increase the cell cost by \$1 to allow for the potentially decreased runtime due to gauge performance. In addition the more accurate gauge will offer a solution that is smaller and lighter, as the pack capacity that is purchased is fully used, rather than just sized up to allow for fuel gauge inaccuracy.

## 10.9.4 Additional Power Savings with Respect to VCCST Rail

FIT tool needs to be configured correctly to power gates and notifying Pcode on these power gates. This will impact power saving options and may impact platform behavior.

**Table 226. FIT Tool and CPU Straps**

VCCSRF_OC (VCCPLL-OC) PG Present	No	The setting determines if VCCSRF_OC PG is present on the platform
VCCST PG Present	No	The setting determines if VCCST PG is present on the platform
VCCSTG PG Present	No	The setting determines if VCCSTG PG is present on the platform

In case there is PG (Power Gate) to one of the power rails, go to Intel® ME Tool, right click power rail and select Yes on PG present.

Example, if the platform has a power gate only for VCCST and VCCSTG, select Yes for VCCST and VCCSTG and No for VCCSRF\_OC

Those CPU straps will be used by Pcode and customer need to configure the value in Intel® ME Tool (FIT Tool), not configuring the right value in the FIT Tool may lead to power impact and functional impact.

## 10.10 Dynamic Fast Charging Technology, DFCT

Fast charging is becoming a feature sought out by many customers. There are several challenges to providing fast charging within a system.

First is the potential impact to the size of the AC Adapter needed to provide this fast charge capability. To charge faster requires more power during at least a portion of the charge cycle. If the requirement is to provide faster charging while the system is in a lightly loaded or off state, it may be possible to fast charge without increasing the AC Adapter wattage. If fast charge is required under all power states, then more AC adapter wattage is likely required.

The cells in the battery must be capable of fast charging. There is increased power dissipation in the charger circuitry while fast charging, so either additional thermal handling capability must be present, or the charge rate must be controlled based upon the thermal environment.

There are several vendors that provide algorithms designed to fast charge "standard" cells, while promising to preserve the cycle life. Previously the method used to report and control fast charging was proprietary to each vendor, which made implementation of solutions complex, and limits reuse when moving between vendors.

DFCT addresses many of these concerns. It provides a standardized set of SMBus commands that are used to define the fast charge. The algorithm resides within the battery pack or fuel gauge in the system, as this subsystem has the best understanding of the cells. Allowing for multiple vendors with the same commands stimulates innovation, and allows for moving between different vendors with various algorithms, without needing new code for the embedded controller. DFCT can be used with Dynamic Platform Thermal Framework, DPTF, to provide fast charging in a way that allows control of the thermal issues within the system.

For further information on DFCT, refer to the following documents:

- Intel Dynamic Fast Charging Technology, SMBus Implementation Specification #564466
- Implementing Fast Charging with Intel Dynamic Fast Charging Technology (Intel DFCT) #564842.

## 10.11 Deep Sx Implementation Design Guidelines

This section describes how to implement Deep Sx feature on the Tiger Lake platform. Deep S3 is no longer supported on Tiger Lake platform. Deep S4/S5 states are supported if battery is low and AMT is **not** provisioned.

### 10.11.1 Hardware Design Changes Required

Tiger Lake processor Platform entry into Deep S4/S5, the Intel ME is in M-Off State. The system memory VR can be turned off in S4 by driving its enable pin low, SLP\_S4# signal can be used directly to control the enable pin on the system memory VR. The control of the enable pin does not need to be off-loaded to platform logic or the EC anymore.

#### SUSWARN# and SUSPWRDNACK Usage Exclusivity

SUSWARN# (used by Deep Sx) share the same physical pin with SUSPWRDNACK on the Tiger Lake processor, and their use are mutually exclusive. The use of this pin as either SUSPWRDNACK or SUSWARN# will be determined by Deep Sx policy setting. SUSPWRDNACK may be used to indicate to the EC that all Tiger Lake processor power rails, with the exception of RTC well, can be turned off. This usage model is mutually exclusive with Deep Sx. When Deep Sx is enabled, the Tiger Lake processor will drive this pin as SUSWARN# to indicate to the platform that SUS well (but not DSW) can be turned off.

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#### NOTE

Deep Sx feature and use of SUSPWRDNACK are mutually exclusive. A platform either supports Deep Sx (in which case the Tiger Lake processor will drive the pin as SUSWARN#) or the platform does not support Deep Sx and may support SUSPWRDNACK. Selection between the two modes is a static configuration. Refer Tiger Lake Processor External Design Specification (#608190) for complete supported policy combinations.

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### 10.11.2 Co-Existence Requirements

If platform supports Intel® Rapid Start and Intel® Smart Connect technologies together with Deep Sx, platform EC needs to be powered up throughout Deep S4/5 states.

## 10.12 Platform Power Sequencing Specification

This section provides the following information:

- Platform Power Sequence requirements for the Tiger Lake platforms
- Platform Voltage Rails Status in the different S-States/M-States

- Voltage Rail Sequencing Requirements

The block diagrams and timing diagrams in this document are references to help demonstrate the timing requirements for the platform, and the actual timing specifications that need to be met by the system are defined in [Power Sequencing Timing Requirements](#) on page 449. Depending on the system architecture, all applicable timings need to be met to ensure proper functionality of the CPU/PCH.

## 10.12.1 Key Changes to Tiger Lake Sequence Architecture

### **RSMRST# and DSW\_PWROK Power Down Design Requirement**

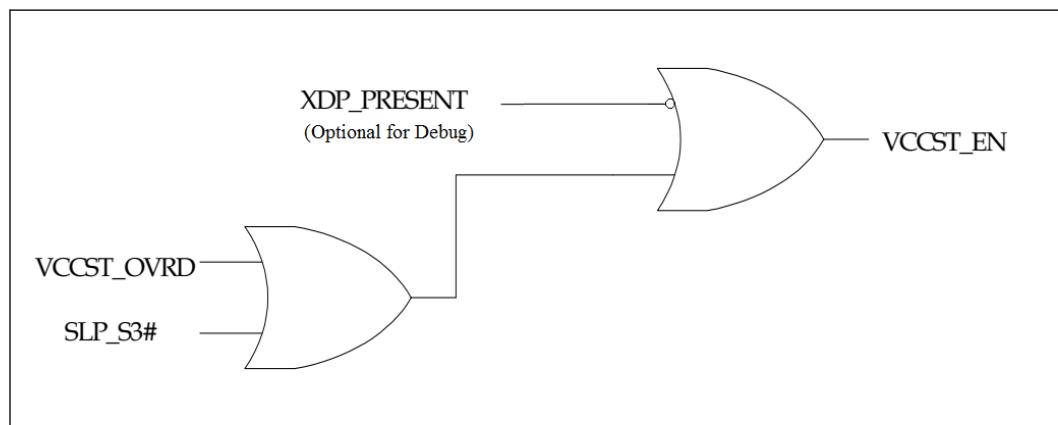
DSx and Non-DSx platforms are required to take RSMRST# and DSW\_PWROK low at the same time when not entering a DSx state. Taking RSMRST low without taking DSW\_PWROK low is not permitted when not entering DSx states. Refer [DSW/PRIM Rail Architecture in DSx and Non-DSx Designs](#) on page 432 and [RSMRST#/DSW\\_PWROK Special Requirements](#) on page 461

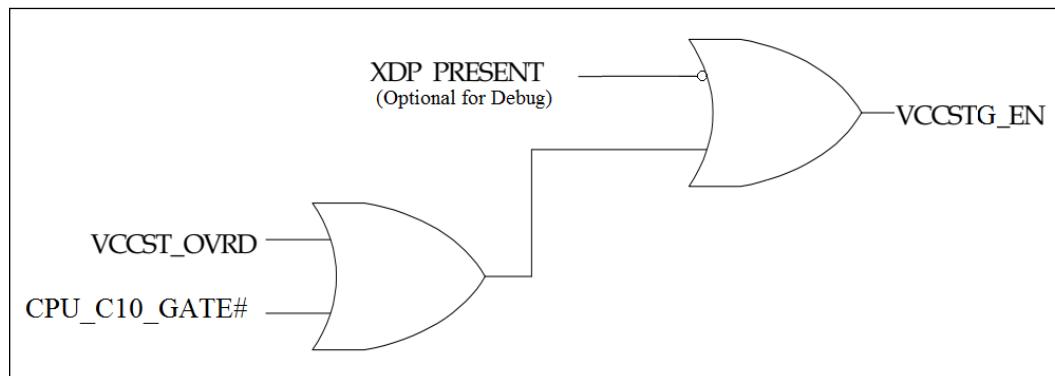
### **Design Consideration for VCCST Rail Enable Logic**

VCCST can be turned OFF even if VCCIN\_AUX is ON.

Refer [Additional Power Savings with Respect to VCCST Rail](#) on page 429 for details around VCCST rail state requirements.

**Figure 243. VCCST Enable Logic**



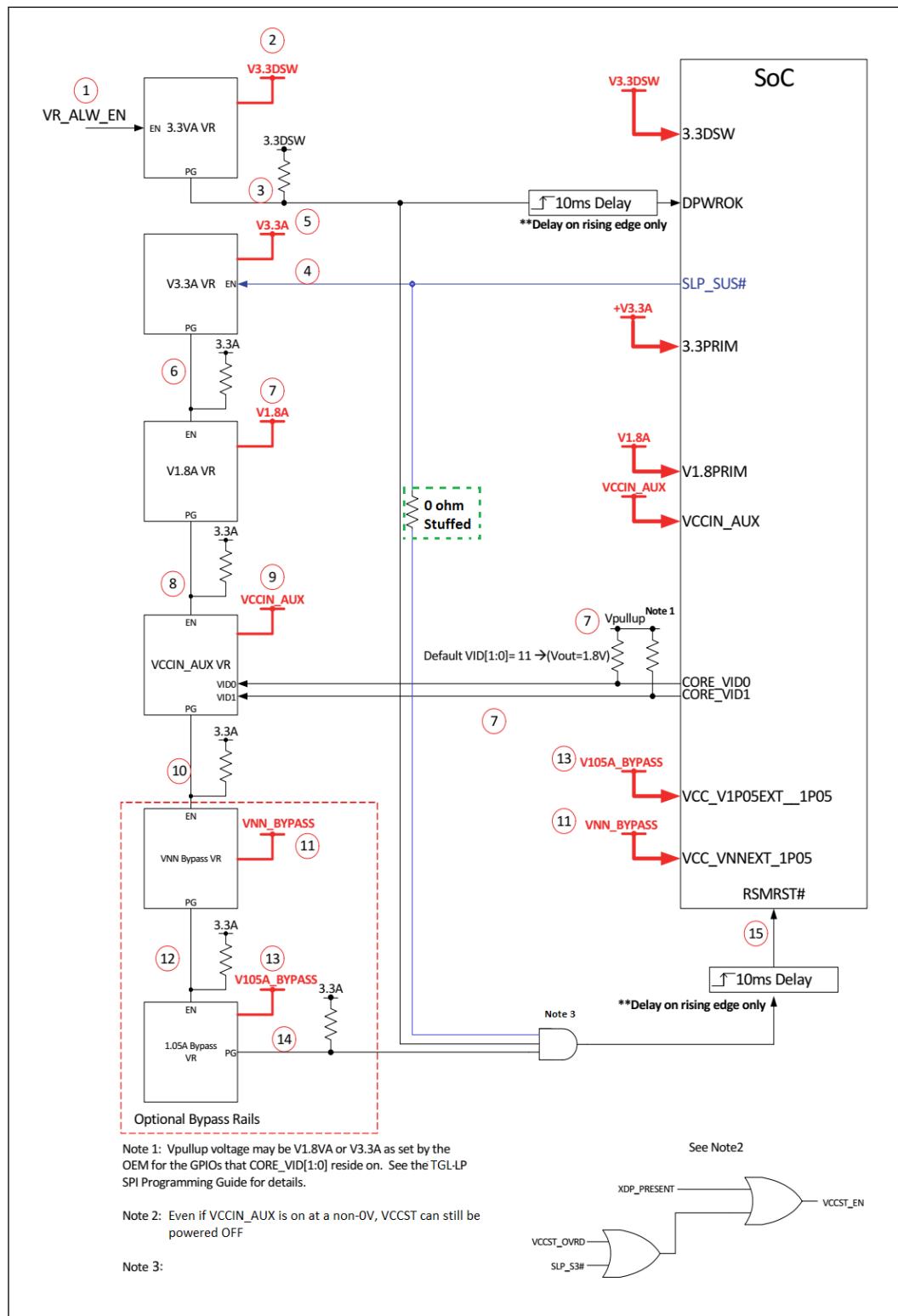
**Figure 244. VCCSTG Enable Logic****DSW/PRIM Rail Architecture in DSx and Non-DSx Designs**

DSx and Non-DSx designs are similar in term of power rail architecture, rail, control, and power good signaling.

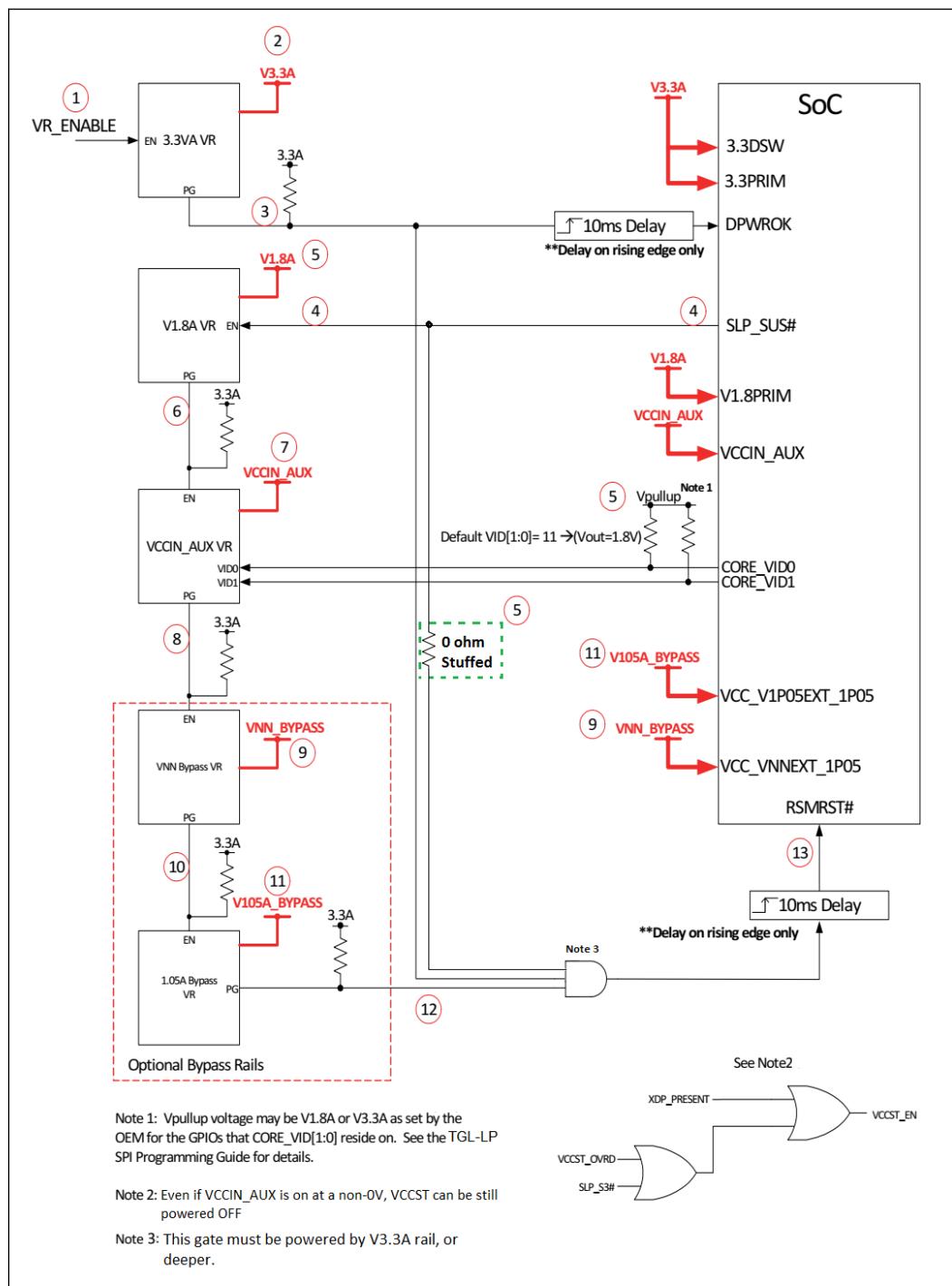
- SLP\_SUS# controls part of all of the PRIM rail enabling in both systems
- DSW\_PWROK and RSMRST# are always separate power good signals

Refer the Figure below and [Figure 246](#) on page 434 for details.

Figure 245. Tiger Lake DSx System Architecture Block Diagram



**Figure 246. Tiger Lake Non-DSx System Architecture Block Diagram**



## 10.12.2 PCH\_PWROK, SYS\_PWROK and Other PWRGD Signal Generation

The power sequencing consists of multiple stages of power state transitions. During each stage, different VRs will be turned on through various control signals from the processor such as the SLP\_SUS#, SLP\_S5#, SLP\_S4#, SLP\_S3#, SLP\_S0# and CPU\_C10\_GATE#. In response, the platform will ramp the required voltage rails in the required order and then asserted the various powergood signals required by the processor, and other platform components, after the necessarily timing requirements have been met. The below figure shows a high-level representative control signal and the powergood logic diagram for generating the PCH\_PWROK and SYS\_PWROK signals. This figure shows the recommended power-on sequencing flow steps from SLP\_S4# de-assertion until PLTRST# de-assertion for the Tiger Lake platform.

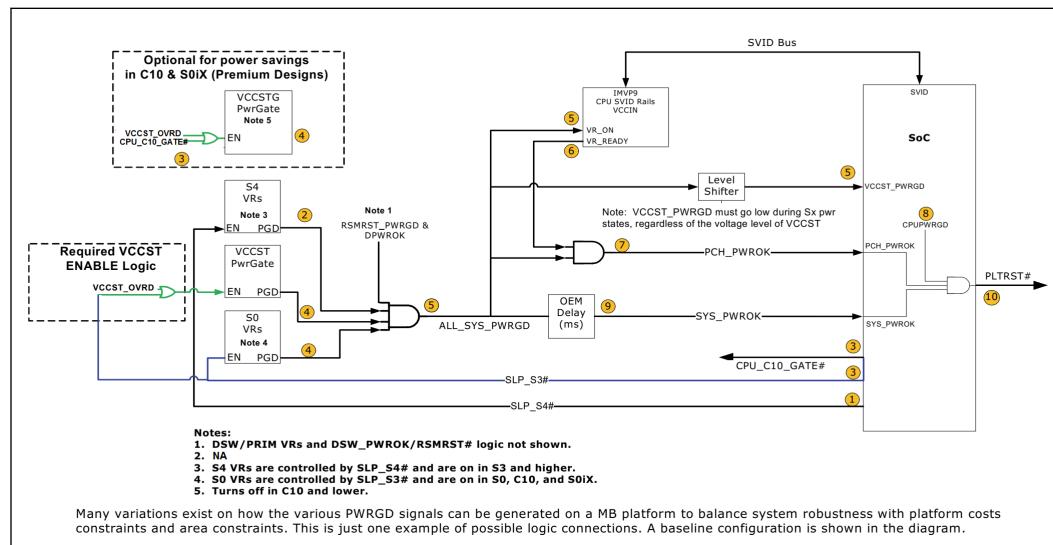
During G3/DSx, S5 to S0 transitions, the platform will need to generate the DSW\_PWROK and RSMRST# signals. In this phase of the power up sequence, the DSW and Primary power well voltage rails are ramped to the processor.

During S5 to S0 and DSx to S0 transitions, the platform will need to generate the VCCST\_PWRGD, PCH\_PWROK and SYS\_PWROK signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up.

The PCH\_PWROK signal is expected to be asserted by the platform to indicate to the processor that all required CPU voltage rails are up and stable, and that the processor may continue the final boot sequence leading up to PLTRST# de-assertion, such as starting to turn on clocks and executing other internal pre-reset activities.

SYS\_PWROK is expected to be asserted by the platform to indicate that the system and all of its non-CPU components are ready for PLTRST# de-assertion. During power state transition to S0, the SYS\_PWROK signal is the final platform controlled hardware gate before PLTRST# de-assertion. Platform designers may optimize when the SYS\_PWROK signal is asserted with respect to the PCH\_PWROK signal to help optimize overall boot latency, depending on system and component timing requirements.

**Figure 247. Premium PWROK Generation Flow Diagram**



### 10.12.3 Sequencing Interface Signals List and Power Rails

**Table 227. Tiger Lake Platform Sequencing Signals List**

Name	Source	Destination	Description
RTCRST#	Platform	PCH	When asserted, this signal resets the register bits in the RTC well.
SRTCST#	Platform	PCH	This signal resets the manageability register bits in the RTC well when the RTC battery is removed
DSW_PWROK	Platform	PCH	Indication to the PCH that VCCDSW_3p3V rail is stable. This signal must be asserted no earlier than 10ms after the DSW power wells are valid. <i>Note:</i> In TGL generation platforms DSW_PWROK and RSMRST# are always separate power ok signals. Refer <a href="#">DSW/PRIM Rail Architecture in DSx and Non-DSx Designs</a> on page 432
RSMRST#	Platform	PCH	This signal is used for resetting the Primary power plane logic. This signal must be asserted for at least 10 ms after the Primary power wells are valid. When de-asserted, this signal is an indication that the power wells are stable. <i>Note:</i> there are special requirements around RSMRST# assertion when NOT entering DSx power states. Refer <a href="#">RSMRST#/DSW_PWROK Special Requirements</a> on page 461 for details.
SUSWARN#	PCH	Platform	This function is only applicable to platforms supporting Deep Sleep Wells  This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (using SLP_SUS#). The EC/motherboard control logic must observe edges on this pin, preparing for Primary well power loss on a falling edge and preparing for Prim well related activity (host/Intel ME wakes and runtime events) on a rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#. <i>Note:</i> In eSPI mode this signal is a virtual wire on the eSPI interface and the hard wire signal from PCH is disabled. Refer eSPI Compatibility Specification (# 508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.
SUSPWRDNACK	PCH	Platform	This function is only applicable to platforms NOT supporting Deep Sleep States.  Asserted high by PCH when it does not require Primary well to be powered. No longer requires a 10-K pull-up to VCCSUS (3.3 V). This signal is required to be connected to EC for platforms with or without M3 support that do not support Deep Sx. This signal gives an added flexibility for the EC to turn OFF the Prim Rails when not needed by the PCH. SUSPWRDNACK can be High/Low in Sx/Moff based on the ME power policy selected. On Platforms that do not support both Deep Sx and M3 EC must keep Prim rails powered ON If, 1. SUSPWRDNACK is de-asserted low Else, EC has the option to turn-off the Prim rails On Platforms that do not support Deep Sx, but supports M3 EC must keep Prim rails powered ON If,

*continued...*

Name	Source	Destination	Description
			<p>1. SUSPWRDNACK is de-asserted low OR      2. SLP_A# is de-asserted high OR      3. It's the first 200 ms after Prim rails power has been applied.      Else,      EC has the option to turn-off the Prim rails.</p> <p><b>Notes:</b> 1. The polarity of SUSPWRDNACK is the opposite of SUS_WARN#. SUS_WARN# will assert low when Primary well power will be turning off, however SUSPWRDNACK will assert high when Primary well power can be turned off.      2. In eSPI mode this signal is a virtual wire on the eSPI interface and the hard wire signal from PCH is disabled. Refer eSPI Compatibility Specification (# 508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.</p>
SUSCLK	PCH	Platform	This clock is an output of the RTC generator circuit for use by other chips for refresh clock. SUSCLK is powered from DSW.
ACPRESENT	Platform	PCH	Used on mobile systems to determine presence of AC power or battery power. In addition to previous Intel® ME to EC communication, PCH uses this signal to implement Deep Sx policies. For example, the platform may be configured to enter Deep Sx only on battery and not AC.
SUS_ACK#	Platform	PCH	<p>For platform supporting Deep Sx state, this signal is driven from the platform EC to PCH to acknowledge that EC has received the SUSWARN# signals and it is preparing to go into DeepSx mode.</p> <p>For non-DSW platforms, this signal can be left unconnected. Due to the internal pull-up on this signal it will be pulled high in order for the boot sequence to proceed. It does not matter if this assertion happens before or after SUSPWRDNACK assertion.</p> <p><b>Note:</b> In eSPI mode this signal is a virtual wire on the eSPI interface and the hard wire signal from PCH is disabled. Refer eSPI Compatibility Specification (# 508740) and Tiger Lake PCH-LP External Design Specification, Volume 1 for details.</p>
SLP_SUS#	PCH	Platform	<p>For platforms supporting Deep Sx state, a low on this signal indicates that PCH is in Deep Sx state and that EC/platform logic does not need to keep the Primary Rails ON.</p> <p>If high means EC must keep Primary rails ON.</p> <p>Unlike previous generation platforms, in TGL SLP_SUS# is used in both DSx and Non-DSx platforms. Refer <a href="#">DSW/PRIM Rail Architecture in DSx and Non-DSx Designs</a> on page 432 for details.</p> <p><b>Note:</b> In eSPI mode this signal is a hard wire only and not a virtual wire.</p>
PWRBTN#	Platform	PCH	Signal driven from EC to PCH indicating a system request to go into Sleep State OR if the system is already in the Sleep State then it will cause a wake event.
SLP_A#	PCH	Platform	<p>This signal is used to control power to devices on the platform in conjunction with the Intel® ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timings as SLP_S3#.</p> <p>On TGL UP3 Platform, SLP_A#/GPD6 is a physical pin (package ball DR41)</p> <p>On TGL UP4 Platform, SLP_A# functionality is implemented on GPP_E4 /SATA_DEVSLP0 pin (package ball DG8). This pin is dedicated for SLP_A# functionality and controlled / owned by the Intel CSME. Therefore, GPP_E4 or SATA_DEVSLP0 function is not available on this pin on TGL UP4 Platform. This pin will behave as SLP_A# once the CSME FW loaded. Prior to that point, this pin will be undriven as it defaults to GPI.</p>

*continued...*

Name	Source	Destination	Description
			<p><i>Note:</i> In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (# 508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.</p>
SLP_LAN#	PCH	Platform	<p>LAN Sub-System Sleep Control. Controls power to the LAN PHY. When "low", indicates that power can be shut off to the external wired LAN (GbE) PHY.</p> <p><i>Note:</i> In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.</p>
SLP_S5#	PCH	Platform	<p>This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S5 (Soft Off) states.</p> <p><i>Note:</i> In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.</p>
SLP_S4#	PCH	Platform	<p>S4 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S4 (Suspend to Disk) and lower (S5).</p> <p><i>Note:</i> In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.</p>
SLP_S3#	PCH	Platform	<p>S3 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S3 (Suspend to RAM) and lower (S4, S5).</p> <p><i>Note:</i> In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details.</p>
CL_RST#	PCH	Platform	This signal connects to the Wireless LAN device supporting Intel® AMT.
VDDQ_PWRGD	Platform VR	Platform Logic	Indicates that the DRAM power supply is stable and within specification.
Platform S0 Rails	Platform	Processor/PC H	These are all the non-core platform rails.
RSMRST_PWRGD#	Platform	Platform	The signal represents power good for VCCPRIM rails and other S5 rails.
ALL_SYS_PWRGD	Platform	Platform	This signal represents the power good for all the rest of platform voltage rails.
IMVP VR_READY	Platform	Platform Logic/SoC	IMVP VR_READY is an active-high output that indicates that the IMVP9 start-up sequence is complete. Assertion of VR_READY indicates that the IMVP9 VR is ready to accept an SVID commands and is operating properly. Refer to the VR_READY definition in the IMVP9 spec for additional details.
PCH_PWROK	Platform	PCH	When asserted, PCH_PWROK indicates that all the main PCH Primary rails and all the CPU rails are up.
SYS_PWROK	Platform	PCH	Generic power good input to the PCH is driven and utilized in a platform-specific manner. Informs PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset (de-asserts PLT_RST# to the processor).

*continued...*

Name	Source	Destination	Description
			<p><b>Note:</b> PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. PCH does not monitor SYS_PWROK until after PCH_PWROK is asserted. SYS_PWROK may be tied to PCH_PWROK if the platform does not need the use of SYS_PWROK.</p>
DDR_RESET#	PCH	Processor	Controls reset to the memory subsystems (DDR4/LPDDR4)
PROCPWRGD	PCH	Processor	<p>Indicates that VCCST, VCCSTG, VCCIN (VCCIO, VCCSA), VDDQ power supplies and clocks are stable. This signal will be asserted only after PCH_PWROK assertion.</p> <p>VCCIO/VCCSA are FIVR based and are internal to SOC in UP3 and UP4 line.</p> <p>Also, in UP3 and UP4 line SOCs PROCPWRGD signal is internal to the package, but may be observable by designer for debug purposes.</p>
SUS_STAT#	PCH	Platform	<p>This signal is asserted by the PCH to indicate that the system will be entering a low power state soon. This can be monitored by device with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes.</p> <p><b>Note:</b> In eSPI mode this signal is a virtual wire on the eSPI interface and the hard wire signal from PCH is disabled. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification (# 576591) for details.</p>
PLTRST#	PCH	Processor	The PCH asserts PLTRST# to reset device on the platform (e.g., SIO, FWH, LAN etc.). Asserted during power-up and when S/W initiates a hard reset sequence through the Reset Control register.
SPI	PCH	Flash Device	<p><b>Serial Peripheral Interface</b> between PCH and BIOS Flash Device.</p> <p><b>Note:</b> In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification (# 576591) for details.</p>
SLP_WLAN#	PCH	WLAN	WLAN Sub-System Sleep Control: When SLP_WLAN# is asserted, power can be shut off to the external wireless LAN device. SLP_WLAN# will always be de-asserted in S0.
LAN_WAKE#	PHY	PCH	<p>Can be used by the LAN PHY as a wake signal.</p> <p><b>Note:</b> In eSPI mode this signal is also virtual wire on the eSPI interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification (# 576591) for details.</p>
ESPI_RESET#	PCH	Platform	Controls reset to eSPI
VCCST_PWRGD	Platform	Processor	Indication that the VCCSTG\VCCST\VDDQ power supplies are stable and within specification
VCCST_OVERRIDE	PCH	Platform/Processor	Signal that allows PCH to keep VCCST powered ON (in case VCCST is powered down) for Type C wake capability.
VCCST_PWRGD_TCS	PCH	Processor	Power good signal to Processor TCSS block for Type C wake capability.
DDR_VTT_CNTL	CPU	VTT VR	Enable signal for the DDR VTT VR
SLP_S0#	PCH	Platform	S0 Sleep Control. When PCH is idle and processor is in C10 state, this pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.

*continued...*

Name	Source	Destination	Description
			<i>Note:</i> In eSPI mode this signal is a hard wire only and not a virtual wire.
CPU_C10_GATE#	CPU	Platform	Power gating control to turn off VCCSTG in C10 and lower. <i>Note:</i> In eSPI mode this signal is a hard wire only and not a virtual wire.

**Table 228. Tiger Lake Power Sequence Related Power Rails**

	Name	Source	Destination	Description
Common	VCCRTC	Platform	PCH	2.0-3.3V +5% supplies for PCH RTC Well. This power is not expected to be shut off in any of the sleep states unless the RTC battery is removed or completely drained.
Common	VCCDSW_3P3	Platform	PCH	3.3-V supply for Deep Sx wells. If Deep Sx is not supported on the platform, tie to VCCPRIM_3p3
Common	VCC1P05_OUT_FET	PCH	Platform	FIVR output of PCH to platform 1.05V Power Gates (VCCST/VCCSTG)
Common	VCCPRIM_1P8/3P3 <sup>2</sup>	Platform	PCH	PCH I/O and Misc rails 1.8/3.3V (Primary Well)
	VCC_VNNEXT_1P05 VNN_BYP	Platform	PCH	Optional BYPASS rail for PCH Prime Core Well (760mV in S0ix and 1.05V in Sx states) or reduced power consumption in low power states
	VCC_V1P05EXT_1P05 V1P05 BYP	Platform	PCH	Optional BYPASS rail for PCH Primary Well (1.05V) for reduced power consumption in low power states
Common	VCCST	Platform	Processor	Sustain voltage for processor in Standby modes
Common	VCCSTG	Platform	Processor	Gated version of VCCST
Common	VPP	Platform	Memory	Memory power rail, voltage dependent on memory technology
Common	VDDQ	Platform	Processor	CPU Memory power rail, voltage dependent on memory technology
	VCCIN	Platform	Processor	Processor FIVR input power supply
	VCCIN_AUX	Platform	PCH	PCH FIVR input power supply

#### 10.12.4 Power States

**Table 229. System with M3 State Supported**

Rails	SKU's	S0/M0 <sup>3</sup>	C10 <sup>2</sup>	S0ix/M-off <sup>4</sup>	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3 <sup>1</sup>
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1P05	All	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P05EXT_1P05	All	ON	ON	ON	ON	ON	OFF	No Power

*continued...*
**No Deep S3 State**

Rails	SKU's	S0/M0 <sup>3</sup>	C10 <sup>2</sup>	S0ix/M-off <sup>4</sup>	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3 <sup>1</sup>
V3.3M <sup>5</sup>	All	ON	ON	OFF	ON <sup>10</sup>	OFF	OFF	No Power
V1.8M <sup>5</sup>	All	ON	ON	OFF	ON <sup>10</sup>	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	OFF <sup>6</sup>	OFF <sup>6</sup>	OFF	No Power
VCCSTG	All	ON	OFF <sup>2</sup>	OFF	OFF	OFF	OFF	No Power
VCC1P8A <sup>15</sup>	H	ON	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON <sup>11</sup>	OFF	OFF	OFF	No Power
VCCIN_AUX <sup>13</sup>	All	ON	ON	ON <sup>11</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF	No Power

- Notes:
1. The state of the system without RTC well powered can also be considered G3.
  2. VCCSTG can be turned off when the processor is in C10
  3. S0/M0 state includes all Package C-states from C0-C10
  4. Assume SLP\_S0# and CPU\_C10\_GATE# have asserted from the PCH
  5. V3.3M and V1.8M are platform rails used by external devices which ME operates during Sx/M3 states. These rails are not used directly by the CPU/PCH, and are not present on non-M3 supported systems
  6. VCCST and VCCSTG can remain powered during S4 and S5 power states for board cost optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Platform Debug and Test Hooks chapter for more details.
  7. NA
  8. NA
  9. VCCSTG is allowed to be ramped to 0V during S0 only when CPU\_C10\_GATE# is asserted. Specific exit latency targets are required when this feature is implemented. If VCCSTG power gating is not supported on the platform (shared with VCCST), VCCSTG is allowed to stay ON during S0ix states. Note that merging power rails may reduce power optimization opportunities on the platform.
  10. For no M3 support on external devices, V3.3M/V1.8M will be OFF in Sx/M3
  11. This supply is expected to be 0V during states where SLP\_S0# is asserted. It may be left on during this condition, but the SoC will not achieve its lowest power consumption. Specific power up latencies apply when exiting this state. Applicable to form factors with battery only (ie. AIO)Optional depending platform design; ON if AC is present
  12. NA
  13. Leakage on VCCIN\_AUX is expected behavior when CORE\_VID[1:0]=00; this leakage voltage may be as high as 1.15V during Sx and S0ix states.
  14. VCCIN\_AUX may be ON in these power states if required by the PCH.
  15. VCC1P8A of Processor rail can be either merged with VCCPRIM1P8 rail of PCH or enabled by CPU\_C10\_GATE# using a power switch. Power gating option is preferred since additional power saving in C10 state is possible. All timing diagrams are drawn under the assumption power gating for VCC1P8 is used.

## 10.12.5 Power Sequencing Timing Diagrams Legacy Signals

Table 230. Legend for Signals in Transition Waveforms

Color/Legend	Comments
Signal Names	Timing of these signals is set by PCH or processor
<b>Signal Names</b>	Timing of these signals should be met by the platform
Signal Names	Voltage rails or chip-to-chip buses
Grey Highlight	Indicates unstable state

Figure 248. Timing Diagram for G3 to S0 [Deep Sx Platform] - 1 OF 2

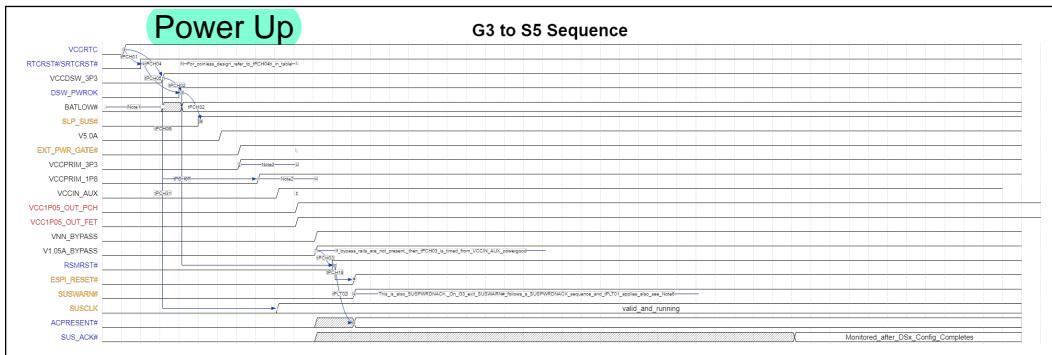
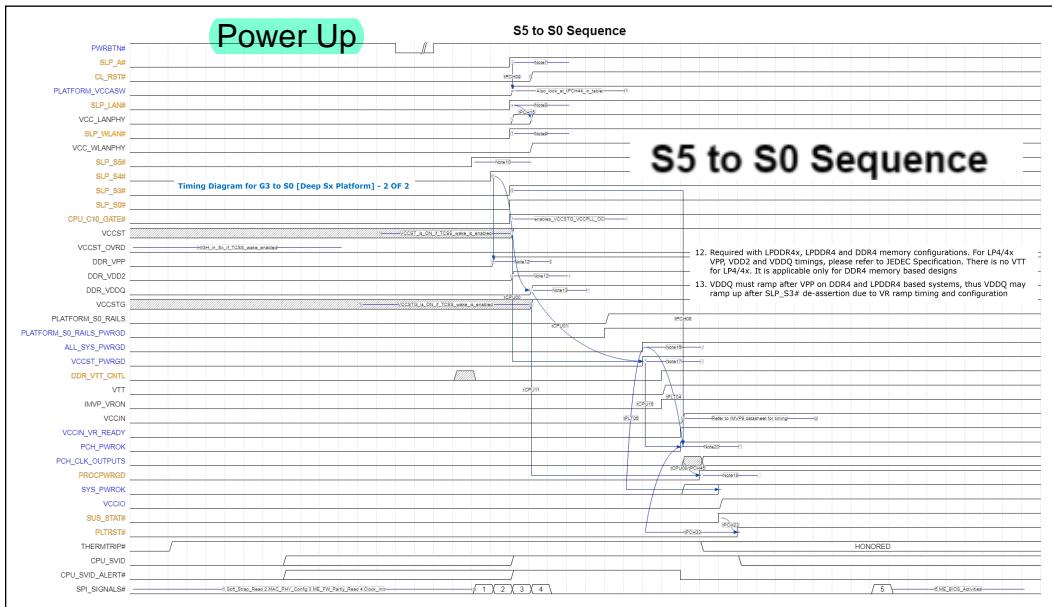


Figure 249. Timing Diagram for G3 to S0 [Deep Sx Platform] - 2 OF 2



**VCCSTPWGOOD\_TSS Topology**  
VCCSTPWGOOD\_TSS is a new input signal on the Tiger Lake processor that been asserted when the USB-C® Subsystem requires keeping VCCST supply on, even when entering S3-S5 states. If required, the VCCST signal level must always change before de-assertion of VCCST\_PWRGD signal at the Sx entry flow. This signal should have a valid level during S0-S3 states.

**TSS** gets a dedicated power-good signal VCCST\_PWRGOOD\_TSS that is derived from a PCH signal called VCCST\_OVERRIDE. This is used in S5 state when Complete CPU in Reset but the **TSS** logic active.

If a dedicated driver is used to drive the VCCST supply, the VCCSTPWGOOD\_TSS should meet the same requirements as VCCST\_PWRGOOD\_TSS.

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**NOTE**

General Note: Some of legacy signals shown in these diagrams are not available as hard signals when eSPI is used.

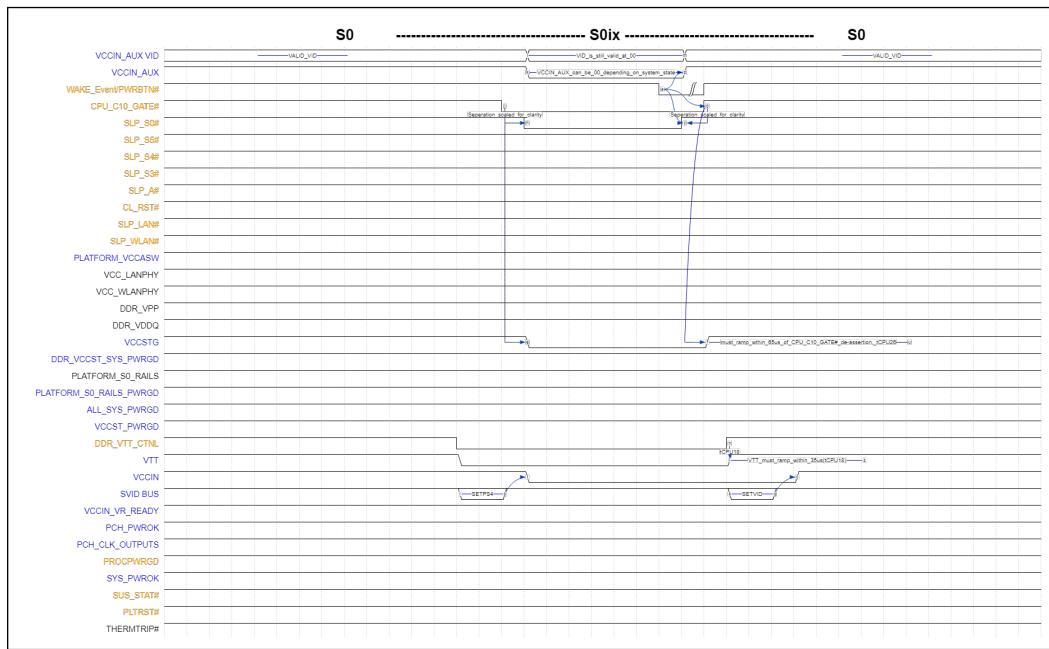
1. PCH will sample BATLOW# on the rising edge of DSW\_PWROK for DSx Systems
2. Refer Rail-to-Rail Power Sequencing Requirement section on PCH prime rail-to-rail power and power down dependencies
3. NA
4. NA
5. For a DSx system, PCH will ignore SUSACK# until after SUSWARN# is valid.
6. EC must ignore SUSWARN pin even in DSx system on G3 exit.
7. SLP\_A# always goes high with or before SLP\_S3#. Depending on PCH settings SLP\_A# may go high, then low, then high again all before SLP\_S3#, but will go high no later than SLP\_S3# on an Sx to S0 transition, or the Sx to S0 portion of G3 exit, Global Reset, and Deep Sx exit.

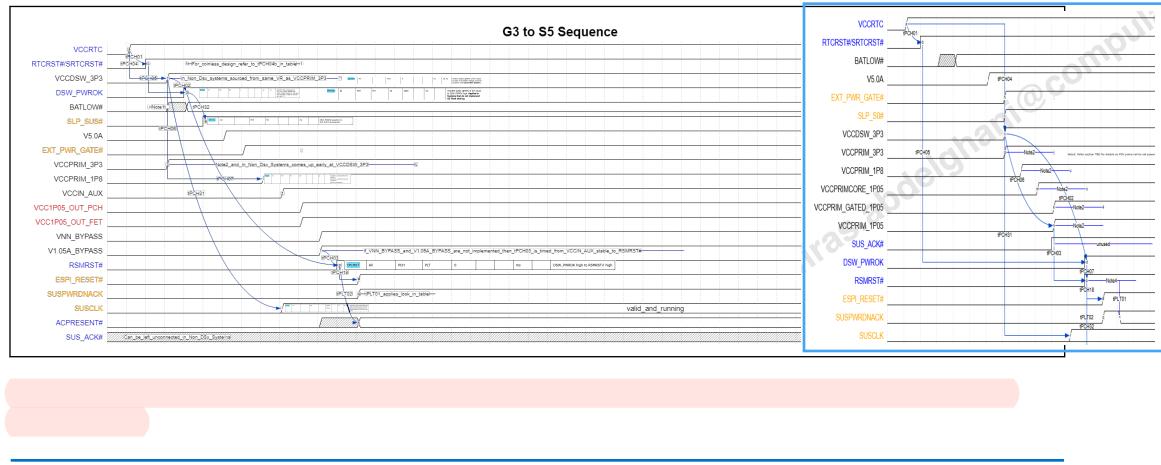
In the event of a global reset after SLP\_A# is de-asserted, during the power up sequence, SLP\_A# will assert and the controller monitoring the sleep signals should reset its timeouts.

8. High for WoL=1, Low for WoL=0. SLP\_LAN# may rise before, but no later than SLP\_A#.
9. On first exit from G3, SLP\_WLAN# de-asserts with SLP\_S3# de-assertion
10. Delay between SLP\_S5#, SLP\_S4#, and SLP\_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode the minimum delay between SLP\_S3#, SLP\_S4#, and SLP\_S5# is not guaranteed
11. VCCST, and VCCSTG can remain powered during S4 and S5 pwr states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer Platform Debug and Test Hooks chapter for more details. VCCSTG should only ramp up equal to or after VCCST.
12. Required with LPDDR4x, LPDDR4 and DDR4 memory configurations. For LP4/4x VPP, VDD2 and VDDQ timings, please refer to JEDEC Specification. There is no VTT for LP4/4x. It is applicable only for DDR4 memory based designs
13. VDDQ must ramp after VPP on DDR4 and LPDDR4 based systems, thus VDDQ may ramp up after SLP\_S3# de-assertion due to VR ramp timing and configuration common
14. NA
15. NA
16. ALL\_SYS\_PWRGD is assumed to logically AND together the PWRGD signals for the major system power rails
17. VCCST\_PWRGD can assert before or equal to PCH\_PWROK, but must never lag it. It is recommended that both VCCST\_PWRGD and PCH\_PWROK include ALL\_SYS\_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time
18. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.
19. NA

20. The Platform should ensure that PCH\_PWROK does not glitch when RSMRST# is de-asserted

**Figure 250. Timing Diagram for S0-S0ix-S0**





1. PCH will sample BATLOW# on the rising edge of DSW\_PWROK for DSx Systems
2. Refer Rail-to-Rail Power Sequencing Requirement section for details on PCH prime rail-to-rail power and power down dependencies.

#### **Additional Notes:**

Some of legacy signals shown in these diagrams, like SUSPWRDNACK, are not available as hard signals when eSPI is used, they are Virtual Wires.

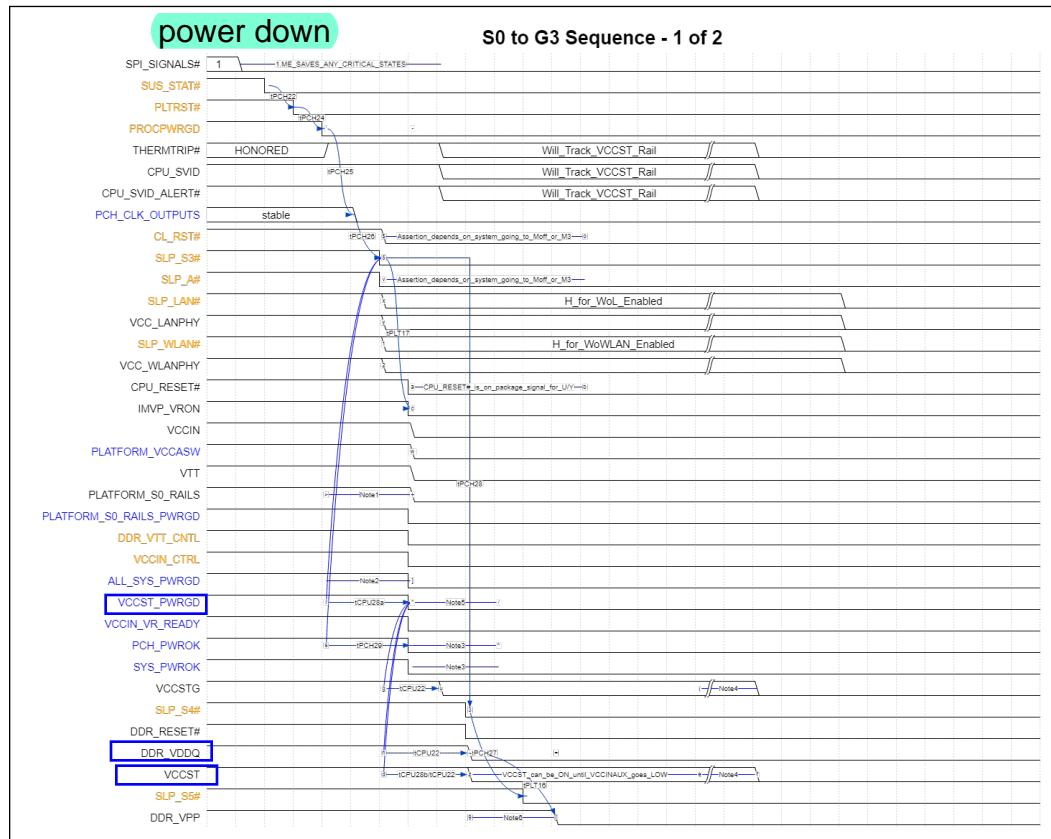
The state of the SLP\_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.

- SUSPWRDNACK
  - *Platform not supporting M3* - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted. Else, EC has an option to do whatever it wants with the SUS Rails
  - *Platform supporting M3* - EC must keep SUS Rails powered ON if: SUSPWRDNACK is asserted OR

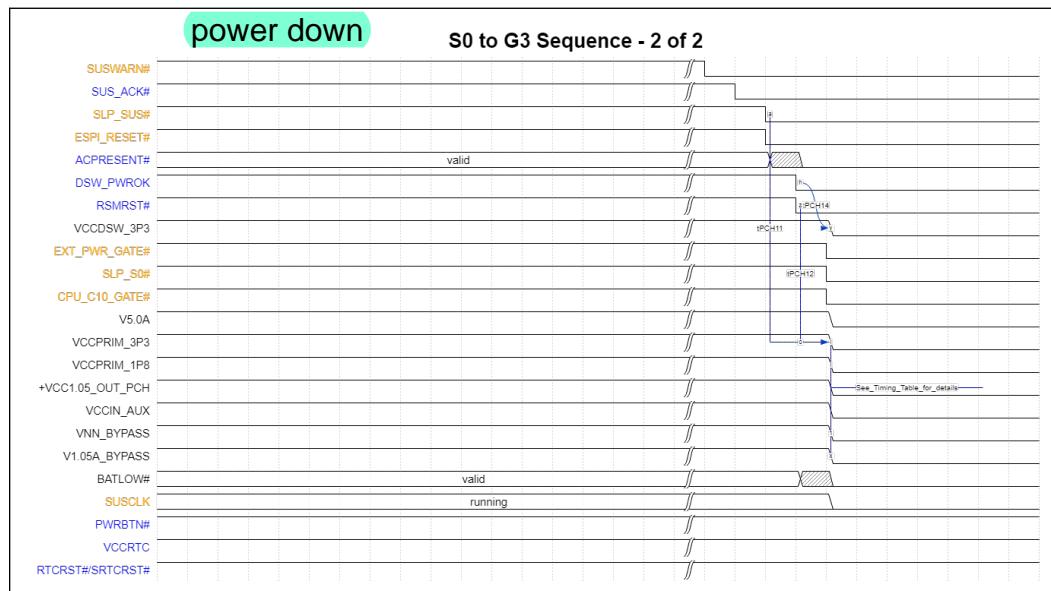
US Rails power has been applied. Else, EC has an option to do things with the SUS Rails

Keep SUS Rail is never

**Figure 252. Timing Diagram for S0/M0 to G3 [Deep Sx Platform]**



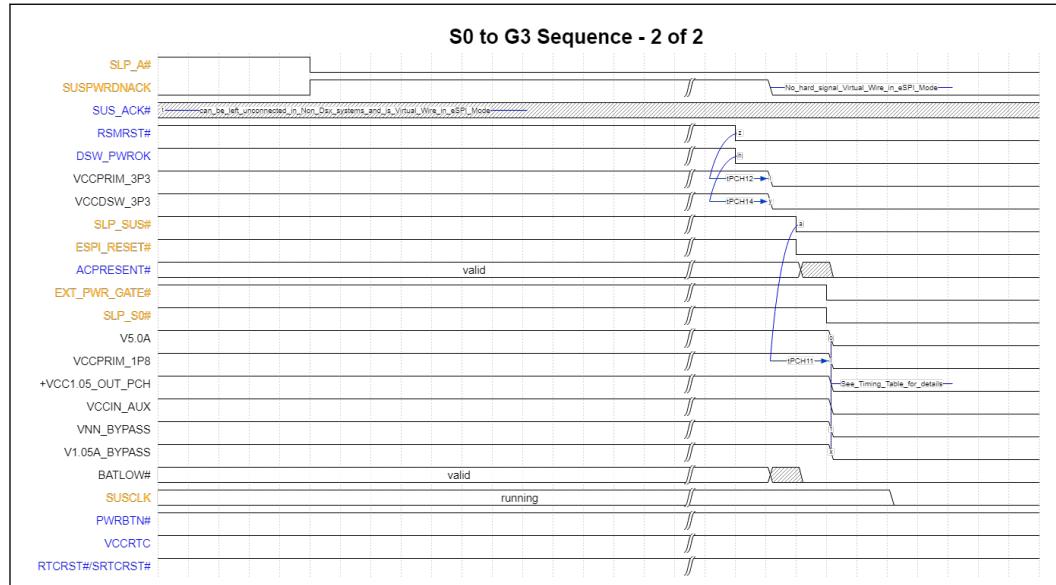
**Figure 253. Timing Diagram for S0/M0 to G3 [ Deep Sx Platform]**



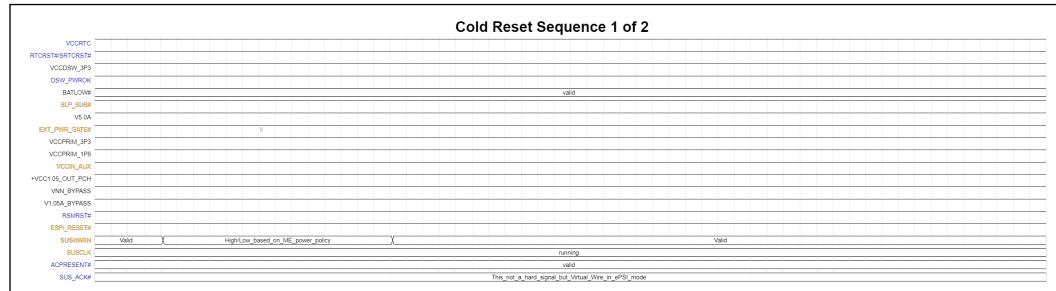
## POWER-DOWN

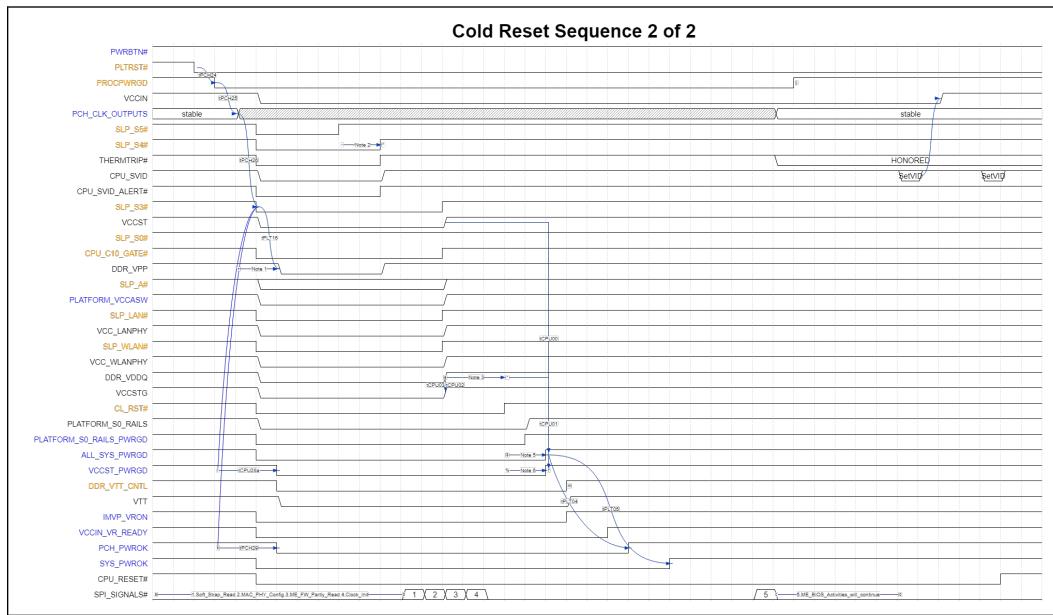
**Figure 254. Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]**

**For S0 to G3 Sequence 1 of 2 Refer to DSx Sequence**



**Figure 255. Timing Diagram for Cold Reset [Deep Sx Platform]**





### NOTES

1. Must ramp down AFTER VDDQ has ramped down
2. If the system EC is driving these signals in ESPI mode, based on the state of eSPI SLP Virtual Wires, the minimum delay between SLP\_S3#, SLP\_S4#, and SLP\_S5# is not guaranteed
3. VDDQ must ramp after VPP on DDR4 and LPDDR4 based systems, thus VDDQ may end up after SLP\_S3# de-assertion due to VR ramp timing and configuration
4. NA
5. ALL\_SYS\_PWRGD is assumed to logically AND together the PWRGD signals for the major system power rails
6. VCCST\_PWRGD can assert before or equal to PCH\_PWROK, but must never lag it. It is recommended that both VCCST\_PWRGD and PCH\_PWROK include ALL\_SYS\_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time. **IMVP VR\_ON is recommended to be triggered by ALL\_SYS\_PWRGD in order to help minimize boot latency.**

**Figure 256. Timing Diagram for Warm Reset [Deep Sx Platform]**

### Power Sequencing Timing Requirements

The following table defines the timing parameters used in the timing diagrams in previous sections. The timing parameters are put into three categories: tCPU, tPCH, and tPLT. tCPU parameters are mostly required by the processor, tPCH parameters are required or controlled by the PCH, and tPLT parameters are mostly controlled by the platform.

The timing parameters are defined by Min, Max and Typical specifications. The Min and Max timings refer to the minimum or maximum timings allowed between the first and second signals in the Description column, as are the timing boundaries that must be followed. The Typical column refer to the typical timing values measured on Intel boards during validation, which do not imply a requirement but can be used as a reference.

**Table 231. Platform Sequencing Timing Parameters**

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tCPU00	All	CPU	PLT	2			ms	6, 7	VCCST, VCCSTG ramped and stable to VccST_PWRGD assertion
tCPU01	All	CPU	PLT	1			ms	6, 7	VDDQ ramped and stable to VccST_PWRGD assertion
tCPU02	All	CPU	PLT		No Limit		ms	43	VCCST, VCCSTG ramped and stable before VDDQ stable Note: tCPU02 and tCPU03 are mutually exclusive, and only one of the parameters needs to be met depending on the rail order of VCCST/VCCSTG and VDDQ

*continued...*

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tCPU03	All	CPU	PLT		No Limit		ms	43	VDDQ ramped and stable before VCCST, VCCSTG stable  Note: tCPU02 and tCPU03 are mutually exclusive, and only one of the parameters needs to be met depending on the rail order of VCCST/VCCSTG and VDDQ
tCPU04	All	CPU	PLT	0			ns	31	VCCST must always ramp with or earlier than VCCSTG. VCCST >= VCCSTG at all times during ramp.
tCPU08	All	CPU	PCH	1			ms	8	PCH CLK outputs stable and CPU VRs stable/ready to PROCPWRGD assertion
tCPU16	All	CPU	PLT	0			ns	32	VCCST_PWRGD assertion to PCH_PWROK assertion
tCPU18	All	CPU	PLT	0	35		us	34	DDR_VTT_CNTL (was DDR_PG_CTL) assertion to DDR_VTT supplied ramped and stable while PLTRST = H (de-asserted).
tCPU19	All		CPU	0	100		ns	9	VccST_PWRGD assertion to DDR_VTT_CNTL (was DDR_PG_CTL) asserted.
tCPU20	All	CPU	PLT + PCH		500		ms		THERMTRIP# assertion until VCCIN VR is disabled and not sourcing power
tCPU21	All	CPU	PCH		1		ms		THERMTRIP# assertion until PCH issues global reset and assertion of SLP_SX signals
tCPU22	All	CPU	PLT	1			us	36, 37	VCCST_PWRGD de-assertion to either VDDQ, VCCST, VCCSTG below specification for normal S0 to Sx transitions. Recommend VCCST_PWRGD goes low with SLP_S3#
tCPU26	All			10	65		us		CPU_C10_GATE# de-assertion to VCCSTG, VCC1P8A stable, the rail must meet this max ramp time.
tCPU29	All	CPU	PLT		100		mV/us	13	Processor power rail instantaneous slew rate.
tPCH01	All	PCH	PLT	9			ms	1, 46, 47	VccRTC = 2.0V to the point in time where voltage on the RTC resets equals 0.65 times the voltage present on the VccRTC rail during ramp. This measurement should be made from VccRTC = 2.0V to the first of RTCRST# or SRTCRST# reaching 0.65 * VccRTC .
tPCH02a	All	PCH	PLT	10	2000		ms		VccDSW stable (@95% of full value) to DSW_PWROK high. <b>Applies to Systems that do not implement G3 Flash sharing</b>
tPCH02b	All	PCH	PLT	10	See Note		ms	48	VccDSW stable (@95% of full value) to DSW_PWROK high. <b>Only applies to Systems that implement G3 Flash sharing</b>
tPCH03a	All	PCH	PLT	10	2000		ms		VccPrimary stable (@95% of full value) to RSMRST# high <b>Applies to Systems that do not implement G3 Flash sharing</b>
tPCH03b	All	PCH	PLT	10	See Note		ms	49	VccPrimary stable (@95% of full value) to RSMRST# high <b>Only applies to Systems that implement G3 Flash sharing</b>
tPCH04a	All		PCH	9			ms	29, 42	VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with <b>coined RTC battery</b>

*continued...*

VCCDSW\_3P3 [-VC-  
CPDSW\_3P3JVC-  
CPRIM\_1P8 [+VC-  
CPRIM\_1P8]

<b>Label</b>	<b>Applicable SKU</b>	<b>Required By</b>	<b>Controlled By</b>	<b>Min.</b>	<b>Max.</b>	<b>Typical</b>	<b>Units</b>	<b>Note #</b>	<b>Description</b>
tPCH04b	All		PCH	30			ms	29, 42	VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with <b>coinless RTC</b> . Please refer to IBP#549657 for Design considerations technical advisory document without RTC battery. Earlier this timing was referred as tPCH48.
tPCH05	All	PCH	PLT	1			us	42	RTCRST# high (voltage above ViH_min) to DSW_PWROK high (when voltage crosses ViL_max such that internally it might be resolved as a logic '1')
tPCH06	All	PCH	PLT	200			us		VccDSW 3.3 stable (@95% of full value) to VccPrimary 1.8V starting to ramp (for DSx or nonDSx configurations)
tPCH07	All	PCH	PLT	0			ms		DSW_PWROK high to RSMRST# high
tPCH08	All	PCH	PLT	1			ms		SLP_S3# de-assertion to PCH_PWROK assertion
tPCH09	All	PCH	PLT	2, 4, 8, 16			ms		SLP_A# high to PCH assuming ASW rails are stable (95% of full value)
tPCH11	All	PCH	PLT	100			ns		SLP_SUS# asserting to VccPRIM dropping 5% of nominal value
tPCH12	All	PCH	PLT	400			ns	5, 24	RSMRST# asserting to VccPRIM dropping 5% of nominal value
tPCH13	All	PCH		0			ms	14	RTCRST# asserting to VccRTC dropping 5% of nominal value (this applies only when RTC battery is removed)
tPCH14	All	PCH	PLT	400			ns	4, 5	DSW_PWROK falling to any of VccDSW, VccPrimary dropping 5% of nominal value
tPCH15	All	PCH	PLT		100		ms		SLP_LAN# (or LANPHYC) rising to VccLANPHY high and stable
tPCH18	All		PCH	90			us		De-assertion of RSMRST# to De-assertion of eSPI_RESET# on exit from G3 (DSx platforms only), or exit from DSx
	All		PCH	90			us		De-assertion of RSMRST# to De-assertion of eSPI_RESET# on exit from G3 (Non-DSx platforms only)
tPCH20	All	PLT	PCH	-100			ns		DDR_RESET# assertion to SLP_S4# assertion (The negative minimum timing implies that DDR_RESET# must either fall before SLP_S4# or within 100 nS after it).
tPCH21	All		PCH	Refer note 38			ms	38	Warm Reset PLTRST# assertion duration time
tPCH22	All		PCH	210			us		SUS_STAT# active to PLTRST# active. <i>Note:</i> Not applicable for eSPI systems.
tPCH23	All		PCH	60			us		SUS_STAT# de-assertion to PLTRST# de-assertion. <i>Note:</i> Not applicable for eSPI systems.
tPCH24	All		PCH	30			us		PLTRST# assertion to PROCPWRGD de-assertion

*continued...*

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tPCH25	All		PCH	10			us		PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF. This timing is programmable (Range = 10us, 100us, 1ms, 10ms). Default is set to 10 us.
tPCH26	All		PCH	1			us		CLKOUT_BCLK turning OFF to SLP_S3# assertion
tPCH27	All		PCH	30			us	33	SLP_S4# assertion to SLP_S5# assertion
tPCH28	All		PCH	30			us	33	SLP_S3# assertion to SLP_S4# assertion
tPCH29	All		PCH	0			ms		SLP_S3# assertion to PCH_PWROK deassertion
tPCH31	All		PCH		tPCH02 + tPCH32		ms	15, 44	VccDSW3p3 ramped and stable until SUSCLK is stable. SUSCLK will start before the max timing, but will not be guaranteed valid until max timing is met
tPCH32	All		PCH	95			ms		DSW_PWROK assertion to SLP_SUS# de-assertion
tPCH33	All		PCH	0, 99			ms	16	PCH_PWROK high to PLTRST# de-assertion. This timing is set by the PCH via Soft strap settings
tPCH34	All	PCH	PLT		50		ms		Time from start of ramp of the first prim rail after SLP_SUS# de-assertion to completion of primary and bypass rail ramp.
tPCH35	All	PCH	PLT		See Note		ms	20, 49	SLP_SUS# low to PCH PRIMARY rails reaching 200mV or less.
tPCH36	All	PCH	PLT		100		mV/us		PCH Power rails instantaneous slew rate
tPCH41	All	PCH	PCH	1			ms		PCH_PWROK high to PCH clock outputs stable
tPCH43	All	PCH	PLT	95			ms	28	DSW_PWROK assertion to PWRBTN# monitored
tPCH44	All	PCH	PLT	500			us		tPCH09 expiring to CL_RST# high
tPCH45	All		PCH	1, 5, 50, 100			ms	39	Clock outputs stable to PROCPWRGD assertion to processor. Timing set by PCH via Soft Strap settings
tPCH46	All		PCH	1, 2, 5, 10			ms	39	PROCPWRGD and SYS_PWROK High to SUS_STAT# de-assertion. This timing is not applicable for eSPI systems. <i>Note:</i> Timing can be adjusted through the FIT tool
tPCH47	UP4		PCH	10.5	200		us	21, 51	De-assertion of EXT_PWR_GATE# until gated VCCMPHYGT_1P05 supply stable (@ 95% of full value)
tPCH48	UP4		PCH	10.5	200		us	50, 51	De-assertion of EXT_PWR_GATE2# until gated VCCPRIM_GATED_1P05 supply stable (@ 95% of full value)
tPCH49	UP4		PCH	6			mV/us	21, 50	MPHYGT_1P05/PRIM_GATED_1P05 Supply instantaneous slew rate
tPLT01	All		PCH	200			ms	2	RSMRST# de-assertion to SUSPWRDNACK valid. Timing set by PCH.
tPLT02	All			0	90		ms		RSMRST# de-assertion to ACPPRESENT valid (not floating). <i>Note:</i> This is only for platforms not supporting Deep Sx state

*continued...*

20. No Ramp down requirement between rails. All VRs should stop regulation based on SLP\_SUS# signal, or another common shutdown signal. Applies to all power down cases except PCH induced FIVR emergency shut down chase where SLP\_SUS# goes low with to shut down PCH VRs.

49. Total exposure to any of the PRIMARY rails > 200mV, with RSMRST# low must not exceed 6 days of the life of the PCH. Failure to meet this requirement over the life of the system could result in reduce component reliability and lifetime.

<b>Label</b>	<b>Applicable SKU</b>	<b>Required By</b>	<b>Controlled By</b>	<b>Min.</b>	<b>Max.</b>	<b>Typical</b>	<b>Units</b>	<b>Note #</b>	<b>Description</b>
	All				0		ms		RSMRST# de-assertion to ACPRESENT valid (not floating) [For platforms supporting Deep Sx state].  Note: ACPRESENT is a powered input to the PCH while in the Deep Sx state (that is, when DSW_PWROK=1 and RSMRST#=0). The PCH implements a weak pull-down on ACPRESENT while RSMRST#=0 such that the input is observed as 0 if not driven actively by the board during this time. If driven actively by the board to 1 while in Deep Sx and if the PCH is enabled to treat the ACPRESENT indication as a wake event from Deep Sx, then the PCH will power up the Primary well.
tPLT04	All	CPU/PCH	PLT	1			ms	3, 19	ALL_SYS_PWRGD assertion to PCH_PWROK. This timing must be controlled on the platform.
tPLT05	All		PLT	Platform dependent	No limit			18	ALL_SYS_PWRGD assertion to SYS_PWROK. This timing must be controlled on the platform. SYS_PWROK provides a platform/EC mechanism to stall the PCH de-assertion of PLTRST# to the platform. Different platform components may have difference timing requirements from when their power rails are stable until their respective reset signal can de-assert. Platform designer should adjust this timing based on their specific platform requirements.
tPLT14	All		PCH	4			s		Power cycle duration time; programmable via PM_CFG.PWR_CYC_DUR bit.
tPLT15	All	PLT (MEM)	PLT		200		us	40	SLP_S4# assertion to VDDQ VR Enable Low [VDDQ VR disabled]. Memory dependent, refer JEDEC requirements
tPLT16	All	PLT (MEM)	PLT	30			ms	30	VDDQ ramp down to start of VPP ramp down when entering S4 and lower. This is not a Processor requirement but a recommended timing to help meet the JEDEC sequencing requirements. Platform designers are responsible for making sure their designs meet the power sequencing requirements for the memory technology used in their designs.
tPLT20	All	PLT (MEM)	PLT	2.5			ms	30	VPP ramped to VDDQ start of ramp when entering S0 at power up. This is not a Processor requirement but a recommended timing to help meet the JEDEC sequencing requirements. Platform designers are responsible for making sure their designs meet the power sequencing requirements for the memory technology used in their designs.

*continued...*

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tPLT17	All	CPU	PLT	0			us	35	IMVP VR_ON low to VCCST below 95% of its value
tPLT19	All	PLT	PLT		10		us	22	RSMRST_PWRGD# or SLP_SUS# assertion to RSMRST# assertion

**Notes:**

1. PCH Primary Rails must never be active while VCCRTC is OFF
2. RSMRST# should be de-asserted for at least 200ms before PCH will consider SUSPWRDNACK valid.
3. PCH can delay de-assertion of PLTRST# with a soft strap setting. Refer tPCH45 (t573) and tPCH46 (t1001) and the SPI Programming Guide for more details.
4. For catastrophic/surprise power failures only.
5. For surprise power down cases, if DSW\_PWROK is de-asserted (tPCH16) before DSW3.3 **and** any other Prim rails droop out of spec, there is no risk of RTC corruption (assuming VCCRTC was previously powered and VCCRTC# is de-asserted) and this spec can be ignored
6. VCCST\_PWRGD has no edge rate requirement, but edges must be monotonic.
7. VCCST\_PWRGD must accurately reflect the state of VCCST and must not glitch when VCCST, VCCSTG or VDDQ power is applied. Additionally, VCCST\_PWRGD must track to the state of PCH\_PWROK on the platform. When PCH\_PWROK de-asserts during S0 --> Sx transitions, then VCCST\_PWRGD must also de-assert.
8. Processor's PROCPWRGD is not expected to be used externally on the platform, but is available for monitoring.
9. DDR\_VTT\_CTL will start to go high on VDD2 ramp with VCCST\_PWRGD low for Sx to S0 power state transitions.
10. It is strongly recommended that the SLP\_S3# be a qualifying input signal to ALL\_SYS\_PWRGD logic, which drives IMVP VR\_ON inputs. Additionally, it is recommended that SLP\_S3# also qualify the EN control to the VCCIO power supply
11. Max timing is only applicable during S0i3 exit if the voltage rail is actively power gated. Not applicable during Sx-S0 transition
12. NA
13. Applies to all CPU power supply rails
14. There are no perceived functional failures if this minimum is violated since all data is lost anyway when VccRTC drops. The only real requirement is to avoid driving a high signal level into the powered down device for an extended period of time, assuming an external device(s) on a different power supply then VCCRTC is driving RTCRST# or any other RTC well input signal.
15. SUSCLK is now powered in DSW well.
16. PCH can delay de-assertion of PLTRST# with a soft strap setting. If tPCH33 is not enabled, the platform is responsible for controlling the assertion timing of PCH\_PWROK and SYS\_PWROK in such a way that it satisfies platform component timing requirements of power stable to reset de-assertion. Refer SPI Programming Guide for more details. On a platform level this timing doesn't necessarily need to meet 99ms, PCH soft straps guarantees a min of 99ms.
17. NA
18. Example, if the platform only has mini-PCIe\* devices requiring a 1 ms delay from power rails stable to PCIe\* reset de-assertion, then the minimum value for ALL\_SYS\_PWRGD assertion to SYS\_PWROK can be reduced to 1 ms. If SYS\_PWROK asserts before PCH\_PWROK, no additional delay will be added by the PCH to delay PLTRST# de-assertion and the final timing value will be subject to internal PCH timing parameters.
19. PCH\_PWROK assertion assumes CPU and PCH voltage rails are ramped and stable.
20. No Ramp down requirement between rails. All VRs should stop regulation based on SLP\_SUS# signal, or another common shutdown signal. Applies to all power down cases except PCH induced FIVR emergency shut down chase where SLP\_SUS# goes low with to shut down PCH VRs.
21. Only applicable to platforms that implement external VCCMPHYGT\_1P05 power gating. Does not apply to G3/DSx to Sx ramp up.
22. 10us max limit is an estimation and will vary based on platform VR and EC implementation details. Platform designers are responsible for ensuring that tPCH12 is not violated during normal DSx entries based on EC and VR response times to assertion of SLP\_SUS# and/or RSMRST\_PWRGD#
23. PCH will have a minimum of a 1ms delay from PCH\_PWROK to assertion of PROCPWRGD. Therefore, the platform is only responsible to have these rails ready a minimum of 0ms before PCH\_PWROK assertion.
24. Applicable to all power down sequences where Prime well rails are turned off and to emergency power loss scenario. Refer RSMRST#/DSW\_PWROK Special Requirements section.
25. NA
26. NA
27. If VCCSTG and VCCIO supplies are merged together as a single supply, then the timing requirement is between VCCST/VCCSTG/VCCIO and VCCSA
28. Applicable to all G3 exits where GEN\_PMCON\_B.AG3E=1. The PWRBTN# must assert for at least 16ms after the minimum tPCH43 timing before PCH will detect PWRBTN# as a wake event
29. For scenarios where the coin-cell is dead or missing, the PCH can electrically tolerate the VCCRTC and VCCDSW/VCCPRIM 3.3V supplies ramping simultaneously with VCCDSW/VCCPRIM 3.3V leading VCCRTC by ~0.2 – 0.3V (ie. voltage drop associated with the coin cell Schottky diode circuit). These scenarios are not allowed as typical power sequencing scenarios, and are expected to be very infrequent. In these scenarios, glitch-free signal operation on DSW signals can not be guaranteed when the platform is configured for DSx mode. Likewise, glitch-free signal operation on DSW and PRIM well signals can not be guaranteed when the platform is configured for non-DSx mode
30. Generally, JEDEC specifications require VPP >= VDDQ for both power up and power down sequences. This timing parameter is a suggested value as ensure this requirement is met on power down, but system designer must account for other platform level considerations such as output decoupling, discharge circuits, etc that can alter this relationship.
31. VCCST supply is typically controlled by SLP\_S3# only, and VCCSTG supply is typically controlled by SLP\_S0# AND SLP\_S3#. Since the timing delay between SLP\_S3# and SLP\_S4# deassertion during a S4/S5 à S0 transition can be small (defined by tPCH28), OEMs may need to take extra steps to ensure this timing is met. Example, power gates of equivalent slew rate may be required on both VCCST and VCCSTG supplies. Alternatively, a small timing delay path might be required on the SLP\_S3# path of the VCCSTG power gate enable
32. VCCST\_PWRGD should start to assert no later than when PCH\_PWROK asserts; however, VCCST\_PWRGD may lag completing its ramp with respect to PCH\_PWROK by up to 20us
33. Not applicable to eSPI mode, refer to the eSPI Compatibility Specification (#508740) for eSPI implementations
34. Only applies to configurations that use DDR\_VTT\_VCTRL signal to enable/disable VTT VR and only applies after PLTRST# has de-asserted (ie, S0). VTT must be completely ramped and ready for full load at or before the de-assertion of PLTRST# on Sx -> S0 transitions.
35. Timing to VR being disabled, not until the VR is fully ramped down
36. S0 to Sx transition with VCCST powered in Sx state. In TGL platforms ST control changes to SLP\_S3# OR VCCST\_OVERRIDE .
37. S0 to Sx transition with VCCST unpowered in Sx
38. Recommend not to exceed 10ms delay with respect to SLP\_S3#
39. During a warm reset sequence, the PCH sequencing flows will internally re-execute several timing parameters and tPCH45 and tPCH46 are two of the parameters that are re-executed. tPCH45 and tPCH46 are primarily for G3/DSx/Sx à S0 flows, but they are executed for cold boot, cold reset, and warm reset. The nominal setting for these timings is partially controlled by the setting of SPI soft straps associated with tPCH45 and tPCH46. The

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
minimum possible PLTRST# assertion time will be equal to the soft strap settings for tPCH45 + tPCH46. The maximum PLTRST# assertion time is not guaranteed across all warm reset cycles, but the typical worst case assertion time is approximately equal to (tPCH45 soft strap setting) + (tPCH46 soft strap setting ) + 20ms.									
40. This is a platform timing recommendation to help ensure that memory device power down sequencing requirements between VDDQ and VPP are likely to be met (refer tPLT16). This is not a requirement for the TGL Processor itself. Refer to the JEDEC LPDDR4 and DDR4 power down sequencing requirements for more details									
41. This parameter is programmable, refer to the Flash Descriptor Record in the SPI Programming Guide in the ME firmware package									
42. For the dead RTC coin cell and coin cell-less with depleted main battery RTC cases where the 3.3DSW ramps and powers the RTC well, the board designer should set the 3.3DSW rail stable to DSW_PWROK assertion delay (tPCH02) for = 30ms. This is required to ensure that SRTCST# and RTCRST# de-assert after VCCRTC is stable, but before DSW_PWROK assertion. Failure to meet this requirement may result in DSW_PWROK asserting with, or before, SRTCST# and RTCRST# reach VIH, which is a sequencing violation and can result in a non-booting system scenario. Refer <a href="#">Real Time Clock (RTC) Design Guidelines</a> on page 123 and <a href="#">RTC External RTCRST# Circuit</a> on page 126 and <a href="#">RTC External SRTCST# Circuit</a> on page 127 for SRTCST# and RTCRST# RC timing network details									
43. tCPU02 and tCPU03 are mutually exclusive, only tCPU02 or tCPU03 needs to be met									
44. SUSCLK stable means the clock is toggling and is within it is defined parameters. This timing spec is applicable to all G3 exits, excluding the G3 exit immediately following the ramp of VCCRTC, which may have a longer delay									
45. Refer tPCH43 for- DSW_PWROK assertion to PWRBTN# monitored timing aspect.									
46. C3 and C4 Capacitors used in the RTC external circuit should be evaluated with regards to aging, voltage and temperature characteristics to ensure reliable operation in the intended operating environment. See section 6.2.3 RTC External RTCRST# Capacitors.									
47. For measurement details, reference RTC Reset Timing Technical Advisory - Document #610459.									
48. Total exposure to DSW above > 200mV, with DSW_PWROK low must not exceed 6 days of the life of the PCH. Failure to meet this requirement over the life of the system could result in reduce component reliability and lifetime.									
49. Total exposure to any of the PRIMARY rails > 200mV, with RSMRST# low must not exceed 6 days of the life of the PCH. Failure to meet this requirement over the life of the system could result in reduce component reliability and lifetime.									
50. Only applicable to platforms that implement external VCCPRIM_GATED_1P05 power gating. Does not apply to G3/DSx to Sx ramp up.									
51. MPHYGT_1P05 and PRIM_GATED_1P05 gates are no longer mandatory to implement. However existing designs with gates can continue with them.									
<b>Additional Notes:</b>									
• Unless otherwise noted, all specifications in this table apply to all processor frequencies.									
• DDR_RESET# behavior does not directly track the state of VDDQ rail. For DDR_RESET# to assert properly on surprise power failure, the VDDQ VR pwrgood output should be an input into the logic generating PCH_PWROK									

## 10.12.6 DSW and PRIMARY Power up / Power Down Special Requirements

The PCH has lifetime exposure limits for the DSW and PRIMARY rails as follows:

- **DSW rail and DSW\_PWROK:** The PCH requires that the sum total time with the VCC\_DSW > 200mV **AND** DSW\_PWROK low, during rail start up and shutdown, must not exceed 6 days of the life of the PCH.
- **Primary Rails and RSMRST#:** The PCH requires that the sum total time with any of the PRIMARY rails > 200mV **AND** RSMRST low, during rail start up and shutdown, not exceed 6 days of the life of the PCH.

Total exposure time will vary by platform implementation. Platform designs that support G3 flash sharing where the PCH is powered with RSMRST# low for more than 2 seconds must pay particular attention to the above requirements. Failure to meet this requirement over the life of the system could result in reduce component reliability and lifetime.

The following example demonstrates how to calculate DSW and PRIMARY rails total exposure time with their respective power goods (DSW\_PWROK and RSMRST#) low over the product lifetime.

### Example System Assumptions

DSx enabled design where system goes to DSx on AC and G3 on battery, **with G3 Flash sharing**.

### System Characteristics as Determined by OEM for Target System Usage

**VR Ramp & Power Good Delays (Power Up):**

- VCCDSW Ramp Time: 1 ms
- DSW rail stable to DWPROK L-->H delay for design: 15 ms
- PRIMARY rail total ramp Time (start of ramp to rail ramp compete): 5 ms
- PRIMARY rails stable to RSMRST# L-->H delay for design: 20 seconds

**Rail Discharge Characteristics (at DSx and G3 entry):**

- DSW discharge time at G3 entry: 30 ms
- PRIMARY discharge time at G3 or DSx entry: 200 ms

**DSx and G3 entry Frequency:**

- Number of DSx entries per day: 10
- Number of G3 entries per day: 5

**Target Product Life: 5 years (1825 days)**

**DSx/G3 Entry Exposure Time Calculation:****DSW per day power down exposure:**

(5 G3 entries per day) \* (30ms discharge per entry) = **150ms per day**

**PRIMARY rail power down exposure on G3 & DSx Entry:**

(10 DSx entries per day + 5 G3 entries per day) \* (200ms discharge per entry) = **3s per day**

**DSx and G3 Exit Exposure Time Calculation:****G3 Exit:****DSW Rail Power Up Exposure on G3 exit:**

5 G3 exits per day \* (1ms DSW ramp time + 15ms DSW stable to DPWROK H) = **80ms per day**

**Primary Rails Power Up Exposure on G3 exit:**

5 G3 exits per day \* (5ms PRIMARY ramp time + 20s PRIMARY rails stable to RSMRST# H) = **100.025s per day**

**DSx Exit:****Primary Rails Power Up Exposure on DSx exit:**

10 DSx exits per day \* (5ms PRIMARY ramp time + 20s PRIMARY rails stable time) = **200.05s per day**

### Final Calculation for Total Life Exposure Time:

#### For DSW Rail:

Total DSW per day exposure time = (G3 Entry Exposure Time) + (G3 Exit Exposure Time)

**Total DSW rail per day Exposure Time** = 150ms per day + 80ms = 230ms (0.23s) per day

**Total DSW rail exposure over life of part:** 0.23s per day \* (1825 days)/86400(s/day) = **0.005 days**

**DSW Final Result:** DSW rail meets the 6 day max exposure requirement.

#### For PRIM Rails:

Total PRIMARY rail per day Exposure time = (DSx/G3 Entry Exposure Time) + (Total DSx and G3 Exit Exposure Time)

**Total PRIMARY rail per day Exposure Time** = 3s per day + (100.025s per day + 200.05s per day) = 303.075s per day

**Total PRIMARY rail exposure over life of part:** 303.075s per day \* (1825 days)/86400(s/day) = **6.4days**

**PRIMARY Final Result:** PRIMARY rails fail to meet the 6 day limit.

#### NOTE

**This must be corrected to ensure component reliability over the life of the part.**

For this case the DSW rail meets the 6 day max limit, but the PRIMARY rails do not due to the long time spent with PRIMARY power and RSMRST# low for G3 FLASH sharing. To fix this the designer must go back and lower the PRIMARY stable to RSMRST# H time to meet the 6 day requirement. The designer must either:

Find a way to lower the per instance time with PRIMARY rails powered with RSMRST# low

#### OR

Add isolation to the shared SPI interface so that the PCH does not need to be powered during point in sequence when the EC is mastering the SPI bus to access the shared FLASH device.

Refer to Section <*Flash Sharing Topology in "SPI0 Flash" sheet provided with PDG package*> for more information on PCH SPI bus isolation with G3 FLASH sharing.

## 10.12.7 Rail-to-Rail Power Sequencing Requirements

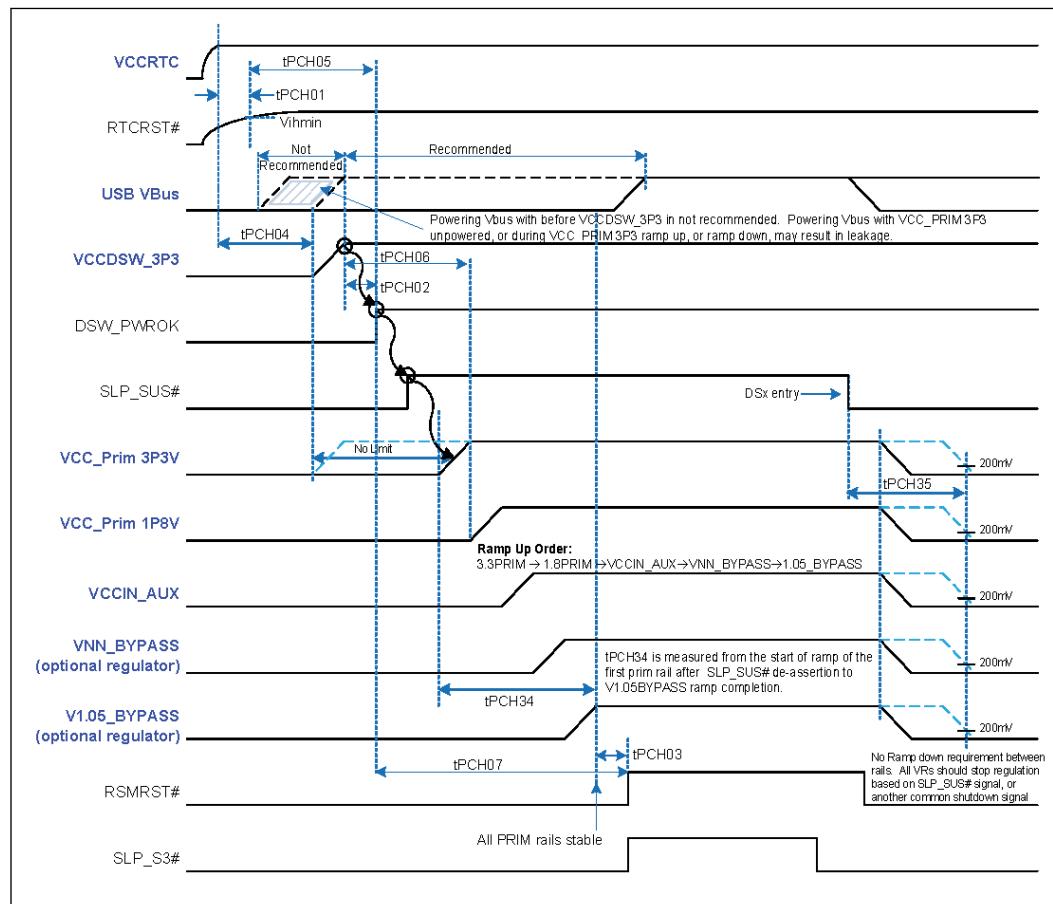
### PCH Rail-to-Rail Sequencing For Various Supplies

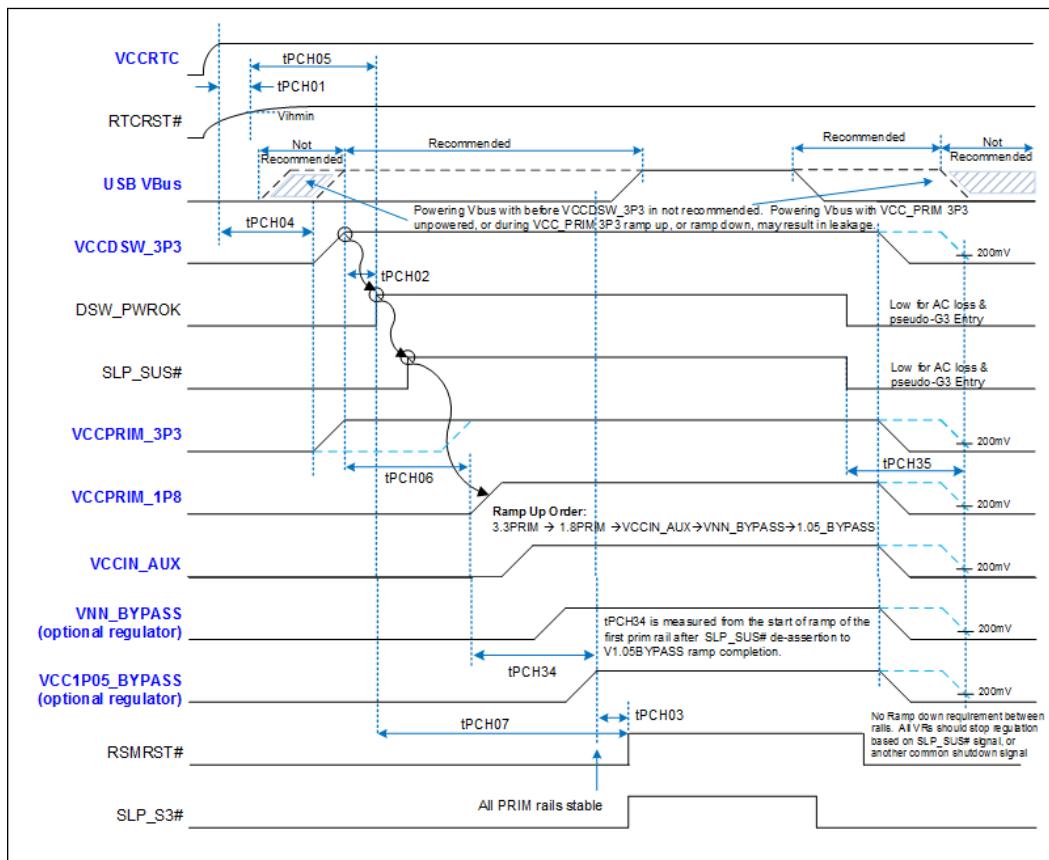
The following diagrams show the recommended rail-to-rail sequencing requirement for Deep Sx configuration( the below figure) and Non-Deep Sx configuration ( [Figure 258](#) on page 460).

PCH architecture implements capabilities to help minimize rail-to-rail sequencing related problems. As long as the RTC 3.3 V supply is powered up properly in advance of DSW and Primary rails, isolation logic is active and will help achieve proper isolation between power rails during power up and power down sequences. The I/O interfaces will achieve proper isolation between the 1.8 V and 3.3 V Primary / DSW supplies. This does not guarantee glitch-free start up during transitions out of G3 and Sx, refer Bypass and Aux Configuration Registers in Intel® 500 Series Chipset Family Platform Controller Hub (PCH) EDS Vol 2 (#619207)

During scenarios where the RTC supply is not powered such as a dead coin cell scenario and it is instead ramping along the Primary /DSW supplies through external platform circuitry, proper isolation between the 1.8 V and 3.3 V Primary / DSW supplies cannot be guaranteed. It is thus possible that current inrush/back drive events could exist in these cases, but these scenarios are not a reliability risk to the PCH. It is, however, assumed that for general operation of PCH, the RTC supply should be ramped and valid before the DSW and Primary rails ramp. Ramping the RTC supply simultaneously with the VCCDSW\_3p3 rail for Deep Sx systems and VCCPRIM\_3p3/ VCCDSW\_3p3 rails for Non-Deep Sx systems as a standard power up sequence for every G3 exit is not a valid configuration and is not allowed.

Figure 257. Rail-to-Rail Sequencing Requirement for Deep Sx Configured System



**Figure 258. Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System**

**Table 232. Rail-to-Rail Sequencing Requirements**

Rail 1	Rail 2	Ramp Up	Ramp Down
VCC_PRIM 3.3 V	VCC_PRIM 1.8 V	VCC_PRIM_3.3 ramps before VCC_PRIM_1.8	All rails must ramp down within tPCH35. Refer General Rail-to-Rail Sequencing
VCC_PRIM 3.3 V	VCCIN_AUX	3.3 V Primary rail ramp in advance of the VCCIN_AUX	All rails must ramp down within tPCH35. Refer General Rail-to-Rail Sequencing
VCC_PRIM 1.8 V	VCCIN_AUX	1.8 V Primary rail ramp in advance of the VCCIN_AUX. VCCIN_AUX can ramp with V1.8A for fixed 1.8V VCCIN_AUX design	All rails must ramp down within tPCH35. Refer General Rail-to-Rail Sequencing
VCC_PRIM 3p3/ VCC_PRIM 1.8V	Vbus	Vbus ramp after VCC_PRIM 3.3V reached 95% of their final value	Vbus ramp down with or at the same time that, the VCCDSW_3P3 is ramping down
VCC_PRIM 1.8V	VNN_BYPASS/ V1.05_BYPASS	VCC_PRIM 1.8V must ramp before the VNN_BYPASS/ V1.05_BYPASS	All rails must ramp down within tPCH35. Refer General Rail-to-Rail Sequencing

- Primary Rails and External USB Vbus Power Sequencing

The Vbus provided to external USB ports can be used by USB devices to power their USB speed detect pull-up resistors. Some devices generate a local 3.3V power supply and pull up the D+ / D- lines with a 1.5k resistor. Other devices, per more recent USB ECRs, are allowed to pull up the D+/D- lines with Vbus voltage directly using ~7.5k resistor; implementation varies with device design.

If Vbus is powered while VCCPRIM\_3p3 is not powered, and a device pulls either data line to 3.3V via its speed select pull-up resistor, the PCH will be exposed to leakage current through its un-powered USB 2.0 buffers. These leakage paths potentially impact both Non-Deep Sx and Deep Sx board designs alike.

The leakage paths exist only when Vbus is powered while VCCPRIM\_3p3 and VCCPRIM\_1.8V are unpowered.

Powering Vbus while the PRIM rails are not powered is permitted, but designers should be aware that leakage through the PCH may occur.

- **General Rail-to-Rail Sequencing**

All platform rails should follow a sequential order for system power on which are already called out in the [Table 231](#) on page 449.

On CPU side, for power up, VCCST always should ramp with or before VCCSTG. System should meet VDDQ rail order relative to VCCST/VCCSTG.

On PCH rails, for power up, all Primary rails should ramp within 80ms of each other. For power down, there are no explicit timing requirements/relationships between the various Primary Well voltages on power down, but it is required that all Primary Well voltage regulators stop regulation simultaneously based on SLP\_SUS# assertion. The power down sequencing should not be staggered from one VR to the next. Natural variance between VRs disabling due to differences in voltage regulator disable time is acceptable on the order of tens of microseconds. It is required that all rails ramp down within tPCH35.

For surprise power down requirements, refer [Surprise Power Down Sequencing Considerations](#) on page 462 for assumptions.

### **RSMRST#/DSW\_PWROK Special Requirements**

1. When the system is powered off (G3), DSW\_PWROK and RSMRST# must not glitch from their Low states while the corresponding PCH rails are not powered or are below normal operating voltage specifications to ensure RTC corruption does not happen.
2. When a system is in S0-S5 state and not entering a Deep Sx, the RSMRST# may only be driven low if the DSW\_PWROK is also driven low at the same time (by an external controller such as EC). Failure to meet this requirement may result in unexpected PCH behavior, including failure to boot (which may only be recovered through a G3 cycling) and possible RTC corruption.
3. RSMRST# must always be driven low before any of the PRIMARY rails fall below the lower end of their tolerance band. This is true for all power states transitions including emergency power loss.

### DSW\_PWROK Min LOW Time during Cycling

DSW\_PWROK de-assertion min low time is 100ms. The platform must then follow the normal power sequence (normal G3 exit sequence). Platform must ensure that all the PCH PRIM rails reach 200mV or less, within tPCH35 timing of the falling edge of SLP\_SUS#. Refer to [Table 231](#) on page 449.

### RTEST# (RTCRST#) Min LOW Time during Cycling

For RTEST# (RTCRST#) de-assertion min low time is 100ms, after the min time platform must follow the normal power sequence (normal G3 exit sequence).

### Surprise Power Down Sequencing Considerations

Surprise power down events will be treated slightly differently on Tiger Lake PCH compared to past generation platforms. The main goal of the various power down timing specification such as tPCH10, tPCH12, tPCH14, etc., is to ensure proper isolation between the associated power well and the RTC well to guarantee that RTC contents are not accidentally corrupted. There are many events that could cause a surprise power down. The following is a short list of some events, but is not exhaustive:

- VR failure (over current, over voltage, IC failure, etc.)
- AC removal with no DC Battery present
- Removal of the primary battery

Properly designed platforms generally should not be experiencing VR failures of any kind; therefore the focus of this section is on the unexpected power removal caused by user interaction, which could be an end user, factory technicians and system level induced power down that removes all power from PCH.

To ensure RTC is not corrupted, the platform must de-assert the appropriate power good signals BEFORE the rails go out of their defined tolerance range. This implies that the platform should monitor the highest voltage available which is usually the main power supply like the battery voltage to determine when it has dropped too low and VR failure/shutdown is eminent. At that point, the PCH power good signals (PCH\_PWROK, RSMRST#, DSW\_PWROK) should be driven Low before their associated rails turn off and droop below the defined tolerance.

Finally, regardless of the reason, any time that SLP\_SUS# is taken low, the platform is responsible for ensuring that tCPH10, 12, and 14 are met. Additionally, once RSMRST# is taken low, the platform is responsible for taking the system to G3 before attempting a restart. See RSMRST# / DSW\_PWROK Special Requirements for details regarding RSMRST# and DSW\_PWROK requirements.

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#### NOTE

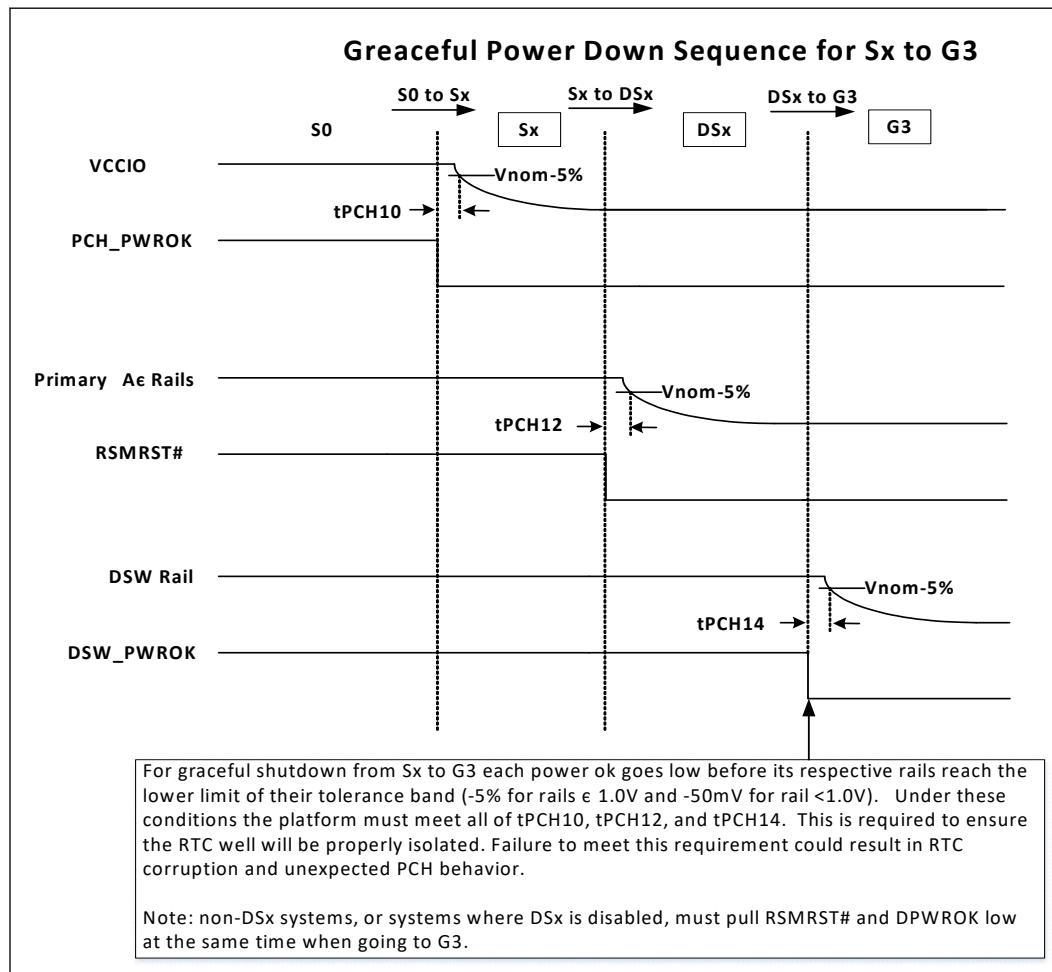
For these cases, de-assertion of DSW\_PWROK and RSMRST# signal is sufficient to activate isolation logic for ALL power wells, thus guaranteeing RTC corruption cannot happen, as shown in the below figure.

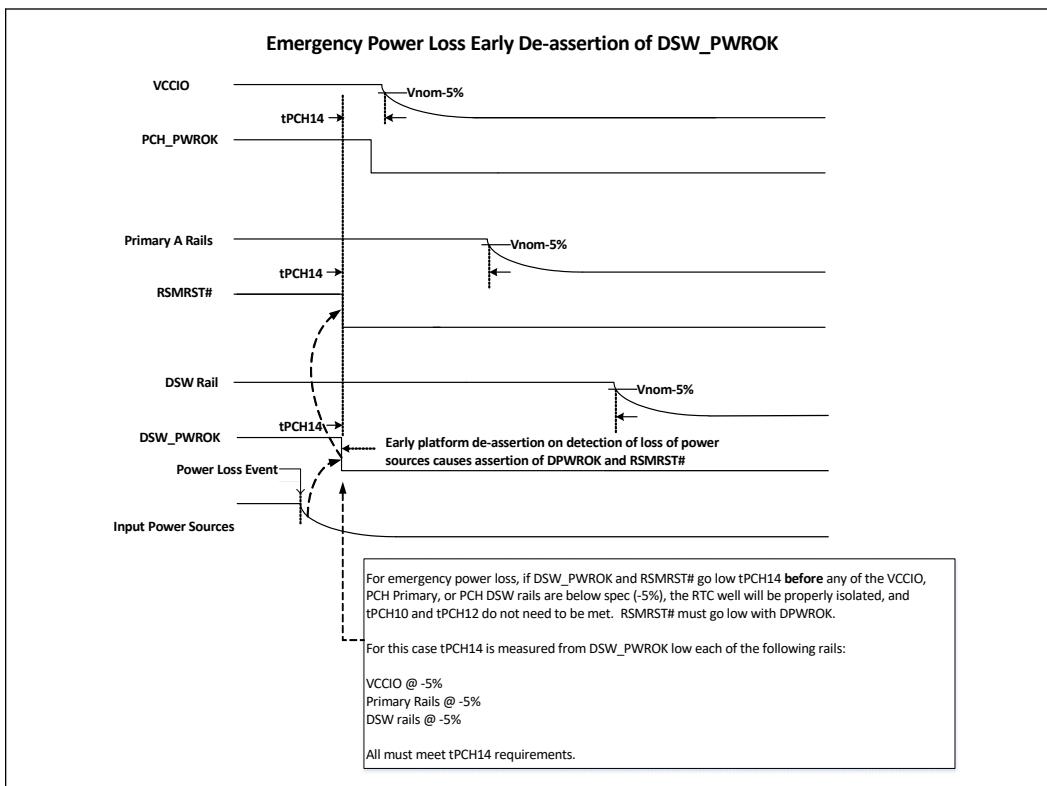
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**NOTE**

As stated previously in [RSMRST# and DSW\\_PWROK Power Down Design Requirement](#) on page 431, it is not permissible to take DSW\_PWROK low without taking RSMRST# low when NOT entering a DSx state. If the platform is designed to take DSW\_PWROK low on emergency power loss, it must also take RSMRST# low at the same time, refer the figure below.

**Figure 259. DSW\_PWROK Requirement for Power Loss**





### eSPI Considerations for Sequencing

In general, eSPI support does not have any major impact to power sequencing requirements. However, there are a few behavioral differences worth noting that could have side effects to platform behavior that should be considered.

With eSPI, the EC may or may not take in or drive physical pins that historically would have been supported by the PCH. The values of these signals (ex. SLP\_S4#) are tunneled over the eSPI interface between the PCH / EC as virtual wires. If the EC is using a combination of hard signals from the PCH and Virtual Wires over eSPI, there is no guarantee of relative timing between the two signal types, other than the hard signals will change state first.

Only the physical signals directly on the PCH are guaranteed to refer the PCH-defined timing relationships. Example, SLP\_S4# de-assertion. SLP\_S3# de-assertion relationship is defined as 30us for the physical pins but could be shorter for the virtual wire relationship on the EC.

SUSPWRDNACK at RSMRST# de-assertion for eSPI designs please ignore eSPI SUSPWRDNACK Virtual Wire (VW) until after receiving the first 1->0 transition, then after that it is valid.

#### 10.12.8

### Glitch Free Design Options and Recommendations

Platform signals are not guaranteed to be glitch free on power up of the DSW and PRIMARY rails. The platform may mitigate glitches on key signals by adding a pull up or pull down as described [PCH Signal Glitch Free Implementation Requirements](#) on page 195

## 10.13 S0ix State Definitions

### NOTE

Refer Tiger Lake Platform S0ix Technical Advisory (#630692) for more information

S0ix is a system low power state. The PCH is self-optimizing for the lowest power when in S0ix. But, the PCH needs platform information to make the best decisions when self-optimizing.

This section describes how the internal PCH states and platform configuration combine to optimize PCH power when in S0ix.

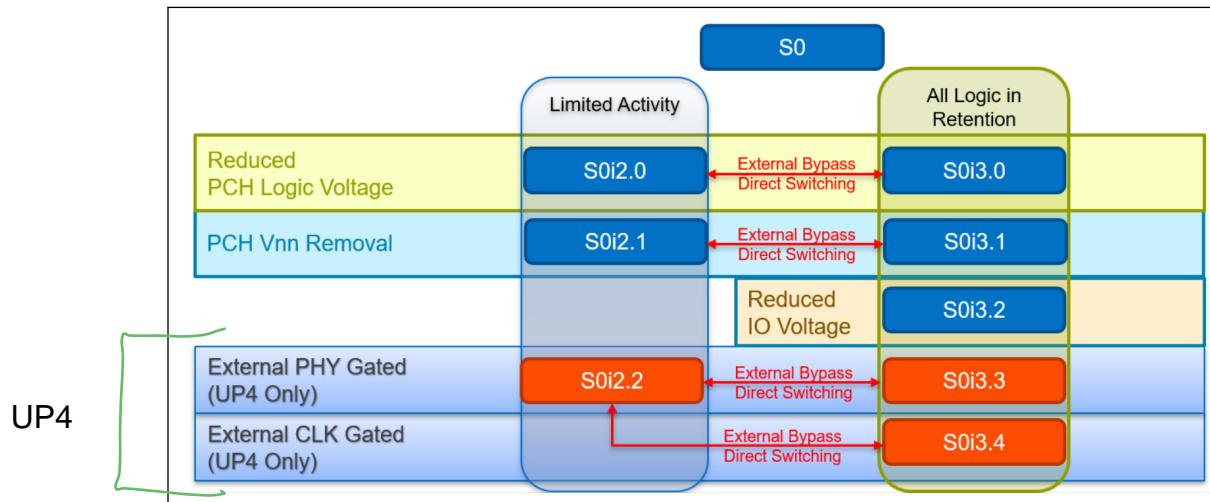
S0ix is used to indicate when the CPU + PCH has achieved a low power state

- S0i2 denotes a state in which certain IPs may be active
- S0i3 denotes a state in which all IPs are idle
- In certain scenarios, it is possible to dynamically move between S0i2 & S0i3
  - This is also referred to as **Direct Switching**, and allows switching between S0ix states.
  - To enable Direct Switching, external bypass VRs are needed

S0ix Substates are additional power actions taken when certain criteria are met.

- Certain device states, latency requirements , and platform components may be required

**Figure 260. S0ix State Definitions**



**Table 233. S0ix State Actions and Power Impact**

State	Actions
S0ix.0	Vnn voltage reduction
S0ix.1	Additional Vnn domains powered off
<i>continued...</i>	

State	Actions
S0ix.0	Vnn voltage reduction
S0ix.1	Additional Vnn domains powered off
S0i2.2	Platform phy PG enabled (UP4) (~2 mW Power Benefit)
S0i3.2	V1p05 voltage reduction
S0i3.3	Platform phy PG enabled (UP4) (~2 mW Power Benefit)

Feature	Incremental Power Benefit
* Vnn Ext Bypass @ 0.78V	See notes
*V1p05 Ext Bypass @ 1.05V	See notes

### NOTES

- For the bypass rails, the value of the bypass rails is highly dependent on the load on those rails. One could assume an ~60-75% efficiency if internal regulators are used. (Voltage margining for bypass rails can offer better power savings in S0ix)
- UP4 platform external PHY PG refers to VCCMPHYGT\_1P05 (+VCC\_MODPHY), which is gated by PCH EXT\_PWR\_GATE# (GPP\_F20)
- UP4 External CLK PG refers to VCCPRIM\_GATED\_1P05 (+VCC\_ISCLK), which is gated by PCH EXT\_PWR\_GATE2# (GPP\_F21).

**Table 234. Basic Minimum Requirements Table (PCH)**

CPU/Devices	CPU	UFS	LPSS	XHCI*	XDCI*	THC	GBE Nahum	CSME	AUDIO	ISH	CNVI	DISPLAY	PCIe	SATA	ModPHY
<b>Condition</b>	C10	D3	D3	D3	D3	D3	Power Gated	Power Gated	Dx	D0lx	ON/OFF	D3/L23	D3	CORE/SUS PG	
<b>S0i2.0</b>	C10	D3	D3	D3	D3	D3	Power Gated	Power Gated	D0 (WoV / LPA)	D0l1	Active	ON	L1.1	D0	Core PG
<b>S0i2.1</b>	C10	D3	D3	D3	D3	D3	Power Gated	Power Gated	D0 (WoV / LPA)	D0l1	Active	ON	D3/L23	D3	Core PG
<b>S0i2.2</b>	C10	D3	D3	D3	D3	D3	Power Gated	Power Gated	D0 (WoV / LPA)	D0l1	Active	ON	D3/L23	D3	SUS PG
<b>S0i3.0</b>	C10	D3	D3	D3	D3	D3	Power Gated	Power Gated	D3	D0l2	Idle	OFF	L1.1	D0	Core PG
<b>S0i3.1</b>	C10	D3	D3	D3	D3	D3	Power Gated	Power Gated	D3	D0l2	Idle	OFF	D3/L23	D3	Core PG
<b>S0i3.2</b>	C10	D3	D3	D3	D3	D3	Power Gated	Power Gated	D3	D0l2	Idle	OFF	D3/L23	D3	Core PG
<b>S0i3.3</b>	C10	D3	D3	D3	D3	D3	Power Gated	Power Gated	D3	D0l2	Idle	OFF	D3/L23	D3	SUS PG

*Notes:*

- PCIe L23 State can be achieved by enabling D3 Cold support
- PCIe L1.1/L1.2 state can be achieved by enabling D3 Hot support
- Not all constraints (e.g., LTR, timers, internal hysteresis, etc.) are listed

**Table 235. Basic Minimum Requirements Table (CPU)**

CPU/Devices	CPU	TCSS TBT DMA	TCSS XHCI	TCSS PCIe	PEG (CPU PCIe)
<b>Condition</b>	C10	D3	D3	D3/L23	D3/L23
<b>S0i2.0</b>	C10	D3	D3	L1	L1.2

*continued...*

CPU/Devices	CPU	TCSS TBT DMA	TCSS XHCI	TCSS PCIe	PEG (CPU PCIe)
<b>S0i2.1</b>	C10	D3	D3	D3/L23	D3/L23
<b>S0i2.2</b>	C10	D3	D3	D3/L23	D3/L23
<b>S0i3.0</b>	C10	D3	D3	L1	L1.2
<b>S0i3.1</b>	C10	D3	D3	D3/L23	D3/L23
<b>S0i3.2</b>	C10	D3	D3	D3/L23	D3/L23
<b>S0i3.3</b>	C10	D3	D3	D3/L23	D3/L23

**Notes:**

- PCIe L23 State can be achieved by enabling D3 Cold support
- PCIe L1.1/L1.2 state can be achieved by enabling D3 Hot support
- Not all constraints (e.g., LTR, timers, internal hysteresis, etc.) are listed

### S0ix State Quick Reference Guide

#### For UP3

- With External Bypass VRs and Direct Switching supported, the lowest S0ix state that is recommended (for optimal power) is S0i3.1. If you do not use CNVi or ISH, S0i3.2 can be achieved.
- Without the External Bypass VRs and/or Direct Switching, the lowest power state that is recommended is S0i2.1.
- UP3 is not able to achieve S0i2.2 and S0i3.3.

#### For UP4

- With External Bypass VRs and Direct Switching supported, the lowest S0ix state that is recommended (for optimal power) is S0i3.3. This is assuming no USB3 Type A ports, no C-link used, no SMBus features used and PHY is power gated.
- Without the External Bypass VRs and/or Direct Switching, the lowest power state that is recommended is S0i2.2. This is assuming no USB3 Type A ports and PHY is power gated. Otherwise, can achieve S0i2.1.
- 

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#### NOTE

It may be possible to achieve lower power states than recommended. Due to stability, however, the recommended power state may have a lower overall power than would be observed using the lowest possible state

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### S0ix Optimization Guidelines

Based on the reply to these questions about your platform, follow the optimization guidance instructions below.

Q 1	Does your platform use Integrated Connectivity (CNVi)?	Yes/No
Q 2	Does your platform use the Integrated Sensor Hub (ISH)?	Yes/No
Q 3	Does your platform have USB3 Type A ports?	Yes/No
<i>continued...</i>		

Q 4	Does your platform use C-Link with an External Wi-Fi card?	Yes/No
Q 5	Does your platform use any of the following SMBus features? <ul style="list-style-type: none"> <li>• SMBus Controller as Slave</li> <li>• SMBus Wake</li> <li>• SMBus Device Hot Plug</li> <li>• TCO Slave</li> </ul>	Yes/No
Q 6	Does your platform have the External PHY PG (UP4 Only)?	Yes/No

### Instructions

- If the cell is marked "YES": Enable the state in the below row, ONLY if you answered "YES" to the question in the above column
- If a cell is marked "NO": Enable the state in the below row, ONLY if you answered "NO" to the question in the above column
- If a cell is marked "-": Ignore this question when deciding whether to enable or disable the state in this row.

**Table 236. External Bypass Supported with Direct Switching**

State Enable	Q1 CNVi	Q2 ISH	Q3 Type A	Q4 C-Link	Q5 SMBus	Q6 PHY PG
S0i2.0	Always Enable					
S0i2.1	Always Enable					
S0i2.2	-	-	NO	-	-	YES
S0i3.0	Always Enable					
S0i3.1	Always Enable					
S0i3.2	NO	NO	-	-	-	-
S0i3.3	-	-	NO	-	-	YES

**Table 237. No Direct Switching or No External Bypass Supported**

State Enable	Q1 CNVi	Q2 ISH	Q3 Type A	Q4 C-Link	Q5 SMBus	Q6 PHY PG
S0i2.0	Always Enable					
S0i2.1	Always Enable					
S0i2.2	-	-	NO	-	-	YES
S0i3.0	NO	NO	-	-	-	-
S0i3.1	NO	NO	-	-	-	-
S0i3.2	NO	NO	-	-	-	-
S0i3.3	NO	NO	NO	-	-	YES

### Voltage Margining

Voltage margining allows bypass VRs to reduce their voltages depending on S0i3.x states. To enable this feature, VNN\_CTRL and V1P05\_CTRL GPIO pins should be configured. This feature can reduce power in S0ix states.

Voltage Margining Feature	Voltage Reduction
Vnn Ext Bypass margining using VNN_CTRL	0.78V -> 0.7V
V1p05 Ext Bypass margining using V1P05_CTRL	1.05v -> 0.96v

<b>Voltage Margining Feature</b>	<b>Voltage Reduction</b>
Vnn Ext Bypass margining using VNN_CTRL	0.78V -> 0.7V
V1p05 Ext Bypass margining using V1P05_CTRL	1.05v -> 0.96v

## 11.0 Platform Instrumentation for Power Measurement and Correlation

This chapter provides instrumentation guidelines for measuring device power on the Tiger Lake platform. As platform battery life targets becomes more important, it is necessary to instrument Tiger Lake platforms (especially on pre-production builds) to accurately measure power and debug power mis-correlation issues with battery life with the targets. This process also helps to identify opportunities for platform power optimization.

Flexible Instrumented Platform, FIP is a recommended design for test used for power optimization. In order to instrument the platform, it is required to plan for sense resistors (power measurement resistors or PMR) on key voltage rails.

### 11.1 Voltage Rail Instrumentation Guidelines

The following table outlines the minimal set of voltage rails that are recommended for instrumentation to measure and debug platform power. This list isolates all the main SOC rails and other key components on the platform. We recommend providing a means to isolate all subsystems on the platform with current sense resistors. A comprehensive list of the power measurement resistors (PMR) on key voltage rails will be utilized in executing the platform power optimization design for test, FIP in Section [Power Instrumentation Coverage Recommendation](#). This recommended as full coverage as possible securing any access needed to analyze power as power management issue can be design dependent that is hard to predict which will be the gating part.

**Table 238. Recommended Voltage Rails for Sense Resistor Addition**

Voltage Rail	Voltage Rail Description	Domain
+VBATA	Battery Rail	
+VCCIN	Output of VccIN Rail (IMVP-9)	CPU and PCH
+VCCIN_AUX	Output of VccIN_Aux rail	
+VCCPRIM_1P8	1.8V Primary well	
+ VCCPRIM_3P3	3.3V Primary well	
+VCC_VNNEXT_1P05 (VNN_BYPASS)	Output of VNN CS/Sx bypass VR (power optimized power map)	
+VCC_V1P05EXT_1P05 (V1P05_BYPASS)	Output of V1.05 CS/Sx bypass VR (power optimized power map)	
+VCC1P8A (TCSS and AGSH)	Type C Sub system and processor analog supply	
+VCCDSW_3P3	Deep Sleep well	
+V_VDDQ	Output of V_VDDQ rail which includes both CPU+DRAM component	CPU+DRAM

*continued...*

Voltage Rail	Voltage Rail Description	Domain
+VTT_VR	DRAM termination	DRAM
+V2.5U	DDR4	
+V_VDDQ_Tx	LPDDR4x DDRIO Buffers	
+V1.8Dx_WIFI/Modem	Wi-Fi/BT/Modem	Peripheral devices (Will vary by design)
+V3.3Dx_WIFI/Modem	Wi-Fi/BT/Modem	
Audio/Sensors	Audio	
Display	eDP Panel	
EC	Embedded Controller Rail	
Sensors	Sensor Hub Rail	
Storage	Storage Rail	
Camera	Camera Rail	
SD Card	SD card Reader	
Display Backlight	Backlight Rail	
Touch Panel	Touch Panel	

## 11.2

## Sense Resistor Implementation Details

Here are some placement guidelines recommended for sense resistors on the platform:

- Use 1% tolerance sense resistors
- Use smallest sense resistor package possible that can still meet the maximum  $I^2R$
- Losses that the resistor must dissipate.
- Place sense resistors close to destination or device endpoint
- Place sense resistors away from switching sources such as buck regulators and oscillators.
- Make sure that the expected droop across the resistor will not violate the Vmin of the components it is powering.

## 11.3

## Flexible Instrumented Platform (FIP) Design

Power instrumentation is vital in measuring and analyzing sub-subsystem power to enable full-system power optimization; Power Sequencing and Low speed signal test for system functionality test/verification and debug. Current system instrumentation technique involves connecting sense resistors on the board to the Data Acquisition Device (DAQ) manually for system power optimization and system functionality verification/debug. This method has several pitfalls and carries risks such as tedious manual re-work, quality concerns, and potential board damage. In this paper we introduce a new technique of power instrumentation called the Flexible Instrumentation Platform (FIP) design. The FIP design offers many advantages over existing methods such as one-time effort requiring no manual rework, no risk of shipping damage and shorter setup time.



### 11.3.1 Background

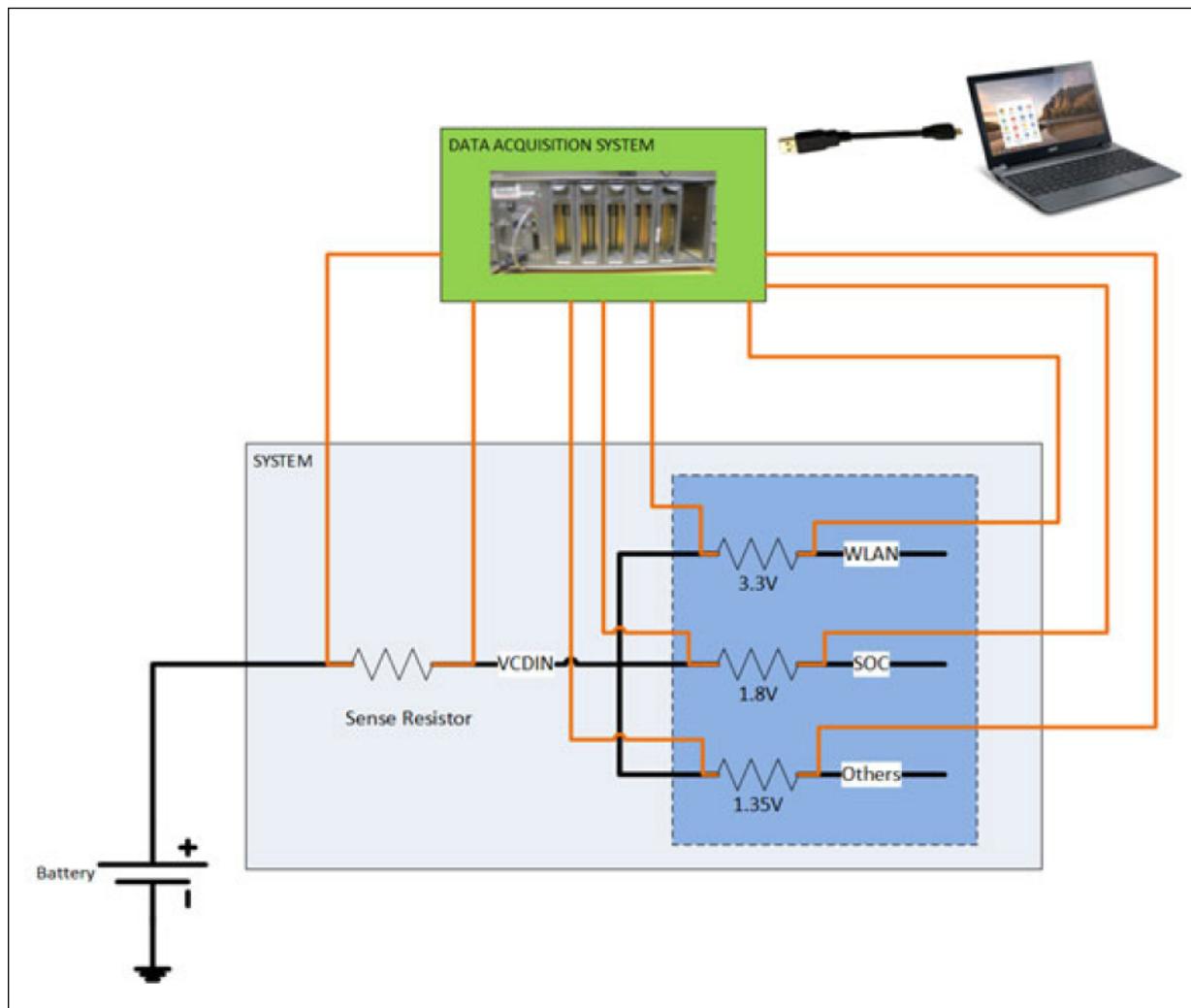
Sense resistors and Power/Electrical test access are typically not part of the production design. Hence power instrumentation and low speed electrical signal test access technique involve manually connecting sense resistors on the board and using wires connected to a pod on the DAQ for measuring current, voltage and power consumption as well as to use a Scope/Digital multi-meter for low speed signal test.

As depicted in Figures below, existing instrumentation introduces several challenges:

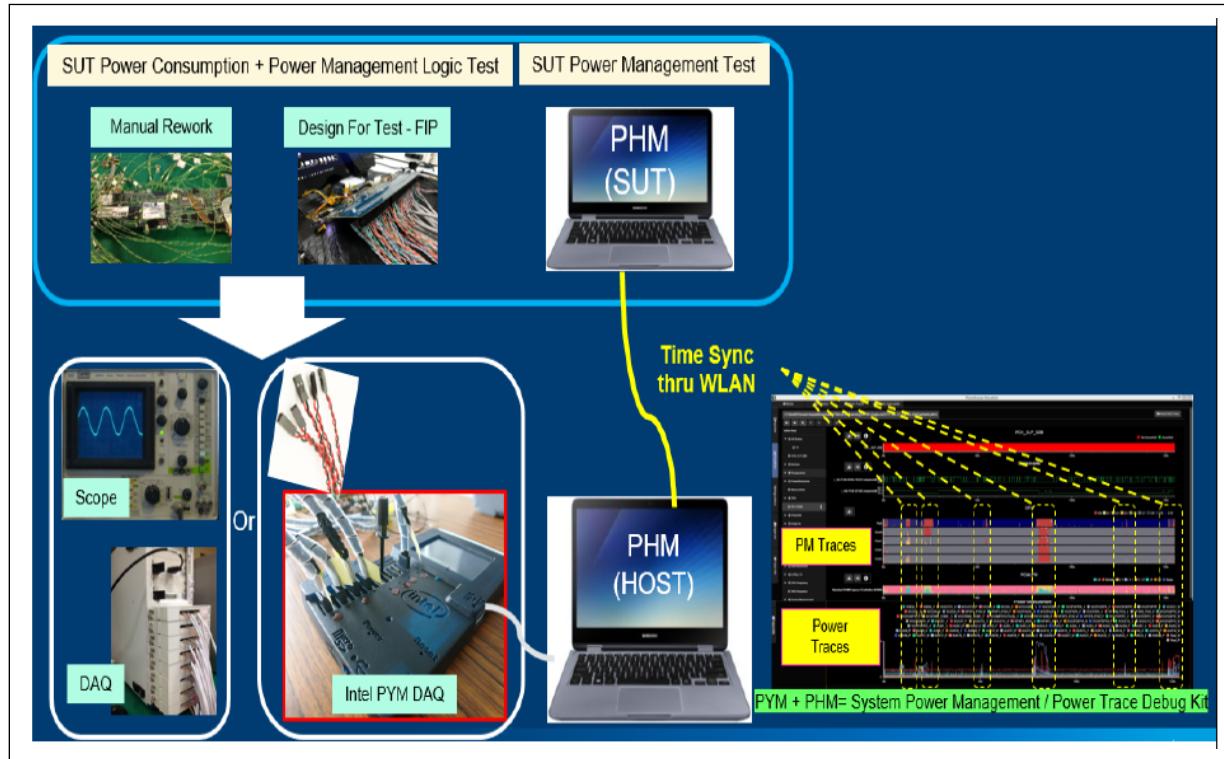
- Manual rework time: instrumentation takes three days best case for the whole board with one dedicated labor. Also this rework has to be done for each board.
- Quality concern: potential lack of quality in soldering can affect power measurement accuracy.
- Potential risk: Board damage caused by rework at limited board and SOC sample stages that may be gating product launch without tuning to extend battery life to meet/exceed target
- Portability Issues: the instrumented platforms connected to pods are sensitive to damage such as wires pulling pads off. This affects ability to move or transport instrumented boards without damage.
- Setup time: connecting individual wires to DAQ takes time and depending on the number of rails/ channels, it can take half a day or more.

Additionally, customers that do take the time to add power instrumentation to their designs do not include consistent accurate labeling to the wires. Also they tend to hot glue the sense resistor location making identification very difficult, sometimes impossible. The FIP implementation proposed here reduces the requirement for power measurement teams to become intimately familiar with the customer design for setup, therefore enabling full focus on software power optimization.

Figure 261. System Instrumentation Block Diagram



**Figure 262. Power Instrumentation Setup**



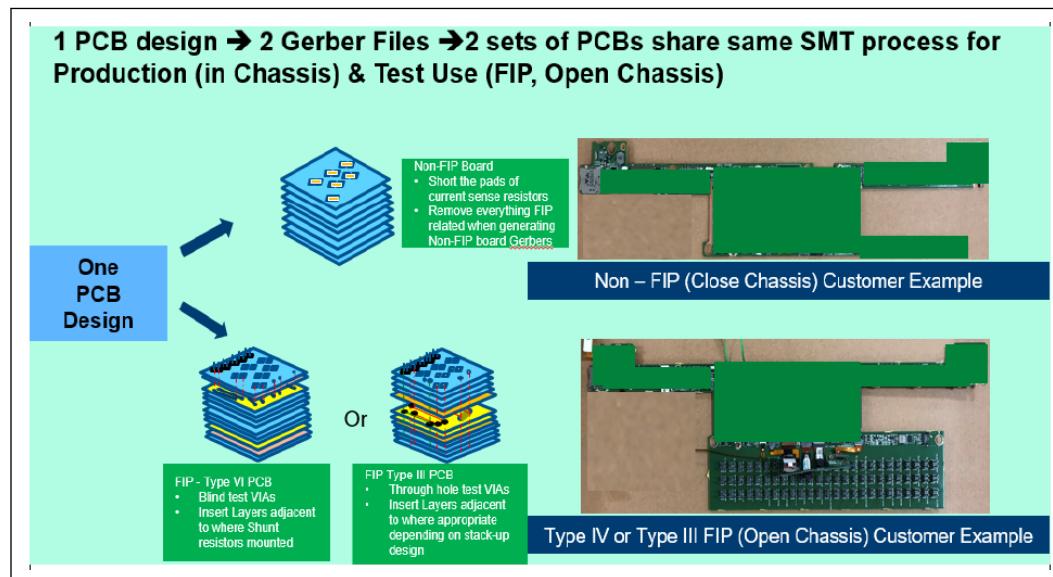
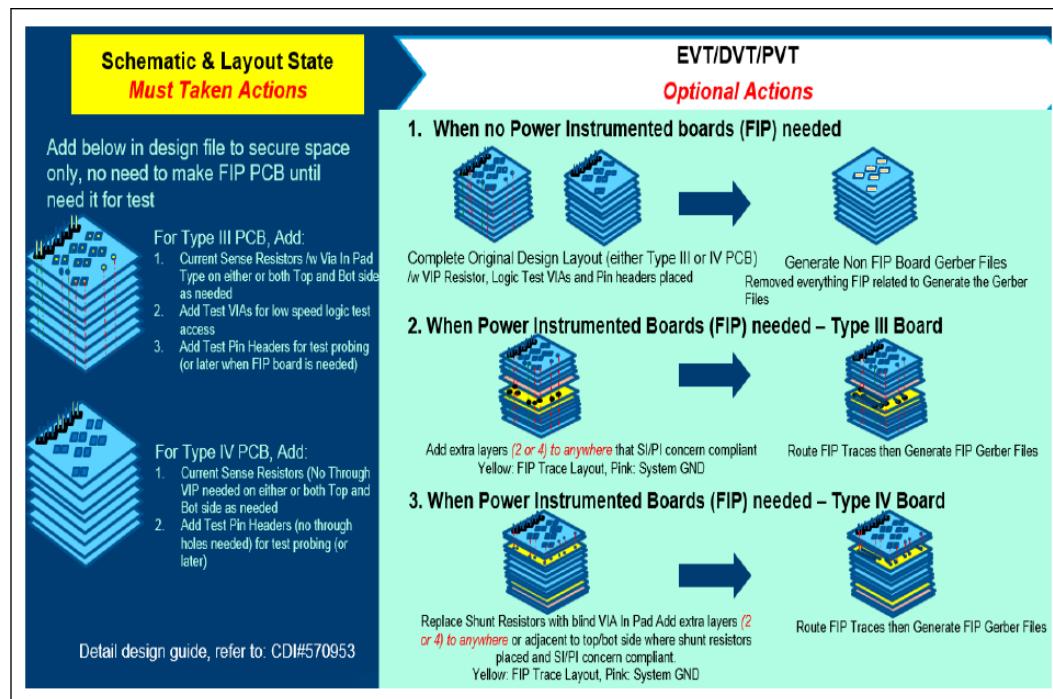
### 11.3.2 Overview

This section introduces a new instrumentation design proposal. FIP design minimizes the risk introduced by the current instrumentation techniques by adding extra layers and routing the instrumented wires on it, depending on the space needed, the PCB may be extended to allow test pin headers or within the original PCB space. The board can then be connected via twisted pair wires for differential voltage sense cables to the DAQ for power measurements and scope for low speed electrical signal measurements. Figure below shows an overview of the FIP design.

FIP involves adding the following components with suggested preparation time lines as the following:

- Current sense resistor symbols with FIP (Via in Pad) and Non-FIP (removed with short traces) options
- Logic Test Via symbol with FIP and Non-FIP (removed)
- Four or Two extra PCB layers
- FIP trace routing
- Industry flexible DuPont header connector
- Flexible extended PCB space (project dependent)

The FIP adoption and implementation flow is shown in [Figure 264](#) on page 475

**Figure 263. Flexible Instrumentation Overview****Figure 264. FIP Adoption Flow and Critical Timing**

### 11.3.3 FIP Design Details

This solution is FIP a design with detachable layout solution with all test trace layout to connector for connection to the DAQ/ scope including below. Total setup time is approximately less than one day for complete system power measurements and risk of damaging the board via reworks or setup is eliminated.

1. Complete system power rail instrumentation.
2. Low speed electrical signal test access.

### FIP Details and Steps

The solution design involves a detachable PCB layout and Gerber method. This package involves designing one PCB layout and generating 2 Gerber files for manufacturing 2 PCBs, one as non-FIP, and the other as a FIP design. The non-FIP design will not have any current sense resistors, and can be ~1USD/piece saving. The FIP PCB can be attached/ removed to the board at any design stage without impact to the original board design. There are no additional design costs nor any rework resource costs associated with addition of power instrumentation to the non-FIP designs. We also avoid the risk of damaging boards by manual rework at limited sample stages and risk of not able to fully debug/fine-tune system low power to extend battery life before product launch schedule.

The PCB design for the two different PCB types is given below:

1. Type 3 PCB
2. HDI PCB

Both recommend to have VIP (Via in Pad) sense resistors: N Layer stackup vs. N+4 L (bigger board size to hold a connector). If the number of boards needed is within manufacturer's sample quantity, then there is a potential to not incur any additional costs as some manufacturer do not charge for samples.

1. The design steps for the FIP are:
2. Add 4x layer to core of the original design
3. Define the FIP symbol (Connectors, Current Sense Resistors, Impedance Coupon for inner layer)
4. PCB placement
5. Route System Traces and FIP traces
6. Generate FIP Gerber and Non-FIP Gerber

- **STEP 1: Add 4x Layer to Core of Original Design**

The PCB stack-up solution is defined by consulting with the project SI and PI engineers. The FIP layers design should have the least impact to the system base design in terms of impedance control, signal ground/ power referencing especially on high speed I/O signals and should avoid cross talk. A PCB stack-up design proposal adding the 4x layer to the original design is shown in Tables below. Table below shows a base design example and [Table 240](#) on page 477 shows the SIP proposal for that base design.

**Table 239. Base Design Proposal**

Base Design			
Layer	Layer Thickness (in mm)		Signal
	Layer	Insulator	
L1	1.55	2.7	Signal
L2	0.6	4	GND
L3	0.6	4	Signal

*continued...*

Base Design			
Layer	Layer Thickness (in mm)		Signal
	Layer	Insulator	
L4	0.6	4	VCC
L5	0.6	4	Signal (only low speed signals will be routed here)/GND
L6	0.6	4	Signal
L7	0.6	2.7	GND
L8	1.55	-	Signal
	Total Thickness	32.1mm	

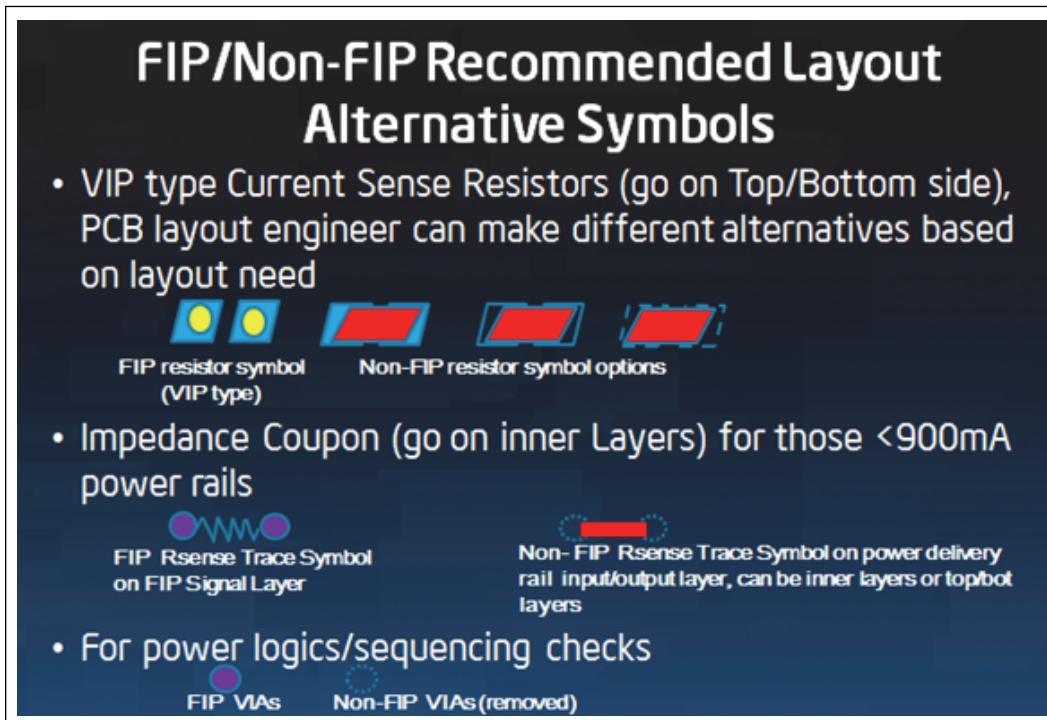
**Table 240. FIP Design Proposal (with 4x layer addition)**

SIP Design			
Layer	Layer Thickness (in mm)		Signal
	Layer	Insulator	
L1	1.55	2.7	Signal
L2	0.6	4	GND
L3	0.6	4	Signal
L4	0.6	4	VCC
L5	0.6	4	FIP-GND (connect to system ground as defined by the layout rules)
L6	0.6	4	FIP-S1
L7	0.6	4	FIP-S2
L8	1	-	FIP-GND (connect to the system ground as defined by the layout rules)
L9	0.6	4	Signal (only low speed signals will be routed here)
L10	0.6	4	Signal
L11	0.6	4	GND
L12	1.55	2.7	Signal
	Total Thickness	46.25mm	

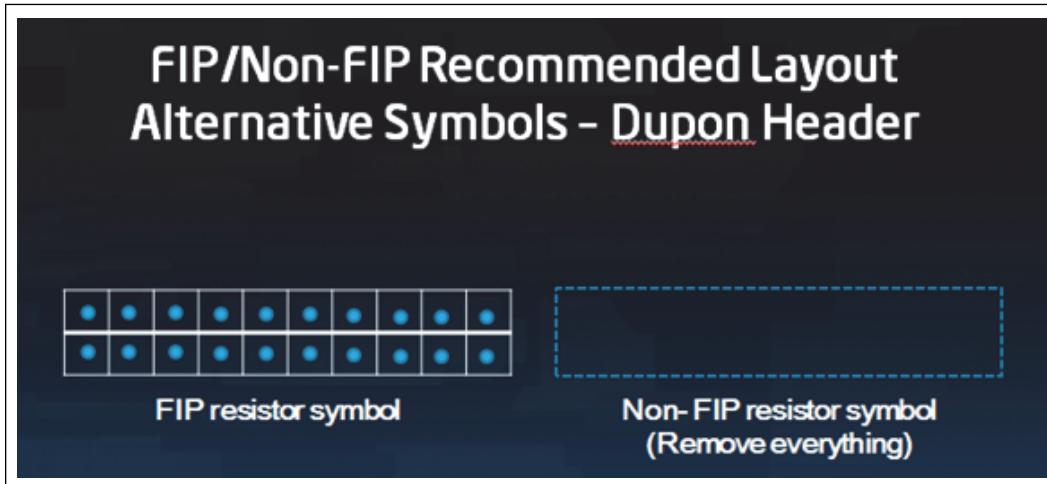
- STEP 2: Define FIP Symbols**

Establish a layout symbol library for the FIP and define the FIP resistor symbol and non-FIP resistor symbol options. Figure below shows the FIP/ non-FIP symbol design.

**Figure 265. FIP/non-FIP Symbol Design Examples-1**



**Figure 266. FIP/non-FIP Symbol Design Examples-2**

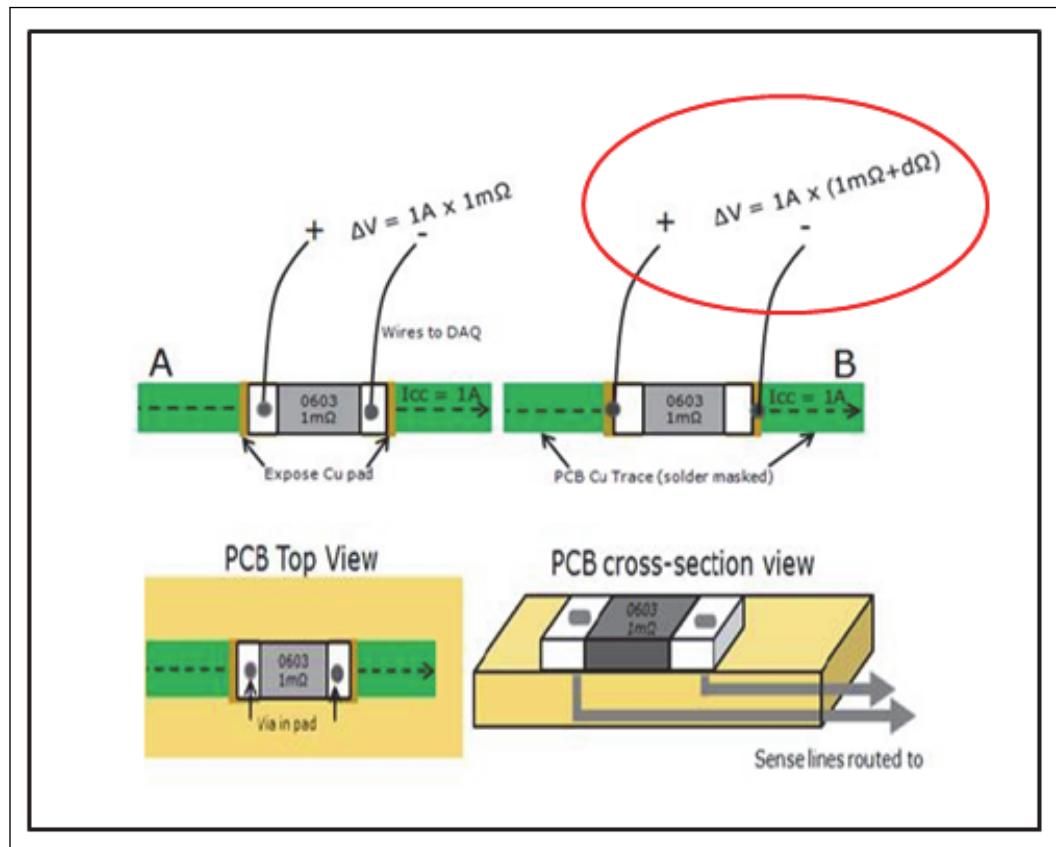


- **STEP 3: PCB Placement**

Secure the sense resistors with via in the PCB placement stage. Via creates a precise contact point between the wire and the sense resistor. The placement of any via on the FIP board is critical since a variation of via placement from one site to next will result in marginal variations in the total resistance used to measure the IR drop and current. This in turn results in discrepancies in the power measurement data that impacts the power data quality as shown in Figure 53-9. Conclusion is, VIP sense resistors should be used as described in Voltage

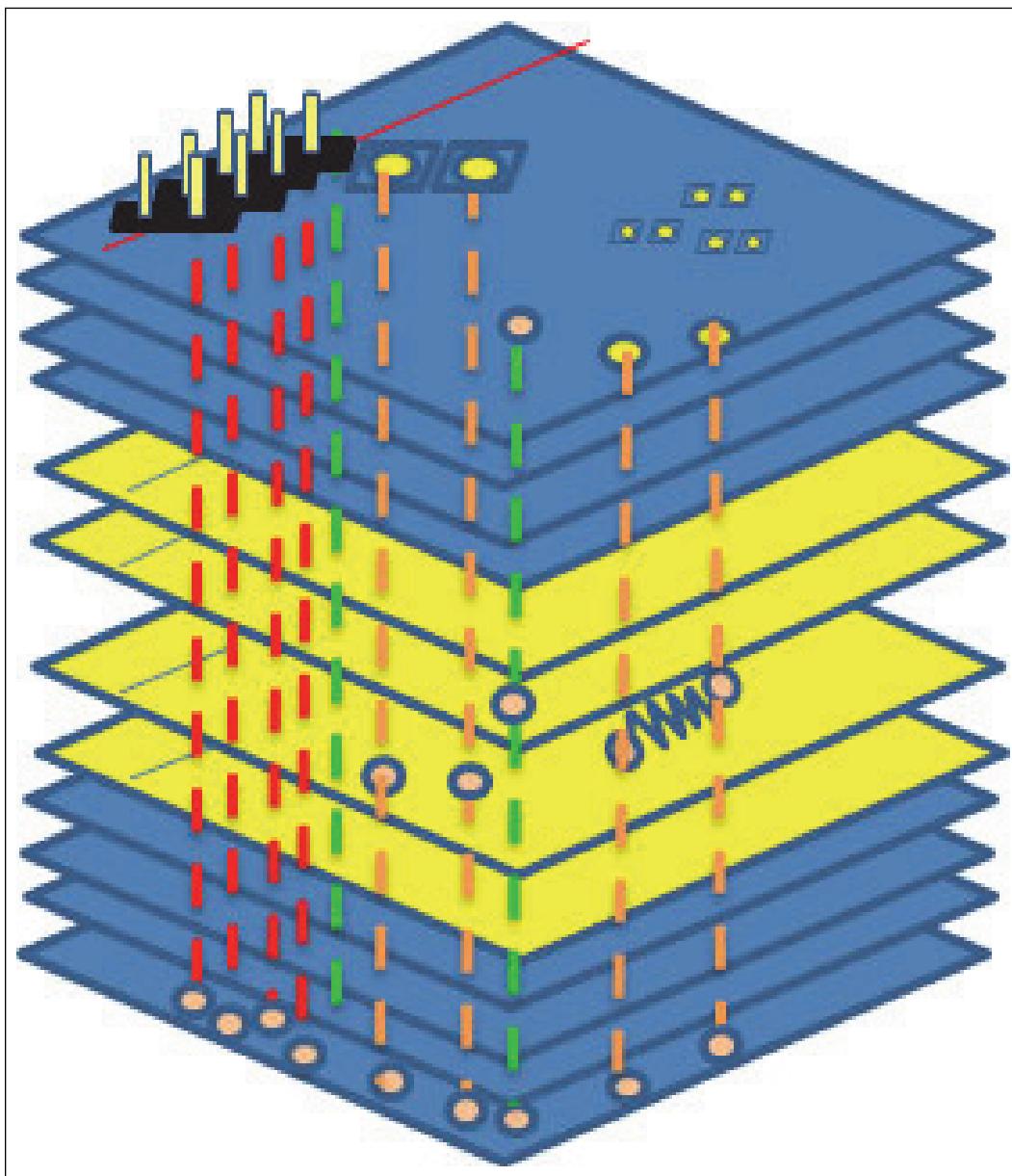
Regulator in Platform Design Guide excelsheet for library generation. Test vias alternative symbols should be generated for low speed signals for FIP and Non-FIP Gerbers.

**Figure 267. Variations in IR Drop due to Via Placement**



- STEP 4: Route System and FIP Traces**

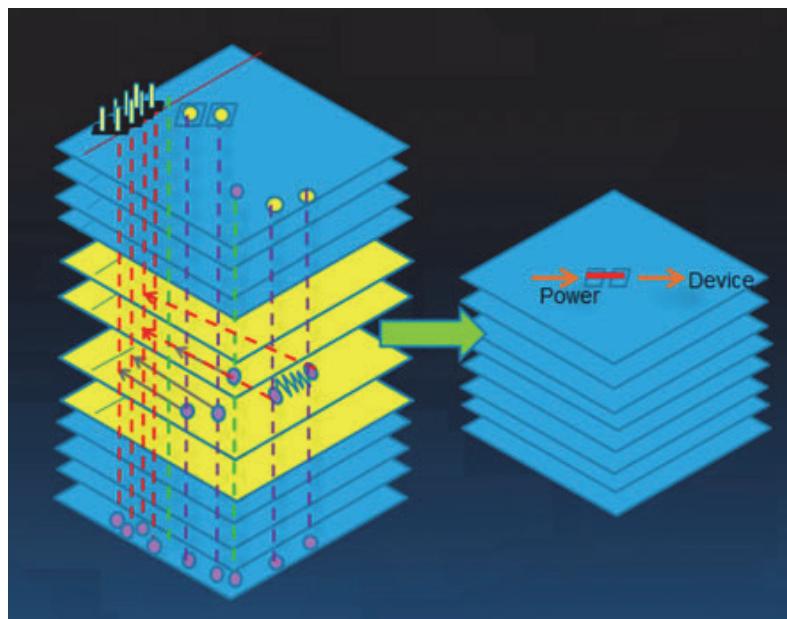
Place the FIP resistors with VIP type and FIP Vias at placement stage and secure the space with VIAs (through Vias and/or Blind/Buried Vias), Route and complete the system traces prior routing the FIP traces. Figure below shows the steps.

**Figure 268. PCB Placement**

- STEP 5: Generate FIP Gerber and Non-FIP Gerber

After routing the system traces and the FIP traces, the next step is to generate the FIP and non-FIP gerber. In the non-FIP gerber, remove all the FIP layers, FIP vias, FIP connector, F/IP traces, and replace the sense resistor symbol with the alternative symbol for short trace (refer Figure below) and remove the test vias for the non-FIP.

**Figure 269. FIP and Non-FIP Gerber/PCB**



#### 11.3.4 General Guidance for FIP Solution

In order to allow power instrumentation design test in place with minimum efforts, it is critical to have implementation in place at schematics and initial layout placement states.

- Prepare schematics to include power instrumentation design for test, current sense resistors, test vias and test pin headers.
- Place current sense resistors (if Type-III PCB, ensure it's VIP type), test vias and test pin headers when initial layout placement state to secure the space for FIP layout when FIP boards needed at later design stages.

For details on layout guidance for FIP design, refer #570953.

### 11.4

#### Power Instrumentation Coverage Recommendation

If the system is exceeding the expected power target, any platform ingredient could be causing the issue. Detailed power breakdown and access to power management signals will be needed for debug. It is best to provide as much power instrumentation coverage as possible to support power analysis and debug. This, theory is the same manual rework as well as for FIP designs. Any component that is not covered could risk the ability to identifying power related issues, and making debug difficult. It may make sense to gang multiple related components onto one resistor if space is a concern. For example, combining two retimers onto one resistor.

Tiger Lake-UP3/UP4 RVP Power Instrumentation resistors as reference is listed on Table below. Be sure to size resistor values properly and isolate subsystems as appropriate for your design.



Table 241. PMR Priority List for FIP Design Solution

DDR4 RVP References					Instrumentation Recommendation
Category	Interface	Device/Function	System Rail	Net Name	PMR Value
CPU		VCCIN Die sense	VCCIN	VCC_VCCIN_SENSE_P	
		VCCIN_AUX Die sense	VCCIN_AUX	VCCIN_AUX_VCCSENSE	
		Test Point	TP	TP_A_VSSA_SENSE	
		Test Point	TP	TP_A_VSSIO_SENSE	
		Test Point	TP	TP_SPARE1_SENSE_N	
		Test Point	TP	TP_SPARE2_SENSE_N	
		+VBATA		VBATA_SENSE_POS	2m
		+VCCIN (PH1)		VCCIN_PH1_SENSE_POS J213315	2m
		+VCCIN (PH2)		VCCIN_PH2_SENSE_POS	2m
		+VCCIN (PH3)		VCCIN_PH3_SENSE_POS	2m
		+VCCIN (PH4)		VCCIN_PH4_SENSE_POS	2m
		+VCCIN_AUX		VCCIN_AUX_SENSE_POS	2m
		+VCCST_CPU		VCCST_CPU_SENSE_POS	5m
		+VCCSTG_CPU		VCCSTG_SENSE_POS	5m
		VCCSFR_SENSE_Neg		VCCSFR_SENSE_POS	10m
		+VDDQ_CPU		VDDQ_CPU_SENSE_POS	2m
		+V_VDDQ_VTT		VTT_LDO_SENSE_POS	10m
		+VDDQ_MEM		VDDQ_MEM_SENSE_POS	2m
		+V1.8U_2.5U_MEM		V1.8U_2.5U_MEM_SENSE_POS	5m
		+VCCSFR_OC		VCCSFR_OC_SENSE_POS	10m
		+VDDQ_TX_MEM		VDDQ_TX_MEM_SENSE_POS	5m
PCH		+VCCPRIM_3P3		VCCPRIM_3P3_SENSE_POS	22m
		+VCCPRTC_3P3		VCCPRTC_3P3_SENSE_POS	22m
		+VCCPDSW_3P3		VCCPDSW_3P3A_SENSE_P OS	22m
		+VCCPFUSE_3P3		VCCPGPPR_3P3_1P8_SENS E_POS	22m
		+VCCPGPPR_3P3_1P8		VCCPSPI_3P3_1P8_SENSE _POS	22m
		+VNN_BYPASS		VNN_BYPASS_SENSE_POS	5m
		+VCCPRIM_1P8		VCCPRIM_1P8_SENSE_POS	22m
		+VCCA_CLKLDO_1P8		VCCA_CLKLDO_1P8_SENSE _POS	22m

continued...

DDR4 RVP References					Instrumentation Recommendation
Category	Interface	Device/Function	System Rail	Net Name	PMR Value
			+VCCPFUSE_1P8	VCCPFUSE_1P8_SENSE_POS	22m
			+V1.05A_BYPASS	V1.05A_BYPASS_SENSE_POS	5m
		Test Point	TP		
Storage	EMC	EMC	+V1.8S_EMMC	V1.8S_EMMC_SENSE_POS	10m
		EMC	+V3.3S_EMMC	V3.3S_EMMC_SENSE_POS	10m
	M.2	SSD	+V3.3DX_SLTM_SSD	V3.3DX_SLTM_SSD_SENSE_POS	5m
	SATA Direct	SSD/HDD	+V5.0DX_SSD	V5.0DX_SSD_SENSE_POS	5m
		Camera	+V3.3S_MCSI_CAMER_A	V3.3S_MCSI_CAMERA_SENSE_POS	5m
		Camera	+V1.8S_MCSI_CAMER_A	V1.8S_MCSI_CAMERA_SENSE_POS	22m
		Touch Pad	+V3.3S_TCH_PAD	V3.3S_TCH_PAD_SENSE_POS	5m
		Touch Pad	+V1.8S_TCH_PAD	V1.8S_TCH_PAD_SENSE_POS	10m
Codec		Audio Codec	+V1.8DX_CORE_CODEC	V1.8DX_CORE_CODEC_SENSE_POS	10m
		Audio Codec	+V1.8DX_3.3DX_AUD_DVDD	V1.8DX_3.3DX_AUD_DVDD_SENSE_POS	10m
		Audio Codec	+V1.8DX_3.3DX_AUD_DVDDIO	V1.8DX_3.3DX_AUD_DVDDIO_SENSE_POS	10m
		Audio Codec	+V1.8DX_AUDIO_SDW	V1.8DX_AUDIO_SDW_SENSE_POS	10m
		Audio Codec	+V5DX_AUDIO	V5DX_AUDIO_SENSE_POS	5m
		Audio Codec	+V3.3DX_AUDIO	V3.3DX_AUDIO_SENSE_POS	10m
Card Reader		SD Card	V3.3DX_SDCARD_SENSE_NEG	V3.3DX_SDCARD_SENSE_POS	10m
WWAN		M.2	+V3.3A_WWAN	V3.3A_WWAN_SENSE_POS	2m
		LAN	+V3.3M_LAN	V3.3M_LAN_SENSE_POS	50m
		EC	+V3.3A_KBC_EC	V3.3A_KBC_EC_SENSE_POS	10m
		EC	+V3.3A_KBC	V3.3A_KBC_SENSE_POS	10m
		Touch Screen	+V3.3DX_V1.8DX_TC_H_PNL_R	V3.3DX_1.8DX_TCH_PNL_SENSE_POS	10m
HAD Header		HDA	+VBATS_HDA_R1	VBATS_HDA_R1_SENSE_POS	50m
		Ambient Light Sensor	+V3.3S_ALS	V3.3S_ALS_SENSE_POS	10m

*continued...*



DDR4 RVP References					Instrumentation Recommendation
Category	Interface	Device/Function	System Rail	Net Name	PMR Value
		sensor hub	+V3.3A_SNSR_HDR	V3.3A_SNSR_HDR_SENSE_POS	5m
		sensor hub	+V3.3A_1.8A_SNSR_HDR	V3.3A_1.8A_SNSR_HDR_SENSE_POS	10m
		finger print sensor	+V3.3S_FPS	V3.3S_FPS_SENSE_POS	10m
		finger print sensor	+V1.8S_3.3S_FPS	V1.8S_3.3S_FPS_SENSE_POS	10m
		Touch panel sensor	+V3.3DX_V1.8DX_TC_H_PNL_R	V3.3DX_1.8DX_TCH_PNL_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_S0_TCP2	VCC3V3_S0_TCP2_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_SX_TCP2	VCC3V3_SX_TCP2_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_S0_TCP3	VCC3V3_S0_TCP3_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_SX_TCP3	VCC3V3_SX_TCP3_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_S0_TCP2	VCC3V3_S0_TCP2_SENSE_POS	10m
		PCIe slot	+V3.3A_DS3_PCIE_S_LOT1	V3.3A_DS3_PCIE_SLOT1_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_S0_TCP0	VCC3V3_S0_TCP0_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_SX_TCP0	VCC3V3_SX_TCP0_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_S0_TCP1	VCC3V3_S0_TCP1_SENSE_POS	10m
		Burnside Bridge USB TypeC retimer	+VCC3V3_SX_TCP1	VCC3V3_S0_TCP1_SENSE_POS	10m
		USB type C PD controller	V3.3A_USBC	V3.3A_USBC_SENSE_POS	5m
		WLAN	V3.3A_WLAN	V3.3A_WLAN_SENSE_POS	5m
eDP Panel	Backlight EDP panel (Connector 2)	VCC_EDP2_BKLT	VCC_EDP2_BKLT_SENSE_POS	10m	
	Backlight EDP panel (Connector 1)	+VCC_EDP1_BKLT	VCC_EDP1_BKLT_SENSE_POS	10m	

continued...



DDR4 RVP References					Instrumentation Recommendation
Category	Interface	Device/Function	System Rail	Net Name	PMR Value
		EDP panel electronics (Connector 2)	+V3.3DX_EDP1	V3.3DX_EDP1_SENSE_POS	10m
		EDP aux power (touchpanel) (Connector 1)	V3.3S_EDP1_AUXPWR	V3.3S_EDP1_AUXPWR_SENSE_POS	10m
		EDP panel electronics (Connector 2)	+V3.3DX_EDP2	V3.3DX_EDP2_SENSE_POS	10m
	eDP Panel	EDP aux power (touchpanel) (Connector 2)	+V3.3S_EDP2_AUXPWR	V3.3S_EDP2_AUXPWR_SENSE_POS	10m
		Audio	V1.8DX_AUDIO_DVD	V1.8DX_AUDIO_DVDD_SENSE_POS	10m
		Audio Amplifier	V5DX_AUDIO_SDW	V5DX_AUDIO_SDW_SENSE_POS	10m
		Touchpad	+V3.3S_TCH_PAD	VCC3V3_SX_TCP1_SENSE_POS	5m
		Touchpad	+V1.8S_TCH_PAD	V3.3S_TCH_PAD_SENSE_POS	10m
		TPM module	+VCC_SPI TPM	VCC_SPI TPM_SENSE_POS	10m
Codec		Audio Codec	+V1.8DX_3.3DX_I2S2	V1.8DX_3.3DX_I2S2_SENSE_POS	10m
		Audio Codec	+V1.8DX_3.3DX_I2S1	V1.8DX_3.3DX_I2S1_SENSE_POS	10m

**NOTE**

The voltage rails listed in red on the table, are only available on LPDDR4.

## 11.5 Logic Signal and Power Sequence Measurement Requirement

The list below illustrates the power sequencing and logic signals used for testing and debugging for power instrumentation on Tiger Lake. Though there are low speed logics, if FIP design will be covering the instrumentation, ensure no violations to the power integrity on the PDG.

**Table 242. Logic Signal and Power Sequencing Measurement Instrumentation List**

No.	Logic Signal/Power Sequence References
1	VCCRTC
2	SRTCRST#
3	RTCRST#
<i>continued...</i>	



No.	Logic Signal/Power Sequence References
4	5VSB
5	VCC_3P3V_DSW
6	DSW_PWROK
7	BATLOW#
8	SLP_SUS#
9	PCH Primary Power Rails
10	RSMRST#
11	SUSWARN#
12	SUSCLK
13	ACPRESENT
14	SUS_ACK#
15	SLP_A#
16	SLP_LAN#
17	LAN_PHY Power
18	SLP_S5#
19	SLP_S4#
20	SLP_S3#
21	SLP_S0#
22	PS_ON#
23	ESPI_RESET#
24	VCCST
25	VPP
26	VDDQ
27	PSU Main Power Rail (P12V, P5V, P3V3)
28	VCCIO
29	VCCSA
30	VTT
31	DDR_VTT_CNTL
32	VDDQPWRGD
33	IMVP_VR_READY
34	PLATFORM S0 RAILS
35	ALL_SYS_PWRGD
36	VCCST_PWRGD
37	PCH_PCH PWROK
38	PROCEPWRGD
39	IMVP_VR_ON

*continued...*

No.	Logic Signal/Power Sequence References
40	SUSPWRDNACK
41	CL_RST#
42	PCH_PWORK
43	DRAM_RESET
44	PROCPWRGD
45	PLTRST#
46	EXT_PWR_GATE#
47	PROCHOT#
48	PECI
49	CATERR#
50	VCCSTG
51	CPU_C10_GATE#
52	VR_ALERTHOT#
53	PWRBTN#

## 11.6 Bus Signal Measurement Recommendation

This section provides the bus signal list associated with Tiger Lake. If FIP design will be covering the instrumentation, ensure no violations to the power integrity on the PDG.

**Table 243. Bus List for Measurement Instrumentation**

Reference Bus Signal Group	Signal Name
I2C Interface (Touch Pad, Touch Screen, LCD, Battery, etc.)	I2C_SDA I2C_SCL
I2S Interface (Touch Pad, Touch Screen, LCD, Battery, etc)	I2S_SCK I2S_WS I2S_SD
SM Bus Interface: (Battery and..)	SMB_CLK SMB_DATA
USB Type-C	CC Channel
SVID	VIDSOUT VIDSCK VIDALERT#

## 12.0 Platform Debug and Test Hooks

The details of this chapter are requirements for run control debug-port design and Intel Direct Connect Interface (DCI), unless the text explicitly states that a design rule or connection is optional.

### NOTES

- While this content provides design solutions to allow both run control tool and boundary scan test JTAG tool to utilize the same JTAG scan chain for debug and manufacturing testing respectively, it does not contain all of the routing and design requirements for use with a boundary scan JTAG tool. Refer your Intel Field Representative if additional information on manufacturing boundary scan testing is needed.
- Intel is committed to reducing debug time and cost for OEMs and system integrators. Many debug features and test hooks have been designed into the platform to help reduce these factors. The following section provides implementation details of the processor debug and test hooks specifically to this platform only and takes priority over any discrepancies existing between this document and any previous Debug Port Design Guide.

## 12.1 Debug Port

This section describes the following:

- Primary Debug Port Routing Guidelines
- Intel® DCI Implementation
- MIPI60 Debug Port Mechanical Specifications
- Additional Debug Port PCB Layout Guidelines
- Depopulation Guidelines for Debug Port

### 12.1.1 Primary Debug Port Routing Guidelines

#### Primary Debug Port: Dual JTAG Scan Chain Only Topology

JTAG Topology in this section supports only Dual TCKs Scan Chain (aka Shared JTAG) covering the CPU and PCH components. This is a typical JTAG routing for the platforms. This topology can not support HVM test tool or any JTAG debugger that requires both processor and PCH JTAG in a single scan chain that is controlled by the same TCK.

Consult Intel representative and your HVM tool vendor if your HVM test tool required a Single Scan Chain (aka Common JTAG) support.

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**NOTE**

The resistor values used for the JTAG signals in this content are meant for ITP or Run control JTAG debugger only and are subject to change according to test/debug tool condition. For example, some third party JTAG test tools may not have enough drive strength to meet the input-threshold requirements of the Intel Silicon with the strong 50-ohm terminations required for the debug device. Consult with your test tool vendor for the appropriate resistor value to use.

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**Table 244. Primary Debug Port - Dual Scan Chain Only Routing Guidelines**

Pin/Signal	Routing Rules
LTB_TCK0	<ul style="list-style-type: none"> <li>Route from LTB_TCK0 to Tiger Lake CPU_TCK and JTAGX as shown in figure in <a href="#">Intel® DCI Implementation</a> on page 500. <ul style="list-style-type: none"> <li>Make sure to fork the traces no more than 28mm from LTB_TCK0 pin.</li> <li>Test Point Placement <ul style="list-style-type: none"> <li>Must be placed on secondary side</li> <li>Place to within 35mm of Tiger Lake CPU_TCK pin and within 28mm of termination.</li> <li>Pad size: Minimum 0.4572mm, Preferred pad size 0.635 mm</li> </ul> </li> </ul> </li> </ul> <p><b>CPU_TCK Termination: 51 ohm ±5% pull down to GND</b></p> <ul style="list-style-type: none"> <li>Placed to within 28mm of Tiger Lake pins.</li> </ul> <p><b>Stub length: 28mm</b></p> <ul style="list-style-type: none"> <li>Any stub length on TCK trace can not be more than 28mm. The stub length should be minimized whenever possible.</li> </ul> <p><b>Trace-to-Trace spacing:</b> 3 x Trace Width</p> <p>Maximum Via count: 4</p> <p><b>Maximum Trace length:</b> 154 mm [per segment, measure from Debug Port pin -&gt; Tiger Lake pin]</p> <p>Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.</p> <ul style="list-style-type: none"> <li>Ideally, TCK should be routed directly to the socket pin of each processor and then exit the via array to continue on to the termination resistor on the trace.</li> </ul> <p><i>Suggestion:</i> Provide a scope test point at Tiger Lake breakout via to verify signal integrity of the first platforms.</p> <p>Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p> <p><i>Note:</i> Some of the Intel reference designs might still have the JTAGX pull up. These pull up is only used to support Intel power-on, can be removed from the design.</p>
LTB_TCK1	<ul style="list-style-type: none"> <li>Route from LTB_TCK1 to Tiger Lake PCH_JTAG_TCK as shown in figure in <a href="#">Intel® DCI Implementation</a> on page 500. <ul style="list-style-type: none"> <li>Test Point Placement <ul style="list-style-type: none"> <li>Must be placed on secondary side</li> <li>Place to within 35mm of Tiger Lake pin and within 28mm of termination.</li> <li>Pad size: Minimum 0.4572mm, Preferred pad size 0.635mm</li> </ul> </li> </ul> </li> </ul> <p><b>Termination: 51 ohm ±5% pull down to GND</b></p> <ul style="list-style-type: none"> <li>Placed to within 28mm of Tiger Lake pins.</li> <li>Leave EMPTY.</li> </ul> <p><b>Stub length: 28mm</b></p> <ul style="list-style-type: none"> <li>Any stub length on TCK trace can not be more than 28mm. The stub length should be minimized whenever possible.</li> </ul> <p><b>Trace-to-Trace spacing:</b> 3 x Trace Width</p> <p>Maximum Via count: 4</p> <p><b>Maximum Trace length: 154mm</b></p> <p>Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.</p> <ul style="list-style-type: none"> <li>Ideally, TCK should be routed directly to the socket pin of each processor and then exit the via array to continue on to the termination resistor on the trace.</li> </ul>

*continued...*

Pin/Signal	Routing Rules
	<ul style="list-style-type: none"> <li><i>Suggestion:</i> Provide a scope test point at Tiger Lake breakout via to verify signal integrity of the first platforms.</li> </ul> <p>Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p>
LTB_TMS	<ul style="list-style-type: none"> <li>Route from LTB_TMS to Tiger Lake CPU_TMS and PCH_JTAG_TMS as shown in figure in <a href="#">Intel® DCI Implementation</a> on page 500. <ul style="list-style-type: none"> <li>Make sure to fork the traces no more than 28mm from LTB_TMS pin.</li> <li>Test Point Placement <ul style="list-style-type: none"> <li>Must be placed on secondary side</li> <li>Place to within 35mm of Tiger Lake pin and within 28mm of termination.</li> <li>Pad size: Minimum 0.4572mm, Preferred pad size 0.635mm</li> </ul> </li> </ul> </li> </ul> <p><b>Termination: 51 ohm ±5% pull up to VCCSTG or equivalent</b></p> <ul style="list-style-type: none"> <li>Placed to within 28mm of Tiger Lake PCH_JTAG_TMS pin [note: CPU_TMS has on-die termination].</li> </ul> <p><b>Stub length: 28mm</b></p> <ul style="list-style-type: none"> <li>Any stub length on this trace can not be more than 28mm. The stub length should be minimized whenever possible.</li> </ul> <p><b>Trace-to-Trace spacing:</b> No limit, but at least 2x trace width when possible Maximum Via count: No limit, but should minimize whenever possible</p> <p><b>Maximum Trace length: 154mm</b> [for each segment, measures from Debug Port-&gt;Tiger Lake pin]</p> <p><b>Length Matching: matching to +/- 6.85mm of TCK</b></p> <ul style="list-style-type: none"> <li>Match CPU_TMS net to CPU_TCK net</li> <li>Match PCH_JTAG_TMS to PCH_JTAG_TCK net</li> <li>Length matching is recommended but it is optional [Note: Length matching to TCK might allow operating at higher TCK frequency]</li> </ul> <p>Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.</p> <ul style="list-style-type: none"> <li>Ideally, TMS will be routed directly to the socket pin of each processor and then exit the via array to continue on to the termination resistor on the trace.</li> </ul> <p><i>Suggestion:</i> Provide a scope test point at Tiger Lake breakout via to verify signal integrity of the first platforms.</p> <p>Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p>
LTB_TRSTn	<ul style="list-style-type: none"> <li>Route daisy chain from LTB_TRSTn to Tiger Lake CPU_TRST# and PCH_TRST# as shown in figure in <a href="#">Intel® DCI Implementation</a> on page 500. <ul style="list-style-type: none"> <li>Test Point Placement <ul style="list-style-type: none"> <li>Must be placed on secondary side</li> <li>Pad size: Minimum 0.4572mm, Preferred pad size 0.635mm</li> </ul> </li> </ul> </li> </ul> <p><b>Termination: None</b></p> <p><b>Stub length: 28mm</b></p> <p><b>Trace-to-Trace spacing:</b> No limit. At least 1x trace width when possible Maximum Via count: No limit. Should minimize whenever possible</p> <p><b>Maximum Trace length: 381mm</b></p> <p><b>Length Matching: None</b></p> <p>Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.</p> <p>Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p> <p><i>Note:</i> Some of the Intel reference designs might still have the LTB_TRSTn pull down. These pull down is only used to support Intel power-on, can be removed from the design.</p>
LTB_TDI	<ul style="list-style-type: none"> <li>Route from LTB_TDI to Tiger Lake CPU_TDI and PCH_JTAG_TDI as shown in figure in <a href="#">Intel® DCI Implementation</a> on page 500. <ul style="list-style-type: none"> <li>Make sure to fork the traces no more than 28mm from LTB_TDI pin.</li> <li>Test Point Placement <ul style="list-style-type: none"> <li>Must be placed on secondary side</li> <li>Place to within 35mm of Tiger Lake pin and within 28mm of termination.</li> <li>Pad size: Minimum 0.4572mm, Preferred pad size 0.635mm</li> </ul> </li> </ul> </li> </ul> <p><b>Termination: 51 ohm ±5% pull up to VCCSTG or equivalent</b></p>

*continued...*

Pin/Signal	Routing Rules
	<ul style="list-style-type: none"> <li>Placed to within 28mm of PCH_JTAG_TDI pin [Note: CPU_TDI has on-die termination].</li> </ul> <p><b>Stub length: 28mm</b></p> <ul style="list-style-type: none"> <li>The stub length should be minimized whenever possible.</li> </ul> <p><b>Trace-to-Trace spacing:</b> No limit, At least 1x trace width when possible</p> <p>Maximum Via count: No limit, Should minimize whenever possible</p> <p><b>Maximum Trace length: 154mm</b> [For each segment, measures from Debug Port-&gt;Tiger Lake pin]</p> <p><b>Length Matching: matching to +/- 6.85mm of TCK</b></p> <ul style="list-style-type: none"> <li>Match PROC_TDI net to PROC_TCK net</li> <li>Match PCH_JTAG_TDI to PCH_JTAG_TCK net</li> <li>Length matching is recommended but it is optional [Note: Length matching to TCK might allow operating at higher TCK frequency]</li> </ul> <p>Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.</p> <p>Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p>
LTB_TDO	<ul style="list-style-type: none"> <li>Route from LTB_TDO to Tiger Lake CPU_TDO and PCH_JTAG_TDO as shown in figure in <a href="#">Intel® DCI Implementation</a> on page 500. <ul style="list-style-type: none"> <li>Make sure to fork the traces no more than 28mm from LTB_TDO pin.</li> <li>Test Point Placement <ul style="list-style-type: none"> <li>Must be placed on secondary side</li> <li>Place to within 35mm of Tiger Lake pin and within 28mm of termination.</li> <li>Pad size: Minimum 0.4572mm, Preferred pad size 0.635mm</li> </ul> </li> </ul> </li> </ul> <p><b>Termination: 100 ohm ±5% pull up to VCCSTG or equivalent</b></p> <ul style="list-style-type: none"> <li>Placed to within 28mm of each Tiger Lake pin.</li> </ul> <p><b>Stub length: 28mm</b></p> <ul style="list-style-type: none"> <li>Any stub length on this trace can not be more than 28mm. The stub length should be minimized whenever possible.</li> </ul> <p><b>Trace-to-Trace spacing:</b> No limit. At least 1x trace width when possible</p> <p>Maximum Via count: No limit. Should minimize whenever possible</p> <p><b>Maximum Trace length: 154mm</b> [For each segment, measures from Debug -&gt;Tiger Lake pin]</p> <p><b>Length Matching: matching to +/- 6.85mm of TCK</b></p> <ul style="list-style-type: none"> <li>Match PROC_TDO net to PROC_TCK net</li> <li>Match PCH_JTAG_TDO to PCH_JTAG_TCK net</li> <li>Length matching is recommended but it is optional [Note: Length matching to TCK might allow operating at higher TCK frequency]</li> </ul> <p>Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.</p> <p>Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p>

### Primary Debug Port: Observation Ports (CFG[0:19]) and PREQ#/PRDY# pins Routing Guidelines

The debug connector has defined 16 observation data signals (OBSDATA ports) and specialized signal ports (4 pairs OBS\_FN).

**Table 245. Primary Debug Port - Observation Pins Routing Guidelines**

Pin/Signal	Routing Rules
OBSFN_A[0] OBSFN_A[1]	<ul style="list-style-type: none"> <li>Route these signals to Tiger Lake signals point-to-point according to <a href="#">Figure 275</a> on page 503: <ul style="list-style-type: none"> <li>Route LTB_OBSFN_A[0] to Tiger Lake PROC_PREQ#</li> <li>Route LTB_OBSFN_A[1] to Tiger Lake PROC_PRDY#</li> </ul> </li> <li>Test Point Placement <ul style="list-style-type: none"> <li>Must be placed on secondary side</li> <li>Place to within 35 mm of each Tiger Lake pin.</li> <li>Pad size: Minimum 0.4572mm, Preferred pad size 0.635mm</li> </ul> </li> </ul> <p><b>Termination: None</b></p>

*continued...*

Pin/Signal	Routing Rules
	<p><b>Stub length: 28mm.</b> The stub length should be minimized whenever possible.  <b>Trace-to-Trace spacing:</b> No limit. At least 1xTrace Width when possible  Maximum Via count: No limit. Should minimize whenever possible  <b>Maximum Trace length: 308mm</b>  <b>Length Matching: None</b>  Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.  Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p>
OBS DATA_A[2:0], OBS DATA_B[3:0] OBS DATA_C[3:0] OBS DATA_D[3:0]	<ul style="list-style-type: none"> <li>• Route these signals to Tiger Lake signals point-to-point according to <a href="#">Figure 275</a> on page 503: <ul style="list-style-type: none"> <li>– Route OBS DATA_A[0] to Tiger Lake CFG[0].</li> <li>– Route OBS DATA_A[1] to Tiger Lake CFG[1].</li> <li>– Route OBS DATA_A[2] to Tiger Lake CFG[2].</li> <li>– Route OBS DATA_A[3] to Tiger Lake CFG[3].</li> <li>– Route OBS DATA_B[0] to Tiger Lake CFG[4].</li> <li>– Route OBS DATA_B[1] to Tiger Lake CFG[5].</li> <li>– Route OBS DATA_B[2] to Tiger Lake CFG[6].</li> <li>– Route OBS DATA_B[3] to Tiger Lake CFG[7].</li> <li>– Route OBS DATA_C[0] to Tiger Lake CFG[8].</li> <li>– Route OBS DATA_C[1] to Tiger Lake CFG[9].</li> <li>– Route OBS DATA_C[2] to Tiger Lake CFG[10].</li> <li>– Route OBS DATA_C[3] to Tiger Lake CFG[11].</li> <li>– Route OBS DATA_D[0] to Tiger Lake CFG[12].</li> <li>– Route OBS DATA_D[1] to Tiger Lake CFG[13].</li> <li>– Route OBS DATA_D[2] to Tiger Lake CFG[14].</li> <li>– Route OBS DATA_D[3] to Tiger Lake CFG[15].</li> </ul> </li> </ul> <p><b>Test Point Placement (CFG[3])</b></p> <ul style="list-style-type: none"> <li>• Must be placed on secondary side</li> <li>• Place to within 35mm of each Tiger Lake pin.</li> <li>• Pad size: Minimum 0.457mm, Preferred pad size 0.635mm</li> </ul> <p><b>Termination: None</b></p> <p><b>Stub length: 28mm.</b> The stub length should be minimized whenever possible.  <b>Trace-to-Trace spacing:</b> No limit, but 2x trace width when possible  Maximum Via count: No limit, but should minimize whenever possible  <b>Maximum Trace length: 305mm</b> [For each segment, measures from DebugPort OBS pin -&gt;Tiger Lake pin]  <b>Length Matching: within +/- 6.85mm of CFG[17]</b>  Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.  Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.  <i>Note:</i> Some of the Intel reference designs might connect CFG[0] to HOOK[2]. This route is not needed on OXM board.</p>
OBS FN_C[0] OBS FN_C[1] OBS FN_D[0] OBS FN_D[1]	<ul style="list-style-type: none"> <li>• Route these signals to Tiger Lake signals point-to-point according to <a href="#">Figure 275</a> on page 503:</li> <li>•</li> </ul> <p><b>Termination: None</b></p> <p><b>Stub length: 28mm.</b> The stub length should be minimized whenever possible.  <b>Trace-to-Trace spacing:</b> 3 x Trace Width  Maximum Via count: 4  <b>Maximum Trace length: 2ns (roughly 305mm)</b>  <b>Length Matching: within +/- 6.85mm of CFG[17]</b>  Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.  Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p>
OBS FN_B[1:0]	<ul style="list-style-type: none"> <li>• Route these signals to Tiger Lake signals according to <a href="#">Figure 275</a> on page 503:</li> </ul> <p><b>Termination: None</b></p>

*continued...*

Pin/Signal	Routing Rules
	<p><b>Stub length: 28mm</b></p> <ul style="list-style-type: none"> <li>Any stub length on this trace can not be more than 28mm. The stub length should be minimized whenever possible.</li> </ul> <p><b>Trace-to-Trace spacing:</b> No limit, but at least 1x trace width when possible</p> <p>Maximum Via count: No limit, but should minimize whenever possible</p> <p><b>Maximum Trace length: 305mm</b></p> <p><b>Length Matching:</b> within +/- 6.85mm of each other</p> <p>Refer to <a href="#">Additional Debug Port PCB Layout Guidelines</a> on page 504 for additional debug port PCB layout rules.</p> <p>Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p>
Tiger Lake BPM#[3:2]#	<ul style="list-style-type: none"> <li>Routed as test points or resistor pads on the platform.             <ul style="list-style-type: none"> <li>The test points or pads must be placed in a location that is probe accessible (avoid location that is blocked by thermal solutions) so that Intel would be able to access them when debug by Intel is required.</li> </ul> </li> </ul> <p>Refer to <a href="#">Depopulation Guidelines for Debug Port</a> on page 506 for debug port depopulation rule.</p>

**Table 246. Debug Port Signal Mapping**

MIP160 Pin#	Intel DPS Generic Signal Name	Target System Signal Name	Direction from Tool	Device	Components	Notes
3	TCK0	CPU_JTAG_TCK		CPU	51Ω to GND	Add CAD note to place within 27.94mm of CPU_JTAG_TCK pin in Layout
		PCH_JTAGx		PCH	N/A	Internal 60Ω - 100Ω ODT to GND in PCH.
51	TCK1	PCH_JTAG_TCK		PCH	<b>empty</b> 51Ω to GND resistor	Defensive, A0 PO boards only. Internal 60Ω - 100Ω ODT to GND in PCH. Add CAD note to place within 27.94mm of PCH_JTAG_TCK pin in Layout
9	TRST_N	CPU_JTAG_TRST_N		CPU	N/A	Internal 50Ω ODT to GND in PCH.
		PCH_CPU_JTAG_T_RST_B		PCH	N/A	
2	TMS	CPU_JTAG_TMS		CPU	N/A	Internal 50Ω ODT to VccST-G in CPU
		PCH_JTAG_TMS		PCH	51Ω to VccSTG_OUT_LGC	
5	TDI	CPU_JTAG_TDI		CPU	N/A	Internal 50Ω ODT to VccST-G in CPU
		PCH_JTAG_TDI		PCH	51Ω to VccSTG_OUT_LGC	
4	TDO	CPU_JTAG_TDO		CPU	100Ω to VccSTG_OUT_LGC	

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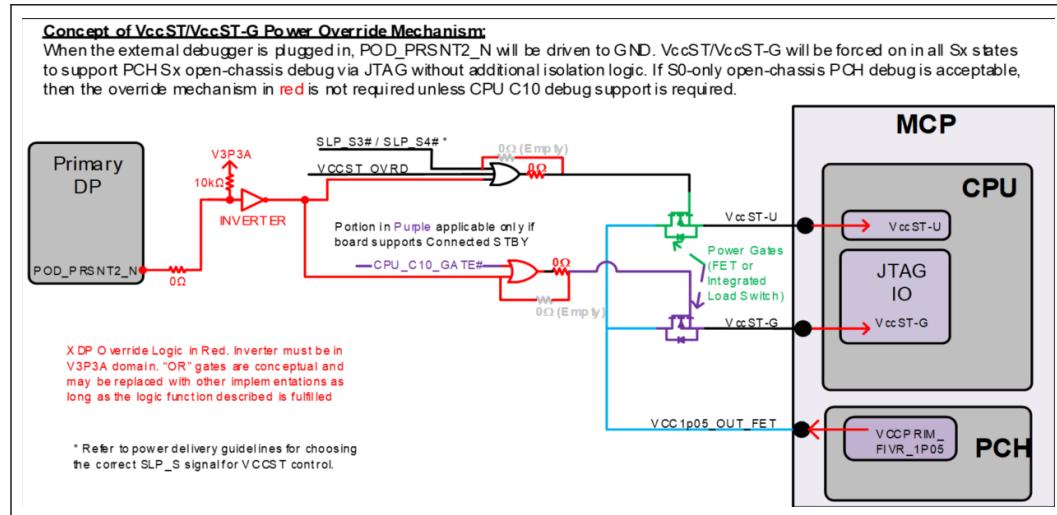
MIPI60 Pin#	Intel DPS Generic Signal Name	Target System Signal Name	Direction from Tool	Device	Components	Notes
		PCH_JTAG_TDO		PCH	100Ω to VccSTG_OUT_LGC	
10	PREQ_N	CPU_PREQ_N		CPU	N/A	UP3/UP4 packages only have a single PREQ_N and PRDY_N pin.
		PCH_PREQ_N		PCH	N/A	
11	PRDY_N	CPU_PRDY_N		CPU	N/A	
		PCH_PRDY_N		PCH	N/A	
8	TRST_PD	No Connect		N/A	No Connect	
42	HOOK[0] (CLTAP_PWRGOOD)	RSMRST#	IN	PCH	1kΩ series	
36	HOOK[3] (BOOT_HALTN_N Strap)	SPI0_MOSI_IO_0 (Strap)	OUT	PCH	4.7kΩ strapping resistor + 20kΩ PU on PCH-side net	<b>Hook[3] solution assumes only PU on SPI signal is 20kΩ board PU.</b>
7	HOOK[6] (RESET_N)	DBG_PMODE	IN	PCH	1kΩ PU to PCH VCC1p05_OUT_FET	
38	HOOK[2] (EAR_N strap)	EAR_N	OUT	CPU	1kΩ - 1.5kΩ strapping resistor	Add CAD note to place strapping resistor within 6.35mm of main hook[2] to cfg[0] trace
15	POD_PRESENT1_N (PCH DEBUG_CONSENT_N Strap) (optional)	SPI0_IO_2 (Strap)		PCH	1kΩ - 1.5kΩ strapping resistor + 20kΩ PU on PCH-side net	<b>Assumes only PU on SPI signal is 20kΩ board PU.</b> Refer Primary DP - Misc Signals tab
17	POD_PRESENT2_N (CPU DEBUG_EN_N)	VccST-G/VccST Override		CPU	PU + inverter	<b>Refer Primary DP - Misc Signals tab for more details.</b>
40	HOOK[1] (POWER_BTN_N)	Power_button_n	OUT	System	1kΩ - 3kΩ PU + 0.1uF cap to GND	PU to adequate voltage rail. Refer Primary DP - Misc Signals tab
6	HOOK[7] / nReset (RESET_BTN_N)	Reset_button_n	OUT	System	1kΩ - 3kΩ PU + 0.1uF cap to GND	
34	RSVD[1]	No Connect		N/A	N/A	N/A
55	HOOK[8]	BPM#_0	IN/OUT	CPU	1kΩ - 10kΩ PU to VCCIO_OUT	Optional
53	HOOK[9]	BPM#_1	IN/OUT	CPU	1kΩ - 10kΩ PU to VCCIO_OUT	Optional
13	PTI_0_CLK	CFG[16]		CPU	N/A	Direct connection.
19..33 odd	PTI_0_DATA[0..7]	CFG[0..7]		CPU	N/A	Direct connection.
59	PTI_3_CLK	CFG[17]		CPU	N/A	Direct connection.

**continued...**

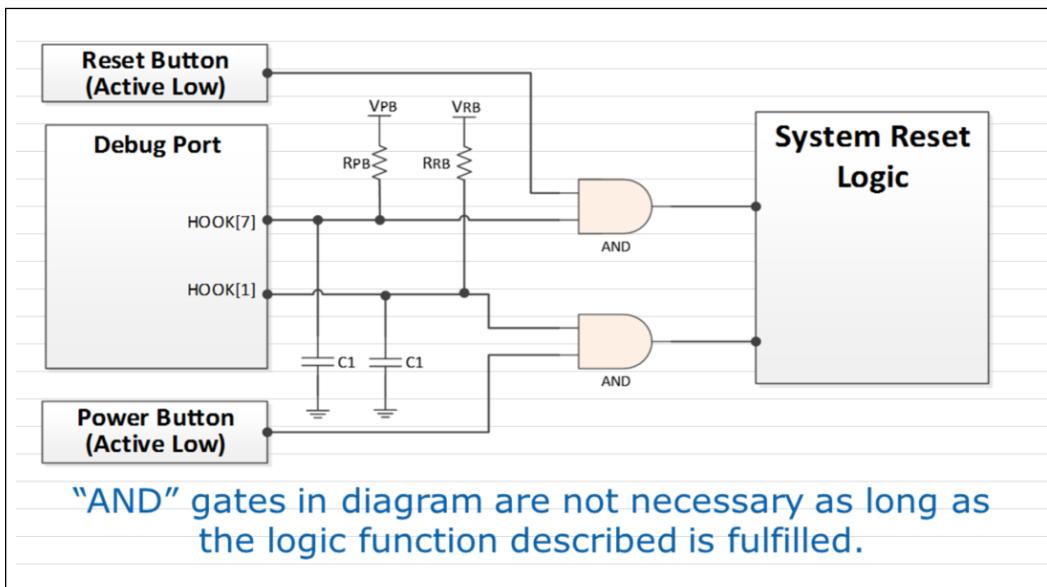
MIP160 Pin#	Intel DPS Generic Signal Name	Target System Signal Name	Direction from Tool	Device	Components	Notes
35..49 odd	PTI_0_DATA[8..15] / PTI_3_DATA[0..7]	CFG[8..15]		CPU	N/A	Direct connection.
14	PTI_1_CLK	GND		N/A	N/A	Unused PTI CLK's must be GND'd
18..32 even	PTI_1_DATA[0..7]	No Connect		N/A	N/A	N/A
60	PTI_2_CLK	GND		N/A	N/A	Unused PTI CLK's must be GND'd
44,46	RSVD[2..4]	No Connect		N/A	N/A	N/A
52	RSVD4	V3P3_AUX		System	N/A	
54	DBG_UART_TX	No Connect		N/A	N/A	
56	DBG_UART_RX	No Connect		N/A	N/A	
57:58	GND	GND				
48	I2C_SCL	I2C_SCL		System	PU	Debugger expects external PU as per I2C/SMBus spec
50	I2C_SDA	I2C_SDA		System	PU	
1	VREF_DEBUG	VCC1p05_OUT_FET		PCH	N/A	VCC1p05_OUT_FET rail from PCH
12	VREF_TRACE	VCCIO_OUT		CPU	N/A	

## VCCST and VCCST-G Override

Figure 270. VCCST and VCCST-G Override



**Figure 271. Hook1 and Hook7 Connection**



### 12.1.2 Intel® Small Form Factor Debug Connector

In order to support smaller form factor board design, the following are several options that board designers can adopt to reduce debug port connector size.

#### 20 Pin Intel® Small Form Factor Debug Connector

In this option, 19 debug signals that are frequently used in debug are selected. It is a mixture of signals from MIPI60 and DCI 4 wire in cases where the mother board design does not have type-A USB port with no redrivers. The following is the pin assignment.

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#### NOTE

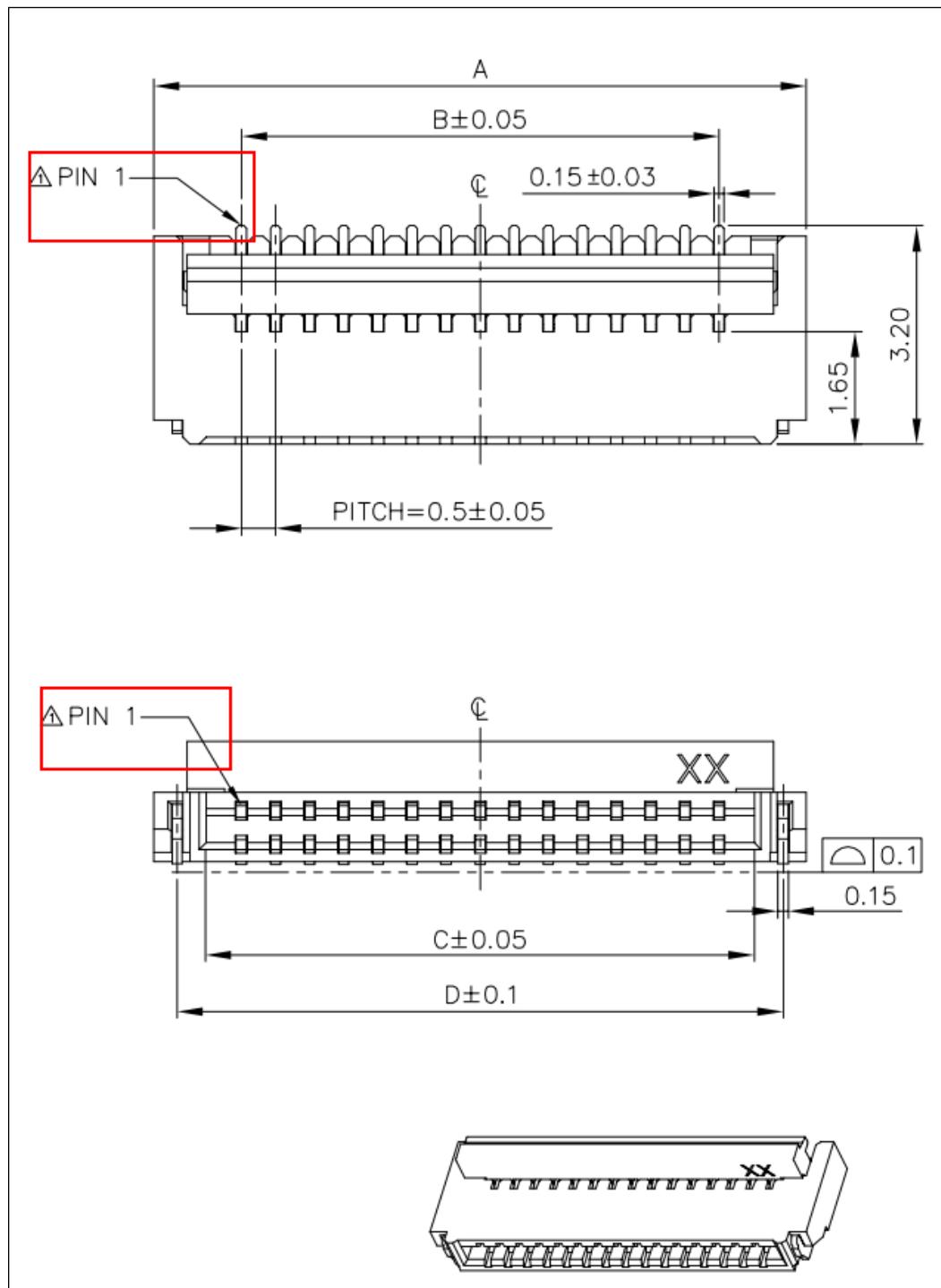
USB routing should be direct with no capacitors/resistors/other components between SOC and the connector

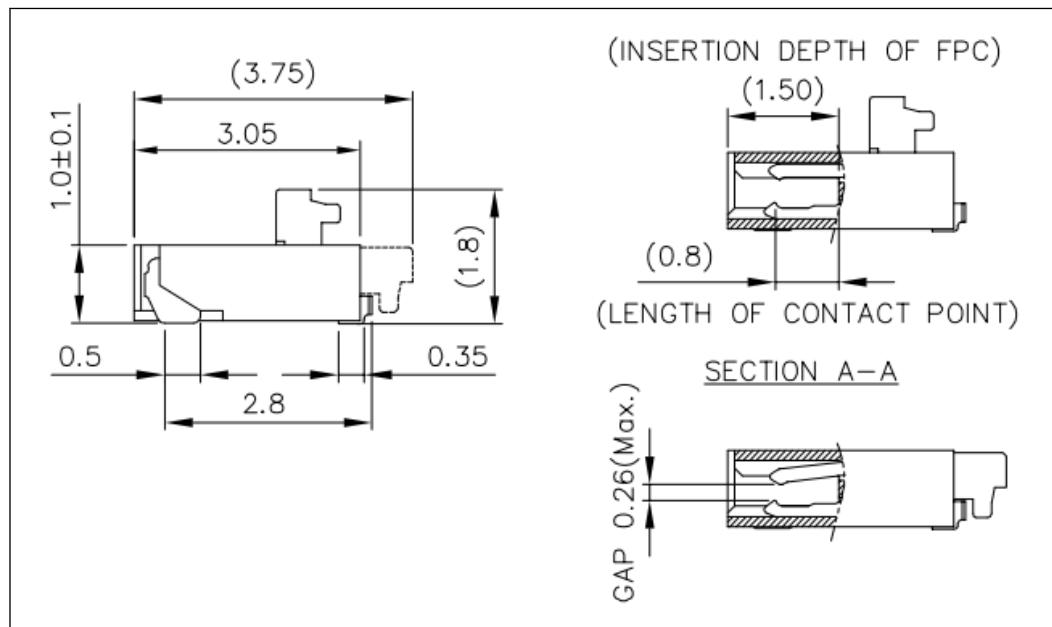
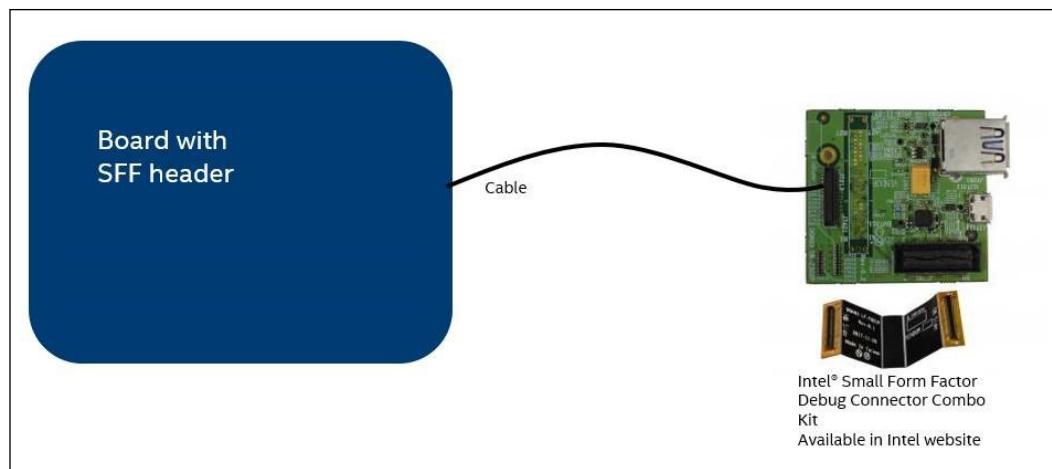
60P MIPI60	RVP Names	MB SFF Header	MB Pin#
		GND	#19
#3	MIPI60_TCLK	H_TCK	#7
#9	MIPI60_TRST_N	H_TRST#	#9
#4	MIPI60_TDO	PCH_TDO_SFF	#5
#5	MIPI60_TDI	PCH_TDI	#8
#2	MIPI60_TMS	PCH_TMS_SFF	#6
#51	MIPI60_TCLK1	PCH_TCK_SFF	#20
#13	MIPI60_CFG16_N	CF6<16>	#10
#19	MIPI60_CFG0_N	CFG<0>	#11

*continued...*

<b>60P MIPI60</b>	<b>RVP Names</b>	<b>MB SFF Header</b>	<b>MB Pin#</b>
#21	MIPI60_CFG1_N	CFG<1>	#12
		USB30_TX_DP	#1
		USB30_TX_DN	#2
		USB30_RX_DP	#3
		USB30_RX_DN	#4
#23	MIPI60_CFG2_N	CFG<2>	#13
#25	MIPI60_CFG3_N	CFG<3>	#14
#27	MIPI60_CFG4_N	CFG<4>	#15
#29	MIPI60_CFG5_N	CFG<5>	#16
#31	MIPI60_CFG6_N	CFG<6>	#17
#33	MIPI60_CFG7_N	CFG<7>	#18

**Figure 272. SFF S Connector Details (a)**



**Figure 273. SFF S Connector Details (b)****Figure 274. Connection to Daughter Card**

Cable ordering info:

[https://designtools.intel.com/ProductDetails.asp?ProductCode=CCECONNBL01\(cable\)](https://designtools.intel.com/ProductDetails.asp?ProductCode=CCECONNBL01(cable))

The connection to standard debug tool is via Intel® Small Form Factor Debug Connector Combo Kit which can be purchased from Intel. Common source for the cable is still being worked on. Please contact Intel for details of the cable fabrication.

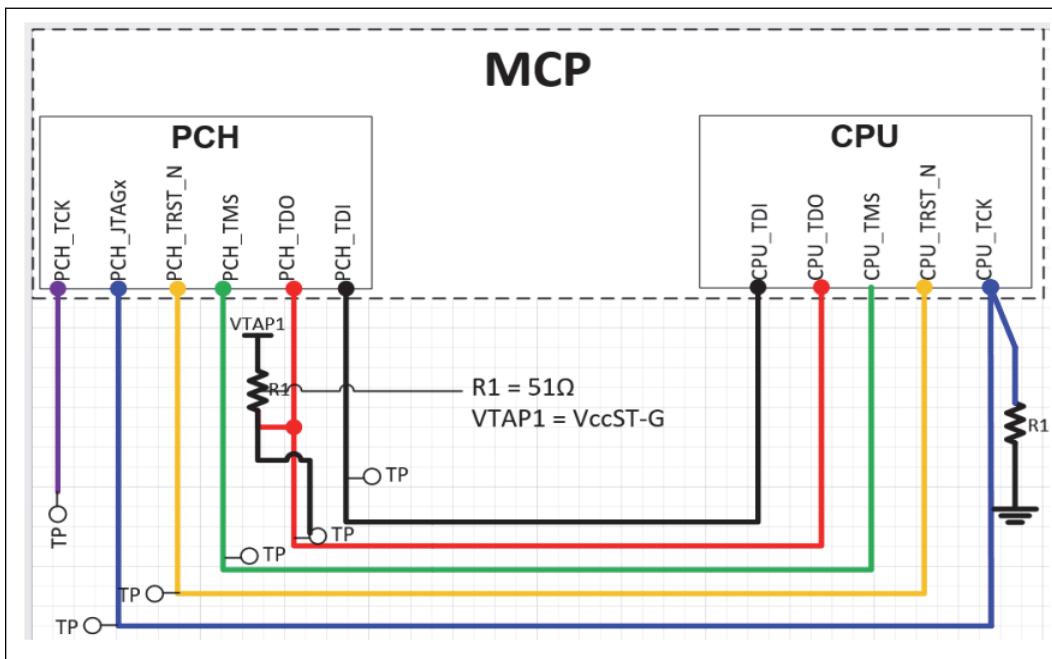
20 pin Intel® Small Form Factor Debug Connector will have some limitation as listed below:

Difference	Mitigation
<b>Cannot reset/power cycle target with debug header</b>	Use other means to reset/power cycle if needed, or use DCI
<b>Cannot detect power presence with debug header</b>	Can be ignored by software
<b>Cannot set break points with debug header</b>	Rarely needed, or use DCI
<b>Cannot do run control with debug header</b>	Run control is normally for software debug. In this case, DCI is good enough
<b>Only 8 CFG for internal signals</b>	Should be enough for most issues, and at worst case, blue wire the other 8

### 12.1.3 Intel® DCI Implementation

Intel® DCI (Direct Connect Interface) is an Intel Technology that allows debug access by re-purposing a USB 3.2 port. The advantage is debug functions and trace features can be connected using existing USB3 ports, rather than the usual additional connectors. If properly supported, many debug functions can be implemented “closed chassis”. The DCI connection supports run-control debug, validation, trace, DMA, OS Debug and scripting.

DCI is implemented using two primary transport topologies: Intel® DCI.OOB (formerly BSSB), and Intel® DCI.USB2/USB3 (formerly DbC).



- **Intel® DCI.OOB Configurations Supporting USB3 Type A**

For Intel® DCI.OOB Hosting DCI functionality to work properly in the system, proper signaling as described in previous section must be preserved. For many USB3 Type A implementations, no re-timer device is required. If a re-timer is required, it will stop DCI.OOB operation. Also, the signals need to be routed from PCH USB3 and not from CPU.

- **Intel® DCI.OOB Configurations Supporting USB Type-C Implementations**

In this case, CPU USB3 ports will be used and DCI.OOB functionality will not be supported. Most debug can be done with just DCI-Debug class. But DCI.OOB should still be reserved for some complicated debug. For designs with only type C, route one of the unused PCH USB3 ports to test points for DCI.OOB functionality. 2-wire DCI.OOB is an extension of the existing Intel DCI protocol supporting very early boot and low power on USB Type C connectors. Its function and capability are similar to the existing 4-wire DCI.OOB solution. However, it should not be used as a replacement because its bandwidth is limited. 2-wire DCI.OOB uses two signal paths that are routed through the SBU pins on the Type C connector and through the type C mux to LSx pin pairs on the PCH. Signaling diagrams in the "USB-C Sub-System" section of this Platform Design Guide explain the hardware connection. Any LSx pair from PCH can support 2-wire DCI.OOB functionality.

#### 2 wire DCI.OOB requirements

- PD controllers: Only TPS65988DHRSHR and CCG5 (2 port) are validated with RVP
- Retimer: Only Intel Burnside Bridge A1 is supported
- For other retimers PD combinations, use 4-wire DCI.OOB either through type A or test points

For designs implementing USB only type-C, SBU pins do not have any functional purpose. Route SBU pins to any of the TBT\_LSX pairs.

SBU0 – TXD

SBU1 – RXD

In BIOS, default the GPIO to native mode 5.

### **USB3/USB2 Hosting**

This is implemented using standard USB3 Super Speed/USB2 High Speed electrical and transport protocol. There are no additional electrical channel or connection requirements for using DCI.USB as the standard USB3 Super Speed/USB2 High Speed channel is used. A standard USB3/USB2 cable can be used for connecting the Host PC and the SUT. No special interface box is required.

- **USB3 Advantage:** Much higher transport speed. No special interface box is required.
- **USB3 Disadvantage:** Starts later in boot process so some early messages and unlock capabilities are not available. Does not operate through power sequences.
- **USB2 Advantage:** Higher speed than DCI.OOB. No special interface box is required. Can trace even in S5.
- **USB2 Disadvantage:** There are some usages that DCI.USB2 cannot handle. Those cases will be handled by Intel using DCI.OOB.

Signaling Considerations for Intel® DCI Support over USB3/USB2.

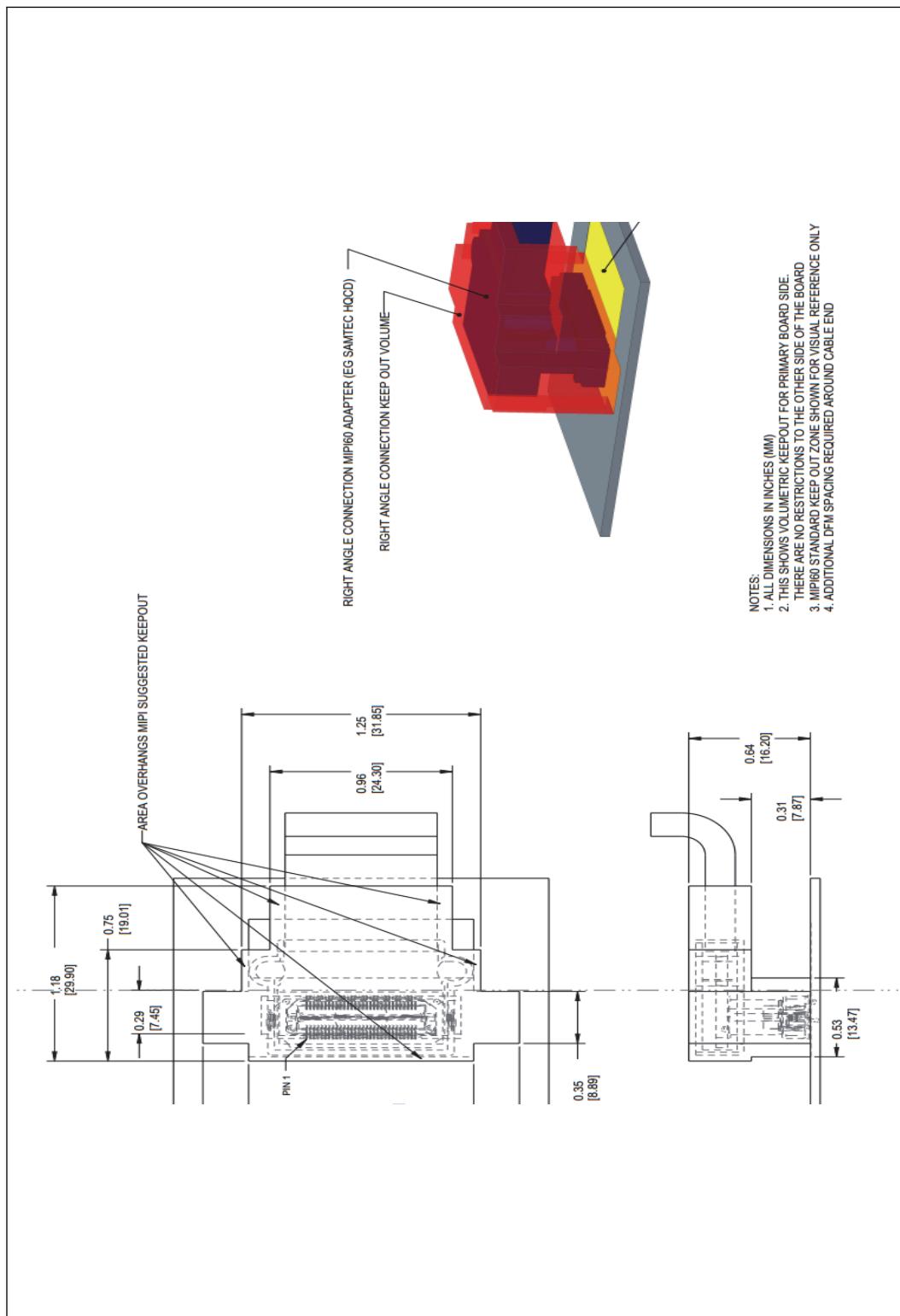
The controllers and multiplexers in the signal path of the USB3/USB2 pins must be powered when Intel DCI is in use for the signals to pass. Standard USB3/USB2 signaling is utilized.

## 12.1.4 MIPI60 Debug Port Mechanical Specifications

The figure below illustrates the target system volume that must be reserved for the Debug device to attach to the target system. It is recommended that the main debug device enclosure be securely attached to the target system to avoid damage to the Debug device and the target system. Four 3.175mm mounting holes are provided on the Debug Device to facilitate attachment with screws or cable ties.

The Debug Device hardware unit has four 12.7mm by 1.588mm slots for cable tie or velcro straps to secure the body of the Debug Device hardware unit to the chassis. Third party vendors run control tools would have different keepout volumes and securing features.

Figure 275. MIPI 60 Debug Connector System Keep-Out Diagram



The placement of the MIPI60 connector on the 2nd side should be avoided if possible. Among other reasons, it should be avoided due to the complexity of hand placing and soldering the device. Cap all vias near the MIPI60 connector pads in compliance with the Intel DFM Guidelines for capped vias. vias need to be capped not only around the MIPI60 connector pads, but also specifically under the MIPI60 connector body. Open vias under the MIPI60 connector can cause shorts.

Contact Intel representative for a formal review of the mechanical placement and layout of the system.

## 12.1.5

### Additional Debug Port PCB Layout Guidelines

This section describes the general high speed layout guidelines must be followed for the debug port:

Electrical lengths of Debug Port traces are provided in units of flight time. Conversion of flight time to board-trace lengths is dependent on what layer routing occurs on, and the dielectric constant of the board materials for a specific design. Rule-of-thumb numbers can be derived by using 5.512 to 7.087ps/mm for outer layers of an FR4 product and 7.087ps/mm for inner layers

**Trace Nominal Impedance for Debug Port** JTAG signals, OBS pins, HOOK[3:0], HOOK[7:6], LTB\_PRESENT#, I<sup>2</sup>C pins: 50 ohm ±17% nominal impedance.  
HOOK[5:4]: 100ohm (differential pair).

Unless indicated otherwise, Signals on the debug port should be routed with this in mind:

- Minimize the number of layer transitions and avoid plane split crossings imposed on each trace (ideally this will be zero). If return paths are well kept then the number of vias are nearly immaterial.
  - Clock signals (TCK, PTI\_CLK) are allowed maximum of 4 vias.
  - Clock signals are not allowed to route across splits or over voids.
- All signals except VCCOBS, GND and HOOK[5:4] pins must be referenced to ground (GND) plane.
- All signals except GND, Vcc, and HOOK[0,1, 2, 3, 6, 7] pins must include ground-stitching/return vias near every layer transition. ground-stitching/return vias should be placed to within 2.54mm of the signal via.
- For situations where these signals are routed referenced to one or more power planes, include a bypass capacitor near every layer transition or plane split between the two referenced planes. bypass capacitor pads should be placed to within 12.7mm from the trace.
- Avoid sharing Debug Port bypass capacitors with other high-speed signals.
- For all signals, pull-up termination resistors should be located above a solid-power plane. If a solid-power plane does not exist at the required termination location, add a 0.1µF ceramic capacitor to GND on the pull-up voltage within 12.7mm of termination resistor.

The length of any un-terminated stub on any TCK (1:0) or observation-port pin nets must be less than 28mm unless otherwise stated. The 51 ±5% ohm recommendation in this document for signal termination has been proven to work on all recommended board impedances. JTAG and observation-port signals my optionally be terminated using the nominal-board impedance.

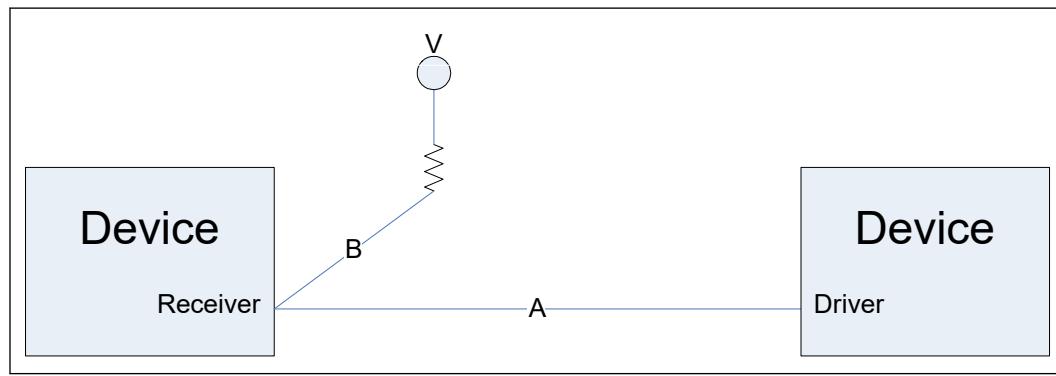
### Termination Resistor Placement

Termination resistors are given, with tolerances, whenever appropriate. Tolerances are documented as within  $\pm$  of the percentage.

With few exceptions (noted specifically in their description), termination resistors must be close to the receiver. The topology, at the end of the chain, must be terminated in one of the following ways (in all cases) except those noted in their specific description.

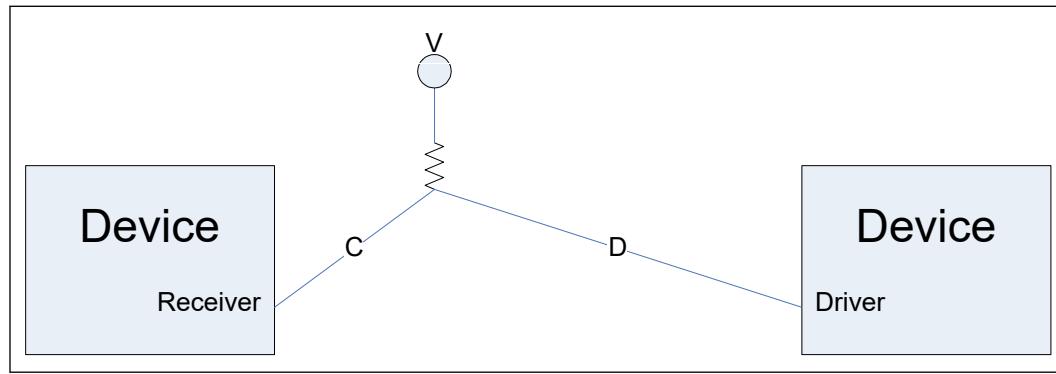
**Preferred Debug Port termination Method:** In the case of the figure below, where there is a termination after the last receiver, (A) must be smaller than any noted maximum routing length. There is no restriction for the length of (B) unless otherwise noted.

**Figure 276. Termination after Last Receiver**



**Option 2 for Debug port termination Method:** the figure below shows another method for termination that is equally valid. This is a termination prior to the end receiver where the maximum routing length of the signal must be less than the length of (D) + (C). (C) must be less than 28mm or noted stub length whichever is smaller.

**Figure 277. Termination Prior to Last Receiver**



In both figures, note that there may be other devices on the (A) or (D) routing of the signal if called for within this document.

### 12.1.6 Depopulation Guidelines for Debug Port

At some point there may be a desire to remove the debug port from the board especially when the debug is no longer needed. It is recommended that the debug port real estate and pads remain in place if they need to be populated for a future problem.

Tiger Lake UP3 and Tiger Lake UP4 has adequate internal bias resistance on JTAG, CPU\_PREQ# and CPU\_PRDY# signals to keep the devices in an idle state without the external pull up resistors.

It is acceptable to replace the standard resistor values with any resistor value between 51 ohm to 3k ohm to reduce bill-of-material items when the debug is no longer needed.

Processor BPM#[3:0] nets can be left floated when not use for debug. Processor CFG[19:0] and PCH chipset test interfaces might have dual purpose usage. From debug port perspective, external components (resistor, jumper, or FET switch) between debug connector and chipset test interfaces can be removed when debug is no longer needed; however, there might be a need to keep the strap resistor and the external components in place for the non debug usage of the interfaces; for example the “OR” gates associated with the VCCST/VCCSTG Power Override Mechanism in [Intel® DCI Implementation](#) on page 500

## 12.2 Additional Test Points

In order to help Intel with further debug, please route all the TP, RSVD\_TP and GPD11 / LANPHYPC /DSWLDO\_MON as testpoints.