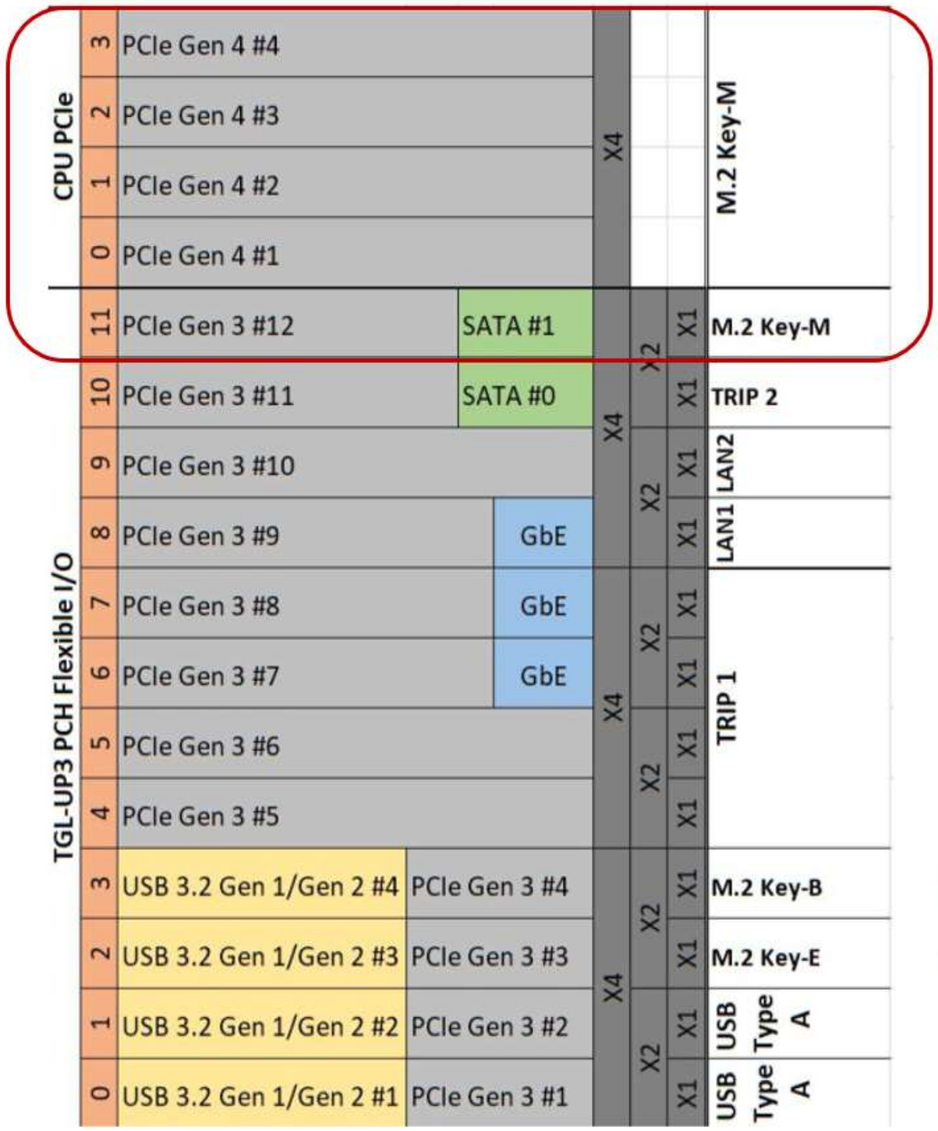
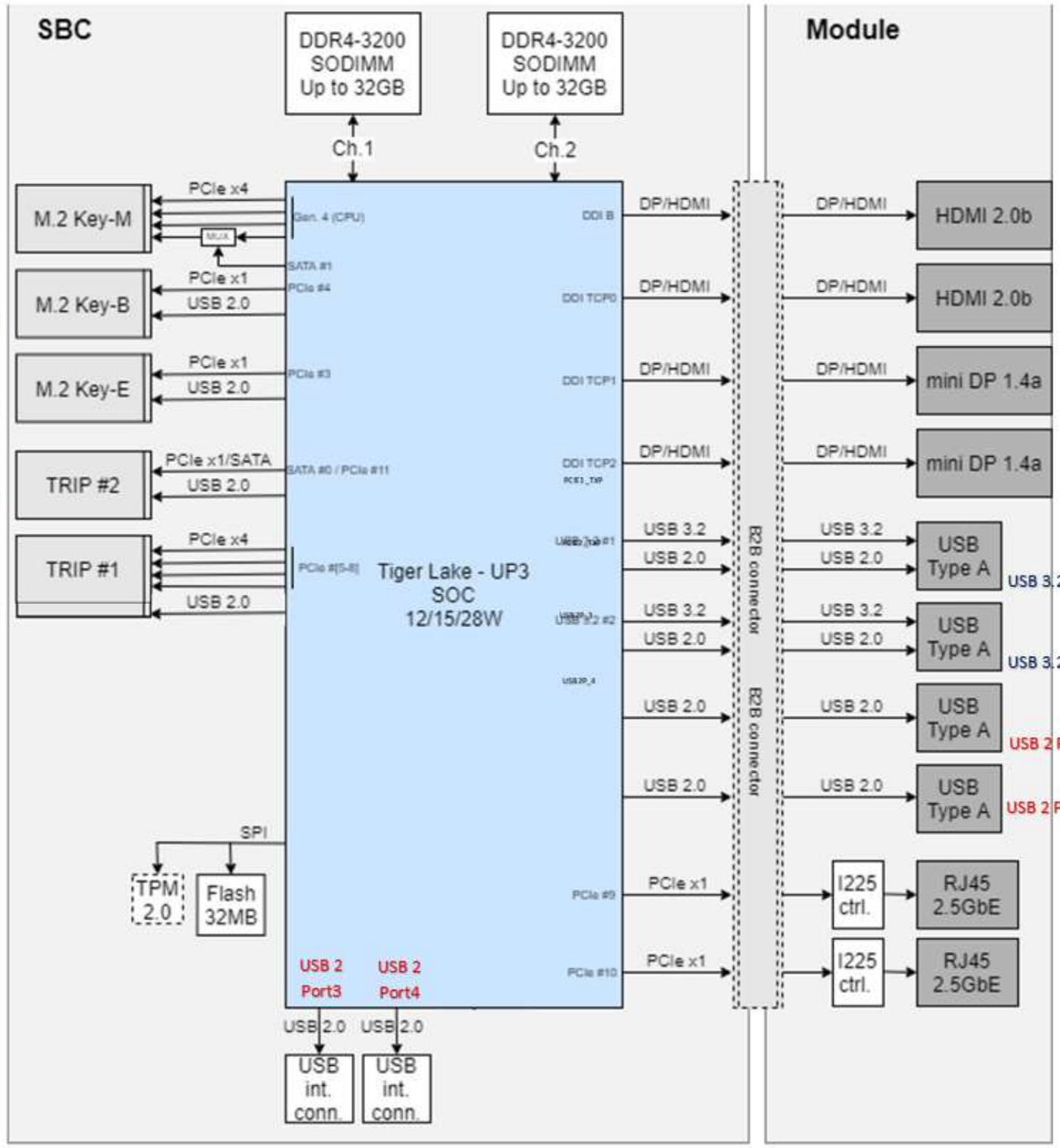


SSD (NVMe Gen 4)

WWAN

WiFi/BT



TRIP 1 & 2:

FT.CA-LAN4
FT.C-LAN2
FT.EC-USB2V4
FT.ED-USB3PCIV4
FT.F-M2NVME
FT.HA-SER1
FT.H-SER4
FT.I-M2B
FT.J-M2E
FT.L-PCIEmini
FT.M-TBT2
FT.N-PCIEx16
FT.Q-CAN
FT.S-GPIO
FT.T-SATA1
FT.U-POE2
FT.W-OPLN2

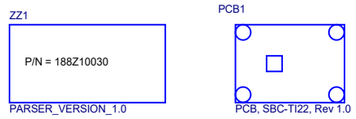
Tiger Lake UP3 Platform

Tiger Lake UP3 Key Feature Summary

Feature	Description
Thermal (SoC)	UP3 4+2: 15W
SoC	TGL UP3 CPU (4+2) PCH – LP
CPU IO	PCIe Gen4, 4x Type-C (TBT, USB 4.0, DP), DDR4,LPDDR4x, LPDDR5, CSI, DSi, DDI, eDP
PCH-LP	12 lanes HSIO, USB2, USB 3.2, eSPI, SPI, LPSS, I2C, SMBus
Power Delivery	CPU FIVR/PCH FIVR w/discrete VR ROP USB-C PD Controller
Memory	DDR4 - Max 64GB @ 3200MT/s LPDDR4x - Max 32GB @ 4266MT/s
Storage	PCIe/SATA
Boot	SPI NOR
Discrete Graphics	Optional x4 PCIe – Hybrid Graphics support w/Hot Plug
Internal Display	eDP , MIPI DSI
External displays	4 Wired Type-C (DP/TBT) Wireless (Miracast2.0 r2) (Wi-Fi) DDI(DP, HDMI)
Wireless	Quasar CNVi w/Harrison Peak (Wi-Fi/BT) module WWAN – XMM 7560
Clocking	38.4MHz Platform Xtal
Wired COMMs	Integrated GbE w/ discrete Gbit Lan Phy

continued...

Feature	Description
Imaging	4x WF/UF 2D Camera – (13MP WF, 2MP UF, 2MP Others) Other Cameras: AutoFocus, Face Tracking, Image Biometrics
Docking/Walk-up-Port	4x Ports Max: Type-C/Type-A
Audio	3.5mm Headphone Jack, Integrated Speakers/Mic, Docking Soundwire, Intel HD Audio, I2S, USB
Sensors	Ambient Light Sensor, Gyroscope, Accelerometer, Compass, Proximity, Pressure
Misc, GPIO's	Power/Vol button/Indicator LEDs/Keyboard/Touchpad/etc



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TIGER LAKE PCH:

The PCH provides extensive I/O support. The functions and capabilities include:
- ACPI Power Management Logic Support, Revision 5.0a
- PCI Express Base Specification Revision 3.0
- Integrated Serial ATA Host controller 3.2, supports data transfer rates of up to 6 Gb/s on all ports
- USB 3.2 Gen 2x1 (10 Gb/s) eXtensible Host Controller (xHCI)
- USB 3.2 Gen 1x1 (5 Gb/s) Dual Role (eXtensible Device Controller - xDCI) Capability
- Serial Peripheral Interface (SPI)
- Enhanced Serial Peripheral Interface (eSPI)
- Flexible I/O–Allows some high speed I/O signals to be configured as PCIe or USB 3.2
- General Purpose Input Output (GPIO)
- Interrupt controller
- Timer functions
- System Management Bus (SMBus) Specification, Version 2.0
- Integrated Clock Controller (ICC)/Real Time Clock Controller (RTCC)
- Intel® High Definition Audio and Intel® Smart Sound Technology (Intel® SST), supporting I2S, MIPI* SoundWire*, and DMIC
- Intel® Serial I/O UART Host controllers
- Intel® Serial I/O I2C Host controllers
- Integrated 10/100/1000 Gigabit Ethernet MAC
- Integrated Sensor Hub (ISH)
- Supports Intel® Rapid Storage Technology (Intel® RST)
- Supports Intel® Active Management Technology (Intel® AMT) (AMT)
- Supports Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Supports Intel® Trusted Execution Technology (Intel® TXT)
- JTAG Boundary Scan support
- Intel® Trace Hub (Intel® TH) and Direct Connect Interface (DCI) for debug
- Supports Intel® CSME (CSME)
- Supports Integrated connectivity (CNVi)

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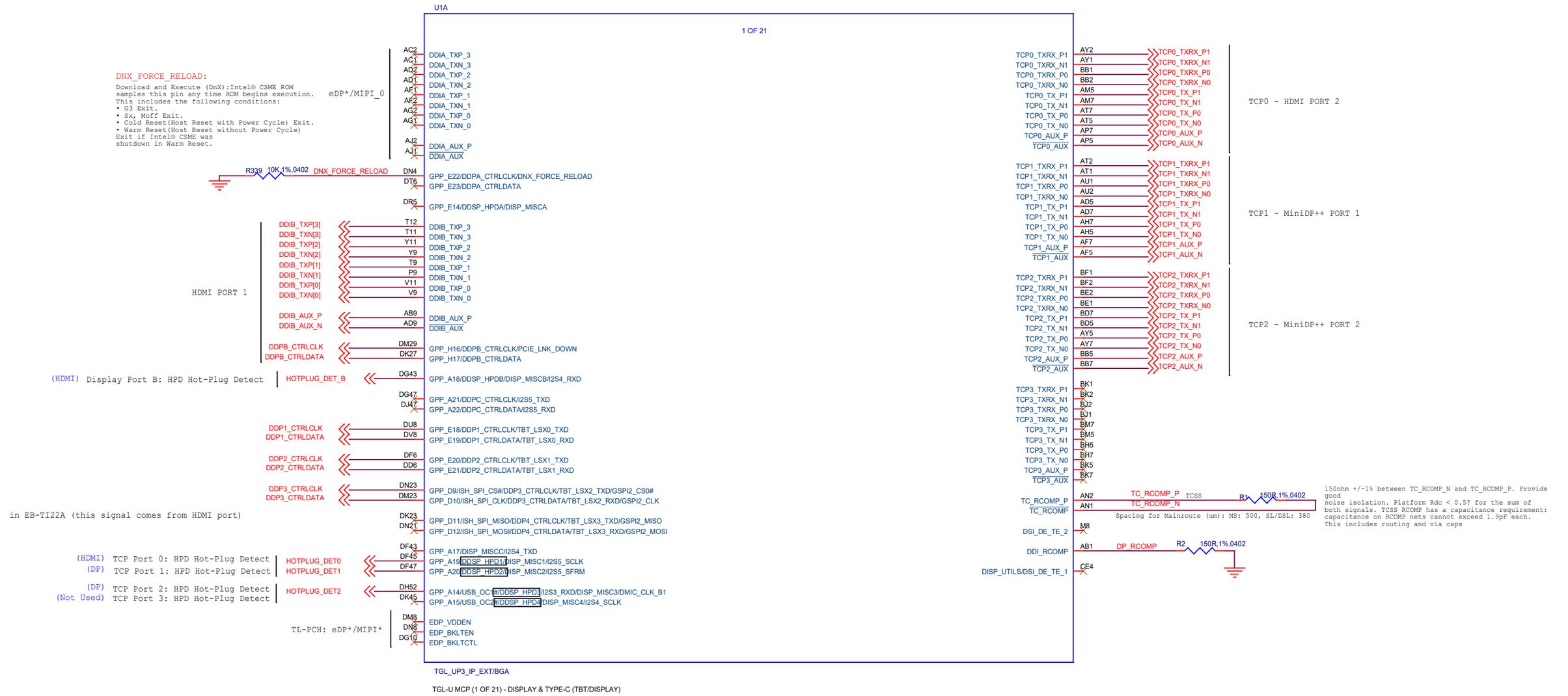
MCP -DP\HDMI



5.3 Display Interfaces

Table 33. DDI Ports Availability

SKU	UP4 Processor Line	UP3 Processor Line
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	eDP*/DP*/HDMI*/MIPI_1	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*
Note: HBR3 supported on TCP ports only. Each of the TCP port can support DPoC* (DisplayPort* over Type-C)		

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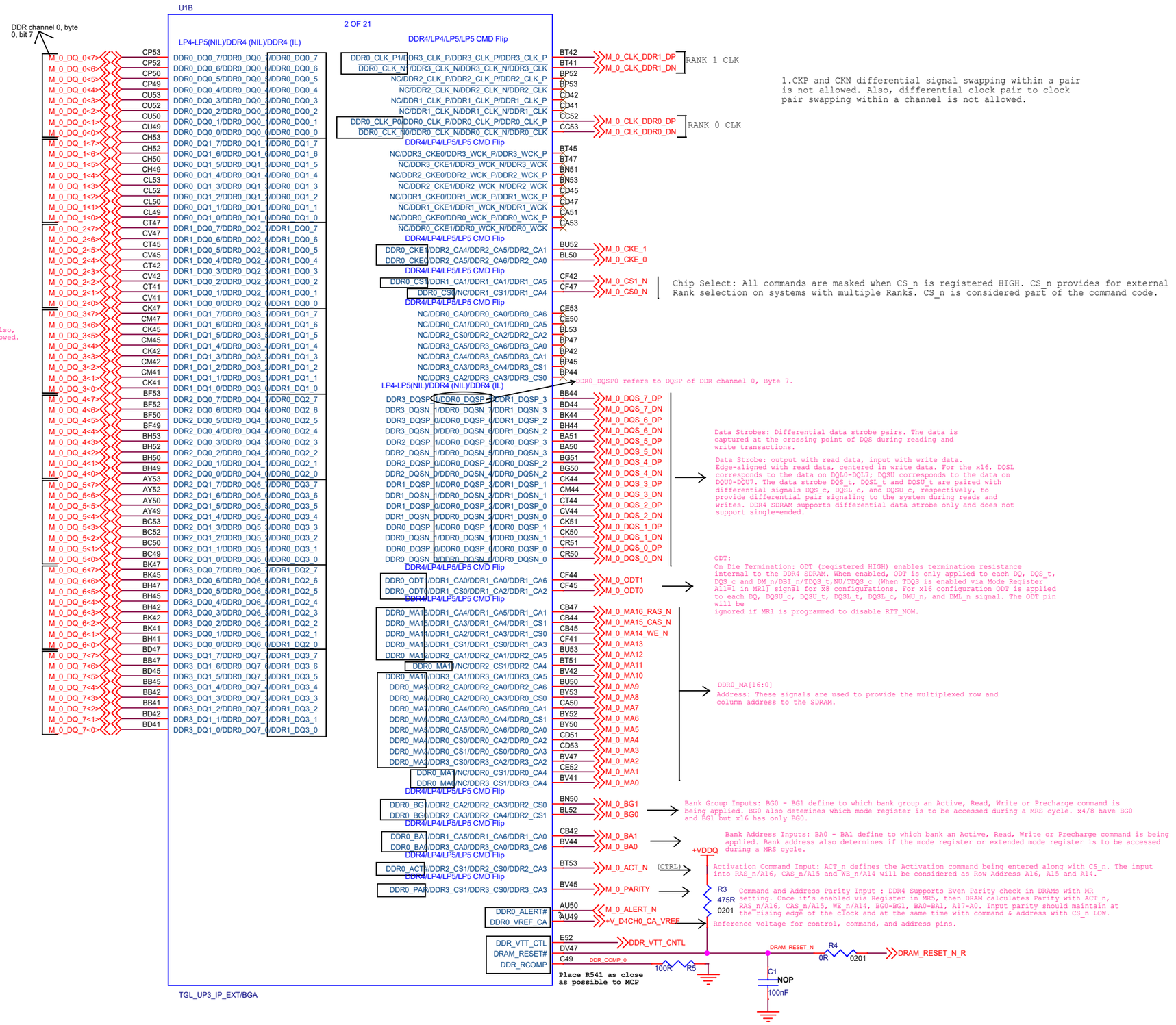
MEMORY CHANNEL A



1.CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.
2.DQ Bit swapping is allowed within the same byte
3.Byte Swapping is allowed within the same channel
4.DQSP and DQSN differential signal swapping within a pair is not allowed.

NOTES:

Each lane of 8bits (Byte) of Data has it's own Data Strobe

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS and register
BA0, BA1	Regsiter bank select input	SDA	I^2C serial data line for SPD/TS and register
BG0, BG1	Regsiter bank group select input	SA0-SA2	I^2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power
WE_n[4]	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12V	Optional Power Supply on socket but not used on RDIMM
CKE0, CEK1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of dif-ferential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.

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MEMORY CHANNEL B

AL53: DDR4_DQ0[7]/DDR1_DQ0[7]
DDR channel 4(1), Byte 0, Bit 7

U1C
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		LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_0<7>	AL53	DDR4_DQ0_7/DDR1_DQ0_7/DDR0_DQ4_7	DDR1_CLK_P1/DDR7_CLK_P/DDR7_CLK_P/DDR7_CLK_P	R41	M_1_CLK_DDR1_DP
M_1_DQ_0<6>	AL52	DDR4_DQ0_6/DDR1_DQ0_6/DDR0_DQ4_6	DDR1_CLK_N1/DDR7_CLK_N/DDR7_CLK_N/DDR7_CLK	R42	M_1_CLK_DDR1_DN
M_1_DQ_0<5>	AL50	DDR4_DQ0_5/DDR1_DQ0_5/DDR0_DQ4_5	NC/DDR6_CLK_P/DDR6_CLK_P/DDR6_CLK_P	M52	
M_1_DQ_0<4>	AL49	DDR4_DQ0_4/DDR1_DQ0_4/DDR0_DQ4_4	NC/DDR6_CLK_N/DDR6_CLK_N/DDR6_CLK	M53	
M_1_DQ_0<3>	AP53	DDR4_DQ0_3/DDR1_DQ0_3/DDR0_DQ4_3	NC/DDR5_CLK_P/DDR5_CLK_P/DDR5_CLK_P	AC42	
M_1_DQ_0<2>	AP52	DDR4_DQ0_2/DDR1_DQ0_2/DDR0_DQ4_2	NC/DDR5_CLK_N/DDR5_CLK_N/DDR5_CLK	AC41	
M_1_DQ_0<1>	AP50	DDR4_DQ0_1/DDR1_DQ0_1/DDR0_DQ4_1	DDR1_CLK_P0/DDR4_CLK_P/DDR4_CLKP/DDR4_CLK_P	Y52	M_1_CLK_DDR0_DP
M_1_DQ_0<0>	AP49	DDR4_DQ0_0/DDR1_DQ0_0/DDR0_DQ4_0	DDR1_CLK_N0/DDR4_CLK_N/DDR4_CLK_N/DDR4_CLK	Y53	M_1_CLK_DDR0_DN
M_1_DQ_1<7>	AF53	DDR4_DQ1_7/DDR1_DQ1_7/DDR0_DQ5_7	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_1<6>	AF52	DDR4_DQ1_6/DDR1_DQ1_6/DDR0_DQ5_6	NC/DDR7_CKE0/DDR7_WCK_P/DDR7_WCK_P	R47	
M_1_DQ_1<5>	AF50	DDR4_DQ1_5/DDR1_DQ1_5/DDR0_DQ5_5	NC/DDR7_CKE1/DDR7_WCK_N/DDR7_WCK	R45	
M_1_DQ_1<4>	AF49	DDR4_DQ1_4/DDR1_DQ1_4/DDR0_DQ5_4	NC/DDR6_CKE0/DDR6_WCK_P/DDR6_WCK_P	K51	
M_1_DQ_1<3>	AH53	DDR4_DQ1_3/DDR1_DQ1_3/DDR0_DQ5_3	NC/DDR6_CKE1/DDR6_WCK_N/DDR6_WCK	K53	
M_1_DQ_1<2>	AH52	DDR4_DQ1_2/DDR1_DQ1_2/DDR0_DQ5_2	NC/DDR5_CKE0/DDR5_WCK_P/DDR5_WCK_P	AC47	
M_1_DQ_1<1>	AH50	DDR4_DQ1_1/DDR1_DQ1_1/DDR0_DQ5_1	NC/DDR5_CKE1/DDR5_WCK_N/DDR5_WCK	AC45	
M_1_DQ_1<0>	AH49	DDR4_DQ1_0/DDR1_DQ1_0/DDR0_DQ5_0	NC/DDR4_CKE0/DDR4_WCK_P/DDR4_WCK_P	W51	
M_1_DQ_2<7>	AR41	DDR5_DQ0_7/DDR1_DQ2_7/DDR1_DQ4_7	NC/DDR4_CKE1/DDR4_WCK_N/DDR4_WCK	W53	
M_1_DQ_2<6>	AV42	DDR5_DQ0_6/DDR1_DQ2_6/DDR1_DQ4_6	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_2<5>	AR42	DDR5_DQ0_5/DDR1_DQ2_5/DDR1_DQ4_5	DDR1_CKE1/DDR6_CA4/DDR6_CA5/DDR6_CA1	P52	M_1_CKE_1
M_1_DQ_2<4>	AV41	DDR5_DQ0_4/DDR1_DQ2_4/DDR1_DQ4_4	DDR1_CKE0/DDR6_CA5/DDR6_CA6/DDR6_CA0	J50	M_1_CKE_0
M_1_DQ_2<3>	AR45	DDR5_DQ0_3/DDR1_DQ2_3/DDR1_DQ4_3	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_2<2>	AV45	DDR5_DQ0_2/DDR1_DQ2_2/DDR1_DQ4_2	DDR1_CS1/DDR5_CA1/DDR5_CA1/DDR5_CA5	AE42	M_1_CS1_N
M_1_DQ_2<1>	AR47	DDR5_DQ0_1/DDR1_DQ2_1/DDR1_DQ4_1	DDR1_CS0/NC/DDR5_CS1/DDR5_CA4	AE47	M_1_CS0_N
M_1_DQ_2<0>	AV47	DDR5_DQ0_0/DDR1_DQ2_0/DDR1_DQ4_0	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_3<7>	AJ41	DDR5_DQ1_7/DDR1_DQ3_7/DDR1_DQ5_7	NC/DDR7_CA5/DDR7_CA6/DDR7_CA0	N42	
M_1_DQ_3<6>	AJ42	DDR5_DQ1_6/DDR1_DQ3_6/DDR1_DQ5_6	NC/DDR7_CA4/DDR7_CA5/DDR7_CA1	N45	
M_1_DQ_3<5>	AL41	DDR5_DQ1_5/DDR1_DQ3_5/DDR1_DQ5_5	NC/DDR7_CA3/DDR7_CA4/DDR7_CS1	N44	
M_1_DQ_3<4>	AL42	DDR5_DQ1_4/DDR1_DQ3_4/DDR1_DQ5_4	NC/DDR7_CA2/DDR7_CA3/DDR7_CS0	N47	
M_1_DQ_3<3>	AJ45	DDR5_DQ1_3/DDR1_DQ3_3/DDR1_DQ5_3	NC/DDR6_CS0/DDR6_CA2/DDR6_CA2	J53	
M_1_DQ_3<2>	AJ47	DDR5_DQ1_2/DDR1_DQ3_2/DDR1_DQ5_2	NC/DDR4_CA1/DDR4_CA1/DDR4_CA5	AC50	
M_1_DQ_3<1>	AL45	DDR5_DQ1_1/DDR1_DQ3_1/DDR1_DQ5_1	NC/DDR4_CA0/DDR4_CA0/DDR4_CA6	AC53	
M_1_DQ_3<0>	AL47	DDR5_DQ1_0/DDR1_DQ3_0/DDR1_DQ5_0	LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)		
M_1_DQ_4<7>	A43	DDR6_DQ0_7/DDR1_DQ4_7/DDR0_DQ6_7	DDR7_DQSP_1/DDR1_DQSP_7/DDR1_DQSP_7	K36	M_1_DQS_7_DP
M_1_DQ_4<6>	B43	DDR6_DQ0_6/DDR1_DQ4_6/DDR0_DQ6_6	DDR7_DQSN_1/DDR1_DQSN_7/DDR1_DQSN_7	K38	M_1_DQS_7_DN
M_1_DQ_4<5>	D43	DDR6_DQ0_5/DDR1_DQ4_5/DDR0_DQ6_5	DDR7_DQSP_0/DDR1_DQSP_6/DDR1_DQSP_6	G44	M_1_DQS_6_DP
M_1_DQ_4<4>	E44	DDR6_DQ0_4/DDR1_DQ4_4/DDR0_DQ6_4	DDR7_DQSN_0/DDR1_DQSN_6/DDR1_DQSN_6	J44	M_1_DQS_6_DN
M_1_DQ_4<3>	A46	DDR6_DQ0_3/DDR1_DQ4_3/DDR0_DQ6_3	DDR6_DQSP_1/DDR1_DQSP_5/DDR0_DQSP_7	D39	M_1_DQS_5_DP
M_1_DQ_4<2>	B46	DDR6_DQ0_2/DDR1_DQ4_2/DDR0_DQ6_2	DDR6_DQSN_1/DDR1_DQSN_5/DDR0_DQSN_7	C39	M_1_DQS_5_DN
M_1_DQ_4<1>	D46	DDR6_DQ0_1/DDR1_DQ4_1/DDR0_DQ6_1	DDR6_DQSP_0/DDR1_DQSP_4/DDR0_DQSP_6	C45	M_1_DQS_4_DP
M_1_DQ_4<0>	E47	DDR6_DQ0_0/DDR1_DQ4_0/DDR0_DQ6_0	DDR6_DQSN_0/DDR1_DQSN_4/DDR0_DQSN_6	D45	M_1_DQS_4_DN
M_1_DQ_5<7>	E38	DDR6_DQ1_7/DDR1_DQ5_7/DDR0_DQ7_7	DDR5_DQSP_1/DDR1_DQSP_3/DDR1_DQSP_5	AJ44	M_1_DQS_3_DP
M_1_DQ_5<6>	D38	DDR6_DQ1_6/DDR1_DQ5_6/DDR0_DQ7_6	DDR5_DQSN_1/DDR1_DQSN_3/DDR1_DQSN_5	AL44	M_1_DQS_3_DN
M_1_DQ_5<5>	B38	DDR6_DQ1_5/DDR1_DQ5_5/DDR0_DQ7_5	DDR5_DQSP_0/DDR1_DQSP_2/DDR1_DQSP_4	AV44	M_1_DQS_2_DP
M_1_DQ_5<4>	A38	DDR6_DQ1_4/DDR1_DQ5_4/DDR0_DQ7_4	DDR5_DQSN_0/DDR1_DQSN_2/DDR1_DQSN_4	AR44	M_1_DQS_2_DN
M_1_DQ_5<3>	E41	DDR6_DQ1_3/DDR1_DQ5_3/DDR0_DQ7_3	DDR4_DQSP_1/DDR1_DQSP_1/DDR0_DQSP_5	AG51	M_1_DQS_1_DP
M_1_DQ_5<2>	D40	DDR6_DQ1_2/DDR1_DQ5_2/DDR0_DQ7_2	DDR4_DQSN_1/DDR1_DQSN_1/DDR0_DQSN_5	AG50	M_1_DQS_1_DN
M_1_DQ_5<1>	B40	DDR6_DQ1_1/DDR1_DQ5_1/DDR0_DQ7_1	DDR4_DQSP_0/DDR1_DQSP_0/DDR0_DQSP_4	AN51	M_1_DQS_0_DP
M_1_DQ_5<0>	A40	DDR6_DQ1_0/DDR1_DQ5_0/DDR0_DQ7_0	DDR4_DQSN_0/DDR1_DQSN_0/DDR0_DQSN_4	AN50	M_1_DQS_0_DN
M_1_DQ_6<7>	G42	DDR7_DQ0_7/DDR1_DQ6_7/DDR1_DQ6_7	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_6<6>	G41	DDR7_DQ0_6/DDR1_DQ6_6/DDR1_DQ6_6	DDR1_ODT1/DDR5_CA0/DDR5_CA0/DDR5_CA6	AE44	M_1_ODT1
M_1_DQ_6<5>	J41	DDR7_DQ0_5/DDR1_DQ6_5/DDR1_DQ6_5	DDR1_ODT0/DDR5_CS0/DDR5_CA2/DDR5_CA2	AE45	M_1_ODT0
M_1_DQ_6<4>	J42	DDR7_DQ0_4/DDR1_DQ6_4/DDR1_DQ6_4	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_6<3>	G45	DDR7_DQ0_3/DDR1_DQ6_3/DDR1_DQ6_3	DDR1_MA16/DDR5_CA4/DDR5_CA5/DDR5_CA1	AA47	M_1_MA16_RAS_N
M_1_DQ_6<2>	J45	DDR7_DQ0_2/DDR1_DQ6_2/DDR1_DQ6_2	DDR1_MA15/DDR5_CA3/DDR5_CA4/DDR5_CS1	AA44	M_1_MA15_CAS_N
M_1_DQ_6<1>	G47	DDR7_DQ0_1/DDR1_DQ6_1/DDR1_DQ6_1	DDR1_MA14/DDR5_CA2/DDR5_CA3/DDR5_CS0	AA45	M_1_MA14_WE_N
M_1_DQ_6<0>	J47	DDR7_DQ0_0/DDR1_DQ6_0/DDR1_DQ6_0	DDR1_MA13/DDR5_CS1/DDR5_CS0/DDR5_CA3	AE41	M_1_MA13
M_1_DQ_7<7>	G38	DDR7_DQ1_7/DDR1_DQ7_7/DDR1_DQ7_7	DDR1_MA12/DDR6_CA1/DDR6_CA1/DDR6_CA5	P53	M_1_MA12
M_1_DQ_7<6>	G36	DDR7_DQ1_6/DDR1_DQ7_6/DDR1_DQ7_6	DDR1_MA11/NC/DDR6_CS1/DDR6_CA4	N51	M_1_MA11
M_1_DQ_7<5>	H36	DDR7_DQ1_5/DDR1_DQ7_5/DDR1_DQ7_5	DDR1_MA10/DDR7_CA1/DDR7_CA1/DDR7_CA5	U42	M_1_MA10
M_1_DQ_7<4>	H38	DDR7_DQ1_4/DDR1_DQ7_4/DDR1_DQ7_4	DDR1_MA9/DDR6_CA0/DDR6_CA0/DDR6_CA6	P50	M_1_MA9
M_1_DQ_7<3>	N36	DDR7_DQ1_3/DDR1_DQ7_3/DDR1_DQ7_3	DDR1_MA8/DDR4_CA2/DDR4_CA3/DDR4_CS0	U53	M_1_MA8
M_1_DQ_7<2>	L36	DDR7_DQ1_2/DDR1_DQ7_2/DDR1_DQ7_2	DDR1_MA7/DDR4_CA4/DDR4_CA5/DDR4_CA1	W50	M_1_MA7
M_1_DQ_7<1>	L38	DDR7_DQ1_1/DDR1_DQ7_1/DDR1_DQ7_1	DDR1_MA6/DDR4_CA3/DDR4_CA4/DDR4_CS1	U52	M_1_MA6
M_1_DQ_7<0>	N38	DDR7_DQ1_0/DDR1_DQ7_0/DDR1_DQ7_0	DDR1_MA5/DDR4_CA5/DDR4_CA6/DDR4_CA0	U50	M_1_MA5
			DDR1_MA4/DDR4_CS0/DDR4_CA2/DDR4_CA2	AA51	M_1_MA4
			DDR1_MA3/DDR4_CS1/DDR4_CS0/DDR4_CA3	AA53	M_1_MA3
			DDR1_MA2/DDR7_CS0/DDR7_CA2/DDR7_CA2	U47	M_1_MA2
			DDR1_MA1/NC/DDR4_CS1/DDR4_CA4	AC52	M_1_MA1
			DDR1_MA0/NC/DDR7_CS1/DDR7_CA4	U41	M_1_MA0
			DDR4/LP4/LP5/LP5 CMD Flip		
			DDR1_BG1/DDR6_CA2/DDR6_CA3/DDR6_CS0	K50	M_1_BG1
			DDR1_BG0/DDR6_CA3/DDR6_CA4/DDR6_CS1	J52	M_1_BG0
			DDR4/LP4/LP5/LP5 CMD Flip		
			DDR1_BA1/DDR5_CA5/DDR5_CA6/DDR5_CA0	AA42	M_1_BA1
			DDR1_BA0/DDR7_CA0/DDR7_CA0/DDR7_CA6	U44	M_1_BA0
			DDR1_ACT#/DDR6_CS1/DDR6_CS0/DDR6_CA3	N53	M_1_ACT_N
			DDR1_PAR/DDR7_CS1/DDR7_CS0/DDR7_CA3	U45	M_1_PARITY
			DDR1_ALERT#	AU53	M_1_ALERT_N
			DDR1_VREF_CA	AU52	+V_D4CH1_CA_VREF

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CATERR#

Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.

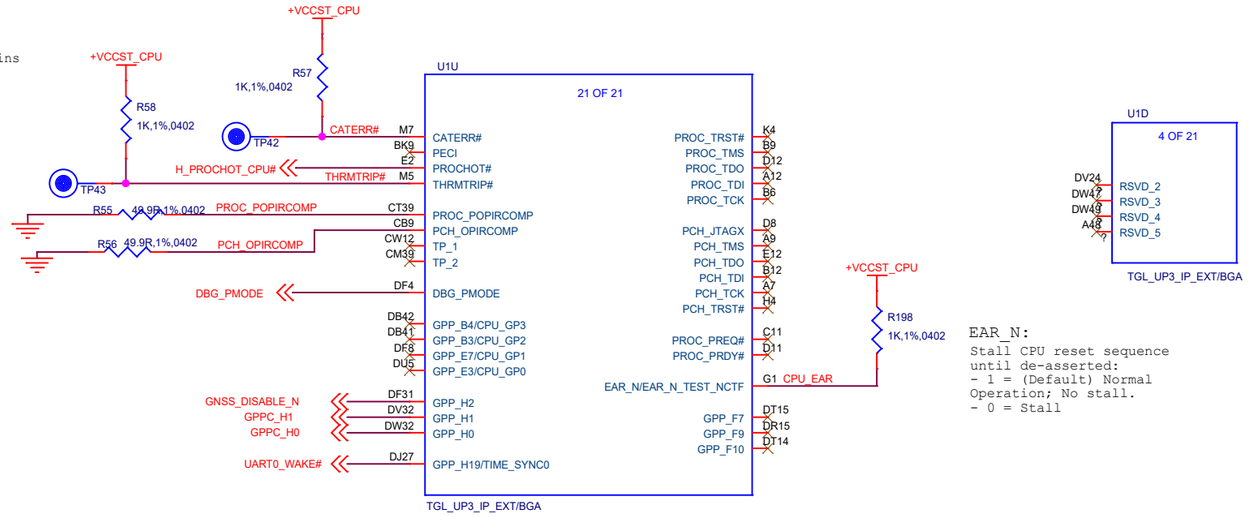
PROCHOT#

The PROCHOT# (processor hot) signal is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling. The PROCHOT# signal can be configured to the following modes:

- Input Only: PROCHOT is driven by an external device.
- Output Only: PROCHOT is driven by processor.
- Bi-Directional: Both Processor and external device can drive PROCHOT signal

Time Synchronization GPIO 0: Timed GPIO event for time synchronization for interfaces that do not support time synchronization natively.

Time Synchronization: Used for synchronization both input (latch time when pin asserted) and output (toggle pin when programmed time is hit).



EAR_N:
Stall CPU reset sequence until de-asserted:
- 1 = (Default) Normal Operation; No stall.
- 0 = Stall

TIME_SYNC:
The PCH supports two Timed GPIOs as native function (TIME_SYNC) that is muxed on GPIO pins. The intent usage of the Timed GPIO function is for time synchronization purpose.
Timed GPIO can be an input or an output.
• As an input, a GPIO input event triggers the HW to capture the PCH Always Running Timer (ART) time in the Time Capture register. The GPIO input event must be asserted for at least two crystal oscillator clocks period in order for the event to be recognized.
• As an output, a match between the ART time and the software programmed time value triggers the HW to generate a GPIO output event and capture the ART time in the Time Capture register. If periodic mode is enabled, HW generates the
periodic GPIO events based on the programmed interval. The GPIO output event is asserted by HW for at least two crystal oscillator clocks period.

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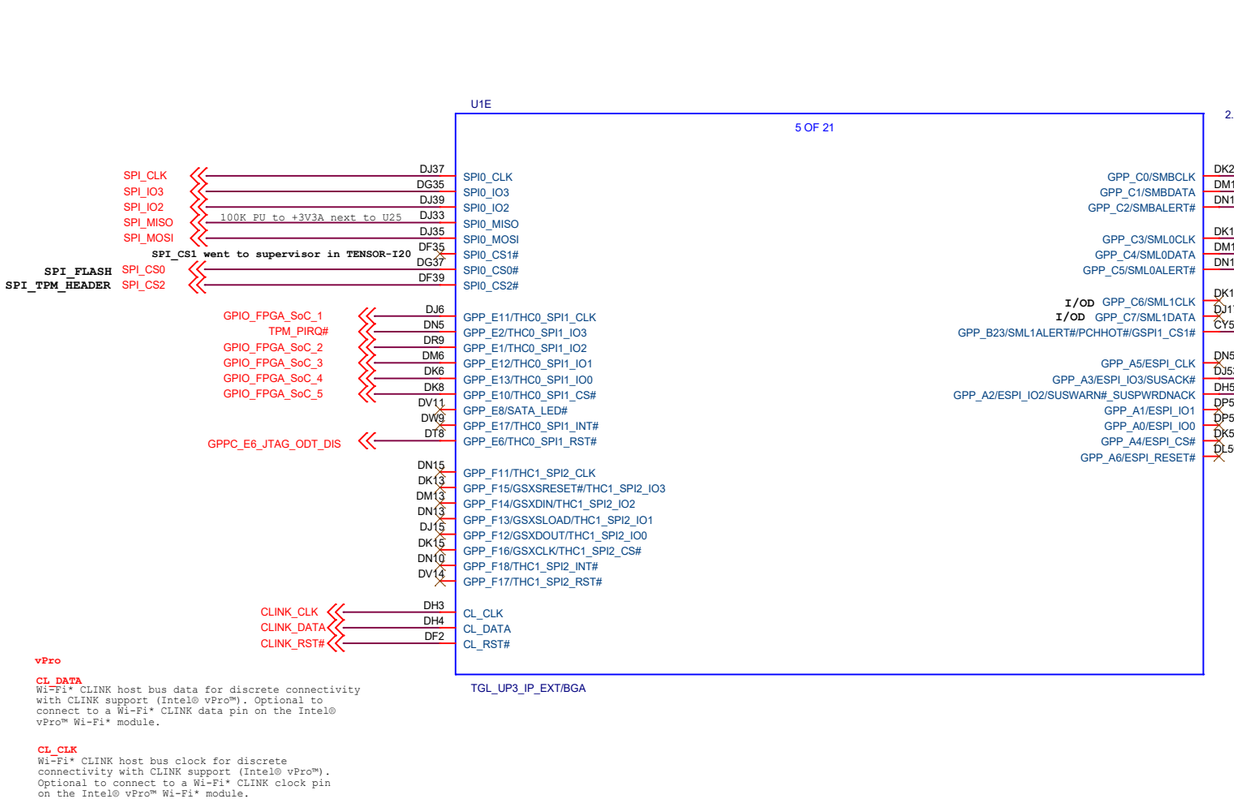


vPro

CL_DATA
Wi-Fi* CLINK host bus data for discrete connectivity with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK data pin on the Intel® vPro™ Wi-Fi* module.

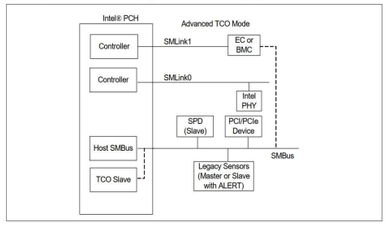
CL_CLK
Wi-Fi* CLINK host bus clock for discrete connectivity with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK clock pin on the Intel® vPro™ Wi-Fi* module.

SML0CLK & SML0DATA
System Management Link clock signal interface to Intel® Ethernet Connection I219. Refer to System Management Interface and SMLink for details on the SML0CLK signal.
Note: The Intel® Ethernet Connection I219 connects to SML0CLK signal.

FUNCTIONALITY:
The SMLink interfaces are controlled by the Intel® CSME.
SMLink0 is mainly used for integrated LAN. When an Intel LAN PHY is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of up to 1 MHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled using a soft strap.
SMLink1 can be used with an Embedded Controller (EC) or Baseboard Management Controller (BMC). Both SMLink0 and SMLink1 support up to 1 MHz.

SUSACK# & SUSWARN#:
This function is only applicable to platforms supporting Deep Sleep Wells
This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (using SLP_SUS#). The EC/ motherboard control logic must observe edges on this pin, preparing
for Primary well power loss on a falling edge and preparing for Prim
well related activity (host/Intel ME wakes and runtime events) on a
rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#.

SMBus / SMlink Connectivity (Advanced TCO Mode)



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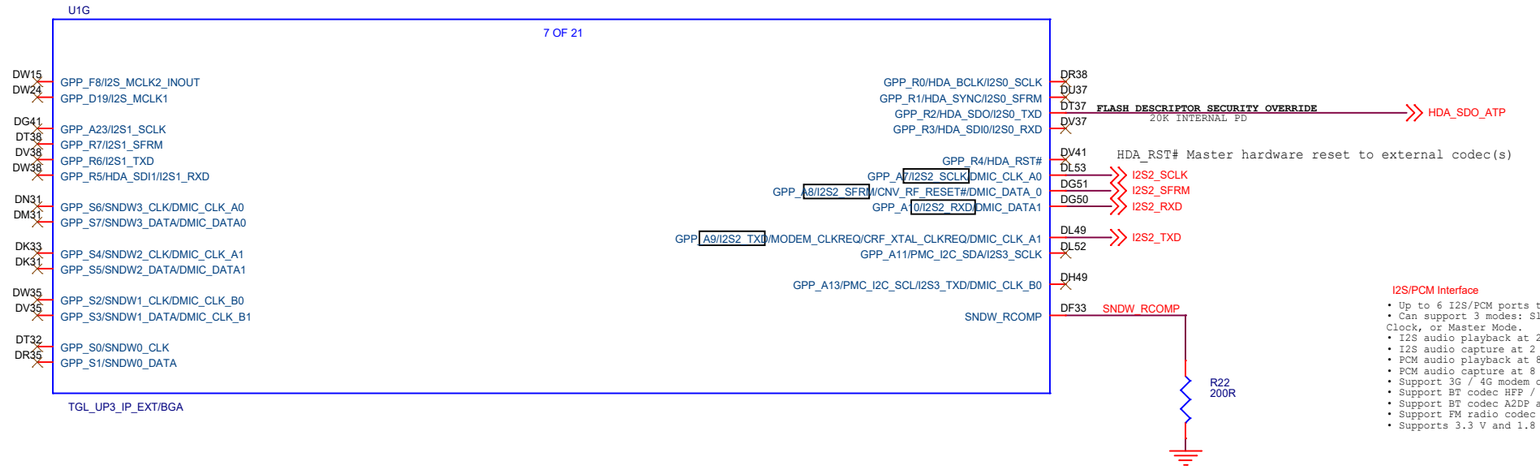
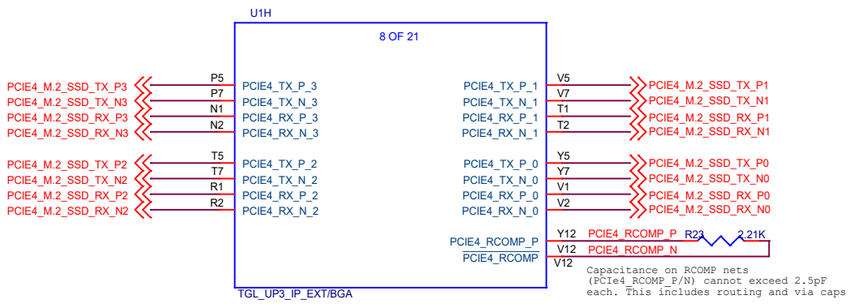


PCIE GEN 4 CAPS: p.158/270 in TL-SBC



12.2 PCIe4 Gen4 Interface Signals

Signal Name	Description	Dir	Buffer Type	Link Type	Availability
PCIE4_RCOMP_P PCIE4_RCOMP_N	Resistance Compensation for PEG channel	I	Analog	Diff	UP3/UP4/H Processor Lines
PCIE4_TX_P[3:0] PCIE4_TX_N[3:0]	PCIe Transmit Differential Pairs	O	PCIE	Diff	UP3/UP4/H Processor Lines
PCIE4_RX_P[3:0] PCIE4_RX_N[3:0]	PCIe Receive Differential Pairs	I	PCIE	Diff	UP3/UP4/H Processor Lines

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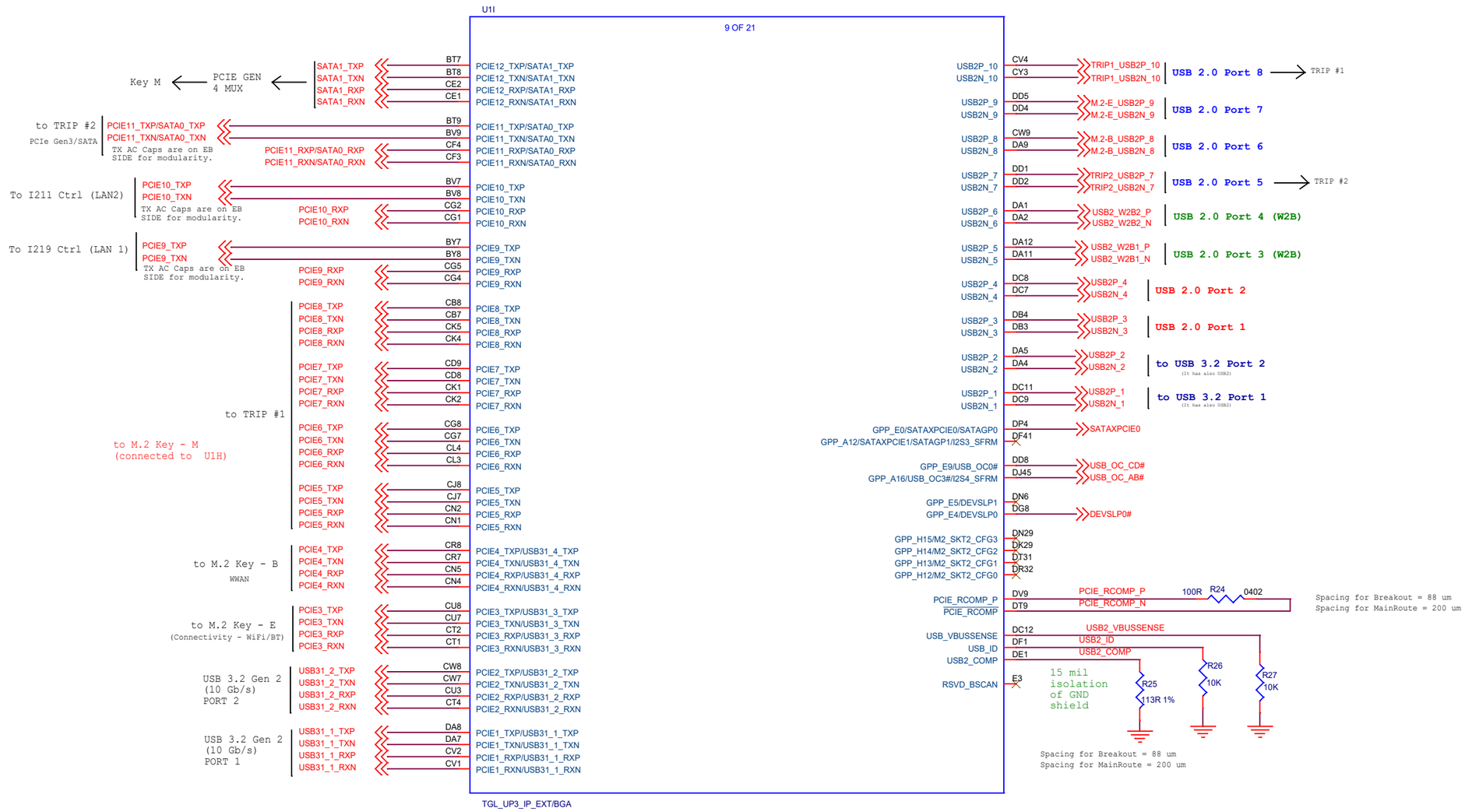

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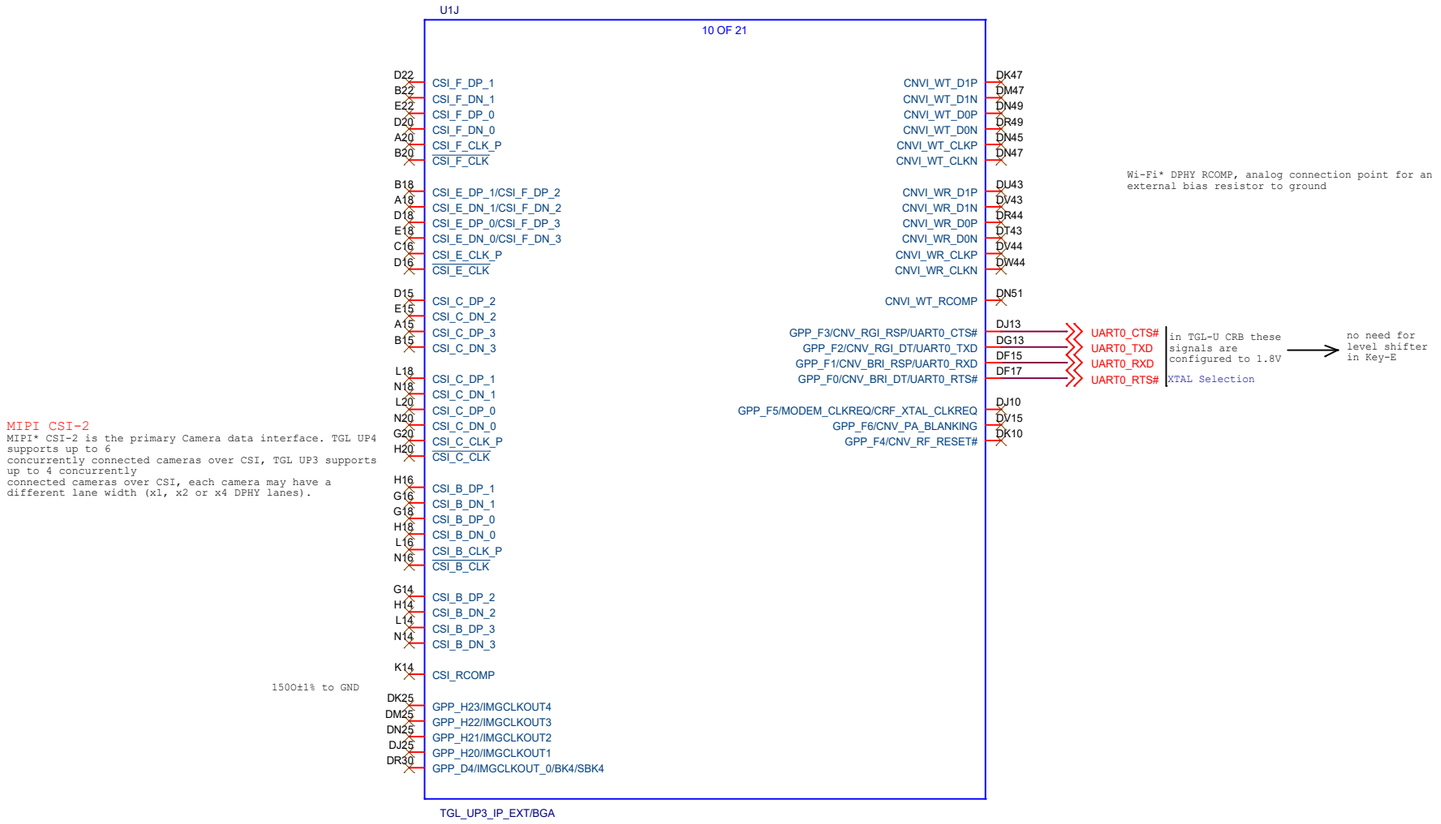

MIPI CSI-2

MIPI* CSI-2 is the primary Camera data interface. TGL UP4 supports up to 6 concurrently connected cameras over CSI, TGL UP3 supports up to 4 concurrently connected cameras over CSI, each camera may have a different lane width (x1, x2 or x4 DPHY lanes).

150Ω±1% to GND

Wi-Fi* DPHY RCOMP, analog connection point for an external bias resistor to ground

UART0_CTS#
UART0_TXD
UART0_RXD
UART0_RTS#

in TGL-U CRB these signals are configured to 1.8V → no need for level shifter in Key-E

XTAL Selection

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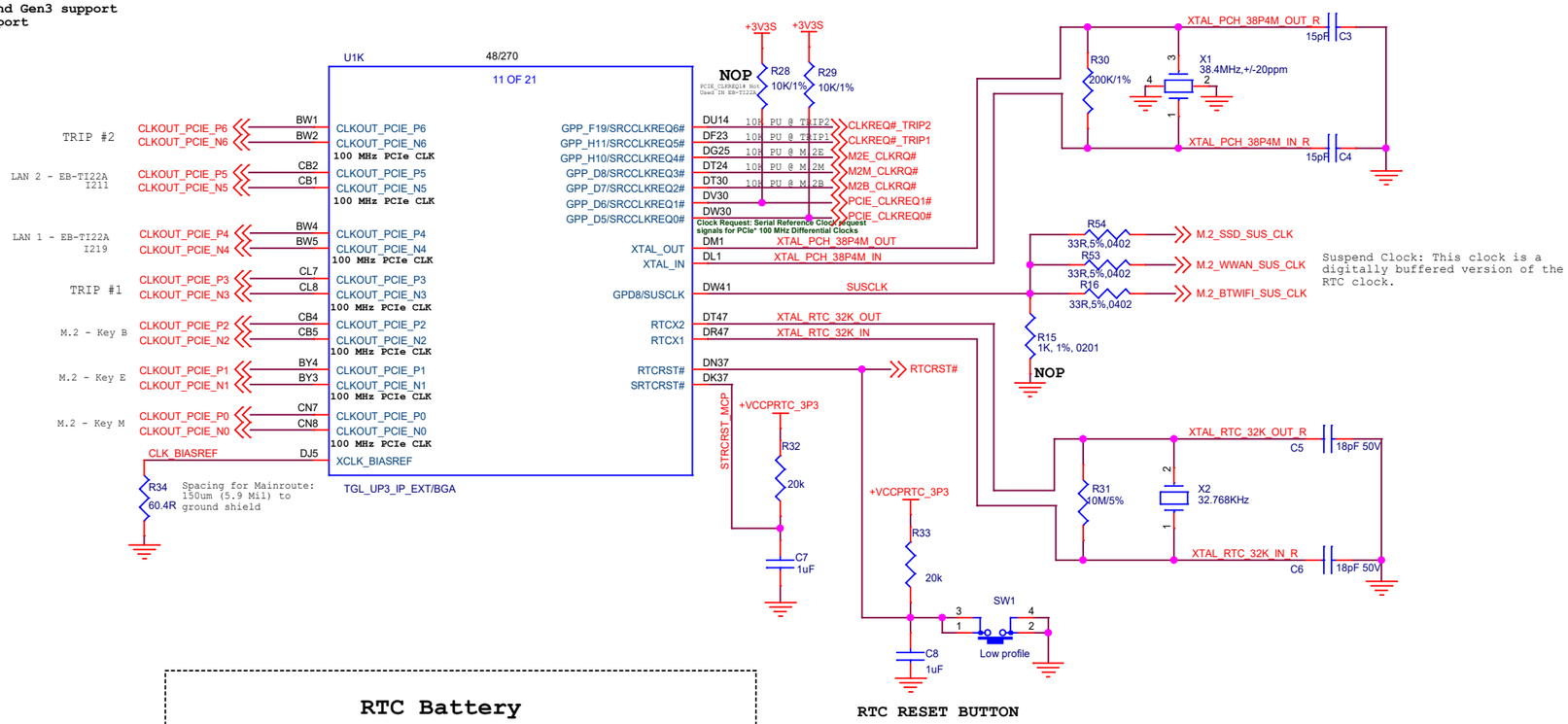
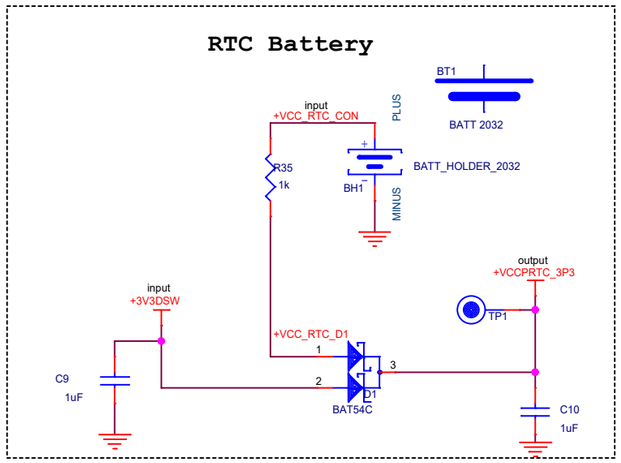
PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices

- **CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support**
- **CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support**



RTC RESET BUTTON



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SLP_S0#
S0 Sleep Control. When PCH is idle and processor is in C10 state, this pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.

SLP_S5#
This signal is for power plane control. When asserted (low), it will shutoff power to all non-critical systems in S5 (Soft Off) states.

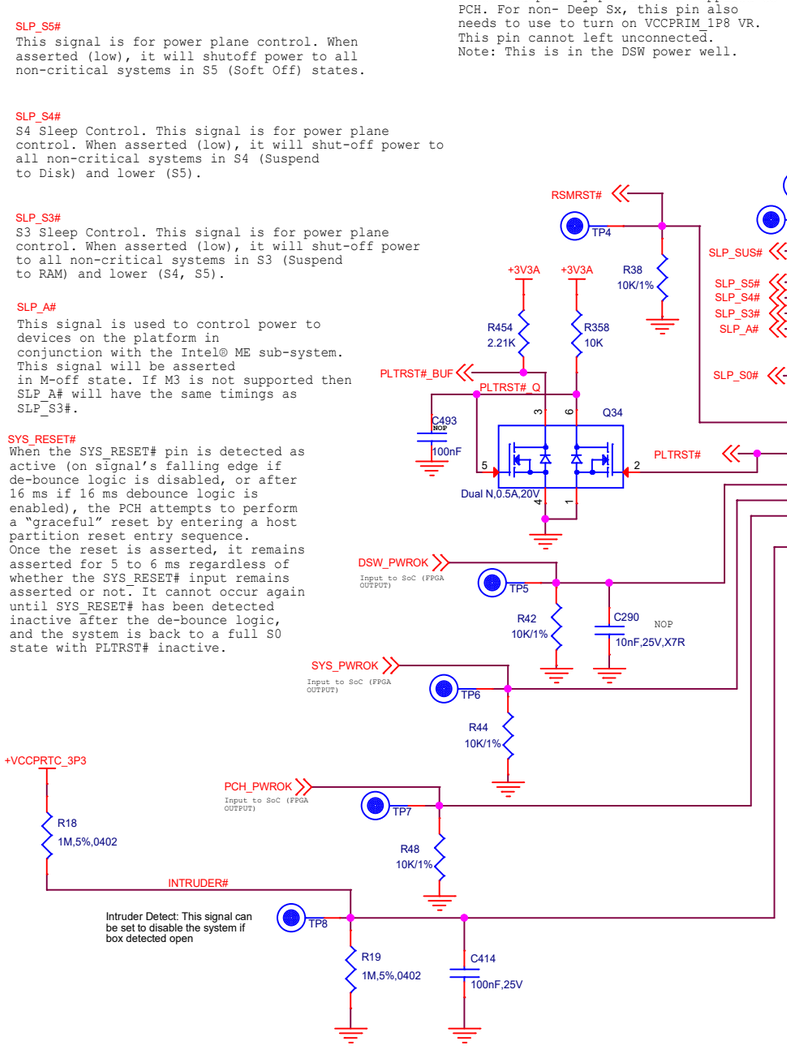
SLP_S4#
S4 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S4 (Suspend to Disk) and lower (S5).

SLP_S3#
S3 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S3 (Suspend to RAM) and lower (S4, S5).

SLP_A#
This signal is used to control power to devices on the platform in conjunction with the Intel® ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timings as SLP_S3#.

SYS_RESET#
When the SYS_RESET# pin is detected as active (on signal's falling edge if de-bounce logic is disabled, or after 16 ms if 16 ms debounce logic is enabled), the PCH attempts to perform a "graceful" reset by entering a host partition reset entry sequence. Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the SYS_RESET# input remains asserted or not. It cannot occur again until SYS_RESET# has been detected inactive after the de-bounce logic, and the system is back to a full S0 state with PLTRST# inactive.

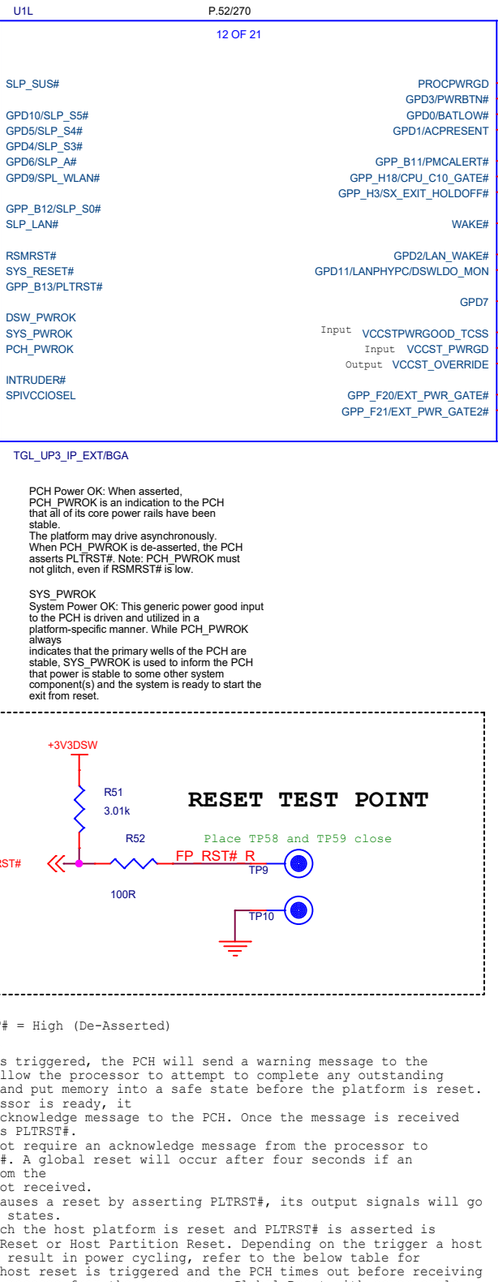
SLP_SUS# (High = Exist from Deep Sx)
Deep Sx Indication: When asserted (driven low), this signal indicates PCH is in Deep Sx state where internal primary power is shut off for enhanced power saving. When de-asserted (driven high), this signal indicates exit from Deep Sx state and primary power can be applied to PCH. For non- Deep Sx, this pin also needs to use to turn on VCCPRIM_1P8 VR. This pin cannot left unconnected.
Note: This is in the DSW power well.



The PCH has an input signal, INTRUDER#, that can be attached to a switch that is activated by the system's case being open. This input has a two RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD_DET bit in the TCTL2 register. The INTRD_SEL bits in the TCTL2 register can enable the PCH to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP_EN bit.

The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD_DET bit. This allows the signal to be used as a GPI if the intruder function is not required.
If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET bit will go to a 0 when INTRUDER# input signal goes inactive.

RTC-Well Input Strap Requirements
All RTC-well inputs (RSMRST#, RTCRST#, SRTCRST#, INTRUDER#, PCH_PWROK, DSW_PWROK) must be either pulled up to VccRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in Figure 63 on page 126 meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PCH_PWROK and DSW_PWROK input signal should also be configured with an external weak pull-down.



PCH Power OK: When asserted, PCH_PWROK is an indication to the PCH that all of its core power rails have been stable.
The platform may drive asynchronously. When PCH_PWROK is de-asserted, the PCH asserts PLTRST#. Note: PCH_PWROK must not glitch, even if RSMRST# is low.

SYS_PWROK
System Power OK: This generic power good input to the PCH is driven and utilized in a platform-specific manner. While PCH_PWROK always
indicates that the primary wells of the PCH are stable, SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset.

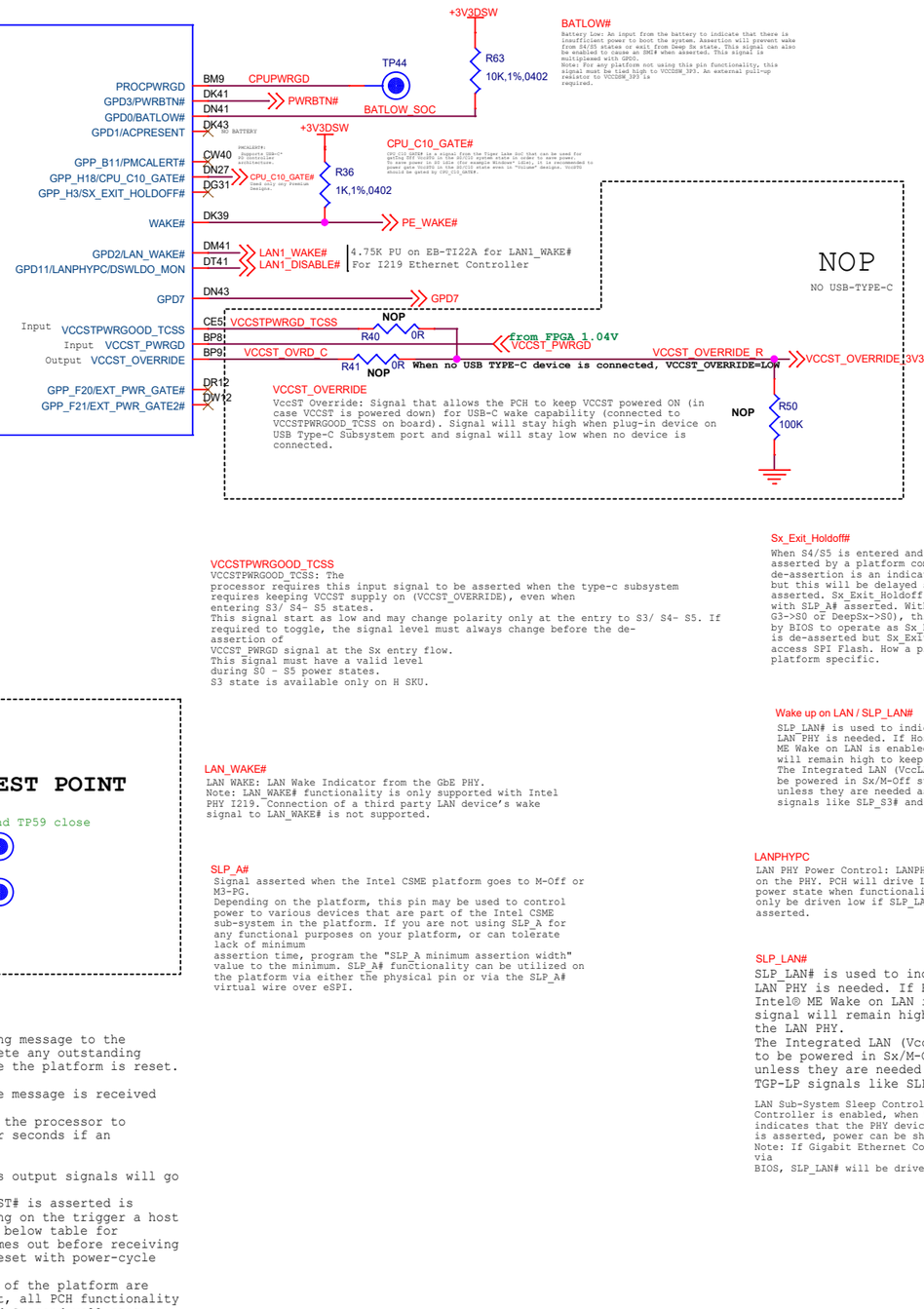
PLTRST# PLTRST# = High (De-Asserted)

Reset Behavior
When a reset is triggered, the PCH will send a warning message to the processor to allow the processor to attempt to complete any outstanding memory cycles and put memory into a safe state before the platform is reset. When the processor is ready, it
will send an acknowledge message to the PCH. Once the message is received the PCH asserts PLTRST#.
The PCH does not require an acknowledge message from the processor to trigger PLTRST#. A global reset will occur after four seconds if an acknowledge from the
processor is not received.
When the PCH causes a reset by asserting PLTRST#, its output signals will go to their reset states.
A reset in which the host platform is reset and PLTRST# is asserted is called a Host Reset or Host Partition Reset. Depending on the trigger a host reset may also result in power cycling, refer to the below table for details. If a host reset is triggered and the PCH times out before receiving an acknowledge message from the processor a Global Reset with power-cycle will occur.
A reset in which the host and Intel® CSME partitions of the platform are reset is called a Global Reset. During a Global Reset, all PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. Intel® CSME and Host power back up after the power-cycle period.
Straight to S5 is another reset type where all power wells that are controlled by the SLP_S3#, SLP_S4#, and SLP_A# pins, as well as SLP_S5# and SLP_LAN# (if pins are not configured as GPIOs), are turned off. All PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. The host stays there until a valid wake event occurs.

WAKE#
WAKE #: Can be used by the LAN PHY as a wake signal.

PCI Express* ports can wake the platform from S4, S5, or Deep Sx using the WAKE# pin. WAKE# is treated as a wake event, but does not cause any bits to go active in the GPE_STS register.

PCI Express* WAKE# pin is an Output in S0ix states hence this pin cannot be used to wake up the system during S0ix states.



BATLOW#
Battery Low: An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S4/S5 states or exit from Deep Sx state. This signal can also be enabled to cause an SMI# when asserted. This signal is multiplexed with GPIO.
Note: For any platform not using this pin functionality, this signal must be tied high to VCCDSW_3P3. An external pull-up resistor to VCCDSW_3P3 is required.

CPU_C10_GATE#
CPU_C10_GATE# is a signal from the Tiger Lake SoC that can be used for platform power optimization. Although this signal is not used for Intel® In-band power in S0 idle (for example Windows* idle), it is recommended to power gate VccRTC in the S0/CO2 state even in "VccLow" designs. VccRTC should be gated by CPU_C10_GATE#.

VCCST_OVERRIDE
VccST Override: Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability (connected to VCCSTPWRGOOD_TCSS on board). Signal will stay high when plug-in device on USB Type-C Subsystem port and signal will stay low when no device is connected.

VCCSTPWRGOOD_TCSS
VCCSTPWRGOOD_TCSS: The processor requires this input signal to be asserted when the type-c subsystem requires keeping VCCST supply on (VCCST_OVERRIDE), even when entering S3/ S4- S5 states.
This signal start as low and may change polarity only at the entry to S3/ S4- S5. If required to toggle, the signal level must always change before the de-assertion of
VCCST_PWRGD signal at the Sx entry flow.
This signal must have a valid level during S0 - S5 power states.
S3 state is available only on H SKU.

LAN_WAKE#
LAN WAKE: LAN Wake Indicator from the GbE PHY.
Note: LAN_WAKE# functionality is only supported with Intel PHY I219. Connection of a third party LAN device's wake signal to LAN_WAKE# is not supported.

SLP_A#
Signal asserted when the Intel CSME platform goes to M-Off or M3-PG.
Depending on the platform, this pin may be used to control power to various devices that are part of the Intel CSME sub-system in the platform. If you are not using SLP_A for any functional purposes on your platform, or can tolerate lack of minimum
assertion time, program the "SLP_A minimum assertion width" value to the minimum. SLP_A# functionality can be utilized on the platform via either the physical pin or via the SLP_A# virtual wire over eSPI.

Sx_Exit_Holdoff#
When S4/S5 is entered and SLP_A# is asserted, Sx_Exit_Holdoff# can be asserted by a platform component to delay resume to S0. SLP_A# de-assertion is an indication of the intent to resume to S0 (power up), but this will be delayed so long as Sx_Exit_Holdoff# is asserted. Sx_Exit_Holdoff is ignored outside of an S4/S5 entry sequence with SLP_A# asserted. With the de-assertion of RSMRST# (either from G3->S0 or DeepSx->S0), this pin is a GPIO input and must be programmed by BIOS to operate as Sx_Exit_Holdoff. When SLP_A# is asserted (or it is de-asserted but Sx_Exit_Holdoff# is asserted), the PCH will not access SPI Flash. How a platform uses this signal is platform specific.

Wake up on LAN / SLP_LAN#
SLP_LAN# is used to indicate when power to the LAN PHY is needed. If Host Wake On LAN or Intel® ME Wake on LAN is enabled, the SLP_LAN# signal will remain high to keep power on to the LAN PHY. The Integrated LAN (VccLAN) rail does not need to be powered in Sx/M-Off state unless they are needed as indicated by the TGP-LP signals like SLP_S3# and SUSPWRDNACK.

LANPHYPC
LAN PHY Power Control: LANPHYPC should be connected to LAN_DISABLE_N on the PHY. PCH will drive LANPHYPC low to put the PHY into a low power state when functionality is not needed. Note: LANPHYPC can only be driven low if SLP_LAN# is de-asserted.

SLP_LAN#
SLP_LAN# is used to indicate when power to the LAN PHY is needed. If Host Wake On LAN or Intel® ME Wake on LAN is enabled, the SLP_LAN# signal will remain high to keep power on to the LAN PHY.
The Integrated LAN (VccLAN) rail does not need to be powered in Sx/M-Off state unless they are needed as indicated by the TGP-LP signals like SLP_S3# and SUSPWRDNACK.

LAN Sub-System Sleep Control: If the Gigabit Ethernet Controller is enabled, when SLP_LAN# is de-asserted (LOW) it indicates that the PHY device must be powered. When SLP_LAN# is asserted, power can be shut off to the PHY device.
Note: If Gigabit Ethernet Controller is statically disabled via
BIOS, SLP_LAN# will be driven low.

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VCCIN, +VDDQ

+VCCIN

Values for Double Sided Board

U1M

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A24	VCCIN_1	VCCIN_66	G32
A26	VCCIN_2	VCCIN_67	H24
A29	VCCIN_3	VCCIN_68	H26
A30	VCCIN_4	VCCIN_69	H30
A33	VCCIN_5	VCCIN_70	H32
A35	VCCIN_6	VCCIN_71	J1
AY39	VCCIN_7	VCCIN_72	J2
B24	VCCIN_8	VCCIN_73	K1
B26	VCCIN_9	VCCIN_74	K2
B29	VCCIN_10	VCCIN_75	K24
B30	VCCIN_11	VCCIN_76	K26
B33	VCCIN_12	VCCIN_77	K30
B35	VCCIN_13	VCCIN_78	K32
BA10	VCCIN_14	VCCIN_79	L24
BA40	VCCIN_15	VCCIN_80	L26
BB39	VCCIN_16	VCCIN_81	L30
BB9	VCCIN_17	VCCIN_82	L32
BC10	VCCIN_18	VCCIN_83	N24
BC40	VCCIN_19	VCCIN_84	N26
BD39	VCCIN_20	VCCIN_85	N30
BD9	VCCIN_21	VCCIN_86	N32
BE10	VCCIN_22	VCCIN_87	P24
BE40	VCCIN_23	VCCIN_88	P26
BF9	VCCIN_24	VCCIN_89	P28
BG10	VCCIN_25	VCCIN_90	P30
BG40	VCCIN_26	VCCIN_91	P32
BH12	VCCIN_27	VCCIN_92	T21
BH39	VCCIN_28	VCCIN_93	T23
BH9	VCCIN_29	VCCIN_94	T25
BJ10	VCCIN_30	VCCIN_95	T27
BJ40	VCCIN_31	VCCIN_96	T31
BK39	VCCIN_32	VCCIN_97	U23
BL10	VCCIN_33	VCCIN_98	U27
BL40	VCCIN_34	VCCIN_99	U29
BM39	VCCIN_35	VCCIN_100	U31
BN40	VCCIN_36	VCCIN_101	U33
BP12	VCCIN_37	VCCIN_102	V23
BP39	VCCIN_38	VCCIN_103	V25
BR10	VCCIN_39	VCCIN_104	V27
BR40	VCCIN_40	VCCIN_105	V29
BT12	VCCIN_41	VCCIN_106	V31
BT39	VCCIN_42	VCCIN_107	V33
BU10	VCCIN_43	VCCIN_108	W22
BU40	VCCIN_44	VCCIN_109	W24
BV12	VCCIN_45	VCCIN_110	W28
BY12	VCCIN_46	VCCIN_111	W32
CA10	VCCIN_47		
CB12	VCCIN_48		
D24	VCCIN_49		
D26	VCCIN_50		
D29	VCCIN_51		
D30	VCCIN_52		
D33	VCCIN_53		
D35	VCCIN_54		
E24	VCCIN_55		
E26	VCCIN_56		
E27	VCCIN_57		
E29	VCCIN_58		
E30	VCCIN_59		
E32	VCCIN_60		
E33	VCCIN_61		
G2	VCCIN_62		
G24	VCCIN_63		
G26	VCCIN_64		
G30	VCCIN_65		

VCCIN_SENSE	R38	VCCIN_VCCSENSE
VSSIN_SENSE	R37	VCCIN_VSSSENSE
VIDSOUT	M12	VCCIN_SVID_DATA
VIDSCK	M11	VCCIN_SVID_CLK
VIDALERT#	P12	VCCIN_SVID_ALERT_N

VCC_VCCIN_SENSE_P
VCC_VCCIN_SENSE_N

At frequencies within the VR's G-BW control, the VR layout placement may be compensated using remote sensing of the voltage at the die through Vcc_SENSE/Vss_SENSE signals.

12 x 10uF 0402 at bottom side

C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22
D402 10uF/10V

Done

NOP

8 x 22uF 0402 at top side

C474 C475 C476 C477 C478
C479 C480 C481
0402 22uF

8 x 22uF 0603 on top side

C28 C29 C30 C31 C32
C36 C37 C38
22uF RC0603

10 x 47uF 0603 on top side

C482 C483 C484 C485 C486 C487 C488 C489 C490 C48
47uF 0603

470uF

NOP

MLCC cap recommendation based on VR solution with 150kHz VR bandwidth or 600kHz switching frequency, assuming BW=1/4 of Fsw. Place board caps as close as possible to package in this order where 0402 to be closest to package pins:

Option 1:
VR->7343->0603->0402->Package
Option 2:
VR->7343->0402->Package

Place on the back side of the SOC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.

Place on the primary side, as close as possible to the vias that connect to the outer row of SoC pins, use wide traces to connect the capacitor pins to the vias. Make sure to put atleast 1 via down near the outer Vdd2 BGA and 1 via down near the cap pad

+VDDQ

U1O

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TGL_UP3_IP_EXT/BGA

AA39	VDD2_1	VCCSTG_OUT_1	AF9
AB40	VDD2_2	VCCSTG_1	AF12
AC39	VDD2_3	VCCSTG_2	AD12
AD40	VDD2_4		
AD51	VDD2_5	VCCSTG_OUT_2	AN10
AD52	VDD2_6	VCCSTG_OUT_3	AM9
AE39	VDD2_7	VCCSTG_OUT_4	AG10
AF40	VDD2_8		
AG39	VDD2_9	VCCIO_OUT	V15
AH40	VDD2_10		
AJ39	VDD2_11	VCCSTG_OUT_LGC	M9
AK40	VDD2_12		
AK51	VDD2_13	VCCST_1	BT2
AK52	VDD2_14	VCCST_2	BT1
AL39	VDD2_15	VCCST_3	BT4
AM40	VDD2_16		
AN39	VDD2_17	VCCSTG_3	BP2
AP40	VDD2_18	VCCSTG_4	BP1
AR39	VDD2_19	VCCSTG_5	BP4
AT52	VDD2_20		
AU40	VDD2_21		
AW40	VDD2_22		
AW51	VDD2_23		
AW52	VDD2_24		
BD51	VDD2_25		
BD52	VDD2_26		
BK51	VDD2_27		
BK52	VDD2_28		
BV51	VDD2_29		
BV52	VDD2_30		
CA40	VDD2_31		
CC40	VDD2_32		
CC49	VDD2_33		
CC50	VDD2_34		
CE40	VDD2_35		
CG40	VDD2_36		
CH39	VDD2_37		
CJ40	VDD2_38		
CL40	VDD2_39		
CN40	VDD2_40		
CP47	VDD2_41		
CR40	VDD2_42		
D50	VDD2_43		
E51	VDD2_44		
F49	VDD2_45		
T51	VDD2_46		
T52	VDD2_47		

8 x 10uF 0402 - 10V on backside

C23 C24 C25 C26 C27
C33 C34 C35
10uF RC0402

8 x 1uF 0402 - 6.3V on top side

C43 C44 C45 C46 C47
C50 C51 C52
0402 1uF

2 x 47uF 0603 on top side

C491 C492
47uF 0603

Place them as close to the VR as possible.
2 caps should be stuffed.

Not connected to anyting, C212 for decoupling.

+VCCSTG_OUT_1

NOP TP11

TL-EDS: p.150 (Processor Pull-up Power Rails Signals)

NOP C212 1uF,16V,X5R/X7R

+VCCIO_OUT

+VCCIO_OUT Reference power rail for all Debug/Config Signals Pull-up on platform.

+VCCSTG_TERM

+VCCSTG_TERM: ReferenCe power rail for all Legacy Signals Pull-up on platform

+VCCST_CPU

Sustain Voltages for processor standby modes.

VCCST, and VCCSTG can remain powered during S0ix and S3 states for power and latency optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for

+VCCST_CPU

+VCCSTG_CPU (RMVD)

C39 C40 C41 C42
1uF

Here we made: +VCCST_CPU = +VCCSTG_CPU

+VCCST_CPU is generated from +VCC1P05_OUT_FET which is genreated from CPU_FIVR

Sustain Voltages for processor standby modes.

PLACE AS CLOSE AS POSSIBLE TO THE BGA PINS. POWER ROUTING ON THE BOARD NEED TO BE ATLEAST ON >2 ROUTE LAYERS, PREFERABLY ON 4 LAYERS. FOLLOW GUIDELINES SHOWN IN BREAKOUT. PMR OF 1MOHM NEED TO BE PLACED IN PARALLEL TO POWERGATE. PG RDSON NEED TO BE <=5MOHM.

+VCCIN

SECONDARY (BOTTOM SIDE CASPS) p.58/270 15x10uF,10V,0402

C425 C426 C427 C461 C463 C464 C465 C466 C467 C468 C469 C470 C471 C472 C473
10uF,10V,0402

Put them as directly below the BGAs as possible.

+VDDQ

SECONDARY (BOTTOM SIDE CASPS) p.59/270 15x1uF,6.3V,0201

C495 C496 C497 C498 C499 C500 C501 C502 C503 C504 C505 C506 C507 C508 C509
1uF,6.3v,0201

Put them as directly below the BGAs as possible.

+VCCIO_OUT

R62
100R,1%,0402
NOP

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VCCIN_AUX, VCCPRIM

From External DC\DC to SoC

U1N

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+VCCIN_AUX

AB12 VCCIN_AUX_1
AC10 VCCIN_AUX_2
AE10 VCCIN_AUX_3
AK2 VCCIN_AUX_4
AR10 VCCIN_AUX_5
AT12 VCCIN_AUX_6
AU10 VCCIN_AUX_7
AW10 VCCIN_AUX_8
BV1 VCCIN_AUX_9
BV39 VCCIN_AUX_10
BW40 VCCIN_AUX_11
BY39 VCCIN_AUX_12
CC1 VCCIN_AUX_13
CD12 VCCIN_AUX_14
CF10 VCCIN_AUX_15
CG12 VCCIN_AUX_16
CH10 VCCIN_AUX_17
CJ1 VCCIN_AUX_18
CJ12 VCCIN_AUX_19
CK10 VCCIN_AUX_20
CL12 VCCIN_AUX_21
CM10 VCCIN_AUX_22
CP1 VCCIN_AUX_23
CP10 VCCIN_AUX_24
CR12 VCCIN_AUX_25
CT10 VCCIN_AUX_26
CU12 VCCIN_AUX_27
CY1 VCCIN_AUX_28
AK1 VCCIN_AUX_29

AV9 VCCIN_AUX_VSSSENSE
AT9 VCCIN_AUX_VCCSENSE

DD17 VCC_VNNEXT_1P05_1
DD18 VCC_VNNEXT_1P05_2

DA15 VCC_V1P05EXT_1P05_1
DA17 VCC_V1P05EXT_1P05_2

DB39 GPP_B2/VRALERT#
DV12 GPP_F22/VNN_CTRL
DT12 GPP_F23/V1P05_CTRL

DB37 GPP_B0/CORE_VID0
DB38 GPP_B1/CORE_VID1

TGL_UP3_IP_EXT/BGA

1.8 V Primary Well.
+VCCPRIM_1P8

CY18 VCCPRIM_1P8_1
CY20 VCCPRIM_1P8_2
CY24 VCCPRIM_1P8_3
CY26 VCCPRIM_1P8_4
DA18 VCCPRIM_1P8_5
DA20 VCCPRIM_1P8_6
DA22 VCCPRIM_1P8_7
DA24 VCCPRIM_1P8_8
DA26 VCCPRIM_1P8_9
DC18 VCCPRIM_1P8_10
DC20 VCCPRIM_1P8_11
DC22 VCCPRIM_1P8_12
DC24 VCCPRIM_1P8_13
DC26 VCCPRIM_1P8_14
DD20 VCCPRIM_1P8_15
DD22 VCCPRIM_1P8_16
DV22 VCCPRIM_1P8_17

+VCCPRIM_3P3
3.3 V Primary Well.
+V3A

DA35 VCCPRIM_3P3_1
DC28 VCCPRIM_3P3_2
DC30 VCCPRIM_3P3_3
DD30 VCCPRIM_3P3_4

DV34 DCPRTC
DV46 VCCLDOSTD_0P85
DV16 VCCA_CLKLDO_1P8_1 INPUT
DC15 VCCA_CLKLDO_1P8_2
DV28 VCCDPHY_1P24 OUTPUT
DD38 VCCDSW_1P05

BR3 VCC1P05_OUT_FET_1
BR4 VCC1P05_OUT_FET_2
BT5 VCC1P05_OUT_FET_3

DA31 VCCPRIM1P05_OUT_PCH_1
DC33 VCCPRIM1P05_OUT_PCH_2
DC31 VCCPRIM1P05_OUT_PCH_3

DC35 VCCRTC
DD37 VCCDSW_3P3
DA28 VCCPGPPR

CY31 VCCPRIM_3P3_5
CY33 VCCPRIM_3P3_6
CV39 VCCPRIM_1P8_18

AP12 RSVD_1

in TL-SBC: +VCCPDSW_3P3 is generated from +V3.3A_DSW (p. 225/270)

+3V3A — R77 0R,5%,0402 NOP — +VCCPGPPR_3P3_1P8

+V1.8A — R6 0R,5%,0402 — +VCCPRIM_1P8

R64 0R,5%,0402 — 0.68uH, 20%, 150mA, 0.8ohm NOP L10 — +VCCA_CLKLDO_1P8

+VCCPGPPR_3P3_1P8 — R78 0R,5%,0402

The inductor and capacitor form an LC filter to filter out the switching noise either from the power supply itself or from the other components connected to the power supply. The resistor dampens the LC filter to prevent unwanted resonance. LC filters like this often use a high ESR tantalum capacitor instead of adding a separate resistor.

LC Filter: LOW PASS

R66 0R,5%,0402

RC_CLKLDO

C211 47uF,6.3V,X5R

R66: Option 1: stuff with 0 ohm if the inductor is not stuffed. Option 2: stuff 100 mohm if the inductor stuffed

TP52 TP51 TP50 TP49

VRALERT_MCP# — 0R — R74 — VRALERT_MCP#_C

VCCIN_AUX_CORE_VID0_R — 0R — R75 — GPPC_B0_CORE_VID_0
VCCIN_AUX_CORE_VID1_R — 0R — R76 — GPPC_B1_CORE_VID_1

VRALERT#: ICC Max. throttling indicator from the PCH voltage regulators. VRALERT# pin allows the VR to force PCH throttling to prevent an over current shutdown. PMC based on the VRALERT# and messages from the processor. The messages from the processor allows the processor to constrain the PCH to a particular power budget.

RTC de-coupling capacitor only. This rail should not be driven by any motherboard power rails.

+VCCRTCEXT

+VCCLDOSTD_OUT_0P85 — This rail is generated internally and needs to be routed out to the motherboard for decoupling purposes. Not Connected to any target except decoupling capacitor: C105

+VCCA_CLKLDO_1P8 — 1.24 V for CNVi logic. This rail is generated internally with an LDO and needs to be routed to the motherboard for decoupling purpose only. This rail should not be driven by any motherboard power rails. Not Connected to any target except decoupling capacitor: C107

+VCCDPHY_1P24_SOC

+VCCDSW_1P05_SOC — Deep Sx Well: 1.05 V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Not Connected to any target except decoupling capacitor: C104

+VCC1P05_OUT_FET

+VCC1P05_OUT_PCH — 1.05 V Primary Well: for CNVi and other internal I/O blocks. (Make small plane not connected to anything except these 3 balls)

+VCCPRTC_3P3

merge pins together

Deep Sx Well +3V3A

+VCCPGPPR_3P3_1P8: Audio Power 3.3 V or 1.8 V. If powered at 3.3 V, the 3.3 V supply can come from the VCCPRIM_3P3 supply. If powered at 1.8 V, the 1.8 V supply can come from the VCCPRIM_1P8 supply.

+VCCPRIM_3P3 3.3 V Primary Well. +3V3A

p234/270 TL-SBC

3.3-V supply for Deep Sx wells. (input)

PCH I/O and Misc 3.3V Rail(Primary Well)

1.8 V Primary Well. +VCCPRIM_1P8

PCH I/O and Misc 1.8V Rail(Primary Well)

+VCCIN_AUX — 15 x 10uF 0402 on topside

C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 — 0402 10uF/10V

+VCCIN_AUX — 10 x 10uF 0402 on bottom — Done

C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82 — 0402 10uF/10V

+VCCIN_AUX 12 x 22uF 0603 on topside

C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 — 22uF RC0603

+VCCIN_AUX — 3 x 47uF 0805 on topside

C510 C511 C512 — 0805 47uF ,6.3V

Use 2.5V rating caps.
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth, or 600kHz switching frequency assuming BW= ¼ of Fsw.
Place board caps as close as possible to package in this order where 0402 to be the closest to package pins:
VR ?7343? 0805? 0603-> 0402 ? package.
*a DCLL of 3.3mohm is required and bulk capacitors must be used.

Pair board caps with power/ground PTHs.
Align caps along current flow path from VR to package pins.

Use 2.5V rating caps.
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth, or 600kHz switching frequency assuming BW= ¼ of Fsw.

Place board caps as close as possible to package

VCCA_CLKLDO_1P8 is supplying to PCH ClockK. (analog supply)

+VCCPRTC_3P3 — C95 1uF — C96 100nF

+VCCPDSW_3P3 +3V3A — C97 NOP 1uF,16V,X5R/X7R

+VCCPRIM_3P3 +3V3A — NOP C98 1uF — NOP C99 100nF

+VCCPRIM_1P8 — NOP C100 1uF

NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA

+VCCDSW_1P05_SOC — TP13 — C104 1uF,6.3V,X5R/X7R

+VCCLDOSTD_OUT_0P85 — TP14 — C105 2.2uF,10V,X5R

+VCCRTCEXT — TP12 — C106 100nF,25V,X5R/X7R

+VCCDPHY_1P24_SOC — C107 4.7uF,10V,20%

Table 214. Differences between Power Maps

Volume	Premium
VccSTG gated by SLP_S3#	VccSTG gated by {CPU_C10_GATE#}
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC _V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load
Various system devices share load switches	Various system devices have their own independent load switches

Note:

1. VCC_VNNEXT_1P05 is also known as VNN BYP
2. VCC _V1P05EXT_1P05 is also known as VP105 BYP
3. Other changes may be present. Refer to the Power Map for details.

The VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two optional dedicated voltage regulators that save platform power during low power states.

Trade-offs - Volume vs. Premium Power Maps:

Power maps are broken into two tiers: Volume and Premium. Volume focuses on cost savings with the fewest VRs and Premium focuses on the smallest solution size with the lowest power consumption. For a design focused on S0ix or Modern Standby* power, the Premium power map is recommended. The designer may choose to implement a hybrid between Volume and Premium as long as guidelines are followed.

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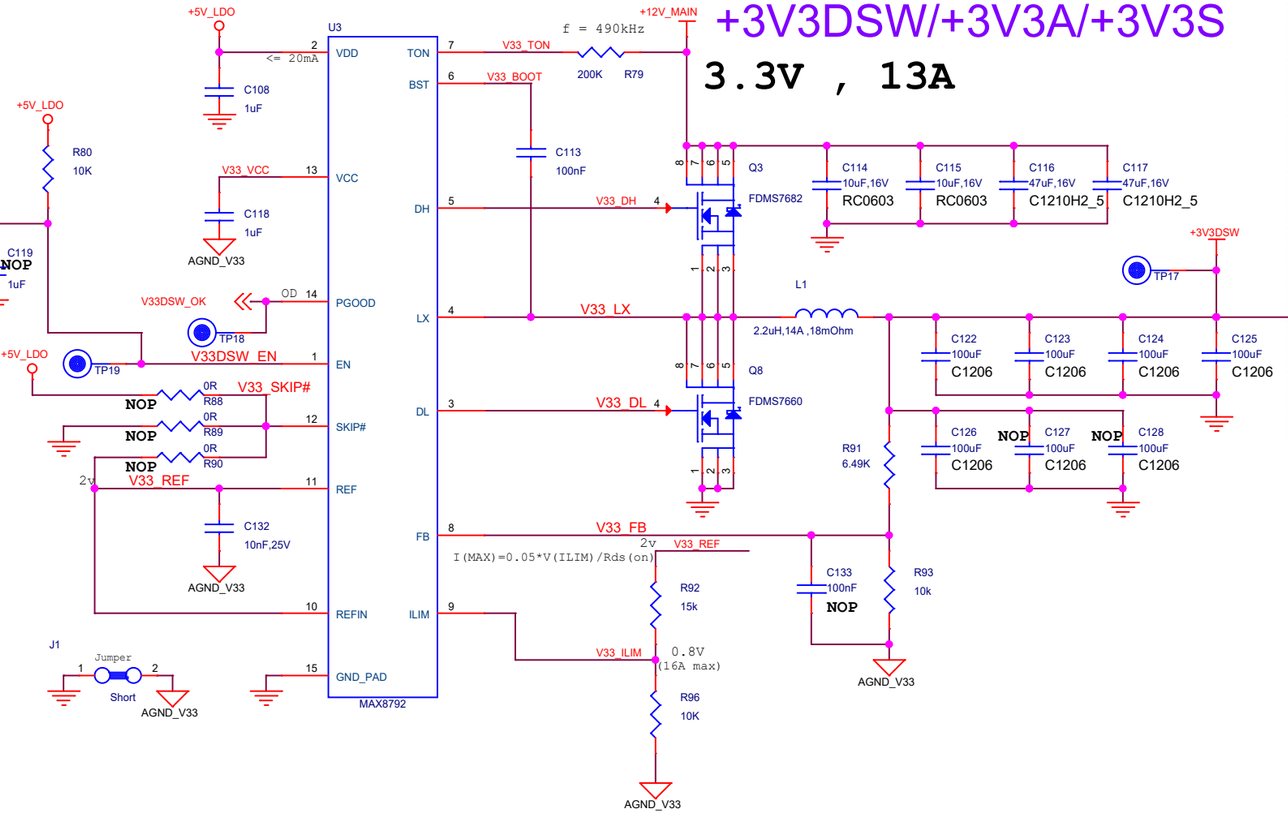
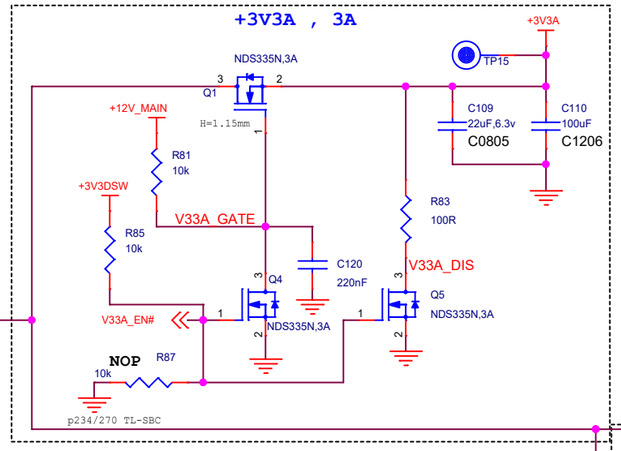
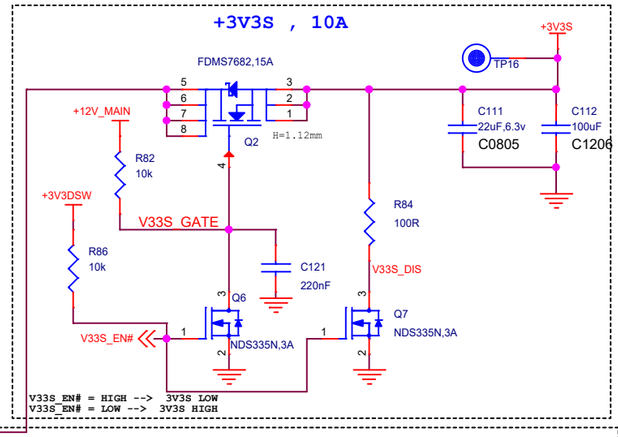
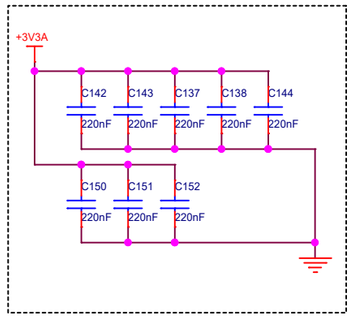
+3V3DSW/+3V3A/+3V3S

3.3V , 13A

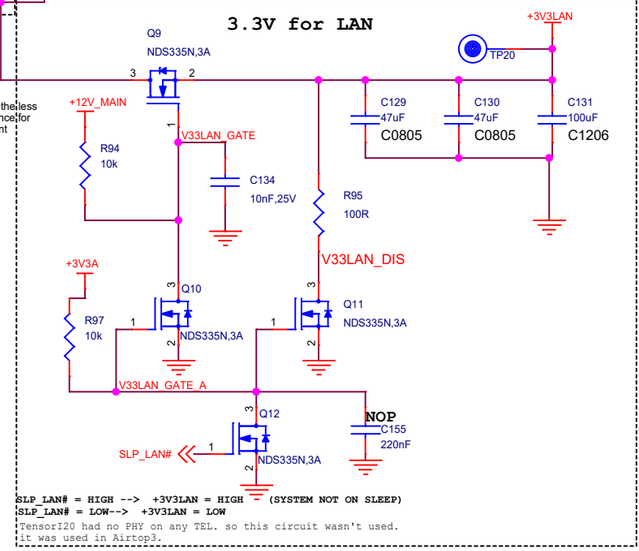


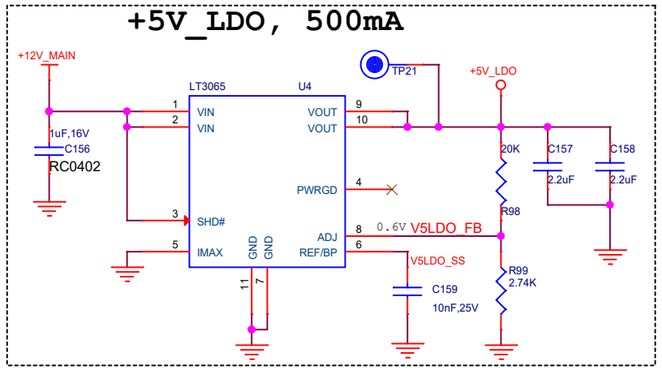






the larger VGS the less Rds(on) Reistance for the same current





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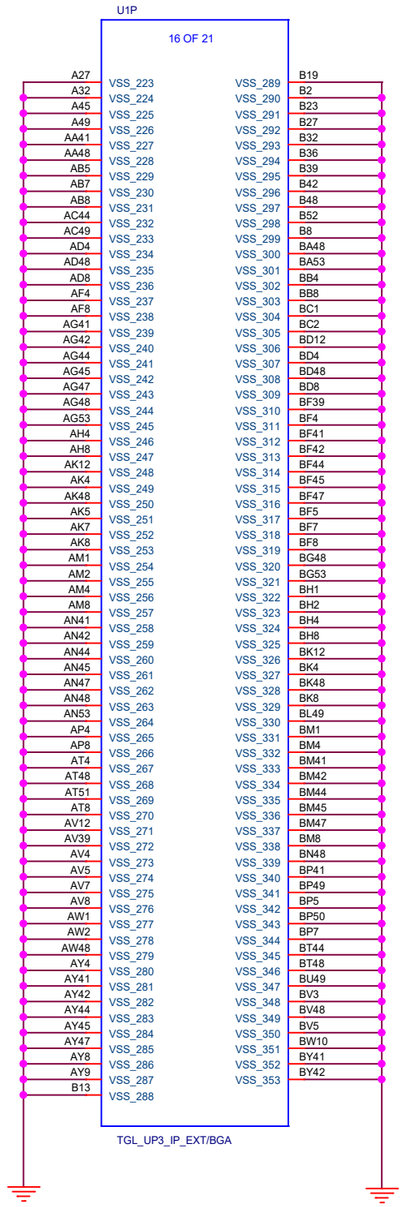

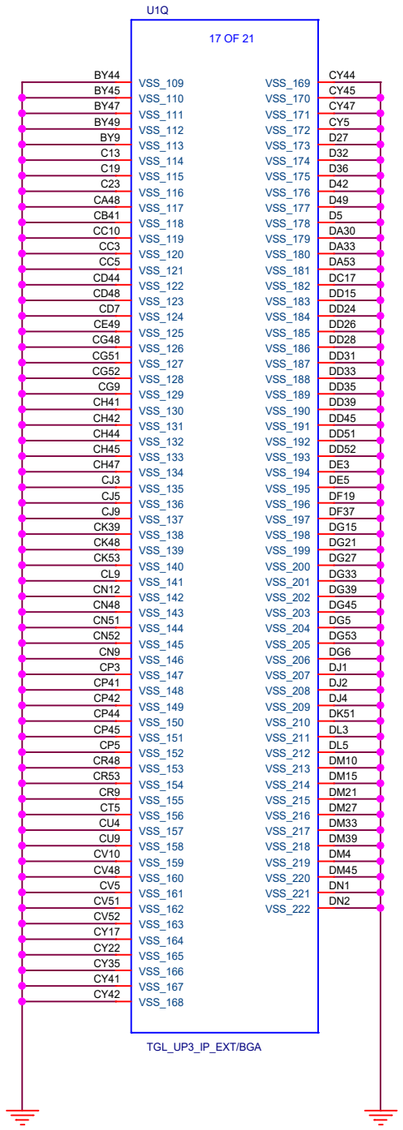

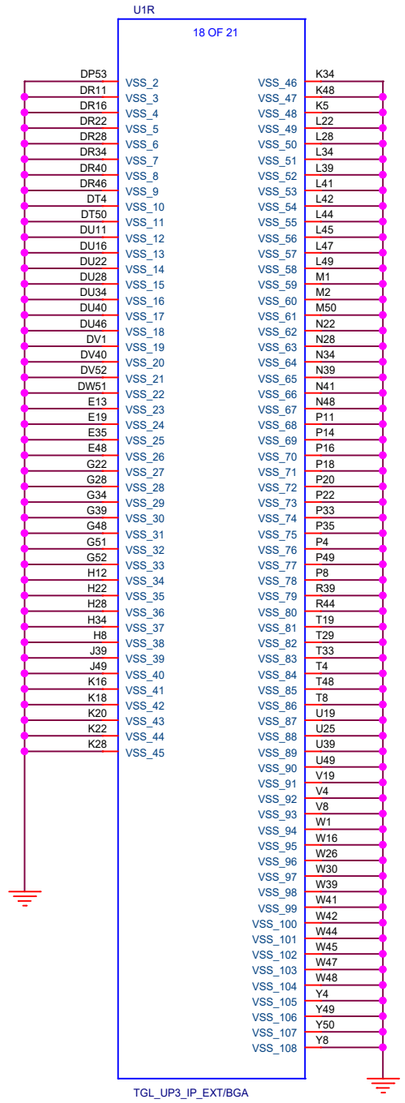

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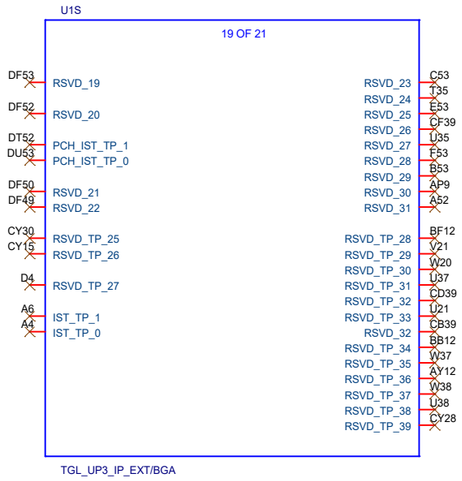

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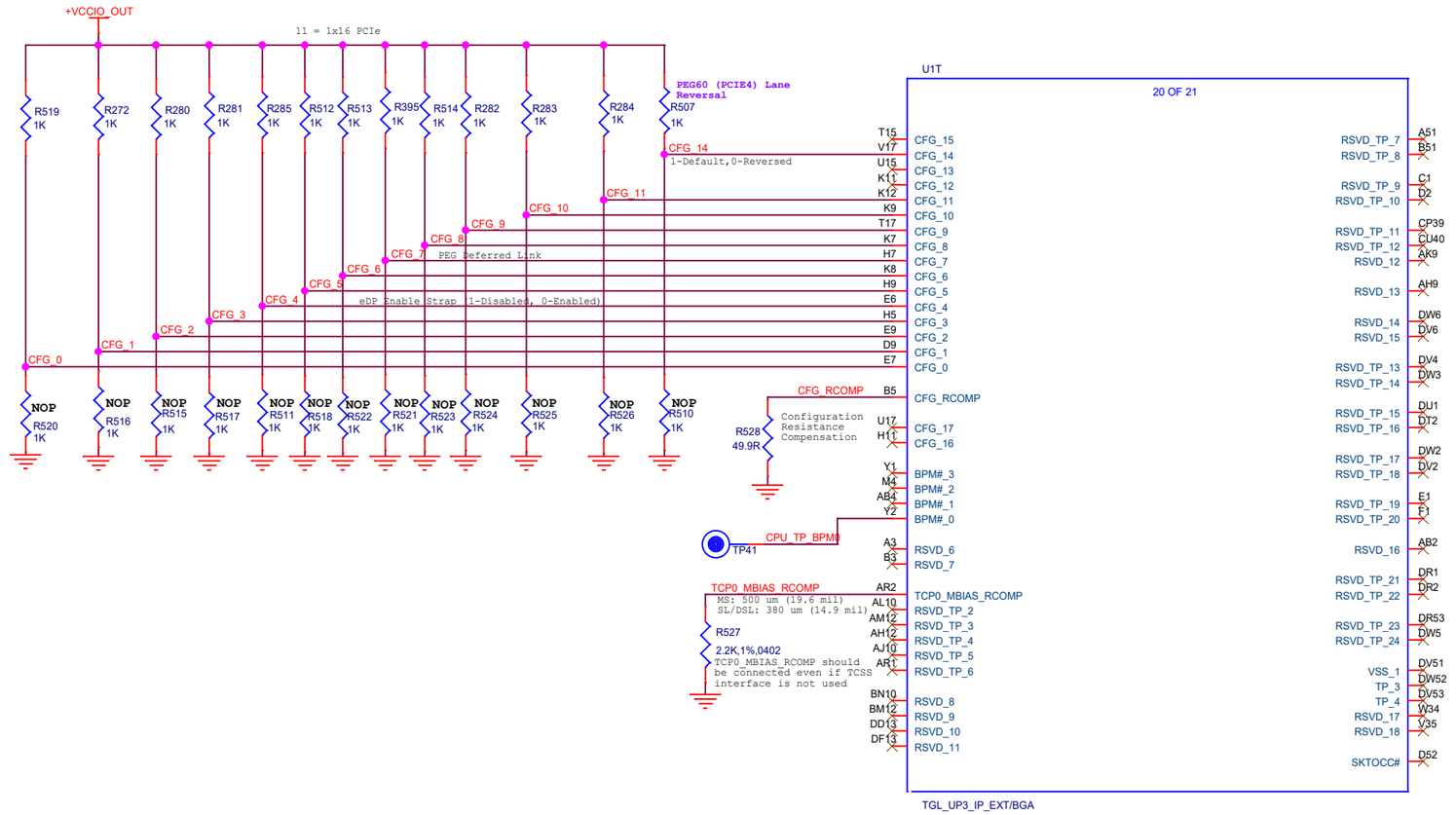
CFG[17:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[3], CFG[0]**: Reserved configuration lane. • **CFG[2]: TGL UP4/UP3** Reserved • **CFG[2]: H** PCI Express* Static x16 Lanes Numbering Reversal. — 1 - (Default) Normal — 0 - Reversed • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]: TGL UP4/UP3** Reserved • **CFG[6:5]: H** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[13:7]:** Reserved configuration lanes. • **CFG[14]**: PEG60 (PCIE4) Lane Reversal: — 1 - (Default) Normal — 0 - Reversed • **CFG[17:15]:** Reserved configuration lanes.	I	GTL	SE	UP3/UP4/H Processor Lines



BPM#[3:0]
Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM#[3:0]	Pull Up/Pull Down	VCC_{IO}_OUT	16-60 Ω
PROC_PREQ#	Pull Up	VCC_{STG}	3 KΩ
PROC_TDI	Pull Up	VCC_{STG}	3 KΩ
PROC_TMS	Pull Up	VCC_{STG}	3 KΩ
PROC_TRST#	Pull Down	VCC_{STG}	3 KΩ
PROC_TCK	Pull Down	VCC_{STG}	3 KΩ
CFG[17:0]	Pull Up	VCC_{IO}_OUT	3 KΩ

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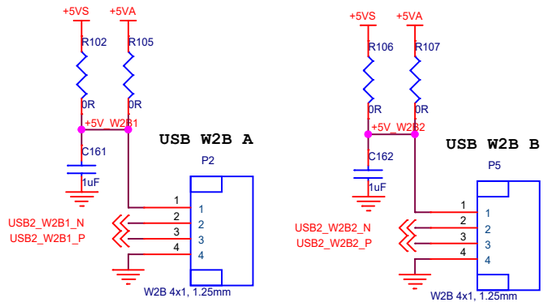
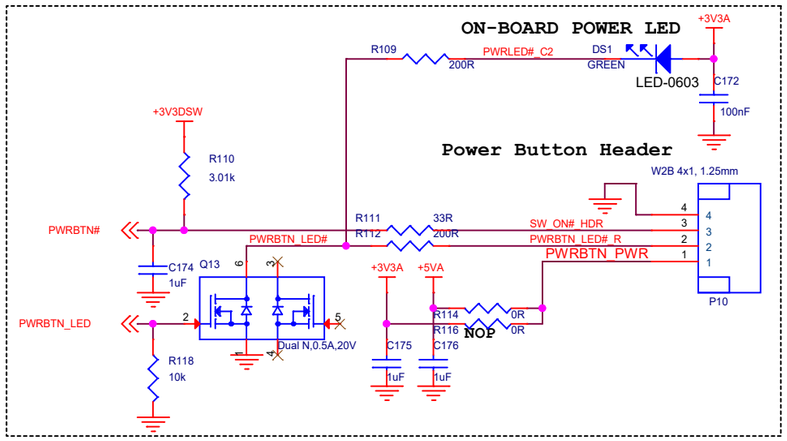
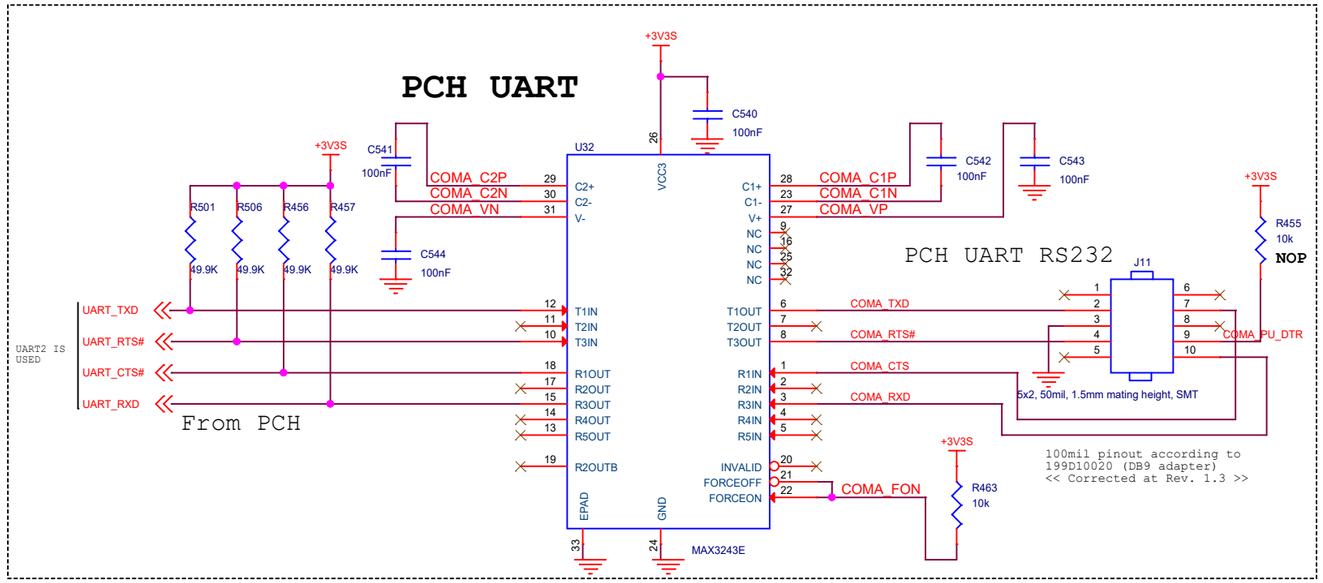
Headers



audio **Extension headers**

Note: The Intel® Ethernet Connection I219 can be connected to one of the following PCI Express* ports 7, 8 or, 9



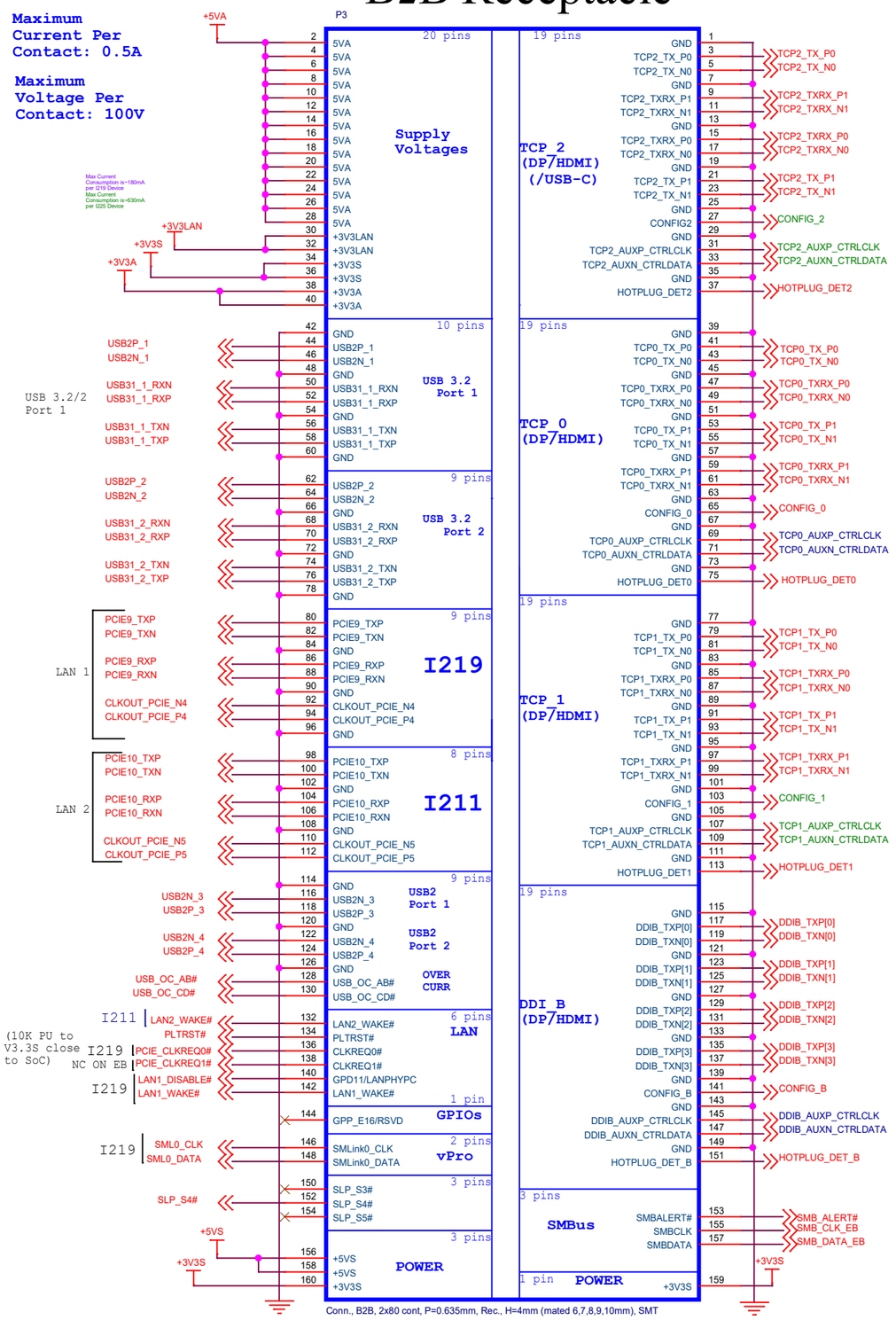


182K16001S

B2B Receptacle

Maximum Current Per Contact: 0.5A

Maximum Voltage Per Contact: 100V



see TL-PDG p 104/506 table 49: DDI port signal mapping to the HDMI connector.

mini DP ++ 2

for this Face Module. this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they belong to HDMI.

HDMI PORT 2

for this Face Module. this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in EB-TI22A Connector.

mini DP++ 1

see TL-PDG p 103/506 table 48: DDI: TCP Port Signal Mapping for HDMI connector.

for this Face Module. this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they belong to HDMI.

HDMI PORT 1

for this Face Module. this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in EB-TI22A Connector.

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p.143/187 TL-EDS

12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] **TX** DDIB_TXN[3:0]	**Digital Display Interface Transmit:** DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P **AUX** DDIB_AUX_N	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

p.103/507 TL-TDG

Table 38. DisplayPort* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx) **TX**	DDIx_TXP/N[3:0]	N/A	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	N/A	2
Aux Channel **AUX**	DDIx_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

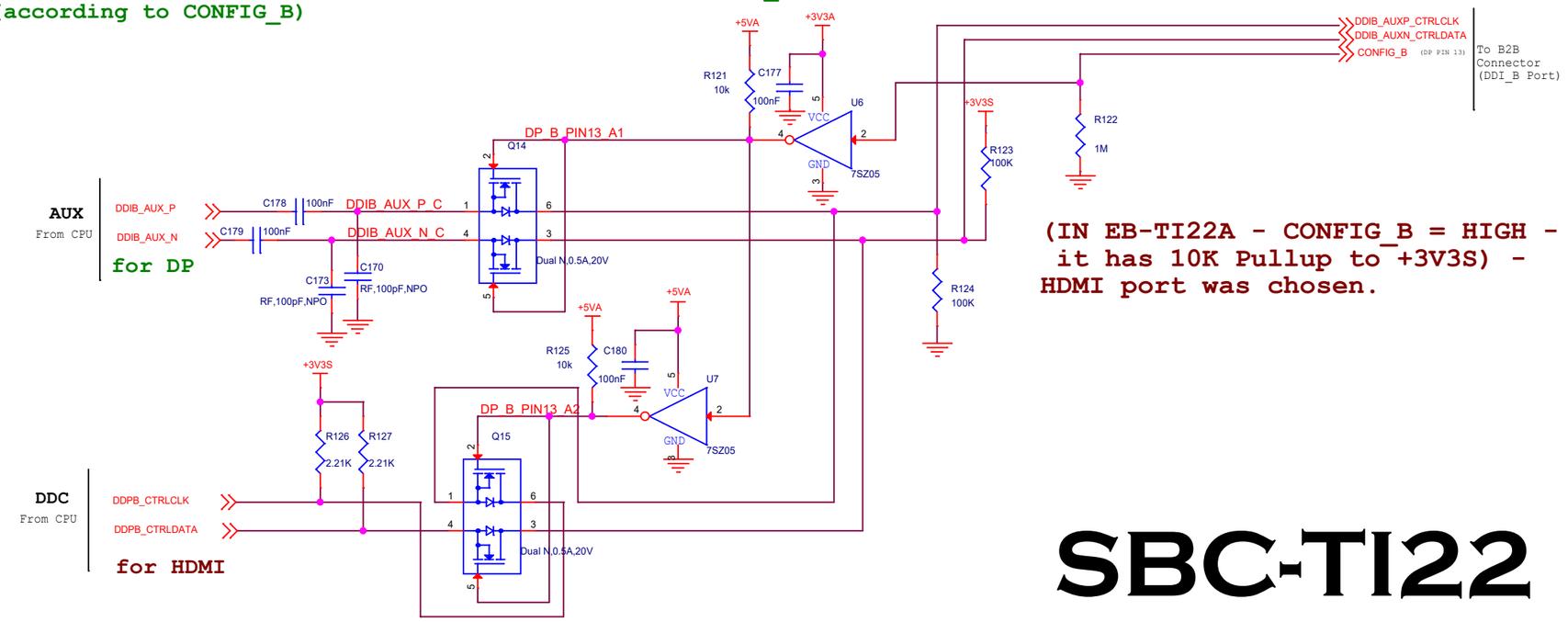
p.103/507 TL-TDG

Table 47. HDMI* Signals

Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx) **TX**	DDIx_TXP/N[3:0]	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	2
DDC **DDC**	N/A	DDPx_CTRLCLK and DDPx_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

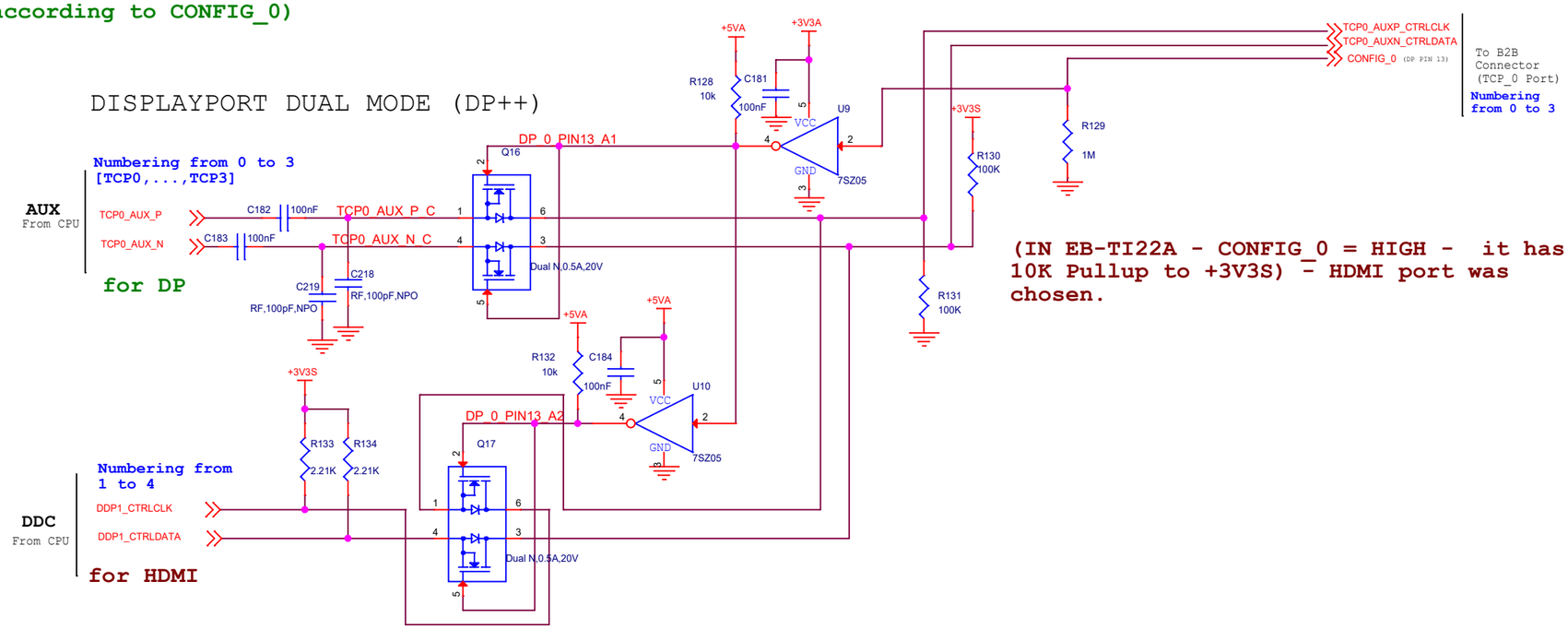
Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

DP(AUXP, AUXN) or HDMI(CTRLCLK, CTRLDATA) select for DDI_B (according to CONFIG_B)



SBC-TI22

DP(AUXP, AUXN) or HDMI(CTRLCLK, CTRLDATA) select for TCP0 (according to CONFIG_0)



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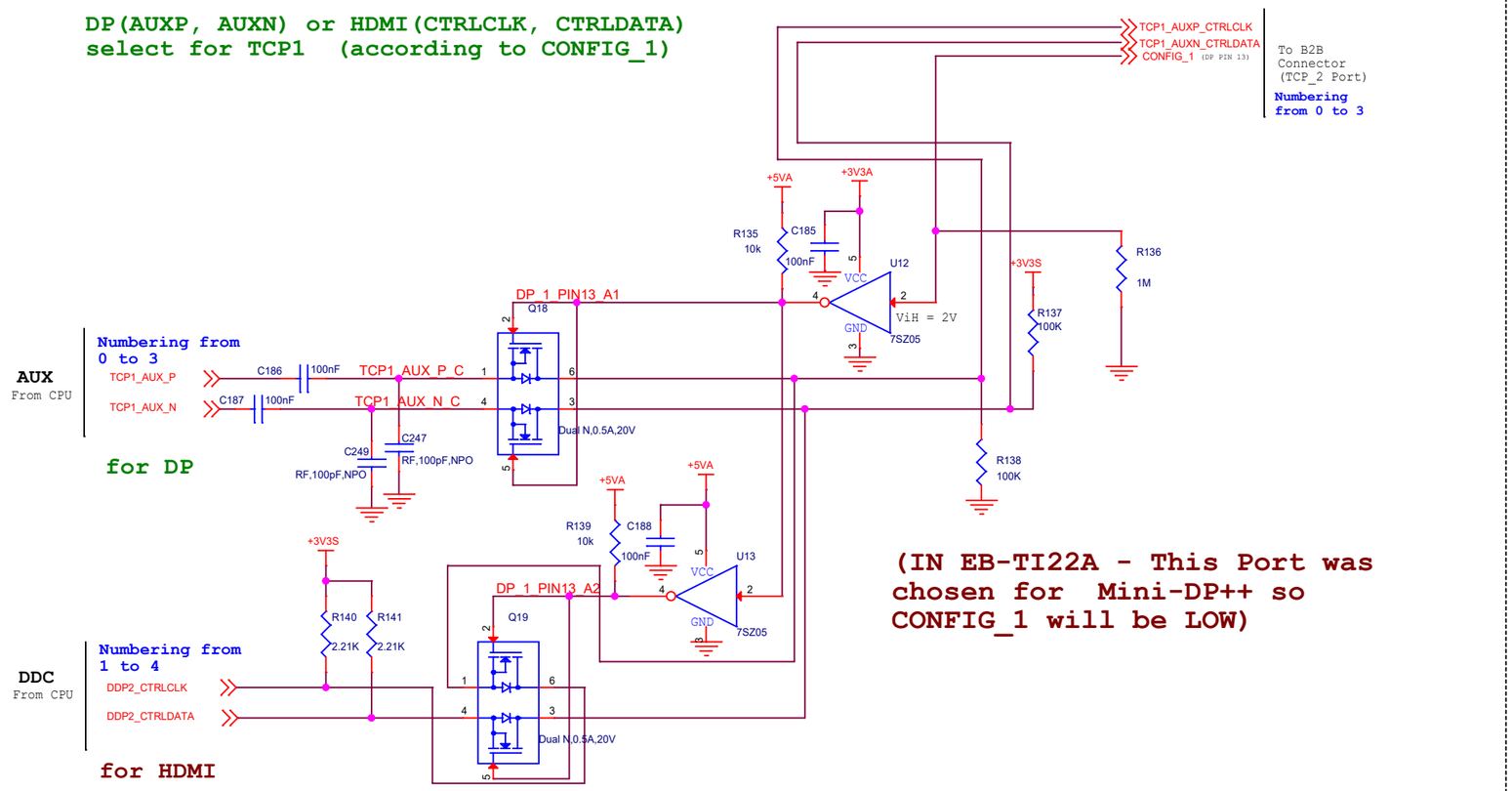

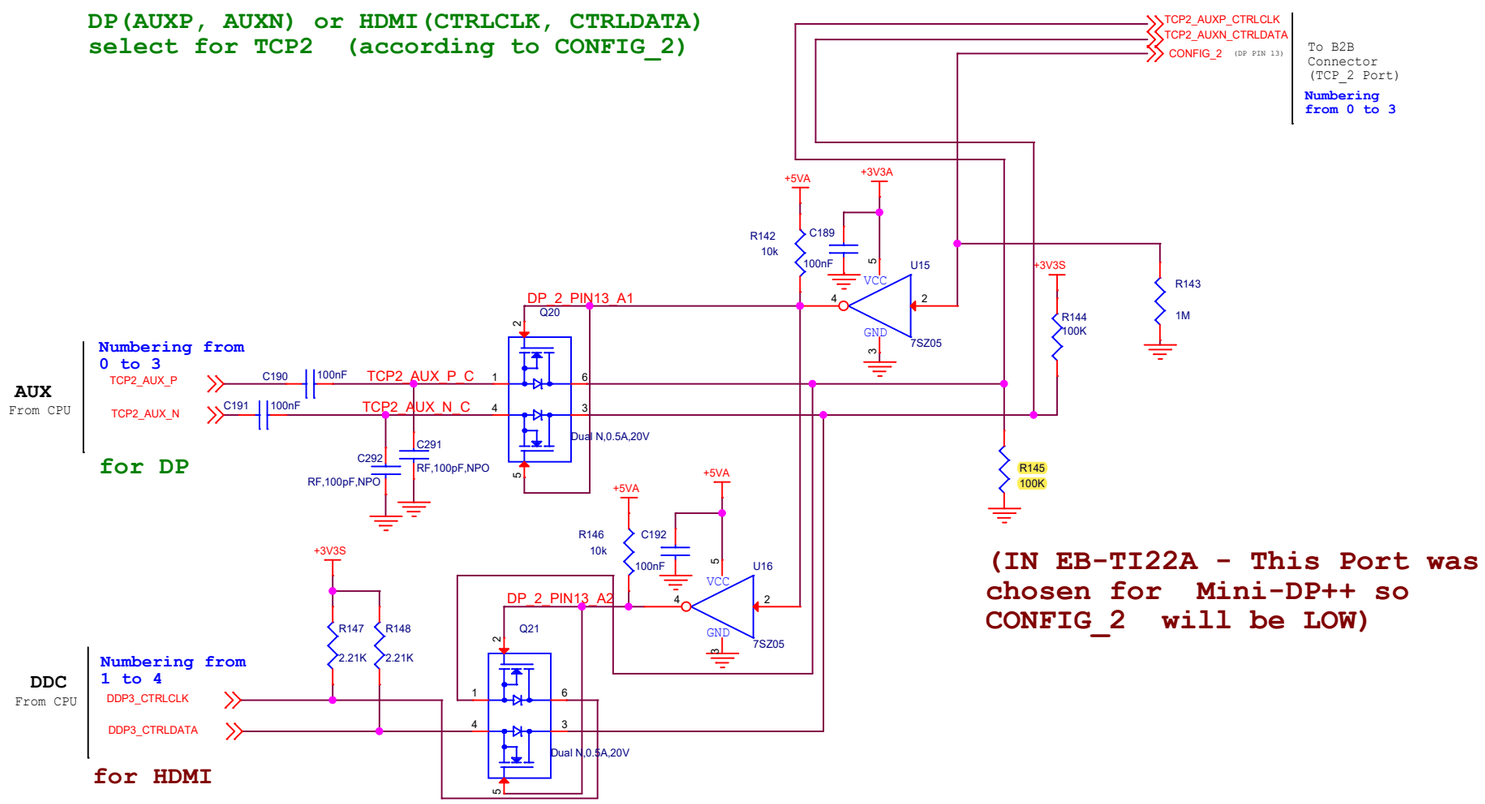

12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] DDIB_TXN[3:0] TX	**Digital Display Interface Transmit:** DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P DDIB_AUX_N AUX	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

Table 38. DisplayPort* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx) TX	DDIx_TXP/N[3:0]	N/A	N/A	1
	TCPx_TX_P/N[1:0] and TCPx_TXRX_P/N[1:0]	N/A	N/A	2
Aux Channel AUX	DDIx_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

Table 47. HDMI* Signals

Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx) TX	DDIx_TXP/N[3:0]	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	2
DDC DDC	N/A	DDPx_CTRLCLK and DDPx_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

Note:
1. Signal names apply for DDI A/B ports.
2. Signal names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

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C:\Users\firas.abdelghani\Dropbox\Board-Design\Design Techniques\DDR4\ACPI DDR4 SO-DIMM 32GB CMA6-5IH01BAR01M00.pdf

Question: how to know what is the address of each SPD in each channel?
how to set which DDR4 is CH0 and which is CH1?

DDR4 SODIMM CH A

Small Outline Dual In-line Memory Module

+VDDQ (+VDD2_MEM / +VDD2_CPU)

DIMM ECC check bits
(No Connection to MCP)

CON
INS5624688
J2C1A

M_0_MA16_RAS_N 152 A16/RAS_N
M_0_MA15_CAS_N 156 A15/CAS_N
M_0_MA14_WE_N 151 A14/WE_N
M_0_MA13 158 A13
M_0_MA12 119 A12
M_0_MA11 120 A11
M_0_MA10 146 A10/AP
M_0_MA9 121 A9
M_0_MA8 125 A8
M_0_MA7 122 A7
M_0_MA6 127 A6
M_0_MA5 126 A5
M_0_MA4 128 A4
M_0_MA3 131 A3
M_0_MA2 132 A2
M_0_MA1 133 A1
M_0_MA0 144 A0

M_0_BA1 145 BA1
M_0_BA0 150 BA0
M_0_BG1 113 BG1
M_0_BG0 115 BG0

RANK 1
M_0_CLK_DDR1_DP 138 CK1P
M_0_CLK_DDR1_DN 140 CK1N
RANK 0
M_0_CLK_DDR0_DP 137 CK0P
M_0_CLK_DDR0_DN 139 CK0N

M_0_CS1_N 157 CS1_N
M_0_CS0_N 149 CS0_N

M_0_CKE_1 110 CKE1
M_0_CKE_0 109 CKE0

M_0_ODT1 161 ODT1
M_0_ODT0 155 ODT0

165 C1/CS3_N/NC
162 C0/CS2_N/NC

M_0_CB7 104 CB7/NC
M_0_CB6 100 CB6/NC
M_0_CB5 87 CB5/NC
M_0_CB4 88 CB4/NC
M_0_CB3 105 CB3/NC
M_0_CB2 101 CB2/NC
M_0_CB1 91 CB1/NC
M_0_CB0 92 CB0/NC

M_0_PARITY 143 PARITY
108 RESET_N

DIMM0_TS_EVENT_N 134 EVENT_N
M_0_ALERT_N 116 ALERT_N
M_0_ACT_N 255 ACT_N
VDDSPD

166 SA2
260 SA1
256 SA0

SMB_DATA_S_R 254 SDA
SMB_CLK_S_R 253 SCL
164 VREFCA

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1 OF 4
K85756-001

M_0_DQ_2<0> 246 DQ63
M_0_DQ_2<6> 245 DQ62
M_0_DQ_2<3> 233 DQ61
M_0_DQ_2<5> 232 DQ60
M_0_DQ_2<2> 250 DQ59
M_0_DQ_2<4> 249 DQ58
M_0_DQ_2<7> 236 DQ57
M_0_DQ_2<1> 237 DQ56
M_0_DQ_3<4> 225 DQ55
M_0_DQ_3<1> 224 DQ54
M_0_DQ_3<5> 212 DQ53
M_0_DQ_3<3> 211 DQ52
M_0_DQ_3<6> 229 DQ51
M_0_DQ_3<2> 228 DQ50
M_0_DQ_3<0> 215 DQ49
M_0_DQ_3<7> 216 DQ48
M_0_DQ_0<1> 204 DQ47
M_0_DQ_0<3> 203 DQ46
M_0_DQ_0<4> 190 DQ45
M_0_DQ_0<6> 191 DQ44
M_0_DQ_0<2> 208 DQ43
M_0_DQ_0<0> 207 DQ42
M_0_DQ_0<7> 194 DQ41
M_0_DQ_0<5> 195 DQ40
M_0_DQ_1<5> 182 DQ39
M_0_DQ_1<7> 183 DQ38
M_0_DQ_1<1> 169 DQ37
M_0_DQ_1<4> 170 DQ36
M_0_DQ_1<0> 186 DQ35
M_0_DQ_1<6> 187 DQ34
M_0_DQ_1<2> 173 DQ33
M_0_DQ_1<3> 174 DQ32
M_0_DQ_4<0> 80 DQ31
M_0_DQ_4<2> 79 DQ30
M_0_DQ_4<5> 67 DQ29
M_0_DQ_4<7> 66 DQ28
M_0_DQ_4<3> 84 DQ27
M_0_DQ_4<1> 83 DQ26
M_0_DQ_4<6> 71 DQ25
M_0_DQ_4<4> 70 DQ24
M_0_DQ_5<3> 59 DQ23
M_0_DQ_5<2> 58 DQ22
M_0_DQ_5<6> 45 DQ21
M_0_DQ_5<4> 46 DQ20
M_0_DQ_5<0> 63 DQ19
M_0_DQ_5<1> 62 DQ18
M_0_DQ_5<7> 49 DQ17
M_0_DQ_5<5> 50 DQ16
M_0_DQ_6<2> 37 DQ15
M_0_DQ_6<7> 38 DQ14
M_0_DQ_6<4> 25 DQ13
M_0_DQ_6<0> 24 DQ12
M_0_DQ_6<6> 42 DQ11
M_0_DQ_6<1> 41 DQ10
M_0_DQ_6<5> 29 DQ9
M_0_DQ_6<3> 28 DQ8
M_0_DQ_7<1> 17 DQ7
M_0_DQ_7<5> 16 DQ6
M_0_DQ_7<6> 3 DQ5
M_0_DQ_7<4> 4 DQ4
M_0_DQ_7<3> 21 DQ3
M_0_DQ_7<0> 20 DQ2
M_0_DQ_7<2> 7 DQ1
M_0_DQ_7<7> 8 DQ0

NOP R152 240R/1% M_0_CB7
NOP R153 240R/1% M_0_CB6
NOP R154 240R/1% M_0_CB5
NOP R155 240R/1% M_0_CB4
NOP R156 240R/1% M_0_CB3
NOP R157 240R/1% M_0_CB2
NOP R158 240R/1% M_0_CB1
NOP R159 240R/1% M_0_CB0

+3V3S
NOP R161 0R
NOP R162 0R
NOP R163 0R
10k R164
10k R165
10k R166
0 0 0

DRAM_RESET_N_R
+3V3S
Place close to DIMM
C209 100nF 25V
C210 2.2uF 10V
240R/1% R160 DIMM0_TS_EVENT_N

SA2_DIMM0
SA1_DIMM0
SA0_DIMM0
1010000 = 0x50 (7 bit notation)
10100000 = 0xA0 (8 bit notation)
SPD ADDRESS: A0/A1 (0x50)

the outside resistors feed value of 000 (0x00) to the 3 pins - so the SPD connected there will respond at address 0x52 (0x50 + 0x00), shifted left 1 bit and the Read/Write bit added on - so 0xA0 or 0xA1

0x50 (Hex) = 01010000
0x50 = 01010000 -> shift left -> 10100000 = 0xA0

+VDDQ
R167 1K
C220 100nF
R168 2.2R
+V_D4CH0_CA_VREF
+VREF_CH0_CA
C221 22nF
R169 1K
VREFCA_RC_SODDIMA
R170 24.9R

CON
J2C1B
INS5623944

DQS8P 97 M_0_DQS_DP<8>
DQS8N 95 M_0_DQS_DN<8>
R149 240R/1%
R150 240R/1%
+VDDQ

DQS7P 242 M_0_DQS_2_DP
DQS7N 240 M_0_DQS_2_DN
DQS6P 221 M_0_DQS_3_DP
DQS6N 219 M_0_DQS_3_DN
DQS5P 200 M_0_DQS_0_DP
DQS5N 198 M_0_DQS_0_DN
DQS4P 179 M_0_DQS_1_DP
DQS4N 177 M_0_DQS_1_DN
DQS3P 76 M_0_DQS_4_DP
DQS3N 74 M_0_DQS_4_DN
DQS2P 55 M_0_DQS_5_DP
DQS2N 53 M_0_DQS_5_DN
DQS1P 34 M_0_DQS_6_DP
DQS1N 32 M_0_DQS_6_DN
DQS0P 13 M_0_DQS_7_DP
DQS0N 11 M_0_DQS_7_DN

+VDDQ
R151 240R/1%

DM8_N/DBI8_N/NC 96 M_0_DM8
DM7_N/DBI7_N/NC 241
DM6_N/DBI6_N/NC 220
DM5_N/DBI5_N/NC 199
DM4_N/DBI4_N/NC 178
DM3_N/DBI3_N/NC 75
DM2_N/DBI2_N/NC 54
DM1_N/DBI1_N/NC 33
DM0_N/DBI0_N/NC 12

CON
K85569-001 2 OF 4
J2C1C
INS5624490

VDD 112
VDD 111
VDD 163
VDD 160
VDD 159
VDD 154
VDD 153
VDD 148
VDD 147
VDD 142
VDD 141
VDD 136
VDD 135
VDD 130
VDD 129
VDD 124
VDD 123
VDD 118
VDD 117

VPP 259
VPP 257
VTT 258

+VDDQ
8 x 1uF 0402
C193 0402 1uF
C194 0402 1uF
C195 0402 1uF
C196 0402 1uF
SODIMM UPPER SIDE

C197 0402 1uF
C198 0402 1uF
C199 0402 1uF
C201 0402 1uF
SODIMM DOWN SIDE

8 x 10uF 0402
C202 0602 10uF 6.3v
C200 0602 10uF 6.3v
C203 0602 10uF 6.3v
C204 0602 10uF 6.3v
SODIMM UPPER SIDE

C205 0602 10uF 6.3v
C206 0602 10uF 6.3v
C207 0602 10uF 6.3v
C208 0602 10uF 6.3v
SODIMM DOWN SIDE

4 caps near each side of DIMM connector close to VDD pins

+VPP
C213 0402 1uF
C214 10uF ,6.3V,0603

+VTT
C215 0402 1uF
C216 0402 1uF
C217 10uF ,6.3V,0603

3/4
3 OF 4
K85756-001

PLACE C217 ON VTT PLANE CLOSE TO DIMM

CON
J2C1D
INS5625532

252 VSS
251 VSS
248 VSS
247 VSS
244 VSS
243 VSS
239 VSS
238 VSS
235 VSS
234 VSS
231 VSS
230 VSS
227 VSS
226 VSS
223 VSS
222 VSS
218 VSS
217 VSS
214 VSS
213 VSS
210 VSS
209 VSS
206 VSS
205 VSS
202 VSS
201 VSS
197 VSS
196 VSS
193 VSS
192 VSS
189 VSS
188 VSS
185 VSS
184 VSS
181 VSS
180 VSS
176 VSS
175 VSS
172 VSS
171 VSS
168 VSS
167 VSS
107 VSS
106 VSS
103 VSS
102 VSS
99 VSS
262 MP2

98 VSS
94 VSS
93 VSS
90 VSS
89 VSS
86 VSS
85 VSS
82 VSS
81 VSS
78 VSS
77 VSS
73 VSS
72 VSS
69 VSS
68 VSS
65 VSS
64 VSS
61 VSS
60 VSS
57 VSS
56 VSS
52 VSS
51 VSS
48 VSS
47 VSS
44 VSS
43 VSS
40 VSS
39 VSS
36 VSS
35 VSS
31 VSS
30 VSS
27 VSS
26 VSS
23 VSS
22 VSS
19 VSS
18 VSS
15 VSS
14 VSS
10 VSS
9 VSS
6 VSS
5 VSS
2 VSS
1 VSS
261 MP1

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K85756-001

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DDR4 SODIMM CH B

Memory, DDR4, SODIMM-260, 32GB, 2400MHz/2666MHz, 1.2V
P/N: 111L63202

Pin Location on SODDIMM:
259-13x2=233

CON
J2C2A
INS17150946

M_1_MA16_RAS_N	152	A16/RAS_N	DQ63	246	M_1_DQ_2<6>
M_1_MA15_CAS_N	156	A15/CAS_N	DQ62	245	M_1_DQ_2<2>
M_1_MA14_WE_N	151	A14/WE_N	DQ61	233	M_1_DQ_2<7>
M_1_MA13	158	A13	DQ60	232	M_1_DQ_2<3>
M_1_MA12	119	A12	DQ59	250	M_1_DQ_2<4>
M_1_MA11	120	A11	DQ58	249	M_1_DQ_2<0>
M_1_MA10	146	A10/AP	DQ57	236	M_1_DQ_2<1>
M_1_MA9	121	A9	DQ56	237	M_1_DQ_2<5>
M_1_MA8	125	A8	DQ55	225	M_1_DQ_3<0>
M_1_MA7	122	A7	DQ54	224	M_1_DQ_3<4>
M_1_MA6	127	A6	DQ53	212	M_1_DQ_3<7>
M_1_MA5	126	A5	DQ52	211	M_1_DQ_3<3>
M_1_MA4	128	A4	DQ51	229	M_1_DQ_3<1>
M_1_MA3	131	A3	DQ50	228	M_1_DQ_3<5>
M_1_MA2	132	A2	DQ49	215	M_1_DQ_3<2>
M_1_MA1	133	A1	DQ48	216	M_1_DQ_3<6>
M_1_MA0	144	A0	DQ47	204	M_1_DQ_0<4>
			DQ46	203	M_1_DQ_0<1>
M_1_BA1	145	BA1	DQ45	190	M_1_DQ_0<5>
M_1_BA0	150	BA0	DQ44	191	M_1_DQ_0<0>
M_1_BG1	113	BG1	DQ43	208	M_1_DQ_0<3>
M_1_BG0	115	BG0	DQ42	207	M_1_DQ_0<2>
			DQ41	194	M_1_DQ_0<6>
M_1_CLK_DDR1_DP	138	CK1P	DQ40	195	M_1_DQ_0<7>
M_1_CLK_DDR1_DN	140	CK1N	DQ39	182	M_1_DQ_1<3>
M_1_CLK_DDR0_DP	137	CK0P	DQ38	183	M_1_DQ_1<1>
M_1_CLK_DDR0_DN	139	CK0N	DQ37	169	M_1_DQ_1<5>
			DQ36	170	M_1_DQ_1<7>
M_1_CS1_N	157	CS1_N	DQ35	186	M_1_DQ_1<4>
M_1_CS0_N	149	CS0_N	DQ34	187	M_1_DQ_1<2>
			DQ33	173	M_1_DQ_1<6>
M_1_CKE_1	110	CKE1	DQ32	174	M_1_DQ_1<0>
M_1_CKE_0	109	CKE0	DQ31	80	M_1_DQ_7<0>
			DQ30	79	M_1_DQ_7<7>
M_1_ODT1	161	ODT1	DQ29	67	M_1_DQ_7<5>
M_1_ODT0	155	ODT0	DQ28	66	M_1_DQ_7<3>
			DQ27	84	M_1_DQ_7<1>
	165	C1/CS3_N/NC	DQ26	83	M_1_DQ_7<4>
	162	C0/CS2_N/NC	DQ25	71	M_1_DQ_7<6>
			DQ24	70	M_1_DQ_7<2>
			DQ23	59	M_1_DQ_6<0>
			DQ22	58	M_1_DQ_6<5>
			DQ21	45	M_1_DQ_6<3>
			DQ20	46	M_1_DQ_6<7>
			DQ19	63	M_1_DQ_6<2>
			DQ18	62	M_1_DQ_6<4>
			DQ17	49	M_1_DQ_6<1>
			DQ16	50	M_1_DQ_6<6>
			DQ15	37	M_1_DQ_4<7>
			DQ14	38	M_1_DQ_4<6>
			DQ13	25	M_1_DQ_4<1>
			DQ12	24	M_1_DQ_4<3>
			DQ11	42	M_1_DQ_4<5>
			DQ10	41	M_1_DQ_4<0>
			DQ9	29	M_1_DQ_4<4>
			DQ8	28	M_1_DQ_4<2>
			DQ7	17	M_1_DQ_5<4>
			DQ6	16	M_1_DQ_5<6>
			DQ5	3	M_1_DQ_5<0>
			DQ4	4	M_1_DQ_5<1>
			DQ3	21	M_1_DQ_5<3>
			DQ2	20	M_1_DQ_5<5>
			DQ1	7	M_1_DQ_5<7>
			DQ0	8	M_1_DQ_5<2>

BYTE 7
BYTE 6 & 7 SWAPPED
BYTE 6

M_1_PARITY	143	PARITY
	108	RESET_N
	134	EVENT_N
M_1_ALERT_N	116	ALERT_N
M_1_ACT_N	114	ACT_N
	255	VDDSPD
SA2_DIMM1	166	SA2
SA1_DIMM1	260	SA1
SA0_DIMM1	256	SA0
SMB_DATA_S_R	254	SDA
SMB_CLK_S_R	253	SCL
	164	VREFCA

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1 OF 4
K85756-001

DRAM_RESET_N_R — C230 100nF — NOP

+3V3S — NOP R182 0R — 10k R183 — NOP R185 0R

Place close to DIMM — C239 100nF 25V — C240 2.2uF 10V

10k R186 — NOP R187 0R — 10k R188

0 1 0

SPD ADDRESS: W: 0XA4, R: 0XA5

the outside resistors feed value of 010 (0x02) to the 3 pins - so the SPD connected there will respond at address 0x52 (0x50 + 0x02), shifted left 1 bit and the Read/Write bit added on - so 0xA4 or 0xA5.

0x52 (Hex) = 01010010
0x52 = 01010010 -> shift left -> 10100100 = 0xA4

+VDDQ — R189 1K — C250 100nF

+V_D4CH1_CA_VREF — R190 2.2R — +VREF_CH1_CA

C251 22nF VREFCA_RC_SODDIMB

R192 1K

R194 24.9R

+VDDQ — NOP R174–R181 240R/1% — M_1_CB7 104, M_1_CB6 100, M_1_CB5 87, M_1_CB4 88, M_1_CB3 105, M_1_CB2 101, M_1_CB1 91, M_1_CB0 92 — CB7/NC … CB0/NC

DRAM_RESET_N_R — M_1_PARITY

+3V3S — R184 240R/1% — DIMM1_TS_EVENT_N

SMB_DATA_S_R — R191 0R 0201 — SMB_DATA_S

SMB_CLK_S_R — R193 0R 0201 — SMB_CLK_S

CON
J2C2B
INS17151371

DQS8P	97	M_1_DQS_DP<8>	R171 240R/1%
DQS8N	95	M_1_DQS_DN<8>	R172 240R/1%
DQS7P	242	M_1_DQS_2_DP	
DQS7N	240	M_1_DQS_2_DN	
DQS6P	221	M_1_DQS_3_DP	
DQS6N	219	M_1_DQS_3_DN	
DQS5P	200	M_1_DQS_0_DP	
DQS5N	198	M_1_DQS_0_DN	
DQS4P	179	M_1_DQS_1_DP	
DQS4N	177	M_1_DQS_1_DN	
DQS3P	76	M_1_DQS_7_DP	
DQS3N	74	M_1_DQS_7_DN	SWAPPED
DQS2P	55	M_1_DQS_6_DP	
DQS2N	53	M_1_DQS_6_DN	
DQS1P	34	M_1_DQS_4_DP	
DQS1N	32	M_1_DQS_4_DN	
DQS0P	13	M_1_DQS_5_DP	
DQS0N	11	M_1_DQS_5_DN	

(+VDD2_MEM) +VDDQ — +VDDQ — R173 %1.5K/1%

DM8_N/DBI8_N/NC	96	M_1_DM8
DM7_N/DBI7_N/NC	241	
DM6_N/DBI6_N/NC	220	
DM5_N/DBI5_N/NC	199	
DM4_N/DBI4_N/NC	178	
DM3_N/DBI3_N/NC	75	
DM2_N/DBI2_N/NC	54	
DM1_N/DBI1_N/NC	33	
DM0_N/DBI0_N/NC	12	

+VDDQ — 8 x 1uF 0402 — C222 C223 C224 C225 0402 1uF — SODIMM UPPER SIDE

C226 C227 C228 C229 0402 1uF — SODIMM DOWN SIDE

8 x 10uF 0402 — C232 C231 C233 C234 0602 10uF 6.3v — SODIMM UPPER SIDE

C235 C236 C237 C238 0602 10uF 6.3v — SODIMM DOWN SIDE

4 caps near each side of DIMM connector close to VDD pins

CON K86569-001 2/4 2 OF 4
J2C2C
INS17151595

VDD	112	
VDD	111	
VDD	163	
VDD	160	
VDD	159	
VDD	154	
VDD	153	
VDD	148	
VDD	147	
VDD	142	
VDD	141	
VDD	136	
VDD	135	
VDD	130	
VDD	129	
VDD	124	
VDD	123	
VDD	118	
VDD	117	
VPP	259	
VPP	257	
VTT	258	

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Change +V_VTT_MEM to +VTT

Change +VPP_2P5U_MEM to +VPP

+VTT — C245 C246 0402 1uF — C248 10uF ,6.3V,0603 NOP

+VPP — C243 0402 1uF — C244 10uF ,6.3V,0603

place as close as possible to DRAM.

CON
J2C2D
INS17151867

252	VSS	VSS	98
251	VSS	VSS	94
248	VSS	VSS	93
247	VSS	VSS	90
244	VSS	VSS	89
243	VSS	VSS	86
239	VSS	VSS	85
238	VSS	VSS	82
235	VSS	VSS	81
234	VSS	VSS	78
231	VSS	VSS	77
230	VSS	VSS	73
227	VSS	VSS	72
226	VSS	VSS	69
223	VSS	VSS	68
222	VSS	VSS	65
218	VSS	VSS	64
217	VSS	VSS	61
214	VSS	VSS	60
213	VSS	VSS	57
210	VSS	VSS	56
209	VSS	VSS	52
206	VSS	VSS	51
205	VSS	VSS	48
202	VSS	VSS	47
201	VSS	VSS	44
197	VSS	VSS	43
196	VSS	VSS	40
193	VSS	VSS	39
192	VSS	VSS	36
189	VSS	VSS	35
188	VSS	VSS	31
185	VSS	VSS	30
184	VSS	VSS	27
181	VSS	VSS	26
180	VSS	VSS	23
176	VSS	VSS	22
175	VSS	VSS	19
172	VSS	VSS	18
171	VSS	VSS	15
168	VSS	VSS	14
167	VSS	VSS	10
107	VSS	VSS	9
106	VSS	VSS	6
103	VSS	VSS	5
102	VSS	VSS	2
99	VSS	VSS	1
262	MP2	MP1	261

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Title	<Title>
Size A3	Document Number <Doc>
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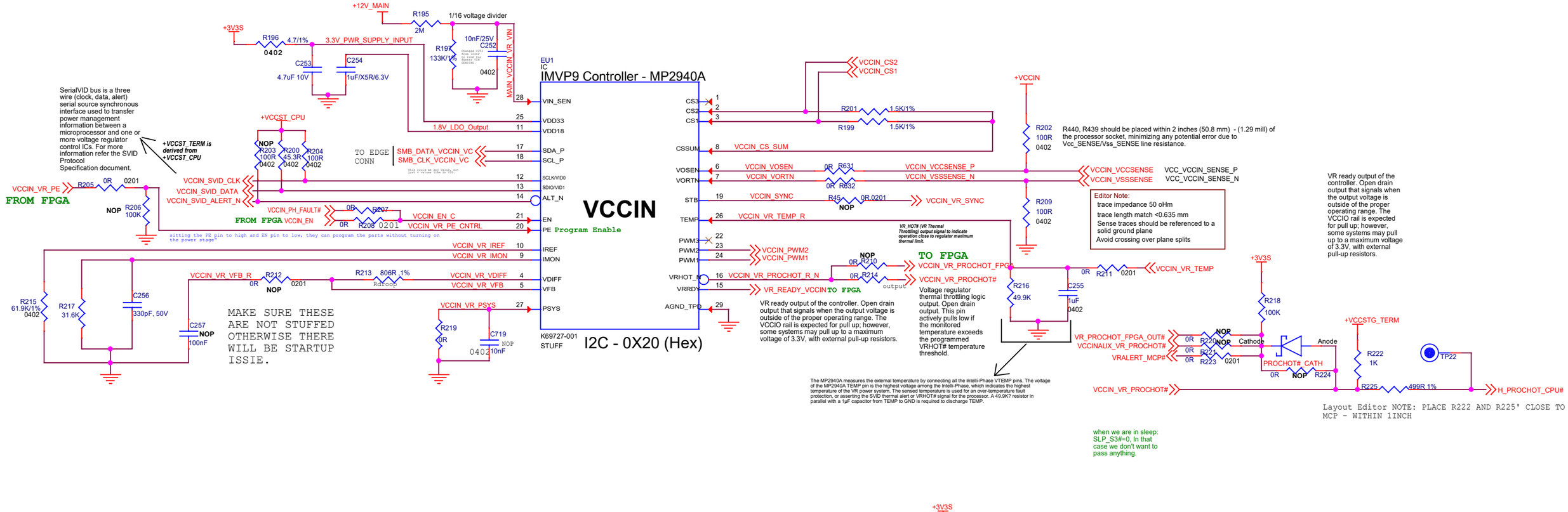
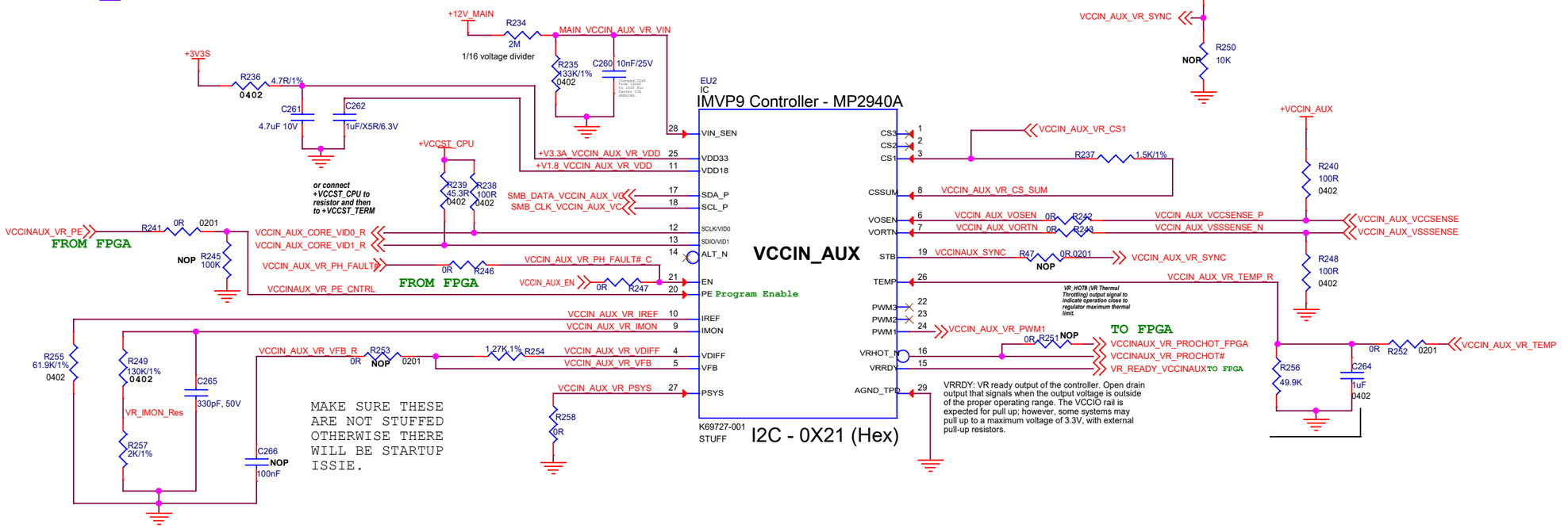
VCCIN RAIL POWER CONVERSION



VCCIN_AUX RAIL POWER CONVERSION



VID TABLE			
VID 1	VID 2	Output Voltage	Usage
0	0	0V	Power Saving State
0	1	1.1V	Register
1	0	1.65V	Full Current, TGL-UP4
1	1	1.8V	Initial boot for TGL-UP3/UP4 Full current, TGL-UP3

Title	IMVP9 CTLR-VCCIN / VCCIN_AUX		
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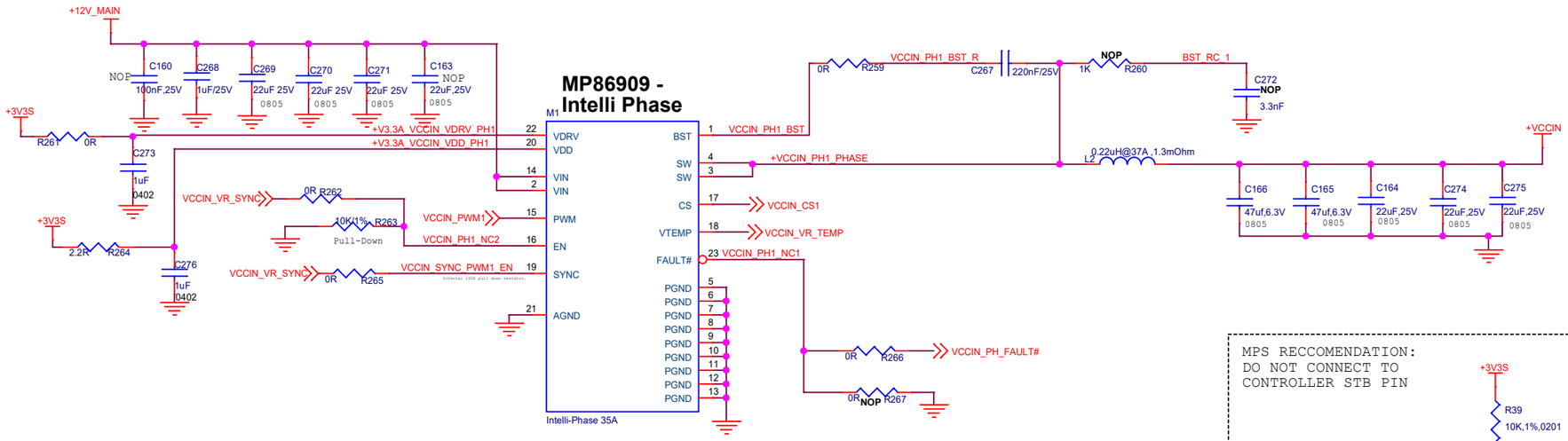
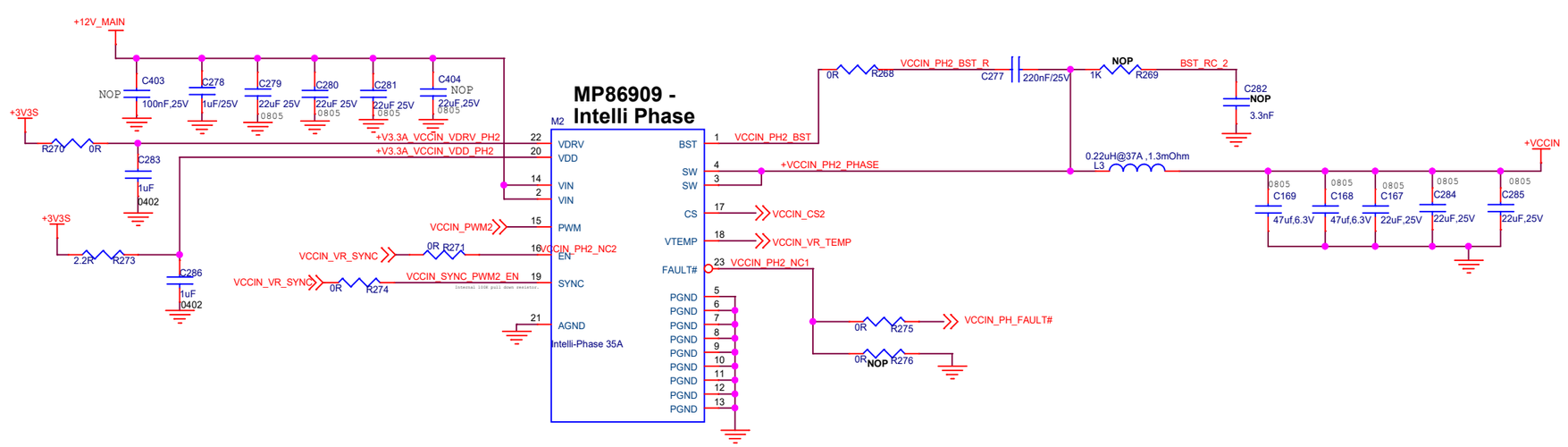


MPS RECCOMENDATION:
DO NOT CONNECT TO
CONTROLLER STB PIN

VCCIN POWER CONVERSION PHASE I



VCCIN POWER CONVERSION PHASE II

Title	PWR IMVP9- VCCIN PH1/PH2/PH3		
Size A3	Document Number <Doc>		Rev <RevCode>
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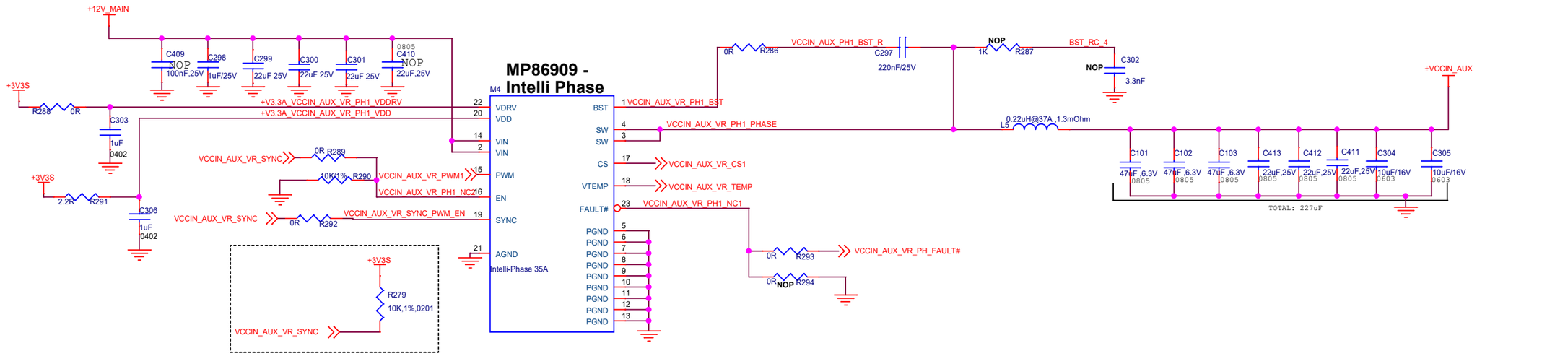
VCCIN_AUX POWER CONVERSION PHASE I



Title	PWR IMVP9- VCCIN_AUX PH1	
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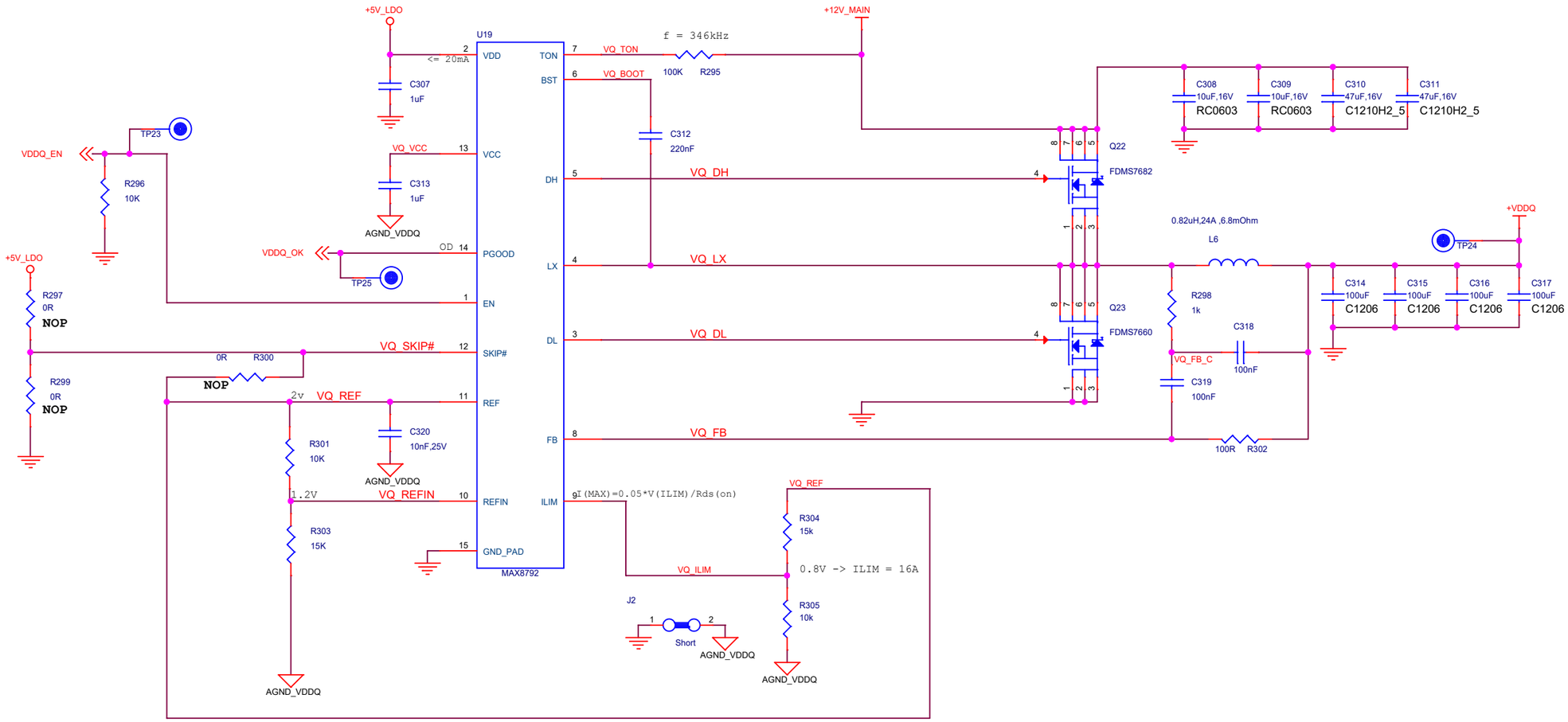
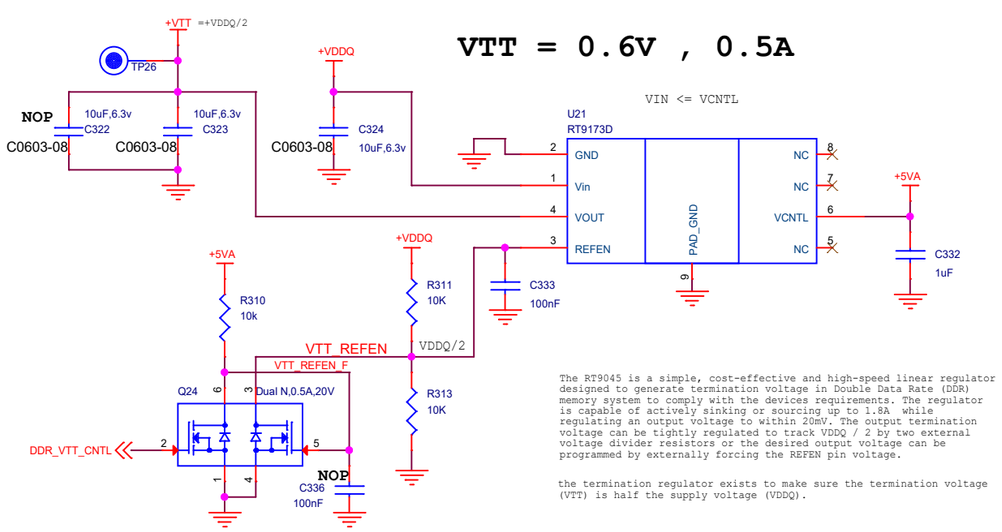
VDDQ = 1.2V , 15A

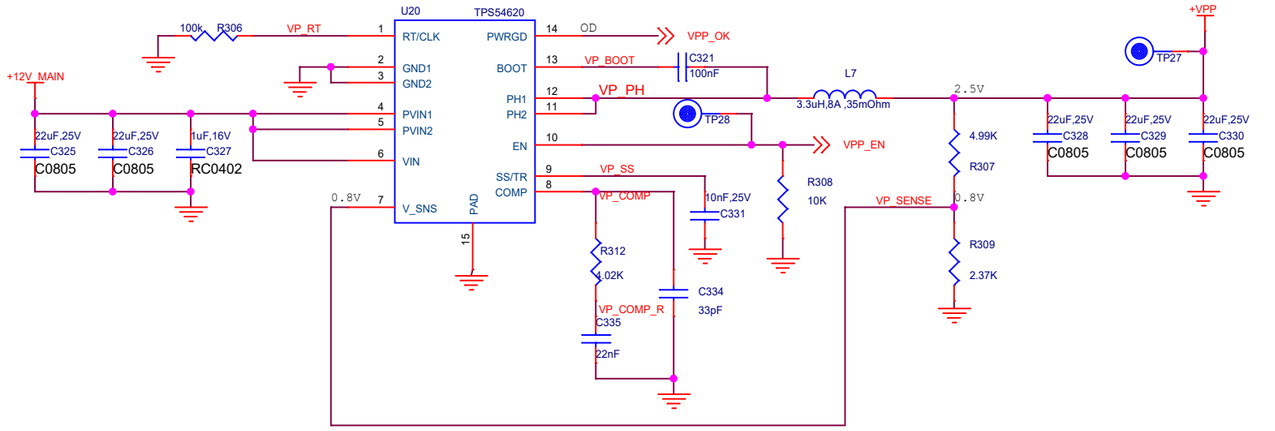


VTT = 0.6V , 0.5A



VPP = 2.5V , 1A

DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)



Title	PWR VDDQ/VTT/VPP	
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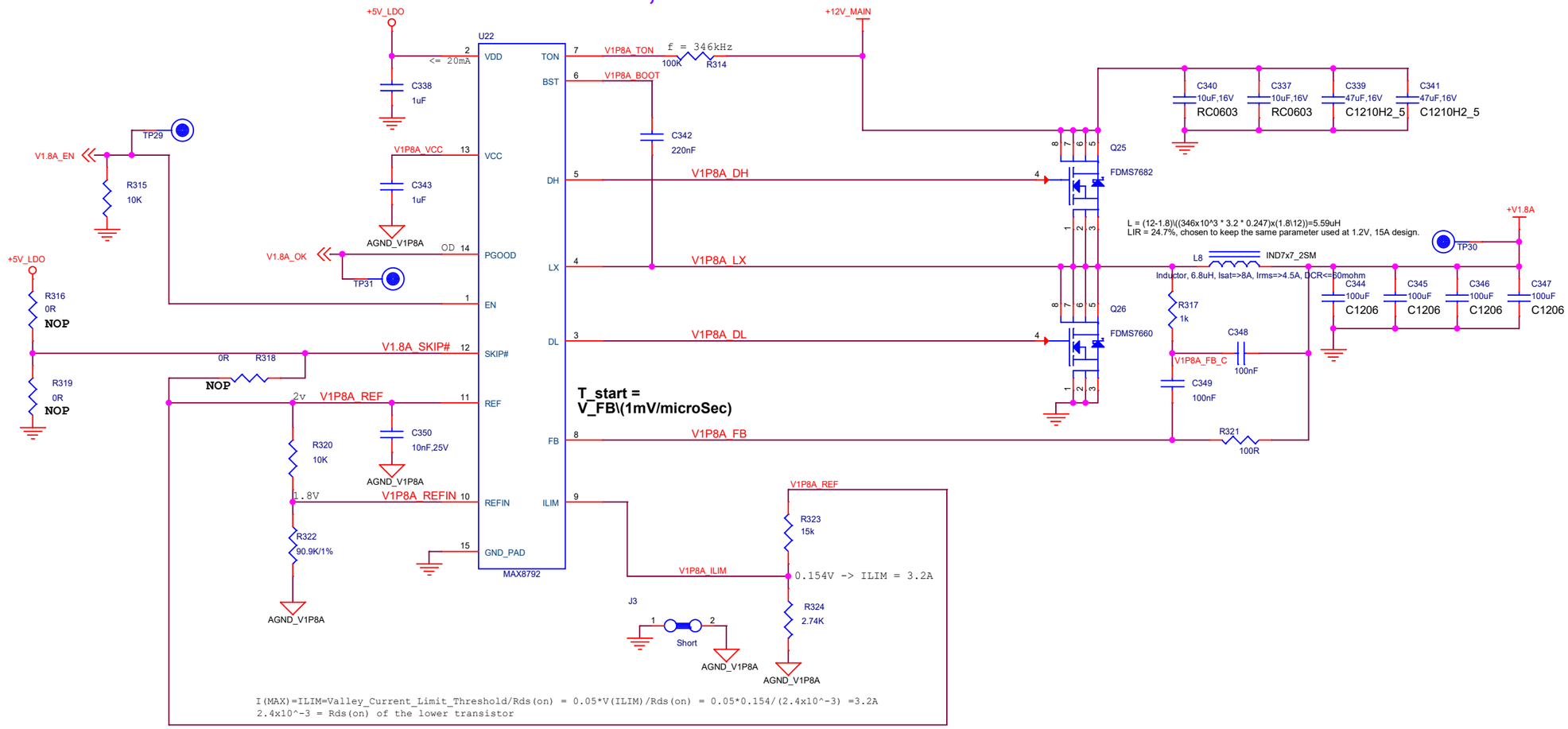
+V1.8A, 3A



Title	PWR +V1.8A	
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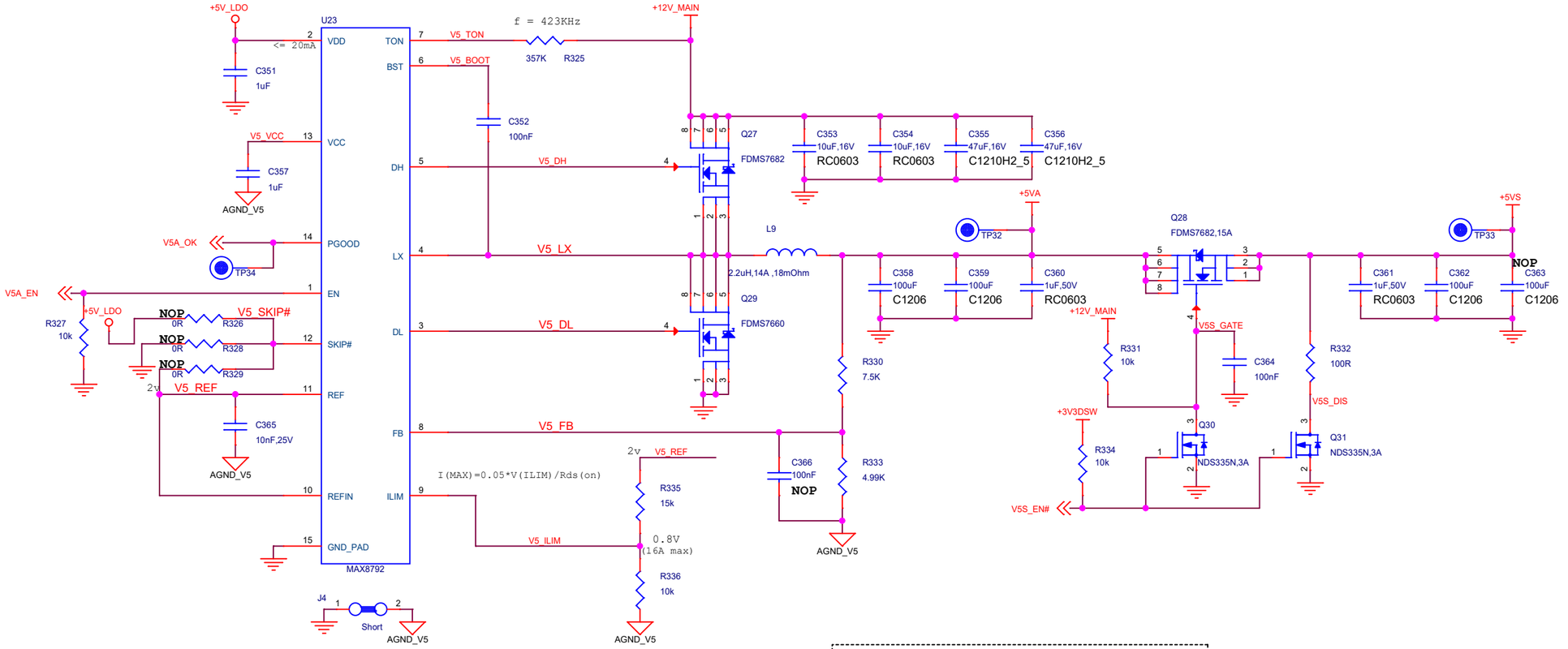
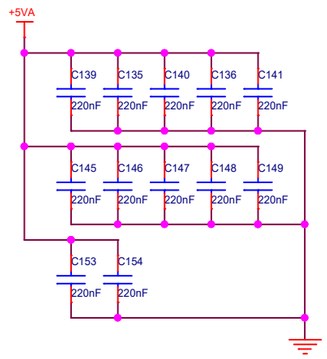
5V , 15A



Plane stitching capacitors



Title: PWR 5V		
Size: A3	Document Number: <Doc>	Rev: <RevCode>
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VCCST_PWRGD
Indication that the VCCSTG\VCCST\VDDQ power supplies are stable and within specification

VCCST Power Good: The processor requires this input signal to be a clean indication that the VCCST and VDDQ power supplies are stable and within specifications. This signal should have a valid level during S0, both S0 and S3 (H SKU) power states. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal then transition monotonically to a high state.

VCCST_PWRGD is a signal on the Tiger Lake processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specifications.

P12J
D2
ANAIN1_D2

+VCCST_CPU
Input Signal
R37
1K, 1%, 0201
VCCST_PWRGD
R338
63.4R
In SBC-CLH vccst_pwrgd is only 1.0 V tolerant
That's why there was a pull-down to GND through 3.01K resistor and a series 6.49K res to VCCST_PWRGD_3V3

P12D
GPIO_FPGA_PM_{1..4} (RMVD)
(Added) V1.8A_EN
V12S_EN (RMVD) V1.8A_OK
FPGA_PU VCCST_OVERRIDE_3V3
V33DSW_OK VCCST_PWRGD_3V3
SLP_SUS#
V12S_OK (RMVD)
FPGA_TP1
TP35
FPGA_TP2
TP36
SV_WD_RESET (RMVD)
V5S_OK moved from IO_3_N12 to IO_2_N2
V33A_OK
V33S_OK
V105A_OK (REPLACED) +VCCST_CPU_OK
(+VCCST_CPU derived from internal SoC VR output:+VCCIP05_OUT_FET)
PCH_SPKR_R (REPLACED) SOC_SPKR
PWRBTN_LED
SUSWARN# SUSACK#
R343 0R SUSWARN# FPGA
R344 0R SUSACK# FPGA
NOP
FPGA_PU RSMRST#
IO_3_L5/DIFFIO_TX_RX_B1N
IO_3_M4/DIFFIO_RX_B2N
IO_3_L4/DIFFIO_TX_RX_B1P
IO_3_M5/DIFFIO_RX_B2P
IO_3_K5/DIFFIO_TX_RX_B3N
IO_3_N4/DIFFIO_RX_B4N
IO_3_J5/DIFFIO_TX_RX_B3P
IO_3_N5/DIFFIO_RX_B4P
IO_3_N6/DIFFIO_TX_RX_B5N
IO_3_N7/DIFFIO_RX_B6N
IO_3_M7/DIFFIO_TX_RX_B5P
IO_3_N8/DIFFIO_RX_B6P
IO_3_J6/DIFFIO_TX_RX_B7N
IO_3_M8/DIFFIO_RX_B8N
IO_3_K6/DIFFIO_TX_RX_B7P
IO_3_M9/DIFFIO_RX_B8P
IO_3_J7/DIFFIO_TX_RX_B9N
IO_3_K7/DIFFIO_TX_RX_B9P
IO_3_N12
IO_3_M13/DIFFIO_TX_RX_B10N
IO_3_N10/DIFFIO_RX_B11N
IO_3_M12/DIFFIO_TX_RX_B10P
IO_3_N9/DIFFIO_RX_B11P
IO_3_M11/DIFFIO_TX_RX_B12N
IO_3_L11/DIFFIO_TX_RX_B12P
IO_3_J8/DIFFIO_TX_RX_B14N
IO_3_K8/DIFFIO_TX_RX_B14P
IO_3_M10/DIFFIO_TX_RX_B16N
IO_3_L10/DIFFIO_TX_RX_B16P
FPGA

P12E
GPIO_FPGA_SV_{1..4} (RMVD)
(From BIOS) HDA_SDO_ATP
R59 1K 1% 0402 HDA_SDO_ATP_RES
VCCST_OK (REPLACED) +VCCST_CPU_OK
VCCST_EN
PCH_PWROK
TPM_GPIO
GPIO_FPGA_EXP_1
GPIO_FPGA_EXP_2
IO_5_K10/DIFFIO_RX_R1P
IO_5_K11/DIFFIO_RX_R2P
IO_5_J10/DIFFIO_RX_R1N
IO_5_L12/DIFFIO_RX_R2N
IO_5_K12/DIFFIO_RX_R7P
IO_5_L13
IO_5_J12/DIFFIO_RX_R7N
IO_5_J9/DIFFIO_RX_R8P
IO_5_J13/DIFFIO_RX_R9P
IO_5_H10/DIFFIO_RX_R8N
IO_5_H13/DIFFIO_RX_R9N
IO_5_H9/DIFFIO_RX_R10P
IO_5_G13/DIFFIO_RX_R11P
IO_5_H8/DIFFIO_RX_R10N
IO_5_G12/DIFFIO_RX_R11N
FPGA

P12K
GND_N13
GND_N1
GND_M6
GND_L9
GND_J4
GND_H12
GND_G7
GND_F3
GND_E11
GND_D5
GND_C3
GND_B8
GND_A13
GND_A1
REFGND_E2
FPGA

a request from BIOS to FPGA to perform operations. 1. restart, start HDA, next start stop the HDA.

when GPIO_FPGA_MCP_1 is pulled low ('0'), we wait for PCH_PWROK =0 (reset), then the FPGA pulls HDA_SDO high ('1')

P12F
(Added) GPIO_FPGA_SoC_1
GPIO_FPGA_SoC_2
GPIO_FPGA_SoC_3
GPIO_FPGA_SoC_4
PWRBTN#
(Added) GPIO_FPGA_SoC_5
(Added) CPU_C10_GATE#
SLP_S4#
VPP_EN
VPP_OK
FPGA_PU
(Added) SLP_S0#
SLP_S3#
DSW_PWROK
IO_6_F12/DIFFIO_RX_R18P
IO_6_E12/DIFFIO_RX_R18N
IO_6_C13
IO_6_F8/DIFFIO_RX_R27P
IO_6_B12/DIFFIO_RX_R28P
IO_6_E9/DIFFIO_RX_R27N
IO_6_B11/DIFFIO_RX_R28N
IO_6_C12/DIFFIO_RX_R29P
IO_6_B13/DIFFIO_RX_R30P
IO_6_C11/DIFFIO_RX_R29N
IO_6_A12/DIFFIO_RX_R30N
IO_6_E10/DIFFIO_RX_R31P
IO_6_D9/DIFFIO_RX_R31N
IO_6_D12/DIFFIO_RX_R33P
IO_6_D11/DIFFIO_RX_R33N
FPGA

+3V3DSW
C368 C369 C370 C371 C372
100nF 100nF 100nF 100nF 100nF
FPGA_VCCA
C373 C374
1uF 100nF
R349
2.2R
100nF near F2
+3V3DSW
C375 C376 C377 C378
100nF 100nF 100nF 100nF

P12A
VCCIO1A_F2
VCCIO1B_G3
VCCIO2_K3
VCCIO2_J3
VCCIO3_L8
VCCIO3_L7
VCCIO3_L6
VCCIO5_J11
VCCIO5_H11
VCCIO6_G11
VCCIO6_F11
VCCIO8_C8
VCCIO8_C7
VCCIO8_C6
VCCA1_K4
VCCA2_D10
VCCA3_D4
VCCA4_K9
VCC_ONE_H7
VCC_ONE_G8
VCC_ONE_G6
VCC_ONE_F7
FPGA

+12V_MAIN
R340
20K
FPGA_ADC
R341 10R
FPGA_ADC_F
C367
3.3nF
R342
2.21K
V33S_EN#
V5S_EN#
V33A_EN#
R345 0R V33A_EN# FPGA
P12B
IO_1A_D1/ADC1IN1/DIFFIO_RX_L1N
IO_1A_C2/ADC1IN2/DIFFIO_RX_L1P
IO_1A_E3/ADC1IN3/DIFFIO_RX_L3N
IO_1A_E4/ADC1IN4/DIFFIO_RX_L3P
IO_1A_C1/ADC1IN5/DIFFIO_RX_L5N
IO_1A_B1/ADC1IN6/DIFFIO_RX_L5P
IO_1A_F1/ADC1IN7/DIFFIO_RX_L7N
IO_1A_E1/ADC1IN8/DIFFIO_RX_L7P
IO_1B_F4/DIFFIO_RX_L14N
IO_1B_G4/DIFFIO_RX_L14P
IO_1B_H2/DIFFIO_RX_L16N
IO_1B_H3/DIFFIO_RX_L16P
FPGA

+3V3DSW +3V3DSW
R356 10k
R409 10k
+3V3DSW
R350 10k
R351 1K
R352 1K
FPGA_JEN
FPGA_TMS
FPGA_TCK
FPGA_TDI
FPGA_TDO
FPGA_CLRN
TP37
FPGA_NCONF
FPGA_CRC_E
TP38
FPGA_NSTAT
FPGA_C_DONE
R410
1K
P12I
IO_1B_E5/JTAGEN
IO_1B_G1/TMS/DIFFIO_RX_L11N
IO_1B_G2/TCK/DIFFIO_RX_L11P
IO_1B_F5/TDI/DIFFIO_RX_L12N
IO_1B_F6/TDO/DIFFIO_RX_L12P
IO_8_B9/DEV_CLRN/DIFFIO_RX_T16N
IO_8_D8/DEV_OE/DIFFIO_RX_T18P
IO_8_D7/CONFIG_SEL
INPUT_ONLY_8_E7/NCONFIG
IO_8_D6/CRC_ERROR/DIFFIO_RX_T22N
IO_8_C4/NSTATUS/DIFFIO_RX_T24P
IO_8_C5/CONF_DONE/DIFFIO_RX_T24N
FPGA

+3V3DSW
C379
100nF
OSC1
VCC EN
GND OUT
25MHz 50ppm 3.2x2.5
FPGA_OSC
Moved here from IO_3_N12 V5S_OK
(Provision) FP_RST#
VREF is NC if internal ref. used
VREFB is for SSTL, HSTL, and HSUL I/O Standards
P12H
IO_2_G5/CLK0N/DIFFIO_RX_L18N
IO_2_H6/CLK0P/DIFFIO_RX_L18P
IO_2_H5/CLK1N/DIFFIO_RX_L20N
IO_2_H4/CLK1P/DIFFIO_RX_L20P
IO_2_N2/DPCLK0/DIFFIO_RX_L22N
IO_2_N3/DPCLK1/DIFFIO_RX_L22P
IO_6_G9/CLK2P/DIFFIO_RX_R14P
IO_6_G10/CLK2N/DIFFIO_RX_R14N
IO_6_F13/CLK3P/DIFFIO_RX_R16P
IO_6_E13/CLK3N/DIFFIO_RX_R16N
IO_6_F9/DPCLK3/DIFFIO_RX_R26P
IO_6_F10/DPCLK2/DIFFIO_RX_R26N
ADC_VREF_D3
VREFB1N0
VREFB2N0
VREFB3N0
VREFB5N0
VREFB6N0
VREFB8N0
FPGA

P12C
V105A_EN (RMVD) (NO VR for 1.05V, it comes from the CPU from Internal VR)
V5A_EN R346 0R V5_EN_FPGA
FPGA_GPIO_WD (RMVD)
RTCRST#_FPGA
V5A_OK
FPGA_PU
FPGA_PU
IO_2_J1/DIFFIO_RX_L19N
IO_2_J2/DIFFIO_RX_L19P
IO_2_M1/DIFFIO_RX_L21N
IO_2_M2/DIFFIO_RX_L21P
IO_2_L2
IO_2_K1/DIFFIO_RX_L28N
IO_2_K2/DIFFIO_RX_L28P
IO_2_M3/PLL_L_CLKOUTN/DIFFIO_RX_L27N
IO_2_L3/PLL_L_CLKOUTP/DIFFIO_RX_L27P
FPGA

CONF_DONE:
The Intel Quartus Prime software uses the CONF_DONE pin to verify the completion of the configuration process through the JTAG port:
• CONF_DONE pin is low—indicates that the configuration has failed.
• CONF_DONE pin is high—indicates that the configuration was successful.

This circuit purpose is to Enable FPGA to perform RTCRST#.
when RTCRST#_FPGA is LOW RTCRST# is LOW.
RTCRST# doesn't go LOW when there is no +3V3DSW. which means after we the SoC has passed all powerup sequence and it's alive, only after that RTCRST# can operate.

RTCRST to FPGA buffer
FPGA_C_DONE
+3V3DSW
R353 10k
NOP
R354 10k
RTCRST#
RTCRST#_FPGA_Q
Q32
RTCRST#_FPGA
(Provision)
Dual N,0.5A,20V
NOP
The purpose of if this circuit is to be able to perform RTCRST from FPGA.

P12G
VDDQ_EN
VDDQ_OK
VR_PROCHOT_FPGA_OUT#
VCCINAUX_VR_PROCHOT_FPGA
FPGA_PU
VCCIO_OK RMVD
VCCIO_EN RMVD
(Added) VCCIN_VR_PROCHOT_FPGA
VCCSA_READY (RMVD) VR_READY_VCCINAUX
VCCSA_EN (RMVD) VCCIN_AUX_EN
(Added) VCCINAUX_VR_PE
VR_READY (REPLACED) VR_READY_VCCIN
(Added) VCCIN_VR_PE
VR_EN (RMVD) VCCIN_EN
PLTRST#
SYS_PWROK
SLP_S5#
IO_8_C10/DIFFIO_RX_T14P
IO_8_A8/DIFFIO_RX_T15P
IO_8_C9/DIFFIO_RX_T14N
IO_8_A9/DIFFIO_RX_T15N
IO_8_B10/DIFFIO_RX_T16P
IO_8_A10/DIFFIO_RX_T17P
IO_8_A11/DIFFIO_RX_T17N
IO_8_E8/DIFFIO_RX_T18N
IO_8_A7/DIFFIO_RX_T19P
IO_8_A6/DIFFIO_RX_T19N
IO_8_B6/DIFFIO_RX_T20P
IO_8_A4/DIFFIO_RX_T21P
IO_8_B5/DIFFIO_RX_T20N
IO_8_A3/DIFFIO_RX_T21N
IO_8_E6/DIFFIO_RX_T22P
IO_8_B3/DIFFIO_RX_T23P
IO_8_B4/DIFFIO_RX_T23N
IO_8_A5
IO_8_A2/DIFFIO_RX_T26P
IO_8_B2/DIFFIO_RX_T26N
FPGA

EDGE CONNECTOR
FPGA, SPI flash and IMVP9 programing edge connector For use with SBC-TI22 ATP

Before Connecting the 5VA Jumper make sure that ATP_HDA_SDO signal is O.K. with 5V.
+3V3DSW
C380
100nF
+3V3DSW +3V3DSW
R71 2.21k
R70 2.21k
NOP
Renesas (ZLUSBEVAL3Z) Adapter already has 4.7K PU to +3V3DSW which is provided.
P13
SPI_ATP_CTRL#
SPI_ATP_SI
SPI_ATP_SO
SPI_ATP_CLK
SPI_ATP_CS0
HDA_SDO_ATP
SMB_DATA_VR
SMB_CLK_VR
+3V3DSW
FPGA_JEN
FPGA_TDI
FPGA_TMS
FPGA_TDO
FPGA_TCK
PCIE x1 EDGE CONN.
R49 0R 5%,0402 SMB_DATA_VCCIN_VC
R67 0R 5%,0402 SMB_CLK_VCCIN_VC
VCCIN IMVP9 Controller
I2C - 0X20 (Hex)
R68 0R 5%,0402 SMB_DATA_VCCIN_AUX_VC
R69 0R 5%,0402 SMB_CLK_VCCIN_AUX_VC
VCCIN_AUX IMVP9 Controller
I2C - 0X21 (Hex)

Title	FPGA/EDGE CONN
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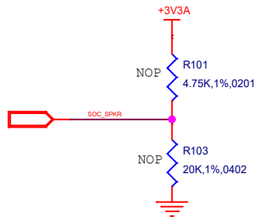
PCH STRAPS

TOP SWAP OVERRIDE

GPP_B14



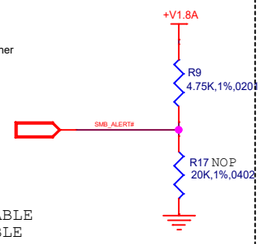
HIGH- TOP SWAP ENABLED
LOW-DISABLED

WEAK INTERNAL PD 20K

Sampled at Rising edge of PCH_PWROK

TLS CONFIDENTIALITY

ME TLS Confidentiality Strap (PU)
This strap has a 20 kohm ± 30% internal pull-down.
0=>Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1=>Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.



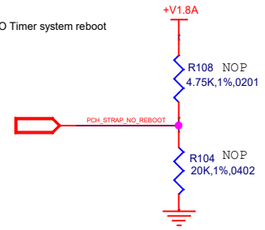
LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

WEAK INTERNAL PD 20K

Sampled at Rising edge of RSMRST#

NO REBOOT

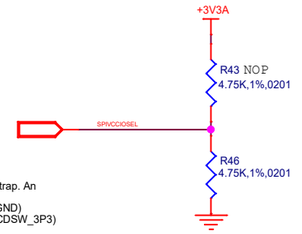
The strap has a 20 kohm ± 30% internal pull-down.
0=>Disable "No Reboot" mode. (Default)
1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
Notes: 1. The internal pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.



HIGH - NO REBOOT
LOW- REBOOT ENABLED
WEAK INTERNAL PD 20K

Sampled at Rising edge of PCH_PWROK

STRAP FOR SPI 1.8V/3.3V SELECTION

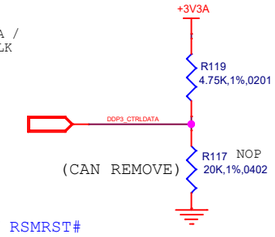


There is no internal pull-up or pull-down on the strap. An external resistor is required.
0 = SPI voltage is 3.3 V (4.7 kohm pull-down to GND)
1 = SPI voltage is 1.8 V (4.7 kohm pull-up to VCCDSW_3P3)

Not sampled. This strap must always be driven to a valid logic level

TBT LSX #2 PINS VCCIO CONFIGURATION

GPP_D10 / ISH_SPI_CLK / DDP3_CTRLDATA / TBT_LSX2_RXD / BSSB_LS2_TX / GSPI2_CLK



HIGH: 3.3V
LOW: 1.8V
WEAK INTERNAL PD 20K

Sampled at Rising edge of RSMRST#

This strap has a 20 kohm ± 30% internal pull-down.
0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8 V
1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3 V

SPI0_IO2 STRAP - RSVD

PU PLACED NEXT TO SPI FLASH (U26)

SPI0_IO3 STRAP - RSVD

PU PLACED NEXT TO SPI FLASH (U26)

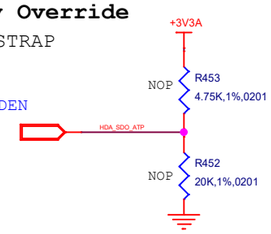
Flash Descriptor Security Override

GPP_R2 / HDA_SDO / I2S0_TXD STRAP

GPP_R2 / HDA_SDO / I2S0_TXD

HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN
WEAK INTERNAL PD 20K

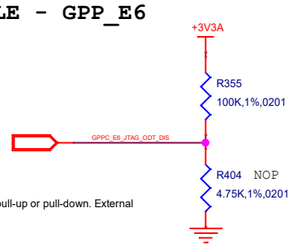
THIS SIGNAL IS TIED TO A JUMPER ON ATP CARD



To support Intel® ME, a SPI flash is required on the platform with sufficient space to hold system BIOS, Intel® ME firmware, Intel® Integrated Sensor Solution firmware and any additional third party data storage. The SPI flash needs to be powered in states S0 through S5, independent of Intel® ME power state.
GPP_R2 / HDA_SDO / I2S0_TXD signal is used for Flash Descriptor Security Override (which is also known as Intel® ME Debug Mode). This signal input should be tied to a jumper which connects to power through an external pull-up (1 KO ±5%) only. When this signal is asserted, the Flash Security gets overridden for ease of image programming.

Sampled at Rising edge of PCH_PWROK

JTAG ODT DISABLE - GPP_E6



This strap does not have an internal pull-up or pull-down. External pull-up is recommended
0=> JTAG ODT is disabled
1=> JTAG ODT is enabled

CAD NOTE:

PLACE R355 AND R404 CLOSE TO THE SPI SIGNAL TO AVOID STUB

USB_OC_CD#

10K PU at EB-TI22A

GPP_E10 / THC0_SPI1_CS#

THC0_SPI1 Chip Select: Used to select the touch devices if it is connected to THC0_SPI1 interface.

THC NOT USED IN TENSOR-I22

CAD NOTE:

PLACE R414,R415 AND R422 CLOSE TO THE SPI SIGNAL TO AVOID STUB

GPP_E11 / THC0_SPI1_CLK

THC0_SPI1 Clock: THC0 SPI1 clock output from PCH. Supports 20 MHz, 33 MHz and 50 MHz.

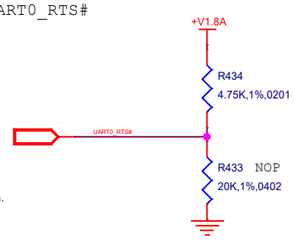
THC NOT USED IN TENSOR-I22

CAD NOTE:

PLACE R429,R430 AND R431 CLOSE TO THE SPI SIGNAL TO AVOID STUB

XTAL Frequency Selection

GPP_F0 / CNV_BRI_DT / UART0_RTS#



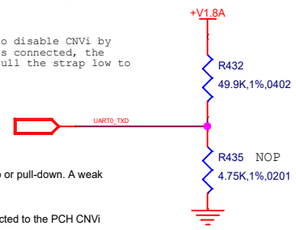
This strap has a 20 kohm ± 30% internal pull-down.
0 = 38.4 MHz (default)
1 = 24 MHz
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

M.2 CNVi Mode Select

GPP_F2 / CNV_RGI_DT / UART0_TXD

A weak external PU is required to disable CNVi by default. When a companion chip is connected, the required PD on the device will pull the strap low to enable CNVi.



This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.
0= Integrated CNVi enabled.
1= Integrated CNVi disabled.
Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

Sampled at Rising edge of RSMRST#

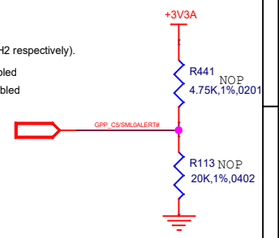
USB_OC_AB#

10K PU at EB-TI22A

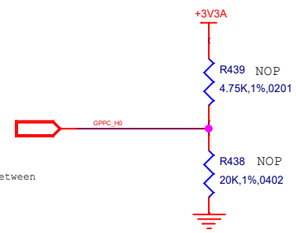
BOOT STRAP - BIT 0

This strap has a 20 kohm ± 30% internal pull-down.
This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration.
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).
4-bit boot strap configuration encodings:
0000 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is enabled

0010 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / Intel CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; Intel CSME on slave attached SPI.
Others: Reserved
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.



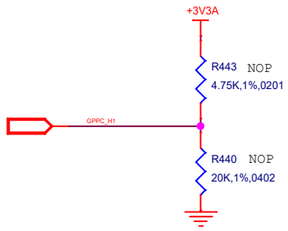
BOOT STRAP - BIT 1



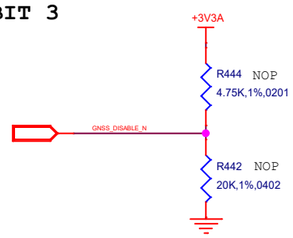
used for M2 PCH SSD RTD3, using AND between BUF_PLTRST# and GPPC_H0

Check TL-SBC (44/270)

BOOT STRAP - BIT 2



BOOT STRAP - BIT 3



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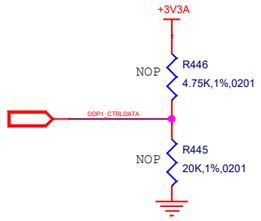
PCH STRAPS

TBT LSX #0 PINS VCCIO CONFIGURATION

GPP_E19 / DDP1_CTRLDATA / TBT_LSX0_RXD / BSSB_LS0_TX



This strap has a 20 kohm ± 30% internal pull-down.
0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8 V
1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

there is 2.2K PU on DPP1_CTRLDATA

Sampled at Rising edge of RSMRST#

TBT LSX #1 PINS VCCIO CONFIGURATION

GPP_E21 / DDP2_CTRLDATA / TBT_LSX1_RXD / BSSB_LS1_TX

NOTE: BSSB - Boundary Scan Sideband Low Speed Receive 1 for debug purposes

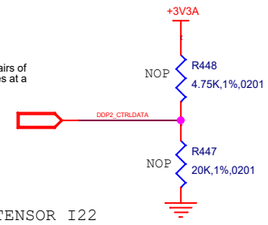
HIGH: 3.3V

LOW: 1.8V

WEAK INTERNAL PD 20K

LSx Interface:

The PCH LSx interface enables communication between one thunderbolt controller to another. TGL UP3/UP4 supports 4 pairs of LSx signals. The LSx signals use a UART interface. It operates at a 1 MHz baud rate and shares identical electrical characteristics/routing guidelines as UART.



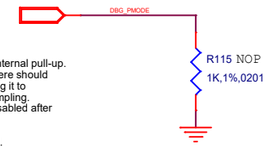
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 1.8 V
1 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

DPP12_CTRLDATA NOT USED IN TENSOR I22

Sampled at Rising edge of RSMRST#

DBG_PMODE

RESERVED

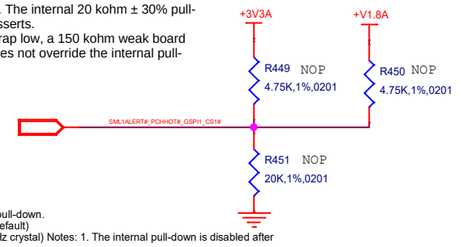


This strap has a 20 kohm ± 30% internal pull-up.
This strap should sample high. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-up is disabled after RSMRST#
de-asserts.
2. This signal is in the primary well.

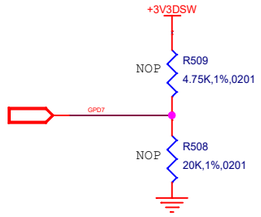
Sampled at Rising edge of RSMRST#

CPUNSSC CLOCK FREQ

Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.
Note: When used as PCHHOT# and strap low, a 150 kohm weak board pull-up is recommended to ensure it does not override the internal pull-down strap sampling.



This strap has a 20 kohm ± 30% internal pull-down.
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal) Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150
kohm pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.



GPP_F10

This strap has a 20 kohm ± 30% internal pull-down.
This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

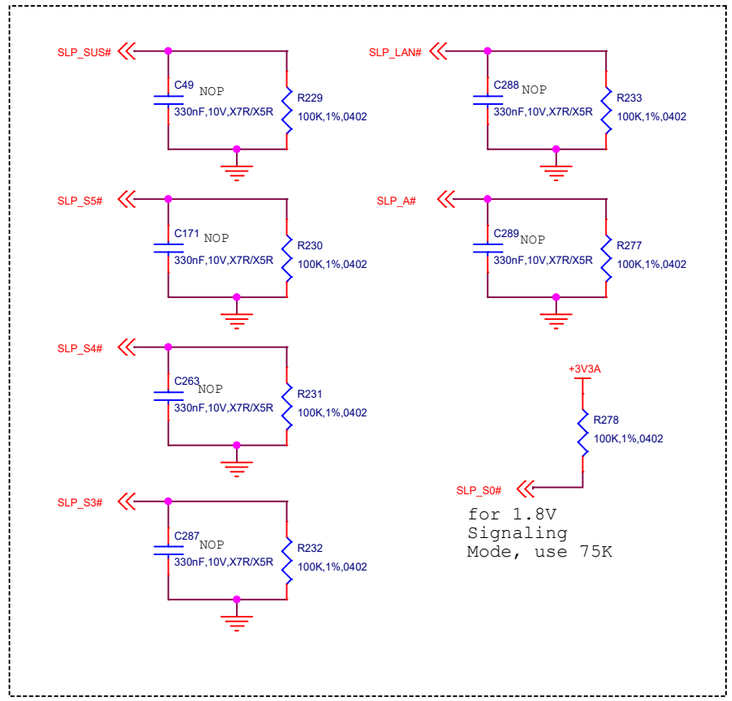
GPD7

This strap has a 20 kohm ± 30% internal pull-down.
This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-down is disabled after DSW_PWROK is high.
2. This signal is in the DSW well.

Sampled at Rising edge of DSW_PWROK

PCH GLITCH ISSUE MITIGATION

RC0201



Title: PCH STRAPS (2 OF 2)		
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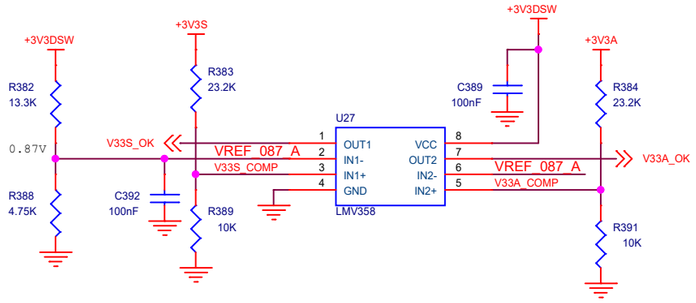
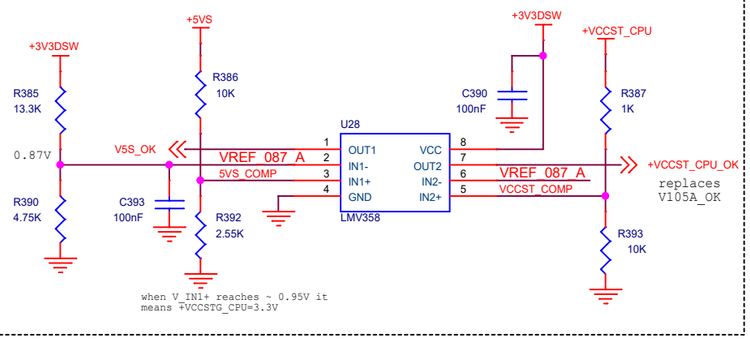
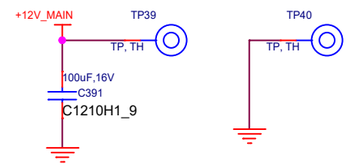
+3V3S,+3V3A PWRGD



+5VS, VCCST_CPU PWRGD



Hanging 1x2 connector



Title	3V3S\3V3A\VCCCST PWRGD	
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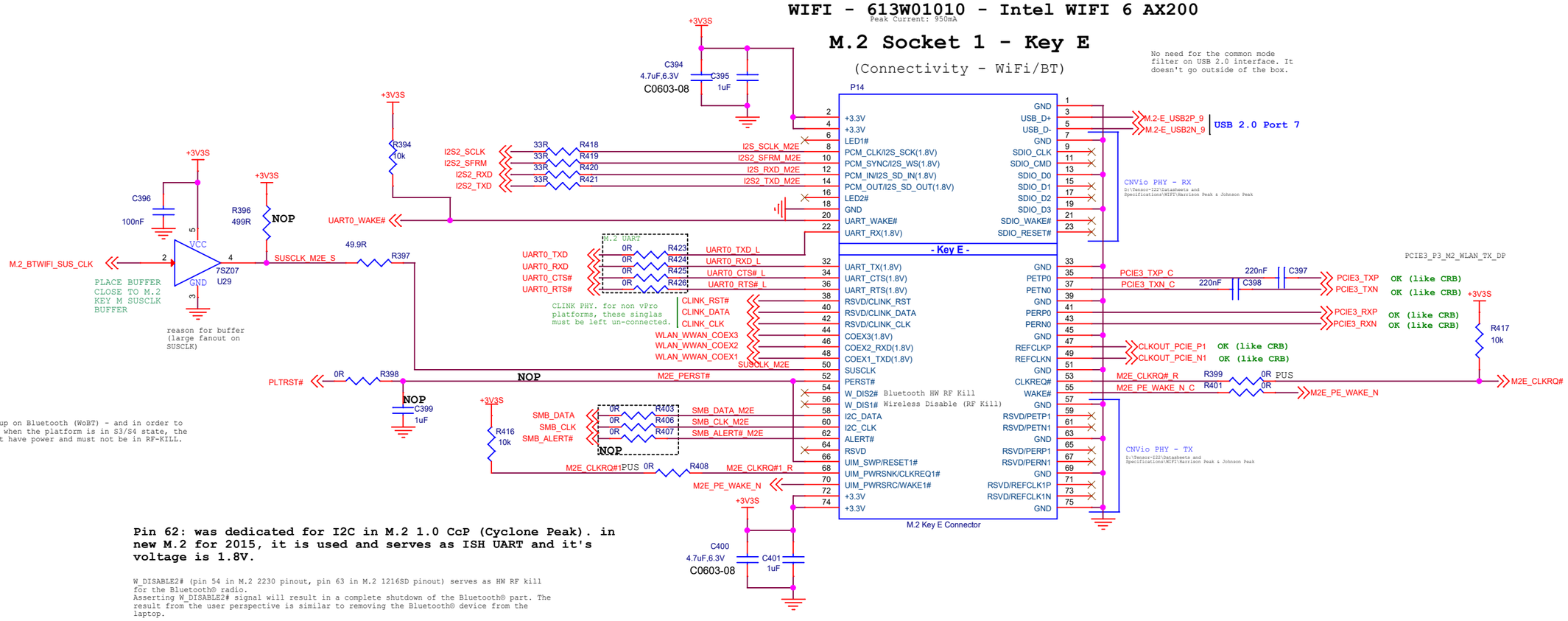
WIFI - 613W01010 - Intel WIFI 6 AX200

Peak Current: 950mA

M.2 Socket 1 - Key E

(Connectivity - WiFi/BT)

No need for the common mode filter on USB 2.0 interface. It doesn't go outside of the box.



To enable Wak-up on Bluetooth (WoBT) - and in order to work correctly when the platform is in S3/S4 state, the controller must have power and must not be in RF-KILL.

PLACE BUFFER CLOSE TO M.2 KEY M SUSCLK BUFFER

reason for buffer (large fanout on SUSCLK)

Pin 62: was dedicated for I2C in M.2 1.0 CcP (Cyclone Peak). in new M.2 for 2015, it is used and serves as ISH UART and it's voltage is 1.8V.

W_DISABLE2# (pin 54 in M.2 2230 pinout, pin 63 in M.2 1216SD pinout) serves as HW RF kill for the Bluetooth® radio.
Asserting W_DISABLE2# signal will result in a complete shutdown of the Bluetooth® part. The result from the user perspective is similar to removing the Bluetooth® device from the laptop.

W_DISABLE2# characteristics

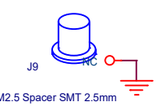
Internal pull-up resistor min 100 kOhm, max 200kOhm

VIL for asserting min 0V, max 0.6V

VIH for de-asserting min 1.26V, max 3.3V or float (not connected)

The recommendation is to use HW RF kill functionality by using a GPIO pin provided by the ACPI to turn on/off the radio of the Bluetooth® device.
BIOS shall implement ACPI function for HW RF-Kill implementation in the OS.
For more information, please refer to Intel document 559910, Intel Connectivity Platform BIOS Guidelines, Section 3.1.5.6, "BT RTD3 control."

SPACER for Key-E



Title	M.2 E (WiFi/BT)	
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Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module type and main host interface
GND	GND	GND	GND	SSD-SATA
GND	NC	GND	GND	SSD-PCIe
NC	GND	GND	GND	WWAN-SSIC
NC	NC	NC	NC	No Module Present

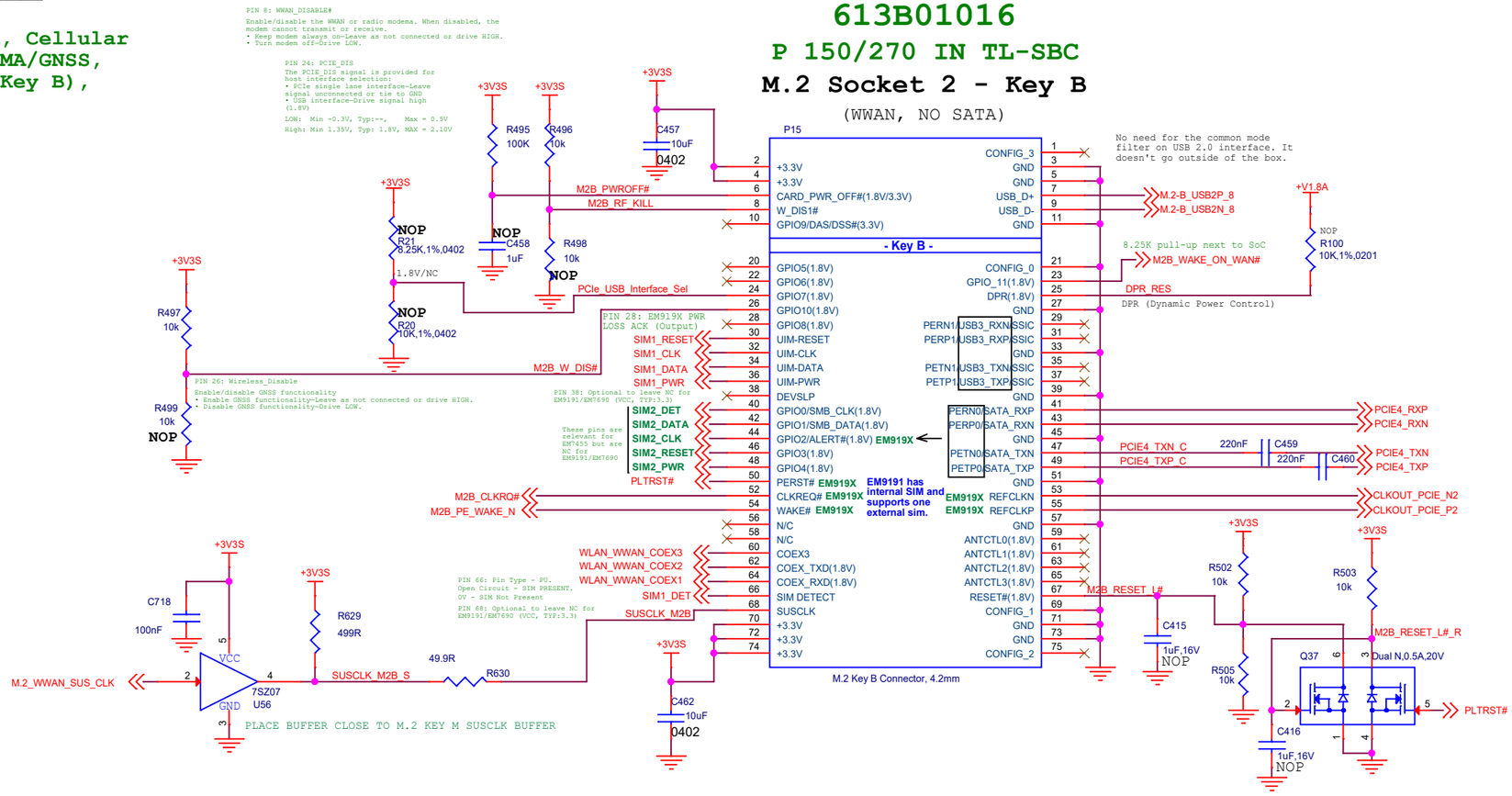
Communication Equipment, Cellular Modem, 5G/LTE/HSPA+/WCDMA/GNSS, Global-Band, M.2 3052 (Key B), Sierra EM9191

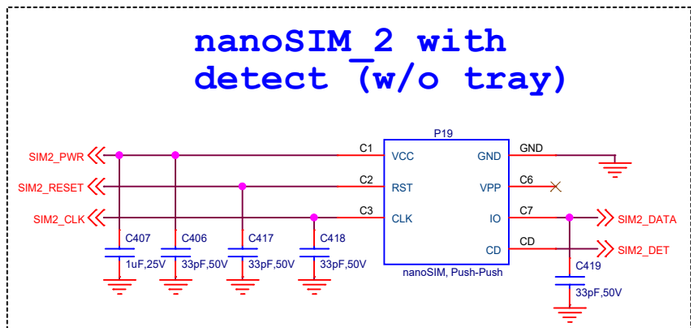
613B01016

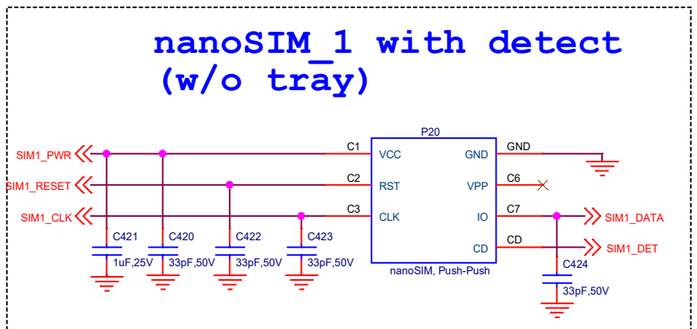
P 150/270 IN TL-SBC

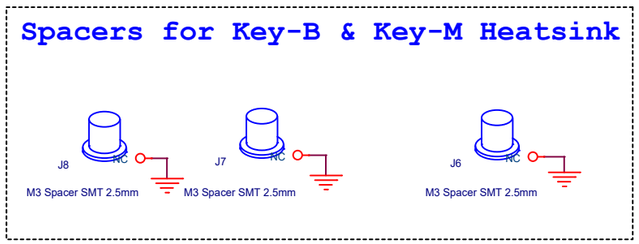
M.2 Socket 2 - Key B

(WWAN, NO SATA)









Title	M.2 B (WWAN)	
Size A3	Document Number <Doc>	Rev <RevCo
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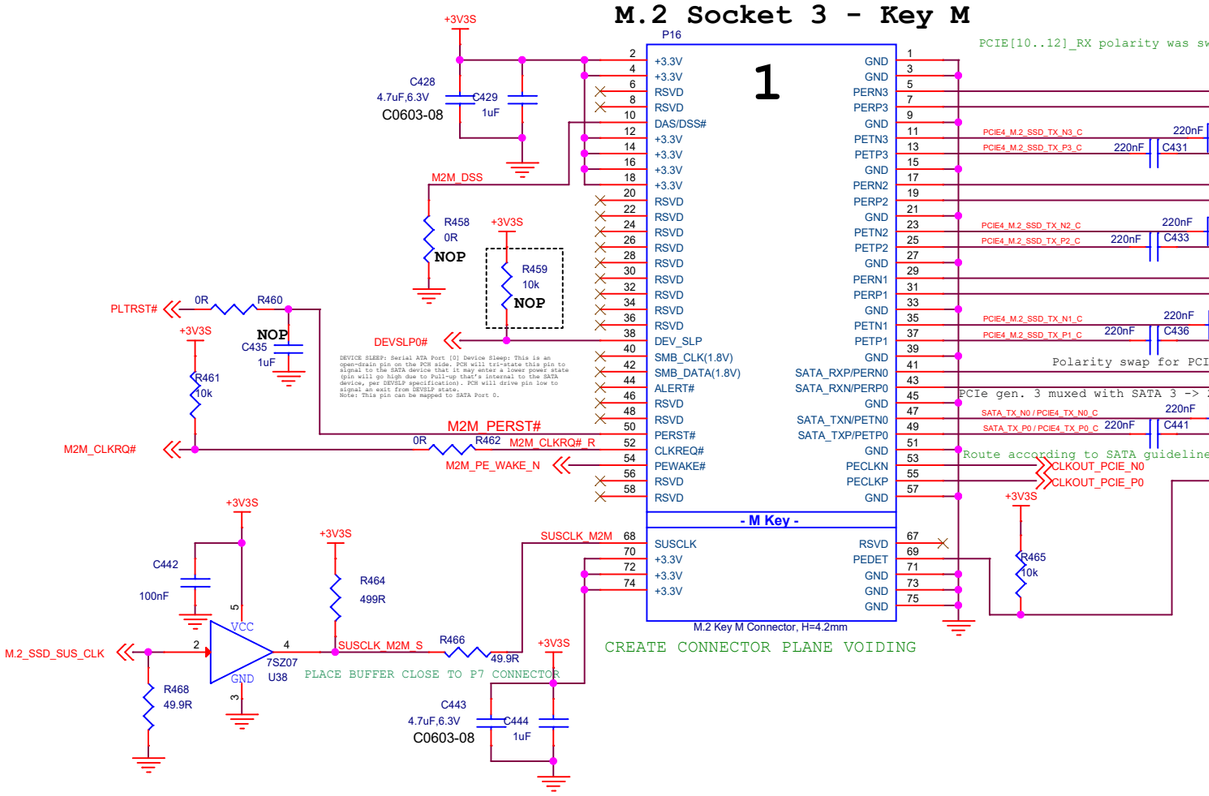
P 143/270 IN TL-SBC

980 PRO PCIe 4.0 NVMe M.2 250GB SSD

changed from H=4.2mm to H=6.7mm

changed from 182K06700S to 182K06706S

M.2 Socket 3 - Key M

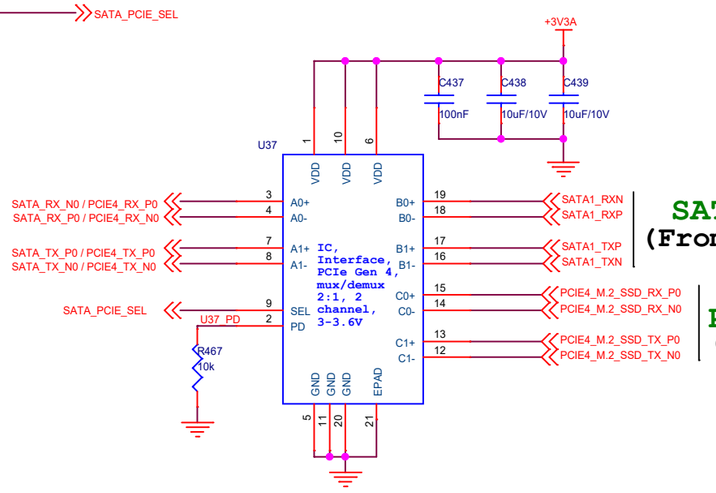


A PCIe* Lane is composed of a single pair of Transmit (TX) and Receive (RX) differential pairs, for a total of four data wires per PCIe* Lane (such as, PCIE[3]_TXP/ PCIE[3]_TXN and PCIE[3]_RXP/ PCIE[3]_RXN make up PCIe Lane 3). A connection between two PCIe* devices is known as a PCIe* Link, and is built up from a collection of one or more PCIe* Lanes which make up the width of the link (such as bundling 2 PCIe* Lanes together would make a x2 PCIe* Link). A PCIe* Link is addressed by the lowest number PCIe* Lane it connects to and is known as the PCIe* Root Port (such as a x2 PCIe* Link connected to PCIe* Lanes 3 and 4 would be called x2 PCIe* Root Port 3).

PCIE-GEN4

PCIe Gen4 : 16.0 GT/s = 1.969 GB/s (per plane)

SATA does not support signal polarity reversal and does not support lane reversal.



SATA #1 (From PCH)

PCIE-GEN4 (From CPU)

Title	M.2 M (SSD)		
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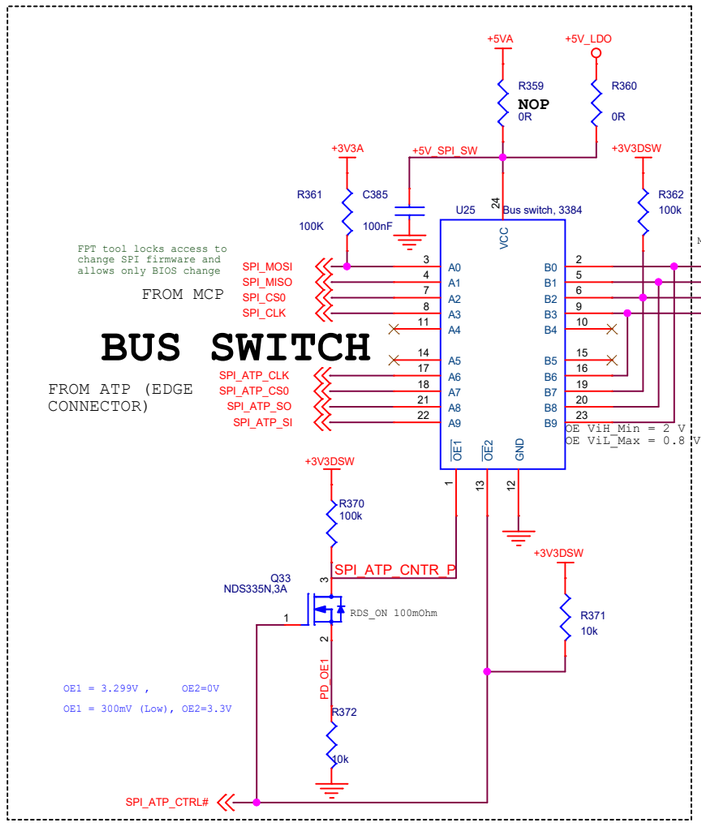
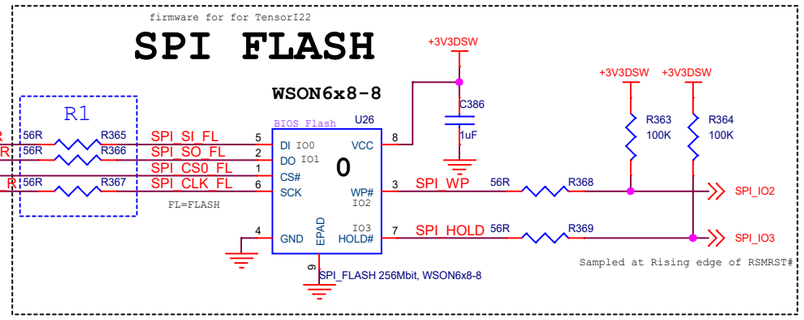
2-Load Branch MAF Topology (Master Attached Flash)

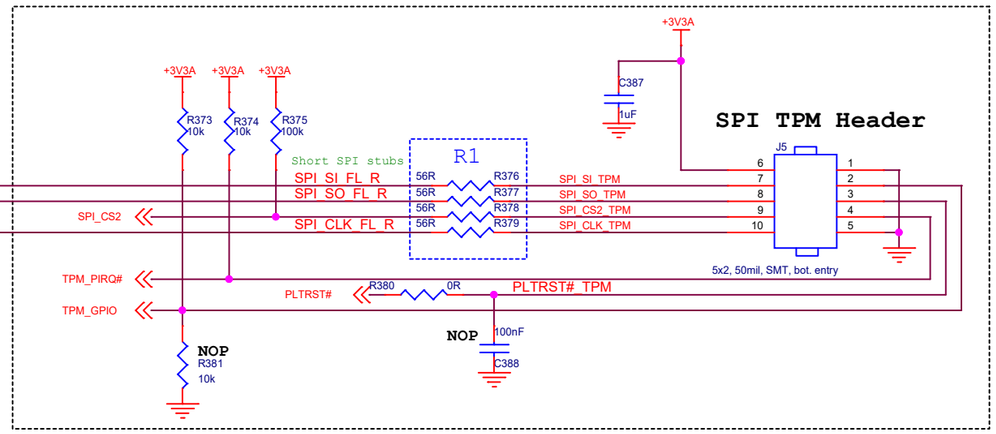
SPI_CLK & SPI_MOSI matched to within 500 mil
SPI_CLK & SPI_CS[0,1] matched to within 500 mil



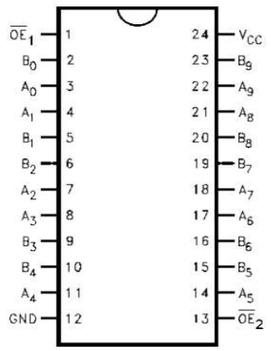
if SPI_ATP_CNTR# = 0V then SPI_ATP_CNTR_P = 3.299V
if SPI_ATP_CNTR# = 3.3V SPI_ATP_CNTR_P = 300mv < 0.8V (V_IL,MAX)



SPI_IO2 & SPI_IO3
External pull-up is required. Recommend 100 kohm if pulled up to 3.3 V or 75 kohm if pulled up to 1.8 V.
This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.



Connection Diagram



Truth Table

$\overline{OE}_1$	$\overline{OE}_2$	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

Title	SPI FLASH/TPM		
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I2C GPIO I/O Expander

U39 Internal 100K PU are enabled by default

PCA9555

Address: 0x40

Internal 100K PU are enabled by default
After power-up, the XRA1201 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled. The XRA1201P has the internal pull-up resistors enabled upon power-up in case it is necessary for the inputs to be in a known state.

the RIBBON ID are inputs to the GPIO EXPANDER, by default, these pins are 1 (internal 100K PU), untill a ground is connected to some Ribbon ID pin in TRIP (on TEL Side)

RN1 10K/8P4R Pull-Down

I2C Mux

U40 PCA9518 I2C HUB

from master

by default, the GPIO exapnder has internal pull up of 100K, which cases the EN pins to be 0.3V (becase of 10K pull down). 0.3 is lower than the ViL which is 0.5V.

74LVC08 (U42A, U42B, U42C, U42D)

NOTE: EEPROM ADRESS ON ALL TELS ARE THE SAME (0x54) BUT DATA THAT SPECIFIES THE PURPOSE OF EACH TEL IS DIFFERENT.

SMB_CLK_1 / SMB_DATA_1 | to Trip 1
EEPROM ADDRESS: 0x54

SMB_CLK_2 / SMB_DATA_2 | to Trip 2
EEPROM ADDRESS: 0x54

SMB_CLK_EB / SMB_DATA_EB | TO EB-TI22A (B2B)
EEPROM ADDRESS: 0x54
I210 Address: 0x49 (P.222)

EEPROM

U41 24C08 (1KB)
EEPROM ADDRESS: 0x54

Title	SMBus_MUX/GPIO_EXPANDER
Size	A3
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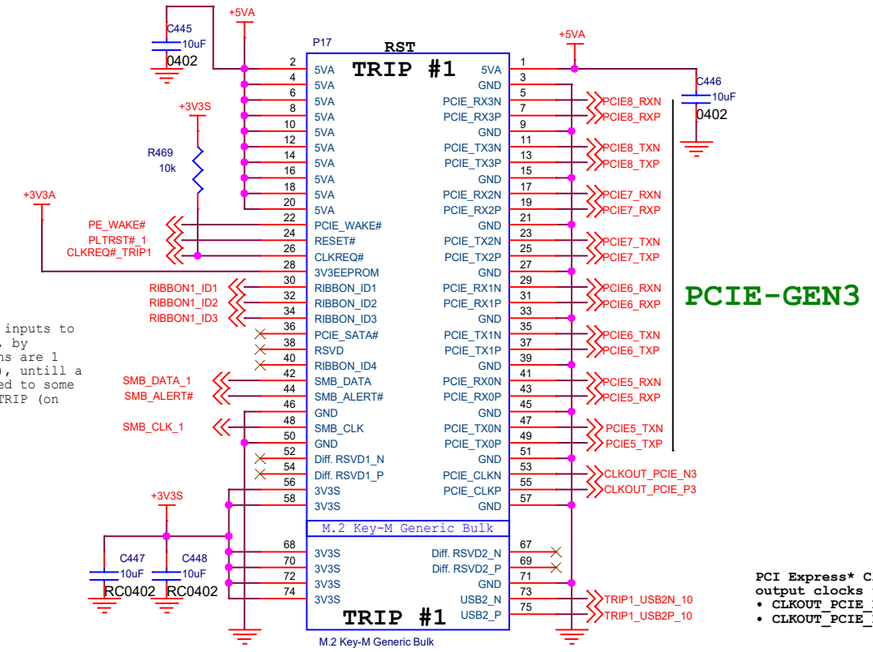
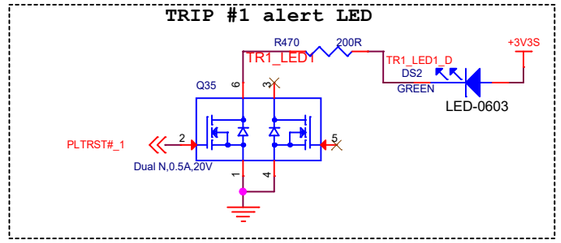
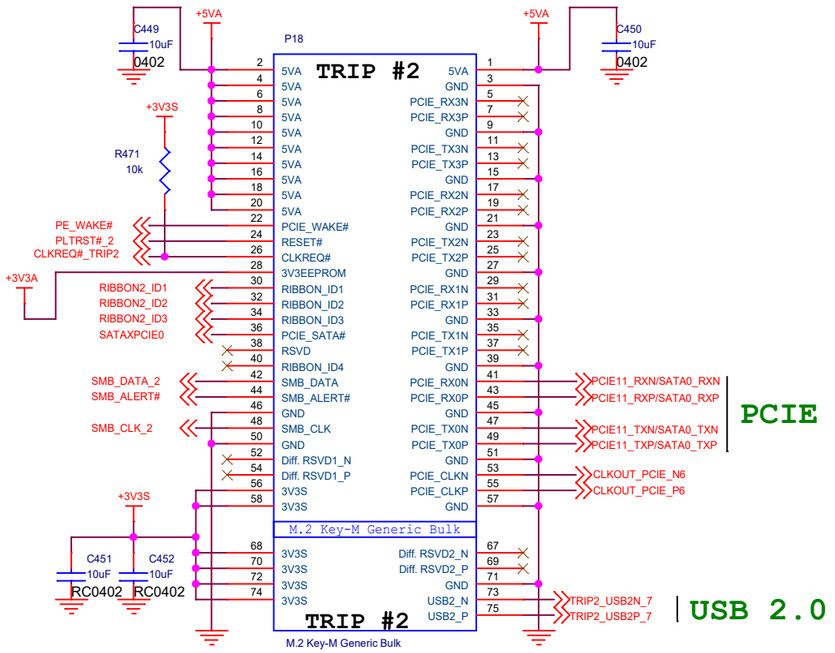


PCIE-GEN3

the RIBBON ID are inputs to the GPIO EXPANDER, by default, these pins are 1 (internal 100K PU), untill a ground is connected to some Ribbon ID pin in TRIP (on TEL Side)

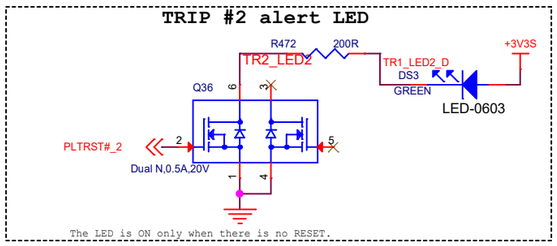


PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices
- **CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support**
- **CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support**



PCIE x1/SATA

USB 2.0



Title	TRIP 1&2		
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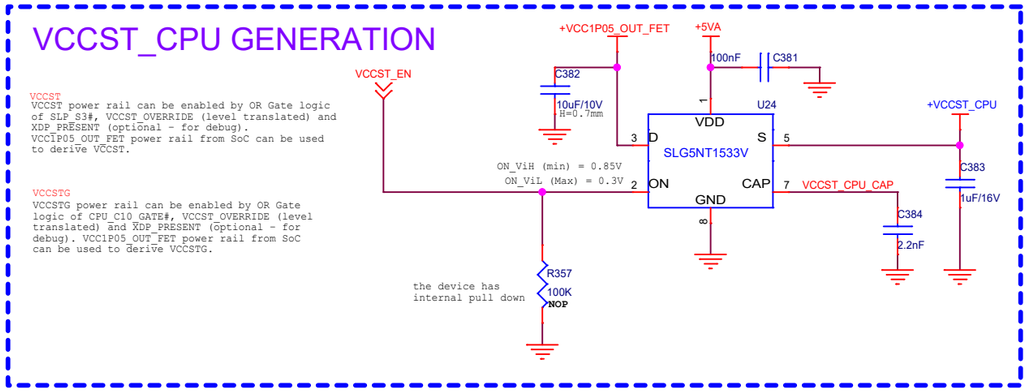
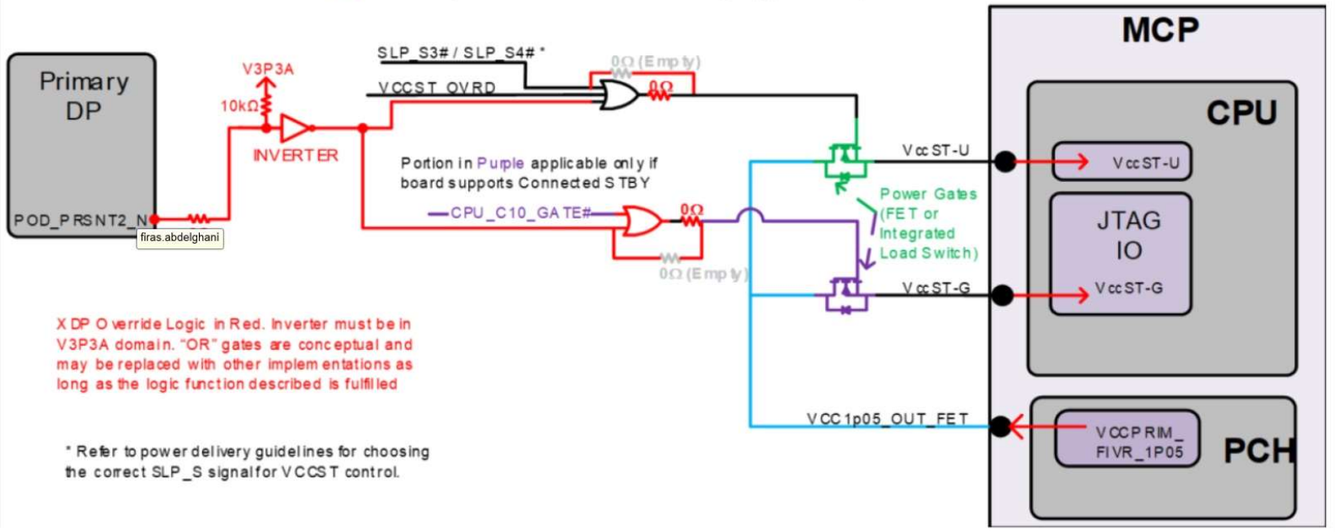


UN-IMPELEMNTED (VCCSTG_CPU & VCCST_CPU WERE MERGED TOGETHER):

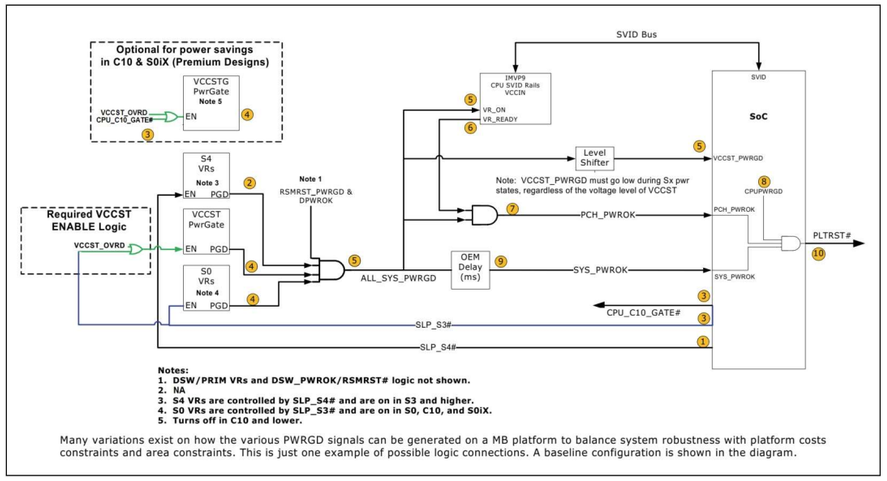
Concept of VccST/VccST-G Power Override Mechanism:
When the external debugger is plugged in, POD_PRSNT2_N will be driven to GND. VccST/VccST-G will be forced on in all Sx states to support PCH Sx open-chassis debug via JTAG without additional isolation logic. If S0-only open-chassis PCH debug is acceptable, then the override mechanism in red is not required unless CPU C10 debug support is required.



IN VOLUME: VccSTG gated by SLP_S3#

IN Premium, VccSTG gated by {CPU_C10_GATE#}

Figure 247. Premium PWROK Generation Flow Diagram



Many variations exist on how the various PWRGD signals can be generated on a MB platform to balance system robustness with platform costs constraints and area constraints. This is just one example of possible logic connections. A baseline configuration is shown in the diagram.

Title	<Title>	
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