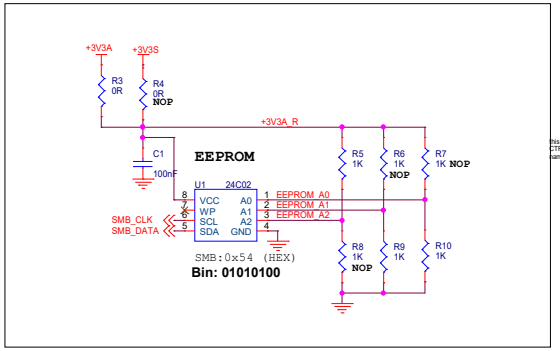
EB-TI22A

Display Interfaces

DDI Ports Availability

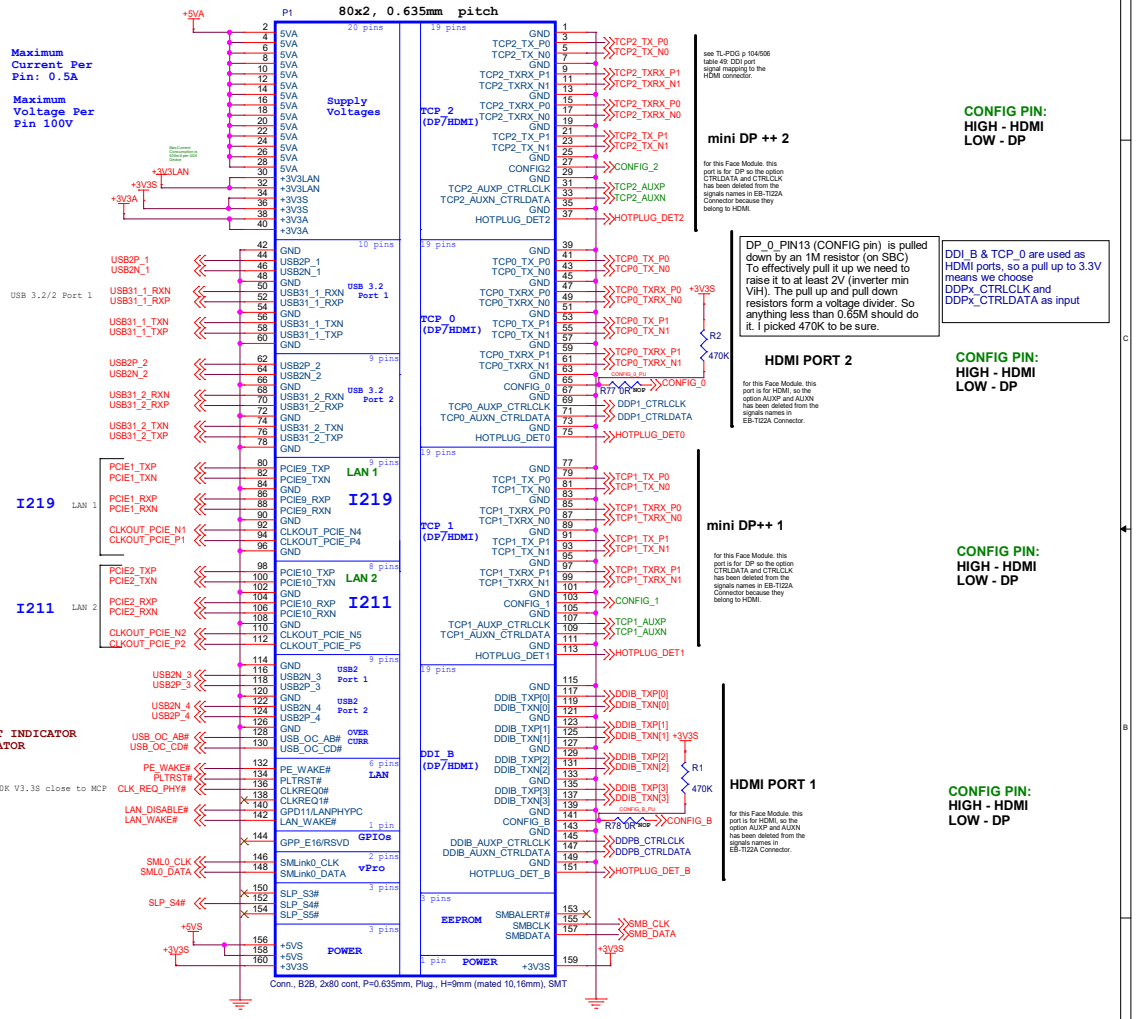
SKU	UP4 Processor Line	UP3 Processor Line
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	eDP*/DP*/HDMI*/MIPI_1	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*

Note: HBR3 supported on TCP ports only.
Each of the TCP port can support DPoC* (DisplayPort* over Type-C)



this connector is DP++, so we delete the CTRLCLK and CTRLDATA from the signal naming

Header



DP_0_PIN13 (CONFIG pin) is pulled down by an 1M resistor (on SBC) To effectively pull it up we need to raise it to at least 2V (inverter min ViH). The pull up and pull down resistors form a voltage divider. So anything less than 0.6SM should do it. I picked 470K to be sure.

DDI_B & TCP_0 are used as HDMI ports, so a pull up to 3.3V means we choose DDPx_CTRLCLK and DDPx_CTRLDATA as input

CONFIG PIN:
HIGH - HDMI
LOW - DP

CONFIG PIN:
HIGH - HDMI
LOW - DP

CONFIG PIN:
HIGH - HDMI
LOW - DP

ZZ1
P/N = 188Z10030
PARSER_VERSION_1.0

PCB1
PCB, EB-TI22A, Rev 1.0

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12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] DDIB_TXN[3:0]	**Digital Display Interface Transmit:** DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P DDIB_AUX_N	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

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Table 49. DDI Port Signal Mapping for HDMI*

Description	Signal Mapping	
	DDI	HDMI
Main Link (Tx)	DDI_TX0	HDMI Data_2
	DDI_TX1	HDMI Data_1
	DDI_TX2	HDMI Data_0
	DDI_TX3	HDMI CLK
Note: Apply to DDIA/B ports only		

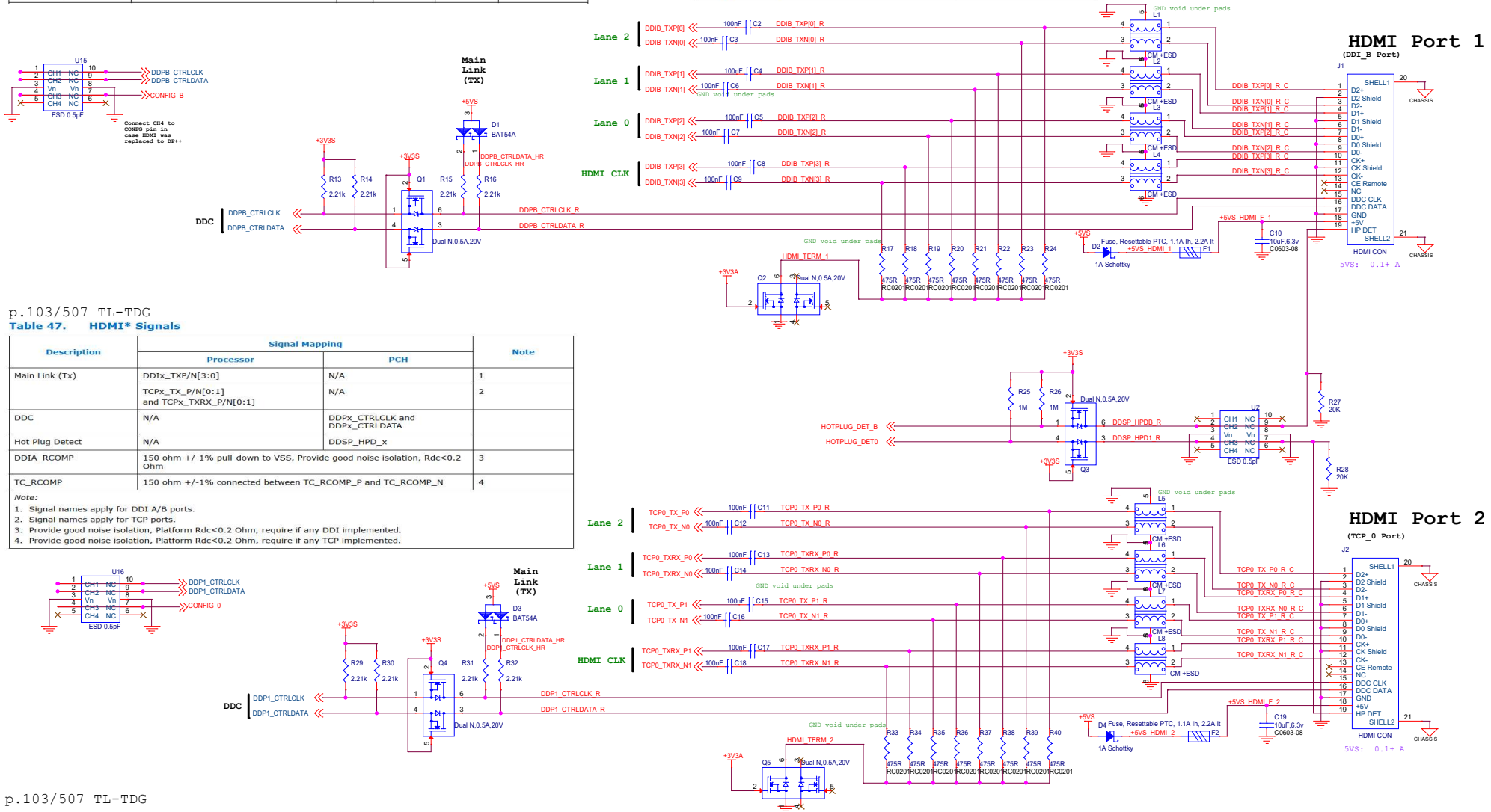

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Table 47. HDMI* Signals

Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx)	DDIx_TXP/N[3:0]	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	2
DDC	N/A	DDPx_CTRLCLK and DDPx_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

Note:
1. Signal names apply for DDI A/B ports.
2. Signal names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

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Table 48. TCP Port Signal Mapping for HDMI*

Description	Signal Mapping	
	TCP	HDMI
Main Link (Tx)	TCP_TX0	HDMI Data_2
	TCP_TX1	HDMI Data_0
	TCP_TXRX0	HDMI Data_1
	TCP_TXRX1	HDMI CLK
Note: Apply to TCP ports only.		

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Table 39. TCP Port Signal Mapping For DisplayPort*

Description	Signal Mapping	
	DDI	DP++
Main Link (Tx)	TCP_TX0	DP Lane_0
	TCP_TX1	DP Lane_2
	TCP_TXRX0	DP Lane_1
	TCP_TXRX1	DP Lane_3
Note: Apply to TCP ports only.		

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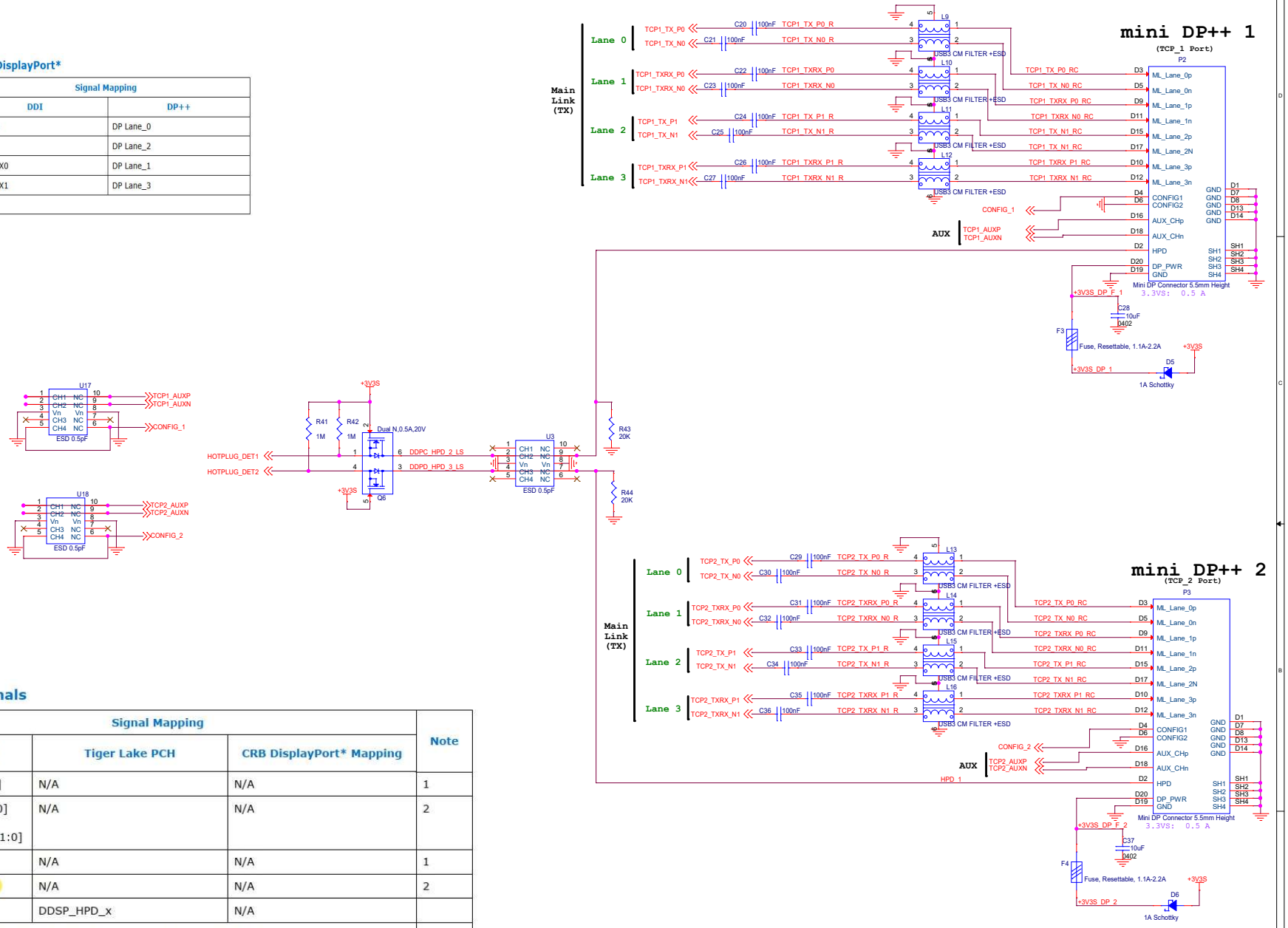
Table 38. DisplayPort* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx)	DDIx_TXP/N[3:0]	N/A	N/A	1
	TCPx_TX_P/N[1:0] and TCPx_TXRX_P/N[1:0]	N/A	N/A	2
Aux Channel	DDIx_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:

1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.



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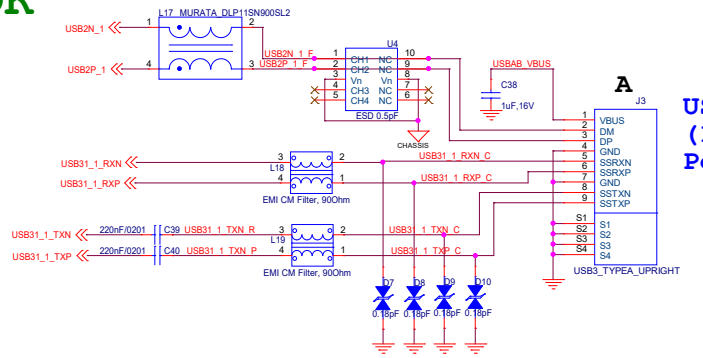
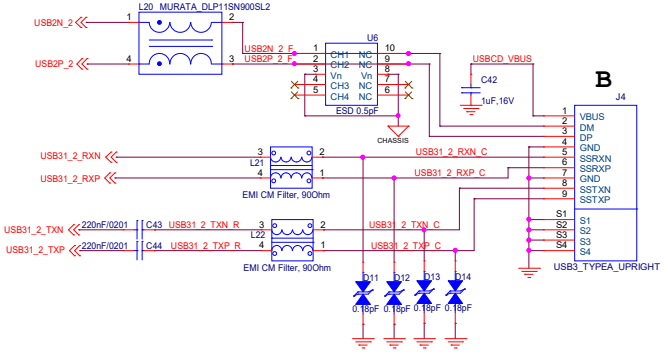


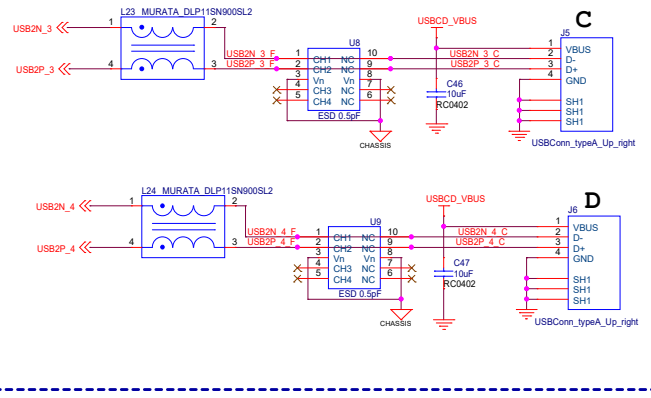
USB 3.1 Gen 2 (10 Gbps) Port 1

OK



USB 3.1 Gen 2 (10 Gbps) Port 2

OK

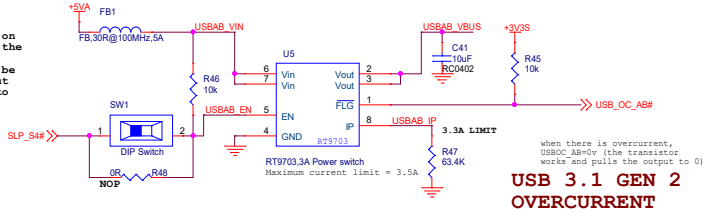


USB 2.0 CONN 1

USB 2.0 CONN 2

SW1 On -> USB A,B Turn off on S4# (when the pc on sleep). the reistor is there in case we don't want this function to be controlled by the switch. but when we want this function to ALWAYS work.

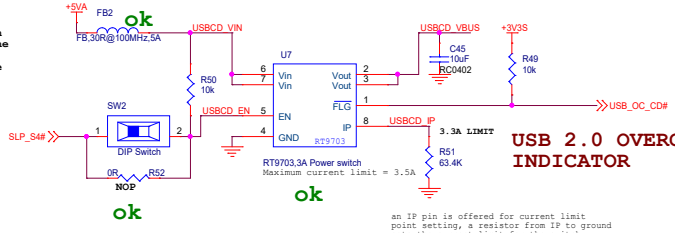
Instead of connecting Pin:1 to SLP signal that came back from TRIP, now it's connected to +3V3S



when there is overcurrent, USBOC_AB=0v (the transistor works and pulls the output to 0)

USB 3.1 GEN 2 OVERCURRENT INDICATOR

SW1 On -> USB C,D Turn off on S4# (when the pc on sleep). the reistor is there in case we don't want this function to be controlled by the switch. but when we want this function to ALWAYS work.



an IP pin is offered for current limit point setting, a resistor from IP to ground sets the current limit for the switch.

USB 2.0 OVERCURRENT INDICATOR

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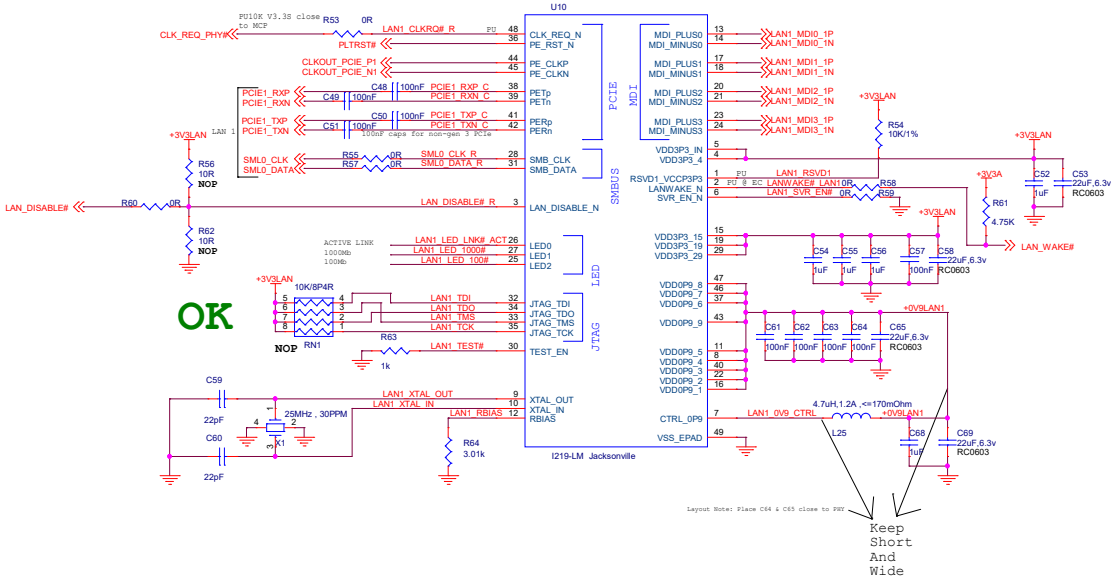
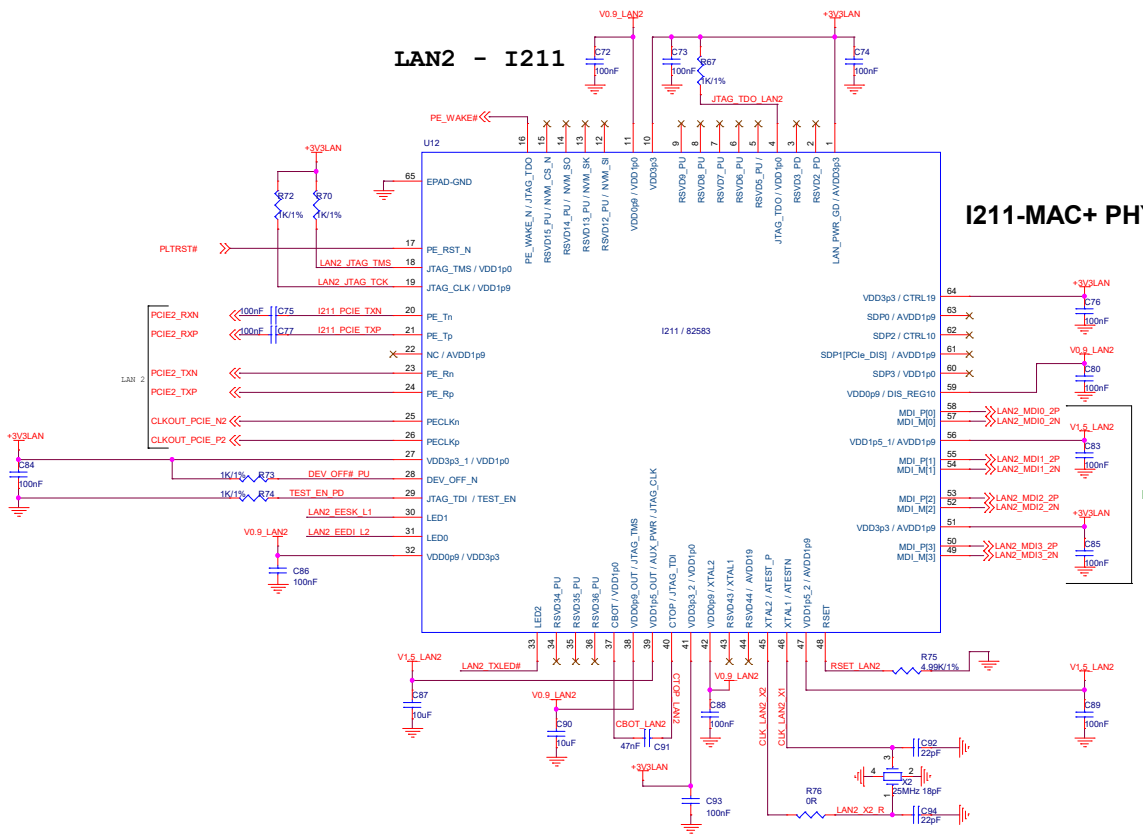
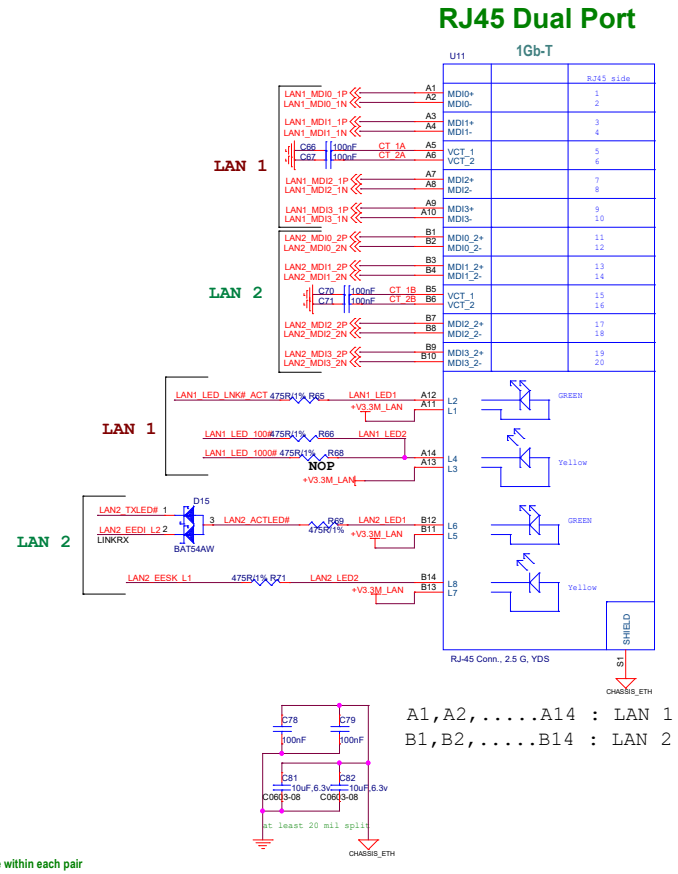
LAN1 - I219



LAN2 - I211



RJ45 Dual Port



A1,A2,.....A14 : LAN 1
B1,B2,.....B14 : LAN 2

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