

Manufacturing with the Intel® Platform Code Named Tiger Lake

Revision 2.5
Q1 2021

RDC: 613010



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Introduction

- This Manufacturing Advantage Services (MAS) course shares Intel manufacturing recommendations to facilitate our customer's manufacturing excellence.
- Tiger Lake Mobile Platform uses the Intel® Core™ Processor Lines:
 - Tiger Lake UP3
 - Tiger Lake H35 (TGL H 300 Series)
 - Tiger Lake UP4
 - Tiger Lake H81
 - Tiger Lake PCH-H

Package Change Notification: Starting with TGL UP3 & UP4 ES2 samples, the die thickness (not including C4 bumps) will increase from 170 to 270um and the stiffener thickness (not including adhesive) will decrease from 300 to 200um. This change will eliminate the need for a pedestal heatsink design starting at the ES2 phase. TGL UP3 & UP4 ES2 packages will also be marked on the metal stiffener with a human readable "270" mark, providing a visual indication of this change. (Refer to Section 4.1 for more details)

Revision History

- Revision 0.5:
 - Initial release
- Revision 1.0:
 - Updated for new UP3 and UP4 processor lines (removed U and Y)
 - Updated TGL UP3 PMD – 1.2
 - Added TGL UP3 dynamic warpage information – 3.2
 - Updated Cu Core Standoff Technology slide – 3.7
 - Added TGL UP3 4 mil stencil recommendation – 3.8
 - Added TGL UP3 5 mil stencil recommendation – 3.8
 - Added TGL UP3 thermocouple location recommendation – 3.10
 - Added TGL UP4 thermocouple location recommendation – 3.10
 - Added TGL UP3 package marking information – 4.1
 - Added TGL UP4 package marking information – 4.1
- Revision 1.5:
 - Updated TGL UP4 PMD – 1.2
 - Added TGL UP4 dynamic warpage information – 3.2
 - Added TGL UP4 3 mil stencil recommendation – 3.8
 - Added TGL UP4 4 mil stencil recommendation – 3.8
- Revision 1.6:
 - Updated TGL UP3 KOZ drawing – 2.2
- Revision 1.7:
 - Updated package change notification – Introduction
 - Updated TGL UP3 attributes table and package change notification – 1.1
 - Updated TGL UP3 PMD – 1.2
 - Updated TGL UP4 PMD notes – 1.2
 - Added TGL UP3 Foot Print Symbol file RDC# – 2.2
 - Updated TGL UP3 land pattern legend colors – 2.3
 - Updated TGL UP3 dynamic warpage information – 3.2
 - Updated TGL UP4 dynamic warpage notes – 3.2
 - Updated solder joint peak reflow temperature – 3.3
 - Updated TGL UP3 package marking reference information – 4.1

Revision History

- Revision 1.8:
 - Added ILN and RDC document numbers to title slide
 - Removed NCTF testing information
 - Updated table of contents
 - Updated TGL UP4 package attributes – 1.1
 - Updated TGL UP4 PMD – 1.2
 - Added land pattern guidance note to TGL UP3 – 2.3
 - Added land pattern guidance note to TGL UP4 – 2.3
 - Updated TGL UP4 dynamic warpage information – 3.2
 - Updated TGL UP4 3 mil stencil recommendation – 3.8
 - Updated TGL UP4 4 mil stencil recommendation – 3.8
 - Updated TGL UP4 package marking – 4.1
- Revision 1.9:
 - Added TGL PCH attributes table – 1.3
 - Added TGL PCH PMD – 1.4
 - Updated TGL UP4 RIMB/HIMB note – 2.2
 - Added TGL UP4 RIMB/HIMB Requirements slide – 2.2
 - Added TGL PCH land pattern (Mobile) – 2.3
 - Added TGL PCH land pattern (Desktop) – 2.3
 - Added Corner NCTF Solder Joint Testability Recommendation – 2.4
 - Added NCTF Implementation – Continuity/Resistance Test Threshold – 2.5
 - Added TGL UP3 NCTF routing information – 2.6
 - Added TGL UP4 NCTF routing information – 2.6
 - Added TGL PCH NCTF routing information – 2.6
 - Added TGL PCH dynamic warpage information – 3.2
 - Added TGL PCH 4 mil stencil recommendation – 3.8
 - Added TGL PCH 5 mil stencil recommendation – 3.8
 - Added TGL PCH thermocouple location recommendations – 3.10
 - Added TGL PCH package marking – 4.1
 - Added TGL PCH shipping media information – 4.2
 - Updated Tray Package Handling BKMs Additional References - 4.4.8
 - Added Tape and Reel Package Handling BKMs – 4.5
 - Added TGL FW Test Information Reference – 5.1
 - Updated reference documents table – 7.1

Revision History

- Revision 2.0:
 - Corrected NCTF information for TGL UP3 in attributes table – 1.1
 - Updated TGL UP3 land pattern design note to final – 2.3
 - Updated TGL UP3 dynamic warpage information – 3.2
 - Updated TGL UP3 4 mil stencil recommendation – 3.8
 - Updated TGL UP3 5 mil stencil recommendation – 3.8
 - Added additional notes and corner glue video link to board level adhesive overview – 3.12
 - Added TGL UP3, TGL UP4 and TGL PCH rework recommendations – 3.13
 - Updated System Integration & ESD Considerations Introduction wording - 6.1
 - Updated TGL UP3 ESD test results – 6.2
- Revision 2.1:
 - Updated introduction sentence and added TGL H81 – Introduction
 - Added TGL H81 attributes table – 1.1
 - Added TGL H81 PMD – 1.2
 - Added TGL H81 motherboard cavity voiding requirements – 2.2
 - Updated TGL UP4 land pattern design note to final – 2.3
 - Added TGL H81 land pattern guidance – 2.3
 - Added TGL H81 NCTF routing information – 2.6
 - Added TGL H81 dynamic warpage information – 3.2
 - Updated SMT parameters table to include note regarding TGL UP4 – 3.3
 - Updated TGL UP4 3 mil stencil recommendation – 3.8
 - Updated TGL UP4 4 mil stencil recommendation – 3.8
 - Added TGL H81 4 mil stencil recommendation – 3.8
 - Added TGL H81 5 mil stencil recommendation – 3.8
 - Added TGL H81 thermocouple location recommendation – 3.10
 - Added TGL UP4 adhesive application guidance – 3.12
 - Added TGL processor line adhesive recommendations for IOTG applications – 3.12
 - Updated Rework Process Parameter Recommendations table and reflow profile graphic – 3.13
 - Updated TGL UP3 metal stiffener '270' marking information – 4.1
 - Updated TGL UP4 metal stiffener '270' marking information – 4.1
 - Added TGL H81 package marking – 4.1
 - Added TGL H81 tray information – 4.2
 - Updated reference documents – 7.1

Revision History

■ Revision 2.2:

- Updated document format
- Removed ES1 sample information from document
- Changed 'UP3' to 'UP3/H35' throughout document
- Added TGL H35 – Introduction
- Removed Heatsink Pedestal Row from attributes table
- Updated attributes table to single slide – [1.1](#)
- Updated TGL H81 column to include Cu Core standoffs solder ball information and SLI bottom to top of stiffener dimension – [1.1](#)
- Removed Heatsink Pedestal Row from attributes table
- Removed "This PMD is for ES2 and onward" from TGL UP3 and TGL UP4 PMD slides
- Updated TGL UP3/H35 Cu Core Standoff Location slide title – [1.2](#)
- Updated TGL H81 PMD – [1.2](#)
- Added TGL H81 Cu Core ball locations slide – [1.2](#)
- Corrected TGL H81 notes wording – [2.3](#)
- Updated Cu Core Technology Slide – [3.7](#)
- Added reflow ambient recommendation note to TGL UP4 stencil slides – [3.8](#)
- Changed TGL UP3/H35 stencil recommendation table from "BGA Long Edge Pads" to "BGA Pads" – [3.8](#), [3.13](#)
- Added Considerations for Corner Glue Removal – [3.13](#)
- Added TGL H81 rework information – [3.13](#)
- Updated rework thermocouple location recommendations for TGL UP3/H35, TGL UP4 and TGL PCH – [3.13](#)
- Updated rework process parameters table – [3.13](#)
- Updated rework profile recommendation slide – [3.13](#)
- Updated How Customers Access documents from ILN, RDC and VIP slides – [7.2-7.4](#)

■ Revision 2.3:

- Added TGL H PCH Symbol Kit to TGL PCH (Mobile) land pattern notes and updated land pattern note to final – [2.3](#)
- Corrected land pattern recommendations table for TGL PCH (Desktop) and updated land pattern note to final – [2.3](#)
- Added FACR Preparation Process – [3.14](#)

Revision History

■ Revision 2.4:

- Updated TGL H81 header from "H81 ES2" to "H81 ES2 to PRQ" – [1.1](#)
- Updated TGL H PMD – [1.2](#)
- Added Board Enabling Platform (BEP) to acronyms table – [Module 2](#)
- Updated TGL H land pattern to final – [2.3](#)
- Corrected TGL PCH NCTF Routing Example Title – [2.6](#)
- Updated TGL H dynamic warpage – [3.2](#)
- Corrected TGL PCH warpage table title – [3.2](#)
- Removed stiffener behavior note from TGL PCH dynamic warpage slide – [3.2](#)
- Updated Critical SMT Recommendations table symbols from “<” to “≤” – [3.3](#)
- Updated reflow ambient note symbol from “<” to “≤” on TGL UP4 3mil stencil – [3.8](#)
- Updated reflow ambient note symbol from “<” to “≤” on TGL UP4 4mil stencil – [3.8](#)
- Added Zymet UA-2605-B* to TGL UP4 adhesive application – [3.12](#)
- Corrected TGL H81 Rework Thermocouple Location Recommendation Title and table – [3.13](#)
- Updated TGL ESD test results table foot note to include TGL PCH – [6.2](#)

■ Revision 2.5:

- Removed TGL MAS document ILN numbers
- Added Die Side Capacitors “400um max height” wording to TGL PCH attributes table – [1.3](#)
- Updated TGL PCH PMD by correcting the DSC thickness from 0.25 Max to 0.4 Max – [1.4](#)



Page Markings and Navigation Aids

Click on the house to go to a Table of Contents page.

| | | | | | | |
|---|--|--|---|---|---|--|
| Module 1: Component Attributes and Drawings | Module 2: Land Pattern (PCB Pad) Design Guidelines | Module 3: Manufacturing Guidelines | Module 4: Shipping & Handling | Module 5: Testing | Module 6: System Integration & ESD Considerations | Module 7: References |
| 1.1 Package Attributes Intel® FCBGA Processors 1.2 Package Mechanical | 2.1 Land Pattern Design Guidelines Introduction 2.2 Mother Board Cavity | 3.1 Introduction 3.2 Example Package Dynamic Warpage Data | 4.1 Processor and Chipset Package Markings | 5.1 Test Information | 6.1 Introduction 6.2 Electro Static Discharge (ESD) | 7.1 Reference Documents 7.2 Intel® Learning |

These headers are links to modules.

Module 1: Component Attributes and Drawings

Manufacturing with the Intel® Platform Code Named Tiger Lake

Overview – Table of Contents

| | | | | | | |
|---|---|---|--|--|--|---|
| Module 1: <u>Component Attributes and Drawings</u> 1.1 Package Attributes Intel® FCBGA Processors 1.2 Package Mechanical Drawings (PMD) FCBGA Processors 1.3 Package Attributes PCH 1.4 Package Mechanical Drawings (PMD) PCH | Module 2: <u>Land Pattern (PCB Pad) Design Guidelines</u> 2.1 Land Pattern Design Guidelines Introduction 2.2 Mother Board Cavity Voiding Requirements 2.3 Land Pattern Design Guidelines (for the different processors & chipset) | Module 3: <u>Manufacturing Guidelines</u> 3.1 Introduction 3.2 Example Package Dynamic Warpage Data 3.3 Critical SMT Recommendations 3.4 Manufacturing Guidelines General Info 3.5 Solder Paste Formulation Optimization 3.6 Solutions to Extend Stencil Aperture Area Ratio 3.7 Cu Core Standoff Technology 3.8 Solder Paste Volume Optimization Stencil Design Recommendations 3.9 SMT Reflow Pallet Recommendations 3.10 SMT Reflow Profile TC Location 3.11 Overview of Board Flexure 3.12 Board Level Adhesive Overview 3.13 Package Rework 3.14 FACR Prep Process | Module 4: <u>Shipping & Handling</u> 4.1 Processor and Chipset Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements 4.4 BGA Package Handling BKMs 4.5 T&R Package Handling BKMs | Module 5: <u>Testing</u> 5.1 Test Information | Module 6: <u>System Integration & ESD Considerations</u> 6.1 Introduction 6.2 Electro Static Discharge (ESD) Platform Component Goals 6.3 Electro Static Discharge (ESD) Design Guidelines 6.4 Electro Static Discharge (ESD) Additional Resources 6.5 Thermal Solution Assembly / Disassembly considerations | Module 7: <u>References</u> 7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Resource Design Center access Information |
|---|---|---|--|--|--|---|



Acronyms Found in this Module

| | |
|-------|---|
| Cu | Copper |
| CuOSP | Copper Organic Solderability Preservative |
| EDS | External Design Specification |
| FCBGA | Flip-Chip Ball Grid Array |
| HIMB | Hole In Mother Board |
| HT | High Temperature |
| MAS | Manufacturing Advantage Service |
| MB | Mother Board |
| MSL | Moisture Sensitivity Level |
| NCTF | Non-Critical to Function |
| PCH | Platform Control Hub |
| PDS | Product Datasheet |
| PMD | Package Mechanical Drawing |
| RIMB | Recess In Mother Board |
| RT | Room Temperature |
| T&R | Tape and Reel |
| TFT | Thermoform Tray |



1.1 Package Attributes

| Attribute | Tiger Lake Processors | | |
|---|---|--|---|
| | UP3/H35 (4C+GT2) | UP4 (4C+GT2) | H81 ES2 to PRQ (8C+GT1) |
| Package Size (mm) | 45.5 x 25 | 26.5 x 18.5 | 50 x 26.5 |
| Solder Ball Material | SAC405 SAC305 (Cu Core Standoffs) | SAC405 | SAC405 SAC305 (Cu Core Standoffs) |
| Surface Finish | NiPdAu | NiPdAu | NiPdAu |
| Ball Count | 1449 | 1598 | 1787 |
| Min Ball Pitch (mm) | 0.65 | 0.40 | 0.65 |
| Ball Diameter (Pre-attach) (um/mil) | 406 / 16 (SAC405 balls) 340 / 13.4 (Cu Core Standoffs) | 229 / 9 | 406 / 16 (SAC405 balls) 340 / 13.4 (Cu Core Standoffs) |
| Pre-SMT z-Height (SLI bottom to die top) (mm) | 1.185 ± 0.096 | 0.963 ± 0.077 | 1.41 ± 0.109 |
| Assumes Zero Package Warpage | | | |
| Pre-SMT z-Height (SLI bottom to stiffener top) (mm) | 1.100 ± 0.101 | 0.878 ± 0.08 | 1.325 ± 0.111 |
| Assumes Zero Package Warpage | | | |
| Post-SMT z-Height | Customer's SMT process & materials affect Post-SMT Z-height. If needed, customers should measure Post-SMT Z-heights on actual product. | | |
| Land Side Capacitor | Yes (250um max height) | Yes (250um max height) | Yes (250um max height) |
| Die Side Capacitor | No | No | No |
| Separate Chipset | No | No | Yes |
| Die Configuration | Multi-Chip Package | Multi-Chip Package | Single Chip Package |
| | 2 dice | 2 dice | 1 die |
| CPU Die Size (mm) | 13.3 x 10.6 | 13.3 x 10.6 | 18.934 x 10.58 |
| 2nd Die Size (mm) | 9.2 x 5.8-PCH | 9.2 x 5.8-PCH | N/A |
| Die Thickness + C4 bumps (um) | CPU: 305 (270 w/out bumps) PCH: 305 (263 w/out bumps) | CPU: 305 (270 w/out bumps) PCH: 305 (263 w/out bumps) | 405 (370 w/out bumps) |
| Substrate thickness (um) | 594±0.08 | 514±0.08 | 719±0.095 |
| NCTF Corner Balls | 11/Corner, 9 at A1 Corner | 8-9/Corner, 14 at A1 Corner | 11/Corner, 9 at A1 Corner |
| PCB Type | Type 3 | Type 4 Only (HDI) | Type 3 |
| Stiffener | Yes | Yes | Yes |
| Stiffener + Adhesive Thickness (um) | 220 | 220 | 320 |
| Hole, Recess or Cavity Void in MB | Yes-Top Cu Layer Cavity & PTH/via Void in MB | Yes-HIMB (with FIVR EMI Shield) or RIMB (Depth: 232+-50um for SAC Reflow Process) Required | Yes-Top Cu Layer Cavity & PTH/via Void in MB |
| Shipping Media | TFT (Soft Tray) | TFT (Soft Tray) | TFT (Soft Tray) |

Package Change Notification: Starting with TGL UP3 & UP4 ES2 samples, the die thickness (not including C4 bumps) will increase from 170 to 270um and the stiffener thickness (not including adhesive) will decrease from 300 to 200um. This change will eliminate the need for a pedestal heatsink design starting at the ES2 phase. **TGL UP3 & UP4 ES2 packages will also be marked on the metal stiffener with a human readable "270" mark, providing a visual indication of this change.** (Refer to Section 4.1 for more details)

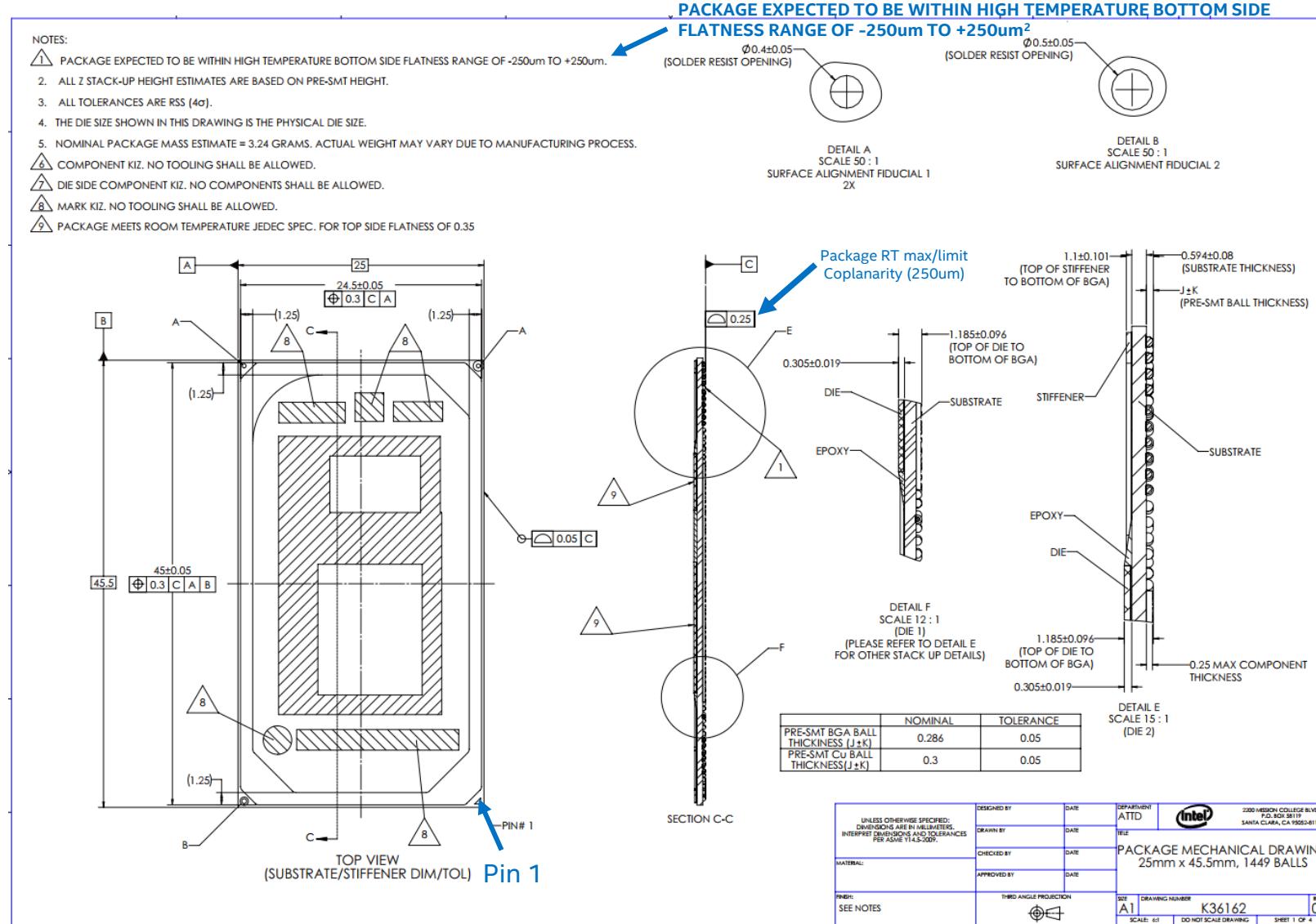
Notes:

- All components are halogen free FCGBAs with a max temp rating of 260°C
- Informational only: Refer to Tiger Lake Mobile Processor - EDS & PDG



1.2 Package Mechanical Drawing

Tiger Lake UP3/H35¹ 45.5x25mm (page 1 of 4)



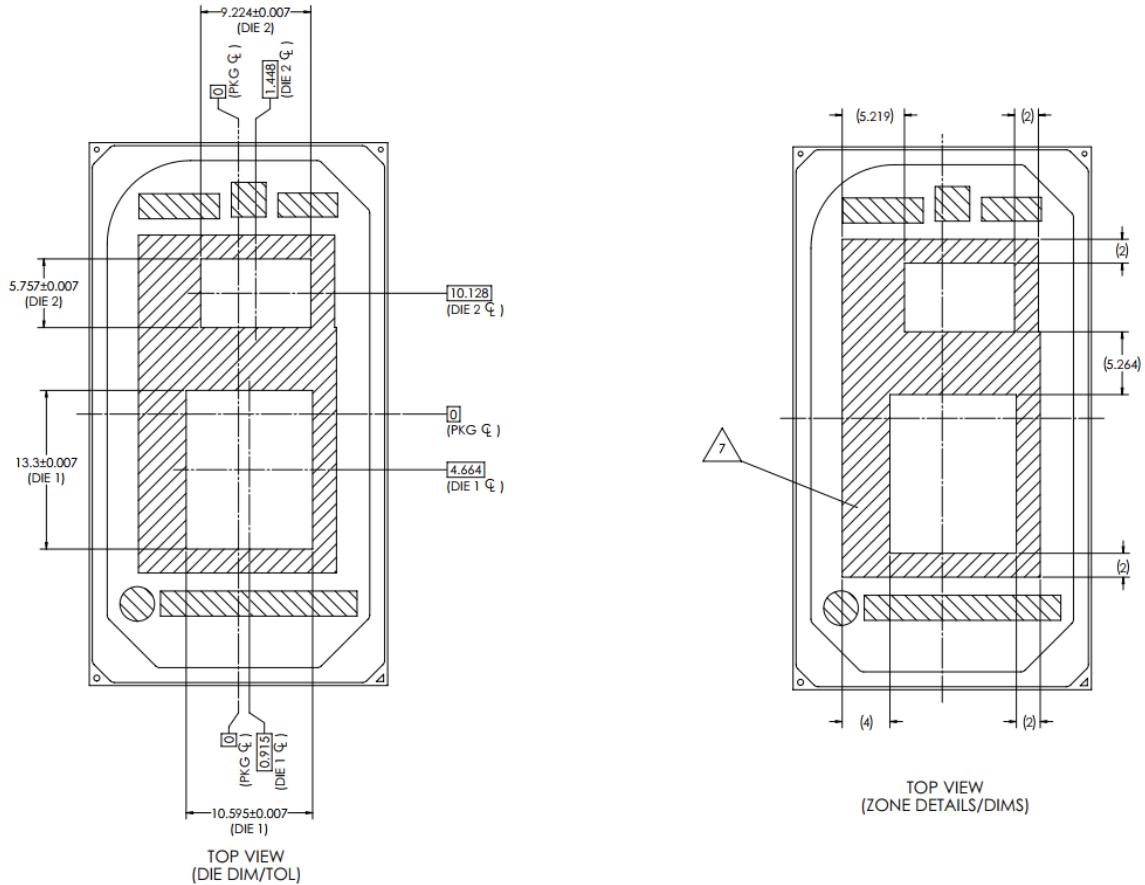
Notes:

- ¹This will be referred to as TGL UP3/H35 in this document.
- ²Between lowest active temperature of the board paste to peak reflow temperature.
- Package Mechanical Drawing (PMD) # K36162, Rev 02



1.2 Package Mechanical Drawing

Tiger Lake UP3/H35¹ 45.5x25mm (page 2 of 4)



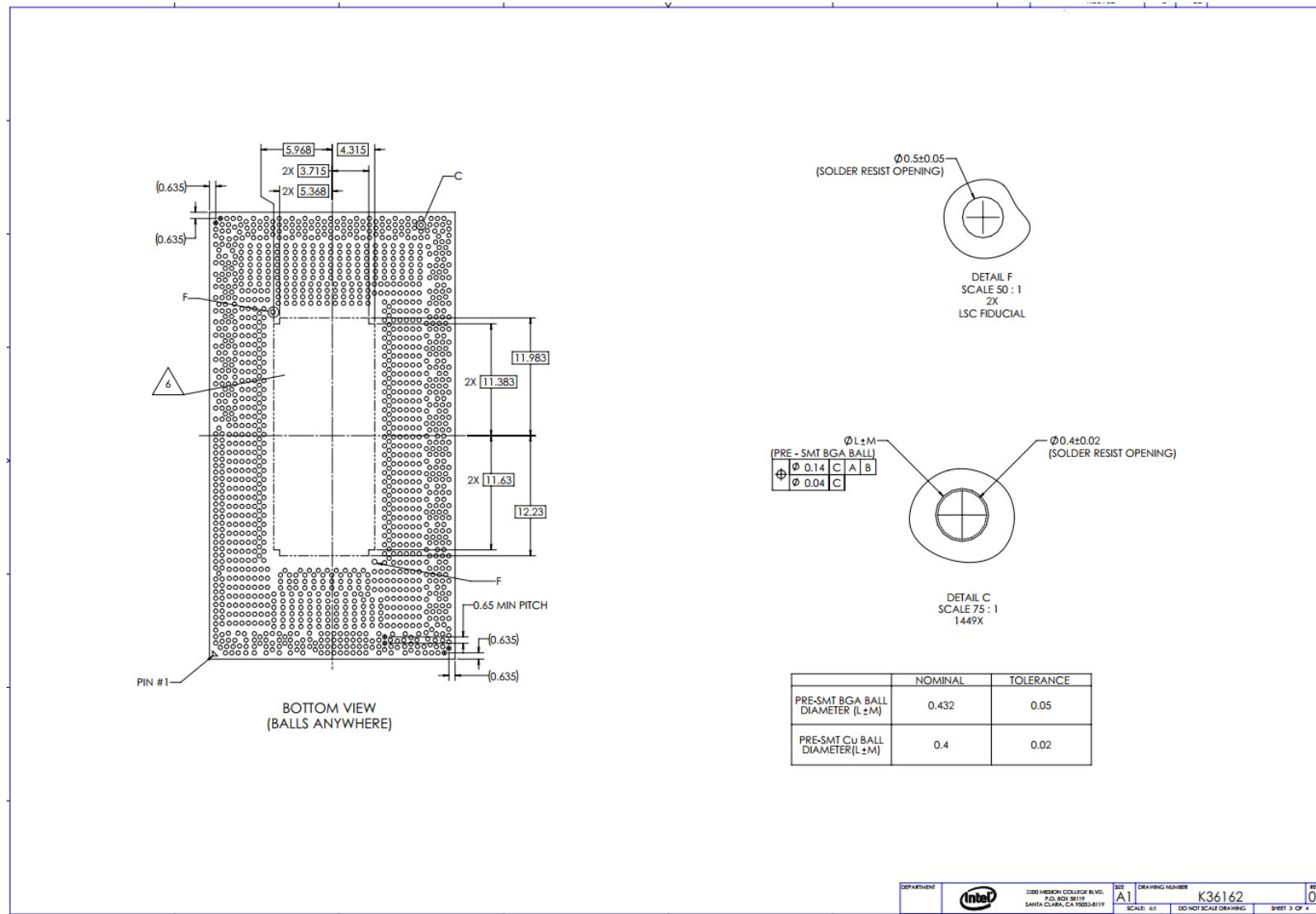
Notes:

- ¹This will be referred to as TGL UP3/H35 in this document.
- Package Mechanical Drawing (PMD) # K36162, Rev 02

| | | | | |
|------------|---|------|----------------|-----|
| DEPARTMENT | 5200 MISION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95051-8119 | SIZE | DRAWING NUMBER | REV |
| Intel | | A1 | K36162 | 02 |

1.2 Package Mechanical Drawing

Tiger Lake UP3/H35¹ 45.5x25mm (page 3 of 4)



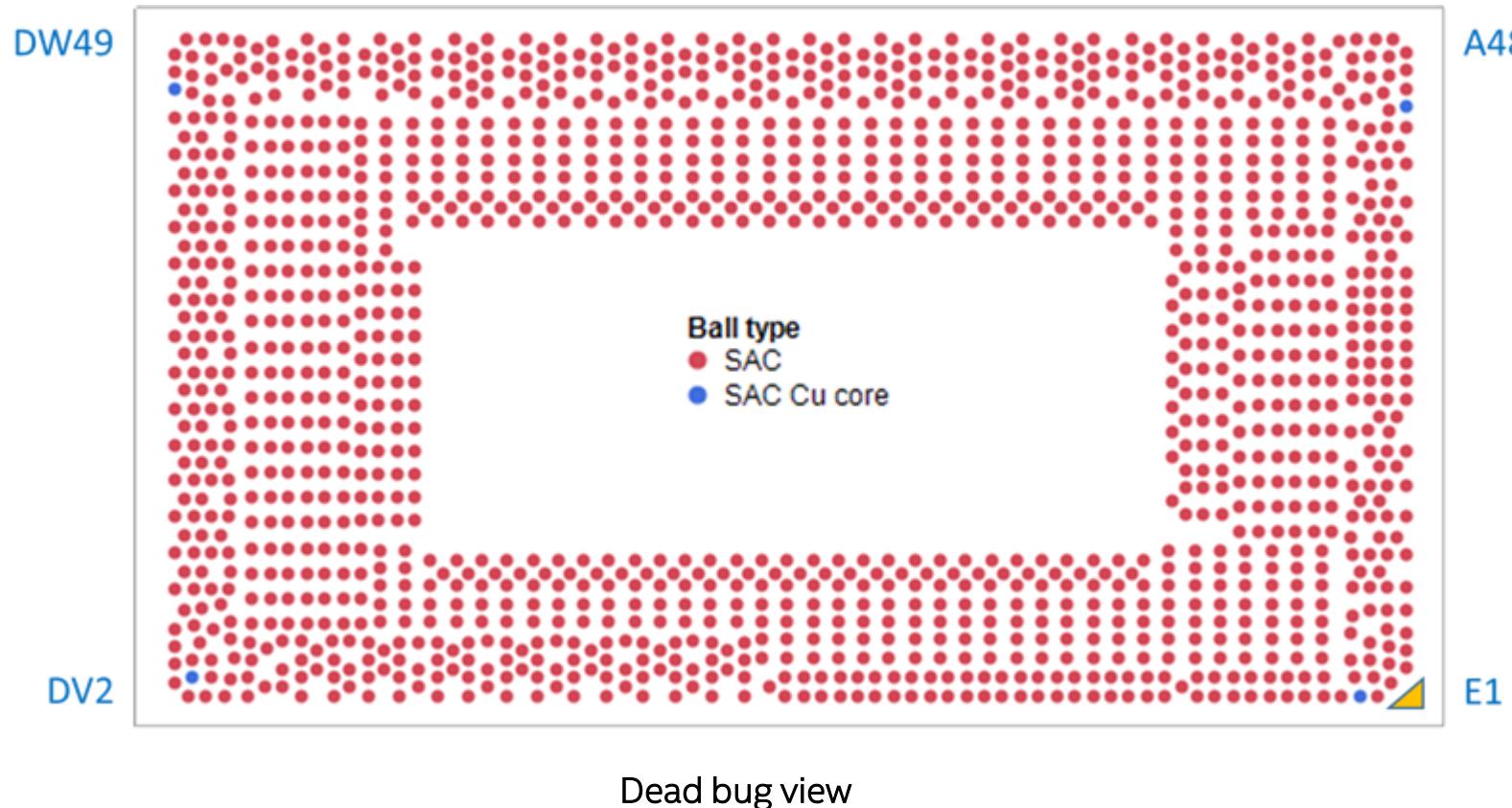
Notes:

- ¹This will be referred to as TGL UP3/H35 in this document.
 - Package Mechanical Drawing (PMD) # K36162, Rev 02



1.2 Cu Core Standoff Locations

Tiger Lake UP3/H35¹

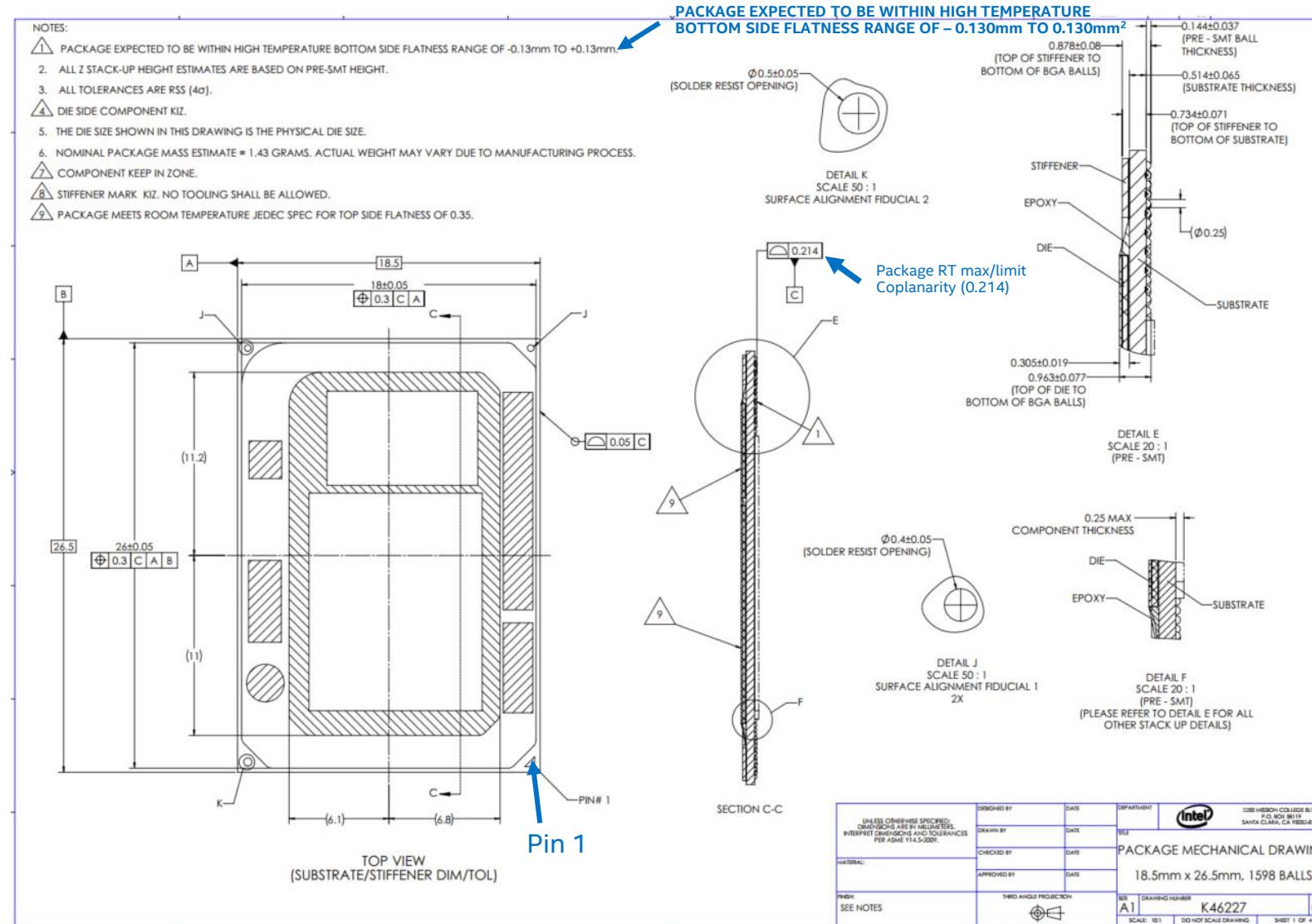


Notes:

- ¹This will be referred to as TGL UP3/H35 in this document.
- This is the Copper Core Standoffs locations drawing

1.2 Package Mechanical Drawing

Tiger Lake UP41 26.5 x 18.5mm (page 1 of 3)



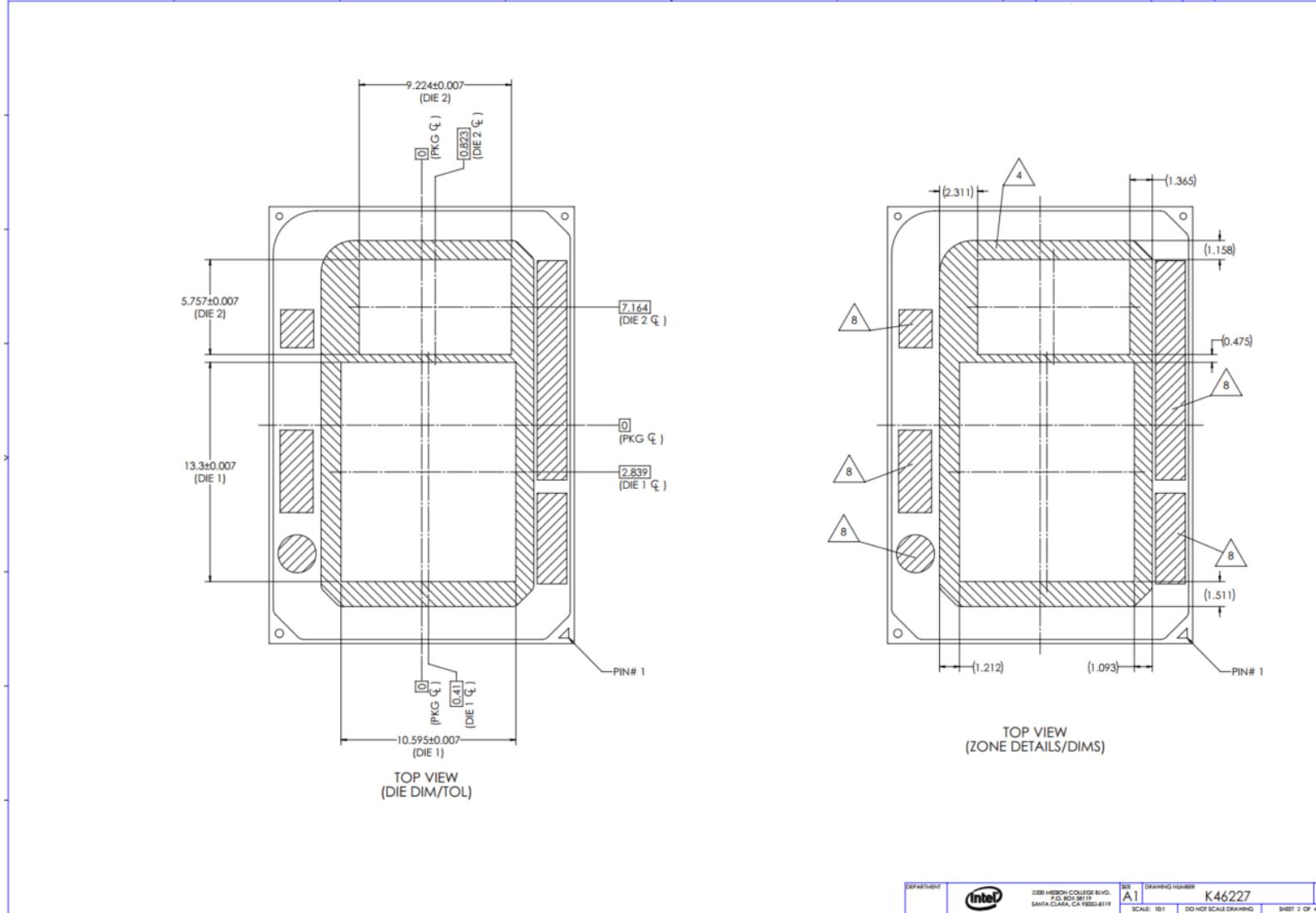
Notes:

- ¹This will be referred to as TGL UP4 in this document.
 - ²Between lowest active temperature of the board paste to peak reflow temperature.
 - Package Mechanical Drawing (PMD) # K46227, Rev 03



1.2 Package Mechanical Drawing

Tiger Lake UP4¹ 26.5 x 18.5mm (page 2 of 3)

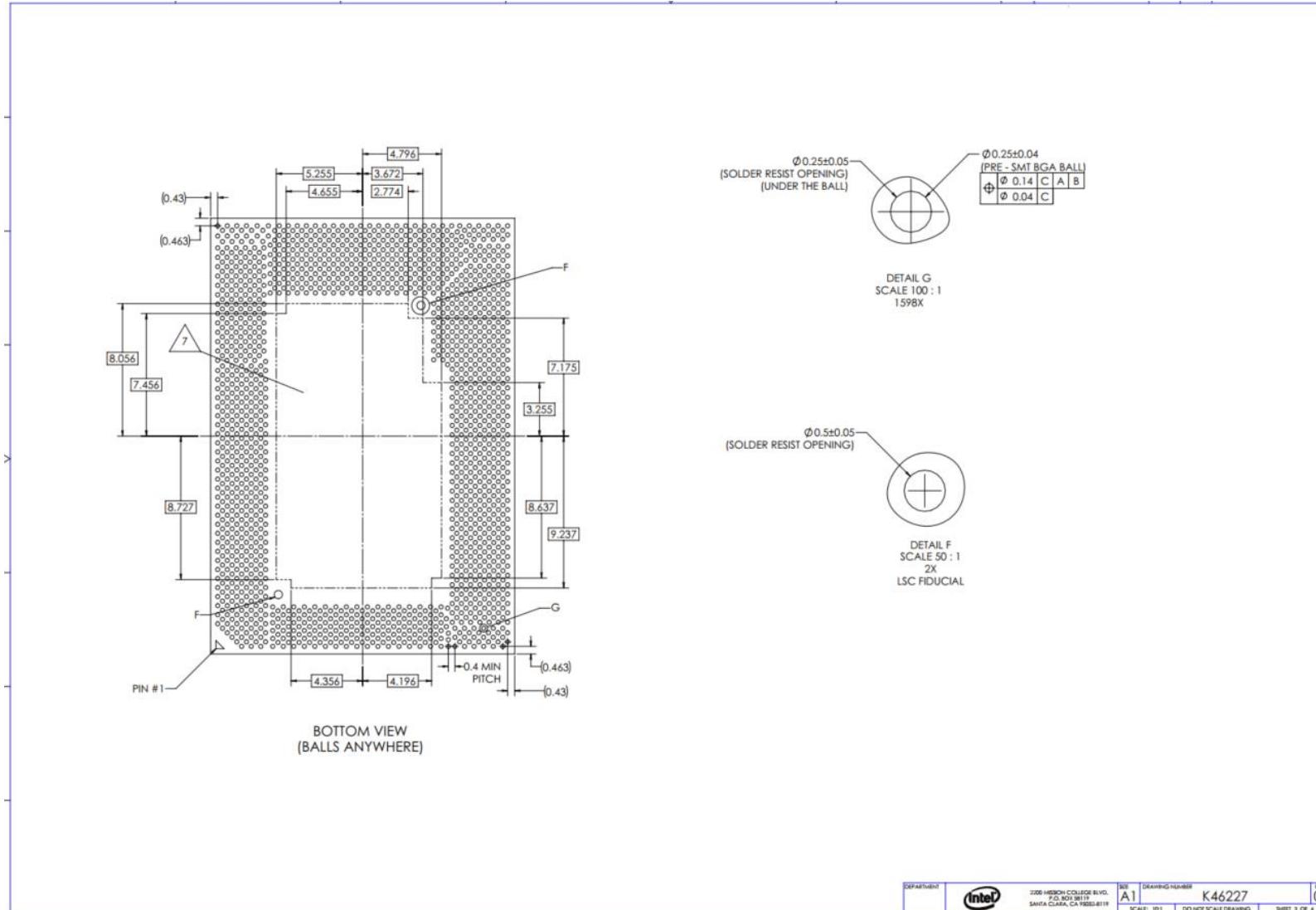


| | | |
|------------|--|--|
| DEPARTMENT | 2000 HERCION COLLEGE BLVD. P.O. BOX 36119 SANTA CLARA, CA 95061-0119 | REV. 03 |
| A1 | DRAWING NUMBER K46227 | SCALE: 101 DO NOT SCALE DRAWING SHEET 2 OF 4 |



1.2 Package Mechanical Drawing

Tiger Lake UP4¹ 26.5 x 18.5mm (page 3 of 3)



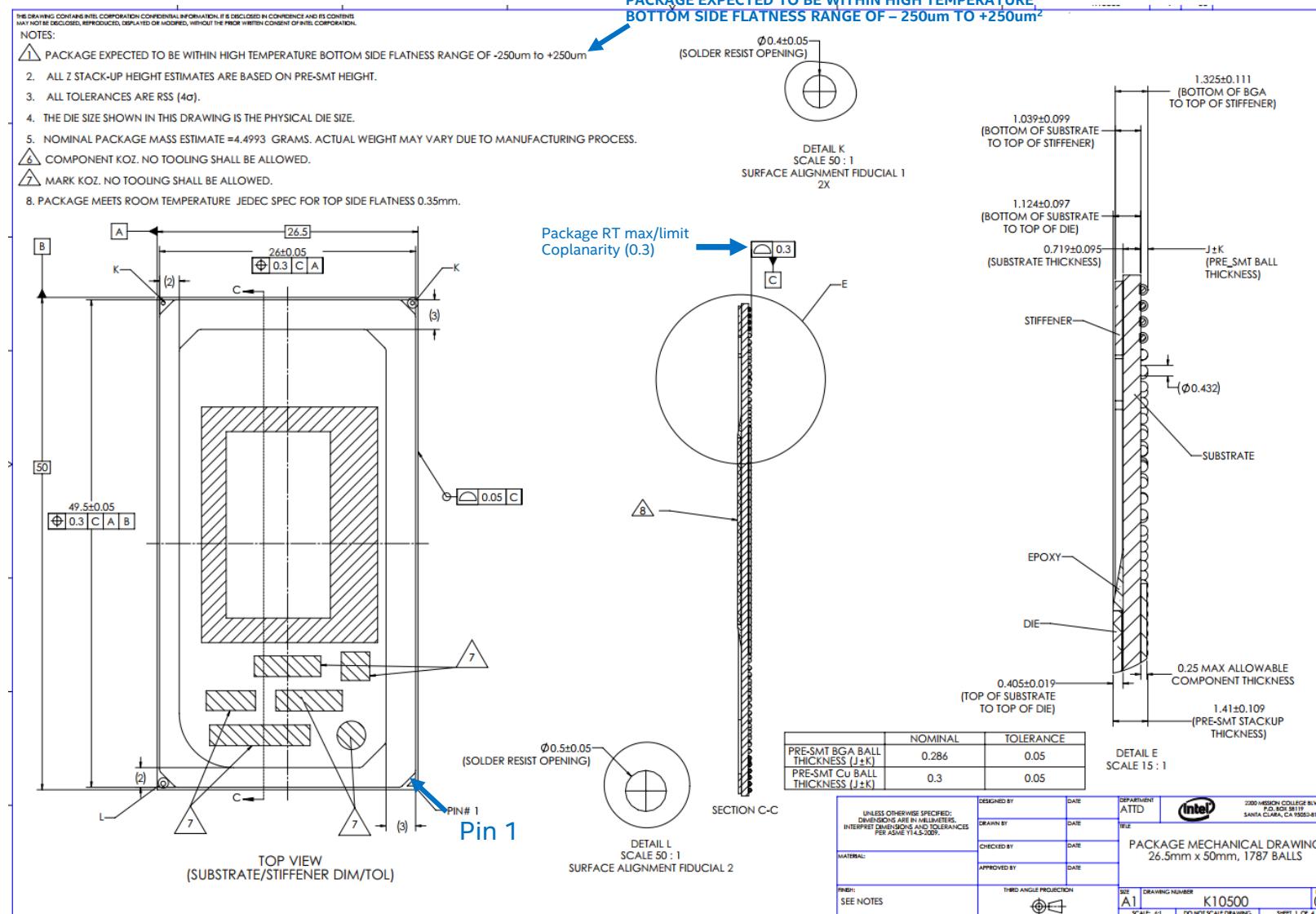
Notes:

- ¹This will be referred to as TGL UP4 in this document.
- Package Mechanical Drawing (PMD) # K46227, Rev 03



1.2 Package Mechanical Drawing

Tiger Lake H81¹ 50 x 26.5mm (page 1 of 4)



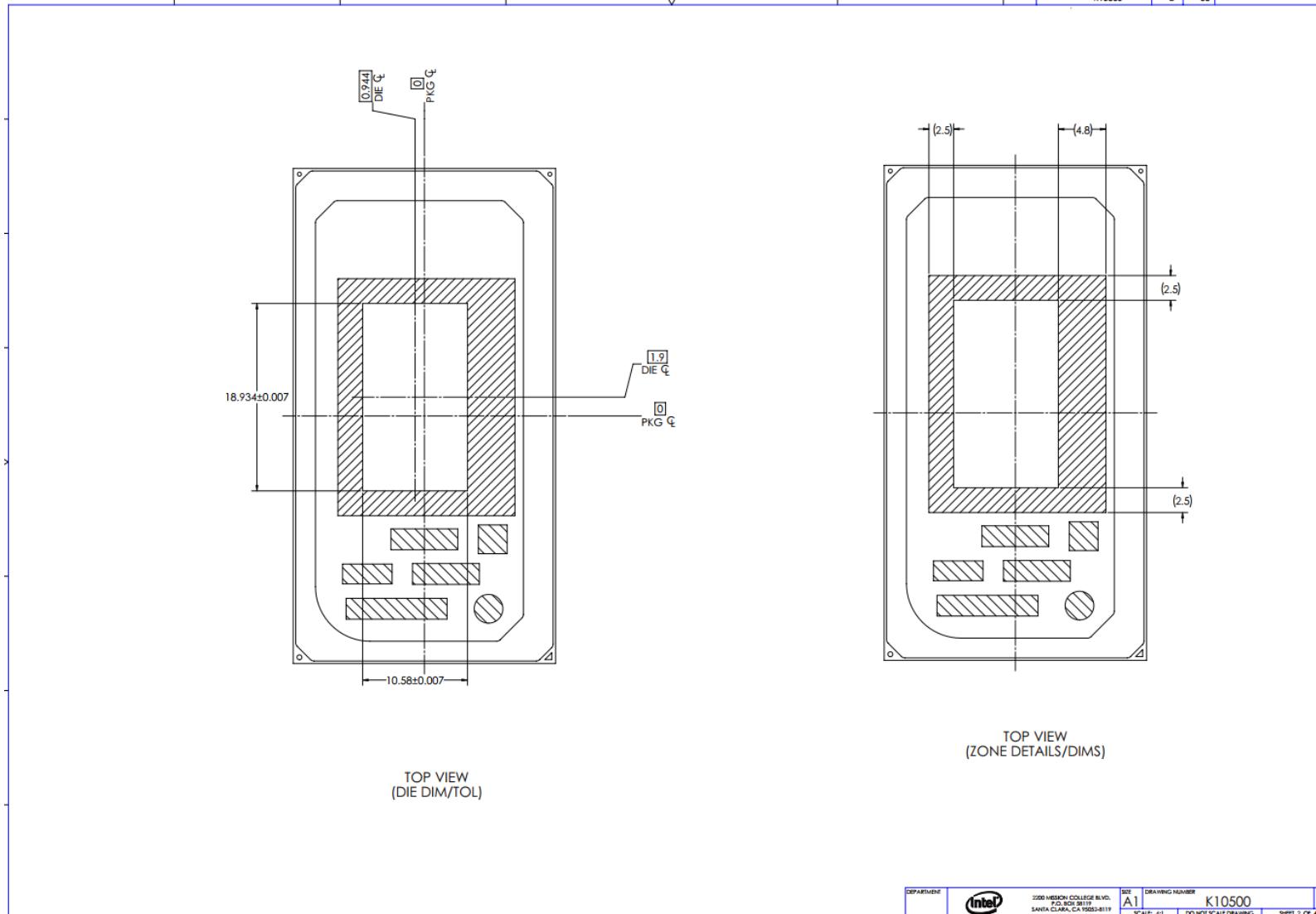
Notes:

- ¹This will be referred to as TGL H81 in this document.
- ²Between lowest active temperature of the board paste to peak reflow temperature.
- Package Mechanical Drawing (PMD) # K10500, Rev 5



1.2 Package Mechanical Drawing

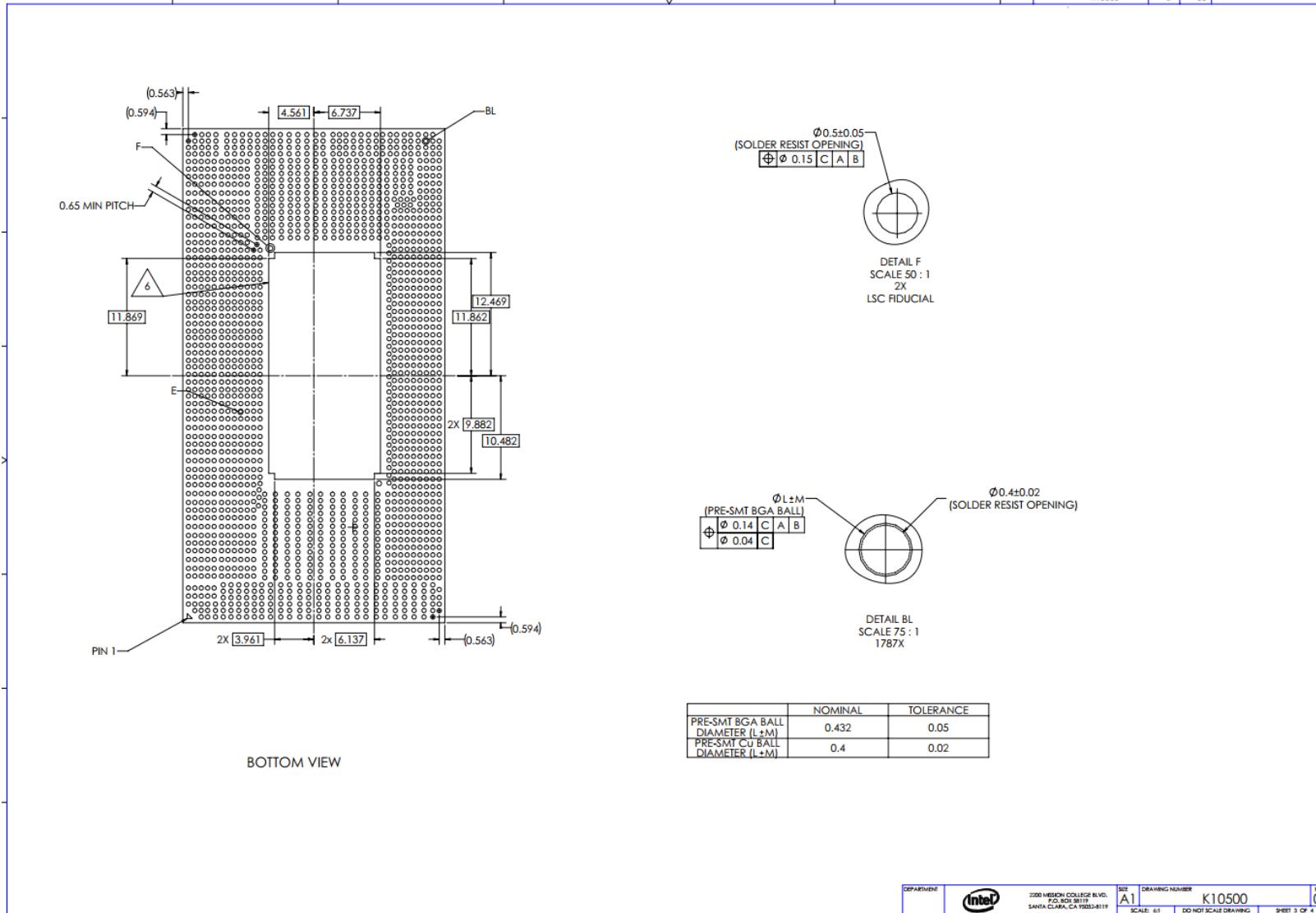
Tiger Lake H81¹ 50 x 26.5mm (page 2 of 4)





1.2 Package Mechanical Drawing

Tiger Lake H81¹ 50 x 26.5mm (page 3 of 4)



Notes:

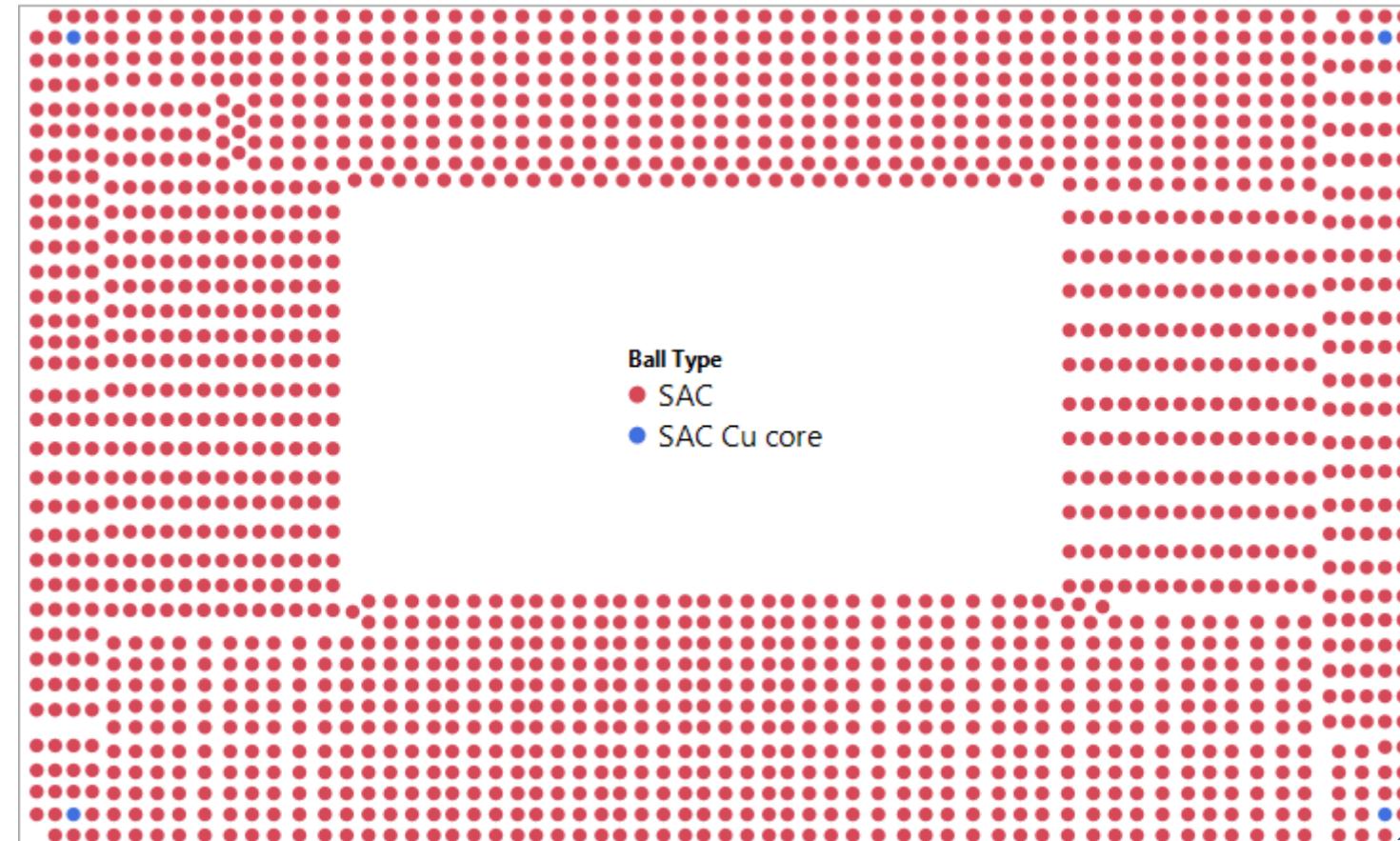
- ¹This will be referred to as TGL H81 in this document.
- Package Mechanical Drawing (PMD) # K10500, Rev 5



1.2 Cu Core Standoff Locations

Tiger Lake H81¹

CR40



C40

Notes:

- ¹This will be referred to as TGL H81 in this document.
- This is the Copper Core Standoffs locations drawing

C2

Dead bug view



1.3 Package Attributes

PCH Package Attributes

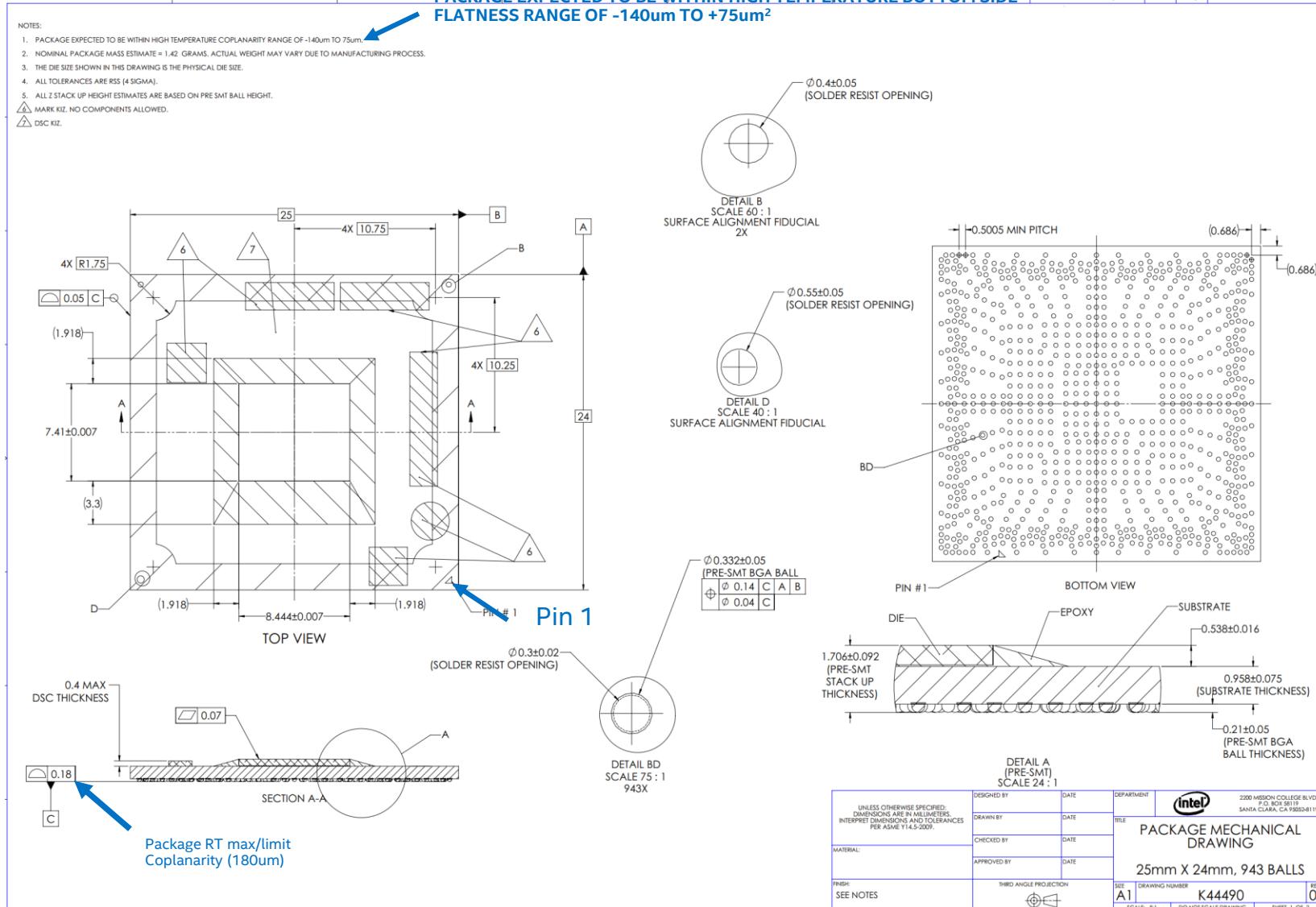
| Attribute | Tiger Lake PCH-H |
|--|---|
| | Mobile/Desktop |
| | Tiger Lake PCH-H Platform Controller Hub |
| Package Size (mm) | 25 x 24 |
| Solder Ball Material | SAC405 |
| Surface Finish | NiPdAu |
| Ball Count | 943 |
| Min Ball Pitch (mm) | 0.5 |
| Ball Diameter (Pre-attach) (um/mil) | 305/12 |
| Pre-SMT z Height (SLI bottom to die top) (mm) Assumes Zero Package Warpage | 1.709 ± 0.091 |
| Post-SMT z Height | Customer's SMT process & materials affect Post-SMT Z-height. If needed, customers should measure Post-SMT Z-heights on actual product.. |
| Land Side Capacitor | N/A |
| Die Side Capacitor | Yes (400um max height) |
| Die Configuration | Single die |
| PCH Die Size (mm) | 8.515 x 7.396 |
| Die Thickness + C4 Bumps (um) | 545 |
| Substrate thickness (um) | 958 |
| NCTF Corner Balls | 7/corner |
| PCB Type | Type3 |
| Stiffener | N/A |
| Top Side Over Molded | N/A |
| Hole, Recess or Cavity Void in MB | N/A |
| Shipping Media | T&R |

Notes:

- All components are halogen free FCBGAs with a max temp rating of 260°C

1.4 Package Mechanical Drawing

Tiger Lake PCH¹ 25x24mm



Notes:

- ¹This will be referred to as TGL PCH in this document.
- ²Between lowest active temperature of the board paste to peak reflow temperature.
- Package Mechanical Drawing (PMD) # K44490, Rev 02

Module 2: Land Pattern Design Guidelines

Manufacturing with the Intel® Platform Code Named Tiger Lake

Overview – Table of Contents

| | | | | | | |
|--|--|--|--|------------------------------------|--|--|
| Module 1: <u>Component Attributes and Drawings</u> | Module 2: <u>Land Pattern (PCB Pad) Design Guidelines</u> | Module 3: <u>Manufacturing Guidelines</u> | Module 4: <u>Shipping & Handling</u> | Module 5: <u>Testing</u> | Module 6: <u>System Integration & ESD Considerations</u> | Module 7: <u>References</u> |
| 1.1 Package Attributes Intel® FCBGA Processors 1.2 Package Mechanical Drawings (PMD) FCBGA Processors 1.3 Package Attributes PCH 1.4 Package Mechanical Drawings (PMD) PCH | 2.1 Land Pattern Design Guidelines Introduction 2.2 Mother Board Cavity Voiding Requirements 2.3 Land Pattern Design Guidelines (for the different processors & chipset) | 3.1 Introduction 3.2 Example Package Dynamic Warpage Data 3.3 Critical SMT Recommendations 3.4 Manufacturing Guidelines General Info 3.5 Solder Paste Formulation Optimization 3.6 Solutions to Extend Stencil Aperture Area Ratio 3.7 Cu Core Standoff Technology 3.8 Solder Paste Volume Optimization Stencil Design Recommendations 3.9 SMT Reflow Pallet Recommendations 3.10 SMT Reflow Profile TC Location 3.11 Overview of Board Flexure 3.12 Board Level Adhesive Overview 3.13 Package Rework 3.14 FACR Prep Process | 4.1 Processor and Chipset Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements 4.4 BGA Package Handling BKMs 4.5 T&R Package Handling BKMs | 5.1 Test Information | 6.1 Introduction 6.2 Electro Static Discharge (ESD) Platform Component Goals 6.3 Electro Static Discharge (ESD) Design Guidelines 6.4 Electro Static Discharge (ESD) Additional Resources 6.5 Thermal Solution Assembly / Disassembly considerations | 7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Resource Design Center access Information |



Acronyms Found in this Module

| | |
|-------|---|
| BEP | Board Enabling Platform |
| Cu | Copper |
| CuOSP | Copper Organic Solderability Preservative |
| EDS | External Design Specification |
| FCBGA | Flip-Chip Ball Grid Array |
| HIMB | Hole In Mother Board |
| HT | High Temperature |
| MAS | Manufacturing Advantage Service |
| MB | Mother Board |
| MSL | Moisture Sensitivity Level |
| NCTF | Non-Critical to Function |
| PCH | Platform Control Hub |
| PDS | Product Datasheet |
| PMD | Package Mechanical Drawing |
| RIMB | Recess In Mother Board |
| RT | Room Temperature |
| T&R | Tape and Reel |
| TFT | Thermoform Tray |

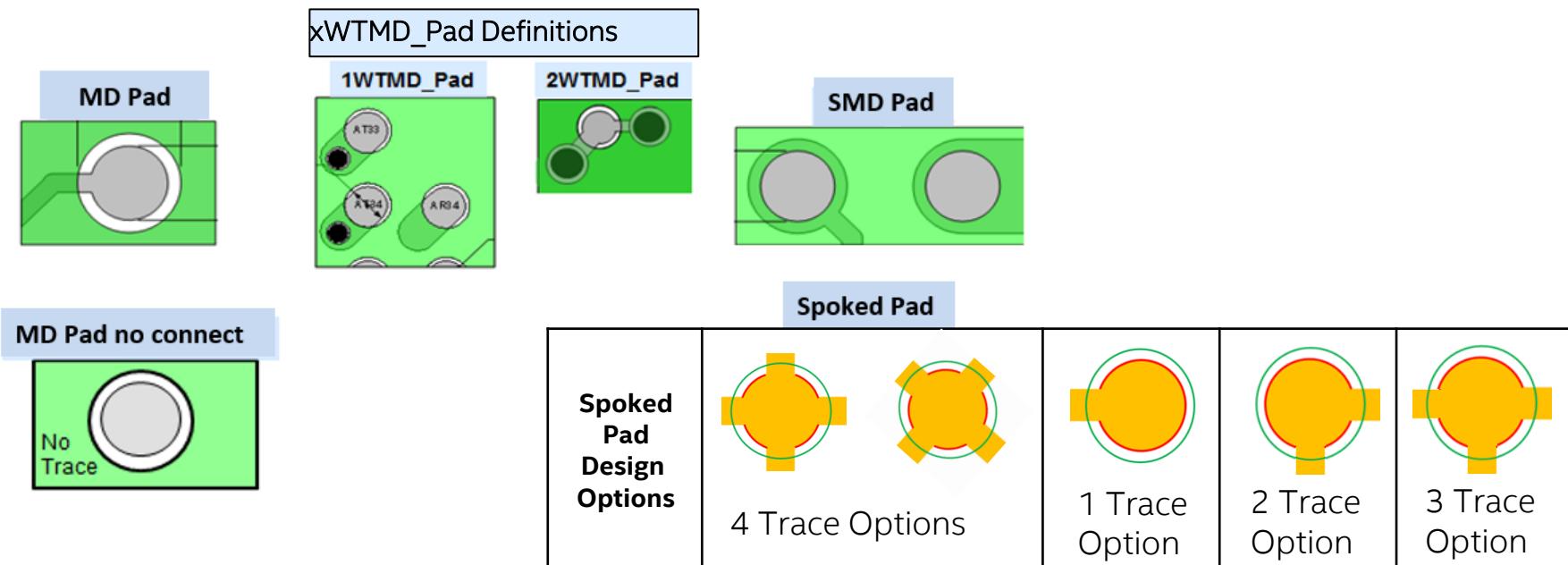


2.1 Land Pattern Design Guidelines Introduction

- In order to achieve the highest solder joint strength & reliability, it is recommended that customers follow the Intel reference Land Pattern design for Mobile Platform FCBGA components.
 - Land pattern designs recommendations included in this module are for pads, traces, trace angles and via-in-pads.
- Corner NCTF test point recommendations will be provided in a future release.
 - A method to test the connectivity of corner NCTF Solder Joints (SJ) on mobile FCBGA processor and chipset packages will be included in this module.

2.1 Land Pattern Definitions

- **MD = Metal Defined** (Traditional dog bone Via to BGA-Pad)
 - Pad is defined as MD when 40% - 100% of the pad circumference is defined by metal.
 - I/O Driven, trace width usually determined by Impedance matching.
 - No connect is metal pad with "NO" trace connected (e.g. uvia in pad).
- **Spoked Pad**
 - Metal Defined pad with up to 4 traces branching off it such that at least 40% of pad periphery is still defined by metal. Used to improve solder joint reliability where a surface plane is present.
- **WTMD = Wide Trace Metal Defined Pad** (Trace = Pad Diameter or Less)
 - $xWTMD >> 1WTMD = 1$ Wide Trace, $2WTMD = 2$ Wide Traces going to BGA Pad.
 - Multiple "Wide Traces", can look/behave as a Spoke design.
- **SMD = Soldermask Defined** (60% - 100% of the pad circumference is defined by Soldermask, pads in flood areas and/or Larger metal pad)



Notes:

- Metal Defined pad type (including Spoked Pad) preferred for temperature cycling performance.
- SMD pad type preferred for shock performance.
- Filled uvia in pad is acceptable.



2.2 Mother Board Cavity Voiding Requirements

TGL UP3/H35

Requirements:

- Packages with Land Side Capacitors (LSCs) have specific mother board design guidance
 - No Cu Planes, PTH's, Silkscreen or Via's are allowed in the LSC cavity area, on the surface layer (remove and void these features, moving to an inner layer if necessary). Package LSCs may cause interference with these features.
 - If Via's are used, a distance of 150um must be maintained from any PTH/via to the package lands side capacitors (as measured from the via edge to LSC body outline) inside the cavity
 - Solder resist is present to prevent any LSC to PTH/via shorting

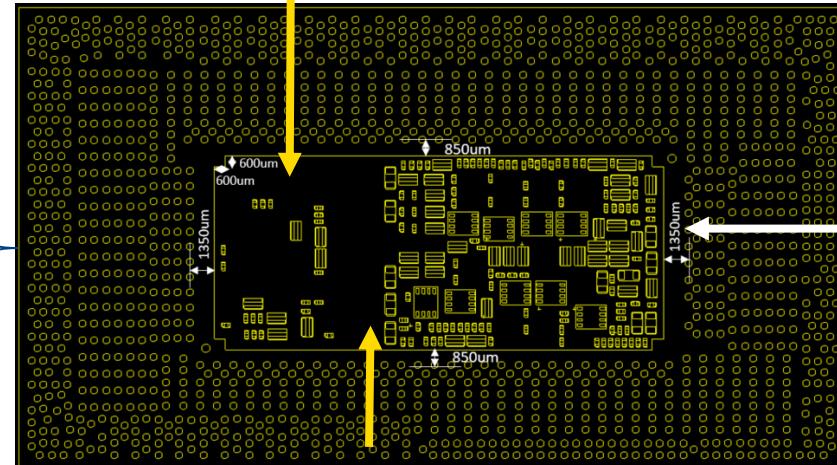
SMT Failure Mechanism:

- If the above mother board design requirements are not met:
 - During the SMT/reflow process, package LSCs come into contact with copper and/or vias + soldermask, creating a standoff on the motherboard
 - This standoff raises the package, limiting the collapse of the solder joints, tilting the package on one side, and creating SJ Open Defects (e.g. Head and Pillow, Non-Contact or Non-Wet Opens)
 - This interaction may cause significant SMT SJ defects and having to rework the component

Board Design Actions to Take:

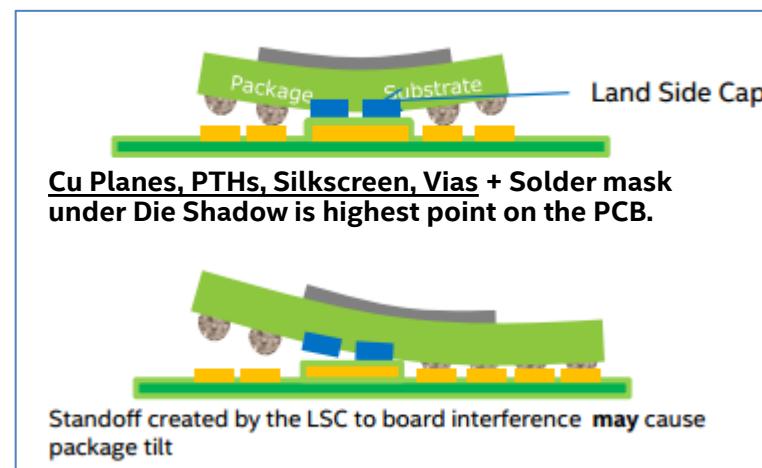
- See the Platform Design Guide (PDG), the Package LSC (.CLP/.DXF LSC File) and the TDK Package Footprint for specific details
- Step 1-Download the Tiger Lake UP3/H35/UP4 PDG:
 - Follow the recommendations in the PDG, Power Integrity Recommendations Chapter: "Tiger Lake UP4 – General Design Recommendations"
- Step 2-Import the TGL UP3/H35/UP4 (.CLP/.DXF LSC File) [[RDC# 608524](#)] or Foot Print Symbol file [RDC# 615721](#) into your mother board design:
 - Ensure that no mother board Cu Planes, PTH's, Silkscreen or Vias interfere with any of the package LSC locations

Package: LSC's
(in this region)



The distances shown are between BGA Pad Center and KOZ

Mother Board: Cu Voided Region
(No Cu Planes, PTH's, Silkscreen or Via's)



Drawings are not to scale and
for illustrative purposes only



2.2 RIMB / HIMB Requirements

TGL UP4

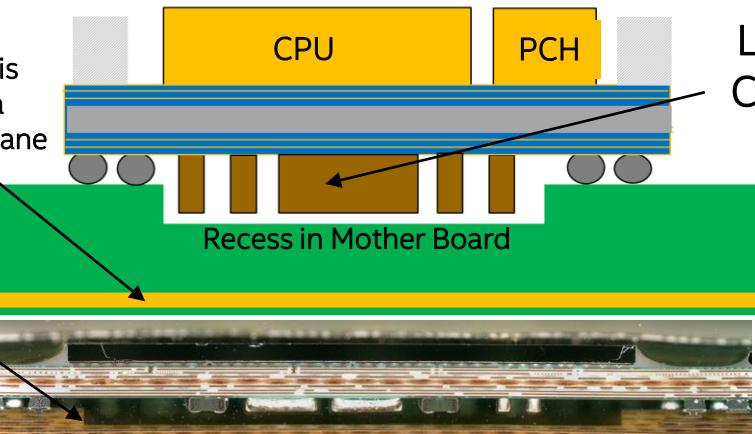
Requirements:

- The Tiger Lake UP4 processor SKU requires either a Hole In Mother Board (HIMB) [plus a FIVR EMI Shield] or a Recess In Mother Board (RIMB) [Depth of 232um +/- 50um for SAC Reflow Process], in the LSC cavity area, to accommodate the height of the Land Side Capacitors (LSC) & ensure high SMT yields
- No Cu Planes, PTH's, Silkscreen or Via's are allowed in the LSC cavity area, on the surface layer (remove and void these features, moving to an inner layer if necessary). If Via's are used, a distance of 150um must be maintained from any PTH/via to the package lands side capacitors (as measured from the via edge to LSC body outline) inside the cavity. Solder resist is present to prevent any LSC to PTH/via shorting. Any laser stop conductive metal must be removed from RIMB area by the PCB vendor.
- Refer to the Tiger Lake PDG for RIMB or HIMB dimensional information

RIMB

RIMB Cavity is covered by a solid GND plane

RIMB Side View, Generic Example



Land Side Capacitors (LSC)

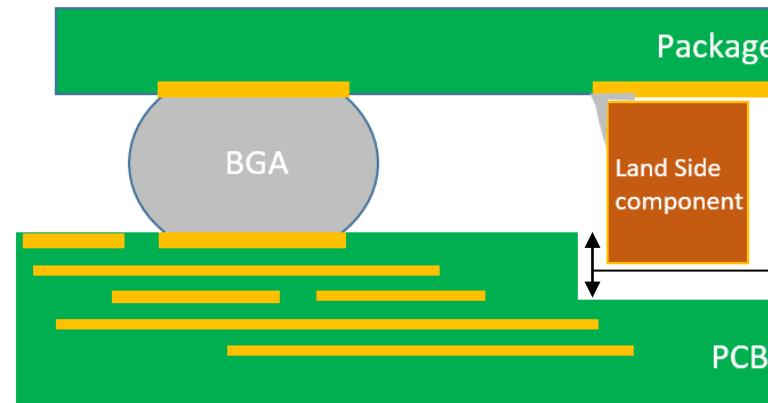
Package

Land Side component

Min cavity depth required from top of pad (w/ estimated HS load)

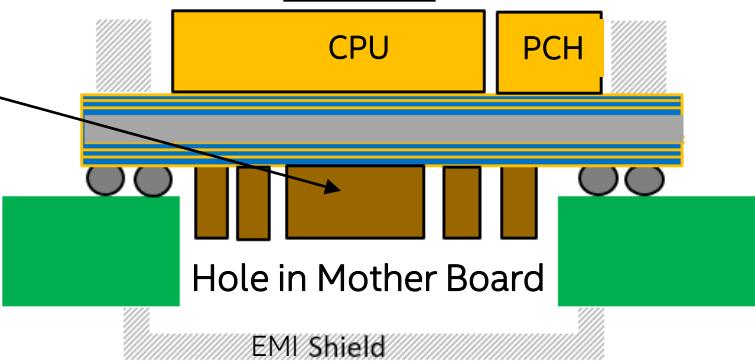
232 um +/- 50 um
Based on 4 sigma RSS assessments @ ~150 upm

Holding this tolerance is critical to achieving high SMT yields



Drawings are not to scale and for illustrative purposes only

HIMB



Hole in Mother Board

EMI Shield

HIMB Design Guidance

1. External Shield required for EMI/RFI performance
2. May optimize shield thickness / material to minimize Z-height impact
 - Flat metal sheet: Z-Height ~0.1mm
 - Conventional EMI shield: Z-Height >0.5mm

CAUTION: The ICL Y EMI Shield will not work for TGL UP4, due to a different HIMB size and shape

Refer to the Tiger Lake PDG for more comprehensive HIMB and RIMB dimensions & guidance

2.2 RIMB / HIMB Requirements

TGL UP4

Tiger Lake UP4 – Recess Shorting Risk Communication

Problem Statement: Electrical power-to-ground shorting of the TGL UP4 Package Land Side Capacitors (LSC) to the Recess In Motherboard (RIMB) metal laser stop feature is possible, if not removed during mfg

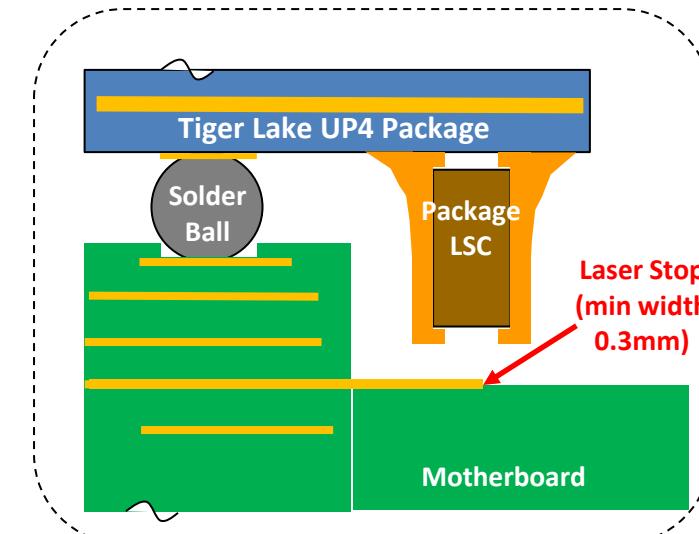
Investigation Findings: The recess for the TGL UP4 package LSC's can be created by PCB vendors using 2 different methods (method will vary by vendor):

- Mechanical Drill Process (leaves no metal in the recess area)
- Laser Drill Process (may leave a perimeter of metal in the recess area, referred to as a "laser stop", if it was not removed during the mfg process)

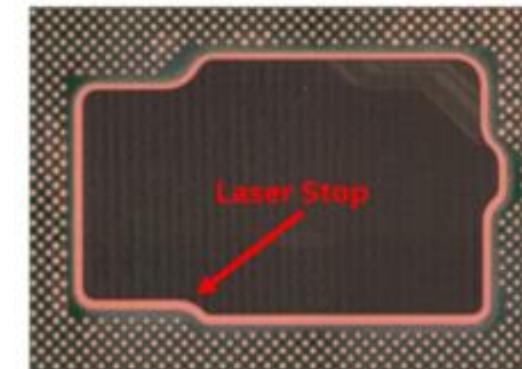
Laser Drill Process: The laser stop is a conductive perimeter of metal (Cu), min of 0.3mm wide inside the cavity, connected to one of the motherboard layers and used to control the laser Z-depth during cavity fabrication

Potential Risk: If any of the TGL UP4 package LSC's come in contact with the conductive perimeter of metal (laser stop), either at T=0 or under loading, it could cause catastrophic power-to-ground shorting and result in electrical failures

Recommendation: Ensure your TGL UP4 PCB vendors utilize a PCB mfg process that completely removes the laser stop metal perimeter prior to final motherboard completion & shipment to the PCB assembly factory



Generic Example - Laser Drill Process with Laser Stop (Side View)



Generic Example - Laser Drill Process with Laser Stop (Top Down View)

Drawings are not to scale and for illustrative purposes only

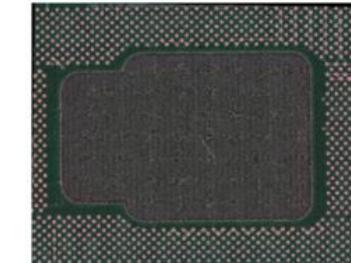
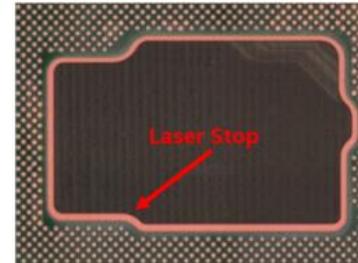
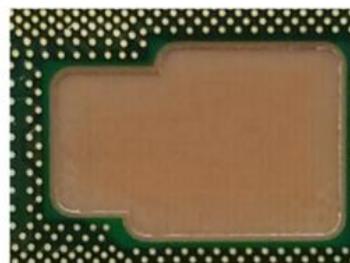
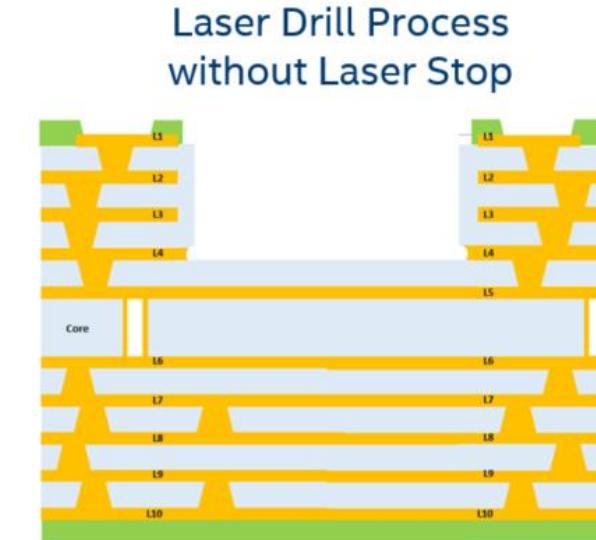
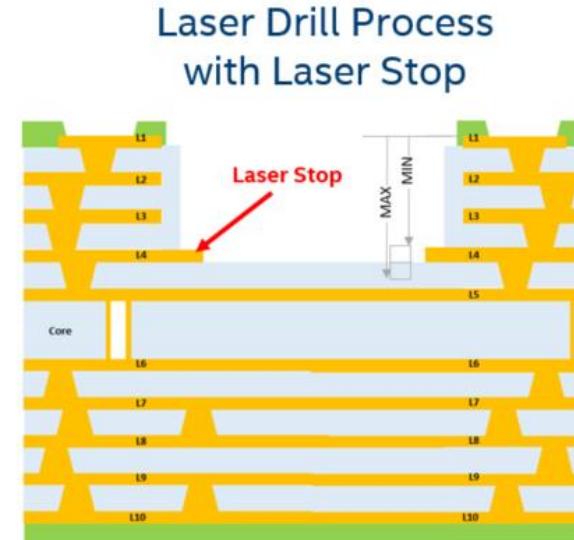
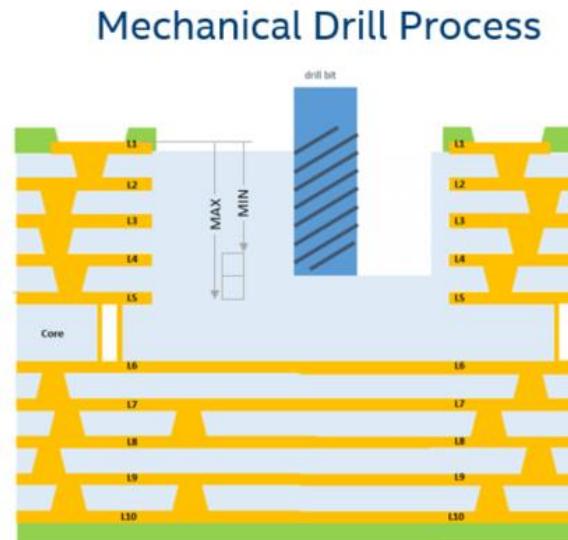


2.2 RIMB / HIMB Requirements

TGL UP4

Tiger Lake UP4 – Recess Shorting Risk Communication

Example Recess Creation Process: Mechanical Drill, Laser Drill with Laser Stop, Laser Drill without Laser Stop



Note: All recess images shown here are generic

Drawings are not to scale and for illustrative purposes only

2.2 RIMB / HIMB Requirements

TGL UP4

Background: During internal evaluation at Intel with multiple PCB suppliers using RIMB technology, Intel observed a dimple on some boards in the recess area (visible on the opposite side of the PCB from the Intel SoC) after the high temperature reflow process (see Figure 1 below). This dimple was not observed on PCBs prior to reflow.

Hypothesis: The hypothesis for this issue is that some combination of PCB material selection and design may result in localized deformation (dimples) under the RIMB during the reflow process. Possible factors may include PCB prepreg thickness or glass style, PCB material processing during manufacturing, copper fill, RIMB depth, etc... Intel was not able to determine the precise root cause of this issue and does not have additional guidance.

Potential Risk: When the PCB is reflowed during SMT, the dimple may result in the recess arcing and pushing back onto the LSCs (on the Intel SoC), which might result in the lifting of the Intel SoC, causing SMT yield issues. However, the internal SMT yield from Intel's RIMB evaluations have not shown any yield issues for both laser and mechanical formed RIMBs.

Recommendation: Recommend that customers work closely with their PCB suppliers during RIMB/product development, to fully inspect, evaluate and mitigate any dimples issues that may be discovered, under the RIMB area POST REFLOW.

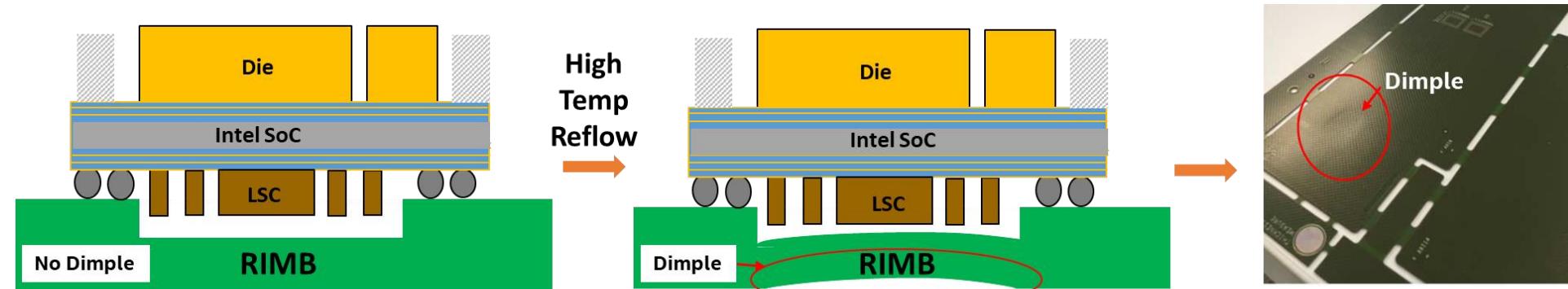


Figure 1

Drawings are not to scale and for illustrative purposes only



2.2 Mother Board Cavity Voiding Requirements

TGL H81

Requirements:

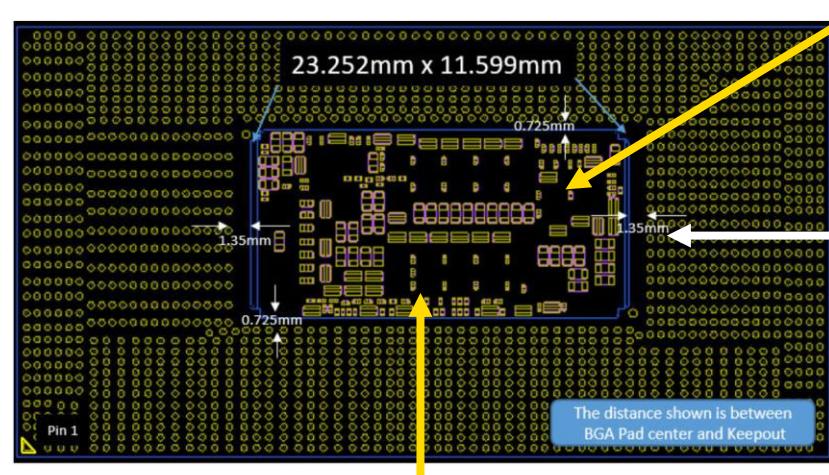
- Packages with Land Side Capacitors (LSCs) have specific mother board design guidance
 - No Cu Planes, PTH's, Silkscreen or Via's are allowed in the LSC cavity area, on the surface layer (remove and void these features, moving to an inner layer if necessary). Package LSCs may cause interference with these features.
 - If Via's are used, a distance of 150um must be maintained from any PTH/via to the package lands side capacitors (as measured from the via edge to LSC body outline) inside the cavity
 - Solder resist is present to prevent any LSC to PTH/via shorting

SMT Failure Mechanism:

- If the above mother board design requirements are not met:
 - During the SMT/reflow process, package LSCs come into contact with copper and/or vias + soldermask, creating a standoff on the motherboard
 - This standoff raises the package, limiting the collapse of the solder joints, tilting the package on one side, and creating SJ Open Defects (e.g. Head and Pillow, Non-Contact or Non-Wet Opens)
 - This interaction may cause significant SMT SJ defects and having to rework the component

Board Design Actions to Take:

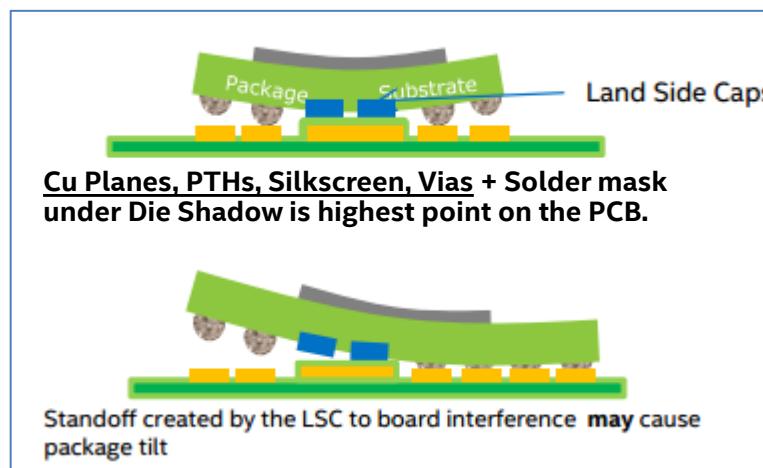
- See the Platform Design Guide (PDG), the Package LSC (.CLP/.DXF LSC File) and the TDK Package Footprint for specific details
- Step 1-Download the Tiger Lake H PDG:
 - Follow the recommendations in the PDG, Processor and PCH Power Integrity Recommendations Chapter: "Processor Layout Recommendation"
- Step 2-Import the TGL H (.CLP/.DXF LSC File) [[RDC# 608524](#)] or Foot Print Symbol file [RDC# 615721](#) into your mother board design:
 - Ensure that no mother board Cu Planes, PTH's, Silkscreen or Vias interfere with any of the package LSC locations



Package: LSC's
(in this region)

The distances shown are between BGA Pad Center and KOZ

Mother Board: Cu Voided Region
(No Cu Planes, PTH's, Silkscreen or Via's)

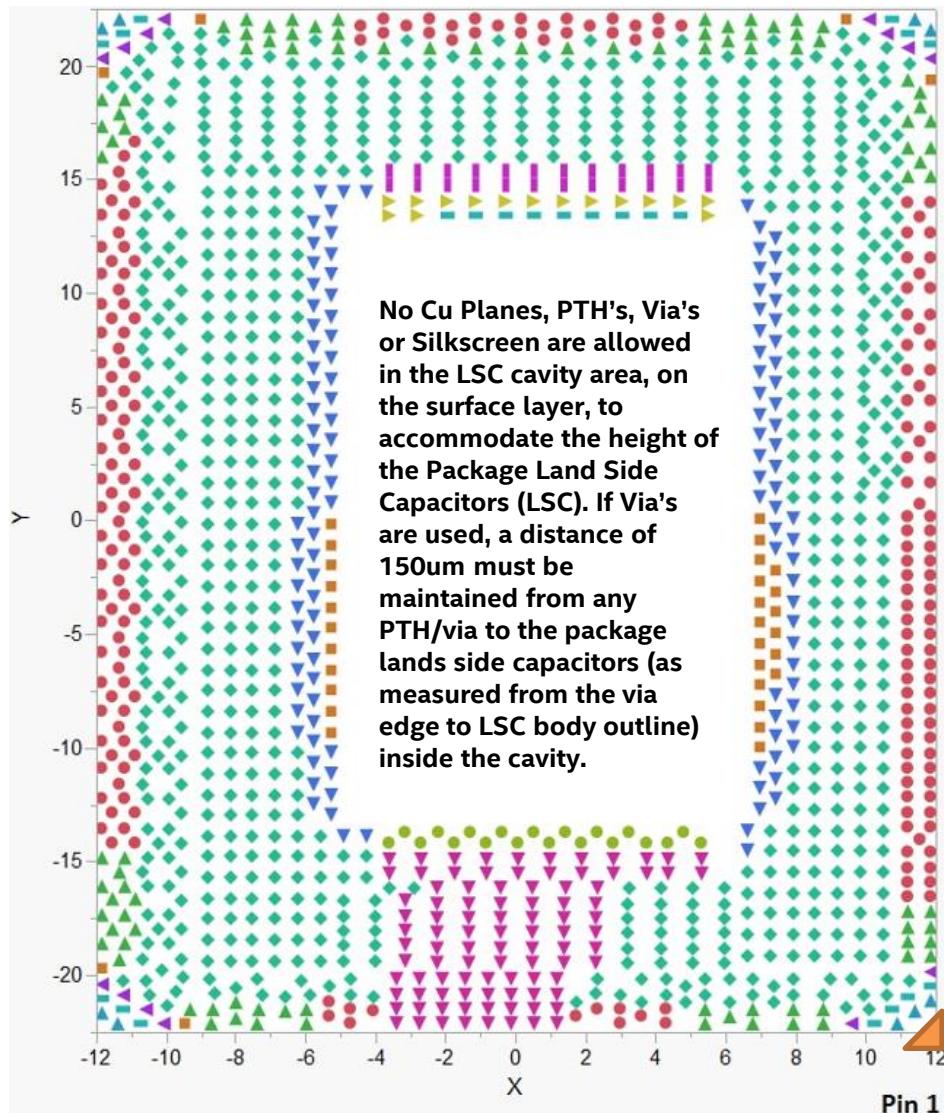


Drawings are not to scale and
for illustrative purposes only



2.3 Land Pattern Guidance

TGL UP3/H35 Processor Line



| Legend | Pad Size (microns/mils) ; SRO Size (microns/mils) | Function | # of Balls |
|--------|---|----------|------------|
| ● | MD or Spoked Pad Diameter: 200x300um, SRO 300x400um; SMD Pad Diameter: 300x400um, SRO: 200x300um | CTF | 204 |
| ▲ | MD or Spoked Pad Diameter: 250x350um, SRO 350x450um; SMD Pad Diameter: 350x450um, SRO: 250x350um | CTF | 92 |
| ▼ | MD or Spoked Pad Diameter: 300um, SRO 400um | CTF | 118 |
| ■ | MD or Spoked Pad Diameter: 300um, SRO 400um | NCTF | 35 |
| ◆ | MD or Spoked Pad Diameter: 300um, SRO 400um; SMD Pad Diameter: 400um, SRO: 300um | CTF | 801 |
| ◀ | MD or Spoked Pad Diameter: 300um, SRO 400um; SMD Pad Diameter: 400um, SRO: 300um | NCTF | 14 |
| ▶ | MD or Spoked Pad Diameter: 330um, SRO 430um; | CTF | 15 |
| ▬ | MD or Spoked Pad Diameter: 330um, SRO 430um; | NCTF | 22 |
| ▬ | MD or Spoked Pad Diameter: 330um, SRO 430um; SMD Pad Diameter: 430um, SRO: 330um | CTF | 24 |
| ● | MD or Spoked Pad Diameter: 355um, SRO 455um | CTF | 20 |
| ▲ | MD or Spoked Pad Diameter: 355um, SRO 455um | NCTF | 9 |
| ▼ | MD or Spoked Pad Diameter: 355um, SRO 455um; SMD Pad Diameter: 455um, SRO: 355um | CTF | 95 |

Alert: This is the FINAL land pattern design to be used for reliability testing.

Intel recommends to follow this land pattern design which is optimized to mitigate any potential solder joint quality and solder joint reliability issues.

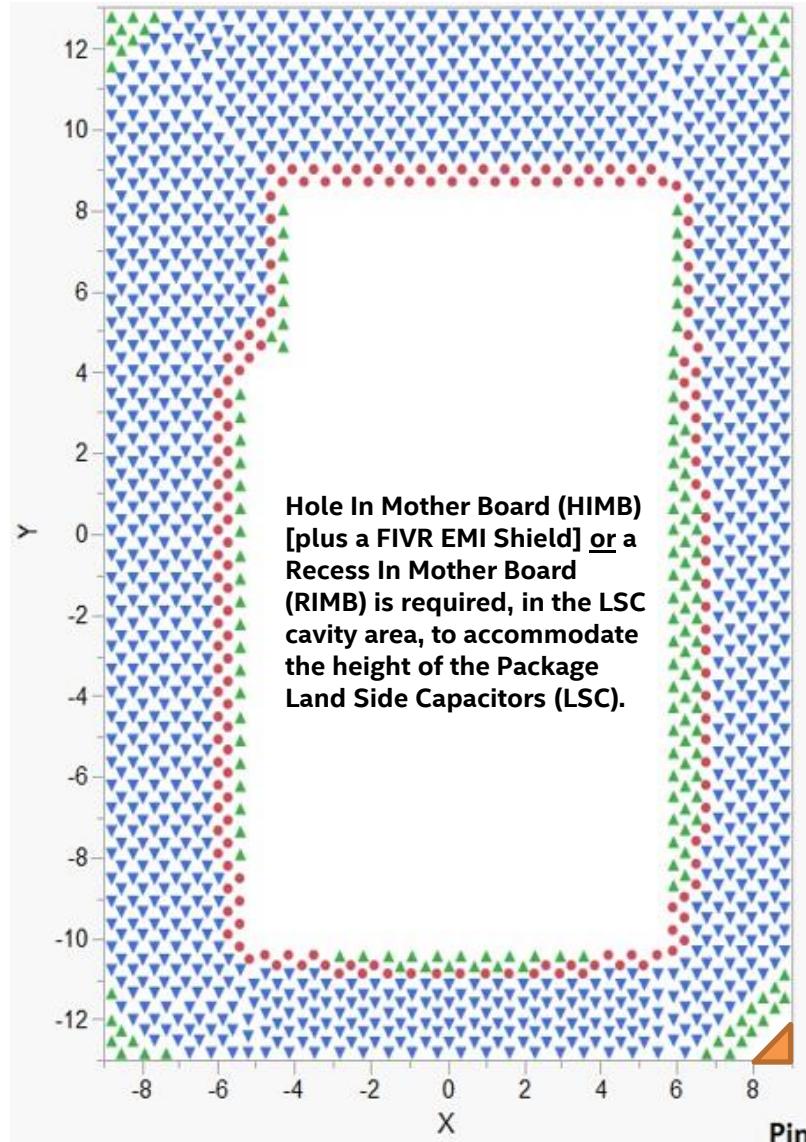
Notes:

- The values provided are intended to reflect the as-manufactured condition. Intel's BGA footprint definition between SRO (solder resist opening) and pad definition is 1:1, with allowance for PCB manufacturer to compensate the SRO to meet the requirements of IPC-SM-840.
- The board layout engineers need to ensure pad in-plane copper connectivity meets pad type definitions (MD, SMD, Spoked) as manufactured.
- Refer to Pad Definitions Slide for pad/trace type and geometry definitions
- Tiger Lake UP3/H35 Platform DDR4 SODIMM Reference Validation Platform (RVP) Technical Documentation Kit (TDK) info can be found RDC# 609003



2.3 Land Pattern Guidance

TGL UP4 Processor Line



| Legend | Pad Size (microns/mils); SRO Size (microns/mils) | Function | # of Balls |
|--------|---|----------|------------|
| ● | MD or Spoked Pad : Pad 250um (10 mils), SRO 325um (13 mils) | CTF | 172 |
| ▲ | MD or Spoked Pad : Pad 250um (10 mils), SRO 325um (13 mils) | NCTF | 153 |
| ▼ | MD or Spoked Pad : Pad 250um (10 mils), SRO 325um (13 mils) SMD Pad : Pad 325um (13 mils), SRO 250um (10 mils) | CTF | 1273 |

Alert: This is the FINAL land pattern design to be used for reliability testing.

Intel recommends to follow this land pattern design which is optimized to mitigate any potential solder joint quality and solder joint reliability issues.

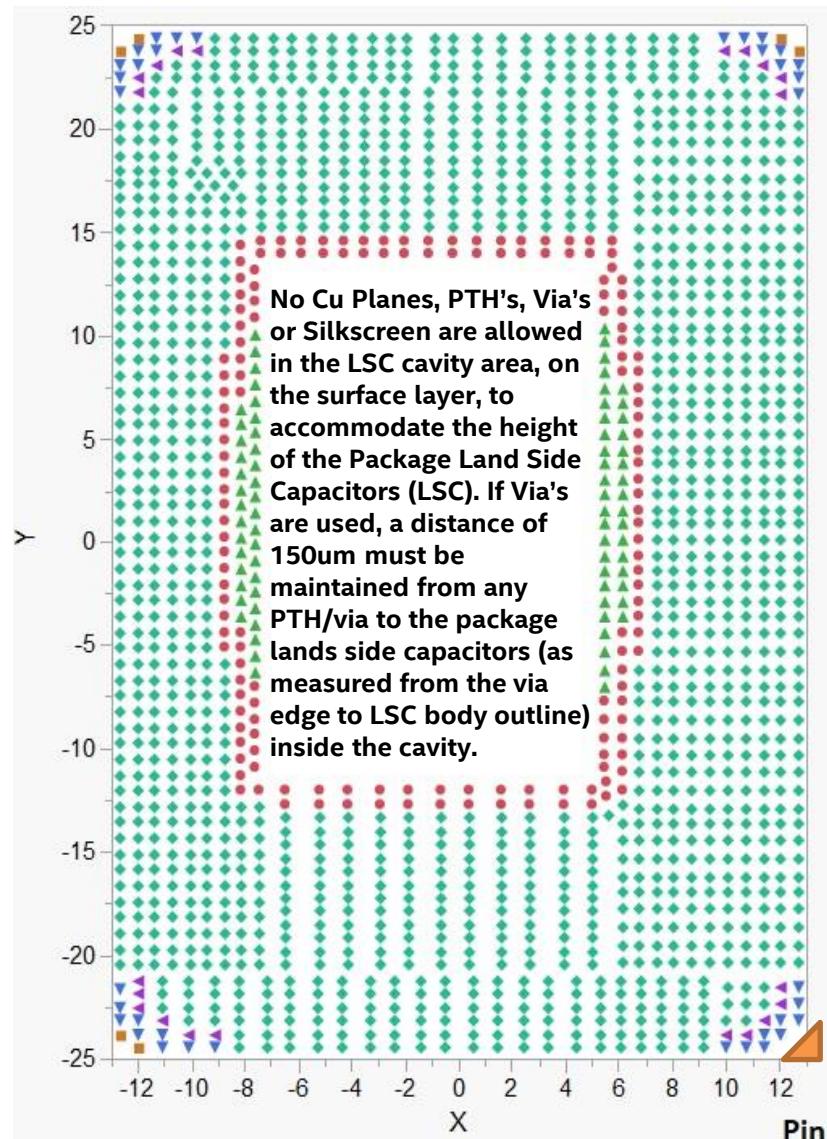
Notes:

- The values provided are intended to reflect the as-manufactured condition. Intel's BGA footprint definition between SRO (solder resist opening) and pad definition is 1:1, with allowance for PCB manufacturer to compensate the SRO to meet the requirements of IPC-SM-840.
- The board layout engineers need to ensure pad in-plane copper connectivity meets pad type definitions (MD, SMD, Spoked) as manufactured.
- Refer to Pad Definitions Slide for pad/trace type and geometry definitions
- Tiger Lake UP4 Platform LP4x Reference Validation Platform (RVP) Technical Documentation Kit (TDK) information is RDC# 610815



2.3 Land Pattern Guidance

TGL H81 Processor Line



| Legend | Pad Size (microns/mils) ; SRO Size (microns/mils) | Function | # of Balls |
|--------|--|----------|------------|
| ● | MD or Spoked Pad Diameter: 300um, SRO 400um | CTF | 155 |
| ▲ | MD or Spoked Pad Diameter: 300um, SRO 400um | NCTF | 76 |
| ▼ | MD or Spoked Pad Diameter: 380um, SRO 480um | NCTF | 36 |
| ■ | MD or Spoked Pad Diameter: 400um, SRO 500um | NCTF | 6 |
| ◆ | MD or Spoked Pad Diameter: 300um, SRO 400um; SMD Pad Diameter: 400um, SRO: 300um | CTF | 1493 |
| ◀ | MD or Spoked Pad Diameter: 355um, SRO 455um; SMD Pad Diameter: 455um, SRO: 355um | CTF | 21 |

Alert: This is the FINAL land pattern design to be used for reliability testing.

Intel recommends to follow this land pattern design which is optimized to mitigate any potential solder joint quality and solder joint reliability issues.

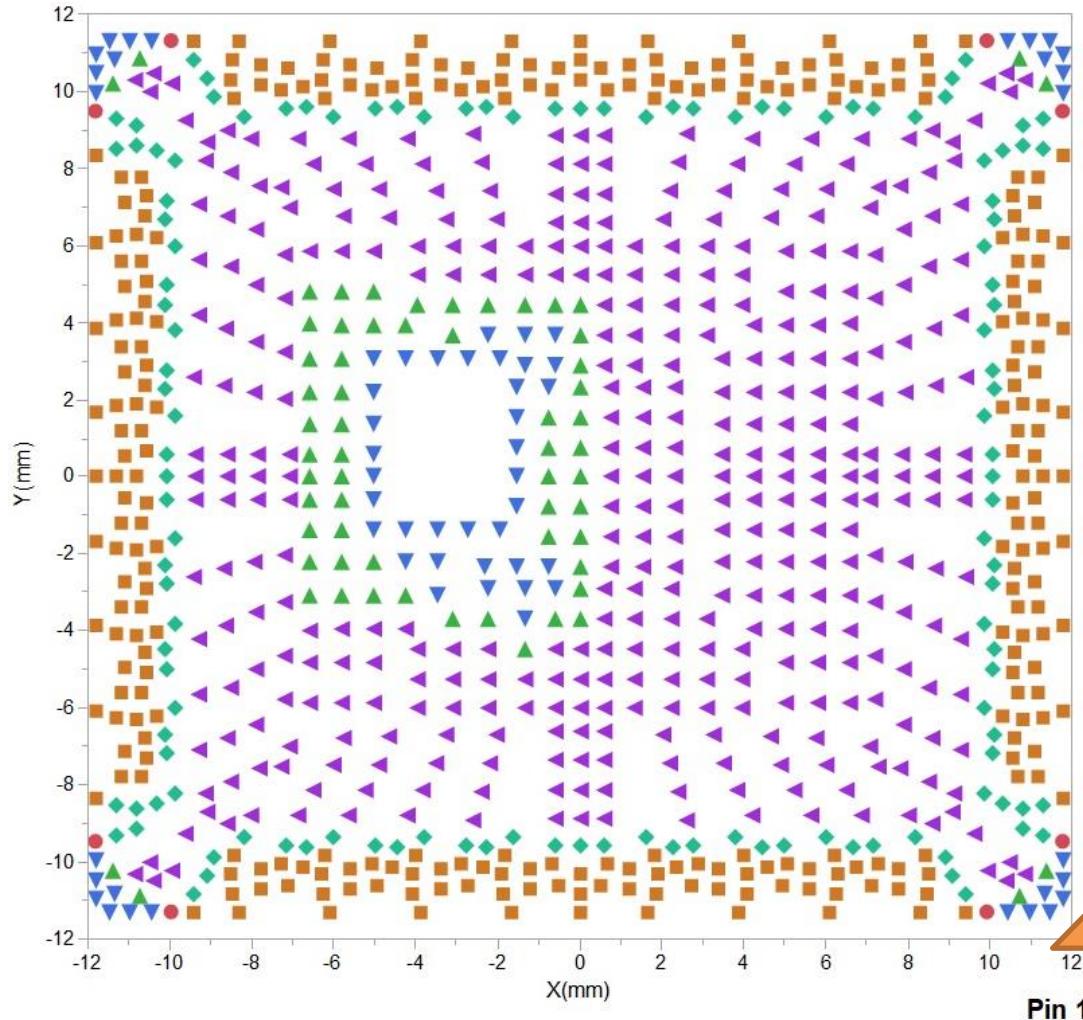
Notes:

- The values provided are intended to reflect the as-manufactured condition. Intel's BGA footprint definition between SRO (solder resist opening) and pad definition is 1:1, with allowance for PCB manufacturer to compensate the SRO to meet the requirements of IPC-SM-840.
- The board layout engineers need to ensure pad in-plane copper connectivity meets pad type definitions (MD, SMD, Spoked) as manufactured.
- Refer to Pad Definitions Slide for pad/trace type and geometry definitions
- Tiger Lake H Reference Validation Platform (RVP) Technical Documentation Kit (TDK) information is RDC
 - TGL H DDR4 Reference Validation Platform (RVP) TDK RDC#618697
 - TGL H DDR5 Reference Validation Platform (RVP) TDK RDC#619361
 - TGL H Board Enabling Platform (BEP) TDK RDC# 618367



2.3 Land Pattern Guidance

TGL PCH (Mobile)



| Legend | Pad Size (microns/mils) ; SRO Size (microns/mils) | Function | # of Balls |
|--------|--|----------|------------|
| ● | MD or spoked pad diameter: 280um(11mil)Pad, 380um(15mil) SRO | CTF | 8 |
| ▲ | MD or spoked pad diameter: 305um(12mil)Pad, 405um(16mil) SRO; | CTF | 63 |
| ▼ | MD or spoked pad diameter: 305um(12mil)Pad, 405um(16mil) SRO; | NCTF | 64 |
| ■ | MD Oblong pad : 205X255um(8X10mil)Pad, 305X355um(12X14mil) SRO; SMD Oblong pad : 305X355um(12X14mil) Pad, 205X255um(8X10mil) SRO. | CTF | 284 |
| ◆ | MD or spoked pad diameter: 255um(10mil)Pad, 355um(14mil) SRO; SMD pad diameter: 355um(14mil) Pad, 255um(10mil) SRO. | CTF | 124 |
| ◀ | MD or spoked pad diameter: 305um(12mil)Pad, 405um(16mil) SRO; SMD pad diameter: 405um(16mil) Pad, 305um(12mil) SRO. | CTF | 400 |

Alert: This is the FINAL land pattern design to be used for reliability testing.

Intel recommends to follow this land pattern design which is optimized to mitigate any potential solder joint quality and solder joint reliability issues.

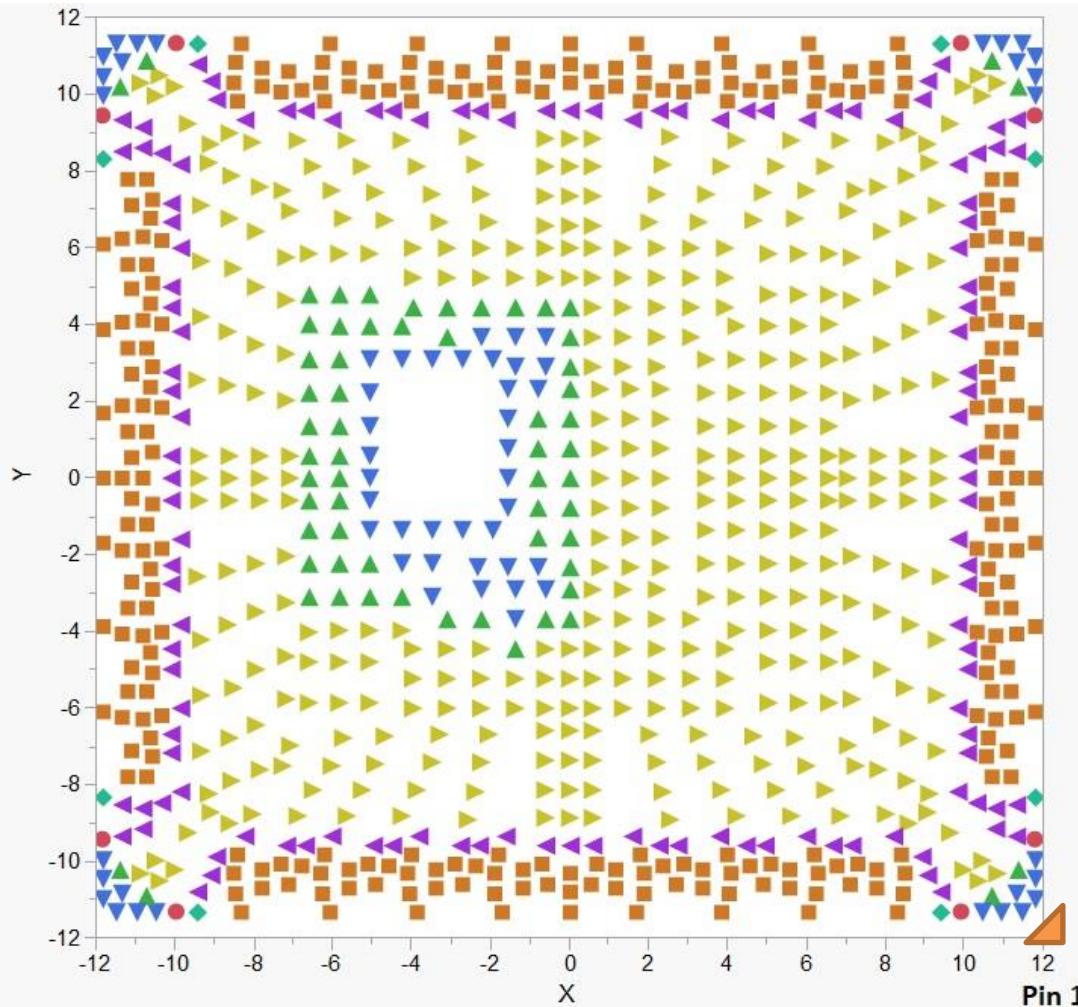
Notes:

- The values provided are intended to reflect the as-manufactured condition. Intel's BGA footprint definition between SRO (solder resist opening) and pad definition is 1:1, with allowance for PCB manufacturer to compensate the SRO to meet the requirements of IPC-SM-840.
- The board layout engineers need to ensure pad in-plane copper connectivity meets pad type definitions (MD, SMD, Spoked) as manufactured.
- Refer to Pad Definitions Slide for pad/trace type and geometry definitions
- Tiger Lake H Reference Validation Platform (RVP) Technical Documentation Kit (TDK) information is RDC
 - TGL H PCH Symbol Kit RDC# 618675
 - TGL H DDR4 Reference Validation Platform (RVP) TDK RDC#618697
 - TGL H DDR5 Reference Validation Platform (RVP) TDK RDC#619361
 - TGL H Board Enabling Platform (BEP) TDK RDC# 618367



2.3 Land Pattern Guidance

TGL PCH (Desktop)



| Legend | Pad Size (microns/mils); SRO Size (microns/mils) | Function | # of Balls |
|--------|---|----------|------------|
| ● | MD or spoked pad diameter: 280um(11mil)Pad, 380um(15mil) SRO | CTF | 8 |
| ▲ | MD or spoked pad diameter: 305um(12mil)Pad, 405um(16mil) SRO; | CTF | 63 |
| ▼ | MD or spoked pad diameter: 305um(12mil)Pad, 405um(16mil) SRO; | NCTF | 64 |
| ■ | MD or spoked pad diameter: 155X255um(6X10mil)Pad, 255X355um(10X14mil) SRO; SMD pad diameter: 255X355um(10X14mil) Pad, 155X255um(6X10mil) SRO. | CTF | 276 |
| ◆ | MD or spoked pad diameter: 205X255um(8X10mil)Pad, 305X355um(12X14mil) SRO; SMD pad diameter: 305X355um(12X14mil) Pad, 205X255um(8X10mil) SRO. | CTF | 8 |
| △ | MD or spoked pad diameter: 255um(10mil)Pad, 355um(14mil) SRO; SMD pad diameter: 355um(14mil) Pad, 255um(10mil) SRO. | CTF | 124 |
| ▶ | MD or spoked pad diameter: 305um(12mil)Pad, 405um(16mil) SRO; SMD pad diameter: 405um(16mil) Pad, 305um(12mil) SRO. | CTF | 400 |

Alert: This is the FINAL land pattern design to be used for reliability testing.

Intel recommends to follow this land pattern design which is optimized to mitigate any potential solder joint quality and solder joint reliability issues.

Notes:

- The values provided are intended to reflect the as-manufactured condition. Intel's BGA footprint definition between SRO (solder resist opening) and pad definition is 1:1, with allowance for PCB manufacturer to compensate the SRO to meet the requirements of IPC-SM-840.
- The board layout engineers need to ensure pad in-plane copper connectivity meets pad type definitions (MD, SMD, Spoked) as manufactured.
- Refer to Pad Definitions Slide for pad/trace type and geometry definitions
- Tiger Lake H Reference Validation Platform (RVP) Technical Documentation Kit (TDK) information is RDC
 - TGL H DDR4 Reference Validation Platform (RVP) TDK RDC#618697
 - TGL H DDR5 Reference Validation Platform (RVP) TDK RDC#619361
 - TGL H Board Enabling Platform (BEP) TDK RDC# 618367



2.4 Corner NCTF Solder Joint Testability Overview

Intel Recommendation: Try to include motherboard test features to test the connectivity of corner NCTF Solder Joints (SJ) on BGA processors

Background:

- Testing the corner NCTF SJ is optional, and can be used to check the BGA SJ integrity during the manufacturing process, identifying potential solder joint defects (e.g. open SJs)
- The corner NCTF solder joints experience the highest strain during board processing / handling and board flexure
 - It is useful to detect when those corner NCTFs fail, as fails at these locations can give an indication of marginal board assembly processing or designs

Motherboard Design Implementation:

- Intel's BGA processors allow for corner NCTF SJ testing capability
 - Some corner NCTF SJ's have pins connected to the package VSS/GROUND plane and/or VCC/POWER plane, which can be used to test SJ connectivity with ICT, using isolated test pads added to the customer's motherboard designs -> see Figures 1 & 2 below
- With motherboard test pads in place, ICT personnel can develop a continuity or resistance test to check connectivity from corner NCTF SJ's to their corresponding isolated test pads on the motherboard

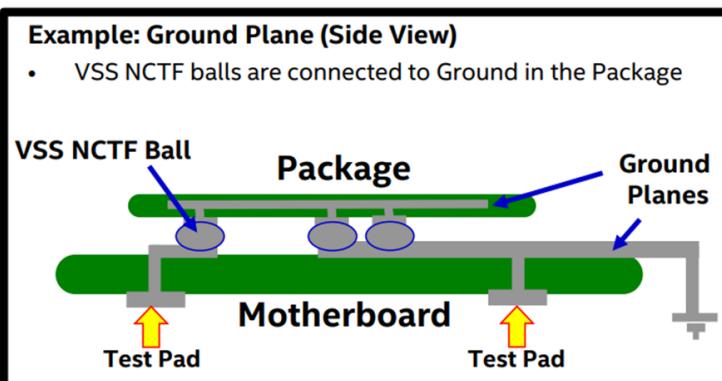
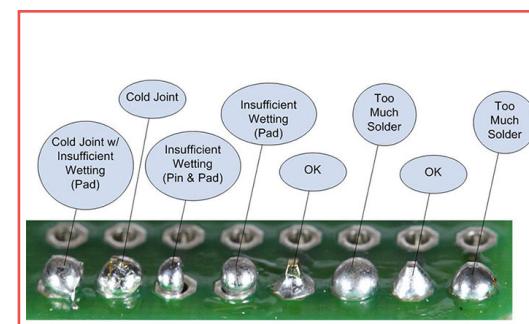


Figure 1: VSS Example

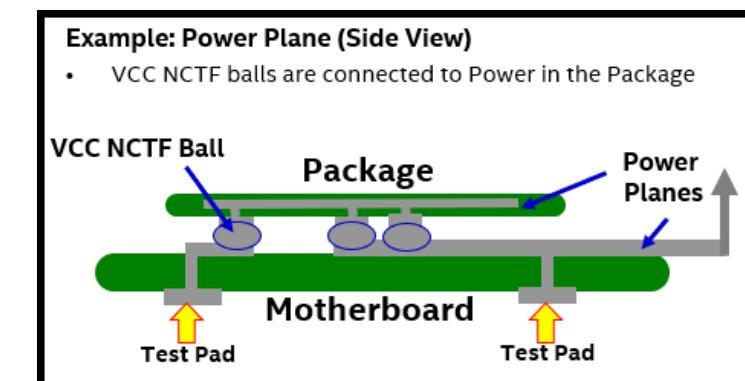


Figure 2: VCC Example



2.5 Corner NCTF Solder Joint Testability – Continuity / Resistance Test Threshold

Continuity / Resistance Test Threshold

- Continuity or resistance tests are developed using a pass/fail resistance threshold
- The pass/fail threshold would be determined by the accuracy of the test equipment and measurement data obtained from boards with known good solder joints
- For motherboards under test, a measurement below the pass/fail threshold may indicate a good package electrical solder joint (pass), and a measurement above the pass/fail threshold may indicate a bad package electrical solder joint (fail)

Note: This type of electrical resistance test can detect a completely open solder joint between the package and board, but can be ineffective in detecting marginal solder joint connectivity (a SJ that may not be mechanically sound)



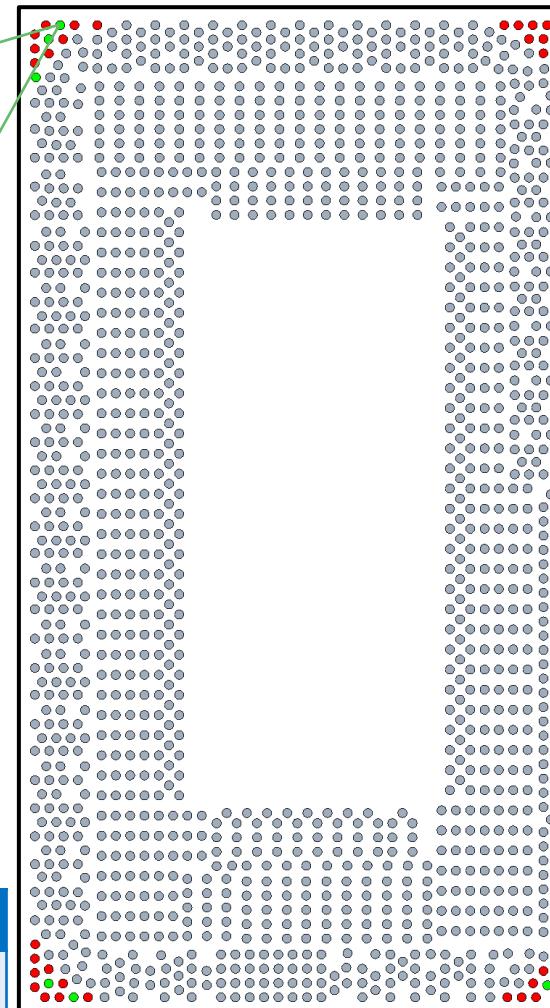
2.6 Processor Corner NCTF Test – PCB Routing Example

Tiger Lake UP3/H35 Processor Line

| Corner DW53 | | |
|-------------|----------|--------------------|
| Pin Number | Pin Name | Description |
| DW51 | NCTFVSS | NCTF Testable Pins |
| DV52 | NCTFVSS | NCTF Testable Pins |
| DP53 | NCTFVSS | NCTF Testable Pins |

NCTF - Non Critical to Function

OPTIONAL: For corner NCTF SJ testability, these BGA pins (shown in the tables and in green color) can be connected to isolated motherboard test pads and not connected to motherboard VCC/VSS plane (refer to Figures 1 & 2 in MAS section 2.4). The disconnection is not a functional concern; however, it is desirable for the routing of the test pads to not cause a split in the planes.



- NCTF Package Corner
- NCTF Testable Pins

| Corner A53 | | |
|------------|----------|--------------------|
| Pin Number | Pin Name | Description |
| B52 | NCTFVSS | NCTF Testable Pins |
| A49 | NCTFVSS | NCTF Testable Pins |

| Corner DW1 | | |
|------------|----------|--------------------|
| Pin Number | Pin Name | Description |
| DV1 | NCTFVSS | NCTF Testable Pins |
| DN1 | NCTFVSS | NCTF Testable Pins |

Note: For pinlist and ballmap information, refer to the **Package Ballout Mechanical Specification** document for this specific product.

| Corner A1 | | |
|------------|----------|--------------------|
| Pin Number | Pin Name | Description |
| B2 | NCTFVSS | NCTF Testable Pins |



2.6 Processor Corner NCTF Test – PCB Routing Example

Tiger Lake UP4 Processor Line

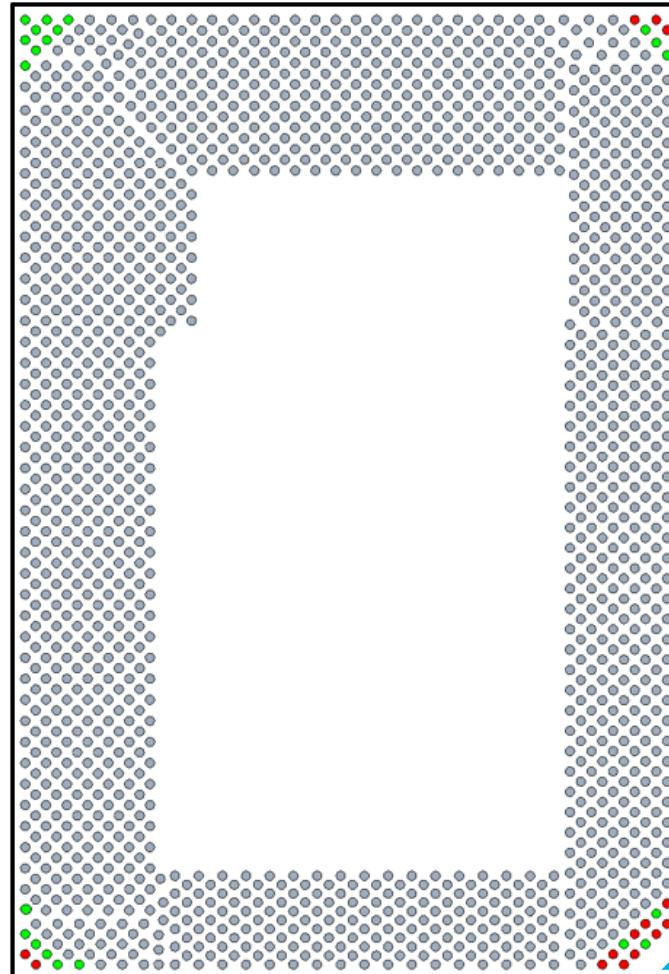
Corner DR67

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| DR67 | NCTFVSS | NCTF Testable Pins |
| DR65 | NCTFVSS | NCTF Testable Pins |
| DP66 | NCTFVSS | NCTF Testable Pins |
| DN67 | NCTFVSS | NCTF Testable Pins |
| DR63 | NCTFVSS | NCTF Testable Pins |
| DP64 | NCTFVSS | NCTF Testable Pins |
| DN65 | NCTFVSS | NCTF Testable Pins |
| DM66 | NCTFVSS | NCTF Testable Pins |
| DK67 | NCTFVSS | NCTF Testable Pins |

OPTIONAL: For corner NCTF SJ testability, these BGA pins (shown in the tables and in green color) can be connected to isolated motherboard test pads and not connected to motherboard VCC/VSS plane (refer to Figures 1 & 2 in MAS section 2.4). The disconnection is not a functional concern; however, it is desirable for the routing of the test pads to not cause a split in the planes.

Corner A67

| Pin Number | Pin Name | Description |
|------------|----------|-----------------|
| D67 | NCTFVSS | TP (Test Point) |
| C66 | NCTFVSS | TP (Test Point) |
| B64 | NCTFVSS | TP (Test Point) |
| A63 | NCTFVSS | TP (Test Point) |
| A61 | NCTFVSS | TP (Test Point) |
| H67 | NCTFVSS | TP (Test Point) |



- NCTF Package Corner
- NCTF Testable Pins

Corner DR1

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| DP5 | NCTFVSS | NCTF Testable Pins |
| DN4 | NCTFVSS | NCTF Testable Pins |
| DM2 | NCTFVSS | NCTF Testable Pins |
| DK1 | NCTFVSS | NCTF Testable Pins |

Note: For pinlist and ballmap information, refer to the **Package Ballout Mechanical Specification** document for this specific product.

Corner A1

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| C4 | NCTFVSS | NCTF Testable Pins |
| F1 | NCTFVSS | NCTF Testable Pins |
| C6 | NCTFVSS | NCTF Testable Pins |
| F3 | NCTFVSS | NCTF Testable Pins |



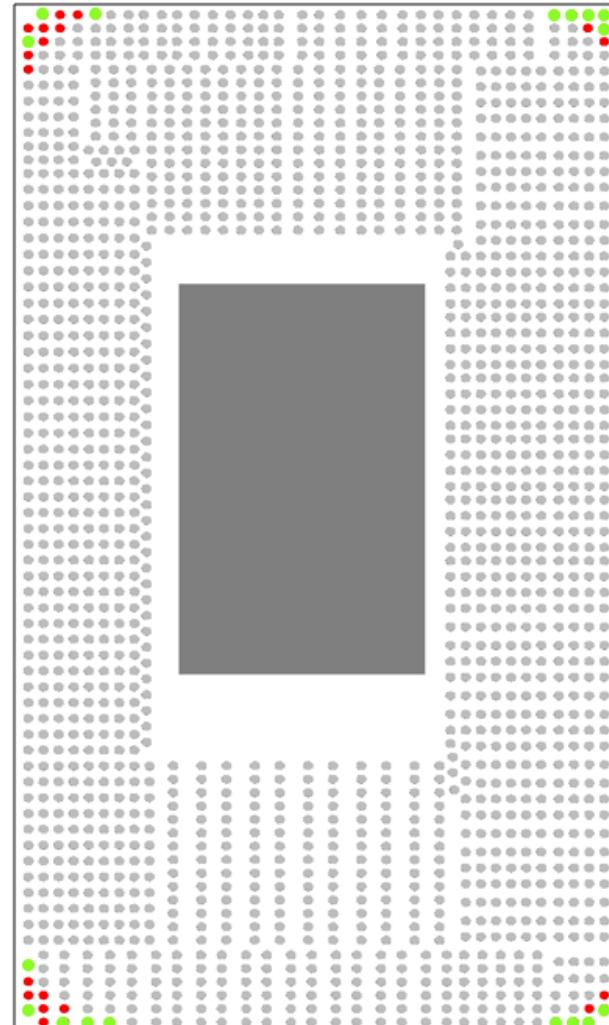
2.6 Processor Corner NCTF Test – PCB Routing Example

Tiger Lake H81 Processor Line

Corner CU41

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| CU40 | VSS | NCTF Testable Pins |
| CR41 | VSS | NCTF Testable Pins |
| CU36 | VSS | NCTF Testable Pins |

OPTIONAL: For corner NCTF SJ testability, these BGA pins (shown in the tables and in green color) can be connected to isolated motherboard test pads and not connected to motherboard VCC/VSS plane (refer to Figures 1 & 2 in MAS section 2.4). The disconnection is not a functional concern; however, it is desirable for the routing of the test pads to not cause a split in the planes.



- NCTF Package Corner
- NCTF Testable Pins

Corner CU1

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| CU2 | VSS | NCTF Testable Pins |
| CT1 | VSS | NCTF Testable Pins |
| CU3 | VSS | NCTF Testable Pins |
| CU4 | VSS | NCTF Testable Pins |
| CU5 | VSS | NCTF Testable Pins |
| CR1 | VSS | NCTF Testable Pins |
| CP1 | VSS | NCTF Testable Pins |
| CN1 | VSS | NCTF Testable Pins |
| CT2 | VSS | NCTF Testable Pins |

Note: For pinlist and ballmap information, refer to the **Package Ballout Mechanical Specification** document for this specific product.

Corner A41

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| B41 | VSS | NCTF Testable Pins |
| A39 | VSS | NCTF Testable Pins |
| A37 | VSS | NCTF Testable Pins |
| E41 | VSS | NCTF Testable Pins |
| A36 | VSS | NCTF Testable Pins |

Corner A1

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| A3 | VSS | NCTF Testable Pins |
| A4 | VSS | NCTF Testable Pins |
| A5 | VSS | NCTF Testable Pins |
| B2 | VSS | NCTF Testable Pins |
| C1 | VSS | NCTF Testable Pins |



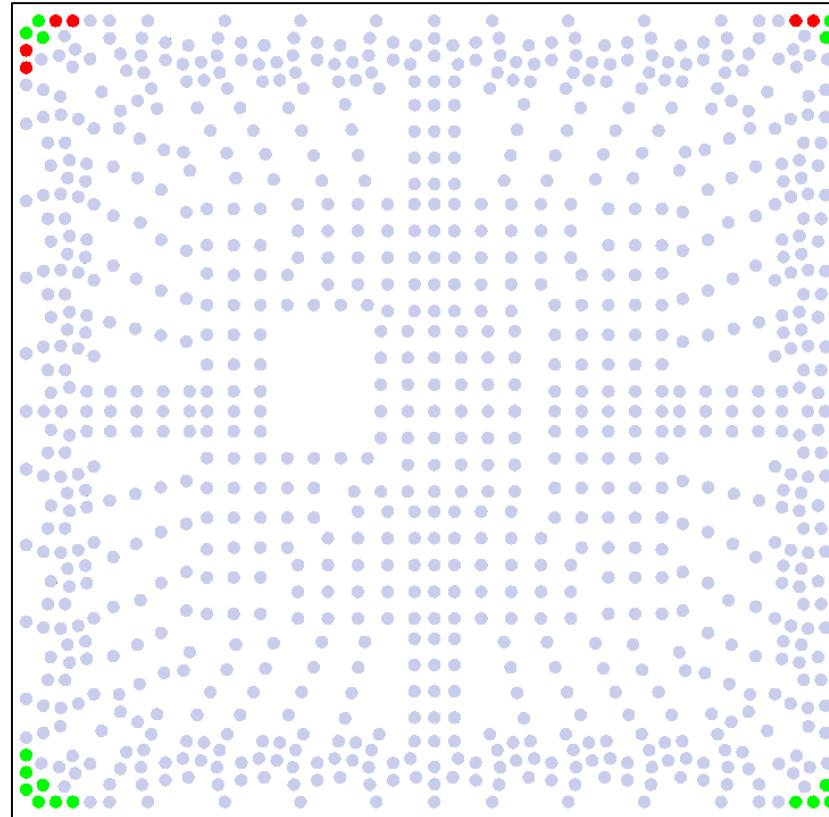
2.6 Processor Corner NCTF Test – PCB Routing Example

Tiger Lake PCH Processor Line

Corner BG49

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| BG48 | VSS | NCTF Testable Pins |
| BF49 | VSS | NCTF Testable Pins |
| BF48 | VSS | NCTF Testable Pins |

OPTIONAL: For corner NCTF SJ testability, these BGA pins (shown in the tables and in green color) can be connected to isolated motherboard test pads and not connected to motherboard VCC/VSS plane (refer to Figures 1 & 2 in MAS section 2.4). The disconnection is not a functional concern; however, it is desirable for the routing of the test pads to not cause a split in the planes.



- NCTF Package Corner
- NCTF Testable Pins

Corner BG1

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| BG2 | VSS | NCTF Testable Pins |
| BF1 | VSS | NCTF Testable Pins |
| BF2 | VSS | NCTF Testable Pins |

Note: For pinlist and ballmap information, refer to the **Package Ballout Mechanical Specification** document for this specific product.

Corner A49

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| A48 | VSS | NCTF Testable Pins |
| A47 | VSS | NCTF Testable Pins |
| A46 | VSS | NCTF Testable Pins |
| B49 | VSS | NCTF Testable Pins |
| B48 | VSS | NCTF Testable Pins |
| C49 | VSS | NCTF Testable Pins |
| D49 | VSS | NCTF Testable Pins |

Corner A1

| Pin Number | Pin Name | Description |
|------------|----------|--------------------|
| A2 | VSS | NCTF Testable Pins |
| A3 | VSS | NCTF Testable Pins |
| A4 | VSS | NCTF Testable Pins |
| B1 | VSS | NCTF Testable Pins |
| B2 | VSS | NCTF Testable Pins |
| C1 | VSS | NCTF Testable Pins |
| D1 | VSS | NCTF Testable Pins |

Module 3: Manufacturing Guidelines

Manufacturing with the Intel® Platform Code Named Tiger Lake

Overview – Table of Contents

| | | | | | | |
|--|--|--|--|------------------------------------|--|--|
| Module 1: <u>Component Attributes and Drawings</u> | Module 2: <u>Land Pattern (PCB Pad) Design Guidelines</u> | Module 3: <u>Manufacturing Guidelines</u> | Module 4: <u>Shipping & Handling</u> | Module 5: <u>Testing</u> | Module 6: <u>System Integration & ESD Considerations</u> | Module 7: <u>References</u> |
| 1.1 Package Attributes Intel® FCBGA Processors 1.2 Package Mechanical Drawings (PMD) FCBGA Processors 1.3 Package Attributes PCH 1.4 Package Mechanical Drawings (PMD) PCH | 2.1 Land Pattern Design Guidelines Introduction 2.2 Mother Board Cavity Voiding Requirements 2.3 Land Pattern Design Guidelines (for the different processors & chipset) | 3.1 Introduction 3.2 Example Package Dynamic Warpage Data 3.3 Critical SMT Recommendations 3.4 Manufacturing Guidelines General Info 3.5 Solder Paste Formulation Optimization 3.6 Solutions to Extend Stencil Aperture Area Ratio 3.7 Cu Core Standoff Technology 3.8 Solder Paste Volume Optimization Stencil Design Recommendations 3.9 SMT Reflow Pallet Recommendations 3.10 SMT Reflow Profile TC Location 3.11 Overview of Board Flexure 3.12 Board Level Adhesive Overview 3.13 Package Rework 3.14 FACR Prep Process | 4.1 Processor and Chipset Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements 4.4 BGA Package Handling BKMs 4.5 T&R Package Handling BKMs | 5.1 Test Information | 6.1 Introduction 6.2 Electro Static Discharge (ESD) Platform Component Goals 6.3 Electro Static Discharge (ESD) Design Guidelines 6.4 Electro Static Discharge (ESD) Additional Resources 6.5 Thermal Solution Assembly / Disassembly considerations | 7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Resource Design Center access Information |



Acronyms Found in this Module

| | |
|-------|---|
| Cu | Copper |
| CuOSP | Copper Organic Solderability Preservative |
| EDS | External Design Specification |
| FCBGA | Flip-Chip Ball Grid Array |
| HIMB | Hole In Mother Board |
| HT | High Temperature |
| MAS | Manufacturing Advantage Service |
| MB | Mother Board |
| MSL | Moisture Sensitivity Level |
| NCTF | Non-Critical to Function |
| PCH | Platform Control Hub |
| PDS | Product Datasheet |
| PMD | Package Mechanical Drawing |
| RIMB | Recess In Mother Board |
| RT | Room Temperature |
| T&R | Tape and Reel |
| TFT | Thermoform Tray |



3.1 Manufacturing Guidelines

Introduction

- Solder Joint Quality (SJQ) refers to the quality and robustness of the solder joints that are formed during the SMT process
- Robust solder joint formation / high SMT yields are a function of many SMT parameters, including...
 - Solder paste formulation, Solder paste volume (stencil design), Reflow profile / environment, PCB dynamic warpage (pallet use), package and mother board warpage, etc...
- An optimized SMT process, tooling, materials and handling have been demonstrated to result in acceptable SMT yields
- This MAS document includes SMT recommendations that have been developed specifically for the FCBGA components of this platform, to accommodate their unique package shape at room temp and high temp (reflow)
- Please also see the technical MAS: Manufacturing with Intel® FCBGA Components for Solder Joint Quality for a deeper training of warpage and solder joint formation fundamentals
- **Caution:** Corner bending could occur on FCBGA packages during tray and T&R handling which could impact package warpage expectations. As such, please follow the specific package handling recommendations found in Module 4 of this MAS.



3.2 Example Package Dynamic Warpage Data

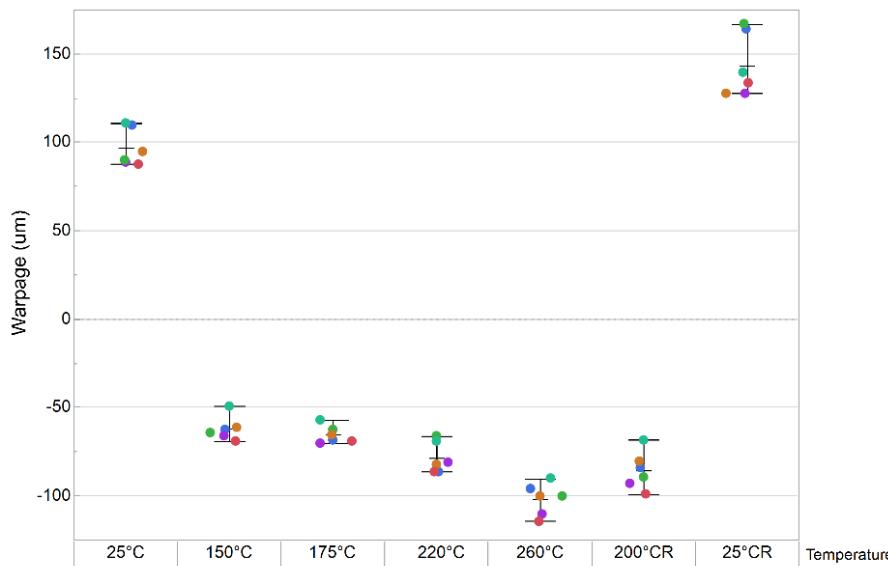
Tiger Lake UP3/H35 Processor Line

Measured: Warpage of the package BGA area through a temperature profile of 25°C, 150°C, 175°C, 220°C, 260°C, 200°C CR, 25°C CR.

Sample Size: 6 units

Summary of Results:

- **Max high-temperature¹ warpage is -112µm (~-4.4mils).**
- All samples have incoming convex shape.
- Transition from convex to concave for all samples is between 25°C and 150°C.



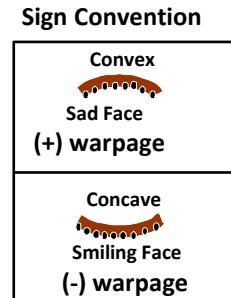
*Behavior due to stiffener (vs. package without stiffener) may include:

- Maximum high-temperature flatness at non-peak temperatures
- Variation from initial to room-temperature return
- More complicated shape at all temperatures

| Intel® TGL UP3/H35 Package Absolute Warpage by Temperature (°C) | | | | | | | |
|---|------|-------|-------|-------|-------|----------|---------|
| Unit ID | 25°C | 150°C | 175°C | 220°C | 260°C | 200°C CR | 25°C CR |
| 1 | 120 | -48 | -52 | -62 | -91 | -61 | 183 |
| 2 | 99 | -68 | -74 | -79 | -105 | -70 | 166 |
| 3 | 108 | -72 | -79 | -96 | -98 | -66 | 175 |
| 4 | 89 | -77 | -86 | -99 | -112 | -77 | 152 |
| 5 | 104 | -66 | -75 | -90 | -95 | -65 | 178 |
| 6 | 81 | -75 | -82 | -95 | -109 | -72 | 146 |

Note:

1. Preliminary reference information only. Refer to the PMD drawings in Module 1 for the expected high-temperature coplanarity range.
2. Same unit used for 150C, 175C and 220C; a separate unit used for 25C, 200Cr and 25Cr, and separate unit for 260C.
3. Intel is a trademark of Intel Corporation or its subsidiaries in the U.S. and/or other countries.





3.2 Example Package Dynamic Warpage Data

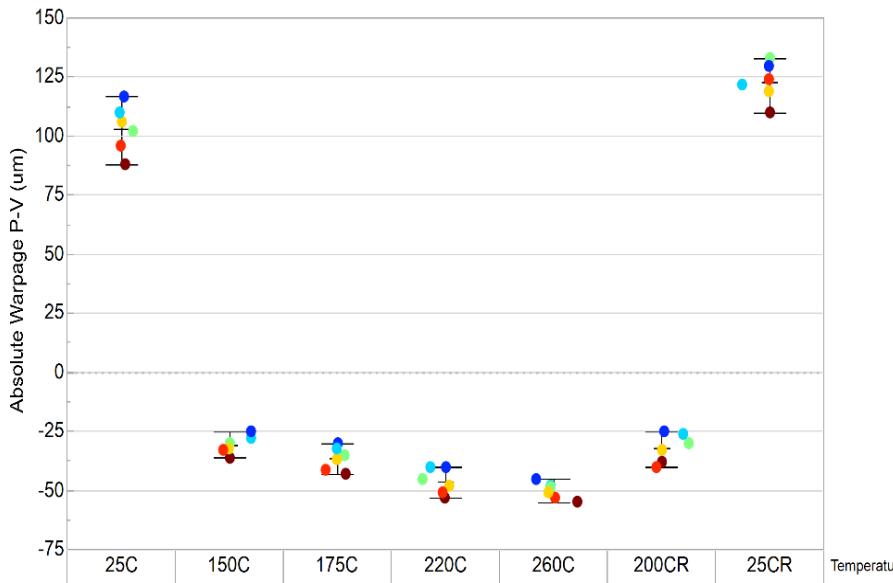
Tiger Lake UP4 Processor Line

Measured: Warpage of the package BGA area through a temperature profile of 25°C, 150°C, 175°C, 220°C, 260°C, 200°C CR, 25°C CR.

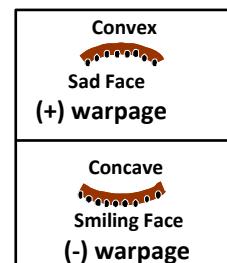
Sample Size: 6 units

Summary of Results:

- **Max high-temperature¹ warpage is $-55\mu\text{m}$ ($\sim-2.17\text{mils}$).**
- All samples have incoming convex shape.
- Transition from convex to concave for all samples is between 25°C and 150°C.



Sign Convention



*Behavior due to stiffener (vs. package without stiffener) may include:

- Maximum high-temperature flatness at non-peak temperatures
- Variation from initial to room-temperature return
- More complicated shape at all temperatures

| Intel® TGL UP4 Package Absolute Warpage by Temperature (°C) | | | | | | | |
|---|------|-------|-------|-------|-------|----------|---------|
| Unit ID | 25°C | 150°C | 175°C | 220°C | 260°C | 200°C CR | 25°C CR |
| 1 | 117 | -25 | -30 | -40 | -45 | -25 | 130 |
| 2 | 110 | -28 | -32 | -40 | -48 | -26 | 122 |
| 3 | 102 | -30 | -35 | -45 | -48 | -30 | 133 |
| 4 | 106 | -32 | -37 | -47 | -51 | -33 | 119 |
| 5 | 96 | -33 | -39 | -48 | -53 | -40 | 124 |
| 6 | 88 | -36 | -43 | -53 | -55 | -38 | 110 |

Note:

1. Preliminary reference information only. Refer to the PMD drawings in Module 1 for the expected high-temperature coplanarity range.
2. Same unit used for 150C, 175C and 220C; a separate unit used for 25C, 200Cr and 25Cr, and separate unit for 260C.
3. Intel is a trademark of Intel Corporation or its subsidiaries in the U.S. and/or other countries.



3.2 Example Package Dynamic Warpage Data

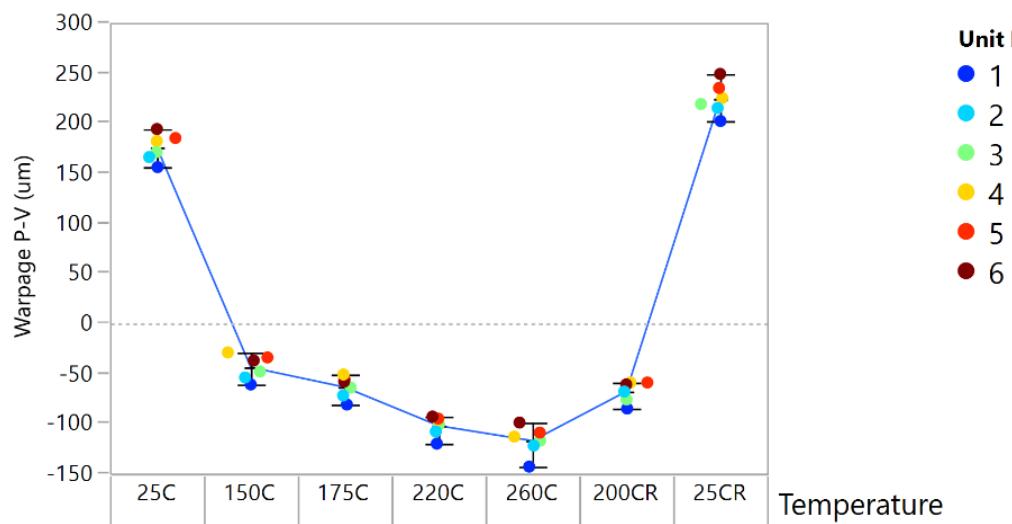
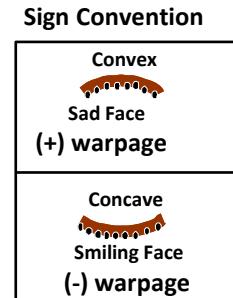
Tiger Lake H81 Processor Line

Measured: Warpage of the package BGA area through a temperature profile of 25°C, 150°C, 175°C, 220°C, 260°C, 200°C CR, 25°C CR.

Sample Size: 6 units

Summary of Results:

- **Max high-temperature¹ warpage is -143µm (~-5.6mils).**
- All samples have incoming convex shape.
- Transition from convex to concave for all samples is between 25°C and 150°C.



*Behavior due to stiffener (vs. package without stiffener) may include:

- Maximum high-temperature flatness at non-peak temperatures
- Variation from initial to room-temperature return
- More complicated shape at all temperatures

| Intel® TGL H81 Package Absolute Warpage by Temperature (°C) | | | | | | | |
|---|------|-------|-------|-------|-------------|---------|--------|
| Unit ID | 25°C | 150°C | 175°C | 220°C | 260°C | 200°C R | 25°C R |
| 1 | 156 | -61 | -81 | -120 | -143 | -85 | 202 |
| 2 | 166 | -54 | -72 | -108 | -122 | -68 | 215 |
| 3 | 171 | -48 | -64 | -101 | -117 | -76 | 219 |
| 4 | 182 | -29 | -51 | -96 | -113 | -59 | 225 |
| 5 | 185 | -34 | -56 | -95 | -109 | -59 | 235 |
| 6 | 194 | -37 | -58 | -93 | -99 | -61 | 249 |

Note:

1. Preliminary reference information only. Refer to the PMD drawings in Module 1 for the expected high-temperature coplanarity range.
2. Multiple sets of samples used: one set for 150C, 175C and 220C; a second set of separate units for 25C, 200CR and 25CR, and a third set of separate units for 260C.



3.2 Example Package Dynamic Warpage Data

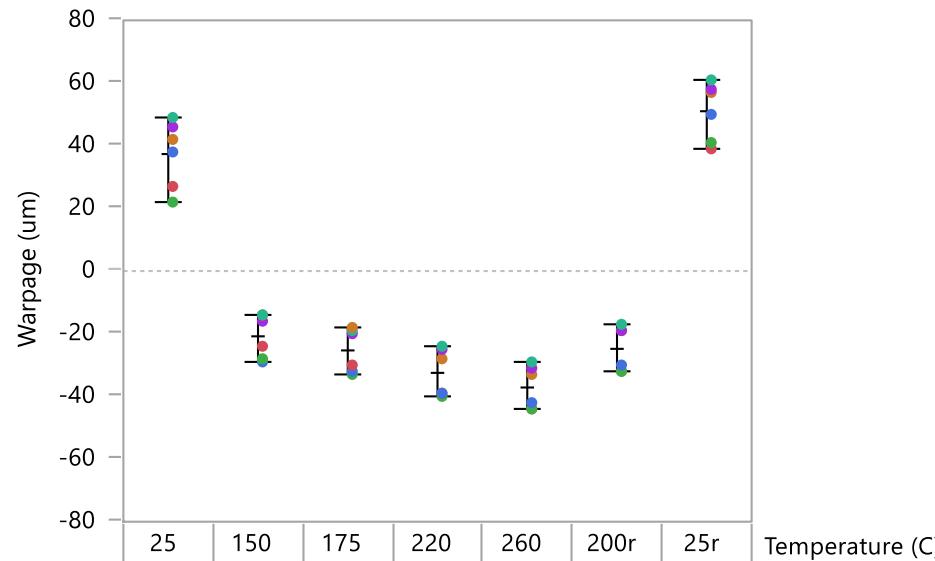
Tiger Lake PCH FCBGA

Measured: Warpage of the package BGA area through a temperature profile of 25°C, 150°C, 175°C, 220°C, 260°C, 200°C_{CR}, 25°C_{CR}.

Sample Size: 6 units

Summary of Results:

- **Max high-temperature¹ warpage is -44µm (~-1.7mils).**
- All samples have incoming convex shape.
- Transition from convex to concave for all samples is between 25°C and 150°C.



Sign Convention

| | |
|--|-----------------------------|
| | Convex |
| | Sad Face (+) warpage |
| | Concave |
| | Smiling Face (-) warpage |

| Intel® TGL PCH Package Absolute Warpage by Temperature (°C) | | | | | | | |
|---|------|-------|-------|-------|-------|---------------------|--------------------|
| Unit ID | 25°C | 150°C | 175°C | 220°C | 260°C | 200°C _{CR} | 25°C _{CR} |
| 1 | 27 | -24 | -30 | -39 | -44 | -32 | 39 |
| 2 | 22 | -28 | -33 | -40 | -44 | -32 | 41 |
| 3 | 38 | -29 | -32 | -39 | -42 | -30 | 50 |
| 4 | 42 | -14 | -18 | -28 | -33 | -19 | 57 |
| 5 | 49 | -14 | -19 | -24 | -29 | -17 | 61 |
| 6 | 46 | -16 | -20 | -25 | -31 | -19 | 58 |

Note:

1. Preliminary reference information only. Refer to the PMD drawings in Module 1 for the expected high-temperature coplanarity range.
2. Same unit used for 150C, 175C and 220C; a separate unit used for 25C, 200Cr and 25Cr, and separate unit for 260C.
3. Intel is a trademark of Intel Corporation or its subsidiaries in the U.S. and/or other countries.



3.3 Critical SMT Recommendations (SAC Process)

| Parameter | Recommendations for Customer Evaluation | |
|--|--|---|
| Moisture | | |
| Moisture Sensitivity Level (MSL) | MSL3 | |
| Solder Paste Print | | |
| Intel Evaluated Solder Pastes | Refer to Intel Evaluated Solder Pastes | |
| Stencil Thickness & Aperture Design | Refer to stencil design recommendations | |
| Pick and Place (PnP) | | |
| Component Placement | 100% ball recognition | |
| Reflow | | |
| Reflow Pallets | Refer to SMT Reflow Pallet Recommendations | |
| Reflow Profile | Reflow Ambient | N_2 ($O_2 \leq 3000$ PPM). Air is acceptable but not recommended. ➤ Recommend N_2 ($O_2 < 3000$ PPM) reflow only for TGL UP4 package |
| | Rising (+) and Falling (-) Ramp Rate | ≤ 3 °C/second |
| | Soak Temp and Time | Paste Dependent. Follow paste manufacturer's requirements |
| | Time Above ≥ 220 °C | 60-90 Seconds for Air reflow 40-90 seconds for N_2 ($O_2 \leq 3000$ PPM) reflow |
| | Solder Joint Peak Reflow Temp | 240 ± 5 °C recommended (do not exceed 250°C) |
| | Maximum Body and Substrate Temp | ≤ 250 °C. Never exceed 260°C |
| | Component Delta T (ΔT) | Control ΔT across component to ≤ 10 °C for uniform heating |

Notes:

- Except for body temp, all temperatures are measured with thermo-couples inside solder joints, for increased accuracy.
- This is Intel's reflow reference process practices and parameters are provided for reference purposes only, based on internal studies, and are not necessarily optimized. Mfg. processes are unique and may require unique solutions to ensure an acceptable level of quality, reliability, and mfg yield. Due to the differences in equipment and materials, process parameter modifications may be required to meet customer's quality, reliability, and manufacturing yield requirements.
- Disclaimer: These results are provided for informational purposes only. Any sourcing decision is solely at the discretion of the Customer. Intel neither warrants, nor makes any representation whatsoever as to any supplier's products, including its availability, suitability, and reliability for the application for which this information is provided. Other pastes not listed above may perform better or worse based on customer SMT / board characteristics.
- *Other names and brands may be claimed as the property of others.



3.4 Manufacturing Guidelines

General Information

- Intel believes that following the process & material parameter recommendations outlined in IPC7095C* and in this module may be required to achieve acceptable SMT yields.
 - Solder paste formulation and solder paste volume optimization are the two most effective ways to mitigate solder joint formation defects.
 - Intel has performed a higher level of SJQ characterization on the FCBGAs and this module contains the recommended solder paste formulations and stencil designs.
 - Intel recognizes customer needs to optimize SMT yield across the entire motherboard and its components. This module serves to provide a starting guide for customers, and final optimization is specific to each customer design and process considerations
- Intel believes that following the process & material parameter recommendations in this module may be required to achieve acceptable SMT yields.

Failure to implement the recommendations in this module can lead to higher than expected SMT yield loss

Notes:

- See the [Manufacturing with Intel® FCBGA Components for Solder Joint Quality MAS](#) for deeper training of warpage fundamentals.
- *Other names and brands may be claimed as the property of others.



3.5 Solder Paste Formulation Optimization (SAC Process)

An extreme SMT stress test was performed on multiple solder paste formulations, to force SMT failures and evaluate SMT yield performance on FCBGA packages.

- Solder Pastes included three types: Halogenated (H), Low Halogen (LH), Zero Halogen (ZH).

Definitions¹:

Halogenated (H): No limit to the content of Chlorine or Bromine (>900 ppm Bromine or Chlorine; >1500 ppm total halogen), either as ions or in elemental form, in the flux of the solder paste.

Low Halogen² (LH): Chlorine or Bromine content is <900 ppm and total combined amount of Chlorine or Bromine <1500 ppm total halogen in the flux of the solder paste.

Zero Halogen (ZH): Chlorine or Bromine not intentionally added to the flux of the solder paste and both would register as non-detectable by current testing methods.

- SMT Yield % is based on T=0 solder joint defects from e-test & Failure Analysis (i.e. NWO, HoP, Bridging).

SMT Stress Test Conditions

- Packages:**
 - FCBGA test packages with a warpage distribution.
- SMT Parameters:**
 - Double sided reflow was simulated by reflowing the unpopulated PCB inverted in a pallet.
 - Forced low solder paste volume at NCTF corners (1:1 / no over-print).
 - Air reflow environment, Time Above $\geq 220^{\circ}\text{C}$ 60-70 seconds, Peak Reflow Temperature $240^{\circ}\text{C} \pm 5^{\circ}\text{C}$.
 - PCB surface finish was OSP.
- Success Criteria: Minimum yield of 80% required.**

¹Disclaimer: These results are provided for informational purposes only. Any sourcing decision is solely at the discretion of the Customer. Intel neither warrants, nor makes any representation whatsoever as to any supplier's products, including its availability, suitability, and reliability for the application for which this information is provided. Other pastes not listed above may perform better or worse based on customer SMT / board characteristics.

²Disclaimer: Low Halogen: Applies only to brominated and chlorinated flame retardants (BFRs/CFRs) and PVC in the final product. Intel® components as well as purchased components on the finished assembly meet JS-709 requirements, and the PCB/Substrate meet IEC 61249-2-21 requirements. The replacement of halogenated flame retardants and/or PVC may not be better for the environment.



3.5 Solder Paste Formulation Optimization (SAC Process)

All of the solder paste formulations below have passed Intel's SMT stress testing and are recommended for customer evaluation with FCBGA packages, to achieve acceptable SMT Yields.

| Intel Evaluated Solder Pastes (in alphabetical order) | Type ¹ |
|--|-------------------|
| Alpha OM364* | Zero Halogen (ZH) |
| Indium 10.8HF* | Zero Halogen (ZH) |
| Senju M705-S101HF(N4)-S4* | Low Halogen (LH) |
| Shenmao PF606-P* | Halogenated (H) |
| Shenmao PF606-P26* | Zero Halogen (ZH) |
| Yunnan Tin YW9-3005-98CY04* | Low Halogen (LH) |

Notes:

- See the [Manufacturing with Intel® FCBGA Components for Solder Joint Quality MAS](#) for deeper training of warpage fundamentals and information on solder paste performance testing.
- Disclaimer: These results are provided for informational purposes only. Any sourcing decision is solely at the discretion of the Customer. Intel neither warrants, nor makes any representation whatsoever as to any supplier's products, including its availability, suitability, and reliability for the application for which this information is provided. Other pastes not listed above may perform better or worse based on customer SMT / board characteristics.
- *Intel, Intel® Core™ Processors, and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries. Other names and brands may be claimed as the property of others.
- ¹Solder Flux Types:
 - Halogenated (H) - No limit to the content of Chlorine or Bromine (>900 ppm Bromine or Chlorine; >1500 ppm total halogen), either as ions or in elemental form, in the flux of the solder paste.
 - Low Halogen (LH) - Chlorine or Bromine content is <900 ppm and total combined amount of Chlorine or Bromine <1500 ppm total halogen in the flux of the solder paste.
 - Zero Halogen (ZH) - Chlorine or Bromine not intentionally added to the flux of the solder paste and both would register as non-detectable by current testing methods.
 - These are common definitions from solder paste suppliers and not Intel's definition



3.6 Solutions to Extend Stencil Aperture Area Ratio

Intel has been working to extend the stencil aperture area ratio (from 0.66 down to 0.50)

Benefits of stencil aperture area ratio extension:

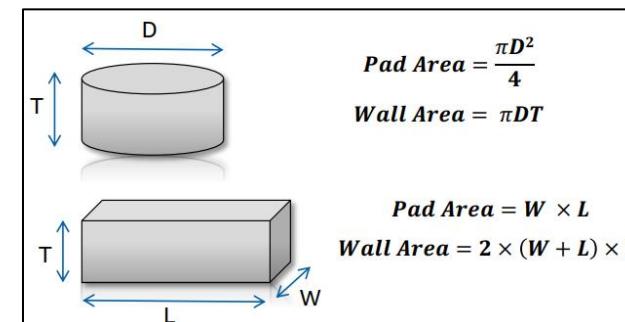
- Increased SMT yield margin for FCBGA Packages
- Supports manufacturability of next generation $\leq 0.35\text{mm}$ pitch packages
- Provides the ability to optimize (i.e. reduce) stencil opening for solder bridge defect reduction
- Reduced PCB print cleaning and rework rate

IPC-7525B* and IPC-7095D* specification provides guideline on the technology solutions to extend the stencil aperture area ratio down to 0.50

The upcoming slides share information & recommendations based on internal and industry data collection activities to extend the stencil aperture area ratio

$$\text{Stencil Aperture Area Ratio} = \frac{\text{Pad Area}}{\text{Wall Area}}$$

Optimal stencil design is critical to ensure consistent release of solder paste (transfer rate) from stencil openings





3.6 Solutions to Extend Stencil Aperture Area Ratio

Current industry standard is Laser Cut stencil + Type 4 solder paste (AR from 0.66 to 0.58)

Based on internal and industry activities, the following technology solutions, shown in the table below, are recommended to enable a stencil print process with stencil aperture area ratio below AR 0.66 [1, 2]

- Nano Laser Cut stencil (coated) + Type 4 solder paste (AR from 0.66 to 0.56)
- Laser Cut stencil + Type 5 solder paste (AR from 0.66 to 0.54)
- Nano Laser cut stencil (coated) + Type 5 solder paste (AR from 0.66 to 0.52)

| Stencil Area Ratio | LC + T4 (Current Industry standard) | NLC + T4 | LC + T5 | NLC + T5 |
|--------------------|--|----------|---------|----------|
| Area Ratio_0.66 | | | | |
| Area Ratio_0.65 | | | | |
| Area Ratio_0.63 | | | | |
| Area Ratio_0.60 | | | | |
| Area Ratio_0.58 | | | | |
| Area Ratio_0.56 | | | | |
| Area Ratio_0.54 | | | | |
| Area Ratio_0.52 | | | | |
| Area Ratio_0.50 | | | | |
| Area Ratio_0.48 | | | | |

Legend:

AR: Area Ratio

LC: Laser cut stencil (uncoated)

NLC: Nano Laser cut stencil (coated)

T4: Type 4 solder paste

T5: Type 5 solder paste

C_p: Process Capability

TE: Transfer Efficiency

CV: Coefficient of Variation

Table Color Legend. Green: Three evaluation criteria's ($C_p \geq 1.33$, $TE \geq 70\%$, $CV \leq 15\%$) were met
Orange: Didn't meet all of the evaluation criteria's

[1] Aravamudhan et al., "Stencil Aperture Area Ratio Extension: Impact of Stencil Technology, Solder Paste Chemistry & Solder Particle Size", SMTA* Conference, 2017

[2] Chang et al., "Stencil Aperture Area Ratio Extension- Impact of Stencil Technology and Coating" SMTA* China East Conference, Shanghai, PR China, 2017



3.6 Solutions to Extend Stencil Aperture Area Ratio

Solder Paste Recommendation:

5 different brands of Type 5 solder paste were tested and there were no difference in performance found across them, in extending the stencil aperture area ratio

Type 5 solder paste provides the ability to pack more solder paste powder into a smaller aperture size than Type 4 solder paste

| Powder Size | Max Powder Size | Min Stencil Opening |
|---------------------|-----------------|---------------------|
| Type 4 (38 to 20um) | 38um | 190um (7.5mils) |
| Type 5 (25 to 15um) | 25um | 125um (5.0mils) |

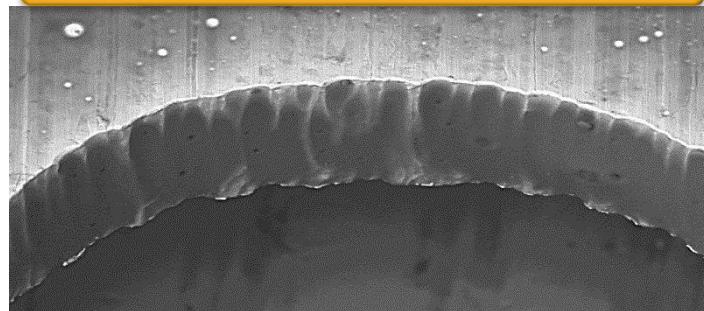
3.6 Solutions to Extend Stencil Aperture Area Ratio

Nano Coat Laser cut stencil Recommendation:

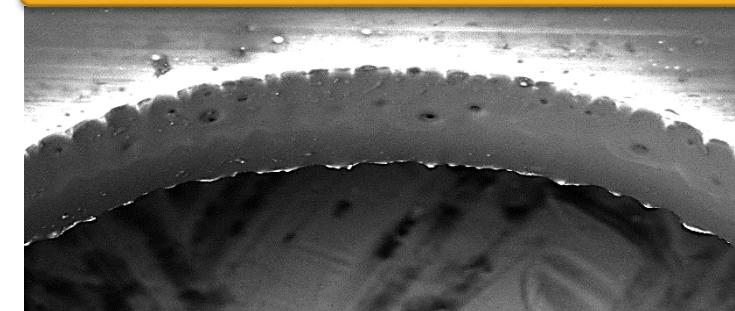
It is highly recommended to use a nano coat technology which is only applied by a spray + cure process

- Need to ensure the nano coat covers all stencil aperture wall surfaces
- Nano coated (spray + cure process) stencils with smooth wall finish (i.e. less surface roughness) helps to minimize the friction between solder paste and stencil walls, which in turn helps the paste to release from stencil walls with improved consistency
- Spray + cure process provides higher stencil cleaning life for stencil coating (using a stencil cleaning agent with pH ≤ 11 will help maintain the coating on stencil aperture walls)

LC: Laser Cut Stencil (uncoated)



NLC: Nano Laser Cut Stencil (coated)



ALERT: The data collection shows that a manual wipe-on coat process does not provide any benefits to extend the stencil aperture area ratio

Please contact your solder paste supplier and/or stencil supplier for technical solutions to extend your stencil aperture area ratio



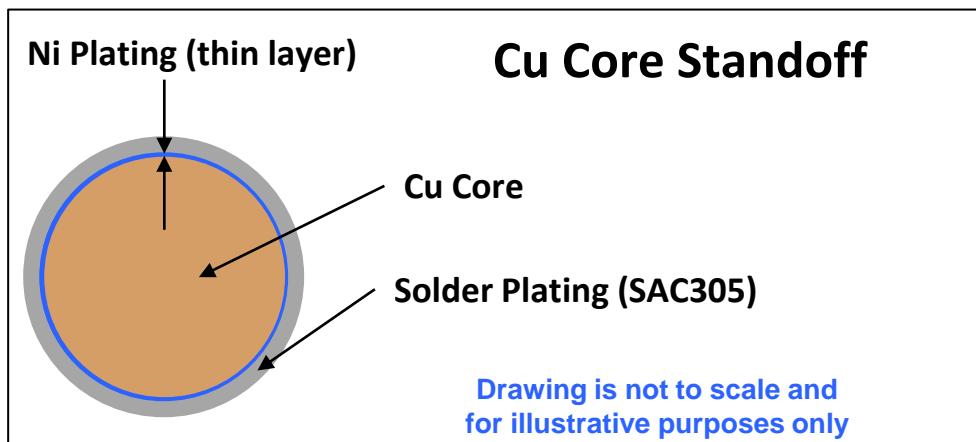
3.7 Cu Core Standoff Technology

Benefits:

- Cu Core solderballs are used for standoff purpose only, for SMT yield improvement serving as package collapse limiters (during SMT reflow) providing additional margin to prevent SBB (Solder Ball Bridging) defects

Cu Core Information:

- Cu Core standoffs are placed in all 4 corner NCTF (Non Critical to Function) pin locations, thus no risk for loss in electrical or mechanical integrity for the Processor
- Incoming Cu Core Ball size = 340um (13.4 mil), Core size = 305um (12 mil)
- Cu Core solder plating alloy = SAC305 (Note: All other solderballs are SAC405)



Factory Considerations:

- Reflow:** There are no reflow profile temperature differences between SAC305 & SAC405 solderballs
- Pick & Place:** Optimize the PnP machine vision settings to not reject the specific Cu Core ball locations
- X-Ray:** Train all factory engineers, operators, and automated X-Ray tools to not reject the specific Cu Core standoff locations

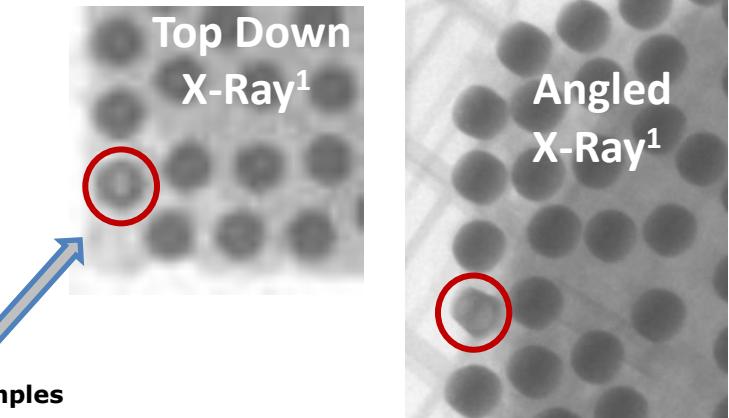
CAUTION: Cu Core standoffs appear to have >25% voids at x-ray but the Cu Core is not a void, this is normal -> Do not reject them!

See Module 1 for specific package Cu Core Standoff Locations

Example Cu Core: Cross Section Image



Example Cu Core: X-Ray Images



¹Images shown are not TGL packages and not from the same samples



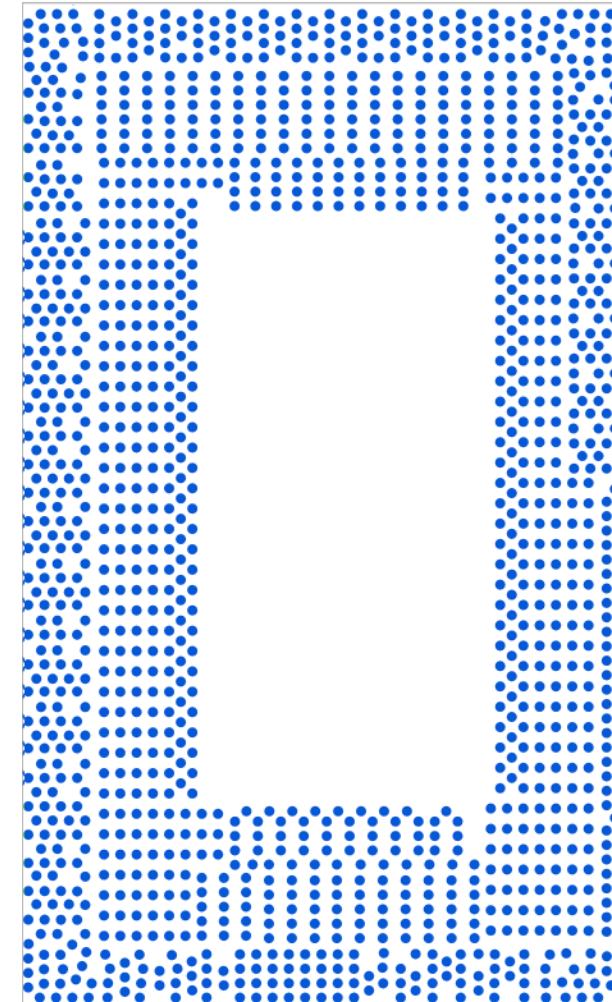
3.8 Solder Paste Volume Optimization

Stencil Design Recommendations (SAC Process)

Tiger Lake UP3/H35 FCBGA Processor Line – 4 mil option

| Stencil Thickness: 102 µm (4 mils) option | | | |
|--|-------------------|----------------------------------|------------|
| Stencil Air Gap Design : ≥ 192 µm (7.5 mils) | | | |
| Stencil Design (Aperture) | Over- printing | Solder Paste Volume Target | Area Ratio |
| BGA Pads • Round 457 µm (18 mils) | Yes | 0.0167 cu. mm (1018 cu. mils) | 1.13 |

- Notes:
- Reference Information Only.
 - Design stencil opening to meet the theoretical volume requirements (above).
 - Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
 - Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





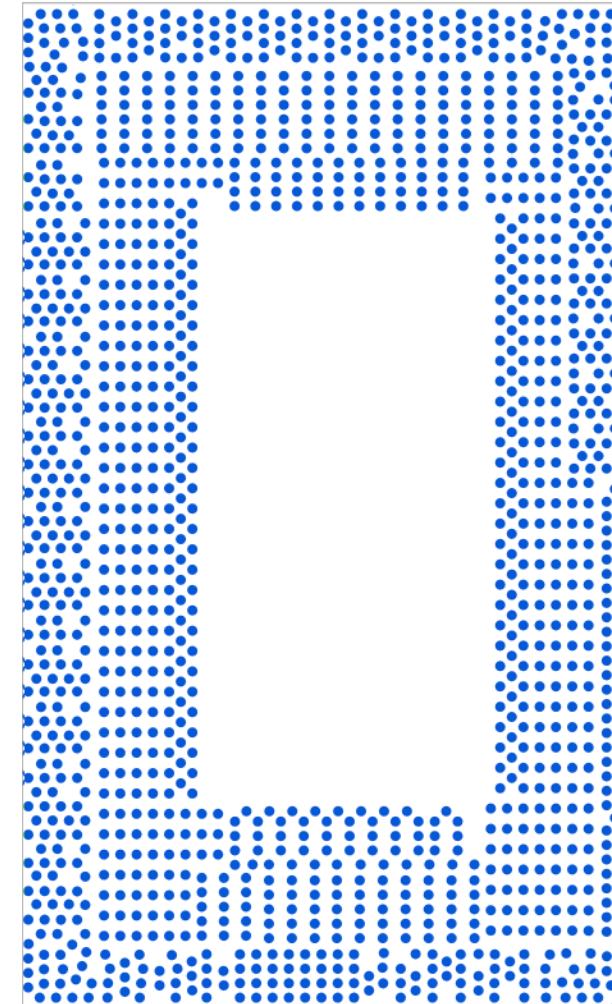
3.8 Solder Paste Volume Optimization

Stencil Design Recommendations (SAC Process)

Tiger Lake UP3/H35 FCBGA Processor Line – 5 mil option

| Stencil Thickness: 127 µm (5 mils) option | | | |
|--|-------------------|----------------------------------|------------|
| Stencil Air Gap Design : ≥ 240 µm (9.5 mils) | | | |
| Stencil Design (Aperture) | Over- printing | Solder Paste Volume Target | Area Ratio |
| BGA Pads • Round 409 µm (16.1 mils) | Yes | 0.0167 cu. mm (1018 cu. mils) | 0.81 |

- Notes:
- Reference Information Only.
 - Design stencil opening to meet the theoretical volume requirements (above).
 - Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
 - Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





3.8 Solder Paste Volume Optimization

Stencil Design Recommendations (SAC Process)

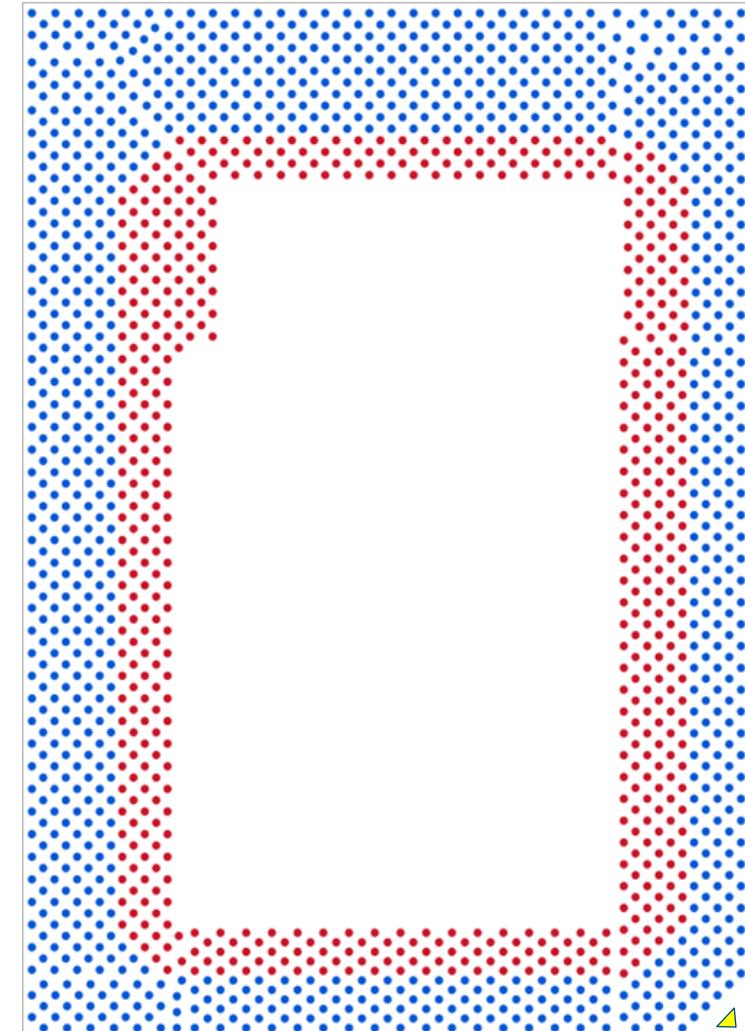
Tiger Lake UP4 FCBGA Processor Line – 3 mil option

| Stencil Thickness: 76 µm (3 mils) | | | |
|---|-------------------|---------------------------------|------------|
| Stencil Air Gap Design : ≥ 133 µm (5.25 mils) | | | |
| Stencil Design (Aperture) | Over- printing | Solder Paste Volume Target | Area Ratio |
| BGA Pads • Round 267 µm (10.5 mils) | Over | 0.0043 cu. mm (260 cu. mils) | 0.88 |
| • Round 241 (9.5 mils) | Under | 0.0035 cu. mm (213 cu. mils) | 0.79 |

For Reflow Ambient, Recommend N₂ (O₂ ≤3000 PPM) reflow
only for TGL UP4 package

Notes:

- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
- Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





3.8 Solder Paste Volume Optimization

Stencil Design Recommendations (SAC Process)

Tiger Lake UP4 FCBGA Processor Line – 4 mil option

Stencil Thickness: **102 µm (4 mils)**

Stencil Air Gap Design : $\geq 133 \mu\text{m}$ (5.25 mils)

| Stencil Design (Aperture) | Over- printing | Solder Paste Volume Target | Area Ratio |
|--|-------------------|---------------------------------|-------------------|
| BGA Pads • Round 267 μm (10.5 mils) | Over | 0.0057 cu. mm (346 cu. mils) | 0.66 |
| • Round 241 (9.5 mils) | Under | 0.0046 cu. mm (284 cu. mils) | 0.59 ¹ |

¹To improve print process capability below 0.66 area ratio, a Laser Cut stencil with Nano Coat stencil technology is recommended, and/or using Type 5 solder paste

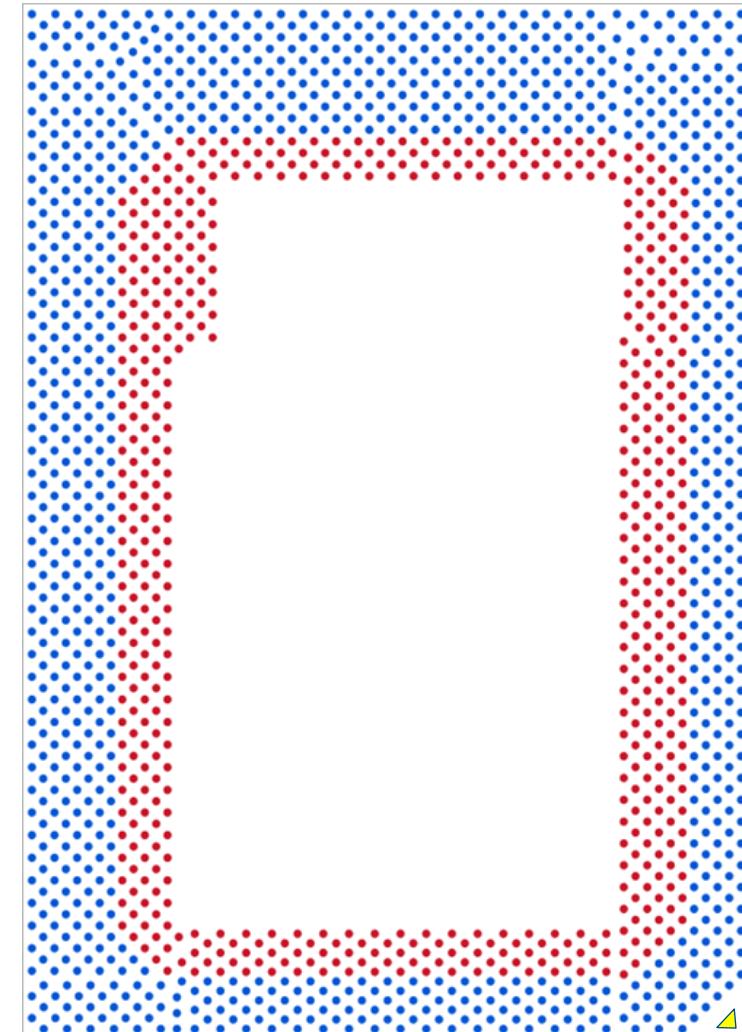
For optimal stencil printing performance with Nano Coat stencil technology, it is highly recommended to ensure the coating is applied to aperture walls (example application techniques; Spray + Cure process, Dip + Casting process)

CAUTION: For Nano Coat stencil technology where the coating is applied only to the underside of the stencil and not covering the aperture walls (example application techniques; manual wipe-on coating process), this method was shown to **not provide** any area ratio improvement benefits

For Reflow Ambient, Recommend N₂ (O₂ \leq 3000 PPM) reflow
only for TGL UP4 package

Notes:

- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
- Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





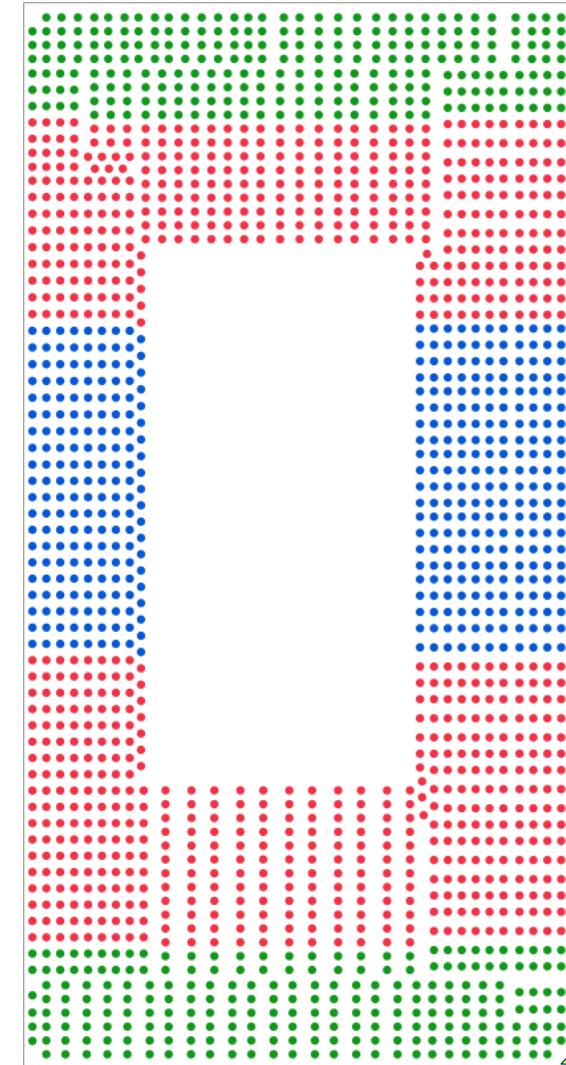
3.8 Solder Paste Volume Optimization

Stencil Design Recommendations (SAC Process)

Tiger Lake H81 FCBGA Processor Line – 4 mil option

| Stencil Thickness: 102 µm (4 mils) option | | | |
|--|---------------|----------------------------------|------------|
| Stencil Air Gap Design : ≥ 180 µm (7.09 mils) | | | |
| Stencil Design (Aperture) | Over-printing | Solder Paste Volume Target | Area Ratio |
| BGA Center Pads ● Round 355 µm (14.0 mils) | Yes | 0.0101 cu. mm (615 cu. mils) | 0.88 |
| BGA Corner Pads ● Round 470 µm (18.5 mils) | Yes | 0.0176 cu. mm (1076 cu. mils) | 1.16 |
| BGA Body Pads ● Round 432 µm (17.0 mils) | Yes | 0.0149 cu. mm (908 cu. mils) | 1.06 |

- Notes:
- Reference Information Only.
 - Design stencil opening to meet the theoretical volume requirements (above).
 - Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
 - Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





3.8 Solder Paste Volume Optimization

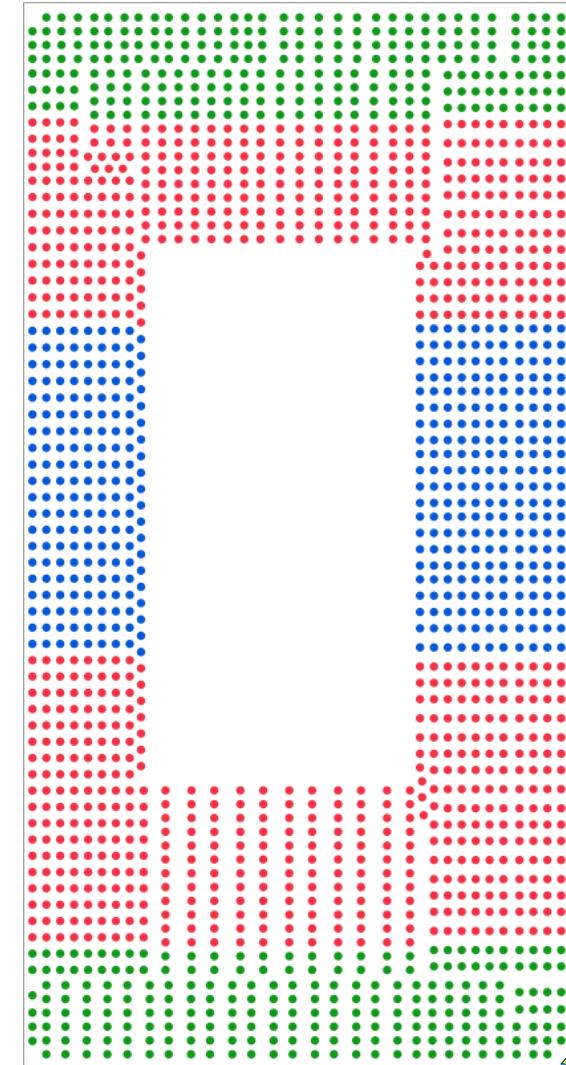
Stencil Design Recommendations (SAC Process)

Tiger Lake H81 FCBGA Processor Line – 5 mil option

| Stencil Thickness: 127 µm (5 mils) option | | | |
|--|---------------|----------------------------------|------------|
| Stencil Air Gap Design : ≥ 180 µm (7.09 mils) | | | |
| Stencil Design (Aperture) | Over-printing | Solder Paste Volume Target | Area Ratio |
| BGA Center Pads ● Round 355 µm (14.0 mils) | Yes | 0.0126 cu. mm (767 cu. mils) | 0.70 |
| BGA Corner Pads ● Round 470 µm (18.5 mils) | Yes | 0.0220 cu. mm (1345 cu. mils) | 0.93 |
| BGA Body Pads ● Round 432 µm (17.0 mils) | Yes | 0.0186 cu. mm (1135 cu. mils) | 0.85 |

Notes:

- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
- Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





3.8 Solder Paste Volume Optimization

Stencil Design Recommendations (SAC Process)

Tiger Lake PCH FCBGA Processor Line – 4 mil option

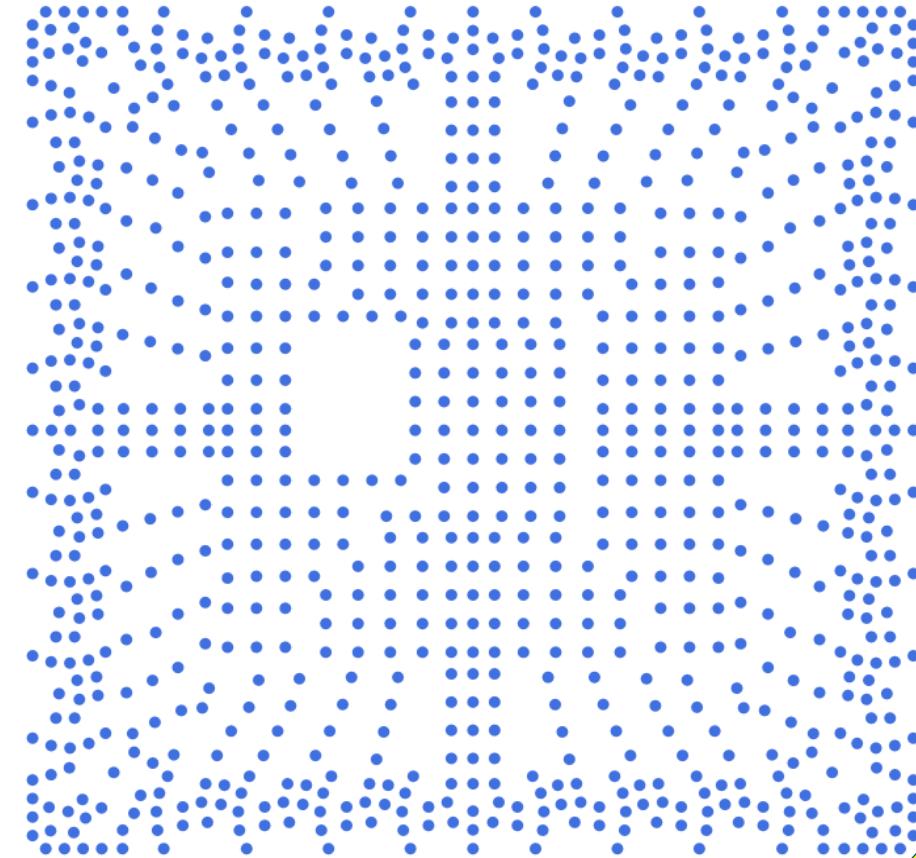
Stencil Thickness: **102 µm (4 mils) option**

Stencil Air Gap Design : $\geq 152 \mu\text{m}$ (6.0 mils)

| Stencil Design (Aperture) | Over- printing | Solder Paste Volume Target | Area Ratio |
|---|-------------------|---------------------------------|------------|
| All Pads • Round 348 μm (13.7 mils) | Yes | 0.0097 cu. mm (590 cu. mils) | 0.86 |

Notes:

- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
- Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





3.8 Solder Paste Volume Optimization

Stencil Design Recommendations (SAC Process)

Tiger Lake PCH FCBGA Processor Line – 5 mil option

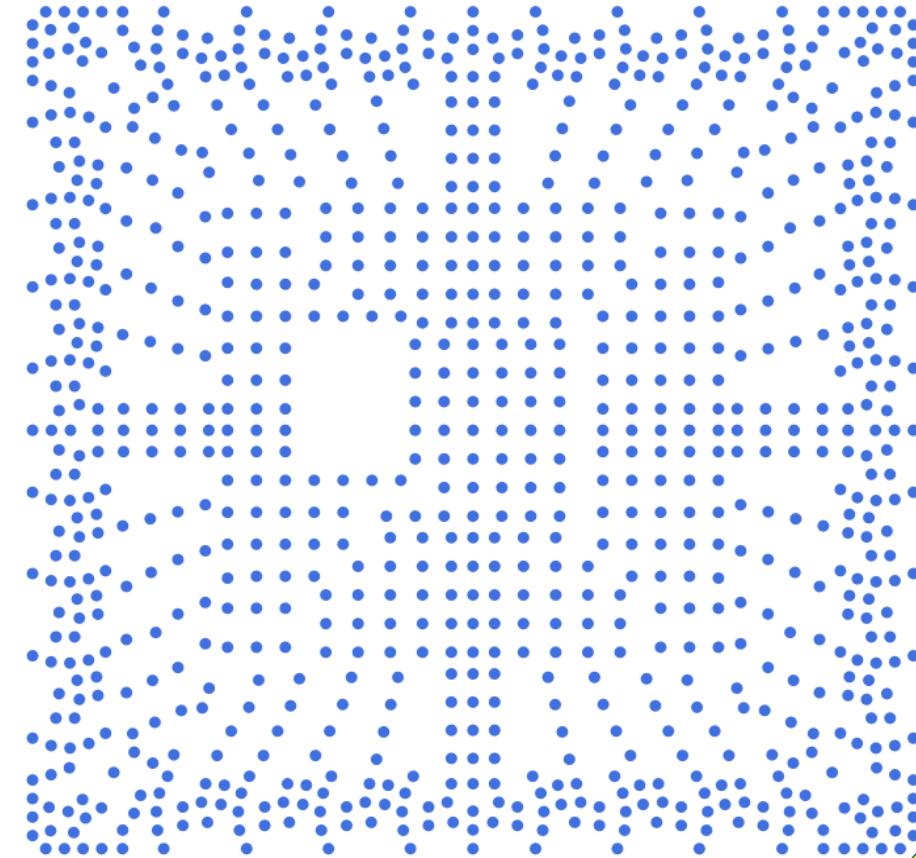
Stencil Thickness: **127 µm (5 mils) option**

Stencil Air Gap Design : $\geq 183 \mu\text{m}$ (7.2 mils)

| Stencil Design (Aperture) | Over- printing | Solder Paste Volume Target | Area Ratio |
|---|-------------------|---------------------------------|------------|
| All Pads • Round 317.5 μm (12.5 mils) | Yes | 0.0101 cu. mm (614 cu. mils) | 0.63 |

Notes:

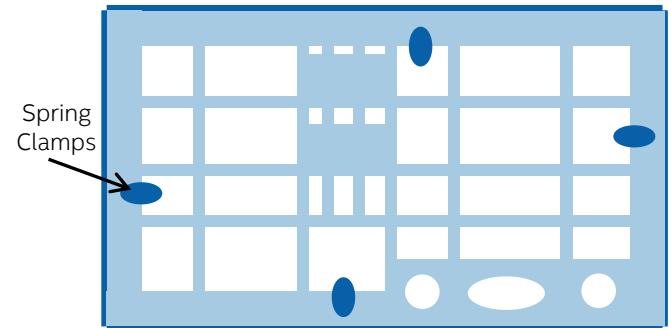
- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
- Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





3.9 SMT Reflow Pallet Recommendations

- **Background:** Pallets are typically used during SMT to keep the board “flat” to improve yield and/or to protect key components.
- **Intel Recommendations:**
 1. Use a pallet for all reflow processes.
 2. Support board across the span to prevent sagging at high temperatures.
 3. Top of board height = top of pallet height (within tolerance ranges)
 4. Provide adequate clearance for thermal expansion of the PCB during reflow: 1mm (min) clearance from all board edges.
 5. Use edge low force spring clamps around the perimeter of the PCB.
 6. Evaluate the product board design to understand high-temperature flatness. See *IPC 9641 High Temperature Printed Board Flatness Guideline* for additional information.



Example Depiction of Pallet Design with Four Spring Clamps and adequate PCB span support



Example of Spring Clamp: (a)
Without Board and (b)
Clamping a Board

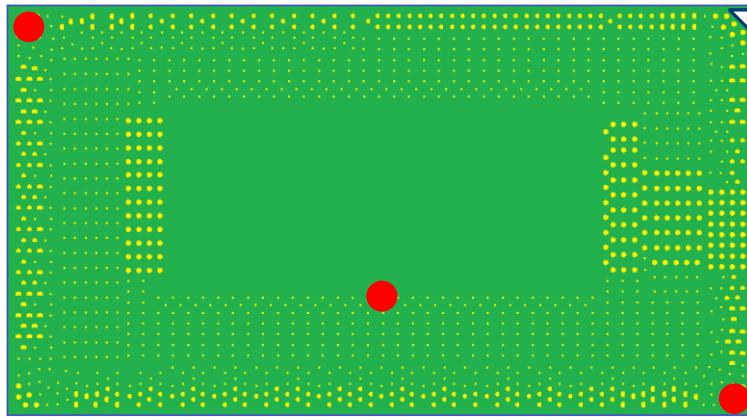
Minimizing board warpage to <50 µm (<2 mils) in the FCBGA area during reflow is strongly recommended. The use of a pallet¹ is one minimizing approach.

¹Results may vary by pallet and board design features: Use of spring clamps, material type, unsupported spans near land area, etc.

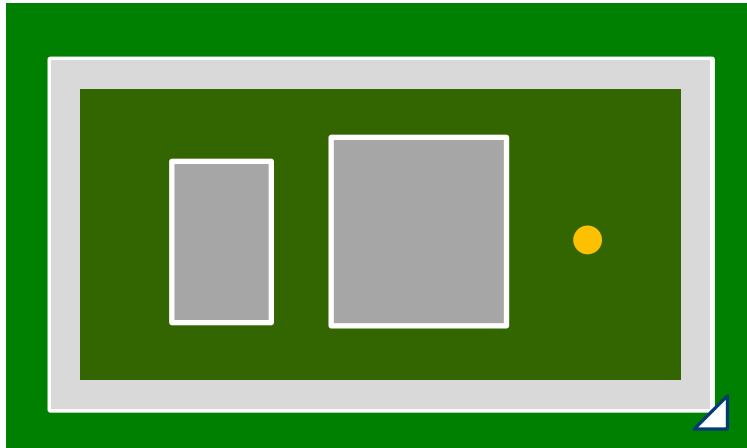


3.10 SMT Reflow Profiling Thermocouple (TC) Location Recommendations

Tiger Lake UP3/H35 Processor Line



- Thermocouple attached to solder joint
- Thermocouple attached to substrate



| Recommended Thermocouple Locations ¹ | |
|---|-----------------|
| 1 | FCBGA Corner |
| 2 | FCBGA Center |
| 3 | FCBGA Corner |
| 4 | FCBGA Substrate |

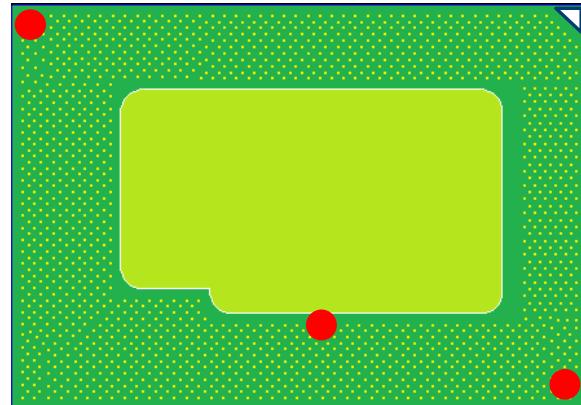
Note:

- ¹Customers are recommended to select thermocouple locations based on their mother board thermal mass.

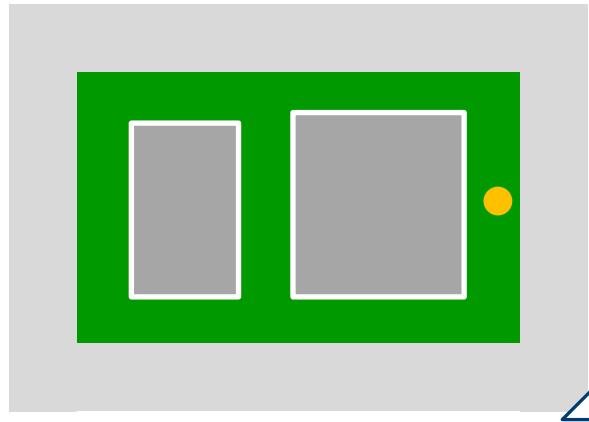


3.10 SMT Reflow Profiling Thermocouple (TC) Location Recommendations

Tiger Lake UP4 Processor Line



- Thermocouple attached to solder joint
- Thermocouple attached to substrate



| Recommended Thermocouple Locations ¹ | |
|---|-----------------|
| 1 | FCBGA Corner |
| 2 | FCBGA Center |
| 3 | FCBGA Corner |
| 4 | FCBGA Substrate |

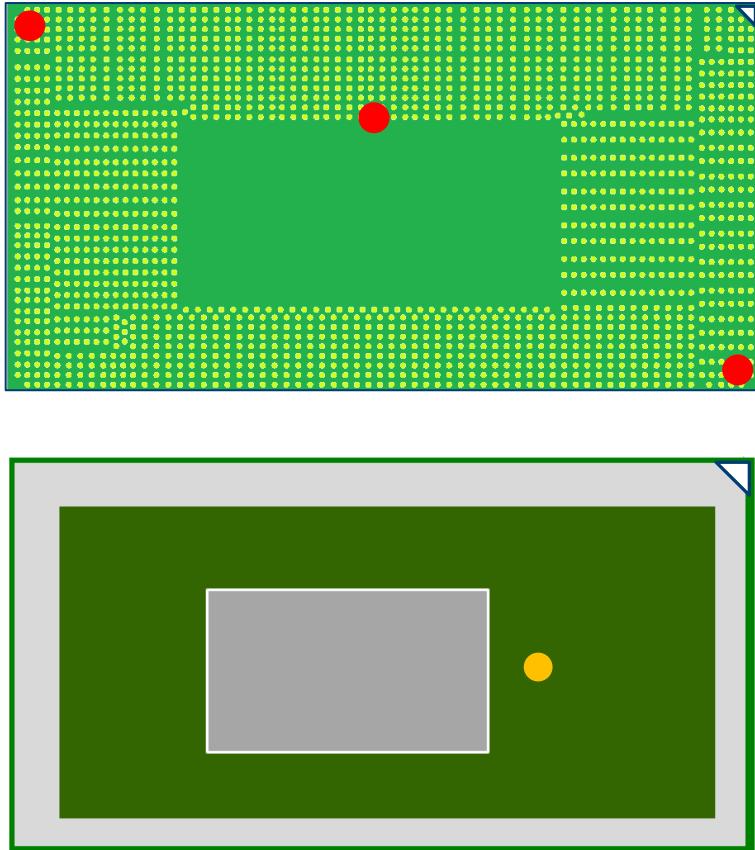
Note:

- ¹Customers are recommended to select thermocouple locations based on their mother board thermal mass.



3.10 SMT Reflow Profiling Thermocouple (TC) Location Recommendations

Tiger Lake H81 Processor Line



- Thermocouple attached to solder joint
- Thermocouple attached to substrate

| Recommended Thermocouple Locations ¹ | |
|---|-----------------|
| 1 | FCBGA Corner |
| 2 | FCBGA Center |
| 3 | FCBGA Corner |
| 4 | FCBGA Substrate |

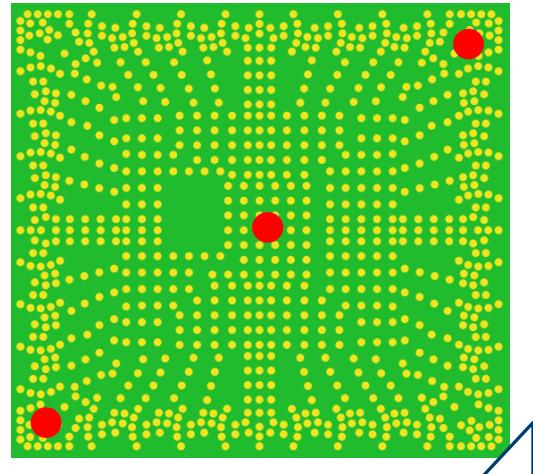
Note:

- ¹Customers are recommended to select thermocouple locations based on their mother board thermal mass.

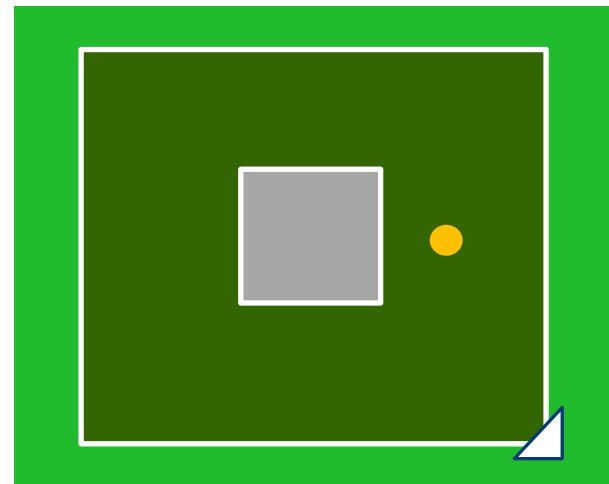


3.10 SMT Reflow Profiling Thermocouple (TC) Location Recommendations

Tiger Lake PCH



- Thermocouple attached to solder joint
- Thermocouple attached to FCBGA substrate



| Recommended Thermocouple Locations ¹ | |
|---|-----------------|
| 1 | FCBGA Corner |
| 2 | FCBGA Center |
| 3 | FCBGA Corner |
| 4 | FCBGA substrate |

Note:

- ¹Customers are recommended to select thermocouple locations based on their mother board thermal mass.

3.11 Board Flexure in Manufacturing Overview (1 of 2)

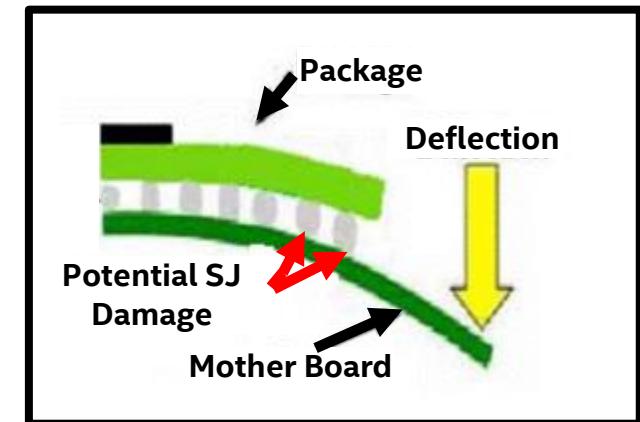
Introduction:

- Intel's Board Flexure Initiative (BFI) methodology was developed to provide customers with the means to monitor and reduce board flexure during manufacturing.
 - This methodology is aligned with industry standard IPC9704A (Printed Circuit Assembly Strain Gage Test Guideline - updated in February 2012).
- BFI methodology involves the use of rectangular rosette strain gages mounted on top-side (primary side) of the PCB at package corners, to indirectly monitor potential solder joint damage.
- Accurate position of strain gage location is critical to take advantage of BFI strain guidance provided by Intel.

Purpose:

- Ensure no NCTF or CTF solder joint cracks / damage during manufacturing.
- Typical areas of concern for board flexure include (but not limited to) router, MDA/ICT & Functional Testing, connector insertion, system assembly processes, etc...
- BFI strain guidance is not applicable during and/or after thermal solution attach for both sockets and BGA products.
- Intel does NOT recommend using BFI methodology to optimize thermal solution attach sequence.

Customers are encouraged to evaluate all manufacturing steps comprehended by board flexure monitoring metrology.



3.11 Board Flexure in Manufacturing Overview (2 of 2)

- **BFI Strain Guidance Metric & Method**
 - Strain Gage location: Use rectangular rosette strain gages placed on top-side at 5mm from BGA package corners along the diagonal (different strain gage location for sockets).
 - Strain Metric: Peak Diagonal Strain (calculated from raw rosette strain data). Monitor all FOUR corners of packages. Applies to both sockets and BGA. Includes the impact of board level adhesives.
- **Reference Documentation**
 - For additional details on Intel's BFI methodology & method, please refer to the MAS link below. Customer should also refer to BFI strain guidance sheets specific to each Tiger Lake Platform Mobile product.

[Two Strain Gage Placement Videos are also available for viewing:](#)



Vishay* Gages: Watch Video on Brightcove*



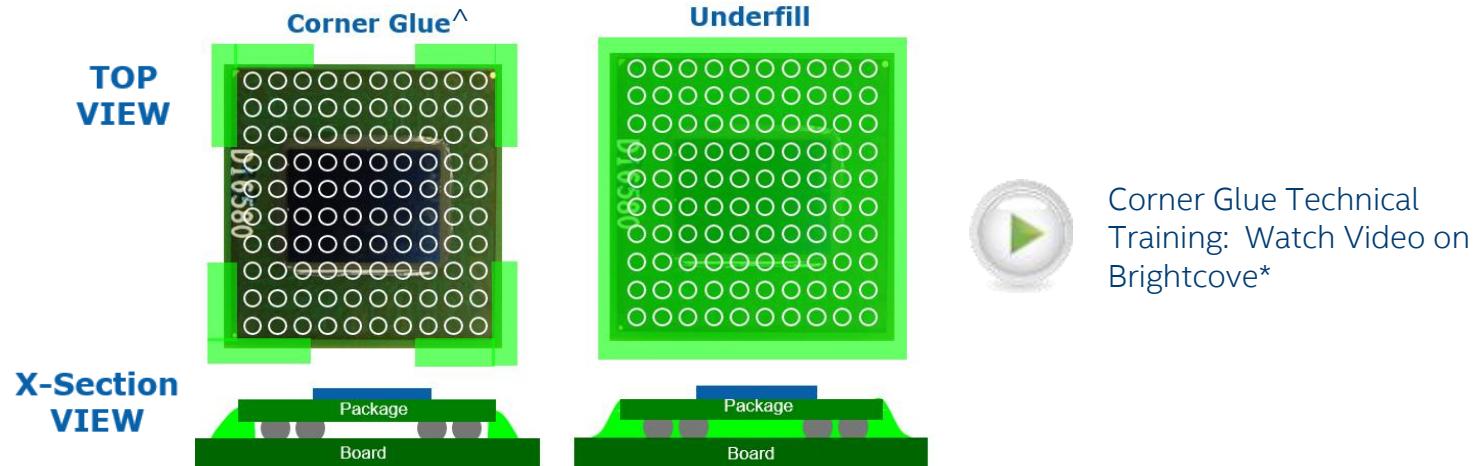
Kyowa* Gages: Watch Video on Brightcove*

Please contact your Intel representative for obtaining BFI Guidance Sheets

Notes:

- Refer to the latest revision of the [Intel® Manufacturing with Intel Components Strain Measurement for Circuit Board Assembly MAS](#) for latest information.
- *Other names and brands may be claimed as the property of others.

3.12 FCBGA Component Board Level Adhesive MAS Overview



Corner Glue Technical Training: Watch Video on Brightcove*

For customers either currently using or planning to use adhesives, Intel has developed an MAS reference document with guidance on adhesive selection and application considerations:

- *Manufacturing with Intel® Products: Adhesive Guidance for Ball Grid Array (BGA) and Package on Package (PoP) (RDC# 573768)*
- This Adhesive MAS covers corner glue and underfill reliability and manufacturing guidance
- It also has a focus on the impact of material selection and properties on reliability performance, and to emphasize workmanship / quality standards
- Customers should always evaluate their adhesives for ionic contamination & corrosive behavior, depending upon the application

Notes:

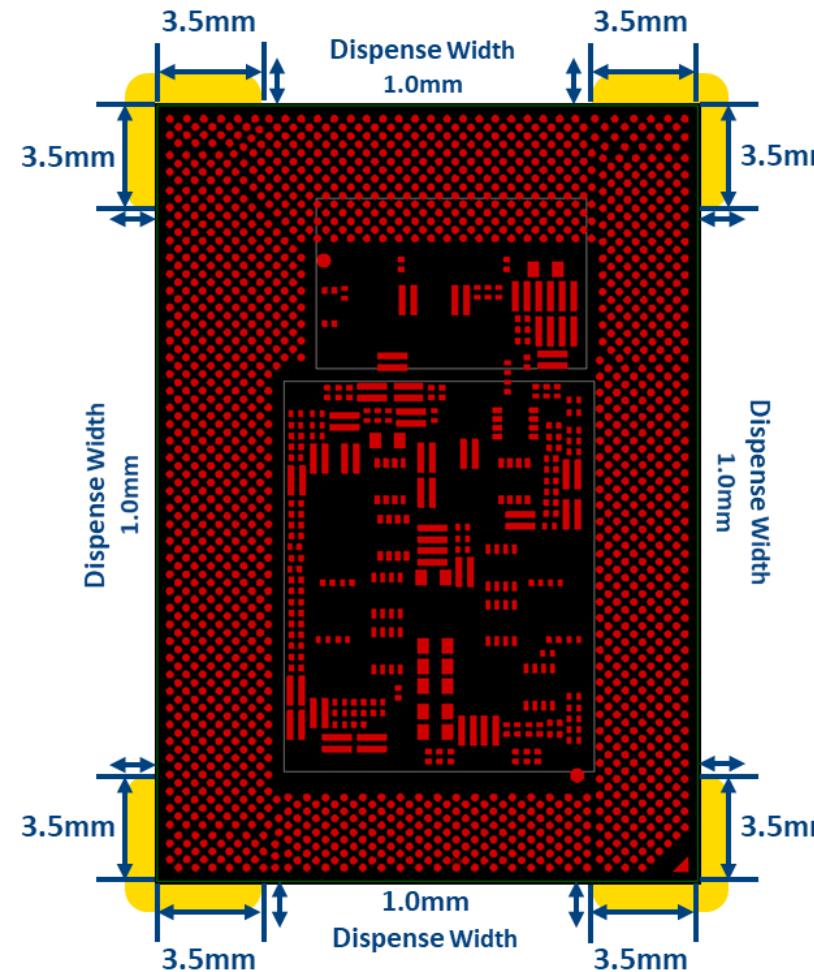
- All adhesives should only be applied to known good components that have been through X-Ray and E-Test to ensure no rework is necessary post adhesive application for these components.
- All adhesive materials that flow underneath a component should not have any through-hole vias and should not undergo any secondary reflow steps post cure application.
- All adhesives rework should be consulted with your material suppliers for rework recommendations for best results in removing the component from the board with minimal damage to both while removing the adhesives.

Notes:

- ^Corner glues are also known as edge bond materials
- *Other names and brands may be claimed as the property of others



3.12 TGL UP4 Board Level Adhesive Application



- Refer to the Tiger Lake TMDG (RDC# 607873) section 3.6.2 for the TGL UP4 corner glue specific recommendations
- If corner glue is applied to TGL UP4, it must be applied at the 4 corners as shown, and the adhesive should cover the corner joints for at least 6 solder joints on the adjacent sides.
 - Zymet UA-2605-B* is recommended
 - The material is then cured per supplier recommendation. Ensure that the adhesive material is at the recommended temperature for the entire duration.
 - It is acceptable for the corner glue to flow under the part and encapsulate the first few rows of solder balls.
 - Intel recommends thermally cured adhesives over UV cured adhesives
 - For this corner glue application:
 - Design PCB adhesive Keep Out Zone (KOZ) width equal to 2.0mm
 - Adhesive dispense width to be 1.0mm (no less than 0.7mm)

| Number of Dispense Locations | Length of Dispense | Width of Dispense | Dispense Weight (Density=1.45)** |
|------------------------------|--------------------|-------------------|----------------------------------|
| 8 | 3.5mm | 1.0mm | 1.8 – 4.4 mg each pass |

Notes:

- *Other names and brands may be claimed as the property of others. Third-party supplier information is provided for information only. Intel accepts no liability for the quality of third-party suppliers and cannot guarantee the correct or suitable operation of third-party products. INTEL DOES NOT ENDORSE ANY SPECIFIC PRODUCT OR ENTITY.
- **Weight values may vary with different material densities.



3.12 TGL Processor Line Adhesive Recommendations For IOTG Applications

For TGL processor line adhesive recommendations for IOTG applications, please refer to :

Tiger Lake IOTG Adhesive Recommendation, RDC#630021



3.13 Package Rework Overview

- Intel provides a separate collateral for reworking Lead Free FCBGA and chipset. Inside is detailed information on the rework reference process to aid in component removal and replacement.
- The following topics are covered in this separate document*:
 - Rework Corner Glue Removal Recommendations
 - Rework Component Replacement: Application Options
 - Rework Process Parameter Recommendations
 - Thermocouple Locations for Rework Thermal Reflow Profile – Mounted into PCB Pads & on the package body surface

*Note: Refer to the [Manufacturing with Intel® Products: Rework Guidance for Ball Grid Array \(BGA\), Package on Package \(PoP\), and Sockets](#) for other process recommendations not mentioned in this module.



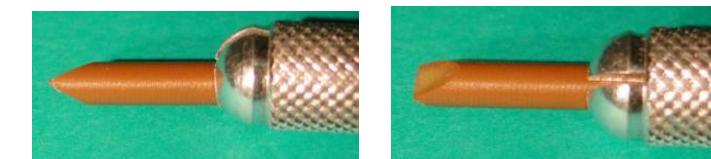
3.13 Considerations for Corner Glue Removal

- For removal of reworkable corner glue material before rework removal, please follow the below steps

- Preheat PCB to as high as 180°C and using a hot air gun, raise the temperature of adhesive at one corner of the component to 200°C. Place heat shields to deflect heat away from adjacent components.
- Use the Torlon¹ scraper tool to scrape off the exposed adhesive. Do not heat directly the Torlon¹ scraper.
- Scrape fillet from the center of the edge toward the corner moving parallel to component edge.
- Work quickly to avoid prolonged high temperature exposure of the adhesive.
- Please note, proper temperature setting might be needed to dislodge the corner glue. Make sure the temperature is not too high. Because high temperature (>260°C) can damage PCB and surrounding component
- After the Corner Glue is removed from the corners, remove the package from the PCB using the Rework Automatic tool (i.e. SRT1100, SRT1800, etc.) following your rework FCBGA process removal. A high temperature-resistant plastic tweezers could be necessary in case the residues of Corner Glue under the corners difficult the removal and tweezers be required to help the tool to pick up the package from the PCB.
- Continue with the rework solder residues removal from the PCB using your normal site dress rework process with the solder wick, flux, solder wire, hot air gun, hot tips or rework station.
- Use Torlon¹ scraper tool to remove the corner glue material residues on the PCB (if it has). It facilitates corner glue residues removal without damage the solder mask.
- Heat PCB to 125°C using bottom heat (225°C hot air) helps to remove the residues.
- Using a hot air pen set at 360°C, raise the temperature of the adhesive residue no higher than needed to melt any remaining solder.
- Scrape off adhesive residue using a Torlon¹ scraper and flux. Use as minimum pressure required when scraping

Tools required:

- Hot air gun, hot air pen (or Rework station)
- Optical Microscope
- Underside board heating system
- High temperature-resistant scraping tool (i.e. Zymet* Torlon¹ scraper tool)
- Rework automatic tool (i.e. SRT1100, SRT1800, etc)



Zymet* Torlon¹ scraper tool

Notes:

Ability to remove corner glue from existing package might depend on the material property. For other materials, please check with Corner Glue manufacturer for rework recommendations

¹Torlon is a commercially available engineering thermoplastic which retains usable mechanical properties up to 275°C. Contact the corner glue supplier for the specific Torlon scraper tool for reworkable corner glue material used.



3.13 Package Rework

Rework Component Replacement: Application Options

The table below shows the rework application options Intel has evaluated and is provided as a reference process in this module:

| FCBGAs/Chipset | Flux-Only Application (applied on the PCB Pads) | Solder Paste Application (applied to the PCB Pads by Mini-Stencil) |
|----------------|--|---|
| TGL UP3/H35 | Not recommended | Recommended |
| TGL UP4 | Recommended | Not recommended |
| TGL H81 | Not recommended | Recommended |
| TGL PCH | Not recommended | Recommended |

*Note: Refer to the [Manufacturing with Intel® Products: Rework Guidance for Ball Grid Array \(BGA\), Package on Package \(PoP\), and Sockets](#) for other process recommendations not mentioned in this module.



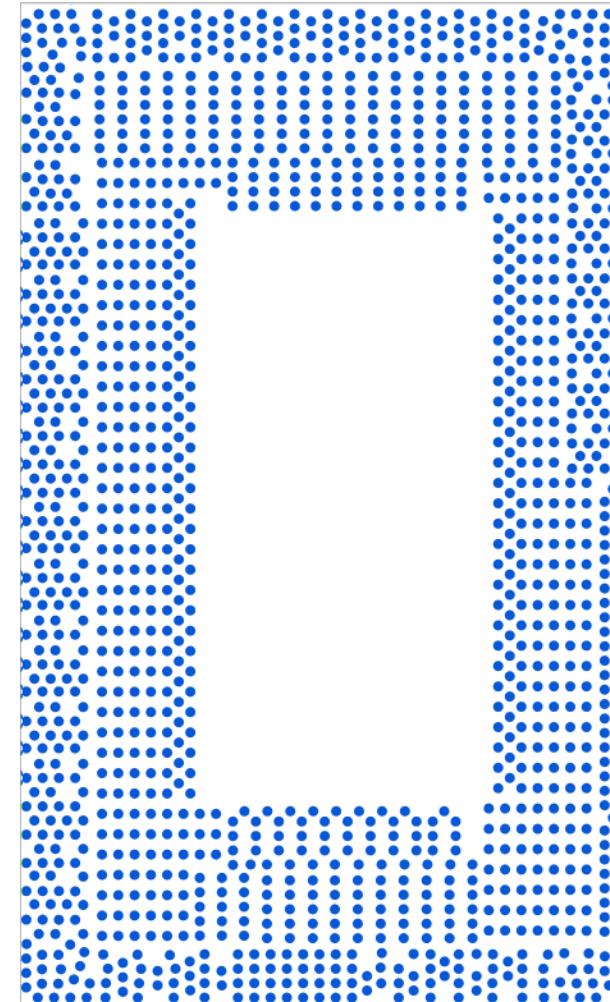
3.13 Solder Paste Volume Optimization Stencil Design Recommendations (SAC Process)

Tiger Lake UP3/H35 FCBGA Processor Line – 4 mil option

| Stencil Thickness: 102 µm (4 mils) option | | | |
|--|-------------------|----------------------------------|------------|
| Stencil Air Gap Design : ≥ 192 µm (7.5 mils) | | | |
| Stencil Design (Aperture) | Over- printing | Solder Paste Volume Target | Area Ratio |
| BGA Pads • Round 457 µm (18 mils) | Yes | 0.0167 cu. mm (1018 cu. mils) | 1.13 |

Notes:

- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
- Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





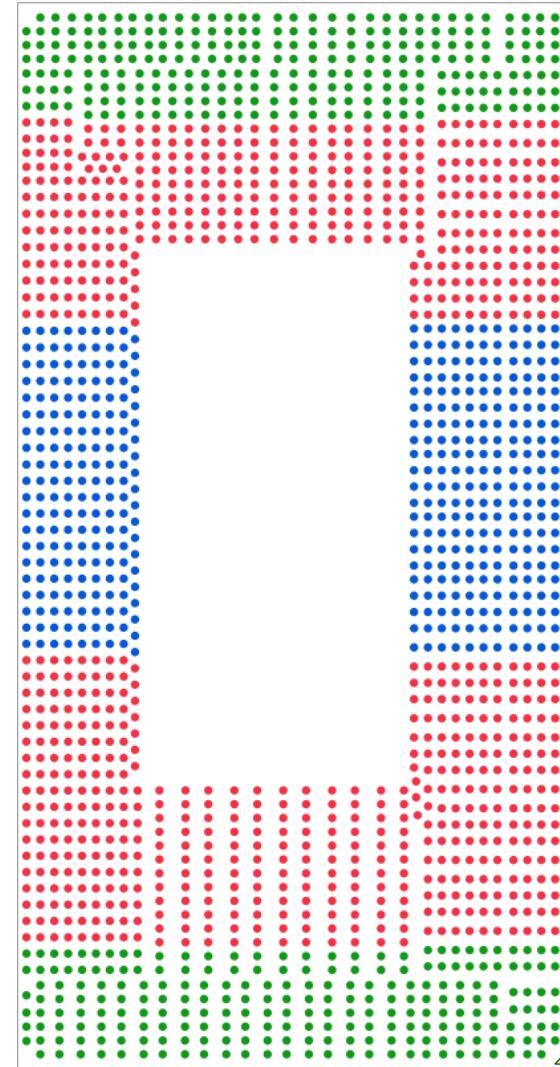
3.13 Solder Paste Volume Optimization Stencil Design Recommendations (SAC Process)

Tiger Lake H81 FCBGA Processor Line – 4 mil option

| Stencil Thickness: 102 µm (4 mils) option | | | |
|---|---------------|----------------------------------|------------|
| Stencil Air Gap Design : $\geq 180 \mu\text{m}$ (7.09 mils) | | | |
| Stencil Design (Aperture) | Over-printing | Solder Paste Volume Target | Area Ratio |
| BGA Center Pads ● Round 355 µm (14.0 mils) | Yes | 0.0101 cu. mm (615 cu. mils) | 0.88 |
| BGA Corner Pads ● Round 470 µm (18.5 mils) | Yes | 0.0176 cu. mm (1076 cu. mils) | 1.16 |
| BGA Body Pads ● Round 432 µm (17.0 mils) | Yes | 0.0149 cu. mm (908 cu. mils) | 1.06 |

Notes:

- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
- Stencil design aligns with this component's PCB Land Pattern Design in Module 2.





3.13 Solder Paste Volume Optimization Stencil Design Recommendations (SAC Process)

Tiger Lake PCH – 4 mil option

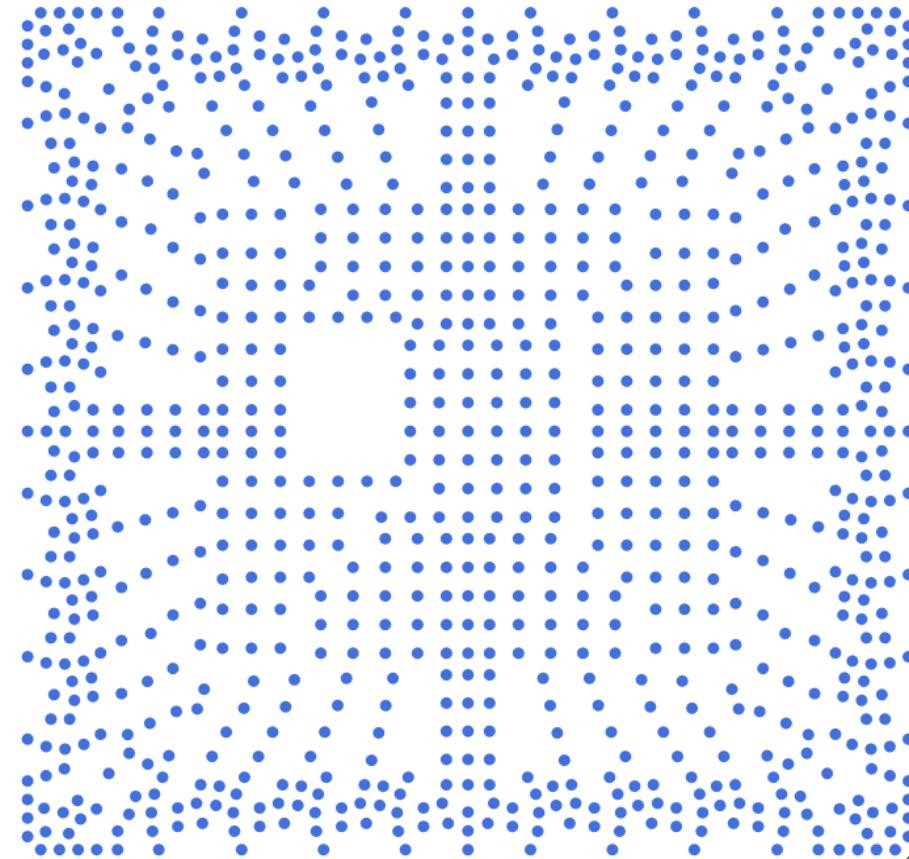
Stencil Thickness: **102 µm (4 mils) option**

Stencil Air Gap Design : $\geq 152 \mu\text{m}$ (6.0 mils)

| Stencil Design (Aperture) | Over- printing | Solder Paste Volume Target | Area Ratio |
|---|-------------------|---------------------------------|------------|
| All Pads • Round 348 μm (13.7 mils) | Yes | 0.0097 cu. mm (590 cu. mils) | 0.86 |

Notes:

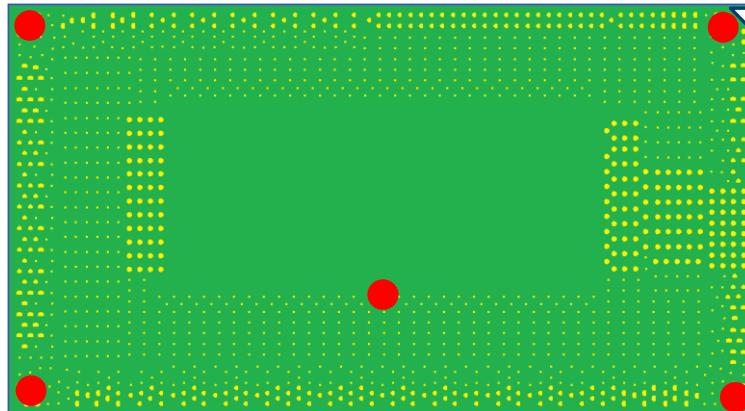
- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.
- Stencil design aligns with this component's PCB Land Pattern Design in Module 2.



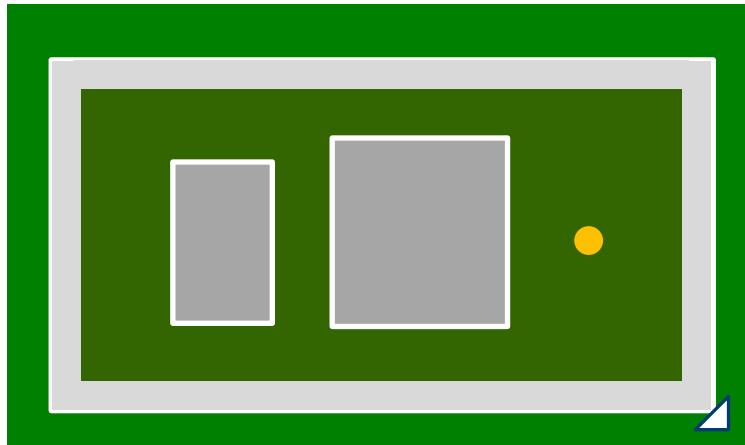


3.13 Rework Profiling Thermocouple (TC) Location Recommendations

Tiger Lake UP3/H35 Processor Line



- Thermocouple attached to solder joint
- Thermocouple attached to substrate/top body of the component
- △ Pin 1 Location



| Recommended Thermocouple Locations ¹ | |
|---|------------------------------------|
| 1 | FCBGA Corner |
| 2 | FCBGA Corner |
| 3 | FCBGA Corner |
| 4 | FCBGA Corner |
| 5 | FCBGA Center |
| 6 | FCBGA Substrate/top body component |

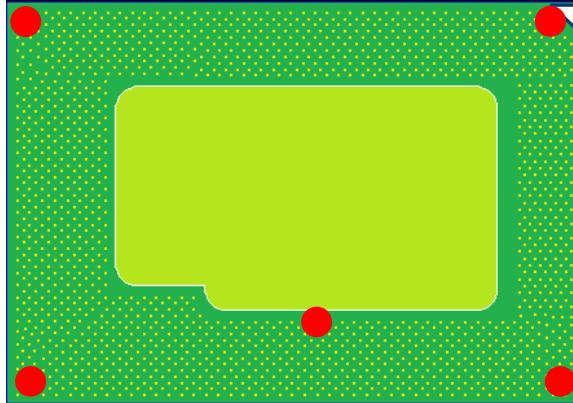
Note:

- ¹Customers are recommended to select thermocouple locations based on their mother board thermal mass.

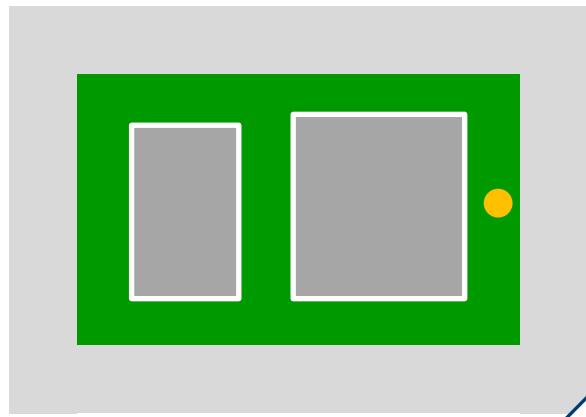


3.13 Rework Profiling Thermocouple (TC) Location Recommendations

Tiger Lake UP4 Processor Line



- Thermocouple attached to solder joint
- Thermocouple attached to substrate/top body of the component
- △ Pin 1 Location



| Recommended Thermocouple Locations ¹ | |
|---|------------------------------------|
| 1 | FCBGA Corner |
| 2 | FCBGA Corner |
| 3 | FCBGA Corner |
| 4 | FCBGA Corner |
| 5 | FCBGA Center |
| 4 | FCBGA Substrate/top body component |

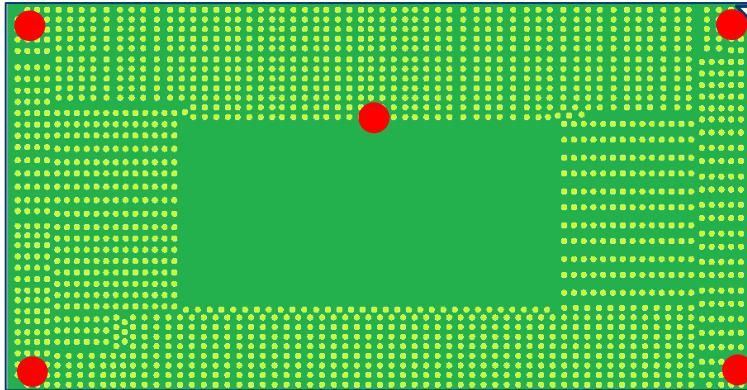
Note:

- ¹Customers are recommended to select thermocouple locations based on their mother board thermal mass.

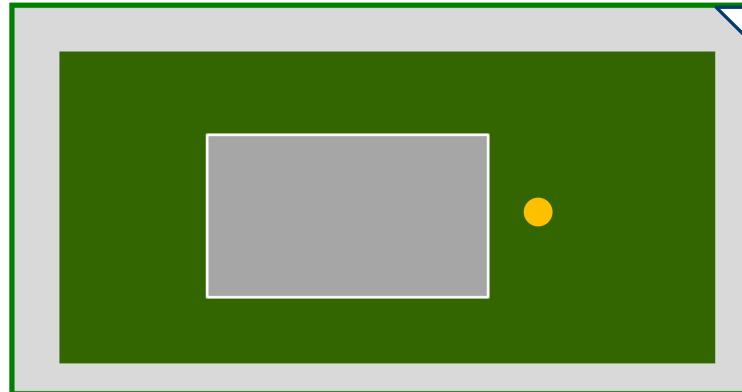


3.13 Rework Profiling Thermocouple (TC) Location Recommendations

Tiger Lake H81 Processor Line



- Thermocouple attached to solder joint
- Thermocouple attached to substrate/top body of the component
- △ Pin 1 Location



| Recommended Thermocouple Locations ¹ | |
|---|---------------------------------------|
| 1 | FCBGA Corner |
| 2 | FCBGA Corner |
| 3 | FCBGA Corner |
| 4 | FCBGA Center |
| 5 | FCBGA Substrate/Top body of component |
| 4 | FCBGA Substrate/Top body of component |

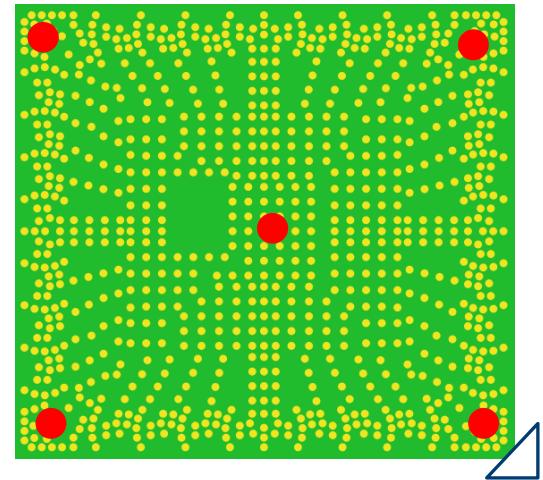
Note:

- ¹Customers are recommended to select thermocouple locations based on their mother board thermal mass.



3.13 Rework Profiling Thermocouple (TC) Location Recommendations

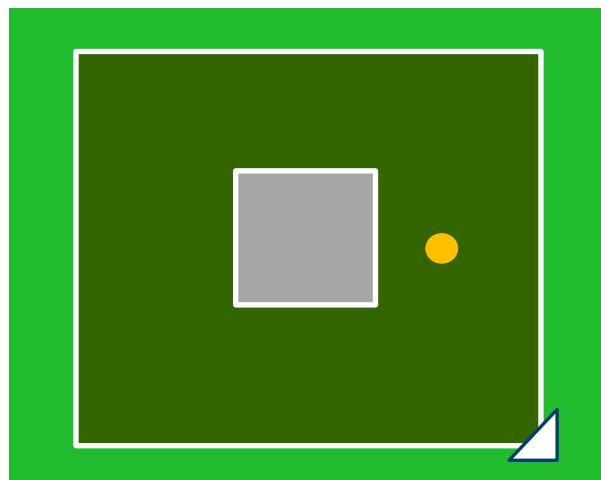
Tiger Lake PCH



● Thermocouple attached to solder joint

● Thermocouple attached to substrate/top body of the component

△ Pin 1 Location



| Recommended Thermocouple Locations ¹ | |
|---|---------------------------------------|
| 1 | FCBGA Corner |
| 2 | FCBGA Corner |
| 3 | FCBGA Corner |
| 4 | FCBGA Corner |
| 5 | FCBGA Center |
| 6 | FCBGA Substrate/Top body of component |

Note:

- ¹Customers are recommended to select thermocouple locations based on their mother board thermal mass.



3.13 Package Rework

Other Rework Process Parameter Recommendations

| Rework recommendations for customer consideration. | |
|--|--|
| Parameters | FCBGA & Chipset |
| Solder Paste Formulation | SAC305 (LF) Type 4. Use recommended SMT pastes (see prior slides) |
| Intel Evaluated Flux Formulation | Tackly flux, Alpha PoP-707 |
| Solder Paste Volume | NA |
| Rework pallets | Highly recommended to keep the board flat during the reflow |
| Gap between nozzle & PCB surface (optimize air flow) | 762 µm (30 mils) |
| Rework Ambient | Air (Nitrogen was not evaluated) |
| Solder Joint Peak Reflow Temperature (PRT) | 240°C ± 5 °C |
| Time Above ≥ 220°C | 60 to 90 seconds |
| Maximum Body Temperature | ≤250°C. Never exceed 260°C |
| Component Delta T (ΔT) | ≤10°C |
| Soak Temp & Time | Paste dependant; consult paste manufacturer. |
| Rising Ramp Rate below 150°C (+) | 0.5 to 2.5°C/sec |
| Rising Ramp Rate between 205°C and 215°C (+) | 0.35 to 0.75°C/sec |
| Falling Ramp Rate (-) | 0.50 to 2.0°C/sec |
| Comments | Other recommendations for TGL UP4: <ul style="list-style-type: none"> • Solder Join Peak Reflow Temperature (PRT) : 230°C-235°C recommended to minimize PCB and package warpage • Flux volume recommended ~10-15mg to minimize BGA package movement during reflow |

Notes:

- Except for body temp, all temperatures are measured with thermo couples inside solder joints, for increased accuracy.
- This is Intel's rework reference process practices and parameters are provided for reference purposes only, based on internal studies, and are not necessarily optimized. Mfg. processes are unique and may require unique solutions to ensure an acceptable level of quality, reliability, and mfg yield. Due to the differences in equipments and materials, process parameter modifications may be required to meet customer's quality, reliability, and manufacturing yield requirements.
- *Other names and brands may be claimed as the property of others.



3.13 Rework Reflow Profile Recommendations for BGA Package (SAC Process)

Step-by-Step BKM for Rework Reflow Profile

| Step 1 Board Preheat | Step 2 Soak Time | Step 3 Peak Reflow & Time Above 220 °C | Step 4 Cool Down |
|--|--|---|---|
| Start with solder joint temp < 40°C | Top heater nozzle should be lowered around 150 °C | Heat from Top heater nozzle and bottom heater is used to reach peak reflow temperature | Raise nozzle after reaching the peak reflow temperature |
| Board Preheat Solder Joint Temp: 125 – 150°C | BGA Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec | Peak Temp Range, and Time Above ≥ 220°C | Cooling Ramp Rate. BGA -0.5 to -2 °C/sec |
| Rising Ramp Rate below 150°C: 0.5 to 2.5 °C/sec | Soak Temp & Time (Flux or Paste dependent; consult manufacturer) | Solder Joint Temp: 230°C -245°C Time Above ≥ 220°C 60 – 90 sec Max Delta Temp at peak reflow ≤10°C Max component temperature ≤ 250 °C. Never exceeds 260 °C | PCB land/pad temperature needs to be at 100 – 130°C ± 5°C |
| Preheat with bottom heater, before nozzle is lowered | Nozzle has lowered to reflow component | Nozzle is down during peak reflow | Board can be removed at 100 to 130°C for PCB pad site preparation |

Note:

- Reference information Only.
- Above recommendation is for Lead-Free SAC alloys
- Temperature should be measured with thermocouples inside solder joints for better accuracy (except for the temperature on the body of the component).
- For TGL UP4 Solder Joint Temperature recommended 230°C-235°C



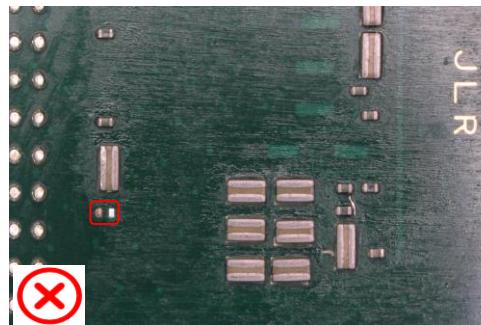
3.14 FACR Preparation Process

Intel requests that any components to be submitted for FACR (Functional Analysis Correlation Request) are properly prepared, without causing any component damage. If the steps below are not followed, Intel may not be able to test the component.

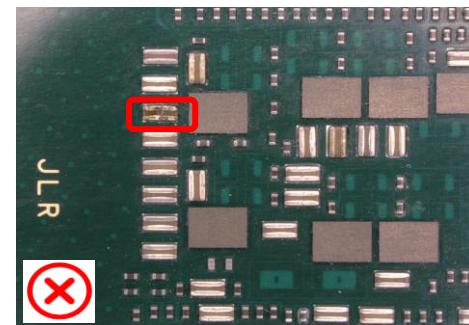
FACR Preparation Steps:

- Bake the board/module to avoid any component delamination per MSL (Moisture Sensitivity Level) requirement
- Visually inspect the component to ensure no damage or other quality issues are present prior to its removal
- Demount the component following the customer's process
- Remove any board level adhesive residue (e.g. corner glue/fill, edge glue, underfill, etc...) from the component
- Perform a visual inspection @ 20X to ensure the component has no damage or other quality issues **caused** by its removal -> look for missing or damaged capacitors, lifted pads, die crack or die chipping, adhesive residue (see below for some examples)
- Do not return the component for FACR if it has any of the damage or quality issues shown below (but not limited to the below examples)

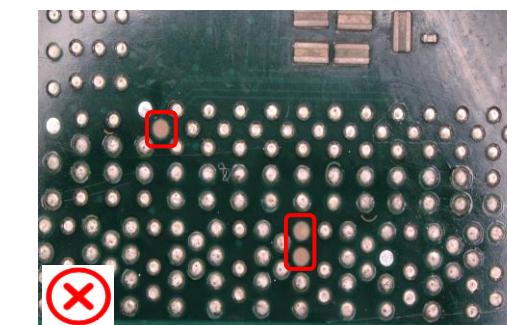
For additional questions regarding FACR, work with the Intel Representative



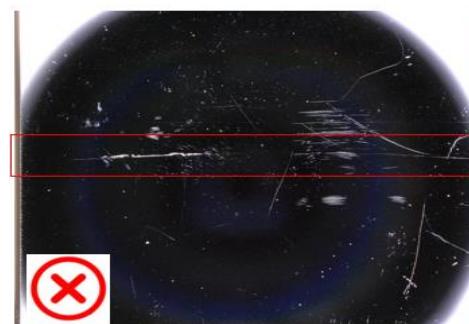
Missing capacitor



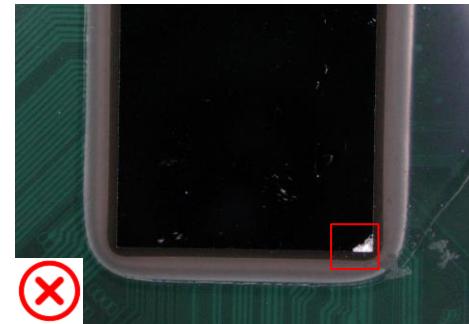
Damaged/Mis-aligned capacitor



Lifted pad



Die crack



Die chipping



Adhesive residue

Module 4: Shipping and Handling

Manufacturing with the Intel® Platform Code Named Tiger Lake

Overview – Table of Contents

| | | | | | | |
|---|--|--|--|------------------------------------|--|--|
| Module 1: <u>Component Attributes and Drawings</u> | Module 2: <u>Land Pattern (PCB Pad) Design Guidelines</u> | Module 3: <u>Manufacturing Guidelines</u> | Module 4: <u>Shipping & Handling</u> | Module 5: <u>Testing</u> | Module 6: <u>System Integration & ESD Considerations</u> | Module 7: <u>References</u> |
| 1.1 Package Attributes Intel® FCBGA Processors 1.2 Package Mechanical Drawings (PMD) FCBGA Processors 1.3 Package Attributes PCH 1.4 Package Mechanical Drawings (PMD) PCH | 2.1 Land Pattern Design Guidelines Introduction 2.2 Mother Board Cavity Voiding Requirements 2.3 Land Pattern Design Guidelines (for the different processors & chipset) | 3.1 Introduction 3.2 Example Package Dynamic Warpage Data 3.3 Critical SMT Recommendations 3.4 Manufacturing Guidelines General Info 3.5 Solder Paste Formulation Optimization 3.6 Solutions to Extend Stencil Aperture Area Ratio 3.7 Cu Core Standoff Technology 3.8 Solder Paste Volume Optimization Stencil Design Recommendations 3.9 SMT Reflow Pallet Recommendations 3.10 SMT Reflow Profile TC Location 3.11 Overview of Board Flexure 3.12 Board Level Adhesive Overview 3.13 Package Rework 3.14 FACR Prep Process | 4.1 Processor and Chipset Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements 4.4 BGA Package Handling BKMs 4.5 T&R Package Handling BKMs | 5.1 Test Information | 6.1 Introduction 6.2 Electro Static Discharge (ESD) Platform Component Goals 6.3 Electro Static Discharge (ESD) Design Guidelines 6.4 Electro Static Discharge (ESD) Additional Resources 6.5 Thermal Solution Assembly / Disassembly considerations | 7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Resource Design Center access Information |



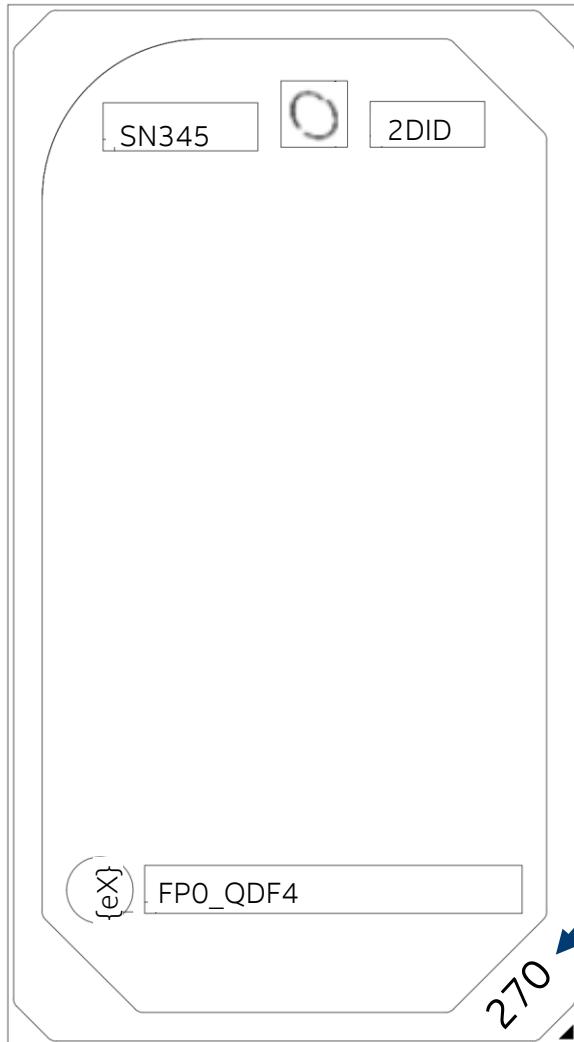
Acronyms Found in this Module

| | |
|-------|---|
| Cu | Copper |
| CuOSP | Copper Organic Solderability Preservative |
| EDS | External Design Specification |
| FCBGA | Flip-Chip Ball Grid Array |
| HIMB | Hole In Mother Board |
| HT | High Temperature |
| MAS | Manufacturing Advantage Service |
| MB | Mother Board |
| MSL | Moisture Sensitivity Level |
| NCTF | Non-Critical to Function |
| PCH | Platform Control Hub |
| PDS | Product Datasheet |
| PMD | Package Mechanical Drawing |
| RIMB | Recess In Mother Board |
| RT | Room Temperature |
| T&R | Tape and Reel |
| TFT | Thermoform Tray |



4.1 Package Marking

Tiger Lake UP3/H35 Processor Line (45.5x25mm)



TGL UP3 ES2 packages will be marked on the metal stiffener with a human readable "270" mark, providing a visual indication of the sample version.

TGL UP3/H35 QS and later package will not have this "270" mark on the stiffener

| Product phase | ES1 | ES2 | QS and onward |
|---------------|-----|-----|---------------|
| "270" mark | No | Yes | No |



Example of TGL UP3 ES2 package with stiffener marking

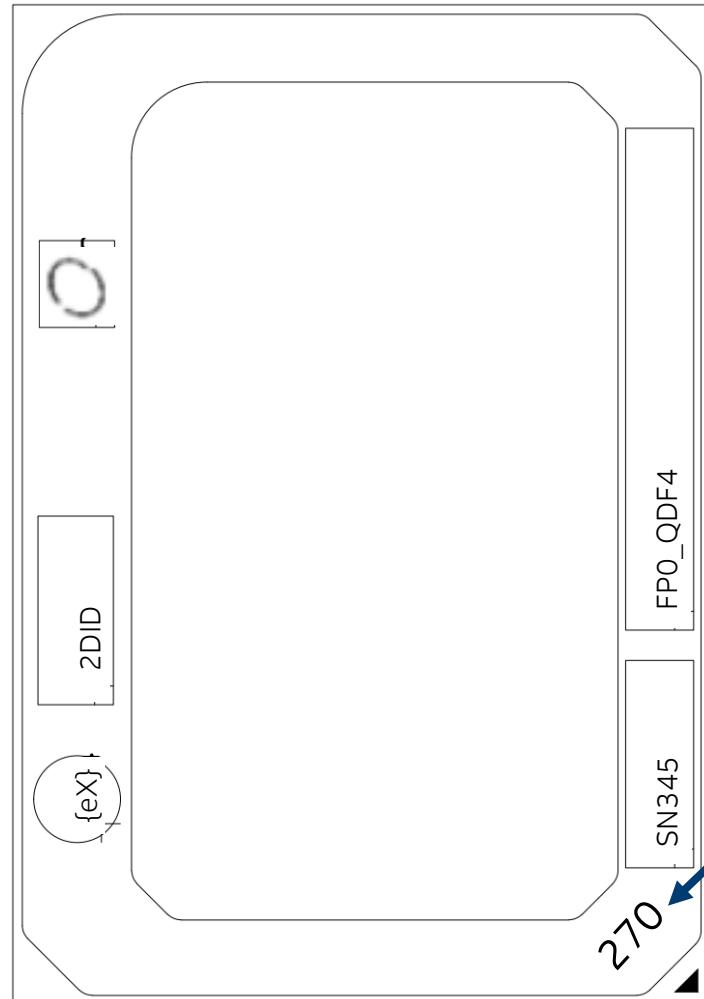
| Item | Abbreviation | Meaning |
|-----------|--------------|----------|
| GRP1LINE1 | G1L1 | {O} |
| GRP2LINE1 | G2L1 | FP0_QDF4 |
| GRP3LINE1 | G3L1 | {eX} |

Notes:

- For reference information only. Picture here for illustration only. Always refer to the latest product marking for final information.

4.1 Package Marking

Tiger Lake UP4 Processor Line (26.5mmx18.5mm)



TGL UP4 ES2 packages will be marked on the metal stiffener with a human readable “270” mark, providing a visual indication of the sample version.

TGL UP4 QS and later package will not have this “270” mark on the stiffener

| Product phase | ES1 | ES2 | QS and onward |
|---------------|-----|-----|---------------|
| “270” mark | No | Yes | No |



Example of TGL UP4 ES2 package with stiffener marking

| Item | Abbreviation | Meaning |
|-----------|--------------|----------|
| GRP1LINE1 | G1L1 | ○ |
| GRP2LINE1 | G2L1 | {eX} |
| GRP6LINE1 | G6L1 | FP0_QDF4 |

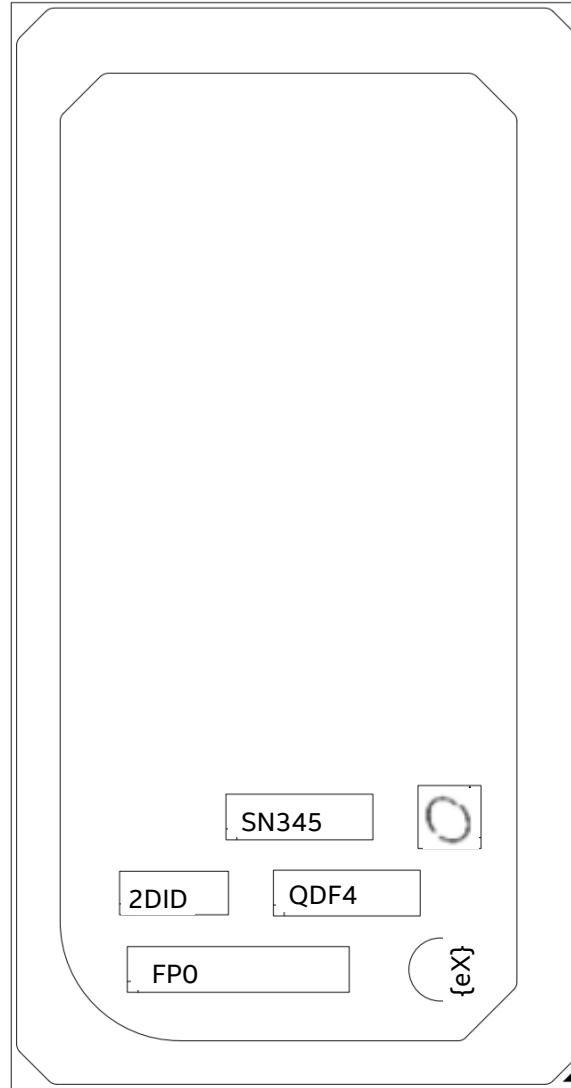
Notes:

- For reference information only. Picture here for illustration only. Always refer to the latest product marking for final information.



4.1 Package Marking

Tiger Lake H81 Processor Line (50mmx26.5mm)



Notes:

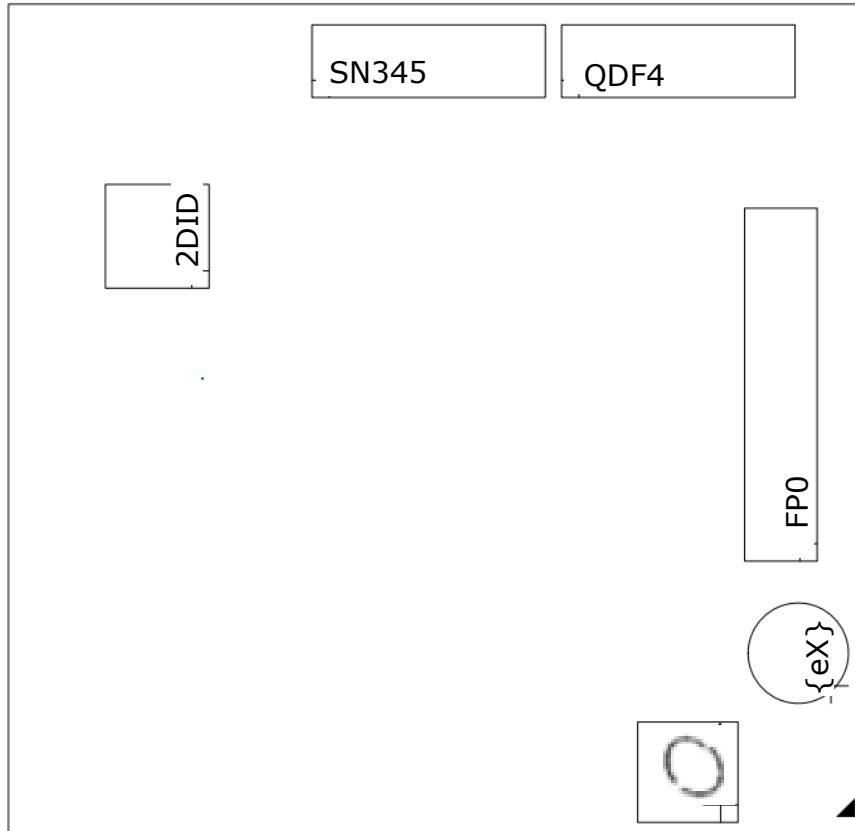
- For reference information only. Picture here for illustration only. Always refer to the latest product marking for final information.

| Item | Abbreviation | Meaning |
|-----------|--------------|---------|
| GRP1LINE1 | G1L1 | O |
| GRP2LINE1 | G2L1 | FPO |
| GRP3LINE1 | G3L1 | QDF4 |
| GRP4LINE1 | G4L1 | {eX} |



4.1 Package Marking

Tiger Lake PCH (25mmx24mm)



| Item | Abbreviation | Meaning |
|-----------|--------------|---------|
| GRP1LINE1 | G1L1 | O |
| GRP2LINE1 | G2L1 | FPO |
| GRP3LINE1 | G3L1 | QDF4 |
| GRP4LINE1 | G4L1 | {eX} |

Notes:

- For reference information only. Picture here for illustration only. Always refer to the latest product marking for final information.



4.2 Tiger Lake Mobile Platform Component Packaging

- For processors in FCBGA packages, trays are generally used. For chipset packages, trays are generally used for samples and Tape & Reels are generally used for high volume manufacturing.
- The thermoform tray (TFT) is made of PET (Polyethylene Terephthalate) and has a maximum exposure temperature (MET) of 50°C, which is NOT compatible with a High Temp Bake option.
- If you must bake them to remove moisture, the bake temperature cannot exceed the max temp of the media used for baking. Baking can also be done on thermoform tray only at lower temperature that do not exceed the material Max Temp Exposure per JEDEC standard J-STD-033B.1 (similar to tape and reel).

| Options to Be Shipped from Intel | | | |
|--|------------------------------------|---|-------------|
| Component Name | Thermoform Tray ¹ (TFT) | Modified Poly-Phenylene Oxide ^{2,3} (MPPO) | Tape & Reel |
| Tiger Lake Processors (FCBGA Package) | Yes | No ³ | No |
| Tiger Lake PCH | No | No | Yes |

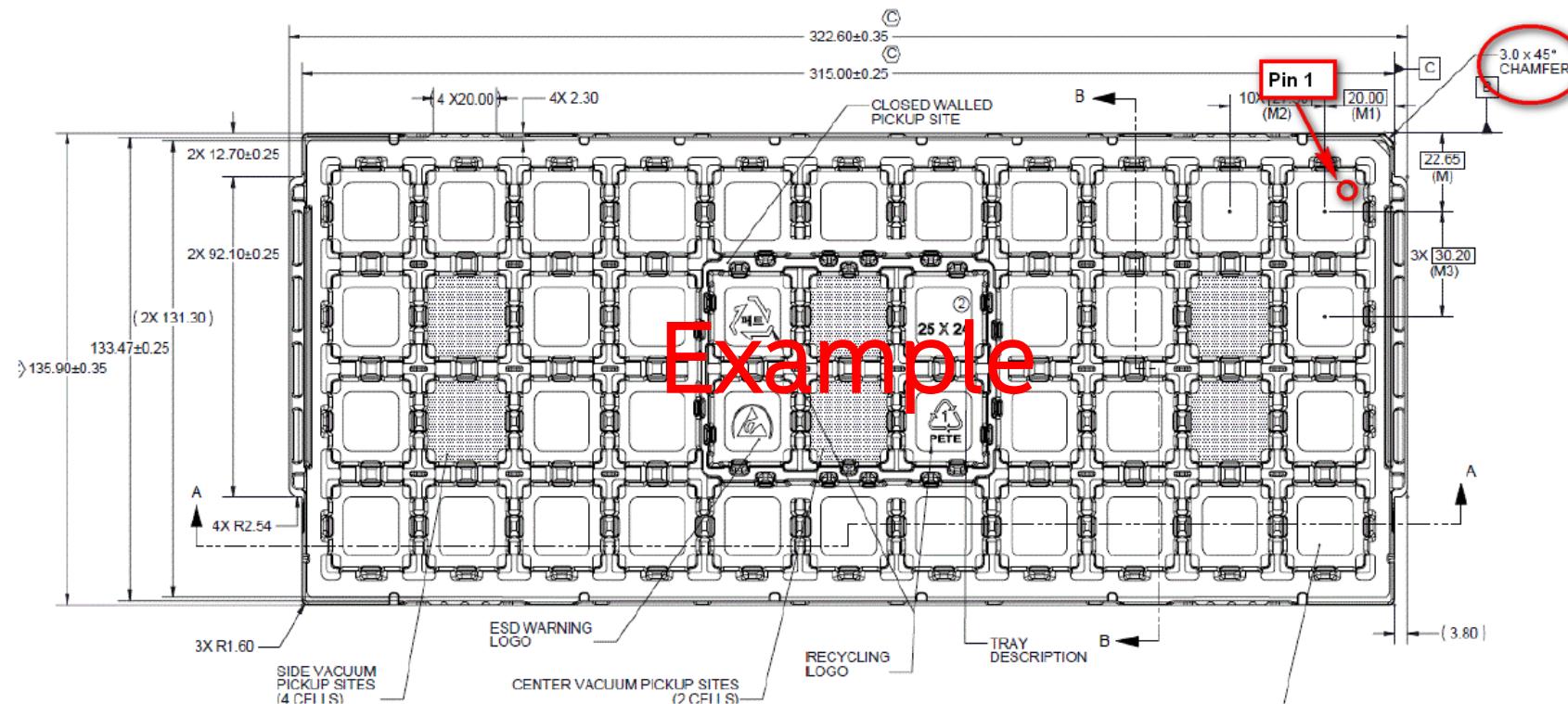
Notes:

- ¹Also known as a Soft Tray.
- ²Also known as a Hard Tray.
- ³A MPPO tray is available for purchase from a 3rd party vendor. See footnote information on each subsequent tray slide in this module
- Information is for reference only and may change at any time.



4.2 Additional TFT Tray information

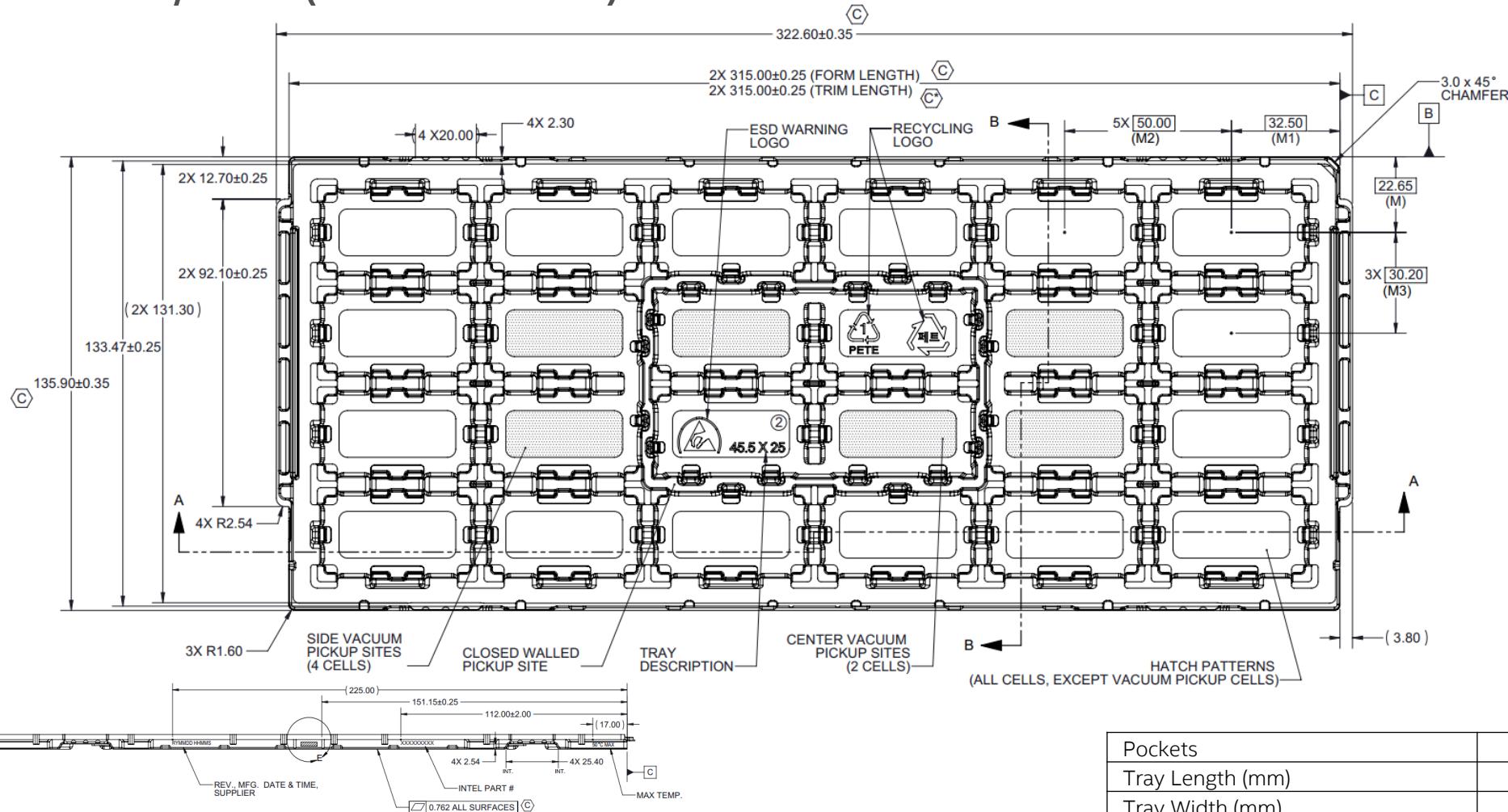
For packages shipped in trays, the BGA Pin 1 location will always align with the tray chamfer. The user feed direction will depend on the customer's SMT process and machine settings, which Intel does not control.





4.2 Thermoform Tray (TFT) Drawing

Tiger Lake UP3/H35 (45.5x25 mm) - 1 of 2 slides

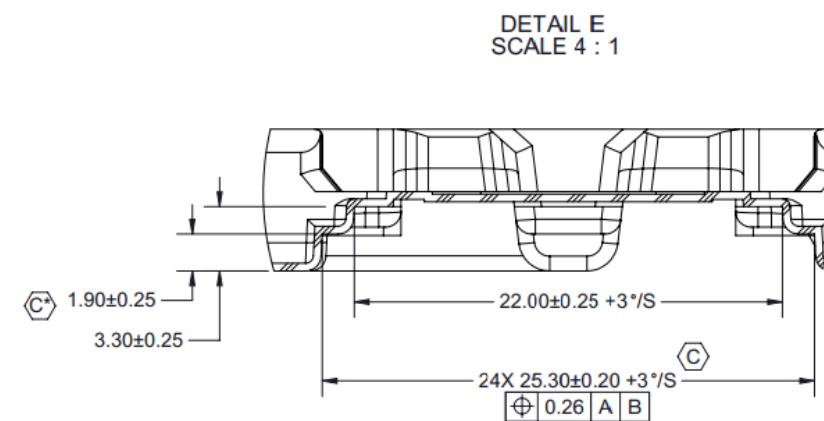
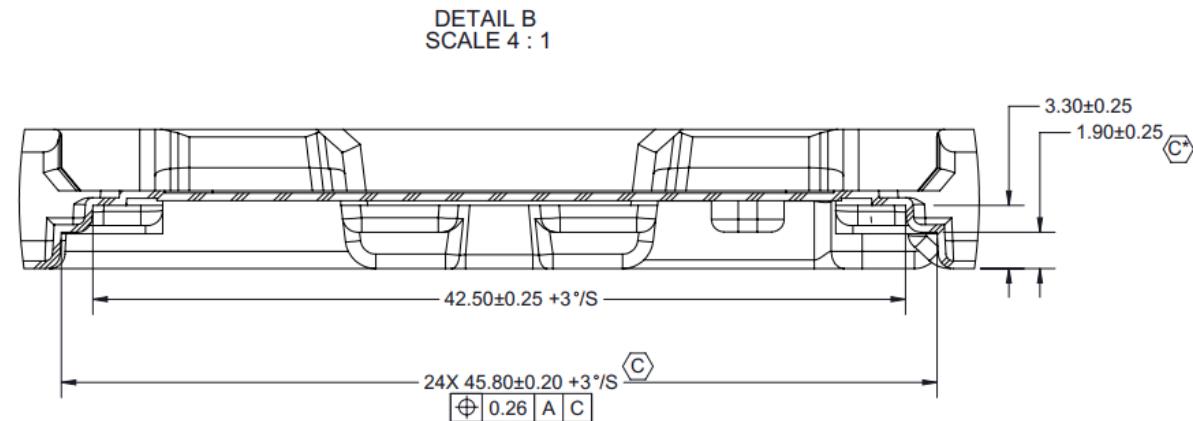
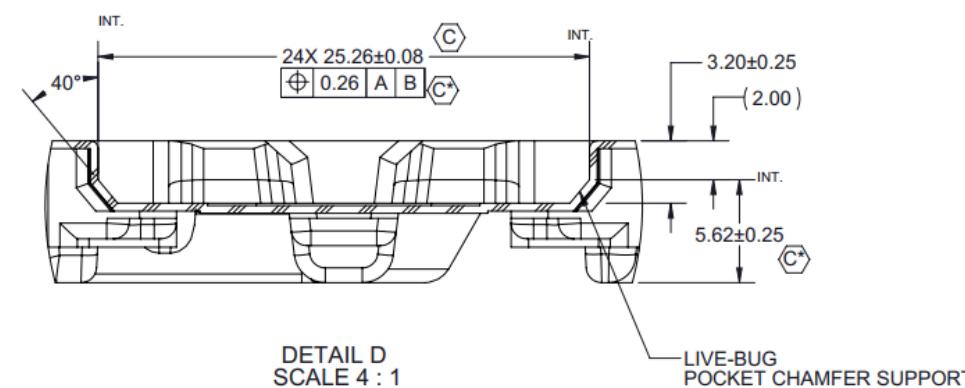
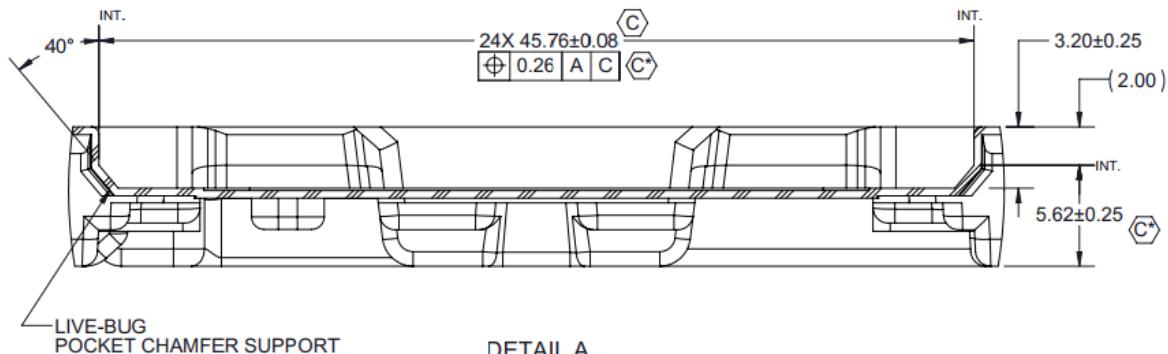


| | |
|-------------------------------|-----------------|
| Pockets | 4 x 6 |
| Tray Length (mm) | 322.60 ± 0.35mm |
| Tray Width (mm) | 135.90 ± 0.35mm |
| Tray Thickness (mm) | 7.62 ± 0.35mm |
| X Axis 1st Pick-Up Point (mm) | 36.3mm |
| Y Axis 1st Pick-Up Point (mm) | 22.65mm |
| X-Axis Pitch (mm) | 50.00mm |
| Y-Axis Pitch (mm) | 30.20mm |



4.2 Thermoform Tray (TFT) Drawing

Tiger Lake UP3/H35 (45.5x25 mm) - 2 of 2 slides



Notes:

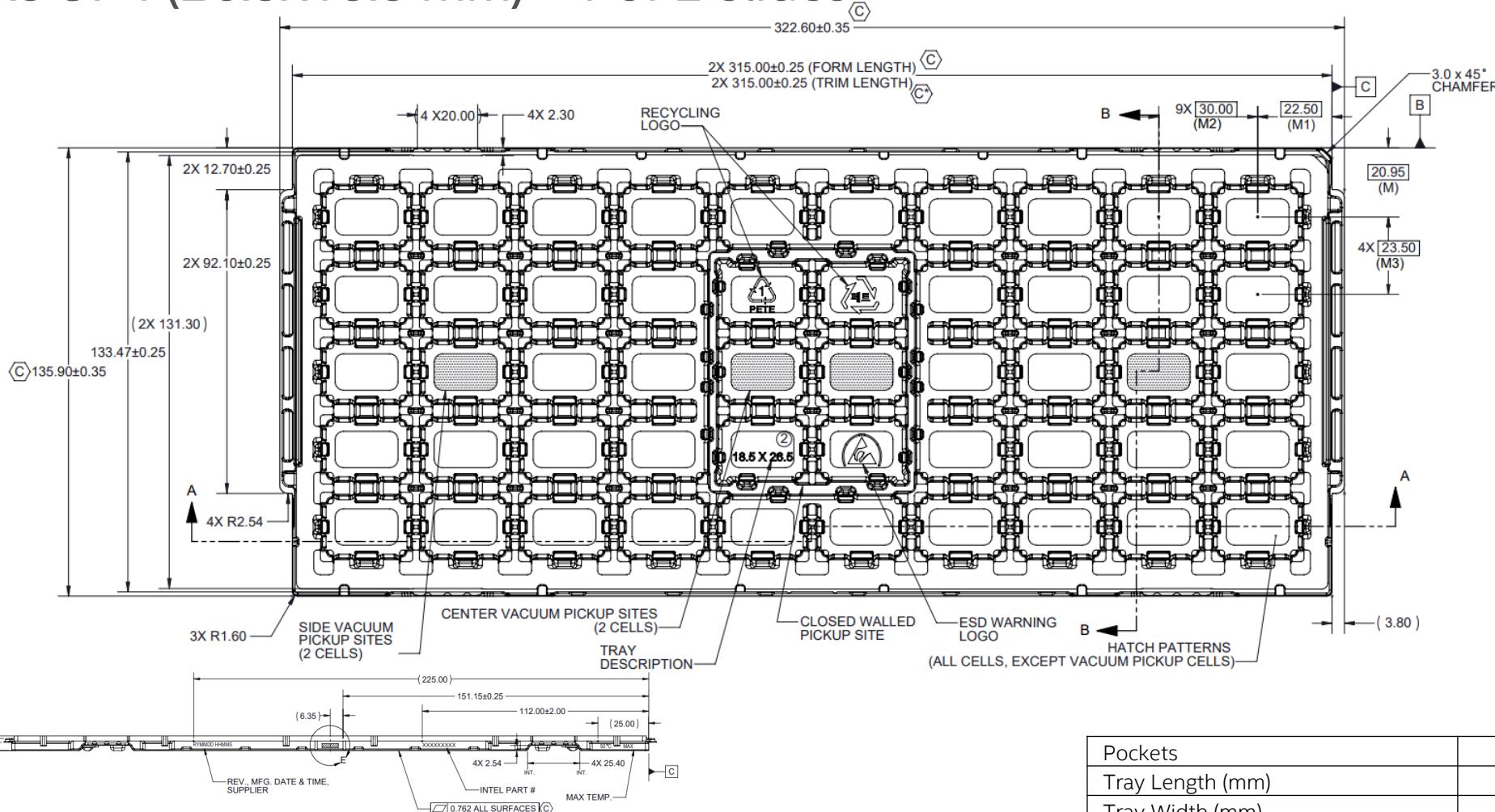
- Information is for reference only and may change at any time.
- Intel Drawing #500372215 – Rev01
- The above TFT can only be heated to 50°C. However, a Modified Poly-Phenylene Oxide (MPPO) material that it is used for higher temp baking is bake able to 150°C max. Our high temp tray supplier is Daewon (IPN: 500359049 / Daewon part number TR184090). Other similar trays may exist. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs.
- Daewon contact: relee@daewonspic.com

| | |
|----------------------------------|--------------|
| Pocket X top dimension | 45.76±0.08mm |
| Pocket X bottom dimension | 45.80±0.20mm |
| Pocket Y top dimension | 25.26±0.08mm |
| Pocket Y bottom dimension | 25.30±0.20mm |
| Top Pocket Depth dimension | 3.20±0.25mm |
| Bottom Pocket Depth dimension | 3.30±0.25mm |



4.2 Thermoform Tray (TFT) Drawing

Tiger Lake UP4 (26.5x18.5 mm) - 1 of 2 slides

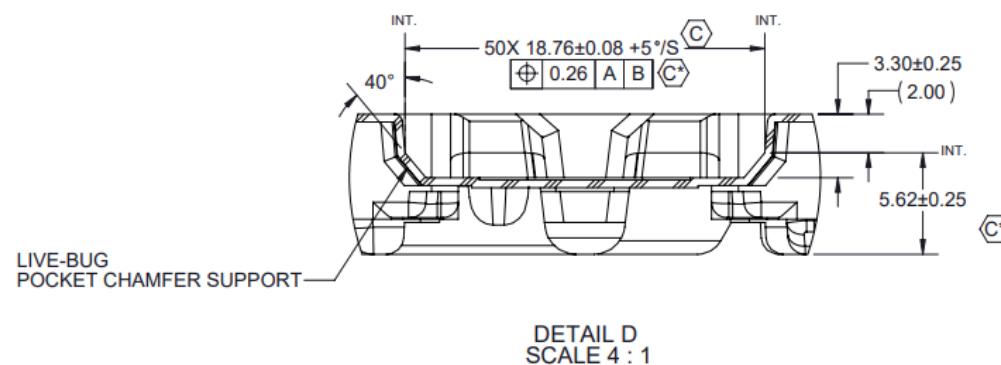
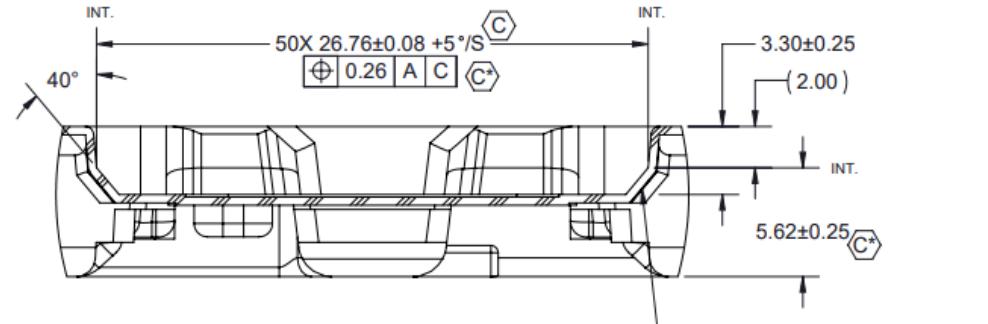


| | |
|-------------------------------|-----------------|
| Pockets | 5 x 10 |
| Tray Length (mm) | 322.60 ± 0.35mm |
| Tray Width (mm) | 135.90 ± 0.35mm |
| Tray Thickness (mm) | 7.62 ± 0.35mm |
| X Axis 1st Pick-Up Point (mm) | 26.3mm |
| Y Axis 1st Pick-Up Point (mm) | 20.95mm |
| X-Axis Pitch (mm) | 30.00mm |
| Y-Axis Pitch (mm) | 23.50mm |

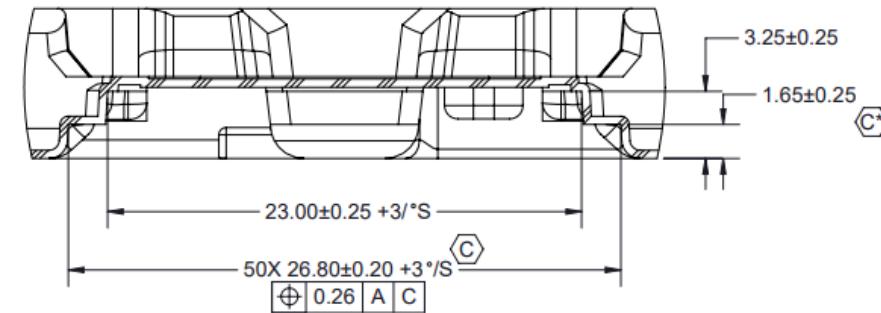


4.2 Thermoform Tray (TFT) Drawing

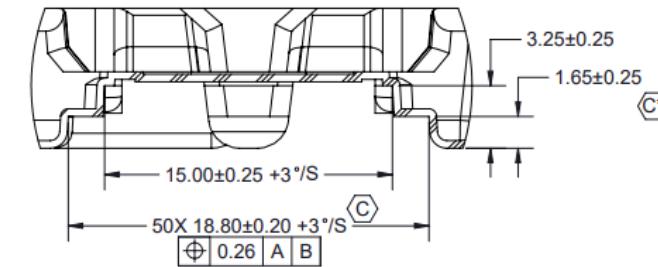
Tiger Lake UP4 (26.5x18.5 mm) - 2 of 2 slides



DETAIL B
SCALE 4 : 1



DETAIL E
SCALE 4 : 1



Notes:

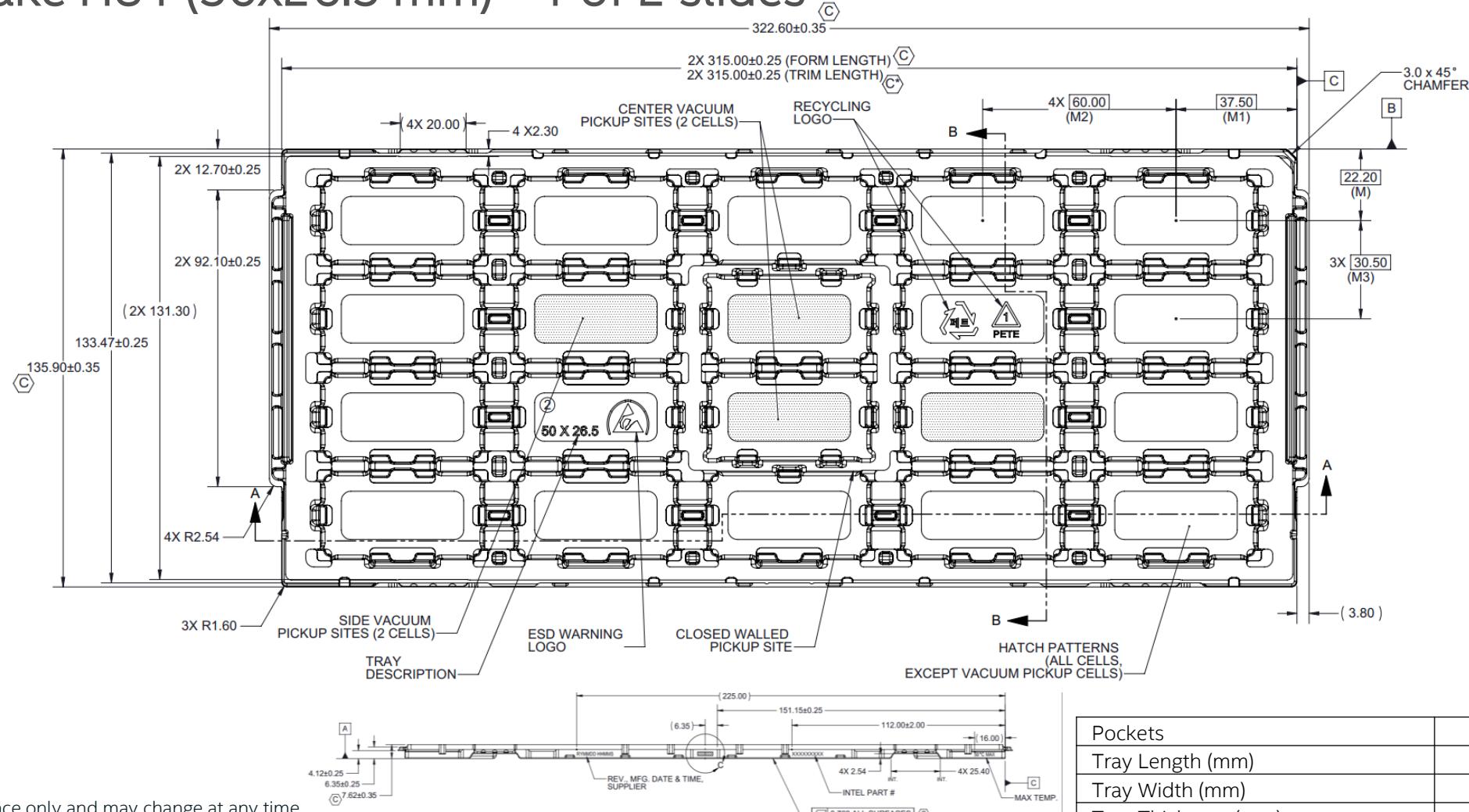
- Information is for reference only and may change at any time.
- Intel Drawing # 500330055 – Rev2
- The above TFT can only be heated to 50°C. However, a Modified Poly-Phenylene Oxide (MPPO) material that it is used for higher temp baking is bake able to 150°C max. Our high temp tray supplier is Daewon (IPN: 500334693 / Daewon part number TR174094). Other similar trays may exist. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs.
- Daewon contact: relee@daewonspic.com

| | |
|-------------------------------|--------------|
| Pocket X top dimension | 26.76±0.08mm |
| Pocket X bottom dimension | 26.80±0.20mm |
| Pocket Y top dimension | 18.76±0.08mm |
| Pocket Y bottom dimension | 18.8±0.20mm |
| Top Pocket Depth dimension | 3.30±0.25mm |
| Bottom Pocket Depth dimension | 3.25±0.25mm |



4.2 Thermoform Tray (TFT) Drawing

Tiger Lake H81 (50x26.5 mm) - 1 of 2 slides



Notes:

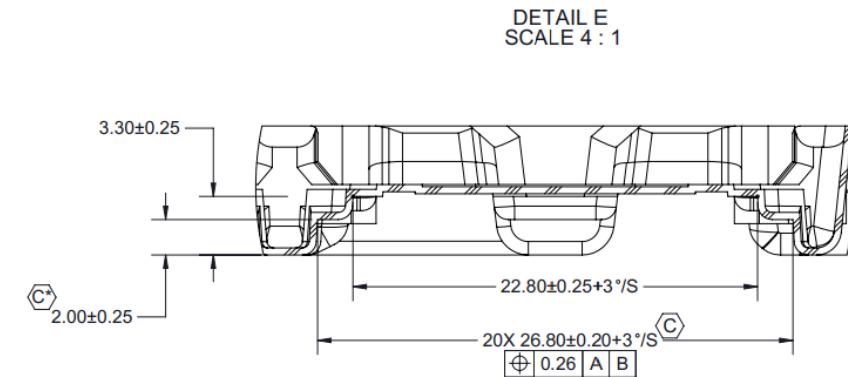
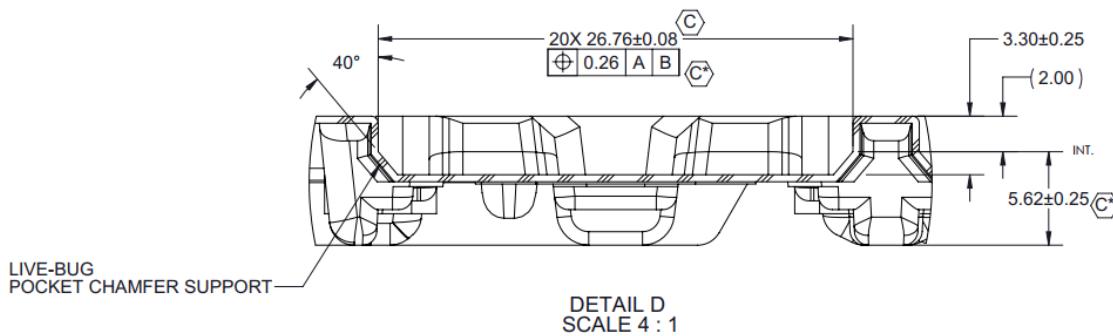
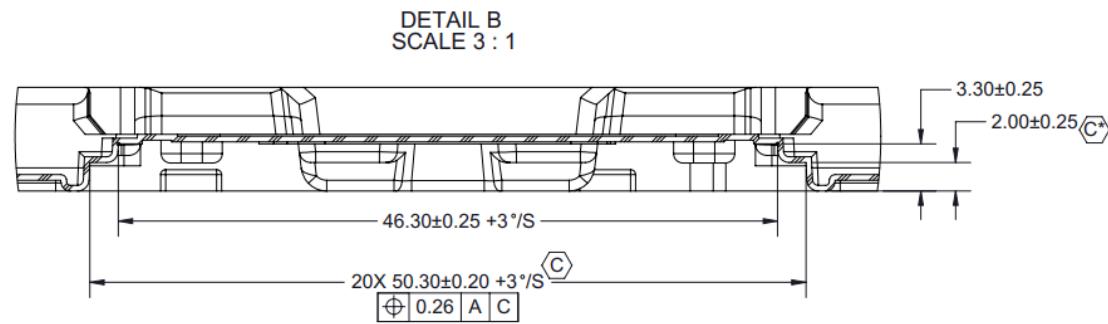
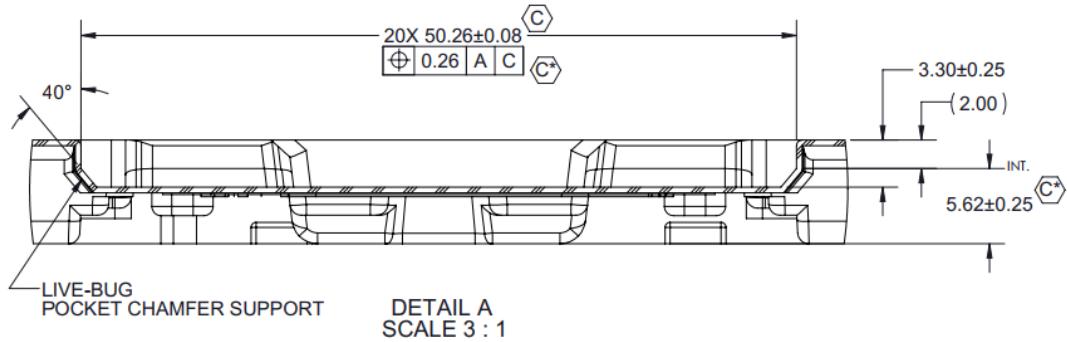
- Information is for reference only and may change at any time.
- Intel Drawing # 500403669 – Rev1
- The above TFT can only be heated to 50°C. However, a Modified Poly-Phenylene Oxide (MPO) material that it is used for higher temp baking is bake able to 150°C max. Our high temp tray supplier is Daewon (IPN: 500397706 / Daewon part number TR198046). Other similar trays may exist. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs.
- Daewon contact: relee@daewonspic.com

| | |
|-------------------------------|----------------------|
| Pockets | 4×5 |
| Tray Length (mm) | 322.60 ± 0.35 mm |
| Tray Width (mm) | 135.90 ± 0.35 mm |
| Tray Thickness (mm) | 7.62 ± 0.35 mm |
| X Axis 1st Pick-Up Point (mm) | 41.3mm |
| Y Axis 1st Pick-Up Point (mm) | 22.20mm |
| X-Axis Pitch (mm) | 60.00mm |
| Y-Axis Pitch (mm) | 30.50mm |



4.2 Thermoform Tray (TFT) Drawing

Tiger Lake H81 (50x26.5 mm) – 2 of 2 slides



Notes:

- Information is for reference only and may change at any time.
- Intel Drawing # 500403669 – Rev1
- The above TFT can only be heated to 50°C. However, a Modified Poly-Phenylene Oxide (MPP0) material that it is used for higher temp baking is bake able to 150°C max. Our high temp tray supplier is Daewon (IPN: 500397706 / Daewon part number TR198046). Other similar trays may exist. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs.
- Daewon contact: relee@daewonspic.com

| | |
|-------------------------------|---------------------|
| Pocket X top dimension | 50.26 ± 0.08 mm |
| Pocket X bottom dimension | 50.30 ± 0.20 mm |
| Pocket Y top dimension | 26.76 ± 0.08 mm |
| Pocket Y bottom dimension | 26.80 ± 0.20 mm |
| Top Pocket Depth dimension | 3.30 ± 0.25 mm |
| Bottom Pocket Depth dimension | 3.30 ± 0.25 mm |



4.2 Tape & Reel (T&R) Information

Tiger Lake PCH (25x24 mm)

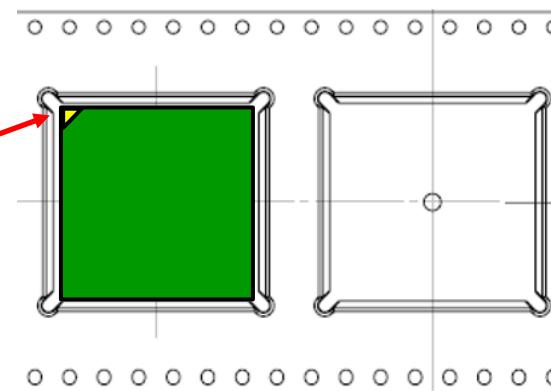
Orientation Guide



Direction of Unreeeling

| Component Package | QFN (Square Geometry) | QFN (Rectangular Geometry) | BGA (Square Geometry) | BGA (Rectangular Geometry) | LCC | | | | | | | | | | | | | | | | | | | | |
|--------------------------------------|--|----------------------------|-----------------------|----------------------------|-----|--|---|---|---|---|--|---|---|---|---|--|---|---|---|---|--|---|---|---|---|
| Orientation in carrier | | | | | | | | | | | | | | | | | | | | | | | | | |
| Termination; Orientation by Quadrant | <table border="1"><tr><td>1</td><td>2</td></tr><tr><td>4</td><td>3</td></tr></table> | 1 | 2 | 4 | 3 | <table border="1"><tr><td>1</td><td>2</td></tr><tr><td>4</td><td>3</td></tr></table> | 1 | 2 | 4 | 3 | <table border="1"><tr><td>1</td><td>2</td></tr><tr><td>4</td><td>3</td></tr></table> | 1 | 2 | 4 | 3 | <table border="1"><tr><td>1</td><td>2</td></tr><tr><td>4</td><td>3</td></tr></table> | 1 | 2 | 4 | 3 | <table border="1"><tr><td>1</td><td>2</td></tr><tr><td>4</td><td>3</td></tr></table> | 1 | 2 | 4 | 3 |
| 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 3 | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 3 | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 3 | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 3 | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 3 | | | | | | | | | | | | | | | | | | | | | | | | |

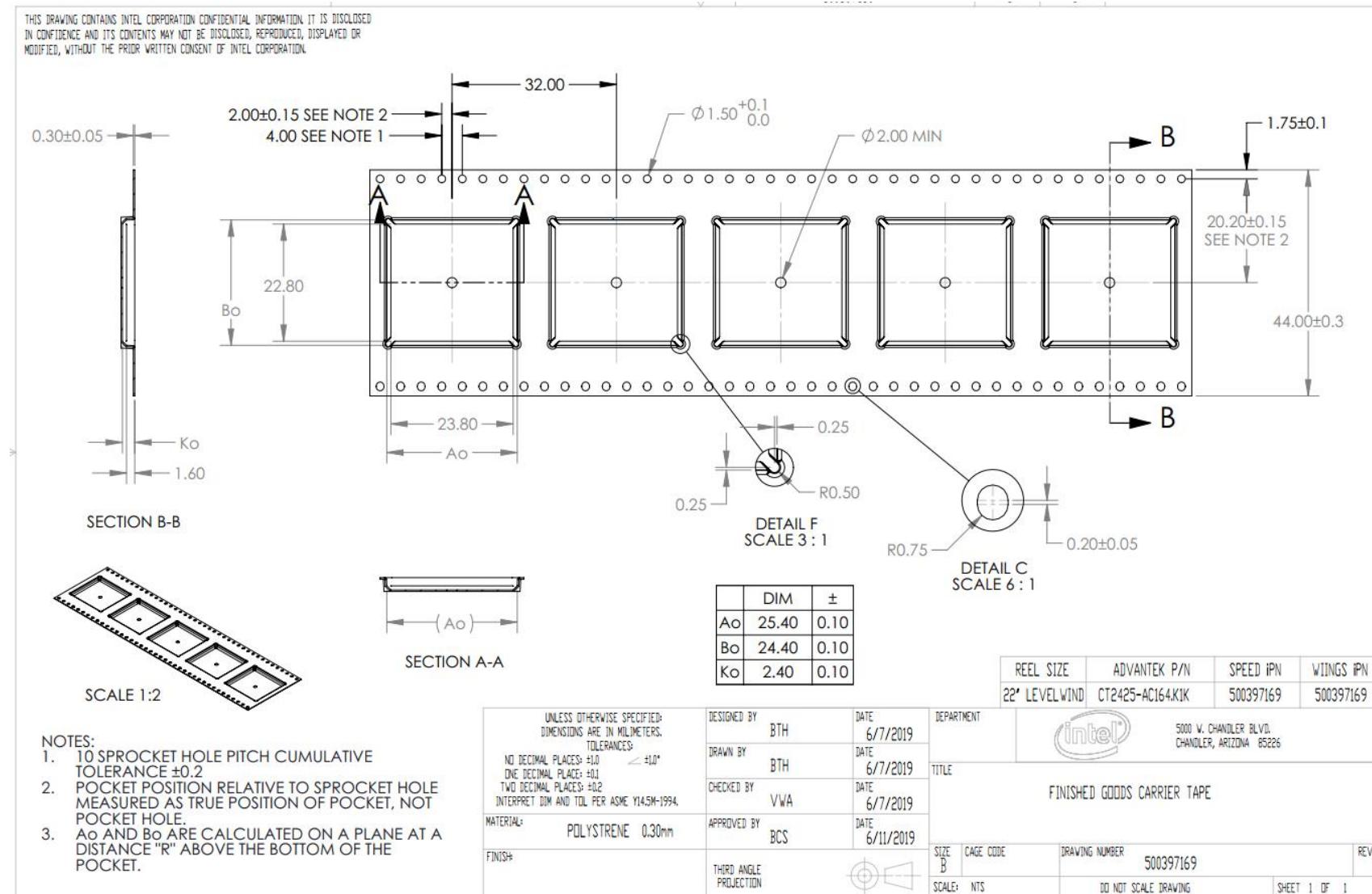
Substrate Pin 1 located
in Quadrant 1 for TGL
PCH-H carrier tape





4.2 Tape & Reel (T&R) Information

Tiger Lake PCH (25x24 mm)



Notes:

- Information is for reference only and may change at any time.
- Intel Drawing # 500397169 – Rev1



4.3 FCBGA Pre-SMT Bake Requirements

- **Moisture Concerns:** Moisture exposure in solder-down devices (e.g. BGA products) can lead to manufacturing defects.¹
- To avoid these humidity-related defects during SMT process, moisture needs to be removed from the product before SMT. As such, a pre-SMT Bake is recommended in either of these 2 conditions:
 1. Humidity in the Moisture Barrier Bag (MBB) exceeds the level indicated by Humidity Indicator Card (HIC)² or
 2. The floor life³ has been exceeded⁴
- **Three Pre-Solder Bake Options:**⁵
 1. High Temp Bake (using High Temp JEDEC Trays or no shipping media):
 2. Medium Temp Bake (using a Medium Temp JEDEC Trays or no shipping media.):
 3. Low Temp Bake (using Thermoform Tray or Tape & Reel media):



Humidity Indicator Card (HIC)¹



Desiccant



Moisture Barrier Bag (MBB)

| Package Body | Moisture Sensitivity Level (MSL) | High Temp Bake @ 125°C +10/-0 °C ⁶ | | Medium Temp Bake @ 90°C + 8°/-0 °C ≤ 5% RH | | Low Temp Bake @ 40°C +5/-0 °C ≤ 5% RH | |
|-------------------|----------------------------------|---|--------------------------------|--|-----------------------------|---------------------------------------|--------------------------------|
| | | Exceeding Floor Life by > 72 h | Exceeding Floor Life by ≤ 72 h | Exceeding Floor Life > 72 h | Exceeding Floor Life ≤ 72 h | Exceeding Floor Life by > 72 h | Exceeding Floor Life by ≤ 72 h |
| Thickness ≤ 1.4mm | 3 | Bake 9 hours | Bake 7 hours | Bake 33 hours | Bake 23 hours | Bake 13 days | Bake 9 days |

Notes:

- ¹ See JEDEC J-STD-033 for more details.
- ² See JEDEC J-STD-033 for more details, including interpretation of HIC card.
- ³ Floor Life is defined per JEDEC STD-033 as the allowable time period between removal of moisture-sensitive devices from a moisture-barrier bag, dry storage, or dry bake and the solder process. Floor life is 168 hours at ≤30 °C/60% RH (for MSL3).
- ⁴ Floor life in the open MBB (out of MBB) depends on the product Moisture Sensitive Level (MSL). MSL rating is printed on the label of a standard intermediate box "LEVEL <N>" and on the label of a MBB "LEVEL <N>".
- ⁵ The Plastic Injection Molded Tray (PIMT) material that it is used for high temperature baking is called Modified Polyphenylene oxide, and it is able to 150C max. A different kind of PIMT made with material MPSU2 is an ultra light tray made by Daewon. It can be baked to a max of 100C. The Thermoform Tray (TFT) is made of Polyethylene Teraphthalate (PETE) and it is good to 50C MAX, this is "printed" on the side of the TFT. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs. For a MSL other than MSL 3, see JEDEC J-STD-033 for more details.
- ⁶ Baking for ≥48 hours at 125°C could lead to solder ball oxidation.



4.4.1 Tray Package Handling BKMs:

1. General Tray Handling Do's and Don'ts
2. Tray Box Handling Recommendations
3. Tray Stack Handling Recommendations
4. Tray Inspection Recommendations
5. Assisted Vacuum Wand Recommendations
6. Unassisted Vacuum Wand Recommendations
7. Tray Manual Handling
8. Additional References



4.4.1 Tray Package Handling BKM^s: Manual Handling Best Practices

Do:

- Minimize manual handling as much as possible
- Ensure all packages are in the tray pocket before picking them up
- If package is found to be out of pocket the operator should gently reseat the package in the tray pocket
- Use assisted (active vacuum¹) vacuum pens to gently pick up the packages from the tray pocket
- Reuse UPS covers if a tray stack is split

Do not:

- Press down hard on the package
- Pick packages that are out of pocket
- Use hands to pick up the package whenever possible
- Discard UPS covers after removal
- Place desiccant directly on top of the tray stack without a UPS cover between the top empty tray and the desiccant

Notes:

- ¹Unassisted vacuum pens and manual handling represent an increased risk of applying downward force on the package and should be used with caution

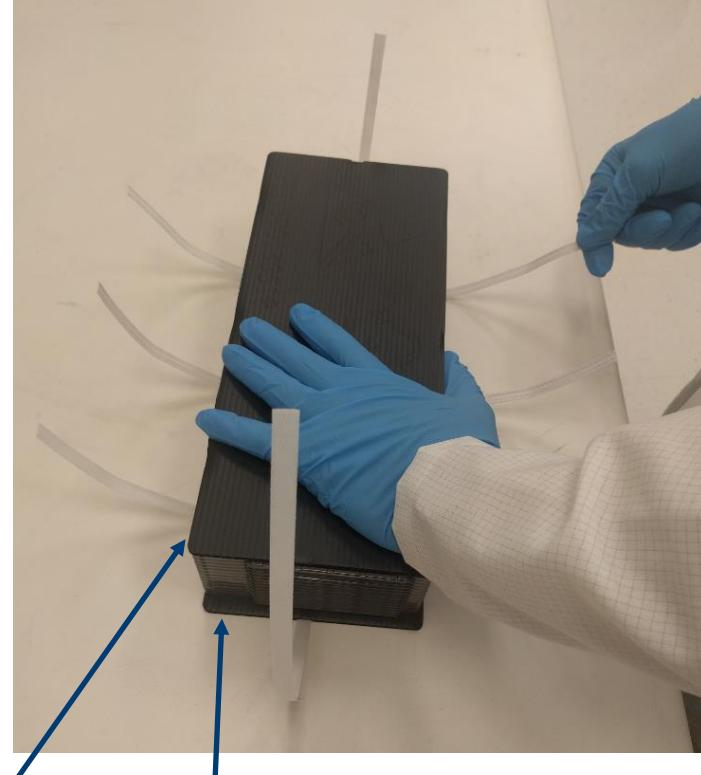


4.4.2 Tray Package Handling BKMs: Tray Box Handling Recommendations

- Always use two hands to hold the box, and always gently put the box on table ensuring the box is level to the table so it is not tilted



- Always use one hand to hold the tray bundles when removing the straps
- Do not discard UPS covers after removal; reuse UPS covers if a tray stack is split



UPS (Universal Plastic Shims)



4.4.3 Tray Package Handling BKMs: Tray Stack Handling Recommendations



Universal Plastic Shim (UPS)



Desiccant on top of the UPS



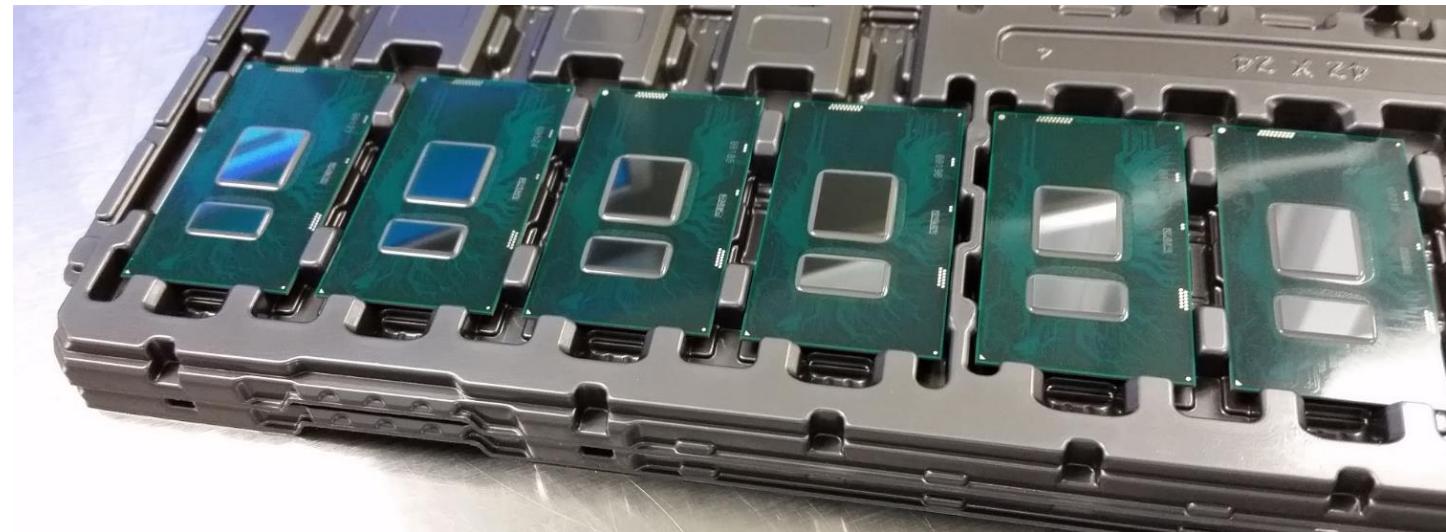
- Do not discard the UPS covers after removal. Instead, save and reuse the UPS covers if a tray stack is split into smaller stacks
- Always make sure tray stacks have a UPS cover on the top and bottom, to protect the components
- Always place a UPS cover between the top empty tray and the desiccant, to prevent tray and package deformation during MBB vacuum

- Do not carry trays without the top and bottom UPS covers
- Always use two hands to hold the tray bundle for short distance movement
- Do not carry tray bundles taller than the width of your hands (thumbs on top and fingers below)
- Try to minimize the amount of movement as much as possible after the strap is removed



4.4.4 Tray Package Handling BKM^s: Tray Inspection Recommendations

Packages in Tray



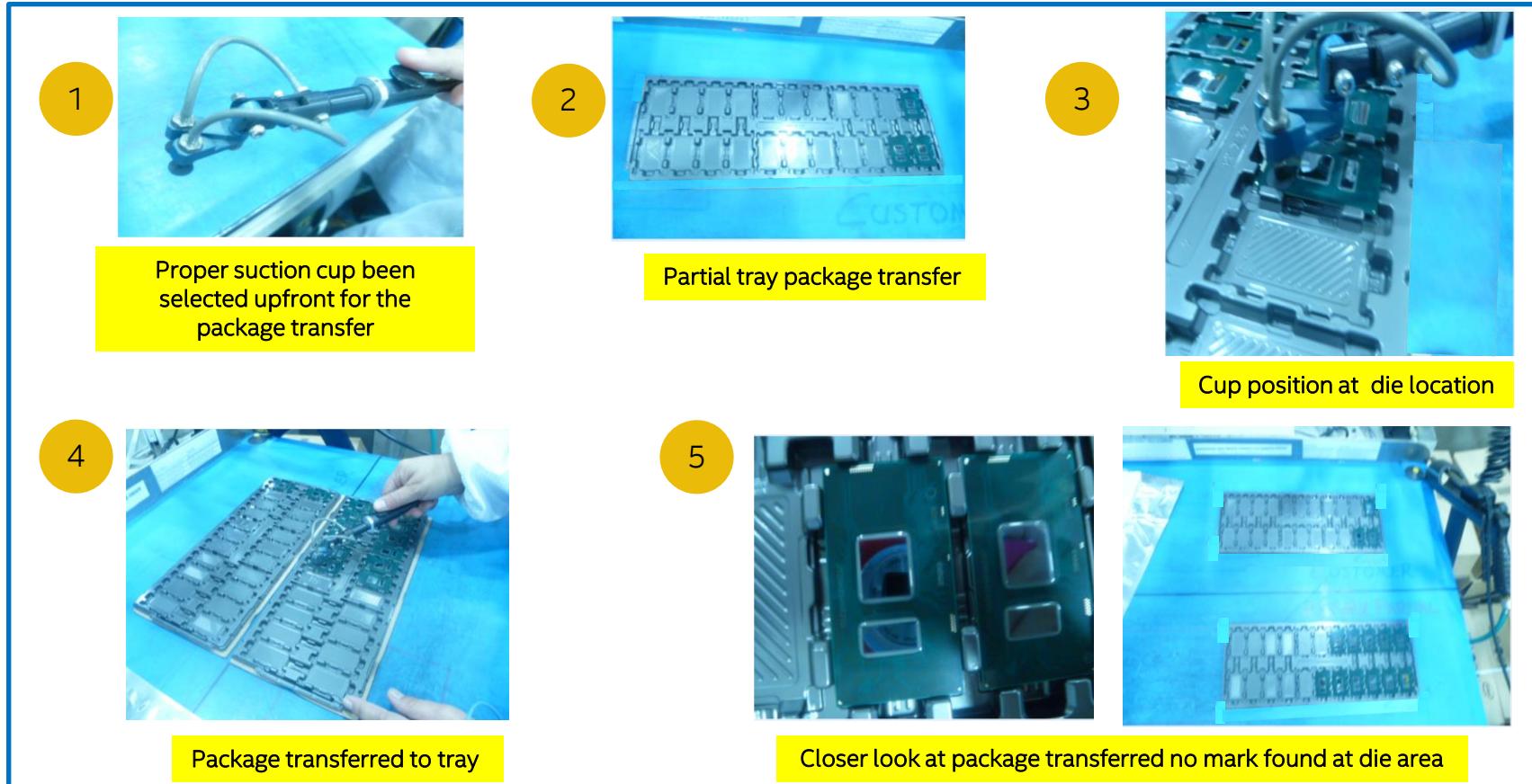
Note: The image shown above is generic

- Make sure all packages are properly seated in the tray pocket
- If package is found to be out of pocket, gently push the edge of the package with a gloved finger or the edge of the suction cup on the vacuum wand to reseat the package



4.4.5 Tray Package Handling BKMs: Assisted Vacuum Wand Recommendations

Example: Using Vacuum wand with proper suction cup



Note: The images shown above are generic

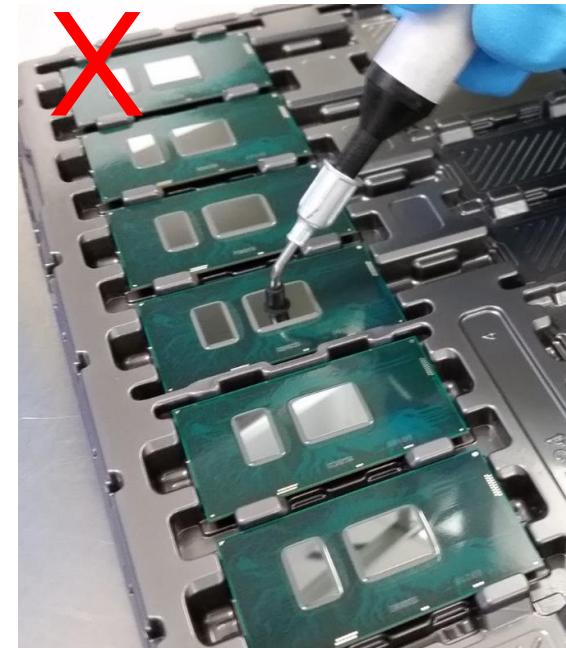
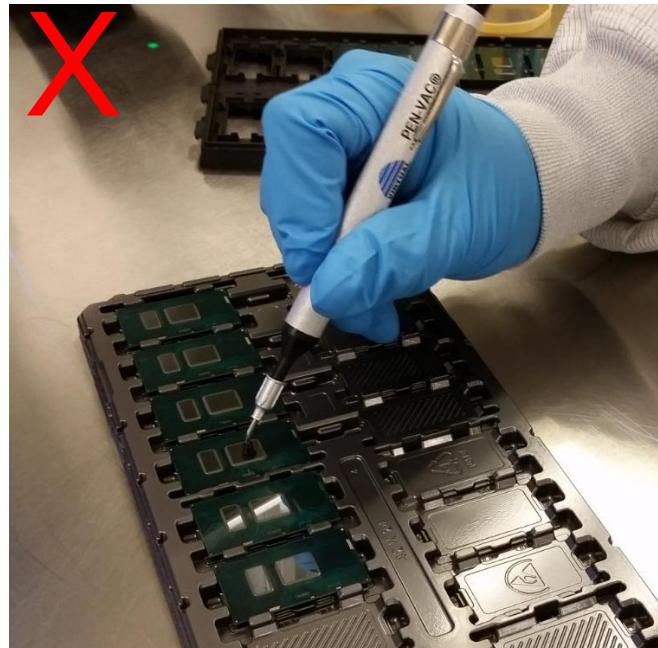


4.4.6 Tray Package Handling BKMs: Unassisted Vacuum Wand Recommendations

Vacuum Pen / Wand Recommendations

Unassisted (no active vacuum) Vacuum Pen is NOT recommended as it may:

- Cause the operator to drop the packages which can induce bending through manual handling
- Cause excessive load to the package and bend the package



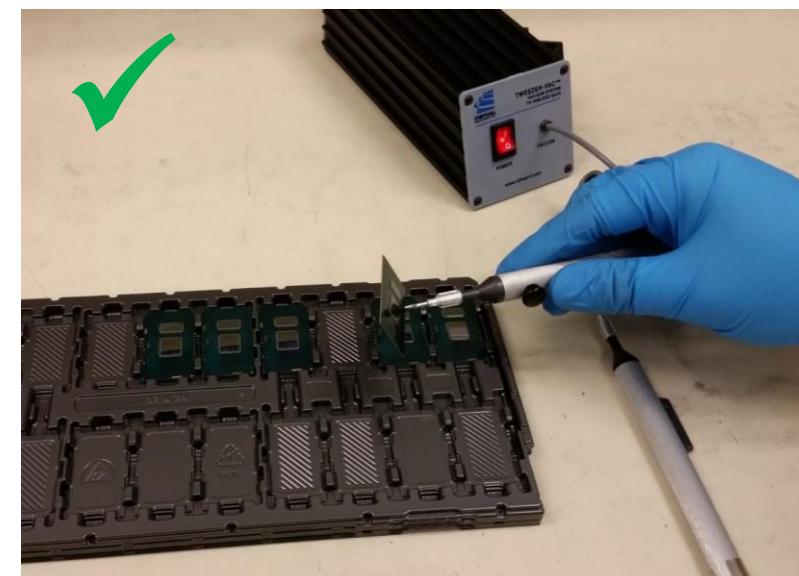
Note: The images shown above are generic



4.4.6 Tray Package Handling BKM^s: Unassisted Vacuum Wand Recommendations

Vacuum Pen Recommendations

Recommend using a tool with active vacuum as a safer method to handle package (i.e., less likely to damage the package).



Note: The images shown above are generic

Package is not bent when using vacuum pen as less pressure is required to maintain good suction (manual handling of the package, as seen on the left, is not recommended).



4.4.7 Tray Package Handling BKM^s: Tray Manual Handling

Manual handling of packages is NOT Recommended as this can induce bending of the package as it is picked up



Package bent from trying to pick up in tray by pushing down on middle of package to grip the edge.

Note: The images shown above are generic



4.4.7 Tray Package Handling BKM^s: Tray Manual Handling

- If you are going to do re-pack certain units, please remember:
 - Reuse UPS covers if a tray stack is split
 - Strapping: Do not strap too tightly (no visible crimping or deformation)
 - Vacuum: Do not **over** vacuum (refer to JEDEC Spec J-STD 033)
 - Recommend vacuum setting = 0sec (light air removal only)
 - Always place a UPS cover between the top empty tray and the desiccant, to prevent tray and package deformation
 - Over vacuum may cause package deformation
 - Over vacuum may also cause the desiccant to not work properly

Over-vacuumed illustration

The bag **tightly vacuumed** around the trays:

1. Beads across surface of desiccant pouches **clearly** visible through MBB
2. Tray straps **well defined** through MBB
3. Features of trays **visible** through MBB



Desiccant on top of the UPS



Light air removal illustration



Note: The images shown above are generic



4.4.8 Tray Package Handling BKMs: Additional References

| Title | Intel® Learning Network ¹ | RDC Document Number ² |
|---|--------------------------------------|----------------------------------|
| Manufacturing with Intel® Products: Transportation Materials and Media Handling and Usage | 17891 | 619185 |

Please note that the above reference(s) provide the latest information related to handling.

Notes:

- ¹Intel® Learning Network - <http://learn.intel.com>
- ²Resource & Design Center (RDC) - <http://rdc.intel.com>
- Contact your Intel representative for all document access questions.



4.5 T&R Package Handling BKMs:

1. General T&R Handling Do's and Don'ts
2. Avoid These Things When Handling
3. Recommendations
4. Standard Intel Packing Information
5. Warehouse Handling Information
6. Unpacking Process BKMs
7. Counting Packages for Tape & Reel
8. Tape & Reel Repacking
9. Additional References



4.5.1 T&R Package Handling BKM^s: Manual Handling Best Practices

Do:

- Minimize manual handling as much as possible
- Ensure all packages are in the T&R pocket before picking them up
- Use assisted (active vacuum¹) vacuum pens to gently pick up the packages from the T&R pocket
- Reuse protective band (if applicable)

Do not:

- Press down hard on the package
- Use hands to pick up the package whenever possible
- Discard protective band (if applicable)

Notes:

- ¹Unassisted vacuum pens and manual handling represent an increased risk of applying downward force on the package and should be used with caution



4.5.2: T&R Package Handling BKMs: Avoid These Things When Handling



Do not hold the T&R with one hand,
as it might cause package bending.

During setup on feeder, do not twist or bend
the tape. Handle the T&R gently.



Do not lay the T&R packages on the table or the floor.



4.5.3: T&R Package Handling BKMs: Recommendations



Support T&R with hand when removing from
Moisture Barrier Bag (MBB).

Note: Use scissors to cut off tape and do not use hands to tear off



4.5.4: T&R Package Handling BKMs: Standard Intel Packing Information

| Pack Type | I-Box (outside view) | MBB Bundle (inside contents) |
|---------------|--|---|
| Tape and Reel |  |  |

Make sure there is no damage on I-Box and MBB. Refer to I-Box and MBB handling MAS collaterals for more detailed information.

4.5.5: T&R Package Handling BKMs:

Warehouse Handling Information

| Scenario | Pictures | Do's | Don'ts | Comments |
|-------------------|----------|--|---|--|
| I-Box on conveyor | | <ul style="list-style-type: none"> Follow I-Box indicated stack orientation (horizontal) T&R maximum stack of 4 layers | <ul style="list-style-type: none"> Wrong stack orientation (vertical) Stack layers over the maximum of 4 layers | <ul style="list-style-type: none"> Box stacking to any degree is not recommended. Box <u>over-</u> stacking is definitely not recommended because it may induce I-Box deformation (and unit damage). |
| I-Box storage | | <ul style="list-style-type: none"> Store I-Box in shipping cage or shelf bins. T&R maximum stack: 6 layers. | <ul style="list-style-type: none"> Over the stack layers Stack MBB bundles | MBB bundle-stacking is never recommended as may damage the MBB |

4.5.5: T&R Package Handling BKMs: Warehouse Handling Information

| Scenario | Pictures | Do's | Don'ts | Comments |
|----------------|---|---|---|---|
| I-Box movement |    | <ul style="list-style-type: none">• Use shipping cage for short distance (<200m) movement, and use space-holders to occupy free space• Use over-pack + shrink wrapped pallet for long-distance movement | <ul style="list-style-type: none">• Do not have excess space for potential unwanted I-Box movement during transit• Do not over-stack boxes | I-Box can become damaged if have too much free space in shipping cage |



4.5.5: T&R Package Handling BKMs: Warehouse Handling Information

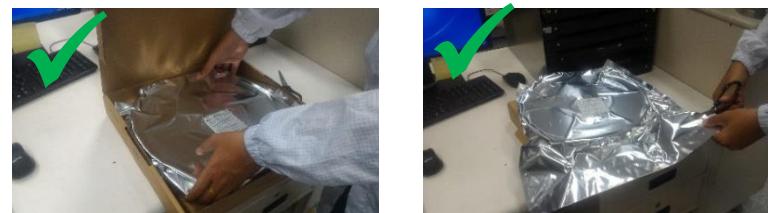
| Scenario | Pictures | Do's | Don'ts | Comments |
|---------------------|---|---|--|--|
| Rewrap |   | <p>Utilize proper vacuum level:</p> <ul style="list-style-type: none"> desiccant outline is clear but beads are not clear reel outline is clear no signs of carrier tape or pockets imprint on MBB | <ul style="list-style-type: none"> Do not over vacuum (refer to JEDEC Spec J-STD 033) Recommend vacuum setting = 0sec (light air removal only) | <ul style="list-style-type: none"> Over vacuum may cause package deformation Over vacuum may also cause the desiccant to not work properly |
| MBB bundle movement |   | <ul style="list-style-type: none"> Use two hands to hold MBB bundles for short distance (<30m), label side facing up Hold 1 bundle per movement | <ul style="list-style-type: none"> Do not use one hand/arm to hold MBB bundles Do not hold >1 bundles per movement | For long distance movement, use appropriate trolley |

4.5.6: T&R Package Handling BKM^s: Unpacking Process BKM^s

- Gently put the box on the table following the top indicator and cut the sealing tape using scissors



- Remove the bundle from the box and cut the MBB using scissors



- Always keep the protective band for future repacking process (if applicable).



4.5.7: T&R Package Handling BKMs: Counting Packages for Tape & Reel

- Intel does not recommend manual cycle counting, as it can cause package damage
- If cycle counting needs to be performed, use a standard counting machine for package counting (example shown below)

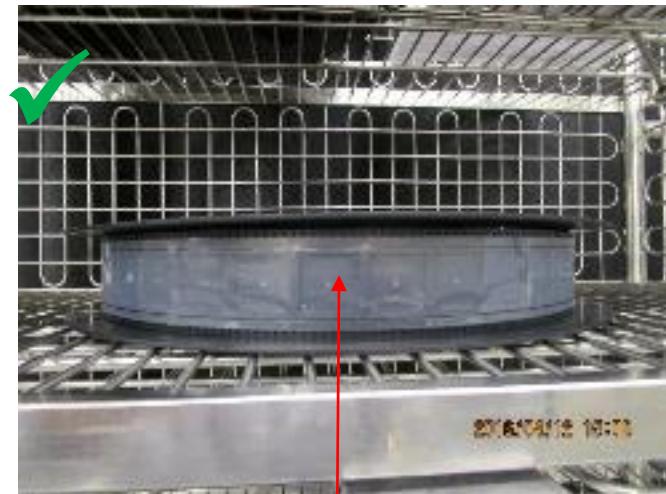


Notes:

- Other names and brands may be claimed as the property of others.

4.5.8: T&R Package Handling BKMs: Tape & Reel Repacking

- The remnant units in reel need to be protected with at least 1 circle of empty carrier tape at outer (Leader) and end-side (Trailer), or protective band at outer side.



Empty Carrier Tape
(Leader)



Protective Band (if applicable)

Notes:

Leader = Empty pockets at the end of the reel

Trailer = Empty pockets closest to the hub of the reel



4.5.9 T&R Package Handling BKMs: Additional References

| Title | Intel® Learning Network ¹ | RDC Document Number ² |
|---|--------------------------------------|----------------------------------|
| Manufacturing with Intel® Products: Transportation Materials and Media Handling and Usage | 17891 | 619185 |

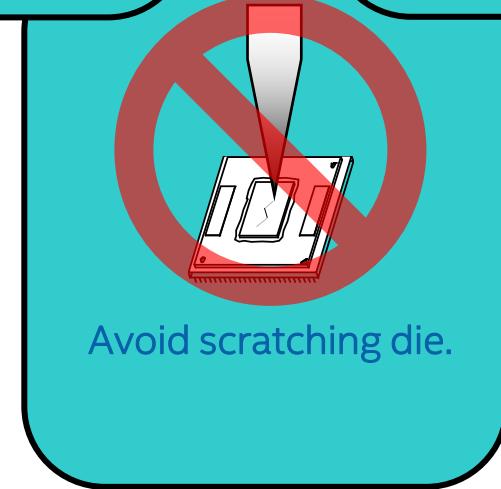
Please note that the above reference(s) provide the latest information related to handling.

Notes:

- ¹Intel® Learning Network - <http://learn.intel.com>
- ²Resource & Design Center (RDC) - <http://rdc.intel.com>
- Contact your Intel representative for all document access questions.



4.5.10 Processors General Handling Recommendations



Module 5: Testing

Manufacturing with the Intel® Platform Code Named Tiger Lake

Overview – Table of Contents

| | | | | | | |
|--|--|--|--|------------------------------------|--|--|
| Module 1: <u>Component Attributes and Drawings</u> | Module 2: <u>Land Pattern (PCB Pad) Design Guidelines</u> | Module 3: <u>Manufacturing Guidelines</u> | Module 4: <u>Shipping & Handling</u> | Module 5: <u>Testing</u> | Module 6: <u>System Integration & ESD Considerations</u> | Module 7: <u>References</u> |
| 1.1 Package Attributes Intel® FCBGA Processors 1.2 Package Mechanical Drawings (PMD) FCBGA Processors 1.3 Package Attributes PCH 1.4 Package Mechanical Drawings (PMD) PCH | 2.1 Land Pattern Design Guidelines Introduction 2.2 Mother Board Cavity Voiding Requirements 2.3 Land Pattern Design Guidelines (for the different processors & chipset) | 3.1 Introduction 3.2 Example Package Dynamic Warpage Data 3.3 Critical SMT Recommendations 3.4 Manufacturing Guidelines General Info 3.5 Solder Paste Formulation Optimization 3.6 Solutions to Extend Stencil Aperture Area Ratio 3.7 Cu Core Standoff Technology 3.8 Solder Paste Volume Optimization Stencil Design Recommendations 3.9 SMT Reflow Pallet Recommendations 3.10 SMT Reflow Profile TC Location 3.11 Overview of Board Flexure 3.12 Board Level Adhesive Overview 3.13 Package Rework 3.14 FACR Prep Process | 4.1 Processor and Chipset Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements 4.4 BGA Package Handling BKMs 4.5 T&R Package Handling BKMs | 5.1 Test Information | 6.1 Introduction 6.2 Electro Static Discharge (ESD) Platform Component Goals 6.3 Electro Static Discharge (ESD) Design Guidelines 6.4 Electro Static Discharge (ESD) Additional Resources 6.5 Thermal Solution Assembly / Disassembly considerations | 7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Resource Design Center access Information |



Acronyms Found in this Module

| | |
|-----|---------------------------------|
| MAS | Manufacturing Advantage Service |
| ME | Management Engine |
| RDC | Resource & Design Center |
| TGL | Tiger Lake |



5.1 Test Information

For Tiger Lake test information refer to:

Manufacturing Test with Intel® Management Engine (Intel® ME) Firmware version 15.x on Tiger Lake Mobile and Desktop Platforms, RDC#626295

Module 6: System Integration & ESD Considerations

Manufacturing with the Intel® Platform Code Named Tiger Lake

Overview – Table of Contents

| | | | | | | |
|---|--|--|--|------------------------------------|--|--|
| Module 1: <u>Component Attributes and Drawings</u> | Module 2: <u>Land Pattern (PCB Pad) Design Guidelines</u> | Module 3: <u>Manufacturing Guidelines</u> | Module 4: <u>Shipping & Handling</u> | Module 5: <u>Testing</u> | Module 6: <u>System Integration & ESD Considerations</u> | Module 7: <u>References</u> |
| 1.1 Package Attributes Intel® FCBGA Processors 1.2 Package Mechanical Drawings (PMD) FCBGA Processors 1.3 Package Attributes PCH 1.4 Package Mechanical Drawings (PMD) PCH | 2.1 Land Pattern Design Guidelines Introduction 2.2 Mother Board Cavity Voiding Requirements 2.3 Land Pattern Design Guidelines (for the different processors & chipset) | 3.1 Introduction 3.2 Example Package Dynamic Warpage Data 3.3 Critical SMT Recommendations 3.4 Manufacturing Guidelines General Info 3.5 Solder Paste Formulation Optimization 3.6 Solutions to Extend Stencil Aperture Area Ratio 3.7 Cu Core Standoff Technology 3.8 Solder Paste Volume Optimization Stencil Design Recommendations 3.9 SMT Reflow Pallet Recommendations 3.10 SMT Reflow Profile TC Location 3.11 Overview of Board Flexure 3.12 Board Level Adhesive Overview 3.13 Package Rework 3.14 FACR Prep Process | 4.1 Processor and Chipset Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements 4.4 BGA Package Handling BKMs 4.5 T&R Package Handling BKMs | 5.1 Test Information | 6.1 Introduction 6.2 Electro Static Discharge (ESD) Platform Component Goals 6.3 Electro Static Discharge (ESD) Design Guidelines 6.4 Electro Static Discharge (ESD) Additional Resources 6.5 Thermal Solution Assembly / Disassembly considerations | 7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Resource Design Center access Information |



Acronyms Found in this Module

| | |
|-----|--------------------------|
| CDM | Charge Device Model |
| ESD | Electro-Static Discharge |
| HBM | Human Body Model |



6.1 System Integration & ESD Considerations Introduction

- This module covers both Electro-Static Discharge (ESD) and Thermal Solution Assembly & Disassembly considerations for this platform.



6.2 ESD Considerations

Tiger Lake Platform Component ESD Goal

| Attributes | | Tiger Lake Platform Components | |
|----------------------------|-----------------------------|--------------------------------|---------------------------|
| Stress Model | Spec # | Stress Condition | Test Results ¹ |
| ESD – Human Body Model | ANSI/ ESDA/ JEDEC JS-001 | ±1000 V | Pass ² |
| ESD – Charged Device Model | ANSI/ ESDA/ JEDEC JS-002 | ±250 V | Pass ² |
| Latch-up – Vcc | JESD78 | 1.5x VCC | Pass ² |
| Latch-up – I/O | JESD78 | I _{pin} = ±100 mA | Pass ² |

²The ESD test results provided currently reflect TGL UP3/H35 and TGL PCH. Other product's ESD test results will be updated in a future release.

Notes:

- ¹Testing will include the Tiger Lake Platform FCBGA processors and chipset.
- Reference Only. Refer to the latest rev of the [Manufacturing with Intel® Products: ESD/EOS Awareness & Preparedness MAS](#)



6.3 ESD Considerations

Tiger Lake Platform Design Guidelines

- The HBM or CDM goal will not require additional design changes, beyond current platform ESD guidance.
- Related Tiger Lake Mobile Platform Design Guide information, with ESD Section Reference, shown below.

| Doc# | Title | Sections |
|--------|---------------------------------------|----------|
| 607872 | Tiger Lake UP3/H35/UP4 Platform Guide | 5, 6, 9 |



6.4 ESD Considerations

Additional Resources

For all additional ESD detail and resources, see below.

Intel Resources:

- Get comprehensive ESD/EOS Awareness & Preparedness from the latest version of *Manufacturing with Intel® Products: ESD/EOS Awareness & Preparedness MAS* (RDC#515426).

External Resources:

- JEDEC Association: www.jedec.org
- ESD Association: www.esda.org
- IEC: <http://www.iec.ch/>
- IPC: <http://www.ipc.org/default.aspx>



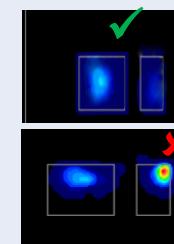
6.5 Considerations During Thermal Solution Assembly/Disassembly (1 of 4)

- Thermal solution assembly/disassembly considerations are aimed at providing guidance to the customers to help prevent risk of die damage that can occur during the thermal solution assembly or disassembly process, or after assembly.
- During the thermal solution assembly/disassembly/repair/rework process, various factors can result in a higher concentrated load, peak pressure and non-uniform pressure distribution that can lead to increased die damage risk. Recommendations are provided in this section to help identify and avoid some of the modulators to reduce the risk of die damage.



6.5 Considerations During Thermal Solution Assembly/Disassembly (2 of 4)

Ideally the load would be distributed as uniformly as possible on the dice during thermal solution assembly/disassembly and after assembly on Intel Component to minimize die damage risk. Load concentration at die edge or die corners during thermal solution assembly/disassembly and after assembly could increase risk of die crack.

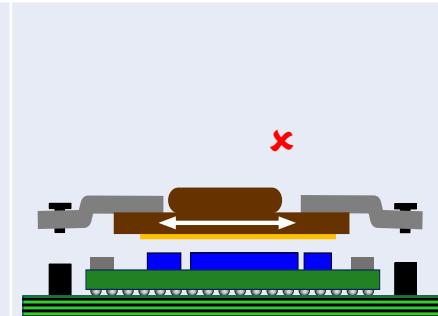


Ensure the value of pressure on dice does not exceed the pressure value specified in Tiger Lake TMDG (RDC# 607873) at anytime during thermal solution assembly/disassembly and after assembly.

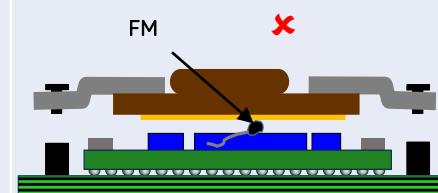
See the Tiger Lake TMDG for details on Intel Reference Thermal Solution Design (where applicable).

Collect mechanical quality and reliability validation data to risk assess thermal Solution assembly process. See *Intel Mobile SoC Die Loading Measurement Techniques*, (RDC#556532)

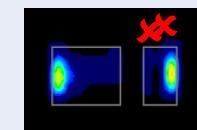
Avoid sliding or dynamic lateral movement of thermal solution on the dice during assembly/ disassembly. Avoid any relative movement between the board, backing plate and thermal solution during assembly/disassembly. This can lead to die damage.



Avoid foreign material (FM) deposited on the dice/ thermal solution surfaces. This can cause concentrated loading on dice during thermal solution assembly/disassembly that can lead to die damage.



Some of the key factors influencing load magnitude and distribution are: 1) Loading Center, 2) TIM type, 3) excess warpage of cold plate, 4) misaligned TIM dispense from die areas, 5) Assembly/disassembly screw sequence, 6) thermal solution tilting during assembly/disassembly and 7) Board support during assembly/disassembly



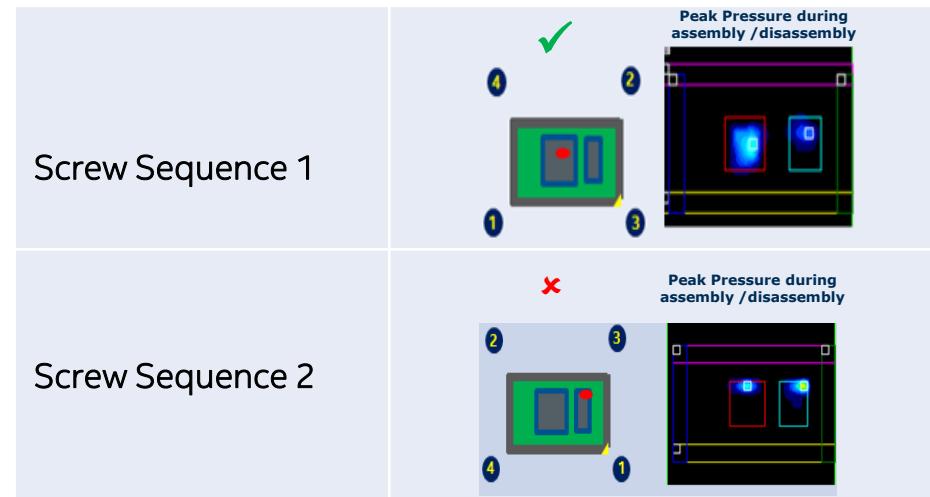
Please note that all the diagrams are example images and not inclusive and representative of all possible scenarios.



6.5 Considerations During Thermal Solution Assembly/Disassembly (3 of 4)

- Ensure screw sequence used for thermal solution assembly/disassembly is optimized to minimize concentrated load during and after assembly process.
 - Every thermal solution design has its own optimum screw sequence that results in minimum concentrated loading during assembly/disassembly and after assembly. It is recommended to choose a screw sequence as per specific thermal solution design to reduce load concentration.
 - Unoptimized screw sequence can result in higher concentrated peak pressure on the dice during assembly/disassembly and after assembly that can lead to die damage.
 - Refer to *Intel Mobile SoC Die Loading Measurement Techniques*, (RDC#556532), for a methodology to determine the optimized screw sequence.

Example of two screw sequence impact on concentrated peak pressure during attachment process of using a specific thermal solution design (4 point) is shown below.



For the specific thermal solution used, screw sequence 1 is preferred over screw sequence 2 as screw sequence 1 gives relatively less load concentration during assembly/disassembly

Please note that all the diagrams are example images and not inclusive and representative of all possible scenarios.

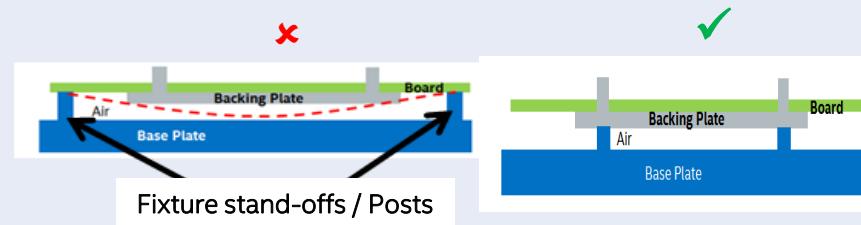


6.5 Considerations During Thermal Solution Assembly/Disassembly (4 of 4)

Ensure the screwdriver used for thermal solution assembly/disassembly is calibrated regularly. Torque of 2.0 kgf-cm or less is recommended for assembly/disassembly process.

Ensure proper placement of board such that no damage is caused to the board and its components during thermal solution assembly/disassembly process.

- Avoid placing board on stand-offs positioned away from the backing plate during attachment of thermal solution. Use of a continuous bottom support is recommended to place the board for thermal solution assembly/disassembly.
- If board is placed on a bottom fixture posts/fixture stand-offs during assembly / disassembly of thermal solution, it is recommended to place the fixture stand-offs/posts under the backing plate. The farther the location of fixture stand-offs from backing plate, the higher the risk of board/ solder joint damage, die corner loading and die damage.



Please refer to Tiger Lake TMDG for Intel recommendation on use of backing plate.

Please note that all the diagrams are example images and not inclusive and representative of all possible scenarios.

Module 7: References

Manufacturing with the Intel® Platform Code Named Tiger Lake

Overview – Table of Contents

| | | | | | | |
|---|--|--|--|------------------------------------|--|--|
| Module 1: <u>Component Attributes and Drawings</u> | Module 2: <u>Land Pattern (PCB Pad) Design Guidelines</u> | Module 3: <u>Manufacturing Guidelines</u> | Module 4: <u>Shipping & Handling</u> | Module 5: <u>Testing</u> | Module 6: <u>System Integration & ESD Considerations</u> | Module 7: <u>References</u> |
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Acronyms Found in this Module

| | |
|------|------------------------------------|
| CNDA | Corporate Non-Disclosure Agreement |
| EDS | External Design Specification |
| ILN | Intel Learning Network |
| MAS | Manufacturing Advantage Service |
| PDG | Platform Design Guide |
| SJQ | Solder Joint Quality |
| TMDG | Thermal & Mechanical Design Guide |



7.1 Reference Documents – slide 1 of 3

| Title | Intel® Learning Network ¹ | Document Number Searchable in RDC ² |
|--|--------------------------------------|--|
| Manufacturing with the Intel® Mobile Platform Code Named Tiger Lake [THIS DOCUMENT] | N/A | 613010 |
| Manufacturing with Intel® FCBGA Components for Solder Joint Quality MAS | 7663 | 506474 |
| Manufacturing with Intel® Products: Adhesive Guidance for Ball Grid Array (BGA) and Package on Package (PoP) | 7671 | 573768 |
| Manufacturing with Intel® Products: ESD/EOS Awareness & Preparedness MAS | 6787 | 515426 |
| Intel® Manufacturing with Intel Components Strain Measurement for Circuit Board Assembly MAS | 10136 | 550235 |
| Manufacturing with Intel® Products: Rework Guidance for Ball Grid Array (BGA), Package on Package (PoP), and Sockets | 9699 | 541231 |
| Surface Mount Technology using Low Temperature Solder Paste MAS | 15372 | 568886 |
| Component Strain Guidance Sheets for the Tiger Lake Mobile Platform Components | N/A | Contact your Intel CQE Representative for Strain Guidance Sheets |

Notes:

- ¹Intel® Learning Network - <http://learn.intel.com>
- ²If you type the provided document number into the search field of RDC it will retrieve the document.
- Contact your Intel representative for all document access questions.



7.1 Reference Documents – slide 2 of 3

| Title | Intel® Learning Network ¹ | Document Number Searchable in RDC ² |
|--|--------------------------------------|---|
| Tiger Lake UP4 Processor line BGA Package Ballout Mechanical Specification | N/A | 607754 |
| Tiger Lake UP3/H35 Processor line BGA Package Ballout Mechanical Specification | N/A | 604917 |
| Tiger Lake Thermal Mechanical Design Guide (TMDG) | N/A | 607873 |
| Tiger Lake UP3/H35/UP4 Package Landside Capacitor (LSC) .DXF and .CLP files | N/A | 608524 |
| Tiger Lake Platform Package Mechanical Drawings | N/A | 576259 |
| Client Thermal Validation BKMs | N/A | 544652 |
| TGL External Design Specification (EDS), V1 | N/A | 575683 |
| TGL External Design Specification (EDS), V2 | N/A | 575681 |
| Tiger Lake UP3/H35/UP4 Platform Design Guide (PDG) | N/A | 607872 |
| Tiger Lake Platform UP4 DDR4 RVP – Technical Documentation Kit (TDK) | N/A | 610815 |
| Tiger Lake Platform UP3/H35 DDR4 RVP – Technical Documentation Kit (TDK) | N/A | 609003 |

Notes:

- ¹Intel® Learning Network - <http://learn.intel.com>
- ²If you type the provided document number into the search field of RDC it will retrieve the document.
- Contact your Intel representative for all document access questions.



7.1 Reference Documents – slide 3 of 3

| Title | Intel® Learning Network ¹ | Document Number Searchable in RDC ² |
|---|--------------------------------------|---|
| Tiger Lake UP3/H35 Platform Symbol | N/A | 615721 |
| Tiger Lake UP4 Platform Symbol | N/A | 615488 |
| Tiger Lake Platform – Message of the Week (MOW) | N/A | 611101 |
| Tiger Lake U Mobile Platform - Consumer and Corporate Dashboard | N/A | 613748 |
| Tiger Lake UP4 Platform Stackup RIMB (Recess in Motherboard) Interference UPM (Units per Million) Calculator Tools | N/A | 614089 |
| Tiger Lake PCH H BGA Package Ballout | N/A | 615462 |
| Tiger Lake PCH H Platform Symbol | N/A | 618675 |
| TGL H DDR4 Reference Validation Platform (RVP) TDK | N/A | 618697 |
| TGL H DDR5 Reference Validation Platform (RVP) TDK | N/A | 619361 |
| Tiger Lake PCH BSDL Package File | N/A | 619276 |
| Manufacturing Test with Intel® Management Engine (Intel® ME) Firmware 15.x on Tiger Lake Mobile and Desktop Platforms | 17958 | 626295 |
| Tiger Lake H Platform Design Guide | N/A | 618429 |

Notes:

- ¹Intel® Learning Network - <http://learn.intel.com>
- ²If you type the provided document number into the search field of RDC it will retrieve the document.
- Contact your Intel representative for all document access questions.



7.2 How CNDAs Customers Access Documents from the Intel® Learning Network (ILN)

The screenshot shows two views of the Intel Learning Network interface. The top view is a search results page with a search bar containing '16289'. An orange arrow points down to the second view, which is a detailed course catalog page for the same search term. This page displays two results for 'Manufacturing with Intel Products Diagnostic Enabling (Response Flow Checklist) MAS – For Server MCERR-IERR Rev1.5 (On-Demand-English)'. Both results show a star rating of 0 reviews and a brief description: 'The Manufacturing Diagnostic Enabling (aka Response Flow Checklist) MAS focuses on Intel Server products MCERR-IERR diagnostic Best Known Methods incl...'. The left sidebar includes filters for Popular by Job Role, Popular by Business Group, Featured Training, Topics (Manufacturing Enabling), Training Types (On-Demand), and Published In (Show All, 30 days, 60 days, 1 year).

- Open your internet browser and go to <http://learn.intel.com>
- Either log in using an existing account or choose and 'click here' to setup a new account.
- Register your new Intel® Learning Network account by setting up a username and password; complete the registration and profile requirements. Please use your company email address as part of the registration process.
- Contact your local Intel representative for training on how to access Manufacturing Advantage Services (MAS) collaterals (such as this document) on Intel® Learning Network. By default, you may not be able to see all MAS collaterals until access is provided by your Intel representative.

7.3 How CNDA Customers Access Documents from the Resource & Design Center (RDC)

The screenshot shows the Intel RDC homepage. At the top, there's a navigation bar with the Intel logo, followed by links for PRODUCTS, SUPPORT, SOLUTIONS, DEVELOPERS (which is underlined), and PARTNERS. To the right of the links are icons for user profile, USA (ENGLISH), and a search bar labeled "Search Intel.com". Below the navigation is a large blue header section with the title "Resource & Design Center" and the subtitle "Technical Resources for Designers, Engineers, and Developers". A welcome message "Welcome back. Let us know if you need any help." is displayed. The main content area is titled "Technical Library" and contains a sub-section "Find the technical documentation, software, tools, and support you need to design and build with Intel® products.". On the left, there's a sidebar with "Most Popular" links: "Search technical content →", "New and updated content →", "Product roadmaps →", "View all products →", and "How to use the RDC →". The main content area lists categories with arrows: "Processors, Boards, and Systems →", "Components →", "Software and Solutions →", "Networking and I/O →", "Memory and storage →", "Wireless and modems →", "Cameras and sensors →", "Technologies and topics →", "Software and services →", "Software development platforms →", "Solutions →", and "Intel platform enablement tools →".

- The Resource & Design Center is an external secure portal that provides Intel customers with customized access to confidential Intel information and applications.
- To access documents in the Resource & Design Center, please contact your Intel Field Representative.
- Visit <http://rdc.intel.com>

7.4 How CNDAs Access Software from Intel® Validation Internet Portal (VIP)

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- Access the Intel® Validation Internet Portal (VIP) to find product documentation and software releases/updates available for Intel platforms. Use a keyword, document number, product or code name to find the software kits or drivers you need.

