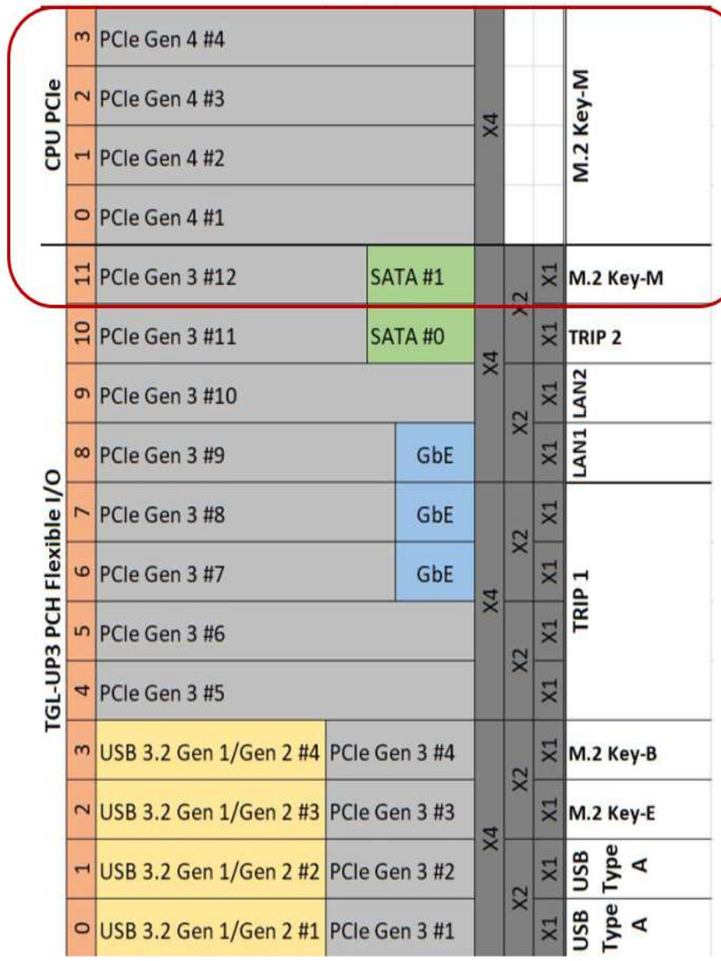
OPTION 1: TRIP1 is PCIe x4, TRIP2: PCIe x1 or SATA
OPTION 2: TRIP1 is 2x(PCIe x1), TRIP2: only SATA



SSD (NVMe Gen 4)

USB 2 Port6

PCIE12

USB 2 Port7

PCIE11 — Could be (PCIe3 x1) or (SATA#0) — Indication from M.2 to CPU: SATAXPCIE0

USB 2 Port8

PCIE10 — I210 (Symbol 9 OF 21)

PCIE9 — I219 (Only Phy, Mac Inside PCH)

USB 2 Port5

WWAN — PCIE4

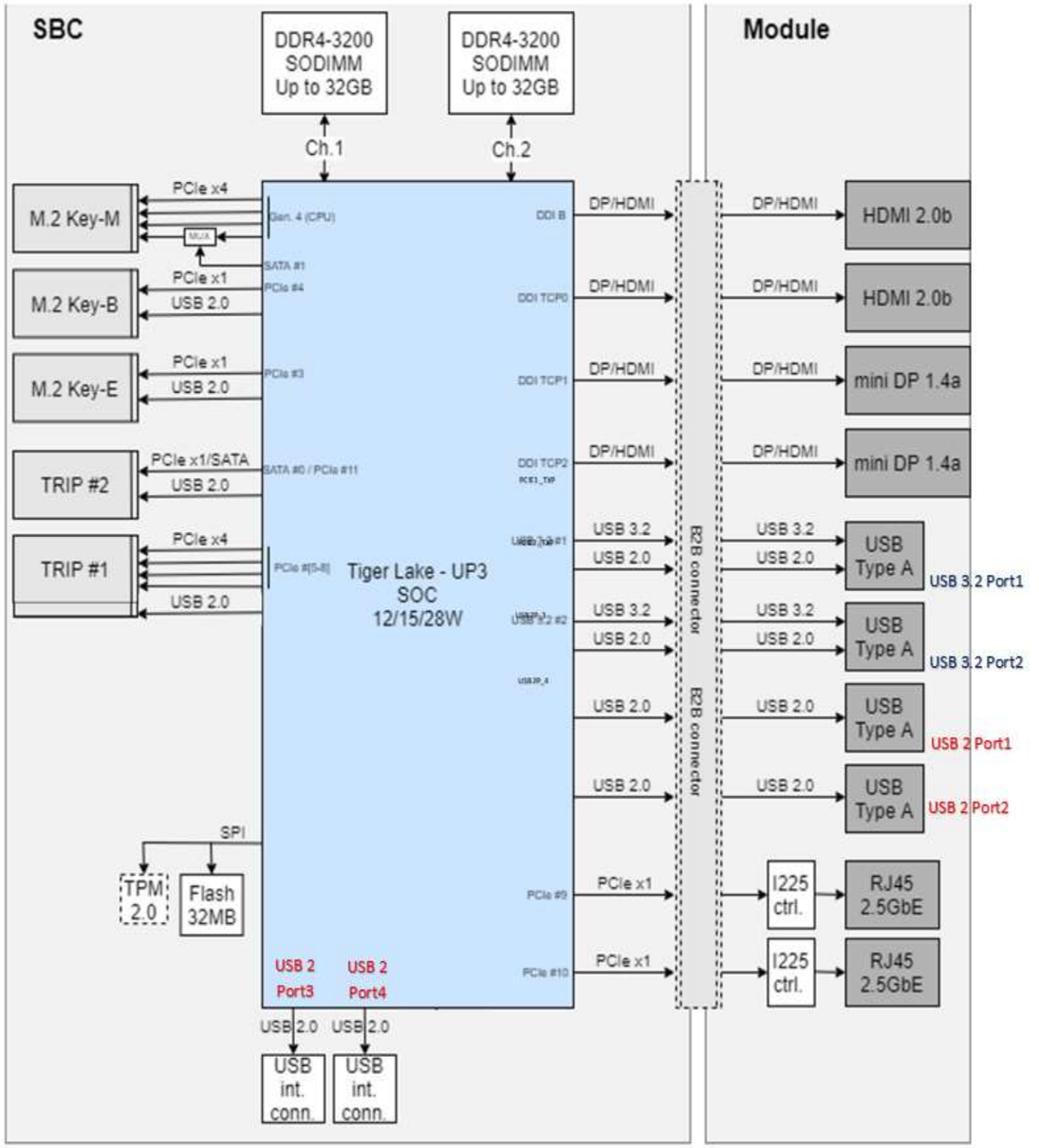
WiFi/BT — PCIE3

USB 3.2 Gen 2 (10 Gb/s) PORT 1USB 3.2 Gen 2 (10 Gb/s) PORT 1 - B2B

USB 3.2 Gen 2 (10 Gb/s) PORT 1USB 3.2 Gen 2 (10 Gb/s) PORT 2 - B2B

TRIP 1 & 2:

FT.CA-LAN4
FT.C-LAN2
FT.EC-USB2V4
FT.ED-USB3PCIV4
FT.F-M2NVME
FT.HA-SER1
FT.H-SER4
FT.I-M2B
FT.J-M2E
FT.L-PCIEmini
FT.M-TBT2
FT.N-PCIEx16
FT.Q-CAN
FT.S-GPIO
FT.T-SATA1
FT.U-POE2
FT.W-OPLN2



Tiger Lake UP3 Platform

Tiger Lake UP3 Key Feature Summary

Feature	Description
Thermal (SoC)	UP3 4+2: 15W
SoC	TGL UP3 CPU (4+2) PCH – LP
CPU IO	PCIe Gen4, 4x Type-C (TBT, USB 4.0, DP), DDR4,LPDDR4x, LPDDR5, CSI, DSi, DDI, eDP
PCH-LP	12 lanes HSIO, USB2, USB 3.2, eSPI, SPI, LPSS, I2C, SMBus
Power Delivery	CPU FIVR/PCH FIVR w/discrete VR ROP USB-C PD Controller
Memory	DDR4 - Max 64GB @ 3200MT/s LPDDR4x - Max 32GB @ 4266MT/s
Storage	PCIe/SATA
Boot	SPI NOR
Discrete Graphics	Optional x4 PCIe – Hybrid Graphics support w/Hot Plug
Internal Display	eDP , MIPI DSI
External displays	4 Wired Type-C (DP/TBT) Wireless (Miracast2.0 r2) (Wi-Fi) DDI(DP, HDMI)
Wireless	Quasar CNVi w/Harrison Peak (Wi-Fi/BT) module WWAN – XMM 7560
Clocking	38.4MHz Platform Xtal
Wired COMMs	Integrated GbE w/ discrete Gbit Lan Phy

continued...

Feature	Description
Imaging	4x WF/UF 2D Camera – (13MP WF, 2MP UF, 2MP Others) Other Cameras: AutoFocus, Face Tracking, Image Biometrics
Docking/Walk-up-Port	4x Ports Max: Type-C/Type-A
Audio	3.5mm Headphone Jack, Integrated Speakers/Mic, Docking Soundwire, Intel HD Audio, I2S, USB
Sensors	Ambient Light Sensor, Gyroscope, Accelerometer, Compass, Proximity, Pressure
Misc, GPIO's	Power/Vol button/Indicator LEDs/Keyboard/Touchpad/etc

ZZ1
P/N = 188Z10030
PARSER_VERSION_1.0

PCB1
PCB, SBC-TI22, Rev 1.0

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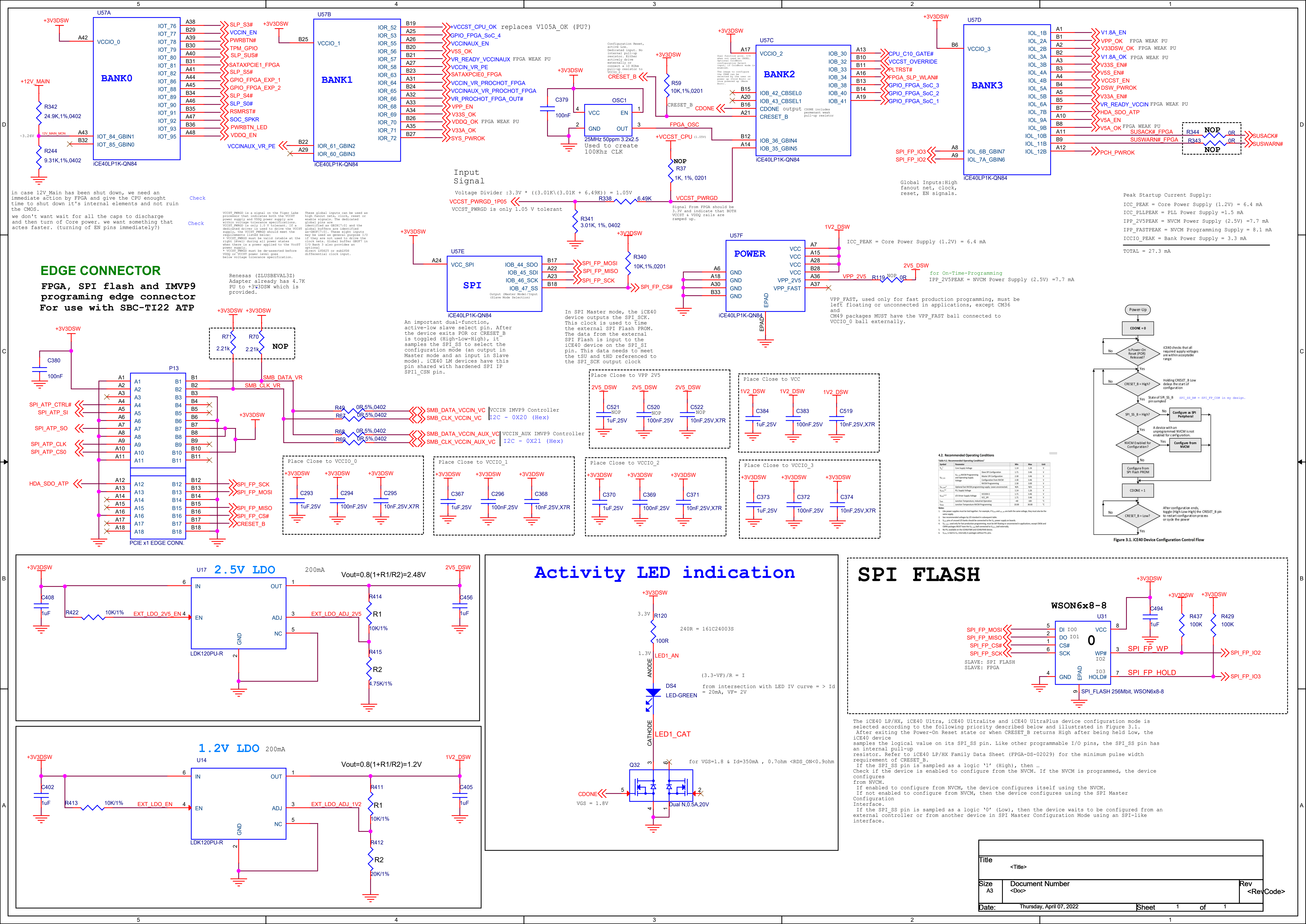
EDGE CONNECTOR
FPGA, SPI flash and IMVP9 programing edge connector For use with SBC-TI22 ATP
U57A BANK0 VCCIO_0 iCE40LP1K-QN84
U57B BANK1 VCCIO_1 iCE40LP1K-QN84
U57C BANK2 VCCIO_2 iCE40LP1K-QN84
U57D BANK3 VCCIO_3 iCE40LP1K-QN84
U57E SPI VCC_SPI IOB_44_SDO IOB_45_SDI IOB_46_SCK IOB_47_SS iCE40LP1K-QN84
U57F POWER VCC GND VPP_2V5 VPP_FAST EPAD iCE40LP1K-QN84
+VCCST_CPU_OK replaces V105A_OK (PU?)
SLP_S3# VCCIN_EN PWRBTN# TPM_GPIO SLP_SUS# SATAXPCIE1_FPGA SLP_S5# GPIO_FPGA_EXP_1 GPIO_FPGA_EXP_2 SLP_S4# SLP_S0# RSMRST# SOC_SPKR PWRBTN_LED VDDQ_EN
GPIO_FPGA_SoC_4 VCCINAUX_EN V5S_OK VR_READY_VCCINAUX FPGA WEAK PU VCCIN_VR_PE SATAXPCIE0_FPGA VCCIN_VR_PROCHOT_FPGA VCCINAUX_VR_PROCHOT_FPGA VR_PROCHOT_FPGA_OUT# VPP_EN V33S_OK VDDQ_OK FPGA WEAK PU V33A_OK SYS_PWROK VCCINAUX_VR_PE
CPU_C10_GATE# VCCST_OVERRIDE PLTRST# FPGA_SLP_WLAN# GPIO_FPGA_SoC_3 GPIO_FPGA_SoC_2 GPIO_FPGA_SoC_1 CRESET_B CDONE
V1.8A_EN VPP_OK FPGA WEAK PU V33DSW_OK FPGA WEAK PU V1.8A_OK FPGA WEAK PU V33S_EN# V5S_EN# VCCST_EN DSW_PWROK V33A_EN# VR_READY_VCCIN FPGA WEAK PU HDA_SDO_ATP V5A_EN V5A_OK FPGA WEAK PU SUSACK#_FPGA SUSWARN#_FPGA SUSACK# SUSWARN# PCH_PWROK R344 R343 0R NOP
OSC1 25MHz 50ppm 3.2x2.5 Used to create 100Khz CLK C379 100nF
R59 10K,1%,0201 R37 1K, 1%, 0201 NOP FPGA_OSC +VCCST_CPU
Input Signal
Voltage Divider :3.3V * ((3.01K\(3.01K + 6.49K)) = 1.05V
VCCST_PWRGD_1P05 VCCST_PWRGD is only 1.05 V tolerant R338 6.49K R341 3.01K, 1%, 0402 VCCST_PWRGD
Signal From FPGA should be 3.3V and indicate that BOTH VCCST & VDDQ rails are ramped up.
Global Inputs:High fanout net, clock, reset, EN signals.
R342 24.9K,1%,0402 R244 9.31K,1%,0402 +12V_MAIN
in case 12V_Main has been shut down, we need an immediate action by FPGA and give the CPU enought time to shut down it's internal elements and not ruin the CMOS.
we don't want wait for all the caps to discharge and then turn of Core power. we want something that actes faster. (turning of EN pins immediately?)
Check
Renesas (ZLUSBEVAL3Z) Adapter already has 4.7K PU to +3V3DSW which is provided.
An important dual-function, active-low slave select pin. After the device exits POR or CRESET_B is toggled (High-Low-High), it samples the SPI_SS to select the configuration mode (an output in Master mode and an input in Slave mode). iCE40 LM devices have this pin shared with hardened SPI IP SPI1_CSN pin.
In SPI Master mode, the iCE40 device outputs the SPI_SCK. This clock is used to time the external SPI Flash PROM. The data from the external SPI Flash is input to the iCE40 device on the SPI_SI pin. This data needs to meet the tSU and tHD requirement to the SPI_SCK output clock
SPI_FP_MOSI SPI_FP_MISO SPI_FP_SCK SPI_FP_CS# R340 10K,1%,0201
ICC_PEAK = Core Power Supply (1.2V) = 6.4 mA
for One-Time-Programming IPP_2V5PEAK = NVCM Power Supply (2.5V) =7.7 mA
R119 0R NOP VPP_2V5
VPP_FAST, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the VPP_FAST ball connected to VCCIO_0 ball externally.
Peak Startup Current Supply:
ICC_PEAK = Core Power Supply (1.2V) = 6.4 mA
ICC_PLLPEAK = PLL Power Supply =1.5 mA
IPP_2V5PEAK = NVCM Power Supply (2.5V) =7.7 mA
IPP_FASTPEAK = NVCM Programming Supply = 8.1 mA
ICCIO_PEAK = Bank Power Supply = 3.3 mA
TOTAL = 27.3 mA
P13 PCIE x1 EDGE CONN. C380 100nF R71 R70 2.21k NOP
SMB_DATA_VR SMB_CLK_VR SPI_ATP_CTRL# SPI_ATP_SI SPI_ATP_SO SPI_ATP_CLK SPI_ATP_CS0 HDA_SDO_ATP CRESET_B
R49 R67 R68 R69 0R,5%,0402
SMB_DATA_VCCIN_VC SMB_CLK_VCCIN_VC VCCIN IMVP9 Controller I2C - 0X20 (Hex)
SMB_DATA_VCCIN_AUX_VC SMB_CLK_VCCIN_AUX_VC VCCIN_AUX IMVP9 Controller I2C - 0X21 (Hex)
Place Close to VPP 2V5 C521 C520 C522 NOP 1uF,25V 100nF,25V 10nF,25V,X7R
Place Close to VCC C384 C383 C519
Place Close to VCCIO_0 C293 C294 C295
Place Close to VCCIO_1 C367 C296 C368
Place Close to VCCIO_2 C370 C369 C371
Place Close to VCCIO_3 C373 C372 C374
Figure 3.1. iCE40 Device Configuration Control Flow
2.5V LDO 200mA U17 LDK120PU-R Vout=0.8(1+R1/R2)=2.48V R422 10K/1% EXT_LDO_2V5_EN EXT_LDO_ADJ_2V5 R414 R1 10K/1% R415 R2 4.75K/1% C408 C456 1uF 2V5_DSW
1.2V LDO 200mA U14 LDK120PU-R Vout=0.8(1+R1/R2)=1.2V R413 10K/1% EXT_LDO_EN EXT_LDO_ADJ_1V2 R411 R1 10K/1% R412 R2 20K/1% C402 C405 1uF 1V2_DSW
Activity LED indication
R120 100R 240R = 161C24003S LED1_AN DS4 LED-GREEN LED1_CAT
(3.3-VF)/R = I
from intersection with LED IV curve = > Id = 20mA, VF= 2V
Q32 Dual N,0.5A,20V for VGS=1.8 & Id=350mA , 0.7ohm <RDS_ON<0.9ohm CDONE VGS = 1.8V
SPI FLASH
WSON6x8-8 U31 SPI_FP_MOSI SPI_FP_MISO SPI_FP_CS# SPI_FP_SCK SLAVE: SPI FLASH SLAVE: FPGA SPI_FP_WP SPI_FP_HOLD SPI_FP_IO2 SPI_FP_IO3 C494 1uF R437 100K R429 100K SPI_FLASH 256Mbit, WSON6x8-8
The iCE40 LP/HX, iCE40 Ultra, iCE40 UltraLite and iCE40 UltraPlus device configuration mode is selected according to the following priority described below and illustrated in Figure 3.1. After exiting the Power-On Reset state or when CRESET_B returns High after being held Low, the iCE40 device samples the logical value on its SPI_SS pin. Like other programmable I/O pins, the SPI_SS pin has an internal pull-up resistor. Refer to iCE40 LP/HX Family Data Sheet (FPGA-DS-02029) for the minimum pulse width requirement of CRESET_B.
If the SPI_SS pin is sampled as a logic '1' (High), then … Check if the device is enabled to configure from the NVCM. If the NVCM is programmed, the device configures from NVCM.
If enabled to configure from NVCM, the device configures itself using the NVCM.
If not enabled to configure from NVCM, then the device configures using the SPI Master Configuration Interface.
If the SPI_SS pin is sampled as a logic '0' (Low), then the device waits to be configured from an external controller or from another device in SPI Master Configuration Mode using an SPI-like interface.
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TIGER LAKE PCH:

The PCH provides extensive I/O support. The functions and capabilities include:
- ACPI Power Management Logic Support, Revision 5.0a
- PCI Express Base Specification Revision 3.0
- Integrated Serial ATA Host controller 3.2, supports data transfer rates of up to 6 Gb/s on all ports
- USB 3.2 Gen 2x1 (10 Gb/s) eXtensible Host Controller (xHCI)
- USB 3.2 Gen 1x1 (5 Gb/s) Dual Role (eXtensible Device Controller - xDCI) Capability
- Serial Peripheral Interface (SPI)
- Enhanced Serial Peripheral Interface (eSPI)
- Flexible I/O—Allows some high speed I/O signals to be configured as PCIe or USB 3.2
- General Purpose Input Output (GPIO)
- Interrupt controller
- Timer functions
- System Management Bus (SMBus) Specification, Version 2.0
- Integrated Clock Controller (ICC)/Real Time Clock Controller (RTCC)
- Intel® High Definition Audio and Intel® Smart Sound Technology (Intel® SST), supporting I2S, MIPI* SoundWire*, and DMIC
- Intel® Serial I/O UART Host controllers
- Intel® Serial I/O I2C Host controllers
- Integrated 10/100/1000 Gigabit Ethernet MAC
- Integrated Sensor Hub (ISH)
- Supports Intel® Rapid Storage Technology (Intel® RST)
- Supports Intel® Active Management Technology (Intel® AMT) (AMT)
- Supports Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Supports Intel® Trusted Execution Technology (Intel® TXT)
- JTAG Boundary Scan support
- Intel® Trace Hub (Intel® TH) and Direct Connect Interface (DCI) for debug
- Supports Intel® CSME (CSME)
- Supports Integrated connectivity (CNVi)

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MCP -DP\HDMI

TGL-U MCP (1 OF 21) - DISPLAY & TYPE-C (TBT/DISPLAY)

Name	Type	Description
GPP_E14 / **DDSP_HPDA** / DISP_MISCA	I	**Display Port A:** HPD Hot-Plug Detect
GPP_A18 / **DDSP_HPDB** / DISP_MISCB / I2S4_RXD	I	**Display Port B:** HPD Hot-Plug Detect
GPP_A19 / **DDSP_HPD1** / DISP_MISC1 / I2S5_SCLK	I	**TCP Port 1:** HPD Hot-Plug Detect 0
GPP_A20 / **DDSP_HPD2** / DISP_MISC2 / I2S5_SFRM	I	**TCP Port 2:** HPD Hot-Plug Detect 1
GPP_A14 / USB_OC1# / **DDSP_HPD3** / I2S3_RXD / DISP_MISC3 / DMIC_CLK_B1	I	**TCP Port 3:** HPD Hot-Plug Detect 2
GPP_A15 / USB_OC2# / **DDSP_HPD4** / DISP_MISC4 / I2S4_SCLK	I	**TCP Port 4:** HPD Hot-Plug Detect 3

5.3 Display Interfaces

Table 33. DDI Ports Availability

SKU	UP4 Processor Line	UP3 Processor Line
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	eDP*/DP*/HDMI*/MIPI_1	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*
Note: HBR3 supported on TCP ports only. Each of the TCP port can support DPoC* (DisplayPort* over Type-C)		

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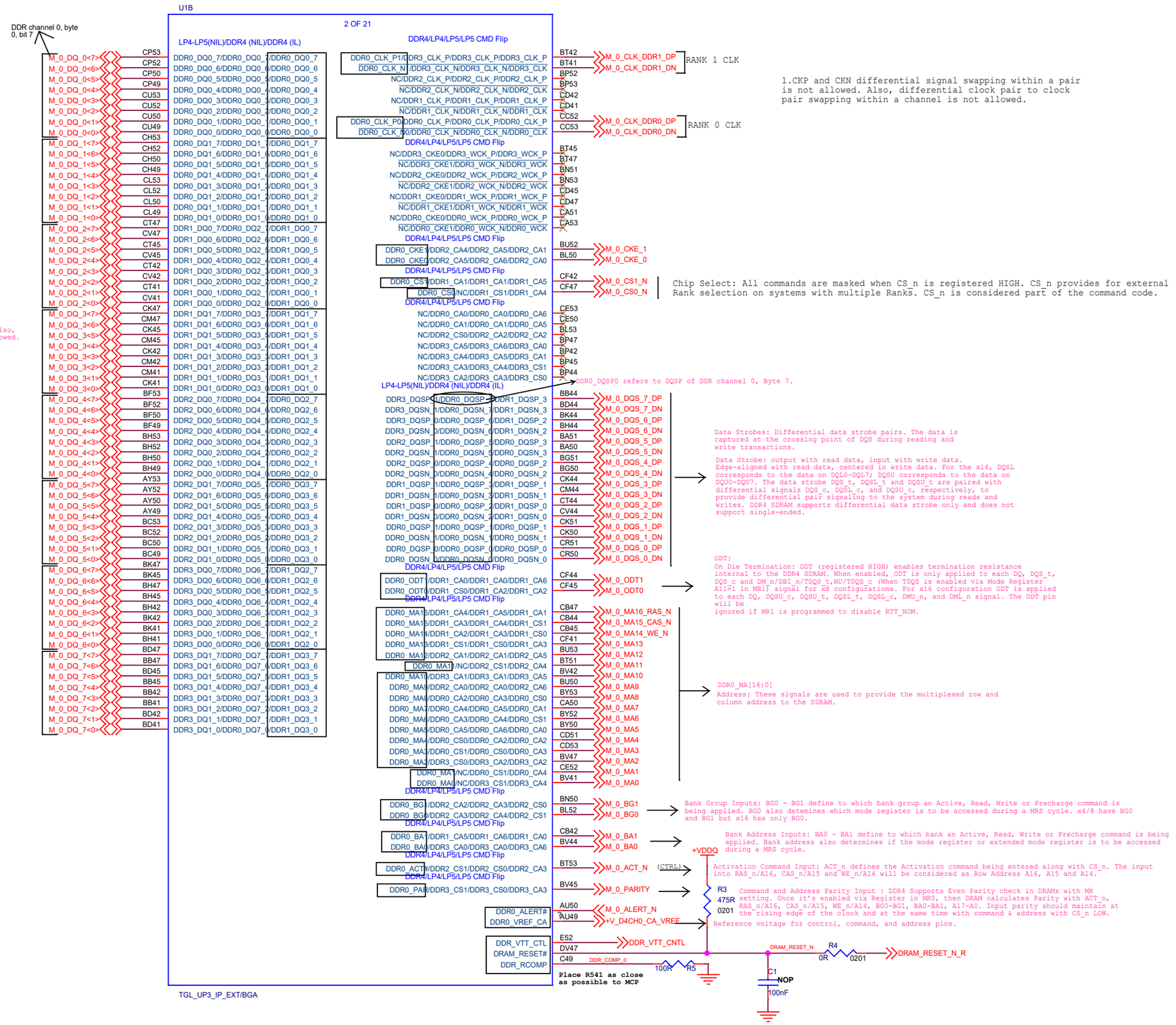
MEMORY CHANNEL A



1.CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.
2.DQ Bit swapping is allowed within the same byte
3.Byte Swapping is allowed within the same channel
4.DQSP and DQSN differential signal swapping within a pair is not allowed.

NOTES:

Each lane of 8bits (Byte) of Data has it's own Data Strobe

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS and register
BA0, BA1	Regsiter bank select input	SDA	I^2C serial data line for SPD/TS and register
BG0, BG1	Regsiter bank group select input	SA0-SA2	I^2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power
WE_n[4]	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12V	Optional Power Supply on socket but not used on RDIMM
CKE0, CEK1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of dif-ferential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.

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MEMORY CHANNEL B

AL53: DDR4_DQ0[7]/DDR1_DQ0[7]
DDR channel 4(1), Byte 0, Bit 7

U1C
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		LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_0<7>	AL53	DDR4_DQ0_7/DDR1_DQ0_7/DDR0_DQ4_7	DDR1_CLK_P1/DDR7_CLK_P/DDR7_CLK_P/DDR7_CLK_P	R41	M_1_CLK_DDR1_DP
M_1_DQ_0<6>	AL52	DDR4_DQ0_6/DDR1_DQ0_6/DDR0_DQ4_6	DDR1_CLK_N1/DDR7_CLK_N/DDR7_CLK_N/DDR7_CLK	R42	M_1_CLK_DDR1_DN
M_1_DQ_0<5>	AL50	DDR4_DQ0_5/DDR1_DQ0_5/DDR0_DQ4_5	NC/DDR6_CLK_P/DDR6_CLK_P/DDR6_CLK_P	M52	
M_1_DQ_0<4>	AL49	DDR4_DQ0_4/DDR1_DQ0_4/DDR0_DQ4_4	NC/DDR6_CLK_N/DDR6_CLK_N/DDR6_CLK	M53	
M_1_DQ_0<3>	AP53	DDR4_DQ0_3/DDR1_DQ0_3/DDR0_DQ4_3	NC/DDR5_CLK_P/DDR5_CLK_P/DDR5_CLK_P	AC42	
M_1_DQ_0<2>	AP52	DDR4_DQ0_2/DDR1_DQ0_2/DDR0_DQ4_2	NC/DDR5_CLK_N/DDR5_CLK_N/DDR5_CLK	AC41	
M_1_DQ_0<1>	AP50	DDR4_DQ0_1/DDR1_DQ0_1/DDR0_DQ4_1	DDR1_CLK_P0/DDR4_CLK_P/DDR4_CLKP/DDR4_CLK_P	Y52	M_1_CLK_DDR0_DP
M_1_DQ_0<0>	AP49	DDR4_DQ0_0/DDR1_DQ0_0/DDR0_DQ4_0	DDR1_CLK_N0/DDR4_CLK_N/DDR4_CLK_N/DDR4_CLK	Y53	M_1_CLK_DDR0_DN
M_1_DQ_1<7>	AF53	DDR4_DQ1_7/DDR1_DQ1_7/DDR0_DQ5_7	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_1<6>	AF52	DDR4_DQ1_6/DDR1_DQ1_6/DDR0_DQ5_6	NC/DDR7_CKE0/DDR7_WCK_P/DDR7_WCK_P	R47	
M_1_DQ_1<5>	AF50	DDR4_DQ1_5/DDR1_DQ1_5/DDR0_DQ5_5	NC/DDR7_CKE1/DDR7_WCK_N/DDR7_WCK	R45	
M_1_DQ_1<4>	AF49	DDR4_DQ1_4/DDR1_DQ1_4/DDR0_DQ5_4	NC/DDR6_CKE0/DDR6_WCK_P/DDR6_WCK_P	K51	
M_1_DQ_1<3>	AH53	DDR4_DQ1_3/DDR1_DQ1_3/DDR0_DQ5_3	NC/DDR6_CKE1/DDR6_WCK_N/DDR6_WCK	K53	
M_1_DQ_1<2>	AH52	DDR4_DQ1_2/DDR1_DQ1_2/DDR0_DQ5_2	NC/DDR5_CKE0/DDR5_WCK_P/DDR5_WCK_P	AC47	
M_1_DQ_1<1>	AH50	DDR4_DQ1_1/DDR1_DQ1_1/DDR0_DQ5_1	NC/DDR5_CKE1/DDR5_WCK_N/DDR5_WCK	AC45	
M_1_DQ_1<0>	AH49	DDR4_DQ1_0/DDR1_DQ1_0/DDR0_DQ5_0	NC/DDR4_CKE0/DDR4_WCK_P/DDR4_WCK_P	W51	
M_1_DQ_2<7>	AR41	DDR5_DQ0_7/DDR1_DQ2_7/DDR1_DQ4_7	NC/DDR4_CKE1/DDR4_WCK_N/DDR4_WCK	W53	
M_1_DQ_2<6>	AV42	DDR5_DQ0_6/DDR1_DQ2_6/DDR1_DQ4_6	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_2<5>	AR42	DDR5_DQ0_5/DDR1_DQ2_5/DDR1_DQ4_5	DDR1_CKE1/DDR6_CA4/DDR6_CA5/DDR6_CA1	P52	M_1_CKE_1
M_1_DQ_2<4>	AV41	DDR5_DQ0_4/DDR1_DQ2_4/DDR1_DQ4_4	DDR1_CKE0/DDR6_CA5/DDR6_CA6/DDR6_CA0	J50	M_1_CKE_0
M_1_DQ_2<3>	AR45	DDR5_DQ0_3/DDR1_DQ2_3/DDR1_DQ4_3	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_2<2>	AV45	DDR5_DQ0_2/DDR1_DQ2_2/DDR1_DQ4_2	DDR1_CS1/DDR5_CA1/DDR5_CA1/DDR5_CA5	AE42	M_1_CS1_N
M_1_DQ_2<1>	AR47	DDR5_DQ0_1/DDR1_DQ2_1/DDR1_DQ4_1	DDR1_CS0/NC/DDR5_CS1/DDR5_CA4	AE47	M_1_CS0_N
M_1_DQ_2<0>	AV47	DDR5_DQ0_0/DDR1_DQ2_0/DDR1_DQ4_0	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_3<7>	AJ41	DDR5_DQ1_7/DDR1_DQ3_7/DDR1_DQ5_7	NC/DDR7_CA5/DDR7_CA6/DDR7_CA0	N42	
M_1_DQ_3<6>	AJ42	DDR5_DQ1_6/DDR1_DQ3_6/DDR1_DQ5_6	NC/DDR7_CA4/DDR7_CA5/DDR7_CA1	N45	
M_1_DQ_3<5>	AL41	DDR5_DQ1_5/DDR1_DQ3_5/DDR1_DQ5_5	NC/DDR7_CA3/DDR7_CA4/DDR7_CS1	N44	
M_1_DQ_3<4>	AL42	DDR5_DQ1_4/DDR1_DQ3_4/DDR1_DQ5_4	NC/DDR7_CA2/DDR7_CA3/DDR7_CS0	N47	
M_1_DQ_3<3>	AJ45	DDR5_DQ1_3/DDR1_DQ3_3/DDR1_DQ5_3	NC/DDR6_CS0/DDR6_CA2/DDR6_CA2	J53	
M_1_DQ_3<2>	AJ47	DDR5_DQ1_2/DDR1_DQ3_2/DDR1_DQ5_2	NC/DDR4_CA1/DDR4_CA1/DDR4_CA5	AC50	
M_1_DQ_3<1>	AL45	DDR5_DQ1_1/DDR1_DQ3_1/DDR1_DQ5_1	NC/DDR4_CA0/DDR4_CA0/DDR4_CA6	AC53	
M_1_DQ_3<0>	AL47	DDR5_DQ1_0/DDR1_DQ3_0/DDR1_DQ5_0	LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)		
M_1_DQ_4<7>	A43	DDR6_DQ0_7/DDR1_DQ4_7/DDR0_DQ6_7	DDR7_DQSP_1/DDR1_DQSP_7/DDR1_DQSP_7	K36	M_1_DQS_7_DP
M_1_DQ_4<6>	B43	DDR6_DQ0_6/DDR1_DQ4_6/DDR0_DQ6_6	DDR7_DQSN_1/DDR1_DQSN_7/DDR1_DQSN_7	K38	M_1_DQS_7_DN
M_1_DQ_4<5>	D43	DDR6_DQ0_5/DDR1_DQ4_5/DDR0_DQ6_5	DDR7_DQSP_0/DDR1_DQSP_6/DDR1_DQSP_6	G44	M_1_DQS_6_DP
M_1_DQ_4<4>	E44	DDR6_DQ0_4/DDR1_DQ4_4/DDR0_DQ6_4	DDR7_DQSN_0/DDR1_DQSN_6/DDR1_DQSN_6	J44	M_1_DQS_6_DN
M_1_DQ_4<3>	A46	DDR6_DQ0_3/DDR1_DQ4_3/DDR0_DQ6_3	DDR6_DQSP_1/DDR1_DQSP_5/DDR0_DQSP_7	D39	M_1_DQS_5_DP
M_1_DQ_4<2>	B46	DDR6_DQ0_2/DDR1_DQ4_2/DDR0_DQ6_2	DDR6_DQSN_1/DDR1_DQSN_5/DDR0_DQSN_7	C39	M_1_DQS_5_DN
M_1_DQ_4<1>	D46	DDR6_DQ0_1/DDR1_DQ4_1/DDR0_DQ6_1	DDR6_DQSP_0/DDR1_DQSP_4/DDR0_DQSP_6	C45	M_1_DQS_4_DP
M_1_DQ_4<0>	E47	DDR6_DQ0_0/DDR1_DQ4_0/DDR0_DQ6_0	DDR6_DQSN_0/DDR1_DQSN_4/DDR0_DQSN_6	D45	M_1_DQS_4_DN
M_1_DQ_5<7>	E38	DDR6_DQ1_7/DDR1_DQ5_7/DDR0_DQ7_7	DDR5_DQSP_1/DDR1_DQSP_3/DDR1_DQSP_5	AJ44	M_1_DQS_3_DP
M_1_DQ_5<6>	D38	DDR6_DQ1_6/DDR1_DQ5_6/DDR0_DQ7_6	DDR5_DQSN_1/DDR1_DQSN_3/DDR1_DQSN_5	AL44	M_1_DQS_3_DN
M_1_DQ_5<5>	B38	DDR6_DQ1_5/DDR1_DQ5_5/DDR0_DQ7_5	DDR5_DQSP_0/DDR1_DQSP_2/DDR1_DQSP_4	AV44	M_1_DQS_2_DP
M_1_DQ_5<4>	A38	DDR6_DQ1_4/DDR1_DQ5_4/DDR0_DQ7_4	DDR5_DQSN_0/DDR1_DQSN_2/DDR1_DQSN_4	AR44	M_1_DQS_2_DN
M_1_DQ_5<3>	E41	DDR6_DQ1_3/DDR1_DQ5_3/DDR0_DQ7_3	DDR4_DQSP_1/DDR1_DQSP_1/DDR0_DQSP_5	AG51	M_1_DQS_1_DP
M_1_DQ_5<2>	D40	DDR6_DQ1_2/DDR1_DQ5_2/DDR0_DQ7_2	DDR4_DQSN_1/DDR1_DQSN_1/DDR0_DQSN_5	AG50	M_1_DQS_1_DN
M_1_DQ_5<1>	B40	DDR6_DQ1_1/DDR1_DQ5_1/DDR0_DQ7_1	DDR4_DQSP_0/DDR1_DQSP_0/DDR0_DQSP_4	AN51	M_1_DQS_0_DP
M_1_DQ_5<0>	A40	DDR6_DQ1_0/DDR1_DQ5_0/DDR0_DQ7_0	DDR4_DQSN_0/DDR1_DQSN_0/DDR0_DQSN_4	AN50	M_1_DQS_0_DN
M_1_DQ_6<7>	G42	DDR7_DQ0_7/DDR1_DQ6_7/DDR1_DQ6_7	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_6<6>	G41	DDR7_DQ0_6/DDR1_DQ6_6/DDR1_DQ6_6	DDR1_ODT1/DDR5_CA0/DDR5_CA0/DDR5_CA6	AE44	M_1_ODT1
M_1_DQ_6<5>	J41	DDR7_DQ0_5/DDR1_DQ6_5/DDR1_DQ6_5	DDR1_ODT0/DDR5_CS0/DDR5_CA2/DDR5_CA2	AE45	M_1_ODT0
M_1_DQ_6<4>	J42	DDR7_DQ0_4/DDR1_DQ6_4/DDR1_DQ6_4	DDR4/LP4/LP5/LP5 CMD Flip		
M_1_DQ_6<3>	G45	DDR7_DQ0_3/DDR1_DQ6_3/DDR1_DQ6_3	DDR1_MA16/DDR5_CA4/DDR5_CA5/DDR5_CA1	AA47	M_1_MA16_RAS_N
M_1_DQ_6<2>	J45	DDR7_DQ0_2/DDR1_DQ6_2/DDR1_DQ6_2	DDR1_MA15/DDR5_CA3/DDR5_CA4/DDR5_CS1	AA44	M_1_MA15_CAS_N
M_1_DQ_6<1>	G47	DDR7_DQ0_1/DDR1_DQ6_1/DDR1_DQ6_1	DDR1_MA14/DDR5_CA2/DDR5_CA3/DDR5_CS0	AA45	M_1_MA14_WE_N
M_1_DQ_6<0>	J47	DDR7_DQ0_0/DDR1_DQ6_0/DDR1_DQ6_0	DDR1_MA13/DDR5_CS1/DDR5_CS0/DDR5_CA3	AE41	M_1_MA13
M_1_DQ_7<7>	G38	DDR7_DQ1_7/DDR1_DQ7_7/DDR1_DQ7_7	DDR1_MA12/DDR6_CA1/DDR6_CA1/DDR6_CA5	P53	M_1_MA12
M_1_DQ_7<6>	G36	DDR7_DQ1_6/DDR1_DQ7_6/DDR1_DQ7_6	DDR1_MA11/NC/DDR6_CS1/DDR6_CA4	N51	M_1_MA11
M_1_DQ_7<5>	H36	DDR7_DQ1_5/DDR1_DQ7_5/DDR1_DQ7_5	DDR1_MA10/DDR7_CA1/DDR7_CA1/DDR7_CA5	U42	M_1_MA10
M_1_DQ_7<4>	H38	DDR7_DQ1_4/DDR1_DQ7_4/DDR1_DQ7_4	DDR1_MA9/DDR6_CA0/DDR6_CA0/DDR6_CA6	P50	M_1_MA9
M_1_DQ_7<3>	N36	DDR7_DQ1_3/DDR1_DQ7_3/DDR1_DQ7_3	DDR1_MA8/DDR4_CA2/DDR4_CA3/DDR4_CS0	U53	M_1_MA8
M_1_DQ_7<2>	L36	DDR7_DQ1_2/DDR1_DQ7_2/DDR1_DQ7_2	DDR1_MA7/DDR4_CA4/DDR4_CA5/DDR4_CA1	W50	M_1_MA7
M_1_DQ_7<1>	L38	DDR7_DQ1_1/DDR1_DQ7_1/DDR1_DQ7_1	DDR1_MA6/DDR4_CA3/DDR4_CA4/DDR4_CS1	U52	M_1_MA6
M_1_DQ_7<0>	N38	DDR7_DQ1_0/DDR1_DQ7_0/DDR1_DQ7_0	DDR1_MA5/DDR4_CA5/DDR4_CA6/DDR4_CA0	U50	M_1_MA5
			DDR1_MA4/DDR4_CS0/DDR4_CA2/DDR4_CA2	AA51	M_1_MA4
			DDR1_MA3/DDR4_CS1/DDR4_CS0/DDR4_CA3	AA53	M_1_MA3
			DDR1_MA2/DDR7_CS0/DDR7_CA2/DDR7_CA2	U47	M_1_MA2
			DDR1_MA1/NC/DDR4_CS1/DDR4_CA4	AC52	M_1_MA1
			DDR1_MA0/NC/DDR7_CS1/DDR7_CA4	U41	M_1_MA0
			DDR4/LP4/LP5/LP5 CMD Flip		
			DDR1_BG1/DDR6_CA2/DDR6_CA3/DDR6_CS0	K50	M_1_BG1
			DDR1_BG0/DDR6_CA3/DDR6_CA4/DDR6_CS1	J52	M_1_BG0
			DDR4/LP4/LP5/LP5 CMD Flip		
			DDR1_BA1/DDR5_CA5/DDR5_CA6/DDR5_CA0	AA42	M_1_BA1
			DDR1_BA0/DDR7_CA0/DDR7_CA0/DDR7_CA6	U44	M_1_BA0
			DDR1_ACT#/DDR6_CS1/DDR6_CS0/DDR6_CA3	N53	M_1_ACT_N
			DDR1_PAR/DDR7_CS1/DDR7_CS0/DDR7_CA3	U45	M_1_PARITY
			DDR1_ALERT#	AU53	M_1_ALERT_N
			DDR1_VREF_CA	AU52	+V_D4CH1_CA_VREF

TGL_UP3_IP_EXT/BGA

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CATERR#

Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The
processor will set this signal for non-
recoverable machine check errors or other
unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.

PROCHOT#

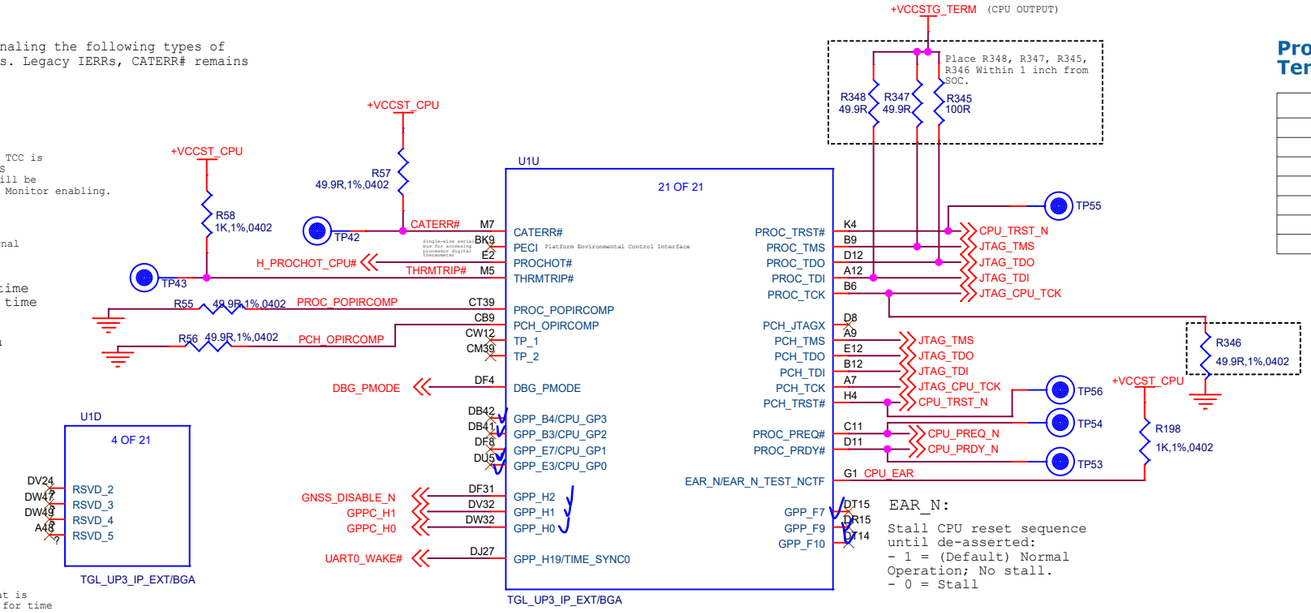
The PROCHOT# (processor hot) signal is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling. The PROCHOT# signal can be configured to the following modes:

- Input Only: PROCHOT is driven by an external device.
- Output Only: PROCHOT is driven by processor.
- Bi-Directional: Both Processor and external device can drive PROCHOT signal

Time Synchronization GPIO 0: Timed GPIO event for time synchronization for interfaces that do not support time synchronization natively.

Time Synchronization: Used for synchronization both input (latch time when pin asserted) and output (toggle pin when programmed time is hit).

TIME_SYNC:
The PCH supports two Timed GPIOs as native function (TIME_SYNC) that is muxed on GPIO pins. The intent usage of the Timed GPIO function is for time synchronization purpose.
Timed GPIO can be an input or an output.
• As an input, a GPIO input event triggers the HW to capture the PCH Always Running Timer (ART) time in the Time Capture register. The GPIO input event must be asserted for at least two crystal oscillator clocks period in order for the event to be recognized.
• As an output, a match between the ART time and the software programmed time value triggers the HW to generate a GPIO output event and capture the ART time in the Time Capture register. If periodic mode is enabled, HW generates the
periodic GPIO events based on the programmed interval. The GPIO output event is asserted by HW for at least two crystal oscillator clocks period.



EAR_N:

Stall CPU reset sequence until de-asserted:
- 1 = (Default) Normal Operation; No stall.
- 0 = Stall

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM#[3:0]	Pull Up/Pull Down	VCC_{IO_OUT}	16-60 Ω
PROC_PREQ#	Pull Up	VCC_{STG}	3 KΩ
PROC_TDI	Pull Up	VCC_{STG}	3 KΩ
PROC_TMS	Pull Up	VCC_{STG}	3 KΩ
PROC_TRST#	Pull Down	VCC_{STG}	3 KΩ
PROC_TCK	Pull Down	VCC_{STG}	3 KΩ
CFG[17:0]	Pull Up	VCC_{IO_OUT}	3 KΩ

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BPM#[3:0]	**Breakpoint and Performance Monitor Signals:** Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	UP3/UP4/H Processor Lines
PROC_PRDY#	**Probe Mode Ready:** PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	O	OD	SE	UP3/UP4/H Processor Lines
PROC_PREQ#	**Probe Mode Request:** PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TCK	**Test Clock:** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal should be driven low or allowed to float during power on Reset.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TDI	**Test Data In:** This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TDO	**Test Data Out:** This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O	OD	SE	UP3/UP4/H Processor Lines
PROC_TMS	**Test Mode Select:** A JTAG specification support signal used by debug tools.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TRST#	**Test Reset:** Resets the Test Access Port (TAP) logic. This signal should be driven low during power on Reset. Refer to the appropriate processor Debug Port Design Guide (Refer to Section 1.10, "Related Documents") for complete implementation details.	I	GTL	SE	UP3/UP4/H Processor Lines

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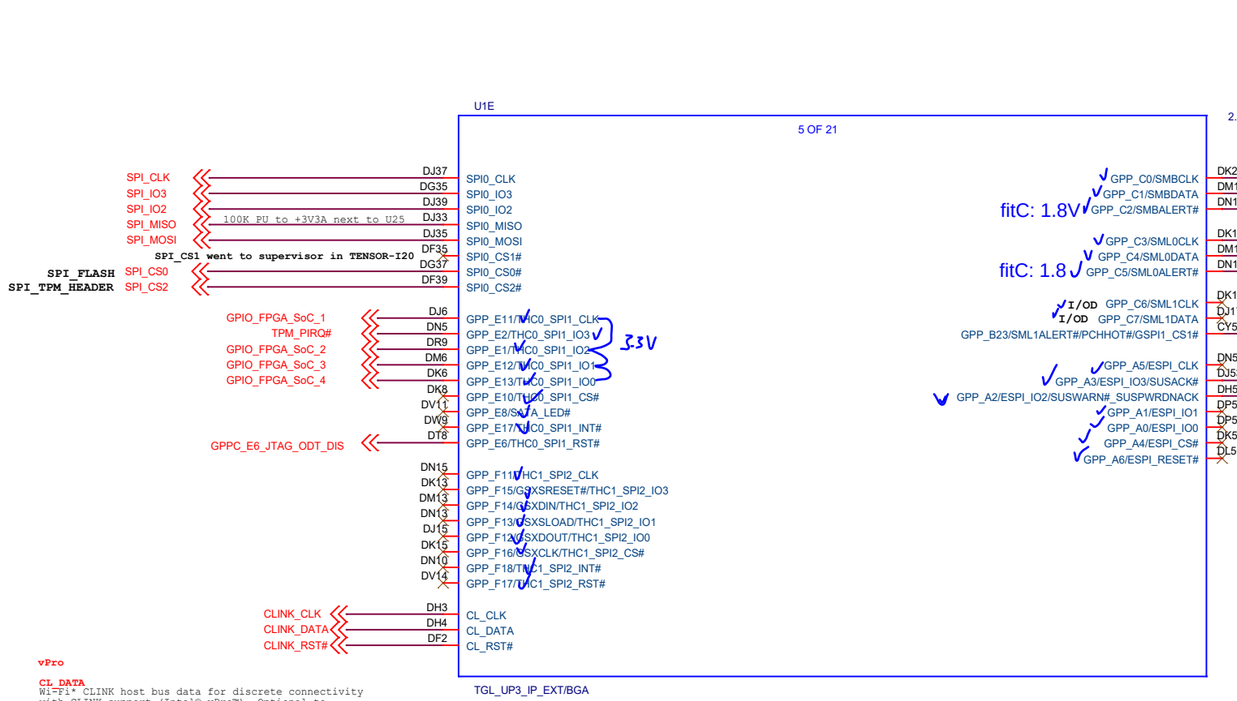


vPro

CL_DATA
Wi-Fi* CLINK host bus data for discrete connectivity with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK data pin on the Intel® vPro™ Wi-Fi* module.

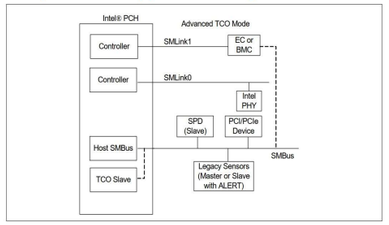
CL_CLK
Wi-Fi* CLINK host bus clock for discrete connectivity with CLINK support (Intel® vPro™). Optional to connect to a Wi-Fi* CLINK clock pin on the Intel® vPro™ Wi-Fi* module.

SML0CLK & SML0DATA
System Management Link clock signal interface to Intel® Ethernet Connection I219. Refer to System Management Interface and SMLink for details on the SML0CLK signal.
Note: The Intel® Ethernet Connection I219 connects to SML0CLK signal.

FUNCTIONALITY:
The SMLink interfaces are controlled by the Intel® CSME.
SMLink0 is mainly used for integrated LAN. When an Intel LAN PHY is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of up to 1 MHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled using a soft strap. SMLink1 can be used with an Embedded Controller (EC) or Baseboard Management Controller (BMC). Both SMLink0 and SMLink1 support up to 1 MHz.

SUSACK# & SUSWARN#:
This function is only applicable to platforms supporting Deep Sleep Wells
This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (using SLP_SUS#). The EC/ motherboard control logic must observe edges on this pin, preparing
for Primary well power loss on a falling edge and preparing for Prim
well related activity (host/Intel ME wakes and runtime events) on a
rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#.

SMBus / SMlink Connectivity (Advanced TCO Mode)



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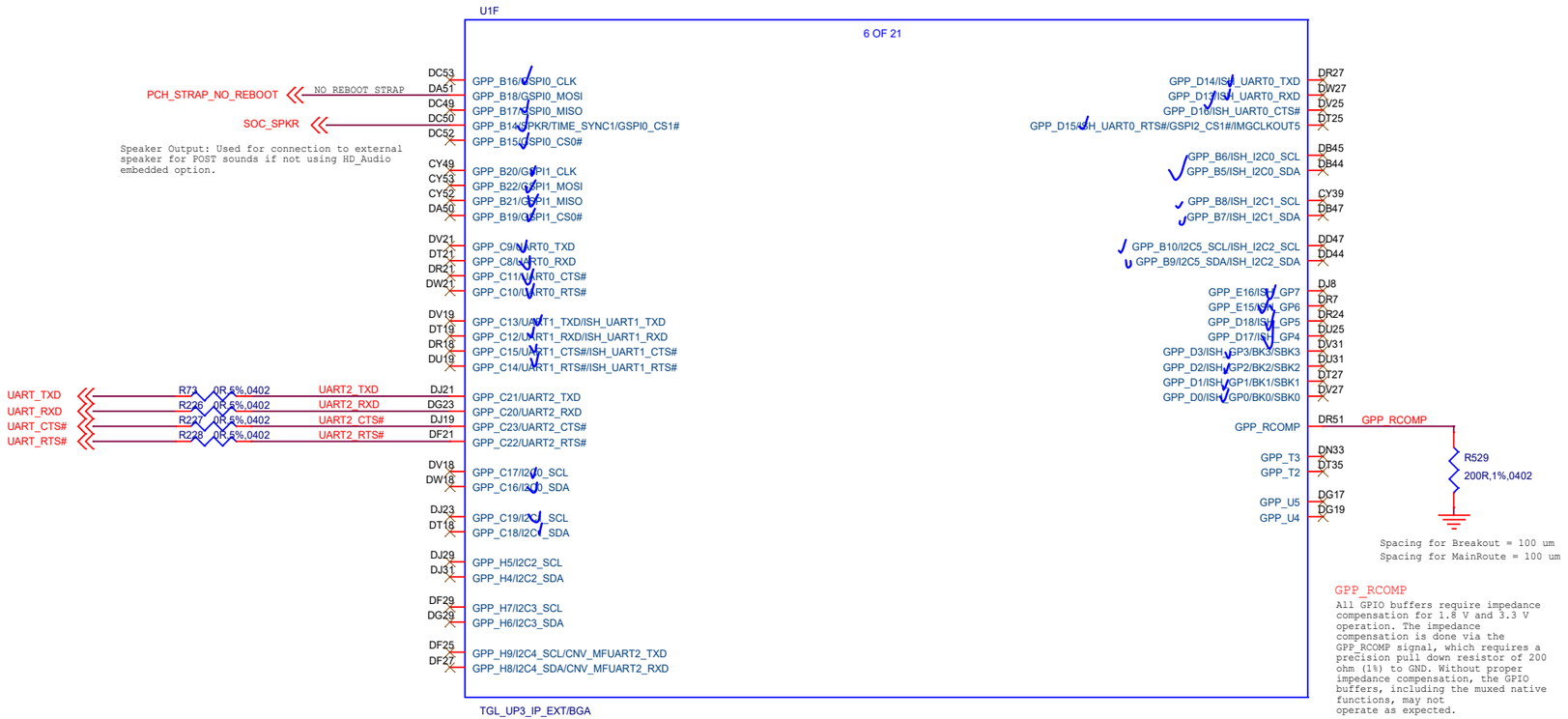

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AUDIO HAS NOT BEEN IMPLEMENTED IN TENSOR I22. INSTEAD, AUDIO TEL IS USED AND IT ONLY NEEDS USB SIGNALS. (P2)

6.10.2 Legacy Audio Interface - Signal Description

Table 86. Legacy Audio Signals

Signal Name	Description
Intel® High Definition Audio Interface	
HDA_RST#	Master hardware reset to external codec(s)
HDA_SYNC	48 KHz fixed rate sample sync to the codec(s)
HDA_BCLK	24.000 MHz serial data clock generated by the Intel® HD Audio controller.
HDA_SDO	Serial TDM data output to the codec(s)
HDA_SDIN [1:0]	Serial TDM data inputs from the codec(s)
I²S Interface	
I2S_MCLK1	I²S* Master Clock Output
I2S_MCLK2_INOUT	Second I²S* Master Clock Output. Can be configured as input as a reference clock.
I2S[5:0]_SCLK	I²S Serial Bit Clocks for connections to I²S devices.
I2S[5:0]_TXD	I²S Transmit Data (Serial Data Out) for connection to I²S devices.
I2S[5:0]_RXD	I²S Receive Data (Serial Data In) for connection to I²S devices.
I2S[5:0]_SFRM	I²S Serial Frame for connection to I²S devices.
DMIC Interface	
DMIC_CLK_A[1:0]	Serial data clock to module A (left microphone) DMIC on interface/port 0 or 1.
DMIC_CLK_B[1:0]	Serial data clock to module B (right microphone) DMIC on interface/port 0 or 1.
DMIC_DATA[1:0]	Serial data input from the digital microphone module

6.11 SoundWire* Interface Design Guidelines

For the Tiger Lake platform, SoundWire* is still the newest audio interface targeting (but not limited to) the phone, mobile, and desktop market as an alternative to Slimbus. Its main advantage is the connection simplicity with a 2 wire multi-drop topology + PDM streaming capabilities. For the Tiger Lake PCH there are 4 separate SoundWire interfaces that can be used.

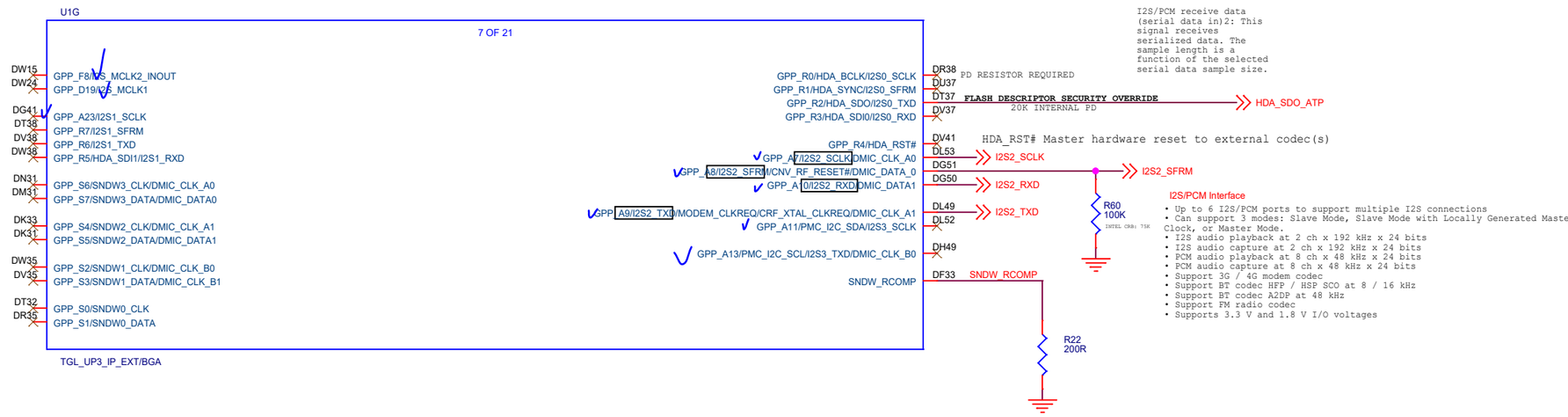
6.11.1 SoundWire* Platform Specific Important Information

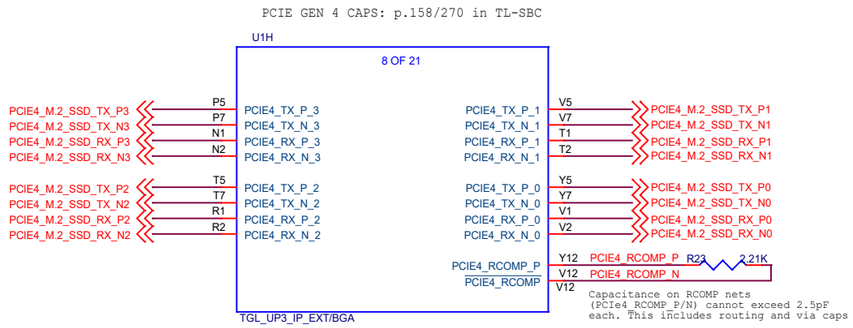
On the Tiger Lake platform the SoundWire* interface and other audio interfaces can be configured by itself or at the same time with other interfaces for connection to end devices. Refer Tiger Lake PCH-LP External Design Specification (#576591) for specific sku pins assignments.

6.11.2 SoundWire* Signal Description

Table 87. SoundWire* Signals

Signal Name	Description
SNDW0_DATA	SoundWire Data 0: Serialized data line containing frame and data being transmitted /Received
SNDW0_CLK	SoundWire Clock 0: Serial bit clock used to control the timing of a transfer.
SNDW1_DATA	SoundWire Data 1: Serialized data line containing frame and data being transmitted /Received
SNDW1_CLK	SoundWire Clock 1: Serial bit clock used to control the timing of a transfer.
SNDW2_DATA	SoundWire Data 2: Serialized data line containing frame and data being transmitted /Received
SNDW2_CLK	SoundWire Clock 2: Serial bit clock used to control the timing of a transfer.
SNDW3_DATA	SoundWire Data 3: Serialized data line containing frame and data being transmitted /Received
SNDW3_CLK	SoundWire Clock 3: Serial bit clock used to control the timing of a transfer.





12.2 PCIe4 Gen4 Interface Signals

Signal Name	Description	Dir	Buffer Type	Link Type	Availability
PCIE4_RCOMP_P PCIE4_RCOMP_N	Resistance Compensation for PEG channel	I	Analog	Diff	UP3/UP4/H Processor Lines
PCIE4_TX_P[3:0] PCIE4_TX_N[3:0]	PCIe Transmit Differential Pairs	O	PCIE	Diff	UP3/UP4/H Processor Lines
PCIE4_RX_P[3:0] PCIE4_RX_N[3:0]	PCIe Receive Differential Pairs	I	PCIE	Diff	UP3/UP4/H Processor Lines

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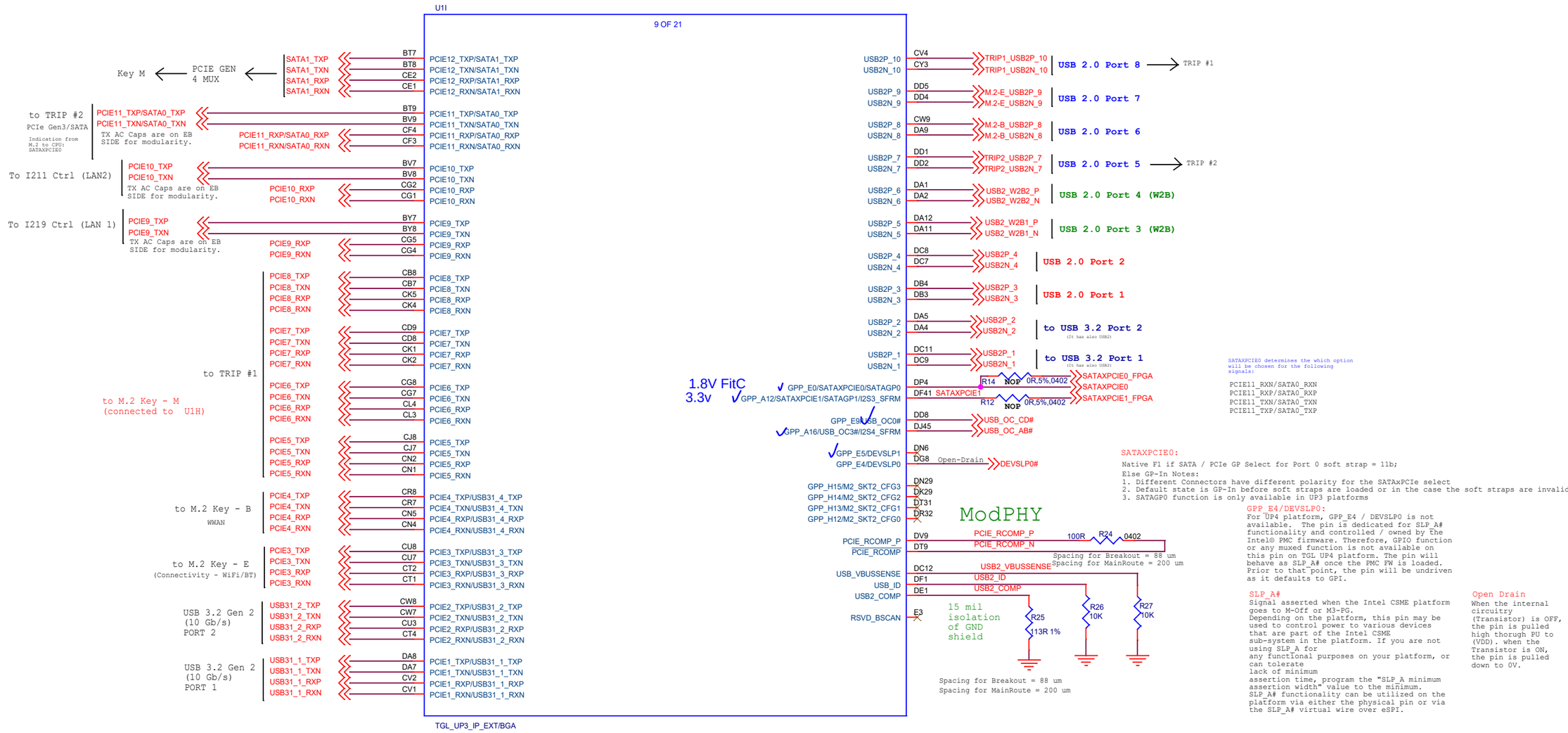

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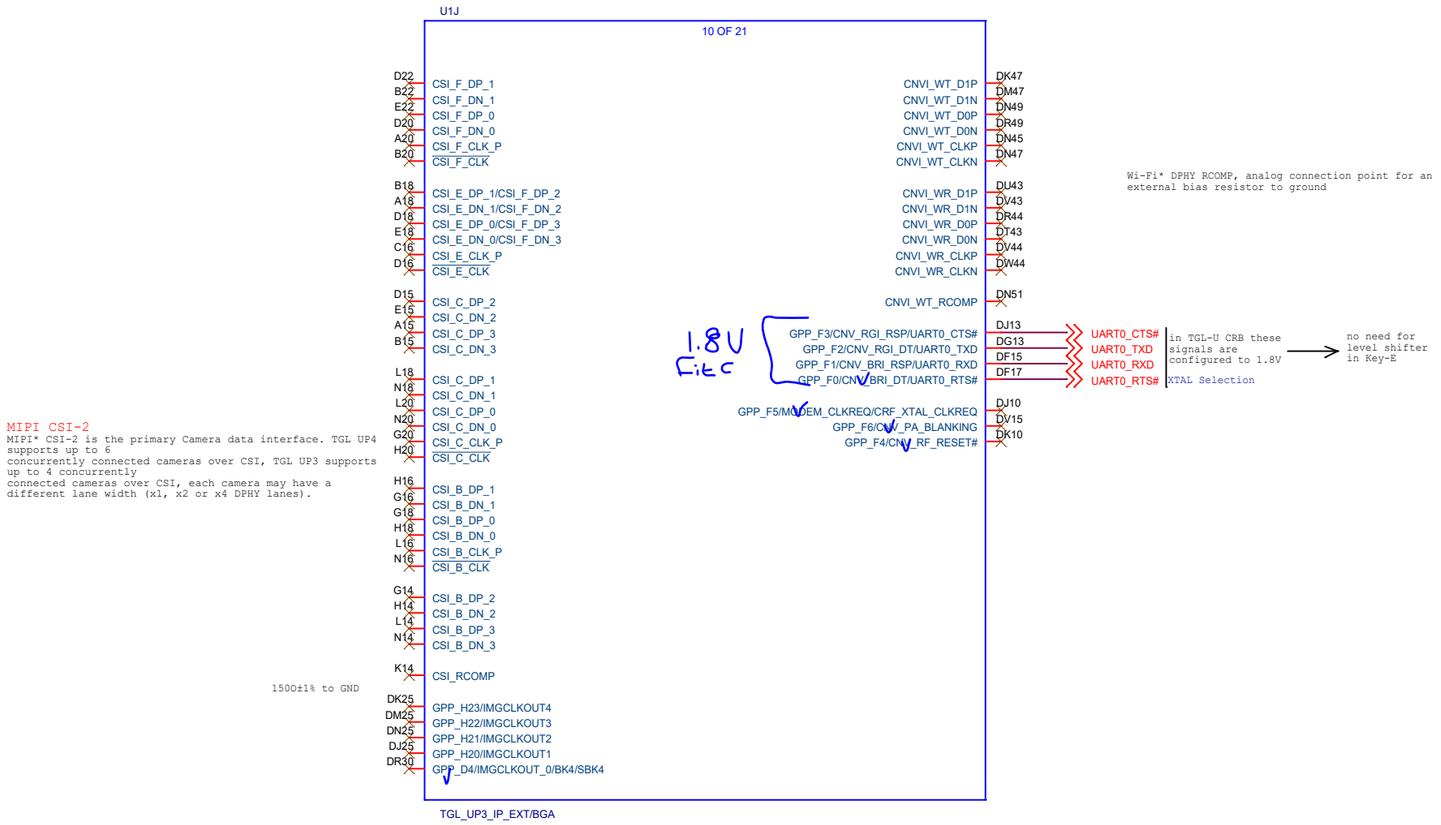

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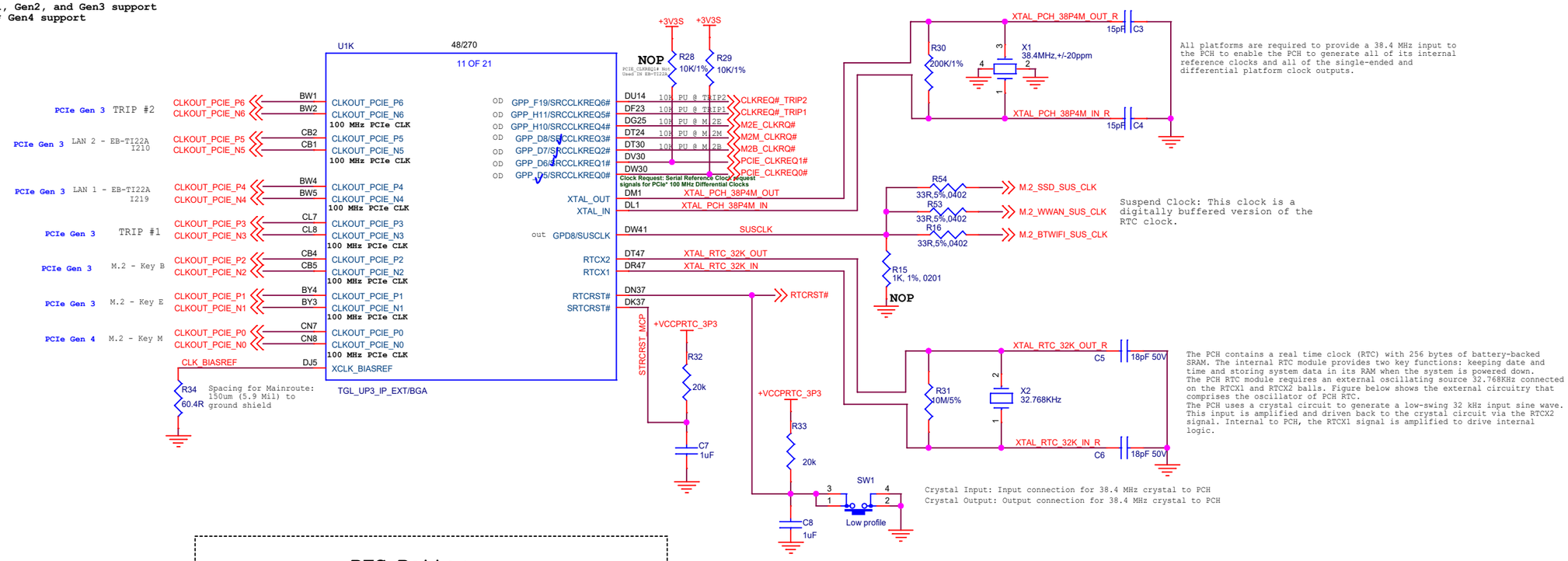
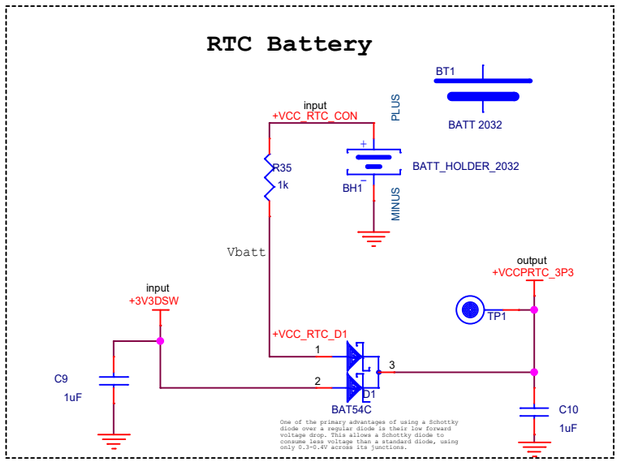
PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices
- **CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support**
- **CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support**



RTC RESET BUTTON



When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a
result of this, when the system boots, the BIOS knows that the RTC battery has been removed.
The RTCRST# signal may also be used to detect a low battery voltage. RTCRST# will be asserted during a power up from G3 state if the battery voltage is below 2V. This will set the RTC_PWR_STS bit as described above. If desired, BIOS may request that the user replace the battery. This RTCRST# circuit is combined with the diode circuit (refer figure above) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. The above figure is an example of this circuitry that is used in
conjunction with the external diode circuit.

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SLP_S0#
S0 Sleep Control. When PCH is idle and processor is in C10 state, this pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.

SLP_S5#
This signal is for power plane control. When asserted (low), it will shutoff power to all non-critical systems in S5 (Soft Off) states.

SLP_S4#
S4 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S4 (Suspend to Disk) and lower (S5).

SLP_S3#
S3 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S3 (Suspend to RAM) and lower (S4, S5).

SLP_A#
This signal is used to control power to additional devices on the platform in conjunction with the Intel© ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timings as SLP_S3#.

SYS_RESET#
When the SYS_RESET# pin is detected as active (on signal's falling edge if de-bounce logic is disabled, or after 16 ms if 16 ms debounce logic is enabled), the PCH attempts to perform a "graceful" reset by entering a host partition reset entry sequence.
Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the SYS_RESET# input remains asserted or not. It cannot occur again until SYS_RESET# has been detected inactive after the de-bounce logic, and the system is back to a full S0 state with PLTRST# inactive.

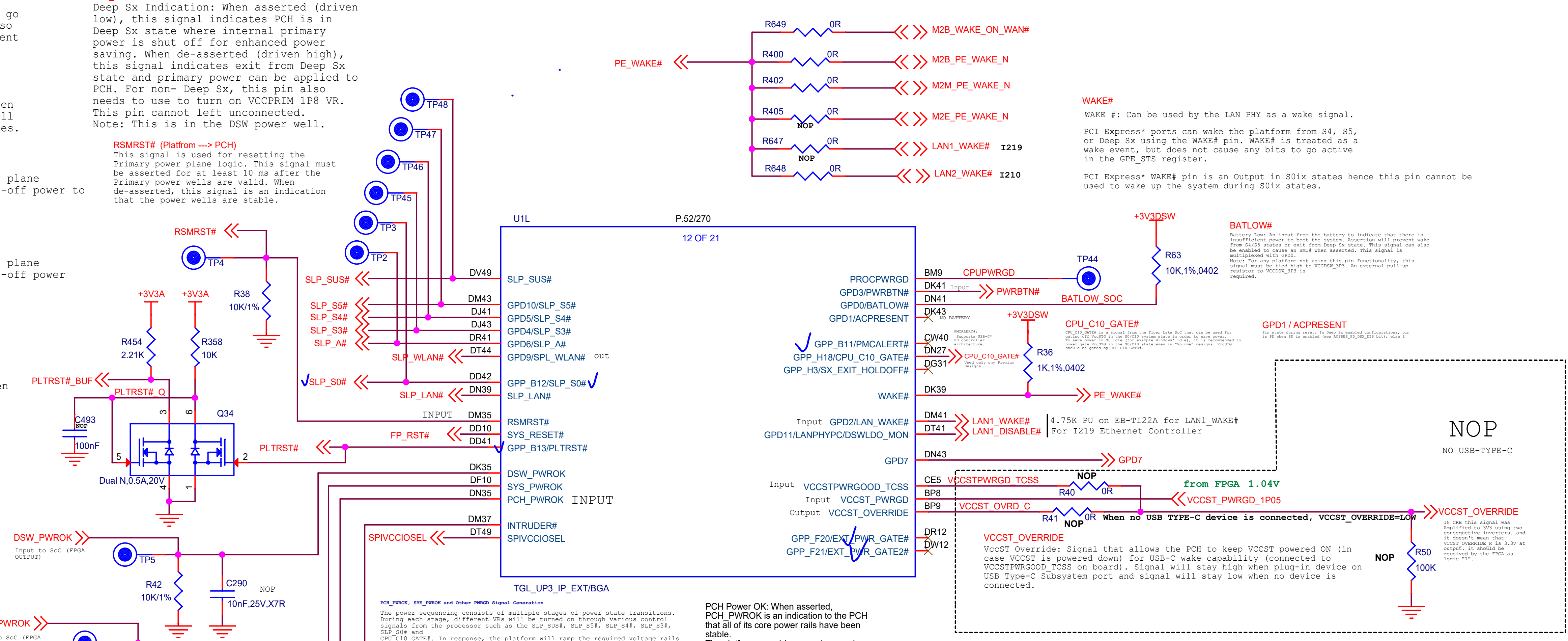
SLP_SUS#
(SLP_SUS# = HIGH --> Exist from Deep Sx)
(SLP_SUS# = LOW --> Enter Deep Sx) DG P.460
Deep Sx Indication: When asserted (driven low), this signal indicates PCH is in Deep Sx state where internal primary power is shut off for enhanced power saving. When de-asserted (driven high), this signal indicates exit from Deep Sx state and primary power can be applied to PCH. For non- Deep Sx, this pin also needs to use to turn on VCCPRIM_1P8 VR. This pin cannot left unconnected.
Note: This is in the DSW power well.

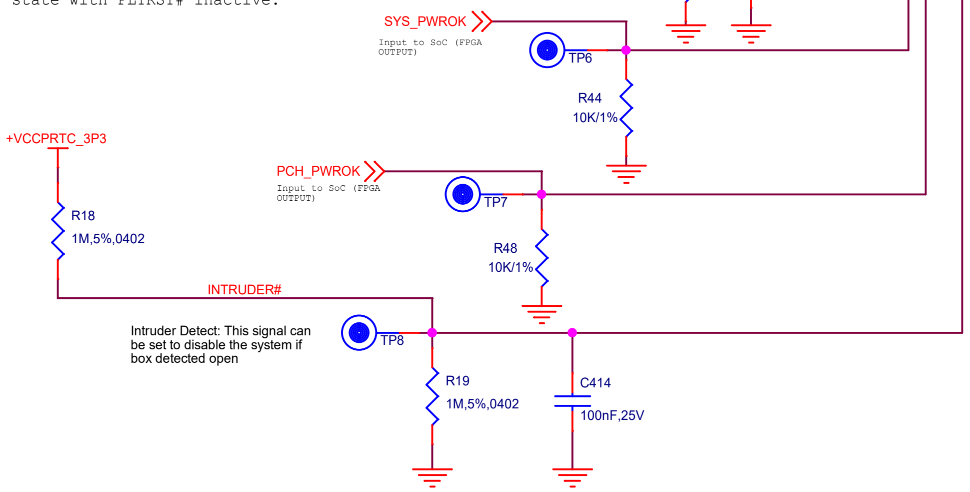
RSMRST# (Platfrom ---> PCH)
This signal is used for resetting the Primary power plane logic. This signal must be asserted for at least 10 ms after the Primary power wells are valid. When de-asserted, this signal is an indication that the power wells are stable.

WAKE#
WAKE #: Can be used by the LAN PHY as a wake signal.

PCI Express* ports can wake the platform from S4, S5, or Deep Sx using the WAKE# pin. WAKE# is treated as a wake event, but does not cause any bits to go active in the GPE_STS register.

PCI Express* WAKE# pin is an Output in S0ix states hence this pin cannot be used to wake up the system during S0ix states.





PCH_PWROK, SYS_PWROK and Other PWRGD Signal Generation

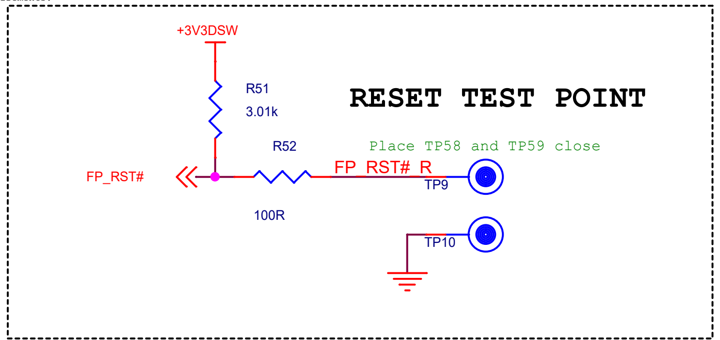
The power sequencing consists of multiple stages of power state transitions. During each stage, different VRs will be turned on through various control signals from the processor such as the SLP_SUS#, SLP_S5#, SLP_S4#, SLP_S3#, SLP_S0# and CPU_C10_GATE#. In response, the platform will ramp the required voltage rails in the required order and then asserted the various powergood signals required by the processor, and other platform components, after the necessarily timing requirements have been met. The below figure shows a high-level representative control signal and the powergood logic diagram for generating the PCH_PWROK and SYS_PWROK signals. This figure shows the recommended power-on sequencing flow steps from SLP_S4# de-assertion until PLTRST# de-assertion for the Tiger Lake platform.
During G3/DSx, S5 to S0 transitions, the platform will need to generate the DSW_PWROK and RSMRST# signals. In this phase of the power up sequence, the DSW and Primary power well voltage rails are ramped to the processor.
During S5 to S0 and DSx to S0 transitions, the platform will need to generate the VCCST_PWRGD, PCH_PWROK and SYS_PWROK signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up.
The PCH_PWROK signal is expected to be asserted by the platform to indicate to the processor that all required CPU voltage rails are up and stable, and that the processor may continue the final boot sequence leading up to PLTRST# de-assertion, such as starting to turn on clocks and executing other internal pre-reset activities.
SYS_PWROK is expected to be asserted by the platform to indicate that the system and all of its non-CPU components are ready for PLTRST# de-assertion. During power state transition to S0, the SYS_PWROK signal is the final platform controlled hardware gate before PLTRST# de-assertion. Platform designers may optimize when the SYS_PWROK signal is asserted with respect to the PCH_PWROK signal to help optimize overall boot latency, depending on system and component timing requirements.

PCH Power OK: When asserted, PCH_PWROK is an indication to the PCH that all of its core power rails have been stable.
The platform may drive asynchronously. When PCH_PWROK is de-asserted, the PCH asserts PLTRST#. Note: PCH_PWROK must not glitch, even if RSMRST# is low.

SYS_PWROK
System Power OK: This generic power good input to the PCH is driven and utilized in a platform-specific manner. While PCH_PWROK always indicates that the primary wells of the PCH are stable, SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset.

VCCSTPWRGOOD_TCSS
VCCSTPWRGOOD_TCSS: The processor requires this input signal to be asserted when the type-c subsystem requires keeping VCCST supply on (VCCST_OVERRIDE), even when entering S3/ S4- S5 states.
This signal start as low and may change polarity only at the entry to S3/ S4- S5. If required to toggle, the signal level must always change before the de-assertion of VCCST_PWRGD signal at the Sx entry flow.
This Signal must have a valid level during S0 - S5 power states.
S3 state is available only on H SKU.

Sx_Exit_Holdoff#
When S4/S5 is entered and SLP_A# is asserted, Sx_Exit_Holdoff# can be asserted by a platform component to delay resume to S0. SLP_A# de-assertion is an indication of the intent to resume to S0 (power up), but this will be delayed so long as Sx_Exit_Holdoff# is asserted. Sx_Exit_Holdoff is ignored outside of an S4/S5 entry sequence with SLP_A# asserted. With the de-assertion of RSMRST# (either from G3->S0 or DeepSx->S0), this pin is a GPIO input and must be programmed by BIOS to operate as Sx_Exit_Holdoff. When SLP_A# is asserted (or it is de-asserted but Sx_Exit_Holdoff# is asserted), the PCH will not access SPI Flash. How a platform uses this signal is platform specific.



Wake up on LAN / SLP_LAN#
SLP_LAN# is used to indicate when power to the LAN PHY is needed. If Host Wake On LAN or Intel© ME Wake on LAN is enabled, the SLP_LAN# signal will remain high to keep power on to the LAN PHY. The Integrated LAN (VccLAN) rail does not need to be powered in Sx/M-Off state unless they are needed as indicated by the TGP-LP signals like SLP_S3# and SUSPWRDNACK.

LAN_WAKE#
LAN WAKE: LAN Wake Indicator from the GbE PHY.
Note: LAN_WAKE# functionality is only supported with Intel PHY I219. Connection of a third party LAN device's wake signal to LAN_WAKE# is not supported.

LANPHYPC
LAN PHY Power Control: LANPHYPC should be connected to LAN_DISABLE_N on the PHY. PCH will drive LANPHYPC low to put the PHY into a low power state when functionality is not needed. Note: LANPHYPC can only be driven low if SLP_LAN# is de-asserted.

The PCH has an input signal, INTRUDER#, that can be attached to a switch that is activated by the system's case being open. This input has a two RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD_DET bit in the TCTL2 register. The INTRD_SEL bits in the TCTL2 register can enable the PCH to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP_EN bit.
The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD_DET bit. This allows the signal to be used as a GPI if the intruder function is not required.
If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET bit will go to a 0 when INTRUDER# input signal goes inactive.

RTC-Well Input Strap Requirements
All RTC-well inputs (RSMRST#, RTCRST#, SRTCRST#, INTRUDER#, PCH_PWROK, DSW_PWROK) must be either pulled up to VccRTC or pulled down to ground while in the G3 state. RTCRST#, when configured as shown in Figure 63 on page 126 meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PCH_PWROK and DSW_PWROK input signal should also be configured with an external weak pull-down.

SLP_WLAN# (GPD9)
The PCH controls the voltage rails into the external wireless LAN PHY using the SLP_WLAN# pin.
• The wireless LAN PHY is always powered when the Host is running.
– SLP_WLAN#='1' whenever SLP_S3#='1'.
• If Wake on Wireless LAN (WoWLAN) is required from S3/S4/S5 states, the host BIOS must set HOST_WLAN_PP_EN.
• If WoWLAN is required from Deep Sx, the host BIOS must set DSX_WLAN_PP_EN.
• If Intel© CSME has access to the Wireless LAN device:
– The Wireless LAN device must always be powered as long as Intel© CSME is powered. SLP_WLAN#='1' whenever SLP_A#='1'.
– If Wake on Wireless LAN (WoWLAN) is required from M-Off state, Intel© CSME will configure SLP_WLAN#='1' in Sx/M-Off.
Intel© CSME configuration of SLP_WLAN# in Sx/M-Off is dependent on Intel© CSME power policy configuration.
When the Wireless LAN device is an integrated connectivity device (CNVi) the connectivity device (CNVi) to the CNVi external RF chip (CRF) must be always on. In this case the SLP_WLAN# shall not control the CRF 3.3 V power rail.

PLTRST# PLTRST# = High (De-Asserted)

Reset Behavior
When a reset is triggered, the PCH will send a warning message to the processor to allow the processor to attempt to complete any outstanding memory cycles and put memory into a safe state before the platform is reset. When the processor is ready, it will send an acknowledge message to the PCH. Once the message is received the PCH asserts PLTRST#.
The PCH does not require an acknowledge message from the processor to trigger PLTRST#. A global reset will occur after four seconds if an acknowledge from the processor is not received.
When the PCH causes a reset by asserting PLTRST#, its output signals will go to their reset states.
A reset in which the host platform is reset and PLTRST# is asserted is called a Host Reset or Host Partition Reset. Depending on the trigger a host reset may also result in power cycling, refer to the below table for details. If a host reset is triggered and the PCH times out before receiving an acknowledge message from the processor a Global Reset with power-cycle will occur.
A reset in which the host and Intel© CSME partitions of the platform are reset is called a Global Reset. During a Global Reset, all PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. Intel© CSME and Host power back up after the power-cycle period.
Straight to S5 is another reset type where all power wells that are controlled by the SLP_S3#, SLP_S4#, and SLP_A# pins, as well as SLP_S5# and SLP_LAN# (if pins are not configured as GPIOs), are turned off. All PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. The host stays there until a valid wake event occurs.

SLP_A#
Signal asserted when the Intel CSME platform goes to M-Off or M3-PG.
Depending on the platform, this pin may be used to control power to various devices that are part of the Intel CSME sub-system in the platform. If you are not using SLP_A for any functional purposes on your platform, or can tolerate lack of minimum assertion time, program the "SLP_A minimum assertion width" value to the minimum. SLP_A# functionality can be utilized on the platform via either the physical pin or via the SLP_A# virtual wire over eSPI.

SLP_LAN#
SLP_LAN# is used to indicate when power to the LAN PHY is needed. If Host Wake On LAN or Intel© ME Wake on LAN is enabled, the SLP_LAN# signal will remain high to keep power on to the LAN PHY.
The Integrated LAN (VccLAN) rail does not need to be powered in Sx/M-Off state unless they are needed as indicated by the TGP-LP signals like SLP_S3# and SUSPWRDNACK.

LAN Sub-System Sleep Control: If the Gigabit Ethernet Controller is enabled, when SLP_LAN# is de-asserted (LOW) it indicates that the PHY device must be powered. When SLP_LAN# is asserted, power can be shut off to the PHY device.
Note: If Gigabit Ethernet Controller is statically disabled via BIOS, SLP_LAN# will be driven low.

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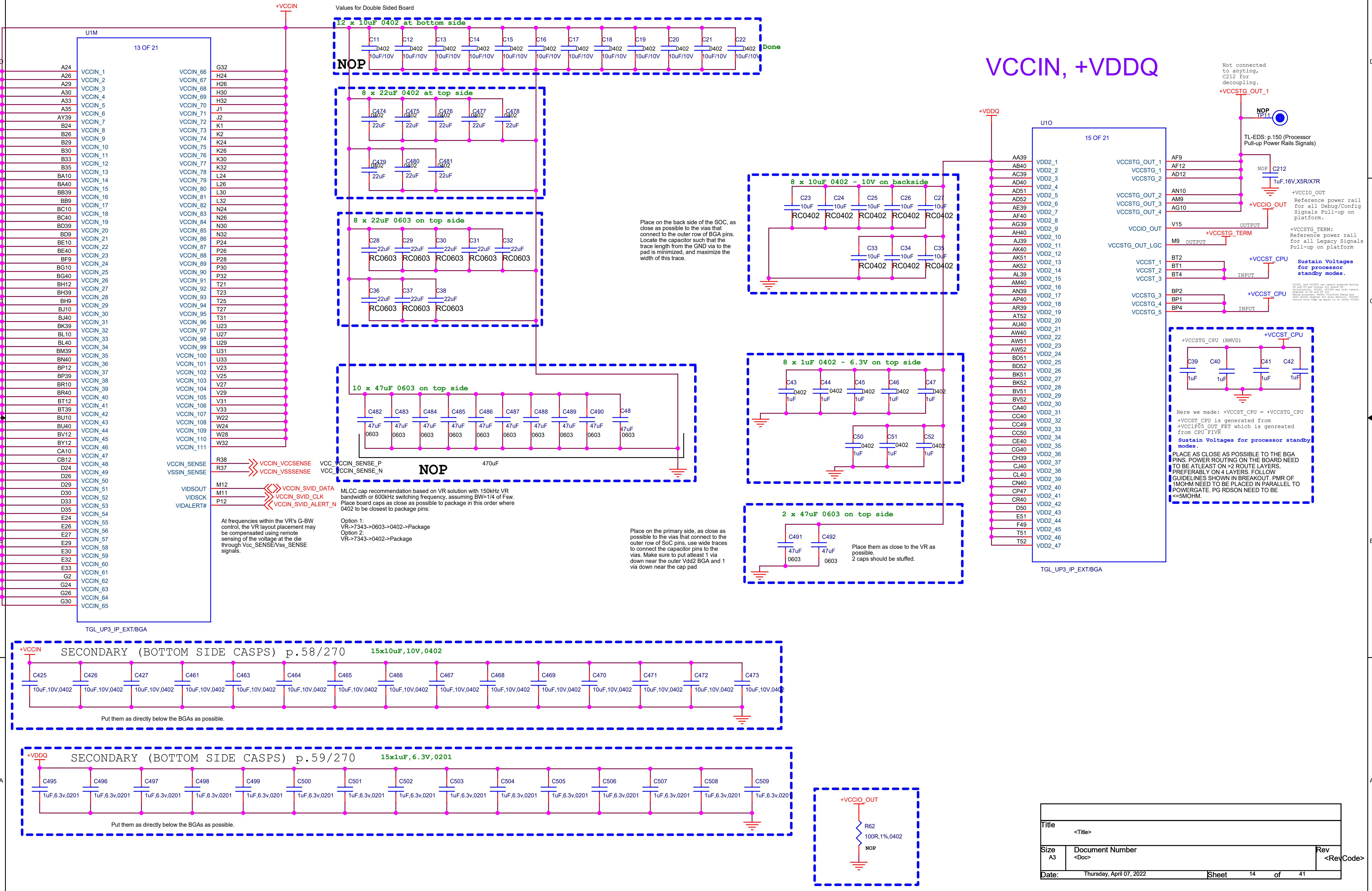

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VCCIN_AUX, VCCPRIM

From External DC\DC to SoC

U1N

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+VCCIN_AUX

AB12 VCCIN_AUX_1
AC10 VCCIN_AUX_2
AE10 VCCIN_AUX_3
AK2 VCCIN_AUX_4
AR10 VCCIN_AUX_5
AT12 VCCIN_AUX_6
AU10 VCCIN_AUX_7
AW10 VCCIN_AUX_8
BV1 VCCIN_AUX_9
BV39 VCCIN_AUX_10
BW40 VCCIN_AUX_11
BY39 VCCIN_AUX_12
CC1 VCCIN_AUX_13
CD12 VCCIN_AUX_14
CF10 VCCIN_AUX_15
CG12 VCCIN_AUX_16
CH10 VCCIN_AUX_17
CJ1 VCCIN_AUX_18
CJ12 VCCIN_AUX_19
CK10 VCCIN_AUX_20
CL12 VCCIN_AUX_21
CM10 VCCIN_AUX_22
CP1 VCCIN_AUX_23
CP10 VCCIN_AUX_24
CR12 VCCIN_AUX_25
CT10 VCCIN_AUX_26
CU12 VCCIN_AUX_27
CY1 VCCIN_AUX_28
AK1 VCCIN_AUX_29

+3V3A → +VCCPGPPR_3P3_1P8 — R77 NOP 0R,5%,0402

in TL-SBC: +VCCPDSW_3P3 is generated from +V3.3A_DSW (p. 225/270)

+V1.8A → +VCCPRIM_1P8 — R6 0R,5%,0402

R64 0R,5%,0402 — 0.68uH, 20%, 150mA, 0.8ohm — NOP L10 — +VCCA_CLKLDO_1P8

The inductor and capacitor form an LC filter to filter out the switching noise either from the power supply itself or from the other components connected to the power supply. The resistor dampens the LC filter to prevent unwanted resonance. LC filters like this often use a high ESR tantalum capacitor instead of adding a separate resistor.
L/C Filter: LOW PASS

+VCCPGPPR_3P3_1P8 — R78 0R,5%,0402

R66 0R,5%,0402 — RC_CLKLDO — C211 47uF,6.3V,X5R

R66:
Option 1: stuff with 0 ohm if the inductor is not stuffed. Option 2: stuff 100 mohm if the inductor stuffed

TP52 TP51 TP50 TP49

VCCIN_AUX_VSSSENSE — AV9 VCCIN_AUX_VSSSENSE
VCCIN_AUX_VCCSENSE — AT9 VCCIN_AUX_VCCSENSE

VCC_VNNEXT_1P05_1 — DD17 VCC_VNNEXT_1P05_1
VCC_VNNEXT_1P05_2 — DD18 VCC_VNNEXT_1P05_2

VCC_V1P05EXT_1P05_1 — DA15 VCC_V1P05EXT_1P05_1
VCC_V1P05EXT_1P05_2 — DA17 VCC_V1P05EXT_1P05_2

VRALERT_MCP# — 0R R74 — VRALERT_MCP#_C — DB39 GPP_B2/VRALERT# (output)
GPPC_B2_BC_PROCHOT_N
DV12 GPP_F22/NNN_CTRL
DT12 GPP_F23/V1P05_CTRL

VCCIN_AUX_CORE_VID0_R — 0R R75 — GPPC_B0_CORE_VID_0 — DB37 GPP_B0/CORE_VID0
VCCIN_AUX_CORE_VID1_R — 0R R76 — GPPC_B1_CORE_VID_1 — DB38 GPP_B1/CORE_VID1

VRALERT#: ICC Max. throttling indicator from the PCH voltage regulators. VRALERT# pin allows the VR to force PCH throttling to prevent an over current shutdown. PMC based on the VRALERT# and messages from the processor. The messages from the processor allows the processor to constrain the PCH to a particular power budget.

TGL_UP3_IP_EXT/BGA

input

1.8 V Primary Well. +VCCPRIM_1P8 (+V1.8A)

CY18 VCCPRIM_1P8_1
CY20 VCCPRIM_1P8_2
CY24 VCCPRIM_1P8_3
CY26 VCCPRIM_1P8_4
DA18 VCCPRIM_1P8_5
DA20 VCCPRIM_1P8_6
DA22 VCCPRIM_1P8_7
DA24 VCCPRIM_1P8_8
DA26 VCCPRIM_1P8_9
DC18 VCCPRIM_1P8_10
DC20 VCCPRIM_1P8_11
DC22 VCCPRIM_1P8_12
DC24 VCCPRIM_1P8_13
DC26 VCCPRIM_1P8_14
DD20 VCCPRIM_1P8_15
DD22 VCCPRIM_1P8_16
DV22 VCCPRIM_1P8_17

+VCCPRIM_3P3 3.3 V Primary Well. +3V3A

DA35 VCCPRIM_3P3_1
DC28 VCCPRIM_3P3_2
DC30 VCCPRIM_3P3_3
DD30 VCCPRIM_3P3_4

RTC de-coupling capacitor only. This rail should not be driven by any motherboard power rails.

+VCCRTCEXT — DV34 DCPRTC

+VCCLDOSTD_OUT_0P85 — DV46 VCCLDOSTD_0P85

This rail is generated internally and needs to be routed out to the motherboard for decoupling purposes.
Not Connected to any target except decoupling capacitor: C105

+VCCA_CLKLDO_1P8

DV16 INPUT VCCA_CLKLDO_1P8_1
DC15 VCCA_CLKLDO_1P8_2

1.24 V for CNVi logic. This rail is generated internally with an LDO and needs to be routed to the motherboard for decoupling purpose only. This rail should not be driven by any motherboard power rails.
Not Connected to any target except decoupling capacitor: C107

+VCCDPHY_1P24_SOC — DV28 OUTPUT VCCDPHY_1P24

Deep Sx Well: 1.05 V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic.
Not Connected to any target except decoupling capacitor: C104

+VCCDSW_1P05_SOC — DD38 VCCDSW_1P05

+VCC1P05_OUT_FET

1.05 V Primary Well: for CNVi and other internal I/O blocks.
(Make small plane not connected to anything except these 3 balls)

+VCC1P05_OUT_PCH

BR3 merge pins together
BR4
BT5
VCC1P05_OUT_FET_1
VCC1P05_OUT_FET_2
VCC1P05_OUT_FET_3

+VCCPRTC_3P3

Audio Power 3.3 V or 1.8 V. is supplied from +V1.8A or from +3V3A

Deep Sx Well +3V3DSW

DA31 VCCPRIM1P05_OUT_PCH_1
DC33 VCCPRIM1P05_OUT_PCH_2
DC31 VCCPRIM1P05_OUT_PCH_3

+VCCPGPPR_3P3_1P8

+VCCPRIM_3P3 3.3 V Primary Well. +3V3A

p234/270 TL-SBC

DC35 VCCRTC
DD37 VCCDSW_3P3 — 3.3-V supply for Deep Sx wells. (input)
DA28 VCCPGPPR

1.8 V Primary Well. +VCCPRIM_1P8

CY31 VCCPRIM_3P3_5
CY33 VCCPRIM_3P3_6 — PCH I/O and Misc 3.3V Rail(Primary Well)
CV39 VCCPRIM_1P8_18 — PCH I/O and Misc 1.8V Rail(Primary Well)

input

AP12 RSVD_1

+VCCIN_AUX — 15 x 10uF 0402 on topside

C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67
0402 10uF/10V

+VCCIN_AUX — 10 x 10uF 0402 on bottom

Done

C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82
0402 10uF/10V

+VCCIN_AUX 12 x 22uF 0603 on topside

C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94
22uF RC0603

C510,C11,C512 (Deleted, See Ver4.5)

Use 2.5V rating caps.
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth, or 600kHz switching frequency assuming BW= ¼ of Fsw.
Place board caps as close as possible to package in this order where 0402 to be the closest to package pins:
VR ?7343? 0805? 0603-> 0402 ? package.
*a DCLL of 3.3mohm is required and bulk capacitors must be used.

Pair board caps with power/ground PTHs.
Align caps along current flow path from VR to package pins.

Use 2.5V rating caps.
MLCC cap recommendation based on VR solution with 150kHz VR bandwidth, or 600kHz switching frequency assuming BW= ¼ of Fsw.

Place board caps as close as possible to package

VCCA_CLKLDO_1P8 is supplying to PCH Clock. (analog supply)

+VCCPRTC_3P3 — C95 1uF — C96 100nF
+VCCPDSW_3P3 / +3V3A — C97 NOP 1uF,16V,X5R/X7R
+VCCPRIM_3P3 / +3V3A — NOP C98 1uF — NOP C99 100nF
+VCCPRIM_1P8 — NOP C100 1uF

NOTE: PLACE CAP CLOSEST POSSIBLE TO THE BGA

+VCCDSW_1P05_SOC — TP13 — C104 1uF,6.3V,X5R/X7R
+VCCLDOSTD_OUT_0P85 — TP14 — C105 2.2uF,10V,X5R
+VCCRTCEXT — TP12 — C106 100nF,25V,X5R/X7R
+VCCDPHY_1P24_SOC — C107 4.7uF,10V,20%

The VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two optional dedicated voltage regulators that save platform power during low power states.

Trade-offs - Volume vs. Premium Power Maps:

Power maps are broken into two tiers: Volume and Premium. Volume focuses on cost savings with the fewest VRs and Premium focuses on the smallest solution size with the lowest power consumption. For a design focused on S0ix or Modern Standby* power, the Premium power map is recommended. The designer may choose to implement a hybrid between Volume and Premium as long as guidelines are followed.

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+3V3DSW/+3V3A/+3V3S

3.3V , 13A

R_TON = Vout/(VFB * f * C_TON) -6.5K = 3.3/(2*(490X10^3)*16.26pF) -6.5K = 200593.90767 Ohm

R_TON = Vout/(VFB * f * TON) -6.5K

f = 490kHz

U3 MAX8792

VDD, TON, BST, VCC, DH, LX, DL, PGOOD, EN, SKIP#, REF, FB, ILIM, REFIN, GND_PAD

+5V_LDO <= 20mA

C108 1uF

R80 10K

C119 NOP 1uF

V33_VCC

C118 1uF

AGND_V33

V33DSW_OK

TP18

V33DSW_EN

TP19

V33_SKIP#

R88 0R NOP

R89 0R NOP

R90 0R NOP

2v

V33_REF

C132 10nF,25V

J1 Jumper Short

V33_TON

R79 200K

V33_BOOT

C113 100nF

V33_DH

VDS = 12V-3.3V = 8.7V

On-time and off-time specifications are measured from 50% point to 50% point at the DR pin with LX = GND, VBST = 5V, and a 250pF capacitor connected from DR to LX. Actual in-circuit times can differ due to MOSFET switching speeds.

Q3 FDMS7682

C114 10uF,16V RC0603

C115 10uF,16V RC0603

C116 47uF,16V C1210H2_5

C117 47uF,16V C1210H2_5

+3V3DSW

TP17

L1 2.2uH,14A ,18mOhm

V33_LX

Q8 FDMS7660

V33_DL

C122 100uF C1206

C123 100uF C1206

C124 100uF C1206

C125 100uF C1206

C126 100uF C1206

C127 NOP 100uF C1206

C128 NOP 100uF C1206

R91 6.49K

V33_FB

I(MAX)=0.05*V(ILIM)/Rds(on)

V33_REF

R92 15k

C133 100nF NOP

R93 10k

V33_ILIM

0.8V (16A max)

R96 10K

AGND_V33

+3V3A , 3A

NDS335N,3A

TP15

+12V_MAIN

Q1 H=1.15mm

R81 10k

+3V3DSW

R85 10k

V33A_GATE

C120 220nF

Q4 NDS335N,3A

V33A_EN#

NOP R87 10k

Q5 NDS335N,3A

V33A_DIS

R83 100R

C109 22uF,6.3v C0805

C110 100uF C1206

V33A_EN# = LOW --> 3V3A High

V33A_EN# = High--> 3V3A LOW

p234/270 TL-SBC

+3V3S , 10A

FDMS7682,15A

TP16

Q2 H=1.12mm

R82 10k

V33S_GATE

C121 220nF

Q6 NDS335N,3A

V33S_EN#

Q7 NDS335N,3A

R84 100R

V33S_DIS

C111 22uF,6.3v C0805

C112 100uF C1206

V33S_EN# = HIGH --> 3V3S LOW

V33S_EN# = LOW --> 3V3S HIGH

Deleted:

C137
C138
C142
C143
C144
C150
C151
C152

the larger VGS the less Rds(on) Reistance for the same current

3.3V for LAN

Q9 NDS335N,3A

TP20

+12V_MAIN

R94 10k

(We need PU's to +3V3A and +12V_MAIN to enable that)

V33LAN_GATE

C134 10nF,25V

R95 100R

V33LAN_DIS

C129 47uF C0805

C130 47uF C0805

C131 100uF C1206

+3V3A

Q10 NDS335N,3A

R97 10k

Q11 NDS335N,3A

V33LAN_GATE_A

Q12 NDS335N,3A

SLP_LAN#

NOP C155 220nF

SLP_LAN# = HIGH --> +3V3LAN = HIGH (SYSTEM NOT ON SLEEP)

SLP_LAN# = LOW--> +3V3LAN = LOW (We need PU's to 12V_MAIN and +3V3A to enable that)

TensorI20 had no PHY on any TEL. so this circuit wasn't used.
it was used in Airtop3.

+5V_LDO, 500mA

+12V_MAIN

TP21

LT3065 U4

VIN, VIN, VOUT, VOUT, PWRGD, SHD#, IMAX, ADJ, REF/BP, GND, GND

C156 1uF,16V RC0402

+5V_LDO

20K R98

C157 2.2uF

C158 2.2uF

0.6V V5LDO_FB

V5LDO_SS

C159 10nF,25V

R99 2.74K

3.3V for WLAN

+3V3A_WLAN

TP35

Q39 NDS335N,3A

+3V3DSW

+12V_MAIN

R352 10k

V3.3A_WLAN_GATE

C378 10nF,25V

C377 1uF,50V RC0603

C376 22uF,6.3v C0805

R353 100R

V3.3A_WLAN_DIS

+3V3A

R354 10k

Q38 NDS335N,3A

Q40 NDS335N,3A

V3.3A_WLAN_GATE_A

3V3A = HIGH ---> V3.3A_WLAN_GATE_A = LOW ---> V3.3A_WLAN_DIS = +V3.3A_WLAN = HIGH

3V3A = HIGH ---> V3.3A_WLAN_GATE_A = LOW ---> V3.3A_WLAN_GATE = HIGH ---> +V3.3A_WLAN = HIGH

+3V3A (SLP WLAN IS NOT ACTIVATED)

R356 100K 1%,0201

SLP_WLAN#

NOP R409 0R 5% 0201

FPGA_SLP_WLAN#

NOP R410 0R 5% 0201

V3.3A_WLAN_SLP_CTRL

Q41 NDS335N,3A

NOP C513 220nF

SLP_WLAN# = HIGH --> +3V3_WLAN = HIGH (SYSTEM NOT ON SLEEP)

SLP_WLAN# = LOW--> +3V3_WLAN = LOW

TensorI20 had no PHY on any TEL. so this circuit wasn't used.
it was used in Airtop3.

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Size A3	Document Number <Doc>	Rev <RevCode>
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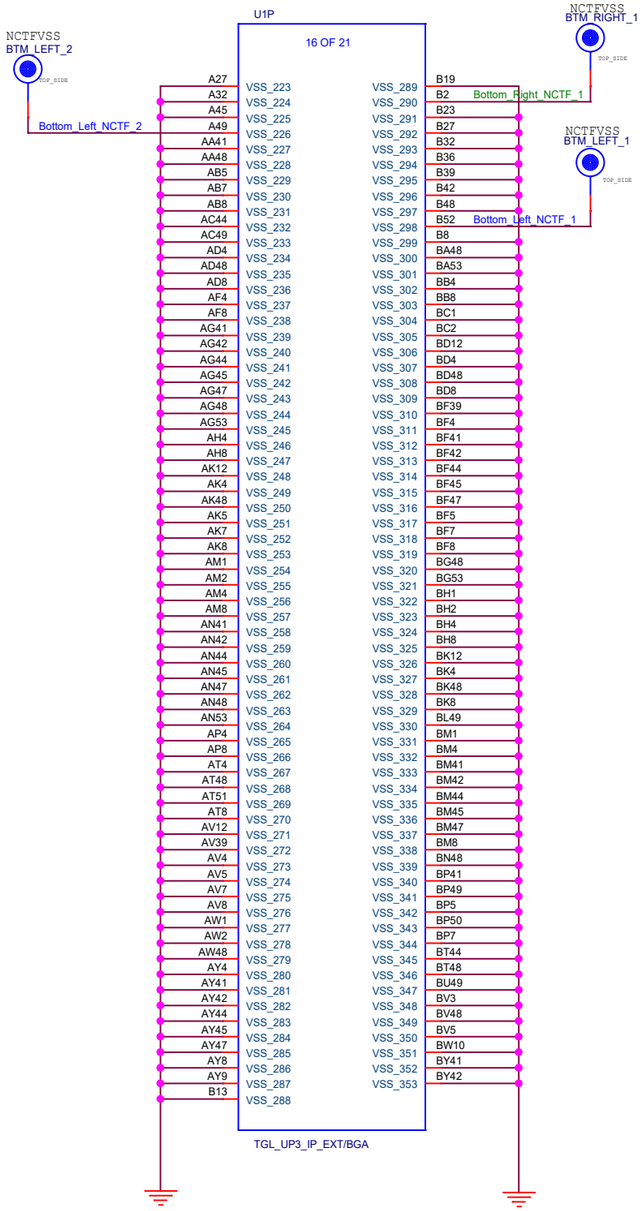
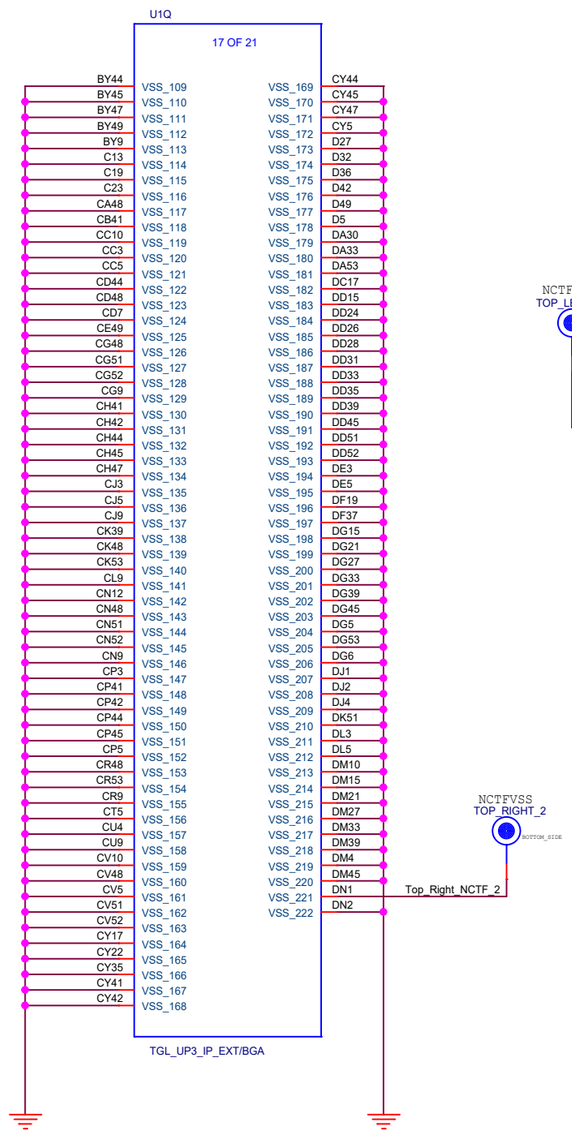
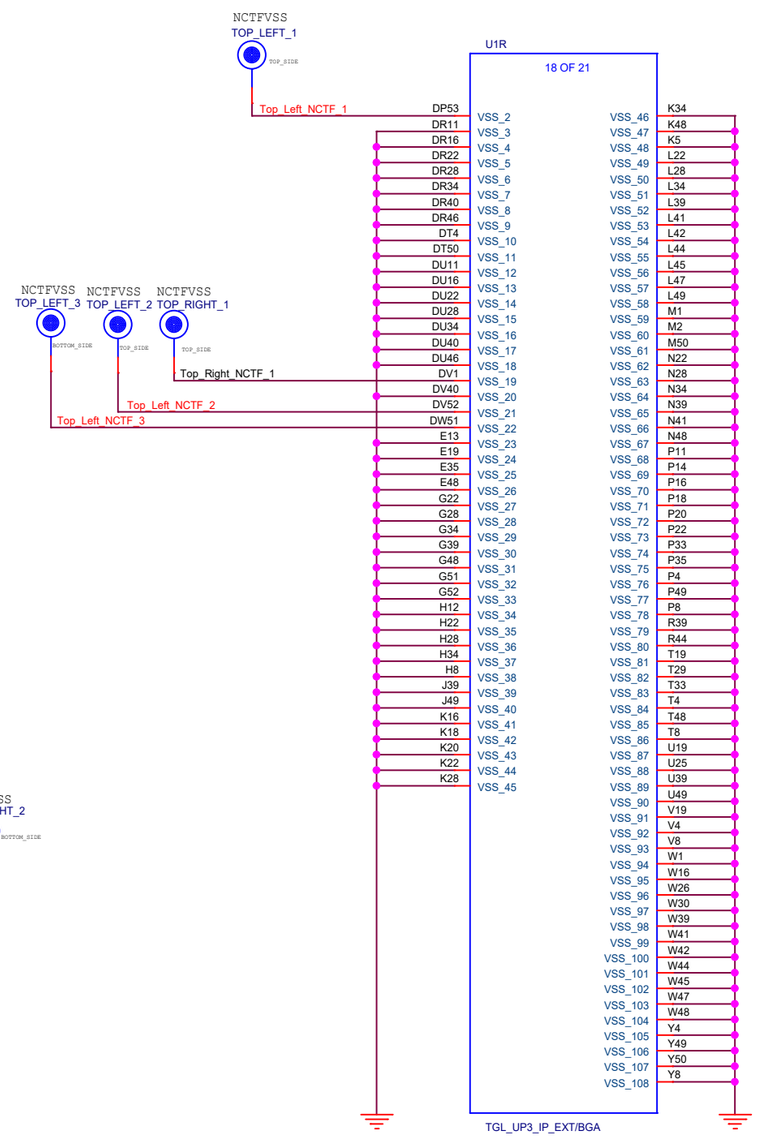
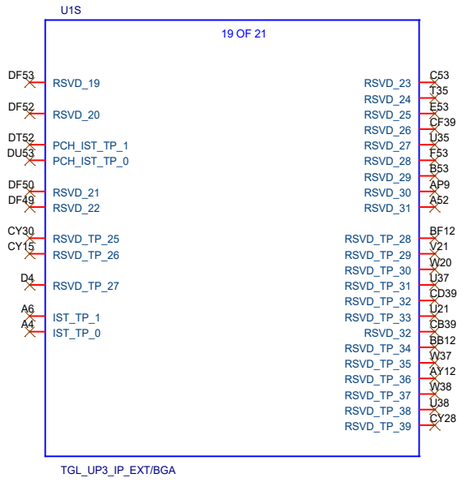






Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Thursday, April 07, 2022	Sheet 17 of 41	



Title <Title>		
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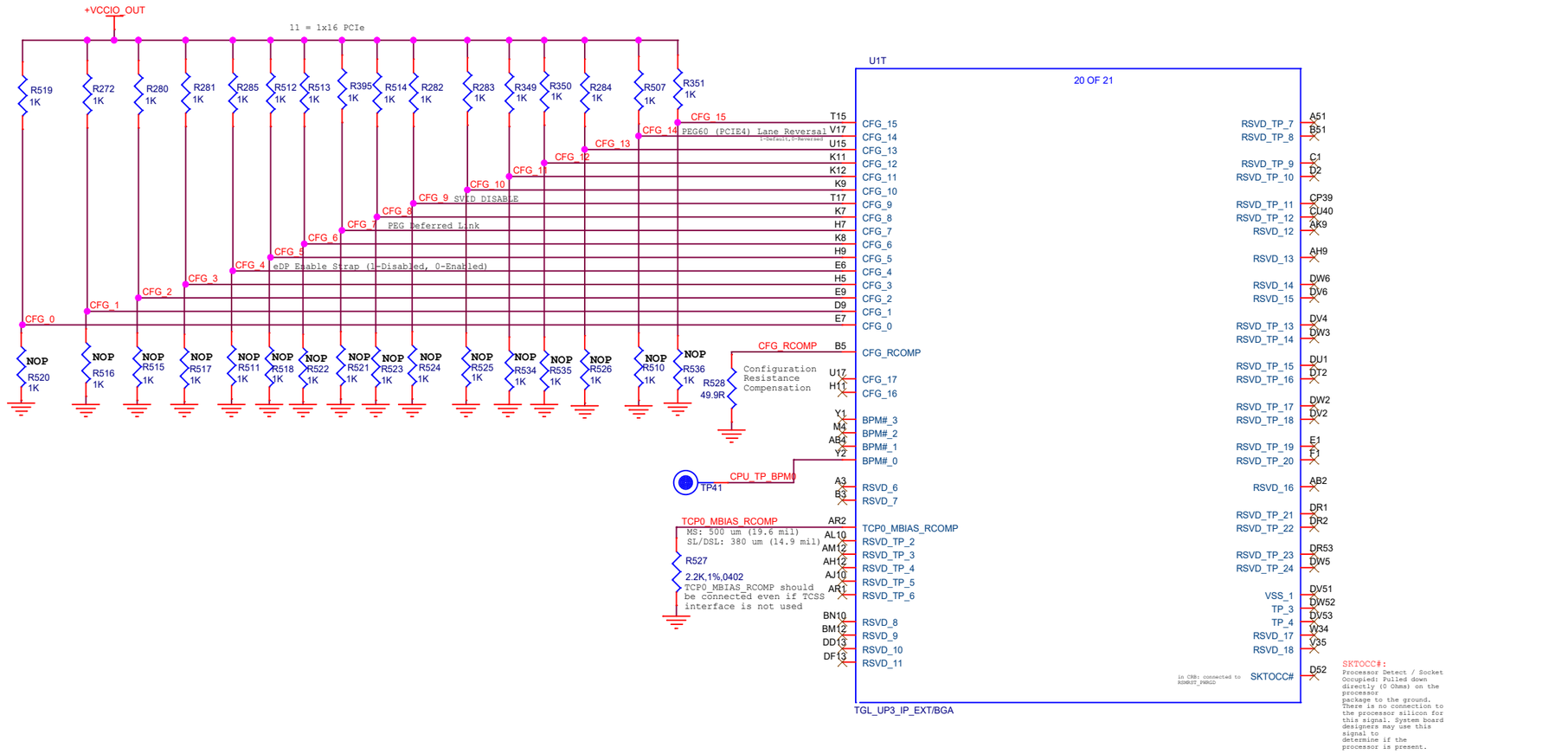
CFG[17:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[3], CFG[0]**: Reserved configuration lane. • **CFG[2]: TGL UP4/UP3** Reserved • **CFG[2]: H** PCI Express* Static x16 Lanes Numbering Reversal. — 1 - (Default) Normal — 0 - Reversed • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]: TGL UP4/UP3** Reserved • **CFG[6:5]: H** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[13:7]:** Reserved configuration lanes. • **CFG[14]**: PEG60 (PCIE4) Lane Reversal: — 1 - (Default) Normal — 0 - Reversed • **CFG[17:15]:** Reserved configuration lanes.	I	GTL	SE	UP3/UP4/H Processor Lines



BPM#[3:0]
Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM#[3:0]	Pull Up/Pull Down	VCC_{IO}_OUT	16-60 Ω
PROC_PREQ#	Pull Up	VCC_{STG}	3 KΩ
PROC_TDI	Pull Up	VCC_{STG}	3 KΩ
PROC_TMS	Pull Up	VCC_{STG}	3 KΩ
PROC_TRST#	Pull Down	VCC_{STG}	3 KΩ
PROC_TCK	Pull Down	VCC_{STG}	3 KΩ
CFG[17:0]	Pull Up	VCC_{IO}_OUT	3 KΩ

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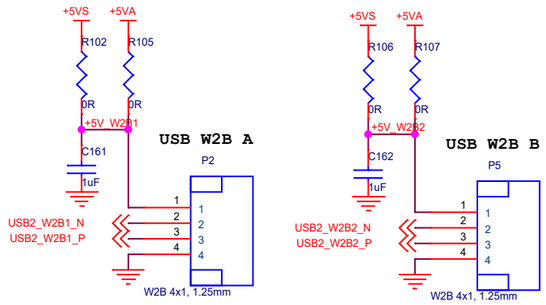
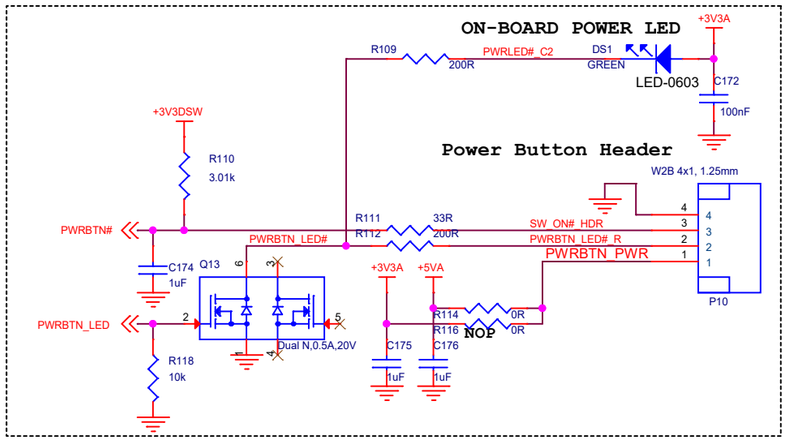
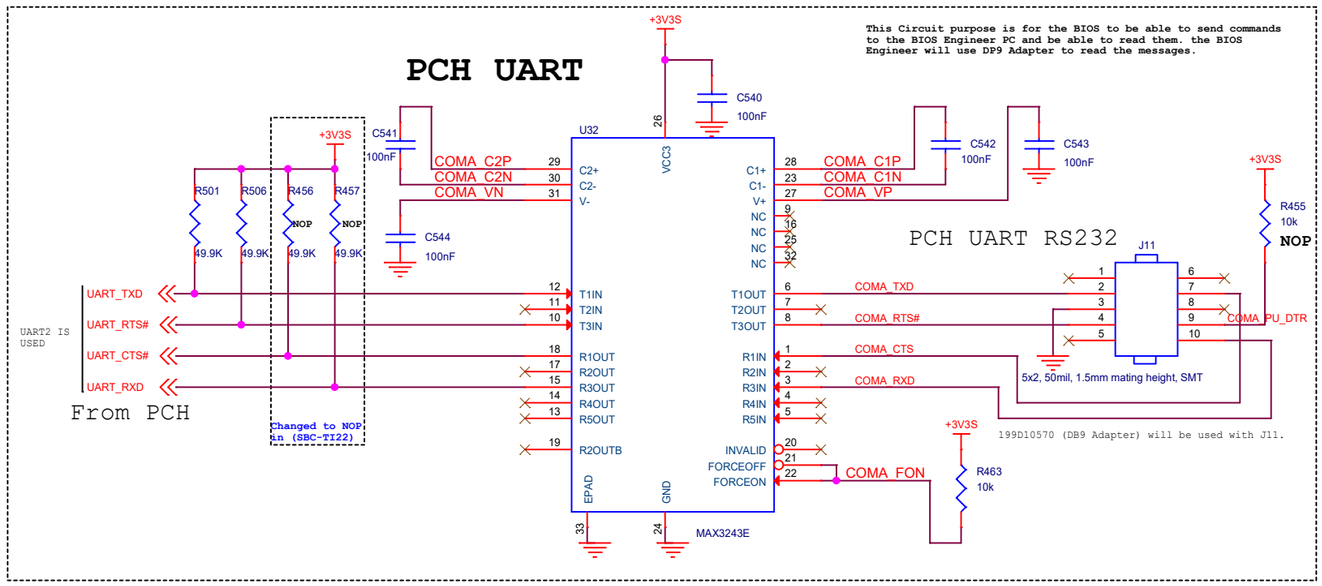
Headers



audio **Extension headers**

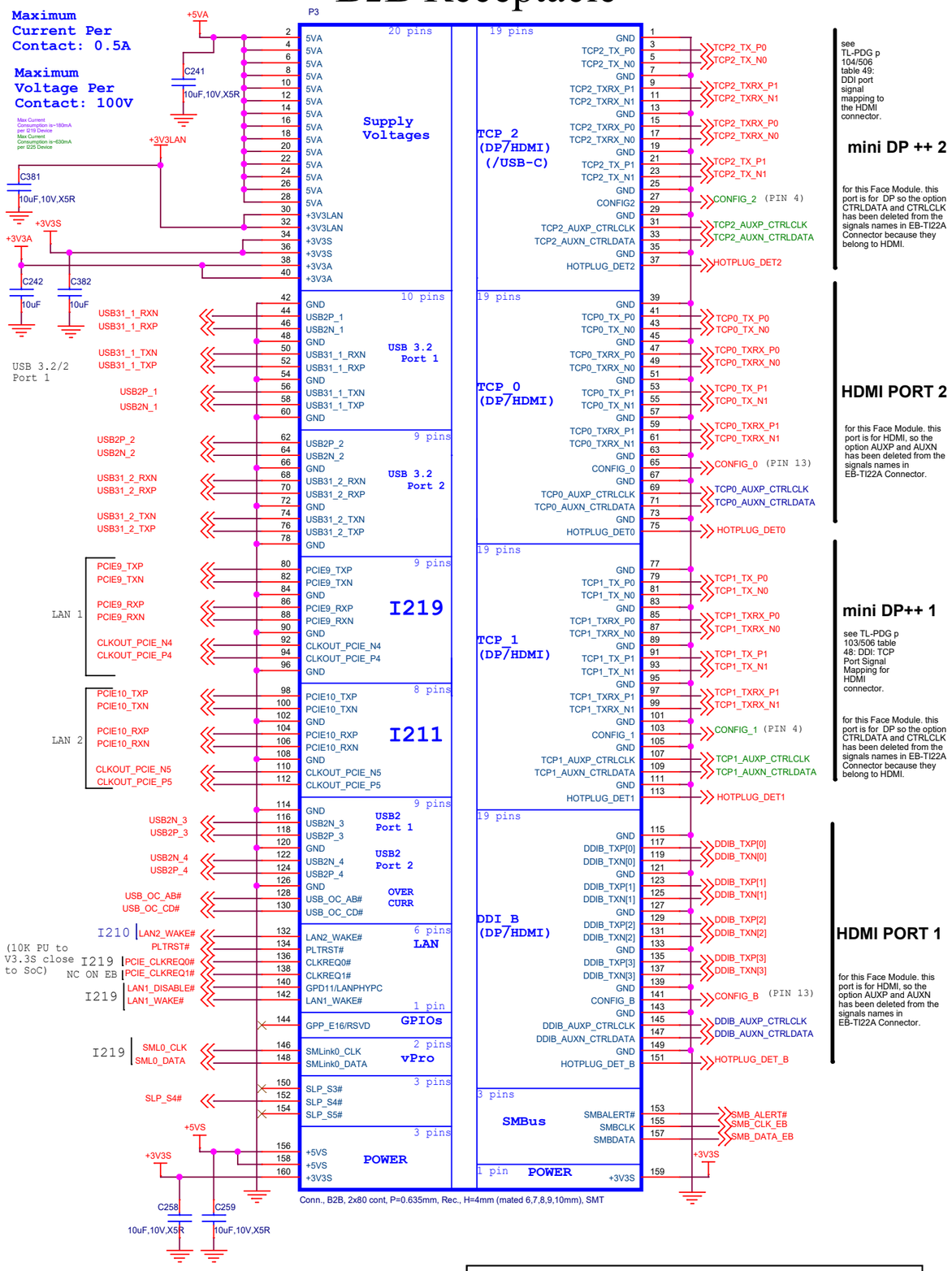
Note: The Intel® Ethernet Connection I219 can be connected to one of the following PCI Express* ports 7, 8 or, 9





182K16001S

B2B Receptacle



see TL-PDG p 104/506 table 49: DDI port signal mapping to the HDMI connector.

mini DP ++ 2

for this Face Module. this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they belong to HDMI.

HDMI PORT 2

for this Face Module. this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in EB-TI22A Connector.

mini DP++ 1

see TL-PDG p 103/506 table 48: DDI: TCP Port Signal Mapping for HDMI connector.

for this Face Module. this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they belong to HDMI.

HDMI PORT 1

for this Face Module. this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in EB-TI22A Connector.

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12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] TX DDIB_TXN[3:0]	**Digital Display Interface Transmit:** DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P AUX DDIB_AUX_N	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

p.103/507 TL-TDG

Table 38. DisplayPort* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx) TX	DDIx_TXP/N[3:0]	N/A	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	N/A	2
Aux Channel AUX	DDIx_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

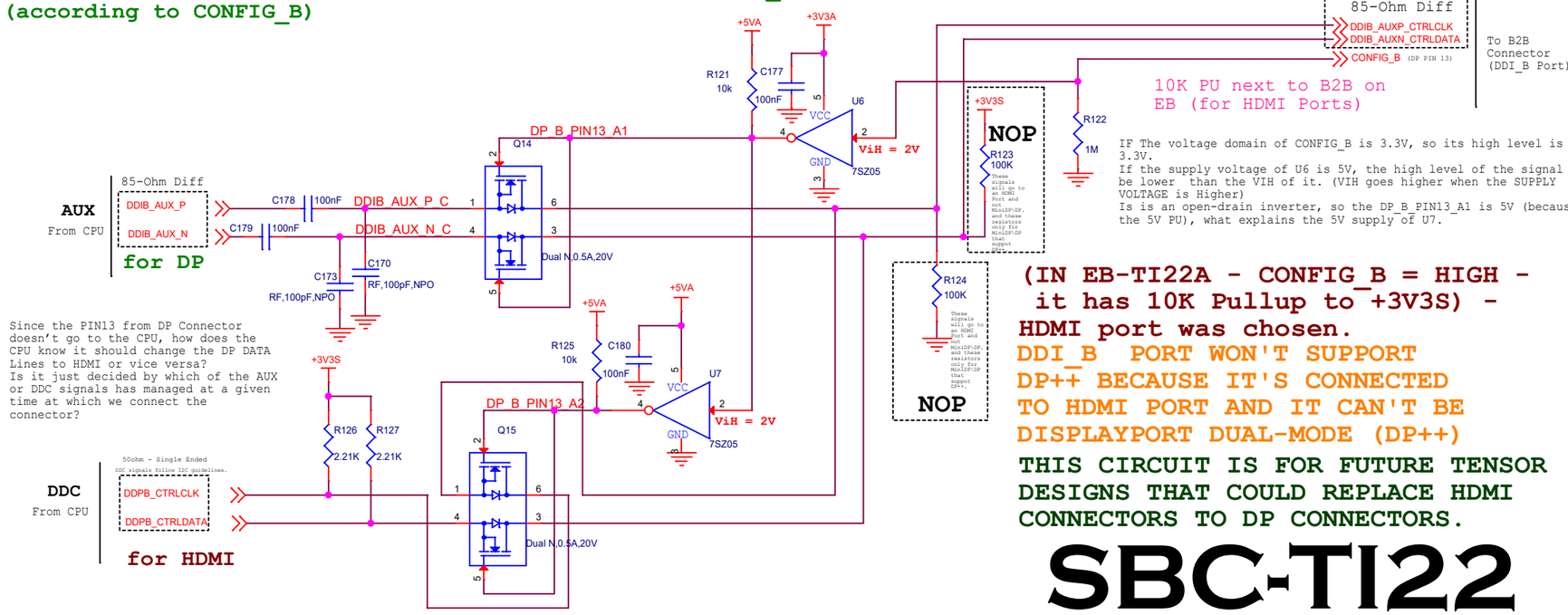
p.103/507 TL-TDG

Table 47. HDMI* Signals

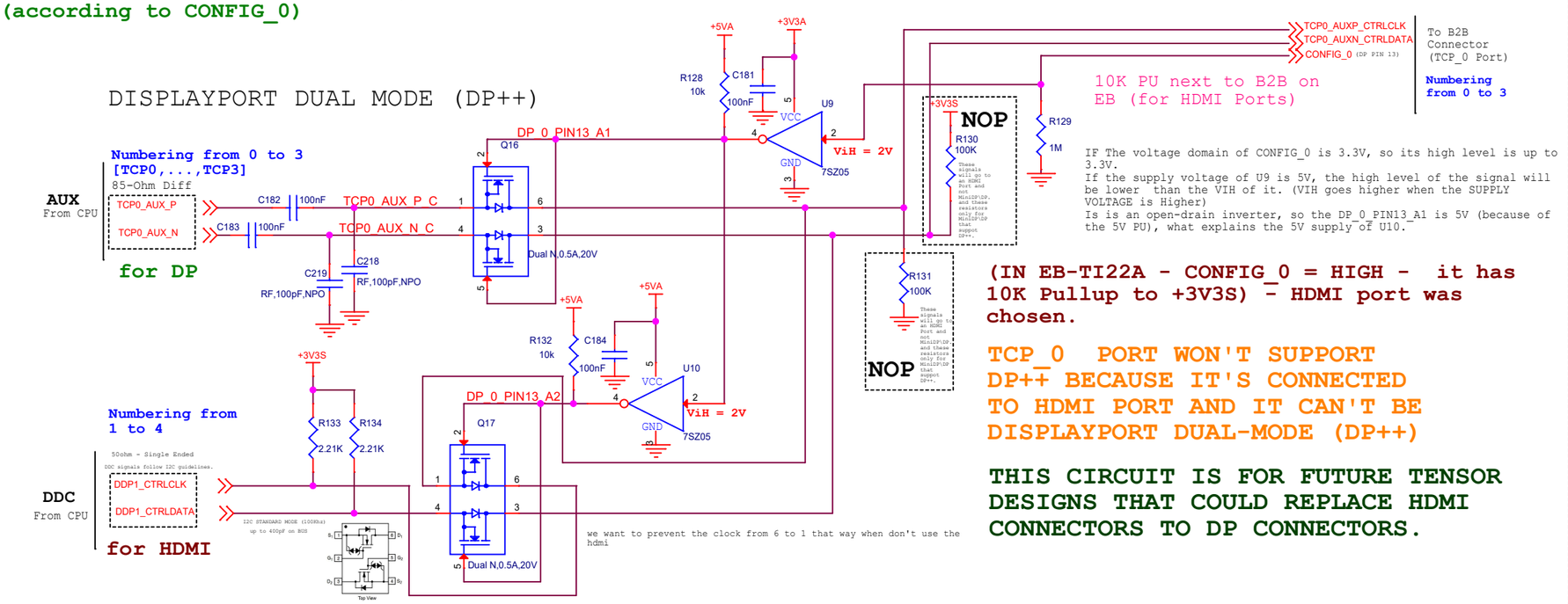
Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx) TX	DDIx_TXP/N[3:0]	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	2
DDC DDC	N/A	DDPx_CTRLCLK and DDPx_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

DP(AUXP, AUXN) or HDMI(CTRLCLK, CTRLDATA) select for DDI_B (according to CONFIG_B)



DP(AUXP, AUXN) or HDMI(CTRLCLK, CTRLDATA) select for TCP0 (according to CONFIG_0)



Title	<Title>	
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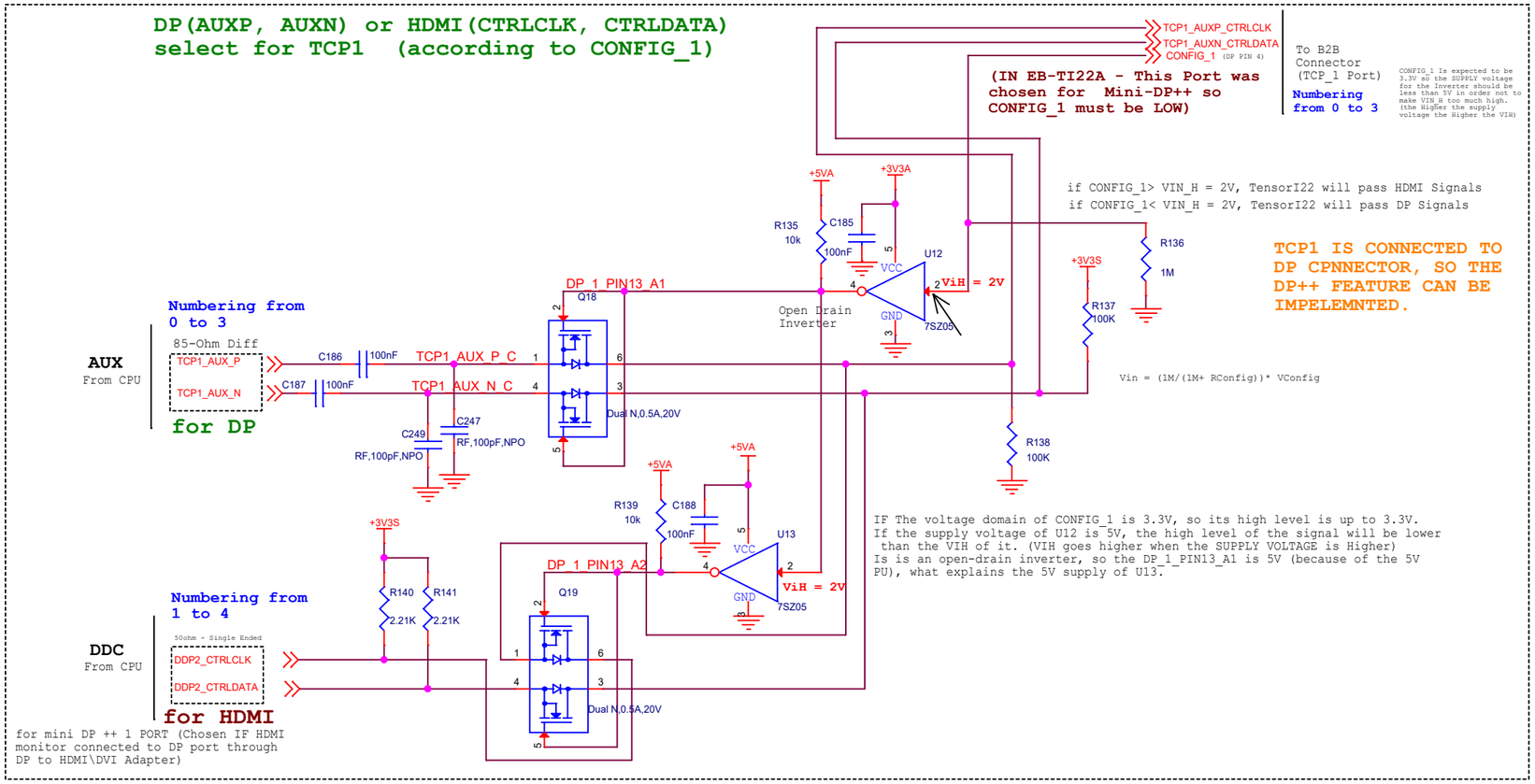

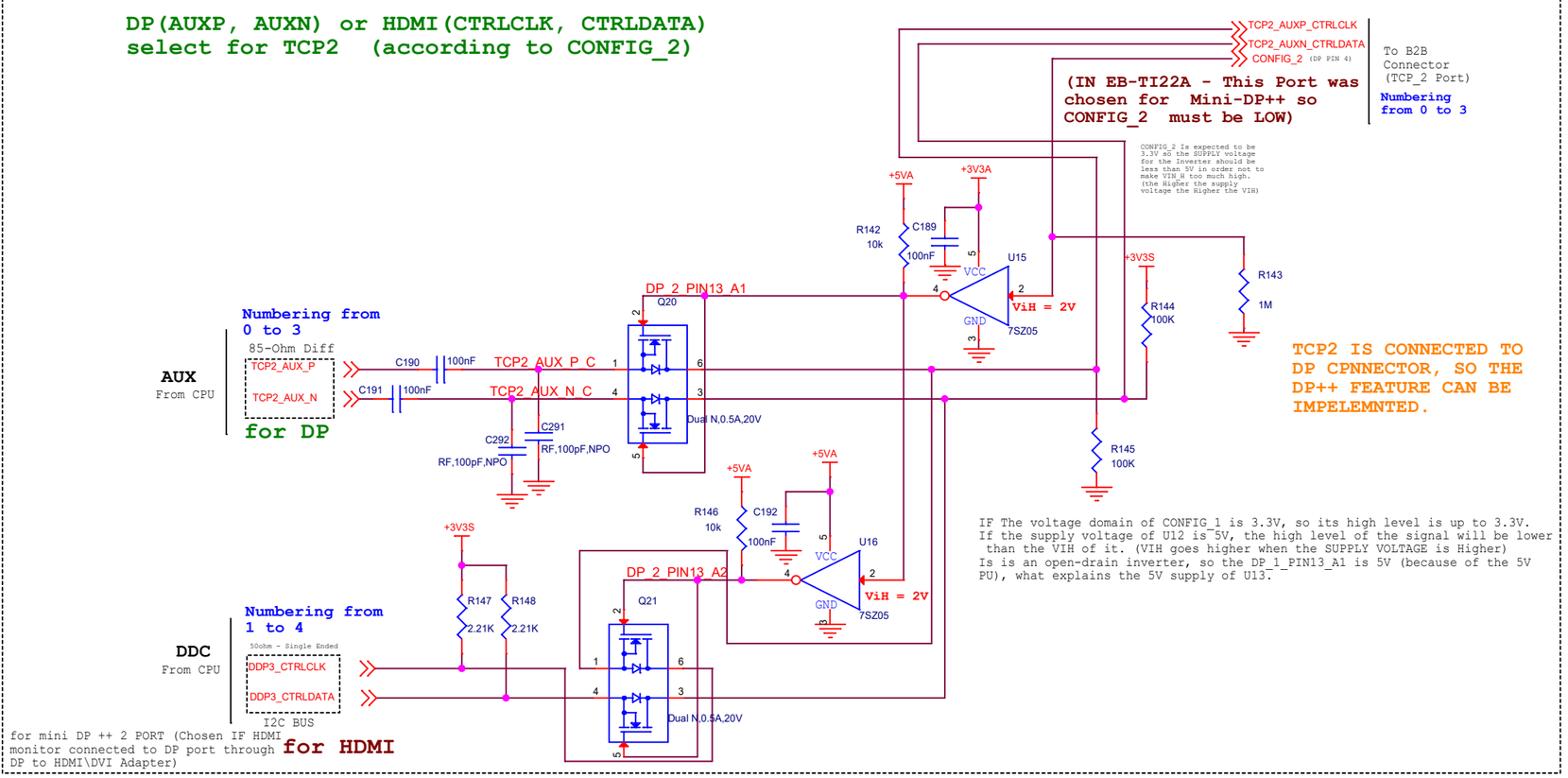

12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] DDIB_TXN[3:0] TX	**Digital Display Interface Transmit:** DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P DDIB_AUX_N AUX	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

Table 38. DisplayPort* Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx) TX	DDIx_TXP/N[3:0]	N/A	N/A	1
	TCPx_TX_P/N[1:0] and TCPx_TXRX_P/N[1:0]	N/A	N/A	2
Aux Channel AUX	DDIx_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_x	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:
1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

Table 47. HDMI* Signals

Description	Signal Mapping		Note
	Processor	PCH	
Main Link (Tx) TX	DDIx_TXP/N[3:0]	N/A	1
	TCPx_TX_P/N[0:1] and TCPx_TXRX_P/N[0:1]	N/A	2
DDC DDC	N/A	DDPx_CTRLCLK and DDPx_CTRLDATA	
Hot Plug Detect	N/A	DDSP_HPD_x	
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS, Provide good noise isolation, Rdc<0.2 Ohm		3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N		4

Note:
1. Signal names apply for DDI A/B ports.
2. Signal names apply for TCP ports.
3. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform Rdc<0.2 Ohm, require if any TCP implemented.

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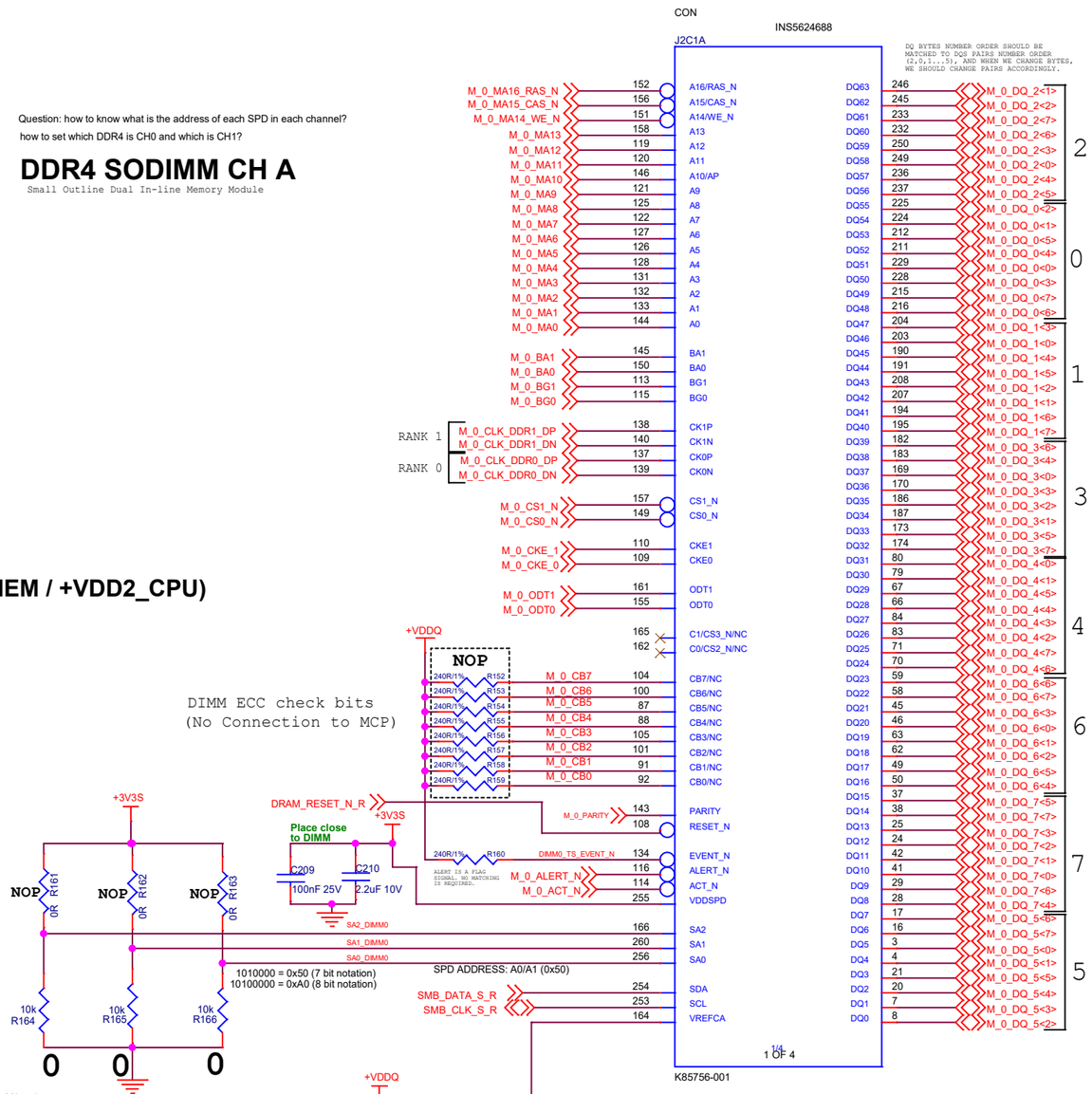
Memory, DDR4, SODIMM-260, 32GB, 2400MHz/2666MHz, 1.2V111L63202

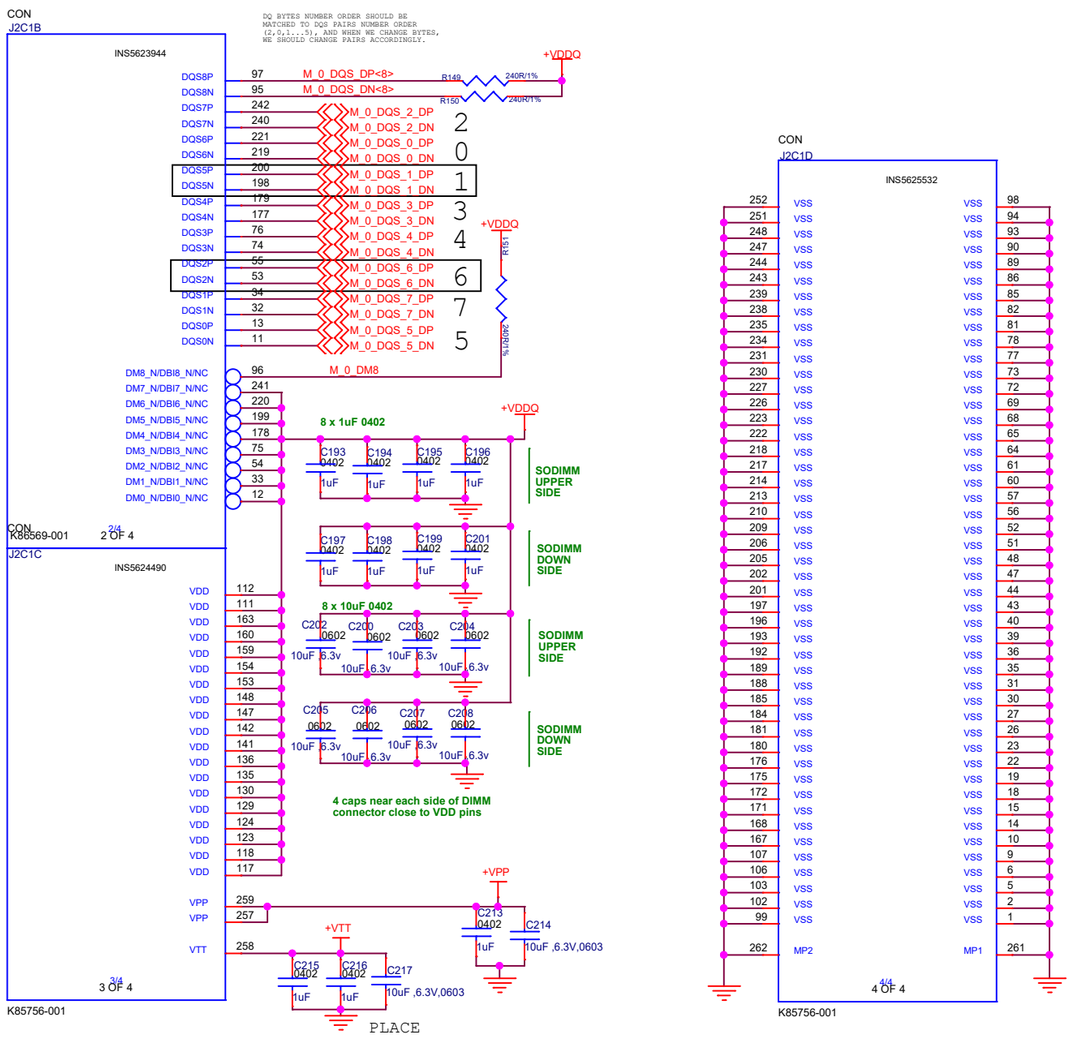
Question: how to know what is the address of each SPD in each channel?
how to set which DDR4 is CH0 and which is CH1?

DDR4 SODIMM CH A

Small Outline Dual In-line Memory Module

+VDDQ (+VDD2_MEM / +VDD2_CPU)





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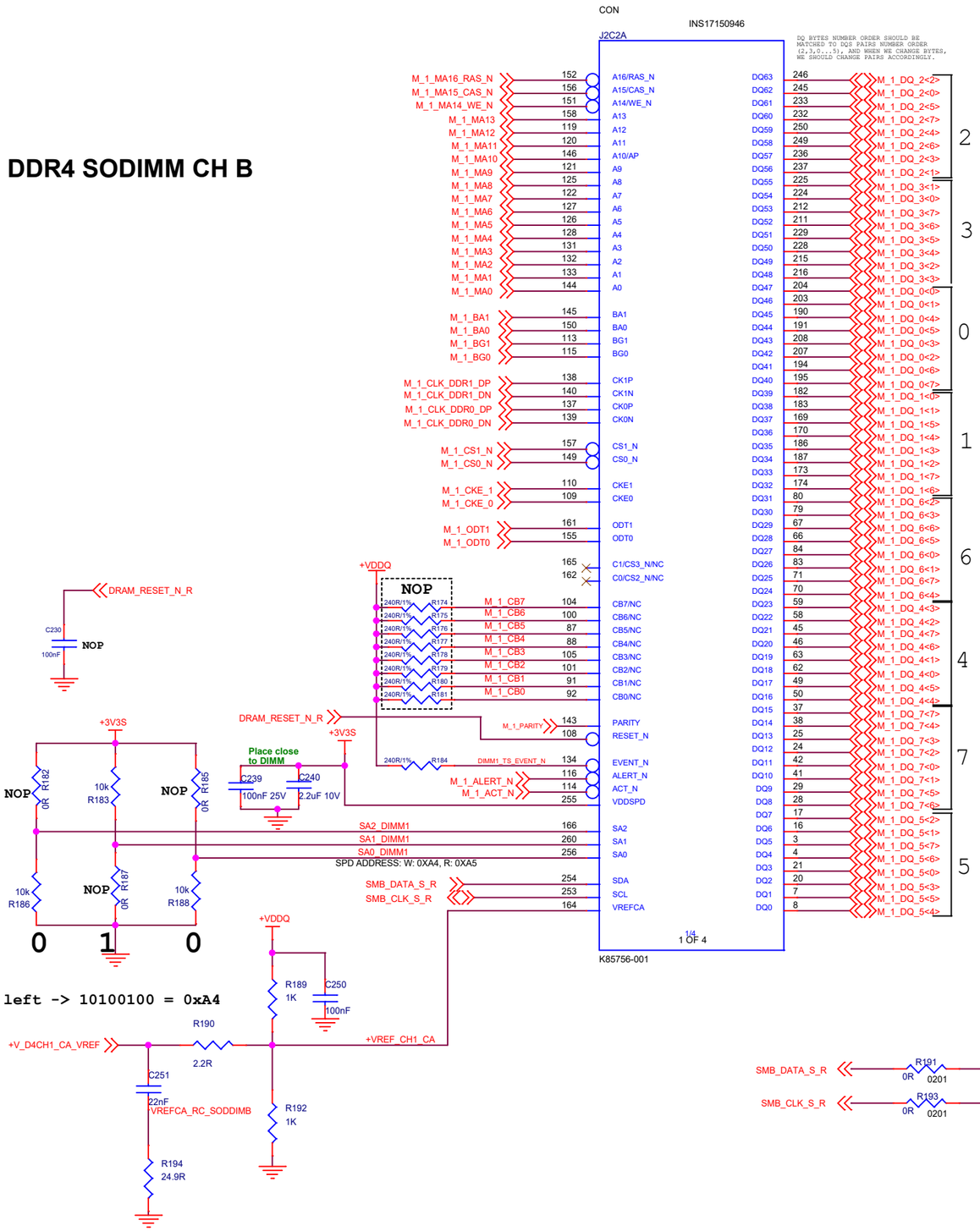
Memory, DDR4, SODIMM-260, 32GB, 2400MHz/2666MHz, 1.2V111L63202

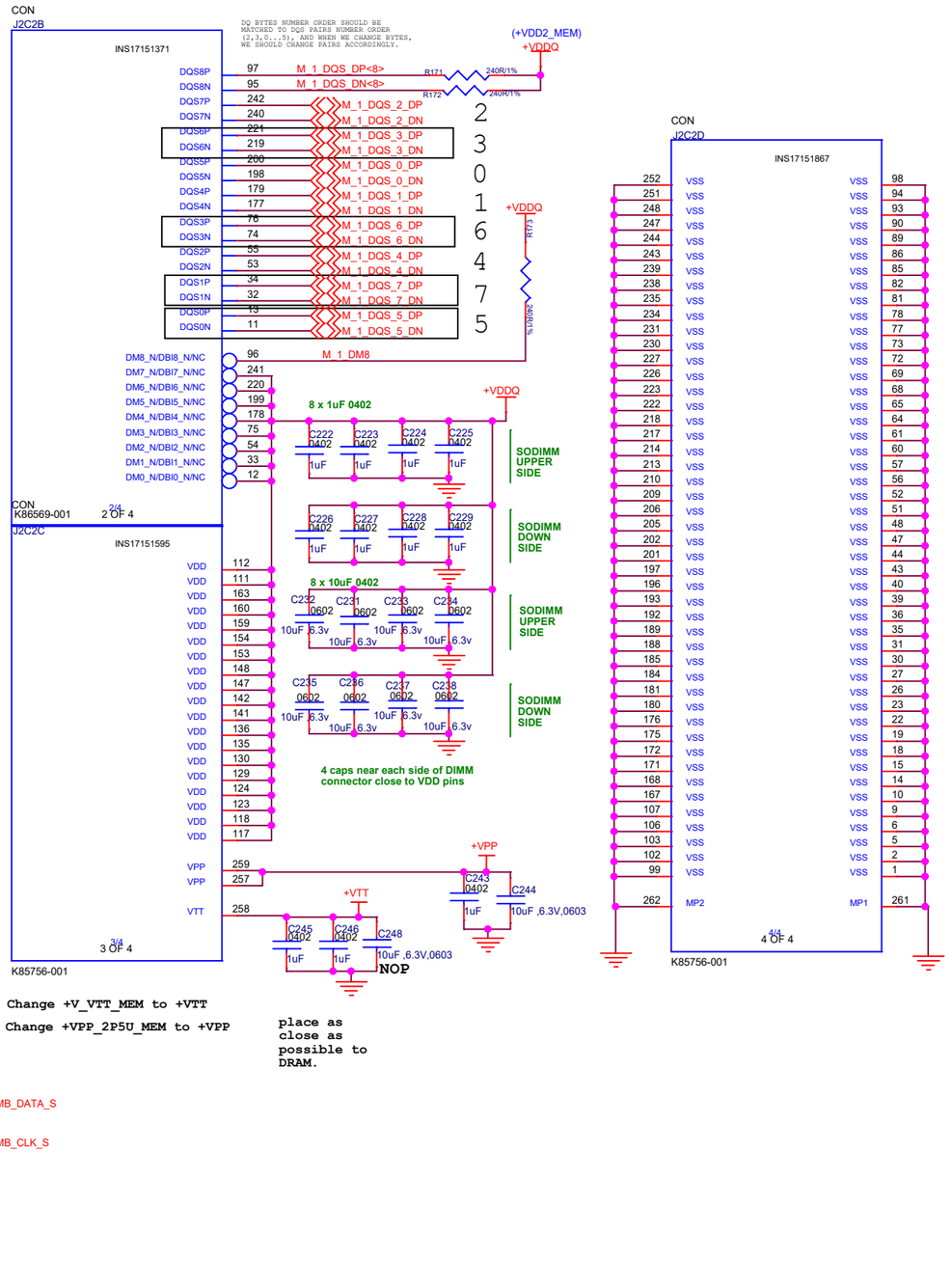
DDR4 SODIMM CH B



Memory, DDR4, SODIMM-260, 32GB, 2400MHz/2666MHz, 1.2V
P/N: 111L63202

Pin Location on SODDIMM:
259-13x2=233

1.CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.
2.DQ Bit swapping is allowed within the same byte
3.Byte Swapping is allowed within the same channel
4.DQSP and DQSN differential signal swapping within a pair is not allowed.



Title	<Title>	
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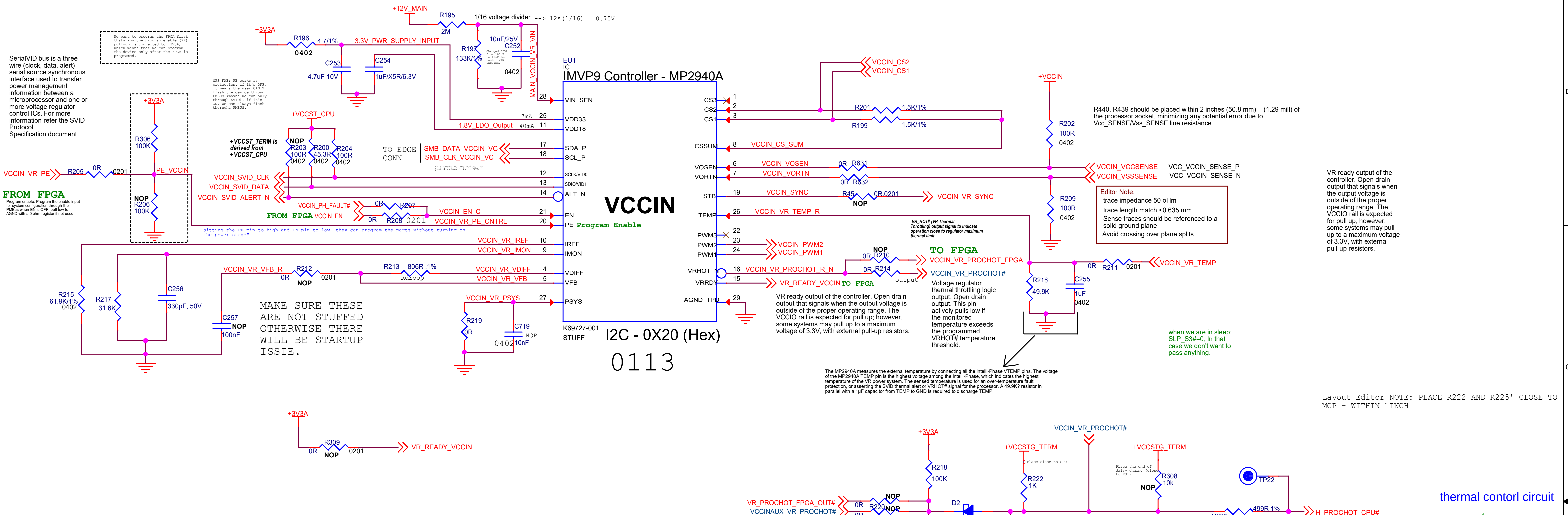
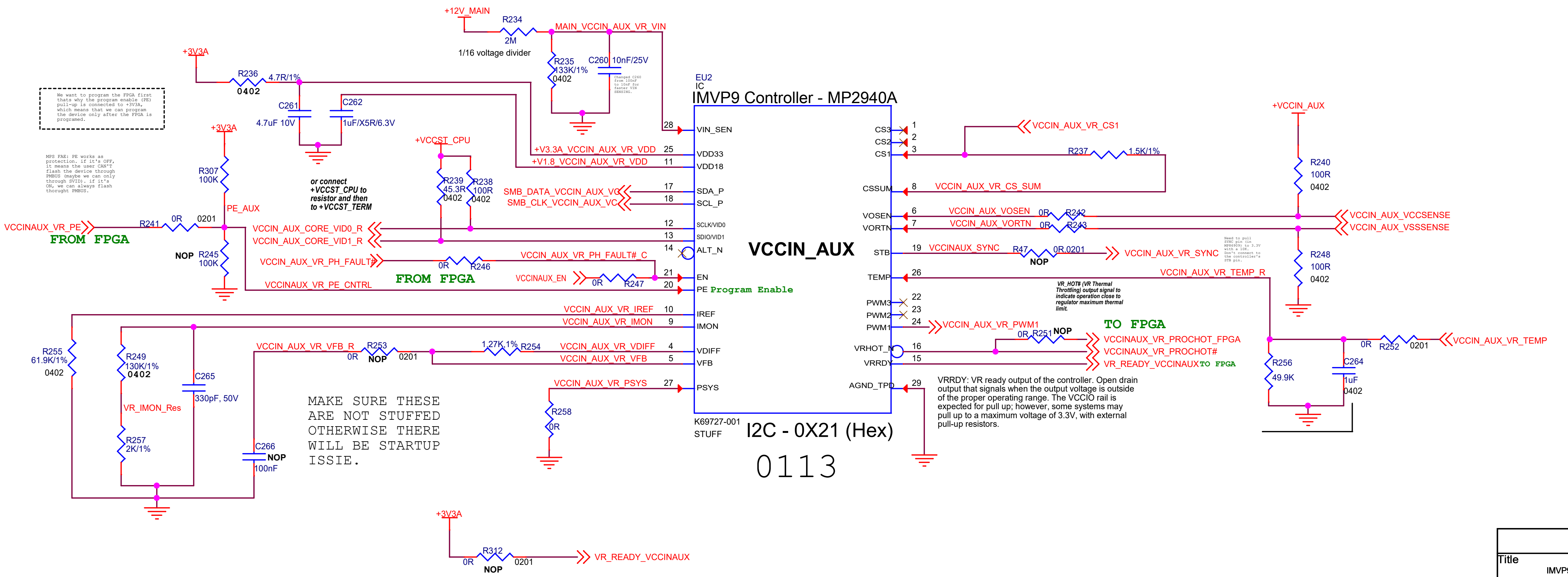
VCCIN RAIL POWER CONVERSION



VCCIN_AUX RAIL POWER CONVERSION



VID TABLE

VID 1	VID 2	Output Voltage	Usage
0	0	0V	Power Saving State
0	1	1.1V	Register
1	0	1.65V	Full Current, TGL-UP4
1	1	1.8V	Initial boot for TGL-UP3/UP4 Full current, TGL-UP3

Title: IMVP9 CTLR-VCCIN / VCCIN_AUX

Size: A3 | Document Number: <Doc> | Rev: <RevCode>

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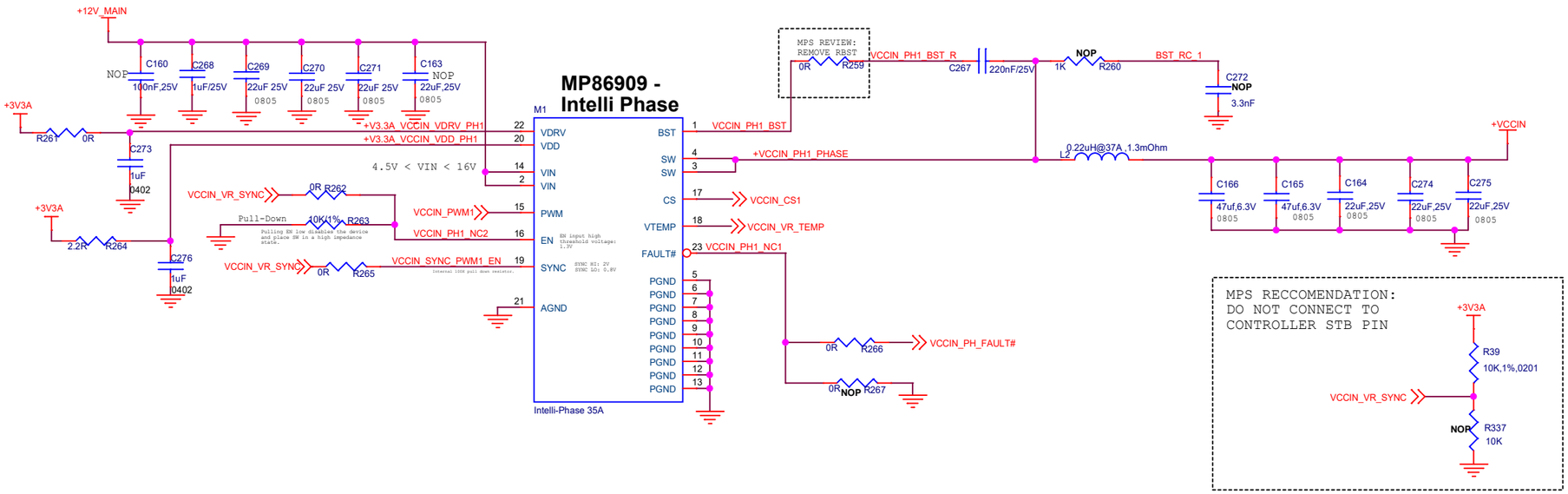
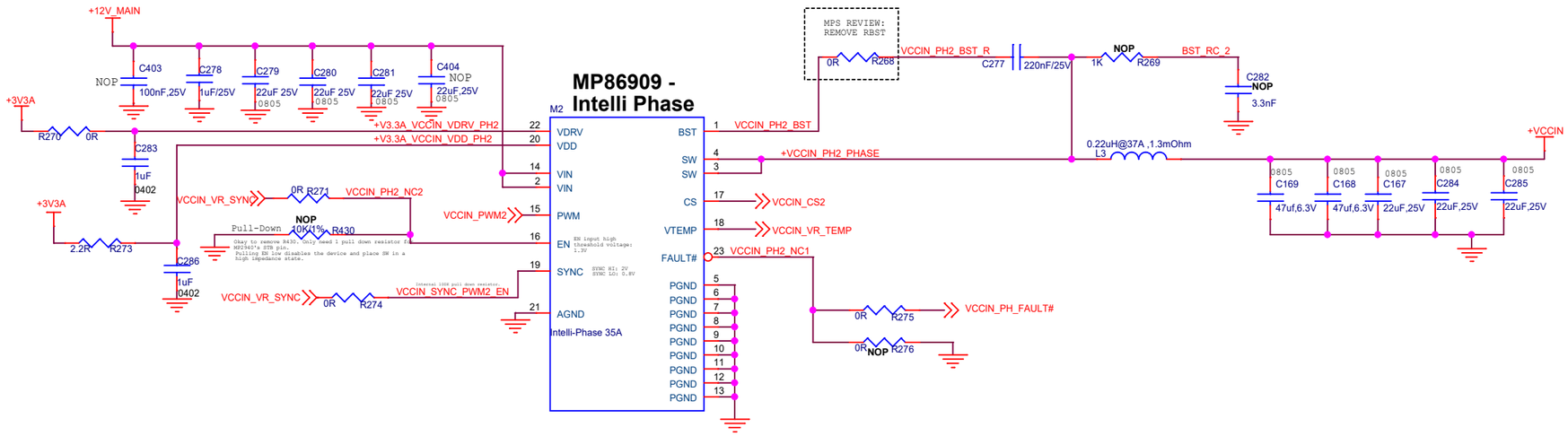


VCCIN POWER CONVERSION PHASE I



VCCIN POWER CONVERSION PHASE II

Title	PWR IMVP9- VCCIN PH1/PH2/PH3	
Size A3	Document Number <Doc>	Rev <RevCode>
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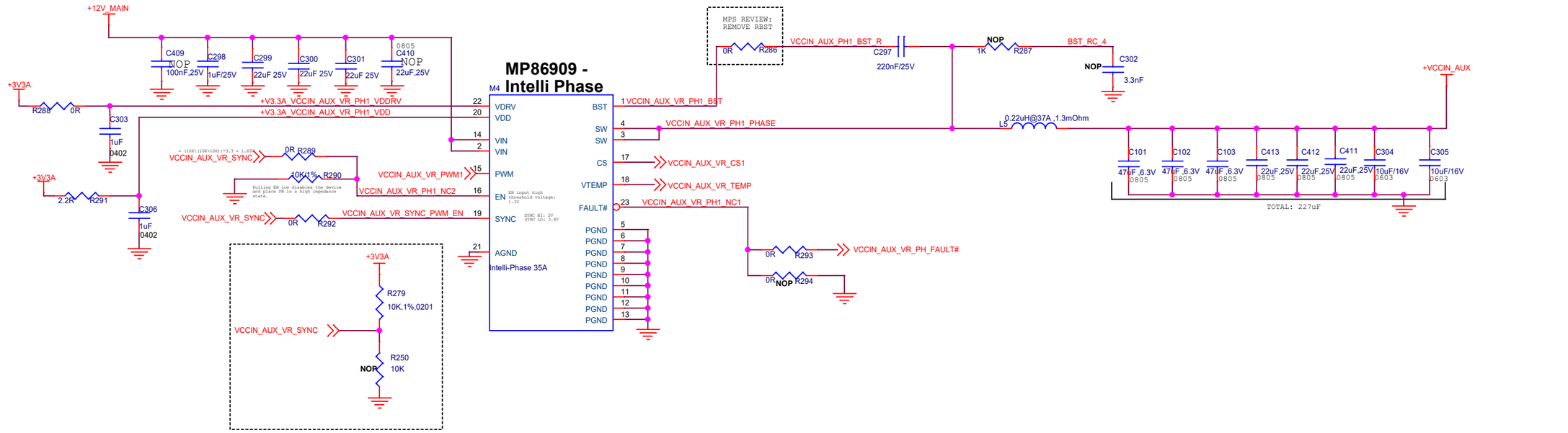
VCCIN_AUX POWER CONVERSION PHASE I



Title	PWR IMVP9- VCCIN_AUX PH1	
Size A3	Document Number <Doc>	Rev <RevCode>
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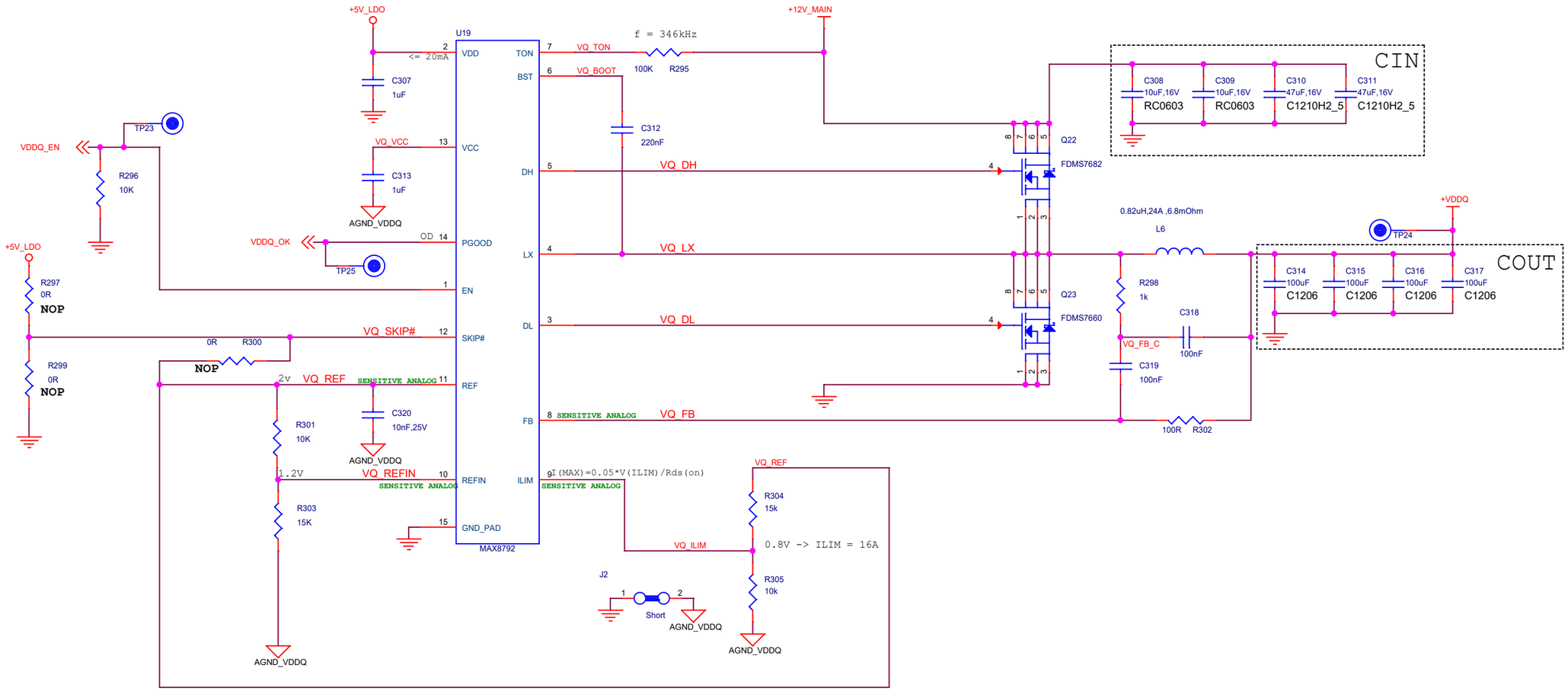
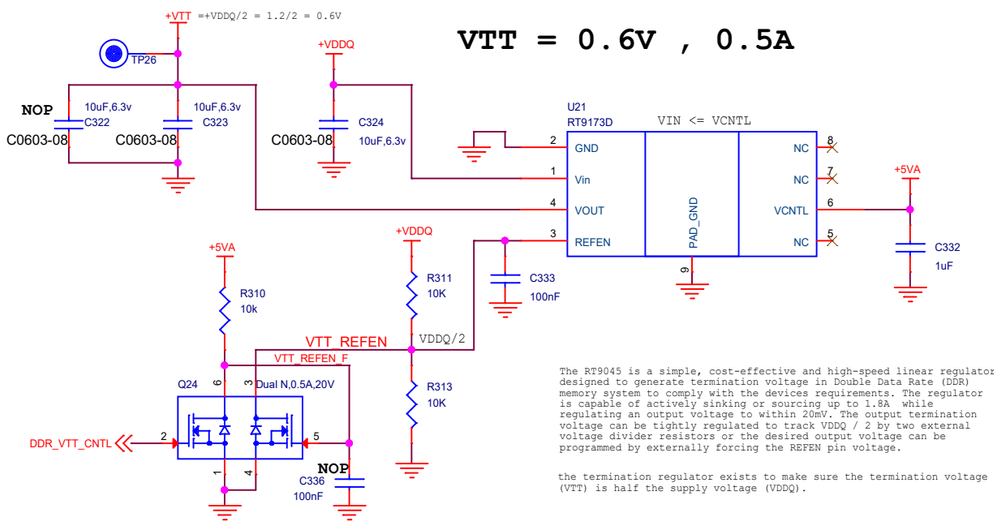
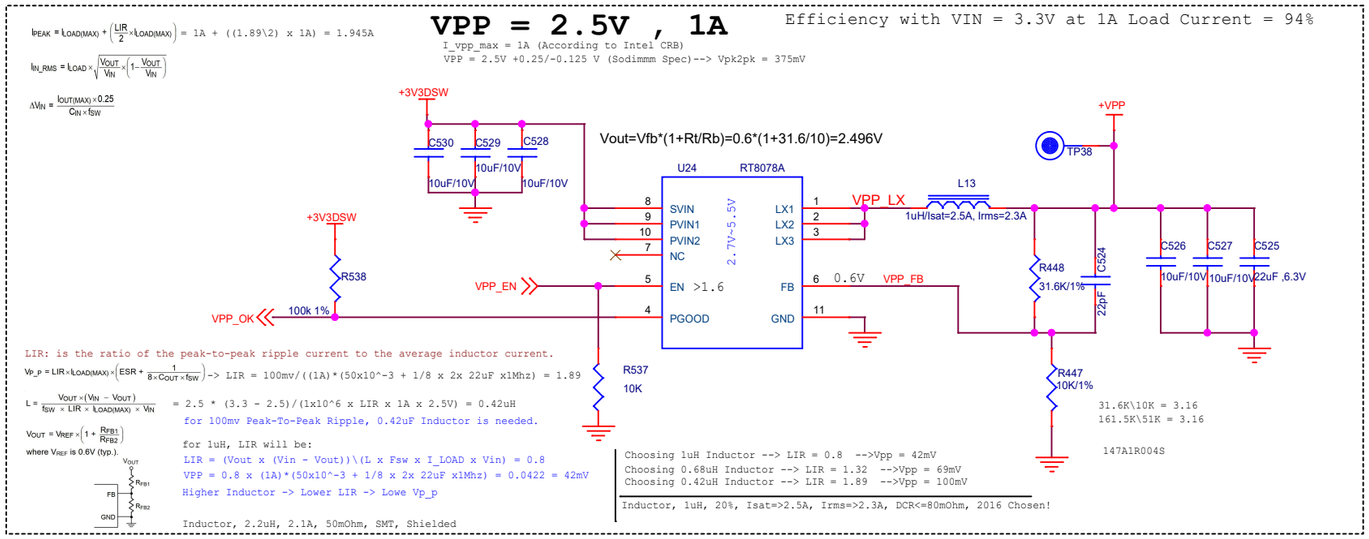
VDDQ = 1.2V , 15A







Title	PWR VDDQ/VTT/VPP	
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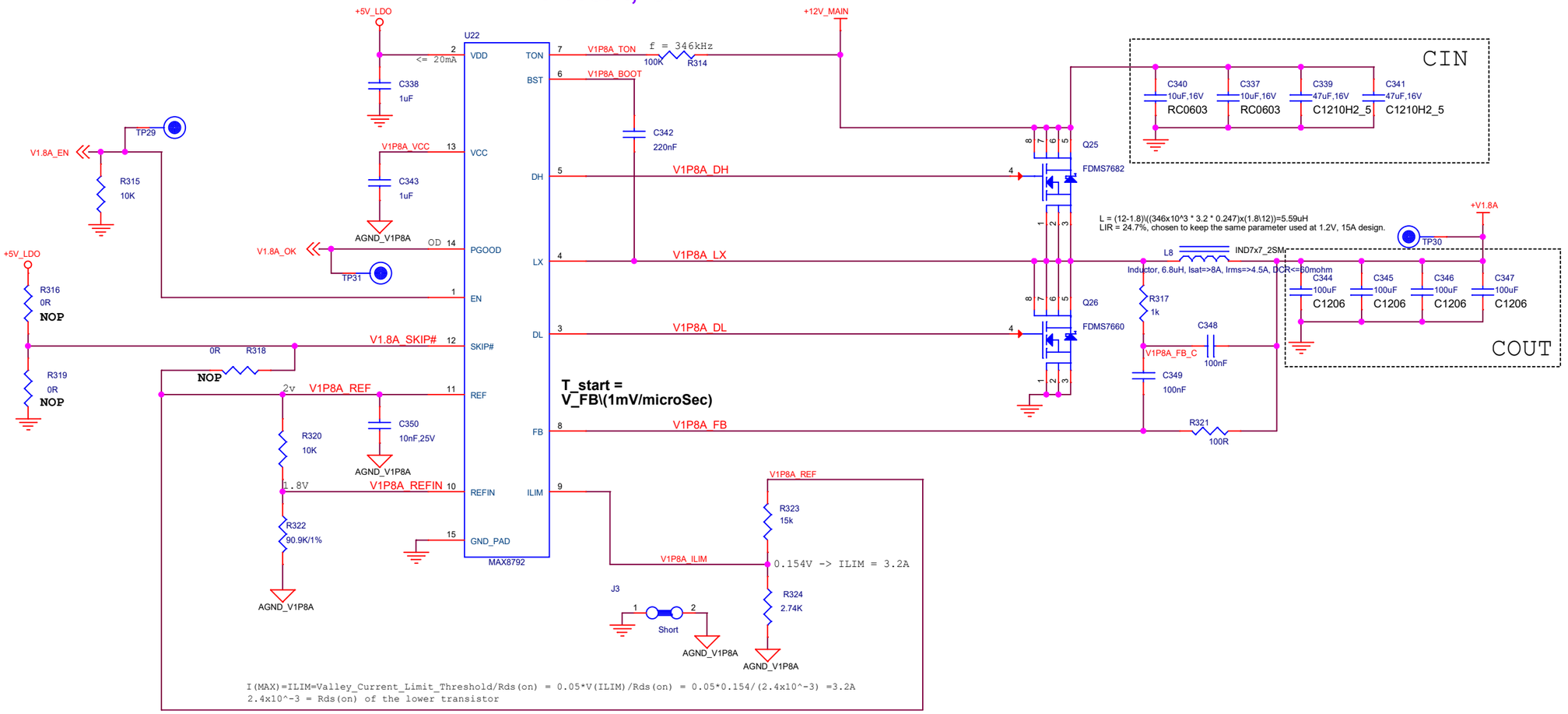
+V1.8A, 3A



I(MAX)=ILIM=Valley_Current_Limit_Threshold/Rds(on) = 0.05*V(ILIM)/Rds(on) = 0.05*0.154/(2.4x10^-3) =3.2A
2.4x10^-3 = Rds(on) of the lower transistor

Title	PWR +V1.8A	
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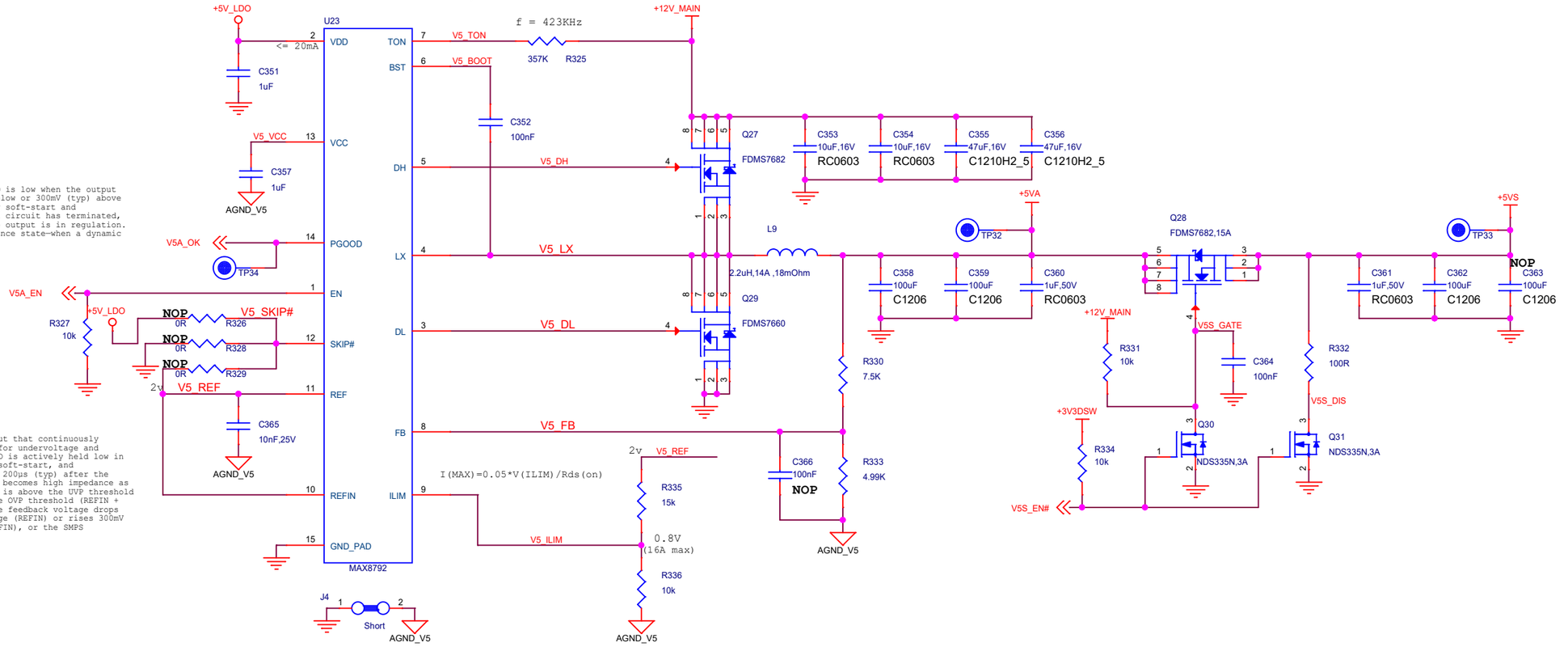
5V , 15A



Open-Drain Power-Good Output. PGOOD is low when the output voltage is more than 200mV (typ) below or 300mV (typ) above the target voltage (VREFIN), during soft-start and soft-shutdown. After the soft-start circuit has terminated, PGOOD becomes high impedance if the output is in regulation. PGOOD is blanked-forced high-impedance state-when a dynamic REFIN transition is detected.

PGOOD is the open-drain output that continuously monitors the output voltage for undervoltage and overvoltage conditions. PGOOD is actively held low in shutdown (EN = GND), during soft-start, and soft-shutdown. Approximately 200µs (typ) after the soft-start terminates, PGOOD becomes high impedance as long as the feedback voltage is above the UVP threshold (REFIN - 200mV) and below the OVP threshold (REFIN + 300mV). PGOOD goes low if the feedback voltage drops 200mV below the target voltage (REFIN) or rises 300mV above the target voltage (REFIN), or the SMPS controller is shut down.

+5VA Plane stitching capacitors

C135-C154 (see in Ver4.5)

Title	PWR 5V		
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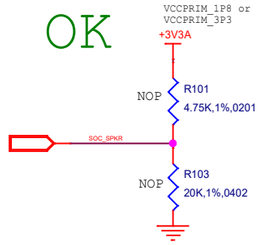
PCH STRAPS

TOP SWAP OVERRIDE

GPP_B14

OK



The strap has a 20 kohm ± 30% internal pull-down.

0=>Disable "Top Swap" mode. (Default)
1=>Enable "Top Swap" mode.

This inverts an address on access to SPI, so the processor fetches the alternate boot block instead of the original boot-block. PCH will invert the appropriate address lines (A[23:16]) as selected in Top Swap Block size soft strap.

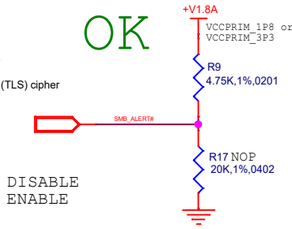
1. The internal pull-down is disabled after PCH_PWROK is high.
2. Software will not be able to clear the Top Swap (TS) bit (Bus0, Device31, Function0, offset DCh, bit 4) until the system is rebooted.
3. The status of this strap is readable using the Top Swap bit.
4. This signal is in the primary well.

Sampled at Rising edge of PCH_PWROK

TLS CONFIDENTIALITY

GPP_C5 / SML0ALERT#

OK



ME TLS Confidentiality Strap (PU)
This strap has a 20 kohm ± 30% internal pull-down.
0=>Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1=>Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

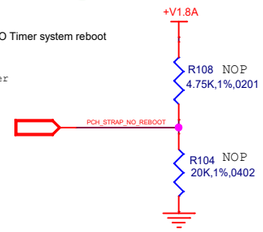
Native F1 if Intel SMBus ASD Mode Configuration soft strap = 1, else GP-Out; Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.

Sampled at Rising edge of RSMRST#

NO REBOOT

GPP_B18 / GSPI0_MOSI

OK



The strap has a 20 kohm ± 30% internal pull-down.
0=>Disable "No Reboot" mode. (Default)
1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

Notes:
1. The internal pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

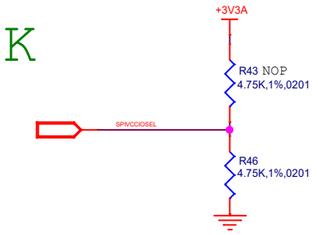
HIGH - NO REBOOT
LOW- REBOOT ENABLED
WEAK INTERNAL PD 20K

Sampled at Rising edge of PCH_PWROK

STRAP FOR SPI 1.8V/3.3V SELECTION

(NOT A GPIO)

OK



There is no internal pull-up or pull-down on the strap. An external resistor is required.
0 = SPI voltage is 3.3 V (4.7 kohm pull-down to GND)
1 = SPI voltage is 1.8 V (4.7 kohm pull-up to VCCDSW_3P3)

Not sampled. This strap must always be driven to a valid logic level

DDP3 I2C / TBT_LSX2 pins VCC configuration

GPP_D10 / ISH_SPI_CLK / DDP3_CTRLDATA / TBT_LSX2_RXD / BSSB_LS2_TX / GSPI2_CLK

OK

VCCPRIM_1P8 or
VCCPRIM_3P3

Already Has 100K PU (R144) to 3V3S at the DP++ HANDLING (Page 22)

This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 1.8 V
1 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 3.3 V

Strap read at rising edge of RSMRST#. External pull-up is required if signal used as HDMI Display I2C. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts

Sampled at Rising edge of RSMRST#

SPI0_IO2 STRAP - RSVD

PU PLACED NEXT TO SPI FLASH (U26)

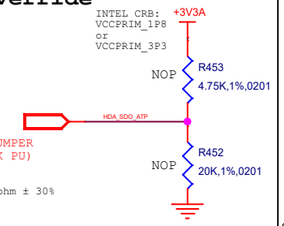
SPI0_IO3 STRAP - RSVD

PU PLACED NEXT TO SPI FLASH (U26)

Flash Descriptor Security Override

GPP_R2 / HDA_SDO / I2S0_TXD STRAP

OK



HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN

WEAK INTERNAL PD 20K

THIS SIGNAL IS TIED TO A JUMPER ON ATP CARD (IF JUMPER INSIDE HDA_SDO_ATP IS PULLED TO +V3VDSW THROUGH 1K PU)

Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% pull-down is disabled after PCH_PWROK is high.

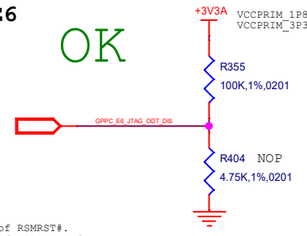
To support Intel® ME, a SPI flash is required on the platform with sufficient space to hold system BIOS, Intel® ME firmware, Intel® Integrated Sensor Solution firmware and any additional third party data storage. The SPI flash needs to be powered in states S0 through S5, independent of Intel® ME power state.
GPP_R2 / HDA_SDO / I2S0_TXD signal is used for Flash Descriptor Security Override (which is also known as Intel® ME Debug Mode). This signal input should be tied to a jumper which connects to power through an external pull-up (1 KΩ ±5%) only. When this signal is asserted, the Flash Security gets overridden for ease of image programming.

Sampled at Rising edge of PCH_PWROK

JTAG ODT DISABLE - GPP_E6

GPP_E6 / THC0_SPI1_RST#

OK



This strap does not have an internal pull-up or pull-down. External pull-up is recommended
0=> JTAG ODT is disabled
1=> JTAG ODT is enabled

CAD NOTE:

Strap read at rising edge of RSMRST#. External pull-up is required. Recommend 100 kohm. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

PLACE R355 AND R404 CLOSE TO THE SPI SIGNAL TO AVOID STUB

USB_OC_CD#

OK

10K PU at EB-TI22A

GPP_E10 / THC0_SPI1_CS#

OK

THC0_SPI1 Chip Select: Used to select the touch devices if it is connected to THC0_SPI1 interface.

THC NOT USED IN TENSOR-I22

CAD NOTE:

PLACE R414,R415 AND R422 CLOSE TO THE SPI SIGNAL TO AVOID STUB

GPP_E11 / THC0_SPI1_CLK

OK

THC0_SPI1 Clock: THC0 SPI1 clock output from PCH. Supports 20 MHz, 33 MHz and 50 MHz.

THC NOT USED IN TENSOR-I22

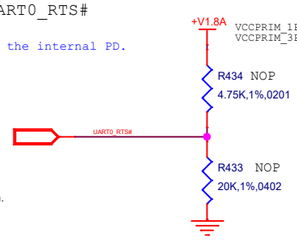
CAD NOTE:

PLACE R429,R430 AND R431 CLOSE TO THE SPI SIGNAL TO AVOID STUB

XTAL Frequency Selection

GPP_F0 / CNV_BRI_DT / UART0_RTS#

OK



GPP_F0 Pin is at 0 (38.4 Mhz) by the internal PD.

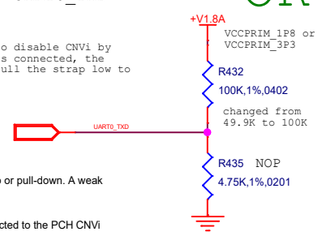
This strap has a 20 kohm ± 30% internal pull-down.
0 = 38.4 MHz (default)
1 = 24 MHz
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

M.2 CNVi Mode Select

GPP_F2 / CNV_RGI_DT / UART0_TXD

OK



A weak external PU is required to disable CNVi by default. When a companion chip is connected, the required PD on the device will pull the strap low to enable CNVi.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.
0= Integrated CNVi enabled.
1= Integrated CNVi disabled.
Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

Sampled at Rising edge of RSMRST#

USB_OC_AB#

OK

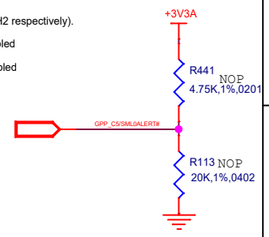
10K PU at EB-TI22A

BOOT STRAP - BIT 0

OK

This strap has a 20 kohm ± 30% internal pull-down.
This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration.
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).
4-bit boot strap configuration encodings:
0000 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is enabled

0010 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / Intel CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; Intel CSME on slave attached SPI.
Others: Reserved
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

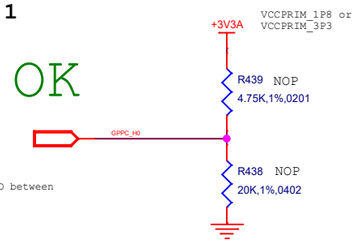


Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.

BOOT STRAP - BIT 1

GPP_H0

OK



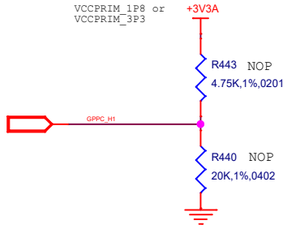
used for M2 PCH SSD RTD3, using AND between BUF_PLTRST# and GPPC_H0

Check TL-SBC (44/270)

BOOT STRAP - BIT 2

GPP_H1

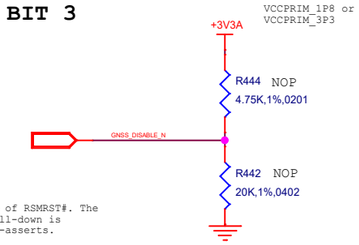
OK



BOOT STRAP - BIT 3

GPP_H2

OK



Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.

Title	PCH STRAPS (1 OF 2)	
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PCH STRAPS

DDP1 I2C / TBT_LSX0 pins VCC configuration

GPP_E19 / DDP1_CTRLDATA / TBT_LSX0_RXD / BSSB_LS0_TX

VCCPRIM_1P8 or VCCPRIM_3P3

OK

Already Has 100K PU (R130) to 3V3S at the DP++ HANDLING (Page 21)

This strap has a 20 kohm ± 30% internal pull-down.
0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8 V
1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

there is 2.2K PU on DPP1_CTRLDATA

Sampled at Rising edge of RSMRST#

DDP2 I2C / TBT_LSX1 pins VCC configuration

GPP_E21 / DDP2_CTRLDATA / TBT_LSX1_RXD / BSSB_LS1_TX

NOTE: BSSB - Boundary Scan Sideband Low Speed Receive 1 for debug purposes

HIGH: 3.3V
LOW: 1.8V

OK

Already Has 100K PU (R137) to 3V3S at the DP++ HANDLING (Page 22)

LSx Interface:
The PCH LSx interface enables communication between one thunderbolt controller to another. TGL UP3/UP4 supports 4 pairs of LSx signals. The LSx signals use a UART interface. It operates at a 1 MHz baud rate and shares identical electrical characteristics/routing guidelines as UART.

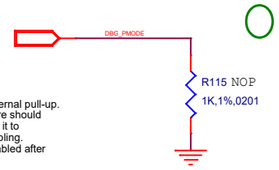
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 1.8 V
1 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

DBG_PMODE

RESERVED

OK



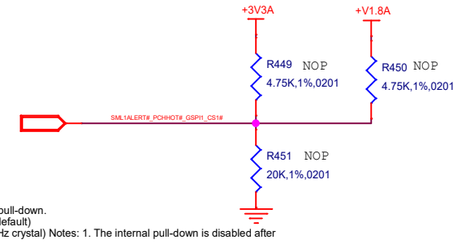
This strap has a 20 kohm ± 30% internal pull-up.
This strap should sample high. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-up is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

CPUNSSC CLOCK FREQ

GPP_B23 / SML1ALERT# / PCHHOT# / GSPI1_CS1#

OK



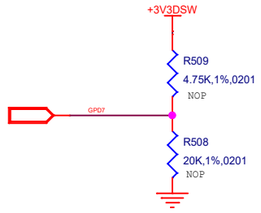
This strap has a 20 kohm ± 30% internal pull-down.
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal) Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150 kohm pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.

GPD7

STRAP: RESERVED

Strap read at rising edge of DSW_PWROK. The internal pull-down 20 kohm ± 30% is disabled after DSW_PWROK is high . This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

OK



GPP_F10

STRAP: RESERVED

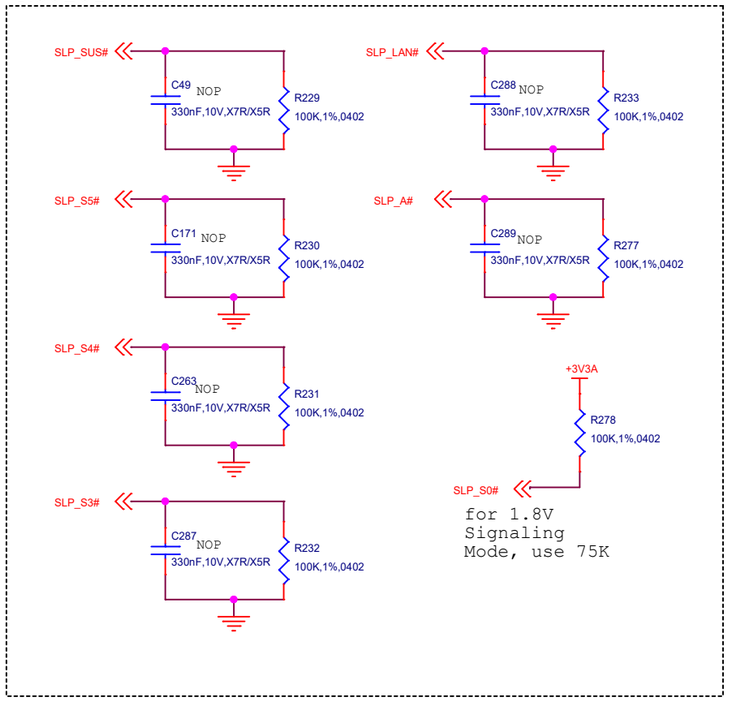
This strap has a 20 kohm ± 30% internal pull-down.
This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

OK

Sampled at Rising edge of RSMRST#

PCH GLITCH ISSUE MITIGATION

RC0201



Title: PCH STRAPS (2 OF 2)		
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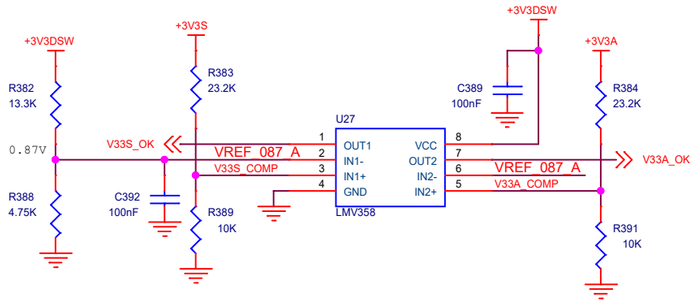
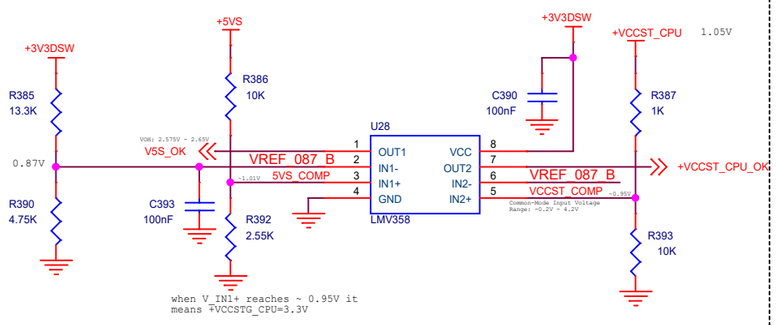
+3V3S,+3V3A PWRGD

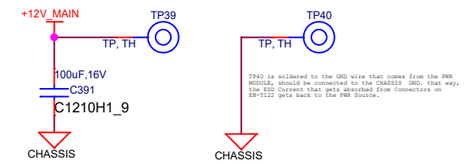


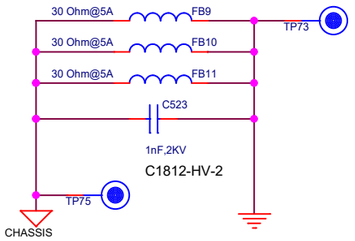
+5VS, VCCST_CPU PWRGD



POWER MODULE CONNECTION - 12V

Hanging 1x2 connector





Title: 3V3S\3V3A\VCCCST PWRGD		
Size: A3	Document Number: <Doc>	Rev: <RevCo
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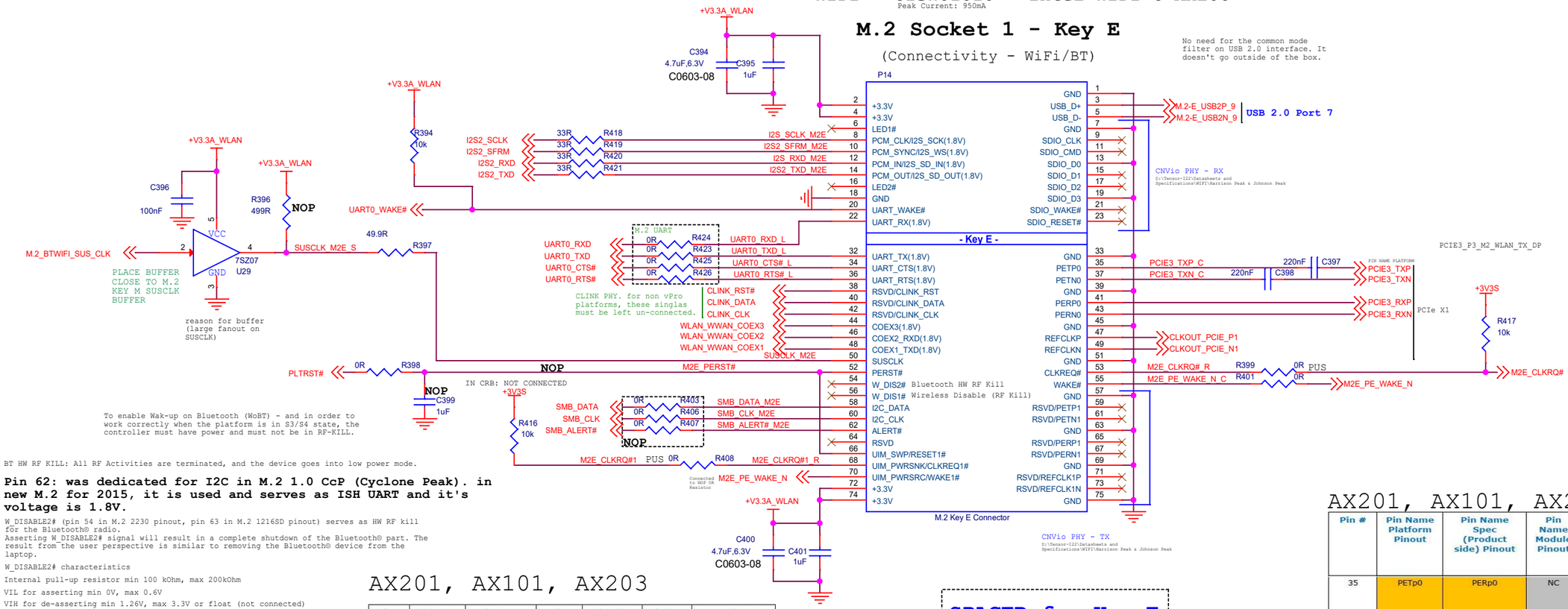
WIFI - 613W01010 - Intel WIFI 6 AX200

Peak Current: 950mA

M.2 Socket 1 - Key E

(Connectivity - WiFi/BT)



BT HW RF KILL: All RF Activities are terminated, and the device goes into low power mode.

Pin 62: was dedicated for I2C in M.2 1.0 CcP (Cyclone Peak). in new M.2 for 2015, it is used and serves as ISH UART and it's voltage is 1.8V.

W_DISABLE2# (pin 54 in M.2 2230 pinout, pin 63 in M.2 1216SD pinout) serves as HW RF kill for the Bluetooth® radio.
Asserting W_DISABLE2# signal will result in a complete shutdown of the Bluetooth® part. The result from the user perspective is similar to removing the Bluetooth® device from the laptop.

W_DISABLE2# characteristics

Internal pull-up resistor min 100 kOhm, max 200kOhm

VIL for asserting min 0V, max 0.6V

VIH for de-asserting min 1.26V, max 3.3V or float (not connected)

The recommendation is to use HW RF kill functionality by using a GPIO pin provided by the ACPI to turn on/off the radio of the Bluetooth® device.
BIOS shall implement ACPI function for HW RF-Kill implementation in the OS.
For more information, please refer to Intel document 559910, Intel Connectivity Platform BIOS Guidelines, Section 3.1.5.6, "BT RTD3 control."

AX201, AX101, AX203

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP/HrP/ JnP2 Module	JfP/HrP /JnP2 Voltage on Module Side	Connection on Platform/Usage
20	UART WAKE#	UART WAKE#	NC	O	3.3 V	Not used by Harrison Peak Optional UART interface when used with Discrete
21	WGR_CLKN	SDIO_WAKE#	WGR_ CLKN	O	CNVio PHY	CNVio bus Rx clock
22	UART TXD/BRI_RSP (fixed: UART RXD on Platform)	UART TXD	BRI_RSP	O	1.8 V	BRI bus RX Optional PCM interface when used with Discrete
23	WGR_CLKP	SDIO_RESET#	WGR_ CLKP	O	CNVio PHY	CNVio bus Rx clock
24	Connector Key	Connector Key	Module Key			
25	Connector Key	Connector Key	Module Key			
26	Connector Key	Connector Key	Module Key			
27	Connector Key	Connector Key	Module Key			
28	Connector Key	Connector Key	Module Key			
29	Connector Key	Connector Key	Module Key			
30	Connector Key	Connector Key	Module Key			
31	Connector Key	Connector Key	Module Key			
32	UART TXD/RGI_DT	UART RXD	RGI_DT	I	1.8 V	RGI bus TX, 1.8v-PU in CRF Optional PCM interface when used with Discrete
33	GND	GND	GND			
34	UART CTS/RGI_RSP	UART RTS	RGI_RSP	O	1.8 V	RGI bus RX Optional PCM interface when used with Discrete
36	UART RTS/BRI_DT	UART CTS	BRI_DT	I	1.8 V	BRI bus TX

SPACER for Key-E

J9 NC

M3 Spacer SMT 2.5mm

AX201, AX101, AX203

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP/HrP/ JnP2 Module	JfP/HrP /JnP2 Voltage on Module Side	Connection on Platform/Usage
35	PETp0	PERp0	NC		PCIe* PHY	Not used by Harrison Peak Shall be connected to PCIe* for Discrete support PCIe* PHY signals
36	UART RTS/BRI_DT	UART CTS	BRI_DT	I	1.8 V	BRI bus TX
37	PETn0	PERn0	NC		PCIe* PHY	Not used by Harrison Peak Shall be connected to PCIe* for Discrete support PCIe* PHY signals
38	CLINK RESET	<Vendor Defined> CLINK RESET	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
39	GND	GND	GND			
40	CLINK DATA	<Vendor Defined> CLINK DATA	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
41	PERp0	PETp0	NC		PCIe* PHY	Not used by Harrison Peak Shall be connected to PCIe* for Discrete support PCIe* PHY signals
42	CLINK CLK	<Vendor Defined> CLINK CLK	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
43	PERn0	PETn0	NC		PCIe* PHY	Not used by Harrison Peak Shall be connected to PCIe* for Discrete support PCIe* PHY signals

Title: M.2 E (WiFi/BT)

Size: A3 | Document Number: <Doc> | Rev: <RevCo

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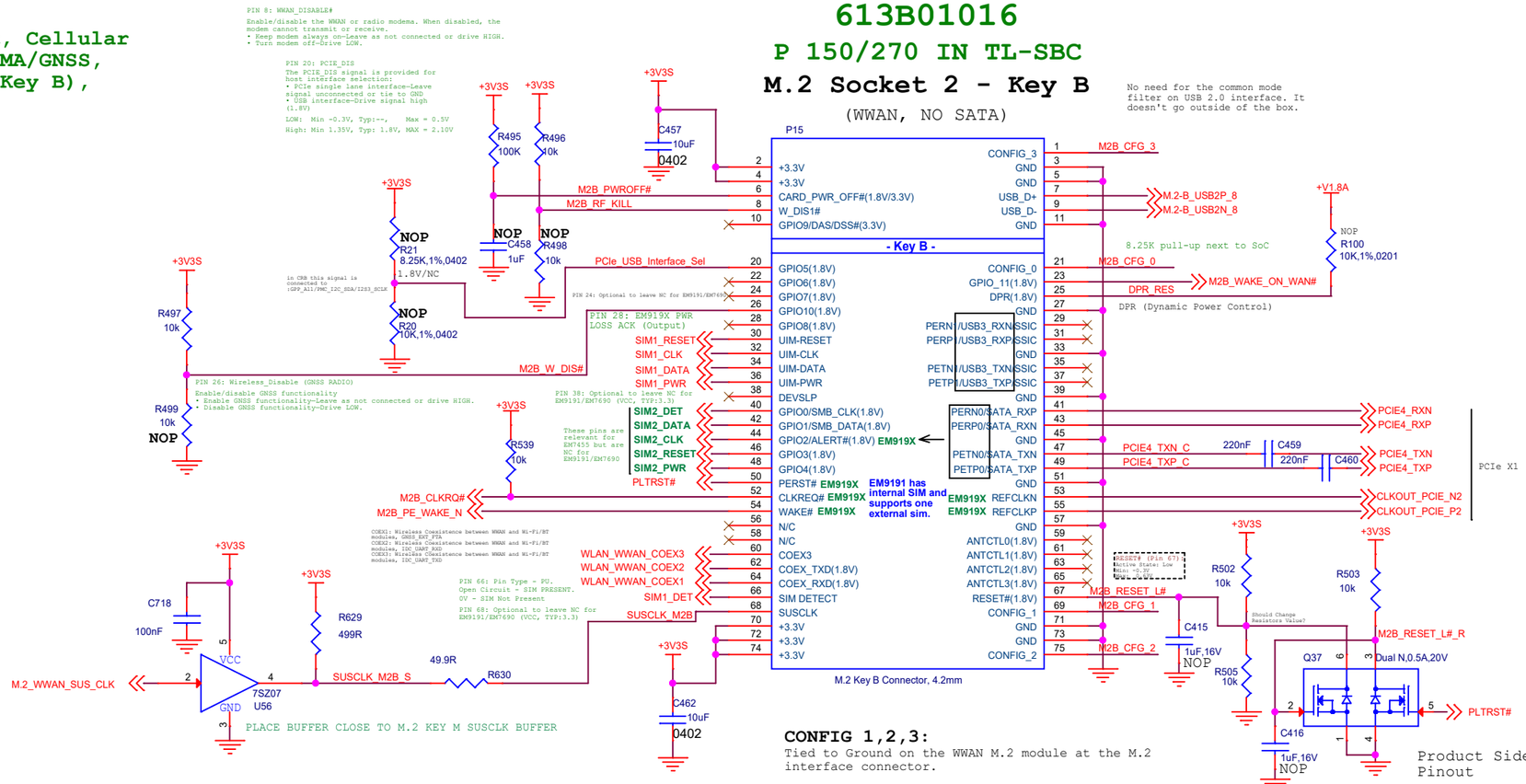
Communication Equipment, Cellular Modem, 5G/LTE/HSPA+/WCDMA/GNSS, Global-Band, M.2 3052 (Key B), Sierra EM9191

613B01016

P 150/270 IN TL-SBC

M.2 Socket 2 - Key B

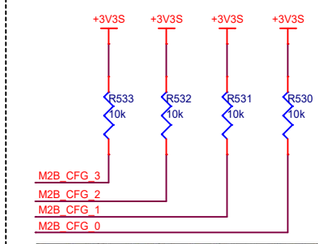
(WWAN, NO SATA)



CONFIG 1,2,3:
Tied to Ground on the WWAN M.2 module at the M.2 interface connector.

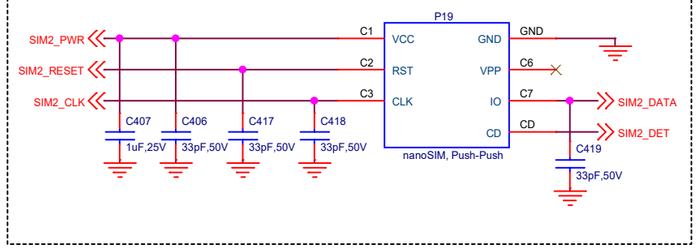
CONFIG 0:
This signal is not connected on the WWAN M.2 module.

M.2 CONFIG PINS

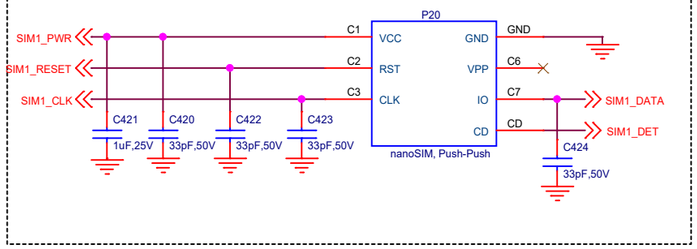


Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module type and main host interface
GND	GND	GND	GND	SSD-SATA
GND	NC	GND	GND	SSD-PCIe
NC	GND	GND	GND	WWAN-SSIC
NC	NC	NC	NC	No Module Present

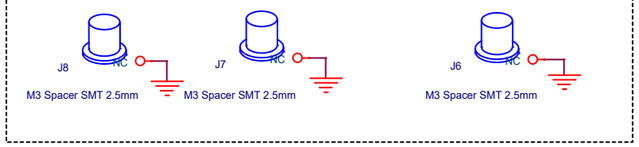
nanoSIM_2 with detect (w/o tray)



nanoSIM_1 with detect (w/o tray)



Spacers for Key-B & Key-M Heatsink



Product Side Pinout

EM919X

Table 3-1: Host Interface (75-pin) Connections—Module View (Continued)

Pin	Signal name	Pin type[a]	Description	Direction[b]	Active state	Voltage levels (V)		
						Min	Typ	Max
41	PCIE_TXM0		PCIe Negative Transmit Data	Output	Differential	–	–	–
42	QTM1_PON[d]	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	–	1.8
					Low	0	–	0.45
43	PCIE_TXP0		PCIe Positive Transmit Data0	Output	Differential	–	–	–
44	QTM2_PON[d]	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	–	1.8
					Low	0	–	0.45
45	GND	V	Ground	Input	Power	–	0	–
46	QTM3_PON[d]	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	–	1.8
					Low	0	–	0.45
47	PCIE_RXM0		PCIe Negative Receive Data0	Input	Differential	–	–	–
48	QTM_IO_1.9V[d]	V	1.904 V power supply	Output	Power	1.8	1.904	2
49	PCIE_RXP0		PCIe Positive Receive Data0	Input	Differential	–	–	–
50	PCIE_PERST_N		PCIe Reset	Input	Low	0	–	0.7
				Input	High	1.5	–	VCC
51	GND	V	Ground	Input	Power	–	0	–
52	PCIE_CLKREQ_N	OC	PCIe Clock Request	Output	Low	0	–	0.35
53	PCIE_REFCLKM		PCIe Negative Reference Clock	Input	Differential	–	–	–
54	PCIE_PEWAKE_N	OC	PCIe Wake	Output	Low	0	–	0.35
55	PCIE_REFCLKP		PCIe Positive Reference Clock	Input	Differential	–	–	–
56	NC		Reserved—Host must not repurpose this pin.					
57	GND	V	Ground	Input	Power	–	0	–
58	NC		Reserved—Host must not repurpose this pin.					
59	ANT_CTRL0		Antenna tuning control (low bands)	Output	High	1.35	–	1.8
				Output	Low	0	–	0.45
60	Reserved		Reserved—Host must not repurpose this pin.					
61	ANT_CTRL1		Antenna tuning control (low bands)	Output	High	1.35	–	1.80
				Output	Low	0	–	0.45

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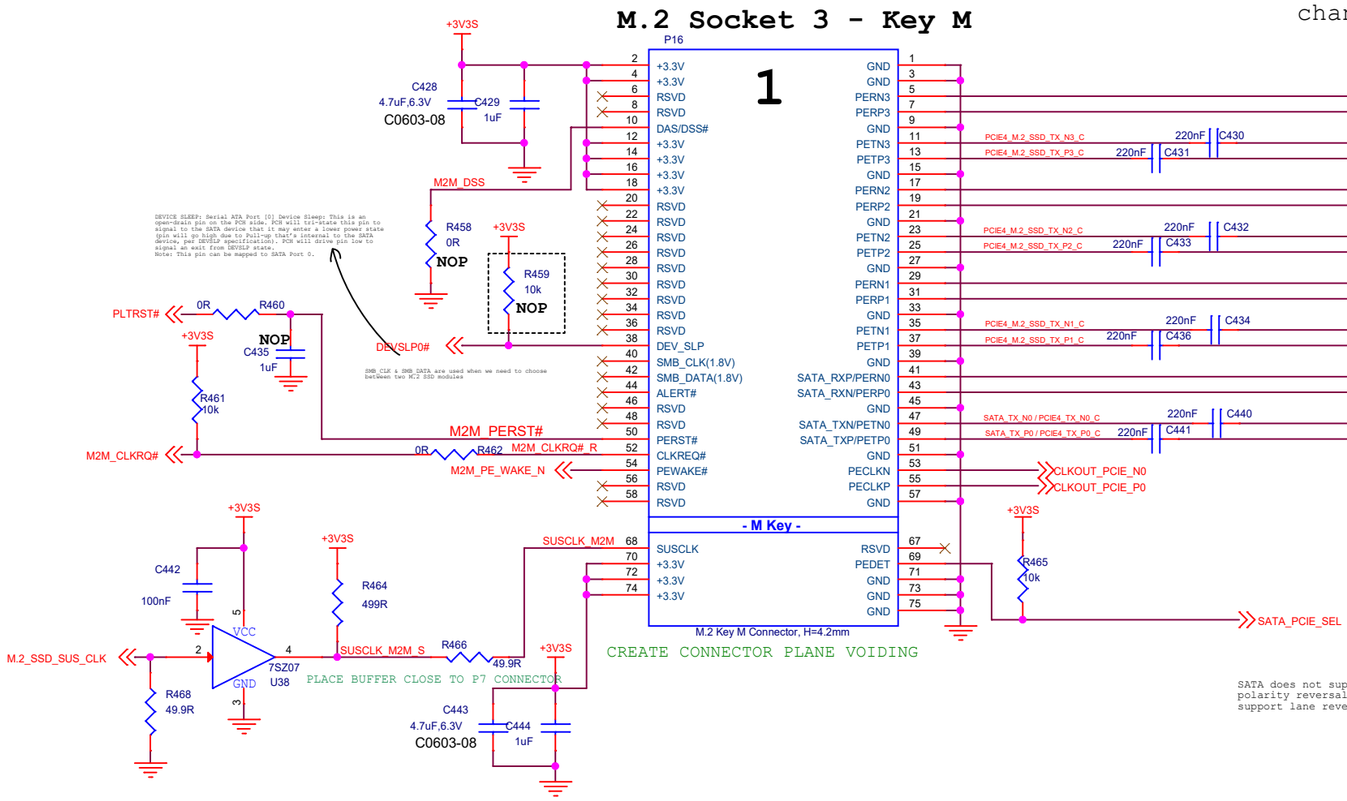
P 143/270 IN TL-SBC

980 PRO PCIe 4.0 NVMe M.2 250GB SSD

changed from H=4.2mm to H=6.7mm

changed from 182K06700S to 182K06706S

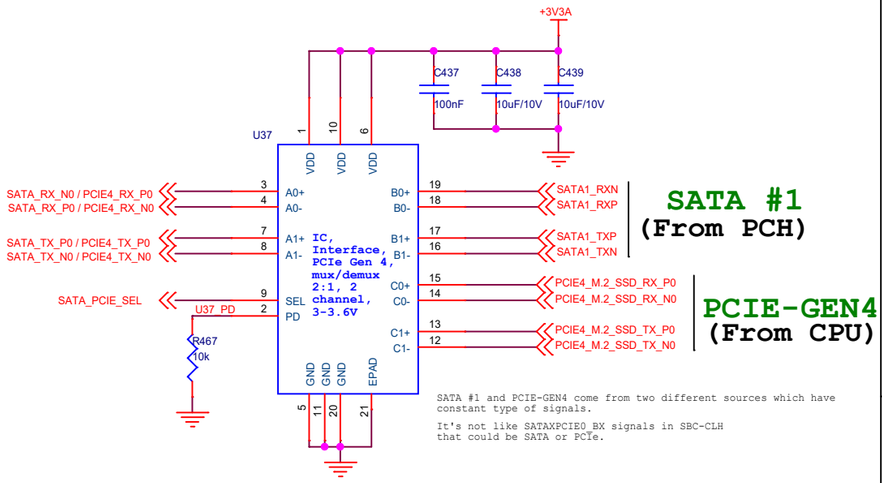
M.2 Socket 3 - Key M



A PCIe* Lane is composed of a single pair of Transmit (TX) and Receive (RX) differential pairs, for a total of four data wires per PCIe* Lane (such as, PCIE[3]_TXP/ PCIE[3]_TXN and PCIE[3]_RXP/ PCIE[3]_RXN make up PCIe Lane 3). A connection between two PCIe* devices is known as a PCIe* Link, and is built up from a collection of one or more PCIe* Lanes which make up the width of the link (such as bundling 2 PCIe* Lanes together would make a x2 PCIe* Link). A PCIe* Link is addressed by the lowest number PCIe* Lane it connects to and is known as the PCIe* Root Port (such as a x2 PCIe* Link connected to PCIe* Lanes 3 and 4 would be called x2 PCIe* Root Port 3).

PCIE-GEN4

PCIe Gen4 : 16.0 GT/s = 1.969 GB/s (per lane)



SATA #1 (From PCH)

PCIE-GEN4 (From CPU)

SATA #1 and PCIE-GEN4 come from two different sources which have constant type of signals.

It's not like SATAXPCIE0_BX signals in SBC-CLH that could be SATA or PCIe.

Title	M.2 M (SSD)	
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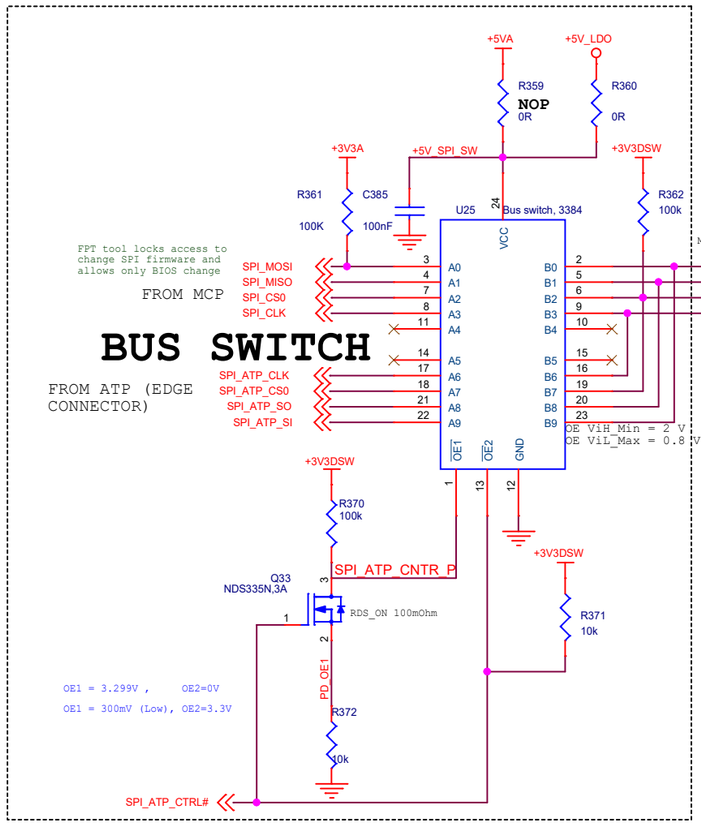
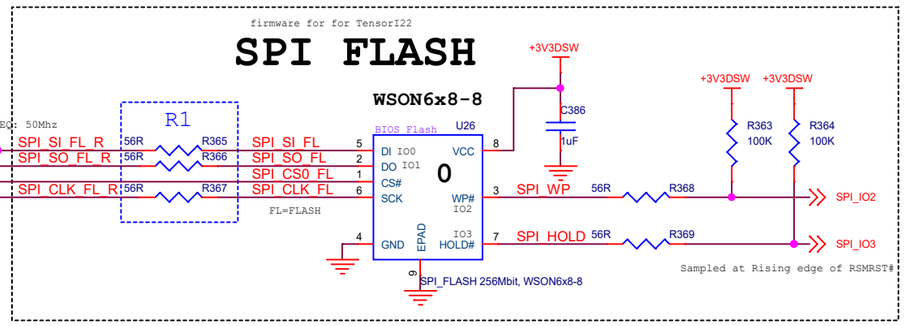
2-Load Branch MAF Topology (Master Attached Flash)

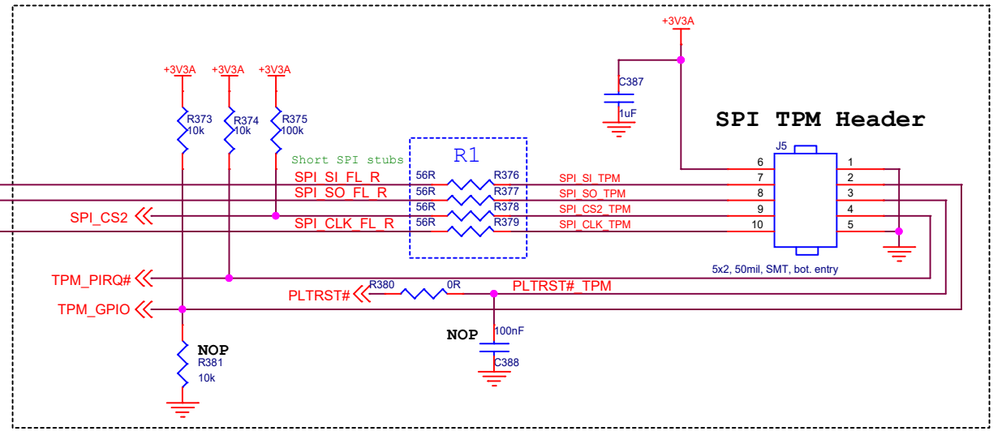
SPI_CLK & SPI_MOSI matched to within 500 mil
SPI_CLK & SPI_CS[0,1] matched to within 500 mil



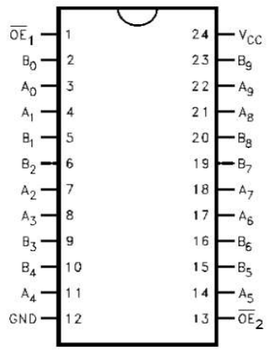
if SPI_ATP_CNTR# = 0V then SPI_ATP_CNTR_P = 3.299V
if SPI_ATP_CNTR# = 3.3V SPI_ATP_CNTR_P = 300mv < 0.8V (V_IL,MAX)



SPI_IO2 & SPI_IO3
External pull-up is required. Recommend 100 kohm if pulled up to 3.3 V or 75 kohm if pulled up to 1.8 V.
This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.



Connection Diagram



Truth Table

$\overline{OE}_1$	$\overline{OE}_2$	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

Title	SPI FLASH/TPM		
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I2C GPIO I/O Expander

U39 Internal 100K PU are enabled by default

PCA9555

Address: 0x40

the RIBBON ID are inputs to the GPIO EXPANDER, by default, these pins are 1 (internal 100K PU), untill a ground is connected to some Ribbon ID pin in TRIP (on TEL Side)

Internal 100K PU are enabled by default
After power-up, the XRA1201 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled. The XRA1201P has the internal pull-up resistors enabled upon power-up in case it is necessary for the inputs to be in a known state.

I2C Mux

U40

PCA9518 I2C HUB

from master

Pull-Down

RN1 10K/8P4R

by default, the GPIO exapnder has internal pull up of 100K, which causes the EN pins to be 0.3V (becase of 10K pull down). 0.3 is lower than the ViL which is 0.5V.

SMB_CLK_1 | to Trip 1
SMB_DATA_1
EEPROM ADDRESS: 0x54

SMB_CLK_2 | to Trip 2
SMB_DATA_2
EEPROM ADDRESS: 0x54

SMB_CLK_EB | TO EB-TI22A (B2B)
SMB_DATA_EB
EEPROM ADDRESS: 0x54
I210 Address: 0x49 (P.222)

EEPROM

U41 24C08 (1KB)

EEPROM ADDRESS: 0x54

74LVC08 U42A

74LVC08 U42B

74LVC08 U42C

74LVC08 U42D

There are TELS that are not supposed to work on certain TRIPS.

the BIOS reads what is written on each TEL's EEPROM and according to it , it knows which TEL is this and it decides whether to send a reset through PLTRST#_BYP_1 and PLTRST#_BYP_2.

The purpose of the reset is not freeze the system in case of mis-installing of TELS.

the RESET is sent only to the SPECIFIC TEL.

AND Gate: Reset Override - if you place an incorrect TEL that shouldn't work on specific TRIP, the BIOS should identify this (the address on TEL is sent back through GPIO EXP to BIOS and then BIOS initiates a reset using PLTRST#_BYP_1).

the GPIO EXP is like an EEPROM, it has a wide range of addresses, and we can change the value of each bit to 0 or 1.

EEPROM ADRESS ON ALL TELS ARE THE SAME (0x54) BUT DATA THAT SPECIFIES THE PURPOSE OF EACH TEL IS DIFFERENT.

Title	SMBus_MUX/GPIO_EXPANDER	
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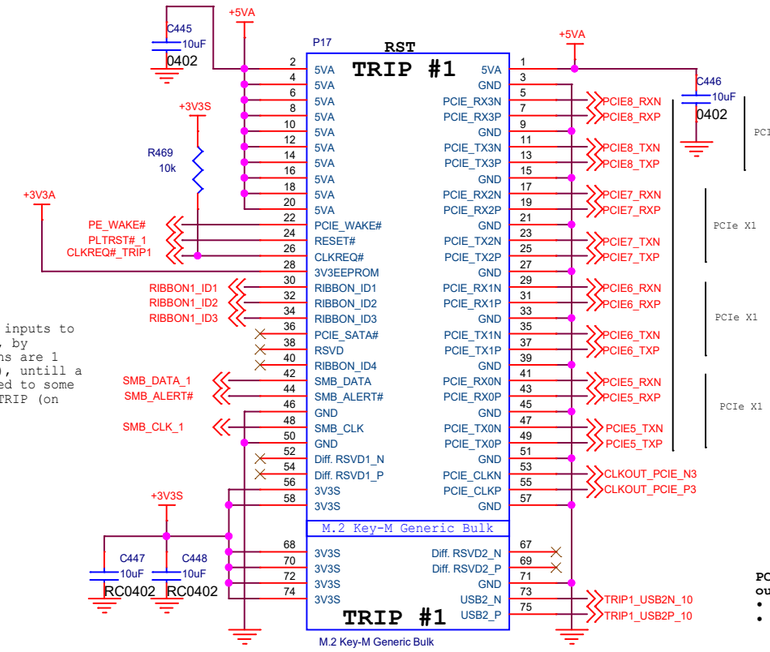
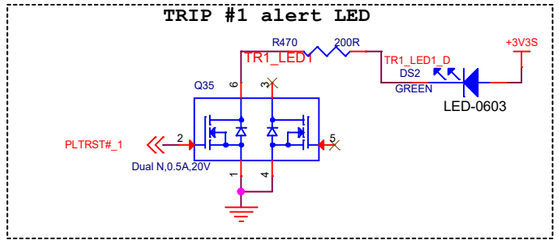


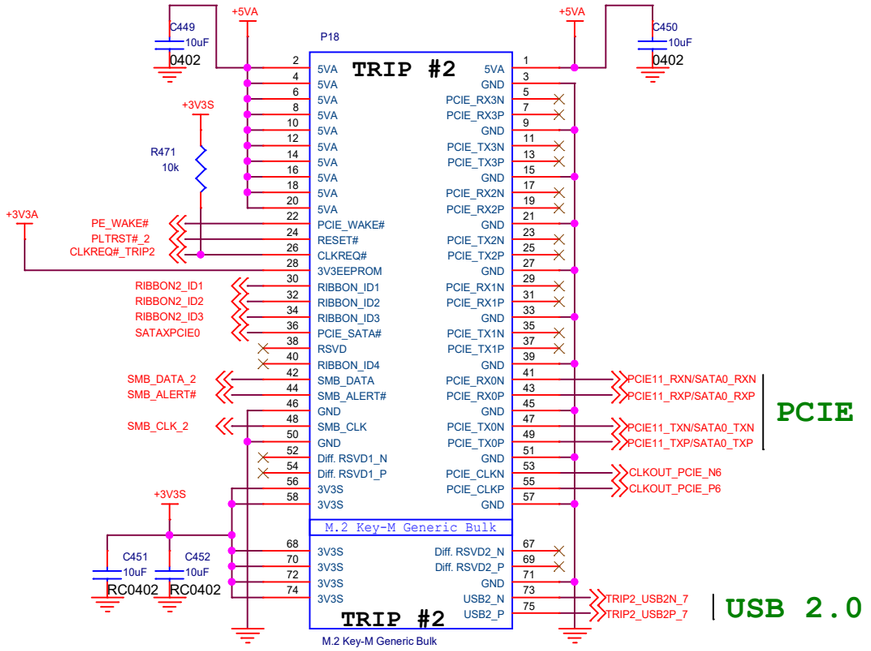
The TX capacitors should be near the connector of the device (in TRIP case, on the TEL), and the RX capacitors will be on the device's PCB.
If the PCIe is for a chip which is on you board, both TX and RX capacitors should be located near the device IC.

the RIBBON ID are inputs to the GPIO EXPANDER, by default, these pins are 1 (internal 100K PU), untill a ground is connected to some Ribbon ID pin in TRIP (on TEL Side)

PCIE-GEN3

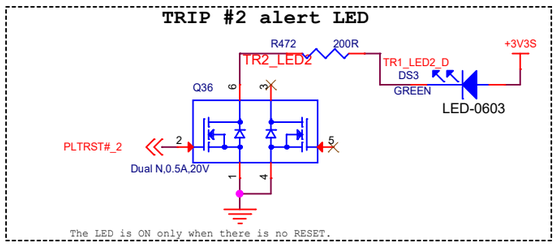


PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices
- **CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support**
- **CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support**



PCIE x1/SATA

USB 2.0



The LED is ON only when there is no RESET.

Title: TRIP 1&2			
Size: A3	Document Number: <Doc>		Rev: <RevCode>
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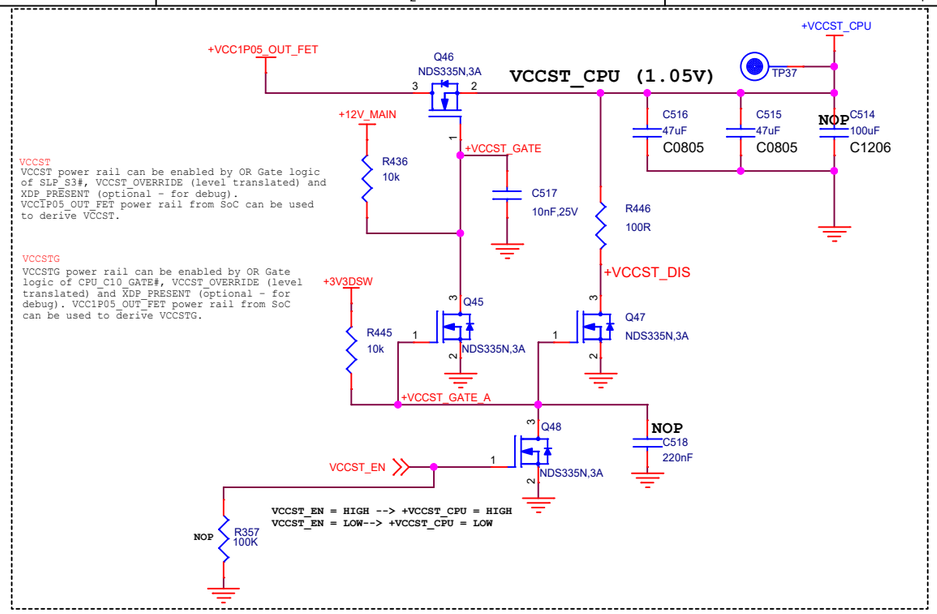
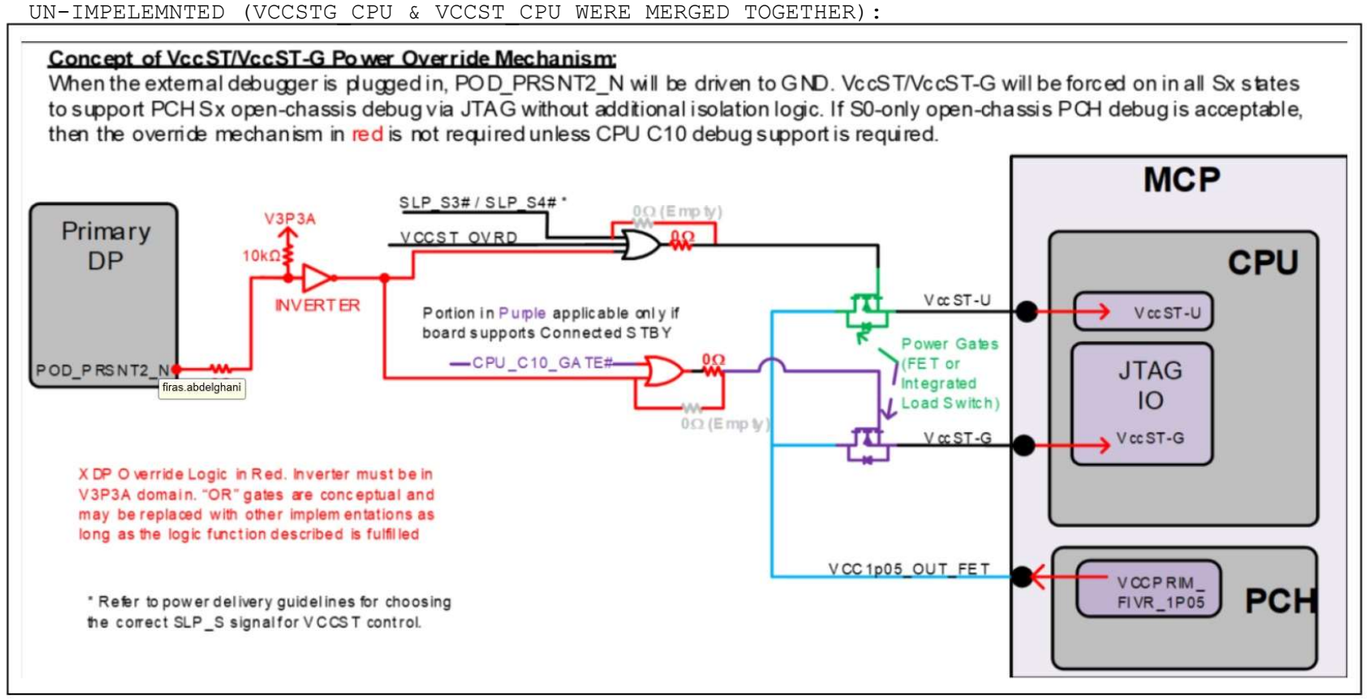


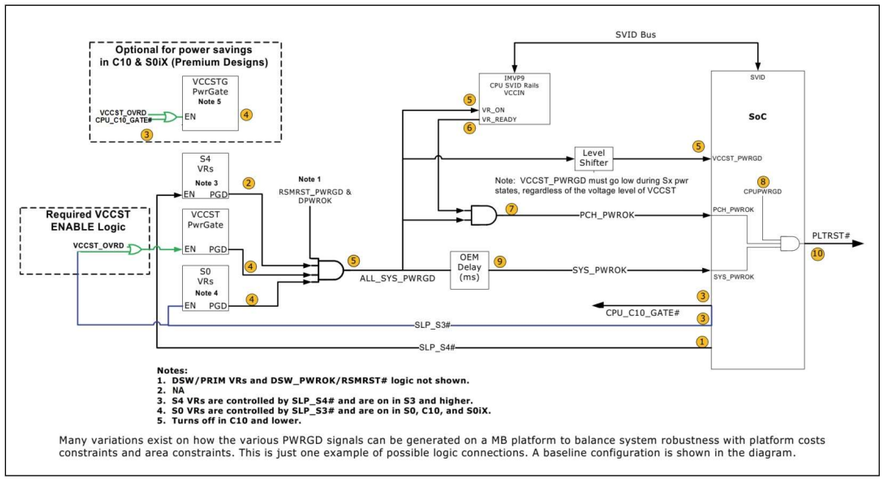
UN-IMPELEMNTED (VCCSTG_CPU & VCCST_CPU WERE MERGED TOGETHER):



IN VOLUME: VccSTG gated by SLP_S3#

IN Premium, VccSTG gated by {CPU_C10_GATE#}

Figure 247. Premium PWROK Generation Flow Diagram



Many variations exist on how the various PWRGD signals can be generated on a MB platform to balance system robustness with platform costs constraints and area constraints. This is just one example of possible logic connections. A baseline configuration is shown in the diagram.

Title	<Title>		
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