TGL Power Map --- Please defer to component EDS/datasheet for offical numbers. Non-Intel devices are current estimates. **Intel CONFIDENTAL for use under NDA** Updated: 2020-August Load Summary Voltage Regulators (VRs) Load Switches (LS) SUB-RAIL NAME RAIL NAME Max R_{dsON} V_{NOMINAL} V_{IN} V_{OUT} I_{TDC} Enable LOAD NAME I_{MAX} V_{IN} VR_EN VDC SVID TGL SKU: UP3-R 4+2 28W VCCIN (IMVP9) SVID 65.00 A 43.00 A VCCIN (IMVP9) CPU PL2/4 Config: Performance Deep Sleep: Non-Deep Sleep ➤ VCCIN_AUX Memory: 32GB DDR4 3200 MT/s VCCIN AUX SLP SUS# VDC VID 27.00 A 14.00 A 1.80 V PD Tier: Volume □ VCCST+VCCSTG Additional Options: Connected Standby Wake on Voice Capability V1.05A (internal rail in PCH FIVR) SLP_S3# PCH FIVR 1.050 V VCCSTG 1.050 V 1.20 V VDD2_MEM SLP_S4# VDC 1.20 V 9.40 A → VDD2_CPU 1.20 V Adapter Non-NVDC 0.60 V DDR VTT CTRL VDC 0.60 V 0.40 A Charger SLP S4# VDC 2.5V 1.00 A 2.50 V NVDC SLP_SUS# VDC 1.80 V 1.30 A CCPRIM_1P8 1.80 V V1.8A_FLASH V1.8A_EC 1.80 V Battery 1.80 V 1.80 V SLP S3# V1.8A V1.8S V1.8S_SSD V1.8S *CCG recommends NVDC charger and 2SxP battery for better VR ▶₩ V1.8S_PLATFORM SLP_S0# && SLP_S3# 1.80 V V1.8A V1.8S_SDCARD V1.8Dx_WIFI performance, however traditional 3SxP battery and non-NVDC 1.80 V charger may implemented in some designs 1.80 V ► III V1.8S_AUDIO V1.8S_AUDIO V1.8S_SENSORS GPIO AUDIO V1.8A 1.80 V 1.80 V **SoC Power Levels** (NC) X VCC_V1P05EXT_1P05 N/A 28 connecting to GND is allowed, but not recommended due to extra leakage PL2: 64 VCC_VNNEXT_1P05 N/A PL3: 66 value for a definiion PL4: 121 ➤ V3.3_DSW 3.30 V 0.20 A 3.30 V VDC VCCDSW 3P3 VCCPRIM_3P3 V3.3A_EC 3.30 V 3.30 V **■** V3.3S V3.3 DSW SLP_S3# V3.35 V3.30x, SSD V3.30x, EDP V3.30x, DPWP V3.30x, TOUCHSCREN V3.30x, CAMERA V3.30x, SDCARD V3.30x, WIFI V3.30x, MODEM V3.30x, MODEM 3.30 V Note: Use of a GPIO+BIOS control is also allowed; consult PDG. V3.3Dx_PLATFORM V3.3 DSW SLP S0# && SLP S3# 3.30 V VR Naming Convention 3.30 V Suffix **Engerized States** 3.30 V On in SO, SOix 3.30 V

SLP SUS# VDC 5.00 V 2.00 A

→ ¥ V3.3S_AUDIO

→ W V5S_PLATFORM

→ WDCDx_EDP

V3.3_DSW

V5A

VDC

GPIO_AUDIO

GPIO_L

3.30 V

3.30 V

3.30 V 3.30 V

3.30 V 3.30 V

5.00 V

5.00 V 5.00 V 5.00 V

VDC

V3.3S_AUDIO V3.3S_SENSORS

V5S_AUDIO V5Dx_HDMIWP V5Dx_USBWP

VDCDx_EDP

On in S0 - S3

On in S0 - S5

On in SO - DS4/DS5

DSW