

11th Gen Intel® Core™ Processors for IoT Platforms Latform Design Guide (PDG) Addendum 1rch 2021 L Confidential Platforms madot 2771; IPLA 3883; RET 1812:364 Fires sheld by an irres above legisle in the computation of the control of

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Revision History

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- Filips	Revision His	Revision	Description	
	March 2021	2.1	Updated note on Chapter 4 MDIO Routing Guidelines Updated Package Name and information in Table SGMII Ethernet-TSN Signals, MDIO Ethernet-TSN Signals and Other Signals Associated with Ethernet-TSN Subsystem Description. Added note on Chapter 4.5.2 Other Signal Associated with Ethernet-TSN Subsystem Routing Guidelines	51305
delgha	November 2020	2.0	Updated note in Table 19, Table 21, and Table 23 Update chapter 4 on MDIO Routing Guidelines	
abu	October 2020	1.8 0	 Added note on Chapter 1.3 Update 11th Gen Intel® Core™ Processors Pin No in Chapter 4.6 	
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	June 2020	delghall	• Added Chapter 14 11th Gen Intel® Core™ Processors - Adhesives Guidance.	201217
	May 2020		 Updated Note No3 in Table 11 and Table 13. Added new Chapter 3 eSPI. Added new Chapter 4 Ethernet Time-Sensitive Networking. Updated Table 16 Other Signal Associated with Ethernet-TSN Subsystem Signal Description on SGMII_INT's Description – removed Wake-on-LAN (WOL) information. 	
3883; R3	May 2020	1.2 at	Updated Chapter 6 DP (without retimer), eDP topologies and removed	_{llab.co.il}
	3; RS1305?	96°	 Added Chapter 10 PCIe Clock. Added Chapter 11 SATA (to SATA device through internal cable). Added Chapter 12 Type-C TBT+USB+DP with retimer. Added Chapter 13 Time-Aware GPIO. 	lab.
	March 2020	1.1	Added Chapter 4 Display and Chapter 5 USB3.2.	



1.0 Introduction

This 11th Gen Intel® Core™ Processor Platform Design Guide (PDG) Addendum may be used as supplement documentation that covers IoT-specific features and extended temperature, such as GSPI routing guidelines, Ethernet-TSN routing guidelines, CNVi routing guidelines and Small Form Factor Display and USB 3.2 routing guidelines. This addendum complements the 11th Gen Intel® Core™ Processor Platform Design Guide (PDG) (RDC #607872). The PDG provides motherboard implementation recommendations for the 11th Gen Intel® Core™ processor.

Note: For IoT use conditions, refer to the link provided in Table 1.2.

1.1 Terminology

Table 1. Terminology

51305364 Firas a	Term	Description il Chi
636h	CLK	Clock
G1305	CML	Current Mode Logic
2	CMOS	Complementary Metal Oxide Semiconductor
	CS	Chipset
	GMII	Gigabit Media Independent Interface
-36A F	IEEE	Institute of Electrical and Electronic Engineers
43055	Ю	Input Output
RS	IoT	Internet of Things
PLA3883; RS1305364FN	LAN	Local Area Network
OLAS	MDC	Management Data Clock
	MDIO	Management Data Input/Output
	MISO	Primary In Secondary out (Master In Slave Out)
	MOSI	Primary Out Secondary In (Master Out Slave In)
283,	P&N	Positive and Negative
al A30	PCH-LP	Platform Controller Hub Low Power
11; IPLA3883; N	PHY	Physical Layer Device
21211	SPI	Serial Peripheral Interface
1930,	TSN 543	Time-Sensitive Networking
, *		101,



Note: This document reflects Intel's adoption of industry-wide changes in the use of inclusive and non-discriminatory language. As such, this document replaces the terms *master* and *slave* with *primary* and *secondary*. Nonetheless, these changes have not as yet been reflected in the software options described in this document; therefore, be aware that when this document uses the terms *primary* or *secondary*, it is referring to menu items or options that might still be labelled *master* or *slave* onscreen.

1.2 Reference Documents

Table 2. Reference Documents

Document	Document No./Location
11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (PDG)	607872
IoT Use Conditions Application	https://www.intel.com/content/www/us/en/secure/design/confidential/products-and-solutions/processors-and-chipsets/iot-use-conditions.html
11th Gen Intel® Core™ Processor UP3 External Design Specification (EDS) Addendum	608733
11th Gen Intel® Core™ Processor Platform Component List (PCL) Addendum	620609

1.3 Pin List for Ethernet-TSN & Time-Aware GPIO and Integrity Features

Table 3. Pin List Details

Pin Name	Pin	and
Ethernet-TSN	igh;co.il	0.
PCIE7_TXN / TSN_0A_TX_DN	CD8	
PCIE7_TXP / TSN_0A_TX_DP	CD9	
PCIE7_RXP / TSN_0A_RX_DP	CK1	
PCIE7_RXN / TSN_OA_RX_DN	CK2	
PCIE8_RXN / TSN_OB_RX_DN	CK4	
PCIE8_RXP / TSN_OB_RX_DP	CK5	Ubn



96.	, 2b.co.ll	,
inte	compulab.co.ll	Introduction
lanifiras.abdelgham	Pin Name	Pin
ani fira	Ethernet-TSN	1; IPL'
	PCIE8_TXN / TSN_OB_TX_DN	CB7
	PCIE8_TXP / TSN_OB_TX_DP	CB8
5.21	GPP_F17 / THC1_SPI2_RST_N / SGMII_MDC_0A	DV14
ras abdelghani firas al	GPP_F18 / THC1_SPI2_INT_N / SGMII_MDIO_0A	DN10
I alghan	GPP_C3 / SMLOCLK / SGMII_MDC_0B	DK19
as above	GPP_C4 / SML0DATA / SGMII_MDIO_0B	DM17
(2)	GPP_S0 / SNDW0_CLK / SGMII_AUXTS	DT32
	GPP_S1 / SNDW0_DATA / SGMII_INT	DR35
10	GPP_S2 / SNDW1_CLK / DMIC_CLK_B0 / SGMII_RESET_N	DW35
	GPP_S3 / SNDW1_DATA / DMIC_CLK_B1 / SGMII_PPS	DV35
305364 Firas abdelo	Time-Aware GPIO	coiller
	GPPC_H19 / TIME_SYNC_0	DJ27
	GPPC_B14 / SPKR / TIME_SYNC_1 / GSPI0_CS1B	DC50
	INTEGRITY FEATURES	1
	GPPC_F22_VNN_CTRL_IEH_CORR_ERROB	DV12
2536A	GPPC_F23_V1P05_CRTL_IEH_NONFATAL_ERR1B	DT12
25130	GPPC_H3_SX_EXIT_HOLDOFFB_IEH_FATAL_ERR2B	DG31
3883 [,] RS1305364 F	GPP_T2	DT35
,5	GPP_T3	DN33
	GPP_C16 / I2C0_SDA	DW18
	GPP_C17 / I2C0_SCL	DV18
, P	GPP_C18 / I2C1_SDA	DT18
012171; IPLA3883; P	GPP_C19 / I2C1_SCL	DJ23
11:11	GPP_H4 / I2C2_SDA	DJ31
121	GPP_H5 / I2C2_SCL	DJ29
	GPP_H6 / I2C3_SDA	DF29



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Introduction	il chdao12171; IPLA3883	intel ^{a Firas} ab
-s.abders	Pin Name	Pin
HINDS	Ethernet-TSN	1:191
	GPP_H7 / I2C3_SCL	DF29
	GPP_B5 / ISH_I2CO_SDA	DB44
abdelghani firas.abd	GPP_B6 / ISH_I2CO_SCL	DB45
ani filia	1/2.	DB47
relalys.	GPP_B8 / ISH_I2C1_SCL	CY39
abor	GPP_B9 / I2C5_SDA / ISH_I2C2_SDA	DD44
	GPP_B10 / I2C5_SDA / ISH_I2C2_SCL	DD47
-364 Fir	as abdelghani@co	3b.co.il cnd20121
3883; RS13053	GPP_B8 / ISH_I2C1_SCL GPP_B9 / I2C5_SDA / ISH_I2C2_SDA GPP_B10 / I2C5_SDA / ISH_I2C2_SCL §	ighani@compula.
2171; IPLA3883; HE	3883; RS130536A Firas abdelone	ore™ Processors for IoT Platforms



2.0 Generic Serial Peripheral Interface (GSPI) 3.3V

2.1 GSPI Platform- Specific Important Information

This chapter is additional supplement for Chapter 6.11 Generic Serial Peripheral Interface (GSPI) from the 11th Gen Intel® Core™ Processor Platform Design Guide (RDC #607872) and is applicable for the extended temperature range. For extended temperature range details, please refer to the 11th Gen Intel® Core™ Processor EDS Addendum.

The Platform Control Hub Low Power (PCH-LP) three generic SPI (GSPI) Interfaces support devices which use SPI serial protocols for transferring data. Each interface consists of four wires: a clock (CLK), two-chip select (CS) and two data lines (MOSI and MISO). GSPI is not the same as the PCH SPI interface for flash devices. This GSPI is used mainly for sensor support on the platform.

2.2 GSPI Signal Descriptions

2.2.1 Signals Group

Table 4. GSPI Signals

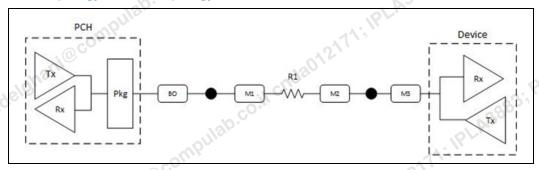
Group	Signal Name	Description
Clock	GSPIO_CLK GSPI1_CLK GSPI2_CLK	Clock signals
Data	GSPI0_MISO GSPI1_MISO GSPI2_MISO	Primary In Secondary Out (Master In Slave Out) signals
CAFIRAS AL	GSPI0_MOSI GSPI1_MOSI GSPI2_MOSI	Primary Out Secondary In (Master Out Slave In) signals
Chip Select	GSPI0_CS0# GSPI1_CS0# GSPI2_CS0#	Chip select signals

2.3 GSPI Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for the generic SPI interfaces.



Figure 1. GSPI Topology: 1-Load Topology (Add-In Card)



Series resistor R1 mentioned in the above GSPI topology have a recommended value of 15 ohm on GSPI [0:2] CLK and GSPI [0:2] MOSI only.

Table 5. GSPI Routing Guideline for 11th Gen Intel® Core™ Processor PCB

Segment	Tline Type	Reference	Nominal Via Count	Impedance	Max. Length Segment, mm (Inches)	Max. Length Total ,mm (Inches)
ВО	MS/SL	VSS	1	Max. 59Ω ± 10%	12.7 (0.5)	
M1	MS	VSS	0	43 Ω ± 10%	17.78 (0.7)	215.9
M2	MS	VSS	1	43 Ω ± 10%	83.82 (3.3)	(8.5)
М3	MS/SL	VSS	0	43 Ω ± 10%	101.6 (4)	

- 1. R1 resistor should be stuffed with 15 Ω . Design guideline applies to GSPI[0:2]_CLK and GSPI[0:2]_MOSI.
- 2. Up to seven vias are allowed in each route.
- 3. Continuous ground reference plane.
- 4. Max. Frequency to 20MHz for ISH and 25MHz for GSPI.



2.4 Trace Length Matching

Table 6. GSPI length matching

		- ^ \
9,,	Notes	Description
	Minimum length	M2: 7.62 mm (0.3 inches)
200	0.11	M3: 12.7 mm (0.5 inches)
i fil'asia	Length matching between CLK and DATA signals	12.7 mm (0.5 inches)
bani	Trace spacing between DATA and DATA signals	BO: w
18/01	i@ ^{CC}	M1-M3: w
as abdelghair	Trace spacing between CLK and DATA	BO: w
-ir35	4e19,	M1-M3: 3w
<i>F</i> 1.	Trace Spacing between GSPI CLK/DATA with other	BO: w
	non GSPI signals	M1-M3: 3w
	71,	

NOTE:

2.5 Debug Guidelines / Recommendations

GSPI signals are multiplexed with GPIOs and default to GPIO functionality. If the GSPI interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

2.6 Tools

Intel does not promote any specific tool for this interface.

§

^{1. &#}x27;w' is the trace width. If there are traces of different widths, the larger width should be taken.



3.0 Enhanced Serial Peripheral Interface (eSPI)

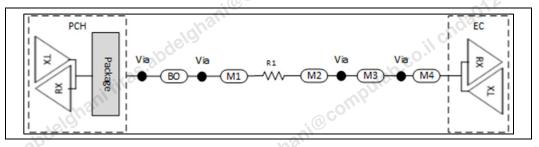
3.1 eSPI Platform – Specific Important Information

This chapter is additional supplement for Chapter 6.12 Enhanced Serial Peripheral Interface (eSPI) from 11th Gen Intel® Core™ Processor Platform Design Guide (RDC #607872) and is applicable for IoT use cases with an activity factor of 100% for approximately 10 years.

3.2 eSPI Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for the eSPI interfaces.

Figure 2. eSPI 1-Load Topology (Device Down)



Series resistor R1 mentioned in the above eSPI topology have a recommended value of 50Ω on ESPI_CLK and 15Ω on ESPI_IO_[0:3].



eSPI 1-Load Topology (Device Down) Routing Guideline Table 7.

Table 7.	eSPI 1-Load Topology (De	vice Down) Routing G	iuideline			
nani firas abs Table 7.	Parameter		Ro	outing Guidel	ines		F
	Transmission Line Segment	во	M1	M2	МЗ	M4	51305364 F1
	PCB Routing Layer(s)		il cho	Any, MS, or S	SL		ai RS
:: 125.2b	Characteristic Impedance	120	.co.,	50Ω ± 10%		A388	
alghani in	Trace Width (w)	4 mil min.		Meet im	pedance		
iras abdelghani firas abd	Trace Spacing (S1) between CLK and other signals	2.5w		3w	1930 ·	2.5w	21.A3883; R5
	Trace Spacing (S2) between data and other data signals		apul	ab .co			A: IPLA386
51305364 Firas abdeldh	Max. Trace Segment Length	12.7mm (500 mils)	12.7mm (500 mils)	0.5mm (19.69 mils)	101.6mm (4000 mils)	12.7mm (500 mils)	
-36A File	Min./Max Total Length (T1+T2+T3)	38.1mm	n (1500 mils)	min./140.2m	ım (5519.69m	nils) max.	
51305	Maximum Via Count			zmp			71:15
	abdelgli R1			0Ω on ESPI_(Ω on ESPI_IO			and20121
GA Fi	Length matching between clock and data		abdels 12	2.7mm (500 r	nils)		W.
130 ⁵³⁰	Reference Plane	di filas	Cont	inuous grour	id only	brilap.	
1,43883; RS1305364 Fil	Length matching between clock and data	0.		2.7mm (500 n			
PLA30	305364 Firas at		i fir	s.abdelgl	/o.		oulab.co.il ch
,3883; RS		abdel	gham			.hani@c	DIUL.
PLA36	Core™ Processors for IoT Platfo	ras c		delghani f	iras.abdel	3),	ompulab.co.il chi
11th Gen Intel® PDG Addendun	Core™ Processors for IoT Platfo	orms	Filas			March 2	2021
16	•	Intel Confid	dential	Do	cument Num	ber: 608734	-2.1



Figure 3. eSPI Add-in-card Topology

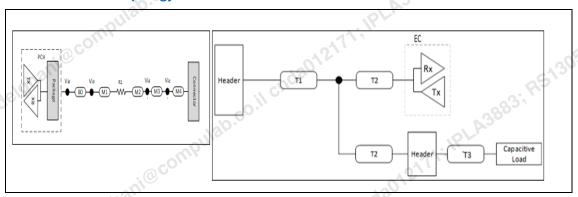


Table 8. eSPI Add-in-card Topology Routing Guideline

	Parameter	Routing G	uidelines
.10	Transmission Line Segment	T1 - MR	T2 - BI
pyelo),	PCB Routing Layer(s)	Any, MS, or SL	48012
eiras al	Characteristic Impedance	50Ω ± 10%	illond
536A T	Trace Width (w)	Meet impedance	4 mil min.
25 ¹³⁰³	Trace Spacing (S1) between CLK and other signals	>3w	w
	Trace Spacing (S2) between Data and other Data Signals	whanie	w
264 Fi	Max. Total Length (T1+T2+T3) on Add-in Card	1.6"	, 50.CO
A3883; R513053	Maximum Via Count	No limit. Ground stitching via m from every layer transi	. ((V)
IPLA36	Length matching between Clock and Data	500 mils (including ler	gths on base board)

§



4.0 Ethernet Time-Sensitive Networking

4.1 Serial Gigabit Media Independent Interface (SGMII)

Serial Gigabit Media Independent Interface (SGMII) is the Cisco Systems* standard used by the Ethernet industry to provide a serialized interface between the Ethernet controller and an external physical layer device (PHY) component. With SGMII, the subsystem can achieve Ethernet LAN speeds of 10Mbps, 100Mbps, 1Gbps, and 2.5G bps.

The Ethernet-TSN MAC provides an SGMII interface to the External PHY. It consists of two sets of differential pairs using Current Mode Logic (CML) circuitry on one multiplexed 11th Gen Intel® Core™ Processors PCH-H ModPHY lanes. The design embeds the transmit clock in the transmit data and expects the receive clock to be embedded in the receive data. For PHY management, the Ethernet Controller also provides two CMOS Management Data Input/Output (MDIO) interface signals.

For specific design and implementation information about the GbE PHYs listed in 11th Gen Intel® Core™ Processor Platform Component List (RDC #620609), refer to the respective vendor website(s).

4.2 SGMII Signal Description

Table 9. SGMII Ethernet-TSN Signals

Signal Name ^{1,2}	Package Name	Type (Voltage Domain)	Direction	Description
TSN_OA _TX_DN	PCIE7_TXN	CML Differential Signal	Output	Transmit P&N of the
TSN_OA_TX_DP	PCIE7_TXP	(1.05V)		serial differential output
TSN_OB _TX_DN	PCIE8_TXN		han	
TSN_OB_TX_DP	PCIE8_TXP		regelo.	
TSN_OA_RX_DN	PCIE7_RXN	CML Differential Signal	Input	Receive P&N of the
TSN_OA_RX_DP	PCIE7_RXP	(1.05V)		serial differential input
TSN_OB_RX_DN	PCIE8_RXN	ighair.		a com
TSN_OB_RX_DP	PCIE8_RXP	nders		nie

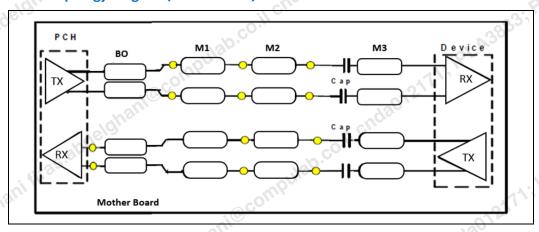
- Refer 11th Gen Intel® Core™ Processor-UP3 EDS Addendum (RDC #608733), Chapter 6: Flexible High-Speed Input/Output (HSIO), for a description of how these signals are routed to and selected by the FIA/MODPHY.
- 2. Only 0A or 0B can be used for single Ethernet-TSN port



4.3 SGMII Topology Description and Routing Guidelines

4.3.1 SGMII Topology Guidelines (Device Down)

Figure 4. SGMII Topology Diagram (Device Down)



4.3.2 SGMII Routing Guidelines (Device Down)

Table 10. SGMII Routing Guidelines (Device Down)

Segment	Tline Type	Reference	Via Count	Impedance	Max. Length, Segment (mm)	Max. Length, Total (mm)
ВО	MS/SL	VSS		ndels	15.2	oil c.
M1 or M2	SL/DSL	VSS	6,05	85 Ω	-	356
М3	MS	VSS			8	omp

NOTES:

- 1. Breakout impedance can vary depending on breakout routing.
- 2. Keep the BO differential impedance close to 85 ohm if possible.

4.3.3 SGMII Platform Routing Design (Device Down)

Table 11. SGMII Platform Routing (Device Down)

Notes	Details
AC capacitor value	75 nF to 265 nF, 100 nF nominal
Number of vias allowed	6
Reference plane	Continuous ground recommended
Breakout length and spacing	An initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed.

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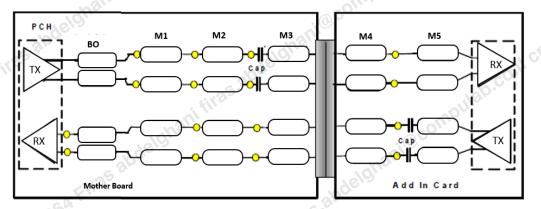


25.200	-70.C	The total br	eakout length is still 15.2mm
ani fira	ambrilge	microstrip	2*w (BO), 3*w (M1orM2), 3*w (M3)
	Spacing - Signal to equivalent signal	stripline	2.7*w (BO), 4.3*w (M1orM2)
	i elgham	dual stripline	4*w (M1orM2)
	3/000	microstrip	3*w (BO), 3*w (M1orM2), 3*w (M3)
V/3	Spacing - Signal to non-	stripline	4*w (BO), 4.3*w (M1orM2)
Johani I	equivalent signal	dual stripline	4*w (M1orM2)
Firas abders	2. Only 0A or 0B can be used for single	e TSN port. ipline and micro	widths, the larger width should be taken. ostrip, refer to "607872_TGL_UP3_PDG_Rev*.xlsx" (RDC #607872) in "U

- 'w' is the trace width. If there are traces of different widths, the larger width should be taken.
- Only OA or OB can be used for single TSN port.
- For line width and spacing of B0 stripline and microstrip, refer to "607872_TGL_UP3_PDG_Rev*.xlsx" (RDC #607872) in "U Tline Spec" tab. Please refer to PCIe under I/O Interface column as interface reference.
- Line width and intra-pair spacing for M1, M2 and M3 are to meet 85 ohm impedance.
- The maximum length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).

SGMII Topology Guidelines (Add-In Card)

SGMII Topology Diagram (Add-In Card)





4.3.5 SGMII Routing Guidelines (Add-In Card)

Table 12. SGMII Routing Guidelines (Add-In Card)

3	Segment	Tline Type	Reference	Via Count	Impedance	Max. Length, Segment (mm)	Max. Length, Total (mm)
ĺ	ВО	MS/SL	VSS	130.		15.2	1 23
	M1 + M2	MS/SL/D SL	VSS	4	85Ω	-	279.6
	М3	MS	VSS			8	-127

NOTES:

- 1. Breakout impedance can vary depending on breakout routing.
- 2. Keep the BO differential impedance close to 85 ohm if possible.

4.3.6 SGMII Platform Routing Design (Add-In Card)

Table 13. SGMII Platform Routing (Add-In Card)

Notes	Details				
i firas.au	The total length of the add-in card (M4 + M5) is usually 38mm to 50.4mm				
Add-in card (M4 + M5)	The M4 + M5 segment is a combination of MS/SL/DSL (MS where required to connect to surface mounted components)				
	The M4 + M5	s segment has a typical via count of 1			
AC capacitor value	75 nF to 265 nF, 100 nF nominal				
Number of vias allowed	4 (not counting via under package)				
Breakout length and spacing	An initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm – 0.16mm is allowed.				
200,	The total breakout length is still 15.2mm				
25	microstrip	2*w (BO), 3*w (M1 or M2), 3*w (M3)			
Spacing between SGMII differential	stripline	2.7*w (BO), 4.3*w (M1 or M2)			
pairs and to other signals	dual stripline	4*w (M1 or M2)			
	microstrip	3*w (BO), 3*w (M1orM2), 3*w (M3)			
Spacing between SGMII differential	stripline	4*w (BO), 4.3*w (M1orM2)			
pairs and to other signals	dual stripline	4*w (M1 or M2)			

- 1. 'w' is the trace width. If there are traces of different widths, the larger width should be taken.
- 2. Only 0A or 0B can be used for single Ethernet-TSN port.
- 3. Line width and intra-pair spacing for M1, M2 and M3 are to meet 85 ohm impedance.
- 4. The maximum length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).



4.3.7 SGMII General Platform Routing Design

Table 14. SGMII General Platform Routing Design

Notes	Details
Length matching between p and n within a differential pair	Within Layer Max. Mismatch: 254µm Total Length Max. Mismatch: 127µm (for channel end-to-end)
Length matching between pair to pair (inter Pair)	Not required.
Voiding recommendation for mainstream stackup	It is recommended to void pads for all components for example AC Caps as well as connector pads to optimize the impedance matching in the channel.
Discrete component part size for mainstream stackup	Recommended to use 0402 or smaller component sizes.
Reference plane	Continuous GND is recommended.
adelghanifiras.abdelghan	If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt).
as abc	If non-continuous power referencing is required on microstrip/surface layer, signal can reference power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
	Length matching between p and n within a differential pair Length matching between pair to pair (inter Pair) Voiding recommendation for mainstream stackup Discrete component part size for mainstream stackup

4.4 Management Data Input/Output (MDIO)

There is one set of MDIO signals for Ethernet-TSN subsystem. These signals are connected to the External PHY component. These signals allow software access to the Ethernet PHY management register of this component.



MDIO Signal Description

Table 15. MDIO Ethernet-TSN Signals

3/112	Signal Name ¹	Package Name	Type (Voltage Domain²)	Direction	Description
	SGMII_MDC_0A	GPP_F17 / THC1_SPI2_RST#	CMOS (1.8V or	Output	Management Data Clock This clock signal is driven by the LAN
20	SGMII_MDC_0B	GPP_C3 / SMLOCLK	3.3V)		Controllers to clock the serial MDIO Data. The clock period is programmable.
abdelglis	SGMII_MDIO_0A	GPP_F18 / THC1_SPI2_INT#	Open- Drain	Input/Output	Management Data Input/Output. This signal is driven by either the LAN
Firasia	SGMII_MDIO_0B	GPP_C4 / SMLODATA	(1.8V or 3.3V)	20.5	Controllers or the External PHY component during the MDIO transaction.

NOTES:

- 1. Only OA or OB can be used for single Ethernet-TSN port.
- The signals should be configured to 1.8V or 3.3V using the multiplexed GPIO's Individual Voltage Select soft strap.

MDIO Routing Guidelines

For routing guidelines, please use guidelines for I2C in 607872 TGL UP3 PDG Rev*.xlsx '#SMB,SML and I2C' tab. Use the guidelines for SCL as that of MDC and the guidelines for SDA as that for MDIO. Match the lengths of MDIO and MDC to within 25.4mm.

The MDIO buffer is open drain and hence needs a pull up resistor. Please use the I2C SDA pull up resistance as a guide for the total pull up resistance value. The external pull up resistance is in parallel with any internal pull resistance set.

For example, if the frequency of the MDC is 2 GHz. the total value of the pull up resistance (external pull up resistor in parallel with any internal pull up resistor) is as shown in Table 16.

Table 16. Total Value Pull Up & Down Resistance (2 GHz.)

SHOWITHI TAble To.		hani	
Total Value Pull Up & Down	n Resistance (2 GHz.)	gelg,	il ci,
Total Bus Capacitance (C _b)	Total Pull Up Resistance	PCH Pull Down Resistance	1/3/b.co.ll
Up to 50 pF	2.2 kohms	100 ohms	Mbn,
50 pF to 100 pF	1.2 kohms	100 ohms	
50 pF to 200 pF	560 ohms	100 ohms	
100 pF to 300 pF	330 ohms	50 ohms	
100 pF to 400 pF	270 ohms	50 ohms	compu



4.5 Other Signals Associated with Ethernet-TSN Subsystem

There are other signals associated with the Ethernet-TSN subsystem, which are AUXTS, INT, RESET_N, and PPS.

4.5.1 Other Signals Associated with Ethernet-TSN Subsystem Signal Description

Table 17. Other Signals Associated with Ethernet-TSN Subsystem Signal Description

Signal Name	Package Name	Type (Voltage Domain)	Direction	Description
SGMII_AUXTS	GPP_S0 / SNDWO_CLK	CMOS (1.8V)	Input	Auxiliary Time Stamp Trigger This edge-sensitive input signal triggers the storing of the time stamp into a 4x64 deep FIFO on its rising edge. If not used, this signal must be tied to GND through 20kOhm internal resistor.
SGMII_INT	GPP_S1 / SNDWO_DATA	CMOS (1.8V)	Input	Interrupt This configurable input signal is driven by the External SGMII PHY device. If not used, this signal must be tied to GND through 20kOhm internal resistor
SGMII_RESET_N	GPP_S2 / SNDW1_CLK / DMIC_CLK_B0	CMOS (1.8V)	Output	PHY Reset This output signal is used to reset the External SGMII device. If not used, should be left as a No Connect.
SGMII_PPS	GPP_S3 / SNDW1_DATA / DMIC_CLK_B1	CMOS (1.8V)	Output	Pulse-Per-Second (PPS) This output signal is generated as a pulse by Ethernet-TSN Controller each time its system timer indicates a new "seconds" value. If not used, should be left as a No Connect.

4.5.2 Other Signal Associated with Ethernet-TSN Subsystem Routing Guidelines

For Other Signal Associated with Ethernet-TSN Subsystem routing guidelines, refer to the GPIO point-to-point routing guidelines in the "607872_TGL_UP3_PDG_Rev*.xlsx" in (RDC #607872) in "PCH GPIO" tab.

Strapping resistor is not required since the Voltage Domain Type is CMOS.



GPY PHY RESET_N signal requires an RC delay circuitry to generate at least 2ms or higher rise time for RC reset. This rise time is required to stabilize the GPY PHYs. Refer to GPY HDK HW collateral for design reference.

4.6 Ethernet-TSN and Ethernet Pin Mapping to External PHY Platform Design

This section shows one of many combinations of External PHYs interfaces arrangements.

Figure 6 shows a typical Ethernet-TSN interface to an External PHY. The figure does not show the additional board components required for AC-Coupling and signal voltage-level converters if needed.

1.8V 11th Gen Intel® Core™ Processor SGMII MDC A0/0B MDC STA SGMII MDIO A0/0B MDIO TSN_OA/OB_TX Ethernet-SGMII or TSN OA/OB RX TSN 2500BASE-X SGMIL RESET N Reset SGMII INT Interrupt SGMII_PPS Test Headers SGMII AUXTS

Figure 6. 11th Gen Intel® Core™ Processor Ethernet-TSN Platform Design

11th Gen Intel® Core™ processors support concurrent Ethernet and Ethernet-TSN port. 11th Gen Intel® Core™ processors support an additional two Ethernet-TSN Ports. Only one Ethernet-TSN port can be enabled. This makes one port of Ethernet 1Gb/ Intel vPro® Technology capable Ethernet and one port of 2.5Gb/TSN capable Ethernet. A total of two Ethernet ports can be enabled simultaneously. Refer to the 11th Gen Intel® Core™ Processor-UP3 EDS Addendum (RDC #608733), Chapter 5: Flexible High-speed Input/Output (HSIO), for a description of how these signals are routed to and selected by the FIA/MODPHY.

Refer to the 11th Gen Intel® Core™ Processor Platform Component List (PCL) Addendum (RDC #620609) for information on different PHYs and Ethernet speed supported.



Refer to the PHY-mapping tables in this section to understand on the details the connection options.

4.6.1 Pin Mapping for GPY211/GPY215/GPY115 and I219

Table 18 shows example of Ethernet-TSN pin mapping to External PHY platform design using GPY211/215/115 and Table 19 shows example of Ethernet -TSN and Ethernet pin mapping to External PHY platform design using GPY211/215/115 and I219.

Table 18. Ethernet-TSN Pin Mapping to External PHY, GPY211/GPY215/GPY115

					-71	
"qelo"	11th Gen Intel®	11th Gen Intel® Core™	Mapping	Option 1	Mapping	Option 2
ras abdelgir	Core™ Processors Pin No	Processors Signal Name	GPY211 / 215 / 115 Pin No	GPY211 / 215 / 115 Pin Name	GPY211 / 215 / 115 Pin No	GPY211 / 215 /115 Pin Name
	CD8	TSN_0A_TX_DN	Not	Used	28	RX0_M
dha	CD9	TSN_0A_TX_DP	Not	Used	27	RX0_P
5130536A Firas abdelgha	CK2	TSN_OA_RX_DN	Not	Used	24	TX0_M
35 AL	CK1	TSN_OA_RX_DP	Not Used		25	TX0_P
CAFILO	CB7	TSN_OB_TX_DN	28	RX0_M	Not	Used
	CB8	TSN_OB_TX_DP	27	RXO_P	Not	Used
3/30	CK4	TSN_OB_RX_DN	24	TX0_M	Not	Used
	CK5	TSN_OB_RX_DP	25	TX0_P	Not Used	
	DV14	SGMII_MDC_0A	11	MDC	Not	Used
Eilis	DN10	SGMII_MDIO_0A	10	MDIO	Not	Used
536A)	DK19	SGMII_MDC_0B	Not	Used	11	MDC
13050	DM17	SGMII_MDIO_0B	Not	Used	10	MDIO
a.RS.	DT32	SGMII_AUXTS	4	GPIO11	4,00	GPIO11
28651	DR35	SGMII_INT	12	MDINT	12	MDINT
ALA3883; RS1305364 Fire	DW35	SGMII_RESET_N	1	HRSTN	1	HRSTN
	DV35	SGMII_PPS	3	GPIO12	3	GPIO12
	.00		•	73.	•	

- Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for platform routing flexibility.
- On platforms with Ethernet-TSN only, MDC/MDIO 0A or 0B can be used for platform routing flexibility.
- 3. For AUXTS and PPS connection, it could be connected when needed by validation.
- 4. For GPY211/215/115, AUXTS and PPS signal, it required Voltage Shifter 3.3V.



Table 19. Ethernet -TSN and Ethernet Pin Mapping to External PHY, GPY211/GPY215/GPY115 and I219

. 111						
hani i delghani firas abde	11th Gen Intel® Core™ Processors Pin No	11th Gen Intel® Core™ Processors Signal Name	GPY211 / 215 / 115 Pin No	GPY211 / 215 / 115 Pin Name	I219 Pin No	I219 Pin Name
.25.21	CD8	PCIE7_TXN	Not I	Jsed	42	PERN
al files	CD9	PCIE7_TXP	Not l	Jsed	41	PERP
ighall.	CK2	PCIE7_RXN	Not l	Jsed	39	PETN
hdels	CK1	PCIE7_RXP	Not l	Jsed	38	PETP
125 al	CB7	TSN_OB_TX_DN	28	RX0_M	Not	Used
	CB8	TSN_OB_TX_DP	27	RXO_P	Not Used	
	CK4	TSN_0B_RX_DN	24	TX0_M	Not	Used
wa/	CK5	TSN_OB_RX_DP	25	TX0_P	Not	Used
delglin	DV14	SGMII_MDC_0A	.01	MDC	Not	Used
3,00	DN10	SGMII_MDIO_0A	10	MDIO	Not	Used
Eiras	DK19	SML0CLK	Not l	Jsed	28	SMB_CLK
-36A '	DM17	SMLODATA	Not l	Jsed	31	SMB_DATA
13000	DT32	SGMII_AUXTS	4	GPIO11	Not	Used
51305364 Firas abdelghar	DR35	SGMII_INT	12	MDINT	Not	Used
	DW35	SGMII_RESET_N	1	HRSTN	Not	Used
O	DV35	SGMII_PPS	3	GPIO12	Not	Used
			100			

- 1. Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either OA or OB for platform routing flexibility.
- In order to implement both Ethernet -TSN and Ethernet on 11th Gen Intel[®] Core™ processors, the Ethernet-TSN port must utilize MDC/MDIO 0A.
- 3. For AUXTS and PPS connection, it could be connected when needed by validation.
- 4. For GPY211/215/115, AUXTS and PPS signal, it required Voltage Shifter 3.3V.
- For I219 others design details such as CLK_REQN, PE_RST, PE_CLK{P,N}, LAN_DISABLE_N and LANWAKE_N, please refer 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (PDG), Chapter 8: Platform Connectivity (RDC #607872).
- Not all PCH's PCIe ports can be used for LAN devices. The I219's PCIE interface pins can be connected to an appropriate 11th Gen Intel® Core™ processor PCH's PCIe Port Number 7, 8, and 9.

4.6.2 Pin Mapping for Marvell 88E2110 and I219

Table 20 shows example of Ethernet -TSN pin mapping to External PHY platform design using Marvell 88E2110 and Table 21 shows example of Ethernet -TSN and Ethernet pin mapping to External PHY platform design using Marvell 88E2110 and I219.

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Table 20. Ethernet -TSN Pin Mapping to External PHY, Marvell 88E2110

hani firas	11th Gen Intel®	11th Gen Intel® Core™	Mapping	g Option 1	Mappin	g Option 2
	Core [™] Processors Pin No	Processors Signal Name	Marvell 88E2110 Pin No	Marvell 88E2110 Pin Name	Marvell 88E2110 Pin No	Marvell 88E2110 Pin Name
abdle and the second of the se	CD8	TSN_0A_TX_DN	Not	Used	В3	SIN
25.01	CD9	TSN_OA_TX_DP	Not	Used	А3	SIP
iras abdelghani firas abde	CK2	TSN_OA_RX_DN	Not	Used	B5	SON
Johan.	CK1	TSN_OA_RX_DP	Not	Used	A5	SOP
abders	CB7	TSN_OB_TX_DN	В3	SIN	No	t Used
	CB8	TSN_OB_TX_DP	А3	SIP	No	t Used
	CK4	TSN_OB_RX_DN	B5	SON	Not Used	
	CK5	TSN_OB_RX_DP	A5	SOP	No	t Used
hal	DV14	SGMII_MDC_0A	F1 off	MDC	No	t Used
idel9.	DN10	SGMII_MDIO_0A	G1	MDIO	No	t Used
	DK19	SGMII_MDC_0B	Not	Used	F1	MDC
Fire	DM17	SGMII_MDIO_0B	Not	Used	G1	MDIO
St305364 Firas abdelghar	DT32	SGMII_AUXTS	L8	GPIO5	L8	GPIO5
6130-	DR35	SGMII_INT	E2	INT_N	E2	INT_N
	DW35	SGMII_RESET_N	A7	RESET_N	A7	RESET_N
	DV35	SGMII_PPS	K8	GPIO4	K8	GPIO4
	5		_/(2/.		

- Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either OA or OB for 1. platform routing flexibility.
- 2. On platforms with only Ethernet-TSN, MDC/MDIO 0A or 0B can be used for platform routing flexibility.
- For AUXTS & PPS connection, it could be connected when needed by validation.

Table 21. Ethernet – TSN and Ethernet Pin Mapping to External PHY, Marvell 88E2110, and 1219

Ethernet – TSN 219	l and Ethernet Pir	ո Mapping to	External PH	Y, Marvell 88	3E2110, and	o.il ch
11th Gen Intel® Core™ Processors Signal Name	11th Gen Intel® Core™ Processors Signal Name	Marvell 88E2110 Pin No	Marvell 88E2110 Pin Name	I219 Pin No	I219 Pin Name	pulab.co.il c.
CD8	PCIE7_TXN	Not	Used	42	PERN	
CD9	PCIE7_TXP	Not	Used	41	PERP	
CK2	PCIE7_RXN	Not	Used	39	PETN	
CK1	PCIE7_RXP	Not	Used	38	PETP	-omp
CB7	TSN_OB_TX_DN	В3	SIN	No	t Used	1000



nani firas.abc	11th Gen Intel® Core™ Processors Signal Name	11th Gen Intel® Core™ Processors Signal Name	Marvell 88E2110 Pin No	Marvell 88E2110 Pin Name	I219 Pin No	I219 Pin Name
	CB8	TSN_OB_TX_DP	A3	SIP	No	t Used
abde	CK4	TSN_OB_RX_DN	B5	SON	No	t Used
iras abdelghani firas abde	CK5	TSN_OB_RX_DP	A5	SOP	No	t Used
	DV14	SGMII_MDC_0A	F1	MDC	No	t Used
	DN10	SGMII_MDIO_0A	G1 MDIO		No	t Used
abole	DK19	SGMII_MDC_0B	Not	Not Used		SMB_CLK
125	DM17	SGMII_MDIO_0B	Not	Used	31	SMB_DATA
	DT32	SGMII_AUXTS	L8	GPIO5	No	t Used
	DR35	SGMII_INT	E2	INT_N	No	t Used
dhal	DW35	SGMII_RESET_N	A7-	RESET_N	No	t Used
	DV35	SGMII_PPS	K8	GPIO4	No	t Used
og A. Firas abdeligha		rnet-TSN data lanes (i. form routing flexibility.		(TX,RX}_D{N,P}) c	an use either 0 <i>4</i>	or OB for

- Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for 1. platform routing flexibility.
- In order to implement both Ethernet-TSN and Ethernet on 11th Gen Intel® Core™ processors, the Ethernet-TSN port must utilize MDC/MDIO 0A.
- For AUXTS & PPS connection, it could be connected when needed by validation.
- For I219 others design details such as CLK REQN, PE RST, PE CLK{P,N}, LAN DISABLE N and LANWAKE_N, please refer 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (PDG), Chapter 8: Platform Connectivity (RDC #607872).
- Not all PCH's PCIe ports can be used for LAN devices. The I219's PCIE interface pins can be connected to an appropriate 11th Gen Intel® Core™ processor PCH's PCIe Port Number 7, 8, and 9.

Pin Mapping for Marvell 88E1512 and I219

Table 22 shows example of Ethernet-TSN pin mapping to External PHY platform design using Marvell 88E152 and Table 23 shows example of Ethernet-TSN and Ethernet pin mapping to External PHY platform design using Marvel 88E1512 and I219.

Table 22. Ethernet-TSN to External PHY, Marvell 88E1512

11th Gen Intel® Core™ Processors Pin No	11th Gen Intel® Core™	Mappi	ng Option 1	Mapping Option 2		
	Processors Signal Name	Marvell 88E1512 Pin No	Marvell 88E1512 Pin Name	Marvell 88E1212 Pin No	Marvell 88E1512 Pin Name	
CD8	TSN_0A_TX_DN	В3	SIN	N N	ot Used	
CD9	TSN_0A_TX_DP	А3	SIP	N	ot Used	
CK2	TSN_0A_RX_DN	B5	SON	Not Used		



					OL-J	/
::35.30	11th Gen Intel®	11th Gen Intel® Core™	Маррі	ng Option 1	Mappii	ng Option 2
hani firas.abu	Core™ Processors Pin No	Processors Signal Name	Marvell 88E1512 Pin No	Marvell 88E1512 Pin Name	Marvell 88E1212 Pin No	Marvell 88E1512 Pin Name
	CK1	TSN_OA_RX_DP	A5	SOP	No	ot Used
iras abdelghani firas abd	CB7	TSN_OB_TX_DN	N ₁	ot Used	В3	SIN
: , 35.01	CB8	TSN_OB_TX_DP	130. N	ot Used	А3	SIP
ni fili	CK4	TSN_OB_RX_DN	N ₁	ot Used	B5	SON
Johan	CK5	TSN_OB_RX_DP	N	ot Used	A5	SOP
abders	DV14	SGMII_MDC_0A	F1	MDC	No.	ot Used
	DN10	SGMII_MDIO_0A	G1	MDIO	No	ot Used
	DK19	SGMII_MDC_0B	N	ot Used	F1	MDC
	DM17	SGMII_MDIO_0B	N ₁	ot Used	G1	MDIO
in a second	DT32	SGMII_AUXTS	13	LED<1>	13	LED<1>
idel9'	DR35	SGMII_INT	12	LED<2>/INT_N	12	LED<2>/INT_N
	DW35	SGMII_RESET_N	16	RESET_N	16	RESET_N
Filipa	DV35	SGMII_PPS	13	LED<1>	13	LED<1>
S1305364 Firas abdelohe		ernet-TSN data lanes (i ing flexibility.	_	COUNT		

- 1. $Ethernet-TSN\ data\ lanes\ (i.e.,\ TSN_0\{A,B\}_{TX,RX}_D\{N,P\})\ can\ use\ either\ OA\ or\ OB\ for\ platform$ routing flexibility.
- On platforms with only Ethernet-TSN, MDC/MDIO 0A or 0B can be used for platform routing flexibility.
- 3. For AUXTS & PPS connection, it could be connected when needed by validation.
- For AUXTS and PPS signal are from same Pin 13. It is valid connections per datasheet. Please refer to Marvell datasheet for further clarification.

Table 23. Ethernet-TSN and Ethernet to External PHY, Marvell 88E1512, and I219

	11th Gen Intel® Core™ Processors Pin No.	11th Gen Intel® Core™ Processors Signal Name	Marvell 88E1512 Pin No	Marvell 88E1512 Pin Name	I219 Pin No.	I219 Pin Name	uab.co.il cnd
	CD8	PCIE7_TXN	2	S_INN	42	PERN	120.00
A ?	CD9	PCIE7_TXP	1	S_INP	41	PERP	Julia
	CK2	PCIE7_RXN	5	S_OUTN	39	PETN	
	CK1	PCIE7_RXP	00 4	S_OUTP	38	PETP	
	CB7	TSN_OB_TX_DN	N	ot Used	No	ot Used	
	CB8	TSN_OB_TX_DP	N	ot Used	No	ot Used	
	CK4	TSN_OB_RX_DN	N	ot Used	No.	ot Used	الام
	CK5	TSN_OB_RX_DP	N	ot Used	No	ot Used	comp
	DV14	SGMII_MDC_0A	7	MDC	No	ot Used	ai [©]
	300			300		1319	hall.



11th Gen Intel® Core™ Processors Pin No.	11th Gen Intel® Core™ Processors Signal Name	Marvell 88E1512 Pin No	Marvell 88E1512 Pin Name	I219 Pin No.	I219 Pin Name
DN10	SGMII_MDIO_0A	8	MDIO	No	ot Used
DK19	SGMII_MDC_0B	Not Used		28	SMB_CLK
DM17	SGMII_MDIO_0B	No.	ot Used	31	SMB_DATA
DT32	SGMII_AUXTS	13	LED<1>	No	ot Used
DR35	SGMII_INT	12	LED<2>/INT_N	No	ot Used
DW35	SGMII_RESET_N	16	RESET_N	No.	ot Used
DV35	SGMII_PPS	13	LED<1>	No	ot Used

- Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for platform routing flexibility.
- In order to implement both Ethernet-TSN and Ethernet on 11th Gen Intel® Core™ processors, the Ethernet-TSN port must utilize MDC/MDIO 0A.
- 3. For AUXTS & PPS connection, it could be connected when needed by validation.
- For AUXTS and PPS signal are from same Pin 13. It is valid connections per datasheet. Please refer to Marvell datasheet for further clarification.
- For I219 others design details such as CLK_REQN, PE_RST, PE_CLK{P,N}, LAN_DISABLE_N and LANWAKE_N, please refer 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (PDG), Chapter 8: Platform Connectivity (RDC #607872).
- Not all PCH's PCIe ports can be used for LAN devices. The I219's PCIE interface pins can be connected to an appropriate 11th Gen Intel® Core™ processor PCH's PCIe Port Number 7, 8, and 9.



5.0 Wireless Connectivity Integration (CNVi) Design Considerations

5.1 Platform Considerations

Selecting Connectivity Solution

The platform motherboard can be designed to support discrete connectivity (either Intel or TPV), integrated connectivity (CNVi).

Note: All CNVi 2230 SKUs can support a "Hybrid Key-E" routing with no jumpers. When considering a TPV module, one should only use a Key-E module if the motherboard design is "Hybrid Key-E". A Key-A module will not fit into this scheme.

Table 24. CNVi Module SKUs

			$\Delta 1$	
SKU	M.2 Type	Wi-Fi Chains	LTE Coex (on-Module BAW Filter	Comments
JfP2 2230	2230	2x2	No	Basic 2x2
JfP2 2230 vPRO	2230 2x2		No	vPro 2x2
JfP2 SD	1216	2x2	Yes	Solder-down 2x2 with LTE Coex
JfP2 SD vPRO	1216	2x2	Yes	Solder-down vPRO 2x2 with LTE Coex
HrP2 2230	2230	2x2	S. No	Basic 2x2
HrP2 2230 vPRO	2230	2x2	No	vPro 2x2
HrP2 SD	1216	2x2	Yes	Solder-down 2x2 with LTE Coex
HrP2 SD vPRO	1216	2x2	Yes	Solder-down vPRO 2x2 with LTE Coex

Note: This is for IoT use condition solutions that are pin and functional compatible.



Table 25. Intel Discrete Module SKUs

.25.	T-	0	*		<u>D</u> 2	=
ani firas.	SKU	M.2 Type	W-Fi Chains	LTE Coex (on-Module BAW Filter	Comments	536A F
	ThP2 2230	2230	2x2	No nda	Basic 2x2	RS1305
as abdelghani firas abr	ThP2 2230 vPRO	2230	2x2	, CO No	vPro 2x2	3; RS1305364 F
Idhani I.	ThP2 2230 EMB	2230	2x2	No	Basic 2x2 EMB	
abders	ThP2 2230 vPRO EMB	2230	2x2	No	vPro 2x2 EMB	IPLA3883; F
	ThP2 SD	1216	2x2	Yes	Solder-down 2x2 with LTE Coex	13800
	ThP2 SD vPRO	1216	2x2	Yes	Solder-down vPRO 2x2 with LTE Coex	11; IPLK
18191	CcP2 2230	2230	2x2	No	Basic 2x2	
305364 Firas abdeldh	CcP2 2230 vPRO	2230	2x2	No	vPro 2x2	
SA FIL	CcP2 SD	1216	2x2	Yes	Solder-down 2x2 with LTE Coex	
A3883, RS1305364 Fi		as abde	ghani fira	35. ²¹	olghani@compulab.cc	
A3883; R51305364 Fi	130536AF	i, c	as abi	delahani firas	,abde.	ompulab.co.il
2012171; IPL	LA3883; R	31 ³⁰⁵³⁶¹	Fira	iras abdi	Solder-down 2x2 with LTE Coex Intel® Core™ Processors for IoT Platf PDG Adder	selghani@comf
March 2021				ith Gen	Intel® Core® Processors for IoT Platf PDG Adder	orms ndum
Desired	.h	n 4	lastal 6	ofisional al	1 DG Addel	



Display **6.0**

Embedded DisplayPort (eDP) Through COM Express 6.1

Figure 7. eDP Topology through COM Express Connector

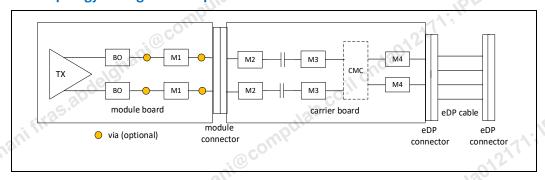




Figure 8. eDP Layout to COM Express Connector

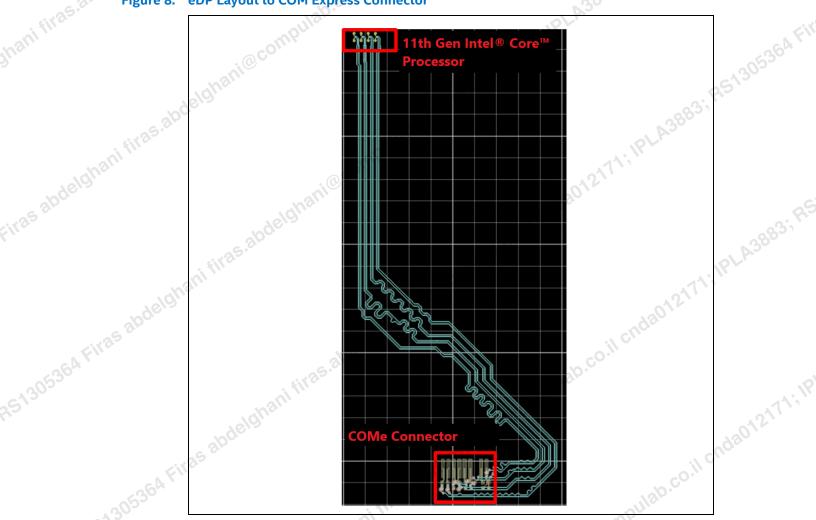


Table 26. Routing Guidelines for HBR2 (5.4 GT/s) main link or HBR3 (8.1 GT/s) with CTLE and DFE equalization or AUX

Parameter	Routing Guidelines						
Transmission Line Segment	ВО	M10	M2	М3	M4	eDP cable	
PCB Routing Layer(s)	MS/SL	MS/SL /DSL	MS	MS	MS	Cable	
Impedance (Ω)	46/0/	85				<u>;@-</u>	
Trace Width (w)	Same as main route	- Moots Impodance					
Intra Pair Line Spacing	Same as line width	Meets Impedance -				-	



70,	0.7		~9~′				
25.20	Microstrip						
nanifiras.abo	Spacing - Signal to Equivalent Signal	1.2w	3w	-			
3.	Spacing - Signal to Non- Equivalent Signal	4w	ad2012. 3W	-			
·	Stripline						
Firas abdelghani firas abd	Spacing - Signal to Equivalent Signal	1.2w	12	A30-			
	Spacing - Signal to Non- Equivalent Signal	4w	4.3w -				
abole	Dual Stripline Dual Stripline						
idhi	Spacing - Signal to Equivalent Signal	-	b.co.il	-			
	Spacing - Signal to Non- Equivalent Signal	-	3.5w	-1: IP			
	Reference	,@co.	VSS	2121			
305364 Firas abders	Max. Trace Segment Length (mm)	13	<u>25</u>	381mm for HBR2 and AUX, 355mm for HBR3			
251303	Max. COM Express Module or Carrier Board Length	101.6	101.6mm 127mm				
	Max. Total Trace Segment Length	s.abde	381mm for HBR2 and AUX, 355mm for HBR3				

- 1. AUX does not need common mode choke (CMC).
- 2. Max. three vias, no limit for AUX
- Reference plane for micro-strip route: Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- Reference plane for stripline and dual stripline route: Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 5. CMC is optional. Murata DLP11SA900HL2. Will not reduce the supported length.
- AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance, for AUX 75 nF to 200 nF including tolerance).
- 7. Cable assembly impedance: $80-100\Omega$ including tolerance. For AUX 75 to 100Ω including tolerance.
- The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872)
- Length matching between P and N within a differential pair: Within layer max: 250μm, Total length max: 125μm.
- 10. Length matching between pair to pair (inter pair), within 25mm.
- 11. It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.

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Table 27. Routing Guidelines for HBR3 (8.1 GT/s) with CTLE only

ani firas.	Parameter		F	Routing Gu	ıidelines				
	Transmission Line Segment	ВО	M1	M2	M3	M4	eDP cable		
	PCB Routing Layer(s)	MS/SL	MS/SL/ DSL	MS	MS	MS	Cable		
ghani firas ab	Impedance (Ω)	0	20.,	85			138		
firas	Trace Width (w)	Same as main route	Meets Impedance			-			
	Intra Pair Line Spacing	Same as line width		Meets iiiit	bedance	57,	-		
	delgi		Microstrip	-11	CLIC				
	Spacing - Signal to Equivalent Signal	1.2w	11.	70.CO.			-		
101	Spacing - Signal to Non- Equivalent Signal	4w	compu	3w	1		2.773		
		hanie	Stripline			_6	130		
	Spacing - Signal to Equivalent Signal	1.2w 4.3w				-			
odelgh	Spacing - Signal to Non- Equivalent Signal	4.3w					-		
	islahar	Dual Stripline							
	Spacing - Signal to Equivalent Signal	-	i alghai	2.5			-, 676		
-36A F	Spacing - Signal to Non- Equivalent Signal	- 25.0	pae	3.5	N		20.CO.11		
	Reference	i fill	•	VSS	5	apu			
`	Max. Trace Segment Length (mm)	13	-	-	a la company	25	355mm		
51 ³⁰⁵³⁶⁴ Fi	Max. COM Express Module or Carrier Board Length	50.9n	nm	abdel	63.7mm		-		
	Max. Total Trace Segment Length		112	1.6mm			355mm		
			97.						

- 1. AUX does not need common mode choke (CMC).
- 2. Number of vias allowed: Max. three vias, no limit for AUX
- 3. Reference plane for micro-strip route: Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 4. Reference plane for stripline and dual stripline route: Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 5. CMC is optional. Murata DLP11SA900HL2. Will not reduce the supported length.
- 6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance, for AUX 75 nF to 200 nF including tolerance).



- 7. Cable assembly impedance: $80\text{-}100\Omega$ including tolerance. For AUX 75 to $100~\Omega$ including tolerance.
- Length matching between P and N within a differential pair: Within layer max: 250μm, Total length max: 125μm.
- 9. Length matching between pair to pair (inter pair), within 25mm.
- It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitor pads is not necessary.
- 11. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872)

Table 28. Estimated Insertion Loss (dB) for HBR2 and HBR3

Cable Length	Estimated In	sertion Loss (dB)
Cable Length	HBR2	HBR3
25mm	-0.41	-0.62
355mm	- 1/1/3/2	-5.10
381mm	-5.10	1

6.2 DisplayPort Type-C Port (DP TCP) Through COM Express Connector

Figure 9. Topology through Com Express Connector with Retimer

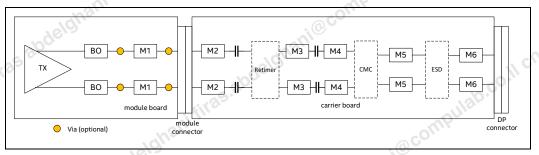


Table 29. Routing Guidelines for Topology through COM Express Connector with Retimer

	4817						
	Parameter	Routing Guidelines					
C.	Transmission Line Segment	ВО	M1	M2	М3	M4+M5+M6	
,3883; RS	PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS	MS/SL/DSL	MS	
	Impedance (Ω)	- 2006	85 Na ⁽¹⁾				
71: IPLACE	Trace Width (w)	Same as main route	Managhadela,				
21	Intra Pair Line Spacing	Same as line width	- Meets Impedance				



100"						
::35.30	12/	o.co.	Microstrip		A380	
shani firas abu	Spacing - Signal to Equivalent Signal	1.2w		-171; IP		
	Spacing - Signal to Non-Equivalent Signal	4w	ii chdal	312,	3w	. P.S
aloc		10	Stripline			1388.21
ani firas.	Spacing - Signal to Equivalent Signal	1.2w			11:1	
siras abdelghani firas.abd	Spacing - Signal to Non-Equivalent Signal	4w		-170	1.3w	
Firas	abdela		Dual Stripline	co.il o		
	Spacing - Signal to Equivalent Signal	-	Sonial).		
abdelgh	Spacing - Signal to Non-Equivalent Signal	-	© COLL	\$	3.5w	12012177
:: 135 '01	Reference	16/9/		VSS	:/ C//	
-S1305364 Firas abdelor	Max. Trace Segment Length (mm)	13	-	-	ap.co.	-
61305	Max. Via Count	1	1	0,00	1	0
52	Max. Total Length		406.6mm	©CO.,	89	mm
	76,2					

- 1. Number of vias allowed: Max. three vias.
- 2. Reference plane for micro-strip route: Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 3. Reference plane for stripline and dual stripline route: Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 4. CMC is optional. PCB CMC or Murata NFP0QHB372HS2. Will not reduce the supported length.
- 5. ESD: Infineon ESD102-U4-05L (I/O-to-GND Capacitance ≤0.65pF).
- 6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
- 7. Retimer assumed DP specification reference with CTLE+DFE EQ.
- 8. Length of retimer to DP connector superseded by retimer vendor recommendations.
- 9. Length matching between P and N within a differential pair: Within layer max: 250um, Total length max: 125um.
- 10. Length matching between pair to pair (inter pair), within 25mm.
- 11. It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
- 12. Unused data signals should be left unconnected at the BGA ball.
- 13. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872)
- Max. date rate: 8.1 GT/s (HBR3). For topology without retimer with data rate of 5.4 GT/s (HBR2), see the section on DP DDI.



6.3 DisplayPort Digital Display Interface (DP DDI) Through COM Express Connector

Figure 10. Main Link Topology through COM Express Connector

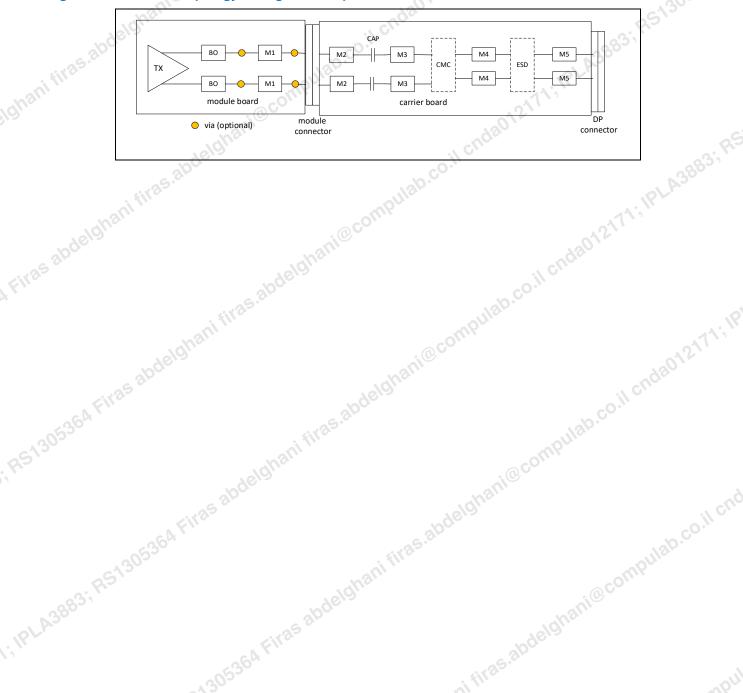




Figure 11. Main Link Layout to COM Express Connector (for both TCP and DDI, no AUX is shown)

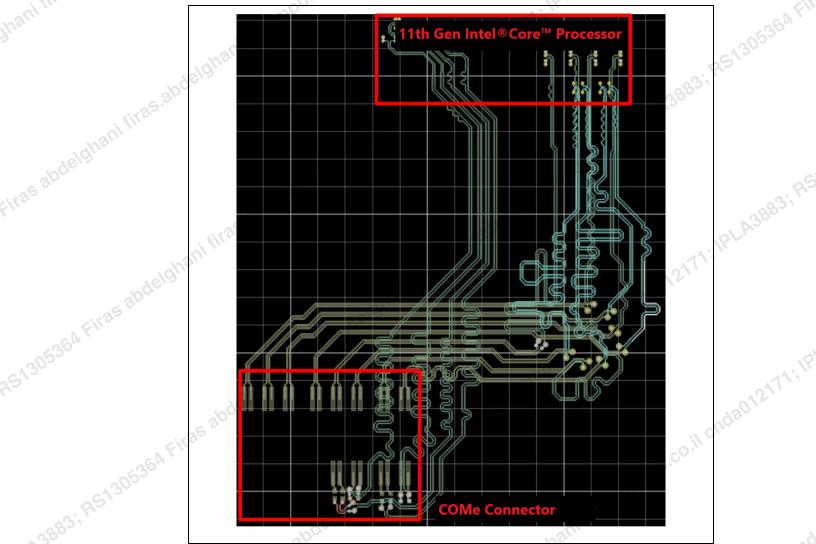


Table 30. Routing Guidelines for DP DDI

Routing Guidelines for DP I	DDI	abd	eldyam			co.il
Parameter	. 1	Routing Guidelines				Ilalo.
Transmission Line Segment	во	M1	M2	МЗ	M4+M5	
PCB Routing Layer(s)	MS/SL	MS/SL/DSL MS		MS	1	
Impedance (Ω)	3.5	85				1
Trace Width (w)	Same as main route	Meets Impedance				
Intra Pair Line Spacing	Same as line width	Idh	Meets im	pedance		@com



i firas.abc	Parameter		elines	
ani filo	ompuls.	Microstrip		
1/10	Spacing - Signal to Equivalent Signal	1.2w	1301211	2
<i>101</i>	Spacing - Signal to Non- Equivalent Signal	4w	100	3w
:va5.at		Stripl	ine	0LA30
airas abdelghani firas.	Spacing - Signal to Equivalent Signal	1.2w		4.3w
abders	Spacing - Signal to Non- Equivalent Signal	4w	and	4,3W
Firas	abders	Dual Str	ipline	
	Spacing - Signal to Equivalent Signal	-	IIIgh.	3.5w
delgh	Spacing - Signal to Non- Equivalent Signal	i@con,,		5.5W
s alou	Reference	'dhall	VSS	andae
305364 Firas abders	Max. Trace Segment Length (mm)	13		- 36.7
-S13053U	Max. COM Express Module or Carrier Board Length	93.1mm	mpul	46.8mm
2 -0	Max. Total Trace Segment Length		139.9mn	n
4				

- 1. Number of vias allowed: Max. three vias.
- 2. Reference plane for micro-strip route: Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 3. Reference plane for stripline and dual stripline route: Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 4. CMC is optional. PCB CMC or Murata NFPOQHB372HS2. Will not reduce the supported length.
- 5. ESD: Infineon ESD102-U4-05L (I/O-to-GND Capacitance ≤0.65pF).
- 6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
- Length matching between P and N within a differential pair: Within layer max: 250μm, Total length max: 125μm.
- 8. Length matching between pair to pair (inter pair), within 25mm.
- It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
- 10. DP_COMP_OBSN: 150Ω +/-1% pulldn to VSS. Provide good noise isolation. Platform RDC <0.2 Ω .
- DP_COMP_OBSN no connect: DP_COMP_OBSN can be unconnected if none of the DDI ports (DP, HDMI, eDP) are used.
- 12. DISP_UTILS: Recommend 50Ω nominal trace impedance with reasonable noise isolation. Requires level shifting on the platform.
- 13. Max. data rate: 5.4 GT/s (HBR2)
- 14. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).



6.4 Display Port Auxiliary (DP AUX) Through COM Express Connector

Figure 12. Main Link Topology through COM Express Connector

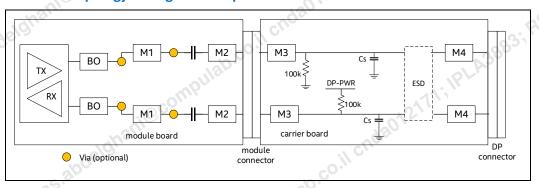


Table 31. Routing Guidelines for Main Link

				-4-1	1
Parameter	:@c0	Routing Guid	delines	151,	
Transmission Line Segment	ВО	M1+M2	M3 00	M4	
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS/SL/DSL	MS/SL/DSL	
Impedance (Ω)	-	اما	85		
Trace Width (w)	Same as main route	Meets Impedance		-171; IP	
Intra Pair Line Spacing	Same as line width		015,		
35	Microstrip			oill cit	
Spacing - Signal to Equivalent Signal	1.2w		amaulal	b.c.	
Spacing - Signal to Non- Equivalent Signal	4w	4	3w		
abde	Stripline	han			-70
Spacing - Signal to Equivalent Signal	1.2w	abdels	4.3w		o.co.il ci
Spacing - Signal to Non- Equivalent Signal	4w Allia				

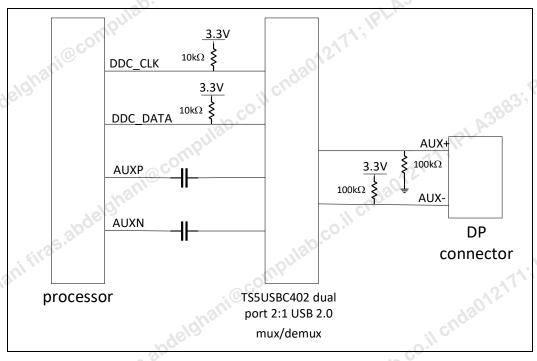


ng - Signal to Equivalent l	-	165		
		-173	2.5	
ng - Signal to Non- alent Signal	- 3.5v		3.5W	
ence	11 61.	VSS	23:	
race Segment Length	25	_	- 25	
	240.3m	m	171.6mm	
Max. Total Trace Segment 411.9mm				
ו ו	Frace Segment Length COM Express Module or Practice Board Length Fotal Trace Segment	COM Express Module or Probable Trace Segment Length 25 Com Express Module or Probable Trace Segment Length 240.3m	Pence VSS Trace Segment Length 25 - COM Express Module or Pr Board Length 240.3mm Total Trace Segment 411.9m	

- Number of vias allowed: No explicit limit for number of vias, use best known routing practices.
- 2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 4. ESD: Infineon ESD102-U4-05L, ESD102-U1-02ELS, or equivalent.
- AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
- Cs cap value: nominal 100pF. This is for optional edge rate control to comply with VESA "AUX Channel PHY SCR v6".
- 7. Length matching between P and N within a differential pair: - Within layer max: 250µm, Total length max: 125 µm.
- 8. Length matching between pair to pair (inter pair), within 25mm.
- Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for ESD's and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
- Unused data signals should be left unconnected at the BGA ball.
- The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core® Processor UP3 UP4 Platform Design Guide (RDC #607872).
- Optional Edge Rate Control: To comply with VESA "AUX Channel PHY SCR v6", an edge rate reduction mechanism such as a 100pF capacitor to VSS may be placed on each AUX signal before



Figure 13. AUX Dual Mode Circuit



Note: This can be implemented with a multiplexer as in example shown. This example does not include the edge rate control.

6.5 HDMI Port Type-C Port (HDMI TCP) Through COM Express Connector

Figure 14. Retiming Level Shifter HDMI TCP with COM Express Connector

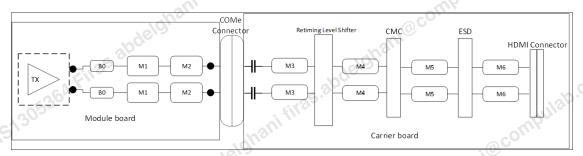




Table 32. Routing Guidelines for HDMI TCP Topology through COM Express Connector

79,					
ni fillion	Parameter		Routing Guidel	lines	
	Transmission Line Segment	ВО	M1+M2	М3	M4+M5+M6
	PCB Routing Layer(s)	,	MS/SL/DSL	-	R
	Reference	cC	VSS		20831
i firas	Max. Length Segment (mm)	13	89	227.6	25
ahan.	Max. Via Count	o con.,	1	2177	1
	Max. Total Length	102	2 mm	25	2.6 mm
Firas abdelghani fili	2. Reference plan	allowed: Max. three via: e for micro-strip route:	- Continuous ground or c	ontinuous powe	er that has low

- Number of vias allowed: Max. three vias.
- 2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 4. CMC is optional. Optional Murata DLP11SA900HL2 or equivalent. Populating will not reduce the supported length
- ESD: Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ≤ 0.65pF). Optional if retimer has integrated ESD that meets discharge requirements.
- 6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
- Retiming LS: TI SN75DP159 or Parade PS8409A
- Retiming LS Trace Impedance: Trace impedance between retiming LS and HDMI connector should follow retiming LS datasheet to meet HDMI 2.0 industry specification.
- Max. Supported Frequency: 5.94Gbps.
- Retimer Sideband Communication: Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).
- Length matching between P and N within a differential pair: Within layer max: 250um, Total length max: 125um.
- 12. Length matching between pair to pair (inter pair), Within 13mm (HDMI 2.0); 25mm (HDMI 1.4).
- Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs, ESDs, and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
- Unused signals: Unused data and AUX signals should be left unconnected at the BGA ball.

Figure 15. Cost Reduced Level Shifter with COM Express Connector (2.97Gbps)

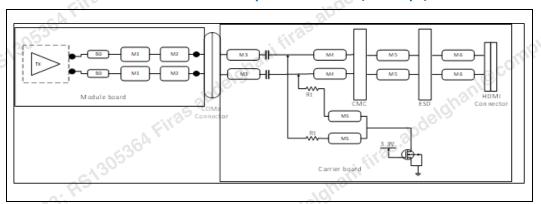




Table 33. Routing Guidelines for HDMI TCP Cost Reduced Level Shifter Topology through COM **Express Connector**

. ***								
gham'	Parameter	W.	Routing	g Guidelines	Guidelines			
	Transmission Line Segment	ВО	M1+M2	М3	M4+M5+M6	MS		
	SPCB Routing Layer(s)	MS/SL/DSL		MS				
	Reference		ulab	VSS	IPLAS			
as abdelghani I.	Max. Length Segment (mm)	13 000	30.3	31	2,111,	3		
abders	Max. Via Count	wanie	1	430,	0			
: ra5 a	Max. Total Length	0,,	87.3 mm	:// C//		13 mm		
	NOTE:)••		1380		

- Number of vias allowed: Max. two vias.
- Reference plane for micro-strip route: Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- Reference plane for stripline and dual stripline route: Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- CMC is optional. Optional Murata DLP11SA900HL2 or equivalent. Populating will not reduce the supported length
- ESD: Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ≤0.65pF). Optional if retimer has integrated ESD that meets discharge requirements.
- AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
- Rt: $470\Omega + /-5\%$. Minimize any stub in the differential pair routing due to this resistor placement. Ideally the resistor pads are placed in the differential pair traces between M3 and M4, resulting no stub at all.
- Max. nFET Ron: 10Ω.
- Max. Data Rate: 2.97 Gbps.
- Length matching between P and N within a differential pair: Within layer max: 250um, Total length max: 125um.
- Length matching between pair to pair (inter pair), Within 13mm (HDMI 2.0); 25mm (HDMI 1.4).
- Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs, ESDs, and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
- Unused signals: Unused data and AUX signals should be left unconnected at the BGA ball.

HDMI Port Digital Display Interface (HDMI DDI) Through COM Express Connector

Figure 16. Retiming Level Shifter HDMI DDI with COM Express Connector

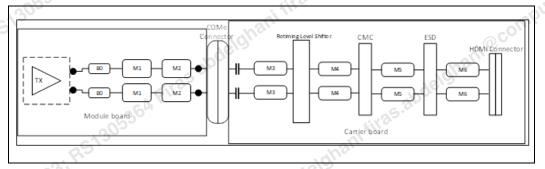




Table 34. Routing Guidelines for HDMI DDI Topology through COM Express Connector

72,		O'Y					
ni fiira	Parameter	Routing Guidelines					
hair	Transmission Line Segment	ВО	M1+M2	М3	M4+M5+M6		
	PCB Routing Layer(s)		MS/SL/DSI	<u>L</u>	P.S		
	Reference		VSS		283 i		
i fil'asi	Max. Length Segment (mm)	13	89	227.6	25		
, aham	Max. Via Count	ocon.,	1	2177			
ndel9	Max. Total Length	10)2 mm	25	2.6 mm		
Firas abdelghani firas	2. Reference plane	1. Number of vias allowed: Max. three vias.					

- Number of vias allowed: Max. three vias.
- 2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 4. CMC is optional. Optional Murata DLP11SA900HL2 or equivalent. Populating will not reduce the supported length
- 5. ESD: Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ≤ 0.65pF). Optional if retimer has integrated ESD that meets discharge requirements.
- 6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
- Retiming LS: TI SN75DP159 or Parade PS8409A
- Retiming LS Trace Impedance: Trace impedance between retiming LS and HDMI connector should follow retiming LS datasheet to meet HDMI 2.0 industry specification.
- 9. Max. Supported Frequency: 5.94Gbps.
- Retimer Sideband Communication: Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).
- Length matching between P and N within a differential pair: Within layer max: 250um, Total length max: 125um.
- 12. Length matching between pair to pair (inter pair), Within 13mm (HDMI 2.0); 25mm (HDMI 1.4).
- Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs, ESDs, and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.

Figure 17. Active Level Shifter with COM Express Connector

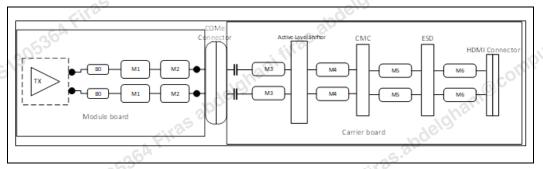




Table 35. Routing Guidelines for HDMI DDI Topology with Active Level Shifter through COM **Express Connector**

. *///							
hani .	Parameter	16.	.0				
eit ^{ro}	Transmission Line Segment	ВО	M1+M2	МЗ	M4+M5+M6		
	SPCB Routing Layer(s)		co.ill of MS	/SL/DSL	3883;		
	Reference		Julab.	VSS	IPLA		
as abdelghani .	Max. Length Segment (mm)	13	89	114.6	76		
abders	Max. Via Count	wain!		1 430			
::r25 a	Max. Total Length	<i>(</i> 9),	102 mm	il cus	190.6 mm		
	NOTE:		, ab. c).	A386		

- 1. Number of vias allowed: Max. three vias.
- 2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- 3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
- CMC is optional. Optional Murata DLP11SA900HL2 or equivalent. Populating will not reduce the supported length
- ESD: Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ≤ 0.65pF). Optional if retimer has integrated ESD that meets discharge requirements.
- 6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
- ALS: Parade PS8203 or equivalent
- 8. Max. Data Rate: 2.97 Gbps.
- 9 Retimer Sideband Communication: Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).
- Length matching between P and N within a differential pair: Within layer max: 250um, Total length max: 125um. 10.
- Length matching between pair to pair (inter pair), Within 13mm (HDMI 2.0); 25mm (HDMI 1.4). 11.0
- Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs, ESDs, and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary

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Universal Serial Bus 3.2 (USB 3.2) 7.0

Note: The design guides for USB in this addendum assumes the transceiver is on the PCH and not on the Type-C ports.

USB 3.2 Gen 2 Through COM Express Connector

Figure 18. PCH through COM Express connector with Redriver

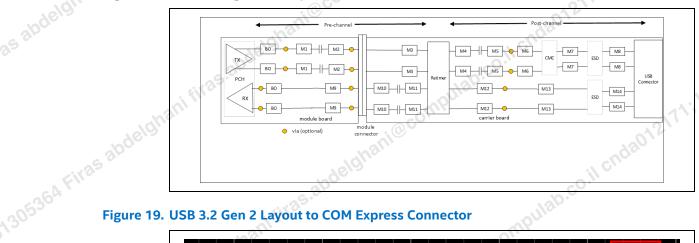


Figure 19. USB 3.2 Gen 2 Layout to COM Express Connector

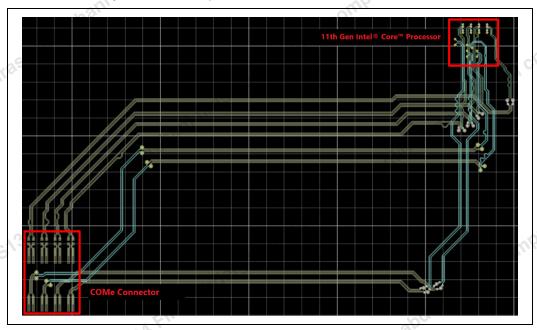




Table 36. Routing Guidelines for Redriver Topology through COM Express Connector

~ G) *		7(0) .					
i firas	Parameter		Rou	uting Gui	delines		
i firas.	Transmission Line Segment	ВО	(M1+M2) or M9	M3 or (M10 + M11)	(M4 + M5) or M12	(M6 + M7) or M13	M8 or M14
delghanifiras abr	PCB Routing Layer(s)	MS/SL	MS/SL/DSL		MS	5 IPLA	30
SUI.	Impedance (Ω)	OWA			80	175	
	Trace Width (w)	Same as main route		Ma	19801,5		
	Intra Pair Line Spacing	Same as line width		Mee.	ets Impedance		
	· fillas.			10			
ndelgh	Spacing - Signal to Equivalent Signal	2w	ni@comb		4w	1201	2171
bdelgh	Spacing - Signal to Non-Equivalent Signal	3w			4.5w	II choc	
	117	(33	Stripline		oular		
	Spacing - Signal to Equivalent Signal	2.67w	200	ni@cor	6w		
264 Fi	Spacing - Signal to Non-Equivalent Signal	4w	s.abdelgli		6.67w	~\0	co:II ch
9		ni fir	Dual Stripli	ne			
05 ^{36A} Fi	Spacing - Signal to Equivalent Signal	odelohar			4.5w),,	
	Spacing - Signal to Non-Equivalent Signal	-	. ماد	s.abde	5w		
	Reference		ni fili	VSS			who is
283, P.S	Max. Trace Segment Length	10.2 mm	Max. len	gth inforr	mation depend	ds on Redriv	ver
LA30	Via Count	1 3	1	0	1	0	0
	1	4.7	·			0.1-	

- It is strongly recommended to use ESD protection devices on each USB data signal. 1.
- Length matching between P and N within a differential pair: Within layer max: 0.254mm, Total length max: 0.127mm.
- Channel and Via stub requirement must meet <381µm for both Tx and Rx signal pairs.



- 4. Reference plane: continuous ground is recommended. If continuous ground cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- Voiding recommendation for mainstream stackup: It is recommended to void pads for all
 components, for example, AC caps as well as connector pads to optimize the impedance
 matching in the channel.
- Discrete component part size for mainstream stackup: It is recommended to use 0402 or smaller component sizes.
- 7. AC coupling capacitor value nominal 100nF (75nF to 265nF according to USB specification).
- 8. It is recommended to place the AC coupling capacitors near the transmitter sides of the re-driver as shown in the topology diagram.
- 9. Important guidelines on repeater/active multiplexer topologies: Max. pre-channel length depends on what the specific repeater selected can compensate for at 10 GT/s speed when used in conjunction with Intel PCH. Please work with the repeater vendor for specific routing recommendations. The afore mentioned DG is superseded by vendor recommendations. In addition, it is recommended to refer to repeater integration white paper *USB 3.1 Repeater Integration Technical White Paper* (RDC #571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
- 10. Max. no. of vias is three on each trace from PCH to USB connector.

7.2 USB 3.2 Gen 1 Through COM Express Connector

Figure 20. External with COM Express Connector

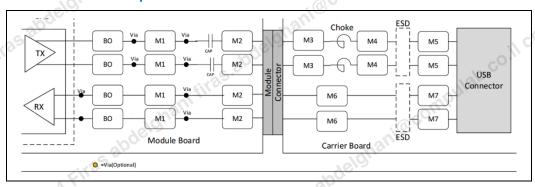


Table 37. Routing Guidelines for USB 3.2 Gen 1 Topology Through COM Express Connector

Parameter	Routing Guidelines					
Transmission Line Segment	во	M1	M2	(M3+M4) or M6	M5 or M7	
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS			
Impedance (Ω)	-	985				
Trace Width (w)	Same as main route	Meets Impedance				



1 - UP						
::35.30	Parameter		Routing	Guidelines		
thanifiras.abu	Intra Pair Line Spacing	Same as line width	-17	. IP		
9,	nio	•	Microstrip			-19
	Spacing - Signal to Equivalent Signal	1.2w	il cho.	3w		283; R5.
i firas.a	Spacing - Signal to Non- Equivalent Signal	4w		3W	IPLA	
han		count	Stripline	017	1	
firas abdelghani firas al	Spacing - Signal to Equivalent Signal	1.2w		4.3w		
Firas	Spacing - Signal to Non- Equivalent Signal	4w	's.co.il'	4.5W		
	ai fili sa	D	Oual Stripline			IPL
deld	Spacing - Signal to Equivalent Signal	00	on.,	3.5w	o'	2177
305364 Firas abder	Spacing - Signal to Non- Equivalent Signal	delapar.		3.5W	cudan	
GA FIL	Reference	io C.	V	/SS		
E130530	Max. Trace Segment Length	15.2mm	-	10.2mm	-	15.2mm
23	Max. Via Count	1	1,00	0	0	0
<	Max. COM Express Module or Carrier Board Length	rd 78.2mm 125m			5mm chdal	
, 30536A.	Max. Total Trace Segment Length	, 411'35.3L	203	.2mm	aulab	,C
_ A D =						

- 1. It is strongly recommended to use ESD protection devices on each USB data signal.
- Length matching between P and N within a differential pair: Within layer max: 0.254mm, Total length max: 0.127mm.
- 3. Channel and Via stub requirement must meet $<381\mu m$ for both Tx and Rx signal pairs.
- 4. Reference plane continuous ground is recommended. If continuous ground cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- Voiding recommendation for mainstream stackup. It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
- Discrete component part size for mainstream stackup, recommended to use 0402 or smaller component sizes.
- 7. AC coupling capacitor value: nominal 100nF (75nF to 265nF according to USB specification).
- 8. Max. no. of vias is two on each trace from PCH to USB connector.



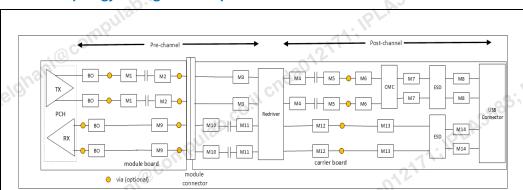


Figure 21. Redriver Topology through COM Express Connector

Firas abdelghani firas abd Table 38. Routing Guidelines for Redriver Topology through COM Express Connector

	Parameter	Routing Guidelines				10.	
5364 Firas abdelgh	Transmission Line Segment	ВО	(M1 + M2) or M9	M3 or (M10 + M11)	(M4 + M5) or M12	(M6 + M7) or M13	M8 or M14
	PCB Routing Layer(s)	MS/SL	MS/SL/DSL			MS	
iras	Impedance (Ω)	200gers			85	0.11	
	Trace Width (w)	Same			130.		
	Intra Pair Line Spacing	as main route		Mee	ets Impedan	ce	
	"pdeles		Micros	trip			۸'
F	Spacing - Signal to Equivalent Signal	1.2w	abdeldy				o.co.il cnd
36 ⁴ Fi	Spacing - Signal to Non-Equivalent Signal	4w	Was.c		3w	ompula	0.0
	600	eld _I	Stripl	ine	nio!		
	Spacing - Signal to Equivalent Signal	1.2w		6	lahar		
	Spacing - Signal to Non-Equivalent Signal	4w	i fi	ras.abde	4.3w		abul.
1. IPLA3883; R.	Signal Signal	25	abdelghan	odelghar		alghair	ioco.
	30538	54 Fire			i firas.al		
	,3883; RS13			odelghan			
PDG Addendur	[®] Core™ Processors for IoT	Platforms	-364 Firas			N	1arch 2021
54		Intel	Confidential		Document	Number: 6	08734 -2.1



10	p.co.	Dual St	ripline	, A38°)	
Spacing - Signal to Equivalent Signal	-		-17	ilbr		
Spacing - Signal to Non-Equivalent Signal	-	., cr	193012,	3.5w		. RS1
Reference		CO.//	VS:	S		28837
Max. Trace Segment Length	15.2 mm	Max. I	ength inforn	nation depend	ds on Redriv	ver
Max. Via Count	OCD//	1	0	1,01	0	0
Max. Total Trace Segment Length		Max. length	information	depends on	Redriver	

- 1. Let it is strongly recommended to use ESD protection devices on each USB data signal.
- 2. Length matching between P and N within a differential pair: Within layer max: 0.254mm, Total length max: 0.127mm.
- 3. Channel and via stub requirement must meet <381µm for both Tx and Rx signal pairs.
- 4. Reference plane continuous ground is recommended. If continuous ground cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- Voiding recommendation for mainstream stackup: it is recommended to void pads for all
 components for example AC caps as well as connector pads to optimize the impedance matching in
 the channel.
- Discrete component part size for mainstream stackup: t is recommended to use 0402 or smaller component sizes.
- 7. AC coupling capacitor value: nominal 100nF (75nF to 265nF according to USB specification).
- 8. It is recommended to place the AC coupling capacitors near the transmitter sides of the re-driver as shown in the topology diagram.
- 9. Important guidelines on repeater/active multiplexer topologies: Max. pre-channel length depends on what the specific repeater selected can compensate for at 5 GT/s speed when used in conjunction with Intel PCH. Please work with the repeater vendor for specific routing recommendations. The aforementioned DG is superseded by vendor recommendations. In addition, it is recommended to refer to repeater integration white paper USB 3.1 Repeater Integration Technical White Paper (RDC #571574). The white paper illustrates in detail the fundamental differences between different repeater types (Redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
- The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).
- 11. Max. no. of vias is three on each trace from PCH to USB connector.

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8.0 PCIe Gen 3 (PCH PCIe)

8.1 Gen 3 Device Down with COM Express Connector

Figure 22. Gen 3 Device Down with COM Express Connector

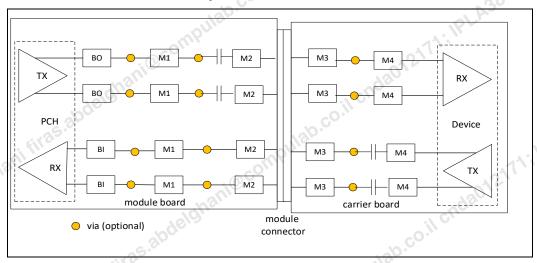


Table 39. Routing Guidelines for Gen 3 Device Down with COM Express Connector - TX

				<u>-0-</u>		
	Parameter		Routin	g Guidelines		
, Ei	Transmission Line Segment	во	M1	M2	M3+M4	
36A	PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS	MS/SL/DSL	
13050	Impedance (Ω)	ni-fill	85			
IPLA3883; RS1305364 Fil	Trace Width (w)	same as main route	ii@coh			
	Intra Pair Line Spacing	same as line width	Meets Impedance			
	-36A		Microstrip			
Q	Spacing - Signal to Equivalent Signal	2w	hanifile	3w	comi	
,3883;	Spacing - Signal to Non-Equivalent Signal	3w	(9)	3w	hani@8	
IPLA		ciras	Stripline		gelg.	
nda012171; IPLA3883; Rs	Spacing - Signal to Equivalent Signal	2.67w		4.3w	~	
ndae	Spacing - Signal to Non-Equivalent Signal	4w	. 819	4.3w		
	0.00	•	0			



difiras.abu	, 20.	CO.	Dual Stripline	, P	380
hani filo	Spacing - Signal to Equivalent Signal	-		4w	
31.	Spacing - Signal to Non-Equivalent Signal	-	2930	4w	
	Reference		11 C1	VSS	31
siras.ab	Max. Trace Segment Length	15.2mm	.co	-	.DLA380
ani II	Max. Via Count	amp		3	.115
as abdelghani file	Max. COM Express Module or Carrier Board Length		85.0mm	snda0'	118.6mm
riva.	Max. Total Trace Segment Length		- 10	203.6mm	

- 1. Number of vias allowed: max. three vias (not counting microvia under package).
- 2. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- 3. AC cap value: 176 to 265 nF; 220 nF nominal.
- 4. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm 0.16mm is allowed. The total breakout length is still 15.2 mm.
- 5. Length matching between P and N within a diff. pair: within layer max. mismatch: 254 μm, total length max. mismatch: 127 μm.
- 6. Length matching between Tx pairs of multiple lanes: not required.
- 7. Length matching between Tx and Rx pairs: not required.
- 8. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88 μm at breakout and 200 μm at main route (currently to low-speed I/O) required.</p>
- Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
- Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
- 11. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).



Table 40. Routing Guidelines for Gen 3 Device Down with COM Express Connector - RX

-G.*		70·		•			
ni firaz	Parameter	Routing Guidelines					
	Transmission Line Segment	ВІ	M1	M2	МЗ	M4	
	PCB Routing Layer(s)	MS/SL	il ch	MS/SL/DSL		MS	
25.30	Impedance (Ω)	-	. 20.CO	85	5	0.380	
	Trace Width (w)	same as main route	main route Meets Impedance				
firas.ab	Intra Pair Line Spacing						
	25.20		Microstr	ip CO			
X	Spacing - Signal to Equivalent Signal	2w	comp	3v	V	-171	
as abdelol	Spacing - Signal to Non-Equivalent Signal	3w	anio	3v	v	ind3012	
		about	Striplin	е	, co.,		
	Spacing - Signal to Equivalent Signal	2.67w		4.3	W		
	Spacing - Signal to Non-Equivalent Signal	4w		13hi 4.3	w		
	II as		Dual Strip	line		60.110	
	Spacing - Signal to Equivalent Signal	- 4	135.0	40	v	oulab.6	
30536AF	Spacing - Signal to Non-Equivalent Signal	lelalusu.		4ν	v ni@com		
	Reference			VSS			
	Max. Trace Segment Length	15.2mm		, as abo	-	8mm	
	Max. Via Count		anit	3		01	
; IPLA3883; R	Max. COM Express Module or Carrier Board Length	- 3/	85.0mm		118	3.6mm	
IPL	Max. Total Trace Segment Length	AFIRAS		203.6mm	abdell	9	
	200		·	-	03		

- 1. Number of vias allowed: max. three vias (not counting microvia under package).
- 2. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition



that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.

- 3. AC cap value: 176 to 265 nF; 220 nF nominal.
- 4. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm 0.16mm is allowed. The total breakout length is still 15.2 mm.
- Length matching between P and N within a diff. pair: within layer max. mismatch: 254 μm, total length max. mismatch: 127 μm.
- 6. Length matching between Rx pairs of multiple lanes: not required.
- 7. Length matching between Tx and Rx pairs: not required.
- 8. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200 µm at main route (currently to low-speed I/O) required.</p>
- Voiding recommendation for mainstream stackup: It is recommended to void pads for all
 components for example AC caps as well as connector pads to optimize the impedance
 matching in the channel.
- Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
- 11. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).

8.2 Gen 3 M.2 connector with COM Express Connector

Figure 23. Gen 3 M.2 connector with COM Express Connector

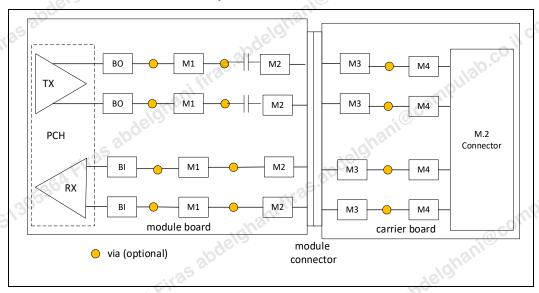




Table 41. Routing Guidelines for Gen 3 M.2 connector with COM Express Connector – TX

ni firas	Parameter		Routing Guidelines					
hani firas.	Transmission Line Segment	ВО	M1	M2	M3+M4			
	PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS	MS/SL/DSL			
do	Impedance (Ω)	-	.0.11	85	2003			
iras abdelghani firas abr	Trace Width (w)	same as main route	Meets Impedance					
4elghan.	Intra Pair Line Spacing	same as line width		larice				
as above	-Idhair.	Microstrip						
ika	Spacing - Signal to Equivalent Signal	2w	-40.C	3w				
	Spacing - Signal to Non-Equivalent Signal	3w	amballa	3w	.1^			
delgh		ni©	Stripline		20127			
Eiras abs	Spacing - Signal to Equivalent Signal	2.7w	7w 4.3w					
51305364 Firas abdeldh	Spacing - Signal to Non-Equivalent Signal	4w	4.3w					
5130	Dual Stripline							
	Spacing - Signal to Equivalent Signal	-	hani®	4w				
A FI	Spacing - Signal to Non-Equivalent Signal	- 2	pqela	4w	co.il			
	Reference	eiras.		VSS	11/3/0.			
. RS130	Max. Trace Segment Length	15.2mm	-	-	compt-			
383,	Max. Via Count			3 anie	7			
PLA3883; RS1305364 FI	Max. COM Express Module or Carrier Board Length	85.0mm 42.6mi			42.6mm			
	Max. Total Trace Segment Length		ni fira 12	27.6mm	n or			

- Number of vias allowed: 3 for Tx (not counting via under package). Express card/M.2/Add-in card vias allowed: 1 (for Tx / Rx lanes).
- 2. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed



- (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- AC cap value: 176 to 265 nF; 220 nF nominal. If multiplexing with SATA, see PCIe (cyan) tab of 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872) for further details.
- 4. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm 0.16mm is allowed. The total breakout length is still 15.2 mm.
- End-to-end maximum transmission line length: The max. length end-to-end from transmitter to receiver is 178 mm.
- 6. Add-in card at M.2 connector: The total length of the add-in card is usually 38mm to 50.4mm. The maximum breakout length on the add-in card is assumed to be 15.2 mm. The add-in card segment is a combination of MS/SL/DSL (MS where required to connect to surface mounted components). The add-in card segment has a typical via count of 1.
- Length matching between P and N within a diff. pair: within layer max. mismatch: 254μm, total length max. mismatch: 127μm.
- 8. Length matching between Tx pairs of multiple lanes: not required.
- 9. Length matching between Tx and Rx pairs: not required.
- 10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88μm at breakout and 200μm at main route (currently to low-speed I/O) required.
- Voiding recommendation for mainstream stackup: It is recommended to void pads for all
 components for example AC caps as well as connector pads to optimize the impedance
 matching in the channel.
- 12. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
- 13. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).

Table 42. Routing Guidelines for Gen 3 M.2 connector with COM Express Connector – RX

	Parameter		Ro	outing Guidelin	es	c.Y
oga Fi	Transmission Line Segment	ВІ	M1 M2 M			M4
LA3883; RS1305364 FI	PCB Routing Layer(s)	MS/SL	MS/SL/DSL MS/S			MS/SL/DSL
	Impedance (Ω)	Wau.		8	5 000	
	Trace Width (w)	same as main route				
	Intra Pair Line Spacing	same as line width				
	20530		Microstrip			
3.78	Spacing - Signal to Equivalent Signal	2w	aham.	3:	W	i@com
,PLA3883; F	Spacing - Signal to Non-Equivalent Signal	ng - Signal to Equivalent Signal 3w 3w				
171; "	,26 ⁰	FILE			5.ab0	



ni firas.abo	190	CO.	Stripline		A380	
hanifile	Spacing - Signal to Equivalent Signal	2.67w		4.3	3w	
	Spacing - Signal to Non-Equivalent Signal	4w	ada	4.3	Зw	
V	9810.	D	ual Stripline	:		2031
i filas.al	Spacing - Signal to Equivalent Signal	-ulab.		4	w	PLA300
35 abdelghani firas	Spacing - Signal to Non-Equivalent Signal	5 counts	- 4w			-
abde	Reference			VSS 30	0.	
Firas C	Max. Trace Segment Length	15.2mm	-	co.il ch	-	8mm
	Max. Via Count		113	3		
deld	Max. COM Express Module or Carrier Board Length	10	85.0mm		42	2.6mm
A Firas above	Max. Total Trace Segment Length	delahar		127.6mm	il Cr	/g/s
30536AFT		lowed: 2 for RX (no	_	a under package).	. Express card	/M.2/Add-in

- Number of vias allowed: 2 for RX (not counting via under package). Express card/M.2/Add-in 1 card vias allowed: 1 (for Tx / Rx lanes).
- Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If noncontinuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- 3. AC cap value: 176 to 265 nF; 220 nF nominal. If multiplexing with SATA, see PCIe (cyan) tab of 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872) for further details.
- Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-topair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2 mm.
- End-to-end maximum transmission line length: The max. length end-to-end from transmitter to receiver is 178 mm.
- Add-in card at M.2 connector: The total length of the add-in card is usually 38mm to 50.4mm. The maximum breakout length on the add-in card is assumed to be 15.2 mm. The add-in card segment is a combination of MS/SL/DSL (MS where required to connect to surface mounted components). The add-in card segment has a typical via count of 1.
- Length matching between P and N within a diff. pair: within layer max. mismatch: 254µm, total length max. mismatch: 127µm.
- 8. Length matching between Rx pairs of multiple lanes: not required.
- Length matching between Tx and Rx pairs: not required.
- MODPHY RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP P and RCOMP N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.



- 11. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
- 12. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
- 13. Max. length values are for all the stackups in 607872_TGL_UP3_PDG_Rev*.xlsx "U Ref Stackup" tab.

elghani firas abdalghani firas abdalghani firas abdalghani ©compulab.co.il cindantati



9.0

PCIe Clock 20.co.il cridant 2171; IPLA 3885 **PCIe Clock to Device Down Through COM Express Connector** 9.1

Figure 24. PCIe Clock to Device Down Topology Through COM Express Connector

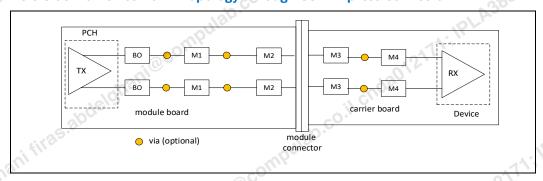


Table 43. Routing Guidelines for PCIe Clock to Device Down Topology Through COM Express Connector - Gen 4

Danie mantani	Daviding Cuidelines								
Parameter		Kou	ting Guidelines						
Transmission Line Segment	ВО	M1 M2 M3+M4							
PCB Routing Layer(s)	MS/SL	MS/SL/DSL MS/SL/DSL							
Impedance (Ω)	-	85							
Trace Width (w)	same as main route	odelo.	Moots Impoda	nco co.il c					
Intra Pair Line Spacing	same as line width	Meets Impedance							
161	ghai.	Microstrip	.0	co,,					
Spacing - Signal to Equivalent Signal	3w		5w						
Spacing - Signal to Non-Equivalent Signal	5w	25	7.6w						
1300		Stripline		m					
Spacing - Signal to Equivalent Signal	4w	No.	7.1w	ani [©] co.					
Spacing - Signal to Non-Equivalent Signal	6.7w		10.9w	delghe					



nifiras.abu	.20.	CO.,	oual Stripline	, A3	900
nani filo	Spacing - Signal to Equivalent Signal	-		6.7w	
2,	Spacing - Signal to Non-Equivalent Signal	-	2950	10.1w	
	Reference		:// C1.	VSS	3
41125	Max. Trace Segment Length	12.7mm	-	25.4mm	DLA380
ani II	Max. Via Count	amp		4	.11'
as abdelghani file	Max. COM Express Module or Carrier Board Length),50	100mm	chda01	192.1mm
Firas	Max. Total Trace Segment Length		.\0	292.1mm	
1		•	7.87		

- 1. Minimum motherboard total length: 76.2mm.
- 2. Number of vias allowed: Max. four vias.
- 3. Reference plane: continuous ground only.
- 4. EMC/RF noise protection: For signal sections which are routed on MS (surface) layer, a GND ring/shield is advised to be added (with similar guidelines following a standard GND ring/shield such as for XTAL) with sufficient GND stitching vias for the length of the MS routed layer. GND ring/shield GND stitching vias should be placed at regular intervals of 4 12mm. It is advised to route in inner layer SL/DSL routing. Limit MS routed section and follow above shielding guidelines.
- 5. Length matching between P and N within a differential pair: Within same layer mismatch: 0.254mm. Total length mismatch: 0.381mm (TX to RX).
- 6. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).
- 7. Reference plane: continuous GND is recommended. Only applicable for Gen3 clocks: if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt).

Table 44. Routing Guidelines for PCIe Clock to Device Down Topology Through COM Express Connector – Gen 3 and below

Parameter	Routing Guidelines				
Transmission Line Segment	ВО	M1 M2		M3+M4	
PCB Routing Layer(s)	MS/SL	MS/SL/DSL		MS/SL/DSL	
Impedance (Ω)	-nge,	85			
Trace Width (w)	same as main route	bdeldha			
Intra Pair Line Spacing	same as line width	Meets Impedance			



25.200	, 20	CO.	Microstrip	, A38	
hani firas abc	Spacing - Signal to Equivalent Signal	2w		3w	
	Spacing - Signal to Non-Equivalent Signal	3w	29301	3.8w	
70	8/0,		Stripline		293,
i firas al	Spacing - Signal to Equivalent Signal	2.7w		4.3w	IPLA36
tiras abdelghani firas.	Spacing - Signal to Non-Equivalent Signal	4w		5.4w	773
abde	ighani	Du	ıal Stripline	-udan.	
Firas	Spacing - Signal to Equivalent Signal	-	10.C	4w	
	Spacing - Signal to Non-Equivalent Signal	-	Mbnian	5w	11.
islahi	Reference	. 0	CO.	VSS	221
	Max. Trace Segment Length	12.7mm	-	25.4mm	., chdao.
File	Max. Via Count	po		4),"
251305364 Firas abdens	Max. COM Express Module or Carrier Board Length		100mm	OWbrilap.	192.1mm
6.0	Max. Total Trace Segment Length		nani 29	92.1mm	

- 1. Minimum motherboard total length: 76.2mm.
- 2. Number of vias allowed: Max. four vias.
- 3. Reference plane: continuous ground only.
- 4. EMC/RF noise protection: For signal sections which are routed on MS (surface) layer, a GND ring/shield is advised to be added (with similar guidelines following a standard GND ring/shield such as for XTAL) with sufficient GND stitching vias for the length of the MS routed layer. GND ring/shield GND stitching vias should be placed at regular intervals of 4 12mm. It is advised to route in inner layer SL/DSL routing. Limit MS routed section and follow above shielding guidelines.
- 5. Length matching between P and N within a differential pair: Within same layer mismatch: 0.254mm. Total length mismatch: 0.381mm (TX to RX).
- The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).
- 7. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt).



10.0 SATA

10.1 SATA with Internal Cable Through COM Express Connector

Figure 25. Direct connect with Internal Cable and COM Express Connector

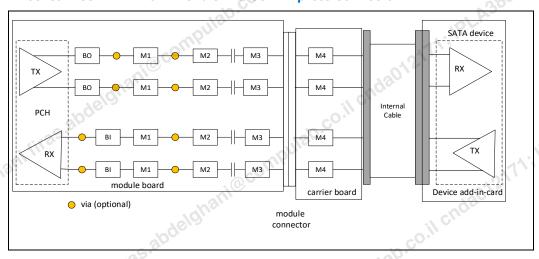


Table 45. Routing Guidelines for SATA with Internal Cable Topology Through COM Express Connector -TX

	Parameter		Ro	uting Guid	lelines		
, Fi	Transmission Line Segment	во/ві	M1	M2	M3	M4	
	PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS/SL/DSL MS MS/SL/E			
61303	Impedance (Ω)	anim			85	wbg.	
PLA3883; RS1305364 FI	Trace Width (w)	same as main route		Meets	s Impedanc	e	
IPL.	Intra Pair Line Spacing	same as line width	as index				
	3055		Microstrip	3.5			
-03. R	Spacing - Signal to Equivalent Signal	2w	46/alusil		3w	aj@com	
1: IPLA380	Spacing - Signal to Non-Equivalent Signal	3w			3w	odelahan.	
nda012171; IPLA3883; R	35130536			han	i firas.		
	283,			relal.			



1 a U						
ani firas.abu	12	o.co.	Stripline		1 A38	30
hani filo	Spacing - Signal to Equivalent Signal	2.67w	4.3w	-17	· iP	4.3w
9,	Spacing - Signal to Non-Equivalent Signal	4w	4.3w	3012	-	4.3w
ab ^c	,		Dual Striplii	ne		73862,
ani firas	Spacing - Signal to Equivalent Signal	-mpul	4w	-	-	4w
iras abdelghani firas	Spacing - Signal to Non-Equivalent Signal	(@co.	4w	-	-nda013	4w
tiras	Reference			VSS	0.	
	Max. Trace Segment Length	15.2mm	الام	ab	10mm	-
, n'i	Max. Via Count		colub	2		-17
A Firas abdelor	Max. COM Express Module or Carrier Board Length	alghar	50.8mm	1		76.2mm
-364 Fire	Max. Total Trace Segment Length	abole		127.0mi	m c	0.11
305	NOTE:	•			Julia	

- 1. Number of vias allowed: 2 vias.
- 2. Minimum total length: 50.8mm.
- AC cap value: 10nF.
- 4. Reference plane: continuous GND recommended. if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pairto-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2mm.
- Length matching between P and N within a diff. pair: Within same layer mismatch: 0.254mm,
 Total length mismatch: 0.127mm.
- 7. Length matching between Tx pairs of multiple lanes: not required.
- 8. Length matching between Rx pairs of multiple lanes: not required.
- 9. Length matching between TX and Rx pairs: not required.
- 10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88μm at breakout and 200μm at main route (currently to low-speed I/O) required.
- Cable loss vs channel length trade-off table: See SATA without Daughter Card with Internal Cable Routing Length versus Cable Loss figure
- 12. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.



- Jhani firas.abdelghani@compulab.co.ii Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes. See SATA with Daughter Card with Internal Cable Routing Length versus Cable Loss figure
 - The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872)

Table 46. Routing Guidelines for SATA with Internal Cable Topology Through COM Express **Connector -RX**

						- 0.0	-
, 411.95.°	Parameter	delile	Routi	ng Guideli	nes	PLAS	
abdelghani firas.a.	Transmission Line Segment	во/ві	M1	M2	М3	M4	
abders	PCB Routing Layer(s)	MS/SL	MS/SL/DSL	N	1 S	MS/SL/DSL	
	Impedance (Ω)	-		11 CL	85		00
	Trace Width (w)	same as main route	illab	Meets I	mpedance		IPLA3883
Idhi	Intra Pair Line Spacing	same as line width	o combr.	11000	mpedance	2171	
abdele		bani	Microstrip			9/307	
305364 Firas abdeloha	Spacing - Signal to Equivalent Signal	2w			3w	C	
30536	Spacing - Signal to Non-Equivalent Signal	3w		0	3w		
	Johan		Stripline	DCOLL.			1211
	Spacing - Signal to Equivalent Signal	2.67w	4.3w		-	4.3w	udao
-36AFII	Spacing - Signal to Non-Equivalent Signal	4w	4.3w		-	4.3w	
C13055		ni filo	Dual Stripline			mpula.	
,3883; RS1305364 Fir	Spacing - Signal to Equivalent Signal	App.	4w		-ni@co	4w	
.30	Spacing - Signal to Non-Equivalent Signal	-	4w	"delah	-	4w	ulab.co.il
	Reference			VSS	, .		12b.cc
25	Max. Trace Segment Length	15.2mm	hani file	-	10mm	- omi	Julia
283,	Max. Via Count	46	0,	2		100	
12171; IPLA3883; R5	Max. COM Express Module or Carrier Board Length	Firas abou	50.8mm		abdi	76.2mm	
1217	Max. Total Trace Segment Length		1	27.0mm	135.		
	NOTE: 1. Number of vias al	llowed: 2 vias.	46	dusi			ai@con



- 2. Minimum total length: 50.8mm.
- 3. AC cap value: 10nF.
- 4. Reference plane: continuous GND recommended.. if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- 5. Breakout length and spacing; an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm 0.16mm is allowed. The total breakout length is still 15.2mm.
- Length matching between P and N within a diff. pair: Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm.
- 7. Length matching between Tx pairs of multiple lanes: not required.
- 8. Length matching between Rx pairs of multiple lanes: not required.
- 9. Length matching between TX and Rx pairs: not required.
- 10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88μm at breakout and 200μm at main route (currently to low-speed I/O) required.</p>
- Cable loss vs channel length trade-off table: See SATA without Daughter Card with Internal Cable Routing Length versus Cable Loss figure
- 12. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
- Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes. See SATA with Daughter Card with Internal Cable Routing Length versus Cable Loss figure
- 14. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872)

Table 47. SATA without Daughter Card with Internal Cable Routing Length vs Cable Loss

Total Trace Length on Module and Carrier Boards (mm)	Internal Cable Assembly Insertion Loss Recommendation up to 3GHz
"hall"	com.
50.8	≤3.6dB
holo	
76.2	≤3.0dB
11/3-	4613
101.6	≤2.3dB
630	
127	≤2.0dB



SATA device M4 M5 M3 M5 M4 Internal Cable PCH M4 M5 TX M4 M3 M1 M5 module board Daughter card carrier board Device add-in-card ovia (optional) module

Figure 26. Direct Connect with Daughter Card, Internal Cable, and COM Express Connector

Table 48. Routing Guidelines for SATA with Daughter Card, Internal Cable, and COM Express Connector -TX

connector

							. A 'A
10/0	Parameter		:@c	Routin	ng Guidelir	nes	2277
as abde	Transmission Line Segment	ВО	M1	nda M5			
305364 Firas abdeloh	PCB Routing Layer(s)	MS/SL	MS/SL/DSL MS MS/SL/DSL				
-130 ⁵⁰	Impedance (Ω)	-			85	PUIL	
52,	Trace Width (w)	same as main route		,ha	Meets Imp	a adamaa	
-36A F	Intra Pair Line Spacing	same as line width	as abd	¹⁶ 10,	Meets iiii	Dedance	, ab.co.il c
61305			Mic	rostrip			Wbrite
PLA3883; RS1305364 F	Spacing - Signal to Equivalent Signal	2w			3w	ghani@cc	,
	Spacing - Signal to Non- Equivalent Signal	3w	200	ani fir?	3w	V	OITIP

71



100						_0.0	7
25.20		13b.co.	Stı	ripline		A380	
ghani firas.abo	Spacing - Signal to Equivalent Signal	2.7w		20	4.3	w	
iras.abd	Spacing - Signal to Non- Equivalent Signal	4w	,18b.co.	II cho	4.3	w	2LA3883:
is and it.			Dual Dual	Striplin	ne	.11	
Firas abdelghani firas abd	Spacing - Signal to Equivalent Signal	hani@c			4v	ynda0121	
200	Spacing - Signal to Non- Equivalent Signal	-		mpul	alo .co. 4v	V	-171
delo.	Reference		10.		VSS		2012
-51305364 Firas abdelon	Max. Trace Segment Length	15.2mm	eldha.	-	10mm	co.il	chois
0530	Max. Via Count	eiras.			2	Ilab.	
25137	Max. COM Express Module or Carrier Board Length		50.8mm	algha	ni@com	25.4mm	50.8mm
305364 Fir	Max. Total Trace Segment Length		i firas abo	1	127.0mm		oulab.co.ll

- 1. Number of vias allowed: 2 vias.
- 2. Minimum total length: 50.8mm.
- 3. AC cap value: 10nF.
- 4. Reference plane: continuous GND recommended. See Power Referencing tab for power referencing guidelines. if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pairto-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2mm.
- Length matching between P and N within a diff. pair: Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm.
- 7. Length matching between Tx pairs of multiple lanes: not required.
- 8. Length matching between Rx pairs of multiple lanes: not required.
- 9. Length matching between TX and Rx pairs: not required.



- Jhani firas.abdelghani@compulab.co MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.
 - 11. Cable loss vs channel length trade-off table: See SATA with Daughter Card with Internal Cable Routing Length versus Cable Loss figure
 - Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
 - 13. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
 - The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).
 - Daughter card length (M5 segment): typical length of daughter card is approximately 50.8mm.

Table 49. Routing Guidelines for SATA with Daughter Card, Internal Cable, and COM Express **Connector -RX**

	Parameter			Routir	ng Guidelin	es	11.
bdelgh	Transmission Line Segment	ВО	M1	M2	МЗ	M4	M5
Firasau	PCB Routing Layer(s)	MS/SL	MS/SL/DSL	ı	MS	MS/	SL/DSL
536h	Impedance (Ω)	35.0.			85	130.0	
51305364 Firas abdelon	Trace Width (w)	same as main route	Meets Impedance				
Fit	Intra Pair Line Spacing	same as line width	bolo	elgha	ricets imp	redance	-0.il c
536 ¹			9 Mic	rostrip			ilab.co
PLA3883; RS1305364 Fit	Spacing - Signal to Equivalent Signal	2w	iu _{i II}		3w	hani@cor	ube
PLA	Spacing - Signal to Non- Equivalent Signal	3w		. files	s.abdel ⁶ 3w		
29	(,5)		St	ripline			omi
da012171; IPLA3883; RS	Spacing - Signal to Equivalent Signal	2.7w	as abdelor.		4.3v	v	Ighani@c
d20121773	Spacing - Signal to Non- Equivalent Signal	536 ¹ 4w			4.3v	Kiras.a.	_



100							
anifiras.abu		13b.co.	Dual	Striplin	е	A380	
ghani file	Spacing - Signal to Equivalent Signal	-			4ν	v	
iras abd	Spacing - Signal to Non- Equivalent Signal	-	,12b.co	il cho	4v	V	2LA3883;
ani in	Reference		Who		VSS	47	
iras abdelghani firas.	Max. Trace Segment Length	15.2mm	-	-	10mm	nd201211	-
Eiras	Max. Via Count	9			2	0.	
, sight	Max. COM Express Module or Carrier Board Length		50.8mm	mpul	alo.cc	25.4 mm	50.8mm
Firas abde	Max. Total Trace Segment Length	300	eldhau	1	27.0mm	.0.il	cudad
05364	NOTE:	of vias allowed	d. 2 vias			aulab.0	

- Number of vias allowed: 2 vias.
- Minimum total length: 50.8mm.
- AC cap value: 10nF.
- Reference plane: continuous GND recommended. See Power Referencing tab for power referencing guidelines. if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
- Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pairto-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2mm.
- Length matching between P and N within a diff. pair: Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm.
- 7.0 Length matching between Tx pairs of multiple lanes: not required.
- 8. Length matching between Rx pairs of multiple lanes: not required.
- Length matching between TX and Rx pairs: not required.
- MODPHY RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP P and RCOMP N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.
- 11 Cable loss vs channel length trade-off table: See SATA with Daughter Card with Internal Cable Routing Length versus Cable Loss figure
- Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.



- Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
- The max. length applies to all the stackups in the 'U Ref Stackup' tab in the 11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (RDC #607872).
- Daughter card length (M5 segment): typical length of daughter card is approximately 50.8mm.

Table 50. SATA with Daughter Card with Internal Routing Length vs. Cable loss

Johani firas abd	Total Trace Length on Module and Carrier Boards and Daughter Card (mm)	Internal Cable Assembly Insertion Loss Recommendation up to 3GHz
ghall	50.8	≤3.6dB
		1301
	76.2	≤3.0dB
	101.6	≤2.3dB
	101.6	≤2.0dB
iras abdelor	bdelghani@	§ Oil cnda0
	thanifiras.ab	compulab.cc
Fir	as abdelghani firas abdelghani firas a	\$ sompulab.co.il cnda0
25130536A	thani firas.8	compulab
	46/9.	:00



11.0 Time-Aware GPIO

Time-Aware GPIO (TGPIO) is used for scheduled trigger and event timestamping. It is one of the features of Time-Synchronization Support in 11th Gen Intel[®] Core[™] processors.

11.1 Time-Aware GPIO Description

Table 51. Time-Aware GPIO Description

Signal Name	Type (Voltage Domain)	Direction	Description
TIME_SYNC_0	CMOS (1.8V)	Input	Time-Aware GPIO Input signal
TIME_SYNC_1	CMOS (1.8V)	Output	Time-Aware GPIO Output signal

11.2 Time-Aware GPIO Routing Guidelines

For Time-Aware GPIO routing guidelines, refer to the GPIO point-to-point routing guidelines in the "607872_TGL_UP3_PDG_Rev*.xlsx" (RDC #607872) in "PCH GPIO" tab.

Strapping resistor is not required since the Voltage Domain Type is CMOS.



12.0 11th Gen Intel® Core™ Processors Adhesives Guidance

12.1 Adhesives Guidance

Intel recommends the use of board level underfill (BLUF) or corner glue/fill (CG/CF) for 11th Gen Intel® Core™ processors for certain product use cases. The below chart is a guideline for temperature cycle risk based on solder ball temperature and power cycles.

If your product falls above Line A, CG, or CF may be advisable to increase the capability of the package solder joints. If your product falls above Line B, BLUF is recommended to ensure no failures over product lifetime. For more information and manufacturing guidance, please see the documents titled *Manufacturing with the Intel Platform Code Named Tiger Lake* (RDC #613010) and *Manufacturing with Intel Products Adhesive Guidance for Ball Grid Array and Package on Package* (RDC #573768).

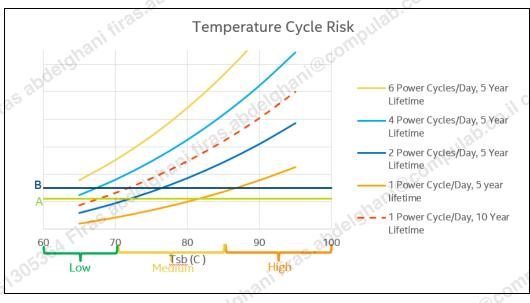


Figure 27. Temperature Cycle Risk

Note: Tsb Guidelines:

Tsb (Temperature at solder ball) is dependent on silicon junction temperature as well as the heat dissipation of the thermal solution. The below ranges are a general guideline for determining Tsb range without having a full system thermal model available.



High Tsb:

E.x.: passive metal heat sink with no air flow, closed chassis

Medium Tsb:

E.x.: heavy heat sink with some air circulation (i.e.: vented chassis)

Low Tsb:

E.x.: heavy desktop-like heat sink with forced air flow (i.e.: integrated fan)

12.2 Assumptions/Definitions

It has two assumptions: power cycle and ambient temperature.

12.2.1 Power Cycle

It has two type of power cycle: On-to-Off Cycle (assuming cooling down to ambient temperature when off) and another is On-to-Standby Cycle (assuming cooling to near-ambient temperatures when in standby)

12.2.2 Ambient Temperature

Ambient temperature is temperature external to system (room temperature) and assumed to be 24° C.

The given product temperature cycle risk assumes a minimum 28 mm board with a 15 lb load and no backing plate. Changes in board thickness, loading, or presence of a backing plate can affect temperature cycle risk.

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