11th Gen Intel® Core™ Processors for IoT Platforms

Platform Design Guide (PDG) Addendum

March 2021

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Revision History

Date	Revision	Description
March 2021	2.1	• Updated note on Chapter 4 MDIO Routing Guidelines • Updated Package Name and information in Table SGMII Ethernet-TSN Signals, MDIO Ethernet-TSN Signals and Other Signals Associated with Ethernet-TSN Subsystem Description. • Added note on Chapter 4.5.2 Other Signal Associated with Ethernet-TSN Subsystem Routing Guidelines • Updated note in Table 19, Table 21, and Table 23
November 2020	2.0	• Update chapter 4 on MDIO Routing Guidelines
October 2020	1.8	• Added note on Chapter 1.3 • Update 11th Gen Intel® Core™ Processors Pin No in Chapter 4.6
September 2020	1.7	• Added HDMI on Chapter 6 Display • Updated Chapter 7 Universal Serial Bus, Chapter 8 PCIe Gen 4 (CPU PCIe), Chapter 9 PCIe Gen 3 (PCH PCIe)- SI values updated according to latest simulations.
August 2020	1.6	• Updated Chapter 6 Display, Chapter 7 Universal Serial Bus, Chapter 8 PCIe Gen 4 (CPU PCIe), Chapter 9 PCIe Gen 3 (PCH PCIe)- SI values updated according to latest simulations.
July 2020	1.5	• Updated Chapter 4 SGMII, Chapter 6 Display, Chapter 7 Universal Serial Bus, Chapter 8 PCIe Gen 4 (CPU PCIe), Chapter 9 PCIe Gen 3 (PCH PCIe), Chapter 10 PCIe Clock & Chapter 11 SATA. - Deleted all notes related to thin stackup.
June 2020	1.3	• Added Chapter 14 11th Gen Intel® Core™ Processors - Adhesives Guidance. • Updated Note No3 in Table 11 and Table 13.
May 2020	1.2	• Added new Chapter 3 eSPI. • Added new Chapter 4 Ethernet Time-Sensitive Networking. • Updated Table 16 Other Signal Associated with Ethernet-TSN Subsystem Signal Description on SGMII_INT's Description – removed Wake-on-LAN (WOL) information. • Updated Chapter 6 DP (without retimer), eDP topologies and removed AUX retimer topology. • Updated Chapter 7 USB (with redriver) topology. • Added Chapter 8 PCIe Gen 4 (CPU PCIe). • Added Chapter 9 PCIe Gen 3 (PCH PCIe). • Added Chapter 10 PCIe Clock. • Added Chapter 11 SATA (to SATA device through internal cable). • Added Chapter 12 Type-C TBT+USB+DP with retimer. • Added Chapter 13 Time-Aware GPIO.
March 2020	1.1	• Added Chapter 4 Display and Chapter 5 USB3.2.
January 2020	1.0	• Initial release.

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1.0 Introduction

This *11th Gen Intel® Core™ Processor Platform Design Guide (PDG) Addendum* may be used as supplement documentation that covers IoT-specific features and extended temperature, such as GSPI routing guidelines, Ethernet-TSN routing guidelines, CNVi routing guidelines and Small Form Factor Display and USB 3.2 routing guidelines. This addendum complements the *11th Gen Intel® Core™ Processor Platform Design Guide (PDG)* (RDC #607872). The PDG provides motherboard implementation recommendations for the 11th Gen Intel® Core™ processor.

Note: For IoT use conditions, refer to the link provided in Table 1.2.

1.1 Terminology

Table 1. Terminology

Term	Description
CLK	Clock
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CS	Chipset
GMII	Gigabit Media Independent Interface
IEEE	Institute of Electrical and Electronic Engineers
IO	Input Output
IoT	Internet of Things
LAN	Local Area Network
MDC	Management Data Clock
MDIO	Management Data Input/Output
MISO	Primary In Secondary out (Master In Slave Out)
MOSI	Primary Out Secondary In (Master Out Slave In)
P&N	Positive and Negative
PCH-LP	Platform Controller Hub Low Power
PHY	Physical Layer Device
SPI	Serial Peripheral Interface
TSN	Time-Sensitive Networking

Note: This document reflects Intel's adoption of industry-wide changes in the use of inclusive and non-discriminatory language. As such, this document replaces the terms *master* and *slave* with *primary* and *secondary*. Nonetheless, these changes have not as yet been reflected in the software options described in this document; therefore, be aware that when this document uses the terms *primary* or *secondary*, it is referring to menu items or options that might still be labelled *master* or *slave* onscreen.

1.2 Reference Documents

Table 2. Reference Documents

Document	Document No./Location
11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (PDG)	607872
IoT Use Conditions Application	https://www.intel.com/content/www/us/en/secure/design/confidential/products-and-solutions/processors-and-chipsets/iot-use-conditions.html
11th Gen Intel® Core™ Processor UP3 External Design Specification (EDS) Addendum	608733
11th Gen Intel® Core™ Processor Platform Component List (PCL) Addendum	620609

1.3 Pin List for Ethernet-TSN & Time-Aware GPIO and Integrity Features

Table 3. Pin List Details

Pin Name	Pin
Ethernet-TSN	
PCIE7_TXN / TSN_0A_TX_DN	CD8
PCIE7_TXP / TSN_0A_TX_DP	CD9
PCIE7_RXP / TSN_0A_RX_DP	CK1
PCIE7_RXN / TSN_0A_RX_DN	CK2
PCIE8_RXN / TSN_0B_RX_DN	CK4
PCIE8_RXP / TSN_0B_RX_DP	CK5

Pin Name	Pin
Ethernet-TSN	
PCIE8_TXN / TSN_0B_TX_DN	CB7
PCIE8_TXP / TSN_0B_TX_DP	CB8
GPP_F17 / THC1_SPI2_RST_N / SGMII_MDC_0A	DV14
GPP_F18 / THC1_SPI2_INT_N / SGMII_MDIO_0A	DN10
GPP_C3 / SML0CLK / SGMII_MDC_0B	DK19
GPP_C4 / SML0DATA / SGMII_MDIO_0B	DM17
GPP_S0 / SNDW0_CLK / SGMII_AUXTS	DT32
GPP_S1 / SNDW0_DATA / SGMII_INT	DR35
GPP_S2 / SNDW1_CLK / DMIC_CLK_B0 / SGMII_RESET_N	DW35
GPP_S3 / SNDW1_DATA / DMIC_CLK_B1 / SGMII_PPS	DV35
Time-Aware GPIO	
GPPC_H19 / TIME_SYNC_0	DJ27
GPPC_B14 / SPKR / TIME_SYNC_1 / GSPI0_CS1B	DC50
INTEGRITY FEATURES	
GPPC_F22_VNN_CTRL_IEH_CORR_ERR0B	DV12
GPPC_F23_V1P05_CRTL_IEH_NONFATAL_ERR1B	DT12
GPPC_H3_SX_EXIT_HOLDOFFB_IEH_FATAL_ERR2B	DG31
GPP_T2	DT35
GPP_T3	DN33
GPP_C16 / I2C0_SDA	DW18
GPP_C17 / I2C0_SCL	DV18
GPP_C18 / I2C1_SDA	DT18
GPP_C19 / I2C1_SCL	DJ23
GPP_H4 / I2C2_SDA	DJ31
GPP_H5 / I2C2_SCL	DJ29
GPP_H6 / I2C3_SDA	DF29

Pin Name	Pin
Ethernet-TSN	
GPP_H7 / I2C3_SCL	DF29
GPP_B5 / ISH_I2C0_SDA	DB44
GPP_B6 / ISH_I2C0_SCL	DB45
GPP_B7 / ISH_I2C1_SDA	DB47
GPP_B8 / ISH_I2C1_SCL	CY39
GPP_B9 / I2C5_SDA / ISH_I2C2_SDA	DD44
GPP_B10 / I2C5_SDA / ISH_I2C2_SCL	DD47

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2.0 Generic Serial Peripheral Interface (GSPI) 3.3V

2.1 GSPI Platform- Specific Important Information

This chapter is additional supplement for Chapter 6.11 Generic Serial Peripheral Interface (GSPI) from the *11th Gen Intel® Core™ Processor Platform Design Guide* (RDC #607872) and is applicable for the extended temperature range. For extended temperature range details, please refer to the *11th Gen Intel® Core™ Processor EDS Addendum*.

The Platform Control Hub Low Power (PCH-LP) three generic SPI (GSPI) Interfaces support devices which use SPI serial protocols for transferring data. Each interface consists of four wires: a clock (CLK), two-chip select (CS) and two data lines (MOSI and MISO). GSPI is not the same as the PCH SPI interface for flash devices. This GSPI is used mainly for sensor support on the platform.

2.2 GSPI Signal Descriptions

2.2.1 Signals Group

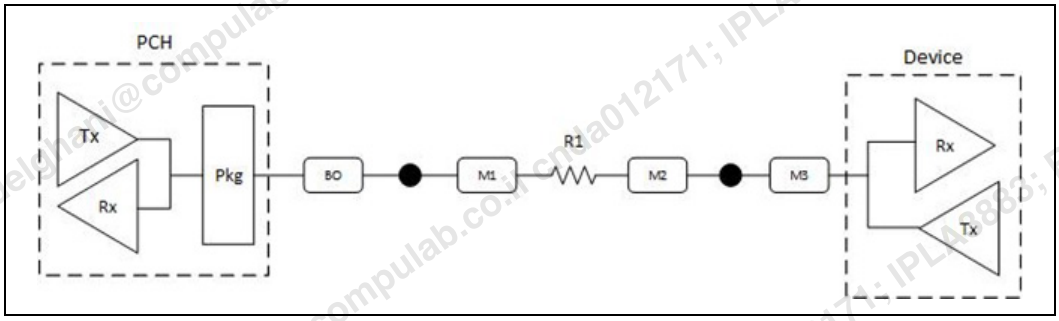
Table 4. GSPI Signals

Group	Signal Name	Description
Clock	GSPI0_CLK GSPI1_CLK GSPI2_CLK	Clock signals
Data	GSPI0_MISO GSPI1_MISO GSPI2_MISO	Primary In Secondary Out (Master In Slave Out) signals
	GSPI0_MOSI GSPI1_MOSI GSPI2_MOSI	Primary Out Secondary In (Master Out Slave In) signals
Chip Select	GSPI0_CS0# GSPI1_CS0# GSPI2_CS0#	Chip select signals

2.3 GSPI Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for the generic SPI interfaces.

Figure 1. GSPI Topology: 1-Load Topology (Add-In Card)



Series resistor R1 mentioned in the above GSPI topology have a recommended value of 15 ohm on GSPI [0:2] CLK and GSPI [0:2] MOSI only.

Table 5. GSPI Routing Guideline for 11th Gen Intel® Core™ Processor PCB

Segment	Tline Type	Reference	Nominal Via Count	Impedance	Max. Length Segment, mm (Inches)	Max. Length Total ,mm (Inches)
BO	MS/SL	VSS	1	Max. 59Ω ± 10%	12.7 (0.5)	215.9 (8.5)
M1	MS	VSS	0	43 Ω ± 10%	17.78 (0.7)	
M2	MS	VSS	1	43 Ω ± 10%	83.82 (3.3)	
M3	MS/SL	VSS	0	43 Ω ± 10%	101.6 (4)	

NOTE:
1. R1 resistor should be stuffed with 15 Ω. Design guideline applies to GSPI[0:2]_CLK and GSPI[0:2]_MOSI.
2. Up to seven vias are allowed in each route.
3. Continuous ground reference plane.
4. Max. Frequency to 20MHz for ISH and 25MHz for GSPI.

2.4 Trace Length Matching

Table 6. GSPI length matching

Notes	Description
Minimum length	M2: 7.62 mm (0.3 inches) M3: 12.7 mm (0.5 inches)
Length matching between CLK and DATA signals	12.7 mm (0.5 inches)
Trace spacing between DATA and DATA signals	BO: w M1-M3: w
Trace spacing between CLK and DATA	BO: w M1-M3: 3w
Trace Spacing between GSPI CLK/DATA with other non GSPI signals	BO: w M1-M3: 3w

NOTE:
1. 'w' is the trace width. If there are traces of different widths, the larger width should be taken.

2.5 Debug Guidelines / Recommendations

GSPI signals are multiplexed with GPIOs and default to GPIO functionality. If the GSPI interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

2.6 Tools

Intel does not promote any specific tool for this interface.

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3.0 Enhanced Serial Peripheral Interface (eSPI)

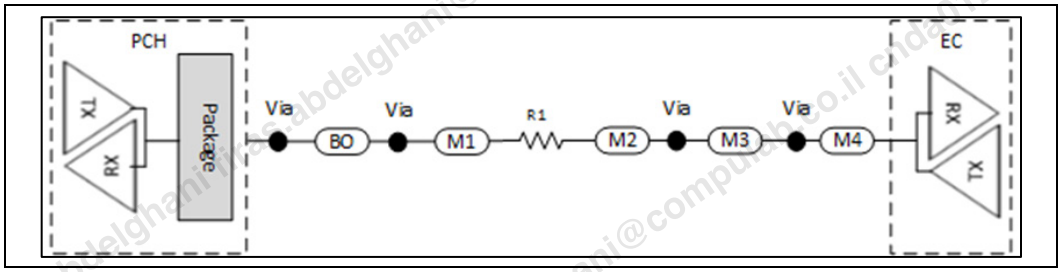
3.1 eSPI Platform – Specific Important Information

This chapter is additional supplement for Chapter 6.12 Enhanced Serial Peripheral Interface (eSPI) from 11th Gen Intel® Core™ Processor Platform Design Guide (RDC #607872) and is applicable for IoT use cases with an activity factor of 100% for approximately 10 years.

3.2 eSPI Topology Guidelines

This section contains preliminary information and details for layout and routing guidelines for the eSPI interfaces.

Figure 2. eSPI 1-Load Topology (Device Down)



Series resistor R1 mentioned in the above eSPI topology have a recommended value of 50Ω on ESPI_CLK and 15Ω on ESPI_IO_[0:3].

Table 7. eSPI 1-Load Topology (Device Down) Routing Guideline

Parameter	Routing Guidelines				
Transmission Line Segment	BO	M1	M2	M3	M4
PCB Routing Layer(s)	Any, MS, or SL				
Characteristic Impedance	50Ω ± 10%				
Trace Width (w)	4 mil min.	Meet impedance			
Trace Spacing (S1) between CLK and other signals	2.5w	3w			2.5w
Trace Spacing (S2) between data and other data signals	1w				
Max. Trace Segment Length	12.7mm (500 mils)	12.7mm (500 mils)	0.5mm (19.69 mils)	101.6mm (4000 mils)	12.7mm (500 mils)
Min./Max Total Length (T1+T2+T3)	38.1mm (1500 mils) min./140.2mm (5519.69mils) max.				
Maximum Via Count	7				
R1	50Ω on ESPI_CLK 15Ω on ESPI_IO[0:3]				
Length matching between clock and data	12.7mm (500 mils)				
Reference Plane	Continuous ground only				
Length matching between clock and data	12.7mm (500 mils)				

Figure 3. eSPI Add-in-card Topology

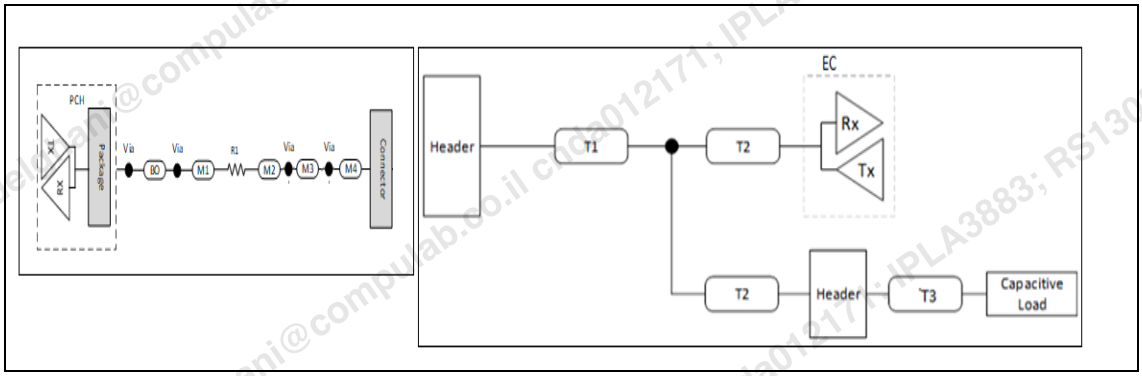


Table 8. eSPI Add-in-card Topology Routing Guideline

Parameter	Routing Guidelines	
Transmission Line Segment	T1 - MR	T2 - BI
PCB Routing Layer(s)	Any, MS, or SL	
Characteristic Impedance	50Ω ± 10%	
Trace Width (w)	Meet impedance	4 mil min.
Trace Spacing (S1) between CLK and other signals	>3w	w
Trace Spacing (S2) between Data and other Data Signals	w	w
Max. Total Length (T1+T2+T3) on Add-in Card	1.6"	
Maximum Via Count	No limit. Ground stitching via must be within 0.05" from every layer transitioning eSPI via.	
Length matching between Clock and Data	500 mils (including lengths on base board)	

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4.0 Ethernet Time-Sensitive Networking

4.1 Serial Gigabit Media Independent Interface (SGMII)

Serial Gigabit Media Independent Interface (SGMII) is the Cisco Systems* standard used by the Ethernet industry to provide a serialized interface between the Ethernet controller and an external physical layer device (PHY) component. With SGMII, the subsystem can achieve Ethernet LAN speeds of 10Mbps, 100Mbps, 1Gbps, and 2.5G bps.

The Ethernet-TSN MAC provides an SGMII interface to the External PHY. It consists of two sets of differential pairs using Current Mode Logic (CML) circuitry on one multiplexed 11th Gen Intel® Core™ Processors PCH-H ModPHY lanes. The design embeds the transmit clock in the transmit data and expects the receive clock to be embedded in the receive data. For PHY management, the Ethernet Controller also provides two CMOS Management Data Input/Output (MDIO) interface signals.

For specific design and implementation information about the GbE PHYs listed in *11th Gen Intel® Core™ Processor Platform Component List* (RDC #620609), refer to the respective vendor website(s).

4.2 SGMII Signal Description

Table 9. SGMII Ethernet-TSN Signals

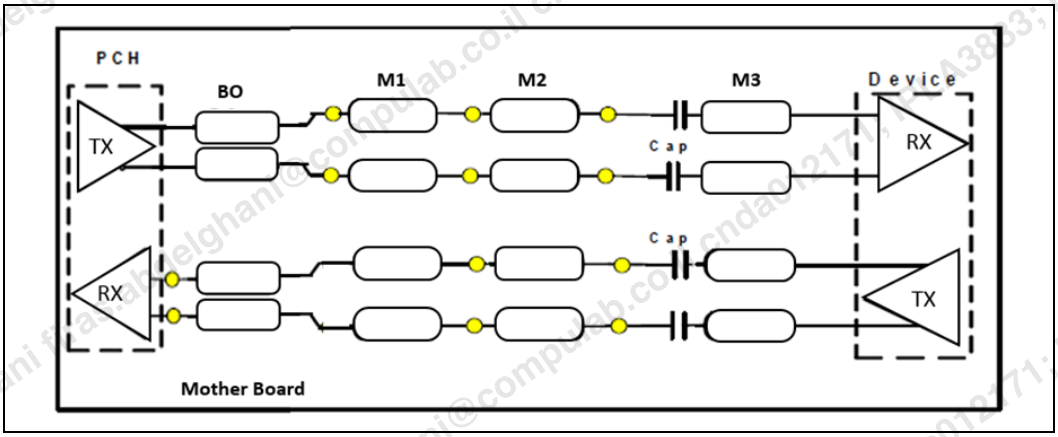
Signal Name[1,2]	Package Name	Type (Voltage Domain)	Direction	Description
TSN_0A _TX_DN	PCIE7_TXN	CML Differential Signal (1.05V)	Output	Transmit P&N of the serial differential output
TSN_0A_TX_DP	PCIE7_TXP			
TSN_0B _TX_DN	PCIE8_TXN			
TSN_0B_TX_DP	PCIE8_TXP			
TSN_0A_RX_DN	PCIE7_RXN	CML Differential Signal (1.05V)	Input	Receive P&N of the serial differential input
TSN_0A_RX_DP	PCIE7_RXP			
TSN_0B_RX_DN	PCIE8_RXN			
TSN_0B_RX_DP	PCIE8_RXP			

NOTES:
1. Refer *11th Gen Intel® Core™ Processor-UP3 EDS Addendum* (RDC #608733), Chapter 6: Flexible High-Speed Input/Output (HSIO), for a description of how these signals are routed to and selected by the FIA/MODPHY.
2. Only 0A or 0B can be used for single Ethernet-TSN port

4.3 SGMII Topology Description and Routing Guidelines

4.3.1 SGMII Topology Guidelines (Device Down)

Figure 4. SGMII Topology Diagram (Device Down)



4.3.2 SGMII Routing Guidelines (Device Down)

Table 10. SGMII Routing Guidelines (Device Down)

Segment	Tline Type	Reference	Via Count	Impedance	Max. Length, Segment (mm)	Max. Length, Total (mm)
BO	MS/SL	VSS	6	-	15.2	356
M1 or M2	SL/DSL	VSS		85 Ω	-	
M3	MS	VSS			8	

NOTES:
1. Breakout impedance can vary depending on breakout routing.
2. Keep the BO differential impedance close to 85 ohm if possible.

4.3.3 SGMII Platform Routing Design (Device Down)

Table 11. SGMII Platform Routing (Device Down)

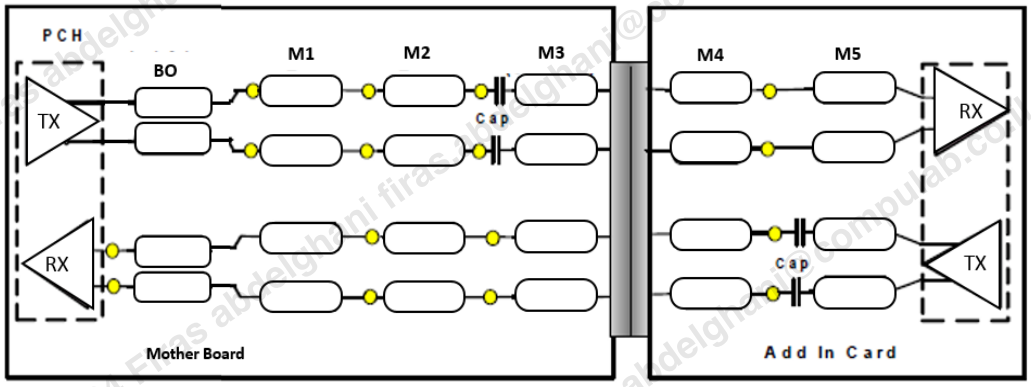
Notes	Details
AC capacitor value	75 nF to 265 nF, 100 nF nominal
Number of vias allowed	6
Reference plane	Continuous ground recommended
Breakout length and spacing	An initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed.

	The total breakout length is still 15.2mm	
Spacing - Signal to equivalent signal	microstrip	2*w (BO), 3*w (M1orM2), 3*w (M3)
	stripline	2.7*w (BO), 4.3*w (M1orM2)
	dual stripline	4*w (M1orM2)
Spacing - Signal to non-equivalent signal	microstrip	3*w (BO), 3*w (M1orM2), 3*w (M3)
	stripline	4*w (BO), 4.3*w (M1orM2)
	dual stripline	4*w (M1orM2)

NOTES:
1. 'w' is the trace width. If there are traces of different widths, the larger width should be taken.
2. Only 0A or 0B can be used for single TSN port.
3. For line width and spacing of B0 stripline and microstrip, refer to "607872_TGL_UP3_PDG_Rev*.xlsx" (RDC #607872) in "U Tline Spec" tab. Please refer to PCIe under I/O Interface column as interface reference.
4. Line width and intra-pair spacing for M1, M2 and M3 are to meet 85 ohm impedance.
5. The maximum length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).

4.3.4 SGMII Topology Guidelines (Add-In Card)

Figure 5. SGMII Topology Diagram (Add-In Card)



4.3.5 SGMII Routing Guidelines (Add-In Card)

Table 12. SGMII Routing Guidelines (Add-In Card)

Segment	Tline Type	Reference	Via Count	Impedance	Max. Length, Segment (mm)	Max. Length, Total (mm)
BO	MS/SL	VSS	4	85Ω	15.2	279.6
M1 + M2	MS/SL/DSL	VSS			-	
M3	MS	VSS			8	

NOTES:
1. Breakout impedance can vary depending on breakout routing.
2. Keep the BO differential impedance close to 85 ohm if possible.

4.3.6 SGMII Platform Routing Design (Add-In Card)

Table 13. SGMII Platform Routing (Add-In Card)

Notes	Details	
Add-in card (M4 + M5)	The total length of the add-in card (M4 + M5) is usually 38mm to 50.4mm	
	The M4 + M5 segment is a combination of MS/SL/DSL (MS where required to connect to surface mounted components)	
	The M4 + M5 segment has a typical via count of 1	
AC capacitor value	75 nF to 265 nF, 100 nF nominal	
Number of vias allowed	4 (not counting via under package)	
Breakout length and spacing	An initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm – 0.16mm is allowed.	
	The total breakout length is still 15.2mm	
Spacing between SGMII differential pairs and to other signals	microstrip	2*w (BO), 3*w (M1 or M2), 3*w (M3)
	stripline	2.7*w (BO), 4.3*w (M1 or M2)
	dual stripline	4*w (M1 or M2)
Spacing between SGMII differential pairs and to other signals	microstrip	3*w (BO), 3*w (M1orM2), 3*w (M3)
	stripline	4*w (BO), 4.3*w (M1orM2)
	dual stripline	4*w (M1 or M2)

NOTES:
1. 'w' is the trace width. If there are traces of different widths, the larger width should be taken.
2. Only 0A or 0B can be used for single Ethernet-TSN port.
3. Line width and intra-pair spacing for M1, M2 and M3 are to meet 85 ohm impedance.
4. The maximum length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).

4.3.7 SGMII General Platform Routing Design

Table 14. SGMII General Platform Routing Design

Notes	Details
Length matching between p and n within a differential pair	Within Layer Max. Mismatch: 254µm Total Length Max. Mismatch: 127µm (for channel end-to-end)
Length matching between pair to pair (inter Pair)	Not required.
Voiding recommendation for mainstream stackup	It is recommended to void pads for all components for example AC Caps as well as connector pads to optimize the impedance matching in the channel.
Discrete component part size for mainstream stackup	Recommended to use 0402 or smaller component sizes.
Reference plane	Continuous GND is recommended.
	If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt).
	If non-continuous power referencing is required on microstrip/surface layer, signal can reference power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.

4.4 Management Data Input/Output (MDIO)

There is one set of MDIO signals for Ethernet-TSN subsystem. These signals are connected to the External PHY component. These signals allow software access to the Ethernet PHY management register of this component.

4.4.1 MDIO Signal Description

Table 15. MDIO Ethernet-TSN Signals

Signal Name[1]	Package Name	Type (Voltage Domain[2])	Direction	Description
SGMII_MDC_0A	GPP_F17 / THC1_SPI2_RST#	CMOS (1.8V or 3.3V)	Output	Management Data Clock This clock signal is driven by the LAN Controllers to clock the serial MDIO Data. The clock period is programmable.
SGMII_MDC_0B	GPP_C3 / SML0CLK			
SGMII_MDIO_0A	GPP_F18 / THC1_SPI2_INT#	Open-Drain (1.8V or 3.3V)	Input/Output	Management Data Input/Output. This signal is driven by either the LAN Controllers or the External PHY component during the MDIO transaction.
SGMII_MDIO_0B	GPP_C4 / SML0DATA			

NOTES:
1. Only 0A or 0B can be used for single Ethernet-TSN port.
2. The signals should be configured to 1.8V or 3.3V using the multiplexed GPIO's Individual Voltage Select soft strap.

4.4.2 MDIO Routing Guidelines

For routing guidelines, please use guidelines for I2C in 607872_TGL_UP3_PDG_Rev*.xlsx '#SMB,SML and I2C' tab. Use the guidelines for SCL as that of MDC and the guidelines for SDA as that for MDIO. Match the lengths of MDIO and MDC to within 25.4mm.

The MDIO buffer is open drain and hence needs a pull up resistor. Please use the I2C SDA pull up resistance as a guide for the total pull up resistance value. The external pull up resistance is in parallel with any internal pull resistance set.

For example, if the frequency of the MDC is 2 GHz. the total value of the pull up resistance (external pull up resistor in parallel with any internal pull up resistor) is as shown in Table 16.

Table 16. Total Value Pull Up & Down Resistance (2 GHz.)

Total Bus Capacitance (C_b)	Total Pull Up Resistance	PCH Pull Down Resistance
Up to 50 pF	2.2 kohms	100 ohms
50 pF to 100 pF	1.2 kohms	100 ohms
50 pF to 200 pF	560 ohms	100 ohms
100 pF to 300 pF	330 ohms	50 ohms
100 pF to 400 pF	270 ohms	50 ohms

4.5 Other Signals Associated with Ethernet-TSN Subsystem

There are other signals associated with the Ethernet-TSN subsystem, which are AUXTS, INT, RESET_N, and PPS.

4.5.1 Other Signals Associated with Ethernet-TSN Subsystem Signal Description

Table 17. Other Signals Associated with Ethernet-TSN Subsystem Signal Description

Signal Name	Package Name	Type (Voltage Domain)	Direction	Description
SGMII_AUXTS	GPP_S0 / SNDW0_CLK	CMOS (1.8V)	Input	Auxiliary Time Stamp Trigger This edge-sensitive input signal triggers the storing of the time stamp into a 4x64 deep FIFO on its rising edge. If not used, this signal must be tied to GND through 20kOhm internal resistor.
SGMII_INT	GPP_S1 / SNDW0_DATA	CMOS (1.8V)	Input	Interrupt This configurable input signal is driven by the External SGMII PHY device. If not used, this signal must be tied to GND through 20kOhm internal resistor
SGMII_RESET_N	GPP_S2 / SNDW1_CLK / DMIC_CLK_B0	CMOS (1.8V)	Output	PHY Reset This output signal is used to reset the External SGMII device. If not used, should be left as a No Connect.
SGMII_PPS	GPP_S3 / SNDW1_DATA / DMIC_CLK_B1	CMOS (1.8V)	Output	Pulse-Per-Second (PPS) This output signal is generated as a pulse by Ethernet-TSN Controller each time its system timer indicates a new “seconds” value. If not used, should be left as a No Connect.

4.5.2 Other Signal Associated with Ethernet-TSN Subsystem Routing Guidelines

For Other Signal Associated with Ethernet-TSN Subsystem routing guidelines, refer to the GPIO point-to-point routing guidelines in the “*607872_TGL_UP3_PDG_Rev*.xlsx*” in (RDC #607872) in “PCH GPIO” tab.

Strapping resistor is not required since the Voltage Domain Type is CMOS.

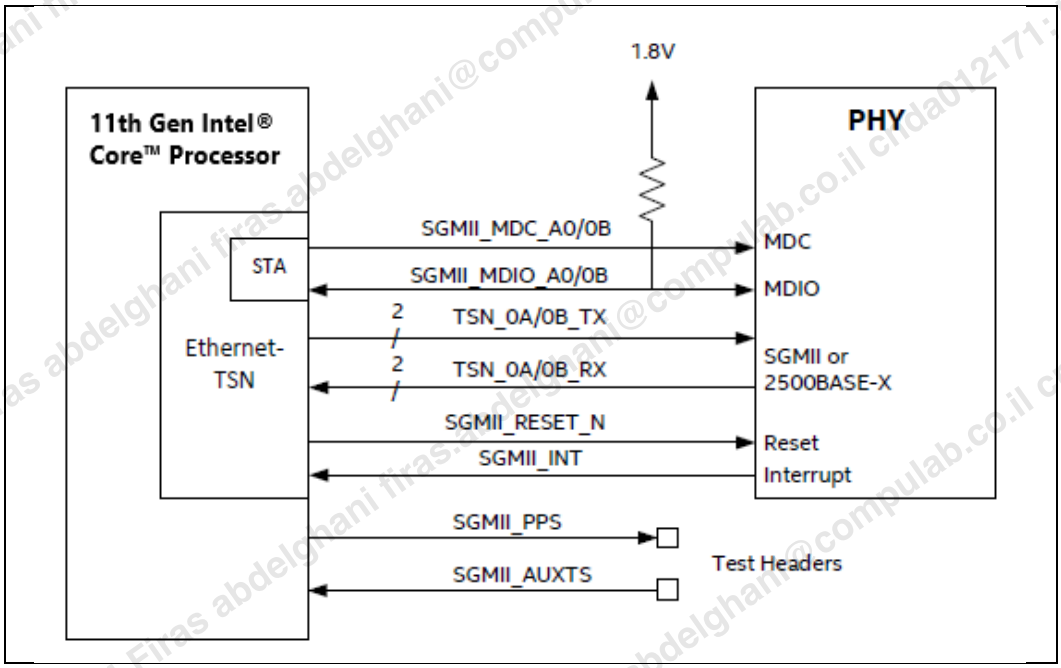
GPY PHY RESET_N signal requires an RC delay circuitry to generate at least 2ms or higher rise time for RC reset. This rise time is required to stabilize the GPY PHYs. Refer to GPY HDK HW collateral for design reference.

4.6 Ethernet-TSN and Ethernet Pin Mapping to External PHY Platform Design

This section shows one of many combinations of External PHYs interfaces arrangements.

Figure 6 shows a typical Ethernet-TSN interface to an External PHY. The figure does not show the additional board components required for AC-Coupling and signal voltage-level converters if needed.

Figure 6. 11th Gen Intel® Core™ Processor Ethernet-TSN Platform Design



11th Gen Intel® Core™ processors support concurrent Ethernet and Ethernet-TSN port. 11th Gen Intel® Core™ processors support an additional two Ethernet-TSN Ports. Only one Ethernet-TSN port can be enabled. This makes one port of Ethernet 1Gb/ Intel vPro® Technology capable Ethernet and one port of 2.5Gb/TSN capable Ethernet. A total of two Ethernet ports can be enabled simultaneously. Refer to the *11th Gen Intel® Core™ Processor-UP3 EDS Addendum* (RDC #608733), Chapter 5: Flexible High-speed Input/Output (HSIO), for a description of how these signals are routed to and selected by the FIA/MODPHY.

Refer to the *11th Gen Intel® Core™ Processor Platform Component List (PCL) Addendum* (RDC #620609) for information on different PHYs and Ethernet speed supported.

Refer to the PHY-mapping tables in this section to understand on the details the connection options.

4.6.1 Pin Mapping for GPY211/GPY215/GPY115 and I219

Table 18 shows example of Ethernet-TSN pin mapping to External PHY platform design using GPY211/215/115 and Table 19 shows example of Ethernet -TSN and Ethernet pin mapping to External PHY platform design using GPY211/215/115 and I219.

Table 18. Ethernet-TSN Pin Mapping to External PHY, GPY211/GPY215/GPY115

11th Gen Intel® Core™ Processors Pin No	11th Gen Intel® Core™ Processors Signal Name	Mapping Option 1		Mapping Option 2	
		GPY211 / 215 / 115 Pin No	GPY211 / 215 / 115 Pin Name	GPY211 / 215 / 115 Pin No	GPY211 / 215 /115 Pin Name
CD8	TSN_0A_TX_DN	Not Used		28	RX0_M
CD9	TSN_0A_TX_DP	Not Used		27	RX0_P
CK2	TSN_0A_RX_DN	Not Used		24	TX0_M
CK1	TSN_0A_RX_DP	Not Used		25	TX0_P
CB7	TSN_0B_TX_DN	28	RX0_M	Not Used	
CB8	TSN_0B_TX_DP	27	RX0_P	Not Used	
CK4	TSN_0B_RX_DN	24	TX0_M	Not Used	
CK5	TSN_0B_RX_DP	25	TX0_P	Not Used	
DV14	SGMII_MDC_0A	11	MDC	Not Used	
DN10	SGMII_MDIO_0A	10	MDIO	Not Used	
DK19	SGMII_MDC_0B	Not Used		11	MDC
DM17	SGMII_MDIO_0B	Not Used		10	MDIO
DT32	SGMII_AUXTS	4	GPIO11	4	GPIO11
DR35	SGMII_INT	12	MDINT	12	MDINT
DW35	SGMII_RESET_N	1	HRSTN	1	HRSTN
DV35	SGMII_PPS	3	GPIO12	3	GPIO12

NOTES:

1. Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for platform routing flexibility.
2. On platforms with Ethernet-TSN only, MDC/MDIO 0A or 0B can be used for platform routing flexibility.
3. For AUXTS and PPS connection, it could be connected when needed by validation.
4. For GPY211/215/115, AUXTS and PPS signal, it required Voltage Shifter 3.3V.

Table 19. Ethernet -TSN and Ethernet Pin Mapping to External PHY, GPY211/GPY215/GPY115 and I219

11th Gen Intel® Core™ Processors Pin No	11th Gen Intel® Core™ Processors Signal Name	GPY211 / 215 / 115 Pin No	GPY211 / 215 / 115 Pin Name	I219 Pin No	I219 Pin Name
CD8	PCIE7_TXN	Not Used		42	PERN
CD9	PCIE7_TXP	Not Used		41	PERP
CK2	PCIE7_RXN	Not Used		39	PETN
CK1	PCIE7_RXP	Not Used		38	PETP
CB7	TSN_0B_TX_DN	28	RX0_M	Not Used	
CB8	TSN_0B_TX_DP	27	RX0_P	Not Used	
CK4	TSN_0B_RX_DN	24	TX0_M	Not Used	
CK5	TSN_0B_RX_DP	25	TX0_P	Not Used	
DV14	SGMII_MDC_0A	11	MDC	Not Used	
DN10	SGMII_MDIO_0A	10	MDIO	Not Used	
DK19	SML0CLK	Not Used		28	SMB_CLK
DM17	SML0DATA	Not Used		31	SMB_DATA
DT32	SGMII_AUXTS	4	GPIO11	Not Used	
DR35	SGMII_INT	12	MDINT	Not Used	
DW35	SGMII_RESET_N	1	HRSTN	Not Used	
DV35	SGMII_PPS	3	GPIO12	Not Used	

NOTES:

1. Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for platform routing flexibility.
2. In order to implement both Ethernet -TSN and Ethernet on 11th Gen Intel® Core™ processors, the Ethernet-TSN port must utilize MDC/MDIO 0A.
3. For AUXTS and PPS connection, it could be connected when needed by validation.
4. For GPY211/215/115, AUXTS and PPS signal, it required Voltage Shifter 3.3V.
5. For I219 others design details such as CLK_REQN, PE_RST, PE_CLK{P,N}, LAN_DISABLE_N and LANWAKE_N, please refer *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (PDG)*, Chapter 8: Platform Connectivity (RDC #607872).
6. Not all PCH's PCIe ports can be used for LAN devices. The I219's PCIE interface pins can be connected to an appropriate 11th Gen Intel® Core™ processor PCH's PCIe Port Number 7, 8, and 9.

4.6.2 Pin Mapping for Marvell 88E2110 and I219

Table 20 shows example of Ethernet -TSN pin mapping to External PHY platform design using Marvell 88E2110 and Table 21 shows example of Ethernet -TSN and Ethernet pin mapping to External PHY platform design using Marvell 88E2110 and I219.

Table 20. Ethernet -TSN Pin Mapping to External PHY, Marvell 88E2110

11th Gen Intel® Core™ Processors Pin No	11th Gen Intel® Core™ Processors Signal Name	Mapping Option 1		Mapping Option 2	
		Marvell 88E2110 Pin No	Marvell 88E2110 Pin Name	Marvell 88E2110 Pin No	Marvell 88E2110 Pin Name
CD8	TSN_0A_TX_DN	Not Used		B3	SIN
CD9	TSN_0A_TX_DP	Not Used		A3	SIP
CK2	TSN_0A_RX_DN	Not Used		B5	SON
CK1	TSN_0A_RX_DP	Not Used		A5	SOP
CB7	TSN_0B_TX_DN	B3	SIN	Not Used	
CB8	TSN_0B_TX_DP	A3	SIP	Not Used	
CK4	TSN_0B_RX_DN	B5	SON	Not Used	
CK5	TSN_0B_RX_DP	A5	SOP	Not Used	
DV14	SGMII_MDC_0A	F1	MDC	Not Used	
DN10	SGMII_MDIO_0A	G1	MDIO	Not Used	
DK19	SGMII_MDC_0B	Not Used		F1	MDC
DM17	SGMII_MDIO_0B	Not Used		G1	MDIO
DT32	SGMII_AUXTS	L8	GPIO5	L8	GPIO5
DR35	SGMII_INT	E2	INT_N	E2	INT_N
DW35	SGMII_RESET_N	A7	RESET_N	A7	RESET_N
DV35	SGMII_PPS	K8	GPIO4	K8	GPIO4

NOTES:

1. Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for platform routing flexibility.
2. On platforms with only Ethernet-TSN, MDC/MDIO 0A or 0B can be used for platform routing flexibility.
3. For AUXTS & PPS connection, it could be connected when needed by validation.

Table 21. Ethernet – TSN and Ethernet Pin Mapping to External PHY, Marvell 88E2110, and I219

11th Gen Intel® Core™ Processors Signal Name	11th Gen Intel® Core™ Processors Signal Name	Marvell 88E2110 Pin No	Marvell 88E2110 Pin Name	I219 Pin No	I219 Pin Name
CD8	PCIE7_TXN	Not Used		42	PERN
CD9	PCIE7_TXP	Not Used		41	PERP
CK2	PCIE7_RXN	Not Used		39	PETN
CK1	PCIE7_RXP	Not Used		38	PETP
CB7	TSN_0B_TX_DN	B3	SIN	Not Used	

11th Gen Intel® Core™ Processors Signal Name	11th Gen Intel® Core™ Processors Signal Name	Marvell 88E2110 Pin No	Marvell 88E2110 Pin Name	I219 Pin No	I219 Pin Name
CB8	TSN_0B_TX_DP	A3	SIP	Not Used	
CK4	TSN_0B_RX_DN	B5	SON	Not Used	
CK5	TSN_0B_RX_DP	A5	SOP	Not Used	
DV14	SGMII_MDC_0A	F1	MDC	Not Used	
DN10	SGMII_MDIO_0A	G1	MDIO	Not Used	
DK19	SGMII_MDC_0B	Not Used		28	SMB_CLK
DM17	SGMII_MDIO_0B	Not Used		31	SMB_DATA
DT32	SGMII_AUXTS	L8	GPIO5	Not Used	
DR35	SGMII_INT	E2	INT_N	Not Used	
DW35	SGMII_RESET_N	A7	RESET_N	Not Used	
DV35	SGMII_PPS	K8	GPIO4	Not Used	

NOTES:

1. Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for platform routing flexibility.
2. In order to implement both Ethernet-TSN and Ethernet on 11th Gen Intel® Core™ processors, the Ethernet-TSN port must utilize MDC/MDIO 0A.
3. For AUXTS & PPS connection, it could be connected when needed by validation.
4. For I219 others design details such as CLK_REQN, PE_RST, PE_CLK{P,N}, LAN_DISABLE_N and LANWAKE_N, please refer *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (PDG)*, Chapter 8: Platform Connectivity (RDC #607872).
5. Not all PCH's PCIe ports can be used for LAN devices. The I219's PCIE interface pins can be connected to an appropriate 11th Gen Intel® Core™ processor PCH's PCIe Port Number 7, 8, and 9.

4.6.3 Pin Mapping for Marvell 88E1512 and I219

Table 22 shows example of Ethernet-TSN pin mapping to External PHY platform design using Marvell 88E152 and Table 23 shows example of Ethernet-TSN and Ethernet pin mapping to External PHY platform design using Marvel 88E1512 and I219.

Table 22. Ethernet-TSN to External PHY, Marvell 88E1512

11th Gen Intel® Core™ Processors Pin No	11th Gen Intel® Core™ Processors Signal Name	Mapping Option 1		Mapping Option 2	
		Marvell 88E1512 Pin No	Marvell 88E1512 Pin Name	Marvell 88E1212 Pin No	Marvell 88E1512 Pin Name
CD8	TSN_0A_TX_DN	B3	SIN	Not Used	
CD9	TSN_0A_TX_DP	A3	SIP	Not Used	
CK2	TSN_0A_RX_DN	B5	SON	Not Used	

11th Gen Intel® Core™ Processors Pin No	11th Gen Intel® Core™ Processors Signal Name	Mapping Option 1		Mapping Option 2	
		Marvell 88E1512 Pin No	Marvell 88E1512 Pin Name	Marvell 88E1212 Pin No	Marvell 88E1512 Pin Name
CK1	TSN_0A_RX_DP	A5	SOP	Not Used	
CB7	TSN_0B_TX_DN	Not Used		B3	SIN
CB8	TSN_0B_TX_DP	Not Used		A3	SIP
CK4	TSN_0B_RX_DN	Not Used		B5	SON
CK5	TSN_0B_RX_DP	Not Used		A5	SOP
DV14	SGMII_MDC_0A	F1	MDC	Not Used	
DN10	SGMII_MDIO_0A	G1	MDIO	Not Used	
DK19	SGMII_MDC_0B	Not Used		F1	MDC
DM17	SGMII_MDIO_0B	Not Used		G1	MDIO
DT32	SGMII_AUXTS	13	LED<1>	13	LED<1>
DR35	SGMII_INT	12	LED<2>/INT_N	12	LED<2>/INT_N
DW35	SGMII_RESET_N	16	RESET_N	16	RESET_N
DV35	SGMII_PPS	13	LED<1>	13	LED<1>

NOTES:

1. Ethernet-TSN data lanes (i.e., TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for platform routing flexibility.
2. On platforms with only Ethernet-TSN, MDC/MDIO 0A or 0B can be used for platform routing flexibility.
3. For AUXTS & PPS connection, it could be connected when needed by validation.
4. For AUXTS and PPS signal are from same Pin 13. It is valid connections per datasheet. Please refer to Marvell datasheet for further clarification.

Table 23. Ethernet-TSN and Ethernet to External PHY, Marvell 88E1512, and I219

11th Gen Intel® Core™ Processors Pin No.	11th Gen Intel® Core™ Processors Signal Name	Marvell 88E1512 Pin No	Marvell 88E1512 Pin Name	I219 Pin No.	I219 Pin Name
CD8	PCIE7_TXN	2	S_INN	42	PERN
CD9	PCIE7_TXP	1	S_INP	41	PERP
CK2	PCIE7_RXN	5	S_OUTN	39	PETN
CK1	PCIE7_RXP	4	S_OUTP	38	PETP
CB7	TSN_0B_TX_DN	Not Used		Not Used	
CB8	TSN_0B_TX_DP	Not Used		Not Used	
CK4	TSN_0B_RX_DN	Not Used		Not Used	
CK5	TSN_0B_RX_DP	Not Used		Not Used	
DV14	SGMII_MDC_0A	7	MDC	Not Used	

11th Gen Intel® Core™ Processors Pin No.	11th Gen Intel® Core™ Processors Signal Name	Marvell 88E1512 Pin No	Marvell 88E1512 Pin Name	I219 Pin No.	I219 Pin Name
DN10	SGMII_MDIO_0A	8	MDIO	Not Used	
DK19	SGMII_MDC_0B	Not Used		28	SMB_CLK
DM17	SGMII_MDIO_0B	Not Used		31	SMB_DATA
DT32	SGMII_AUXTS	13	LED<1>	Not Used	
DR35	SGMII_INT	12	LED<2>/INT_N	Not Used	
DW35	SGMII_RESET_N	16	RESET_N	Not Used	
DV35	SGMII_PPS	13	LED<1>	Not Used	

NOTES:

1. Ethernet-TSN data lanes (i.e. TSN_0{A,B}_{TX,RX}_D{N,P}) can use either 0A or 0B for platform routing flexibility.
2. In order to implement both Ethernet-TSN and Ethernet on 11th Gen Intel® Core™ processors, the Ethernet-TSN port must utilize MDC/MDIO 0A.
3. For AUXTS & PPS connection, it could be connected when needed by validation.
4. For AUXTS and PPS signal are from same Pin 13. It is valid connections per datasheet. Please refer to Marvell datasheet for further clarification.
5. For I219 others design details such as CLK_REQN, PE_RST, PE_CLK{P,N}, LAN_DISABLE_N and LANWAKE_N, please refer *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide (PDG)*, Chapter 8: Platform Connectivity (RDC #607872).
6. Not all PCH's PCIe ports can be used for LAN devices. The I219's PCIE interface pins can be connected to an appropriate 11th Gen Intel® Core™ processor PCH's PCIe Port Number 7, 8, and 9.

§

5.0 Wireless Connectivity Integration (CNVi) Design Considerations

5.1 Platform Considerations

Selecting Connectivity Solution

The platform motherboard can be designed to support discrete connectivity (either Intel or TPV), integrated connectivity (CNVi).

Note: All CNVi 2230 SKUs can support a "Hybrid Key-E" routing with no jumpers. When considering a TPV module, one should only use a Key-E module if the motherboard design is "Hybrid Key-E". A Key-A module will not fit into this scheme.

Table 24. CNVi Module SKUs

SKU	M.2 Type	Wi-Fi Chains	LTE Coex (on-Module BAW Filter	Comments
JfP2 2230	2230	2x2	No	Basic 2x2
JfP2 2230 vPRO	2230	2x2	No	vPro 2x2
JfP2 SD	1216	2x2	Yes	Solder-down 2x2 with LTE Coex
JfP2 SD vPRO	1216	2x2	Yes	Solder-down vPRO 2x2 with LTE Coex
HrP2 2230	2230	2x2	No	Basic 2x2
HrP2 2230 vPRO	2230	2x2	No	vPro 2x2
HrP2 SD	1216	2x2	Yes	Solder-down 2x2 with LTE Coex
HrP2 SD vPRO	1216	2x2	Yes	Solder-down vPRO 2x2 with LTE Coex

Note: This is for IoT use condition solutions that are pin and functional compatible.

Table 25. Intel Discrete Module SKUs

SKU	M.2 Type	W-Fi Chains	LTE Coex (on-Module BAW Filter	Comments
ThP2 2230	2230	2x2	No	Basic 2x2
ThP2 2230 vPRO	2230	2x2	No	vPro 2x2
ThP2 2230 EMB	2230	2x2	No	Basic 2x2 EMB
ThP2 2230 vPRO EMB	2230	2x2	No	vPro 2x2 EMB
ThP2 SD	1216	2x2	Yes	Solder-down 2x2 with LTE Coex
ThP2 SD vPRO	1216	2x2	Yes	Solder-down vPRO 2x2 with LTE Coex
CcP2 2230	2230	2x2	No	Basic 2x2
CcP2 2230 vPRO	2230	2x2	No	vPro 2x2
CcP2 SD	1216	2x2	Yes	Solder-down 2x2 with LTE Coex

§

6.0 Display

6.1 Embedded DisplayPort (eDP) Through COM Express Connector

Figure 7. eDP Topology through COM Express Connector

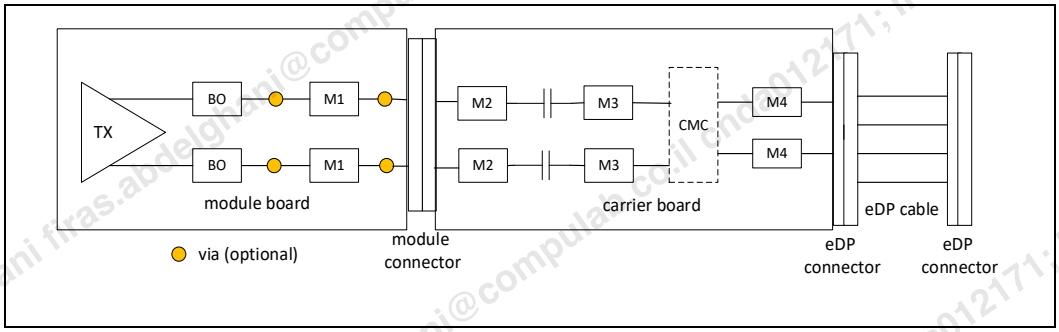


Figure 8. eDP Layout to COM Express Connector

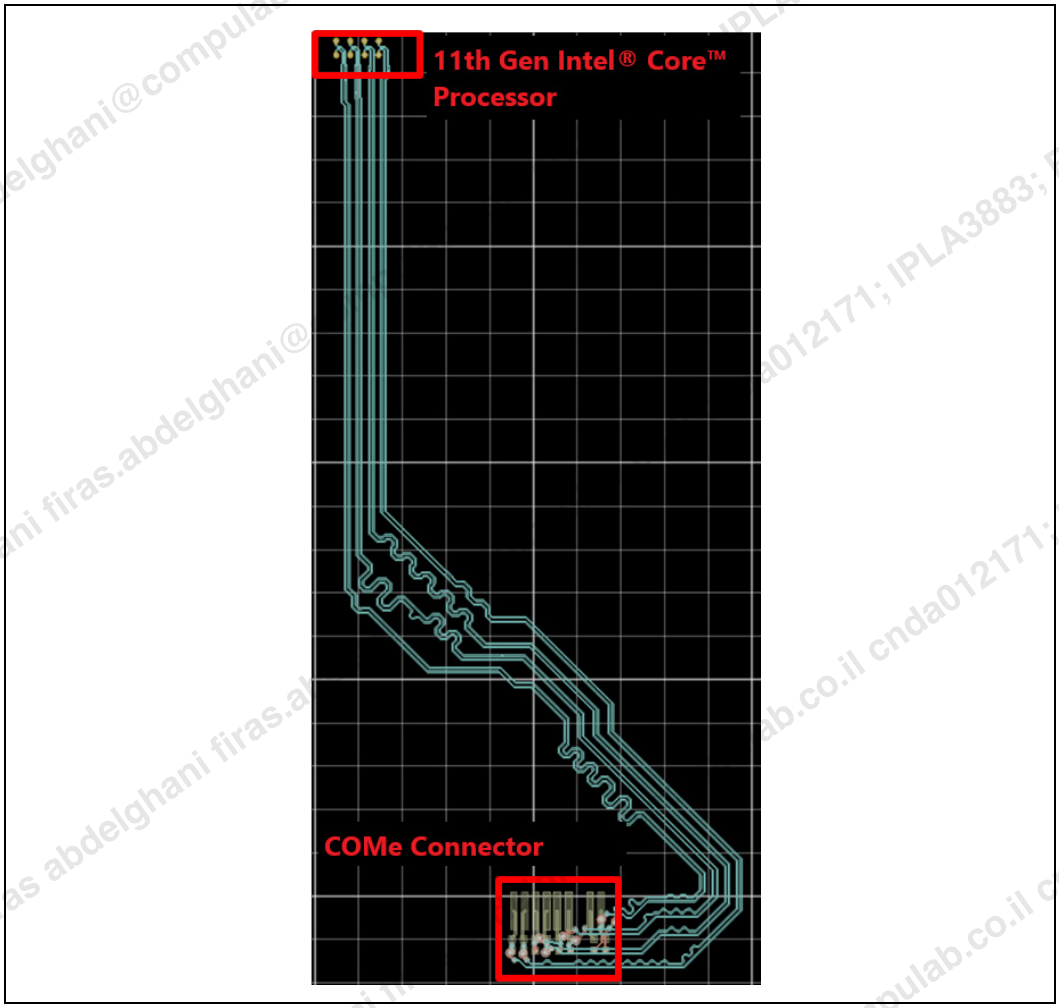


Table 26. Routing Guidelines for HBR2 (5.4 GT/s) main link or HBR3 (8.1 GT/s) with CTLE and DFE equalization or AUX

Parameter	Routing Guidelines					
Transmission Line Segment	BO	M1	M2	M3	M4	eDP cable
PCB Routing Layer(s)	MS/SL	MS/SL /DSL	MS	MS	MS	Cable
Impedance (Ω)	-	85				-
Trace Width (w)	Same as main route	Meets Impedance				-
Intra Pair Line Spacing	Same as line width					-

Microstrip					
Spacing - Signal to Equivalent Signal	1.2w	3w			-
Spacing - Signal to Non-Equivalent Signal	4w				-
Stripline					
Spacing - Signal to Equivalent Signal	1.2w	4.3w			-
Spacing - Signal to Non-Equivalent Signal	4w				-
Dual Stripline					
Spacing - Signal to Equivalent Signal	-	3.5w			-
Spacing - Signal to Non-Equivalent Signal	-				-
Reference	VSS				
Max. Trace Segment Length (mm)	13	-	-	25	381mm for HBR2 and AUX, 355mm for HBR3
Max. COM Express Module or Carrier Board Length	101.6mm		127mm		-
Max. Total Trace Segment Length	228.6mm				381mm for HBR2 and AUX, 355mm for HBR3

NOTE:

1. AUX does not need common mode choke (CMC).
2. Max. three vias, no limit for AUX
3. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
5. CMC is optional. Murata DLP11SA900HL2. Will not reduce the supported length.
6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance, for AUX 75 nF to 200 nF including tolerance).
7. Cable assembly impedance: 80-100Ω including tolerance. For AUX 75 to 100 Ω including tolerance.
8. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872)
9. Length matching between P and N within a differential pair: - Within layer max: 250µm, Total length max: 125µm.
10. Length matching between pair to pair (inter pair), within 25mm.
11. It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.

Table 27. Routing Guidelines for HBR3 (8.1 GT/s) with CTLE only

Parameter	Routing Guidelines					
Transmission Line Segment	BO	M1	M2	M3	M4	eDP cable
PCB Routing Layer(s)	MS/SL	MS/SL/ DSL	MS	MS	MS	Cable
Impedance (Ω)	-	85				-
Trace Width (w)	Same as main route	Meets Impedance				-
Intra Pair Line Spacing	Same as line width					-
Microstrip						
Spacing - Signal to Equivalent Signal	1.2w	3w				-
Spacing - Signal to Non-Equivalent Signal	4w					-
Stripline						
Spacing - Signal to Equivalent Signal	1.2w	4.3w				-
Spacing - Signal to Non-Equivalent Signal	4w					-
Dual Stripline						
Spacing - Signal to Equivalent Signal	-	3.5w				-
Spacing - Signal to Non-Equivalent Signal	-					-
Reference	VSS					
Max. Trace Segment Length (mm)	13	-	-	25		355mm
Max. COM Express Module or Carrier Board Length	50.9mm		63.7mm			-
Max. Total Trace Segment Length	114.6mm					355mm

NOTE:

1. AUX does not need common mode choke (CMC).
2. Number of vias allowed: Max. three vias, no limit for AUX
3. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
5. CMC is optional. Murata DLP11SA900HL2. Will not reduce the supported length.
6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance, for AUX 75 nF to 200 nF including tolerance).

7. Cable assembly impedance: 80-100Ω including tolerance. For AUX 75 to 100 Ω including tolerance.
8. Length matching between P and N within a differential pair: - Within layer max: 250µm, Total length max: 125µm.
9. Length matching between pair to pair (inter pair), within 25mm.
10. It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitor pads is not necessary.
11. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872)

Table 28. Estimated Insertion Loss (dB) for HBR2 and HBR3

Cable Length	Estimated Insertion Loss (dB)	
	HBR2	HBR3
25mm	-0.41	-0.62
355mm	-	-5.10
381mm	-5.10	-

6.2 DisplayPort Type-C Port (DP TCP) Through COM Express Connector

Figure 9. Topology through Com Express Connector with Retimer

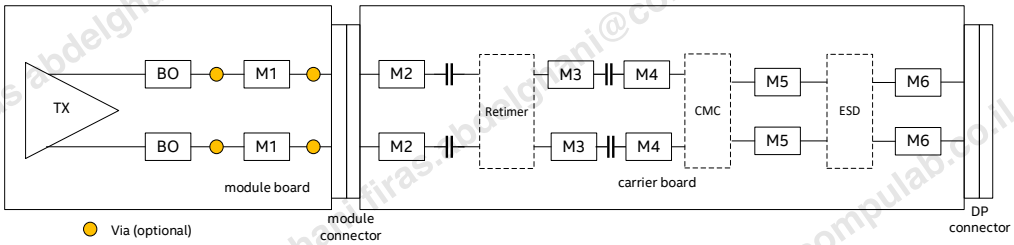


Table 29. Routing Guidelines for Topology through COM Express Connector with Retimer

Parameter	Routing Guidelines				
Transmission Line Segment	BO	M1	M2	M3	M4+M5+M6
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS	MS/SL/DSL	MS
Impedance (Ω)	-	85			
Trace Width (w)	Same as main route	Meets Impedance			
Intra Pair Line Spacing	Same as line width				

Microstrip					
Spacing - Signal to Equivalent Signal	1.2w	3w			
Spacing - Signal to Non-Equivalent Signal	4w				
Stripline					
Spacing - Signal to Equivalent Signal	1.2w	4.3w			
Spacing - Signal to Non-Equivalent Signal	4w				
Dual Stripline					
Spacing - Signal to Equivalent Signal	-	3.5w			
Spacing - Signal to Non-Equivalent Signal	-				
Reference	VSS				
Max. Trace Segment Length (mm)	13	-	-	-	-
Max. Via Count	1	1	0	1	0
Max. Total Length	406.6mm			89mm	

NOTE:

1. Number of vias allowed: Max. three vias.
2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. CMC is optional. PCB CMC or Murata NFP0QHB372HS2. Will not reduce the supported length.
5. ESD: Infineon ESD102-U4-05L (I/O-to-GND Capacitance ≤0.65pF).
6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
7. Retimer assumed DP specification reference with CTLE+DFE EQ.
8. Length of retimer to DP connector superseded by retimer vendor recommendations.
9. Length matching between P and N within a differential pair: - Within layer max: 250um, Total length max: 125um.
10. Length matching between pair to pair (inter pair), within 25mm.
11. It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
12. Unused data signals should be left unconnected at the BGA ball.
13. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872)
14. Max. date rate: 8.1 GT/s (HBR3). For topology without retimer with data rate of 5.4 GT/s (HBR2), see the section on DP DDI.

6.3 DisplayPort Digital Display Interface (DP DDI) Through COM Express Connector

Figure 10. Main Link Topology through COM Express Connector

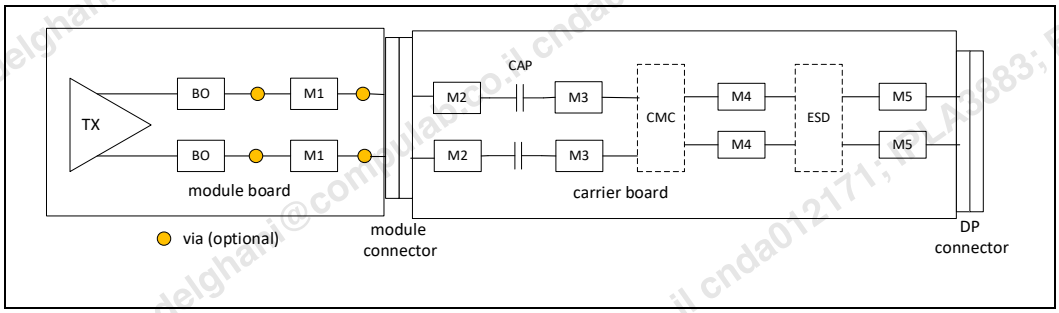


Figure 11. Main Link Layout to COM Express Connector (for both TCP and DDI, no AUX is shown)

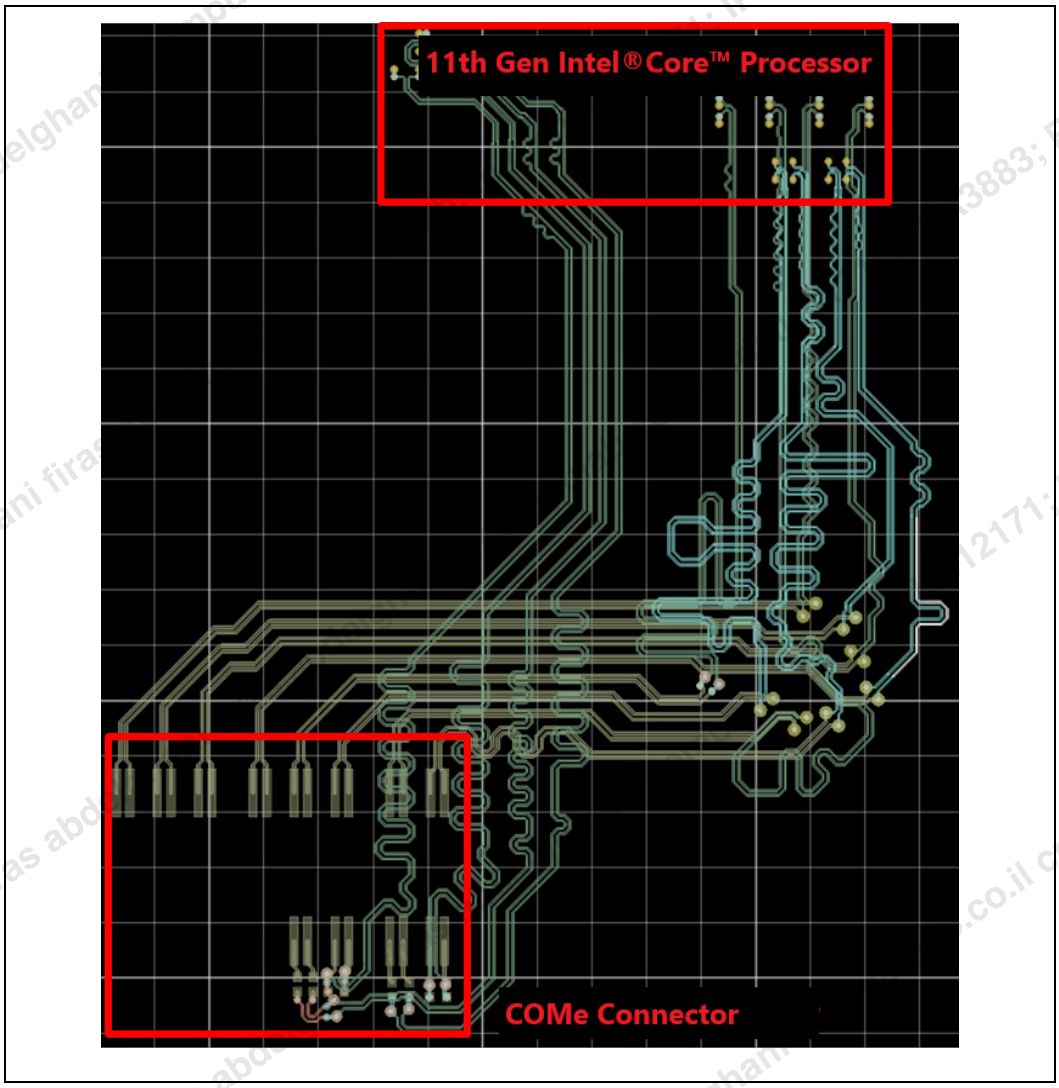


Table 30. Routing Guidelines for DP DDI

Parameter	Routing Guidelines				
Transmission Line Segment	BO	M1	M2	M3	M4+M5
PCB Routing Layer(s)	MS/SL	MS/SL/DSL		MS	
Impedance (Ω)	-	85			
Trace Width (w)	Same as main route	Meets Impedance			
Intra Pair Line Spacing	Same as line width				

Parameter	Routing Guidelines			
Microstrip				
Spacing - Signal to Equivalent Signal	1.2w	3w		
Spacing - Signal to Non-Equivalent Signal	4w			
Stripline				
Spacing - Signal to Equivalent Signal	1.2w	4.3w		
Spacing - Signal to Non-Equivalent Signal	4w			
Dual Stripline				
Spacing - Signal to Equivalent Signal	-	3.5w		
Spacing - Signal to Non-Equivalent Signal	-			
Reference	VSS			
Max. Trace Segment Length (mm)	13	-	-	36.7
Max. COM Express Module or Carrier Board Length	93.1mm		46.8mm	
Max. Total Trace Segment Length	139.9mm			

NOTE:

1. Number of vias allowed: Max. three vias.
2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. CMC is optional. PCB CMC or Murata NFP0QHB372HS2. Will not reduce the supported length.
5. ESD: Infineon ESD102-U4-05L (I/O-to-GND Capacitance ≤0.65pF).
6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
7. Length matching between P and N within a differential pair: - Within layer max: 250µm, Total length max: 125µm.
8. Length matching between pair to pair (inter pair), within 25mm.
9. It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
10. DP_COMP_OBSN: - 150Ω +/-1% pulldn to VSS. Provide good noise isolation. Platform RDC <0.2Ω.
11. DP_COMP_OBSN no connect: - DP_COMP_OBSN can be unconnected if none of the DDI ports (DP, HDMI, eDP) are used.
12. DISP_UTILS: - Recommend 50Ω nominal trace impedance with reasonable noise isolation. Requires level shifting on the platform.
13. Max. data rate: 5.4 GT/s (HBR2)
14. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).

6.4 Display Port Auxiliary (DP AUX) Through COM Express Connector

Figure 12. Main Link Topology through COM Express Connector

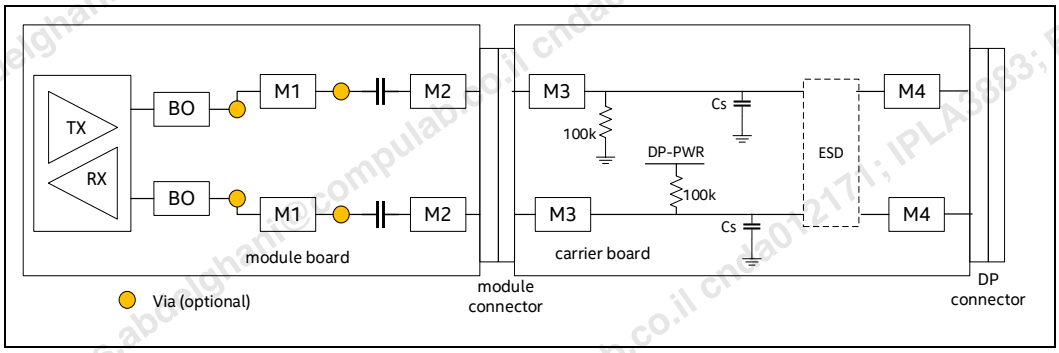


Table 31. Routing Guidelines for Main Link

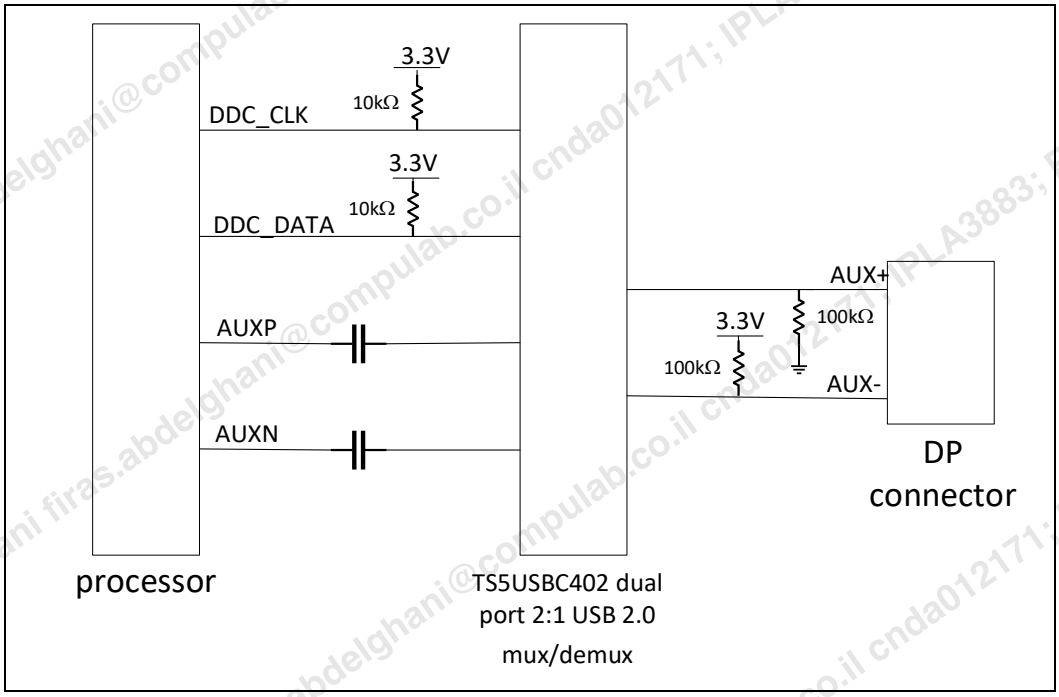
Parameter	Routing Guidelines			
Transmission Line Segment	BO	M1+M2	M3	M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS/SL/DSL	MS/SL/DSL
Impedance (Ω)	-	85		
Trace Width (w)	Same as main route	Meets Impedance		
Intra Pair Line Spacing	Same as line width			
Microstrip				
Spacing - Signal to Equivalent Signal	1.2w	3w		
Spacing - Signal to Non-Equivalent Signal	4w			
Stripline				
Spacing - Signal to Equivalent Signal	1.2w	4.3w		
Spacing - Signal to Non-Equivalent Signal	4w			

Dual Stripline				
Spacing - Signal to Equivalent Signal	-	3.5w		
Spacing - Signal to Non-Equivalent Signal	-			
Reference	VSS			
Max. Trace Segment Length (mm)	25	-	-	25
Max. COM Express Module or Carrier Board Length	240.3mm		171.6mm	
Max. Total Trace Segment Length	411.9mm			

NOTE:

1. Number of vias allowed: No explicit limit for number of vias, use best known routing practices.
2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. ESD: Infineon ESD102-U4-05L, ESD102-U1-02ELS, or equivalent.
5. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
6. Cs cap value: nominal 100pF. This is for optional edge rate control to comply with VESA "AUX Channel PHY SCR v6".
7. Length matching between P and N within a differential pair: - Within layer max: 250µm, Total length max: 125µm.
8. Length matching between pair to pair (inter pair), within 25mm.
9. Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for ESD's and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
10. Unused data signals should be left unconnected at the BGA ball.
11. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).
12. Optional Edge Rate Control: To comply with VESA "AUX Channel PHY SCR v6", an edge rate reduction mechanism such as a 100pF capacitor to VSS may be placed on each AUX signal before the ESD.

Figure 13. AUX Dual Mode Circuit



Note: This can be implemented with a multiplexer as in example shown. This example does not include the edge rate control.

6.5 HDMI Port Type-C Port (HDMI TCP) Through COM Express Connector

Figure 14. Retiming Level Shifter HDMI TCP with COM Express Connector

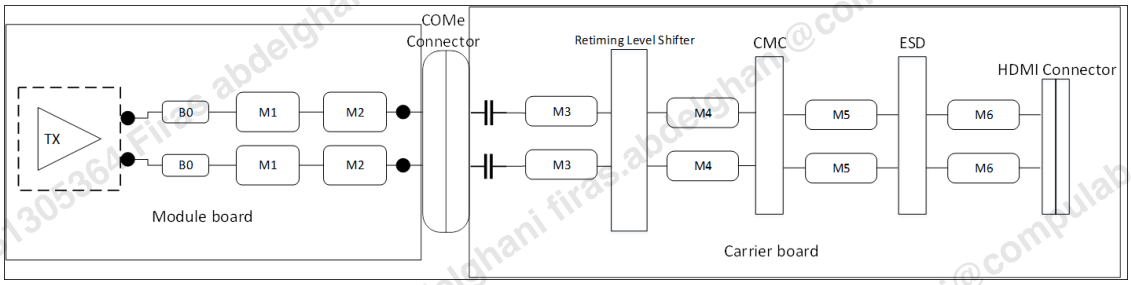


Table 32. Routing Guidelines for HDMI TCP Topology through COM Express Connector

Parameter	Routing Guidelines			
Transmission Line Segment	BO	M1+M2	M3	M4+M5+M6
PCB Routing Layer(s)	MS/SL/DSL			
Reference	VSS			
Max. Length Segment (mm)	13	89	227.6	25
Max. Via Count	1			
Max. Total Length	102 mm		252.6 mm	

NOTE:

1. Number of vias allowed: Max. three vias.
2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. CMC is optional. Optional Murata DLP11SA900HL2 or equivalent. Populating will not reduce the supported length
5. ESD: Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ≤ 0.65pF). Optional if retimer has integrated ESD that meets discharge requirements.
6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
7. Retiming LS：TI SN75DP159 or Parade PS8409A
8. Retiming LS Trace Impedance：Trace impedance between retiming LS and HDMI connector should follow retiming LS datasheet to meet HDMI 2.0 industry specification。
9. Max. Supported Frequency：5.94Gbps。
10. Retimer Sideband Communication：Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).
11. Length matching between P and N within a differential pair: - Within layer max: 250um, Total length max: 125um.
12. Length matching between pair to pair (inter pair), Within 13mm (HDMI 2.0); 25mm (HDMI 1.4).
13. Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs, ESDs, and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
14. Unused signals: Unused data and AUX signals should be left unconnected at the BGA ball.

Figure 15. Cost Reduced Level Shifter with COM Express Connector (2.97Gbps)

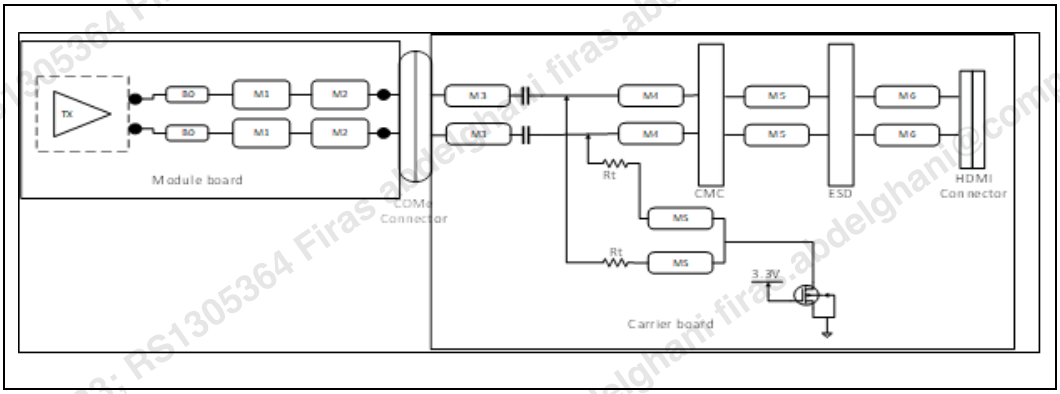


Table 33. Routing Guidelines for HDMI TCP Cost Reduced Level Shifter Topology through COM Express Connector

Parameter	Routing Guidelines				
Transmission Line Segment	BO	M1+M2	M3	M4+M5+M6	MS
SPCB Routing Layer(s)	MS/SL/DSL		MS		
Reference	VSS				
Max. Length Segment (mm)	13	30.3	31	13	
Max. Via Count	1		0		
Max. Total Length	87.3 mm				13 mm

NOTE:

1. Number of vias allowed: Max. two vias.
2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. CMC is optional. Optional Murata DLP11SA900HL2 or equivalent. Populating will not reduce the supported length
5. ESD: Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ⩽0.65pF). Optional if retimer has integrated ESD that meets discharge requirements.
6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
7. Rt: 470Ω +/-5%. Minimize any stub in the differential pair routing due to this resistor placement. Ideally the resistor pads are placed in the differential pair traces between M3 and M4, resulting no stub at all.
8. Max. nFET Ron: 10Ω.
9. Max. Data Rate: 2.97 Gbps.
10. Length matching between P and N within a differential pair: - Within layer max: 250um, Total length max: 125um.
11. Length matching between pair to pair (inter pair), Within 13mm (HDMI 2.0); 25mm (HDMI 1.4).
12. Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs, ESDs, and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.
13. Unused signals: Unused data and AUX signals should be left unconnected at the BGA ball.

6.6 HDMI Port Digital Display Interface (HDMI DDI) Through COM Express Connector

Figure 16. Retiming Level Shifter HDMI DDI with COM Express Connector

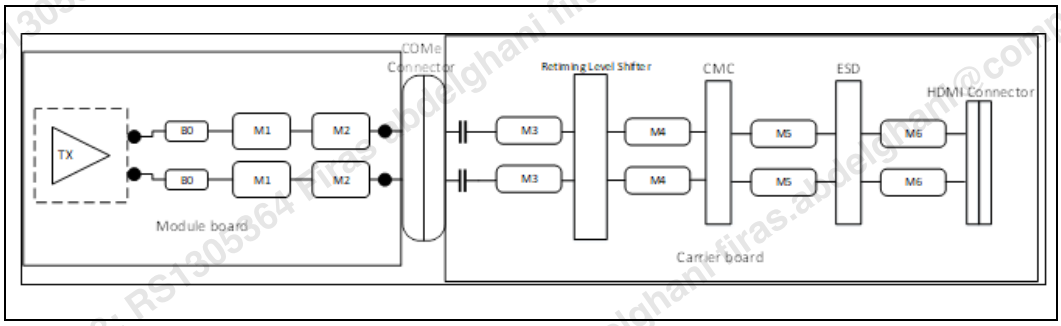


Table 34. Routing Guidelines for HDMI DDI Topology through COM Express Connector

Parameter	Routing Guidelines			
Transmission Line Segment	BO	M1+M2	M3	M4+M5+M6
PCB Routing Layer(s)	MS/SL/DSL			
Reference	VSS			
Max. Length Segment (mm)	13	89	227.6	25
Max. Via Count	1			
Max. Total Length	102 mm		252.6 mm	

NOTE:

1. Number of vias allowed: Max. three vias.
2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. CMC is optional. Optional Murata DLP11SA900HL2 or equivalent. Populating will not reduce the supported length
5. ESD: Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ≤ 0.65pF). Optional if retimer has integrated ESD that meets discharge requirements.
6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
7. Retiming LS：TI SN75DP159 or Parade PS8409A
8. Retiming LS Trace Impedance：Trace impedance between retiming LS and HDMI connector should follow retiming LS datasheet to meet HDMI 2.0 industry specification。
9. Max. Supported Frequency：5.94Gbps。
10. Retimer Sideband Communication：Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).
11. Length matching between P and N within a differential pair: - Within layer max: 250um, Total length max: 125um.
12. Length matching between pair to pair (inter pair), Within 13mm (HDMI 2.0); 25mm (HDMI 1.4).
13. Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs, ESDs, and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.

Figure 17. Active Level Shifter with COM Express Connector

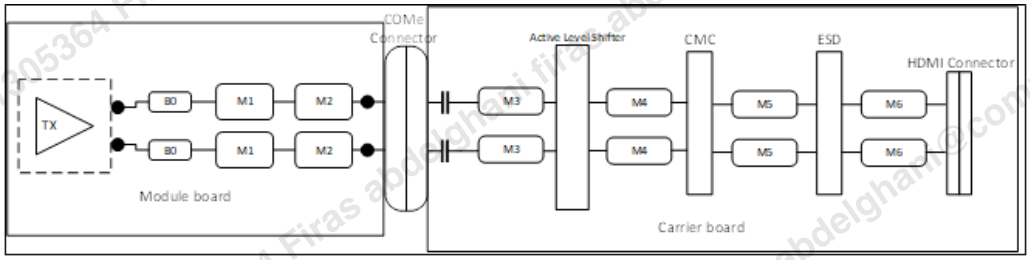


Table 35. Routing Guidelines for HDMI DDI Topology with Active Level Shifter through COM Express Connector

Parameter	Routing Guidelines			
Transmission Line Segment	BO	M1+M2	M3	M4+M5+M6
SPCB Routing Layer(s)	MS/SL/DSL			
Reference	VSS			
Max. Length Segment (mm)	13	89	114.6	76
Max. Via Count	1			
Max. Total Length	102 mm		190.6 mm	

NOTE:

1. Number of vias allowed: Max. three vias.
2. Reference plane for micro-strip route: - Continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
3. Reference plane for stripline and dual stripline route: - Both sides can either be continuous ground or continuous power that has low frequency peak to peak noise, ground preferred.
4. CMC is optional. Optional Murata DLP11SA900HL2 or equivalent. Populating will not reduce the supported length
5. ESD: Infineon ESD102-U1-02ELS or Nexperia\NXP PUSB3FR4 (I/O-to-GND Capacitance ≤0.65pF). Optional if retimer has integrated ESD that meets discharge requirements.
6. AC cap value: nominal 100nF recommended (75nF to 265nF including tolerance).
7. ALS: Parade PS8203 or equivalent
8. Max. Data Rate: 2.97 Gbps.
9. Retimer Sideband Communication： Any port configured to support HDMI must implement sideband communications via the DDC (I2C) channel associated with that HDMI port as defined in the Video BIOS Table (VBT).
10. Length matching between P and N within a differential pair: - Within layer max: 250um, Total length max: 125um.
11. Length matching between pair to pair (inter pair), Within 13mm (HDMI 2.0); 25mm (HDMI 1.4).
12. Voiding recommendation: It is recommended to void unused (non-functional) pads for differential vias, and pin pads for CMCs, ESDs, and connectors to optimize the impedance matching in the channel. Voiding of 0402 or smaller AC capacitors pads is not necessary.

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7.0 Universal Serial Bus 3.2 (USB 3.2)

Note: The design guides for USB in this addendum assumes the transceiver is on the PCH and not on the Type-C ports.

7.1 USB 3.2 Gen 2 Through COM Express Connector

Figure 18. PCH through COM Express connector with Redriver

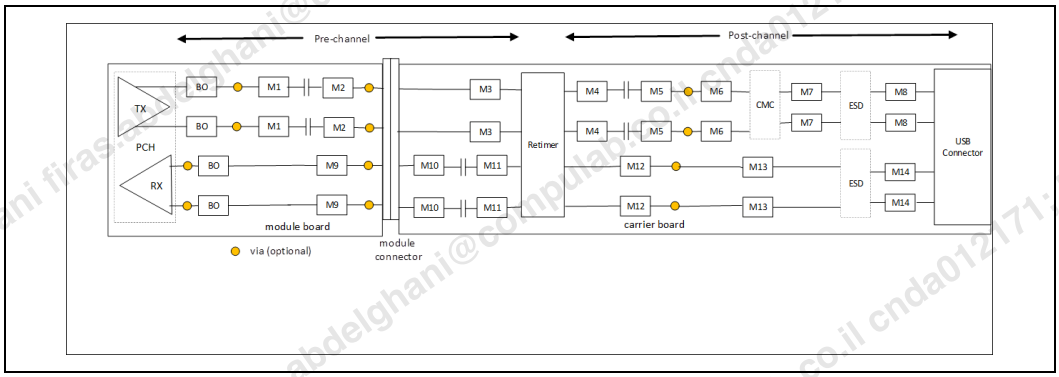

Figure 19. USB 3.2 Gen 2 Layout to COM Express Connector

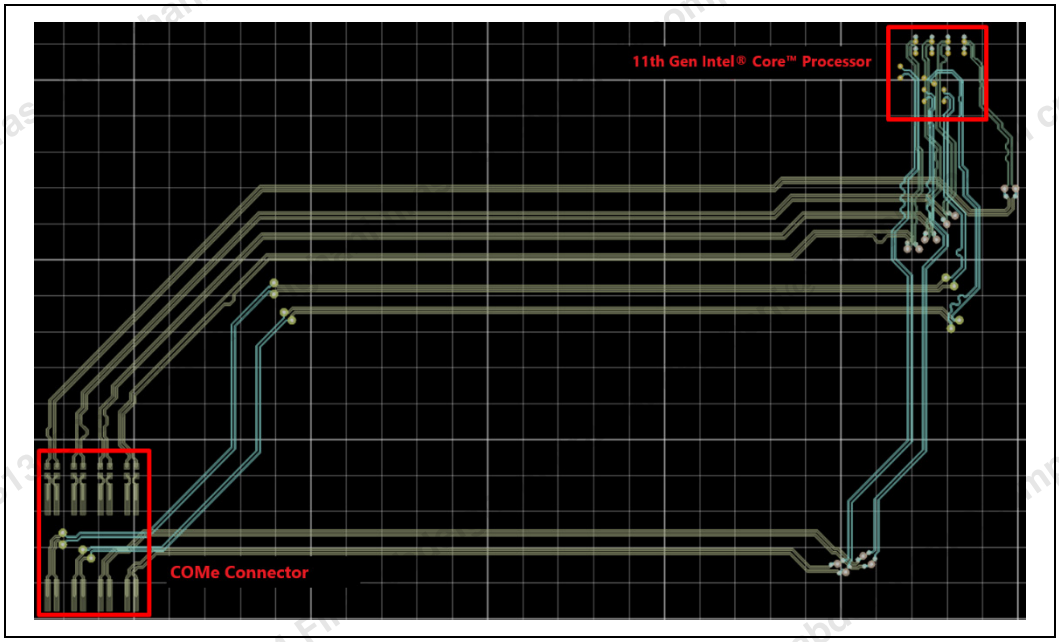

Table 36. Routing Guidelines for Redriver Topology through COM Express Connector

Parameter	Routing Guidelines					
Transmission Line Segment	BO	(M1+M2) or M9	M3 or (M10 + M11)	(M4 + M5) or M12	(M6 + M7) or M13	M8 or M14
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS			
Impedance (Ω)	-	80				
Trace Width (w)	Same as main route	Meets Impedance				
Intra Pair Line Spacing	Same as line width					
Microstrip						
Spacing - Signal to Equivalent Signal	2w	4w				
Spacing - Signal to Non-Equivalent Signal	3w	4.5w				
Stripline						
Spacing - Signal to Equivalent Signal	2.67w	6w				
Spacing - Signal to Non-Equivalent Signal	4w	6.67w				
Dual Stripline						
Spacing - Signal to Equivalent Signal	-	4.5w				
Spacing - Signal to Non-Equivalent Signal	-	5w				
Reference	VSS					
Max. Trace Segment Length	10.2 mm	Max. length information depends on Redriver				
Via Count	1	1	0	1	0	0

NOTE:

1. It is strongly recommended to use ESD protection devices on each USB data signal.
2. Length matching between P and N within a differential pair: - Within layer max: 0.254mm, Total length max: 0.127mm.
3. Channel and Via stub requirement must meet <381µm for both Tx and Rx signal pairs.

4. Reference plane: continuous ground is recommended. If continuous ground cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
5. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components, for example, AC caps as well as connector pads to optimize the impedance matching in the channel.
6. Discrete component part size for mainstream stackup: It is recommended to use 0402 or smaller component sizes.
7. AC coupling capacitor value nominal 100nF (75nF to 265nF according to USB specification).
8. It is recommended to place the AC coupling capacitors near the transmitter sides of the re-driver as shown in the topology diagram.
9. Important guidelines on repeater/active multiplexer topologies: Max. pre-channel length depends on what the specific repeater selected can compensate for at 10 GT/s speed when used in conjunction with Intel PCH. Please work with the repeater vendor for specific routing recommendations. The afore mentioned DG is superseded by vendor recommendations. In addition, it is recommended to refer to - repeater integration white paper *USB 3.1 Repeater Integration Technical White Paper* (RDC #571574). The white paper illustrates in detail the fundamental differences between different repeater types (redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
10. Max. no. of vias is three on each trace from PCH to USB connector.

7.2 USB 3.2 Gen 1 Through COM Express Connector

Figure 20. External with COM Express Connector

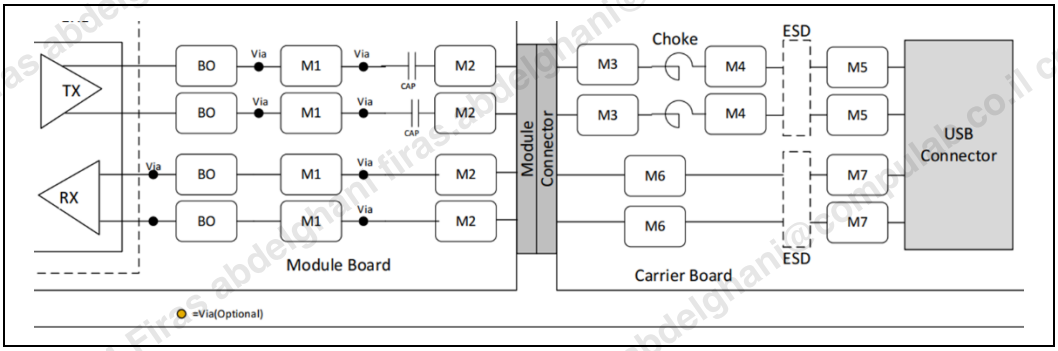

Table 37. Routing Guidelines for USB 3.2 Gen 1 Topology Through COM Express Connector

Parameter	Routing Guidelines				
Transmission Line Segment	BO	M1	M2	(M3+M4) or M6	M5 or M7
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS		
Impedance (Ω)	-	85			
Trace Width (w)	Same as main route	Meets Impedance			

Parameter	Routing Guidelines				
Intra Pair Line Spacing	Same as line width				
Microstrip					
Spacing - Signal to Equivalent Signal	1.2w	3w			
Spacing - Signal to Non-Equivalent Signal	4w				
Stripline					
Spacing - Signal to Equivalent Signal	1.2w	4.3w			
Spacing - Signal to Non-Equivalent Signal	4w				
Dual Stripline					
Spacing - Signal to Equivalent Signal	-	3.5w			
Spacing - Signal to Non-Equivalent Signal	-				
Reference	VSS				
Max. Trace Segment Length	15.2mm	-	10.2mm	-	15.2mm
Max. Via Count	1	1	0	0	0
Max. COM Express Module or Carrier Board Length	78.2mm			125mm	
Max. Total Trace Segment Length	203.2mm				

NOTE:

1. It is strongly recommended to use ESD protection devices on each USB data signal.
2. Length matching between P and N within a differential pair: - Within layer max: 0.254mm, Total length max: 0.127mm.
3. Channel and Via stub requirement must meet <381µm for both Tx and Rx signal pairs.
4. Reference plane continuous ground is recommended. If continuous ground cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
5. Voiding recommendation for mainstream stackup. It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
6. Discrete component part size for mainstream stackup, recommended to use 0402 or smaller component sizes.
7. AC coupling capacitor value: nominal 100nF (75nF to 265nF according to USB specification).
8. Max. no. of vias is two on each trace from PCH to USB connector.

Figure 21. Redriver Topology through COM Express Connector

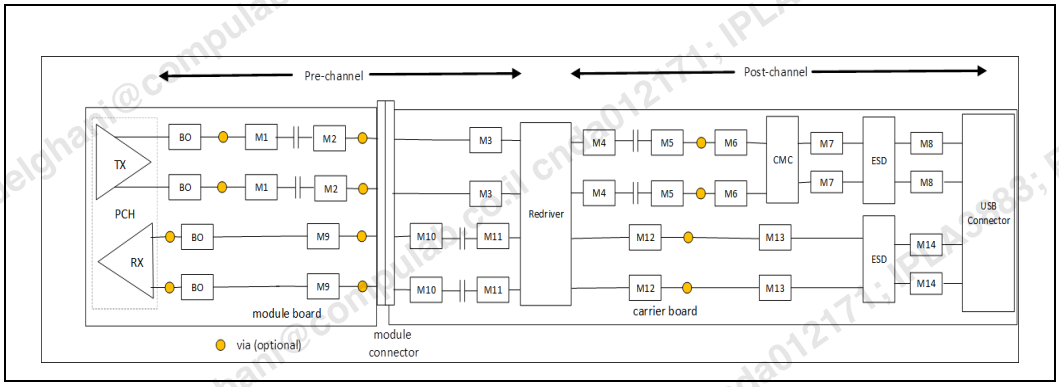

Table 38. Routing Guidelines for Redriver Topology through COM Express Connector

Parameter	Routing Guidelines					
Transmission Line Segment	BO	(M1 + M2) or M9	M3 or (M10 + M11)	(M4 + M5) or M12	(M6 + M7) or M13	M8 or M14
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS			
Impedance (Ω)	-	85				
Trace Width (w)	Same as main route	Meets Impedance				
Intra Pair Line Spacing						
Microstrip						
Spacing - Signal to Equivalent Signal	1.2w	3w				
Spacing - Signal to Non-Equivalent Signal	4w					
Stripline						
Spacing - Signal to Equivalent Signal	1.2w	4.3w				
Spacing - Signal to Non-Equivalent Signal	4w					

Dual Stripline						
Spacing - Signal to Equivalent Signal	-	3.5w				
Spacing - Signal to Non-Equivalent Signal	-					
Reference	VSS					
Max. Trace Segment Length	15.2 mm	Max. length information depends on Redriver				
Max. Via Count	1	1	0	1	0	0
Max. Total Trace Segment Length	Max. length information depends on Redriver					

NOTE:

1. It is strongly recommended to use ESD protection devices on each USB data signal.
2. Length matching between P and N within a differential pair: - Within layer max: 0.254mm, Total length max: 0.127mm.
3. Channel and via stub requirement must meet <381µm for both Tx and Rx signal pairs.
4. Reference plane continuous ground is recommended. If continuous ground cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
5. Voiding recommendation for mainstream stackup: it is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
6. Discrete component part size for mainstream stackup : t is recommended to use 0402 or smaller component sizes.
7. AC coupling capacitor value: nominal 100nF (75nF to 265nF according to USB specification).
8. It is recommended to place the AC coupling capacitors near the transmitter sides of the re-driver as shown in the topology diagram.
9. Important guidelines on repeater/active multiplexer topologies: Max. pre-channel length depends on what the specific repeater selected can compensate for at 5 GT/s speed when used in conjunction with Intel PCH. Please work with the repeater vendor for specific routing recommendations. The aforementioned DG is superseded by vendor recommendations. In addition, it is recommended to refer to - repeater integration white paper *USB 3.1 Repeater Integration Technical White Paper* (RDC #571574). The white paper illustrates in detail the fundamental differences between different repeater types (Redriver vs retimer), and the efforts needed to enable such repeater in customer system designs.
10. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).
11. Max. no. of vias is three on each trace from PCH to USB connector.

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8.0 PCIe Gen 3 (PCH PCIe)

8.1 Gen 3 Device Down with COM Express Connector

Figure 22. Gen 3 Device Down with COM Express Connector

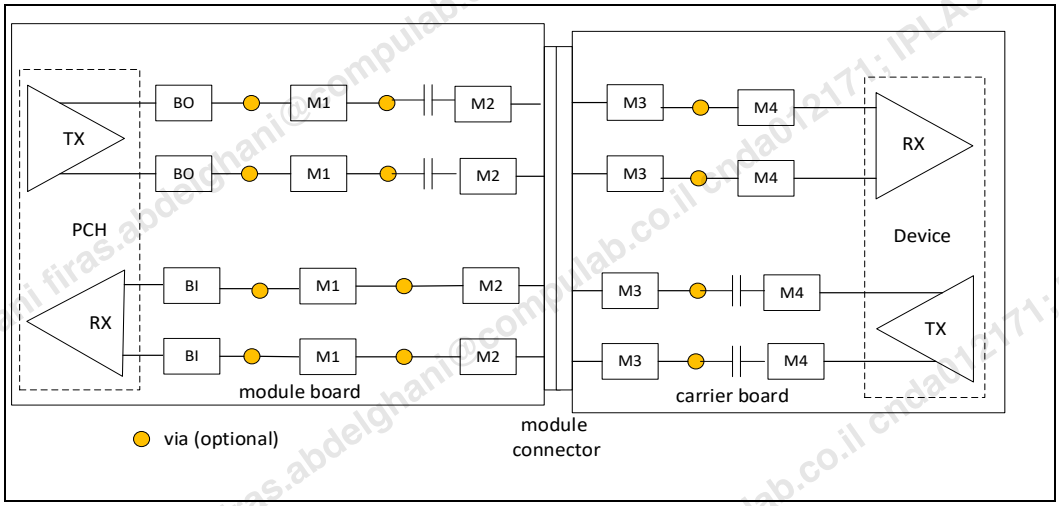

Table 39. Routing Guidelines for Gen 3 Device Down with COM Express Connector - TX

Parameter	Routing Guidelines			
Transmission Line Segment	BO	M1	M2	M3+M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS	MS/SL/DSL
Impedance (Ω)	-	85		
Trace Width (w)	same as main route	Meets Impedance		
Intra Pair Line Spacing	same as line width			
Microstrip				
Spacing - Signal to Equivalent Signal	2w	3w		
Spacing - Signal to Non-Equivalent Signal	3w	3w		
Stripline				
Spacing - Signal to Equivalent Signal	2.67w	4.3w		
Spacing - Signal to Non-Equivalent Signal	4w	4.3w		

Dual Stripline				
Spacing - Signal to Equivalent Signal	-	4w		
Spacing - Signal to Non-Equivalent Signal	-	4w		
Reference	VSS			
Max. Trace Segment Length	15.2mm	-	-	-
Max. Via Count	3			
Max. COM Express Module or Carrier Board Length	85.0mm			118.6mm
Max. Total Trace Segment Length	203.6mm			

NOTE:

1. Number of vias allowed: max. three vias (not counting microvia under package).
2. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
3. AC cap value: 176 to 265 nF; 220 nF nominal.
4. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2 mm.
5. Length matching between P and N within a diff. pair: within layer max. mismatch: 254 µm, total length max. mismatch: 127 µm.
6. Length matching between Tx pairs of multiple lanes: not required.
7. Length matching between Tx and Rx pairs: not required.
8. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88 µm at breakout and 200 µm at main route (currently to low-speed I/O) required.
9. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
10. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
11. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).

Table 40. Routing Guidelines for Gen 3 Device Down with COM Express Connector - RX

Parameter	Routing Guidelines				
Transmission Line Segment	BI	M1	M2	M3	M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL			MS
Impedance (Ω)	-	85			
Trace Width (w)	same as main route	Meets Impedance			
Intra Pair Line Spacing	same as line width				
Microstrip					
Spacing - Signal to Equivalent Signal	2w	3w			
Spacing - Signal to Non-Equivalent Signal	3w	3w			
Stripline					
Spacing - Signal to Equivalent Signal	2.67w	4.3w			
Spacing - Signal to Non-Equivalent Signal	4w	4.3w			
Dual Stripline					
Spacing - Signal to Equivalent Signal	-	4w			
Spacing - Signal to Non-Equivalent Signal	-	4w			
Reference	VSS				
Max. Trace Segment Length	15.2mm	-	-	-	8mm
Max. Via Count	3				
Max. COM Express Module or Carrier Board Length	85.0mm			118.6mm	
Max. Total Trace Segment Length	203.6mm				

NOTE:
1. Number of vias allowed: max. three vias (not counting microvia under package).
2. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition

that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.

3. AC cap value: 176 to 265 nF; 220 nF nominal.
4. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2 mm.
5. Length matching between P and N within a diff. pair: within layer max. mismatch: 254 µm, total length max. mismatch: 127 µm.
6. Length matching between Rx pairs of multiple lanes: not required.
7. Length matching between Tx and Rx pairs: not required.
8. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200 µm at main route (currently to low-speed I/O) required.
9. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
10. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
11. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).

8.2 Gen 3 M.2 connector with COM Express Connector

Figure 23. Gen 3 M.2 connector with COM Express Connector

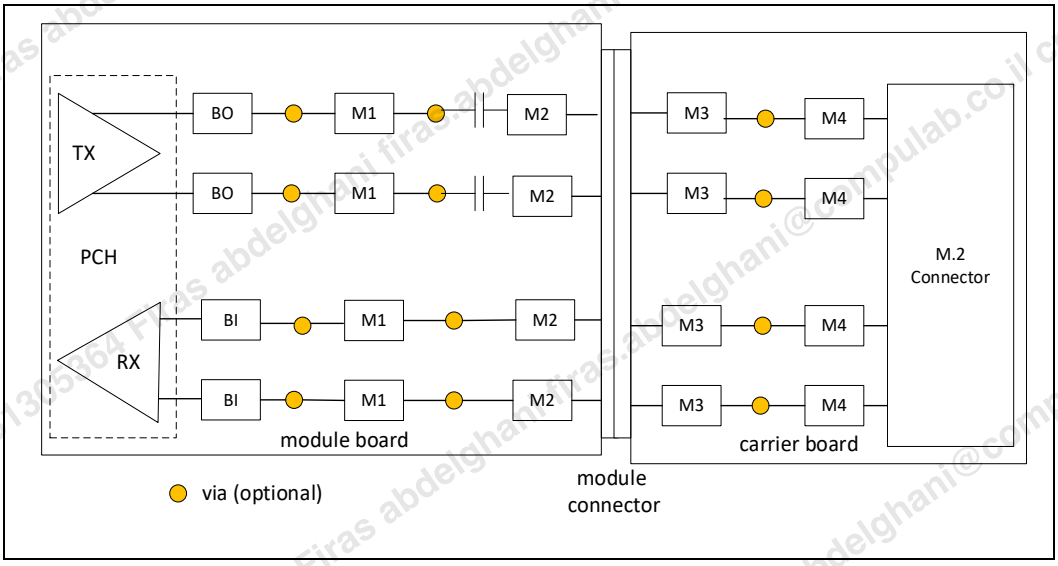

Table 41. Routing Guidelines for Gen 3 M.2 connector with COM Express Connector – TX

Parameter	Routing Guidelines			
Transmission Line Segment	BO	M1	M2	M3+M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS	MS/SL/DSL
Impedance (Ω)	-	85		
Trace Width (w)	same as main route	Meets Impedance		
Intra Pair Line Spacing	same as line width			
Microstrip				
Spacing - Signal to Equivalent Signal	2w	3w		
Spacing - Signal to Non-Equivalent Signal	3w	3w		
Stripline				
Spacing - Signal to Equivalent Signal	2.7w	4.3w		
Spacing - Signal to Non-Equivalent Signal	4w	4.3w		
Dual Stripline				
Spacing - Signal to Equivalent Signal	-	4w		
Spacing - Signal to Non-Equivalent Signal	-	4w		
Reference	VSS			
Max. Trace Segment Length	15.2mm	-	-	-
Max. Via Count	3			
Max. COM Express Module or Carrier Board Length	85.0mm			42.6mm
Max. Total Trace Segment Length	127.6mm			

NOTE:

1. Number of vias allowed: 3 for Tx (not counting via under package). Express card/M.2/Add-in card vias allowed: 1 (for Tx / Rx lanes).
2. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed

(di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.

3. AC cap value: 176 to 265 nF; 220 nF nominal. If multiplexing with SATA, see PCIe (cyan) tab of *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872) for further details.
4. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2 mm.
5. End-to-end maximum transmission line length: The max. length end-to-end from transmitter to receiver is 178 mm.
6. Add-in card at M.2 connector: The total length of the add-in card is usually 38mm to 50.4mm. The maximum breakout length on the add-in card is assumed to be 15.2 mm. The add-in card segment is a combination of MS/SL/DSL (MS where required to connect to surface mounted components). The add-in card segment has a typical via count of 1.
7. Length matching between P and N within a diff. pair: within layer max. mismatch: 254µm, total length max. mismatch: 127µm.
8. Length matching between Tx pairs of multiple lanes: not required.
9. Length matching between Tx and Rx pairs: not required.
10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.
11. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
12. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
13. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).

Table 42. Routing Guidelines for Gen 3 M.2 connector with COM Express Connector – RX

Parameter	Routing Guidelines				
Transmission Line Segment	BI	M1	M2	M3	M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL			MS/SL/DSL
Impedance (Ω)	-	85			
Trace Width (w)	same as main route	Meets Impedance			
Intra Pair Line Spacing	same as line width				
Microstrip					
Spacing - Signal to Equivalent Signal	2w	3w			
Spacing - Signal to Non-Equivalent Signal	3w	3w			

Stripline					
Spacing - Signal to Equivalent Signal	2.67w	4.3w			
Spacing - Signal to Non-Equivalent Signal	4w	4.3w			
Dual Stripline					
Spacing - Signal to Equivalent Signal	-	4w			
Spacing - Signal to Non-Equivalent Signal	-	4w			
Reference	VSS				
Max. Trace Segment Length	15.2mm	-	-	-	8mm
Max. Via Count	3				
Max. COM Express Module or Carrier Board Length	85.0mm			42.6mm	
Max. Total Trace Segment Length	127.6mm				

NOTE:

1. Number of vias allowed: 2 for RX (not counting via under package). Express card/M.2/Add-in card vias allowed: 1 (for Tx / Rx lanes).
2. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). If non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
3. AC cap value: 176 to 265 nF; 220 nF nominal. If multiplexing with SATA, see PCIe (cyan) tab of *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872) for further details.
4. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2 mm.
5. End-to-end maximum transmission line length: The max. length end-to-end from transmitter to receiver is 178 mm.
6. Add-in card at M.2 connector: The total length of the add-in card is usually 38mm to 50.4mm. The maximum breakout length on the add-in card is assumed to be 15.2 mm. The add-in card segment is a combination of MS/SL/DSL (MS where required to connect to surface mounted components). The add-in card segment has a typical via count of 1.
7. Length matching between P and N within a diff. pair: within layer max. mismatch: 254µm, total length max. mismatch: 127µm.
8. Length matching between Rx pairs of multiple lanes: not required.
9. Length matching between Tx and Rx pairs: not required.
10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.

11. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
12. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
13. Max. length values are for all the stackups in 607872_TGL_UP3_PDG_Rev*.xlsx "U Ref Stackup" tab.

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9.0 PCIe Clock

9.1 PCIe Clock to Device Down Through COM Express Connector

Figure 24. PCIe Clock to Device Down Topology Through COM Express Connector

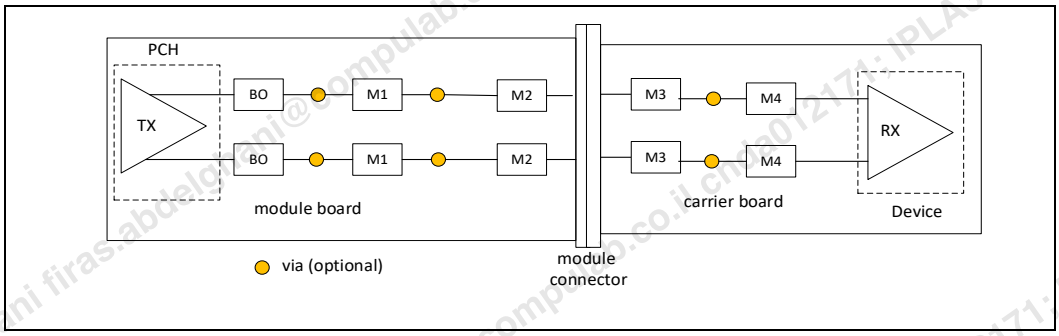

Table 43. Routing Guidelines for PCIe Clock to Device Down Topology Through COM Express Connector – Gen 4

Parameter	Routing Guidelines			
Transmission Line Segment	BO	M1	M2	M3+M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL		MS/SL/DSL
Impedance (Ω)	-	85		
Trace Width (w)	same as main route	Meets Impedance		
Intra Pair Line Spacing	same as line width			
IMicrostrip				
Spacing - Signal to Equivalent Signal	3w	5w		
Spacing - Signal to Non-Equivalent Signal	5w	7.6w		
Stripline				
Spacing - Signal to Equivalent Signal	4w	7.1w		
Spacing - Signal to Non-Equivalent Signal	6.7w	10.9w		

Dual Stripline				
Spacing - Signal to Equivalent Signal	-	6.7w		
Spacing - Signal to Non-Equivalent Signal	-	10.1w		
Reference	VSS			
Max. Trace Segment Length	12.7mm	-	25.4mm	-
Max. Via Count	4			
Max. COM Express Module or Carrier Board Length	100mm			192.1mm
Max. Total Trace Segment Length	292.1mm			

NOTE:

1. Minimum motherboard total length: 76.2mm.
2. Number of vias allowed: Max. four vias.
3. Reference plane: continuous ground only.
4. EMC/RF noise protection: For signal sections which are routed on MS (surface) layer, a GND ring/shield is advised to be added (with similar guidelines following a standard GND ring/shield such as for XTAL) with sufficient GND stitching vias for the length of the MS routed layer. GND ring/shield GND stitching vias should be placed at regular intervals of 4 - 12mm. It is advised to route in inner layer SL/DSL routing. Limit MS routed section and follow above shielding guidelines.
5. Length matching between P and N within a differential pair: Within same layer mismatch: 0.254mm. Total length mismatch: 0.381mm (TX to RX).
6. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).
7. Reference plane: continuous GND is recommended. Only applicable for Gen3 clocks : if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt).

Table 44. Routing Guidelines for PCIe Clock to Device Down Topology Through COM Express Connector – Gen 3 and below

Parameter	Routing Guidelines			
Transmission Line Segment	BO	M1	M2	M3+M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL		MS/SL/DSL
Impedance (Ω)	-	85		
Trace Width (w)	same as main route	Meets Impedance		
Intra Pair Line Spacing	same as line width			

Microstrip				
Spacing - Signal to Equivalent Signal	2w	3w		
Spacing - Signal to Non-Equivalent Signal	3w	3.8w		
Stripline				
Spacing - Signal to Equivalent Signal	2.7w	4.3w		
Spacing - Signal to Non-Equivalent Signal	4w	5.4w		
Dual Stripline				
Spacing - Signal to Equivalent Signal	-	4w		
Spacing - Signal to Non-Equivalent Signal	-	5w		
Reference	VSS			
Max. Trace Segment Length	12.7mm	-	25.4mm	-
Max. Via Count	4			
Max. COM Express Module or Carrier Board Length	100mm			192.1mm
Max. Total Trace Segment Length	292.1mm			

NOTE:

1. Minimum motherboard total length: 76.2mm.
2. Number of vias allowed: Max. four vias.
3. Reference plane: continuous ground only.
4. EMC/RF noise protection: For signal sections which are routed on MS (surface) layer, a GND ring/shield is advised to be added (with similar guidelines following a standard GND ring/shield such as for XTAL) with sufficient GND stitching vias for the length of the MS routed layer. GND ring/shield GND stitching vias should be placed at regular intervals of 4 - 12mm. It is advised to route in inner layer SL/DSL routing. Limit MS routed section and follow above shielding guidelines.
5. Length matching between P and N within a differential pair: Within same layer mismatch: 0.254mm. Total length mismatch: 0.381mm (TX to RX).
6. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).
7. Reference plane: continuous GND is recommended. If continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt).

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10.0 SATA

10.1 SATA with Internal Cable Through COM Express Connector

Figure 25. Direct connect with Internal Cable and COM Express Connector

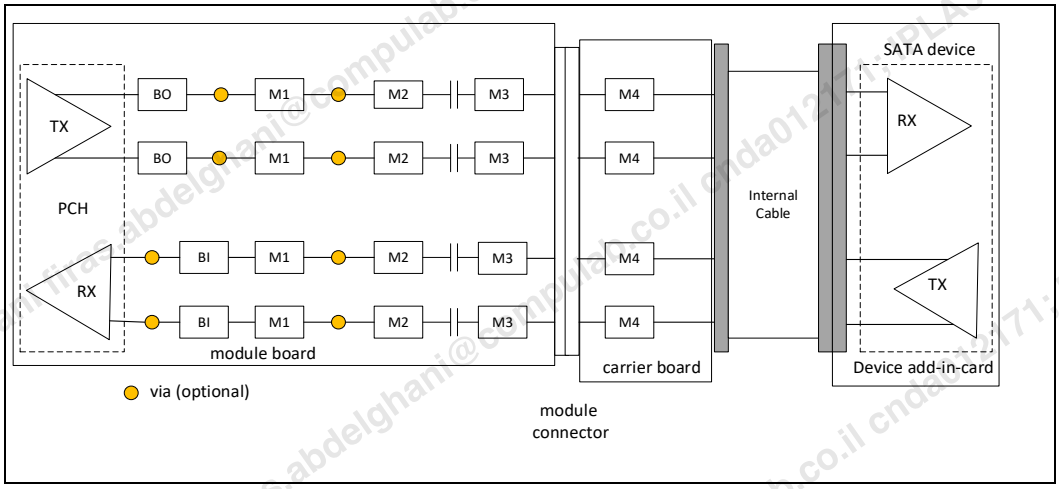

Table 45. Routing Guidelines for SATA with Internal Cable Topology Through COM Express Connector -TX

Parameter	Routing Guidelines				
Transmission Line Segment	BO/BI	M1	M2	M3	M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS		MS/SL/DSL
Impedance (Ω)	-	85			
Trace Width (w)	same as main route	Meets Impedance			
Intra Pair Line Spacing	same as line width				
Microstrip					
Spacing - Signal to Equivalent Signal	2w	3w			
Spacing - Signal to Non-Equivalent Signal	3w	3w			

Stripline					
Spacing - Signal to Equivalent Signal	2.67w	4.3w	-		4.3w
Spacing - Signal to Non-Equivalent Signal	4w	4.3w	-		4.3w
Dual Stripline					
Spacing - Signal to Equivalent Signal	-	4w	-		4w
Spacing - Signal to Non-Equivalent Signal	-	4w	-		4w
Reference	VSS				
Max. Trace Segment Length	15.2mm	-	-	10mm	-
Max. Via Count	2				
Max. COM Express Module or Carrier Board Length	50.8mm				76.2mm
Max. Total Trace Segment Length	127.0mm				

NOTE:

1. Number of vias allowed: 2 vias.
2. Minimum total length: 50.8mm.
3. AC cap value: 10nF.
4. Reference plane: continuous GND recommended. if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
5. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2mm.
6. Length matching between P and N within a diff. pair: Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm.
7. Length matching between Tx pairs of multiple lanes: not required.
8. Length matching between Rx pairs of multiple lanes: not required.
9. Length matching between TX and Rx pairs: not required.
10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.
11. Cable loss vs channel length trade-off table: See SATA without Daughter Card with Internal Cable Routing Length versus Cable Loss figure
12. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.

13. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes. See SATA with Daughter Card with Internal Cable Routing Length versus Cable Loss figure
14. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872)

Table 46. Routing Guidelines for SATA with Internal Cable Topology Through COM Express Connector -RX

Parameter	Routing Guidelines				
Transmission Line Segment	BO/BI	M1	M2	M3	M4
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS		MS/SL/DSL
Impedance (Ω)	-	85			
Trace Width (w)	same as main route	Meets Impedance			
Intra Pair Line Spacing	same as line width				
Microstrip					
Spacing - Signal to Equivalent Signal	2w	3w			
Spacing - Signal to Non-Equivalent Signal	3w	3w			
Stripline					
Spacing - Signal to Equivalent Signal	2.67w	4.3w	-		4.3w
Spacing - Signal to Non-Equivalent Signal	4w	4.3w	-		4.3w
Dual Stripline					
Spacing - Signal to Equivalent Signal	-	4w	-		4w
Spacing - Signal to Non-Equivalent Signal	-	4w	-		4w
Reference	VSS				
Max. Trace Segment Length	15.2mm	-	-	10mm	-
Max. Via Count	2				
Max. COM Express Module or Carrier Board Length	50.8mm				76.2mm
Max. Total Trace Segment Length	127.0mm				

NOTE:
1. Number of vias allowed: 2 vias.

2. Minimum total length: 50.8mm.
3. AC cap value: 10nF.
4. Reference plane: continuous GND recommended. . if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
5. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2mm.
6. Length matching between P and N within a diff. pair: Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm.
7. Length matching between Tx pairs of multiple lanes: not required.
8. Length matching between Rx pairs of multiple lanes: not required.
9. Length matching between TX and Rx pairs: not required.
10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.
11. Cable loss vs channel length trade-off table: See SATA without Daughter Card with Internal Cable Routing Length versus Cable Loss figure
12. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
13. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes. See SATA with Daughter Card with Internal Cable Routing Length versus Cable Loss figure
14. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872)

Table 47. SATA without Daughter Card with Internal Cable Routing Length vs Cable Loss

Total Trace Length on Module and Carrier Boards (mm)	Internal Cable Assembly Insertion Loss Recommendation up to 3GHz
50.8	≤3.6dB
76.2	≤3.0dB
101.6	≤2.3dB
127	≤2.0dB

Figure 26. Direct Connect with Daughter Card, Internal Cable, and COM Express Connector

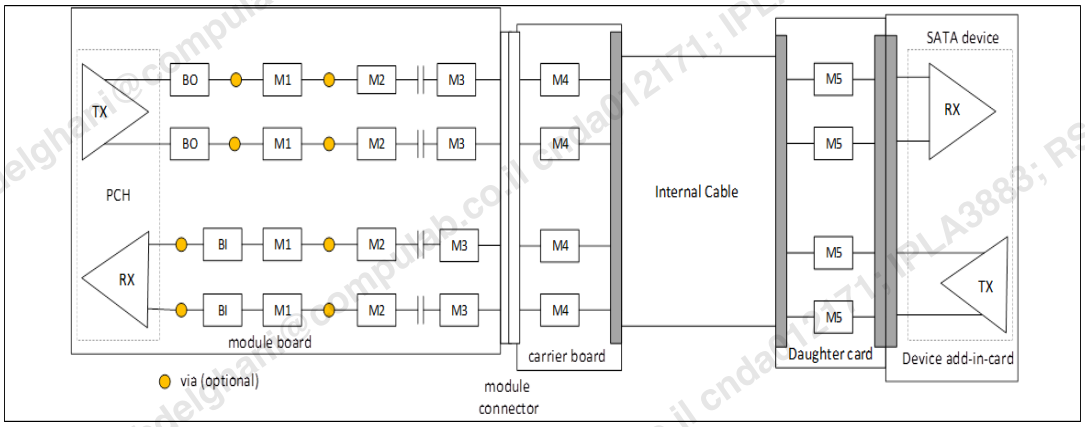

Table 48. Routing Guidelines for SATA with Daughter Card, Internal Cable, and COM Express Connector -TX

Parameter	Routing Guidelines					
Transmission Line Segment	BO	M1	M2	M3	M4	M5
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS		MS/SL/DSL	
Impedance (Ω)	-	85				
Trace Width (w)	same as main route	Meets Impedance				
Intra Pair Line Spacing	same as line width					
Microstrip						
Spacing - Signal to Equivalent Signal	2w	3w				
Spacing - Signal to Non-Equivalent Signal	3w	3w				

Stripline					
Spacing - Signal to Equivalent Signal	2.7w	4.3w			
Spacing - Signal to Non-Equivalent Signal	4w	4.3w			
Dual Stripline					
Spacing - Signal to Equivalent Signal	-	4w			
Spacing - Signal to Non-Equivalent Signal	-	4w			
Reference	VSS				
Max. Trace Segment Length	15.2mm	-	-	10mm	-
Max. Via Count	2				
Max. COM Express Module or Carrier Board Length	50.8mm			25.4mm	50.8mm
Max. Total Trace Segment Length	127.0mm				

NOTE:

1. Number of vias allowed: 2 vias.
2. Minimum total length: 50.8mm.
3. AC cap value: 10nF.
4. Reference plane: continuous GND recommended. See Power Referencing tab for power referencing guidelines. if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
5. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2mm.
6. Length matching between P and N within a diff. pair: Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm.
7. Length matching between Tx pairs of multiple lanes: not required.
8. Length matching between Rx pairs of multiple lanes: not required.
9. Length matching between TX and Rx pairs: not required.

10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.
11. Cable loss vs channel length trade-off table: See SATA with Daughter Card with Internal Cable Routing Length versus Cable Loss figure
12. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.
13. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
14. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).
15. Daughter card length (M5 segment): typical length of daughter card is approximately 50.8mm.

Table 49. Routing Guidelines for SATA with Daughter Card, Internal Cable, and COM Express Connector -RX

Parameter	Routing Guidelines					
Transmission Line Segment	BO	M1	M2	M3	M4	M5
PCB Routing Layer(s)	MS/SL	MS/SL/DSL	MS		MS/SL/DSL	
Impedance (Ω)	-	85				
Trace Width (w)	same as main route	Meets Impedance				
Intra Pair Line Spacing	same as line width					
Microstrip						
Spacing - Signal to Equivalent Signal	2w	3w				
Spacing - Signal to Non-Equivalent Signal	3w	3w				
Stripline						
Spacing - Signal to Equivalent Signal	2.7w	4.3w				
Spacing - Signal to Non-Equivalent Signal	4w	4.3w				

Dual Stripline					
Spacing - Signal to Equivalent Signal	-	4w			
Spacing - Signal to Non-Equivalent Signal	-	4w			
Reference	VSS				
Max. Trace Segment Length	15.2mm	-	-	10mm	-
Max. Via Count	2				
Max. COM Express Module or Carrier Board Length	50.8mm			25.4 mm	50.8mm
Max. Total Trace Segment Length	127.0mm				

NOTE:

1. Number of vias allowed: 2 vias.
2. Minimum total length: 50.8mm.
3. AC cap value: 10nF.
4. Reference plane: continuous GND recommended. See Power Referencing tab for power referencing guidelines. if continuous GND cannot be implemented, a combination of GND on one side and continuous power plane on the other with the condition that the GND plane be the closer reference (dual-reference) can be implemented. The continuous power plane requires low peak-to-peak noise and low current switching speed (di/dt). if non-continuous power referencing is required on microstrip/surface layer, signal can reference over power planes with a low peak-to-peak noise and low current switching speed (di/dt), but stitching caps are required over each plane split and need to be placed within 6mm of a signal running across the plane split.
5. Breakout length and spacing: an initial breakout segment of 4mm in length with a tighter pair-to-pair spacing of 0.11mm - 0.16mm is allowed. The total breakout length is still 15.2mm.
6. Length matching between P and N within a diff. pair: Within same layer mismatch: 0.254mm, Total length mismatch: 0.127mm.
7. Length matching between Tx pairs of multiple lanes: not required.
8. Length matching between Rx pairs of multiple lanes: not required.
9. Length matching between TX and Rx pairs: not required.
10. MODPHY_RCOMP P/N sideband/Comp signals: 100 Ohm +/-1% differential routing between RCOMP_P and RCOMP_N. Length matching and closely coupled routing as per standard differential pair. DC-resistance of <0.5 ohm is required (no specific trace width, only to meet DC-R target). Isolation of 88µm at breakout and 200µm at main route (currently to low-speed I/O) required.
11. Cable loss vs channel length trade-off table: See SATA with Daughter Card with Internal Cable Routing Length versus Cable Loss figure
12. Voiding recommendation for mainstream stackup: It is recommended to void pads for all components for example AC caps as well as connector pads to optimize the impedance matching in the channel.

13. Discrete component part size for mainstream stackup: Recommended to use 0402 or smaller component sizes.
14. The max. length applies to all the stackups in the 'U Ref Stackup' tab in the *11th Gen Intel® Core™ Processor UP3 UP4 Platform Design Guide* (RDC #607872).
15. Daughter card length (M5 segment): typical length of daughter card is approximately 50.8mm.

Table 50. SATA with Daughter Card with Internal Routing Length vs. Cable loss

Total Trace Length on Module and Carrier Boards and Daughter Card (mm)	Internal Cable Assembly Insertion Loss Recommendation up to 3GHz
50.8	≤3.6dB
76.2	≤3.0dB
101.6	≤2.3dB
127	≤2.0dB

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11.0 Time-Aware GPIO

Time-Aware GPIO (TGPIO) is used for scheduled trigger and event timestamping. It is one of the features of Time-Synchronization Support in 11th Gen Intel® Core™ processors.

11.1 Time-Aware GPIO Description

Table 51. Time-Aware GPIO Description

Signal Name	Type (Voltage Domain)	Direction	Description
TIME_SYNC_0	CMOS (1.8V)	Input	Time-Aware GPIO Input signal
TIME_SYNC_1	CMOS (1.8V)	Output	Time-Aware GPIO Output signal

11.2 Time-Aware GPIO Routing Guidelines

For Time-Aware GPIO routing guidelines, refer to the GPIO point-to-point routing guidelines in the “607872_TGL_UP3_PDG_Rev*.xlsx” (RDC #607872) in “PCH GPIO” tab.

Strapping resistor is not required since the Voltage Domain Type is CMOS.

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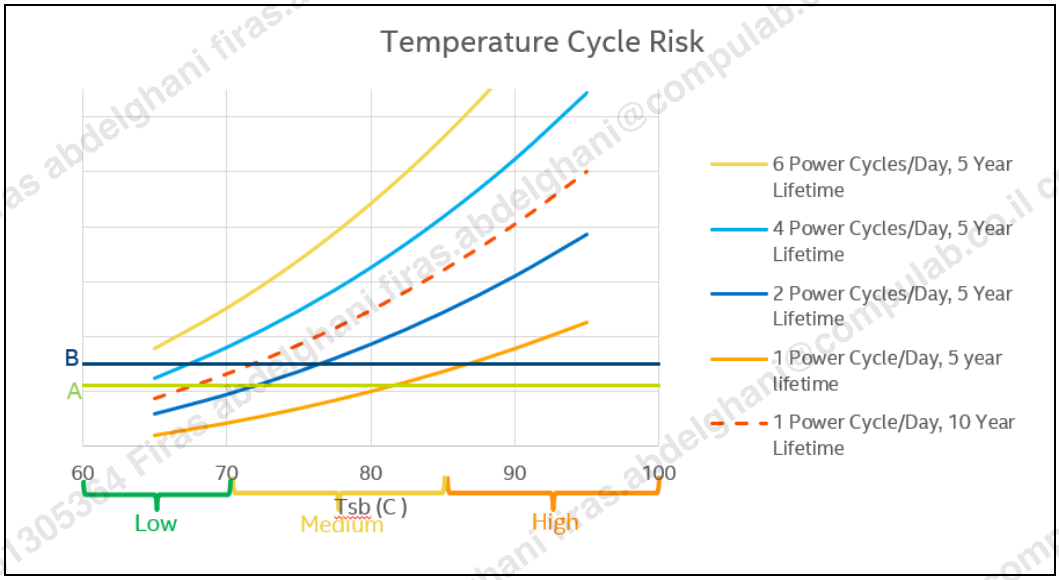
12.0 11th Gen Intel® Core™ Processors Adhesives Guidance

12.1 Adhesives Guidance

Intel recommends the use of board level underfill (BLUF) or corner glue/fill (CG/CF) for 11th Gen Intel® Core™ processors for certain product use cases. The below chart is a guideline for temperature cycle risk based on solder ball temperature and power cycles.

If your product falls above Line A, CG, or CF may be advisable to increase the capability of the package solder joints. If your product falls above Line B, BLUF is recommended to ensure no failures over product lifetime. For more information and manufacturing guidance, please see the documents titled *Manufacturing with the Intel Platform Code Named Tiger Lake* (RDC #613010) and *Manufacturing with Intel Products Adhesive Guidance for Ball Grid Array and Package on Package* (RDC #573768).

Figure 27. Temperature Cycle Risk



Note: **Tsb Guidelines:**

Tsb (Temperature at solder ball) is dependent on silicon junction temperature as well as the heat dissipation of the thermal solution. The below ranges are a general guideline for determining Tsb range without having a full system thermal model available.

High Tsb:

E.x.: passive metal heat sink with no air flow, closed chassis

Medium Tsb:

E.x.: heavy heat sink with some air circulation (i.e.: vented chassis)

Low Tsb:

E.x.: heavy desktop-like heat sink with forced air flow (i.e.: integrated fan)

12.2 Assumptions/Definitions

It has two assumptions: power cycle and ambient temperature.

12.2.1 Power Cycle

It has two type of power cycle: On-to-Off Cycle (assuming cooling down to ambient temperature when off) and another is On-to-Standby Cycle (assuming cooling to near-ambient temperatures when in standby)

12.2.2 Ambient Temperature

Ambient temperature is temperature external to system (room temperature) and assumed to be 24°C.

The given product temperature cycle risk assumes a minimum 28 mm board with a 15 lb load and no backing plate. Changes in board thickness, loading, or presence of a backing plate can affect temperature cycle risk.

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