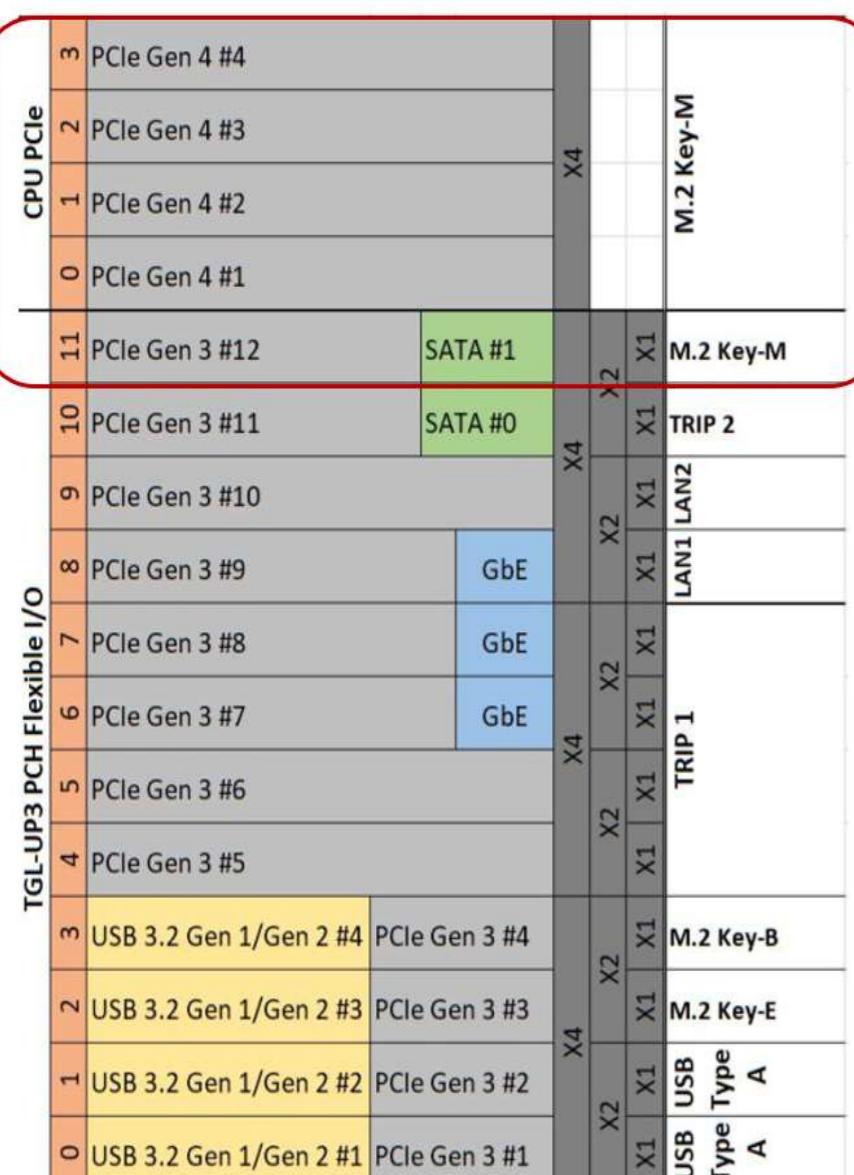


OPTION 1: TRIP1 is PCIe x4, TRIP2: PCIe x1 or SATA

OPTION 2: TRIP1 is 2x(PCIE x1), TRIP2: only SATA



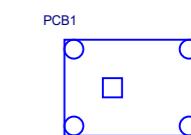
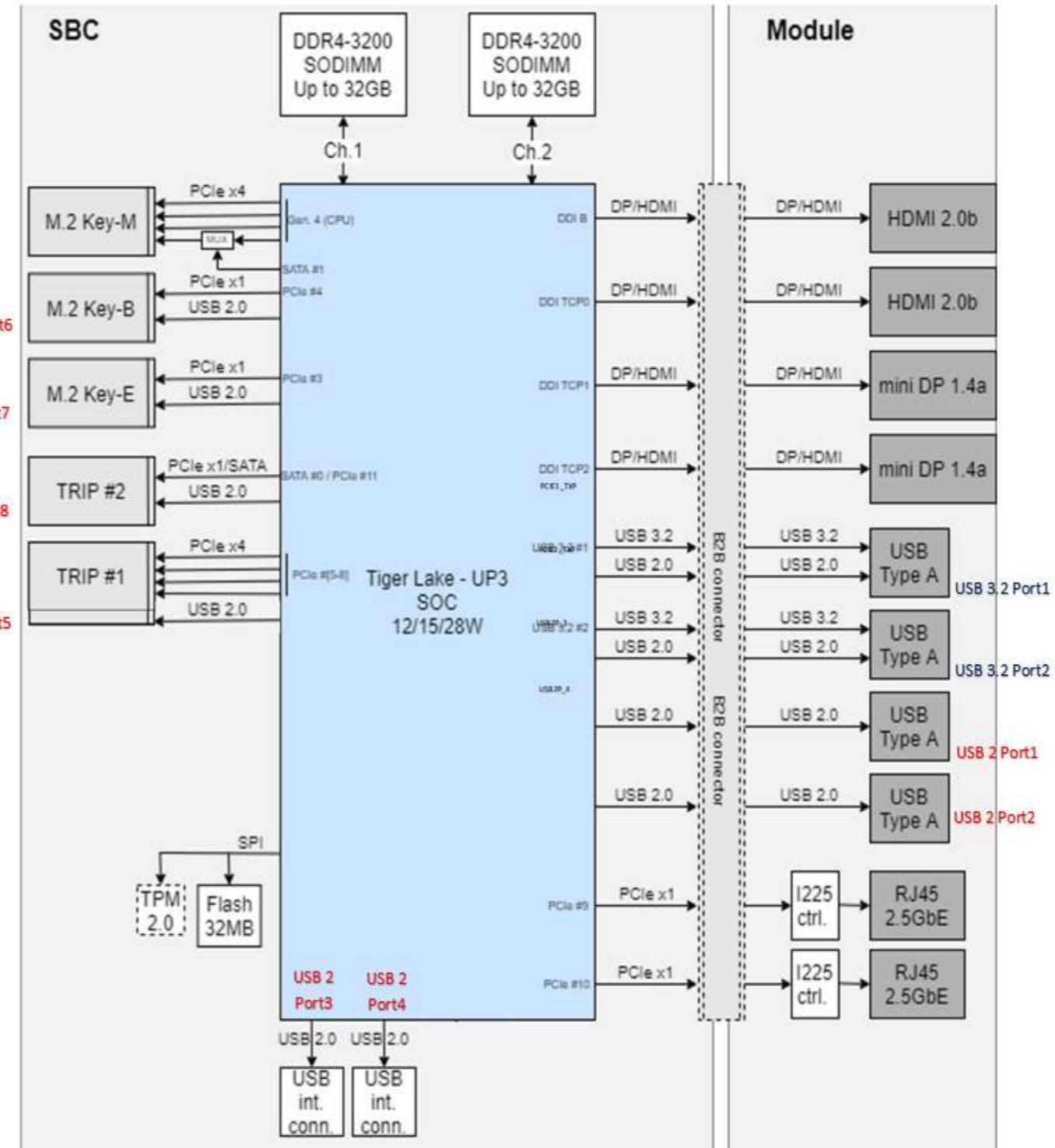
Tiger Lake UP3 Platform

Tiger Lake UP3 Key Feature Summary

Feature	Description
Thermal (Soc)	UP3 4+2: 15W
SoC	TGL UP3 CPU (4+2) PCH - LP
CPU IO	PCIe Gen4, 4x Type-C (TBT, USB 4.0, DP), DDR4,LPDDR4x, LPDDR5, CSI, DSI, DDI, eDP
PCH-LP	12 lanes HSIO, USB2, USB 3.2, eSPI, SPI, LPSS, I2C, SMBus
Power Delivery	CPU FIVR/PCH FIVR w/discrete VR ROP USB-C PD Controller
Memory	DDR4 - Max 64GB @ 3200MT/s LPDDR4x - Max 32GB @ 4266MT/s
Storage	PCIe/SATA
Boot	SPI NOR
Discrete Graphics	Optional x4 PCIe - Hybrid Graphics support w/Hot Plug
Internal Display	eDP , MIPI DSI
External displays	4 Wired Type-C (DP/TBT) Wireless (Miracast2.0 r2) (Wi-Fi) DDI(DP, HDMI)
Wireless	Quasar CNVI w/Harrison Peak (Wi-Fi/BT) module WWAN - XMM 7560
Clocking	38.4MHz Platform Xtal
Wired COMMs	Integrated GbE w/ discrete Gbit Lan Phy

continued...

Feature	Description
Imaging	4x WF/UF 2D Camera - (13MP WF, 2MP UF, 2MP Others) Other Cameras: AutoFocus, Face Tracking, Image Biometrics
Docking/Walk-up-Port	4x Ports Max: Type-C/Type-A
Audio	3.5mm Headphone Jack, Integrated Speakers/Mic, Docking Soundwire, Intel HD Audio, I2S, USB
Sensors	Ambient Light Sensor, Gyroscope, Accelerometer, Compass, Proximity, Pressure
Misc, GPIO's	Power/Vol button/Indicator LEDs/Keyboard/Touchpad/etc



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MCP -DP\HDMI



Name	Type	Description
GPP_E14 / DDSP_HPD1 / DISP_MISC1	I	Display Port A: HPD Hot-Plug Detect
GPP_A18 / DDSP_HPD2 / DISP_MISC2 / I2S4_RXD	I	Display Port B: HPD Hot-Plug Detect
GPP_A19 / DDSP_HPD1 / DISP_MISC1 / I2S5_SCLK	I	TCP Port 1: HPD Hot-Plug Detect
GPP_A20 / DDSP_HPD2 / DISP_MISC2 / I2S5_SFRM	I	TCP Port 2: HPD Hot-Plug Detect
GPP_A14 / USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1	I	TCP Port 3: HPD Hot-Plug Detect
GPP_A15 / USB_OC2#/DDSP_HPD4/DISP_MISC4 / I2S4_SCLK	I	TCP Port 4: HPD Hot-Plug Detect

5.3 Display Interfaces

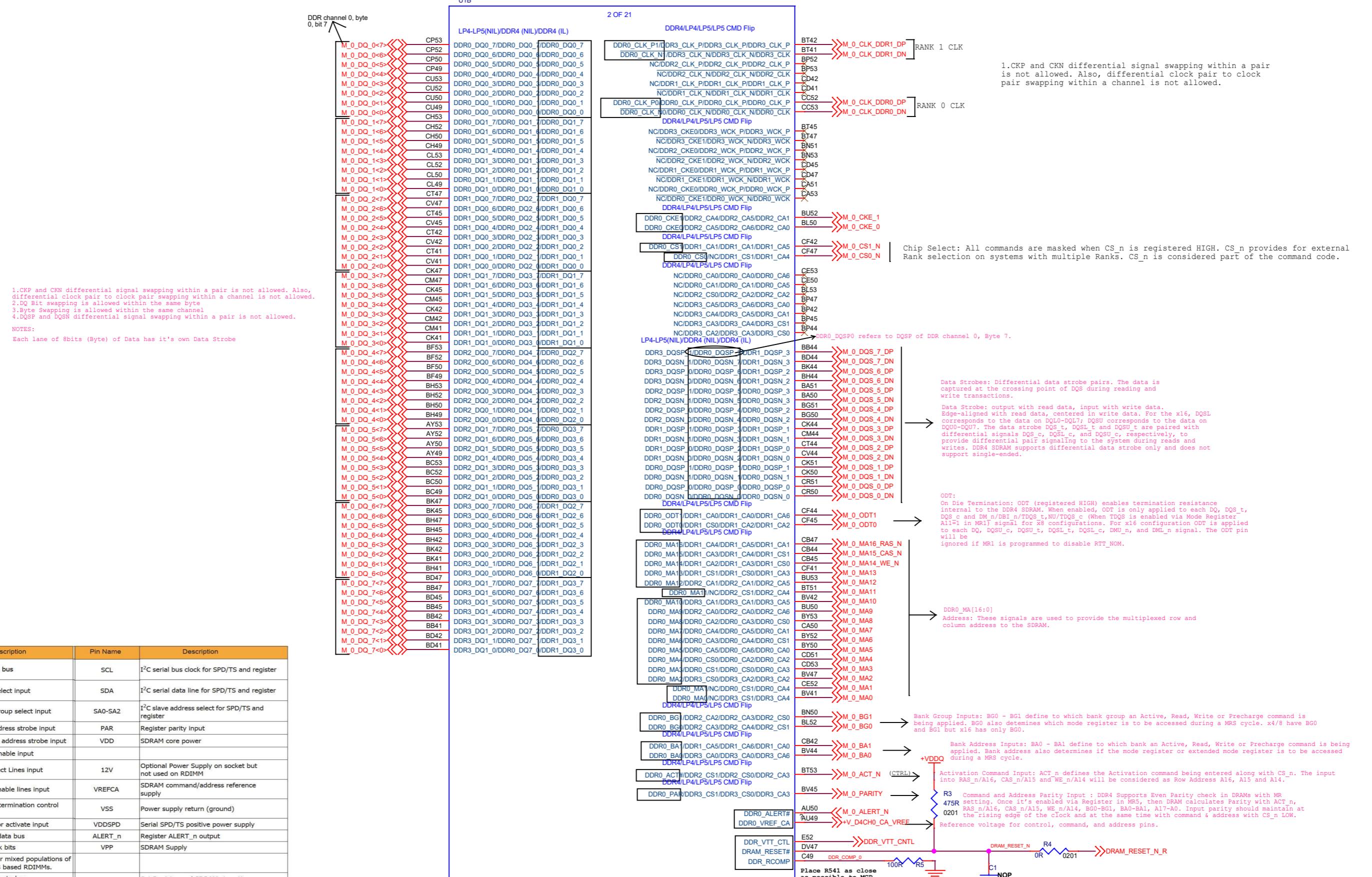
Table 33. DDI Ports Availability

SKU	UP4 Processor Line	UP3 Processor Line
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	eDP*/DP*/HDMI*/MIPI_1	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*

Note: HBR3 supported on TCP ports only.
Each of the TCP port can support DPoC* (DisplayPort* over Type-C)

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MEMORY CHANNEL A



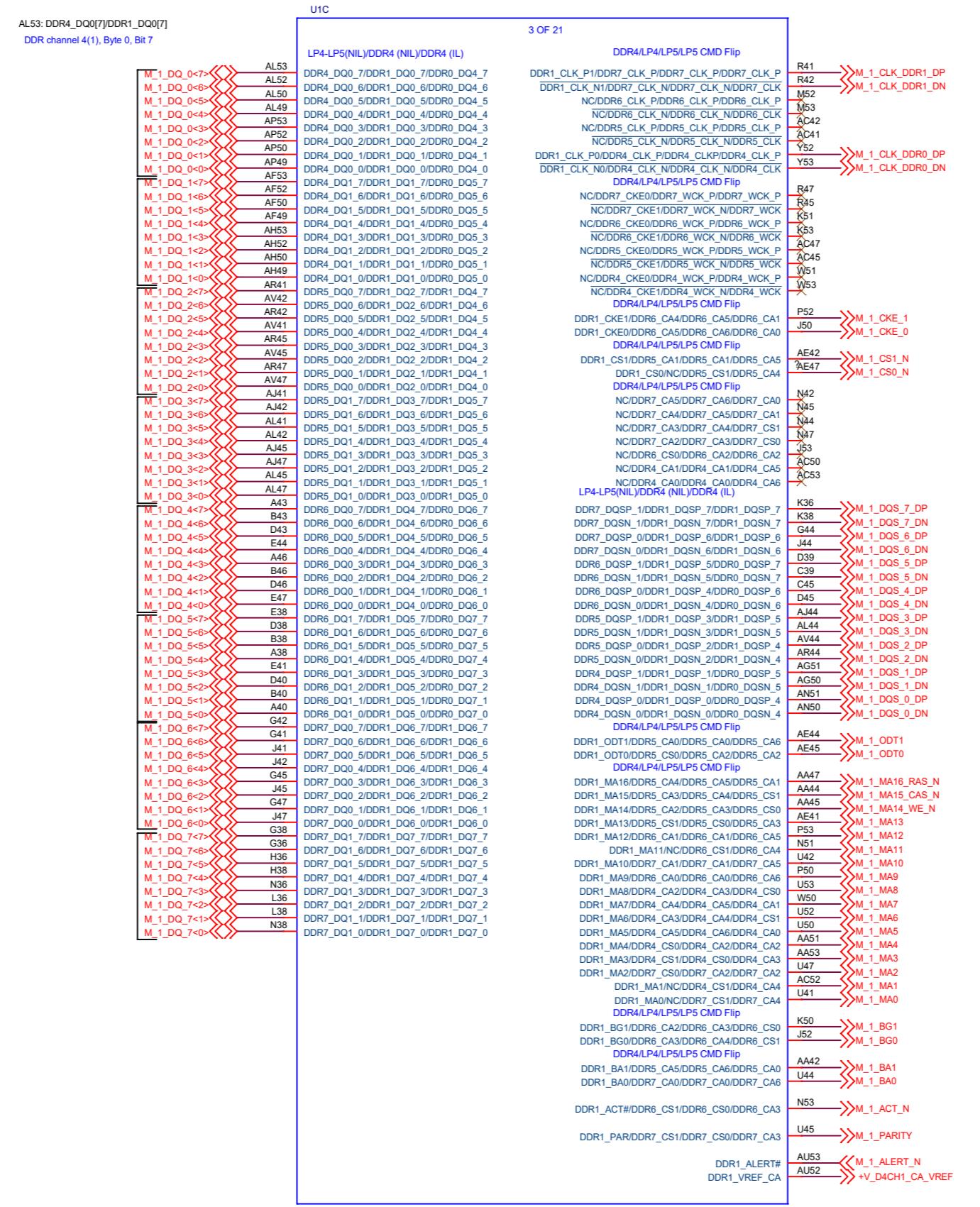
Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I ² C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I ² C serial data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0-SA2	I ² C slave address select for SPD/TS and register
RAS_n ²	Register row address strobe input	PAR	Register parity input
CAS_n ³	Register column address strobe input	VDD	SDRAM core power
WE_n ⁴	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12V	Optional Power Supply on socket but not used on RDIMM
CKE0, CEK1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODTO, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CBO-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQSO_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

1. BAS_n is a multiplexed function with A16

1. RAS_H is a multiplexed function with A18.
2. CAS_H is a multiplexed function with A15.

3. WE_n is a multiplexed function with A14.

MEMORY CHANNEL B



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CATERR#

Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLks. Legacy IERRs, CATERR# remains asserted until warm or cold reset.

PROCHOT#

The PROCHOT# (processor hot) signal is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling. The PROCHOT# signal can be configured to the following modes:

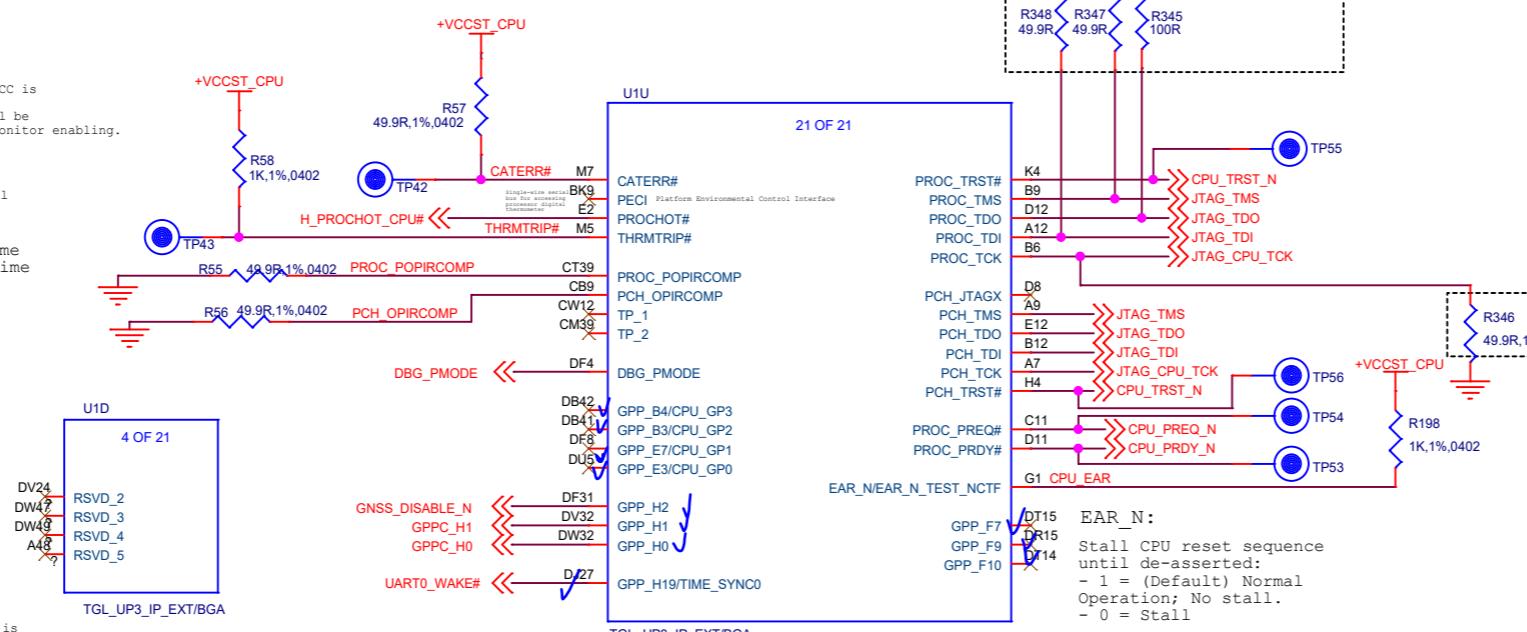
- Input Only: PROCHOT is driven by an external device.
- Output Only: PROCHOT is driven by processor.
- Bi-Directional: Both Processor and external device can drive PROCHOT signal

Time Synchronization GPIO 0: Timed GPIO event for time synchronization for interfaces that do not support time synchronization natively.

Time Synchronization: Used for synchronization both input (latch time when pin asserted) and output (toggle pin when programmed time is hit).

TIME_SYNC:
The PCH supports two Timed GPIOs as native function (TIME_SYNC) that is muxed on GPIO pins. The intent usage of the Timed GPIO function is for time synchronization purpose.

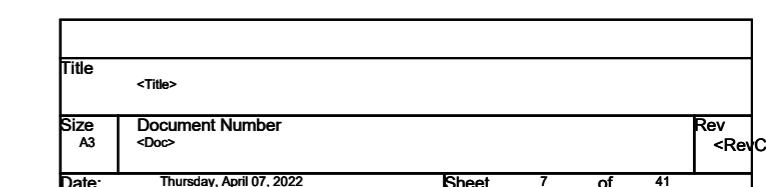
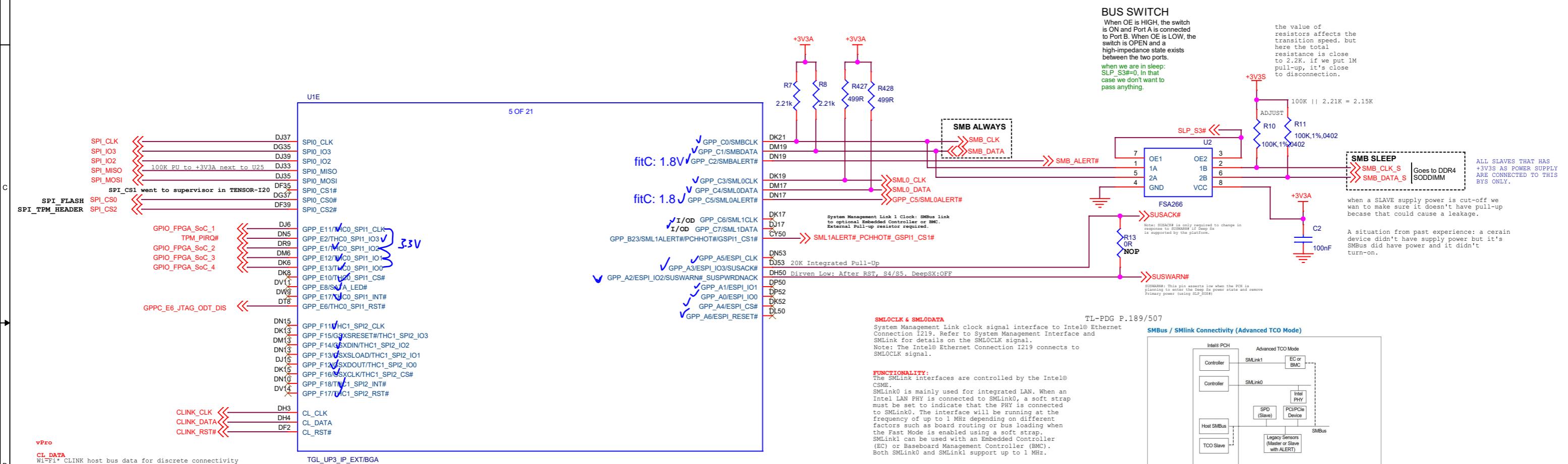
- Timed GPIO can be an input or an output.
- As an input, a GPIO input event triggers the HW to capture the PCH Always Running Timer (ART) time in the Time Capture register. The GPIO input event must be asserted for at least two crystal oscillator clocks period in order for the event to be recognized.
- As an output, a match between the ART time and the software programmed time value triggers the HW to generate a GPIO output event and capture the ART time in the Time Capture register. If periodic mode is enabled, HW generates the periodic GPIO events based on the programmed interval. The GPIO output event is asserted by HW for at least two crystal oscillator clocks period.

**Processor Internal Pull-Up / Pull-Down Terminations**

Signal Name	Pull Up/Pull Down	Rail	Value
BPM#[3:0]	Pull Up/Pull Down	VCC _{IO_OUT}	16-60 Ω
PROC_PREQ#	Pull Up	VCC _{STG}	3 kΩ
PROC_TDI	Pull Up	VCC _{STG}	3 kΩ
PROC_TMS	Pull Up	VCC _{STG}	3 kΩ
PROC_TDO	Pull Down	VCC _{STG}	3 kΩ
PROC_TDI	Pull Down	VCC _{STG}	3 kΩ
PROC_TCK	Pull Down	VCC _{STG}	3 kΩ
CFG[17:0]	Pull Up	VCC _{IO_OUT}	3 kΩ

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BPM#[3:0]	Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	UP3/UP4/H Processor Lines
PROC_PRDY#	Probe Mode Ready: PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	O	OD	SE	UP3/UP4/H Processor Lines
PROC_PREQ#	Probe Mode Request: PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TCK	Test Clock: This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal should be driven low or allowed to float during power on Reset.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TDI	Test Data In: This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TDO	Test Data Out: This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O	OD	SE	UP3/UP4/H Processor Lines
PROC_TMS	Test Mode Select: A JTAG specification support signal used by debug tools.	I	GTL	SE	UP3/UP4/H Processor Lines
PROC_TRST#	Test Reset: Resets the Test Access Port (TAP) logic. This signal should be driven low during power on Reset. Refer to the appropriate processor Debug Port Design Guide (Refer to Section 1.10, "Related Documents") for complete implementation details.	I	GTL	SE	UP3/UP4/H Processor Lines

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AUDIO HAS NOT BEEN
IMPLEMENTED IN TENSOR I22.
INSTEAD, AUDIO TEL IS USED
AND IT ONLY NEEDS USB
SIGNALS. (P2)

6.11 SoundWire* Interface Design Guidelines

For the Tiger Lake platform, SoundWire* is still the newest audio interface targeting (but not limited to) the phone, mobile, and desktop market as an alternative to Slimbus. Its main advantage is the connection simplicity with a 2 wire multi-drop topology + PDM streaming capabilities. For the Tiger Lake PCH there are 4 separate SoundWire interfaces that can be used.

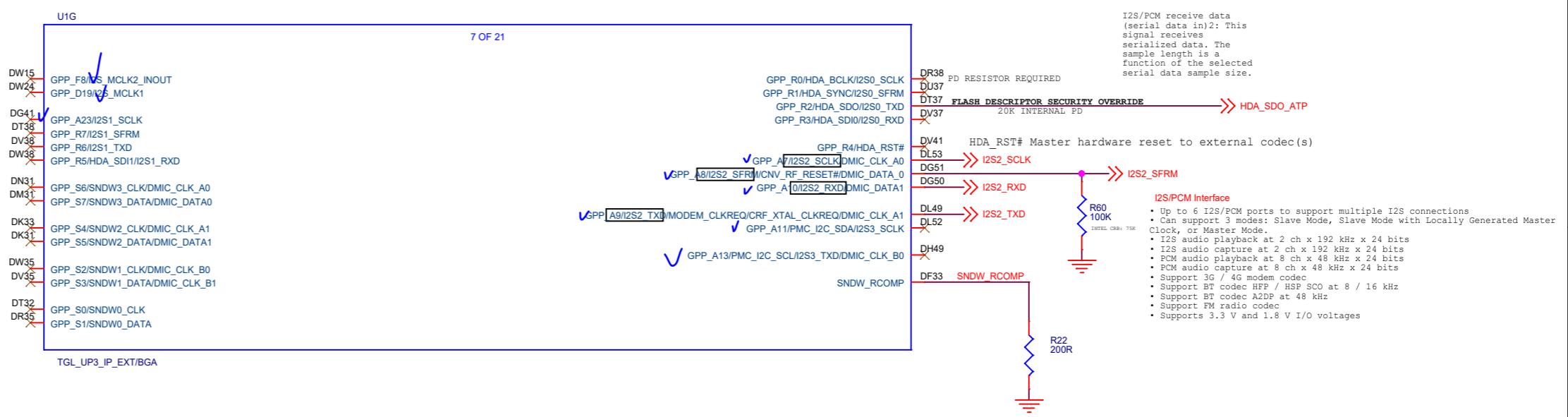
6.11.1 SoundWire® Platform Specific Important Information

On the Tiger Lake platform the SoundWire* interface and other audio interfaces can be configured by itself or at the same time with other interfaces for connection to end devices. Refer Tiger Lake PCH-LP External Design Specification (#576591) for specific pin assignments.

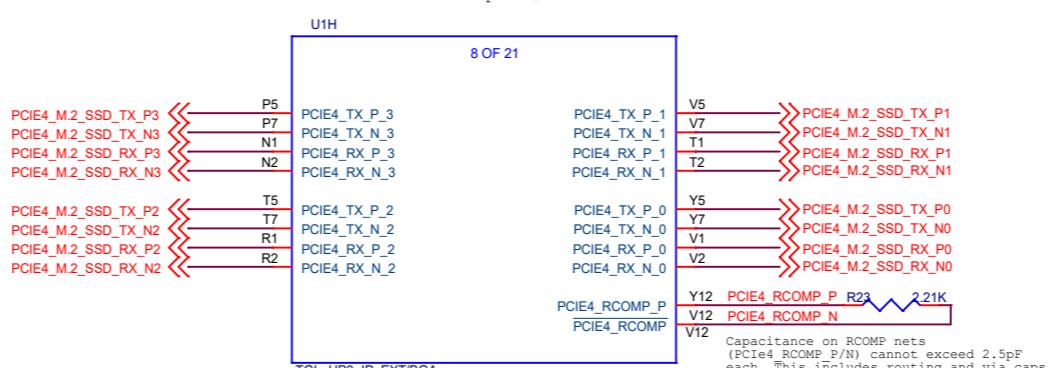
6.11.2 SoundWire® Signal Description

Table 87 SoundWire® Signals

Signal Name	Description
SNDW0_DATA	SoundWire Data 0: Serialized data line containing frame and data being transmitted /Received
SNDW0_CLK	SoundWire Clock 0: Serial bit clock used to control the timing of a transfer.
SNDW1_DATA	SoundWire Data 1: Serialized data line containing frame and data being transmitted /Received
SNDW1_CLK	SoundWire Clock 1: Serial bit clock used to control the timing of a transfer.
SNDW2_DATA	SoundWire Data 2: Serialized data line containing frame and data being transmitted /Received
SNDW2_CLK	SoundWire Clock 2: Serial bit clock used to control the timing of a transfer.
SNDW3_DATA	SoundWire Data 3: Serialized data line containing frame and data being transmitted /Received
SNDW3_CLK	SoundWire Clock 3: Serial bit clock used to control the timing of a transfer



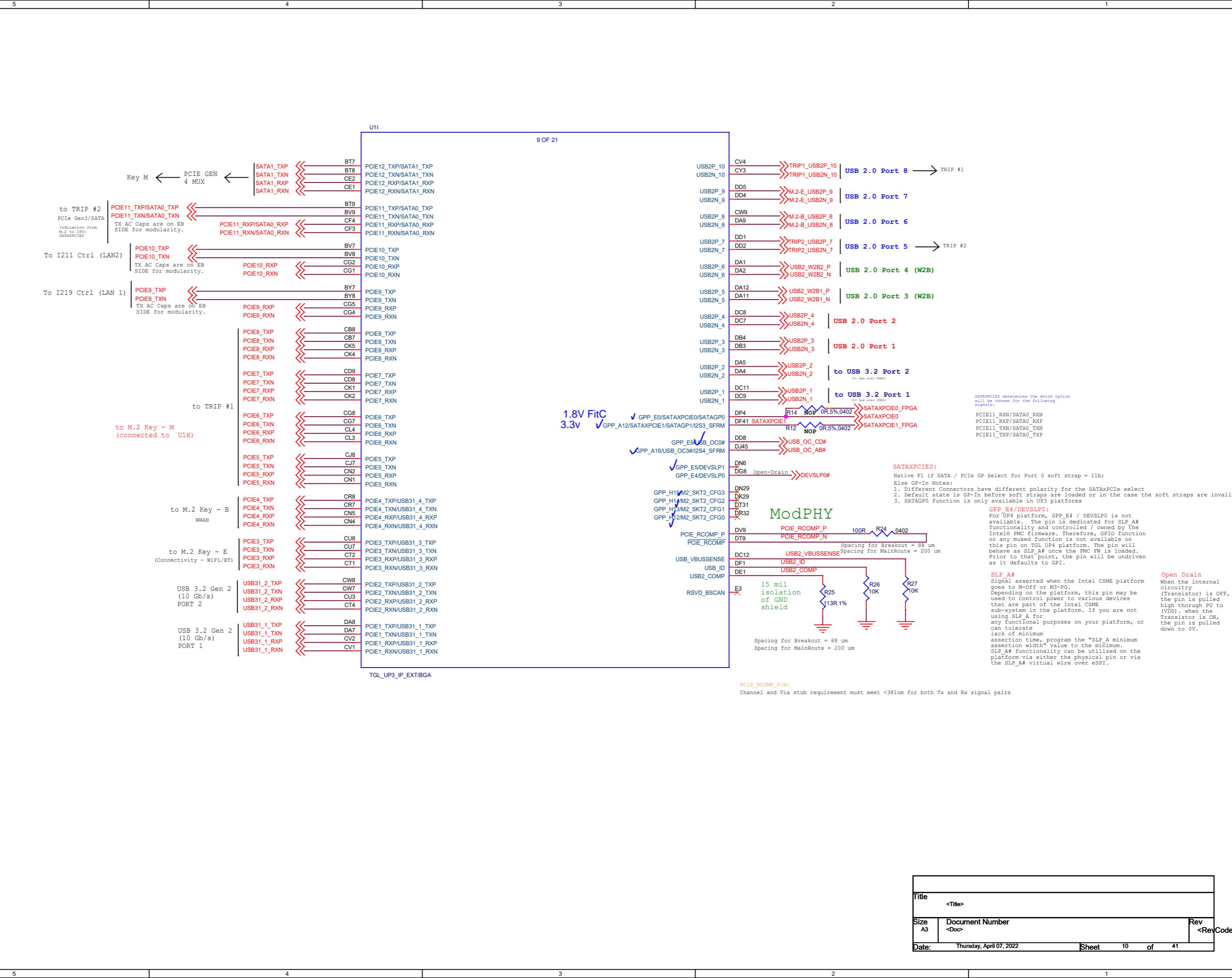
PCIe GEN 4 CAPS: n. 158/370 in MI_SPC

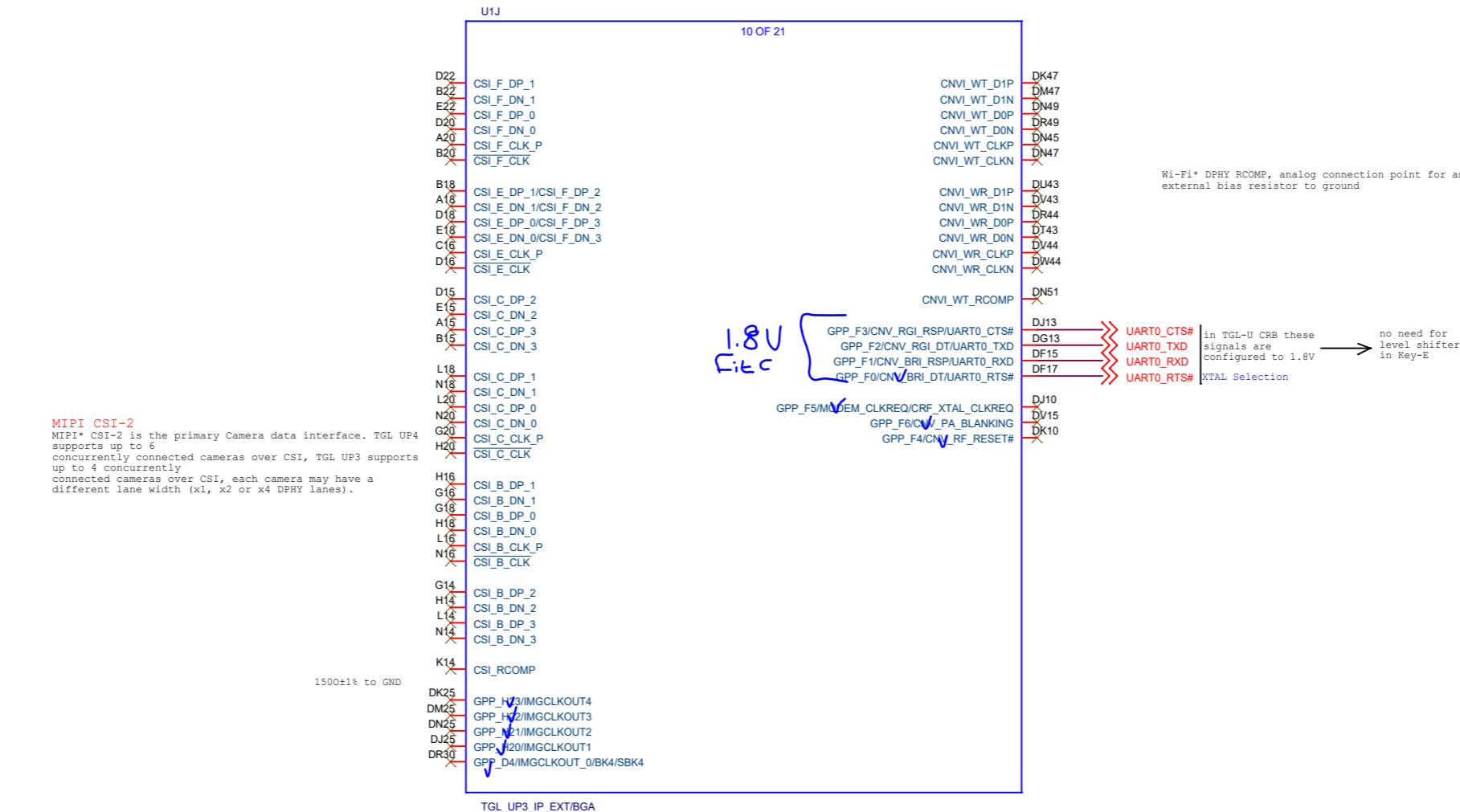


12.2 PCIe4 Gen4 Interface Signals

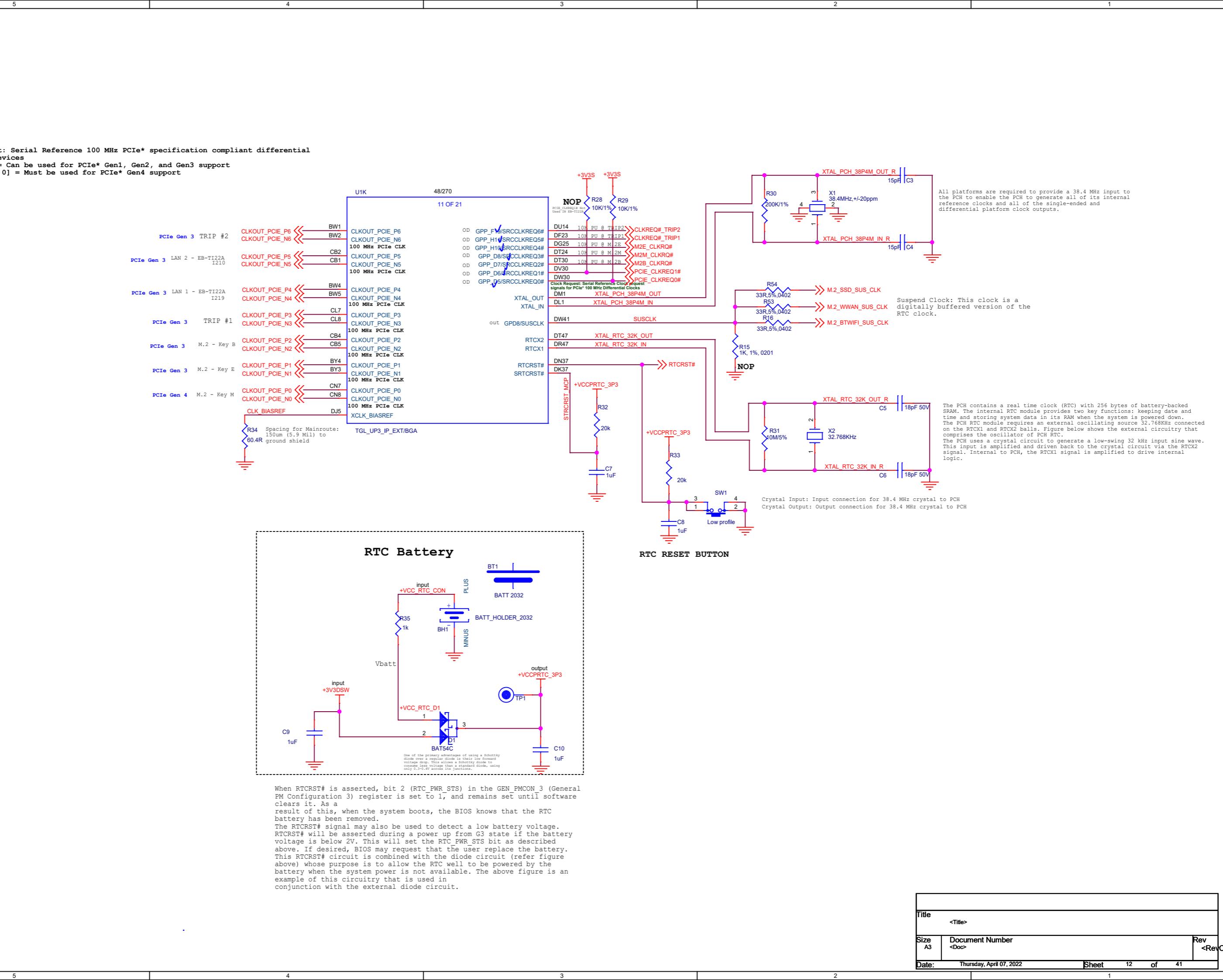
Signal Name	Description	Dir	Buffer Type	Link Type	Availability
PCIE4_RCOMP_P PCIE4_RCOMP_N	Resistance Compensation for PEG channel	I	Analog	Diff	UP3/UP4/H Processor Lines
PCIE4_TX_P[3:0] PCIE4_TX_N[3:0]	PCIe Transmit Differential Pairs	O	PCIE	Diff	UP3/UP4/H Processor Lines
PCIE4_RX_P[3:0] PCIE4_RX_N[3:0]	PCIe Receive Differential Pairs	I	PCIE	Diff	UP3/UP4/H Processor Lines

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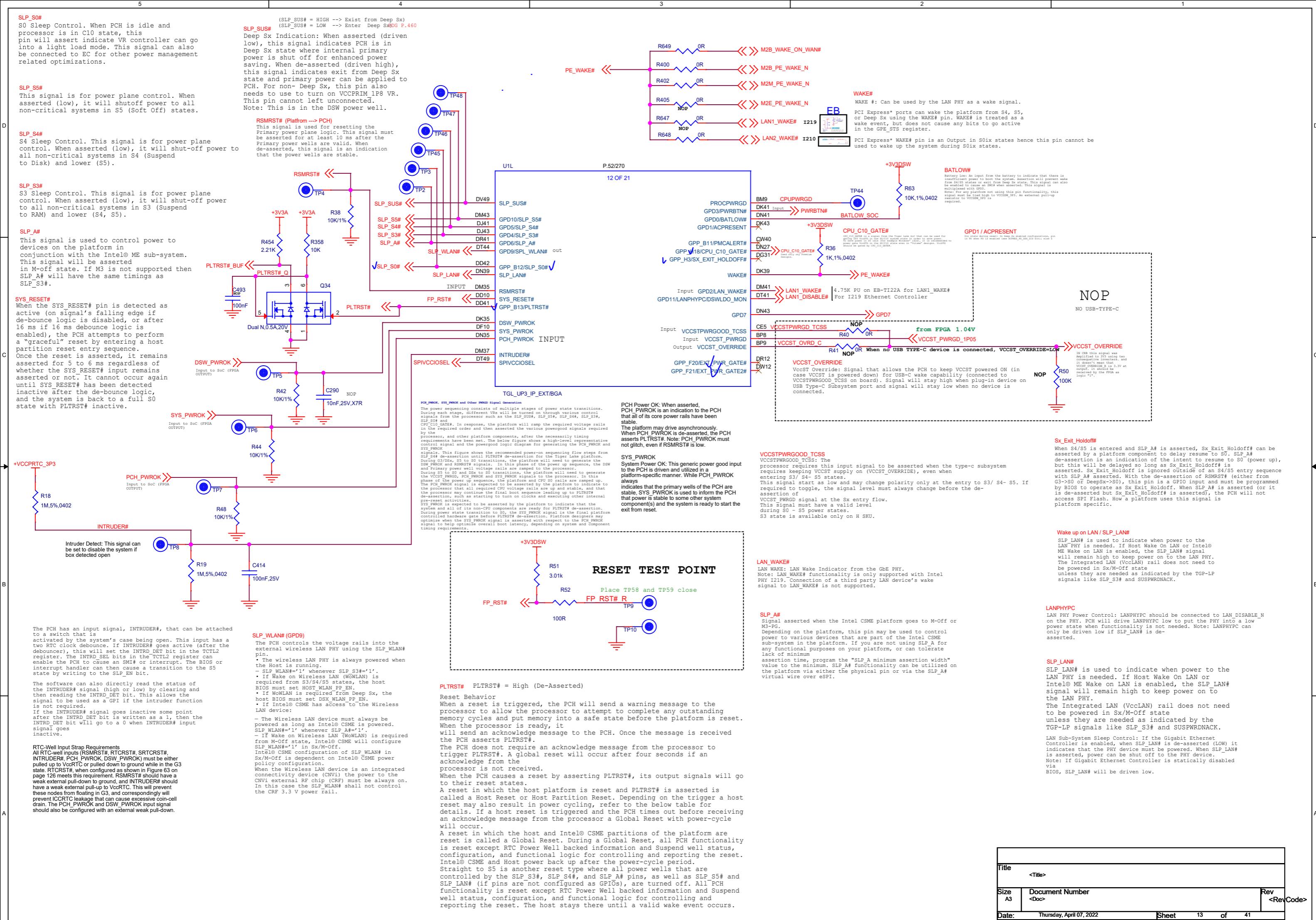


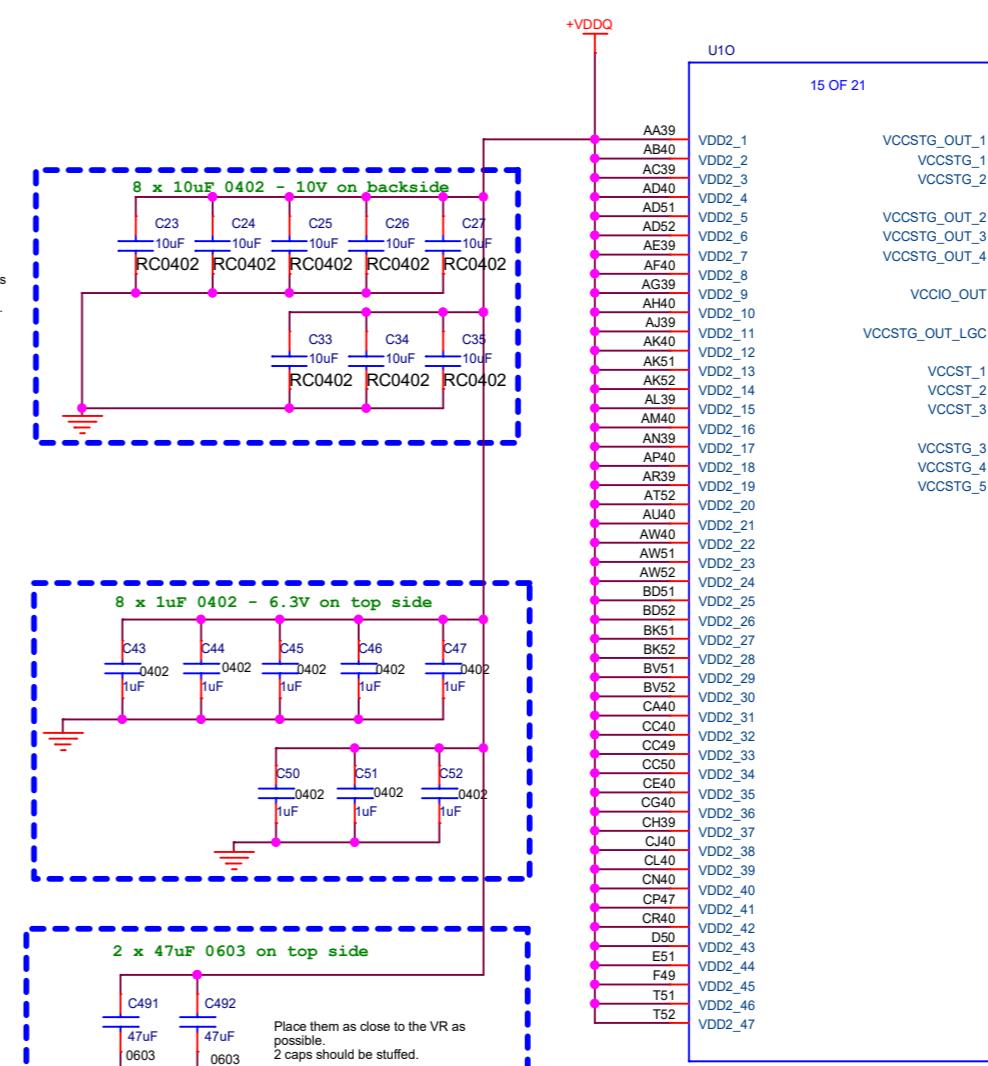
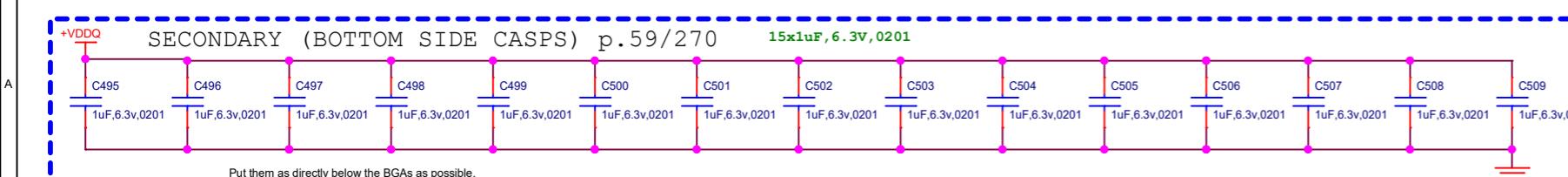
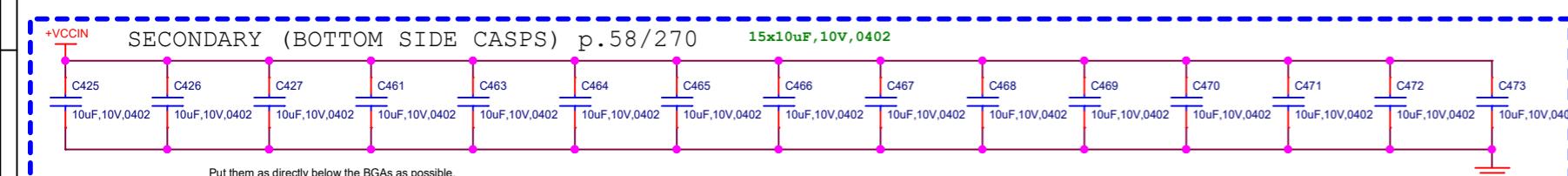
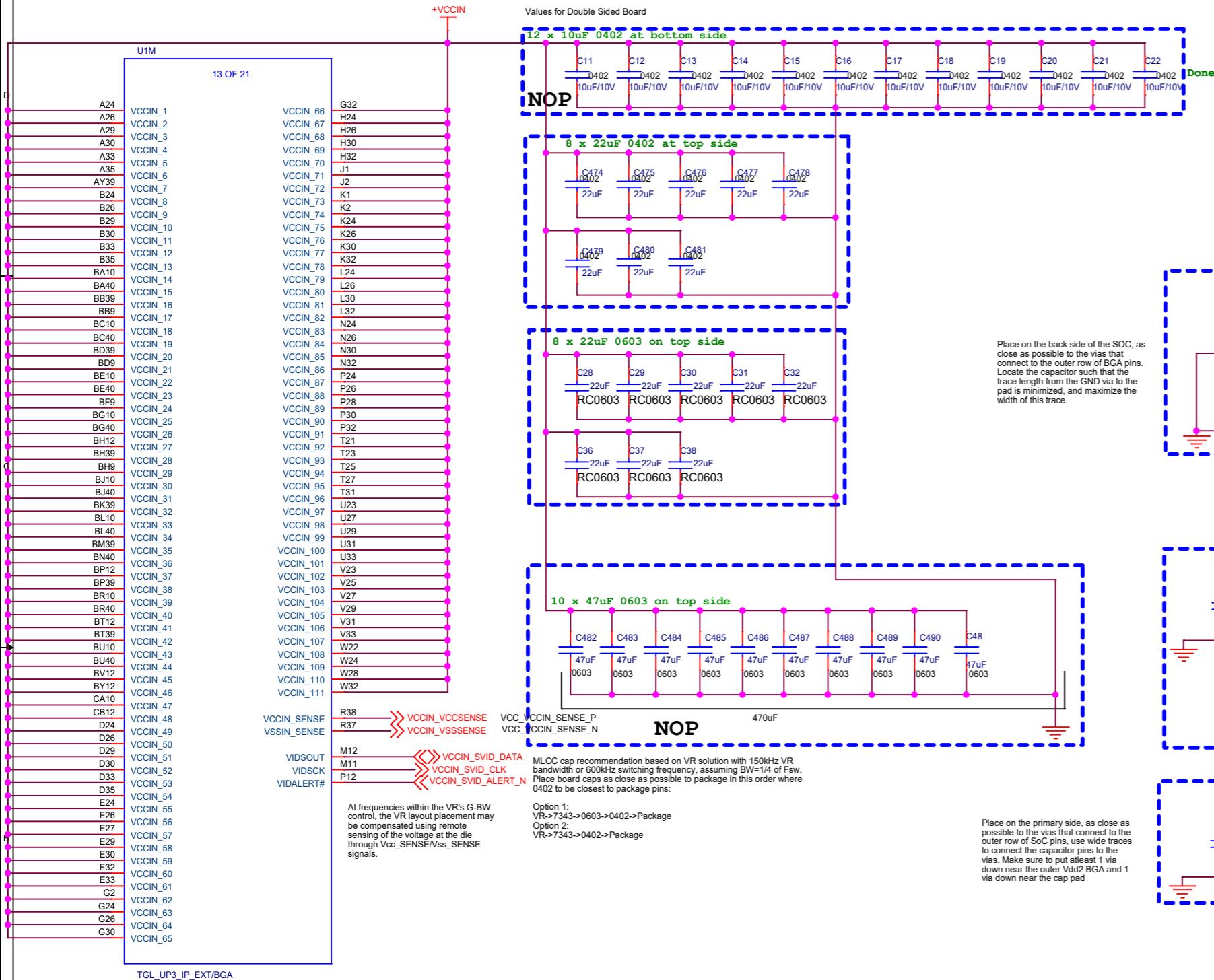


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Not connected to anything, C212 for decoupling.

+VCCSTG_OUT_1

NOP TP11

TL-EDS: p.150 (Processor Pull-up Power Rails Signals)

NOP C212

1uF,16V,X5R/X7R

+VCCIO_OUT Reference for all Digital Signals Pull-up on platform.

+VCCSTG_TERM

+VCCSTG_OUT

OUTPUT

+VCCSTG_CPU

INPUT

+VCCST_CPU

INPUT

Sustain V_{DD} for processor standby mode

VCCSTG and VCCST can be used as reference for optimization. VCCSTG is recommended for best noise immunity. Best choice for VCCST is VCCIO_OUT.

+VCCSTG_CPU

C40

1uF

C41

1uF

C42

1uF

made: +VCCST_CPU = +VCCSTG_CPU
PU is generated from OUT_FET which is generated FIVR

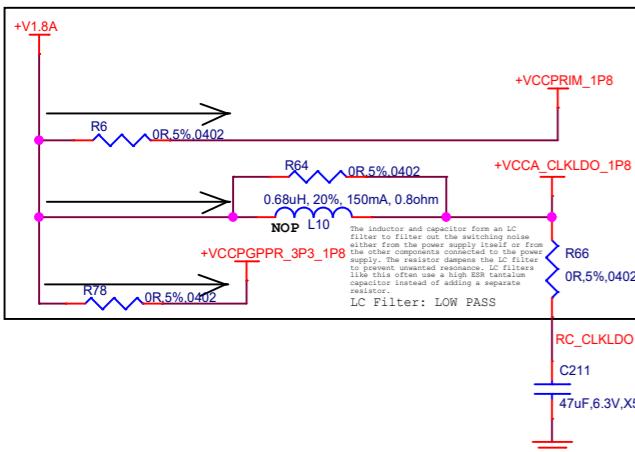
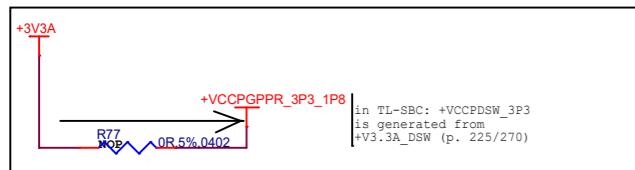
Voltages for processor standby

CLOSE AS POSSIBLE TO THE BGA
ROUTING ON THE BOARD NEED
AS MUCH AS 2 ROUTE LAYERS,
1 ON 4 LAYERS FOLLOWING
SHOWN IN BREAKOUT. PMR OF
NEED TO BE PLACED IN PARALLEL TO
E. PC RDSON NEED TO BE

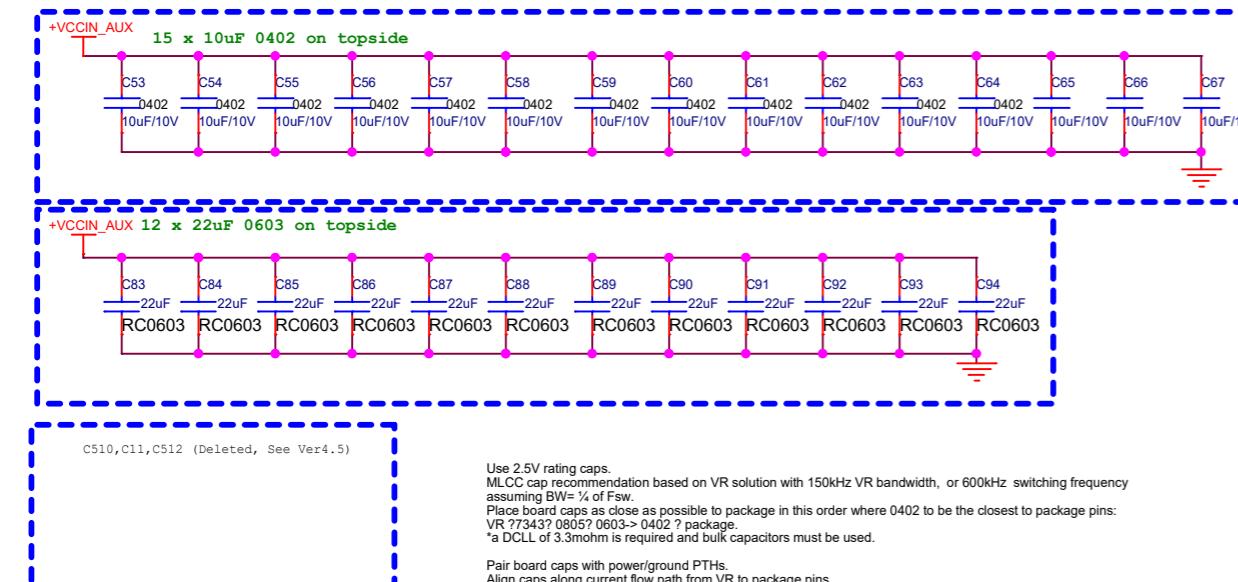
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From
External
DC\DC

to SoC

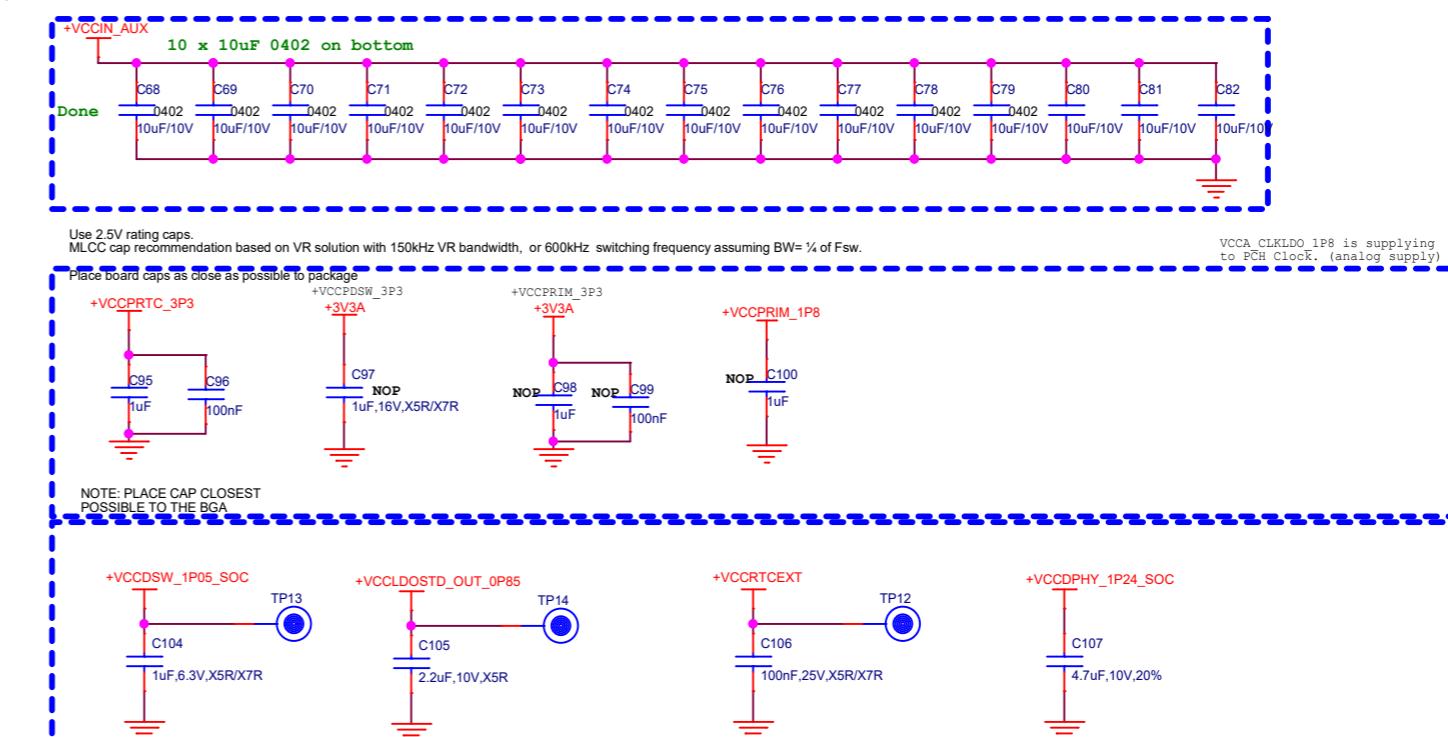
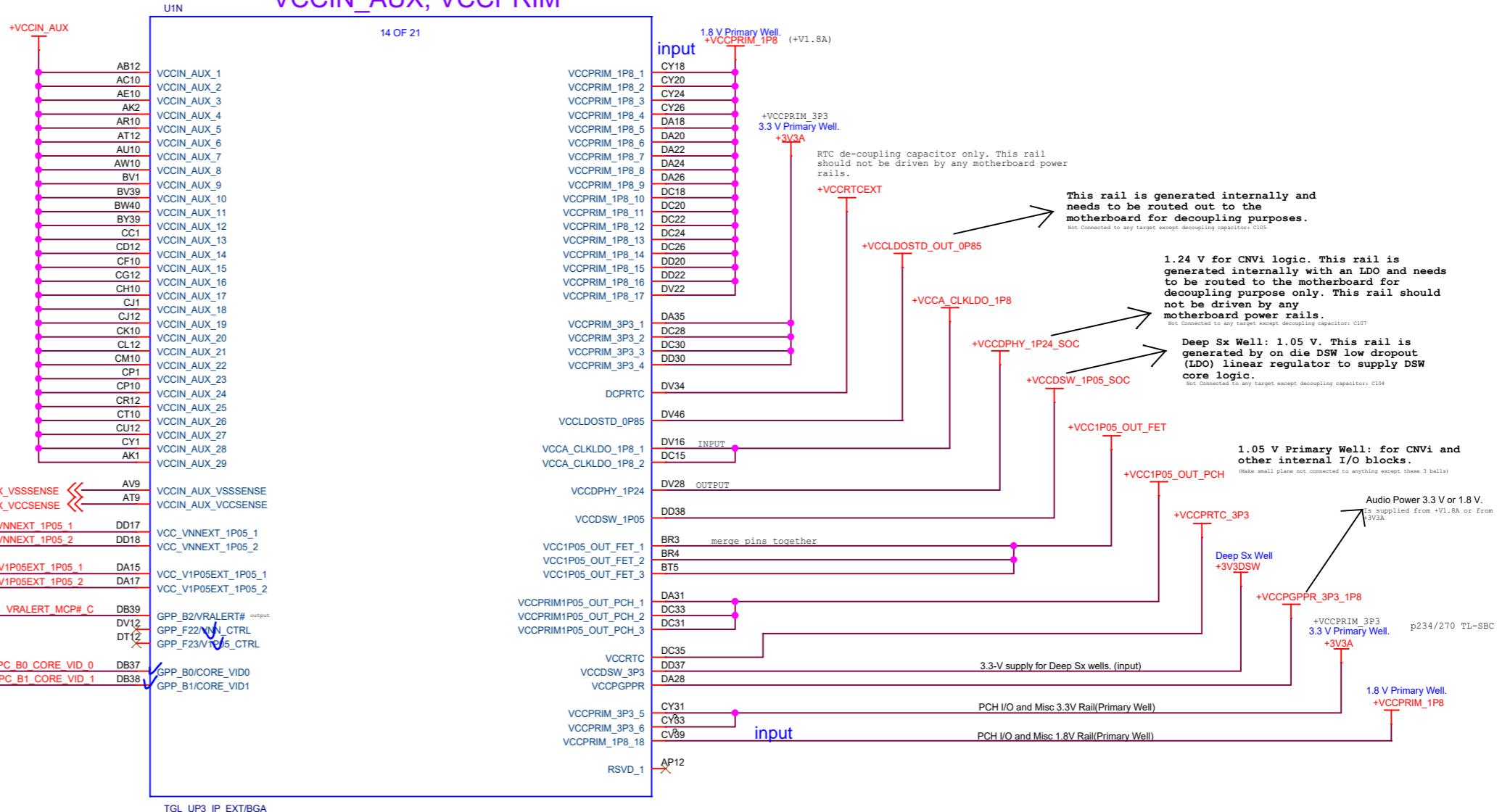


VRALERT#: ICC Max. throttling indicator from the PCH voltage regulators. VRALERT# pin allows the VR to force PCH throttling to prevent an over current shutdown. PMC based on the VRALERT# and messages from the processor. The messages from the processor allows the processor to constrain the PCH to a particular power budget.



The VCC_VNNEXT_1P05 (VNNEV_BYB) and VCC_V1P05EXT_1P05 (V1P05_BYB) are two optional dedicated voltage regulators that save platform power during low power states.

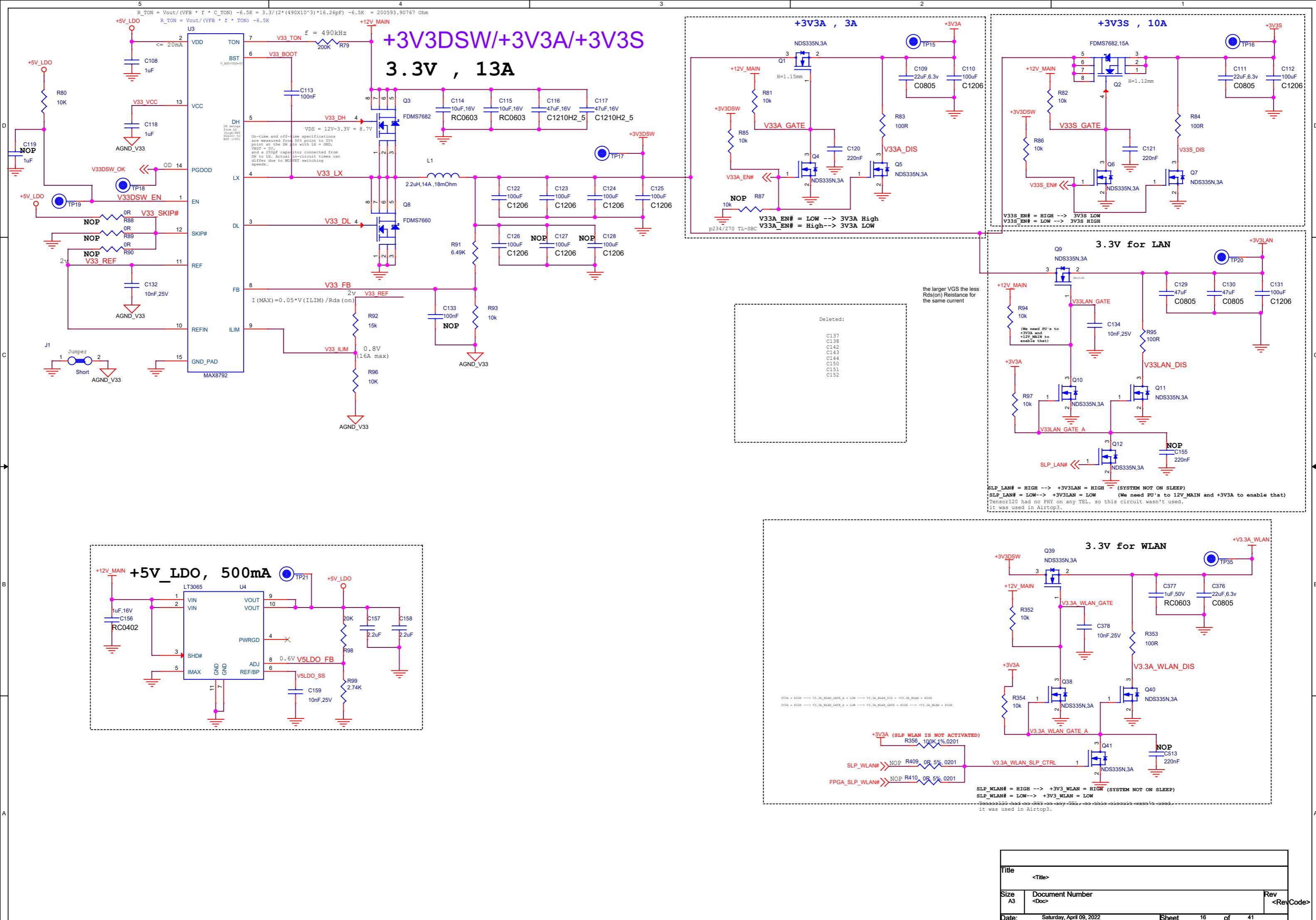
VCCIN_AUX, VCCPRIM

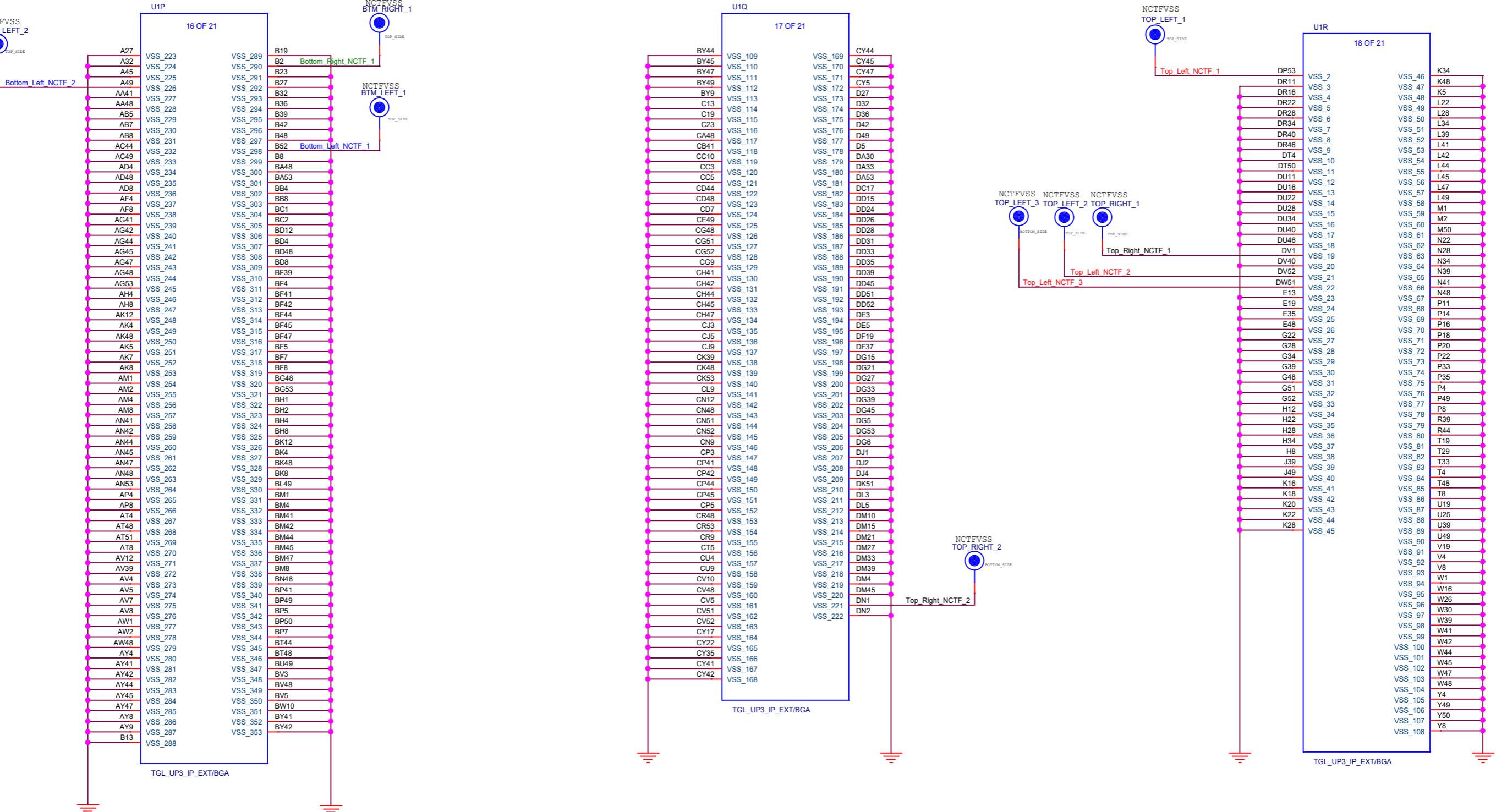


Trade-offs - Volume vs. Premium Power Maps:

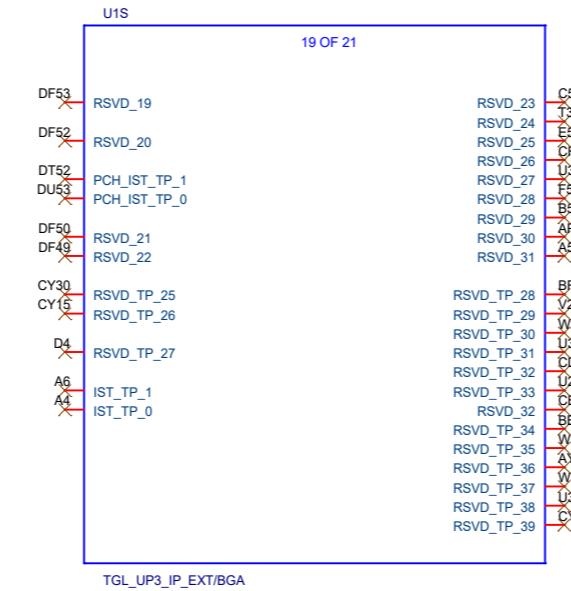
Power maps are broken into two tiers: Volume and Premium. Volume focuses on cost savings with the fewest VRs and Premium focuses on the smallest solution size with the lowest power consumption. For a design focused on S0ix or Modern Standby* power, the Premium power map is recommended. The designer may choose to implement a hybrid between Volume and Premium as long as guidelines are followed.

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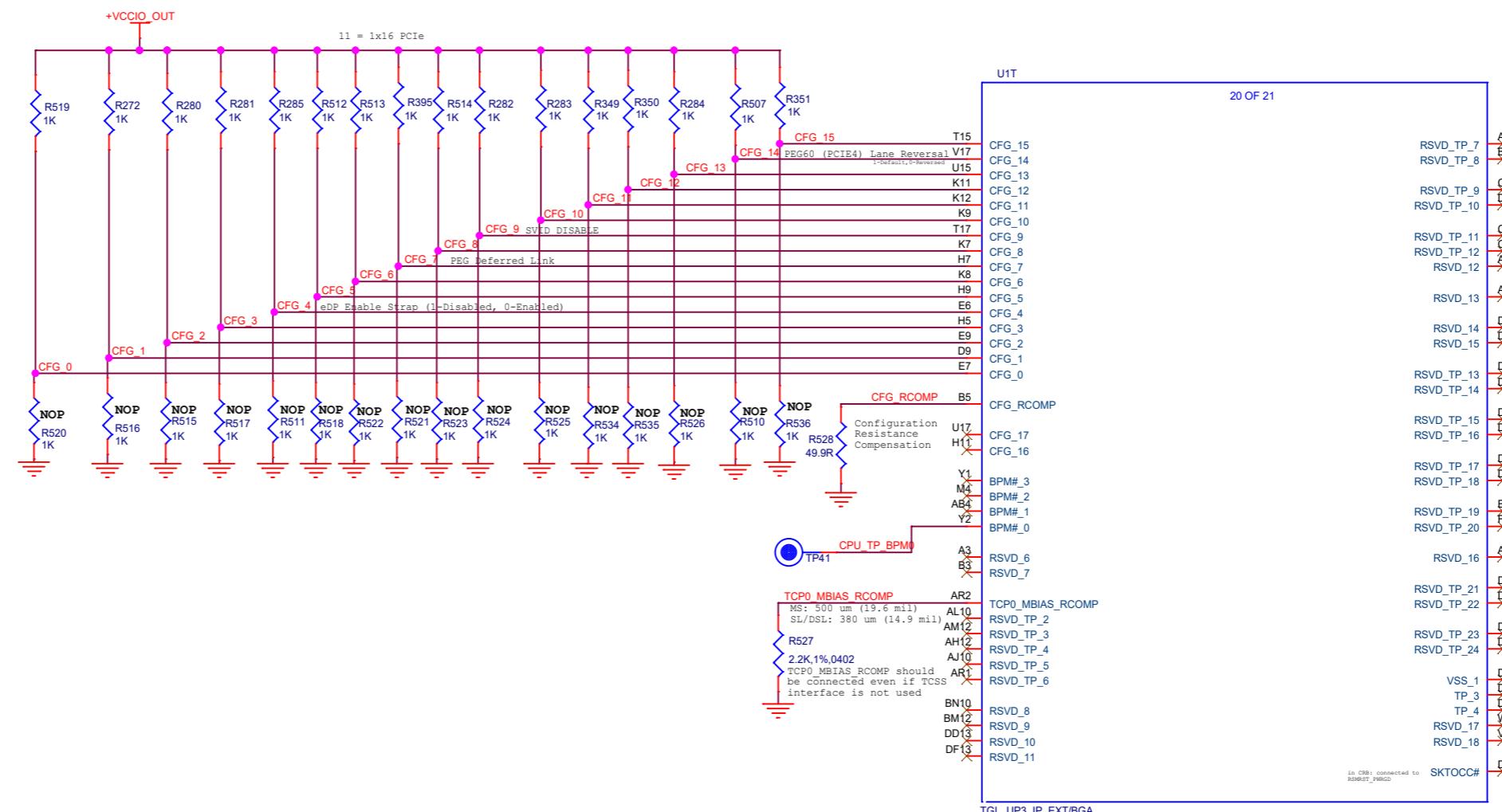
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CFG[17:0]	I GTL	SE	UP3/UP4/H Processor Lines

Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

Intel recommends placing test points on the board for CFG pins.

- **CFG[3], CFG[0]:** Reserved configuration lane.
- **CFG[2]: TGL_UP4/UP3 Reserved**
- **CFG[2]: H PCI Express* Static x16 Lanes Numbering Reversal.**
 - 1 - (Default) Normal
 - 0 - Reversed
- **CFG[4]: eDP enable:**
 - 1 = Disabled.
 - 0 = Enabled.
- **CFG[6:5]: TGL_UP4/UP3 Reserved**
- **CFG[6:5]: H PCI Express* Bifurcation**
 - 00 = 1x8, 2 x4 PCI Express*
 - 01 = reserved
 - 10 = 2 x8 PCI Express*
 - 11 = 1x16 PCI Express*
- **CFG[13:7]: Reserved configuration lanes.**
- **CFG[14]: PEG60 (PCIE4) Lane Reversal:**
 - 1 - (Default) Normal
 - 0 - Reversed
- **CFG[17:15]: Reserved configuration lanes.**



SKTOCC#:
Processor Select / Socket Connect. Pulled down directly (0 Ohms) on the processor package.
There is no connection to the processor silicon for this pin. Board designers may use this signal to determine if the processor is present.

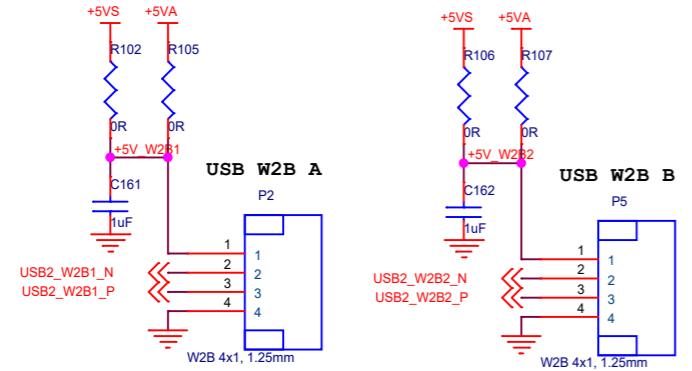
BPM#[3:0]
Breakpoint and Performance Monitor Signals: Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM#[3:0]	Pull Up/Pull Down	VCC _{IO_OUT}	16-60 Ω
PROC_PREQ#	Pull Up	VCC _{STG}	3 kΩ
PROC_TDI	Pull Up	VCC _{STG}	3 kΩ
PROC_TMS	Pull Up	VCC _{STG}	3 kΩ
PROC_TRST#	Pull Down	VCC _{STG}	3 kΩ
PROC_TCK	Pull Down	VCC _{STG}	3 kΩ
CFG[17:0]	Pull Up	VCC _{IO_OUT}	3 kΩ

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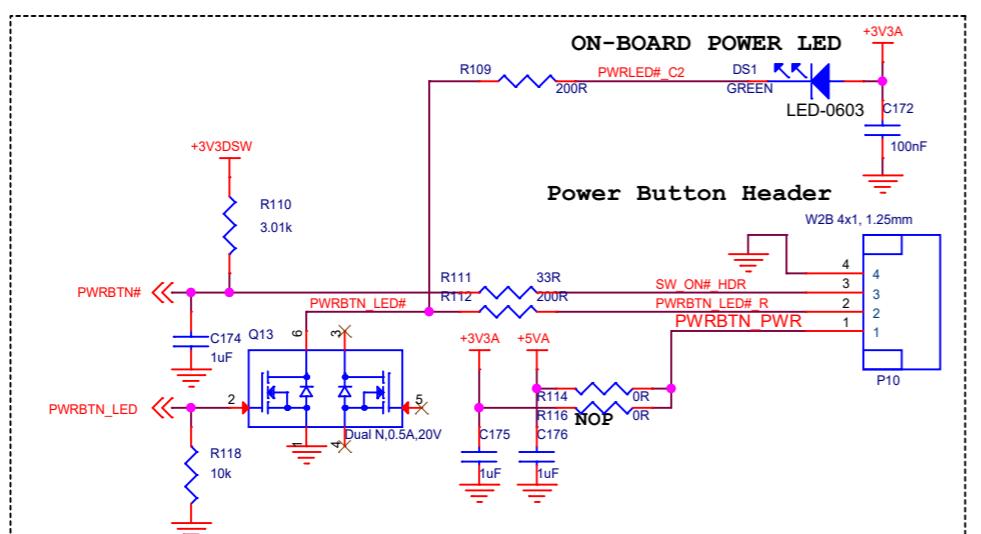
Headers



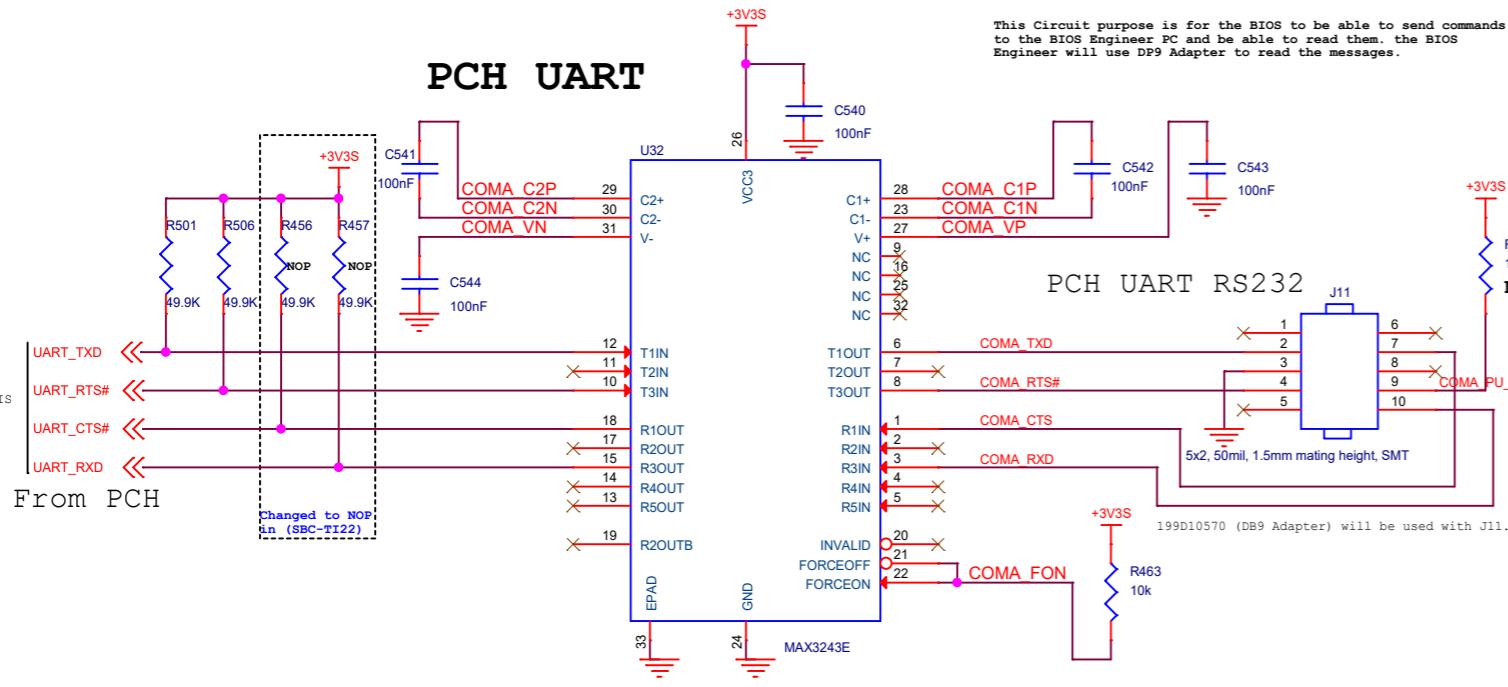
audio

Extension headers

Note: The Intel® Ethernet Connection I219 can be connected to one of the following PCI Express* ports 7, 8 or, 9

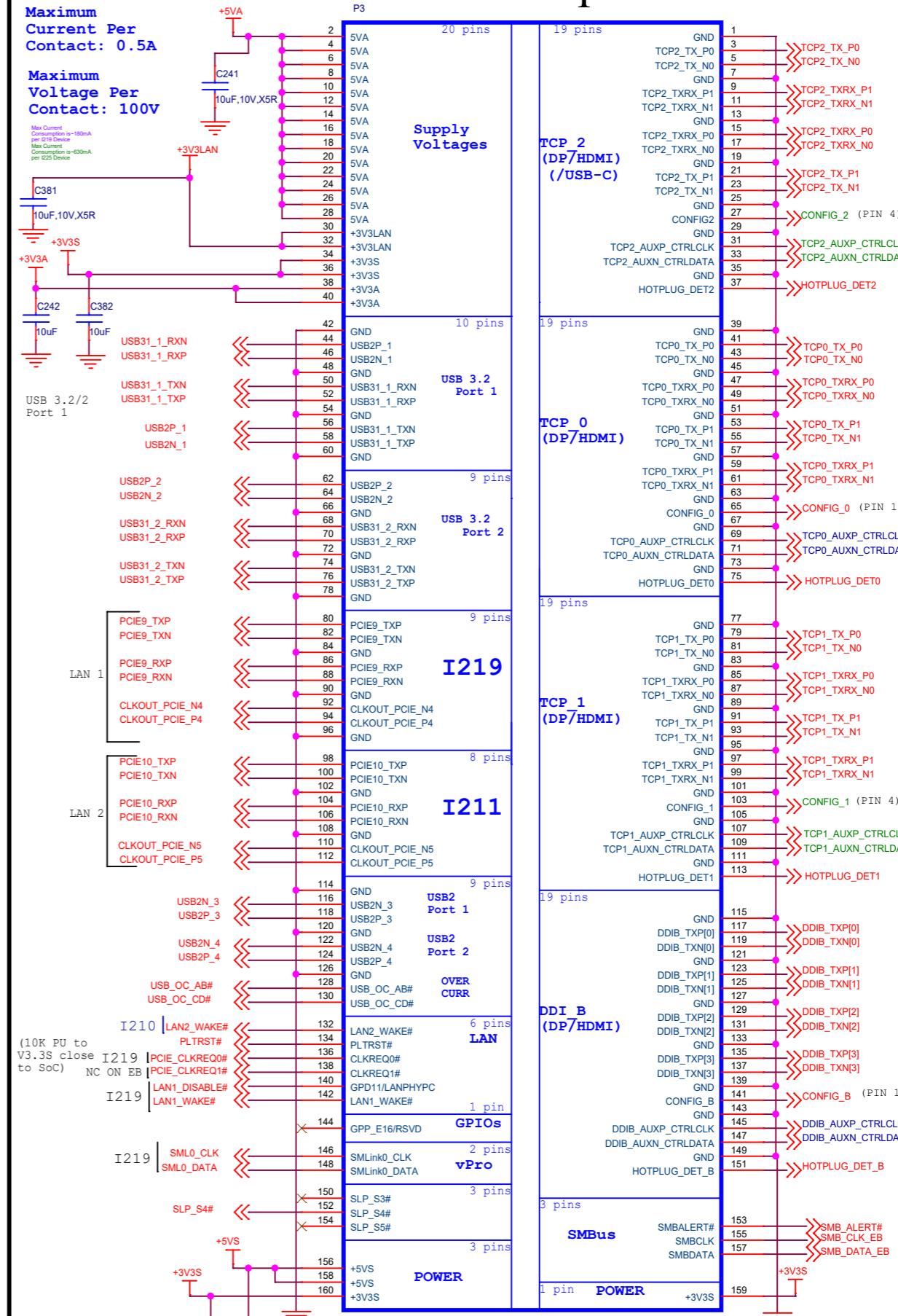


PCH UART



182K16001S

B2B Receptacle



see
TL-PDG p
104/506
table 49:
DDI port
signal
mapping to
the HDMI
connector.

mini DP ++ 2

HDMI PORT 2

for this Face Module, this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in FB-TI22A Connector.

mini DP++ 1

see TL-PDG
103/506 tab
48: DDI: TC
Port Signal
Mapping for
HDMI
connector.

for this Face Module. this port is for DP so the option CTRLDATA and CTRLCLK has been deleted from the signals names in EB-TI22A Connector because they

HDMI PORT 1

for this Face Module. this port is for HDMI, so the option AUXP and AUXN has been deleted from the signals names in

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12.6.3 Digital Display Interface (DDI) Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDIA_TXP[3:0] DDIA_TXN[3:0] DDIB_TXP[3:0] TX DDIB_TXN[3:0]	Digital Display Interface Transmit: DisplayPort and HDMI Differential Pairs	O	DP*/HDMI	Diff	All Processor Lines.
DDIA_AUX_P DDIA_AUX_N DDIB_AUX_P AUX DDIB_AUX_N	Digital Display Interface Display Port Auxiliary: Half-duplex, bidirectional channel consist of one differential pair for each channel.	I/O	DP*	Diff	

p.103/507 TL-TDG

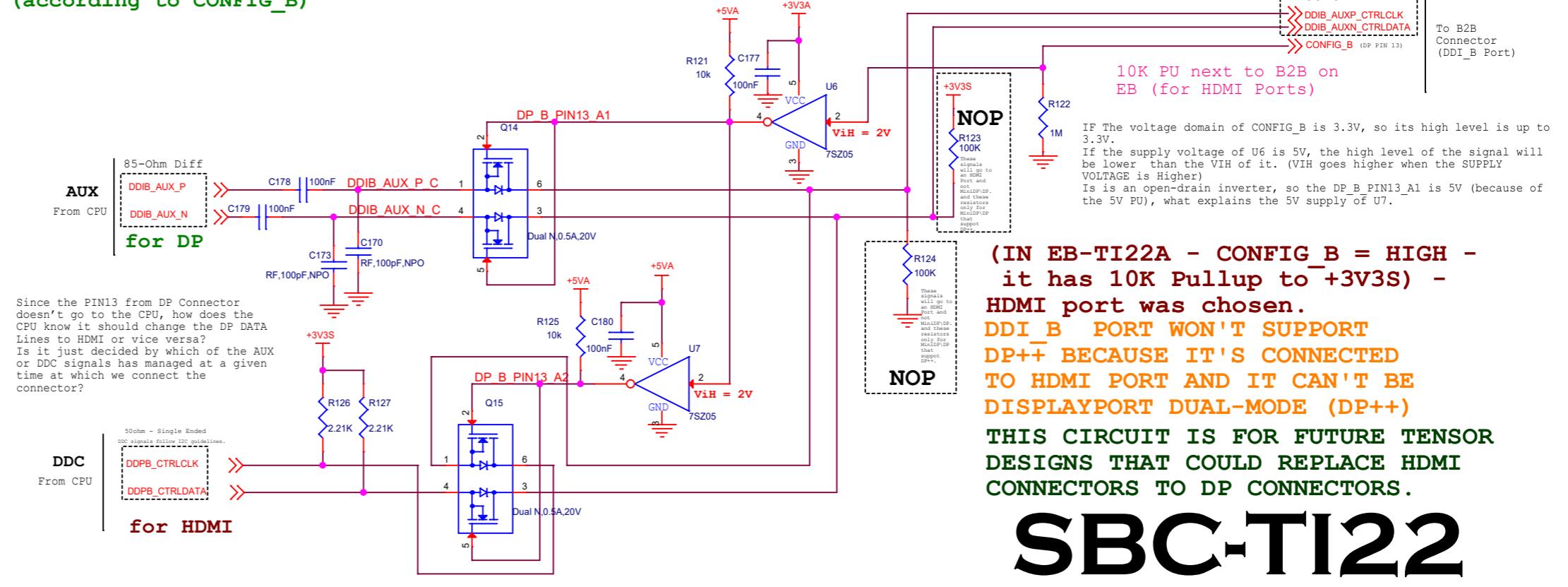
Table 38. DisplayPort® Signals

Description	Signal Mapping			Note
	Tiger Lake Processor	Tiger Lake PCH	CRB DisplayPort* Mapping	
Main Link (Tx) TX	DDIX_TXP[N[3:0]]	N/A	N/A	1
	TCPx_TX_P/N[1:0] and TCPx_TXRX_P/N[1:0]	N/A	N/A	2
 Aux Channel AUX	DDIX_AUXP/N	N/A	N/A	1
	TCPx_AUX_P/N	N/A	N/A	2
Hot Plug Detect	N/A	DDSP_HPD_X	N/A	
DISP_UTILS	Recommend 50 ohm nominal trace impedance. Requires level shifting on the platform.			
DDIA_RCOMP	150 ohm +/-1% pull-down to VSS			3
TC_RCOMP	150 ohm +/-1% connected between TC_RCOMP_P and TC_RCOMP_N			4

Note:

1. Signals names apply for DDI A/B ports.
2. Signals names apply for TCP ports.
3. Provide good noise isolation, Platform $Rdc < 0.2$ Ohm, require if any DDI implemented.
4. Provide good noise isolation, Platform $Rdr < 0.2$ Ohm, require if any TCP implemented.

**DP(AUXP, AUXN) or HDMI(CTRLCLK, CTRLDATA) select for DDI_B
(according to CONFIG_B)**



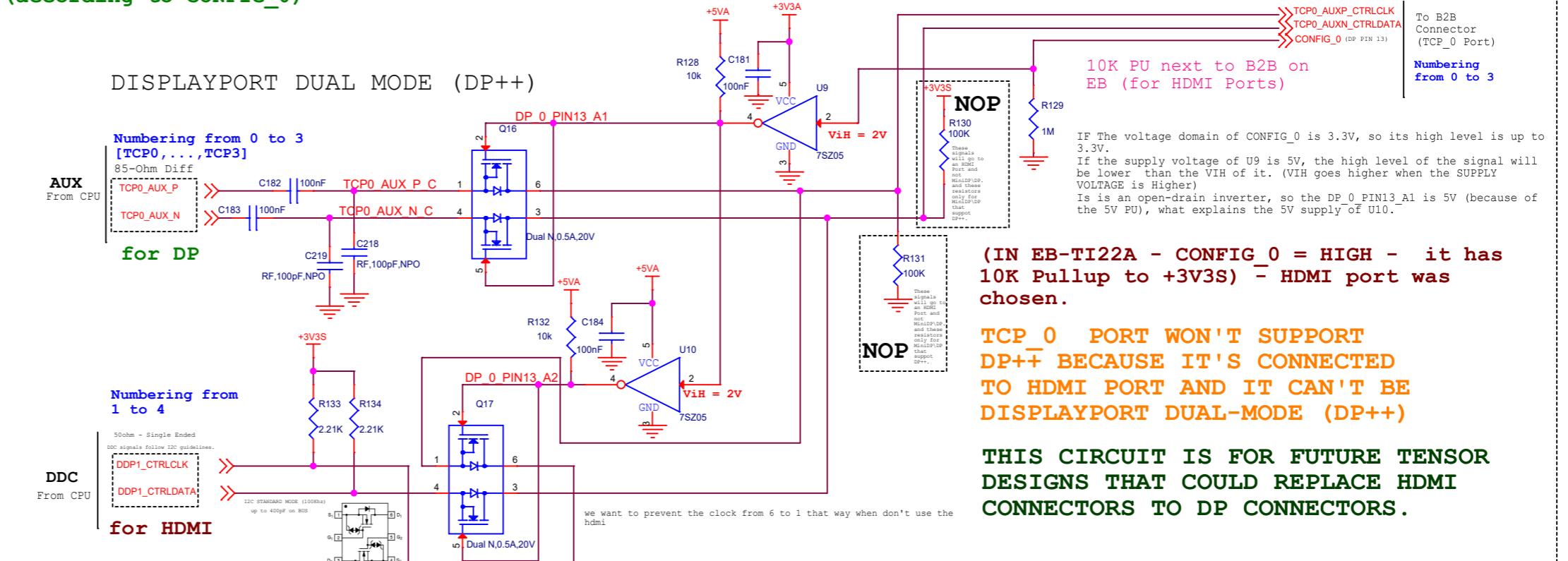
(IN EB-TI22A - CONFIG_B = HIGH -
it has 10K Pullup to +3V3S) -
HDMI port was chosen

DDI_B PORT WON'T SUPPORT DP++ BECAUSE IT'S CONNECTED TO HDMI PORT AND IT CAN'T BE DISPLAYPORT DUAL-MODE (DP++)

THIS CIRCUIT IS FOR FUTURE TENSOR DESIGNS THAT COULD REPLACE HDMI CONNECTORS TO DP CONNECTORS.

SBC-TI22

**DP (AUXP, AUXN) or HDMI (CTRLCLK, CTRLDATA) select for TCP0
(according to CONFIG_0)**

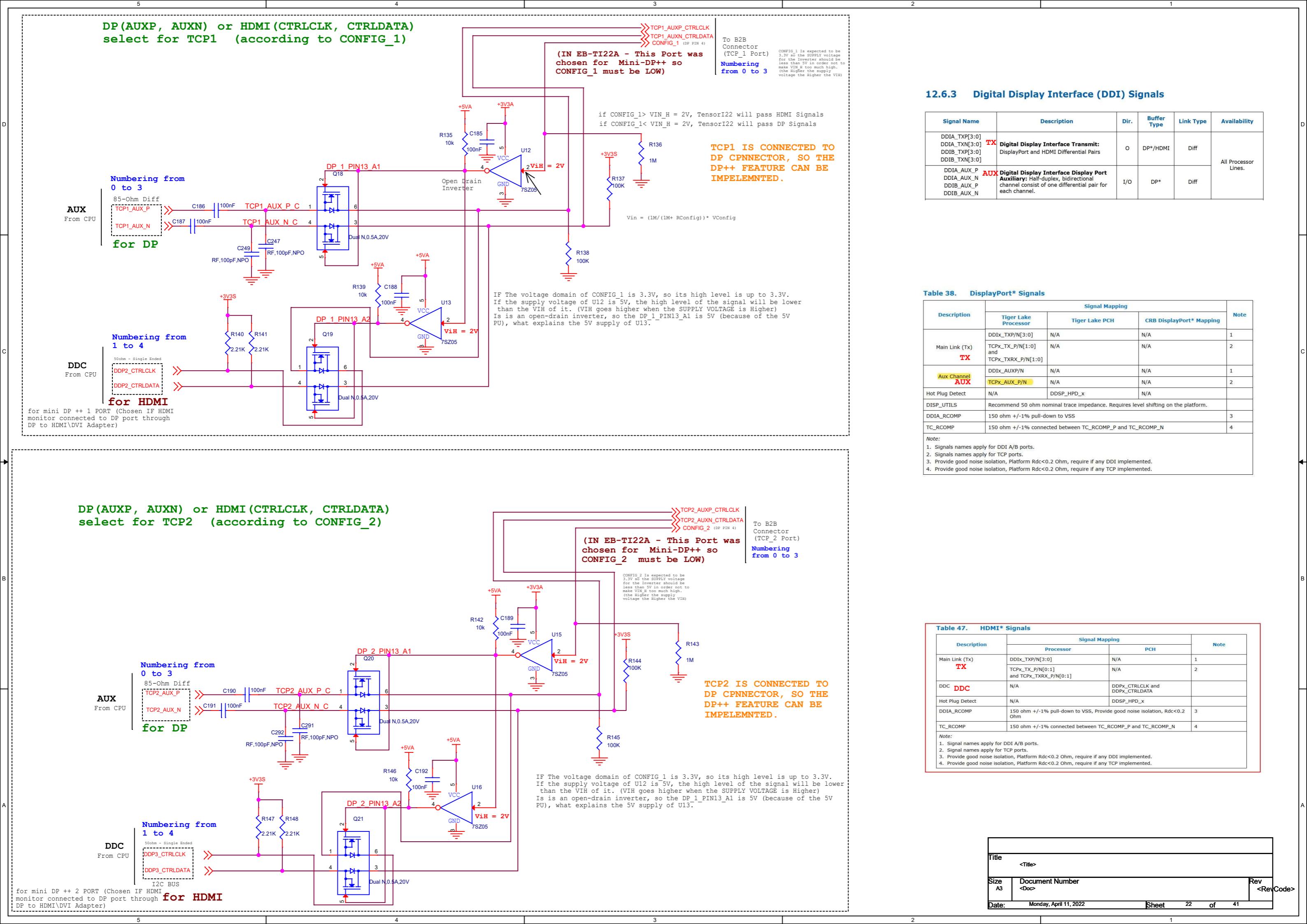


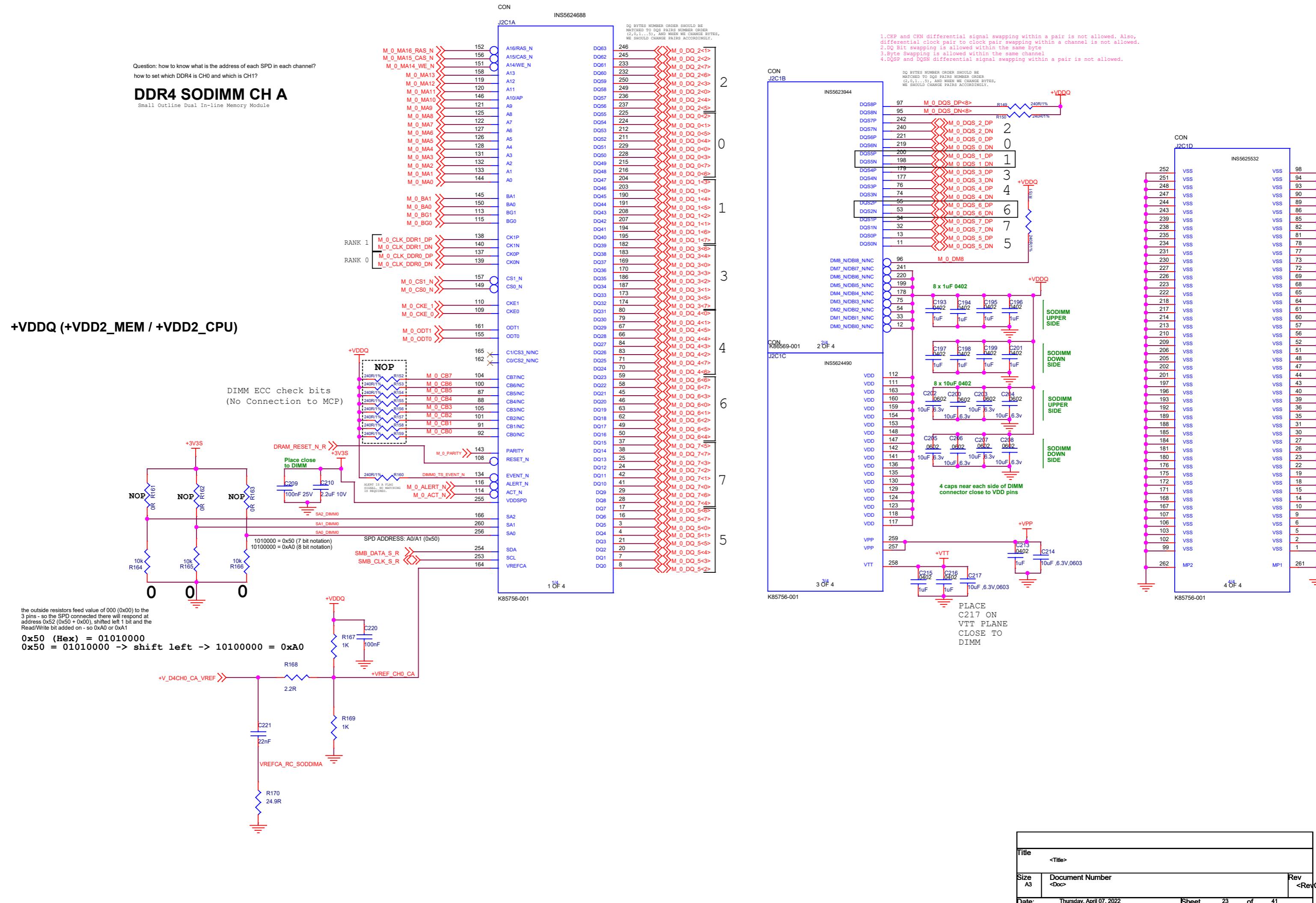
 IF The voltage domain of CONFIG_0 is 3.3V, so its high level is up to 3.3V.
 If the supply voltage of U9 is 5V, the high level of the signal will be lower than the VIH of it. (VIH goes higher when the SUPPLY VOLTAGE is Higher)
 Is it an open-drain inverter, so the DP_0 PIN13_A1 is 5V (because of $V_{DD} = 5V$, $V_{DD} > V_{IH}$, so $V_{DD} > V_{IH}$)

IN EB-TI22A - CONFIG_0 = HIGH - it has
0K Pullup to +3V3S) - HDMI port was
chosen.

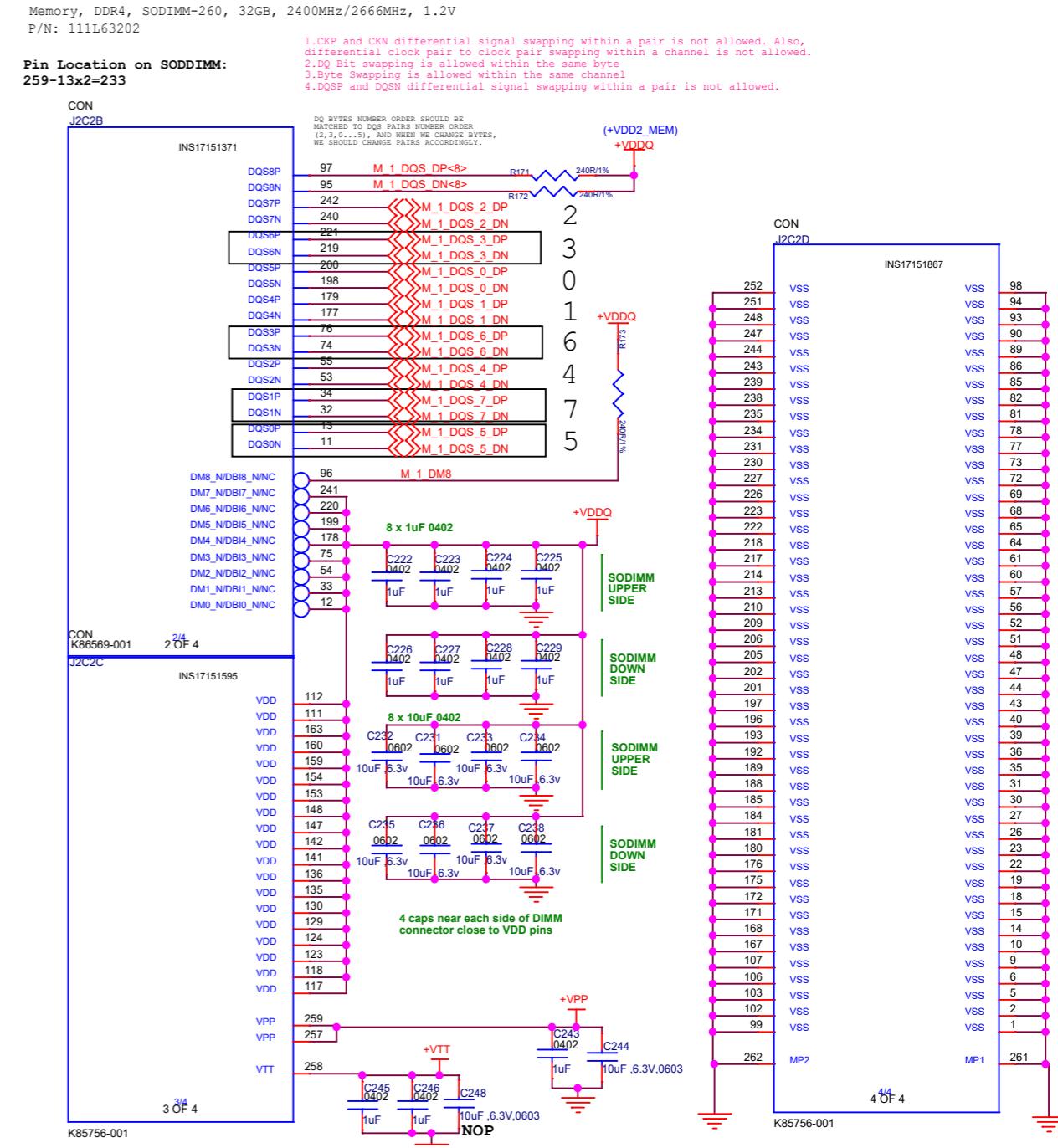
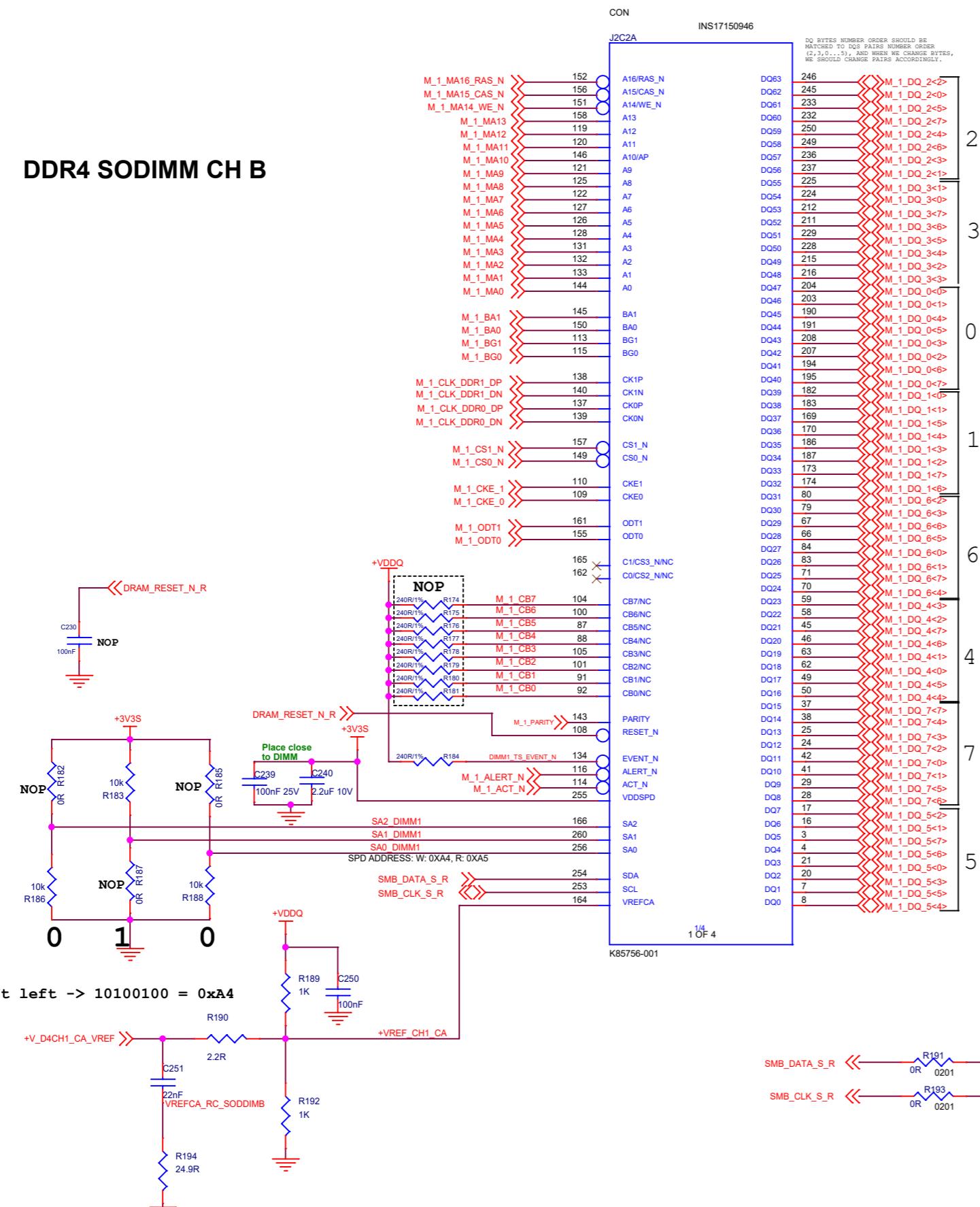
PC_0 PORT WON'T SUPPORT DP++ BECAUSE IT'S CONNECTED TO HDMI PORT AND IT CAN'T BE DISPLAYPORT DUAL-MODE (DP++)

THIS CIRCUIT IS FOR FUTURE TENSOR DESIGNS THAT COULD REPLACE HDMI CONNECTORS TO DP CONNECTORS.





DDR4 SODIMM CH B

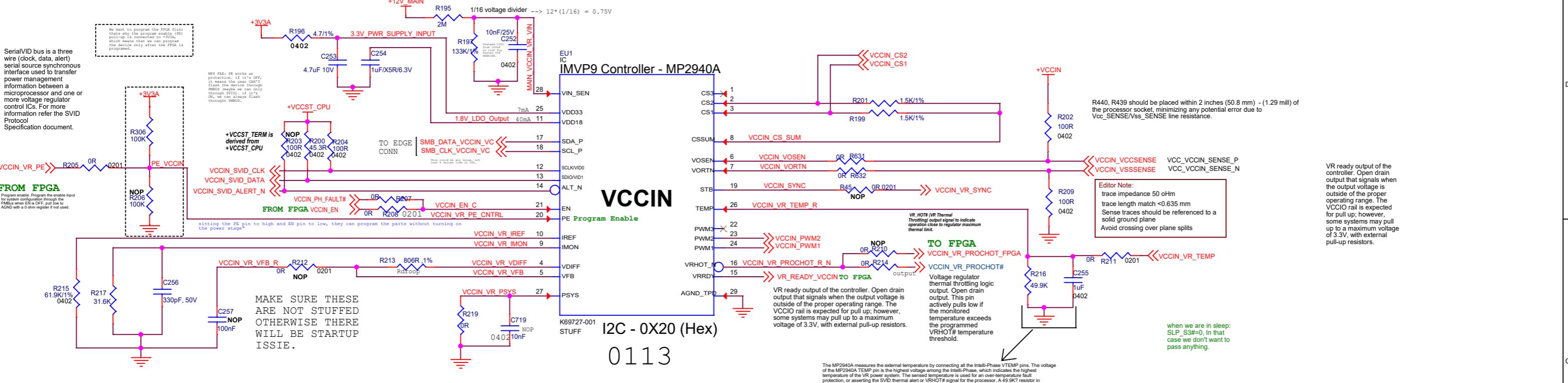


Change +V_VTT_MEM to +VTT
Change +VPP_2P5U_MEM to +V

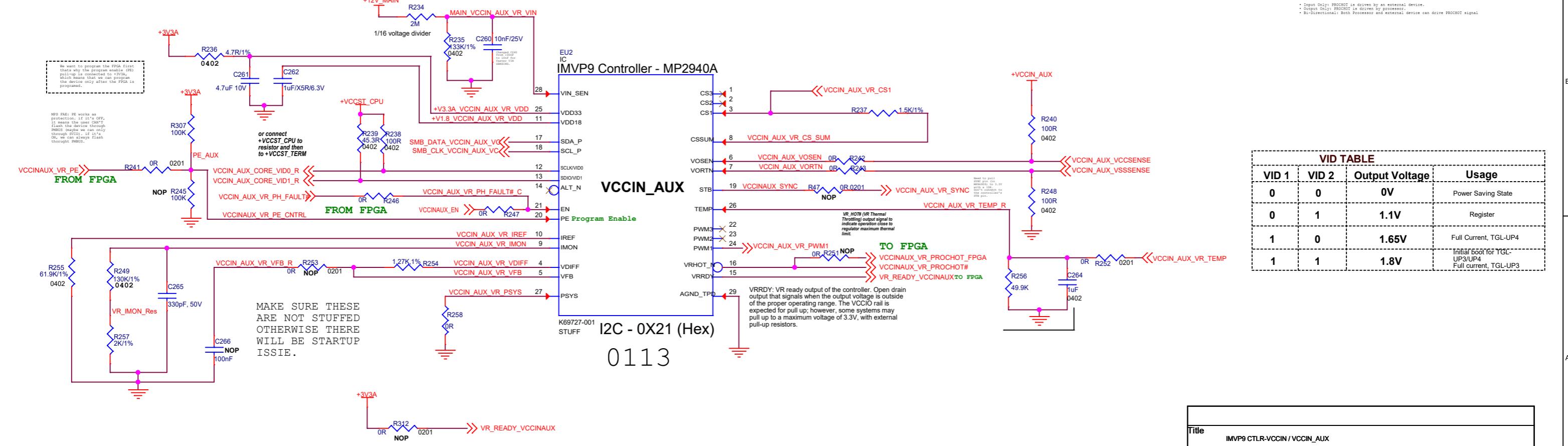
place as
close as
possible to
DRAM

Title	
<Title>	
Size A3	Document Number <Doc>
	Rev <Rev>
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VCCIN RAIL POWER CONVERSION

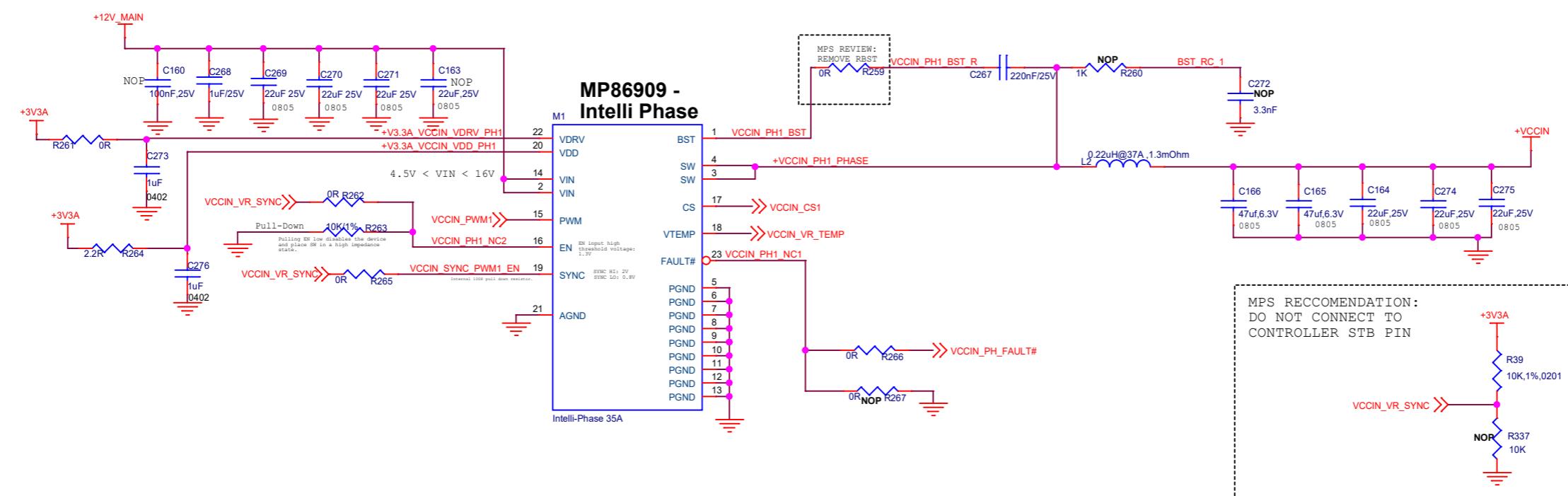


VCCIN AUX RAIL POWER CONVERSION

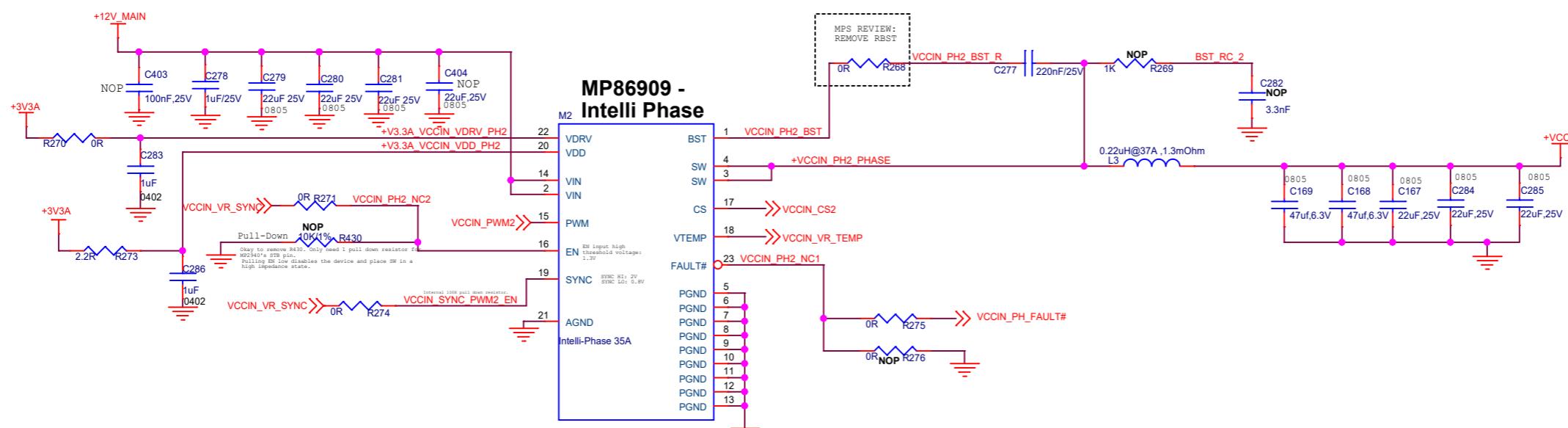


VID TABLE			
VID 1	VID 2	Output Voltage	Usage
0	0	0V	Power Saving State
0	1	1.1V	Register
1	0	1.65V	Full Current, TGL-UP4
1	1	1.8V	Tmax 660mV TGL-UP4 Current Limit TGL-UP3

Title		
IMVP9 CTLR-VCCIN / VCCIN_AUX		
Size A3	Document Number <Doc>	Rev <Rev>Co
Date:	Sunday, April 10, 2022	Sheet 25 of 41



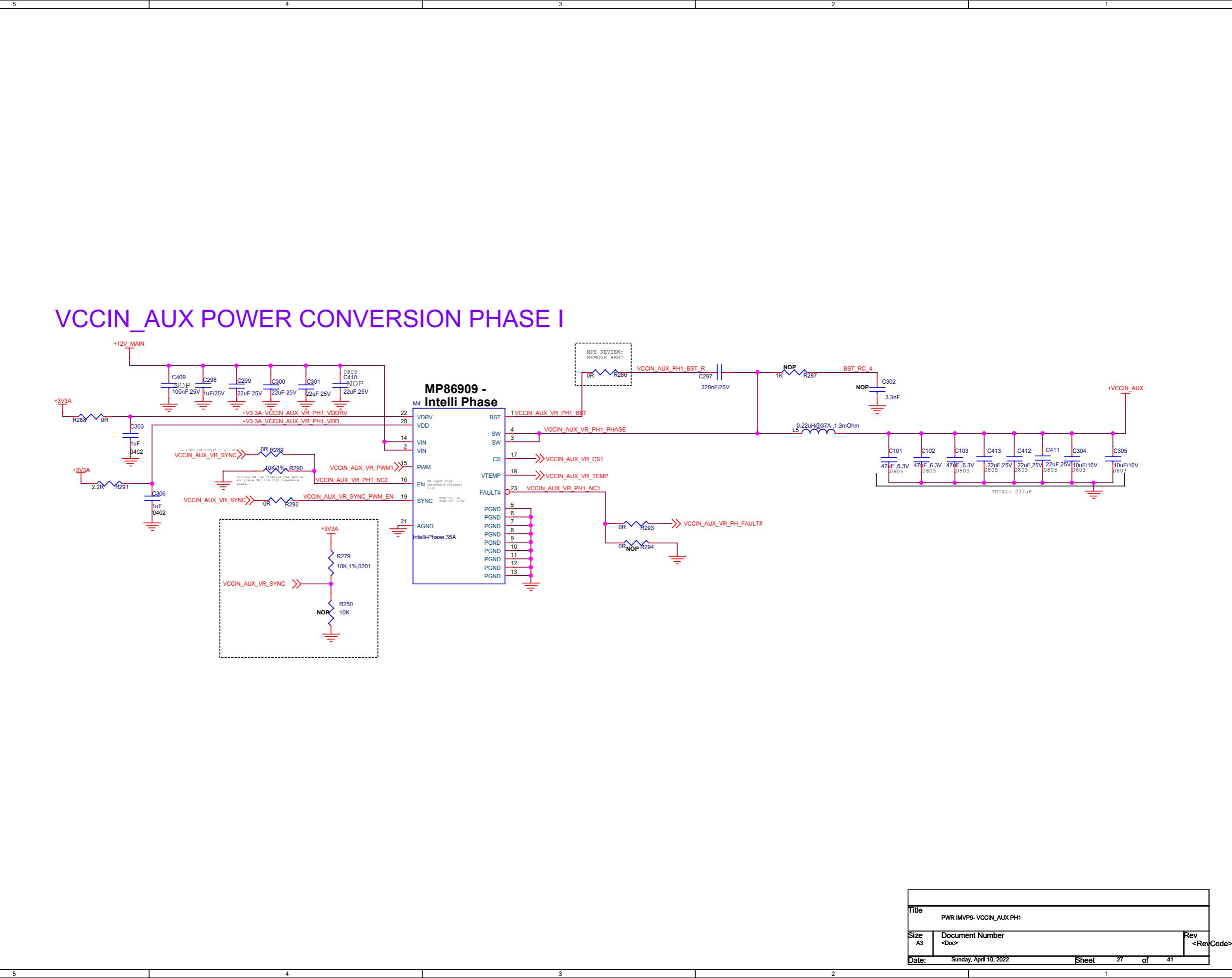
VCCIN POWER CONVERSION PHASE I

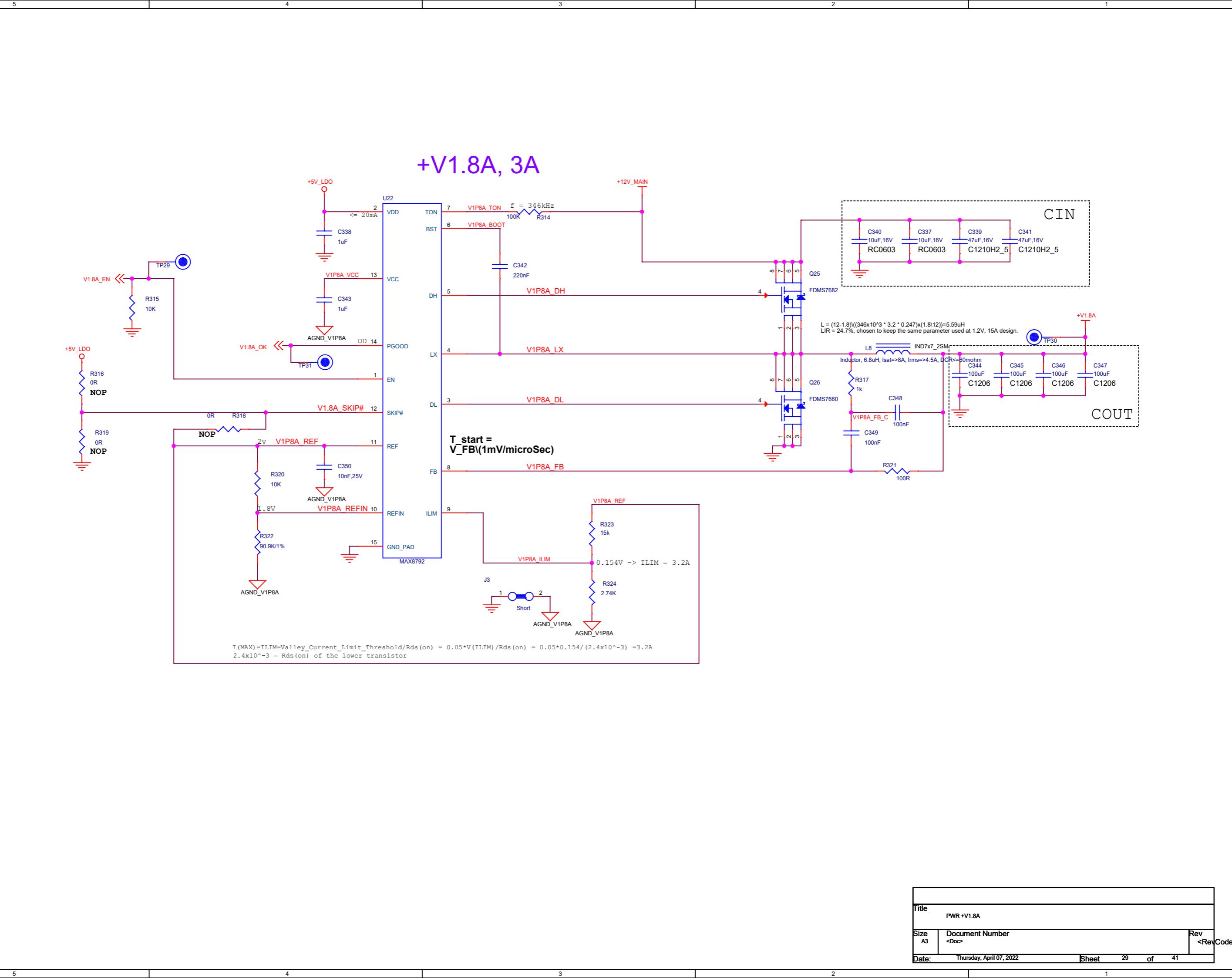


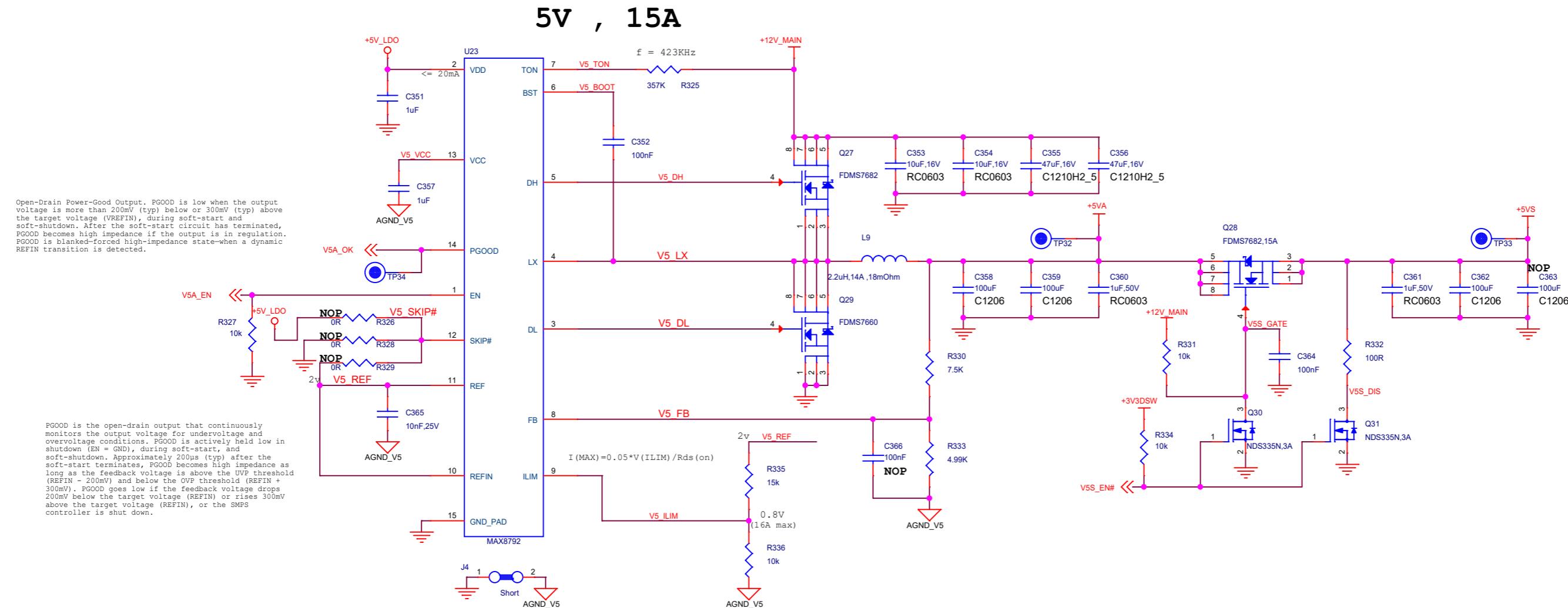
VCCIN POWER CONVERSION PHASE II

Title	
PWR IMVP9- VCCIN PH1/PH2/PH3	
Size	Document Number
A3	<Doc>

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+5VA Plane stitching capacitors

C135-C154 (see in Ver4.5)

Title	
PWR 5V	
Size	
A3	Document Number
	<Doc>
Rev	<Rev>
	Code
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PCH STRAPS

TOP SWAP OVERRIDE

GPP_B14

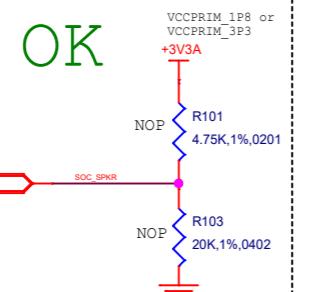
The strap has a 20 kohm ± 30% internal pull-down.

0=>Disable "Top Swap" mode. (Default)
1=>Enable "Top Swap" mode.

This inverts an address on access to SPI, so the processor fetches the alternate boot block instead of the original boot-block. PCH will invert the appropriate address lines (A[23:16]) as selected in Top Swap Block size soft strap.

1. The internal pull-down is disabled after PCH_PWROK is high.
2. Software will not be able to clear the Top Swap (TS) bit (Bus0, Device31, Function0, offset DCh, bit 4) until the system is rebooted.
3. The status of this strap is readable using the Top Swap bit.
4. This signal is in the primary well.

Sampled at Rising edge of PCH_PWROK



OK

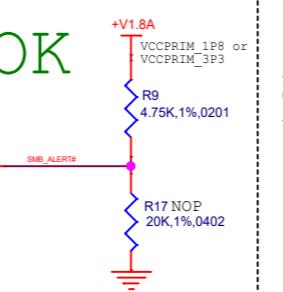
TLS CONFIDENTIALITY

GPP_C5 / SMB_ALERT#

ME TLS Confidentiality Strap (PU)
This strap has a 20 kohm ± 30% internal pull-down.
0=>Disable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1=>Enable Intel® CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

Native F1 if Intel SMBus ASD Mode Configuration soft strap = 1, else GP-Out; Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.



OK

NO REBOOT

GPP_B18 / GPIO10_MOSI

The strap has a 20 kohm ± 30% internal pull-down.
0=>Disable "No Reboot" mode. (Default)
1=>Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

- Notes:
1. The internal pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

HIGH - NO REBOOT
LOW - REBOOT ENABLED
WEAK INTERNAL PD 20K

Sampled at Rising edge of PCH_PWROK

OK

STRAP FOR SPI 1.8V/3.3V SELECTION (NOT A GPIO)

(GPP_B18 / GPIO10_MOSI)

There is no internal pull-up or pull-down on the strap. An external resistor is required.
1 = SPI voltage is 3.3 V (4.7 kohm pull-down to GND)
0 = SPI voltage is 1.8 V (4.7 kohm pull-up to VCCDSW_3P3)



OK

Not sampled. This strap must always be driven to a valid logic level

DDP3 I2C / TBT_LSX2 pins VCC configuration

GPP_D10 / ISH_SPI_CLK / DDP3_CTRLDATA / TBT_LSX2_RXD / BSSB_LS2_TX / GSPI2_CLK

OK

VCCPRIM_1P8 or VCCPRIM_3P3

Already Has 100K PU (R144) to 3V3S at the DP++ HANDLING (Page 22)

This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 1.8 V
1 = DDP3 I2C / TBT_LSX2 / BSSB_LS2 pins at 3.3 V

Strap read at rising edge of RSMRST#. External pull-up is required if signal used as HDMI Display I2C. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts

Sampled at Rising edge of RSMRST#

JTAG ODT DISABLE - GPP_E6

GPP_E6 / THCO_SPI1_RST#

OK

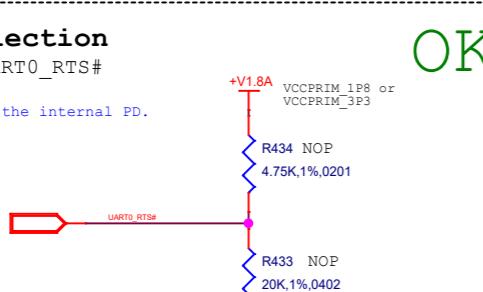
+3V3A

VCCPRIM_1P8 or VCCPRIM_3P3

This strap does not have an internal pull-up or pull-down. External pull-up is recommended.
0=> JTAG ODT is disabled
1=> JTAG ODT is enabled

CAD NOTE:
Strap read at rising edge of RSMRST#. External pull-up is required. Recommend 100 kohm. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

PLACE R355 AND R404 CLOSE TO THE SPI SIGNAL TO AVOID STUB



OK

USB_OC_CD#

OK

10K PU at EB-TI22A

M.2 CNVi Mode Select

GPP_F2 / CNV_RGI_DT / UART0_TXD

A weak external PU is required to disable CNVi by default. When a companion chip is connected, the required PD on the device will pull the strap low to enable CNVi.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.
0= Integrated CNVi enabled.
1= Integrated CNVi disabled.
Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

Sampled at Rising edge of RSMRST#



OK

GPP_E10 / THCO_SPI1_CS#

GPP_E10 / THCO_SPI1_CS#

THCO_SPI1 Chip Select: Used to select the touch devices if it is connected to THCO_SPI1 interface.

THC NOT USED IN TENSOR-I22

CAD NOTE:

PLACE R414, R415 AND R422 CLOSE TO THE SPI SIGNAL TO AVOID STUB

OK

GPP_E11 / THCO_SPI1_CLK

THCO_SPI1 Clock: THCO SPI1 clock output from PCH. Supports 20 MHz, 33 MHz and 50 MHz.

THC NOT USED IN TENSOR-I22

CAD NOTE:

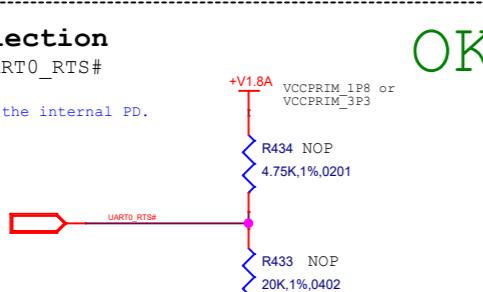
PLACE R429, R430 AND R431 CLOSE TO THE SPI SIGNAL TO AVOID STUB

OK

XTAL Frequency Selection

GPP_F0 / CNV_BRI_DT / UART0_RTS#

GPP_F0 Pin is at 0 (38.4 Mhz) by the internal PD.



OK

USB_OC_AB#

OK

10K PU at EB-TI22A

A weak external PU is required to disable CNVi by default. When a companion chip is connected, the required PD on the device will pull the strap low to enable CNVi.

This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.
0= Integrated CNVi enabled.
1= Integrated CNVi disabled.
Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.

Sampled at Rising edge of RSMRST#



OK

BOOT STRAP - BIT 0

R441 NOP

+3V3A

This strap has a 20 kohm ± 30% internal pull-down. This is bit 0 (LSB) of a total of 4-bit encoded pin straps for boot configuration.

This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).

4-bit boot strap configuration encodings:

0000 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is enabled

0010 = Master Attached Flash Configuration (BIOS / Intel CSME on SPI). eSPI is disabled

0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI

1000 = Slave Attached Flash Configuration (BIOS / Intel CSME on eSPI attached device).

1100 = BIOS on eSPI peripheral Channel; Intel CSME on slave attached SPI.

Other Reserved

Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.

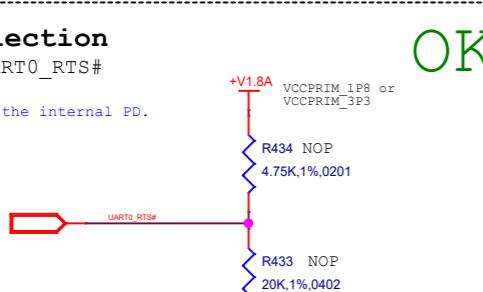
2. This signal is in the primary well.

OK

Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.

BOOT STRAP - BIT 1

GPP_H0



OK

BOOT STRAP - BIT 2

GPP_H1



OK

BOOT STRAP - BIT 3

GPP_H2

OK

Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.



OK

Title

PCH STRAPS (1 OF 2)

Size A3

Document Number <Doc>

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PCH STRAPS

DDP1 I2C / TBT_LSX0 pins VCC configuration

GPP_E19 / DDP1_CTRLDATA / TBT_LSX0_RXD / BSSB_LSO_TX
VCCPRIM_1P8 or VCCPRIM_3P3

Already Has 100K PU (R130) to 3V3S at the DP++ HANDLING (Page 21)

This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP1 I2C / TBT_LSX0 / BSSB_LSO pins at 1.8 V
1 = DDP1 I2C / TBT_LSX0 / BSSB_LSO pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

there is 2.2K PU on DPP1_CTRLDATA

Sampled at Rising edge of RSMRST#

OK

DDP2 I2C / TBT_LSX1 pins VCC configuration

GPP_E21 / DDP2_CTRLDATA / TBT_LSX1_RXD / BSSB_LS1_TX
NOTE: BSSB - Boundary Scan Sideband Low Speed Receive 1 for debug purposes

HIGH: 3.3V
LOW: 1.8V

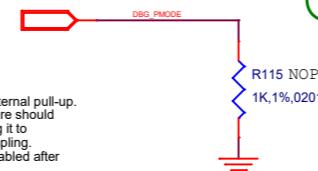
Already Has 100K PU (R137) to 3V3S at the DP++ HANDLING (Page 22)

LSx Interface:
The PCH LSx interface enables communication between one thunderbolt controller to another. TGL UP3/UP4 supports 4 pairs of LSx signals. The LSx signals use a UART interface. It operates at a 1 MHz baud rate and shares identical electrical characteristics/routing guidelines as UART.
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 1.8 V
1 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 3.3 V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

DBG PMODE

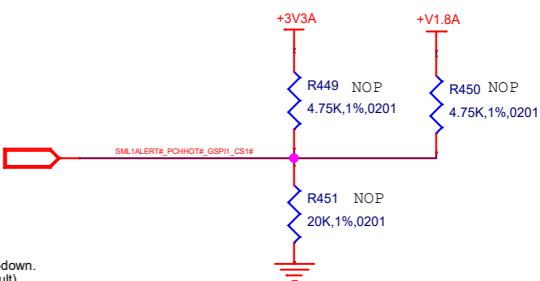
RESERVED



OK

CPUNSSC CLOCK FREQ

GPP_B23 / SML1ALERT# / PCHHOT# / GSPI1_CS1#

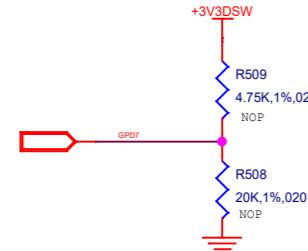


OK

GPD7

STRAP: RESERVED

Strap read at rising edge of DSW_PWROK. The internal pull-down 20 kohm ± 30% is disabled after DSW_PWROK is high. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



OK

GPP_F10

STRAP: RESERVED

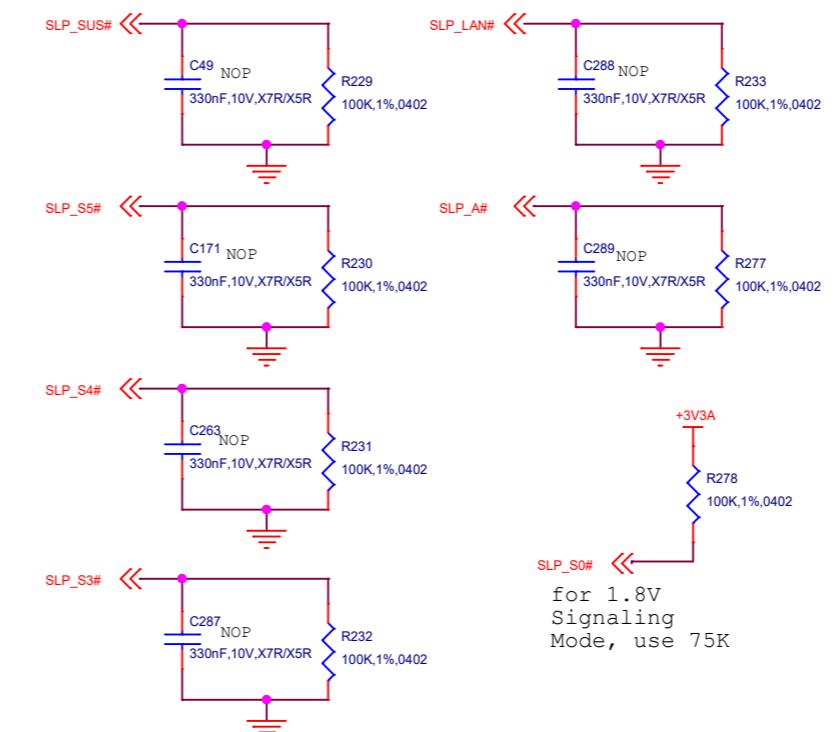
This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Sampled at Rising edge of RSMRST#

OK

PCH GLITCH ISSUE MITIGATION

RC0201

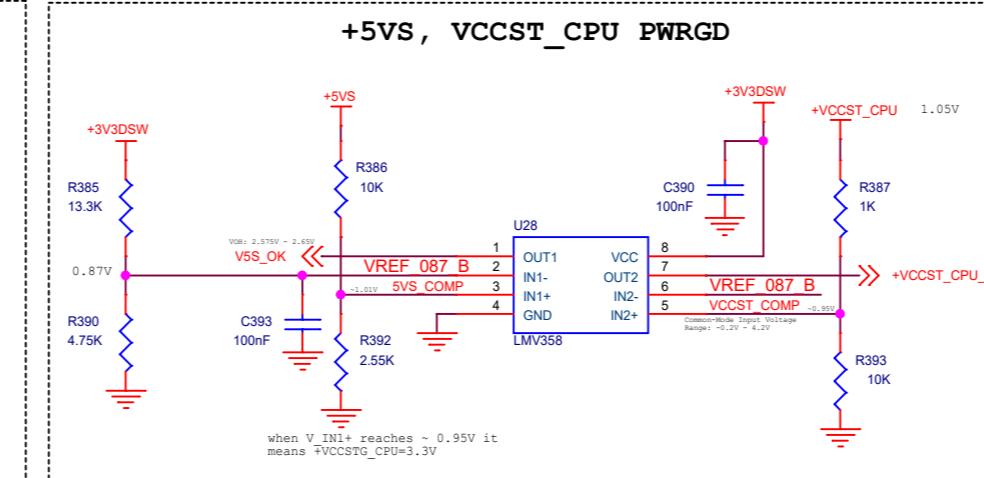
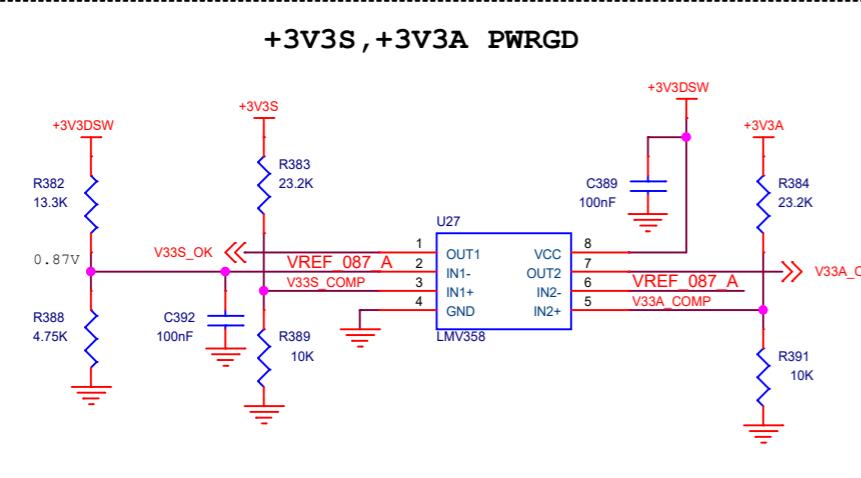


Title	
PCH STRAPS (2 OF 2)	
Size	Document Number
A3	<Doc>

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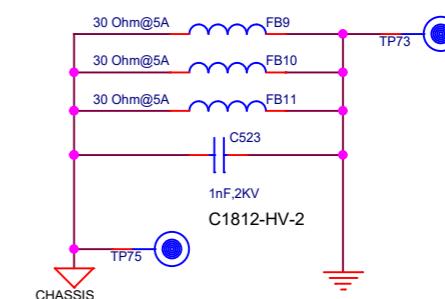
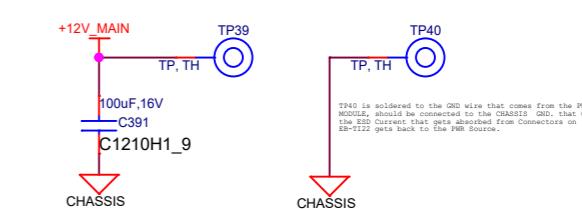
Sheet 33 of 41

Rev <Rev>Code>

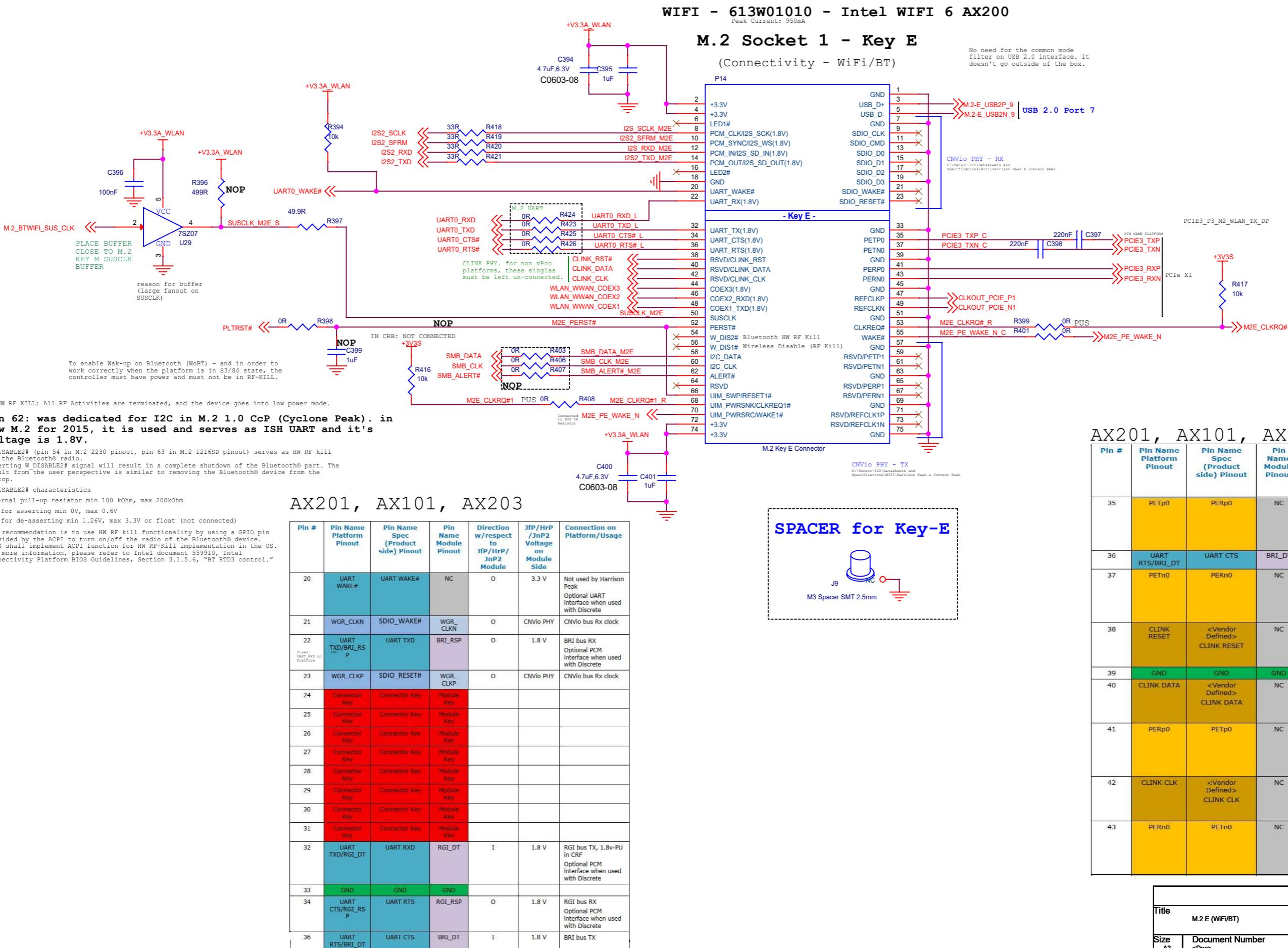


POWER MODULE CONNECTION - 12V

Hanging 1x2 connector



Title	3V3S 3V3A VCCST PWRGD
Size	A3
Document Number	<Doc>
Date:	Thursday, April 07, 2022
Rev	<Rev>

**AX201, AX101, AX203**

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/ respect to Jfp/Hrp / JnP2 Module	Jfp/Hrp / JnP2 Voltage on Module Side	Connection on Platform/Usage
35	PETp0	PERp0	NC			PCIe* PHY
36	UART_RTS/BRI_DT	UART_CTS	BRI_DT	I	1.8 V	BRI bus TX
37	PETn0	PERn0	NC			PCIe* PHY
38	CLINK_RESET	<Vendor Defined> CLINK_RESET	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
39	GND	GND	GND			
40	CLINK_DATA	<Vendor Defined> CLINK_DATA	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
41	PERp0	PETp0	NC			PCIe* PHY
42	CLINK_CLK	<Vendor Defined> CLINK_CLK	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
43	PERn0	PETn0	NC			PCIe* PHY

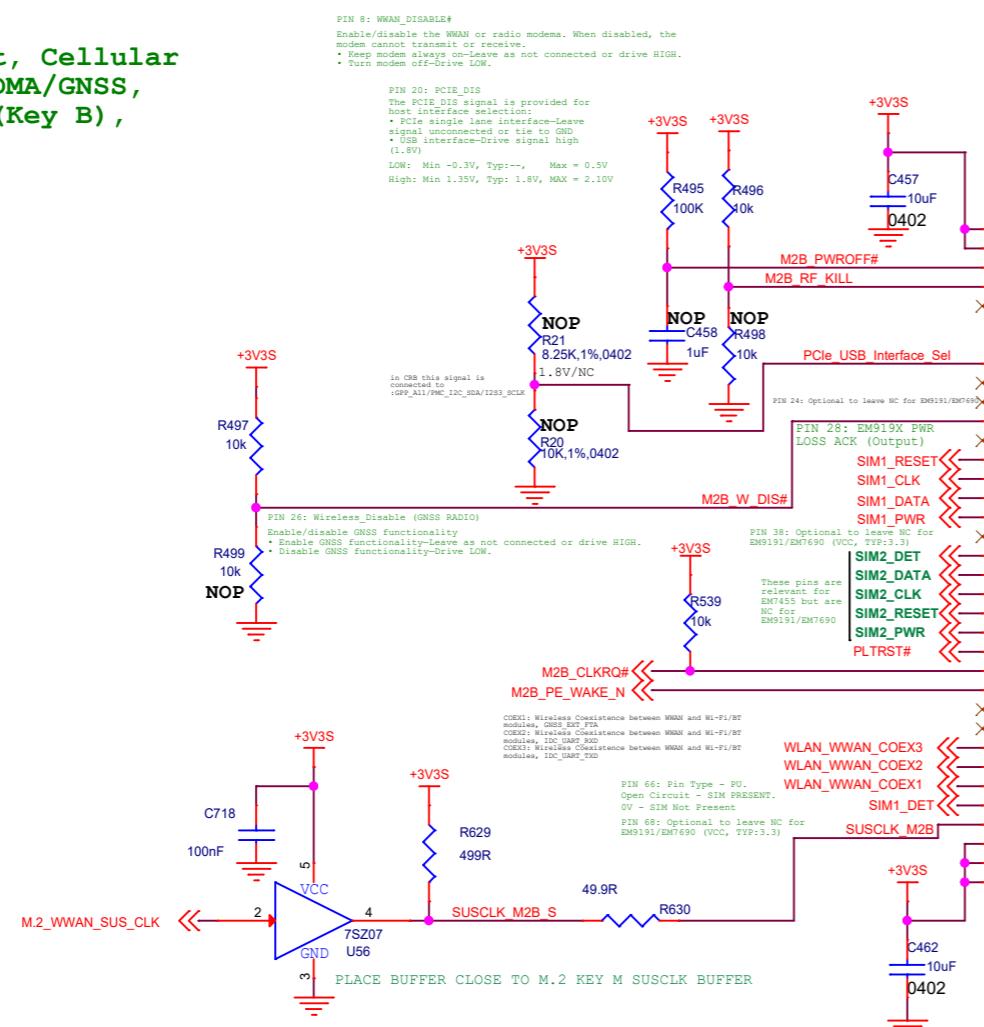
Title
M.2 E (WiFi/BT)

Size A3 Document Number
<Doc>

Rev <Rev>

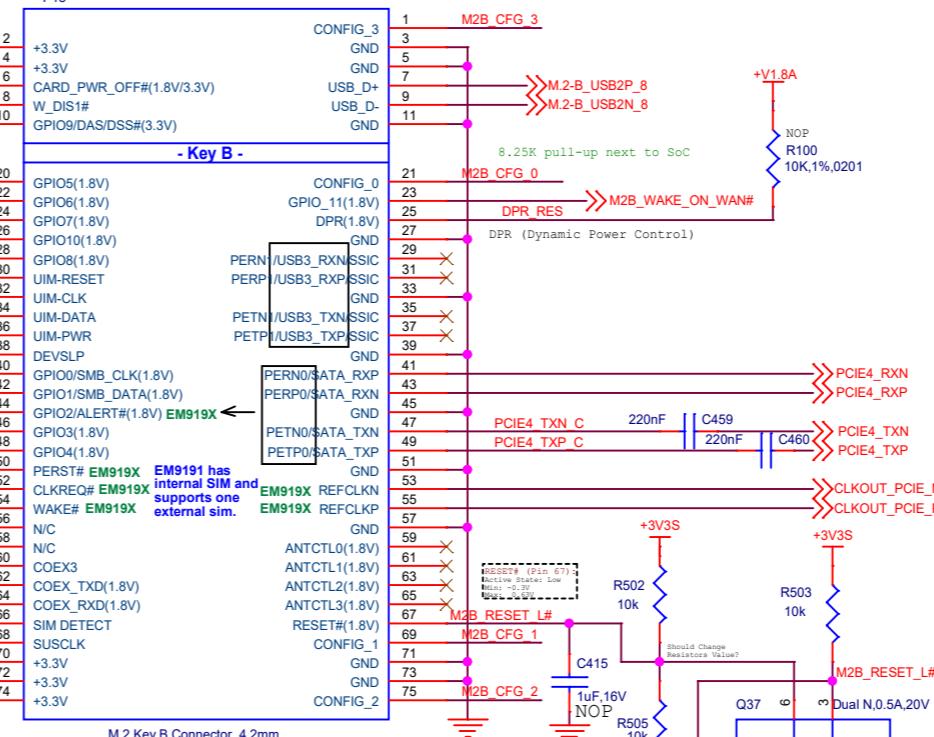
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Communication Equipment, Cellular Modem, 5G/LTE/HSPA+/WCDMA/GNSS, Global-Band, M.2 3052 (Key B), Sierra EM9191



613B01016 P 150/270 IN TL-SBC M.2 Socket 2 - Key B (WWAN, NO SATA)

No need for the common mode filter on USB 2.0 interface. It doesn't go outside of the box.



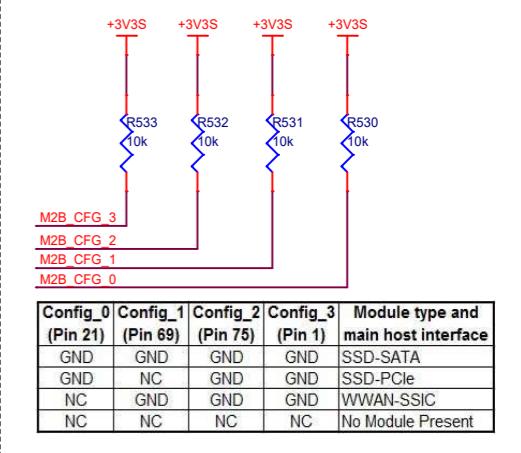
CONFIG 1,2,3:
Tied to Ground on the WWAN M.2 module at the M.2 interface connector.

CONFIG 0:

This signal is not connected on the WWAN M.2 module.

Product Side Pinout

M.2 CONFIG PINS



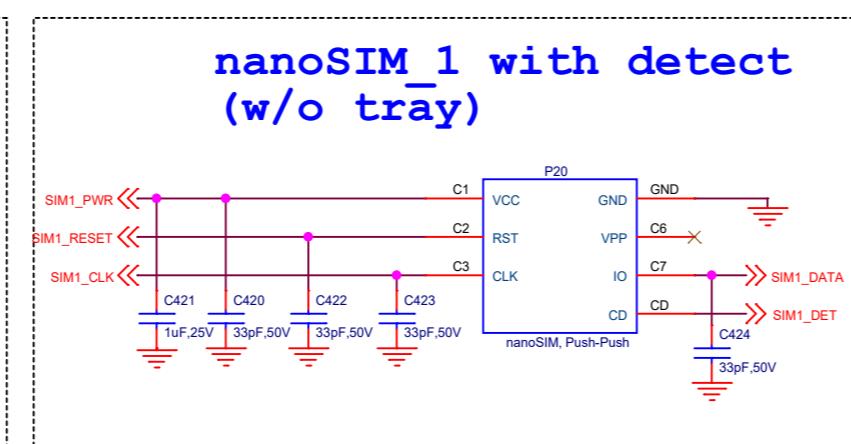
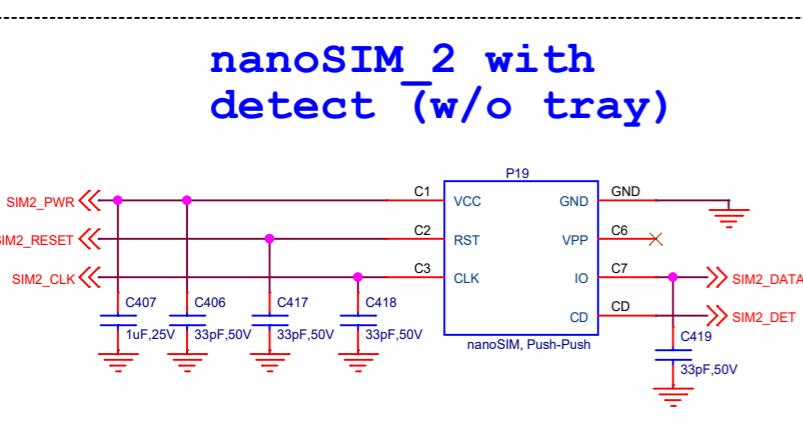
EM919X

Table 3-1: Host Interface (75-pin) Connections—Module View (Continued)

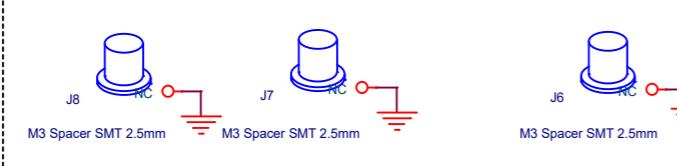
Pin	Signal name	Pin type ^a	Description	Direction ^b	Active state	Voltage levels (V)		
						Min	Typ	Max
41	PCIe_TXM0		PCIe Negative Transmit Data	Output	Differential	-	-	-
42	QTM1_PON ^c	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	-	1.8
43	PCIe_TXP0		PCIe Positive Transmit Data ^d	Output	Differential	-	-	-
44	QTM2_PON ^c	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	-	1.8
45	GND	V	Ground	Input	Power	-	0	-
46	QTM3_PON ^c	O	mmWave antenna module Power On signal (from EM9190)	Output	High	1.35	-	1.8
47	PCIe_RXM0		PCIe Negative Receive Data ^d	Input	Differential	-	-	-
48	QTM_IO_1.9V ^d	V	1.904 V power supply	Output	Power	1.8	1.904	2
49	PCIe_RXP0		PCIe Positive Receive Data ^d	Input	Differential	-	-	-
50	PCIe_PERST_N		PCIe Reset	Input	Low	0	-	0.7
51	GND	V	Ground	Input	Power	-	0	-
52	PCIe_CLKREQ_N	OC	PCIe Clock Request	Output	Low	0	-	0.35
53	PCIe_REFCLKM		PCIe Negative Reference Clock	Input	Differential	-	-	-
54	PCIe_PEWAKE_N	OC	PCIe Wake	Output	Low	0	-	0.35
55	PCIe_REFCLKP		PCIe Positive Reference Clock	Input	Differential	-	-	-
56	NC		Reserved—Host must not repurpose this pin.					
57	GND	V	Ground	Input	Power	-	0	-
58	NC		Reserved—Host must not repurpose this pin.					
59	ANT_CTRL0		Antenna tuning control (low bands)	Output	High	1.35	-	1.8
60	Reserved		Reserved—Host must not repurpose this pin.					
61	ANT_CTRL1		Antenna tuning control (low bands)	Output	High	1.35	-	1.80

nanoSIM 2 with detect (w/o tray)

nanoSIM 1 with detect (w/o tray)



Spacers for Key-B & Key-M Heatsink

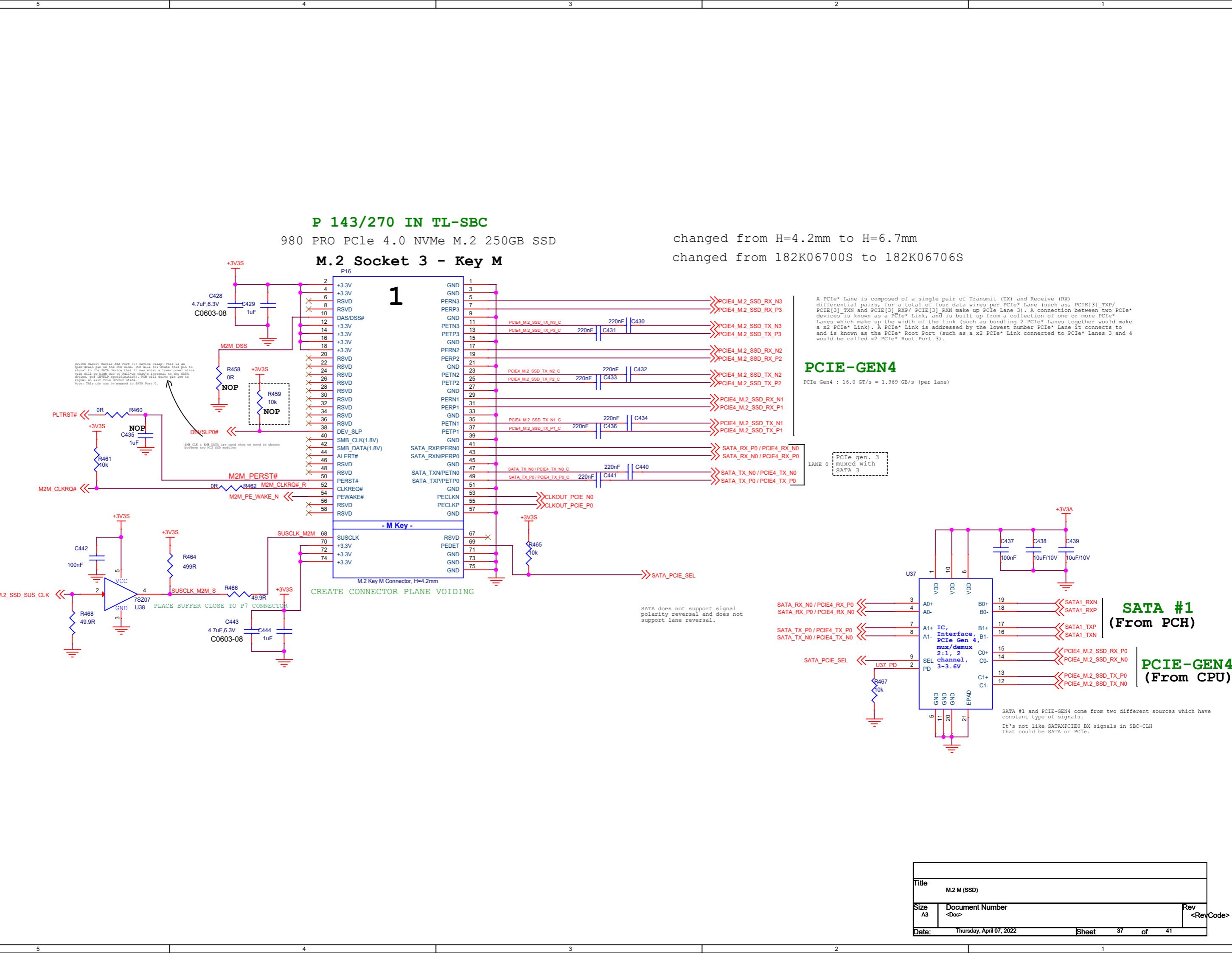


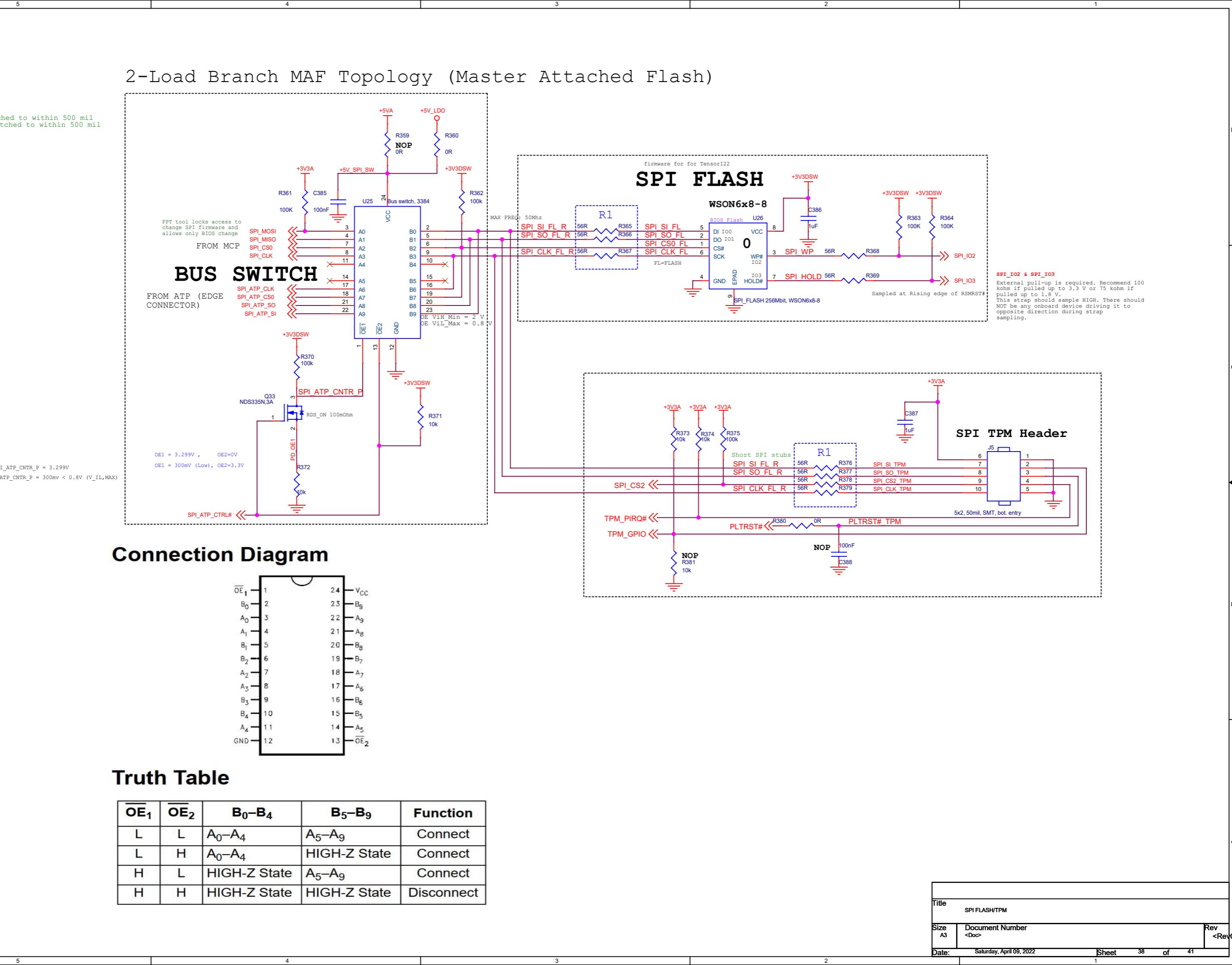
Title M.2 B (WWAN)

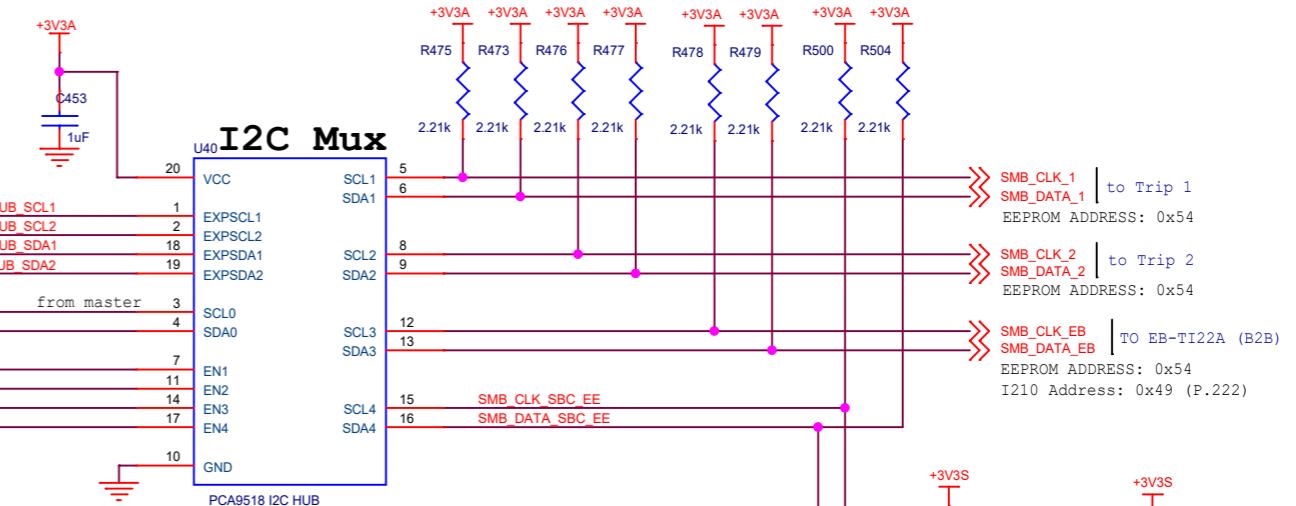
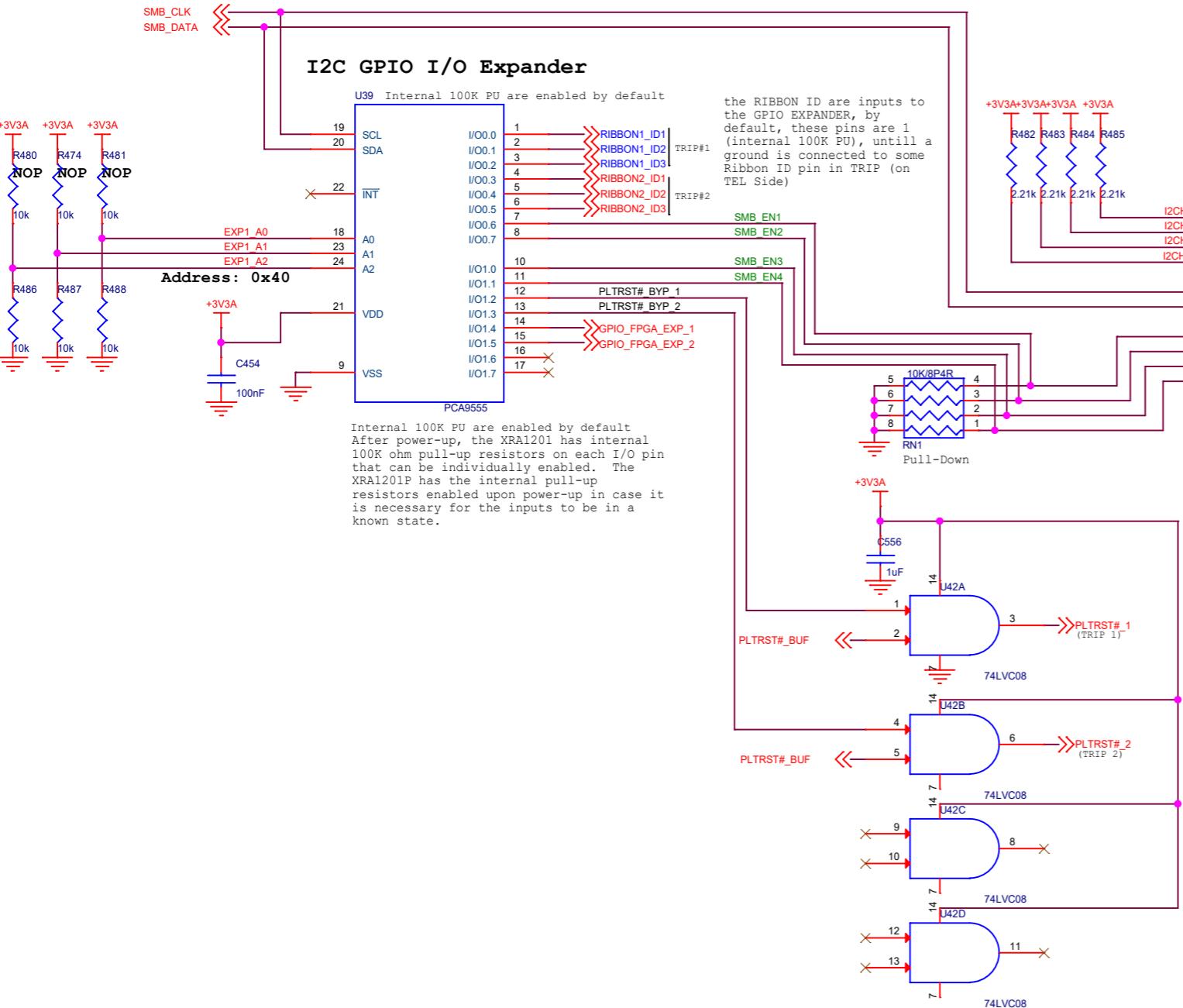
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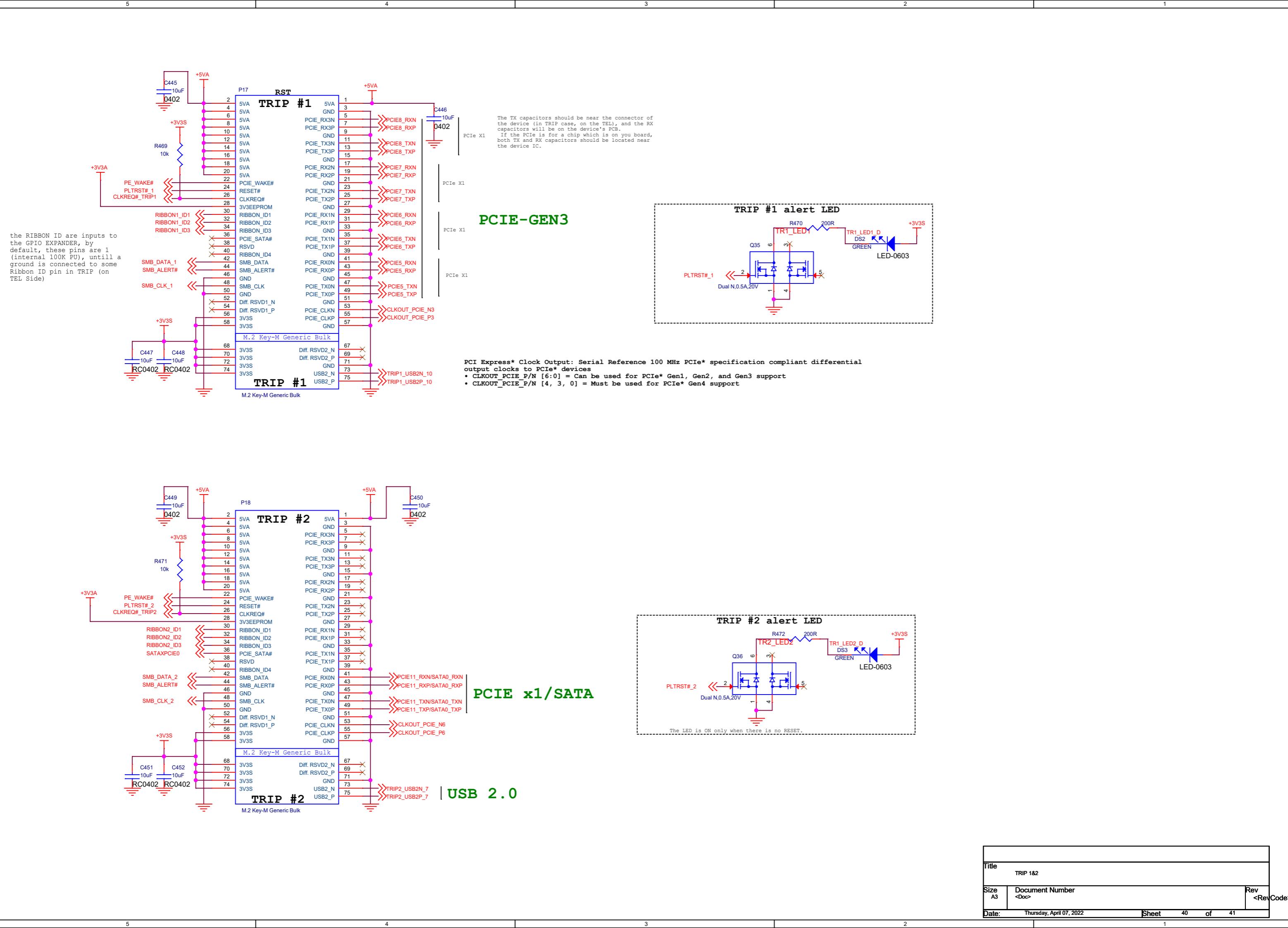


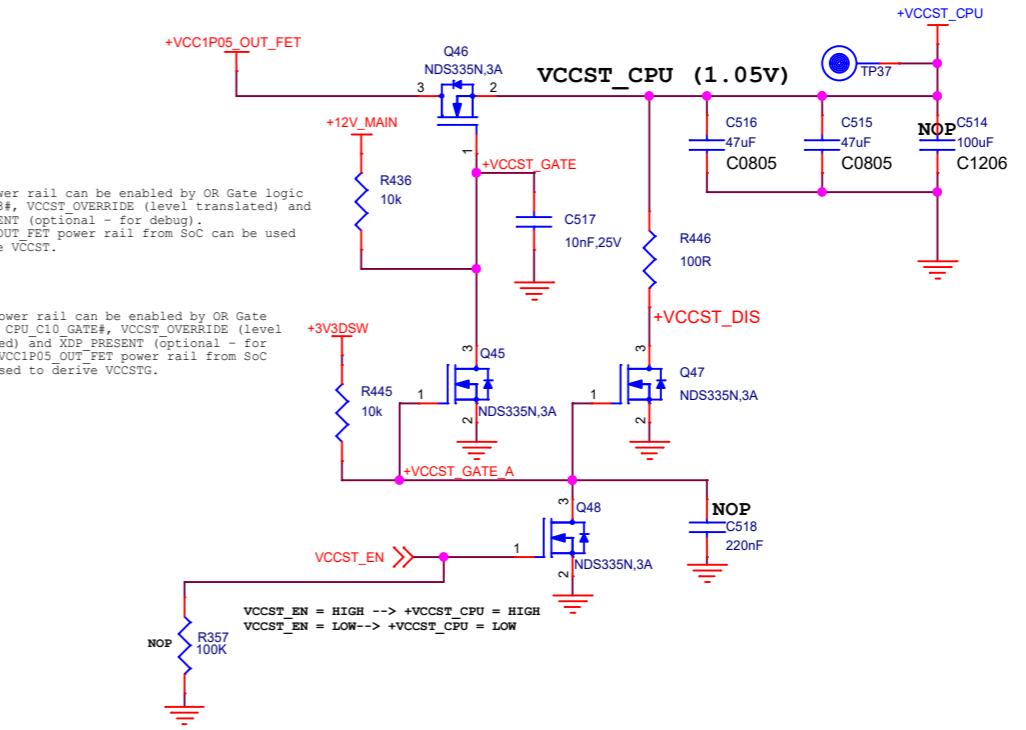


by default, the GPIO expander has internal pull up of 100K, which causes the EN pins to be 0.3V (because of 10K pull down). 0.3 is lower than the VIL which is 0.5V.

There are TELS that are not supposed to work on certain TRIPS.
the BIOS reads what is written on each TEL's EEPROM and according to it, it knows which TEL is this and it decides whether to send a reset through PLTRST#_BYP_1 and PLTRST#_BYP_2.
The purpose of the reset is not freeze the system in case of mis-installing of TELS.
the RESET is sent only to the SPECIFIC TEL.
AND Gate: Reset Override - if you place an incorrect TEL that shouldn't work on specific TRIP, the BIOS should identify this (the address on TEL is sent back through GPIO EXP to BIOS and then BIOS initiates a reset using PLTRST#_BYP_1).
the GPIO EXP is like an EEPROM, it has a wide range of addresses, and we can change the value of each bit to 0 or 1.
EEPROM ADDRESS ON ALL TELS ARE THE SAME (0x54) BUT DATA THAT SPECIFIES THE PURPOSE OF EACH TEL IS DIFFERENT.

Title		SMBus_MUX/GPIO_EXPANDER	
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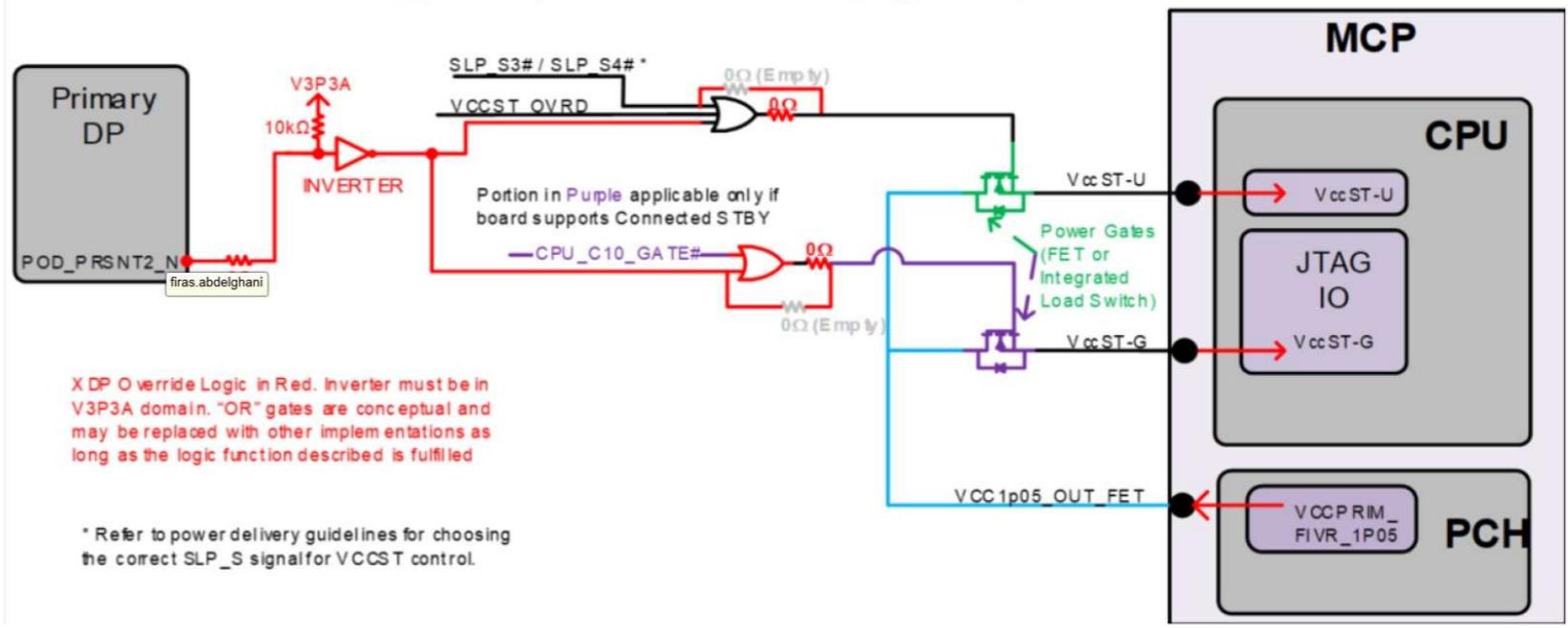




UN-IMPLEMENTED (VCCSTG CPU & VCCST CPU WERE MERGED TOGETHER) :

Concept of VccST/VccST-G Power Override Mechanism:

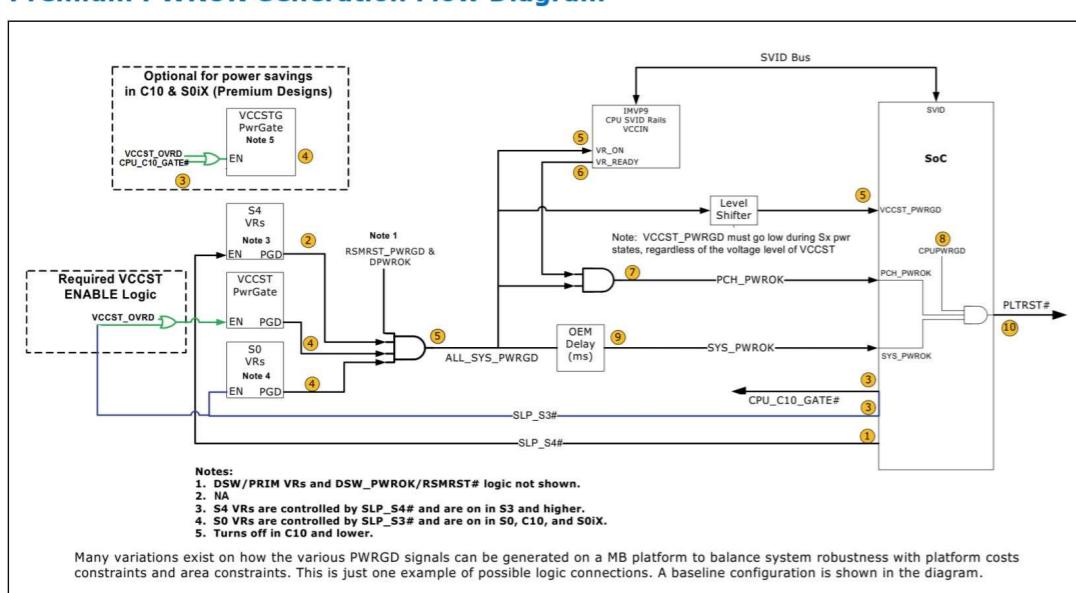
When the external debugger is plugged in, POD_PRSNT2_N will be driven to GND. VccST/VccST-G will be forced on in all Sx states to support PCH Sx open-chassis debug via JTAG without additional isolation logic. If S0-only open-chassis PCH debug is acceptable, then the override mechanism in red is not required unless CPU C10 debug support is required.



* Refer to power delivery guidelines for choosing the correct SLP_S signal for VCCST control.

IN VOLUME: VccSTG gated by SLP_S3#

IN Premium, VccSTG gated by {CPU_C10_GATE#}



Many variations exist on how the various PWROK signals can be generated on a MB platform to balance system robustness with platform costs constraints and area constraints. This is just one example of possible logic connections. A baseline configuration is shown in the diagram.

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