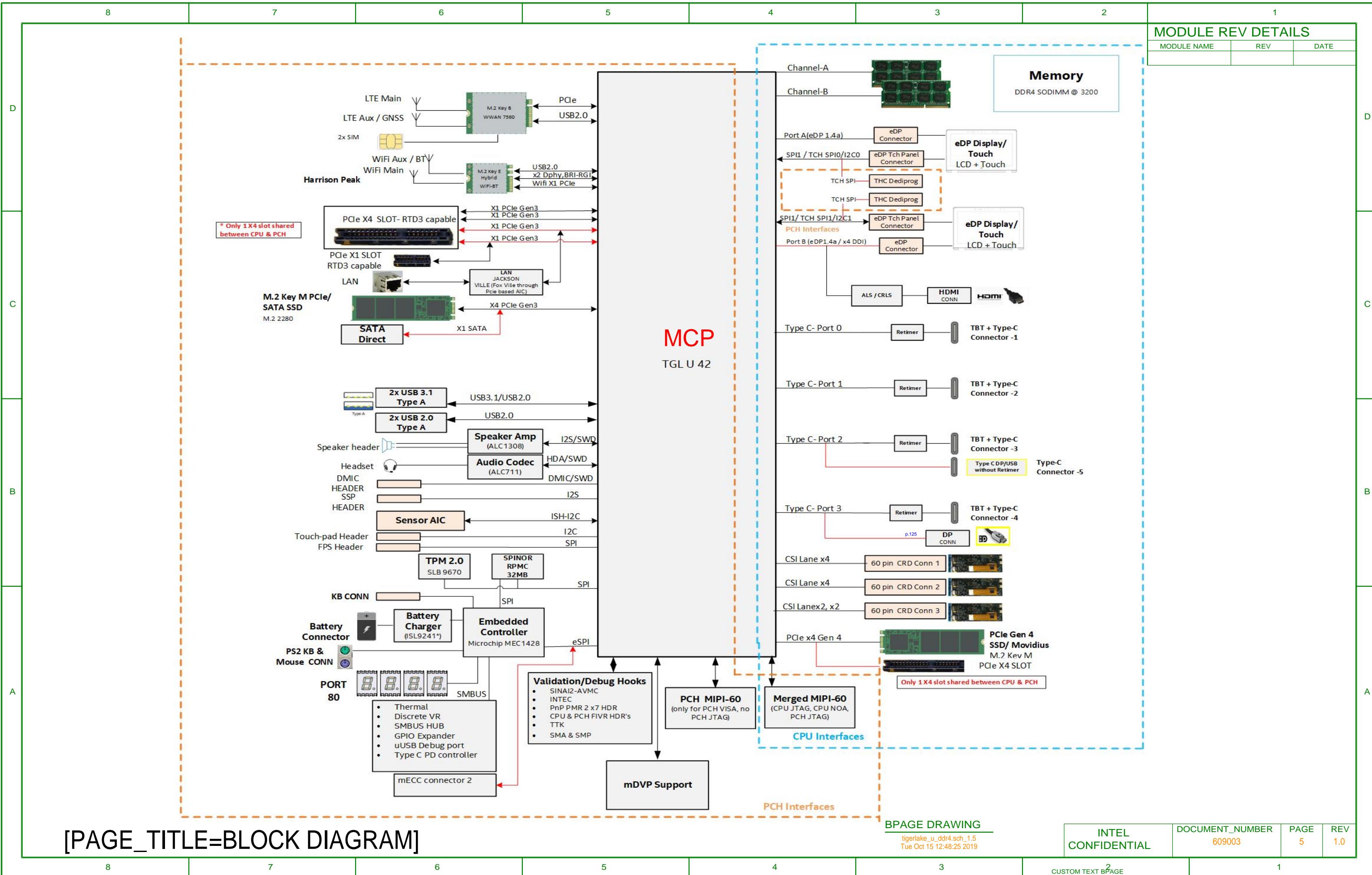


| 8  | 7 | 6 | 5 | 4   | 3 | 2               | 1                  |
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| [1. TITLE PAGE]  |   |   |   | [47. CLOCK - CRYSTAL]   |   |                 | MODULE REV DETAILS |
| [2. INDEX -1]  |   |   |   | [48. GPIO - ISH GPIO SHARING OPTIONS - 1]                             |   |                 | MODULE NAME        |
| [3. INDEX -2]  |   |   |   | [49. TGL-U MCP (12 OF 21) - SYSTEM POWER MANAGEMENT]                  |   |                 | REV                |
| [4. INDEX -3]  |   |   |   | [50. SYSTEM POWER MANAGEMENT OPTIONS]                                 |   |                 | DATE               |
| [5. BLOCK DIAGRAM]   |   |   |   | [51. PLATFORM RESET BUFFER]   |   |                 |                    |
| [6. LED DISCRIPTION]   |   |   |   | [52. TGL-U MCP (13 OF 21) - CPU POWER 1 OF 2]                         |   |                 |                    |
| [7. Z0 VS A0 PINLIST]  |   |   |   | [53. TGL-U MCP (15 OF 21) - CPU POWER 2 OF 2]                         |   |                 |                    |
| [8. TABLE - MPHYS MAPPING]   |   |   |   | [54. CPU PDBOM 1 OF 2]  |   |                 |                    |
| [9. ALC711 ES1 vs ES2]   |   |   |   | [55. CPU PDBOM 2 OF 2]  |   |                 |                    |
| [10. CLK_SRC MAPPING]  |   |   |   | [56. PCH PDBOM 2 OF 2]  |   |                 |                    |
| [11. JUMPER/SWITCH SETTINGS]   |   |   |   | [57. TGL-U MCP (14 OF 21) - PCH POWER 1 OF 2]                         |   |                 |                    |
| [12. TGL-U MCP (1 OF 21) - DISPLAY & TYPE-C (TBT/DISPLAY)]                               | ✓ |   |   | [58. RESERVE]   |   |                 |                    |
| [13. DISPLAY - DDIA - PORT AC CAPS]  |   |   |   | [59. PCH PDBOM 1 OF 2]  |   |                 |                    |
| [14. DISPLAY - DDIB - PORT SHARING, AC CAPS]   |   |   |   | [60. PCH DERIVED RAILS]   |   |                 |                    |
| [15. DISPLAY - TYPE-C PORT 0 SHARING, AC CAPS]   |   |   |   | [61. RESERVED]  |   |                 |                    |
| [16. DISPLAY - TYPE-C PORT 1 AC CAPS]  |   |   |   | [62. TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)]                       |   |                 |                    |
| [17. DISPLAY - TYPE-C PORT 2 AC CAPS]  |   |   |   | [63. TGL-U MCP (19 OF 21) - FIVR DEBUG]                               |   |                 |                    |
| [18. DISPLAY - TYPE-C PORT3 SHARING, AC CAPS]  |   |   |   | [64. CPU FIVR DEBUG HEADER]   |   |                 |                    |
| [19. TGL-U MCP (2 OF 21) - MEMORY CHANNEL - A]   |   |   |   | [65. TGL-U MCP (20 OF 21) - RESERVED SIGNALS]                         |   |                 |                    |
| [20. TGL-U MCP (3 OF 21) - MEMORY CHANNEL - B]   |   |   |   | [66. JTAG/CFG - CFG TERMINATIONS]                                     |   |                 |                    |
| [21. TGL-U MCP (4 OF 21) - CPU MISC]   |   |   |   | [67. JTAG/CFG - MERGED JTAG OPTIONS]                                  |   |                 |                    |
| [22. TGL-U MCP (5 OF 21) - LSIO - SPI, ESPI, THC, MLINK, SMLINK, SMBUS]                  |   |   |   | [68. JTAG/CFG - CPU/PCH MERGED MIPI 60 CONNECTOR]                     |   |                 |                    |
| [23. TGL-U MCP (6 OF 21) - LPSS - GSPI, UART, I2C, ISH-SPI, ISH UART, ISH I2C, ISH GPIO] |   |   |   | [69. JTAG/CFG - PCH DEBUG SHARING OPTIONS]                            |   |                 |                    |
| [24. TGL-U MCP (7 OF 21) - AUDIO, SD3.0, DISPLAY MISC]                                   |   |   |   | [70. JTAG/CFG - PCH MIPI 60 VISA CONNECTOR]                           |   |                 |                    |
| [25. PCH SMBUS EXPANDER, FRU]  |   |   |   | [71. PD AIC CONNECTOR]  |   |                 |                    |
| [26. SHARING OPTIONS - 1 - ESPI, SMLINKS]  |   |   |   | [72. USB-C RSVD]]   |   |                 |                    |
| [27. GPIO - LPSS SHARING OPTIONS - 2 - GSPI, UART]                                       |   |   |   | [73. MECC TRIPAD SHARING]   |   |                 |                    |
| [28. GPIO - LPSS SHARING OPTIONS - 3 - I2C, ISH I2C]                                     |   |   |   | [74. TGL-U MCP(8 OF 21)- RESERVE GENERAL -5]                          |   |                 |                    |
| [29. GPIO - LPSS SHARING OPTIONS - 4 - I2C]  |   |   |   | [75. CPU_STRAPS_1]  |   |                 |                    |
| [30. GPIO - SHARING OPTIONS -1 - THC, SPI, UART]   |   |   |   | [76. CPU_STRAPS_2]  |   |                 |                    |
| [31. GPIO - ISH SHARING OPTIONS -2 - I2C, GPIO]  |   |   |   |   |   |                 |                    |
| [32. GPIO - OTHER PCH GPIO SHARING OPTIONS - 1]  |   |   |   |   |   |                 |                    |
| [33. SVID SIGNALS]   |   |   |   | [79. FLEX CONNECTOR]  |   |                 |                    |
| [34. TGL-U MCP (9 OF 21) - MODPHY ]  |   |   |   | [80. MEMORY - DDR4 SODIMM CHANNEL -A (1 OF 2)]                        |   |                 |                    |
| [35. PCIE PORT 0&1 SHARING OPTIONS, AC CAPS]   |   |   |   | [81. MEMORY - DDR4 SODIMM CHANNEL -A (2 OF 2)]                        |   |                 |                    |
| [36. PCIE PORT 2&3 SHARING OPTIONS, AC CAPS]   |   |   |   | [82. MEMORY - DDR4 SODIMM CHANNEL -B (1 OF 2)]                        |   |                 |                    |
| [37. PCIE PORT 4&5 SHARING OPTIONS, AC CAPS]   |   |   |   | [83. MEMORY - DDR4 SODIMM CHANNEL -B (2 OF 2)]                        |   |                 |                    |
| [38. PCIE PORT 6&7 SHARING OPTIONS, AC CAPS]   |   |   |   | [84. MEMORY - DDR4 SODIMM CHANNEL -A PD BOM]                          |   |                 |                    |
| [39. PCIE PORT 8&9 SHARING OPTIONS, AC CAPS]   |   |   |   | [85. MEMORY - DDR4 SODIMM CHANNEL -BPD BOM]                           |   |                 |                    |
| [40. PCIE PORT 10&11 SHARING OPTIONS, AC CAPS]   |   |   |   | [86. MEMORY - DDR VREF CIRCUITRY -1 - PROCESSOR, OPTIONS]             |   |                 |                    |
| [41. PCIE PORT RESET RTD3 CIRCUIT]   |   |   |   | [87. MEMORY - DDR4 SODIMM & LPDIMM CONN PINOUT]                       |   |                 |                    |
| [42. PCIE WAKE RTD3  |   |   |   | [88. MEMORY - DDR VREF CIRCUITRY - 3 - AVMC OPTION]                   |   |                 |                    |
| [43. USB2 CMC & SHARING]   |   |   |   | [89. DISPLAY - eDP connector 1 - CMC]                                 |   |                 |                    |
| [44. TGL-U MCP (10 OF 21) - CSI2, CNVI]  |   |   |   | [90. DISPLAY - eDP connector 1 - MISC]                                |   |                 |                    |
| [45. TGL-U MCP (11 OF 21) - CLOCK SIGNALS]   |   |   |   | [91. DISPLAY - eDP connector 1]                                       |   |                 |                    |
| [46. SRC CLOCKS ]  |   |   |   | [92. DISPLAY - EDP CONNECTOR 2 - CMC]                                 |   |                 |                    |
| [PAGE_TITLE=INDEX -1]  |   |   |   | BPAGE DRAWING<br>tigerlake_u_ddr4.sch_1.2<br>Thu Dec 26 15:55:37 2019 |   |                 |                    |
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| RefDes | LED Description |
|--------|-----------------|
| DS4G1  | V1P05_CTRL      |
| DS4G2  | VNN_CTRL        |
| DS8H5  | S3 STATE        |
| DS8H3  | S4 STATE        |
| DS8H4  | S5 STATE        |
| DS8H2  | DSW STATE       |
| DS8H1  | M0/M3 STATE     |
| DS3H1  | ME PWR Gate     |

| RefDes | LED Description |
|--------|-----------------|
| DS8H6  | CAPS LOCK       |
| DS8H7  | NUM LOCK        |
| DS7G1  | POWER BUTTON    |
| DS7H1  | BAT STATUS LED  |

| RefDes | LED Description |
|--------|-----------------|
| DS8G6  | SLP S0 LED      |
| DS8G4  | PWRGD           |
| DS8G5  | CATERR          |
| DS6G1  | C10 GATE        |
| DS6G2  | CS INDICATE     |

| RefDes | LED Description            |
|--------|----------------------------|
| DS9B1  | SATA Direct connect DEVSLP |
| DS9E1  | M.2 SSD DEVSLP             |
| DS8G7  | SATA ACTIVITY              |
| DS6D1  | PCIE LINK DOWN             |
| DS4G4  | WLAN                       |
| DS4G3  | BT                         |
| DS7D1  | WWAN                       |

| Error Type       | Error Code | Caps Lock LED<br>(DS9H2) | Scroll Lock LED<br>(DS7G1) | Num Lock LED<br>(DS9J1) |
|------------------|------------|--------------------------|----------------------------|-------------------------|
| No Error         | 0          | Off                      | Off                        | Off                     |
| RSMRST_PWRGD_N   | 1          | Off                      | Off                        | Flash                   |
| PM_SLP_S5_N      | 2          | Off                      | Flash                      | Off                     |
| PM_SLP_S4_N      | 3          | Off                      | Flash                      | Flash                   |
| PM_SLP_S3_N      | 4          | Flash                    | Off                        | Off                     |
| PM_SLP_M_N       | 5          | Flash                    | Off                        | Flash                   |
| ALL_SYS_PWRGD    | 6          | Flash                    | Flash                      | Off                     |
| PLT_RST_N        | 7          | Flash                    | Flash                      | Flash                   |
| DOCK_SYS_PWRGD_N | 8          | On                       | On                         | Flash                   |
| SUSWARNB         | 9          | On                       | Flash                      | On                      |

Note: KSC Thermal Shutdown is indicated by flashing of Num\_Lock and Caps\_Lock LEDs alternatively.  
DS7G1 acts as led indication for error code in case of any error otherwise works as power button LED

[PAGE\_TITLE= LED DISCRIPTION]

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| MODULE REV DETAILS |     |      |
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| MODULE NAME        | REV | DATE |
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| Interface             | WHL       | TGL       |
|-----------------------|-----------|-----------|
| Board ID              |           |           |
| PCIE Gen4 – DEKEL PHY | No        | Yes       |
| TYPE C                | No        | Yes       |
| XTAL_IN               | 24MHz     | 38.4MHz   |
| Memory                | 1 Channel | 2 channel |
| CSI                   | No        | Yes       |

| No.   | Changes            | WHL                                | TGL  | Status      |
|-------|--------------------|------------------------------------|--|-------------|
| 1     | XXDP_COMP          | 24.9 ohm PU to VCCIO               | 24.9 ohm PU to VCCIN<br>/+VCC1P05_OUT_FET (default)<br>on extra added pin on one of the<br>spare pins of TGL_A0. | implemented |
| 2     | XXDDR_COMP[0]      | 121 ohm PD                         | 121 ohm PD on Pin DW 49  | implemented |
| 3     | XXDDR_COMP[1]      | 80.6 ohm PD                        | 80.6 ohm PD on pin DW47  | implemented |
| STRAP |                    |                                    |  |             |
| 4     | SVID DISABLE STRAP | J3B1 to 1-2                        | J3B1 to 1-X  | WIP         |
| 5     | GPPC_F10           | High, SW9C1 Switch closed, 4.7K PU | LOW, Internal PD 20K   | WIP         |
| 6     | GPPC_F0*           | High, SW9C1 Switch closed, 4.7K PU | LOW, Internal PD 20K   | WIP         |

[PAGE\_TITLE=Z0 VS A0 PINLIST]

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|   |   |           |                         |   |   |                 | MODULE NAME    REV    DATE  |  |  |  |  |
| <b>TGL-U 42 ROW RVP's Mphy Allocation</b> |   |           |                         |   |   |                 |                             |  |  |  |  |
| PCIe Controller                           |   | Lane #    | Flex IO                 |   | HSIO Topology 1<br>(Default)                | HSIO Topology 2 | HSIO Topology 3<br>(SV SKU) |  |  |  |  |
| x4 Controller 1                           |   | Lane 0    | PCIE3_1_USB31_1         |   |   |                 |                             |  |  |  |  |
|   |   | Lane 1    | PCIE3_2_USB31_2         |   |   |                 |                             |  |  |  |  |
|   |   | Lane 2    | PCIE3_3_USB31_3         |   |   |                 |                             |  |  |  |  |
|   |   | Lane 3    | PCIE3_4_USB31_4         |   |   |                 |                             |  |  |  |  |
| x4 Controller 2                           |   | Lane 4    | PCIE3_5                 |   | Lane 0 for x4 PCIe slot                     |                 | x4 PCIe Slot                |  |  |  |  |
|   |   | Lane 5    | PCIE3_6                 |   | Lane 1 for x4 PCIe slot                     |                 |                             |  |  |  |  |
|   |   | Lane 6    | PCIE3_7_LAN_0A_UFS_00   |   | Jacksonville Gbe LAN                        |                 |                             |  |  |  |  |
|   |   | Lane 7    | PCIE3_8_LAN_0B_UFS_01   |   | x1 PCIe Slot                                |                 |                             |  |  |  |  |
| x4 Controller 3                           |   | Lane 8    | PCIE3_9_LAN_0C_UFS_1_00 |   | M.2 Key M x4 SSD(Lane reversal for x4 PCIe) |                 | HSIO Connector              |  |  |  |  |
|   |   | Lane 9    | PCIE3_10_UFS_1_01       |   |   |                 |                             |  |  |  |  |
|   |   | Lane 10   | PCIE3_11_SATA_0         |   |   |                 |                             |  |  |  |  |
|   |   | Lane 11   | PCIE3_12_SATA_1         |   |   |                 |                             |  |  |  |  |
| x4 Controller 4<br>(Gen 4 North side)     |   | CPU Lane0 | CPU_PCIE_0              |   | M.2 Key M x4 SSD                            |                 | x4 PCIe Slot                |  |  |  |  |
|   |   | CPU Lane1 | CPU_PCIE_1              |   |   |                 |                             |  |  |  |  |
|   |   | CPU Lane2 | CPU_PCIE_2              |   |   |                 |                             |  |  |  |  |
|   |   | CPU Lane3 | CPU_PCIE_3              |   |   |                 |                             |  |  |  |  |

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| <b>MODULE REV DETAILS</b>      |   |   |   |   |   |   |   |
| MODULE NAME      REV      DATE |   |   |   |   |   |   |   |

| SRC CLK                      |   | SRC CLK REF                           |  | TGL U RVP mPHY allocation- DDR4 |  |                |  |
|------------------------------|---|---------------------------------------|--|---------------------------------|--|----------------|--|
| HSIO Topology 1<br>(Default) |   | HSIO Topology 2                       |  | HSIO Topology 3<br>(SV SKJ)     |  | HSIO Connector |  |
| 0                            | 0 | CPU Gen4 PCIe x4 M.2 SSD              |  | CPU Gen4 x4 PCIe Slot           |  |                |  |
| 1                            | 1 | M.2 Hybrid Key E- (WLAN x1 PCIe)      |  |                                 |  |                |  |
| 2                            | 2 | M.2 Key-B WWAN X1 PCIe                |  |                                 |  |                |  |
| 3                            | 3 | x4 M.2 SSD(Lane reversal for x4 PCIe) |  |                                 |  |                |  |
| 4                            | 4 | Gbe LAN                               |  |                                 |  |                |  |
| 5                            | 5 | x1 PCIe Slot                          |  |                                 |  |                |  |
| 6                            | 6 | PCH PCIe x4 PCIe DT Slot              |  |                                 |  |                |  |

[PAGE\_TITLE=CLK\_SRC MAPPING]

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| MODULE REV DETAILS |     |      |
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| MODULE NAME        | REV | DATE |
|                    |     |      |

| RefDes | Jumper Description                       | Default   |
|--------|--|-----------|
| J1A3   | MIPI60 OVERRIDE N                        | '1-X'     |
| J2H3   | MIPI60 PRESENT1 N                        | '1-X'     |
| J1C1   | TYPEC DISABLE                            | '1-X'     |
| J1F3   | NO REBOOT STRAP                          | '1-X'     |
| J1F4   | FLASH DESCRIPTOR SECURITY OVERRIDE STRAP | '1-X'     |
| J3B1   | SVID DISABLE STRAP                       | '1-X'     |
| J1F4   | A0 PERSONALITY STRAP                     | '1-X'     |
| J3H1   | DDI3 HPD                                 | '1-X'     |
| J9J5   | BT RF KILL N, WIFI RF KILL N             | '1-X,3-X' |
| J9J4   | CNVI Disable                             | '1-2'     |
| J5U1   | TOUCH PANEL POWER SUPPLY GENERATION      | '1-2'     |
| J8J3   | PROCHOT EC JPR                           | '1-X'     |
| J9J3   | SMC_RST_N JPR                            | '1-X'     |
| J9J2   | SMC_LID JPR                              | '1-X'     |
| J8D2   | SVID CLOCK                               | '1-2,3-X' |
| J8D3   | SVID ALERT                               | '1-2,3-X' |
| J8D4   | SVID DATA                                | '1-2,3-X' |
| J8G3   | PCH GLITCH ISSUE MITIGATION              | '1-X'     |
| J7G1   | SRTC/RTC CLEAR CMOS JPR                  | '1-X'     |
| J7H2   | SPD_PRSNT JPR                            | '1-2'     |
| J8H3   | FRU SMB CLK S3                           | '1-2'     |
| J8H5   | FRU SMB DATA S3                          | '1-2'     |
| J6J1   | PECI_MUX_CTRL_SNI_R                      | '1-X'     |
| J8J1   | FRU POWER SUPPLY                         | '1-2'     |
| J6G4   | H_PECI_CPU JPR                           | '1-X'     |

| RefDes | Jumper Description   | Default   |
|--------|--|---|
| SW4V1  | MIPI60 FN[0:3]   | 1-8(OFF);<br>2-7(OFF);<br>3-6(OFF);<br>4-5(OFF) |
| SW5V1  | 1 - VDDQ_VR_PWRGD - IMVP_VR_EN<br>2 - ALL_SYS_PWRGD - IMVP_VR_EN<br>3 - SATAXPCIE_0_SATAGP_0_R<br>4 - BIOS_REC           | 1-8(OFF);<br>2-7(OFF);<br>3-6(OFF);<br>4-5(OFF) |
| SW6J2  | 1 - EC_SHD_CS_SW<br>2 - NC<br>3 - RETIMER_BYPASS_STRAP<br>4 - ESPI_TESTCRD_DET   | 1-8(OFF);<br>2-7(OFF);<br>3-6(OFF);<br>4-5(OFF) |
| SW9C1  | 1 - BUF_PLT_RST_1.8 - WF_CAM_RST_N<br>2 - WF_CAM_RST_ND - WF_CAM_RST_N<br>3 +V1.8A - XTAL_SEL1_J<br>4 +V3.3A - XTAL_IN_J | 1-8(OFF);<br>2-7(ON);<br>3-6(OFF);<br>4-5(OFF)  |
| SW8W1  | 1 - PNP_NPNP_SKU<br>2 - VIRTUAL_DOCK_DET_N<br>3 - VIRTUAL_BATTERY<br>4 - FLIP_TO_TABLET_MODE                             | 1-8(OFF);<br>2-7(OFF);<br>3-6(OFF);<br>4-5(OFF) |

[PAGE\_TITLE=JUMPER/SWITCH SETTINGS]

## MODULE REV DETAILS

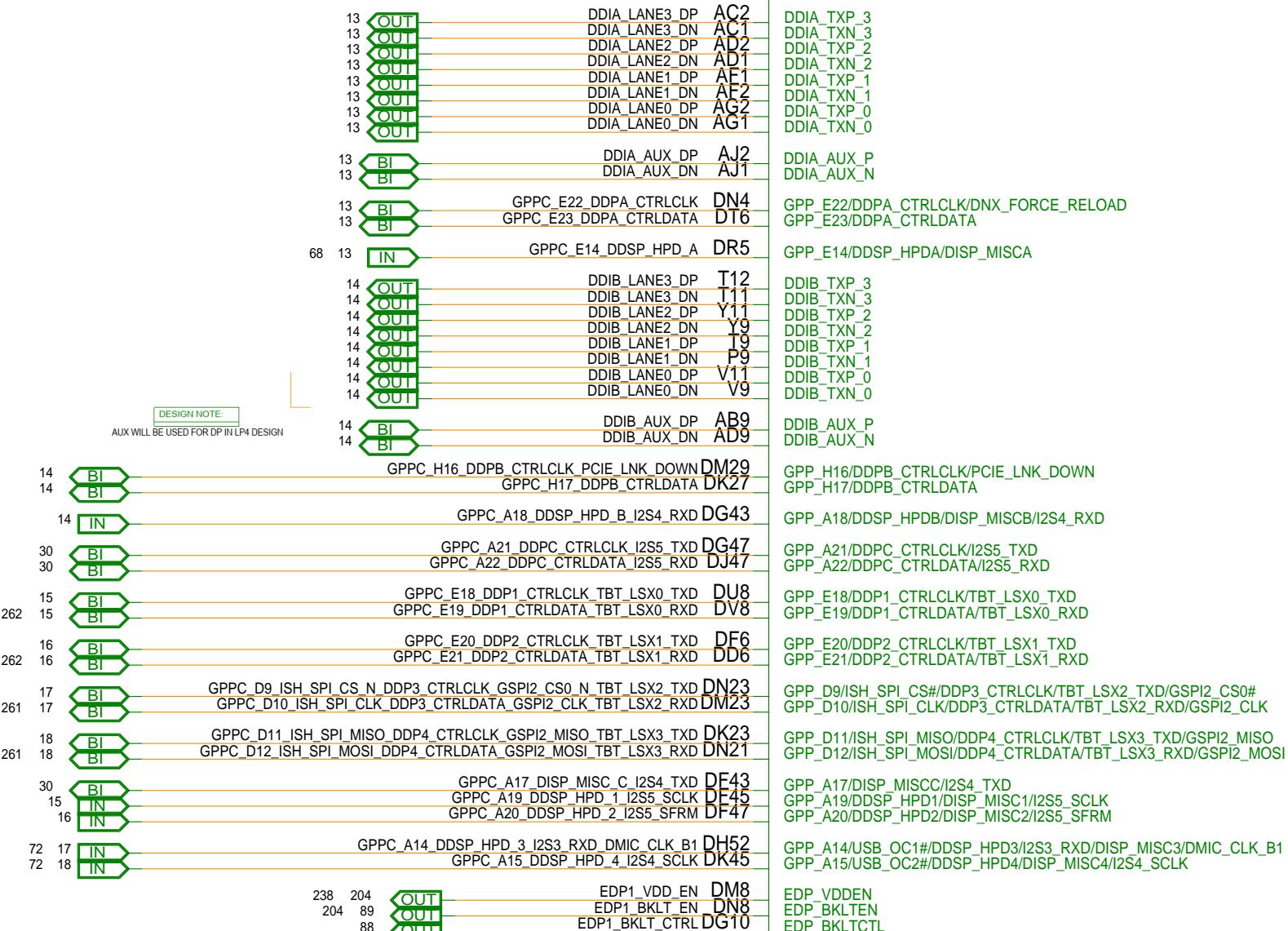
| MODULE NAME | REV | DATE |
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U4E1  
SOC1.6  
BGA  
TGL\_UP3\_IP\_EXT

1 OF 21

DESIGN NOTE:  
AUX WILL BE USED FOR DP IN LP4 DESIGN

DESIGN NOTE:

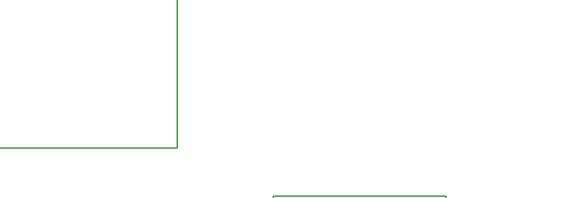
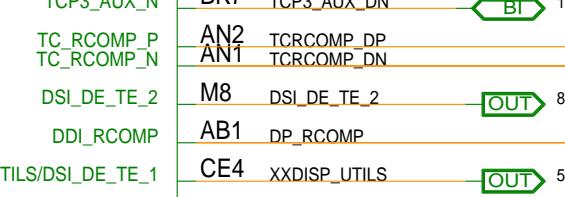
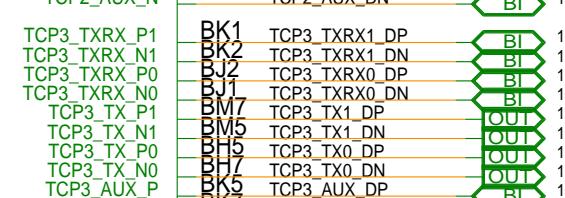
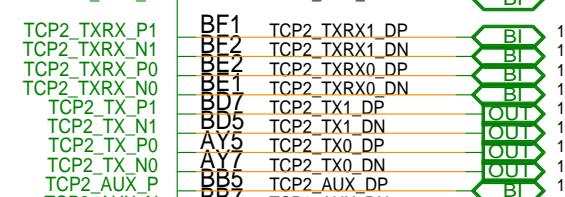
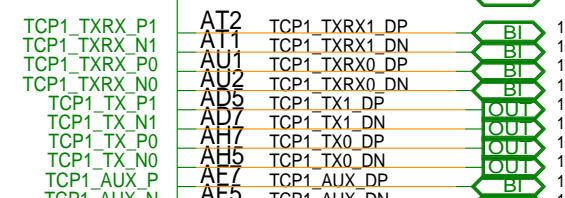
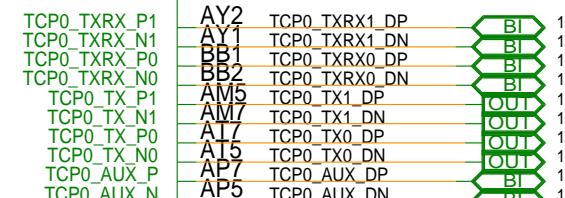
LSX\_A:LSX TXD, LSX\_B:LSX RXD

DESIGN NOTE:

LSX\_A:BSSB RXD, LSX\_B:BSSB TXD

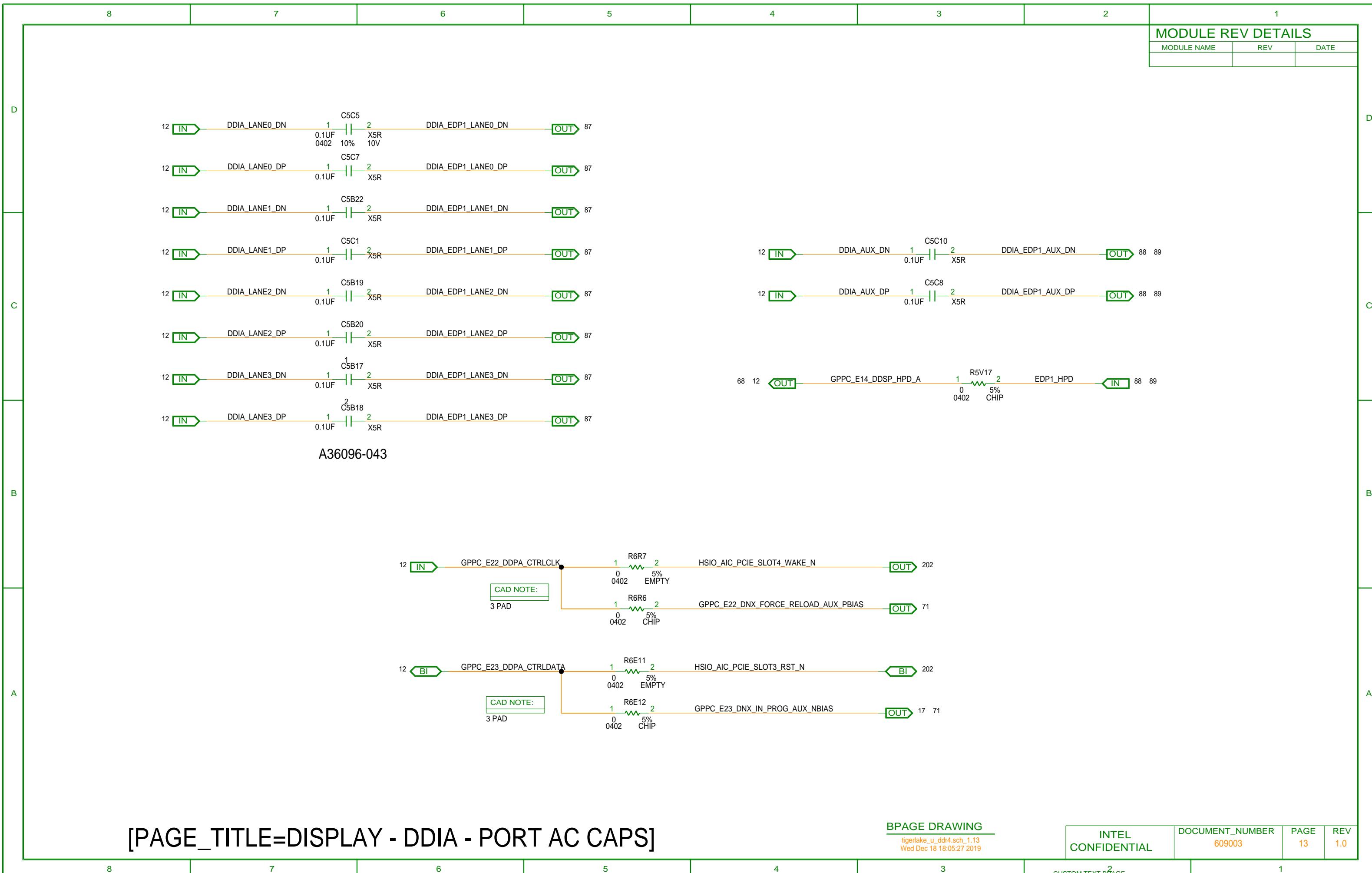
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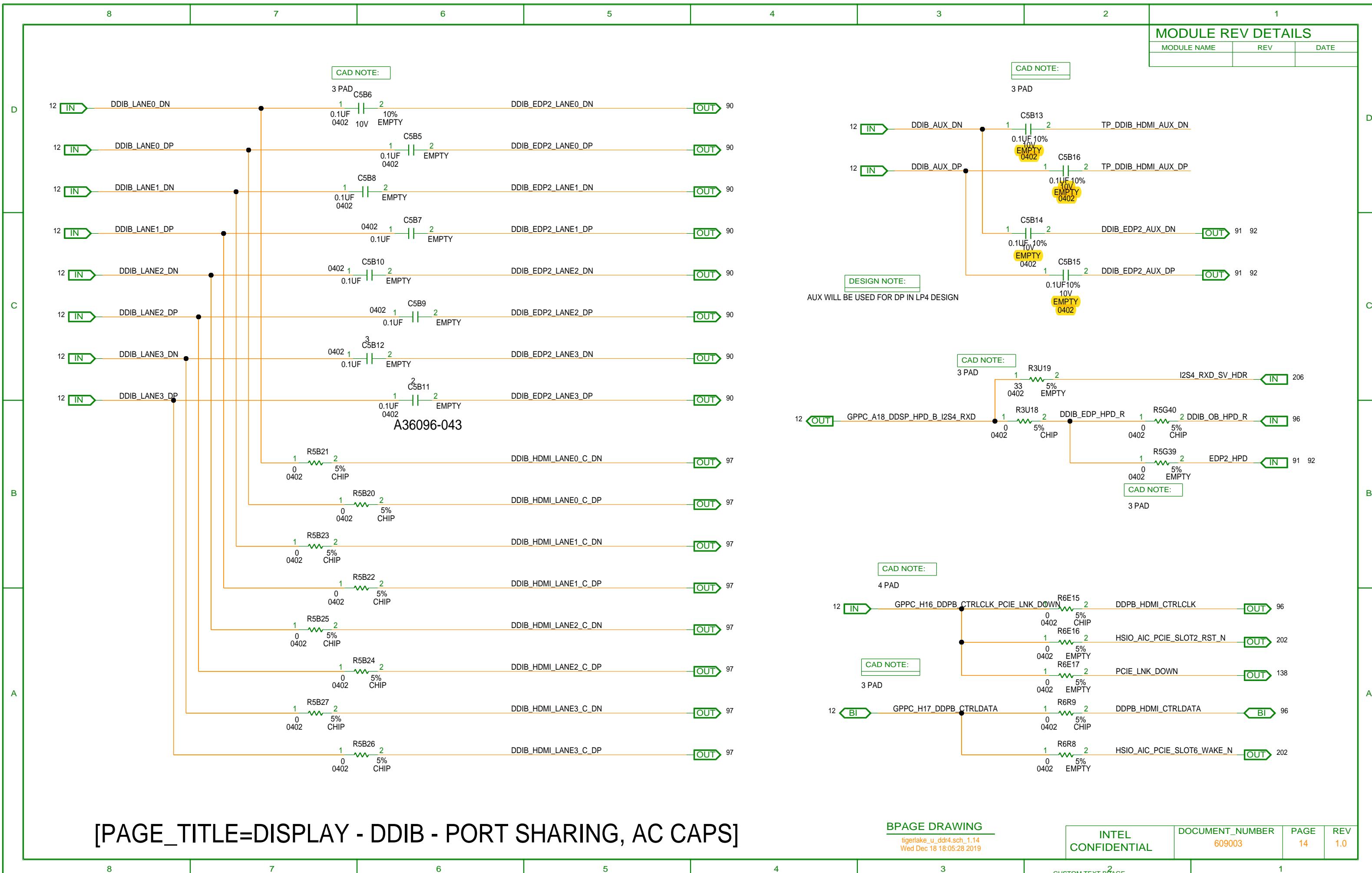
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

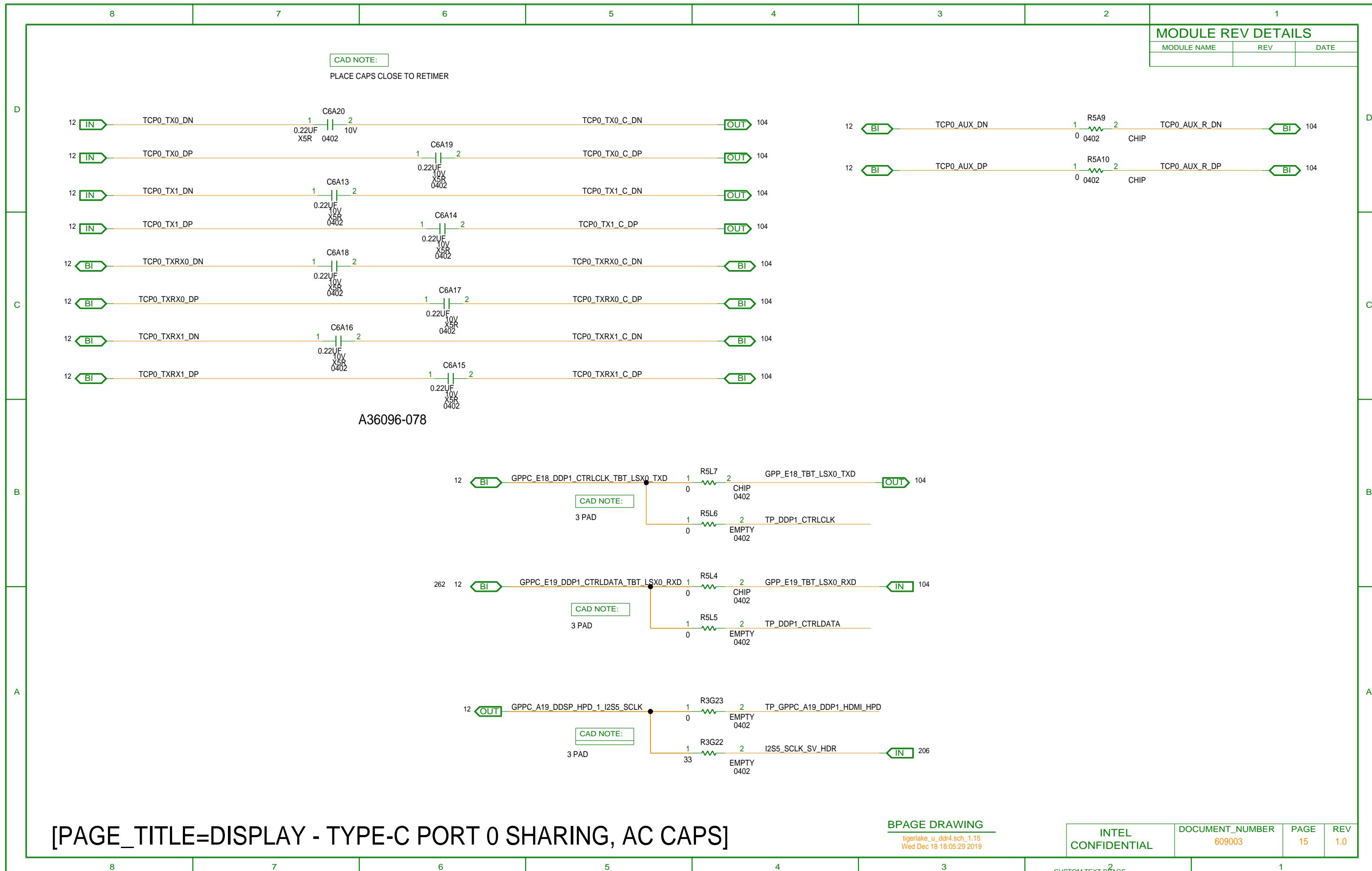
DESIGN NOTE:  
GPPC\_A17=VDDEN, GPPC\_A21=BKLT\_EN & GPPC\_A22=BKLT\_CTRLR4D17  
150  
1%  
1/16W  
CHIP  
A93548-005M8, DSI\_DE\_TE\_2, OUT, 88, 91  
1/16W1% CHIP A93548-005

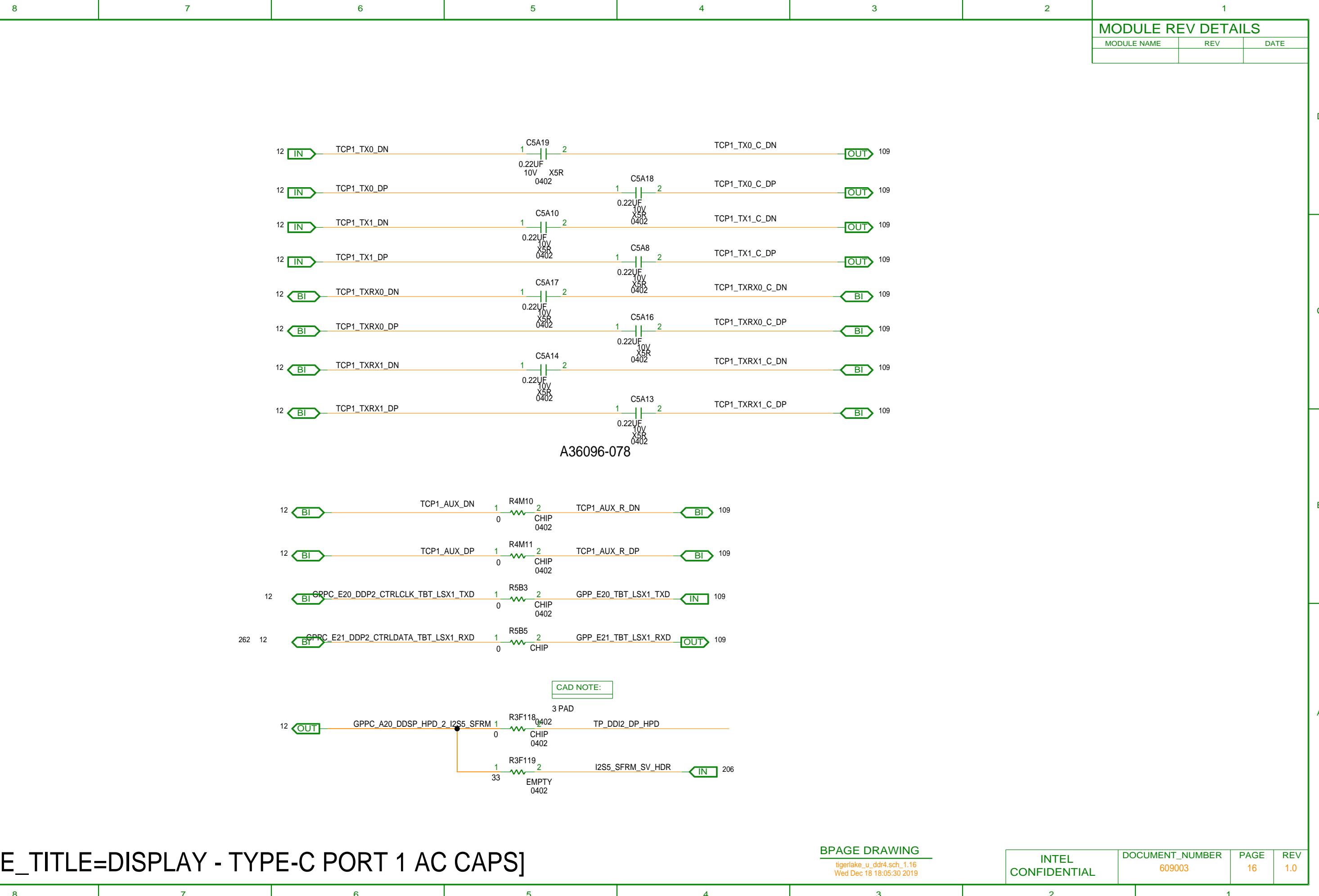
AB1, DP\_RCOMP

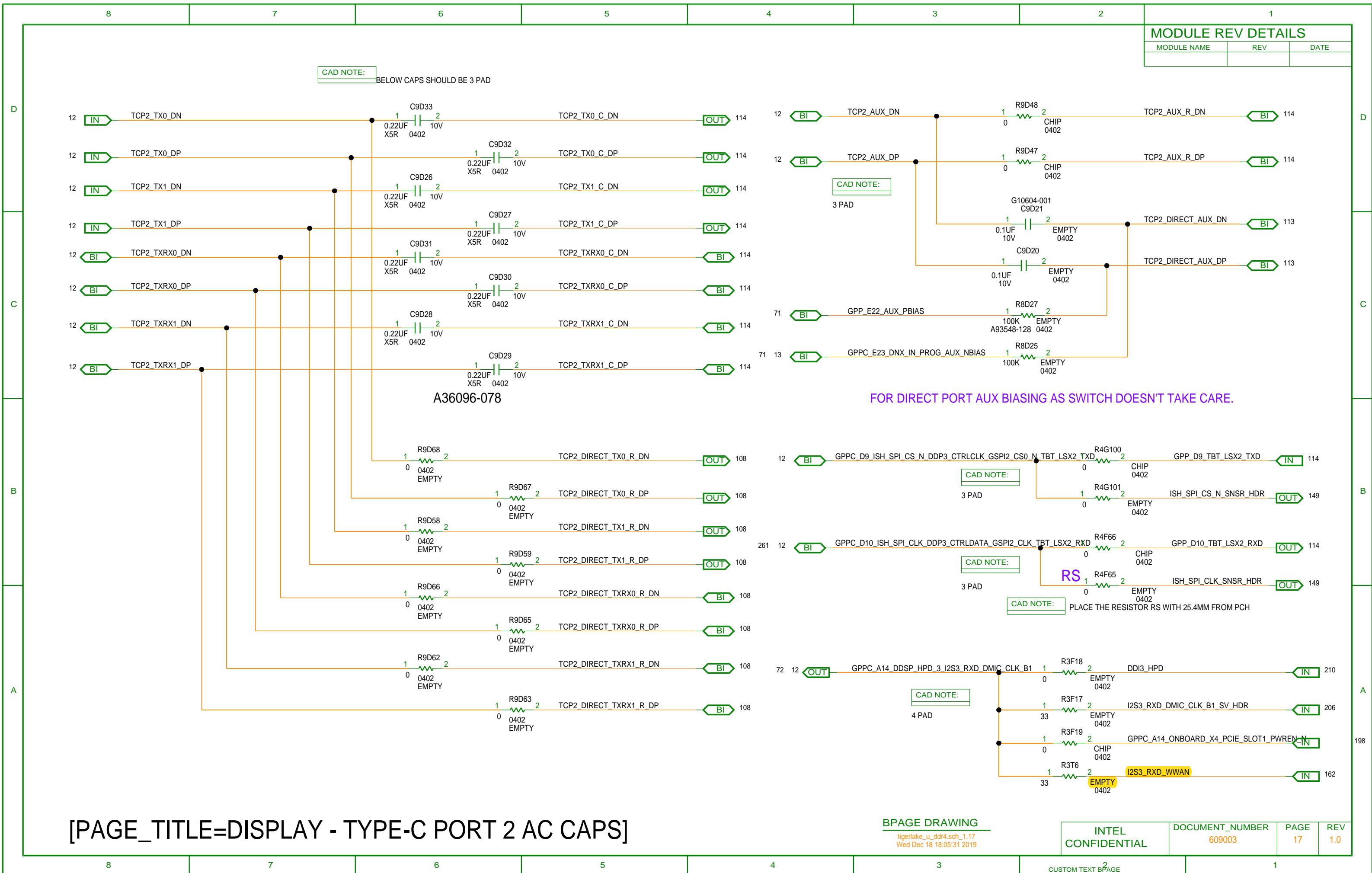
CE4, XXDISP\_UTILS, OUT, 50  
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1%  
1/16W  
CHIP  
A93548-005

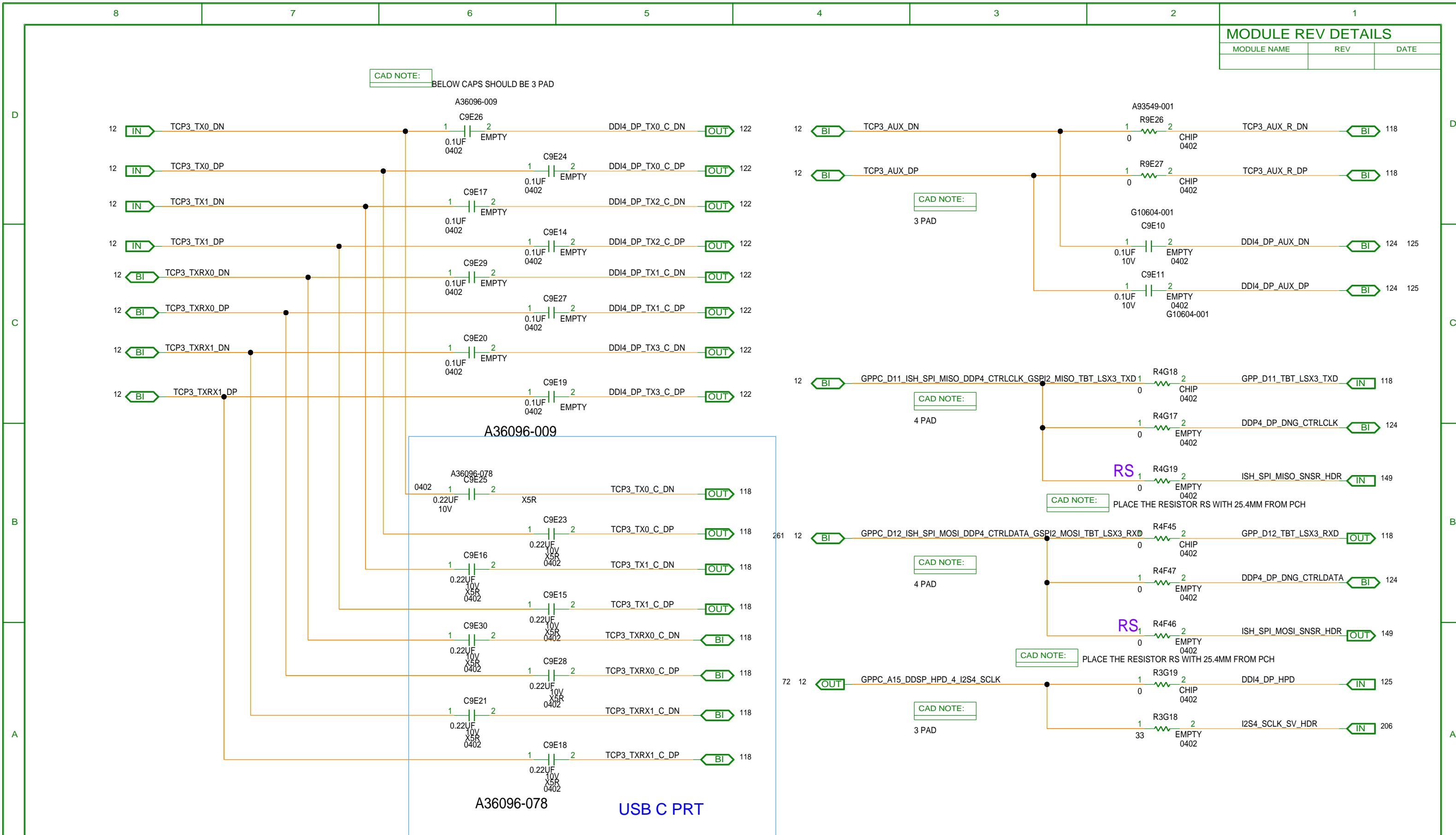


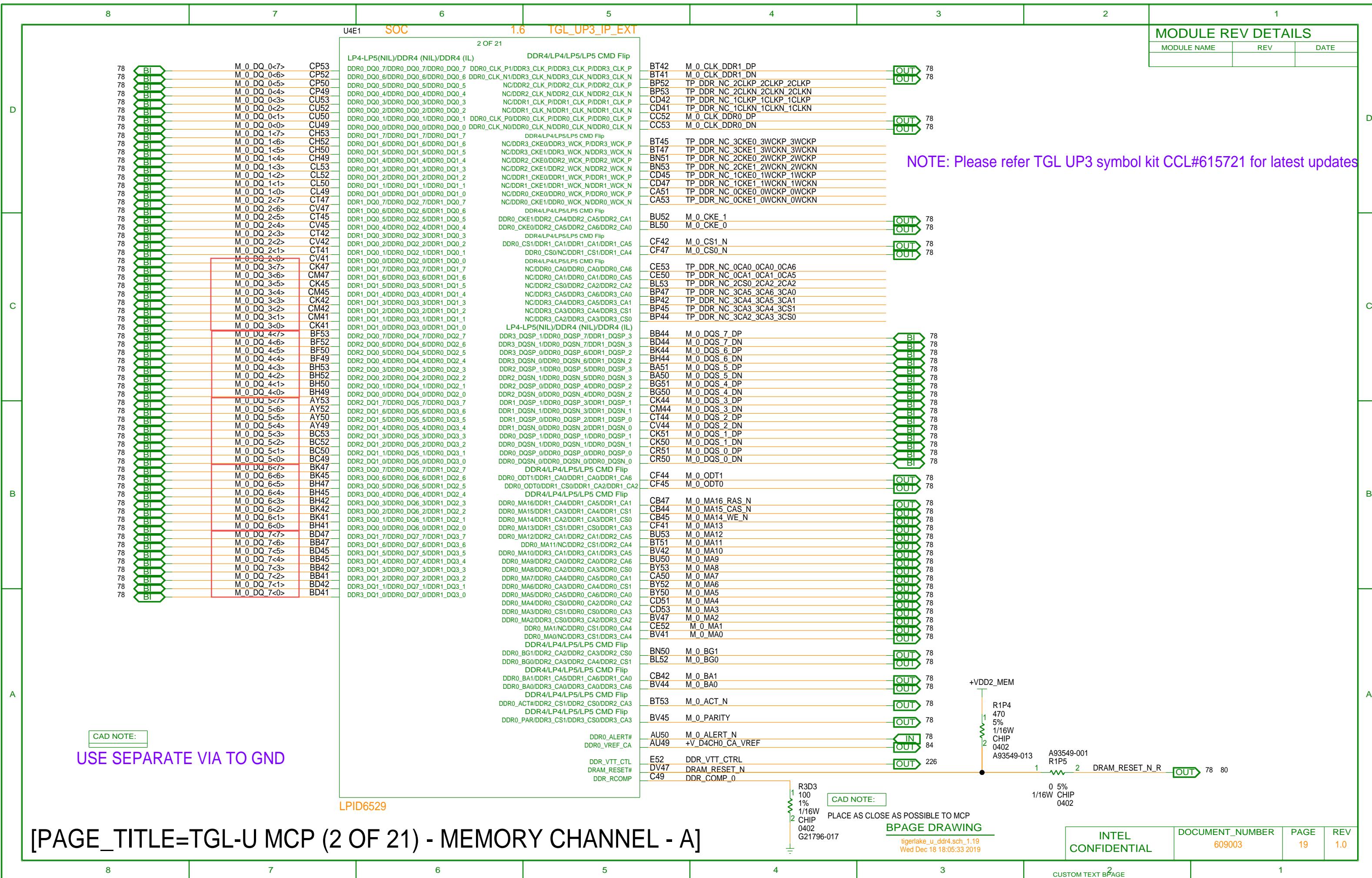


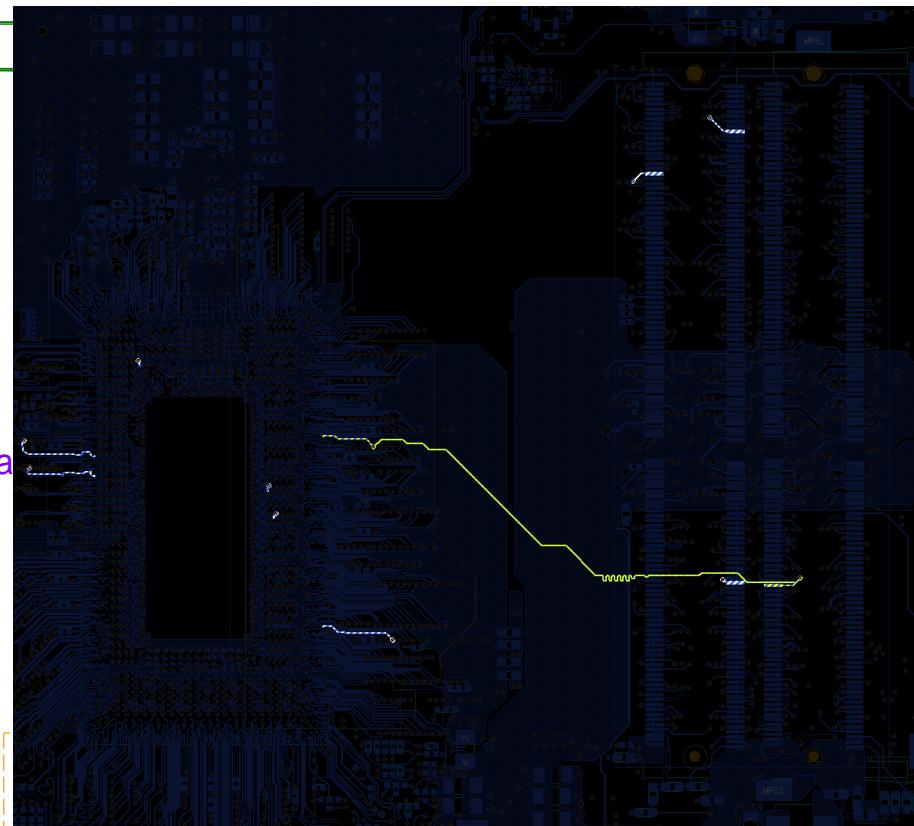
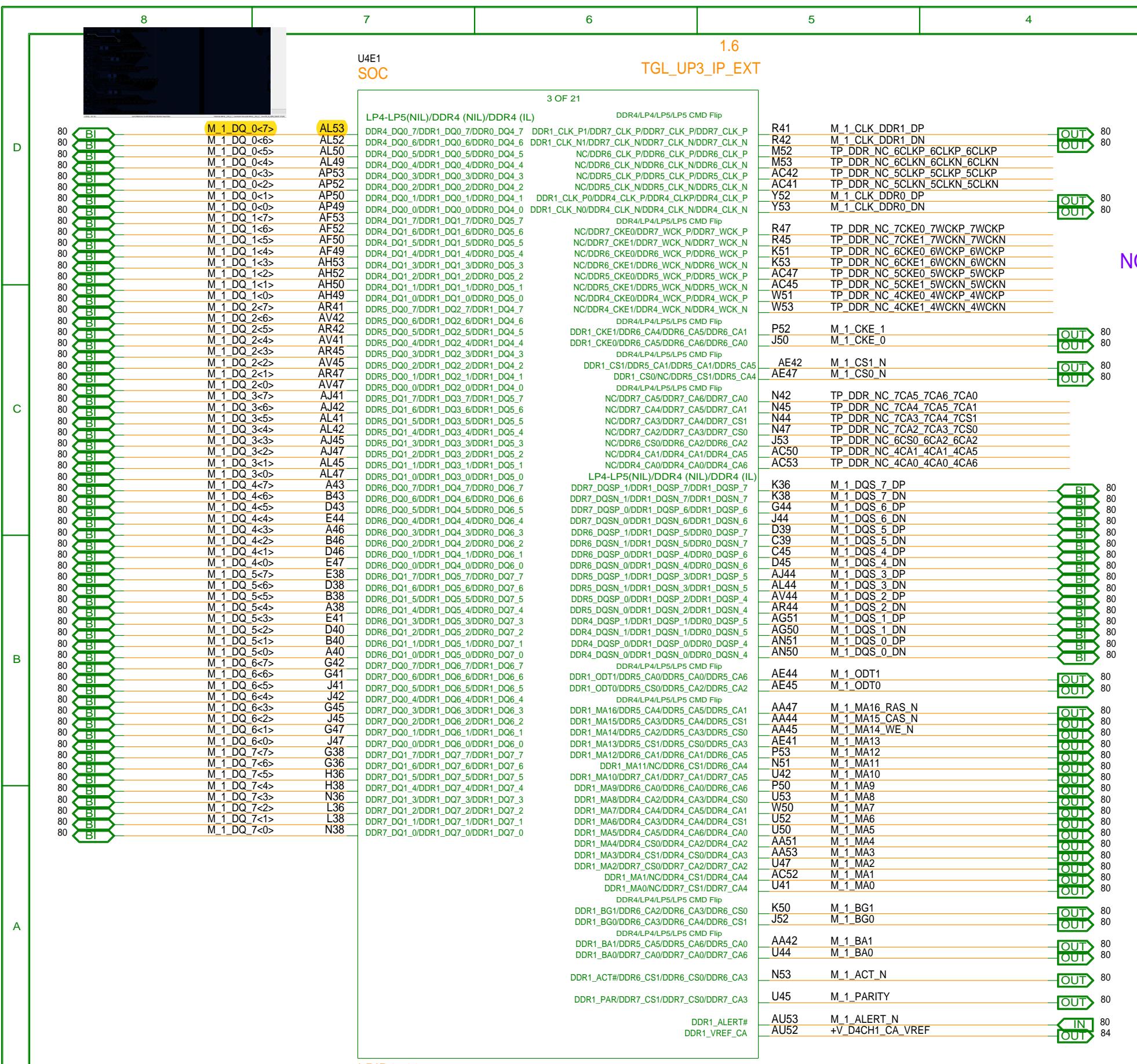






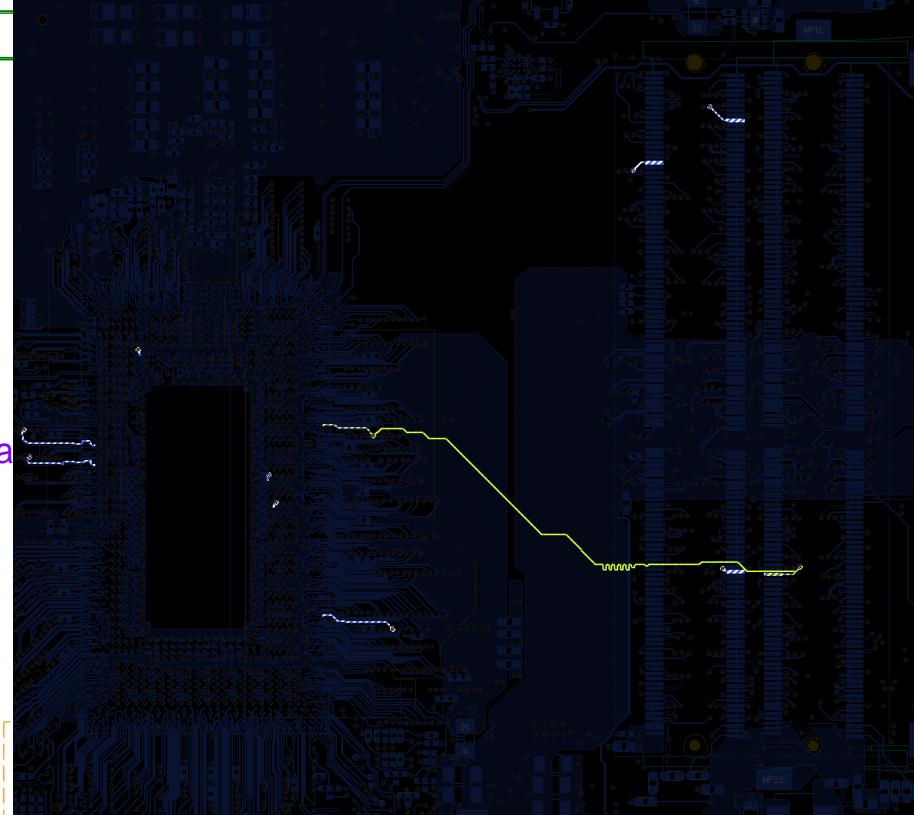




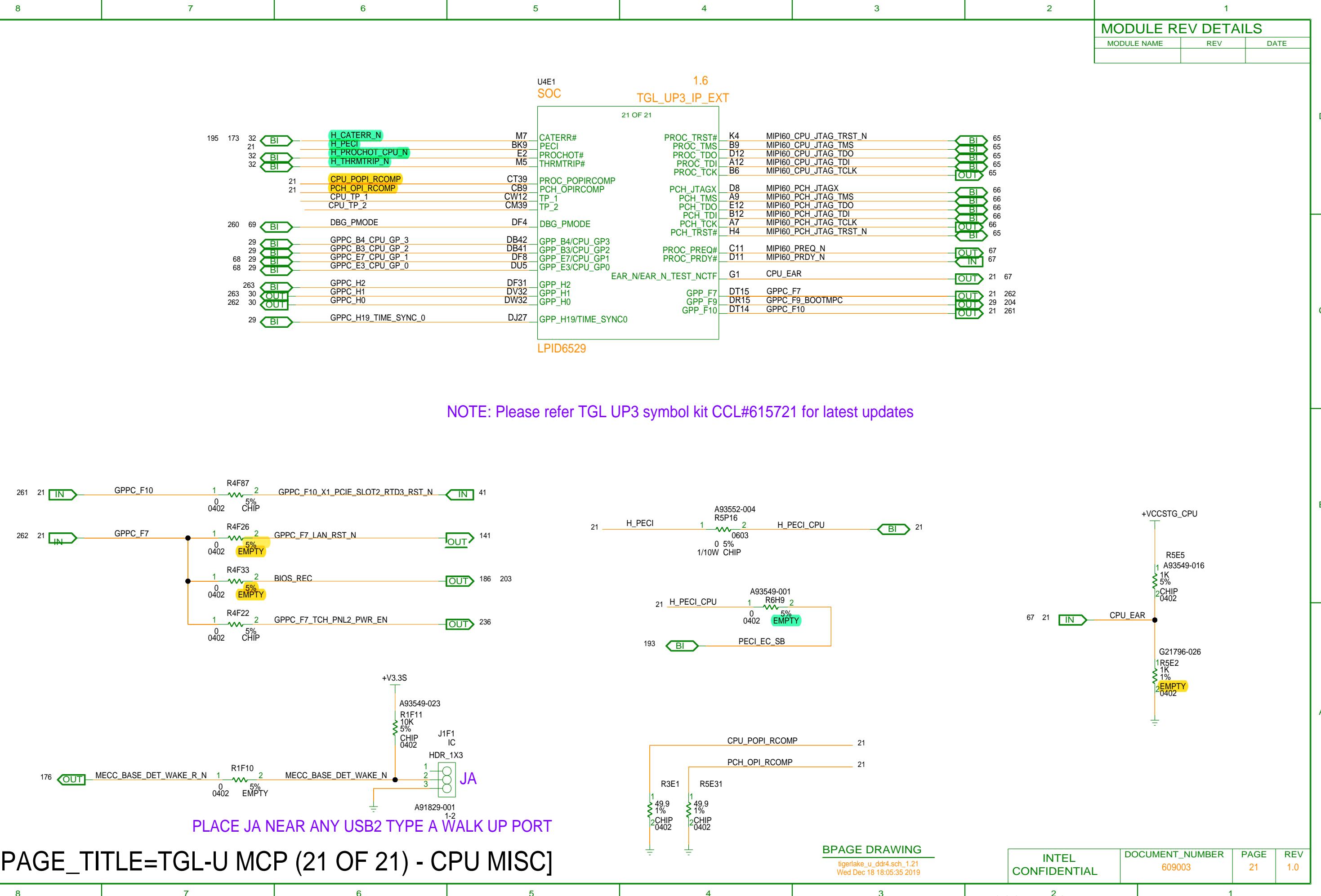


**NOTE:** Plea

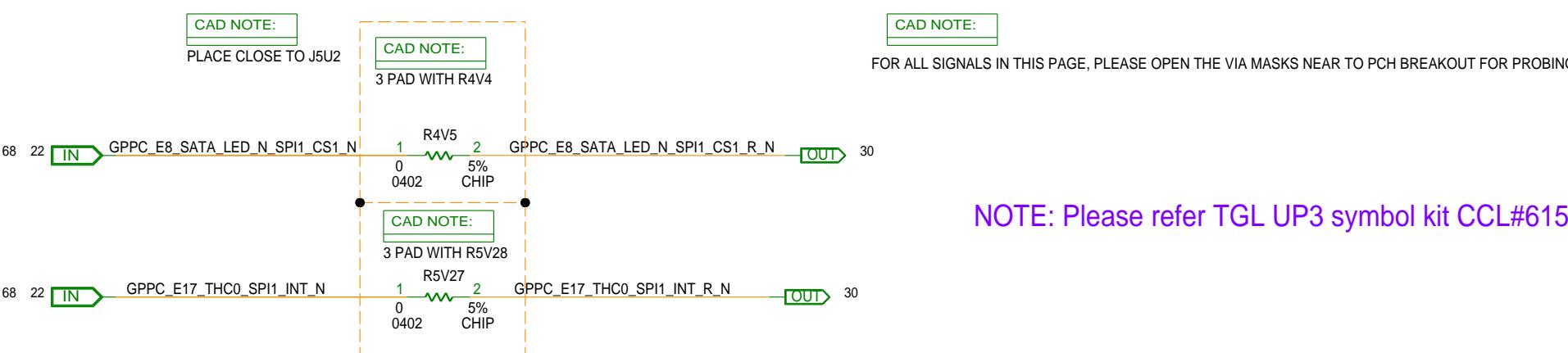
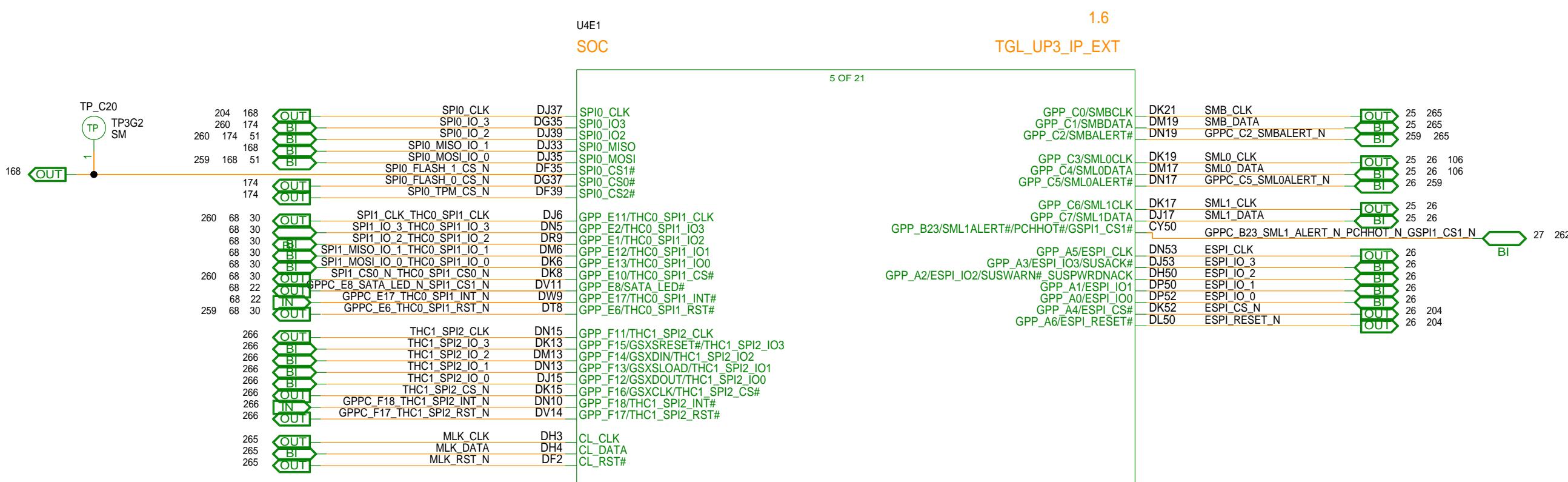
1.6 U4E1  
TGL UP3 IP EXT SOC



[PAGE TITLE=TGLU MCP (3 OF 21) - MEMORY CHANNEL - B]



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| 8                         | 7 | 6 | 5 | 4 | 3 | 2   | 1    |
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| MODULE NAME               |   |   |   |   |   | REV | DATE |

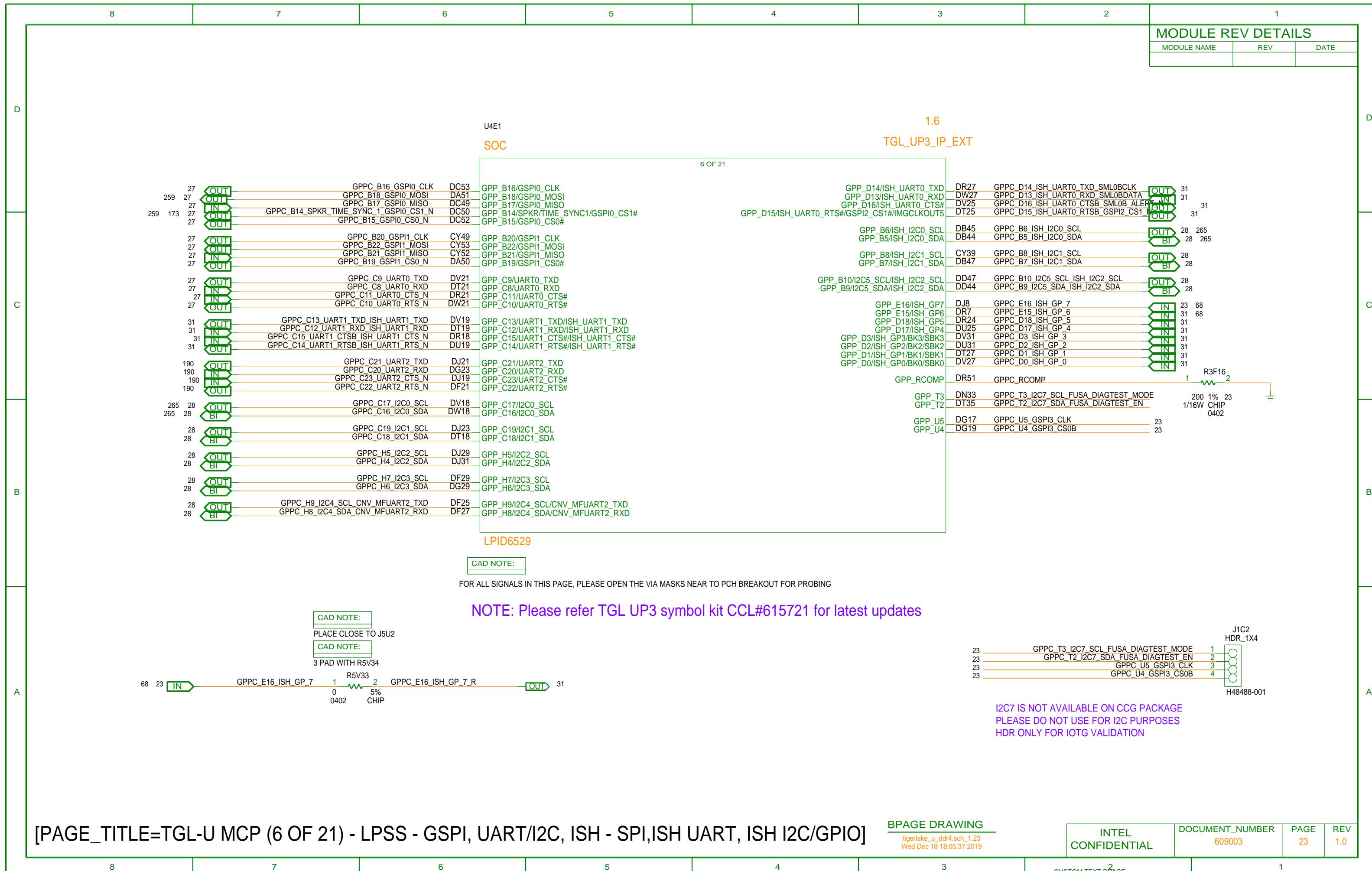


[PAGE\_TITLE=TGL-U MCP (5 OF 21) - LSIO - SPI, ESPI, THC, MLINK, SMLINK, SMBUS]

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tigerlake\_u\_ddr4.sch\_1.22  
Wed Dec 18 18:05:36 2019

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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>22 | REV<br>1.0 |
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| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

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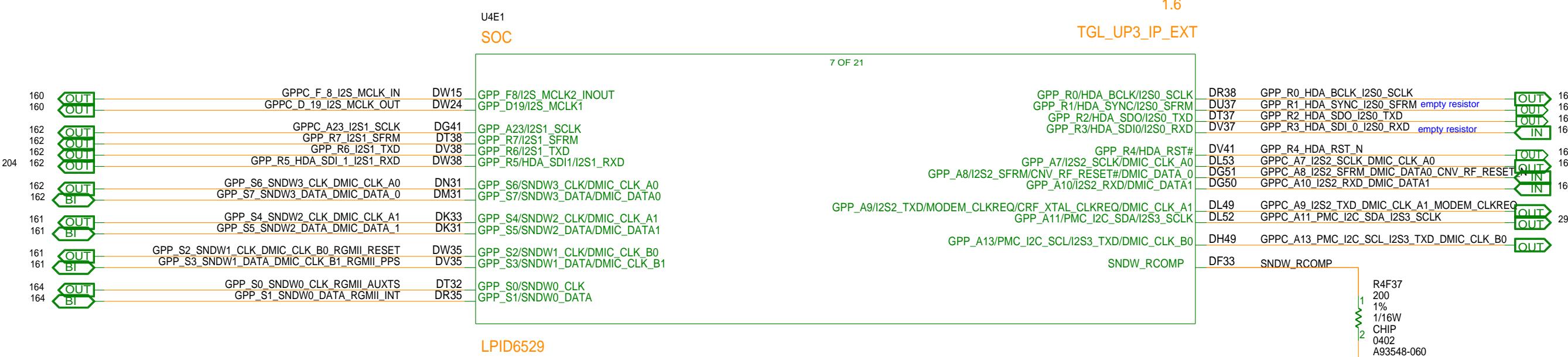
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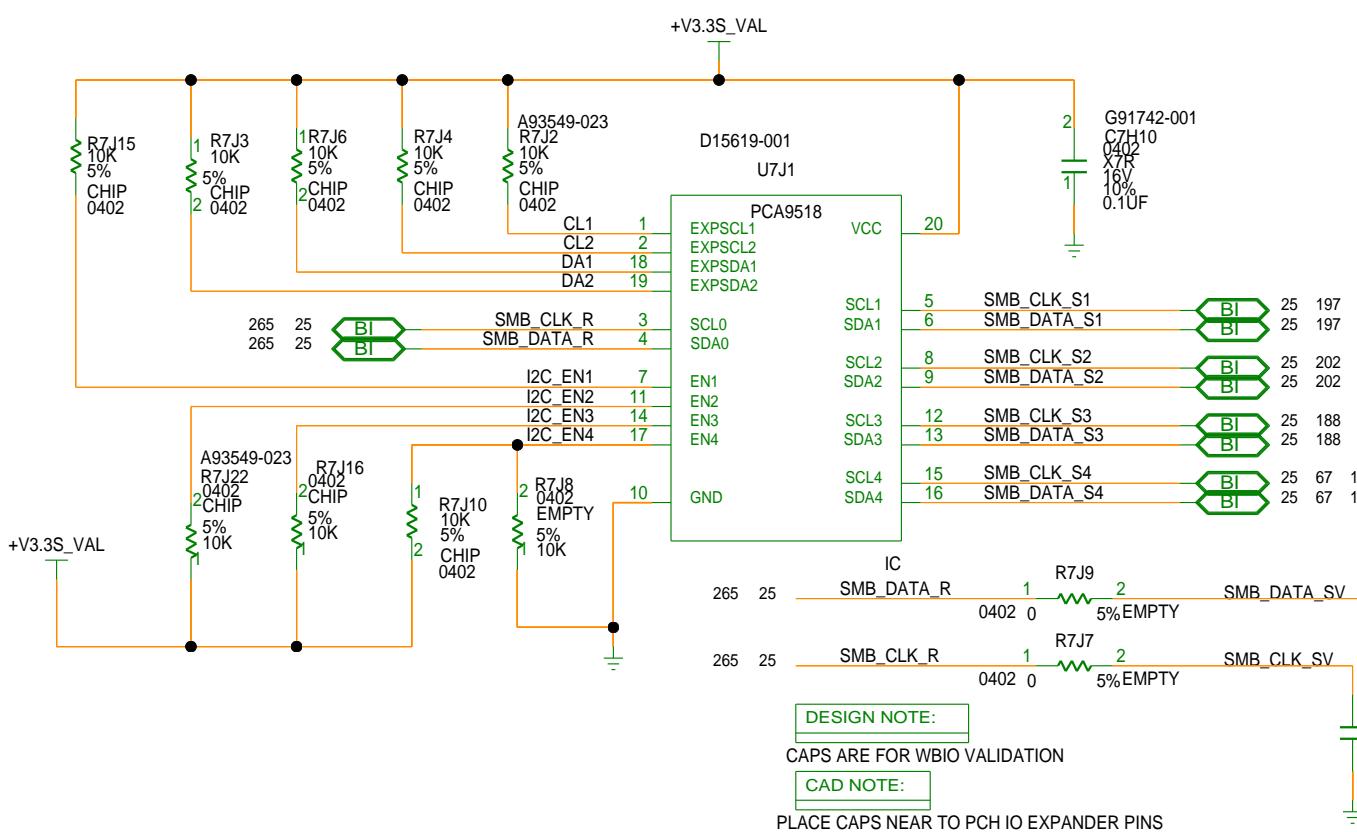


NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

# PCH SMBUS IO EXPANDER

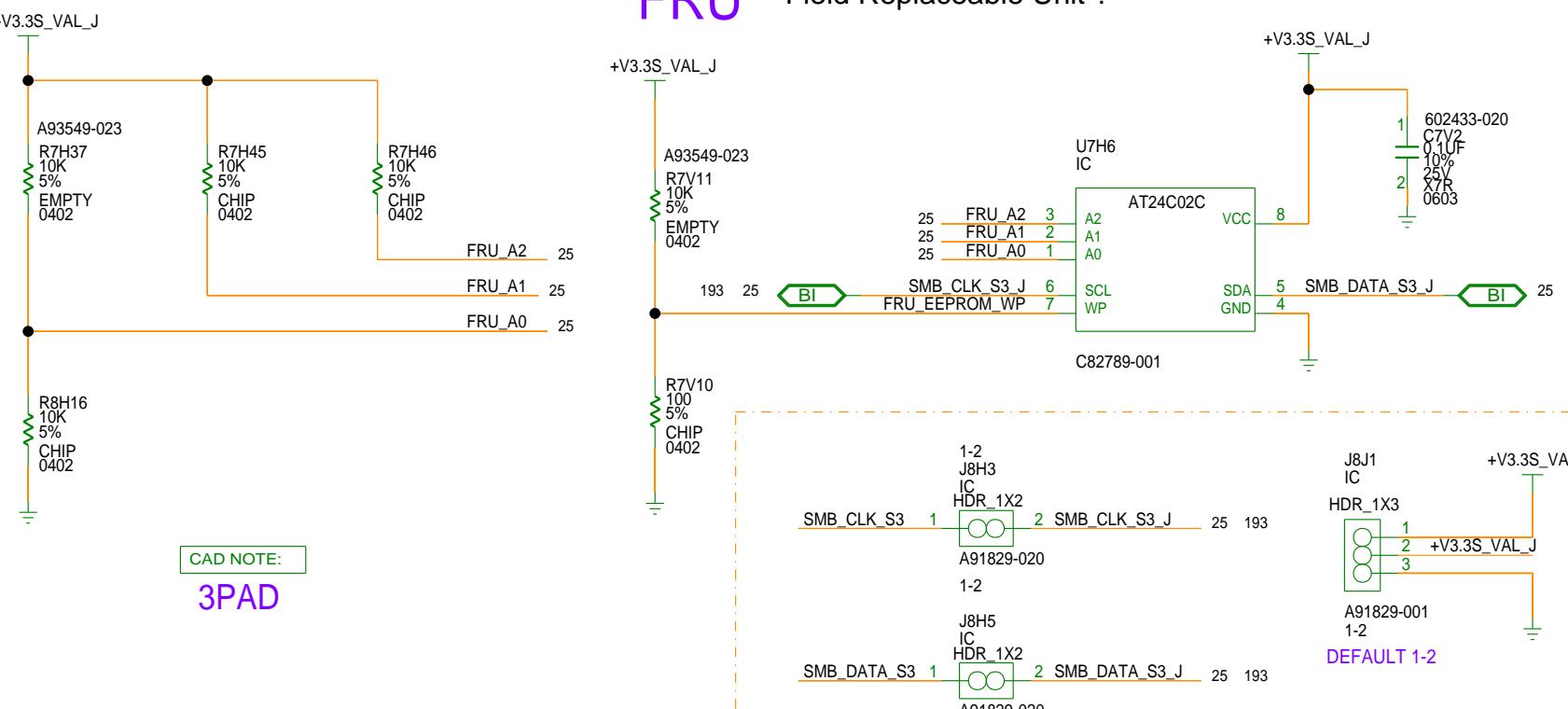
## SMBUS AND SMLINK PULL UPS

| MODULE REV DETAILS |             |     |      |
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|                    |             |     |      |



FRU

Field Replaceable Unit ?

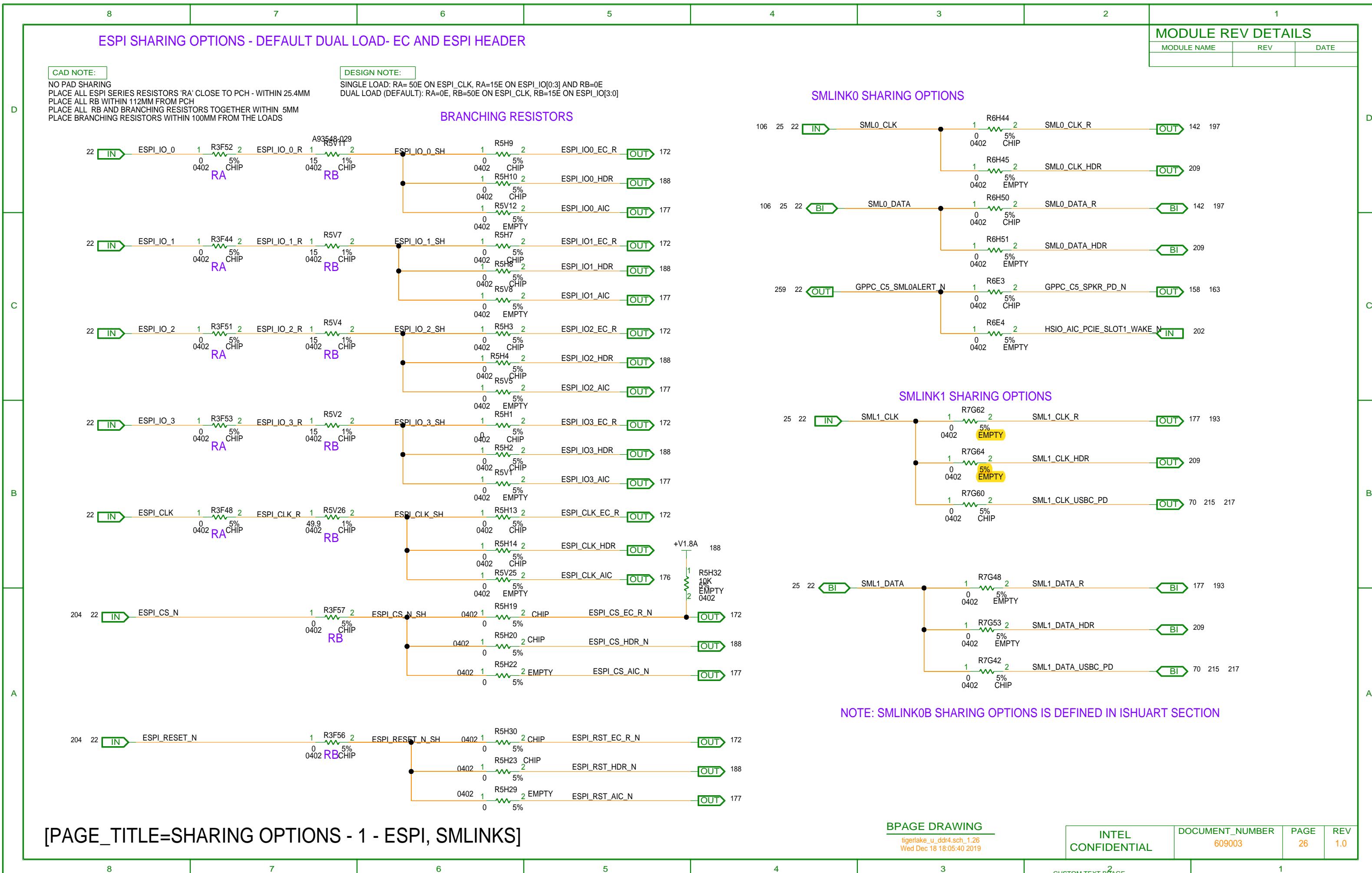


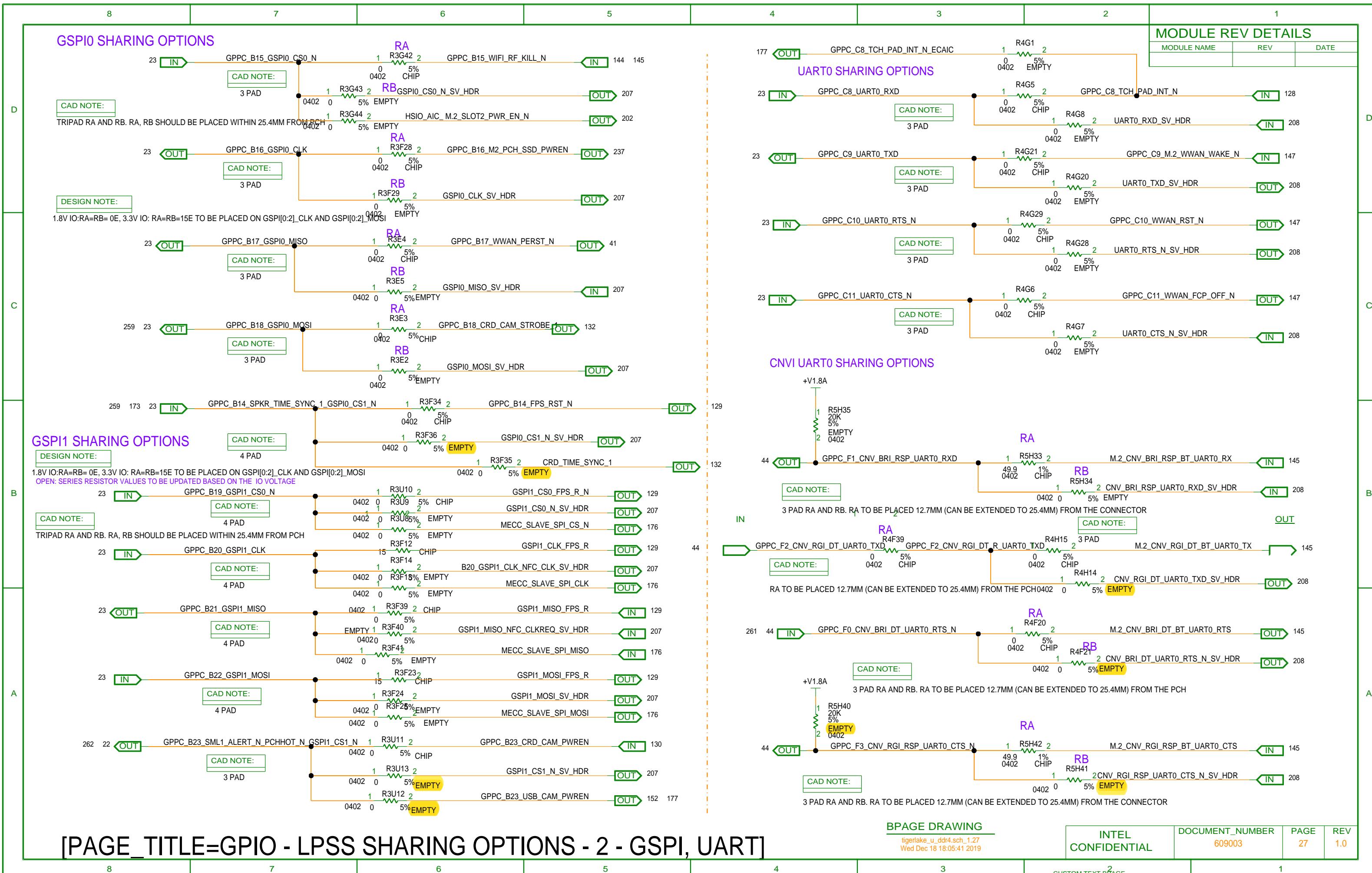
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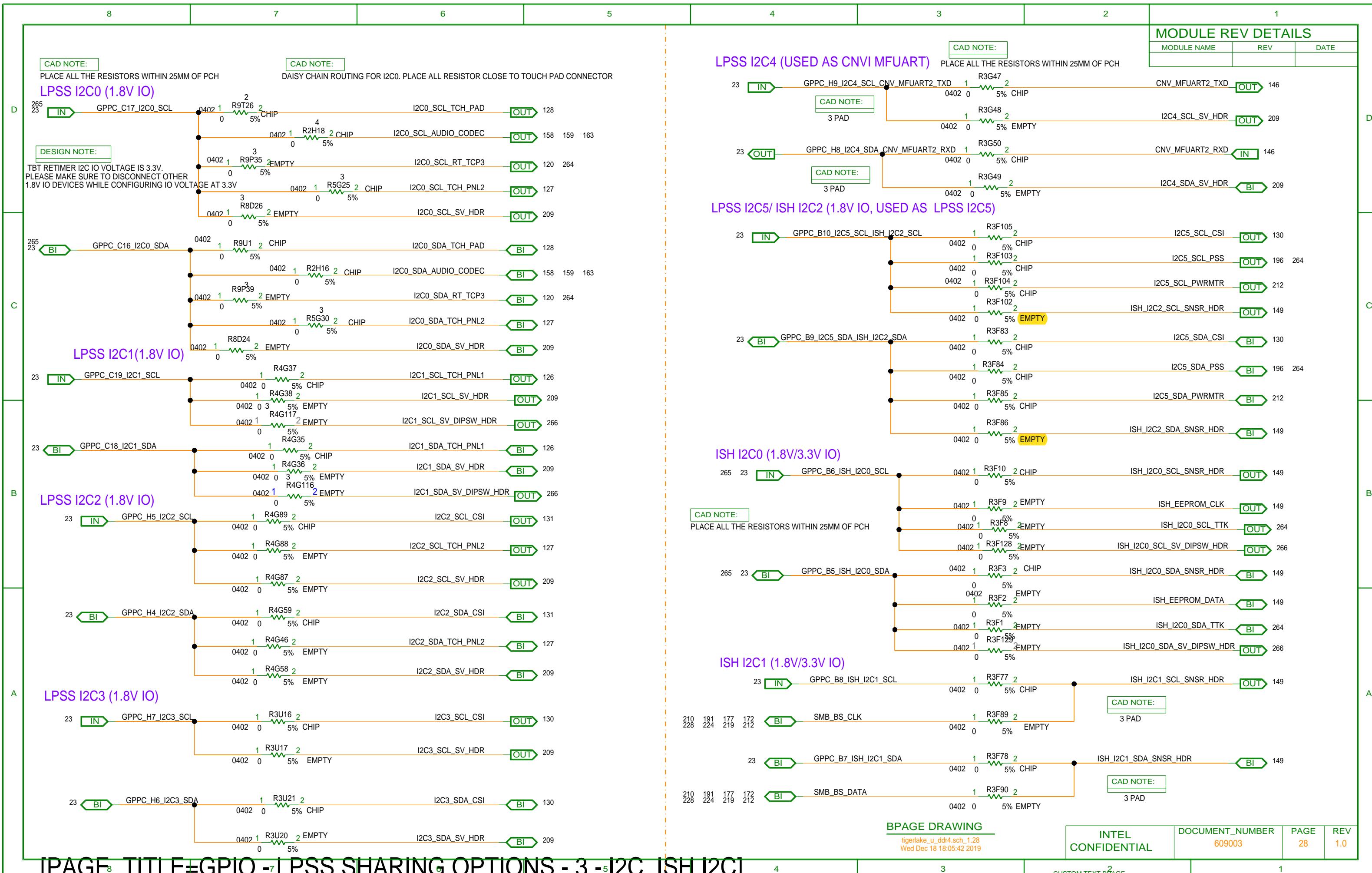
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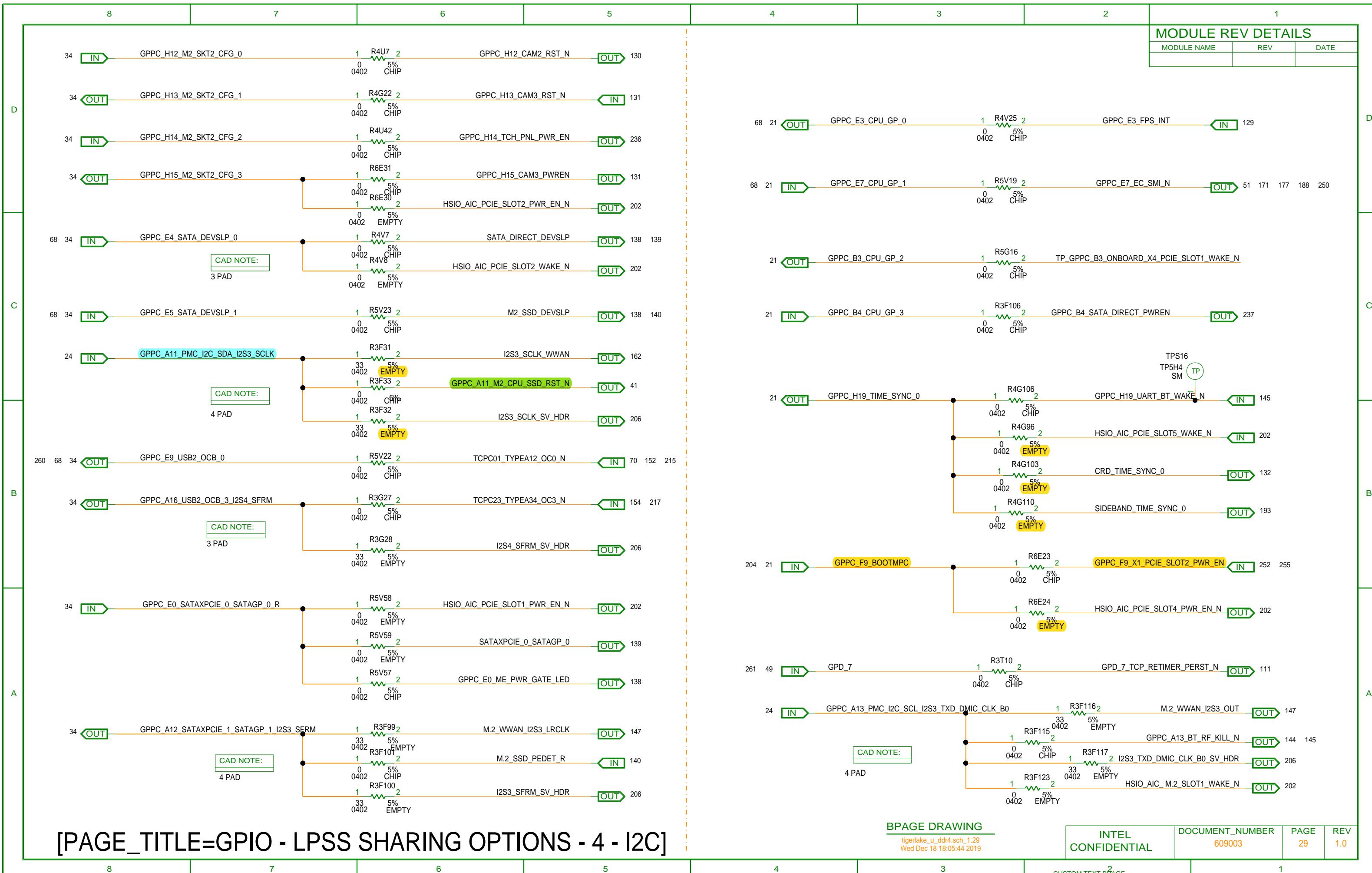
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Wed Dec 18 18:05:39 2019

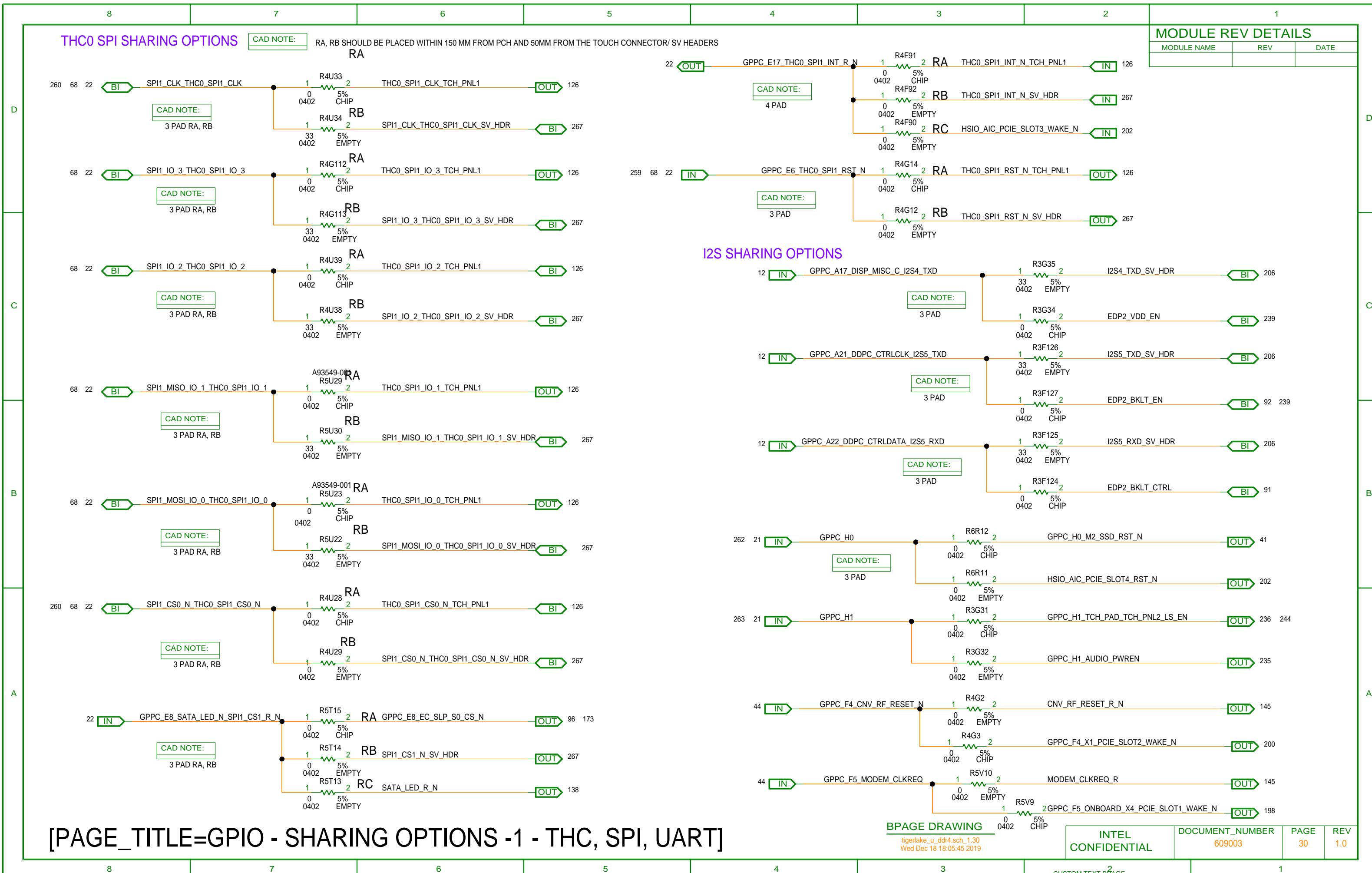
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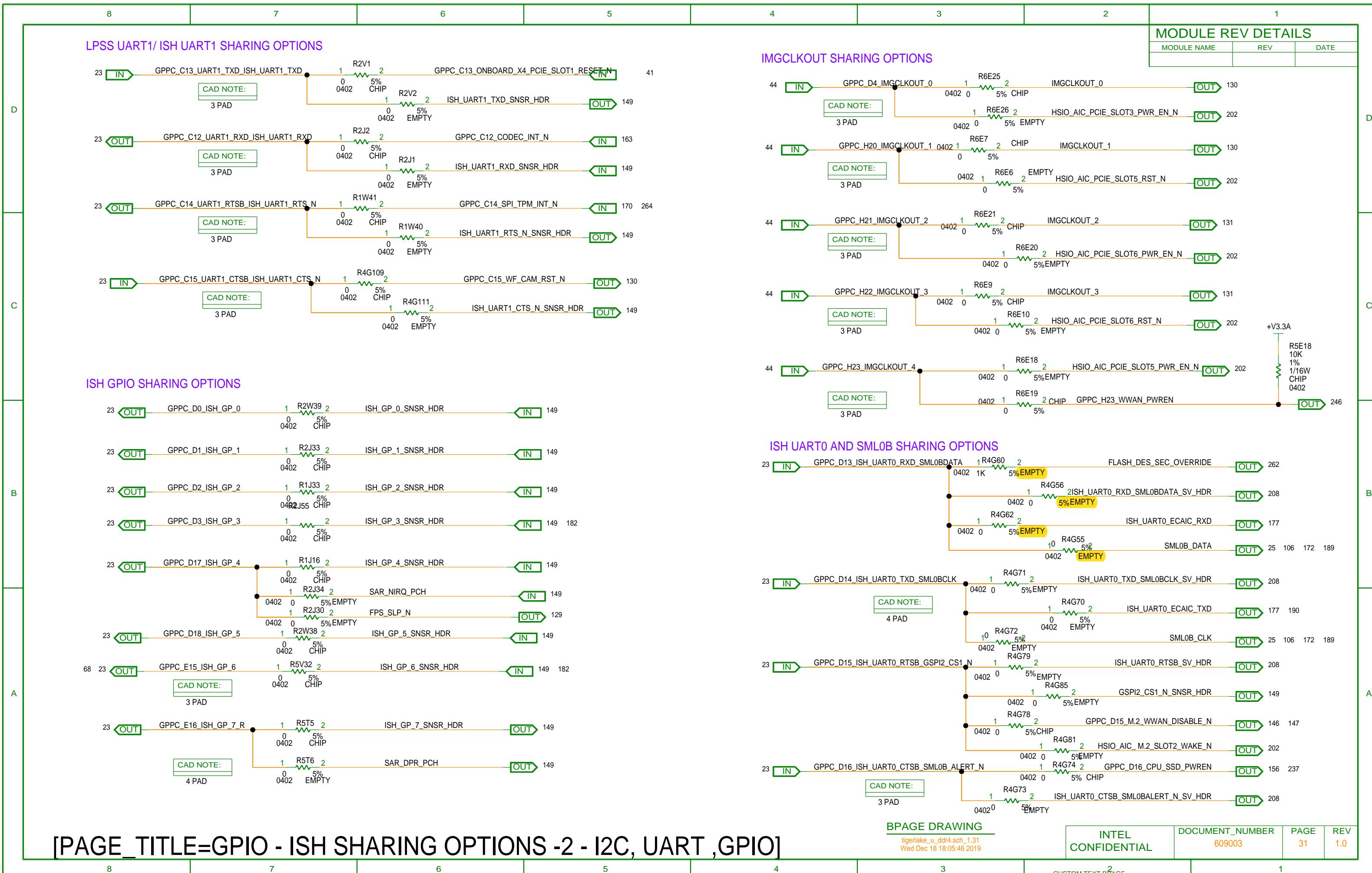






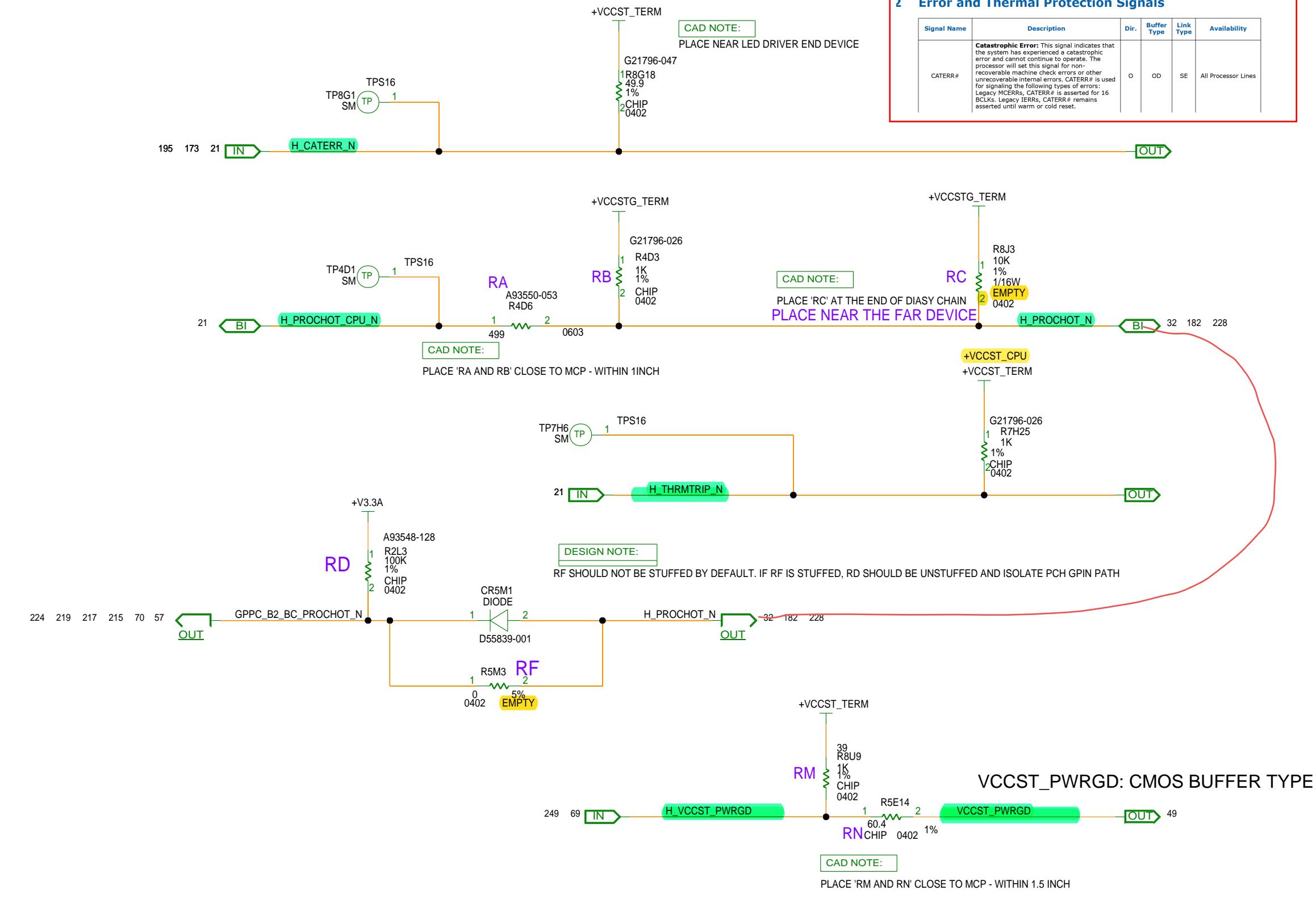






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# CPU SIDEBAND SIGNALS

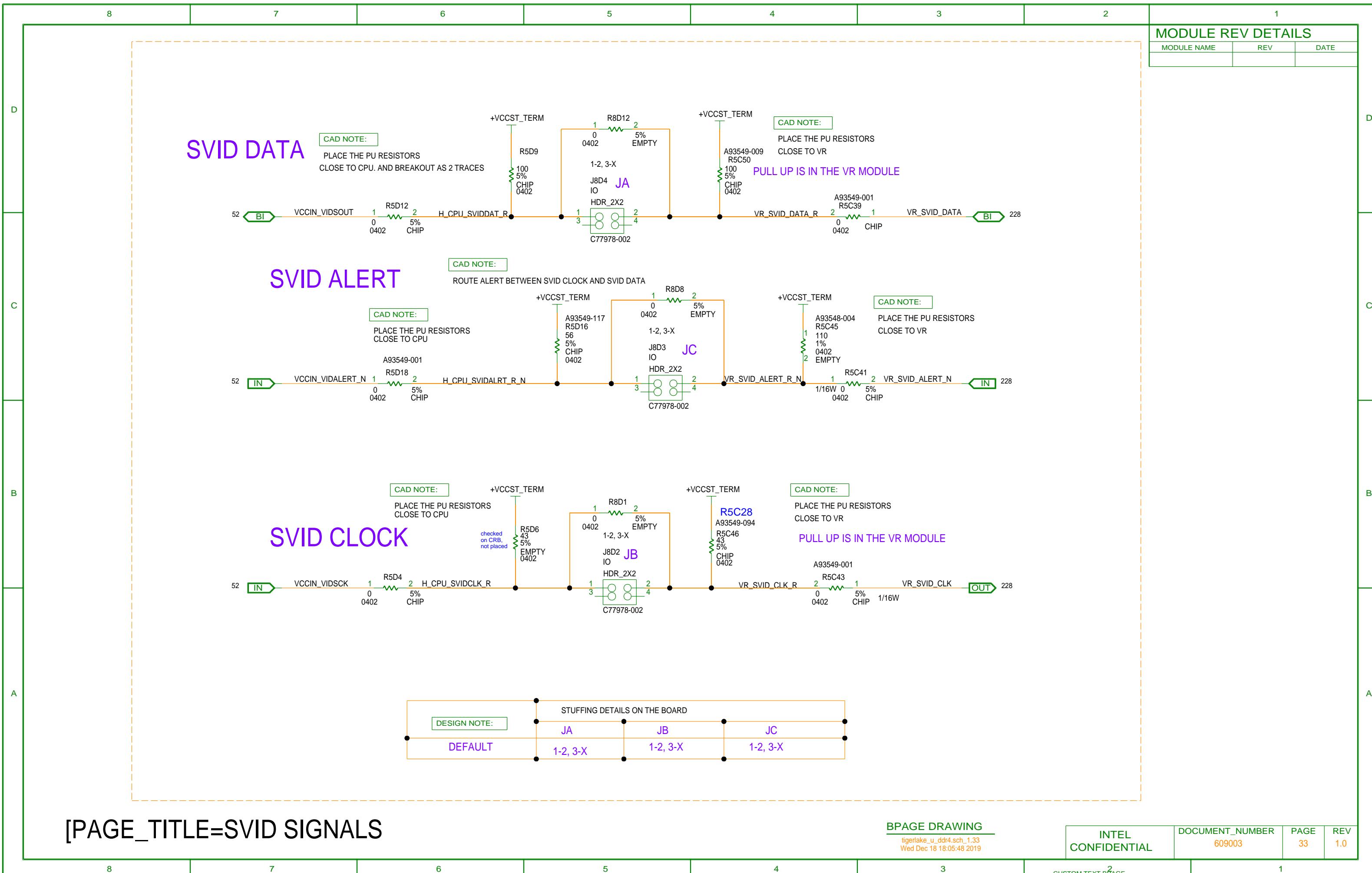


[PAGE\_TITLE=GPIO - OTHER PCH GPIO SHARING OPTIONS - 1]

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Wed Dec 18 18:05:47 2019

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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>32 | REV<br>1.0 |
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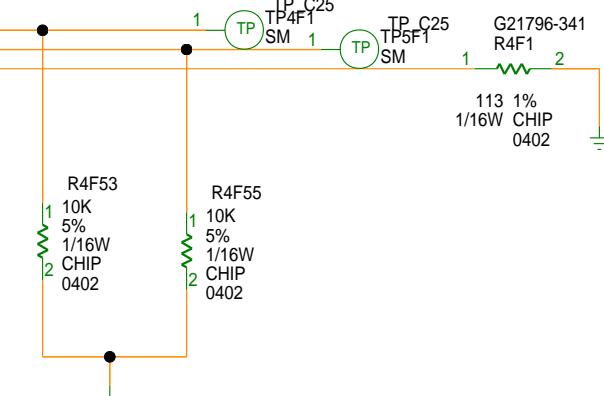
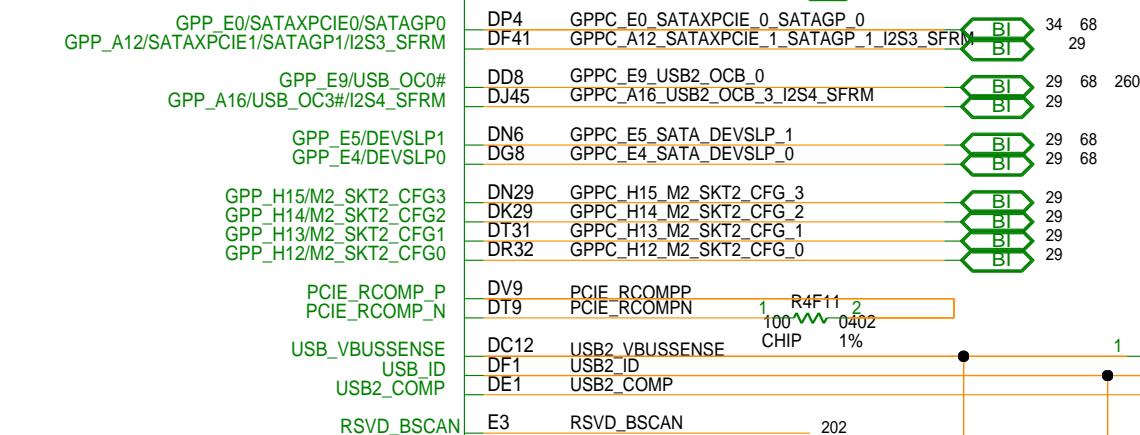
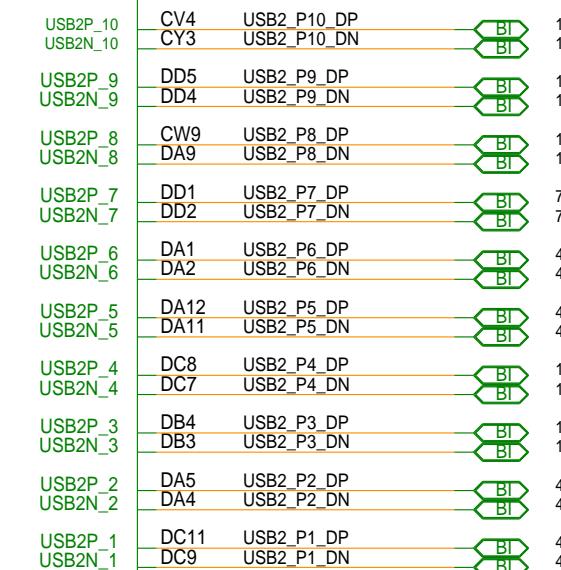
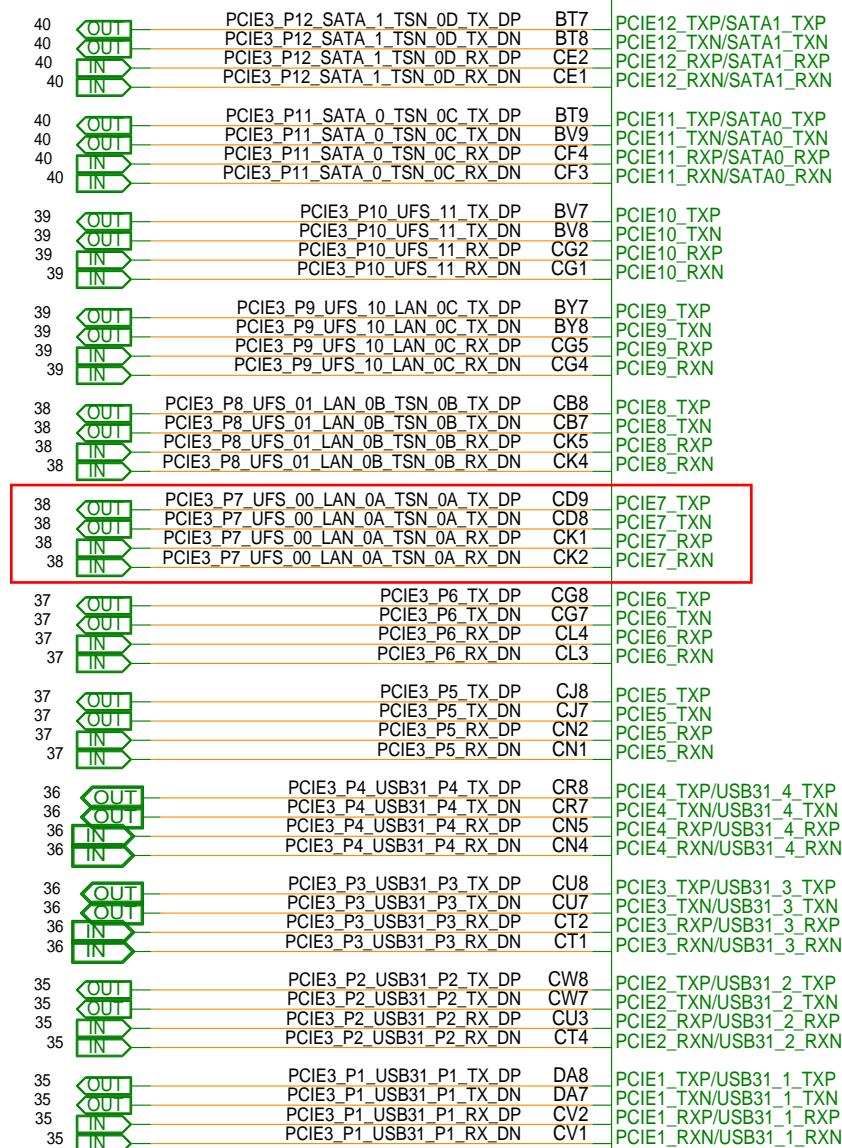
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**MODULE REV DETAILS**

| MODULE NAME | REV | DATE |
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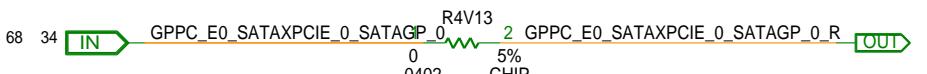
U4E1  
SOC  
1.6  
TGL\_UP3\_IP\_EXT

9 OF 21



LPID6529

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates



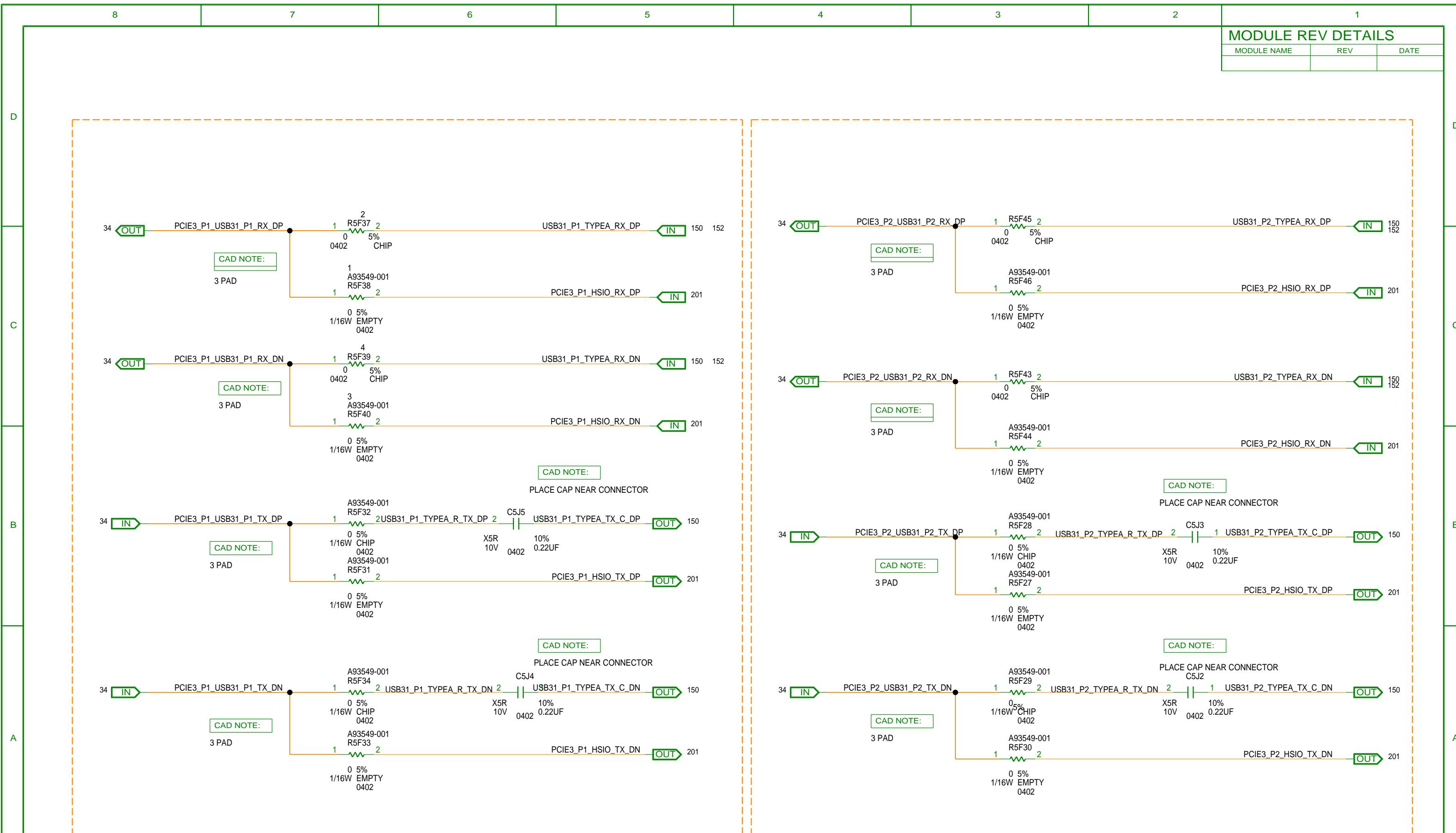
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Wed Dec 18 18:05:49 2019

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| 609003                | 34              | 1.0  |     |

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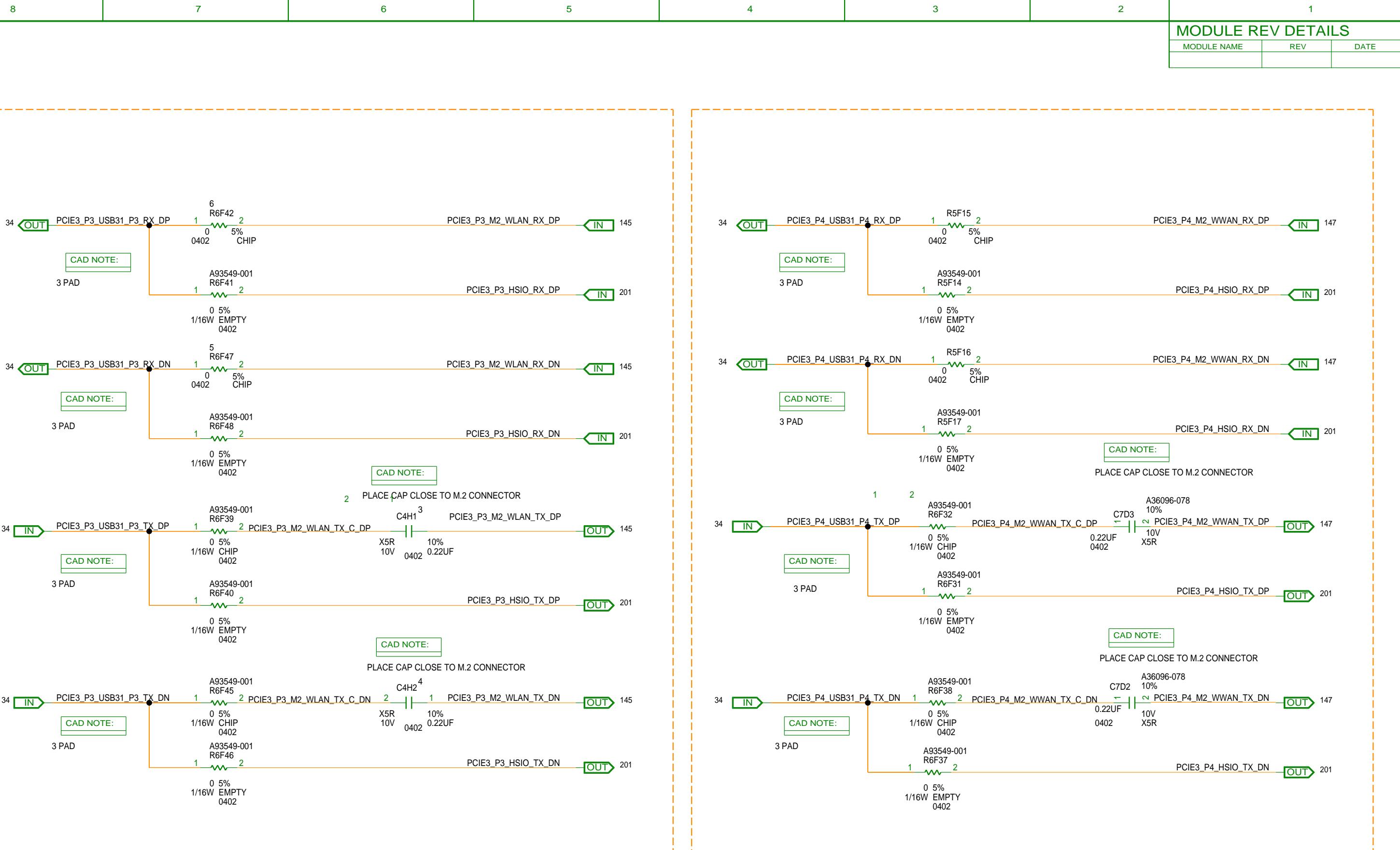
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[PAGE\_TITLE=PCIE PORT 1&2 SHARING OPTIONS, AC CAPS]

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Wed Dec 18 18:05:50 2019

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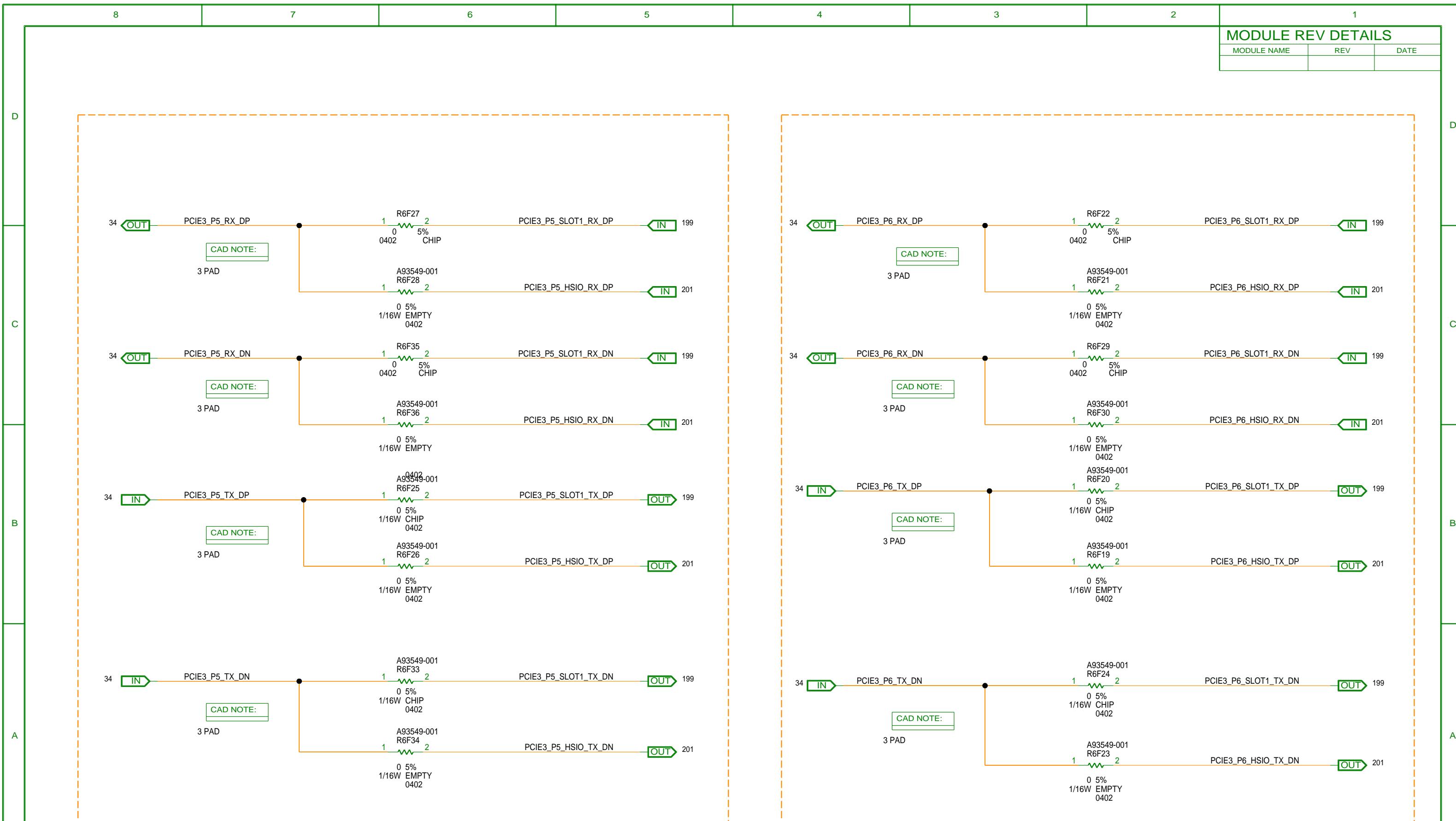


[PAGE\_TITLE=PCIE PORT 3&4 SHARING OPTIONS, AC CAPS]

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Wed Dec 18 18:05:51 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>36 | REV<br>1.0 |
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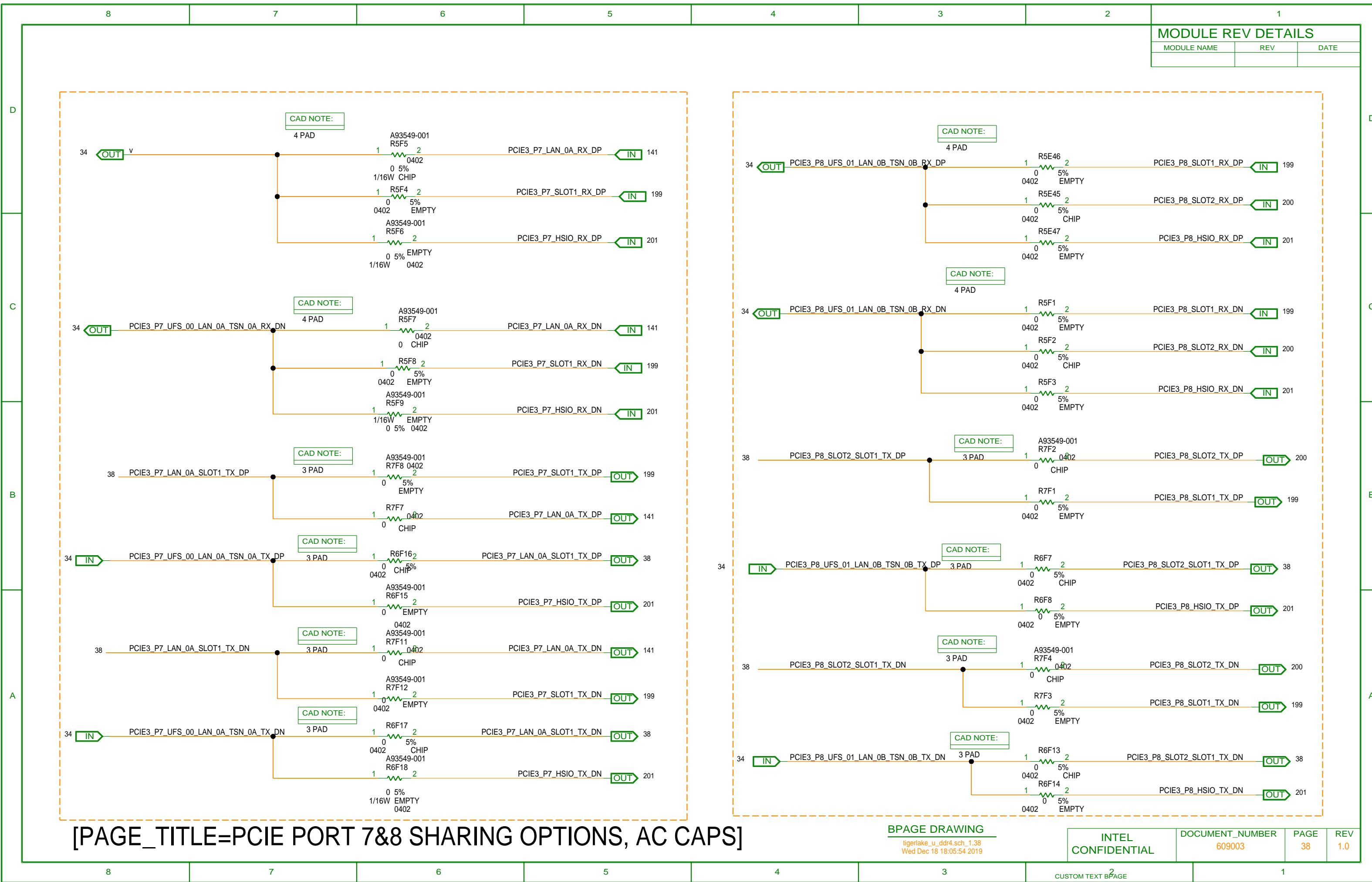
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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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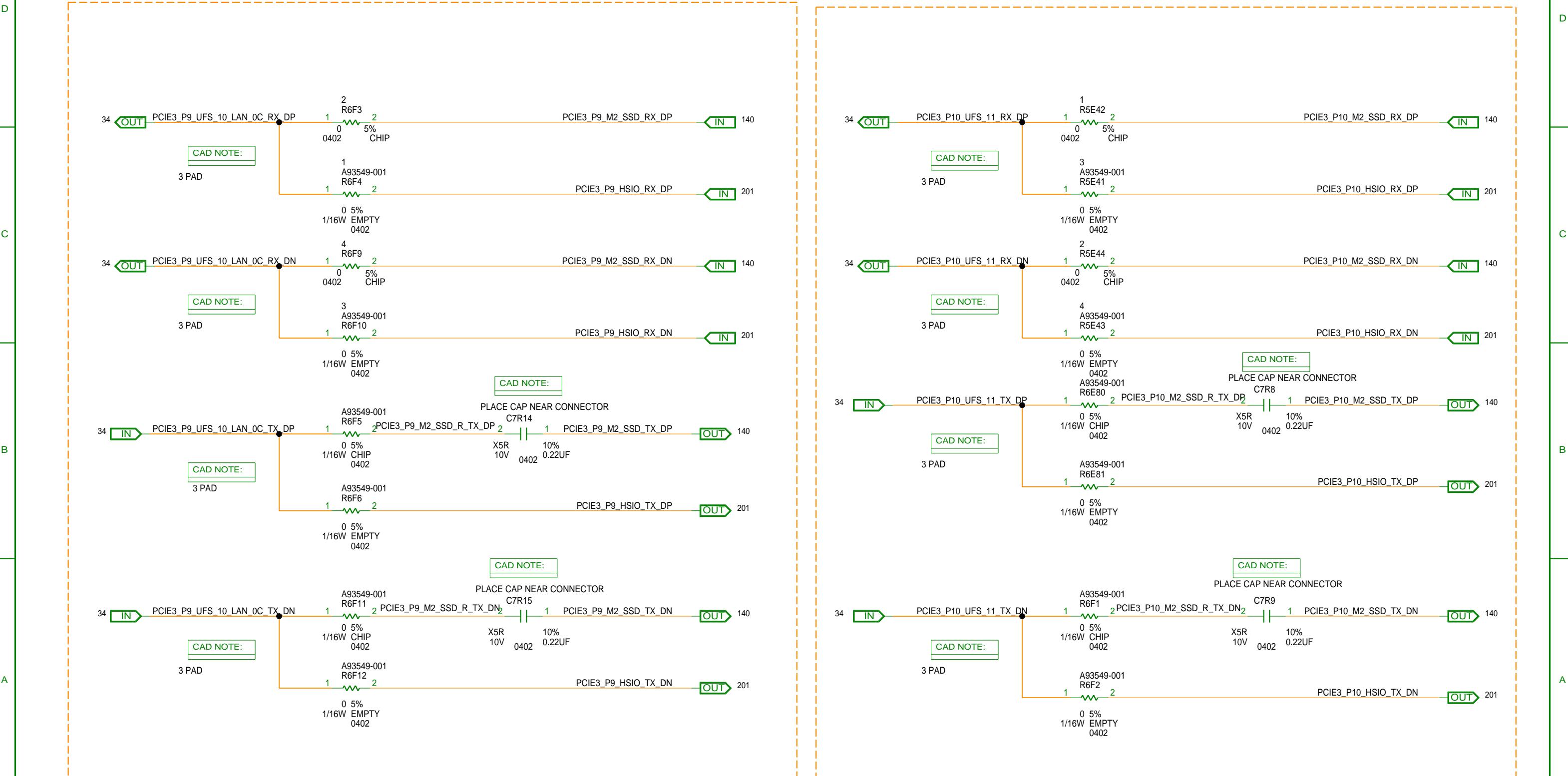
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Wed Dec 18 18:05:52 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>37 | REV<br>1.0 |
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| CUSTOM TEXT<br>2 PAGE |                           |            |            |



| 8                  | 7   | 6    | 5 | 4 | 3 | 2 | 1 |
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| MODULE REV DETAILS |     |      |   |   |   |   |   |
| MODULE NAME        | REV | DATE |   |   |   |   |   |
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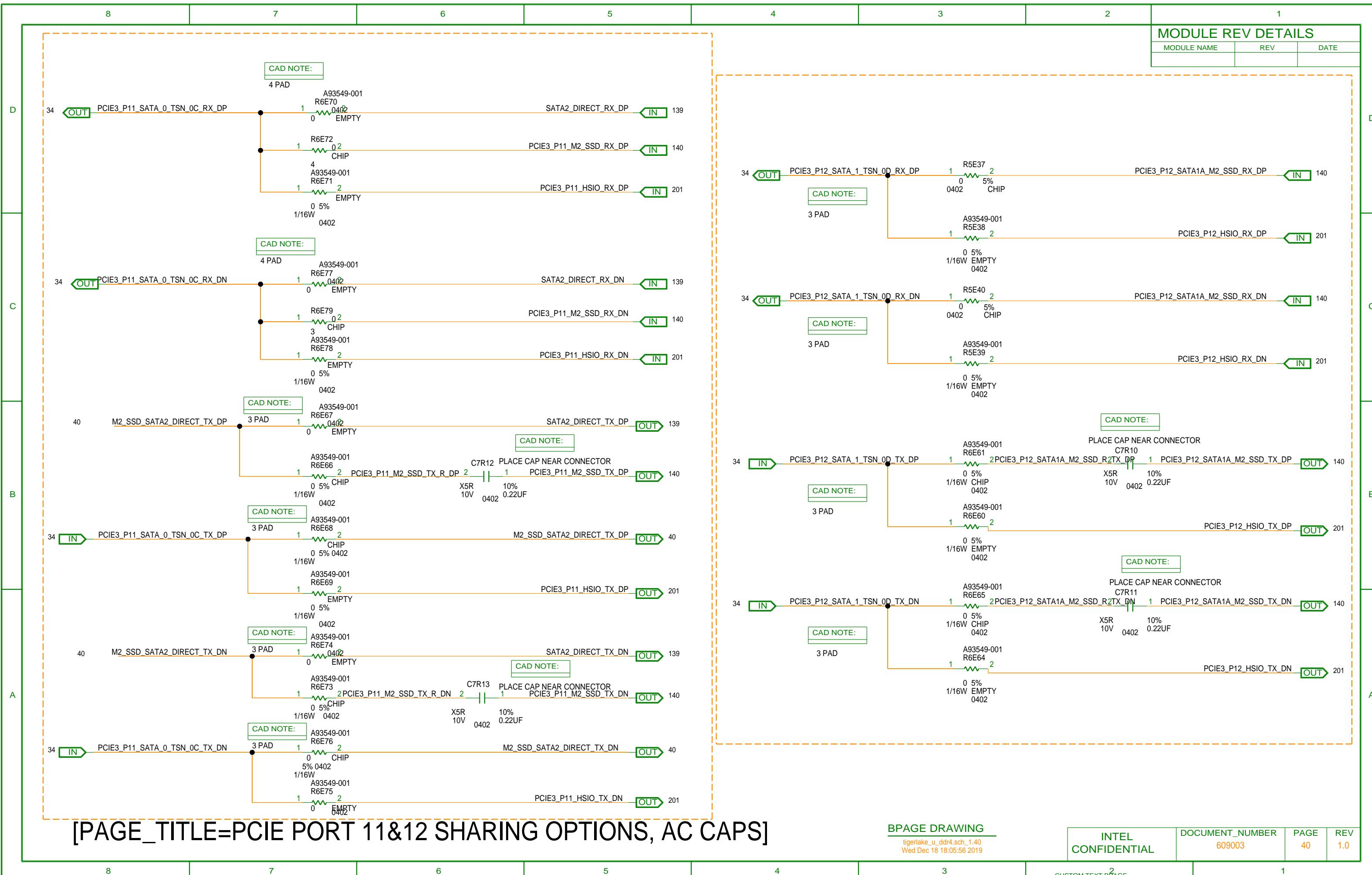
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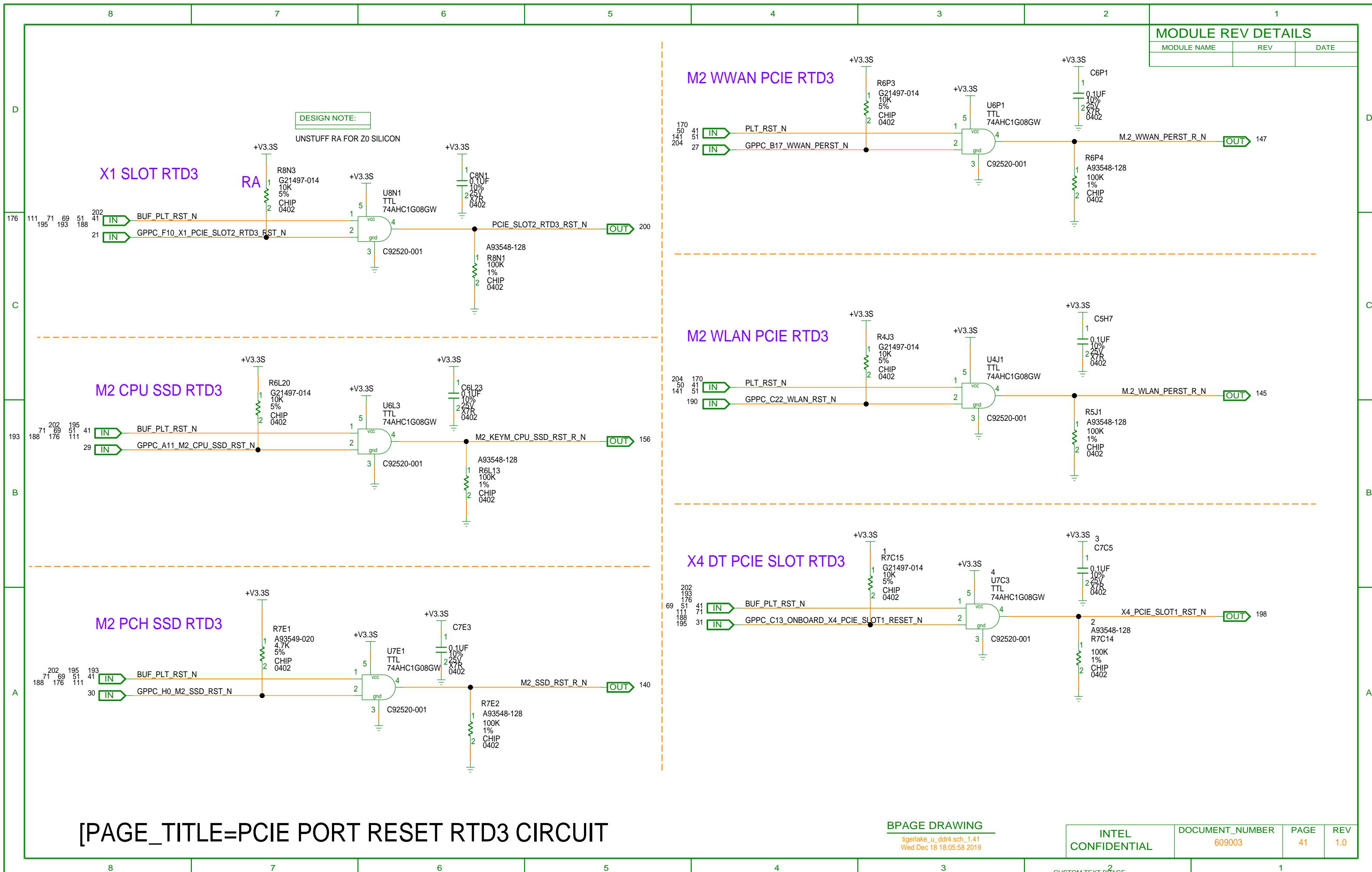
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|                    | 609003          | 39   | 1.0 |

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| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

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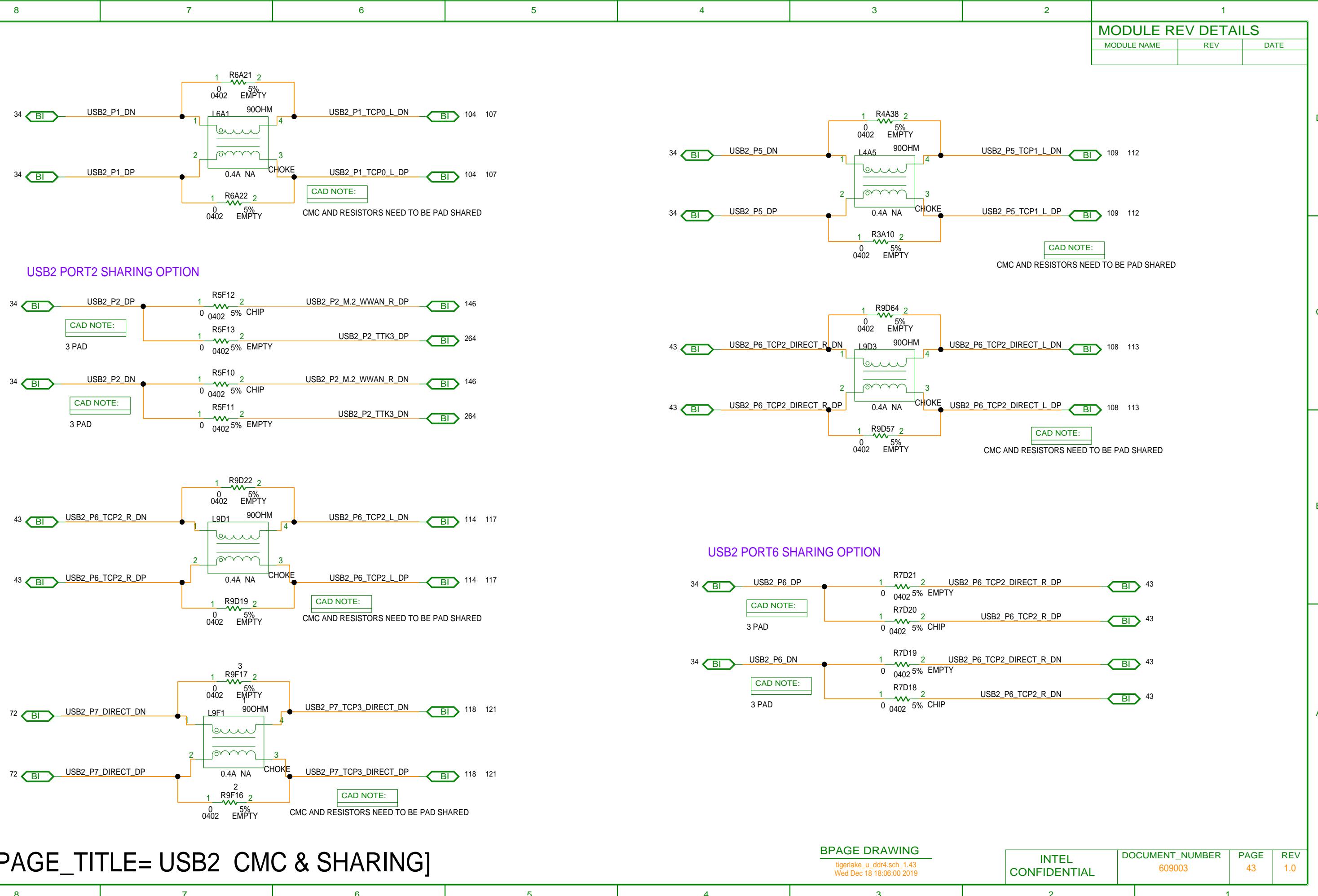
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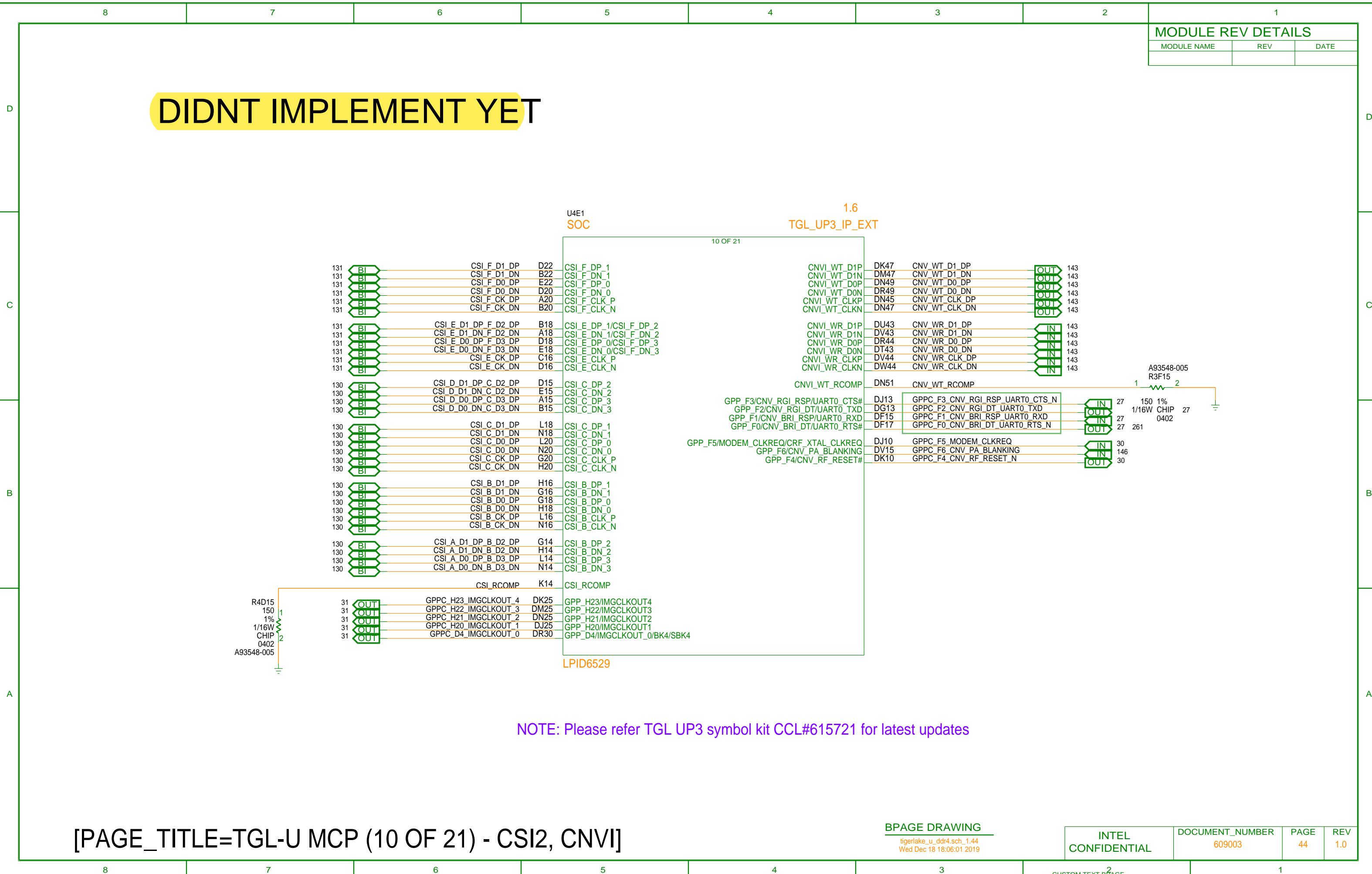
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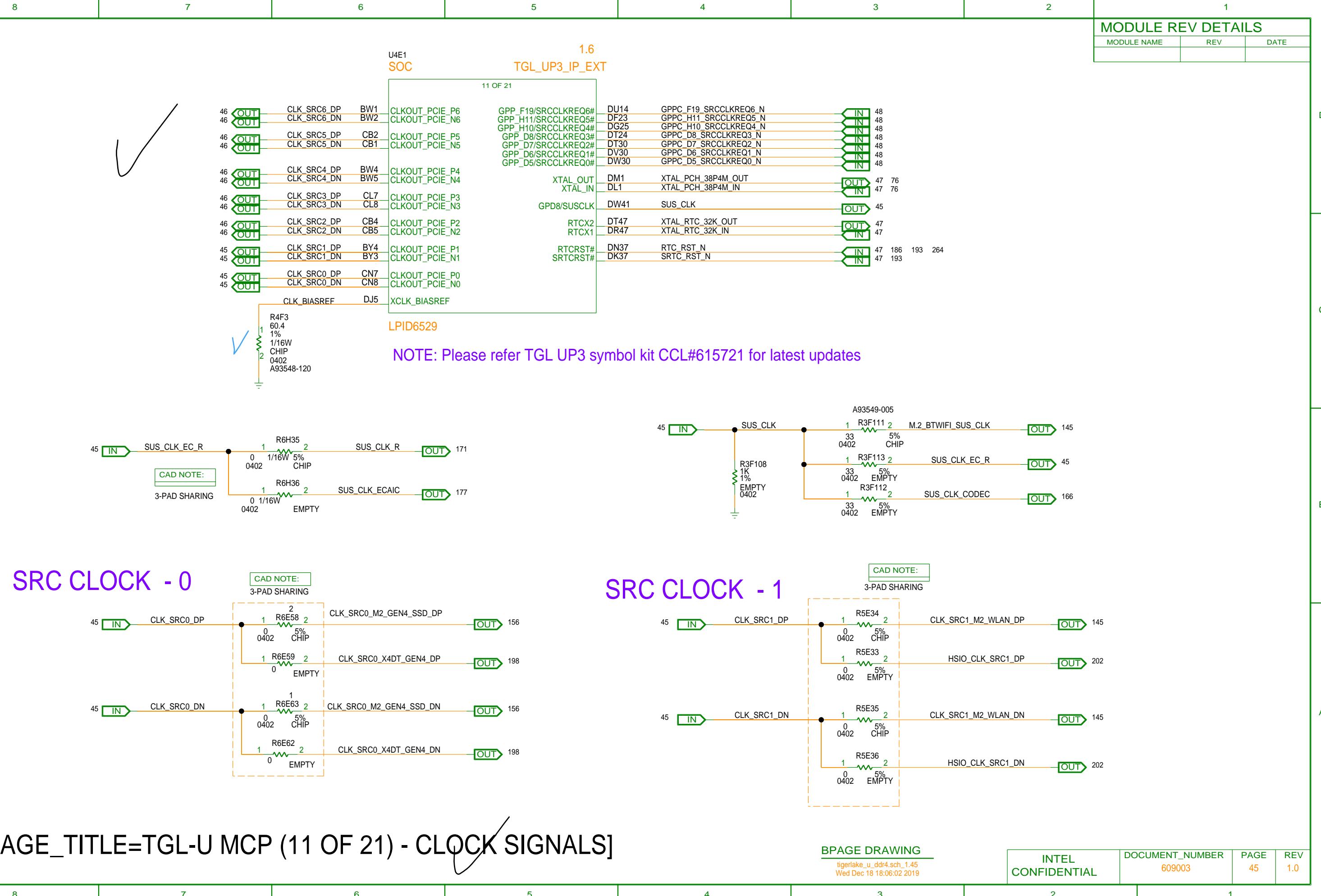
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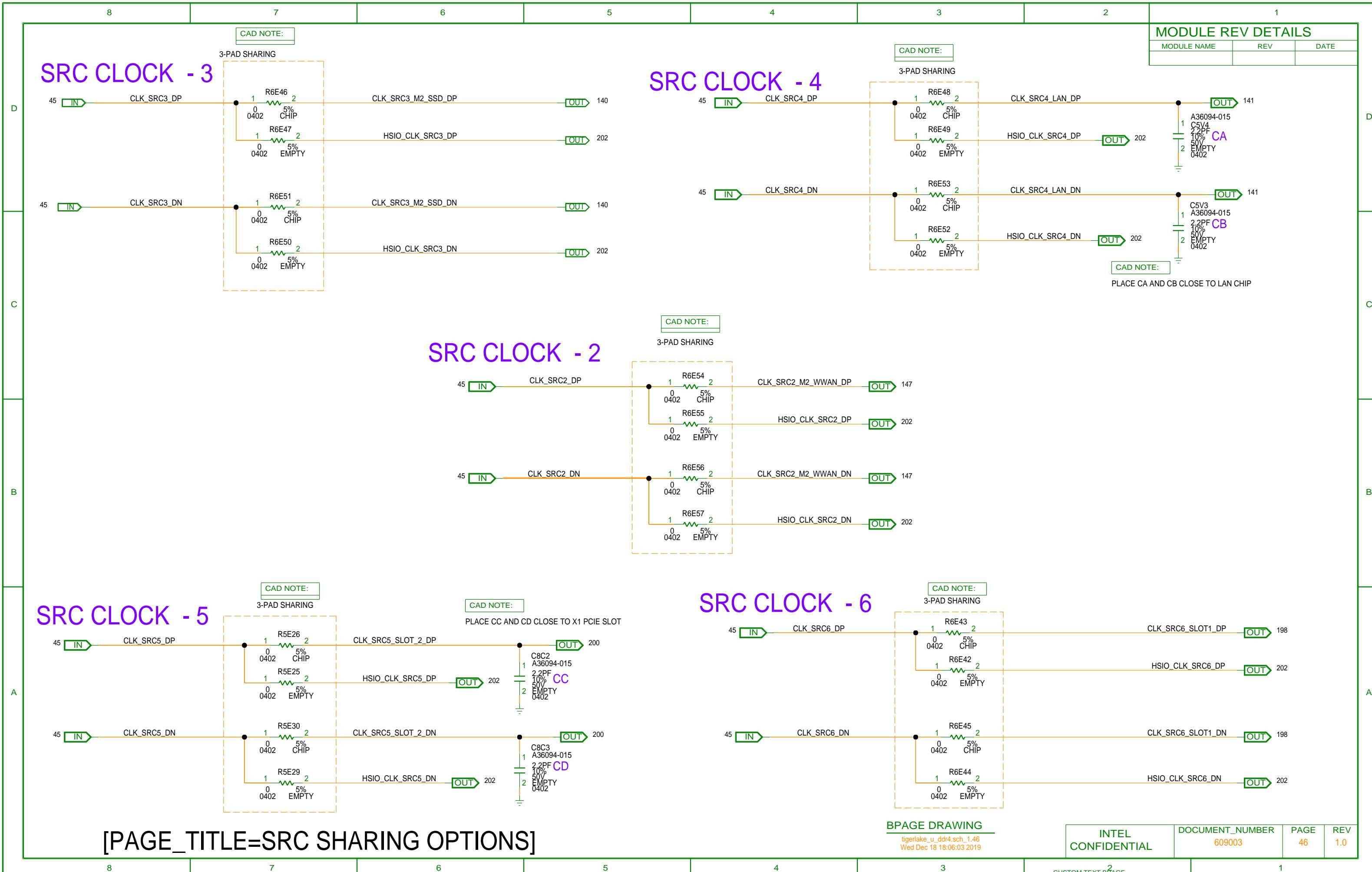
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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>42 | REV<br>1.0 |
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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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**MODULE REV DETAILS**

| MODULE NAME | REV | DATE |
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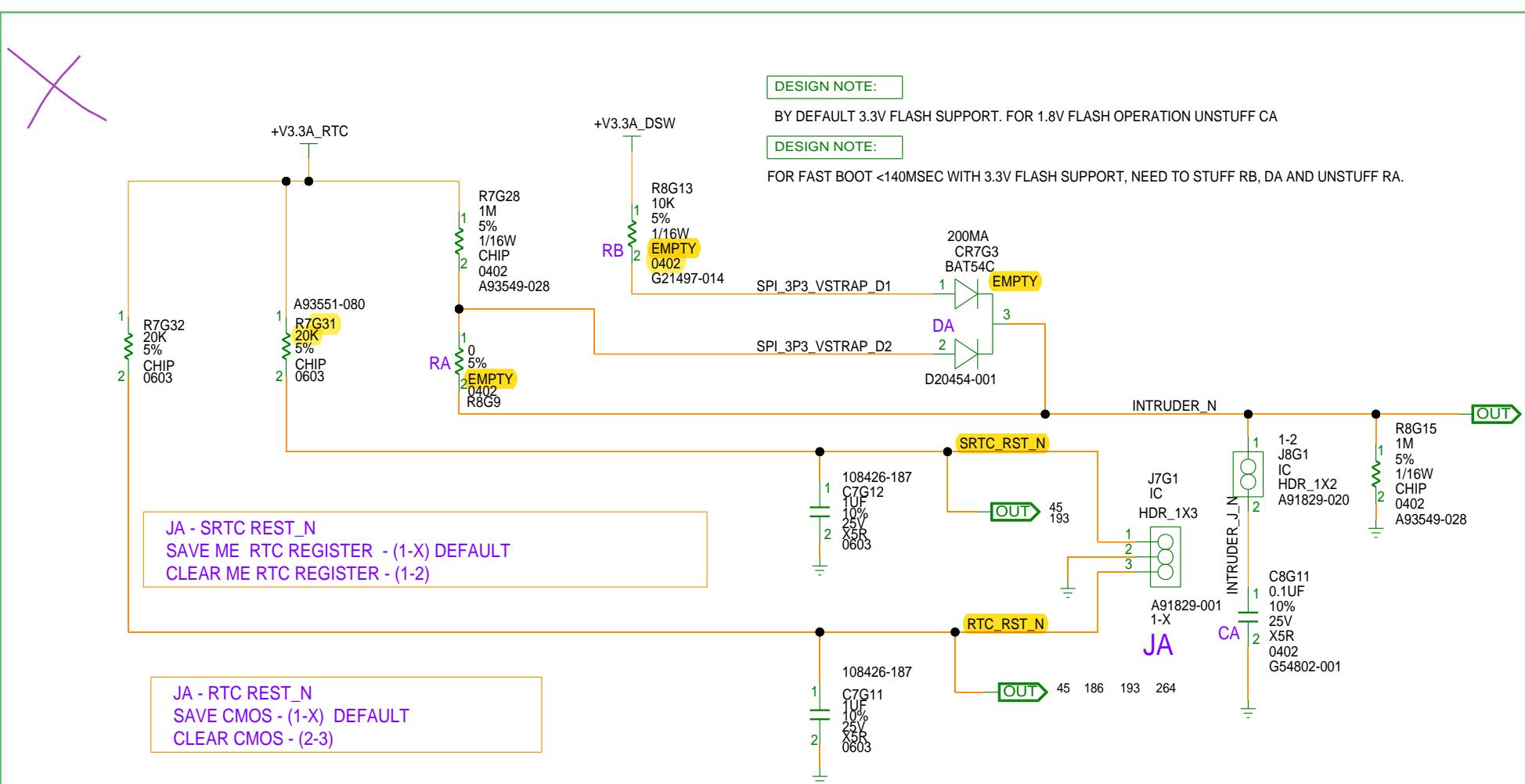
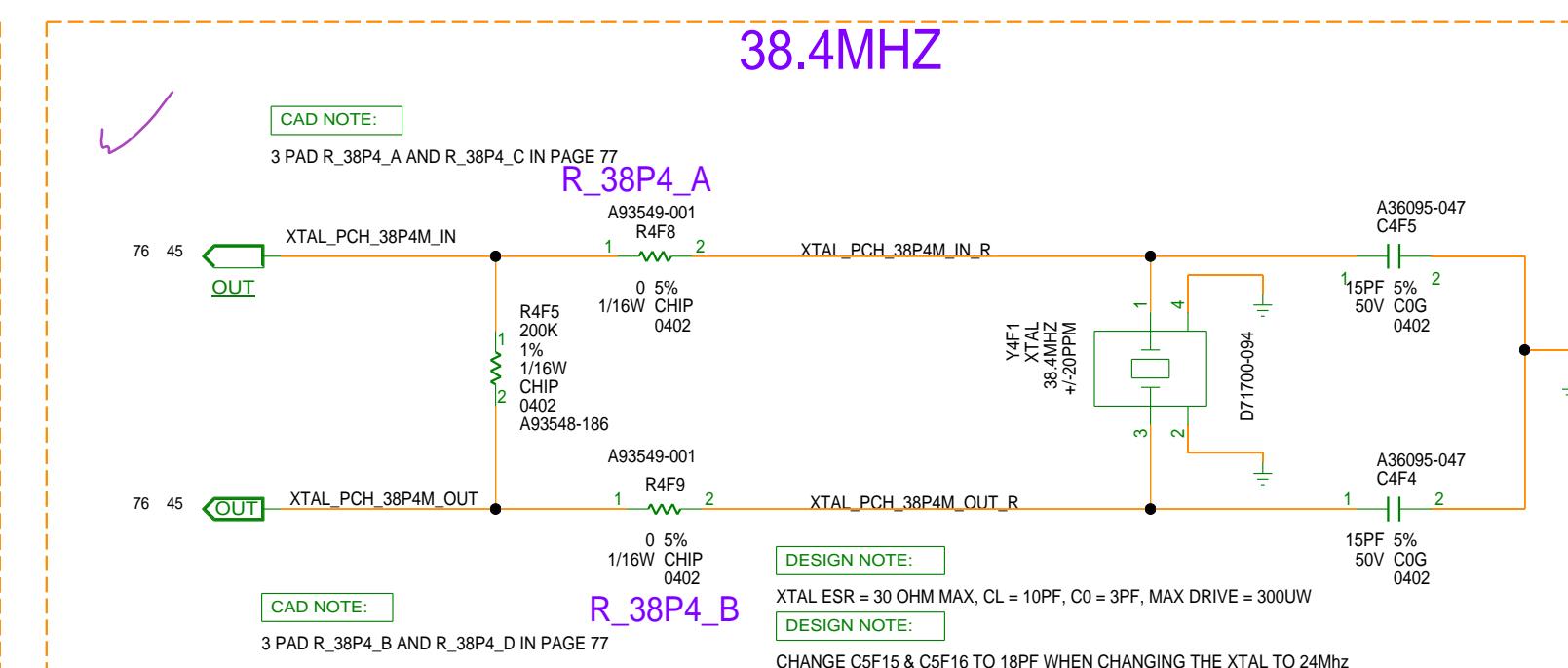
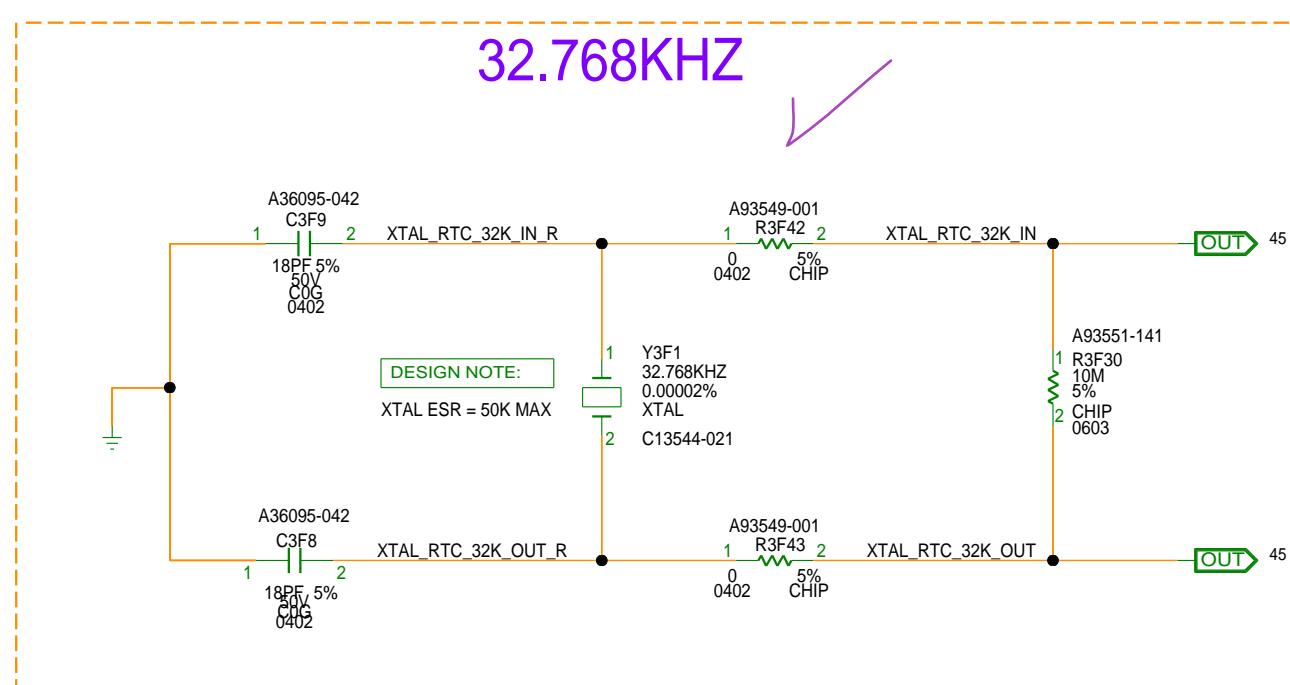
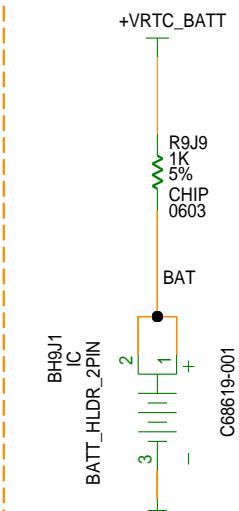
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**+V3.3A\_RTC GENERATION**

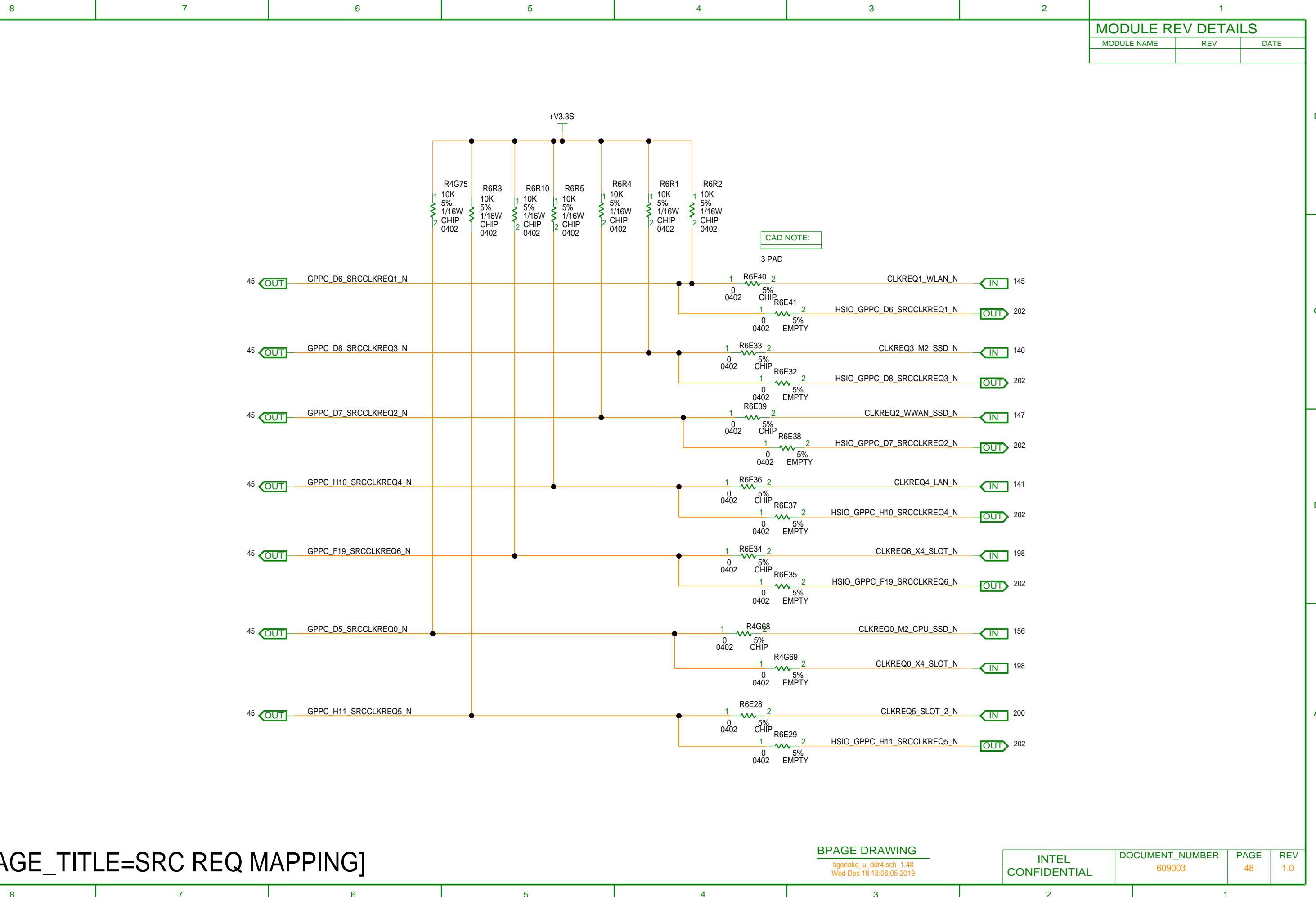
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tigerlake\_u\_ddr4.sch\_1.47  
Wed Dec 18 18:06:04 2019

| INTEL CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
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| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

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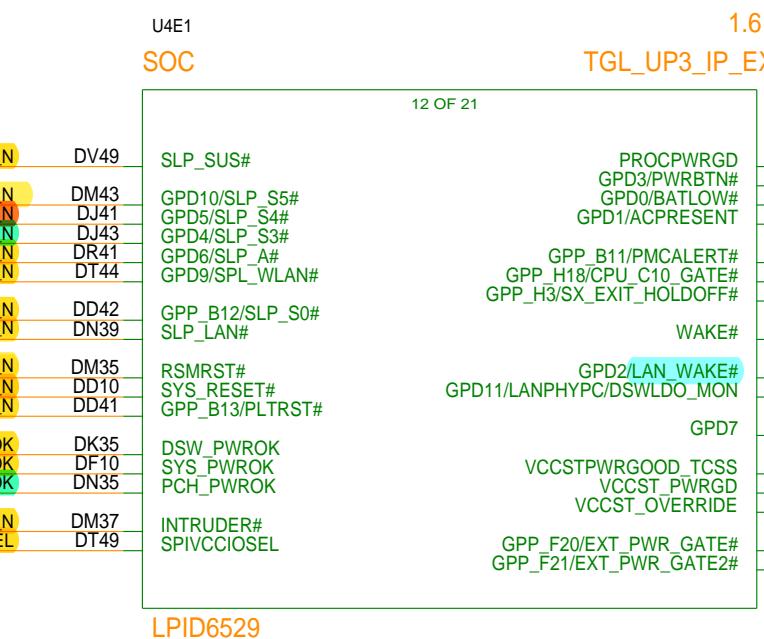
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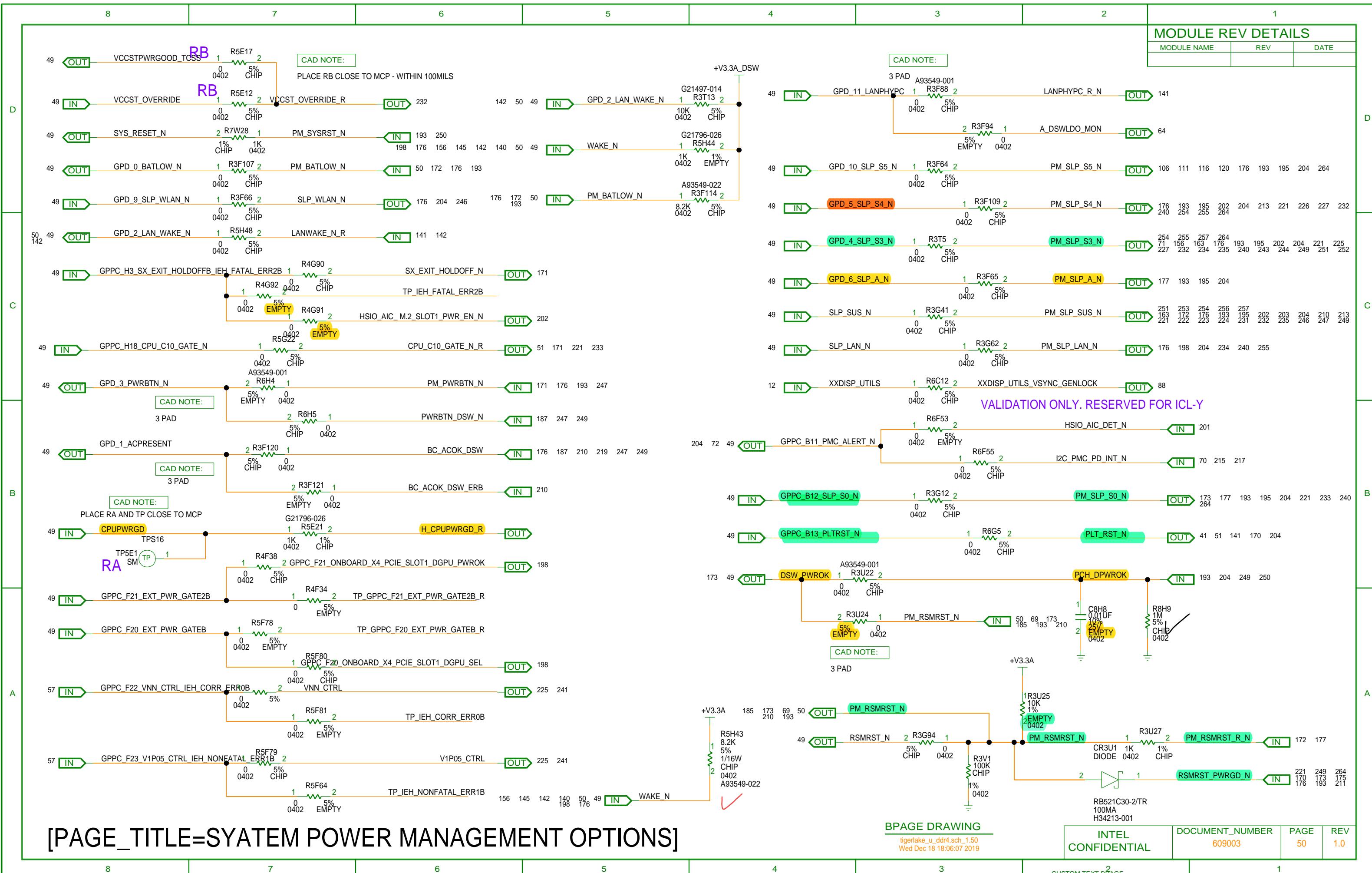
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A

A

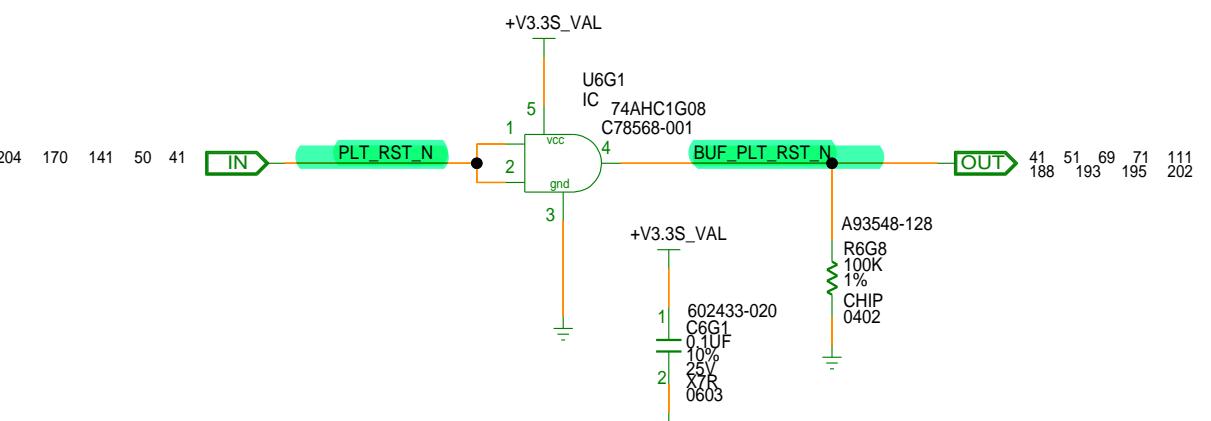
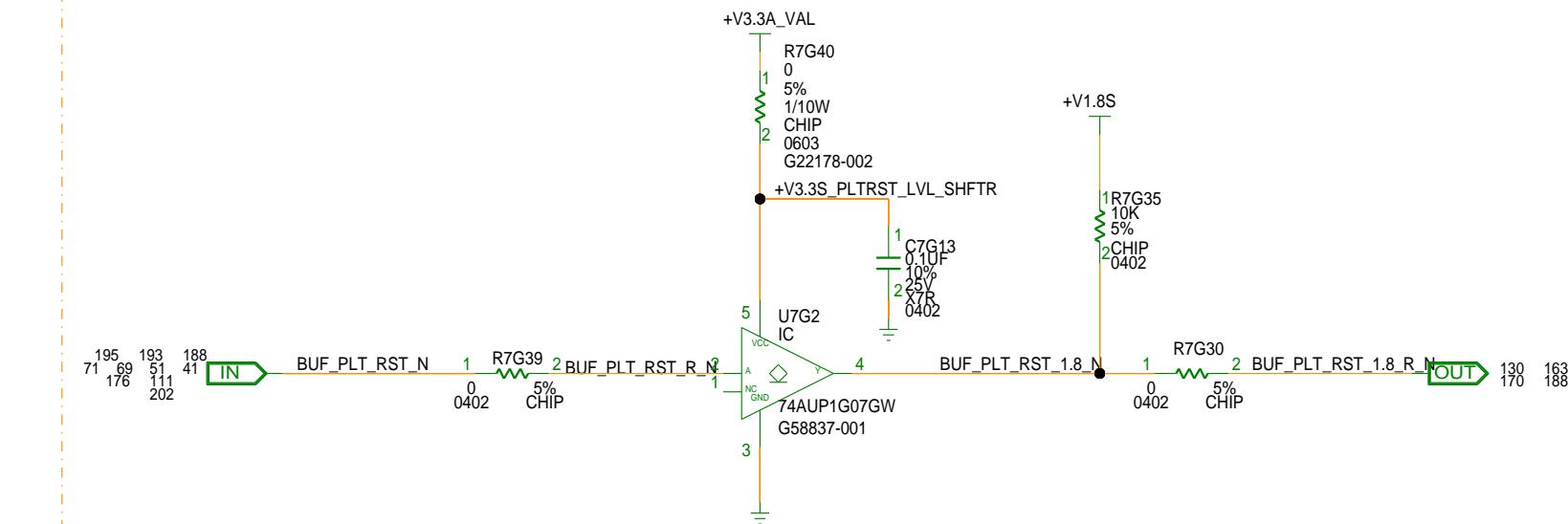


NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates



|                           |   |   |   |   |   |   |   |
|---------------------------|---|---|---|---|---|---|---|
| 8                         | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |   |   |   |   |   |   |

D

**BUFFER TO REDUCE LOADING ON PLT\_RST\_N****PLATFORM RESET LEVEL SHIFTER - 3.3V TO 1.8V**

C

B

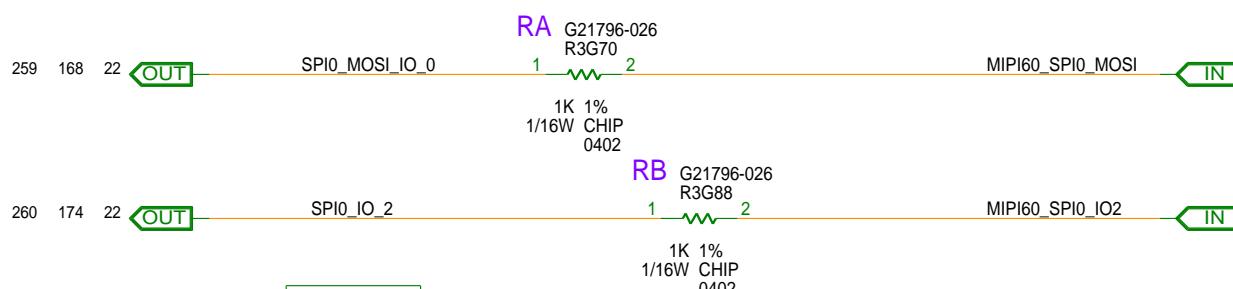
A

D

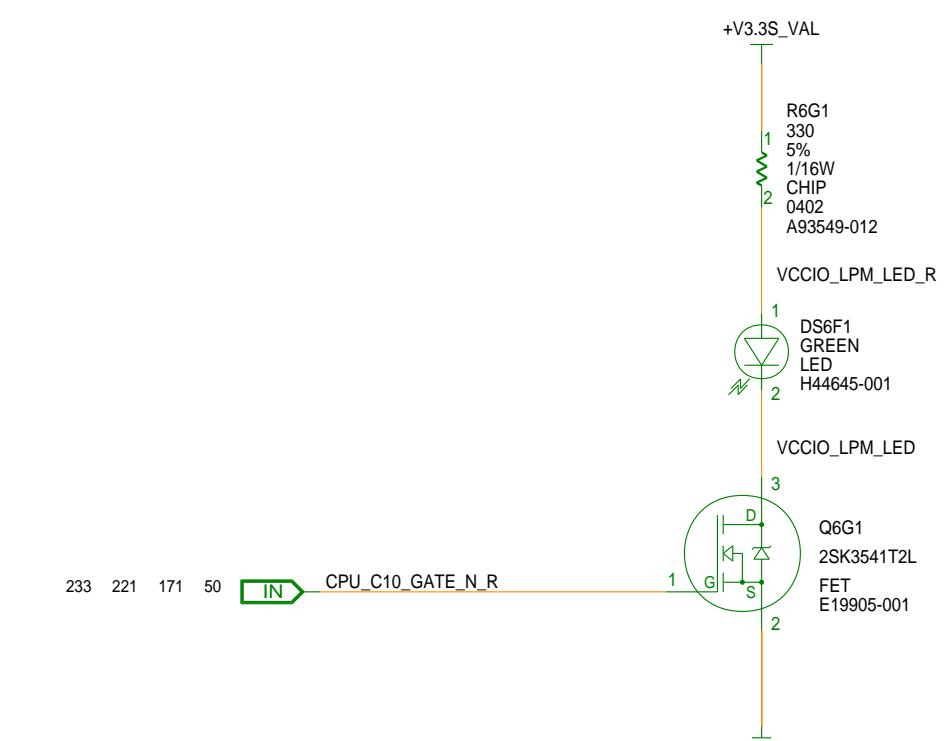
C

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**CAD NOTE:**  
RA AND RB RESISTORS NEED TO BE PLACED NEAR TO MCP, WITHOUT STUB ON SPI



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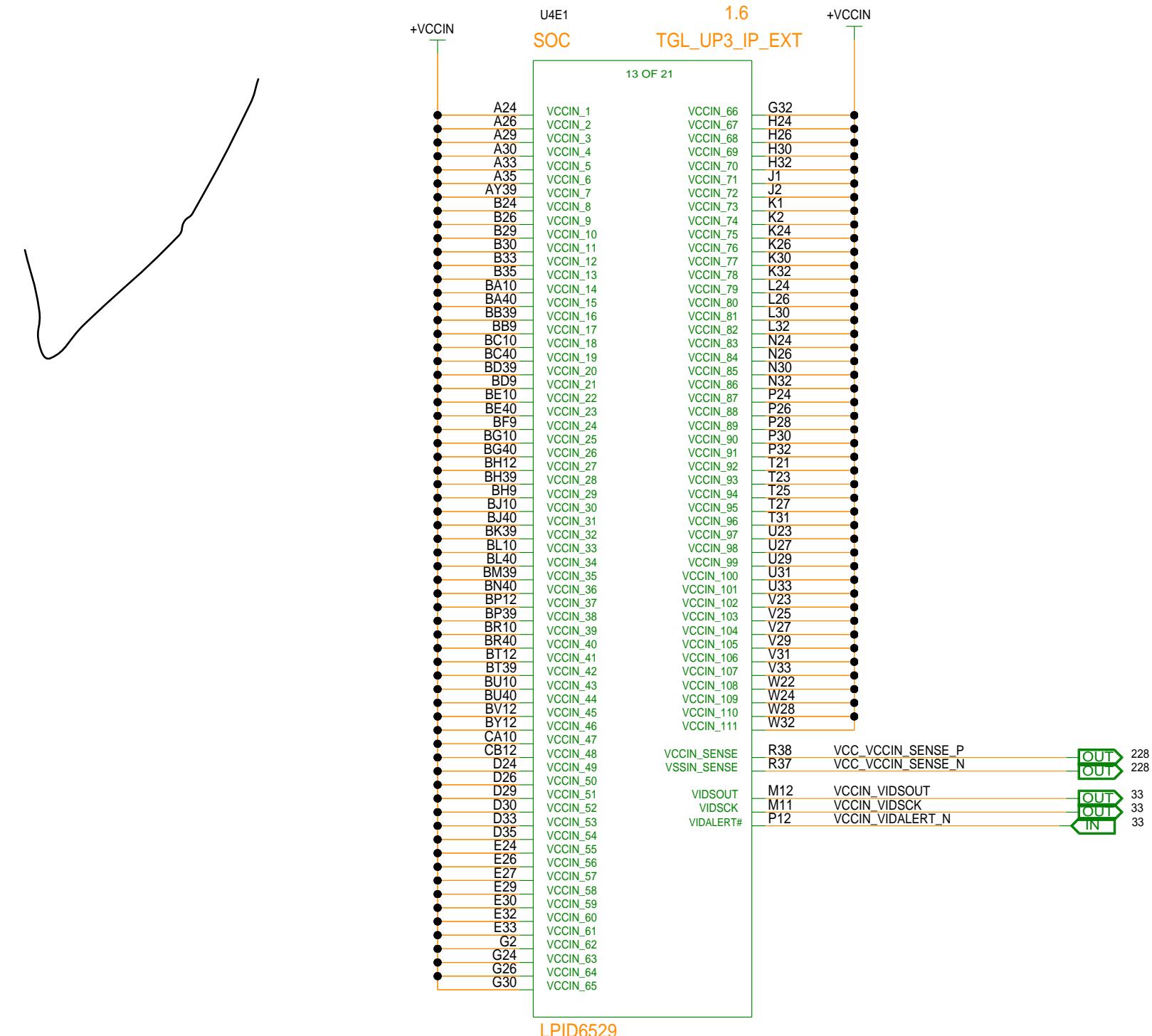
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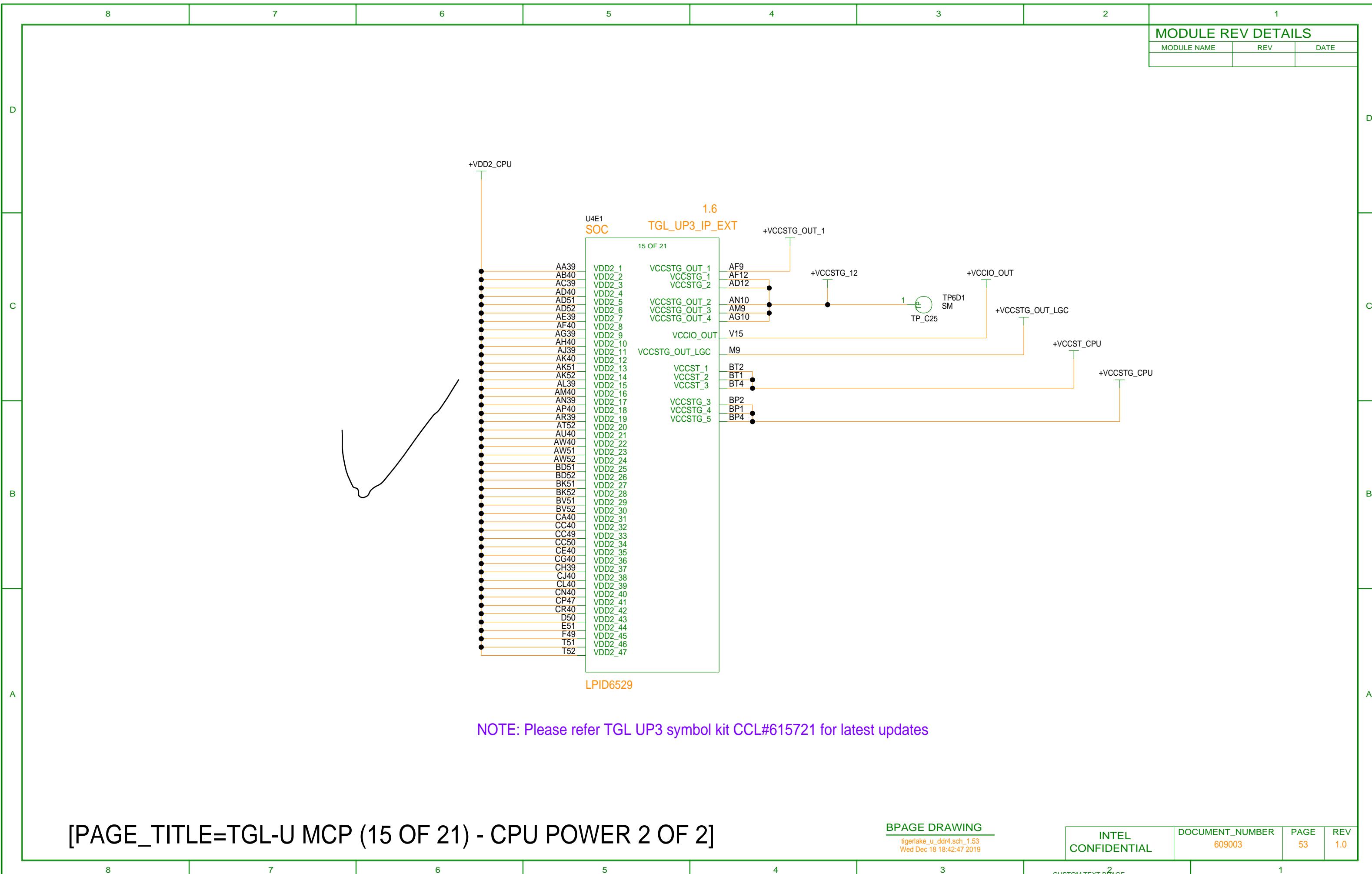
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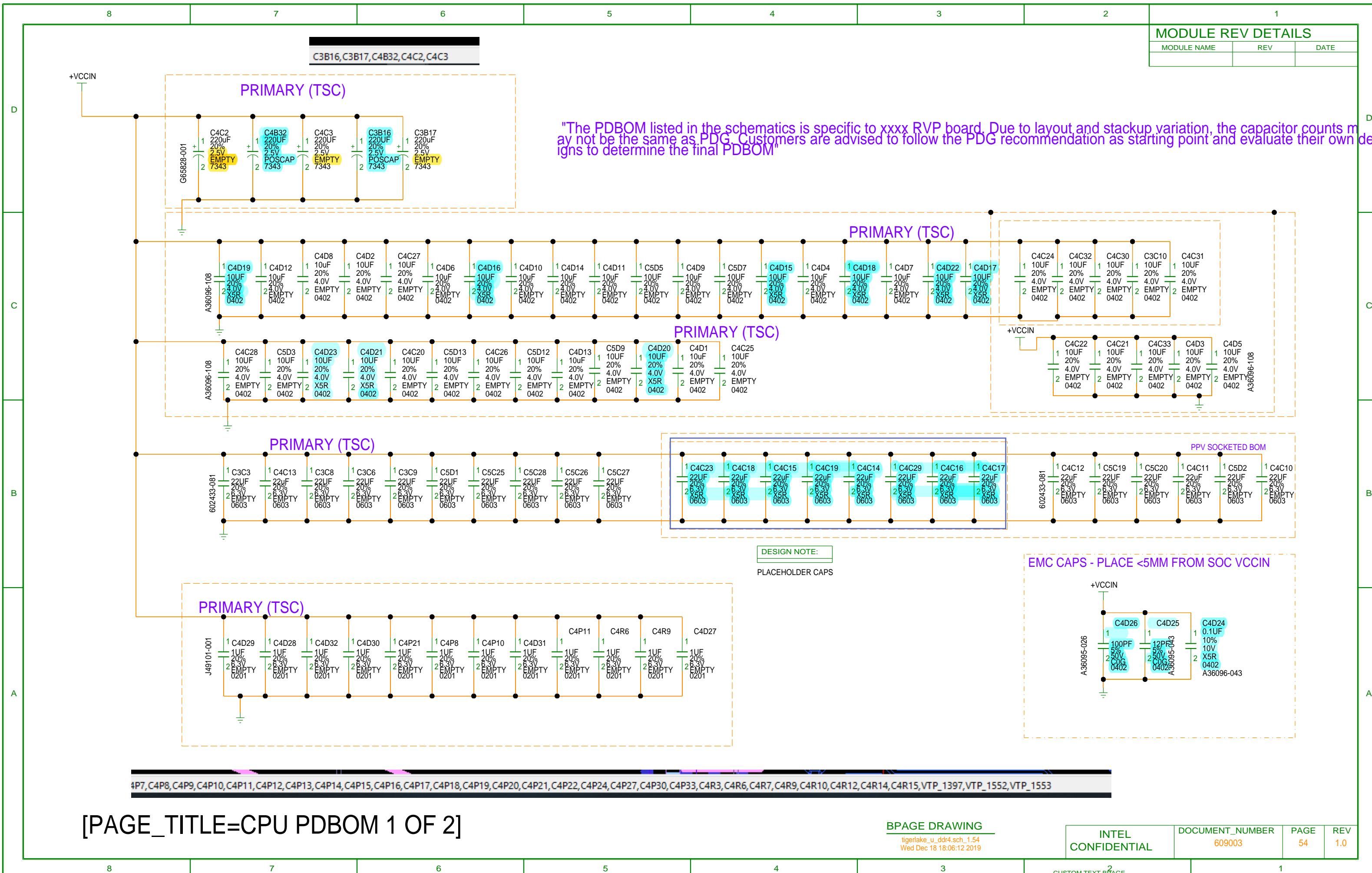
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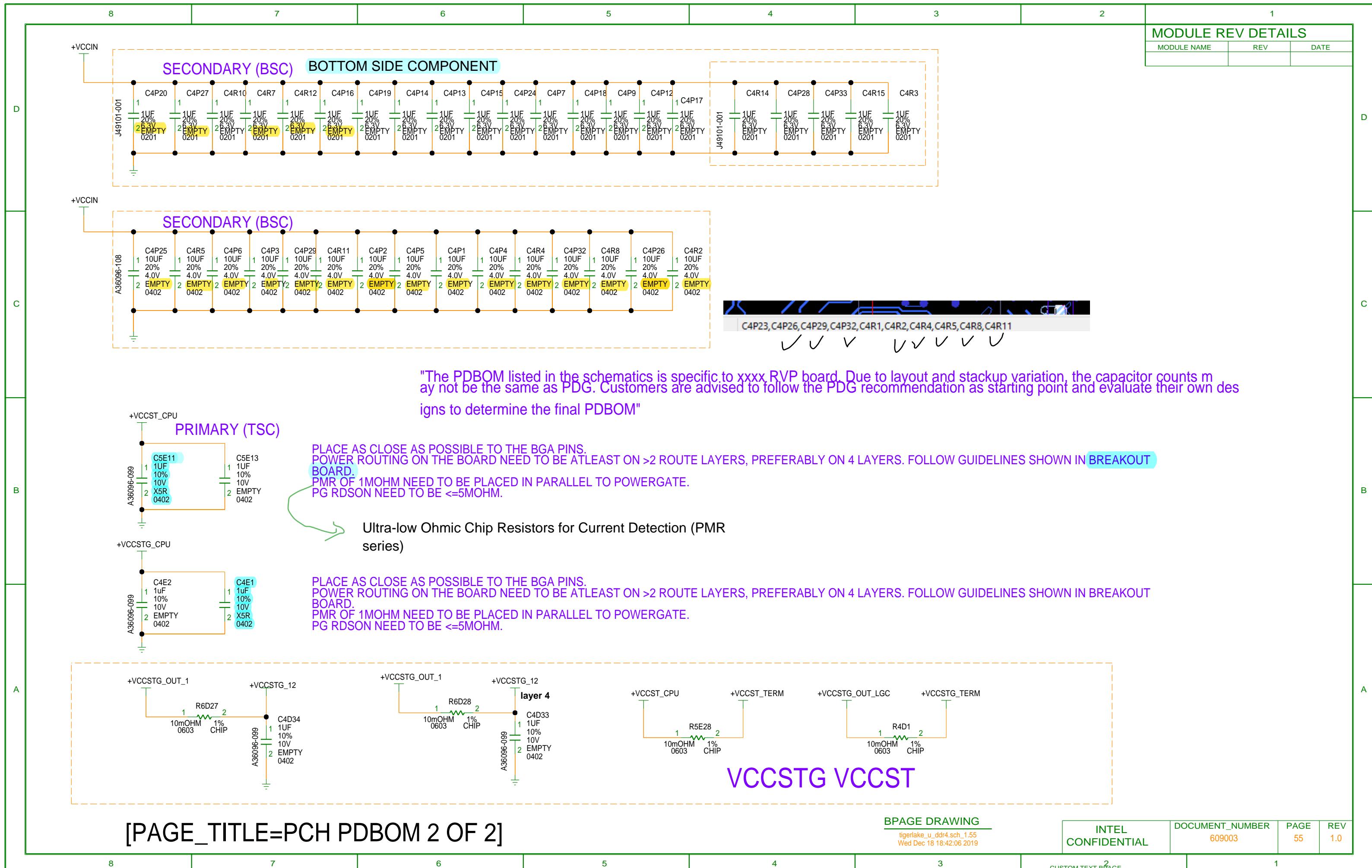
## MODULE REV DETAILS

| MODULE NAME | REV | DATE |
|-------------|-----|------|
|             |     |      |





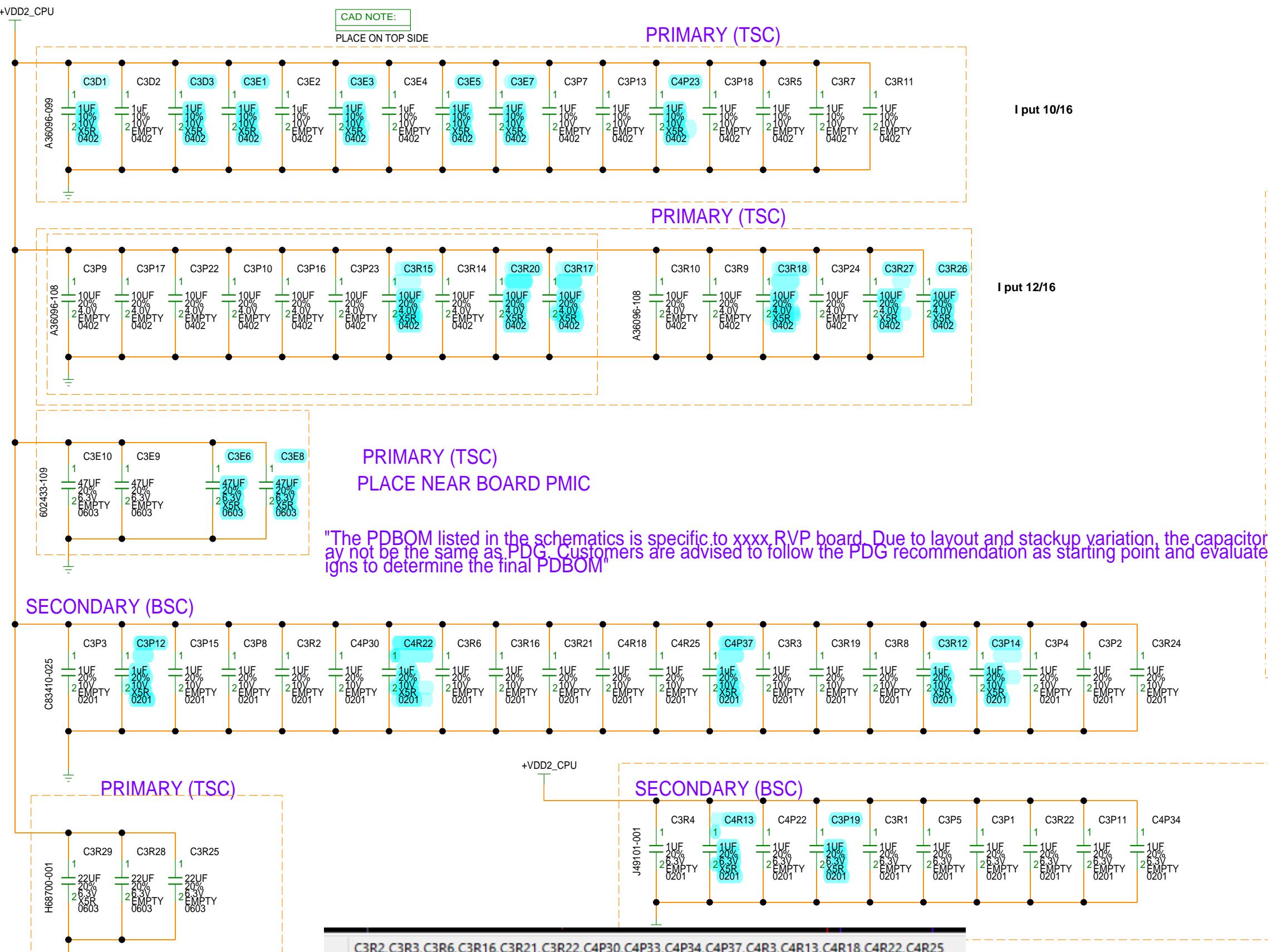




VDD2

| MODULE REV DETAILS |     |      |
|--------------------|-----|------|
| MODULE NAME        | REV | DATE |
|                    |     |      |

EMC CAPS - PLACE &lt;4MM FROM SOC VDDQ, WITH EACH PAIR &lt;12MM APART



[PAGE\_TITLE=CPU PDBOM 2 OF 2]

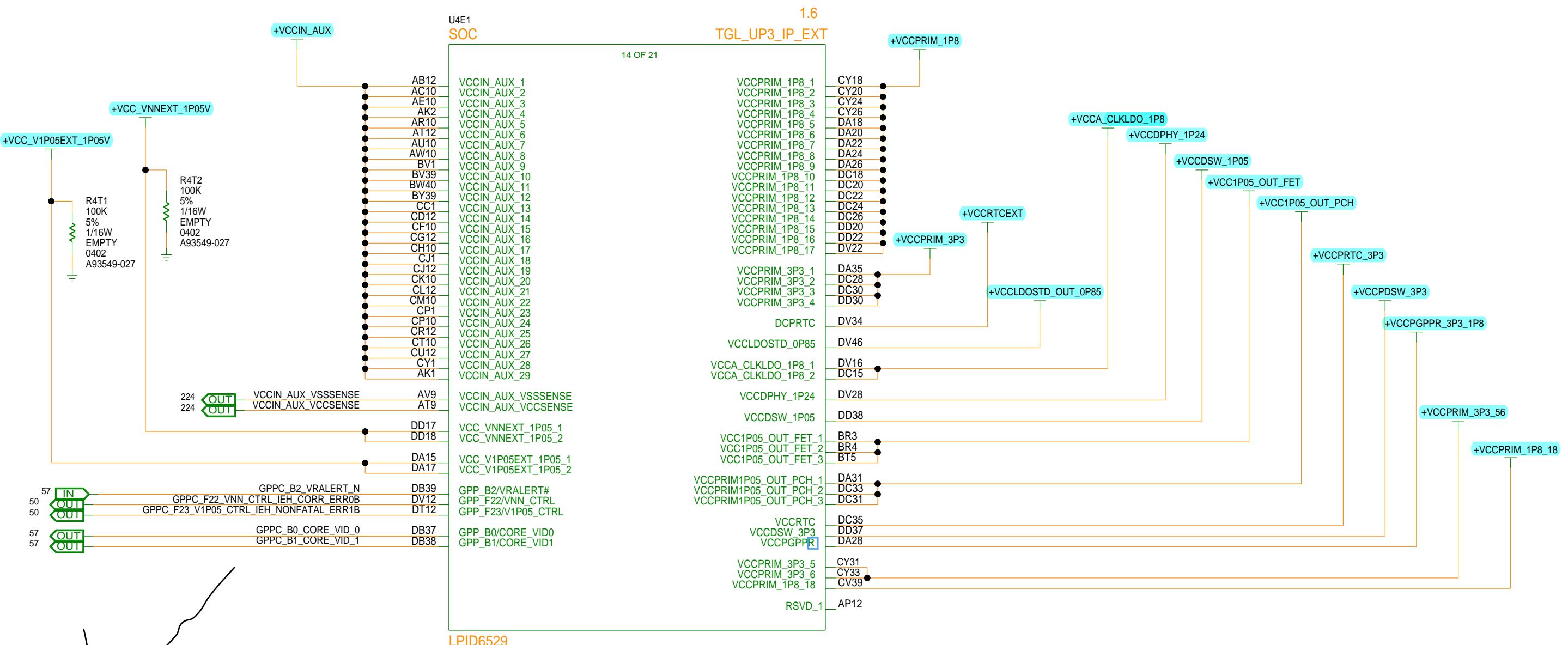
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tigerlake\_u\_ddr4.sch\_156  
Wed Dec 18 18:06:14 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
|-----------------------|-----------------|------|-----|
|                       | 609003          | 56   | 1.0 |

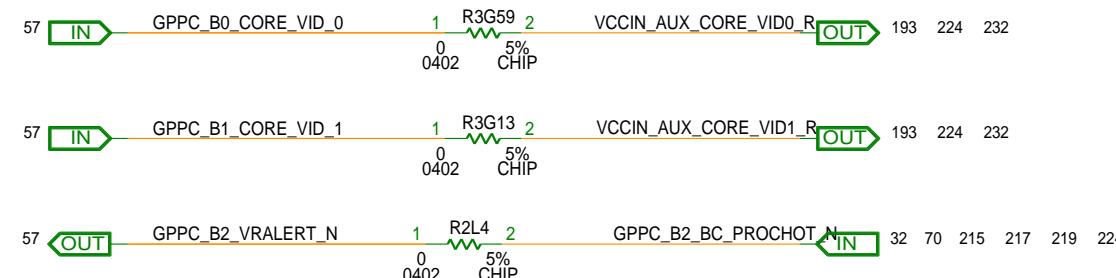
CUSTOM TEXT BPAGE

8 7 6 5 4 3 2 1

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

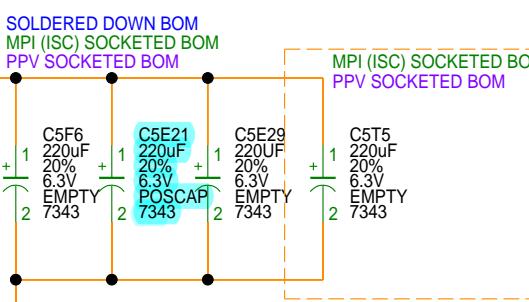


# VCCIN\_AUX\_1P8

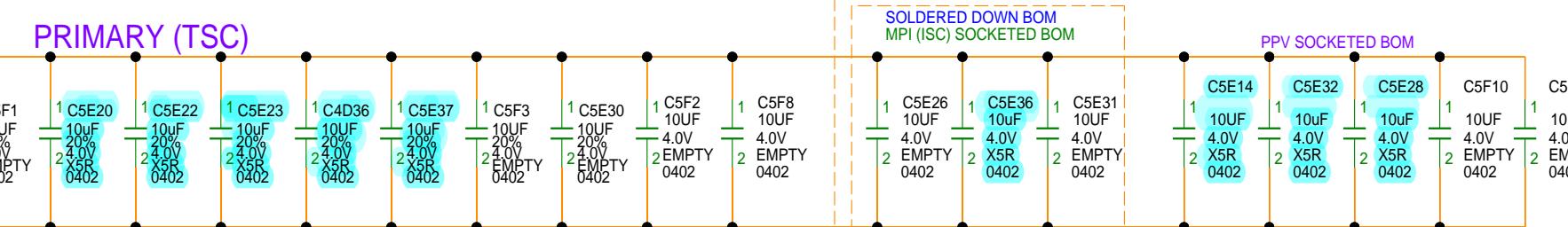
## MODULE REV DETAILS

| MODULE NAME | REV | DATE |
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|             |     |      |

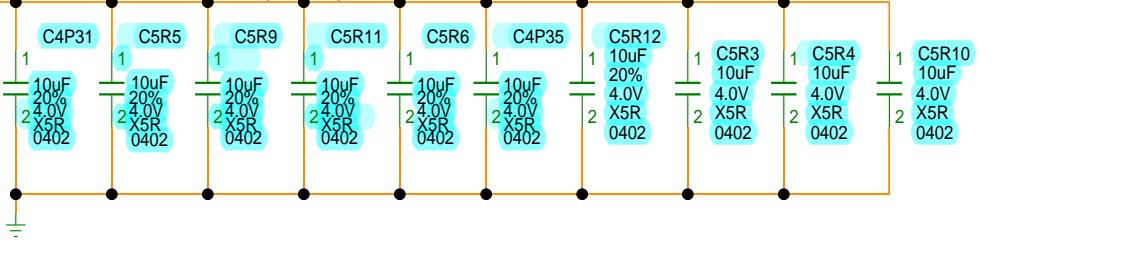
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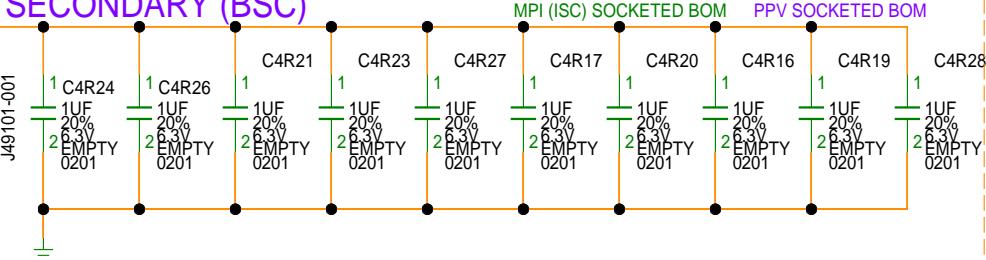
### PRIMARY (TSC)



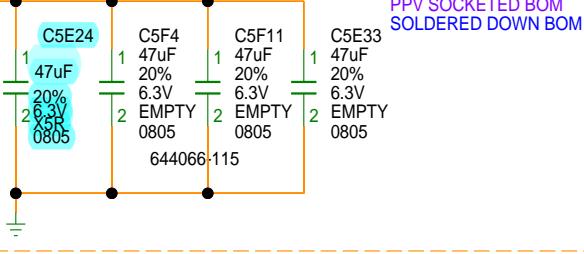
### SECONDARY (BSC)



### SECONDARY (BSC)



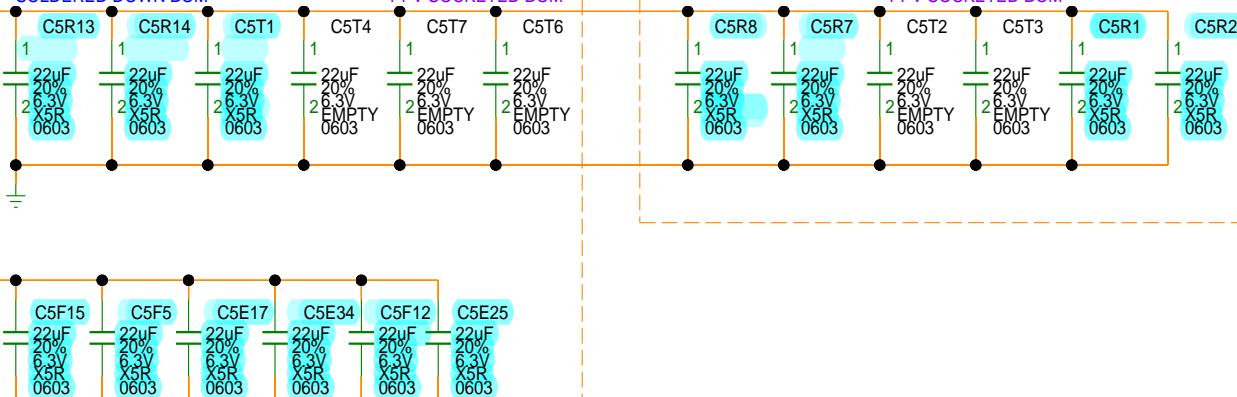
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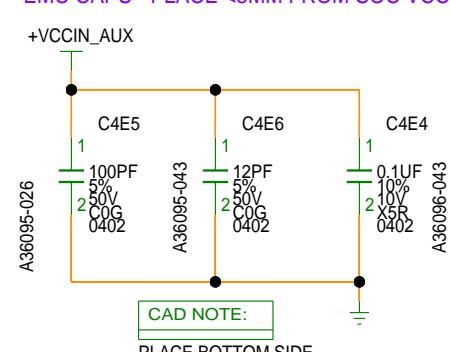
+VCCIN\_AUX

CAP ADDED FOR PI SIMULATION AS PER PI FEEDBACK  
PLACE CLOSE TO PIN AK1 of SoC

### SOLDERED DOWN BOM MPI (ISC) SOCKETED BOM PPV SOCKETED BOM



### EMC CAPS - PLACE <5MM FROM SOC VCCIN\_AUX



[PAGE\_TITLE=PDBOM- VCCIN\_AUX]

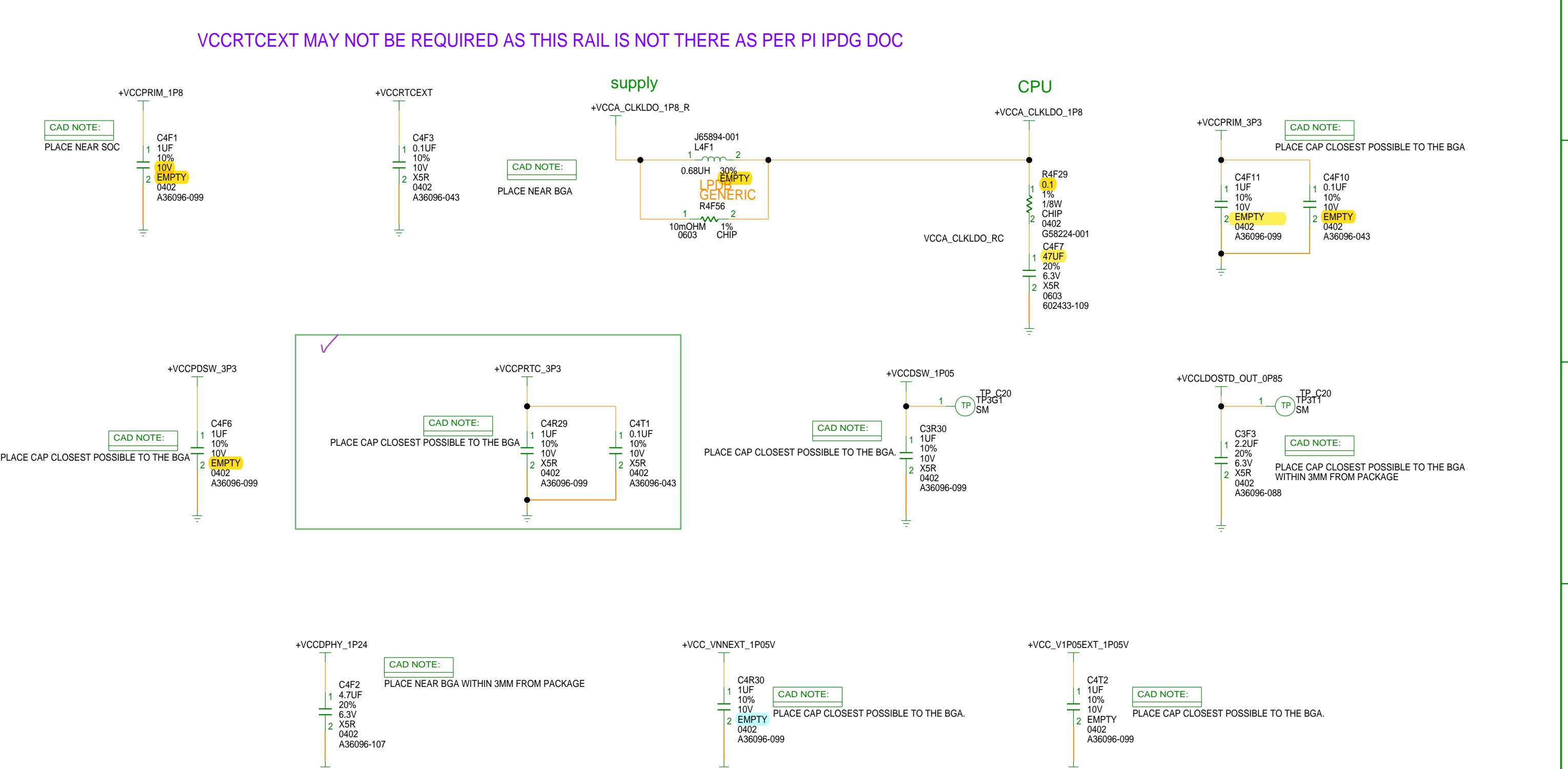
BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.58  
Wed Dec 18 18:42:42 2019

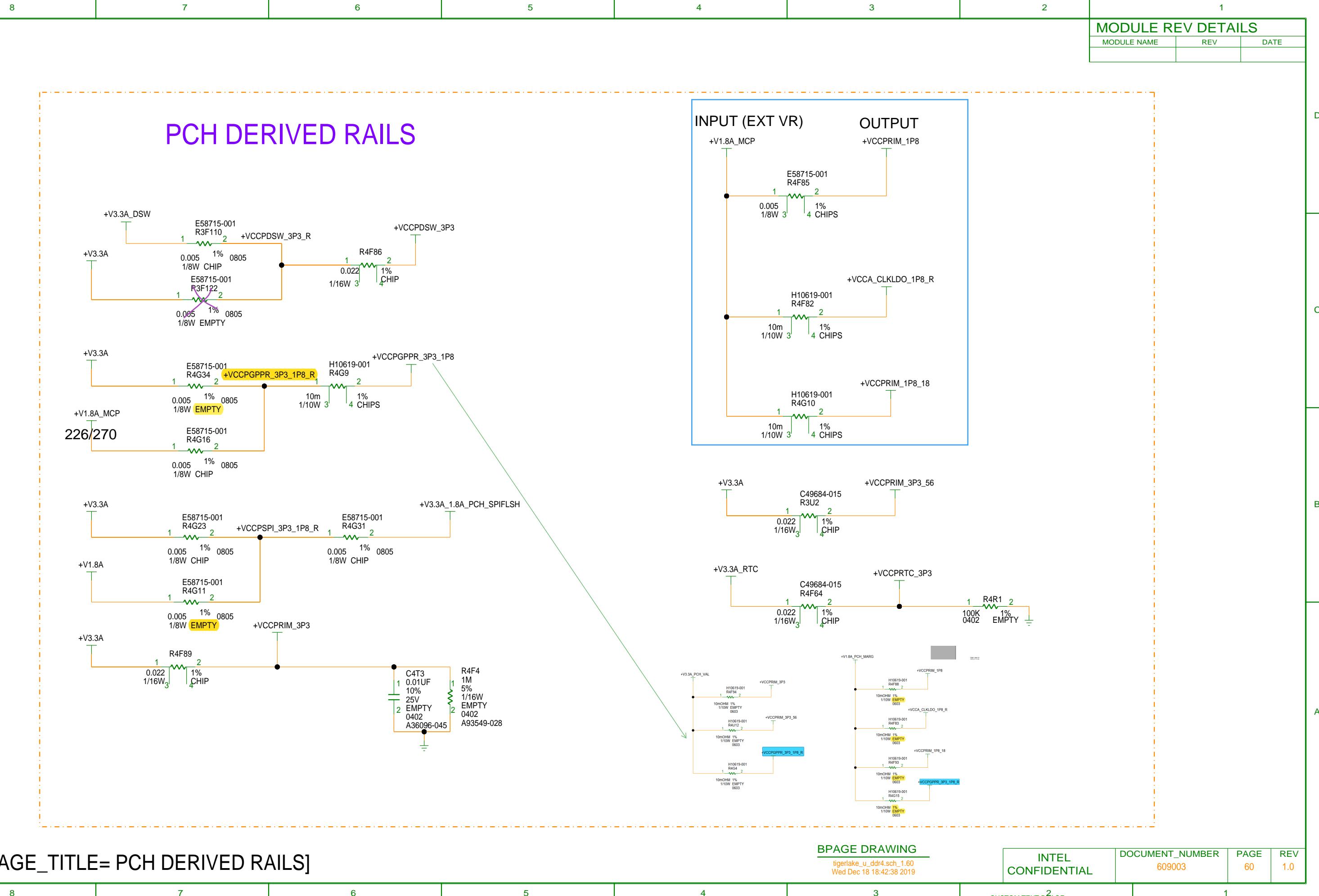
| INTEL CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
|--------------------|-----------------|------|-----|
|                    | 609003          | 58   | 1.0 |

CUSTOM TEXT BPAGE

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|---------------------------|---|-----|------|---|---|---|---|
| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

VCCRTCEXT MAY NOT BE REQUIRED AS THIS RAIL IS NOT THERE AS PER PI IPDG DOC



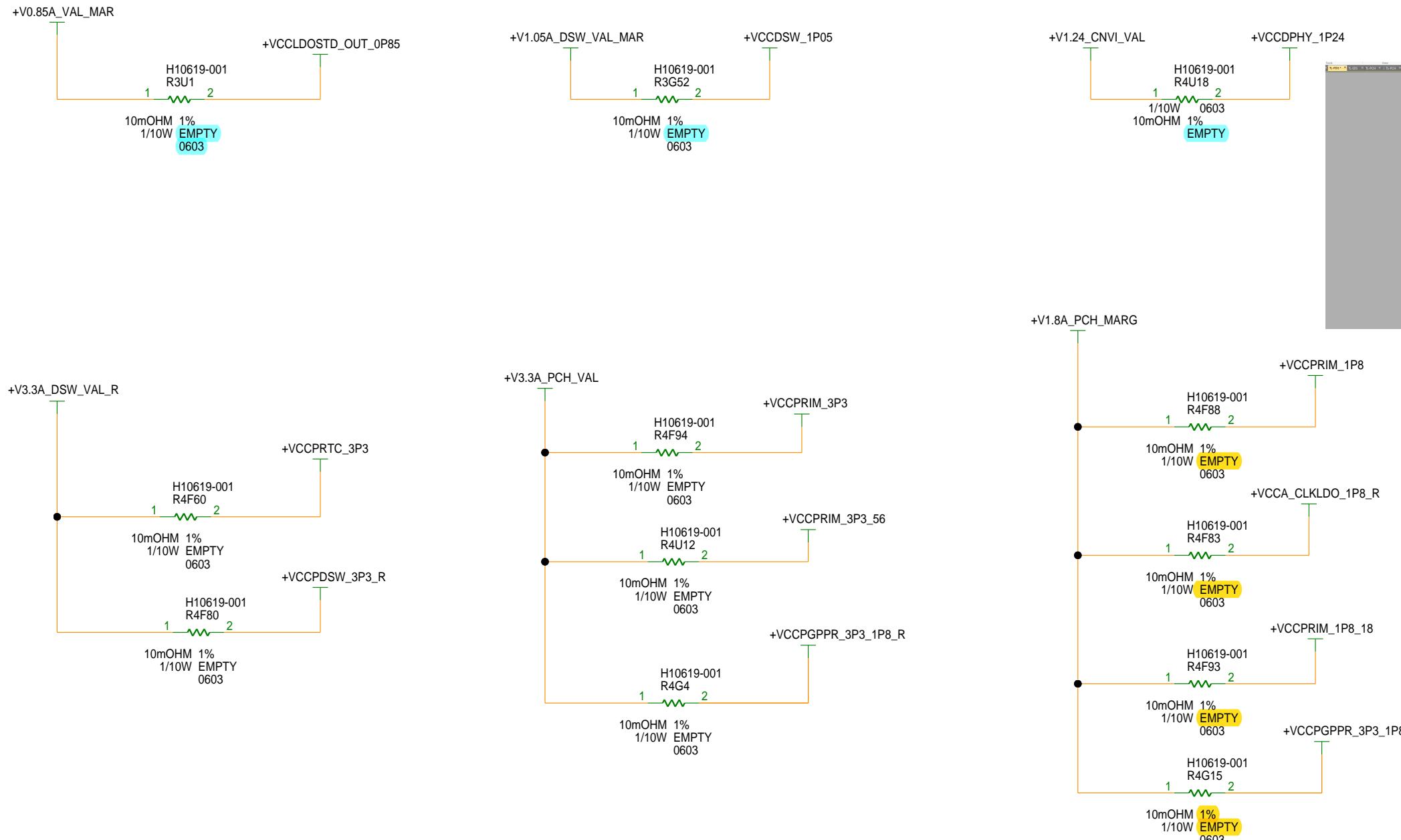


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|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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# PCH MARGINING RAILS

## MODULE REV DETAILS

| MODULE NAME | REV | DATE |
|-------------|-----|------|
|             |     |      |



| Table 237. No Direct Switching or No External Bypass Supported |               |        |           |           |          |           |
|--|---------------|--------|-----------|-----------|----------|-----------|
| State Enable   | Q1 CNVI       | Q2 ISH | Q3 Type A | Q4 C-Link | Q5 SMBus | Q6 PHY PG |
| S02.0  | Always Enable | -      | -         | -         | -        | -         |
| S02.1  | Always Enable | -      | -         | -         | -        | -         |
| S02.2  | -             | -      | NO        | -         | -        | YES       |
| S03.0  | NO            | NO     | -         | -         | -        | -         |
| S03.1  | NO            | NO     | -         | -         | -        | -         |
| S03.2  | NO            | NO     | -         | -         | -        | -         |
| S03.3  | NO            | NO     | NO        | -         | -        | YES       |

**Voltage Margining**  
Voltage margining allows bypass VRs to reduce their voltages depending on S03.x states. To enable this feature, VNN\_CTRL and V1P05\_CTRL GPIO pins should be configured. This feature can reduce power in Soix states.

Tiger Lake UP3 UP4 H35 UP3 Refresh Platform

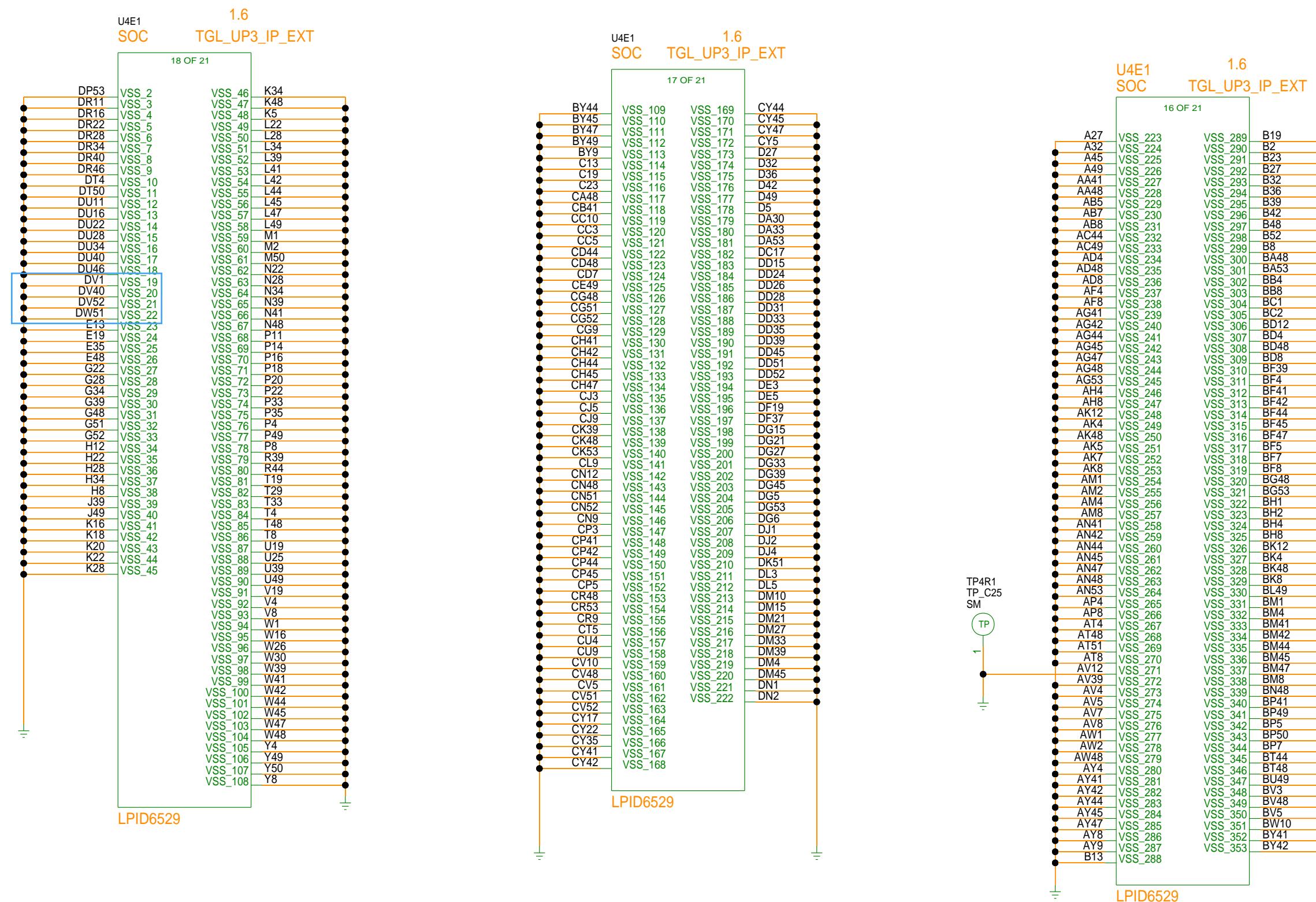
Document ID: 00000000000000000000000000000000

November 2020

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|

**MODULE REV DETAILS**

| MODULE NAME | REV | DATE |
|-------------|-----|------|
|             |     |      |



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE\_TITLE=TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)]

BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.62  
Wed Dec 18 18:06:20 2019

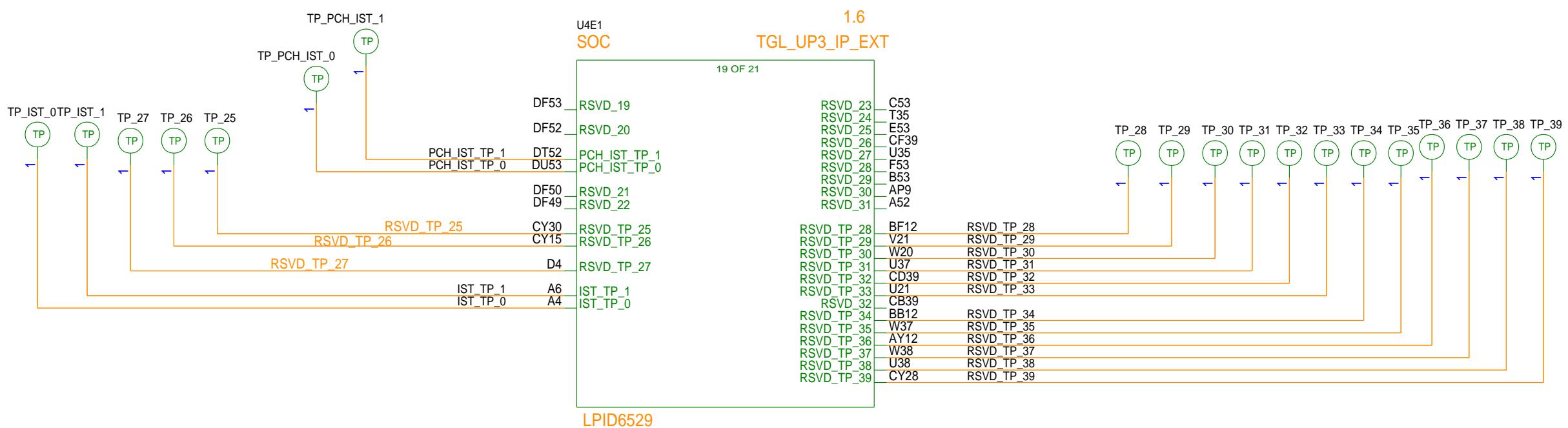
|                       |                           |            |            |
|-----------------------|---------------------------|------------|------------|
| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>62 | REV<br>1.0 |
|-----------------------|---------------------------|------------|------------|

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CUSTOM TEXT BPAGE

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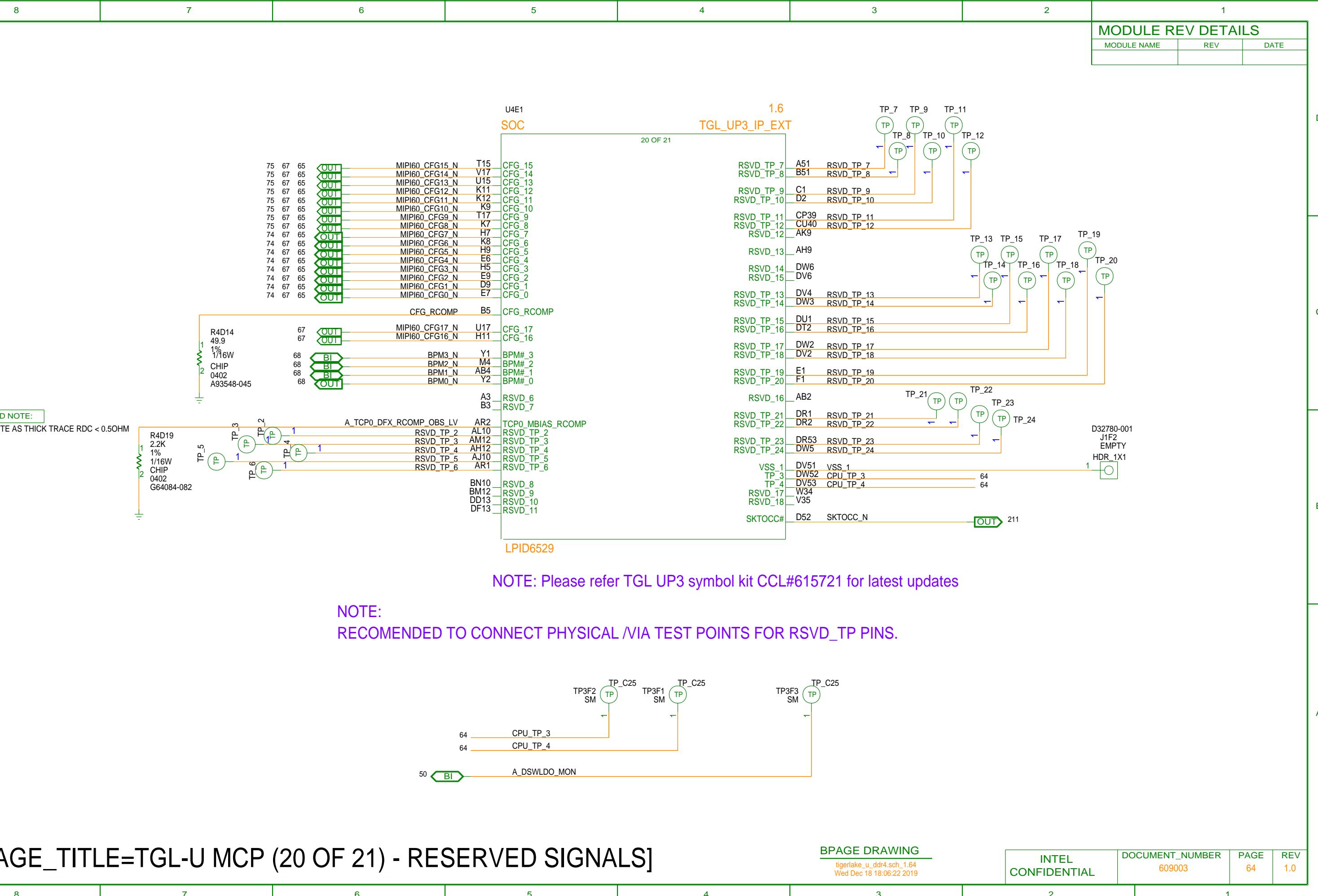
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|---------------------------|---|---|---|---|---|-------------|-----|------|
| 8                         | 7 | 6 | 5 | 4 | 3 | 2           | 1   |      |
| <b>MODULE REV DETAILS</b> |   |   |   |   |   | MODULE NAME | REV | DATE |



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

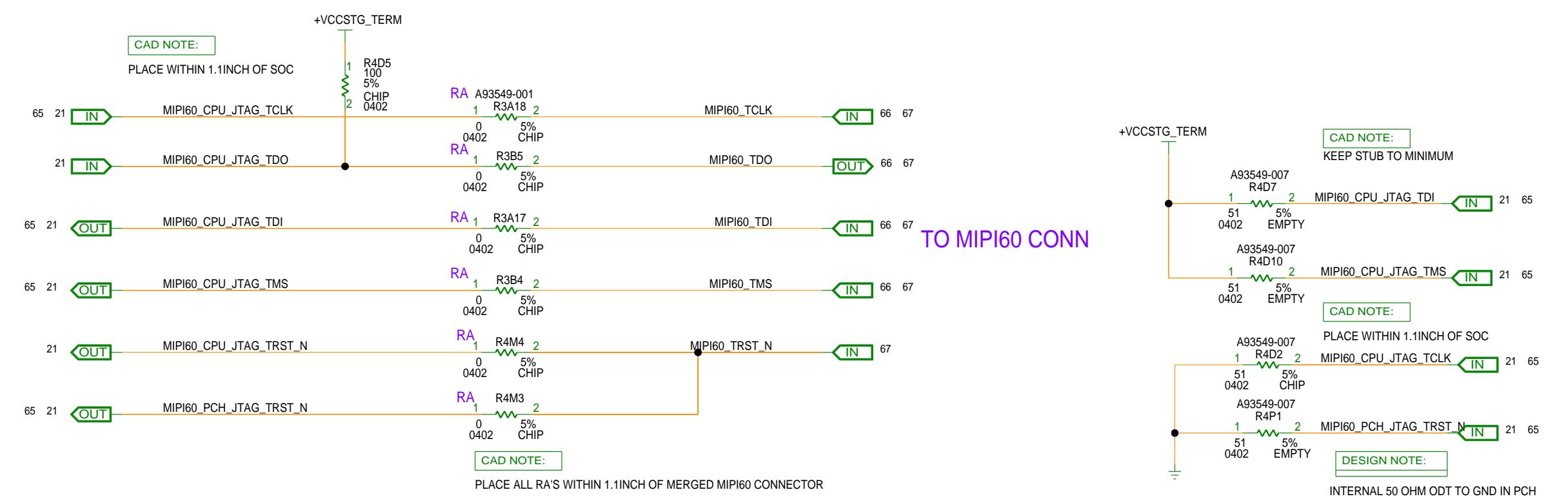
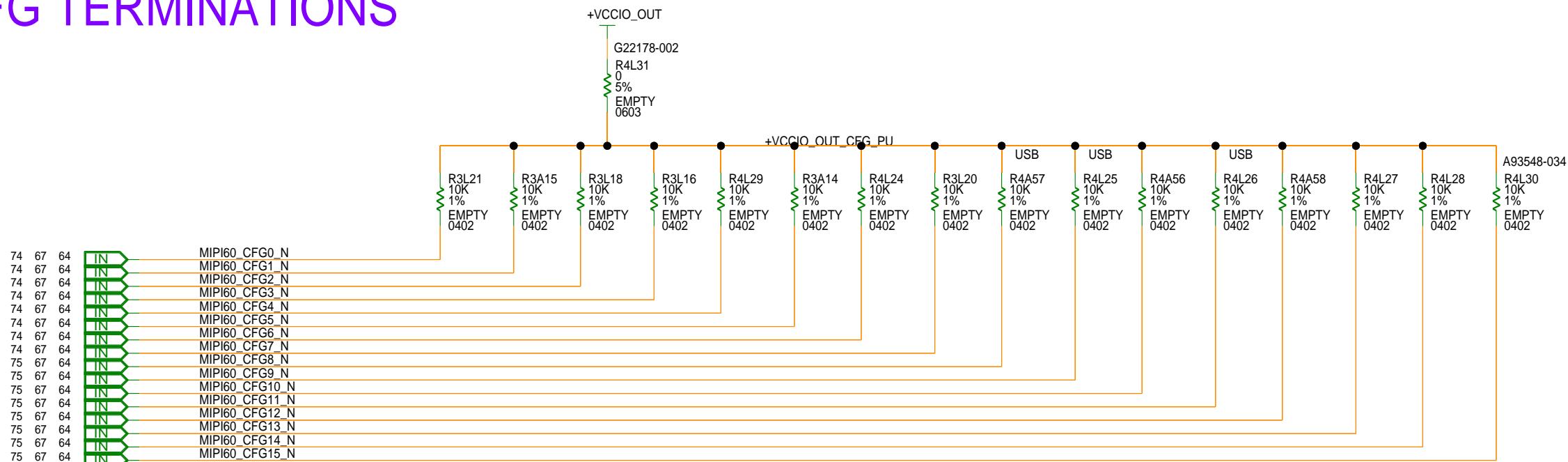
**NOTE:**

RECOMENDED TO CONNECT PHYSICAL /VIA TEST POINTS FOR RSVD\_TP PINS.



| 8                  | 7   | 6    | 5 | 4 | 3 | 2 | 1 |
|--------------------|-----|------|---|---|---|---|---|
| MODULE REV DETAILS |     |      |   |   |   |   |   |
| MODULE NAME        | REV | DATE |   |   |   |   |   |
|                    |     |      |   |   |   |   |   |

## CFG TERMINATIONS



[PAGE\_TITLE=JTAG/CFG - CFG TERMINATIONS]

BPAGE DRAWING

tigerlake\_u\_ddr4.sch\_1.65  
Wed Dec 18 18:06:23 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
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|                       | 609003          | 65   | 1.0 |

CUSTOM TEXT BPAGE

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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| MODULE REV DETAILS |     |      |
|--------------------|-----|------|
| MODULE NAME        | REV | DATE |
|                    |     |      |

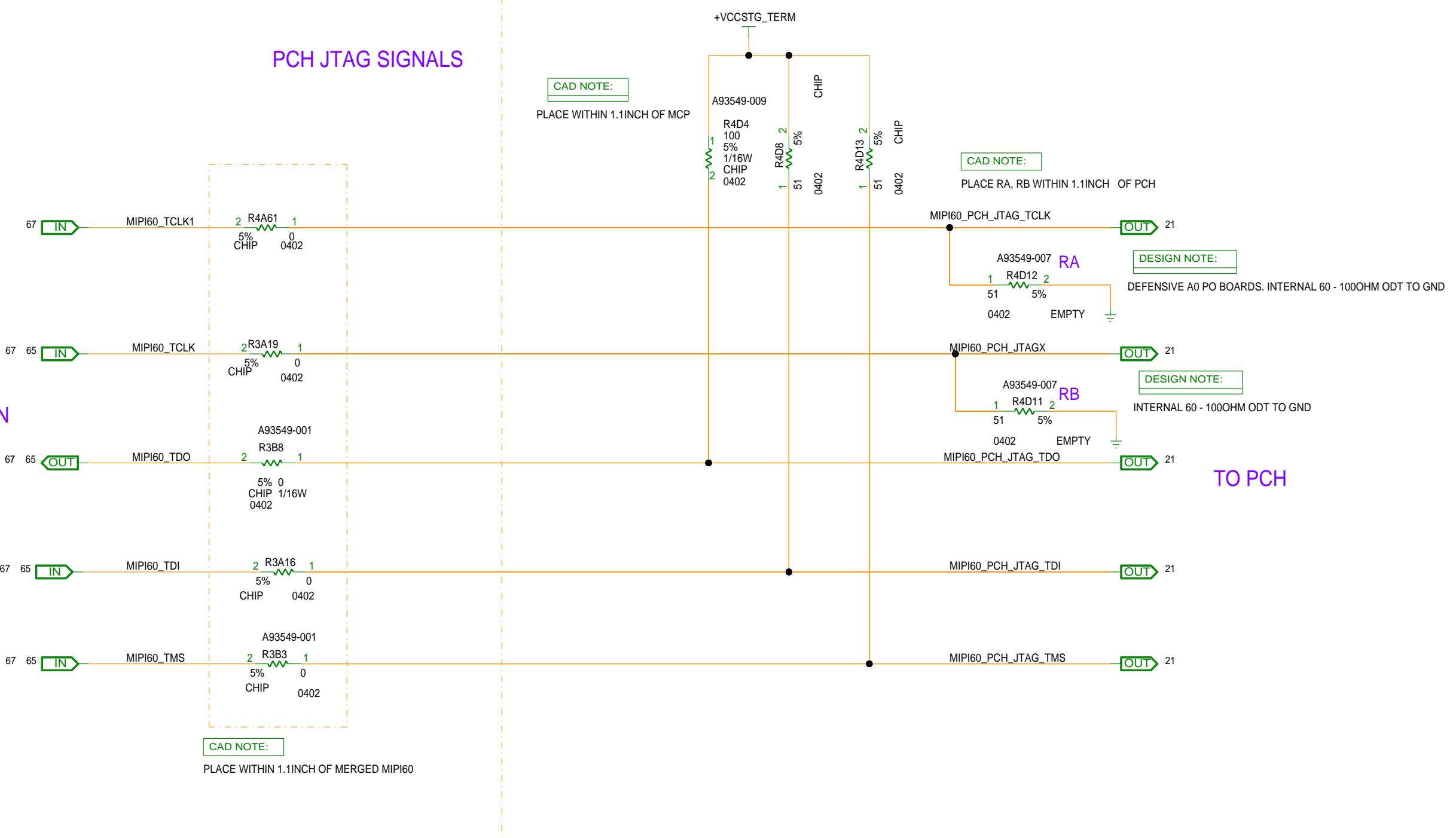
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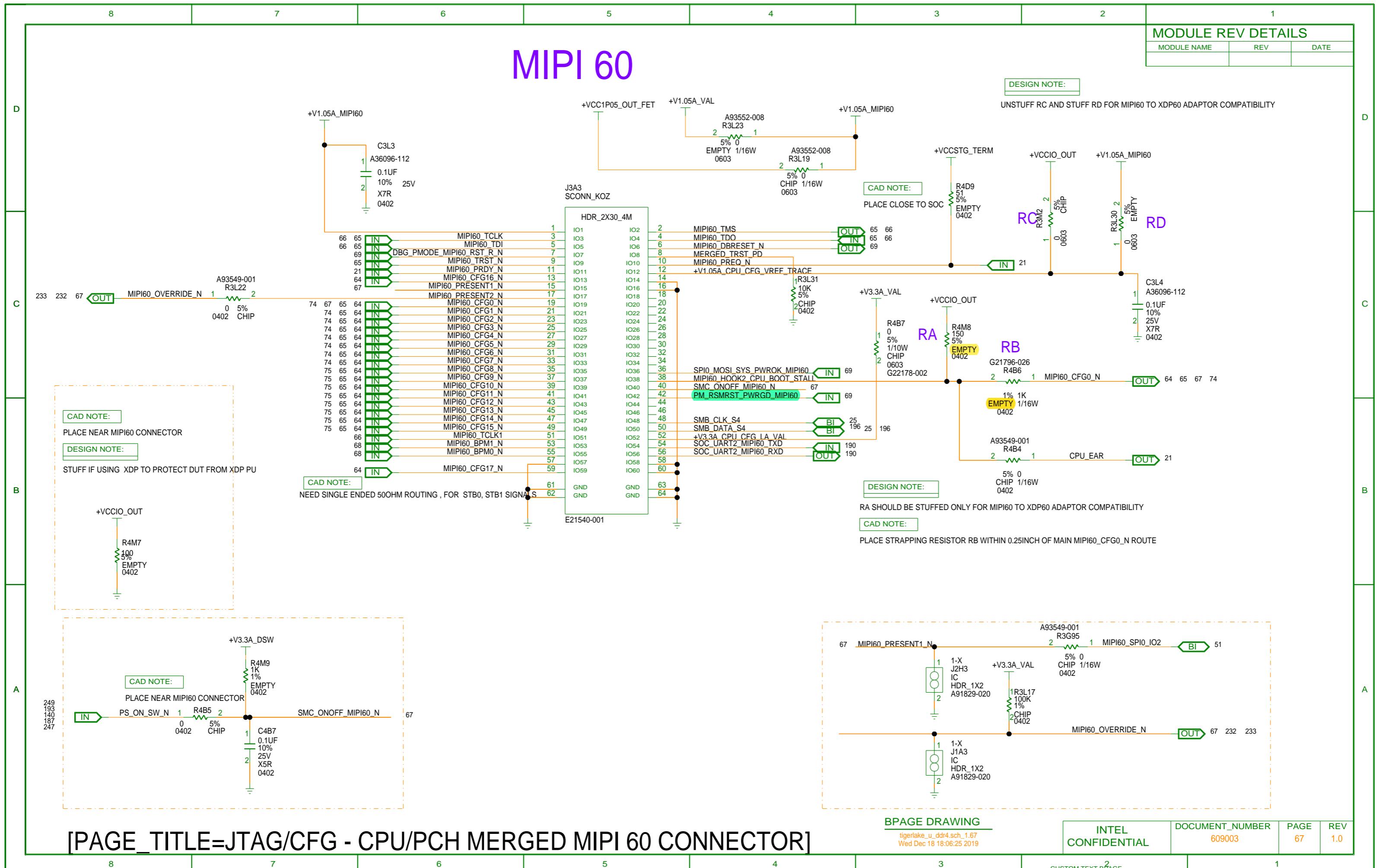
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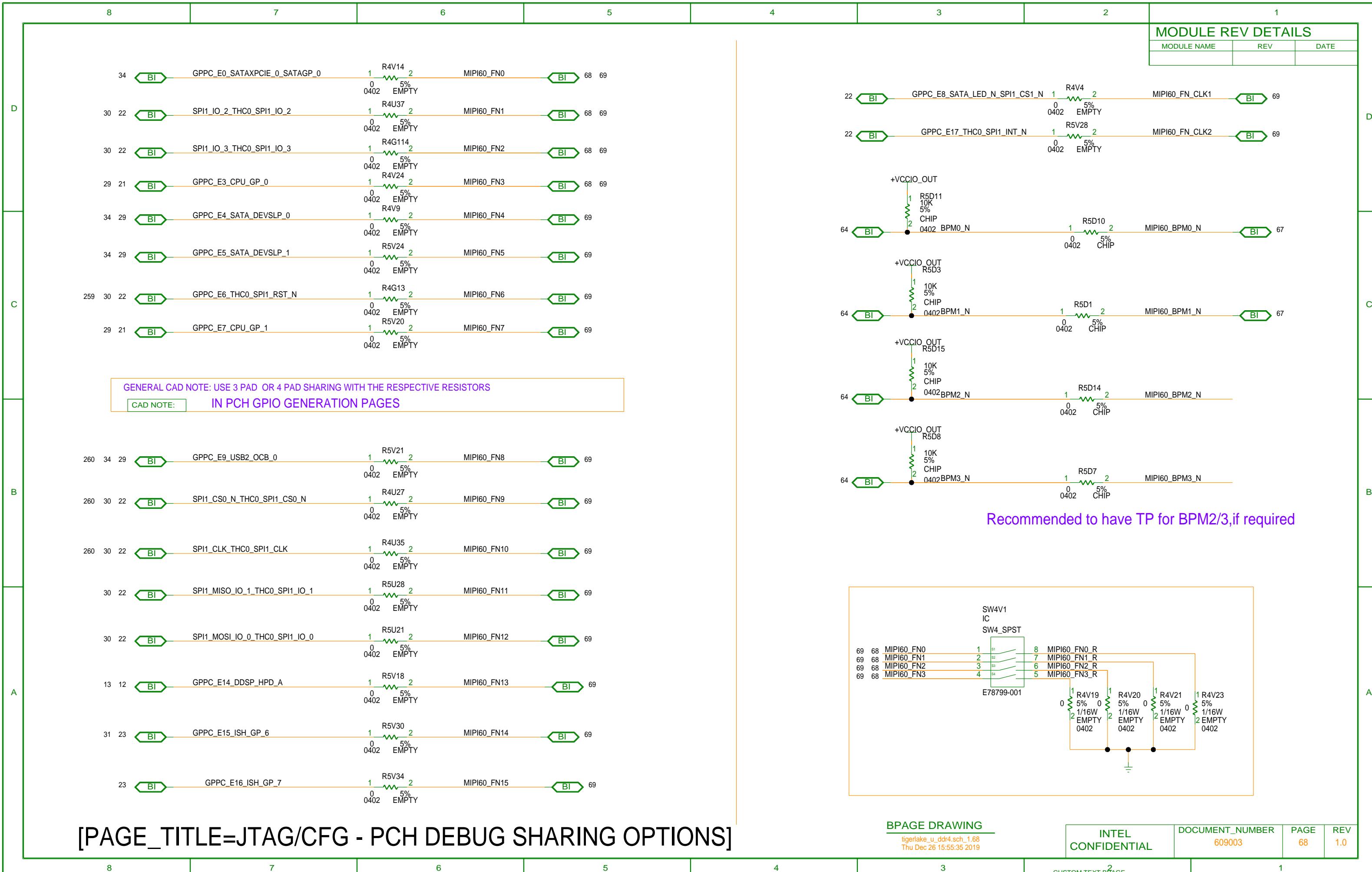
## PCH JTAG SIGNALS

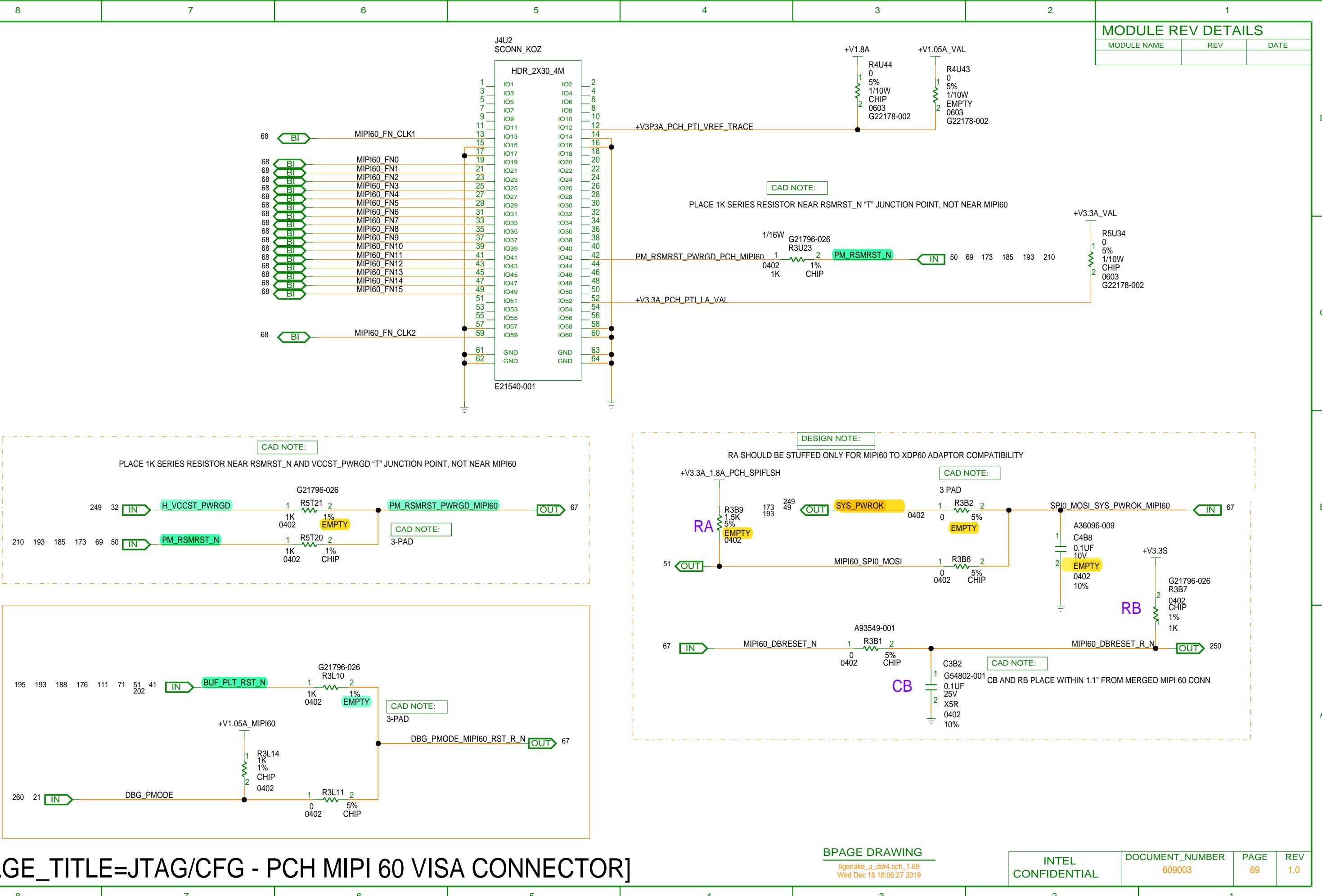
### TO MIPI60 CONN

### TO PCH







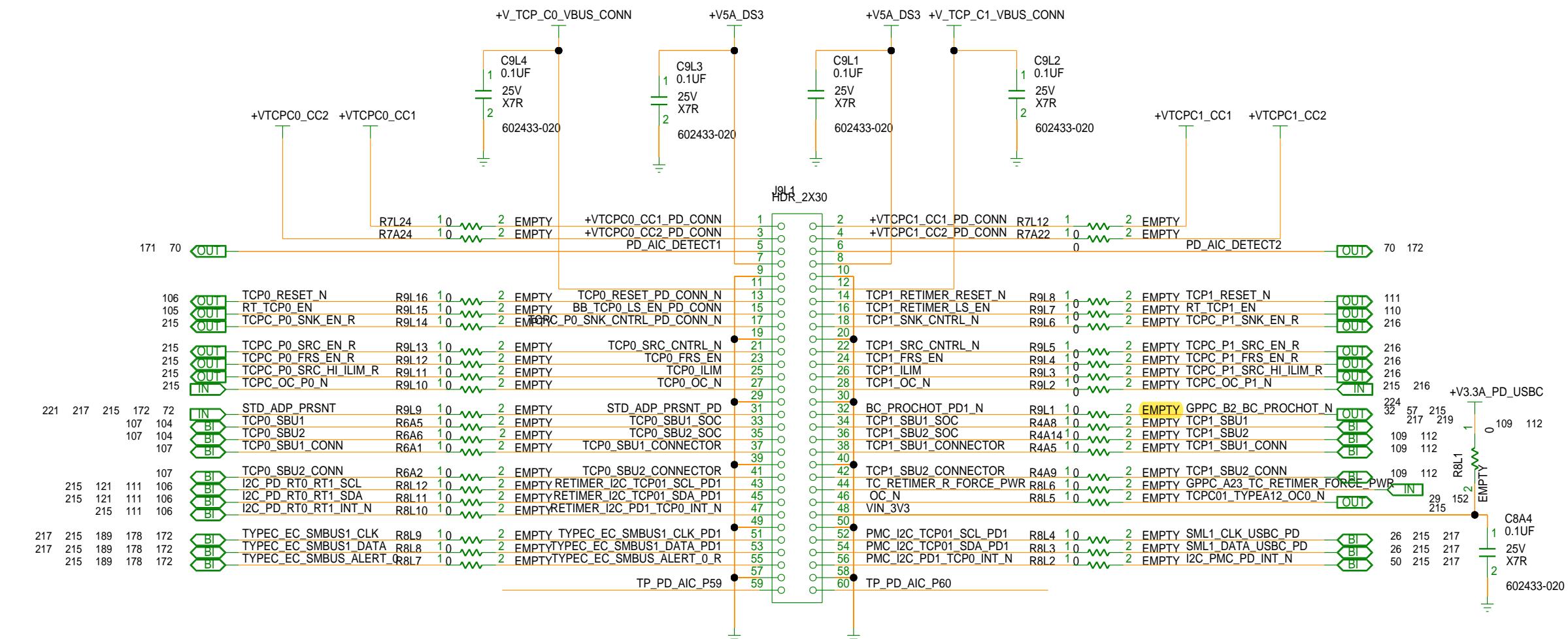


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|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|

# PD AIC CONTROLLER

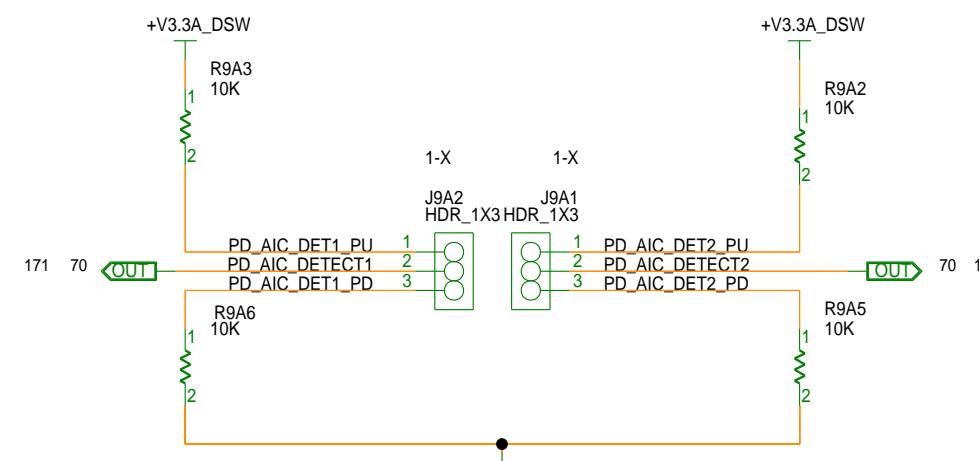
## MODULE REV DETAILS

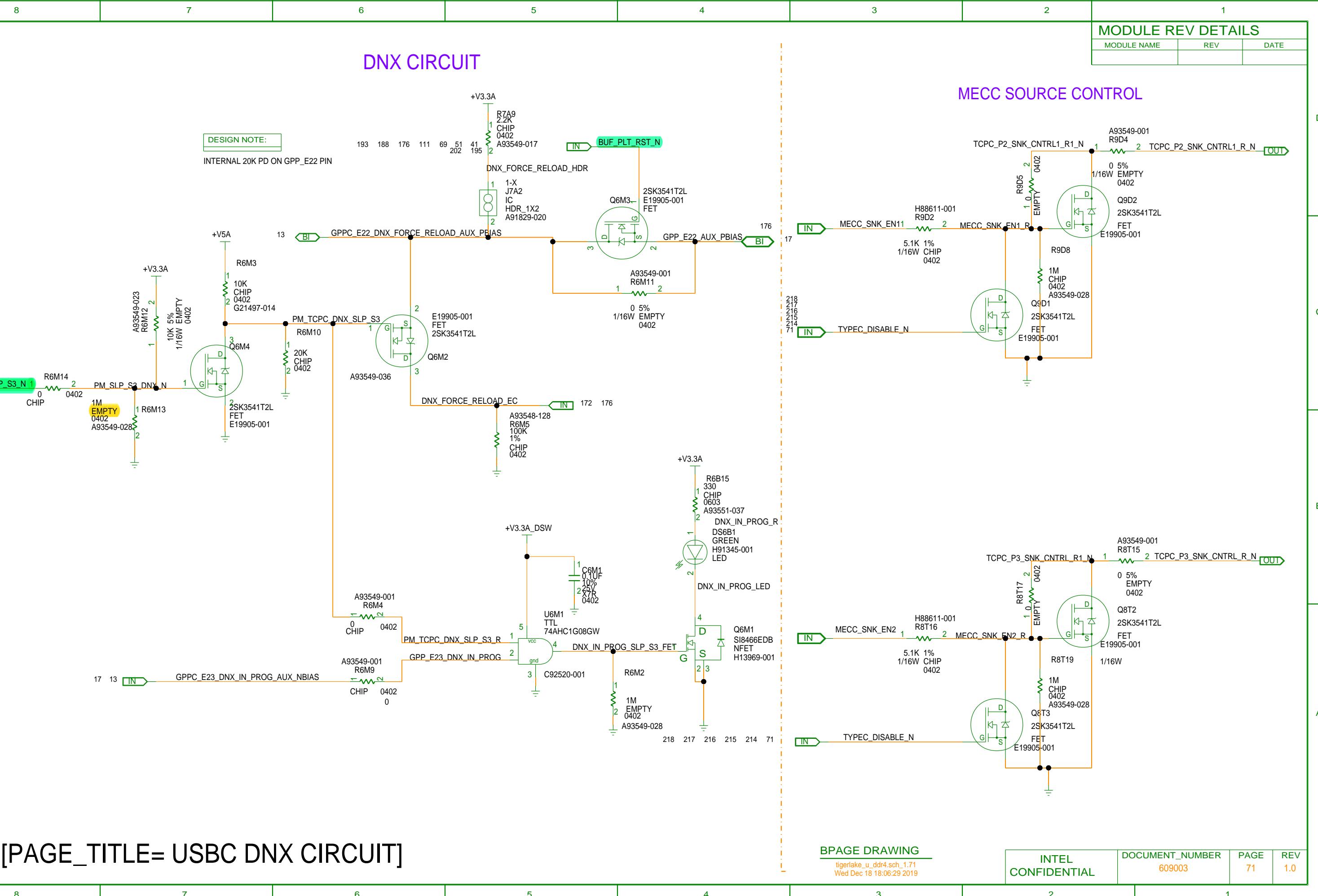
| MODULE NAME | REV | DATE |
|-------------|-----|------|
|             |     |      |

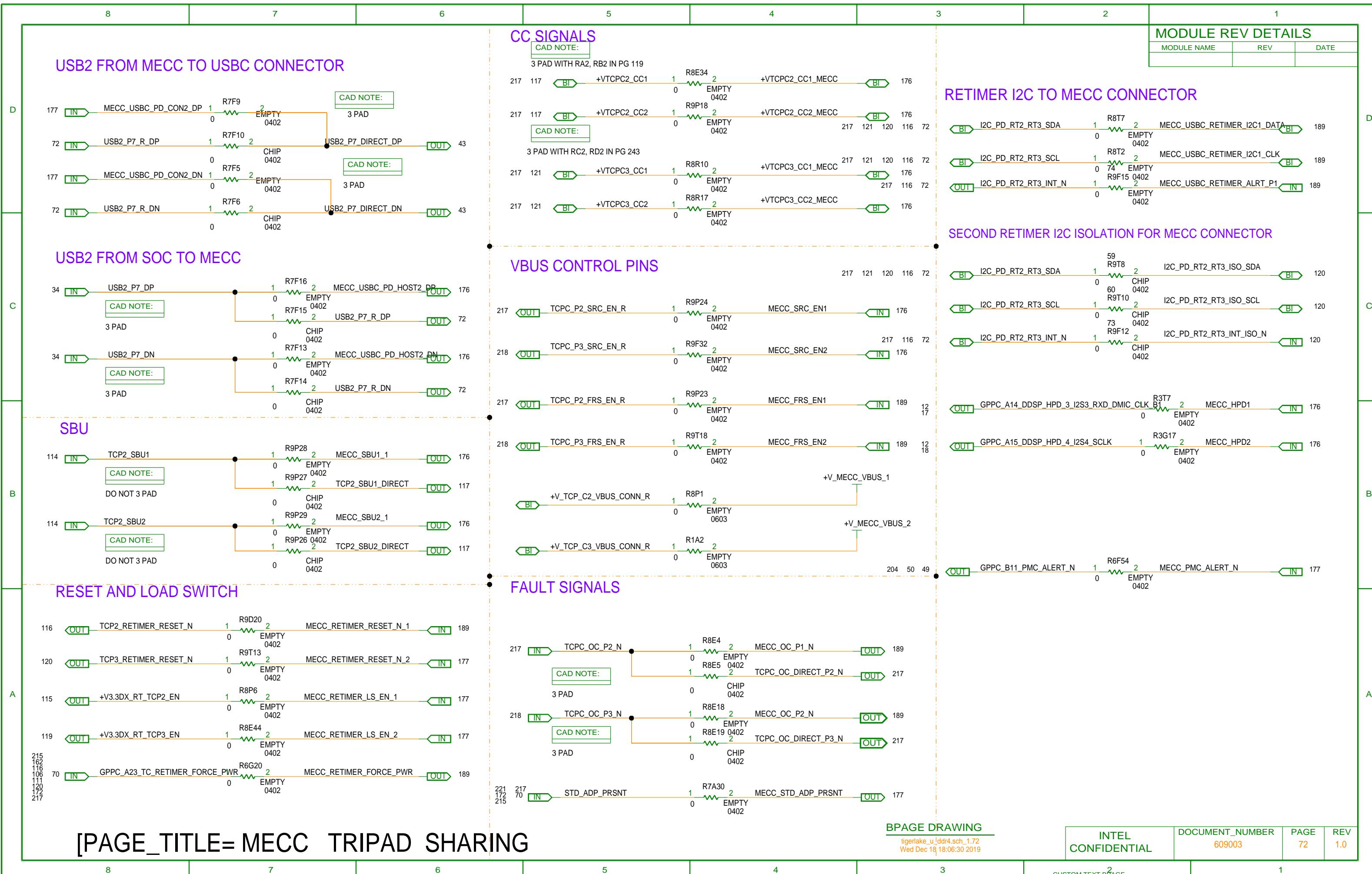


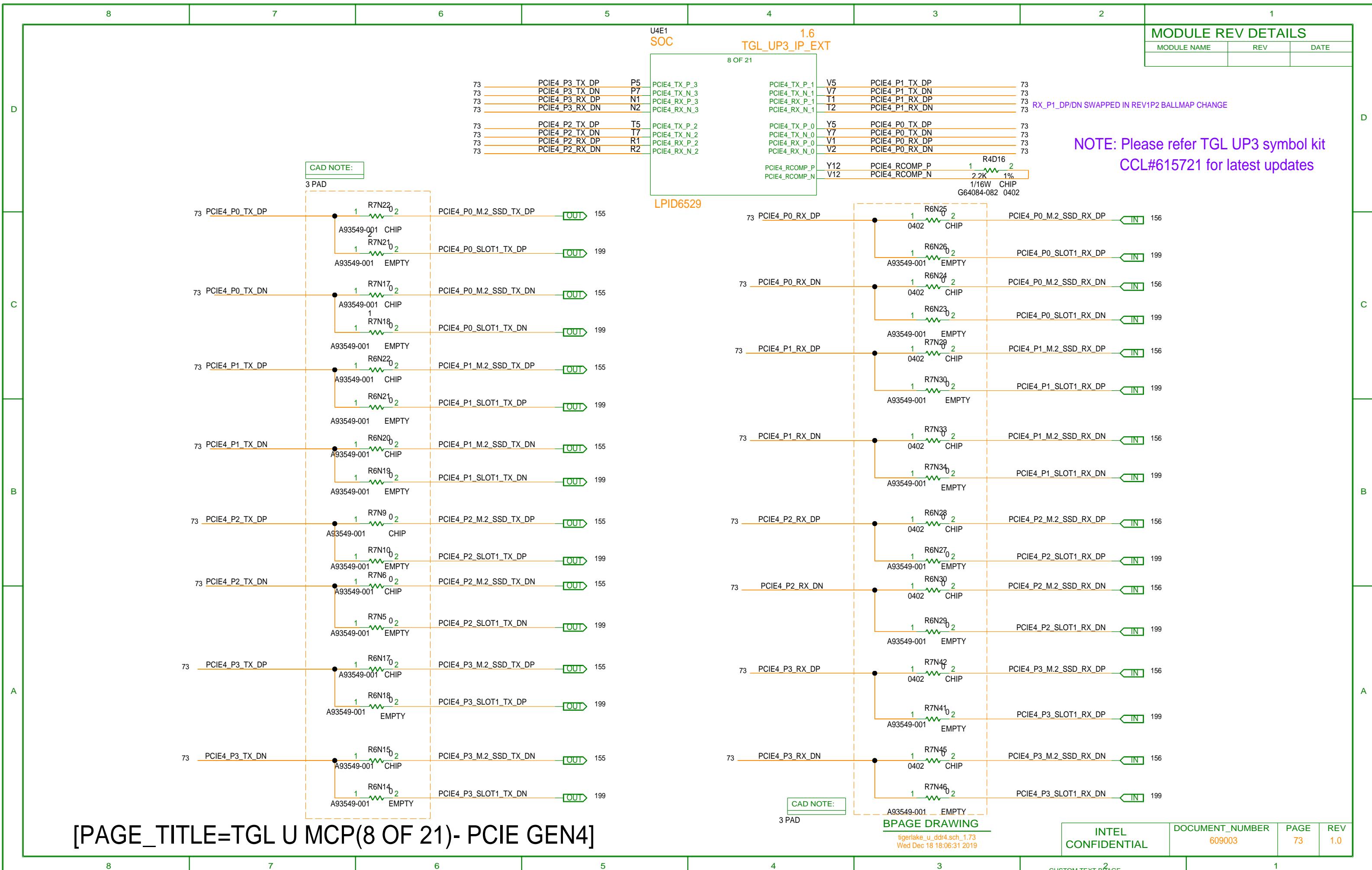
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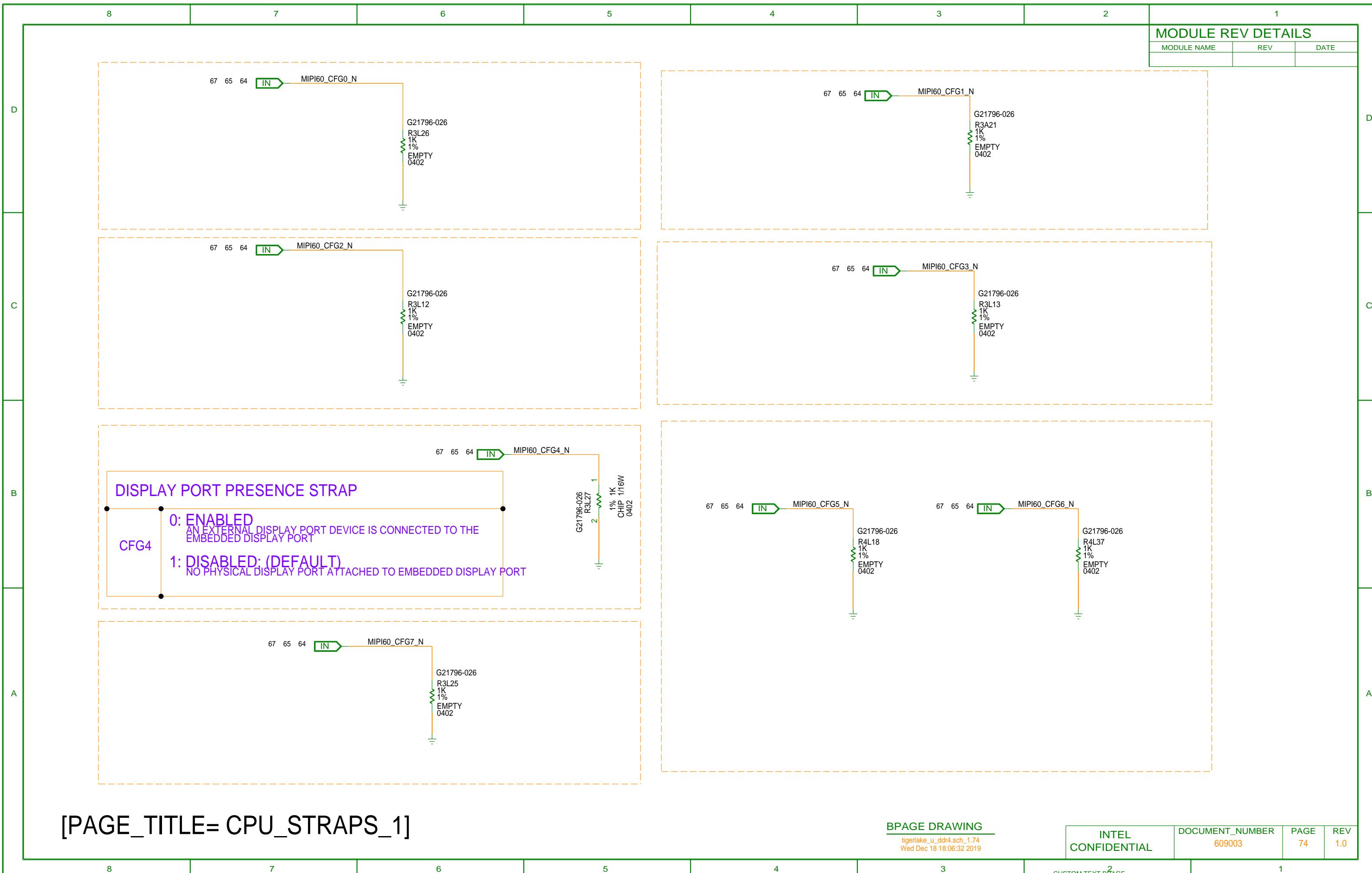
ALL THE RESISTORS IN THIS PAGE SHOULD BE TRIPAD WITH RESPECTIVE RESISTOR IN OTHER SECTION

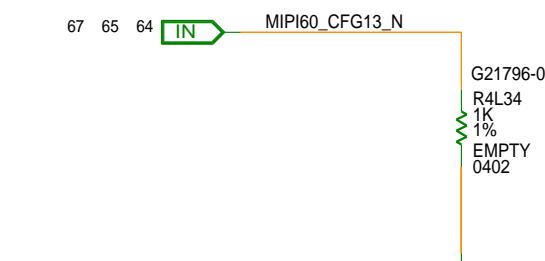
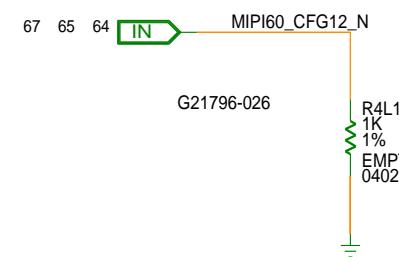
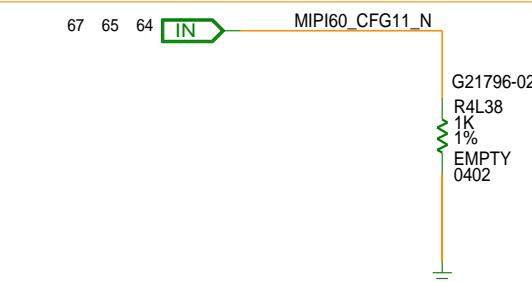
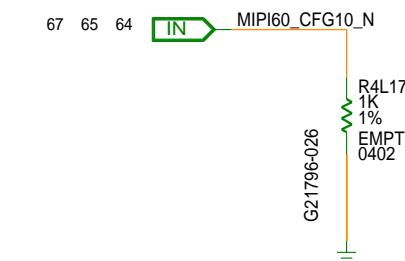
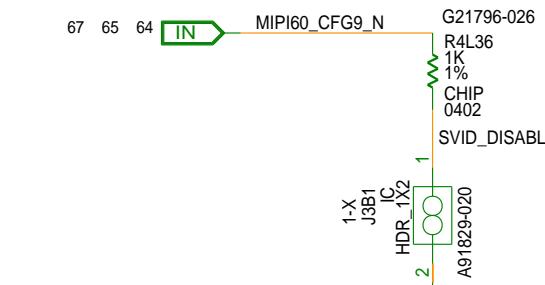
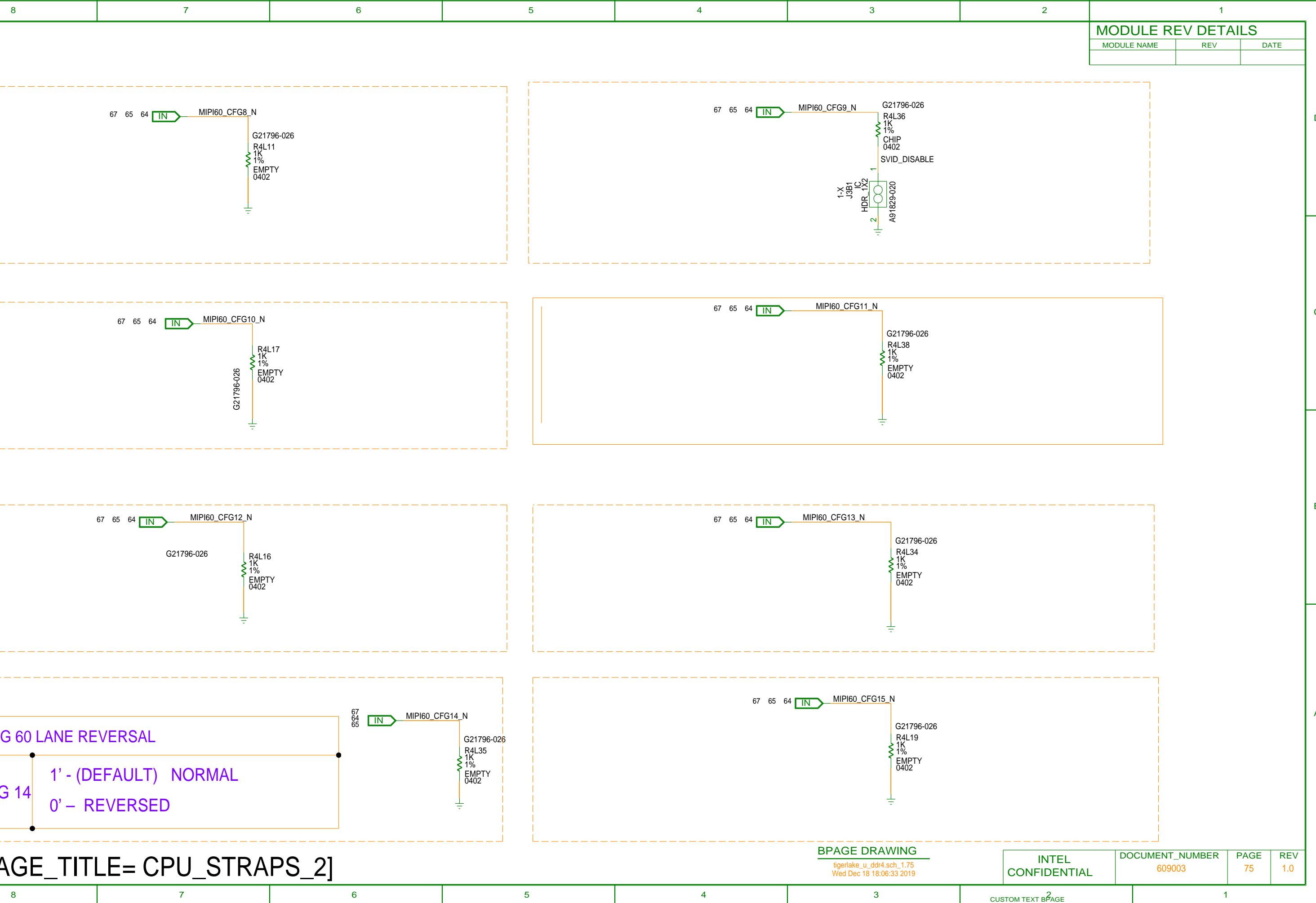












PEG 60 LANE REVERSAL  
1' - (DEFAULT) NORMAL  
0' – REVERSED  
CFG 14

[PAGE\_TITLE= CPU\_STRAPS\_2]

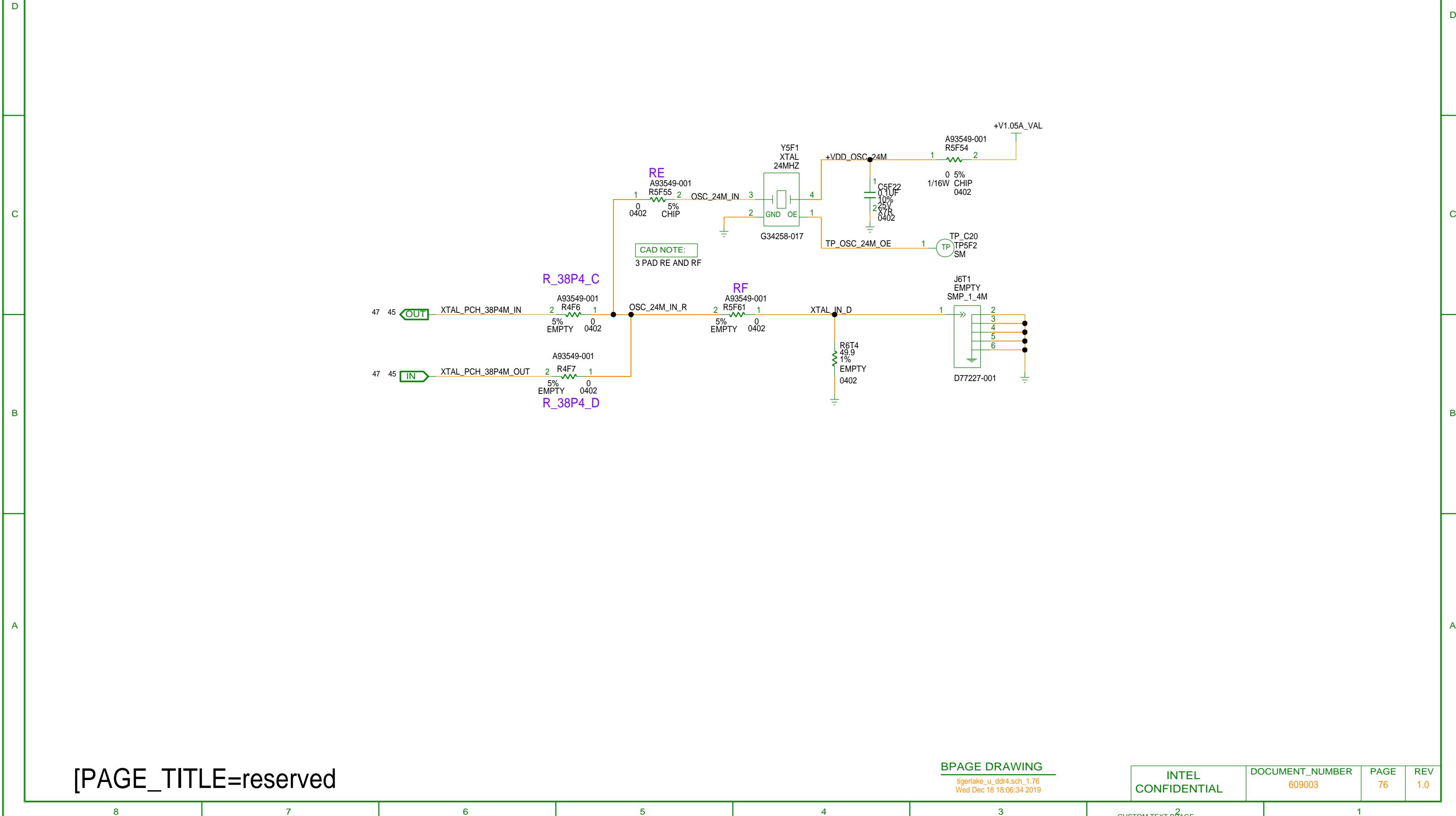
BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.75  
Wed Dec 18 18:06:33 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>75 | REV<br>1.0 |
|-----------------------|---------------------------|------------|------------|
|                       |                           |            |            |

CUSTOM TEXT BPAGE

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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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| MODULE REV DETAILS |     |      |
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| MODULE NAME        | REV | DATE |
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[PAGE\_TITLE=reserved]

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tigerlake\_u\_ddr4.sch\_1.76  
Wed Dec 18 18:06:34 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
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|                       | 609003          | 76   | 1.0 |

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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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CUSTOM TEXT BPAGE

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| MODULE REV DETAILS |     |      |
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[PAGE\_TITLE=RESERVE]

BPAGE DRAWING  
 tigerlake\_u\_ddr4.sch\_1.77  
 Tue Oct 15 12:49:33 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
|-----------------------|-----------------|------|-----|
|                       | 609003          | 77   | 1.0 |

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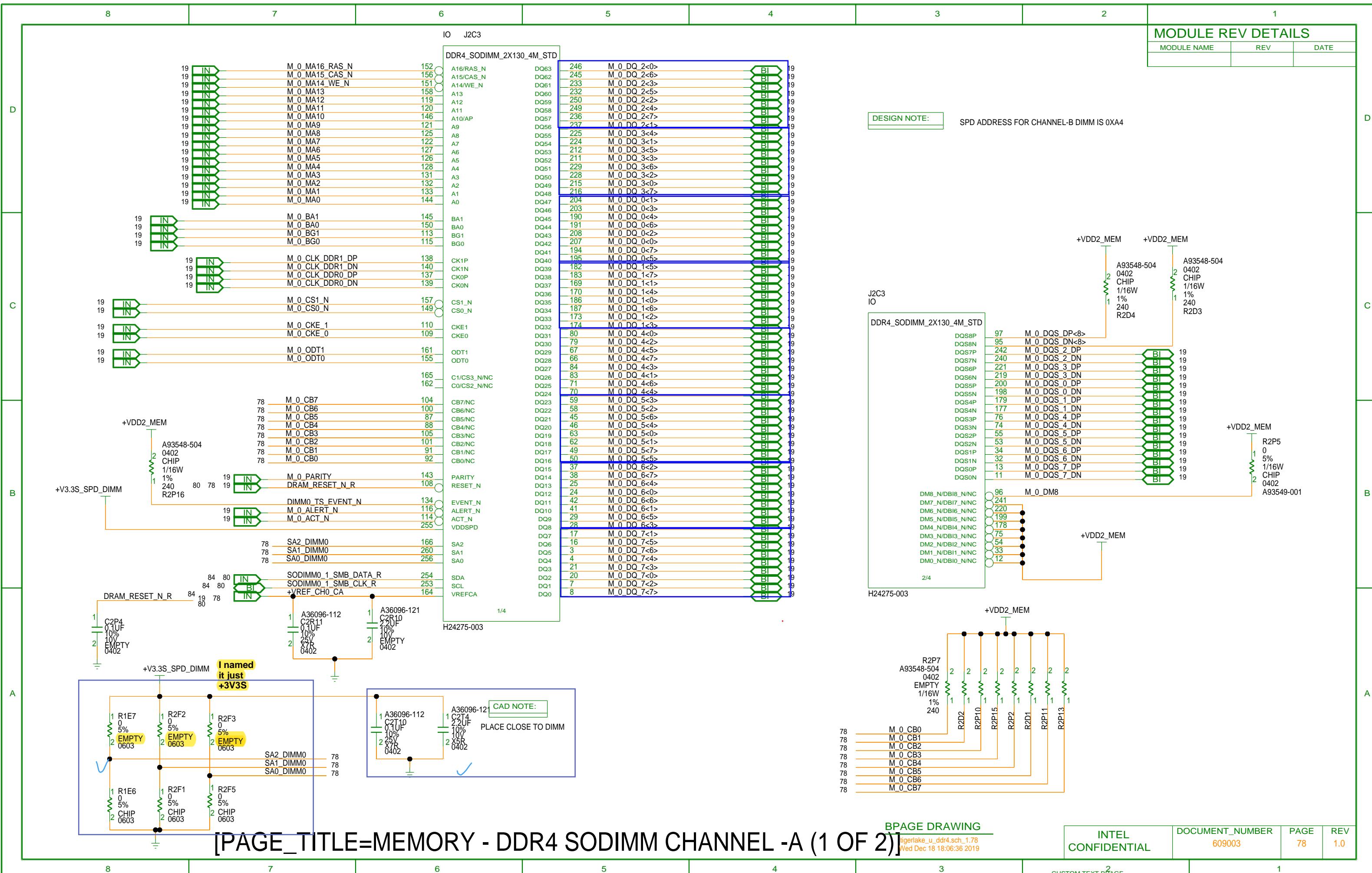
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CUSTOM TEXT 2 PAGE

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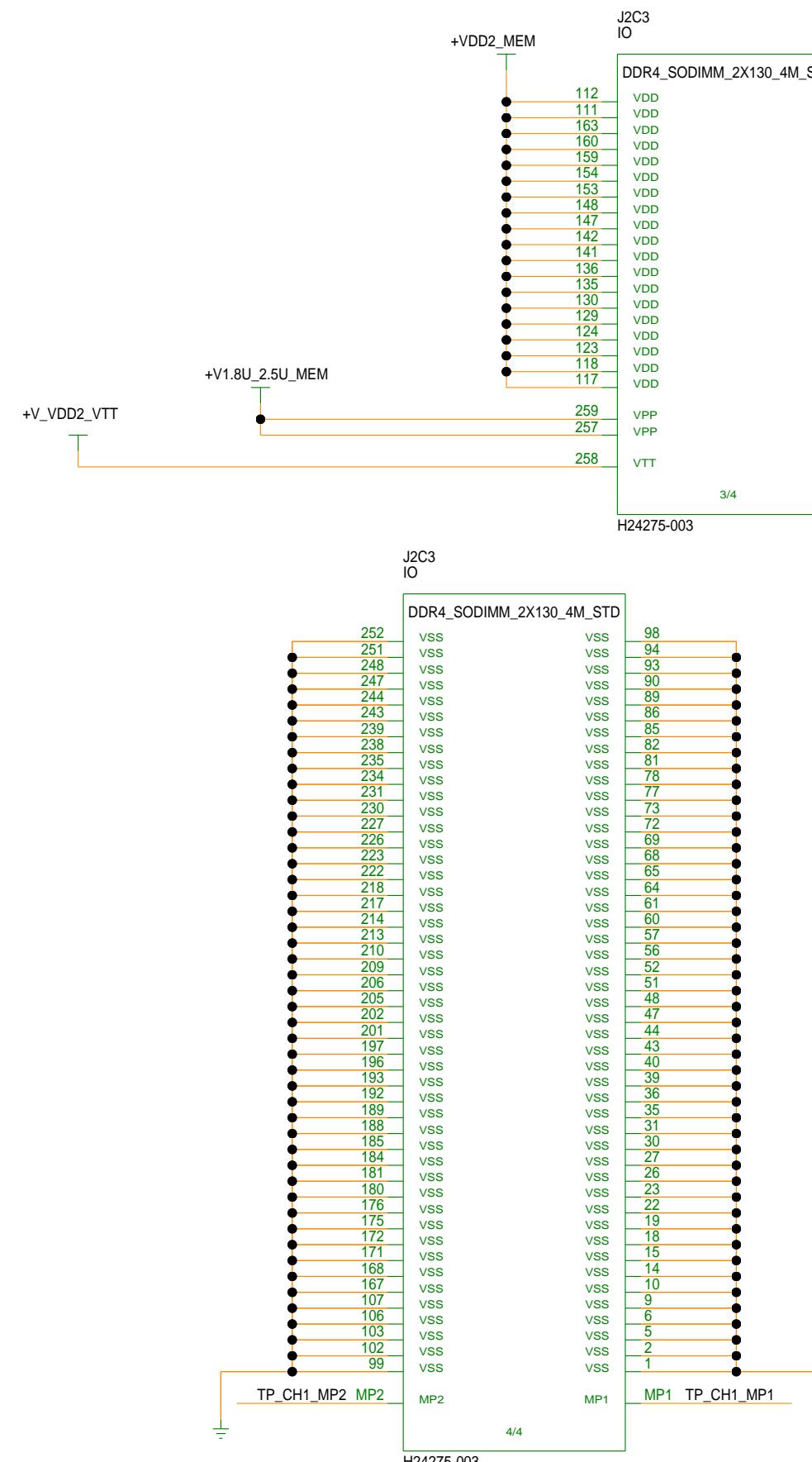
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**MODULE REV DETAILS**

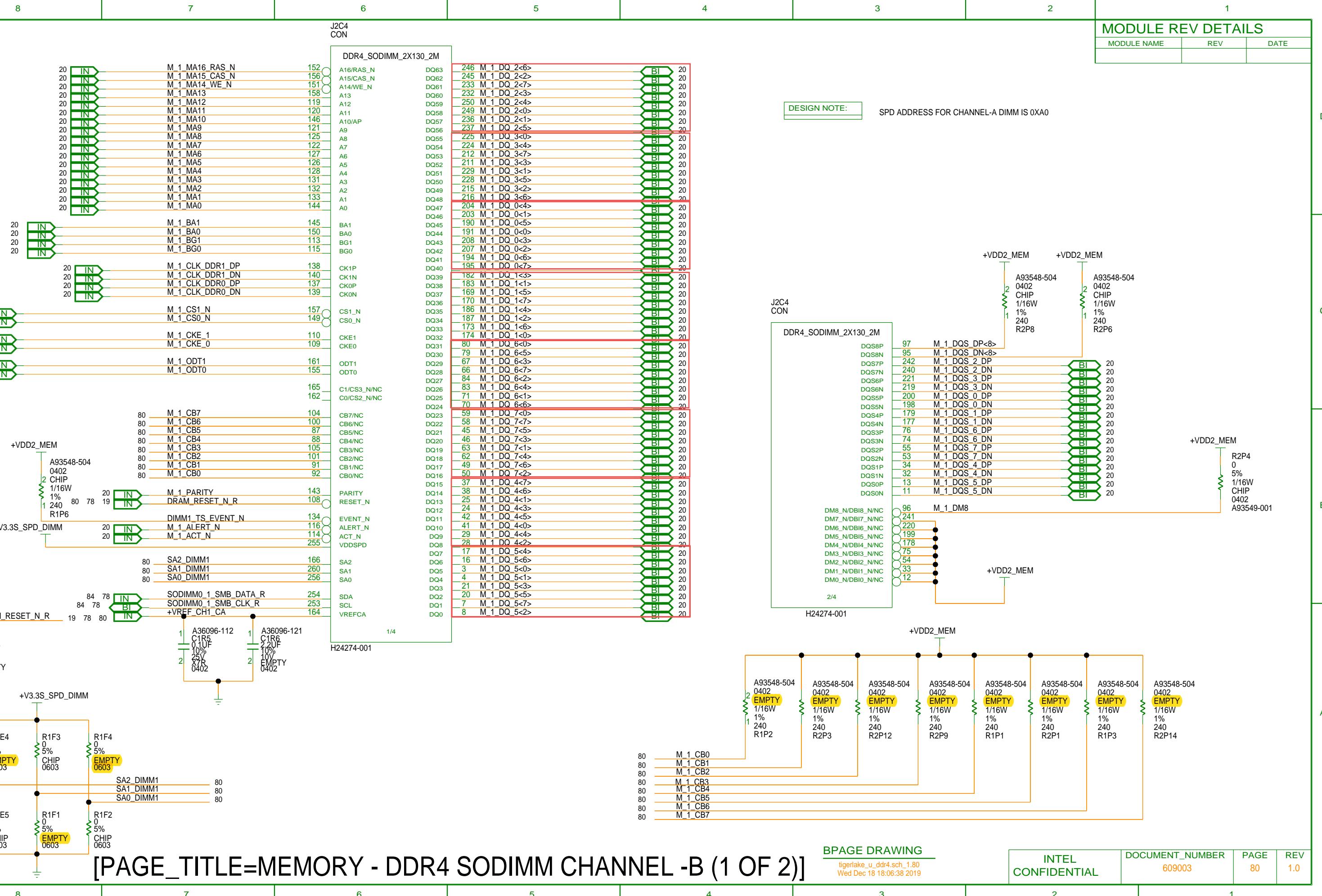
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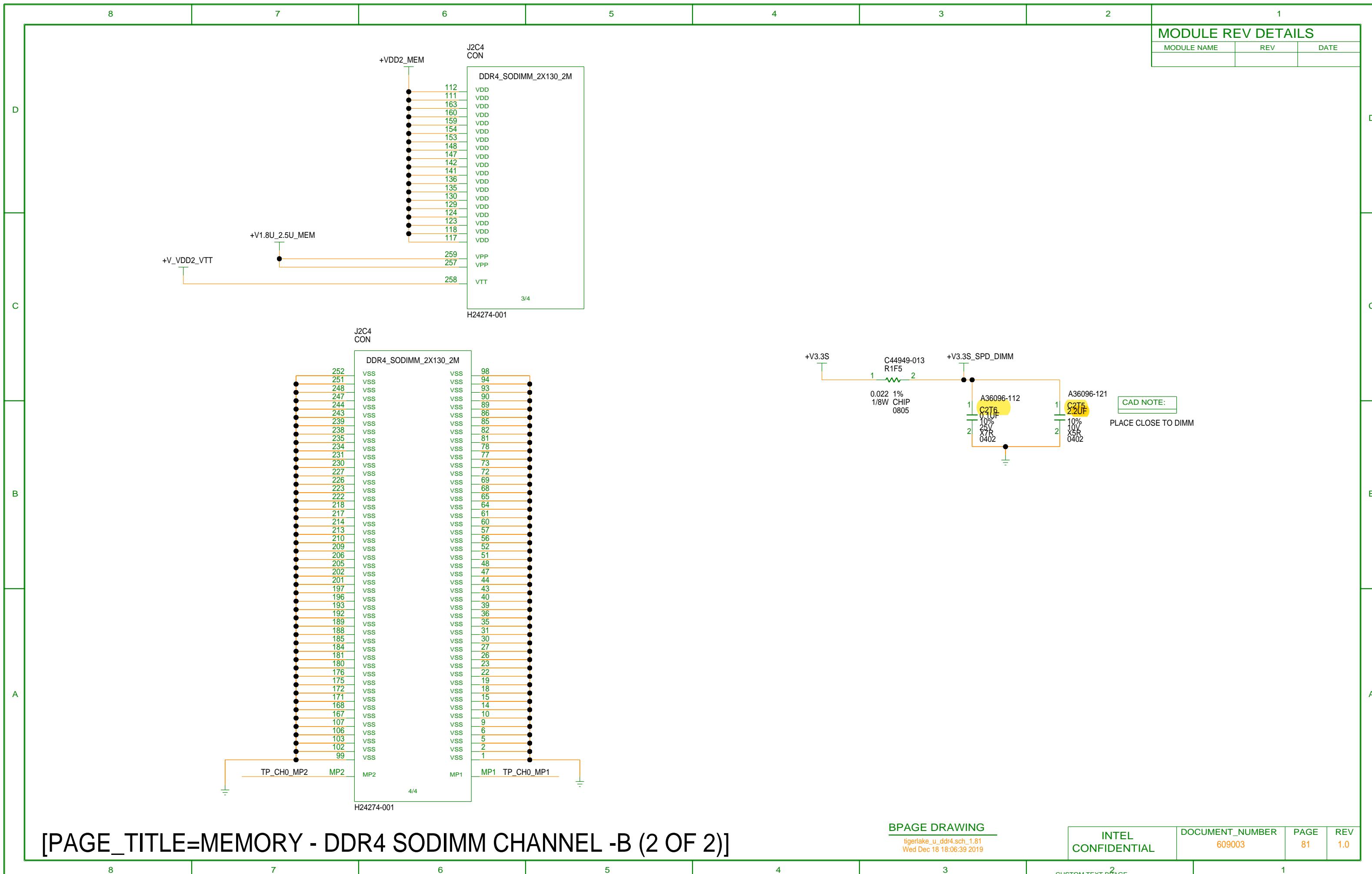


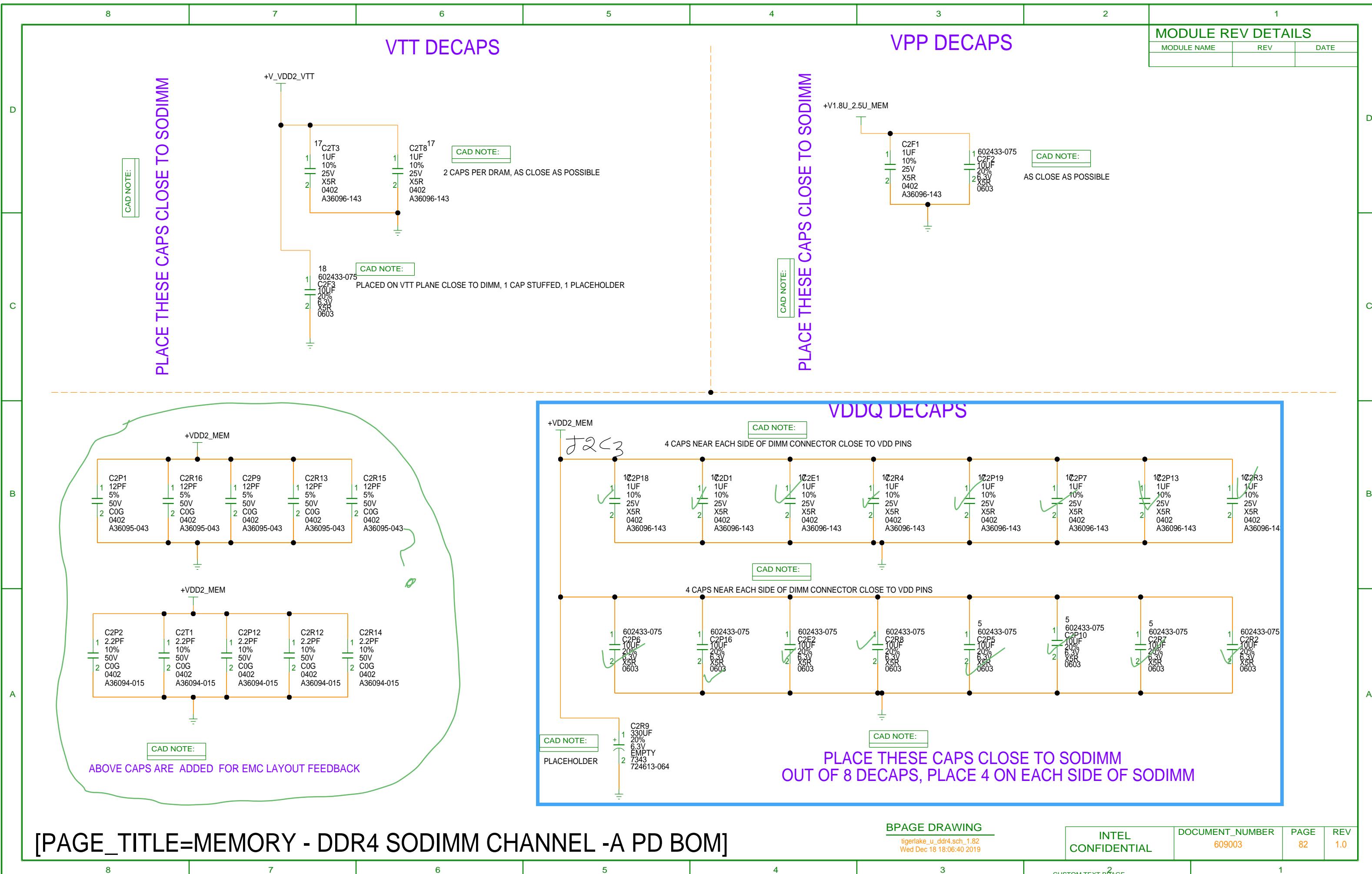
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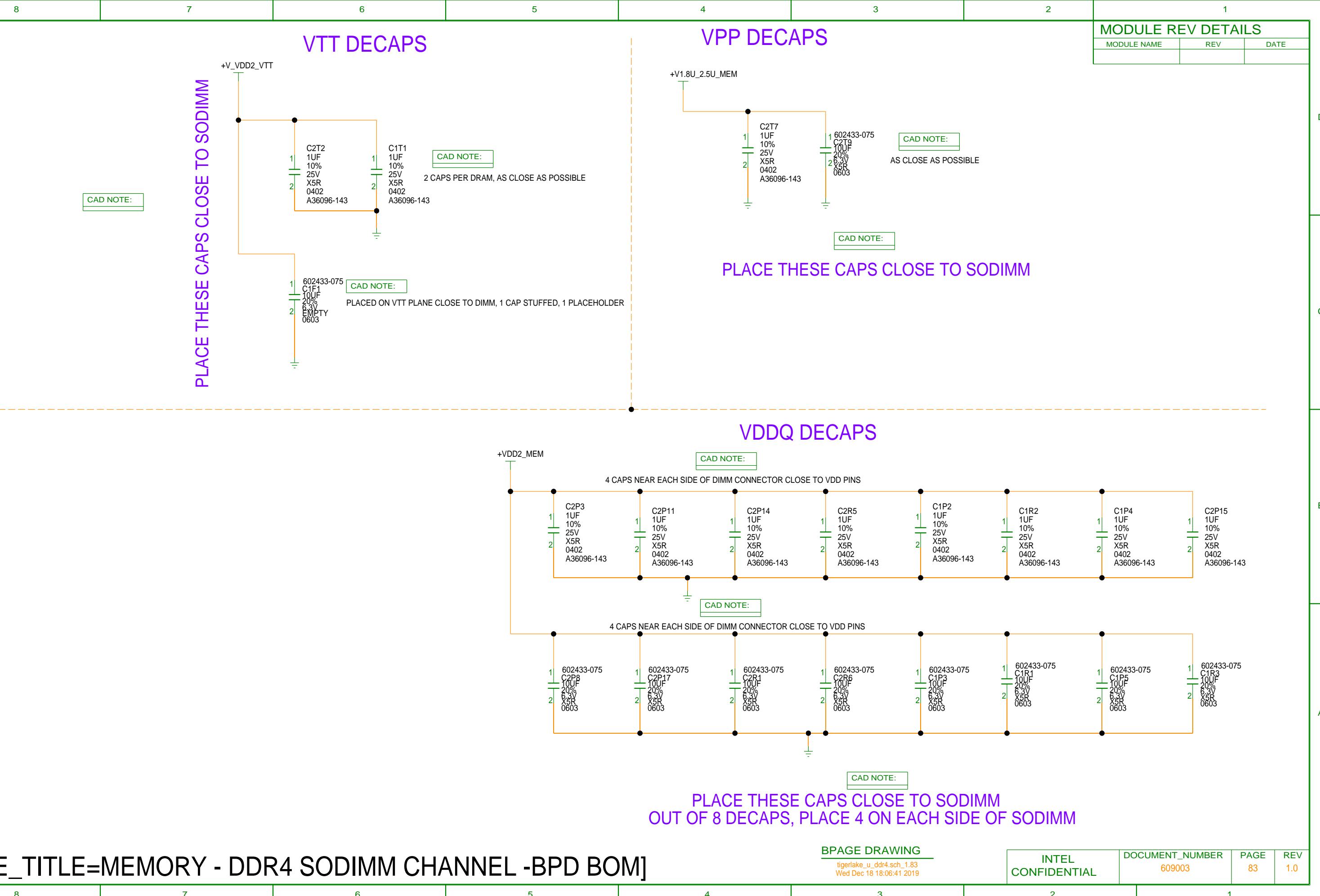
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Wed Dec 18 18:06:37 2019

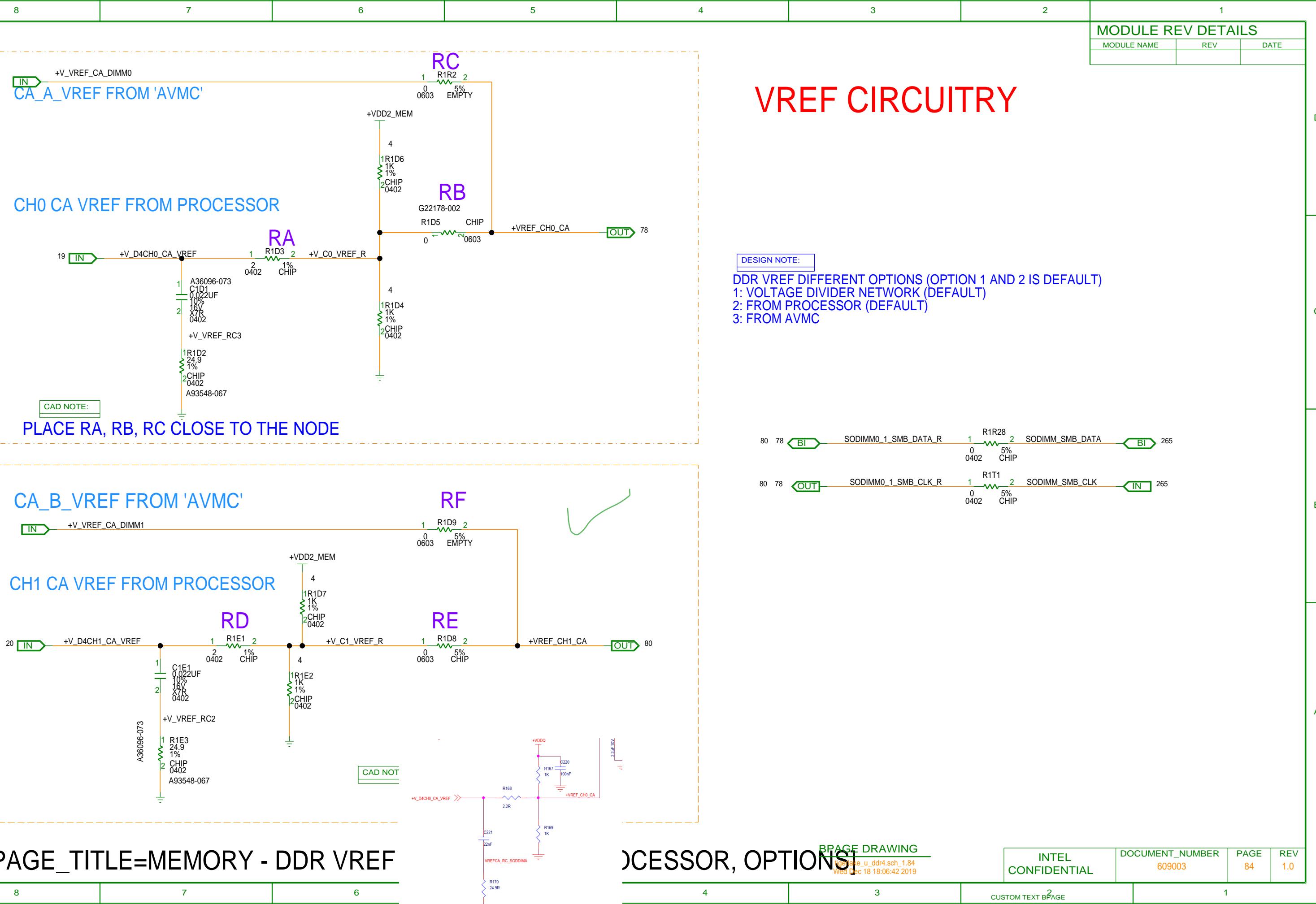
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**MODULE REV DETAILS**

| MODULE NAME | REV | DATE |
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**[PAGE\_TITLE=MEMORY - RESERVE]**

BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.85  
Tue Oct 15 12:49:41 2019

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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>85 | REV<br>1.0 |
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CUSTOM TEXT  
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**MODULE REV DETAILS**

| MODULE NAME | REV | DATE |
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[PAGE\_TITLE=]RESERVED

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tigerlake\_u\_ddr4.sch\_1.86  
Wed Dec 18 16:29:20 2019

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|-----------------------|---------------------------|------------|------------|
| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>86 | REV<br>1.0 |
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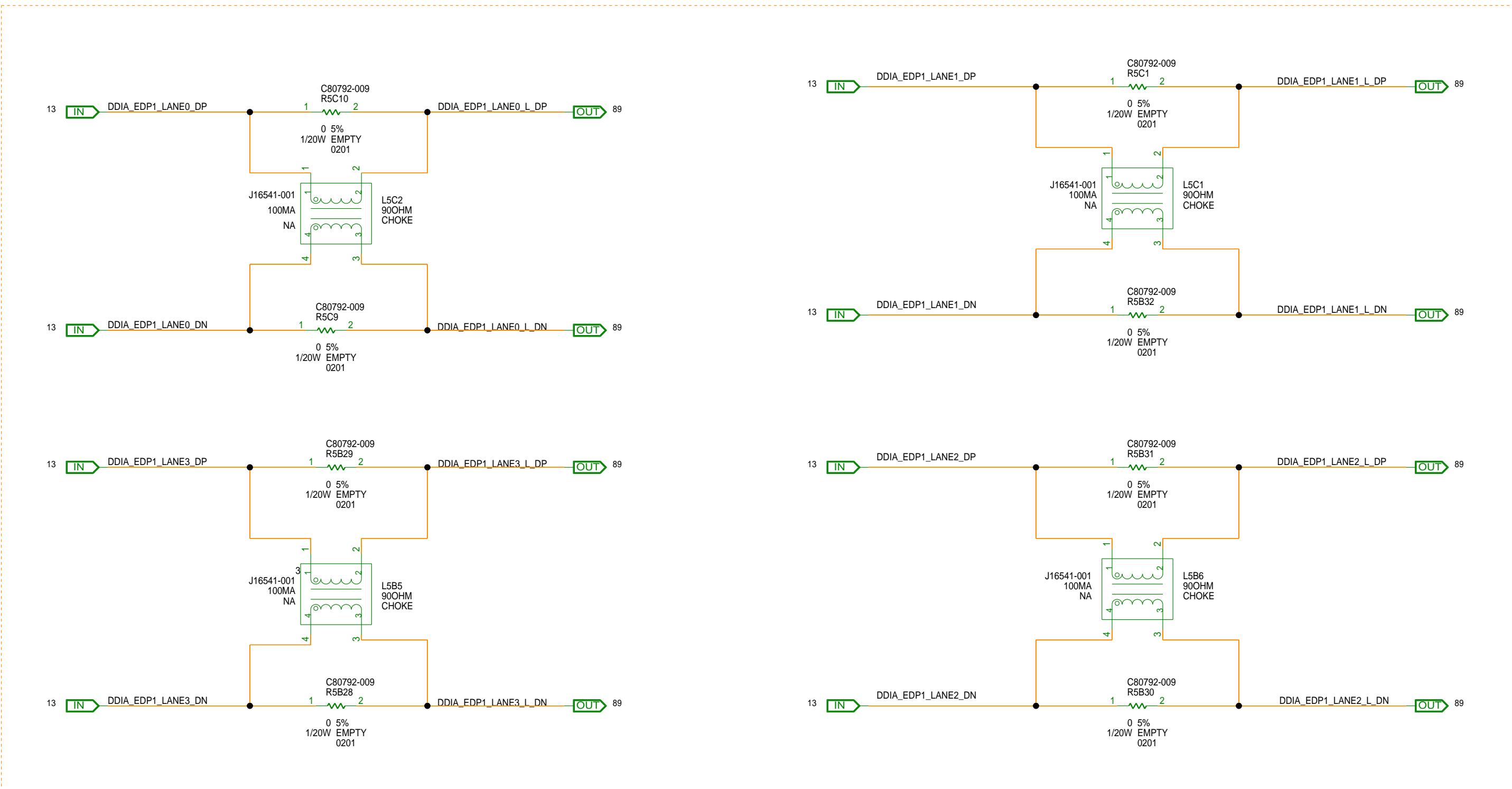
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CUSTOM TEXT  
2 PAGE

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| 8                  | 7   | 6    | 5 | 4 | 3 | 2 | 1 |
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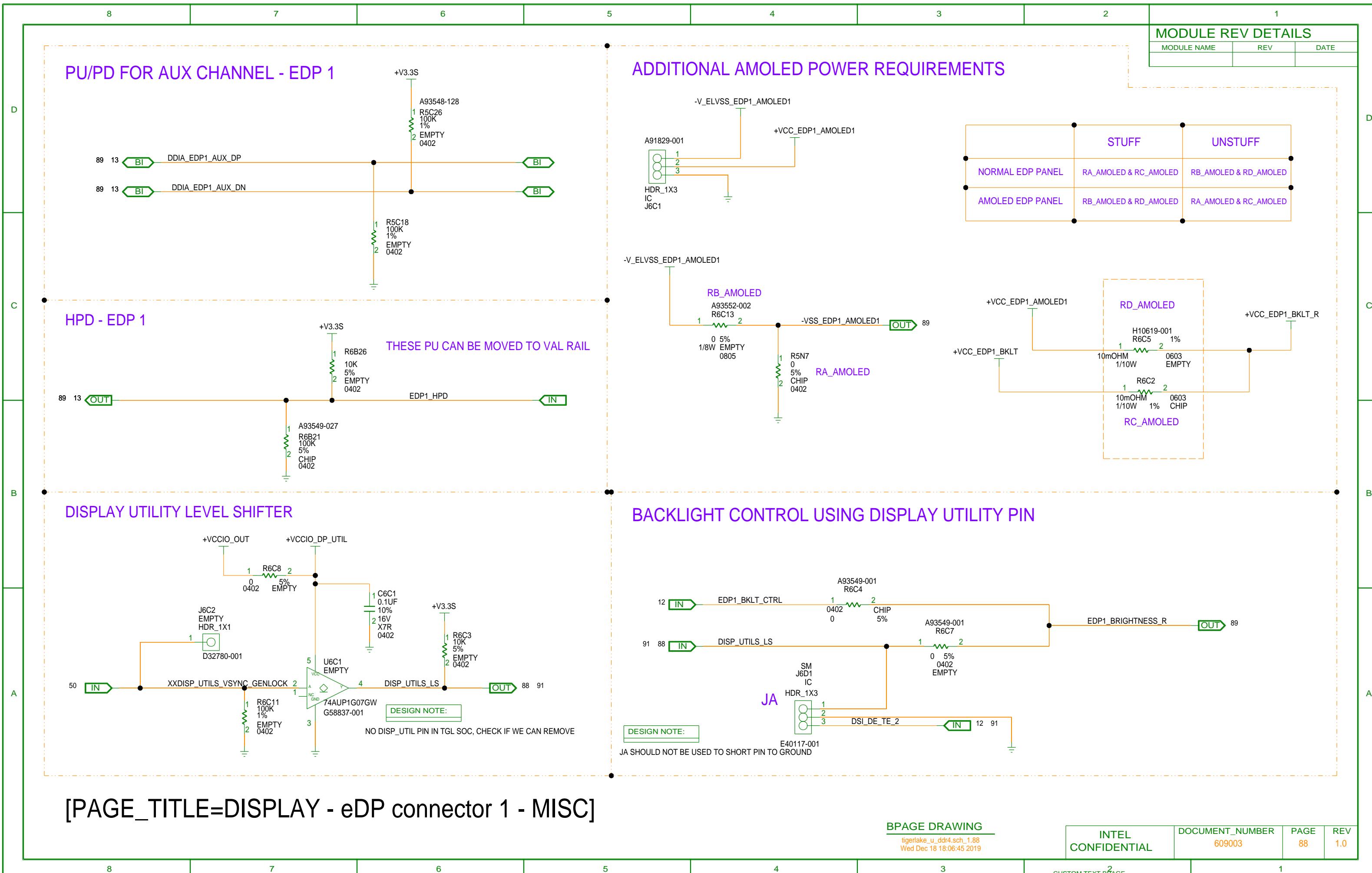
# EDP CONNECTOR 1 - CMC



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Tue Oct 15 12:49:42 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>87 | REV<br>1.0 |
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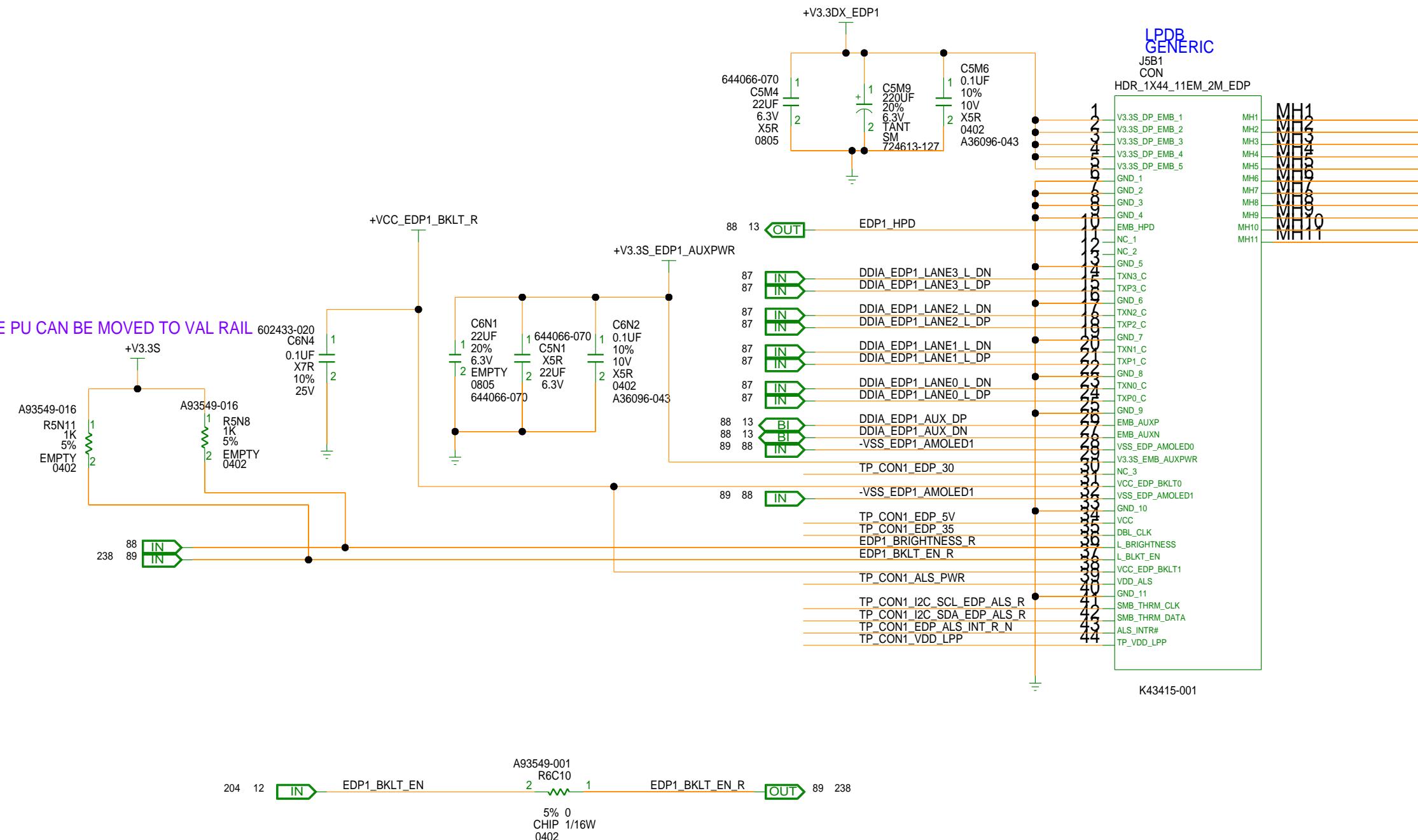
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# EDP CONNECTOR 1

CHANGE TANT CAP TO LOWER VALUE

THESE PU CAN BE MOVED TO VAL RAIL



[PAGE\_TITLE=DISPLAY - eDP connector 1]

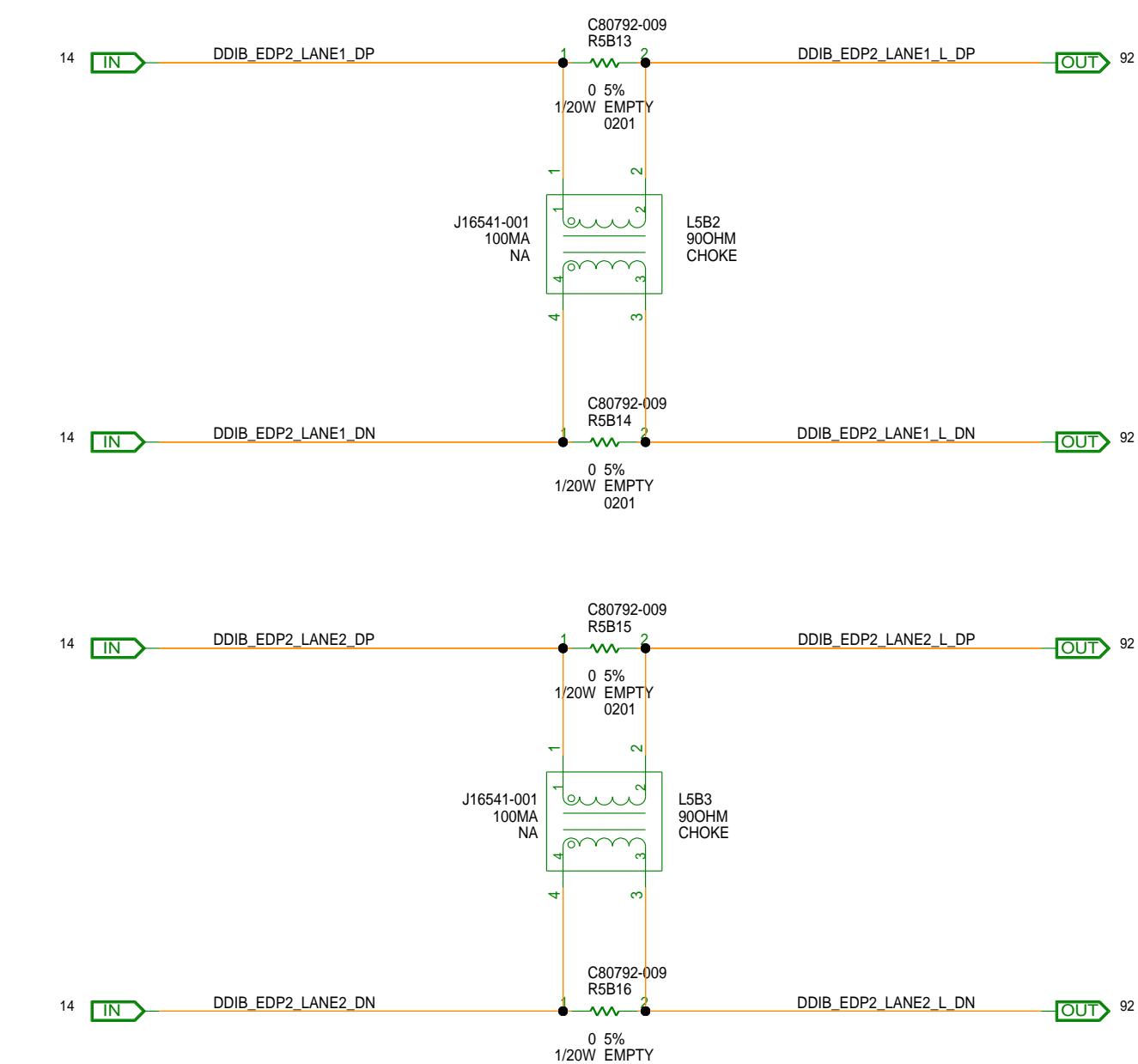
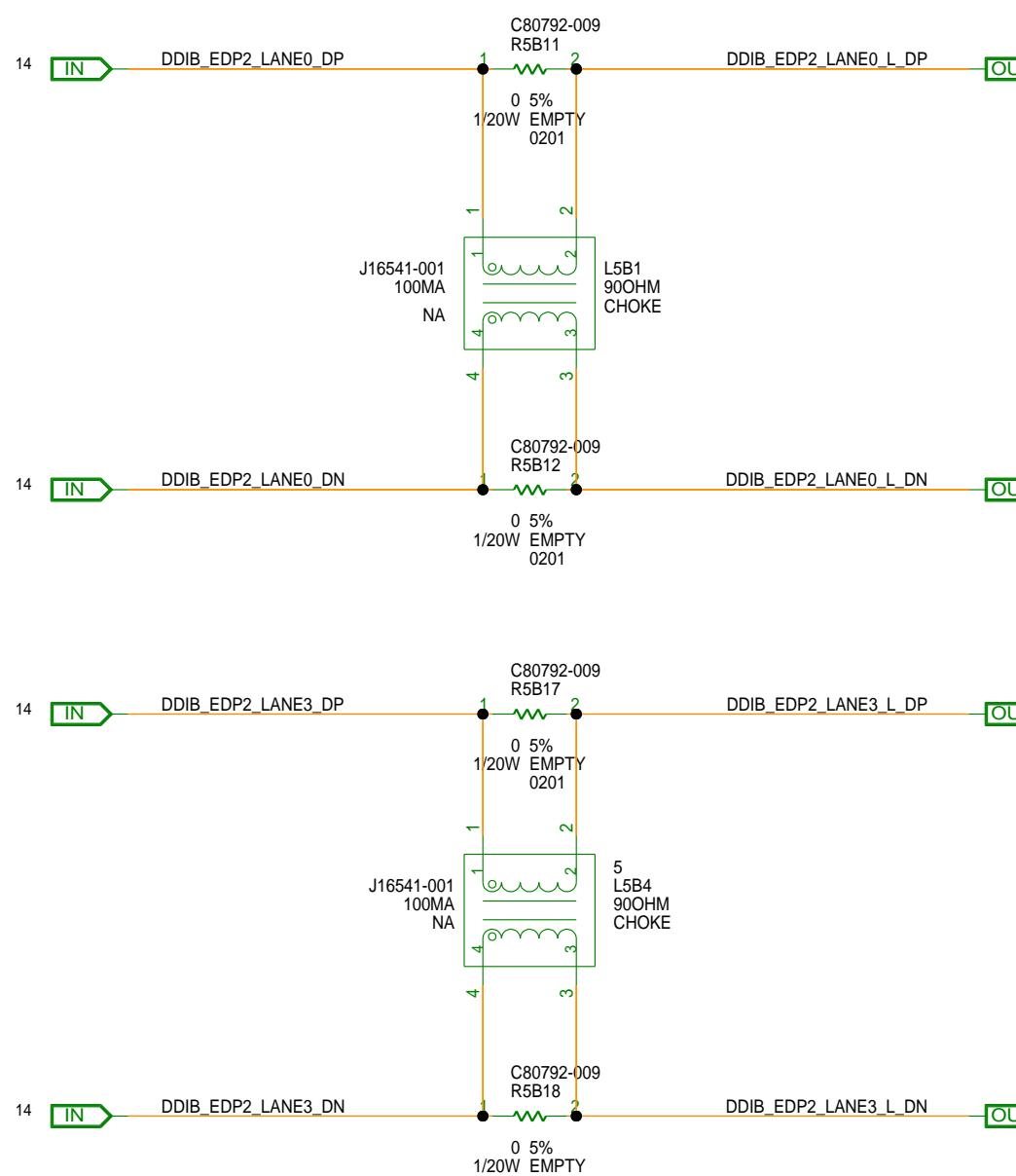
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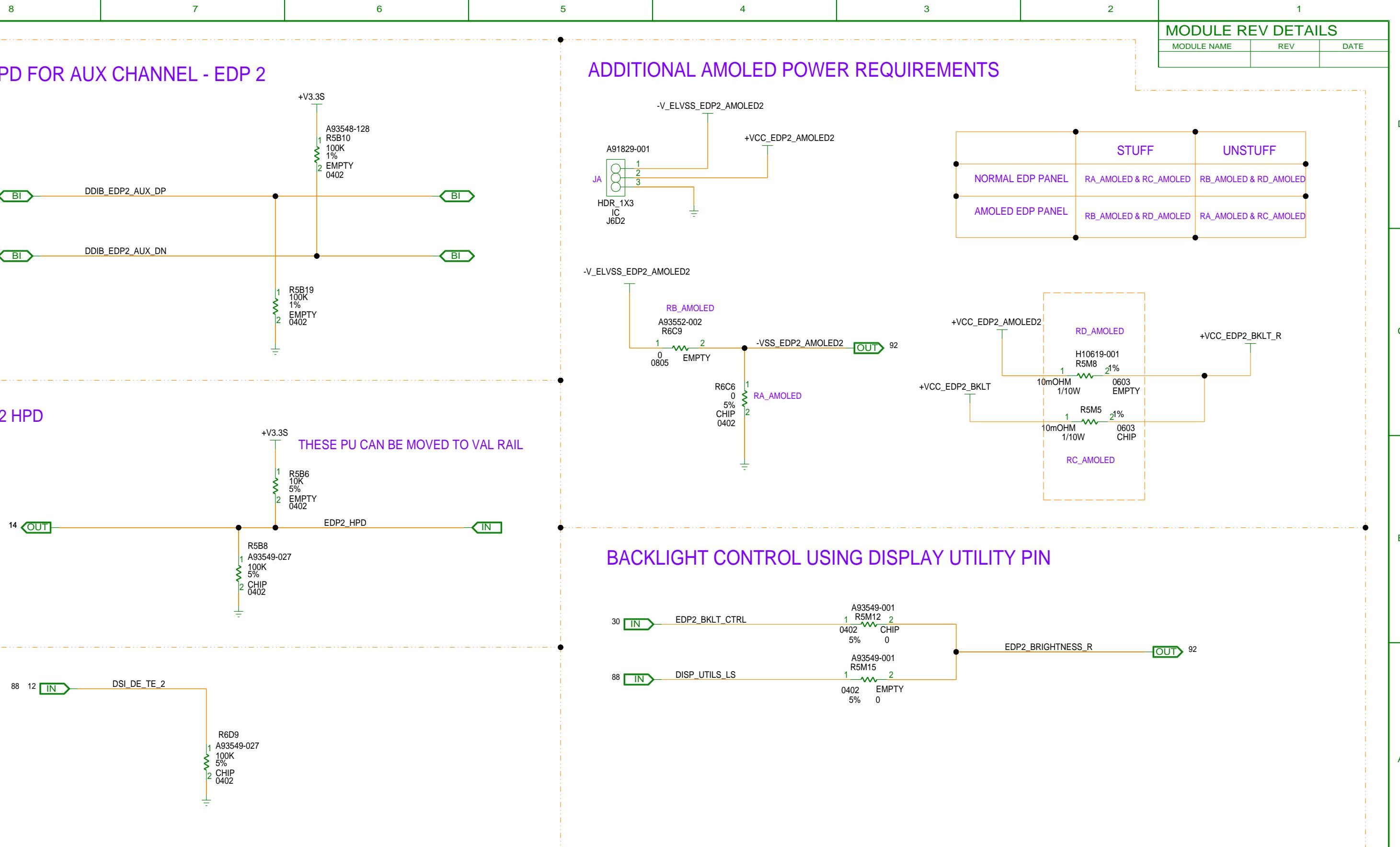
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Wed Dec 18 18:06:46 2019

| INTEL CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
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# EDP CONNECTOR 2 - CMC





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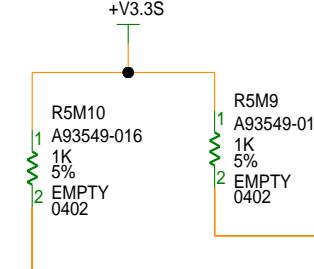
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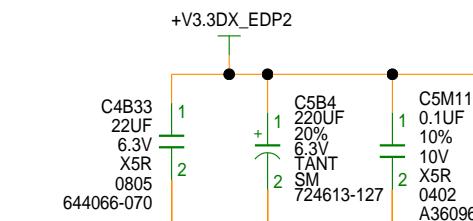
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## EDP CONNECTOR 2

THESE PU CAN BE MOVED TO VAL RAIL



CHANGE TANT CAP TO LOWER VALUE



644066-070

J4B1 CON

HDR\_1X44\_11EM\_2M\_EDP

LPDB GENERIC

MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9 MH10 MH11

V3.3S\_DP\_EMB\_1 V3.3S\_DP\_EMB\_2 V3.3S\_DP\_EMB\_3 V3.3S\_DP\_EMB\_4 V3.3S\_DP\_EMB\_5 GND\_1 GND\_2 GND\_3 GND\_4 GND\_5 NC\_1 NC\_2 NC\_3 NC\_4 NC\_5 TXN3\_C TXP3\_C GND\_6 TXN2\_C TXP2\_C GND\_7 TXN1\_C TXP1\_C GND\_8 TXN0\_C TXP0\_C GND\_9 EMB\_AUXP EMB\_AUXN VSS\_EDP\_AMOLED0 V3.3S\_EMB\_AUXPWR NC\_10 VCC\_EDP\_BKLT0 VSS\_EDP\_AMOLED1 GND\_11 VCC DBL\_CLK L\_BRIGHTNESS L\_BLKT\_EN VCC\_EDP\_BKLT1 VDD\_ALS GND\_12 SMB\_THRM\_CLK SMB\_THRM\_DATA ALS\_INTR# TP\_VDD\_LPP

91 14 OUT EDP2\_HPD

90 90 DDIB\_EDP2\_LANE3\_L\_DN DDIB\_EDP2\_LANE3\_L\_DP

90 90 DDIB\_EDP2\_LANE2\_L\_DN DDIB\_EDP2\_LANE2\_L\_DP

90 90 DDIB\_EDP2\_LANE1\_L\_DN DDIB\_EDP2\_LANE1\_L\_DP

90 90 DDIB\_EDP2\_LANE0\_L\_DN DDIB\_EDP2\_LANE0\_L\_DP

91 14 BI BI DDIB\_EDP2\_AUX\_DP DDIB\_EDP2\_AUX\_DN

92 91 -VSS\_EDP2\_AMOLED2 TP\_CON2\_EDP\_30

92 91 IN -VSS\_EDP2\_AMOLED2 TP\_CON2\_EDP\_5V

TP\_CON2\_EDP\_35 EDP2\_BRIGHTNESS\_R

EDP2\_BKLT\_EN

TP\_CON2\_ALS\_PWR

TP\_CON2\_I2C\_SCL\_EDP\_ALS\_R

TP\_CON2\_I2C\_SDA\_EDP\_ALS\_R

TP\_CON2\_EDP\_ALS\_INT\_R\_N

TP\_CON2\_VDD\_LPP

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**MODULE REV DETAILS**

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Tue Oct 15 12:49:48 2019

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CUSTOM TEXT <sup>2</sup>BPAGE

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 Tue Oct 15 12:49:49 2019

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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>94 | REV<br>1.0 |
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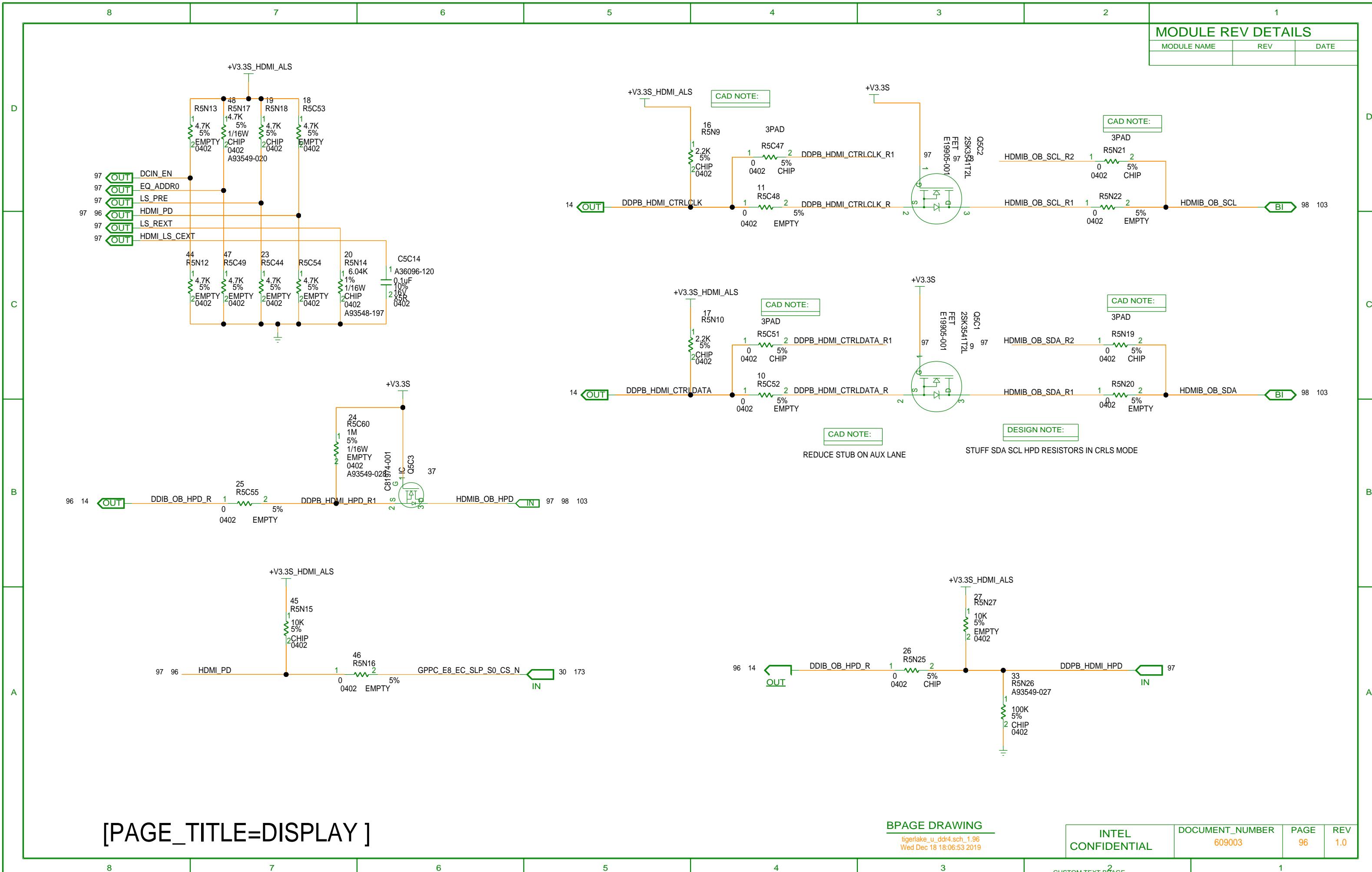
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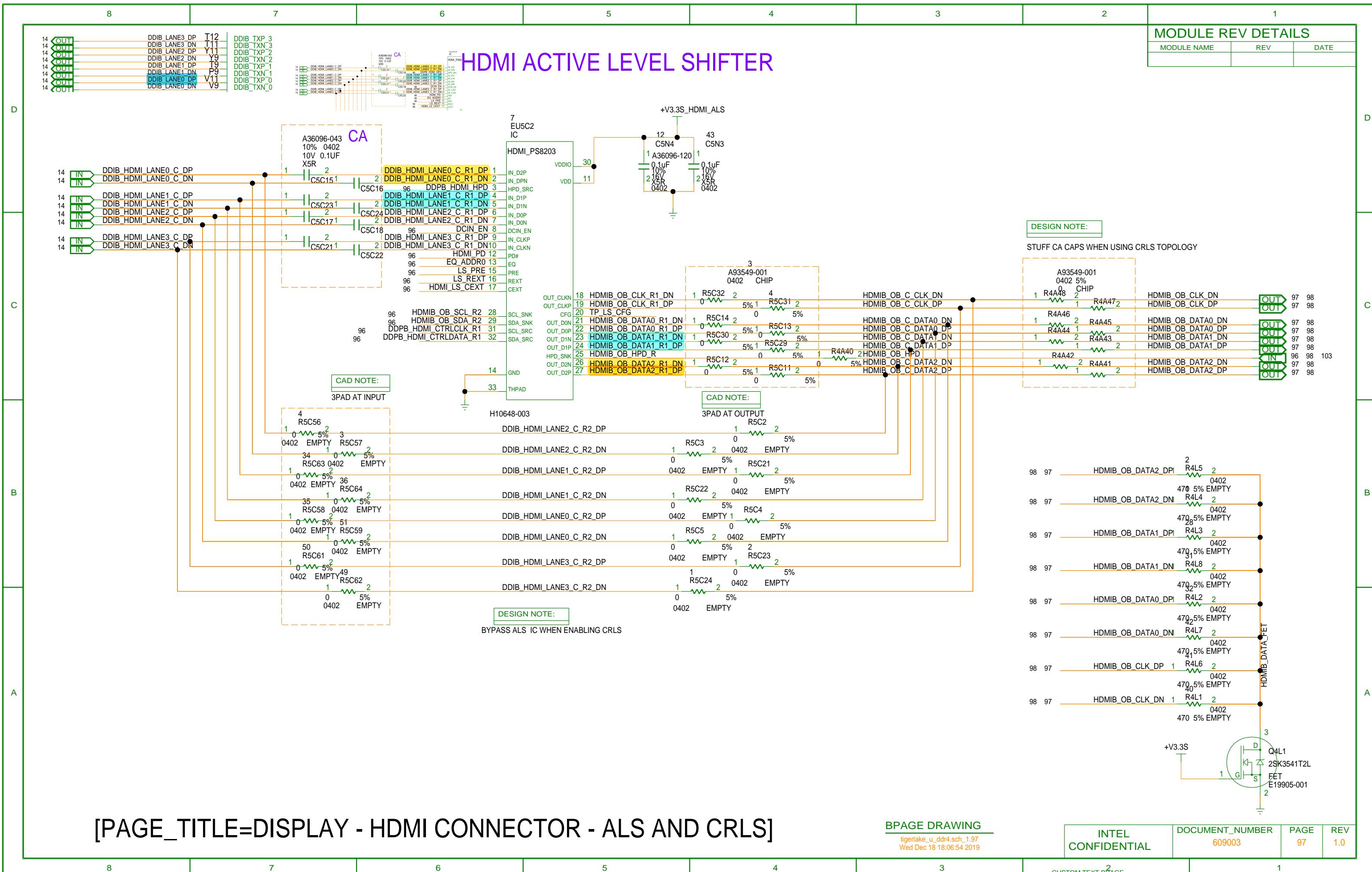
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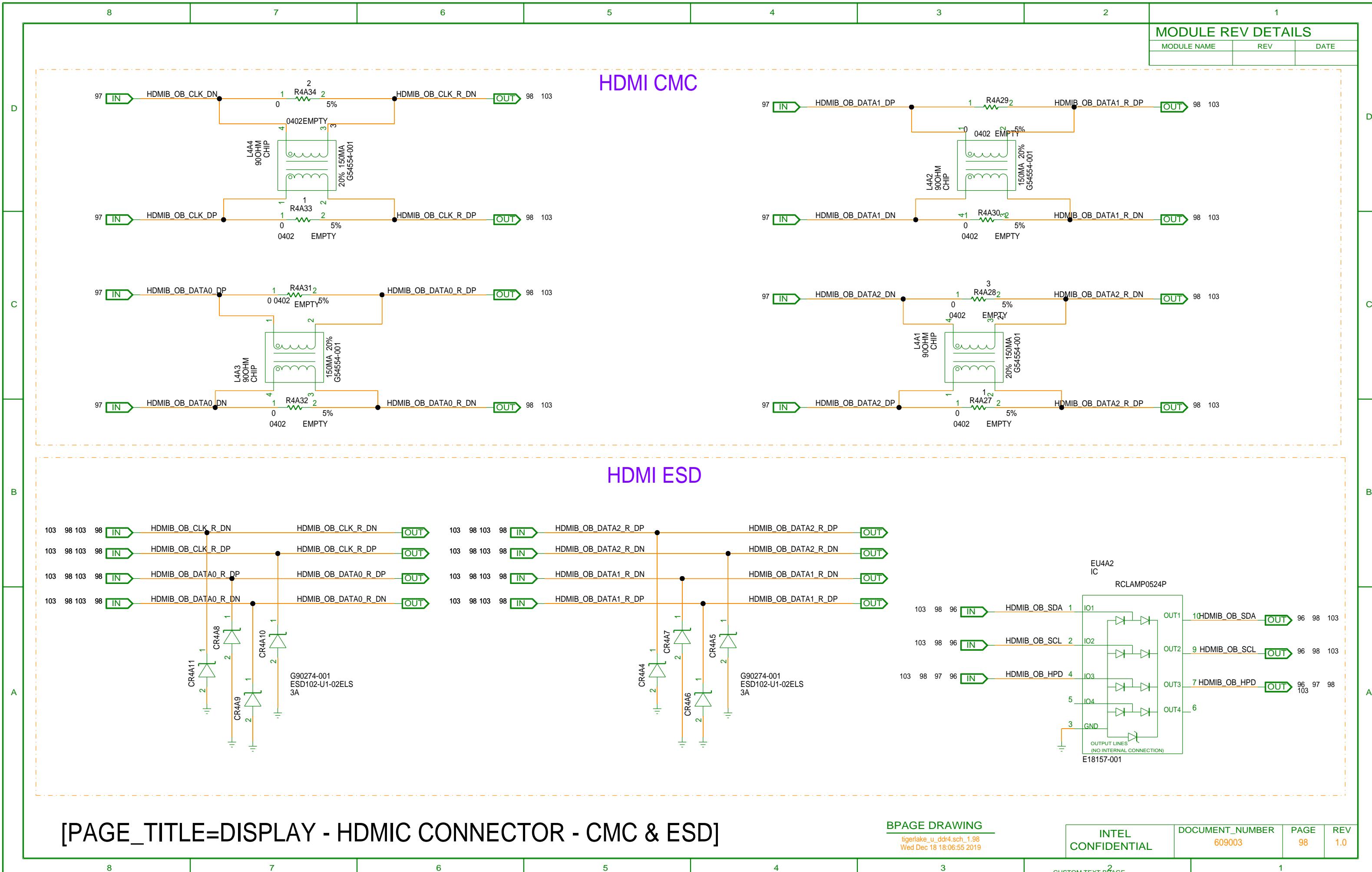
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# DP CONNECTOR 2 - CMC

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CUSTOM TEXT 2 PAGE

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# DP CONNECTOR 2 - ESD

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| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
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**MODULE REV DETAILS**

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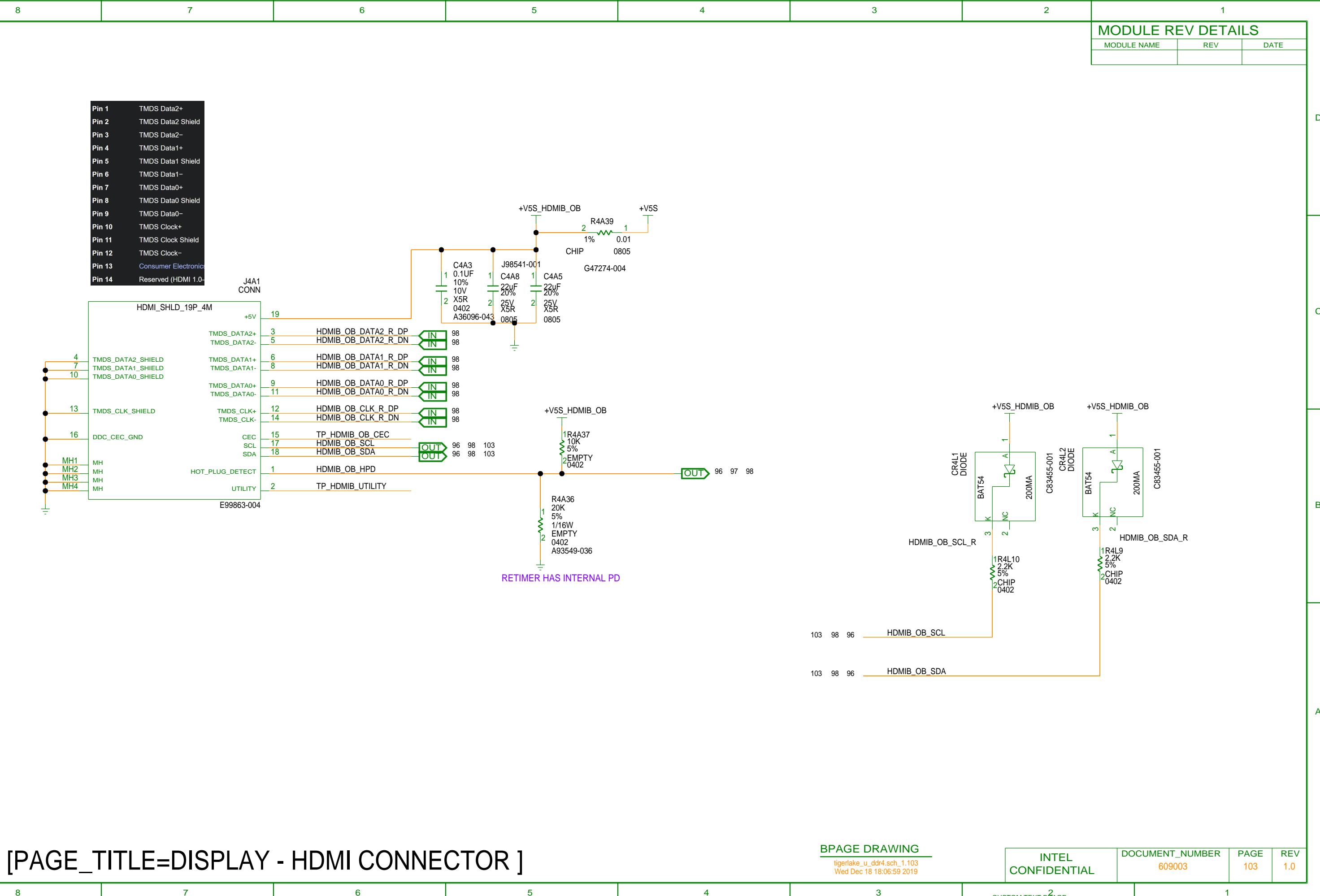
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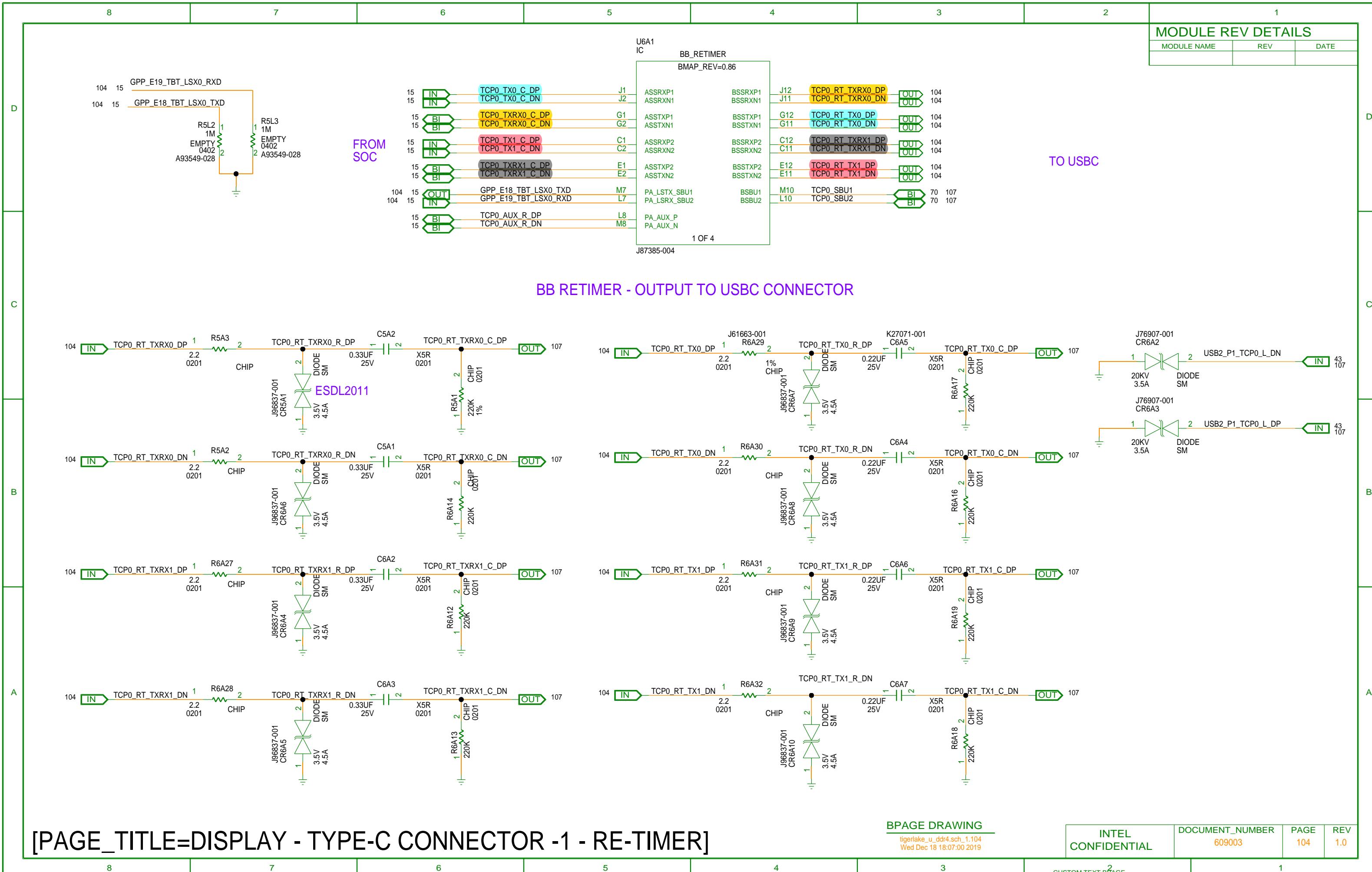
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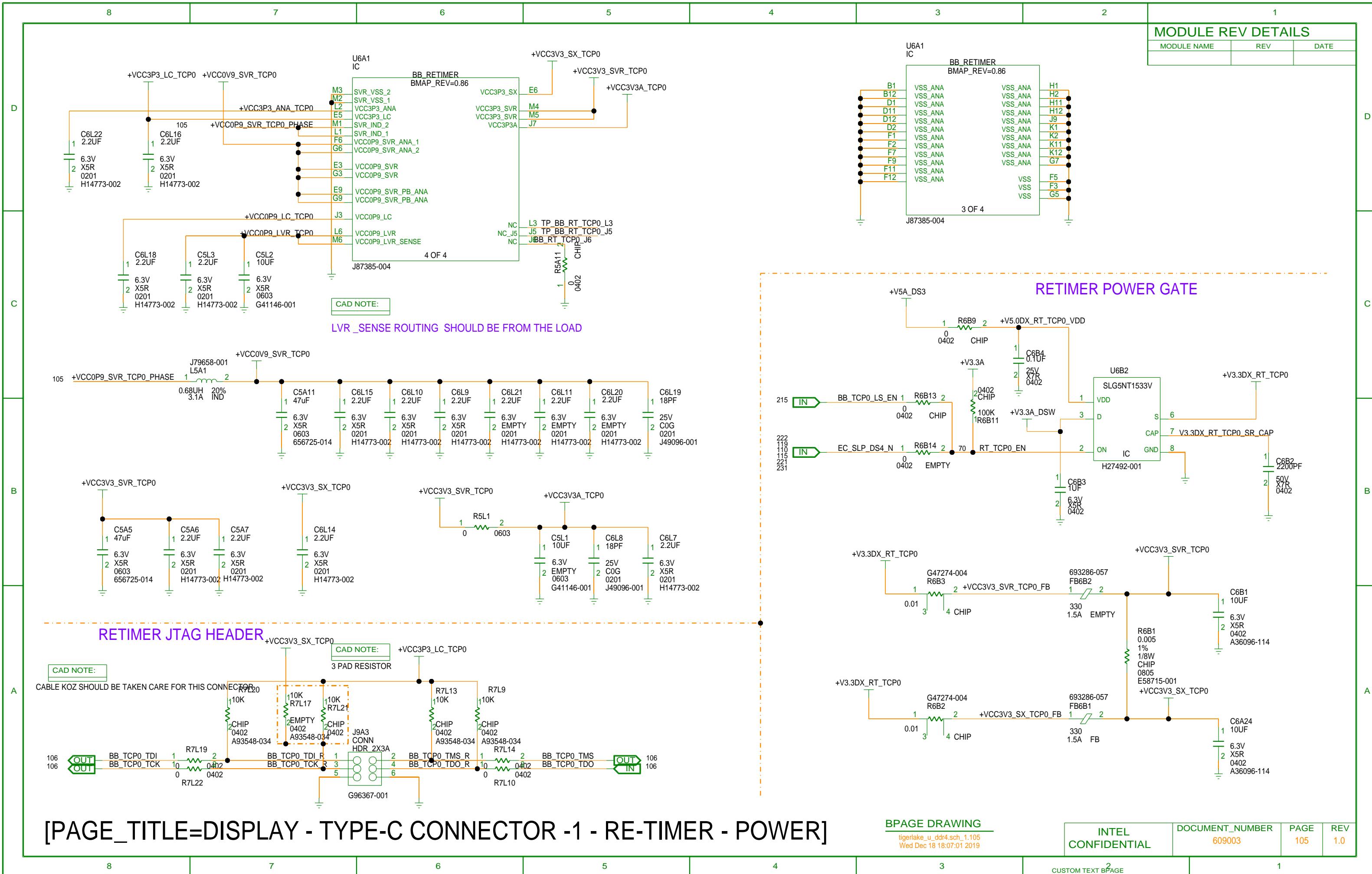
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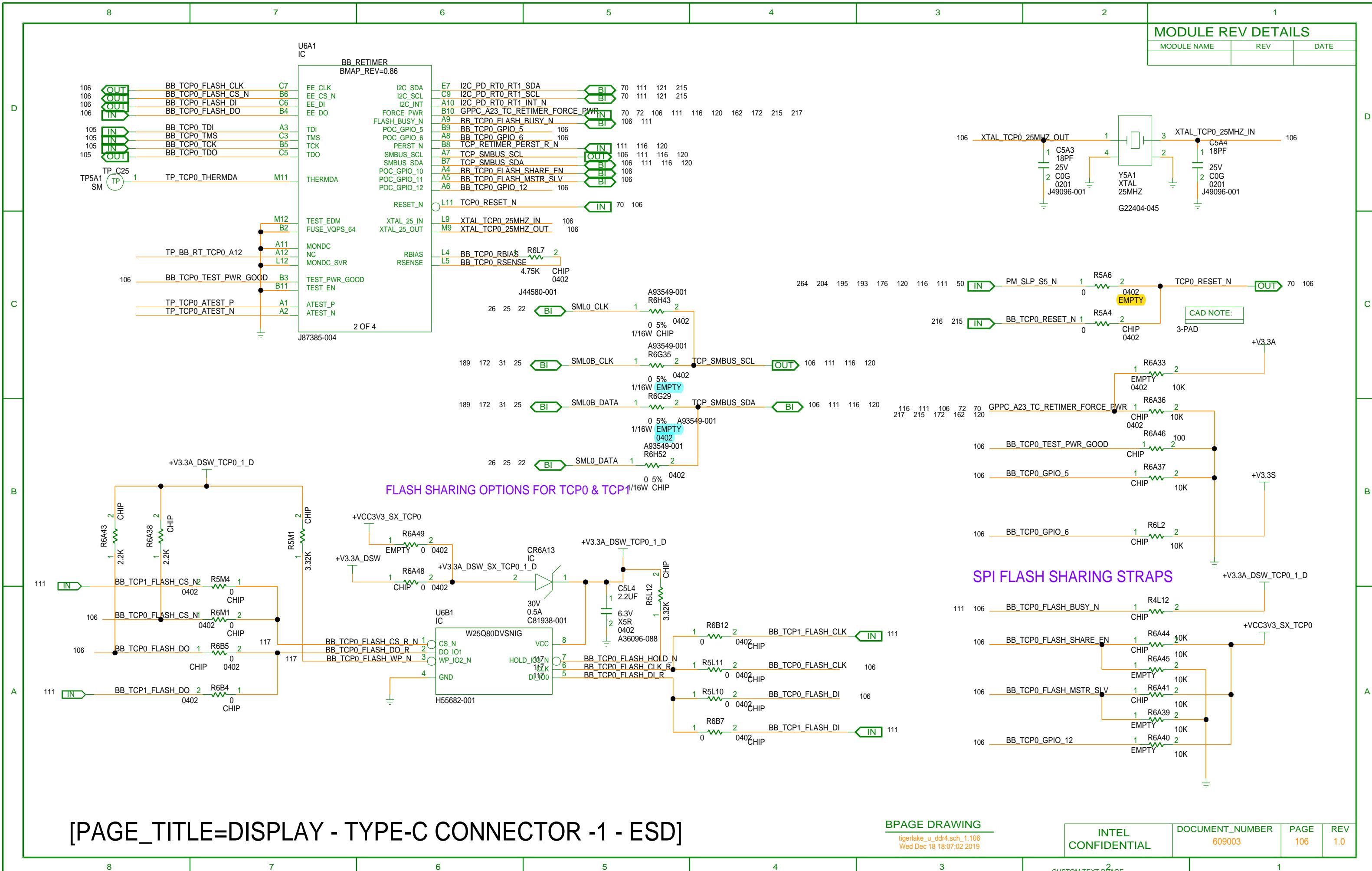
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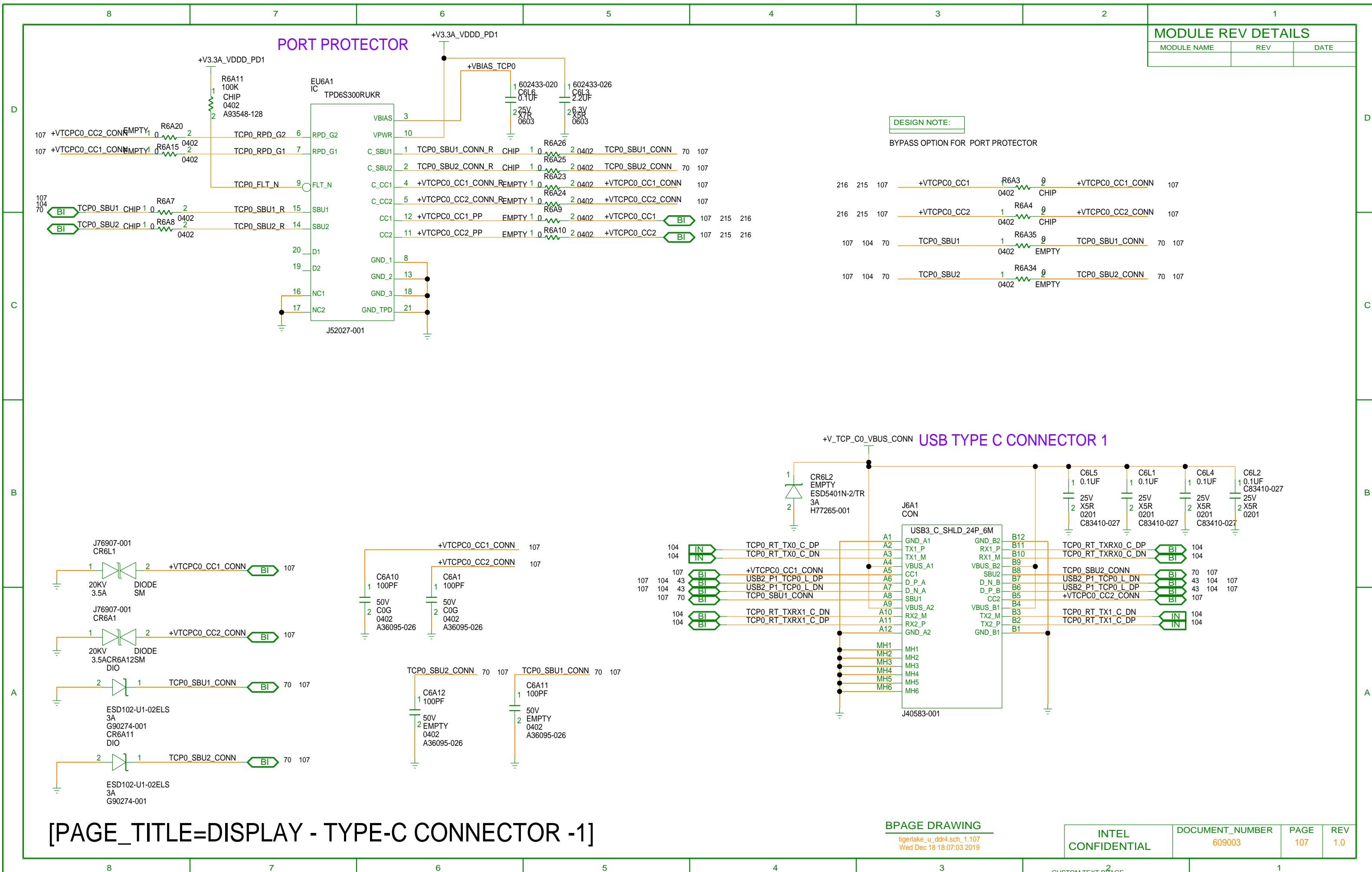
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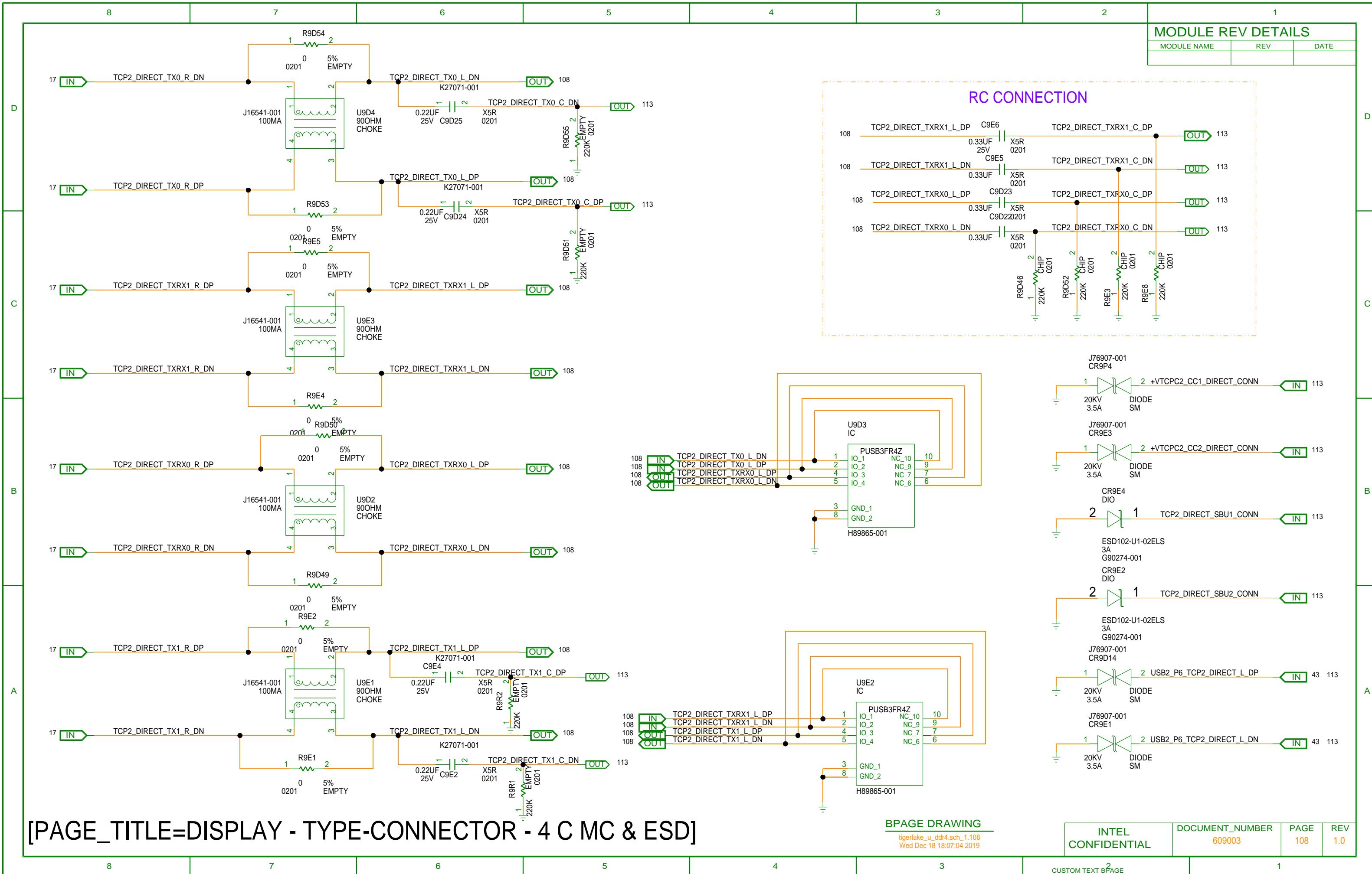


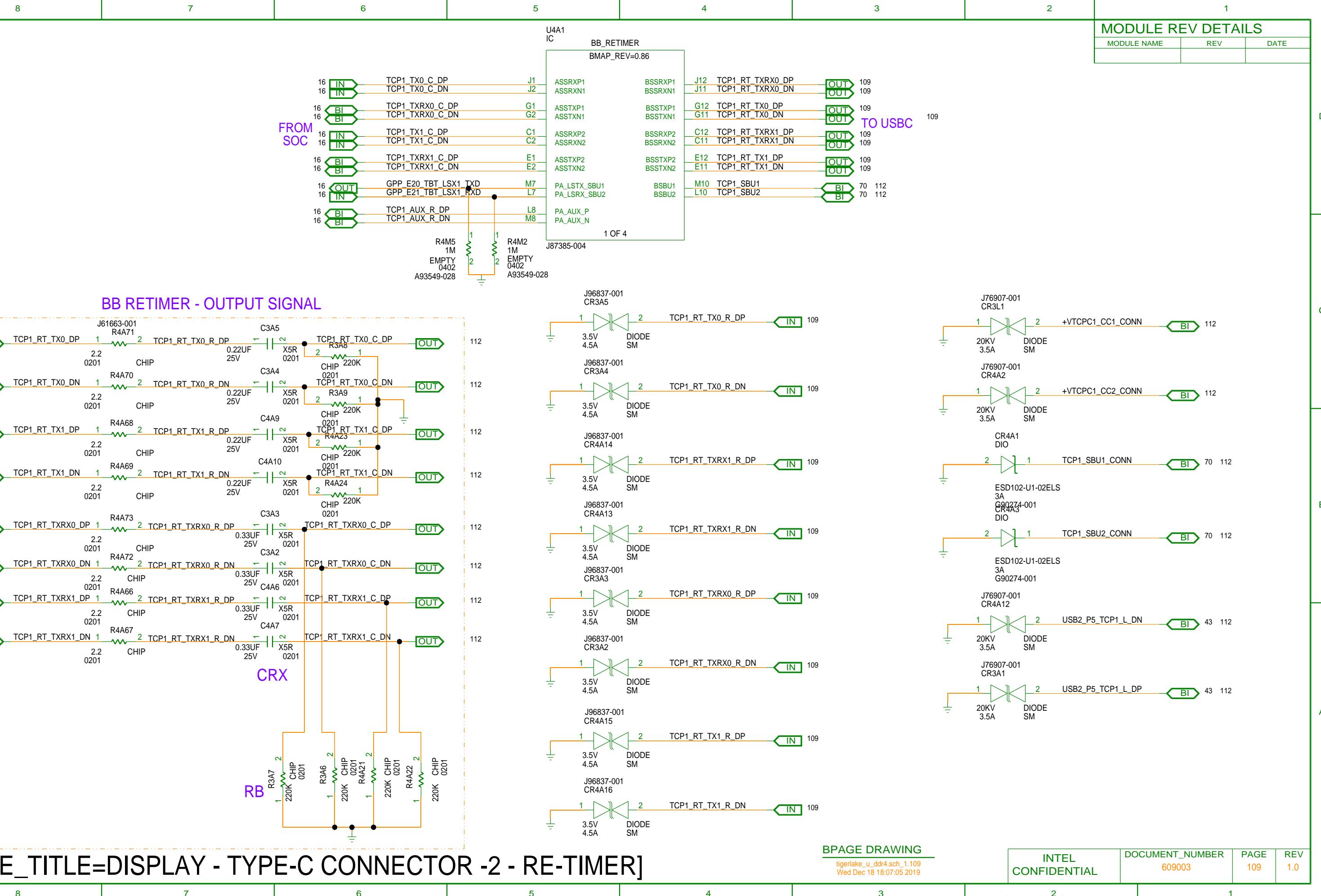


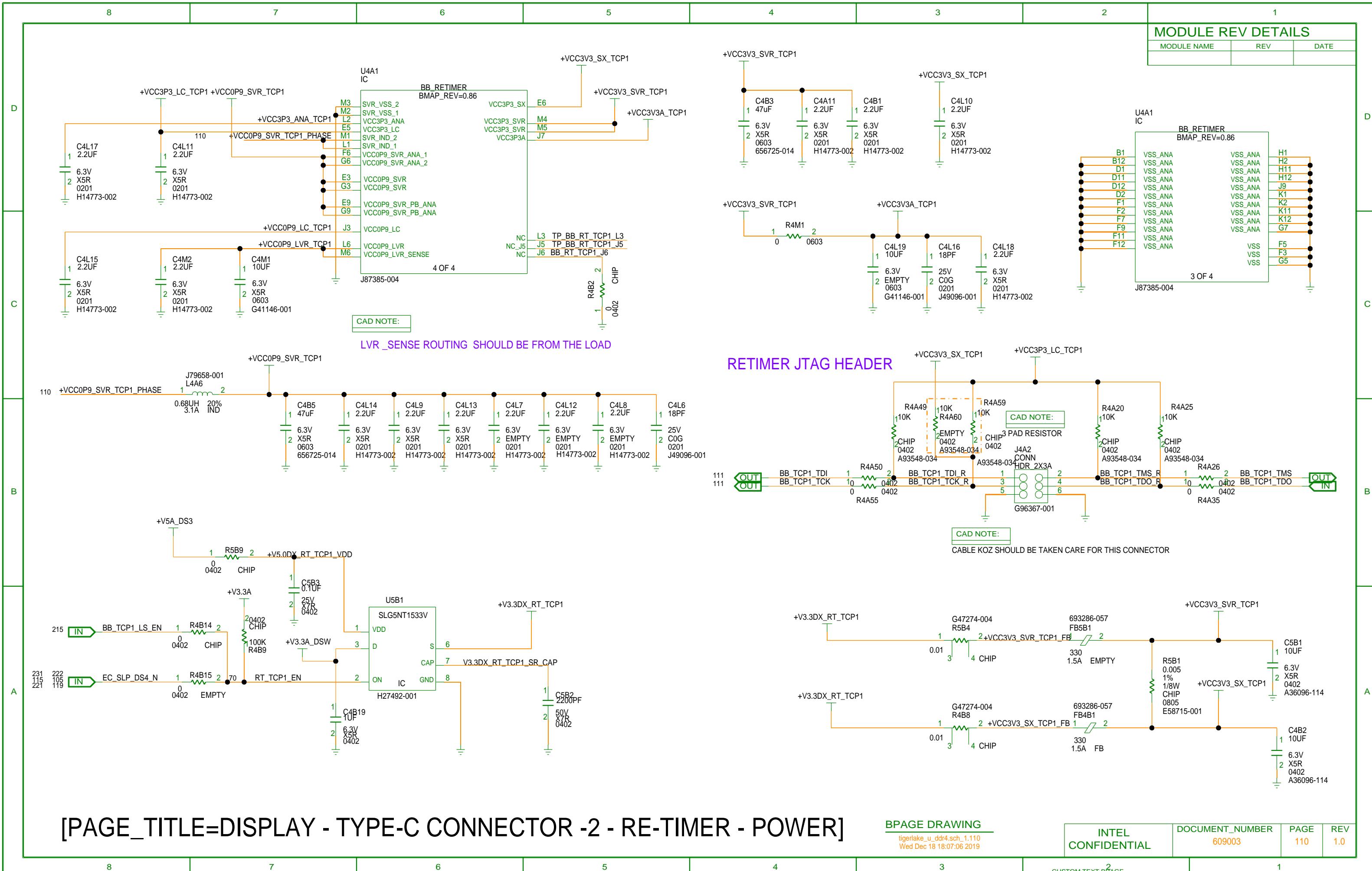


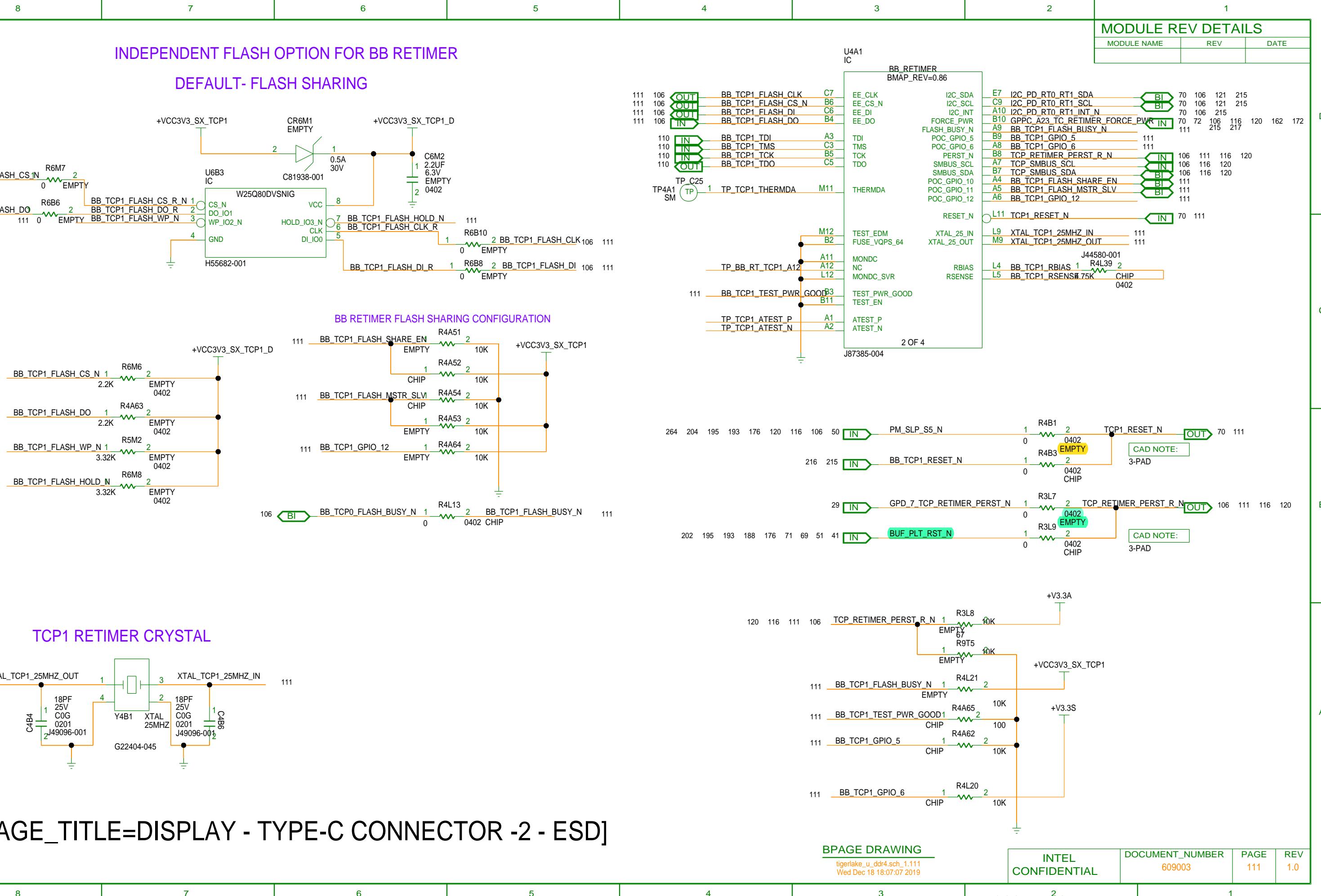


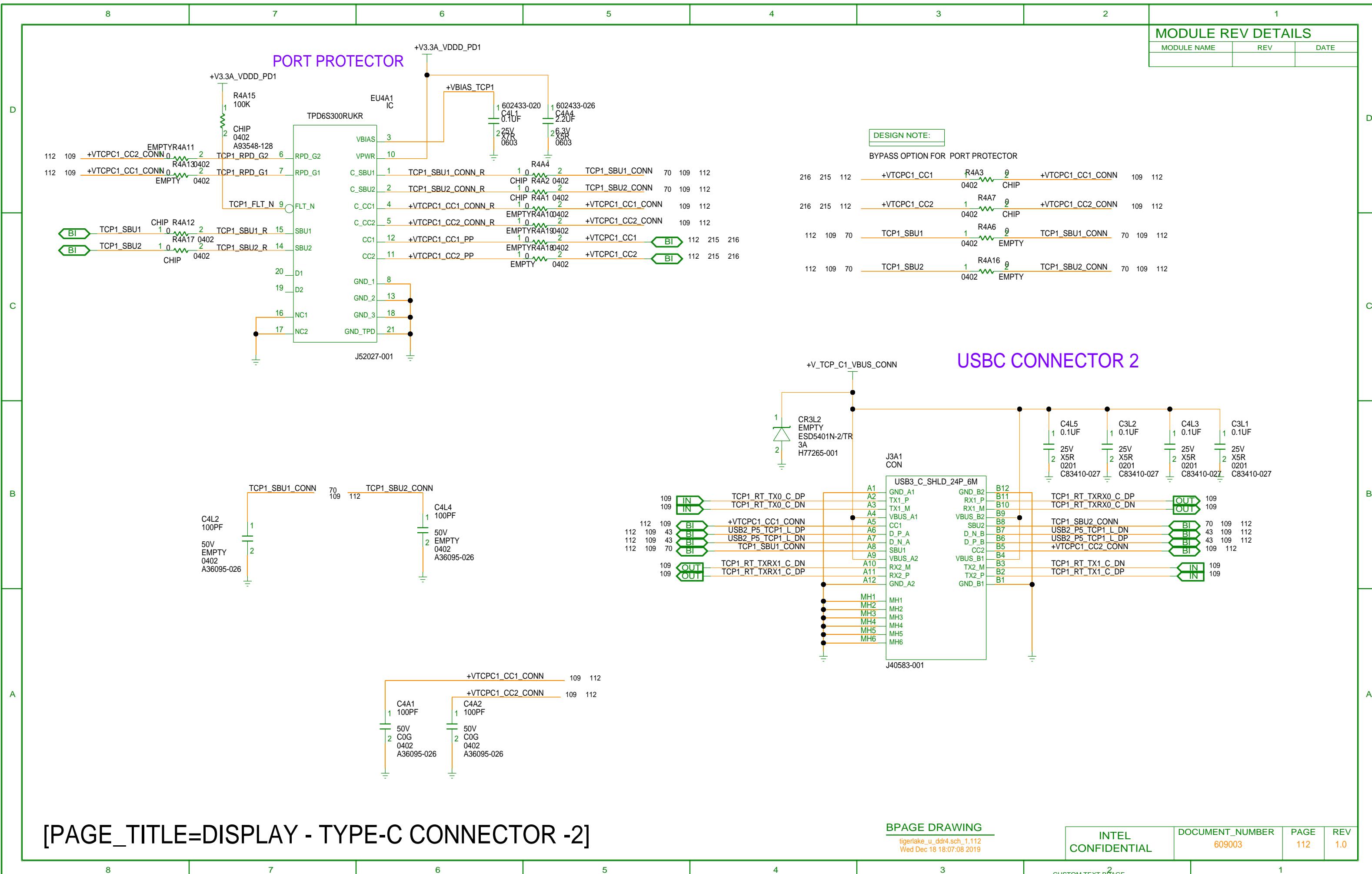


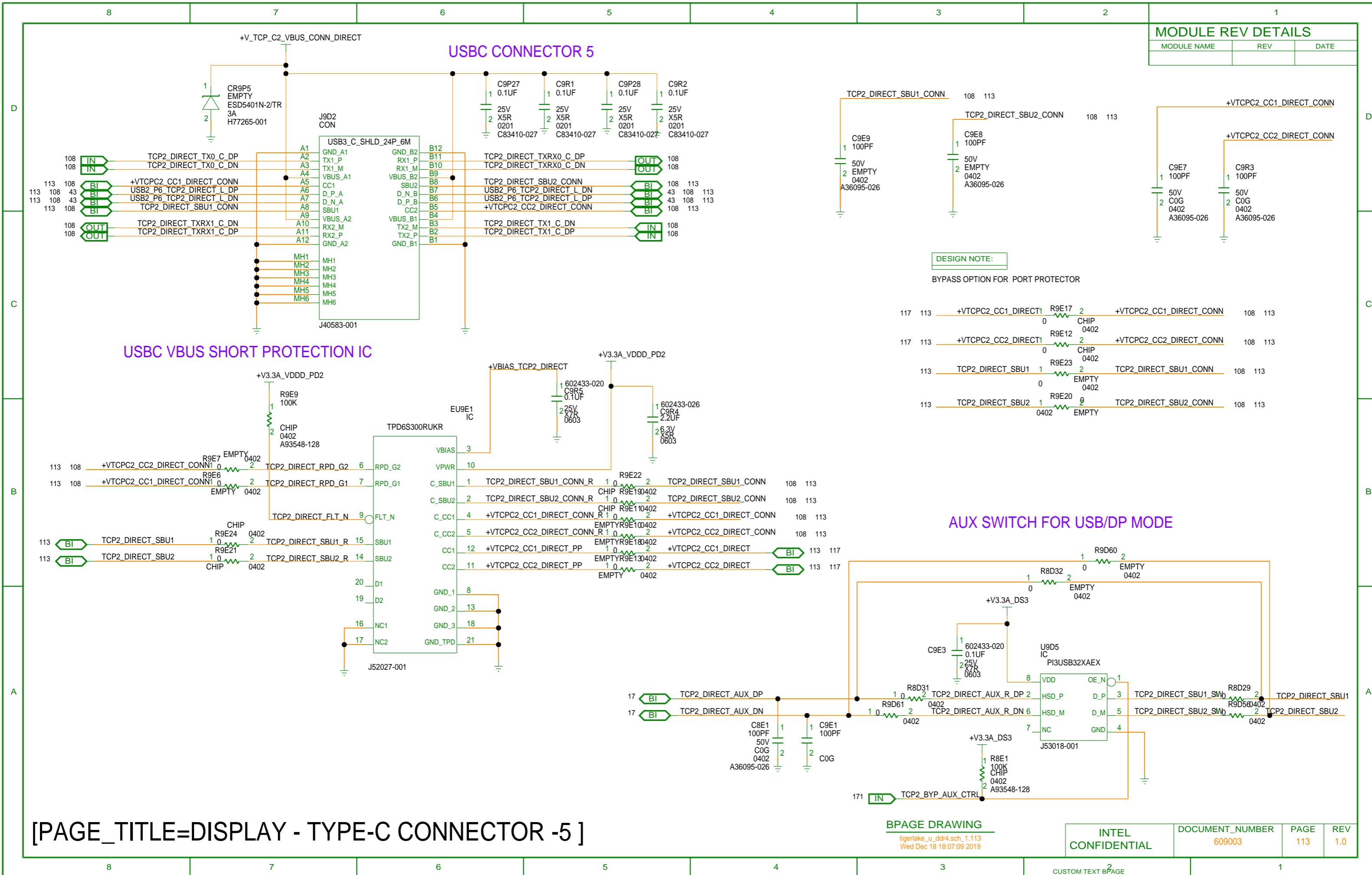


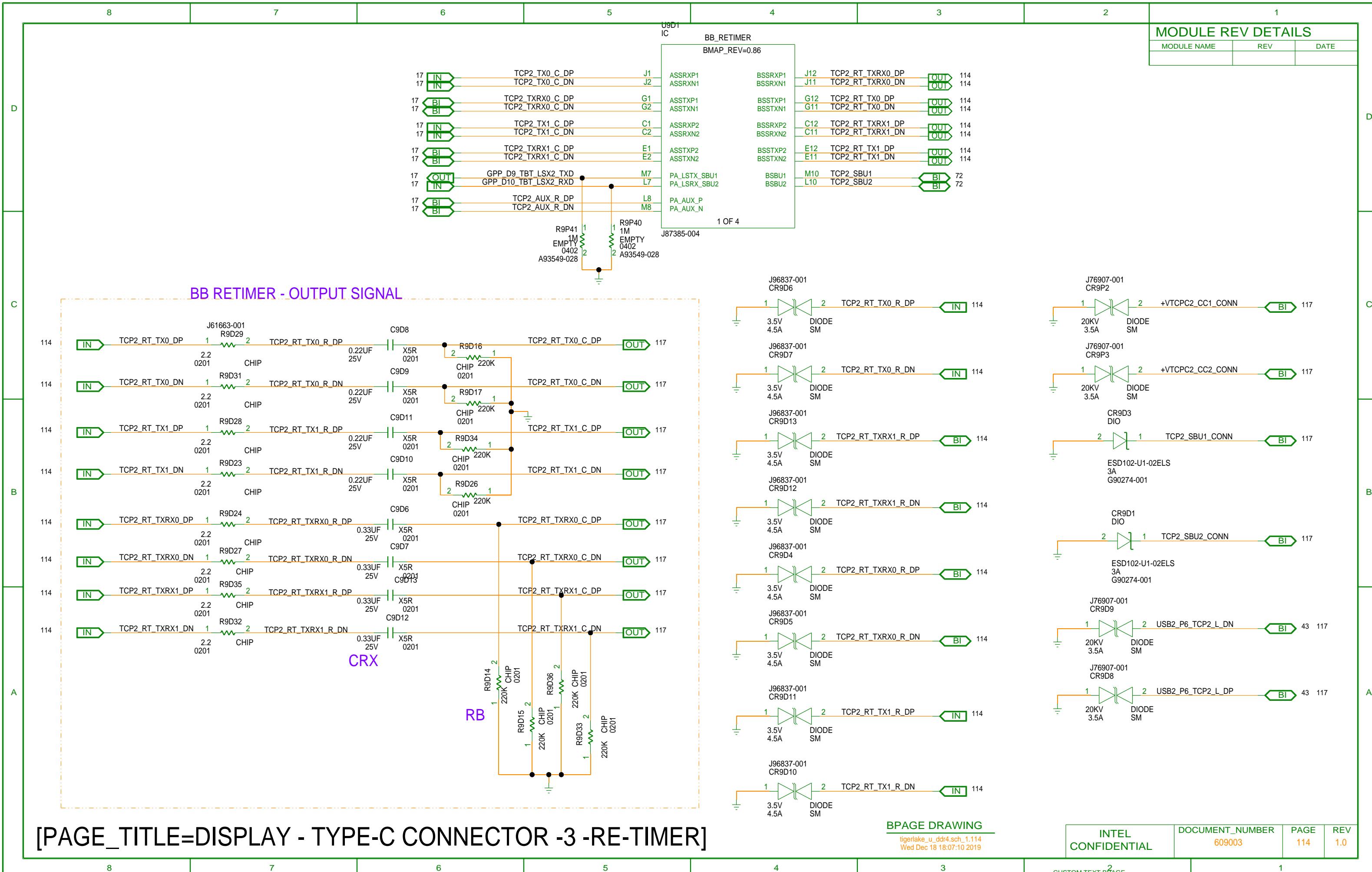


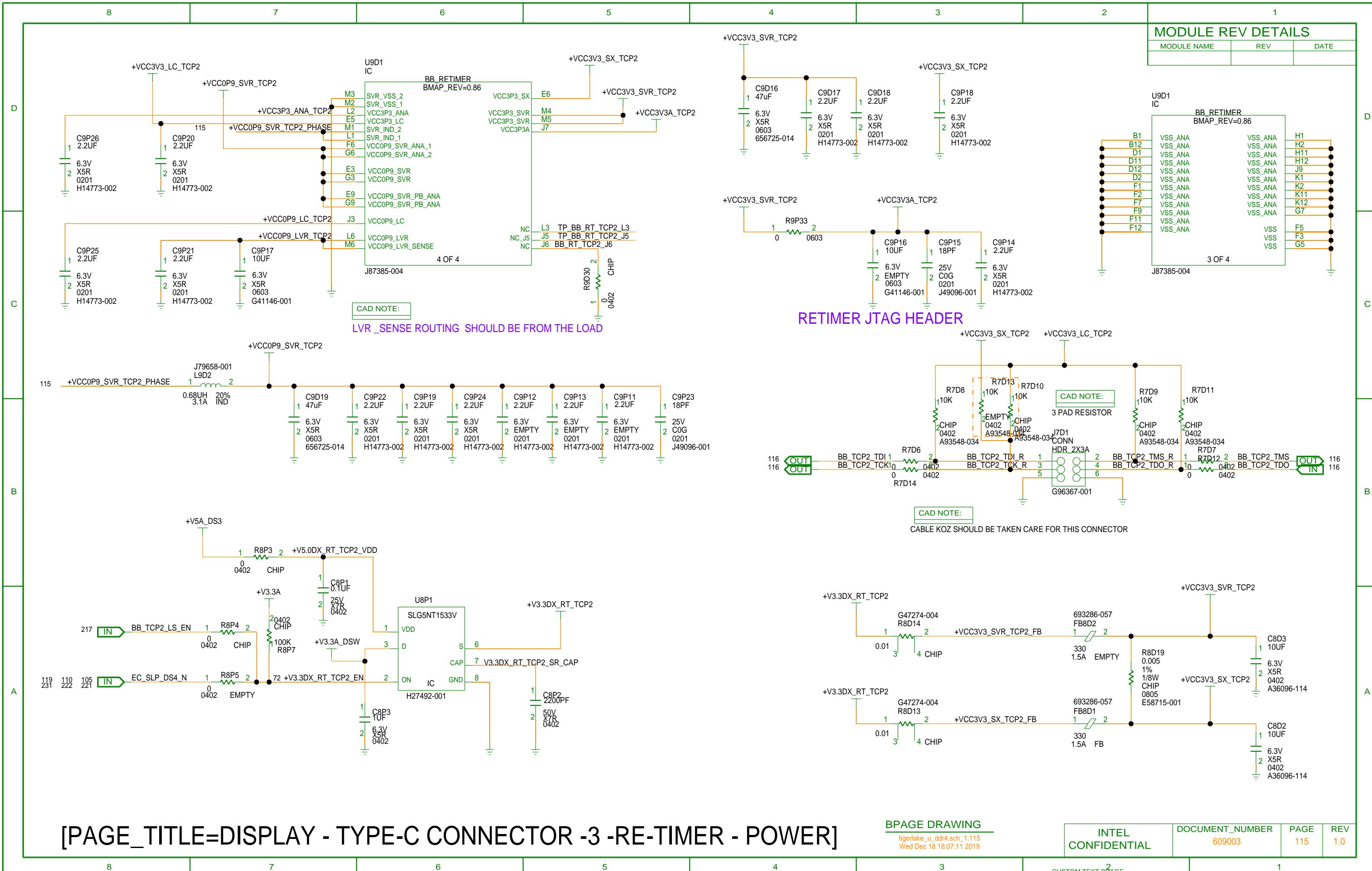


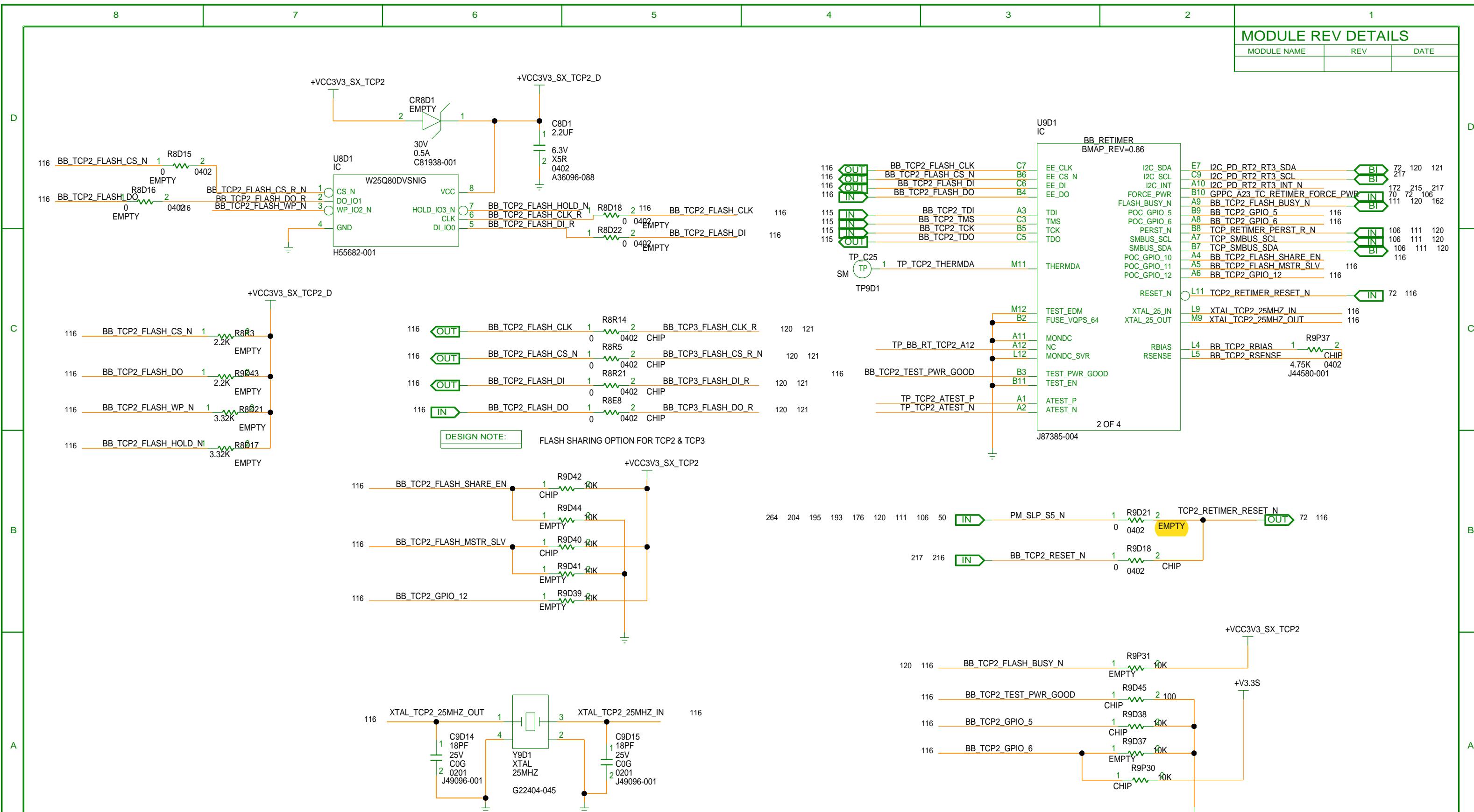












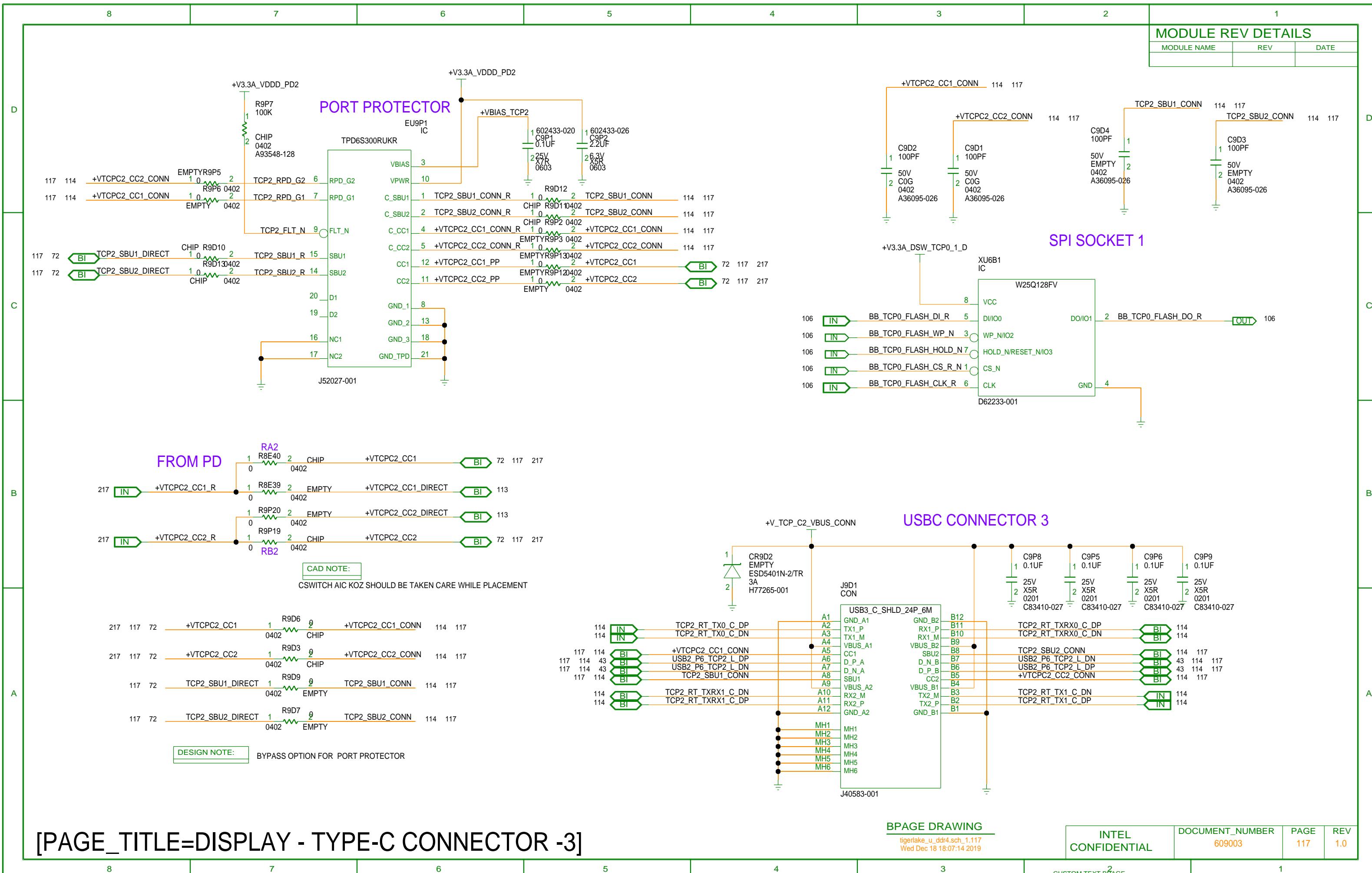
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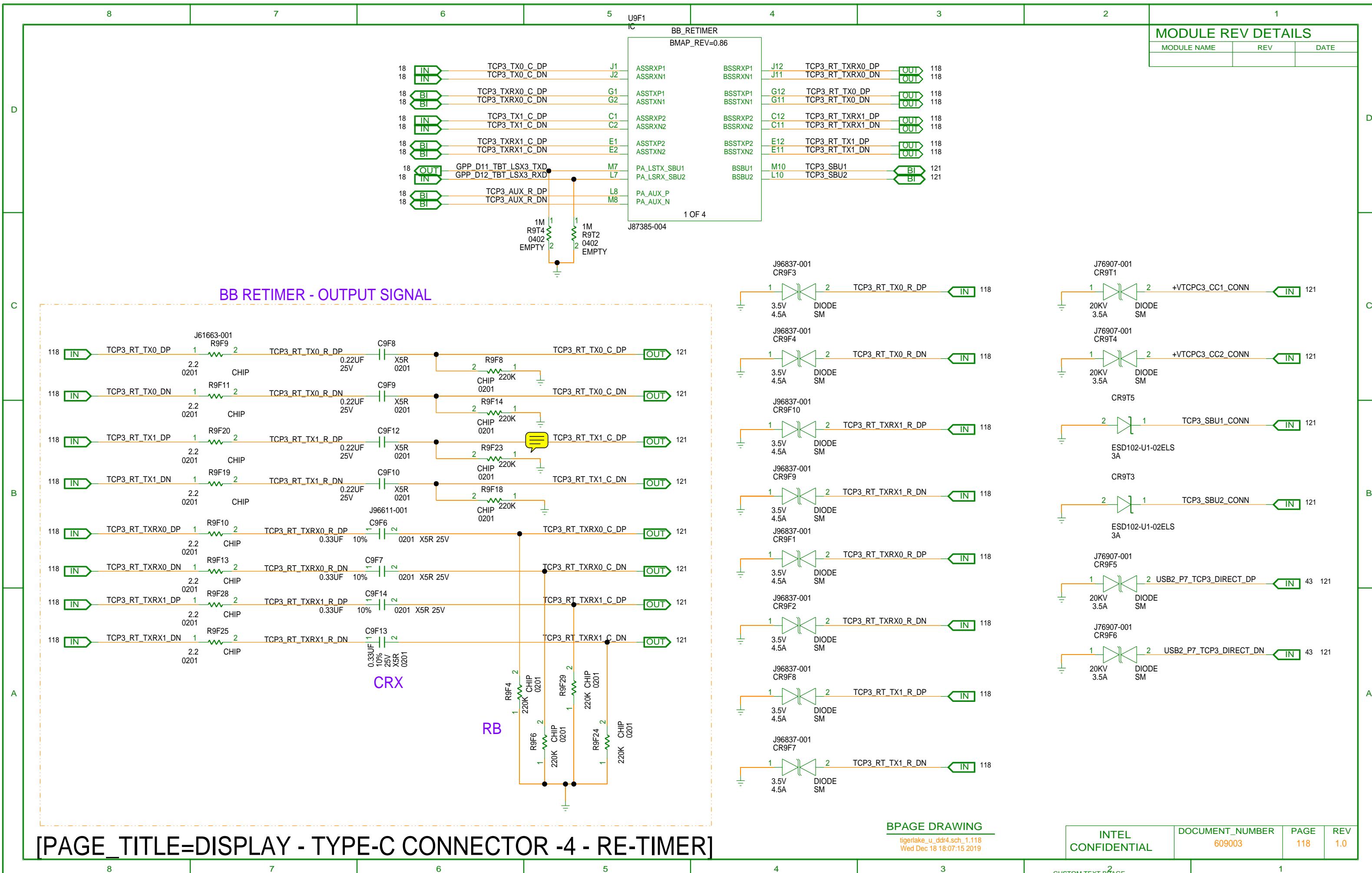
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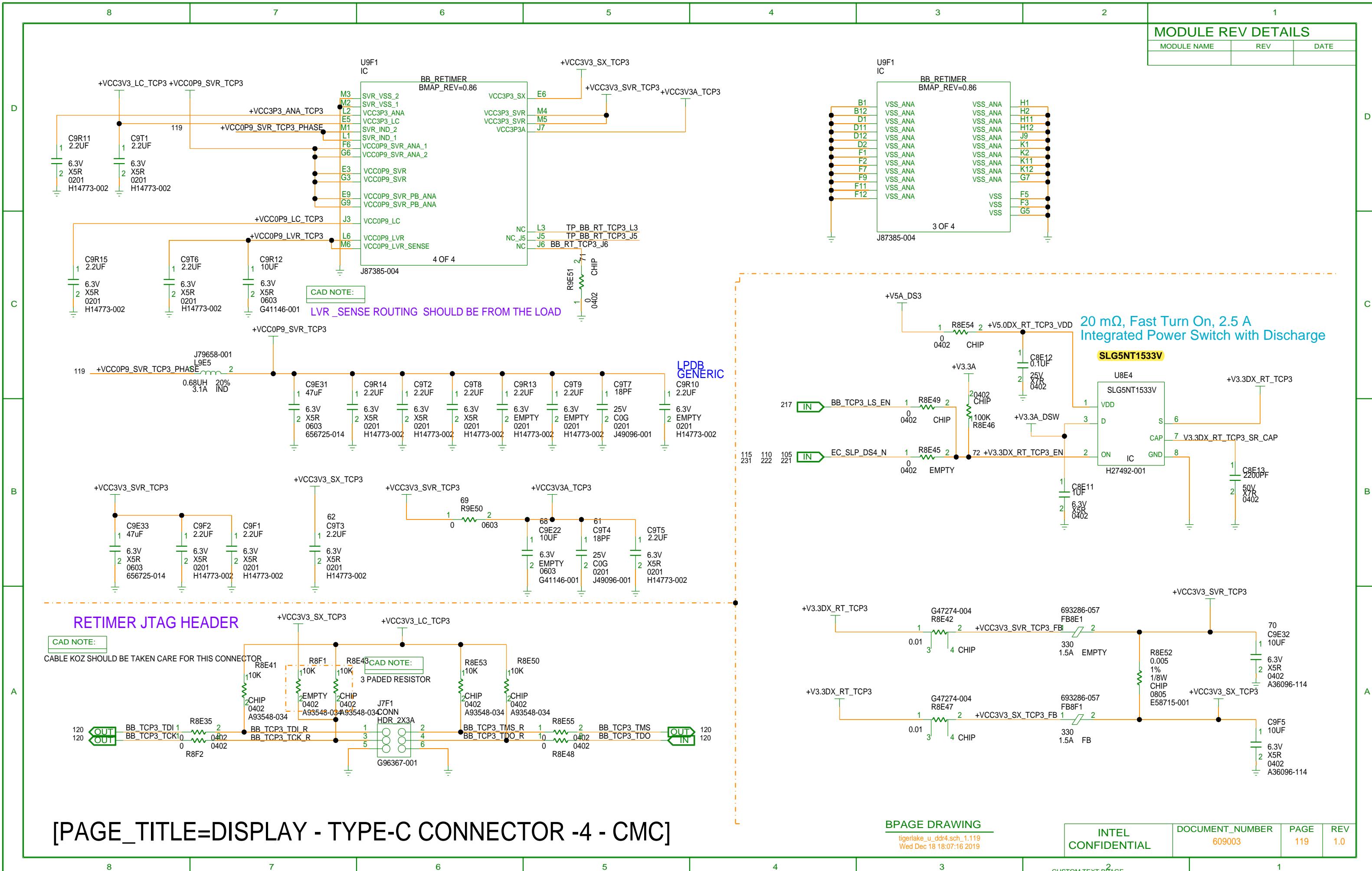
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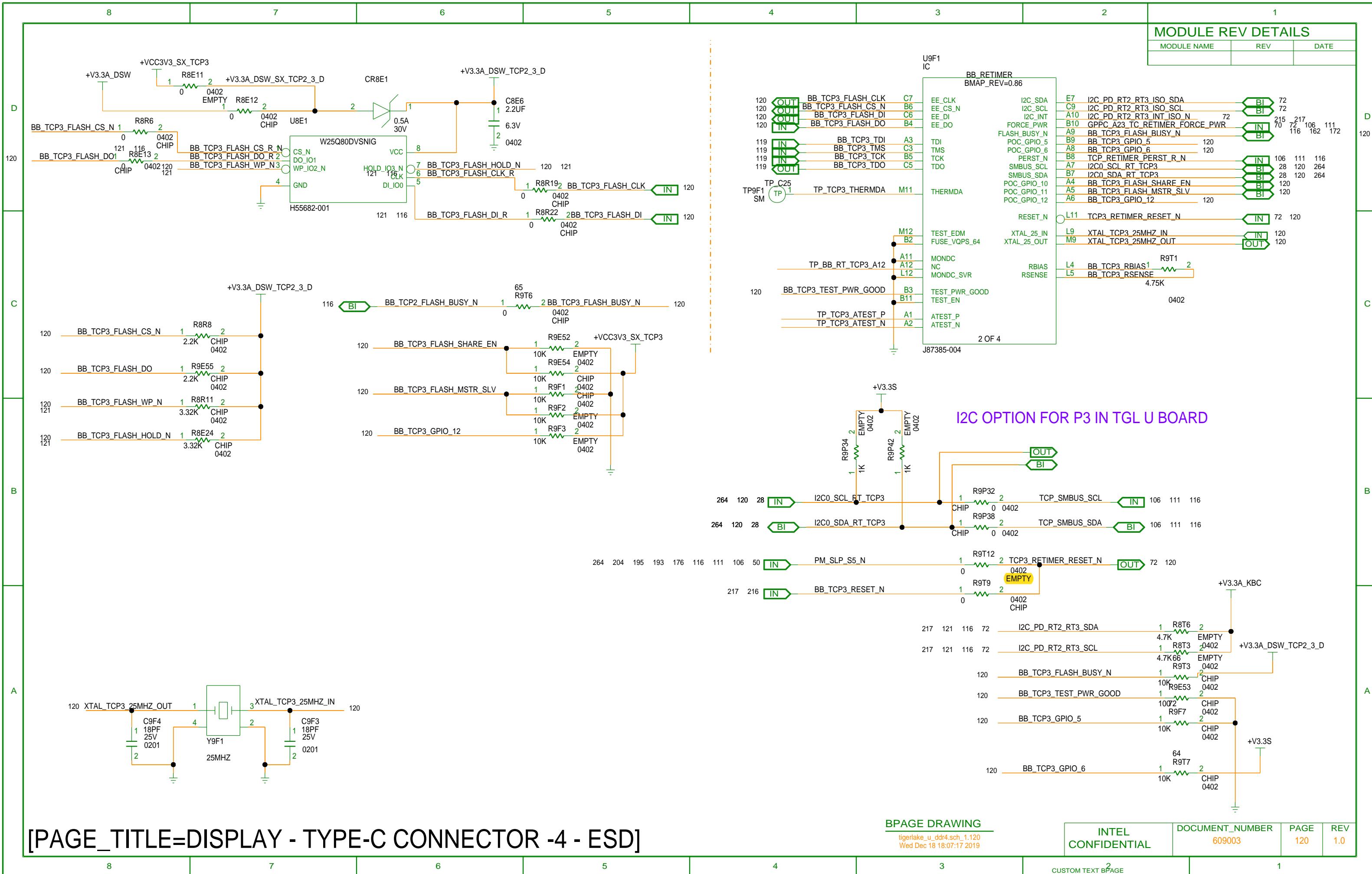
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Wed Dec 18 18:07:12 2019

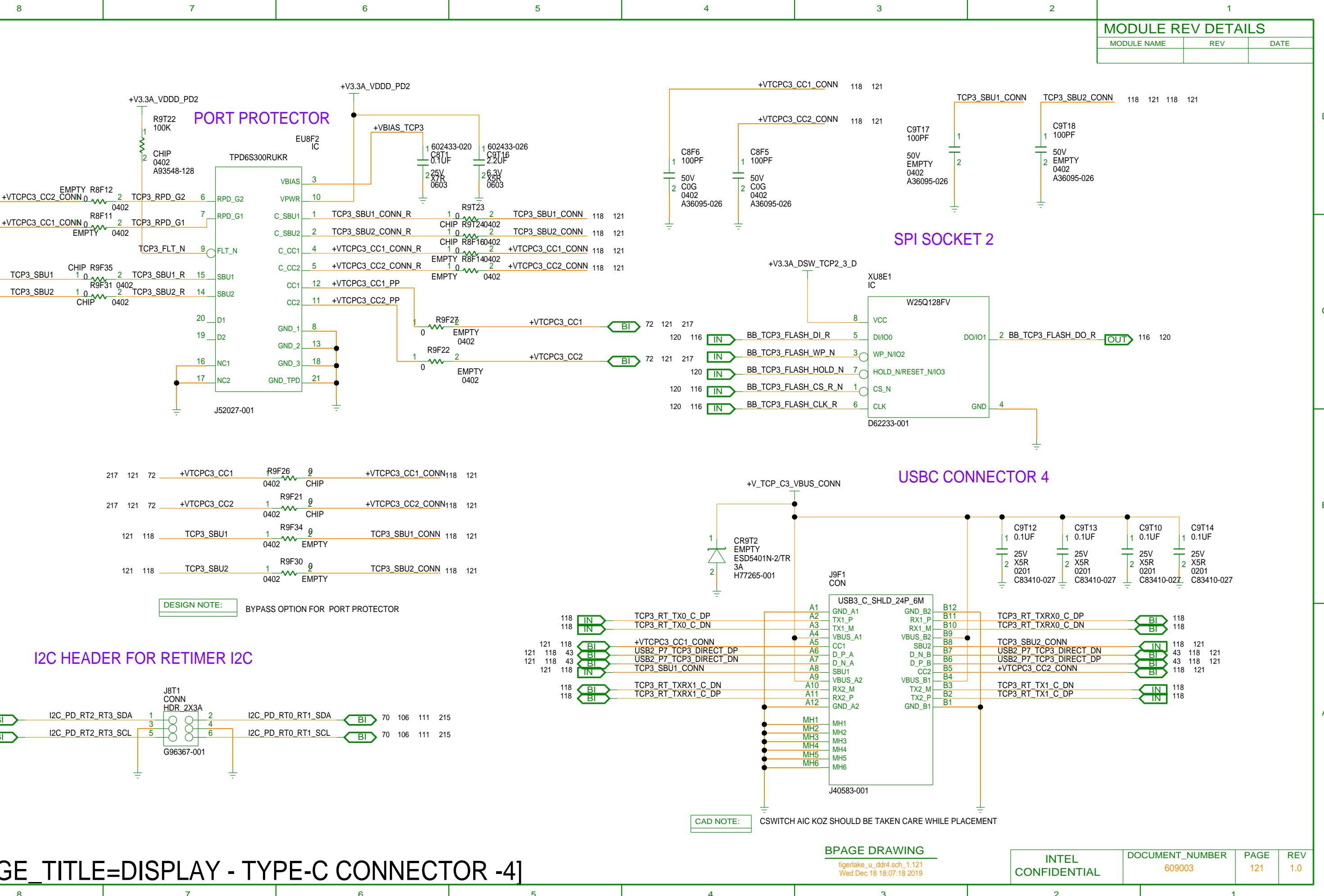
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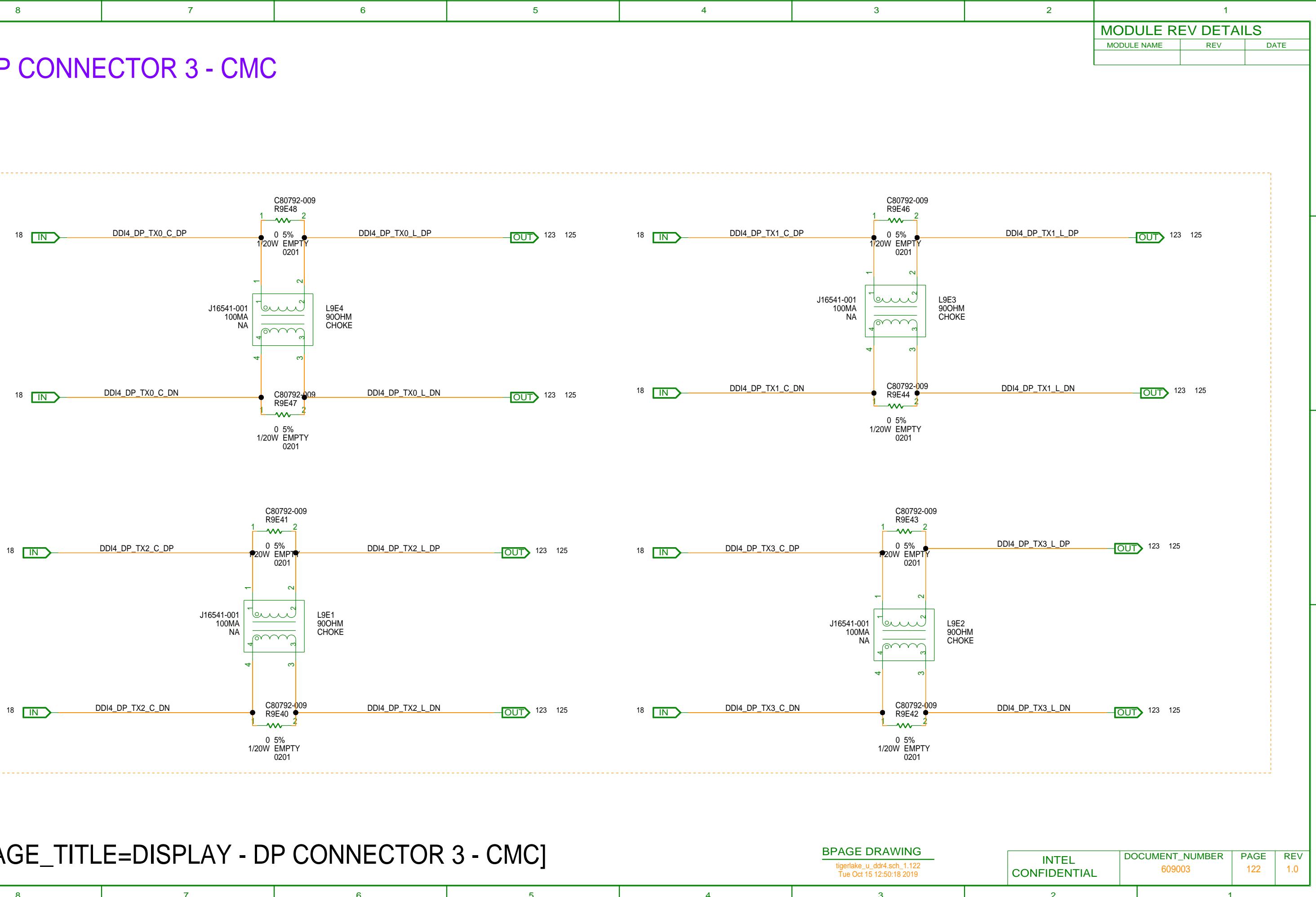








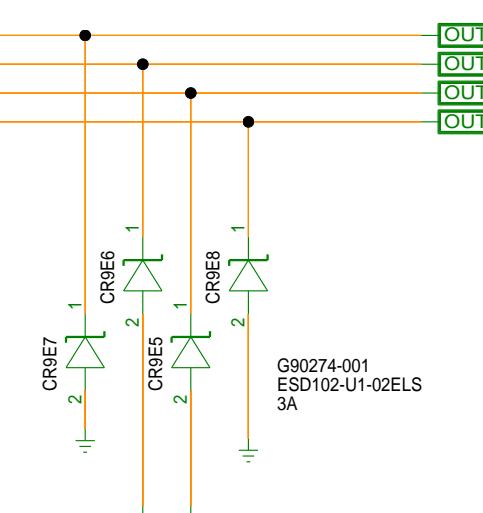
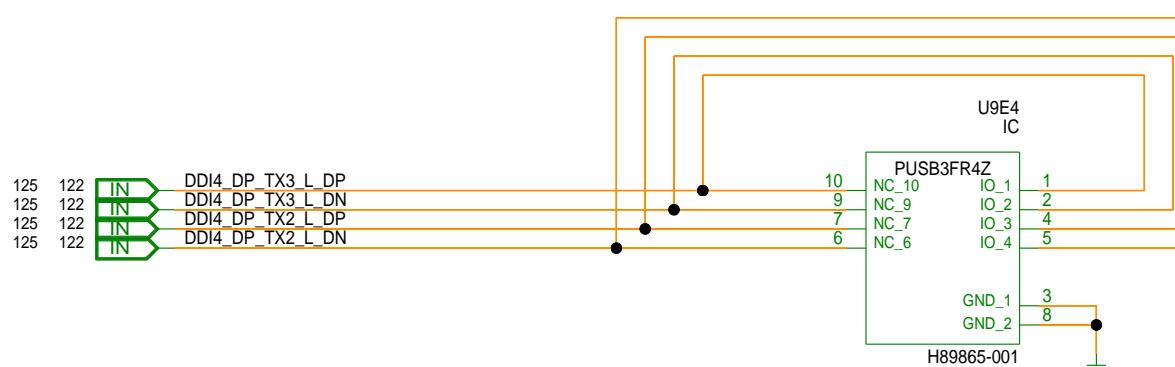
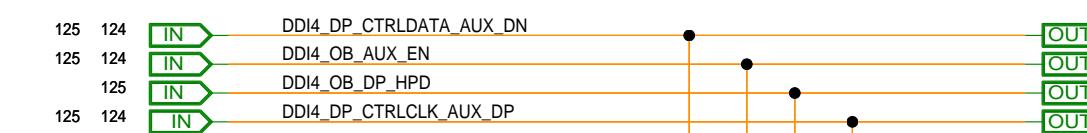
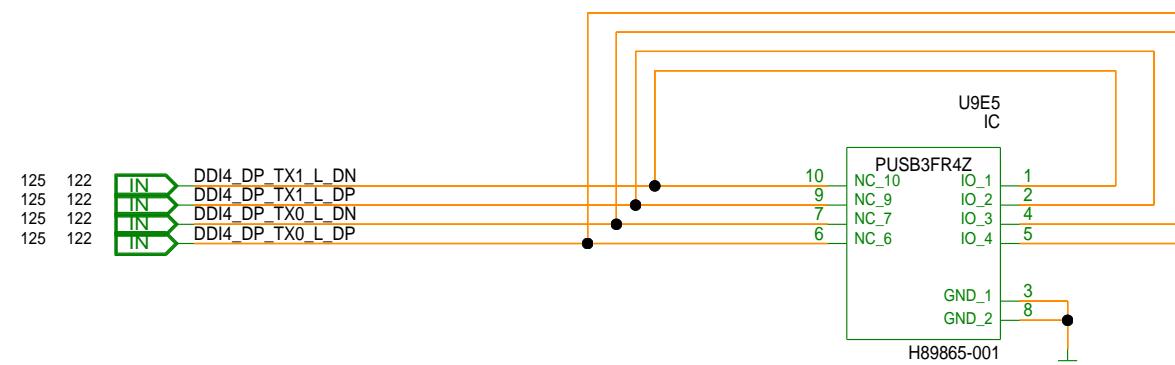




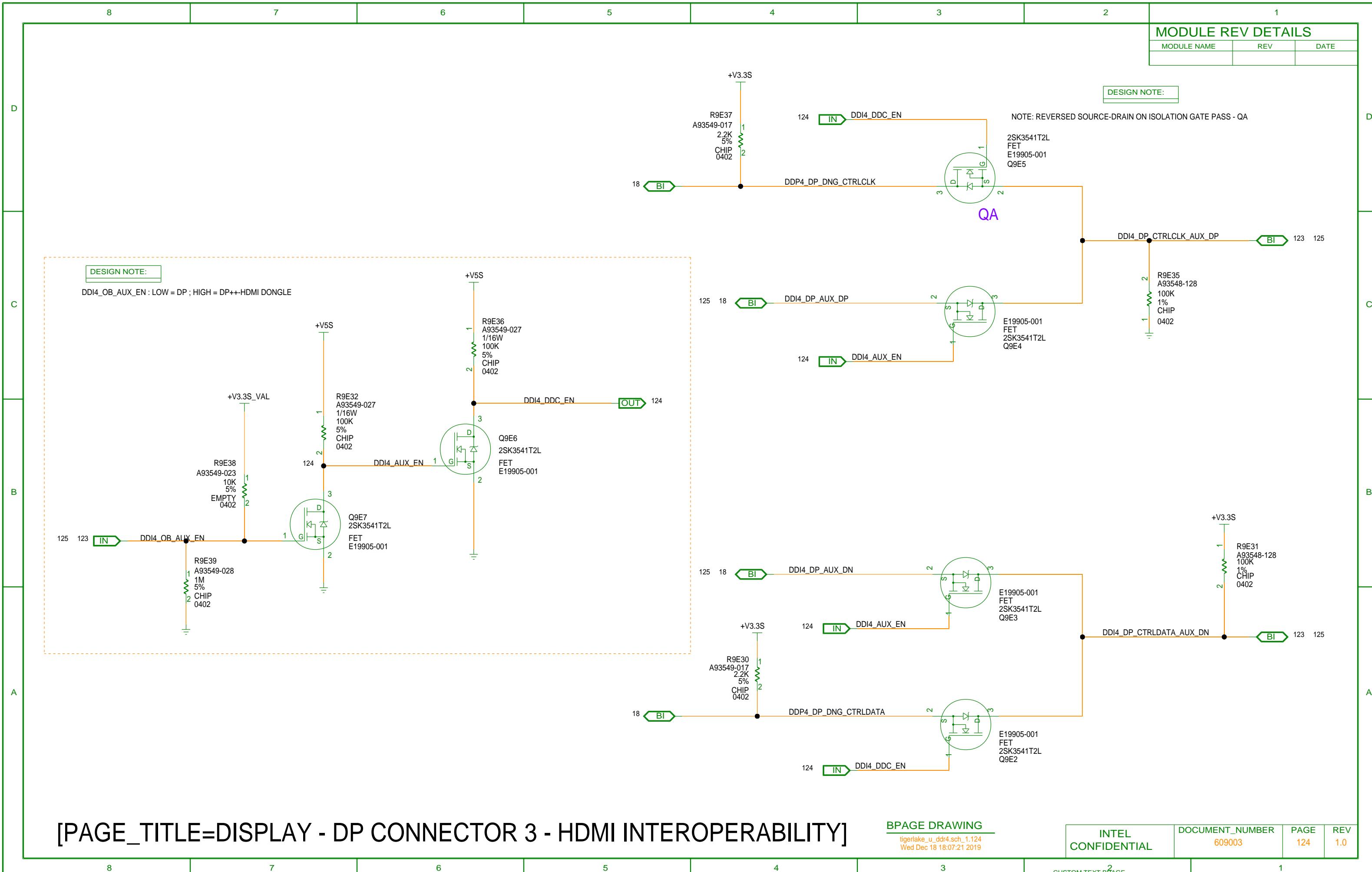
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# DP CONNECTOR 3 - ESD

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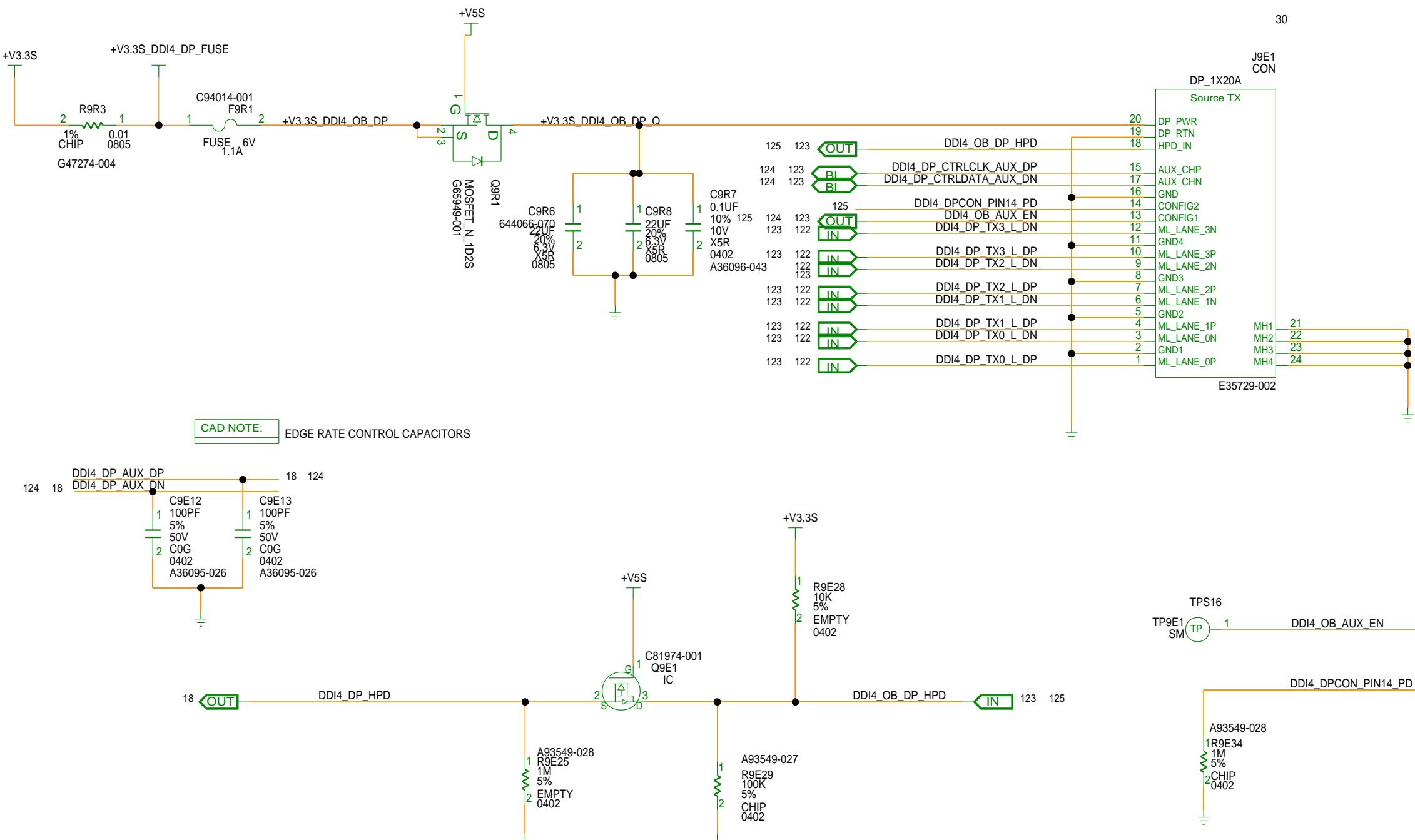


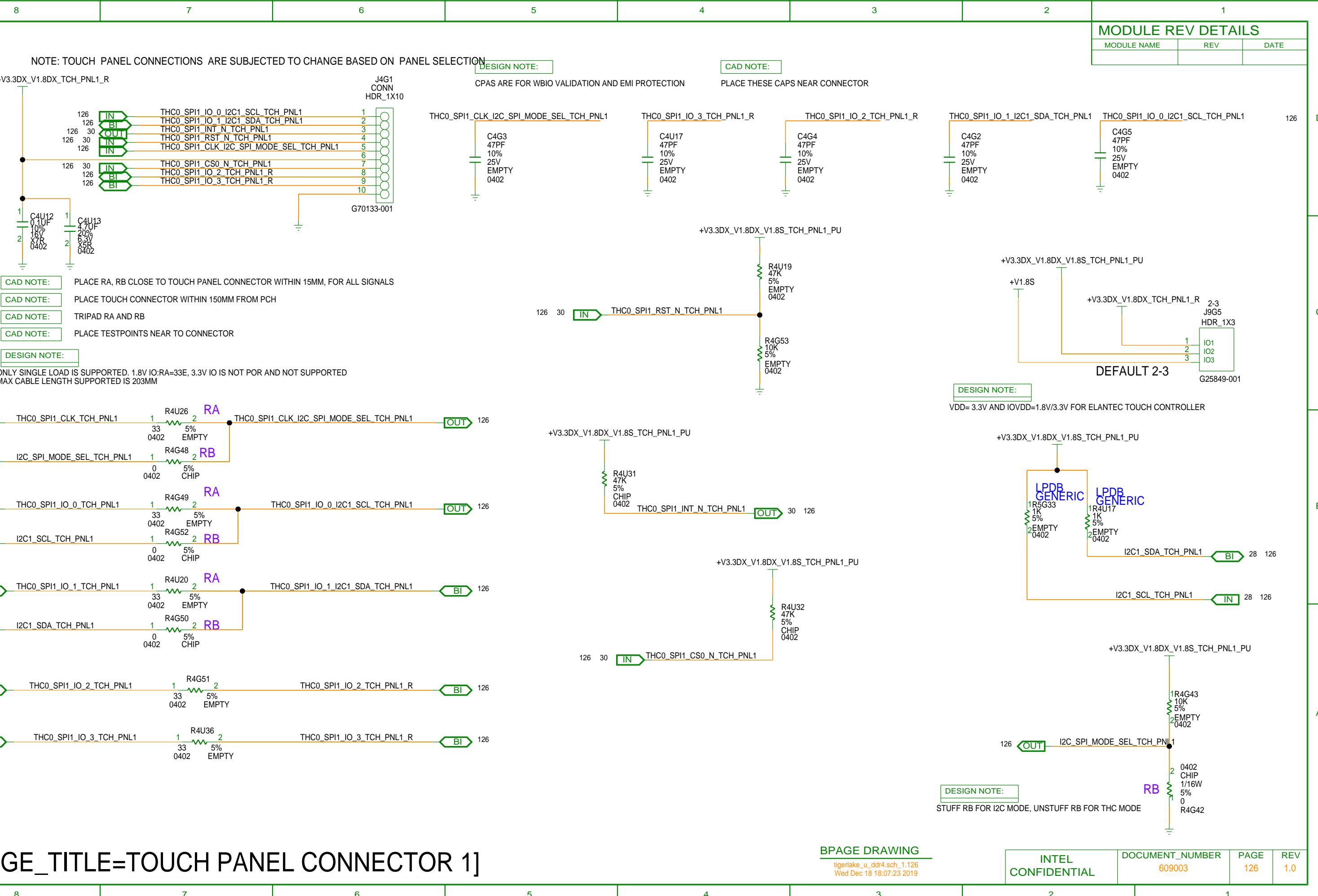
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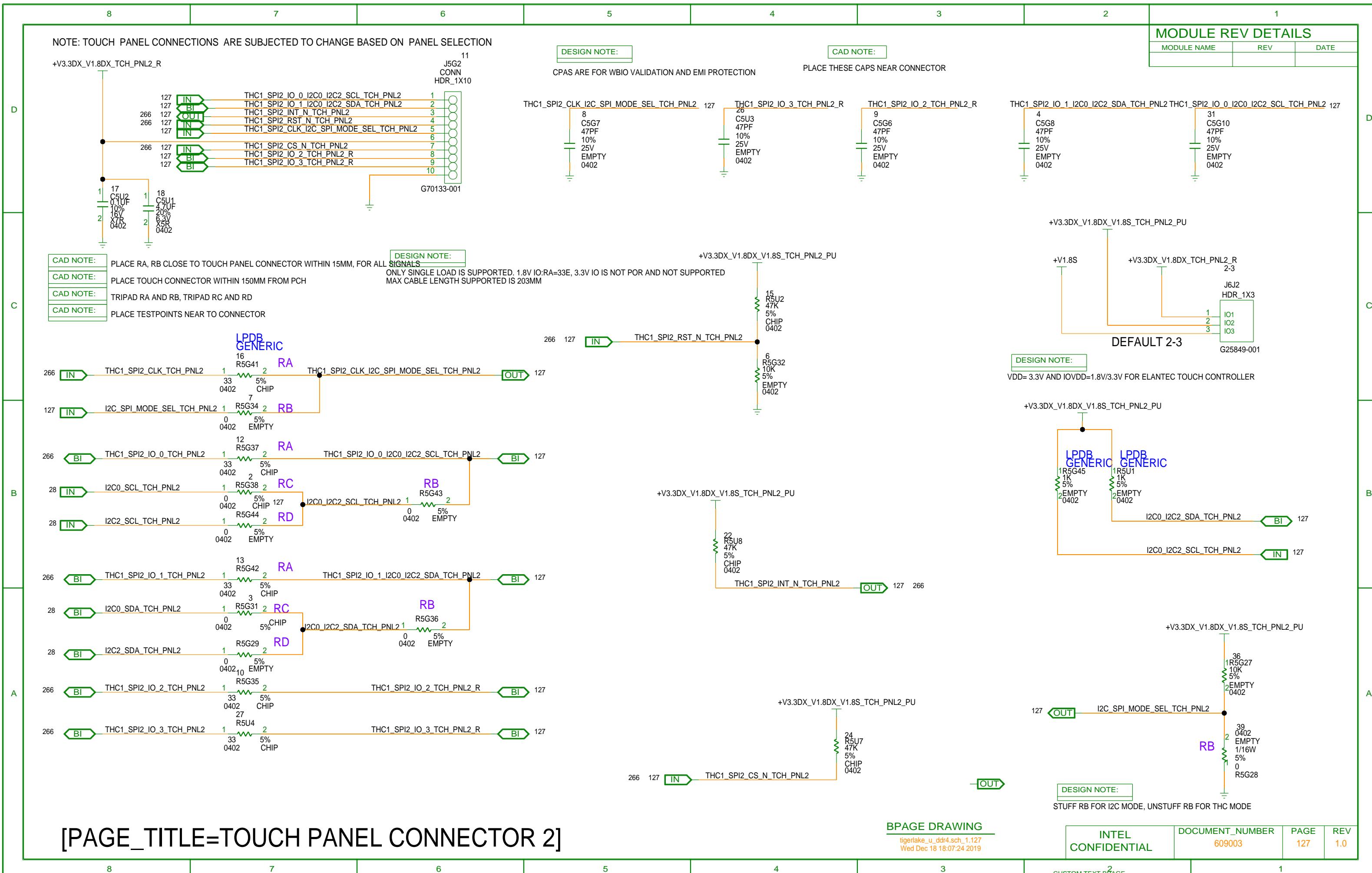


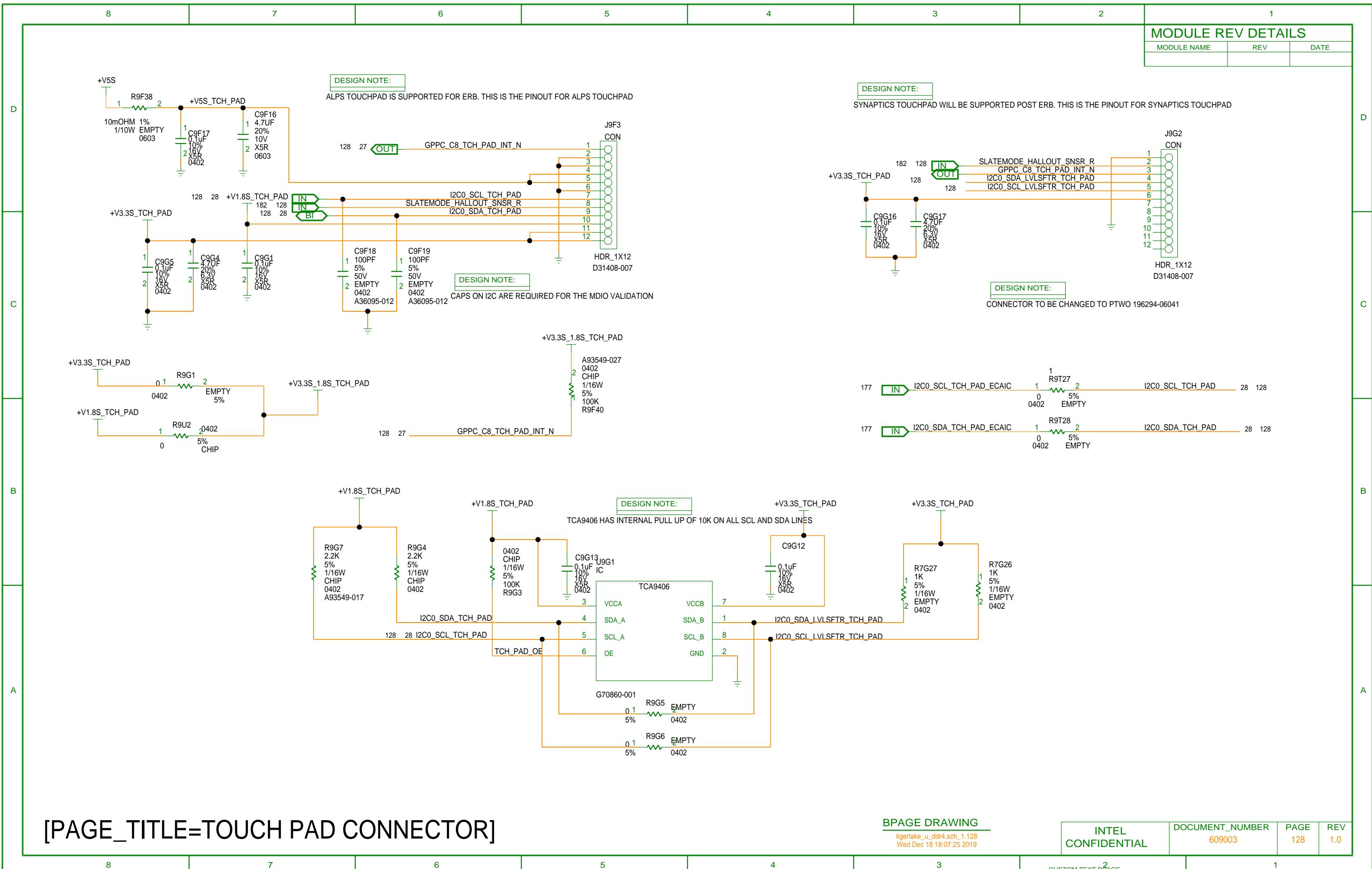
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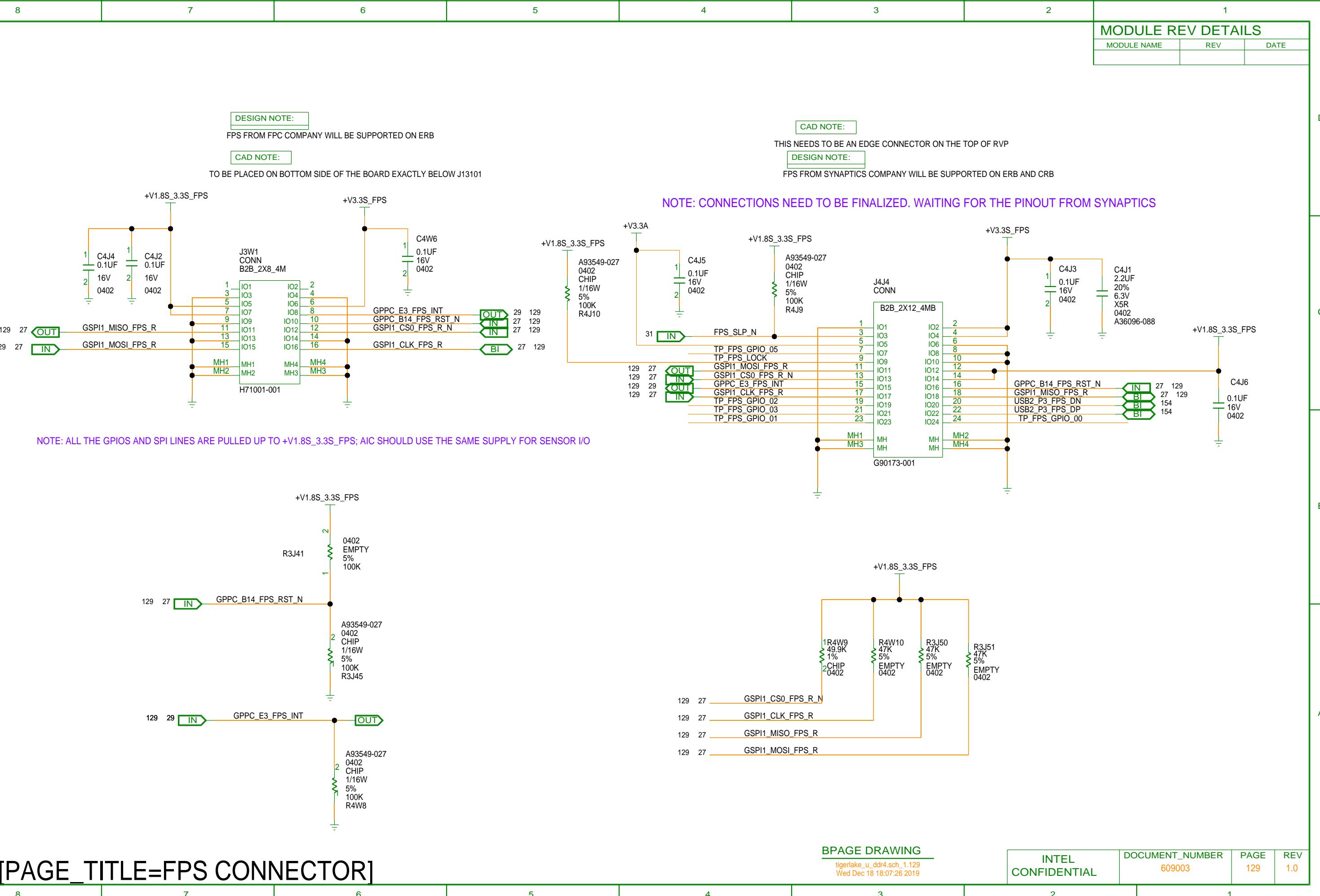
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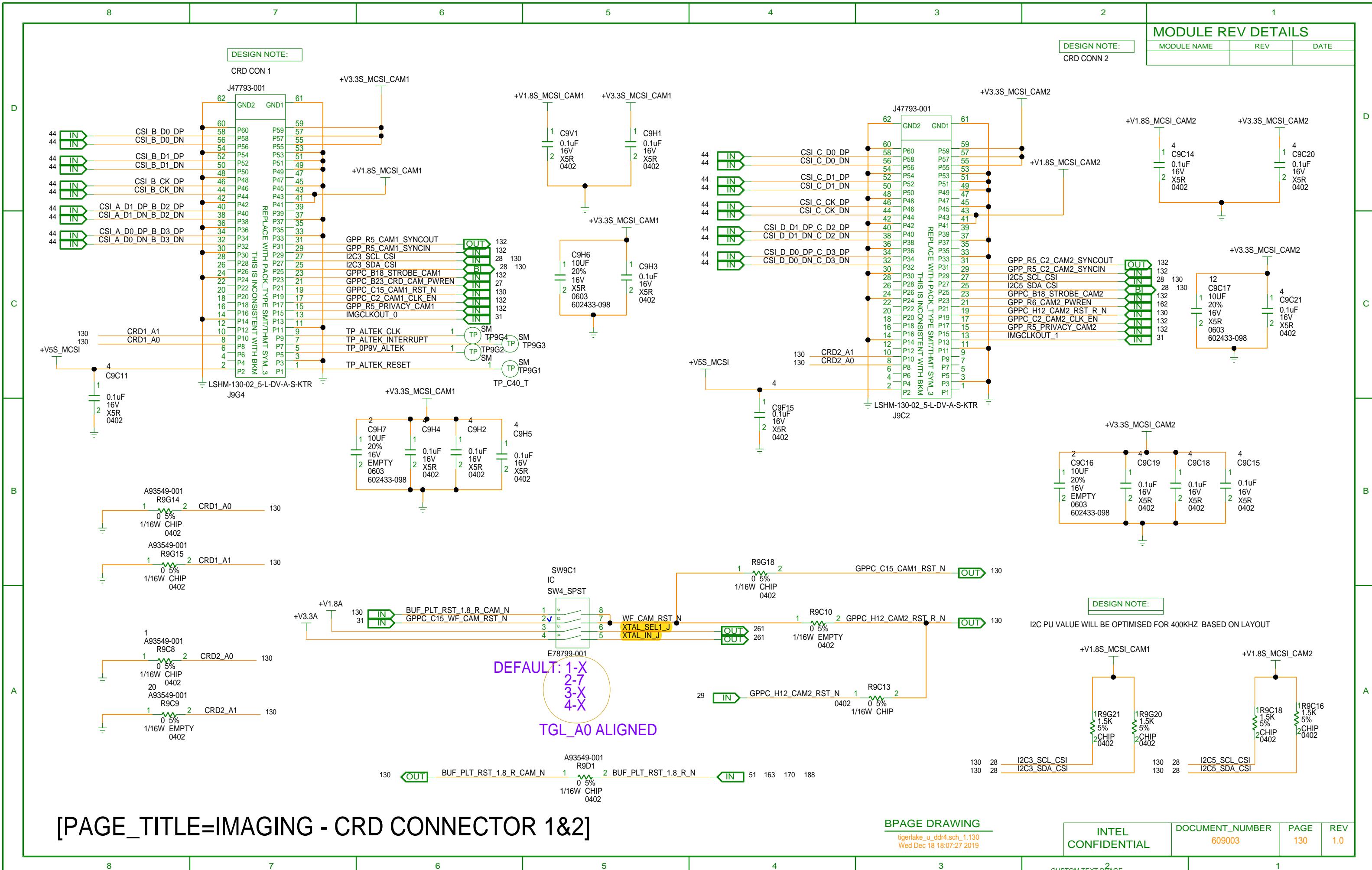








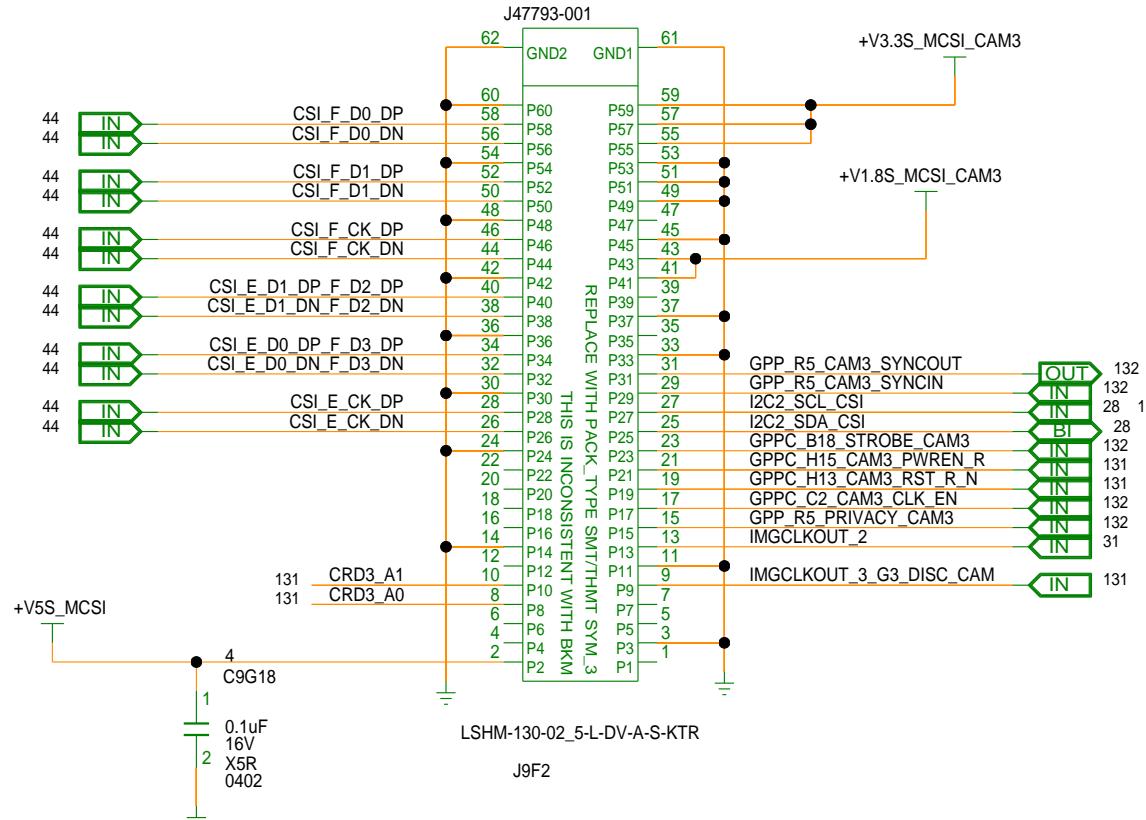




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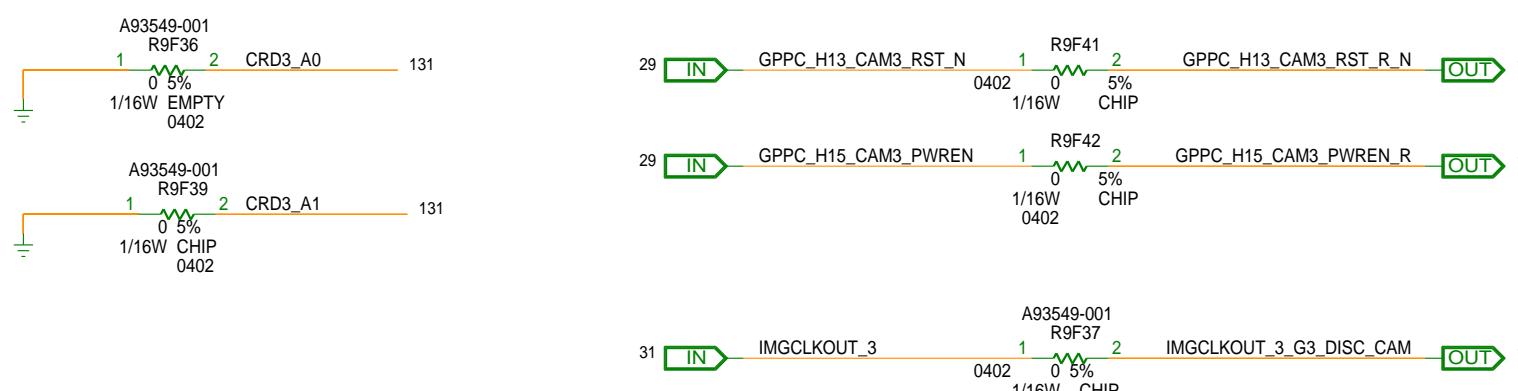
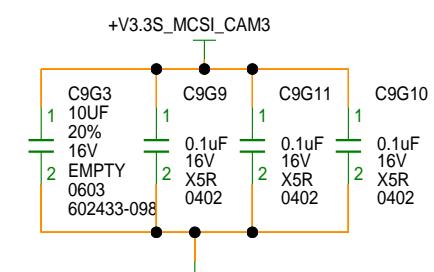
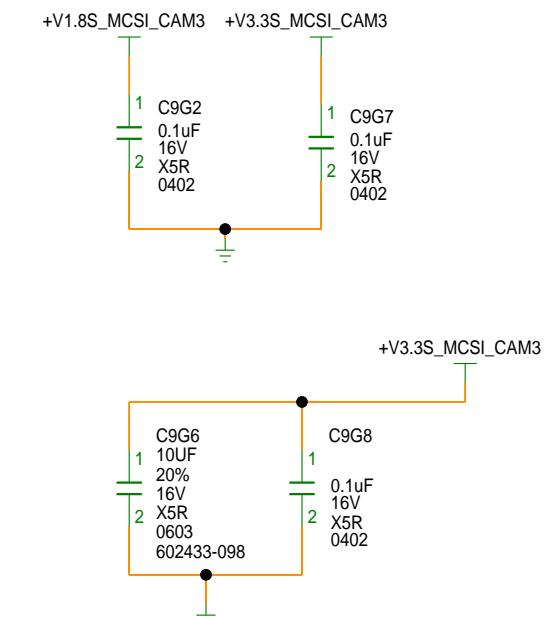
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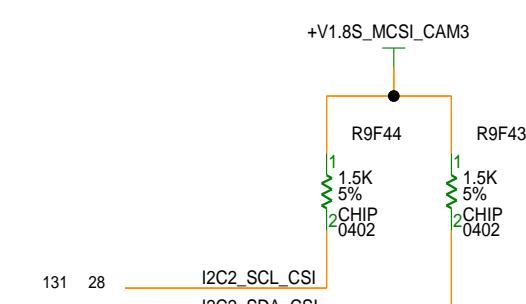


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I2C PU VALUE WILL BE OPTIMISED FOR 400KHZ BASED ON LAYOUT



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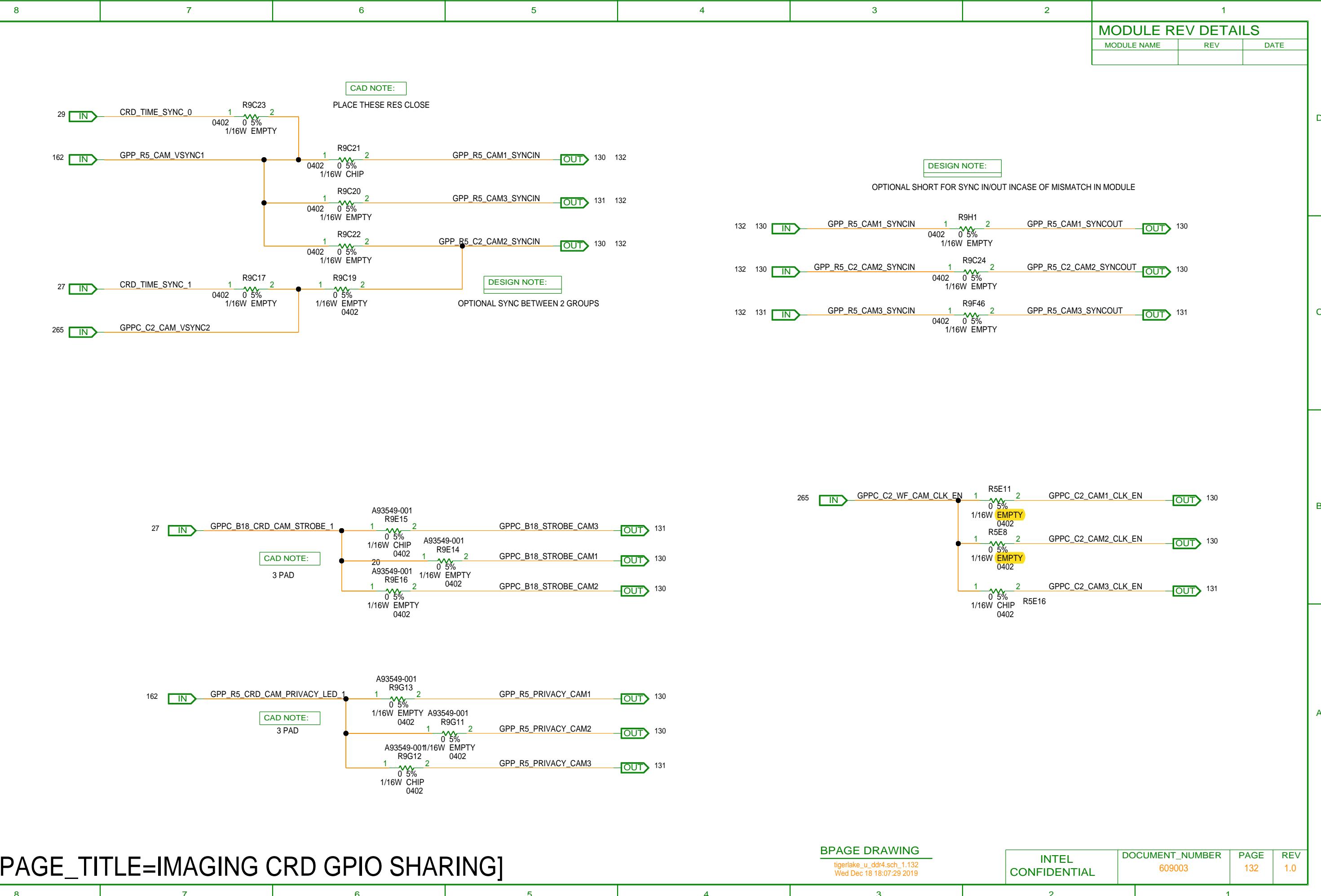
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CUSTOM TEXT BPAGE



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**MODULE REV DETAILS**

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**MODULE REV DETAILS**

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Tue Oct 15 12:50:31 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
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|                       | 609003          | 134  | 1.0 |

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CUSTOM TEXT 2 PAGE

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| 8                            | 7   | 6    | 5 | 4  | 3 | 2                                 | 1 |             |     |      |  |  |  |
|------------------------------|---|------|---|--|---|-----------------------------------|---|-------------|-----|------|--|--|--|
| D                            | <b>MODULE REV DETAILS</b>   |      |   |  |   |                                   |   |             |     |      |  |  |  |
|                              | <table border="1"> <thead> <tr> <th>MODULE NAME</th><th>REV</th><th>DATE</th></tr> </thead> <tbody> <tr> <td></td><td></td><td></td></tr> </tbody> </table> |      |   |  |   |                                   |   | MODULE NAME | REV | DATE |  |  |  |
| MODULE NAME                  | REV   | DATE |   |  |   |                                   |   |             |     |      |  |  |  |
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| C                            |   |      |   |  |   |                                   | C |             |     |      |  |  |  |
| B                            |   |      |   |  |   |                                   | B |             |     |      |  |  |  |
| A                            |   |      |   |  |   |                                   | A |             |     |      |  |  |  |
| <p>[PAGE_TITLE= RESERVE]</p> |   |      |   | <u>BPAGE DRAWING</u><br><small>tigerlake_u_ddr4.sch_1.135<br/>Tue Oct 15 12:50:32 2019</small> |   |                                   |   |             |     |      |  |  |  |
| 8                            | 7   | 6    | 5 | 4  | 3 | CUSTOM TEXT <small>2</small> PAGE | 1 |             |     |      |  |  |  |

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**MODULE REV DETAILS**

| MODULE NAME | REV | DATE |
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BPAGE DRAWING

tigerlake\_u\_ddr4.sch\_1.136  
Tue Oct 15 12:50:33 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
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CUSTOM TEXT 2 PAGE

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| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

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tigerlake\_u\_ddr4.sch\_1.137  
Tue Oct 15 12:50:34 2019

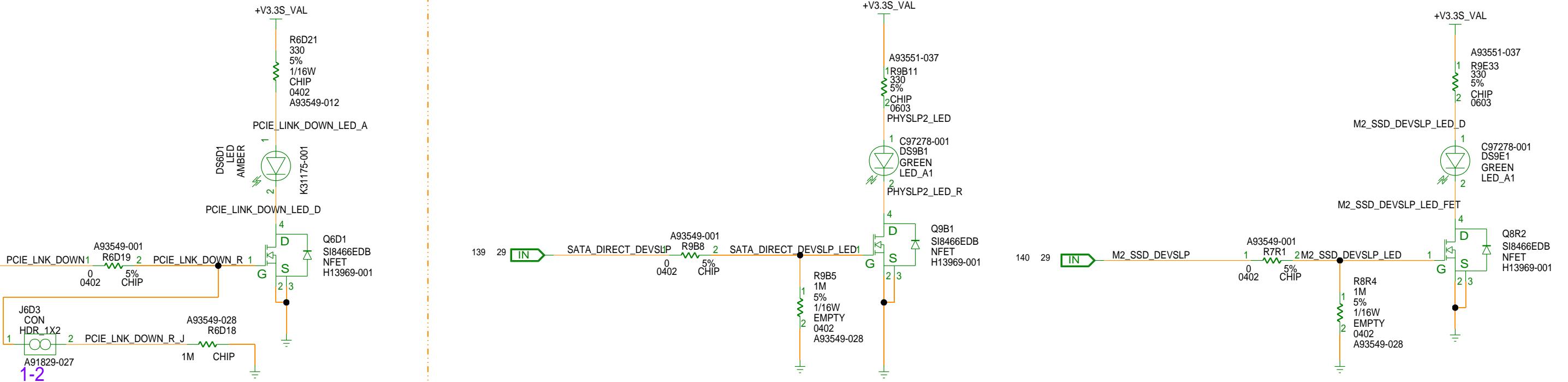
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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>137 | REV<br>1.0 |
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| 8 | 7 | 6 | 5 | 4 | 3 | CUSTOM TEXT 2 PAGE | 1 |
|---|---|---|---|---|---|--------------------|---|

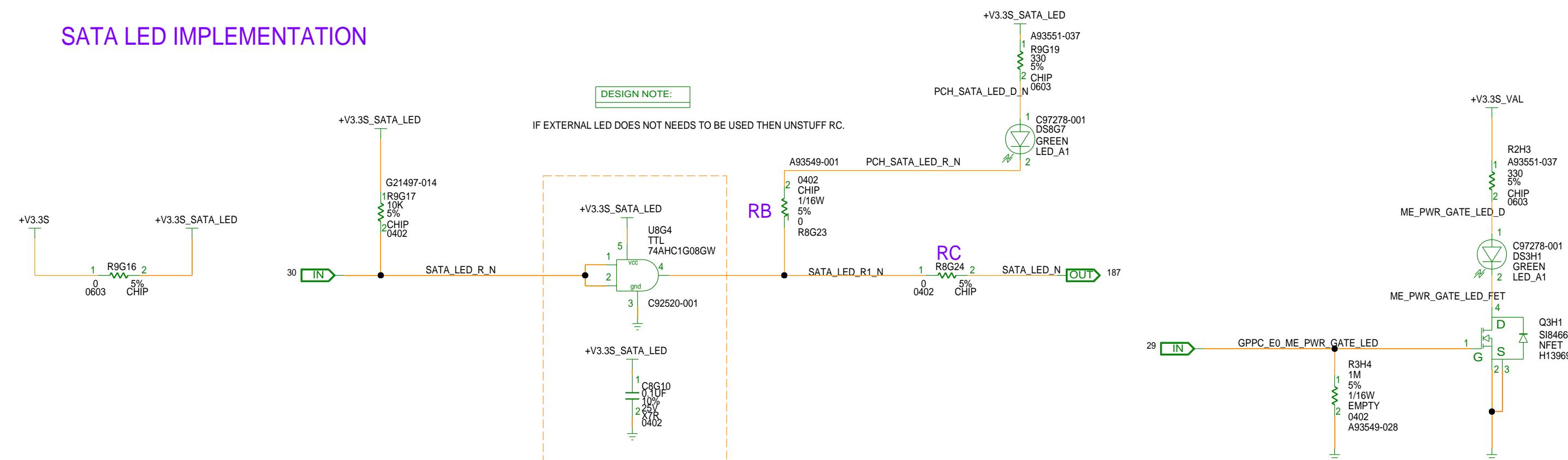
## PCIE\_LINK\_DOWN\_LED

## SATA DEV SLEEP LED

| MODULE REV DETAILS |     |      |
|--------------------|-----|------|
| MODULE NAME        | REV | DATE |
|                    |     |      |



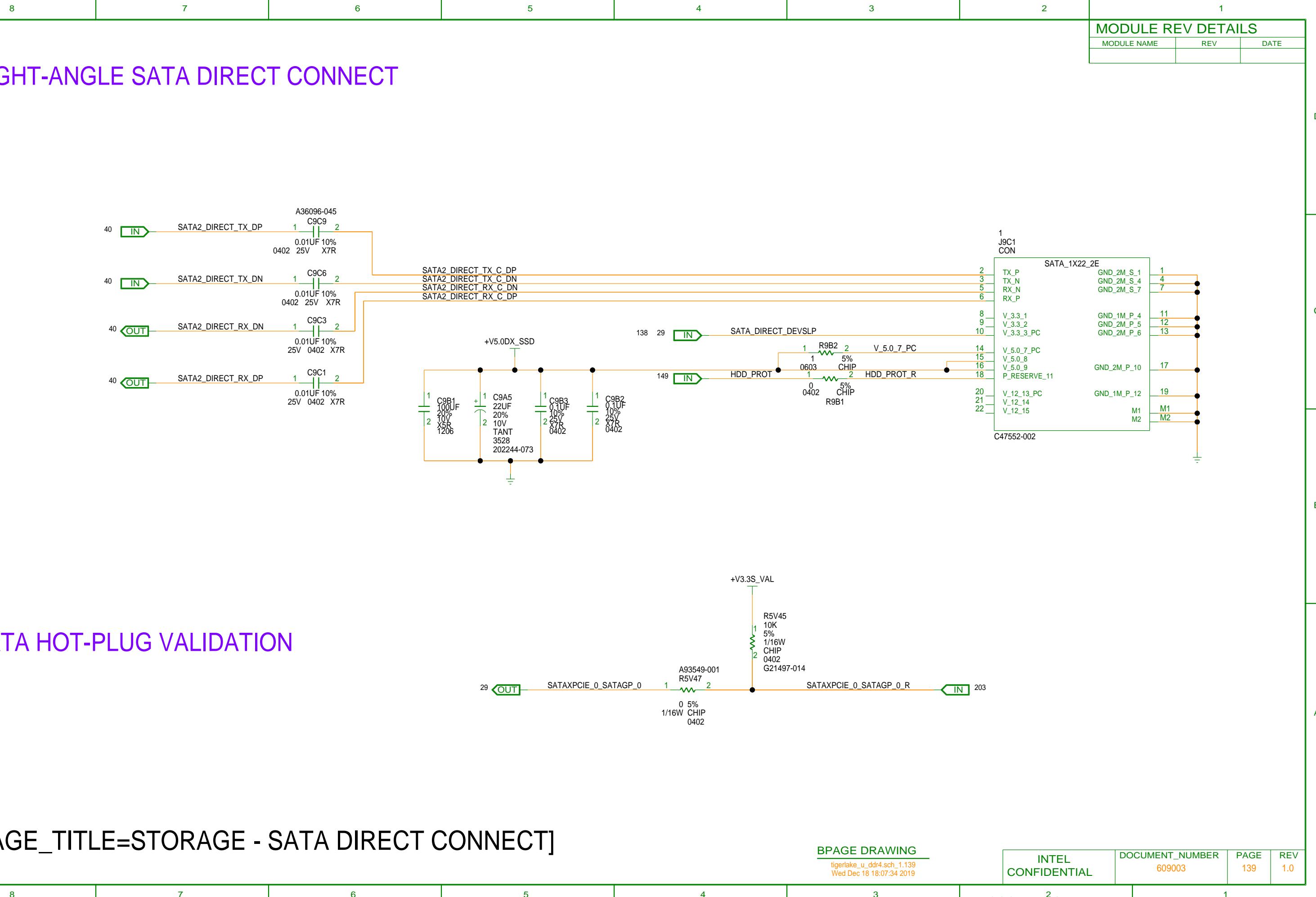
## SATA LED IMPLEMENTATION

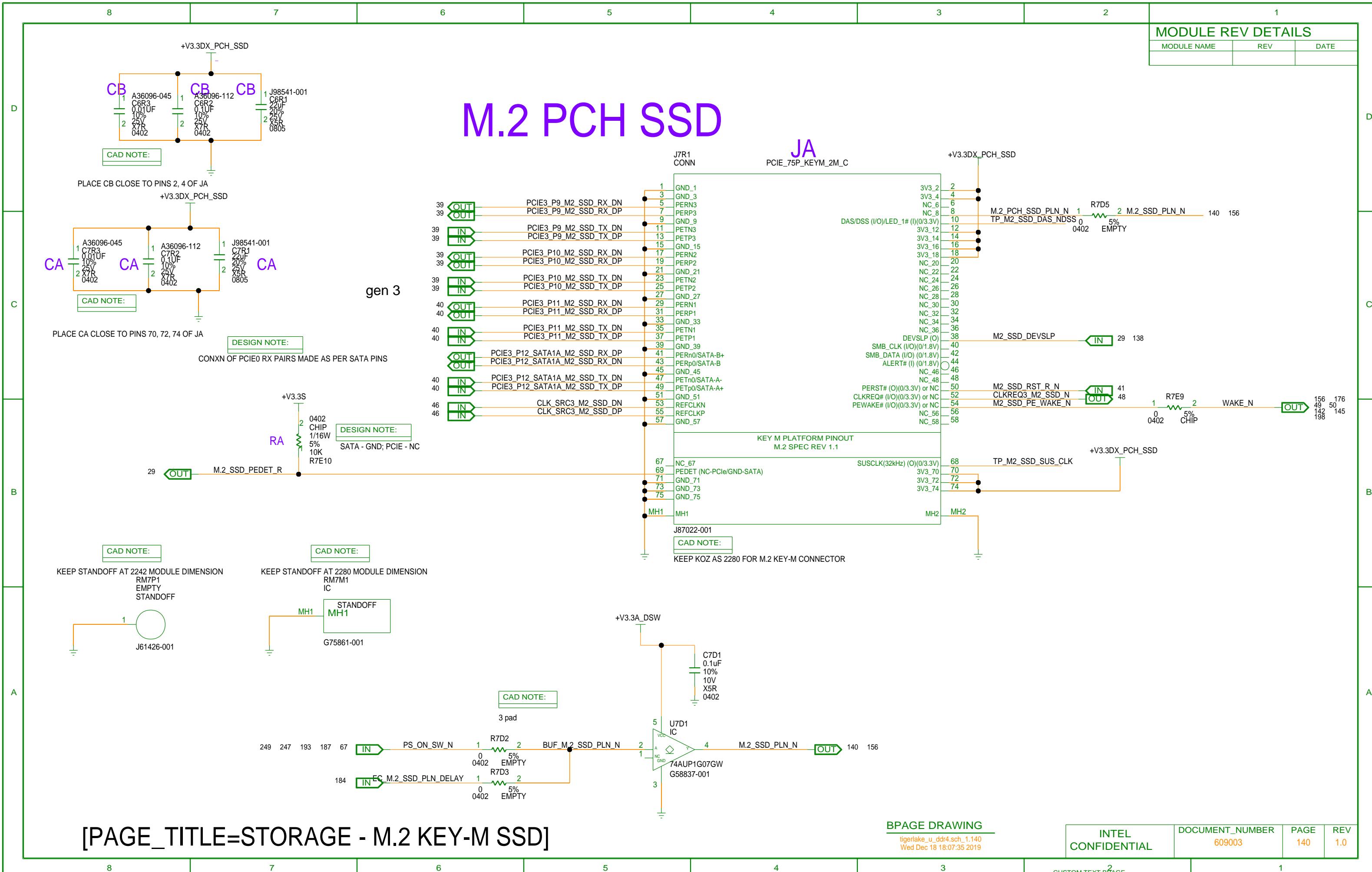


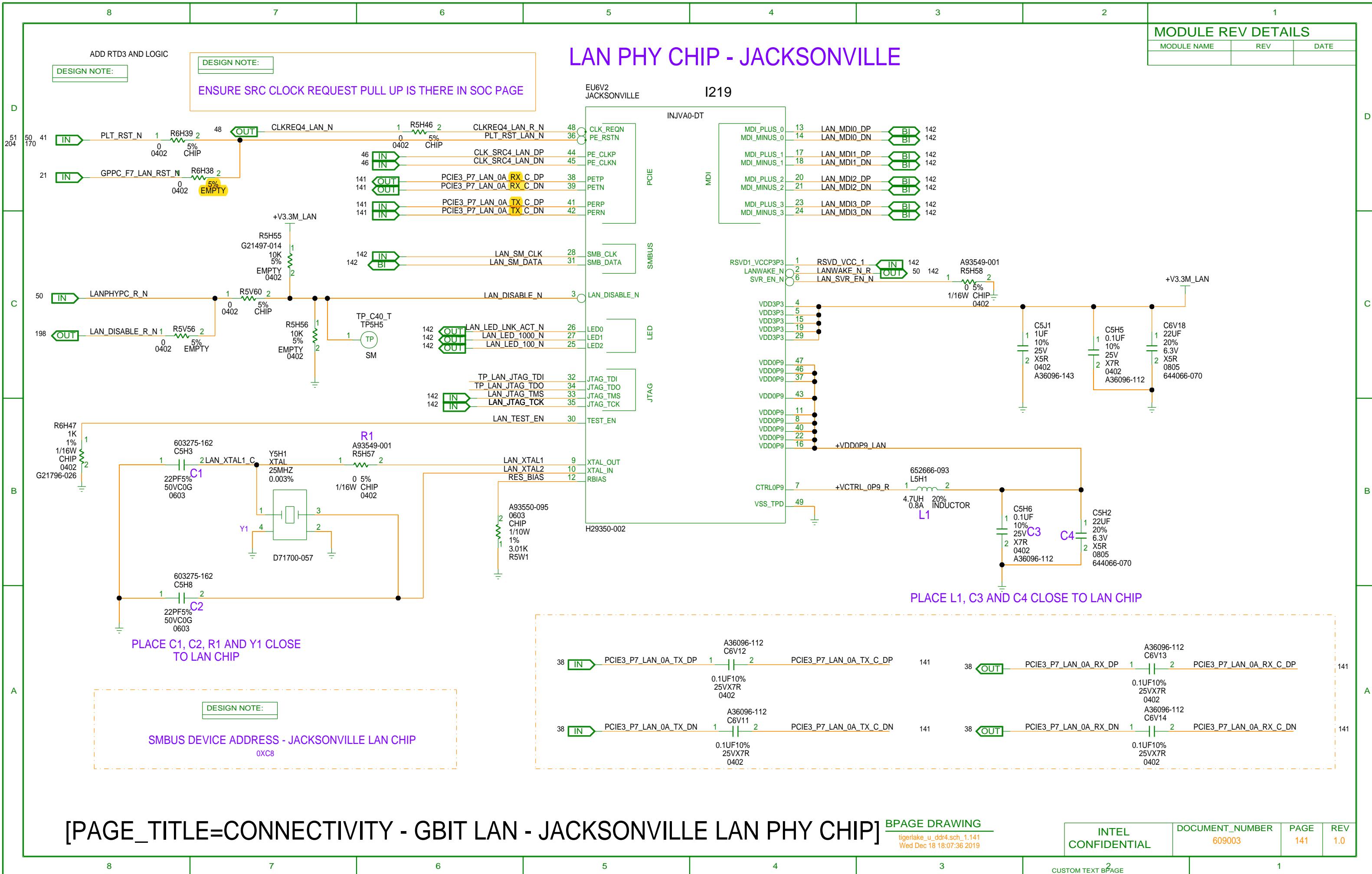
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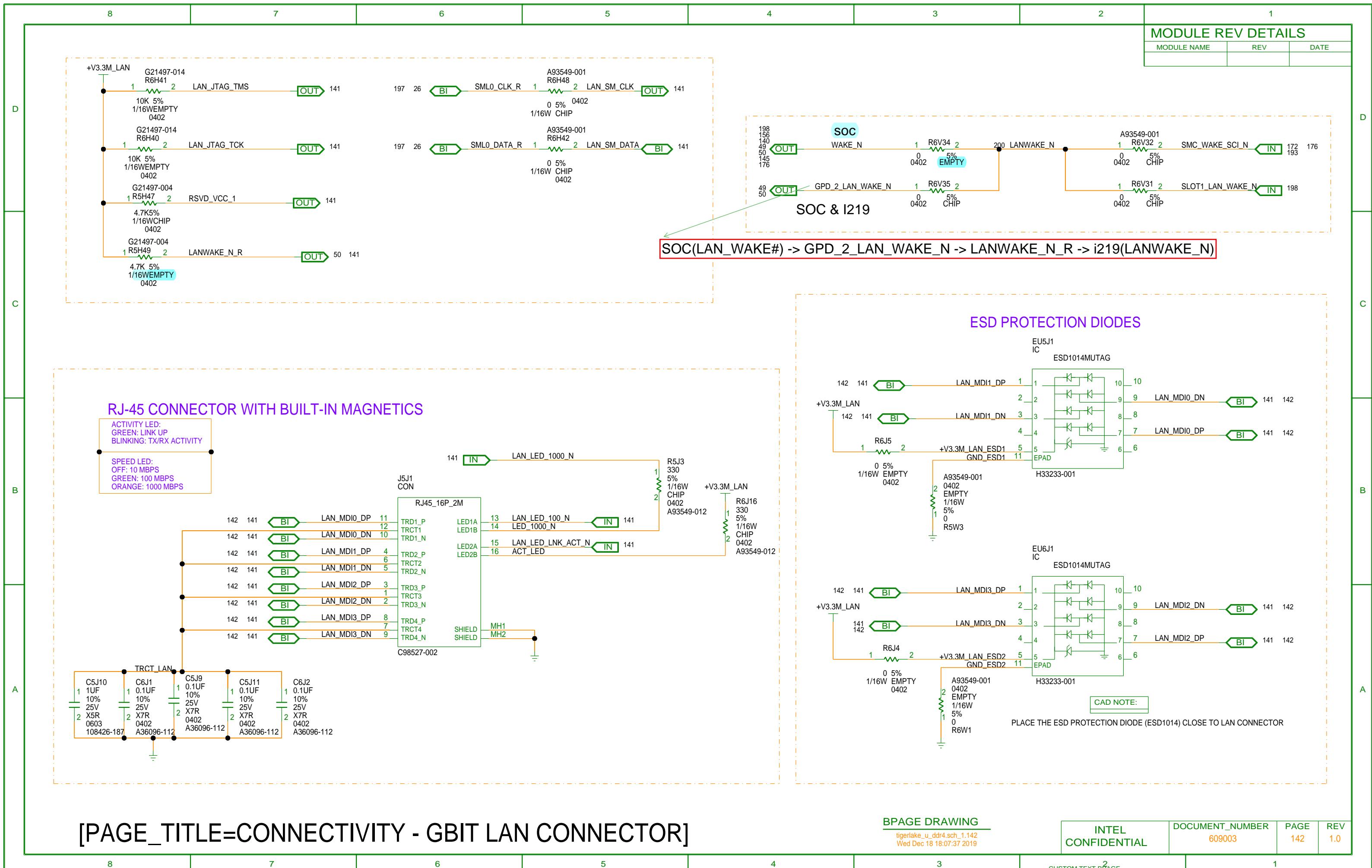
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tigerlake\_u\_ddr4.sch\_1.138  
Wed Dec 18 18:07:33 2019

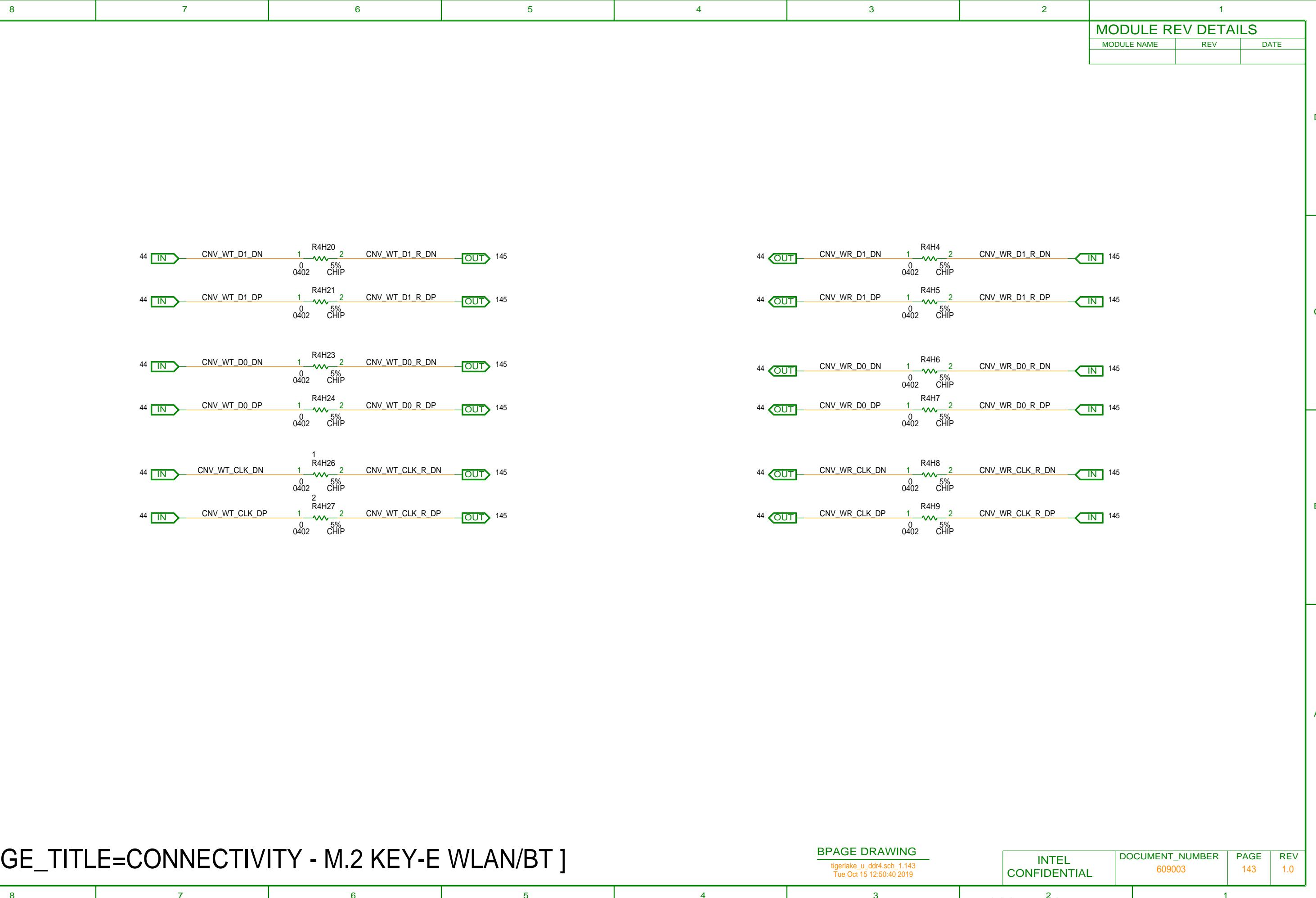
| INTEL CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
|--------------------|-----------------|------|-----|
| CUSTOM TEXT BPAGE  | 609003          | 138  | 1.0 |

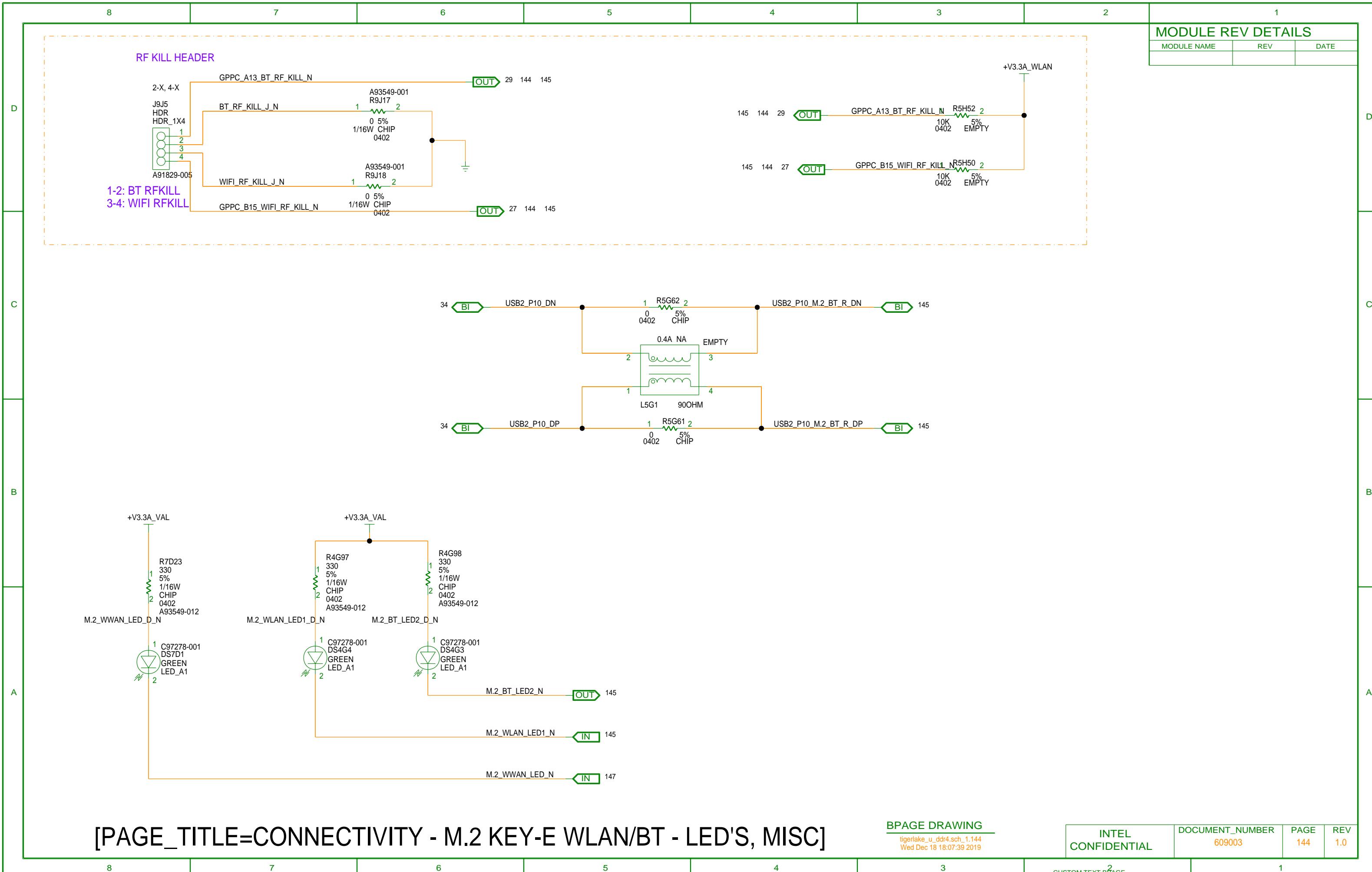


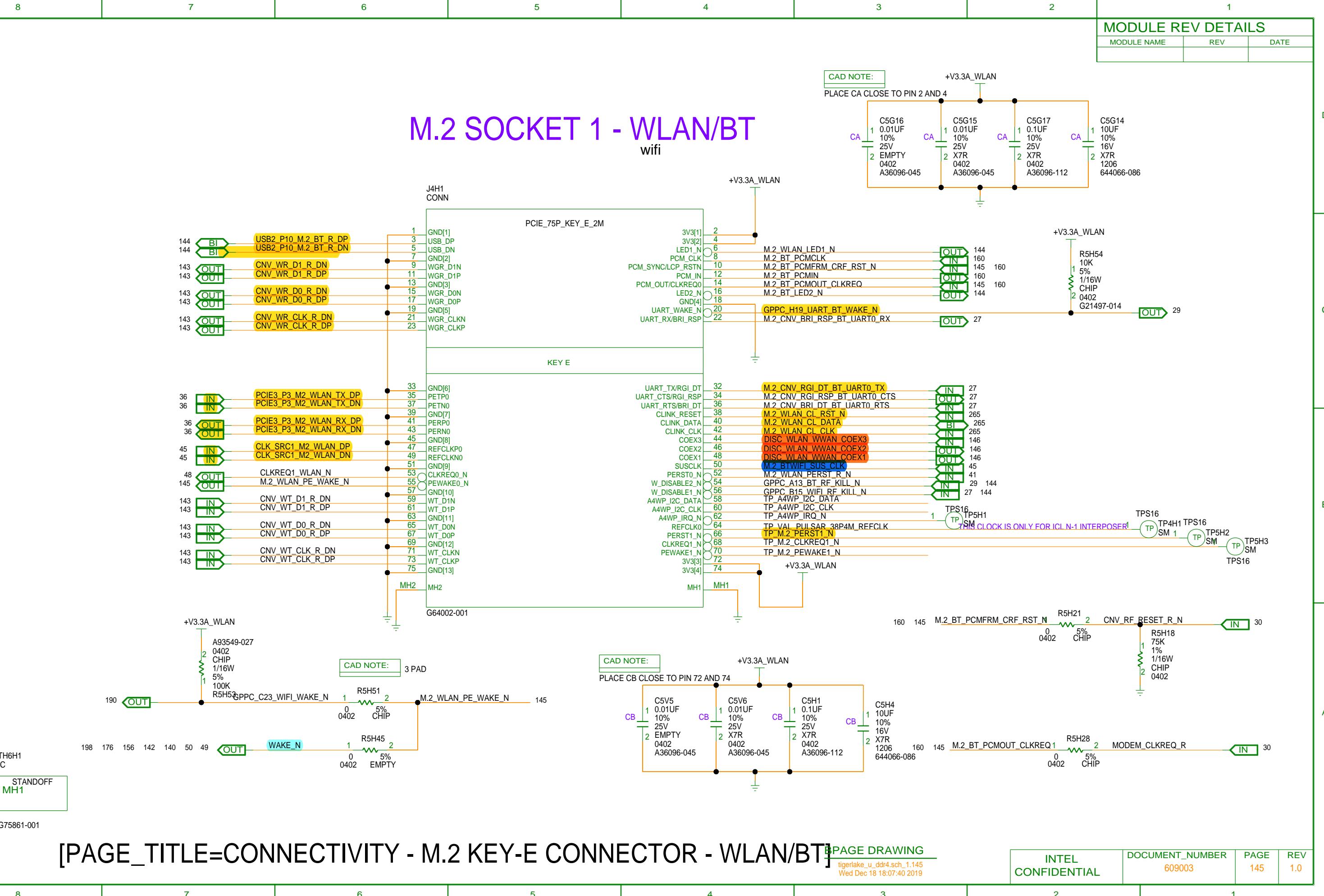


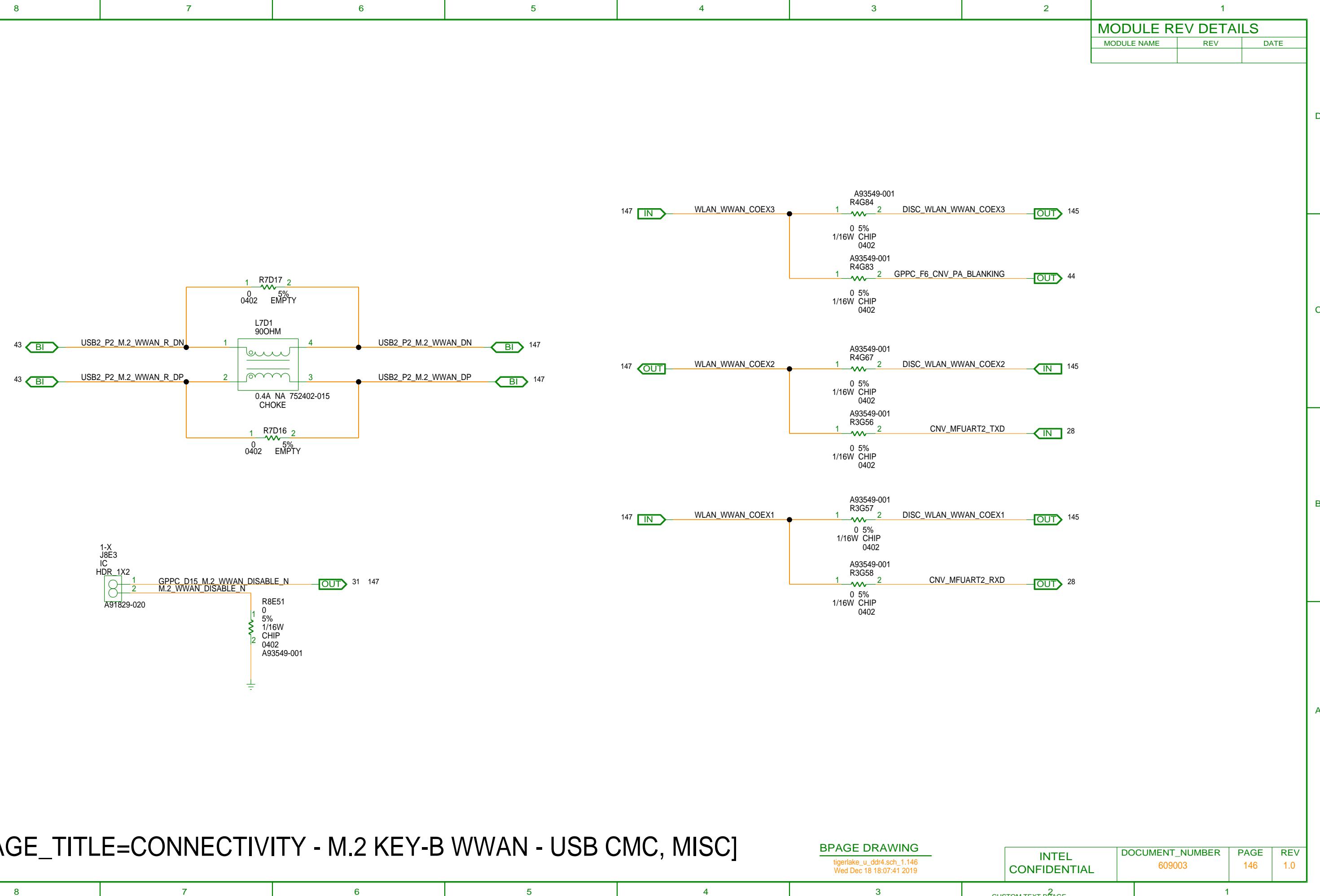


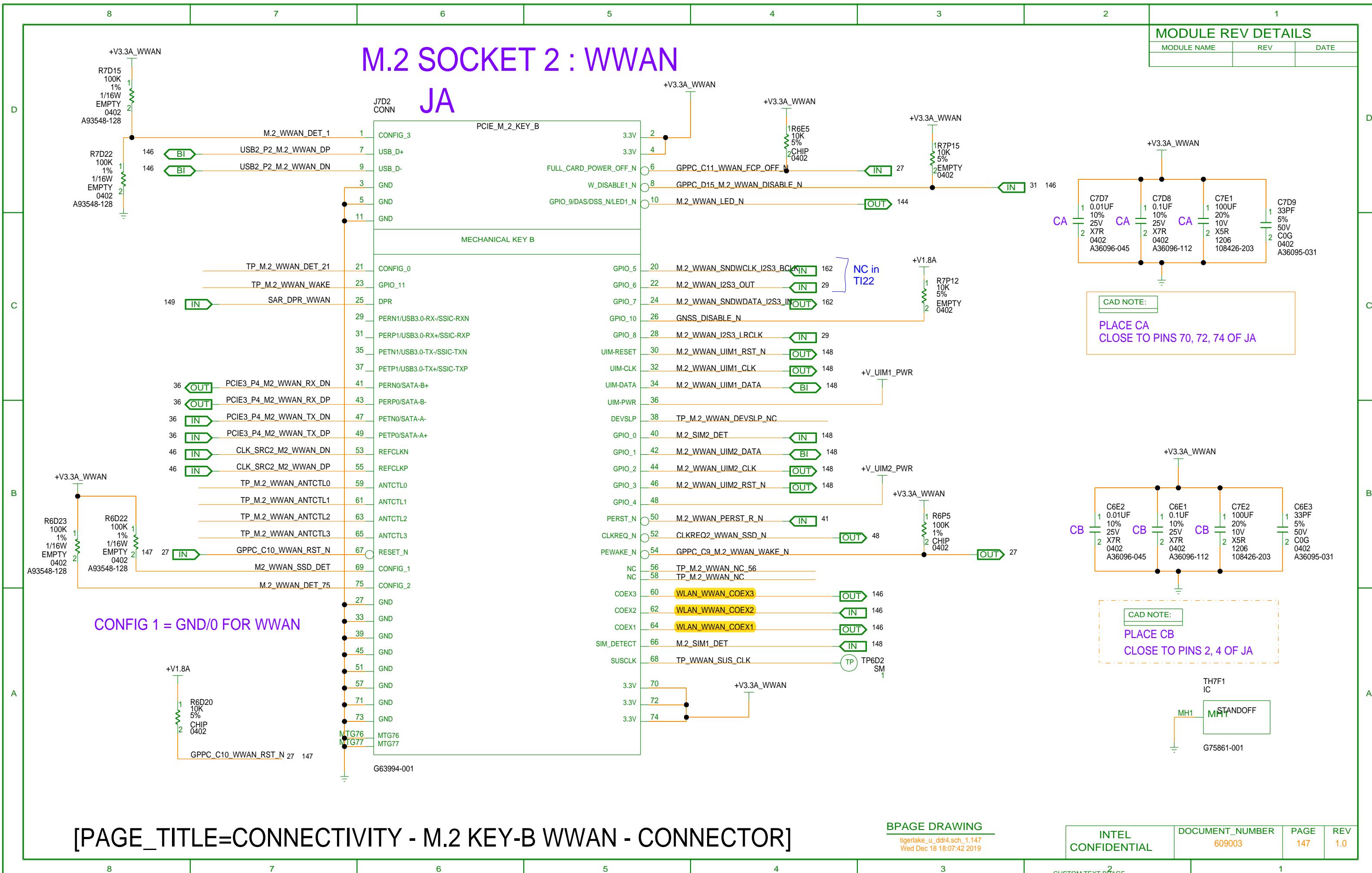


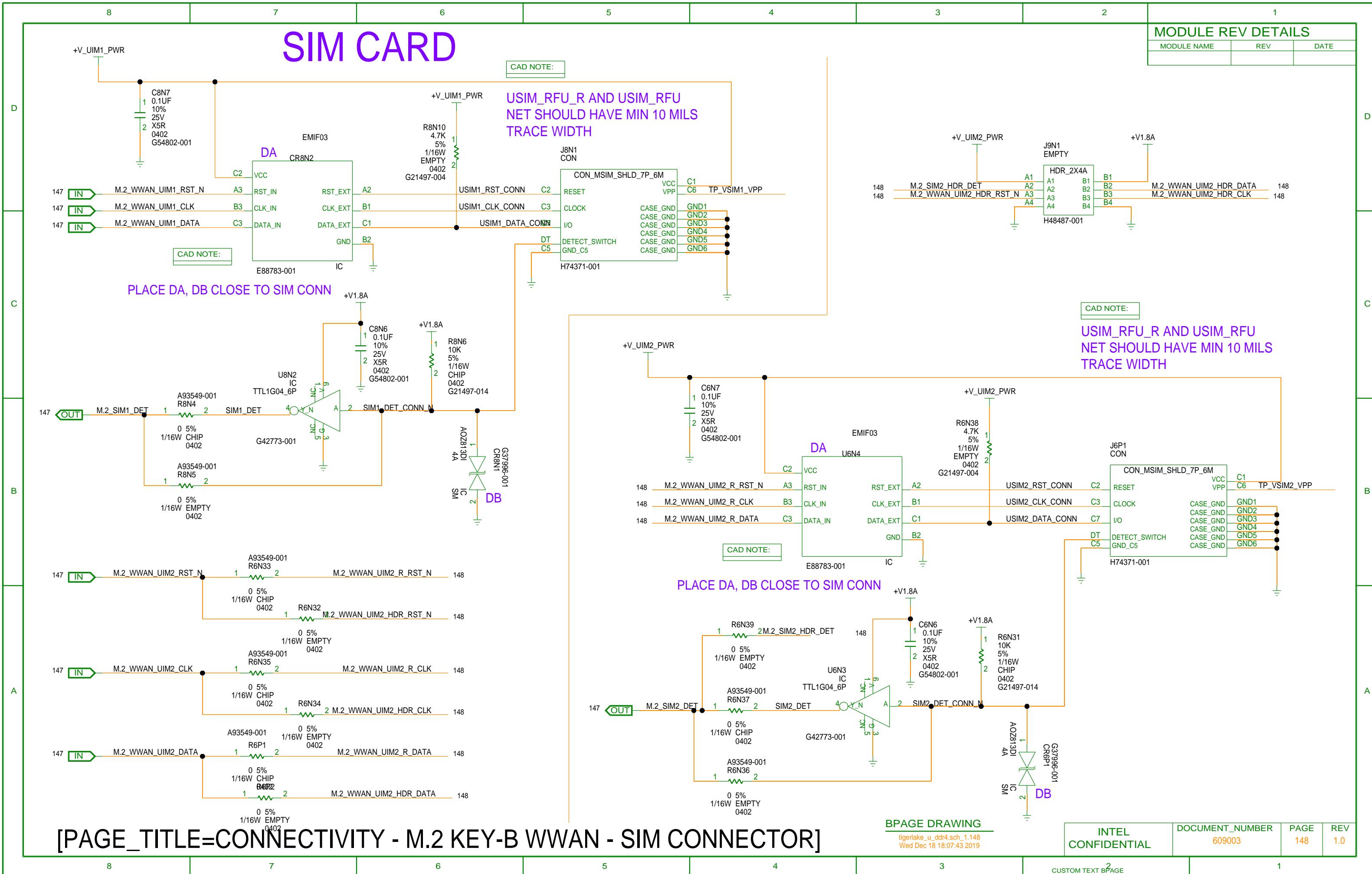


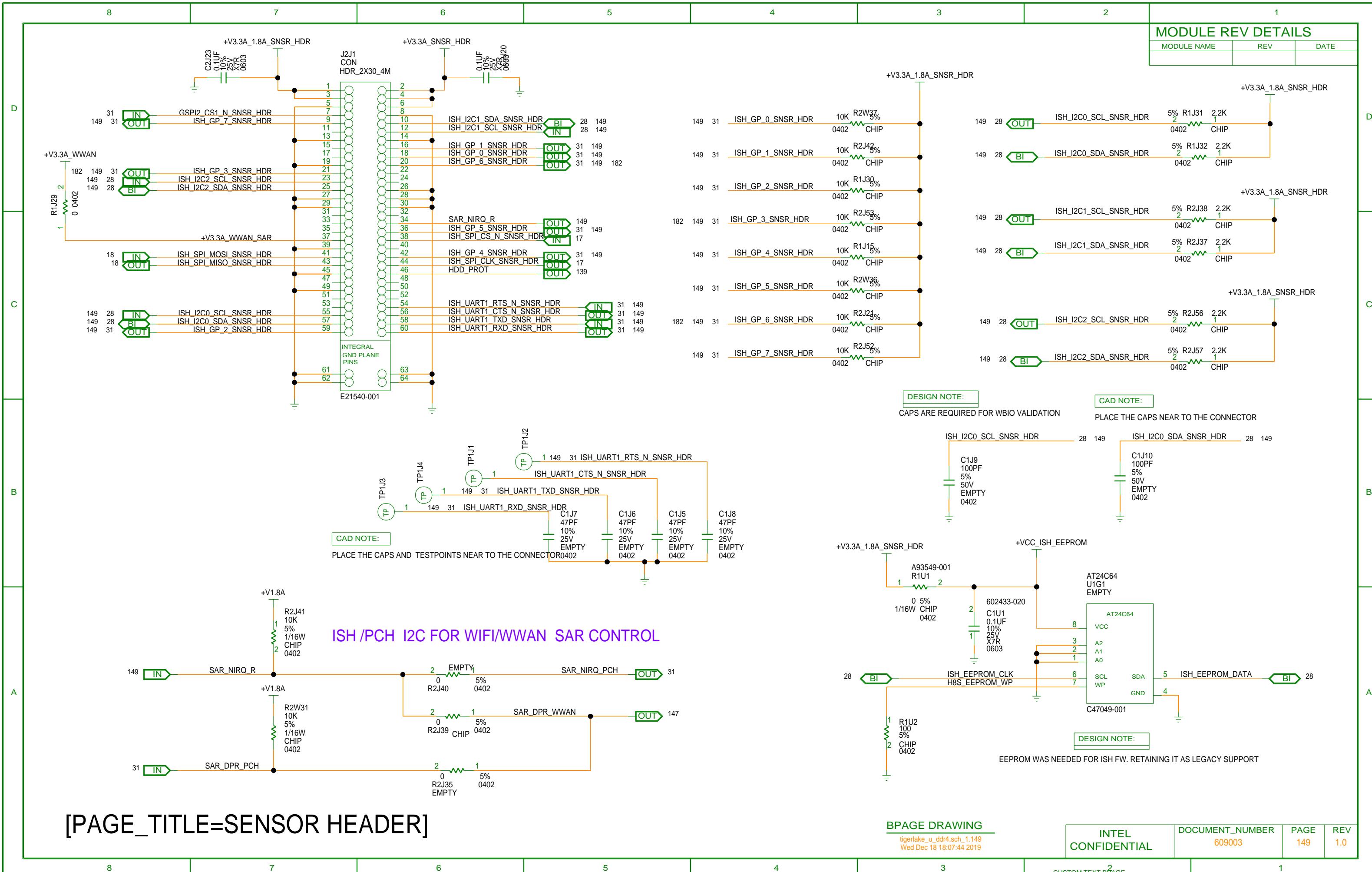






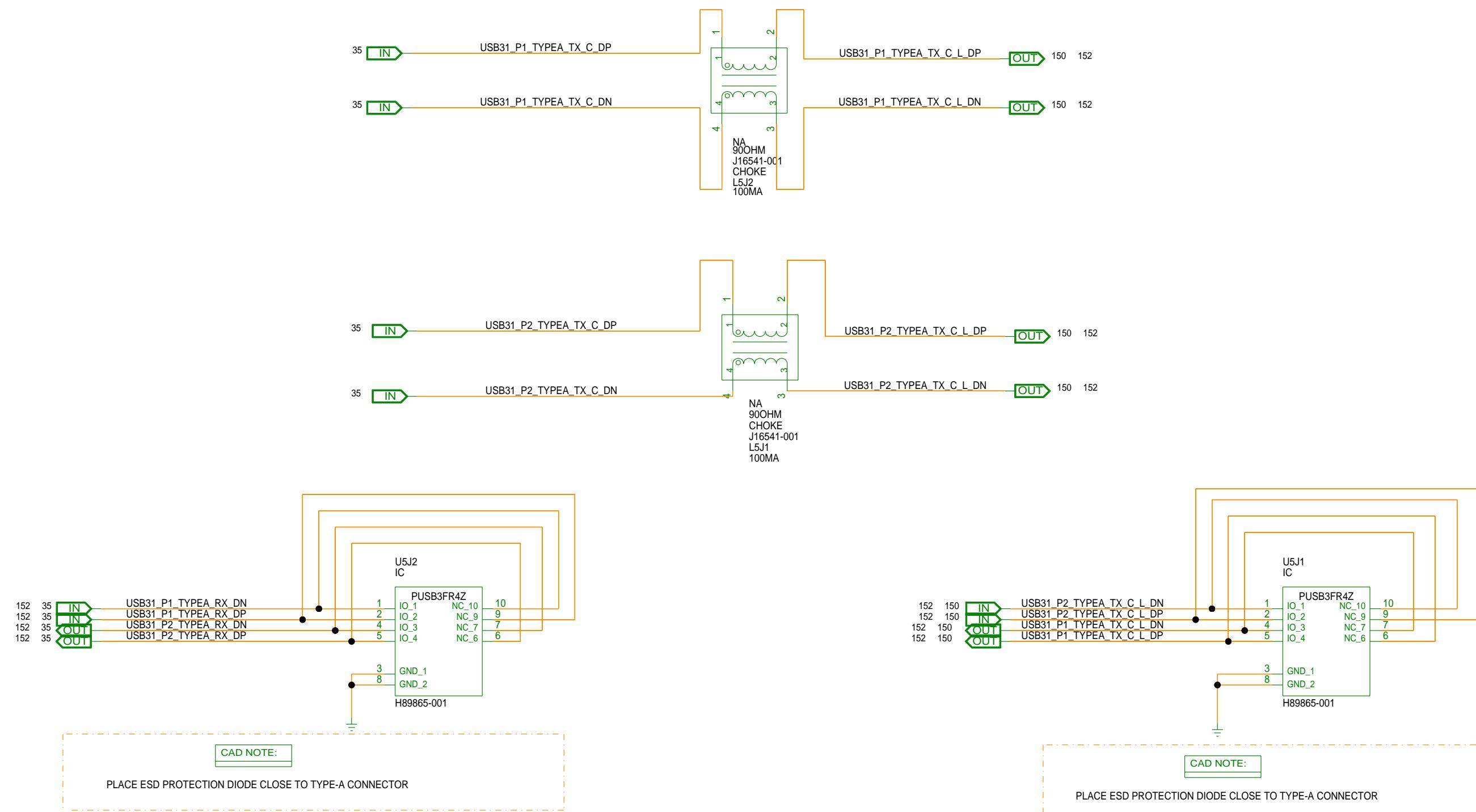


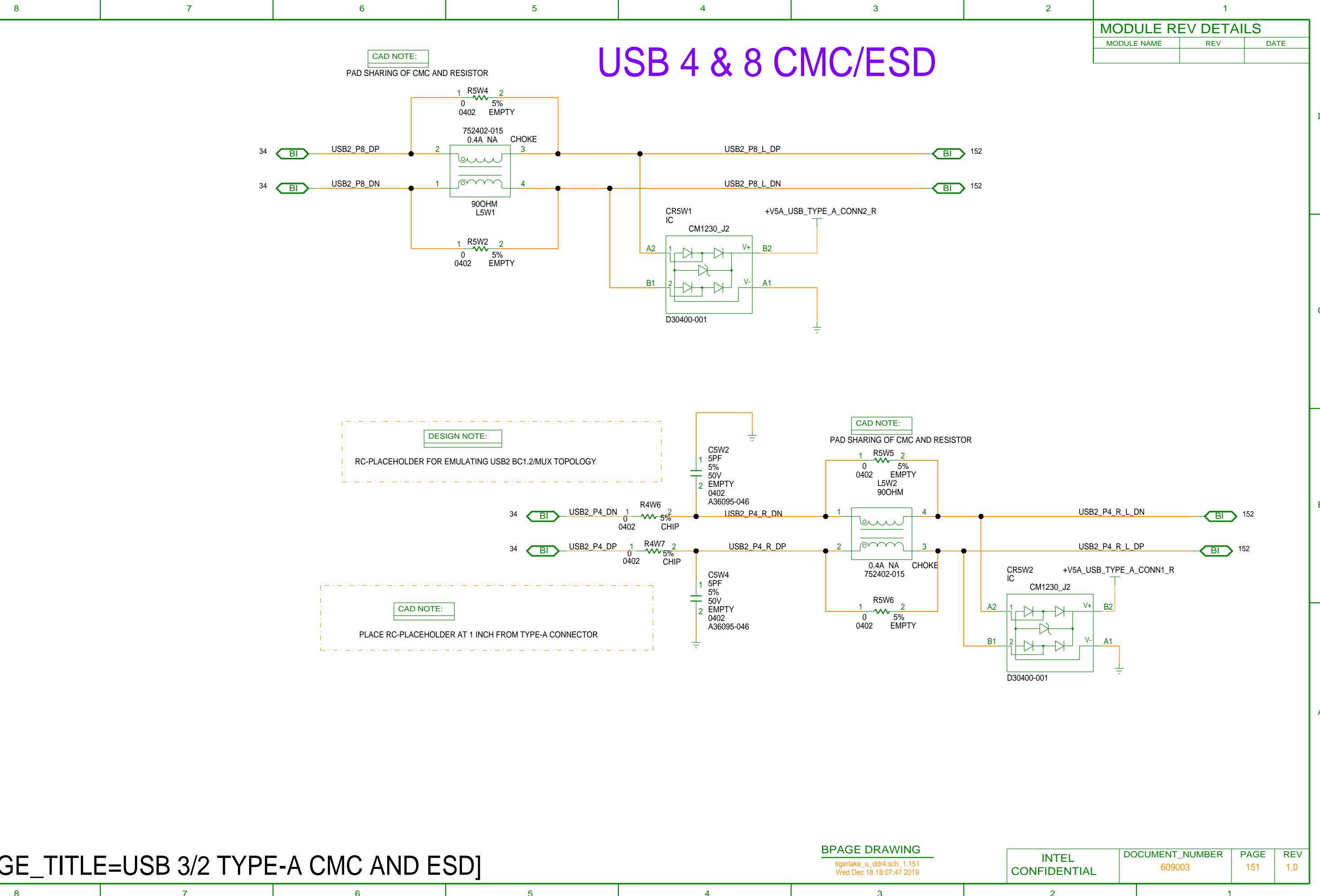


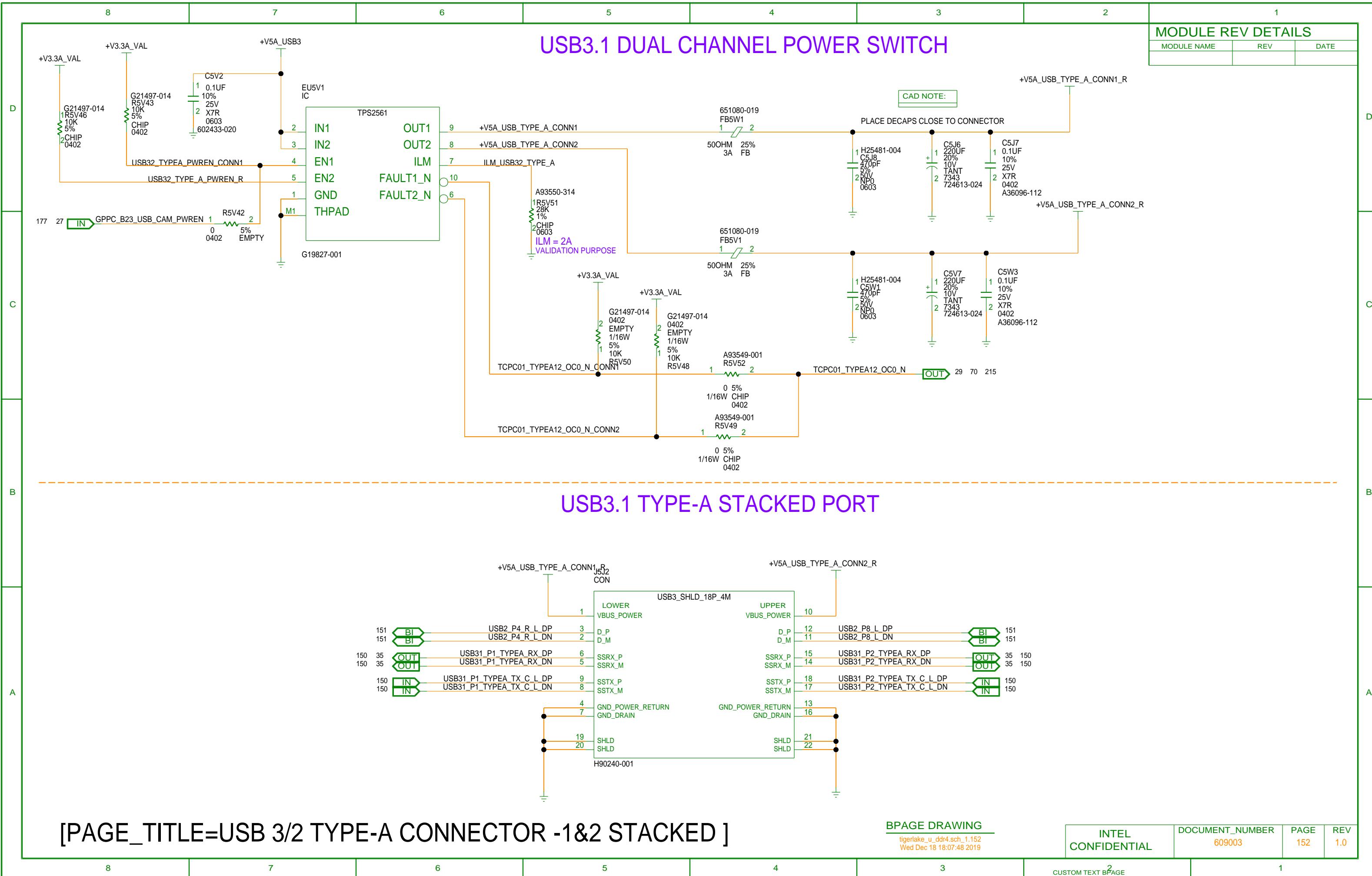


|                           |   |   |   |   |   |   |   |
|---------------------------|---|---|---|---|---|---|---|
| 8                         | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |   |   |   |   |   |   |

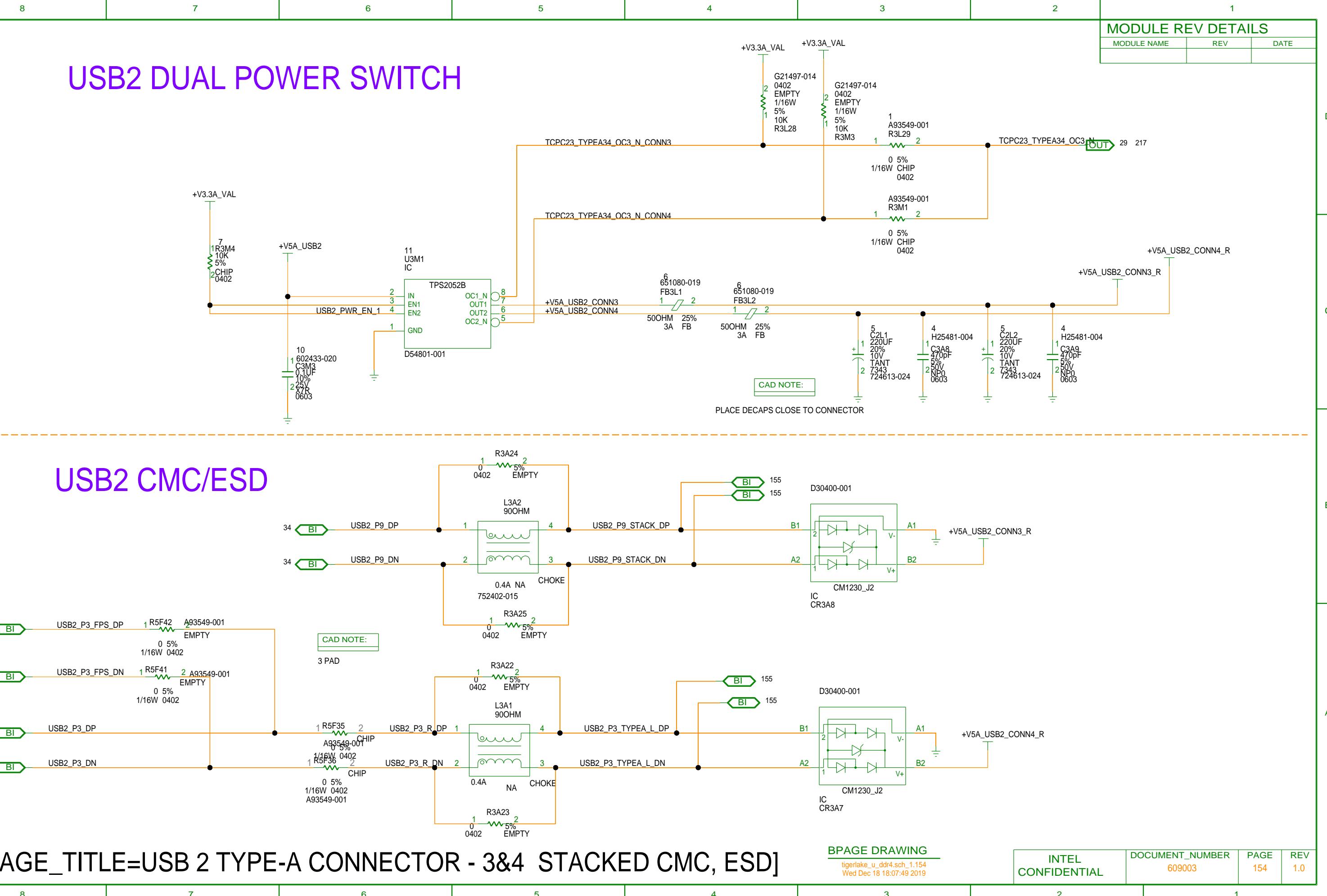
# USB3.1 CMC/ESD

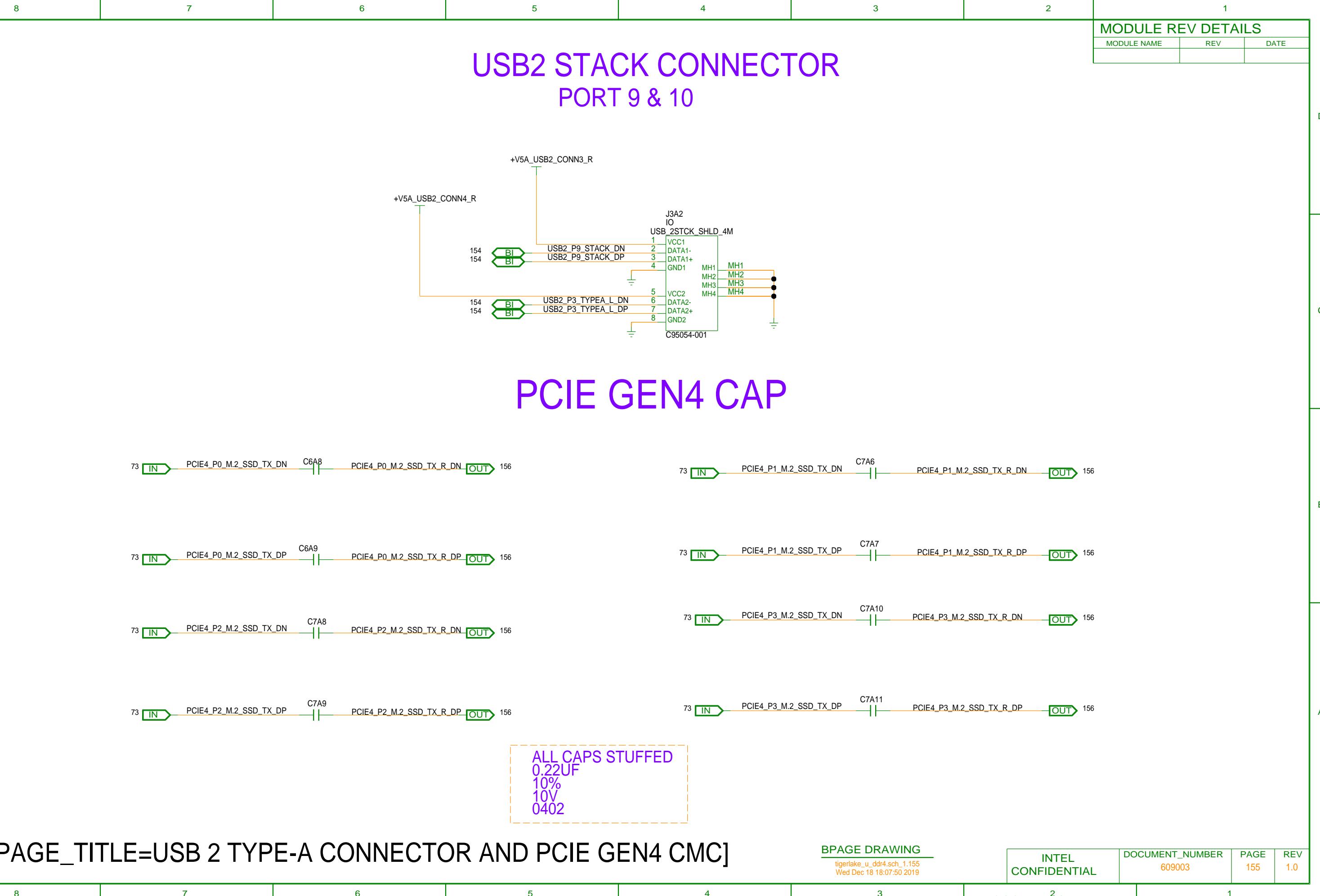






| 8   | 7   | 6    | 5 | 4  | 3 | 2                                 | 1           |     |      |  |  |  |  |
|---|-----|------|---|--|---|-----------------------------------|-------------|-----|------|--|--|--|--|
| <b>MODULE REV DETAILS</b>   |     |      |   |  |   |                                   |             |     |      |  |  |  |  |
| <table border="1"> <thead> <tr> <th>MODULE NAME</th><th>REV</th><th>DATE</th></tr> </thead> <tbody> <tr> <td></td><td></td><td></td></tr> </tbody> </table> |     |      |   |  |   |                                   | MODULE NAME | REV | DATE |  |  |  |  |
| MODULE NAME   | REV | DATE |   |  |   |                                   |             |     |      |  |  |  |  |
|   |     |      |   |  |   |                                   |             |     |      |  |  |  |  |
|   |     |      |   |  |   |                                   |             |     |      |  |  |  |  |
|   |     |      |   |  |   |                                   |             |     |      |  |  |  |  |
| D   |     |      |   |  |   |                                   | D           |     |      |  |  |  |  |
| C   |     |      |   |  |   |                                   | C           |     |      |  |  |  |  |
| B   |     |      |   |  |   |                                   | B           |     |      |  |  |  |  |
| A   |     |      |   |  |   |                                   | A           |     |      |  |  |  |  |
| <p>[PAGE_TITLE=RESERVE]</p>   |     |      |   | <u>BPAGE DRAWING</u><br><small>tigerlake_u_ddr4.sch_1.153<br/>Tue Oct 15 12:50:51 2019</small> |   |                                   |             |     |      |  |  |  |  |
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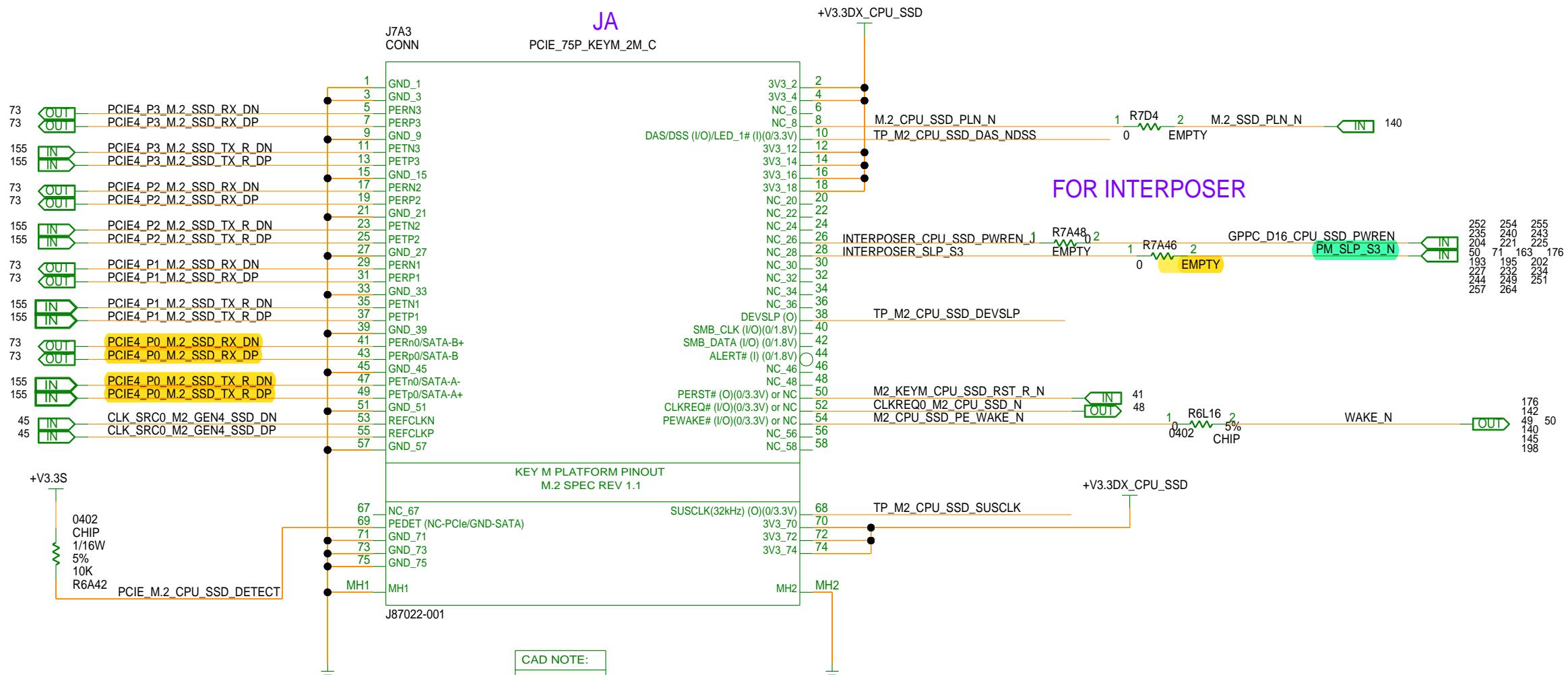


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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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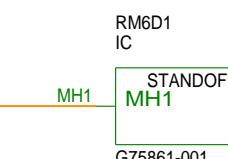
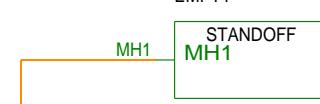
# PCIE GEN4 SSD

**MODULE REV DETAILS**

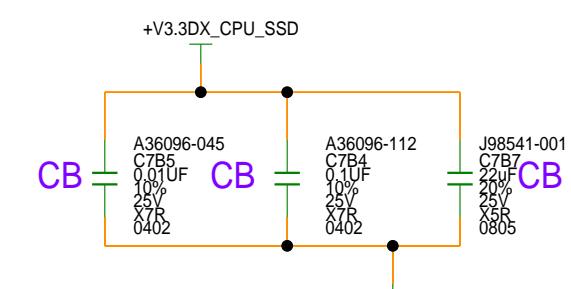
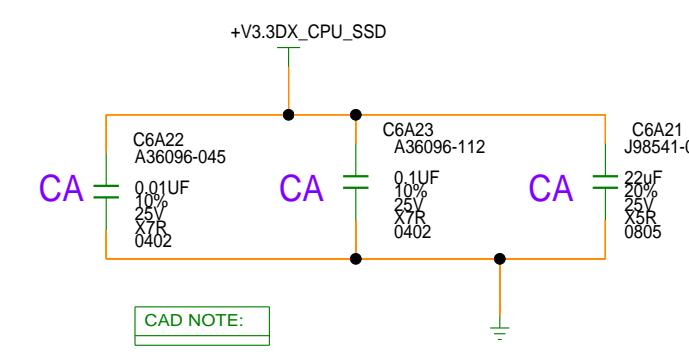
| MODULE NAME | REV | DATE |
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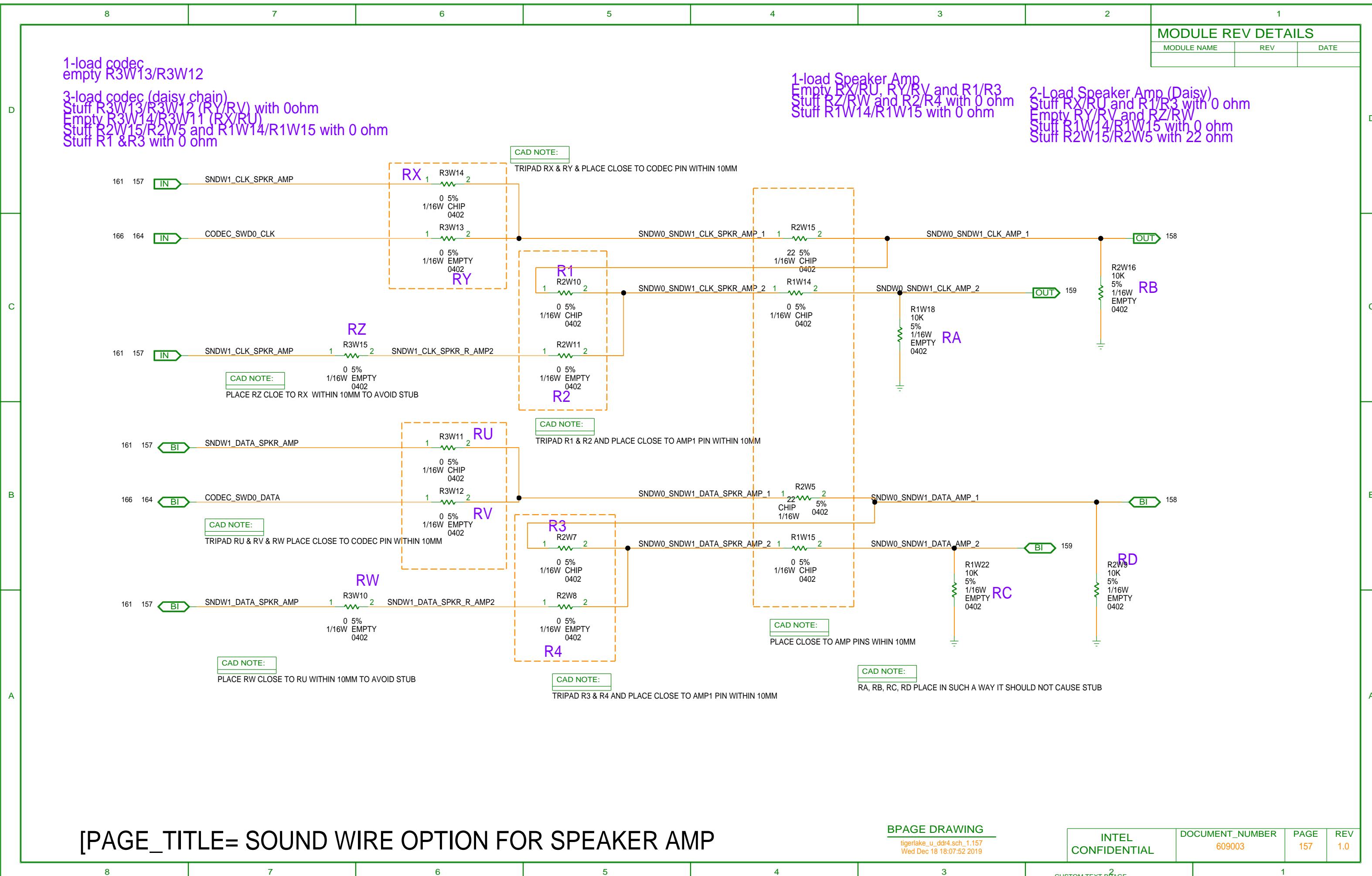


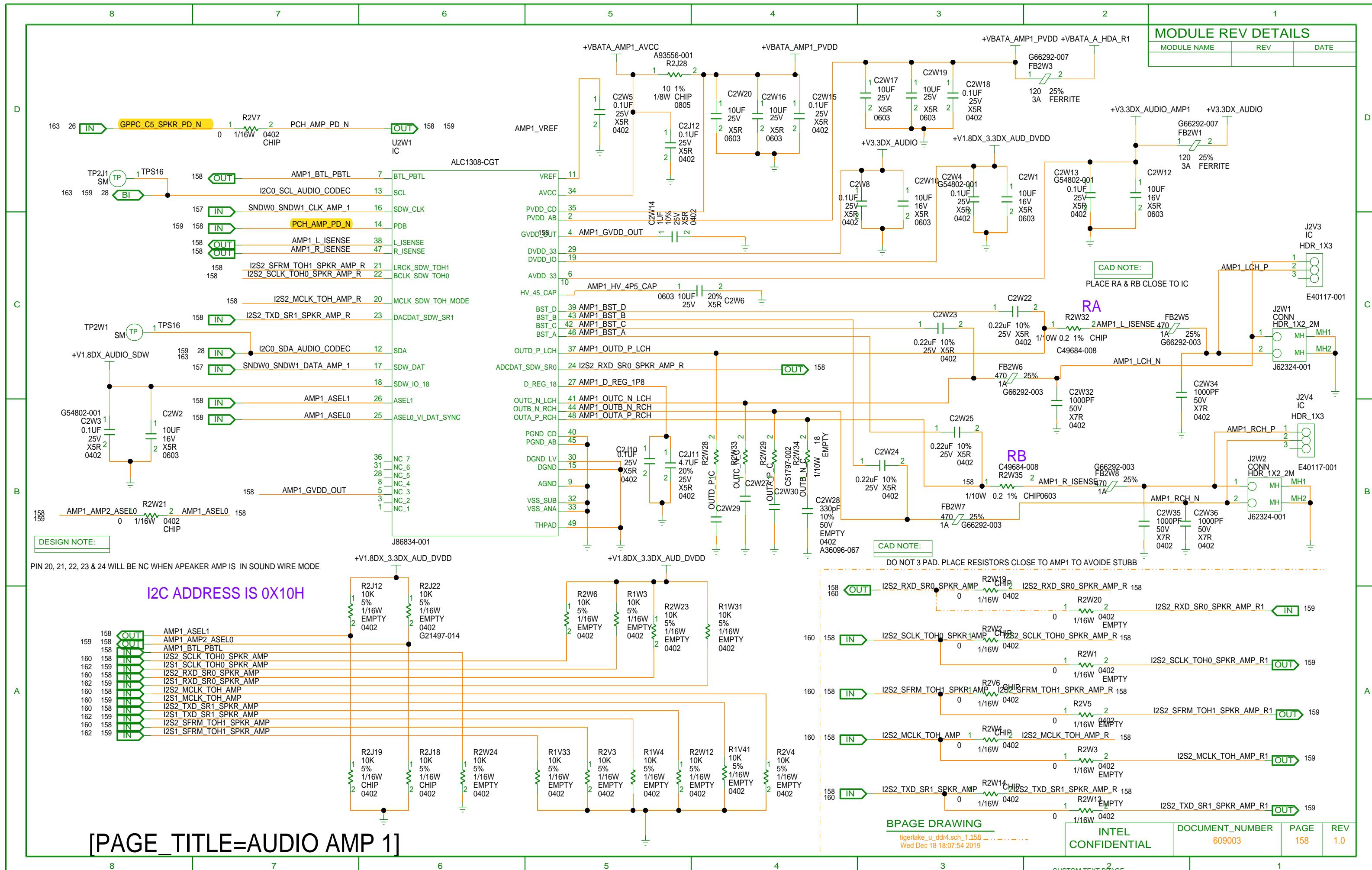
KEEP STANOFF AT 2242 MODULE DIMENSION  
RM6N1  
EMPTY

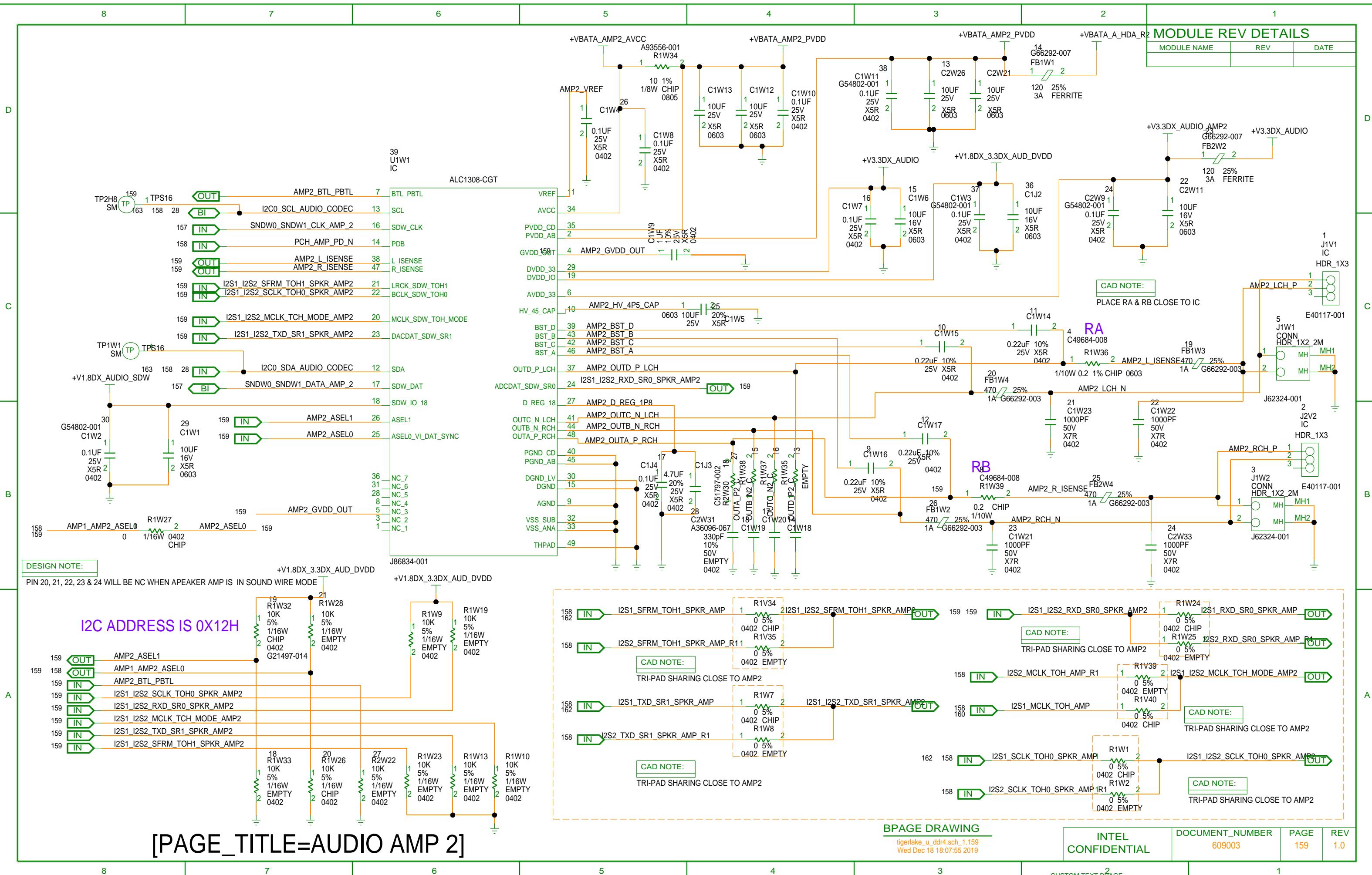


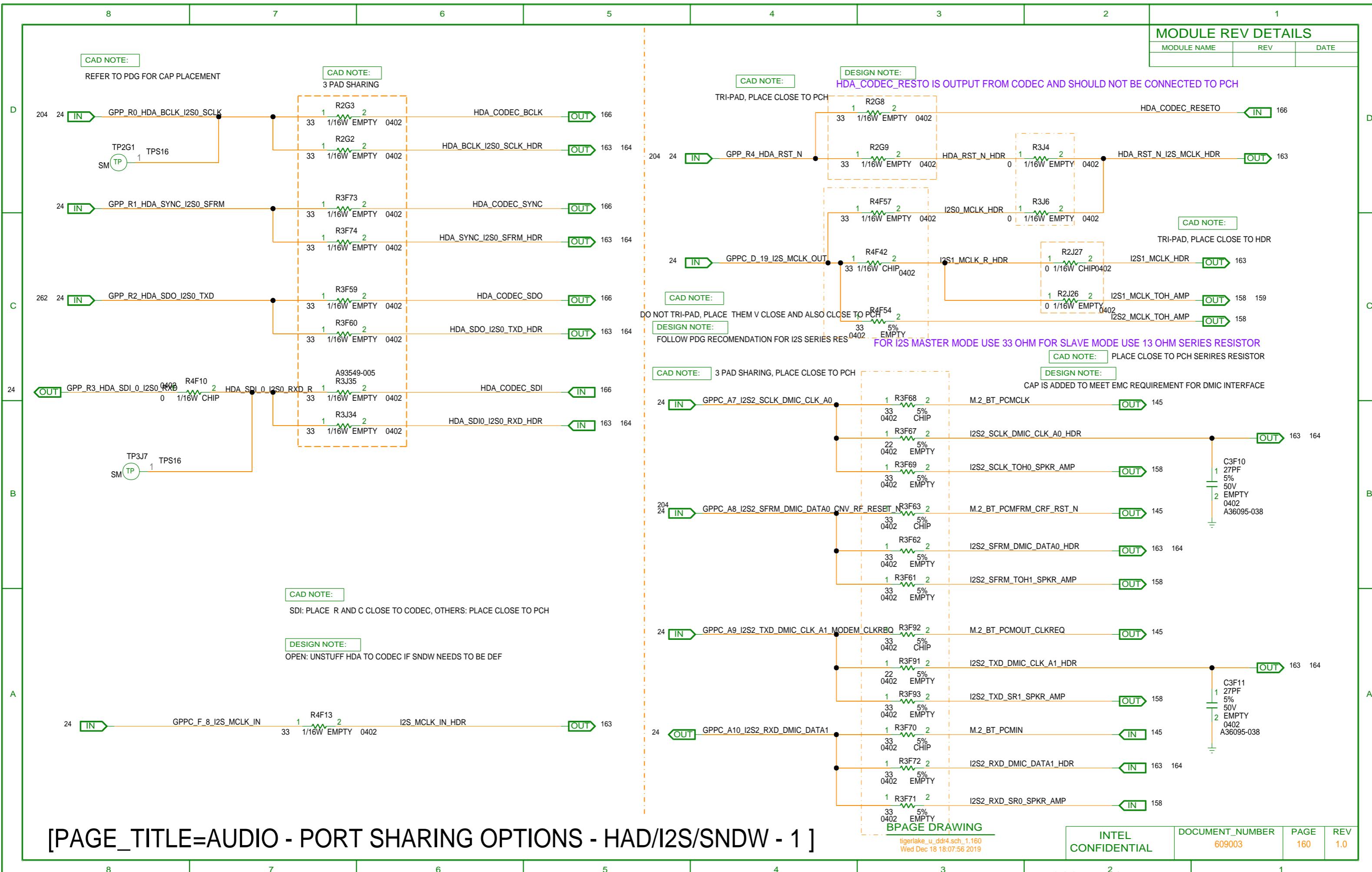
KEEP K0Z AS 2280 FOR M.2 KEY-M CONNECTOR

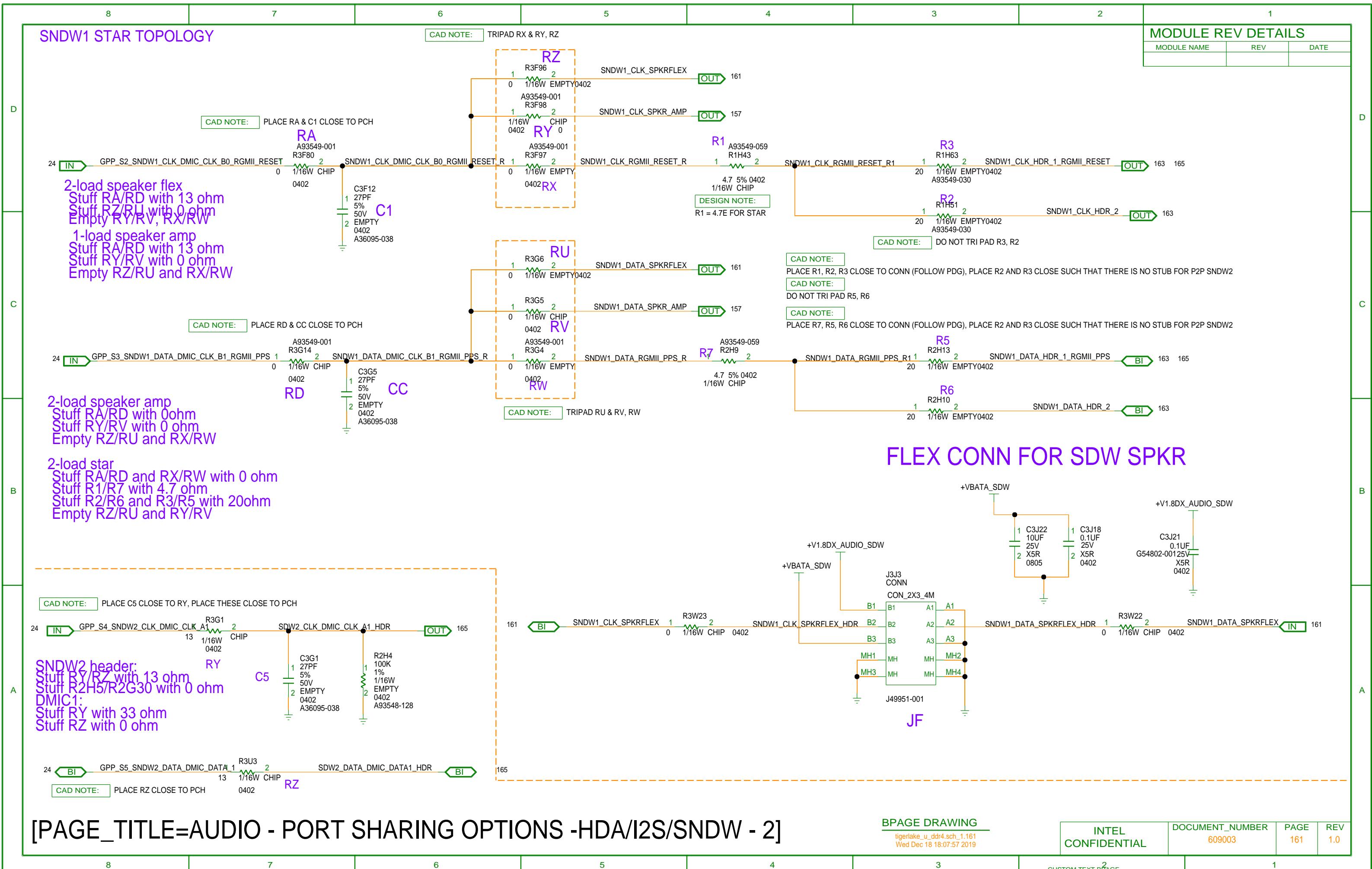


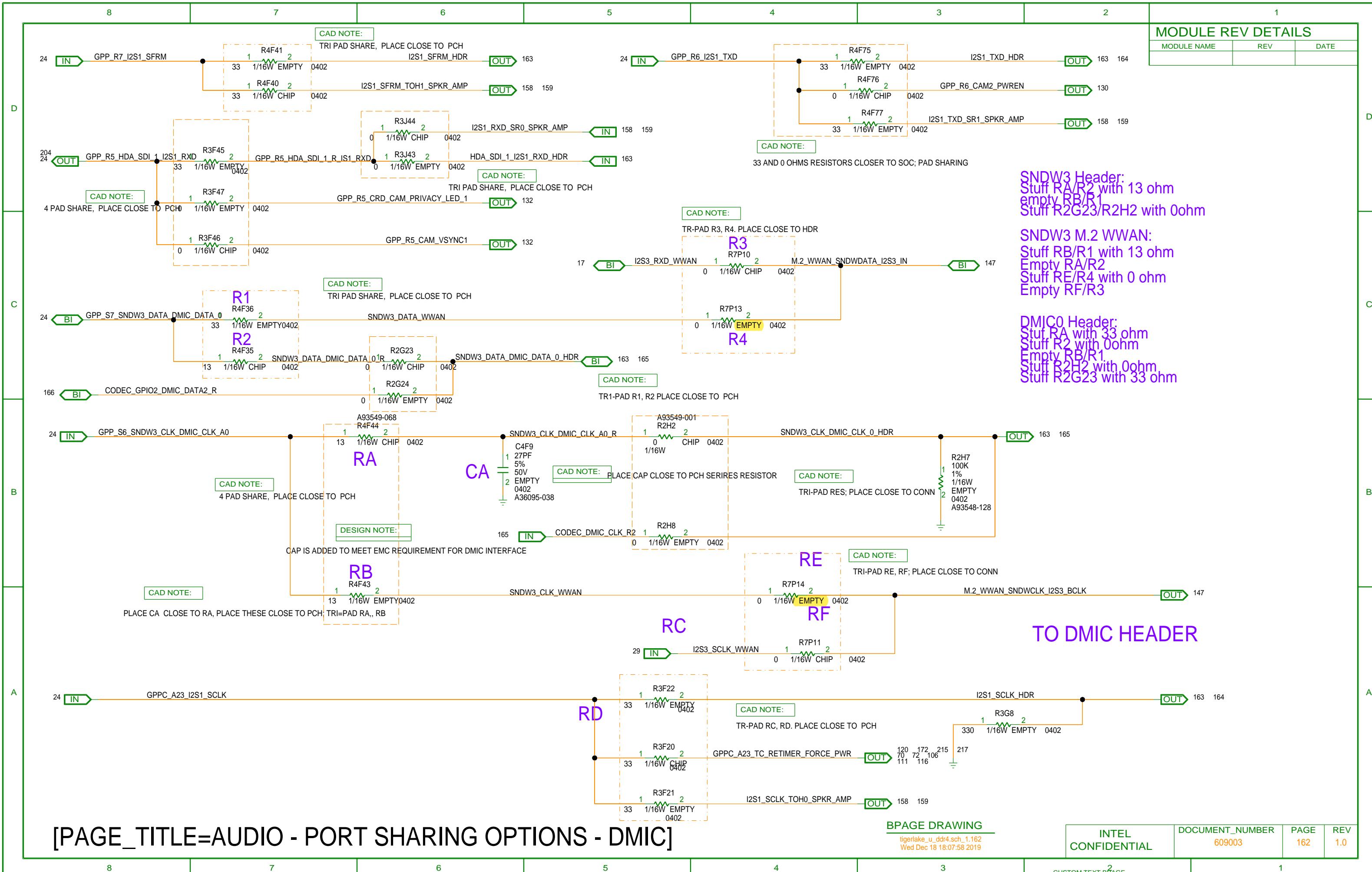


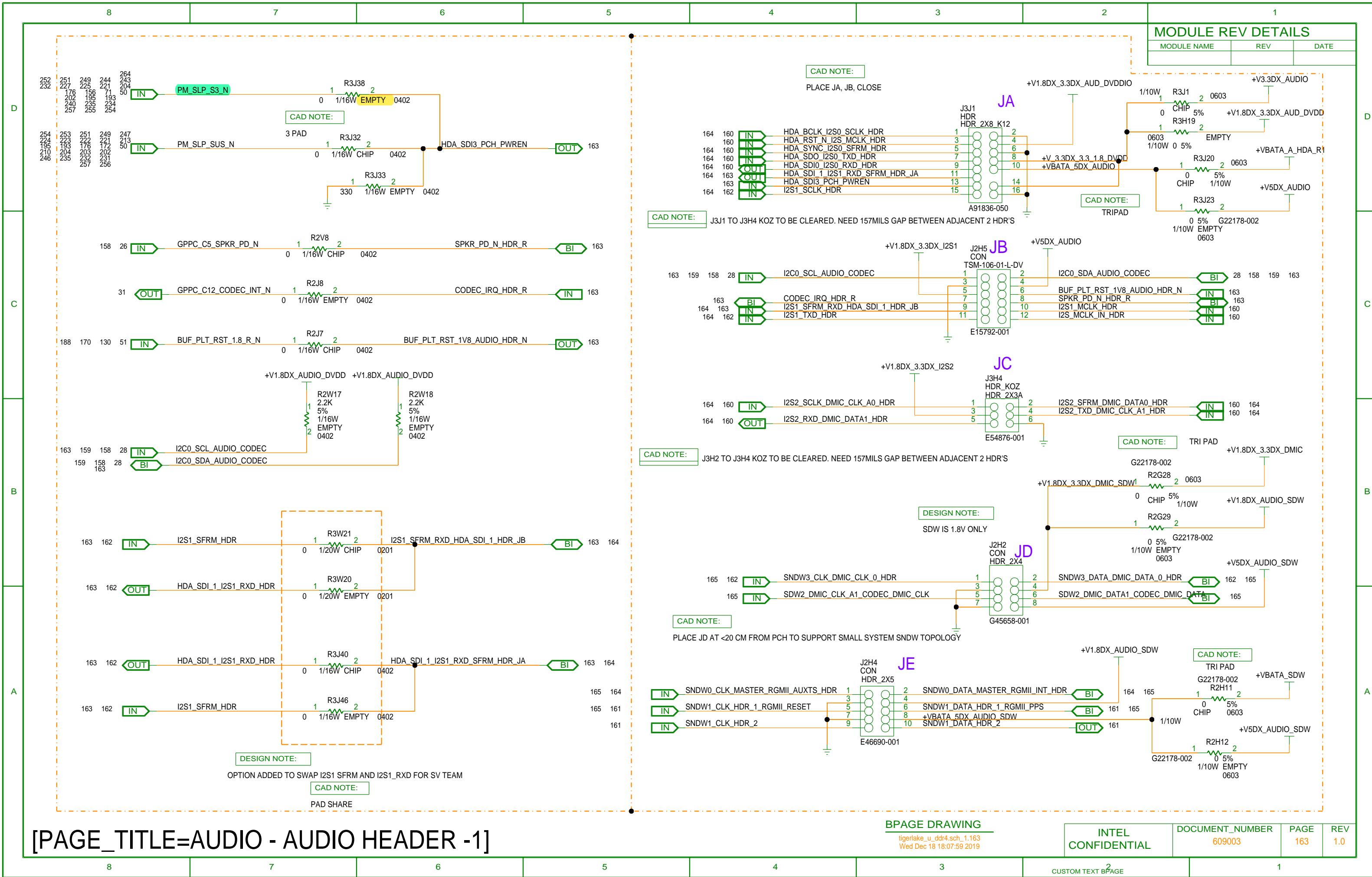








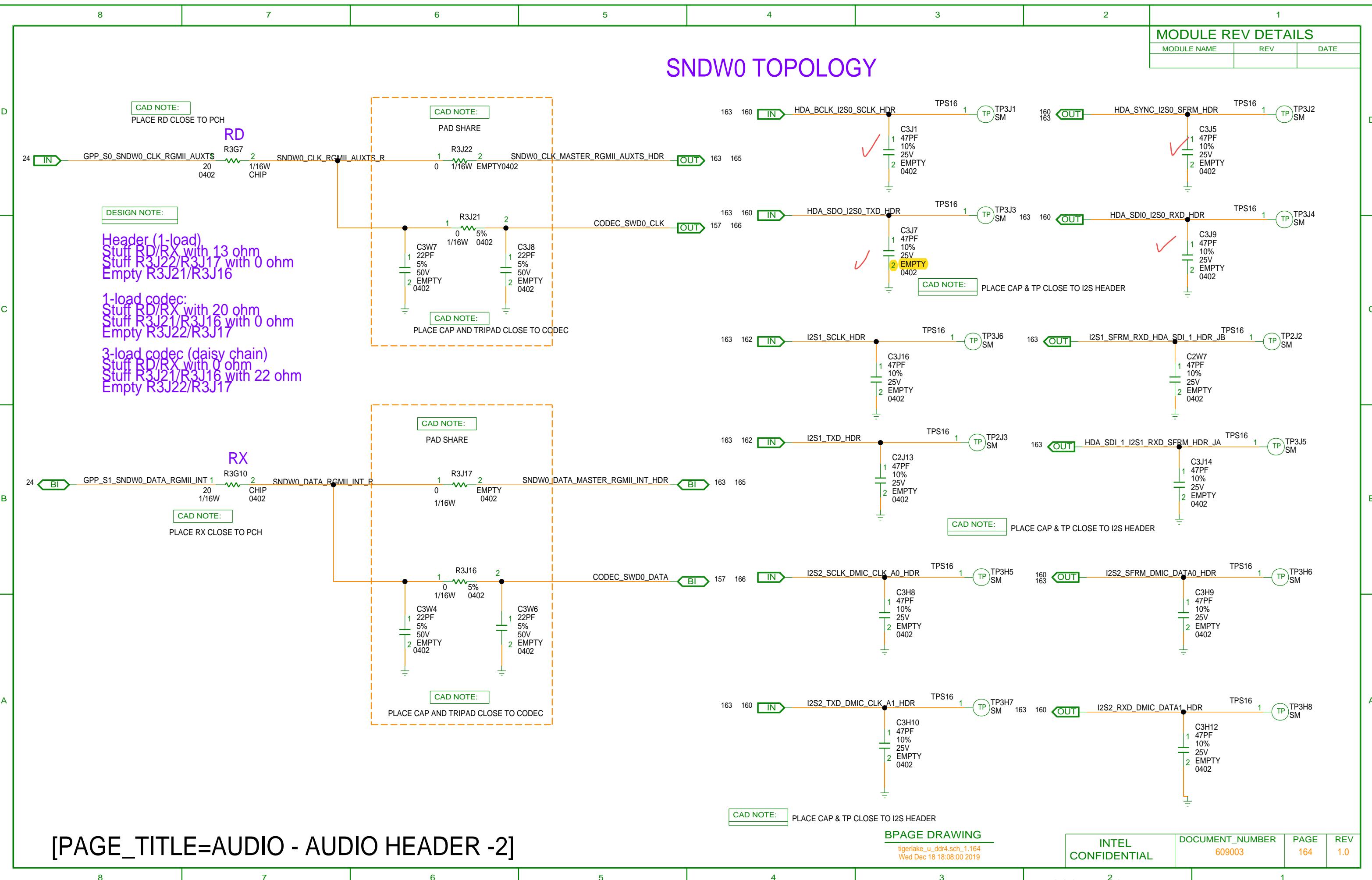


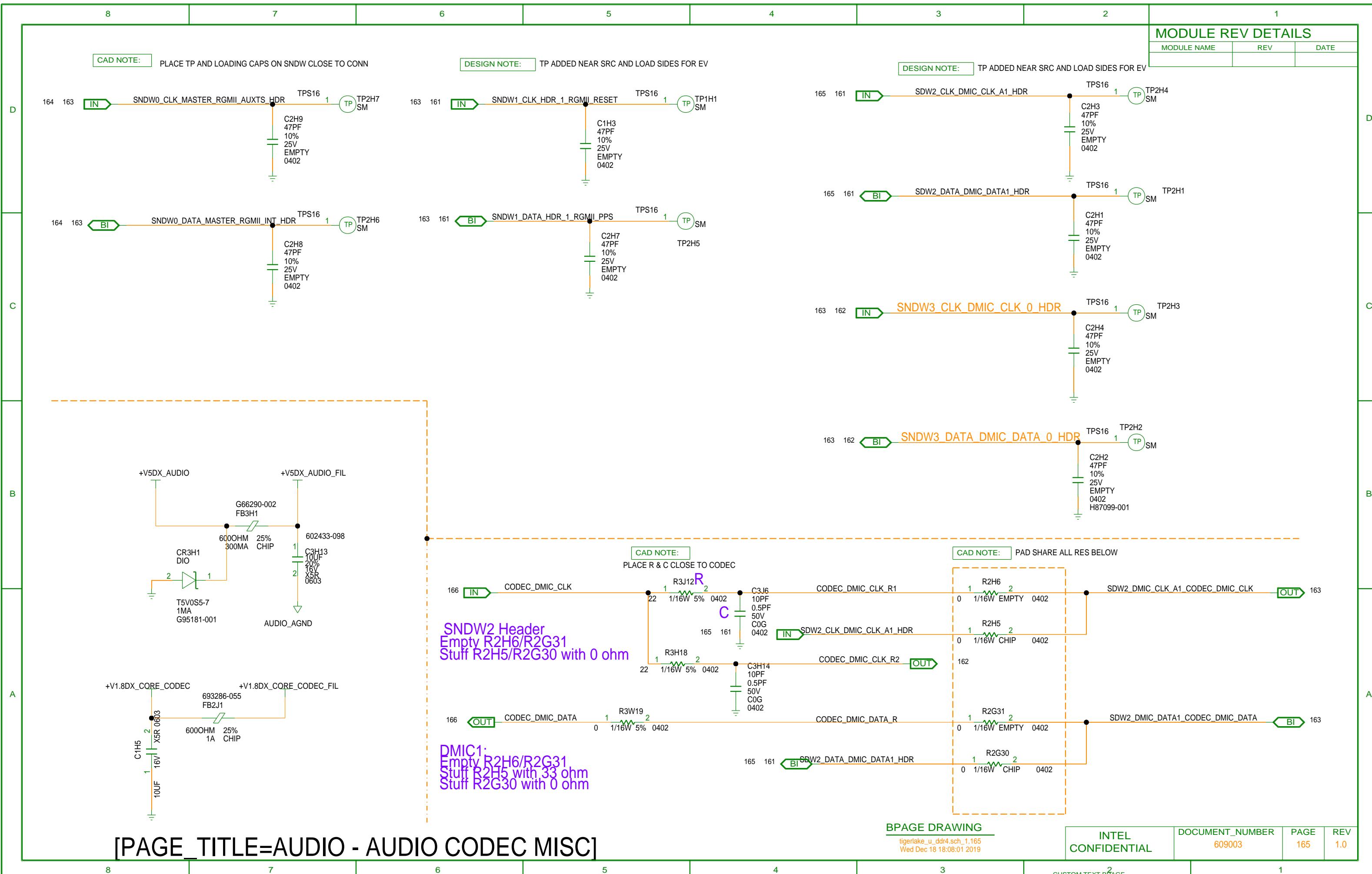


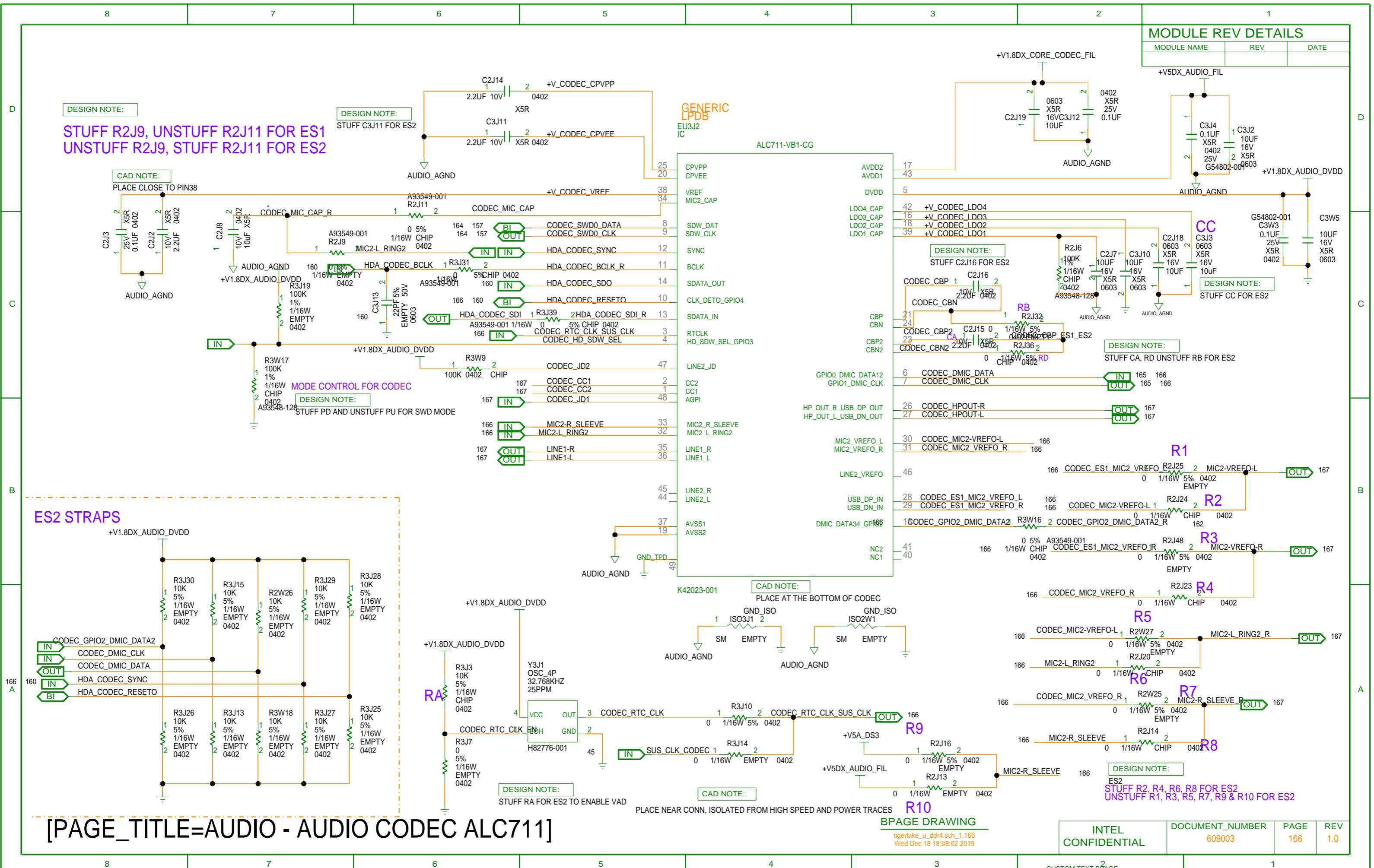
# SNDW0 TOPOLOGY

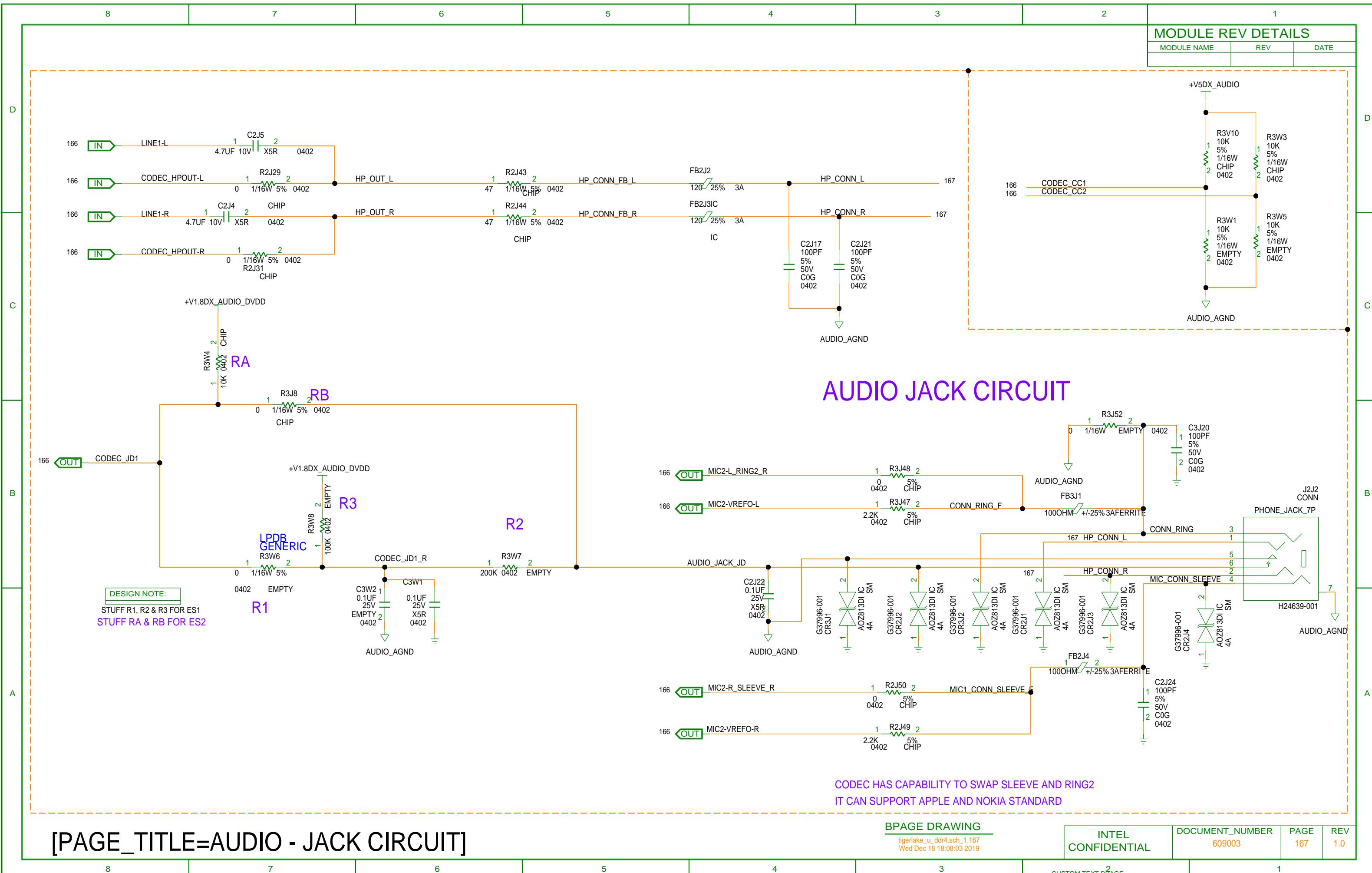
## MODULE REV DETAILS

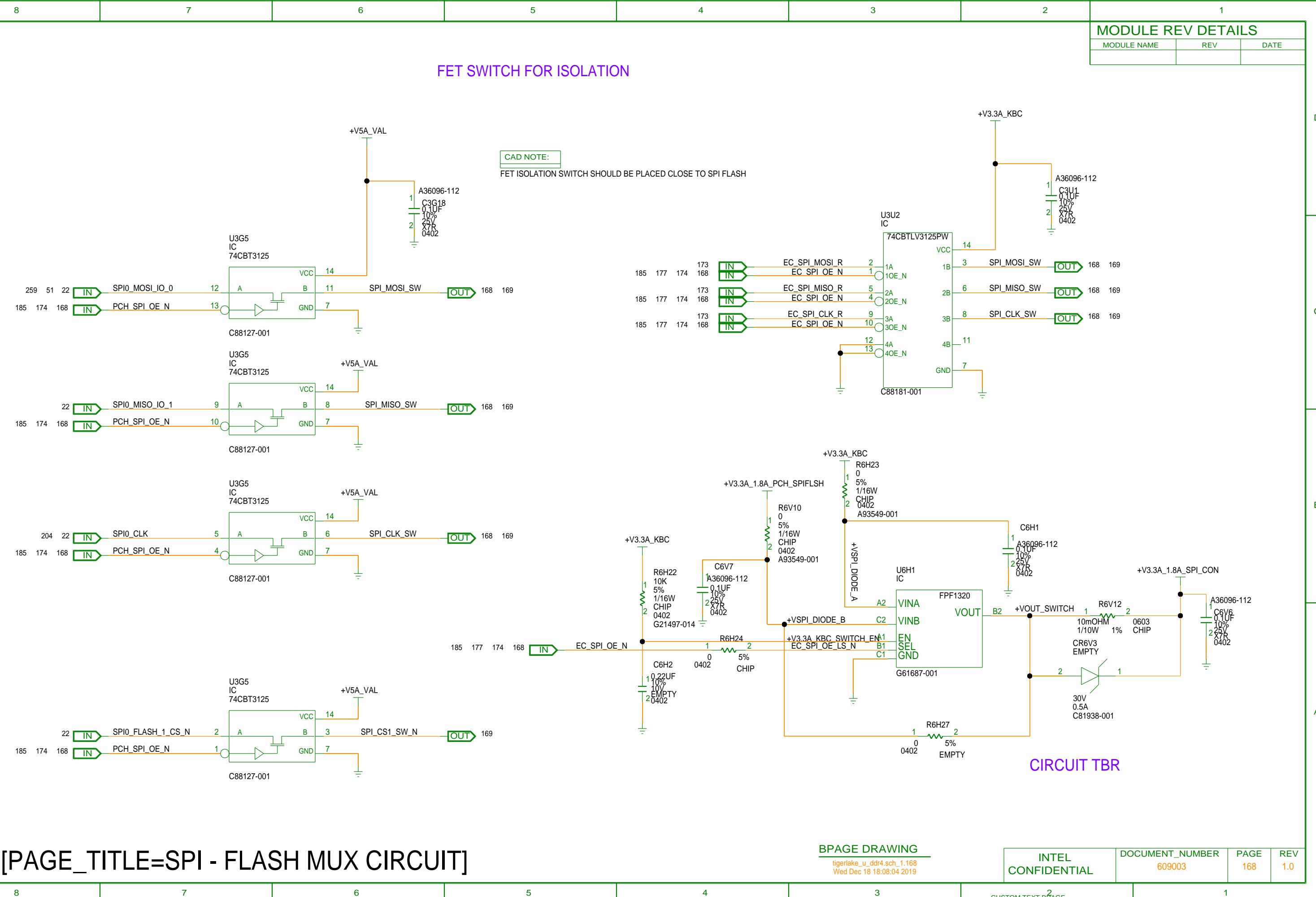
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|-------------|-----|------|
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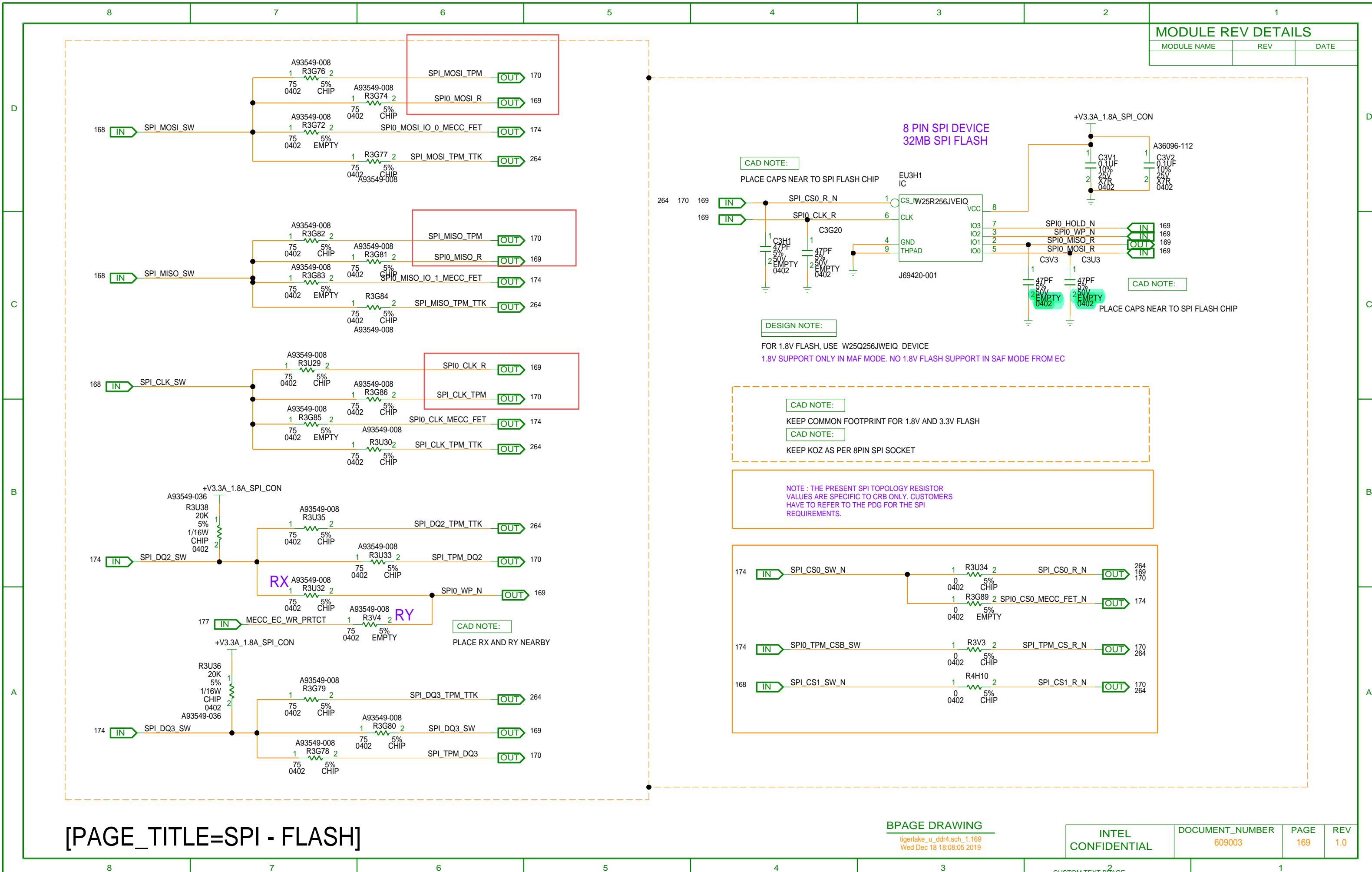










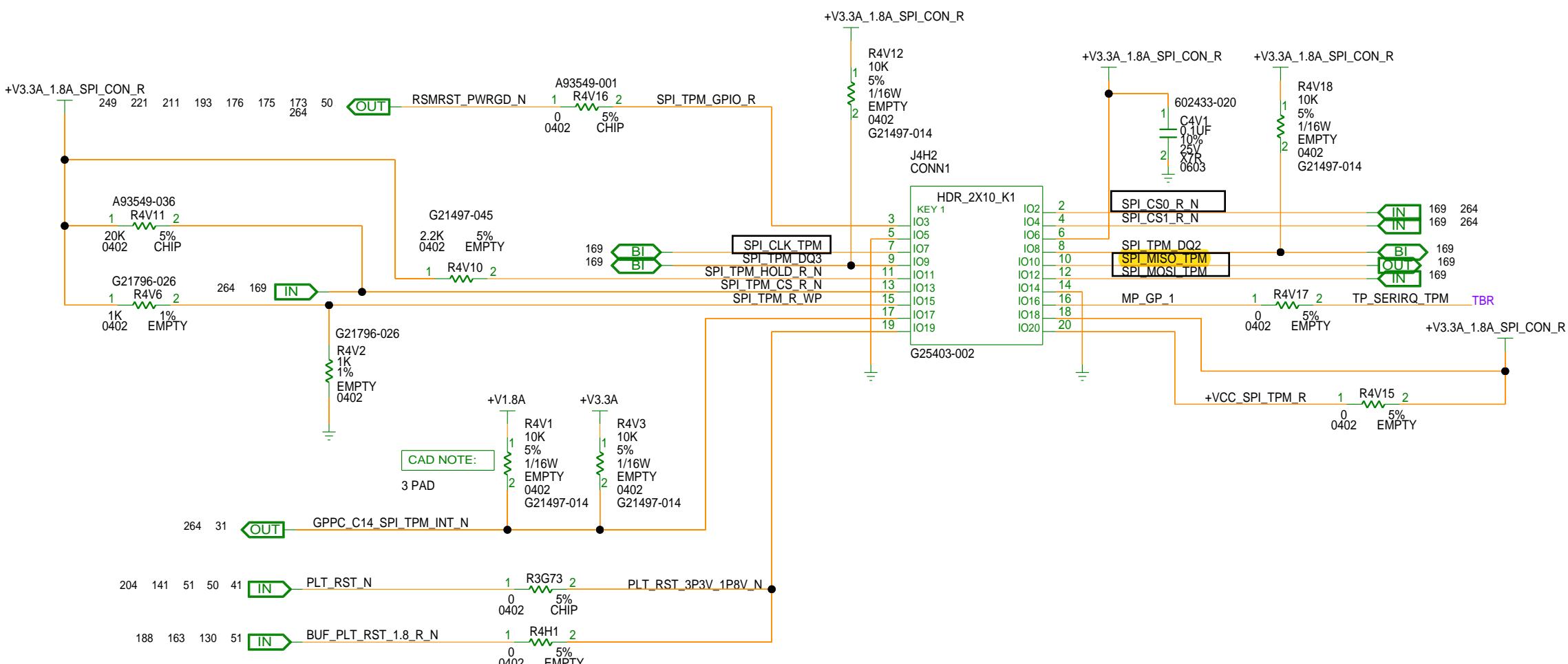


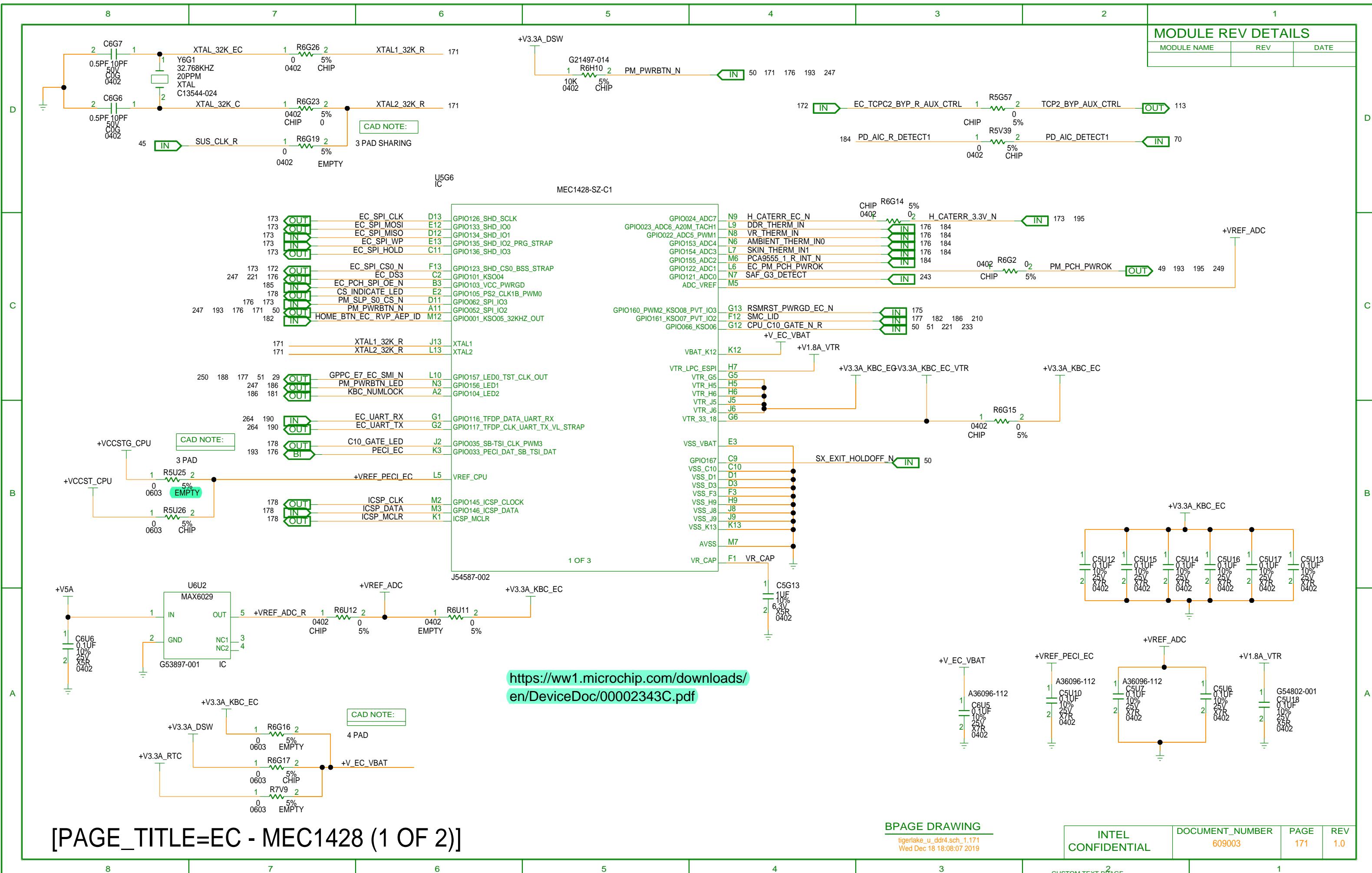
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|---------------------------|---|---|---|---|---|-----|------|
| 8                         | 7 | 6 | 5 | 4 | 3 | 2   | 1    |
| <b>MODULE REV DETAILS</b> |   |   |   |   |   |     |      |
| MODULE NAME               |   |   |   |   |   | REV | DATE |

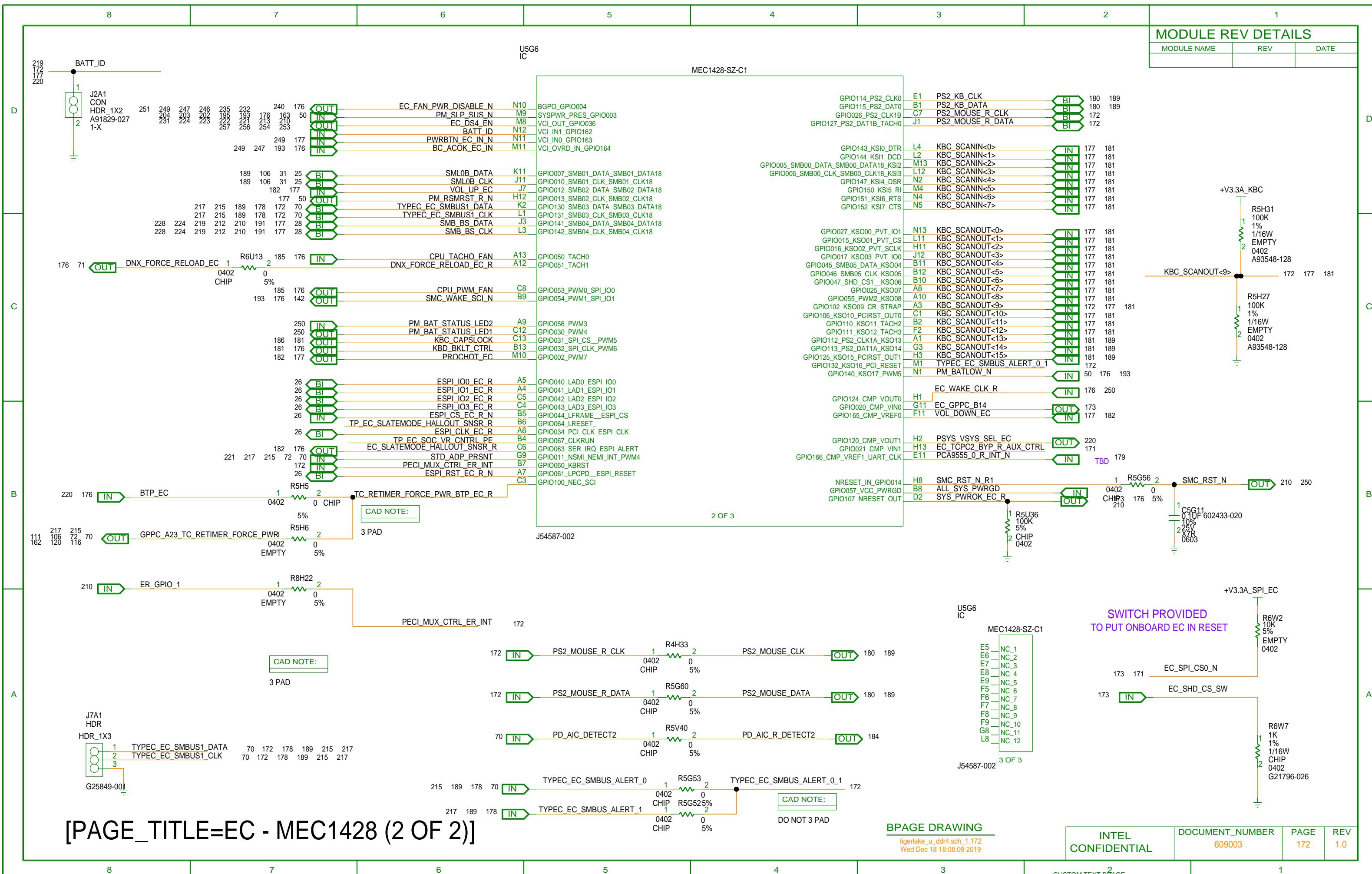
# SF600 BASED SPI BASED TPM HEADER

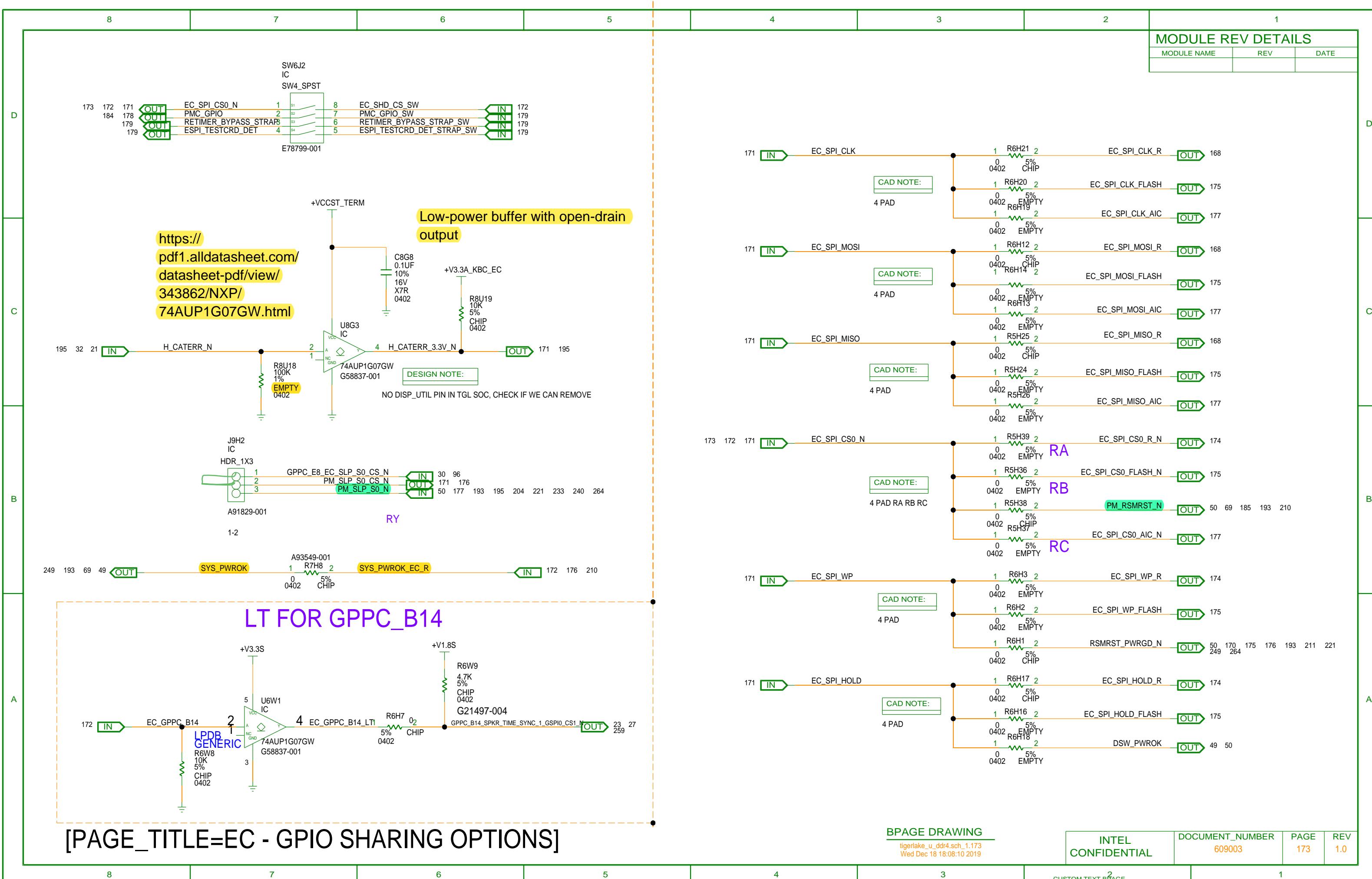
CAD NOTE:

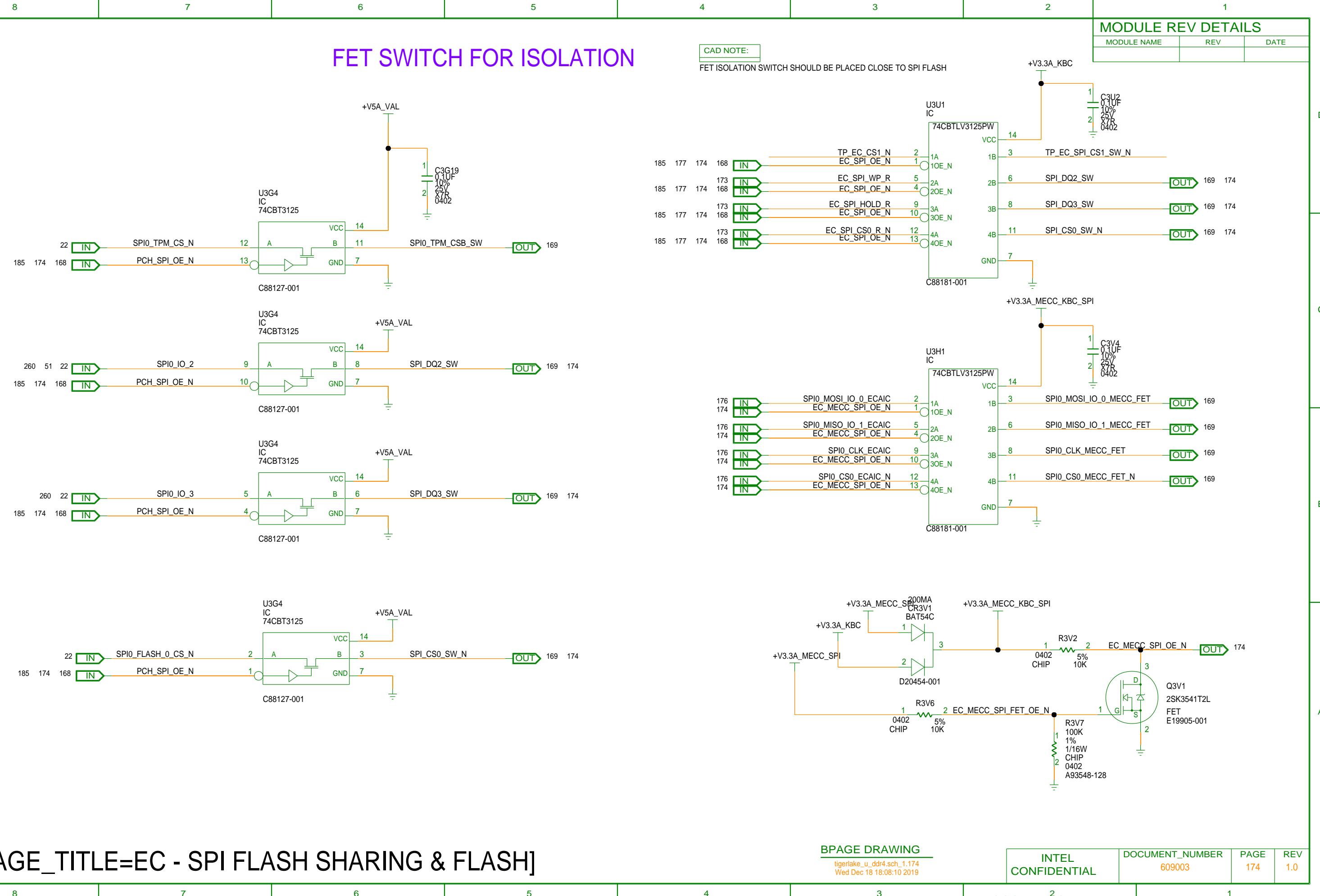
SPI0\_FLASH\_1\_CS\_N SIGNAL TO BE ROUTED 1.5 INCH MORE LENGTH THAN OTHER SPI0 SIGNALS







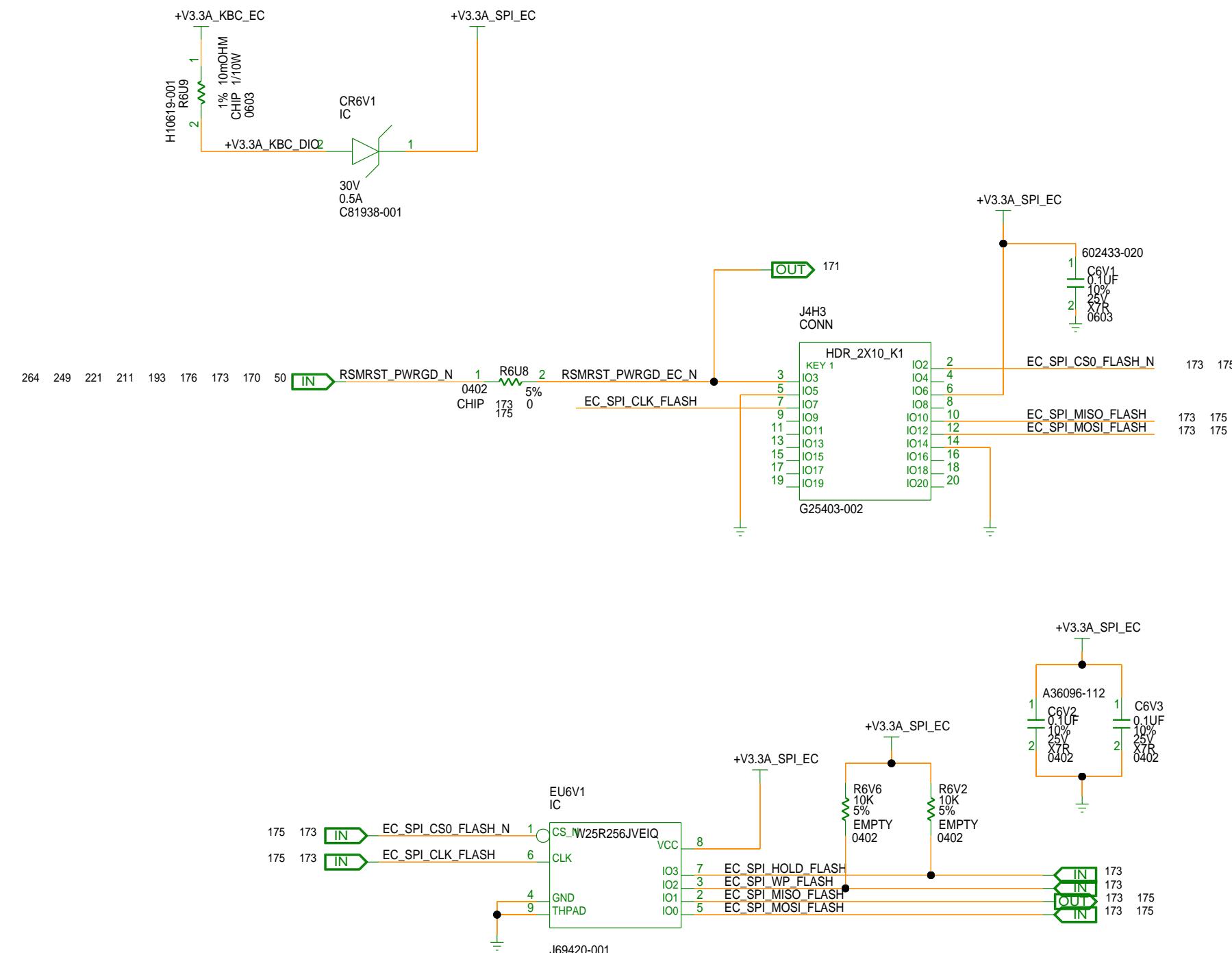




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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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# SF600 BASED TPM HEADER (DEDICATED FOR EC)

| MODULE REV DETAILS |     |      |
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| MODULE NAME        | REV | DATE |
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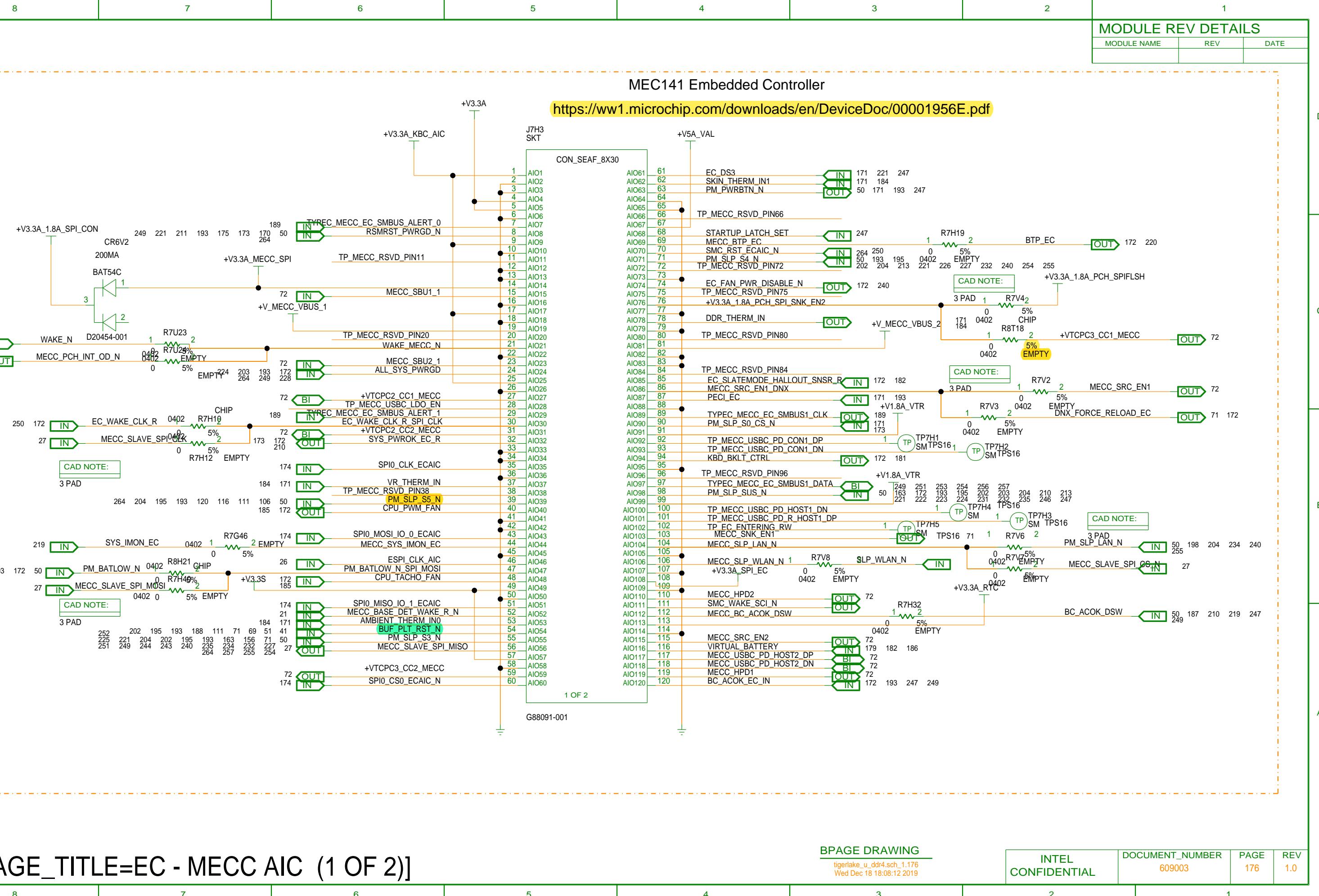


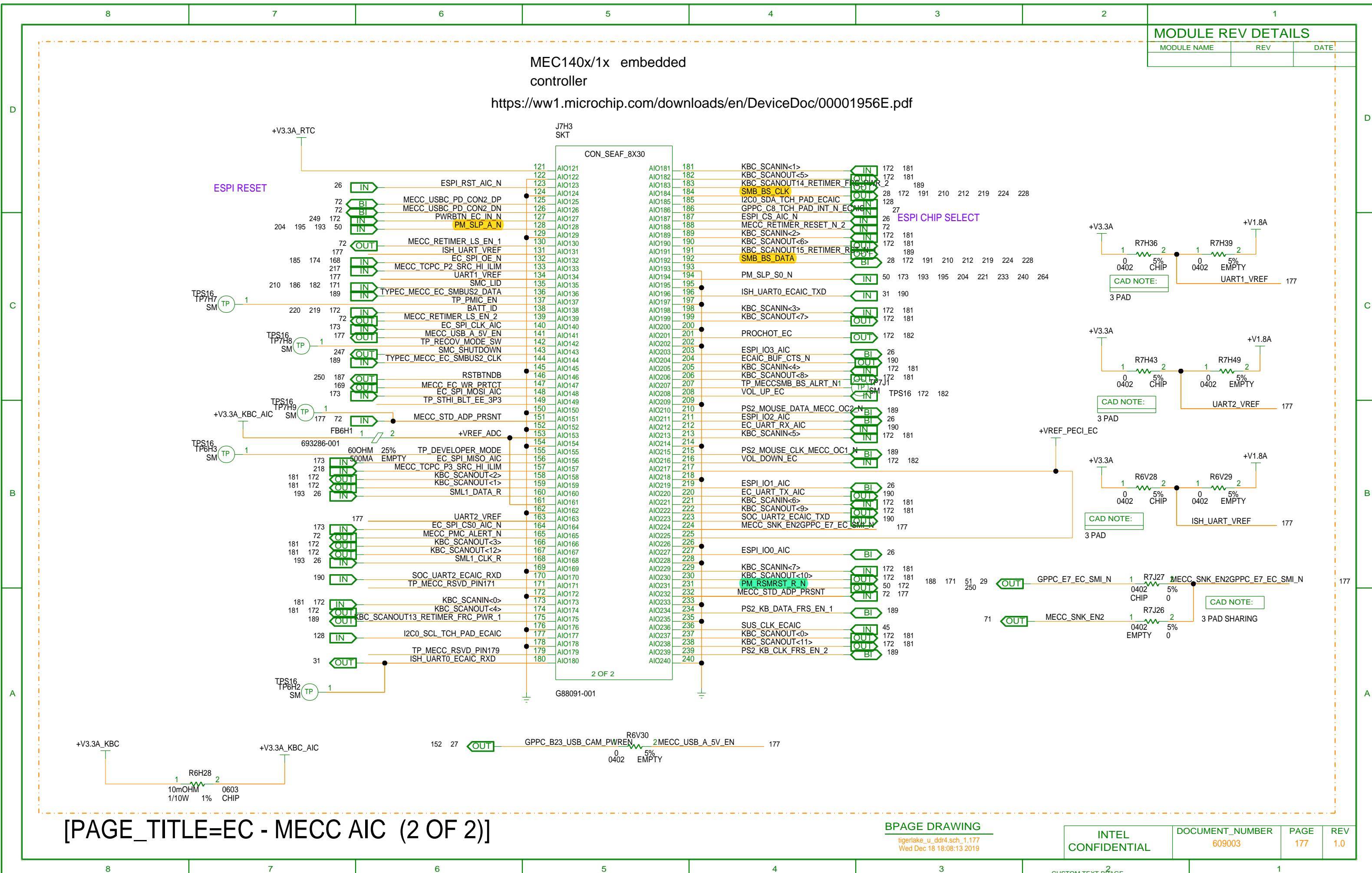
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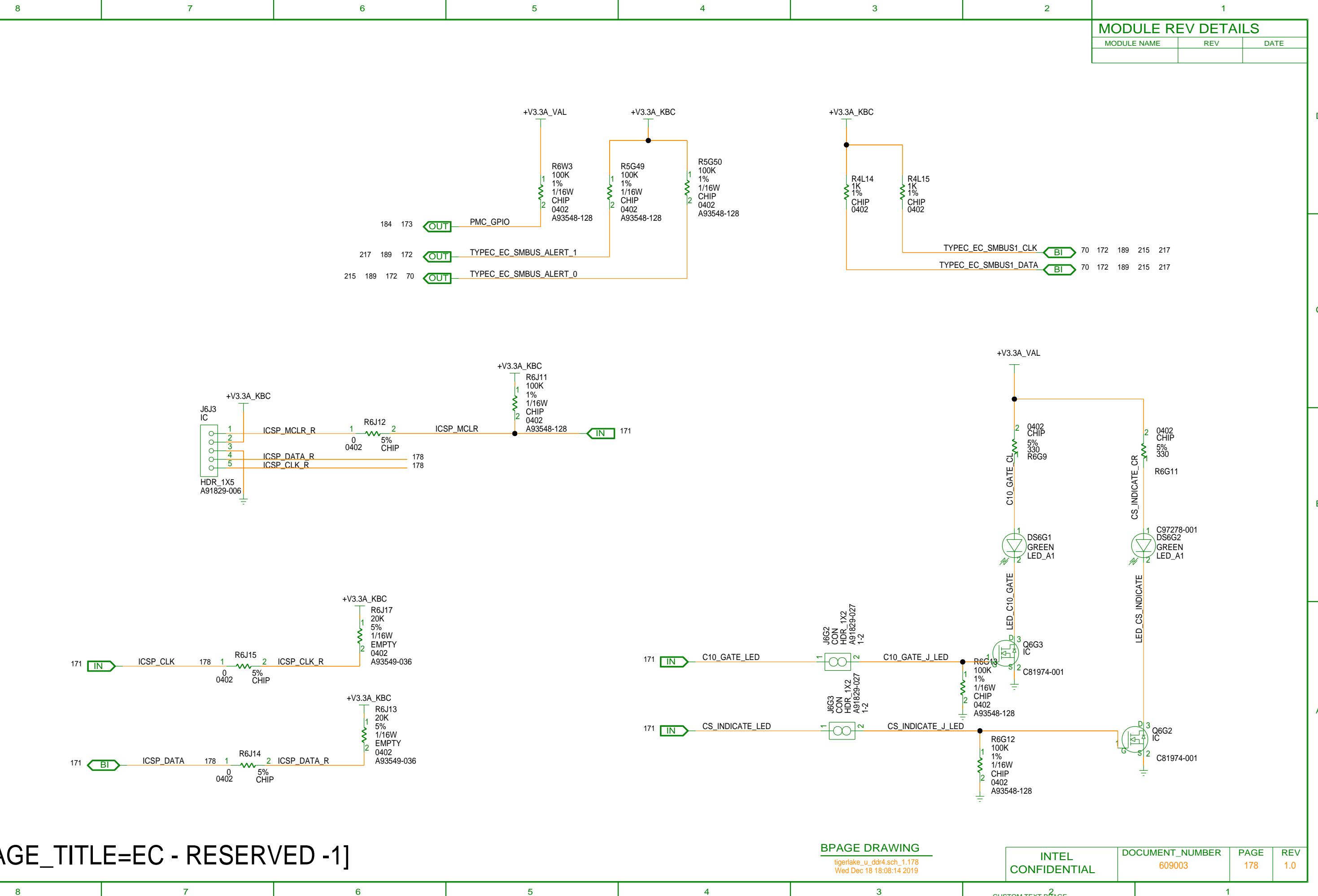
BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.175  
Wed Dec 18 18:08:11 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>175 | REV<br>1.0 |
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| CUSTOM TEXT BPAGE     |                           |             |            |

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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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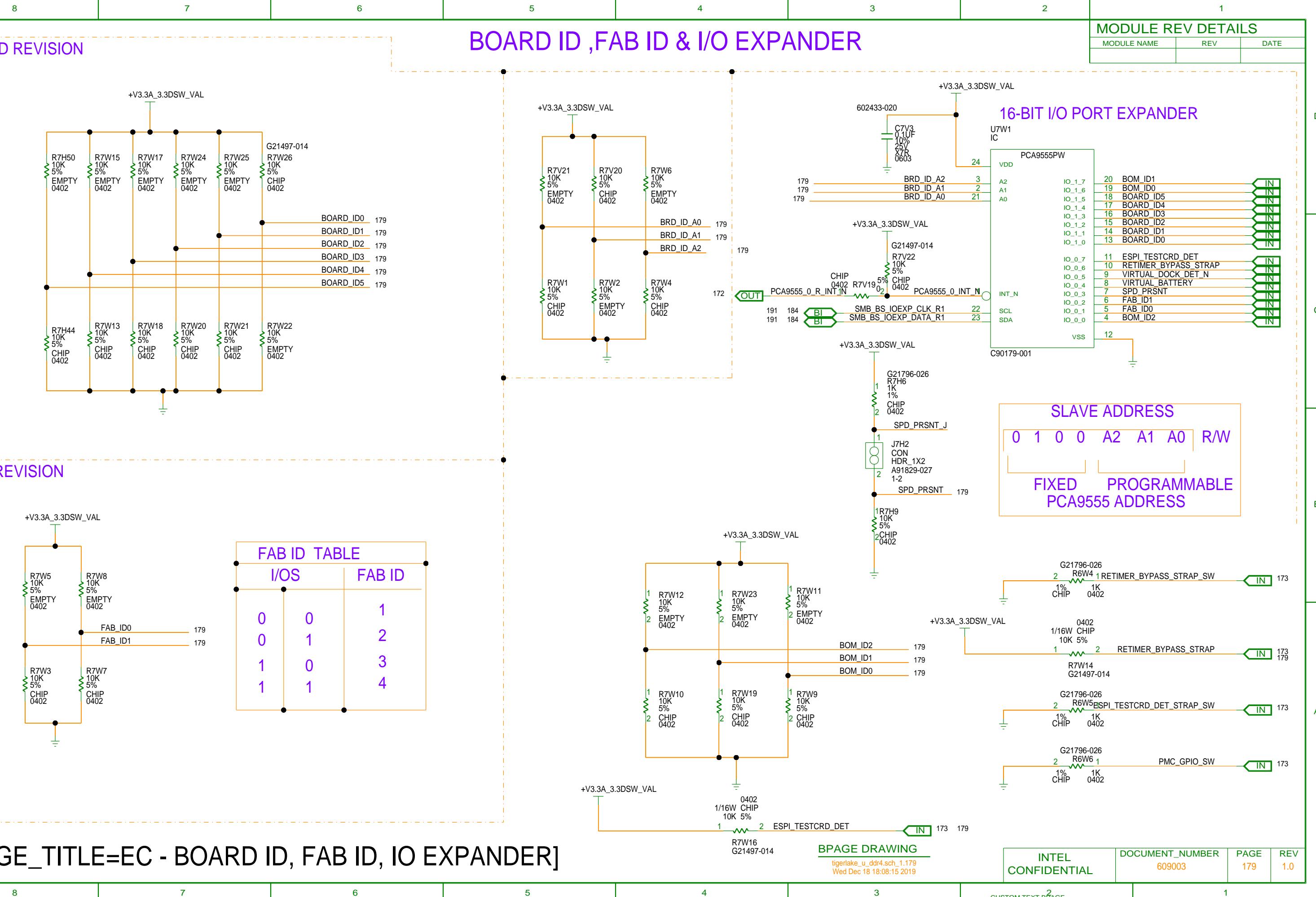


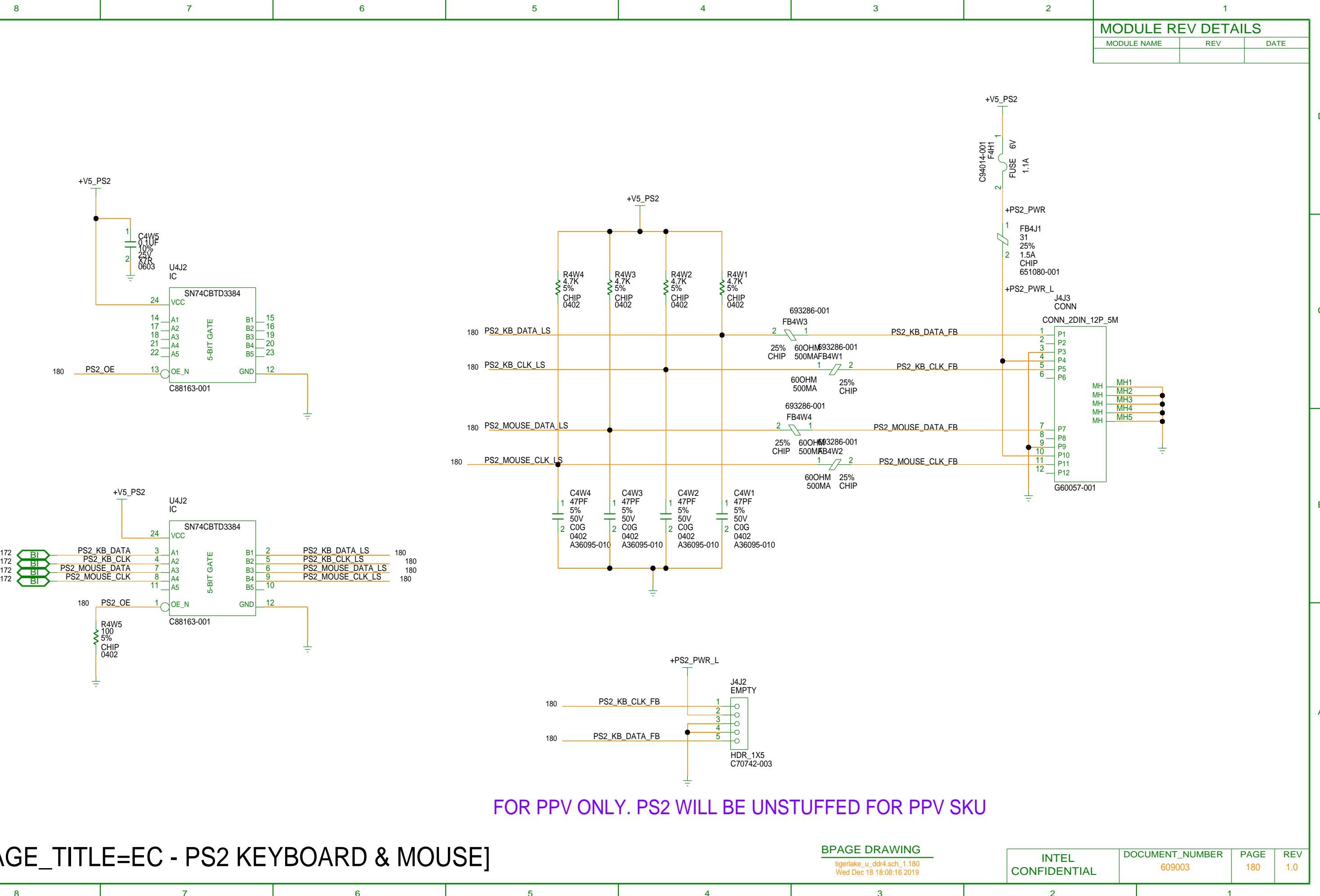


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*tigerlake\_u\_ddr4.sch\_1.178*  
*Wed Dec 18 18:08:14 2019*

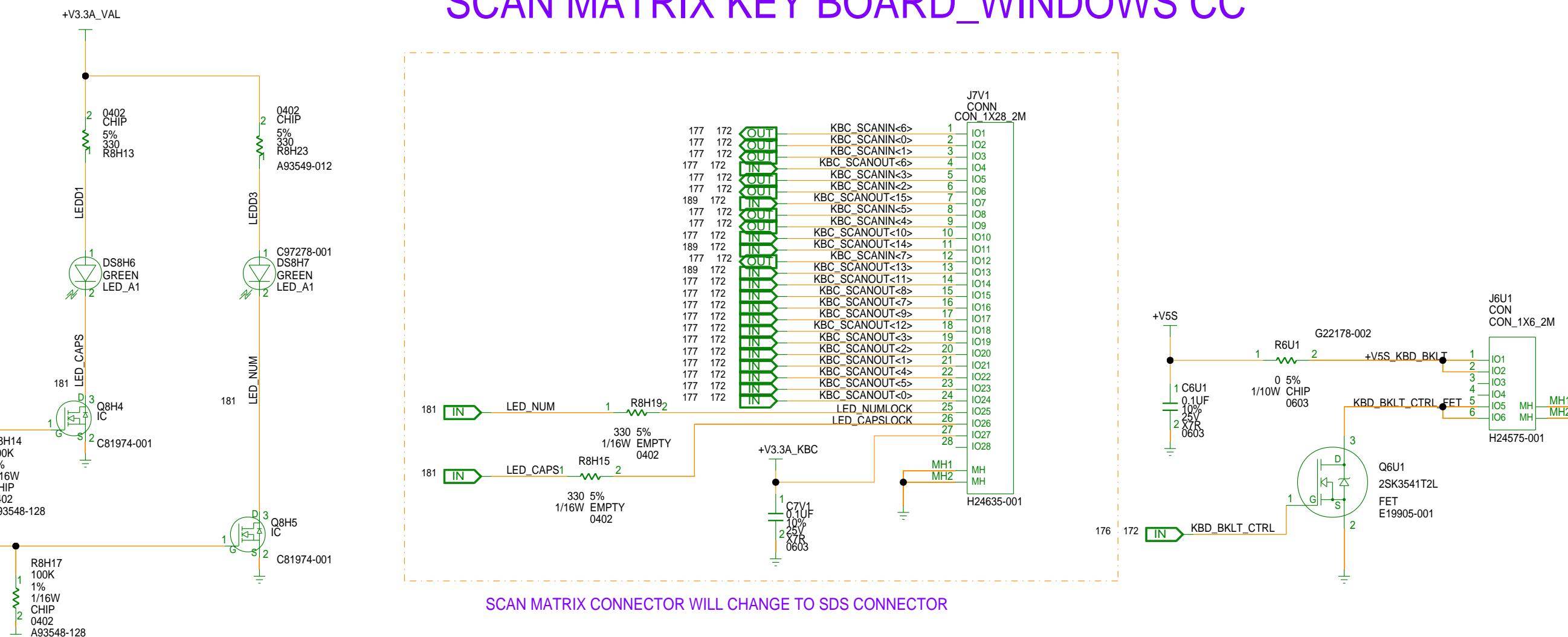
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| CUSTOM TEXT BPAGE     |                           |             |            |





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| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

# SCAN MATRIX KEY BOARD\_WINDOWS CC

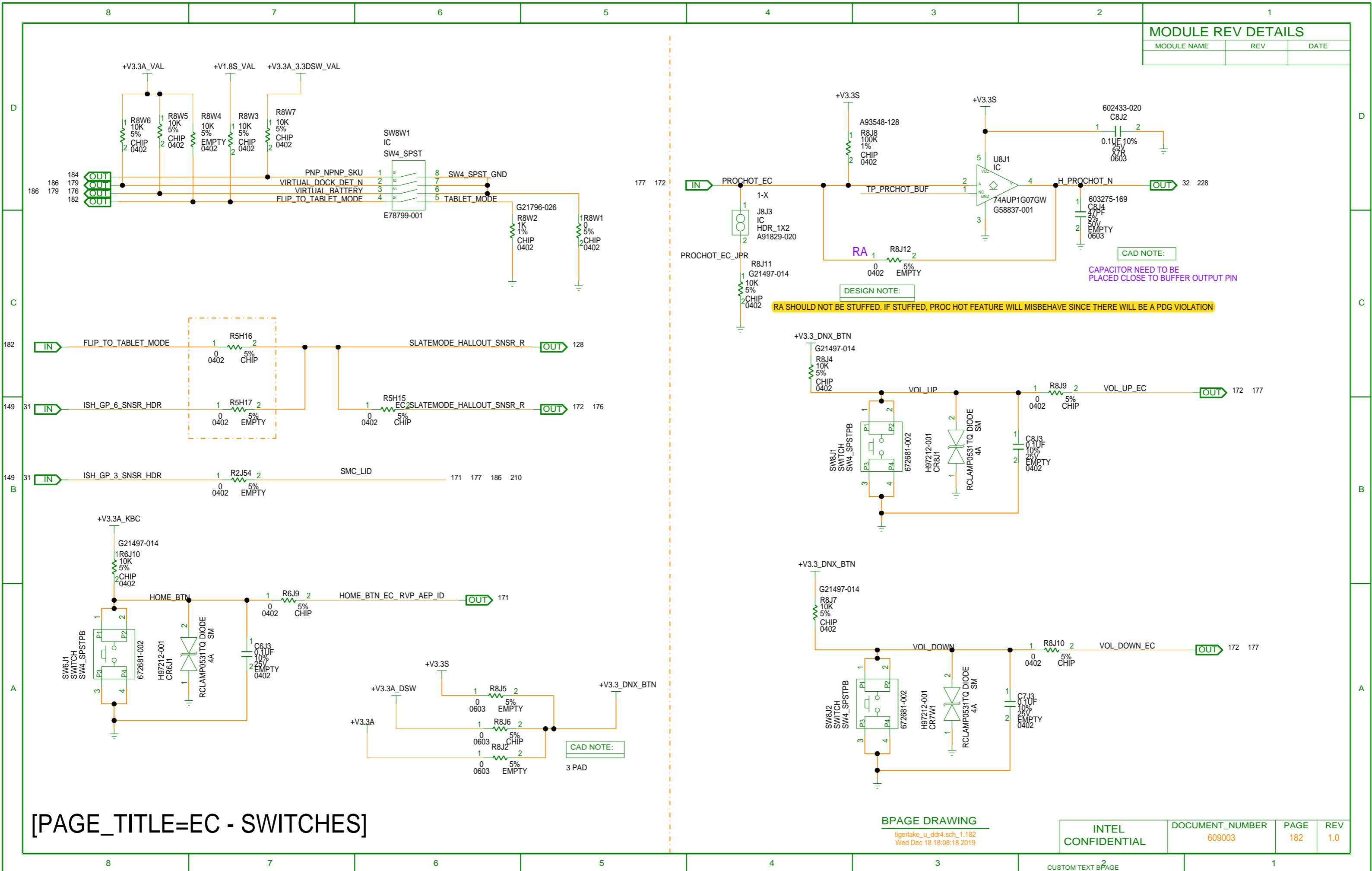


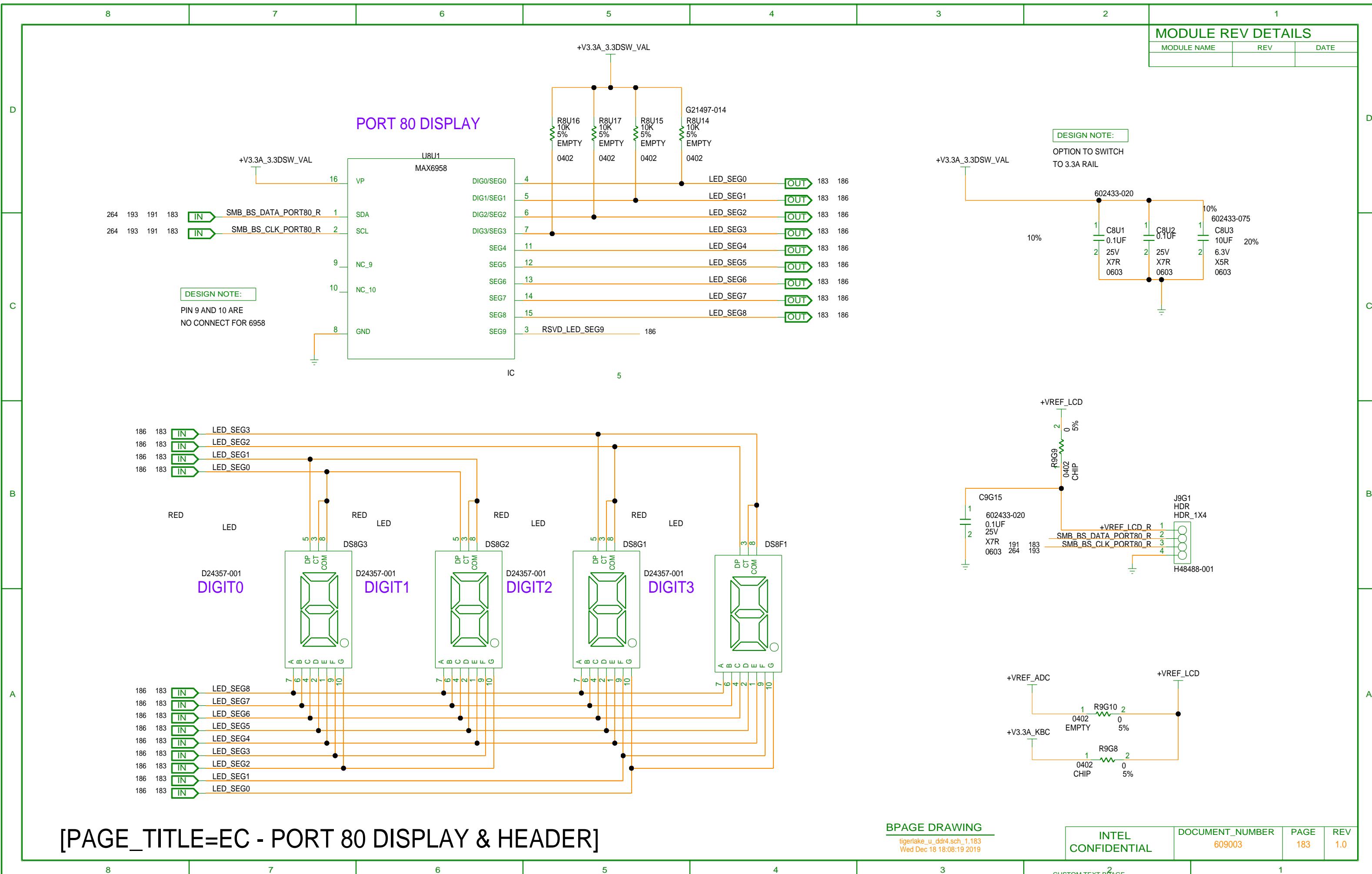
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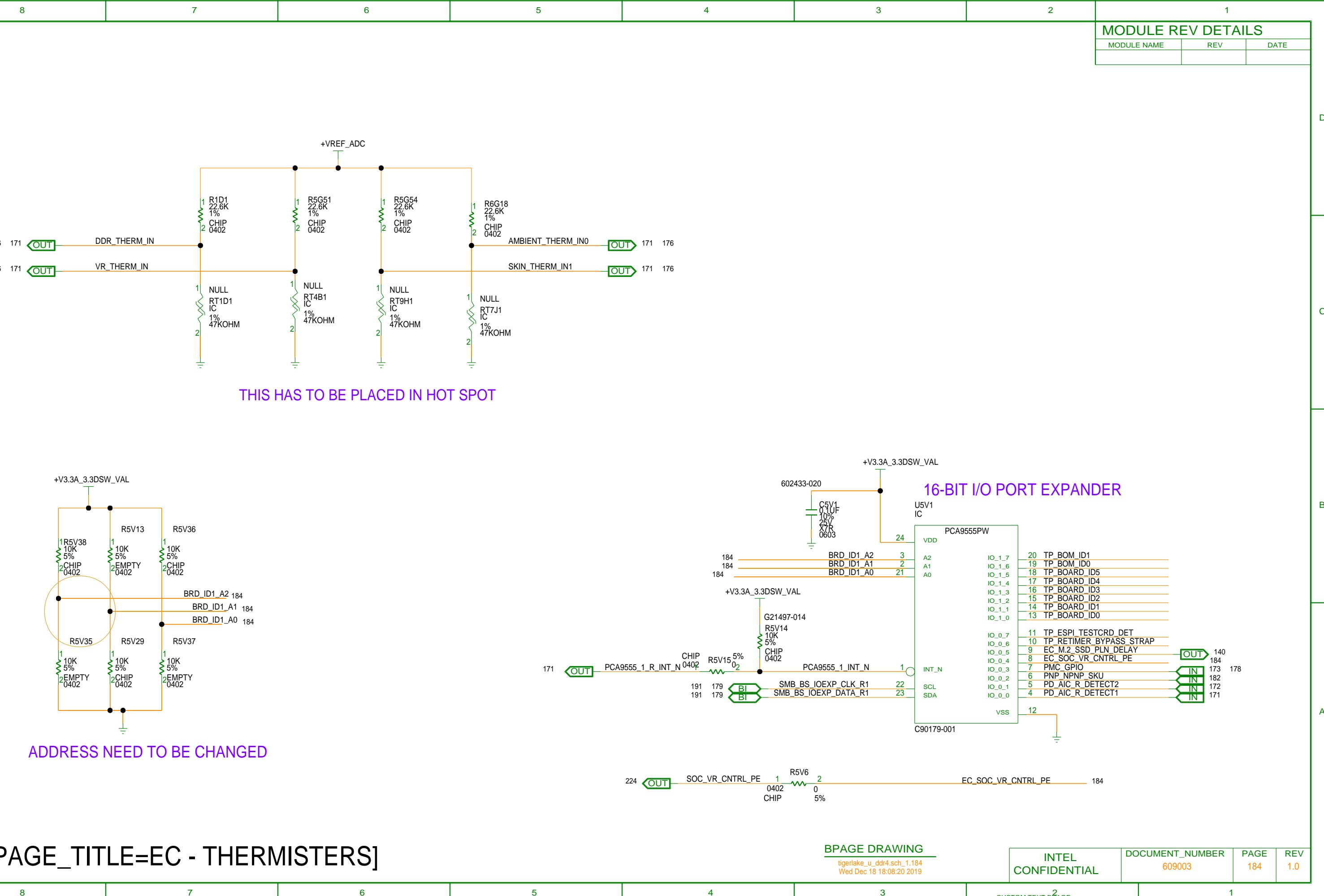
BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.181  
Wed Dec 18 18:08:17 2019

|                       |                           |             |            |
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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>181 | REV<br>1.0 |
| CUSTOM TEXT BPAGE     |                           |             | 1          |

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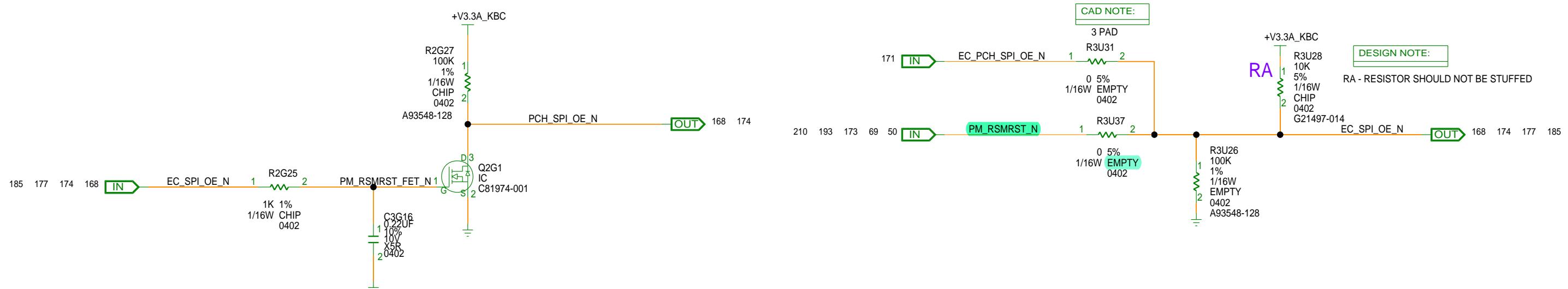
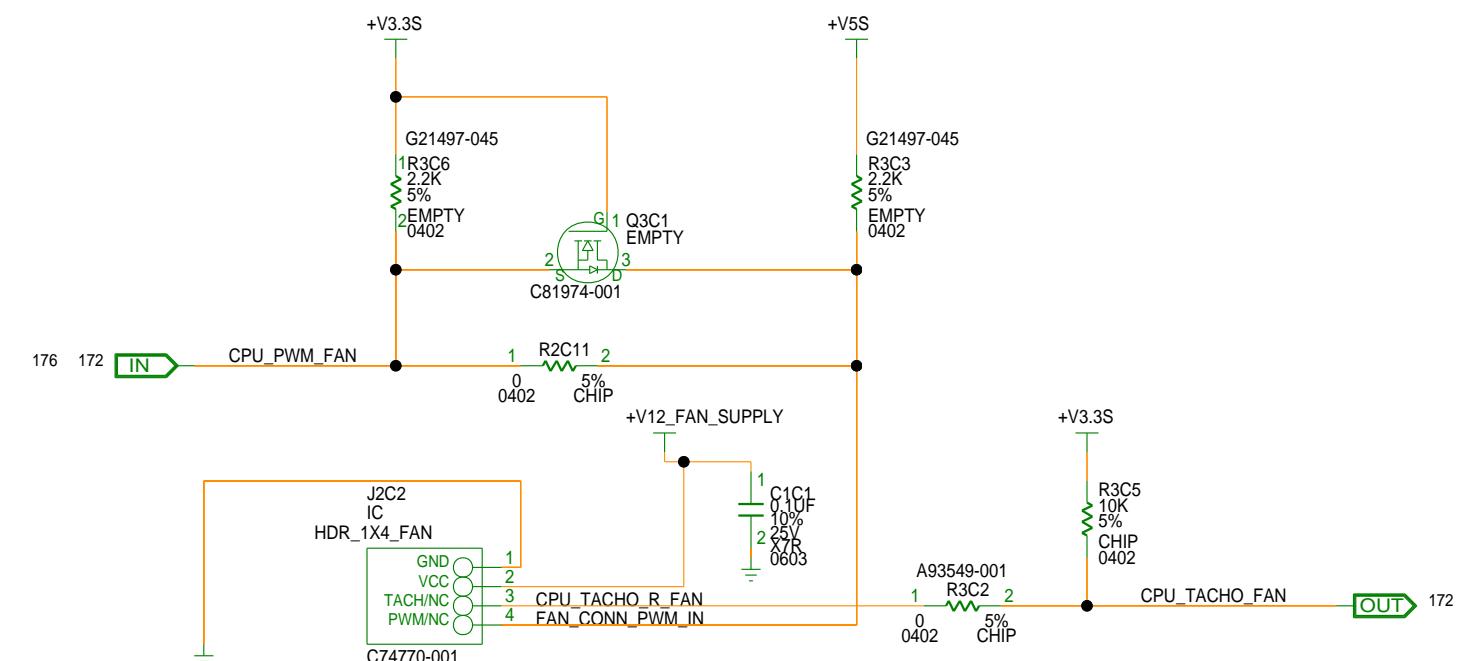




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| MODULE REV DETAILS |     |      |
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| MODULE NAME        | REV | DATE |
|                    |     |      |

# PROCESSOR FAN CONTROL



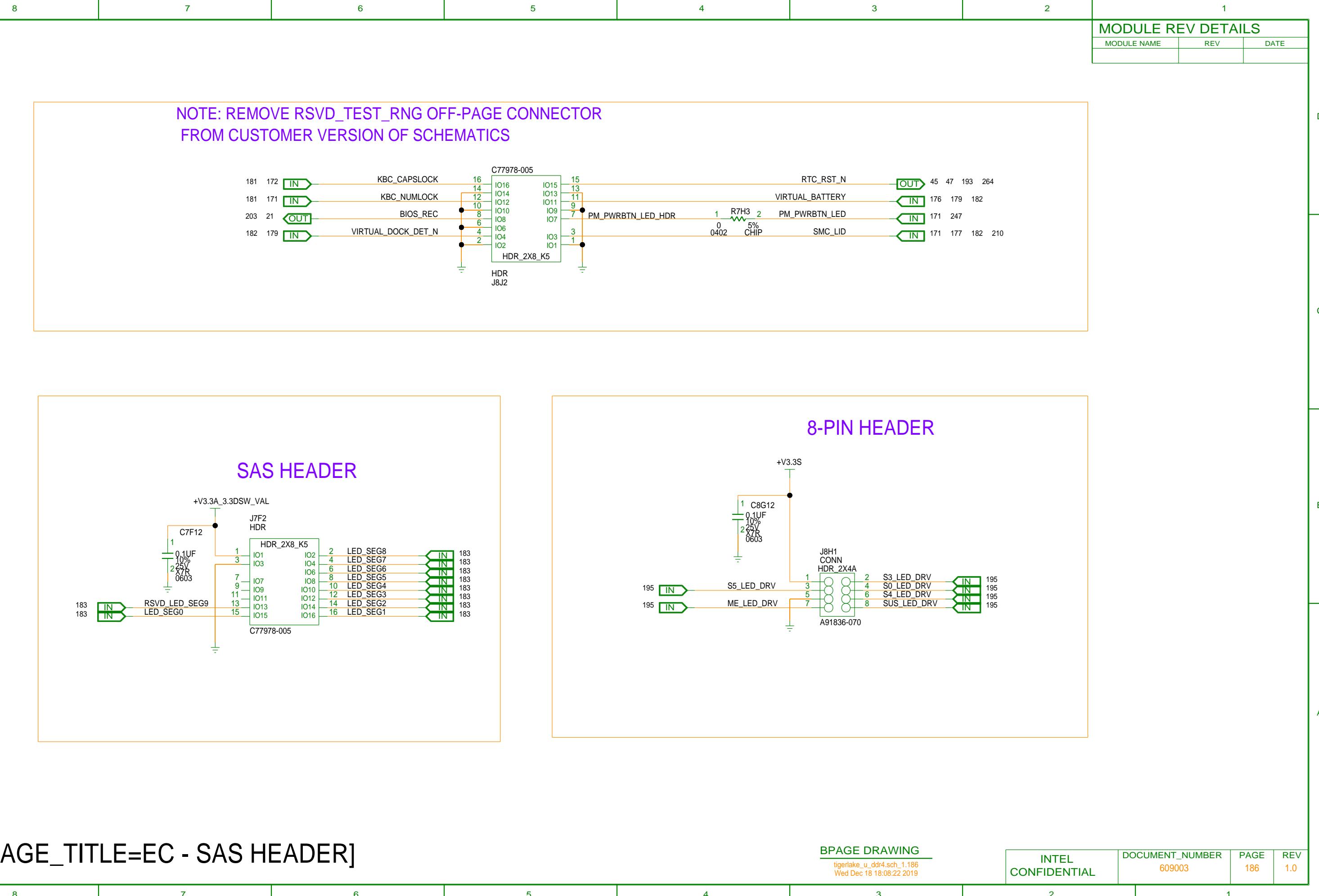
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BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.185  
Wed Dec 18 18:08:21 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
|-----------------------|-----------------|------|-----|
|                       | 609003          | 185  | 1.0 |

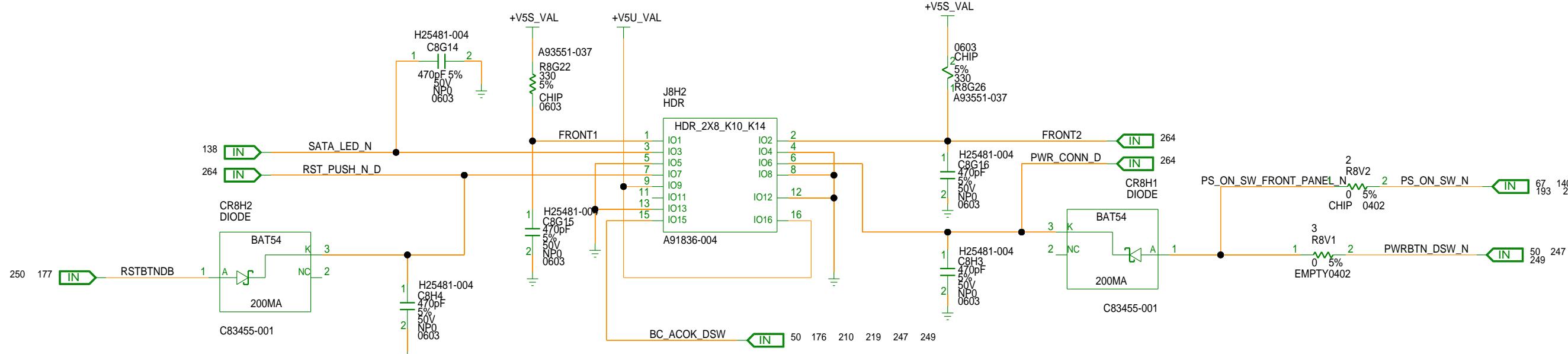
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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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| 8                         | 7 | 6 | 5 | 4 | 3 | 2   | 1    |
| <b>MODULE REV DETAILS</b> |   |   |   |   |   |     |      |
| MODULE NAME               |   |   |   |   |   | REV | DATE |

## FRONT PANEL HEADER



[PAGE\_TITLE=EC - FRONT PANEL HEADER]

BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.187  
Wed Dec 18 18:08:23 2019

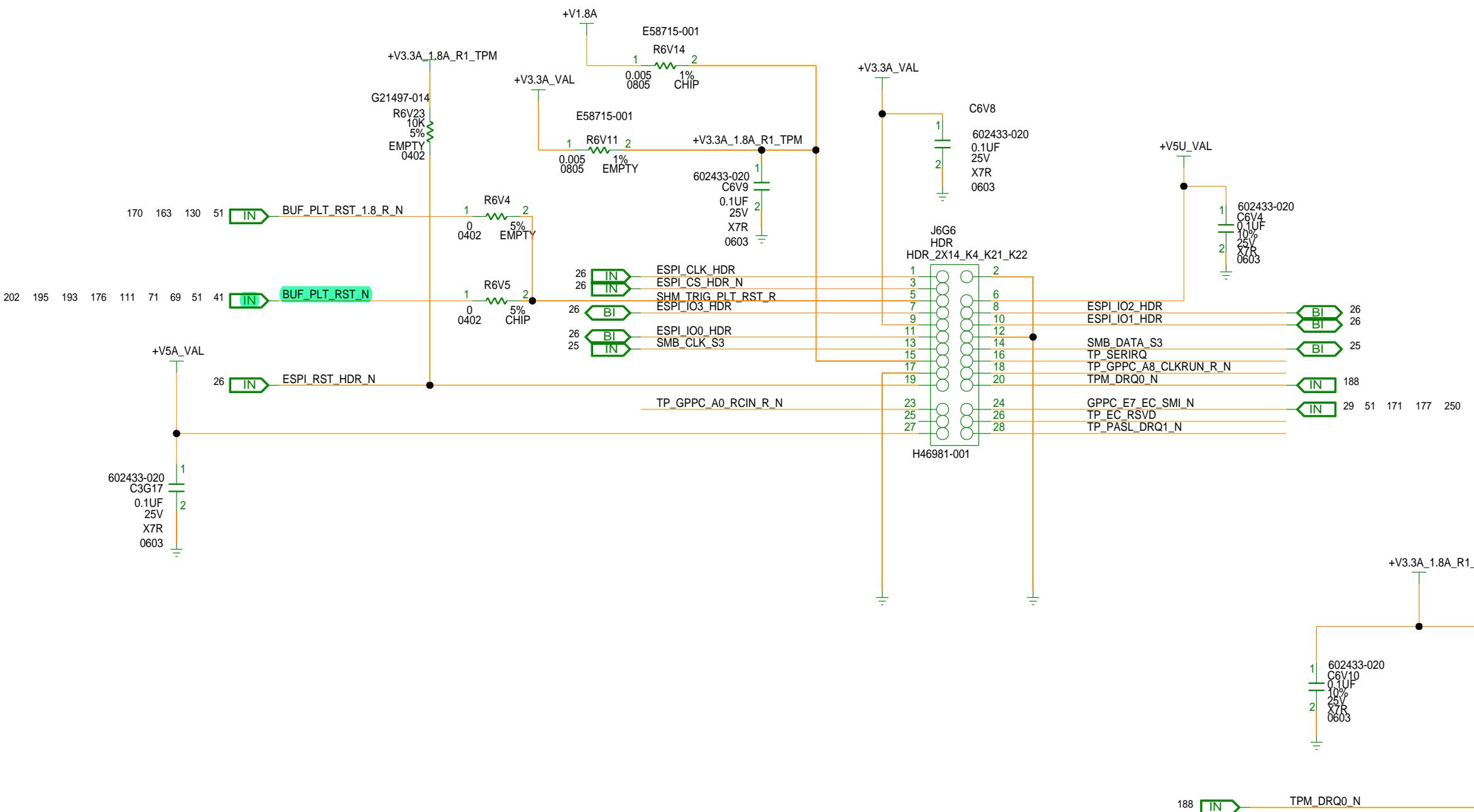
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|-----------------------|---------------------------|-------------|------------|
| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>187 | REV<br>1.0 |
| CUSTOM TEXT BPAGE     |                           |             | 1          |

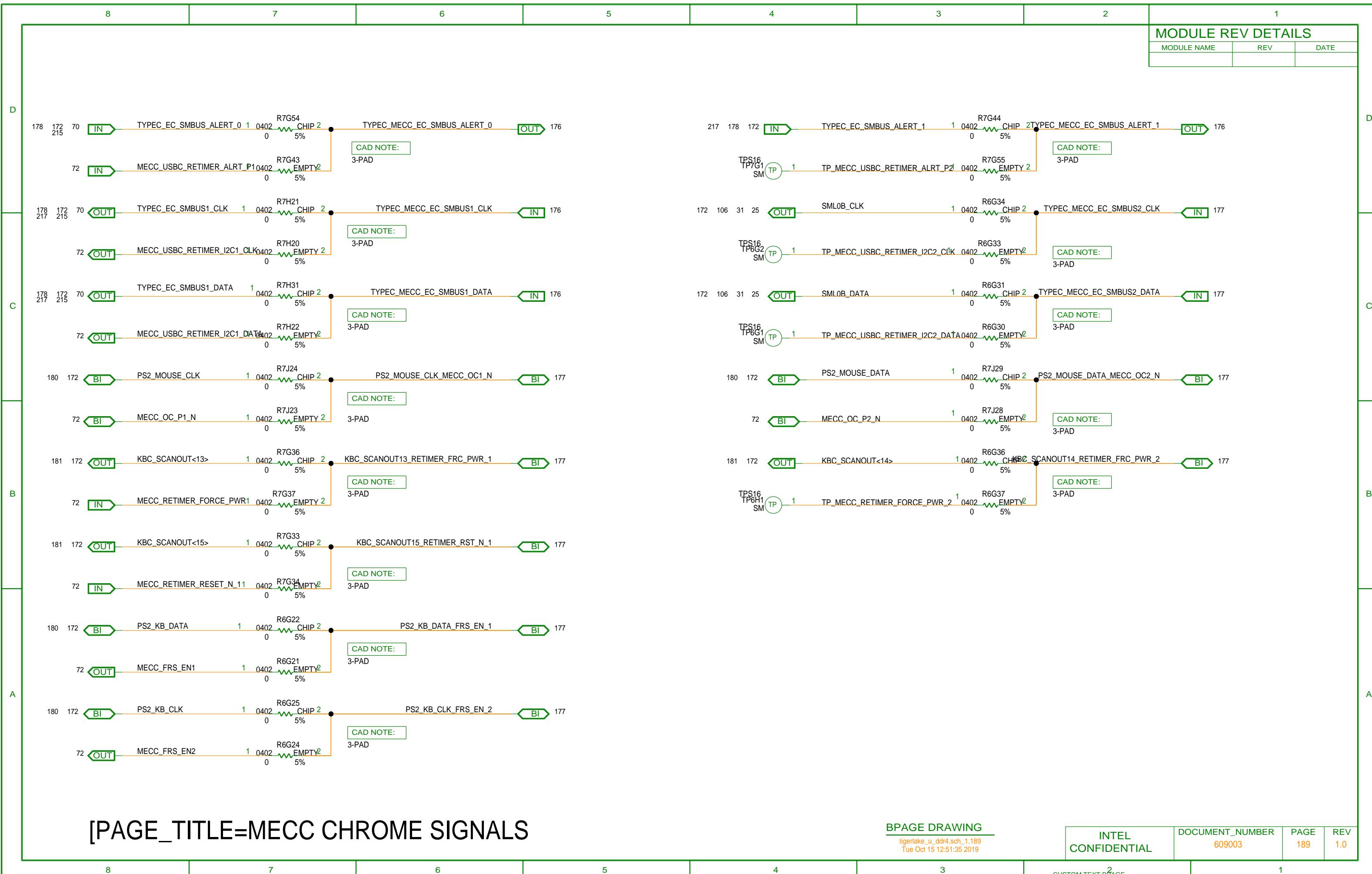
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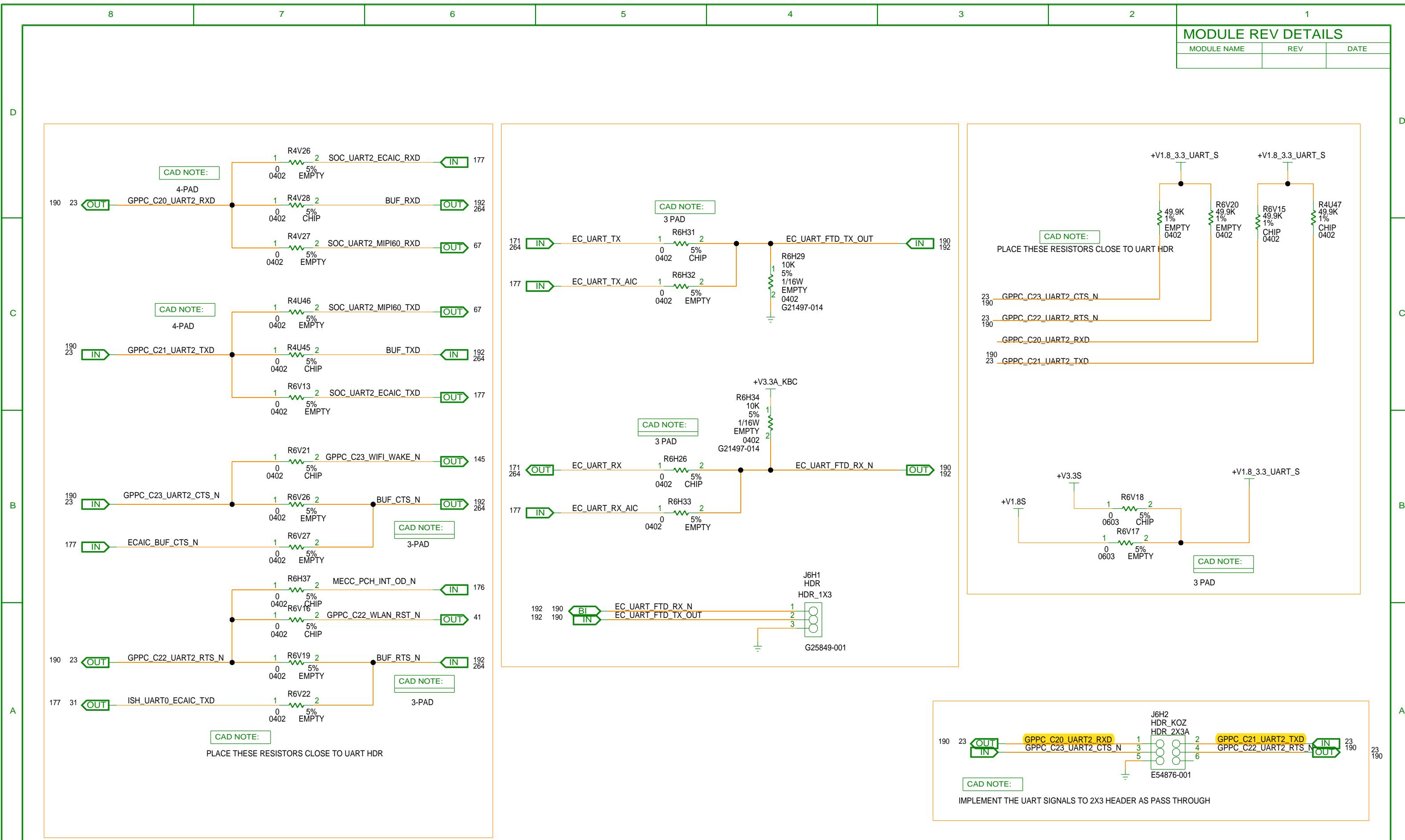
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| <b>MODULE REV DETAILS</b> |   |   |   |   |   |   |   |

| MODULE NAME | REV | DATE |
|-------------|-----|------|
|             |     |      |

# ESPI BUS HEADER







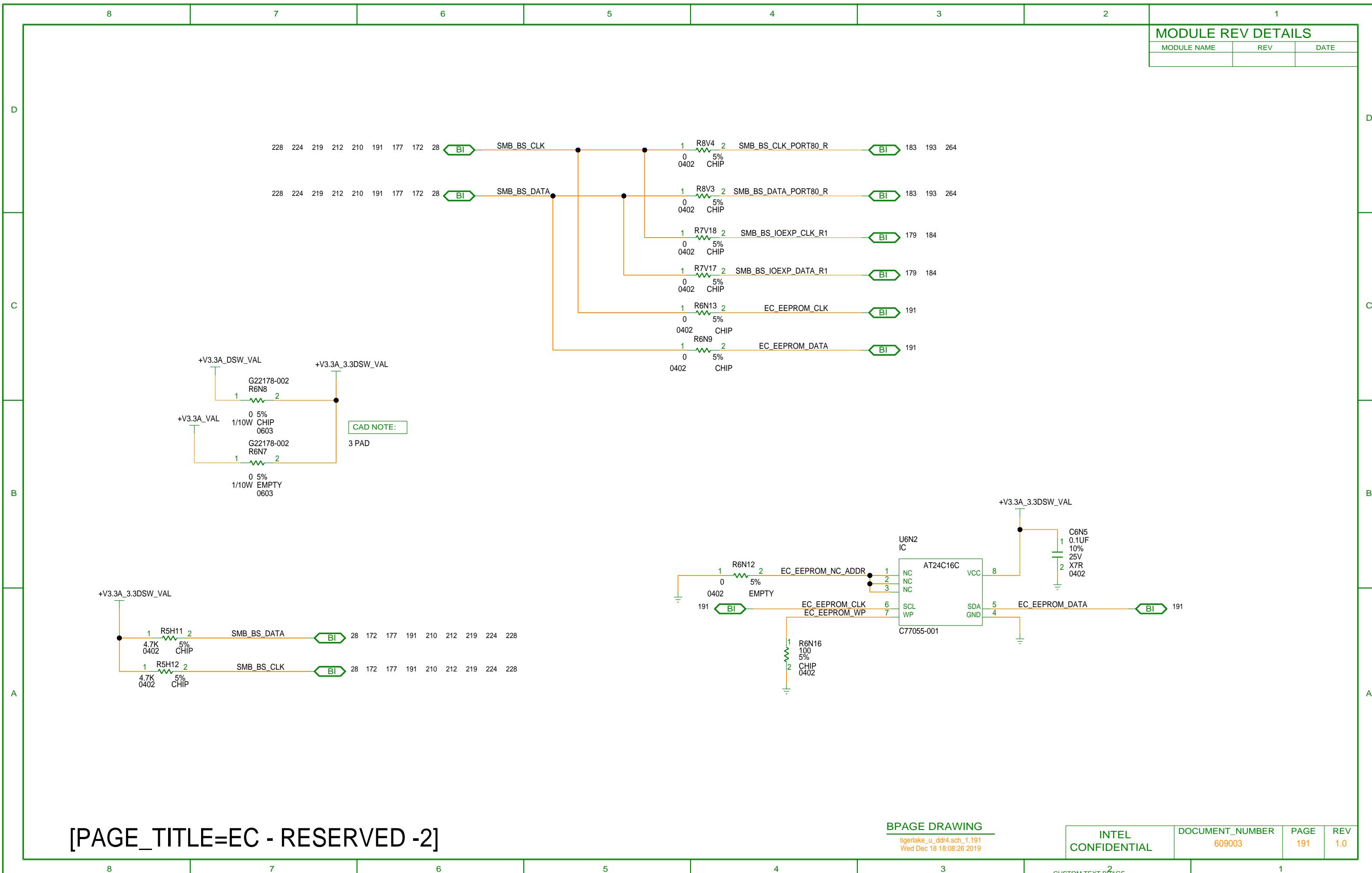
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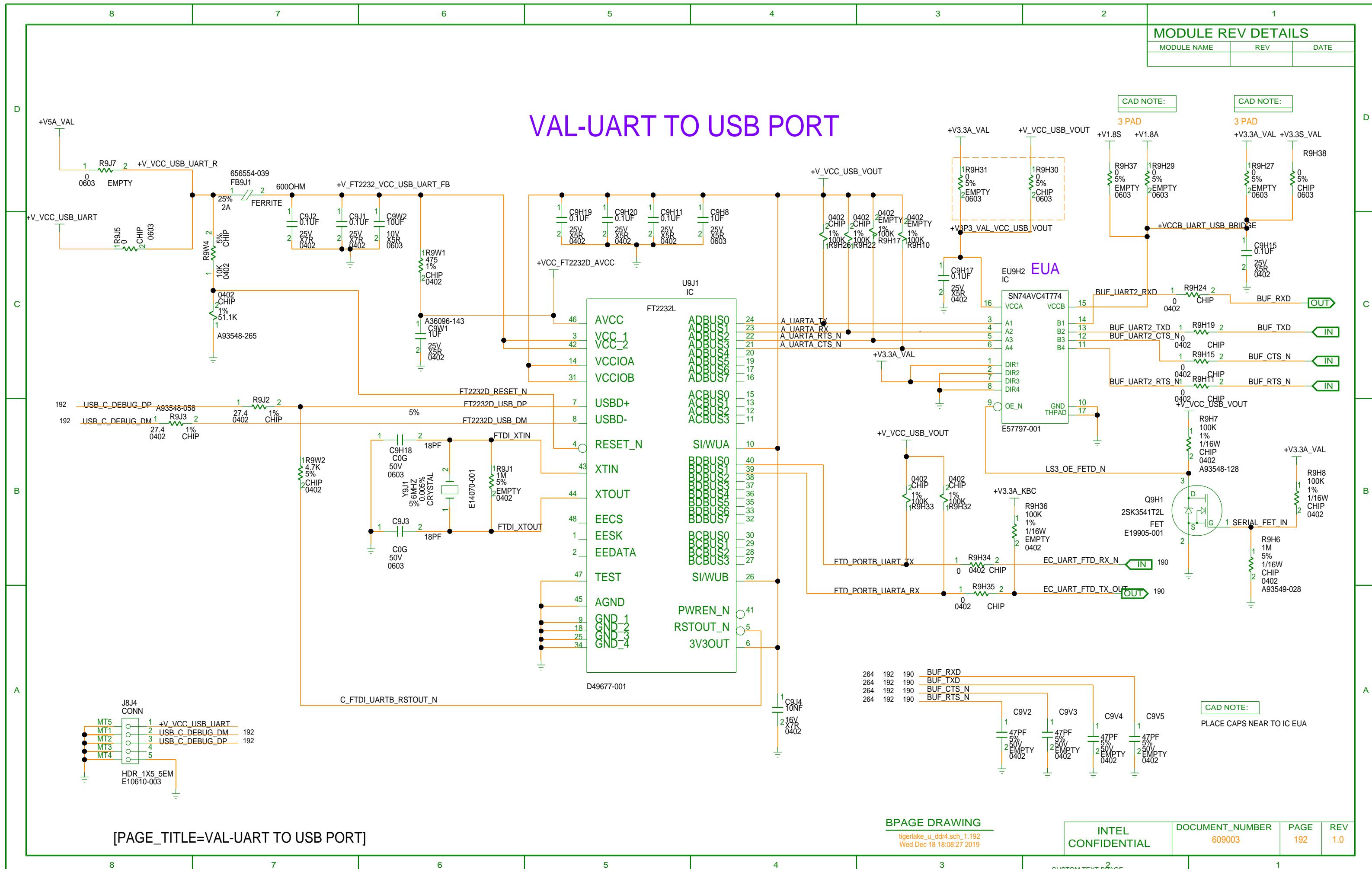
BPAGE DRAWING

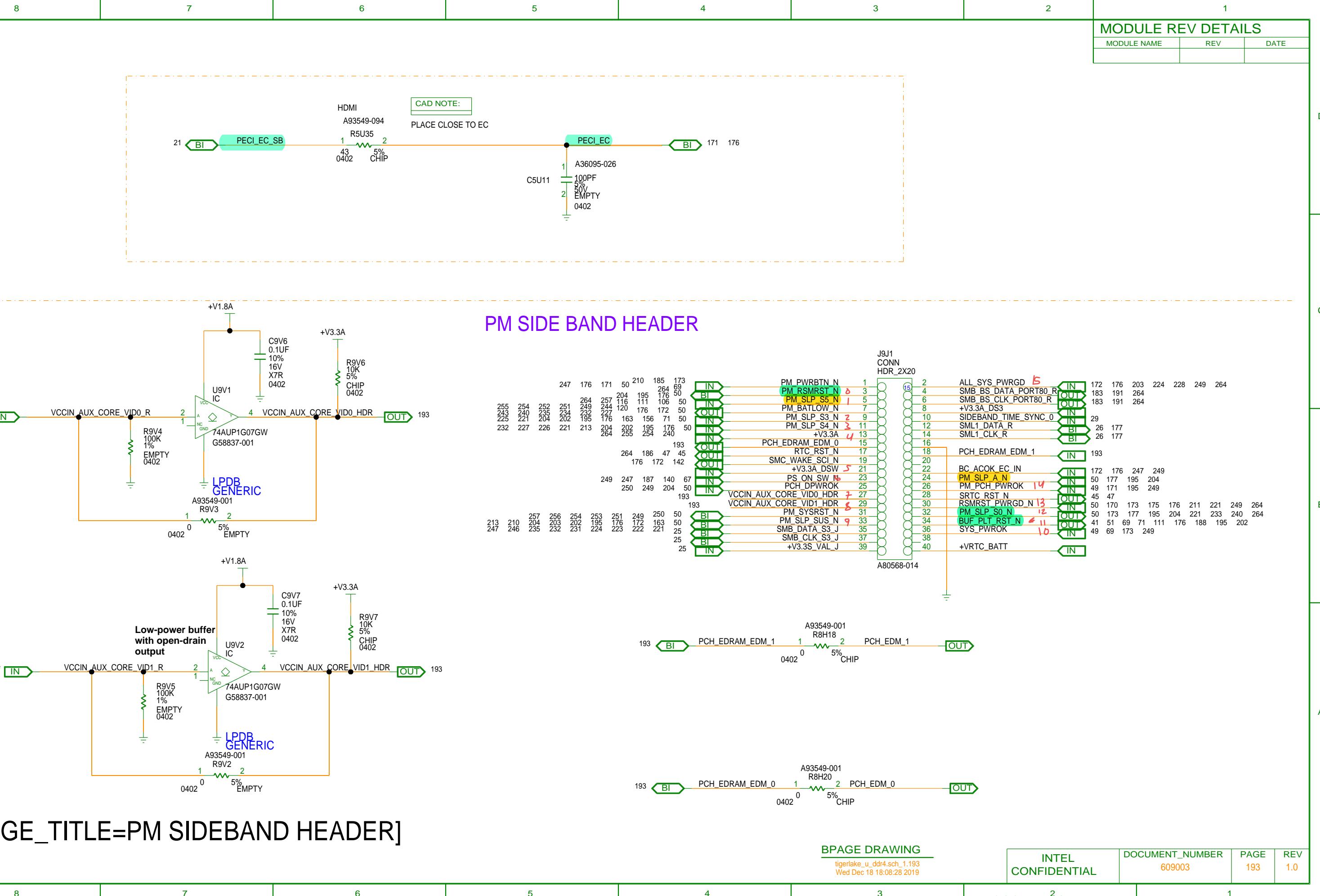
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Wed Dec 18 18:08:25 2019

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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>190 | REV<br>1.0 |
|-----------------------|---------------------------|-------------|------------|

CUSTOM TEXT PAGE 2







|                           |   |     |      |   |   |   |   |
|---------------------------|---|-----|------|---|---|---|---|
| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

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[PAGE\_TITLE=RESERVED]

BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.194  
Tue Oct 15 12:51:41 2019

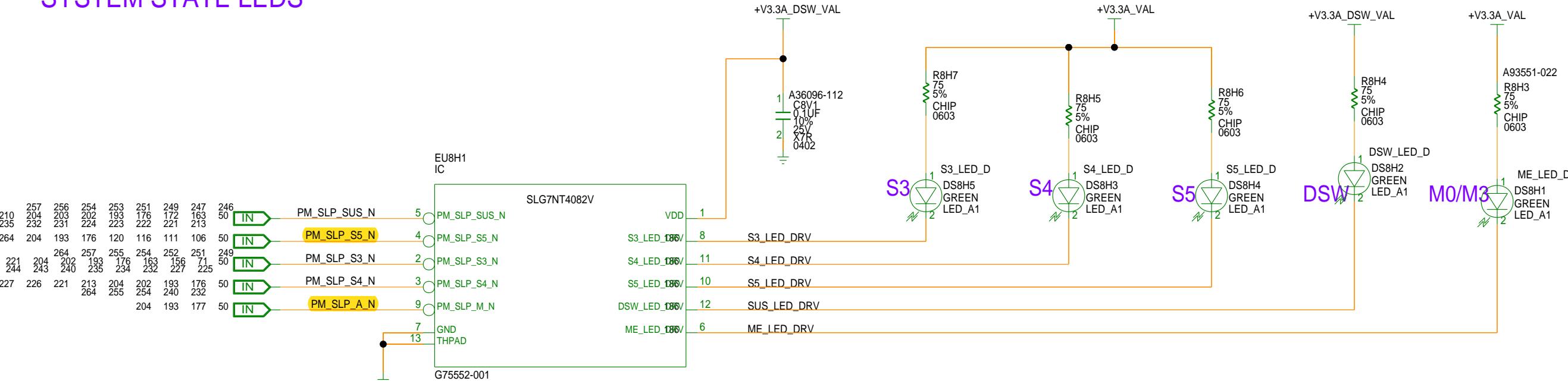
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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>194 | REV<br>1.0 |
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| 8 | 7 | 6 | 5 | 4 | 3 | CUSTOM TEXT 2 PAGE | 1 |
|---|---|---|---|---|---|--------------------|---|

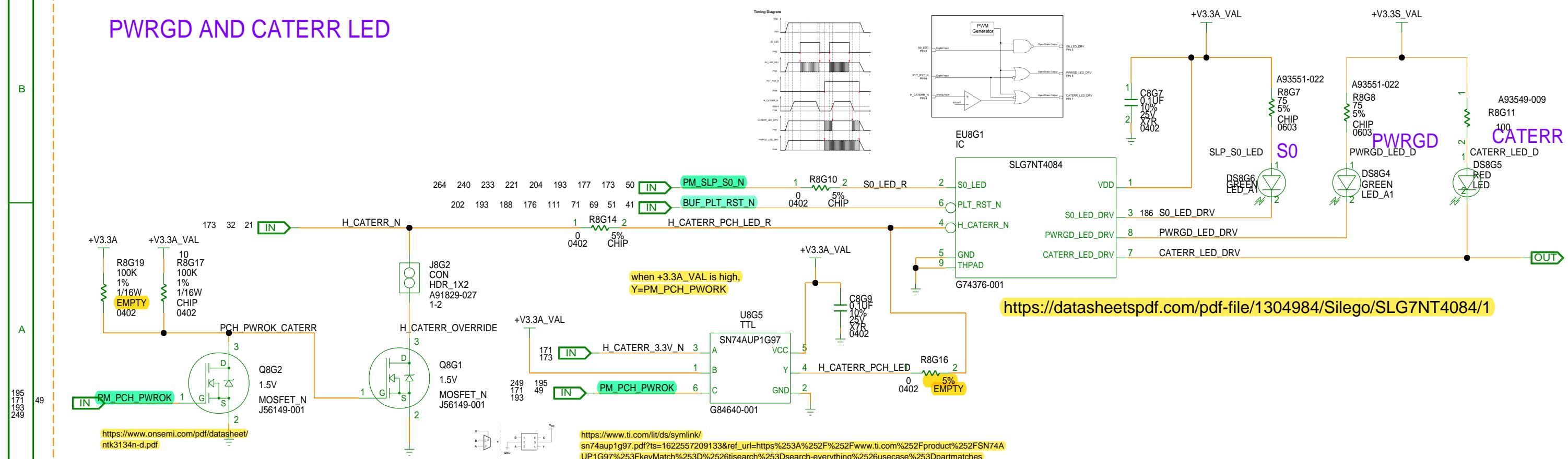
## MODULE REV DETAILS

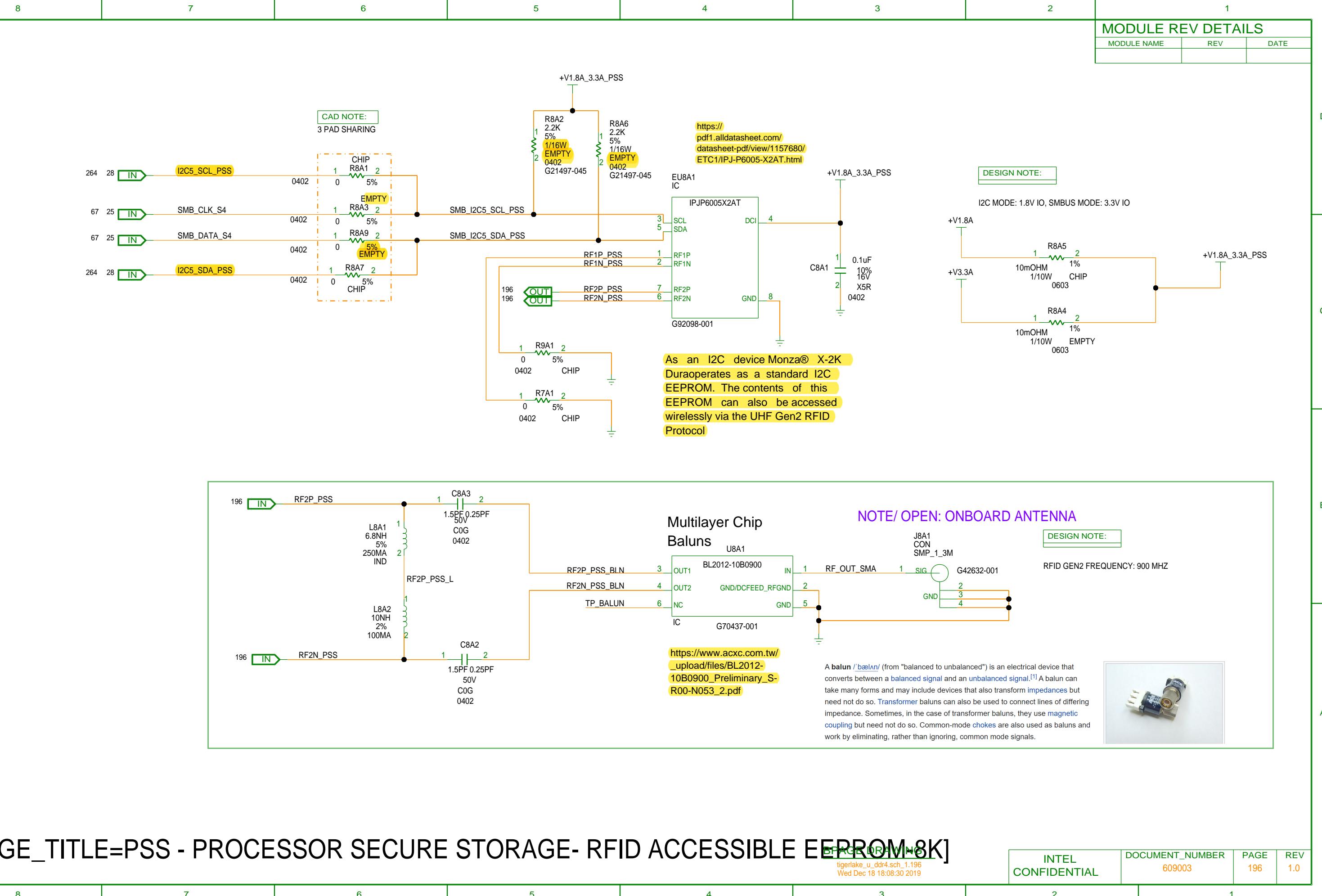
| MODULE NAME | REV | DATE |
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## SYSTEM STATE LEDS



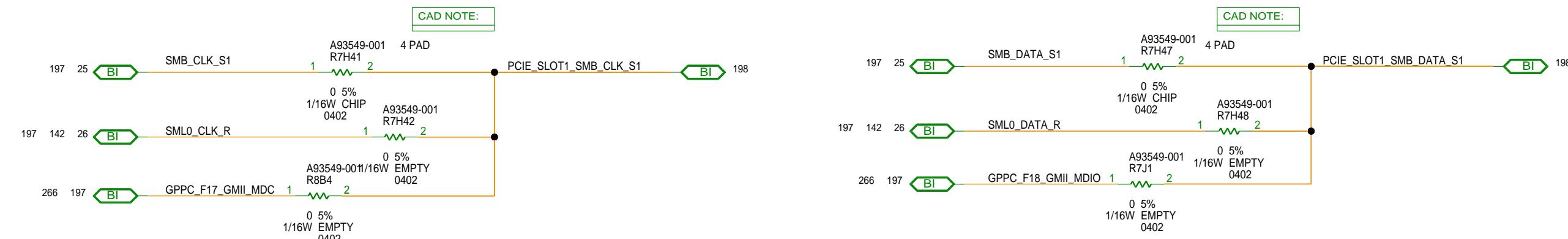
## PWRGD AND CATERR LED



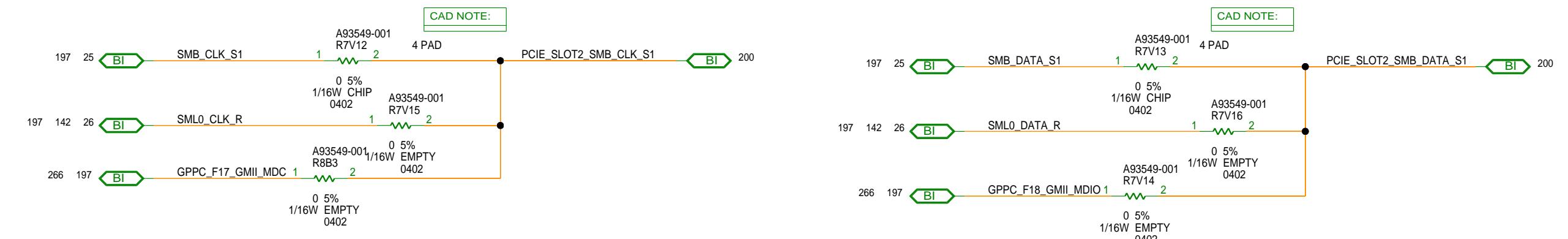


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| 8                  | 7 | 6 | 5 | 4   | 3    | 2 | 1 |
| MODULE REV DETAILS |   |   |   |     |      |   |   |
| MODULE NAME        |   |   |   | REV | DATE |   |   |

## PCIE SLOT 1 SMB SIGNALS



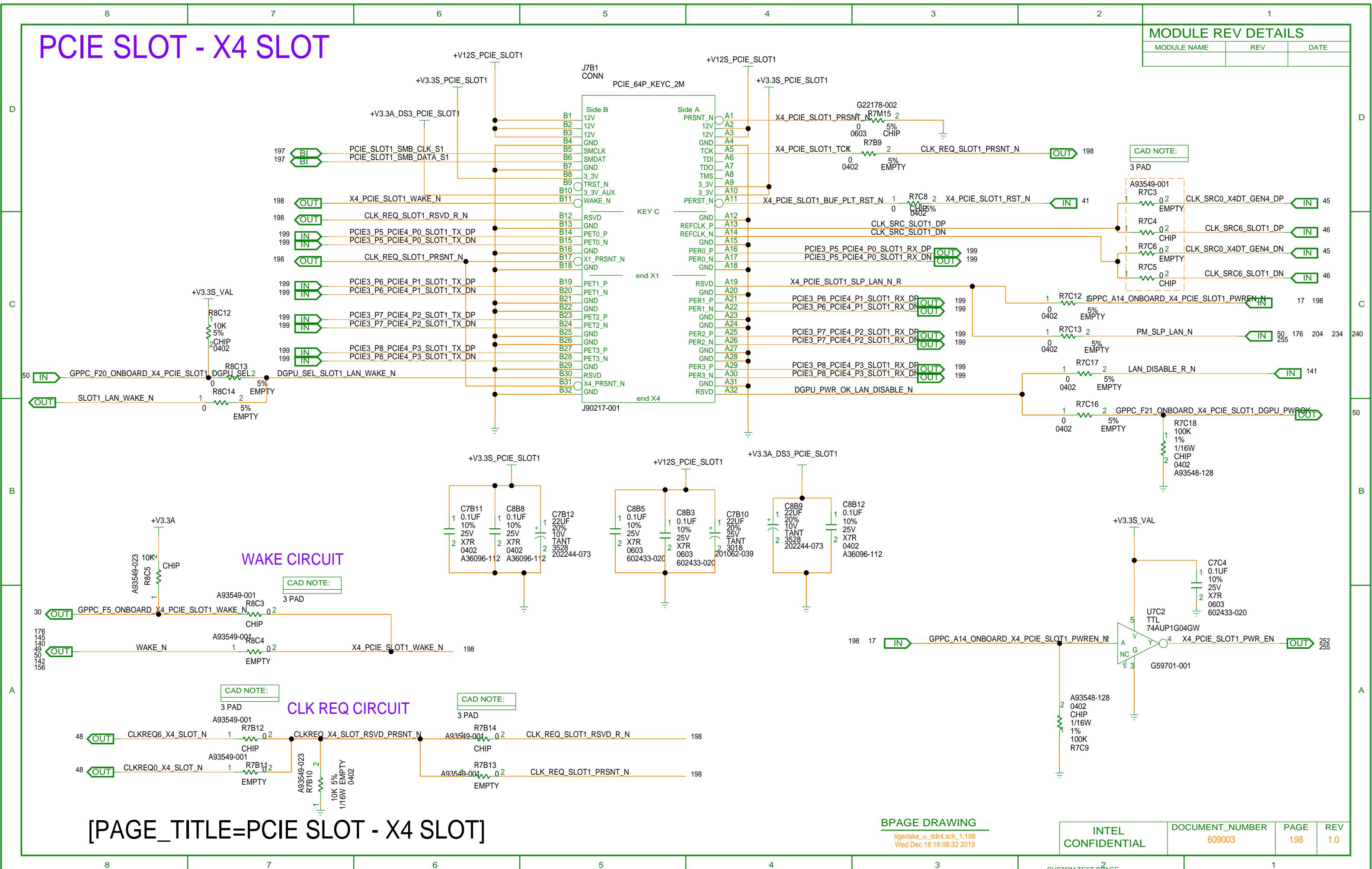
## PCIE SLOT 2 SMB SIGNALS

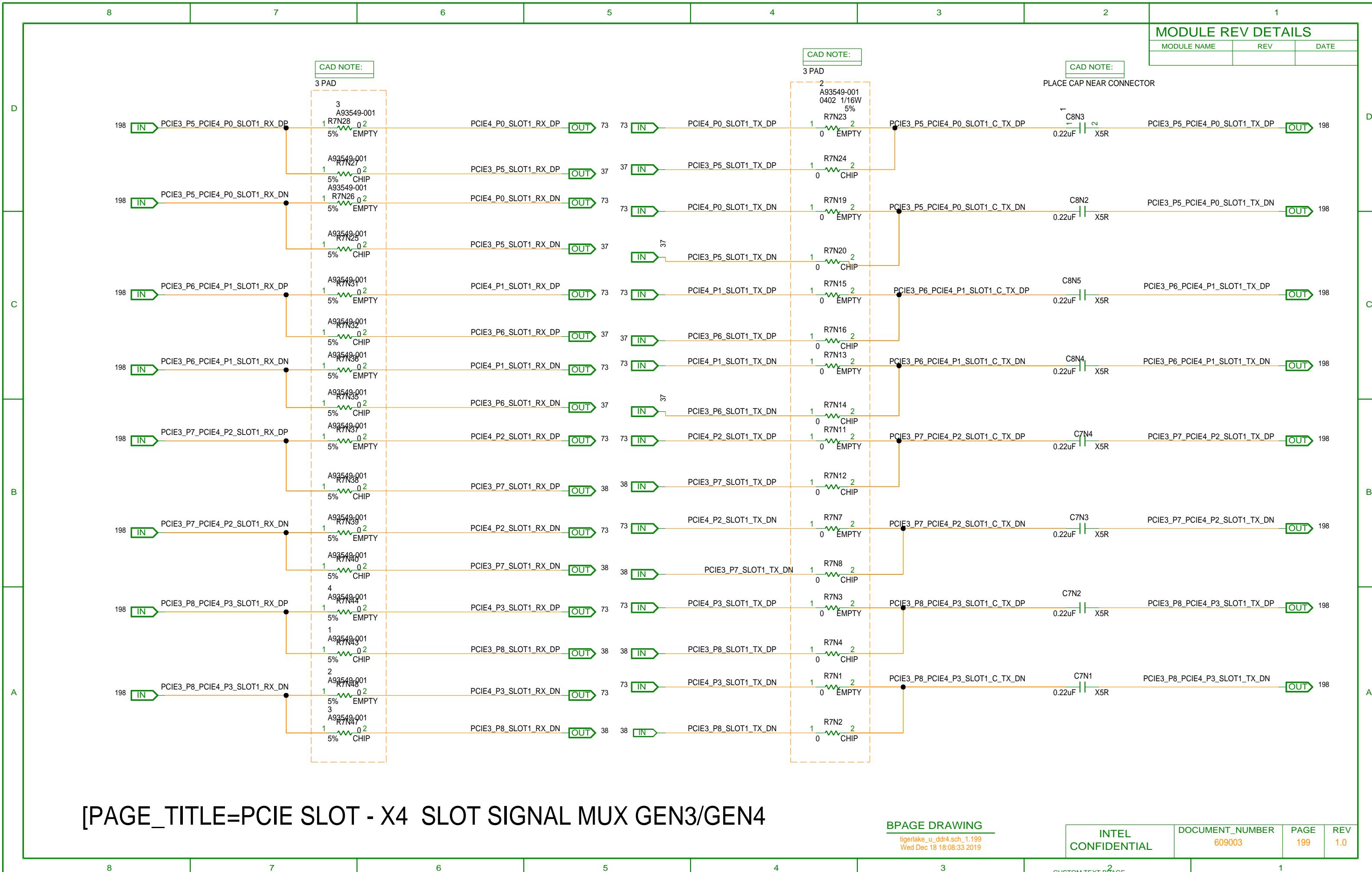


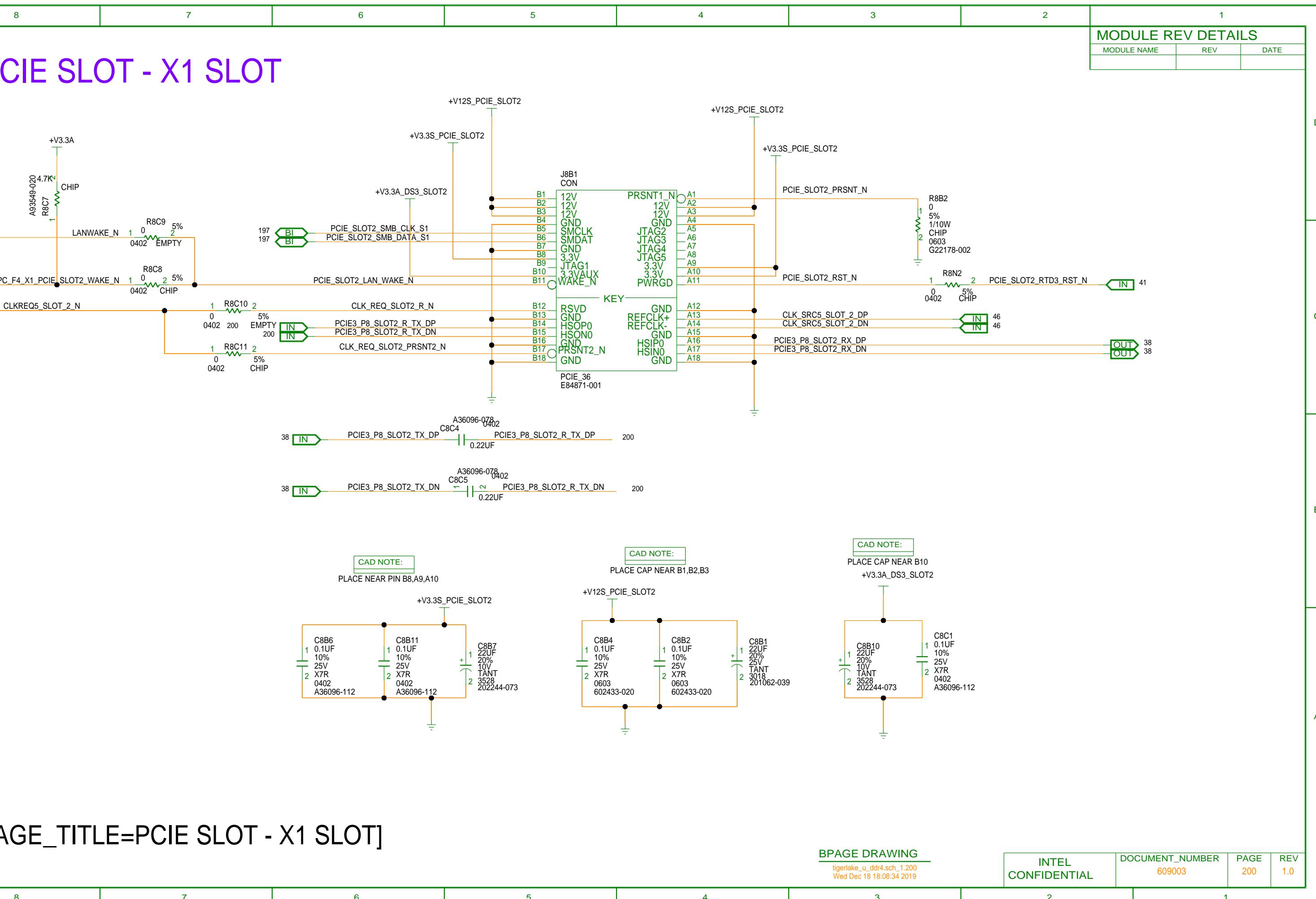
BPAGE DRAWING

tigerlake\_u\_ddr4.sch\_1.197  
Wed Dec 18 18:08:31 2019

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| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>197 | REV<br>1.0 |
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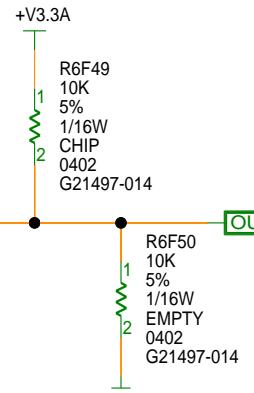
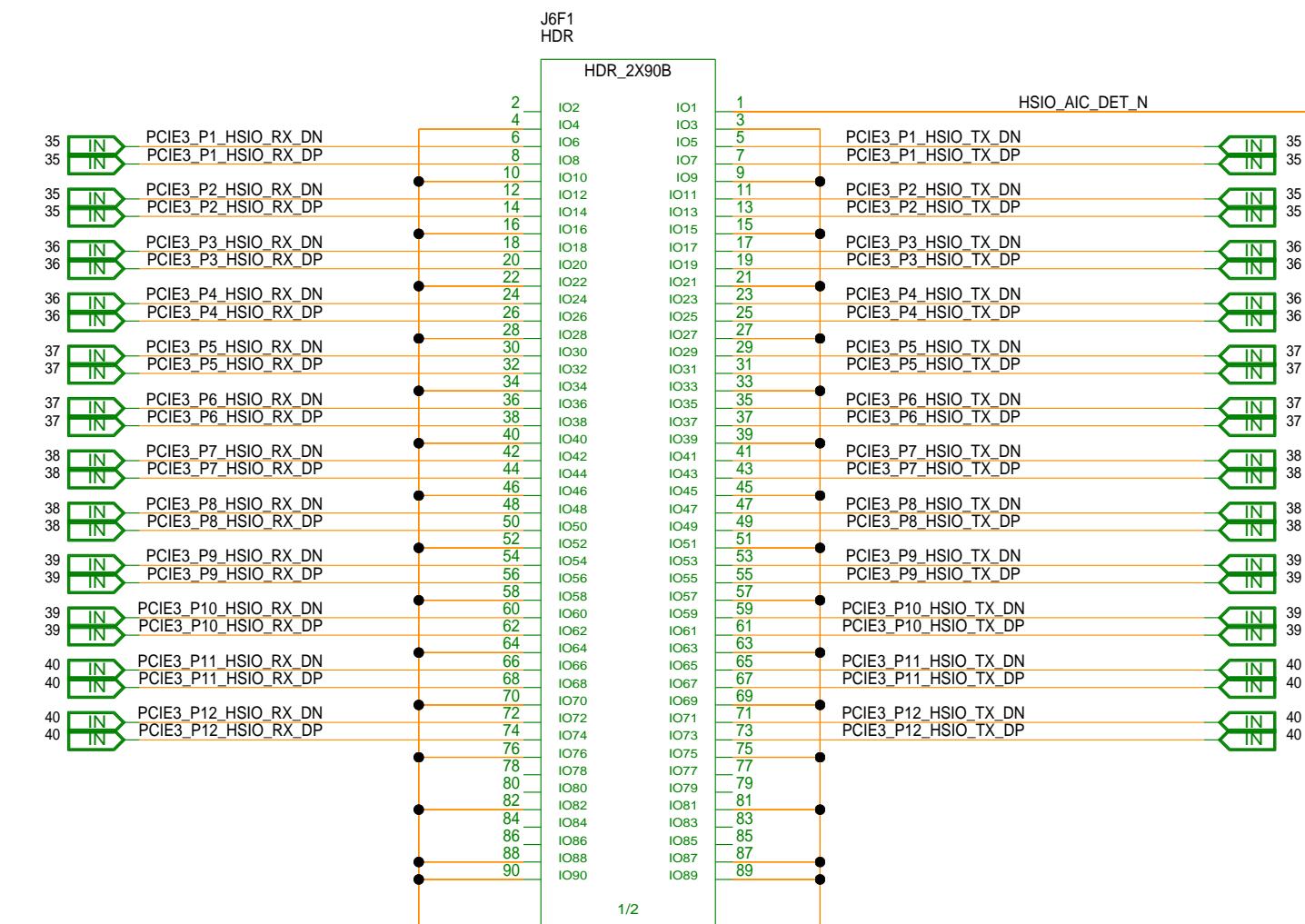
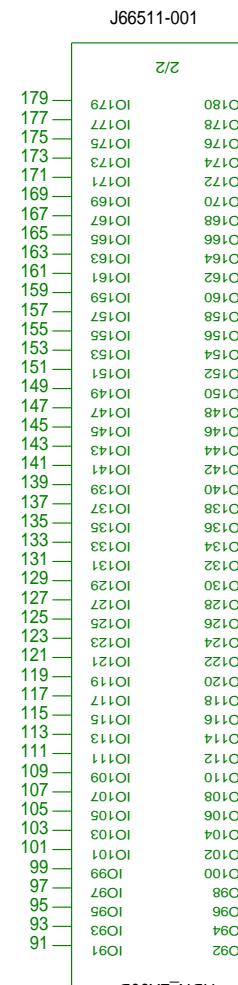






|                           |   |   |   |   |   |     |      |
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| 8                         | 7 | 6 | 5 | 4 | 3 | 2   | 1    |
| <b>MODULE REV DETAILS</b> |   |   |   |   |   |     |      |
| MODULE NAME               |   |   |   |   |   | REV | DATE |

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



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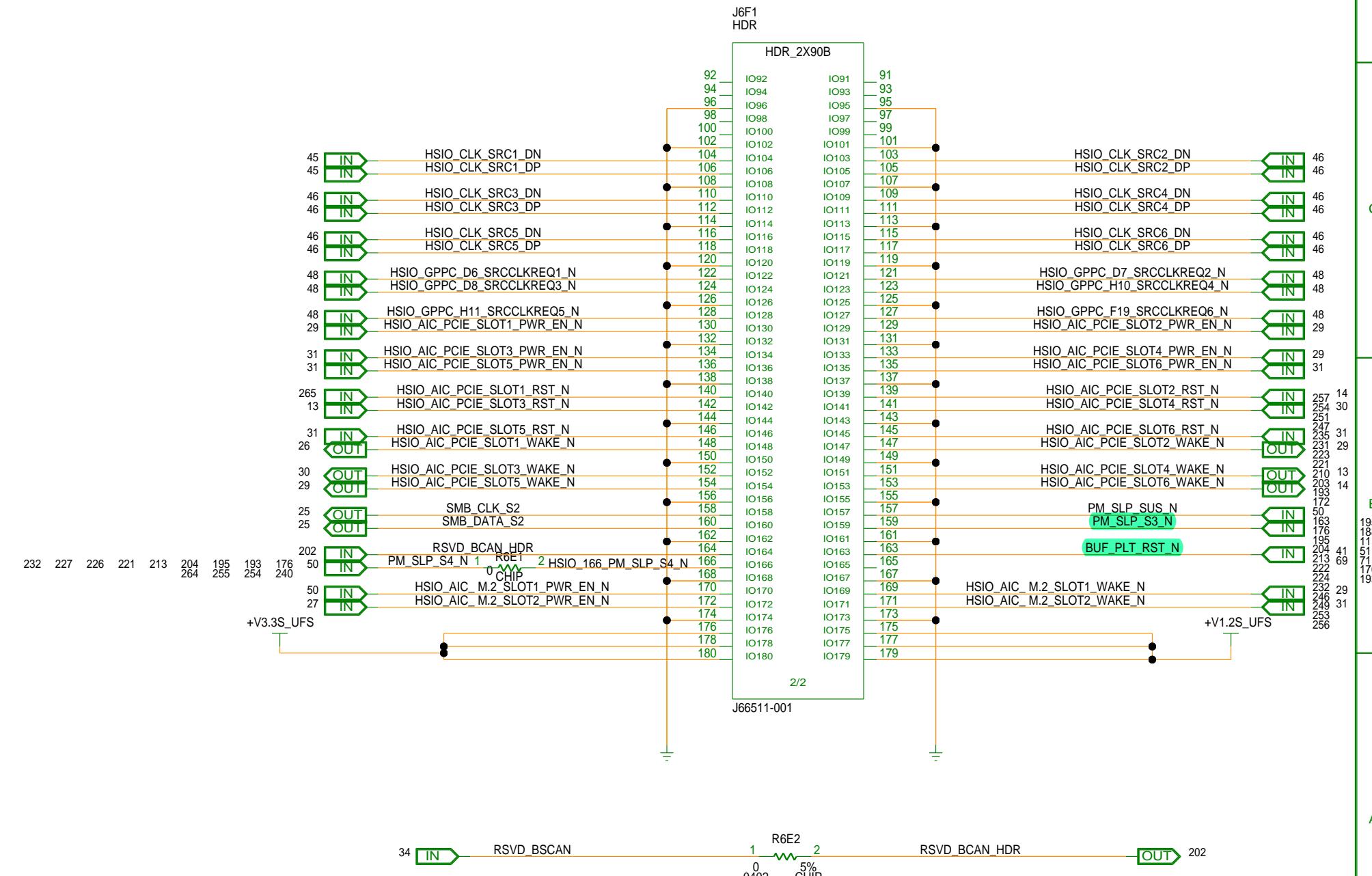
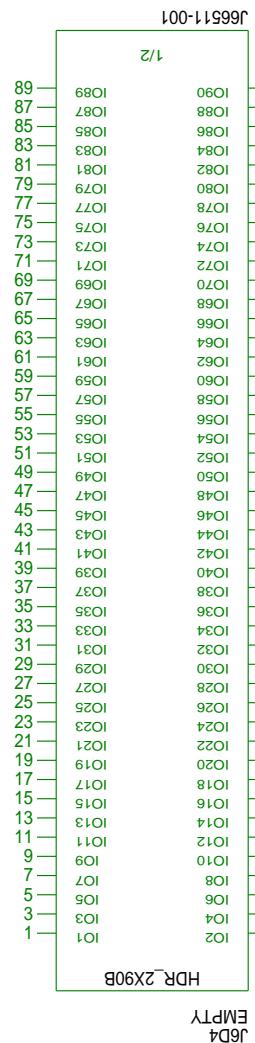
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|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|

| MODULE REV DETAILS |     |      |
|--------------------|-----|------|
| MODULE NAME        | REV | DATE |
|                    |     |      |

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



[PAGE\_TITLE=HSIO CONNECTOR (2 OF 4)]

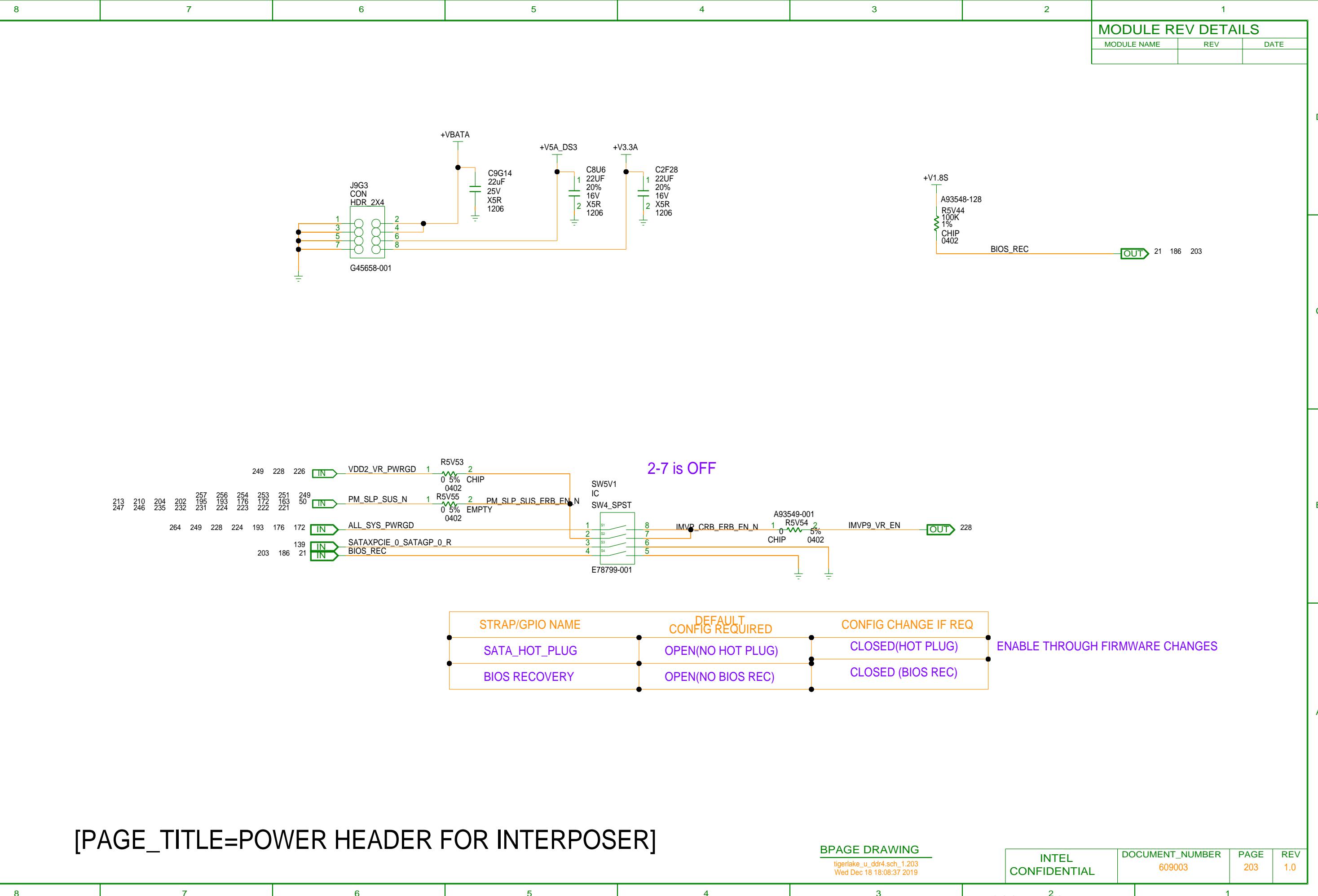
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Wed Dec 18 18:08:36 2019

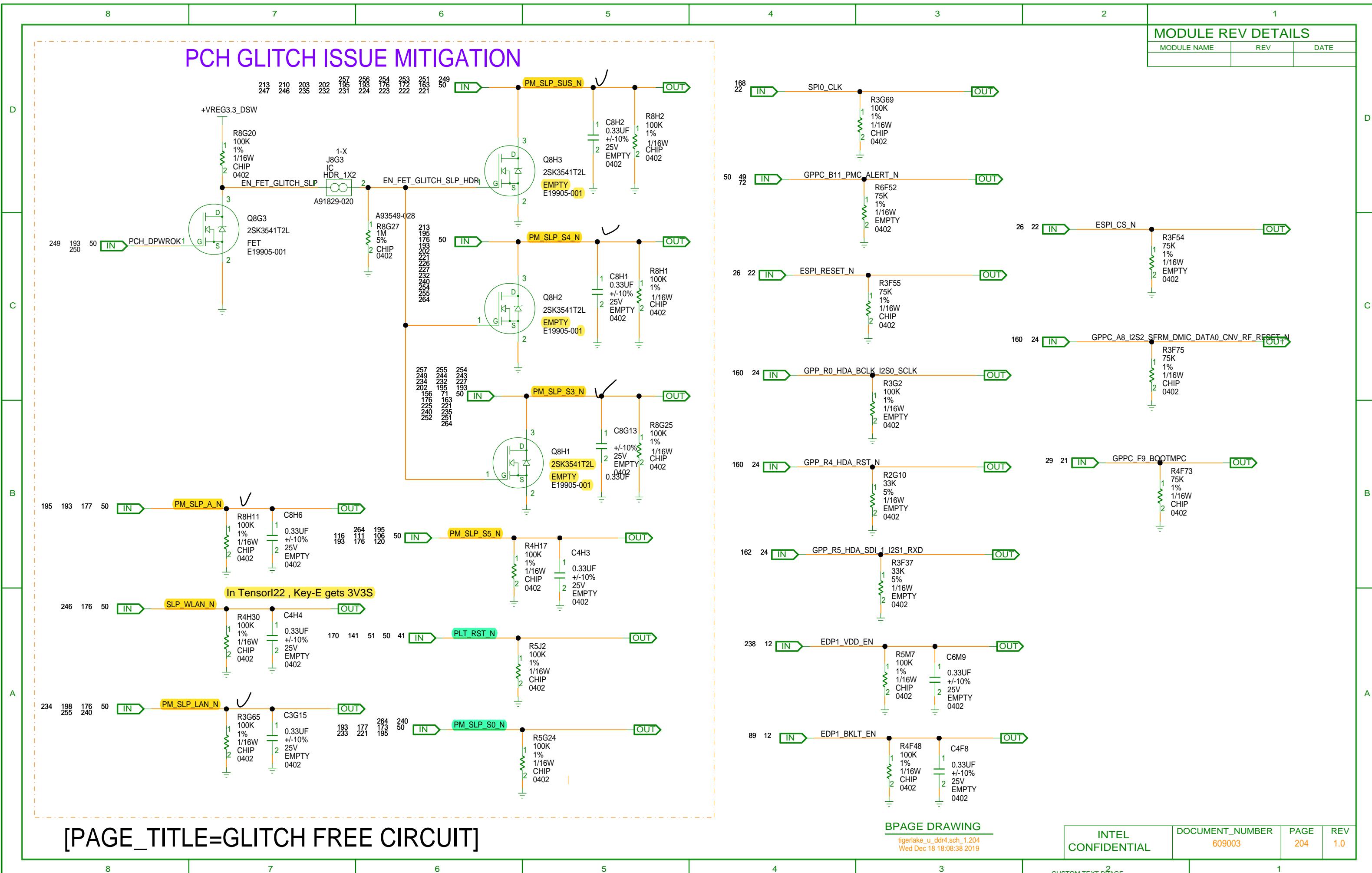
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|-----------------------|-----------------|------|-----|
|                       | 609003          | 202  | 1.0 |

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|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|

CUSTOM TEXT B PAGE

1





|                           |   |     |      |   |   |   |   |
|---------------------------|---|-----|------|---|---|---|---|
| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

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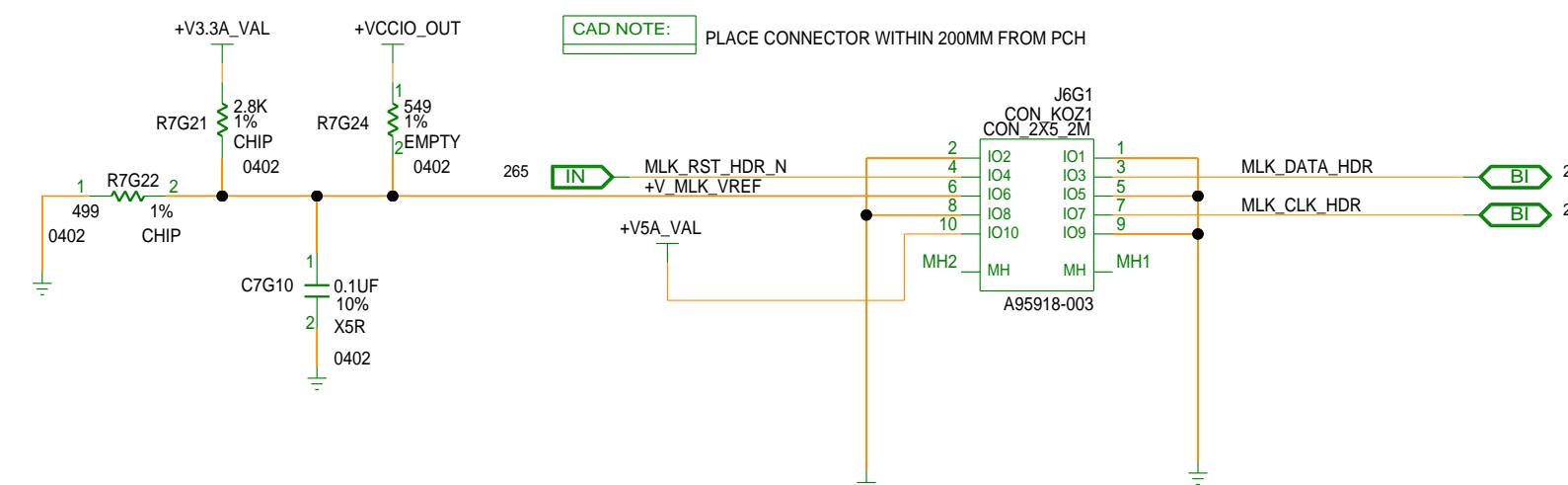
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## MLINK HEADER



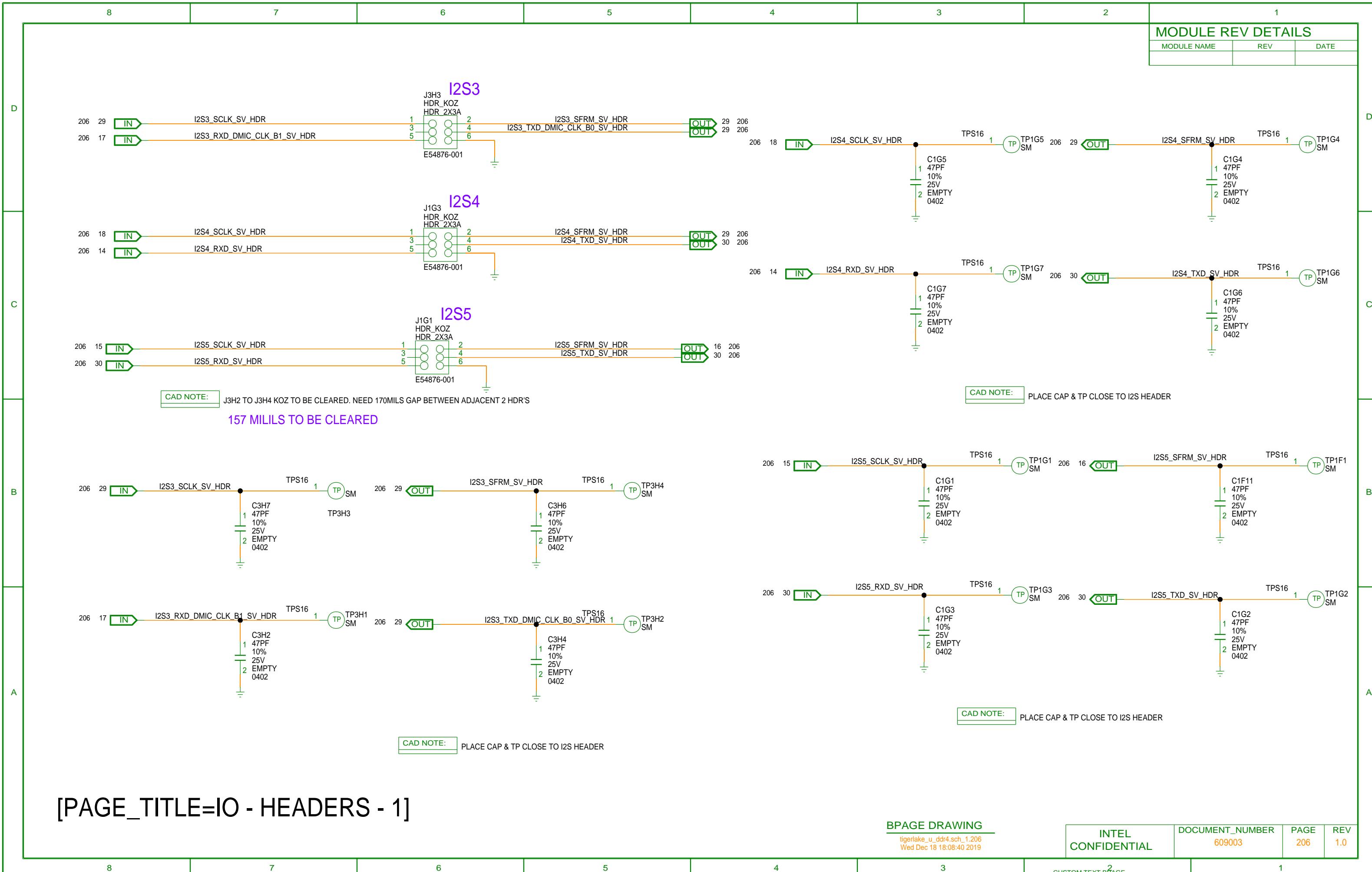
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BPAGE DRAWING

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Wed Dec 18 18:08:39 2019

| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
|-----------------------|-----------------|------|-----|
|                       | 609003          | 205  | 1.0 |

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|-------------------|---|---|---|---|---|---|---|
| 8                 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| CUSTOM TEXT BPAGE |   |   |   |   |   |   |   |
|                   |   |   |   |   |   |   |   |



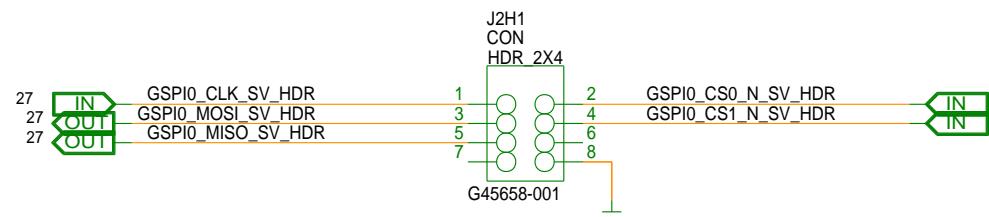
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|---------------------------|---|---|---|---|---|---|---|
| 8                         | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |   |   |   |   |   |   |

CAD NOTE: MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

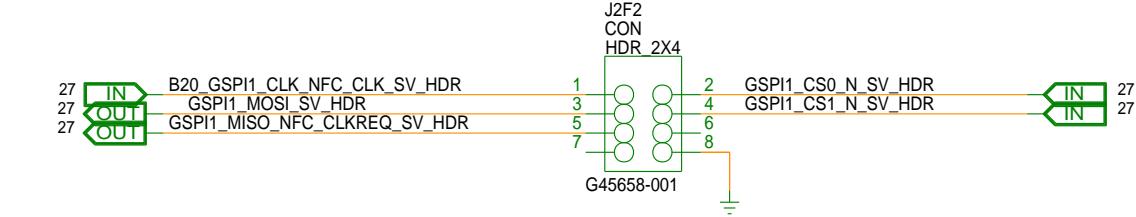
CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

## GSPI0 HEADER



## GSPI1 HEADER



GSPI2 IS AVAILABLE ON ISH SPI AND ISH UART HEADER  
SPI1 IS AVAILABLE ON THC SV HEADER

|                           |   |     |      |   |   |   |   |
|---------------------------|---|-----|------|---|---|---|---|
| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

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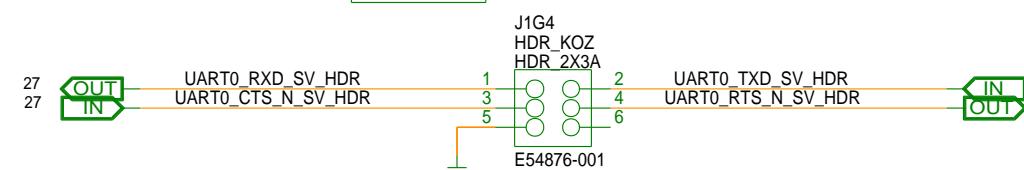
CAD NOTE:

MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

## LPSS UART0 HEADER

CAD NOTE:

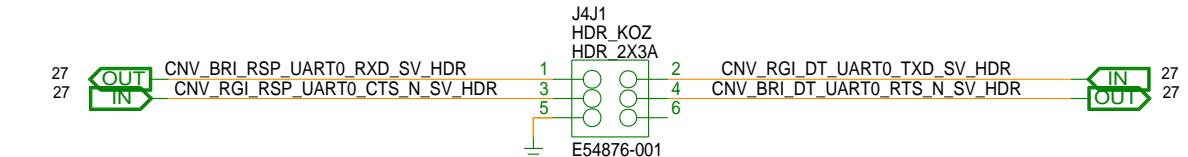
PLACE CONNECTOR WITHIN 300MM FROM PCH



## CNV UART0 HEADER

CAD NOTE:

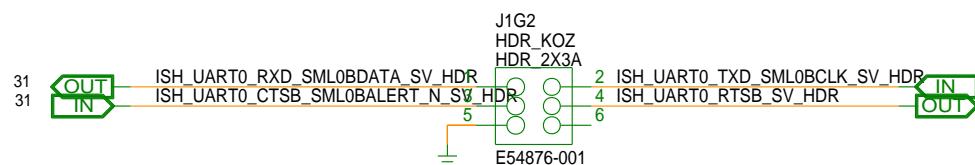
PLACE CONNECTOR WITHIN 300MM FROM PCH



## ISH UART0 / SMLINK0B HEADER

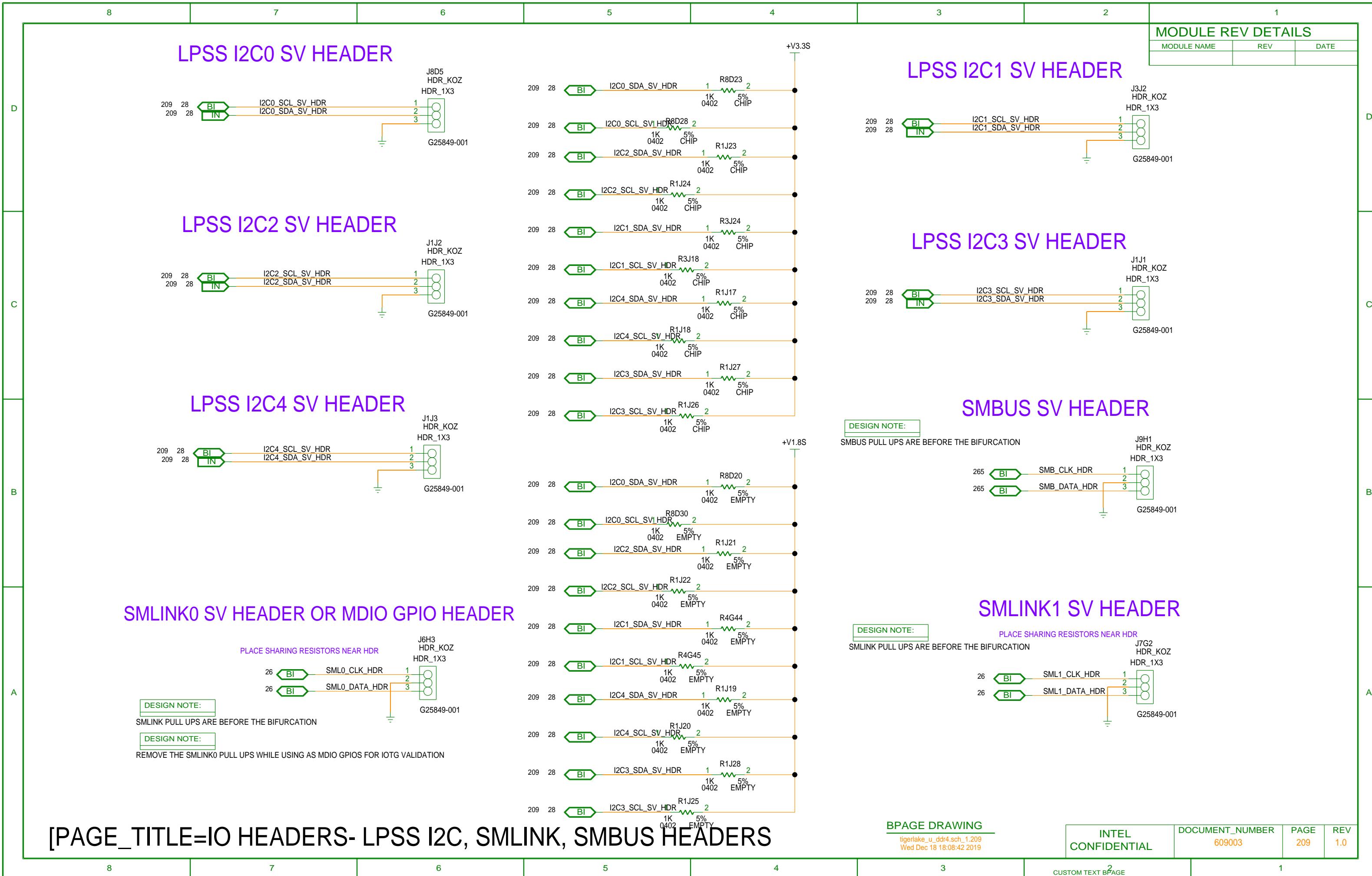
CAD NOTE:

PLACE CONNECTOR WITHIN 300MM FROM PCH



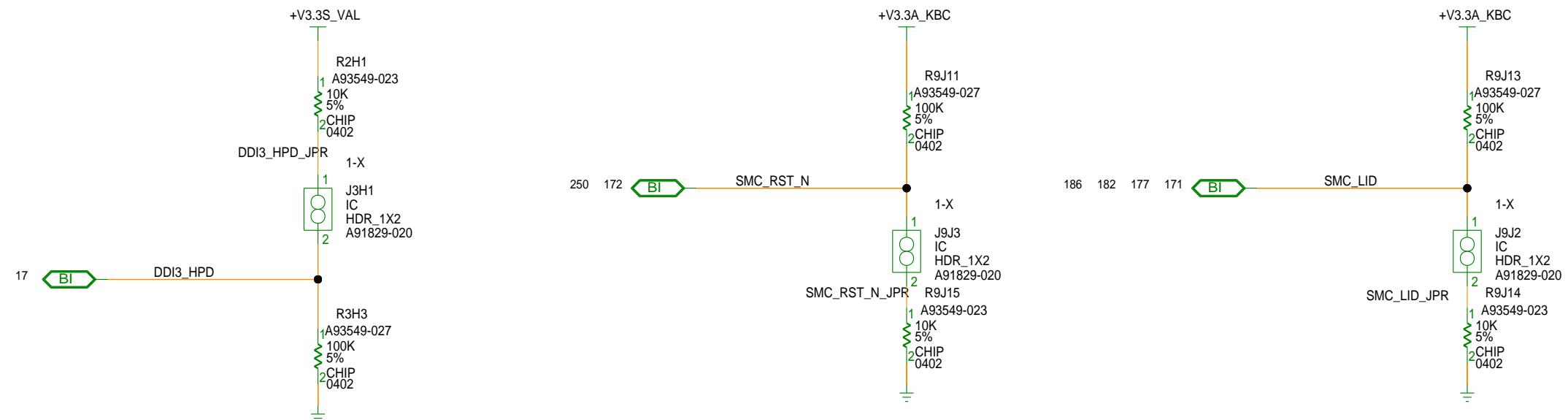
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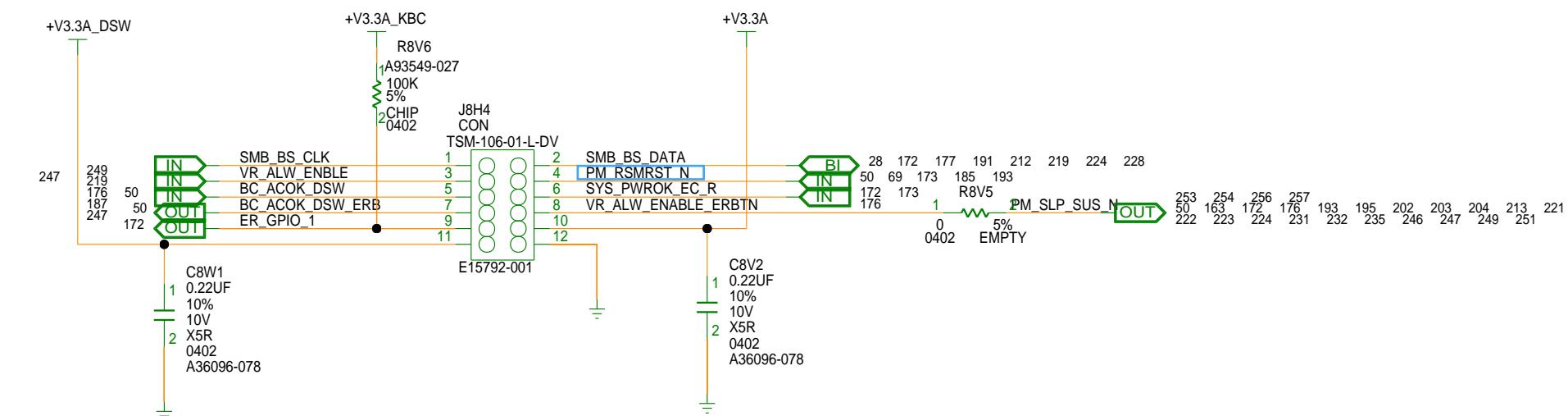


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|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|

## JUMPERS FOR VALIDATION



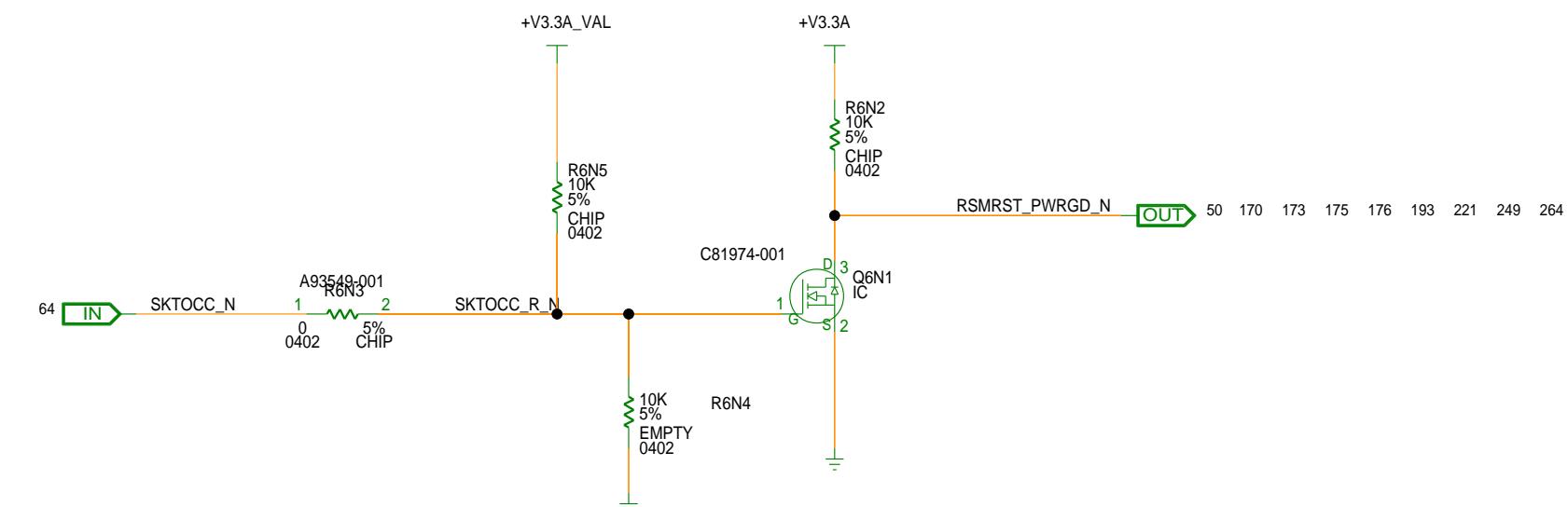
## EYE RIVER VALIDATION HEADER



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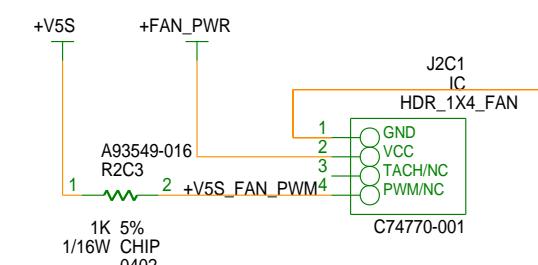
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| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

## SKTOCC\_N -> H\_PRESENT\_N (CPU DETECT,SKTOCC\_N)



CONNECT TO A PROPER VSS PIN OF PCH  
PROCESSOR & PCH PART DETECT

## FAN HEADER



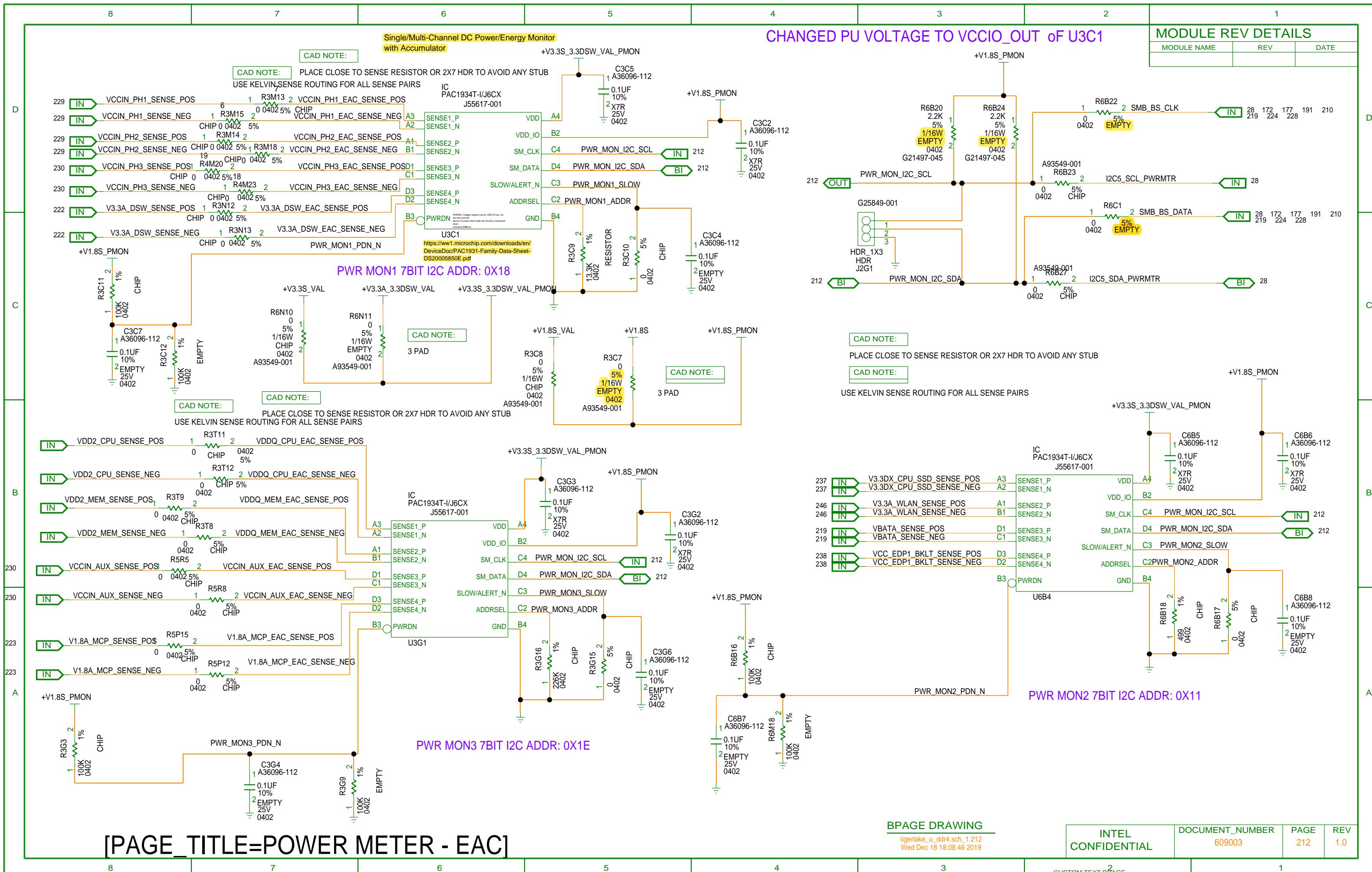
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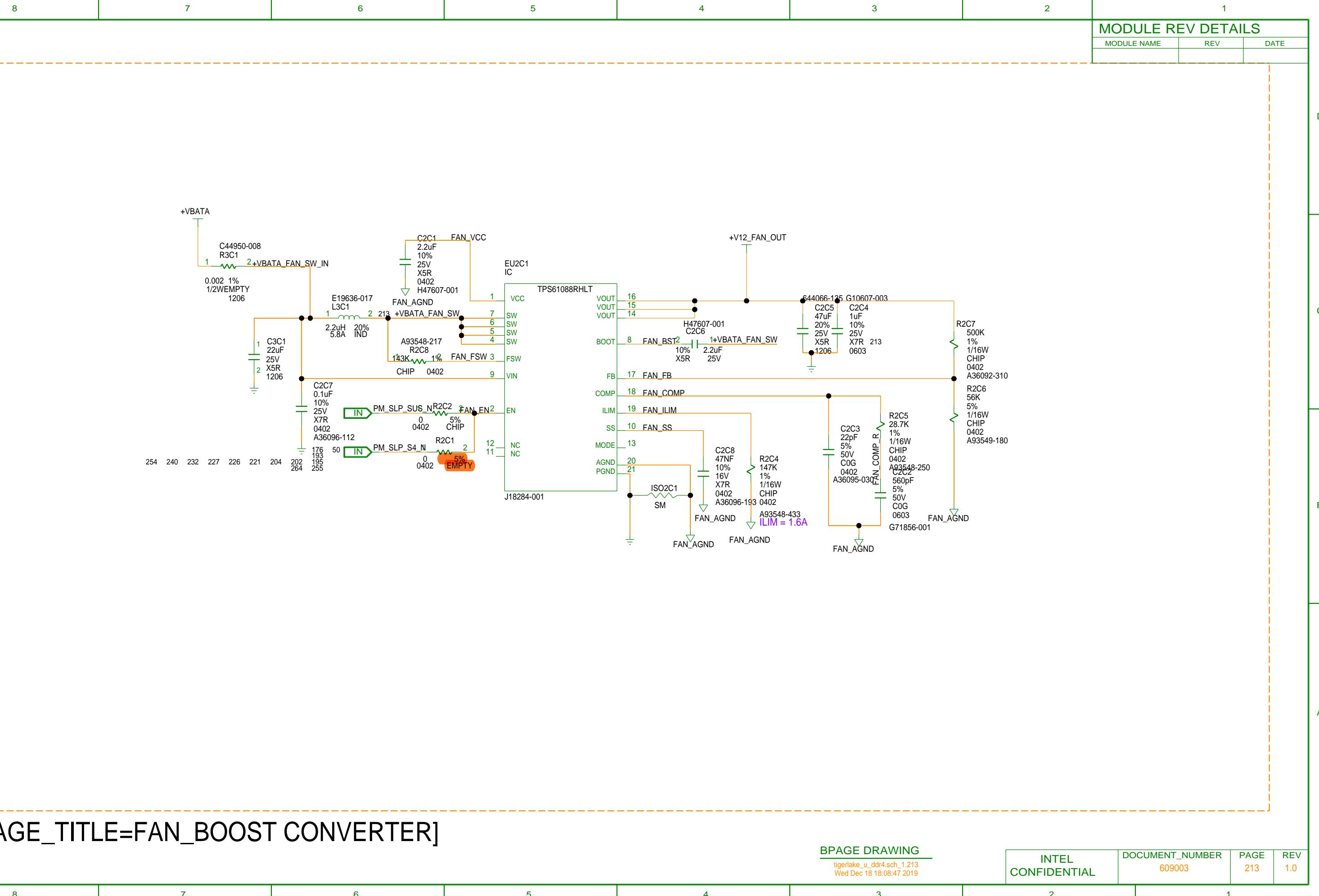
J2A4 FAN CONNECTOR ON & STANDBY(S3)

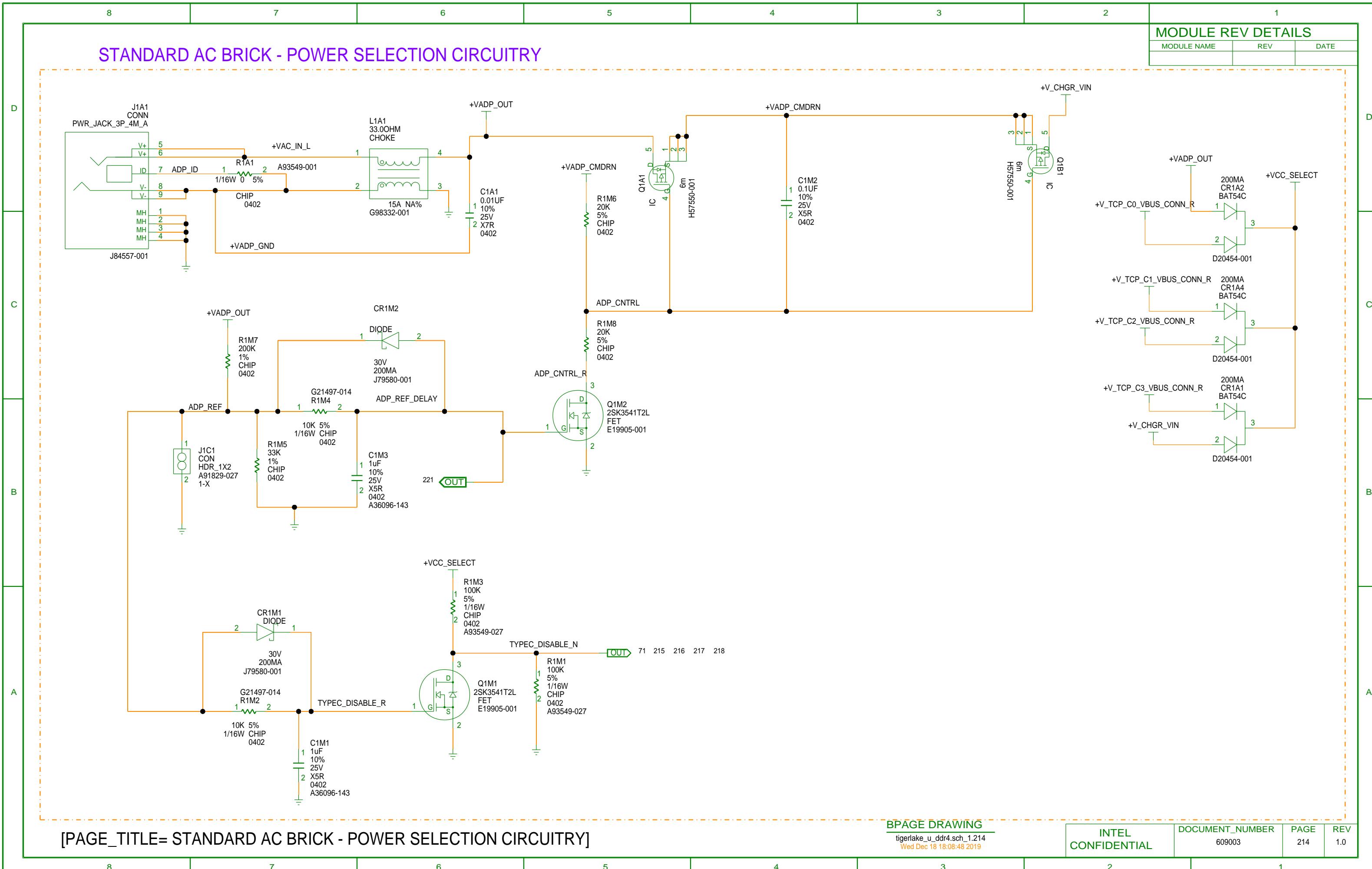
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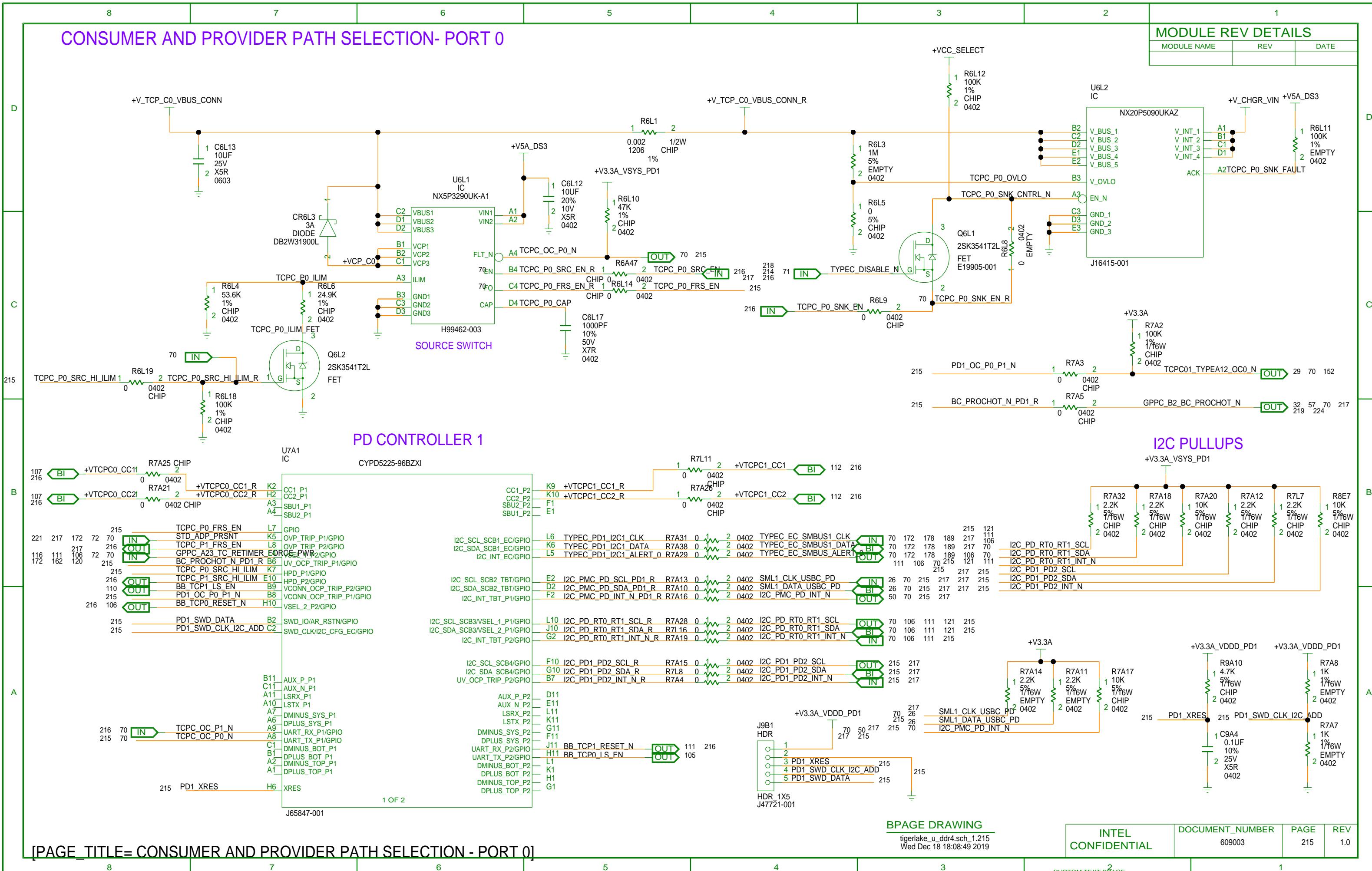
BPAGE DRAWING  
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Wed Dec 18 18:08:45 2019

|                       |                           |             |            |
|-----------------------|---------------------------|-------------|------------|
| INTEL<br>CONFIDENTIAL | DOCUMENT_NUMBER<br>609003 | PAGE<br>211 | REV<br>1.0 |
| CUSTOM TEXT 2 PAGE    |                           |             | 1          |





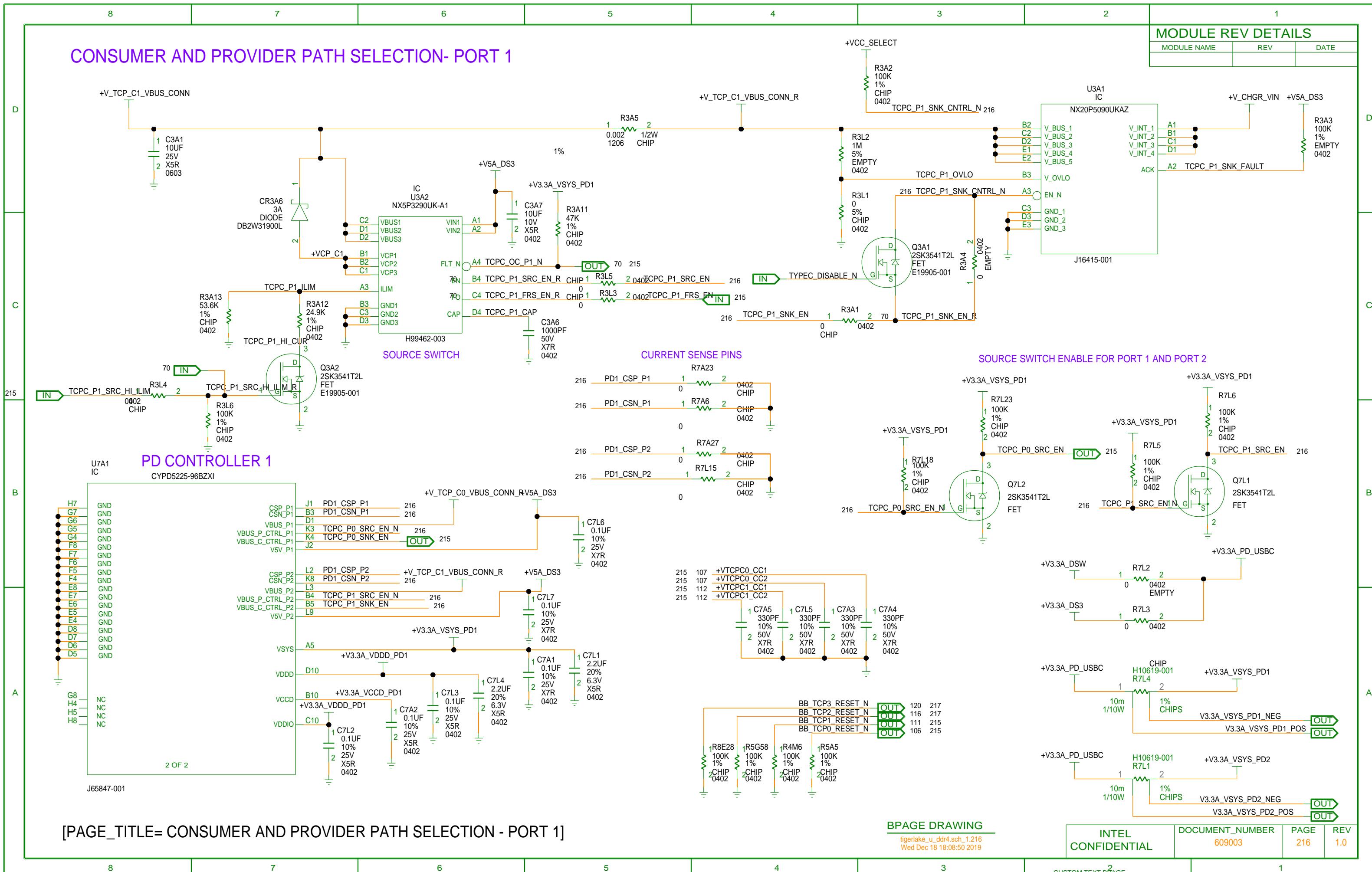


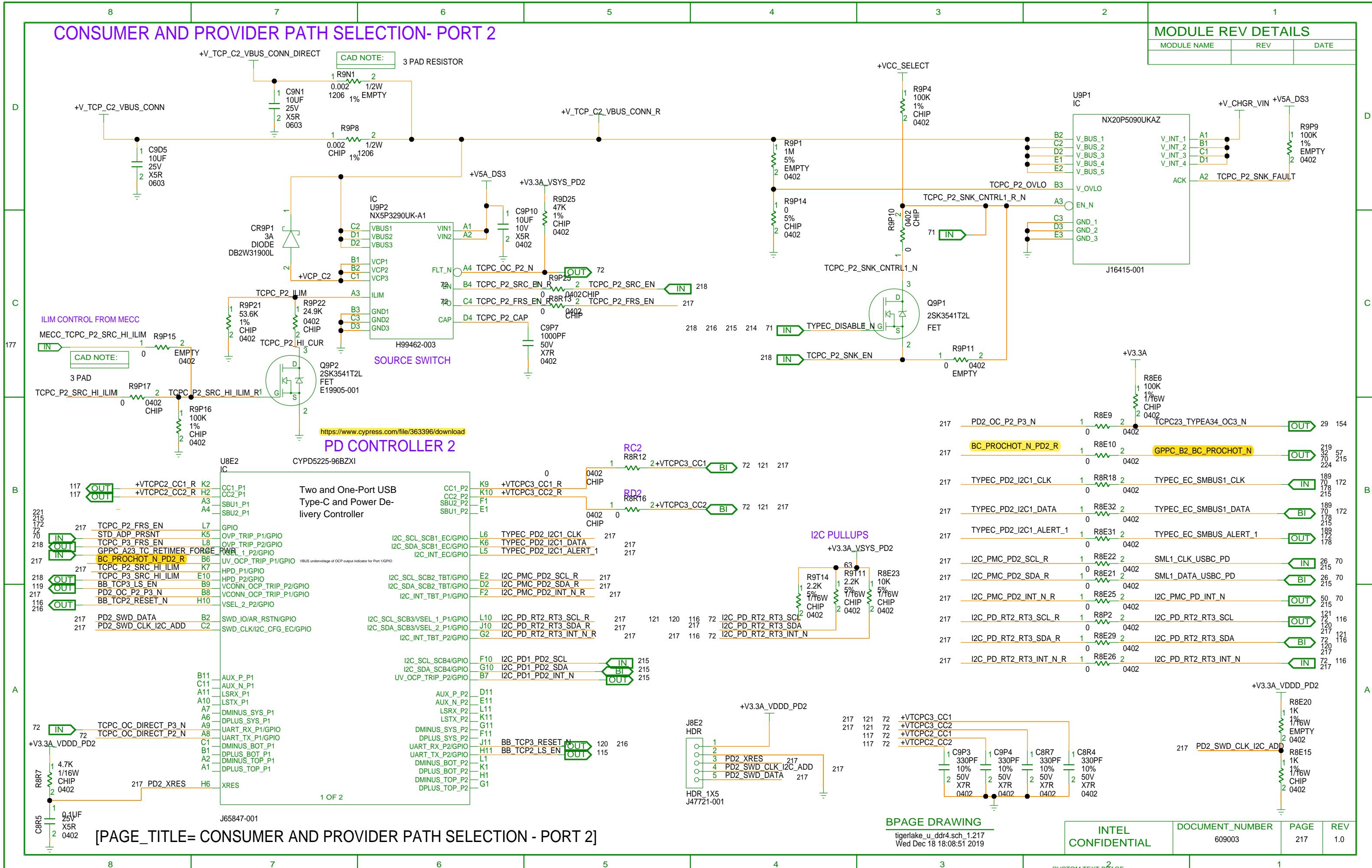


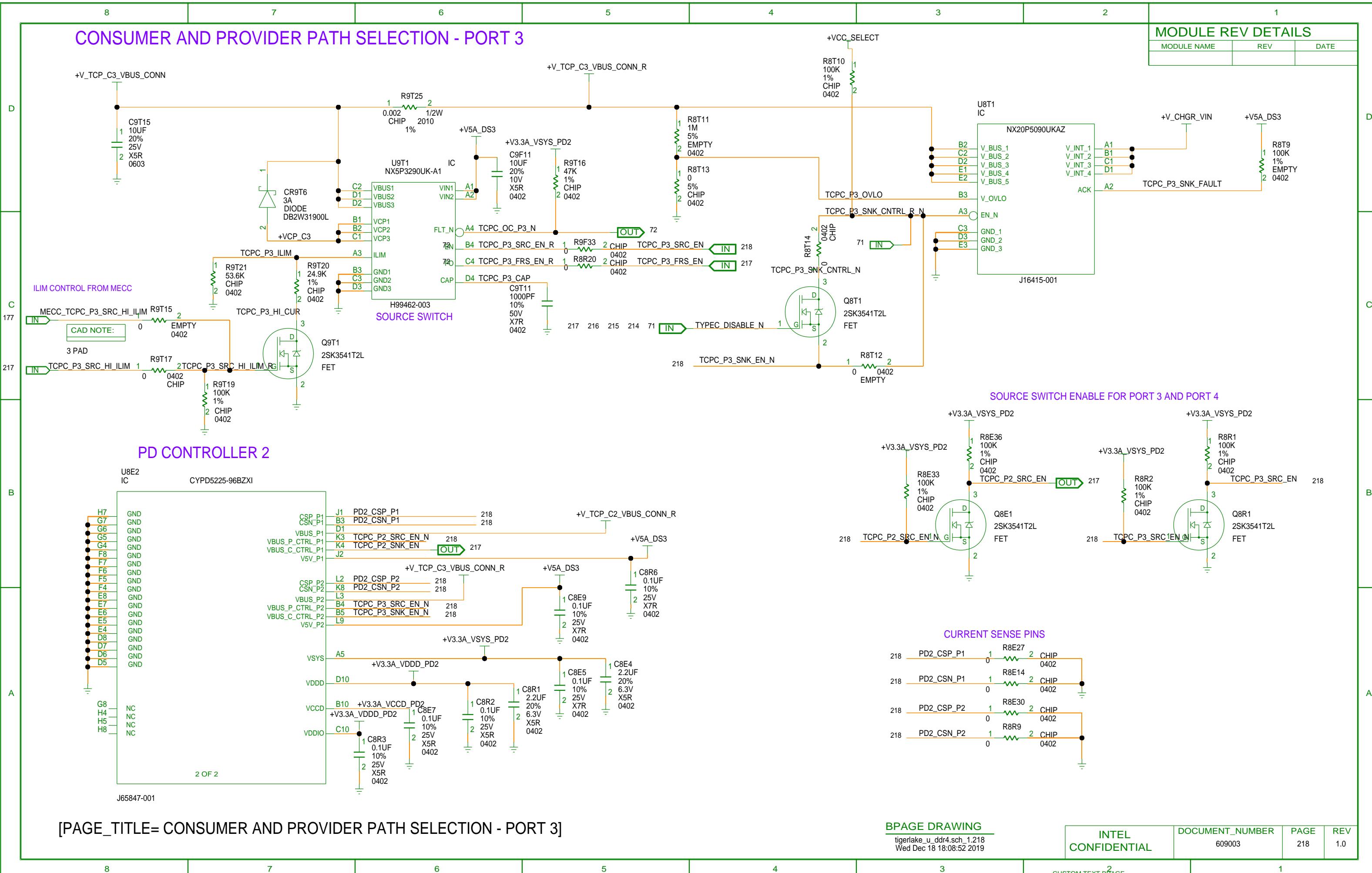
## CONSUMER AND PROVIDER PATH SELECTION- PORT 1

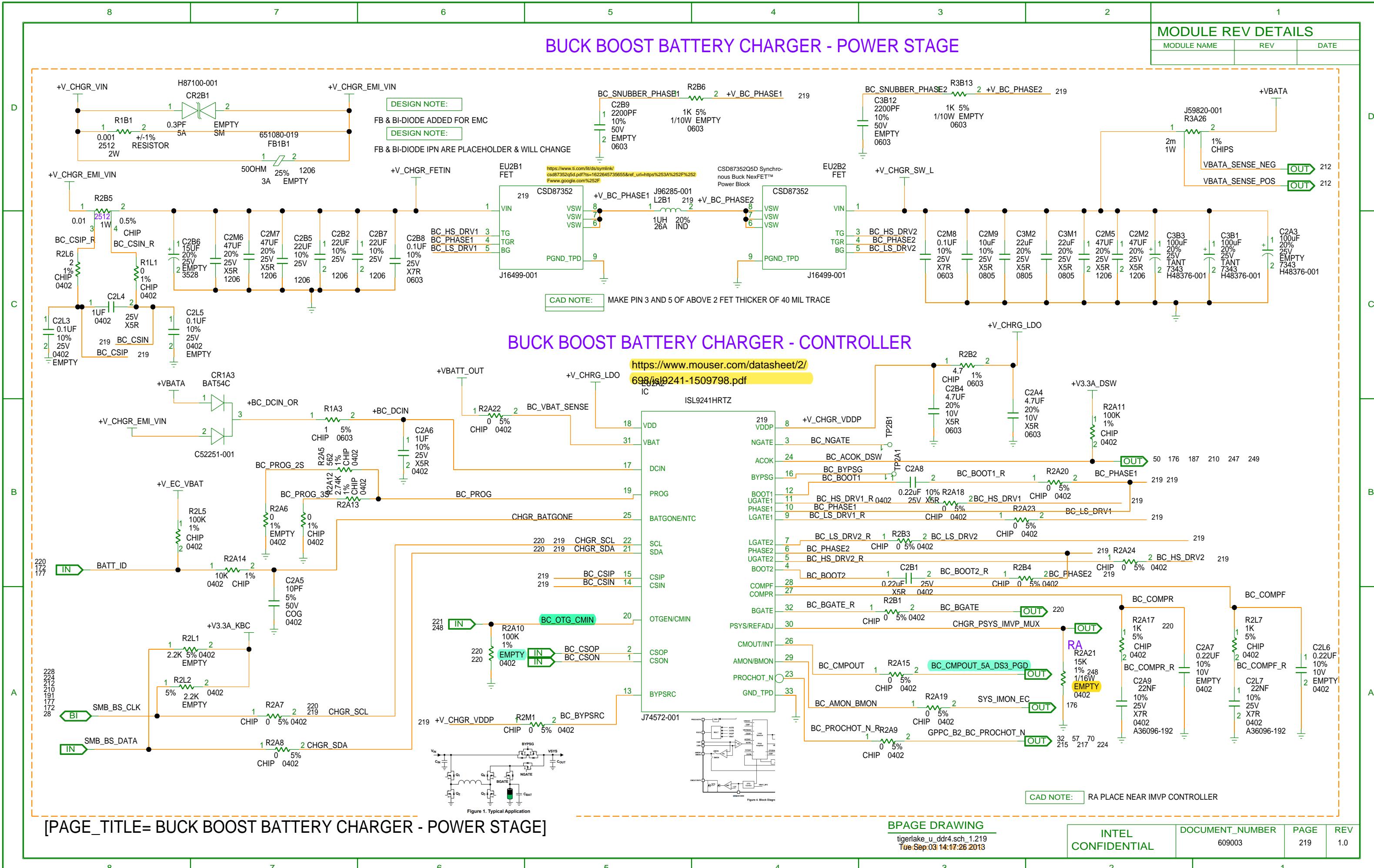
## MODULE REV DETAILS

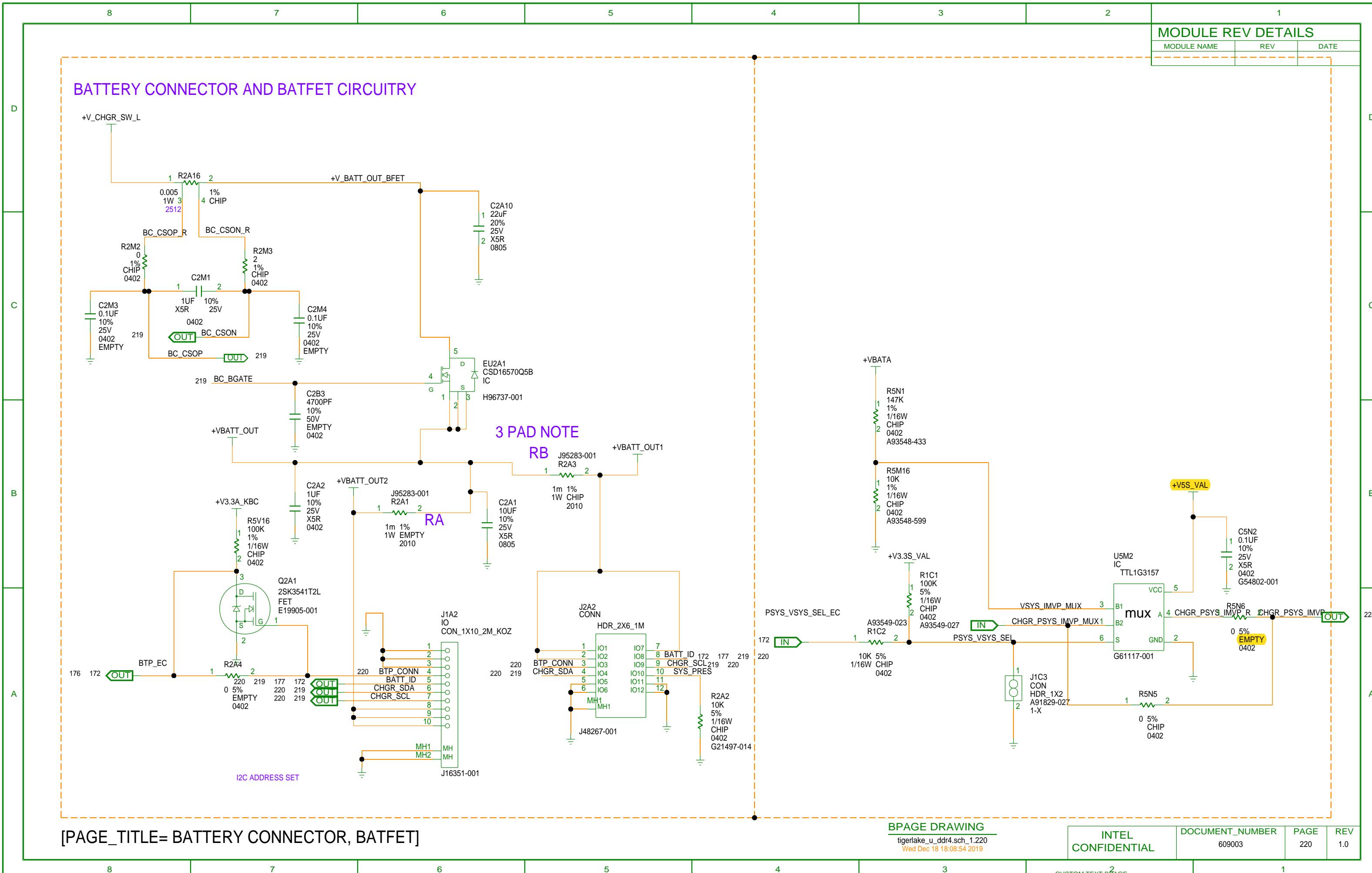
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|-------------|-----|------|
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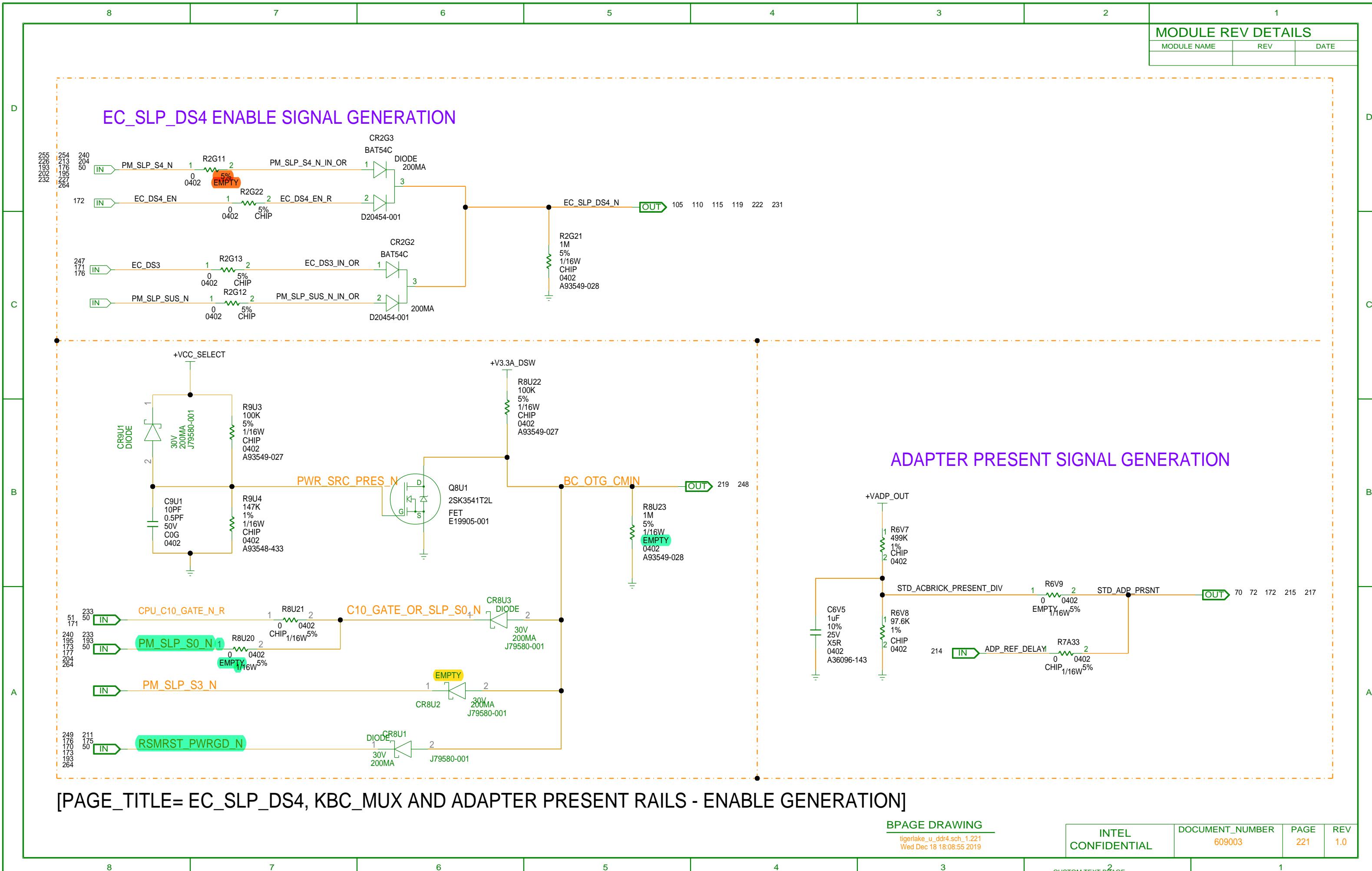


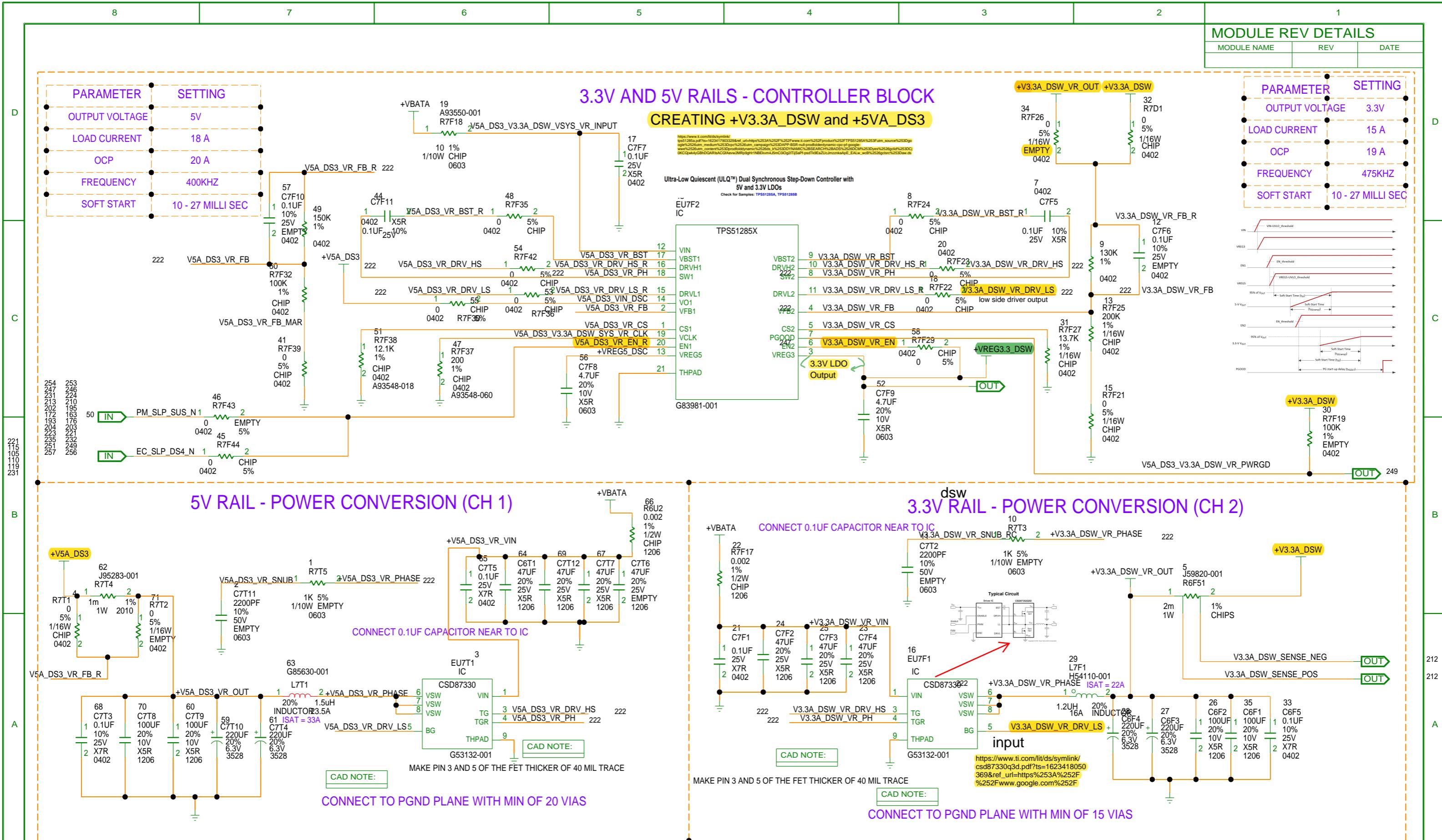












[PAGE TITLE= 3.3V AND 5V RAILS - POWER CONVERSION]

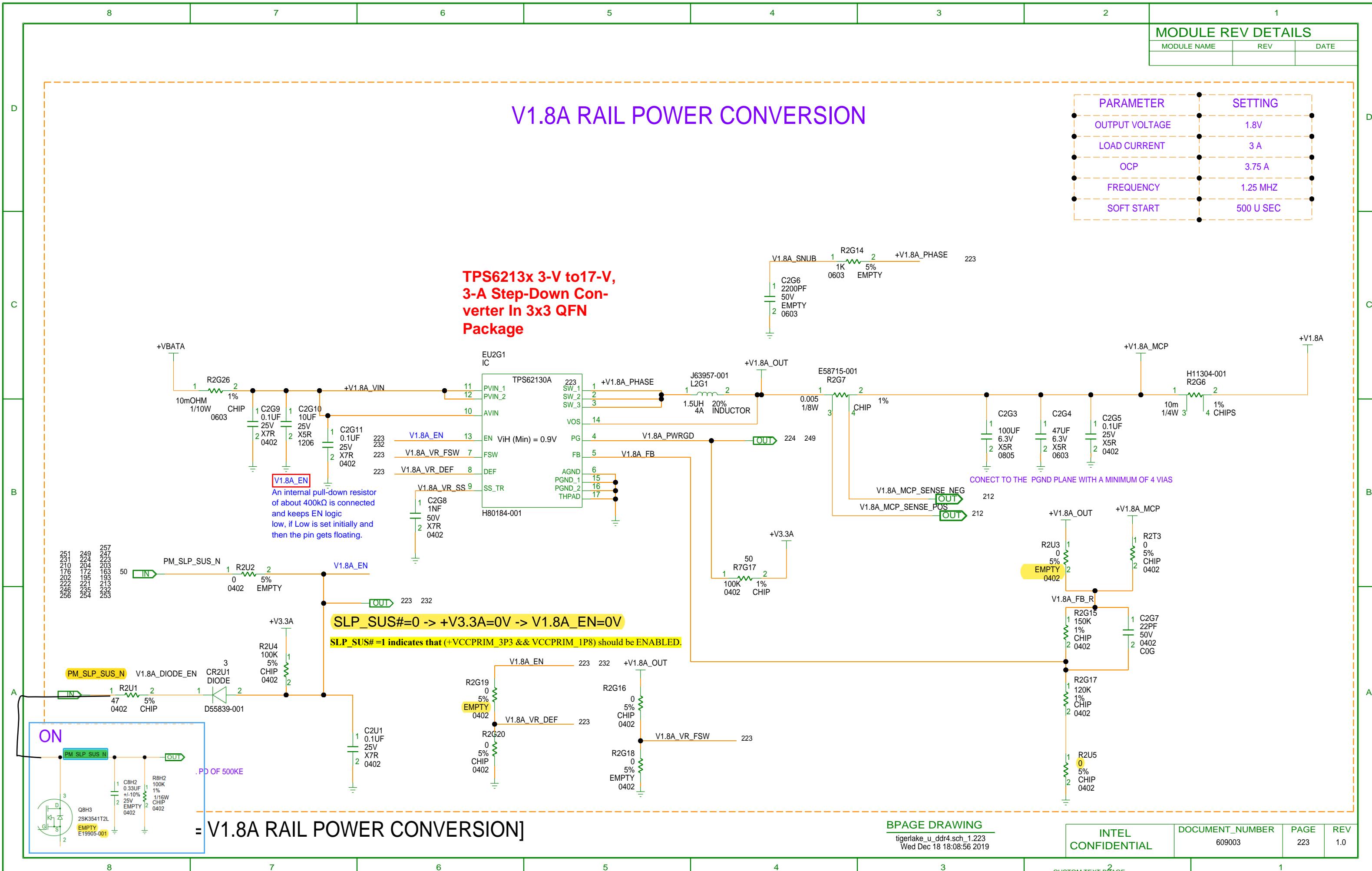
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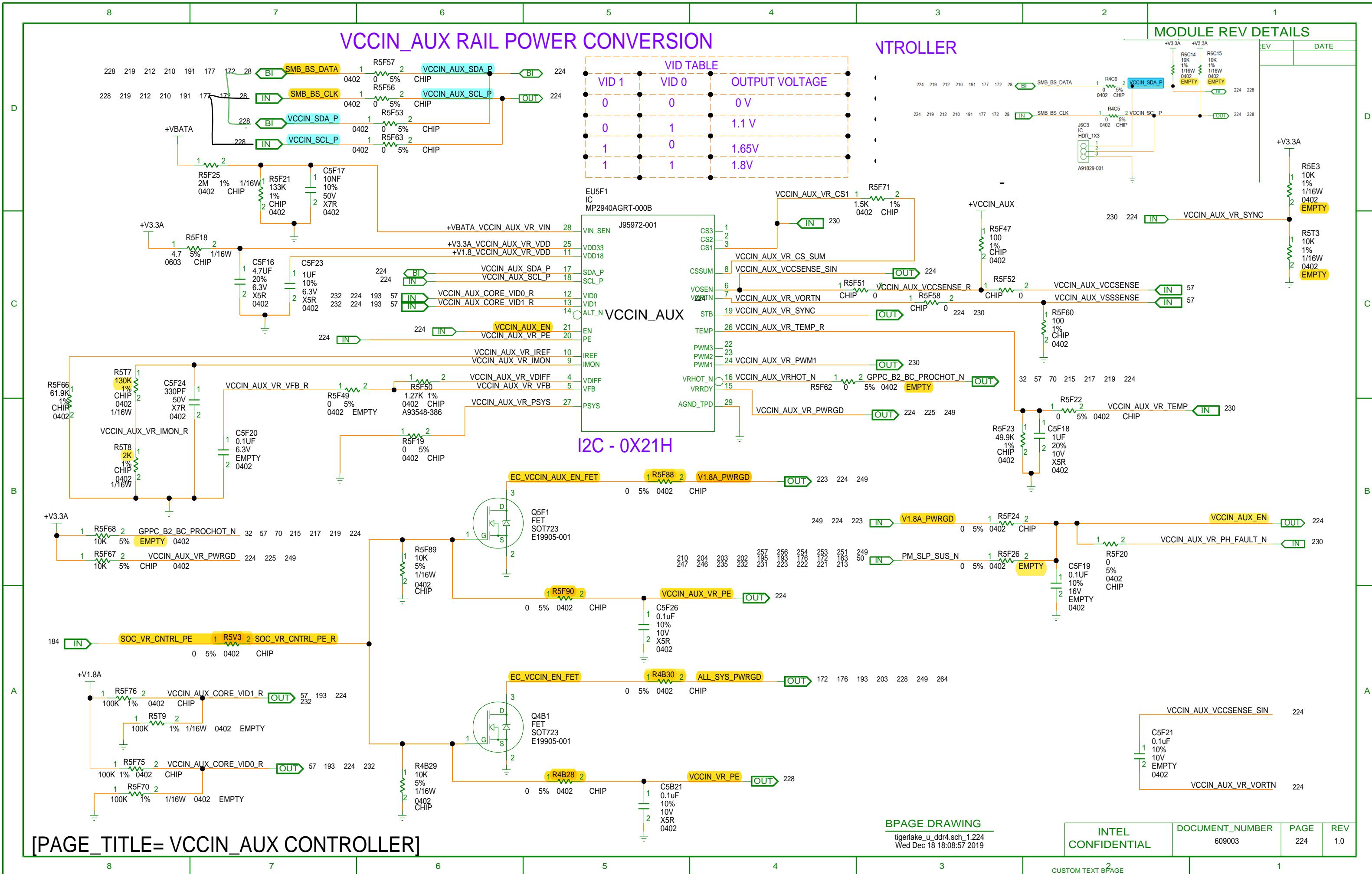
INTEL  
CONFIDENTIAL

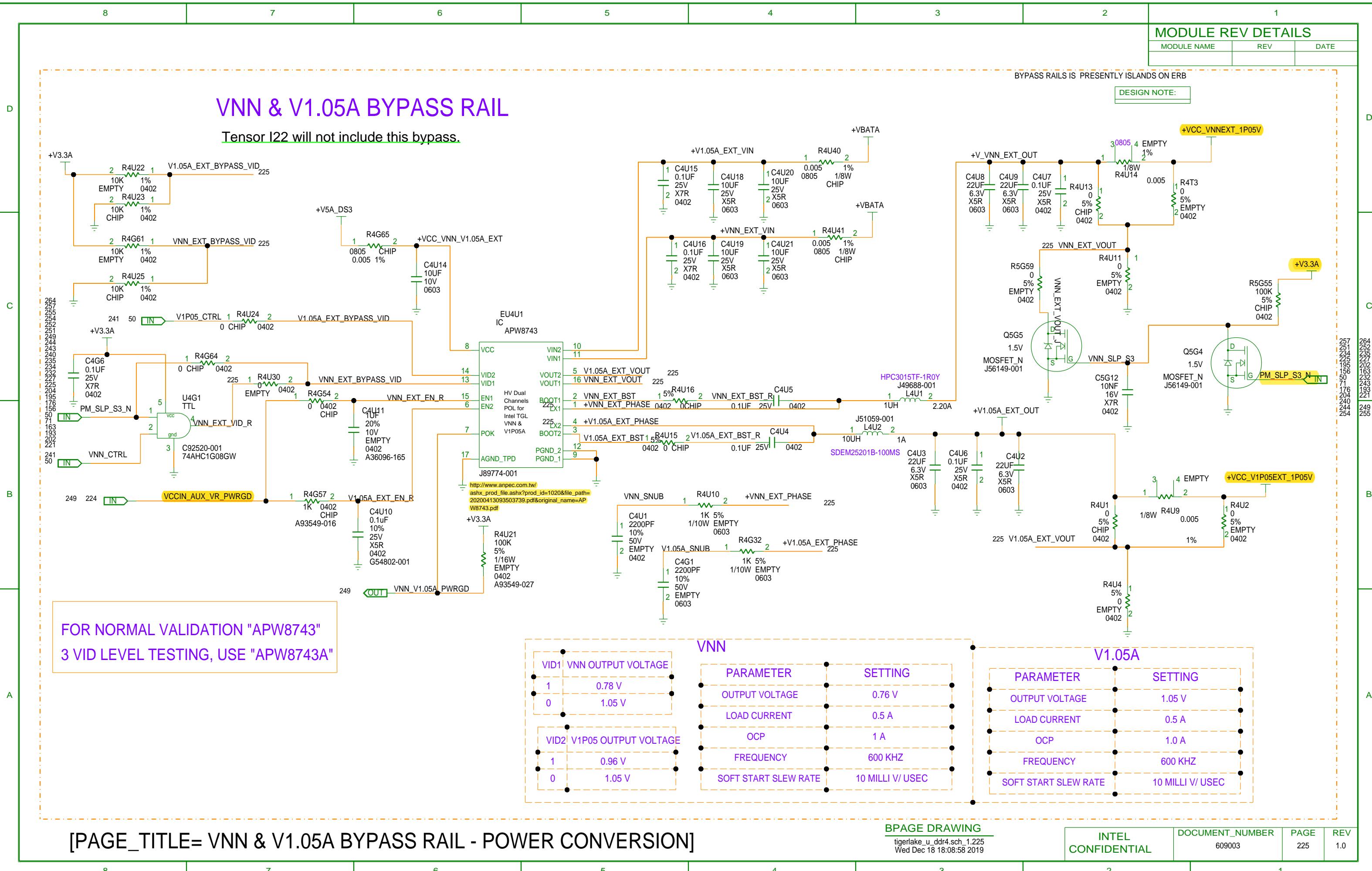
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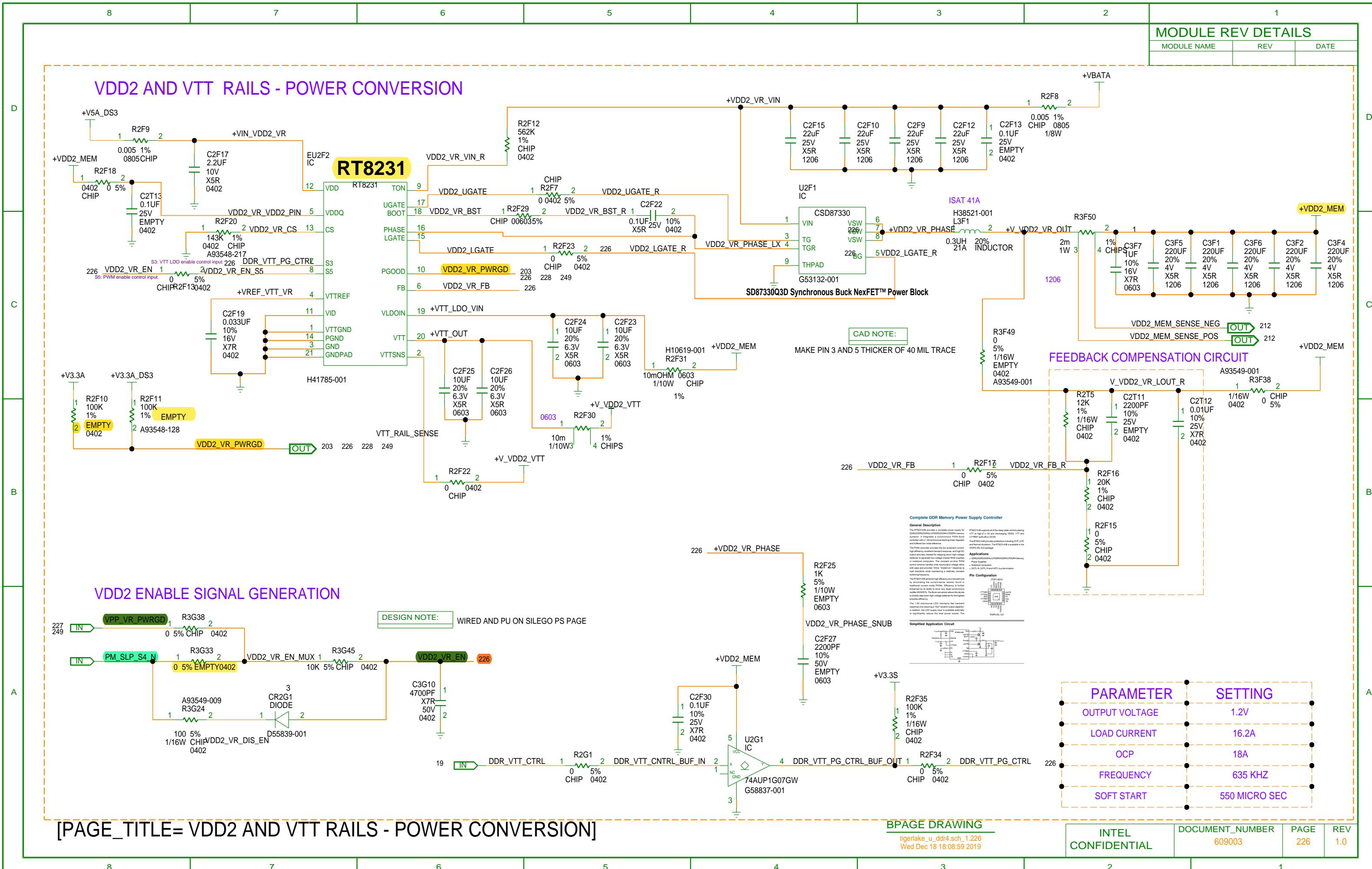
PAGE REV  
222 1.0

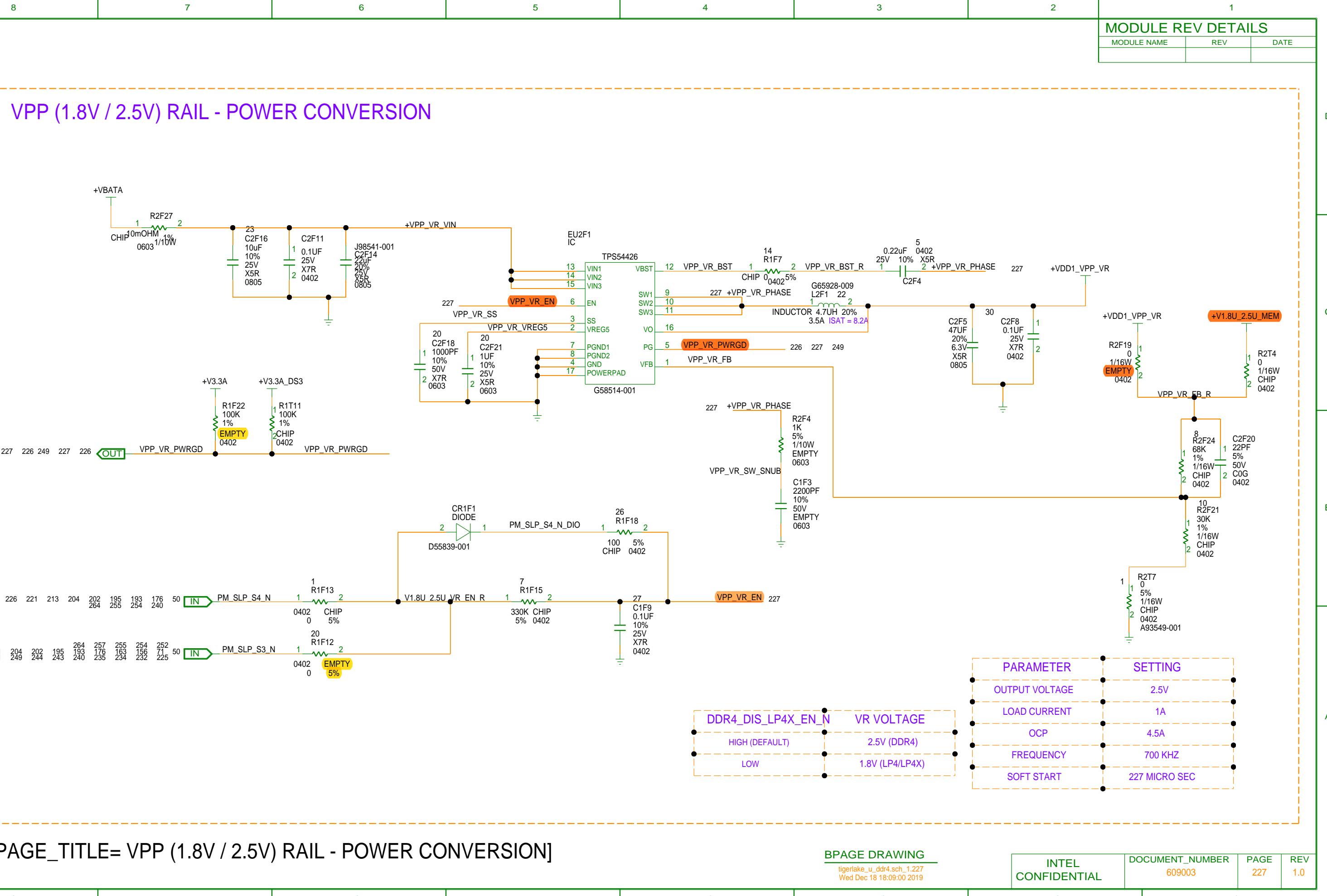
CUSTOM TEXT B PAGE 2

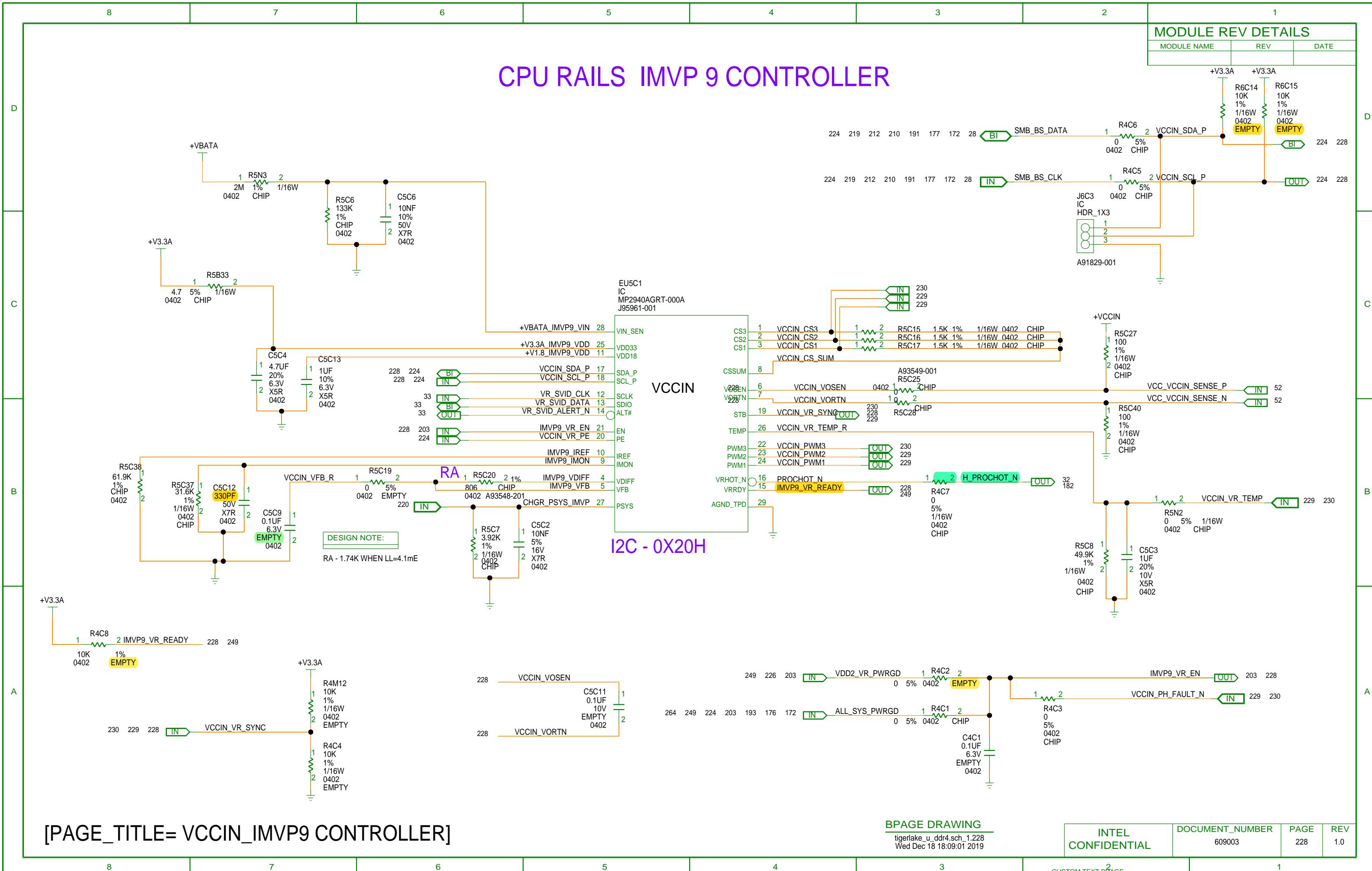


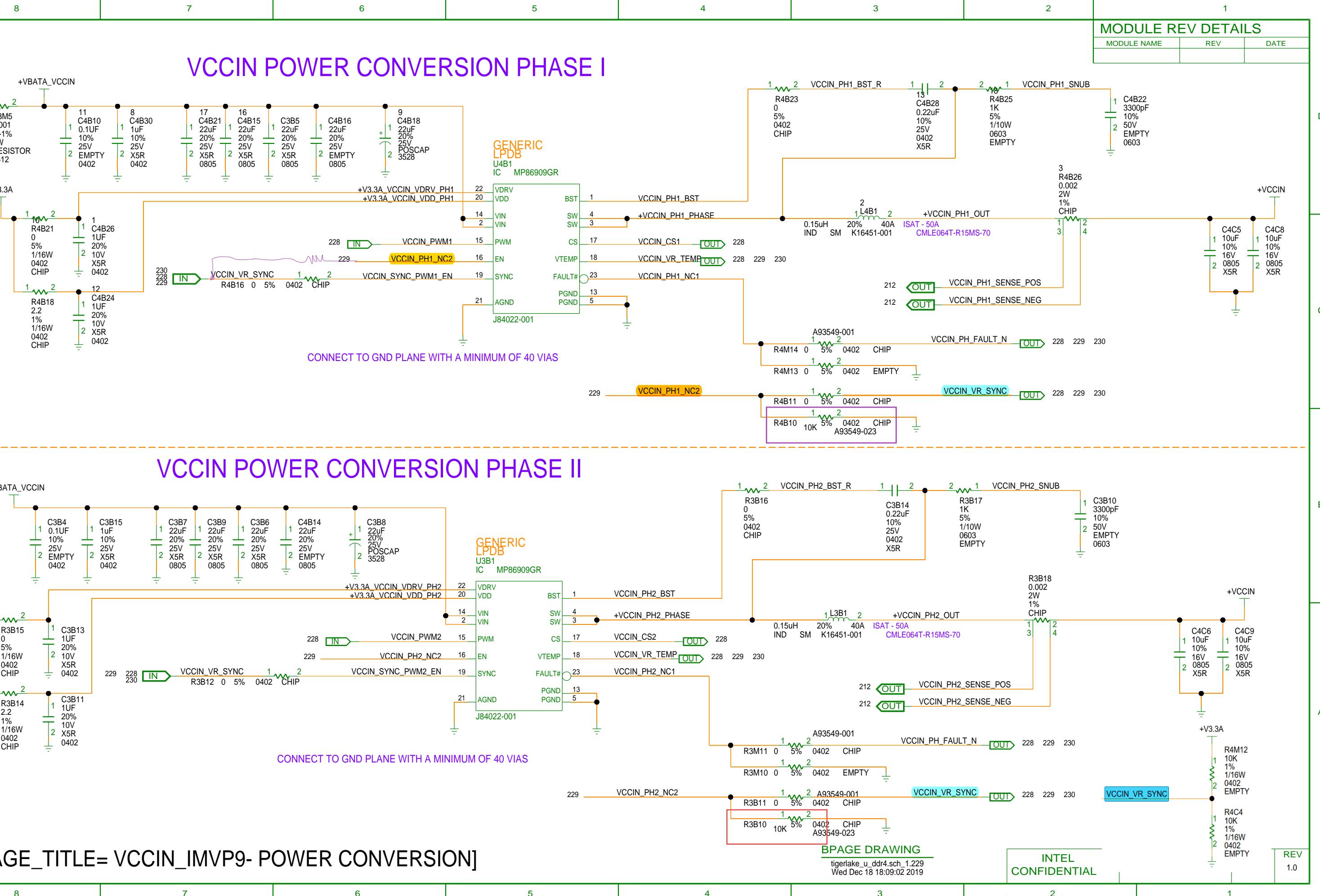








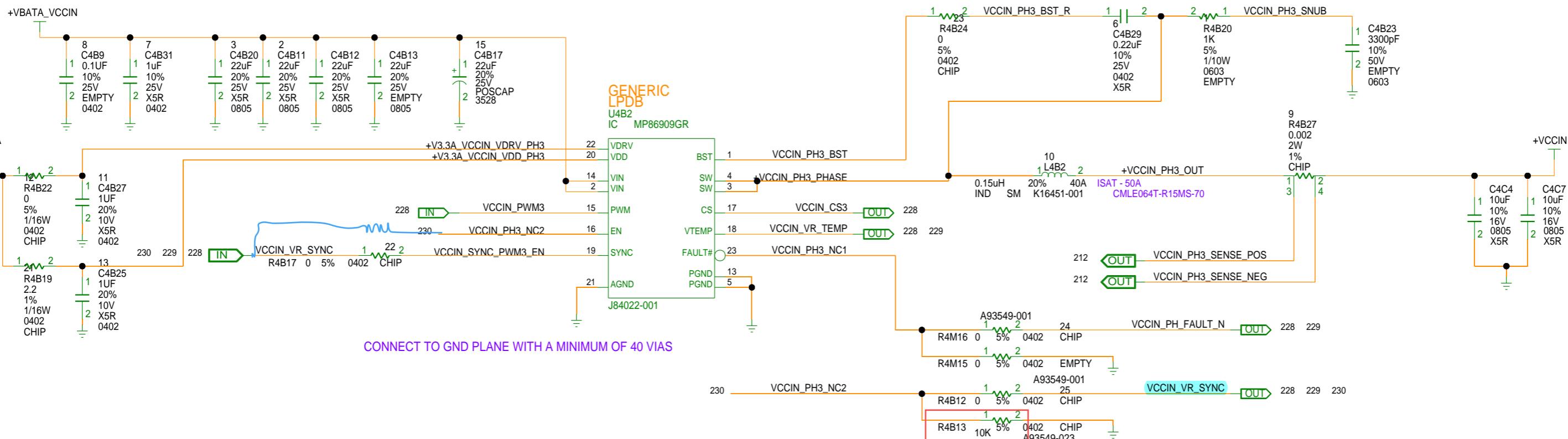




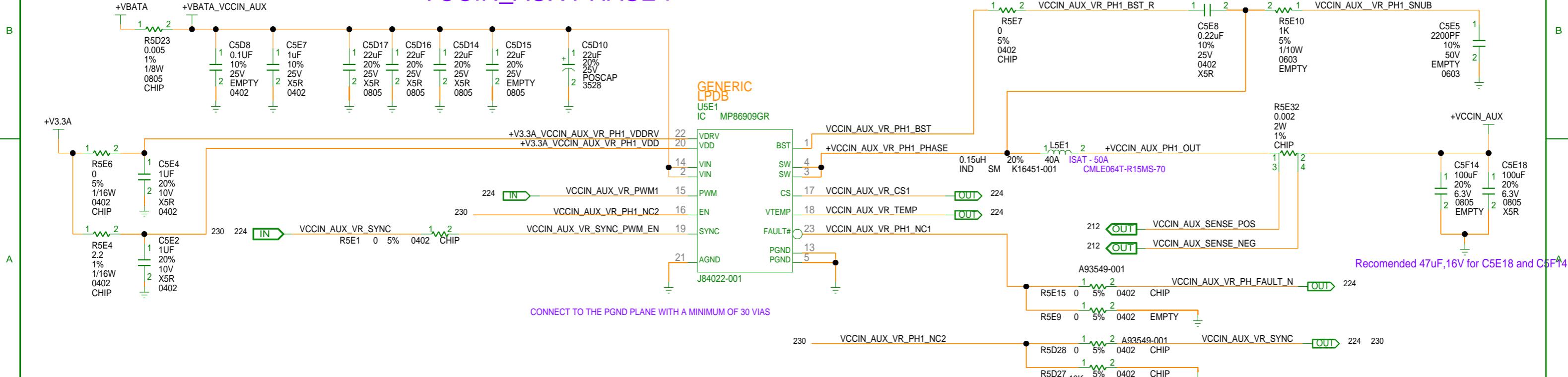
## VCCIN POWER CONVERSION PHASE III

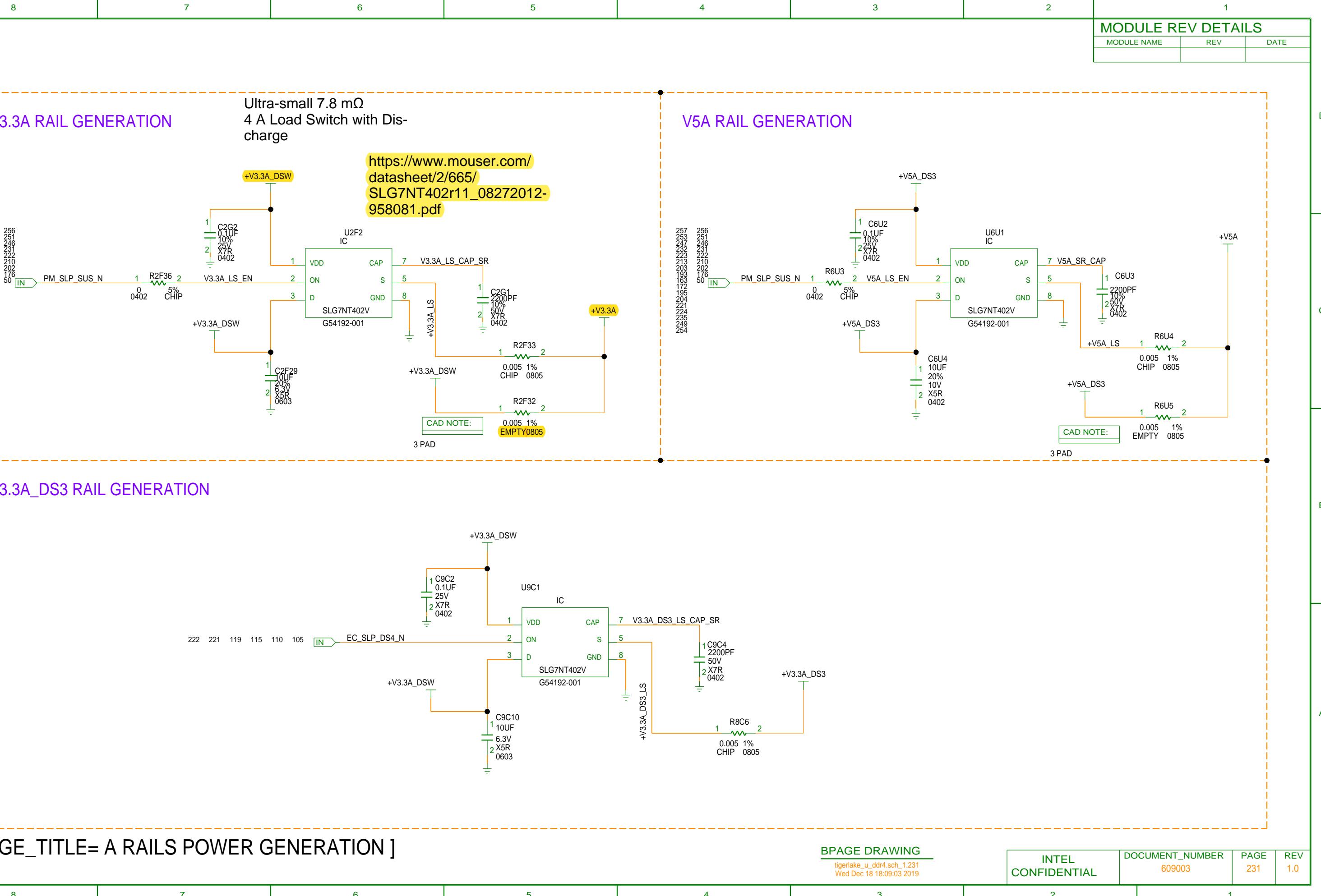
### MODULE REV DETAILS

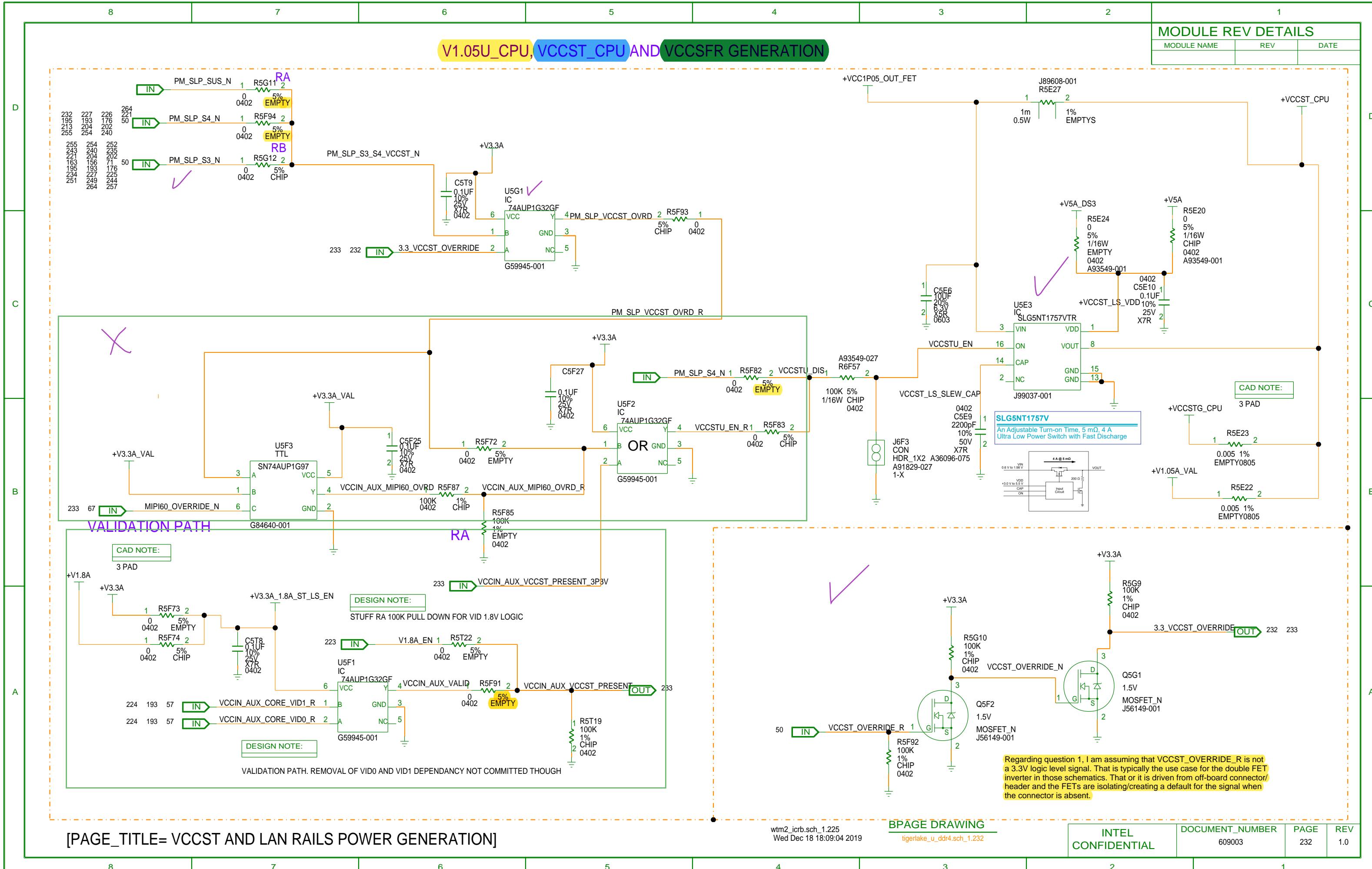
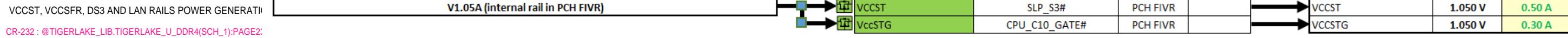
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|-------------|-----|------|
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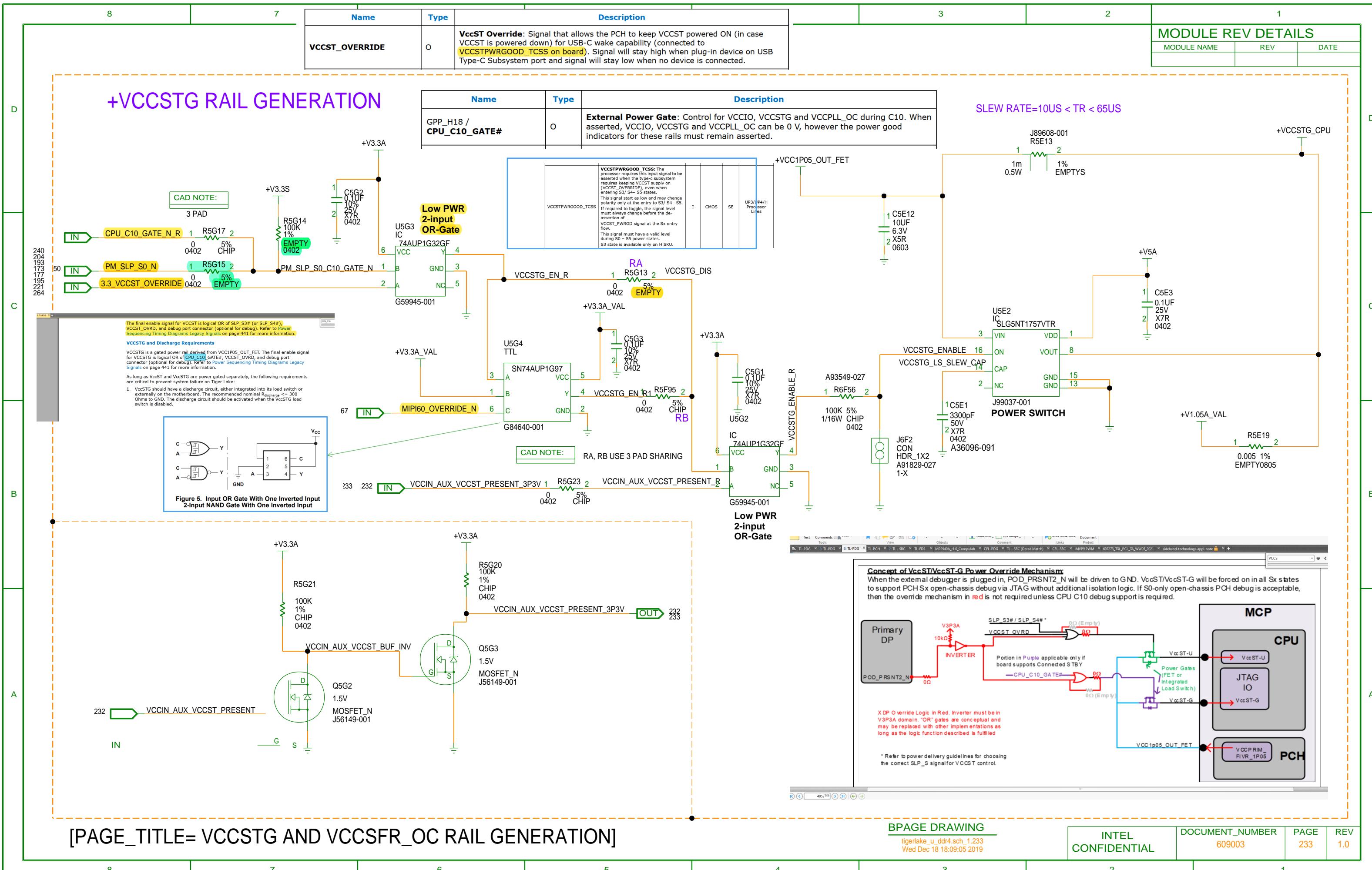


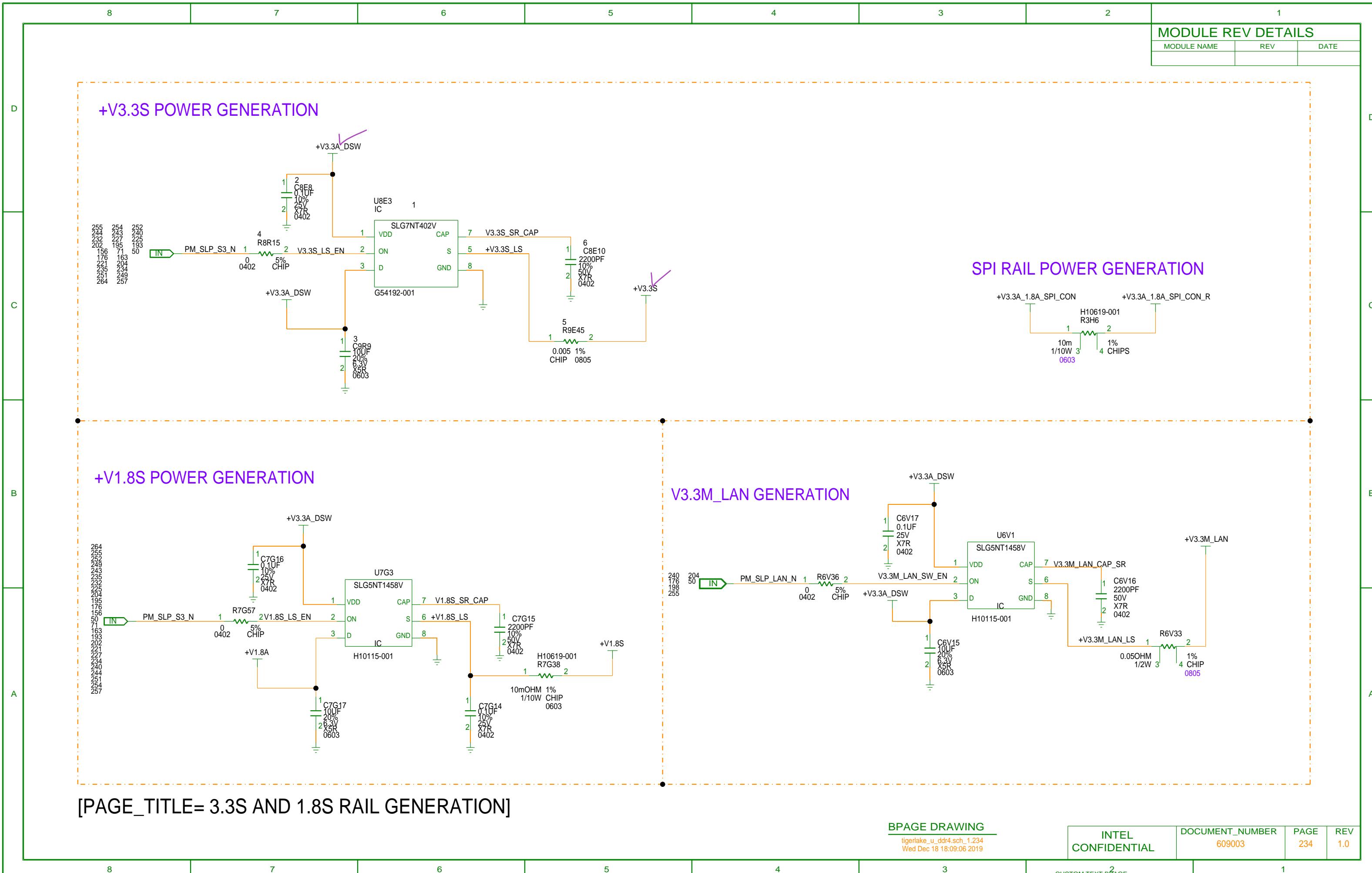
## VCCIN\_AUX PHASE I







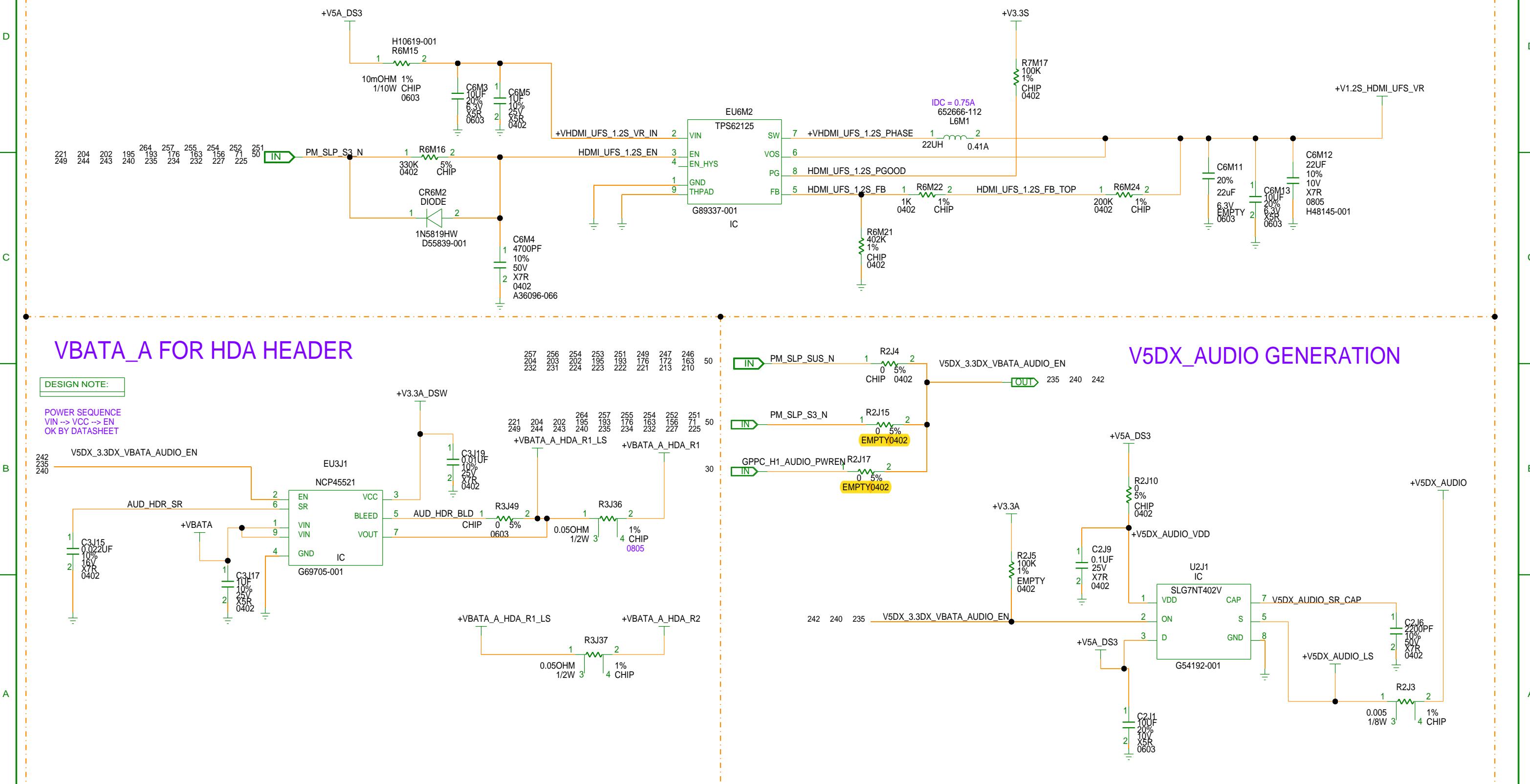




## 1.2V RAIL FOR HDMI AND UFS - POWER CONVERSION

## MODULE REV DETAILS

| MODULE NAME | REV | DATE |
|-------------|-----|------|
|             |     |      |



[PAGE\_TITLE= 1.2V RAIL FOR HDMI AND UFS, VBATA\_A FOR HDA AND AUDIO POWER GENERATION]

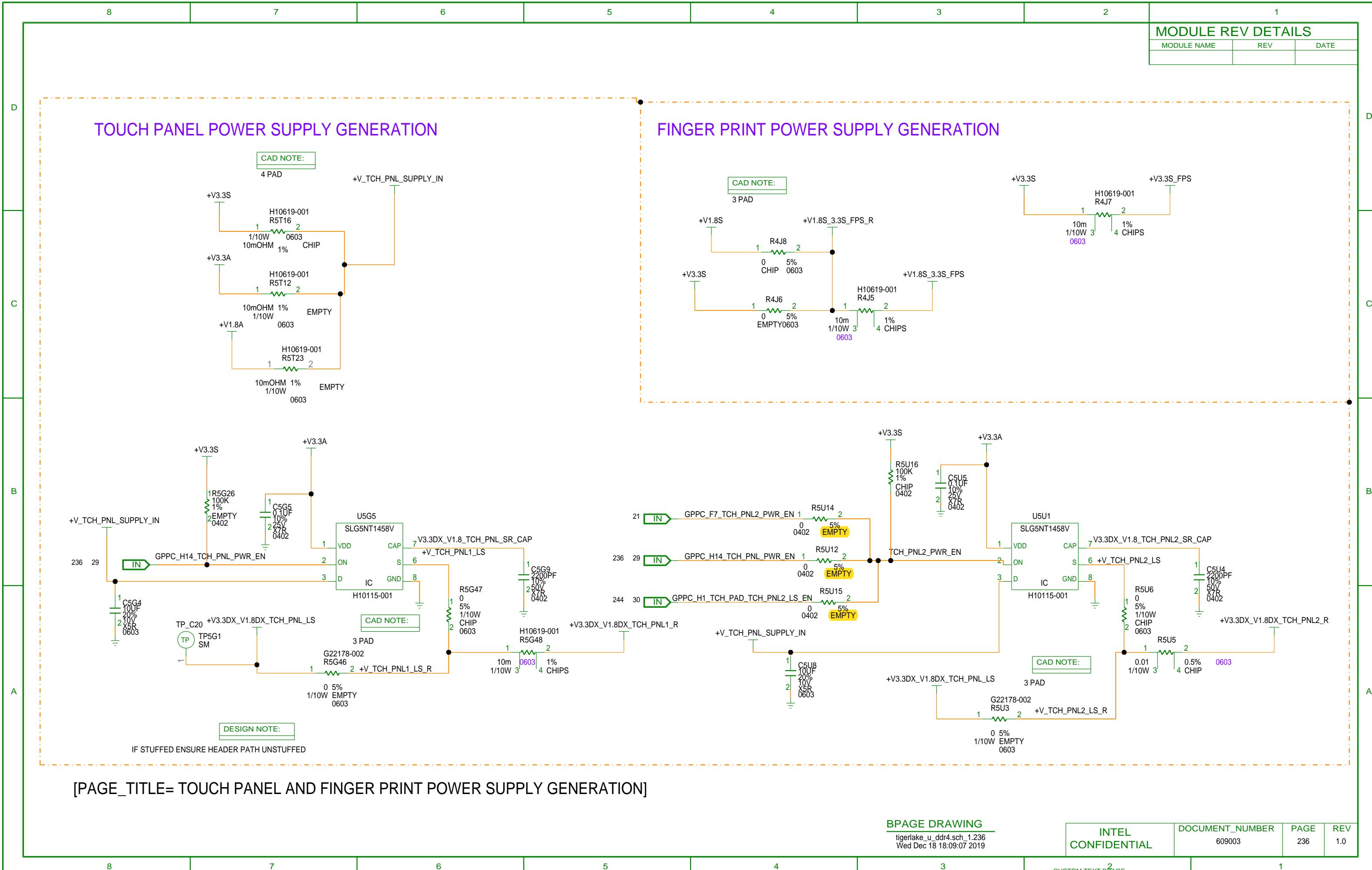
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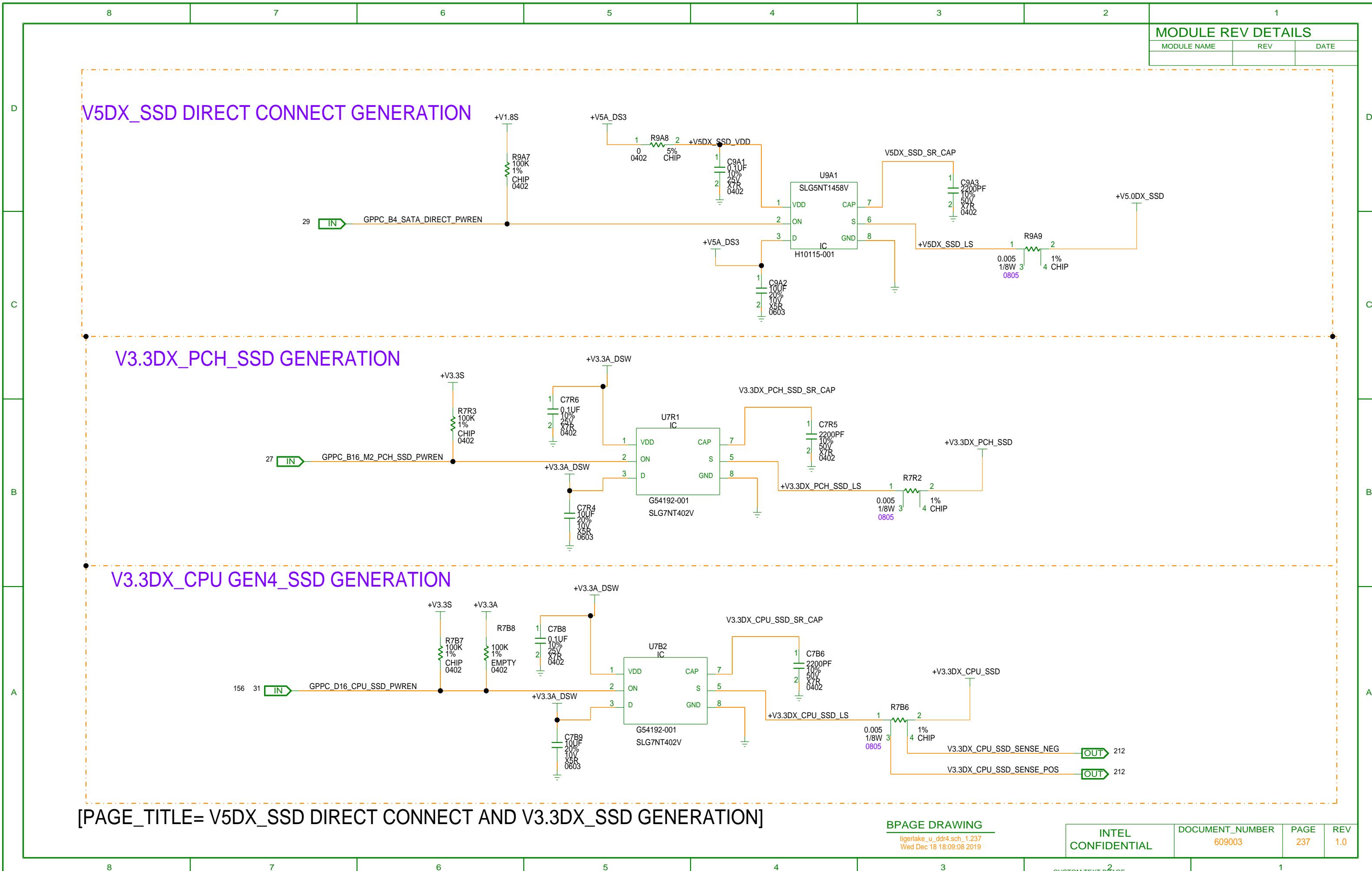
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Wed Dec 18 18:09:07 2019

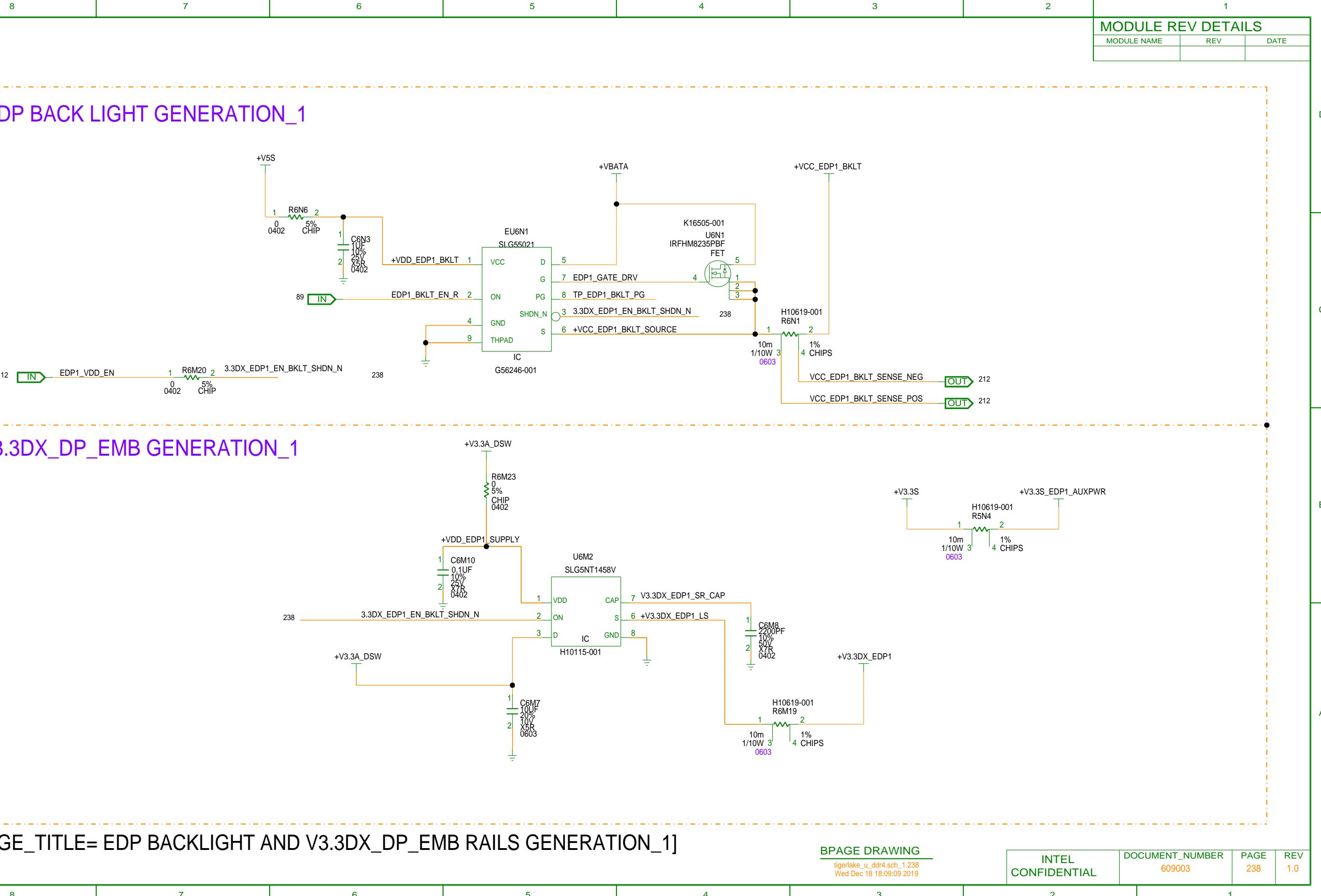
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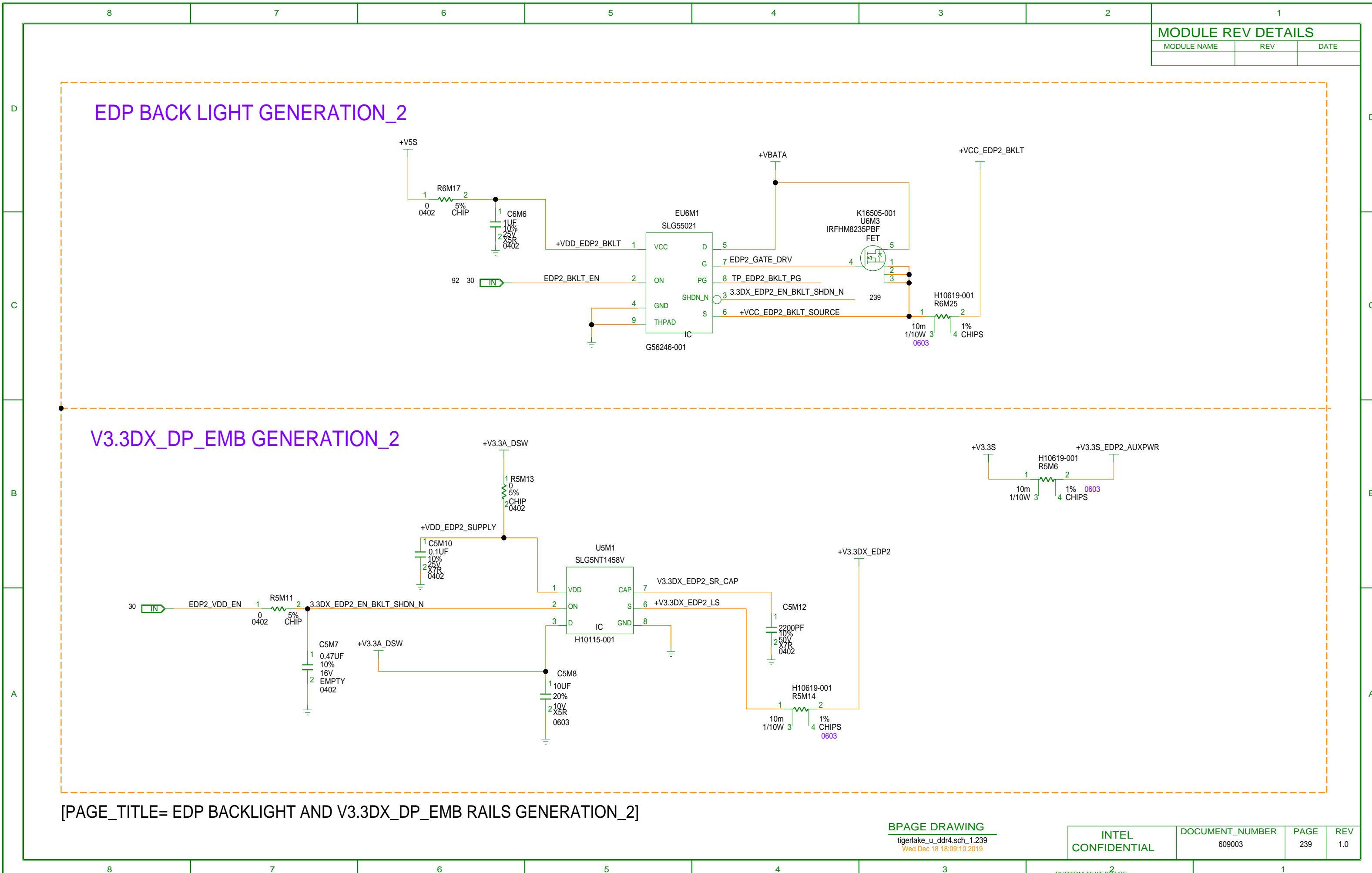
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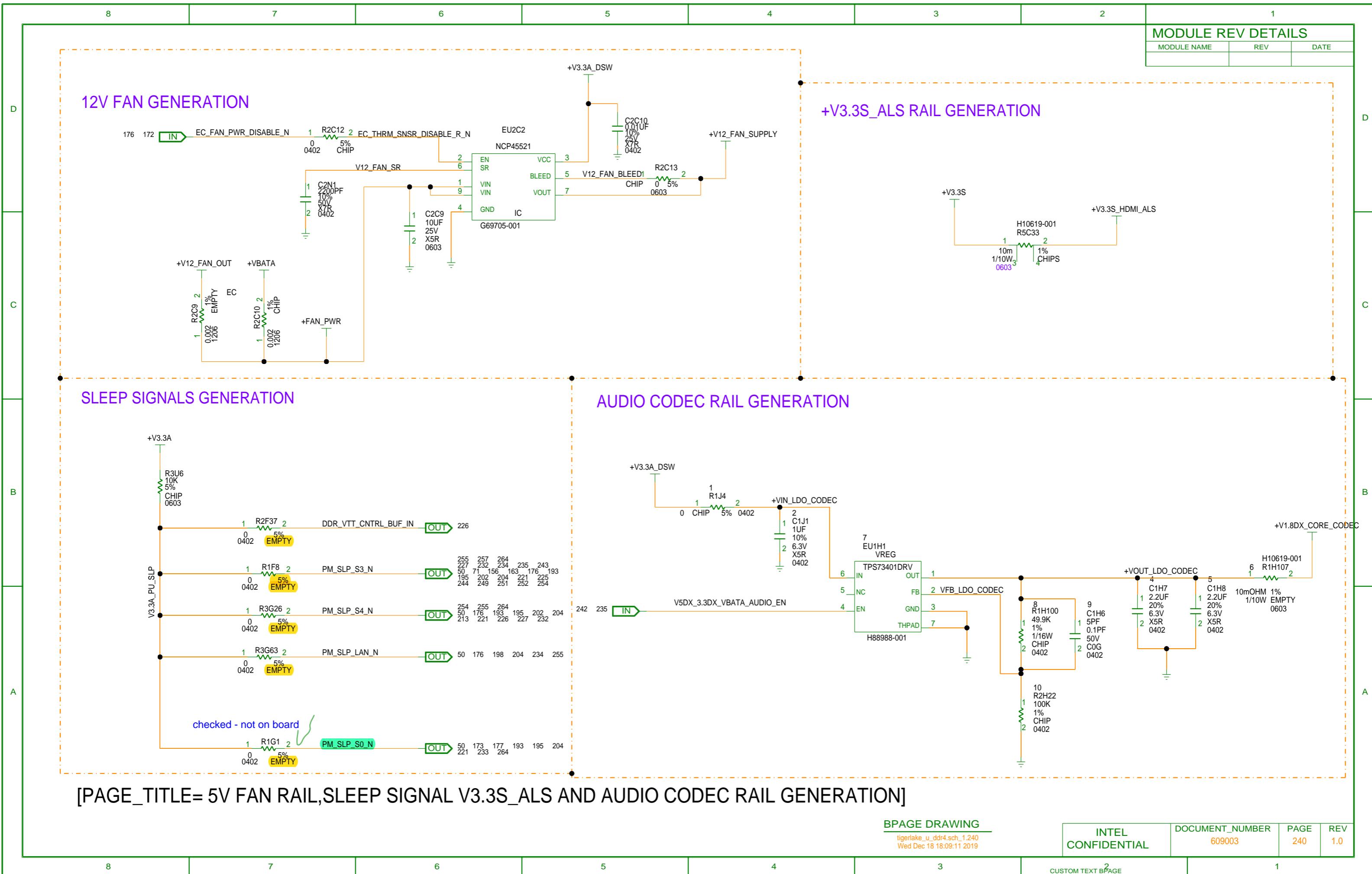
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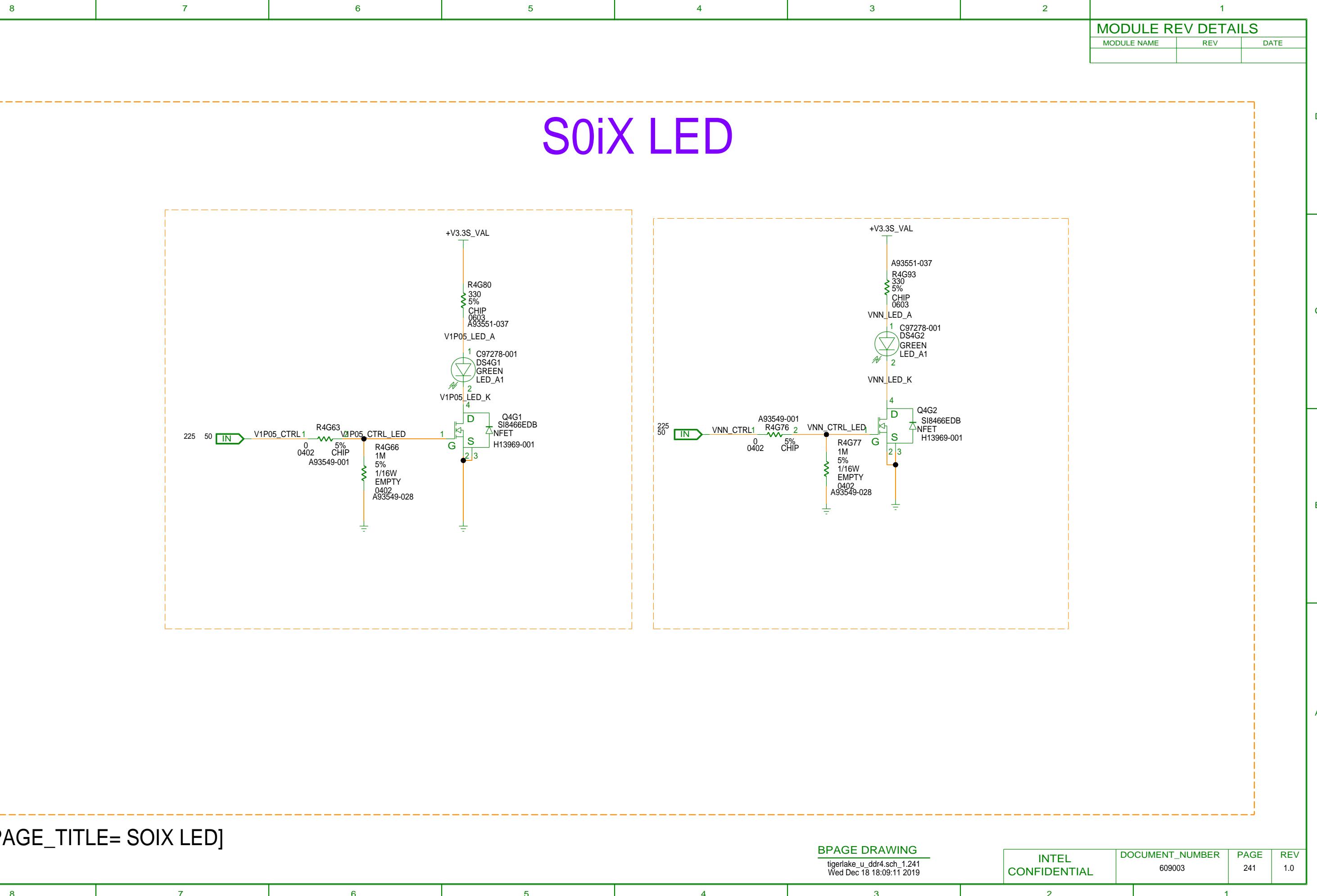


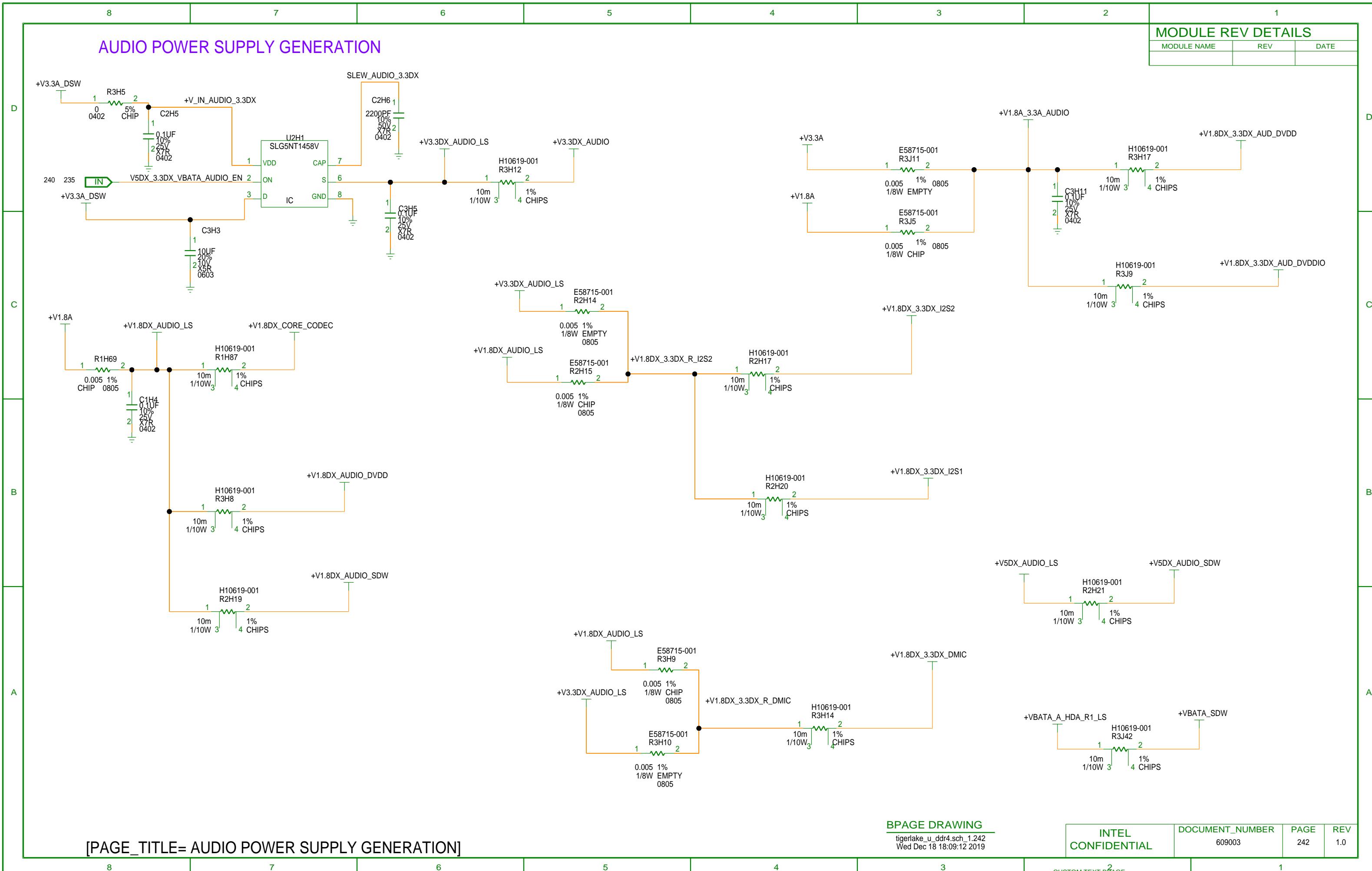


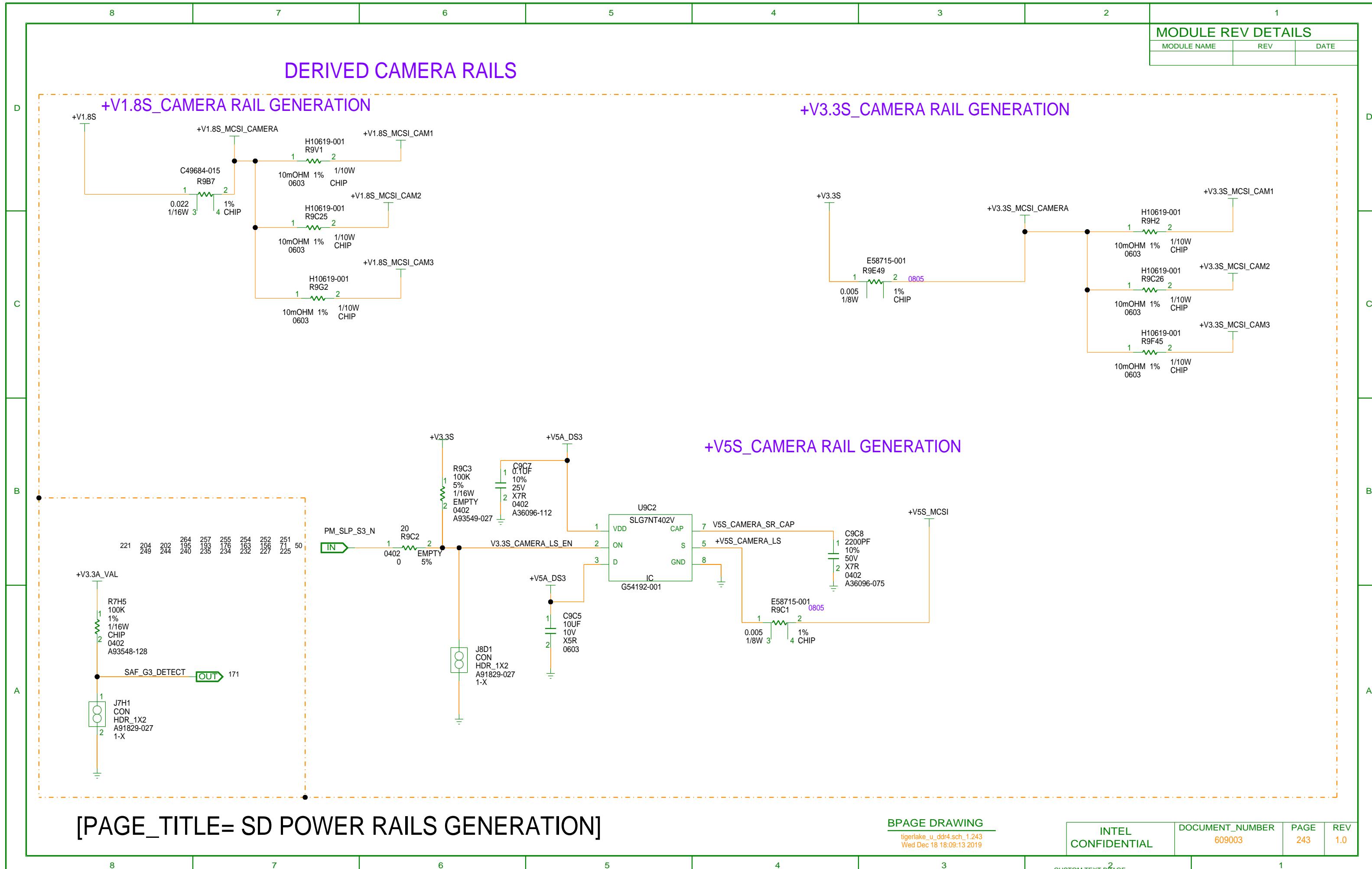


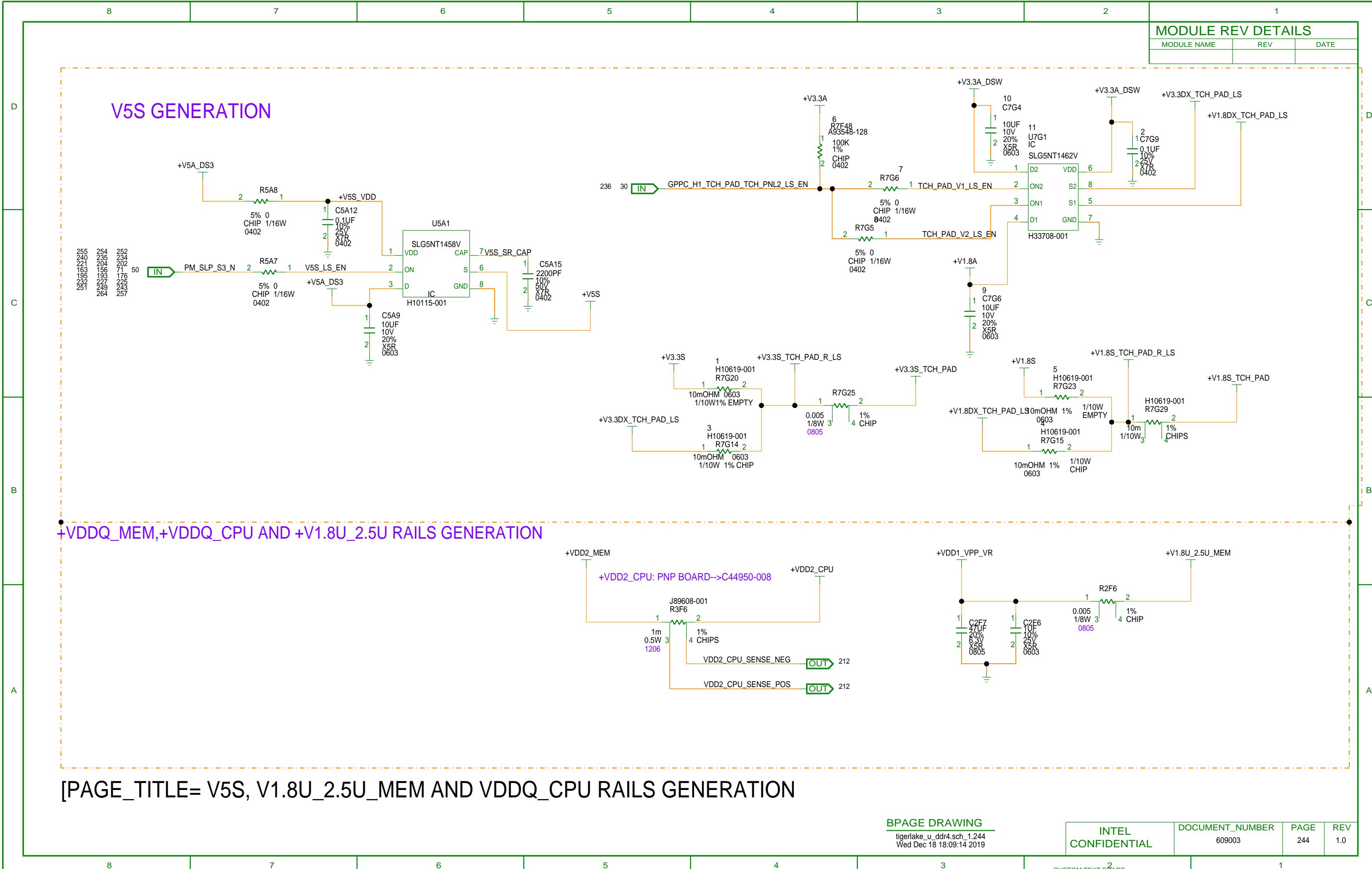






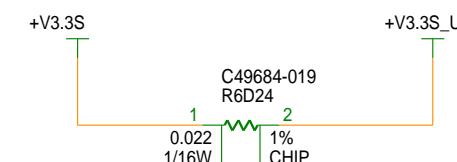
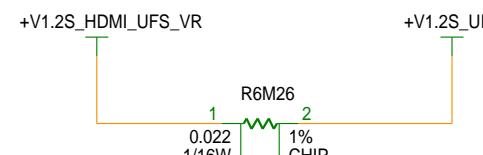
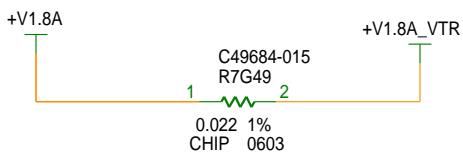
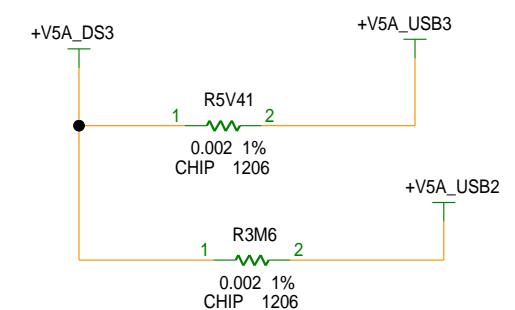
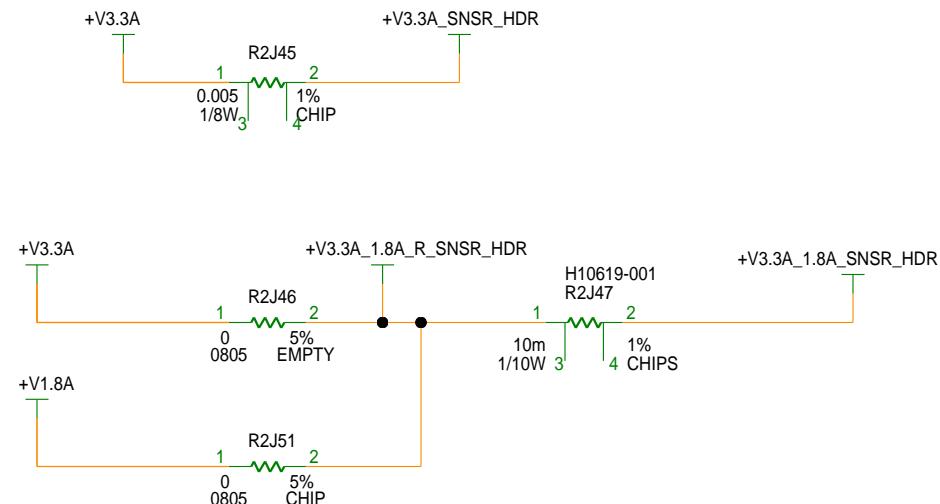
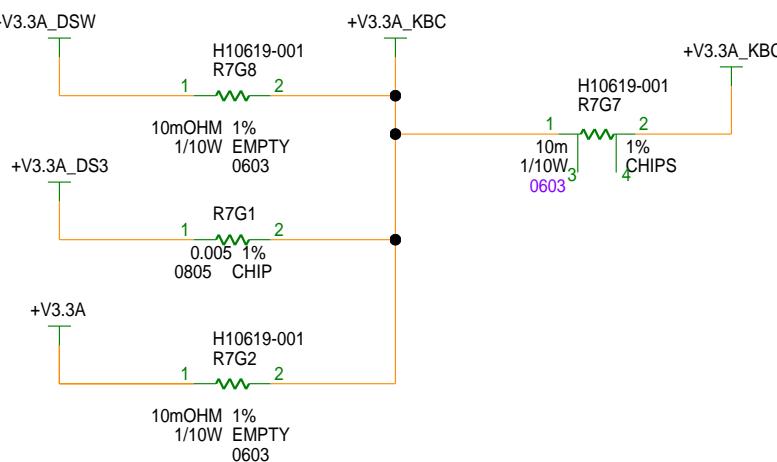


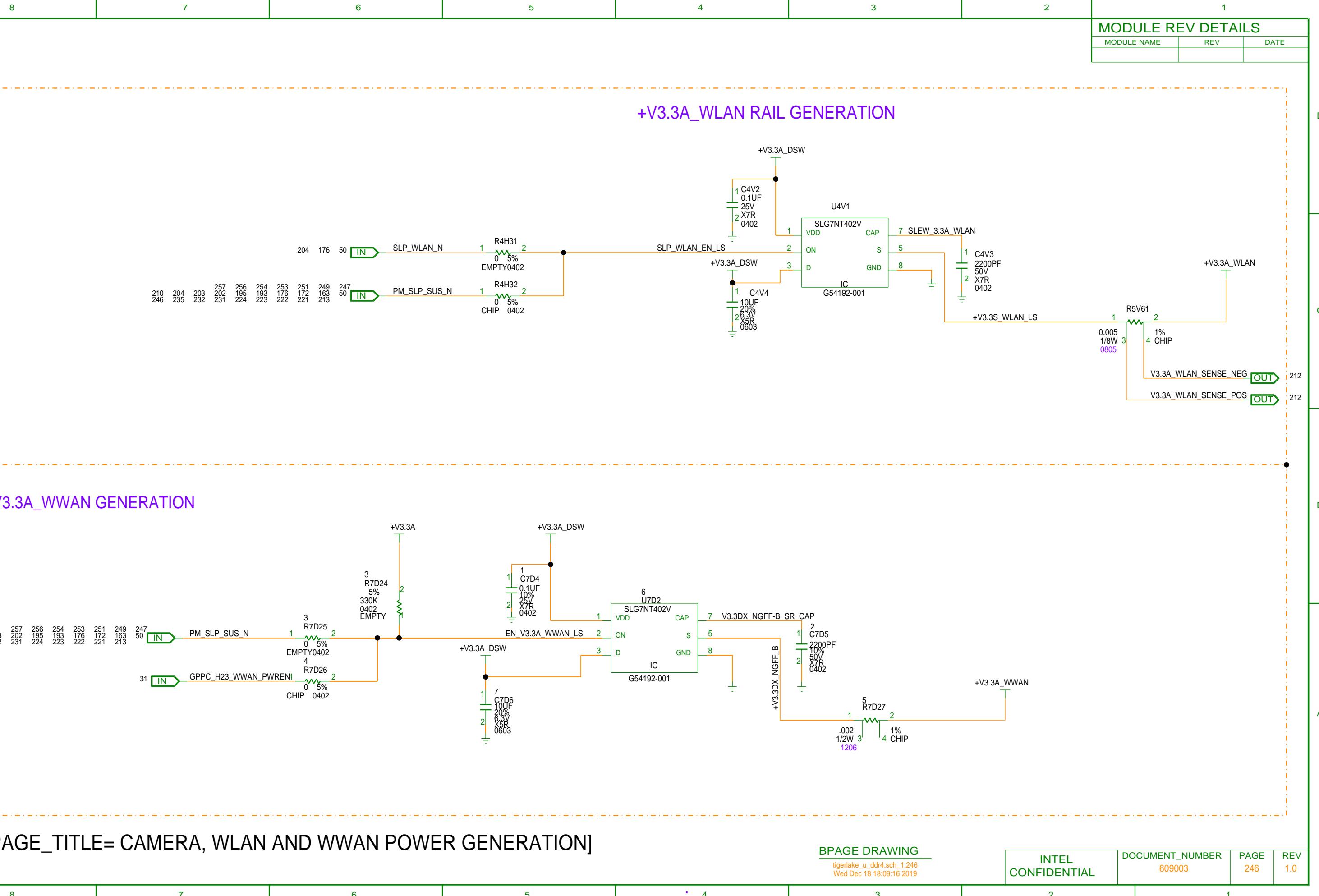


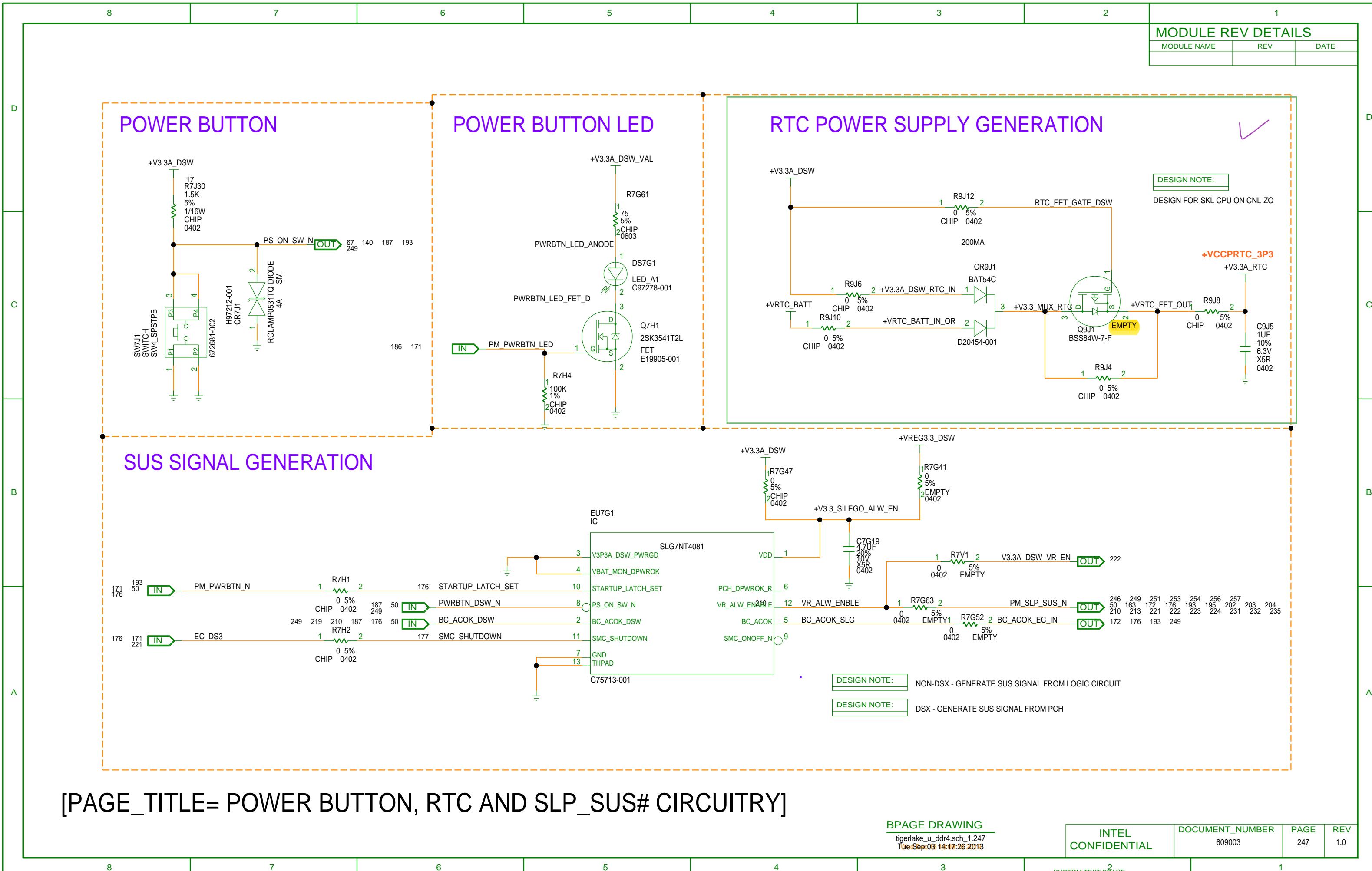


|                           |   |   |   |   |   |   |   |
|---------------------------|---|---|---|---|---|---|---|
| 8                         | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| <b>MODULE REV DETAILS</b> |   |   |   |   |   |   |   |

## DERIVED POWER RAILS







| 8                         | 7 | 6   | 5    | 4 | 3 | 2 | 1 |
|---------------------------|---|-----|------|---|---|---|---|
| <b>MODULE REV DETAILS</b> |   |     |      |   |   |   |   |
| MODULE NAME               |   | REV | DATE |   |   |   |   |

## POWER SEQUENCING LOGIC - PAGE I

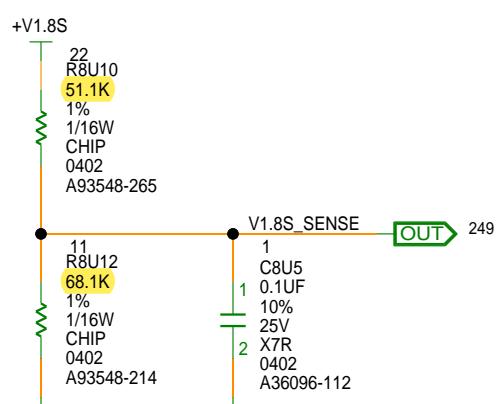
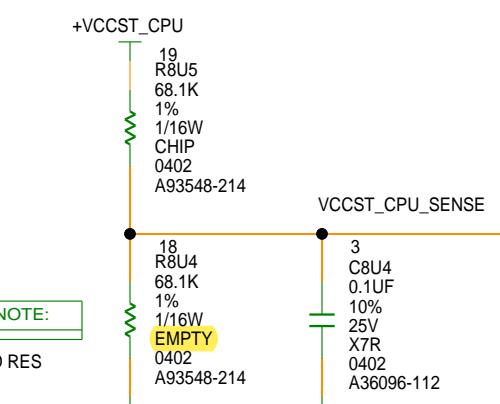
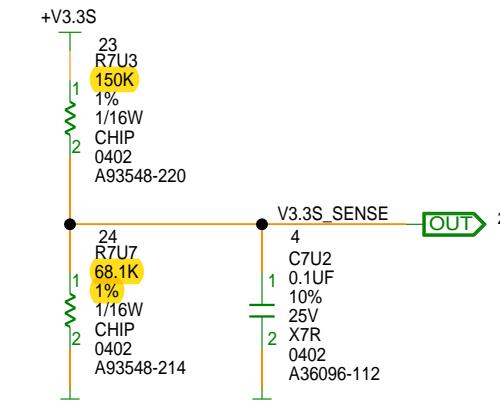
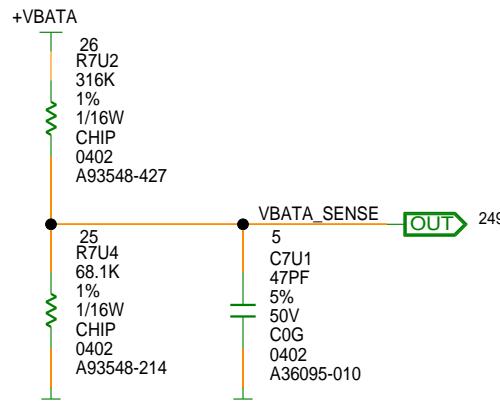


Table 1. TPS3779, TPS3780 Truth Table

| CONDITIONS          | OUTPUT      |
|---------------------|-------------|
| SENSE1 < $V_{IT^-}$ | OUT1 = low  |
| SENSE2 < $V_{IT^-}$ | OUT2 = low  |
| SENSE1 > $V_{IT^+}$ | OUT1 = high |
| SENSE2 > $V_{IT^+}$ | OUT2 = high |

| $V_{IT^+}$    | Positive-going input threshold voltage | $V_{(SENSE)} \text{ rising}$  | -1% | 1% | V |
|---------------|--|-------------------------------|-----|----|---|
| $V_{IT^+}$    | TPS3779A (0.5% hysteresis)             | 1.194                         |     |    |   |
|               | TPS3779B (5% hysteresis)               | 1.188                         |     |    |   |
|               | TPS3779C (10% hysteresis)              | 1.134                         |     |    |   |
|               | TPS3779D (1% hysteresis)               | 1.074                         |     |    |   |
|               |  | 1.182                         |     |    |   |
| $V_{IT^-}$    | Negative-going input threshold voltage | $V_{(SENSE)} \text{ falling}$ | -1% | 1% |   |
|               | TPS3779A (0.5% hysteresis)             | 1.194                         |     |    |   |
|               | TPS3779B (5% hysteresis)               | 1.188                         |     |    |   |
|               | TPS3779C (10% hysteresis)              | 1.134                         |     |    |   |
|               | TPS3779D (1% hysteresis)               | 1.074                         |     |    |   |
|               |  | 1.182                         |     |    |   |
| $V_{(SENSE)}$ | falling                                | -1%                           | 1%  |    |   |

DO NOT STUFF THE PD RES

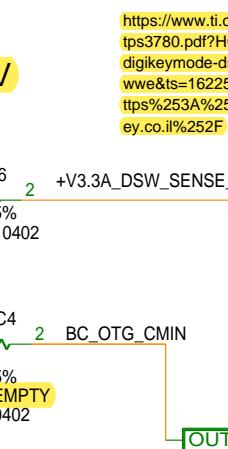
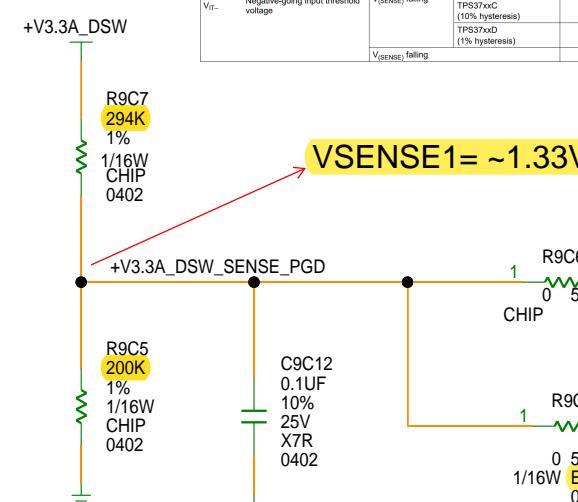
OUT1

5

2

O

OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below  $V_{IT^-}$ . OUT1 is deasserted (goes high) after SENSE1 rises higher than  $V_{IT^+}$ . OUT1 is a push-pull output for the TPS3779 and an open-drain output for the TPS3780. The open-drain device (TPS3780) can be pulled up to 6.5 V independent of VDD; a pull-up resistor is required for this device.

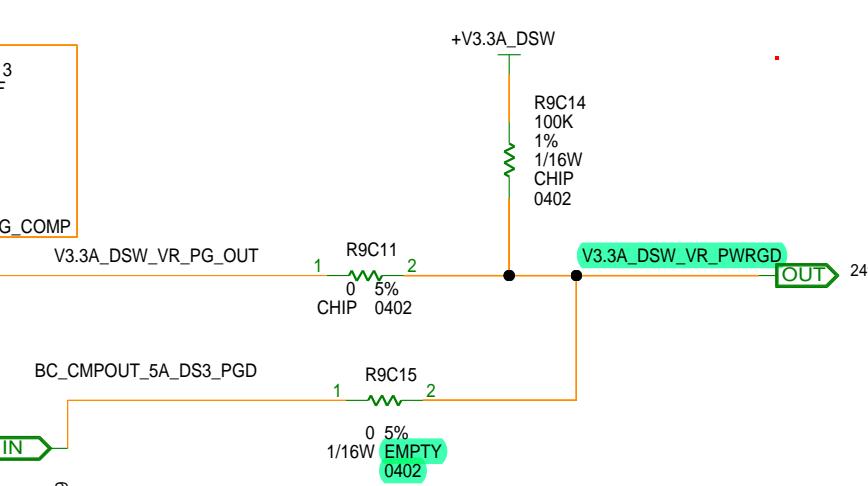
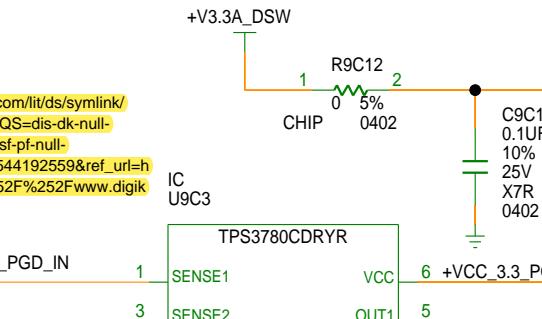


221 219

TPS37xx Dual-Channel, Low-Power,  
High-Accuracy Voltage Detectors

DESIGN NOTE:

SENSE2 COMPARATOR IS NOT USED



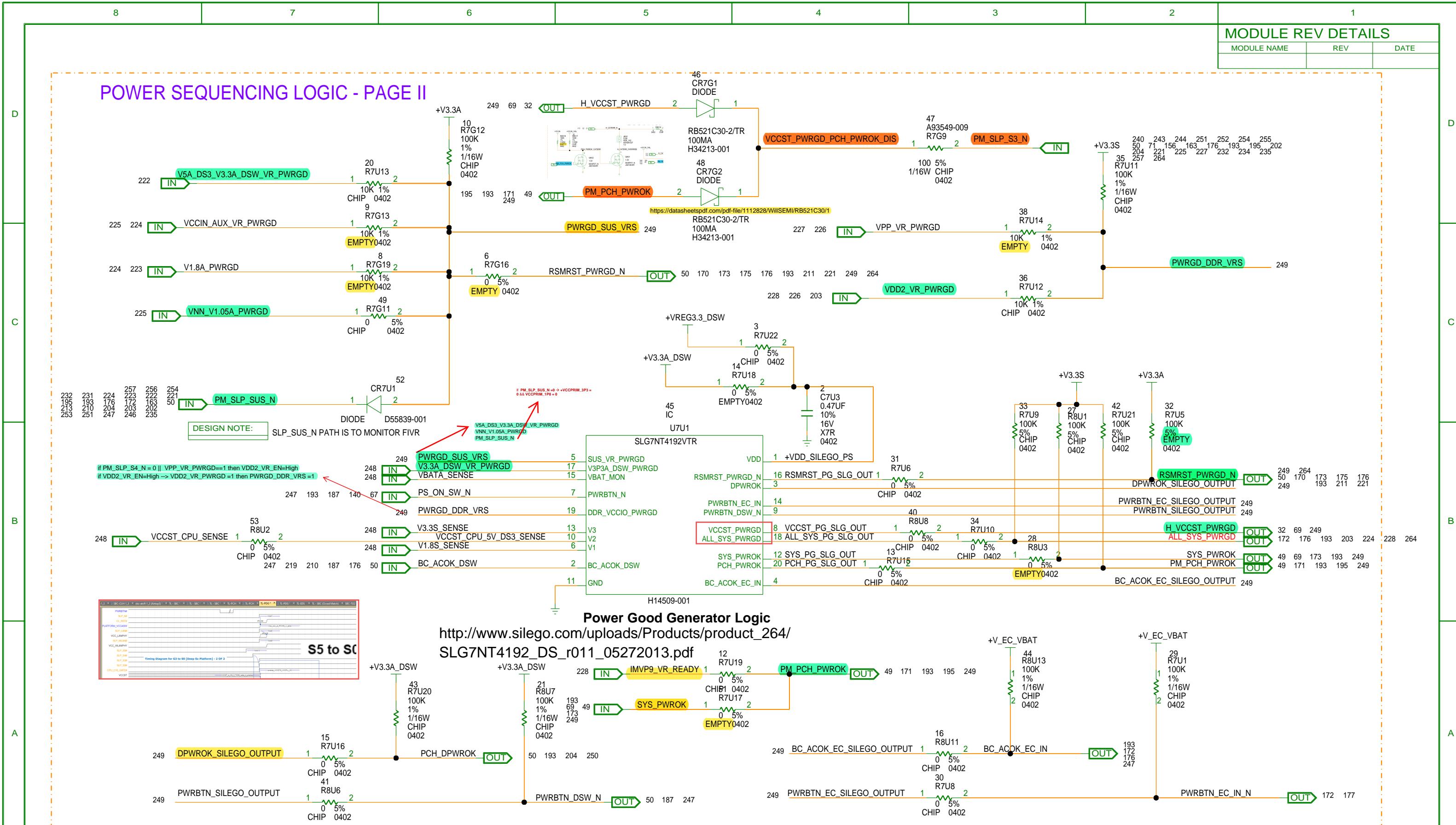
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Wed Dec 18 18:09:17 2019

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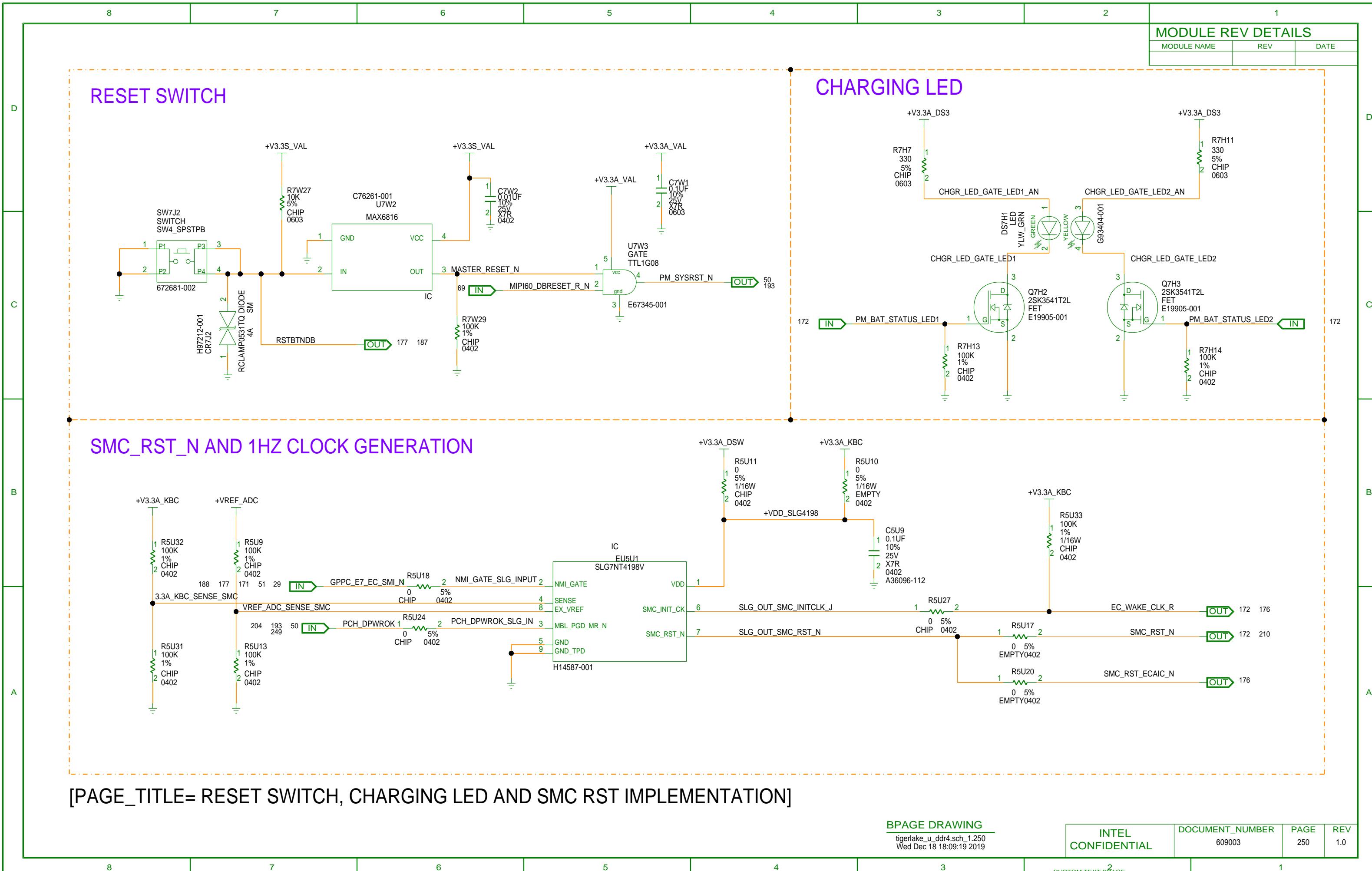
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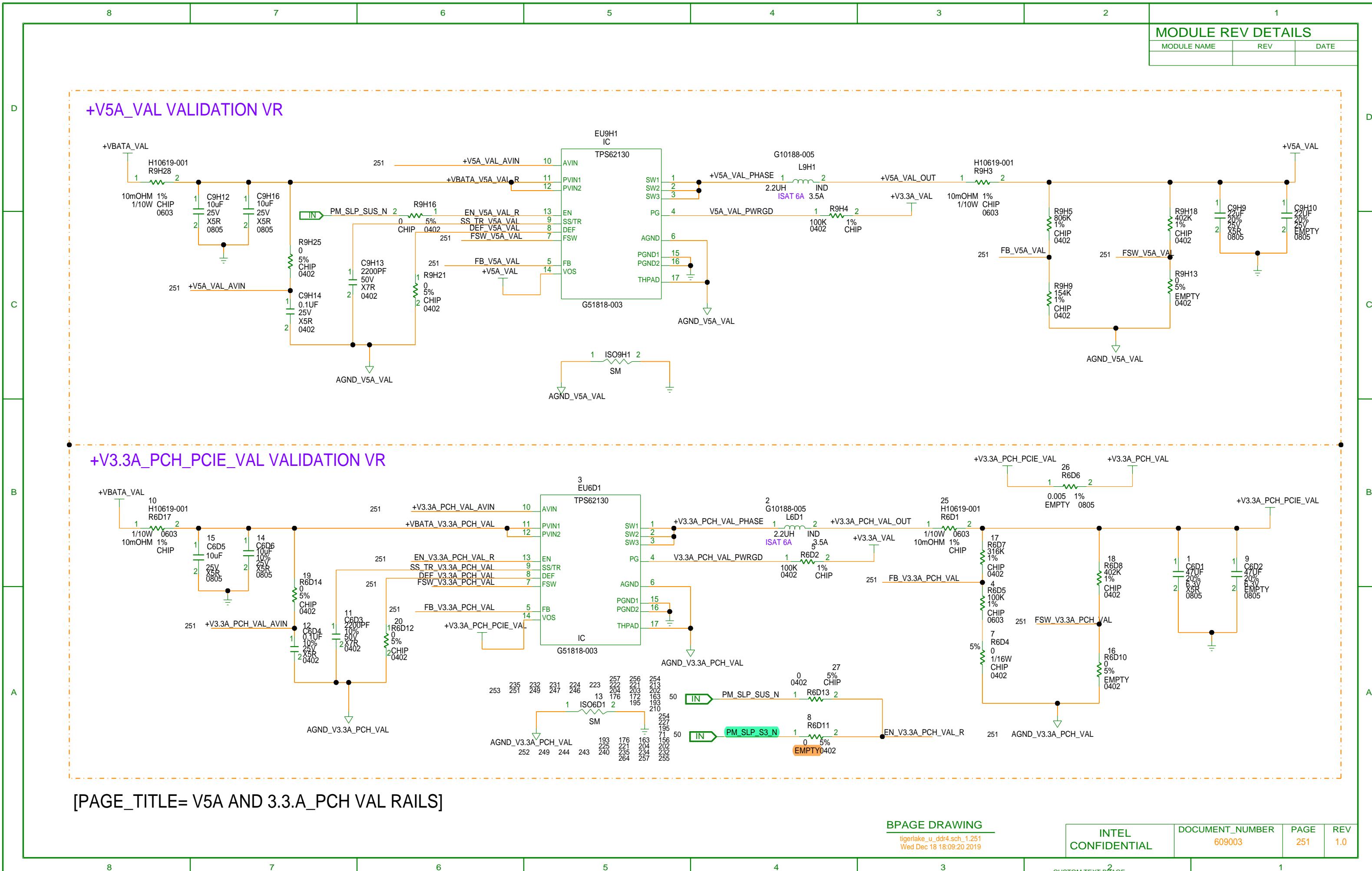


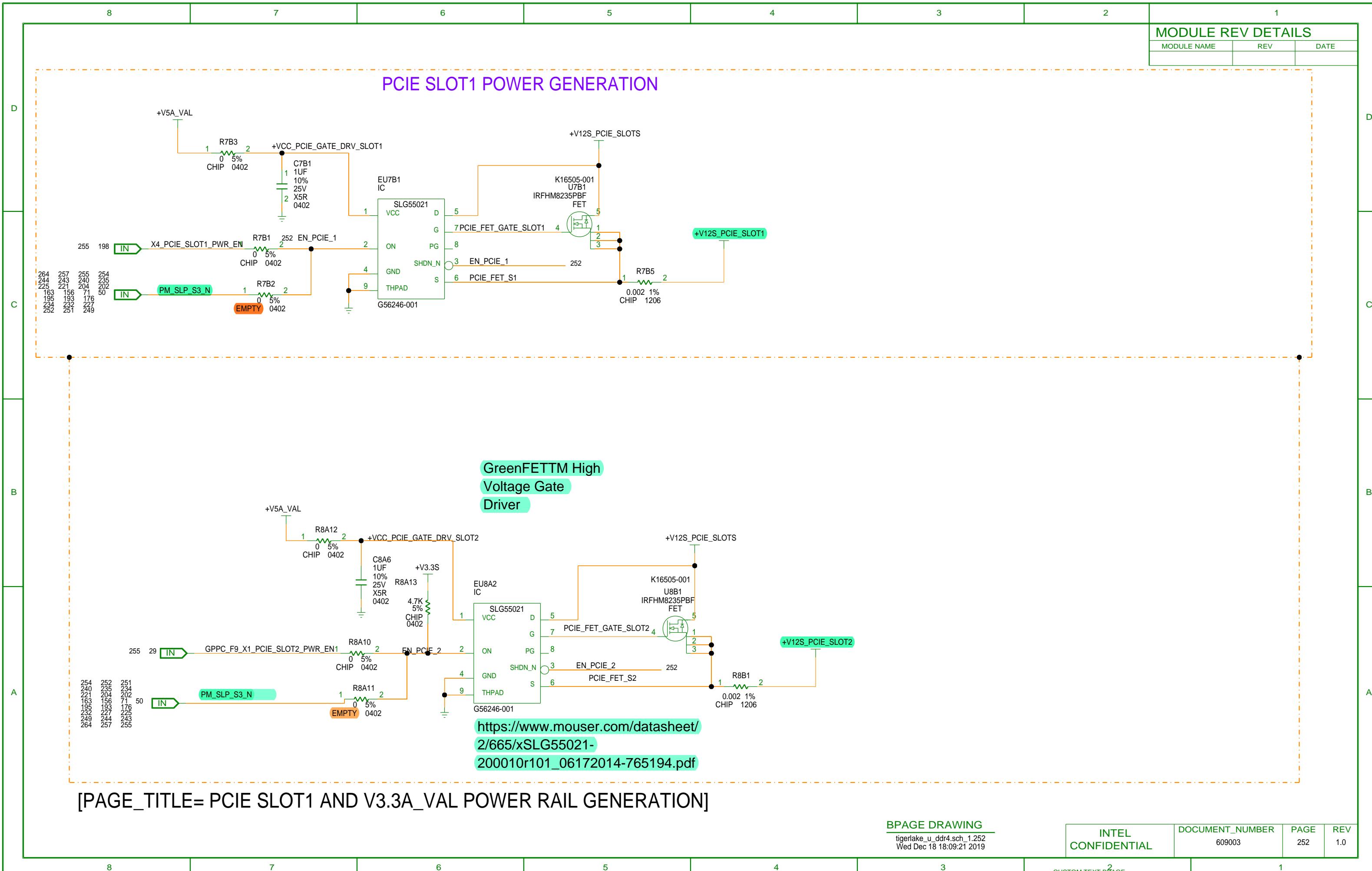
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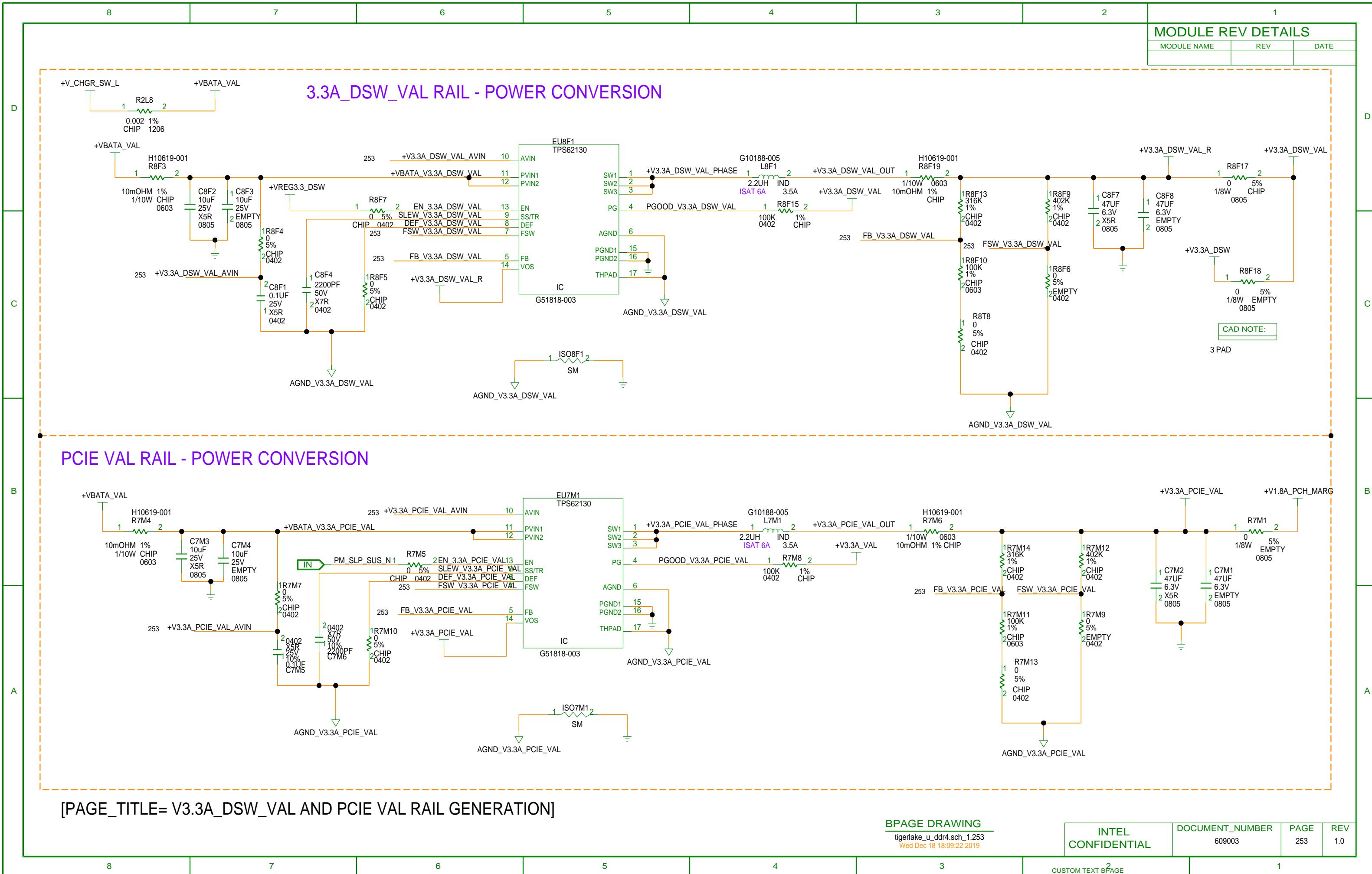
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| 2                     |                           | 1           |            |



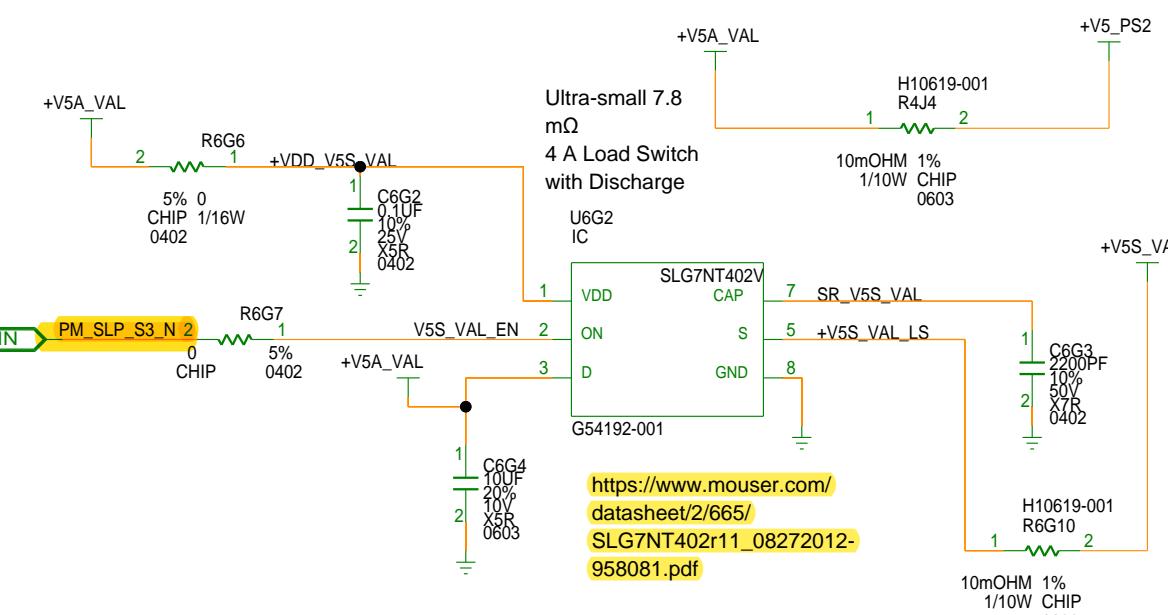




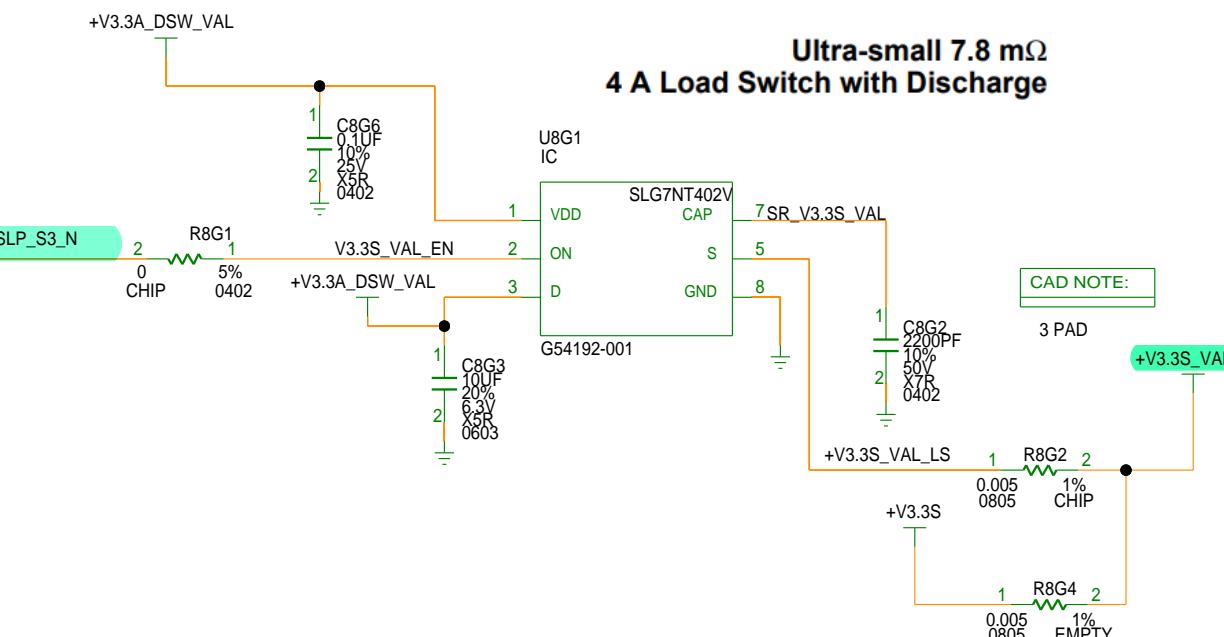


| 8                         | 7 | 6 | 5 | 4 | 3 | 2   | 1    |
|---------------------------|---|---|---|---|---|-----|------|
| <b>MODULE REV DETAILS</b> |   |   |   |   |   |     |      |
| MODULE NAME               |   |   |   |   |   | REV | DATE |

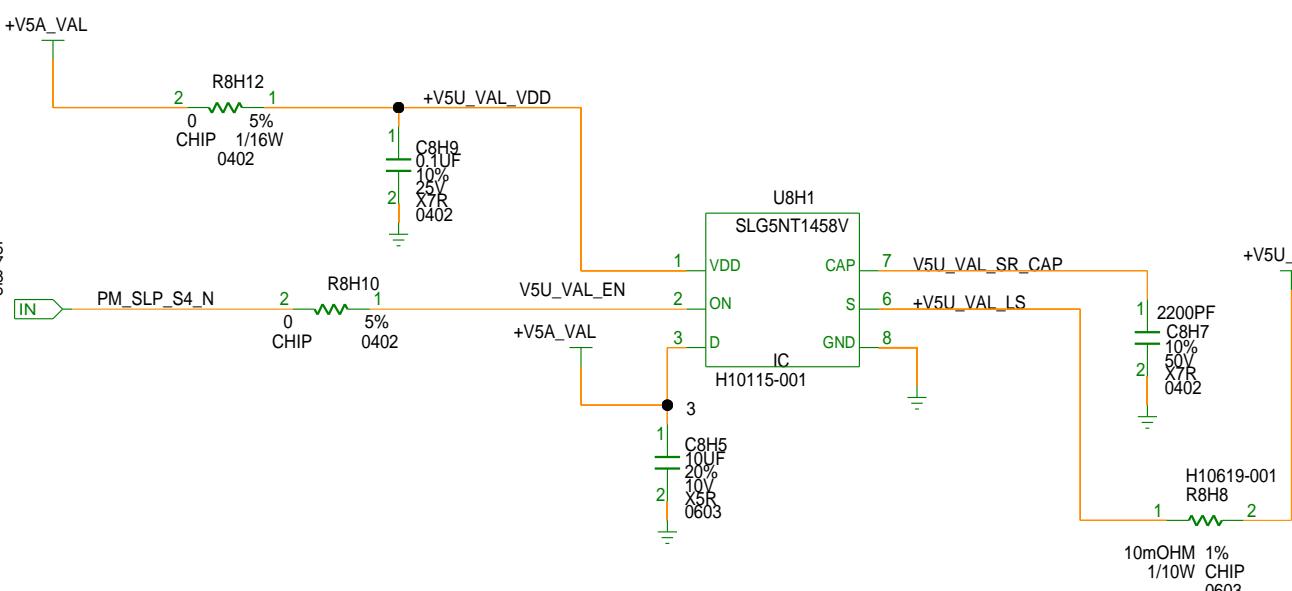
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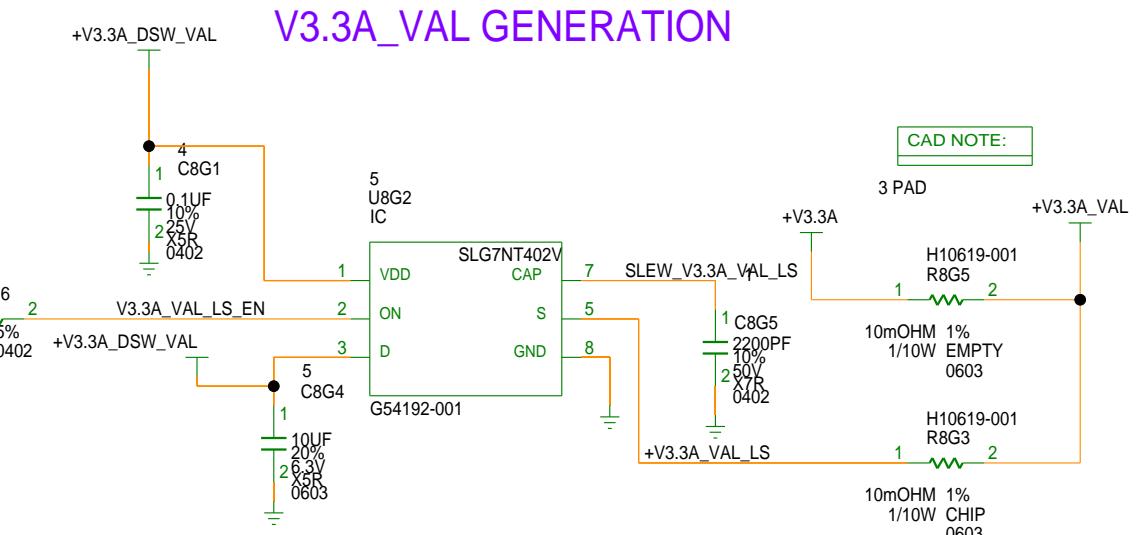
### V3.3S\_VAL GENERATION



### V5U\_VAL GENERATION



### V3.3A\_VAL GENERATION



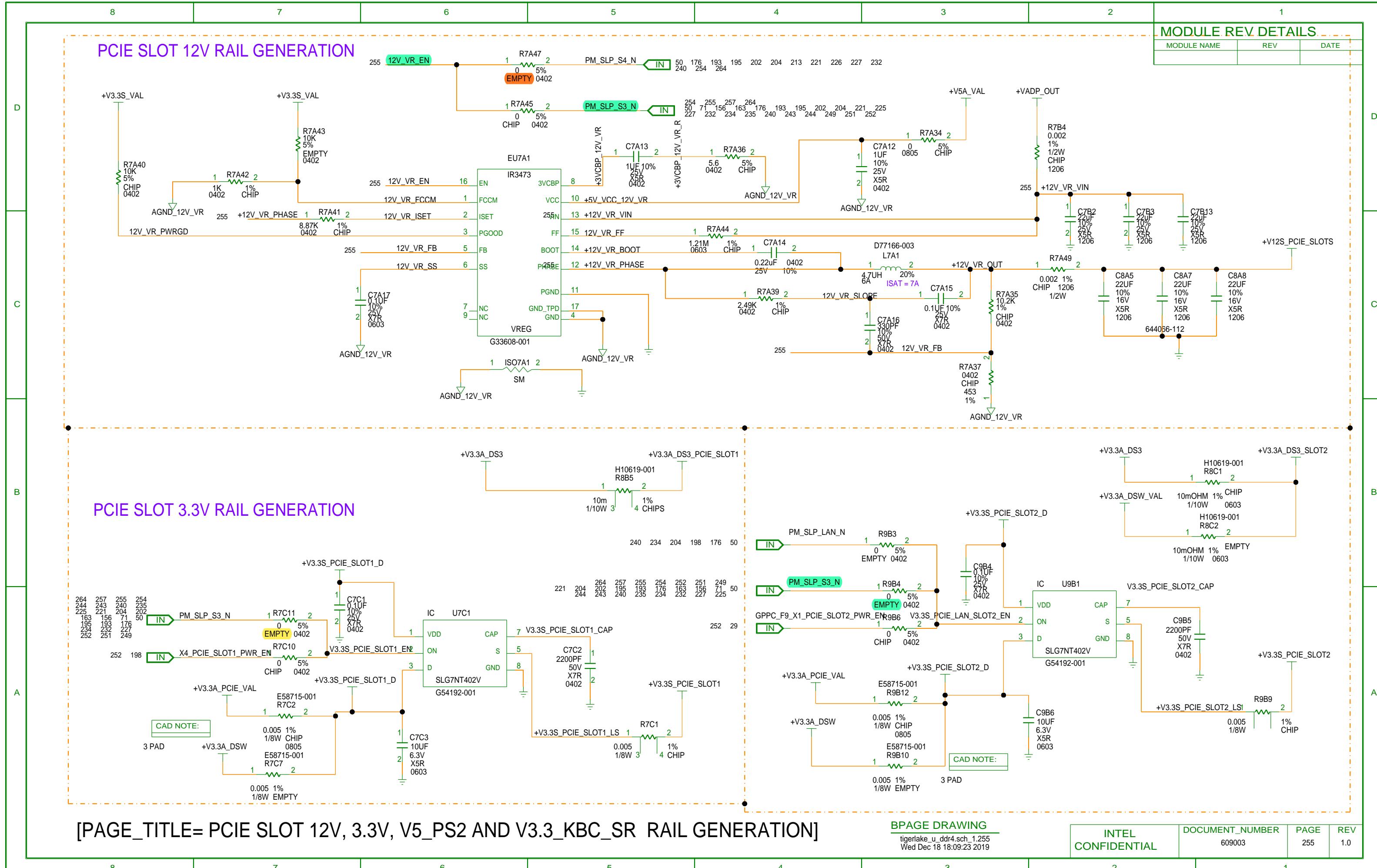
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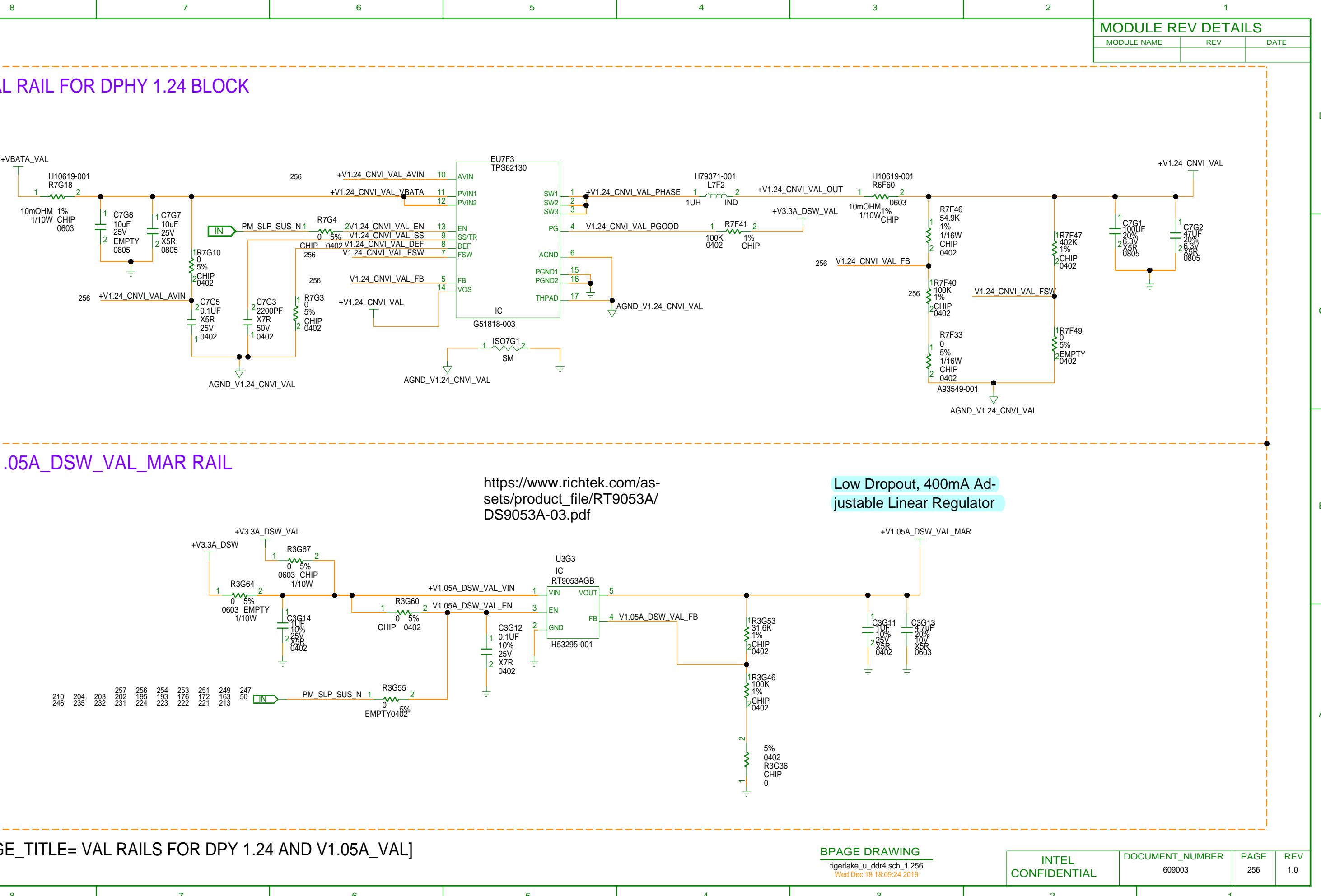
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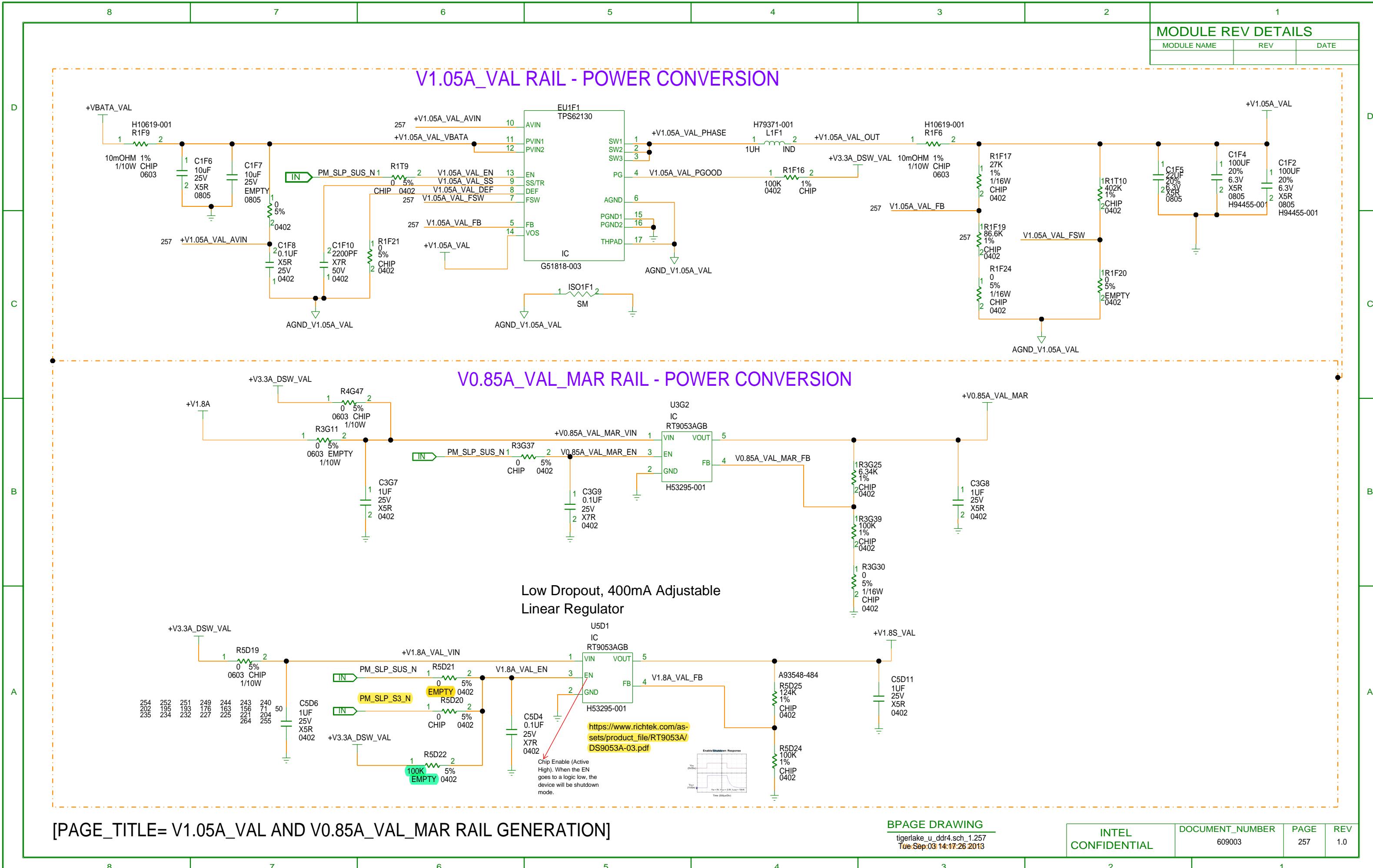
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Wed Dec 18 18:09:22 2019

| INTEL CONFIDENTIAL | DOCUMENT_NUMBER | PAGE | REV |
|--------------------|-----------------|------|-----|
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CUSTOM TEXT 2 PAGE







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|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|

| MODULE REV DETAILS |     |      |
|--------------------|-----|------|
| MODULE NAME        | REV | DATE |
|                    |     |      |

D

D

STF\_MTG\_HOLE  
EMPTY  
MH6J1  
MTG\_HOLE  
 9  
GND=1,2,3,4,5,6,7,8  
G39082-001

STF\_MTG\_HOLE  
EMPTY  
MH1B1  
MTG\_HOLE  
 9  
GND=1,2,3,4,5,6,7,8  
G39082-001

STF\_MTG\_HOLE  
EMPTY  
MH6F1  
MTG\_HOLE  
 9  
GND=1,2,3,4,5,6,7,8  
G39082-001

STF\_MTG\_HOLE  
EMPTY  
MH1J1  
MTG\_HOLE  
 9  
GND=1,2,3,4,5,6,7,8  
G39082-001

C

C

STF\_MTG\_HOLE  
EMPTY  
MH6A1  
MTG\_HOLE  
 9  
GND=1,2,3,4,5,6,7,8  
G39082-001

STF\_MTG\_HOLE  
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MTG\_HOLE  
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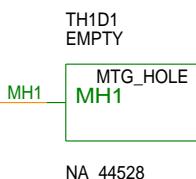
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G39082-001

STF\_MTG\_HOLE  
EMPTY  
MH9J1  
MTG\_HOLE  
 9  
GND=1,2,3,4,5,6,7,8  
G39082-001

B

B

STF\_MTG\_HOLE  
EMPTY  
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GND=1,2,3,4,5,6,7,8  
G39082-001



ADDED FOR MEMORY INTERPOSER

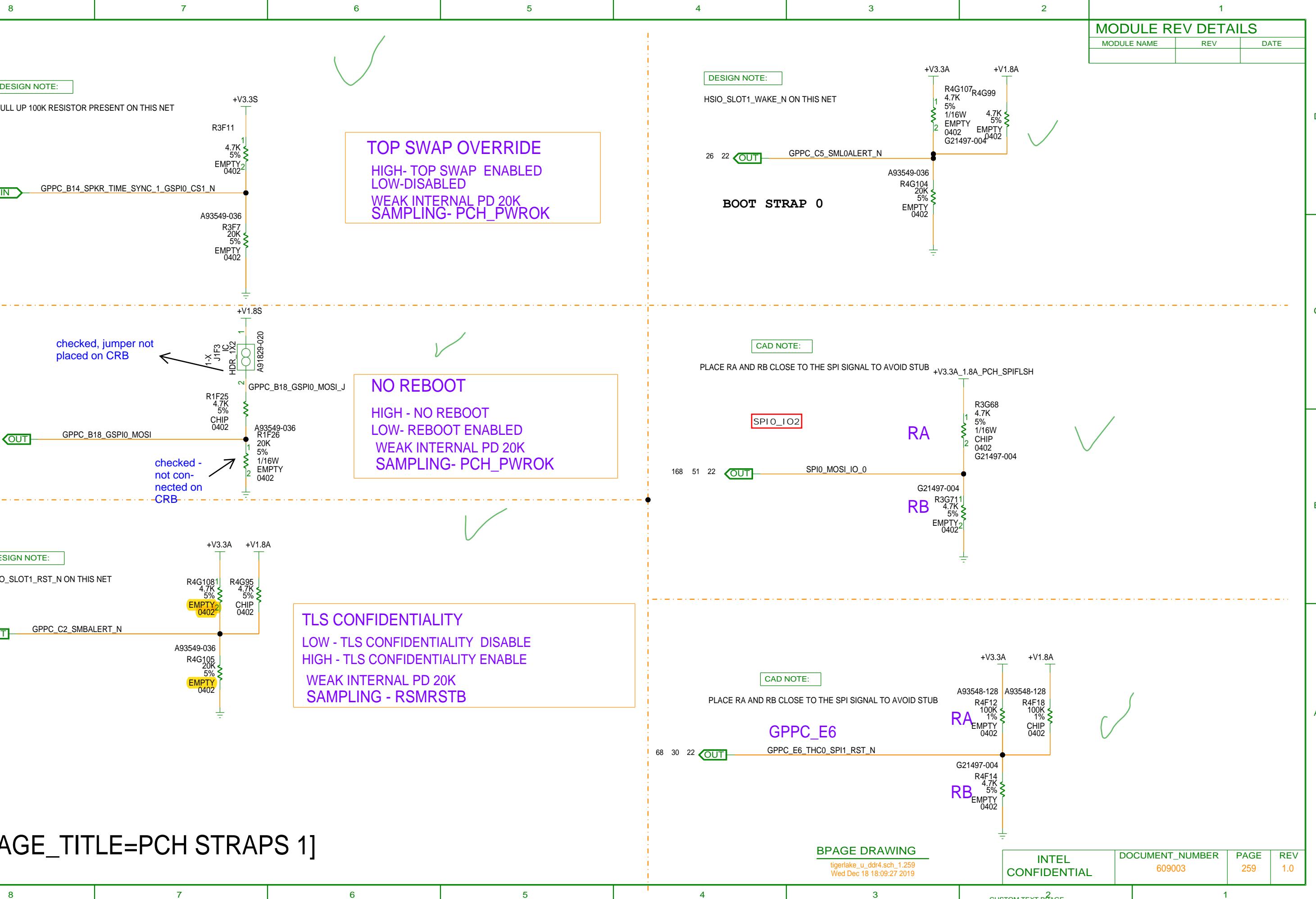
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Wed Dec 18 18:09:26 2019

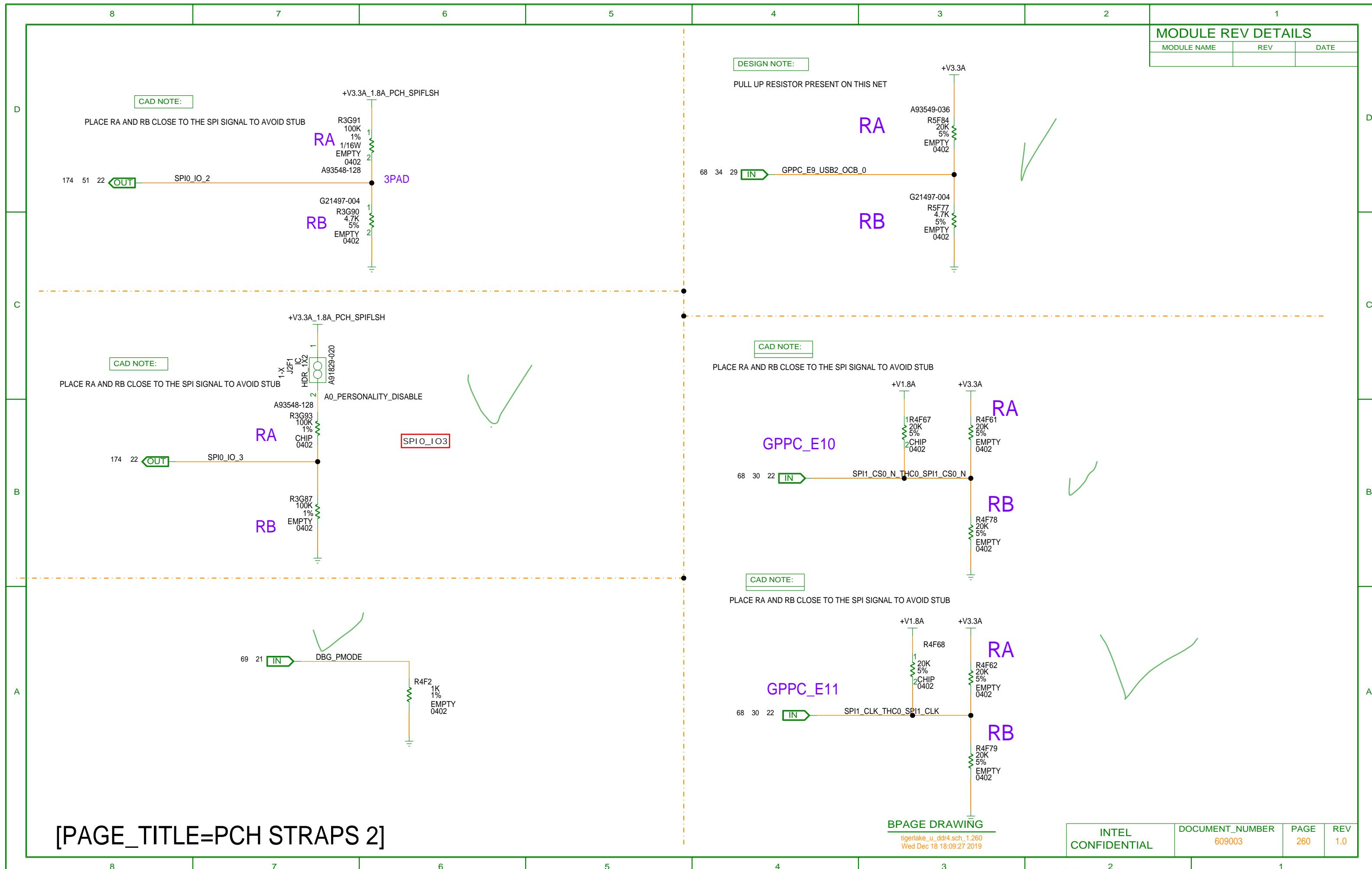
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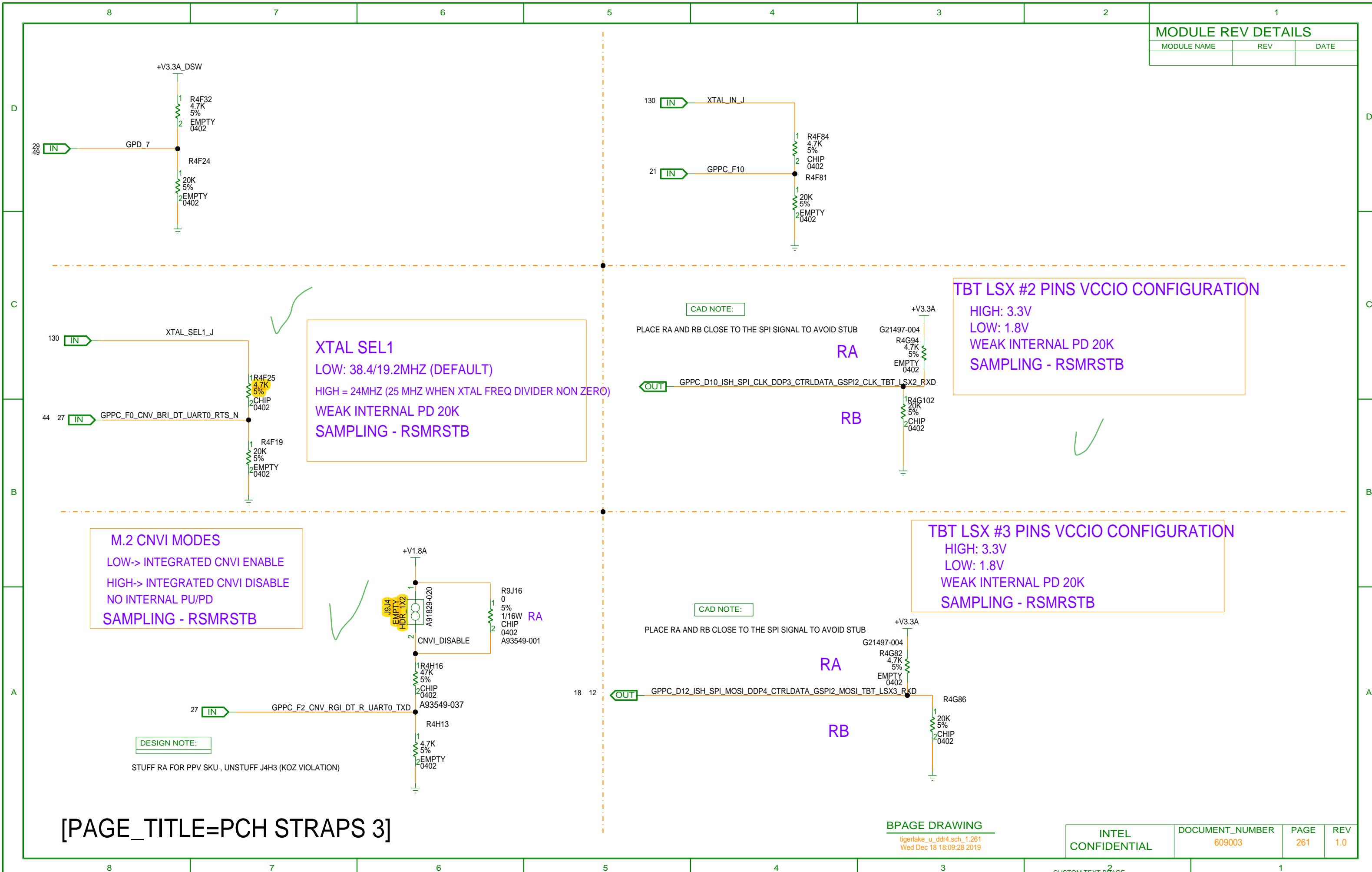
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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|

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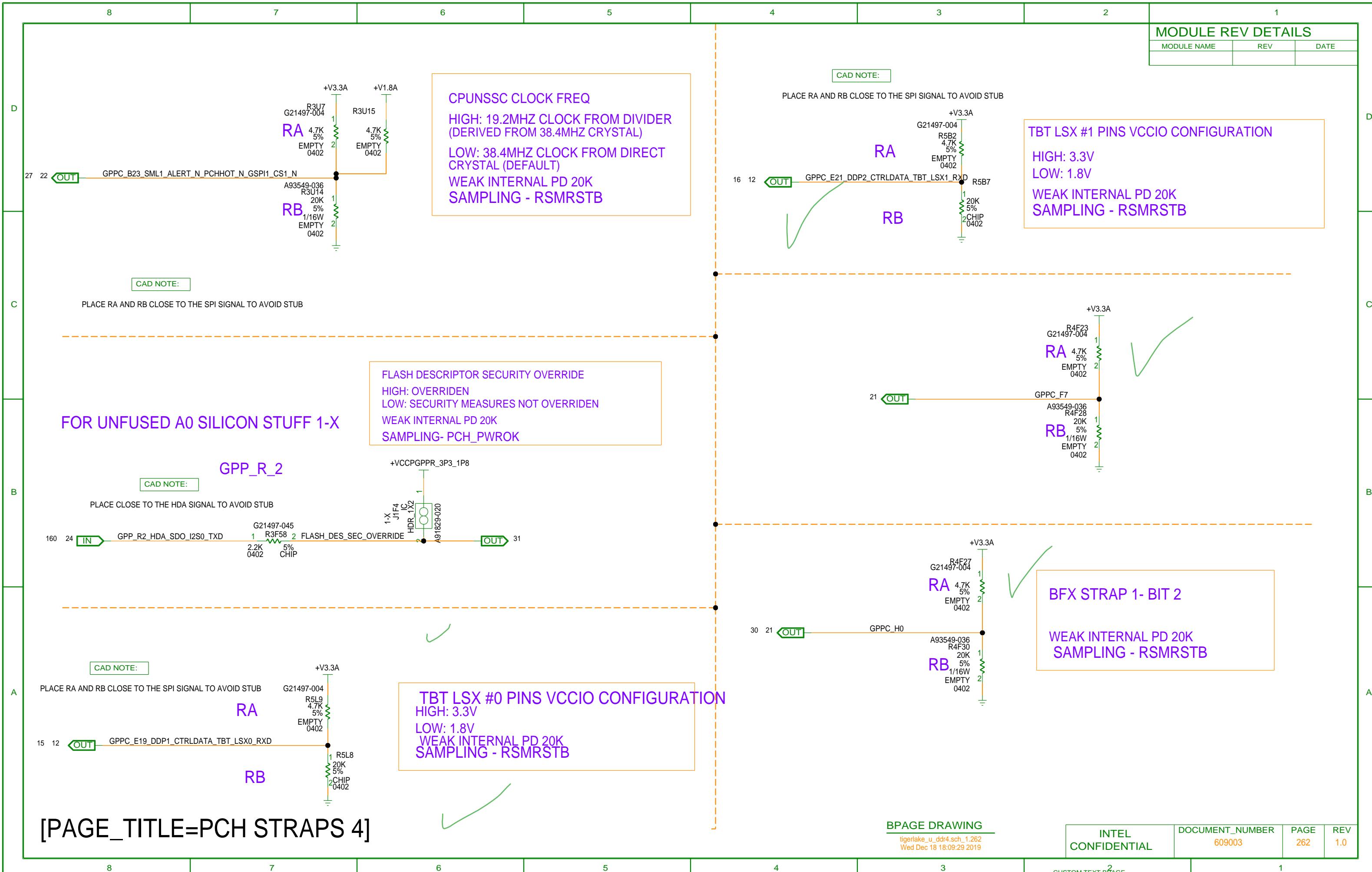


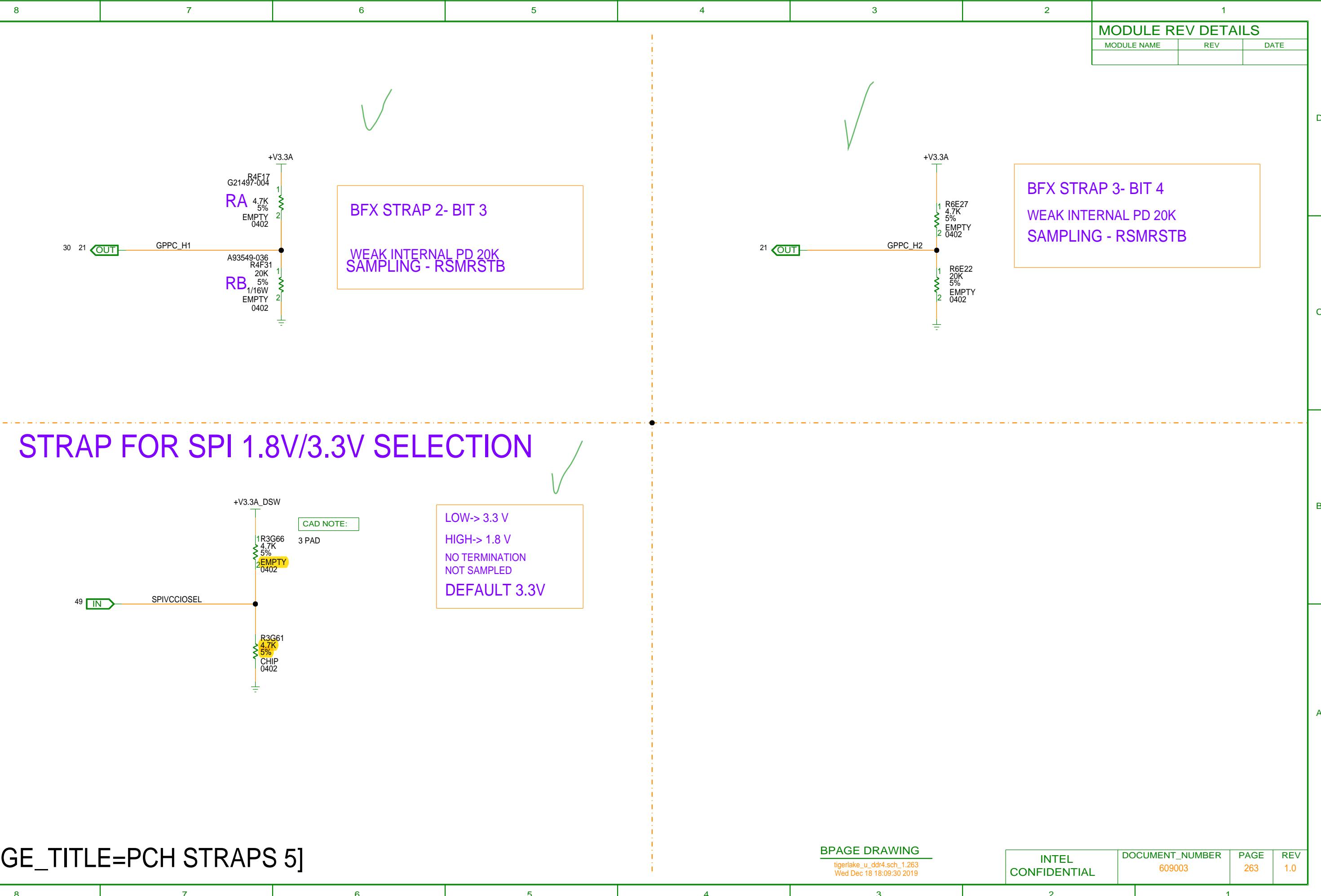
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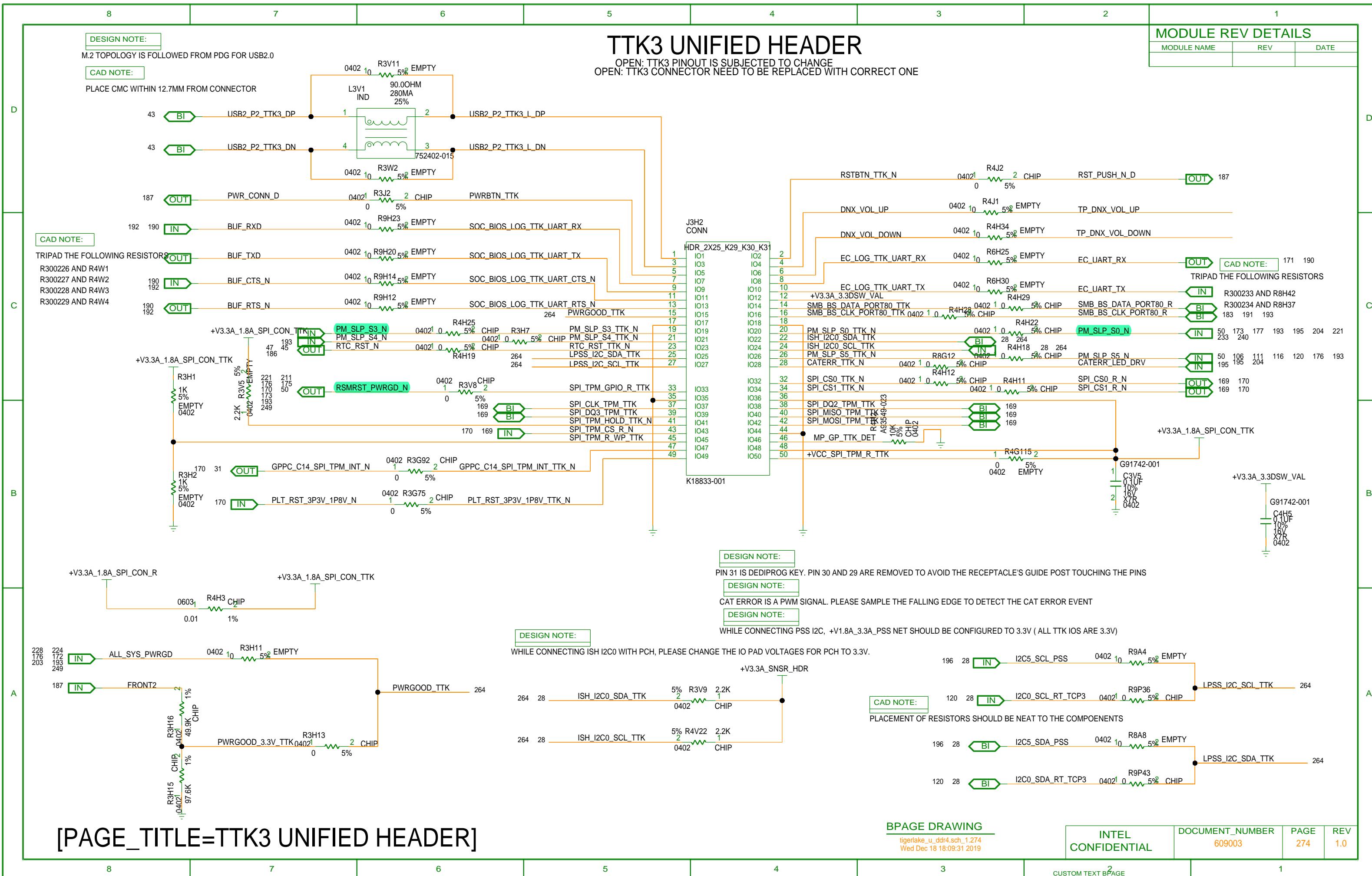


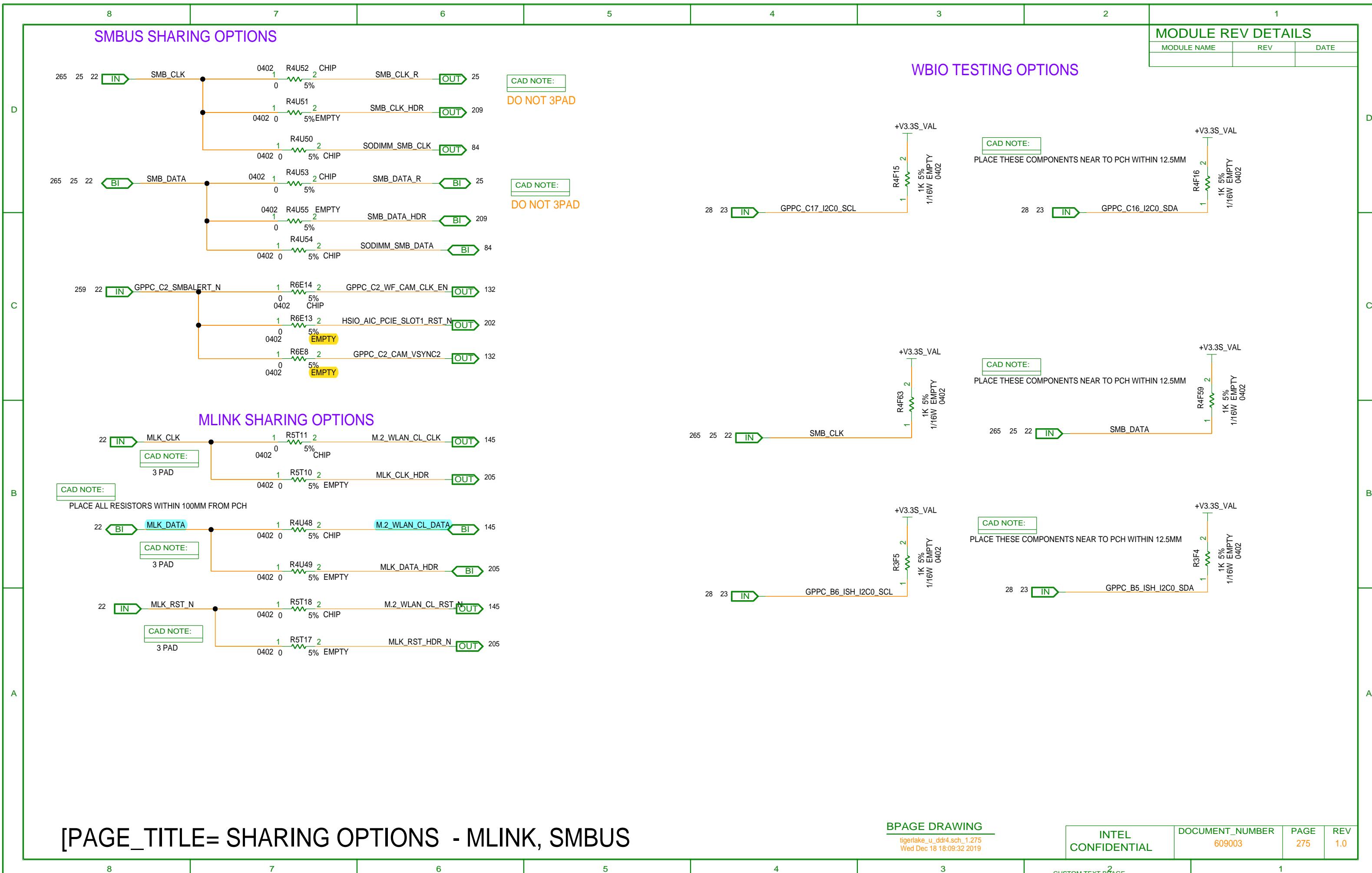


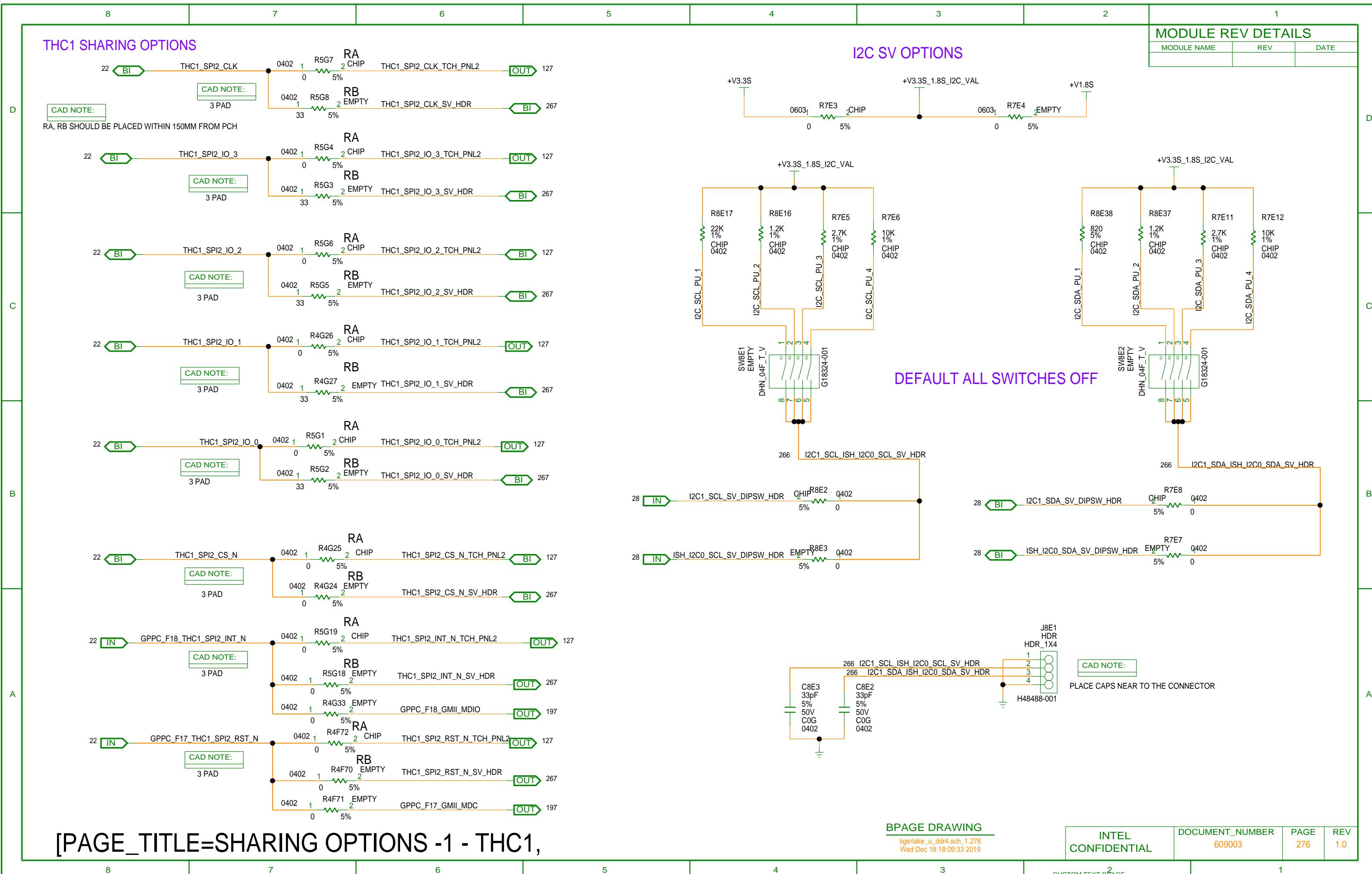
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| MODULE REV DETAILS |     |      |
|--------------------|-----|------|
| MODULE NAME        | REV | DATE |
|                    |     |      |

D

D

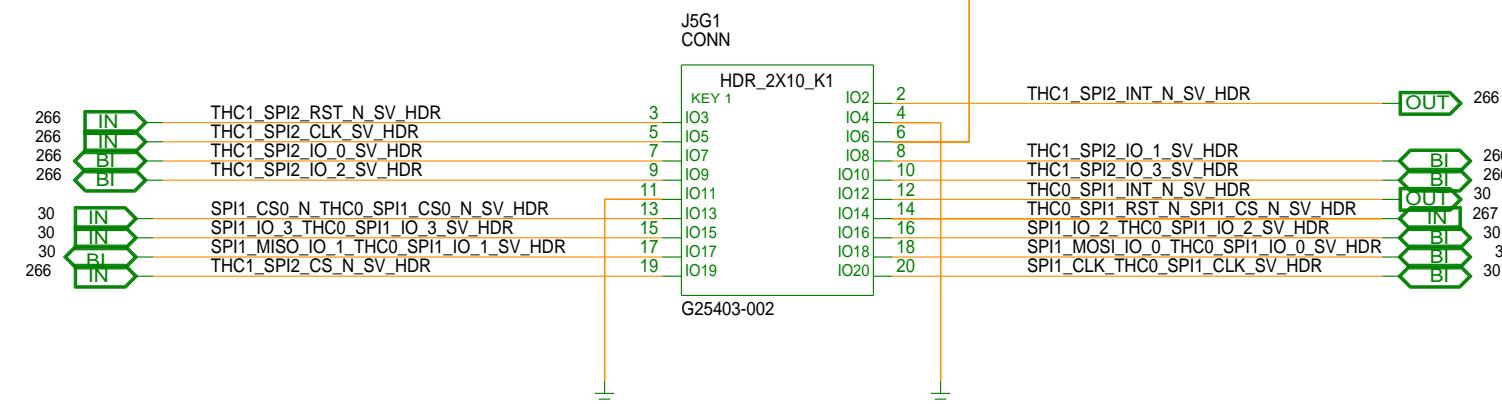
## THC0 , THC1 AND SPI1 SV VALIDATION HEADER

**DESIGN NOTE:**

ONLY SINGLE LOAD IS SUPPORTED. 1.8V IO:RA=33E, 3.3V IO IS NOT POR AND NOT SUPPORTED  
MAX CABLE LENGTH SUPPORTED IS 203MM

**CAD NOTE:**

PLACE RA CLOSE TO CONNECTOR WITHIN 25MM, FOR ALL SIGNALS  
PLACE CONNECTOR WITHIN 250MM FROM PCH



**DESIGN NOTE:**

ON LKF, SPI1 CS1 AND THC0 RESET ARE MULTIPLEXED. HENCE SAME OPTION IS MAINTAINED VIA RESISTOR STUFFING REWORK ON TGL FOR UNIFICATION BETWEEN PLATFORMS

