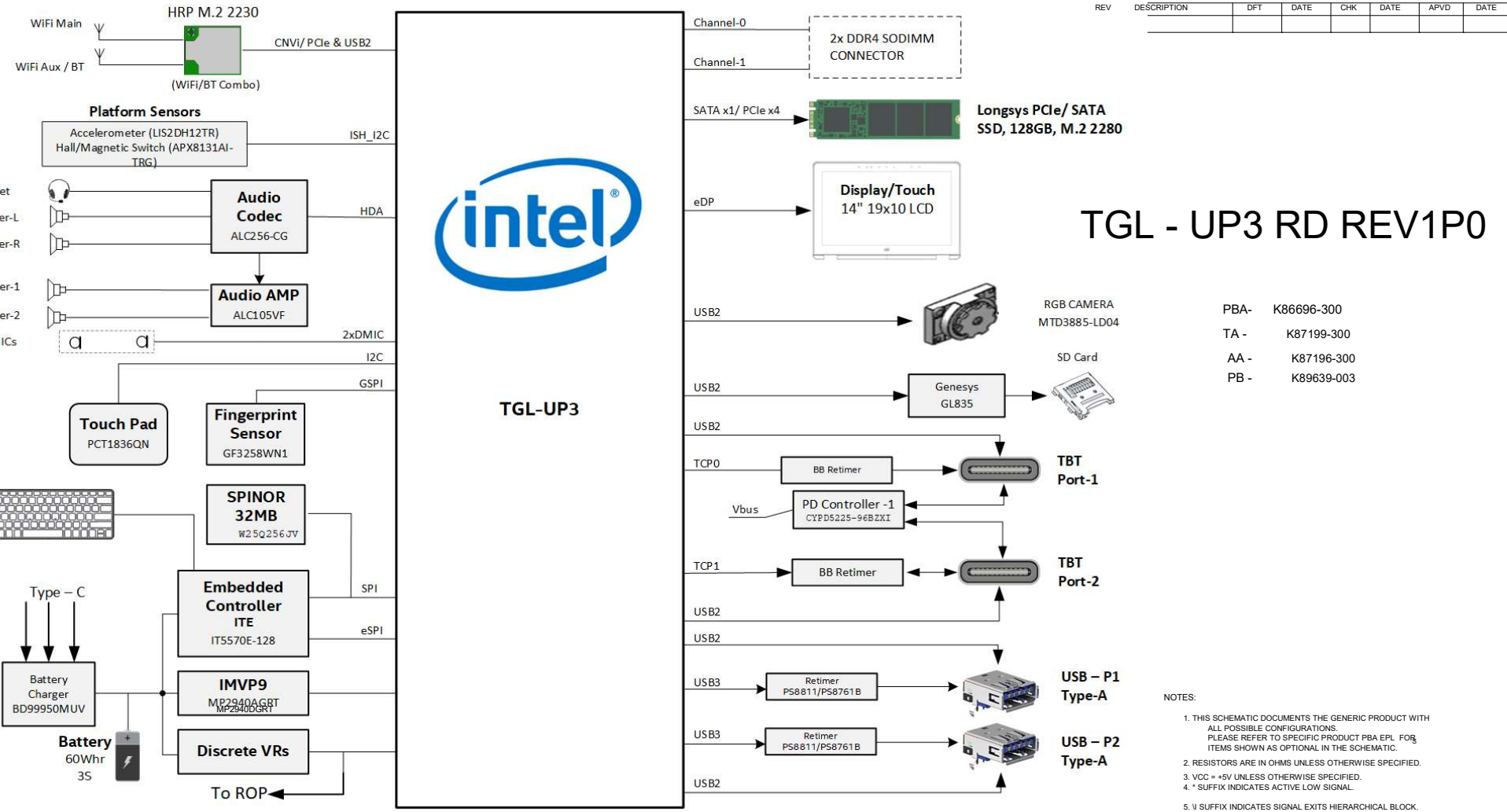

TGL - UP3 RD REV1P0

PBA- K86696-300
TA - K87199-300
AA - K87196-300
PB - K89639-003

REVISIONS

REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \ SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

BPAGE DRAWING

tgl_u_rd1
Fri Feb 28 13:40:47 2020

BOM_RELEASE_DATE	<BOM_RELEASE_DATE>	PB_NUMBER	<PB_NUMBER>
SIGNATURE	DATE	intel	3065 BOWERS AVE SANTA CLARA, CA 95051
DRN_BY <DRN_BY>	<DRN_BY_DATE>		
CHK_BY <CHK_BY>	<CHK_BY_DATE>	TITLE	TGL UP3 RD
ENGR_APVD <ENGR_APVD>	<ENGR_APVD_DATE>		
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<XR_PAGE_TITLE>

MODULE REV DETAILS		
MODULE NAME	REV	DATE

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IMPORTANT NOTE

SHEET NO.	SHEET NAME
68	POWER METER CIRCUITS ARE ONLY FOR VALIDATION PURPOSE, FOR MASS PRODUCTION ALL THESE CIRCUIT CAN BE DELETED or MADE IT UNSTUFF
Note : 1	R153,R208, R6601, R1810, R1811, R18, R27, R61, R342, R6001 - All these SENSE resistor must be deleted for better performance and cost reduction
Note : 2	R659, R1340, R274, R4704 R8709, R8601 - All these Shunt resistor provisions are for Validation purpose (can be used for power measurement sense resistor)
Note : 3	In this design PS8811 RETIMER PART is used due to longer routing length, For routing length is lesser than 10inch design can replace the part with PS8761 (Get the latest update and design details from vendor)

BPAGE DRAWING

tgl_u_rdi

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MODULE REV DETAILS

MODULE NAME	REV	DATE

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EDP_TX3_DP
EDP_TX3_DN
EDP_TX2_DP
EDP_TX2_DN
EDP_TX1_DP
EDP_TX1_DN
EDP_TX0_DP
EDP_TX0_DN
EDP_AUX_DP
EDP_AUX_DN
TP_GPPC_E22_DNX_FORCE_RELOAD
EDP_HPD
GPPC_E18_TBT_LSX0_TXD
GPPC_E19_TBT_LSX0_RXD
GPPC_E20_TBT_LSX1_TXD
GPPC_E21_TBT_LSX1_RXD
EDP_VDD_EN
EDP_BKLT_EN
EDP_BKLT_CTRL

DDIA_TXP_3 AC2
DDIA_TXN_3 AC1
DDIA_TXP_2 AD2
DDIA_TXN_2 AD1
DDIA_TXP_1 AF1
DDIA_TXN_1 AF2
DDIA_TXP_0 AG2
DDIA_TXN_0 AG1
DDIA_AUX_P AJ2
DDIA_AUX AJ1
GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD DN4
GPP_E23/DDPA_CTRLDATA DT6
GPP_E14/DDSP_HPDA/DISP_MISCA DR5
DDIB_TXP_3 T12
DDIB_TXN_3 T11
DDIB_TXP_2 Y11
DDIB_TXN_2 Y9
DDIB_TXP_1 T9
DDIB_TXN_1 R8
DDIB_TXP_0 V11
DDIB_TXN_0 V9
DDIB_AUX_P AB9
DDIB_AUX AD9
GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN DM29
GPP_H17/DDPB_CTRLDATA DK27
GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD DG43
GPP_A21/DDPC_CTRLCLK/I2S5_TXD DG47
GPP_A22/DDPC_CTRLDATA/I2S5_RXD DJ47
GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD DU8
GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD DV8
GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD DF6
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD DD6
GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0# DN23
GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK DM23
GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO DK23
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI DN21
GPP_A17/DISP_MISCC/I2S4_TXD DF43
GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK DF45
GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM DF47
GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1 DH52
GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK DK45
EDP_VDDEN DM8
EDP_BKLTEN DN8
EDP_BKLTCTL DG10

TCP0_TXRX_P1 AY2
TCP0_TXRX_N1 AY1
TCP0_TXRX_P0 BB1
TCP0_TXRX_N0 BB2
TCP0_TX_P1 AM5
TCP0_TX_N1 AM7
TCP0_TX_P0 AT7
TCP0_TX_N0 AT5
TCP0_AUX_P AP7
TCP0_AUX AP5
TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX AF5
TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE2
TCP2_TXRX_N0 BE1
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX BB7
TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX BK7
TC_RCOMP_P AN2
TC_RCOMP AN1
DSI_DE_TE_2 M8
DDI_RCOMP AB1
DISP_UTILS/DSI_DE_TE_1 CE4

TCP0_TXRX1_DP
TCP0_TXRX1_DN
TCP0_TXRX0_DP
TCP0_TXRX0_DN
TCP0_TX1_DP
TCP0_TX1_DN
TCP0_TX0_DP
TCP0_TX0_DN
TCP0_AUX_DP
TCP0_AUX_DN
TCP1_TXRX1_DP
TCP1_TXRX1_DN
TCP1_TXRX0_DP
TCP1_TXRX0_DN
TCP1_TX1_DP
TCP1_TX1_DN
TCP1_TX0_DP
TCP1_TX0_DN
TCP1_AUX_DP
TCP1_AUX_DN
TCRCOMP_DP
TCRCOMP_DN
DP_RCOMP

150 RES 1% 0201 R401
R402 150 1% 0201 RES
0

TGL_UP3_IP_EXT/BGA

DESIGN NOTE:

LSX MODE
LSX_TXD:LSX TXD, LSX_RXD:LSX RXD

DESIGN NOTE:

BSSB MODE
LSX_TXD:BSSB RXD, LSX_RXD:BSSB TXD

CAD NOTE:

TC_RCOMP_P/N RDC SHOULD BE <0.5 OHMS (SUM OF BOTH TRACES) AND WITH MAIN ROUTE TRACE SPACING OF 380UM (SL/DSL) OR 500UM (MS). PROVIDE GOOD NOISE ISOLATION. CAPACITANCE REQUIREMENT IS <1.9PF INCLUDING ROUTING AND VIA CAPS

DDI_RCOMP RDC SHOULD BE <0.2 OHM WITH MAIN ROUTE TRACE SPACING OF 380UM (SL/DSL) OR 500UM (MS). PROVIDE GOOD NOISE ISOLATION

BPAGE DRAWING

tgl_u_rd:GND
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U1B

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LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

M_0_DQ_0<7>	CP53	DDR0_DQ0_7/DDR0_DQ0_7/DDR0_DQ0_7	
M_0_DQ_0<6>	CP52	DDR0_DQ0_6/DDR0_DQ0_6/DDR0_DQ0_6	
M_0_DQ_0<5>	CP50	DDR0_DQ0_5/DDR0_DQ0_5/DDR0_DQ0_5	
M_0_DQ_0<4>	CP49	DDR0_DQ0_4/DDR0_DQ0_4/DDR0_DQ0_4	
M_0_DQ_0<3>	CU53	DDR0_DQ0_3/DDR0_DQ0_3/DDR0_DQ0_3	
M_0_DQ_0<2>	CU52	DDR0_DQ0_2/DDR0_DQ0_2/DDR0_DQ0_2	
M_0_DQ_0<1>	CU50	DDR0_DQ0_1/DDR0_DQ0_1/DDR0_DQ0_1	
M_0_DQ_0<0>	CU49	DDR0_DQ0_0/DDR0_DQ0_0/DDR0_DQ0_0	
M_0_DQ_1<7>	CH53	DDR0_DQ1_7/DDR0_DQ1_7/DDR0_DQ1_7	
M_0_DQ_1<6>	CH52	DDR0_DQ1_6/DDR0_DQ1_6/DDR0_DQ1_6	
M_0_DQ_1<5>	CH50	DDR0_DQ1_5/DDR0_DQ1_5/DDR0_DQ1_5	
M_0_DQ_1<4>	CH49	DDR0_DQ1_4/DDR0_DQ1_4/DDR0_DQ1_4	
M_0_DQ_1<3>	CL53	DDR0_DQ1_3/DDR0_DQ1_3/DDR0_DQ1_3	
M_0_DQ_1<2>	CL52	DDR0_DQ1_2/DDR0_DQ1_2/DDR0_DQ1_2	
M_0_DQ_1<1>	CL50	DDR0_DQ1_1/DDR0_DQ1_1/DDR0_DQ1_1	
M_0_DQ_1<0>	CL49	DDR0_DQ1_0/DDR0_DQ1_0/DDR0_DQ1_0	
M_0_DQ_2<7>	CT47	DDR0_DQ2_7/DDR0_DQ2_7/DDR1_DQ0_7	
M_0_DQ_2<6>	CV47	DDR1_DQ0_6/DDR0_DQ2_6/DDR1_DQ0_6	
M_0_DQ_2<5>	CT45	DDR1_DQ0_5/DDR0_DQ2_5/DDR1_DQ0_5	
M_0_DQ_2<4>	CV45	DDR1_DQ0_4/DDR0_DQ2_4/DDR1_DQ0_4	
M_0_DQ_2<3>	CT42	DDR1_DQ0_3/DDR0_DQ2_3/DDR1_DQ0_3	
M_0_DQ_2<2>	CV42	DDR1_DQ0_2/DDR0_DQ2_2/DDR1_DQ0_2	
M_0_DQ_2<1>	CT41	DDR1_DQ0_1/DDR0_DQ2_1/DDR1_DQ0_1	
M_0_DQ_2<0>	CV41	DDR1_DQ0_0/DDR0_DQ2_0/DDR1_DQ0_0	
M_0_DQ_3<7>	CK47	DDR1_DQ1_7/DDR0_DQ3_7/DDR1_DQ1_7	
M_0_DQ_3<6>	CM47	DDR1_DQ1_6/DDR0_DQ3_6/DDR1_DQ1_6	
M_0_DQ_3<5>	CK45	DDR1_DQ1_5/DDR0_DQ3_5/DDR1_DQ1_5	
M_0_DQ_3<4>	CM45	DDR1_DQ1_4/DDR0_DQ3_4/DDR1_DQ1_4	
M_0_DQ_3<3>	CK42	DDR1_DQ1_3/DDR0_DQ3_3/DDR1_DQ1_3	
M_0_DQ_3<2>	CM42	DDR1_DQ1_2/DDR0_DQ3_2/DDR1_DQ1_2	
M_0_DQ_3<1>	CM41	DDR1_DQ1_1/DDR0_DQ3_1/DDR1_DQ1_1	
M_0_DQ_3<0>	CK41	DDR1_DQ1_0/DDR0_DQ3_0/DDR1_DQ1_0	
M_0_DQ_4<7>	BF53	LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)	
M_0_DQ_4<6>	BF52	DDR2_DQ0_7/DDR0_DQ4_7/DDR0_DQ2_7	
M_0_DQ_4<5>	BF50	DDR2_DQ0_6/DDR0_DQ4_6/DDR0_DQ2_6	
M_0_DQ_4<4>	BF49	DDR2_DQ0_5/DDR0_DQ4_5/DDR0_DQ2_5	
M_0_DQ_4<3>	BH53	DDR2_DQ0_4/DDR0_DQ4_4/DDR0_DQ2_4	
M_0_DQ_4<2>	BH52	DDR2_DQ0_3/DDR0_DQ4_3/DDR0_DQ2_3	
M_0_DQ_4<1>	BH50	DDR2_DQ0_2/DDR0_DQ4_2/DDR0_DQ2_2	
M_0_DQ_4<0>	BH49	DDR2_DQ0_1/DDR0_DQ4_1/DDR0_DQ2_1	
M_0_DQ_5<7>	AY53	DDR2_DQ0_0/DDR0_DQ4_0/DDR0_DQ2_0	
M_0_DQ_5<6>	AY52	DDR2_DQ1_7/DDR0_DQ5_7/DDR0_DQ3_7	
M_0_DQ_5<5>	AY50	DDR2_DQ1_6/DDR0_DQ5_6/DDR0_DQ3_6	
M_0_DQ_5<4>	AY49	DDR2_DQ1_5/DDR0_DQ5_5/DDR0_DQ3_5	
M_0_DQ_5<3>	BC53	DDR2_DQ1_4/DDR0_DQ5_4/DDR0_DQ3_4	
M_0_DQ_5<2>	BC52	DDR2_DQ1_3/DDR0_DQ5_3/DDR0_DQ3_3	
M_0_DQ_5<1>	BC50	DDR2_DQ1_2/DDR0_DQ5_2/DDR0_DQ3_2	
M_0_DQ_5<0>	BC49	DDR2_DQ1_1/DDR0_DQ5_1/DDR0_DQ3_1	
M_0_DQ_6<7>	BK47	DDR2_DQ1_0/DDR0_DQ5_0/DDR0_DQ3_0	
M_0_DQ_6<6>	BK45	DDR3_DQ0_7/DDR0_DQ6_7/DDR1_DQ2_7	
M_0_DQ_6<5>	BH47	DDR3_DQ0_6/DDR0_DQ6_6/DDR1_DQ2_6	
M_0_DQ_6<4>	BH45	DDR3_DQ0_5/DDR0_DQ6_5/DDR1_DQ2_5	
M_0_DQ_6<3>	BH42	DDR3_DQ0_4/DDR0_DQ6_4/DDR1_DQ2_4	
M_0_DQ_6<2>	BK42	DDR3_DQ0_3/DDR0_DQ6_3/DDR1_DQ2_3	
M_0_DQ_6<1>	BK41	DDR3_DQ0_2/DDR0_DQ6_2/DDR1_DQ2_2	
M_0_DQ_6<0>	BH41	DDR3_DQ0_1/DDR0_DQ6_1/DDR1_DQ2_1	
M_0_DQ_7<7>	BD47	DDR3_DQ0_0/DDR0_DQ6_0/DDR1_DQ2_0	
M_0_DQ_7<6>	BB47	DDR3_DQ1_7/DDR0_DQ7_7/DDR1_DQ3_7	
M_0_DQ_7<5>	BD45	DDR3_DQ1_6/DDR0_DQ7_6/DDR1_DQ3_6	
M_0_DQ_7<4>	BB45	DDR3_DQ1_5/DDR0_DQ7_5/DDR1_DQ3_5	
M_0_DQ_7<3>	BB42	DDR3_DQ1_4/DDR0_DQ7_4/DDR1_DQ3_4	
M_0_DQ_7<2>	BB41	DDR3_DQ1_3/DDR0_DQ7_3/DDR1_DQ3_3	
M_0_DQ_7<1>	BD42	DDR3_DQ1_2/DDR0_DQ7_2/DDR1_DQ3_2	
M_0_DQ_7<0>	BD41	DDR3_DQ1_1/DDR0_DQ7_1/DDR1_DQ3_1	
		DDR3_DQ1_0/DDR0_DQ7_0/DDR1_DQ3_0	

DDR4/LP4/LP5/LP5 CMD Flip

		DDR0_CLK_P1/DDR3_CLK_P/DDR3_CLK_P/DDR3_CLK_P	BT42
		DDR0_CLK_N1/DDR3_CLK_N/DDR3_CLK_N/DDR3_CLK	BT41
		NC/DDR2_CLK_P/DDR2_CLK_P/DDR2_CLK_P	BP52
		NC/DDR2_CLK_N/DDR2_CLK_N/DDR2_CLK	BP53
		NC/DDR1_CLK_P/DDR1_CLK_P/DDR1_CLK_P	CD42
		NC/DDR1_CLK_N/DDR1_CLK_N/DDR1_CLK	CD41
		DDR0_CLK_P0/DDR0_CLK_P/DDR0_CLK_P/DDR0_CLK_P	CC52
		DDR0_CLK_N0/DDR0_CLK_N/DDR0_CLK_N/DDR0_CLK	CC53
		DDR4/LP4/LP5/LP5 CMD Flip	
		NC/DDR3_CKE0/DDR3_WCK_P/DDR3_WCK_P	BT45
		NC/DDR3_CKE1/DDR3_WCK_N/DDR3_WCK	BT47
		NC/DDR2_CKE0/DDR2_WCK_P/DDR2_WCK_P	BN51
		NC/DDR2_CKE1/DDR2_WCK_N/DDR2_WCK	BN53
		NC/DDR1_CKE0/DDR1_WCK_P/DDR1_WCK_P	CD45
		NC/DDR1_CKE1/DDR1_WCK_N/DDR1_WCK	CD47
		NC/DDR0_CKE0/DDR0_WCK_P/DDR0_WCK_P	CA51
		NC/DDR0_CKE1/DDR0_WCK_N/DDR0_WCK	CA53
		DDR4/LP4/LP5/LP5 CMD Flip	
		DDR0_CKE1/DDR2_CA4/DDR2_CA5/DDR2_CA1	BU52
		DDR0_CKE0/DDR2_CA5/DDR2_CA6/DDR2_CA0	BL50
		DDR4/LP4/LP5/LP5 CMD Flip	
		DDR0_CS1/DDR1_CA1/DDR1_CA1/DDR1_CA5	CF42
		DDR0_CS0/NC/DDR1_CS1/DDR1_CA4	CF47
		DDR4/LP4/LP5/LP5 CMD Flip	
		NC/DDR0_CA0/DDR0_CA0/DDR0_CA6	CE53
		NC/DDR0_CA1/DDR0_CA1/DDR0_CA5	CE50
		NC/DDR2_CS0/DDR2_CA2/DDR2_CA2	BL53
		NC/DDR3_CA5/DDR3_CA6/DDR3_CA0	BP47
		NC/DDR3_CA4/DDR3_CA5/DDR3_CA1	BP42
		NC/DDR3_CA3/DDR3_CA4/DDR3_CS1	BP45
		NC/DDR3_CA2/DDR3_CA3/DDR3_CS0	BP44
		LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)	
		DDR3_DQSP_1/DDR0_DQSP_7/DDR1_DQSP_3	BB44
		DDR3_DQSN_1/DDR0_DQSN_7/DDR1_DQSN_3	BD44
		DDR3_DQSP_0/DDR0_DQSP_6/DDR1_DQSP_2	BK44
		DDR3_DQSN_0/DDR0_DQSN_6/DDR1_DQSN_2	BH44
		DDR2_DQSP_1/DDR0_DQSP_5/DDR0_DQSP_3	BA51
		DDR2_DQSN_1/DDR0_DQSN_5/DDR0_DQSN_3	BA50
		DDR2_DQSP_0/DDR0_DQSP_4/DDR0_DQSP_2	BG51
		DDR2_DQSN_0/DDR0_DQSN_4/DDR0_DQSN_2	BG50
		DDR1_DQSP_1/DDR0_DQSP_3/DDR1_DQSP_1	CK44
		DDR1_DQSN_1/DDR0_DQSN_3/DDR1_DQSN_1	CM44
		DDR1_DQSP_0/DDR0_DQSP_2/DDR1_DQSP_0	CT44
		DDR1_DQSN_0/DDR0_DQSN_2/DDR1_DQSN_0	CV44
		DDR0_DQSP_1/DDR0_DQSP_1/DDR0_DQSP_1	CK51
		DDR0_DQSN_1/DDR0_DQSN_1/DDR0_DQSN_1	CK50
		DDR0_DQSP_0/DDR0_DQSP_0/DDR0_DQSP_0	CR51
		DDR0_DQSN_0/DDR0_DQSN_0/DDR0_DQSN_0	CR50
		DDR4/LP4/LP5/LP5 CMD Flip	
		DDR0_ODT1/DDR1_CA0/DDR1_CA0/DDR1_CA6	CF44
		DDR0_ODT0/DDR1_CS0/DDR1_CA2/DDR1_CA2	CF45
		DDR4/LP4/LP5/LP5 CMD Flip	
		DDR0_MA16/DDR1_CA4/DDR1_CA5/DDR1_CA1	CB47
		DDR0_MA15/DDR1_CA3/DDR1_CA4/DDR1_CS1	CB44
		DDR0_MA14/DDR1_CA2/DDR1_CA3/DDR1_CS0	CB45
		DDR0_MA13/DDR1_CS1/DDR1_CS0/DDR1_CA3	CF41
		DDR0_MA12/DDR2_CA1/DDR2_CA1/DDR2_CA5	BU53
		DDR0_MA11/NC/DDR2_CS1/DDR2_CA4	BT51
		DDR0_MA10/DDR3_CA1/DDR3_CA1/DDR3_CA5	BV42
		DDR0_MA9/DDR2_CA0/DDR2_CA0/DDR2_CA6	BU50
		DDR0_MA8/DDR0_CA2/DDR0_CA3/DDR0_CS0	BY53
		DDR0_MA7/DDR0_CA4/DDR0_CA5/DDR0_CA1	CA50
		DDR0_MA6/DDR0_CA3/DDR0_CA4/DDR0_CS1	BY52
		DDR0_MA5/DDR0_CA5/DDR0_CA6/DDR0_CA0	BY50
		DDR0_MA4/DDR0_CS0/DDR0_CA2/DDR0_CA2	CD51
		DDR0_MA3/DDR0_CS1/DDR0_CS0/DDR0_CA3	CD53
		DDR0_MA2/DDR3_CS0/DDR3_CA2/DDR3_CA2	BV47
		DDR0_MA1/NC/DDR0_CS1/DDR0_CA4	CE52
		DDR0_MA0/NC/DDR3_CS1/DDR3_CA4	BV41
		DDR4/LP4/LP5/LP5 CMD Flip	
		DDR0_BG1/DDR2_CA2/DDR2_CA3/DDR2_CS0	BN50
		DDR0_BG0/DDR2_CA3/DDR2_CA4/DDR2_CS1	BL52
		DDR4/LP4/LP5/LP5 CMD Flip	
		DDR0_BA1/DDR1_CA5/DDR1_CA6/DDR1_CA0	CB42
		DDR0_BA0/DDR3_CA0/DDR3_CA0/DDR3_CA6	BV44
		DDR4/LP4/LP5/LP5 CMD Flip	
		DDR0_ACT#/DDR2_CS1/DDR2_CS0/DDR2_CA3	BT53
		DDR4/LP4/LP5/LP5 CMD Flip	
		DDR0_PAR/DDR3_CS1/DDR3_CS0/DDR3_CA3	BV45
		DDR0_ALERT#	AU50
		DDR0_VREF_CA	AU49
		DDR_VTT_CTL	E52
		DRAM_RESET#	DV47
		DDR_RCOMP	C49

TGL_UP3_IP_EXT/BGA

+VDDQ

R502 470 1% RES 0201

CAD NOTE:

DDR_RCOMP RDC SHOULD BE <0.5 OHMS
MAIN ROUTE TRACE SPACING OF 500UM (FOR U ONLY)

PLACE R501 AS CLOSE AS POSSIBLE TO MCP

0201 5% R503 RES

DRAM_RESET_N_R

30,32

0201 1% 100 R501 RES

0

M_0_CLK_DDR1_DP
M_0_CLK_DDR1_DN
TP_PG5_CD42
TP_PG5_CD41
M_0_CLK_DDR0_DP
M_0_CLK_DDR0_DN
TP_PG5_BT45
TP_PG5_BT47
TP_PG5_CD45
TP_PG5_CD47
TP_PG5_CA53
M_0_CKE_1
M_0_CKE_0
M_0_CS1_N
M_0_CS0_N
TP_PG5_CE53
TP_PG5_CE50
TP_PG5_BL53
TP_PG5_BP47
TP_PG5_BP42
TP_PG5_BP45
TP_PG5_BP44
M_0_DQS_7_DP
M_0_DQS_7_DN
M_0_DQS_6_DP
M_0_DQS_6_DN
M_0_DQS_5_DP
M_0_DQS_5_DN
M_0_DQS_4_DP
M_0_DQS_4_DN
M_0_DQS_3_DP
M_0_DQS_3_DN
M_0_DQS_2_DP
M_0_DQS_2_DN
M_0_DQS_1_DP
M_0_DQS_1_DN
M_0_DQS_0_DP
M_0_DQS_0_DN
M_0_ODT1
M_0_ODT0
M_0_MA16_RAS_N
M_0_MA15_CAS_N
M_0_MA14_WE_N
M_0_MA13
M_0_MA12
M_0_MA11
M_0_MA10
M_0_MA9
M_0_MA8
M_0_MA7
M_0_MA6
M_0_MA5
M_0_MA4
M_0_MA3
M_0_MA2
M_0_MA1
M_0_MA0
M_0_BG1
M_0_BG0
M_0_BA1
M_0_BA0
M_0_ACT_N
M_0_PARITY
M_0_ALERT_N
+V_DACH0_CA_VREF
DDR_VTT_CTRL
DRAM_RESET_N
DDR_COMP_0

MODULE REV DETAILS

MODULE NAME	REV	DATE

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MODULE REV DETAILS		
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TGL_UP3_IP_EXT/BGA

M_1_DQ_0<7>	AL53	DDR4_DQ0_7/DDR1_DQ0_7/DDR0_DQ4_7	LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)			
M_1_DQ_0<6>	AL52	DDR4_DQ0_6/DDR1_DQ0_6/DDR0_DQ4_6				
M_1_DQ_0<5>	AL50	DDR4_DQ0_5/DDR1_DQ0_5/DDR0_DQ4_5				
M_1_DQ_0<4>	AL49	DDR4_DQ0_4/DDR1_DQ0_4/DDR0_DQ4_4				
M_1_DQ_0<3>	AP53	DDR4_DQ0_3/DDR1_DQ0_3/DDR0_DQ4_3				
M_1_DQ_0<2>	AP52	DDR4_DQ0_2/DDR1_DQ0_2/DDR0_DQ4_2				
M_1_DQ_0<1>	AP50	DDR4_DQ0_1/DDR1_DQ0_1/DDR0_DQ4_1				
M_1_DQ_0<0>	AP49	DDR4_DQ0_0/DDR1_DQ0_0/DDR0_DQ4_0				
M_1_DQ_1<7>	AF53	DDR4_DQ1_7/DDR1_DQ1_7/DDR0_DQ5_7				
M_1_DQ_1<6>	AF52	DDR4_DQ1_6/DDR1_DQ1_6/DDR0_DQ5_6				
M_1_DQ_1<5>	AF50	DDR4_DQ1_5/DDR1_DQ1_5/DDR0_DQ5_5				
M_1_DQ_1<4>	AF49	DDR4_DQ1_4/DDR1_DQ1_4/DDR0_DQ5_4				
M_1_DQ_1<3>	AH53	DDR4_DQ1_3/DDR1_DQ1_3/DDR0_DQ5_3				
M_1_DQ_1<2>	AH52	DDR4_DQ1_2/DDR1_DQ1_2/DDR0_DQ5_2				
M_1_DQ_1<1>	AH50	DDR4_DQ1_1/DDR1_DQ1_1/DDR0_DQ5_1				
M_1_DQ_1<0>	AH49	DDR4_DQ1_0/DDR1_DQ1_0/DDR0_DQ5_0				
M_1_DQ_2<7>	AR41	DDR5_DQ0_7/DDR1_DQ2_7/DDR1_DQ4_7				
M_1_DQ_2<6>	AV42	DDR5_DQ0_6/DDR1_DQ2_6/DDR1_DQ4_6	DDR4/LP4/LP5/LP5 CMD Flip			
M_1_DQ_2<5>	AR42	DDR5_DQ0_5/DDR1_DQ2_5/DDR1_DQ4_5				
M_1_DQ_2<4>	AV41	DDR5_DQ0_4/DDR1_DQ2_4/DDR1_DQ4_4				
M_1_DQ_2<3>	AR45	DDR5_DQ0_3/DDR1_DQ2_3/DDR1_DQ4_3				
M_1_DQ_2<2>	AV45	DDR5_DQ0_2/DDR1_DQ2_2/DDR1_DQ4_2				
M_1_DQ_2<1>	AR47	DDR5_DQ0_1/DDR1_DQ2_1/DDR1_DQ4_1				
M_1_DQ_2<0>	AV47	DDR5_DQ0_0/DDR1_DQ2_0/DDR1_DQ4_0	DDR4/LP4/LP5/LP5 CMD Flip			
M_1_DQ_3<7>	AJ41	DDR5_DQ1_7/DDR1_DQ3_7/DDR1_DQ5_7				
M_1_DQ_3<6>	AJ42	DDR5_DQ1_6/DDR1_DQ3_6/DDR1_DQ5_6				
M_1_DQ_3<5>	AL41	DDR5_DQ1_5/DDR1_DQ3_5/DDR1_DQ5_5				
M_1_DQ_3<4>	AL42	DDR5_DQ1_4/DDR1_DQ3_4/DDR1_DQ5_4				
M_1_DQ_3<3>	AJ45	DDR5_DQ1_3/DDR1_DQ3_3/DDR1_DQ5_3				
M_1_DQ_3<2>	AJ47	DDR5_DQ1_2/DDR1_DQ3_2/DDR1_DQ5_2				
M_1_DQ_3<1>	AL45	DDR5_DQ1_1/DDR1_DQ3_1/DDR1_DQ5_1				
M_1_DQ_3<0>	AL47	DDR5_DQ1_0/DDR1_DQ3_0/DDR1_DQ5_0	LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)			
M_1_DQ_4<7>	A43	DDR6_DQ0_7/DDR1_DQ4_7/DDR0_DQ6_7				
M_1_DQ_4<6>	B43	DDR6_DQ0_6/DDR1_DQ4_6/DDR0_DQ6_6				
M_1_DQ_4<5>	D43	DDR6_DQ0_5/DDR1_DQ4_5/DDR0_DQ6_5				
M_1_DQ_4<4>	E44	DDR6_DQ0_4/DDR1_DQ4_4/DDR0_DQ6_4				
M_1_DQ_4<3>	A46	DDR6_DQ0_3/DDR1_DQ4_3/DDR0_DQ6_3				
M_1_DQ_4<2>	B46	DDR6_DQ0_2/DDR1_DQ4_2/DDR0_DQ6_2				
M_1_DQ_4<1>	D46	DDR6_DQ0_1/DDR1_DQ4_1/DDR0_DQ6_1				
M_1_DQ_4<0>	E47	DDR6_DQ0_0/DDR1_DQ4_0/DDR0_DQ6_0				
M_1_DQ_5<7>	E38	DDR6_DQ1_7/DDR1_DQ5_7/DDR0_DQ7_7				
M_1_DQ_5<6>	D38	DDR6_DQ1_6/DDR1_DQ5_6/DDR0_DQ7_6				
M_1_DQ_5<5>	B38	DDR6_DQ1_5/DDR1_DQ5_5/DDR0_DQ7_5				
M_1_DQ_5<4>	A38	DDR6_DQ1_4/DDR1_DQ5_4/DDR0_DQ7_4				
M_1_DQ_5<3>	E41	DDR6_DQ1_3/DDR1_DQ5_3/DDR0_DQ7_3				
M_1_DQ_5<2>	D40	DDR6_DQ1_2/DDR1_DQ5_2/DDR0_DQ7_2				
M_1_DQ_5<1>	B40	DDR6_DQ1_1/DDR1_DQ5_1/DDR0_DQ7_1				
M_1_DQ_5<0>	A40	DDR6_DQ1_0/DDR1_DQ5_0/DDR0_DQ7_0				
M_1_DQ_6<7>	G42	DDR7_DQ0_7/DDR1_DQ6_7/DDR1_DQ6_7	DDR4/LP4/LP5/LP5 CMD Flip			
M_1_DQ_6<6>	G41	DDR7_DQ0_6/DDR1_DQ6_6/DDR1_DQ6_6				
M_1_DQ_6<5>	J41	DDR7_DQ0_5/DDR1_DQ6_5/DDR1_DQ6_5				
M_1_DQ_6<4>	J42	DDR7_DQ0_4/DDR1_DQ6_4/DDR1_DQ6_4				
M_1_DQ_6<3>	G45	DDR7_DQ0_3/DDR1_DQ6_3/DDR1_DQ6_3				
M_1_DQ_6<2>	J45	DDR7_DQ0_2/DDR1_DQ6_2/DDR1_DQ6_2				
M_1_DQ_6<1>	G47	DDR7_DQ0_1/DDR1_DQ6_1/DDR1_DQ6_1				
M_1_DQ_6<0>	J47	DDR7_DQ0_0/DDR1_DQ6_0/DDR1_DQ6_0				
M_1_DQ_7<7>	G38	DDR7_DQ1_7/DDR1_DQ7_7/DDR1_DQ7_7				
M_1_DQ_7<6>	G36	DDR7_DQ1_6/DDR1_DQ7_6/DDR1_DQ7_6				
M_1_DQ_7<5>	H36	DDR7_DQ1_5/DDR1_DQ7_5/DDR1_DQ7_5				
M_1_DQ_7<4>	H38	DDR7_DQ1_4/DDR1_DQ7_4/DDR1_DQ7_4				
M_1_DQ_7<3>	N36	DDR7_DQ1_3/DDR1_DQ7_3/DDR1_DQ7_3				
M_1_DQ_7<2>	L36	DDR7_DQ1_2/DDR1_DQ7_2/DDR1_DQ7_2				
M_1_DQ_7<1>	L38	DDR7_DQ1_1/DDR1_DQ7_1/DDR1_DQ7_1				
M_1_DQ_7<0>	N38	DDR7_DQ1_0/DDR1_DQ7_0/DDR1_DQ7_0				

DDR4/LP4/LP5/LP5 CMD Flip			
DDR1_CLK_P1/DDR7_CLK_P/DDR7_CLK_P/DDR7_CLK_P	R41	M_1_CLK_DDR1_DP	32
DDR1_CLK_N1/DDR7_CLK_N/DDR7_CLK_N/DDR7_CLK	R42	M_1_CLK_DDR1_DN	32
NC/DDR6_CLK_P/DDR6_CLK_P/DDR6_CLK_P	M52	TP_PG6_M52	
NC/DDR6_CLK_N/DDR6_CLK_N/DDR6_CLK	M53	TP_PG6_M53	
NC/DDR5_CLK_P/DDR5_CLK_P/DDR5_CLK_P	AC42	TP_PG6_AC42	
NC/DDR5_CLK_N/DDR5_CLK_N/DDR5_CLK	AC41	TP_PG6_AC41	
DDR1_CLK_P0/DDR4_CLK_P/DDR4_CLKP/DDR4_CLK_P	Y52	M_1_CLK_DDR0_DP	32
DDR1_CLK_N0/DDR4_CLK_N/DDR4_CLK_N/DDR4_CLK	Y53	M_1_CLK_DDR0_DN	32
DDR4/LP4/LP5/LP5 CMD Flip			
NC/DDR7_CKE0/DDR7_WCK_P/DDR7_WCK_P	BJ47		
NC/DDR7_CKE1/DDR7_WCK_N/DDR7_WCK	BJ45		
NC/DDR6_CKE0/DDR6_WCK_P/DDR6_WCK_P	K51	TP_PG6_K51	
NC/DDR6_CKE1/DDR6_WCK_N/DDR6_WCK	K53	TP_PG6_K53	
NC/DDR5_CKE0/DDR5_WCK_P/DDR5_WCK_P	AC47	TP_PG6_AC47	
NC/DDR5_CKE1/DDR5_WCK_N/DDR5_WCK	AC45	TP_PG6_AC45	
NC/DDR4_CKE0/DDR4_WCK_P/DDR4_WCK_P	W51	TP_PG6_W51	
NC/DDR4_CKE1/DDR4_WCK_N/DDR4_WCK	W53	TP_PG6_W53	
DDR4/LP4/LP5/LP5 CMD Flip			
DDR1_CKE1/DDR6_CA4/DDR6_CA5/DDR6_CA1	P52	M_1_CKE_1	
DDR1_CKE0/DDR6_CA5/DDR6_CA6/DDR6_CA0	J50	M_1_CKE_0	32
DDR4/LP4/LP5/LP5 CMD Flip			32
DDR1_CS1/DDR5_CA1/DDR5_CA1/DDR5_CA5	AE42	M_1_CS1_N	
DDR1_CS0/NC/DDR5_CS1/DDR5_CA4	AE47	M_1_CS0_N	32
DDR4/LP4/LP5/LP5 CMD Flip			32
NC/DDR7_CA5/DDR7_CA6/DDR7_CA0	N42		
NC/DDR7_CA4/DDR7_CA5/DDR7_CA1	N45		
NC/DDR7_CA3/DDR7_CA4/DDR7_CS1	N44		
NC/DDR7_CA2/DDR7_CA3/DDR7_CS0	N47		
NC/DDR6_CS0/DDR6_CA2/DDR6_CA2	J53	TP_PG6_J53	
NC/DDR4_CA1/DDR4_CA1/DDR4_CA5	AC50		
NC/DDR4_CA0/DDR4_CA0/DDR4_CA6	AC53	TP_PG6_AC53	
LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)			
DDR7_DQSP_1/DDR1_DQSP_7/DDR1_DQSP_7	K36	M_1_DQS_7_DP	32
DDR7_DQSN_1/DDR1_DQSN_7/DDR1_DQSN_7	K38	M_1_DQS_7_DN	32
DDR7_DQSP_0/DDR1_DQSP_6/DDR1_DQSP_6	G44	M_1_DQS_6_DP	32
DDR7_DQSN_0/DDR1_DQSN_6/DDR1_DQSN_6	J44	M_1_DQS_6_DN	32
DDR6_DQSP_1/DDR1_DQSP_5/DDR0_DQSP_7	D39	M_1_DQS_5_DP	32
DDR6_DQSN_1/DDR1_DQSN_5/DDR0_DQSN_7	C39	M_1_DQS_5_DN	32
DDR6_DQSP_0/DDR1_DQSP_4/DDR0_DQSP_6	C45	M_1_DQS_4_DP	32
DDR6_DQSN_0/DDR1_DQSN_4/DDR0_DQSN_6	D45	M_1_DQS_4_DN	32
DDR5_DQSP_1/DDR1_DQSP_3/DDR1_DQSP_5	AJ44	M_1_DQS_3_DP	32
DDR5_DQSN_1/DDR1_DQSN_3/DDR1_DQSN_5	AL44	M_1_DQS_3_DN	32
DDR5_DQSP_0/DDR1_DQSP_2/DDR1_DQSP_4	AV44	M_1_DQS_2_DP	32
DDR5_DQSN_0/DDR1_DQSN_2/DDR1_DQSN_4	AR44	M_1_DQS_2_DN	32
DDR4_DQSP_1/DDR1_DQSP_1/DDR0_DQSP_5	AG51	M_1_DQS_1_DP	32
DDR4_DQSN_1/DDR1_DQSN_1/DDR0_DQSN_5	AG50	M_1_DQS_1_DN	32
DDR4_DQSP_0/DDR1_DQSP_0/DDR0_DQSP_4	AN51	M_1_DQS_0_DP	32
DDR4_DQSN_0/DDR1_DQSN_0/DDR0_DQSN_4	AN50	M_1_DQS_0_DN	32
DDR4/LP4/LP5/LP5 CMD Flip			32
DDR1_ODT1/DDR5_CA0/DDR5_CA0/DDR5_CA6	AE44	M_1_ODT1	
DDR1_ODT0/DDR5_CS0/DDR5_CA2/DDR5_CA2	AE45	M_1_ODT0	32
DDR4/LP4/LP5/LP5 CMD Flip			32
DDR1_MA16/DDR5_CA4/DDR5_CA5/DDR5_CA1	AA47	M_1_MA16_RAS_N	
DDR1_MA15/DDR5_CA3/DDR5_CA4/DDR5_CS1	AA44	M_1_MA15_CAS_N	32
DDR1_MA14/DDR5_CA2/DDR5_CA3/DDR5_CS0	AA45	M_1_MA14_WE_N	32
DDR1_MA13/DDR5_CS1/DDR5_CS0/DDR5_CA3	AE41	M_1_MA13	32
DDR1_MA12/DDR6_CA1/DDR6_CA1/DDR6_CA5	P53	M_1_MA12	32
DDR1_MA11/NC/DDR6_CS1/DDR6_CA4	N51	M_1_MA11	32
DDR1_MA10/DDR7_CA1/DDR7_CA1/DDR7_CA5	U42	M_1_MA10	32
DDR1_MA9/DDR6_CA0/DDR6_CA0/DDR6_CA6	P50	M_1_MA9	32
DDR1_MA8/DDR4_CA2/DDR4_CA3/DDR4_CS0	U53	M_1_MA8	32
DDR1_MA7/DDR4_CA4/DDR4_CA5/DDR4_CA1	W50	M_1_MA7	32
DDR1_MA6/DDR4_CA3/DDR4_CA4/DDR4_CS1	U52	M_1_MA6	32
DDR1_MA5/DDR4_CA5/DDR4_CA6/DDR4_CA0	U50	M_1_MA5	32
DDR1_MA4/DDR4_CS0/DDR4_CA2/DDR4_CA2	AA51	M_1_MA4	32
DDR1_MA3/DDR4_CS1/DDR4_CS0/DDR4_CA3	AA53	M_1_MA3	32
DDR1_MA2/DDR7_CS0/DDR7_CA2/DDR7_CA2	U47	M_1_MA2	32
DDR1_MA1/NC/DDR4_CS1/DDR4_CA4	AC52	M_1_MA1	32
DDR1_MA0/NC/DDR7_CS1/DDR7_CA4	U41	M_1_MA0	32
DDR4/LP4/LP5/LP5 CMD Flip			32
DDR1_BG1/DDR6_CA2/DDR6_CA3/DDR6_CS0	K50	M_1_BG1	
DDR1_BG0/DDR6_CA3/DDR6_CA4/DDR6_CS1	J52	M_1_BG0	32
DDR4/LP4/LP5/LP5 CMD Flip			32
DDR1_BA1/DDR5_CA5/DDR5_CA6/DDR5_CA0	AA42	M_1_BA1	
DDR1_BA0/DDR7_CA0/DDR7_CA0/DDR7_CA6	U44	M_1_BA0	32
			32
DDR1_ACT#/DDR6_CS1/DDR6_CS0/DDR6_CA3	N53	M_1_ACT_N	
			32
DDR1_PAR/DDR7_CS1/DDR7_CS0/DDR7_CA3	U45	M_1_PARITY	
			32
DDR1_ALERT#	AU53	M_1_ALERT_N	
DDR1_VREF_CA	AU52	+V_D4CH1_CA_VREF	32
			36

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MODULE REV DETAILS		
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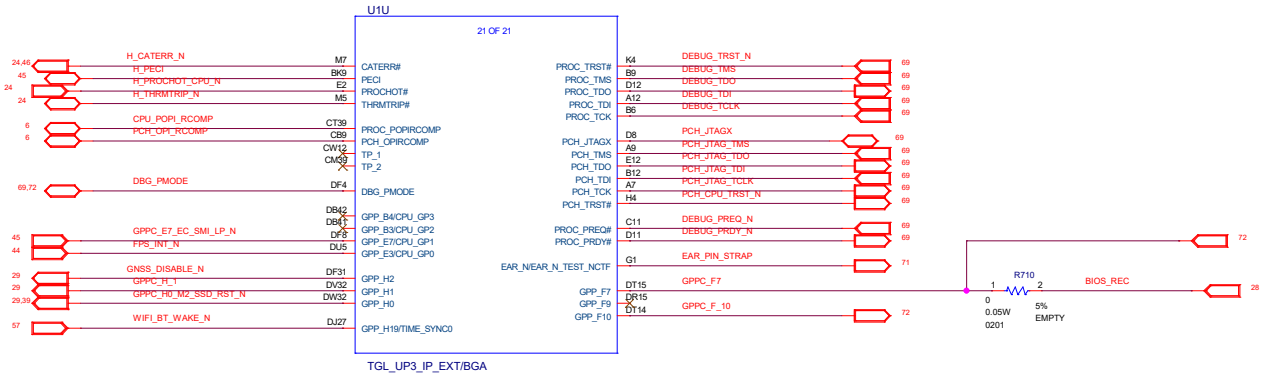
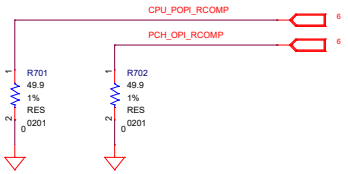
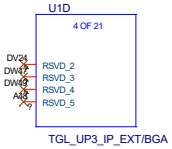




CAD NOTE:

BOTH CPU_POPI_RCOMP AND PCH_POPI_RCOMP RDC SHOULD BE < 0.1 OHM
MAIN ROUTE TRACE SPACING REQUIREMENT IS 300UM (SL/DSL) OR 500UM (MS)



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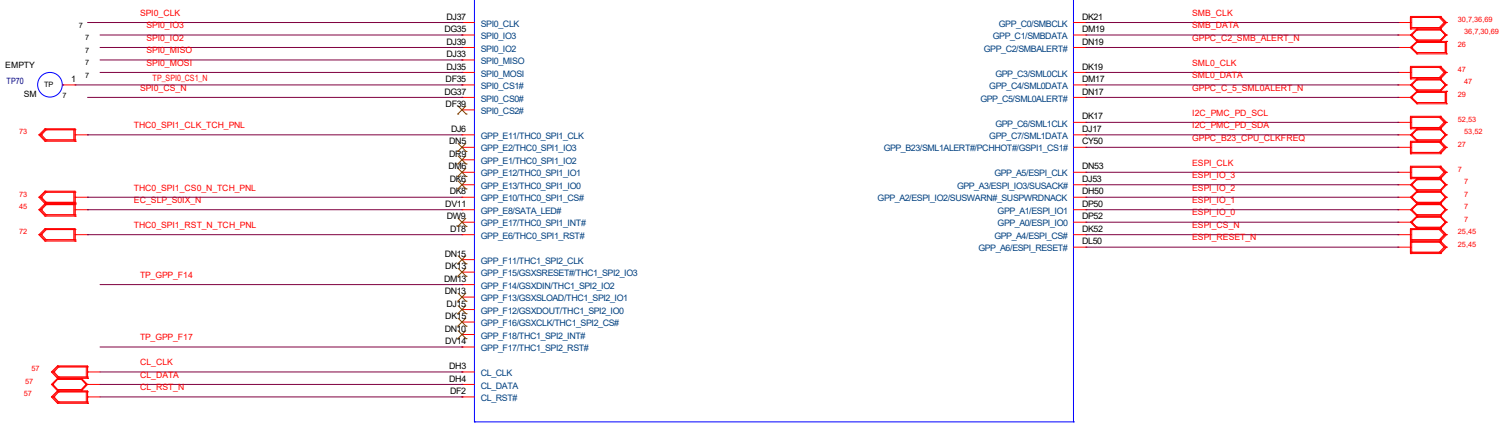
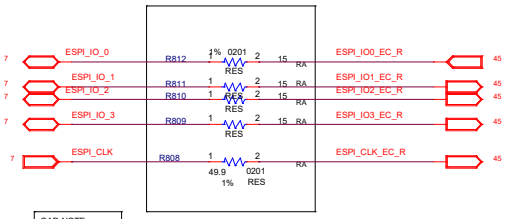
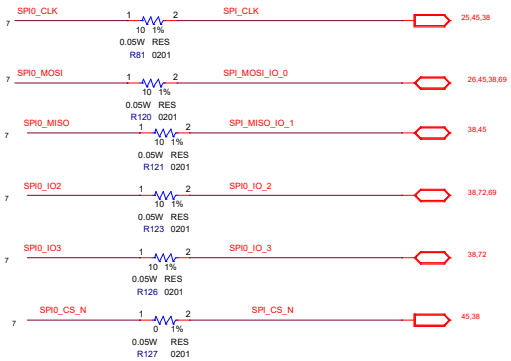


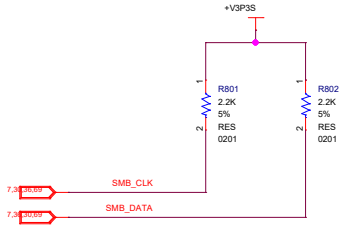
TGL_UP3_IP_EXT/BGA



CAD NOTE:

PLACE ALL ESPI SERIES RESISTORS 'RA' CLOSE TO PCH - WITHIN 25.4MM





BPAGE DRAWING

tgl_u_rd +V3P3.7
Fri Feb 28 13:40:49 2020

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	<DOCUMENT_NUMBER>	7	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

U1F

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TGL_UP3_IP_EXT/BGA

M2_PCH_SSD_PWREN
GPPC_B18_UF_CAM_STROBE
FPS_RST_N
GPPC_B15_WIFI_RF_KILL_N
GSPI1_CLK_R
GSPI1_MOSI_R
GSPI1_MISO_R
GSPI1_CS0_R_N
GPPC_C9_TCH_PAD_RST_N
GPPC_C8_TCH_PAD_INT_N
GPPC_C21_UART2_TXD
GPPC_C20_UART2_RXD
GPPC_C23_UART2_CTS_N
GPPC_C_22_UART2
I2C0_SCL_TCH_PAD
I2C0_SDA_TCH_PAD
I2C3_SCL_RETIMER
I2C3_SDA_RETIMER
WLAN_COEX2
WLAN_COEX1

GPP_B16/GSPI0_CLK
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
GPP_B15/GSPI0_CS0#
GPP_B20/GSPI1_CLK
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B19/GSPI1_CS0#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_H5/I2C2_SCL
GPP_H4/I2C2_SDA
GPP_H7/I2C3_SCL
GPP_H6/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5
GPP_B6/ISH_I2C0_SCL
GPP_B5/ISH_I2C0_SDA
GPP_B8/ISH_I2C1_SCL
GPP_B7/ISH_I2C1_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA
GPP_E16/ISH_GP7
GPP_E15/ISH_GP6
GPP_D18/ISH_GP5
GPP_D17/ISH_GP4
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPP_RCOMP
GPP_T3
GPP_T2
GPP_U5
GPP_U4

CPU_SSD_PWREN
ISH_I2C0_SCL
ISH_I2C0_SDA
I2C1_SCL
I2C1_SDA
PWR_MON_I2C_SCL_R
PWR_MON_I2C_SDA_R
PWR_MON_I2C_SCL
PWR_MON_I2C_SDA
HALL_SENSOR_PCH_IN
ISH_GP_3_HALL_SENSOR_INT
ISH_GP_0_ACCEL_INT
GPPC_RCOMP
TP_GPPC_T_3_I2C7_SCL
TP_GPPC_T_2_I2C7_SDA
TP_GPPC_U_5_GSPI3_CLK
TP_GPPC_U_4_GSPI3_CS0B

R805 0 EMPTY
R806 0 EMPTY
R815 200 1% 0201 EMPTY
R905 200 1% 0201 RES

CAD NOTE:

GPPC_RCOMP RDC SHOULD BE < 0.1
OHM
MAIN ROUTE TRACE SPACING REQUIREMENT IS 100UM

CAD NOTE:

PLACE ALL GSPI SERIES RESISTORS 'RA' CLOSE TO PCH - WITHIN 25.4MM

RA

GSPI1_MOSI_FPS — R904 15 0201 RES — GSPI_MOSI_R
GSPI1_CS0_FPS_N — R906 15 0201 RES — GSPI1_CS0_R_N
GSPI1_CLK_FPS — R907 15 0201 RES — GSPI1_CLK_R
GSPI1_MISO_FPS — R908 15 0201 RES — GSPI1_MISO_R

BPAGE DRAWING

tgl_u_rd.GND
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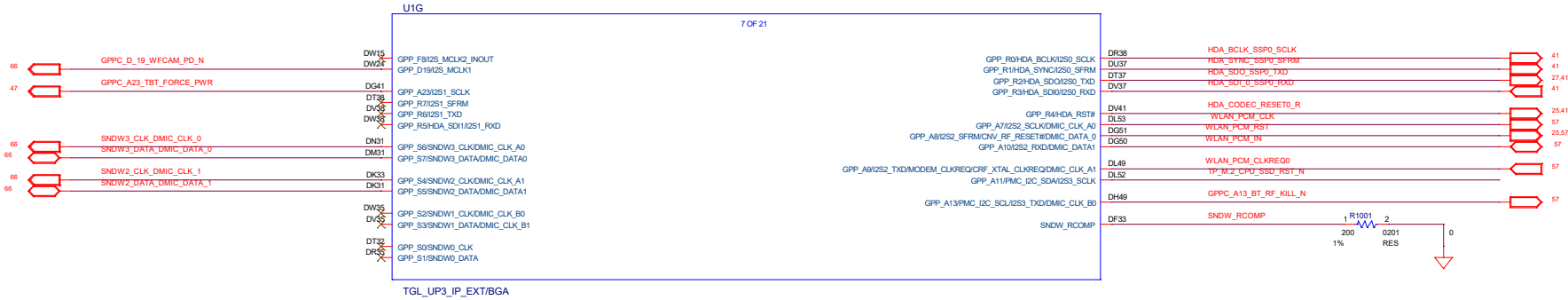
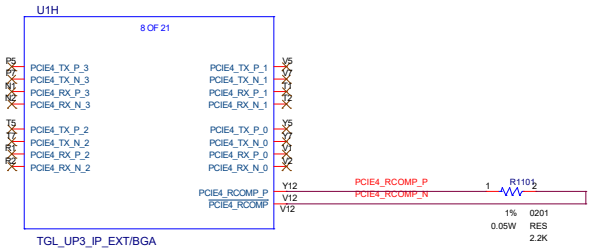
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



CAD NOTE:

SNDW_RCOMP RDC SHOULD BE < 0.1
OHM
MAIN ROUTE TRACE SPACING REQUIREMENT IS 100UM



NOTE [CLOSED CHASSIS] : PCIE GEN4 CPU SSD SUPPORT IS REMOVED

CAD NOTE:

PCIE4 RCOMP CAPACITANCE CANNOT EXCEED 2.5PF FOR EACH NET (P AND N)
THIS INCLUDES ROUTING AND VIA CAPS

BPAGE DRAWING

tgl_u_rd.GND
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

MODULE REV DETAILS		
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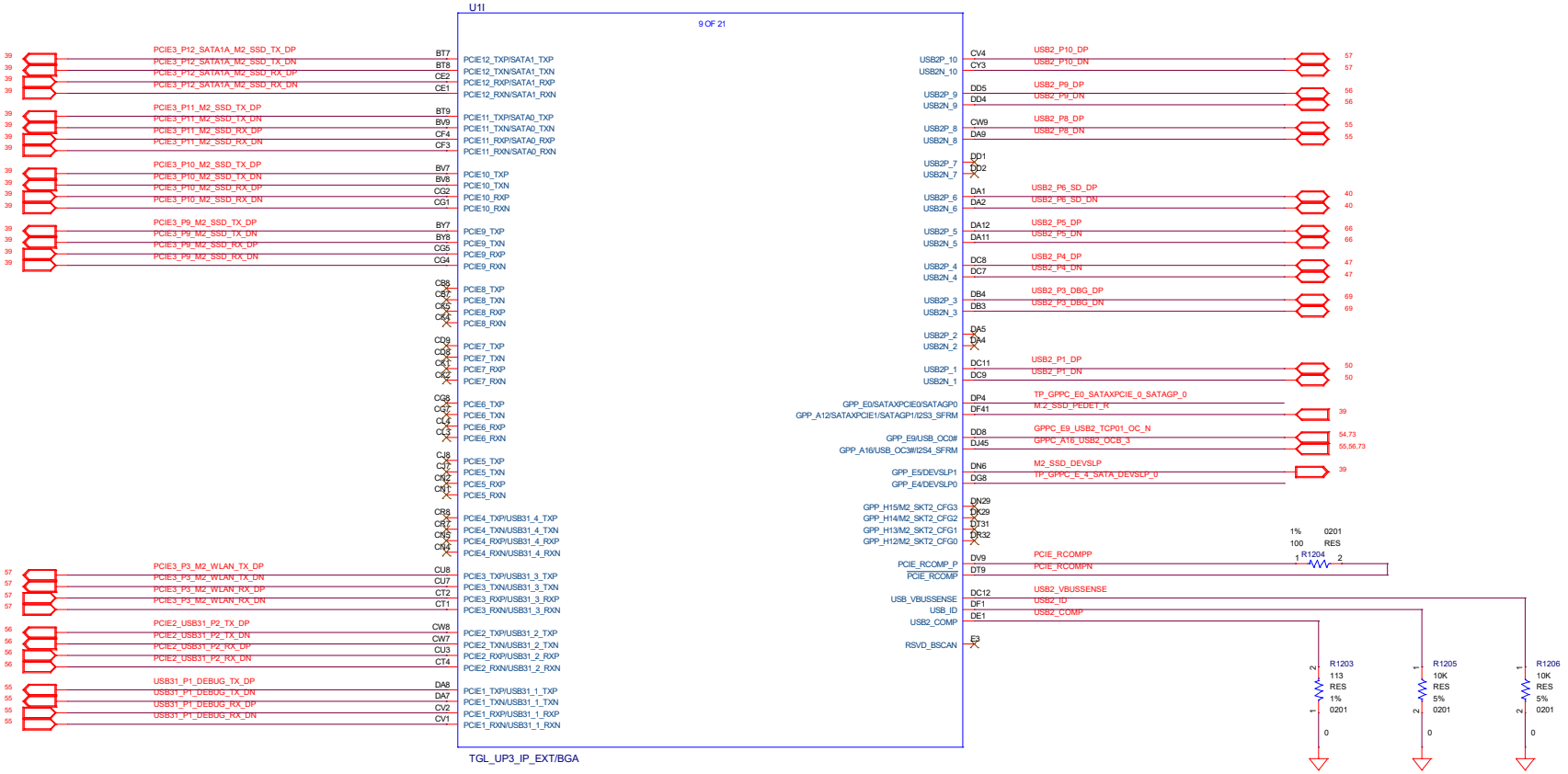

CAD NOTE:

PCIE RCOMP P/N RDC SHOULD BE <0.1 OHM. AVOID ROUTING CLOSE TO ANY CLOCKS. REFERENCE PLANE IS GND

RECOMMENDED PLACING AA VSS SHIELD OF AT LEAST 0.1MM WIDE BETWEEN THE RCOMP SIGNALS AND ANY ADJACENT I/O SIGNAL. MOTHERBOARD LENGTH MATCHING M1-M2=+/-0.127MM

USB2_COMP ROUTE SIGNAL USING 50 OHM SINGLE ENDED IMPEDANCE AND 12.7MM MAX TRACE LENGTH (SHOULD NOT BE LONGER THAN 11.43MM)
AVOID ROUTING NEXT TO CLOCK PINS OR UNDER STITCHING CAPACITORS. RECOMMENDED MINIMUM SPACING TO OTHER SIGNALS TRACES IS 0.381MM

BPAGE DRAWING

tgl_u_rd.GND
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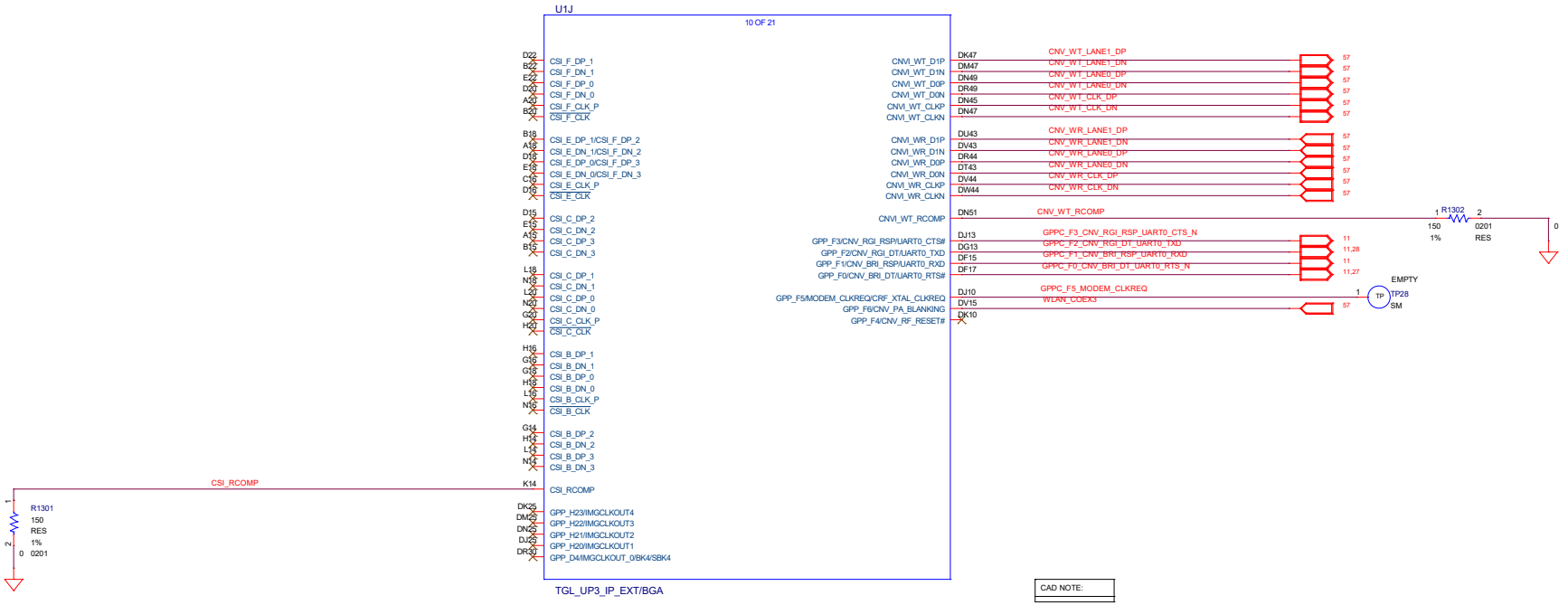
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

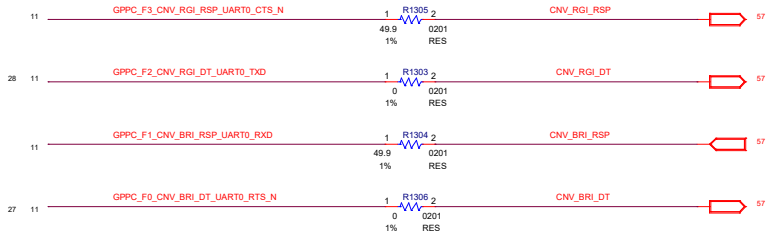


CAD NOTE:

CNVI_RCOMP RDC SHOULD BE < 0.5 OHM.
MAIN ROUTE TRACE SPACING 200 UM.
THESE SIGNALS SHOULD BE REFERENCED TO VSS.
NOISY OR SWITCHING REFERENCES SHOULD BE AVOIDED. IF BOARD SPACE ALLOWS, IT IS RECOMMENDED TO ADD A VSS SHIELD.
CSI_RCOMP RDC SHOULD BE < 0.5 OHM. PROVIDE GOOD NOISE ISOLATION. MAIN ROUTE TRACE SPACING 380UM

CAD NOTE:

PLACE RESISTOR AT 12.7MM FROM THE PCH FOR CNV_BRI_DT AND CNV_RGI_DT
PLACE RESISTOR AT 12.7MM FROM THE CONNECTOR FOR CNV_BRI_RSP AND CNV_RGI_RSP
DISTANCE IN BOTH CASES CAN BE EXTENDED TO 25.4MM



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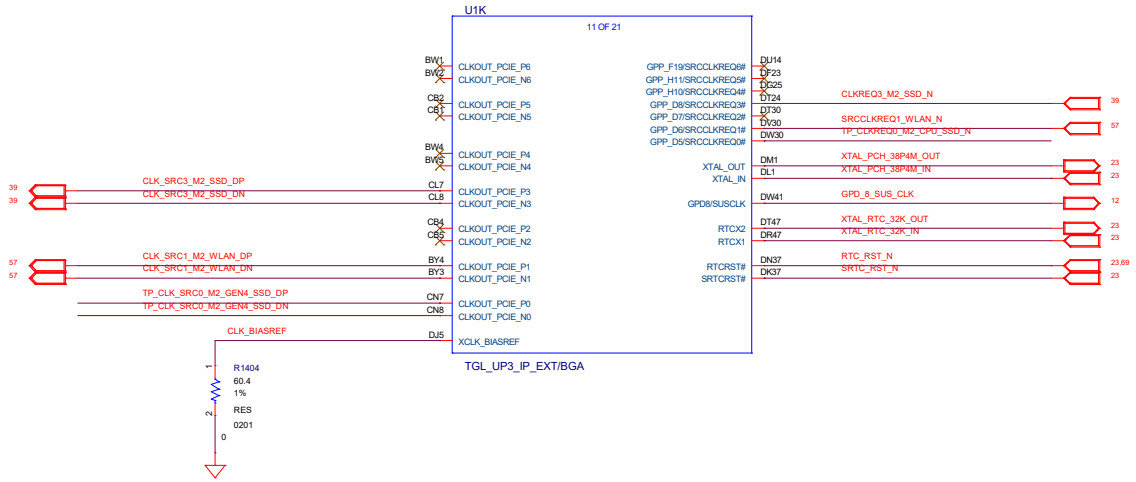
CUSTOM TEXT BPAGE

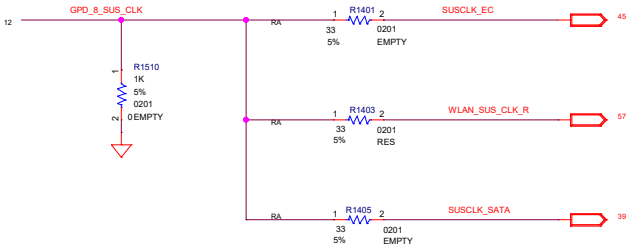
MODULE REV DETAILS		
MODULE NAME	REV	DATE



CAD NOTE:

FOR XCLK_BIASREF REFERENCE PLANE SHOULD BE GND. DC RESISTANCE <0.5 OHM

IF DESIRED ADD A VSS SHIELD OF AT LEAST 0.1016MM WIDE WITH A 6MILS MIN SPACING
ROUTE THIS SIGNAL AS SHORT AS POSSIBLE WHERE THE EXTERNAL SERIES RESISTOR IS PLACED WITHIN 25.4MM FROM PCH



CAD NOTE:

PLACE RA WITHIN 50.8 MM FROM PCH.

BPAGE DRAWING

tgl_u_rd.GND
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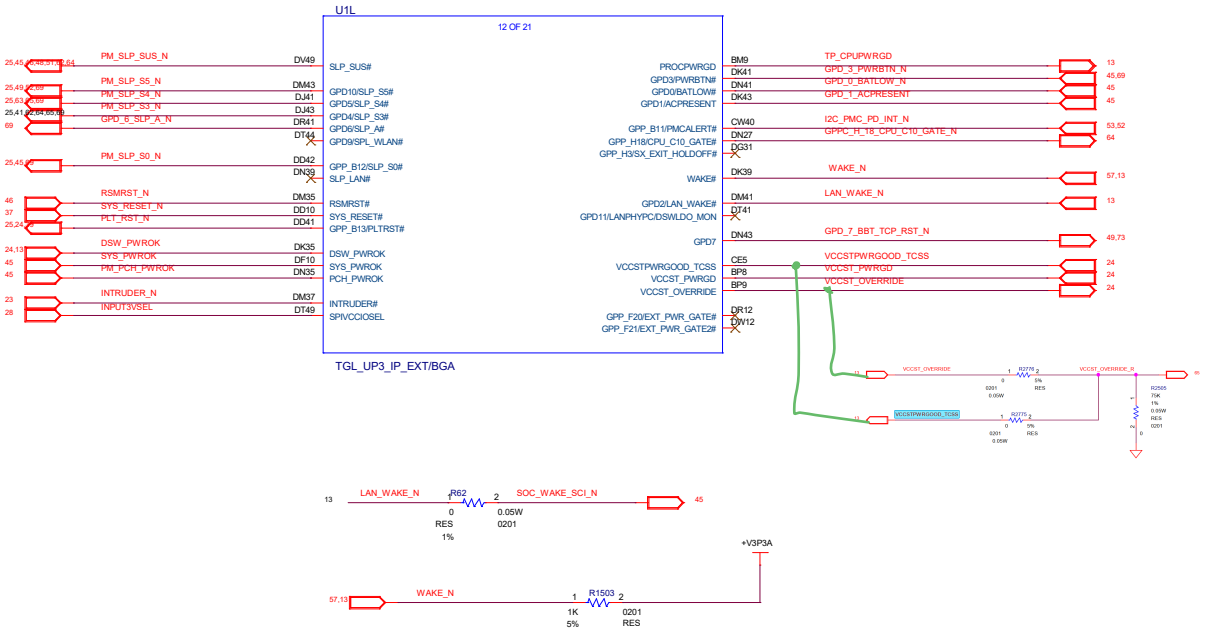

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tgl_u_rd.+V3P3.13
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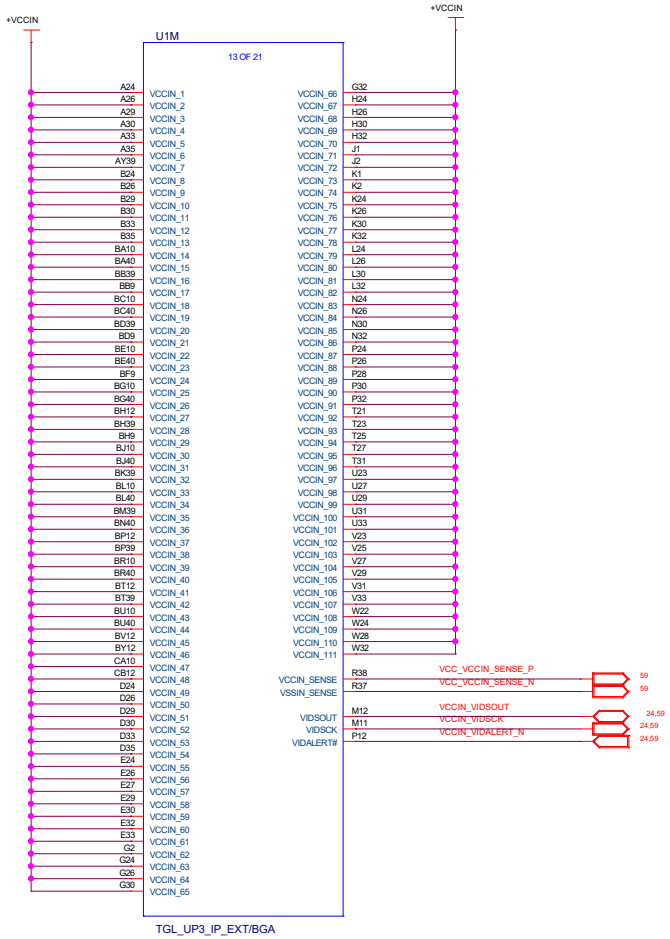
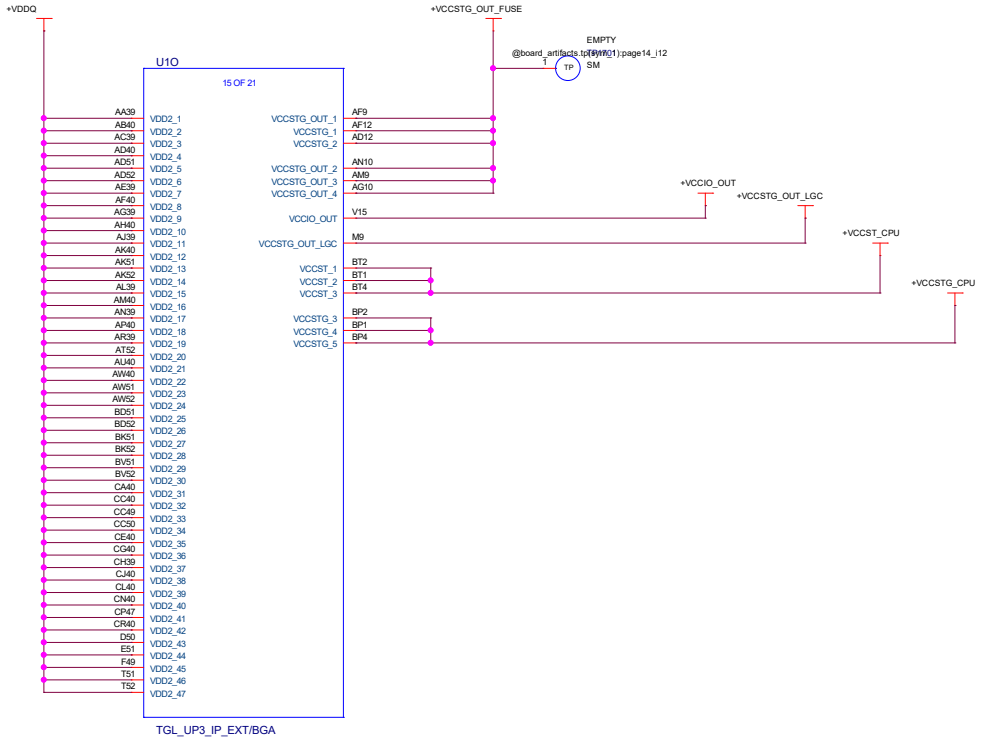
MODULE REV DETAILS		
MODULE NAME	REV	DATE





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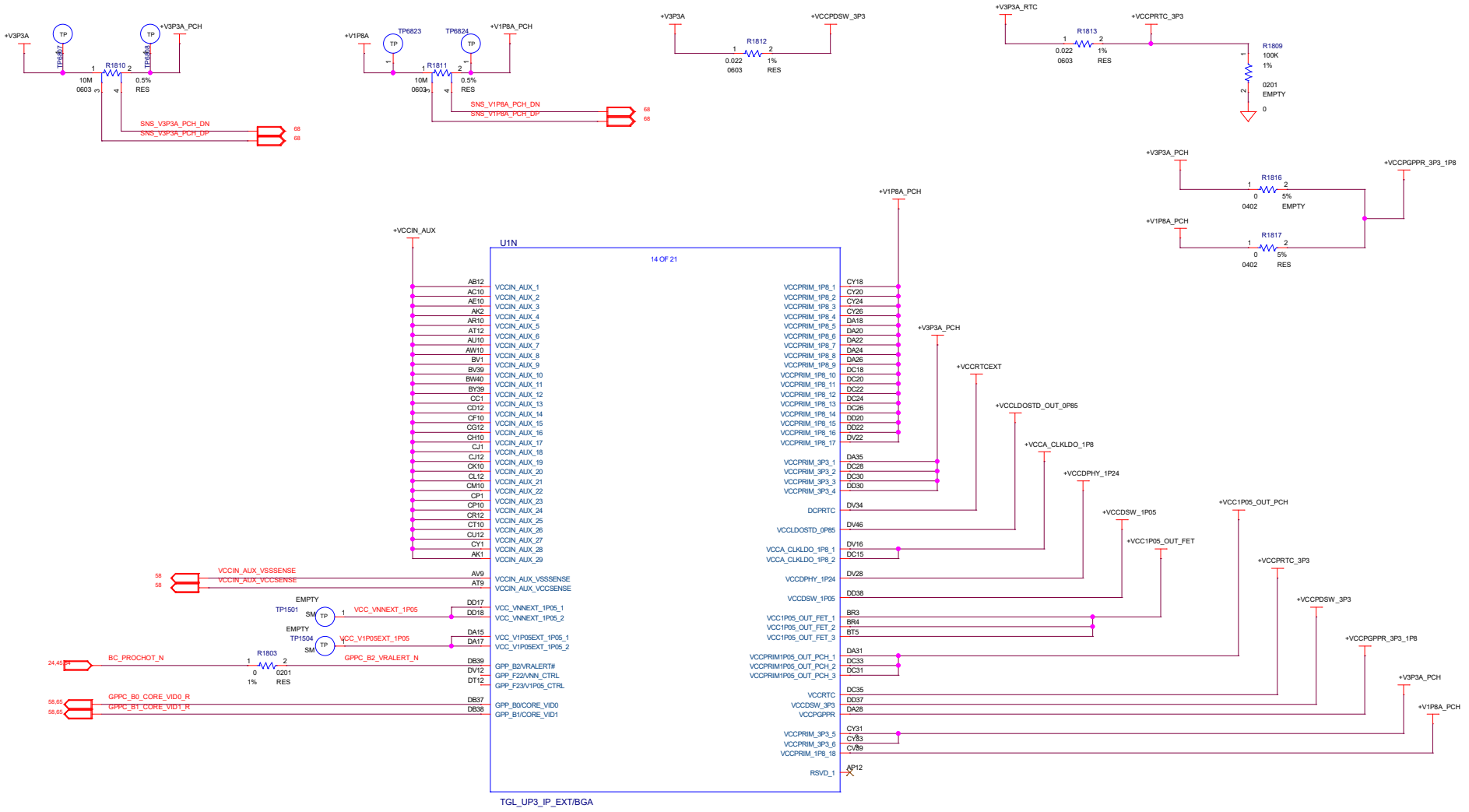
MODULE REV DETAILS		
MODULE NAME	REV	DATE



BPAGE DRAWING

tgl_u_rd.+V1P8.15
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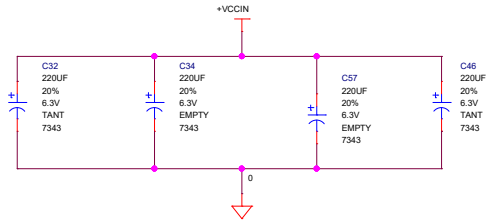
	<DOCUMENT_NUMBER>	15	1P0

CUSTOM TEXT BPAGE

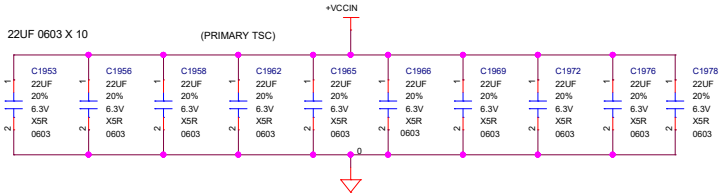
MODULE REV DETAILS		
MODULE NAME	REV	DATE

+VCCIN

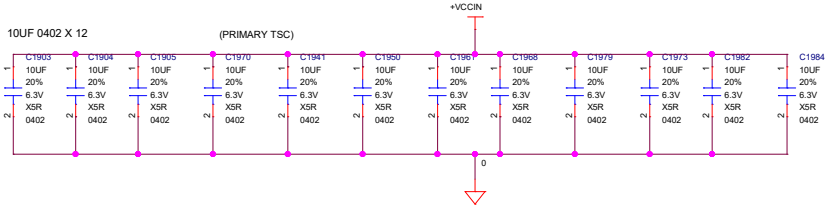
220UF 7343 X 4 (PRIMARY TSC)



22UF 0603 X 10 (PRIMARY TSC)



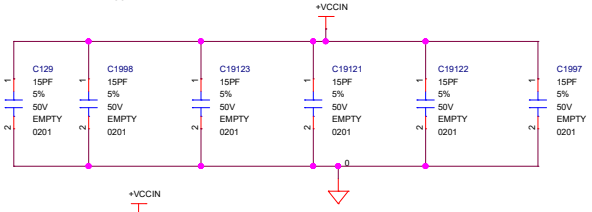
10UF 0402 X 12 (PRIMARY TSC)

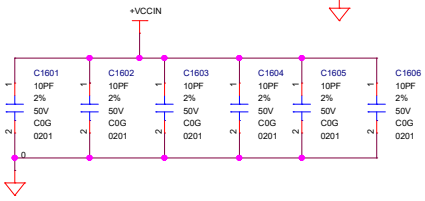


EMC

CAD NOTE:

EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN





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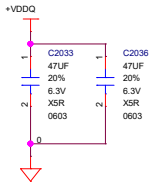
+VDD2_CPU

MODULE REV DETAILS

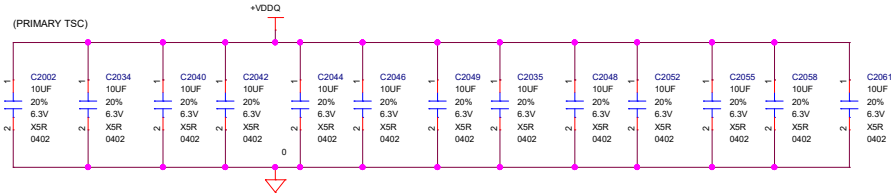
MODULE NAME	REV	DATE

47UF 0603 X2 (PRIMARY TSC)

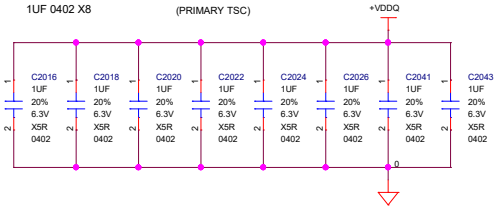


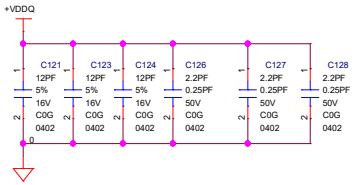
10UF 0402 X13

(PRIMARY TSC)



1UF 0402 X8 (PRIMARY TSC)





CAD NOTE:

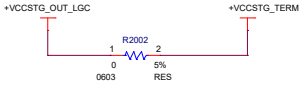
0603 PH ON PRIMARY SIDE. 0402 PH ON SECONDARY SIDE

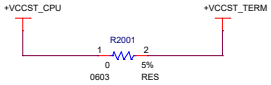
VCCSTG/VCCST

DESIGN NOTE:

FINAL CAP COUNT WILL BE PUBLISHED

IN REV 0.7 IPDS. NEED TO BE CHECKED





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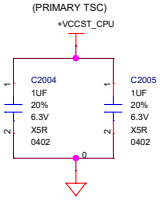

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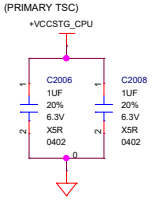
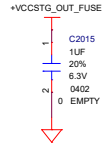
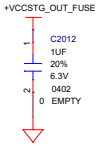


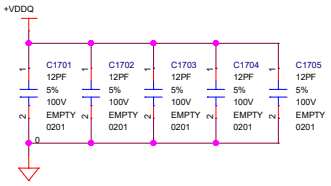




EMC

CAD NOTE:

EMC CAPS -PLACEMENT: < 50MM AROUND THE +VDDQ SHAPE



BPAGE DRAWING

tgl_u_rd.01

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	<DOCUMENT_NUMBER>	17	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:

USING 10L-T4-DS SDS (ISC) SOCKETED BOM FROM TGL-U AEP WHITE PAPER

DESIGN NOTE:

INDUCTOR IS A PLACEHOLDER PER PI BOM (0.6UH <30MOHM DCR)

+V1P8A_PCH

L2101 0.68UH 3A EMPTY 30% SM

+VCCA_CLKLDO_1P8

R2102 0.01 1% 0603 0.1W RES

+VCCA_CLKLDO_1P8_C

R2103 5% 0 0.1W RES 0402

C2107 47UF 20% 6.3V X5R 0603

CAD NOTE:

PAD SHARE THE L2101 AND R2102

PLACE C2107 AS CLOSE AS POSSIBLE TO BGA

+VCCA_CLKLDO_1P8

CAD NOTE:

PLACE NEAR BGA WITHIN 3MM FROM PACKAGE EDGE

+VCCEDOSTD_OUT_0P85

C2103 2.2UF 20% 6.3V X5R 0402

TP2101 @board_artifacts.tp(sym_1):page18_i50 EMPTY SM

CAD NOTE:

PLACE AS CLOSE AS POSSIBLE TO BGA

+VCCPRTC_3P3

C2105 1UF 10% 16V X5R 0402

C2101 0.10UF 10% 10V X5R 0402

CAD NOTE:

PLACE NEAR BGA

+VCCDSW_1P05

C2106 1UF 20% 6.3V X5R 0402

TP2102 @board_artifacts.tp(sym_1):page18_i58 EMPTY SM

CAD NOTE:

PLACE AS CLOSE AS POSSIBLE TO BGA

+VCCPDSW_3P3

C2110 1UF 10% 16V EMPTY 0402

+VCCRTCEXT

C2117 0.1UF 10% 10V X5R 0402

VCCPRIM_3P3

+V3P3A_PCH

C2102 0.10UF 10% 10V EMPTY 0402

C2104 1UF 10% 16V EMPTY 0402

CAD NOTE:

PLACE AS CLOSE AS POSSIBLE TO BGA

C2102 & C2104 ARE PLACEHOLDERS

CAD NOTE:

PLACE WITHIN 3MM FROM PACKAGE EDGE NEAR BGA

+VCCDPHY_1P24

C2111 4.7UF 20% 6.3V X5R 0402

CAD NOTE:

PLACE AS CLOSE AS POSSIBLE TO BGA

(PRIMARY TSC)

VCCPRIM_1P8

+V1P8A_PCH

C2109 1UF 20% 6.3V EMPTY 0402

BPAGE DRAWING

tgl_u_rd.+VCCD.18

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	<DOCUMENT_NUMBER>	18	1P0

CUSTOM TEXT BPAGE

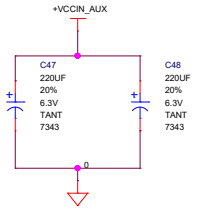
+VCCIN_AUX

MODULE REV DETAILS		
MODULE NAME	REV	DATE

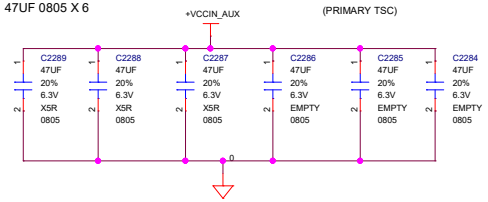
DESIGN NOTE:

USING 10L-T4-DS SDS (ISC) SOCKETED BOM FROM TGL-U AEP WHITE PAPER

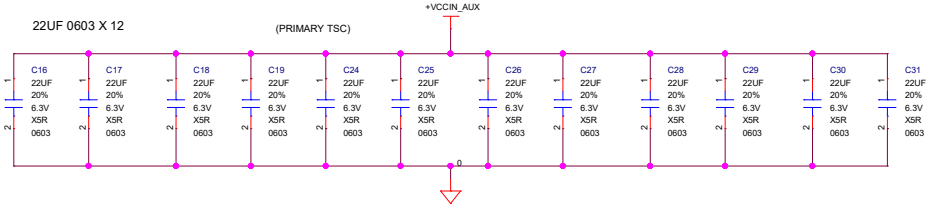
220UF 7343 X 2



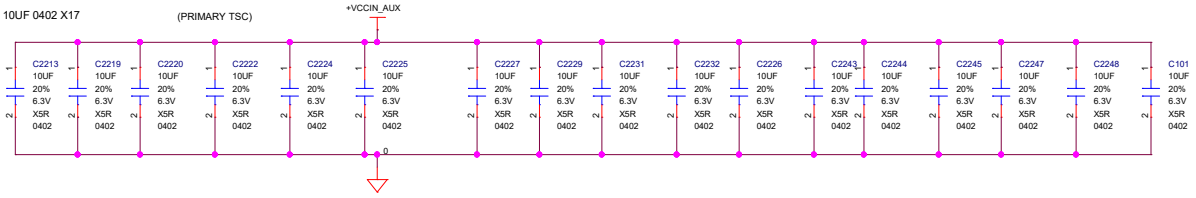
47UF 0805 X 6



22UF 0603 X 12



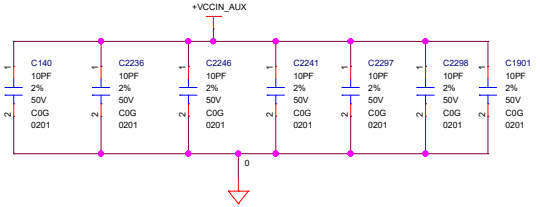
10UF 0402 X17



EMC

CAD NOTE:

EMC CAPS -PLACEMENT: < 5MM FROM SOC'S VCCIN_AUX



BPAGE DRAWING

tgl_u_rd.oi5
Fri Feb 28 13:40:51 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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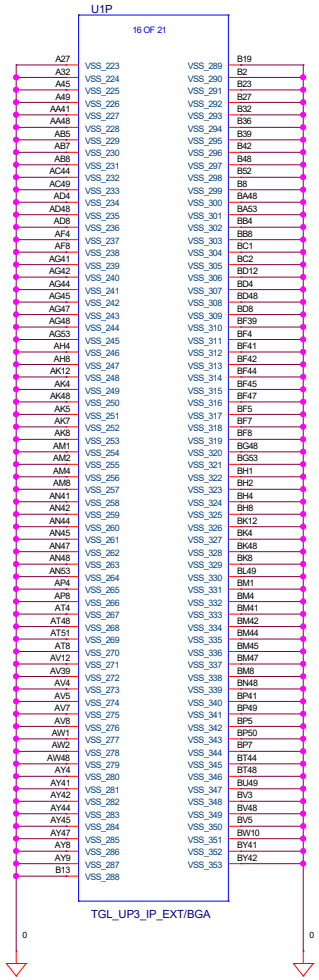
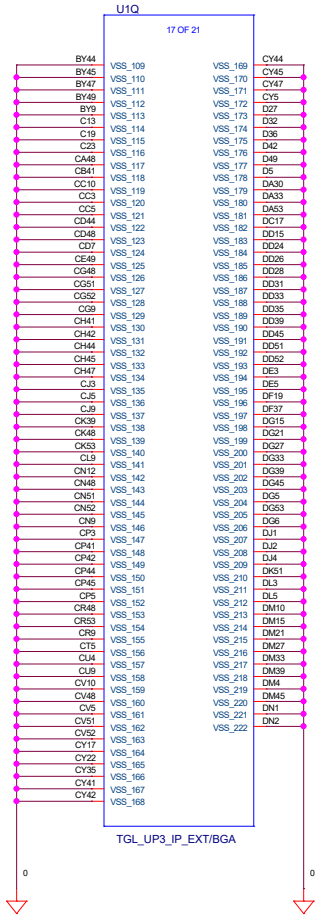
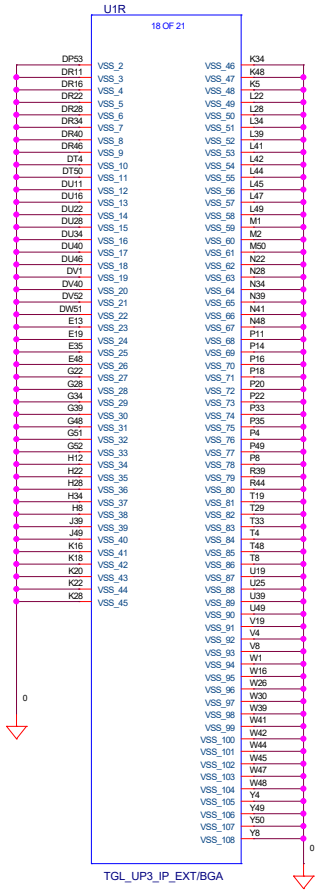
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE







BPAGE DRAWING

tgl_u_rd.GND
Fri Feb 28 13:40:52 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	20	1P0

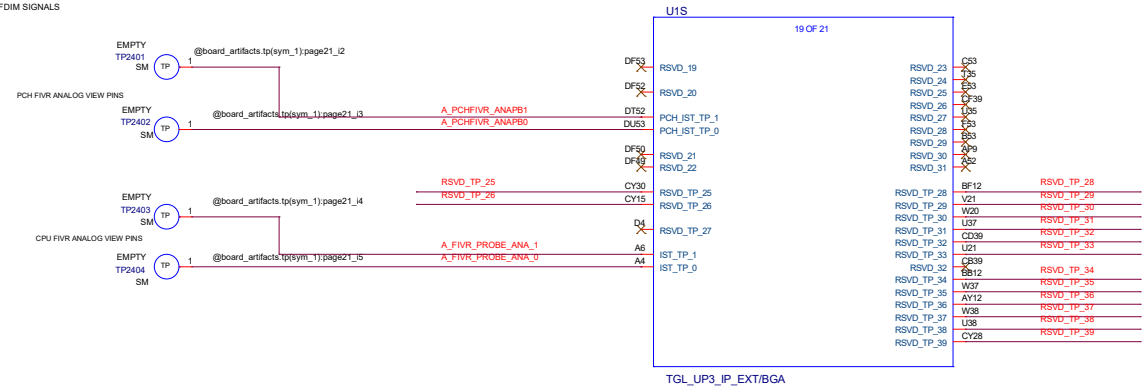
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

NOTE: DEBUG HOOKS - CUSTOMER INVISIBLE PAGES.

DESIGN NOTE:

TP2401, TP2402, TP2403 AND TP2404 ARE FOR IFDIM SIGNALS



BPAGE DRAWING

tgl_u_rd.0ADI~21
Fri Feb 28 13:40:52 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	21	1P0

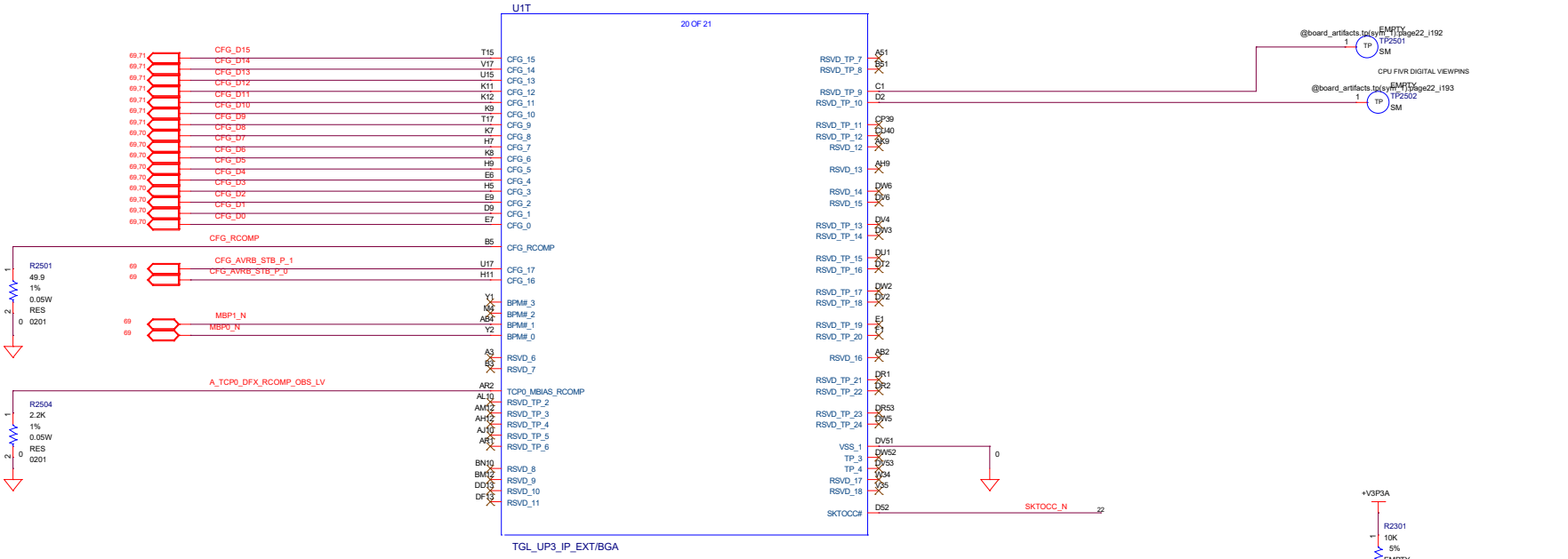
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

NOTE: DEBUG HOOKS - CUSTOMER INVISIBLE PAGES.

DESIGN NOTE:

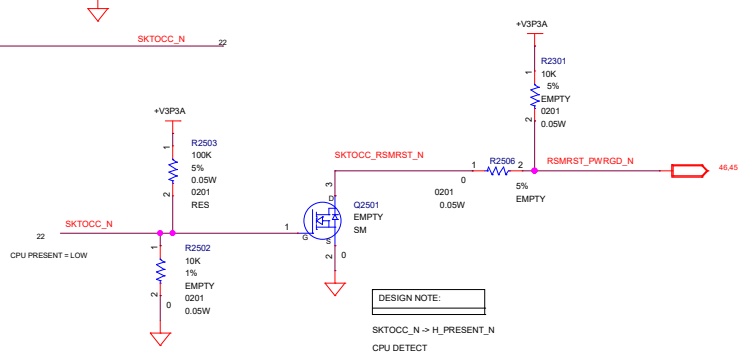
TP2501 AND TP2502 ARE FOR IFDIM SIGNALS



CAD NOTE:

CFG_RCOMP (PEG_RCOMP) ACCORDING TO IPDG, HAS NO BOARD RDC ASSIGNED.
MAIN ROUTE TRACE SPACING IS 380 UM (SL/DSL) OR 500UM (MS)

TCP0 RCOMP RDC SHOULD BE < 0.5 OHMS
WHILE SPACING SHOULD BE 500UM (MS) OR 380 (SL/DSL)



DESIGN NOTE:

SKTOCC_N -> H_PRESENT_N
CPU DETECT

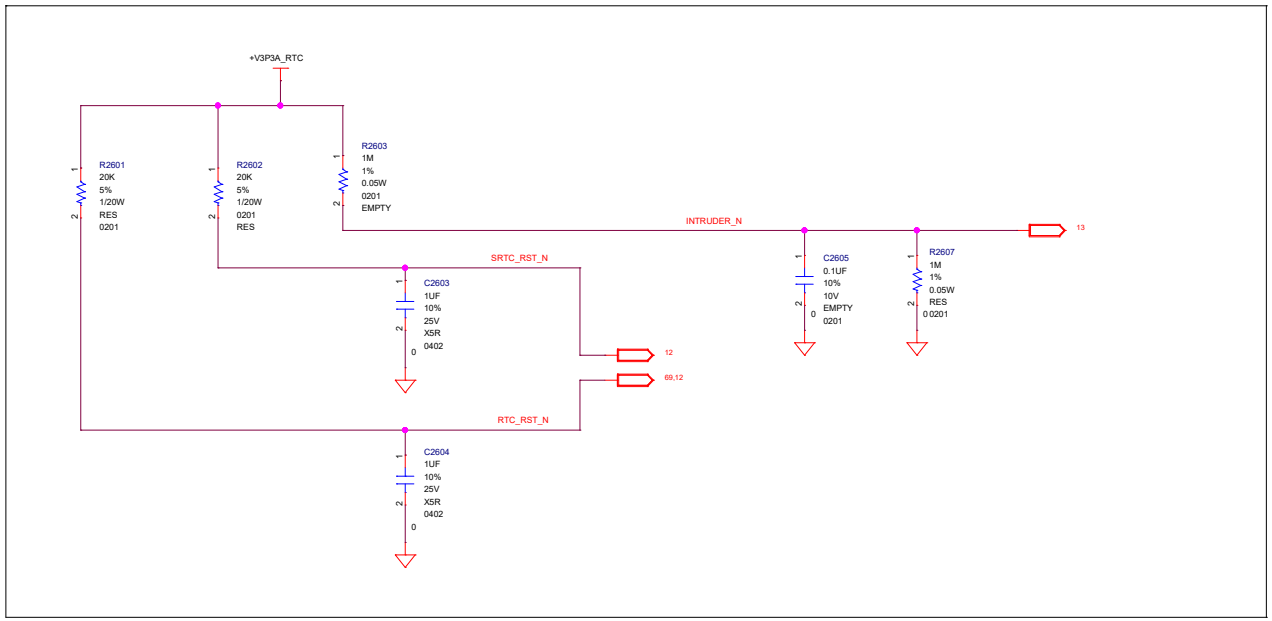
BPAGE DRAWING

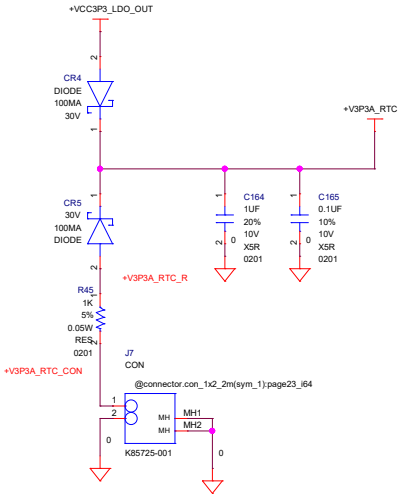
tgl_u_rd.GND
Fri Feb 28 13:40:52 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	22	1P0

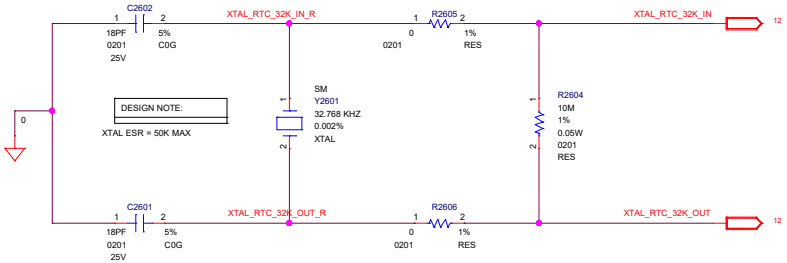
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE





RTC CRYSTAL

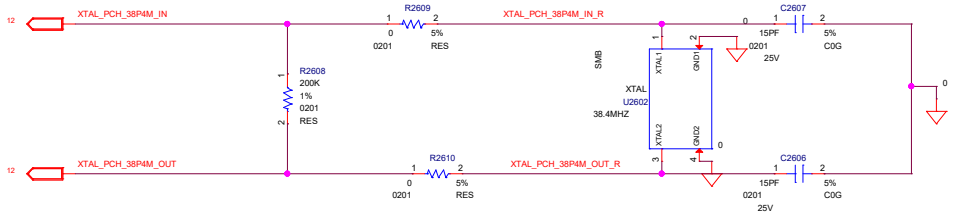


CAD NOTE:

PER PDG, TOTAL LENGTH MATCHING BETWEEN XTAL_IN AND XTAL_OUT 1.27MM

NUMBER OF VIAS ALLOWED: MAX
2
GND SHIELDING TO ADJACENT SIGNALS (ESPECIALLY HSIO) IS RECOMMENDED

XTAL 38.4MHZ



DESIGN NOTE:

REMOVED CHOKE AS IT WAS AN EMPTY COMPONENT AND NOT REQUIRED PER PDG

BPAGE DRAWING

tgl_u_rd:GND
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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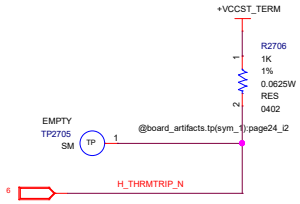
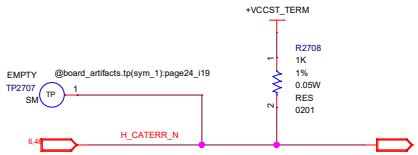
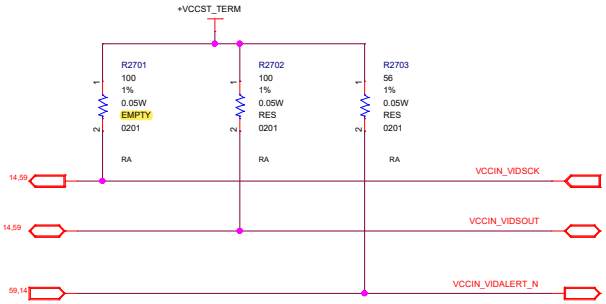
CUSTOM TEXT BPAGE

CPU SIDEBAND SIGNALS

MODULE REV DETAILS		
MODULE NAME	REV	DATE







CAD NOTE:

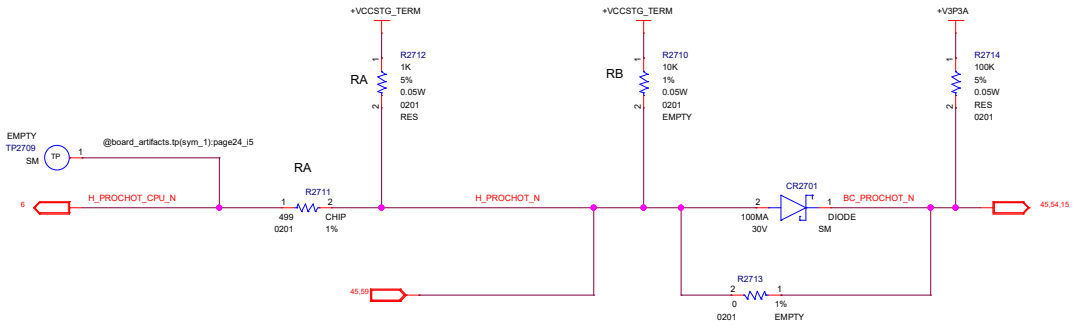
THESE RA RESISTORS SHOULD BE PLACED WITHIN 75MM FROM CPU

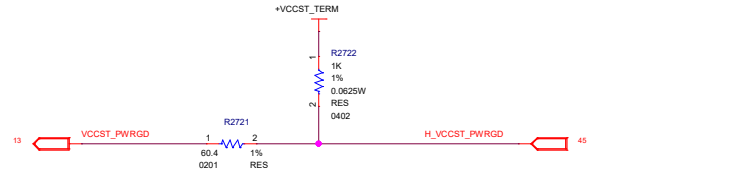
CAD NOTE:

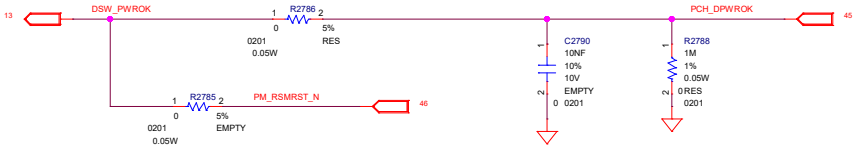
PLACE 'RA' CLOSE TO MCP - WITHIN 1INCH

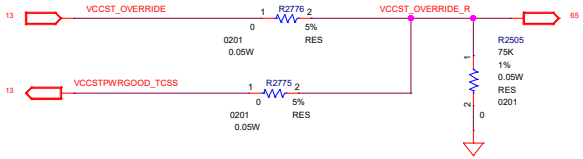
CAD NOTE:

PLACE 'RB' AT THE END OF DIASY CHAIN









BPAGE DRAWING

tgl_u_rd.+VCCS.24
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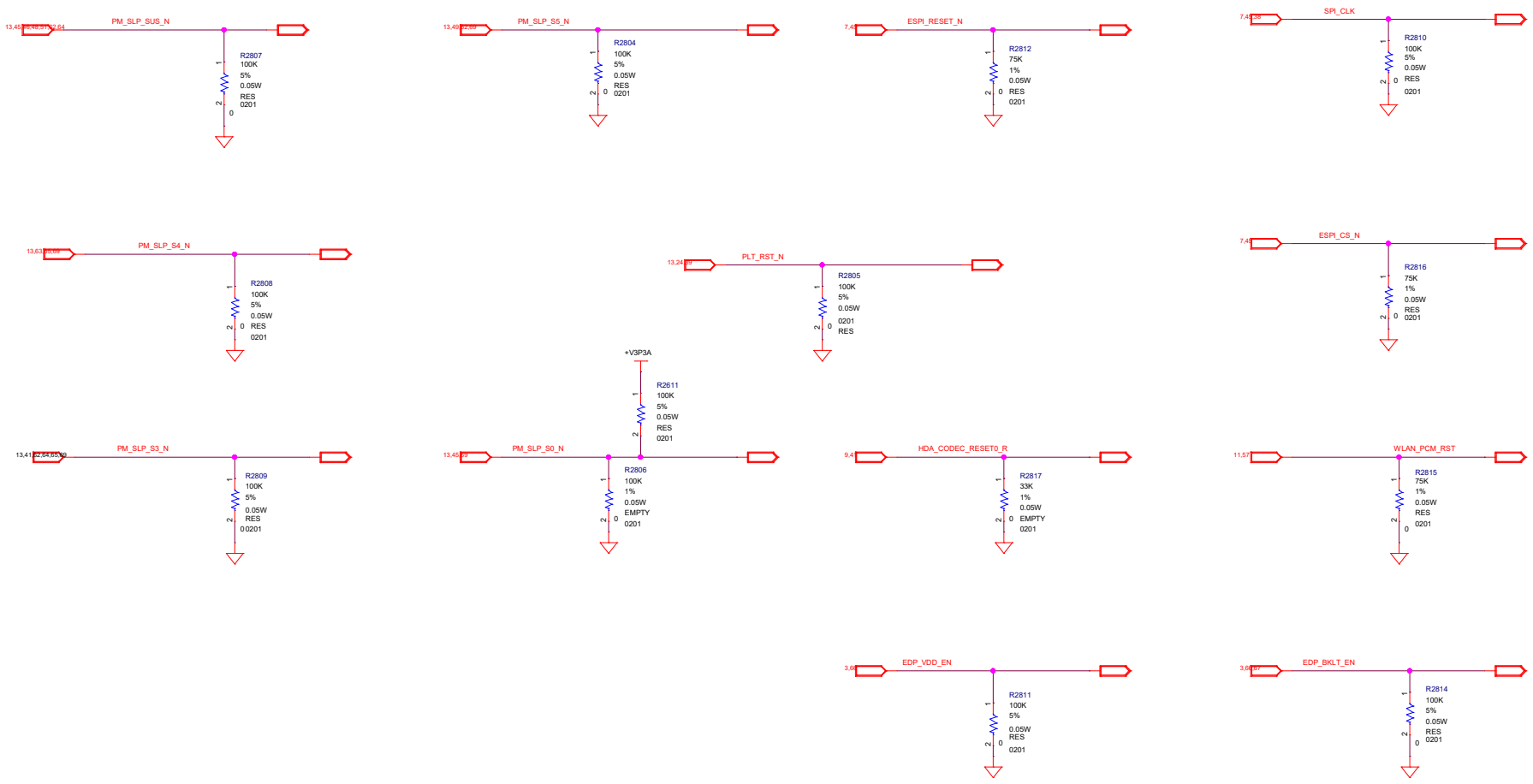
	<DOCUMENT_NUMBER>	24	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PCH GLITCH ISSUE MITIGATION



BPAGE DRAWING

tgl_u_rd.GND
Fri Feb 28 13:40:53 2020

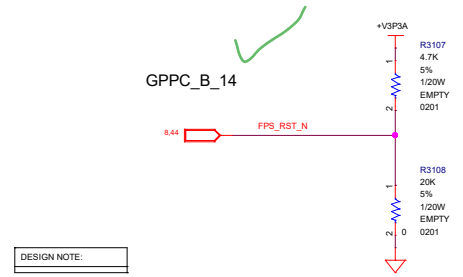
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	25	1P0

CUSTOM TEXT BPAGE

PCH STRAPS

MODULE REV DETAILS

MODULE NAME	REV	DATE



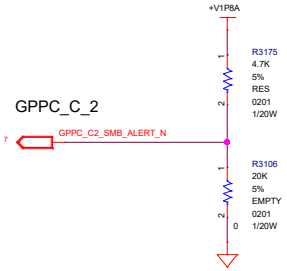
DESIGN NOTE:

PULL DOWN RESISTOR (100K) RESISTOR PRESENT ON THIS NET

TOP SWAP OVERRIDE

HIGH- TOP SWAP ENABLED
LOW-DISABLED

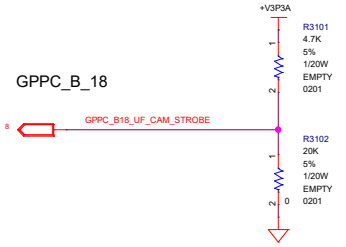
WEAK INTERNAL PD 20K



TLS CONFIDENTIALITY

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

WEAK INTERNAL PD 20K



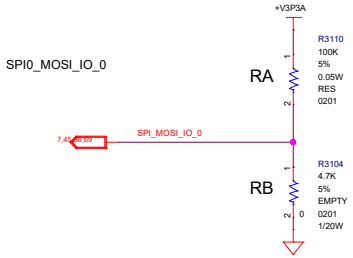
NO REBOOT

HIGH - NO REBOOT
LOW- REBOOT ENABLED

WEAK INTERNAL PD 20K

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



BOOT HALT

HIGH - DISABLED
LOW- ENABLED

NO INTERNAL PU/PD

BPAGE DRAWING

tgl_u_rd:GND
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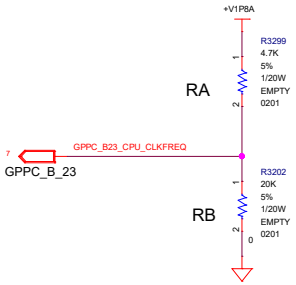
	<DOCUMENT_NUMBER>	26	1P0

CUSTOM TEXT BPAGE

PCH STRAPS

MODULE REV DETAILS		
MODULE NAME	REV	DATE

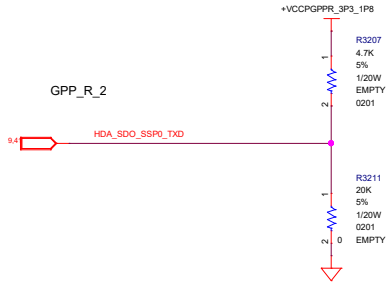


CPUNSSC CLOCK FREQ

HIGH: 19.2MHZ CLOCK FROM DIVIDER
(DERIVED FROM 38.4MHZ CRYSTAL)

LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)

WEAK INTERNAL PD 20K



FLASH DESCRIPTOR SECURITY OVERRIDE

HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN

WEAK INTERNAL PD 20K

XTAL SEL

0- 38.4/19.2MHZ (DEFAULT)

1- 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

WEAK INTERNAL PD 20K

BPAGE DRAWING

tgl_u_rd.+VCCP.27
Fri Feb 28 13:40:54 2020

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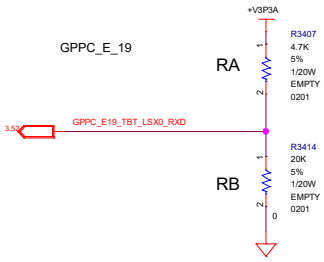
	<DOCUMENT_NUMBER>	27	1P0

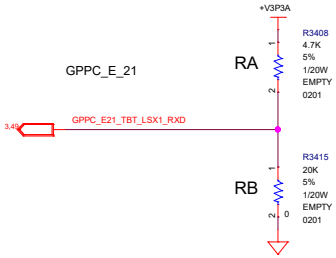
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

PCH STRAPS

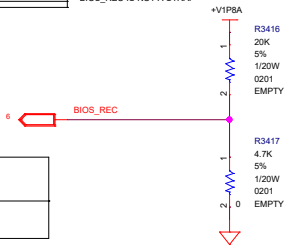


TBT LSX#0 PINS VCCIO CONFIGURATION
HIGH: 3.3V
LOW: 1.8V
WEAK INTERNAL PD 20K



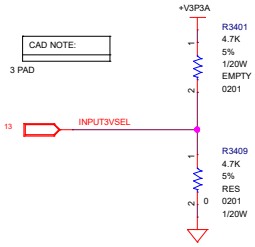
TBT LSX#1 PINS VCCIO CONFIGURATION
HIGH: 3.3V
LOW: 1.8V
WEAK INTERNAL PD 20K

DESIGN NOTE:
BIOS_REC IS NOT A STRAP



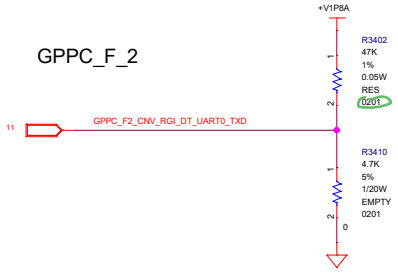
STRAP/GPIO NAME	DEFAULT CONFIG REQUIRED	CONFIG CHANGE IF REQ
BIOS RECOVERY	OPEN(NO BIOS REC)	CLOSED (BIOS REC)

CAD NOTE:
3 PAD



SPI 1.8V/3.3V SELECTION

LOW->3.3V
HIGH->1.8V
NO TERMINATION, NOT SAMPLED
DEFAULT 3.3V



M.2 CNVI MODES

LOW-> INTEGRATED CNVI ENABLE
HIGH-> INTEGRATED CNVI DISABLE
NO INTERNAL PU/PD

BPAGE DRAWING

tgl_u_rd.+V1P8.28
Fri Feb 28 13:40:54 2020

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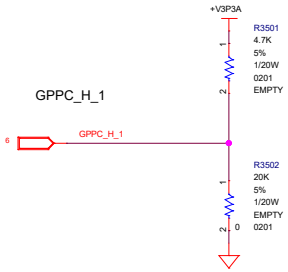
	<DOCUMENT_NUMBER>	28	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

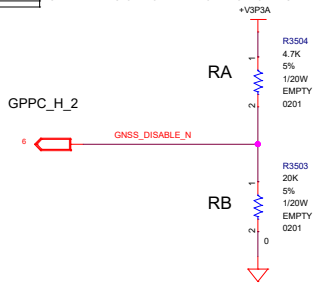
PCH STRAPS



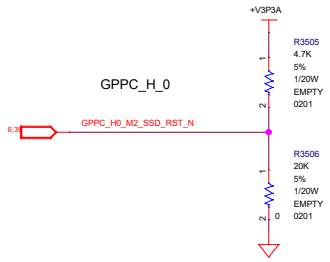
BFX STRAP 2 -BIT3
WEAK INTERNAL PD 20K

BFX STRAP 1 -BIT1
WEAK INTERNAL PD 20K

CAD NOTE: PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



BFX STRAP 3 -BIT4
WEAK INTERNAL PD 20K



BFX STRAP 1 -BIT2
WEAK INTERNAL PD 20K

4-BIT BOOT STRAP CONFIGURATION ENCODINGS:

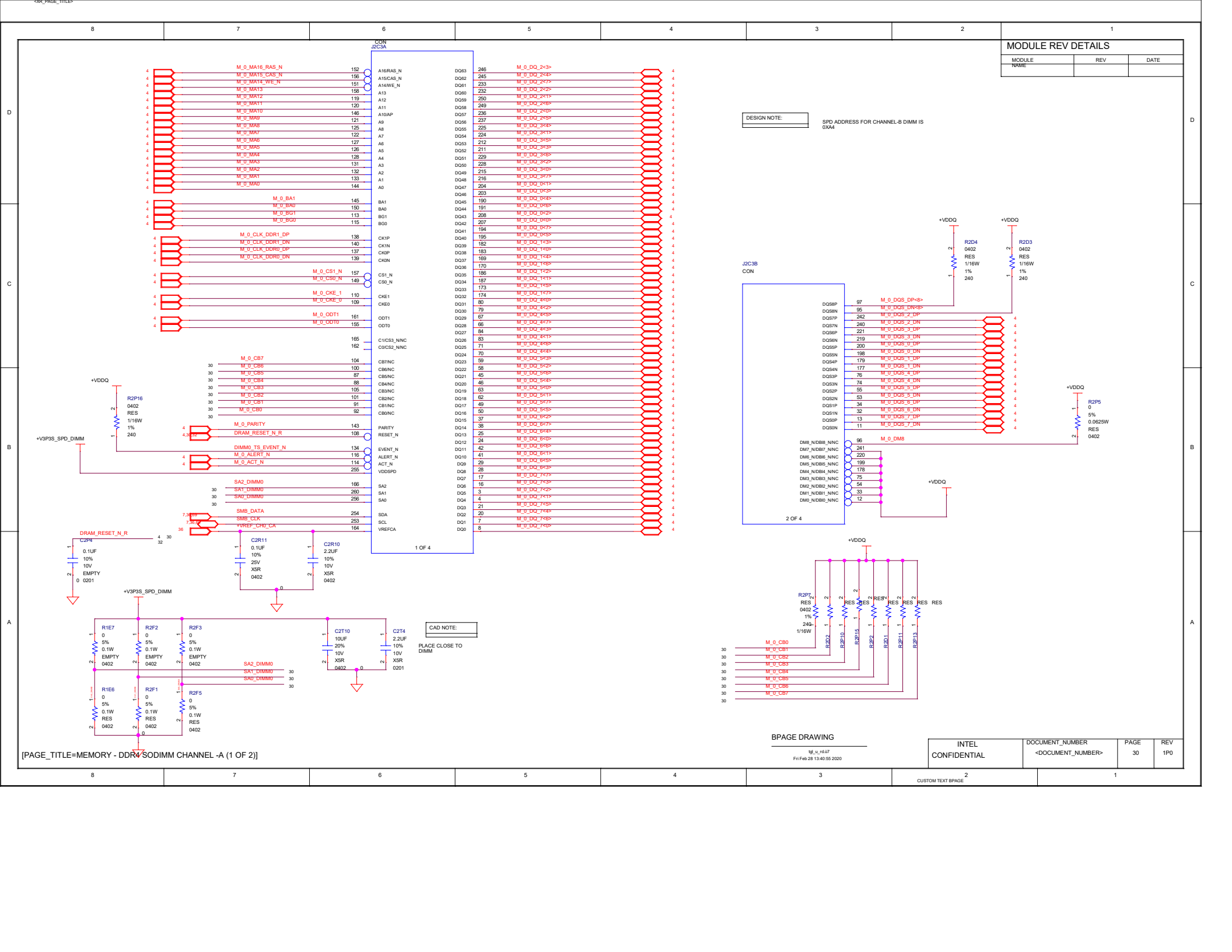
0000 = MASTER ATTACHED FLASH CONFIGURATION (BIOS/CSME ON SPI).
1000 = SLAVE ATTACHED FLASH CONFIGURATION (BIOS/CSME ON ESPI ATTACHED DEVICE).
1100 = BIOS ON ESPI PERIPHERAL CHANNEL; CSME ON SLAVE ATTACHED SPI.
0100 = BIOS ON ESPI PERIPHERAL CHANNEL; CSME ON MASTER ATTACHED SPI

OTHERS: RESERVED

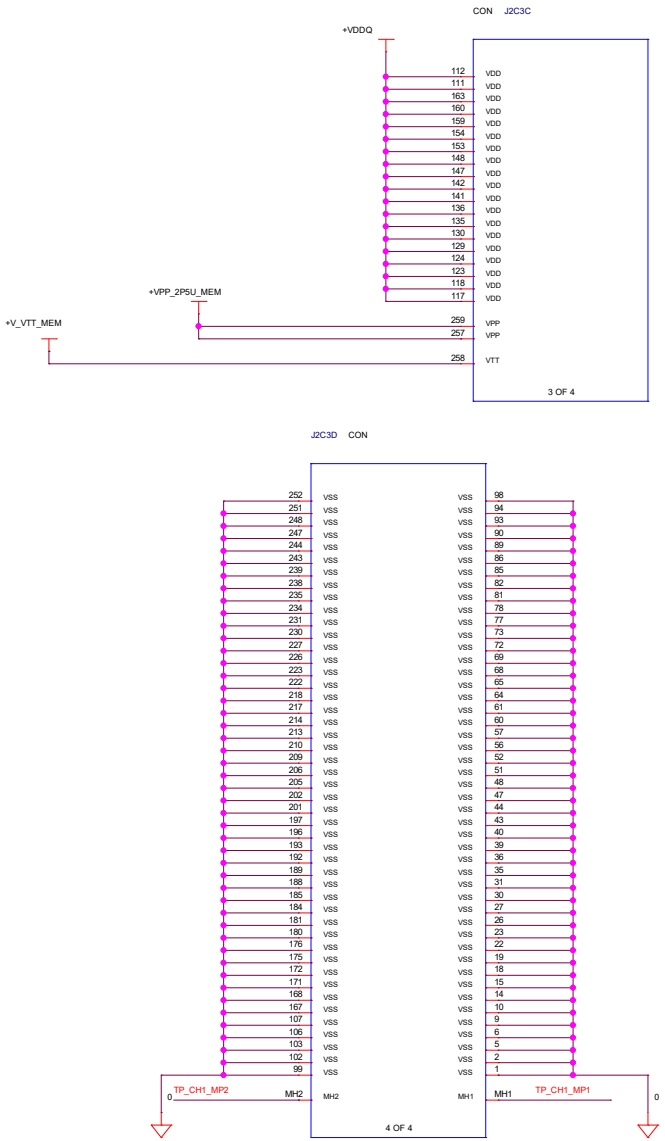
BPAGE DRAWING
tgl_u_rd.GND
Fri Feb 28 13:40:55 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	29	1P0

CUSTOM TEXT BPAGE


MODULE REV DETAILS
MODULE NAME
REV
DATE
DESIGN NOTE:
SPD ADDRESS FOR CHANNEL-B DIMM IS 0XA4
CAD NOTE:
PLACE CLOSE TO DIMM
BPAGE DRAWING
tgl_u_rd.07
Fri Feb 28 13:40:55 2020
[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -A (1 OF 2)]
INTEL CONFIDENTIAL
DOCUMENT_NUMBER
<DOCUMENT_NUMBER>
PAGE
30
REV
1P0
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -A (2 OF 2)]

BPAGE DRAWING

tgl_u_rd.+V_VT.31
Fri Feb 28 13:40:55 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	31	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CON J2C4A

M_1_MA16_RAS_N
M_1_MA15_CAS_N
M_1_MA14_WE_N
M_1_MA13
M_1_MA12
M_1_MA11
M_1_MA10
M_1_MA9
M_1_MA8
M_1_MA7
M_1_MA6
M_1_MA5
M_1_MA4
M_1_MA3
M_1_MA2
M_1_MA1
M_1_MA0

M_1_BA1
M_1_BA0
M_1_BG1
M_1_BG0

M_1_CLK_DDR1_DP
M_1_CLK_DDR1_DN
M_1_CLK_DDR0_DP
M_1_CLK_DDR0_DN

M_1_CS1_N
M_1_CS0_N

M_1_CKE_1
M_1_CKE_0

M_1_ODT1
M_1_ODT0

M_1_CB7
M_1_CB6
M_1_CB5
M_1_CB4
M_1_CB3
M_1_CB2
M_1_CB1
M_1_CB0

M_1_PARITY
DRAM_RESET_N_R

DIMM1_TS_EVENT_N
M_1_ALERT_N
M_1_ACT_N

SA2_DIMM1
SA1_DIMM1
SA0_DIMM1

SODIMM0_1_SMB_DATA_R
SODIMM0_1_SMB_CLK_R
+VREF_CH1_CA

M_1_DQ_2<6>
M_1_DQ_2<2>
M_1_DQ_2<7>
M_1_DQ_2<3>
M_1_DQ_2<4>
M_1_DQ_2<0>
M_1_DQ_2<1>
M_1_DQ_2<5>
M_1_DQ_3<0>
M_1_DQ_3<4>
M_1_DQ_3<7>
M_1_DQ_3<3>
M_1_DQ_3<1>
M_1_DQ_3<5>
M_1_DQ_3<2>
M_1_DQ_3<6>
M_1_DQ_0<4>
M_1_DQ_0<1>
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M_1_DQ_0<0>
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M_1_DQ_0<7>
M_1_DQ_1<3>
M_1_DQ_1<1>
M_1_DQ_1<5>
M_1_DQ_1<7>
M_1_DQ_1<2>
M_1_DQ_1<6>
M_1_DQ_1<4>
M_1_DQ_6<4>
M_1_DQ_6<5>
M_1_DQ_6<1>
M_1_DQ_6<7>
M_1_DQ_6<2>
M_1_DQ_6<0>
M_1_DQ_6<3>
M_1_DQ_6<6>
M_1_DQ_7<0>
M_1_DQ_7<7>
M_1_DQ_7<5>
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M_1_DQ_4<6>
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M_1_DQ_5<0>
M_1_DQ_5<1>
M_1_DQ_5<3>
M_1_DQ_5<5>
M_1_DQ_5<7>
M_1_DQ_5<2>

1 OF 4
K86569-001

DESIGN NOTE:
SPD ADDRESS FOR CHANNEL-A DIMM IS 0XA0

CON J2C4B
2 OF 4
K86569-001

M_1_DQS_DP<8>
M_1_DQS_DN<8>
M_1_DQS_2_DP
M_1_DQS_2_DN
M_1_DQS_3_DP
M_1_DQS_3_DN
M_1_DQS_0_DP
M_1_DQS_0_DN
M_1_DQS_1_DP
M_1_DQS_1_DN
M_1_DQS_6_DP
M_1_DQS_6_DN
M_1_DQS_7_DP
M_1_DQS_7_DN
M_1_DQS_4_DP
M_1_DQS_4_DN
M_1_DQS_5_DP
M_1_DQS_5_DN
M_1_DM8

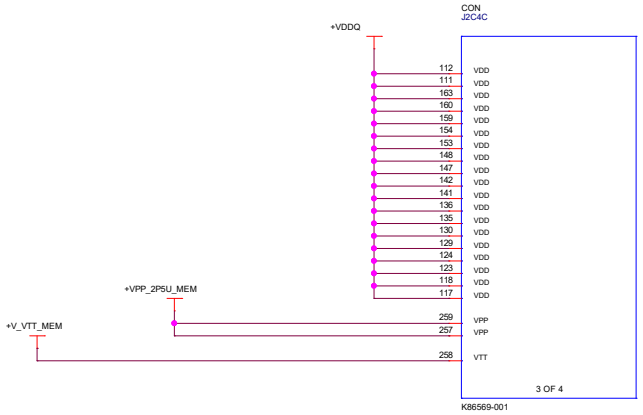
BPAGE DRAWING

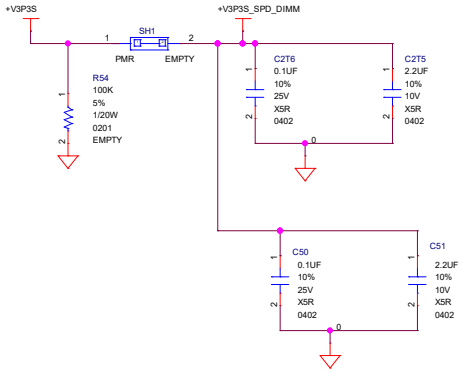
tgl_u_rd.+VDDQ.32
Fri Feb 28 13:40:55 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	32	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE





CAD NOTE:

PLACE CLOSE TO DIMM

[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -B (2 OF 2)]

BPAGE DRAWING

tgl_u_rd.+V3P3.33
Fri Feb 28 13:40:56 2020

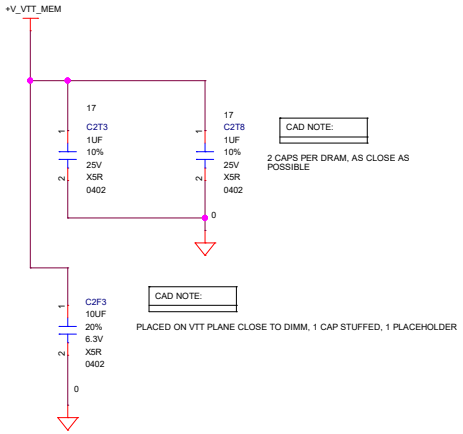
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	33	1P0

CUSTOM TEXT BPAGE

VTT DECAPS

PLACE THESE CAPS CLOSE TO SODIMM

CAD NOTE:



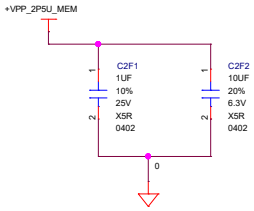
CAD NOTE:
2 CAPS PER DRAM, AS CLOSE AS POSSIBLE

CAD NOTE:
PLACED ON VTT PLANE CLOSE TO DIMM, 1 CAP STUFFED, 1 PLACEHOLDER

VPP DECAPS

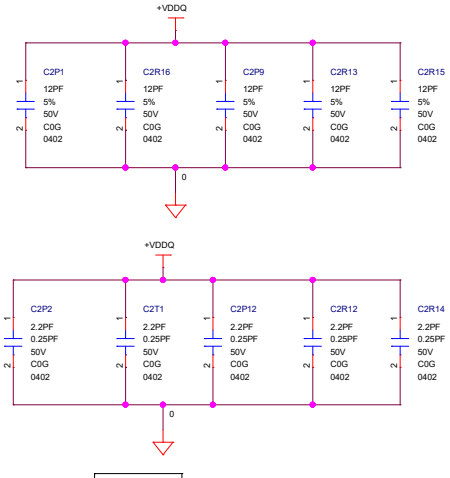
PLACE THESE CAPS CLOSE TO SODIMM

CAD NOTE:

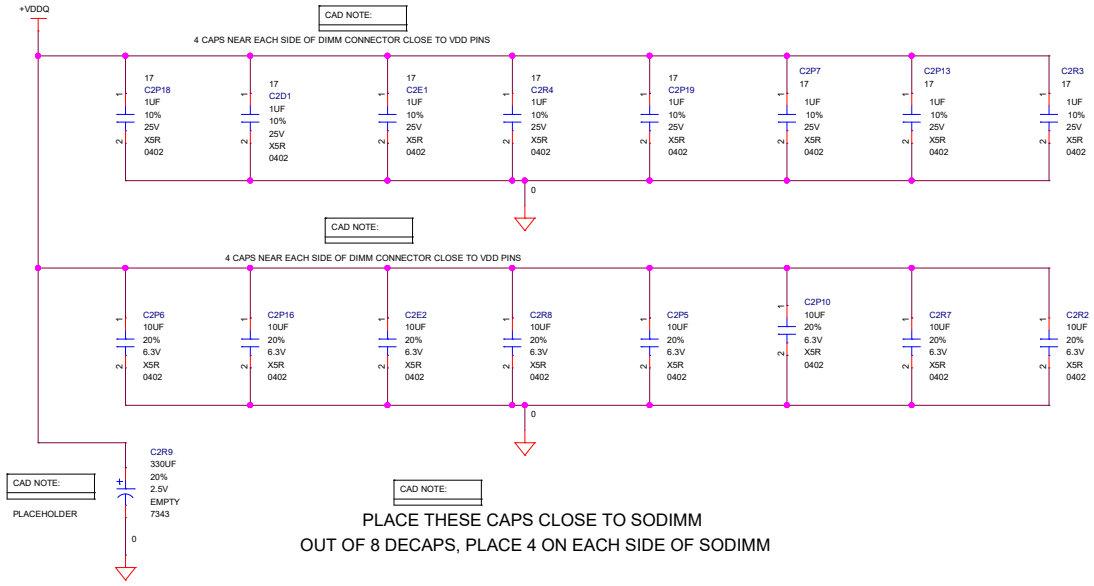


CAD NOTE:
AS CLOSE AS POSSIBLE

VDDQ DECAPS



CAD NOTE:
ABOVE CAPS ARE ADDED FOR EMC LAYOUT FEEDBACK



PLACE THESE CAPS CLOSE TO SODIMM
OUT OF 8 DECAPS, PLACE 4 ON EACH SIDE OF SODIMM

MODULE REV DETAILS

MODULE NAME	REV	DATE

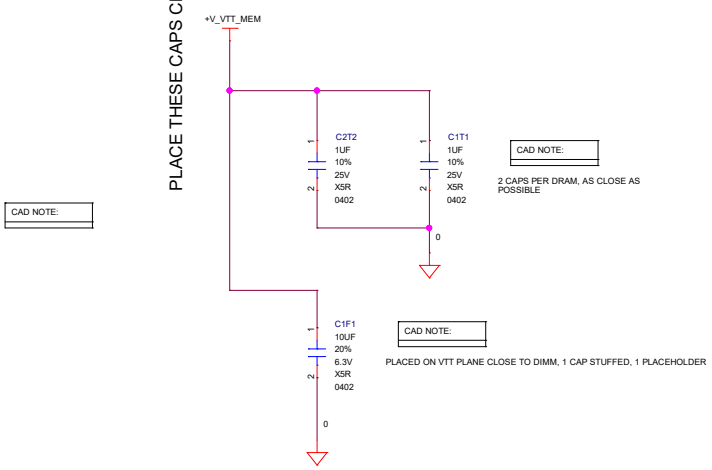
[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -A PD BOM]

BPAGE DRAWING
tgl_u_rd.a9
Fri Feb 28 13:40:56 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	34	1P0

CUSTOM TEXT BPAGE

VTT DECAPS



CAD NOTE:

2 CAPS PER DRAM, AS CLOSE AS POSSIBLE

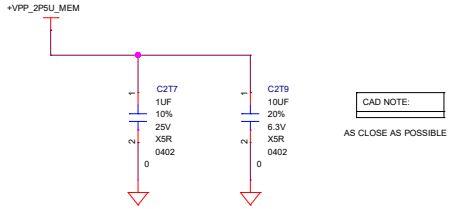
CAD NOTE:

PLACED ON VTT PLANE CLOSE TO DIMM, 1 CAP STUFFED, 1 PLACEHOLDER

CAD NOTE:

PLACE THESE CAPS CLOSE TO SODIMM

VPP DECAPS



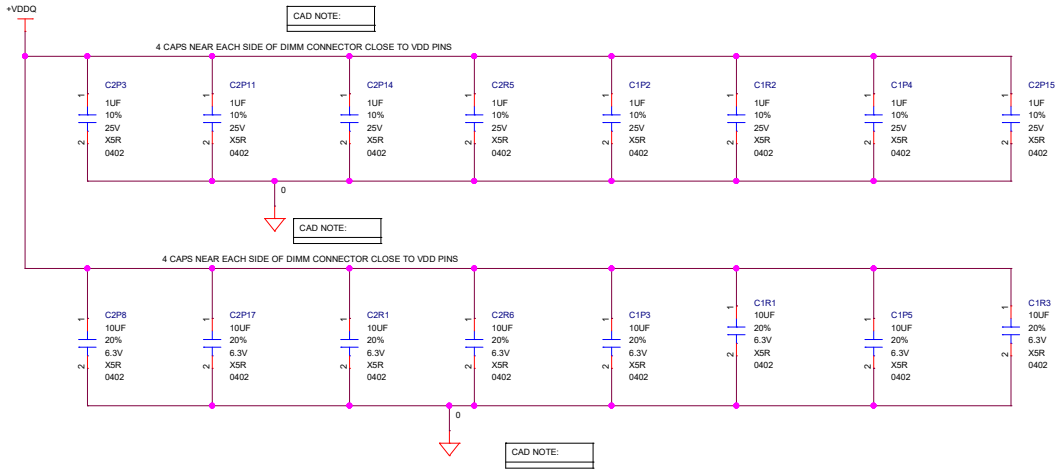
CAD NOTE:

AS CLOSE AS POSSIBLE

CAD NOTE:

PLACE THESE CAPS CLOSE TO SODIMM

VDDQ DECAPS



CAD NOTE:

4 CAPS NEAR EACH SIDE OF DIMM CONNECTOR CLOSE TO VDD PINS

CAD NOTE:

4 CAPS NEAR EACH SIDE OF DIMM CONNECTOR CLOSE TO VDD PINS

CAD NOTE:

PLACE THESE CAPS CLOSE TO SODIMM

OUT OF 8 DECAPS, PLACE 4 ON EACH SIDE OF SODIMM

MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=MEMORY - DDR4 SODIMM CHANNEL -BPD BOM]

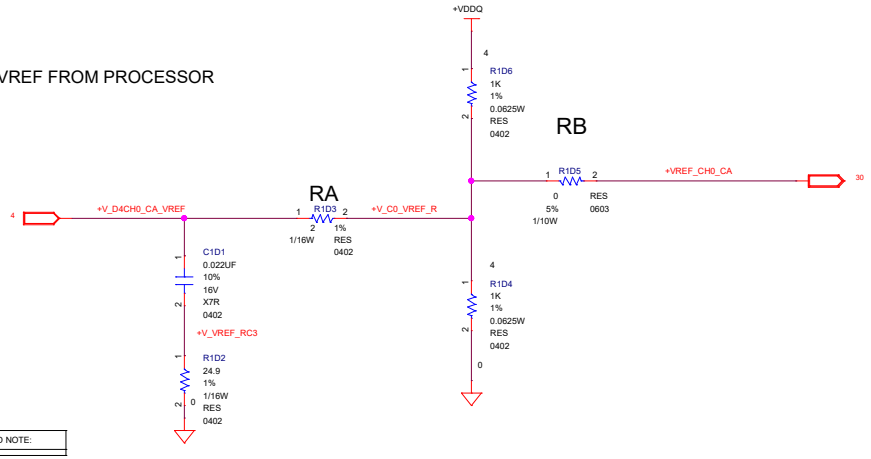
BPAGE DRAWING

tgl_u_rd.GND
Fri Feb 28 13:40:56 2020

MODULE REV DETAILS		
MODULE NAME	REV	DATE

VREF CIRCUITRY

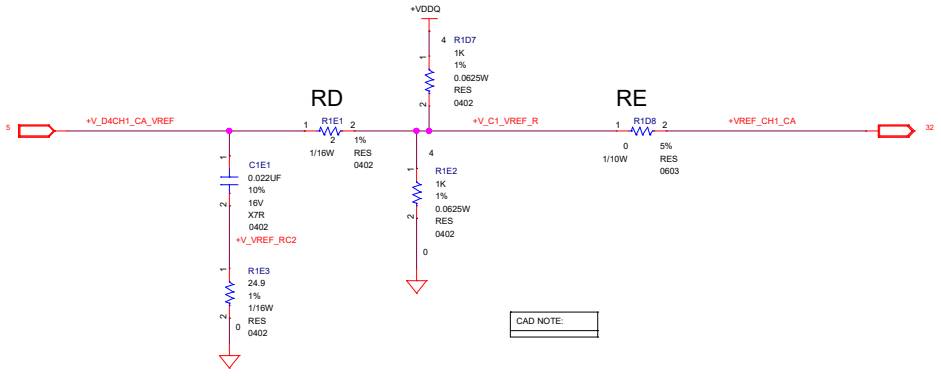
CH0 CA VREF FROM PROCESSOR



CAD NOTE:

PLACE RA, RB, RC CLOSE TO THE NODE

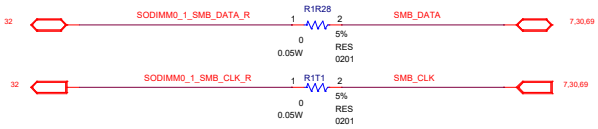
CH1 CA VREF FROM PROCESSOR



CAD NOTE:

DESIGN NOTE:

DDR VREF DIFFERENT OPTIONS (OPTION 1 AND 2 IS DEFAULT)
1: VOLTAGE DIVIDER NETWORK (DEFAULT)
2: FROM PROCESSOR (DEFAULT)



[PAGE_TITLE=MEMORY - DDR VREF CIRCUITRY -1 - PROCESSOR, OPTIONS]

BPAGE DRAWING

tgl_u_rd.GND
Fri Feb 28 13:40:56 2020

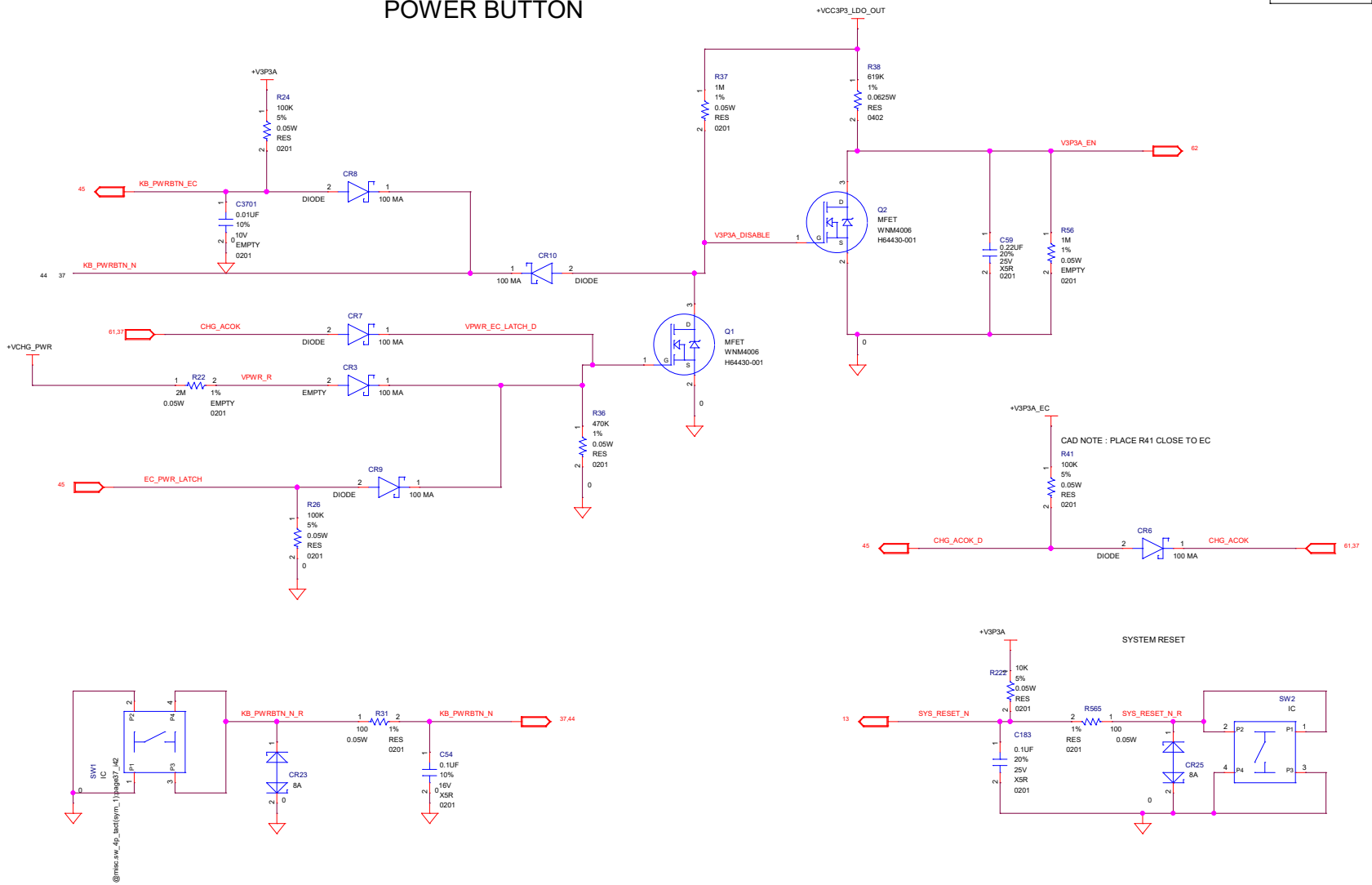
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	36	1P0

CUSTOM TEXT BPAGE

POWER BUTTON

MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=POWER BUTTON]

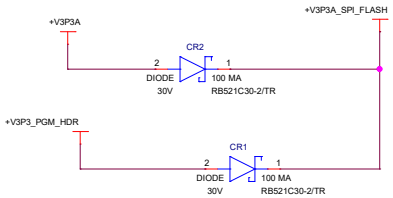
BPAGE DRAWING

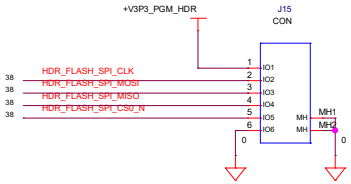
tgl_u_rd.GND
Fri Feb 28 13:40:57 2020

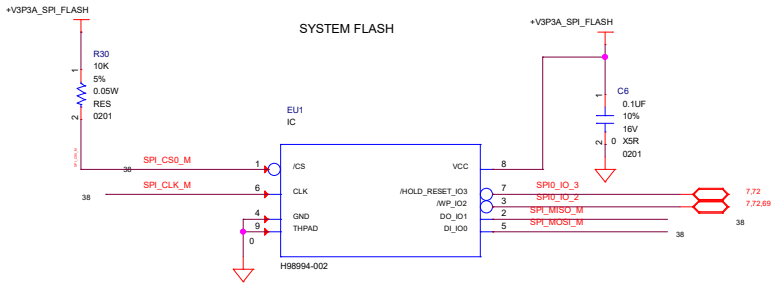
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	37	1P0

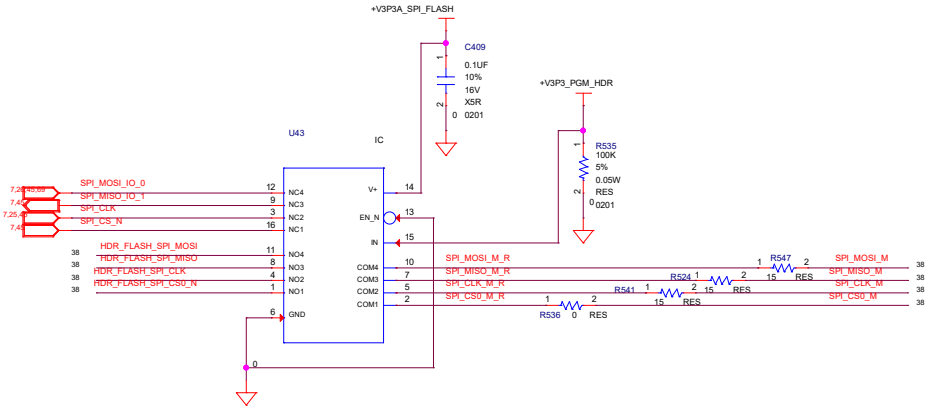
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE









[PAGE_TITLE=SYSTEM FLASH]

BPAGE DRAWING

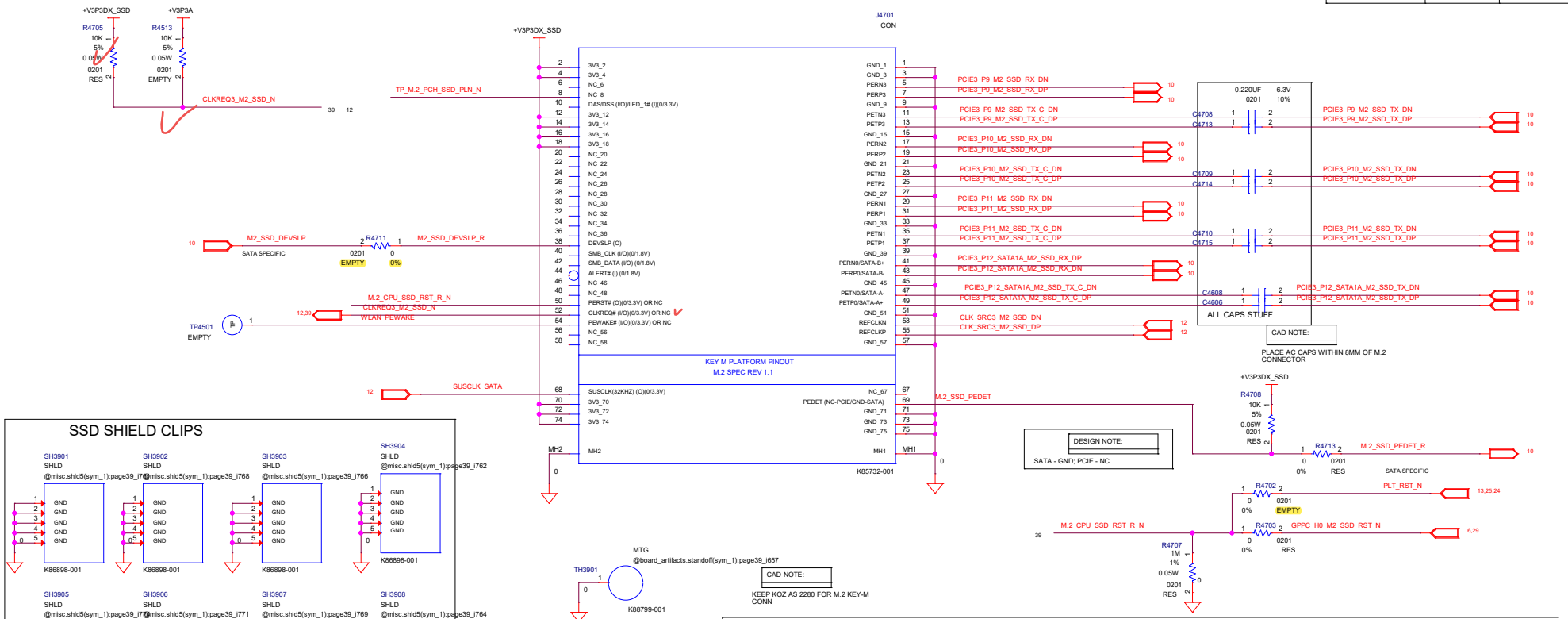
tgl_u_rd.GND
Fri Feb 28 13:40:57 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	38	1P0

CUSTOM TEXT BPAGE

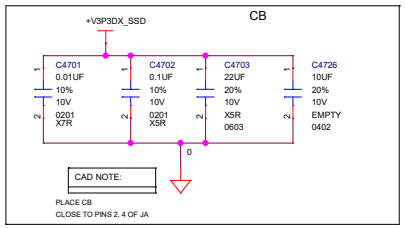
M.2 PCIE GEN3 SSD MODULE KEY-M CONNECTOR

MODULE REV DETAILS		
MODULE NAME	REV	DATE

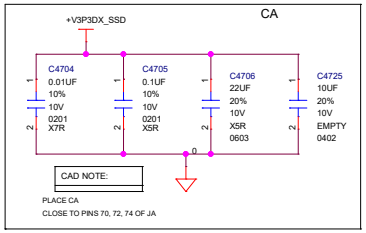


SSD SHIELD CLIPS

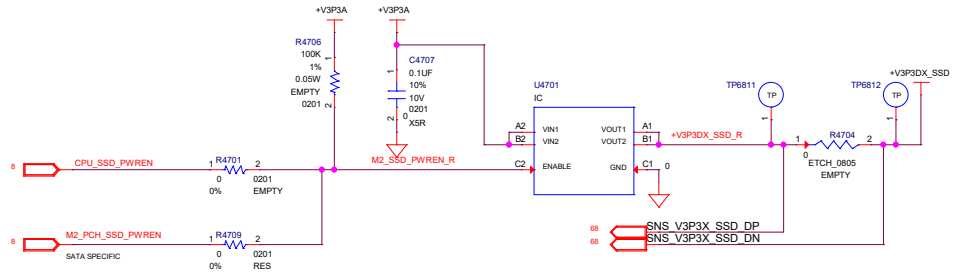
CB



CA



SSD RAIL GENERATION

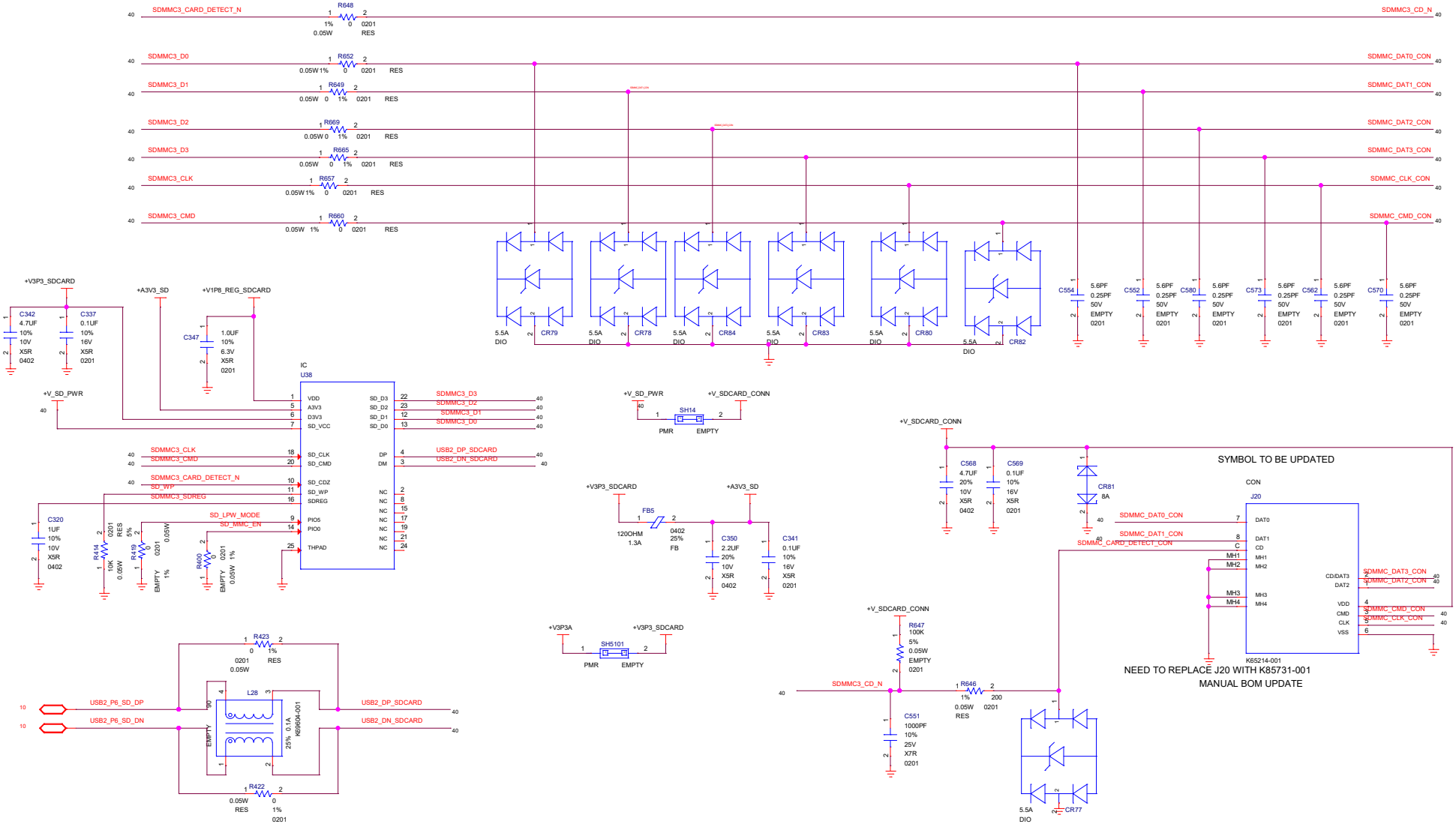


INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	39	1P0

CUSTOM TEXT BPAGE

SDCARD INTERFACE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



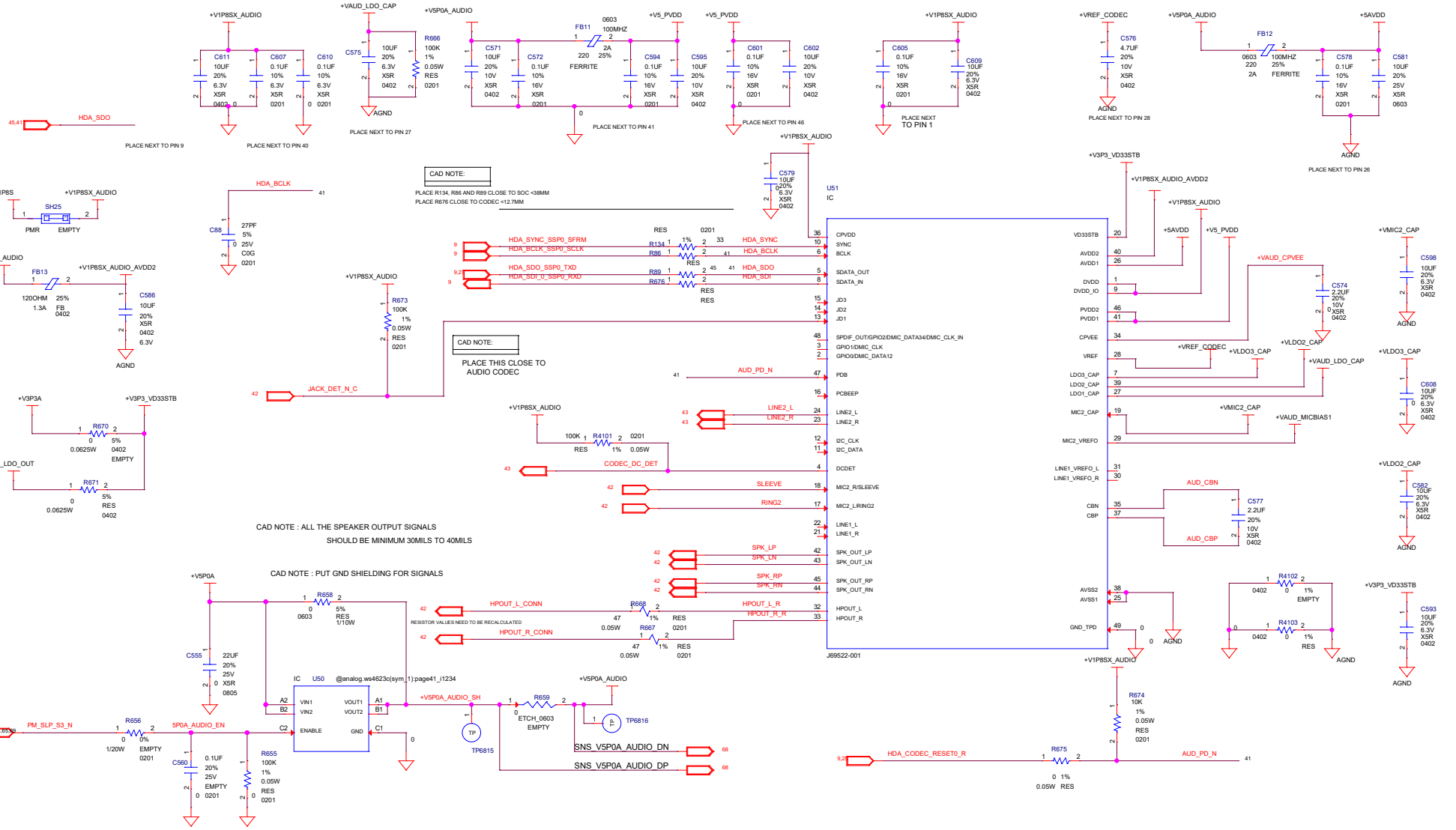
[PAGE_TITLE=SD CARD]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	40	1P0

CUSTOM TEXT BPAGE

AUDIO CODEC

MODULE REV DETAILS		
MODULE NAME	REV	DATE



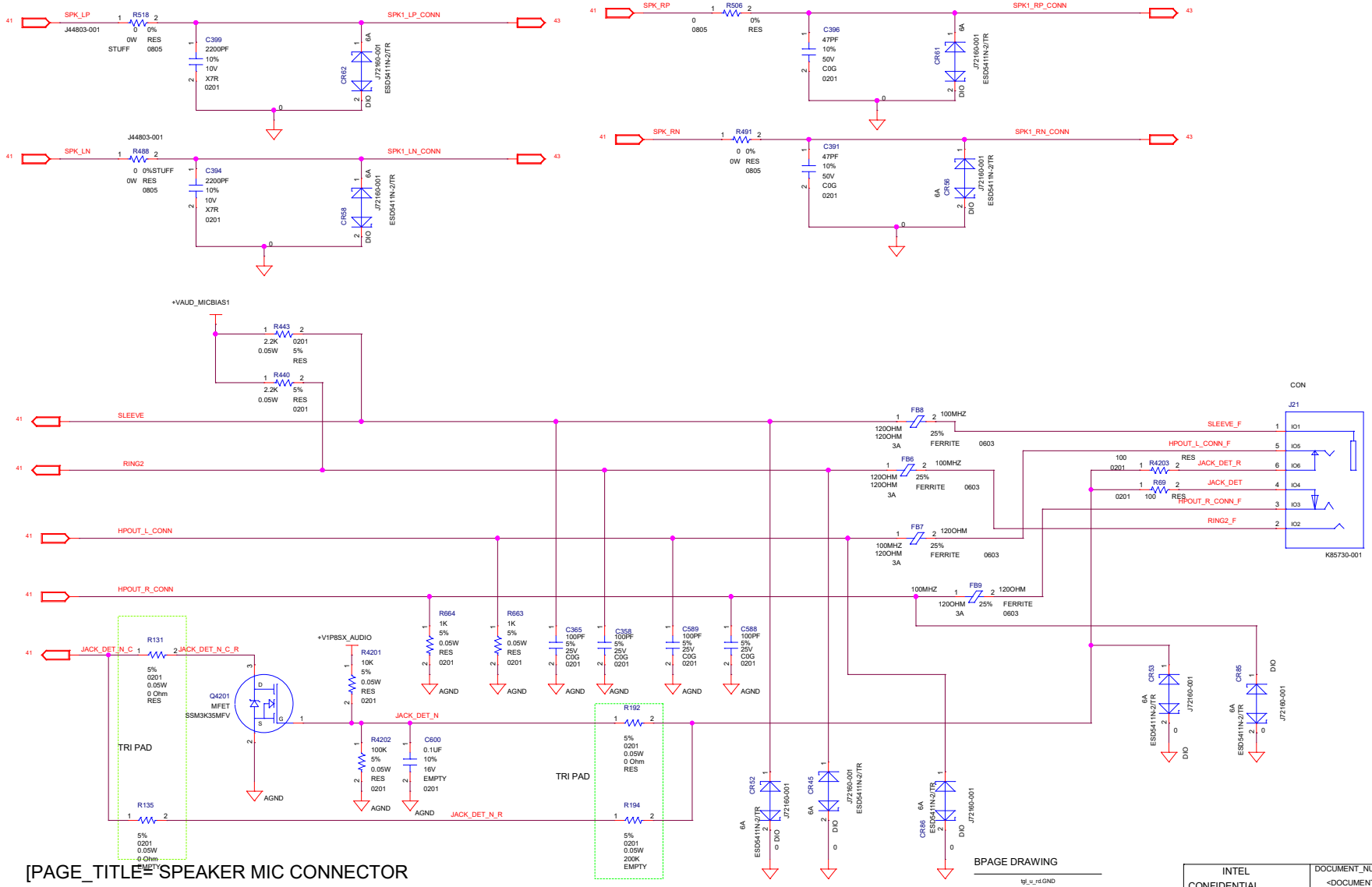
[PAGE_TITLE=AUDIO CODEC]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	41	1P0

CUSTOM TEXT BPAGE

AUDIO - SPEAKER

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= SPEAKER MIC CONNECTOR

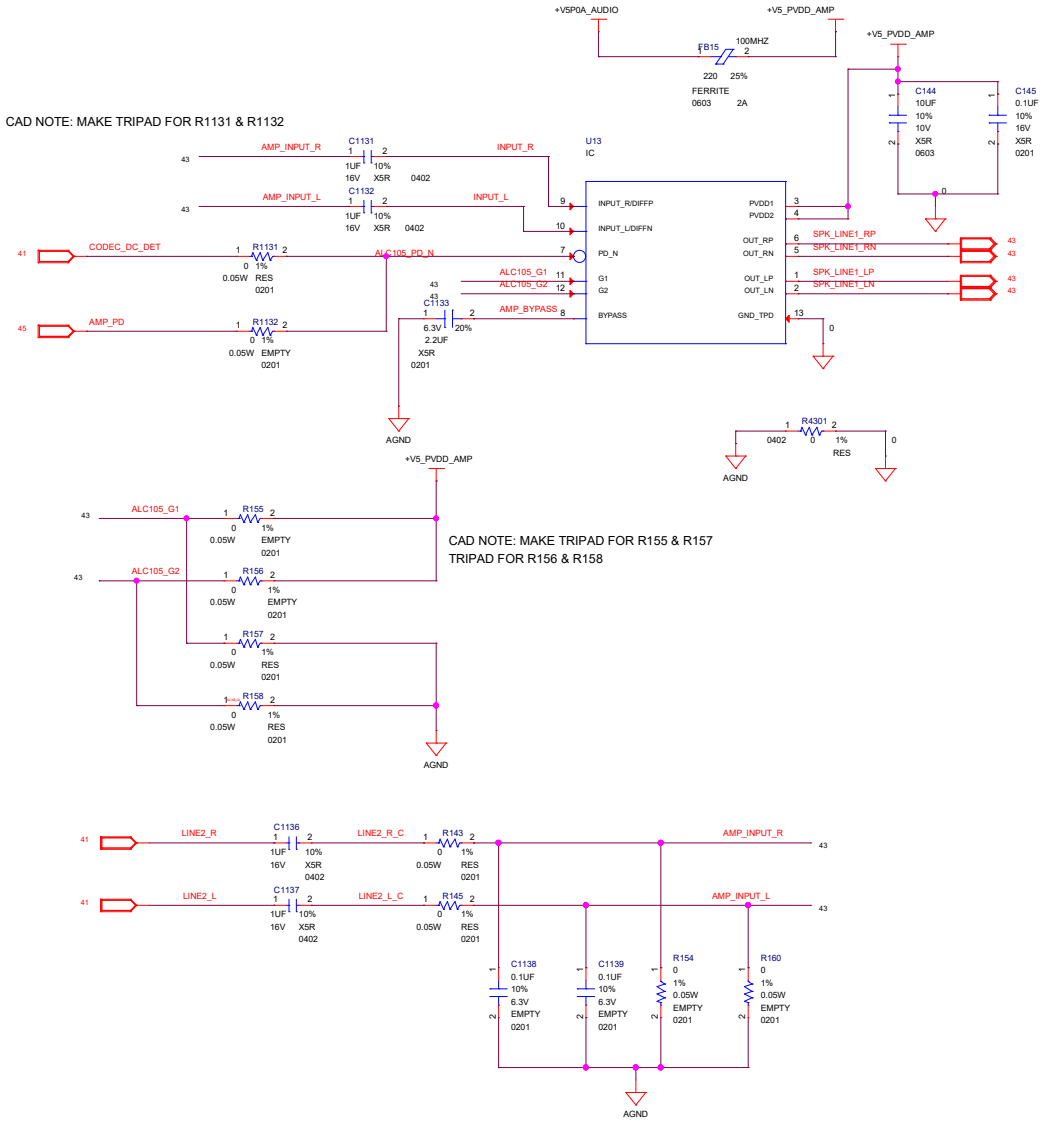
BPAGE DRAWING

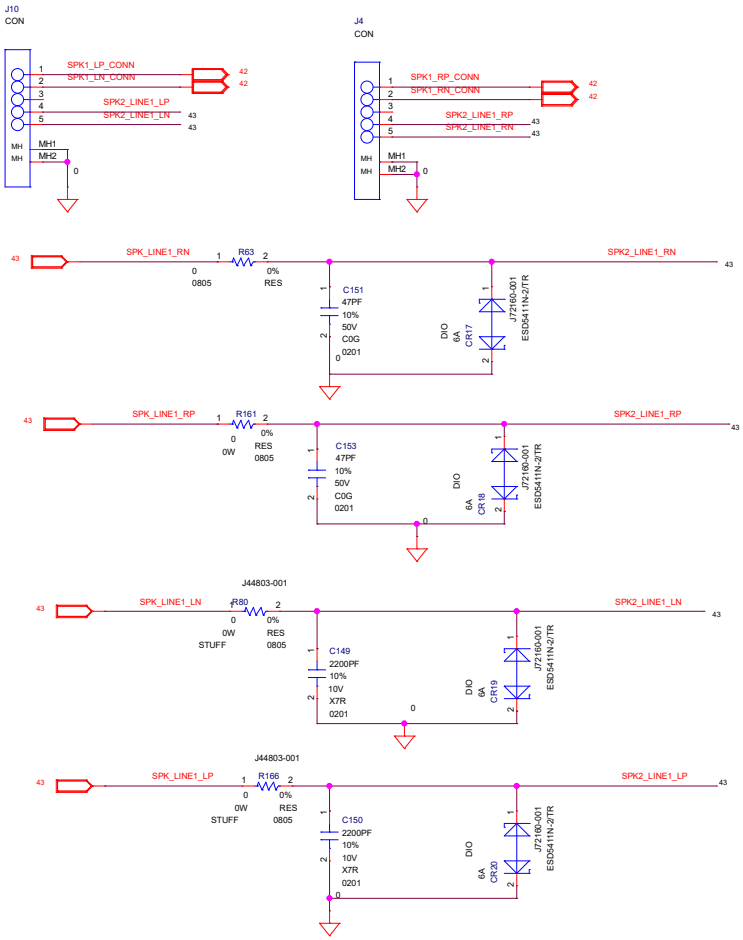
tgl_u_rd.GND
Fri Feb 28 13:40:59 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	42	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE





BPAGE DRAWING

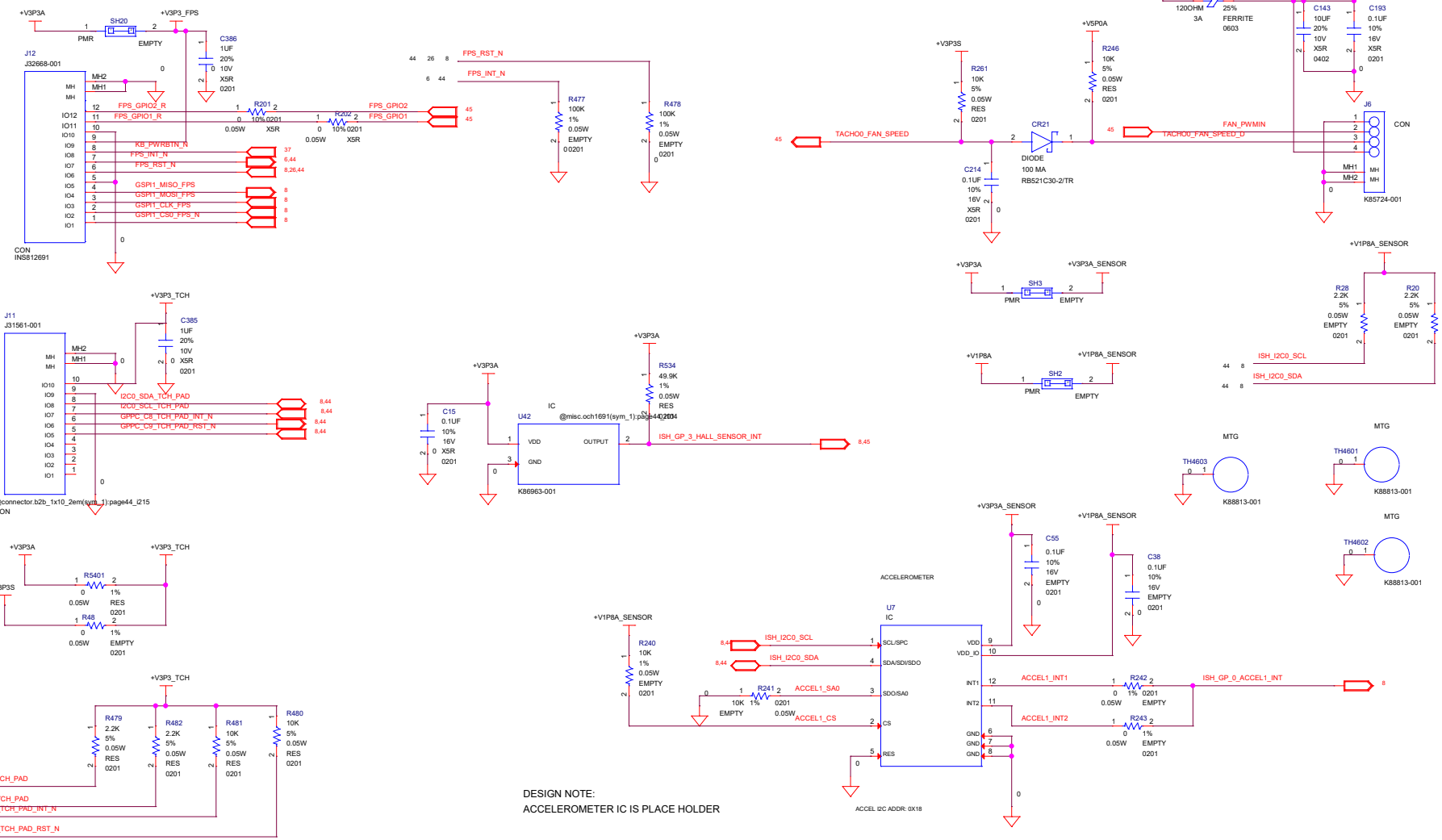
tgl_u_rd.GND
Fri Feb 28 13:40:59 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	43	1P0

CUSTOM TEXT BPAGE

FPS AND TOUCH CONNECTOR

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE= FPS & TOUCH CONNECTOR]

BPAGE DRAWING

tgl_u_rd:GND
Fri Feb 28 13:40:59 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	44	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

IC U41A

1 OF 2

IC U41B

2 OF 2

DESIGN NOTE:
H_VCCST_PWRGD SHOULD BE OPEN DRAIN
CONFIGURE ADP_DISABLE AS OPEN DRAIN

CAD NOTE:
R429 AND R428 SHOULD BE TRY PAD

CAD NOTE:
PLACE THRM_ALERT3 AWAY FROM EC

CAD NOTE:
C393 AND C392 SHOULD BE REFERENCED TO PIN AVSS

BPAGE DRAWING

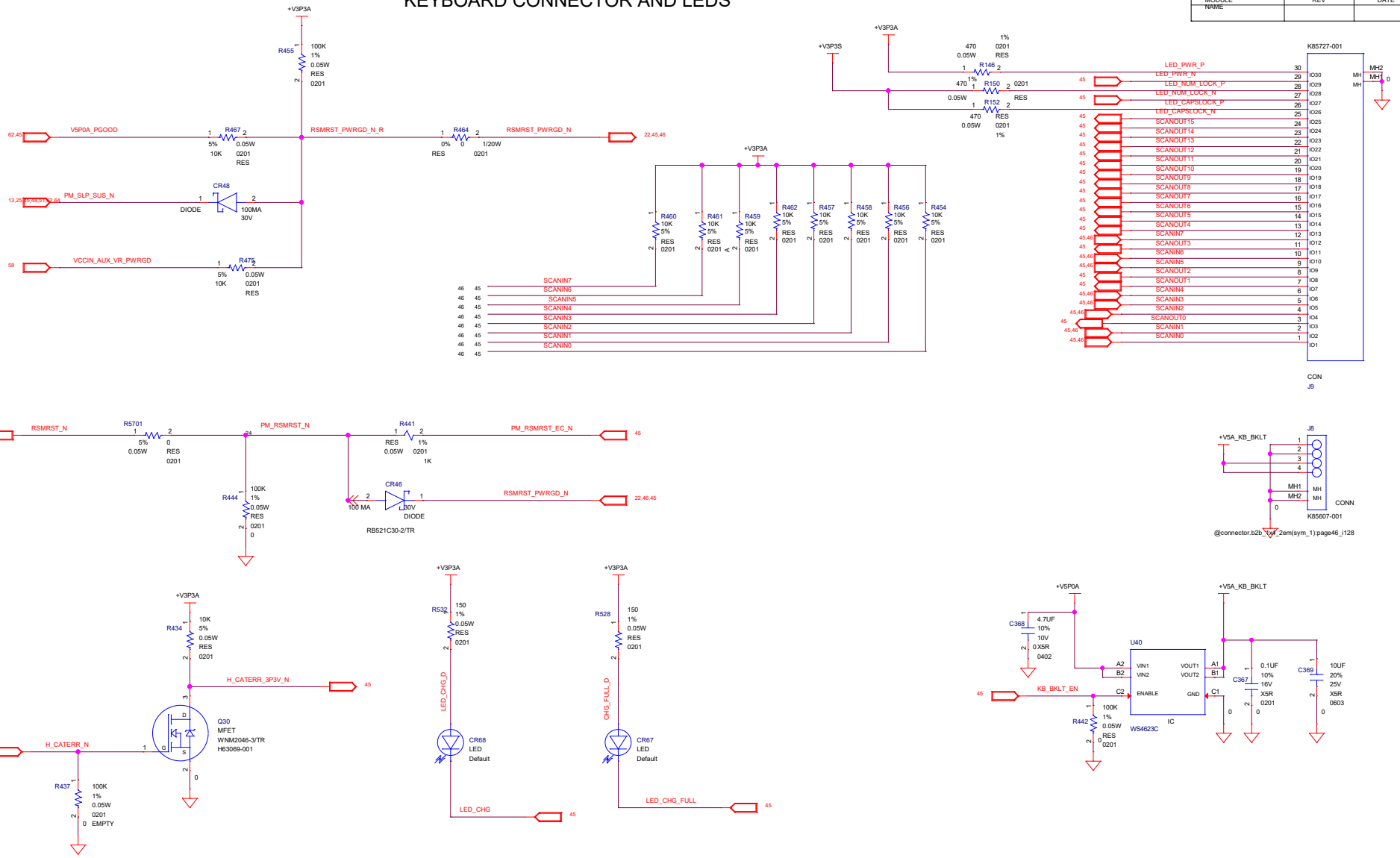
tgl_u_rd3@0wj 45
Fri Feb 28 13:41:00 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	45	1P0

CUSTOM TEXT BPAGE

KEYBOARD CONNECTOR AND LEDS

MODULE REV DETAILS		
MODULE NAME	REV	DATE



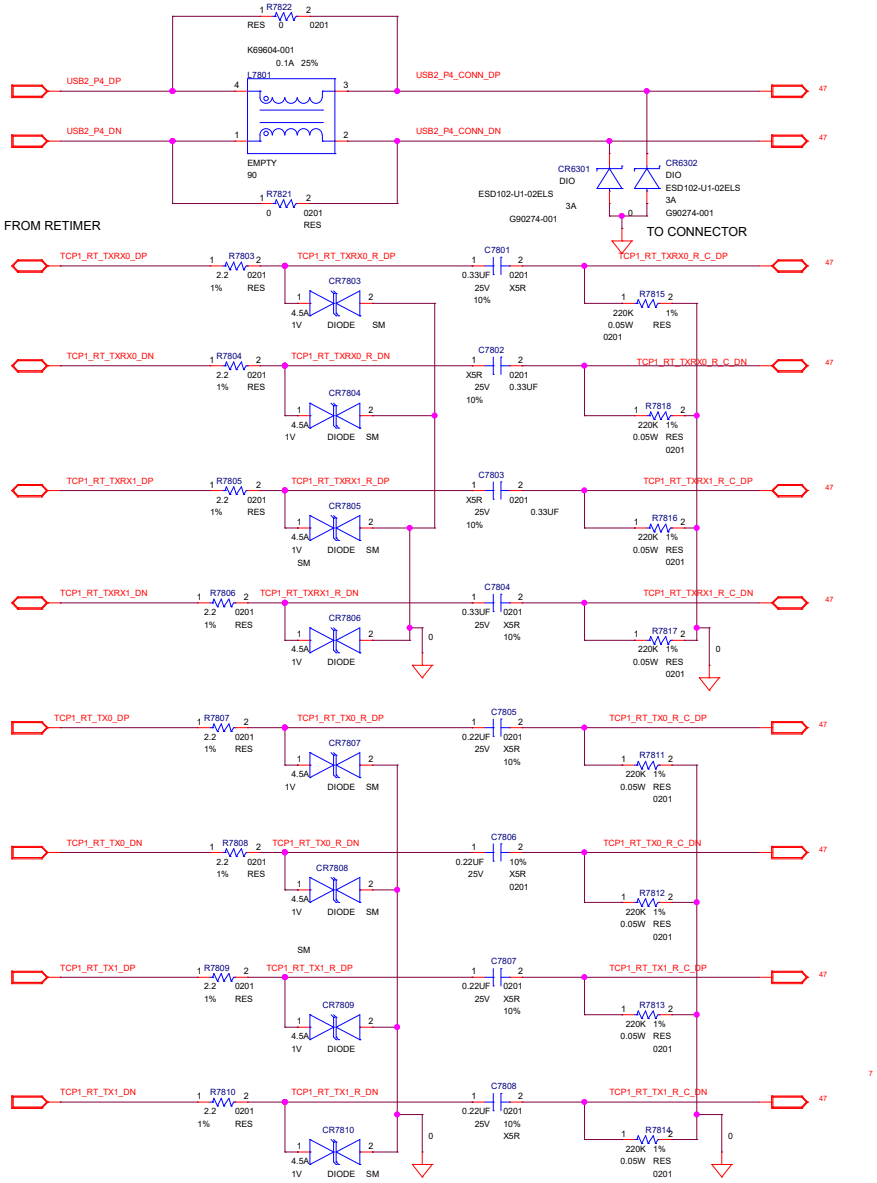
BPAGE DRAWING

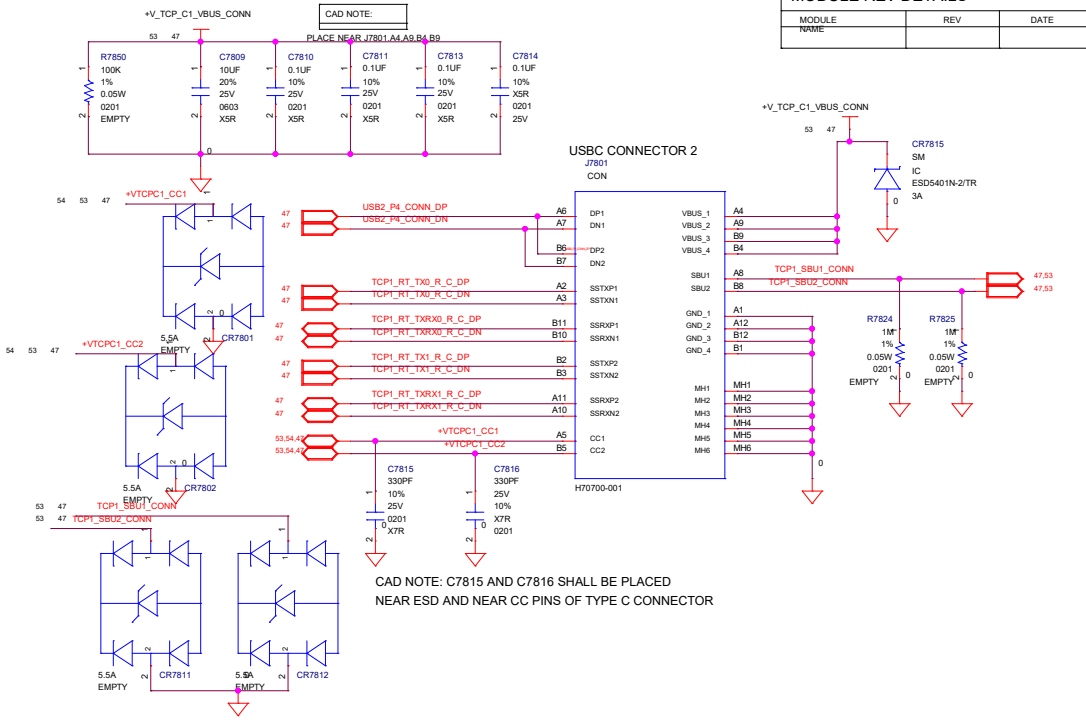
tgl_u_rd.GND
Fri Feb 28 13:41:00 2020

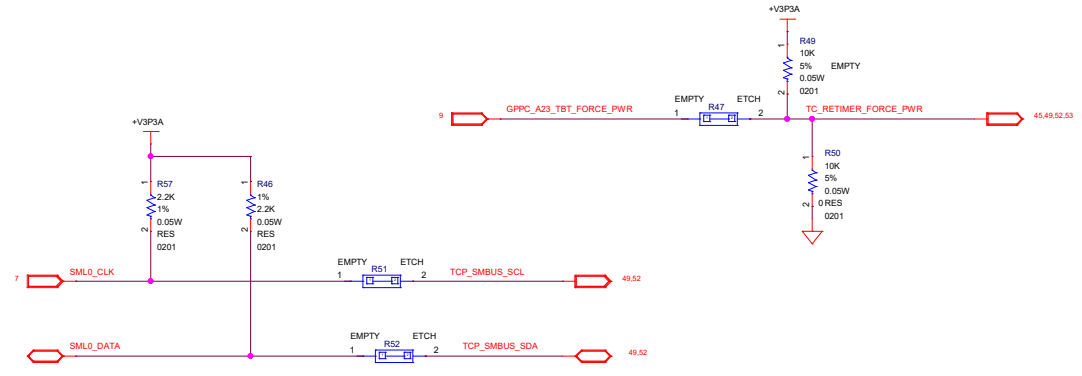
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	46	1P0

CUSTOM TEXT BPAGE

TYPE-C TBT PORT-1







MODULE REV DETAILS		
MODULE NAME	REV	DATE

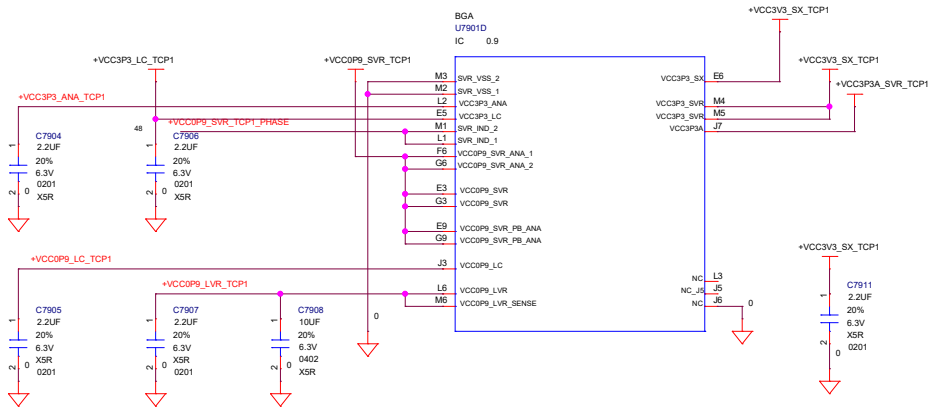
BPAGE DRAWING

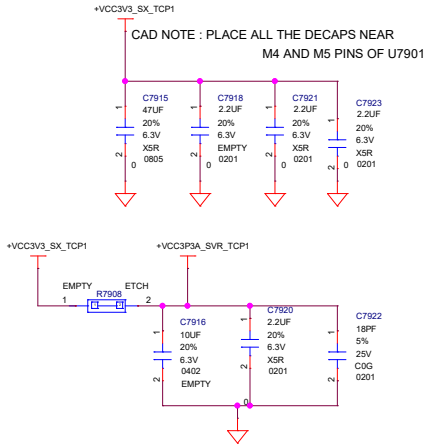
tgl_u_rd.tl'
Fri Feb 28 13:41:01 2020

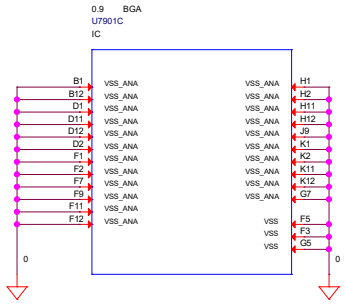
CUSTOM TEXT BPAGE

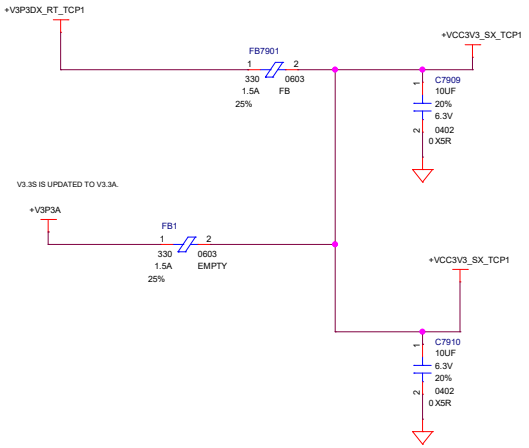
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	47	1P0

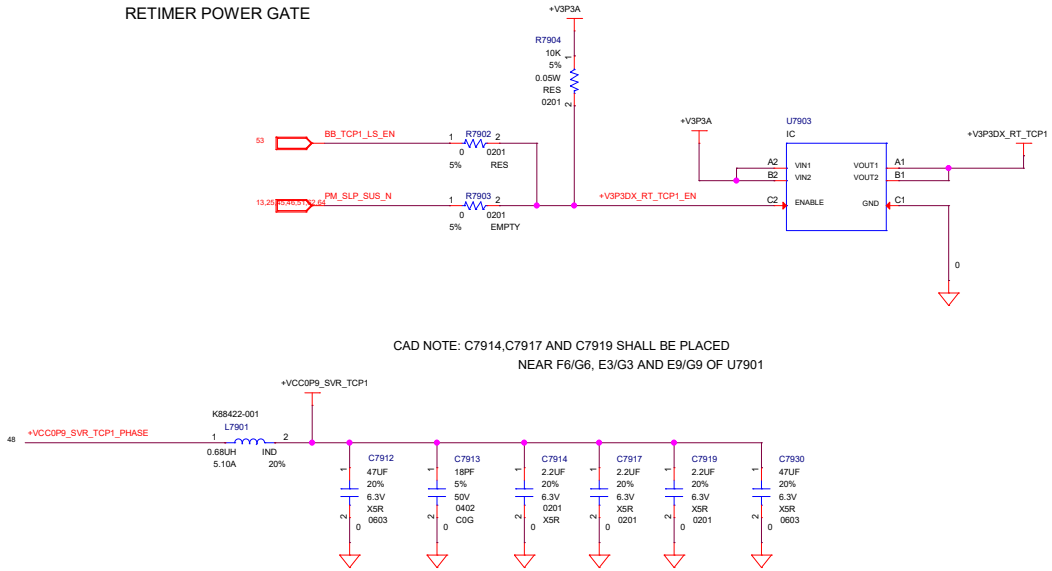
MODULE REV DETAILS		
MODULE NAME	REV	DATE











BPAGE DRAWING

tgl_u_rd:GND
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CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

ALL THESE CAPS ARE STUFFED

U7901A 0.9 IC BGA

U7901B BGA 0.9 IC

TCP1_TX0_DP / TCP1_TX0_DN — C8001 / C8005 0.22UF 10V 20% 0201 X5R — TCP1_TX0_C_DP / TCP1_TX0_C_DN — J1 / J2 ASSRXP1 / ASSRXN1

TCP1_TXRX0_DP / TCP1_TXRX0_DN — C8002 / C8006 — TCP1_TXRX0_C_DP / TCP1_TXRX0_C_DN — G1 / G2 ASSTXP1 / ASSTXN1

TCP1_TX1_DP / TCP1_TX1_DN — C8003 / C8007 — TCP1_TX1_C_DP / TCP1_TX1_C_DN — C1 / C2 ASSRXP2 / ASSRXN2

TCP1_TXRX1_DP / TCP1_TXRX1_DN — C8004 / C8008 — TCP1_TXRX1_C_DP / TCP1_TXRX1_C_DN — E1 / E2 ASSTXP2 / ASSTXN2

GPPC_E20_TBT_LSX1_TXD / GPPC_E21_TBT_LSX1_RXD — M7 / L7 PA_LSTX_SBU1 / PA_LSRX_SBU2

TCP1_AUX_DP / TCP1_AUX_DN — L8 / M8 PA_AUX_P / PA_AUX_N

BSSRXP1 / BSSRXN1 — J12 / J11 — TCP1_RT_TXRX1_DN / TCP1_RT_TXRX1_DP

BSSTXP1 / BSSTXN1 — G12 / G11 — TCP1_RT_TX1_DN / TCP1_RT_TX1_DP

BSSRXP2 / BSSRXN2 — C12 / C11 — TCP1_RT_TXRX0_DP / TCP1_RT_TXRX0_DN

BSSTXP2 / BSSTXN2 — E12 / E11 — TCP1_RT_TX0_DP / TCP1_RT_TX0_DN

BSBU1 / BSBU2 — M10 / L10 — TCP1_SBU1 / TCP1_SBU2

R8004 1M 1% 0.05W 0201 EMPTY

R8005 1M 1% 0.05W 0201 EMPTY

BB_TCP1_FLASH_CLK / BB_TCP1_FLASH_CS_N / BB_TCP1_FLASH_DI / BB_TCP1_FLASH_DO — C7 / B6 / C6 / B4 EE_CLK / EE_CS_N / EE_DI / EE_DO

TCP1_RT_TDI / TCP1_RT_TMS / TCP1_RT_TCK / TCP1_RT_TDO — A3 / C3 / B5 / C5 TDI / TMS / TCK / TDO

TP_TCP1_THERMDA — M11 THERMDA — TP8001 EMPTY

TEST_EDM / FUSE_VQPS_64 — M12 / B2

MONDC / NC / MONDC_SVR — A11 / A12 / L12 — TP_TCP1_BB_NC

TEST_PWR_GOOD / TEST_EN — B3 / B11 — BB_TCP1_TEST_PWR_GOOD

ATEST_P / ATEST_N — A1 / A2 — TP_TCP1_ATEST_P / TP_TCP1_ATEST_N

I2C_SDA / I2C_SCL / I2C_INT — E7 / C9 / A10 — I2C_PD_RT0_RT1_SDA / I2C_PD_RT0_RT1_SCL / I2C_RT0_RT1_PD_INT_N

FORCE_PWR / FLASH_BUSY_N / POC_GPIO_5 / POC_GPIO_6 / PERST_N — B10 / A9 / B9 / A8 / B8 — I2C_RETIMER_FORCE_PWR / BB_TCP1_FLASH_BUSY_N / BB_TCP1_GPIO_5 / BB_TCP1_GPIO_6 / BB_TCP_PERST_R_N

SMBUS_SCL / SMBUS_SDA / POC_GPIO_10 / POC_GPIO_11 / POC_GPIO_12 — A7 / B7 / A4 / A5 / A6 — TCP_SMBUS_SCL / TCP_SMBUS_SDA / BB_TCP1_FLASH_SHARE_EN / BB_TCP1_FLASH_MSTR_SLV / BB_TCP1_GPIO_12

RESET_N — L11 — BB_TCP1_RESET_R_N

XTAL_25_IN / XTAL_25_OUT — L9 / M9 — XTAL_TCP1_25MHZ_IN / XTAL_TCP1_25MHZ_OUT

RBIAS / RSENSE — L4 / L5 — BB_TCP1_RBIAS / BB_TCP1_RSENSE — R8024 RES 4.75K 0402

SMB U8001 XTAL 25MHZ 0.003% — XTAL1 / XTAL2 / GND1 / GND2

C8010 18PF 2% 25V 0201 C0G

C8011 18PF 2% 25V 0201 C0G

CAD NOTE: STITCH AS MANY POSSIBLE GND VIAS OVER XTAL SHIELD

PM_SLP_S5_N — R8011 0 5% 0201 EMPTY — BB_TCP1_RESET_R_N

BB_TCP1_RESET_N — R8012 0 5% 0201 RES — R8013 100K 5% 0.05W 0201 RES

CAD NOTE: 3 PAD

GPD_7_BBT_TCP_RST_N — R8019 0 5% 0201 EMPTY — BB_TCP_PERST_R_N

PLTRST_R_N — R8020 0 5% 0201 RES — R8021 100K 5% 0.05W 0201 EMPTY

CAD NOTE: 3 PAD

+VCC3P3_LC_TCP1

R8014 10K 1% 0.05W 0201 EMPTY

R8015 10K 1% 0.05W 0201 EMPTY

R8016 10K 1% 0.05W 0201 EMPTY

R8017 10K 1% 0.05W 0201 EMPTY

TCP1_RT_TDI — TP8002 EMPTY

TCP1_RT_TMS — TP8003 EMPTY

TCP1_RT_TCK — TP8004 EMPTY

TCP1_RT_TDO — TP8005 EMPTY

FLASH SHARING CONFIGURATION

PLTRST_R_N — TAPPING THE SIGNAL — +VCC3V3_SX_TCP1

BB_TCP1_GPIO_6 — R8025 100K 5% 0.05W 0201 EMPTY — PM_SLP_S3_N

CAD NOTE: TRIPAD CA AND CB

CA / CB — R6501 100K 5% 0.05W 0201 RES

BB_TCP1_TEST_PWR_GOOD — R8026 100 1% 0.05W 0201 RES

BB_TCP1_GPIO_5 — R8027 10K 1% 0.05W 0201 RES

BB_TCP1_FLASH_SHARE_EN — R8028 10K 1% 0.05W 0201 EMPTY

R8032 10K 1% 0.05W 0201 RES

BB_TCP1_FLASH_MSTR_SLV — R8029 10K 1% 0.05W 0201 EMPTY

R8030 10K 1% 0.05W 0201 RES

BB_TCP1_GPIO_12 — R8031 10K 1% 0.05W 0201 EMPTY

+V3.3A_DSW_TCP0_1_D

R8001 4.7K 5% 1/20W RES 0201

R8002 2.2K 5% 0.05W RES 0201

R8003 2.2K 5% 0.05W RES 0201

+V3P3A — DIODE CR8001 100 MA RBS21C30-2/TR SM — +V3.3A_DSW_TCP0_1_D

C8009 2.2UF 20% 6.3V 0201 X5R

R8006 4.7K 5% 1/20W 0201 RES

IC U8002 SOIC

CS_N / DO_IO1 / WP_IO2_N / GND — VCC / HOLD_IO3_N / CLK / DI_IO0

BB_TCP01_FLASH_CS_N / BB_TCP01_FLASH_DO / BB_TCP01_FLASH_WP_N

BB_TCP01_FLASH_HOLD_N / BB_TCP01_FLASH_CLK / BB_TCP01_FLASH_DI

MANUAL BOM UPDATE. REPLACE U8002 BY K44942-004

BB_TCP0_FLASH_BUSY_N — R8018 EMPTY ETCH — BB_TCP1_FLASH_BUSY_N — R8023 10K 1% 0.05W 0201 RES — +V3.3A_DSW_TCP0_1_D

BPAGE DRAWING

tgf_u_rd.09

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CUSTOM TEXT BPAGE

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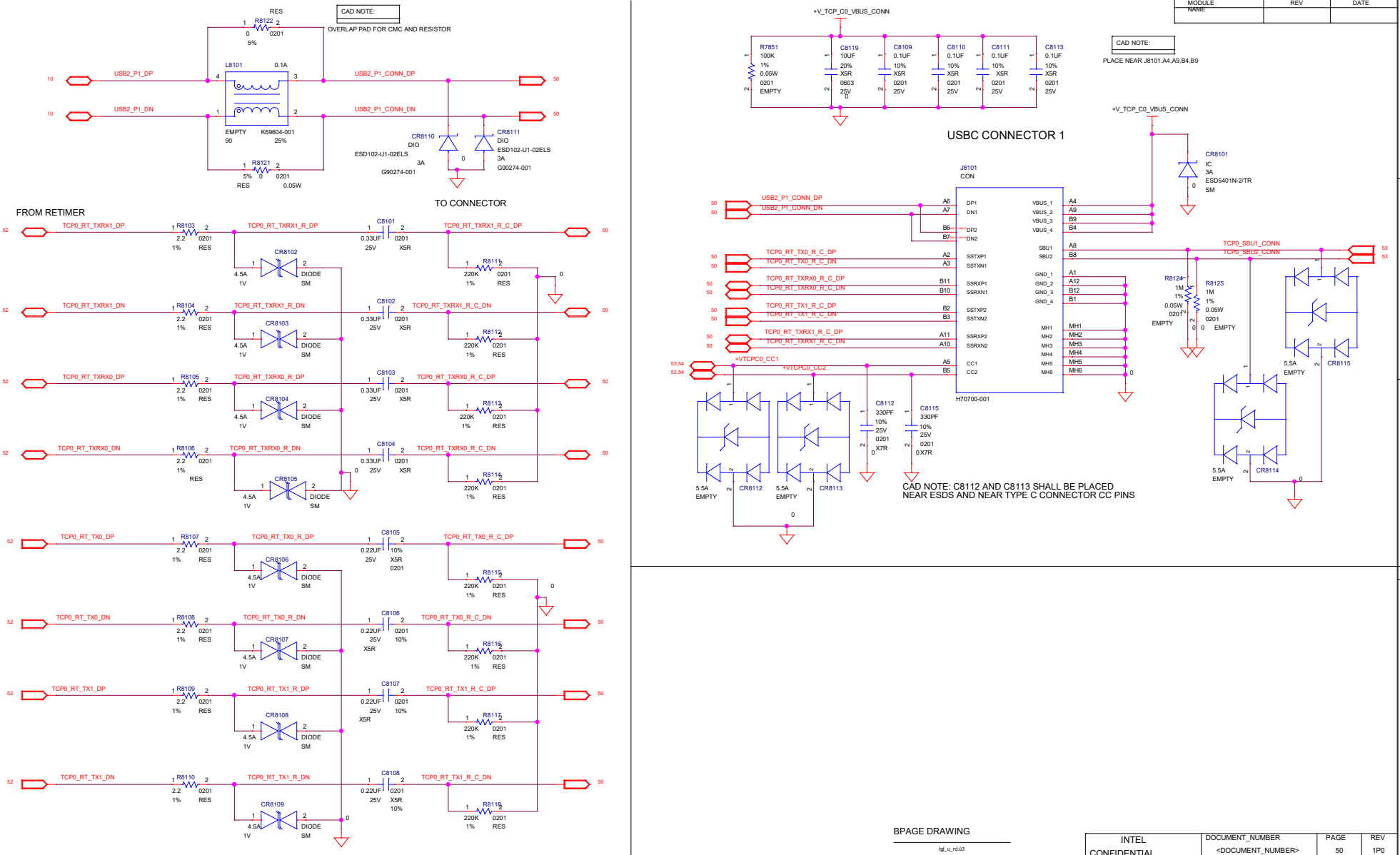

MODULE REV DETAILS

MODULE NAME	REV	DATE

BPAGE DRAWING

tgl_u_rd.i3
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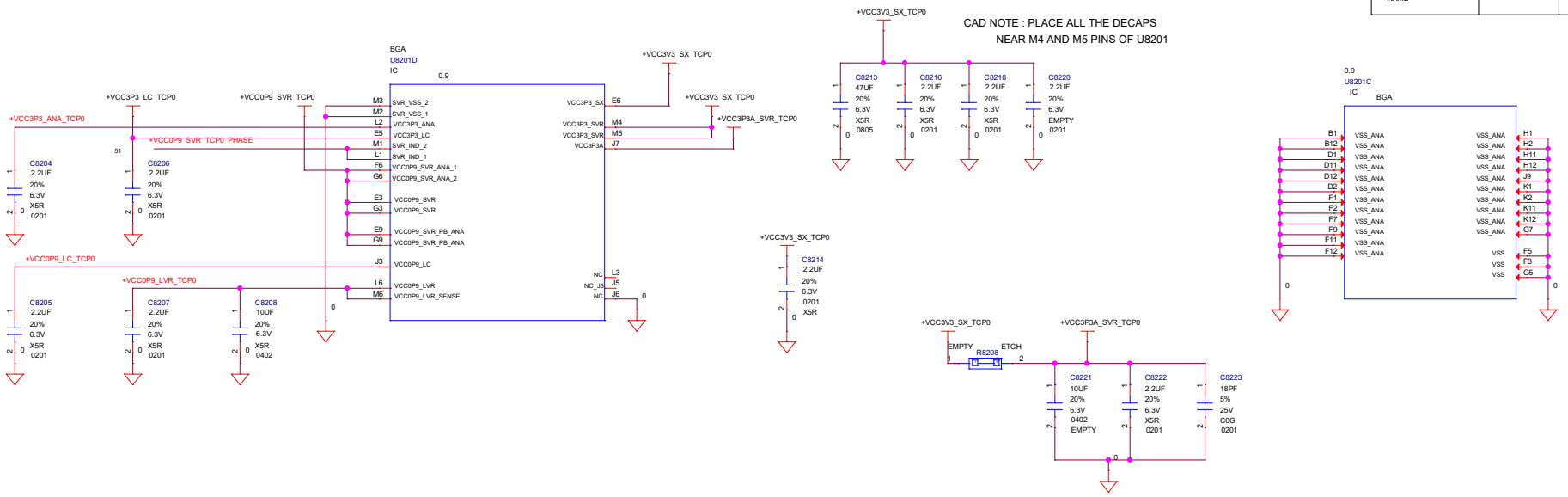
	<DOCUMENT_NUMBER>	50	1P0

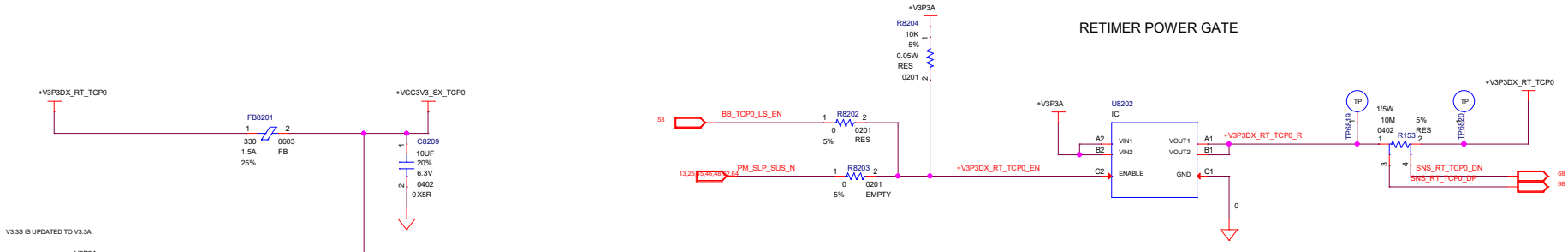
CUSTOM TEXT BPAGE

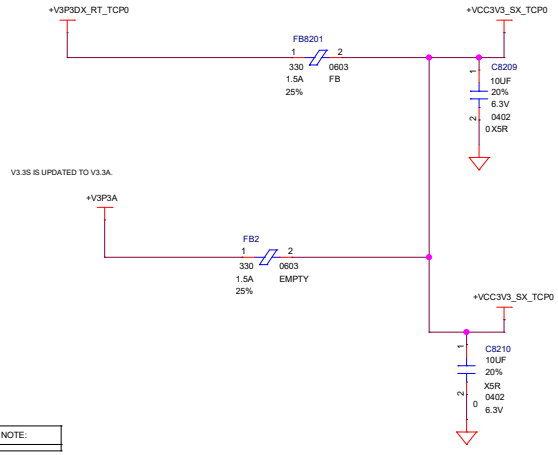
MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE : PLACE ALL THE DECAPS
NEAR M4 AND M5 PINS OF U8201

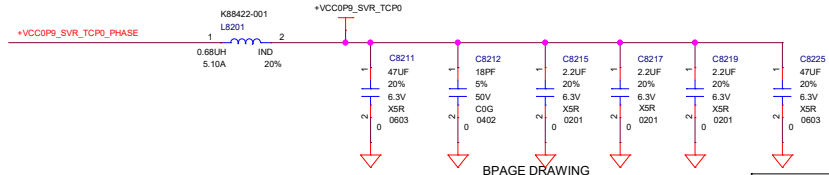


RETIMER POWER GATE





CAD NOTE: C8215,C8217 AND C8219 SHALL BE PLACED
NEAR F6/G6, E3/G3 AND E9/G9 OF U8201



CAD NOTE:
RA ,RB SHOULD BE 3 PAD RESISTOR

BPAGE DRAWING

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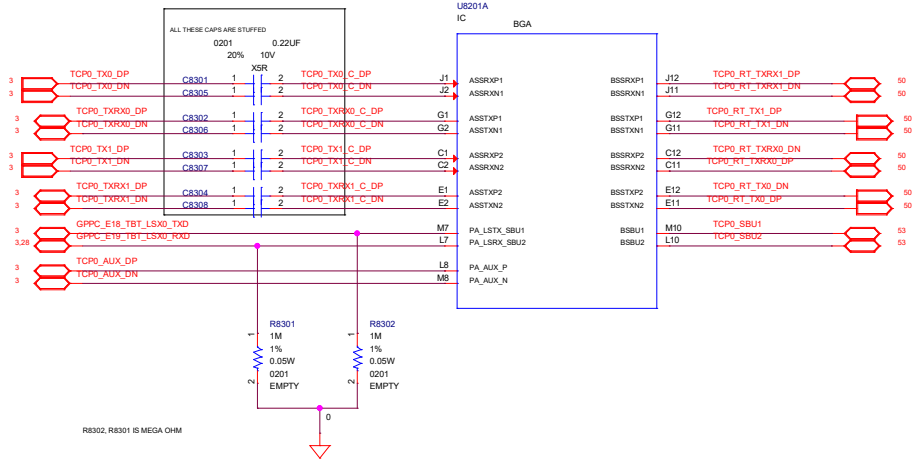
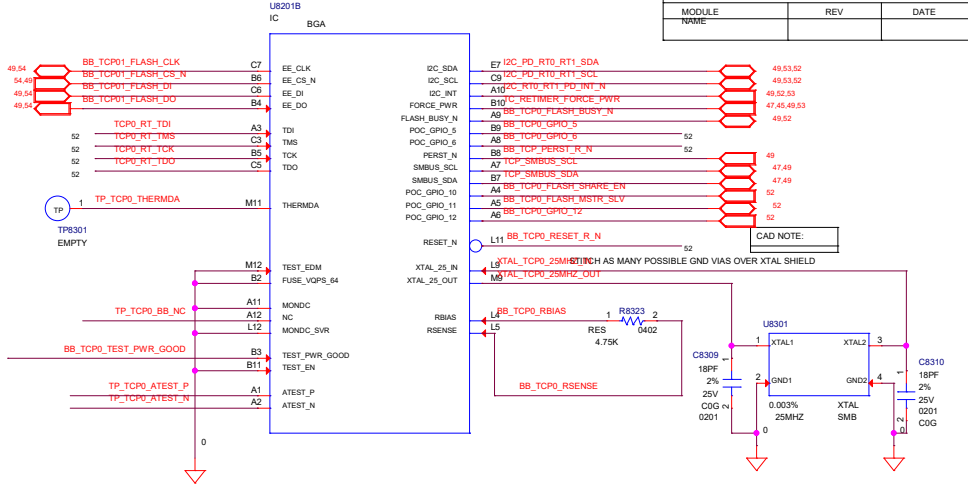
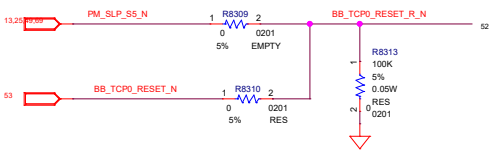
CUSTOM TEXT BPAGE

MODULE REV DETAILS

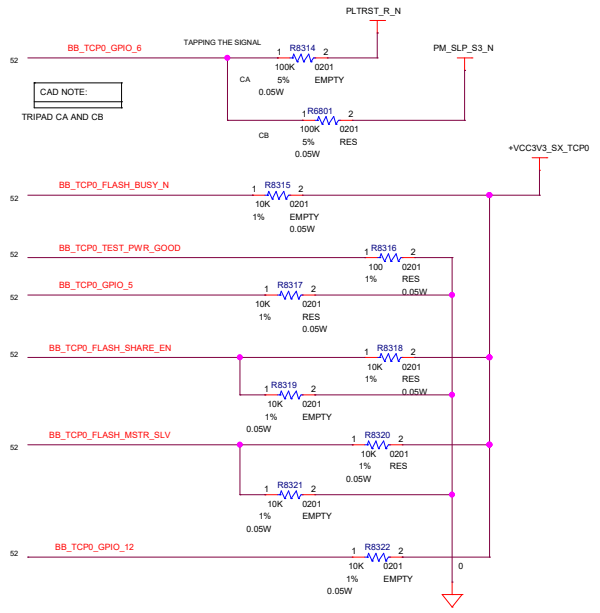
MODULE NAME	REV	DATE

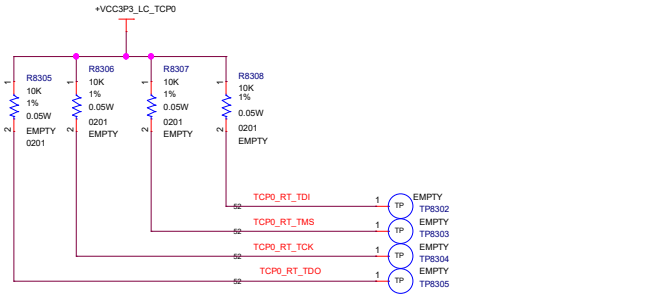


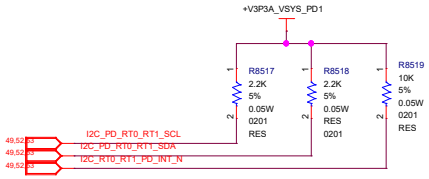


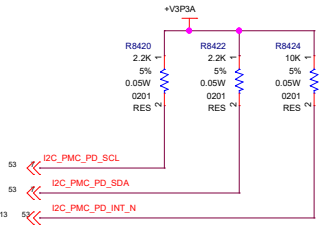


FLASH SHARING CONFIGURATION









BPAGE DRAWING

tgl_u_rd.PLTRS.52
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CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

SOURCE SWITCH

+V_TCP_C1_VBUS_CONN

C8609 10UF 20% X5R 0603 25V

R8601 0 ETCH_0805 EMPTY

CR8601 3A DB2W31900L DIODE SM

U8602 IC

C8611 10UF 20% 10V 0402 X5R

+V3P3A_VSYS_PD1

R8612 47K 5% 0.05W 0201 RES

+VCP_C1

TCPC_P1_ILIM

RILIM:53.6K: ILIM=0.9A

RILIM:17K: ILIM=3A

R8609 33K 1% 0.05W 0201 RES STUFF C48657-283

R8611 33K 1% 0.05W 0201 RES

USBC_P1_HI_CUR

TCPC_OC_P1_N

TCPC_P1_SRC_EN

TCPC_P1_FRS_EN

TCPC_P1_CAP

C8610 1000PF 10% 25V 0201 X7R

CSP

SOURCE SWITCH

PD CONTROLLER

TCPC_P1_SRC_HI_ILIM

Q8601 MFET

R8610 100K 1% 0.05W 0201 RES

U8601A IC

+VTCPC0_CC1 +VTCPC0_CC2

TCP0_SBU1_CONN TCP0_SBU2_CONN

TCPC_P0_FRS_EN

TCPC_P1_FRS_EN TCPC_OVP_TRIP_P1

BB_TCP0_RESET_N TC_RETIMER_FORCE_PWR

BC_PROCHOT_N_PD1_R

TCPC_P1_SRC_HI_ILIM TCPC_P0_SRC_HI_ILIM

BB_TCP1_LS_EN PD1_OC_P0_P1_N

PD1_SWD_DATA PD1_SWD_CLK_I2C_ADD

R6902 100K 1% 0.05W 0201 RES

R7101 EMPTY

R7102 ETCH

TCP0_PD_SBU1 TCP0_PD_SBU2

CC2_P1 CC1_P1 SBU2_P1 SBU1_P1 GPIO OVP_TRIP_P2/GPIO I2C_SDA_SCB4/OVP_TRIP_P1/GPIO VSEL_2_P2/GPIO VSEL_1_P2/GPIO UV_OCP_TRIP_P1/GPIO HPD_P2/GPIO HPD_P1/GPIO VCONN_OCP_TRIP_P2/GPIO VCONN_OCP_TRIP_P1/GPIO SWD_IO/AR_RST_N /GPIO SWD_CLK/I2C_CFG_EC/GPIO AUX_P_P1 AUX_N_P1 LSTX_P1 LSRX_P1 DMINUS_SYS_P1 DPLUS_SYS_P1 DMINUS_BOT_P1 DPLUS_BOT_P1 DMINUS_TOP_P1 DPLUS_TOP_P1 UART_TX_P1/GPIO UART_RX_P1/GPIO XRES

CC2_P2 CC1_P2 SBU2_P2 SBU1_P2 I2C_SCL_SCB1_EC/GPIO I2C_SDA_SCB1_EC/GPIO I2C_INT_EC/GPIO I2C_SCL_SCB2_TBT/GPIO I2C_SDA_SCB2_TBT/GPIO I2C_INT_TBT_P1/GPIO I2C_INT_TBT_P2/GPIO I2C_SCL_SCB4/GPIO I2C_SDA_SCB4/GPIO UV_OCP_TRIP_P2/GPIO I2C_SDA_SCB3/VSEL_2_P1/GPIO I2C_SCL_SCB3/VSEL_1_P1/GPIO AUX_P_P2 AUX_N_P2 LSTX_P2 LSRX_P2 DMINUS_SYS_P2 DPLUS_SYS_P2 DMINUS_BOT_P2 DPLUS_BOT_P2 DMINUS_TOP_P2 DPLUS_TOP_P2 UART_TX_P2/GPIO UART_RX_P2/GPIO

+VTCPC1_CC1 +VTCPC1_CC2

TCP1_SBU1_CONN TCP1_SBU2_CONN

PD_EC_SMBUS1_CLK PD_EC_SMBUS1_DATA PD_EC_SMBUS1_ALERT1_0_N I2C_PMC_PD_SCL I2C_PMC_PD_SDA I2C_PMC_PD_INT_N I2C_RT0_RT1_PD_INT_N

I2C_PD_RT0_RT1_SDA I2C_PD_RT0_RT1_SCL

TCP1_PD_SBU1 TCP1_PD_SBU2

R7103 EMPTY R7104 ETCH

BB_TCP0_LS_EN BB_TCP1_RESET_N

U8601 TO BE UPDATED WITH K53341-001

MANUAL BOM UPDATE

J65847-001

1 OF 2

PD CONTROLLER

PD1_SWD_CLK_I2C_ADD

PD1_XRES

R8603 1K 5% 0.05W 0201 EMPTY

R8602 4.7K 5% 0.05W 0201 RES

R8604 1K 5% 0.05W 0201 EMPTY

C8601 0.1UF 10% 6.3V 0201 X5R

+V3P3A_VDDD_PD1

+V3P3A_VSYS_PD1

C8608 2.2UF 20% 6.3V X5R 0201

C8607 0.1UF 10% 6.3V 0201 X5R

C8606 2.2UF 20% 6.3V X5R 0201

C8604 0.1UF 10% 6.3V 0201 X5R

+V3P3A_VCCD_PD1

C8603 0.1UF 10% 6.3V X5R 0201

C8602 0.1UF 10% 6.3V 0201 X5R

U8601B IC

VSYS VDDD VCCD VDDIO GND NC

CSP_P2 CSN_P2 VBUS_P2 VBUS_P_CTRL_P2 VBUS_C_CTRL_P2 VSV_P2 CSP_P1 CSN_P1 VBUS_P1 VBUS_P_CTRL_P1 VBUS_C_CTRL_P1 VSV_P1

PD1_CSP_P2 PD1_CSN_P2 TCPC_P1_SRC_EN_N TCPC_P1_SNK_EN_N PD1_CSP_P1 PD1_CSN_P1 TCPC_P0_SRC_EN_N TCPC_P0_SNK_EN_N

2 OF 2

J65847-001

R71 1K 5% 0.05W RES 0201

R72 1K 5% 0.05W RES 0201

PD_EC_SMBUS1_CLK

PD_EC_SMBUS1_DATA

SINK SWITCH

+V_TCP_C1_VBUS_CONN_R

+VCHG_PWR

+V_TCP_C1_FET

Q6901 MFET AON7409 H21795-001

C6901 1UF 20% 25V X5R 0402

R53 1% 49.9K 0.05W RES 0201

Q6902 MFET H21795-001 AON7409

TCPC_P1_SNK_EN_N

R205 10K RES

TCPC_P1_SNK_EN_N_R

+V_TCP_C1_VBUS_CONN_R

+V5P0A

C8612 0.1UF 10% 10V 0201 X5R

+V_TCP_C0_VBUS_CONN_R

C8605 0.1UF 10% 10V X5R 0201

EMPTY TP8609

BPAGE DRAWING

tgl_u_rd.dG

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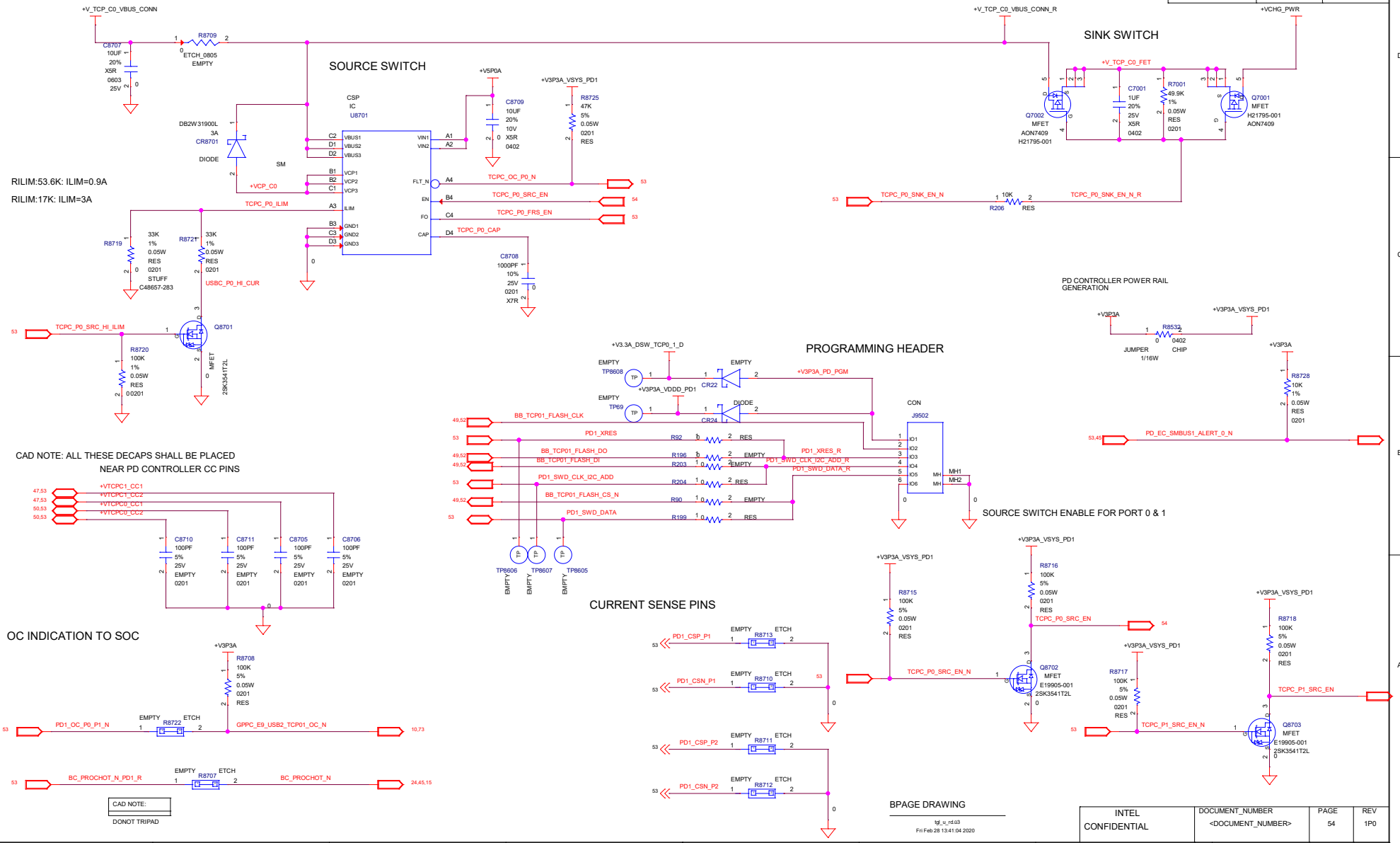
	<DOCUMENT_NUMBER>	53	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



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CUSTOM TEXT BPAGE

DESIGN NOTE:

BELOW RESISTOR OPTIONS SHALL BE USED
DURING PIN CONTROL MODE

USING INTERNAL PULL DOWN
[ADDR1,ADDR0] = 00

00 : 0X50 ~0X53 (DEFAULT)

CAD NOTE :

PLACE C73,C74,C76 CLOSE TO PIN 19,24,23 AND 22
PLACE C82,C83 CLOSE TO PIN 4 AND 10
PLACE C84 CLOSE TO PIN 34
PLACE C85,C87 CLOSE TO PIN 28
PLACE C7101 NEAR TO PIN 4

DESIGN NOTE:
FOR PS8761B,DNI R124
AND R125

FOR PS8761B,DNI C73 TO C87

DESIGN NOTE:
FOR PS8761B RETIMER,
REPLACE R67 WITH 2.2UF CAPACITOR

MODULE REV DETAILS		
MODULE NAME	REV	DATE

BPAGE DRAWING

tgl_u_rd.+V1P2.55
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	<DOCUMENT_NUMBER>	55	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:

BELOW RESISTOR OPTIONS SHALL BE USED
DURING PIN CONTROL MODE

CAD NOTE :

PLACE C100,C102,C104 CLOSE TO PIN 19,24,23 AND 22
PLACE C114,C115 CLOSE TO PIN 4 AND 10
PLACE C120 CLOSE TO PIN 34
PLACE C130,C134 CLOSE TO PIN 28
PLACE C7201 NEAR TO PIN 4

DESIGN NOTE:
FOR PS8761B,DNI R140
AND R142

[ADDR1,ADDR0] = 11
11 : 0XE4 ~0XE7

FOR PS8761B,DNI C100 TO C134

DESIGN NOTE:
FOR PS8761B RETIMER,
REPLACE R70 WITH 2.2UF
CAPACITOR

TRIPAD FOR R174 AND R5605

TRIPAD FOR R175 AND R5606

BPAGE DRAWING

tgl_u_rd.0-
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	<DOCUMENT_NUMBER>	56	1P0

CUSTOM TEXT BPAGE

M.2 KEY-E CONNECOR (WLAN)

MODULE REV DETAILS

MODULE NAME	REV	DATE

CAD NOTE: OVERLAP PAD FOR CMC AND RESISTOR

CAD NOTE: PLACE AC CAPACITORS WITHIN 8MM

CAD NOTE: PLACE CLOSE TO PIN 2 AND 4

CAD NOTE: PLACE CLOSE TO PIN 72 AND 74

CAD NOTE: TRIPAD FOR R162 AND R163
TRIPAD FOR R164 AND R165

MTG @board_artifacts.standoff(sym_1):page57_i187

BPAGE DRAWING

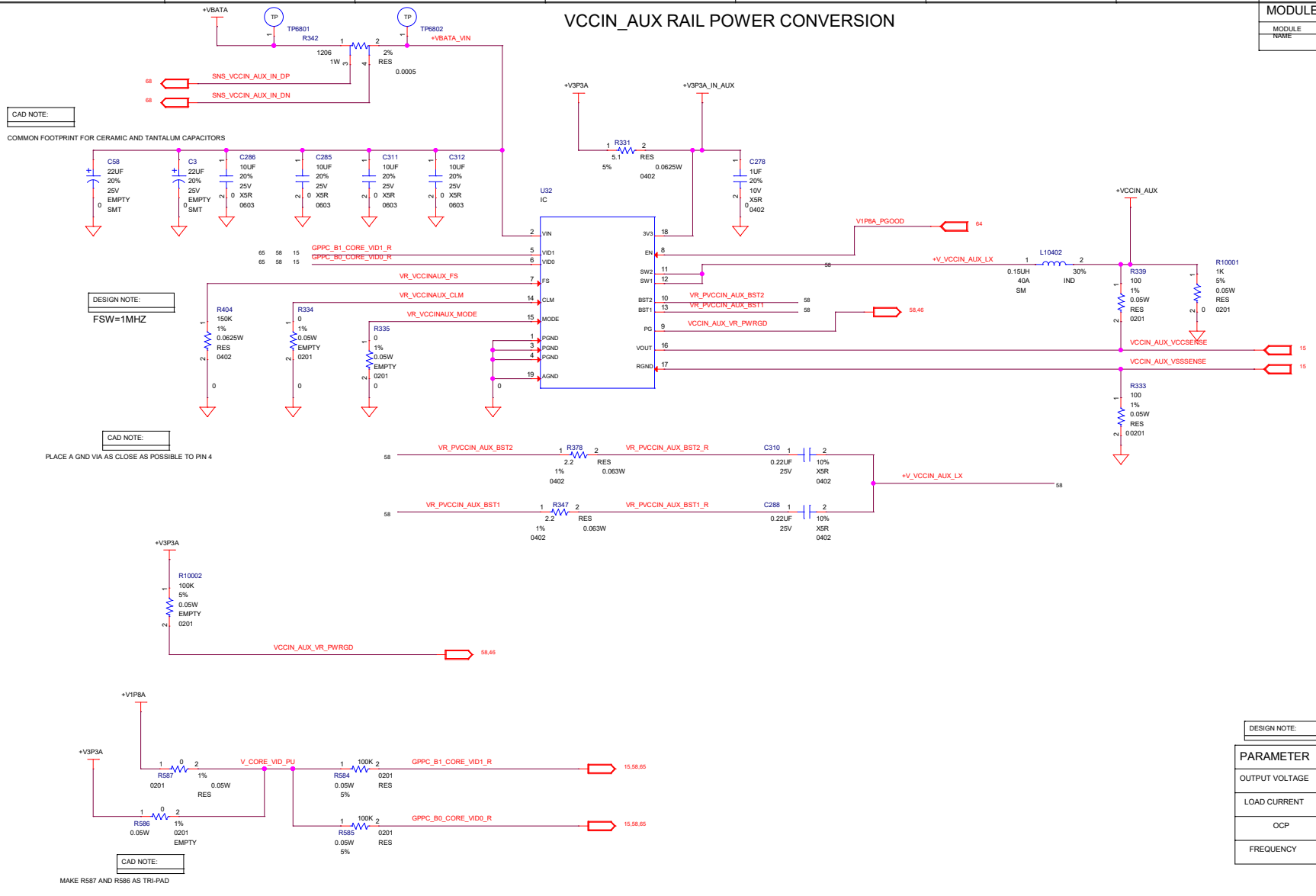
tgl_u_rd.01
Fri Feb 28 13:41:05 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	57	1P0

CUSTOM TEXT BPAGE

VCCIN_AUX RAIL POWER CONVERSION

MODULE REV DETAILS		
MODULE NAME	REV	DATE



DESIGN NOTE:

PARAMETER	SETTING
OUTPUT VOLTAGE	1.8V
LOAD CURRENT	32A
OCP	16A/PHASE
FREQUENCY	1000KHZ

BPAGE DRAWING

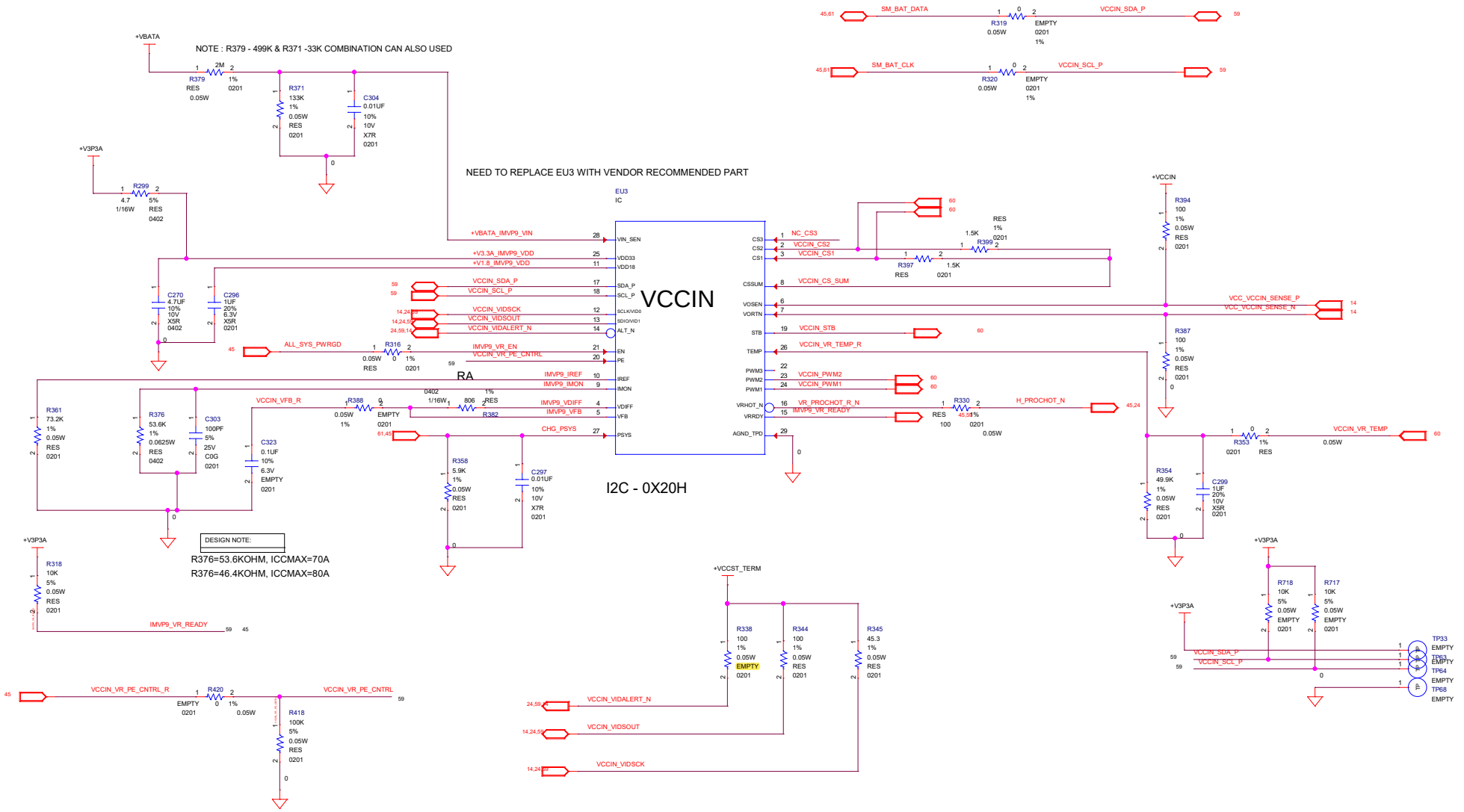
tgl_u_rd.GNDIG.58
Fri Feb 28 13:41:05 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	58	1P0

CUSTOM TEXT BPAGE

CPU RAILS IMVP 9 CONTROLLER

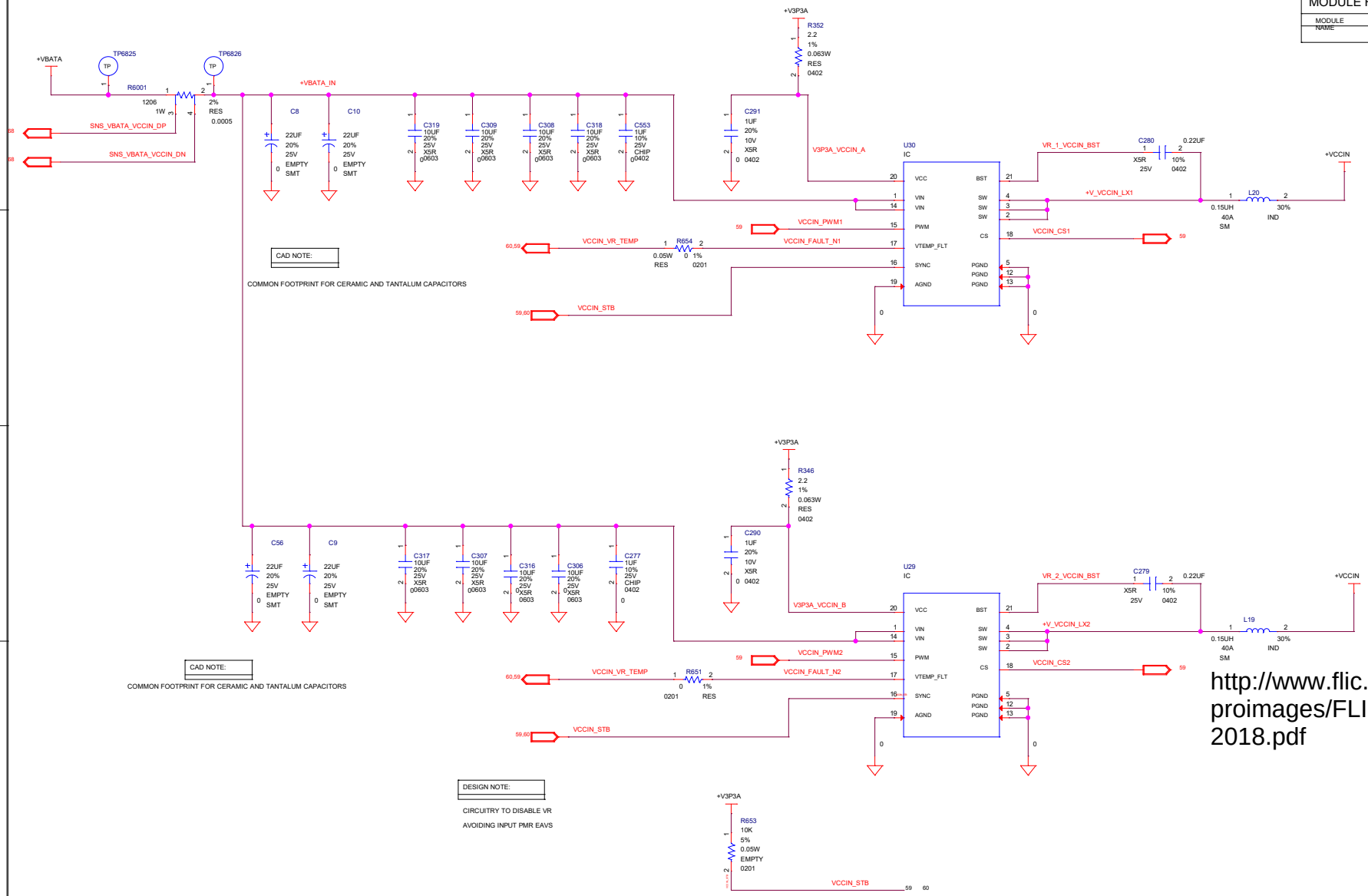
MODULE REV DETAILS		
MODULE NAME	REV	DATE



INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	59	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



http://www.flic.com.tw/proimages/FLIHP-6030---2018.pdf

BPAGE DRAWING

tgl_u_rd.07
Fri Feb 28 13:41:06 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	60	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

CAD NOTE:

COMMON FOOTPRINT FOR CERAMIC AND TANTALUM CAPACITORS ON +VCHG_PWR_IN AND +VACN_CHG

CAD NOTE:

CLOSE TO CHARGER IC
PLACE RESISTOR DIVIDER

CAD NOTE: USE COMMON FOOTPRINT FOR Q6101 AND Q6103
AND SIMILARLY Q6102 WITH Q6104
PARALLEL TO IT

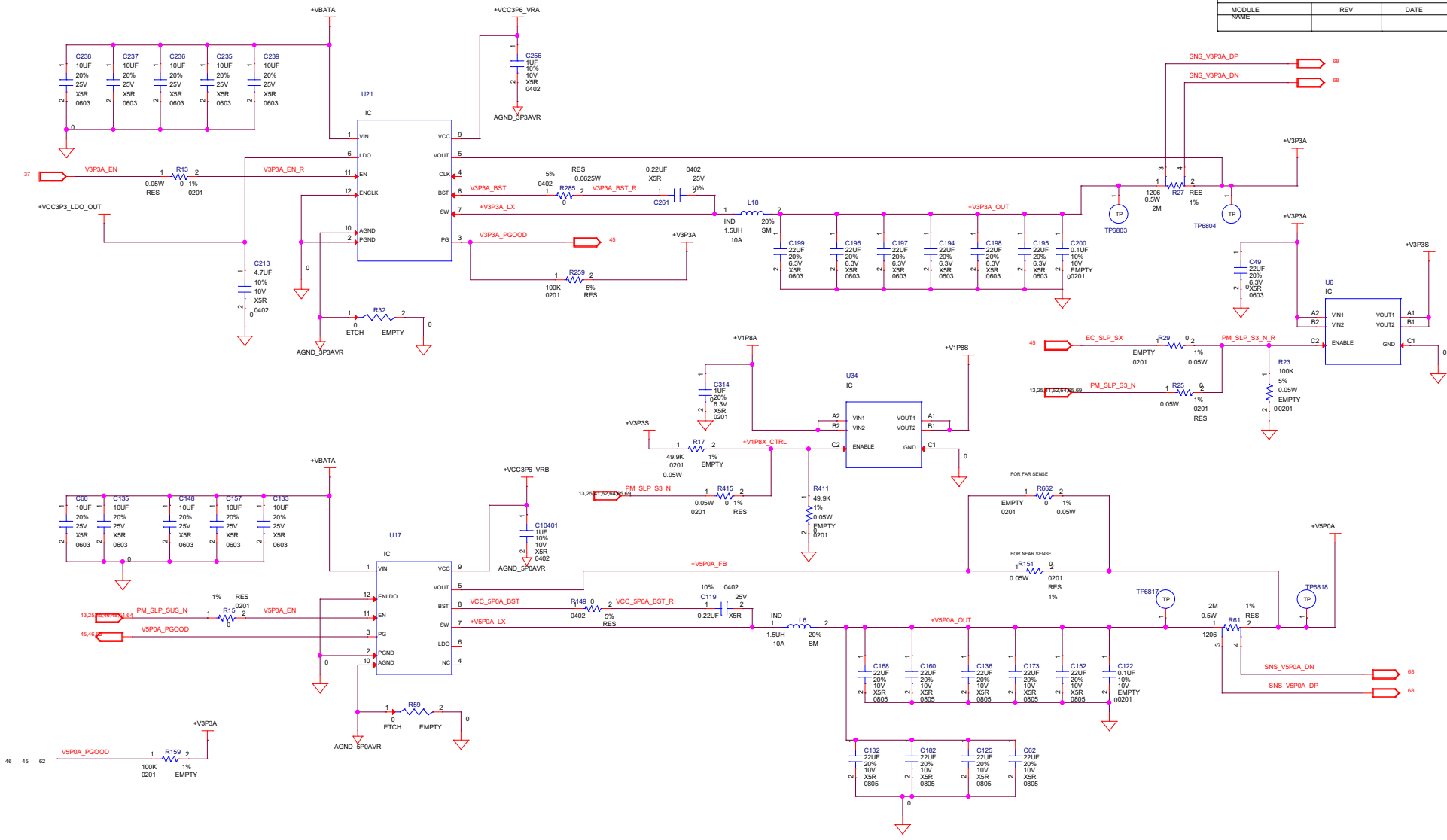
FOR NORMAL CHARGING SUPPORT	FOR FAST CHARGING SUPPORT
STUFF: Q6101 AND Q6102	STUFF: Q6103 AND Q6104
EMPTY: Q6103 AND Q6104	EMPTY: Q6101 AND Q6102

BPAGE DRAWING

tgl_u_rd.07
Fri Feb 28 13:41:06 2020

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	61	1P0

CUSTOM TEXT BPAGE


MODULE REV DETAILS
MODULE NAME
REV
DATE
+VBATA
+VCC3P6_VRA
AGND_3P3AVR
U21
IC
V3P3A_EN
V3P3A_EN_R
+VCC3P3_LDO_OUT
V3P3A_BST
V3P3A_BST_R
+V3P3A_LX
V3P3A_PGOOD
+V3P3A_OUT
SNS_V3P3A_DP
SNS_V3P3A_DN
+V3P3A
+V3P3S
AGND_5P0AVR
+VCC3P6_VRB
AGND_5P0AVR
U17
U34
U6
+V1P8A
+V1P8S
+V1P8X_CTRL
PM_SLP_S3_N
PM_SLP_S3_N_R
EC_SLP_SX
+V5P0A_FB
VCC_5P0A_BST
VCC_5P0A_BST_R
+V5P0A_LX
+V5P0A_OUT
PM_SLP_SUS_N
V5P0A_EN
V5P0A_PGOOD
SNS_V5P0A_DN
SNS_V5P0A_DP
FOR FAR SENSE
FOR NEAR SENSE
BPAGE DRAWING
tgl_u_rd.03
Fri Feb 28 13:41:07 2020
INTEL CONFIDENTIAL
DOCUMENT_NUMBER
<DOCUMENT_NUMBER>
PAGE
62
REV
1P0
CUSTOM TEXT BPAGE

VDD2 VPP AND VDDQ - POWER CONVERSION

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE:
PLACE C405
CLOSE TO PIN 1

CAD NOTE:
ADD EXTRA POWER SHAPES INCLUDING GND VIAS

DESIGN NOTE:
PLACE C45
NEAR TO INDUCTOR

DESIGN NOTE:
PLACE C52
CLOSE TO PIN 8

CAD NOTE:
PLACE R2 CLOSE TO THE VR AND TAKE +VDDQ FROM PMR NEAR TO MEMORY SECTION

WHILE VALIDATING NEED TO CHECK THE EFFICIENCY WITH AND WITHOUT USM MODE

DESIGN NOTE:

PARAMETER	SETTING
OUTPUT VOLTAGE	1.2V
LOAD CURRENT	8A
OCP	11.25A
FREQUENCY	700 KHZ
SOFT START	2.8 MILLI SEC

BPAGE DRAWING

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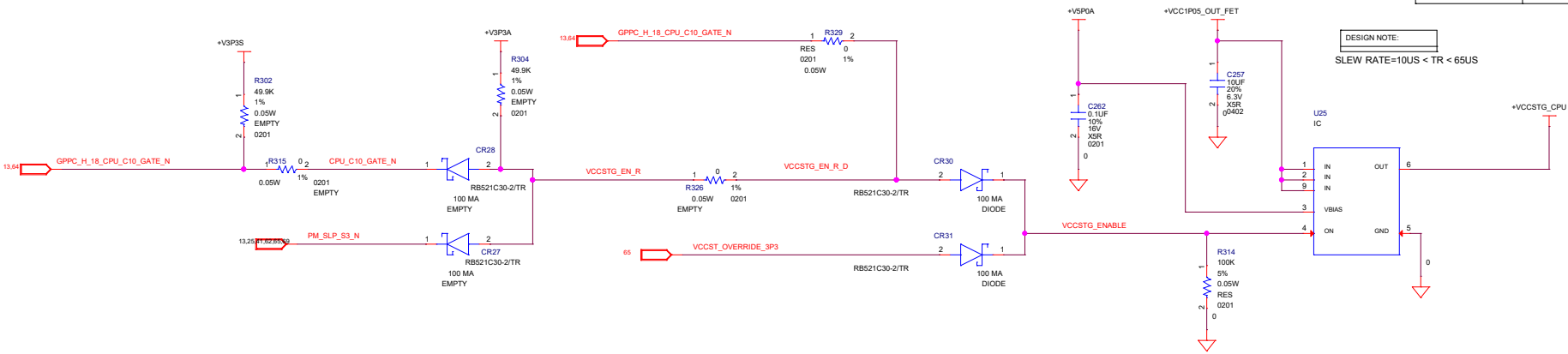
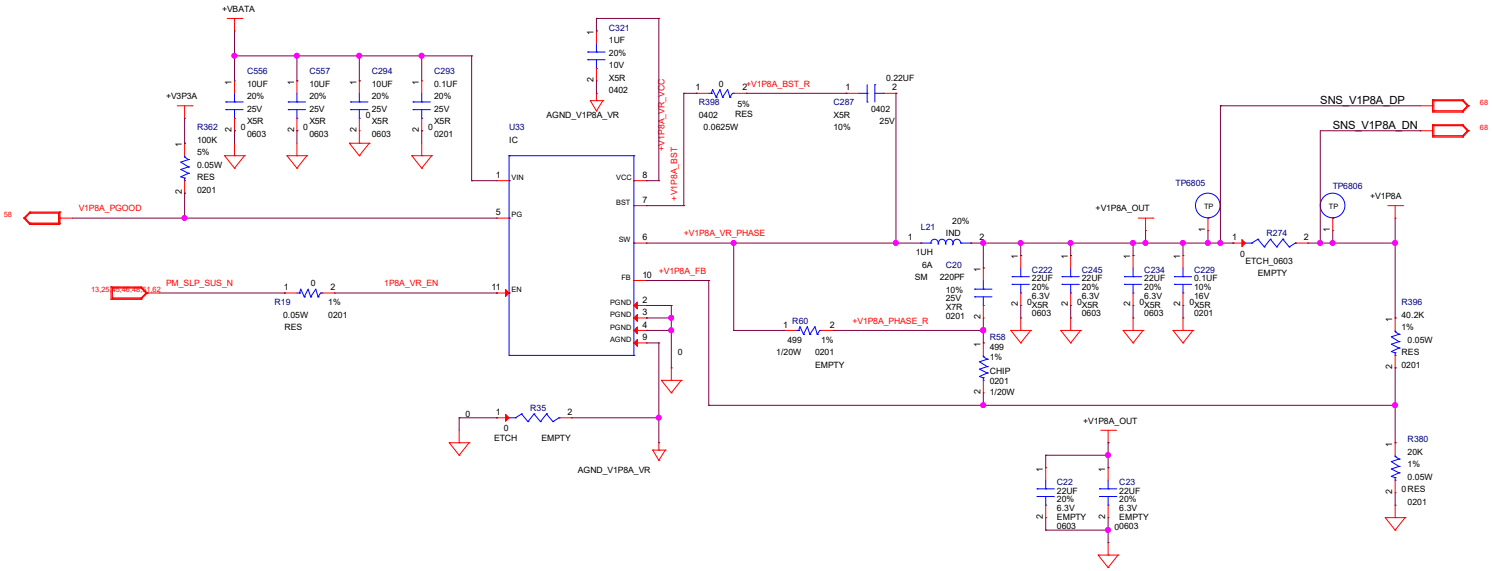
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	63	1P0

CUSTOM TEXT BPAGE

+VCCSTG RAIL GENERATION



+V1.8A GENERATION



MODULE REV DETAILS

MODULE NAME	REV	DATE

BPAGE DRAWING

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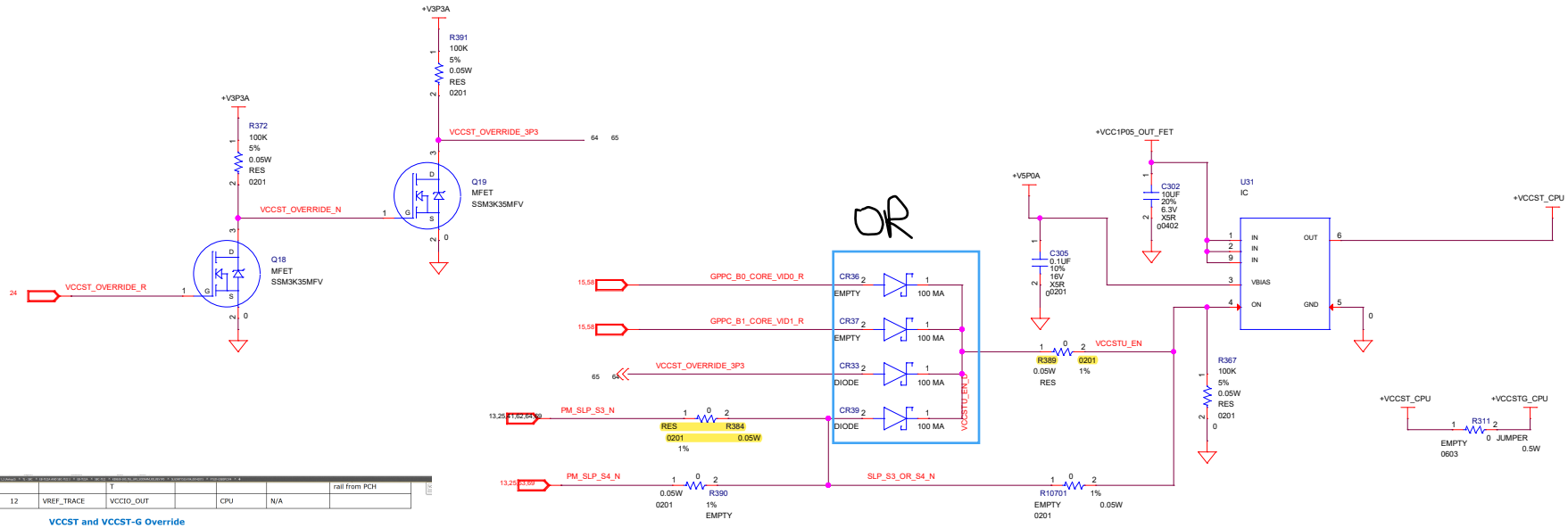
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	64	1P0

CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

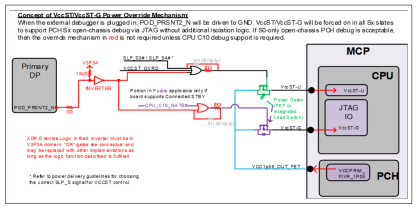
VCCST_CPU GENERATION



		T			rail from PCH
12	VREF_TRACE	VCCIO_OUT		CPU	N/A

VCCST and VCCST-G Override

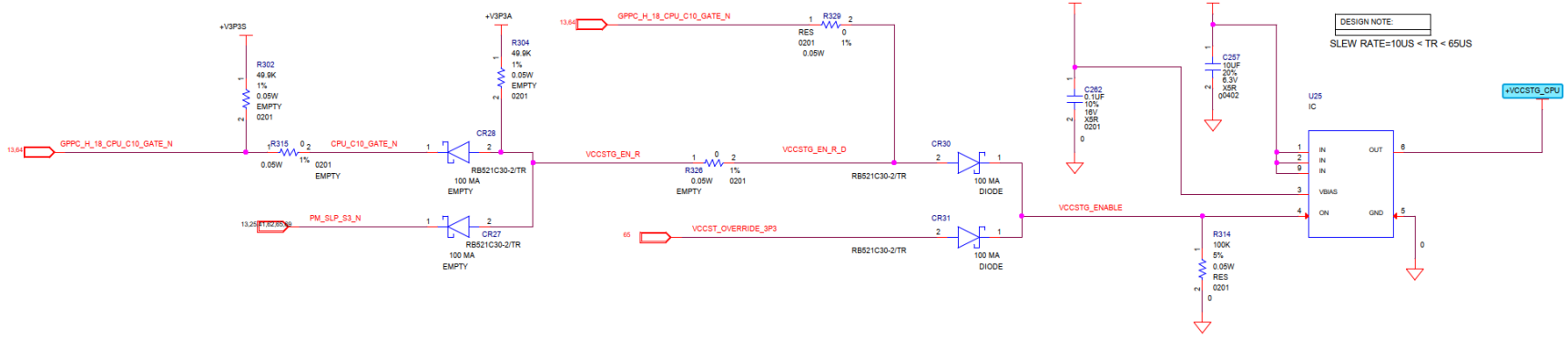
Figure 270. VCCST and VCCST-G Override



When no Type-C device is connected,
VCCST_OVERRIDE=LOW

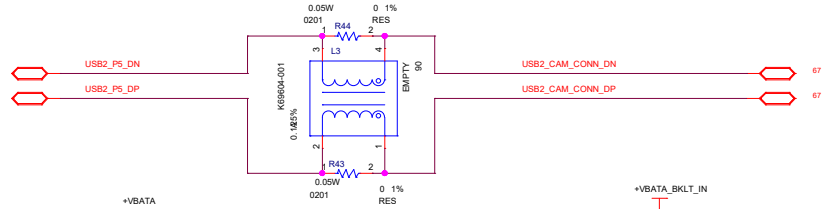
MODULE REV DETAILS		
MODULE NAME	REV	DATE

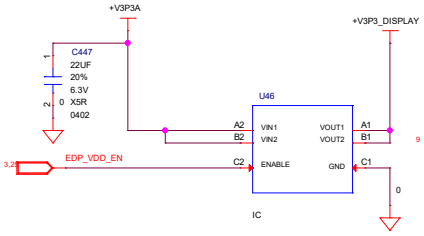
+VCCSTG RAIL GENERATION

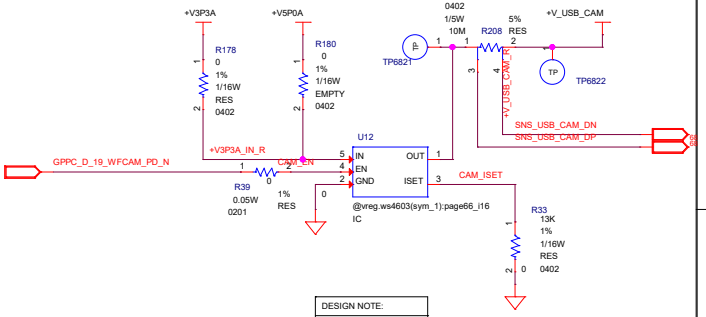


USB CAM AND EDP - MISC

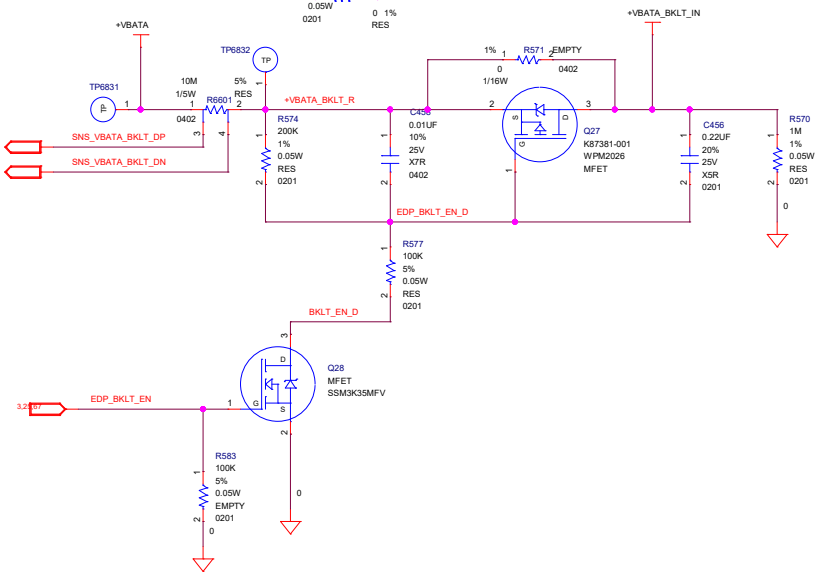
MODULE REV DETAILS		
MODULE NAME	REV	DATE

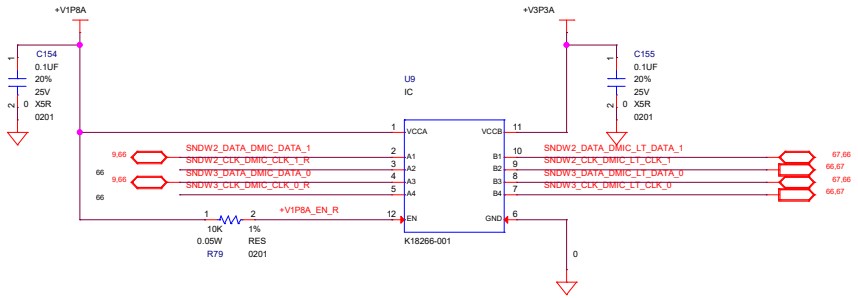




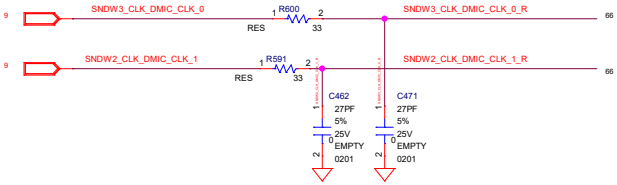


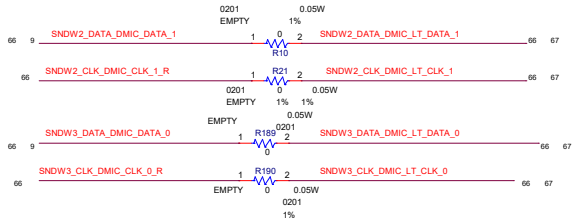
DESIGN NOTE:
ISET:- 567MA





CAD NOTE:
PLACE R600, C462, C471 AND R591 NEAR TO SOC





BPAGE DRAWING

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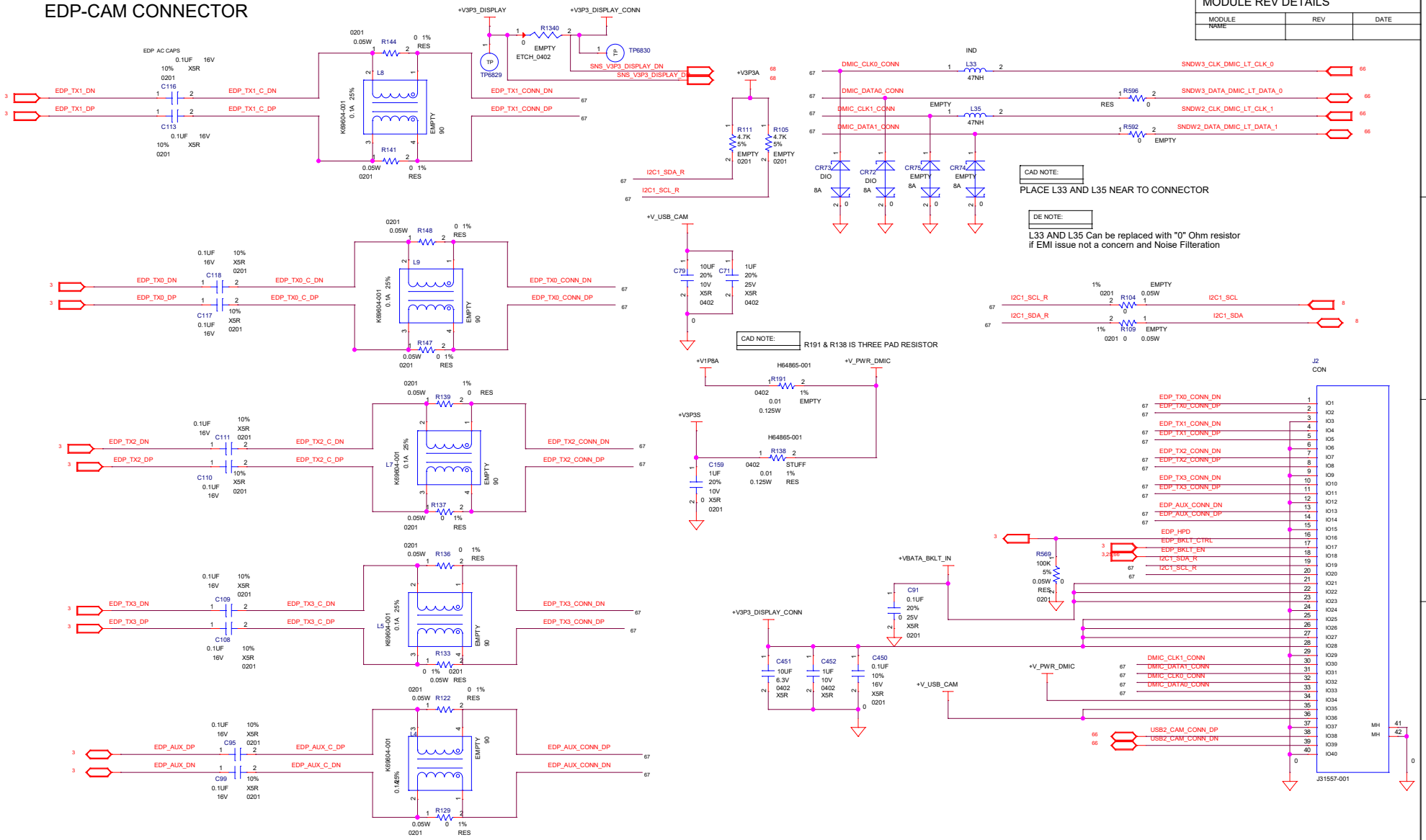
	<DOCUMENT_NUMBER>	66	1P0

CUSTOM TEXT BPAGE

EDP-CAM CONNECTOR



MODULE REV DETAILS

MODULE NAME	REV	DATE

BPAGE DRAWING

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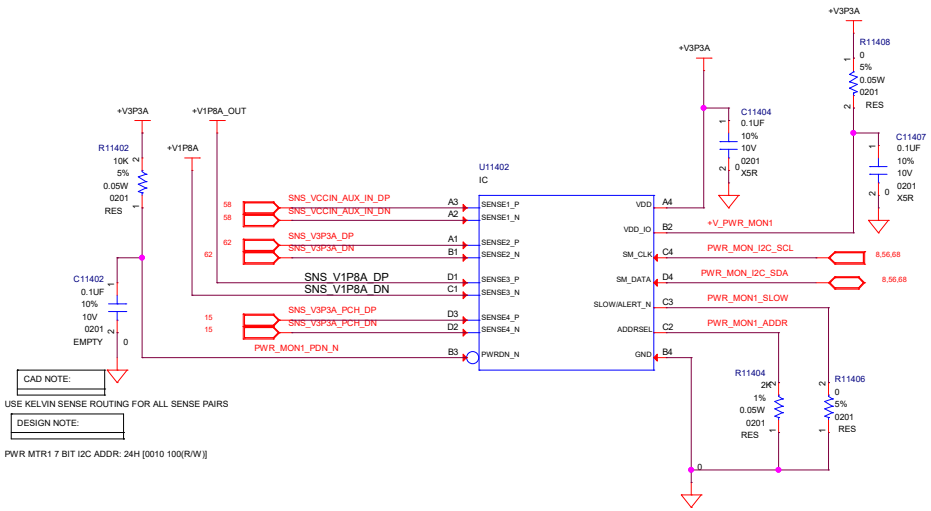
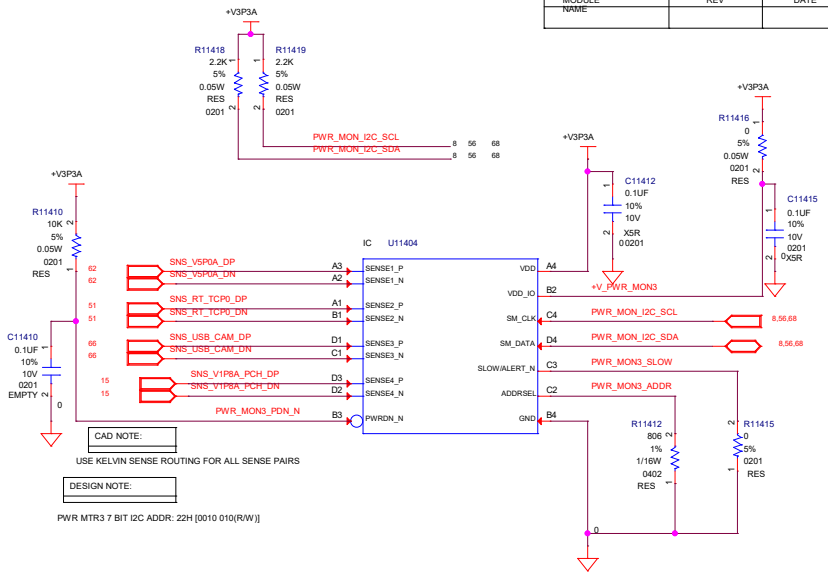
	<DOCUMENT_NUMBER>	67	1P0

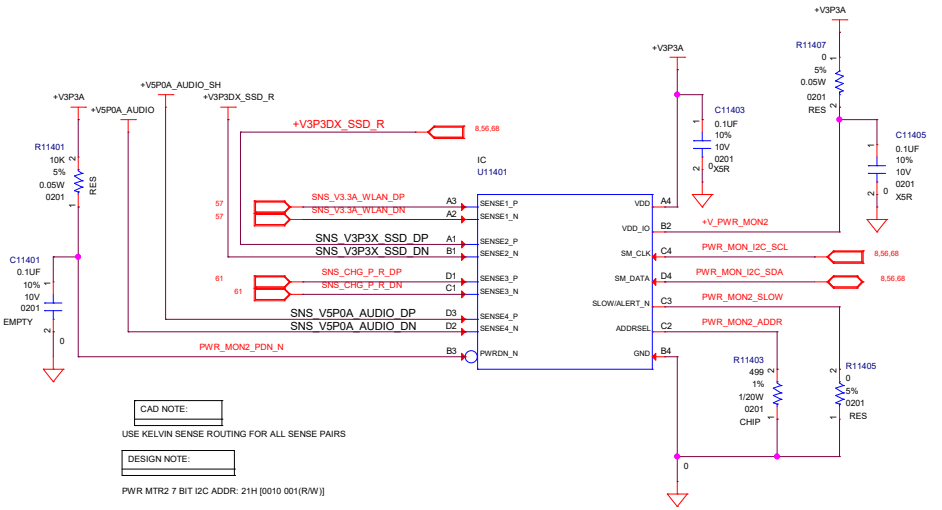
CUSTOM TEXT BPAGE

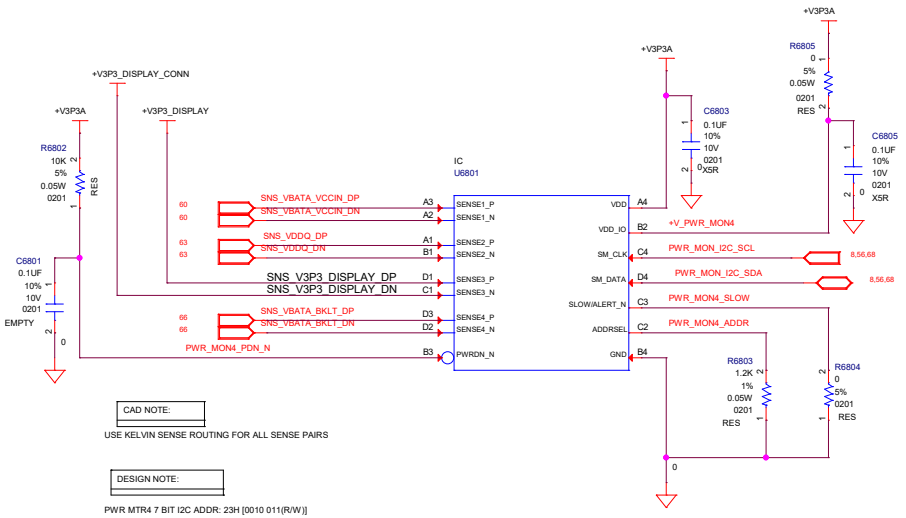
POWER METER

MODULE REV DETAILS		
MODULE NAME	REV	DATE









BPAGE DRAWING

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Fri Feb 28 13:41:09 2020

Note : "This circuit page only for Validation purpose- Can be removed or unstuff for mass production"

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	<DOCUMENT_NUMBER>	68	1P0

CUSTOM TEXT BPAGE

DEBUG SECTION

MOUNTING HOLES

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE : PLACE RA AND RB CLOSE TO THE SOC BRANCH WITHOUT STUB LENGTH

BPAGE DRAWING

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	<DOCUMENT_NUMBER>	69	1P0

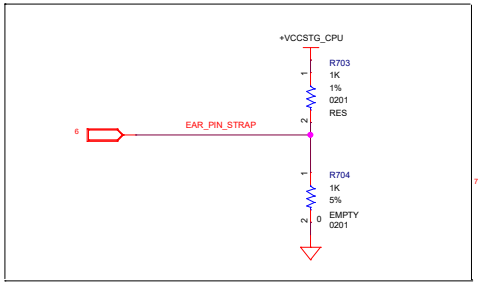
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE

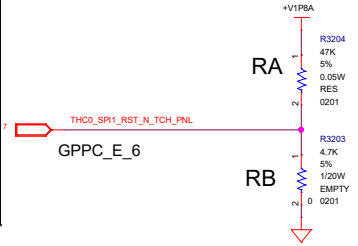
CPU STRAPS

DESIGN NOTE:

THE CFG SIGNALS HAVE A DEFAULT VALUE OF '1' IF NOT TERMINATED ON THE BOARD.



CUSTOMER INVISIBLE RESERVED STRAPS



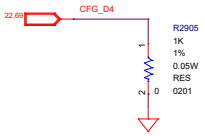
JTAG ODT DISABLE

LOW: JTAG ODT DISABLED
HIGH: JTAG ODT ENABLED

NO INTERNAL PU/PD

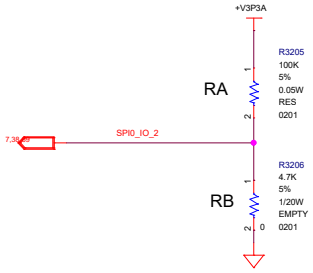
DISPLAY PORT PRESENCE STRAP

CFG4	0:ENABLED EXTERNAL DISPLAY DEVICE CONNECTED TO EMBEDDED DISPLAY PORT 1:DISABLED; NO PHYSICAL DISPLAY PORT ATTACHED



CAD NOTE:

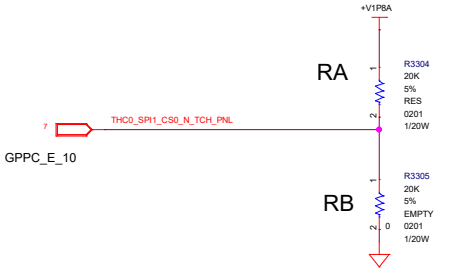
PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



CONSENT STRAP

HIGH: DISABLED
LOW: ENABLED

NO INTERNAL PU/PD



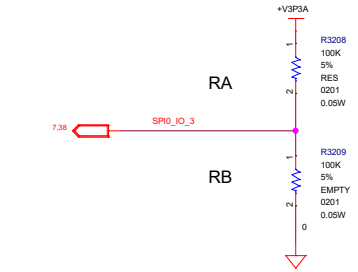
XTAL INPUT FREQUENCY [0]
(HVM ONLY)
00:24MHZ
01:25MHZ
10:250MHZ
11:100MHZ

(QUALIFIED BY DFXTESTMODE)

NO INTERNAL PU/PD

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



FOR UNFUSED A0 SILICON STUFF PD

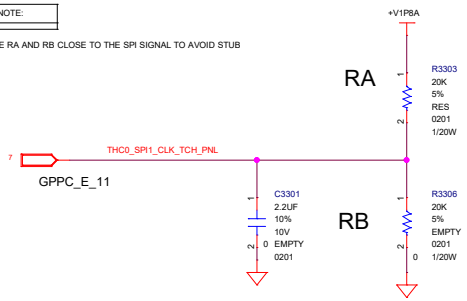
A0 PERSONALITY STRAP

HIGH: DISABLED
LOW: ENABLED

NO INTERNAL PU/PD

CAD NOTE:

PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



XTAL INPUT FREQUENCY [1]
(HVM ONLY)
00:24MHZ
01:25MHZ
10:250MHZ
11:100MHZ

(QUALIFIED BY DFXTESTMODE)

NO INTERNAL PU/PD

BPAGE DRAWING

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CUSTOM TEXT BPAGE