Figure 248. Timing Diagram for G3 to S0 [Deep Sx Platform] - 1 OF 2

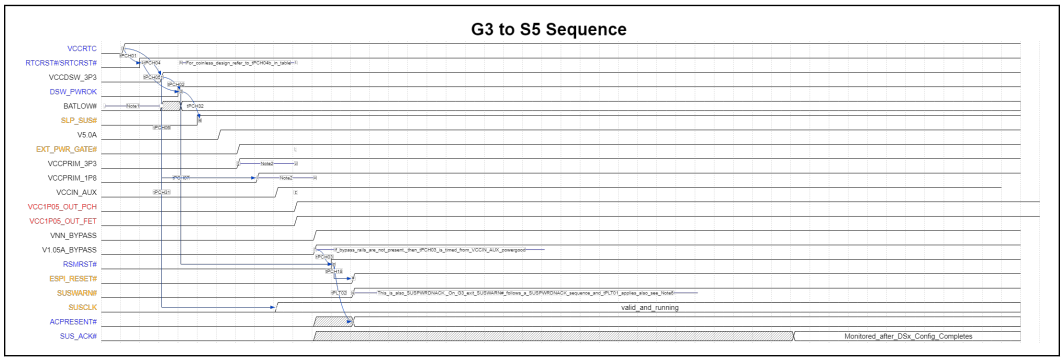
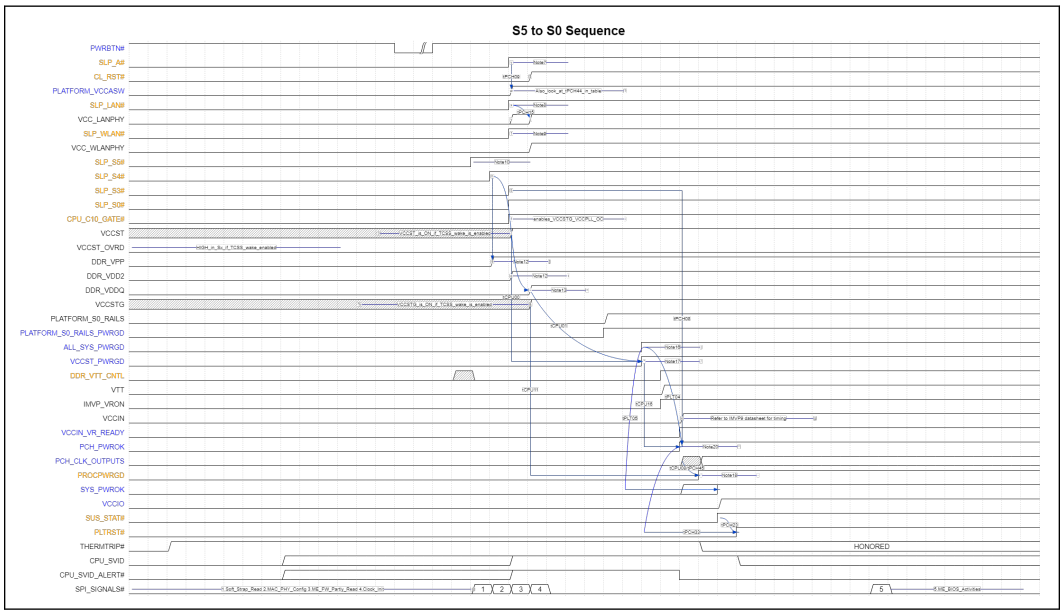


Figure 249. Timing Diagram for G3 to S0 [Deep Sx Platform] - 2 OF 2



NOTE

General Note: Some of legacy signals shown in these diagrams are not available as hard signals when eSPI is used.

1. PCH will sample BATLOW# on the rising edge of DSW_PWROK for DSx Systems
2. Refer Rail-to-Rail Power Sequencing Requirement section on PCH prime rail-to-rail power and power down dependencies
3. NA
4. NA
5. For a DSx system, PCH will ignore SUSACK# until after SUSWARN# is valid.
6. EC must ignore SUSWARN pin even in DSx system on G3 exit.
7. SLP_A# always goes high with or before SLP_S3#. Depending on PCH settings SLP_A# may go high, then low, then high again all before SLP_S3#, but will go high no later than SLP_S3# on an Sx to S0 transition, or the Sx to S0 portion of G3 exit, Global Reset, and Deep Sx exit.

   In the event of a global reset after SLP_A# is de-asserted, during the power up sequence, SLP_A# will assert and the controller monitoring the sleep signals should reset its timeouts.
8. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#.
9. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
10. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
11. VCCST, and VCCSTG can remain powered during S4 and S5 pwr states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer Platform Debug and Test Hooks chapter for more details. VCCSTG should only ramp up equal to or after VCCST.
12. Required with LPDDR4x, LPDDR4 and DDR4 memory configurations. For LP4/4x VPP, VDD2 and VDDQ timings, please refer to JEDEC Specification. There is no VTT for LP4/4x. It is applicable only for DDR4 memory based designs
13. VDDQ must ramp after VPP on DDR4 and LPDDR4 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
14. NA
15. NA
16. ALL_SYS_PWRGD is assumed to logically AND together the PWRGD signals for the major system power rails
17. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time
18. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.
19. NA

20. The Platform should ensure that PCH_PWROK does not glitch when RSMRST# is de-asserted

Figure 250. Timing Diagram for S0-S0ix-S0

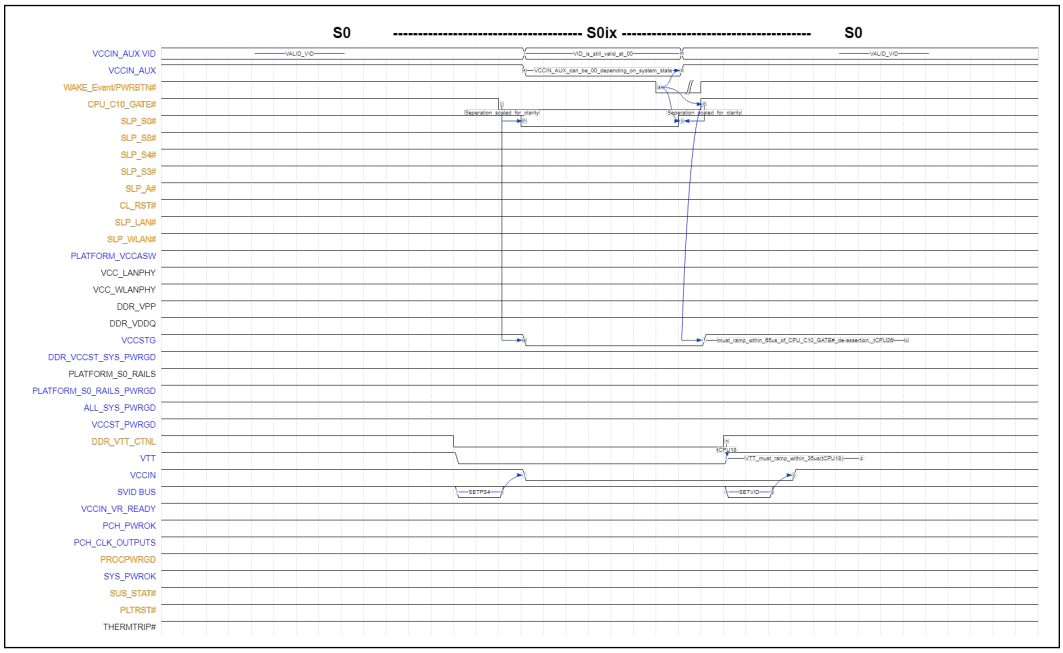
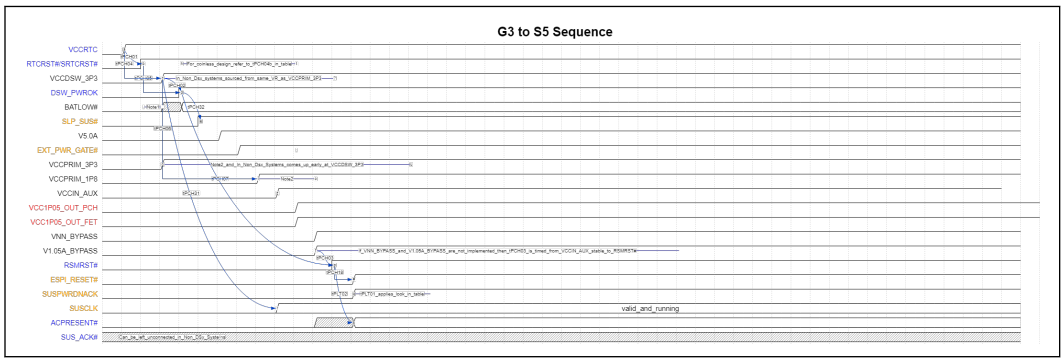


Figure 251. Timing Diagram for G3 to S0[Non-Deep Sx Platform]



S5 to S0 sequence is same as DSx Sequence (refer to DSx S5-S0 sequence diagram).

NOTES

1. PCH will sample BATLOW# on the rising edge of DSW_PWROK for DSx Systems
2. Refer Rail-to-Rail Power Sequencing Requirement section for details on PCH prime rail-to-rail power and power down dependencies.

Additional Notes:

Some of legacy signals shown in these diagrams, like SUSPWRDNACK, are not available as hard signals when eSPI is used, they are Virtual Wires.

The state of the SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.

- SUSPWRDNACK
  - — *Platform not supporting M3* - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted. Else, EC has an option to do whatever it wants with the SUS Rails
  - — *Platform supporting M3* - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** SLP_A# is de-asserted **OR** it is the first 200mS after SUS Rails power has been applied. Else, EC has an option to do whatever it wants with the SUS Rails
- Primary rails and Deep Sx Rails should **never** be active while VccRTC rail is inactive.

Figure 252. Timing Diagram for S0/M0 to G3 [Deep Sx Platform]

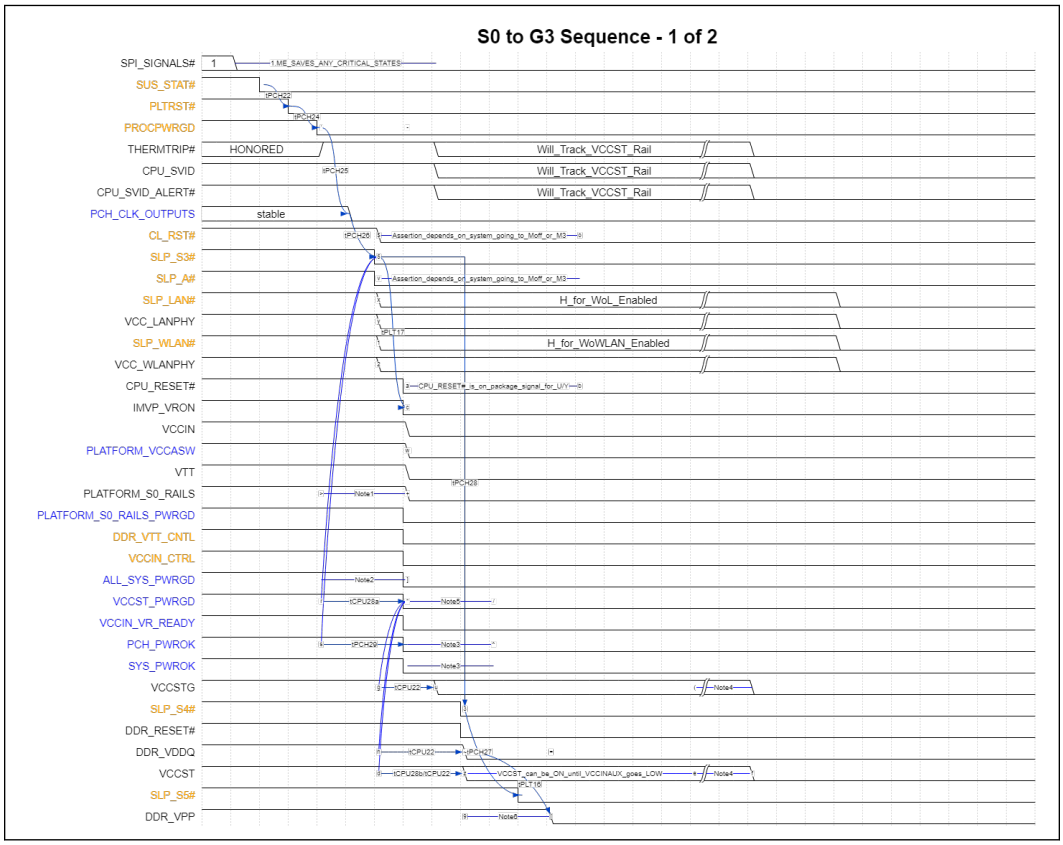


Figure 253. Timing Diagram for S0/M0 to G3 [Deep Sx Platform]

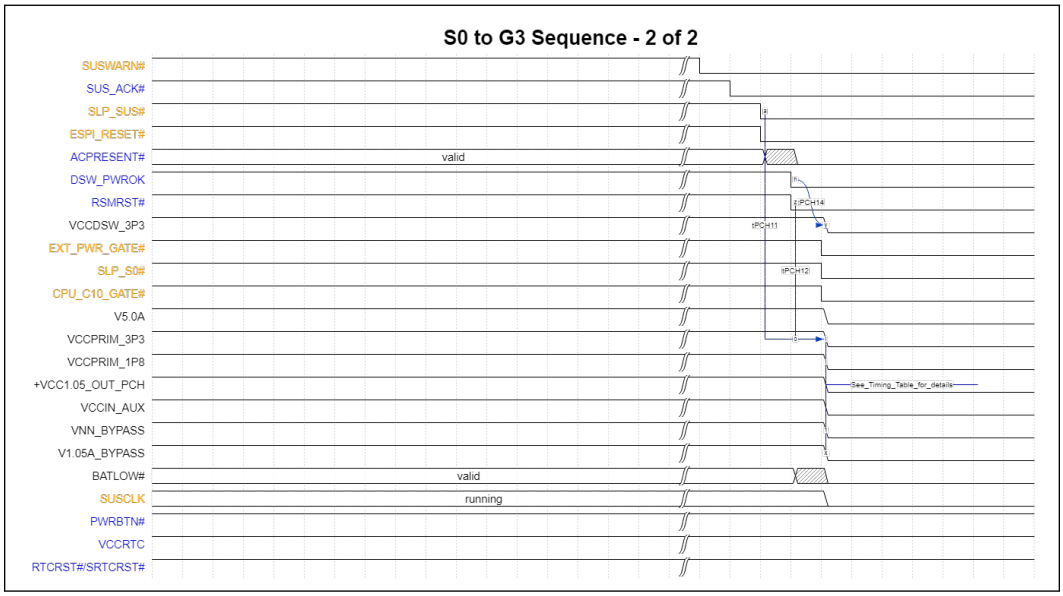


Figure 254. Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]

For S0 to G3 Sequence 1 of 2 Refer to DSx Sequence

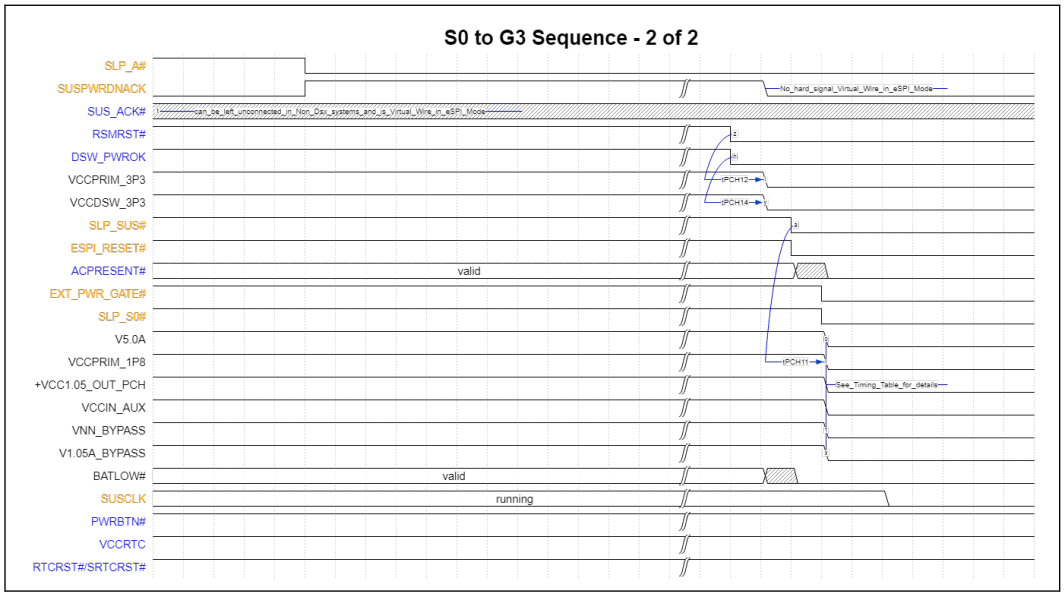
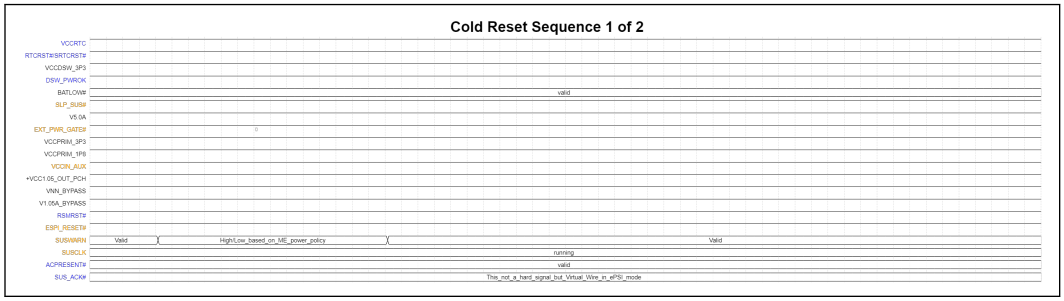
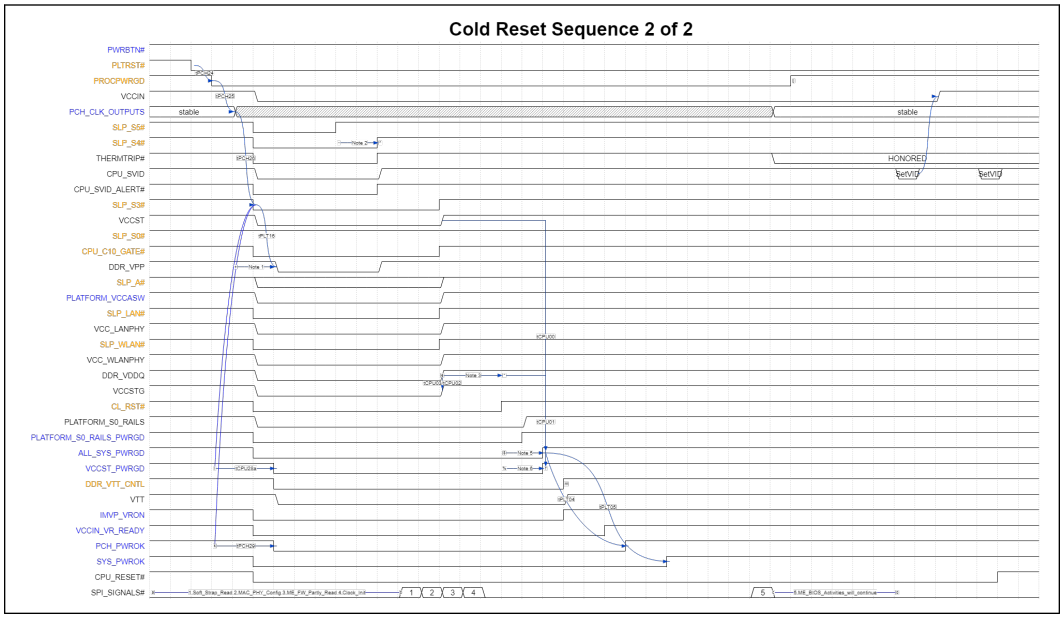


Figure 255. Timing Diagram for Cold Reset [Deep Sx Platform]





NOTES

1. Must ramp down AFTER VDDQ has ramped down
2. If the system EC is driving these signals in ESPI mode, based on the state of eSPI SLP Virtual Wires, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
3. VDDQ must ramp after VPP on DDR4 and LPDDR4 based systems, thus VDDQ may end up after SLP_S3# de-assertion due to VR ramp timing and configuration
4. NA
5. ALL_SYS_PWRGD is assumed to logically AND together the PWRGD signals for the major system power rails
6. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time IMVP VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.

Figure 256. Timing Diagram for Warm Reset [Deep Sx Platform]

Power Sequencing Timing Requirements

The following table defines the timing parameters used in the timing diagrams in previous sections. The timing parameters are put into three categories: tCPU, tPCH, and tPLT. tCPU parameters are mostly required by the processor, tPCH parameters are required or controlled by the PCH, and tPLT parameters are mostly controlled by the platform.

The timing parameters are defined by Min, Max and Typical specifications. The Min and Max timings refer to the minimum or maximum timings allowed between the first and second signals in the Description column, as are the timing boundaries that must be followed. The Typical column refer to the typical timing values measured on Intel boards during validation, which do not imply a requirement but can be used as a reference.

Table 231. Platform Sequencing Timing Parameters

if this condition is met, it will happen after vccst is ramped for sure, and it demands 3 ms delay.

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tCPU00	All	CPU	PLT ✓	2 VCCST_CPU_OK < vccin_en < vccin_ready < vccst_ok < delayed_vccin_ok < vccst_pwrgd			ms	6, 7	VCCST, VCCSTG ramped and stable to VccST_PWRGD assertion
tCPU01	All	CPU	PLT ✓	1			ms	6, 7	VDDQ ramped and stable to VccST_PWRGD assertion
tCPU02	All	CPU	PLT		No Limit		ms	43	VCCST, VCCSTG ramped and stable before VDDQ stable *Note:* tCPU02 and tCPU03 are mutually exclusive, and only one of the parameters needs to be met depending on the rail order of VCCST/VCCSTG and VDDQ

-- slp_s4n < vpp_en < vpp_pwrgd < vddq_en < vddq_pwrgd

VCCST_CPU_OK AND SLP_S3# < vccin_en < vccin_ready < vccin_ok < delayed_vccin_ok < vccst_pwrgd

43. tCPU02 and tCPU03 are mutually exclusive, only tCPU02 or tCPU03 needs to be met

continued...

6. VCCST_PWRGD has no edge rate requirement, but edges must be monotonic.
7. VCCST_PWRGD must accurately reflect the state of VCCST and must not glitch when VCCST, VCCSTG or VDDQ power is applied. Additionally, VCCST_PWRGD must track to the state of PCH_PWROK on the platform. When PCH_PWROK de-asserts during S0 --> Sx transitions, then VCCST_PWRGD must also de-assert.

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tCPU03	All	CPU	PLT		No Limit		ms	43	VDDQ ramped and stable before VCCST, VCCSTG stable *Note:* tCPU02 and tCPU03 are mutually exclusive, and only one of the parameters needs to be met depending on the rail order of VCCST/VCCSTG and VDDQ
tCPU04	All	CPU	PLT	0			ns	31	VCCST must always ramp with or earlier then VCCSTG. VCCST >= VCCSTG at all times during ramp.
tCPU08	All	CPU	PCH	1			ms	8	PCH CLK outputs stable and CPU VRs stable/ready to PROCPWRGD assertion
tCPU16	All	CPU	PLT	0			ns	32	VCCST_PWRGD assertion to PCH_PWROK assertion
tCPU18	All	CPU	PLT	0	35		us	34	DDR_VTT_CNTL (was DDR_PG_CTL) assertion to DDR VTT supplied ramped and stable while PLTRST = H (de-asserted).

34. Only applies to configurations that use DDR_VTT_VCTRL signal to enable/disable VTT VR and only applies after PLTRST# has de-asserted (ie, S0). VTT must be completely ramped and ready for full load at or before the de-assertion of PLTRST# on Sx -> S0 transitions.

tCPU19	All		CPU	0	100		ns	9	VccST_PWRGD assertion to DDR_VTT_CNTL (was DDR_PG_CTL) asserted.
tCPU20		**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 ºC. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	PLT + PCH	not implemented	500		ms		THERMTRIP# assertion until VCCIN VR is disabled and not sourcing power
tCPU21	All	CPU	PCH		1		ms		THERMTRIP# assertion until PCH issues global reset and assertion of SLP_SX signals
tCPU22	All	CPU	PLT	1			us	36, 37	VCCST_PWRGD de-assertion to either VDDQ, VCCST, VCCSTG below specification for normal S0 to Sx transitions. Recommend VCCST_PWRGD goes low with SLP_S3#
tCPU26	All			10	65		us		CPU_C10_GATE# de-assertion to VCCSTG, VCC1P8A stable, the rail must meet this max ramp time.
tCPU29	All	CPU	PLT		100		mV/us	13	Processor power rail instantaneous slew rate.
tPCH01	All	PCH	PLT	9			ms	1, 46, 47	VccRTC = 2.0V to the point in time where voltage on the RTC resets equals 0.65 times the voltage present on the VccRTC rail during ramp. This measurement should be made from VccRTC = 2.0V to the first of RTCRST# or SRTCRST# reaching 0.65 * VccRTC .
tPCH02a	All	PCH	PLT	10	2000		ms		VccDSW stable (@95% of full value) to DSW_PWROK high. **Applies to Systems that do not implement G3 Flash sharing**
tPCH02b	All	PCH	PLT	10	See Note		ms	48	VccDSW stable (@95% of full value) to DSW_PWROK high. **Only applies to Systems that implement G3 Flash sharing**
tPCH03a	All	PCH	PLT	10	2000		ms		VccPrimary stable (@95% of full value) to RSMRST# high **Applies to Systems that do not implement G3 Flash sharing**
tPCH03b	All	PCH	PLT	10	See Note		ms	49	VccPrimary stable (@95% of full value) to RSMRST# high **Only applies to Systems that implement G3 Flash sharing**
tPCH04a	All		PCH	9			ms	29, 42	VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with **coined RTC battery**

vddq_en <= '1' WHEN (slp_s4n= '1') AND (vpp_pwrgd = '1')

48. Total exposure to DSW above > 200mV with DSW_PWROK low must not exceed 6 days of the life of the PCH. Failure to meet this requirement over the life of the system could result in reduce component reliability and lifetime.

42. For the dead RTC coin cell and coin cell-less with depleted main battery RTC cases where the 3.3DSW ramps and powers the RTC well, the board designer should set the 3.3DSW rail stable to DSW_PWROK assertion delay (tPCH02) for = 30ms. This is required to ensure that SRTCRST# and RTCRST# de-assert after VCCRTC is stable, but before DSW_PWROK assertion. Failure to meet this requirement may result in DSW_PWROK asserting with, or before, SRTCRST# and RTCRST# reach VIH, which is a sequencing violation and can result in a non-booting system scenario. Refer Real Time Clock (RTC) Design Guidelines on page 123 and RTC External RTCRST# Circuit on page 126 and RTC External SRTCRST# Circuit on page 127 for SRTCRST# and RTCRST# RC timing network details.

continued...

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tPCH04b	All		PCH	30			ms	29, 42	VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with **coinless RTC**. Please refer to IBP#549657 for Design considerations technical advisory document without RTC battery. Earlier this timing was referred as tPCH48.
tPCH05	All	PCH	PLT	1			us	42	RTCRST# high (voltage above ViH_min) to DSW_PWROK high (when voltage crosses ViL_max such that internally it might be resolved as a logic '1')
tPCH06	All	PCH	PLT	200			us		VccDSW 3.3 stable (@95% of full value) to VccPrimary 1.8V starting to ramp (for DSx or nonDSx configurations
tPCH07				0			ms		DSW_PWROK high to RSMRST# high
tPCH08	All	PCH	PLT	1			ms		SLP_S3# de-assertion to PCH_PWROK assertion
tPCH09	All	PCH	PLT	2, 4, 8, 16			ms		SLP_A# high to PCH assuming ASW rails are stable (95% of full value)
tPCH11	All	PCH	PLT	100			ns		SLP_SUS# asserting to VccPRIM dropping 5% of nominal value
tPCH12	All	PCH	PLT	400			ns	5, 24	RSMRST# asserting to VccPRIM dropping 5% of nominal value
tPCH13	All	PCH		0			ms	14	RTCRST# asserting to VccRTC dropping 5% of nominal value (this applies only when RTC battery is removed)
tPCH14	All	PCH	PLT	400			ns	4, 5	DSW_PWROK falling to any of VccDSW, VccPrimary dropping 5% of nominal value
tPCH15	All	PCH	PLT		100		ms		SLP_LAN# (or LANPHYPC) rising to VccLANPHY high and stable
tPCH18	All		PCH	90			us		De-assertion of RSMRST# to De-assertion of eSPI_RESET# on exit from G3 (DSx platforms only), or exit from DSx
	All		PCH	90			us		De-assertion of RSMRST# to De-assertion of eSPI_RESET# on exit from G3 (Non-DSx platforms only)
tPCH20	All	PLT	PCH	-100			ns		DDR_RESET# assertion to SLP_S4# assertion (The negative minimum timing implies that DDR_RESET# must either fall before SLP_S4# or within 100 nS after it).
tPCH21	All		PCH	Refer note 38			ms	38	Warm Reset PLTRST# assertion duration time
tPCH22	All		PCH	210			us		SUS_STAT# active to PLTRST# active. *Note:* Not applicable for eSPI systems.
tPCH23	All		PCH	60			us		SUS_STAT# de-assertion to PLTRST# de-assertion. *Note:* Not applicable for eSPI systems.
tPCH24	All		PCH	30			us		PLTRST# assertion to PROCPWRGD de-assertion

continued...

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tPCH25	All		PCH	10			us		PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF. This timing is programmable (Range = 10us, 100us, 1ms, 10ms). Default is set to 10 us.
tPCH26	All		PCH	1			us		CLKOUT_BCLK turning OFF to SLP_S3# assertion
tPCH27	All		PCH	30			us	33	SLP_S4# assertion to SLP_S5# assertion
tPCH28	All		PCH	30			us	33	SLP_S3# assertion to SLP_S4# assertion
tPCH29	All		PCH	0			ms		SLP_S3# assertion to PCH_PWROK deassertion
tPCH31	All		PCH		tPCH02 + tPCH32		ms	15, 44	VccDSW3p3 ramped and stable until SUSCLK is stable. SUSCLK will start before the max timing, but will not be guaranteed valid until max timing is met
tPCH32	All		PCH	95			ms		DSW_PWROK assertion to SLP_SUS# de-assertion
tPCH33	All		PCH	0, 99			ms	16	PCH_PWROK high to PLTRST# de-assertion. This timing is set by the PCH via Soft strap settings
tPCH34	All	PCH	PLT		50		ms		Time from start of ramp of the first prim rail after SLP_SUS# de-assertion to completion of primary and bypass rail ramp.
tPCH35	All	PCH	PLT		See Note		ms	20, 49	SLP_SUS# low to PCH PRIMARY rails reaching 200mV or less.
tPCH36	All	PCH	PLT		100		mV/us		PCH Power rails instantaneous slew rate
tPCH41	All	PCH	PCH	1			ms		PCH_PWROK high to PCH clock outputs stable
tPCH43	All	PCH	PLT	95			ms	28	DSW_PWROK assertion to PWRBTN# monitored
tPCH44	All	PCH	PLT	500			us		tPCH09 expiring to CL_RST# high
tPCH45	All		PCH	1, 5, 50, 100			ms	39	Clock outputs stable to PROCPWRGD assertion to processor. Timing set by PCH via Soft Strap settings
tPCH46	All		PCH	1, 2, 5, 10			ms	39	PROCPWRGD and SYS_PWROK High to SUS_STAT# de-assertion. This timing is not applicable for eSPI systems. *Note:* Timing can be adjusted through the FIT tool
tPCH47	UP4		PCH	10.5	200		us	21, 51	De-assertion of EXT_PWR_GATE# until gated VCCMPHYGT_1P05 supply stable (@ 95% of full value)
tPCH48	UP4		PCH	10.5	200		us	50, 51	De-assertion of EXT_PWR_GATE2# until gated VCCPRIM_GATED_1P05 supply stable (@ 95% of full value)
tPCH49	UP4		PCH	6			mV/us	21, 50	MPHYGT_1P05/PRIM_GATED_1P05 Supply instantaneous slew rate
tPLT01	All		PCH	200			ms	2	RSMRST# de-assertion to SUSPWRDNACK valid. Timing set by PCH.
tPLT02	All			0	90		ms		RSMRST# de-assertion to ACPRESENT valid (not floating). *Note:* This is only for platforms not supporting Deep Sx state

continued...

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
	All				0		ms		RSMRST# de-assertion to ACPRESENT valid (not floating) [For platforms supporting Deep Sx state]. *Note:* ACPRESENT is a powered input to the PCH while in the Deep Sx state (that is, when DSW_PWROK=1 and RSMRST#=0). The PCH implements a weak pull-down on ACPRESENT while RSMRST#=0 such that the input is observed as 0 if not driven actively by the board during this time. If driven actively by the board to 1 while in Deep Sx and if the PCH is enabled to treat the ACPRESENT indication as a wake event from Deep Sx, then the PCH will power up the Primary well.
tPLT04	All	CPU/PCH	PLT	1			ms	3, 19	ALL_SYS_PWRGD assertion to PCH_PWROK. This timing must be controlled on the platform.
tPLT05	All		PLT	Platform dependent	No limit			18	ALL_SYS_PWRGD assertion to SYS_PWROK. This timing must be controlled on the platform. SYS_PWROK provides a platform/EC mechanism to stall the PCH de-assertion of PLTRST# to the platform. Different platform components may have difference timing requirements from when their power rails are stable until their respective reset signal can de-assert. Platform designer should adjust this timing based on their specific platform requirements.
tPLT14	All		PCH	4			s		Power cycle duration time; programmable via PM_CFG.PWR_CYC_DUR bit.
tPLT15	All	PLT (MEM)	PLT		200		us	40	SLP_S4# assertion to VDDQ VR Enable Low [VDDQ VR disabled]. Memory dependent, refer JEDEC requirements
tPLT16	All	PLT (MEM)	PLT	30			ms	30	VDDQ ramp down to start of VPP ramp down when entering S4 and lower. This is not a Processor requirement but a recommended timing to help meet the JEDEC sequencing requirements. Platform designers are responsible for making sure their designs meet the power sequencing requirements for the memory technology used in their designs.
tPLT20	All	PLT (MEM)	PLT	2.5			ms	30	VPP ramped to VDDQ start of ramp when entering S0 at power up. This is not a Processor requirement but a recommended timing to help meet the JEDEC sequencing requirements. Platform designers are responsible for making sure their designs meet the power sequencing requirements for the memory technology used in their designs.

continued...

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description
tPLT17	All	CPU	PLT	0			us	35	IMVP VR ON low to VCCST below 95% of its value
tPLT19	All	PLT	PLT		10		us	22	RSMRST_PWRGD# or SLP_SUS# assertion to RSMRST# assertion

Notes:

1. PCH Primary Rails must never be active while VCCRTC is OFF
2. RSMRST# should be de-asserted for at least 200ms before PCH will consider SUSPWRDNACK valid.
3. PCH can delay de-assertion of PLTRST# with a soft strap setting. Refer tPCH45 (t573) and tPCH46 (t1001) and the SPI Programming Guide for more details.
4. For catastrophic/surprise power failures only.
5. For surprise power down cases, if DSW_PWROK is de-asserted (tPCH16) before DSW3.3 **and** any other Prim rails droop out of spec, there is no risk of RTC corruption (assuming VCCRTC was previously powered and VCCRTC# is de-asserted) and this spec can be ignored
6. VCCST_PWRGD has no edge rate requirement, but edges must be monotonic.
7. VCCST_PWRGD must accurately reflect the state of VCCST and must not glitch when VCCST, VCCSTG or VDDQ power is applied. Additionally, VCCST_PWRGD must track to the state of PCH_PWROK on the platform. When PCH_PWROK de-asserts during S0 --> Sx transitions, then VCCST_PWRGD must also de-assert.
8. Processor's PROCPWRGD is not expected to be used externally on the platform, but is available for monitoring.
9. DDR_VTT_CTL will start to go high on VDD2 ramp with VCCT_PWRGD low for Sx to S0 power state transitions.
10. It is strongly recommended that the SLP_ S3# be a qualifying input signal to ALL_SYS_PWRGD logic, which drives IMVP VR_ON inputs. Additionally, it is recommended that SLP_S3# also qualify the EN control to the VCCIO power supply
11. Max timing is only applicable during S0i3 exit if the voltage rail is actively power gated. Not applicable during Sx-S0 transition
12. NA
13. Applies to all CPU power supply rails
14. There are no perceived functional failures if this minimum is violated since all data is lost anyway when VccRTC drops. The only real requirement is to avoid driving a high signal level into the powered down device for an extended period of time, assuming an external device(s) on a different power supply then VCCRTC is driving RTCRST# or any other RTC well input signal.
15. SUSCLK is now powered in DSW well.
16. PCH can delay de-assertion of PLTRST# with a soft strap setting. If tPCH33 is not enabled, the platform is responsible for controlling the assertion timing of PCH_PWROK and SYS_PWROK in such a way that it satisfies platform component timing requirements of power stable to reset de-assertion. Refer SPI Programming Guide for more details. On a platform level this timing doesn't necessarily need to meet 99ms, PCH soft straps guarantees a min of 99ms.
17. NA
18. Example, if the platform only has mini-PCIe* devices requiring a 1 ms delay from power rails stable to PCIe* reset de-assertion, then the minimum value for ALL_SYS_PWRGD assertion to SYS_PWROK can be reduced to 1 ms. If SYS_PWROK asserts before PCH_PWROK, no additional delay will be added by the PCH to delay PLTRST# de-assertion and the final timing value will be subject to internal PCH timing parameters.
19. PCH_PWROK assertion assumes CPU and PCH voltage rails are ramped and stable.
20. No Ramp down requirement between rails. All VRs should stop regulation based on SLP_SUS# signal, or another common shutdown signal. Applies to all power down cases except PCH induced FIVR emergency shut down chase where SLP_SUS# goes low with to shut down PCH VRs.
21. Only applicable to platforms that implement external VCCMPHYGT_1P05 power gating. Does not apply to G3/DSx to Sx ramp up.
22. 10us max limit is an estimation and will vary based on platform VR and EC implementation details. Platform designers are responsible for ensuring that tPCH12 is not violated during normal DSx entries based on EC and VR response times to assertion of SLP_SUS# and/or RSMRST_PWRGD#
23. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD. Therefore, the platform is only responsible to have these rails ready a minimum of 0ms before PCH_PWROK assertion.
24. Applicable to all power down sequences where Prime well rails are turned off and to emergency power loss scenario. Refer RSMRST#/DSW_PWROK Special Requirements section.
25. NA
26. NA
27. If VCCSTG and VCCIO supplies are merged together as a single supply, then the timing requirement is between VCCST/VCCSTG/VCCIO and VCCSA
28. Applicable to all G3 exits where GEN_PMCON_B.AG3E=1. The PWRBTN# must assert for at least 16ms after the minimum tPCH43 timing before PCH will detect PWRBTN# as a wake event
29. For scenarios where the coin-cell is dead or missing, the PCH can electrically tolerate the VCCRTC and VCCDSW/VCCPRIM 3.3V supplies ramping simultaneously with VCCDSW/VCCPRIM 3.3V leading VCCRTC by ~0.2 – 0.3V (ie. voltage drop associated with the coin cell Schottky diode circuit). These scenarios are not allowed as typical power sequencing scenarios, and are expected to be very infrequent. In these scenarios, glitch-free signal operation on DSW signals can not be guaranteed when the platform is configured for DSx mode. Likewise, glitch-free signal operation on DSW and PRIM well signals can not be guaranteed when the platform is configured for non-DSx mode
30. Generally, JEDEC specifications require VPP >= VDDQ for both power up and power down sequences. This timing parameter is a suggested value as ensure this requirement is met on power down, but systems designer must account for other platform level considerations such as output decoupling, discharge circuits, etc that can alter this relationship.
31. VCCST supply is typically controlled by SLP_S3# only, and VCCSTG supply is typically controlled by SLP_S0# AND SLP_S3#. Since the timing delay between SLP_S3# and SLP_S4# deassertion during a S4/S5 à S0 transition can be small (defined by tPCH28) , OEMs may need to take extra steps to ensure this timing is met. Example, power gates of equivalent slew rate may be required on both VCCST and VCCSTG supplies. Alternatively, a small timing delay path might be required on the SLP_S3# path of the VCCSTG power gate enable
32. VCCST_PWRGD should start to assert no later than when PCH_PWROK asserts; however, VCCST_PWRGD may lag completing its ramp with respect to PCH_PWROK by up to 20us
33. Not applicable to eSPI mode, refer to the eSPI Compatibility Specification (#508740) for eSPI implementations
34. Only applies to configurations that use DDR_VTT_VCTRL signal to enable/disable VTT VR and only applies after PLTRST# has de-asserted (ie, S0). VTT must be completely ramped and ready for full load at or before the de-assertion of PLTRST# on Sx -> S0 transitions.
35. Timing to VR being disabled, not until the VR is fully ramped down
36. S0 to Sx transition with VCCST powered in Sx state. In TGL platforms ST control changes to SLP_S3# OR VCCST_OVERRIDE .
37. S0 to Sx transition with VCCST unpowered in Sx
38. Recommend not to exceed 10ms delay with respect to SLP_S3#
39. During a warm reset sequence, the PCH sequencing flows will internally re-execute several timing parameters and tpch45 and tpch46 are two of the parameters that are re-executed. tPCH45 and tPCH46 are primarily for G3/DSx/Sx à S0 flows, but they are executed for cold boot, cold reset, and warm reset. The nominal setting for these timings is partially controlled by the setting of SPI soft straps associated with tPCH45 and tPCH46. The

Label	Applicable SKU	Required By	Controlled By	Min.	Max.	Typical	Units	Note #	Description

minimum possible PLTRST# assertion time will be equal to the soft strap settings for tPCH45 + tPCH46. The maximum PLTRST# assertion time is not guaranteed across all warm reset cycles, but the typical worst case assertion time is approximately equal to (tPCH45 soft strap setting) + (tPCH46 soft strap setting) + 20ms.

40. This is a platform timing recommendation to help ensure that memory device power down sequencing requirements between VDDQ and VPP are likely to be met (refer tPLT16). This is not a requirement for the TGL Processor itself. Refer to the JEDEC LPDDR4 and DDR4 power down sequencing requirements for more details
41. This parameter is programmable, refer to the Flash Descriptor Record in the SPI Programming Guide in the ME firmware package
42. For the dead RTC coin cell and coin cell-less with depleted main battery RTC cases where the 3.3DSW ramps and powers the RTC well, the board designer should set the 3.3DSW rail stable to DSW_PWROK assertion delay (tPCH02) for = 30ms. This is required to ensure that SRTCRST# and RTCRST# de-assert after VCCRTC is stable, but before DSW_PWROK assertion. Failure to meet this requirement may result in DSW_PWROK asserting with, or before, SRTCRST# and RTCRST# reach VIH, which is a sequencing violation and can result in a non-booting system scenario. Refer Real Time Clock (RTC) Design Guidelines on page 123 and RTC External RTCRST# Circuit on page 126 and RTC External SRTCRST# Circuit on page 127 for SRTCRST# and RTCRST# RC timing network details
43. tCPU02 and tCPU03 are mutually exclusive, only tCPU02 or tCPU03 needs to be met
44. SUSCLK stable means the clock is toggling and is within it is defined parameters. This timing spec is applicable to all G3 exits, excluding the G3 exit immediately following the ramp of VCCRTC, which may have a longer delay
45. Refer tPCH43 for- DSW_PWROK assertion to PWRBTN# monitored timing aspect.
46. C3 and C4 Capacitors used in the RTC external circuit should be evaluated with regards to aging, voltage and temperature characteristics to ensure reliable operation in the intended operating environment. See section 6.2.3 RTC External RTCRST# Capacitors.
47. For measurement details, reference RTC Reset Timing Technical Advisory - Document #610459.
48. Total exposure to DSW above > 200mV, with DSW_PWROK low must not exceed 6 days of the life of the PCH. Failure to meet this requirement over the life of the system could result in reduce component reliability and lifetime.
49. Total exposure to any of the PRIMARY rails > 200mV, with RSMRST# low must not exceed 6 days of the life of the PCH. Failure to meet this requirement over the life of the system could result in reduce component reliability and lifetime.
50. Only applicable to platforms that implement external VCCPRIM_GATED_1P05 power gating. Does not apply to G3/DSx to Sx ramp up.
51. MPHYGT_1P05 and PRIM_GATED_1P05 gates are no longer mandatory to implement. However existing designs with gates can continue with them.

Additional Notes:

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- DDR_RESET# behavior does not directly track the state of VDDQ rail. For DDR_RESET# to assert properly on surprise power failure, the VDDQ VR pwrgood output should be an input into the logic generating PCH_PWROK

10.12.6 DSW and PRIMARY Power up / Power Down Special Requirements

The PCH has lifetime exposure limits for the DSW and PRIMARY rails as follows:

- **DSW rail and DSW_PWROK:** The PCH requires that the sum total time with the VCC_DSW > 200mV **AND** DSW_PWROK low, during rail start up and shutdown, must not exceed 6 days of the life of the PCH.
- **Primary Rails and RSMRST#:** The PCH requires that the sum total time with any of the PRIMARY rails > 200mV **AND** RSMRST low, during rail start up and shutdown, not exceed 6 days of the life of the PCH.

Total exposure time will vary by platform implementation. Platform designs that support G3 flash sharing where the PCH is powered with RSMRST# low for more than 2 seconds must pay particular attention to the above requirements. Failure to meet this requirement over the life of the system could result in reduce component reliability and lifetime.

The following example demonstrates how to calculate DSW and PRIMARY rails total exposure time with their respective power goods (DSW_PWROK and RSMRST#) low over the product lifetime.

Example System Assumptions

DSx enabled design where system goes to DSx on AC and G3 on battery, **with** G3 Flash sharing.

System Characteristics as Determined by OEM for Target System Usage