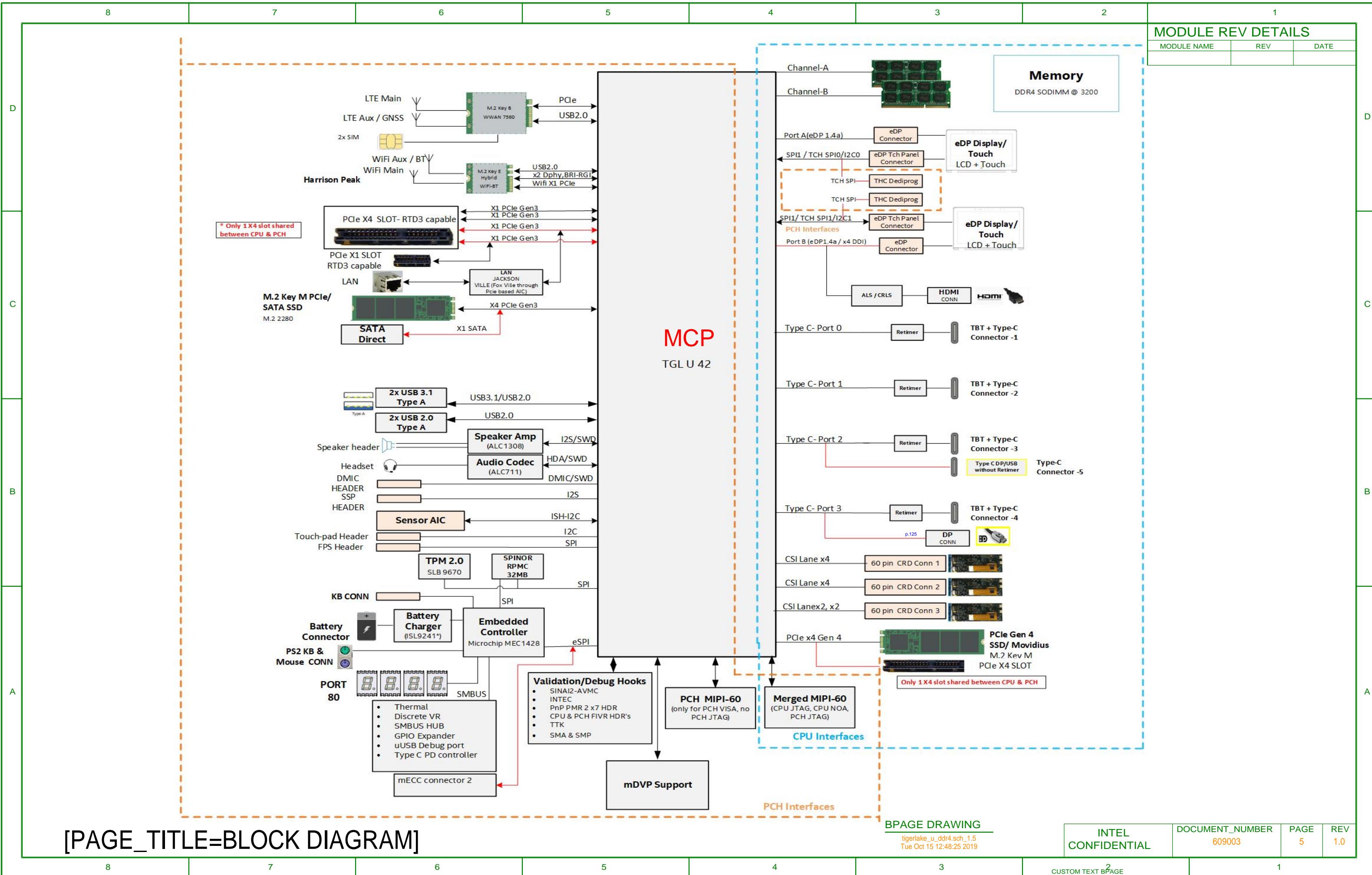


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D	[93. DISPLAY - eDP connector 2 - MISC] [94. DISPLAY - eDP connector 2] [95. DISPLAY - DP CONNECTOR 1 - CMC] [96. DISPLAY - DP CONNECTOR 1 - ESD] [97. DISPLAY - DP CONNECTOR 1 - HDMI INTEROPERABILITY] [98. DISPLAY - HDMI RETIMER] [99. DISPLAY - HDMIC CONNECTOR - ACTIVE LEVELSHIFTER] [100. DISPLAY - HDMIC CONNECTOR - CMC & ESD] [101. DISPLAY - DP CONNECTOR 2 CMC] [102. DISPLAY - DP CONNECTOR 2 - ESD] [103. DISPLAY - DP CONNECTOR 2 - HDMI INTEROPERABILITY] [104. DISPLAY - DP2 & HDMI STACK CONN] [105. NO PAGE TITLE FOUND!!!] [106. DISPLAY - TYPE-C CONNECTOR -1 - RE-TIMER] [107. DISPLAY - TYPE-C CONNECTOR -1 - RE-TIMER - POWER] [108. DISPLAY - TYPE-C CONNECTOR -1 - ESD] [109. DISPLAY - TYPE-C CONNECTOR -1] [110. DISPLAY - TYPE-C CONNECTOR -5 - CMC & ESD] [111. DISPLAY - TYPE-C CONNECTOR -2 - RE-TIMER] [112. DISPLAY - TYPE-C CONNECTOR -2 - RE-TIMER - POWER] [113. DISPLAY - TYPE-C CONNECTOR -2 - ESD] [114. DISPLAY - TYPE-C CONNECTOR -2] [115. DISPLAY - TYPE-C CONNECTOR -5] [116. DISPLAY - TYPE-C CONNECTOR -3 -RE-TIMER] [117. DISPLAY - TYPE-C CONNECTOR -3 -RE-TIMER - POWER] [118. DISPLAY - TYPE-C CONNECTOR -3 - ESD] [119. DISPLAY - TYPE-C CONNECTOR -3] [120. DISPLAY - TYPE-C CONNECTOR -4 - RE-TIMER] [121. DISPLAY - TYPE-C CONNECTOR -4 - CMC] [122. DISPLAY - TYPE-C CONNECTOR -4 - ESD] [123. DISPLAY - TYPE-C CONNECTOR -4] [124. DISPLAY - DP CONNECTOR 3 - CMC] [125. DISPLAY - DP CONNECTOR 3 - ESD] [126. DISPLAY - DP CONNECTOR 3 - HDMI INTEROPERABILITY] [127. DISPLAY - DP CONNECTOR 3] [128. TOUCH PANEL CONNECTOR 1] [129. TOUCH PANEL CONNECTOR 2] [130. TOUCH PAD CONNECTOR] [131. FPS CONNECTOR] [132. IMAGING - CRD CONNECTOR 1&2] [133. IMAGING - CRD CONNECTOR 3&4] [134. RESERVE PAGE - IMAGING - CRD CONNECTOR 5] [135. RESERVE] [136. RESERVE] [137. RESERVE] [138. RESERVE] [139. RESERVE] [140. STORAGE - SATA DEV SLEEP, LED] [PAGE_TITLE=INDEX -2]	[141. STORAGE - SATA DIRECT CONNECT] [142. STORAGE - M.2 KEY-M SSD] [143. CONNECTIVITY - GBIT LAN - JACKSONVILLE LAN PHY CHIP] [144. CONNECTIVITY - GBIT LAN CONNECTOR] [145. CONNECTIVITY - M.2 KEY-E WLAN/BT - RESERVE] [146. CONNECTIVITY - M.2 KEY-E WLAN/BT - LED'S, MISC] [147. CONNECTIVITY - M.2 KEY-E CONNECTOR - WLAN/BT] [148. CONNECTIVITY - M.2 KEY-B WWAN - USB CMC, MISC] [149. CONNECTIVITY - M.2 KEY-B WWAN - CONNECTOR] [150. CONNECTIVITY - M.2 KEY-B WWAN - SIM CONNECTOR] [151. SENSOR HEADER] [152. USB 3/2 TYPE-A CONNECTOR -1&2 STACKED POWER SWITCH] [153. USB 3/2 TYPE-A CONNECTOR -1&2 STACKED CMC, ESD] [154. USB 3/2 TYPE-A CONNECTOR -1&2 STACKED] [155. USB 2 TYPE-A CONNECTOR - 3&4 STACKED POWER SWITCH] [156. USB 2 TYPE-A CONNECTOR - 3&4 STACKED CMC, ESD] [157. USB 2 TYPE-A CONNECTOR - 3&4 STACKED] [158. RESERVE PAGE - USB 2 TYPE-A CONNECTOR - 5 POWER SWITCH] [159. SOUND WIRE OPTION FOR SPEAKER AMP] [160. ALC1308-CGT SECTION 1] [161. ALC1308-CGT SECTION 2] [162. AUDIO - PORT SHARING OPTIONS - HAD/I2S/SNDW - 1] [163. AUDIO - PORT SHARING OPTIONS - HAD/I2S/SNDW - 2] [164. AUDIO - PORT SHARING OPTIONS - DMIC] [165. AUDIO - AUDIO HEADER -1] [166. AUDIO - AUDIO HEADER -2] [167. AUDIO - AUDIO CODEC MISC] [168. AUDIO - AUDIO CODEC ALC700] [169. AUDIO - JACK CIRCUIT] [170. SPI - FLASH MUX CIRCUIT] [171. SPI - FLASH] [172. SPI - PROGRAMING SF600/TPM HEADER] [173. EC - MEC1418/28 (1 OF 2)] [174. EC - MEC1418/28 (2 OF 2)] [175. EC - GPIO SHARING OPTIONS] [176. EC - SPI FLASH SHARING & FLASH] [177. EC - SPI FLASH SF600 PROGRAMER] [178. EC - MECC AIC (1 OF 2)] [179. EC - MECC AIC (2 OF 2)] [180. EC - RESERVED -1] [181. EC - BOARD ID, FAB ID, IO EXPANDER] [182. EC - PS2 KEYBOARD & MOUSE] [183. EC - SCAN MATRIX KEY BOARD] [184. EC - SWITCHES] [185. EC - PORT 80 DISPLAY & HEADER] [186. EC - THERMISTERS] [187. EC - FAN HEADER] [188. EC - SAS HEADER] [189. EC - FRONT PANEL HEADER]	MODULE REV DETAILS					
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B								
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BPAGE DRAWING
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CUSTOM TEXT BPAGE



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RefDes	LED Description
DS4G1	V1P05_CTRL
DS4G2	VNN_CTRL
DS8H5	S3 STATE
DS8H3	S4 STATE
DS8H4	S5 STATE
DS8H2	DSW STATE
DS8H1	M0/M3 STATE
DS3H1	ME PWR Gate

RefDes	LED Description
DS8H6	CAPS LOCK
DS8H7	NUM LOCK
DS7G1	POWER BUTTON
DS7H1	BAT STATUS LED

RefDes	LED Description
DS8G6	SLP S0 LED
DS8G4	PWRGD
DS8G5	CATERR
DS6G1	C10 GATE
DS6G2	CS INDICATE

RefDes	LED Description
DS9B1	SATA Direct connect DEVSLP
DS9E1	M.2 SSD DEVSLP
DS8G7	SATA ACTIVITY
DS6D1	PCIE LINK DOWN
DS4G4	WLAN
DS4G3	BT
DS7D1	WWAN

Error Type	Error Code	Caps Lock LED (DS9H2)	Scroll Lock LED (DS7G1)	Num Lock LED (DS9J1)
No Error	0	Off	Off	Off
RSMRST_PWRGD_N	1	Off	Off	Flash
PM_SLP_S5_N	2	Off	Flash	Off
PM_SLP_S4_N	3	Off	Flash	Flash
PM_SLP_S3_N	4	Flash	Off	Off
PM_SLP_M_N	5	Flash	Off	Flash
ALL_SYS_PWRGD	6	Flash	Flash	Off
PLT_RST_N	7	Flash	Flash	Flash
DOCK_SYS_PWRGD_N	8	On	On	Flash
SUSWARNB	9	On	Flash	On

Note: KSC Thermal Shutdown is indicated by flashing of Num_Lock and Caps_Lock LEDs alternatively.
DS7G1 acts as led indication for error code in case of any error otherwise works as power button LED

[PAGE_TITLE= LED DISCRIPTION]

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

Interface	WHL	TGL
Board ID		
PCIE Gen4 – DEKEL PHY	No	Yes
TYPE C	No	Yes
XTAL_IN	24MHz	38.4MHz
Memory	1 Channel	2 channel
CSI	No	Yes

No.	Changes	WHL	TGL	Status
1	XXDP_COMP	24.9 ohm PU to VCCIO	24.9 ohm PU to VCCIN /+VCC1P05_OUT_FET (default) on extra added pin on one of the spare pins of TGL_A0.	implemented
2	XXDDR_COMP[0]	121 ohm PD	121 ohm PD on Pin DW 49	implemented
3	XXDDR_COMP[1]	80.6 ohm PD	80.6 ohm PD on pin DW47	implemented
STRAP				
4	SVID DISABLE STRAP	J3B1 to 1-2	J3B1 to 1-X	WIP
5	GPPC_F10	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K	WIP
6	GPPC_F0*	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K	WIP

[PAGE_TITLE=Z0 VS A0 PINLIST]

8	7	6	5	4	3	2	1			
							MODULE REV DETAILS			
							MODULE NAME REV DATE			
TGL-U 42 ROW RVP's Mphy Allocation										
PCIe Controller		Lane #	Flex IO		HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 3 (SV SKU)			
x4 Controller 1		Lane 0	PCIE3_1_USB31_1							
		Lane 1	PCIE3_2_USB31_2							
		Lane 2	PCIE3_3_USB31_3							
		Lane 3	PCIE3_4_USB31_4							
x4 Controller 2		Lane 4	PCIE3_5		Lane 0 for x4 PCIe slot		x4 PCIe Slot			
		Lane 5	PCIE3_6		Lane 1 for x4 PCIe slot					
		Lane 6	PCIE3_7_LAN_0A_UFS_00		Jacksonville Gbe LAN					
		Lane 7	PCIE3_8_LAN_0B_UFS_01		x1 PCIe Slot					
x4 Controller 3		Lane 8	PCIE3_9_LAN_0C_UFS_1_00		M.2 Key M x4 SSD(Lane reversal for x4 PCIe)	SATA Direct Connect	HSIO Connector			
		Lane 9	PCIE3_10_UFS_1_01							
		Lane 10	PCIE3_11_SATA_0							
		Lane 11	PCIE3_12_SATA_1							
x4 Controller 4 (Gen 4 North side)		CPU Lane0	CPU_PCIE_0		M.2 Key M x4 SSD	x4 PCIe Slot				
		CPU Lane1	CPU_PCIE_1							
		CPU Lane2	CPU_PCIE_2							
		CPU Lane3	CPU_PCIE_3							

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

IC name	ALC711 ES-1	ALC711 ES-2
package	QFN-48	QFN-48
Bilingual mode(HD-A/SdW)	O	O
Combo jack (HP+MIC2) + Line1	O	O
Line2 (In) port	O	O
SdW Master I/F	O	O
SdW Slave I/F	O	O
Line1(in)/Line2(in)	O	O
VAD energy detector	X	O
VAD buffer(64KB) with SRAM controller	X	O
USB type-c switch and analog switch	X	O
DMIC	2ch	2ch
HP JD type	JD port	Decide by AGPI and CC1/CC2 status
Power strap	Slew rate(MSB)	Slew rate/self-time turn off/SdW slave ID
GPIO2	X	O
LDO4	X	O
LINE2-VREFO	X	O

[PAGE_TITLE - ALC711 ES1 vs ES2]

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MODULE REV DETAILS							
MODULE NAME REV DATE							

SRC CLK		SRC CLK REF		TGL U RVP mPHY allocation- DDR4			
HSIO Topology 1 (Default)		HSIO Topology 2		HSIO Topology 3 (SV SKJ)		HSIO Connector	
0	0	CPU Gen4 PCIe x4 M.2 SSD		CPU Gen4 x4 PCIe Slot			
1	1	M.2 Hybrid Key E- (WLAN x1 PCIe)					
2	2	M.2 Key-B WWAN X1 PCIe					
3	3	x4 M.2 SSD(Lane reversal for x4 PCIe)					
4	4	Gbe LAN					
5	5	x1 PCIe Slot					
6	6	PCH PCIe x4 PCIe DT Slot					

[PAGE_TITLE=CLK_SRC MAPPING]

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

RefDes	Jumper Description	Default
J1A3	MIPI60 OVERRIDE N	'1-X'
J2H3	MIPI60 PRESENT1 N	'1-X'
J1C1	TYPEC DISABLE	'1-X'
J1F3	NO REBOOT STRAP	'1-X'
J1F4	FLASH DESCRIPTOR SECURITY OVERRIDE STRAP	'1-X'
J3B1	SVID DISABLE STRAP	'1-X'
J1F4	A0 PERSONALITY STRAP	'1-X'
J3H1	DDI3 HPD	'1-X'
J9J5	BT RF KILL N, WIFI RF KILL N	'1-X,3-X'
J9J4	CNVI Disable	'1-2'
J5U1	TOUCH PANEL POWER SUPPLY GENERATION	'1-2'
J8J3	PROCHOT EC JPR	'1-X'
J9J3	SMC_RST_N JPR	'1-X'
J9J2	SMC_LID JPR	'1-X'
J8D2	SVID CLOCK	'1-2,3-X'
J8D3	SVID ALERT	'1-2,3-X'
J8D4	SVID DATA	'1-2,3-X'
J8G3	PCH GLITCH ISSUE MITIGATION	'1-X'
J7G1	SRTC/RTC CLEAR CMOS JPR	'1-X'
J7H2	SPD_PRSNT JPR	'1-2'
J8H3	FRU SMB CLK S3	'1-2'
J8H5	FRU SMB DATA S3	'1-2'
J6J1	PECI_MUX_CTRL_SNI_R	'1-X'
J8J1	FRU POWER SUPPLY	'1-2'
J6G4	H_PECI_CPU JPR	'1-X'

RefDes	Jumper Description	Default
SW4V1	MIPI60 FN[0:3]	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW5V1	1 - VDDQ_VR_PWRGD - IMVP_VR_EN 2 - ALL_SYS_PWRGD - IMVP_VR_EN 3 - SATAXPCIE_0_SATAGP_0_R 4 - BIOS_REC	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW6J2	1 - EC_SHD_CS_SW 2 - NC 3 - RETIMER_BYPASS_STRAP 4 - ESPI_TESTCRD_DET	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
SW9C1	1 - BUF_PLT_RST_1.8 - WF_CAM_RST_N 2 - WF_CAM_RST_ND - WF_CAM_RST_N 3 +V1.8A - XTAL_SEL1_J 4 +V3.3A - XTAL_IN_J	1-8(OFF); 2-7(ON); 3-6(OFF); 4-5(OFF)
SW8W1	1 - PNP_NPNP_SKU 2 - VIRTUAL_DOCK_DET_N 3 - VIRTUAL_BATTERY 4 - FLIP_TO_TABLET_MODE	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)

[PAGE_TITLE=JUMPER/SWITCH SETTINGS]

MODULE REV DETAILS

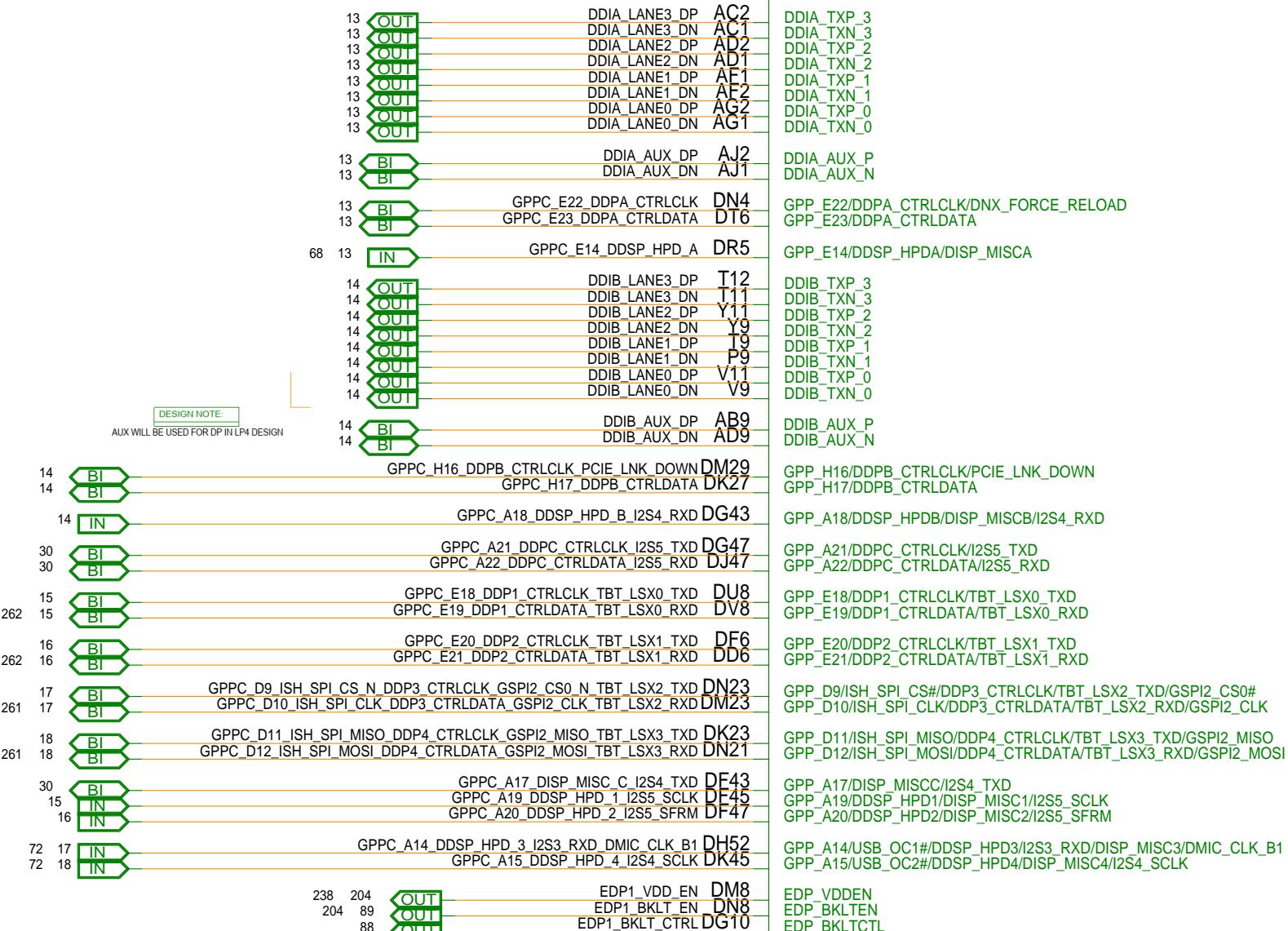
MODULE NAME	REV	DATE

D

D

U4E1
SOC1.6
BGA
TGL_UP3_IP_EXT

1 OF 21

DESIGN NOTE:
AUX WILL BE USED FOR DP IN LP4 DESIGN

DESIGN NOTE:

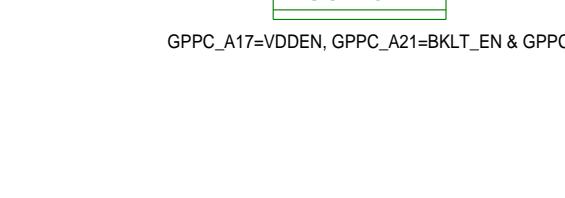
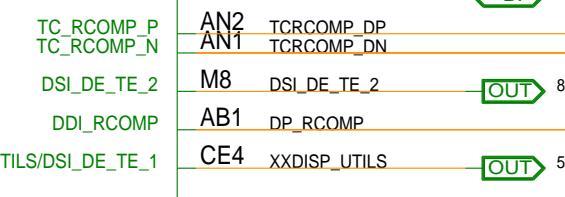
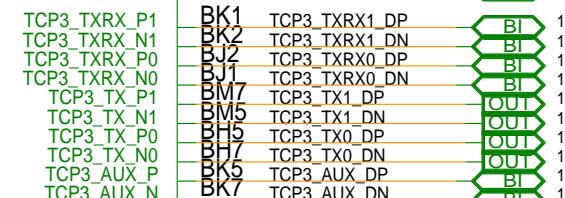
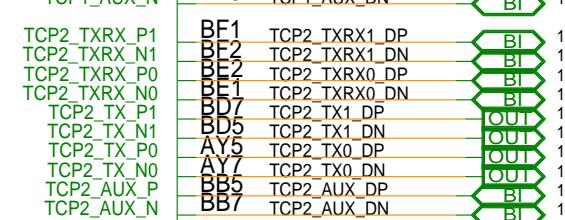
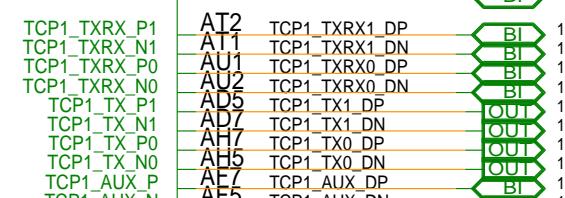
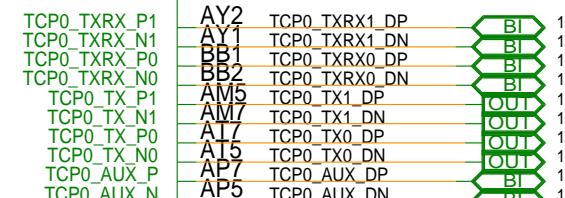
LSX_A:LSX TXD, LSX_B:LSX RXD

DESIGN NOTE:

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LPID6529

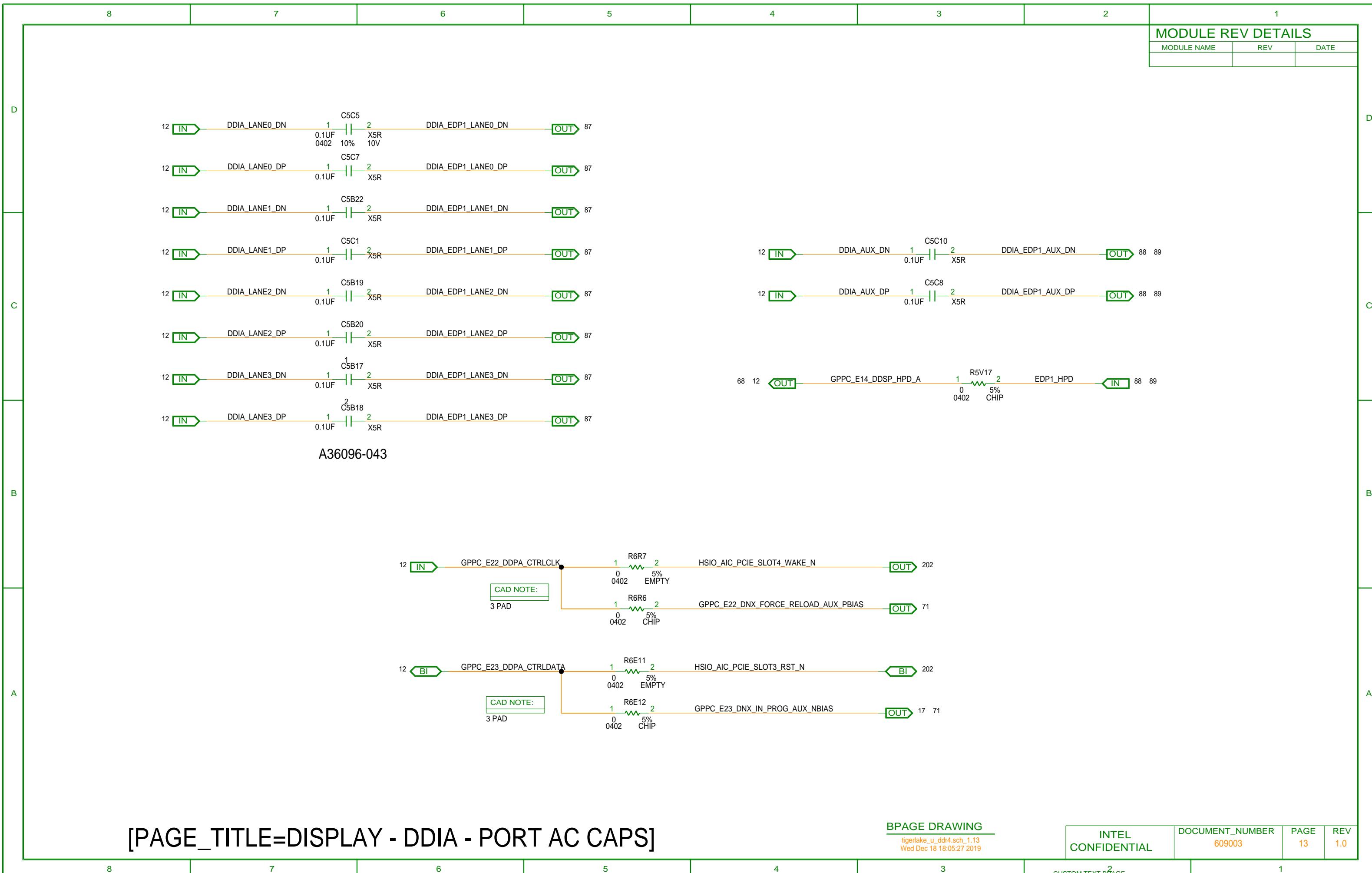
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

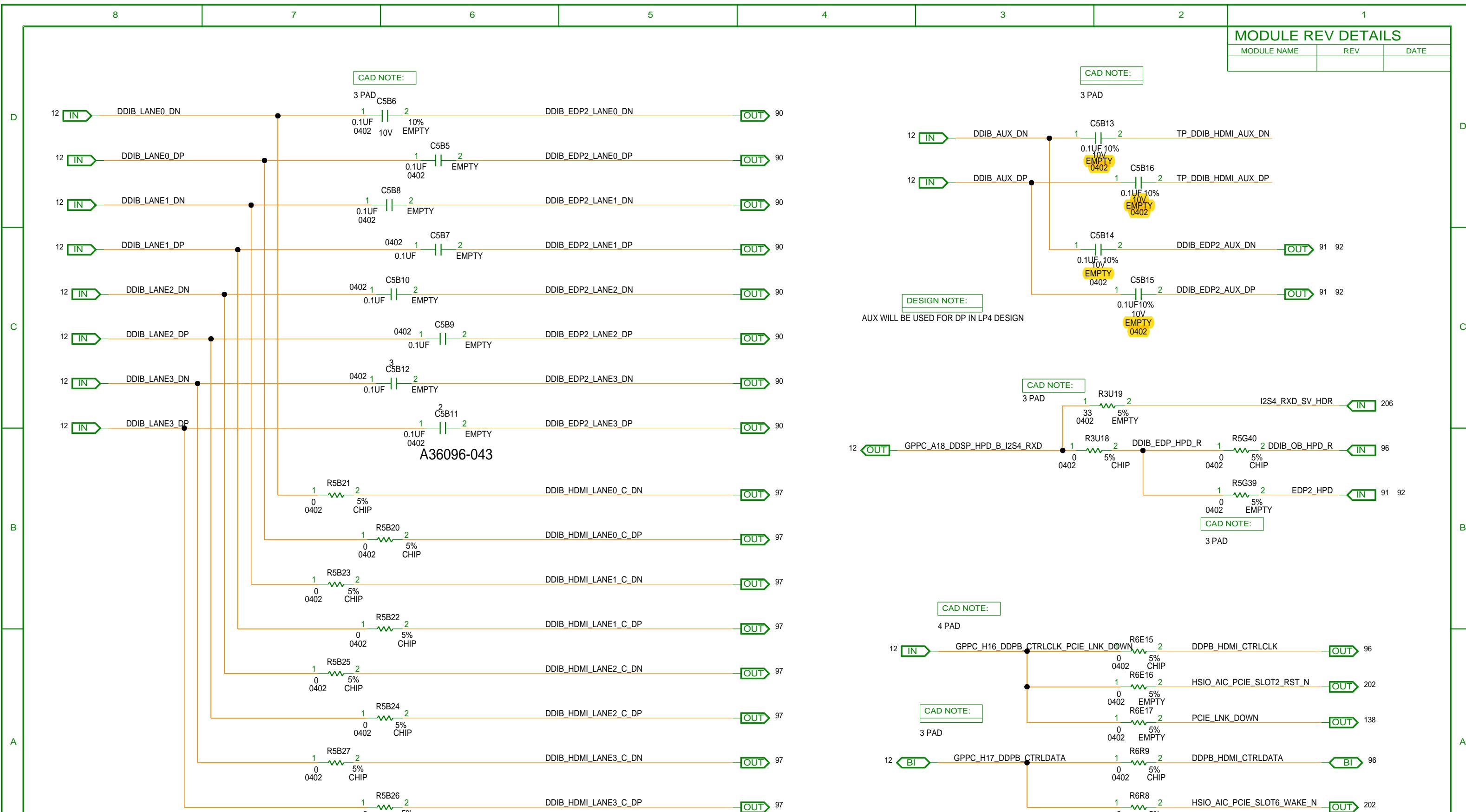
DESIGN NOTE:
GPPC_A17=VDDEN, GPPC_A21=BKLT_EN & GPPC_A22=BKLT_CTRL

1/16W1% CHIP A93548-005

1/16W CHIP 0402 A93548-005

1% 0402 A93548-005

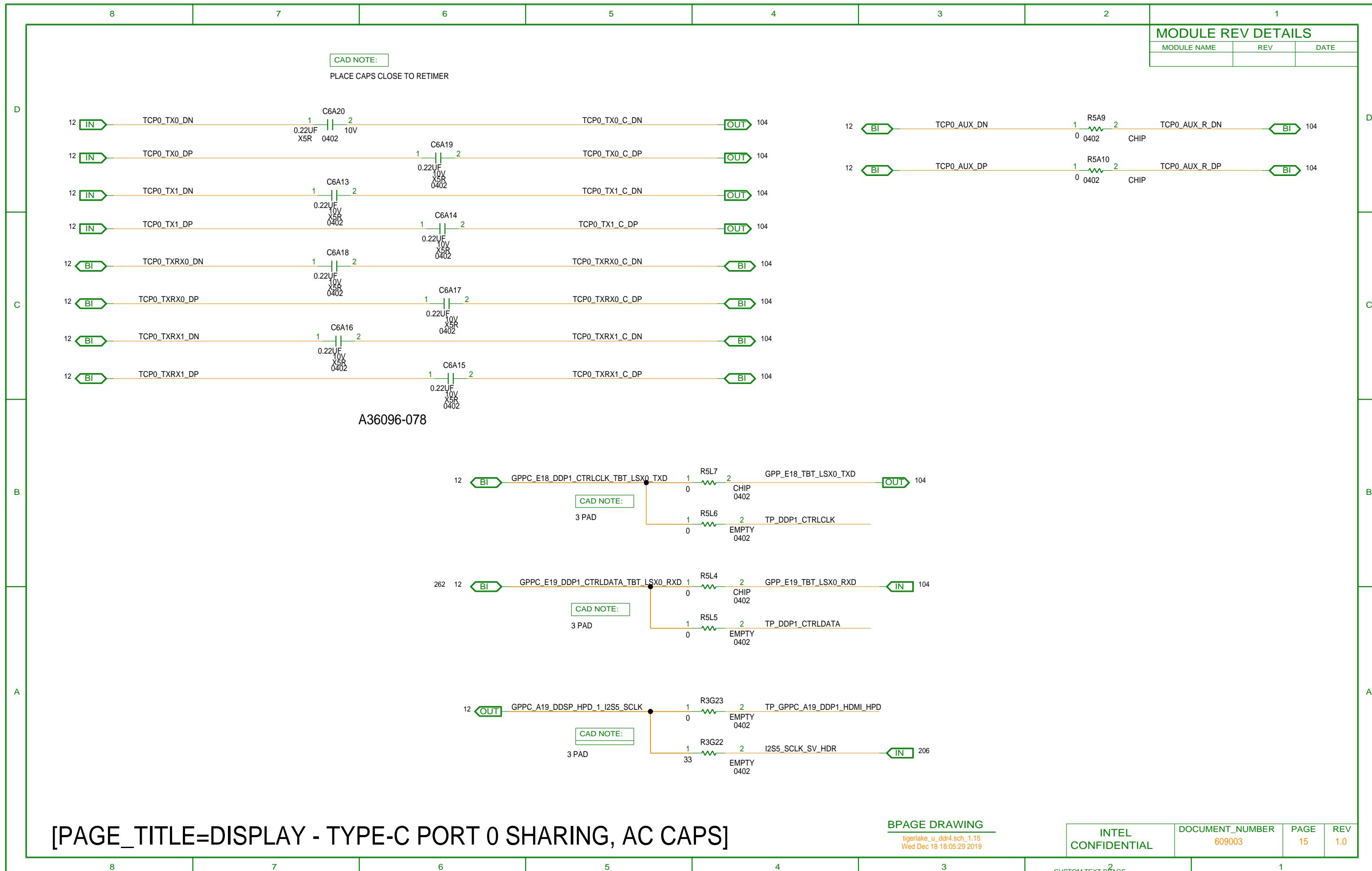


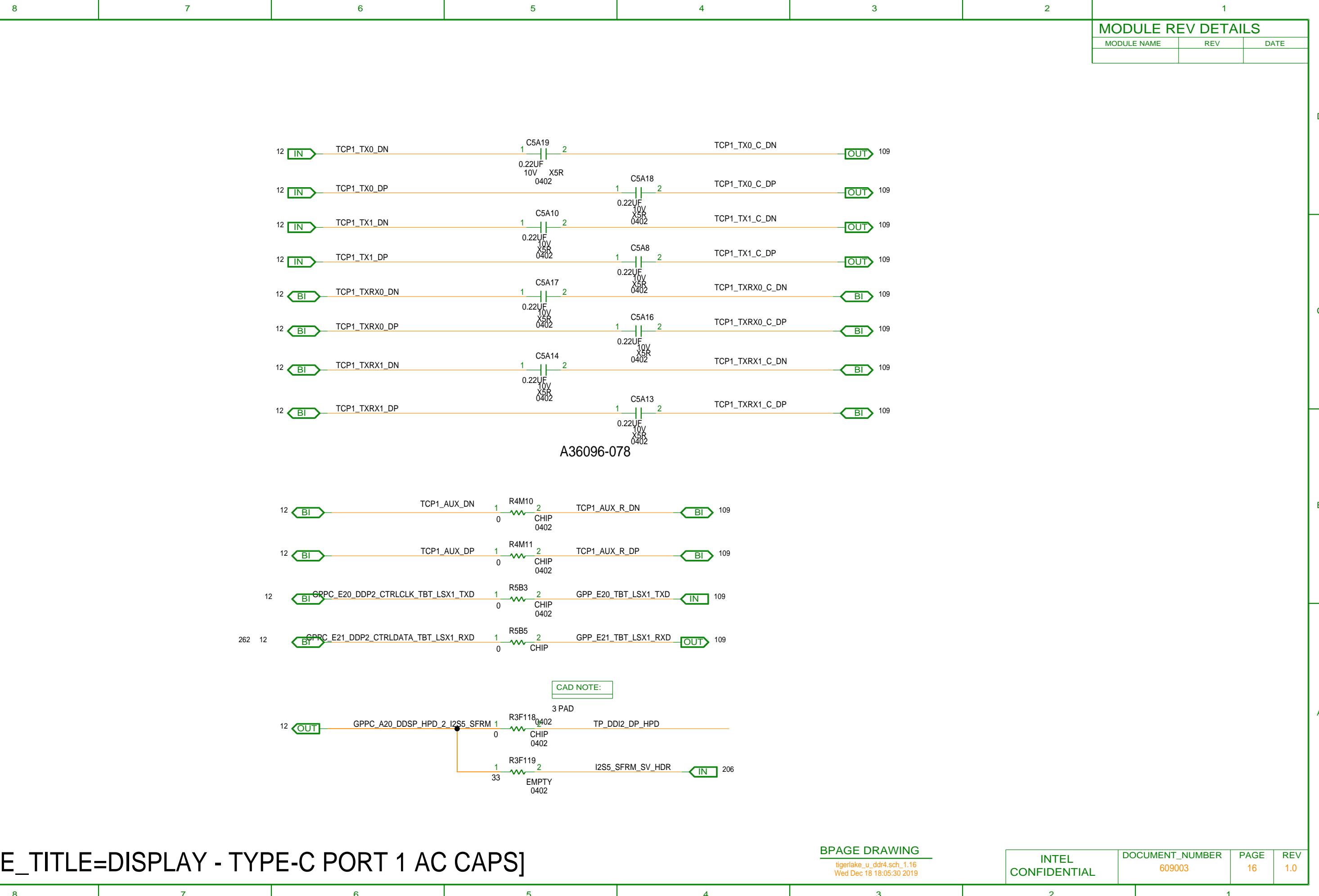


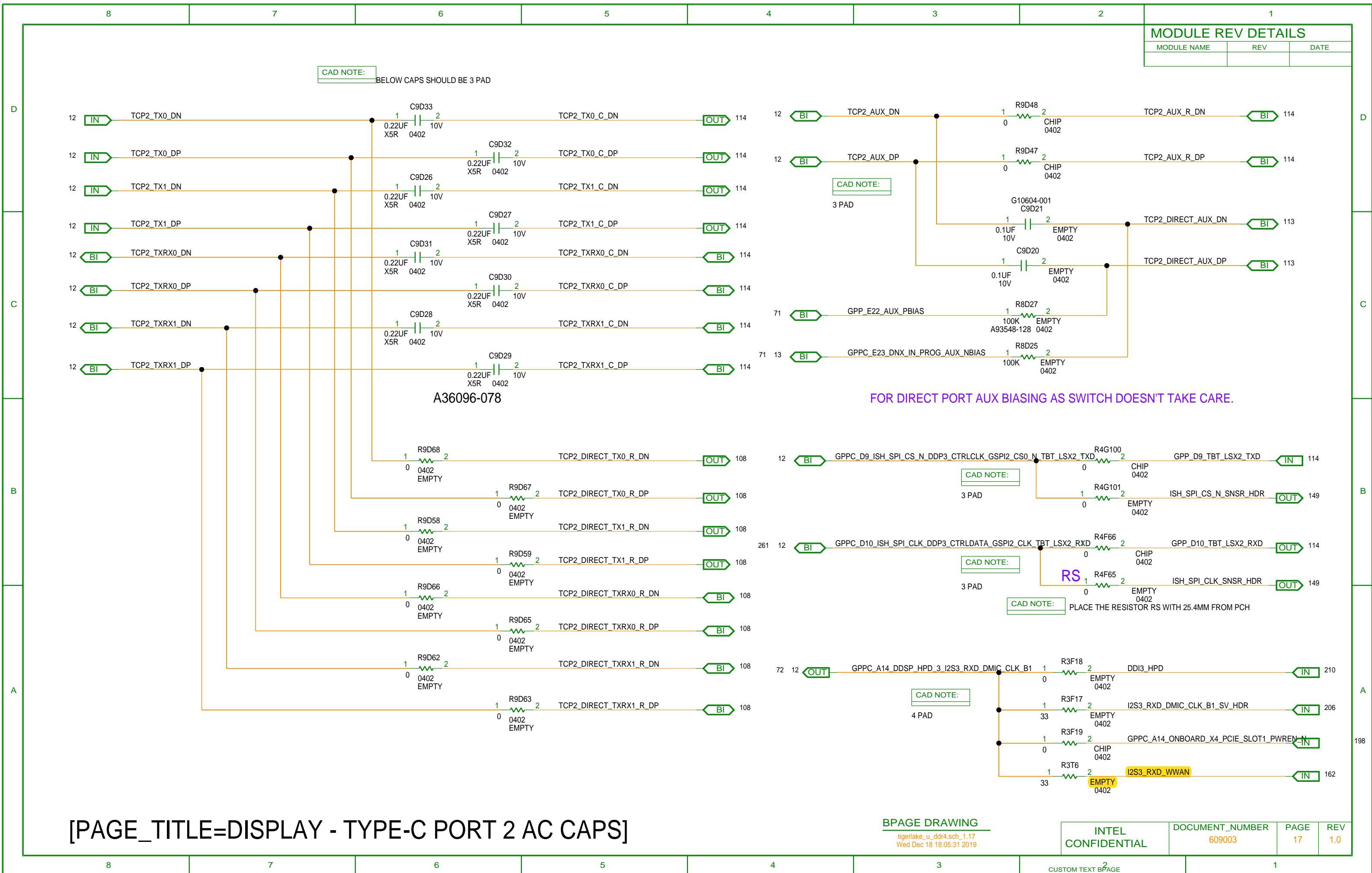
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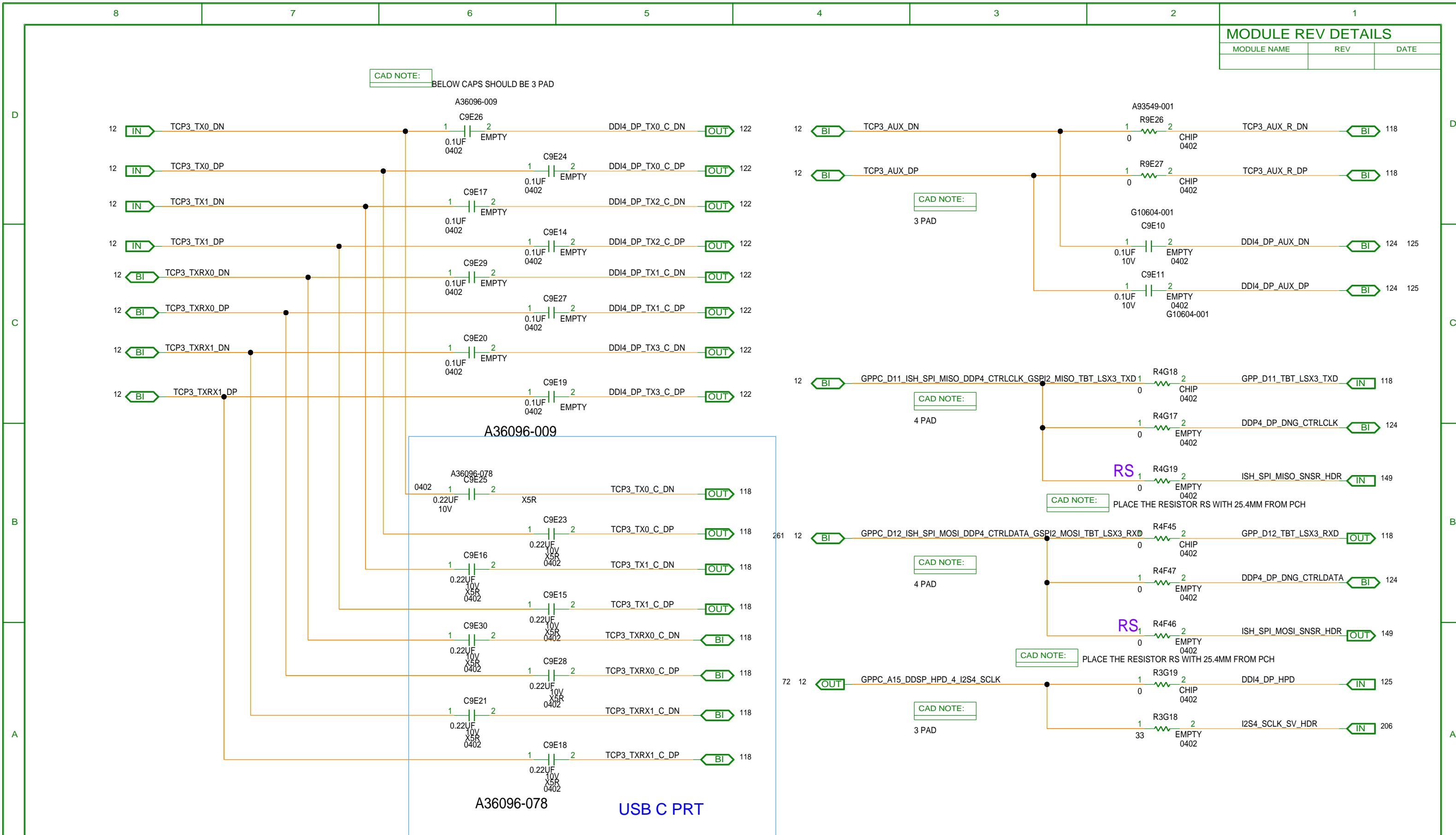
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Wed Dec 18 18:05:28 2019

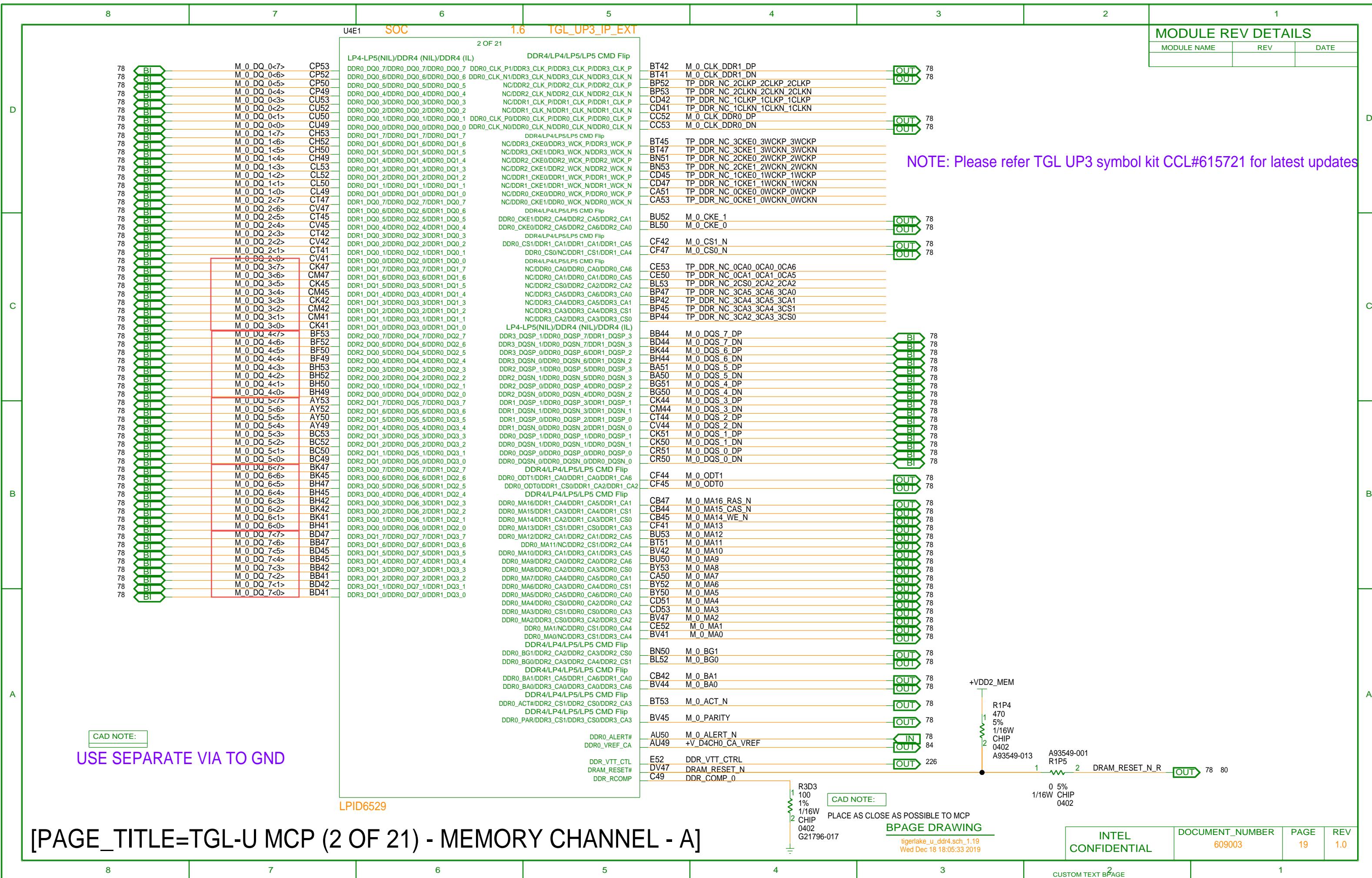
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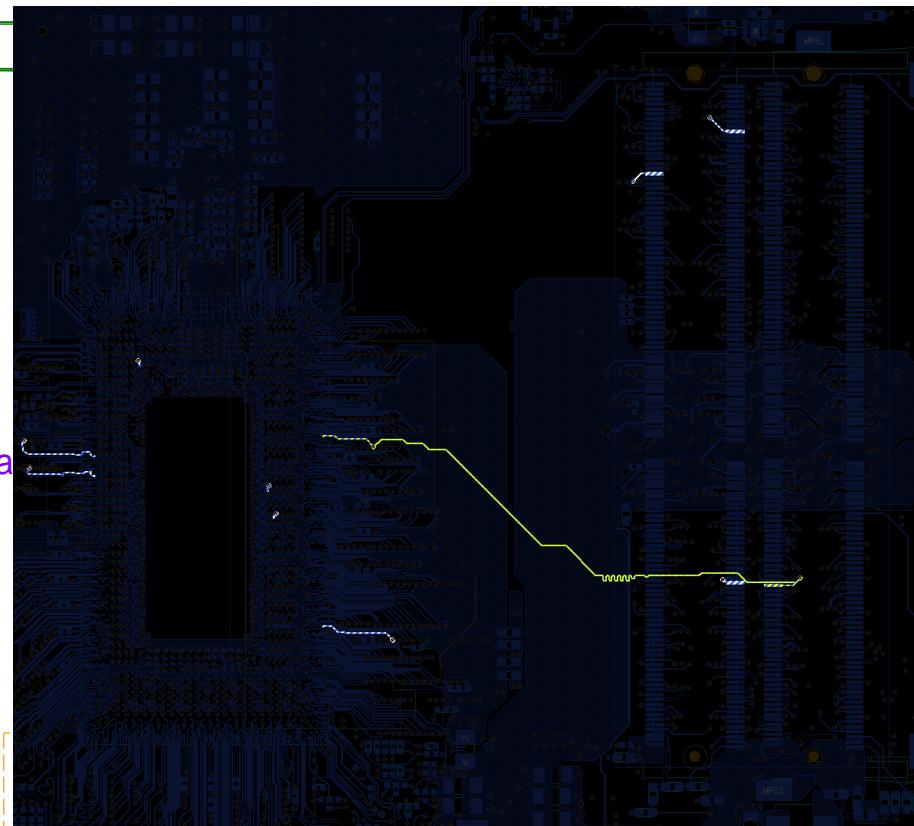
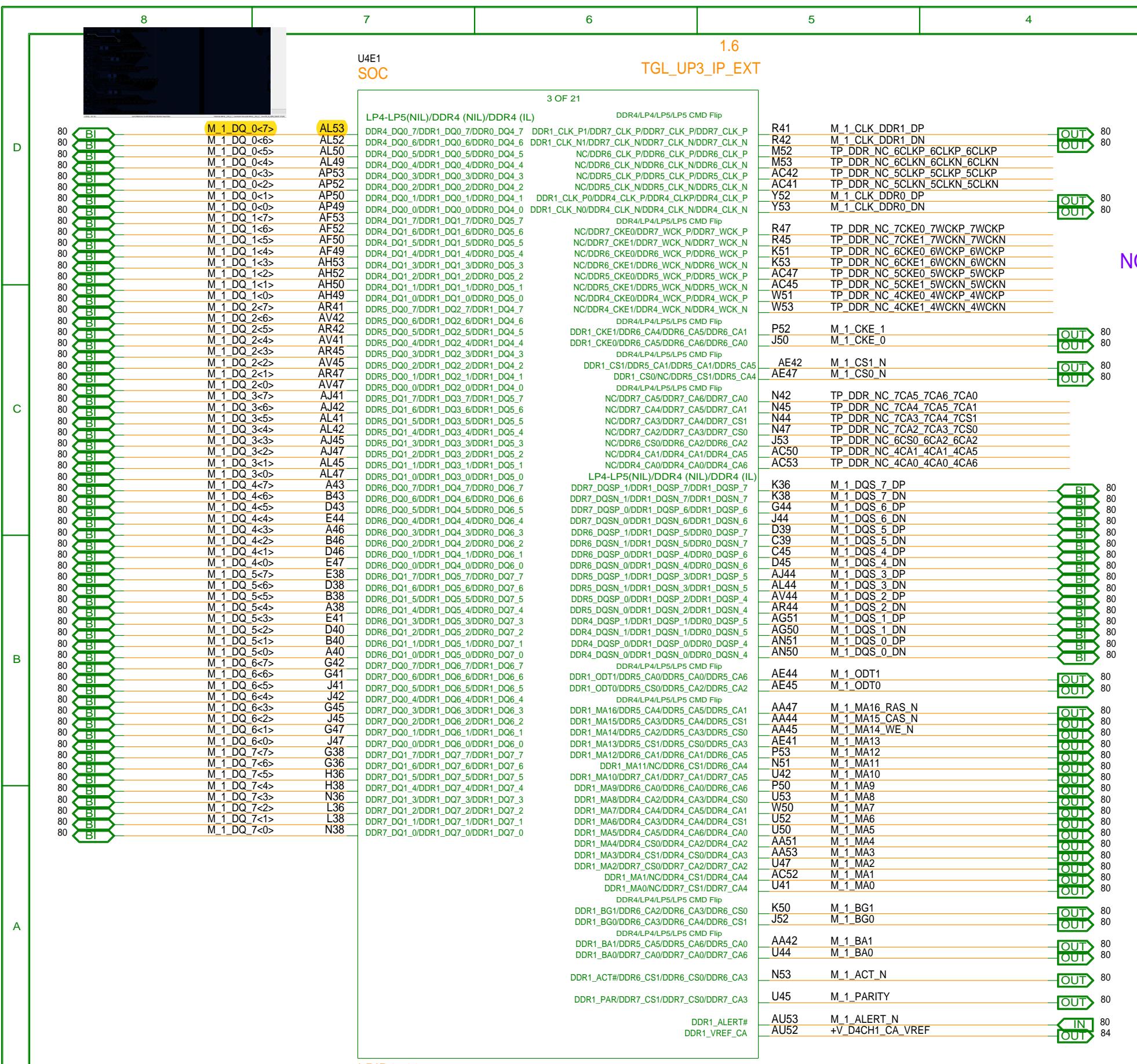






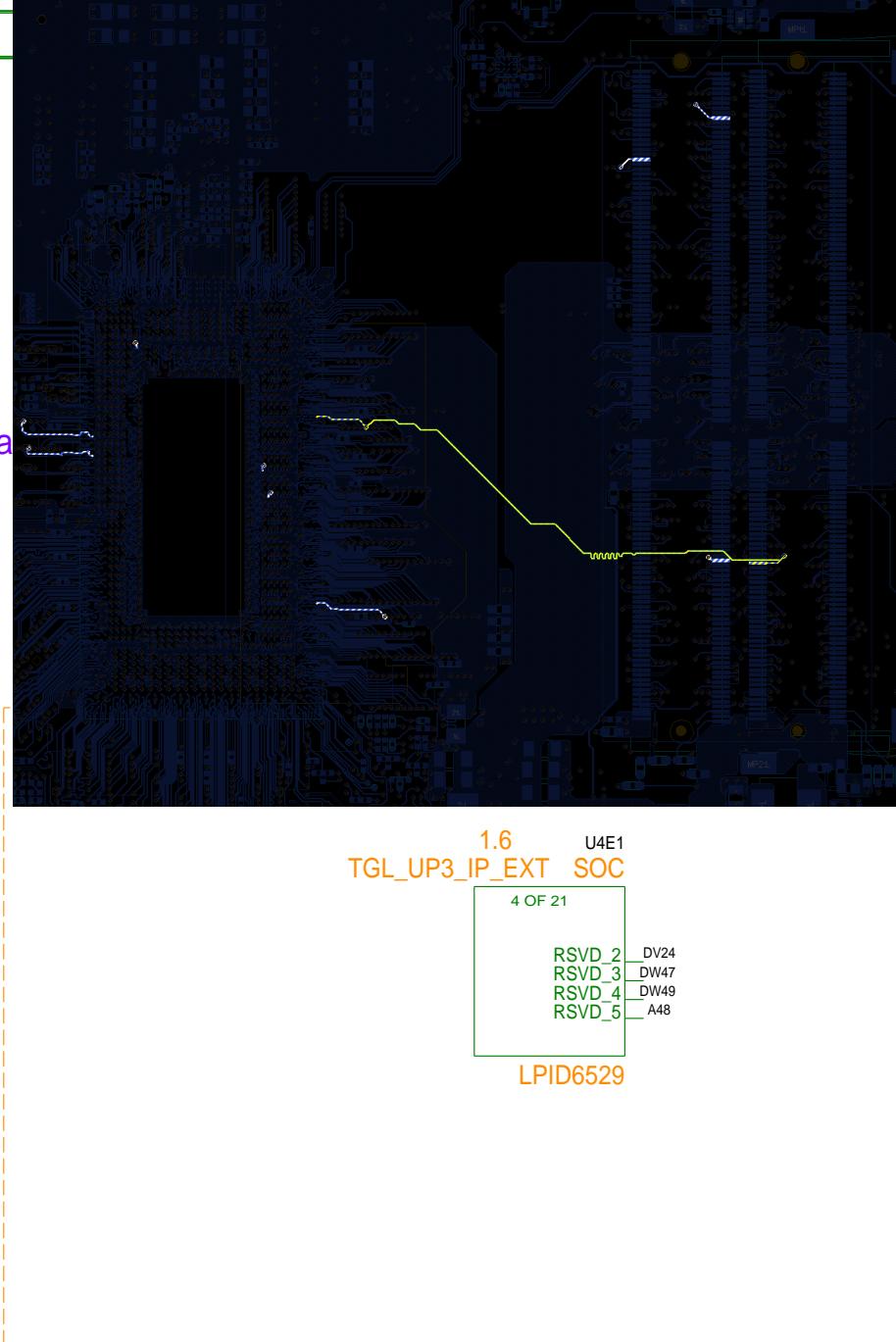




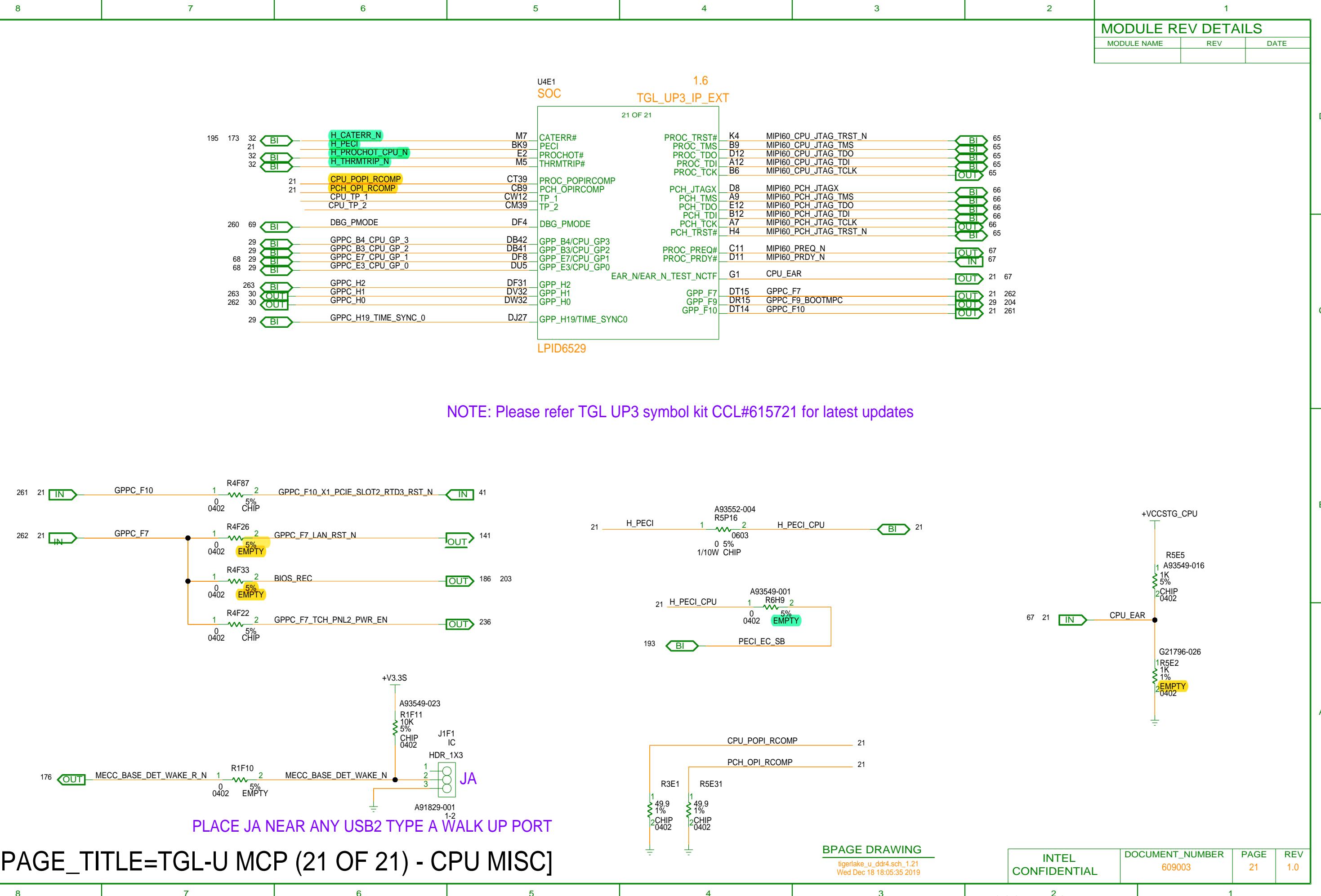


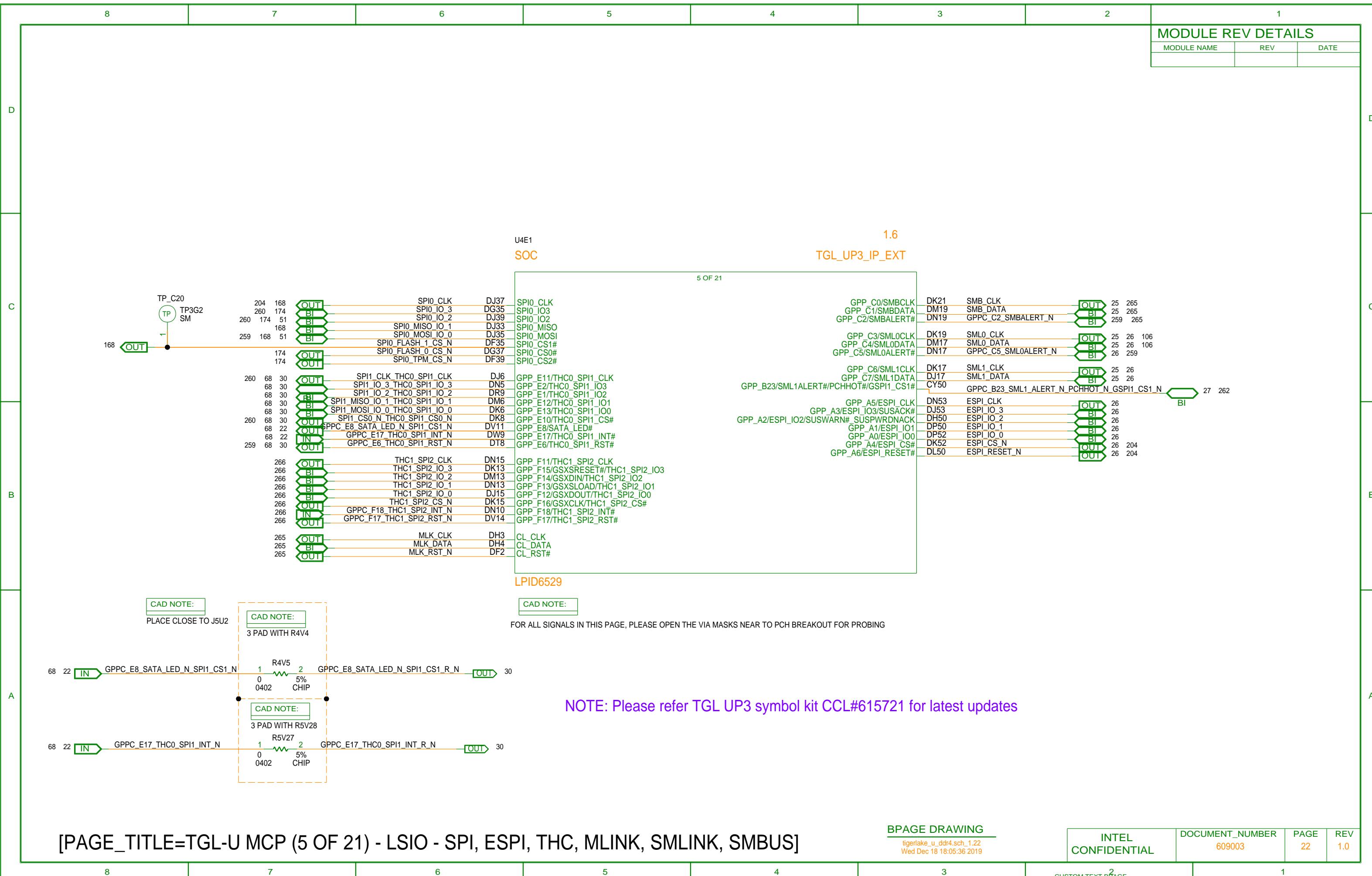
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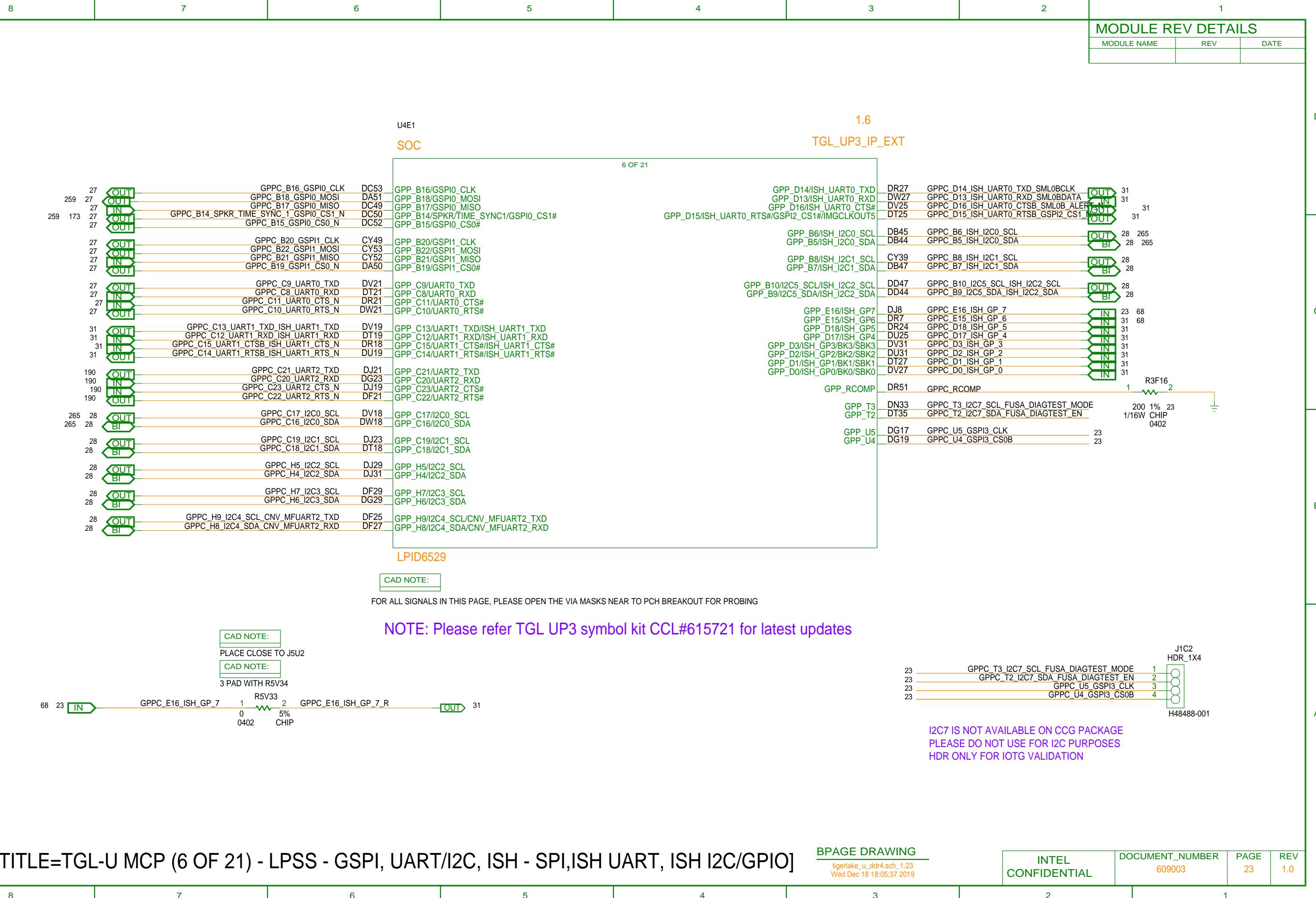
1.6 U4E1
TGL UP3 IP EXT SOC



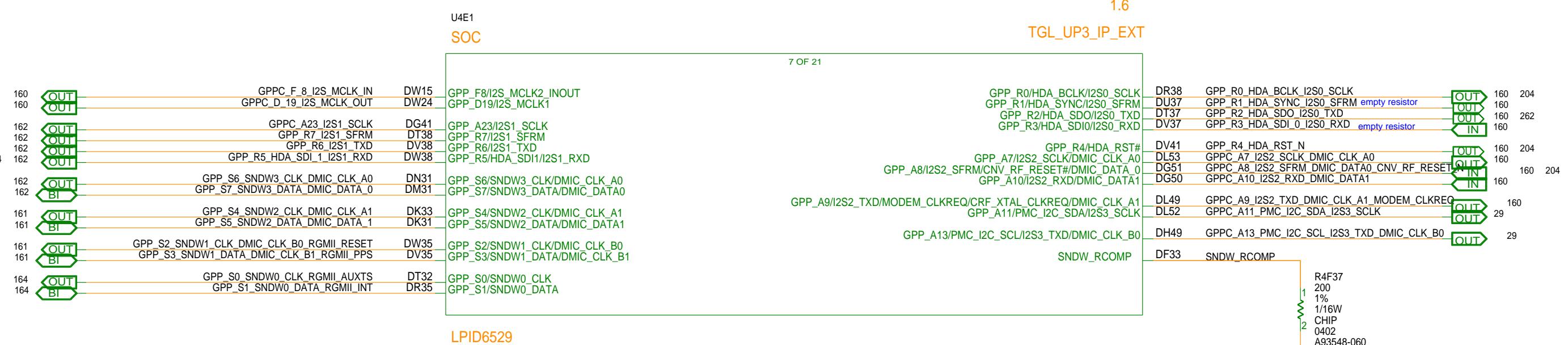
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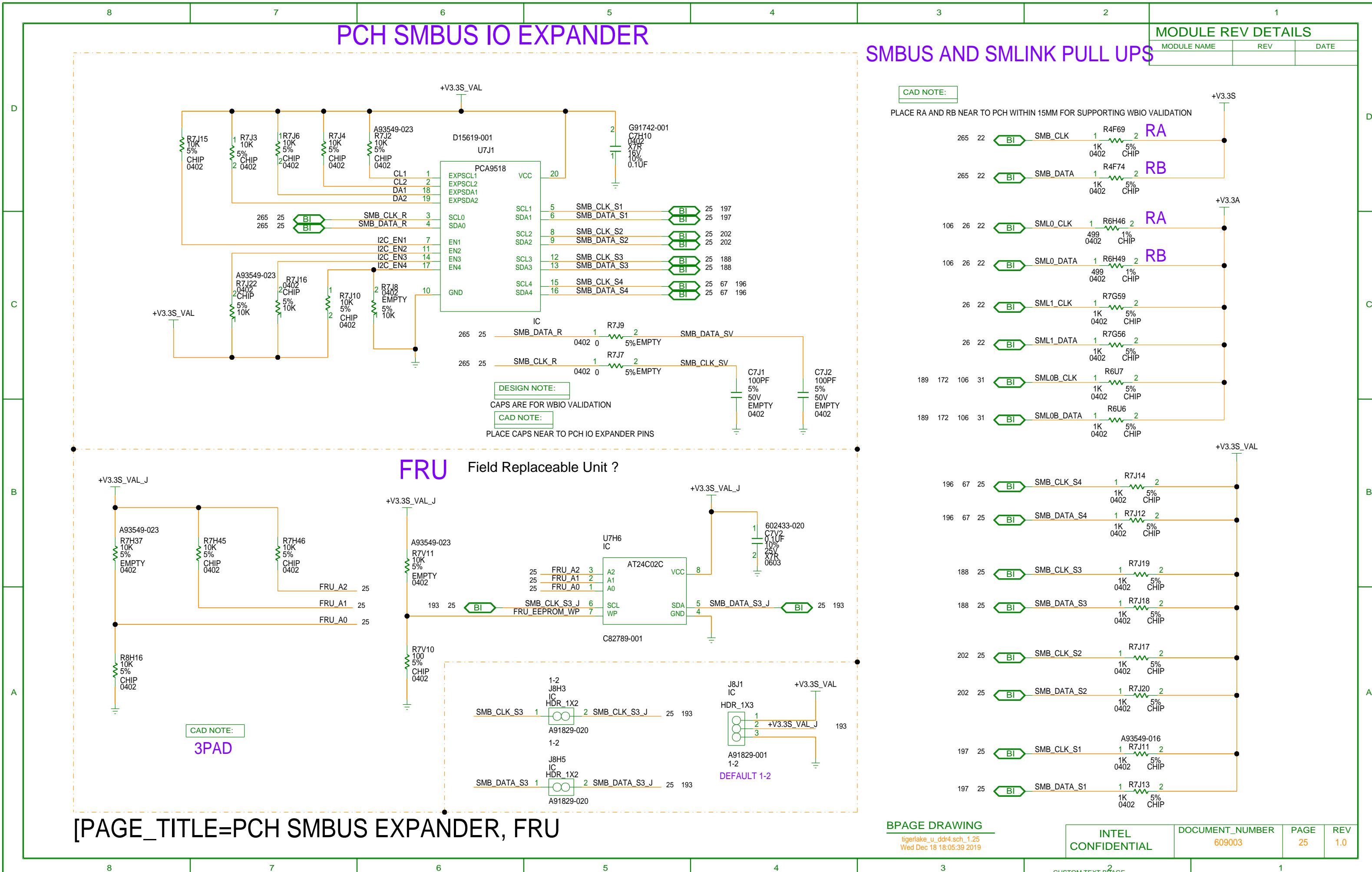


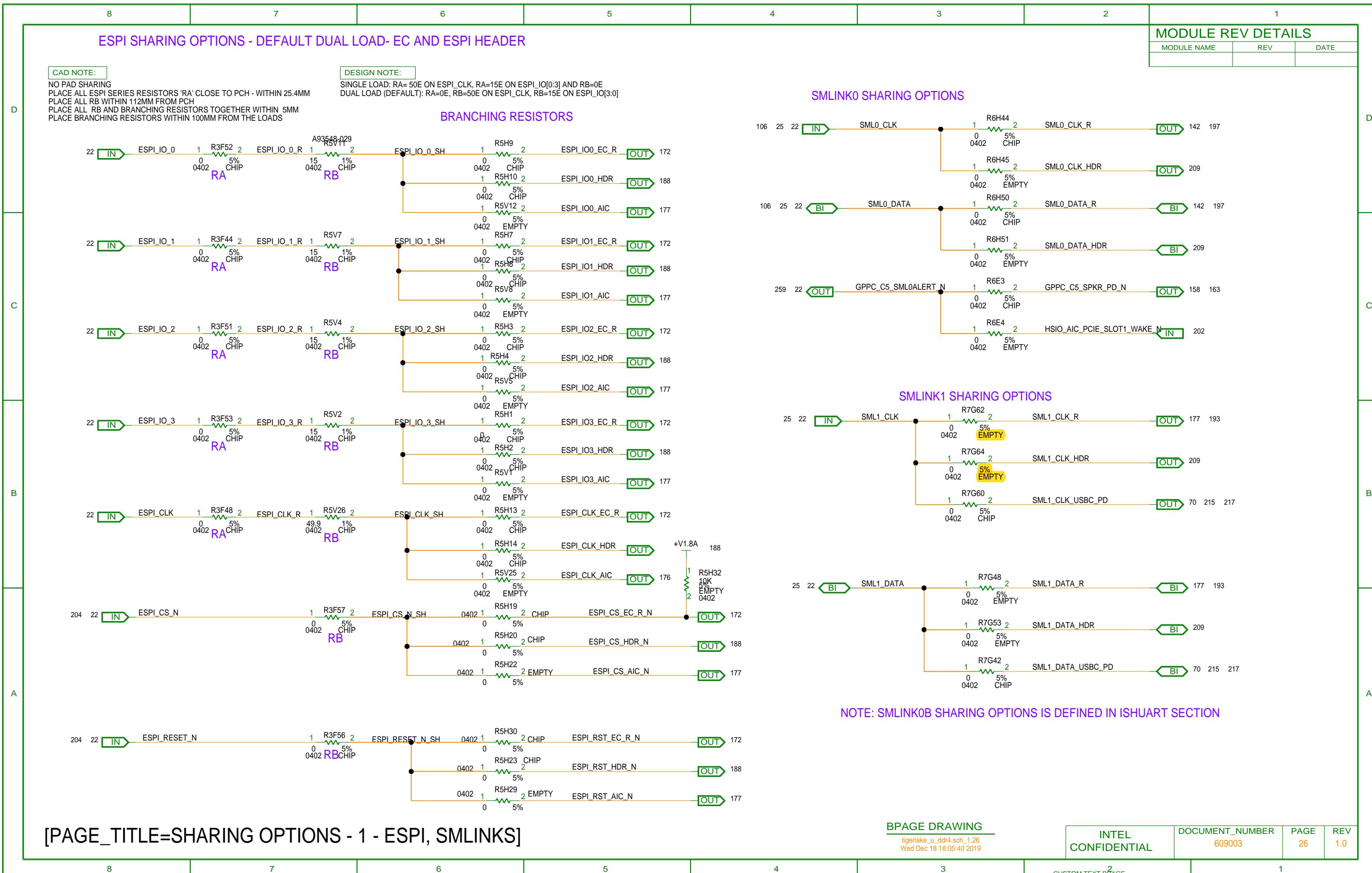


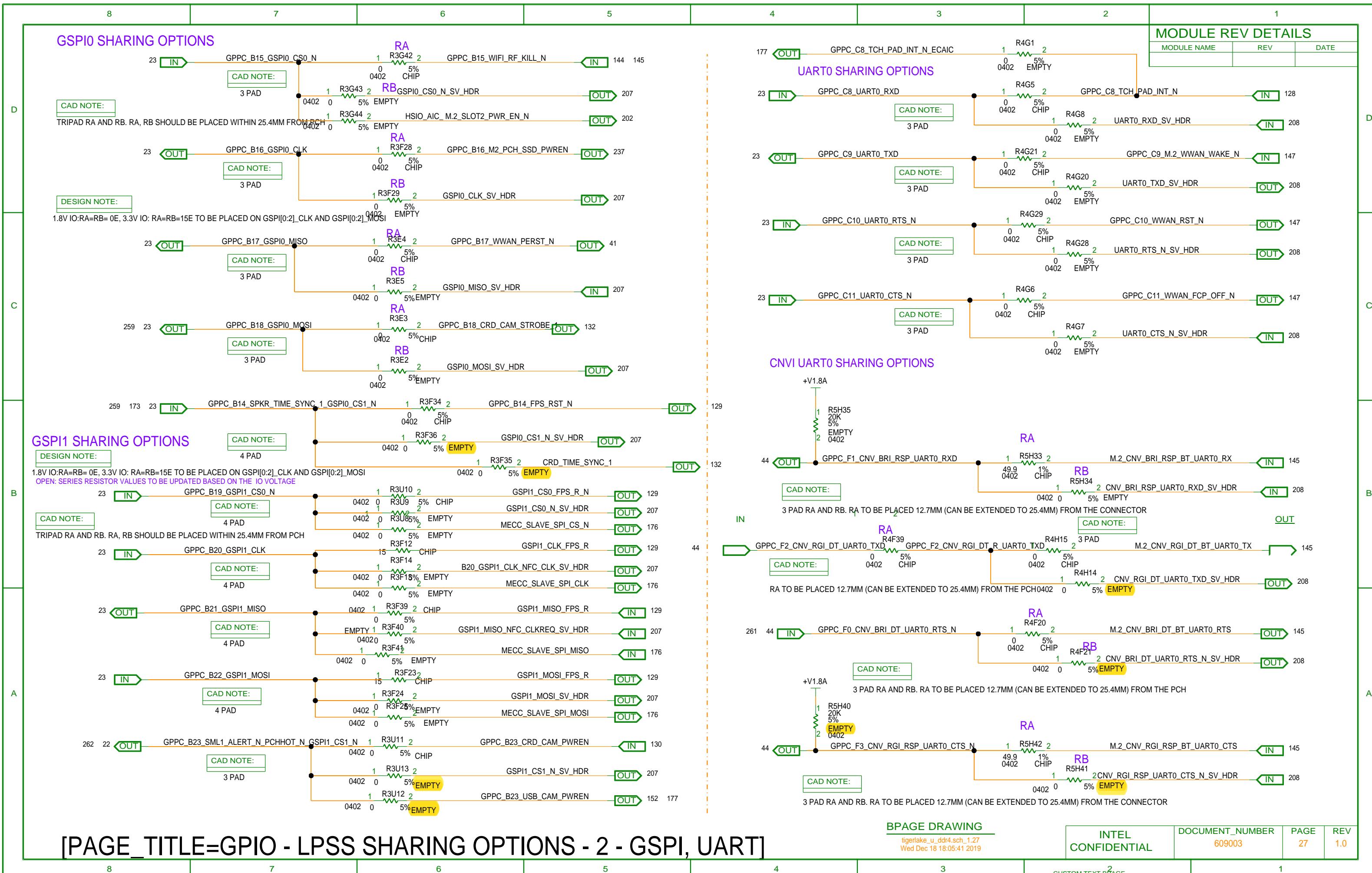
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MODULE REV DETAILS							

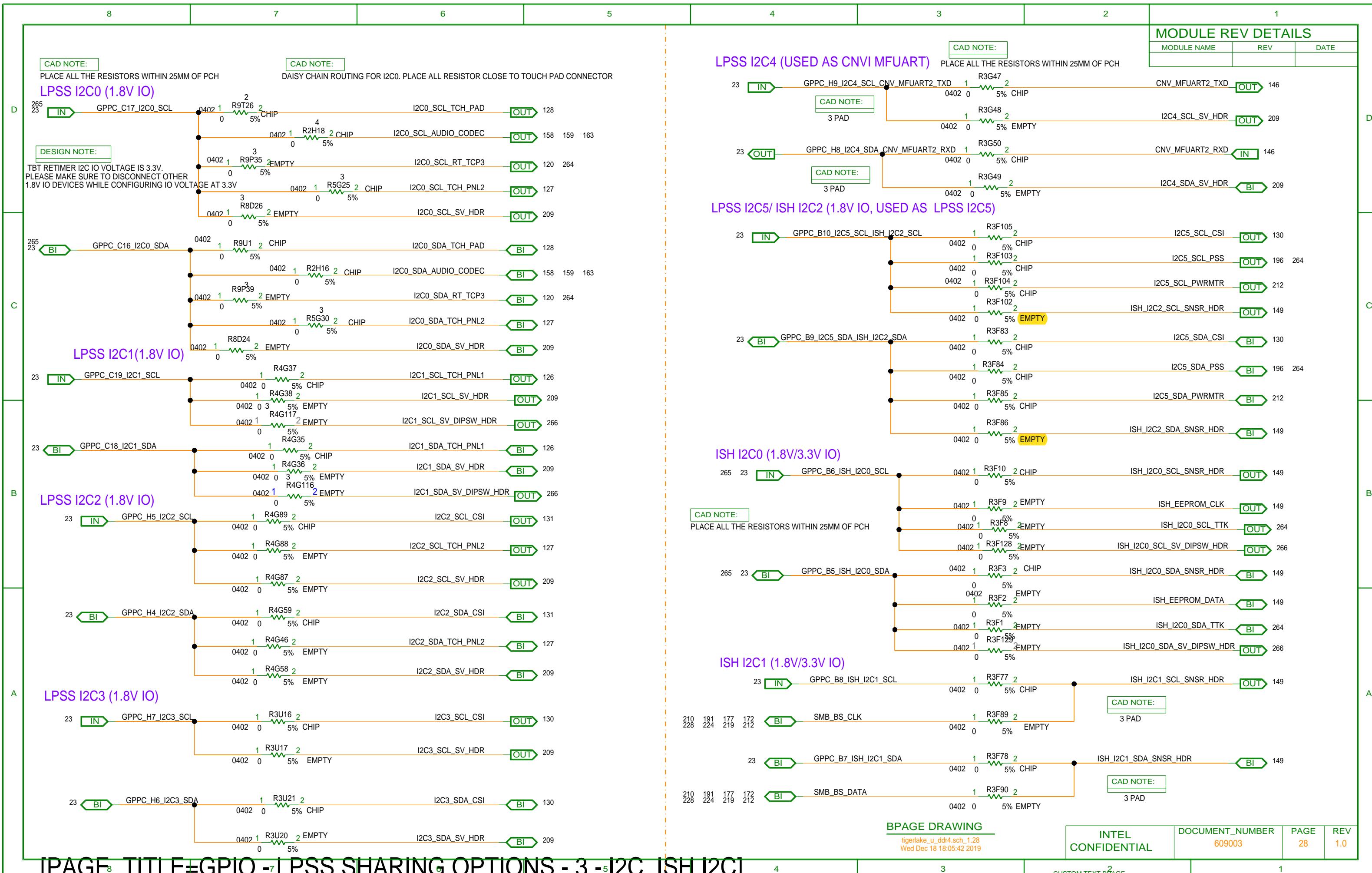


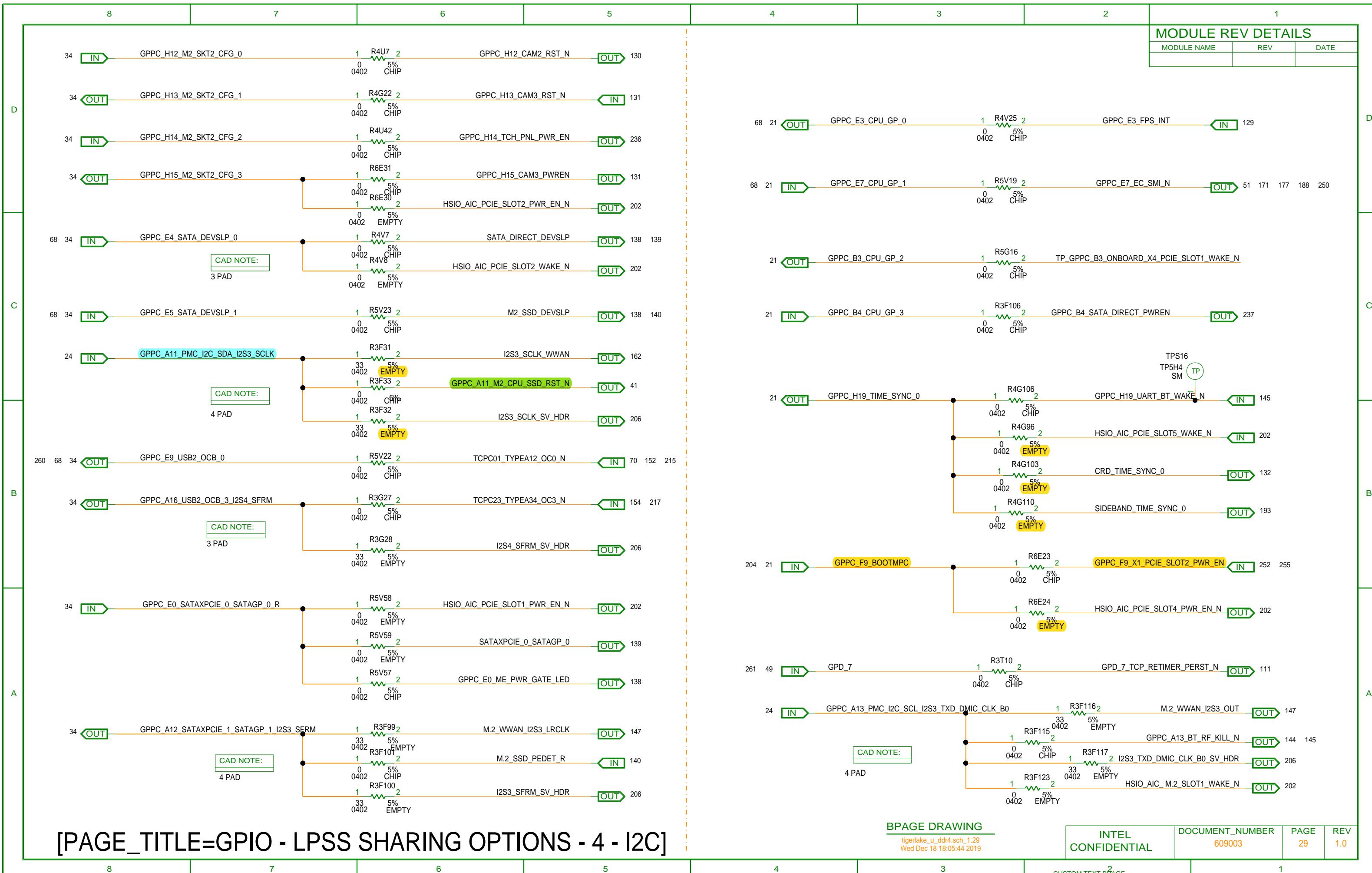
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

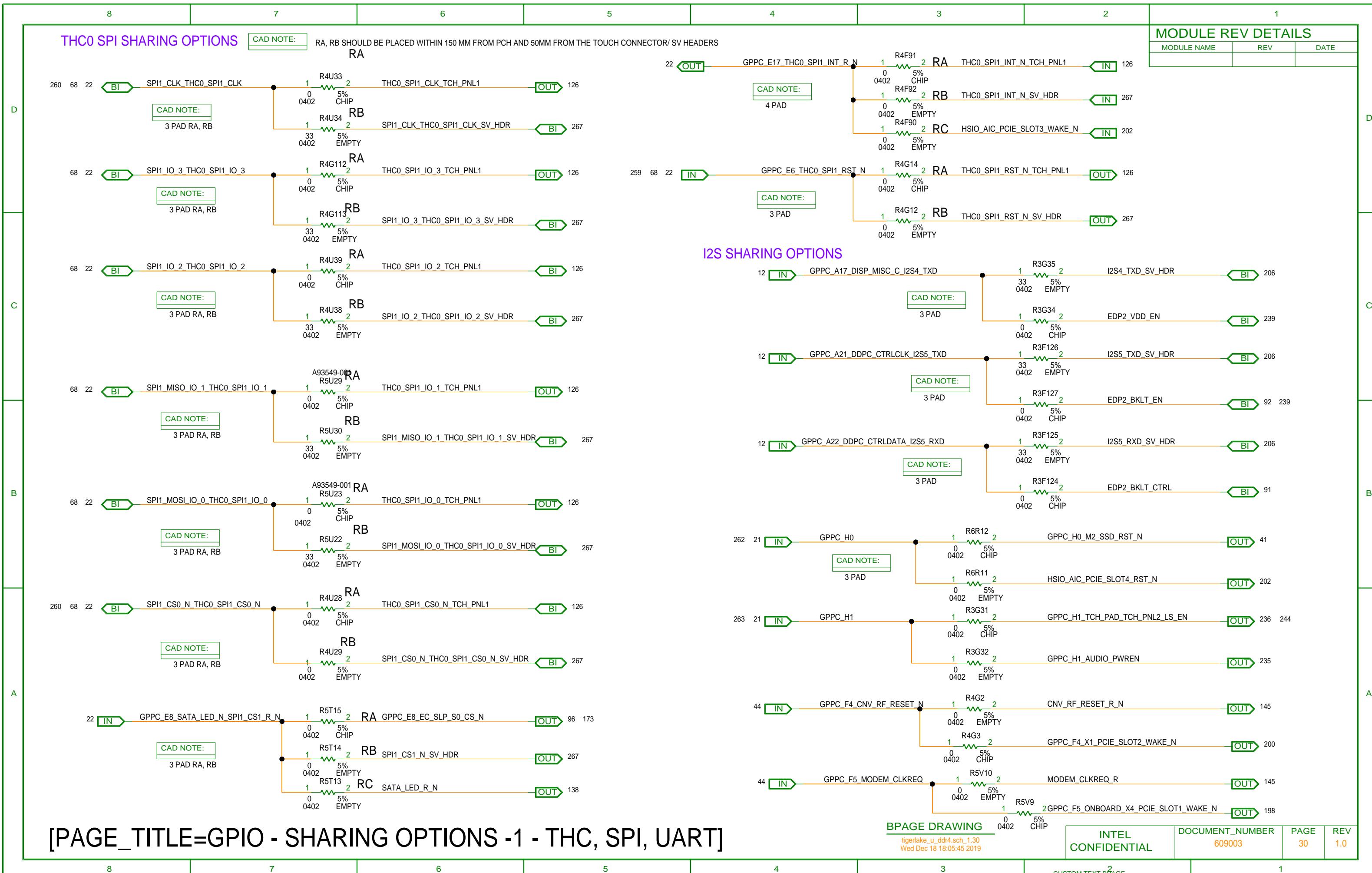


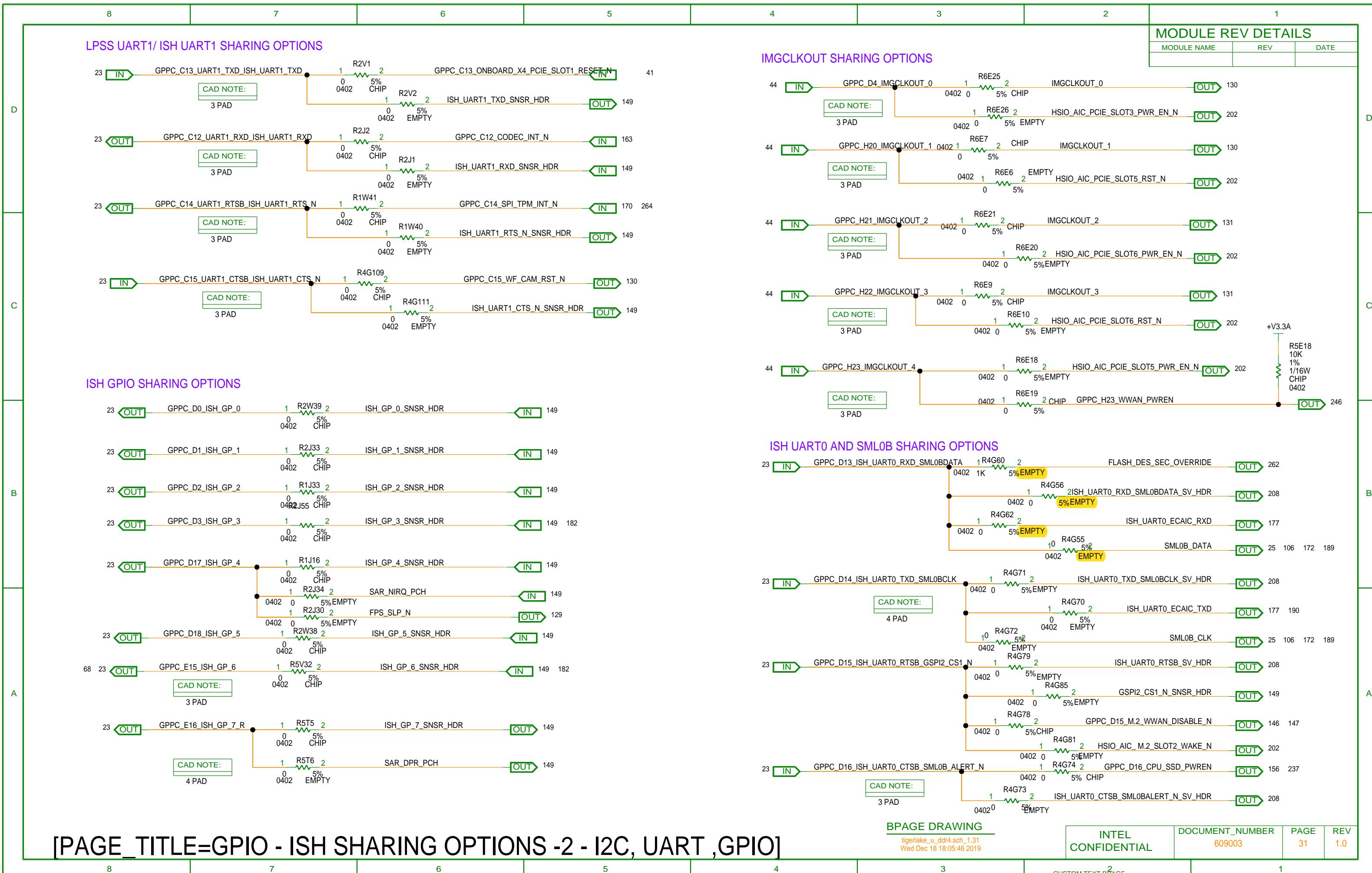

[PAGE_TITLE=SHARING OPTIONS - 1 - ESPI, SMLINKS] 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |





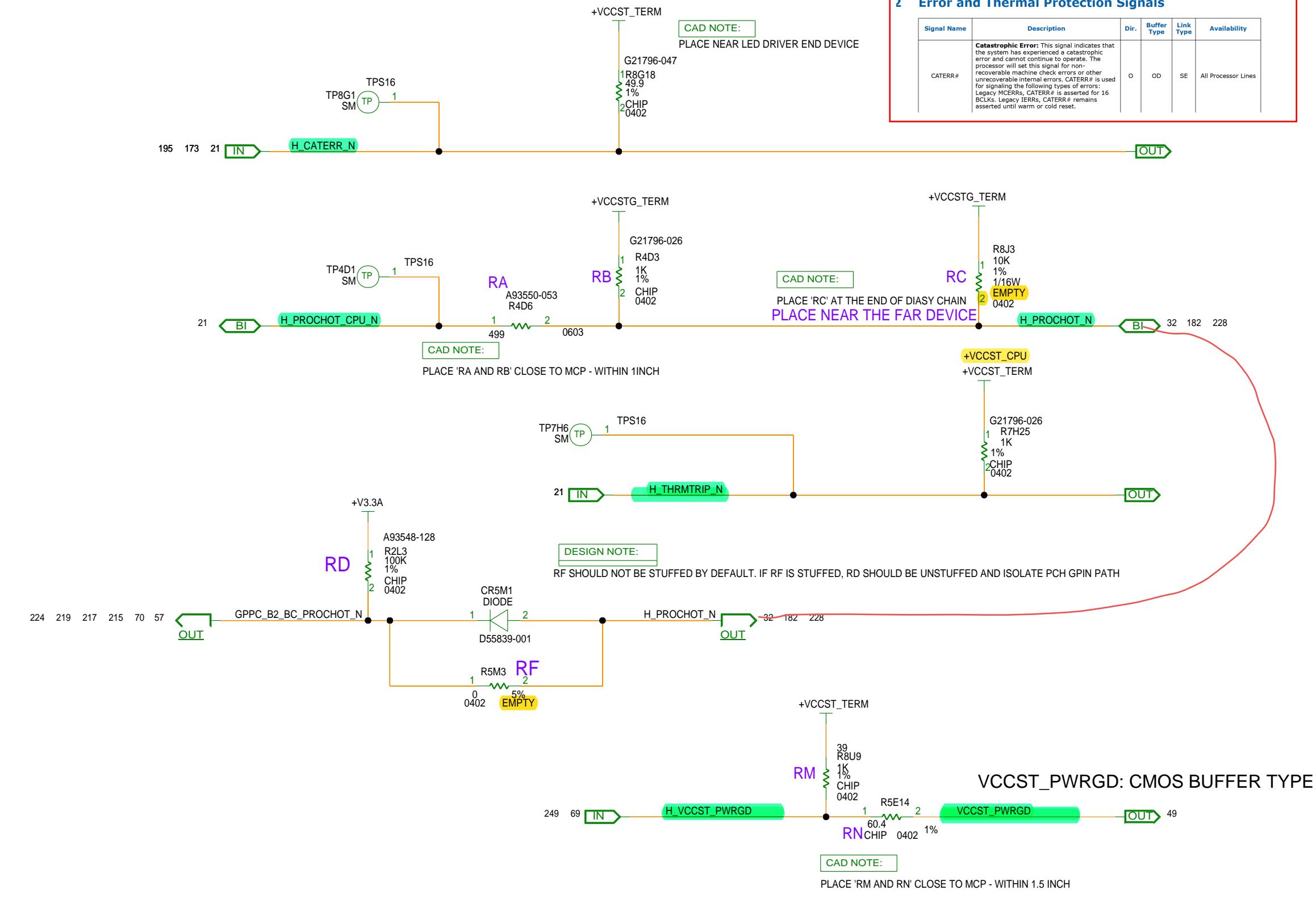






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CPU SIDEBAND SIGNALS

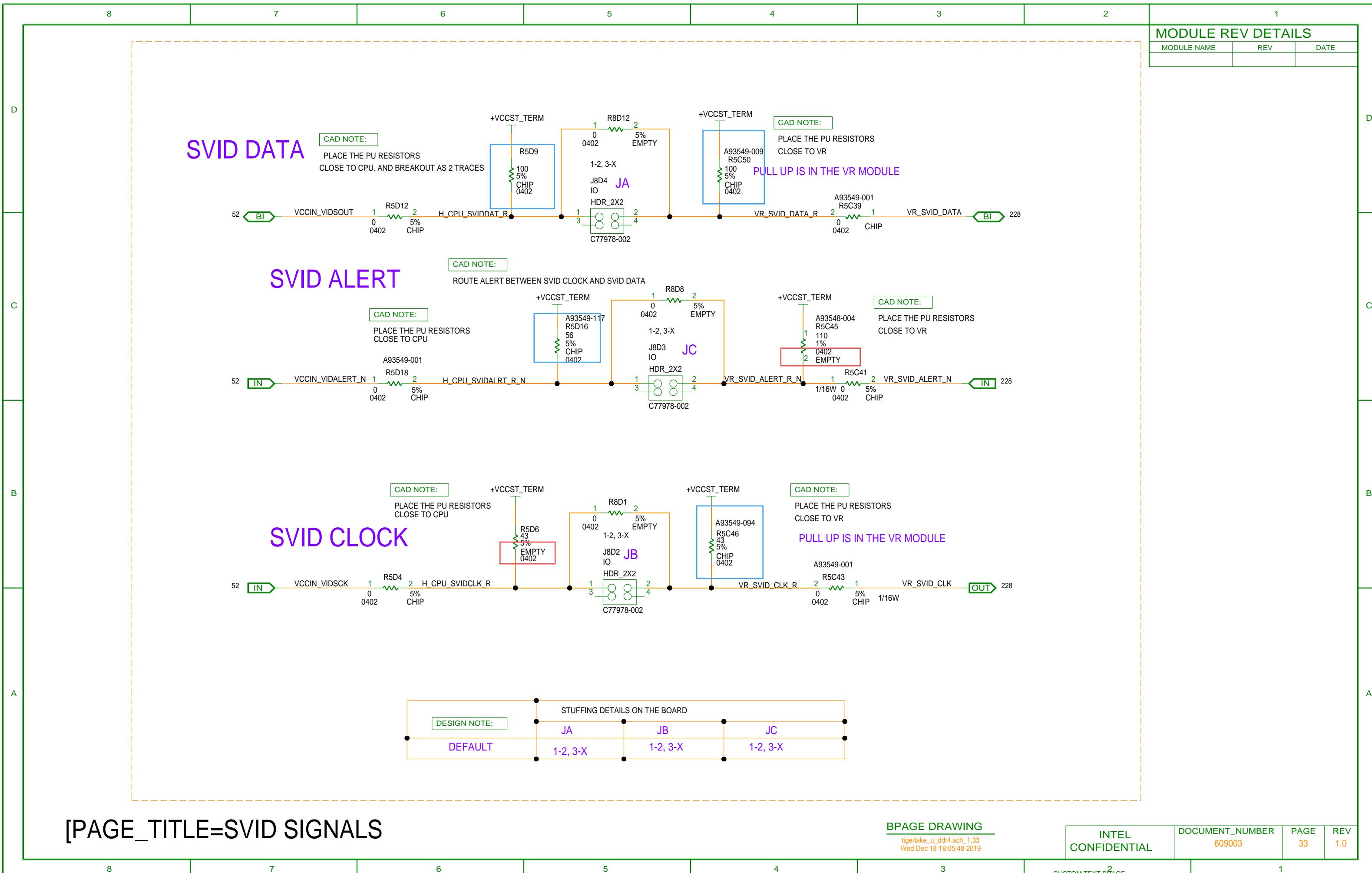


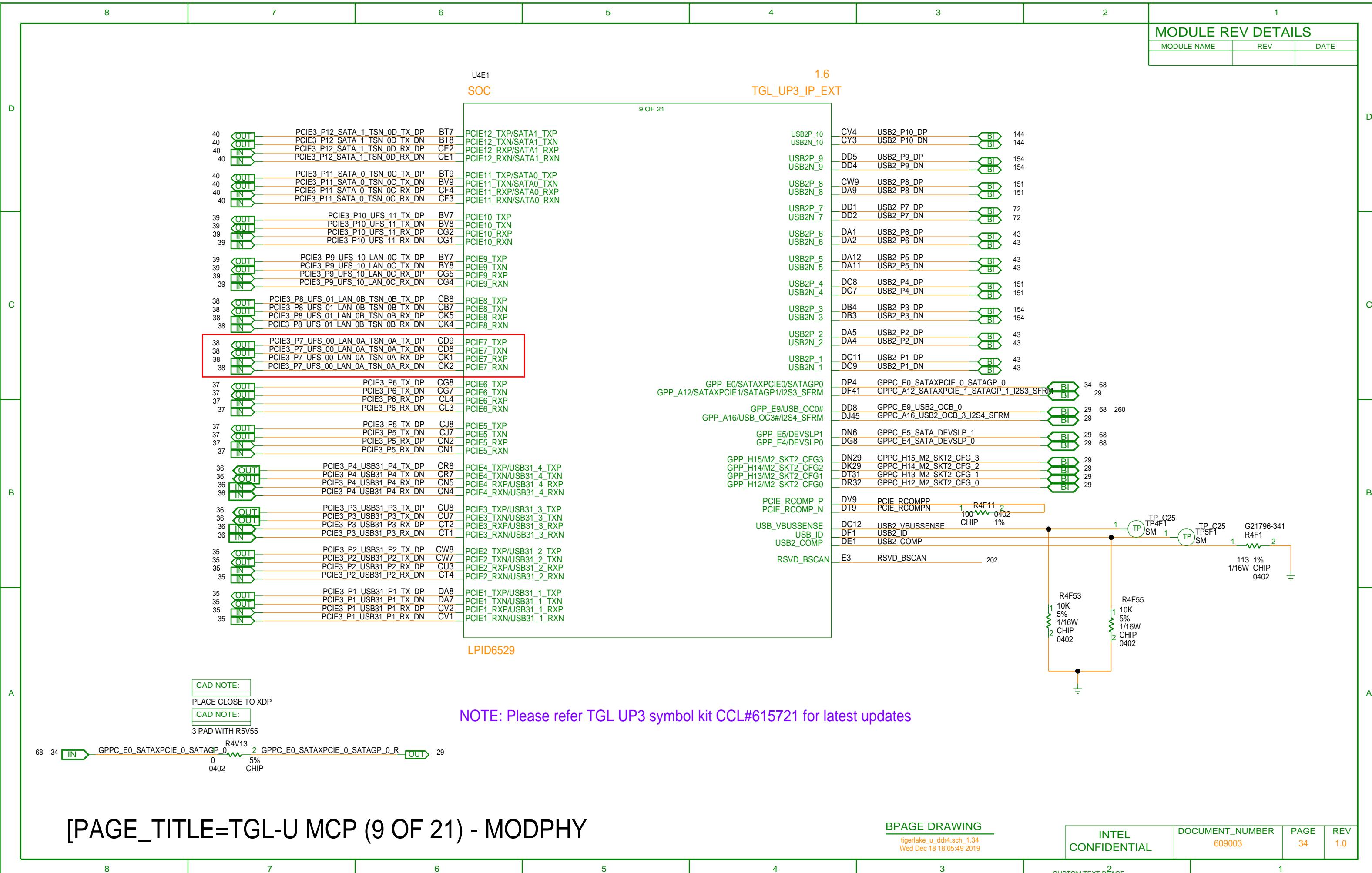
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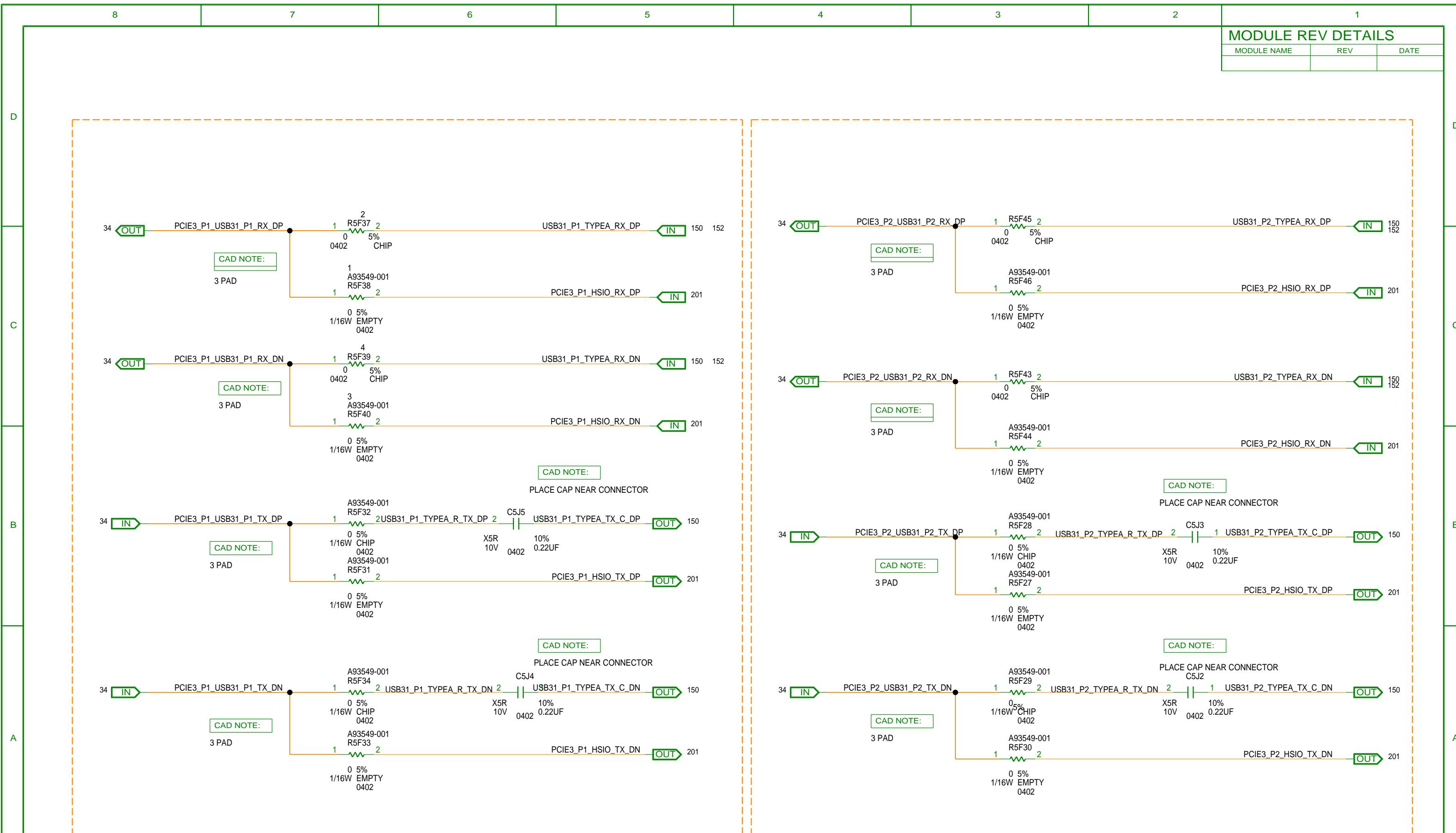
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tigerlake_u_ddr4.sch_1.32
Wed Dec 18 18:05:47 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 32	REV 1.0
CUSTOM TEXT 2 PAGE			

8	7	6	5	4	3	2	1
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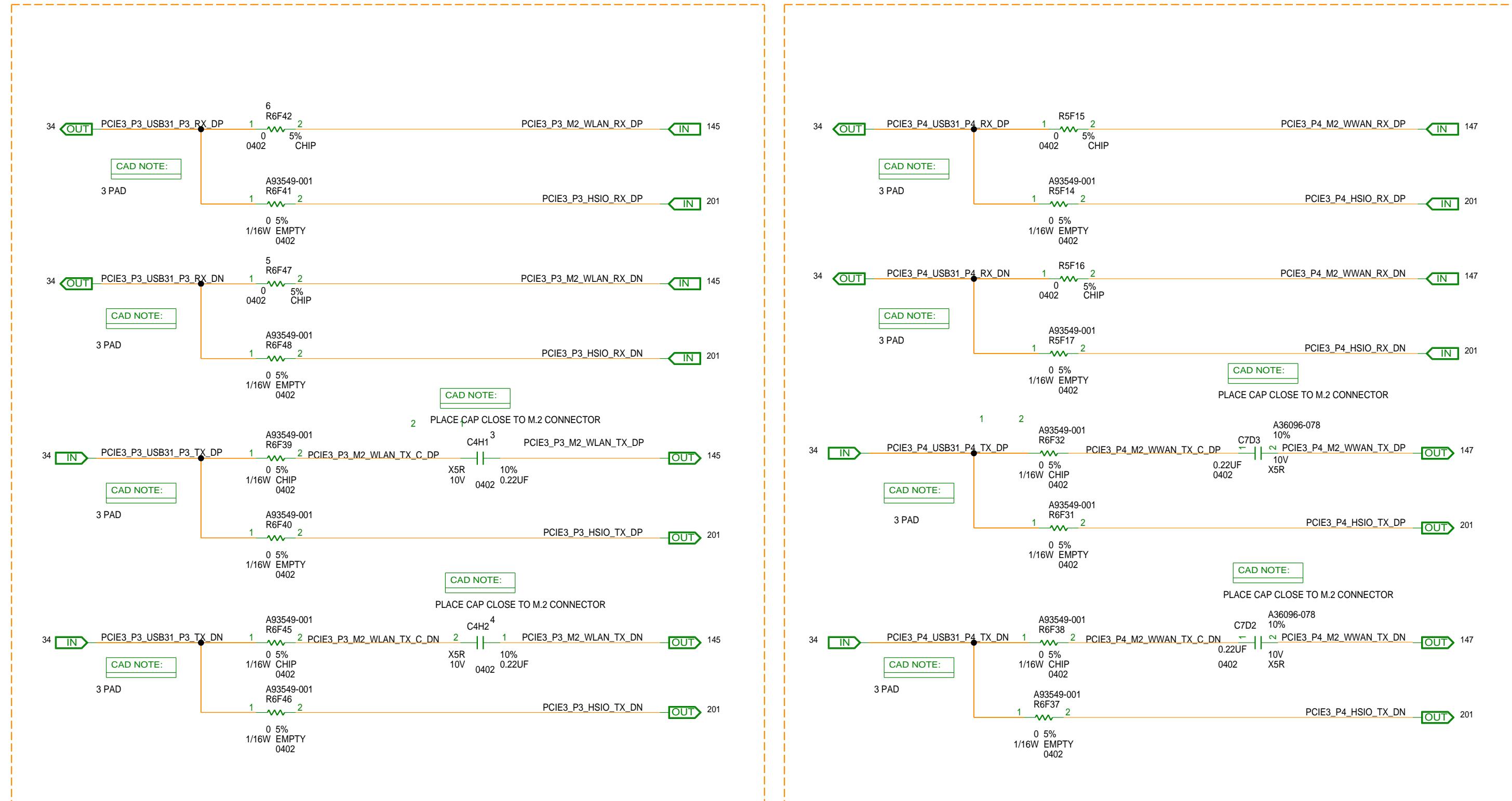


[PAGE_TITLE=PCIE PORT 1&2 SHARING OPTIONS, AC CAPS]

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Wed Dec 18 18:05:50 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 35	REV 1.0
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MODULE REV DETAILS							
MODULE NAME	REV	DATE					



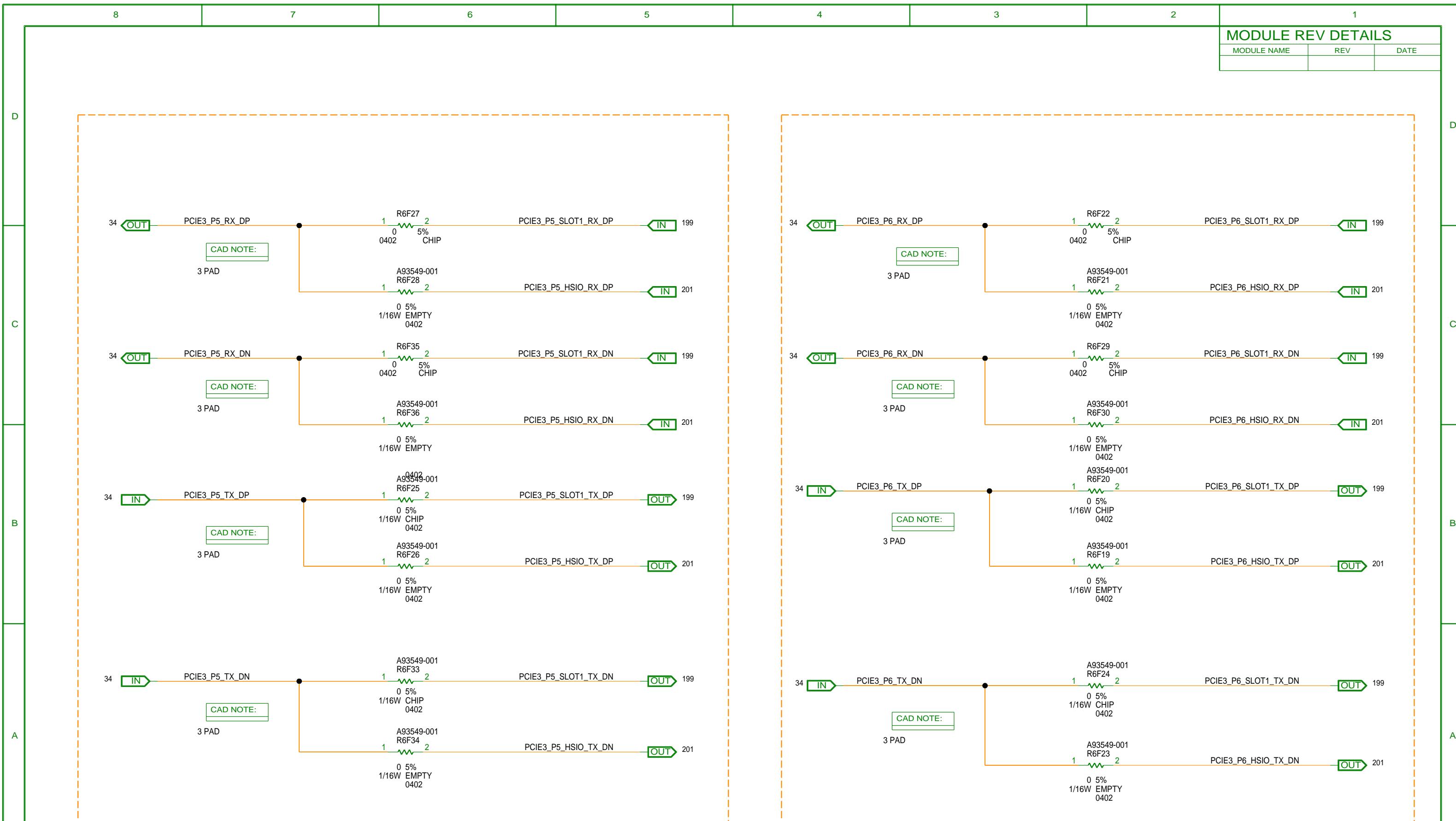
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

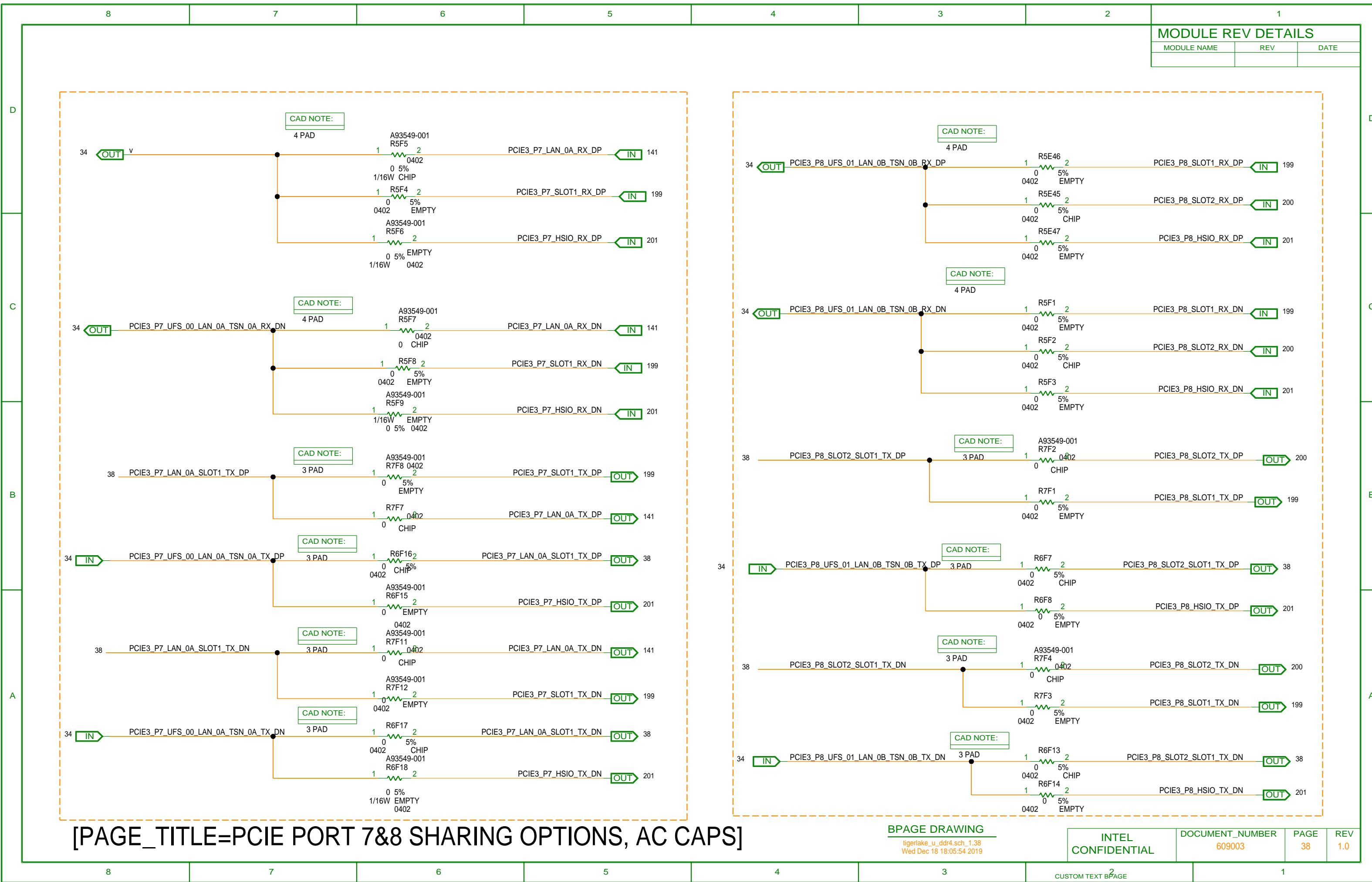
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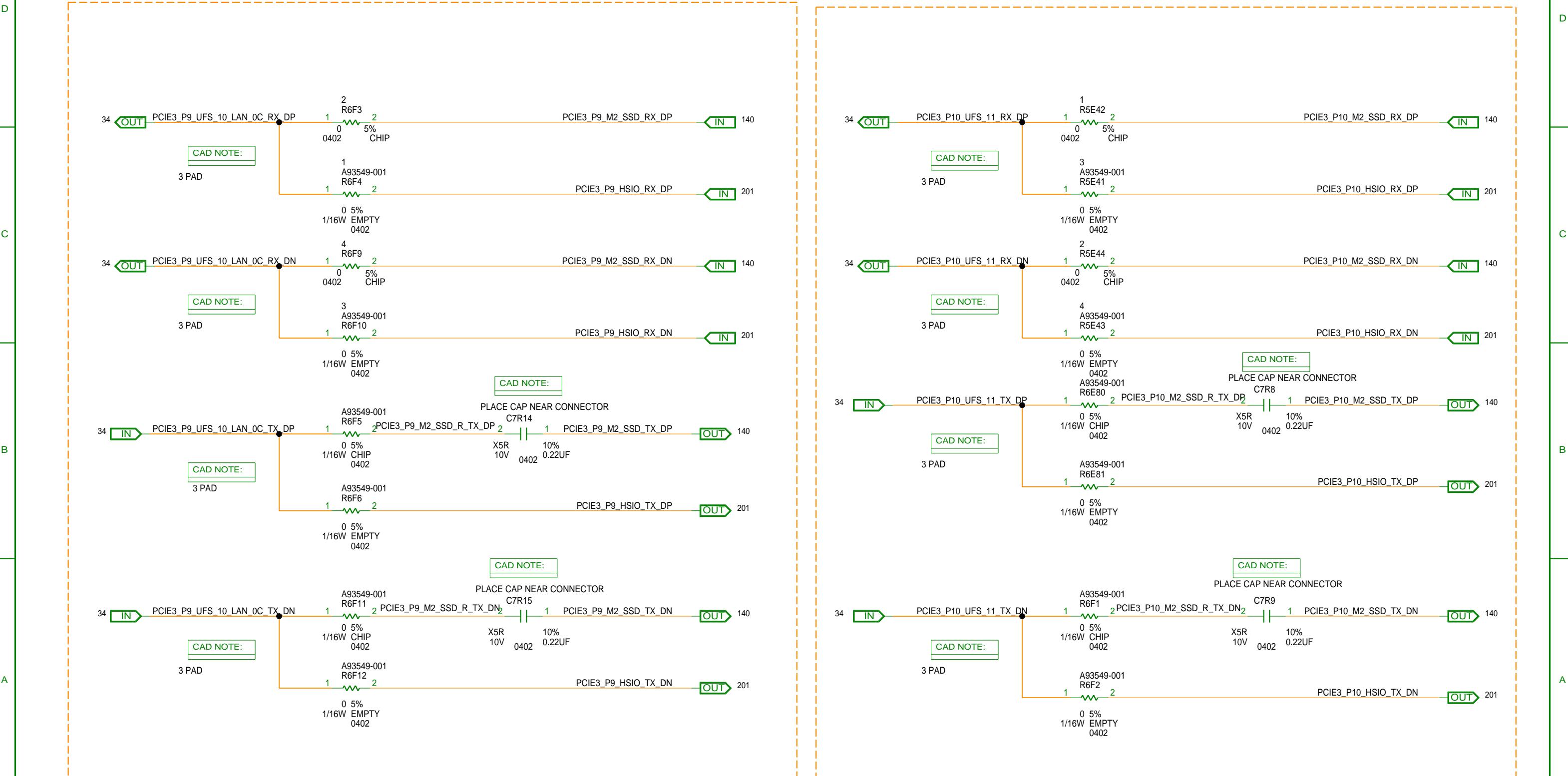
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Wed Dec 18 18:05:52 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 37	REV 1.0
CUSTOM TEXT 2 PAGE			



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MODULE REV DETAILS							
MODULE NAME	REV	DATE					



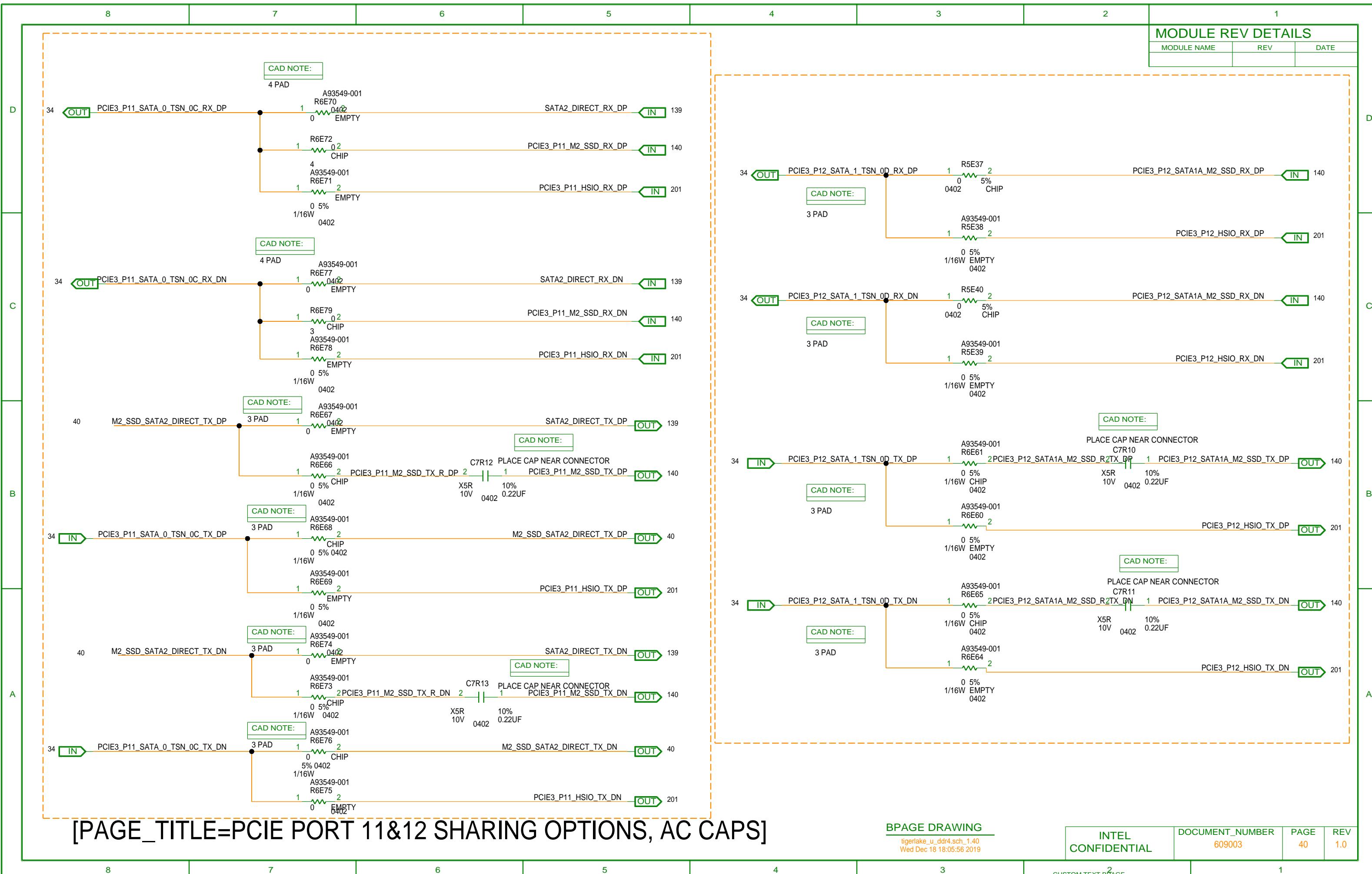
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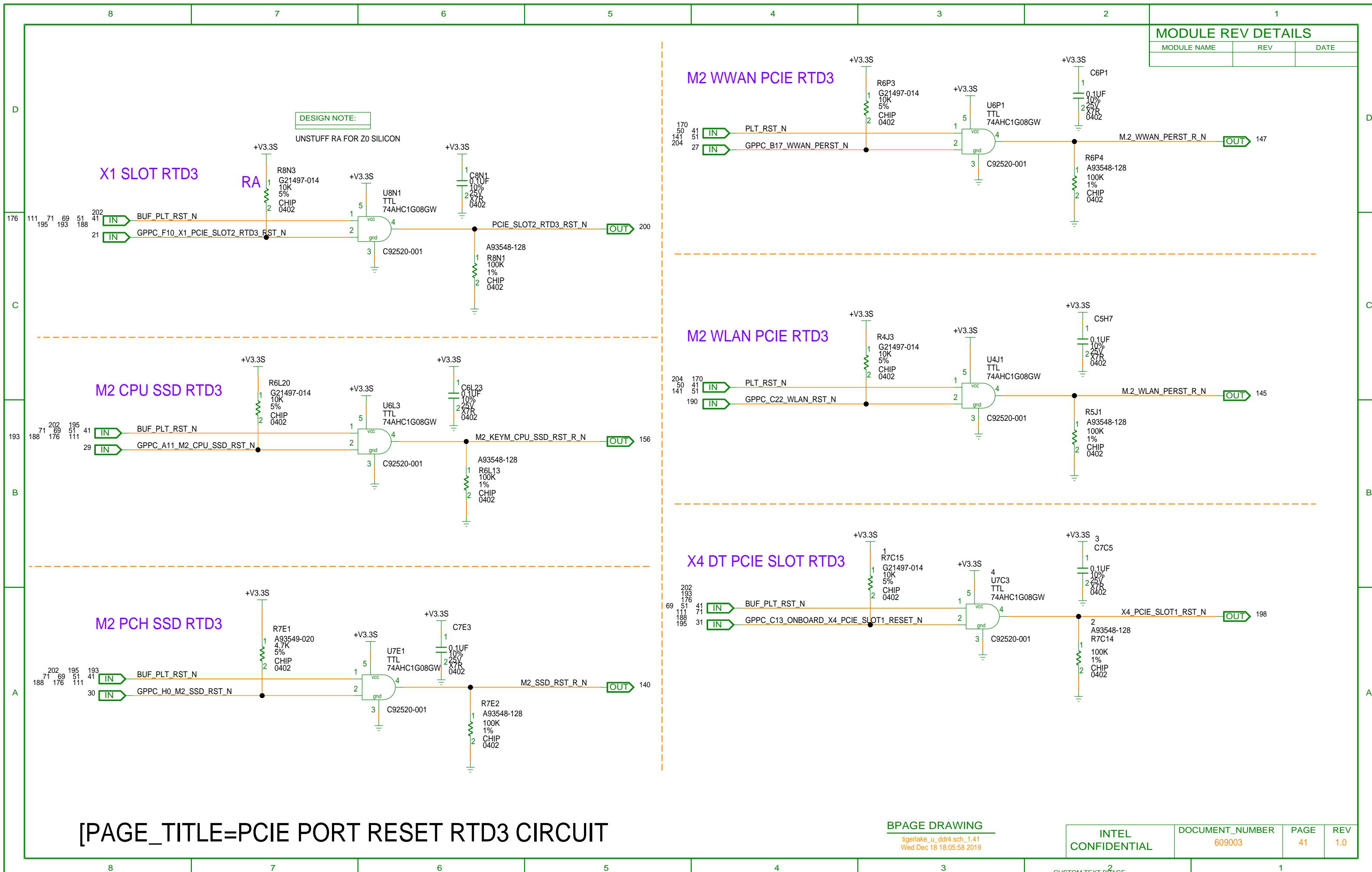
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Wed Dec 18 18:05:55 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	39	1	1.0

CUSTOM TEXT BPAGE

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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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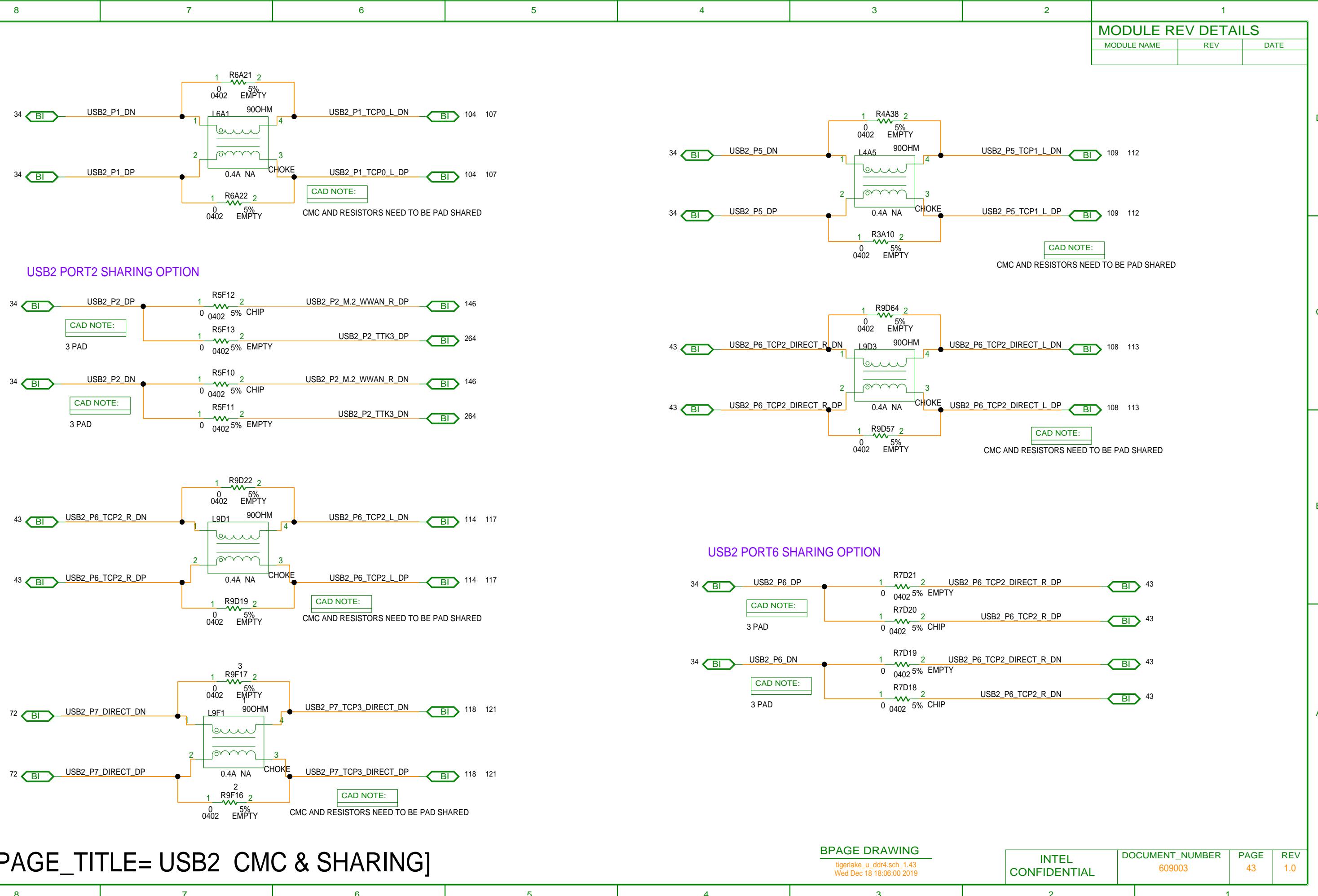
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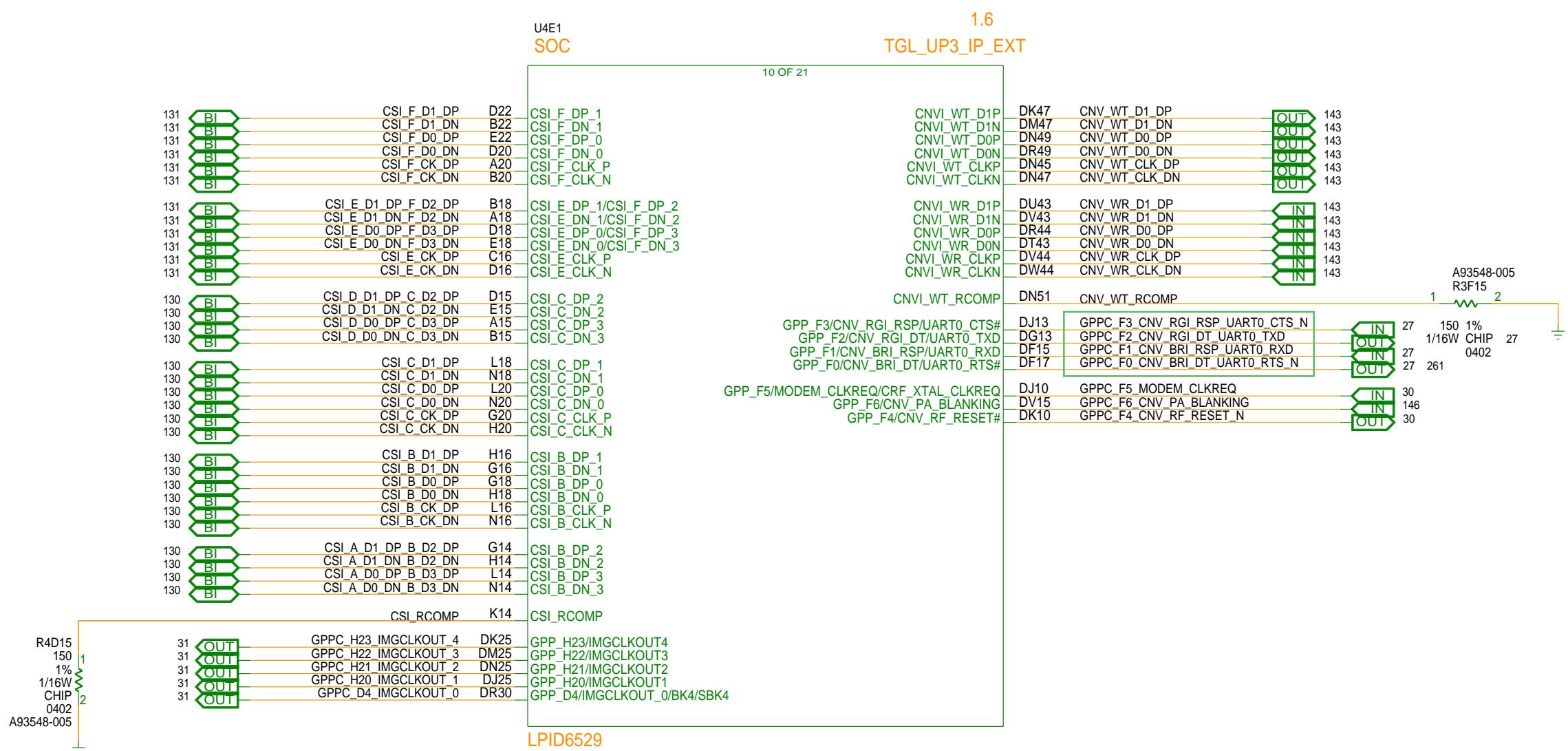
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 42	REV 1.0
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8	7	6	5	4	3	CUSTOM TEXT ² PAGE	1
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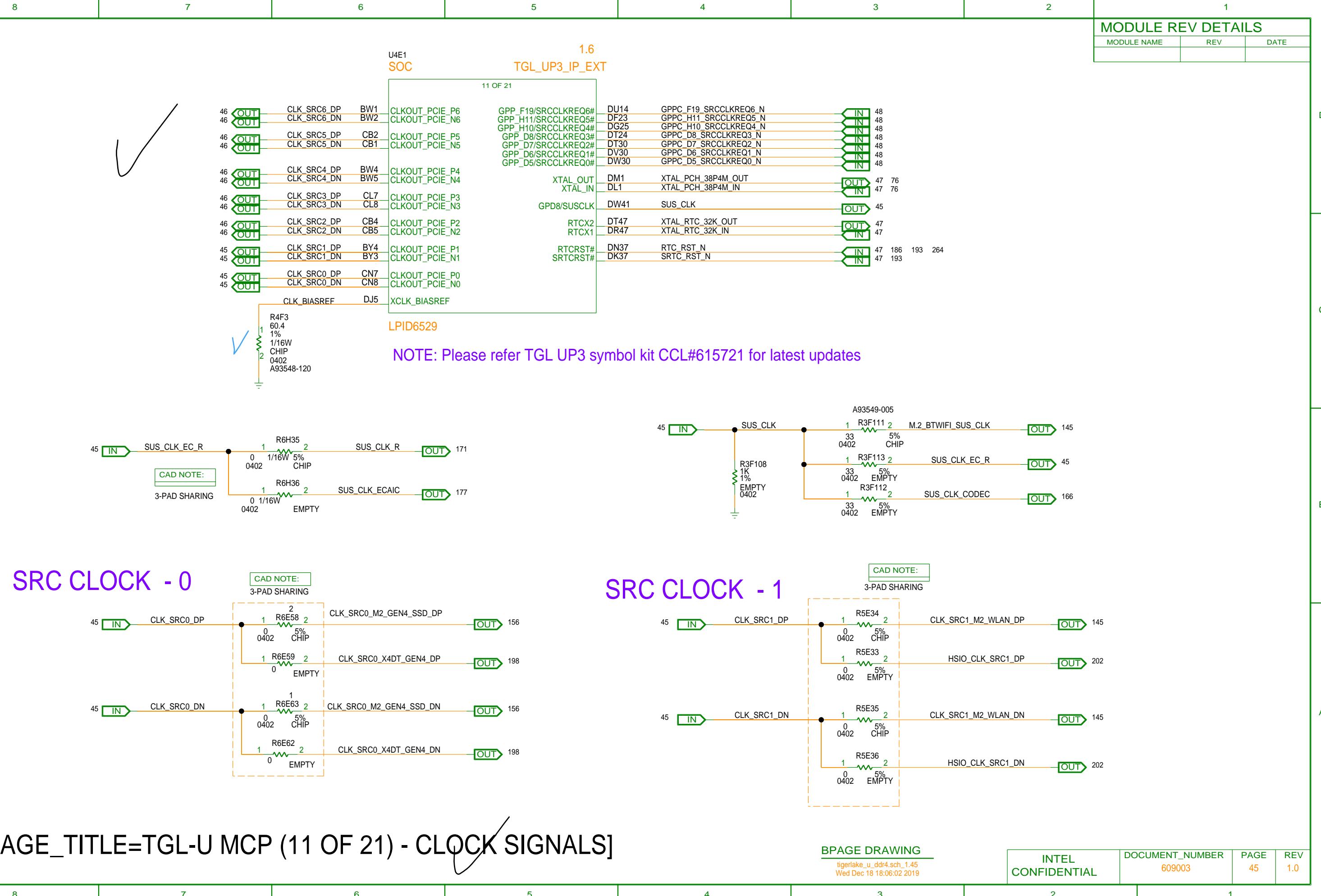


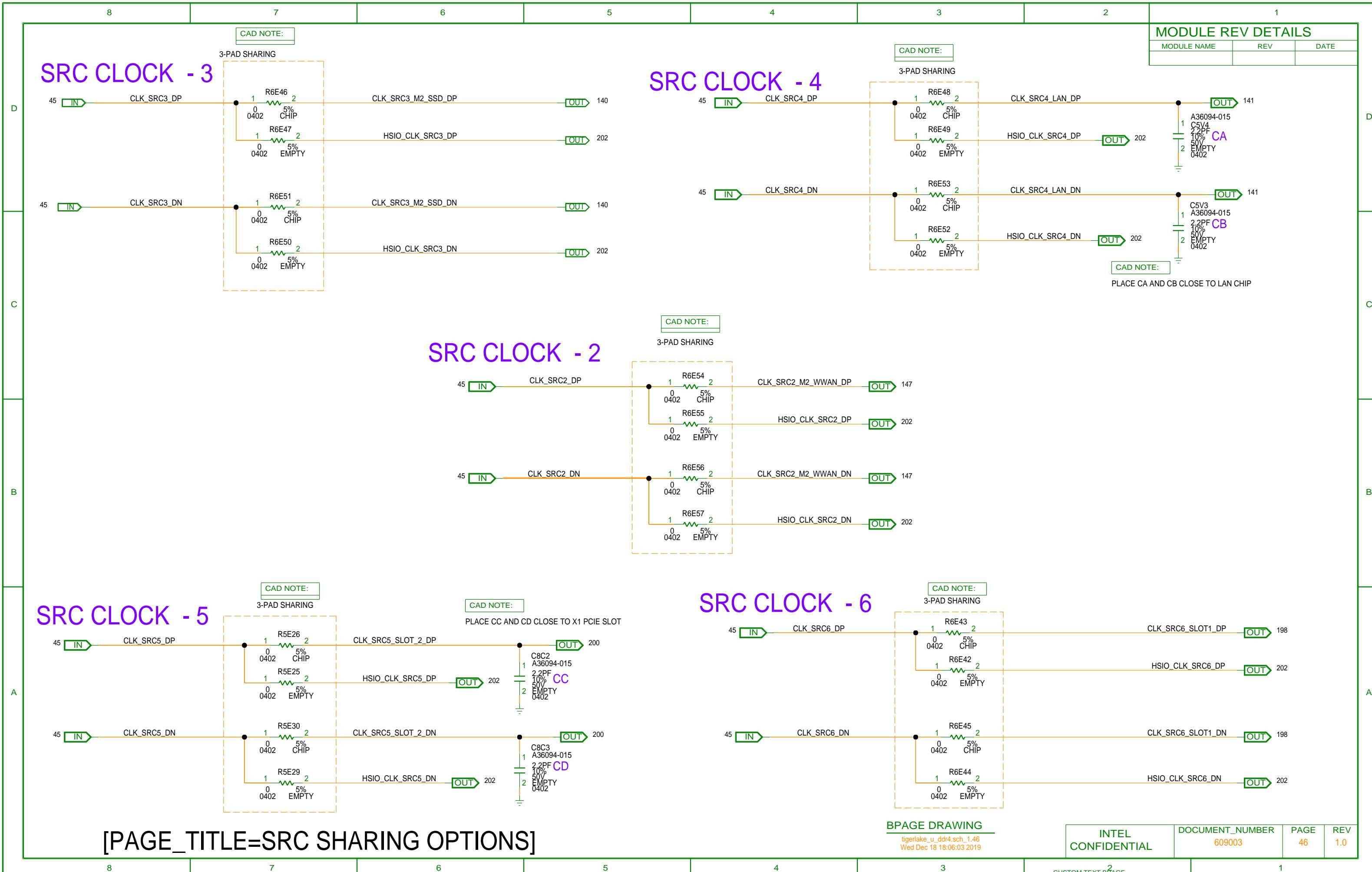
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MODULE REV DETAILS							

DIDNT IMPLEMENT YET



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates





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MODULE REV DETAILS

MODULE NAME	REV	DATE

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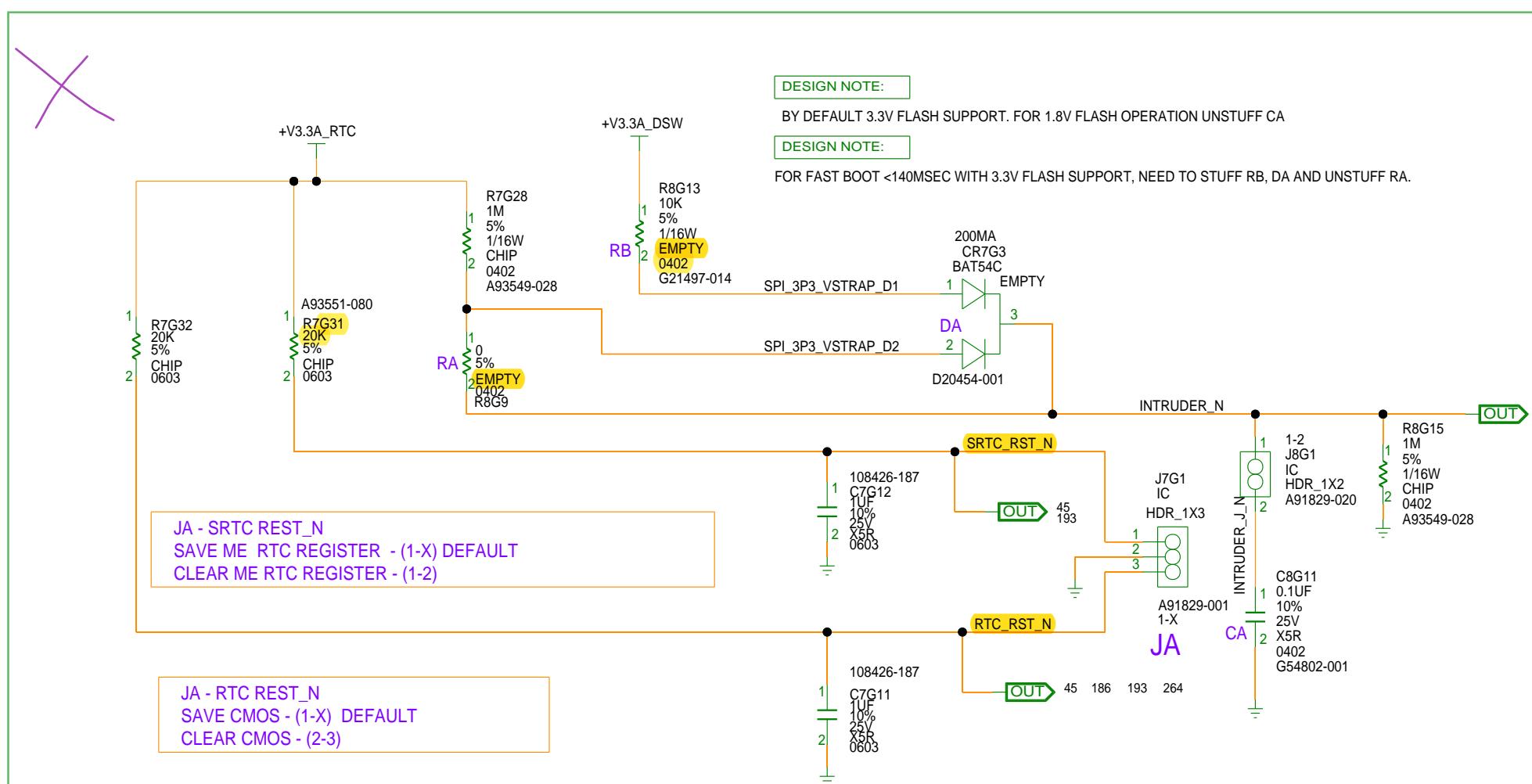
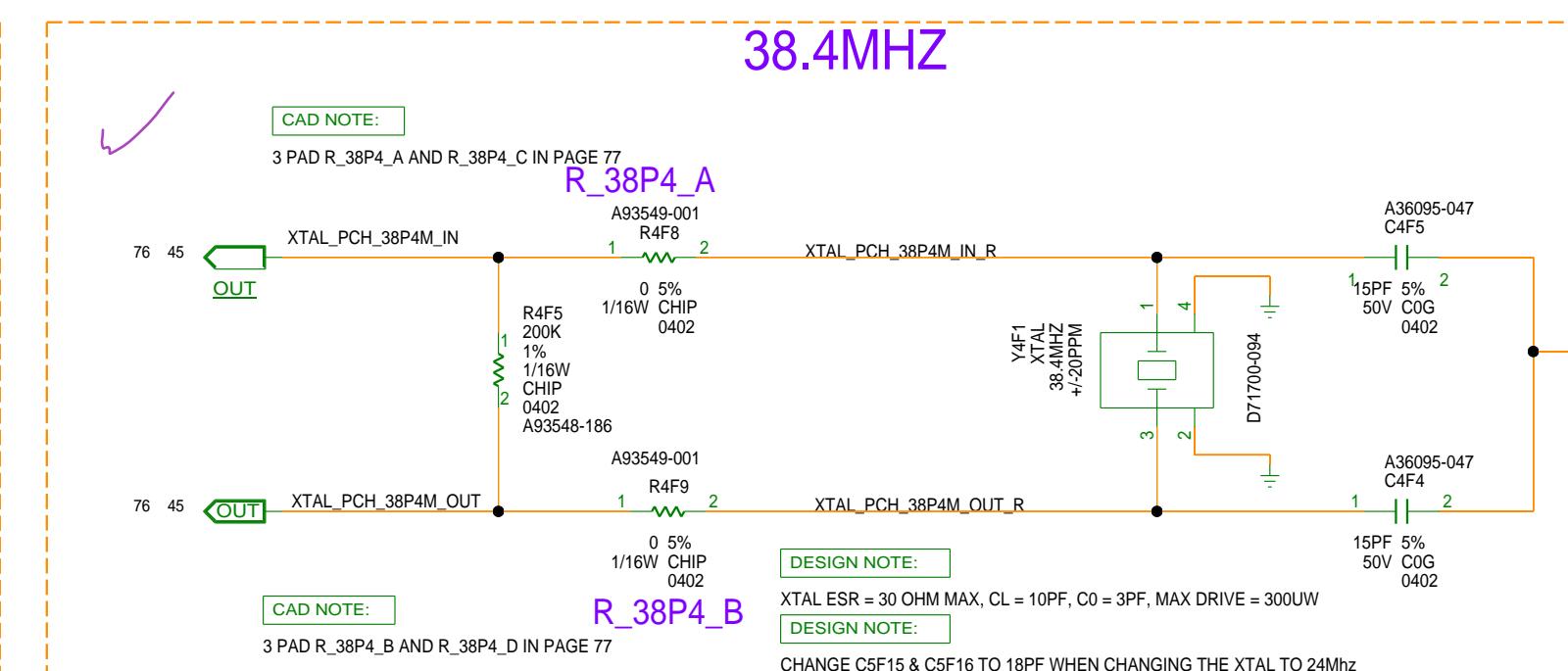
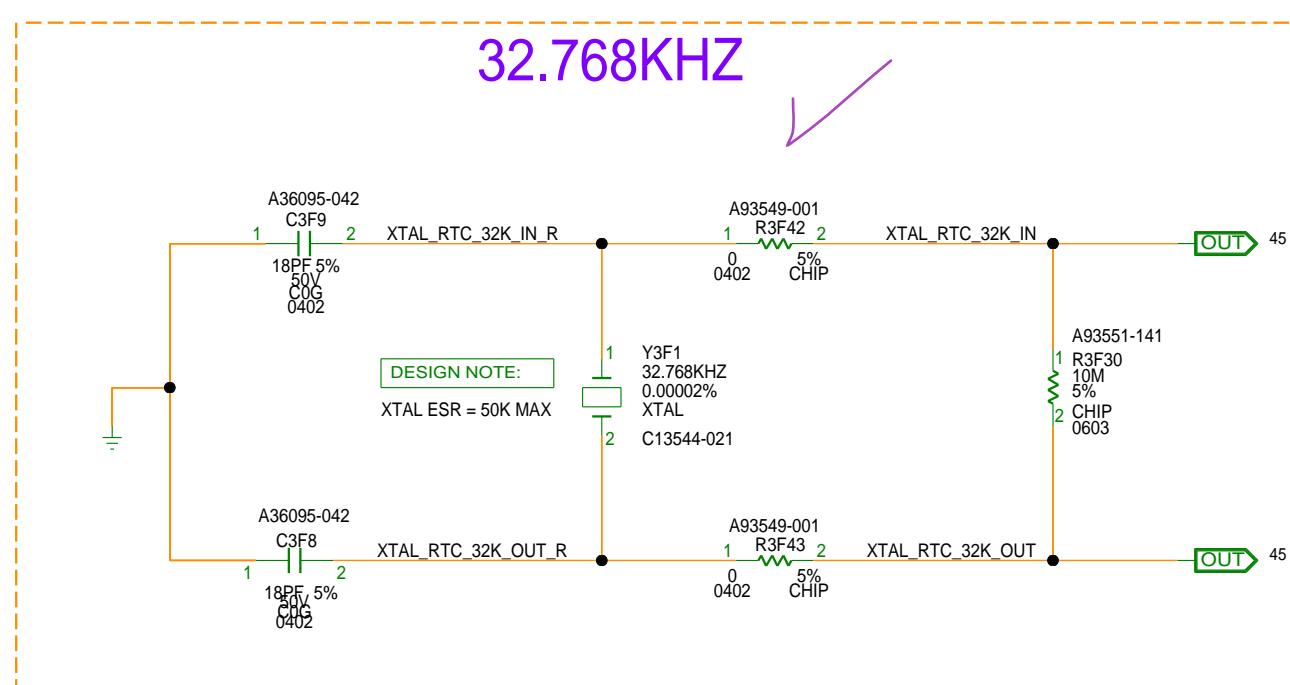
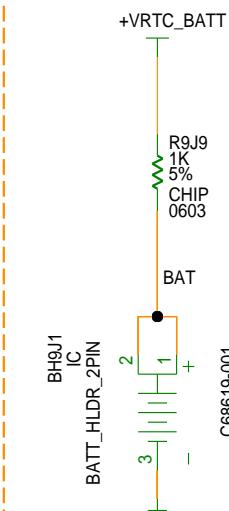
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**+V3.3A_RTC GENERATION**

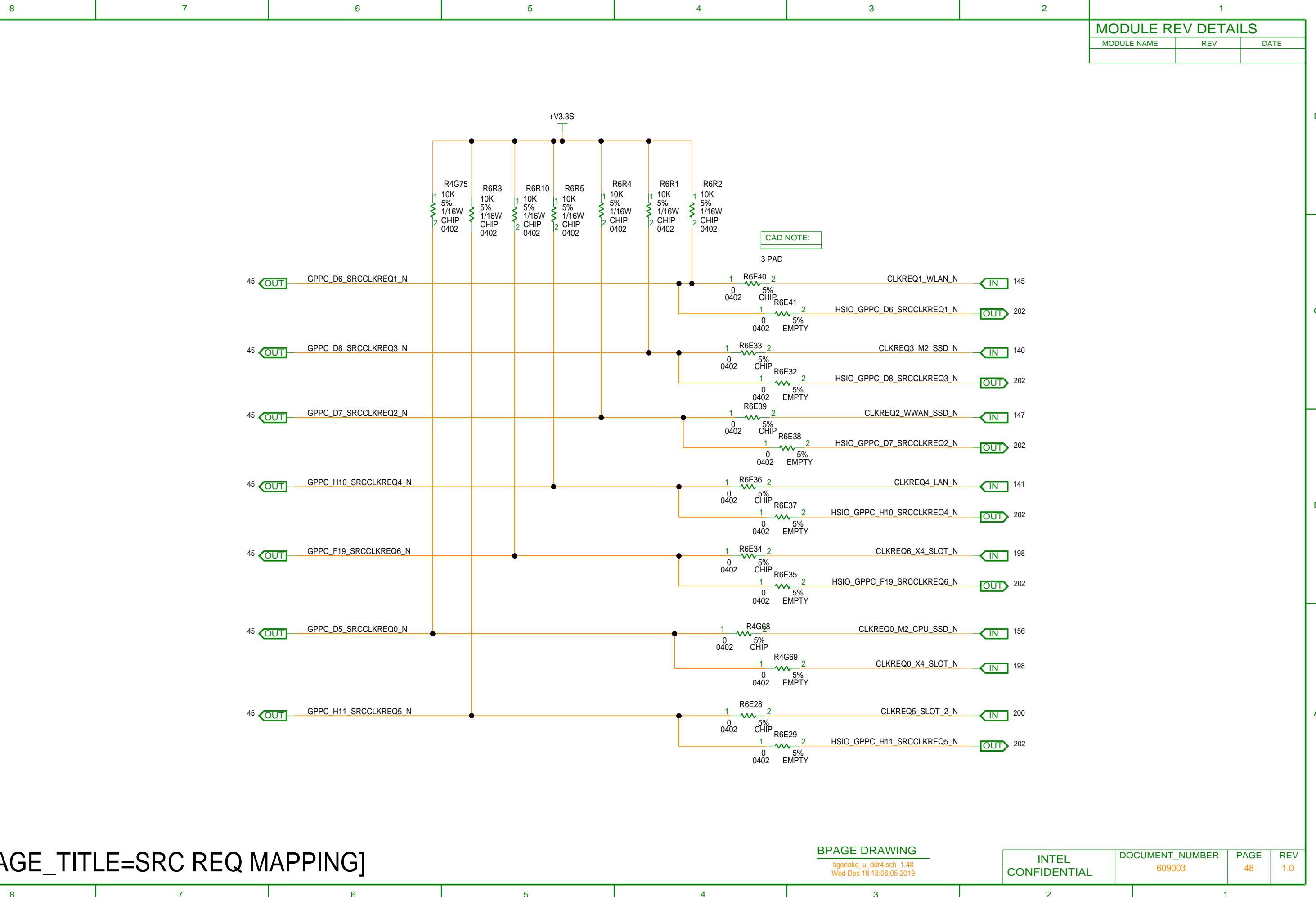
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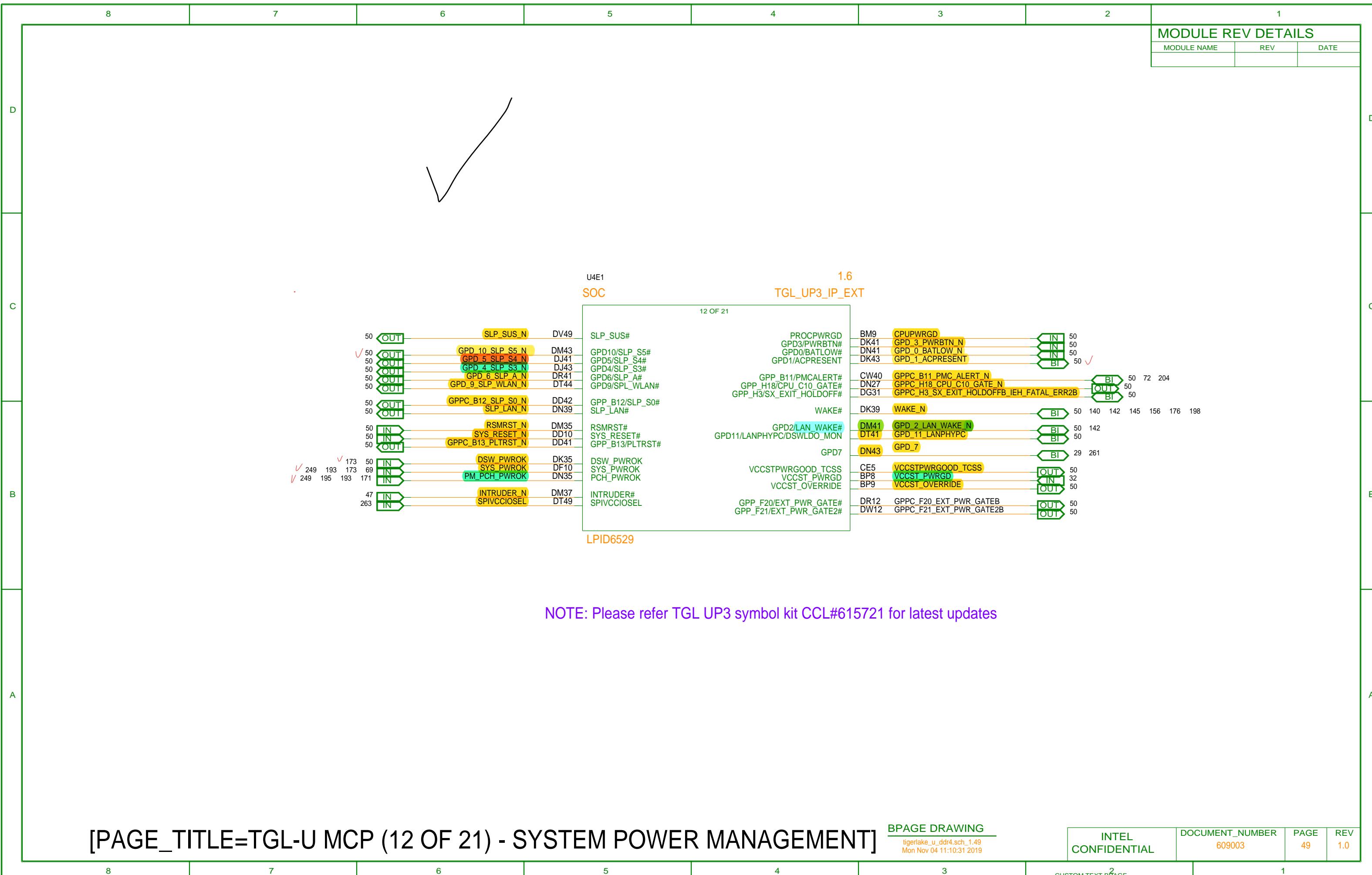
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Wed Dec 18 18:06:04 2019

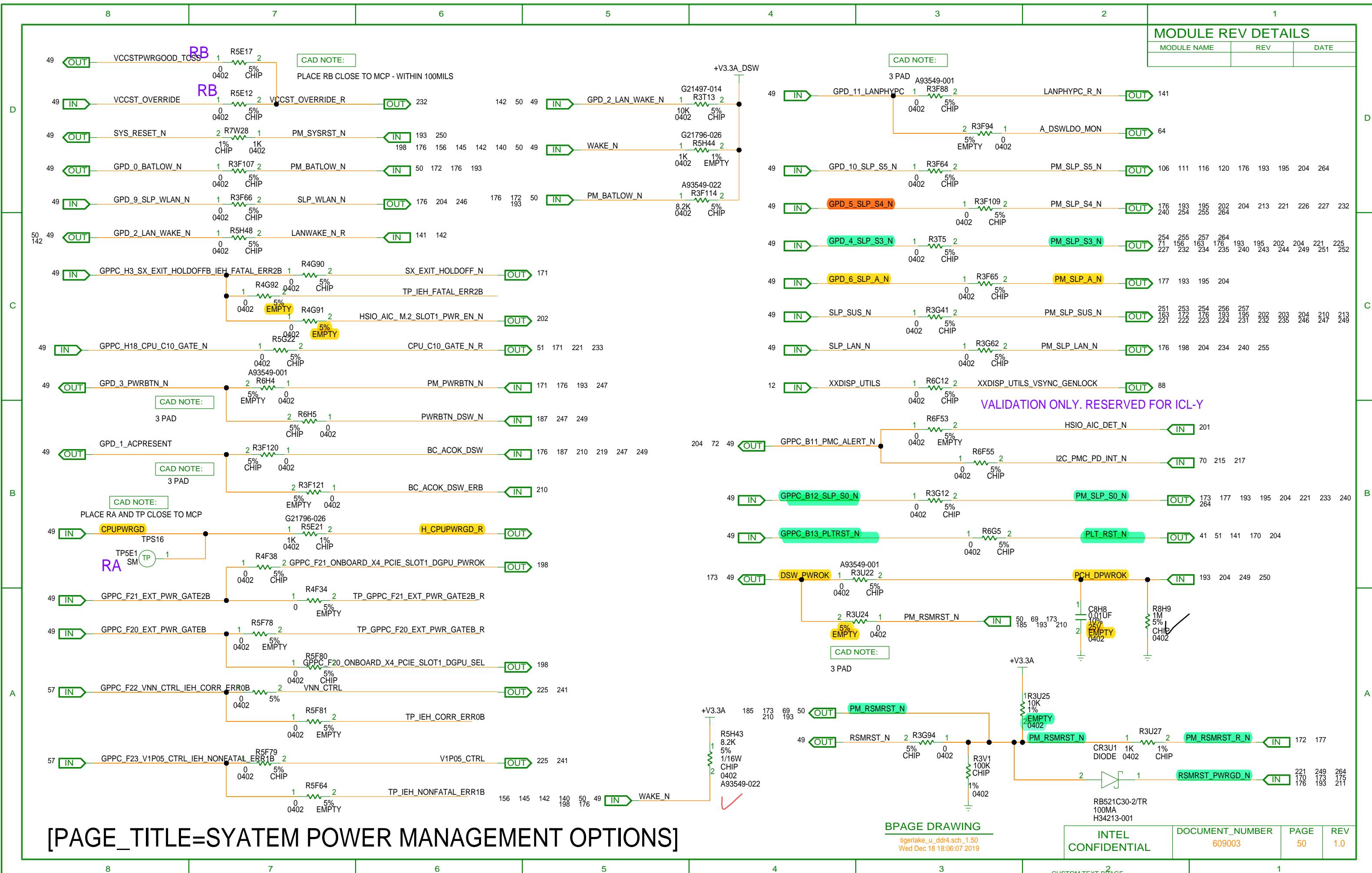
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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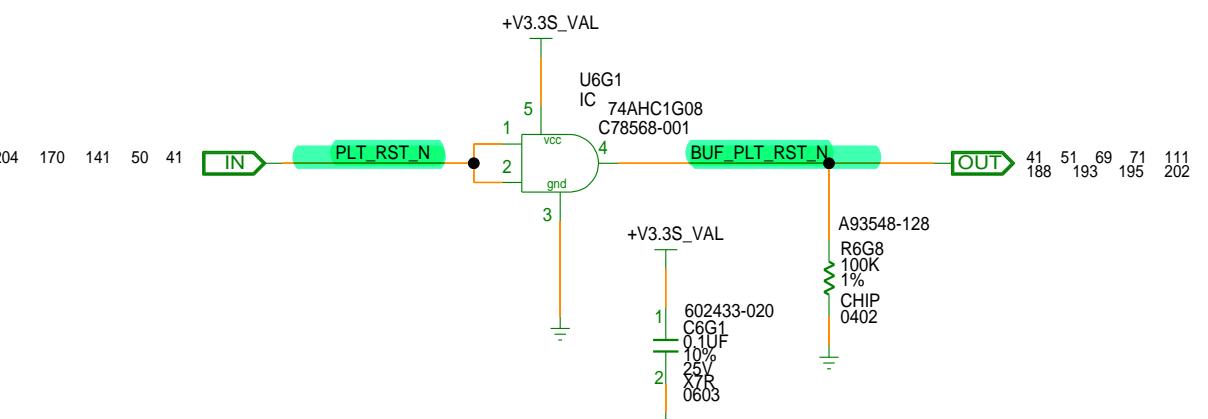




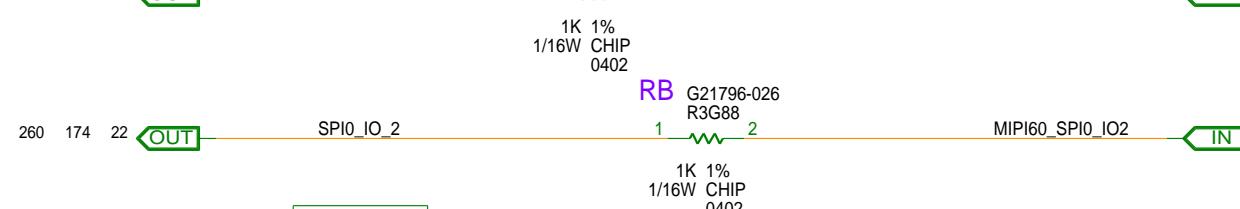
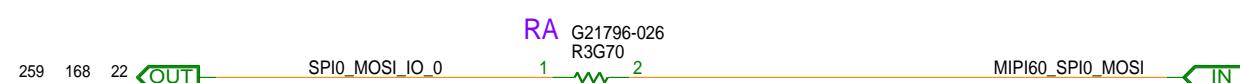
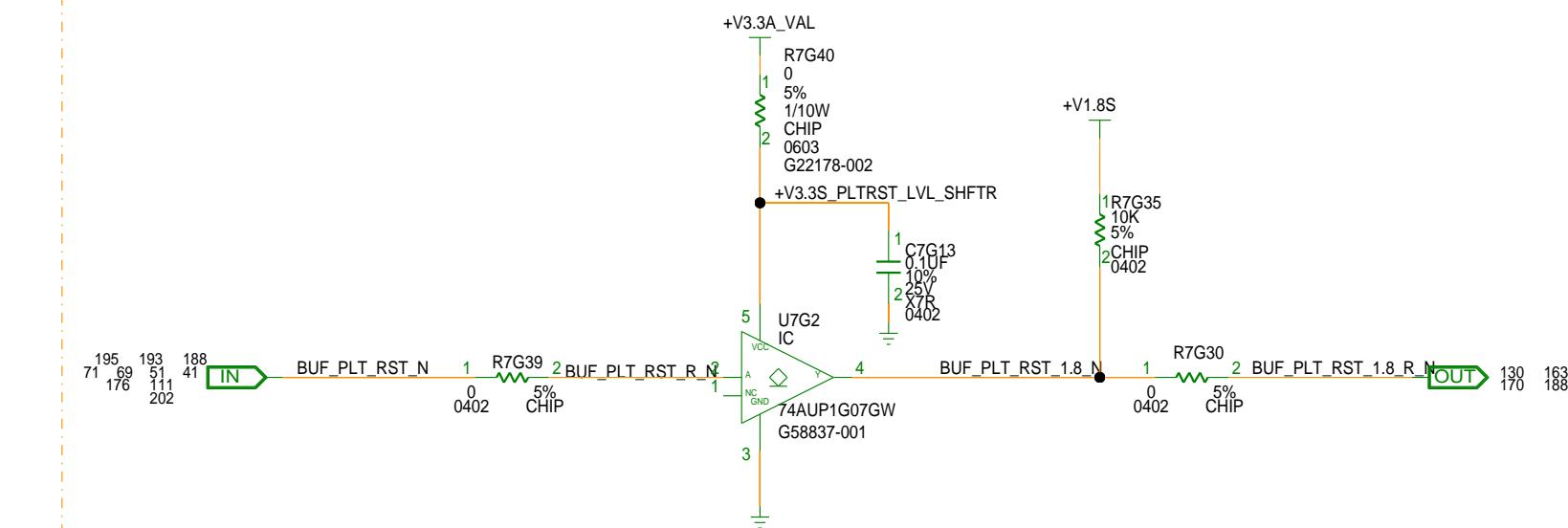


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MODULE REV DETAILS							

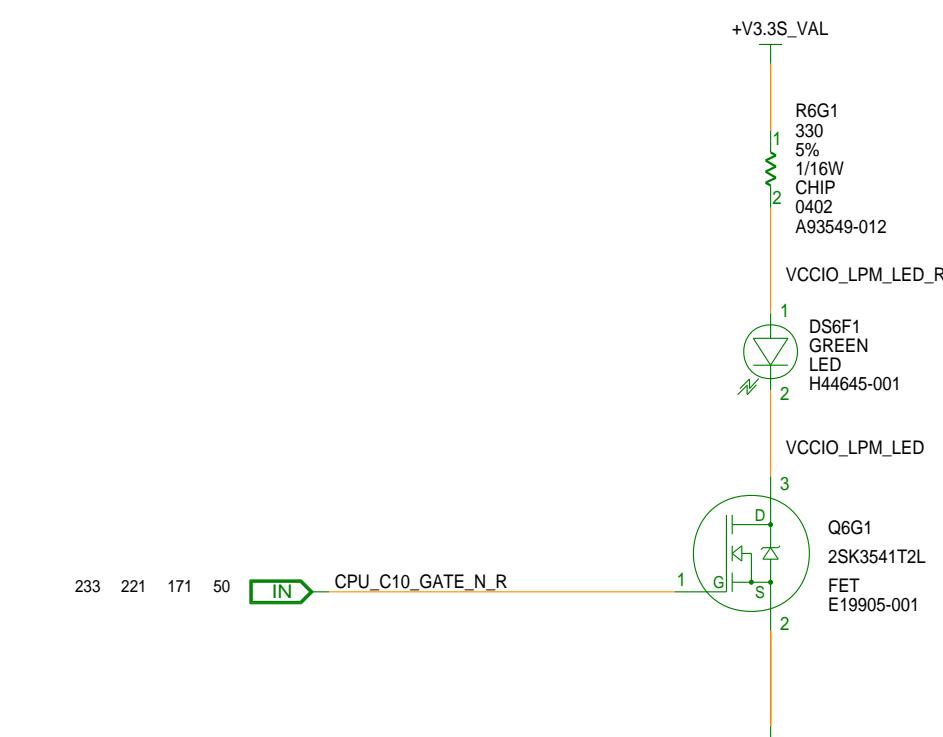
BUFFER TO REDUCE LOADING ON PLT_RST_N



PLATFORM RESET LEVEL SHIFTER - 3.3V TO 1.8V



CAD NOTE:
RA AND RB RESISTORS NEED TO BE PLACED NEAR TO MCP, WITHOUT STUB ON SPI



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MODULE REV DETAILS

MODULE NAME	REV	DATE

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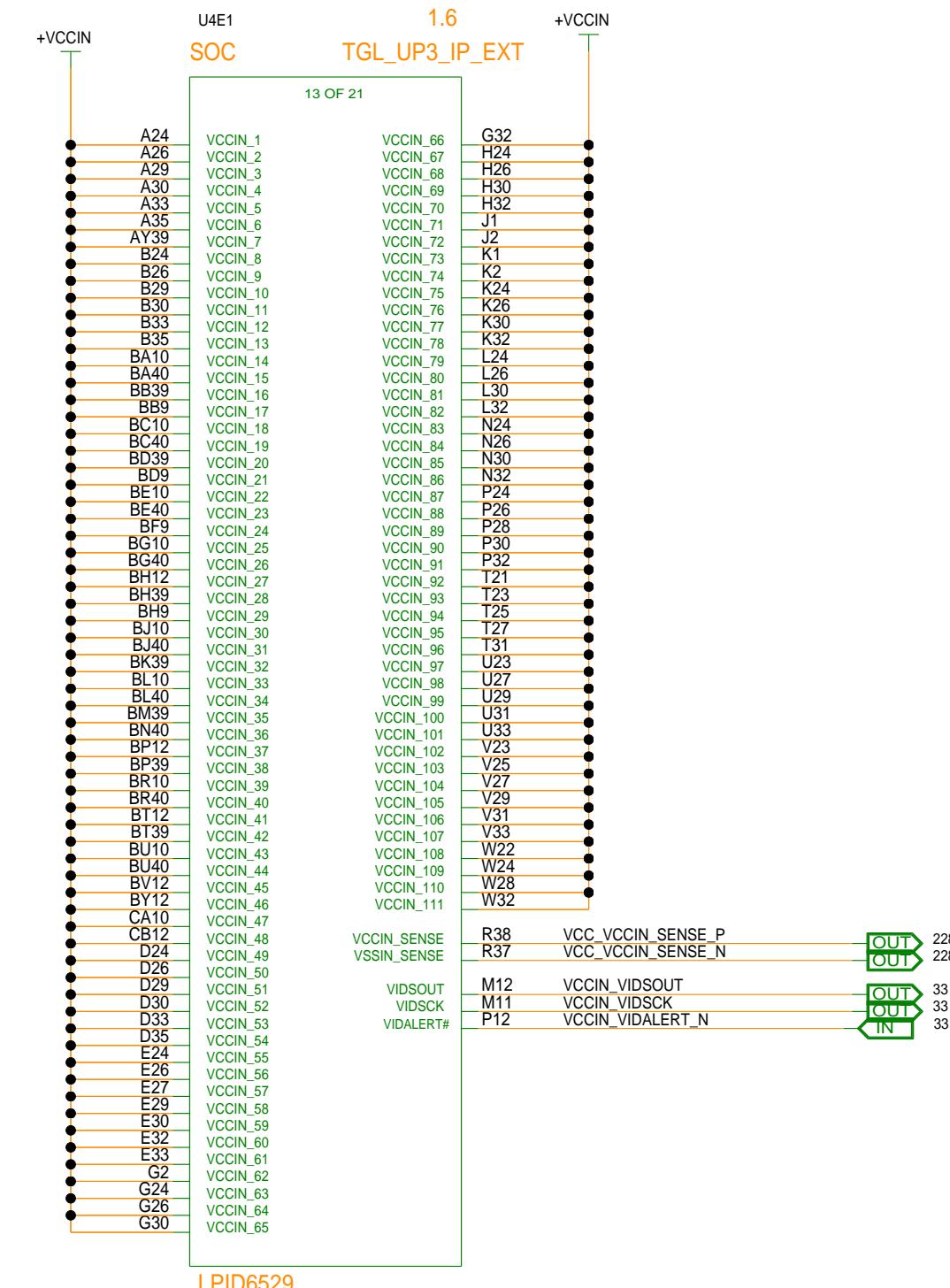
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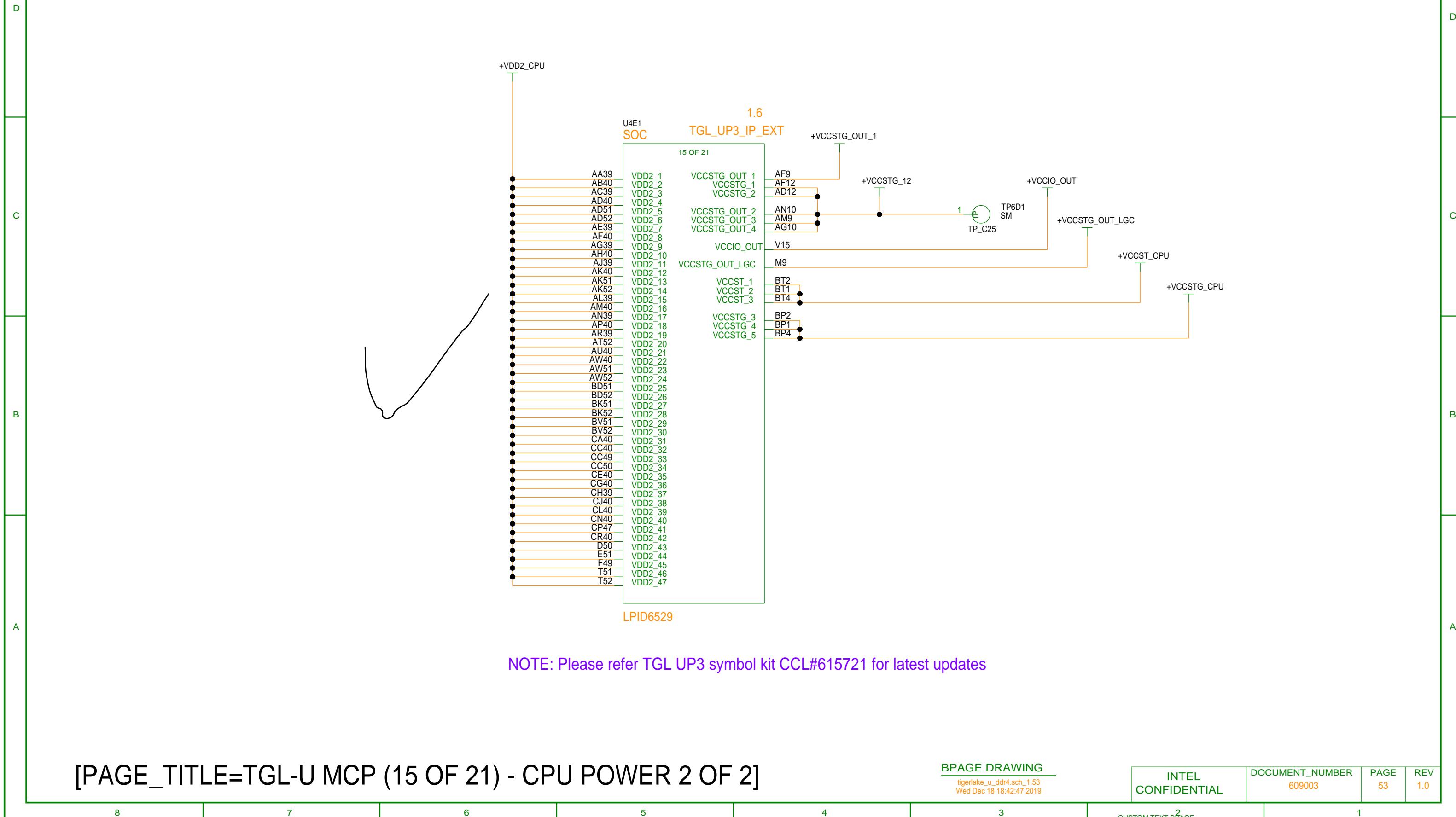
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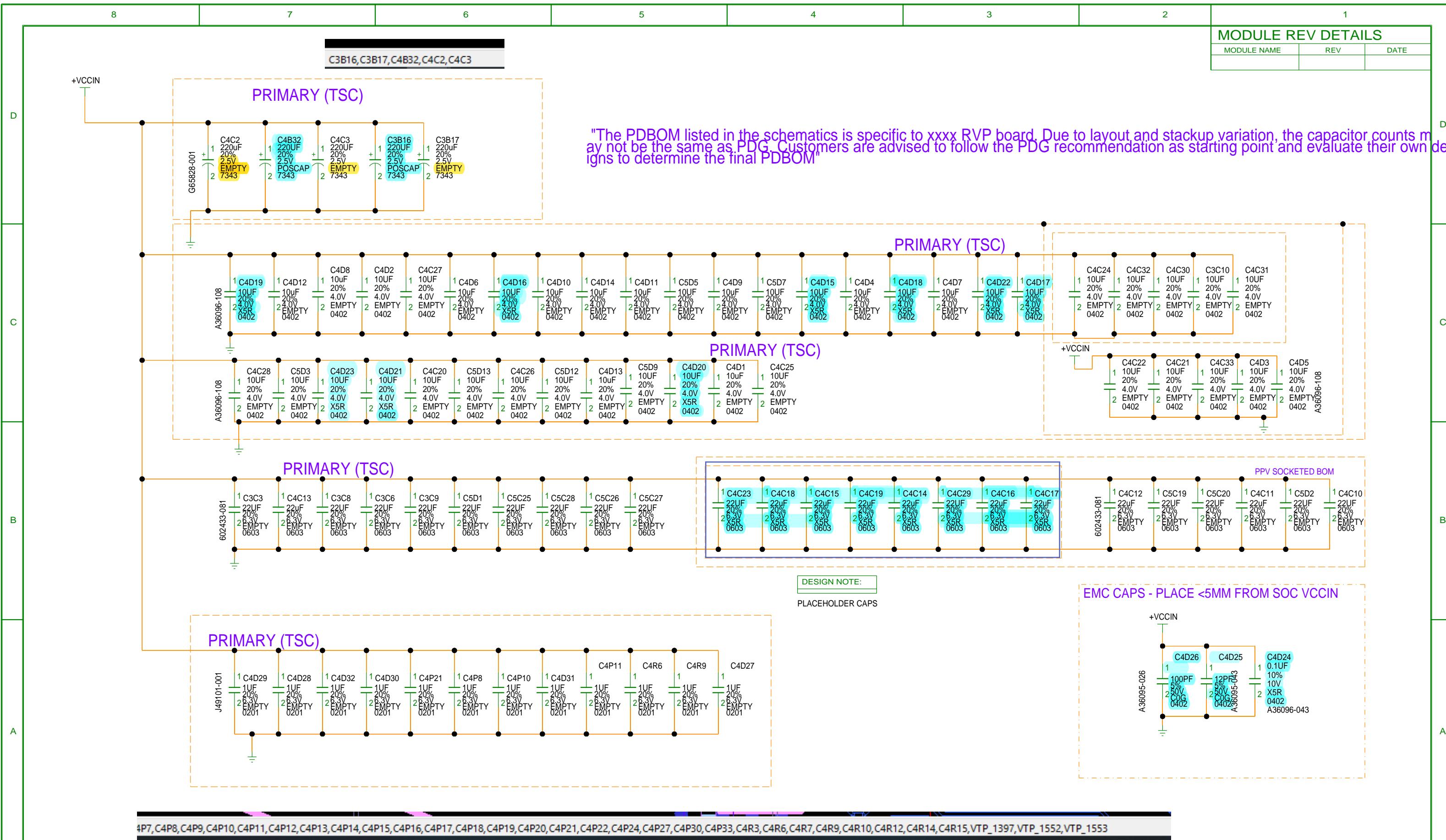
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NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				



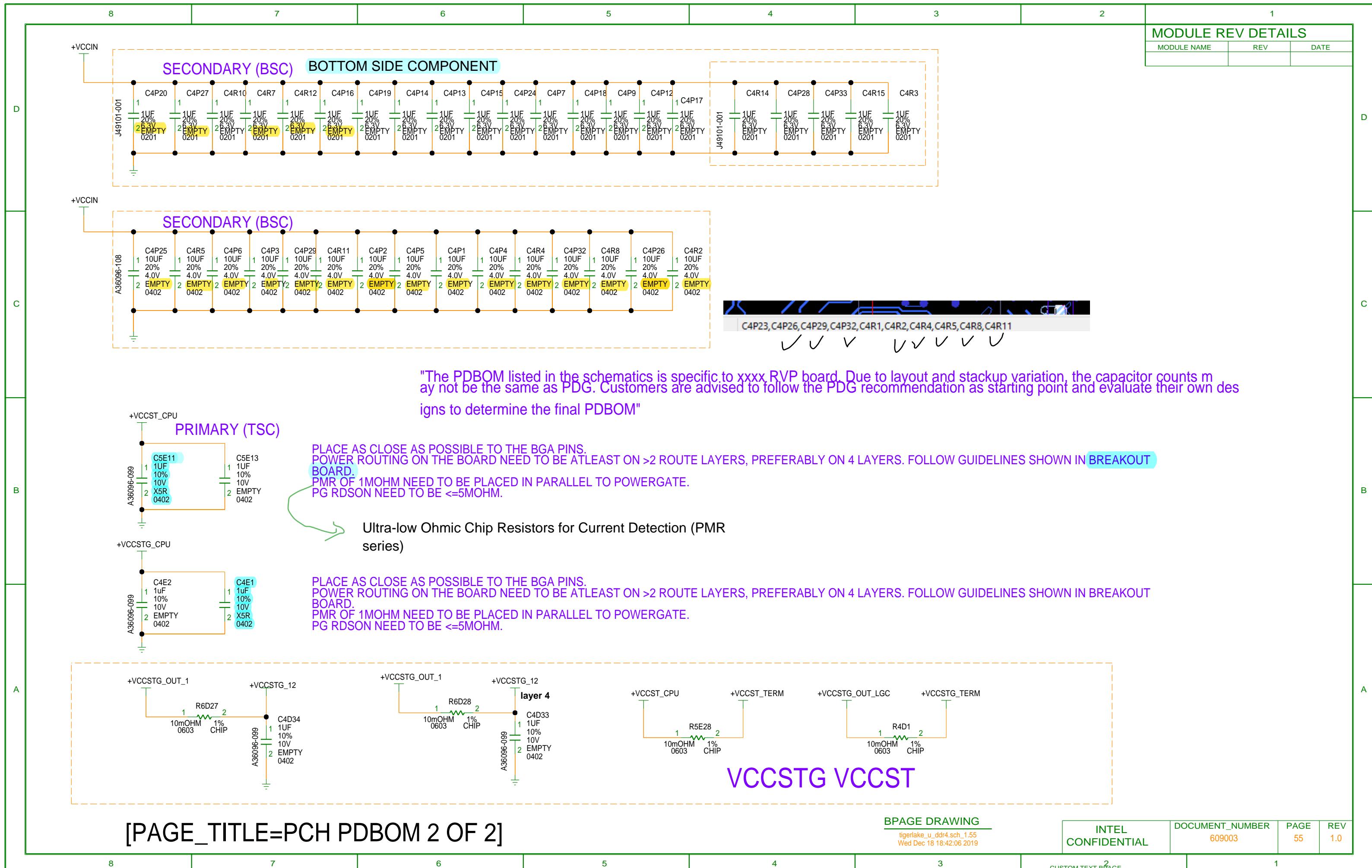


[PAGE_TITLE=CPU PDBOM 1 OF 2]

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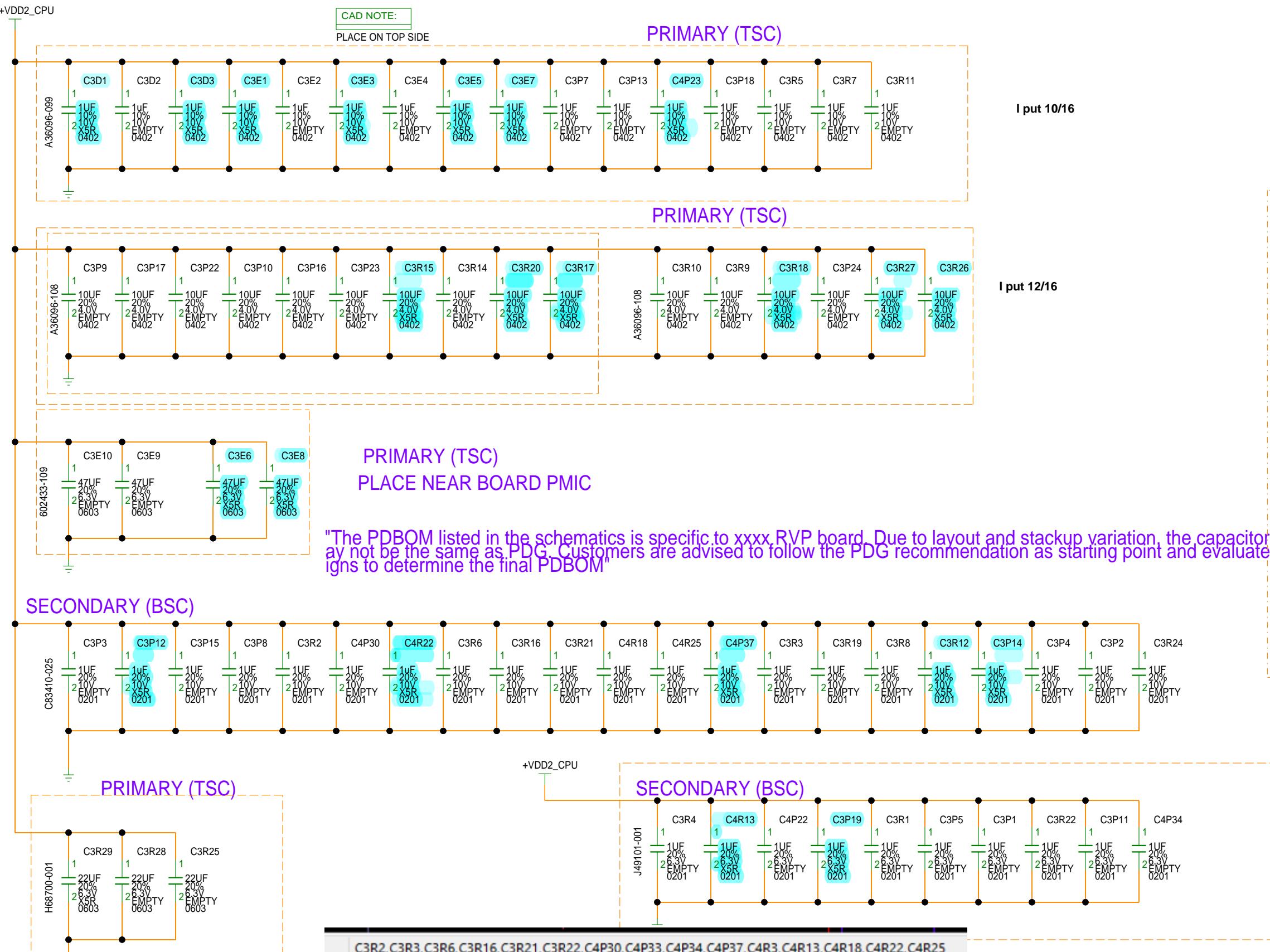
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 54	REV 1.0
2		1	



VDD2

MODULE REV DETAILS		
MODULE NAME	REV	DATE

EMC CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART



[PAGE_TITLE=CPU PDBOM 2 OF 2]

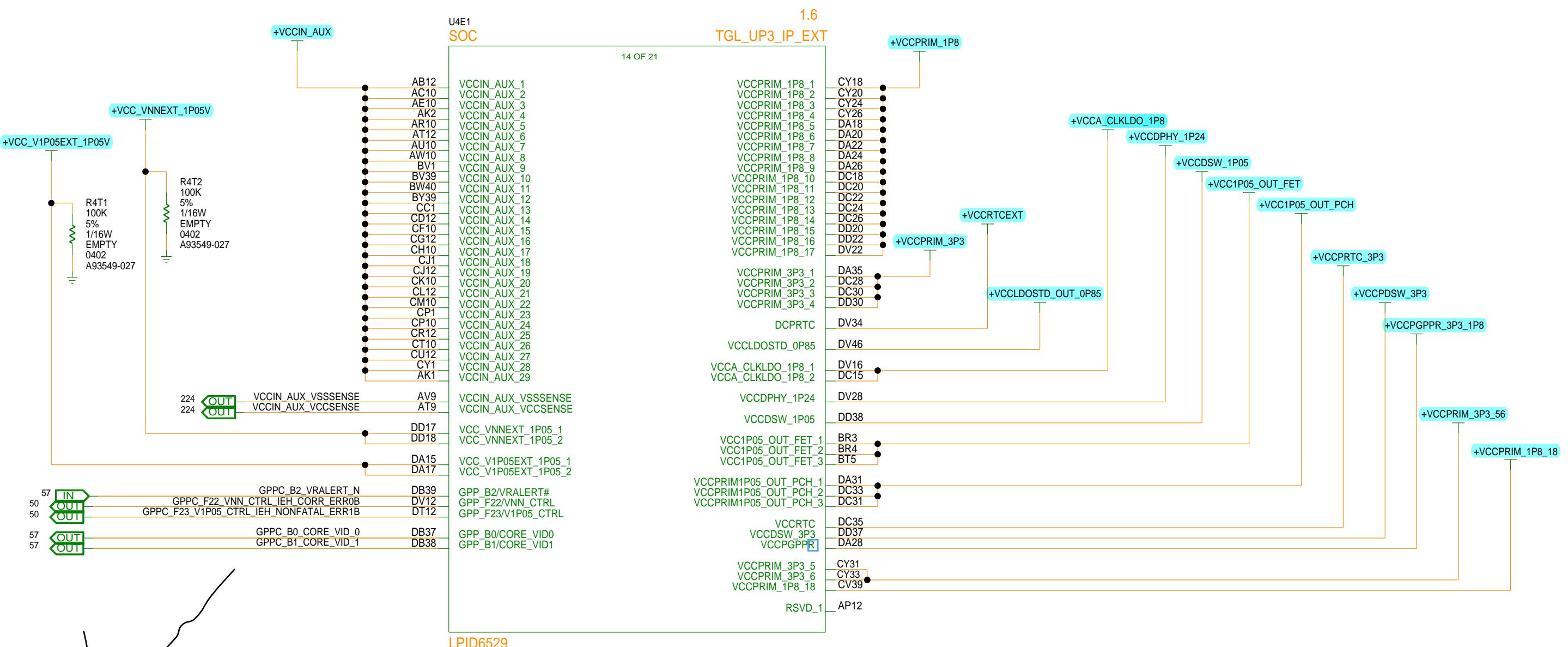
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

8 7 6 5 4 3 2 1

8	7	6	5	4	3	2	1
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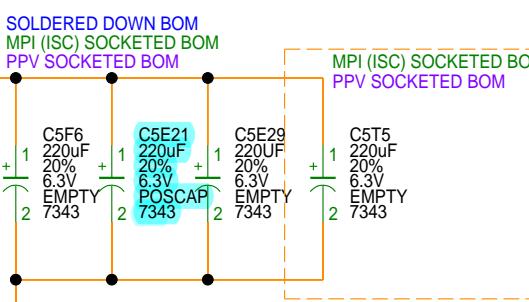


VCCIN_AUX_1P8

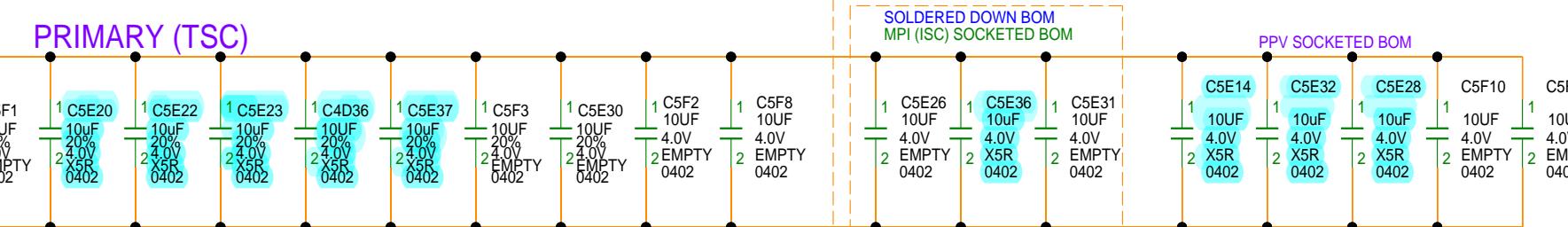
MODULE REV DETAILS

MODULE NAME	REV	DATE

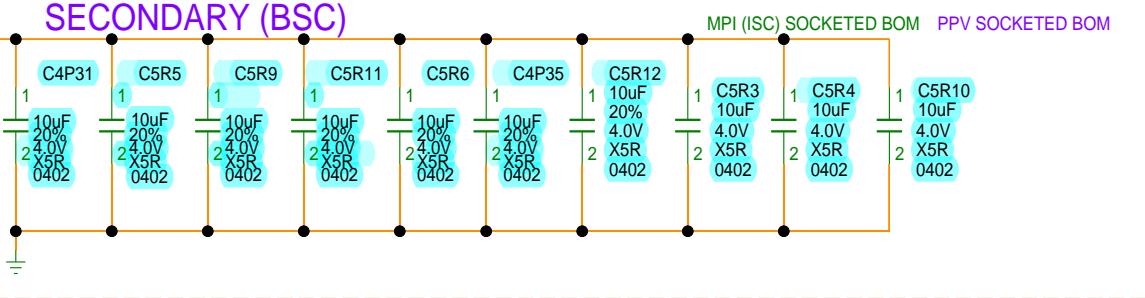
PRIMARY (TSC)



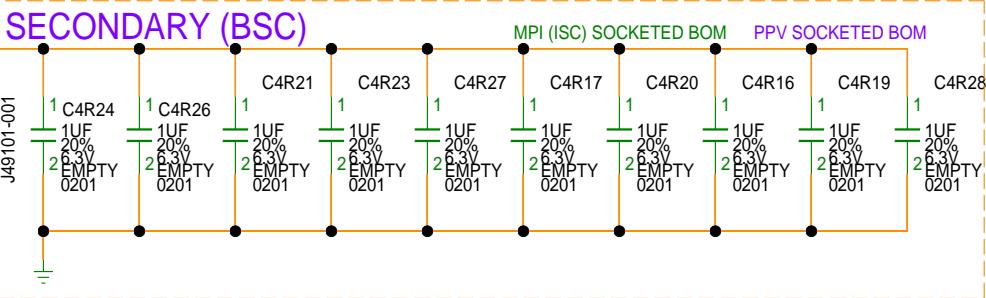
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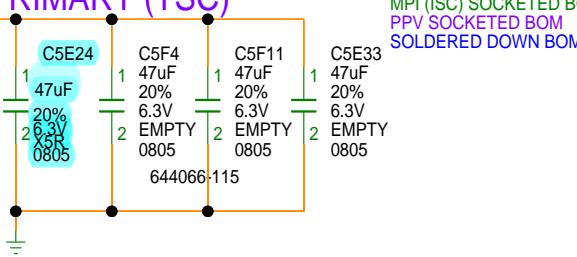
SECONDARY (BSC)



SECONDARY (BSC)

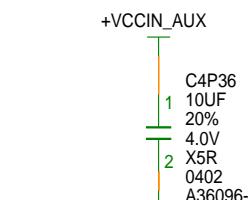


PRIMARY (TSC)

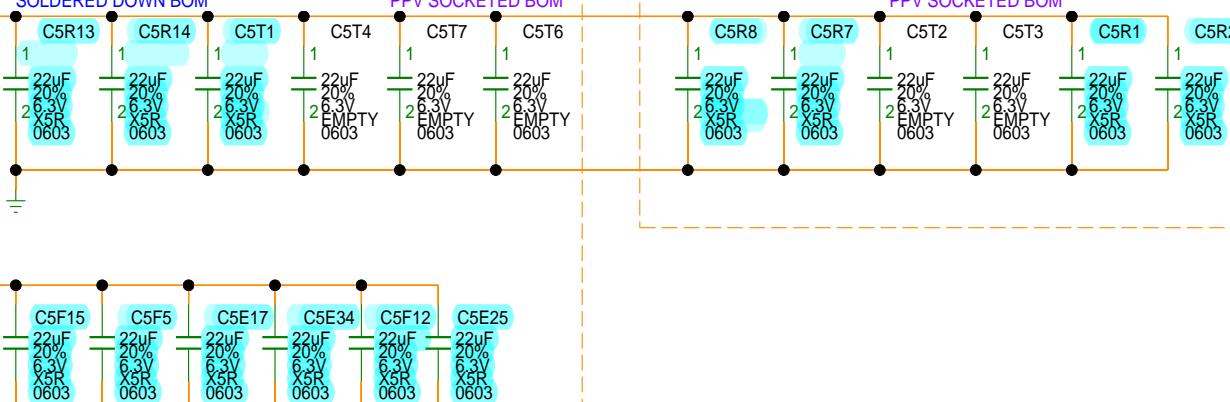


+VCCIN_AUX

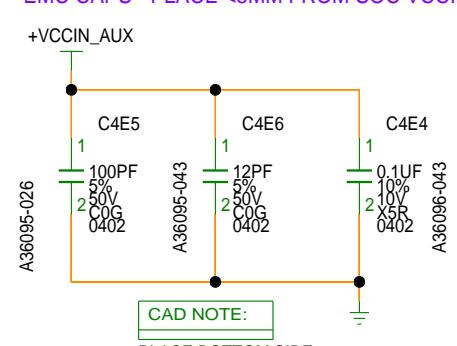
CAP ADDED FOR PI SIMULATION AS PER PI FEEDBACK
PLACE CLOSE TO PIN AK1 of SoC



SOLDERED DOWN BOM MPI (ISC) SOCKETED BOM PPV SOCKETED BOM



EMC CAPS - PLACE <5MM FROM SOC VCCIN_AUX



[PAGE_TITLE=PDBOM- VCCIN_AUX]

BPAGE DRAWING
tigerlake_u_ddr4.sch_158
Wed Dec 18 18:42:42 2019

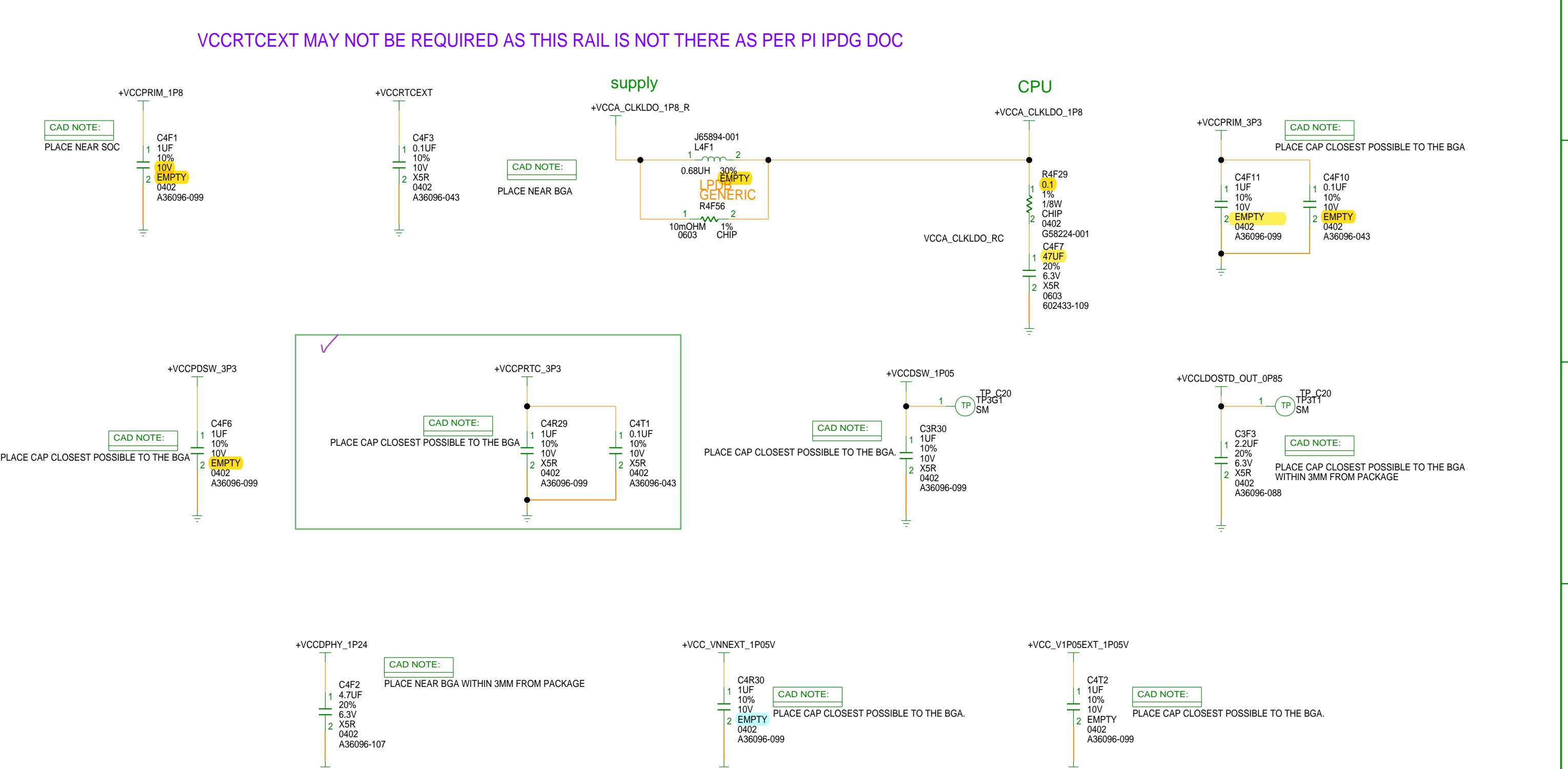
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	58	1.0	

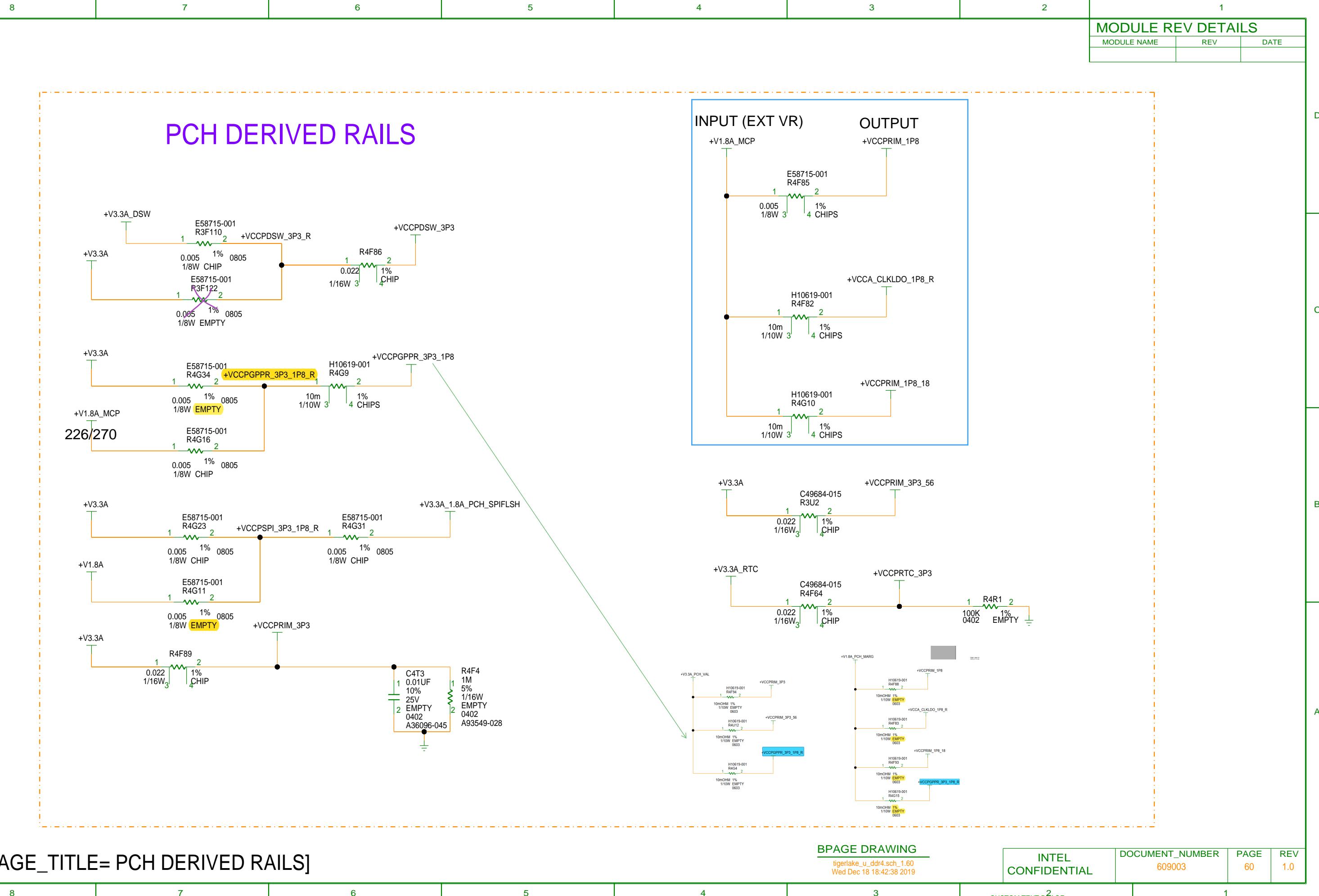
CUSTOM TEXT BPAGE

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8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

VCCRTCEXT MAY NOT BE REQUIRED AS THIS RAIL IS NOT THERE AS PER PI IPDG DOC





8	7	6	5	4	3	2	1
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PCH MARGINING RAILS

MODULE REV DETAILS

MODULE NAME	REV	DATE

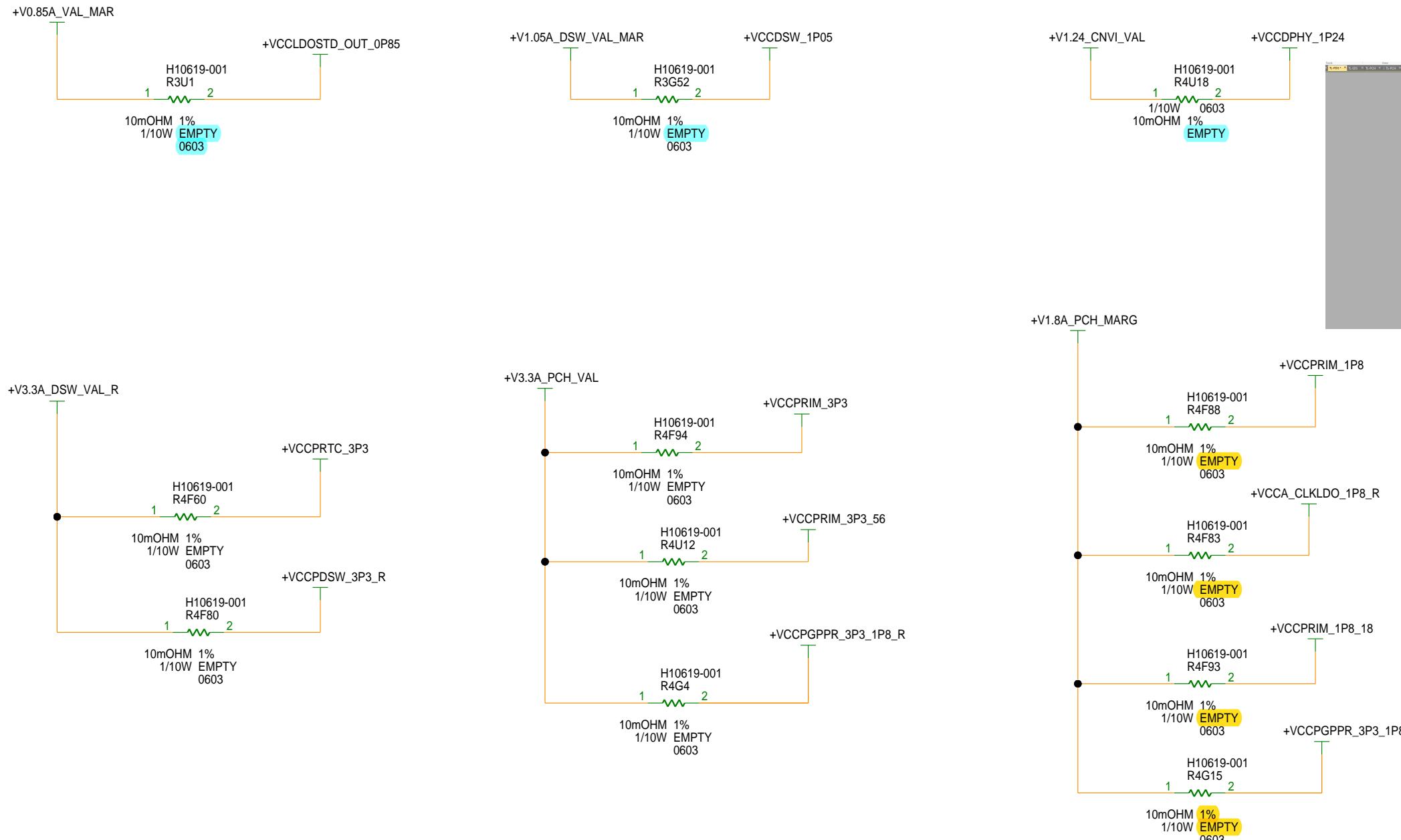
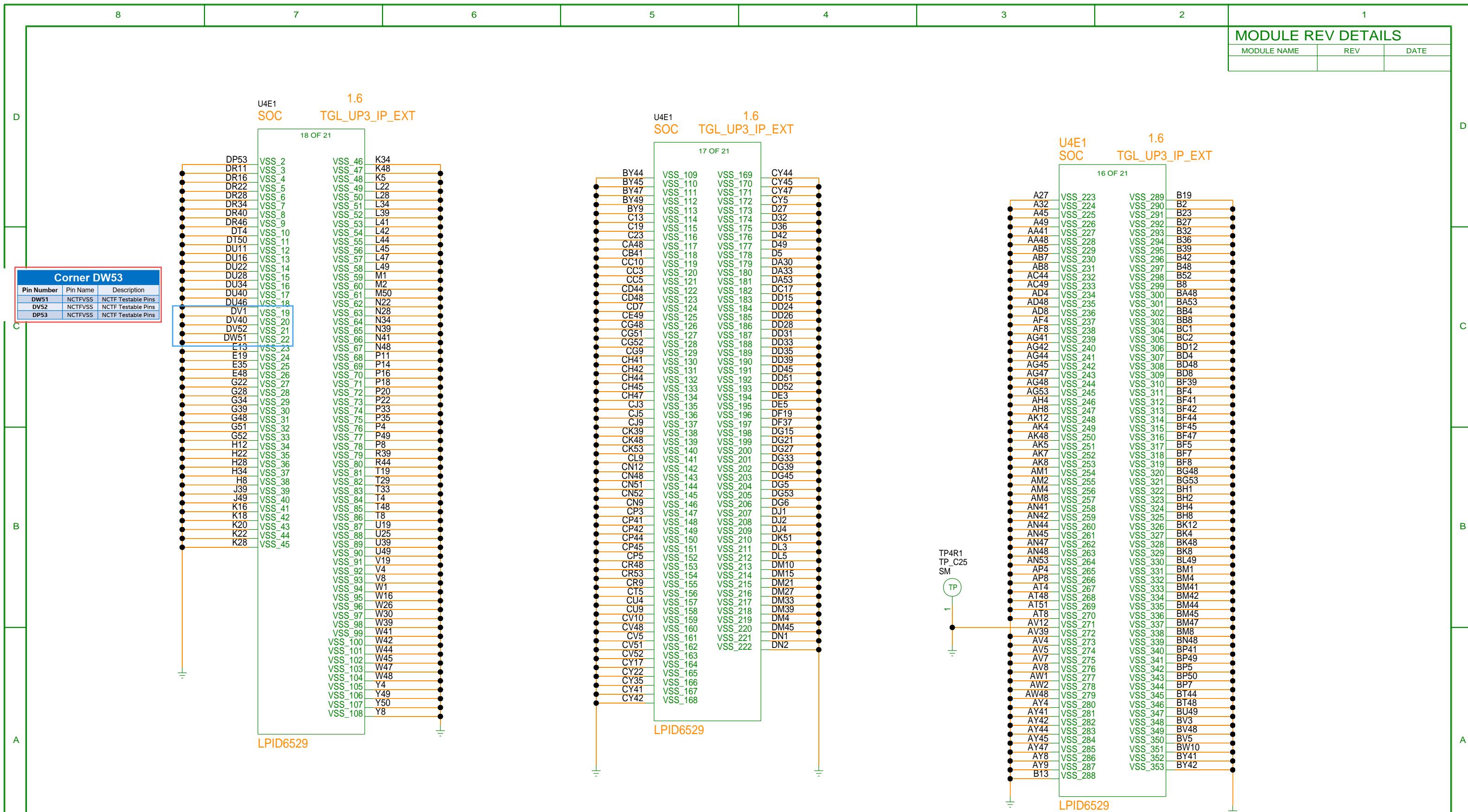


Table 237. No Direct Switching or No External Bypass Supported						
State Enable	Q1 CNVI	Q2 ISH	Q3 Type A	Q4 C-Link	Q5 SMBus	Q6 PHY PG
S02.0	Always Enable	-	-	-	-	-
S02.1	Always Enable	-	-	-	-	YES
S02.2	-	-	NO	-	-	-
S03.0	NO	NO	-	-	-	-
S03.1	NO	NO	-	-	-	-
S03.2	NO	NO	-	-	-	-
S03.3	NO	NO	NO	-	-	YES

Voltage Margining
Voltage margining allows bypass VRs to reduce their voltages depending on S03.x states. To enable this feature, VNN_CTRL and V1P05_CTRL GPIO pins should be configured. This feature can reduce power in Soix states.

Tiger Lake UP3 UP4 H35 UP3 Refresh Platform

November 2020



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

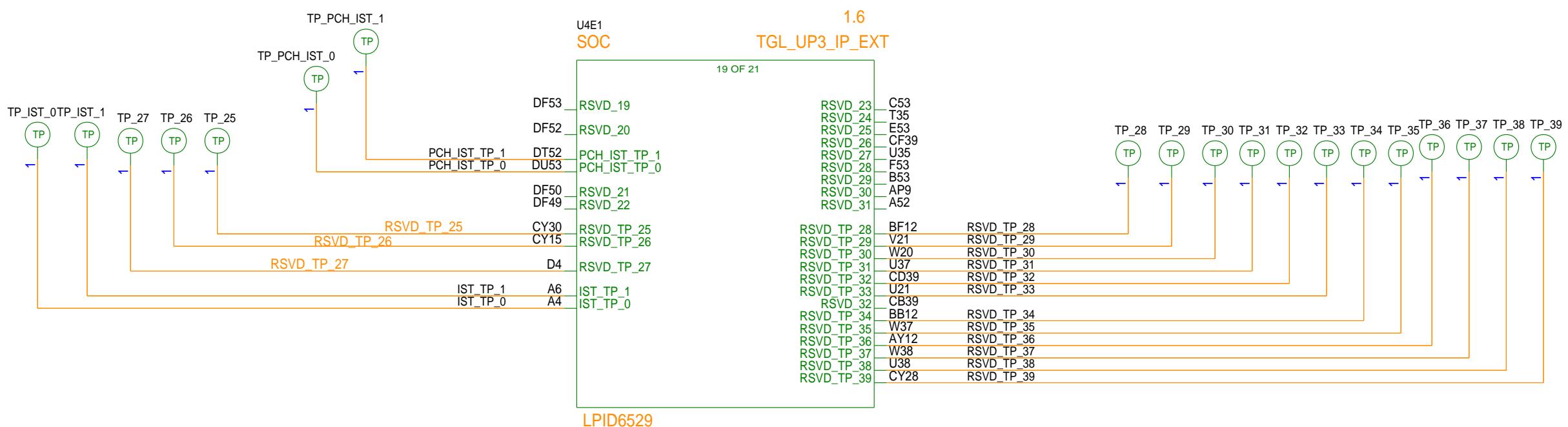
[PAGE_TITLE=TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)]

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.62
Wed Dec 18 19:06:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 62	REV 1.0
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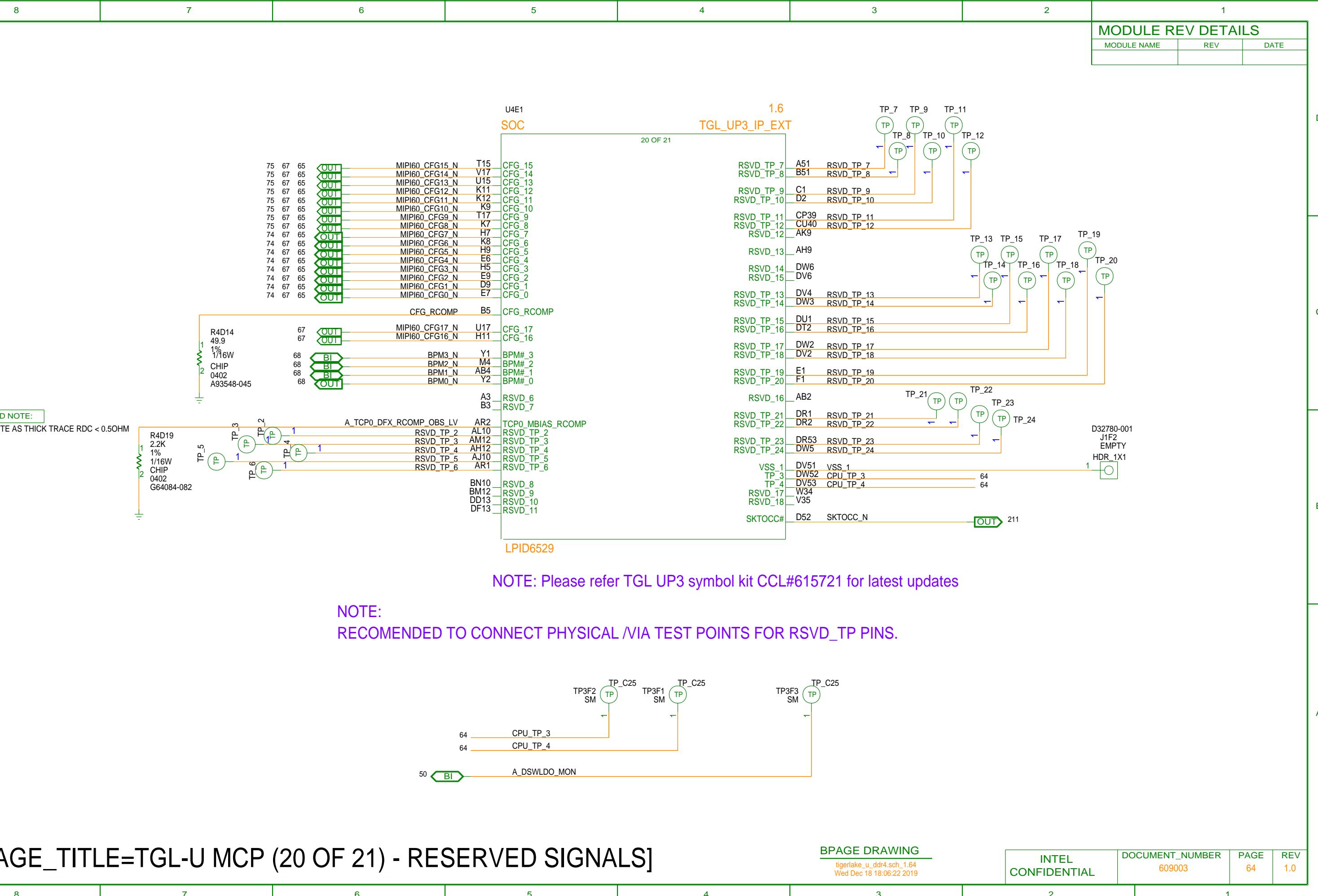
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MODULE REV DETAILS						MODULE NAME	REV	DATE



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

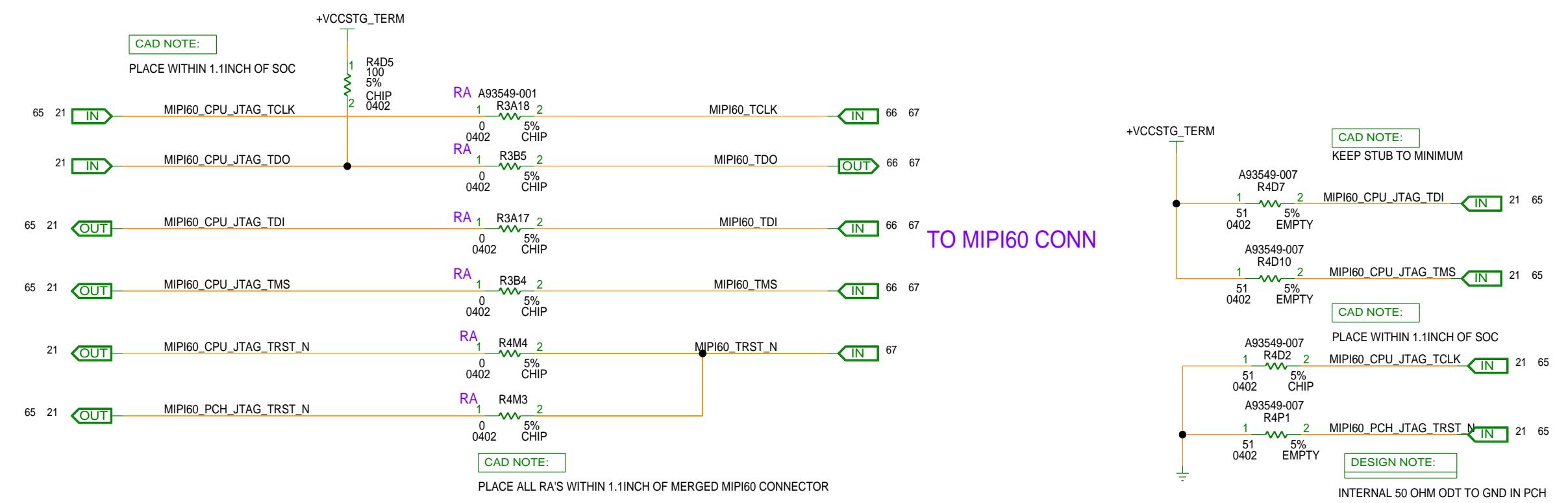
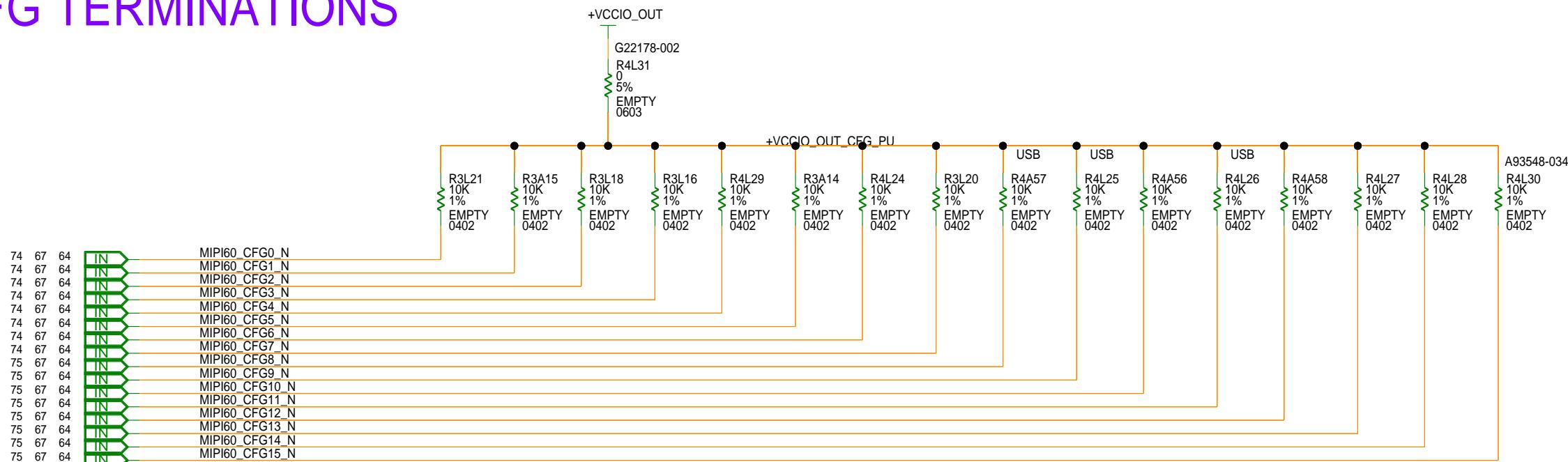
NOTE:

RECOMENDED TO CONNECT PHYSICAL /VIA TEST POINTS FOR RSVD_TP PINS.



8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME	REV	DATE					

CFG TERMINATIONS



[PAGE_TITLE=JTAG/CFG - CFG TERMINATIONS]

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.65
Wed Dec 18 18:06:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

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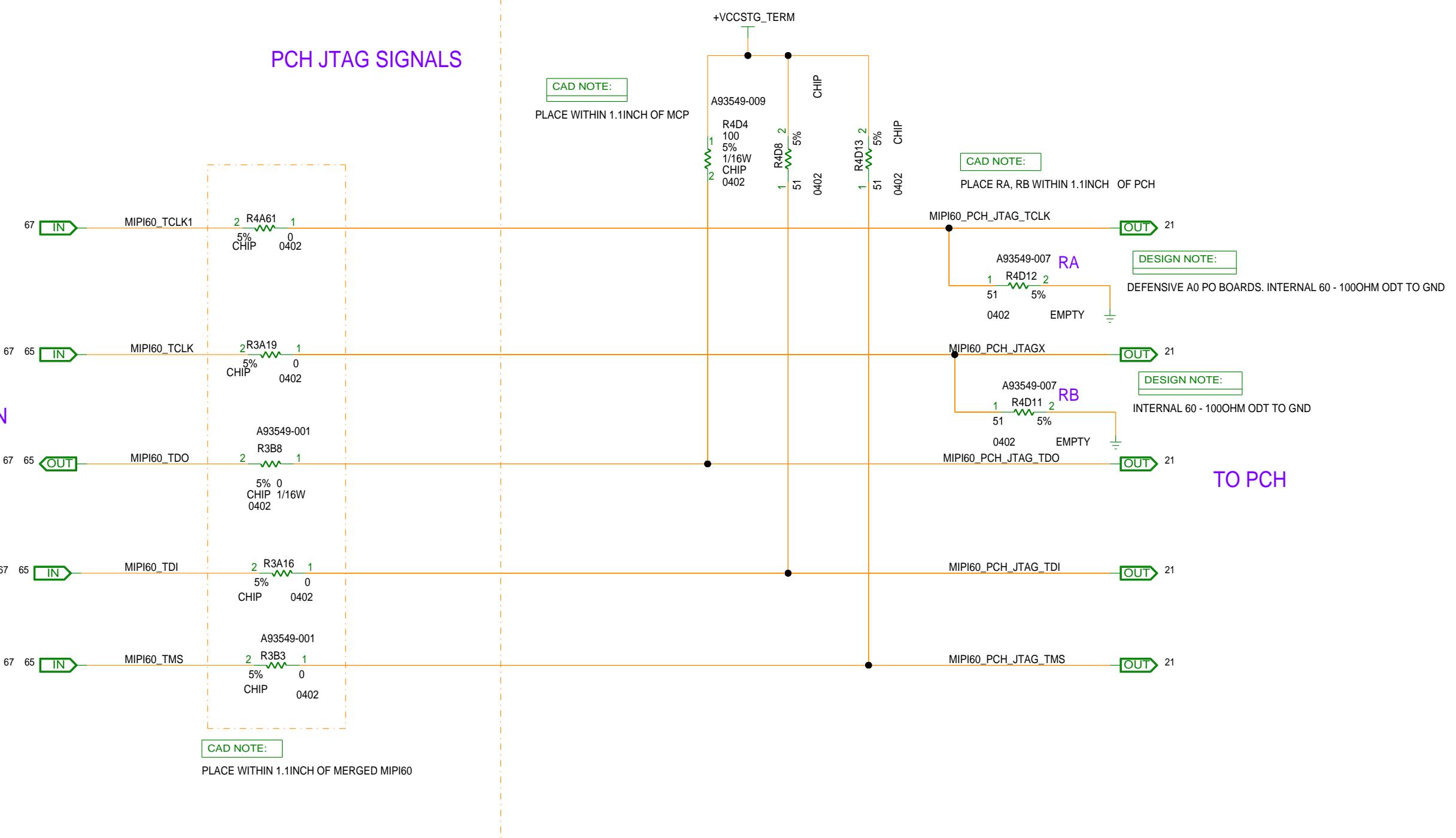
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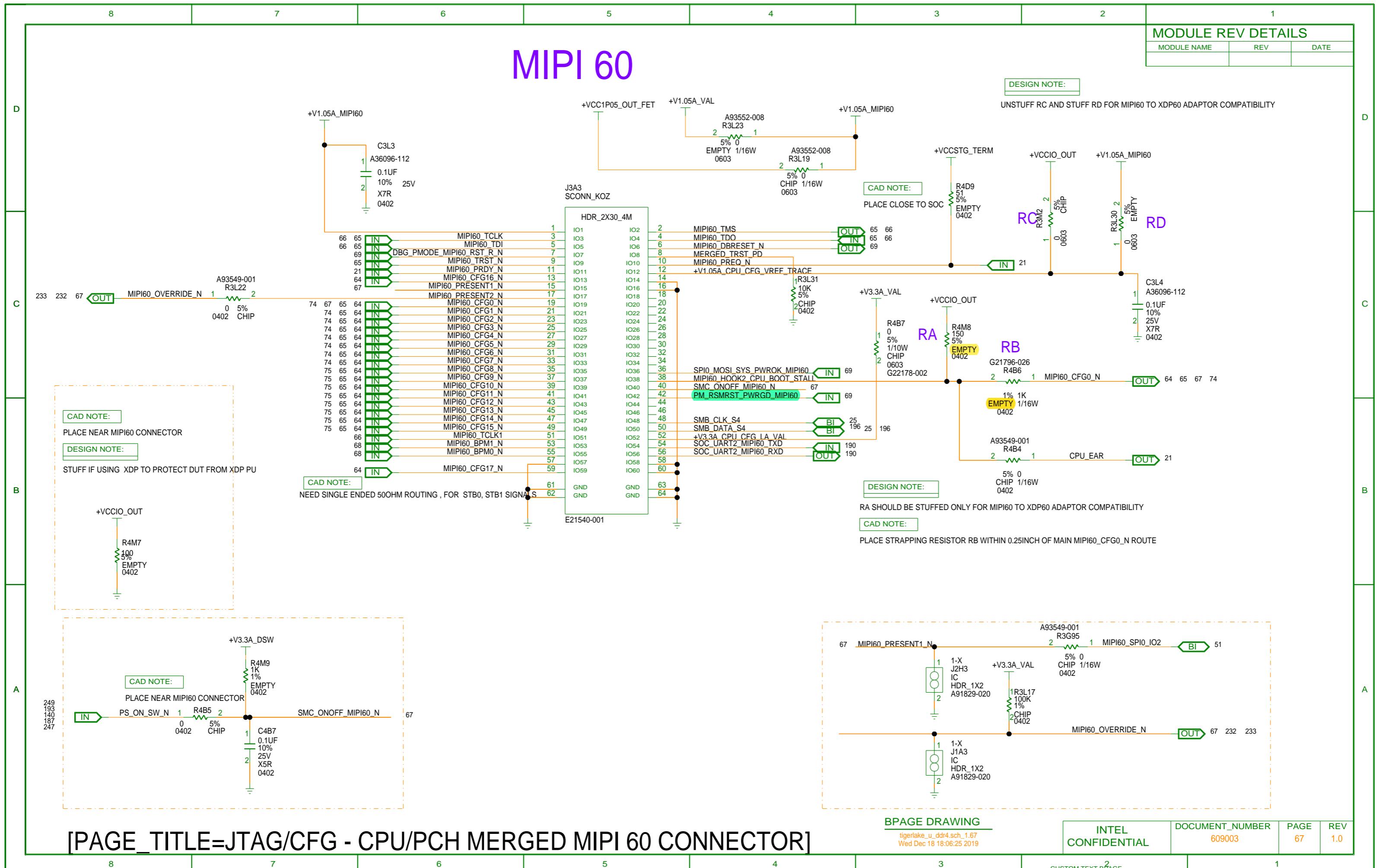
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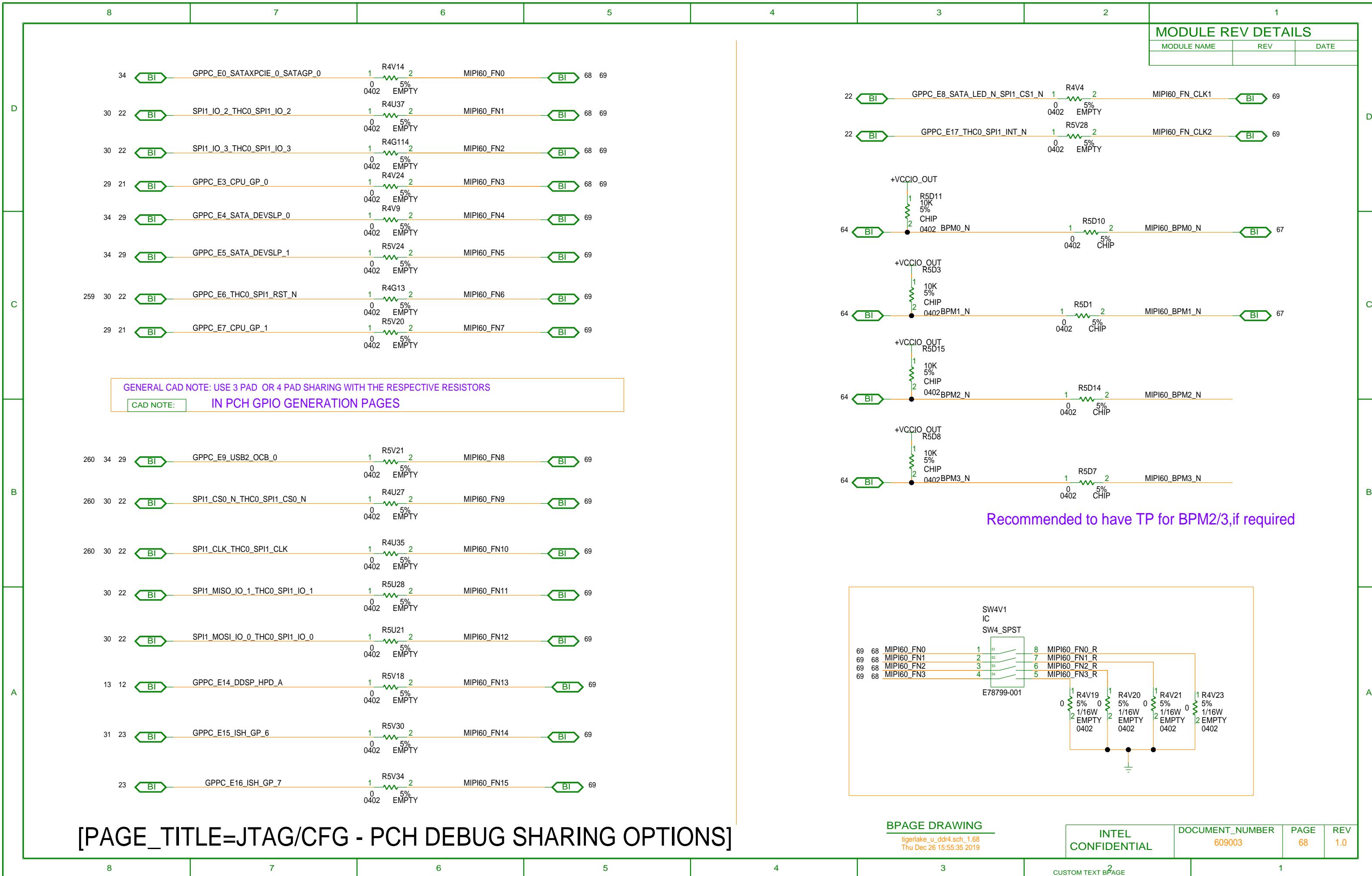
MODULE NAME	REV	DATE

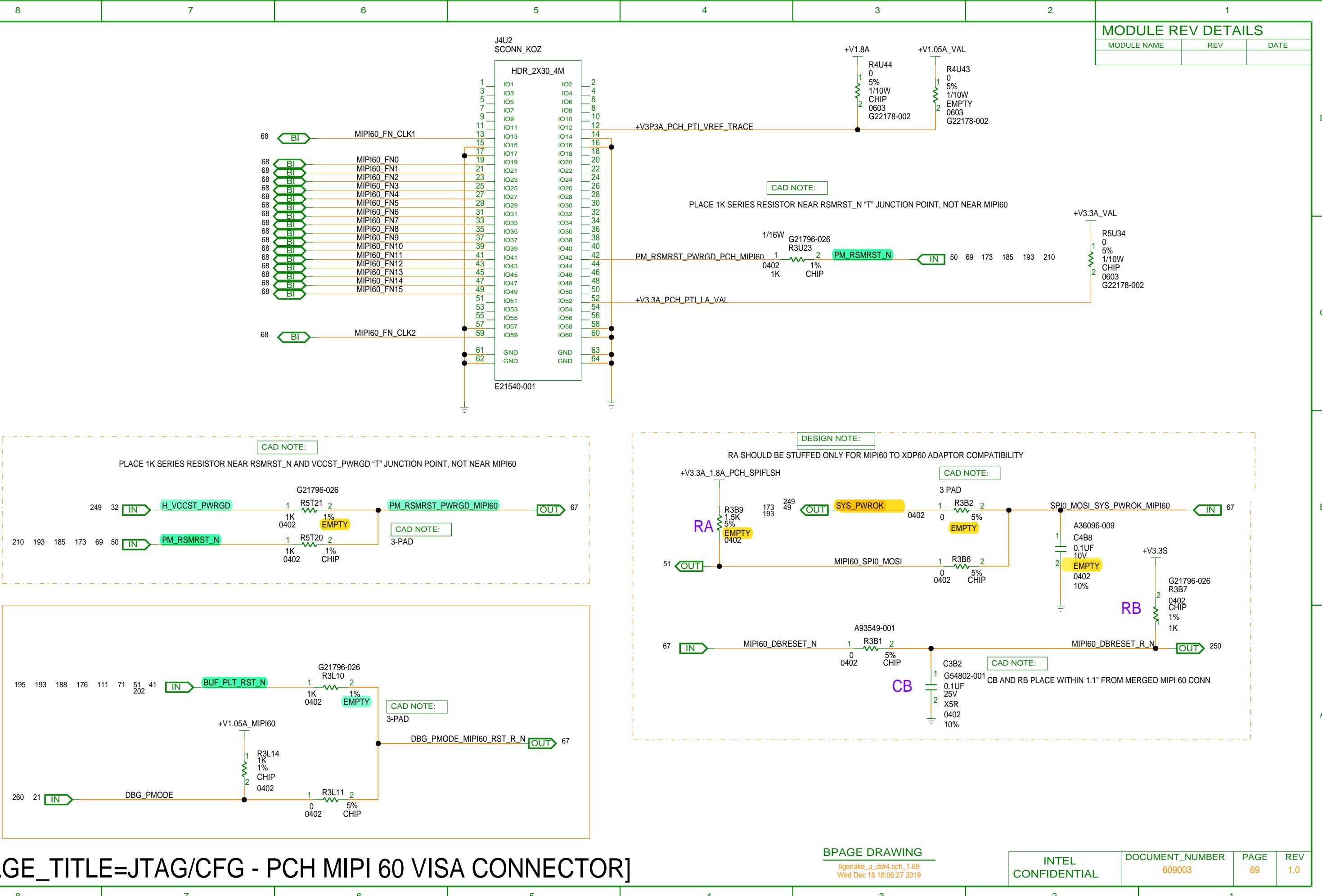
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PCH JTAG SIGNALS**TO MIPI60 CONN****TO PCH**





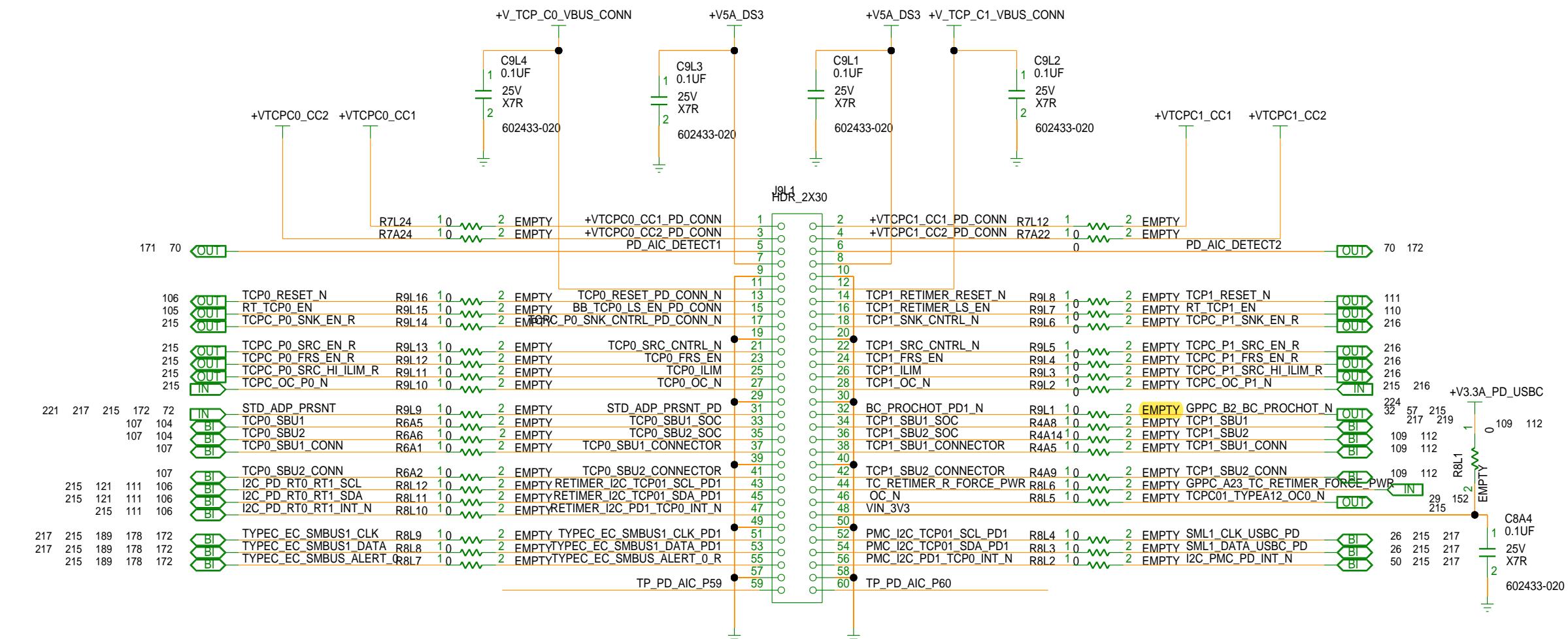


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PD AIC CONTROLLER

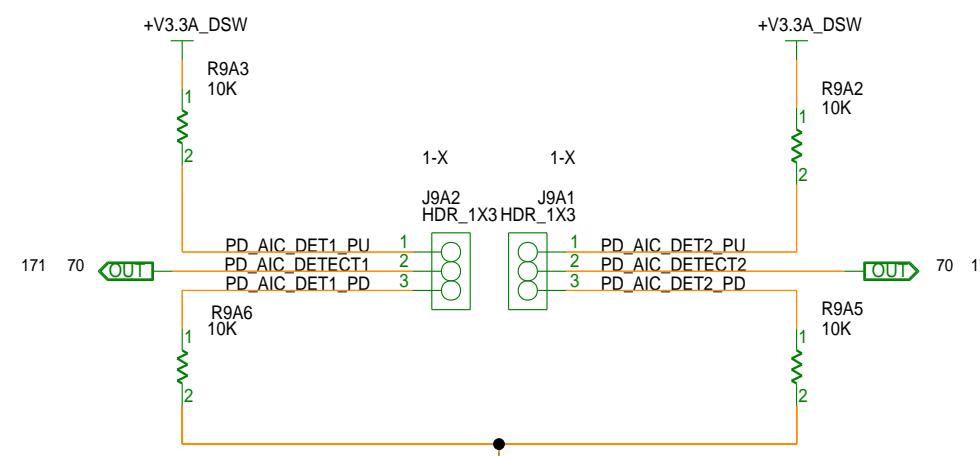
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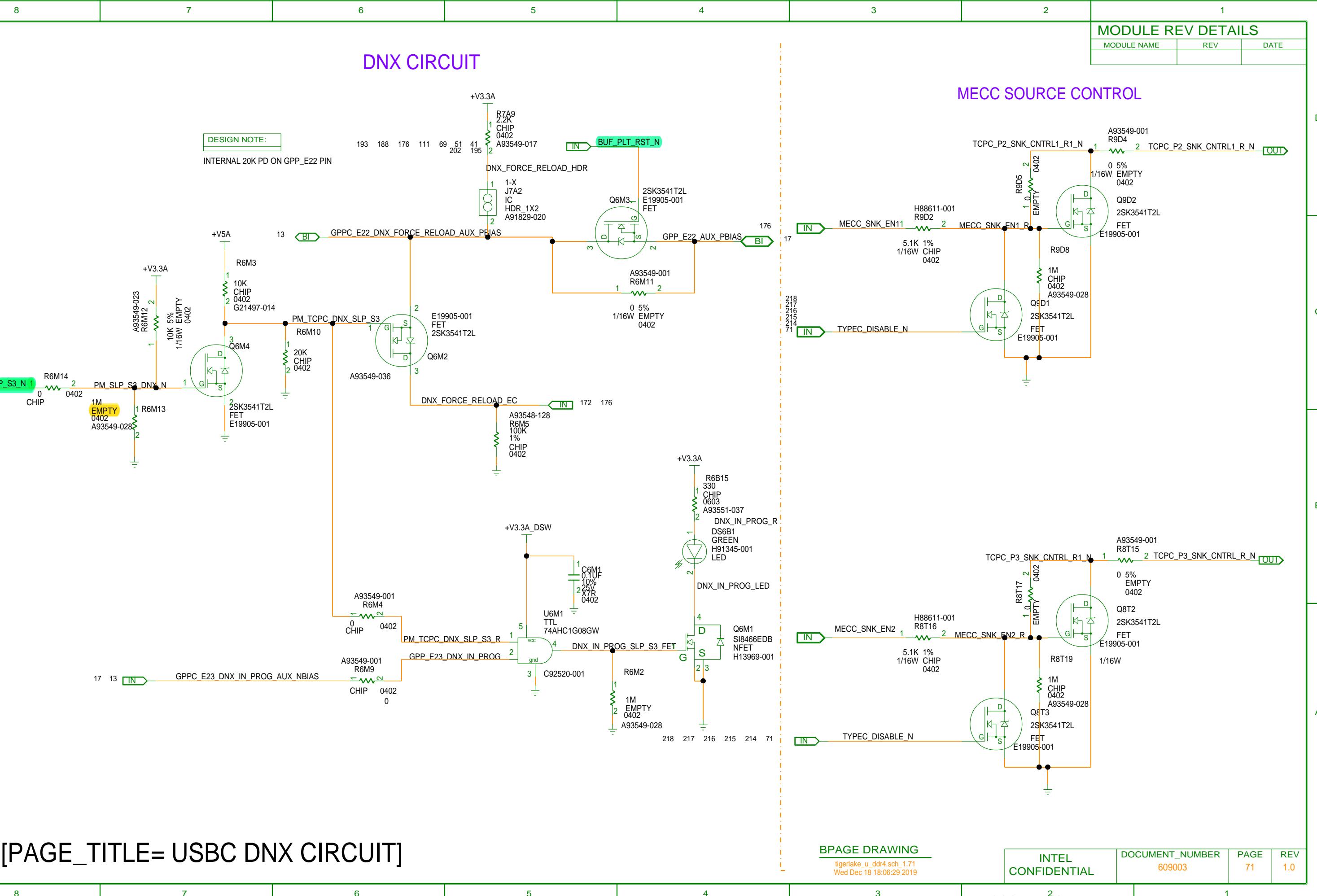
MODULE NAME	REV	DATE

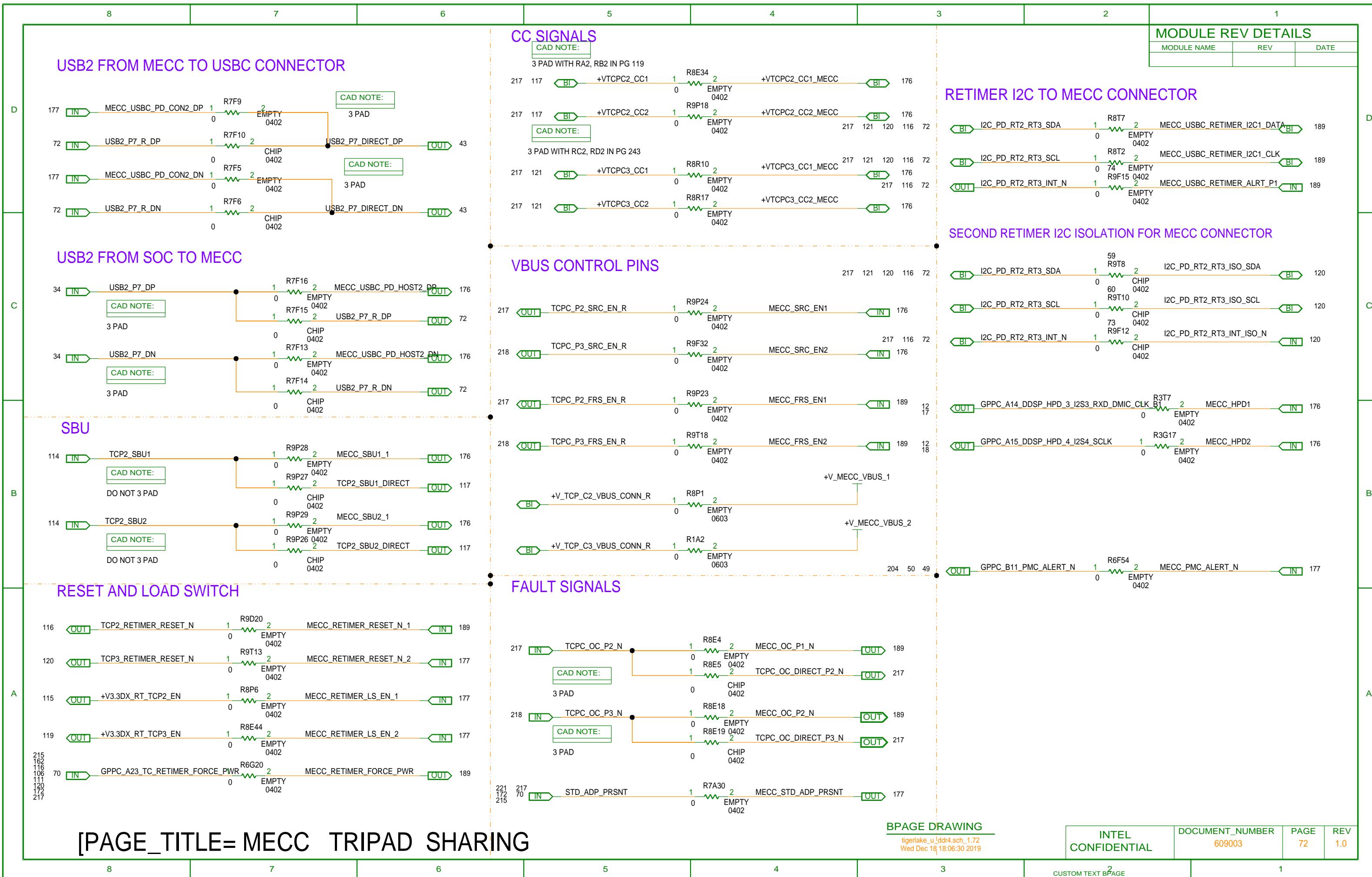


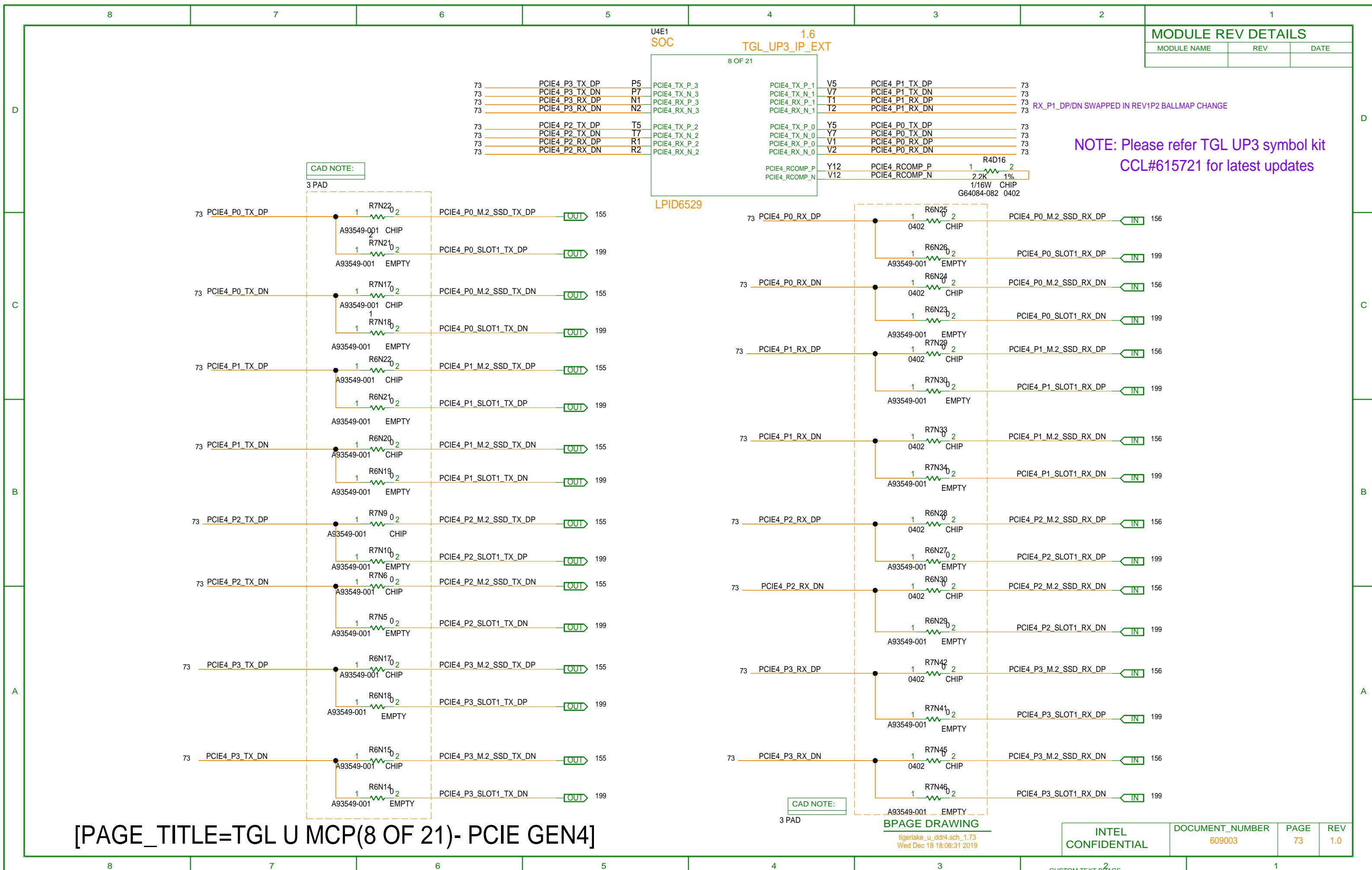
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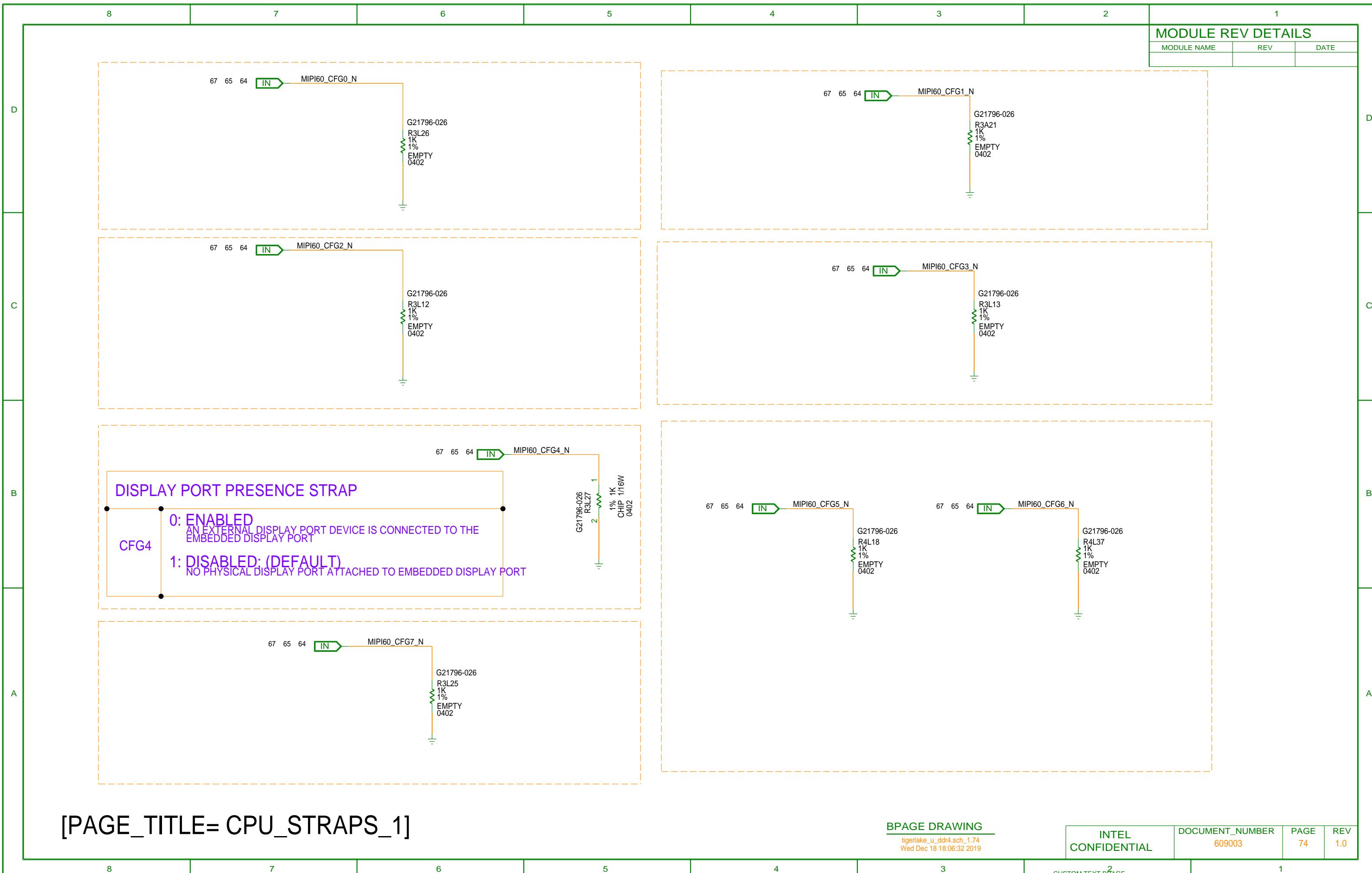
ALL THE RESISTORS IN THIS PAGE SHOULD BE TRIPAD WITH RESPECTIVE RESISTOR IN OTHER SECTION

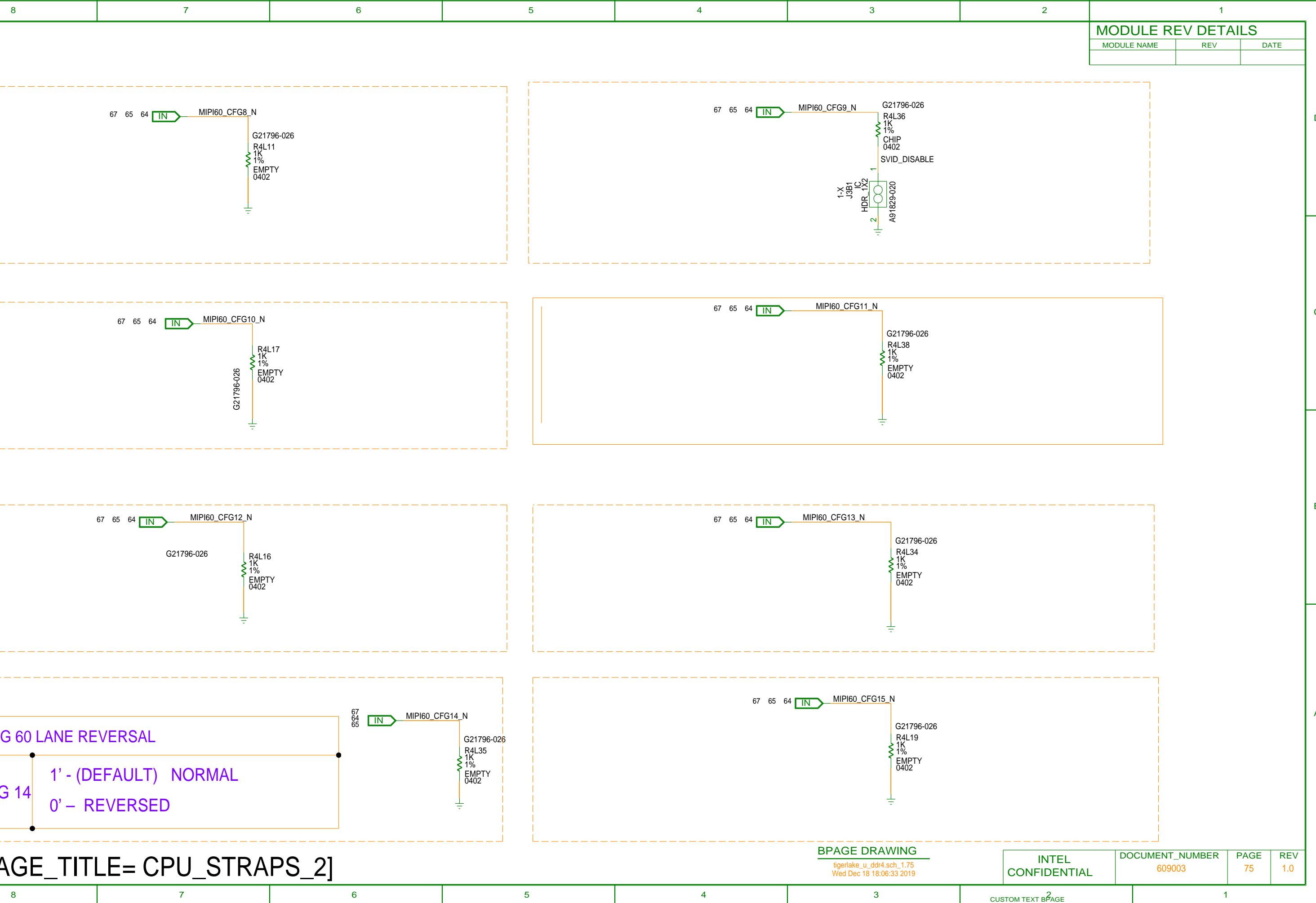






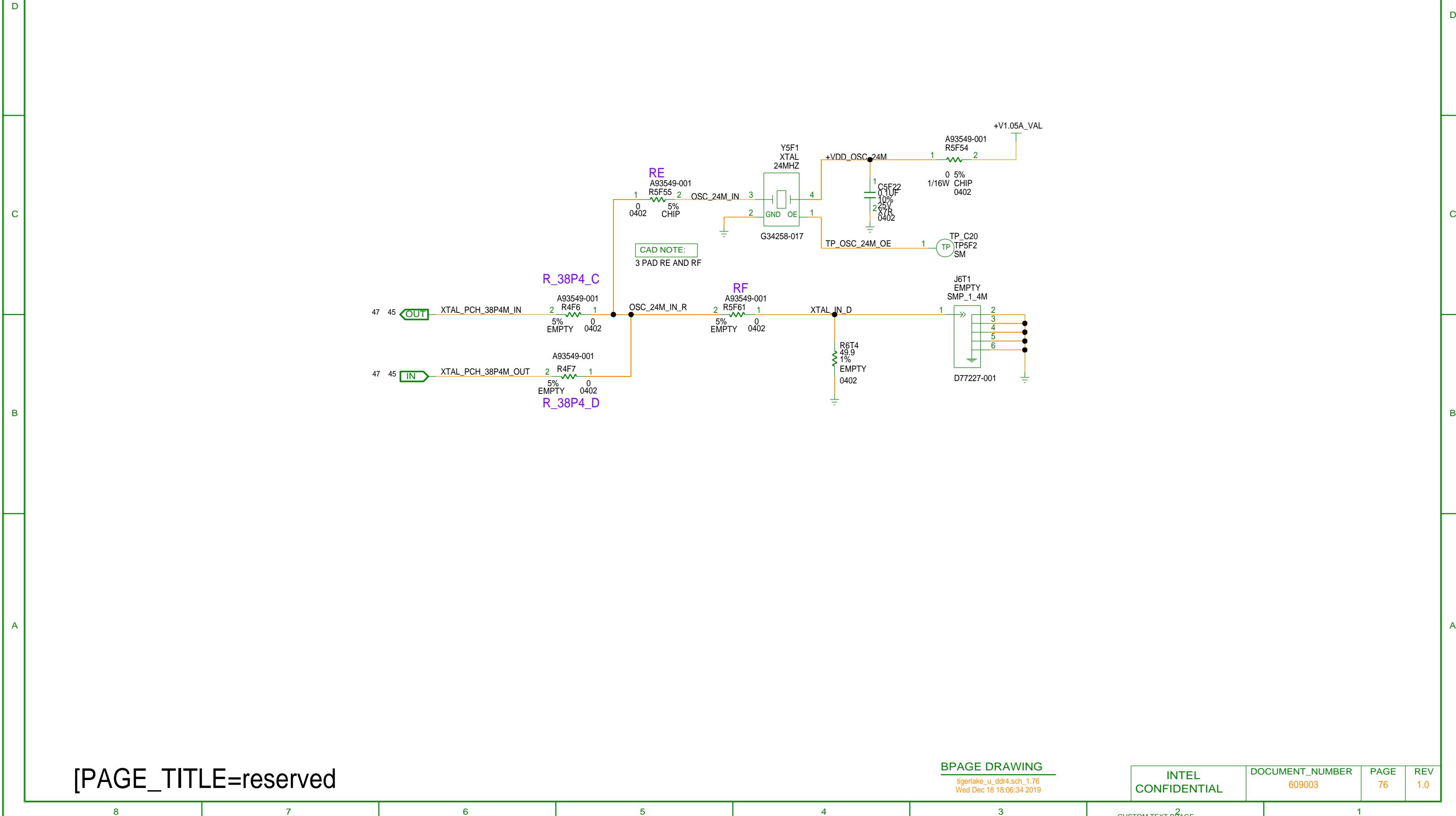






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MODULE REV DETAILS		
MODULE NAME	REV	DATE



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Wed Dec 18 18:06:34 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE

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MODULE REV DETAILS

MODULE NAME	REV	DATE

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[PAGE_TITLE=RESERVE]BPAGE DRAWING

tigerlake_u_ddr4.sch_1.77
Tue Oct 15 12:49:33 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	77	1.0

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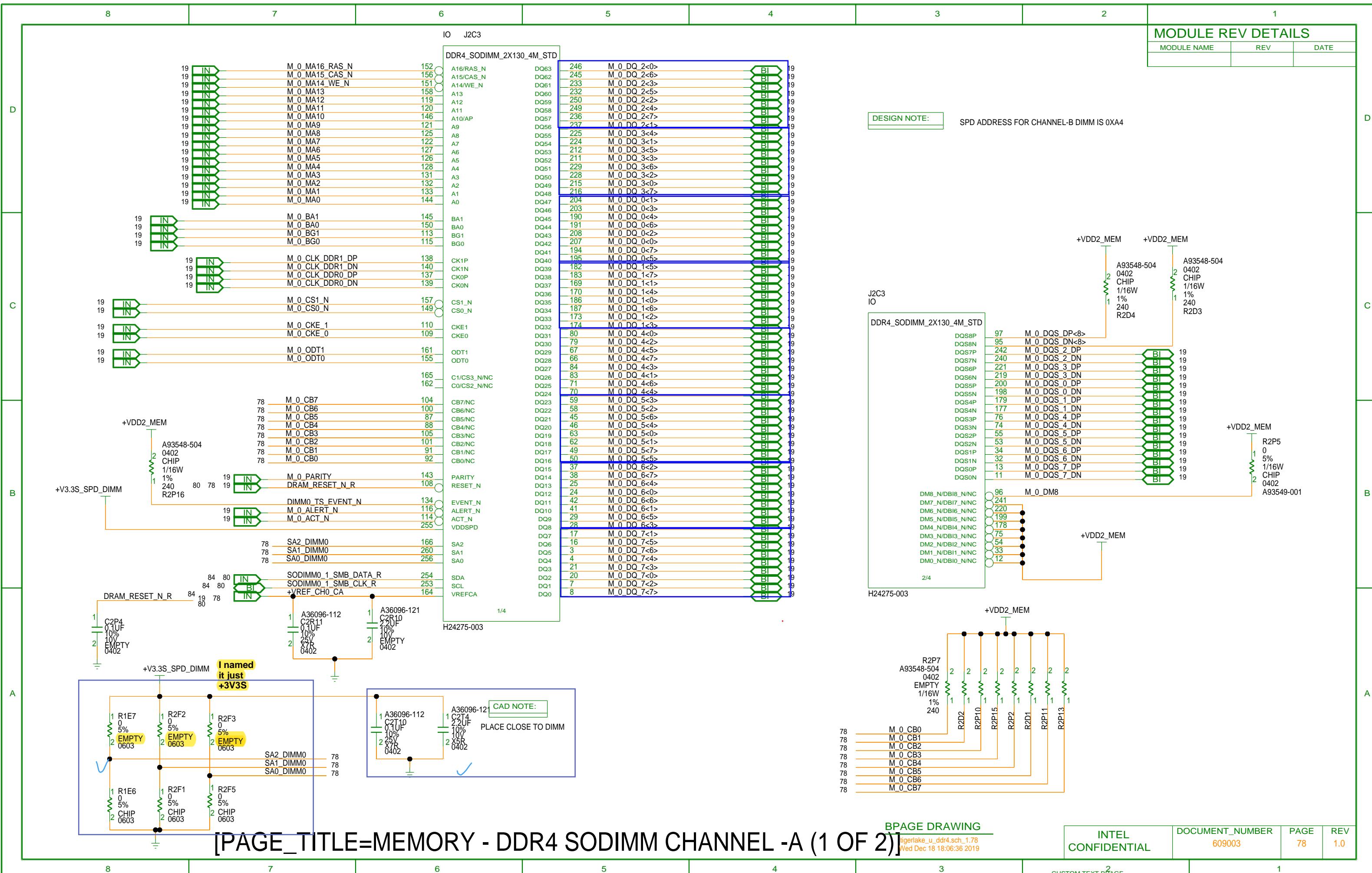
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CUSTOM TEXT 2 PAGE

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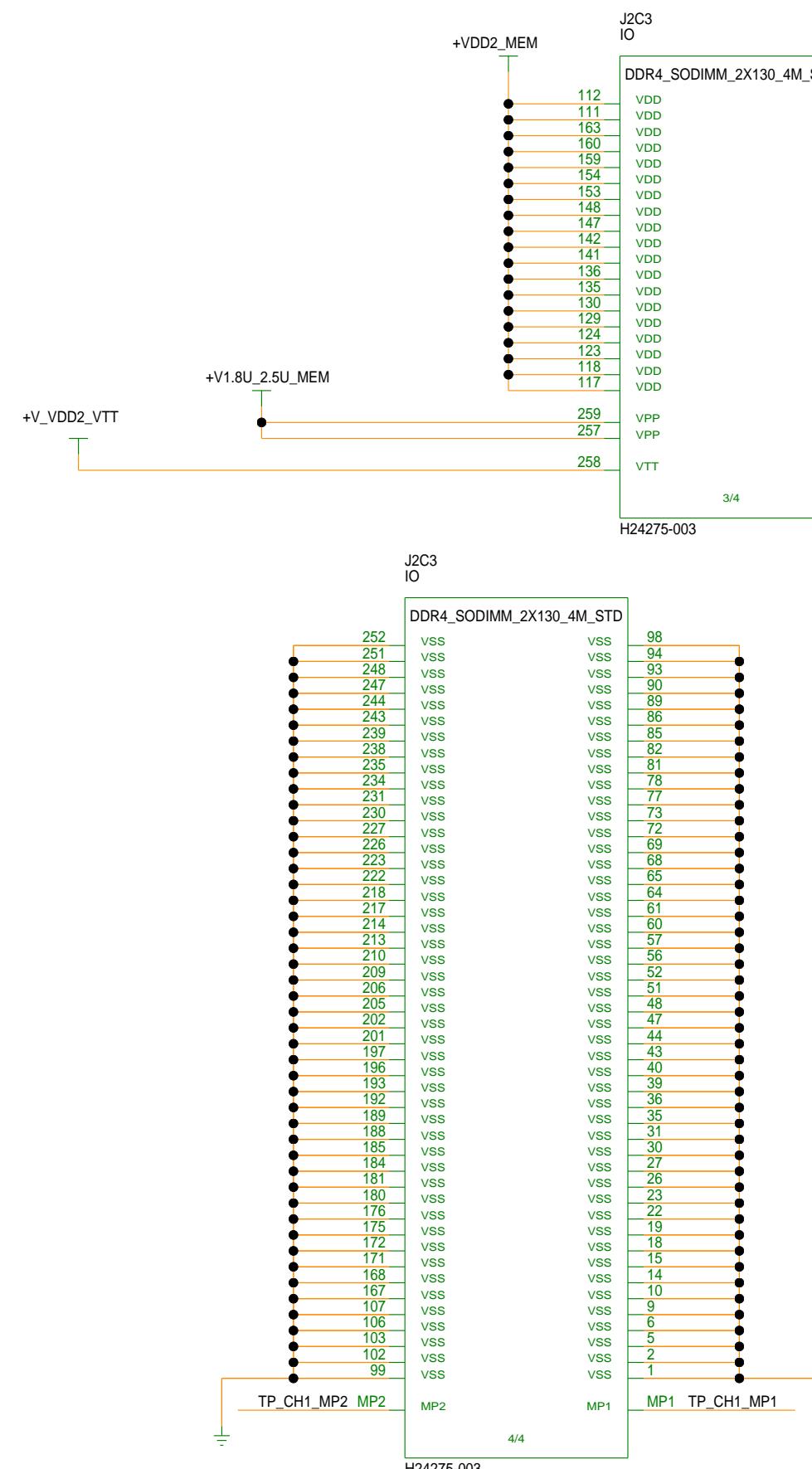
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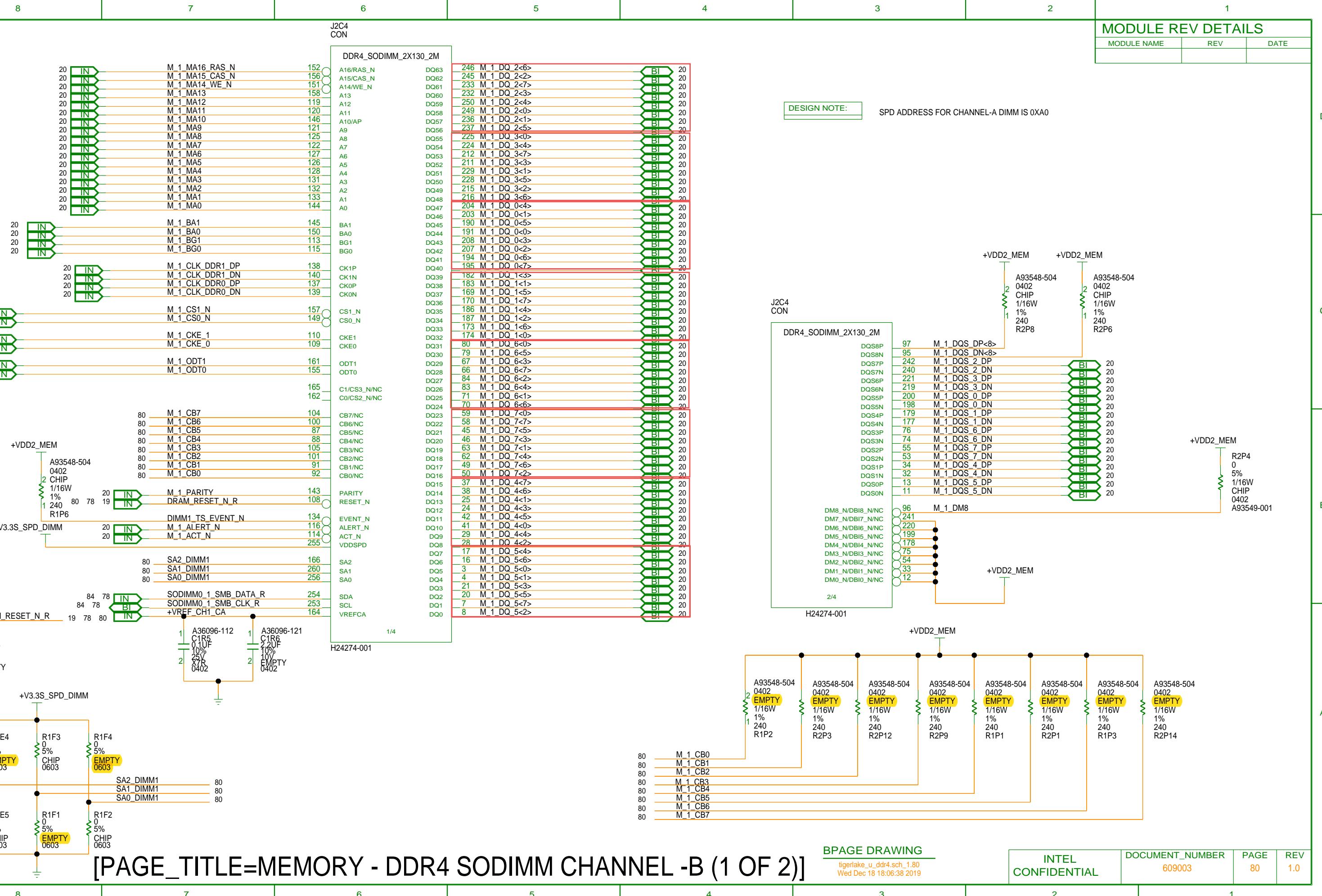
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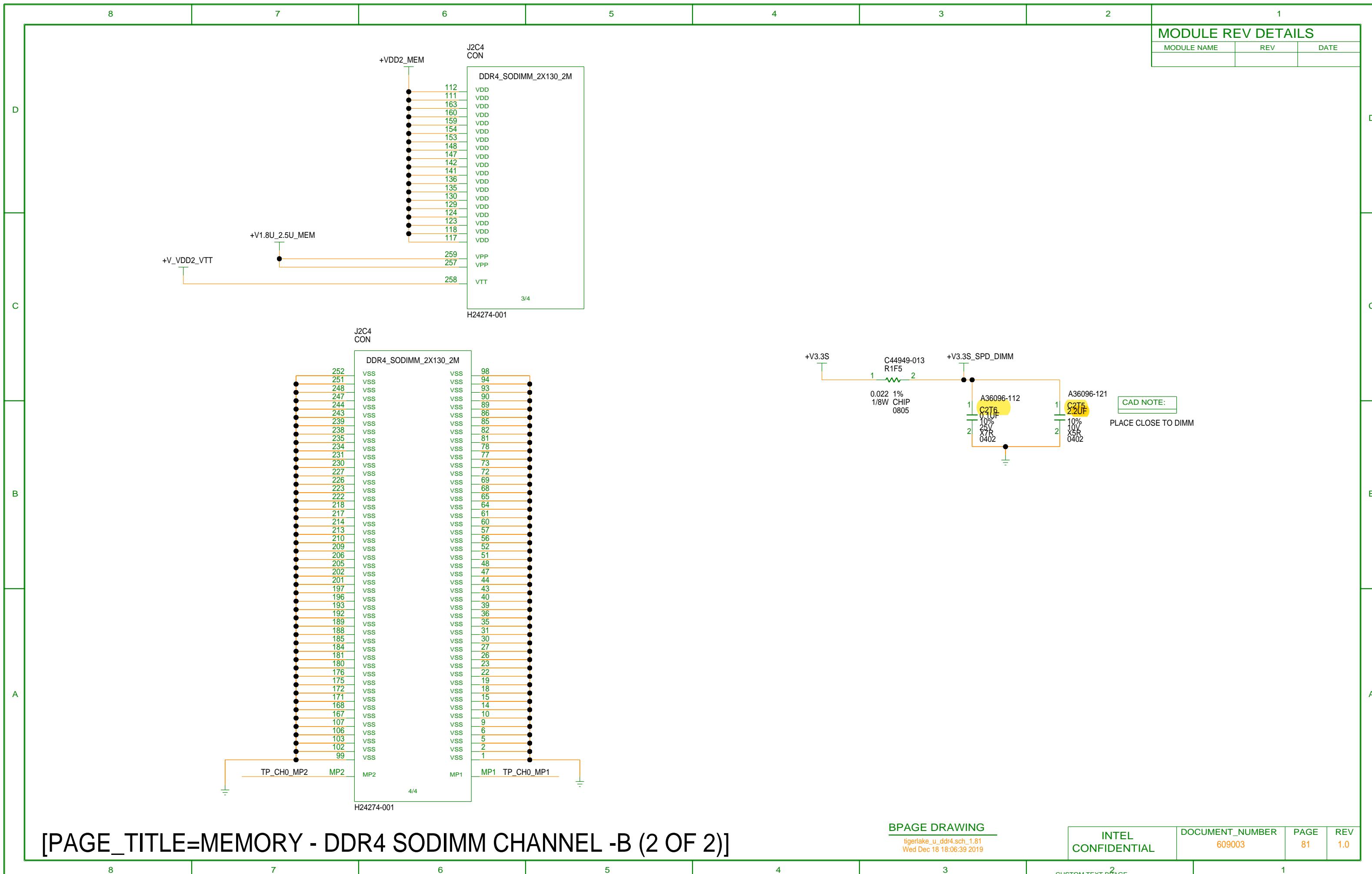
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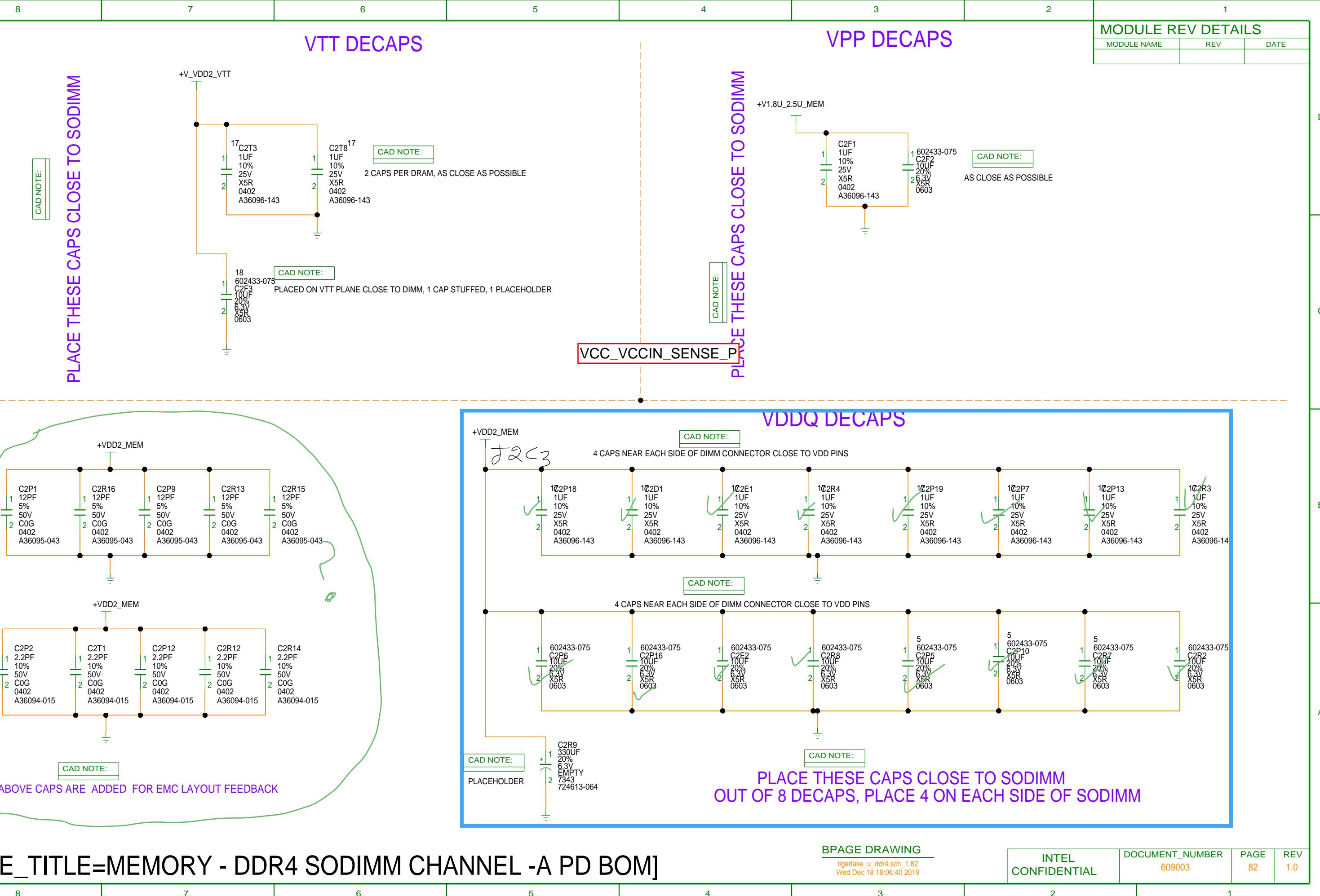
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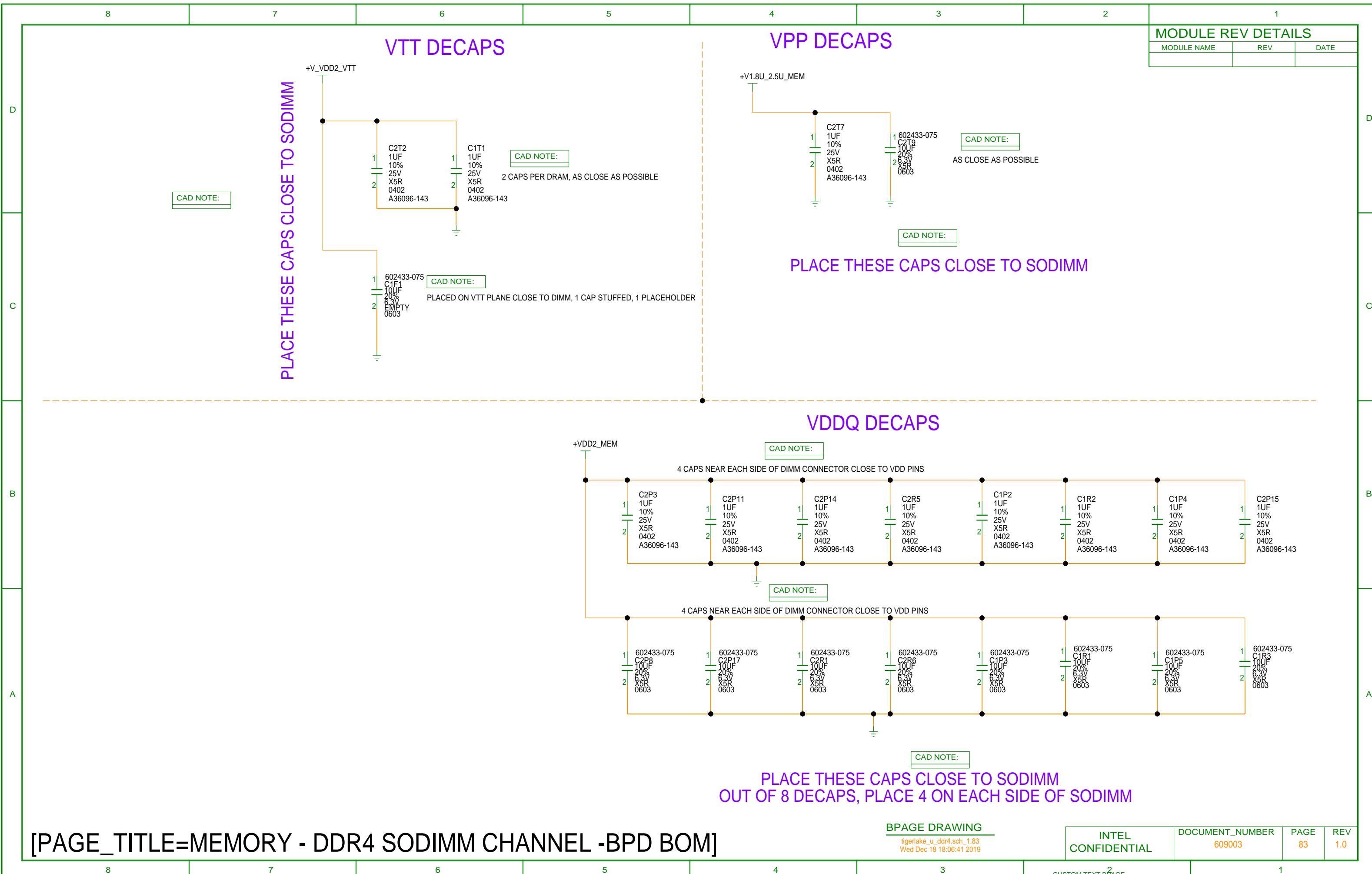
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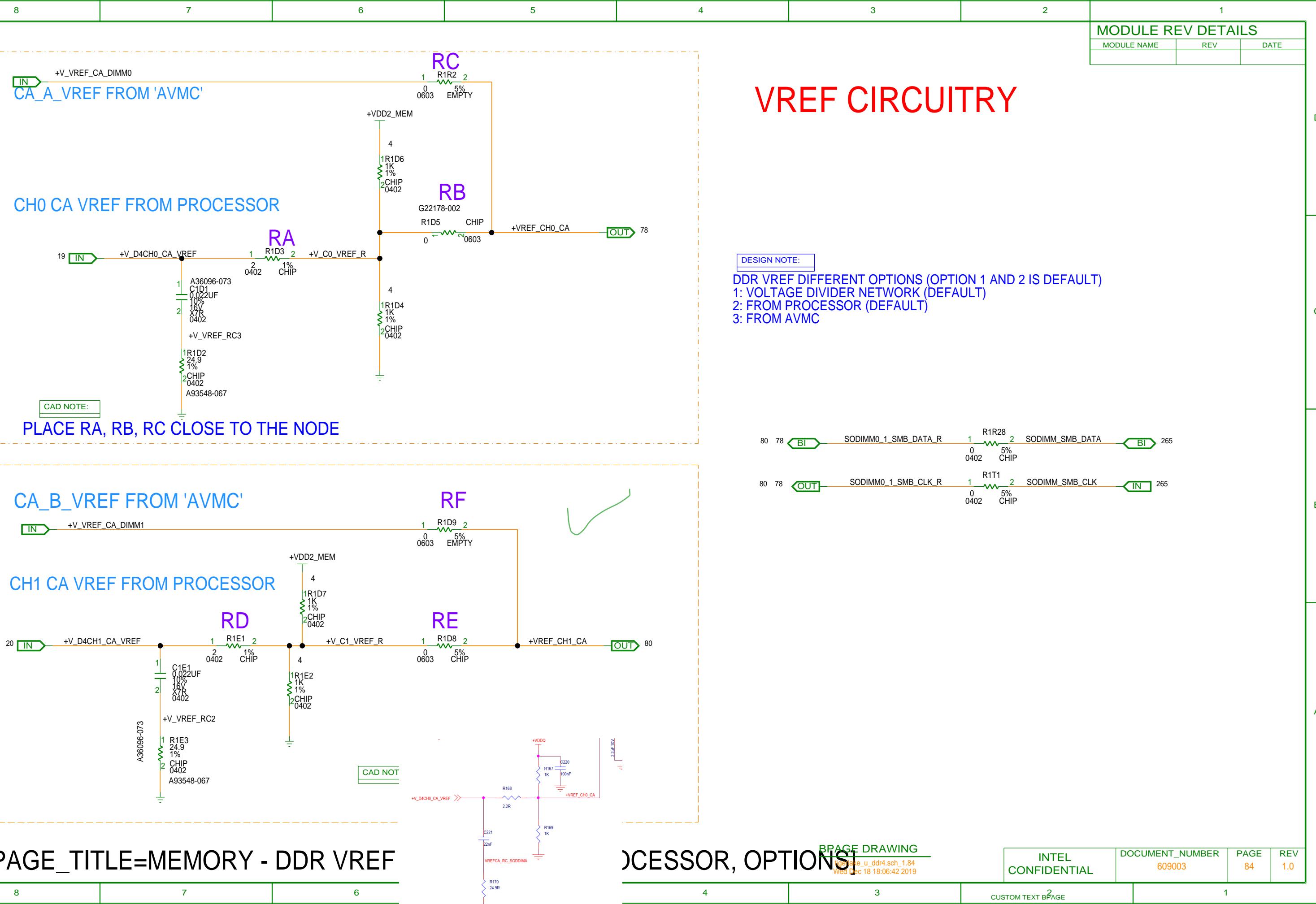












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MODULE REV DETAILS

MODULE NAME	REV	DATE

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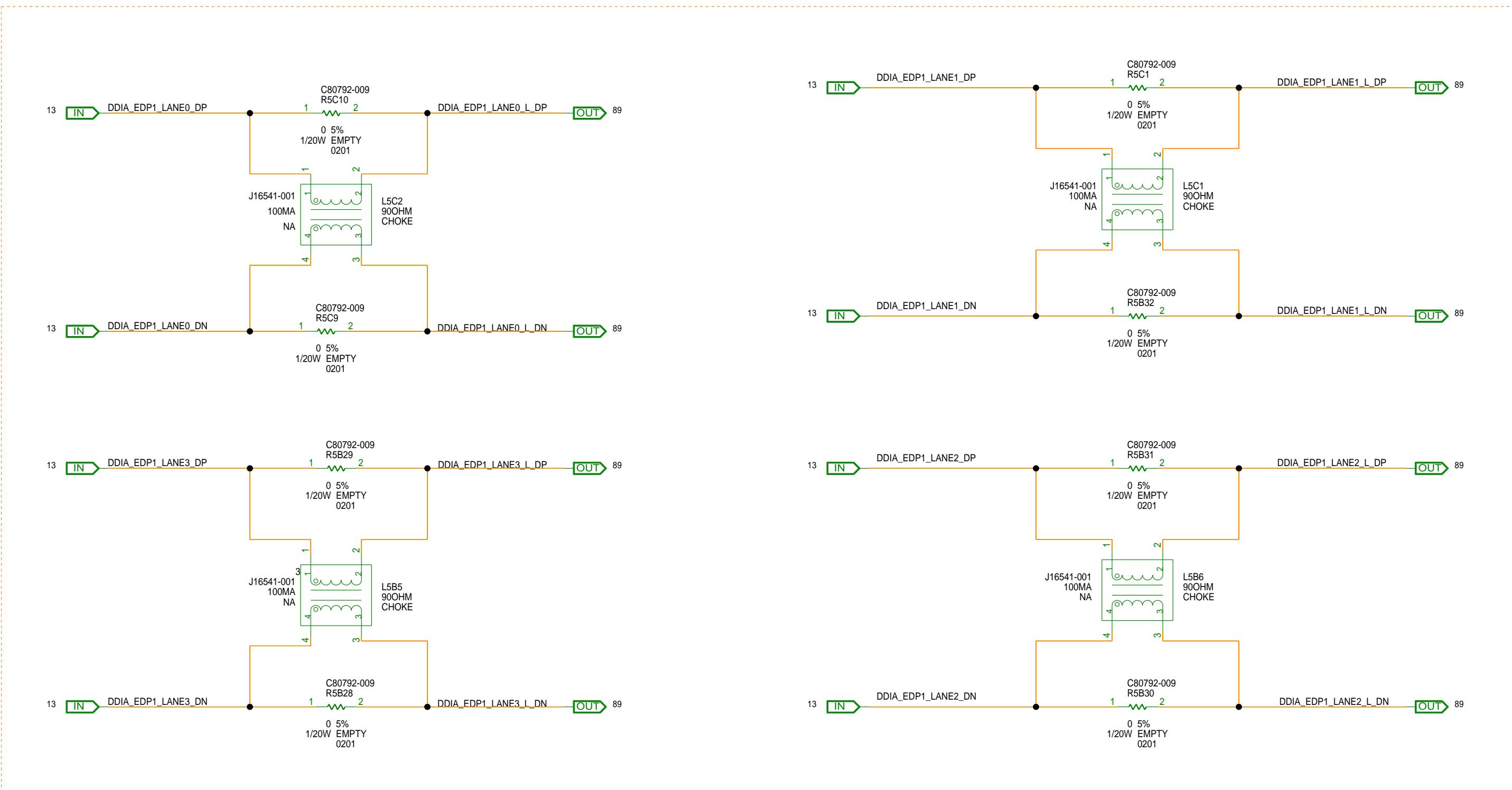
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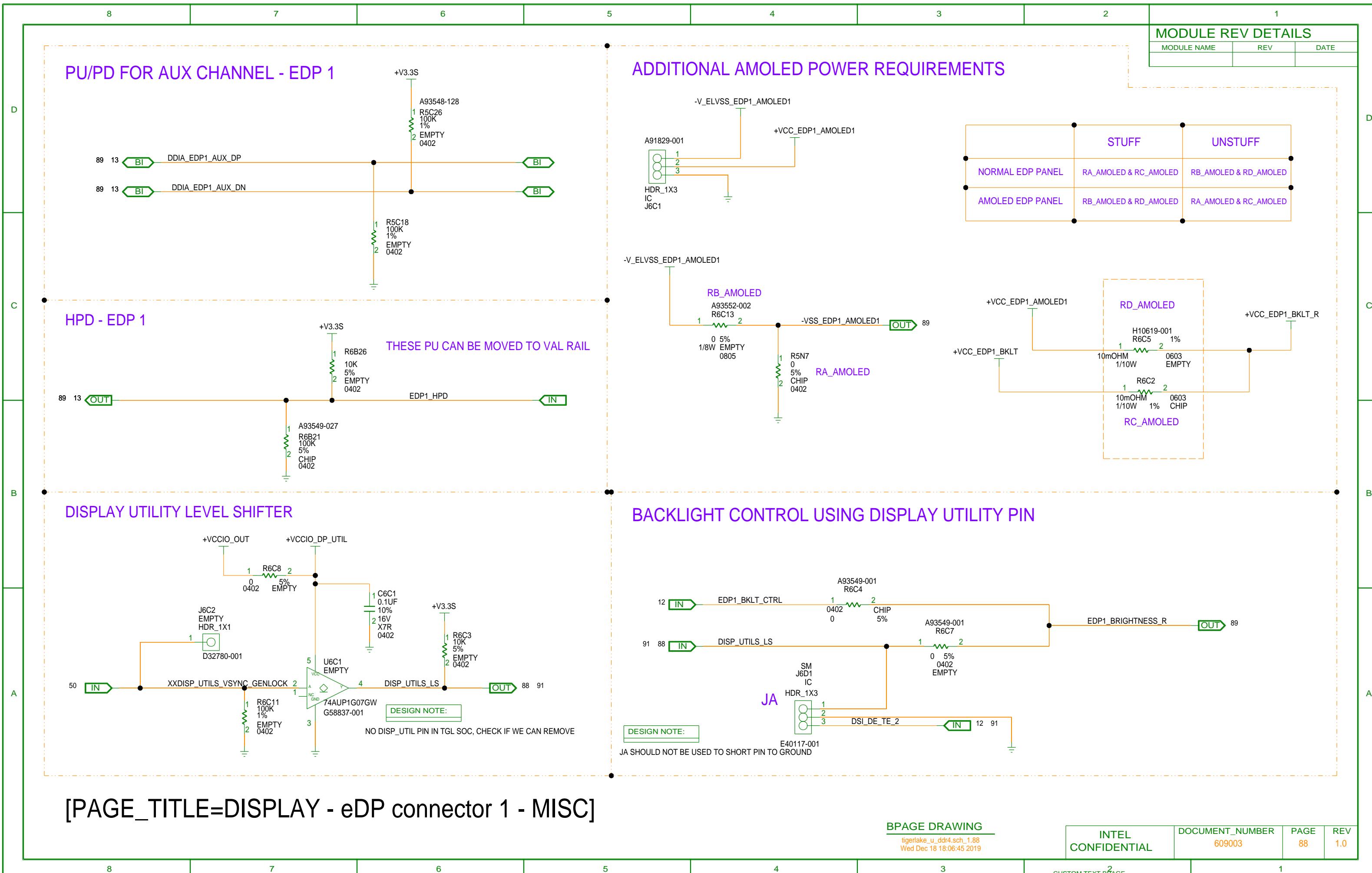


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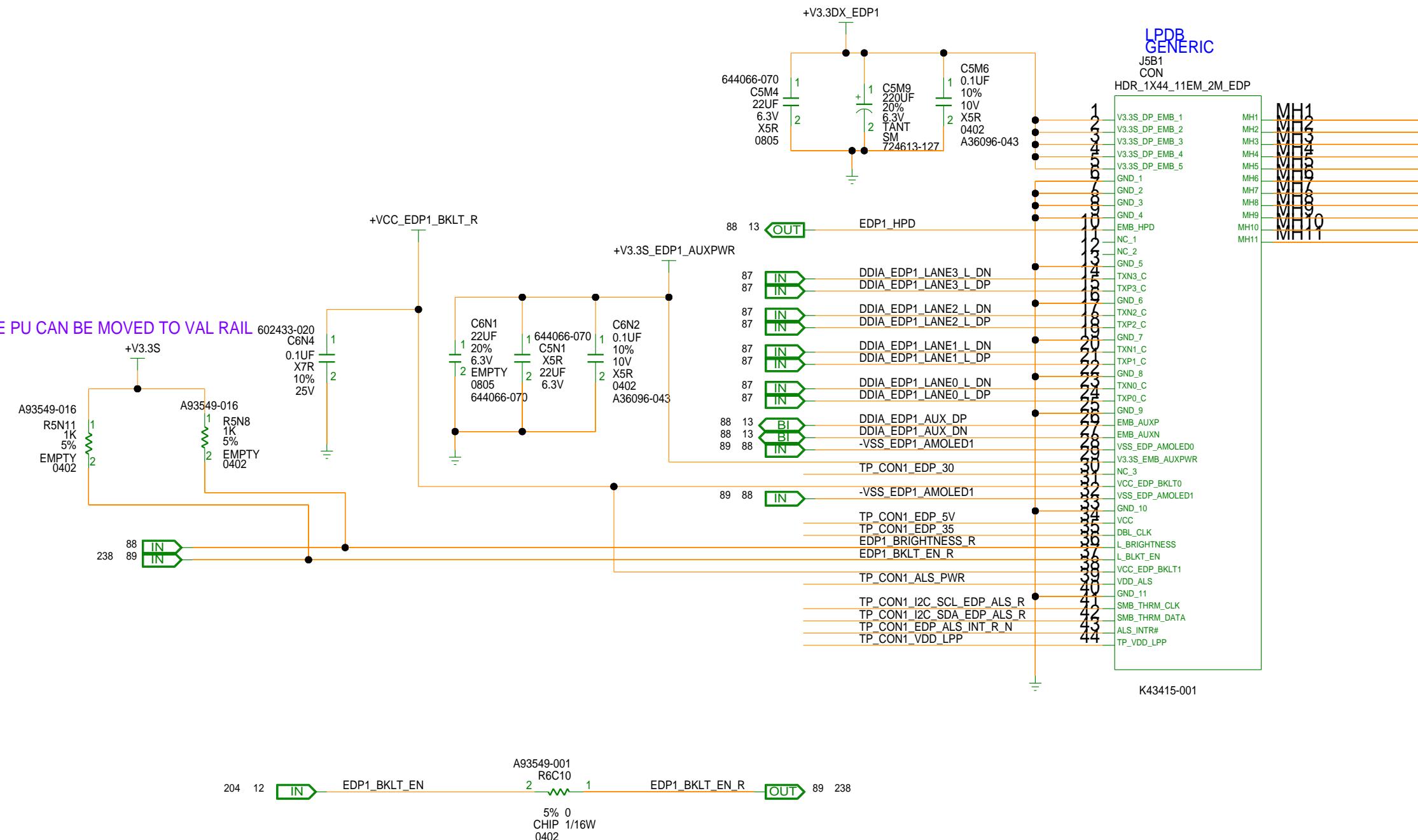
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MODULE NAME	REV	DATE

EDP CONNECTOR 1

CHANGE TANT CAP TO LOWER VALUE

THESE PU CAN BE MOVED TO VAL RAIL



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tigerlake_u_ddr4.sch_1.89
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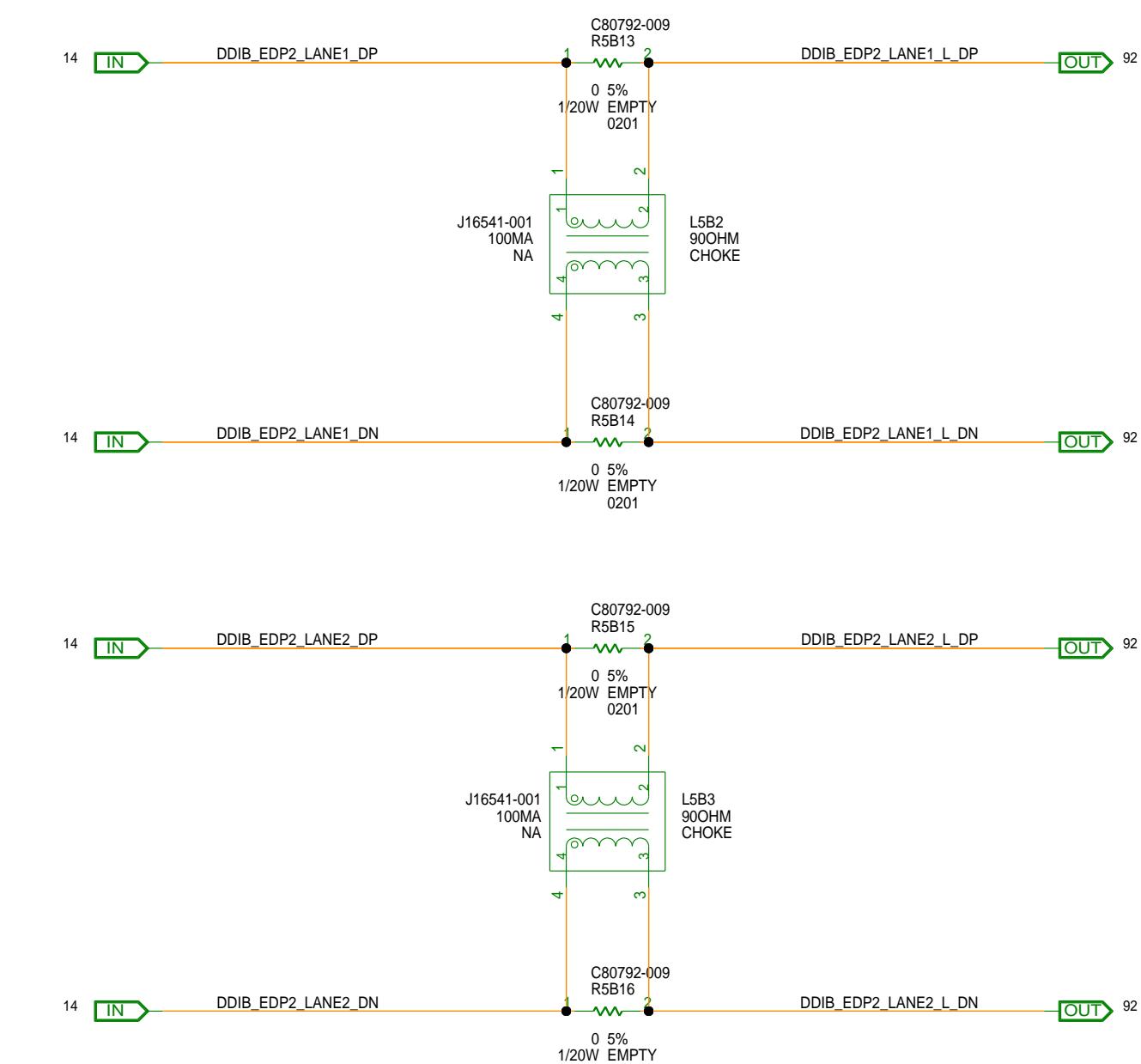
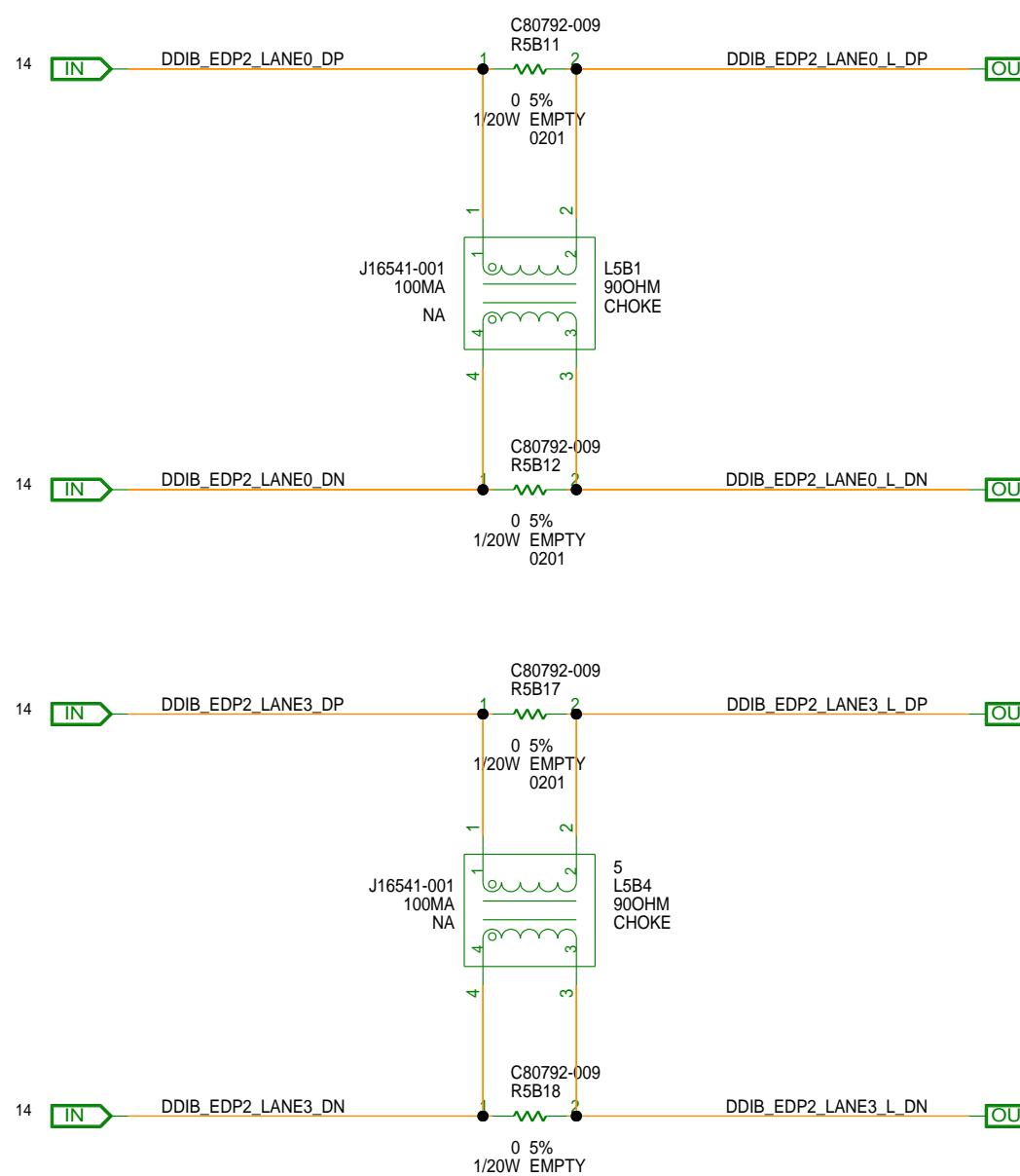
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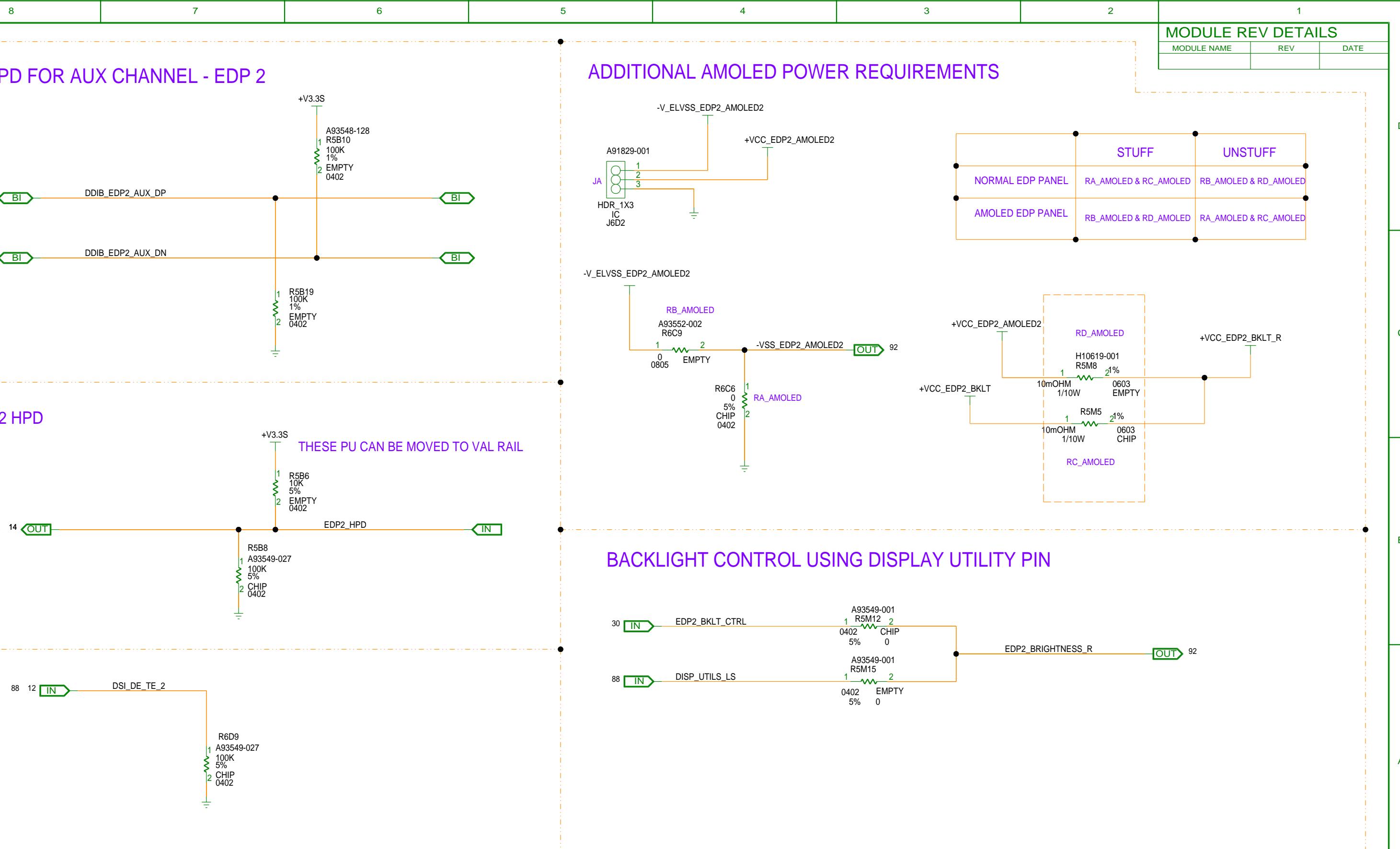
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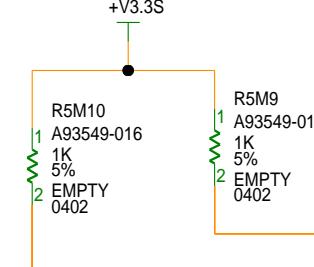


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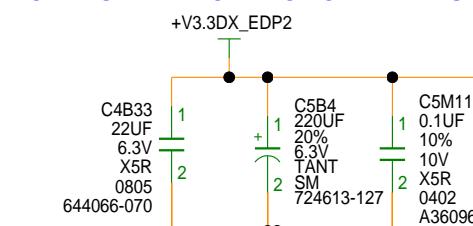
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EDP CONNECTOR 2

THESE PU CAN BE MOVED TO VAL RAIL



CHANGE TANT CAP TO LOWER VALUE



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A36096-043

J4B1 CON

HDR_1X44_11EM_2M_EDP

MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9 MH10 MH11

V3.3S_DP_EMB_1 V3.3S_DP_EMB_2 V3.3S_DP_EMB_3 V3.3S_DP_EMB_4 V3.3S_DP_EMB_5 GND_1 GND_2 GND_3 GND_4 GND_5 NC_1 NC_2 TXN3_C TXP3_C GND_6 TXN2_C TXP2_C GND_7 TXN1_C TXP1_C GND_8 TXN0_C TXP0_C GND_9 EMB_AUXP EMB_AUXN VSS_EDP_AMOLED0 V3.3S_EMB_AUXPWR NC_3 VCC_EDP_BKLT0 VSS_EDP_AMOLED1 GND_10 VCC DBL_CLK L_BRIGHTNESS L_BLKT_EN VCC_EDP_BKLT1 VDD_ALS GND_11 SMB_THRM_CLK SMB_THRM_DATA ALS_INTR# TP_VDD_LPP

K43415-001

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MODULE REV DETAILS

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MODULE REV DETAILS		
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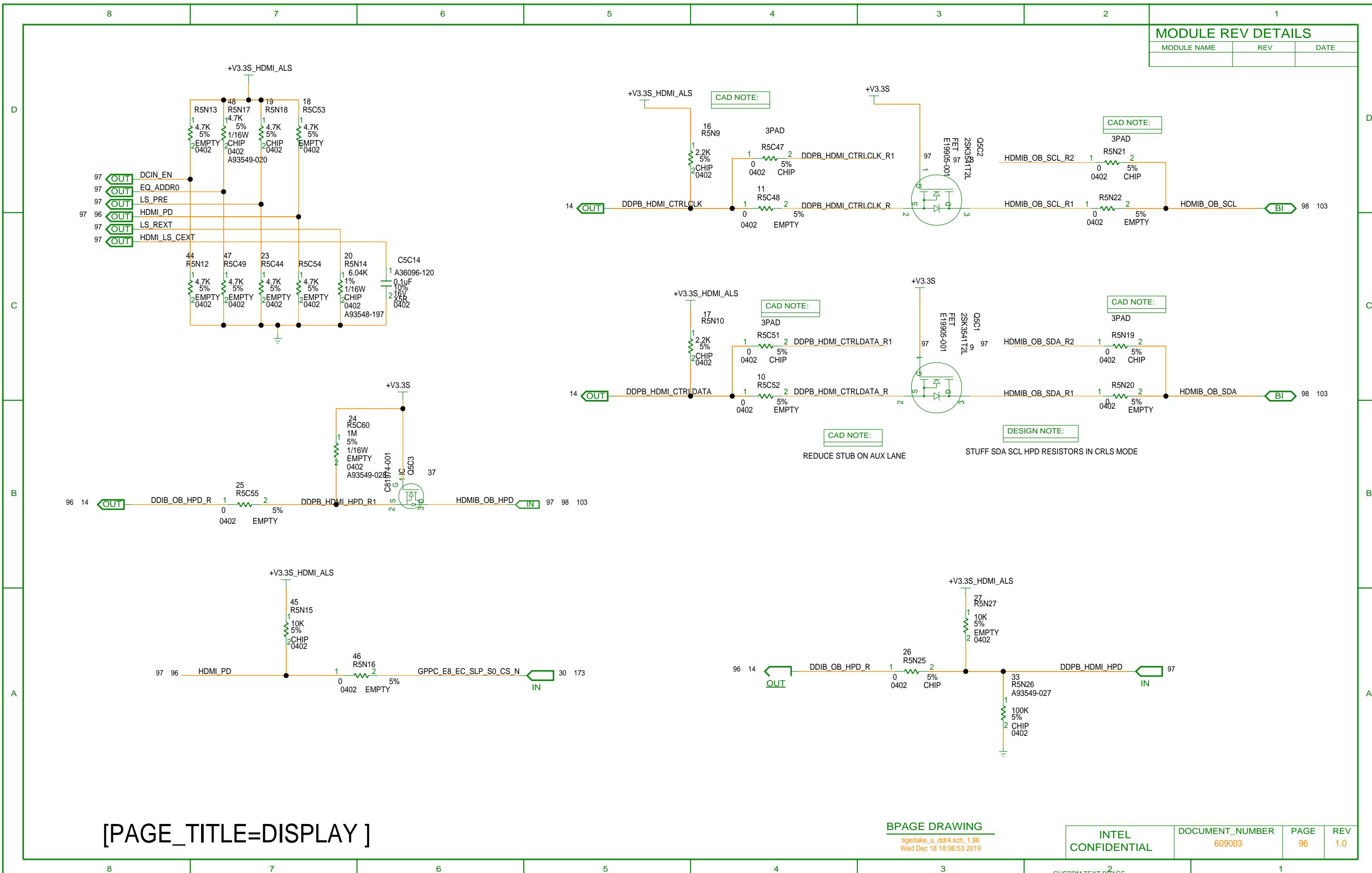
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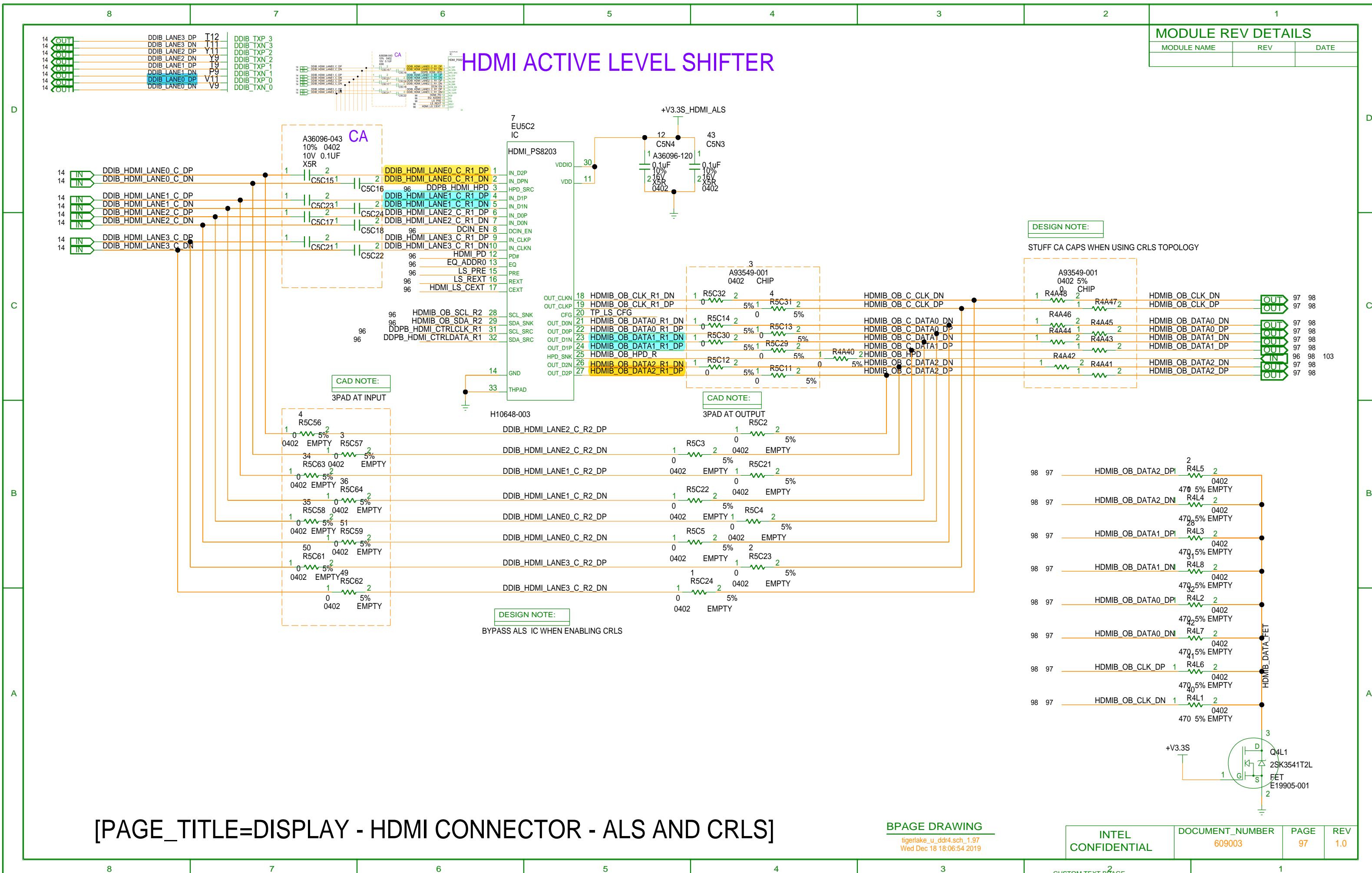
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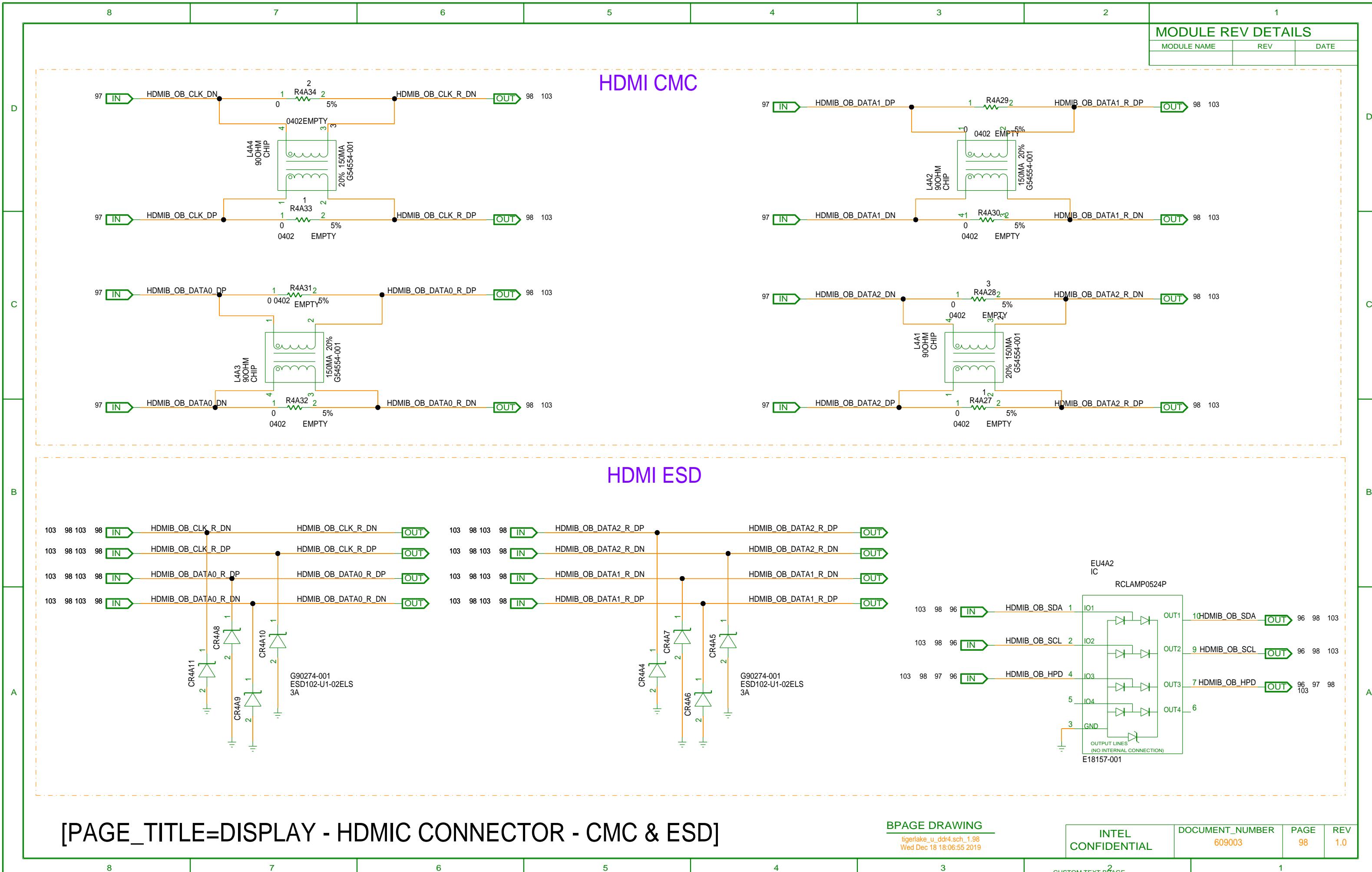
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

DP CONNECTOR 2 - CMC

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CUSTOM TEXT 2 PAGE

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MODULE REV DETAILS		
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DISPLAY - DDI 1&2 HPD & CONNECTOR

MODULE REV DETAILS

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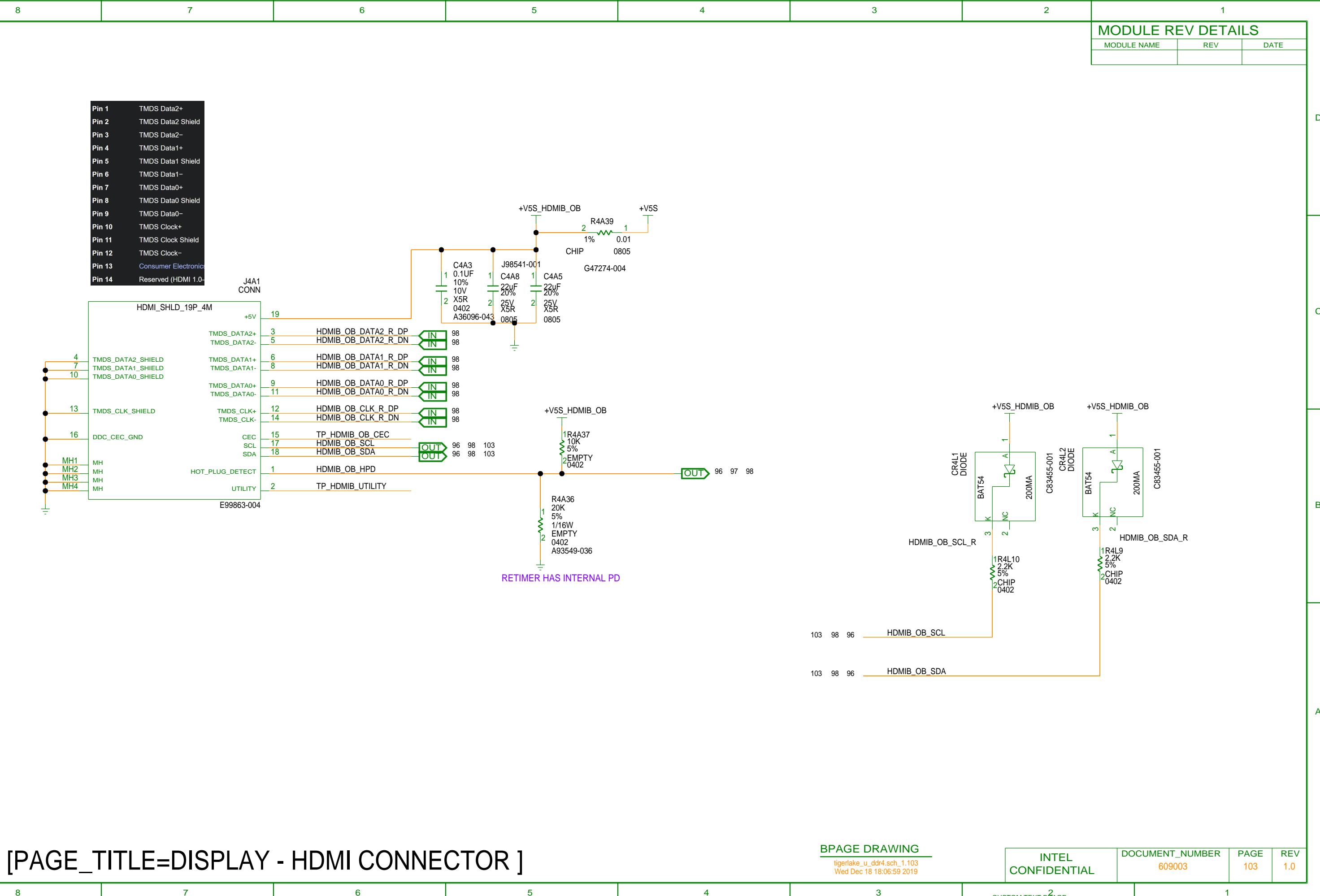
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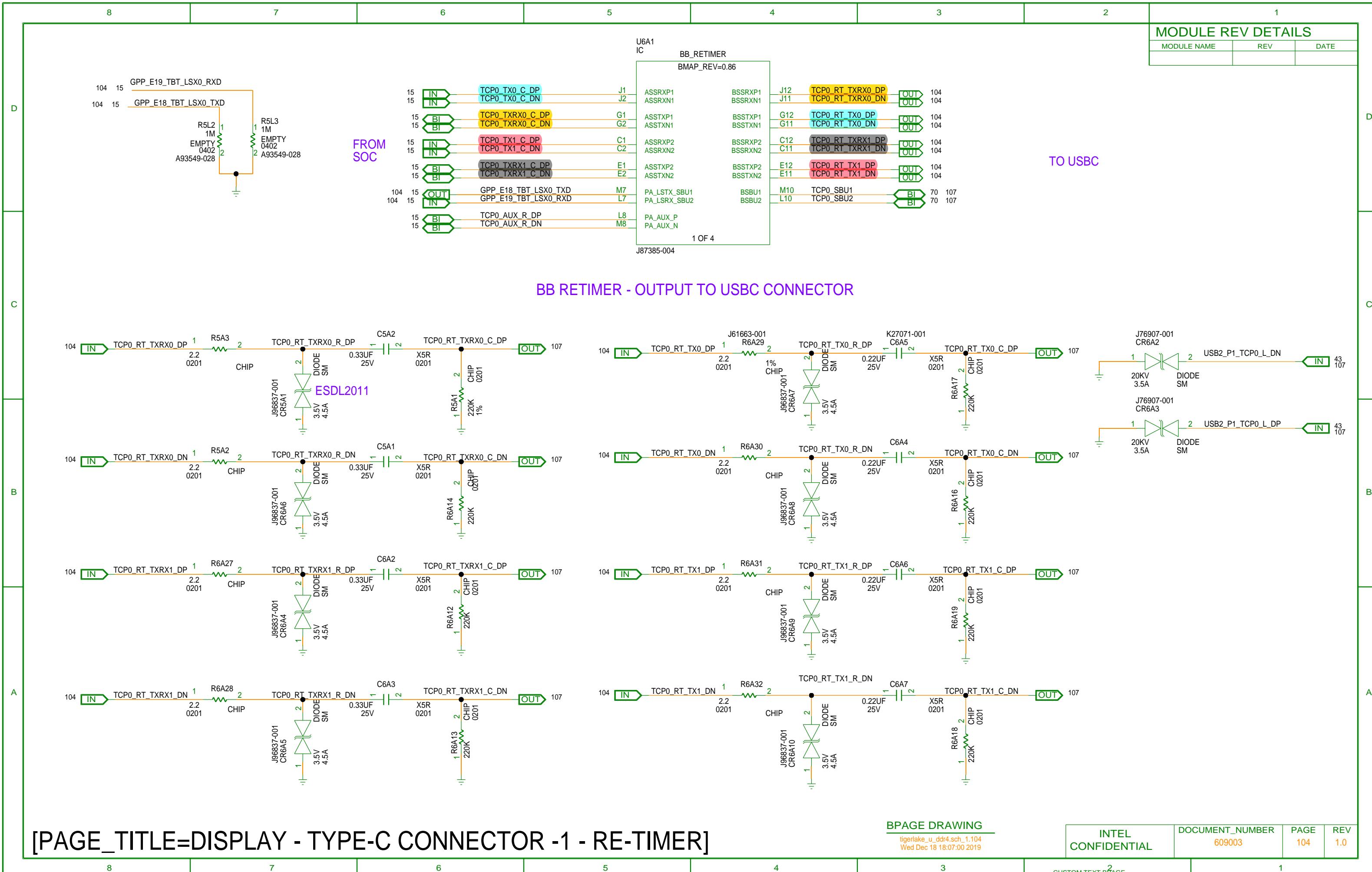
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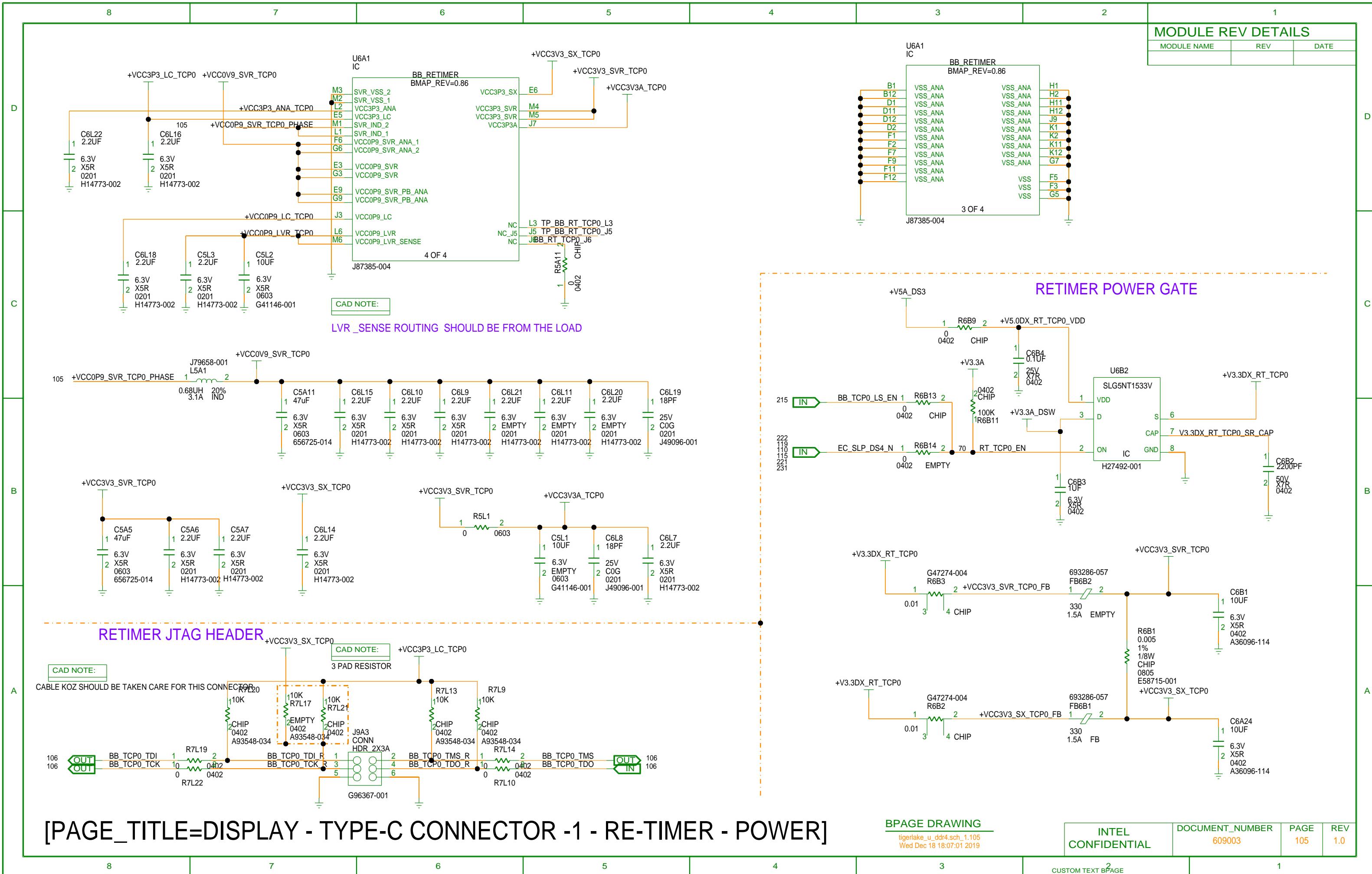
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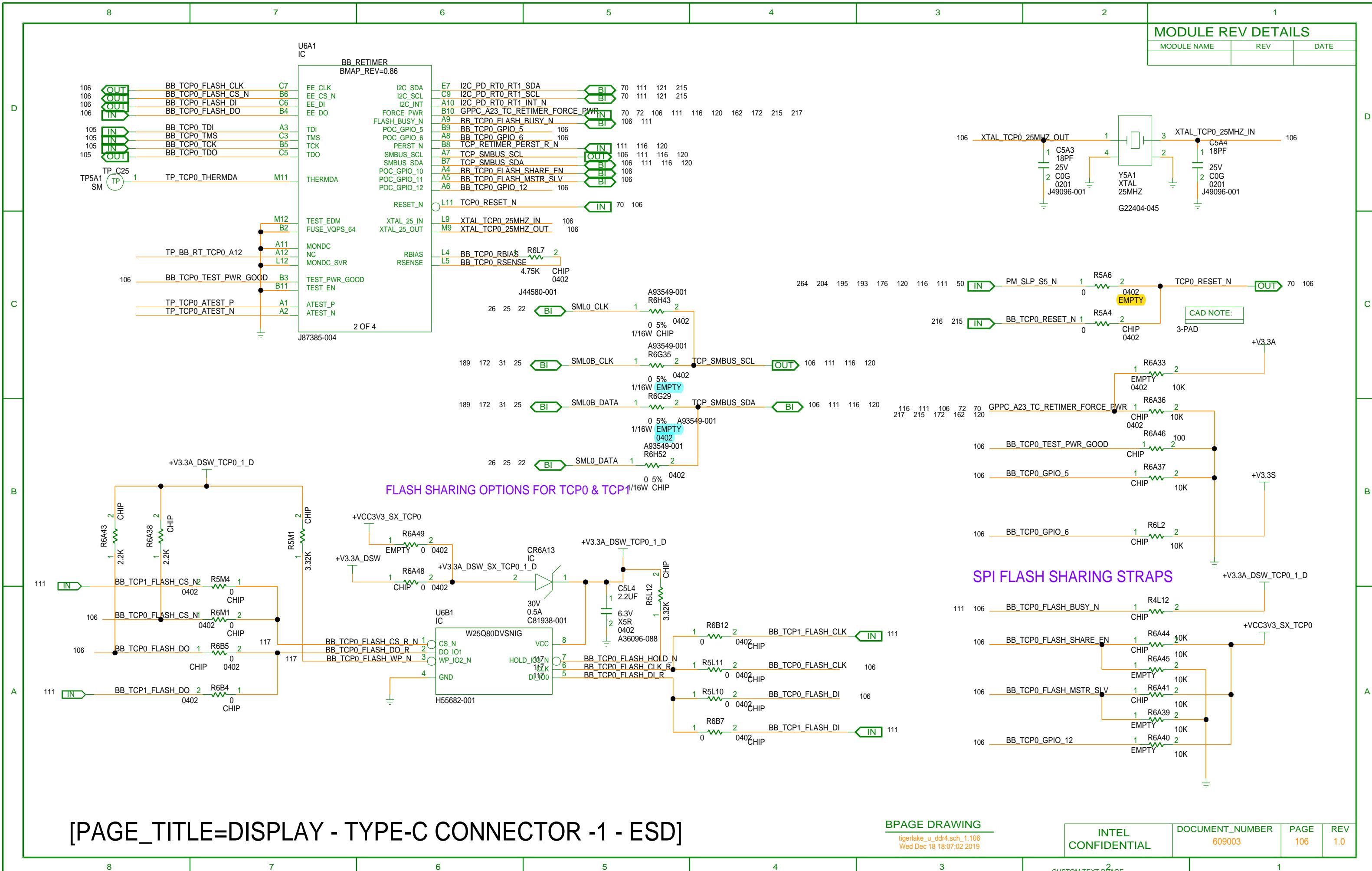
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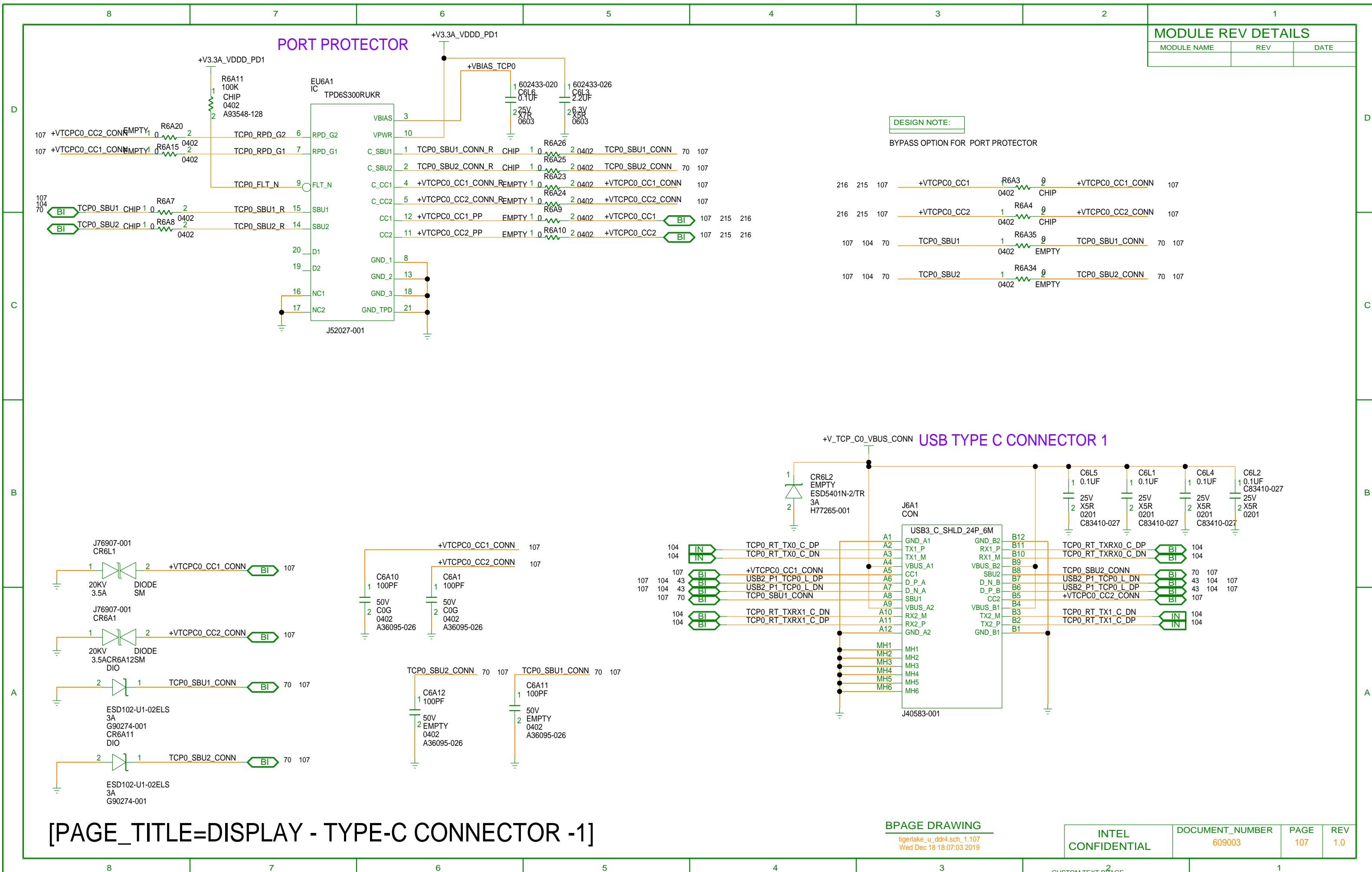
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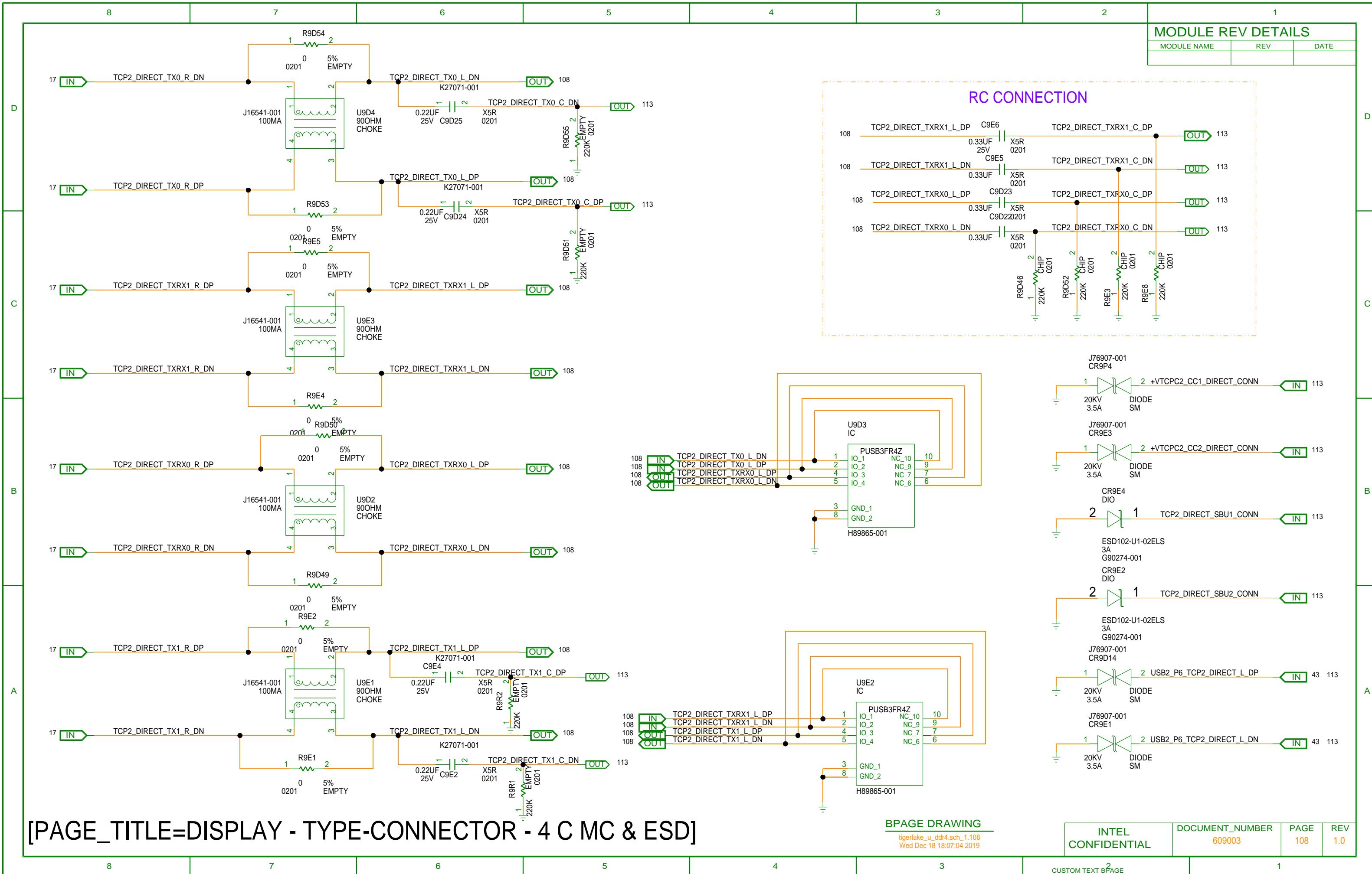


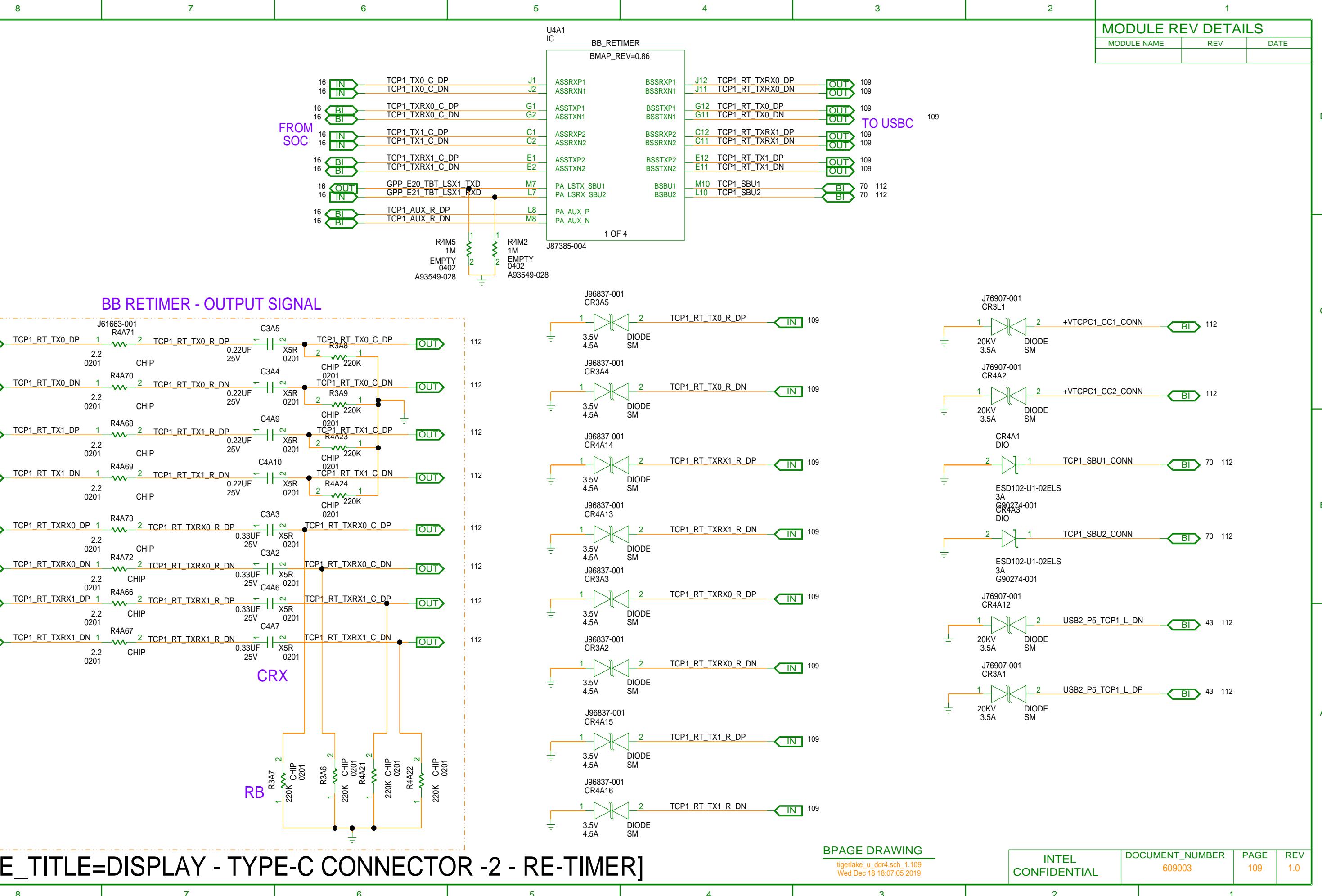


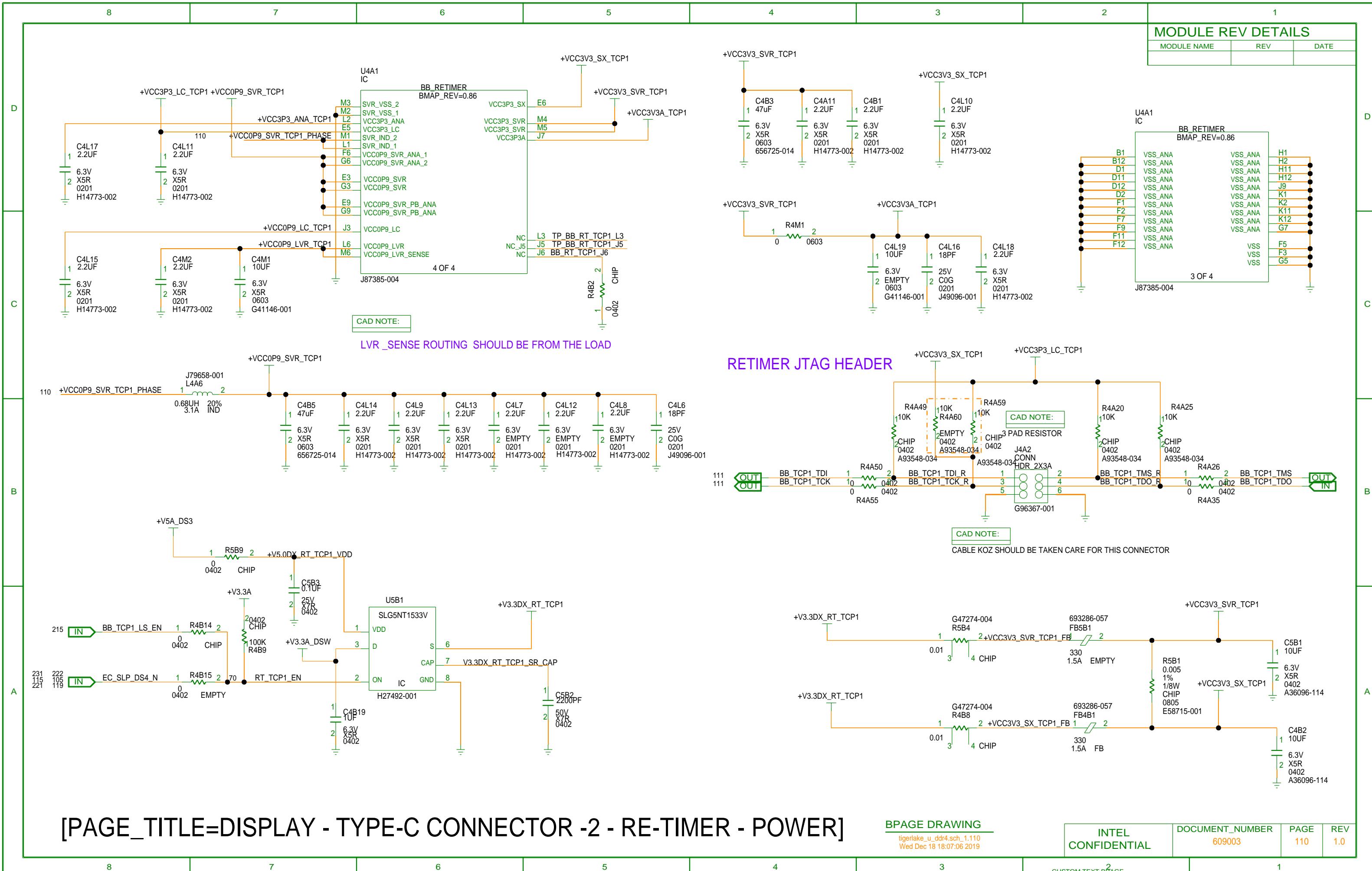


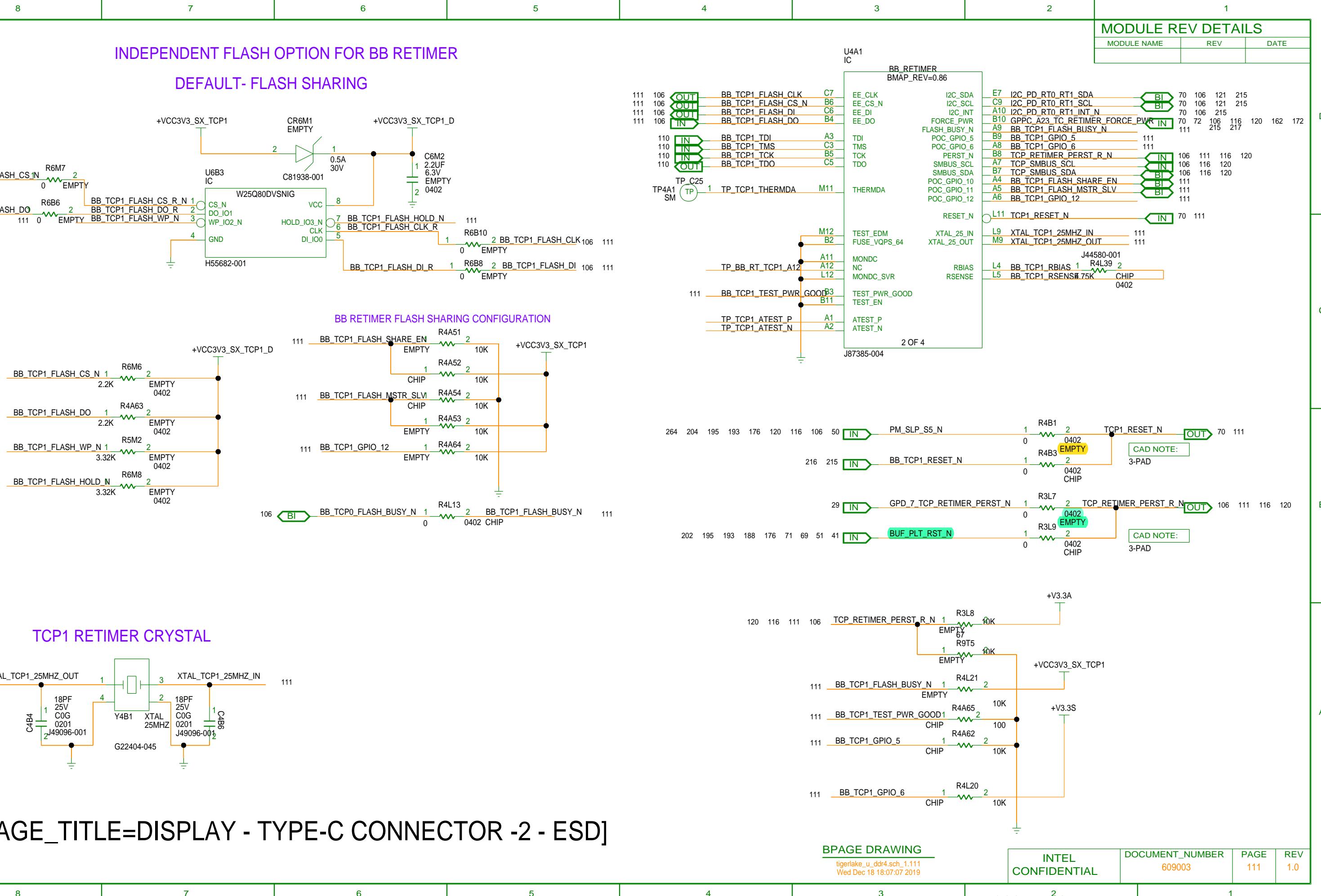


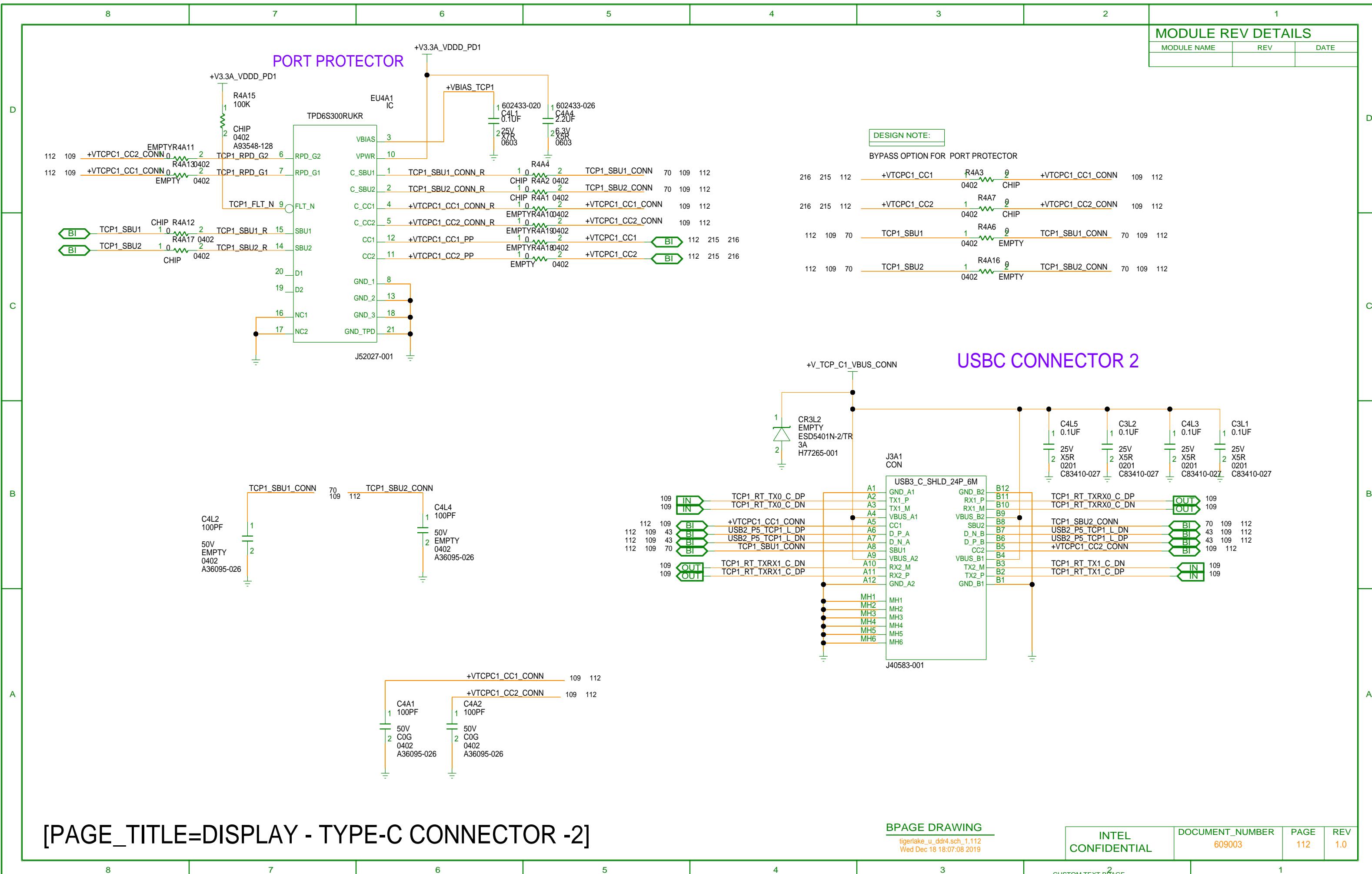


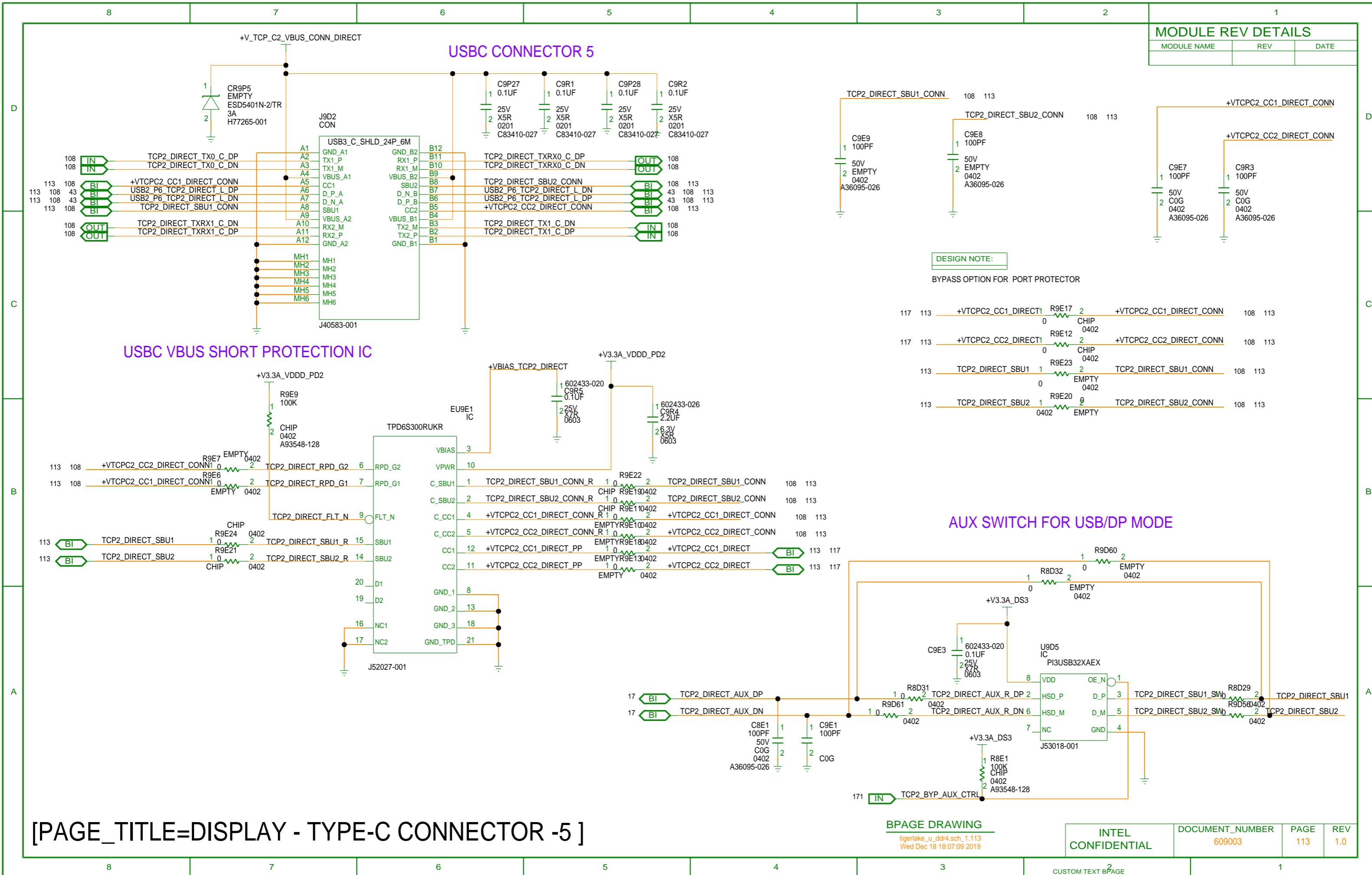


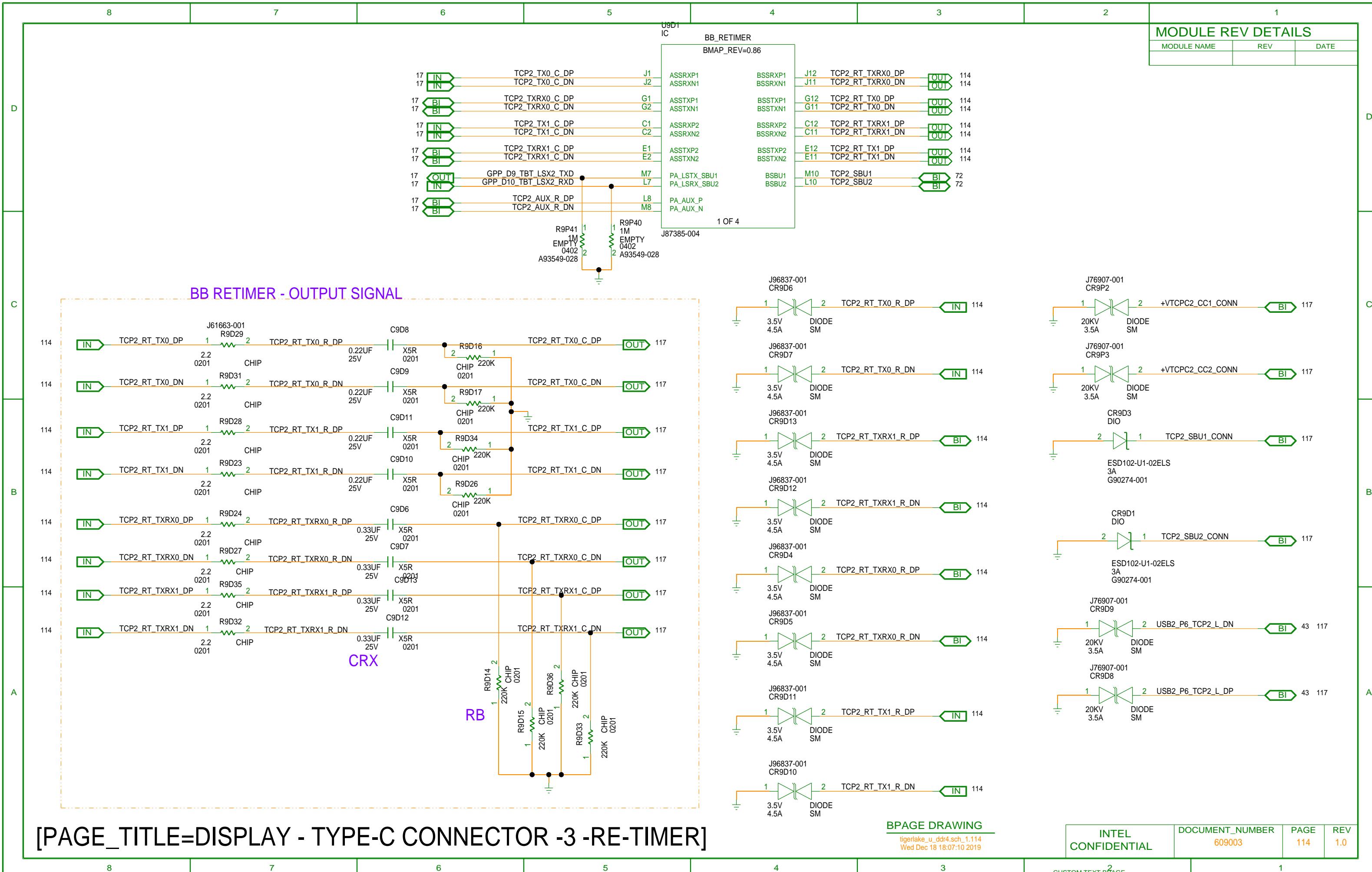


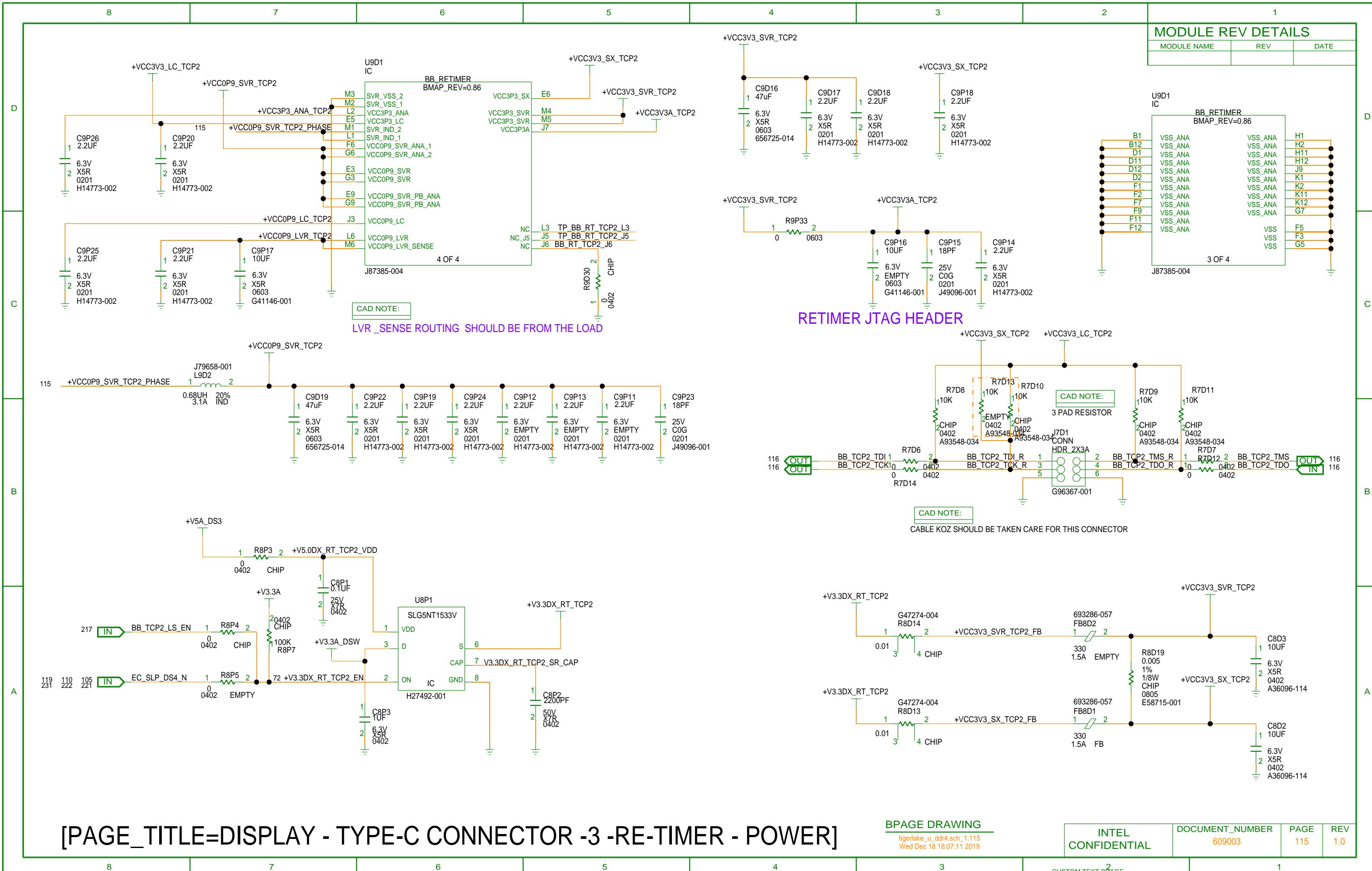


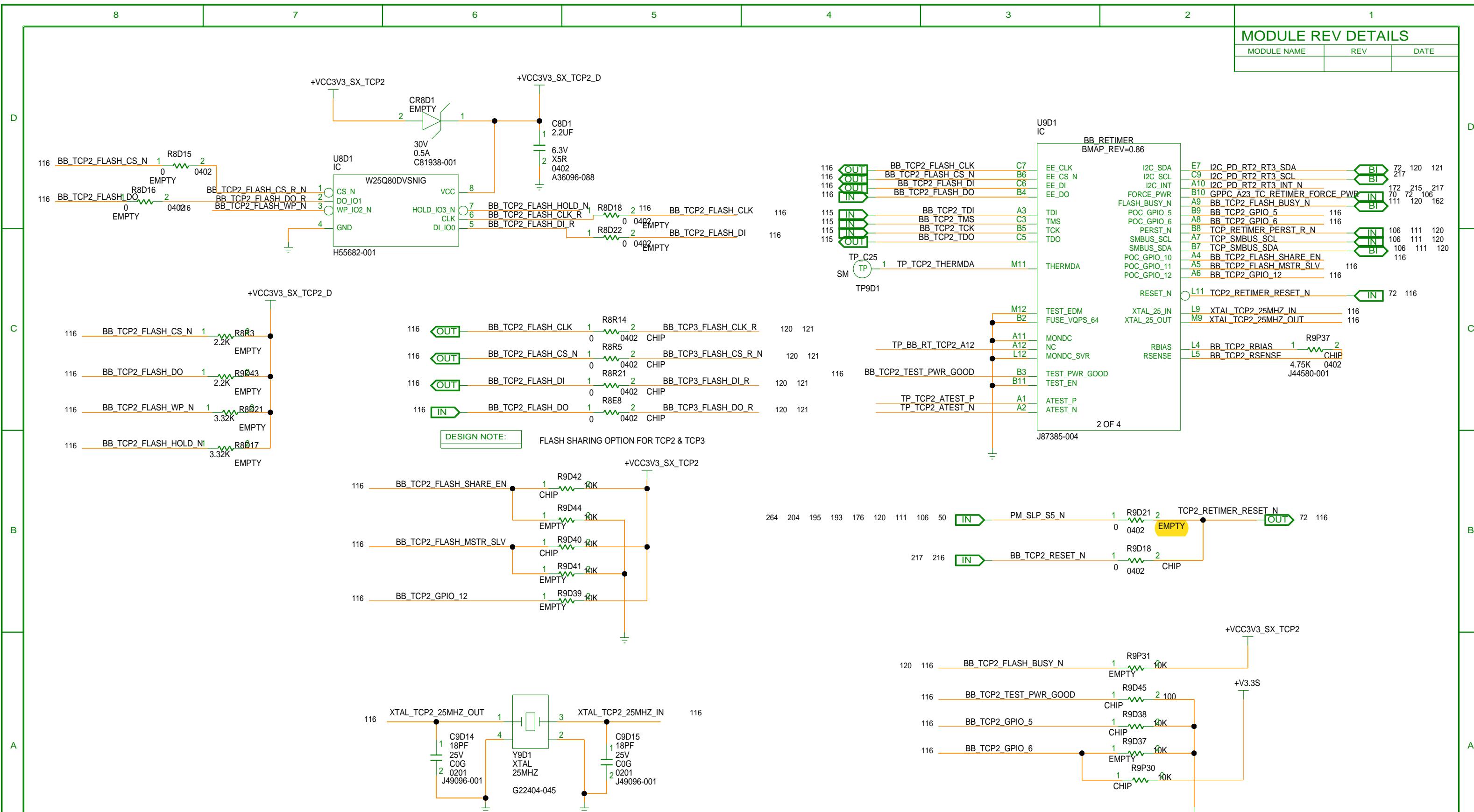










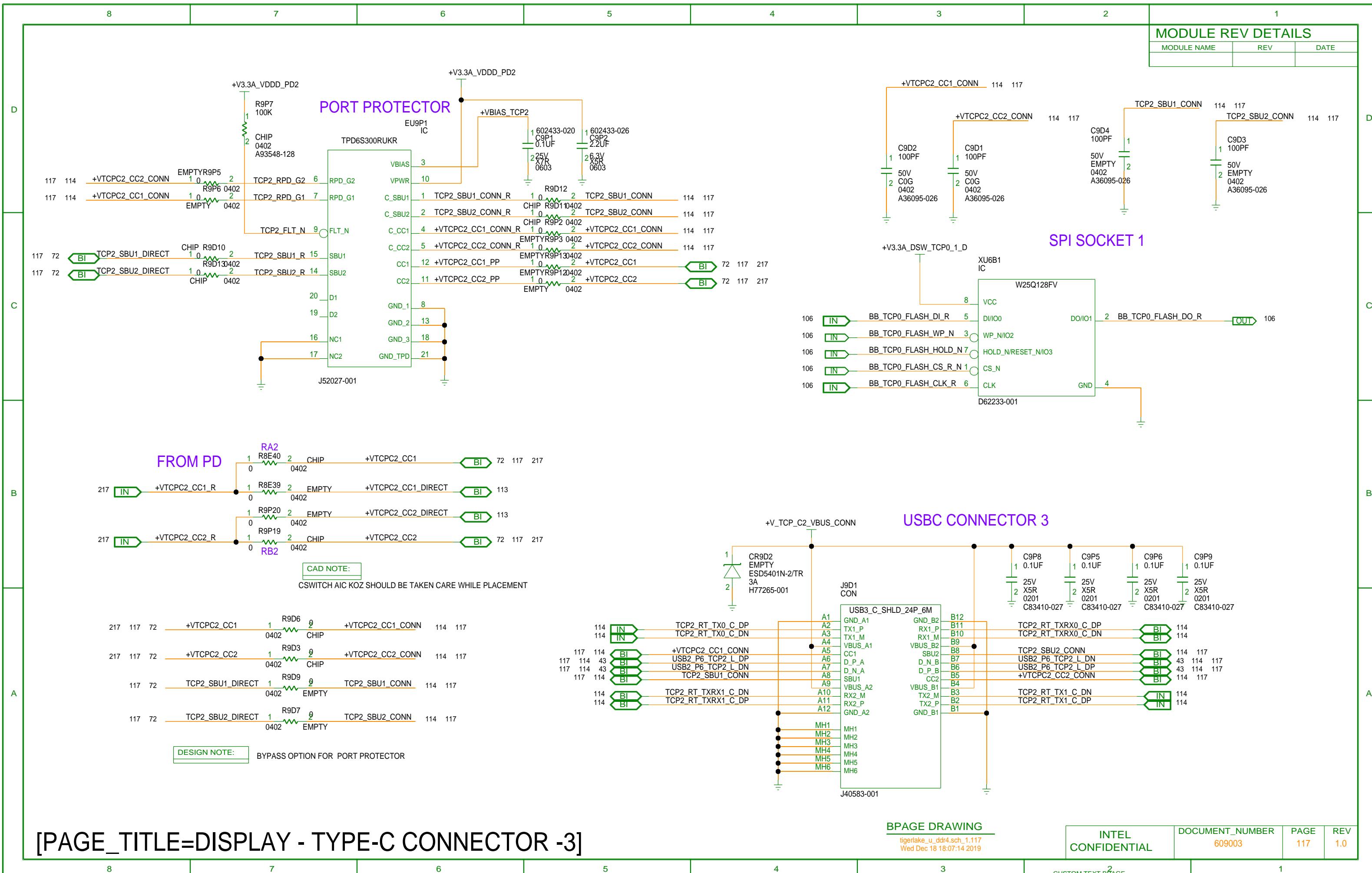


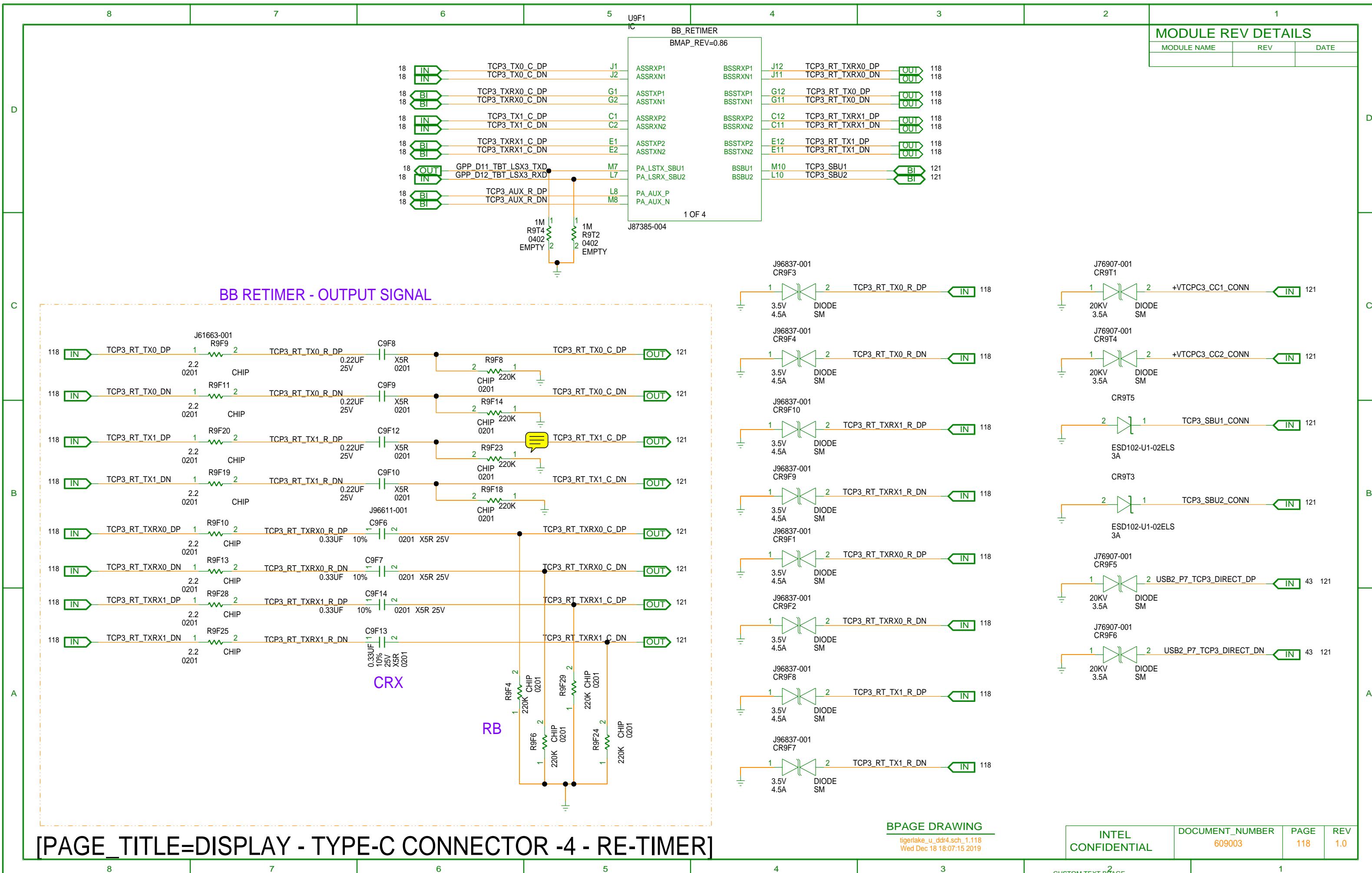
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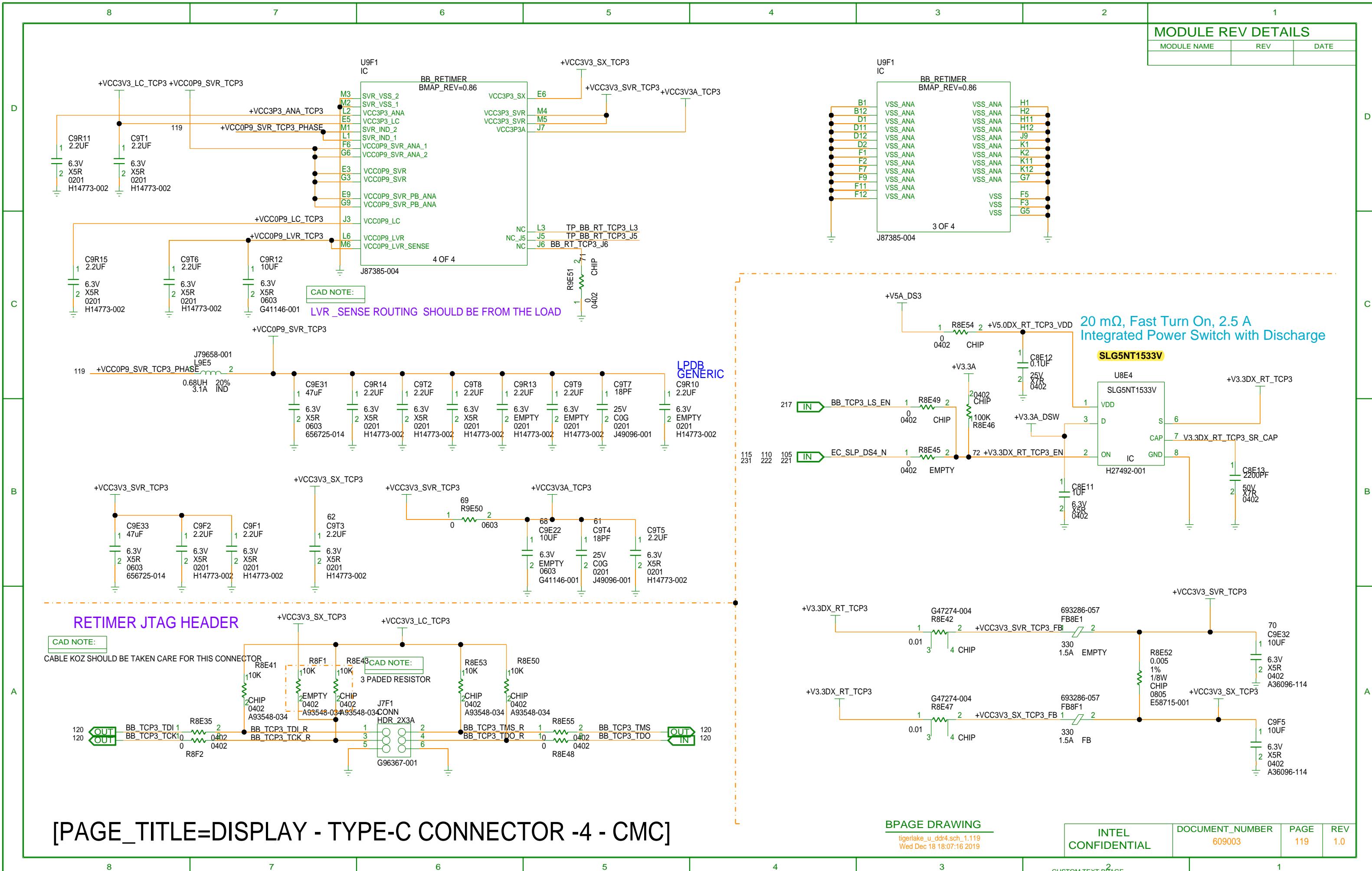
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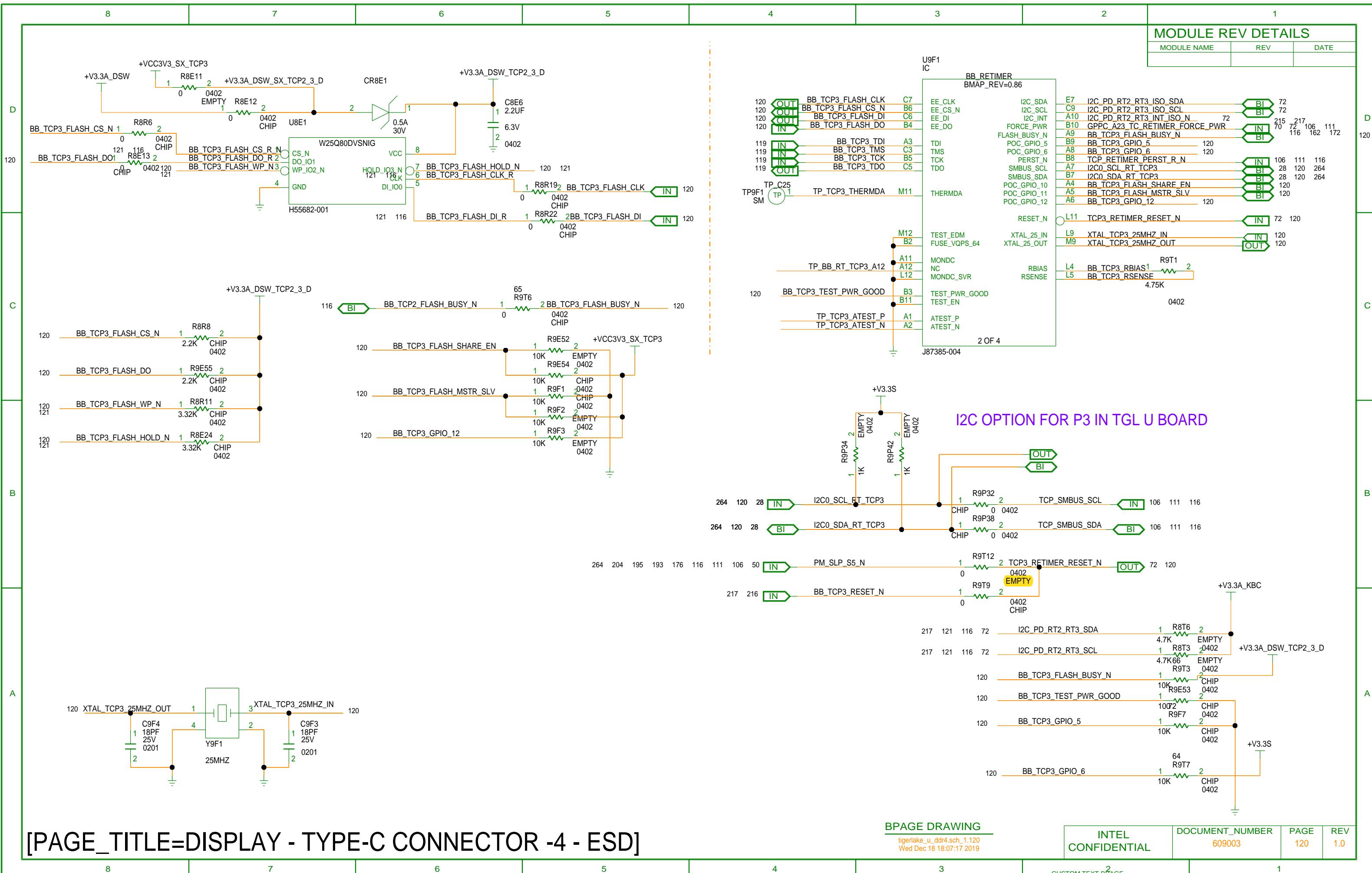
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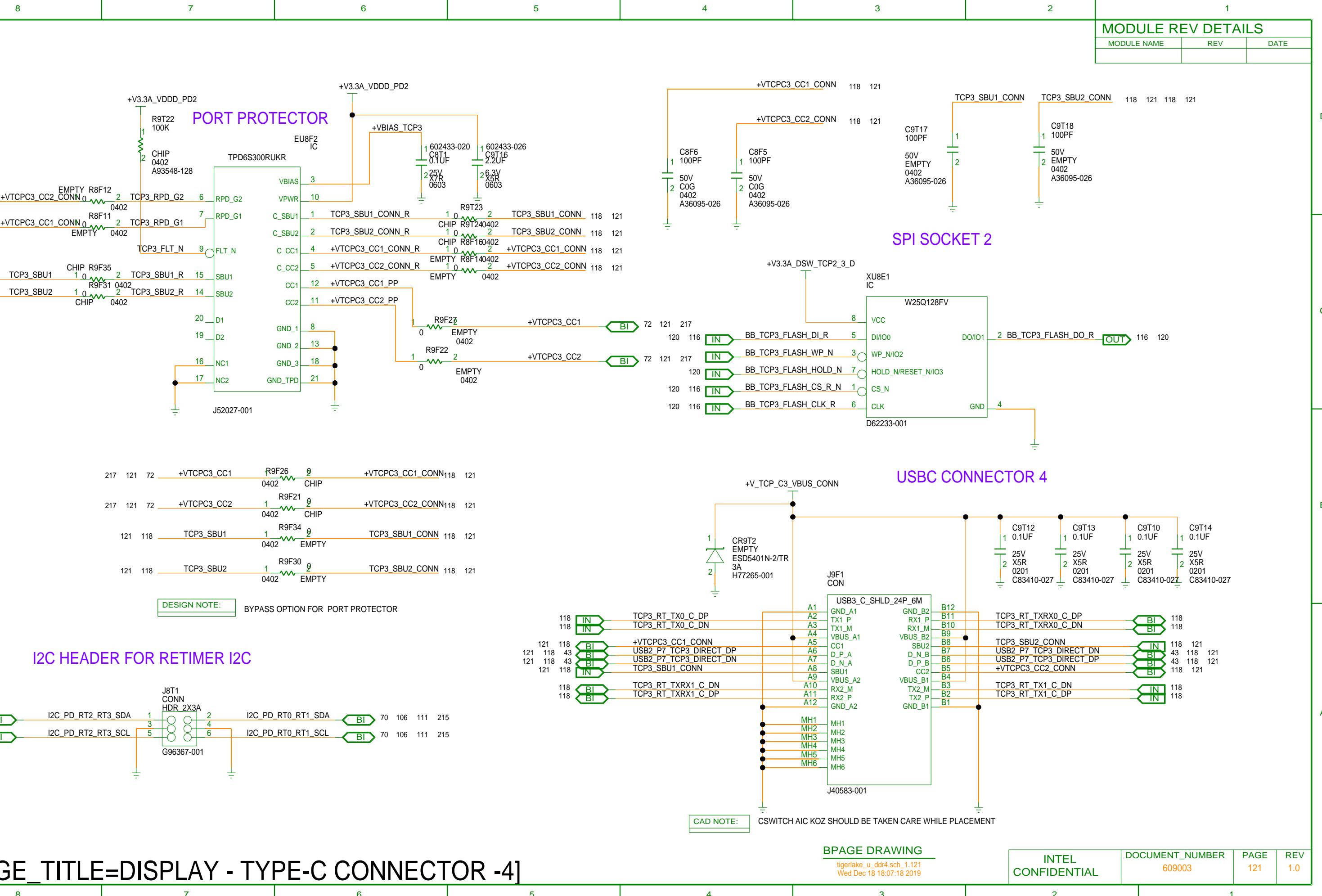
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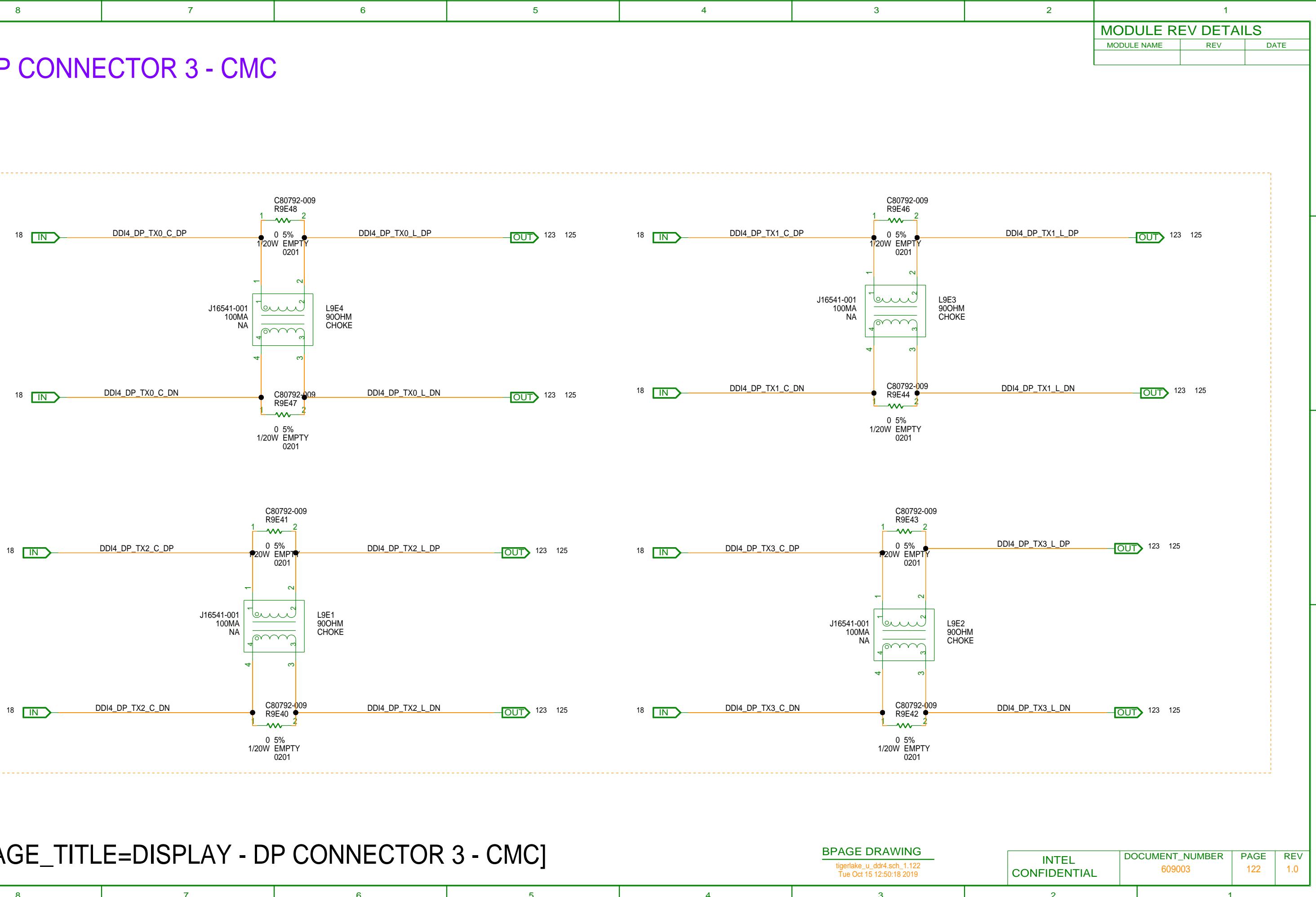












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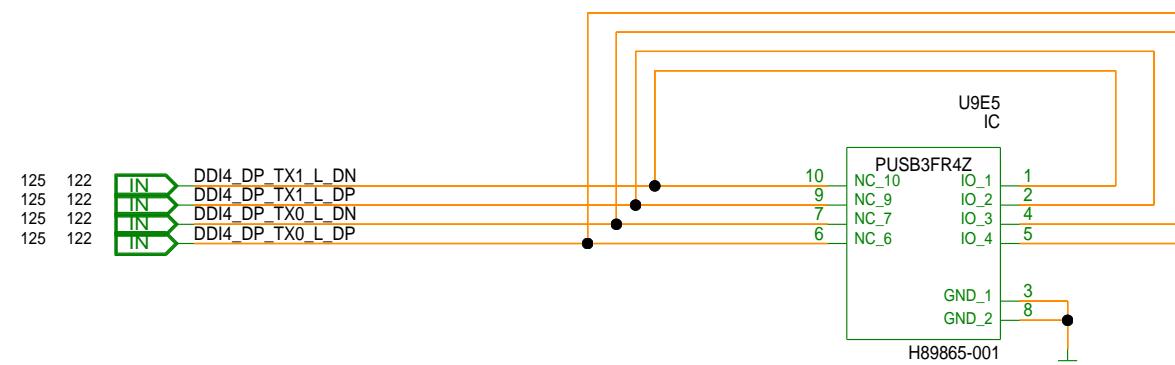
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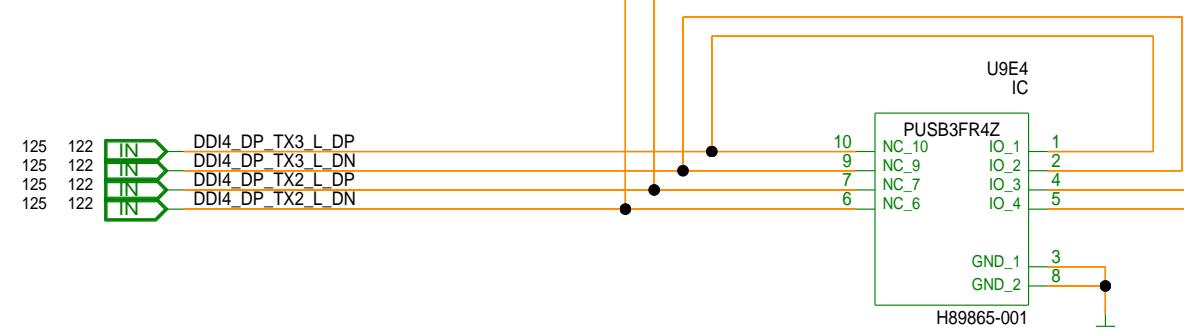
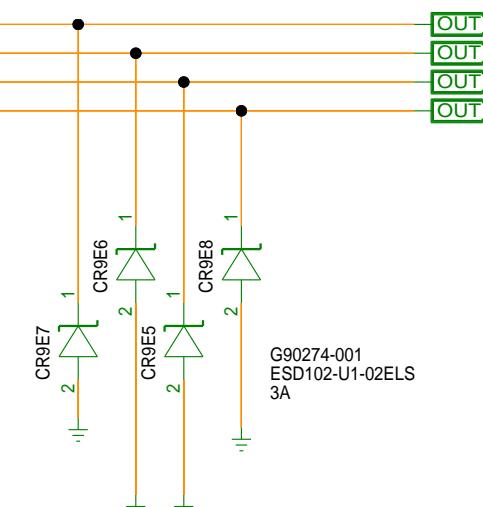
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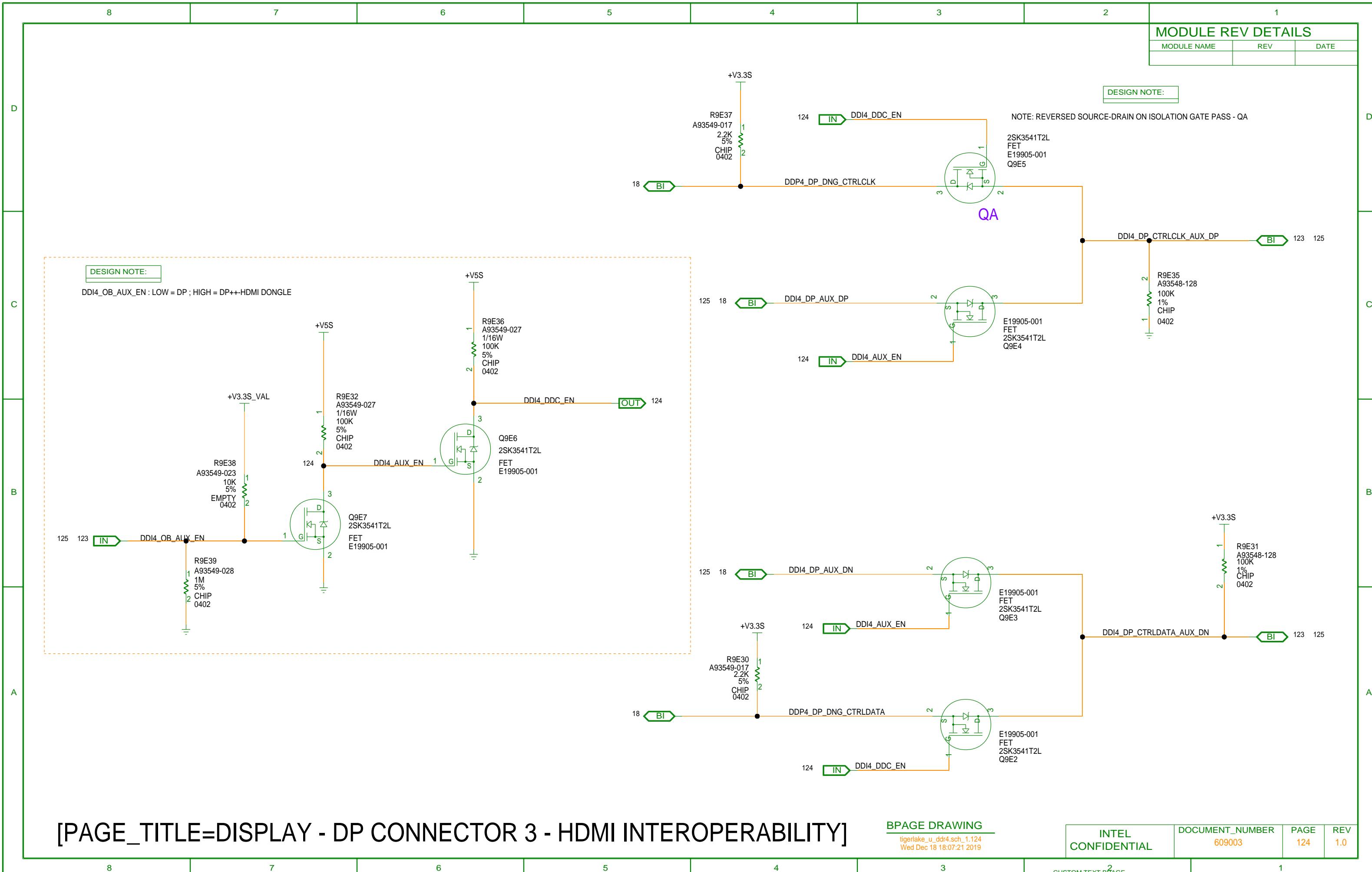
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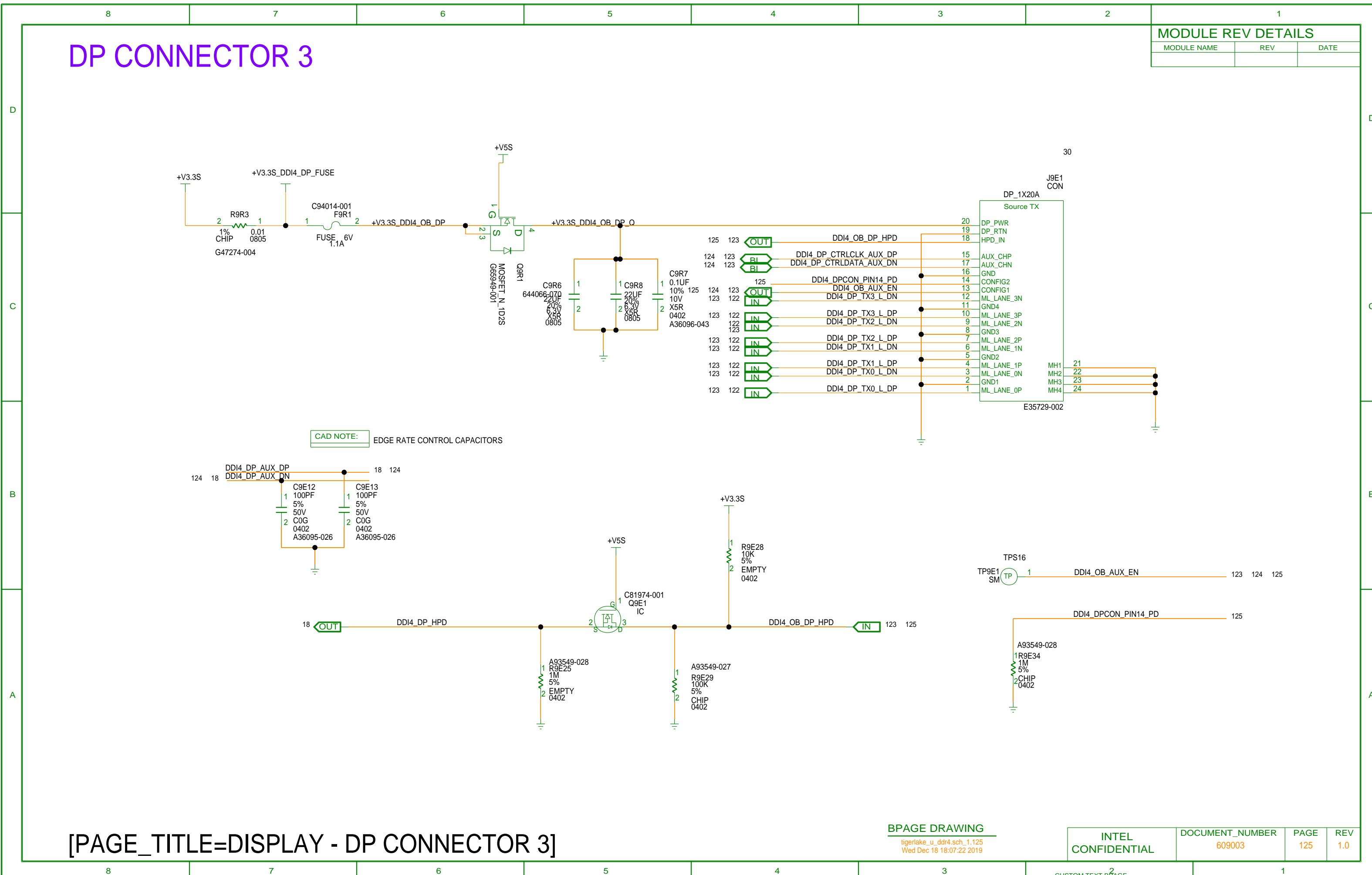
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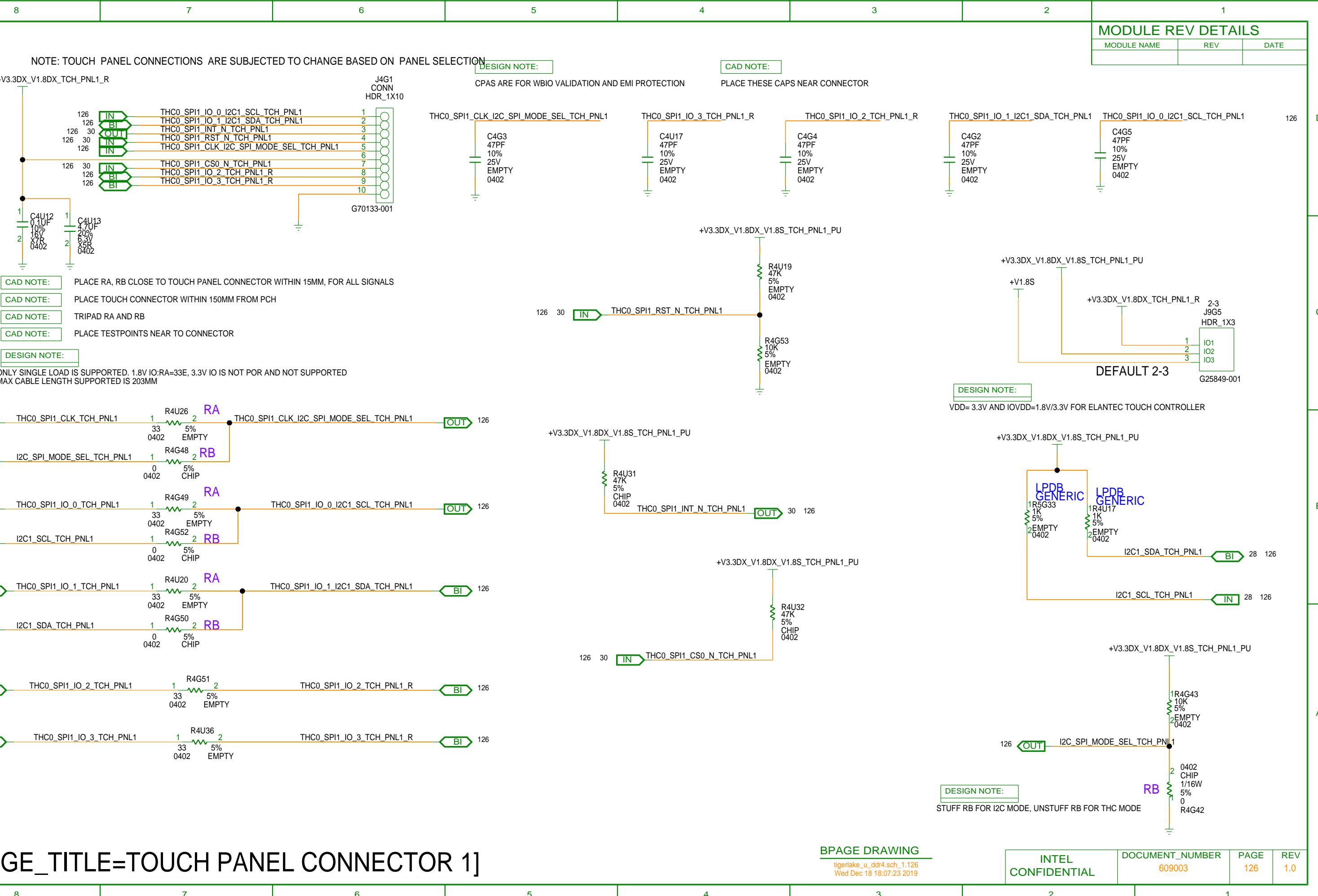


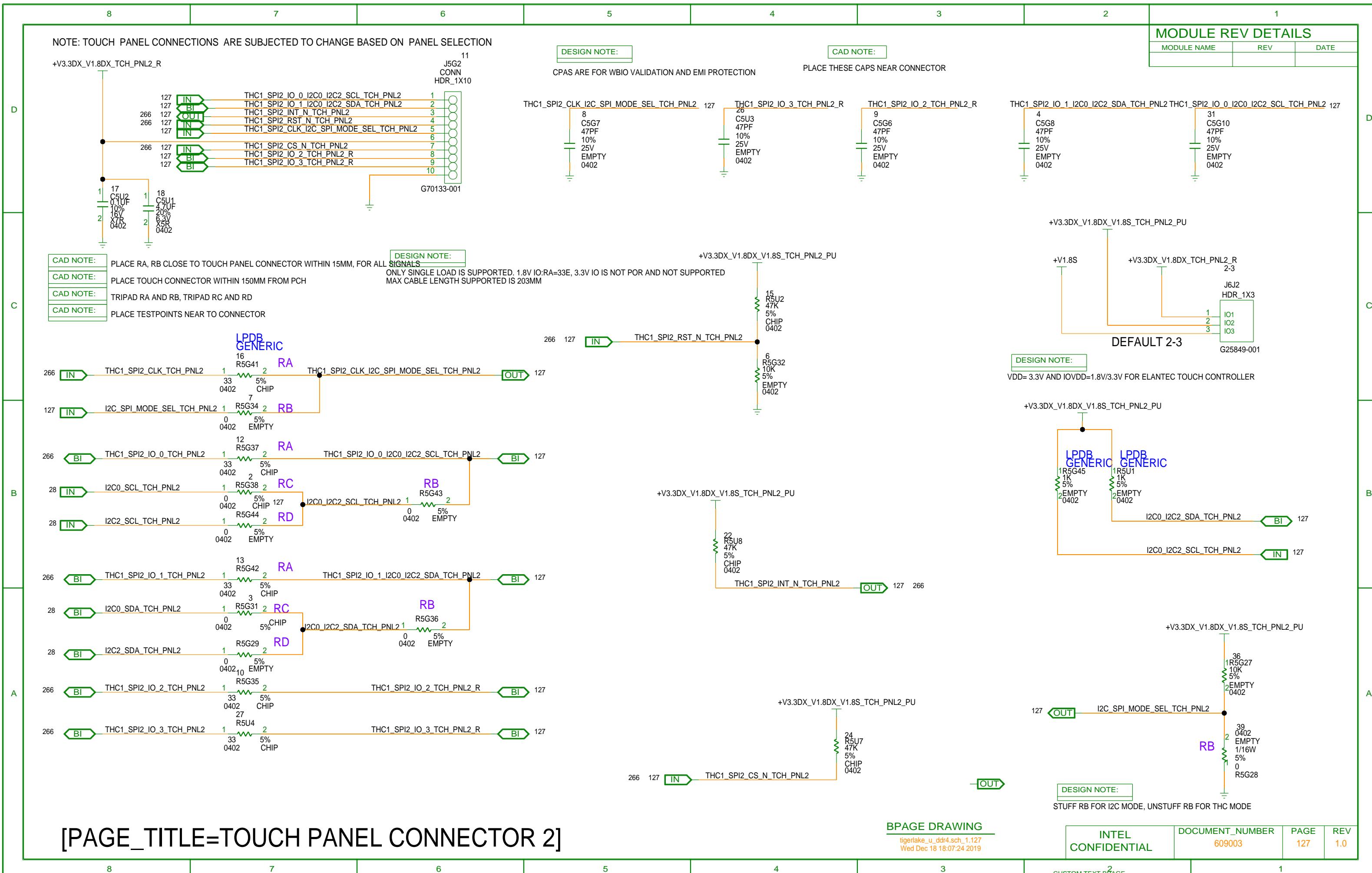
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125 124 [IN] DDI4_DP_CTRLCLK_AUX_DP

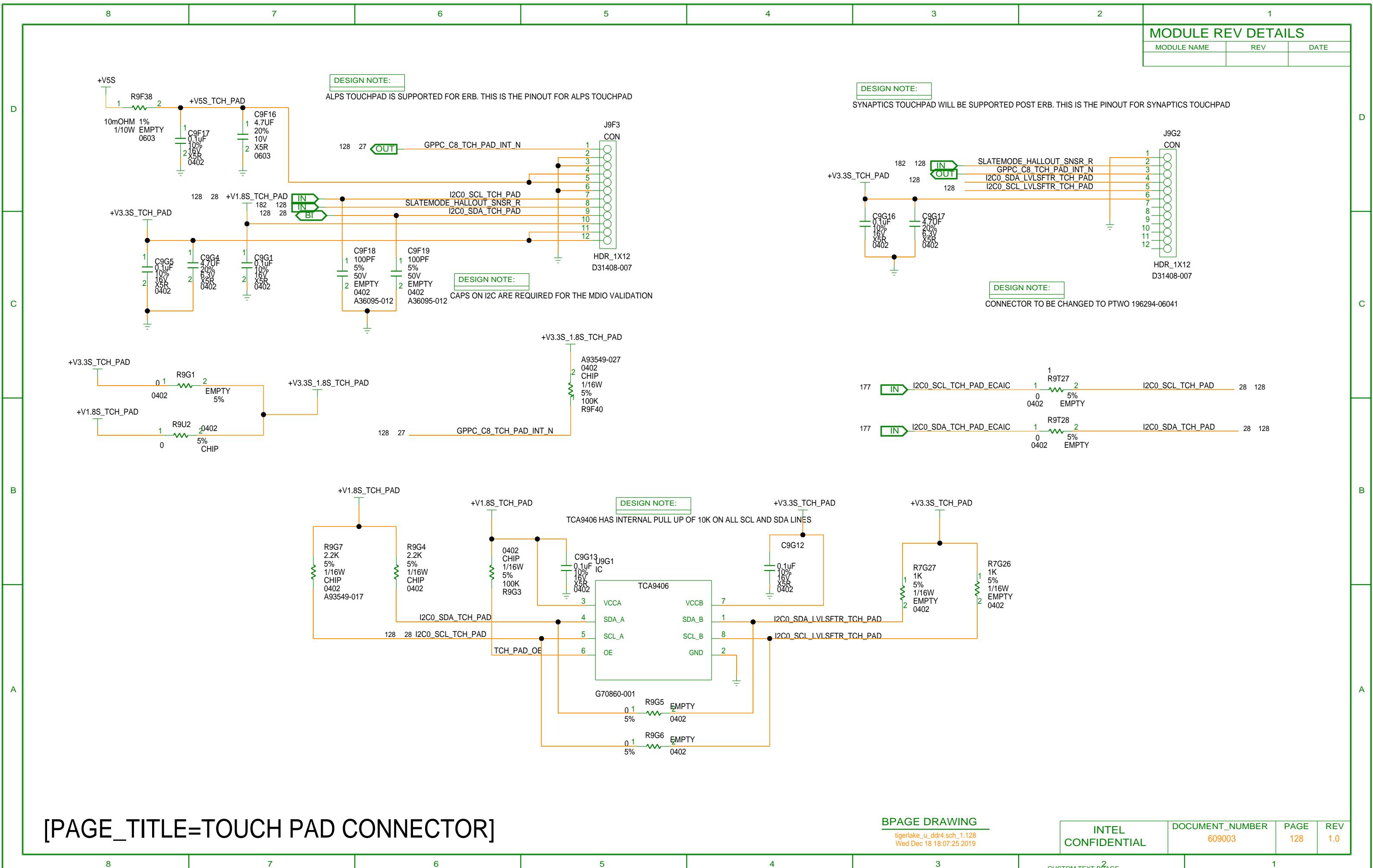


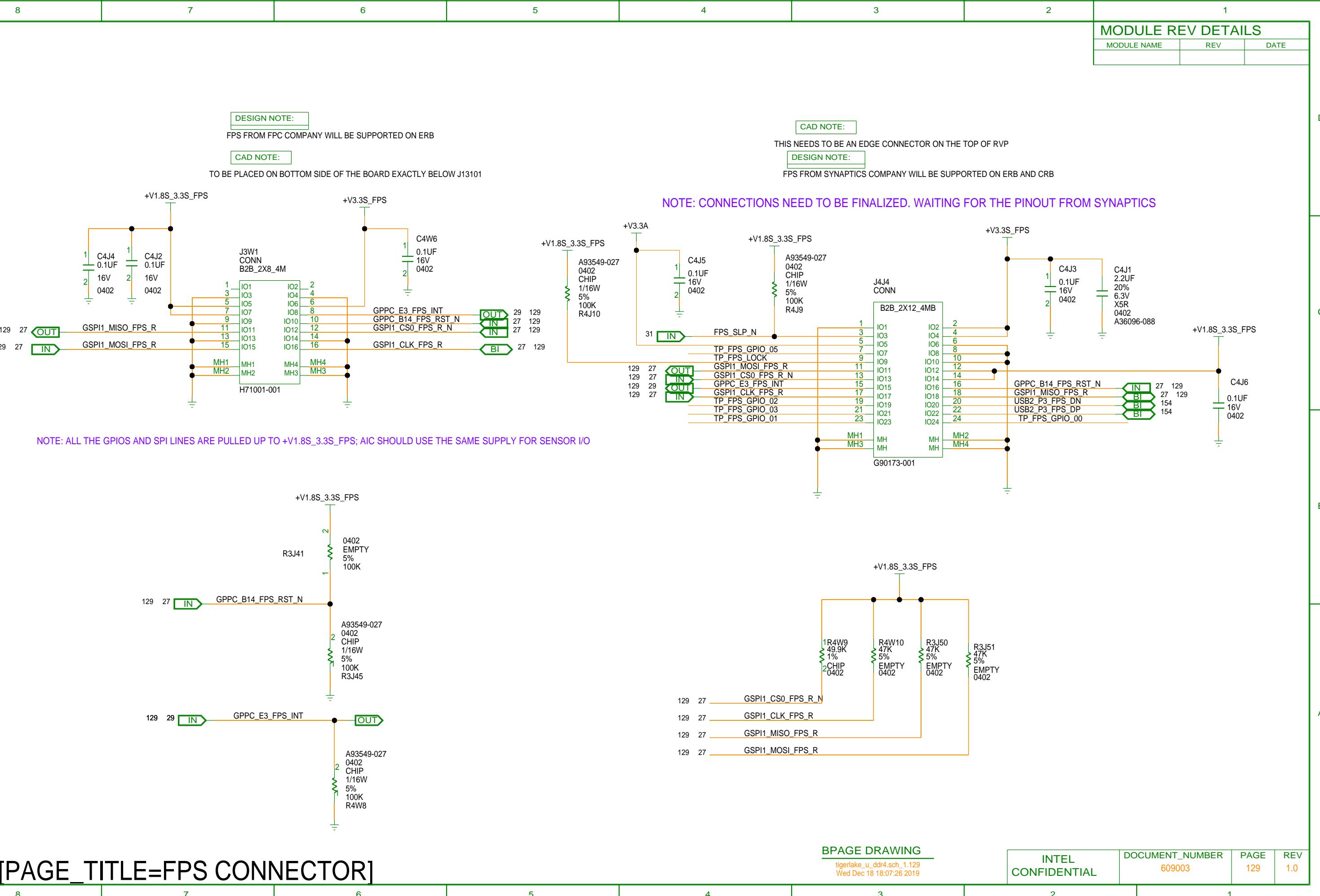


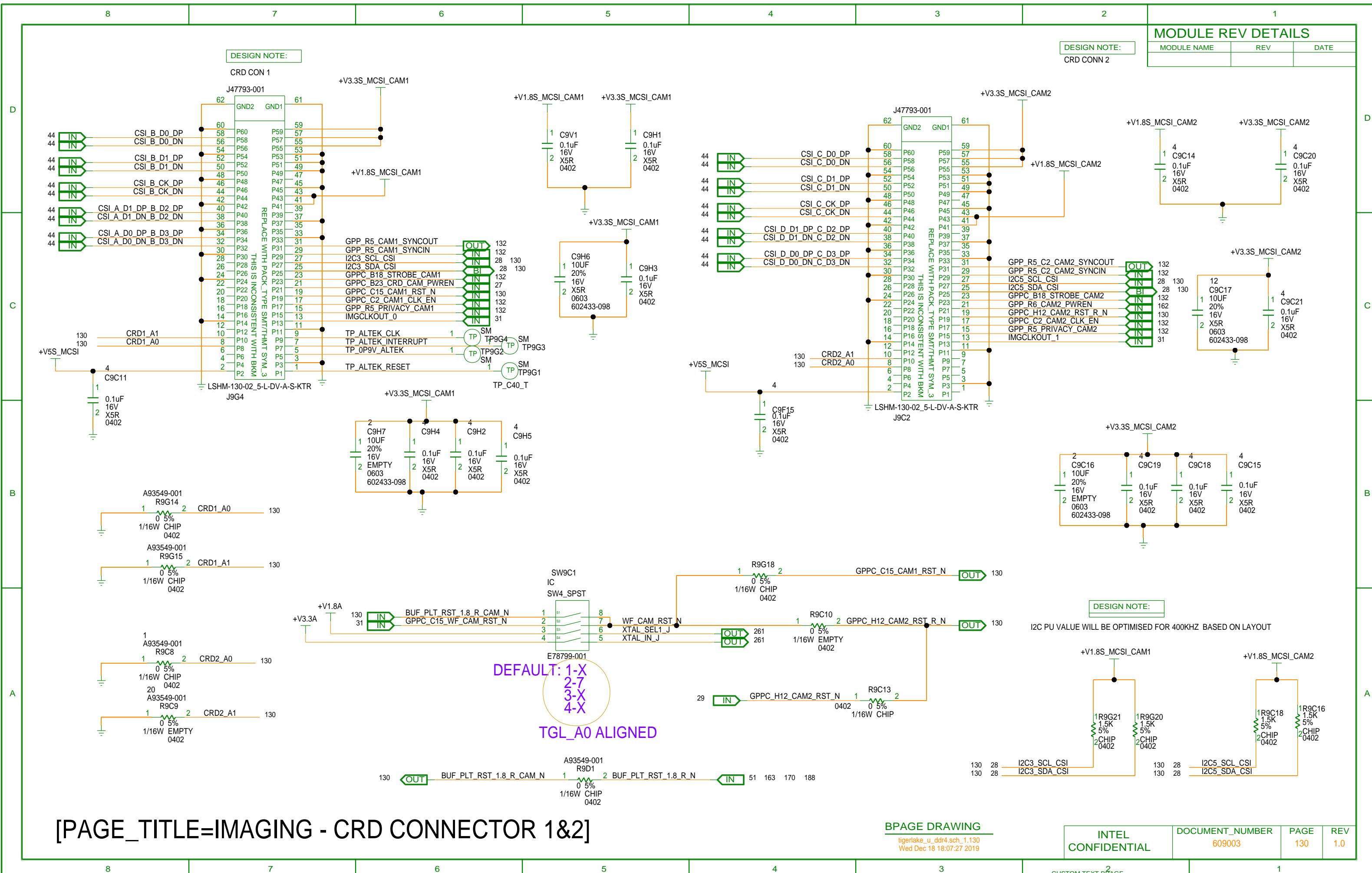








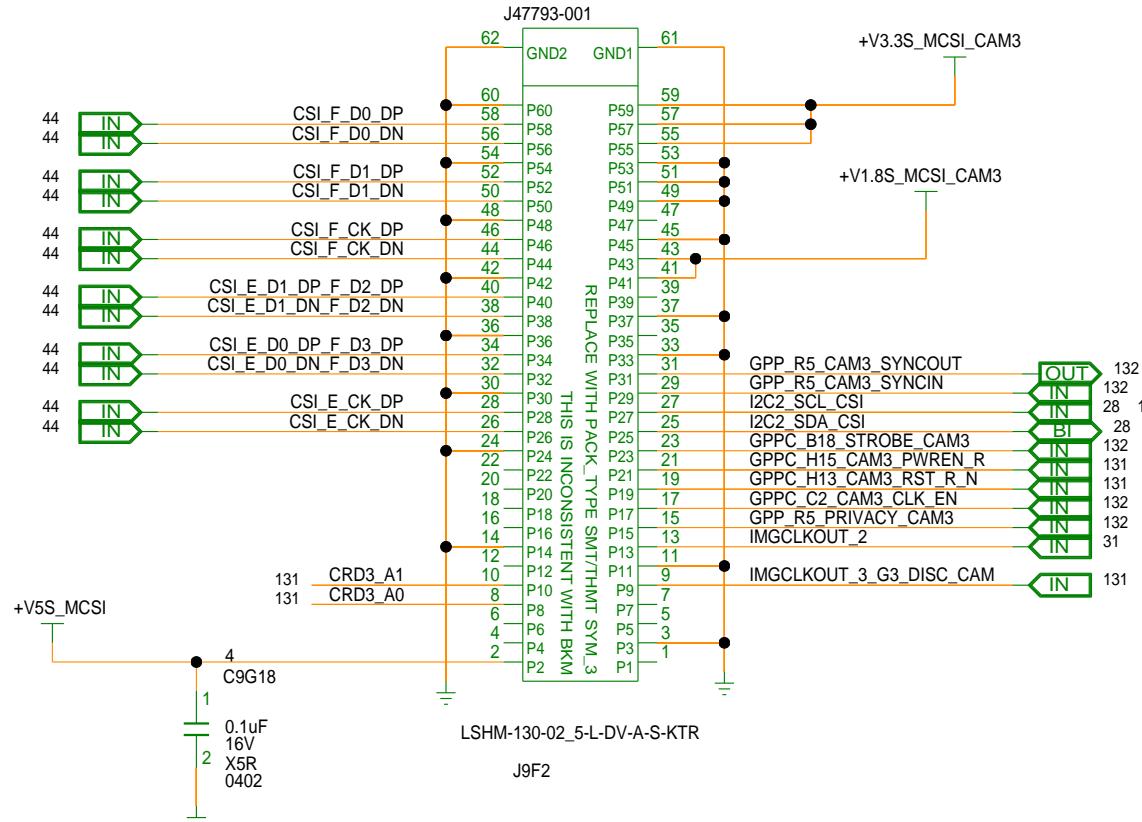




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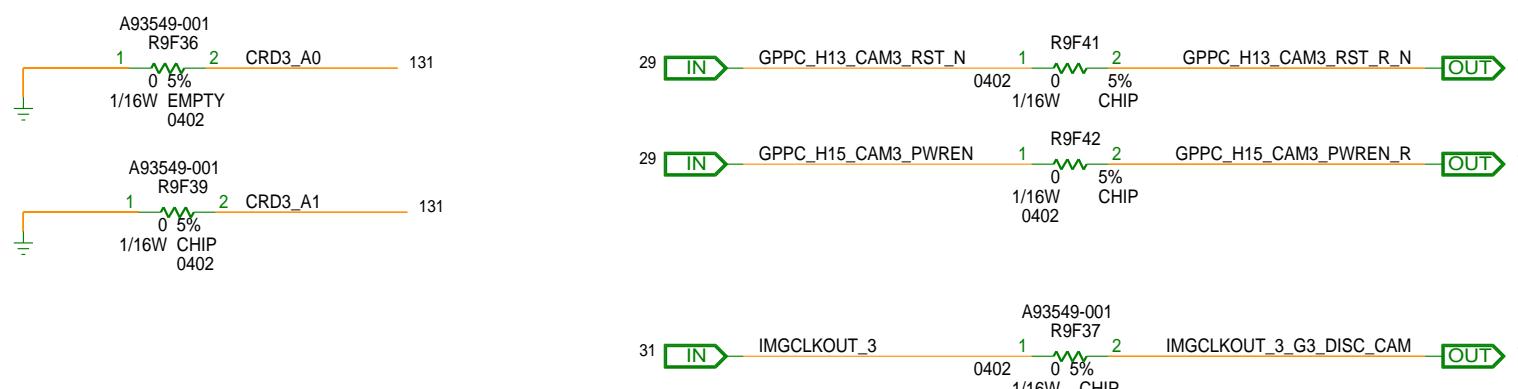
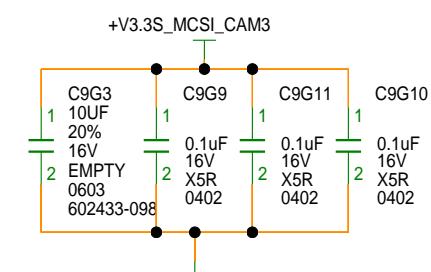
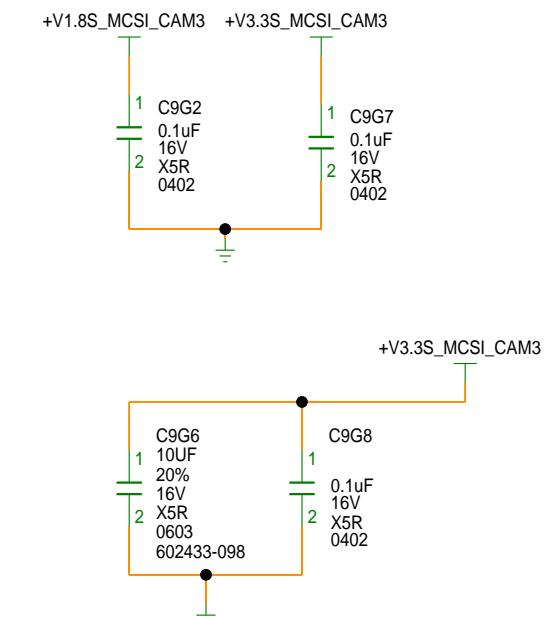
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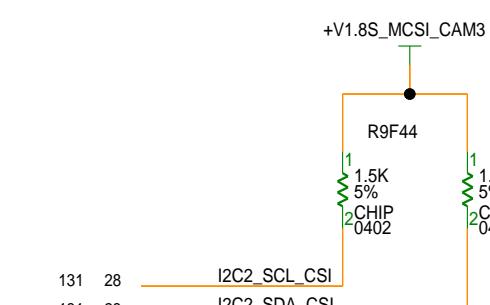


MODULE REV DETAILS

MODULE NAME	REV	DATE



I2C PU VALUE WILL BE OPTIMISED FOR 400KHZ BASED ON LAYOUT



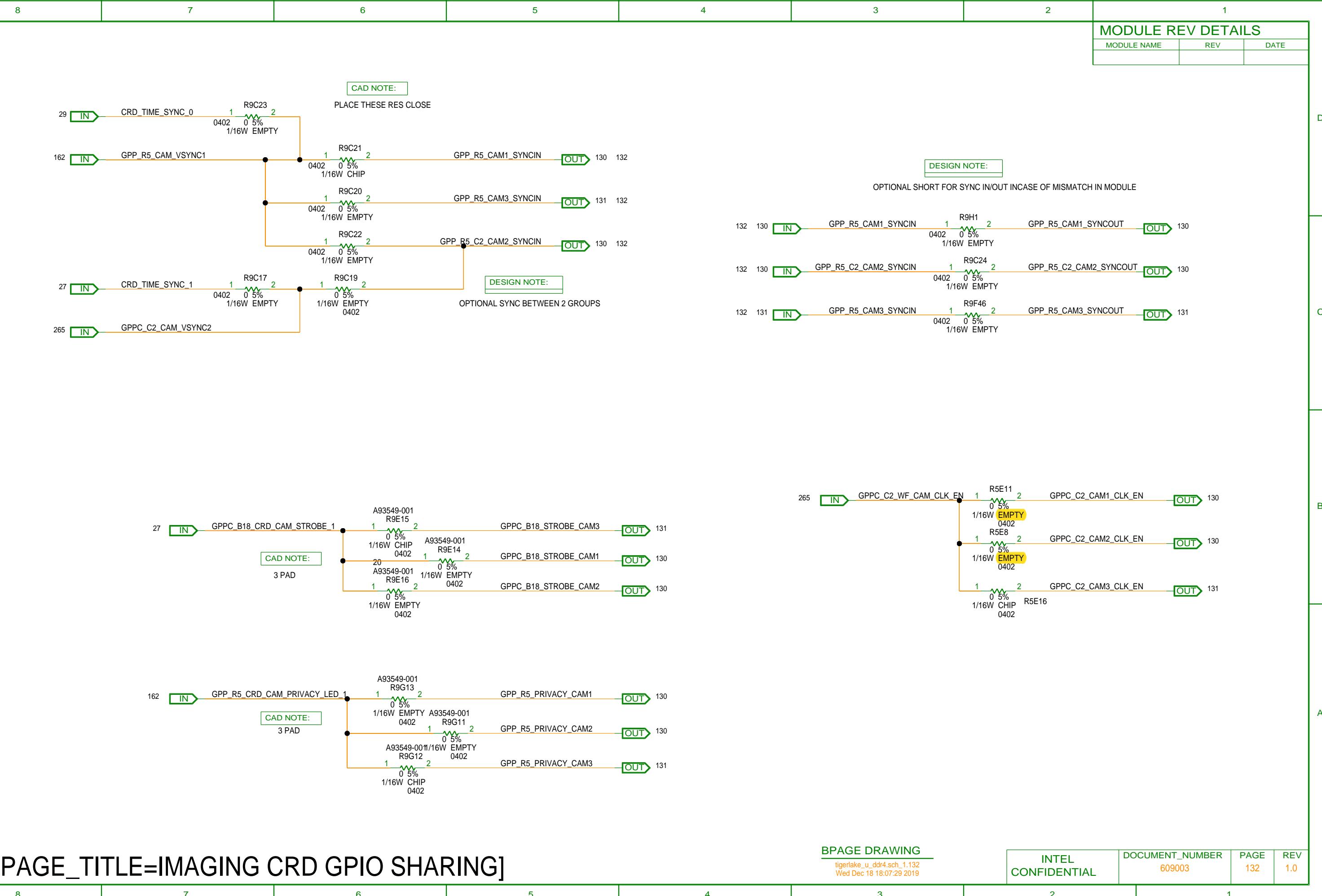
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Wed Dec 18 18:07:28 2019

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MODULE REV DETAILS

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MODULE NAME		REV	DATE				

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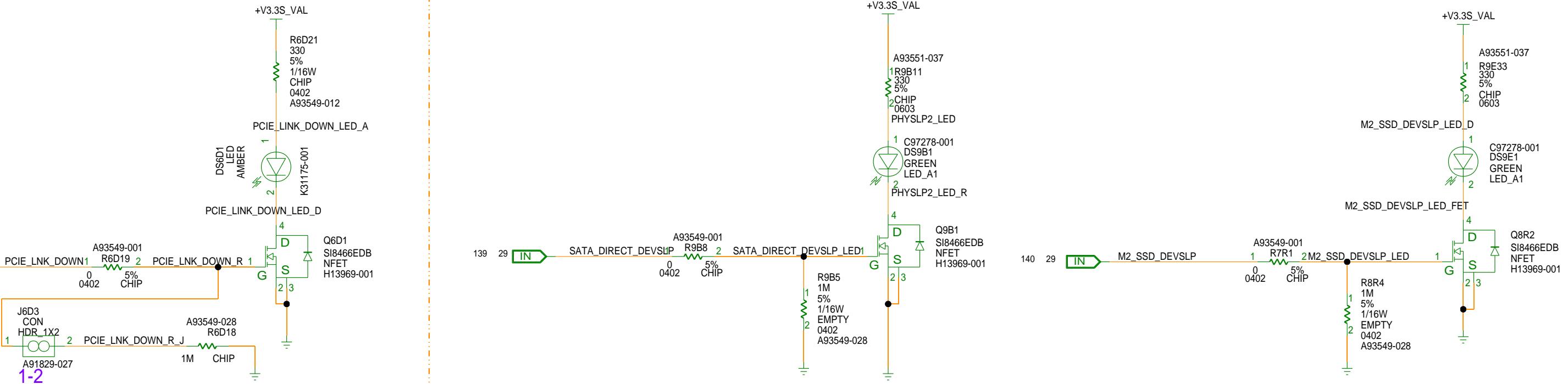
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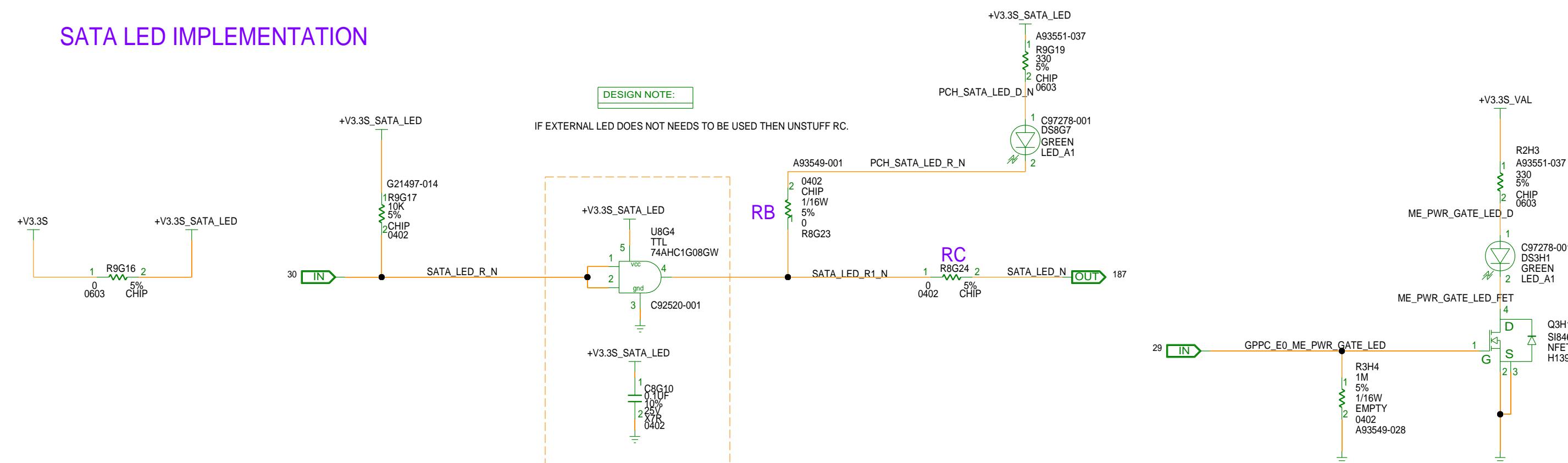
PCIE_LINK_DOWN_LED

SATA DEV SLEEP LED

MODULE REV DETAILS		
MODULE NAME	REV	DATE



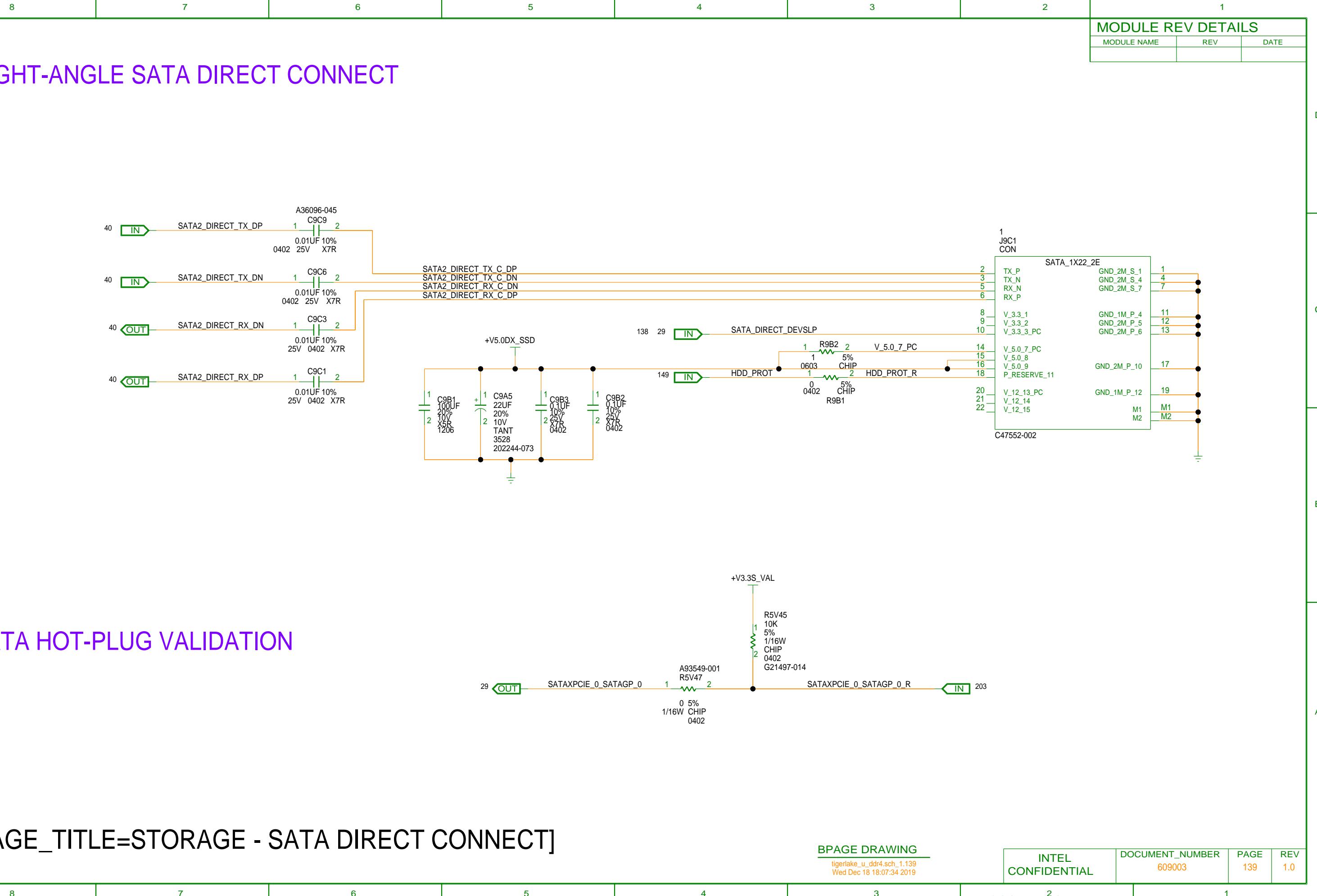
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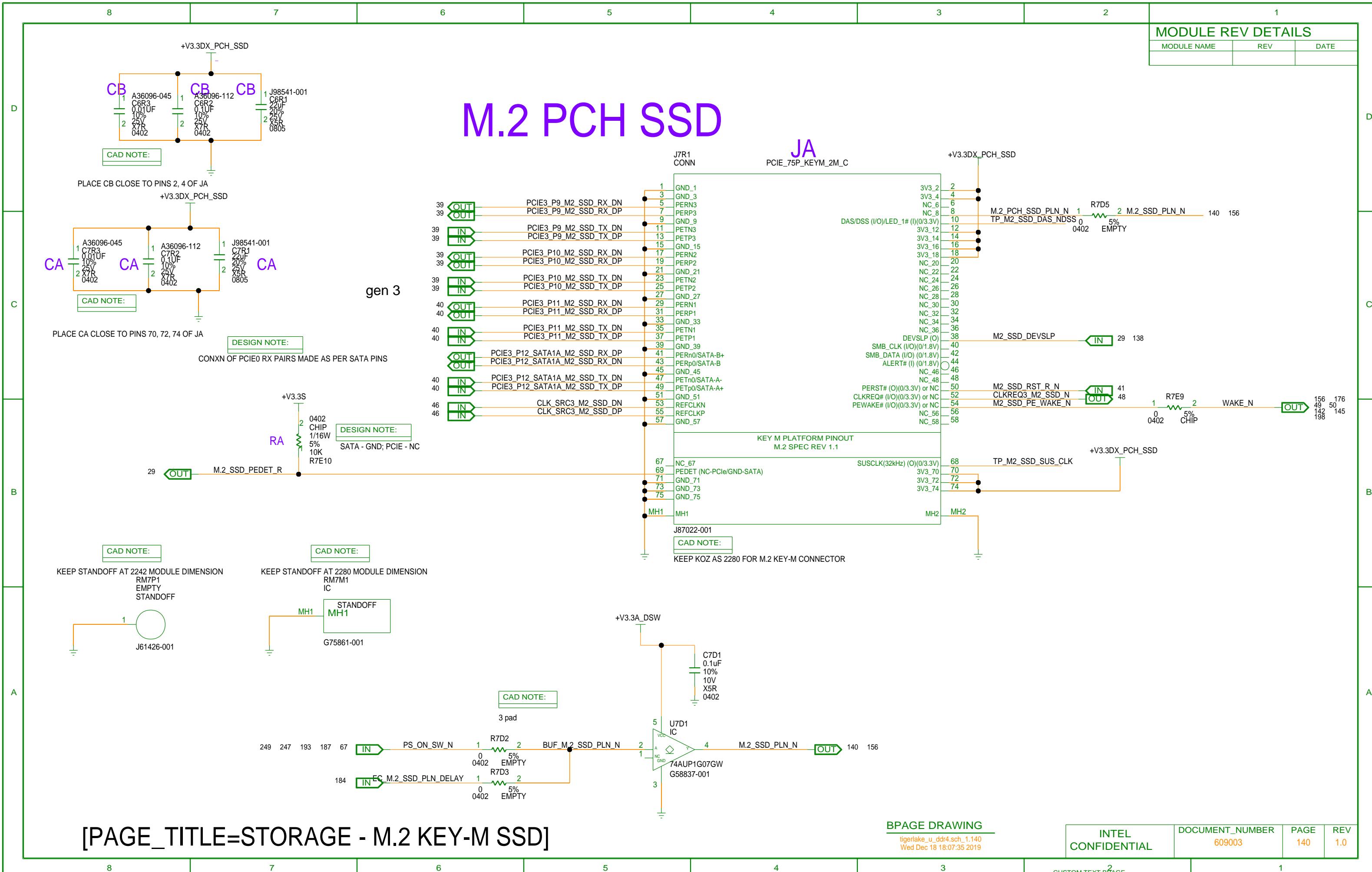


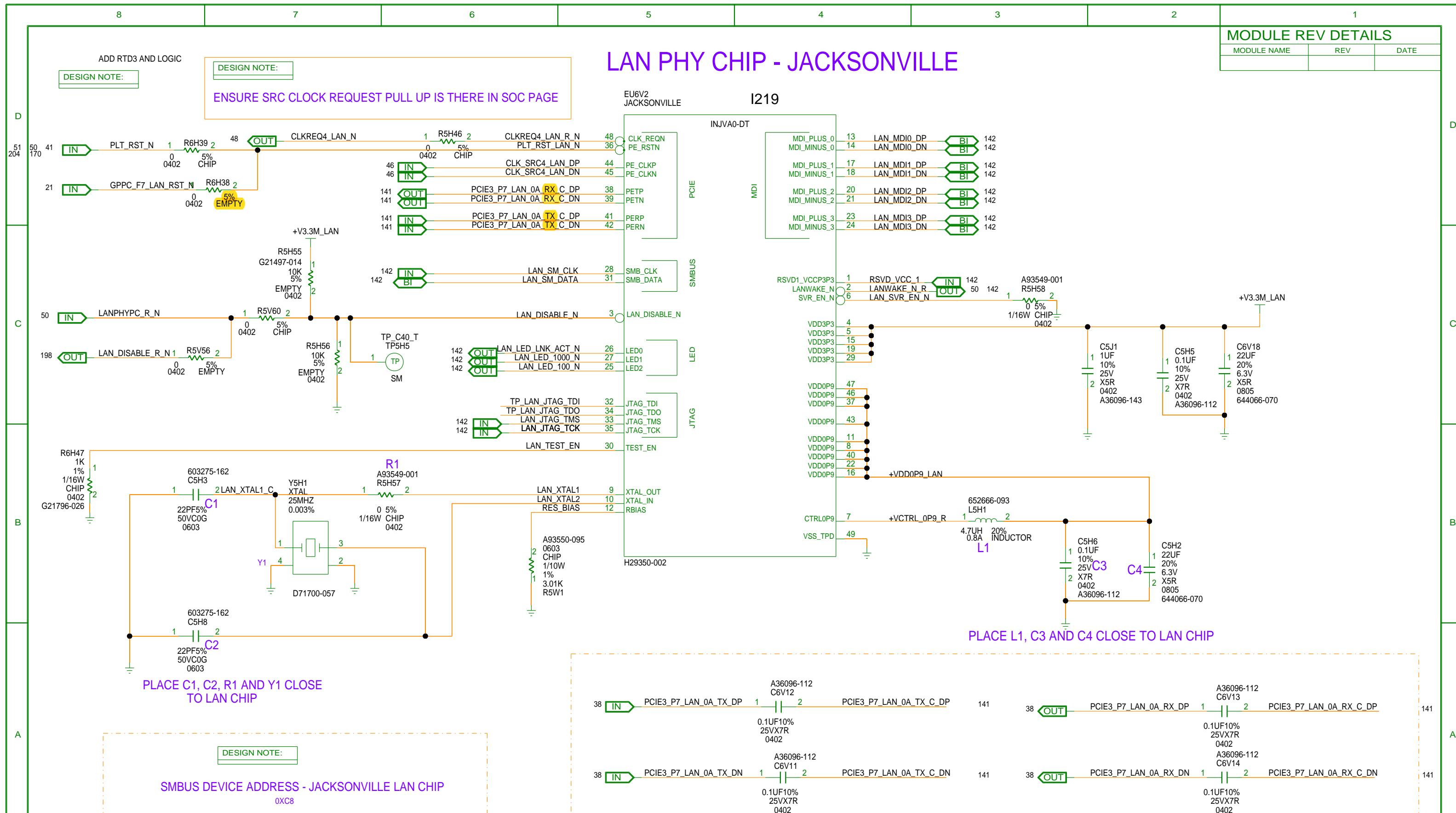
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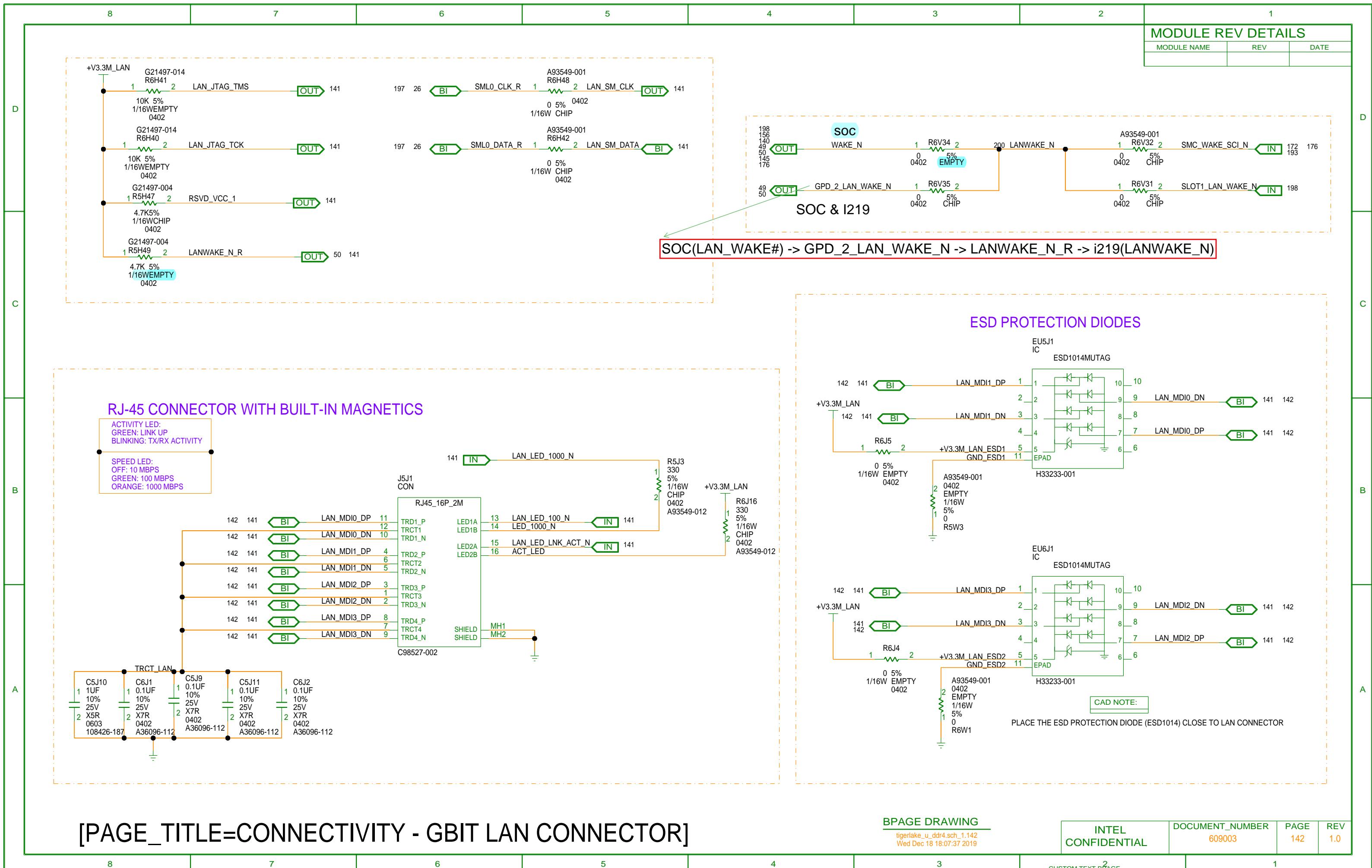
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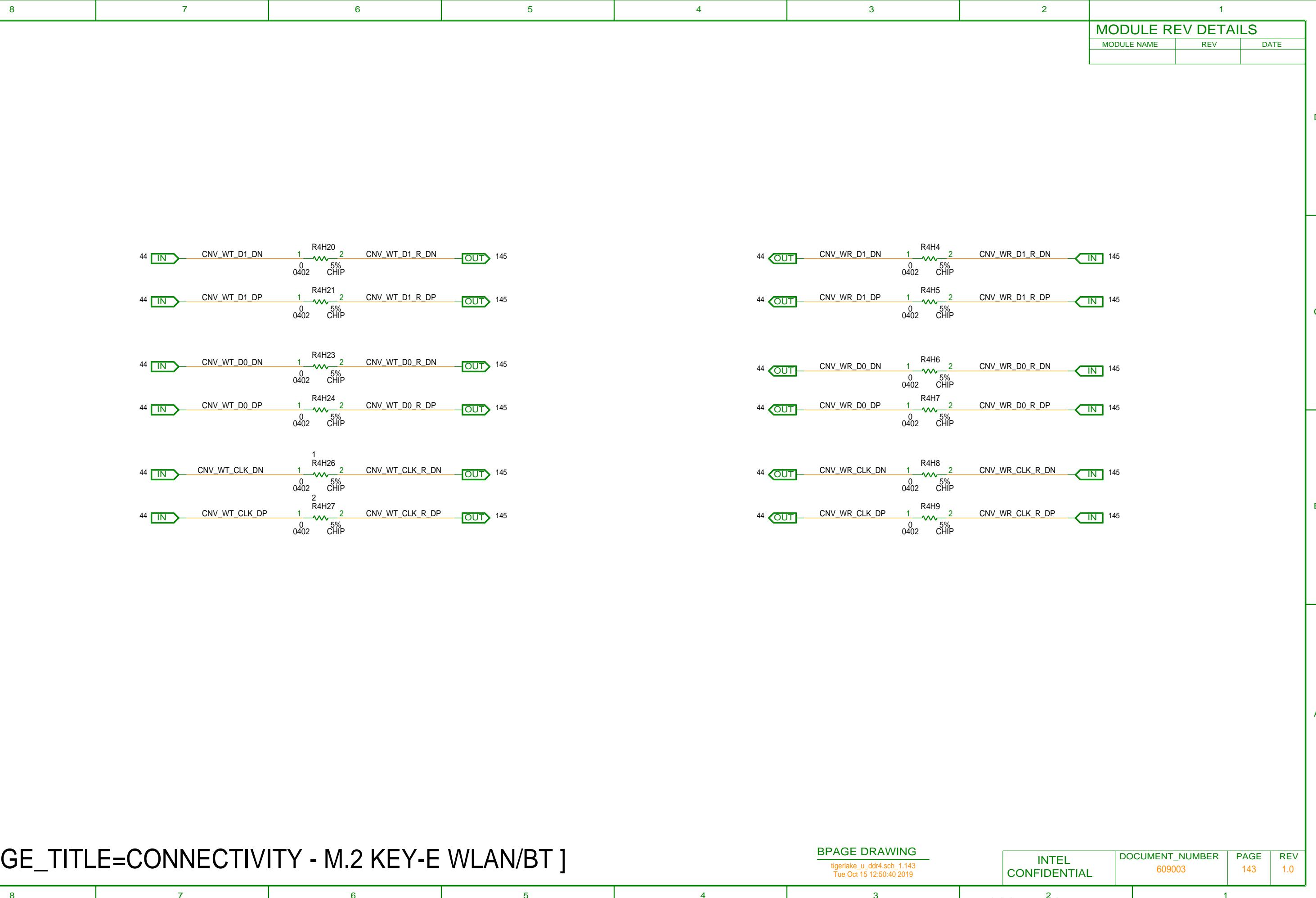
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	609003	138	1.0

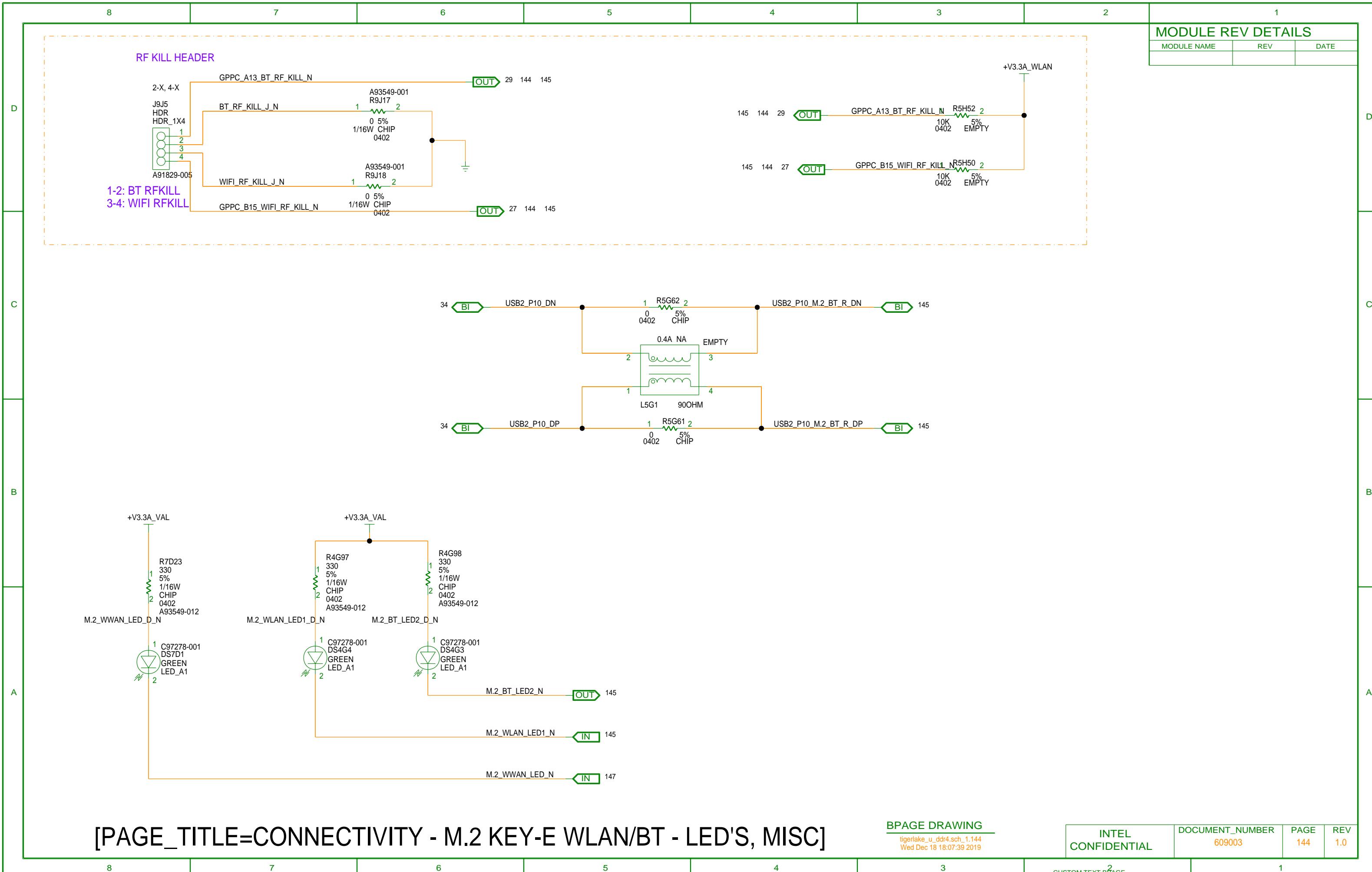


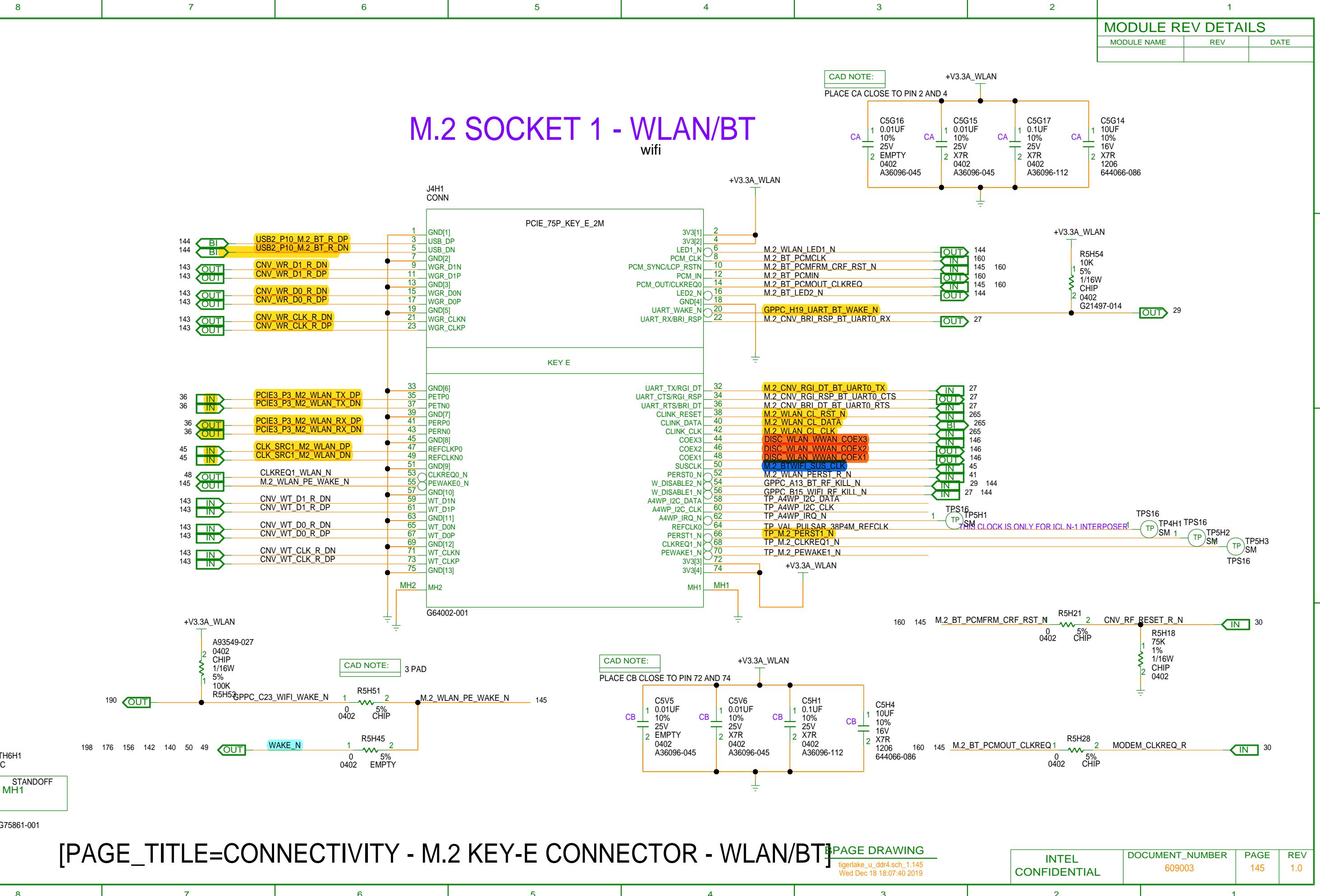


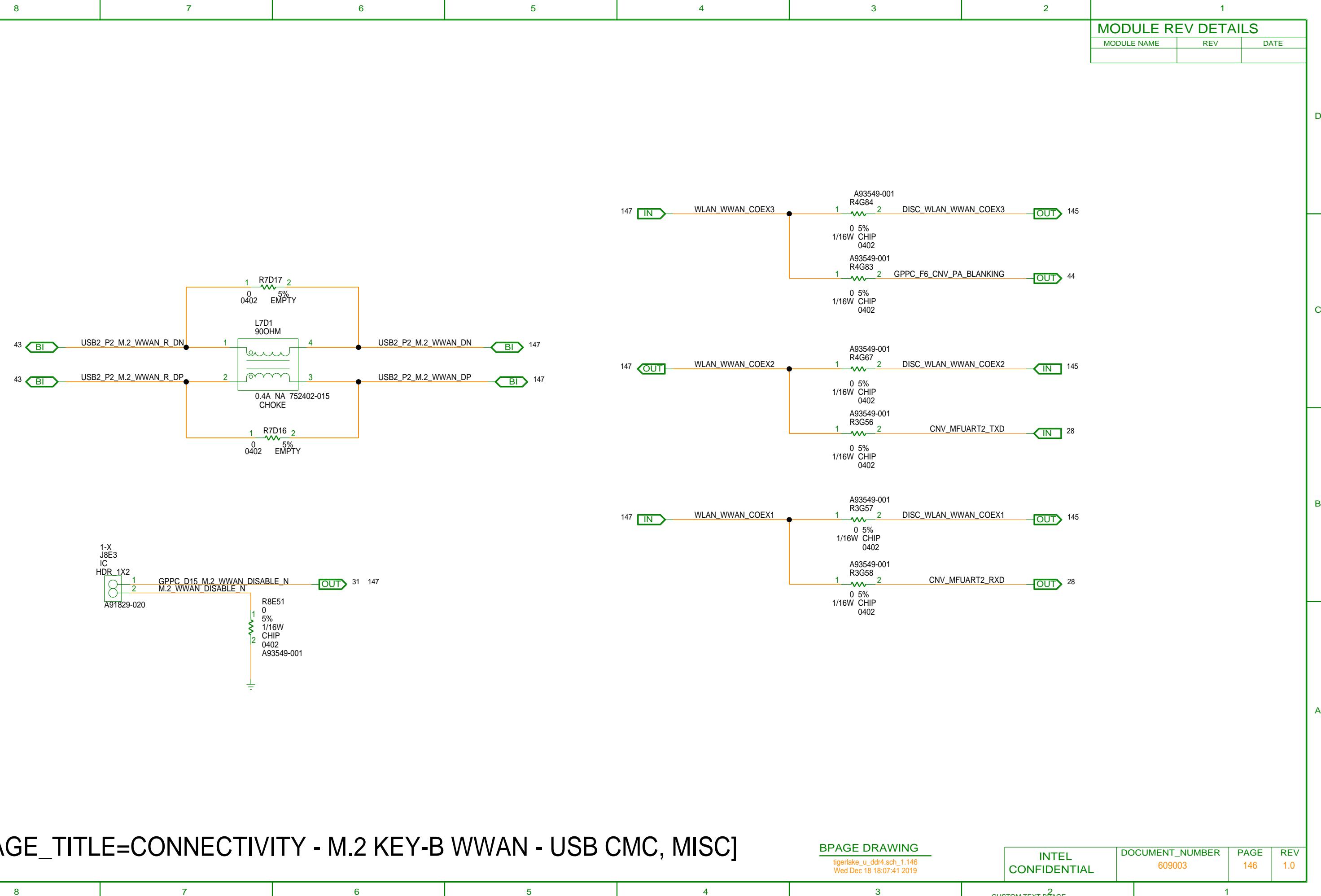


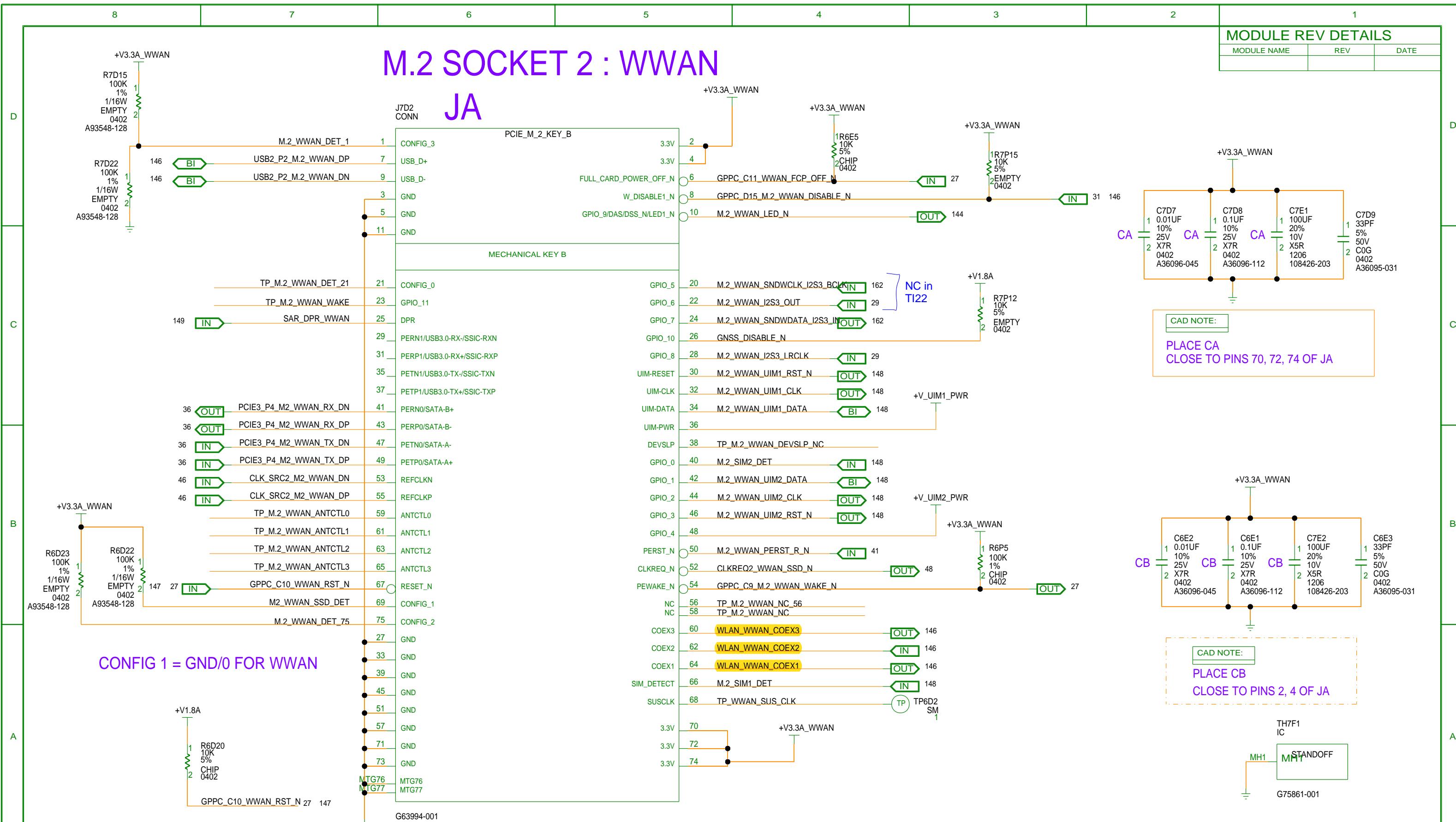








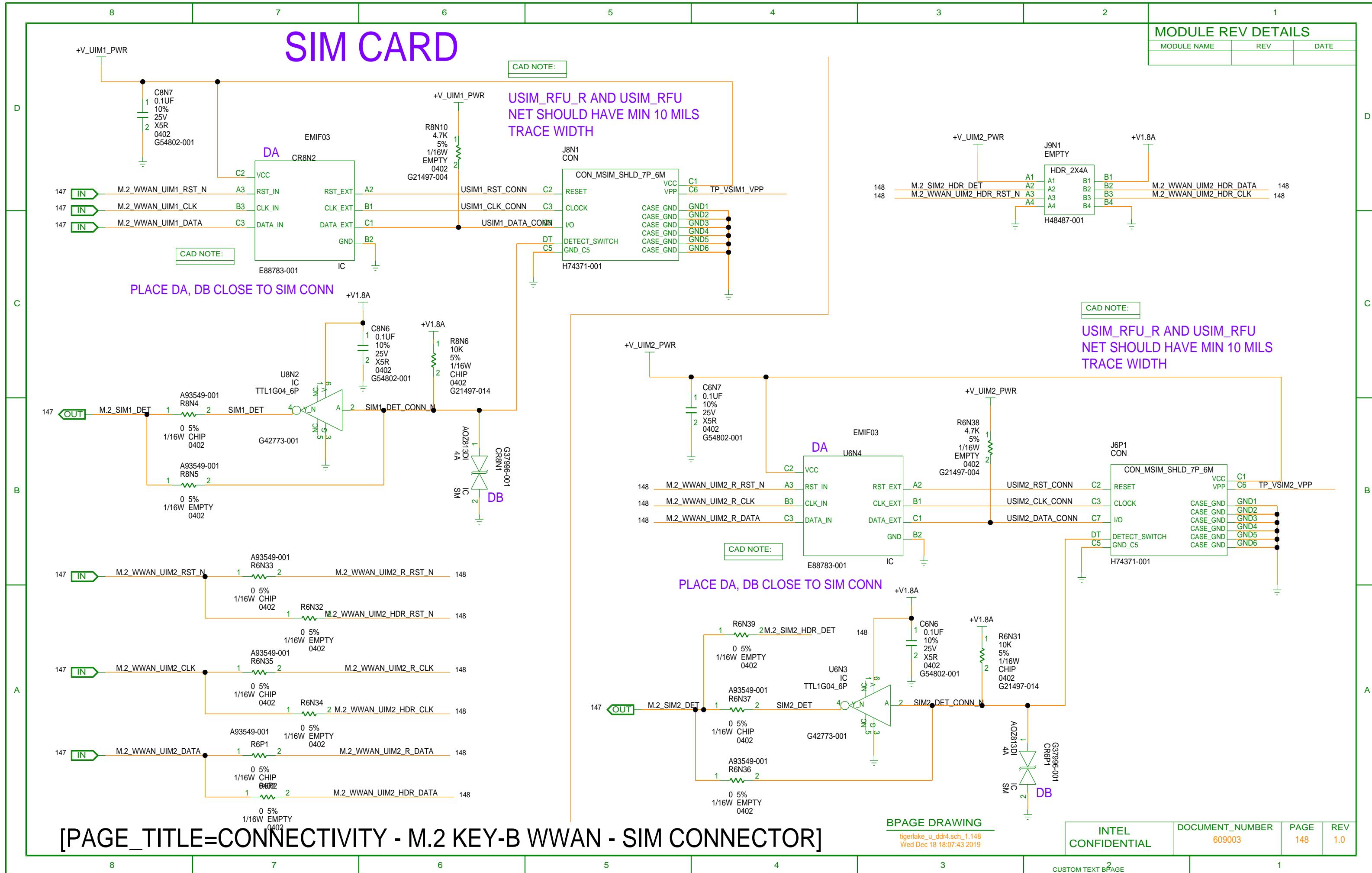


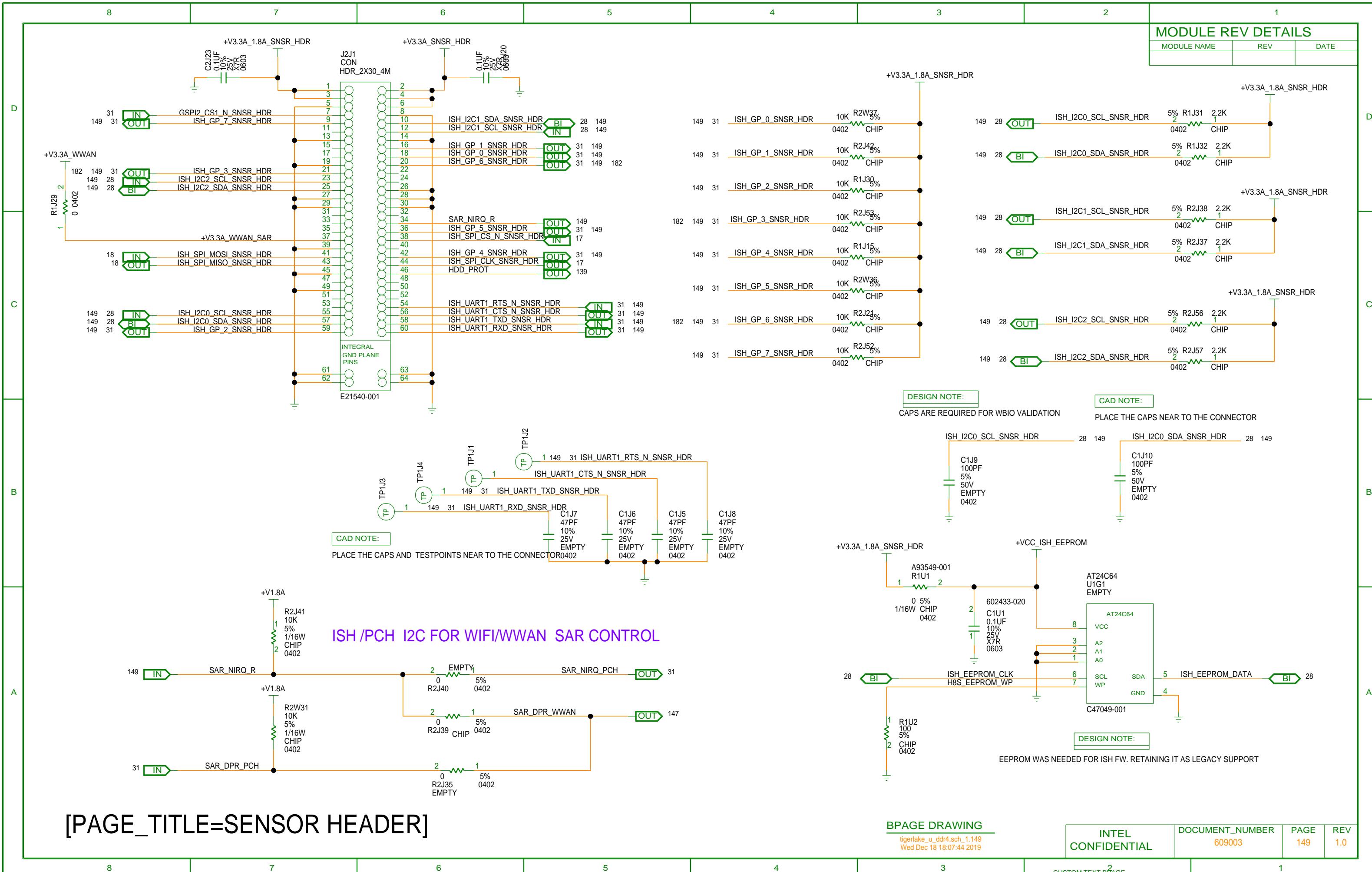


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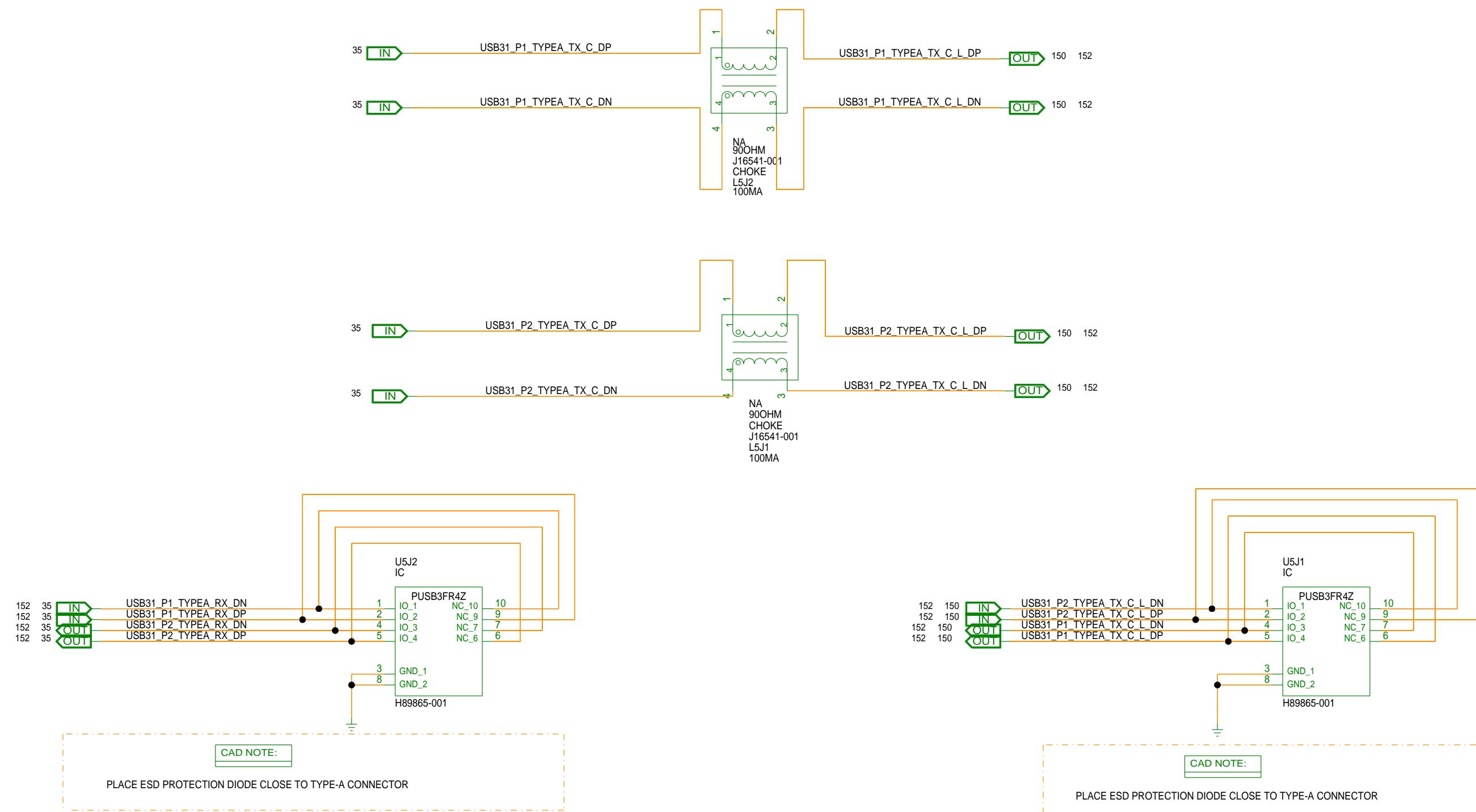




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MODULE REV DETAILS		
MODULE NAME	REV	DATE

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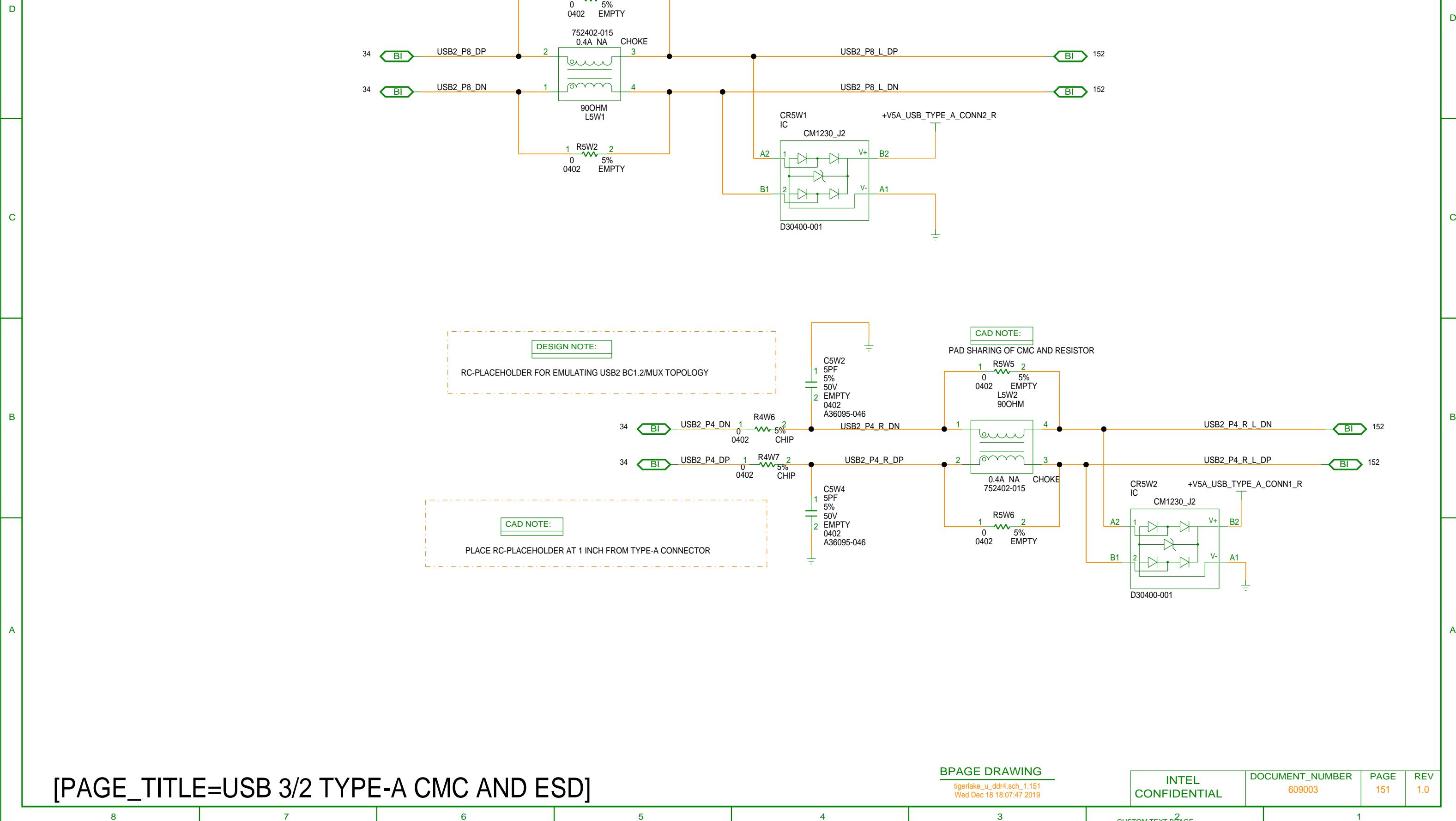
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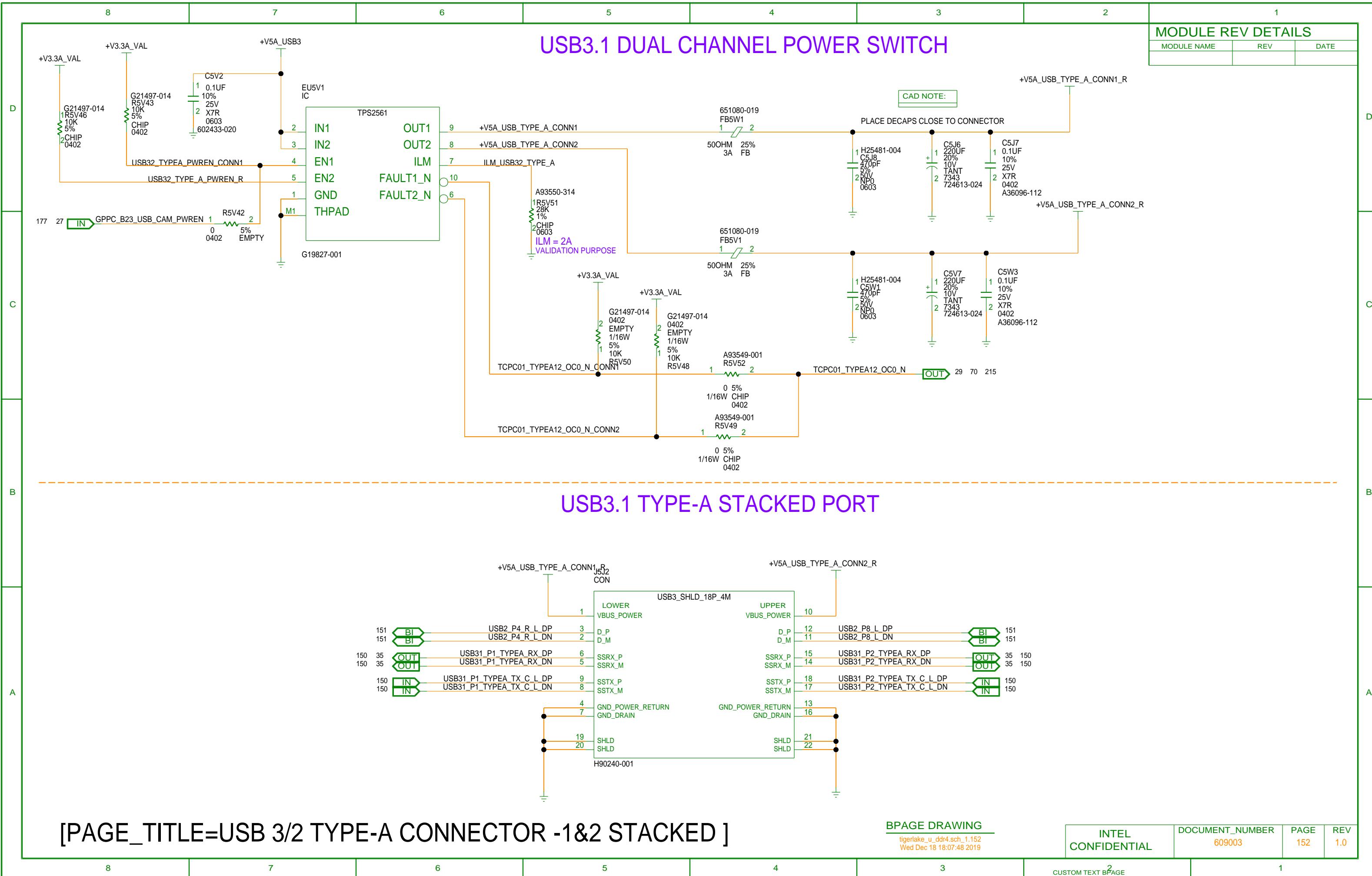
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USB 4 & 8 CMC/ESD

MODULE REV DETAILS

MODULE NAME	REV	DATE





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MODULE REV DETAILS

MODULE NAME	REV	DATE

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tigerlake_u_ddr4.sch_1.153
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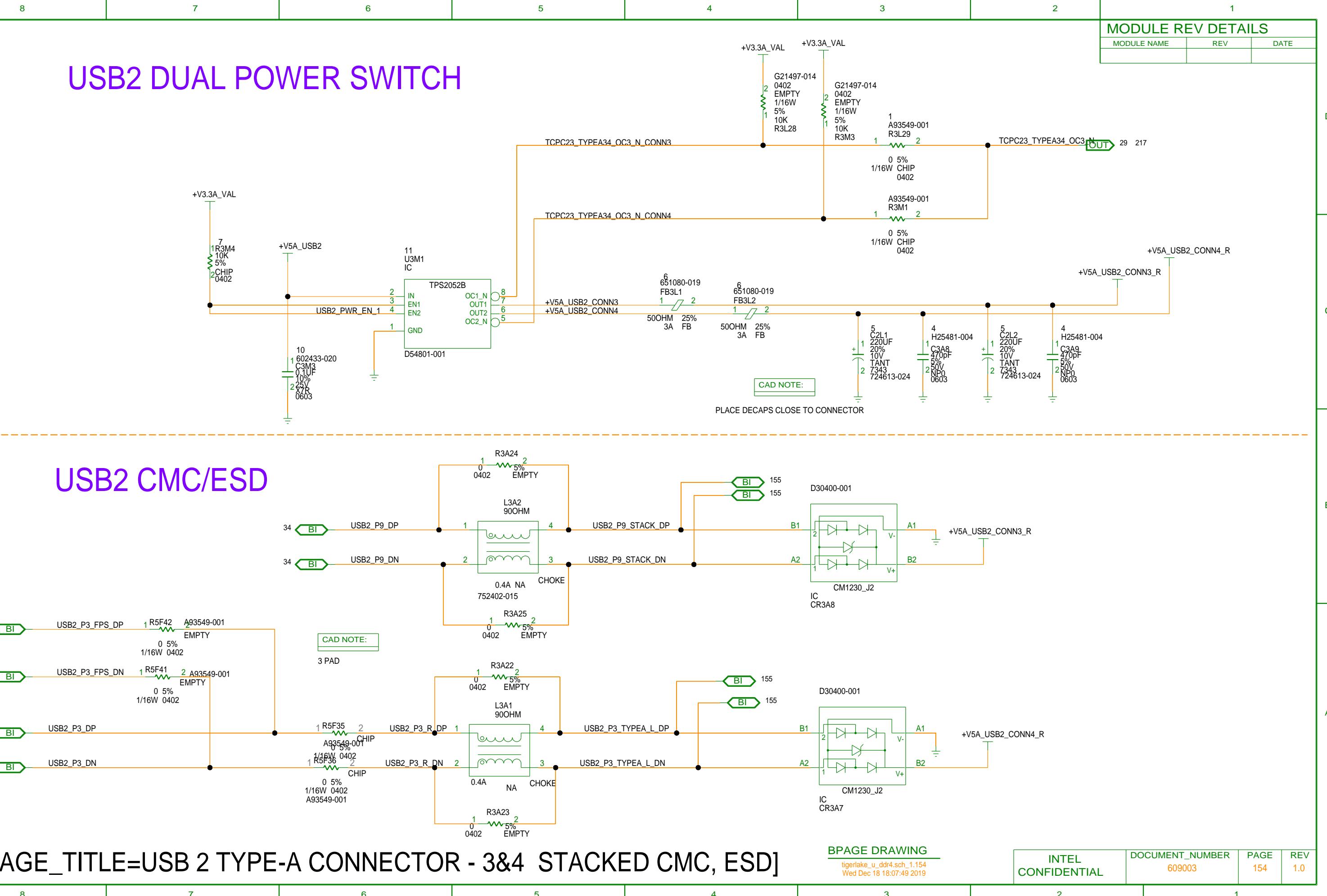
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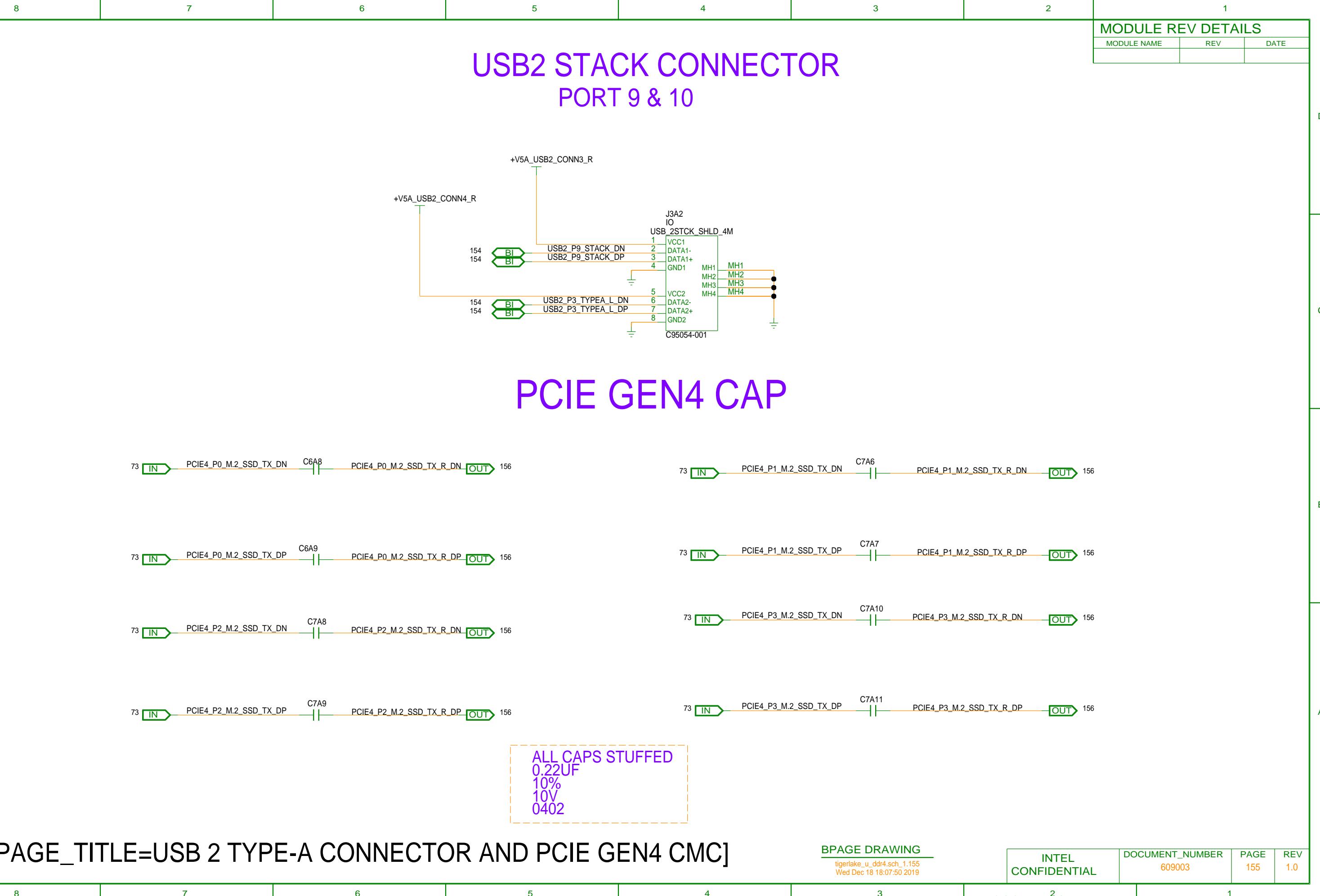
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BPAGE

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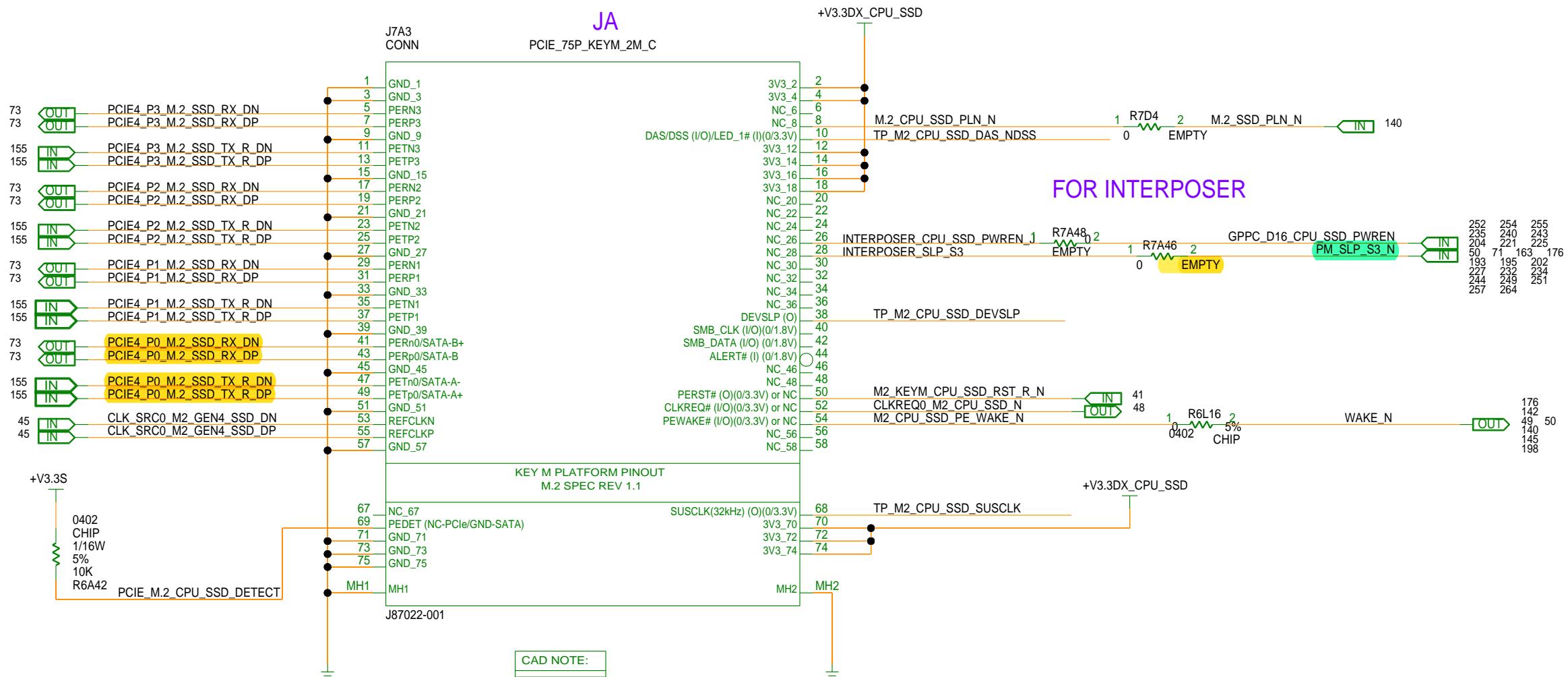


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PCIE GEN4 SSD

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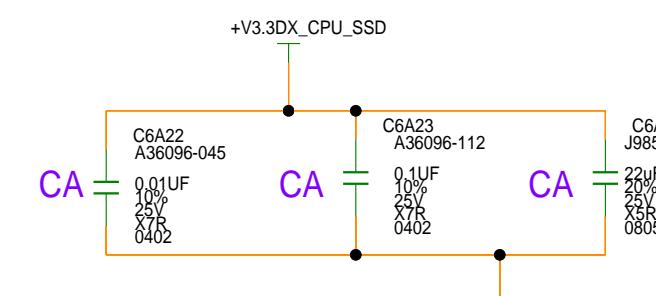
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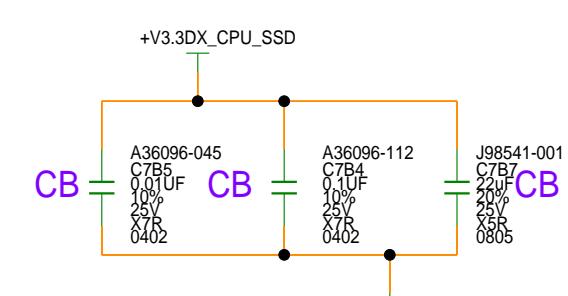
CAD NOTE: KEEP STANOFF AT 2242 MODULE DIMENSION

RM6N1
EMPTY

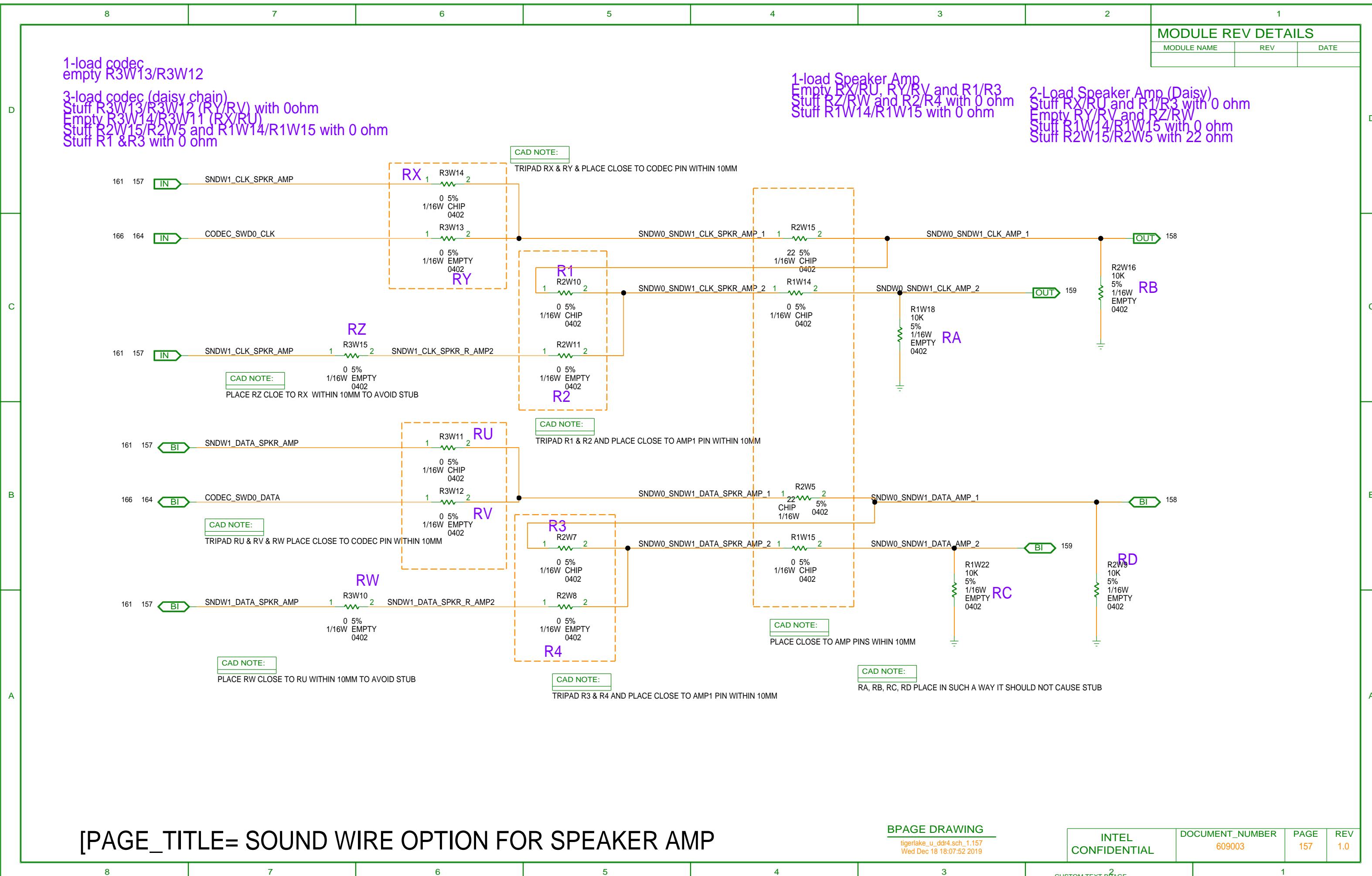
KEEP K0Z AS 2280 FOR M.2 KEY-M CONNECTOR

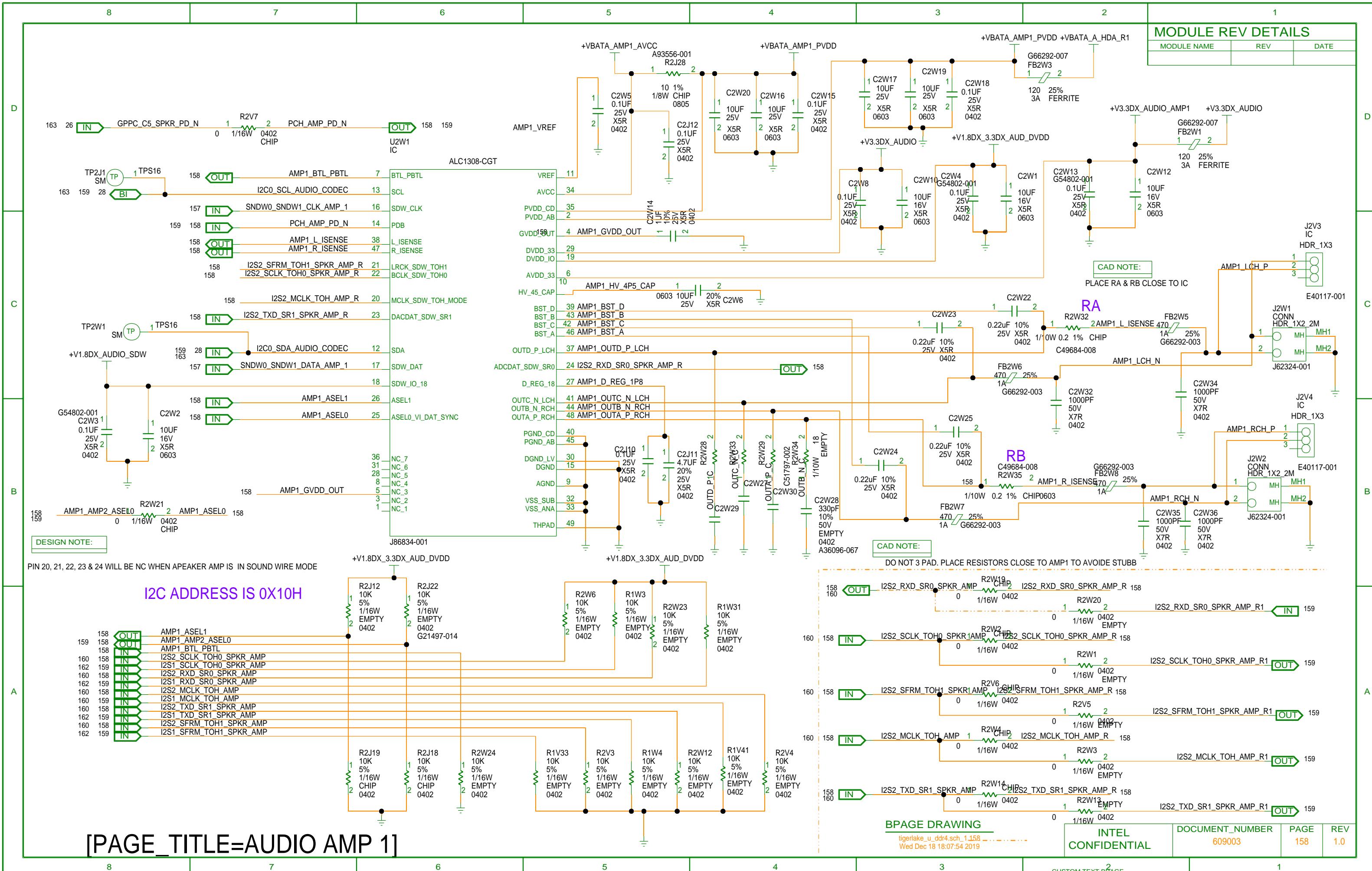


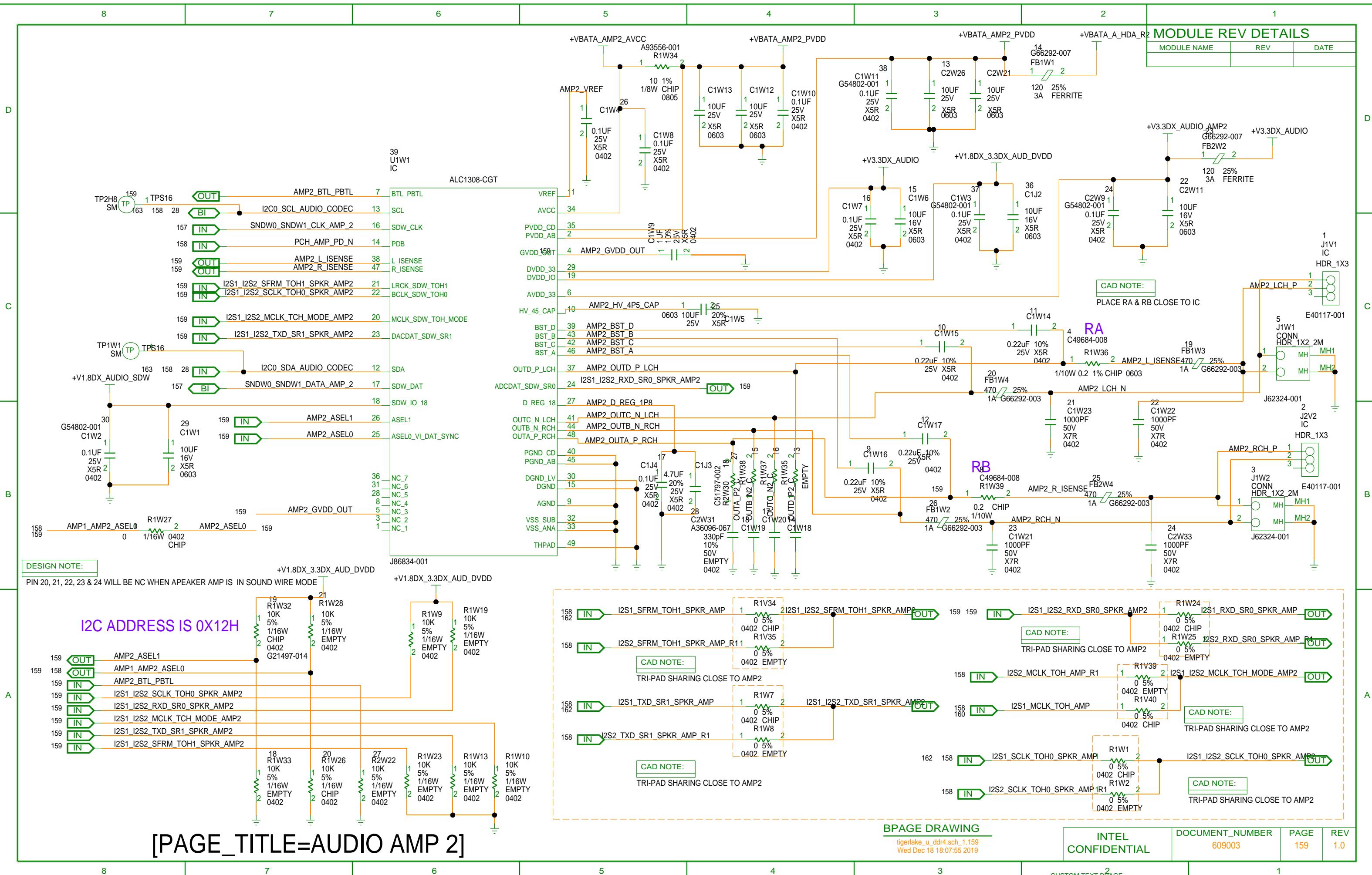
PLACE CA CLOSE TO PINS 70, 72, 74 OF JA

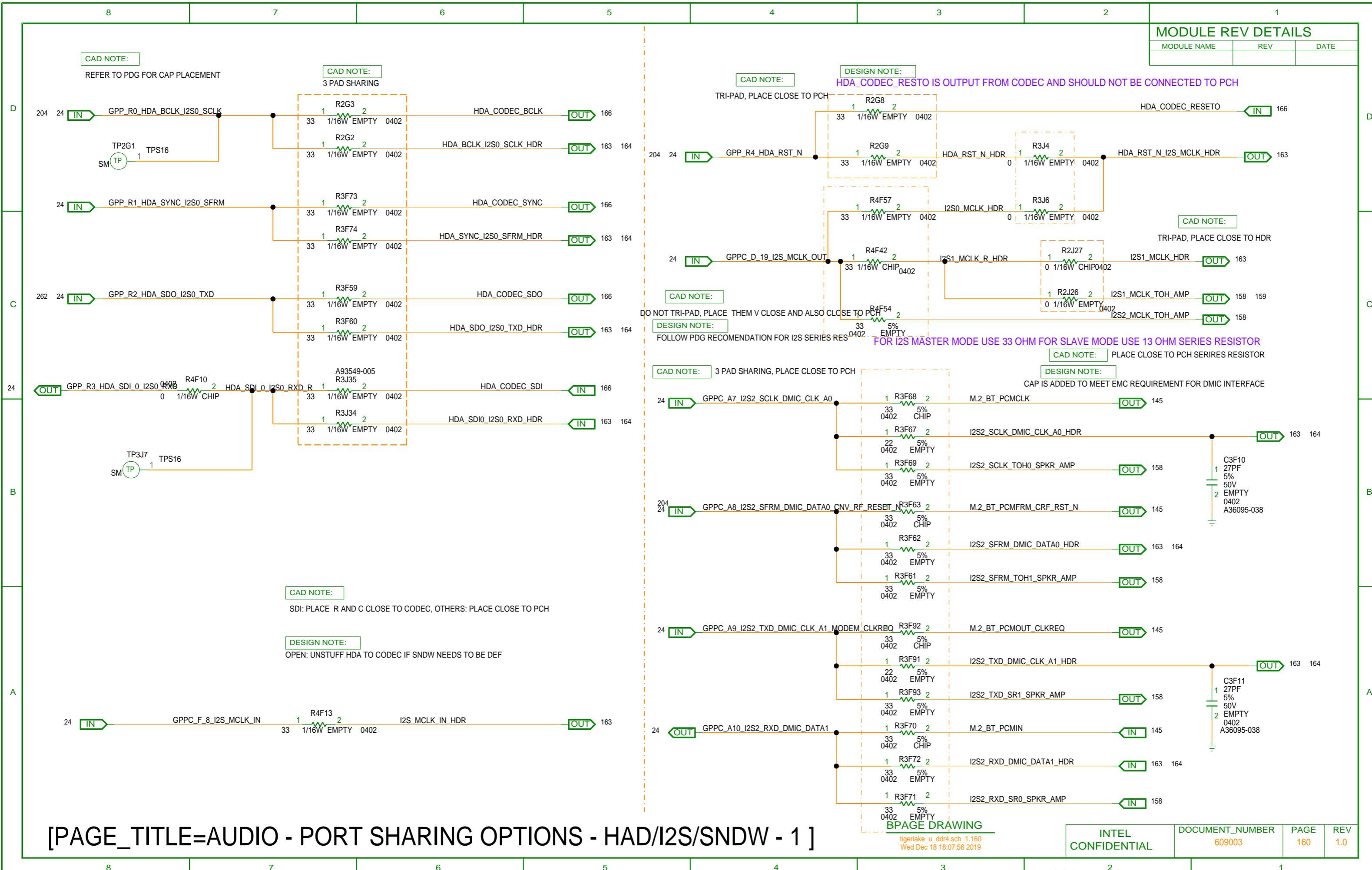


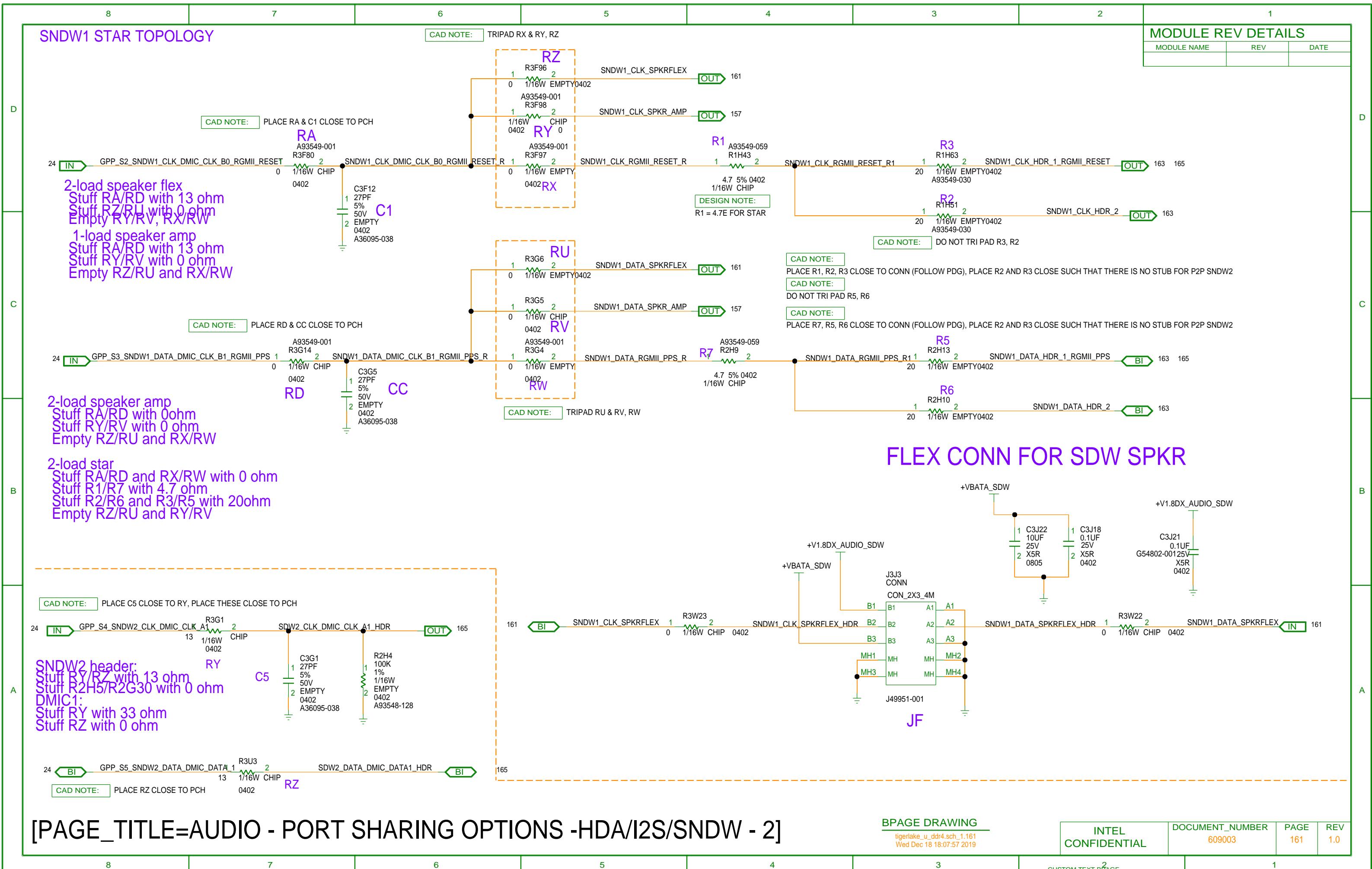
PLACE CB CLOSE TO PINS 2, 4 OF JA

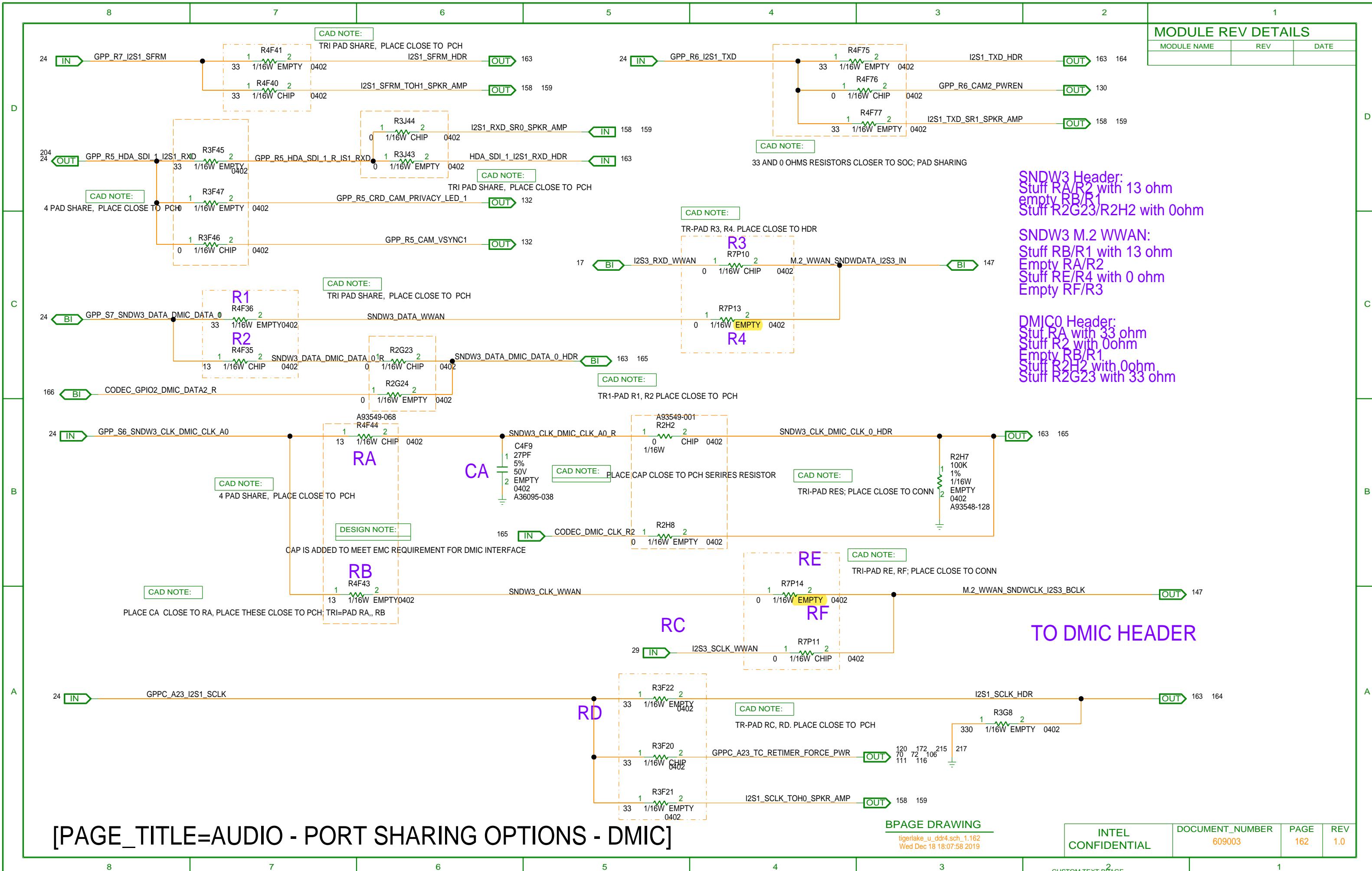


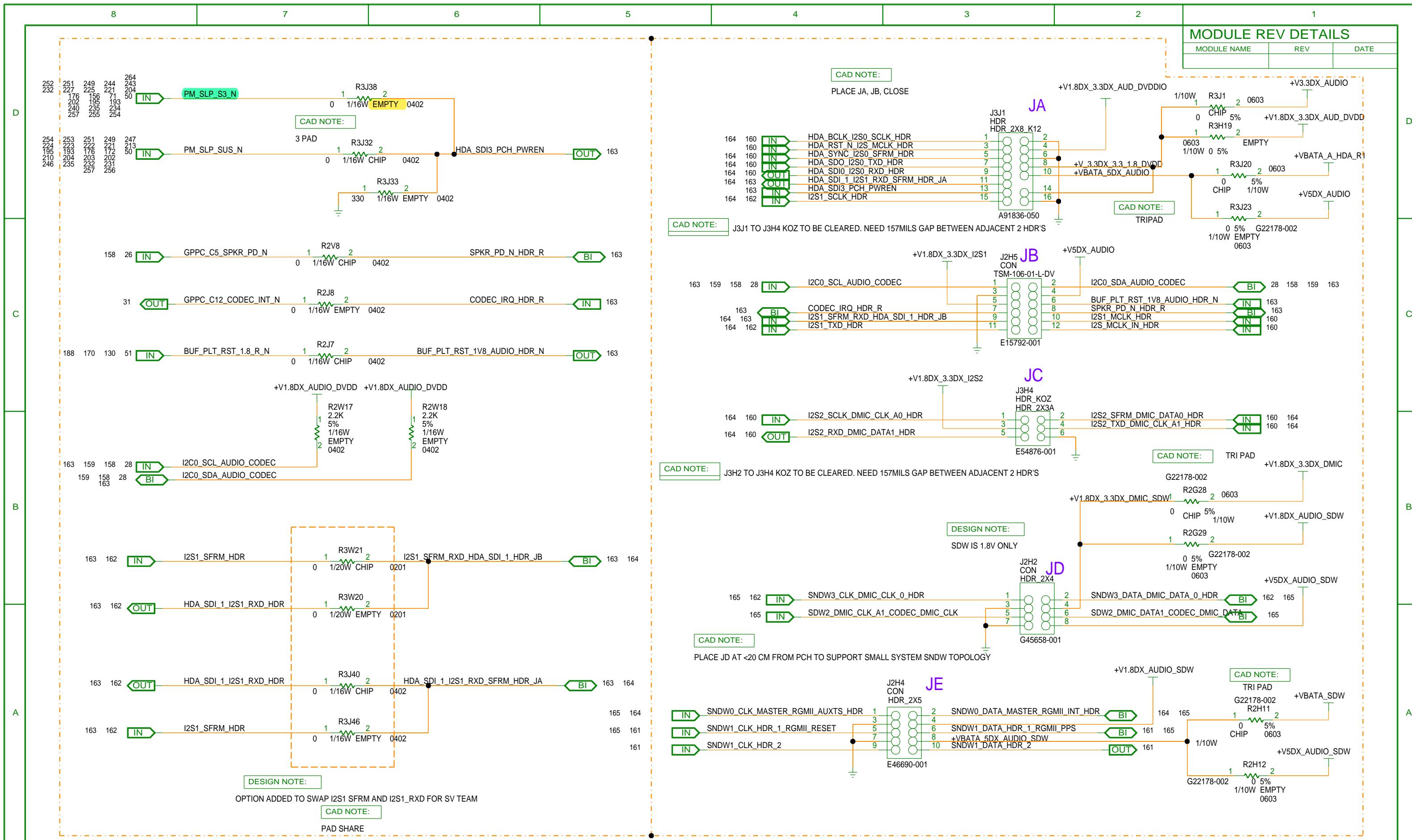








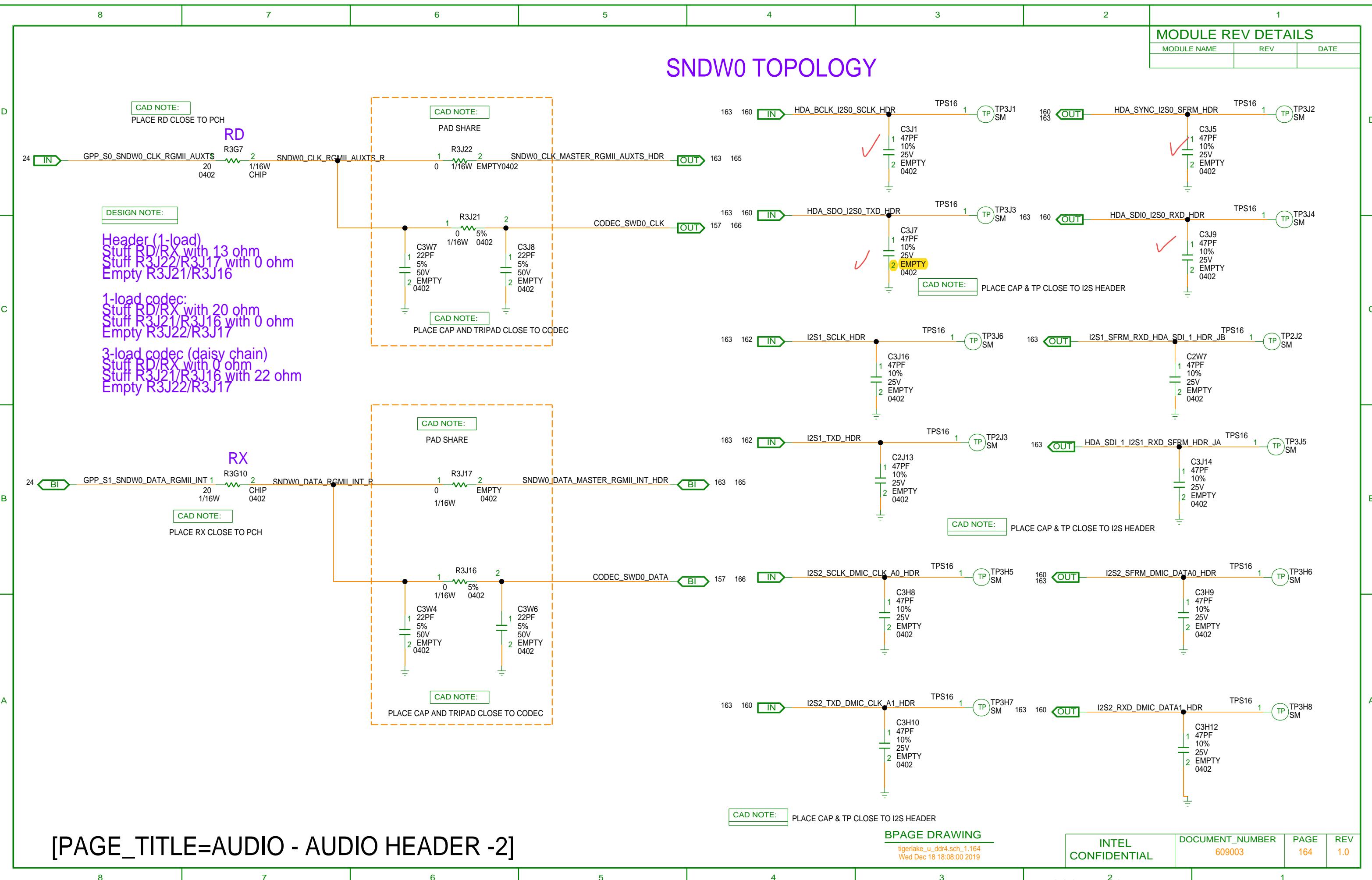


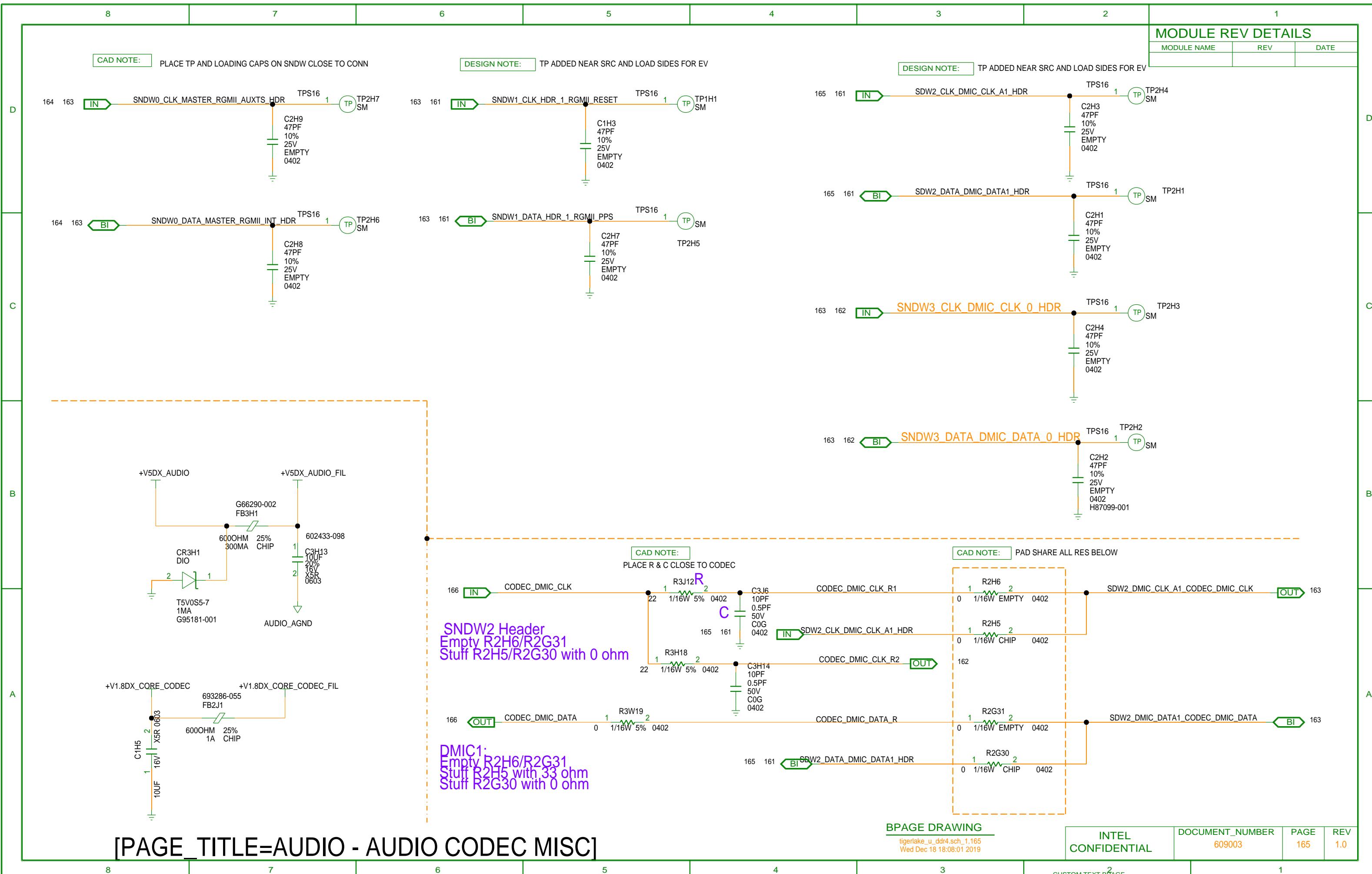


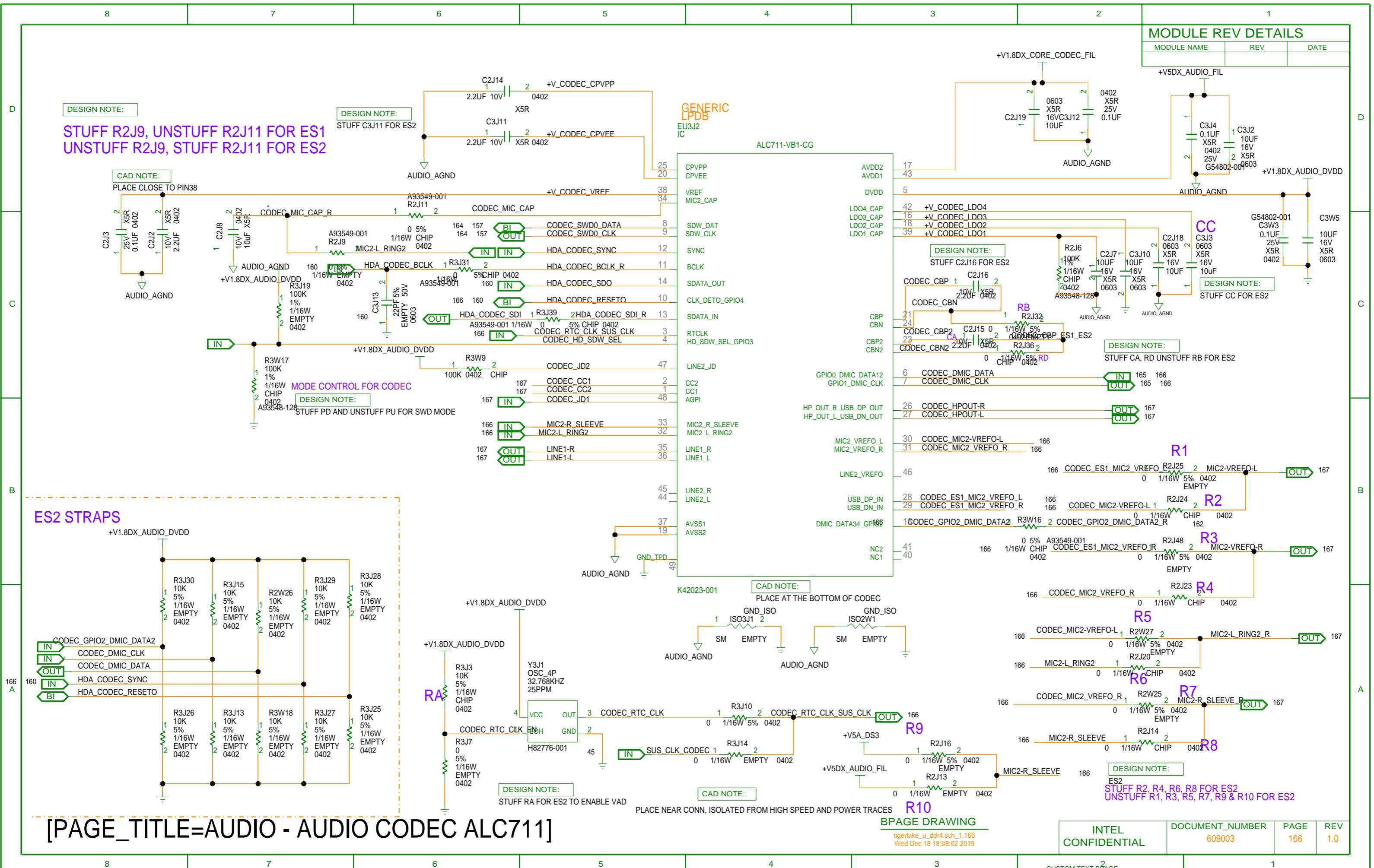
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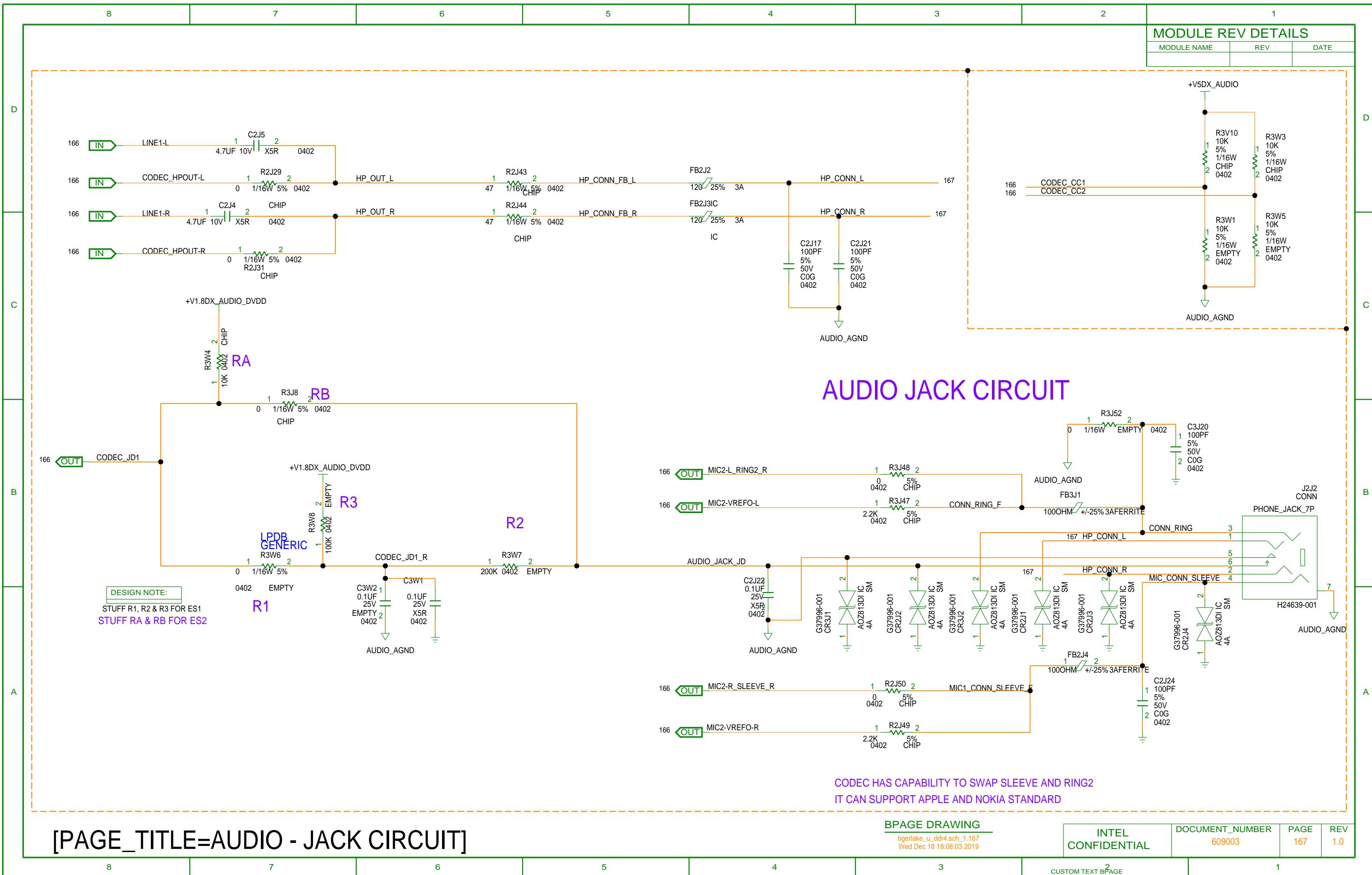
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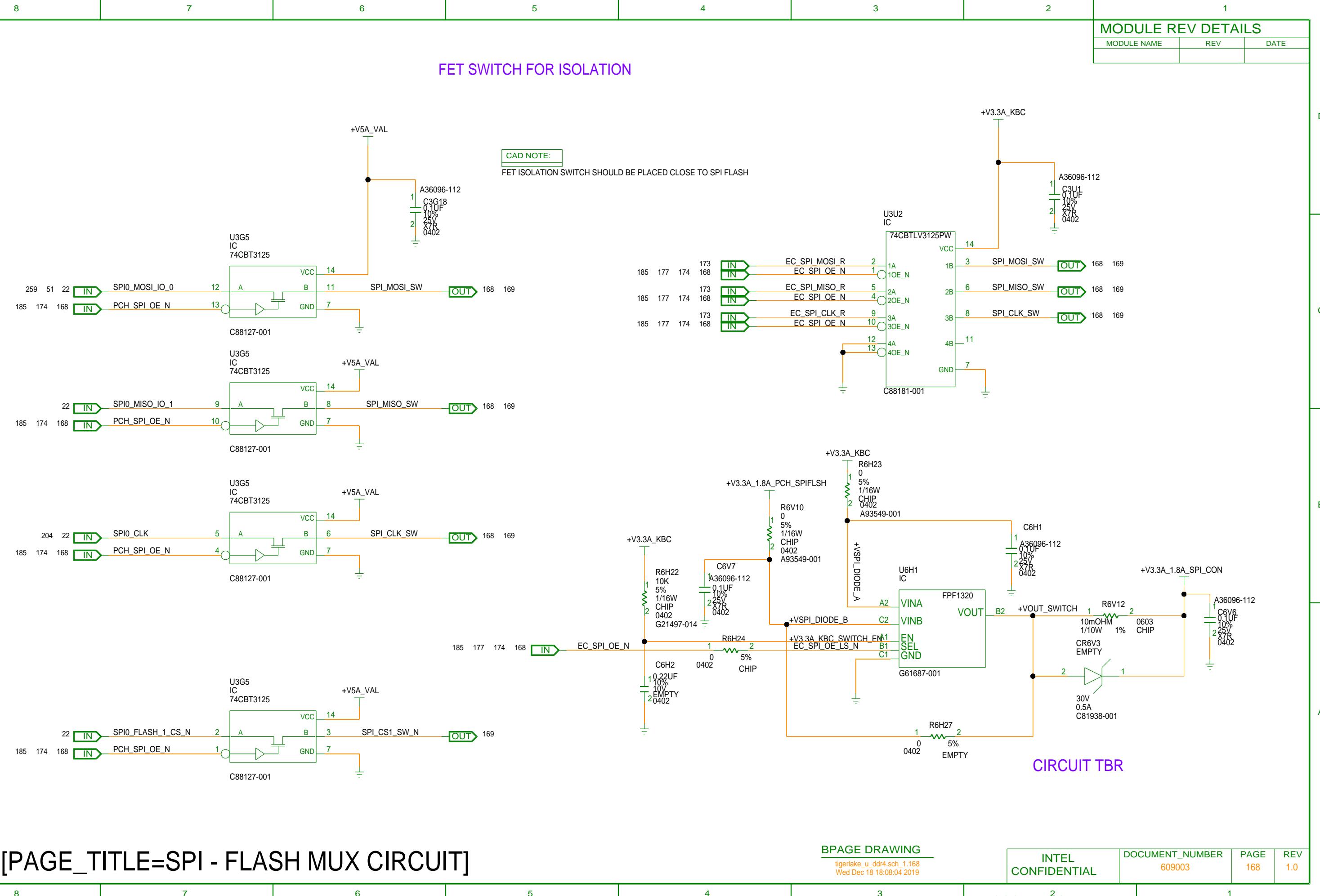
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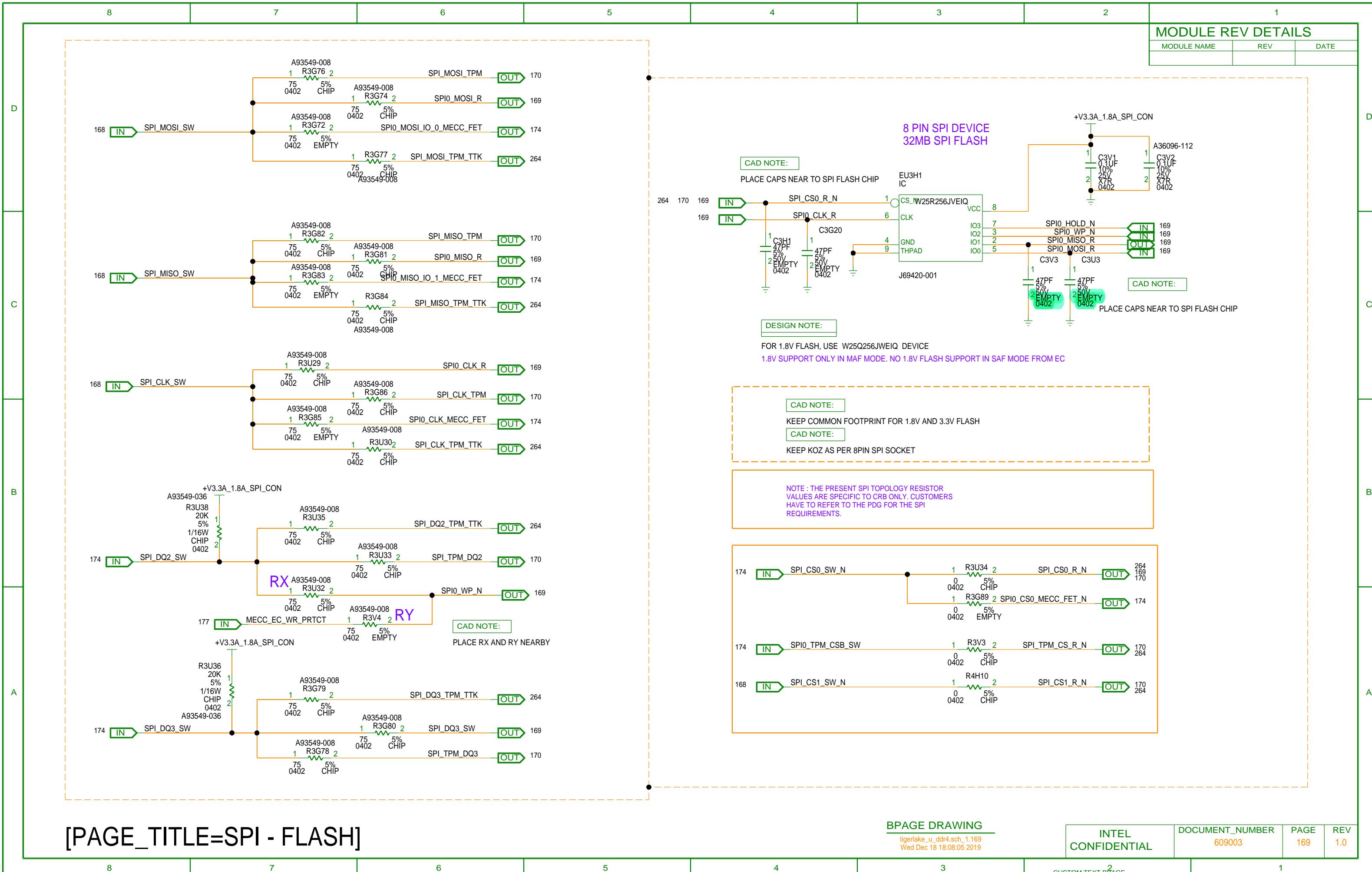












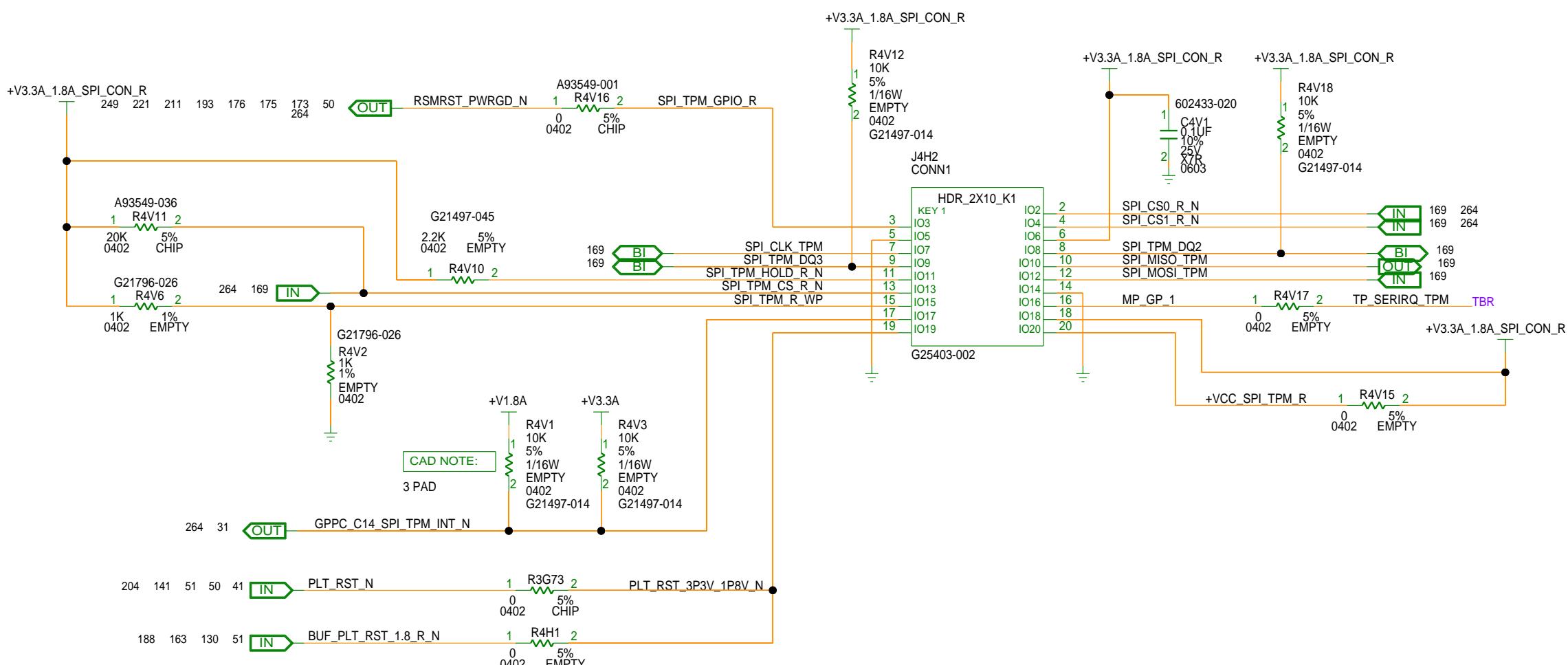
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

SF600 BASED SPI BASED TPM HEADER

CAD NOTE:

SPI0_FLASH_1_CS_N SIGNAL TO BE ROUTED 1.5 INCH MORE LENGTH THAN OTHER SPI0 SIGNALS

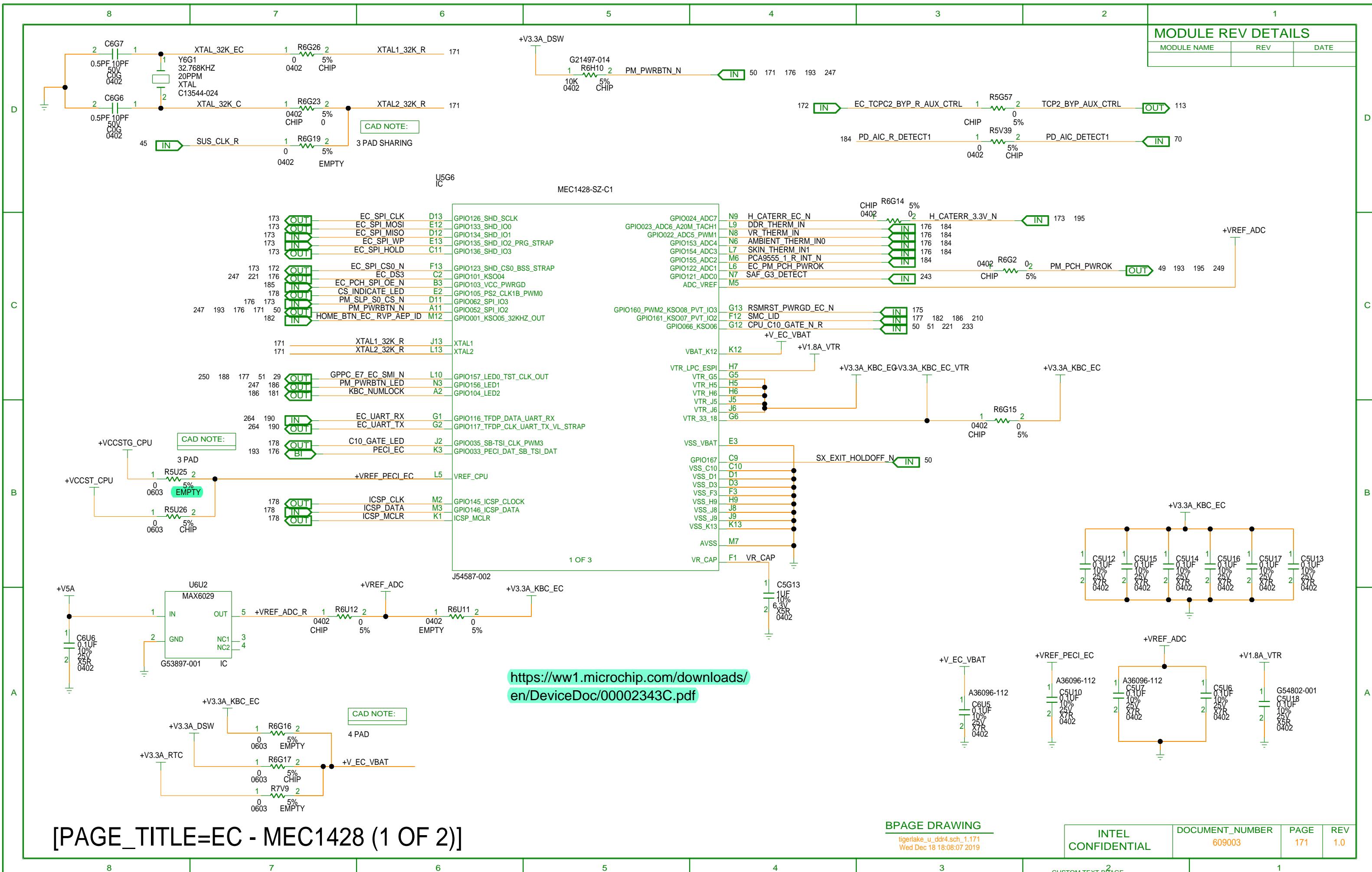


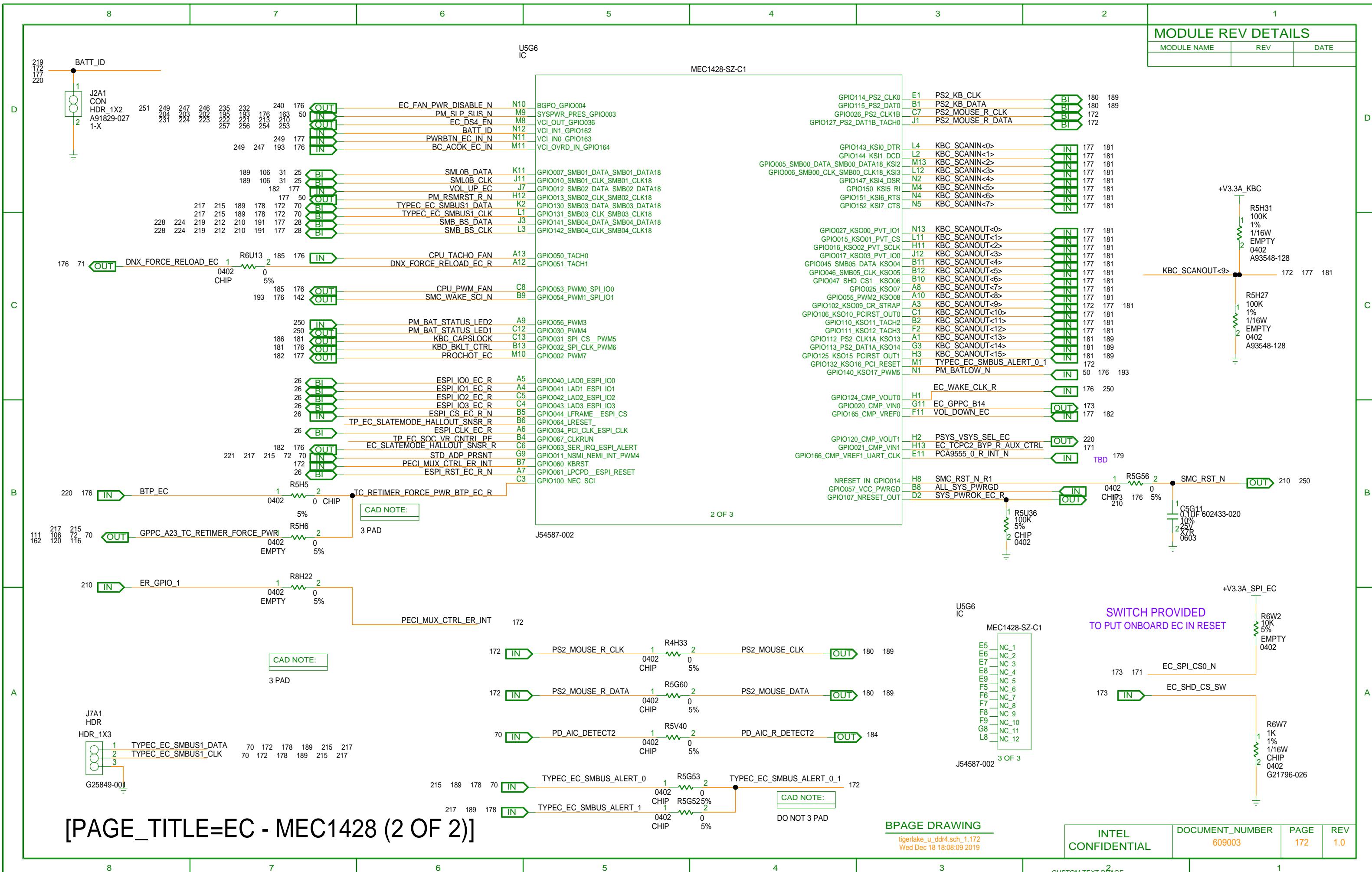
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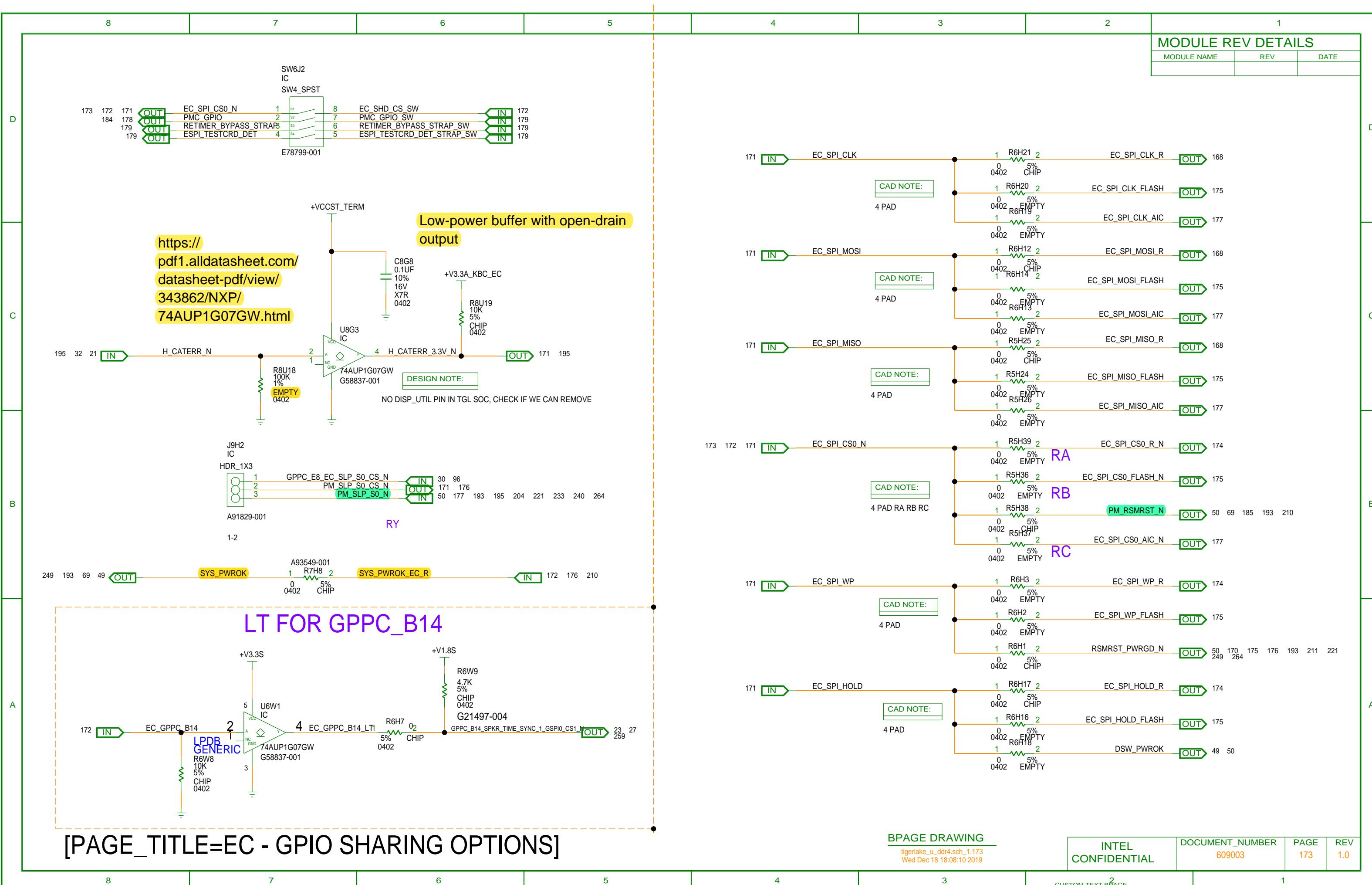
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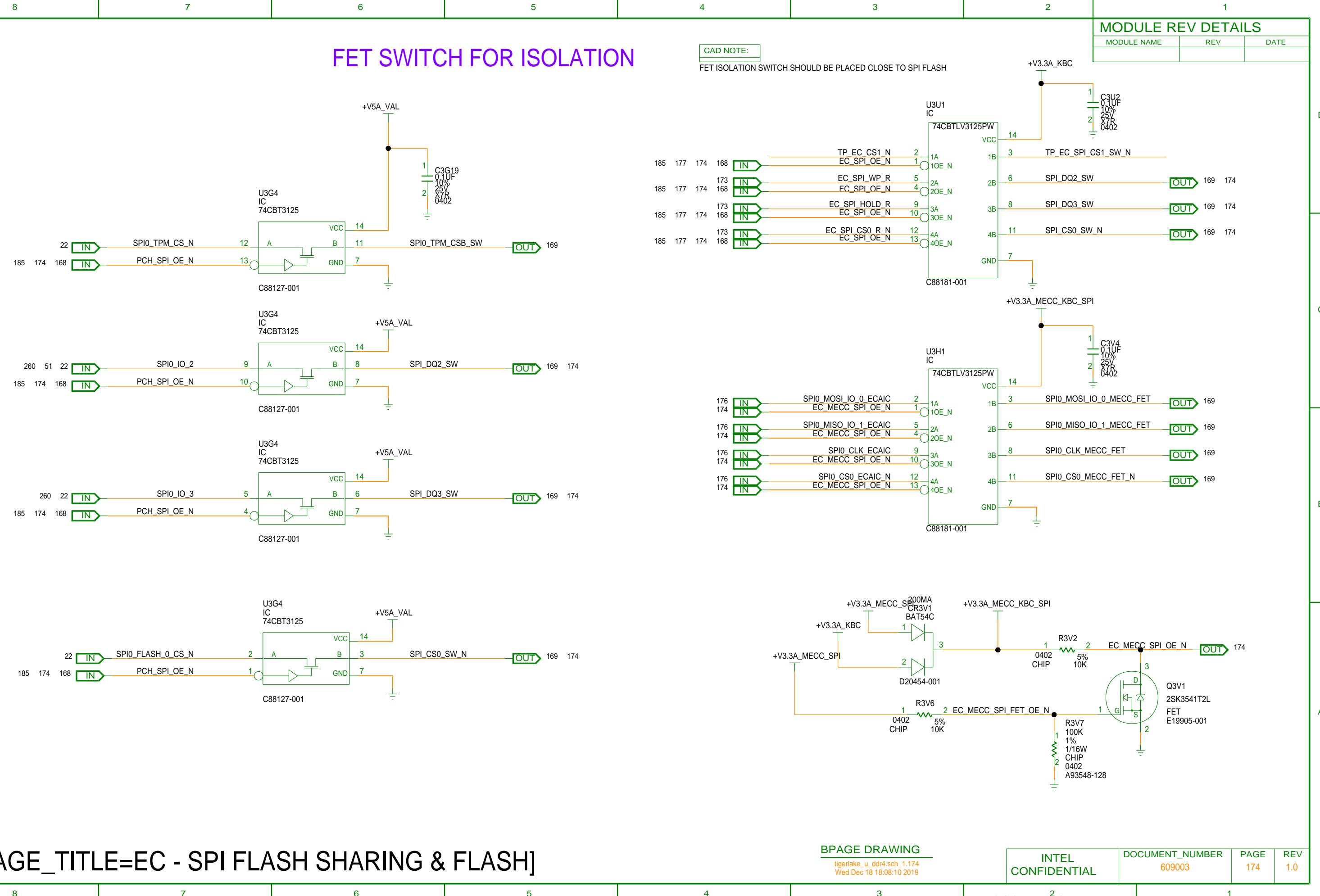
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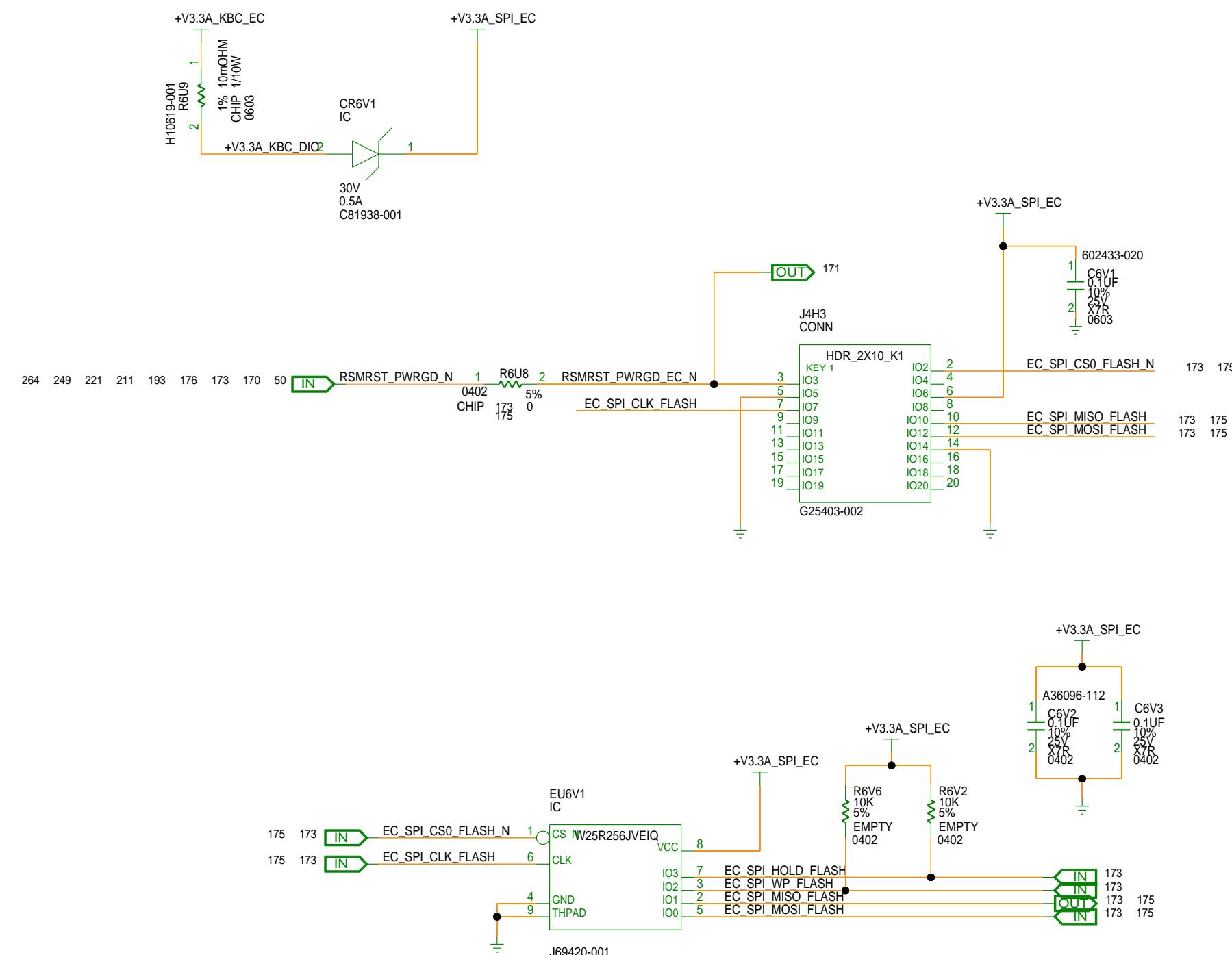






SF600 BASED TPM HEADER (DEDICATED FOR EC)

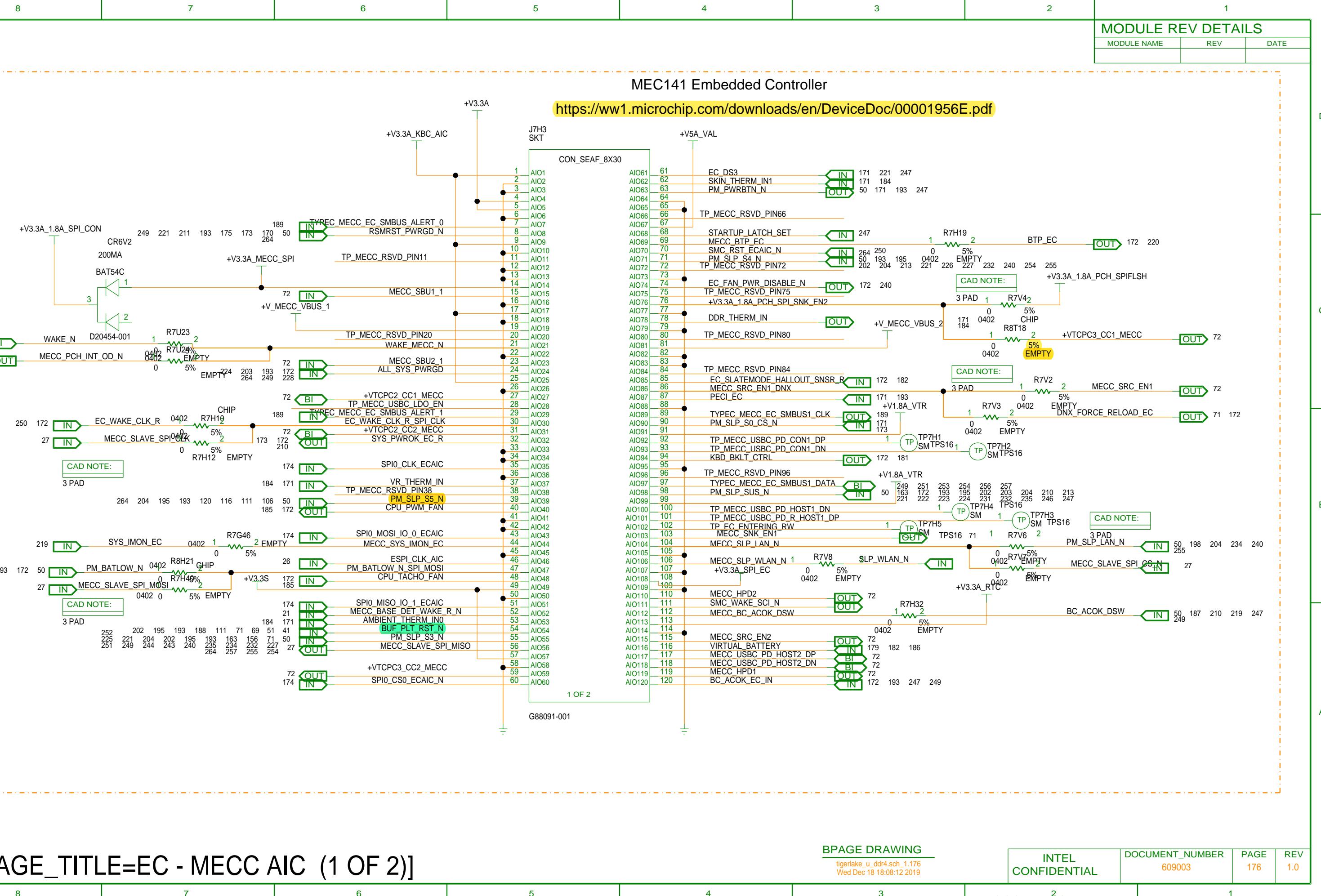
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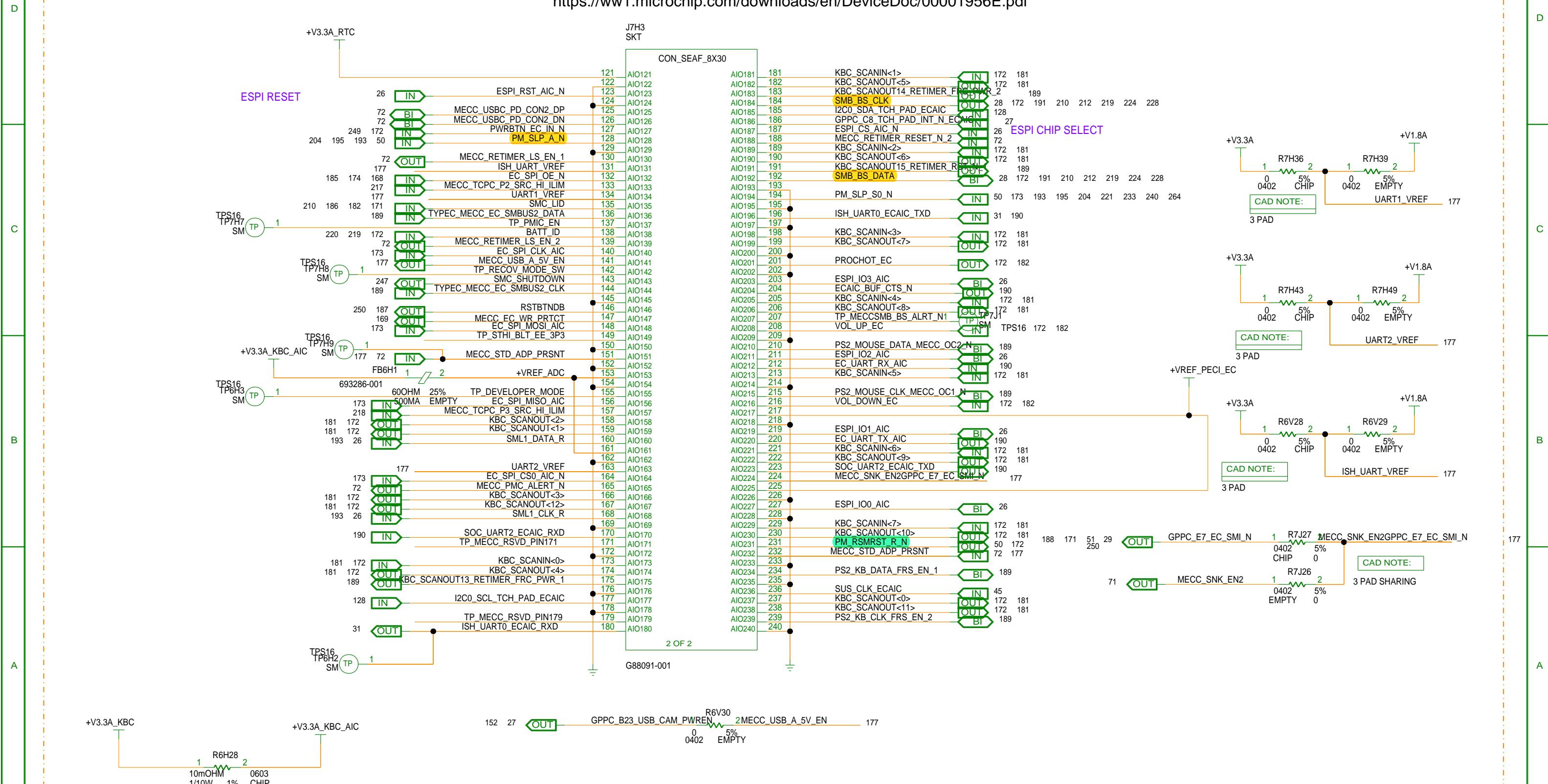
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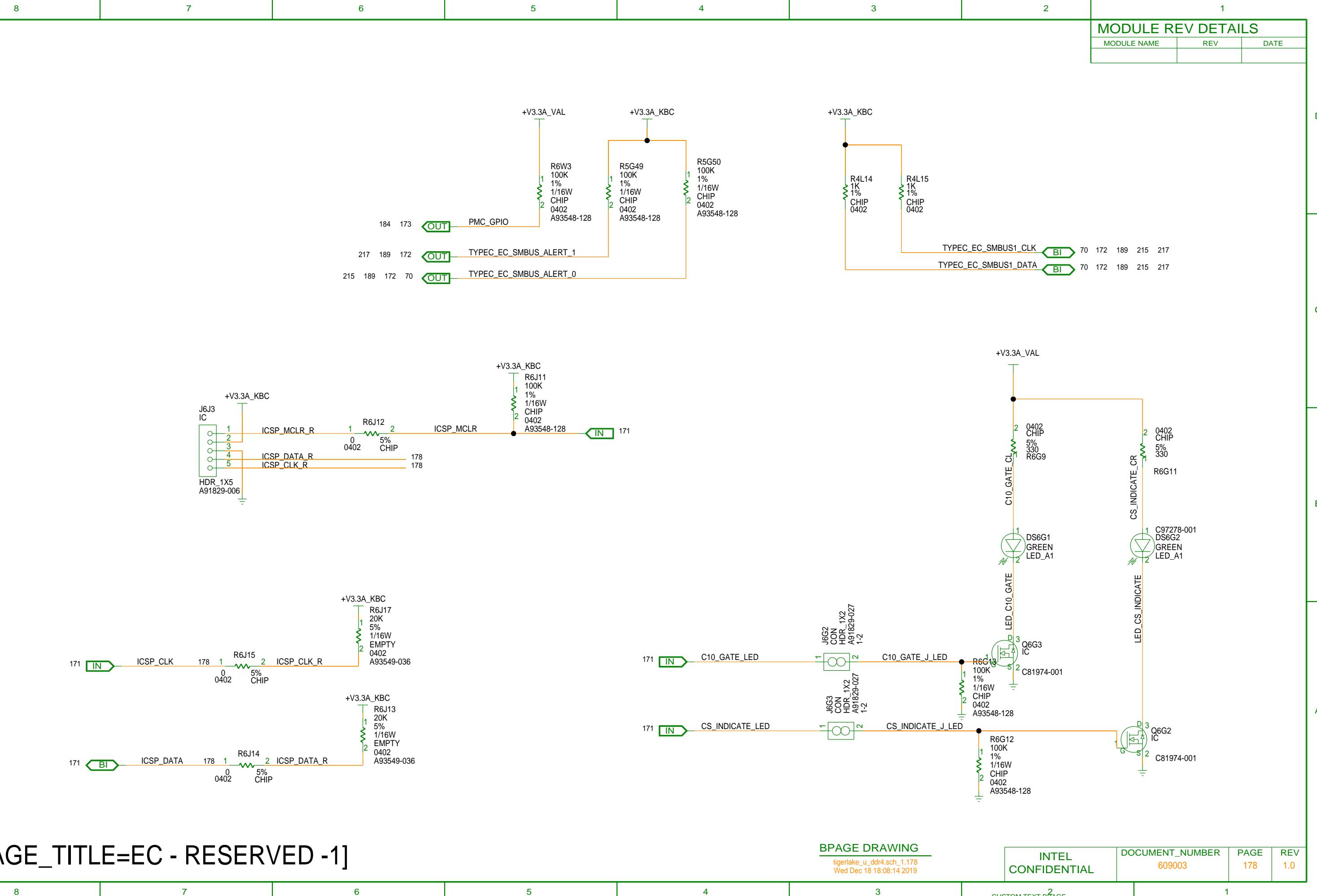
controller

<https://ww1.microchip.com/downloads/en/DeviceDoc/00001956E.pdf>

MODULE REV DETAILS

MODULE NAME	REV	DATE

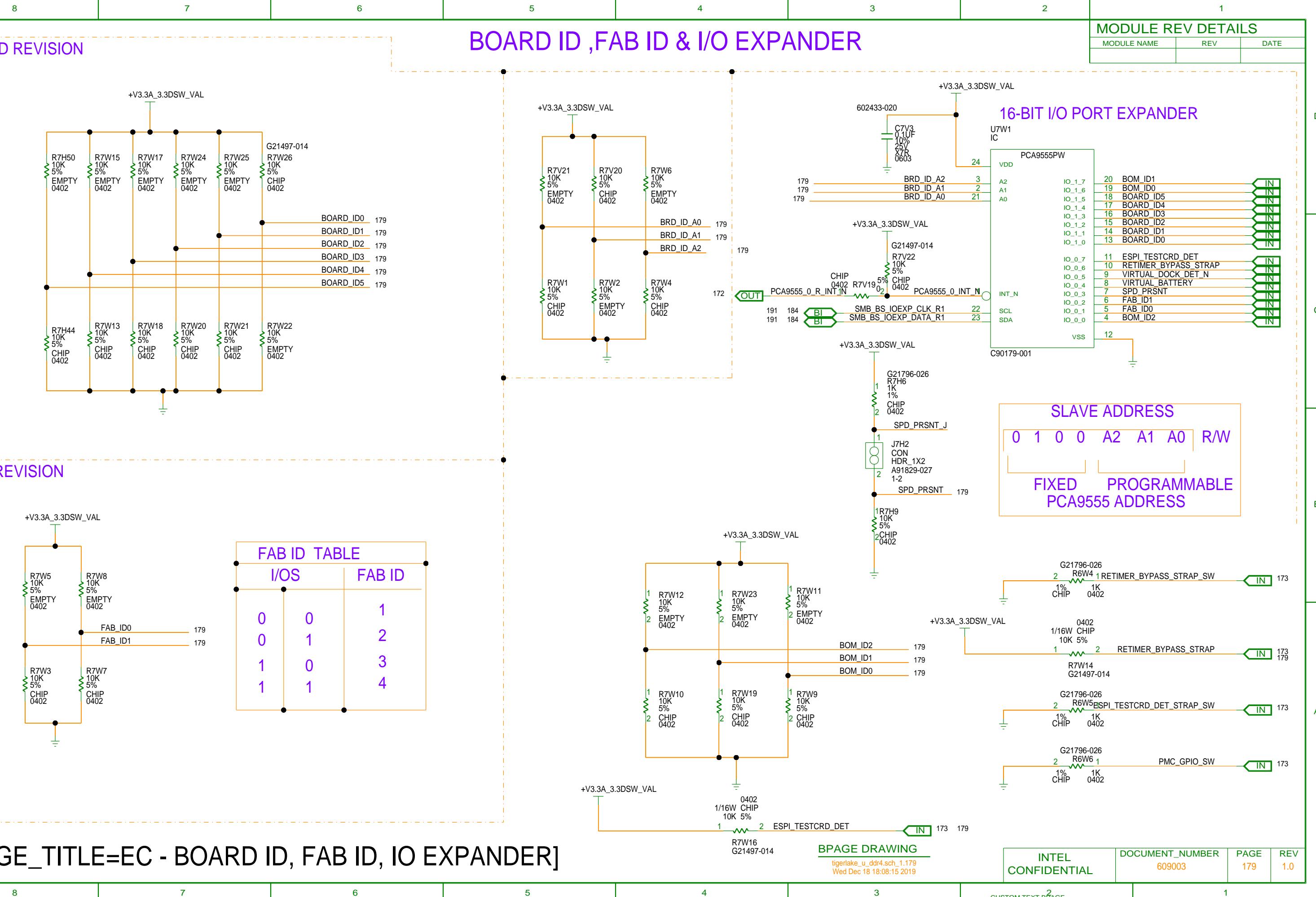


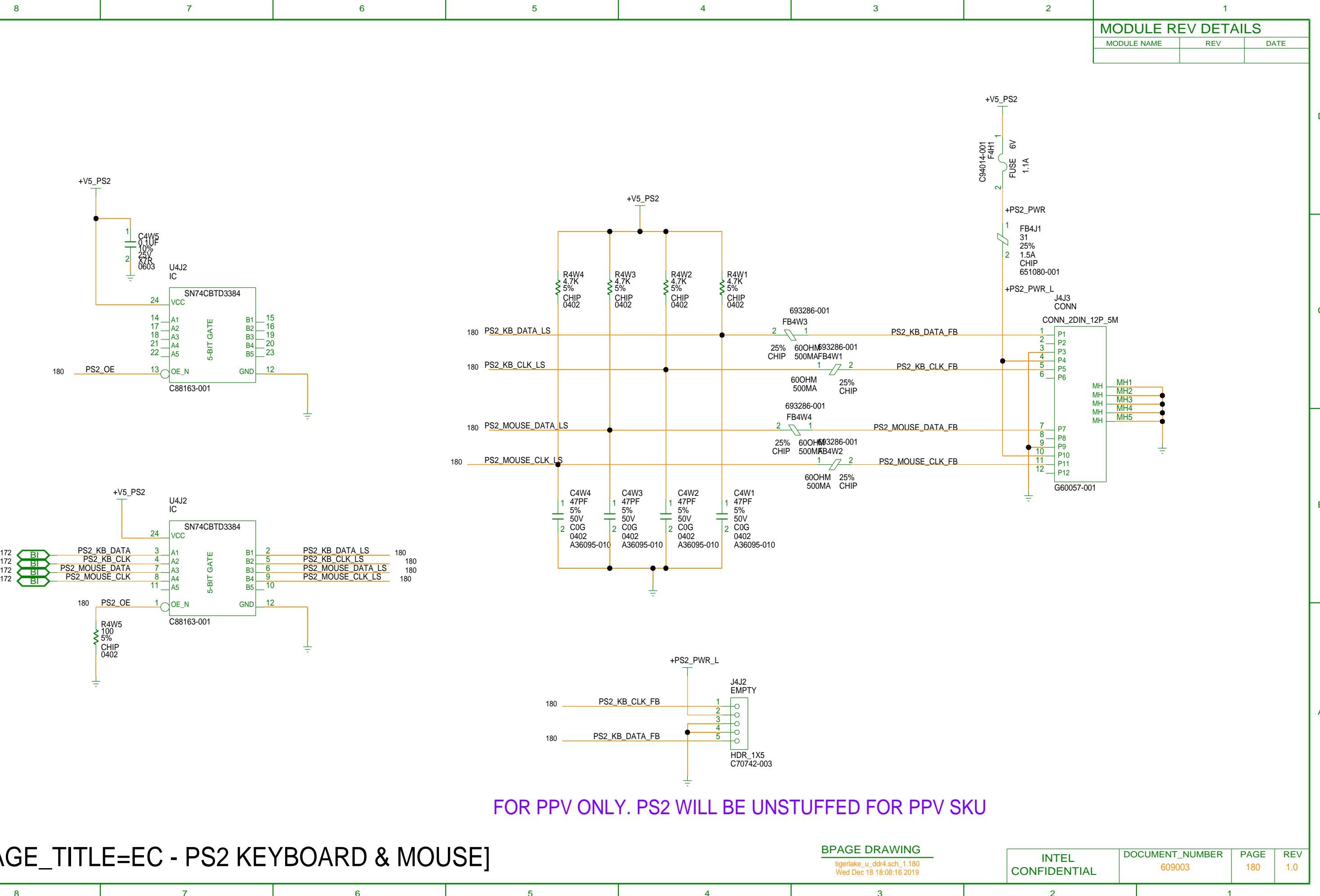


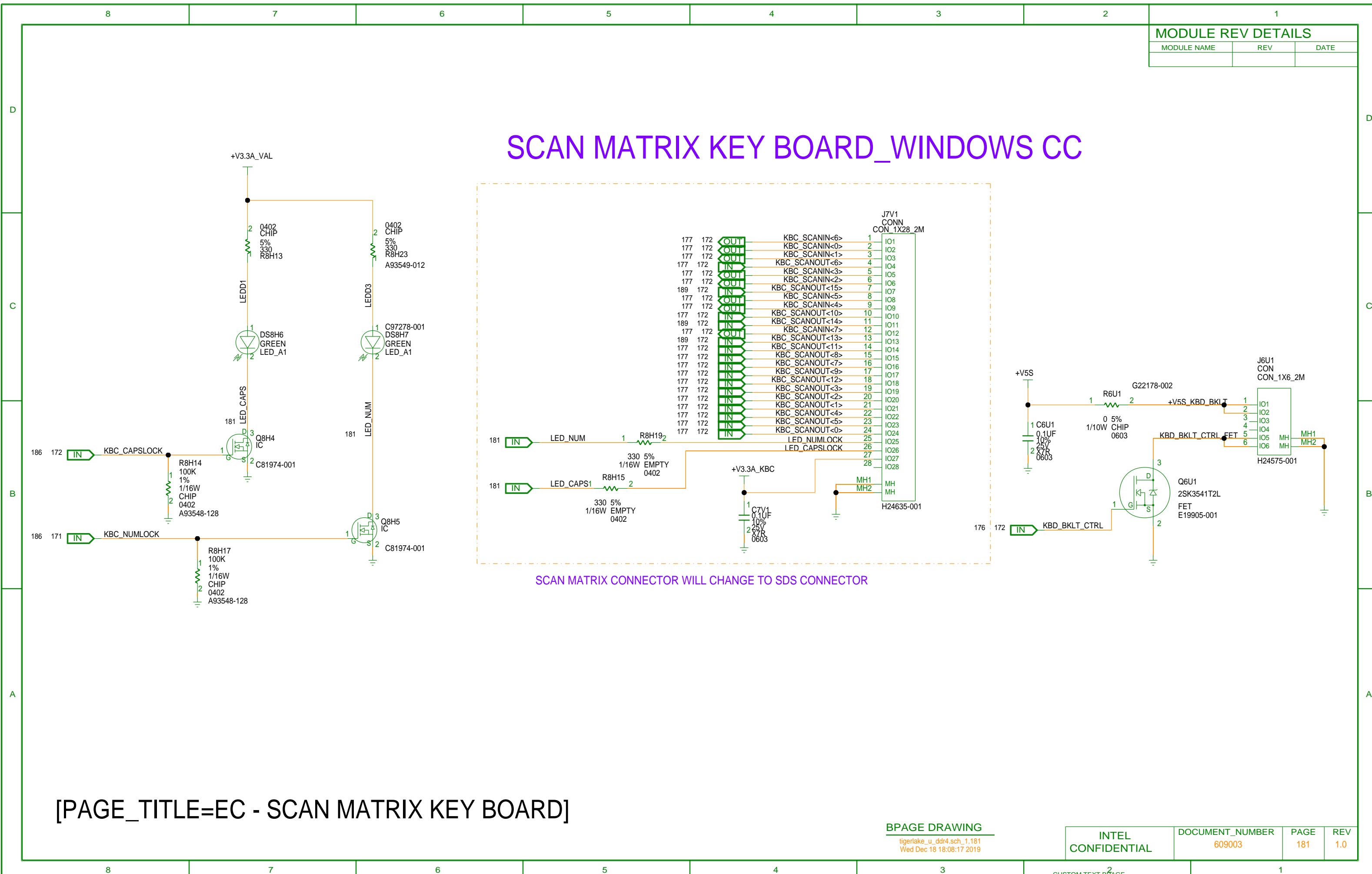
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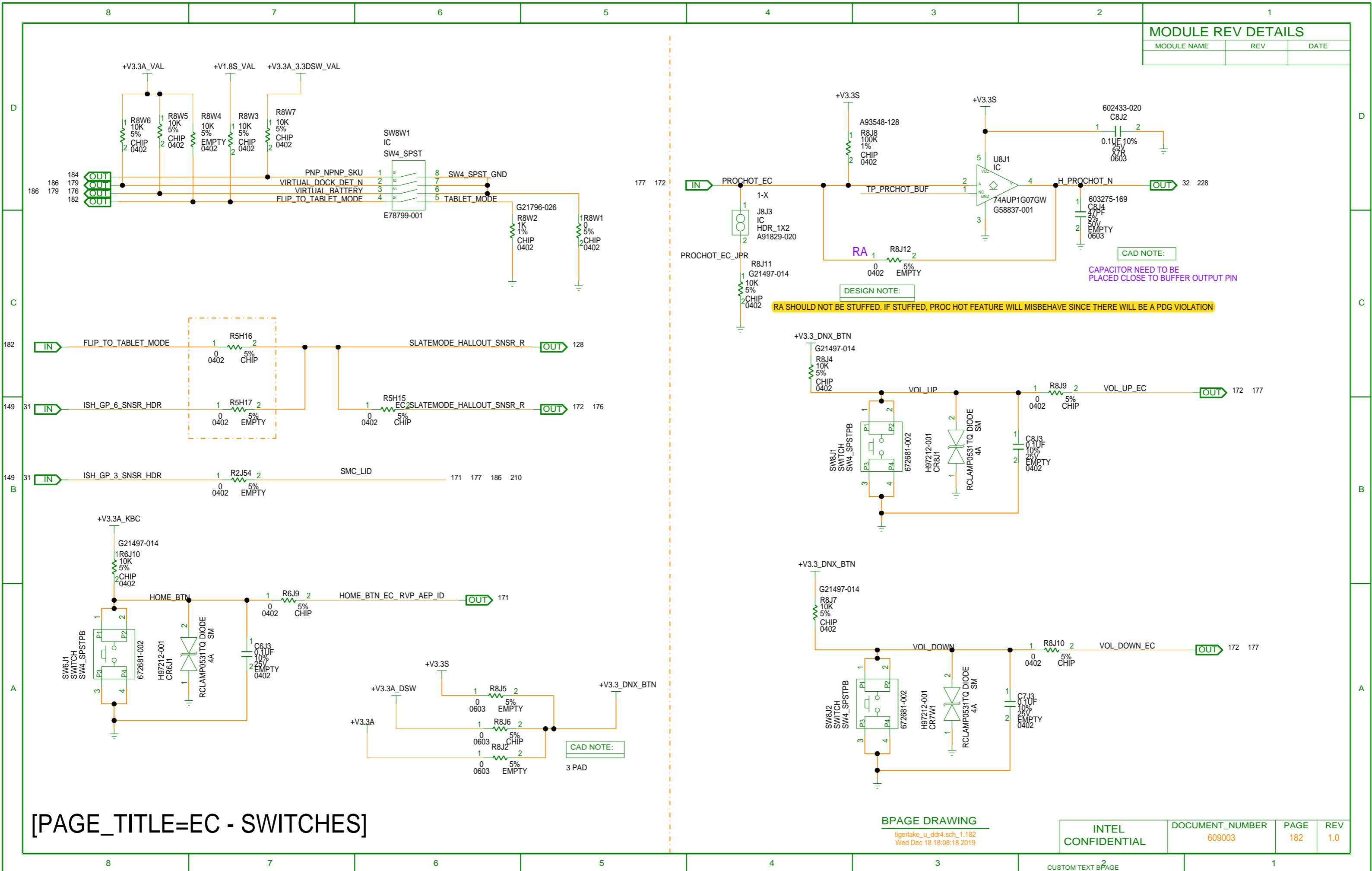
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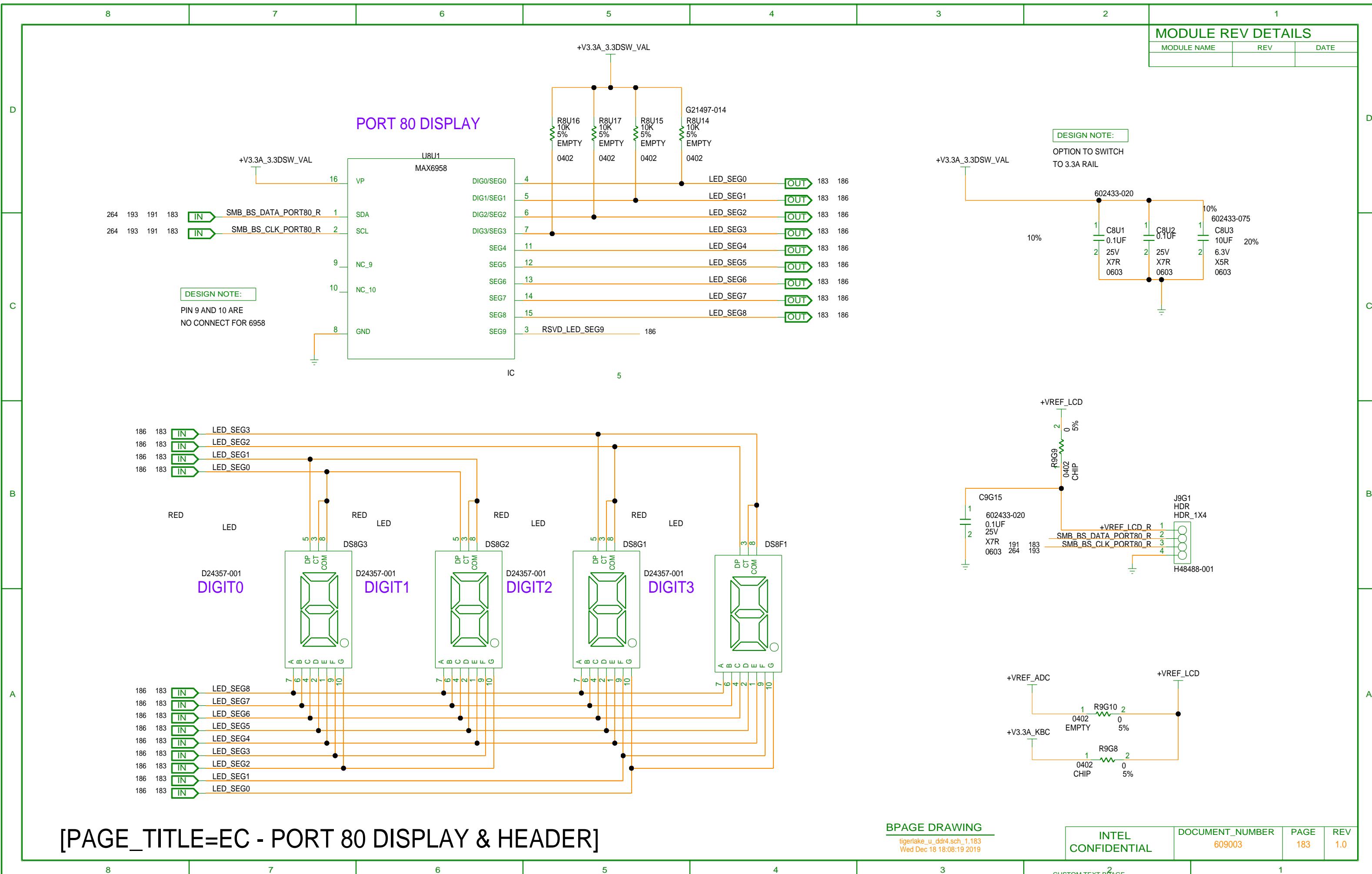
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 178	REV 1.0
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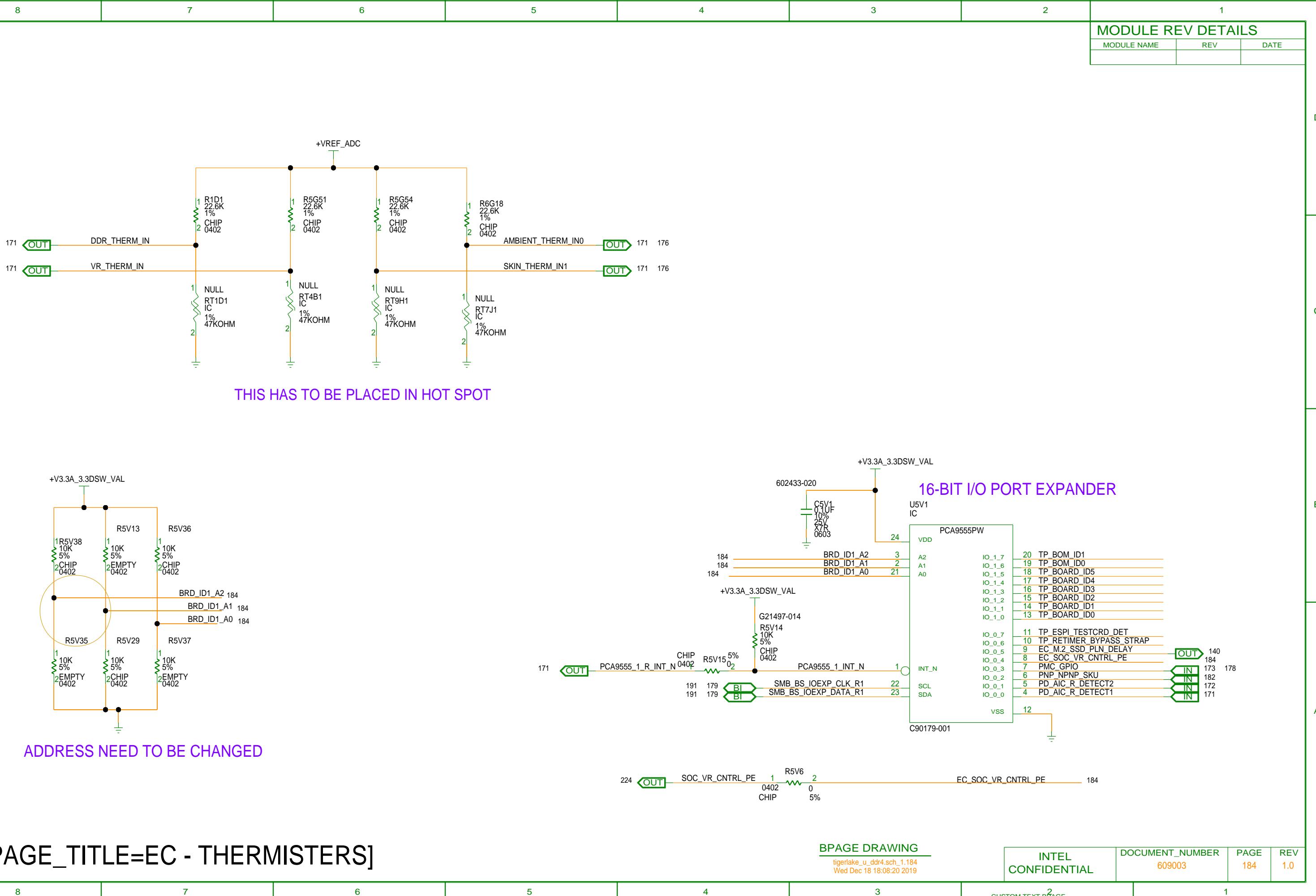








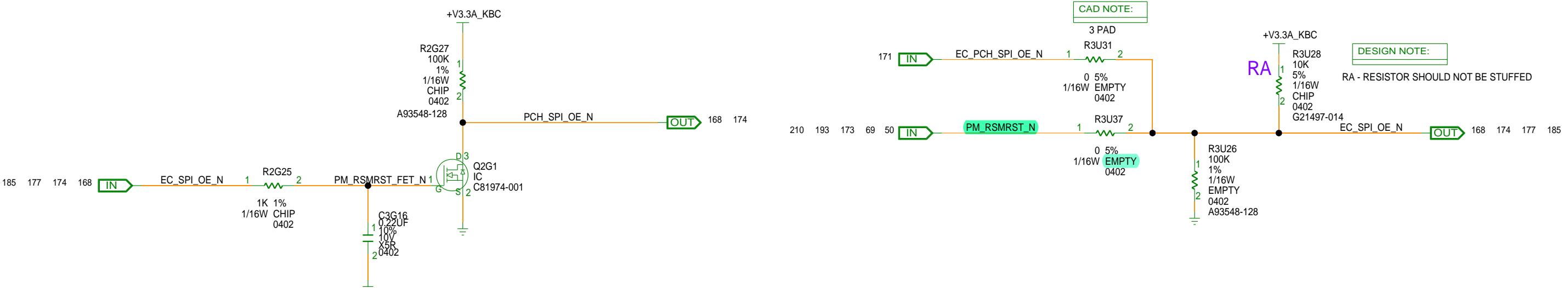
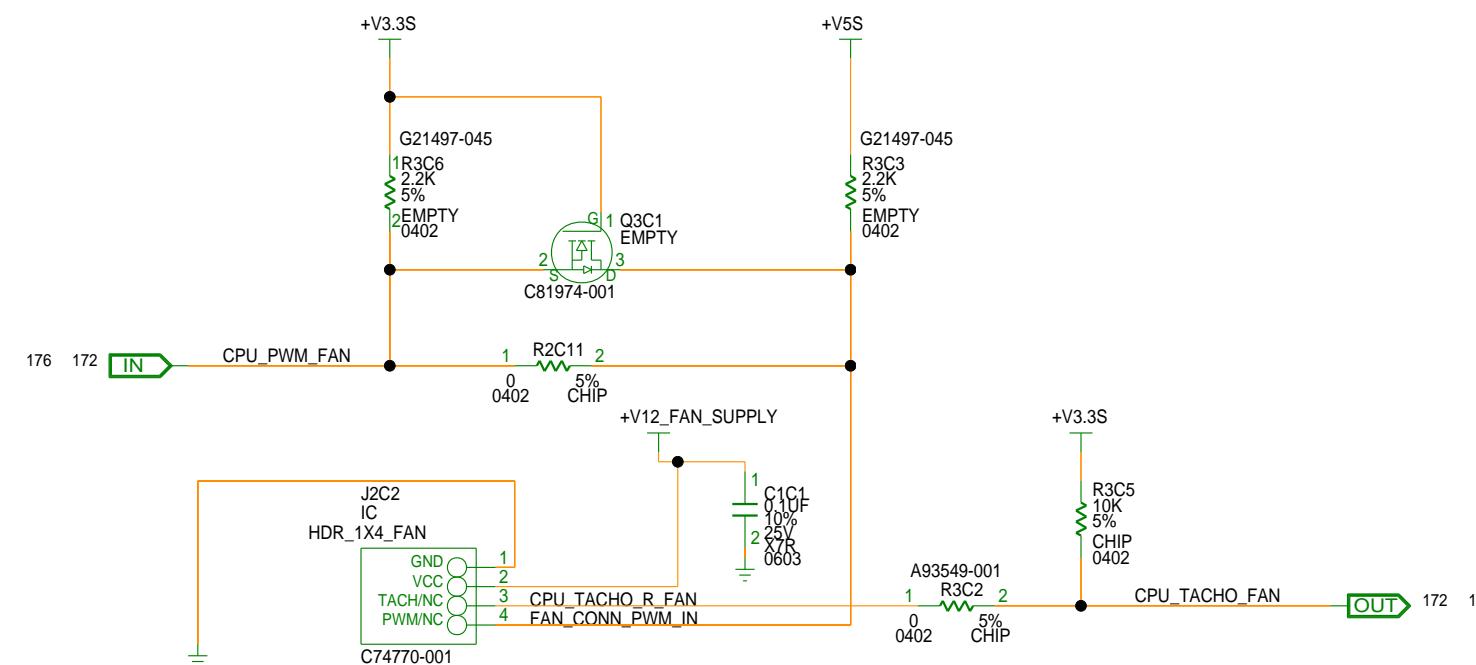




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MODULE REV DETAILS		
MODULE NAME	REV	DATE

PROCESSOR FAN CONTROL



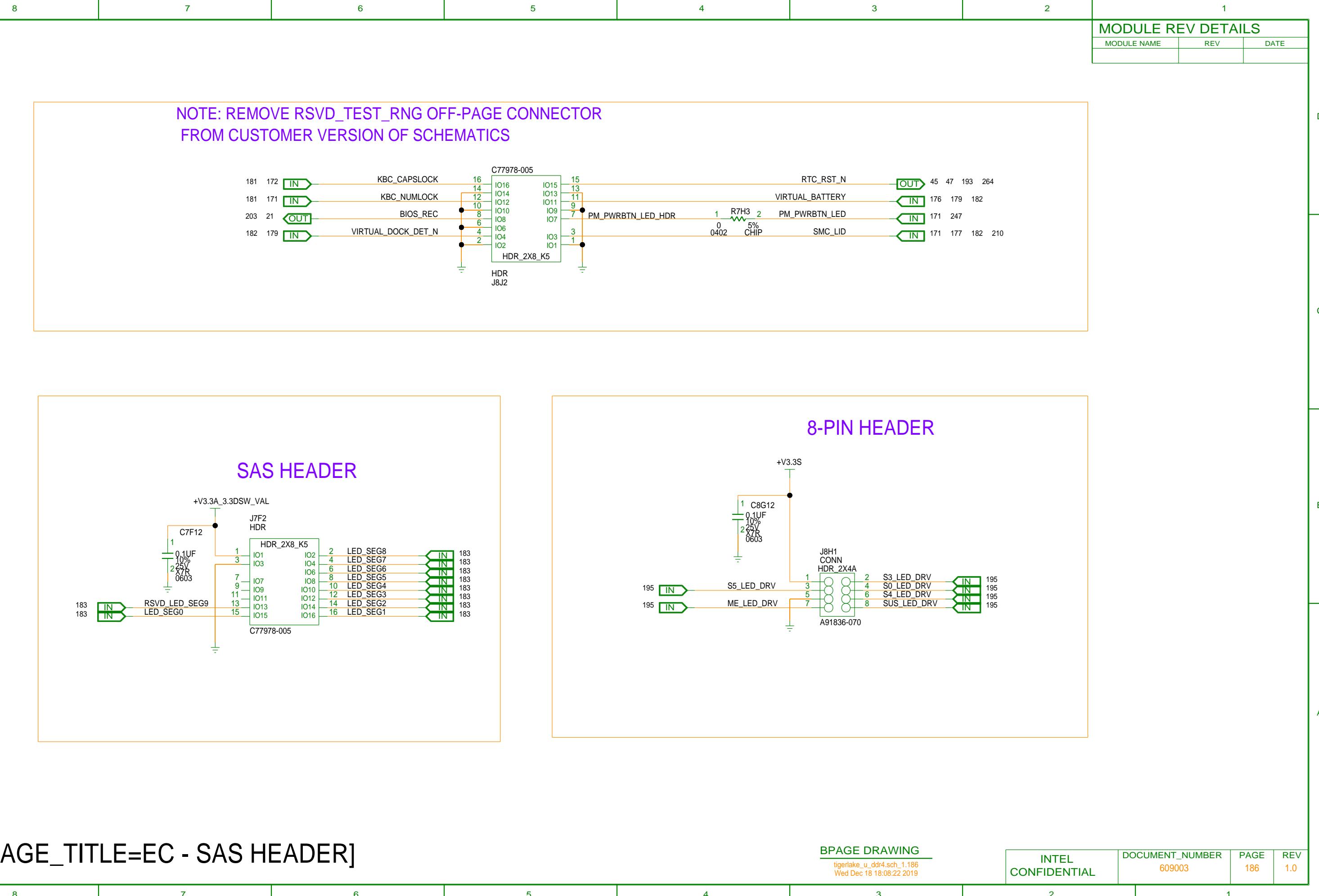
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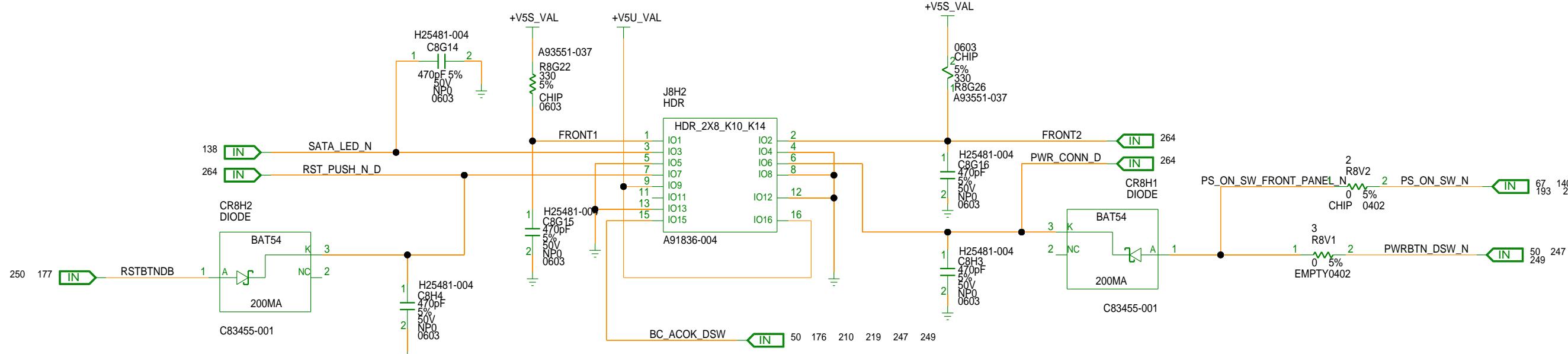
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MODULE NAME						REV	DATE

FRONT PANEL HEADER



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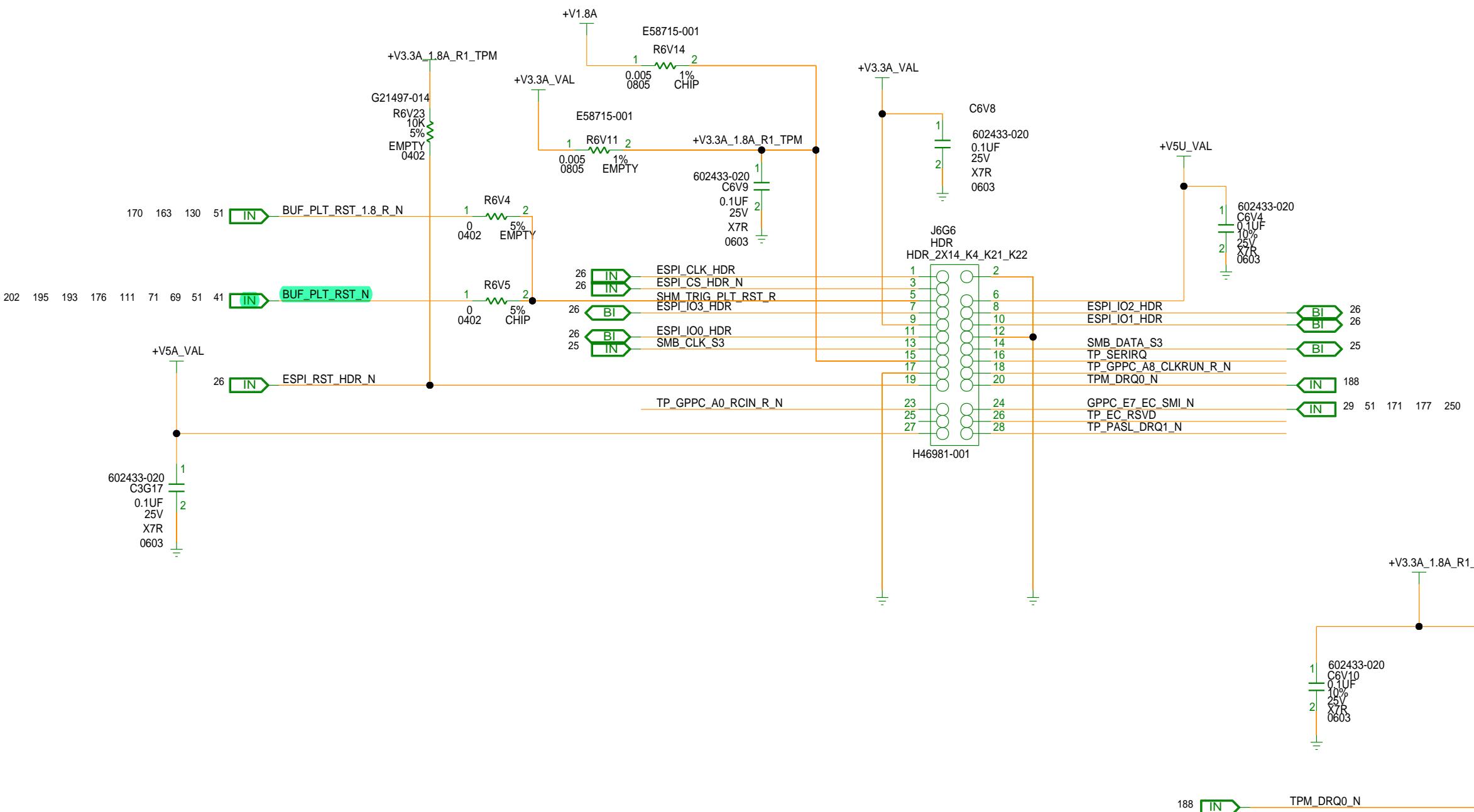
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ESPI BUS HEADER

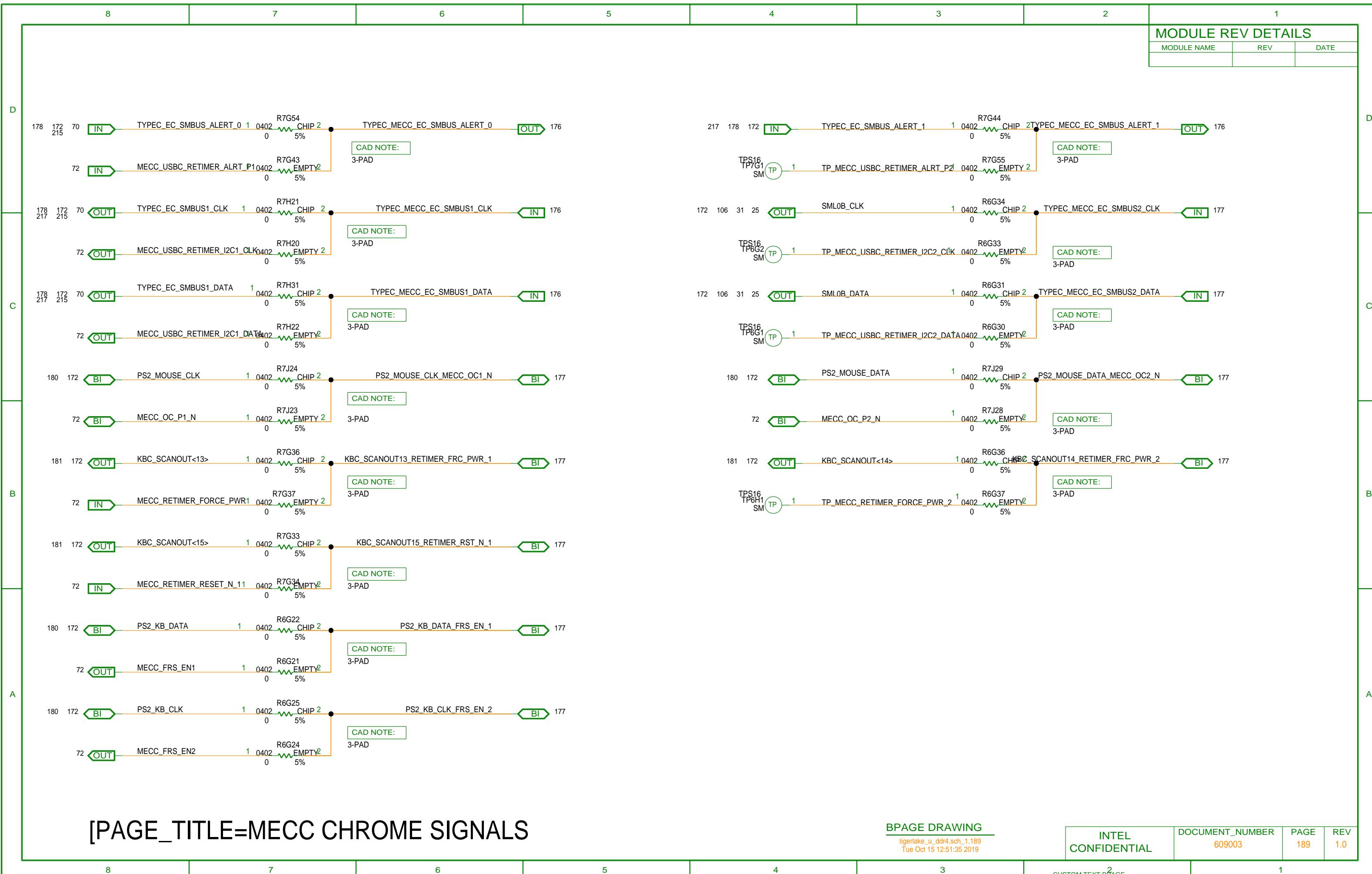


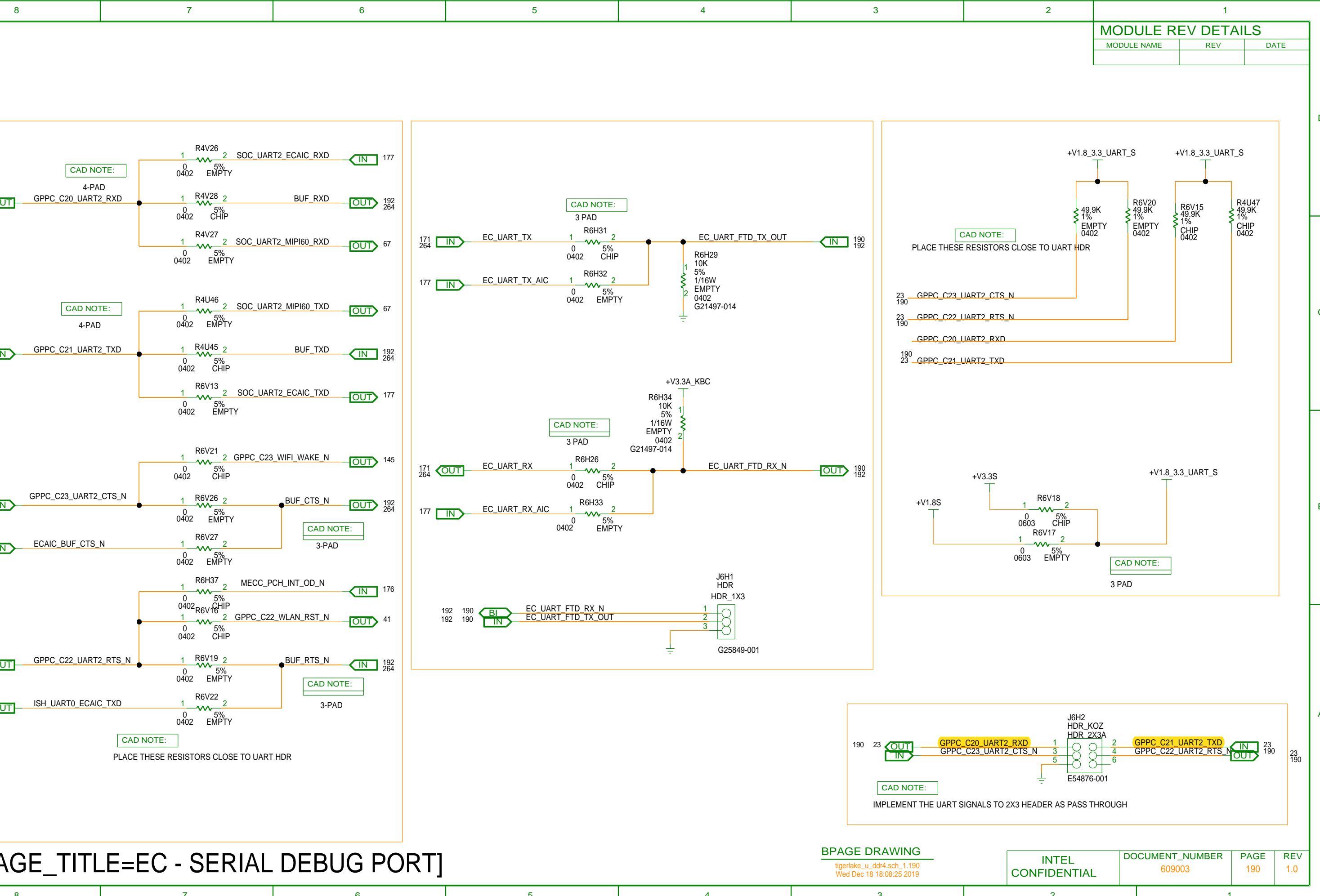
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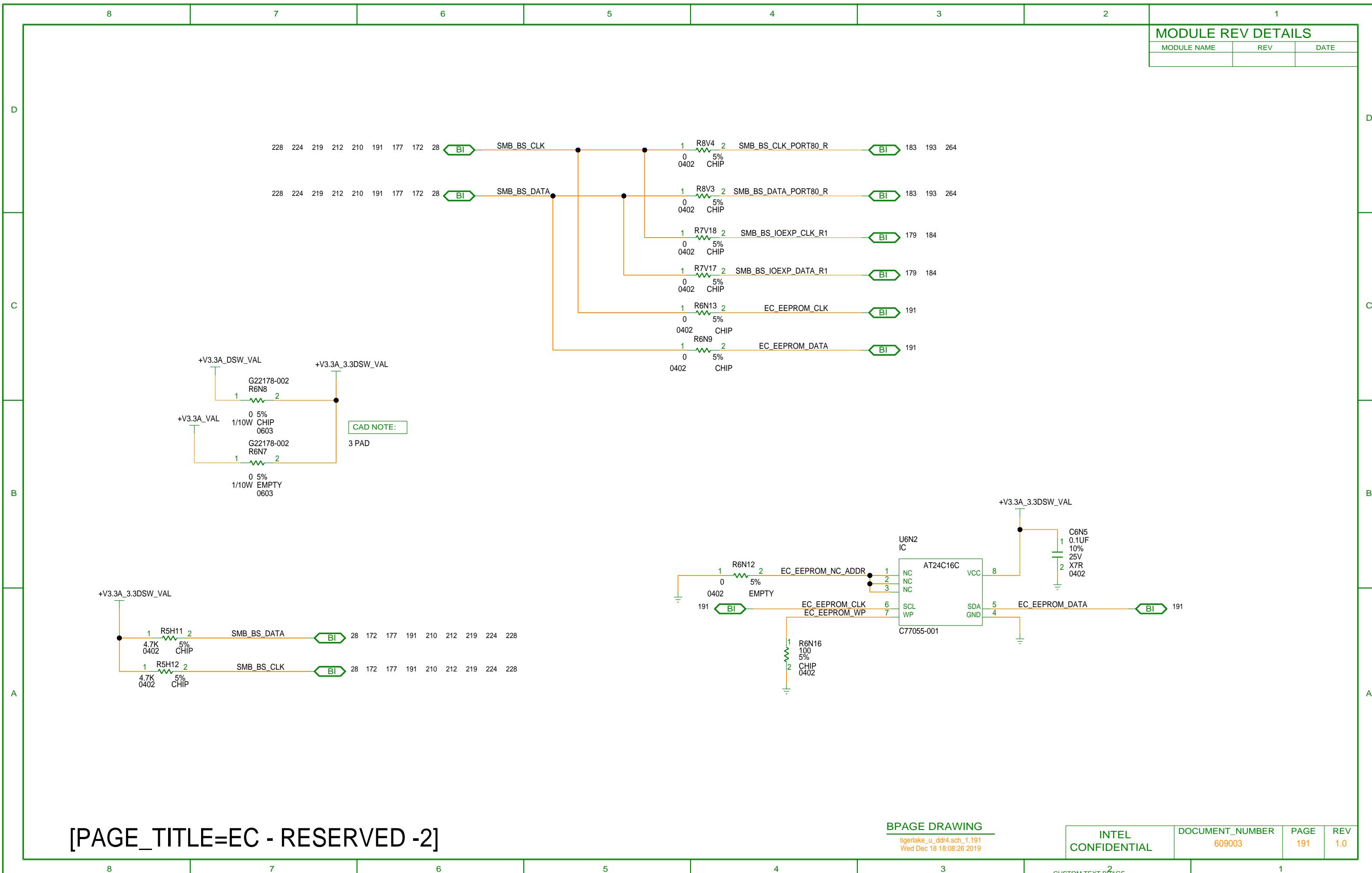
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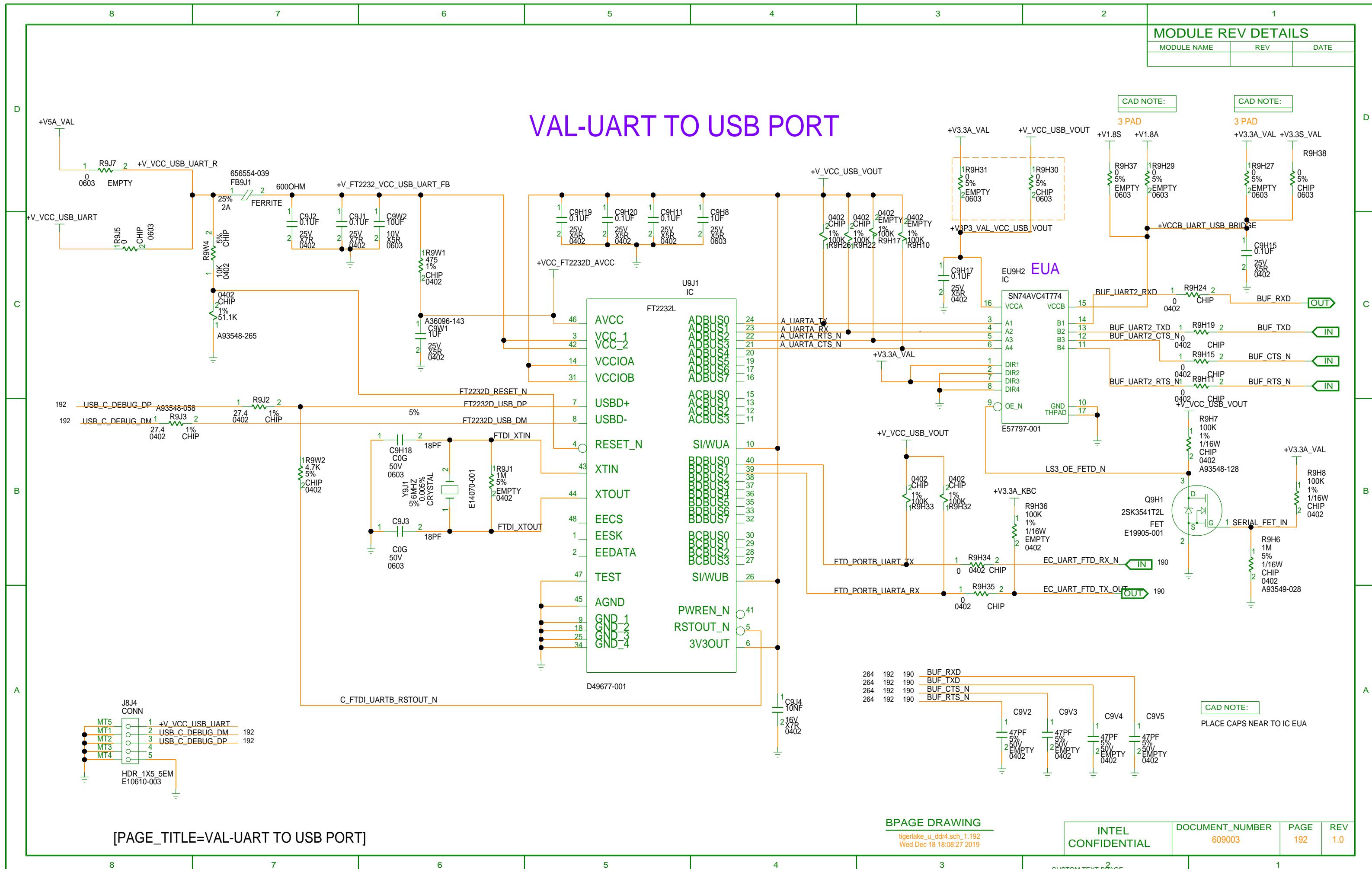
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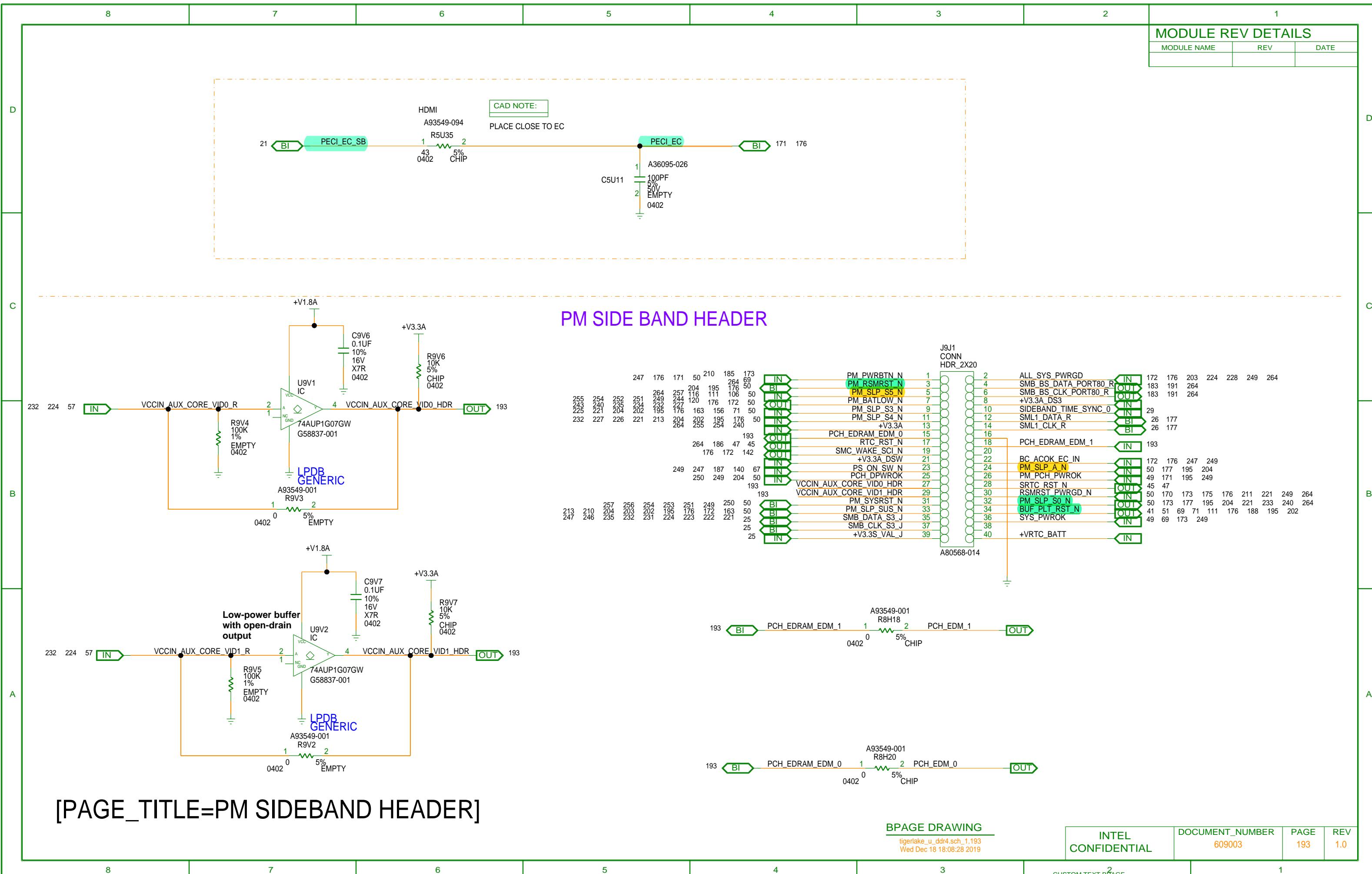
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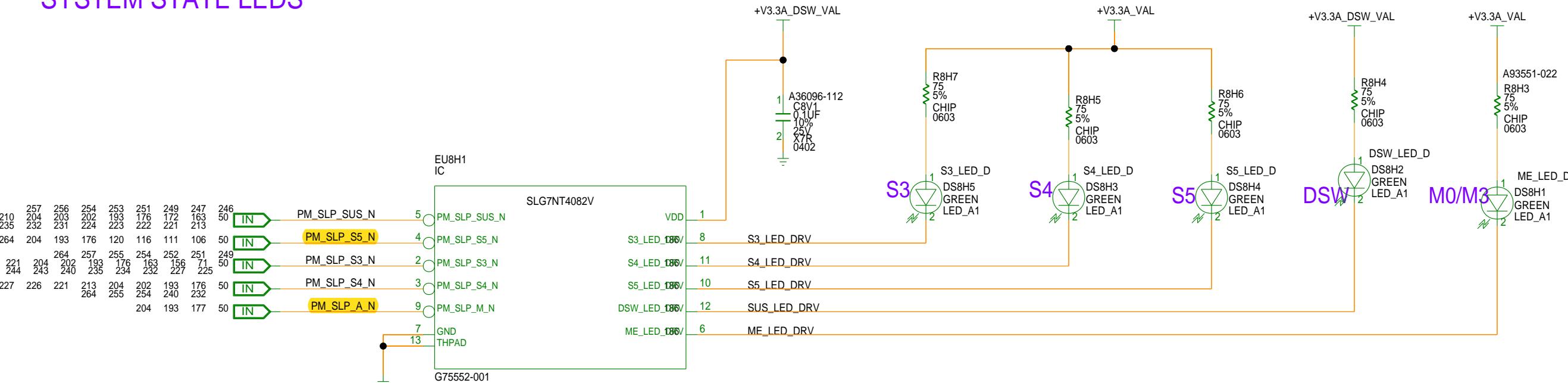
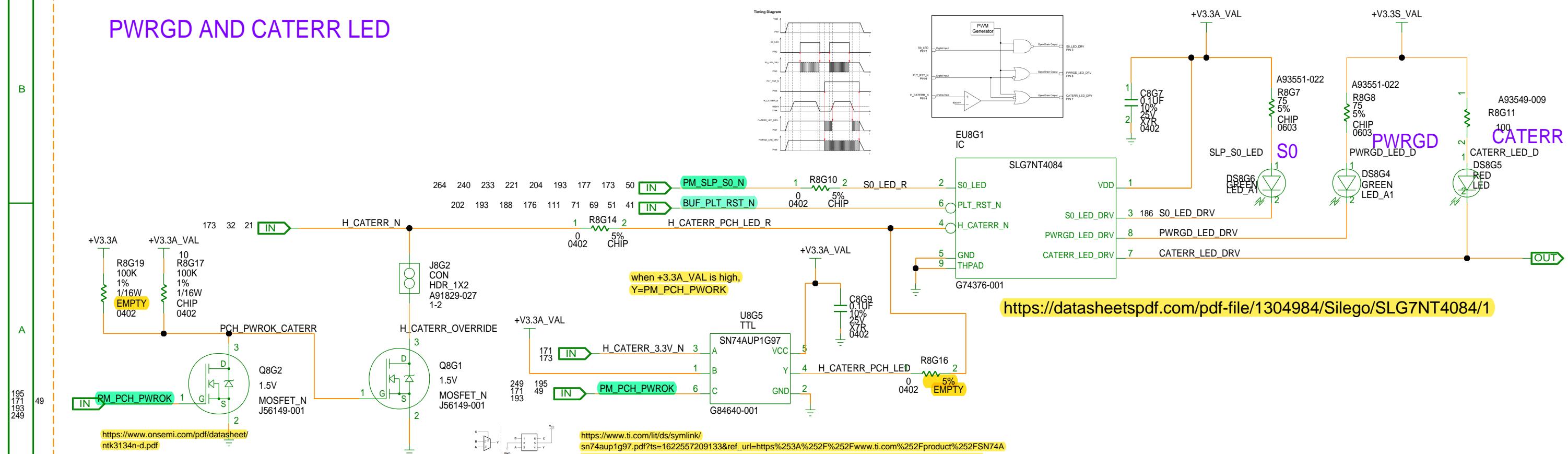
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 194	REV 1.0
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MODULE REV DETAILS

MODULE NAME	REV	DATE

SYSTEM STATE LEDS**PWRGD AND CATERR LED**

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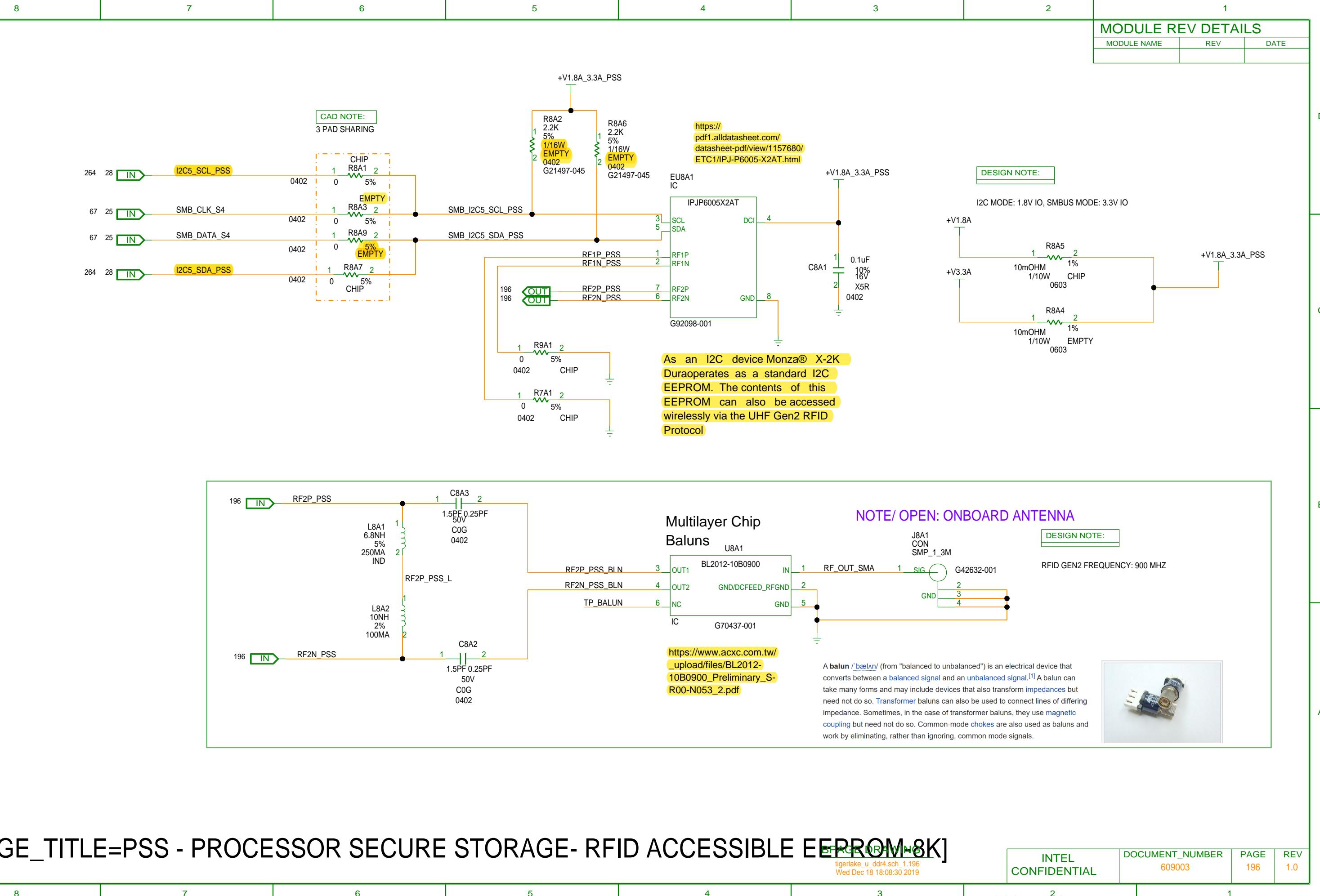
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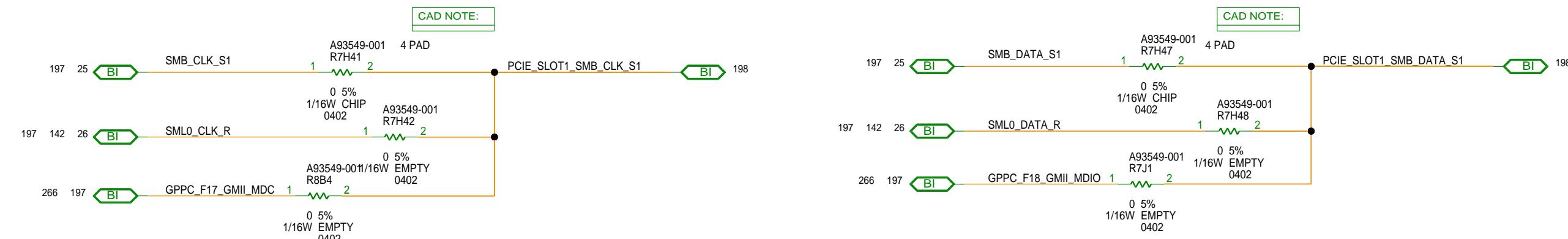
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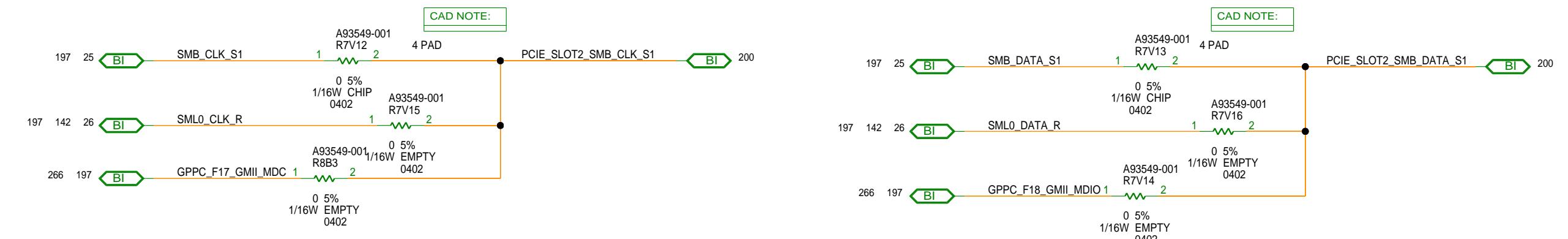


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MODULE NAME				REV	DATE		

PCIE SLOT 1 SMB SIGNALS



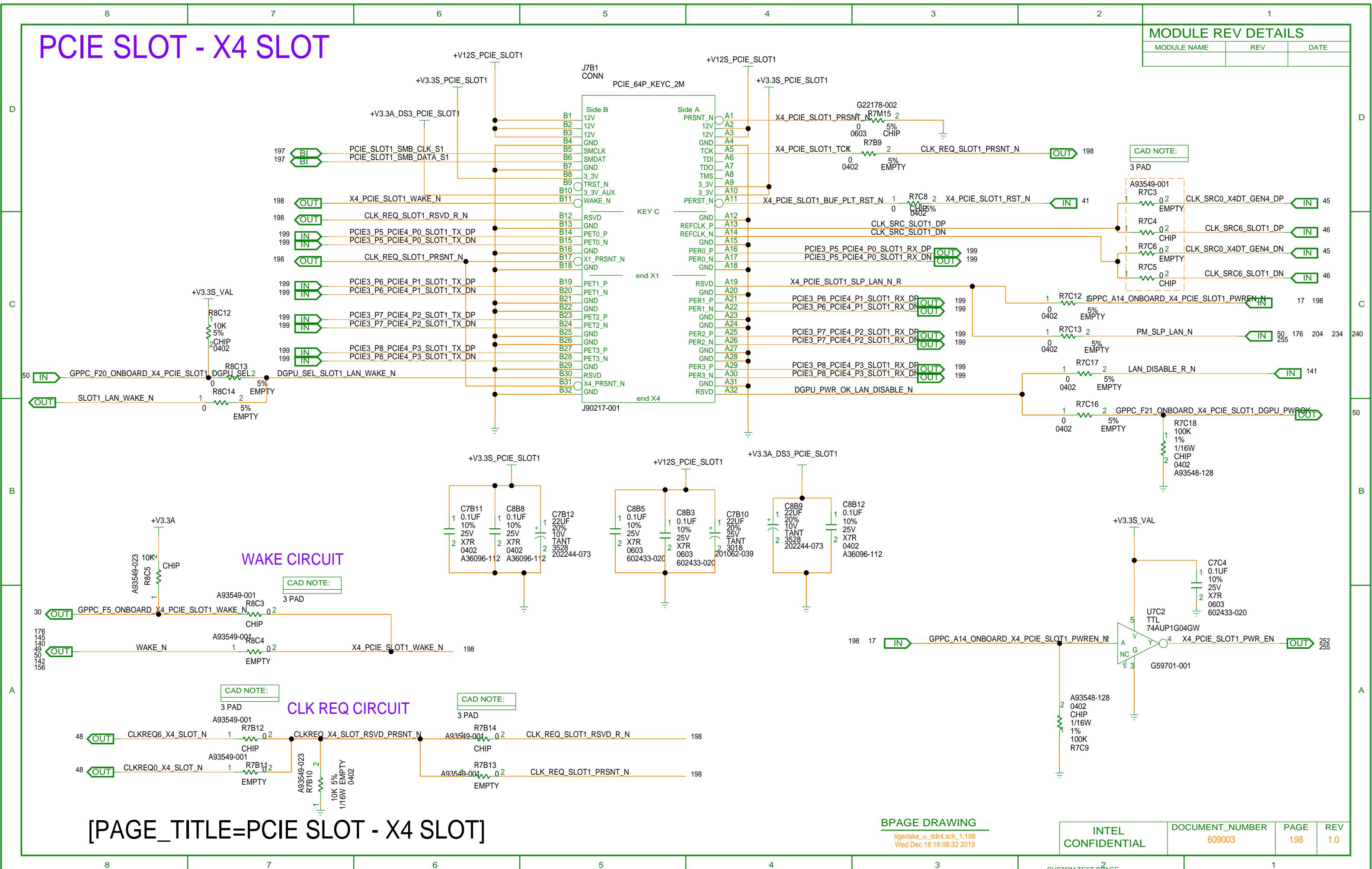
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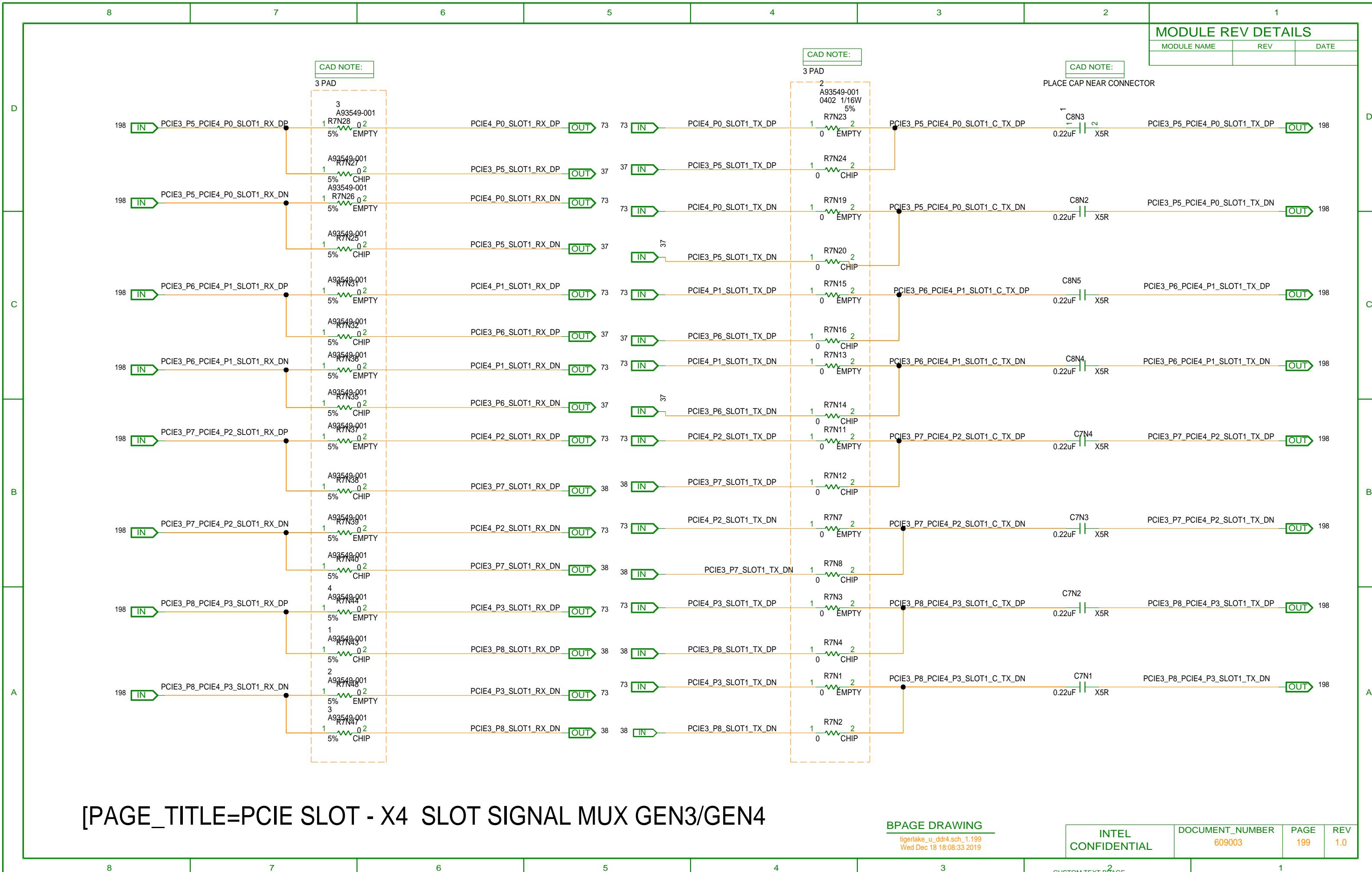


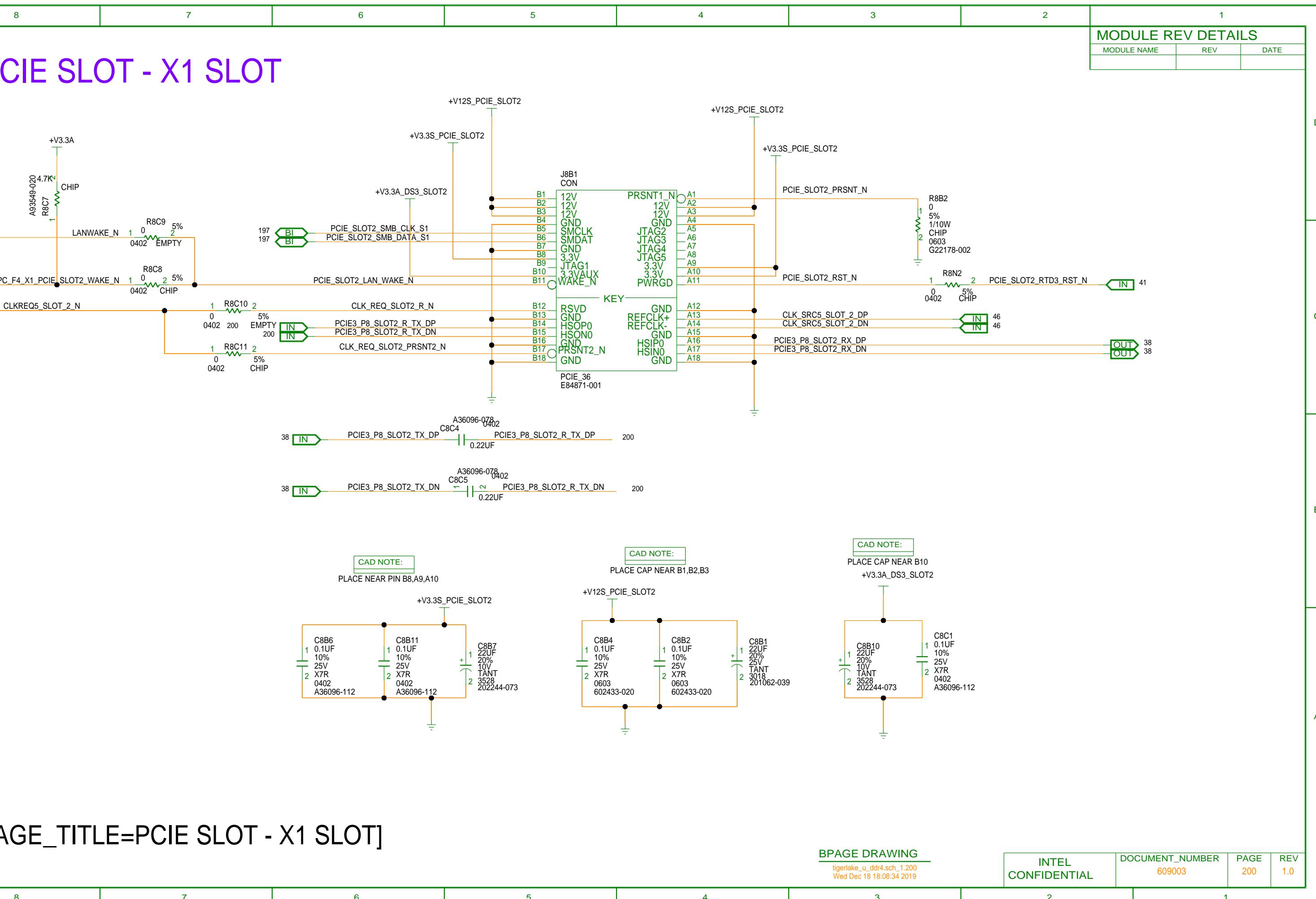
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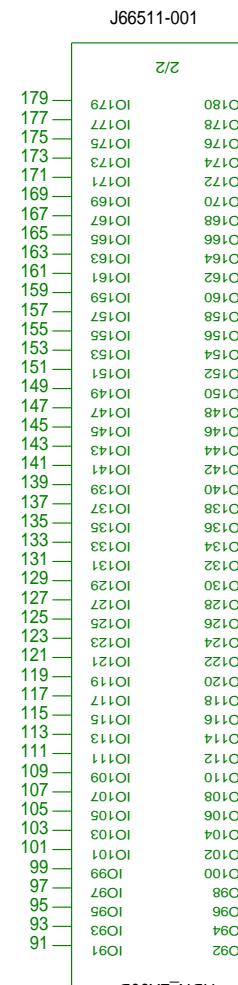




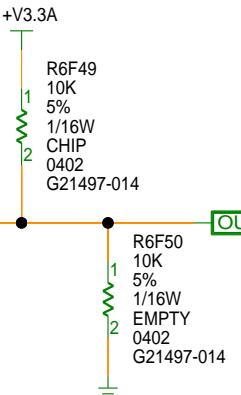
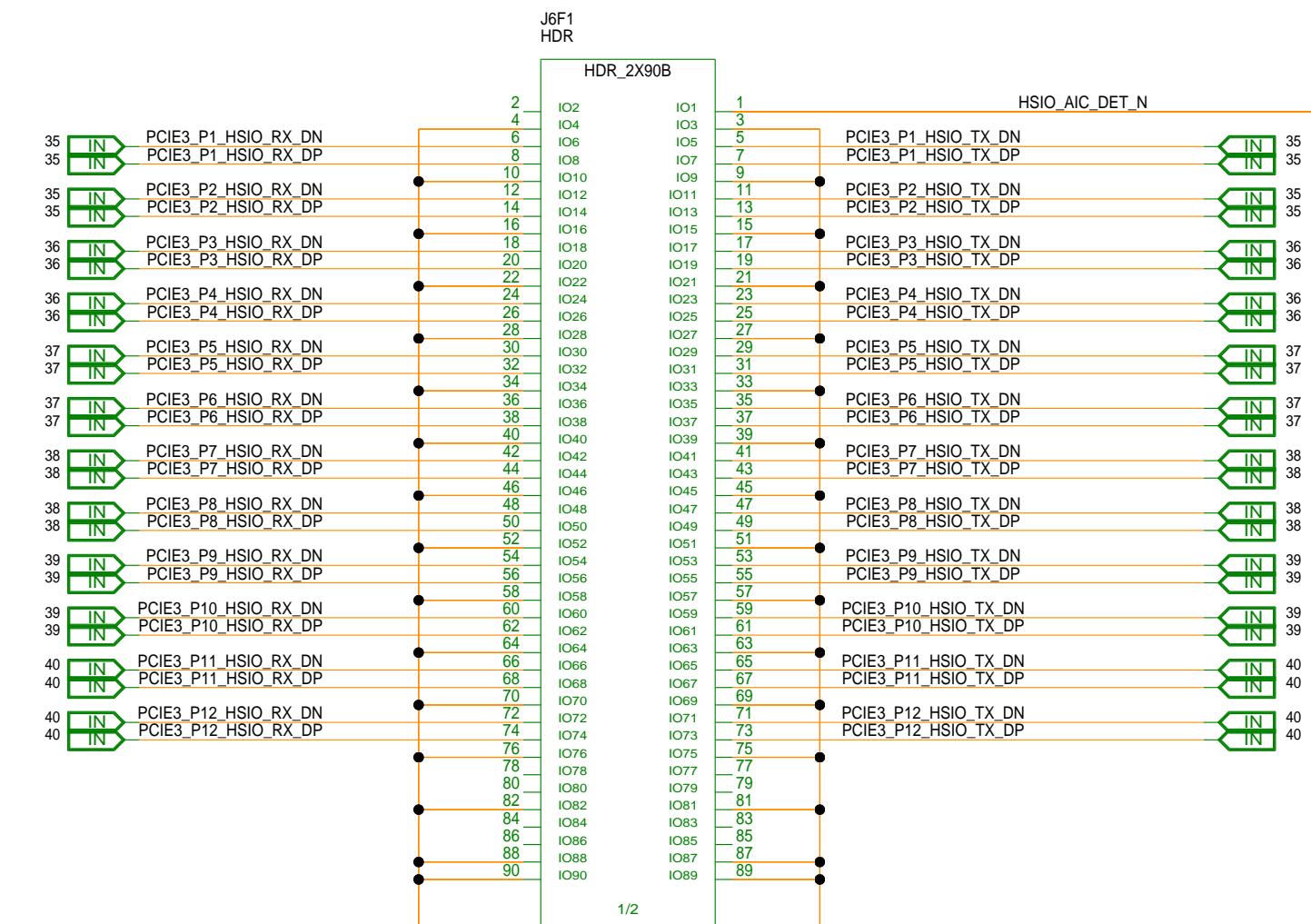


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MODULE REV DETAILS							
MODULE NAME						REV	DATE

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



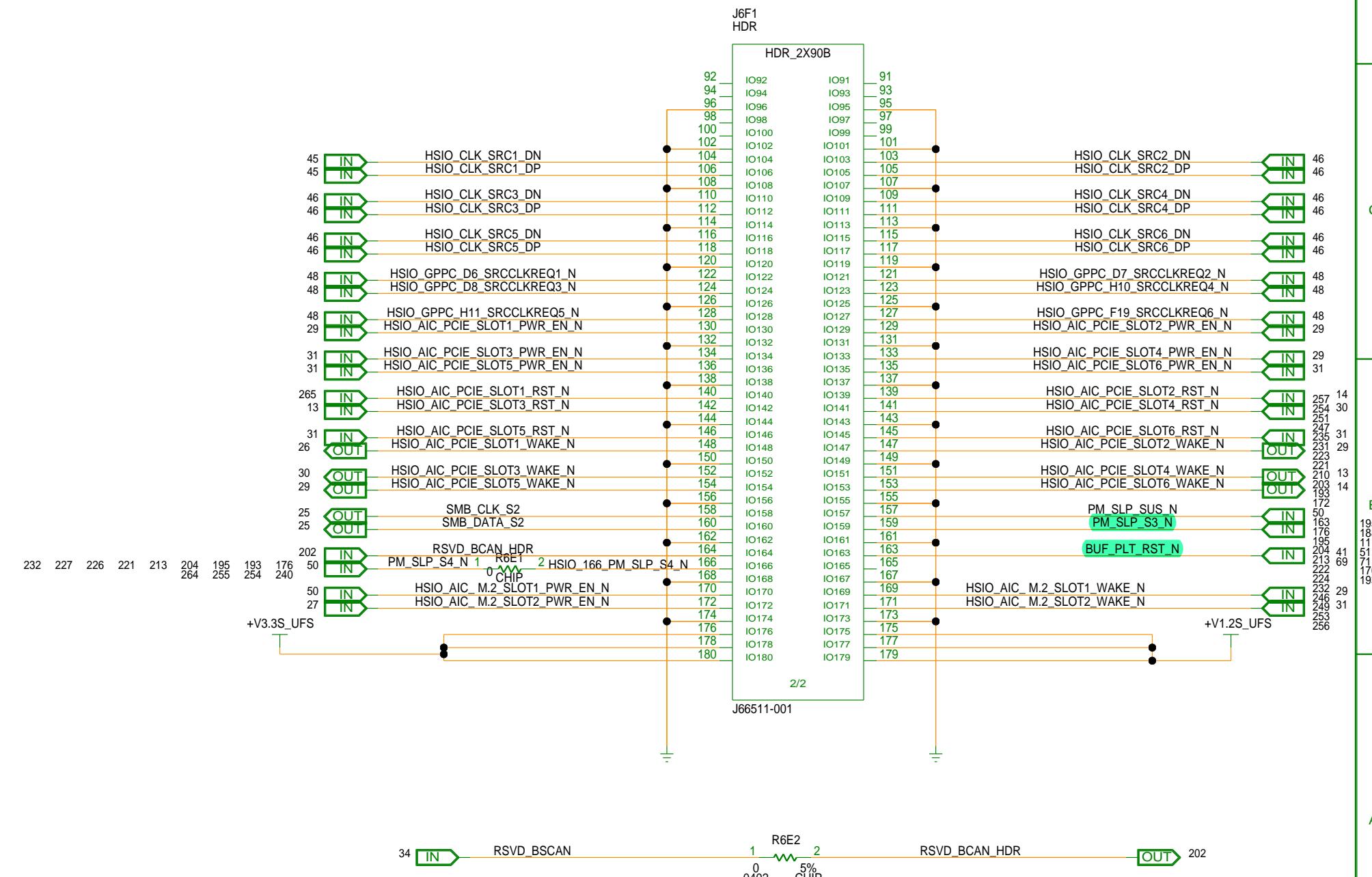
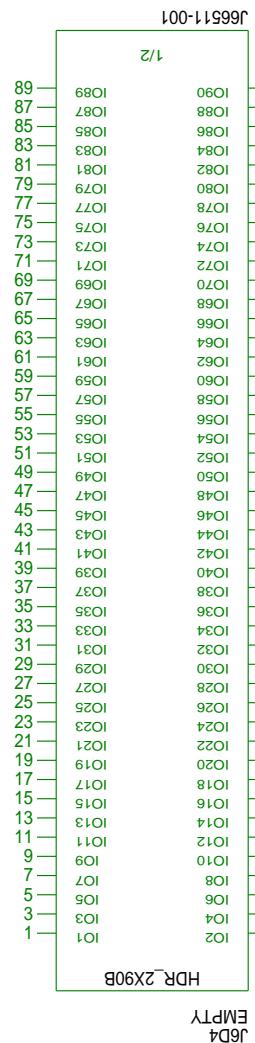
J6D4
EMPTY



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MODULE REV DETAILS		
MODULE NAME	REV	DATE

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



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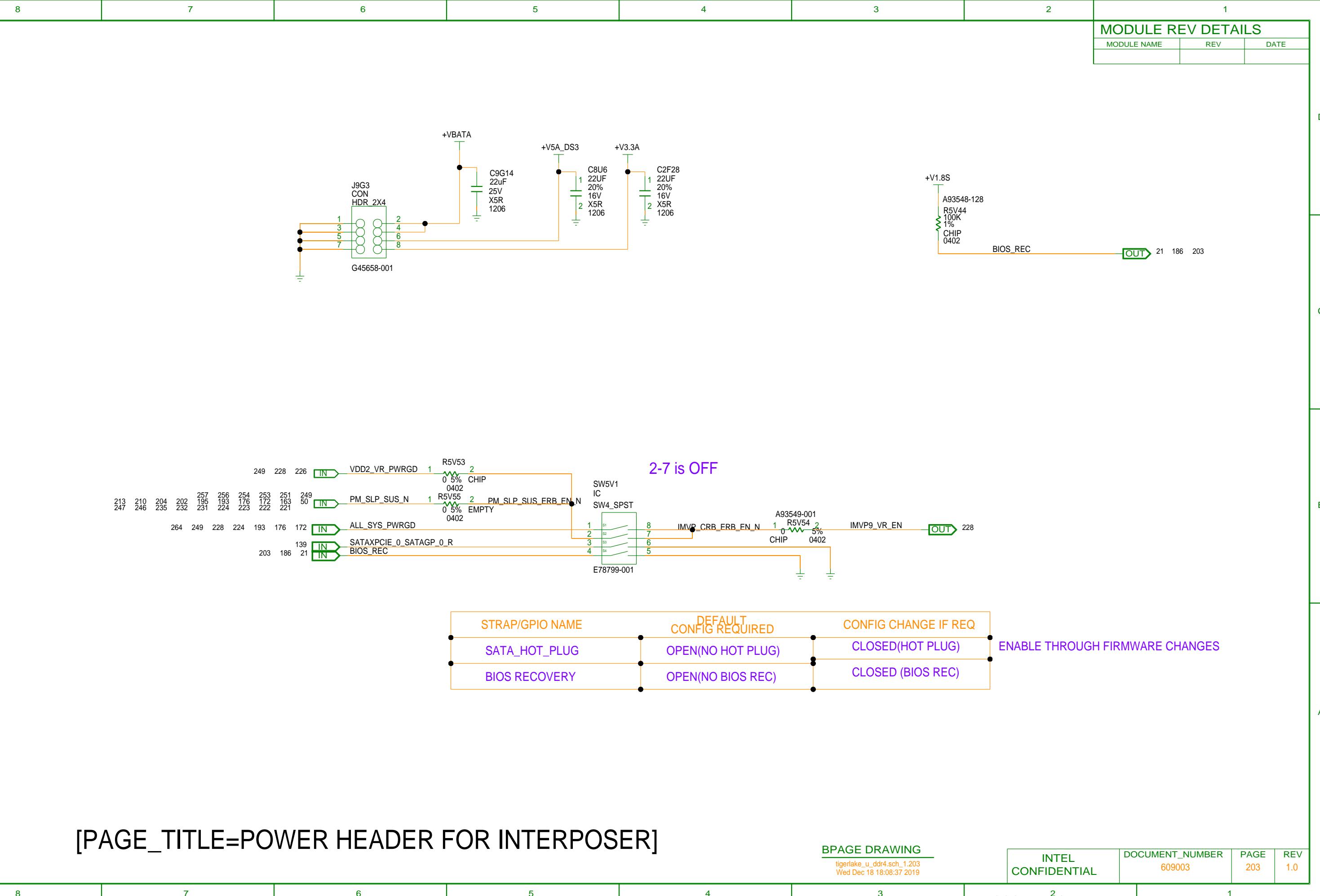
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Wed Dec 18 18:08:36 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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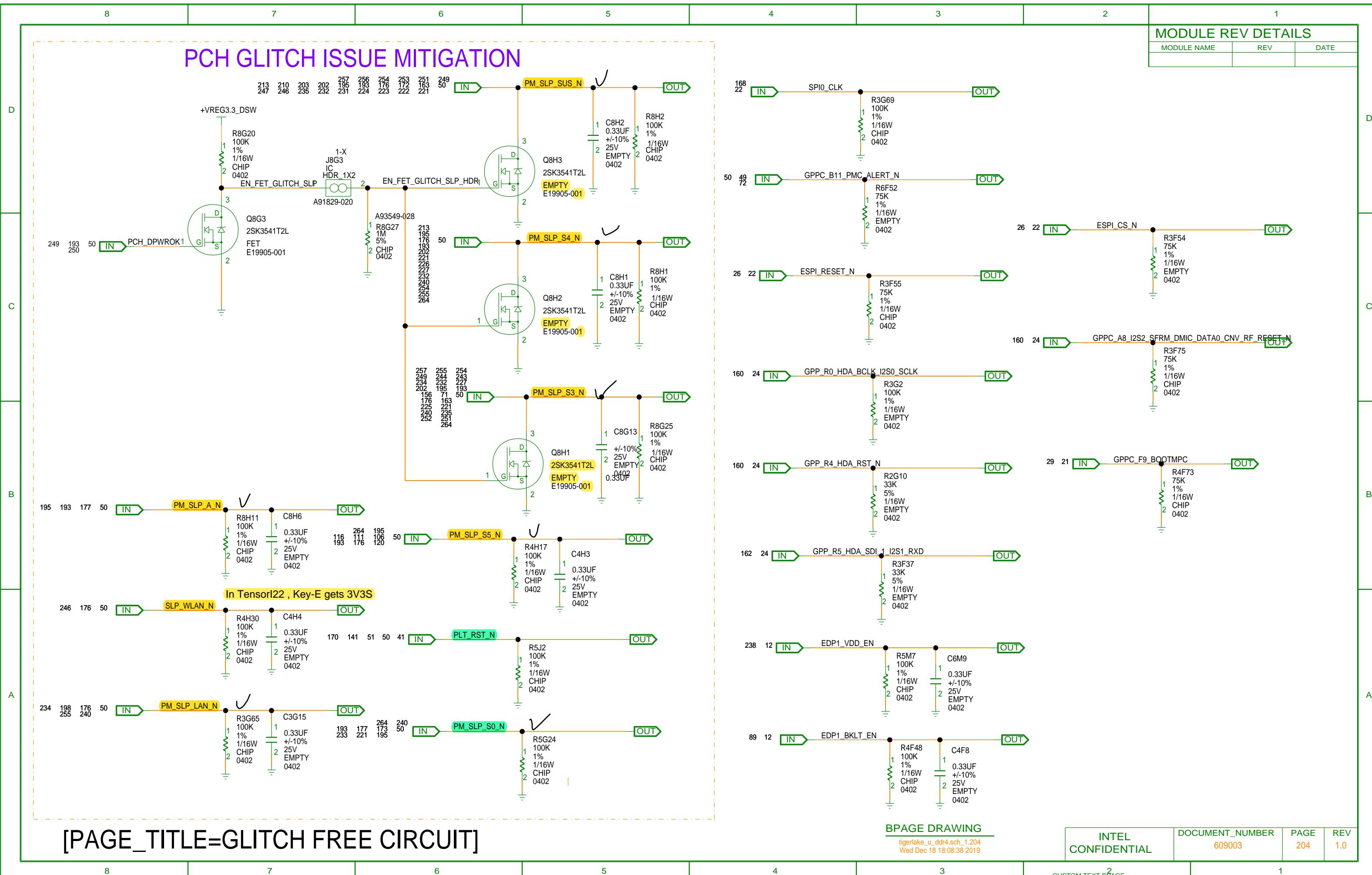
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CUSTOM TEXT B PAGE

1



PCH GLITCH ISSUE MITIGATION



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*tigerlake_u_ddr4.sch_1.204
Wed Dec 18 18:08:38 2019*

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 204	REV 1.0
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D

D

C

C

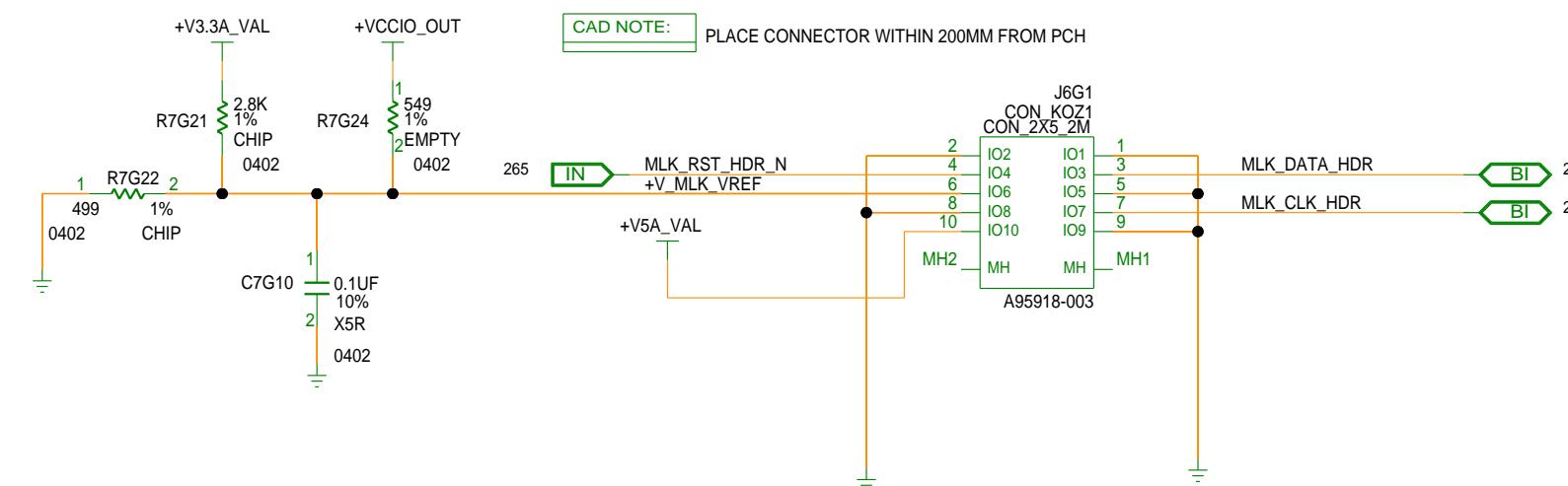
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B

A

A

MLINK HEADER



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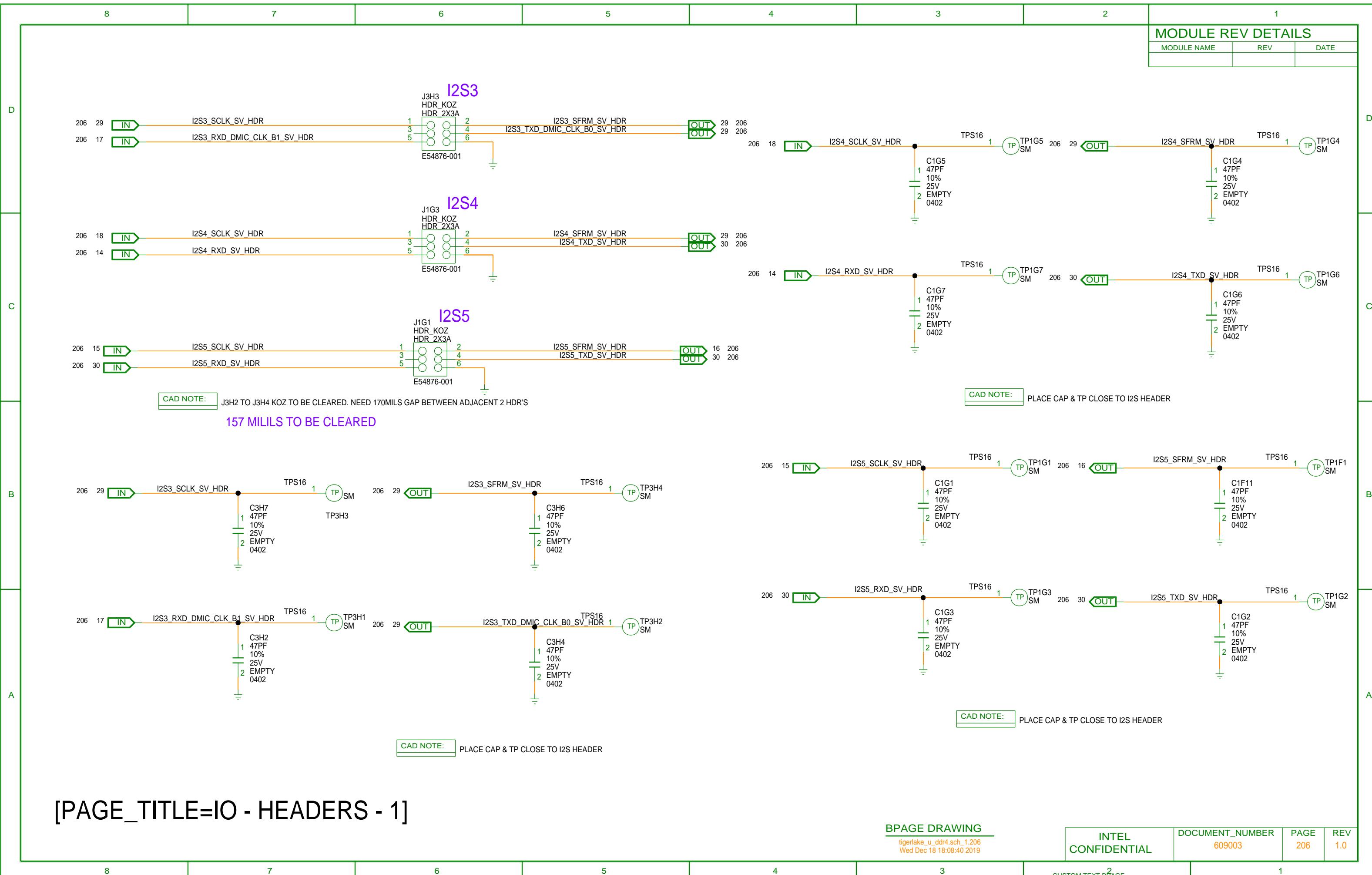
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Wed Dec 18 18:08:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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BPAGE							

MODULE REV DETAILS

MODULE NAME	REV	DATE



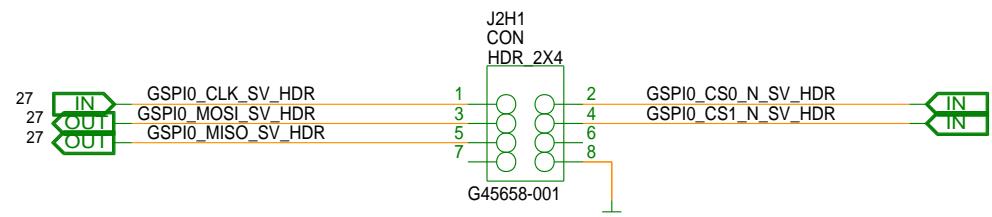
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MODULE REV DETAILS							

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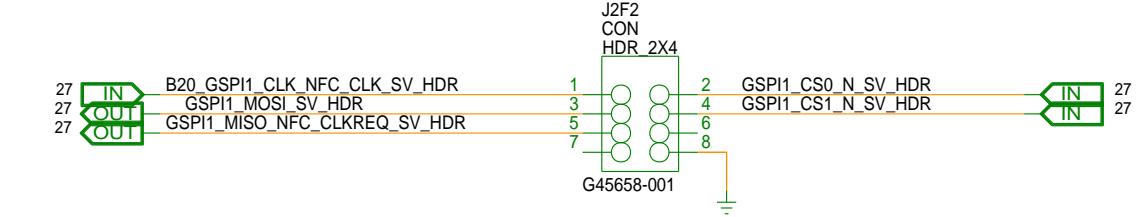
CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

GSPI0 HEADER



GSPI1 HEADER



GSPI2 IS AVAILABLE ON ISH SPI AND ISH UART HEADER
SPI1 IS AVAILABLE ON THC SV HEADER

8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

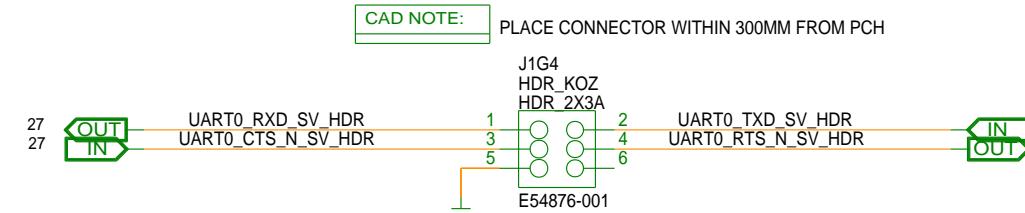
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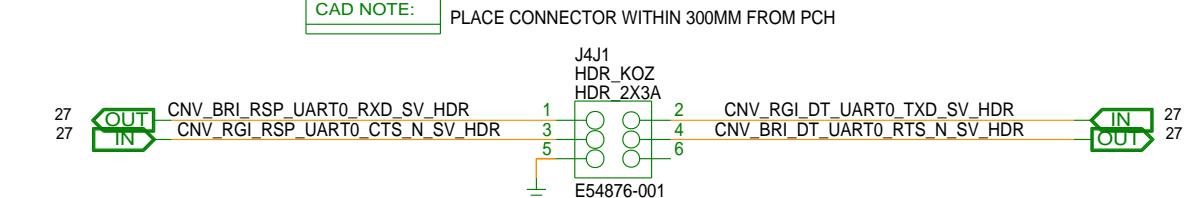
CAD NOTE:

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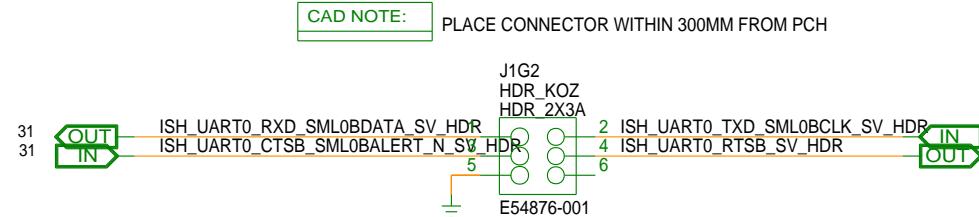
LPSS UART0 HEADER



CNV UART0 HEADER

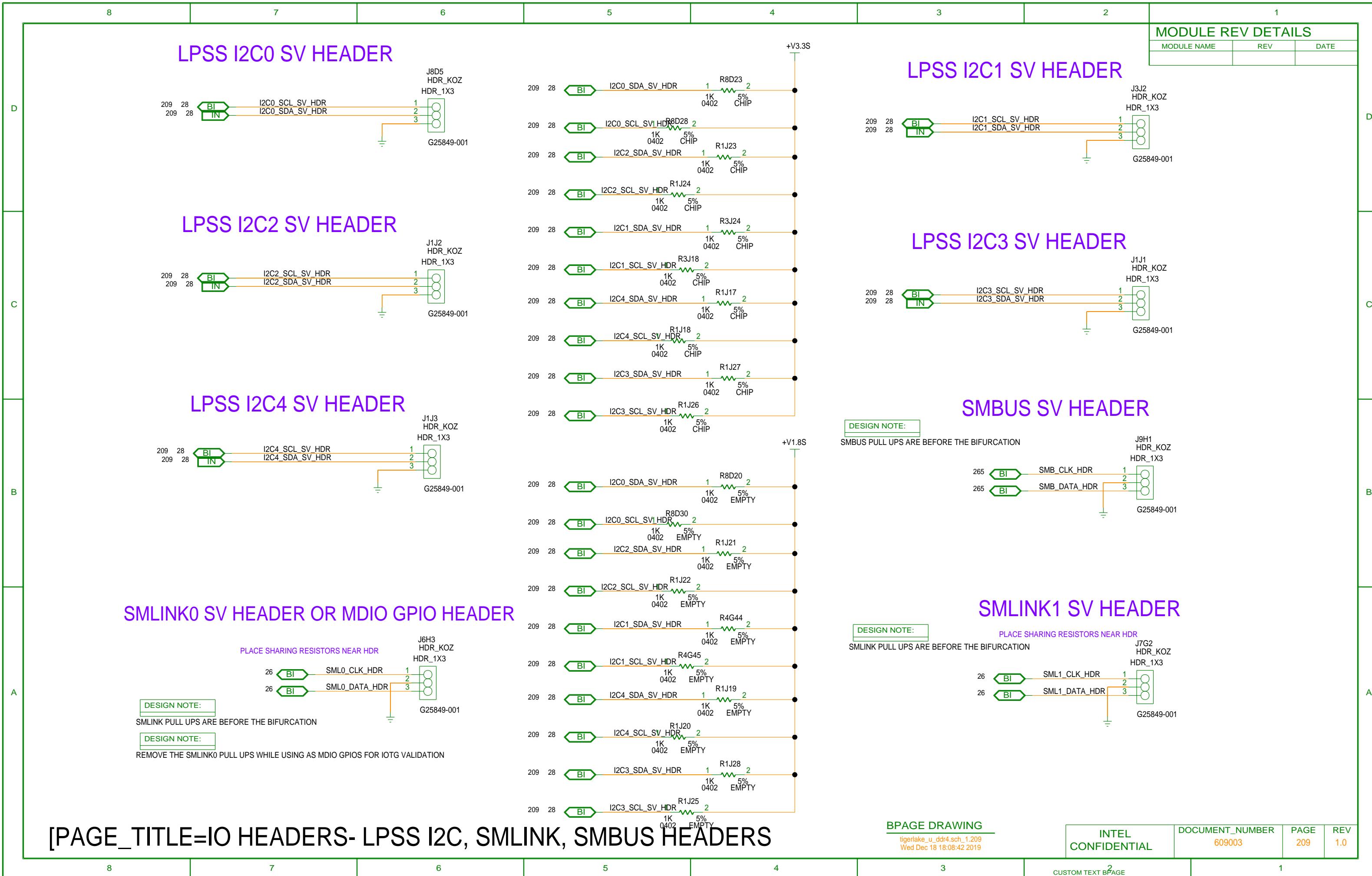


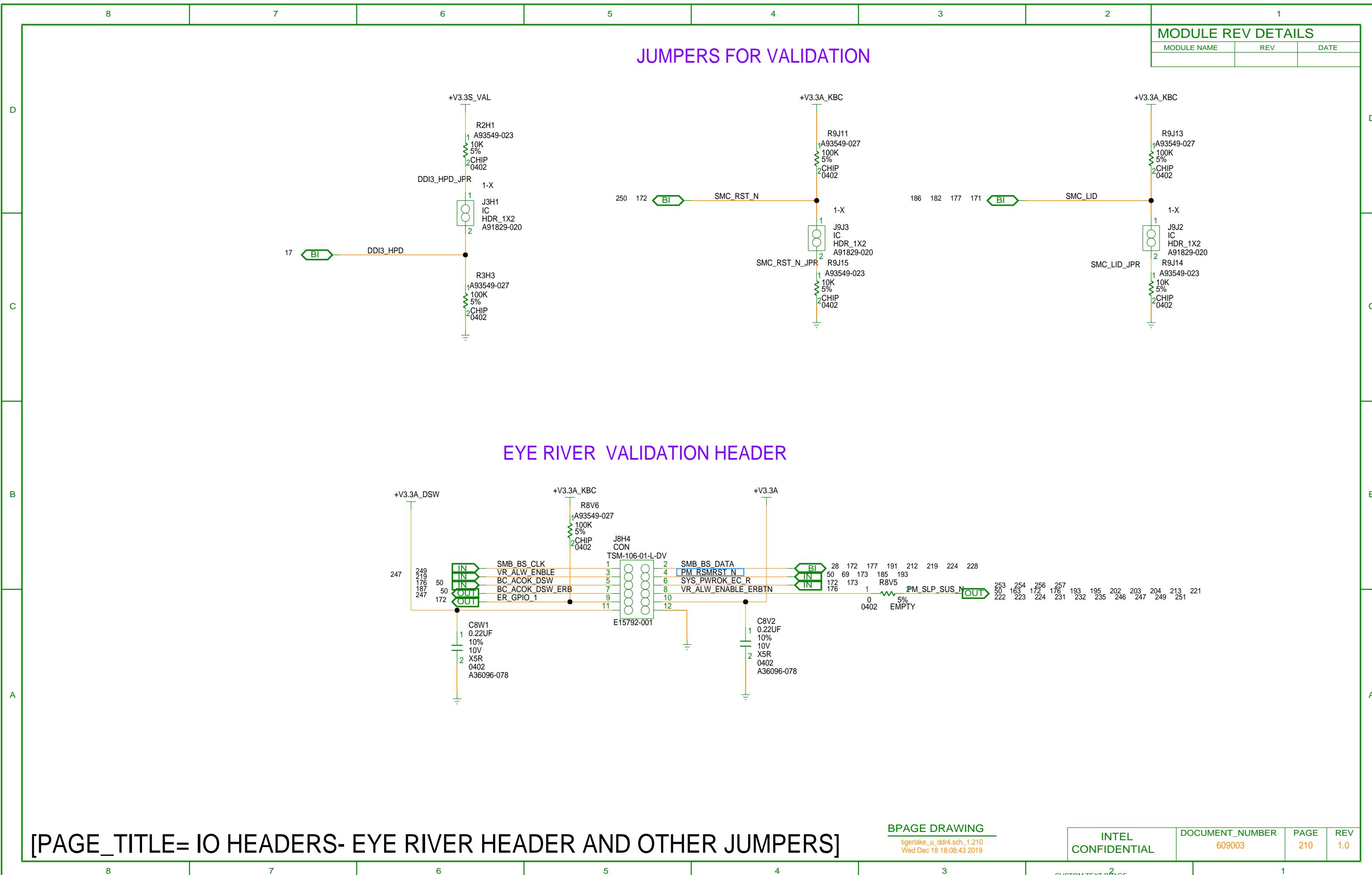
ISH UART0 / SMLINK0B HEADER



A

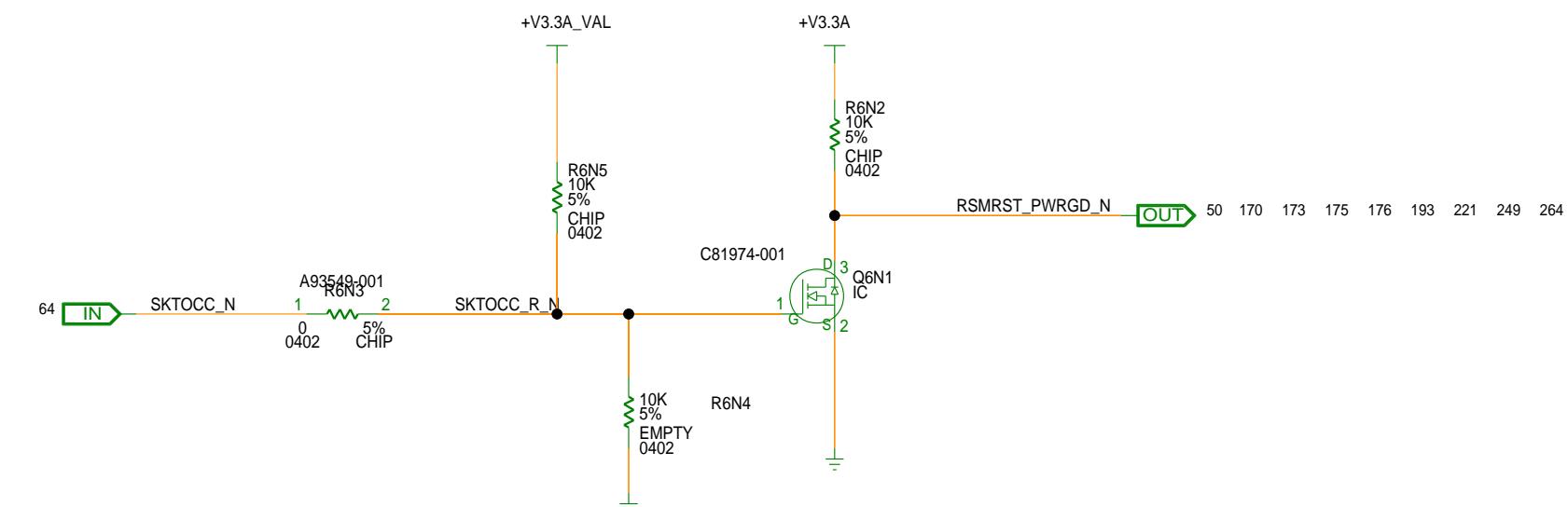
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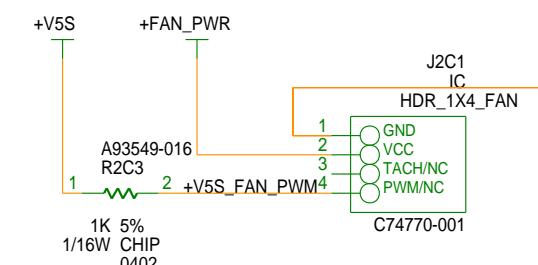
8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

SKTOCC_N -> H_PRESENT_N (CPU DETECT,SKTOCC_N)



CONNECT TO A PROPER VSS PIN OF PCH
PROCESSOR & PCH PART DETECT

FAN HEADER



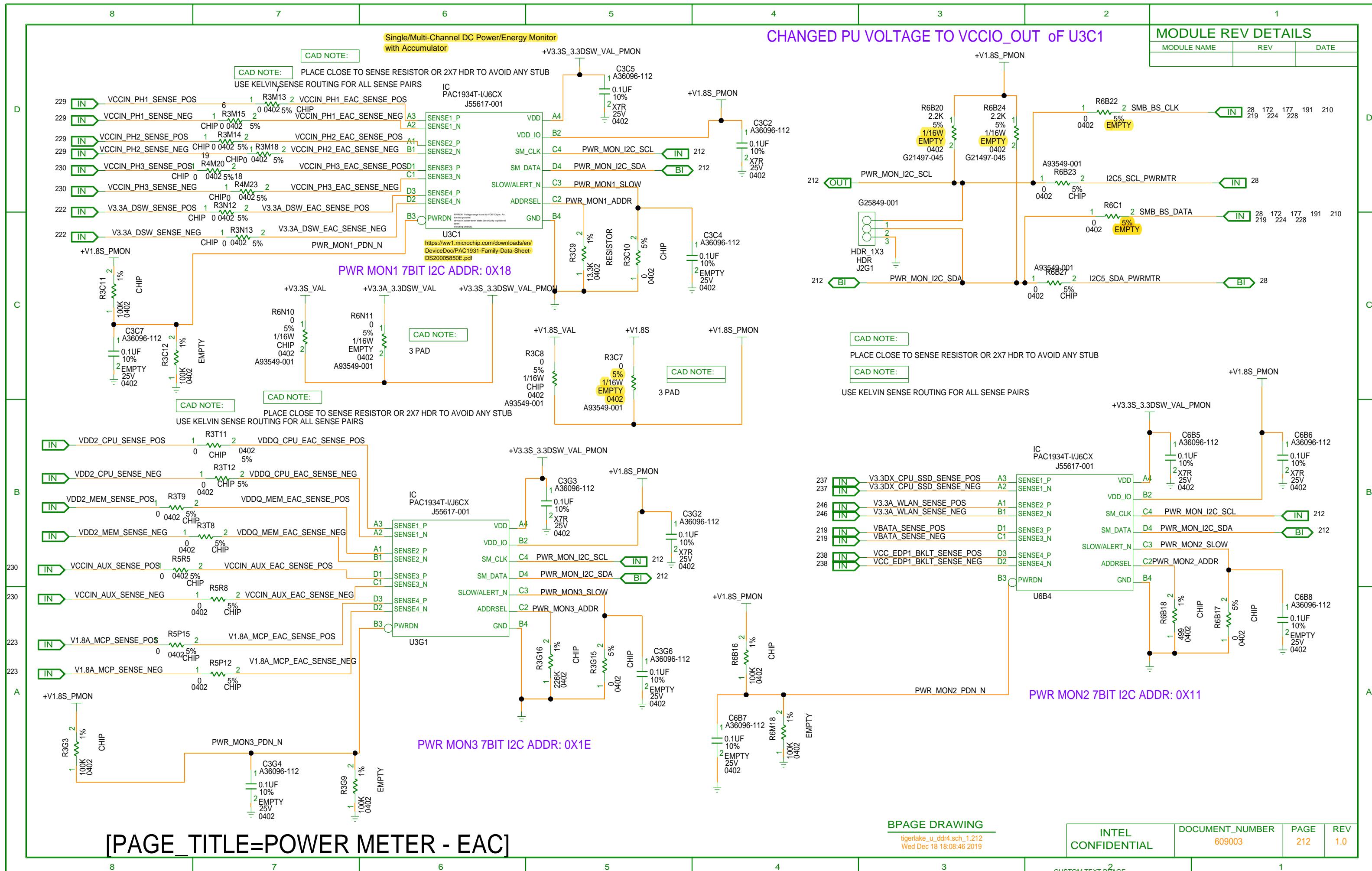
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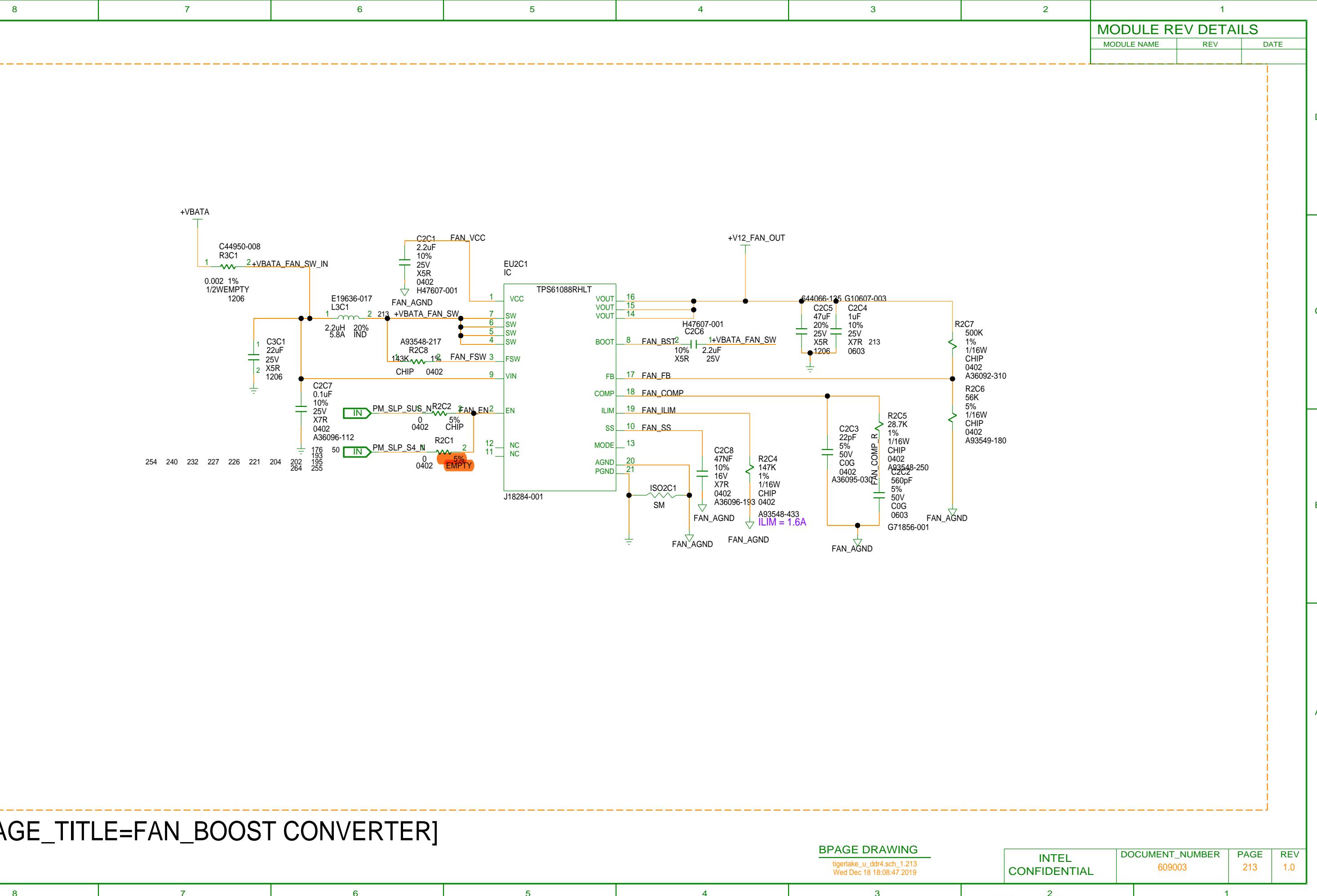
J2A4 FAN CONNECTOR ON & STANDBY(S3)

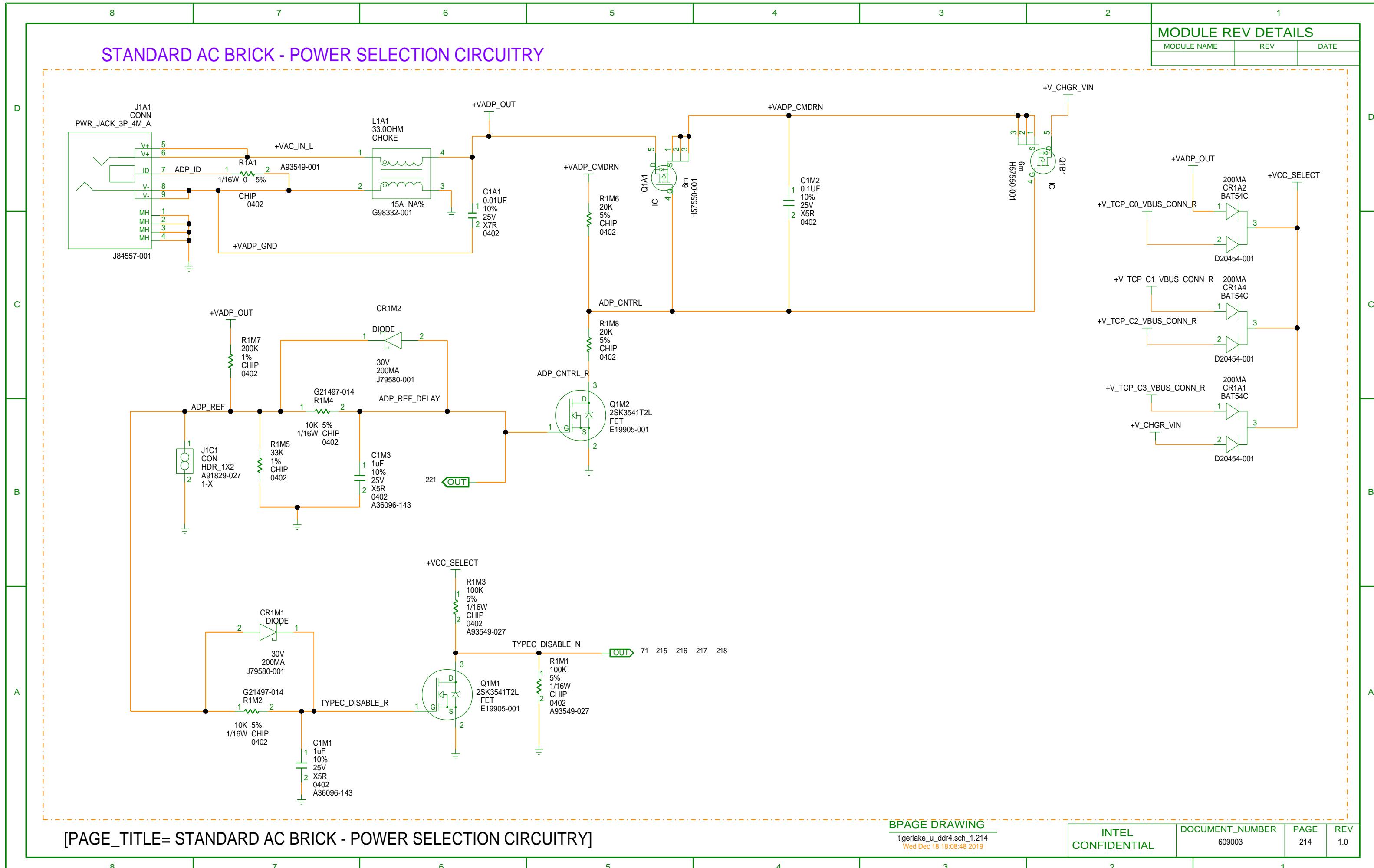
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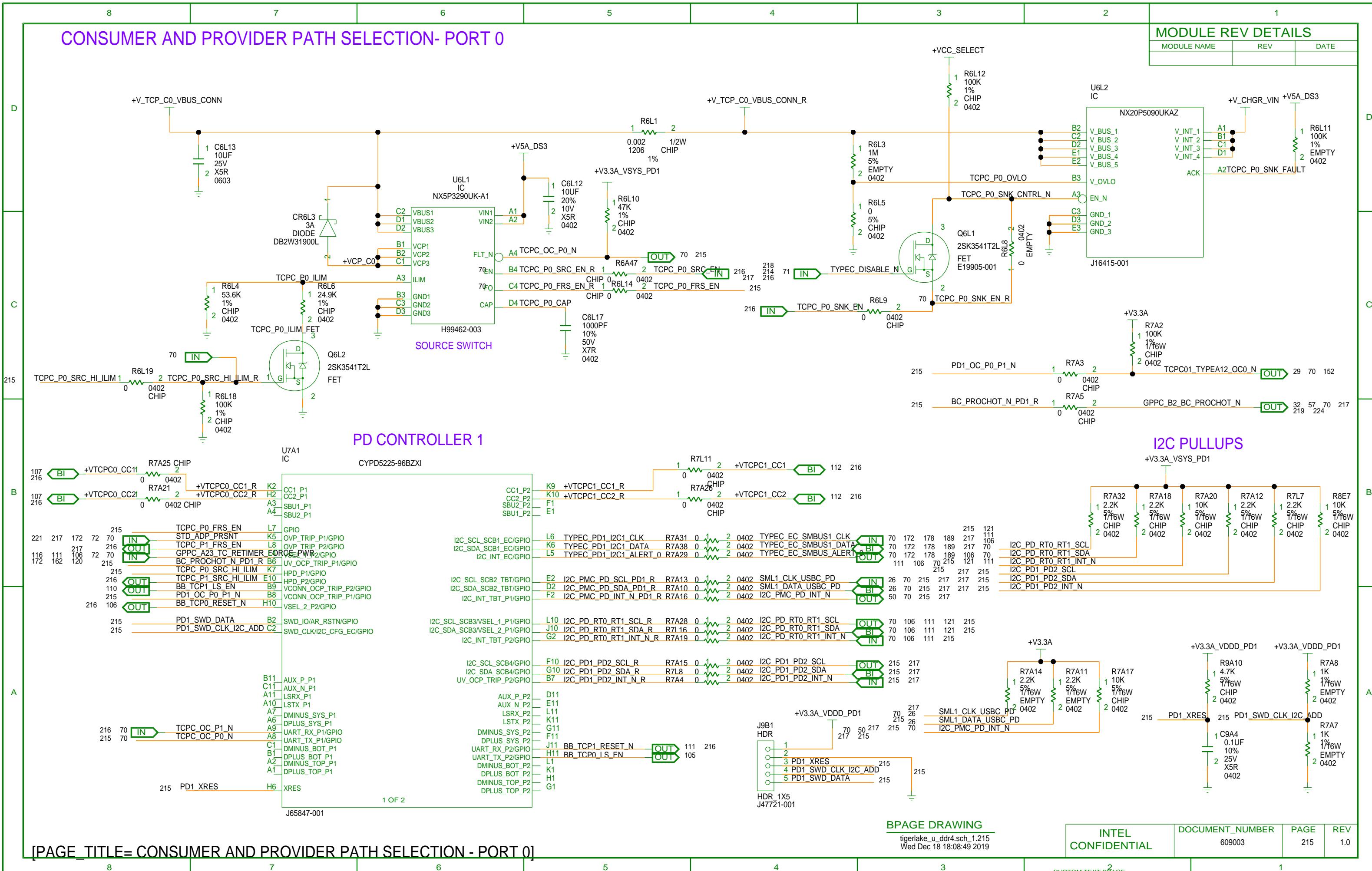
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Wed Dec 18 18:08:45 2019

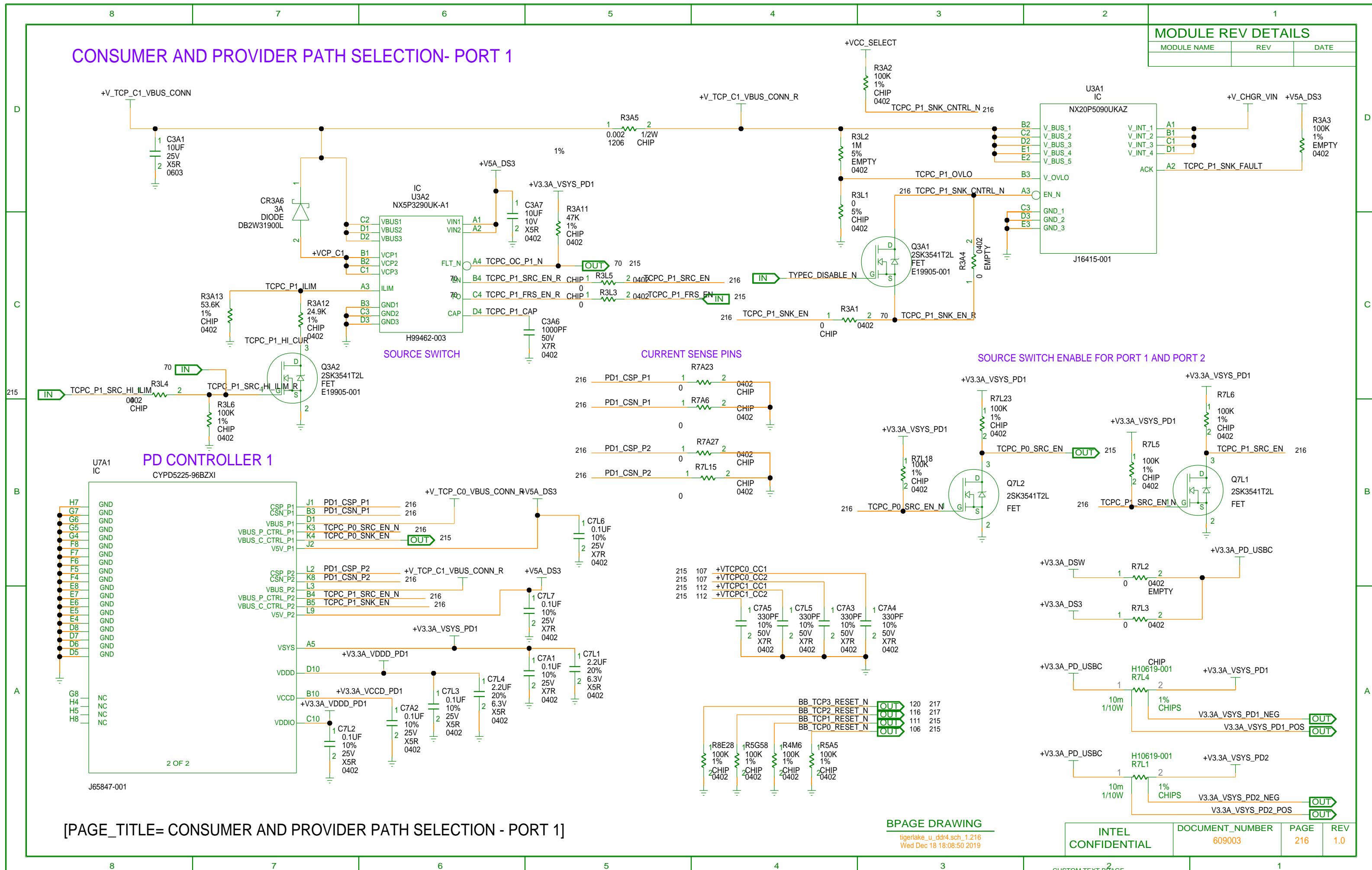
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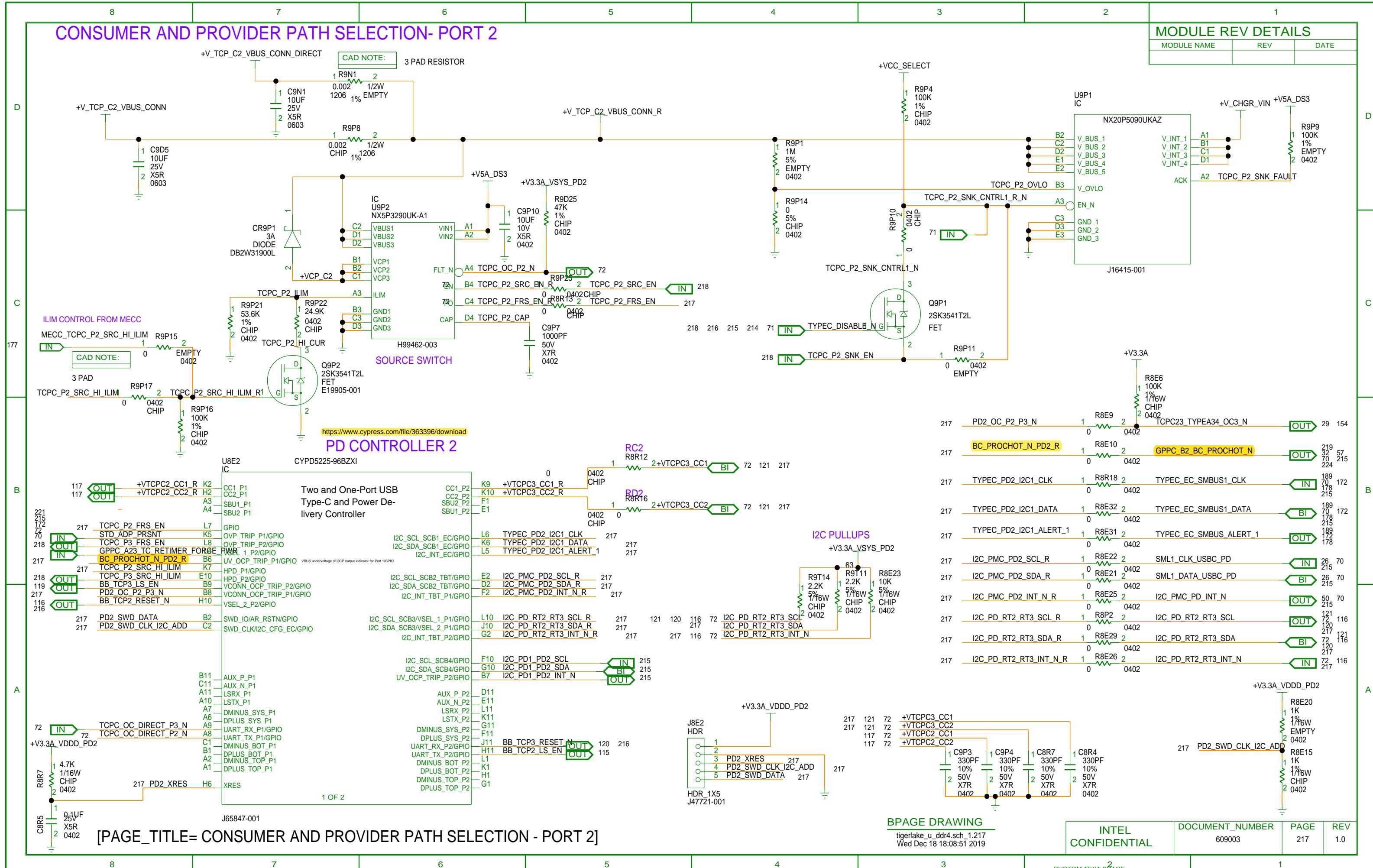


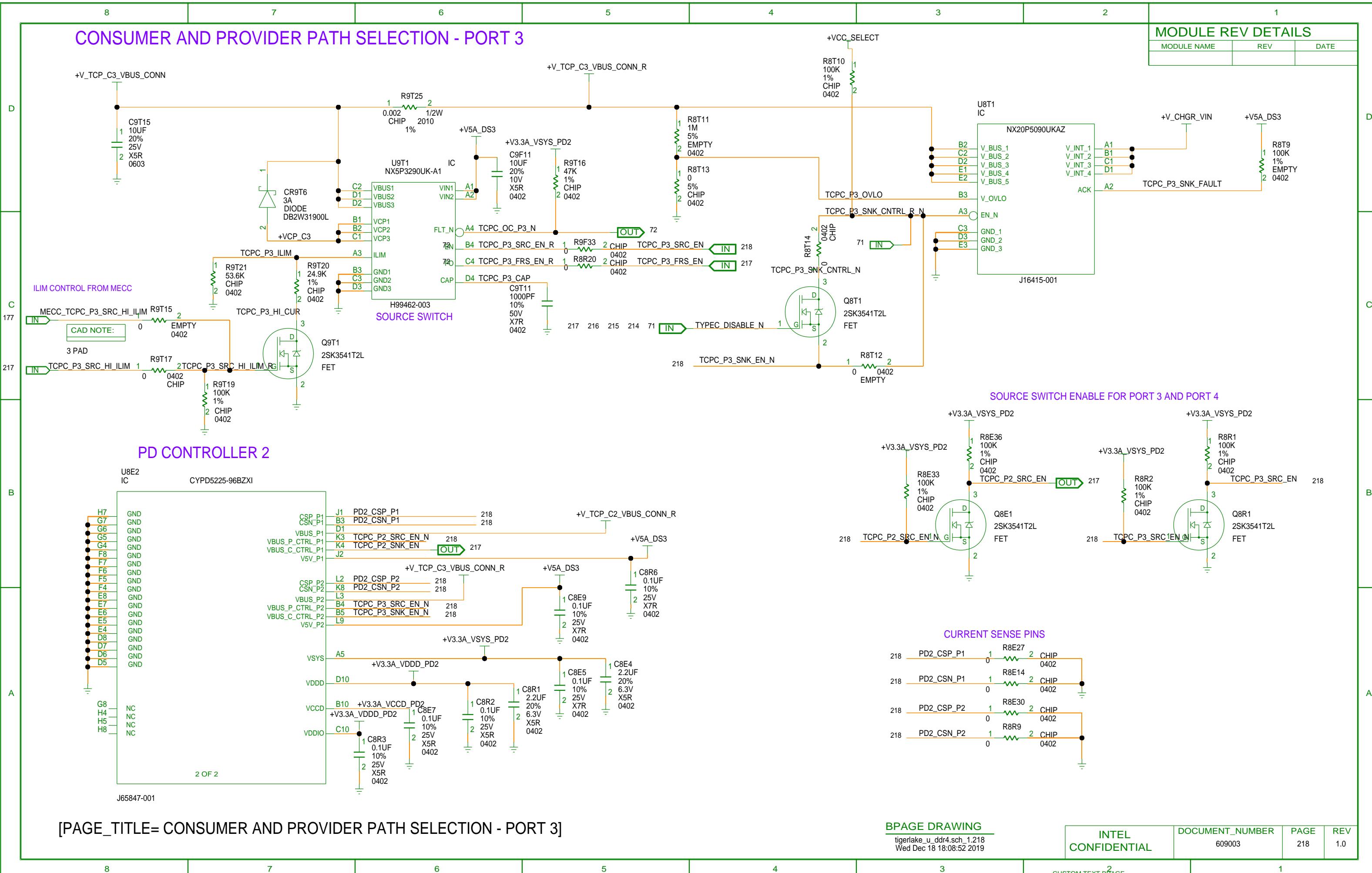


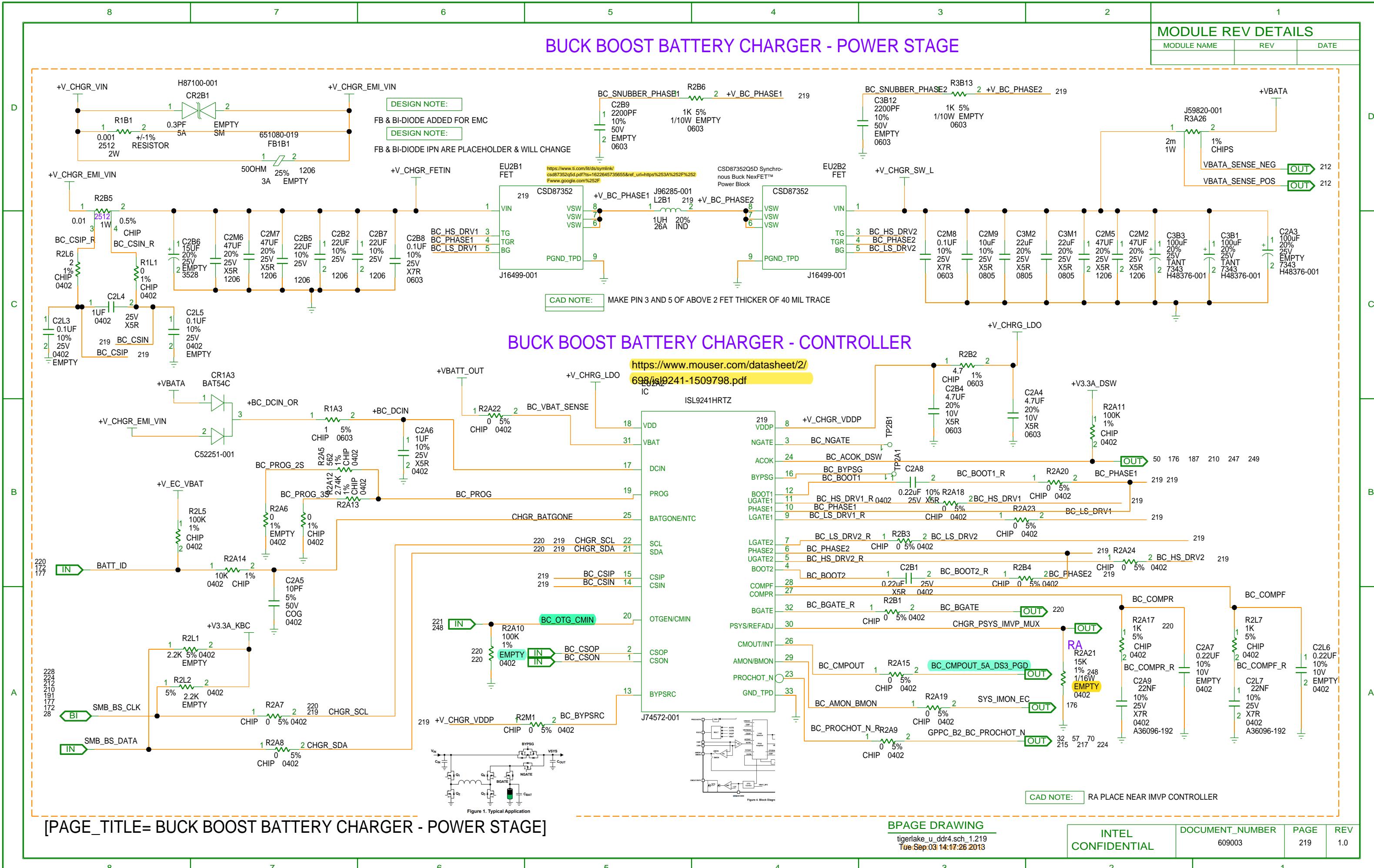


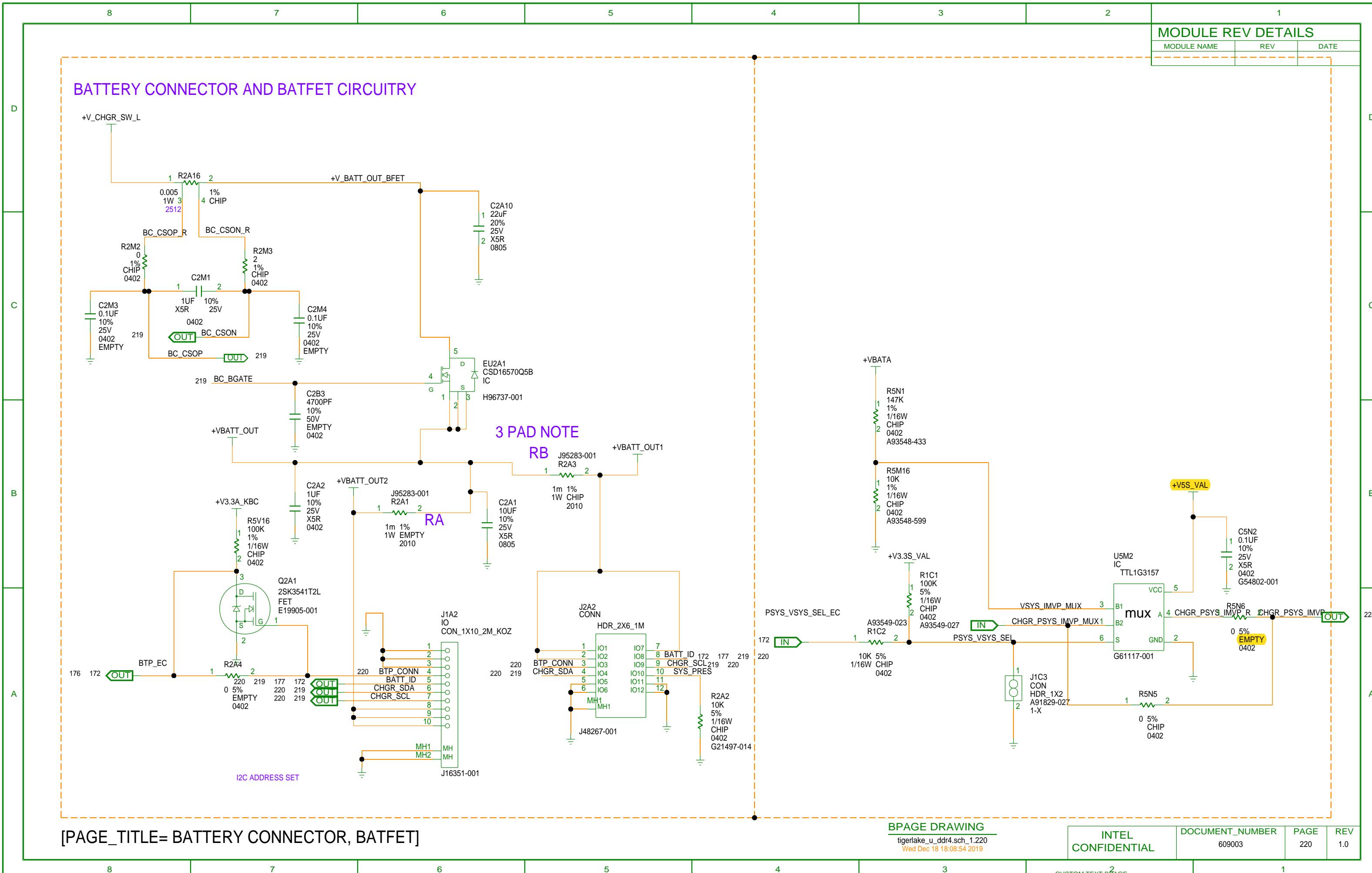


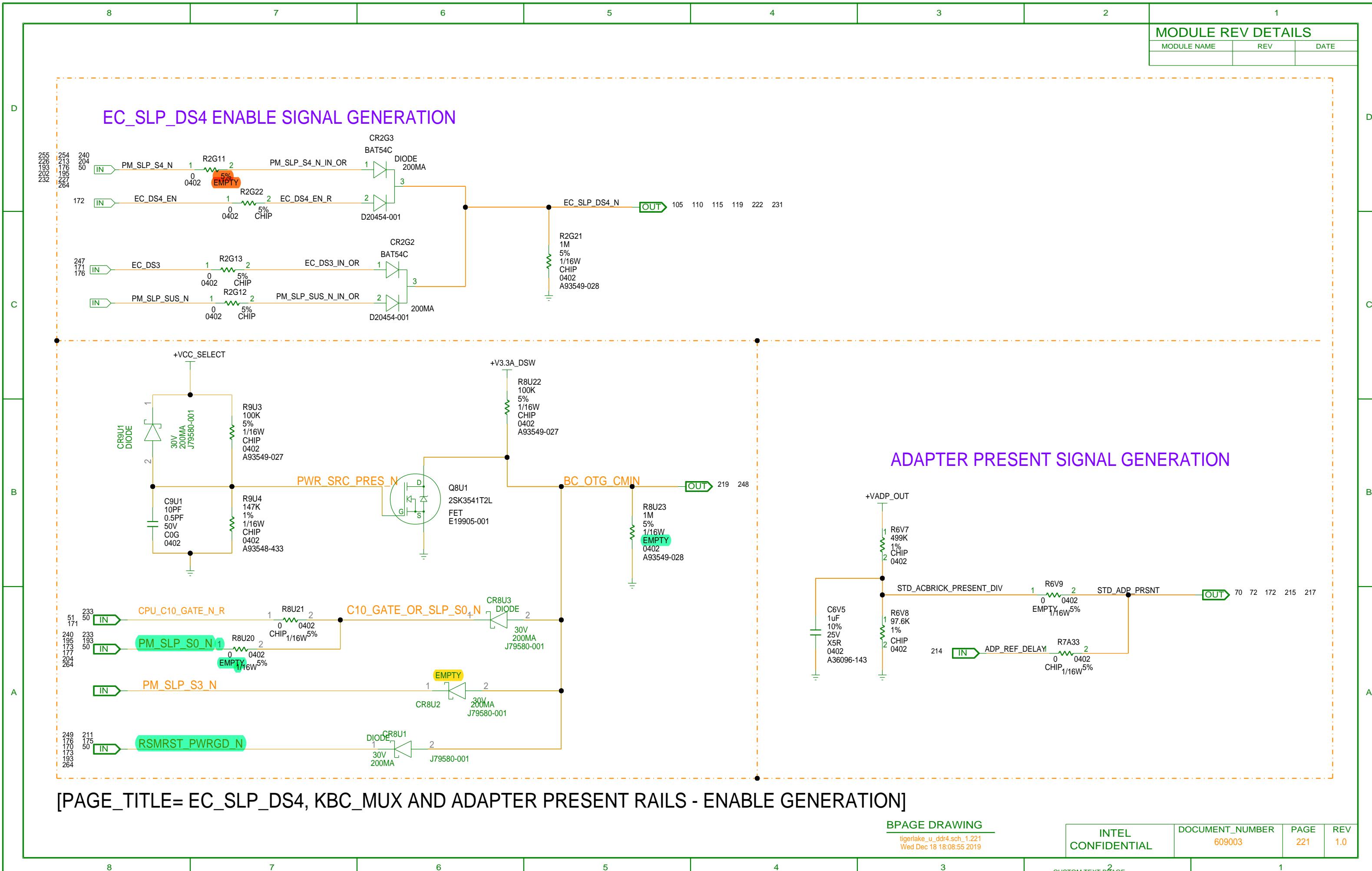


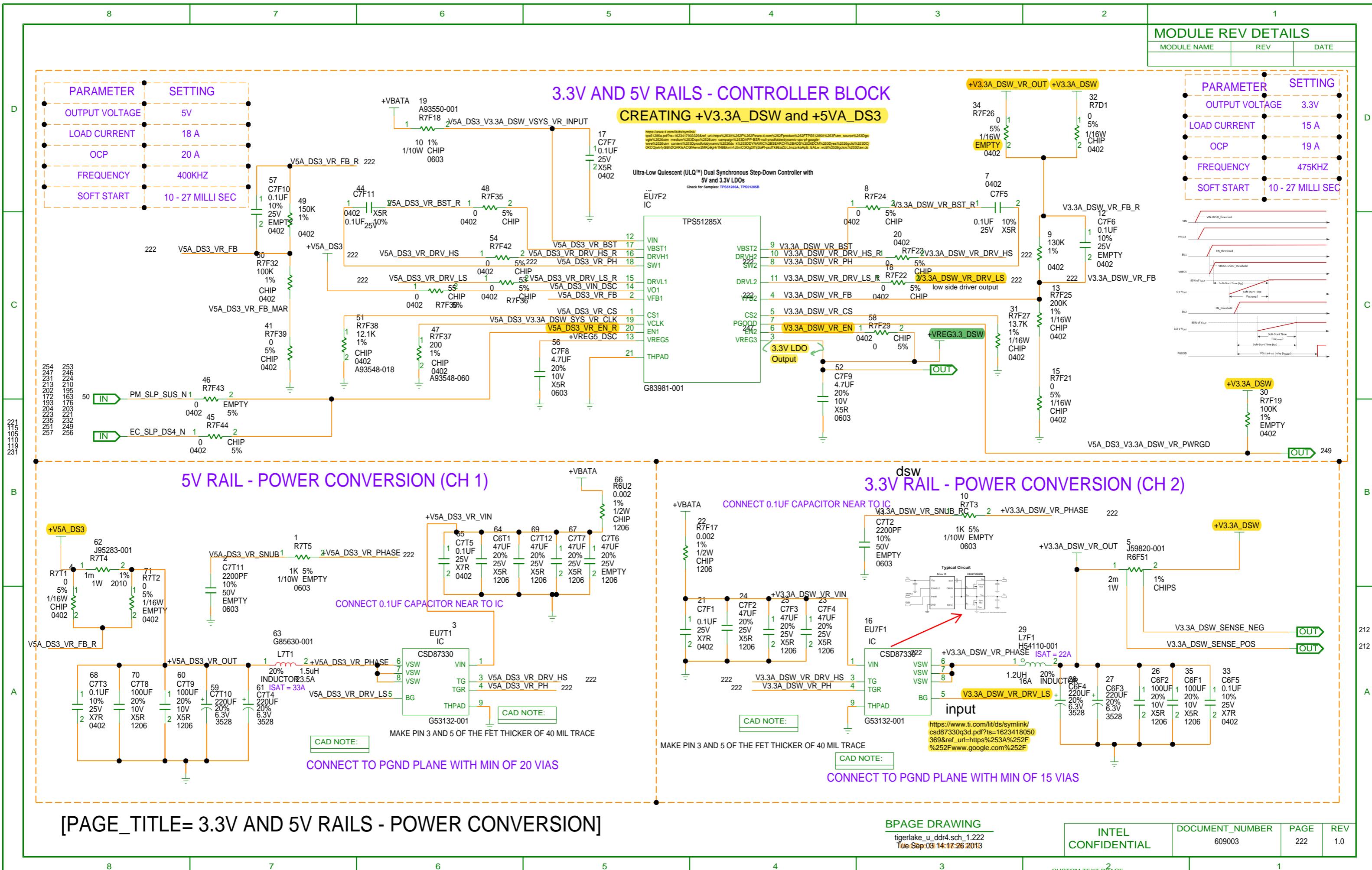


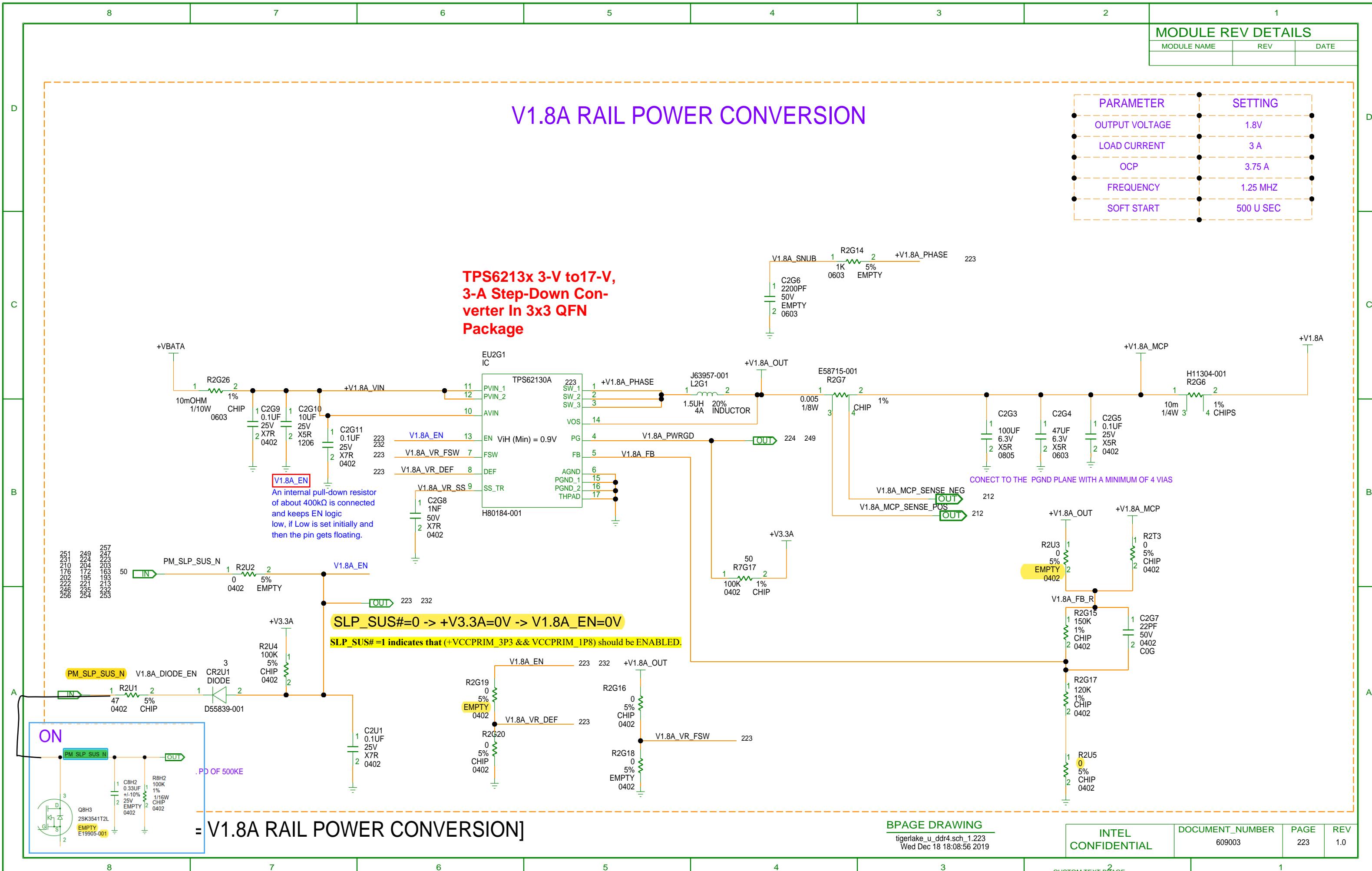


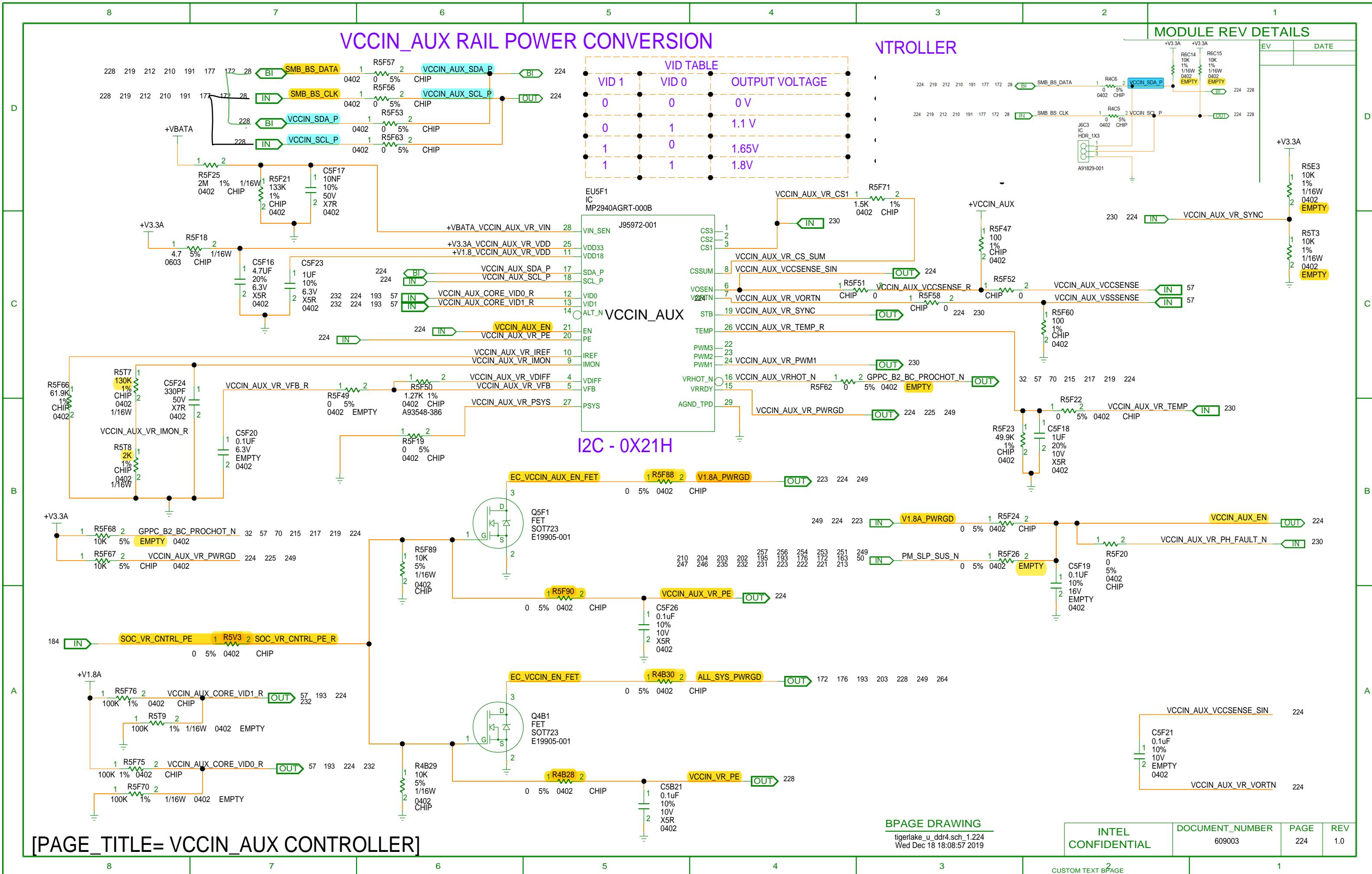


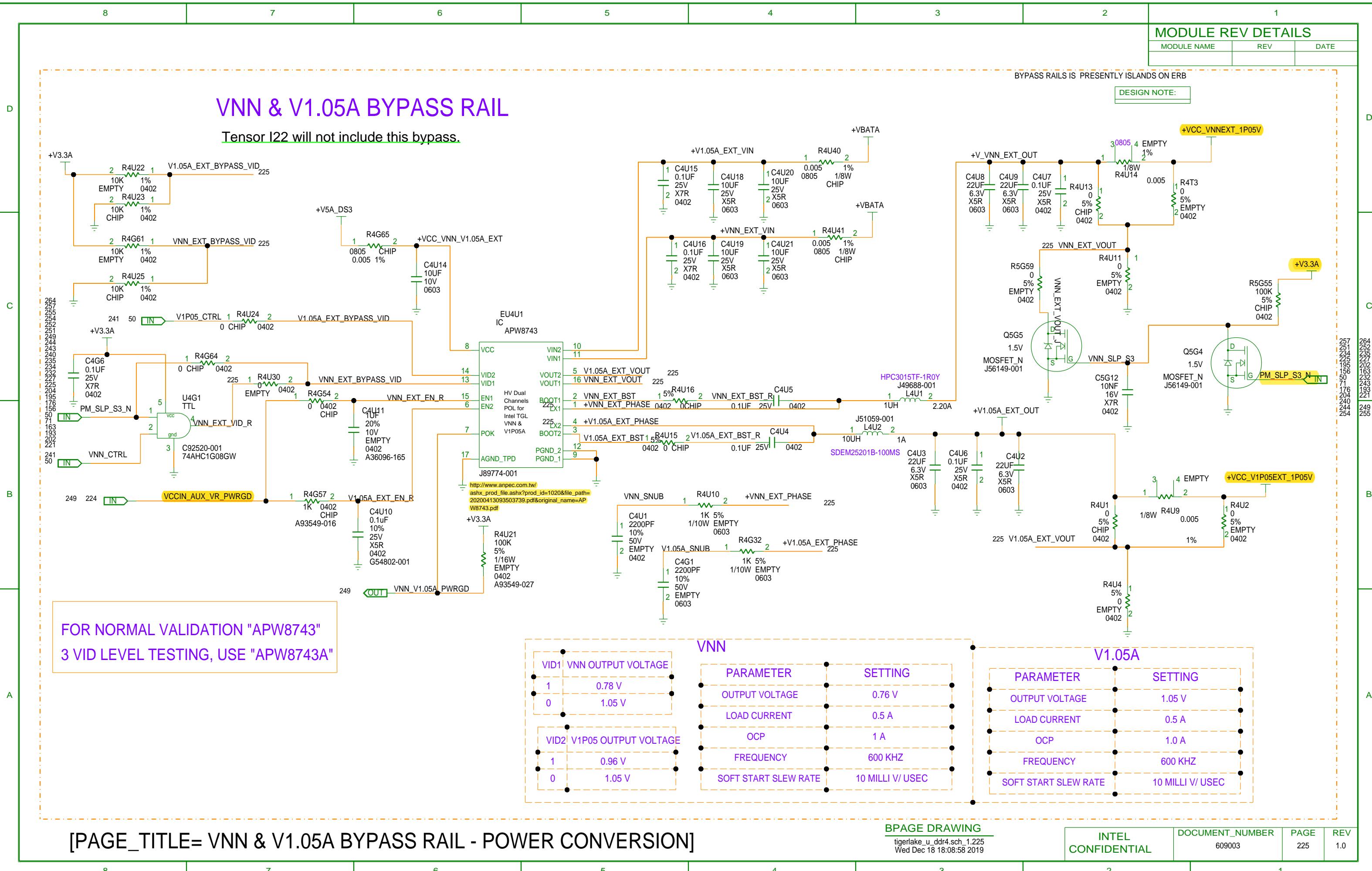


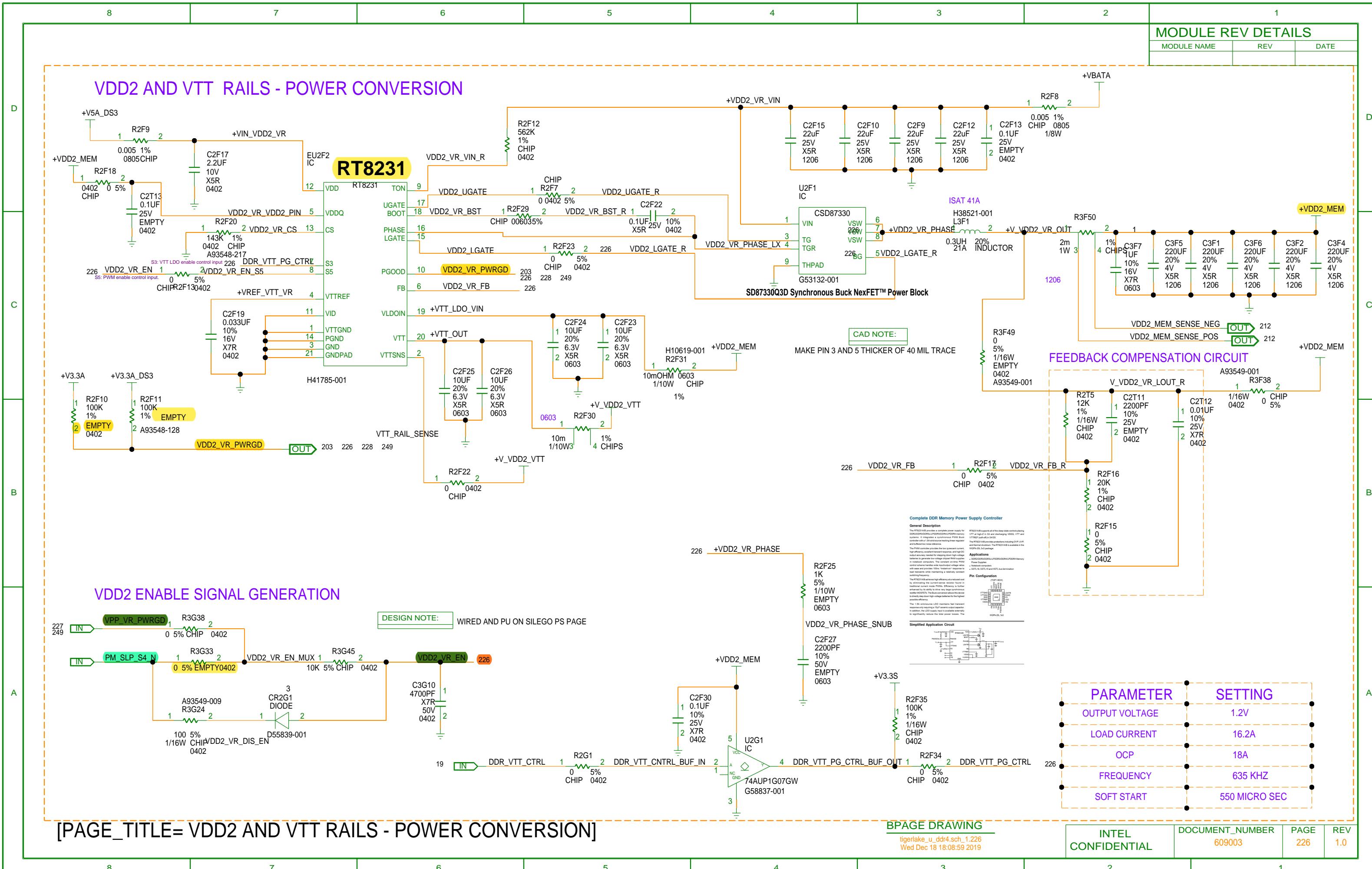


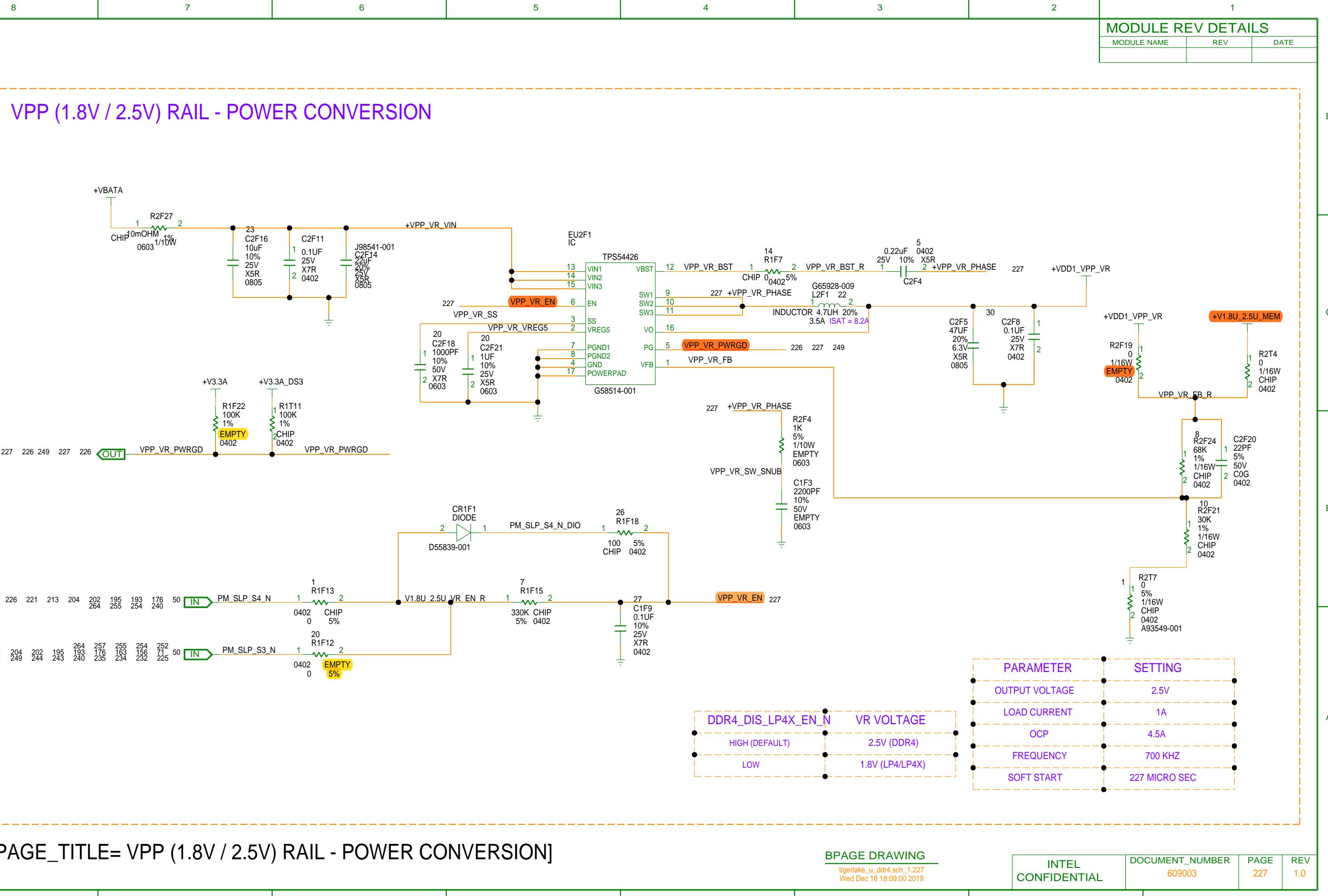


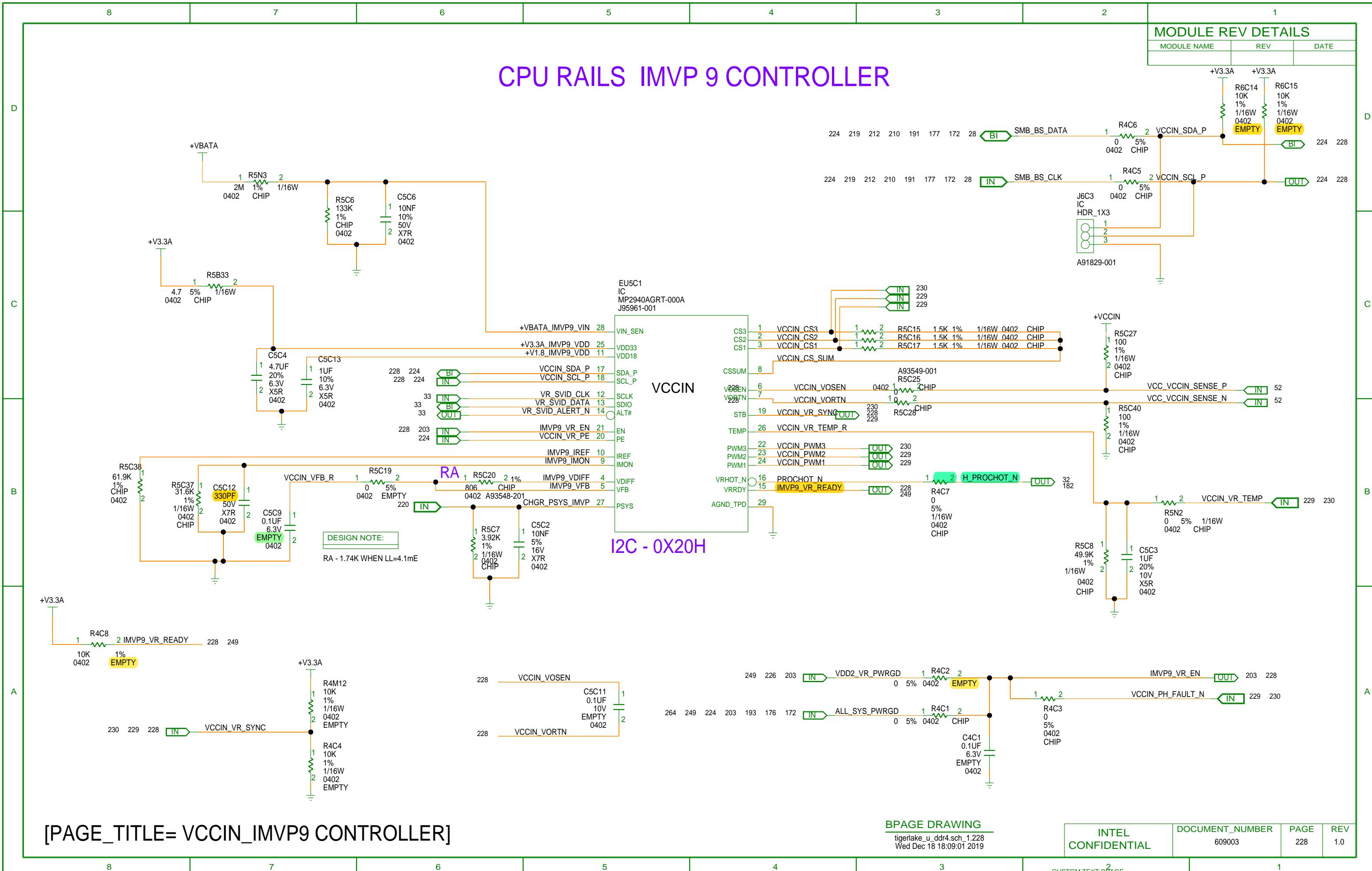


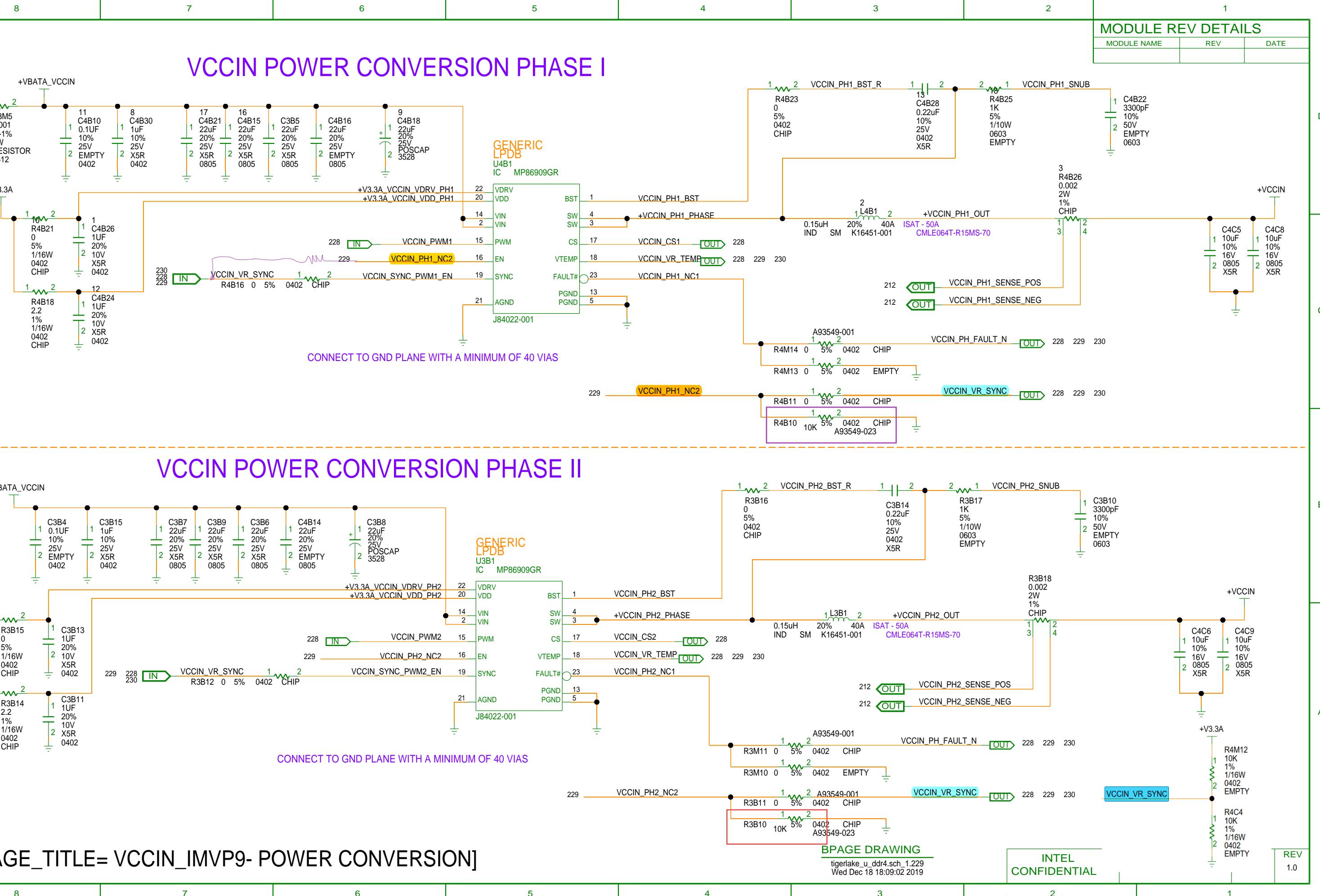








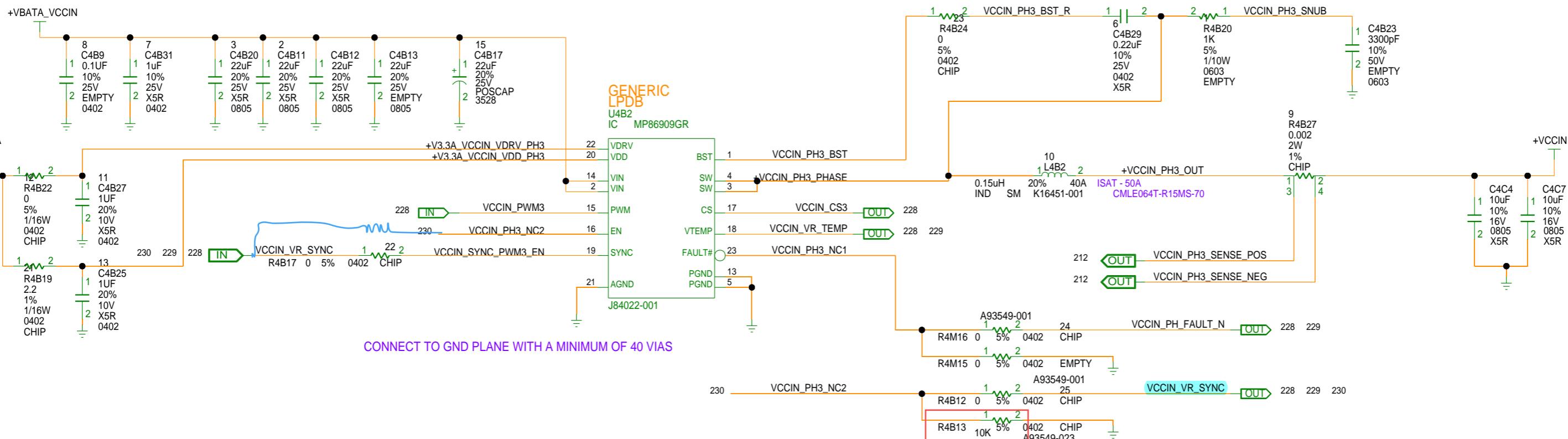




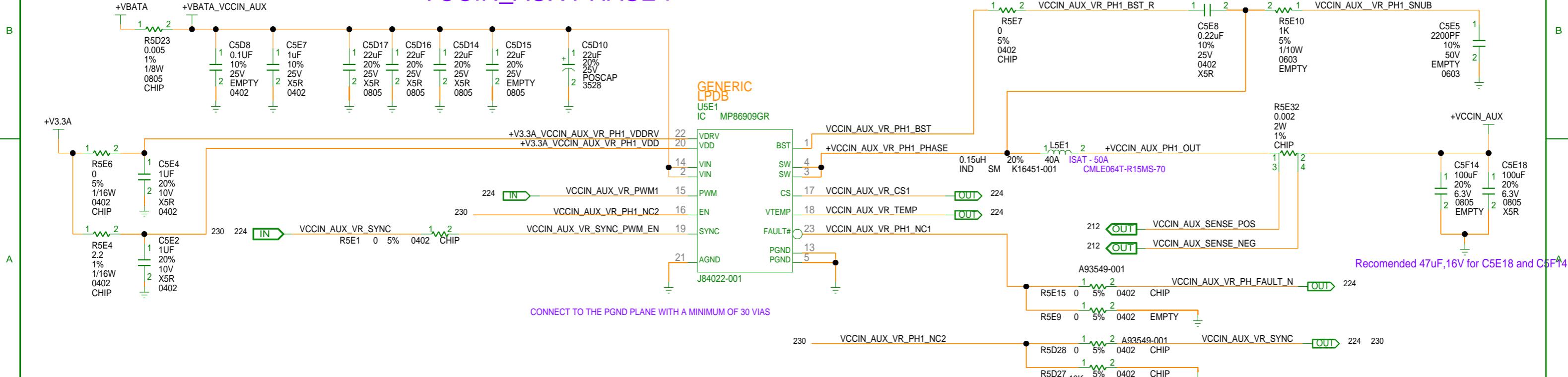
VCCIN POWER CONVERSION PHASE III

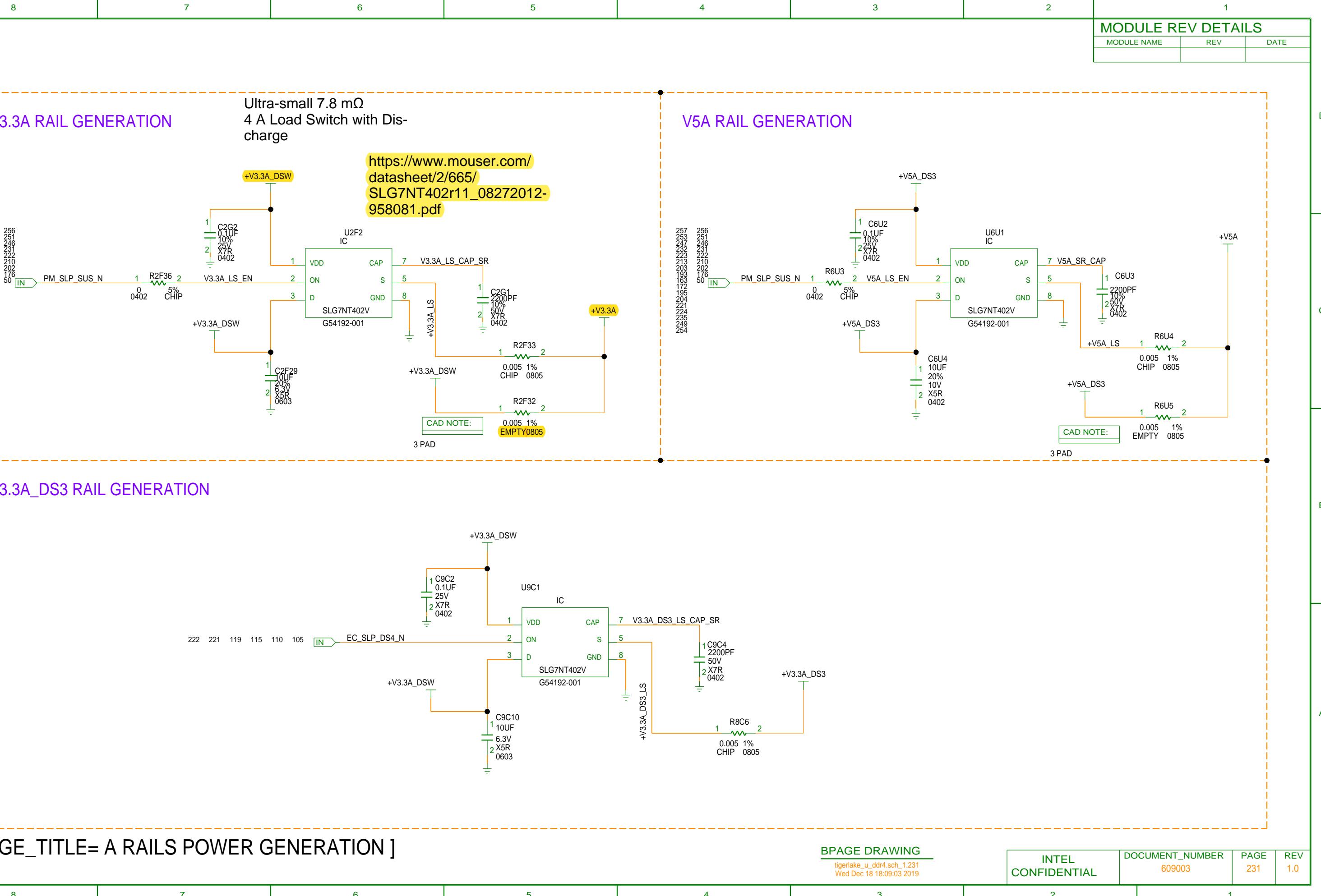
MODULE REV DETAILS

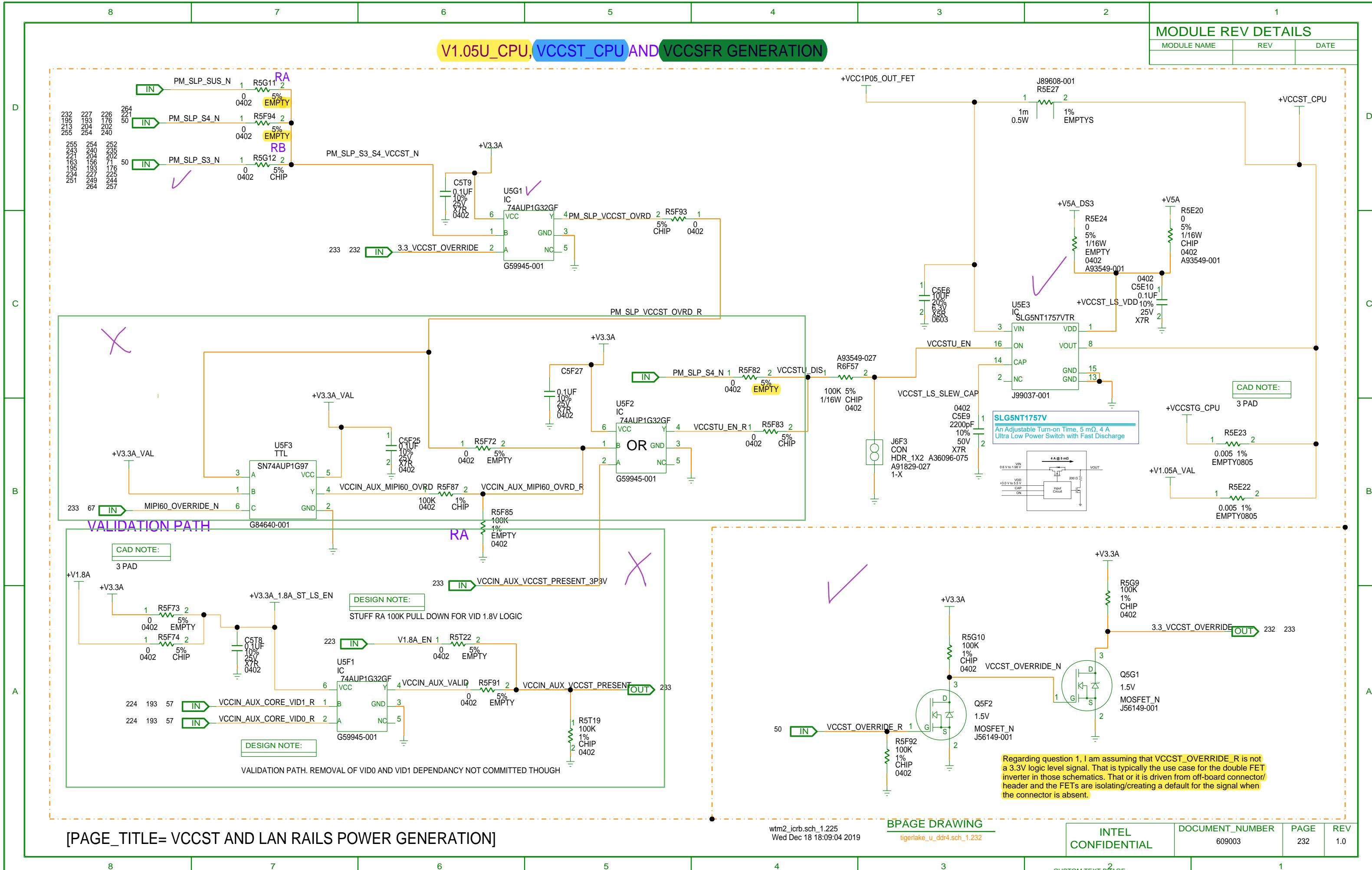
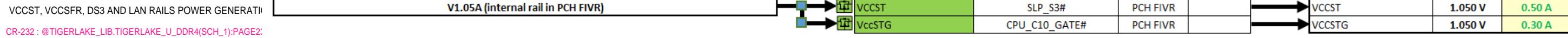
MODULE NAME	REV	DATE

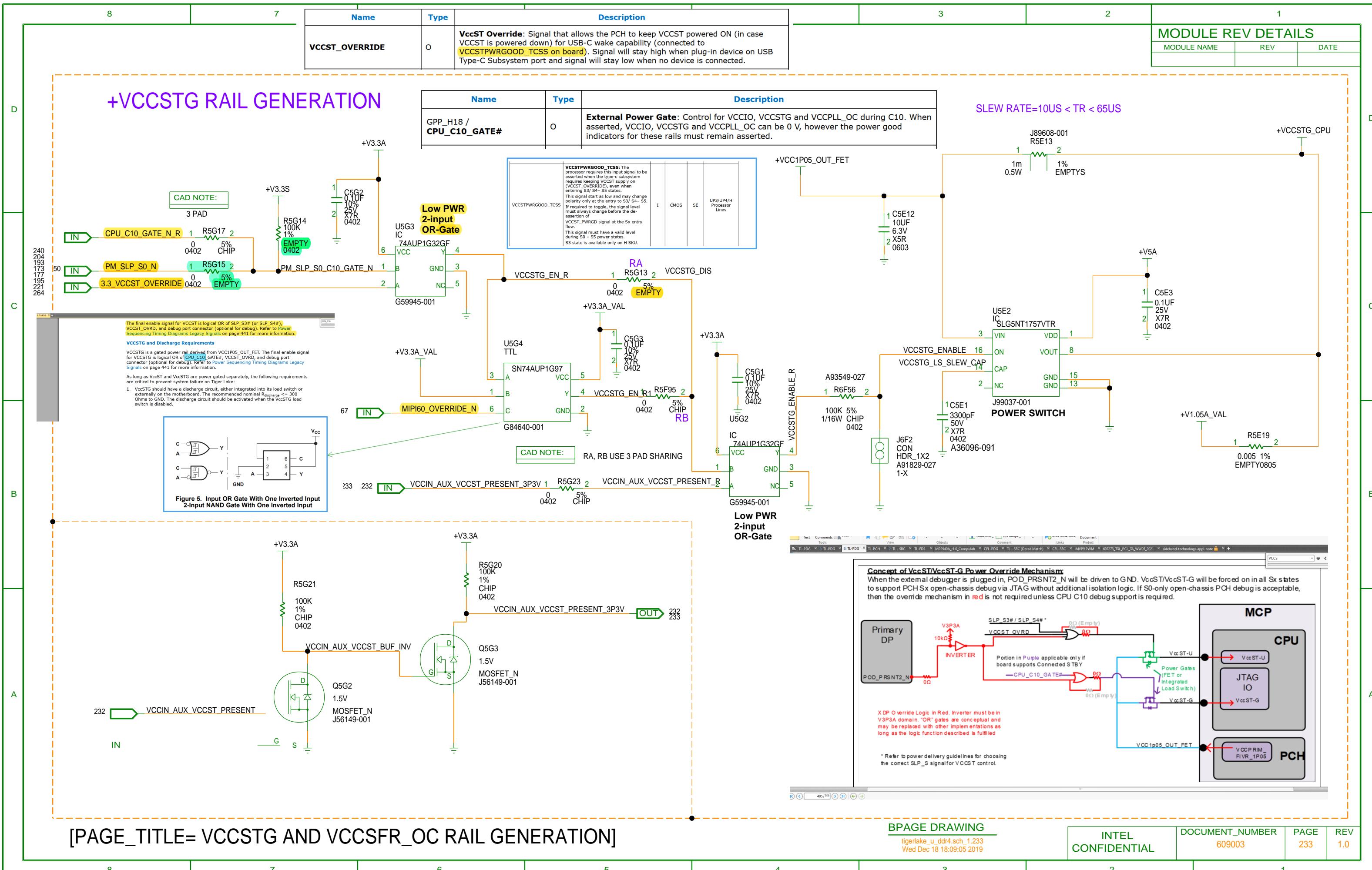


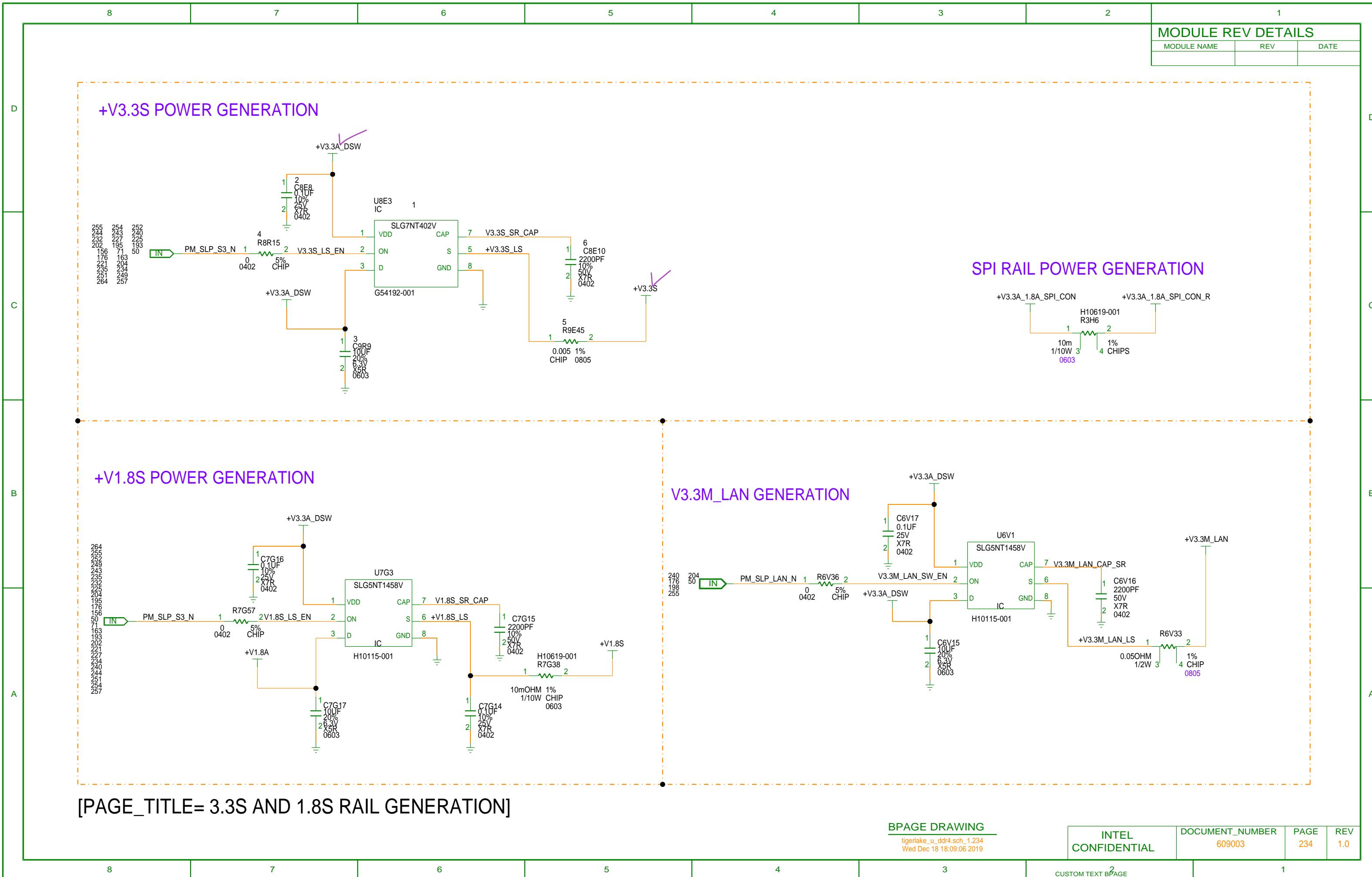
VCCIN_AUX PHASE I







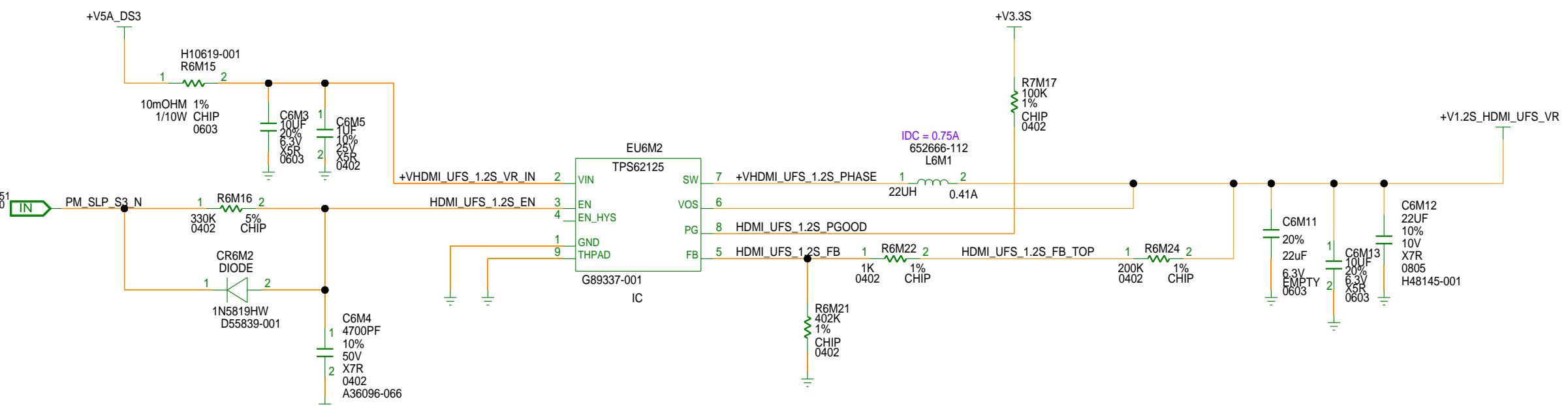




1.2V RAIL FOR HDMI AND UFS - POWER CONVERSION

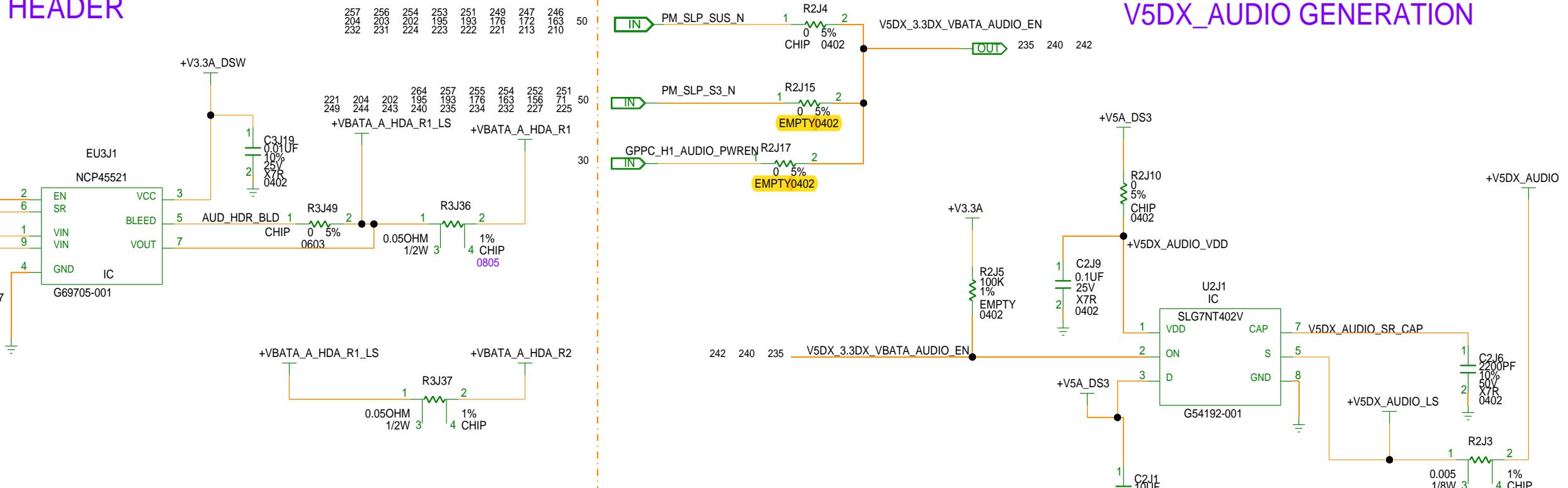
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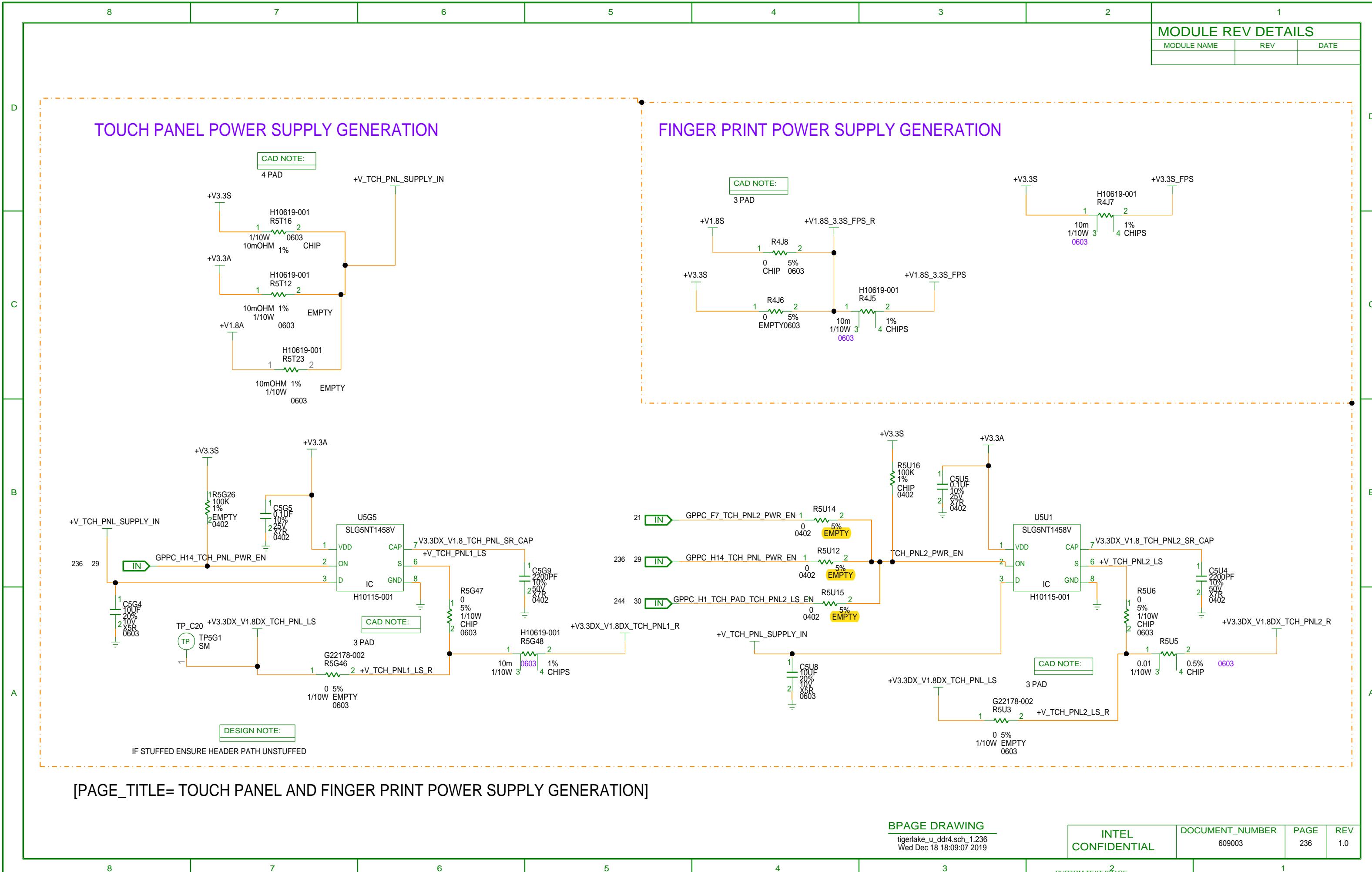
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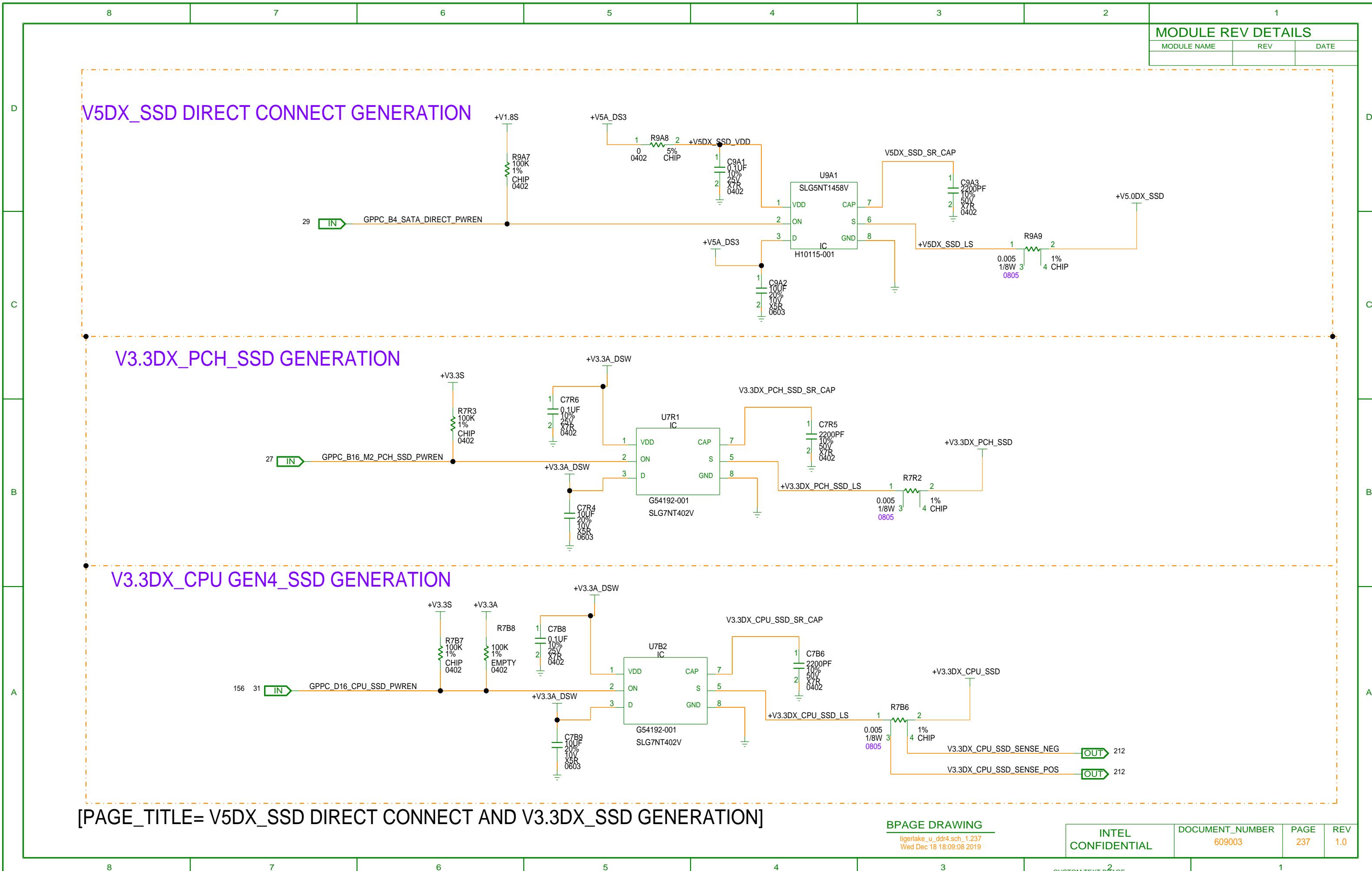


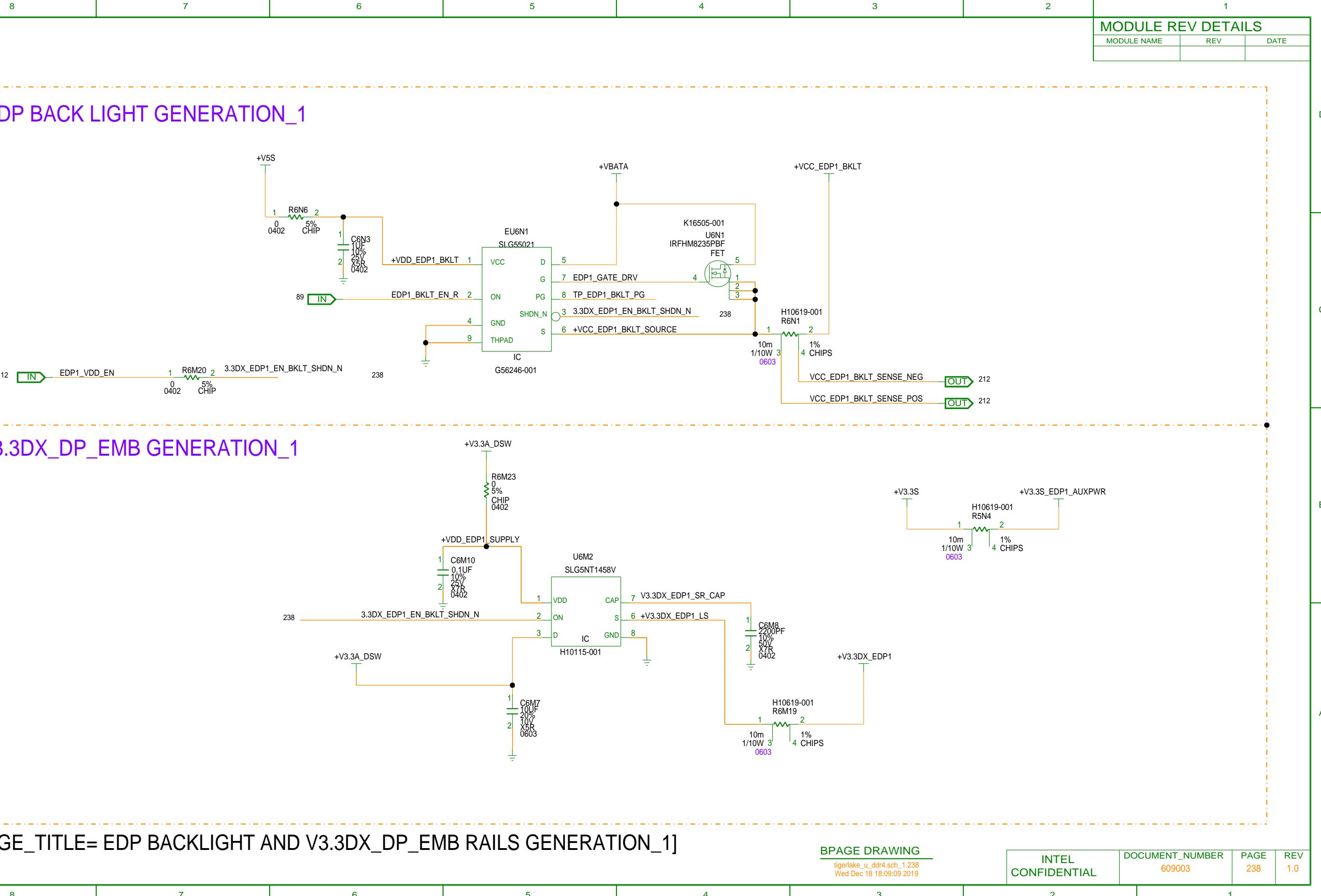
VBATA_A FOR HDA HEADER

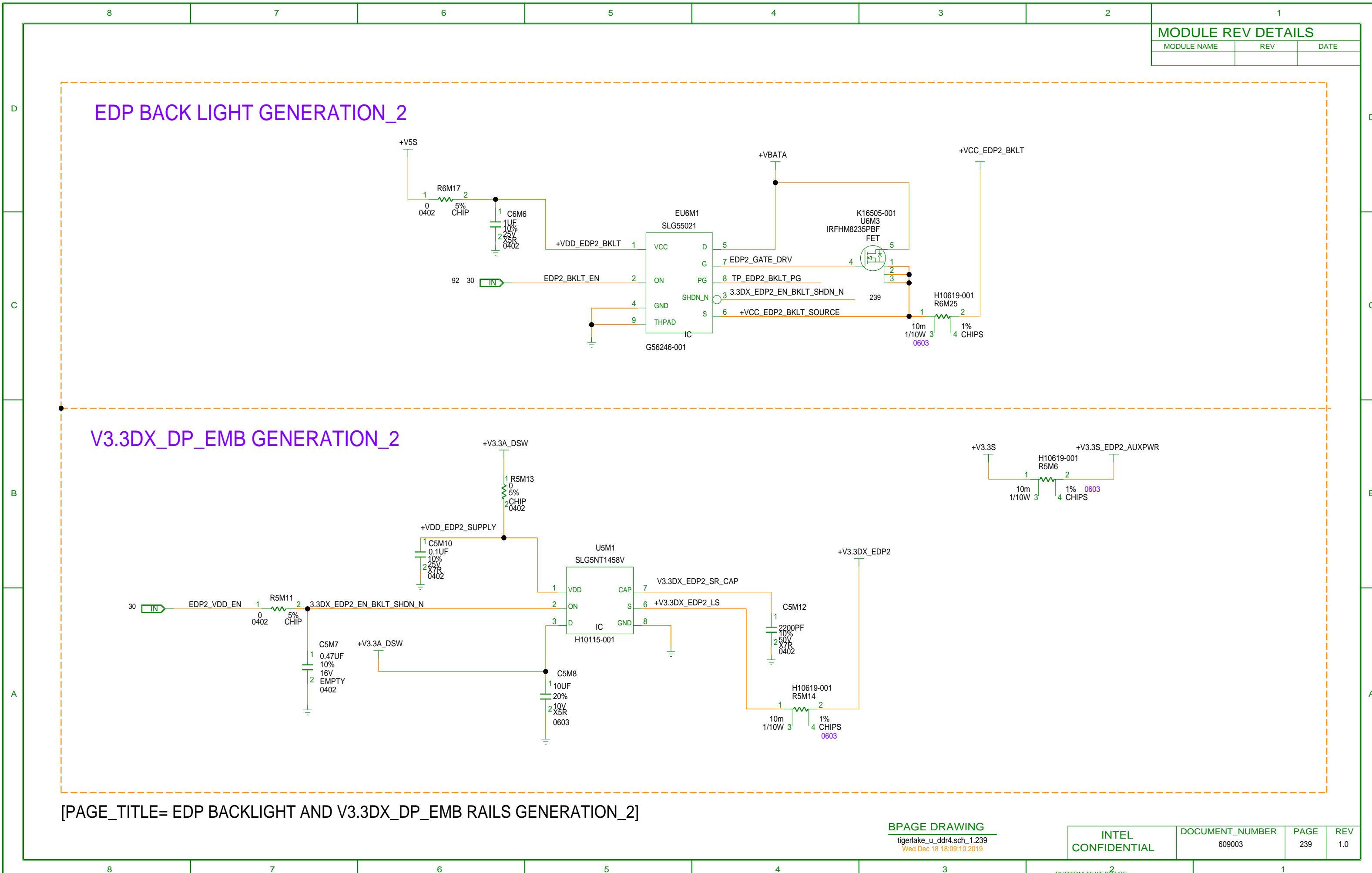
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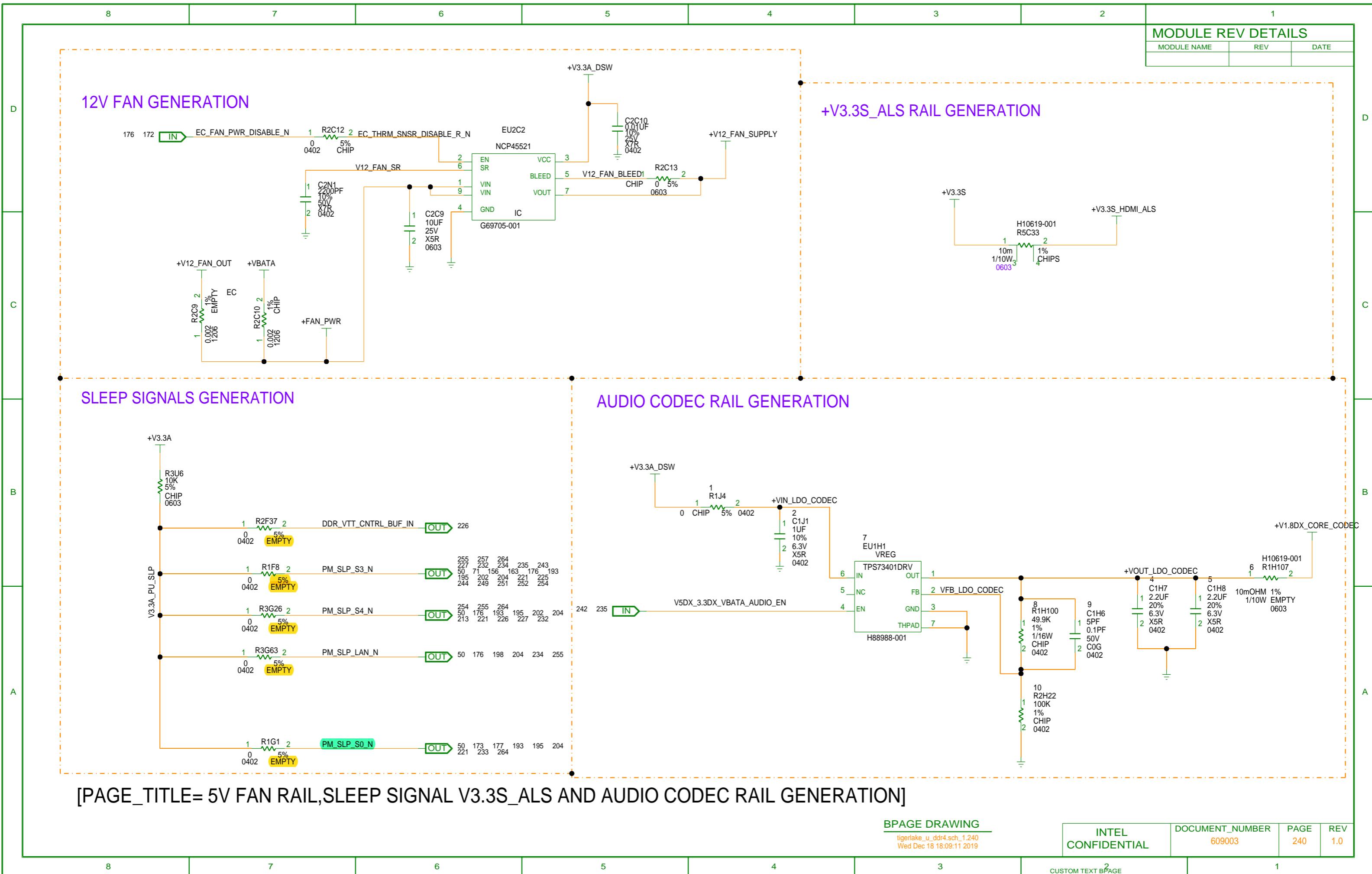
POWER SEQUENCE
VIN --> VCC --> EN
OK BY DATASHEET

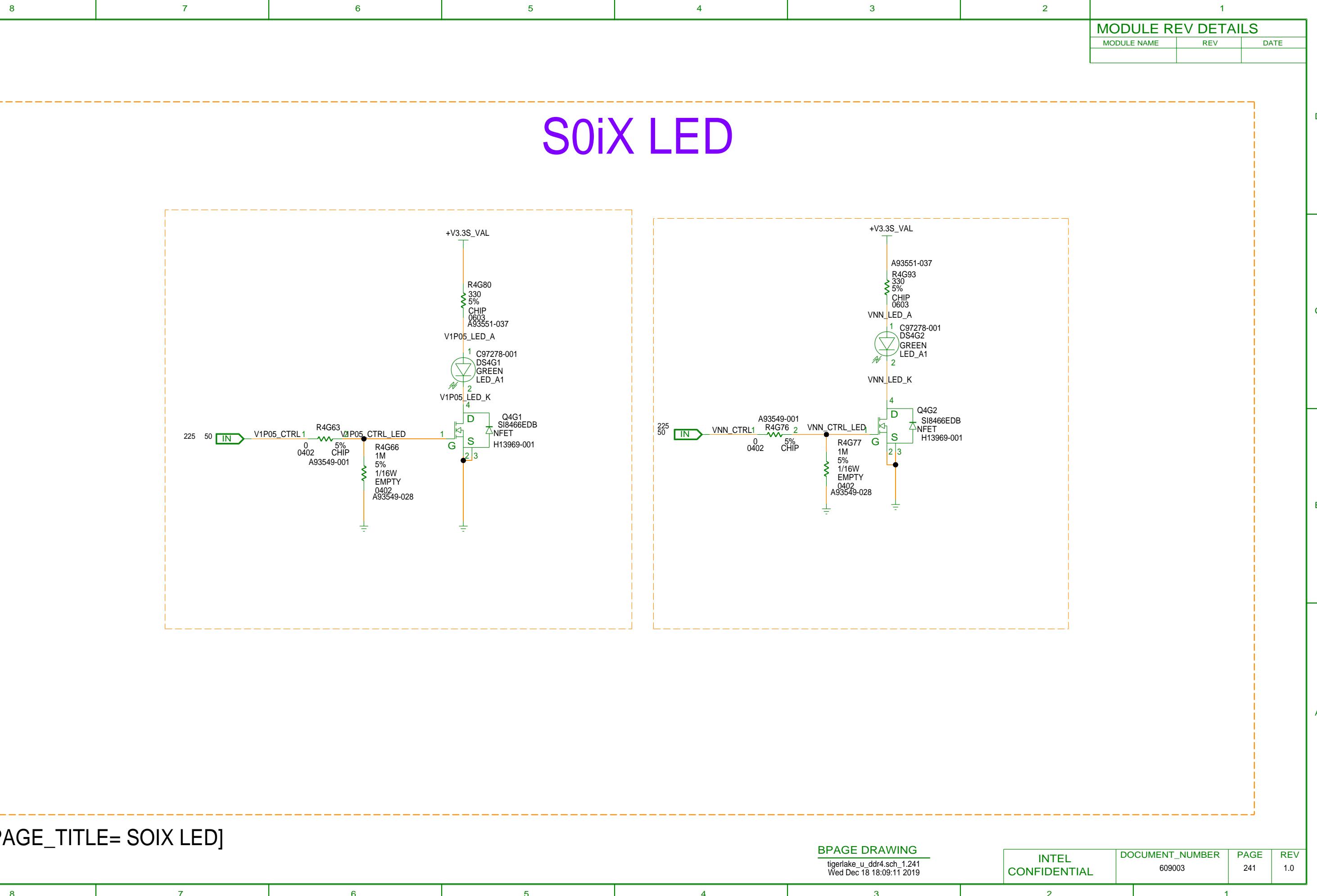


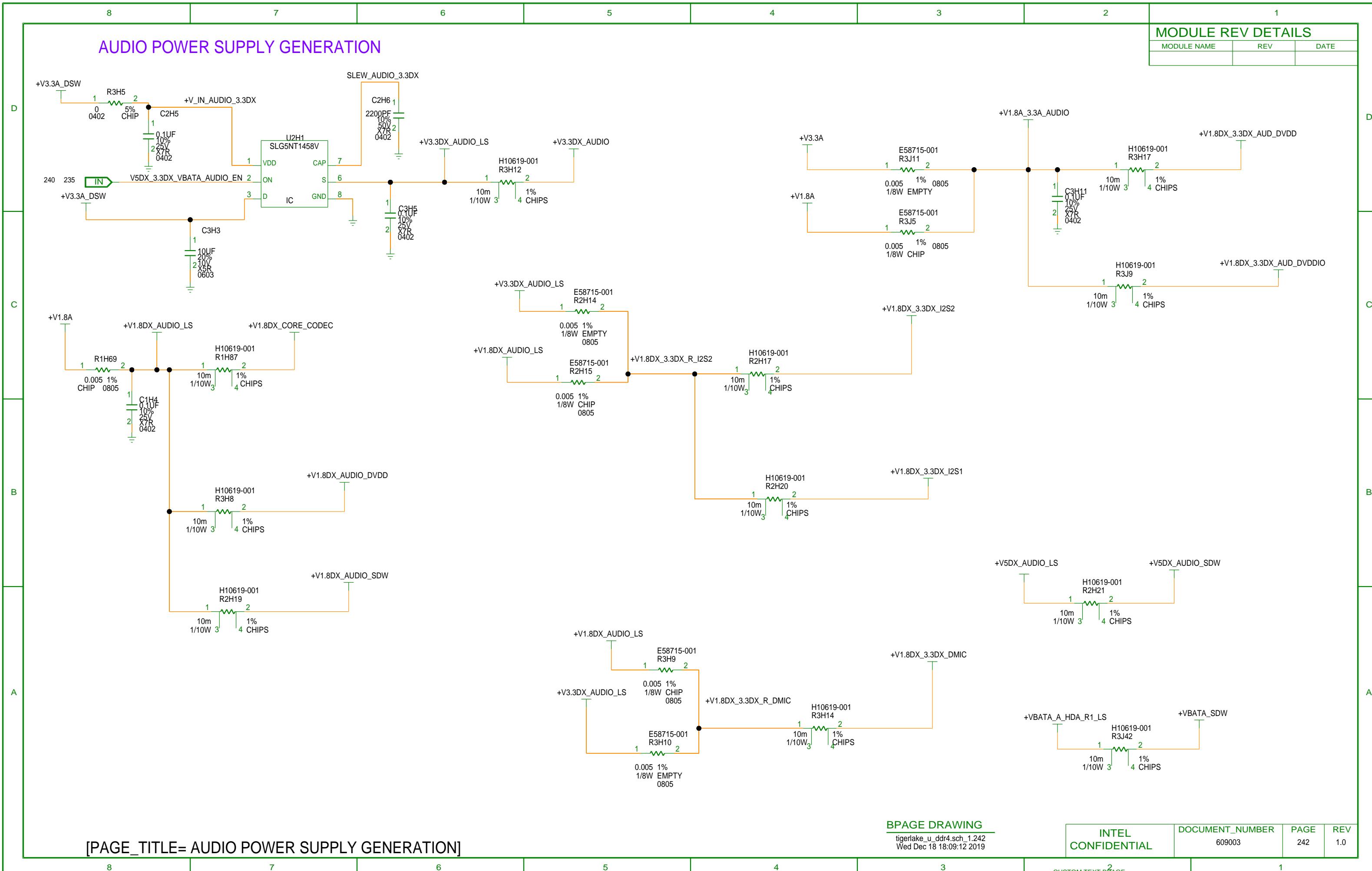


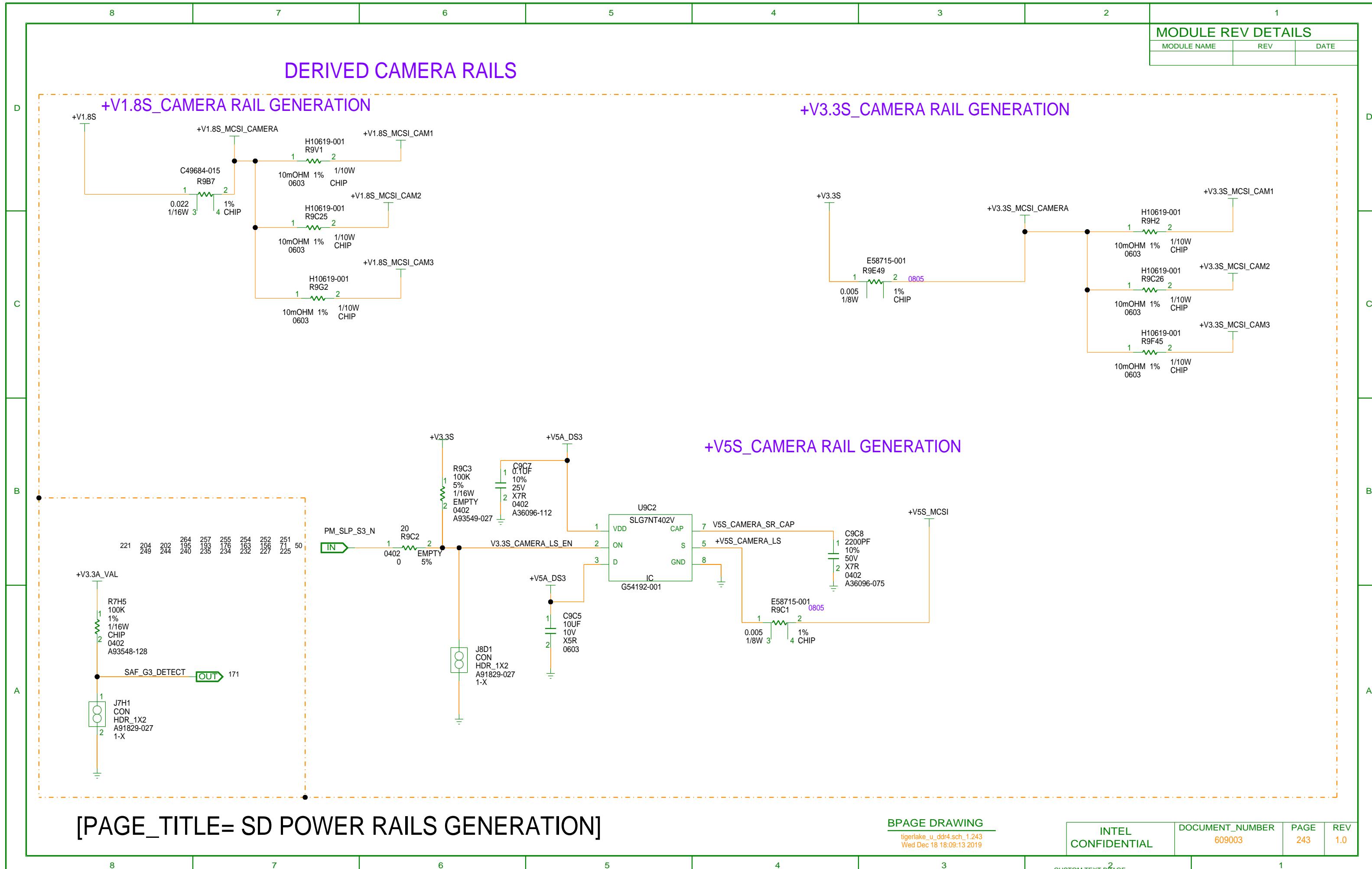


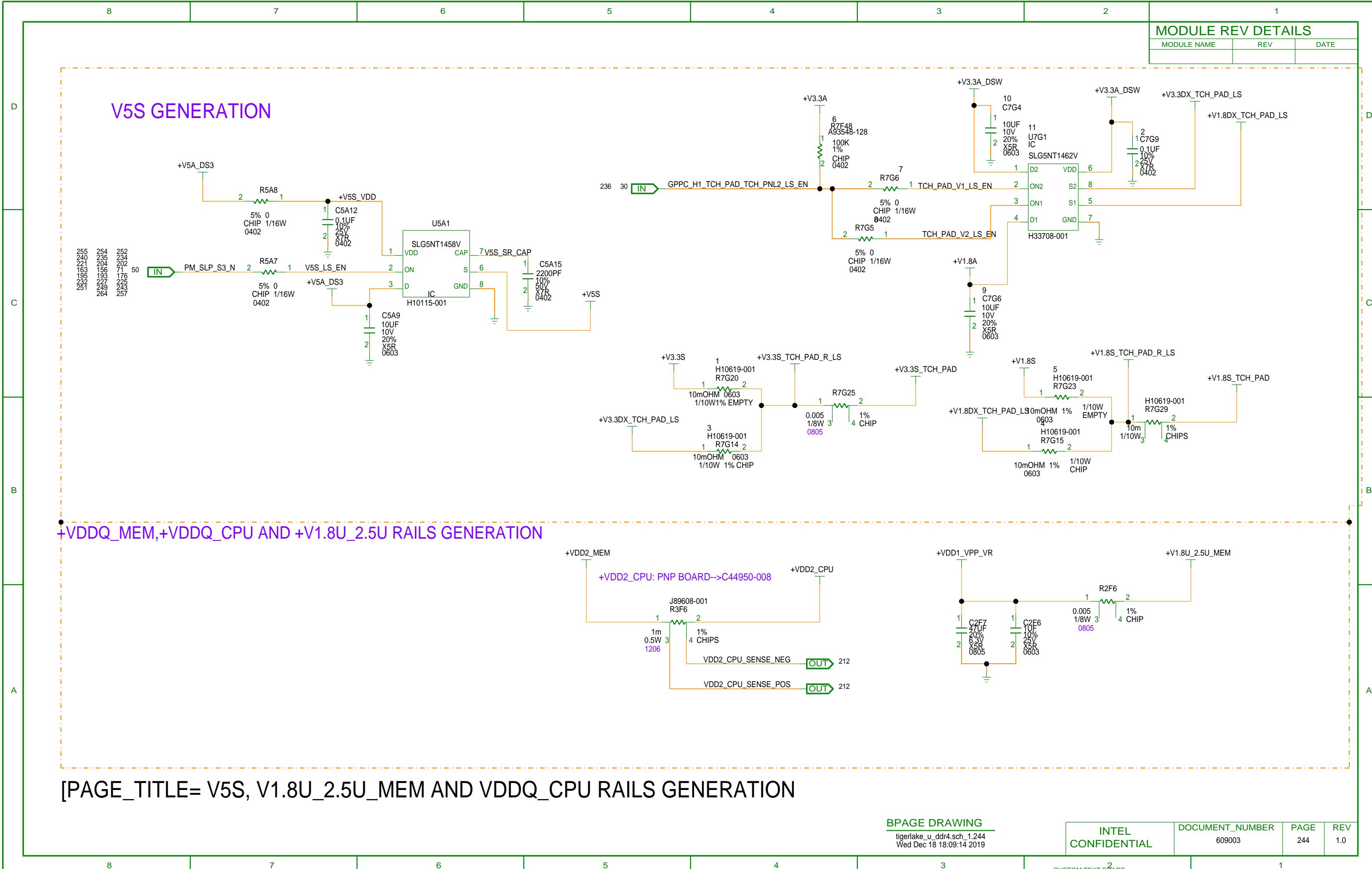






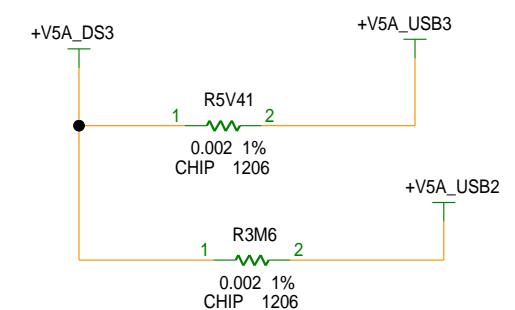
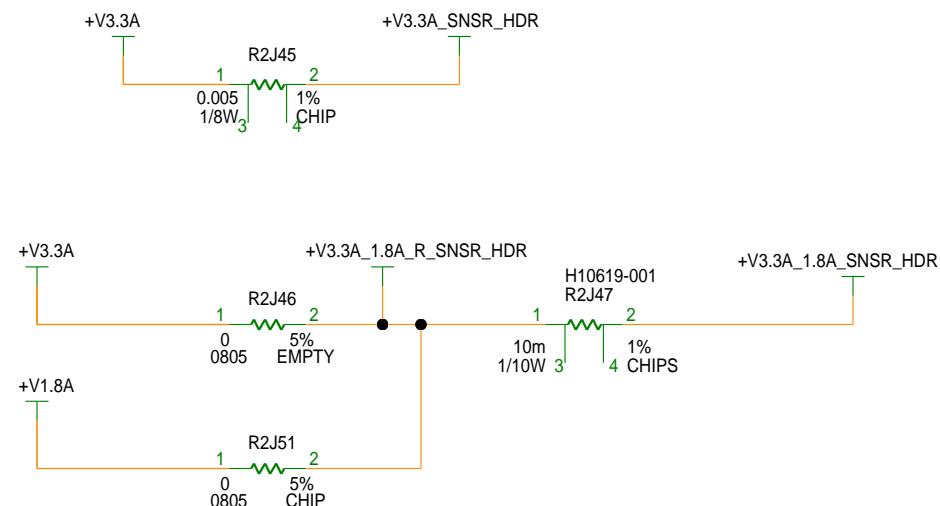
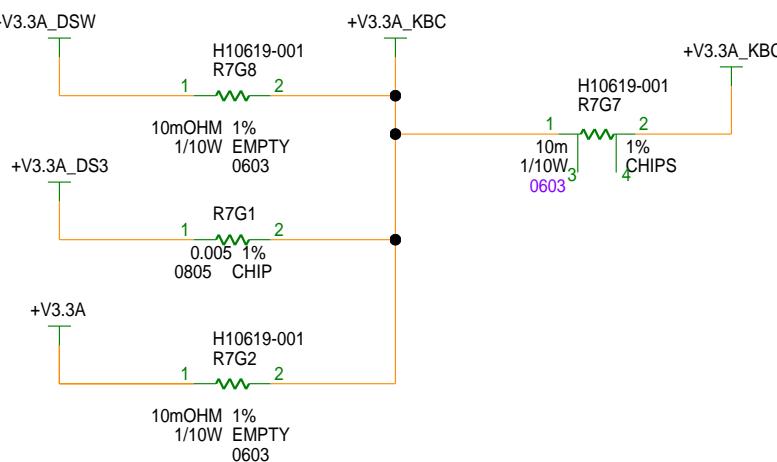


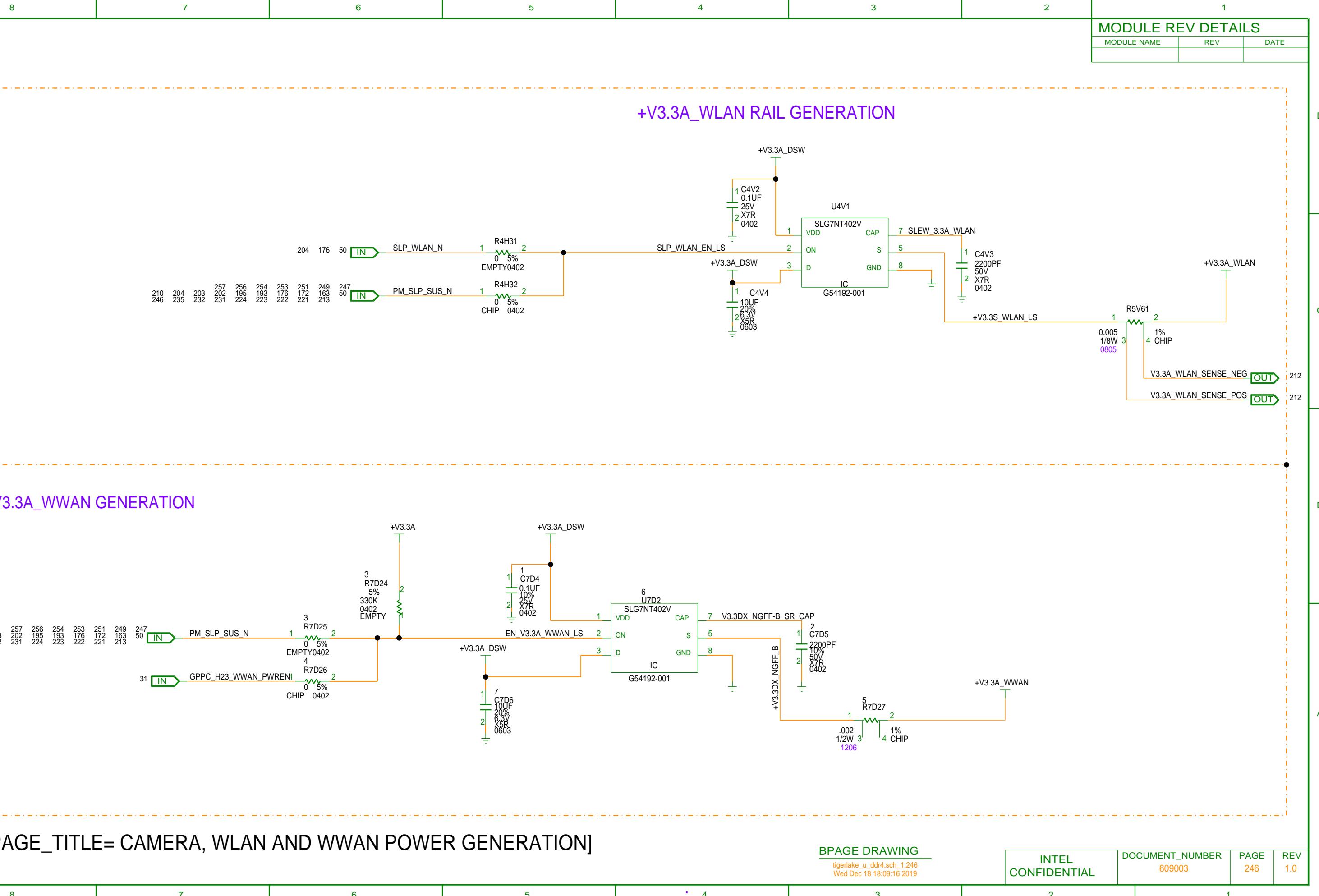


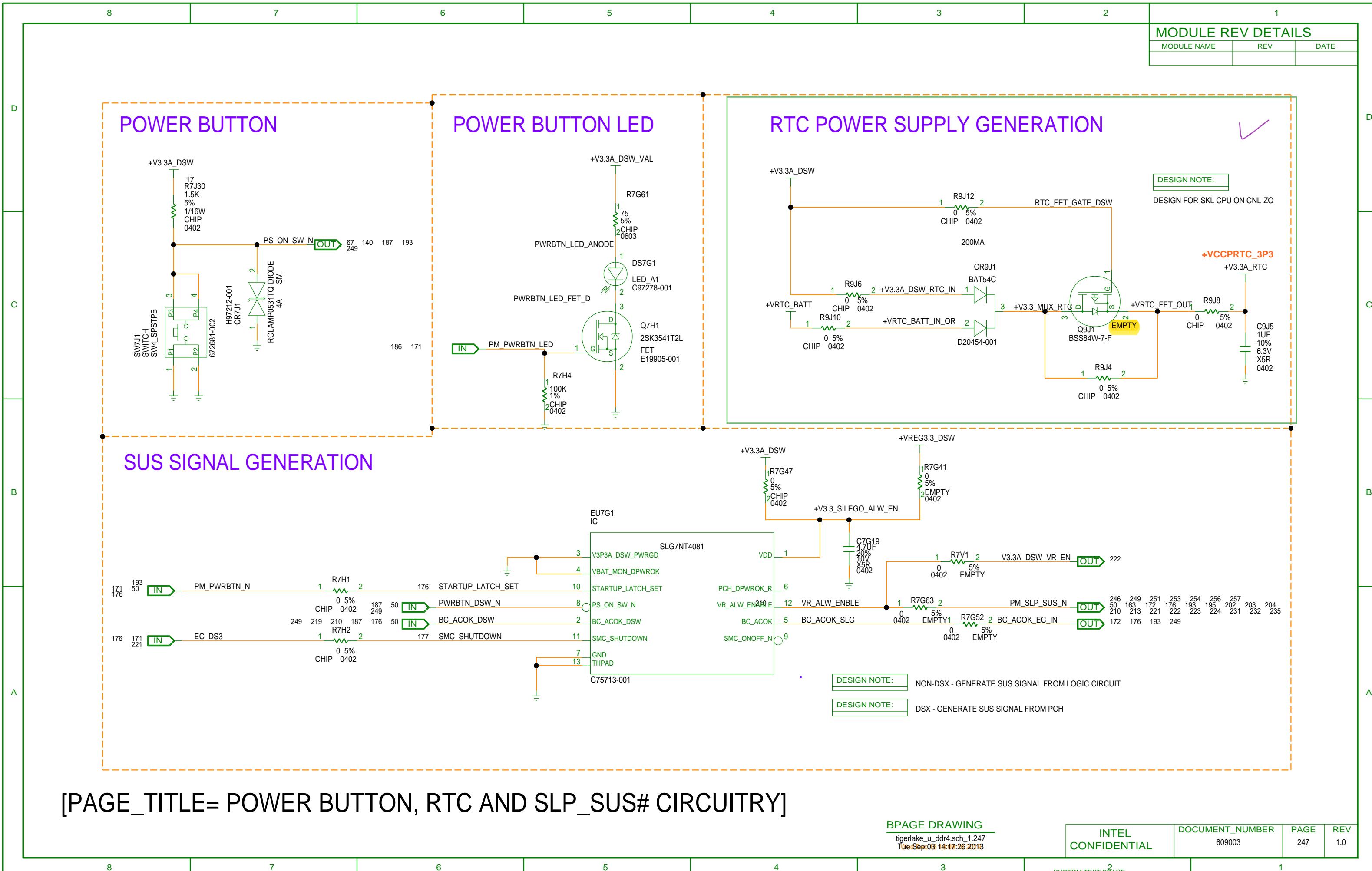


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MODULE REV DETAILS							

DERIVED POWER RAILS

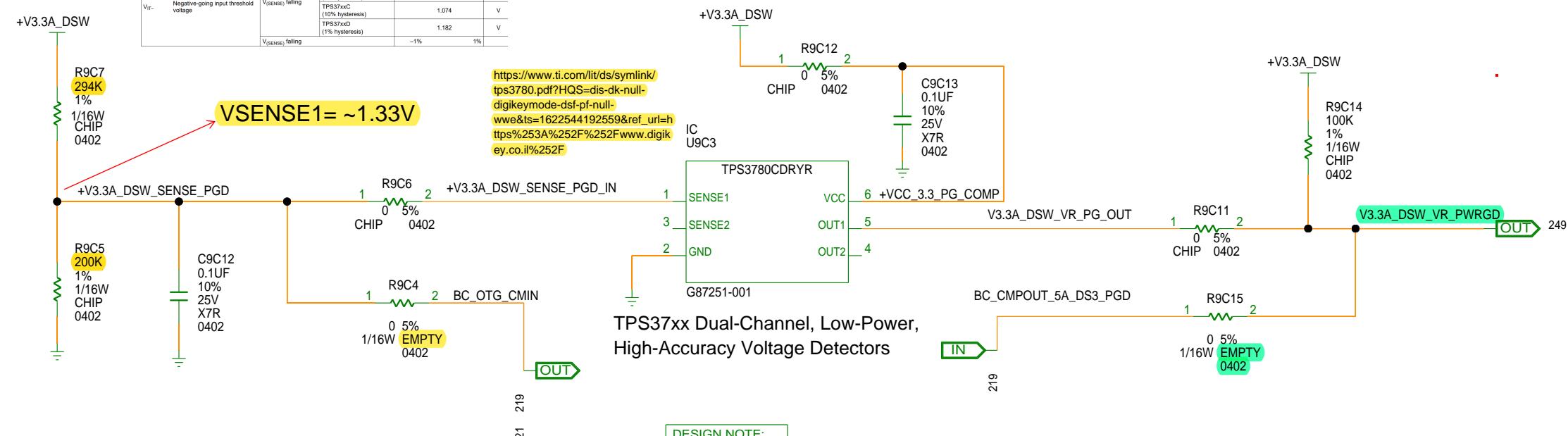
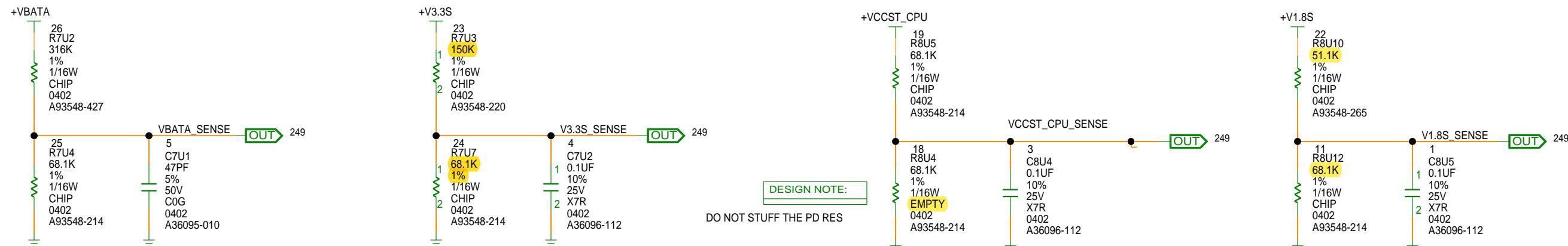






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MODULE NAME		REV	DATE				

POWER SEQUENCING LOGIC - PAGE I

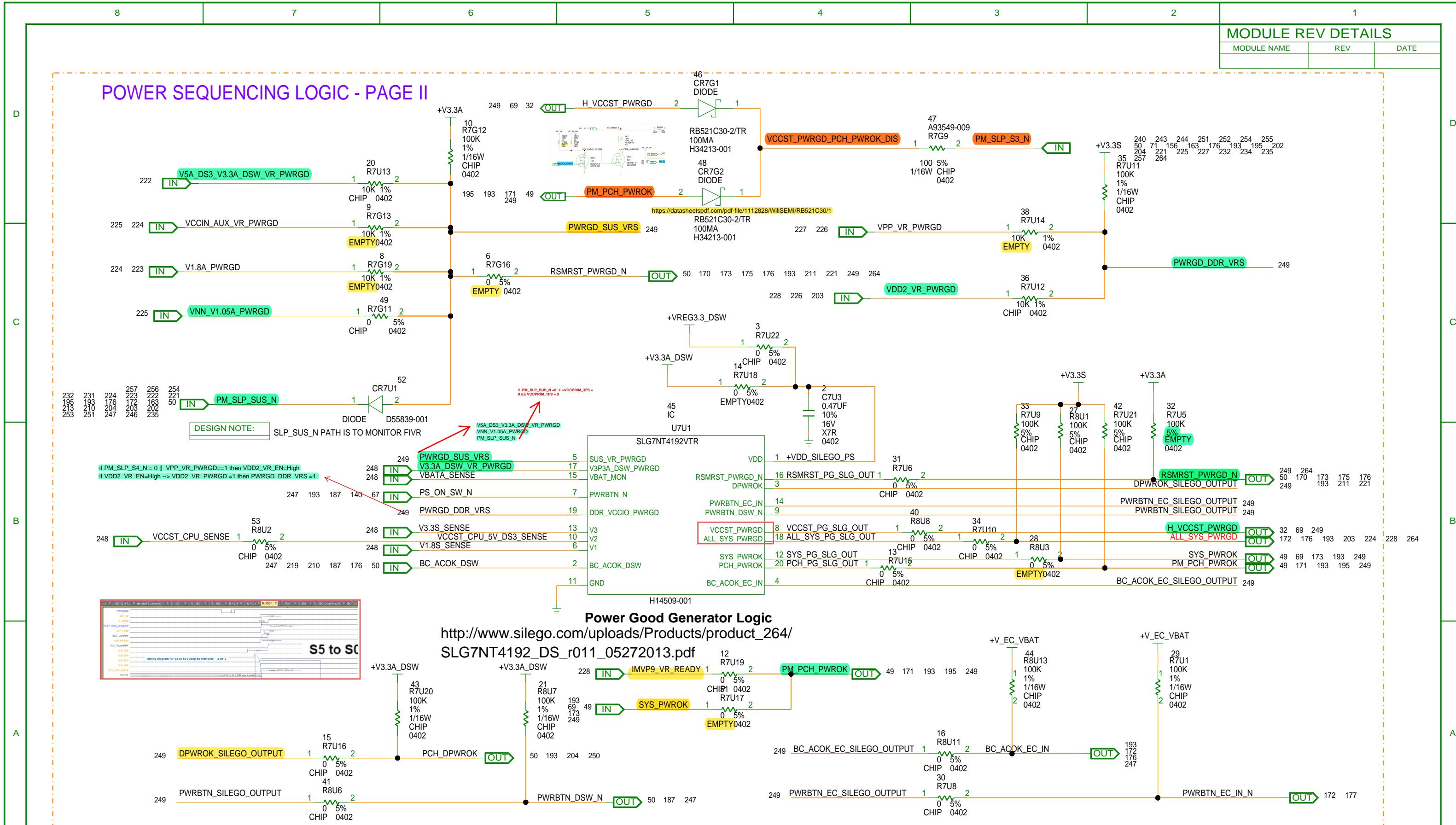


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Wed Dec 18 18:09:17 2019

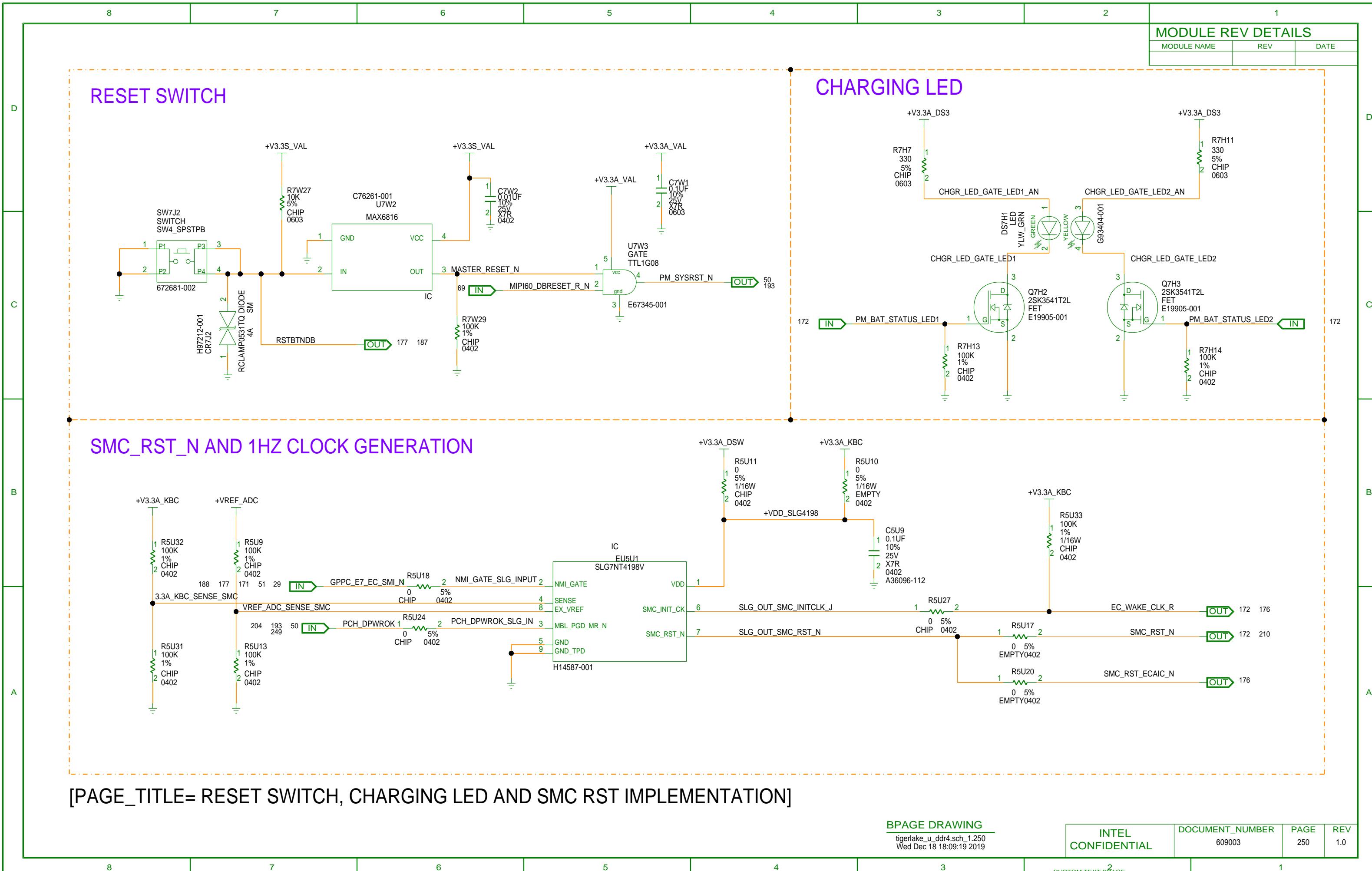
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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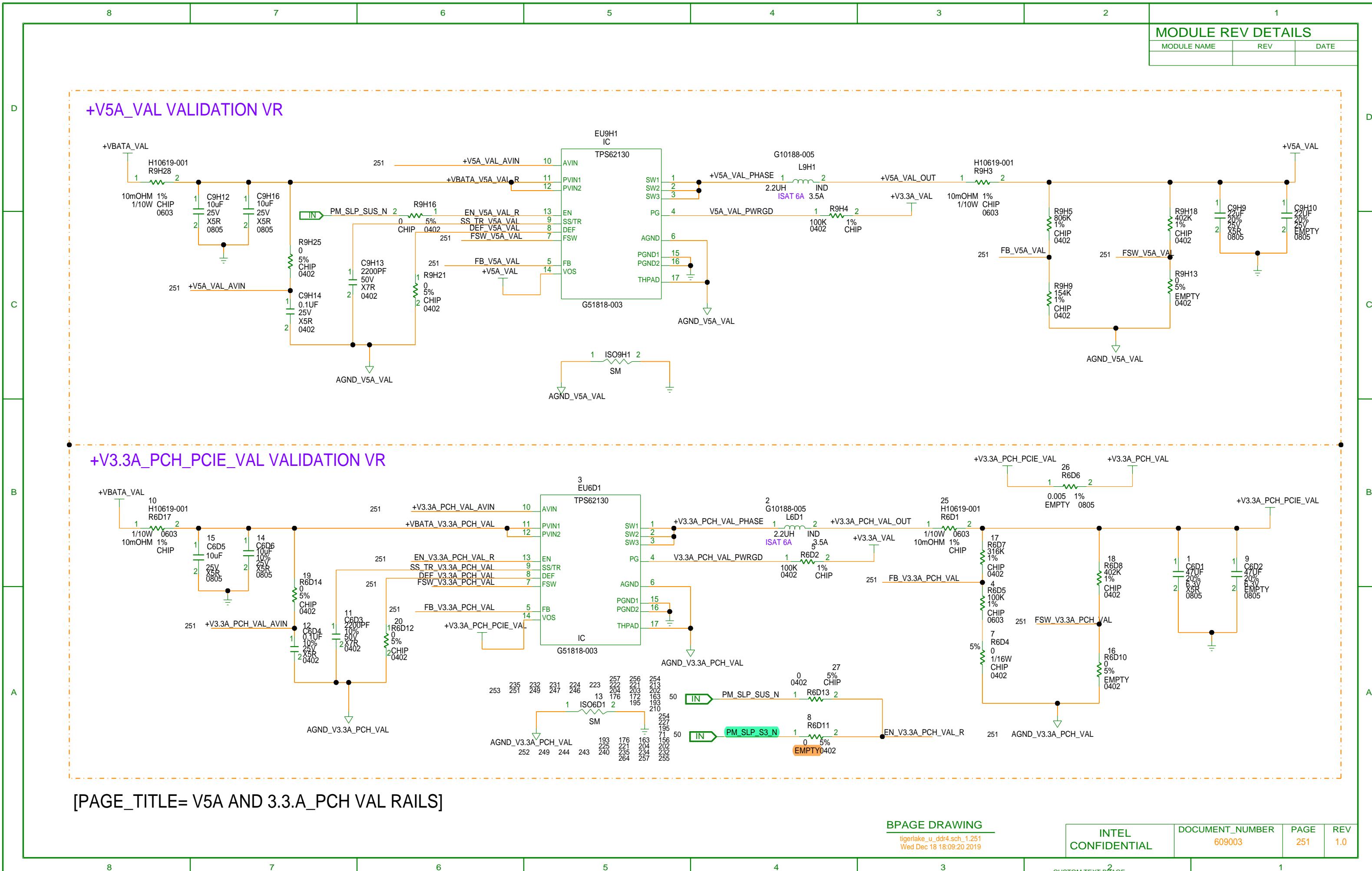


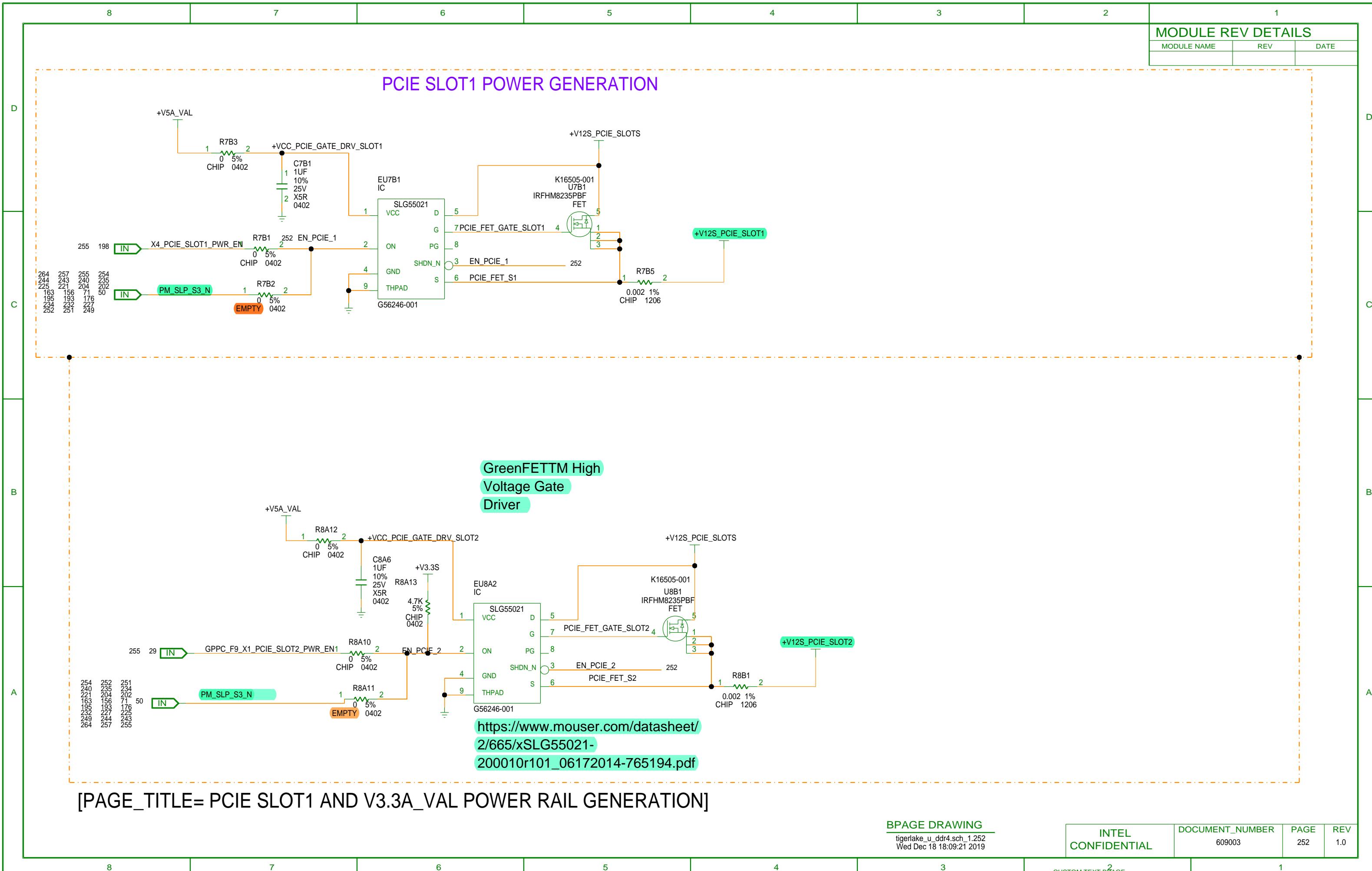
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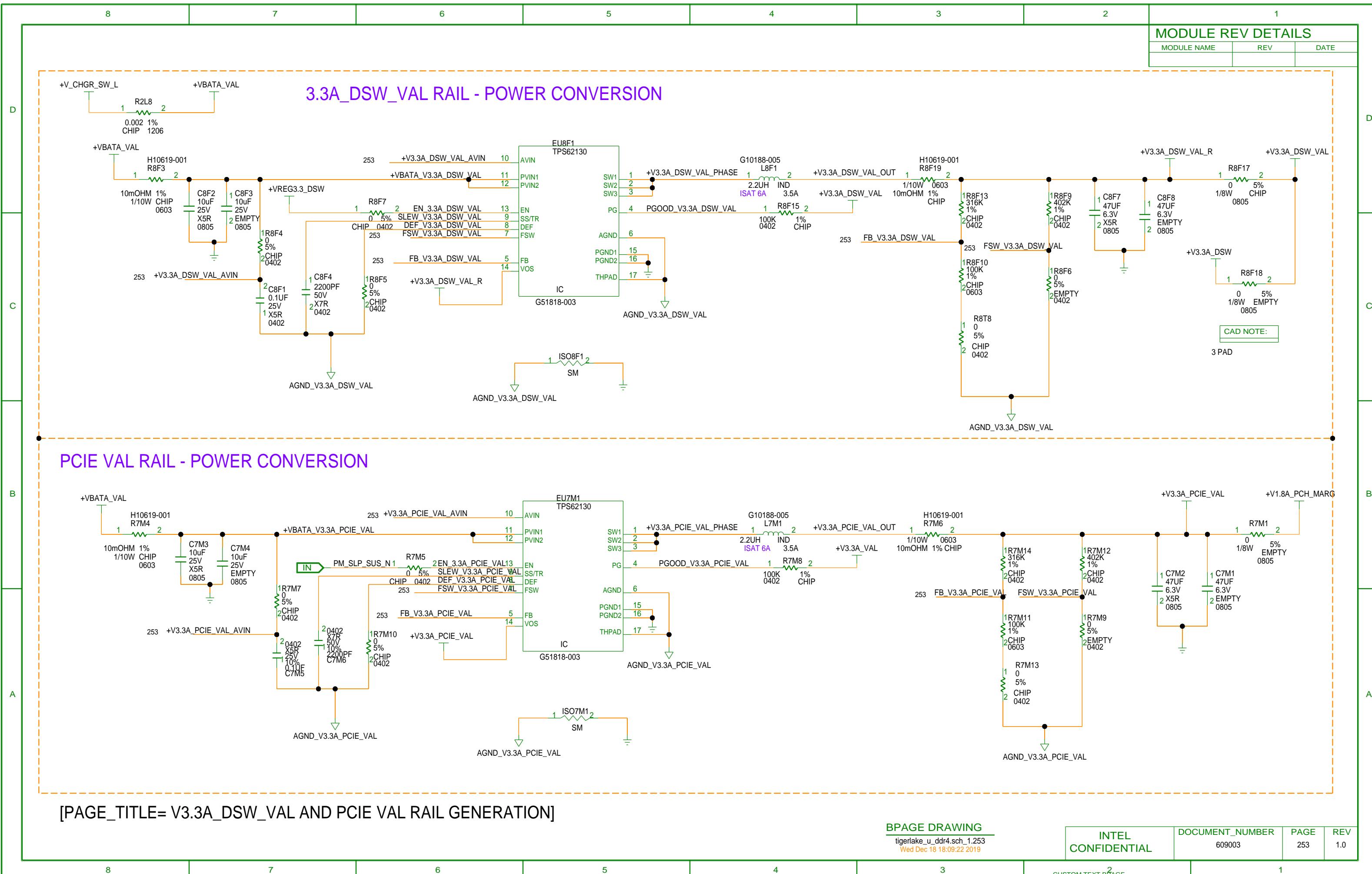
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Wed Dec 18 18:00:18 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 249	REV 1.0
2		1	



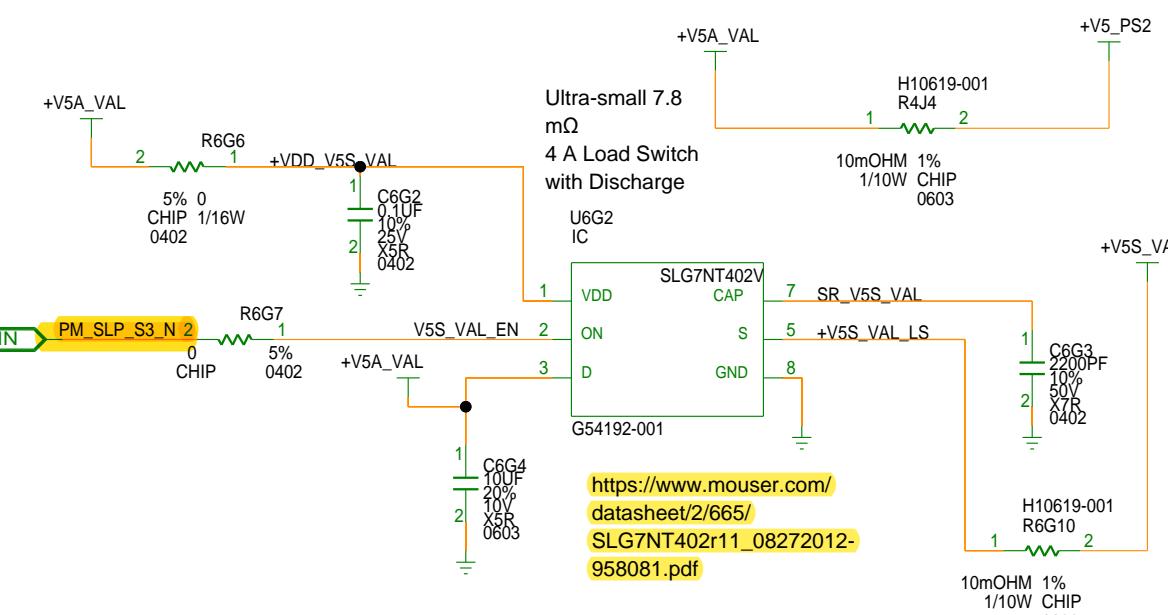




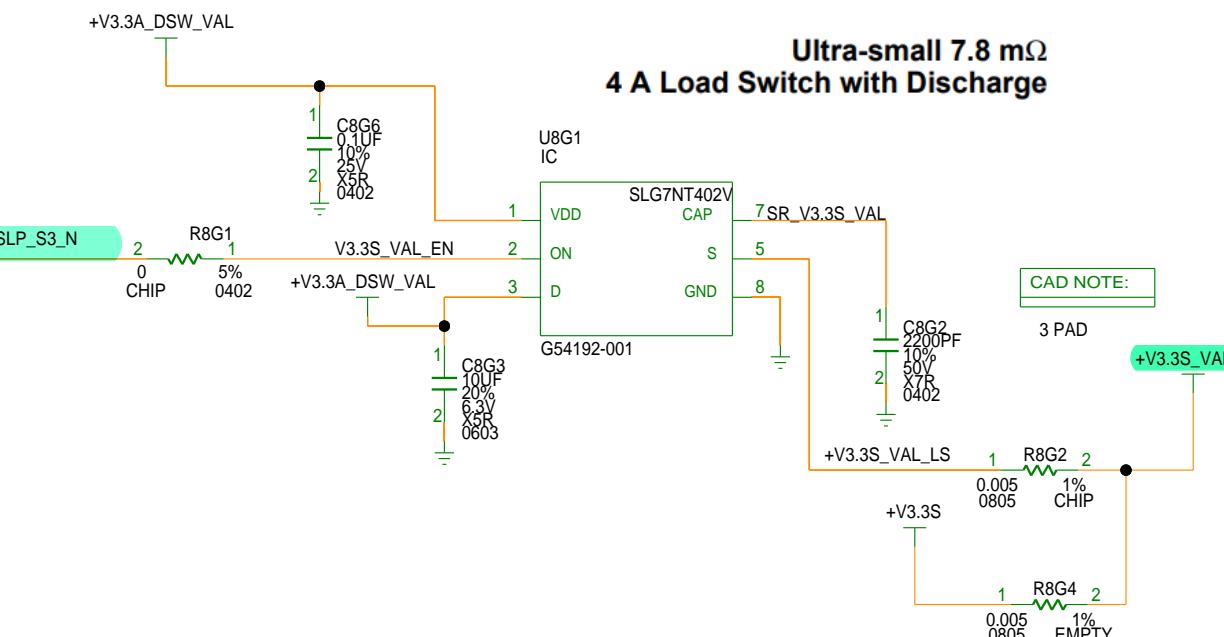


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MODULE REV DETAILS							
MODULE NAME						REV	DATE

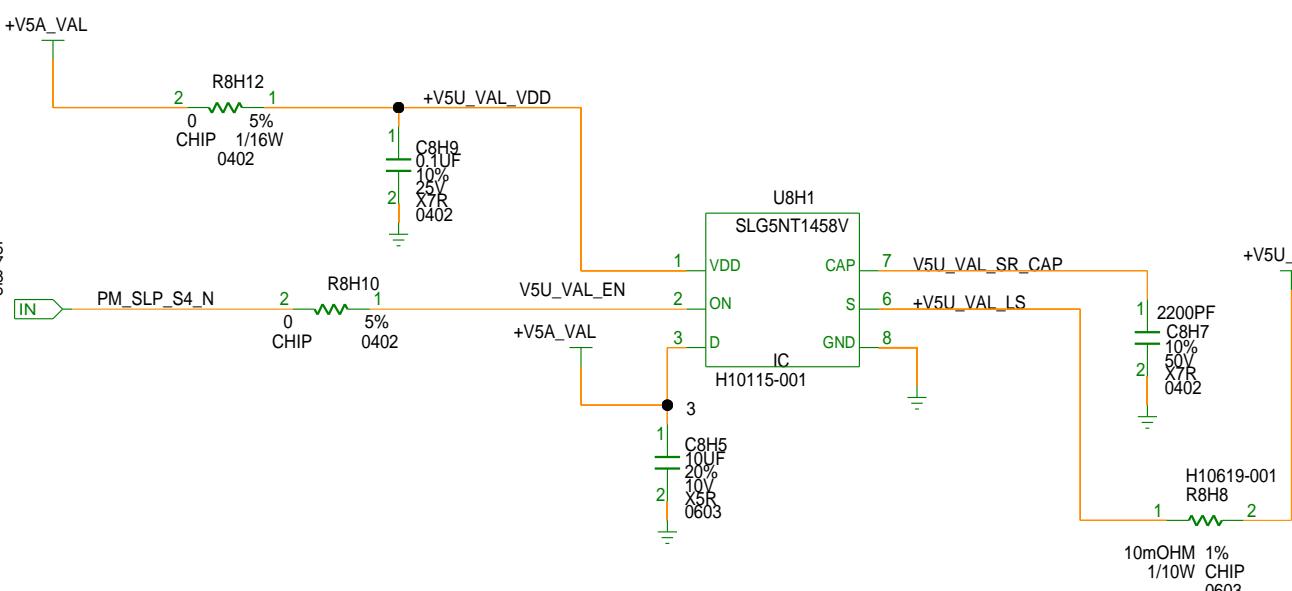
V5S_VAL GENERATION



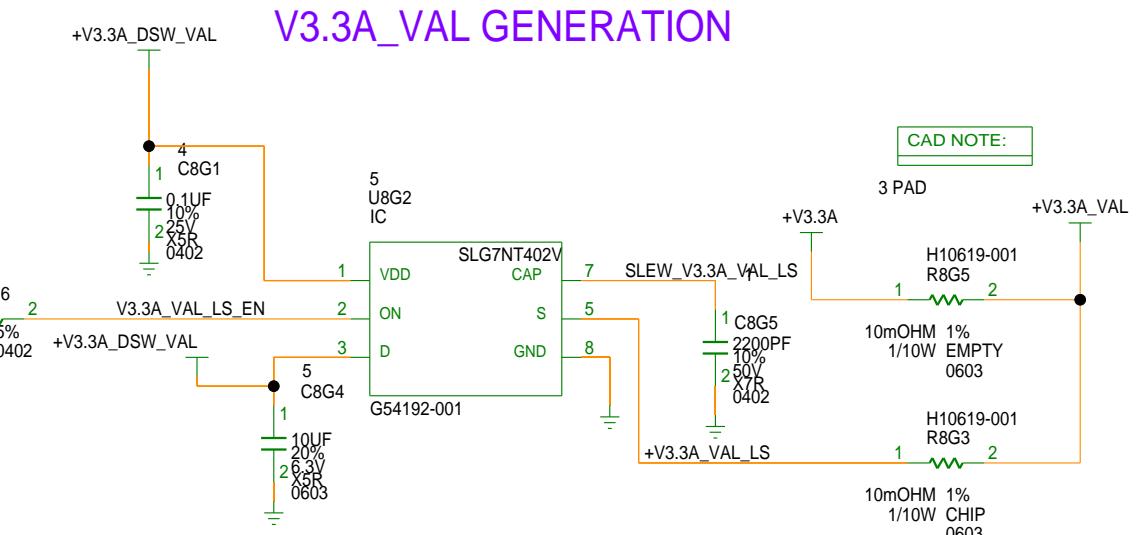
V3.3S_VAL GENERATION



V5U_VAL GENERATION



V3.3A_VAL GENERATION



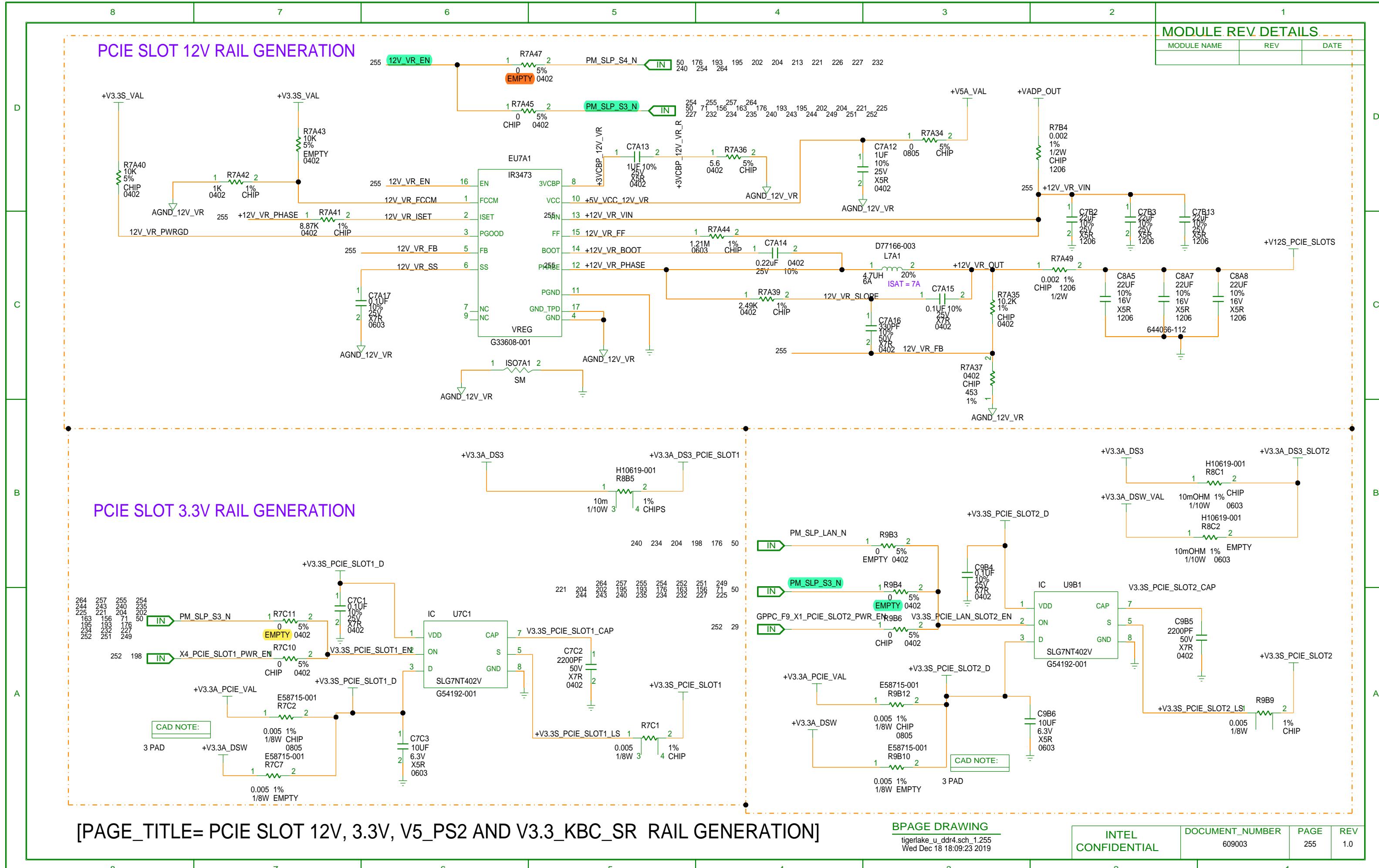
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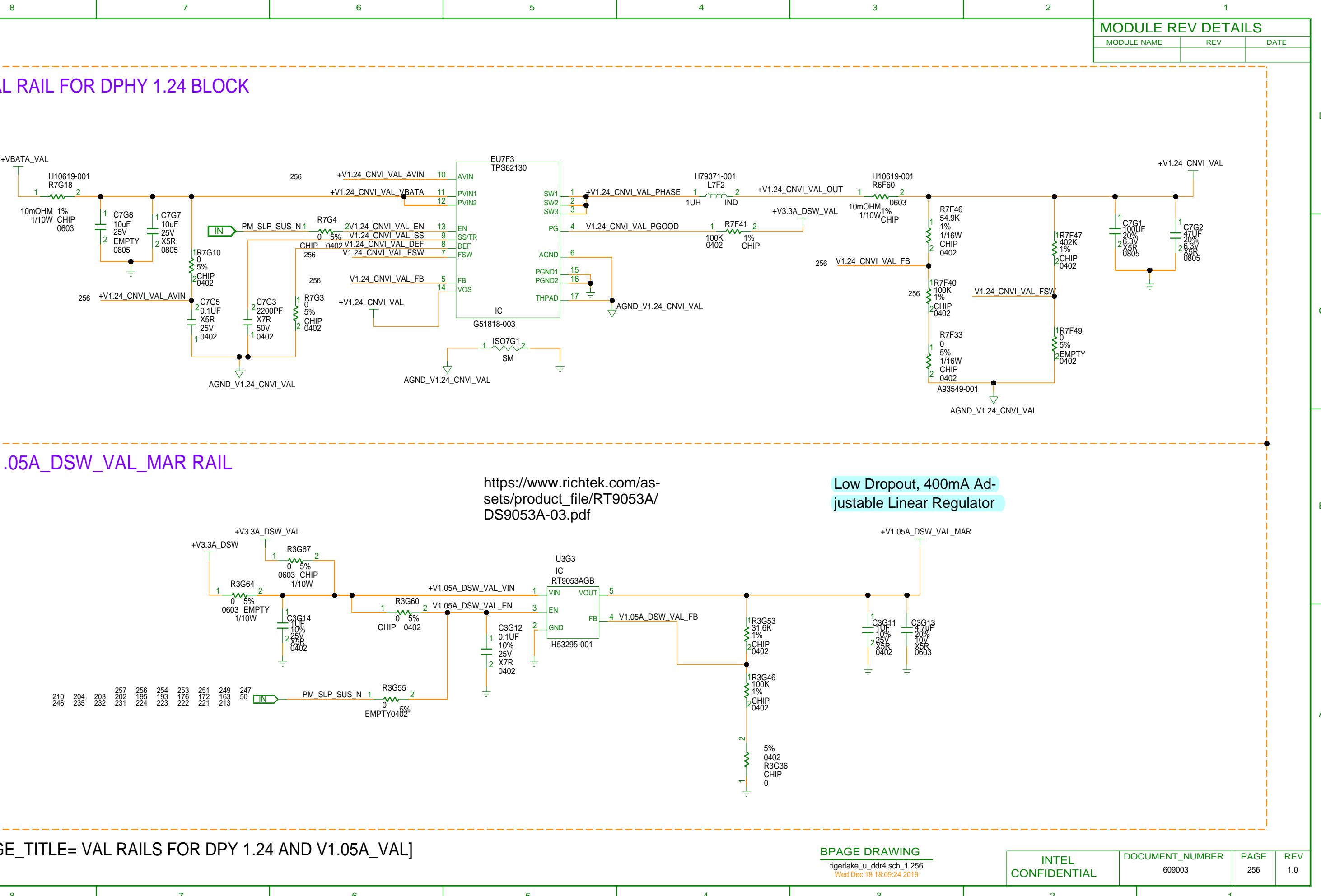
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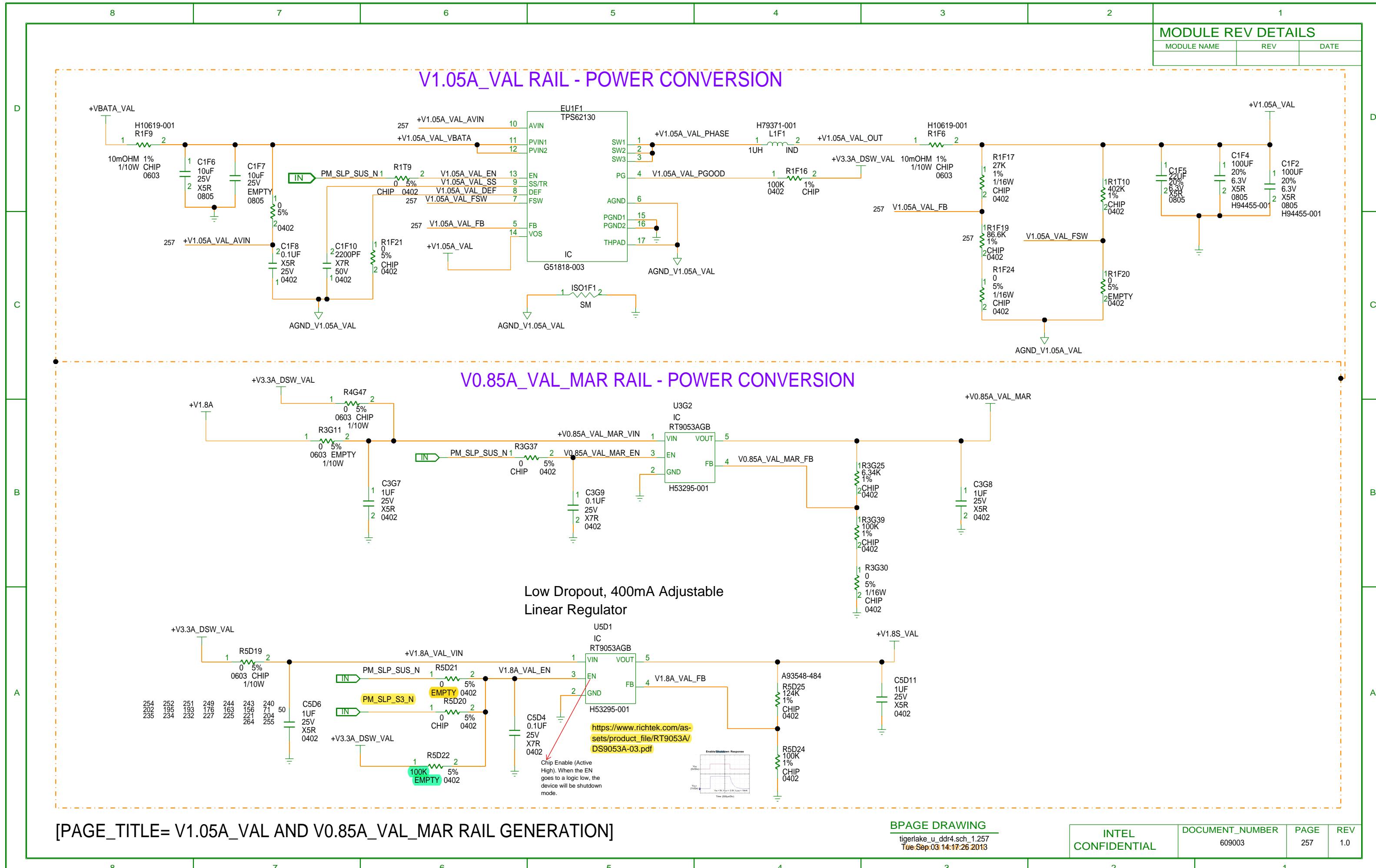
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Wed Dec 18 18:09:22 2019

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CUSTOM TEXT 2 PAGE







8	7	6	5	4	3	2	1
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

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D

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MTG_HOLE
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G39082-001

STF_MTG_HOLE
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MH1B1
MTG_HOLE
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G39082-001

STF_MTG_HOLE
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C

C

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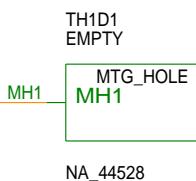
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G39082-001

STF_MTG_HOLE
EMPTY
MH9J1
MTG_HOLE
 9
GND=1,2,3,4,5,6,7,8
G39082-001

B

B

STF_MTG_HOLE
EMPTY
MH9F1
MTG_HOLE
 9
GND=1,2,3,4,5,6,7,8
G39082-001



ADDED FOR MEMORY INTERPOSER

[PAGE_TITLE=MOUNTING HOLES]

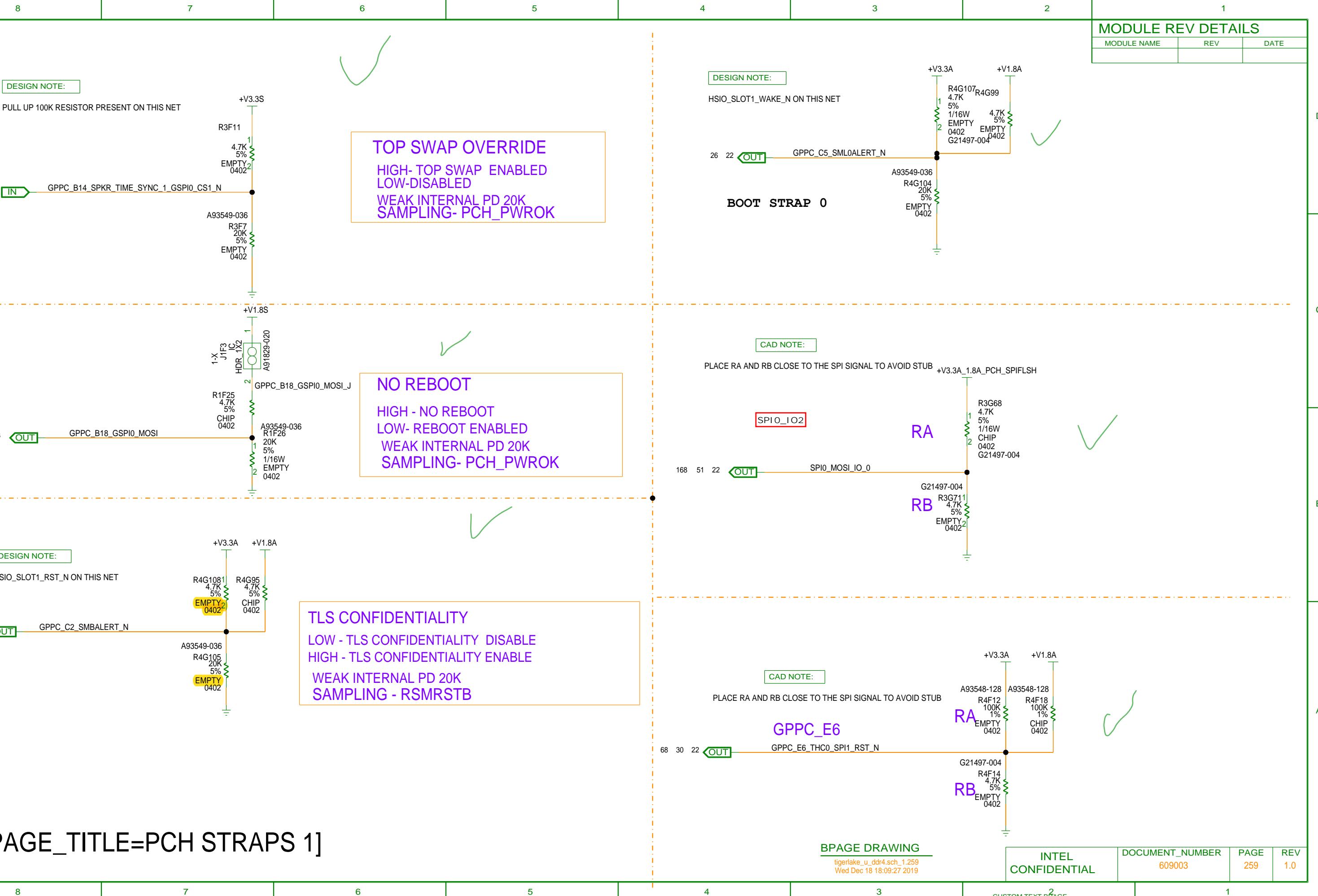
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Wed Dec 18 18:09:26 2019

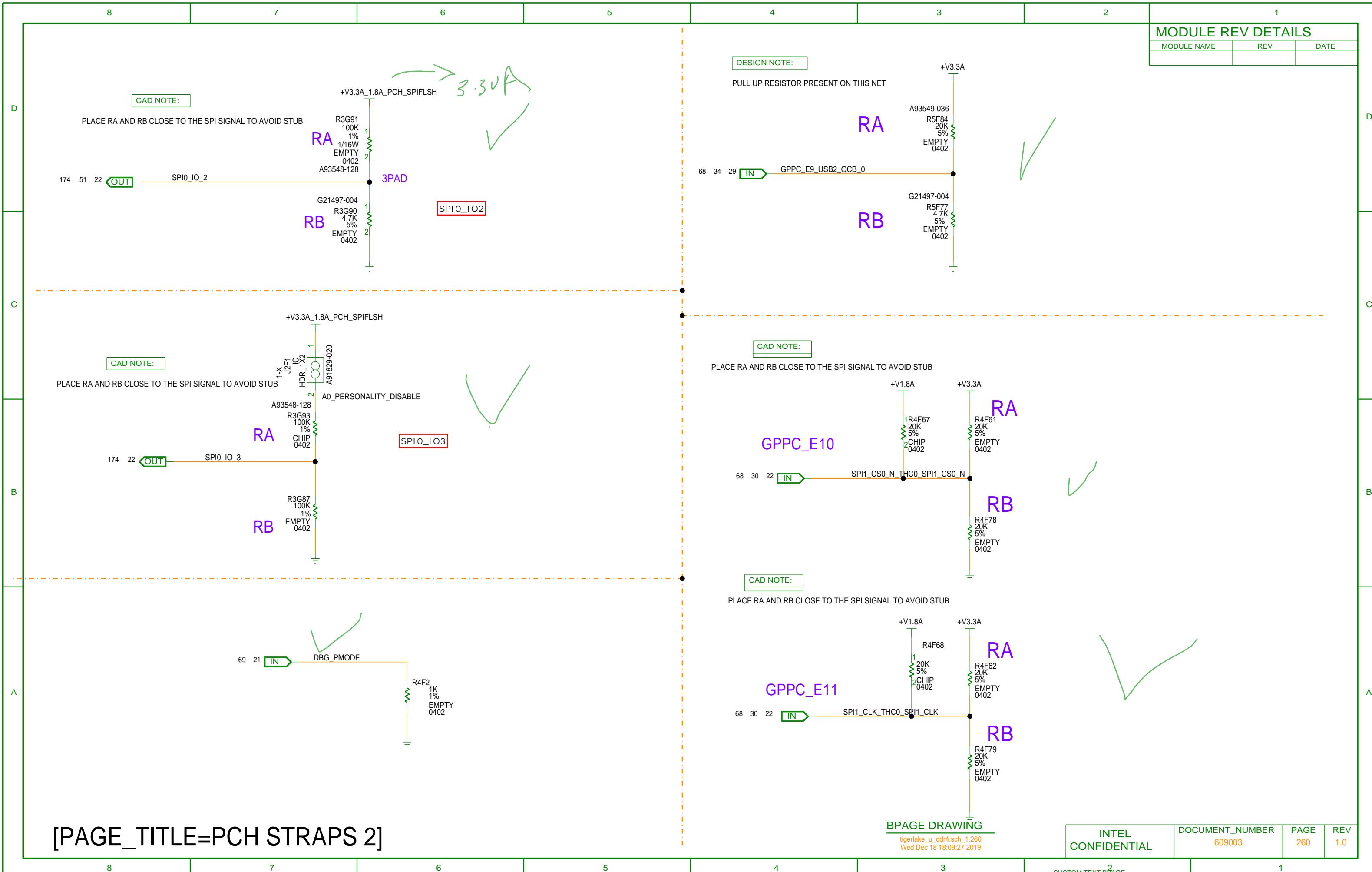
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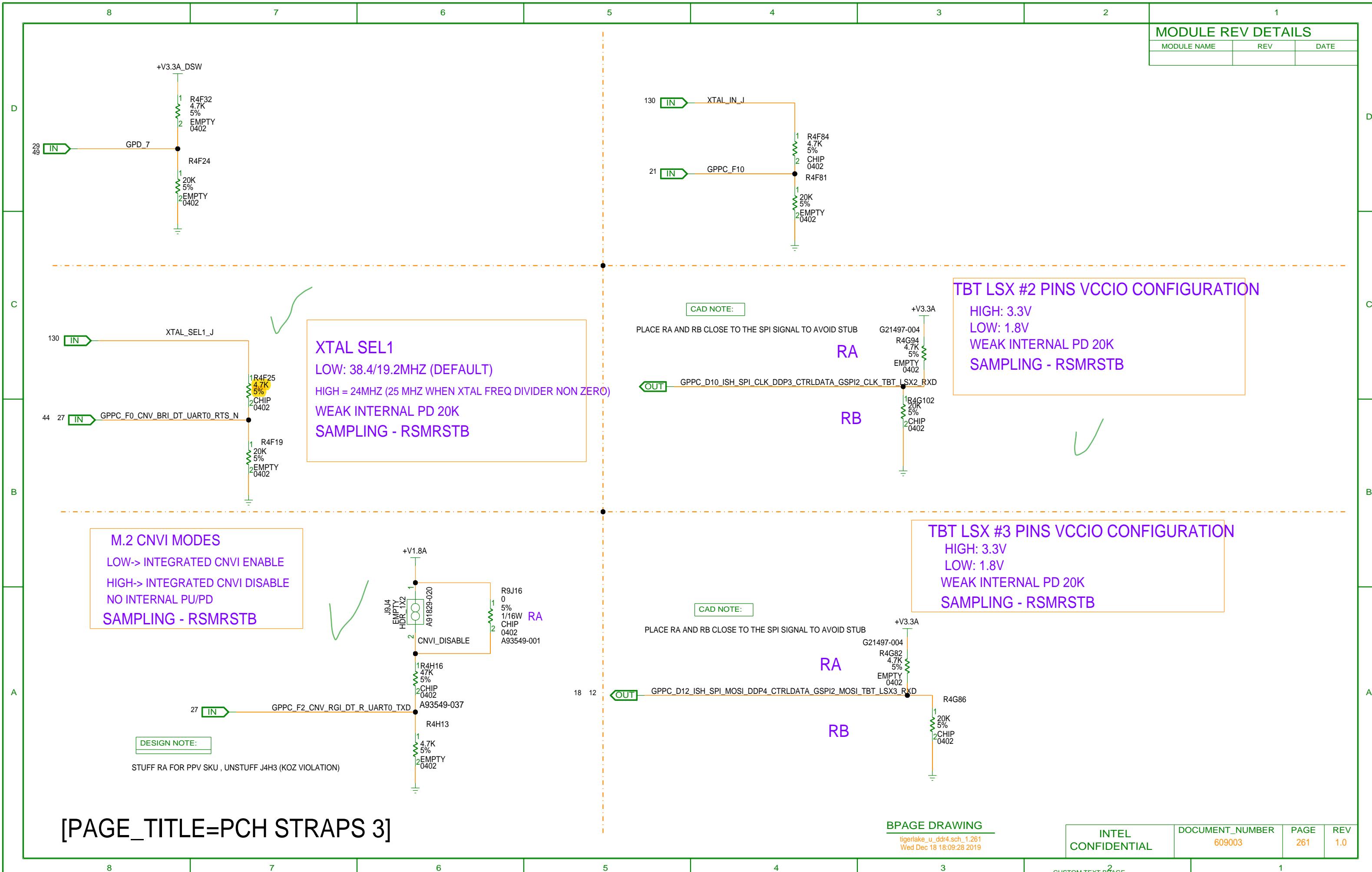
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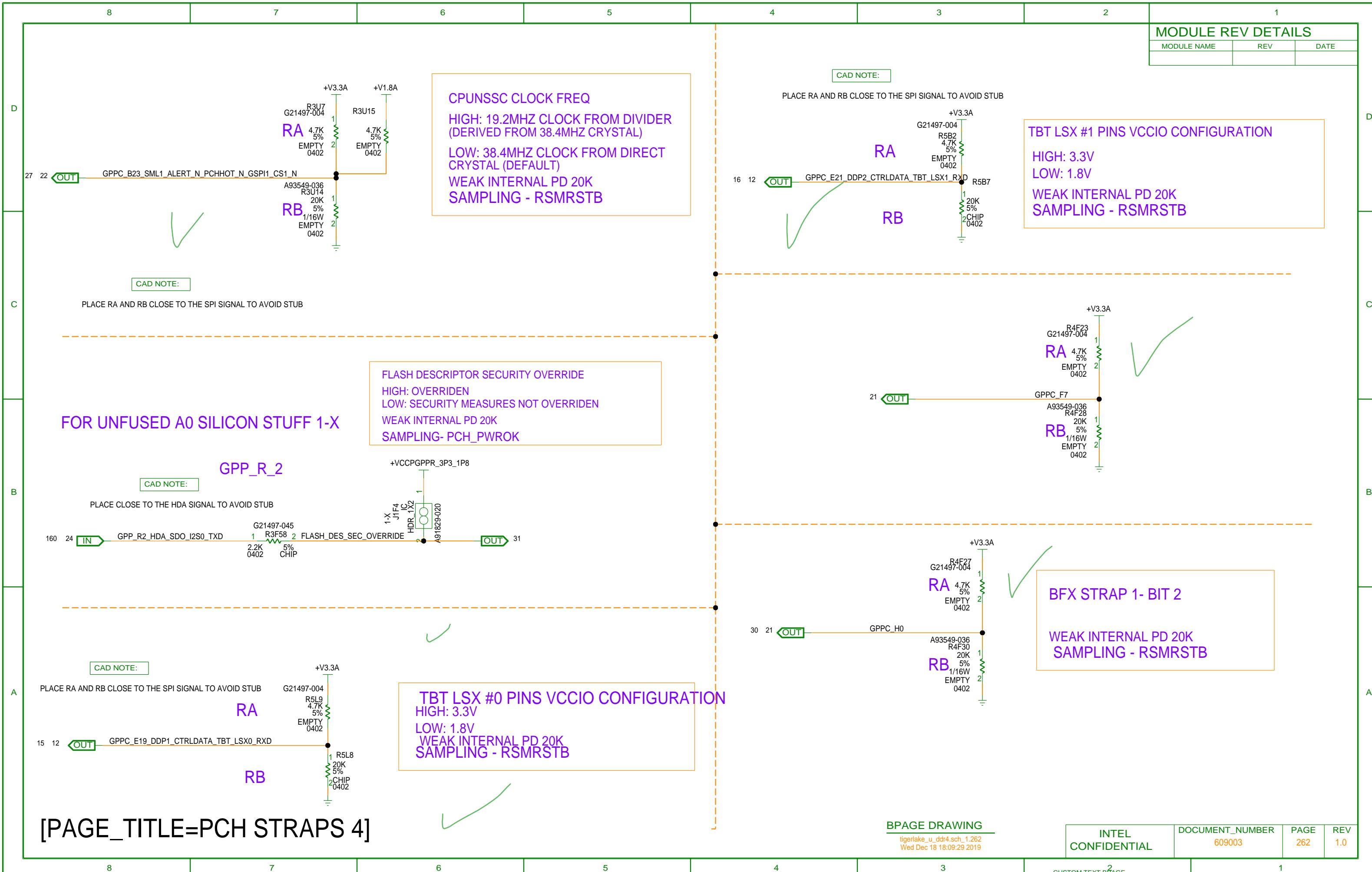
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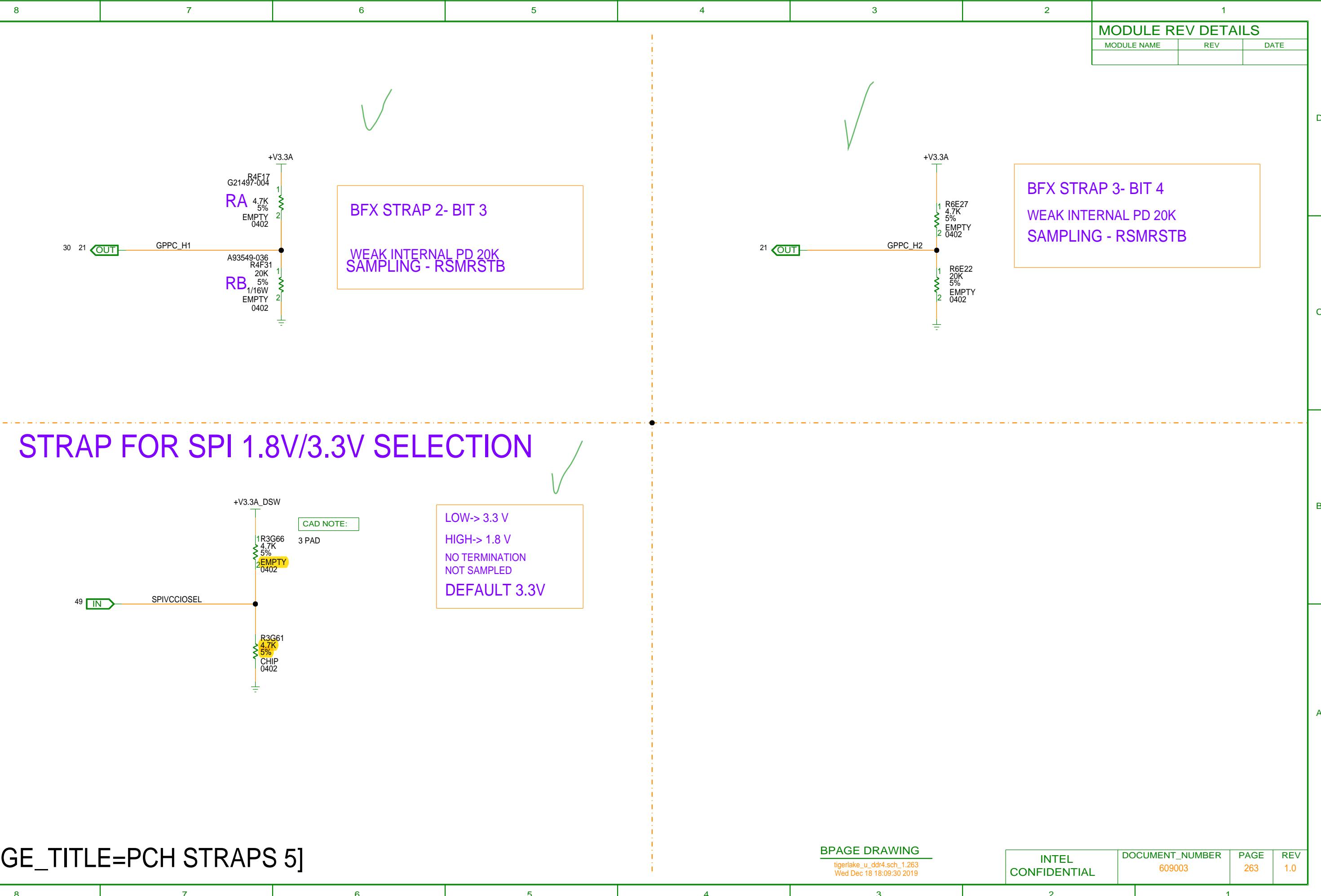
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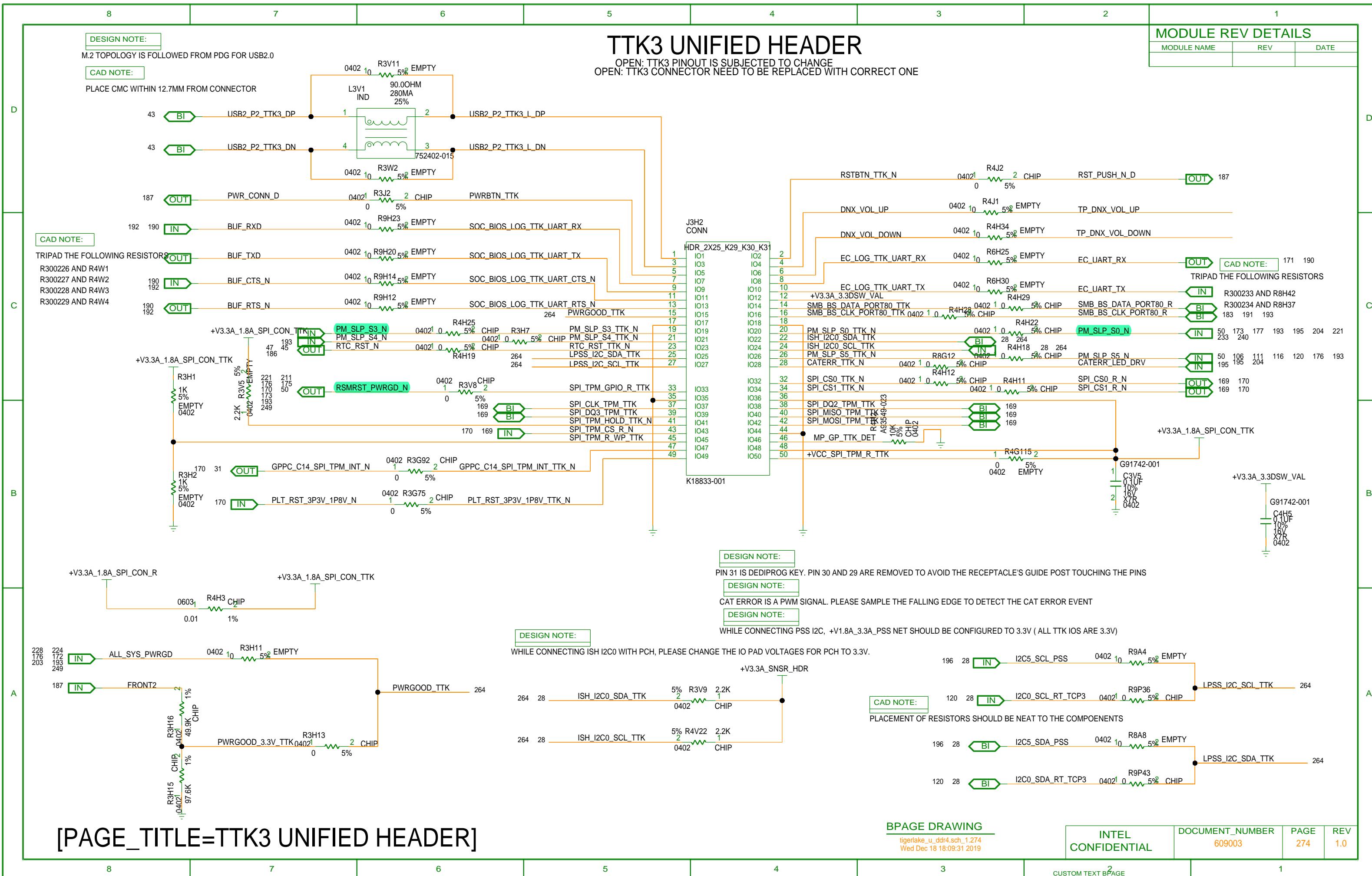


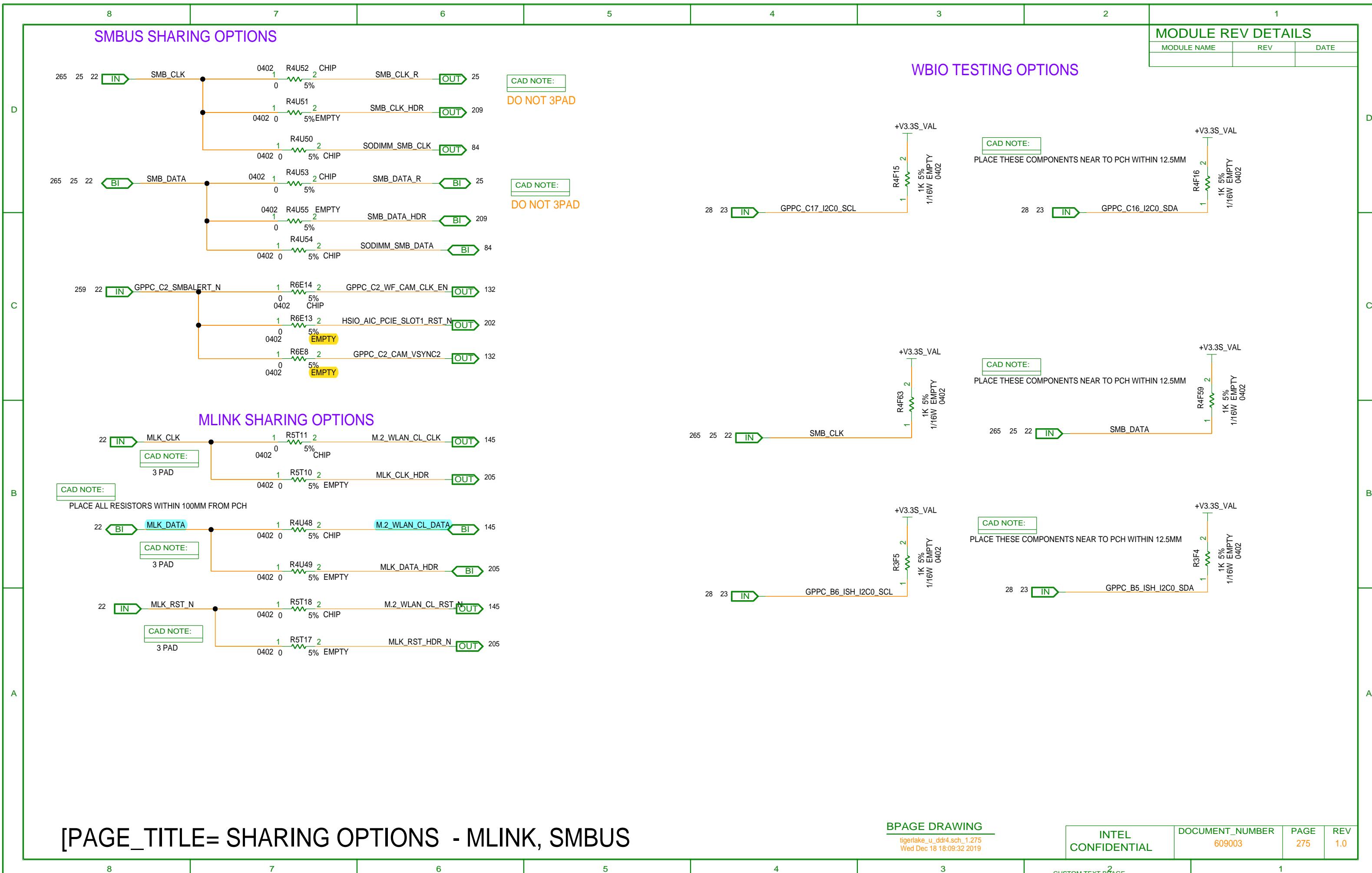


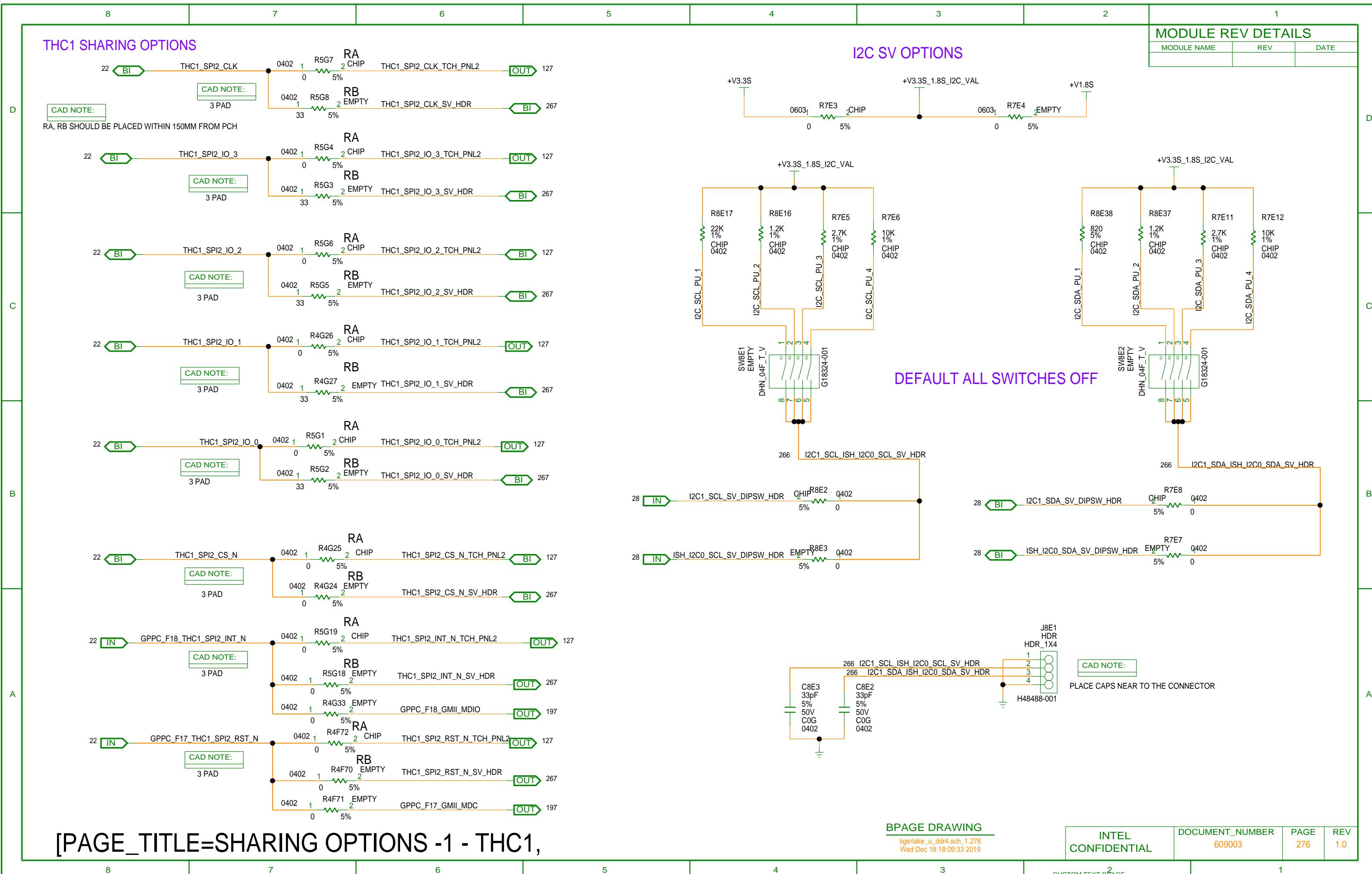












MODULE REV DETAILS		
MODULE NAME	REV	DATE

D

D

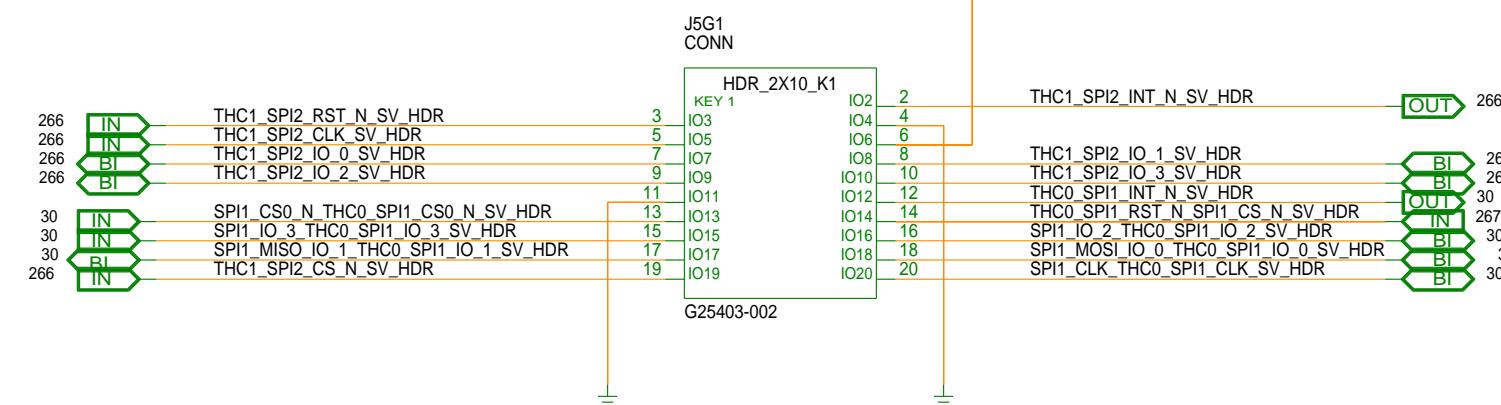
THC0 , THC1 AND SPI1 SV VALIDATION HEADER

DESIGN NOTE:

ONLY SINGLE LOAD IS SUPPORTED. 1.8V IO:RA=33E, 3.3V IO IS NOT POR AND NOT SUPPORTED
MAX CABLE LENGTH SUPPORTED IS 203MM

CAD NOTE:

PLACE RA CLOSE TO CONNECTOR WITHIN 25MM, FOR ALL SIGNALS
PLACE CONNECTOR WITHIN 250MM FROM PCH



DESIGN NOTE:

ON LKF, SPI1 CS1 AND THC0 RESET ARE MULTIPLEXED. HENCE SAME OPTION IS MAINTAINED VIA RESISTOR STUFFING REWORK ON TGL FOR UNIFICATION BETWEEN PLATFORMS

