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								MODULE REV DETAILS		
								MODULE NAME	REV	DATE
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c										
B									B	
A									A	
	[79. FLEX CONNECTOR] [80. MEMORY - DDR4 SODIMM CHANNEL -A (1 OF 2)] [81. MEMORY - DDR4 SODIMM CHANNEL -A (2 OF 2)] [82. MEMORY - DDR4 SODIMM CHANNEL -B (1 OF 2)] [83. MEMORY - DDR4 SODIMM CHANNEL -B (2 OF 2)] [84. MEMORY - DDR4 SODIMM CHANNEL -A PD BOM] [85. MEMORY - DDR4 SODIMM CHANNEL -BPD BOM] [86. MEMORY - DDR VREF CIRCUITRY -1 - PROCESSOR, OPTIONS] [87. MEMORY - DDR4 SODIMM & LPDIMM CONN PINOUT] [88. MEMORY - DDR VREF CIRCUITRY - 3 - AVMC OPTION] [89. DISPLAY - eDP connector 1 - CMC] [90. DISPLAY - eDP connector 1 - MISC] [91. DISPLAY - eDP connector 1] [92. DISPLAY - EDP CONNECTOR 2 - CMC]									
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c								
B								
A								

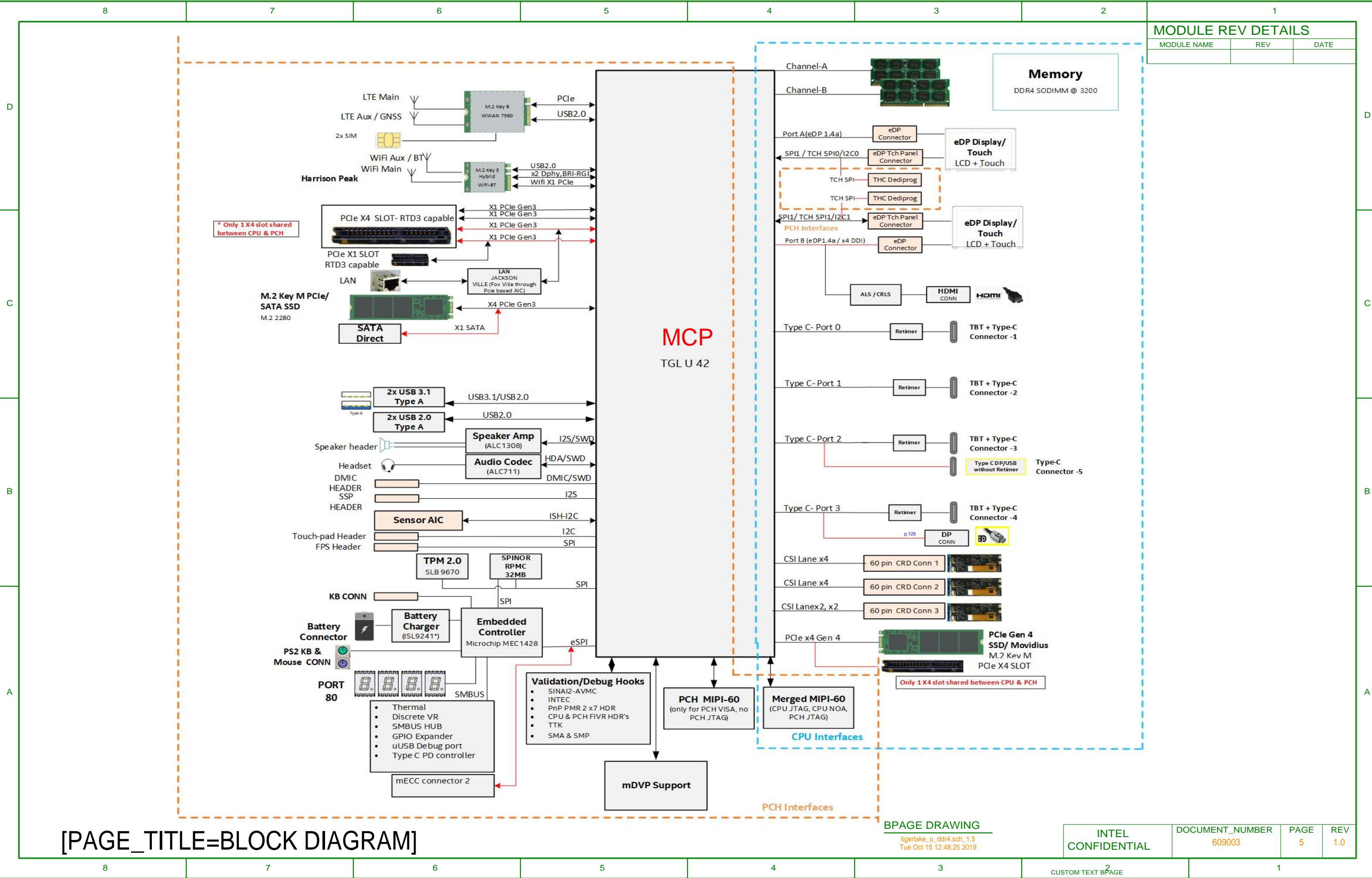
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	MODULE REV DETAILS							
	MODULE NAME	REV	DATE					
D	[190. EC - TPM HEADER FOR ESPI ONLY] [191. MECC CHROME SIGNALS] [192. EC - SERIAL DEBUG PORT] [193. EC - RESERVED -2] [194. UART TO USB PORT] [195. PM SIDEband HEADER] [196. RESERVED] [197. SYSTEM STATE LED CIRCUITRY] [198. PSS CIRCUIT - RFID CHIP] [199. PCIE SLOT - X4 RTD3] [200. PCIE SLOT - X4 SLOT] [201. PCIE SLOT -X4 SIGNAL BIFURCATION] [202. PCIE SLOT - X1 SLOT] [203. HSIO CONNECTOR (1 OF 4)] [204. HSIO CONNECTOR (2 OF 4)] [205. POWER HEADER FOR INTERPOSER] [206. GLITCH FREE CIRCUIT] [207. MLX HEADER] [208. IO - HEADERS - 1] [209. IO - HEADERS - GSPI AND SPI] [210. IO - HEADERS - 3] [211. IO - HEADERS - 4] [212. IO - HEADERS - 5] [213. INTEC THERMAL CONNECTOR]	[239. FAN_BOOST CONVERTER] [240. STANDARD AC BRICK - POWER SELECTION CIRCUITRY] [241. CONSUMER AND PROVIDER PATH SELECTION - PORT 0] [242. CONSUMER AND PROVIDER PATH SELECTION - PORT 1] [243. CONSUMER AND PROVIDER PATH SELECTION - PORT 2] [244. CONSUMER AND PROVIDER PATH SELECTION - PORT 3] [245. BUCK BOOST BATTERY CHARGER - POWER STAGE] [246. BATTERY CONNECTOR, BATFET AND USBC LDO IMPLEMENTATION] [247. EC_SLP_DS4, KBC_MUX AND ADAPTER PRESENT RAILS - ENABLE GENERATION] [248. 3.3V AND 5V RAILS - POWER CONVERSION] [249. V1.8A RAIL POWER CONVERSION] [250. POWER CONVERSION - VCCIN_AUX RAIL] [251. VNN & V1.05A BYPASS RAIL - POWER CONVERSION] [252. VDD2 AND VTT RAILS - POWER CONVERSION] [253. VPP (1.8V / 2.5V) RAIL - POWER CONVERSION] [254. IMVP9 CONTROLLER] [255. IMVP DRMOS PHASE 1 AND 2] [256. IMVP DRMOS PHASE 3] [257. A RAILS POWER GENERATION] [258. VCCST AND LAN RAILS POWER GENERATION] [259. VCCSTG AND VCCSFR_OC RAIL GENERATION] [260. 3.3S AND 1.8S RAIL GENERATION] [261. 1.2V RAIL FOR HDMI AND UFS, VBATA_A FOR HDA AND AUDIO POWER GENERATION] [262. TOUCH PANEL AND FINGER PRINT POWER SUPPLY GENERATION] [263. V5DX_SSD DIRECT CONNECT AND V3.3DX_SSD GENERATION] [264. EDP BACKLIGHT AND V3.3DX_DP_EMB RAILS GENERATION_1] [265. EDP BACKLIGHT AND V3.3DX_DP_EMB RAILS GENERATION_2] [266. 5V FAN RAIL, SLEEP SIGNAL V3.3S_ALS AND AUDIO CODEC RAIL GENERATION] [267. S0iX LED] [268. AUDIO POWER SUPPLY GENERATION] [269. SD POWER RAILS GENERATION] [270. V5S, V1.8U_2.5U_MEM AND VDDQ_CPU RAILS GENERATIO] [271. POWER MEASUREMENT RESISTORS] [272. CAMERA, WLAN AND WWAN POWER GENERATION] [273. POWER BUTTON, RTC AND SLP_SUS# CIRCUITRY] [274. POWER SEQUENCING LOGIC - PAGE I] [275. POWER SEQUENCING LOGIC - PAGE II] [276. RESET SWITCH, CHARGING LED AND SMC RST IMPLEMENTATION] [277. V5A AND 3.3A_PCH VAL RAILS] [278. PCIE SLOT1 AND V3.3A_VAL POWER RAIL GENERATION] [279. V3.3A_DSW_VAL AND PCIE VAL RAIL GENERATION] [280. U AND S VALIDATION RAILS] [281. PCIE SLOT 12V, 3.3V, V5_PS2 AND V3.3_KBC_SR RAIL GENERATION] [282. VAL RAILS FOR DPY 1.24 AND V1.05A_VAL] [283. V1.05A_VAL AND V0.85A_VAL_MAR RAIL GENERATION] [284. MOUNTING HOLES]	[285 PCH STRAPS 1] [286. PCH STRAPS 2] [287. PCH STRAPS 3] [288. PCH STRAPS 4] [289. PCH STRAPS 5] [300 TTK3 HEADER] [301 MLINK SHARING OPTIONS] [302 THC1 SHARING OPTIONS] [303 THC0]	D				
C								C
B	[223. POWER METER - EAC]							B
A								A
	[PAGE_TITLE=INDEX -3]							



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1

RefDes	LED Description
DS4G1	V1P05_CTRL
DS4G2	VNN_CTRL
DS8H5	S3 STATE
DS8H3	S4 STATE
DS8H4	S5 STATE
DS8H2	DSW STATE
DS8H1	M0/M3 STATE
DS3H1	ME PWR Gate

RefDes	LED Description
DS8H6	CAPS LOCK
DS8H7	NUM LOCK
DS7G1	POWER BUTTON
DS7H1	BAT STATUS LED

RefDes	LED Description
DS8G6	SLP S0 LED
DS8G4	PWRGD
DS8G5	CATERR
DS6G1	C10 GATE
DS6G2	CS INDICATE

RefDes	LED Description
DS9B1	SATA Direct connect DEVSLP
DS9E1	M.2 SSD DEVSLP
DS8G7	SATA ACTIVITY
DS6D1	PCIE LINK DOWN
DS4G4	WLAN
DS4G3	BT
DS7D1	WWAN

Error Type	Error Code	Caps Lock LED (DS9H2)	Scroll Lock LED (DS7G1)	Num Lock LED (DS9J1)
No Error	0	Off	Off	Off
RSMRST_PWRGD_N	1	Off	Off	Flash
PM_SLP_S5_N	2	Off	Flash	Off
PM_SLP_S4_N	3	Off	Flash	Flash
PM_SLP_S3_N	4	Flash	Off	Off
PM_SLP_M_N	5	Flash	Off	Flash
ALL_SYS_PWRGD	6	Flash	Flash	Off
PLT_RST_N	7	Flash	Flash	Flash
DOCK_SYS_PWRGD_N	8	On	On	Flash
SUSWARNB	9	On	Flash	On

Note: KSC Thermal Shutdown is indicated by flashing of Num_Lock and Caps_Lock LEDs alternatively.
DS7G1 acts as led indication for error code in case of any error otherwise works as power button LED

[PAGE_TITLE= LED DISCRIPTION]

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D		MODULE NAME		REV		DATE	
C							
B							
A							
Interface	WHL	TGL					
Board ID							
PCIE Gen4 – DEKEL PHY	No		Yes				
TYPE C	No		Yes				
XTAL_IN	24MHz		38.4MHz				
Memory	1 Channel		2 channel				
CSI	No		Yes				
No.	Changes	WHL	TGL	Status			
1	XXDP_COMP	24.9 ohm PU to VCCIO	24.9 ohm PU to VCCIN /+VCC1P05_OUT_FET (default) on extra added pin on one of the spare pins of TGL_A0.	implemented			
2	XXDDR_COMP[0]	121 ohm PD	121 ohm PD on Pin DW 49	implemented			
3	XXDDR_COMP[1]	80.6 ohm PD	80.6 ohm PD on pin DW47	implemented			
STRAP							
4	SVID DISABLE STRAP	J3B1 to 1-2	J3B1 to 1-X				
5	GPPC_F10	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K				
6	GPPC_F0*	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K				

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							MODULE REV DETAILS			
							MODULE NAME REV DATE			
TGL-U 42 ROW RVP's Mphy Allocation										
PCIe Controller		Lane #	Flex IO		HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 3 (SV SKU)			
x4 Controller 1		Lane 0	PCIE3_1_USB31_1							
		Lane 1	PCIE3_2_USB31_2							
		Lane 2	PCIE3_3_USB31_3							
		Lane 3	PCIE3_4_USB31_4							
x4 Controller 2		Lane 4	PCIE3_5		Lane 0 for x4 PCIe slot		x4 PCIe Slot			
		Lane 5	PCIE3_6		Lane 1 for x4 PCIe slot					
		Lane 6	PCIE3_7_LAN_0A_UFS_00		Jacksonville Gbe LAN					
		Lane 7	PCIE3_8_LAN_0B_UFS_01		x1 PCIe Slot					
x4 Controller 3		Lane 8	PCIE3_9_LAN_0C_UFS_1_00		M.2 Key M x4 SSD(Lane reversal for x4 PCIe)	SATA Direct Connect	HSIO Connector			
		Lane 9	PCIE3_10_UFS_1_01							
		Lane 10	PCIE3_11_SATA_0							
		Lane 11	PCIE3_12_SATA_1							
x4 Controller 4 (Gen 4 North side)		CPU Lane0	CPU_PCIE_0		M.2 Key M x4 SSD	x4 PCIe Slot				
		CPU Lane1	CPU_PCIE_1							
		CPU Lane2	CPU_PCIE_2							
		CPU Lane3	CPU_PCIE_3							

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

IC name	ALC711 ES-1	ALC711 ES-2
package	QFN-48	QFN-48
Bilingual mode(HD-A/SdW)	O	O
Combo jack (HP+MIC2) + Line1	O	O
Line2 (In) port	O	O
SdW Master I/F	O	O
SdW Slave I/F	O	O
Line1(in)/Line2(in)	O	O
VAD energy detector	X	O
VAD buffer(64KB) with SRAM controller	X	O
USB type-c switch and analog switch	X	O
DMIC	2ch	2ch
HP JD type	JD port	Decide by AGPI and CC1/CC2 status
Power strap	Slew rate(MSB)	Slew rate/self-time turn off/SdW slave ID
GPIO2	X	O
LDO4	X	O
LINE2-VREFO	X	O

[PAGE_TITLE - ALC711 ES1 vs ES2]

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

D	RefDes	Jumper Description	Default
	J1A3	MIPI60 OVERRIDE N	'1-X'
	J2H3	MIPI60 PRESENT1 N	'1-X'
	J1C1	TYPEC DISABLE	'1-X'
	J1F3	NO REBOOT STRAP	'1-X'
	J1F4	FLASH DESCRIPTOR SECURITY OVERRIDE STRAP	'1-X'
c	J3B1	SVID DISABLE STRAP	'1-X'
	J1F4	A0 PERSONALITY STRAP	'1-X'
	J3H1	DDI3 HPD	'1-X'
	J9J5	BT RF KILL N, WIFI RF KILL N	'1-X,3-X'
	J9J4	CNVI Disable	'1-2'
	J5U1	TOUCH PANEL POWER SUPPLY GENERATION	'1-2'
	J8J3	PROCHOT EC JPR	'1-X'
	J9J3	SMC_RST_N JPR	'1-X'
	J9J2	SMC_LID JPR	'1-X'
	J8D2	SVID CLOCK	'1-2,3-X'
	J8D3	SVID ALERT	'1-2,3-X'
	J8D4	SVID DATA	'1-2,3-X'
	J8G3	PCH GLITCH ISSUE MITIGATION	'1-X'
	J7G1	SRTC/RTC CLEAR CMOS JPR	'1-X'
	J7H2	SPD_PRSNT JPR	'1-2'
	J8H3	FRU SMB CLK S3	'1-2'
	J8H5	FRU SMB DATA S3	'1-2'
	J6J1	PECI_MUX_CTRL_SNI_R	'1-X'
	J8J1	FRU POWER SUPPLY	'1-2'
	J6G4	H_PECI_CPU JPR	'1-X'

D	RefDes	Jumper Description	Default
	SW4V1	MIPI60 FN[0:3]	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
c	SW5V1	1 - VDDQ_VR_PWRGD - IMVP_VR_EN 2 - ALL_SYS_PWRGD - IMVP_VR_EN 3 - SATAXPCIE_0_SATAGP_0_R 4 - BIOS_REC	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
	SW6J2	1 - EC_SHD_CS_SW 2 - NC 3 - RETIMER_BYPASS_STRAP 4 - ESPI_TESTCRD_DET	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
	SW9C1	1 - BUF_PLT_RST_1.8 - WF_CAM_RST_N 2 - WF_CAM_RST_ND - WF_CAM_RST_N 3 +V1.8A - XTAL_SEL1_J 4 +V3.3A - XTAL_IN_J	1-8(OFF); 2-7(ON); 3-6(OFF); 4-5(OFF)
	SW8W1	1 - PNP_NPNP_SKU 2 - VIRTUAL_DOCK_DET_N 3 - VIRTUAL_BATTERY 4 - FLIP_TO_TABLET_MODE	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)

[PAGE_TITLE=JUMPER/SWITCH SETTINGS]

MODULE REV DETAILS

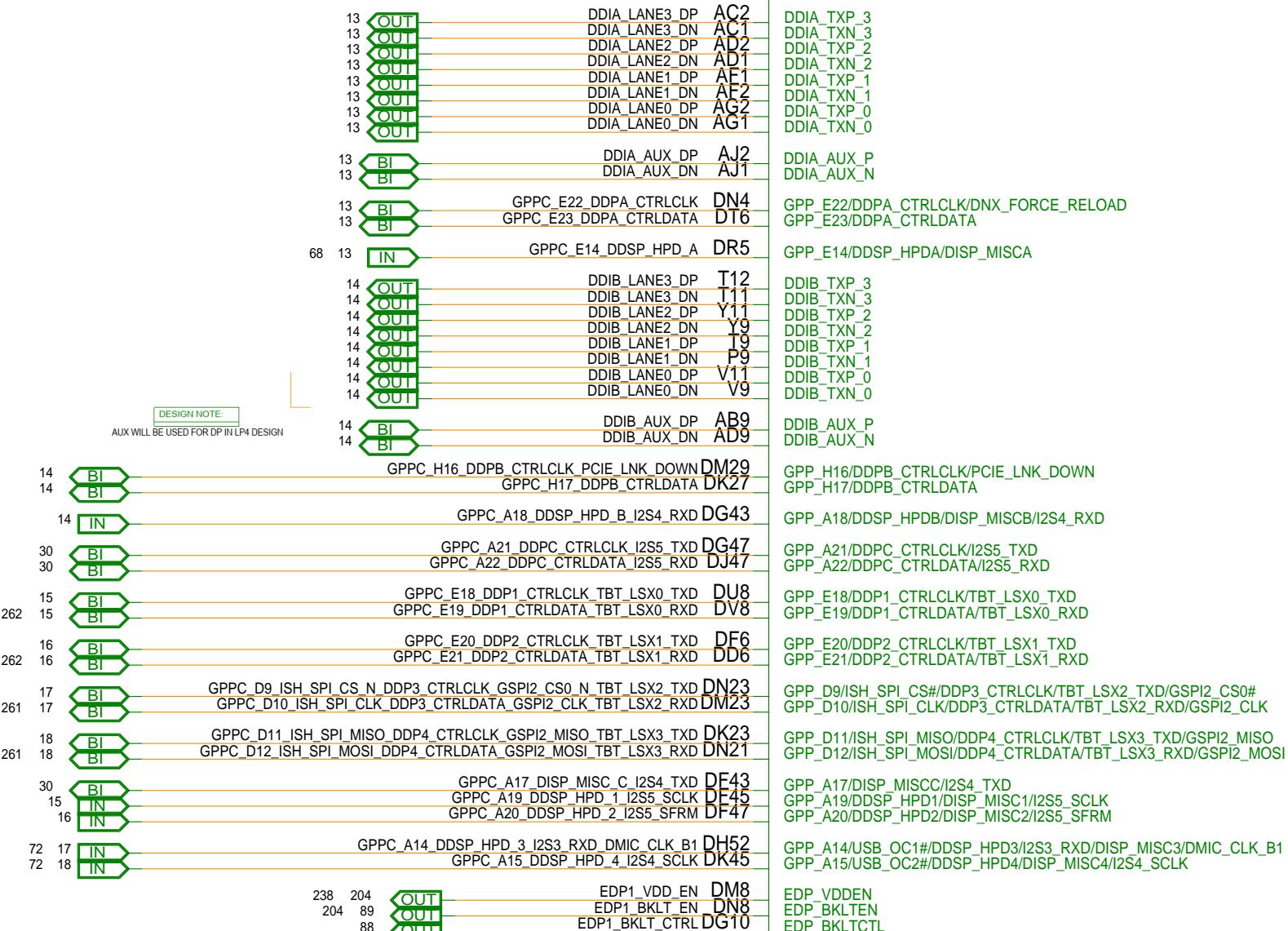
MODULE NAME	REV	DATE

D

D

U4E1
SOC1.6
BGA
TGL_UP3_IP_EXT

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DESIGN NOTE:
AUX WILL BE USED FOR DP IN LP4 DESIGN

DESIGN NOTE:

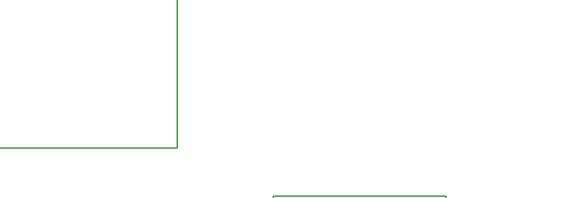
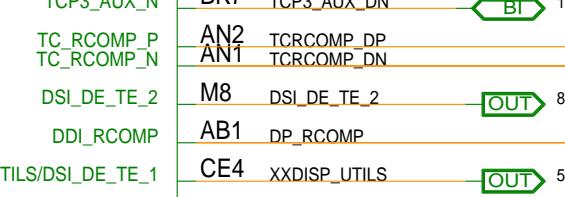
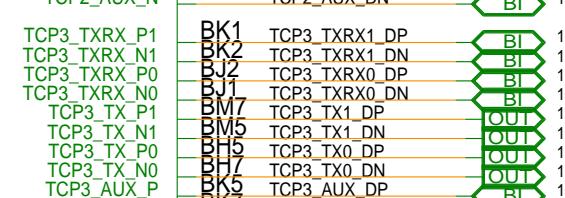
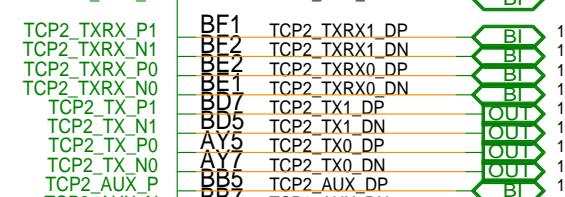
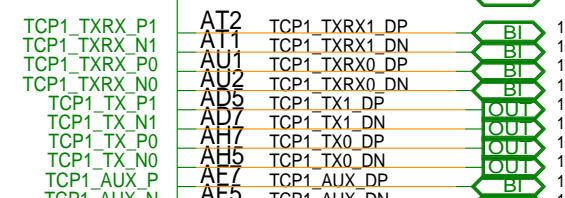
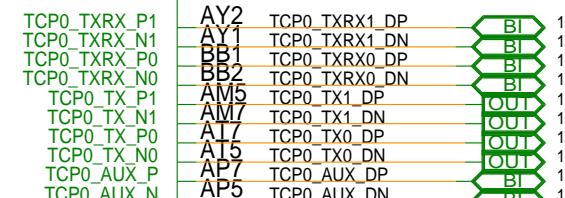
LSX_A:LSX TXD, LSX_B:LSX RXD

DESIGN NOTE:

LSX_A:BSSB RXD, LSX_B:BSSB TXD

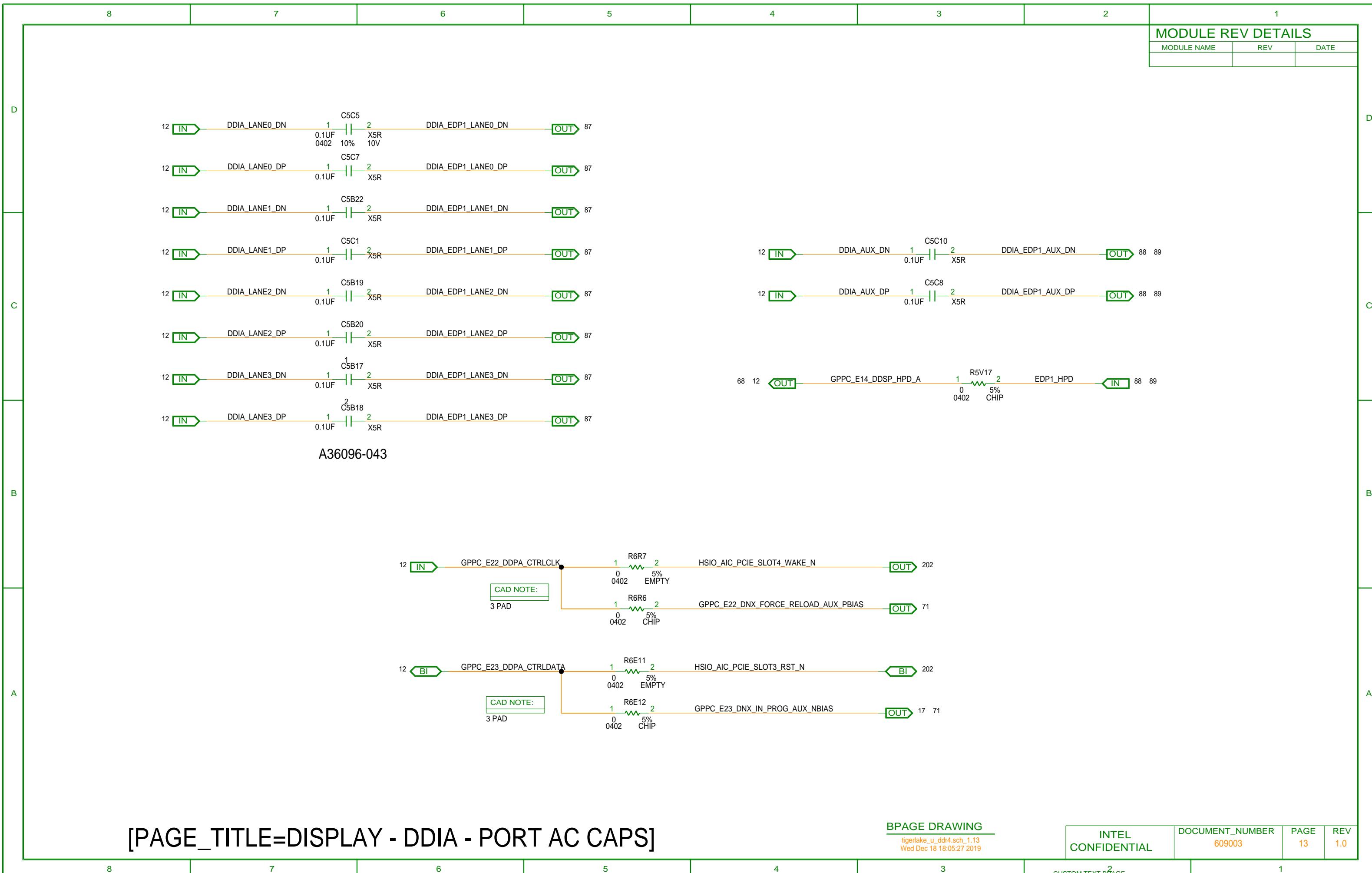
LPID6529

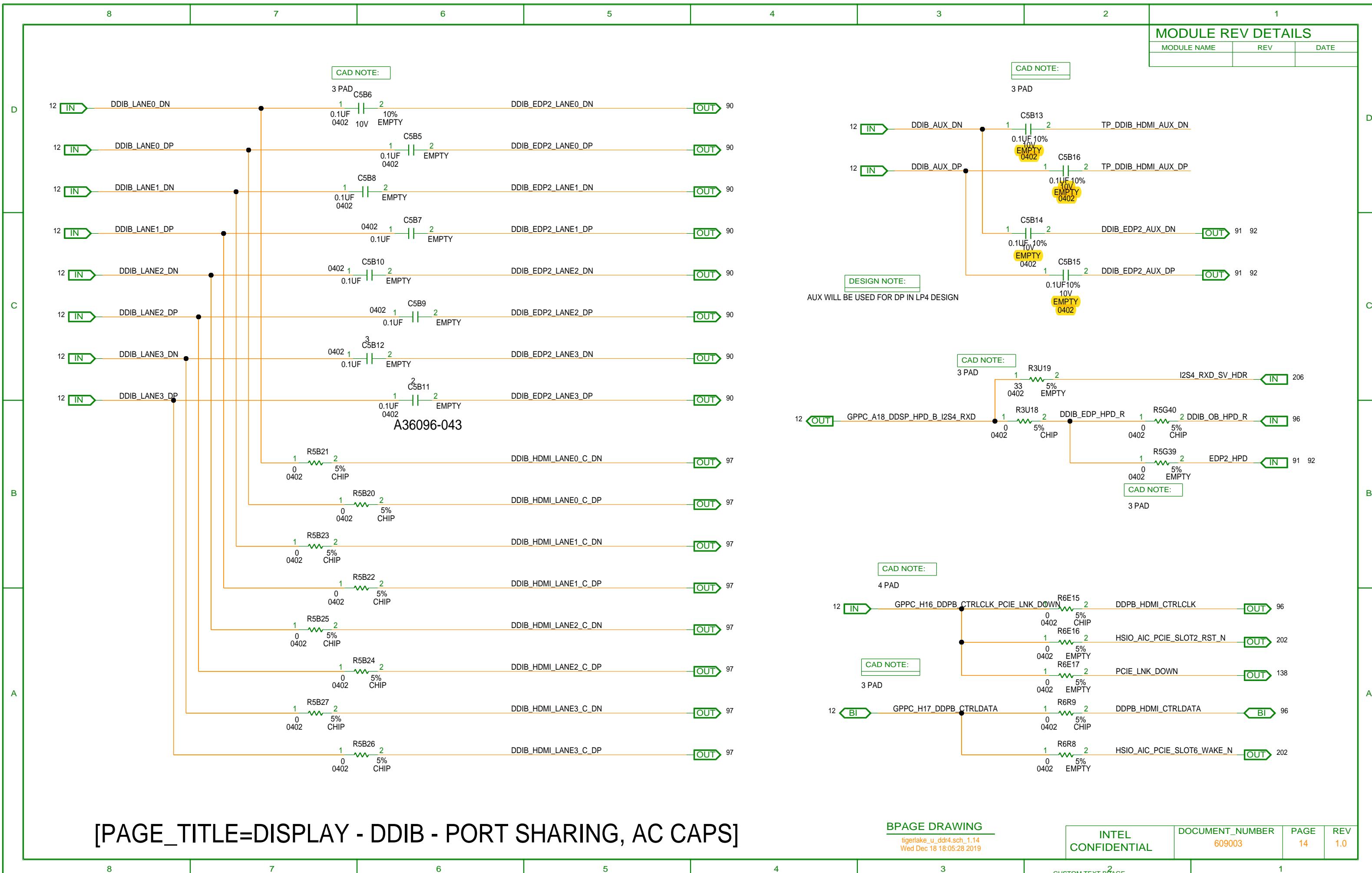
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

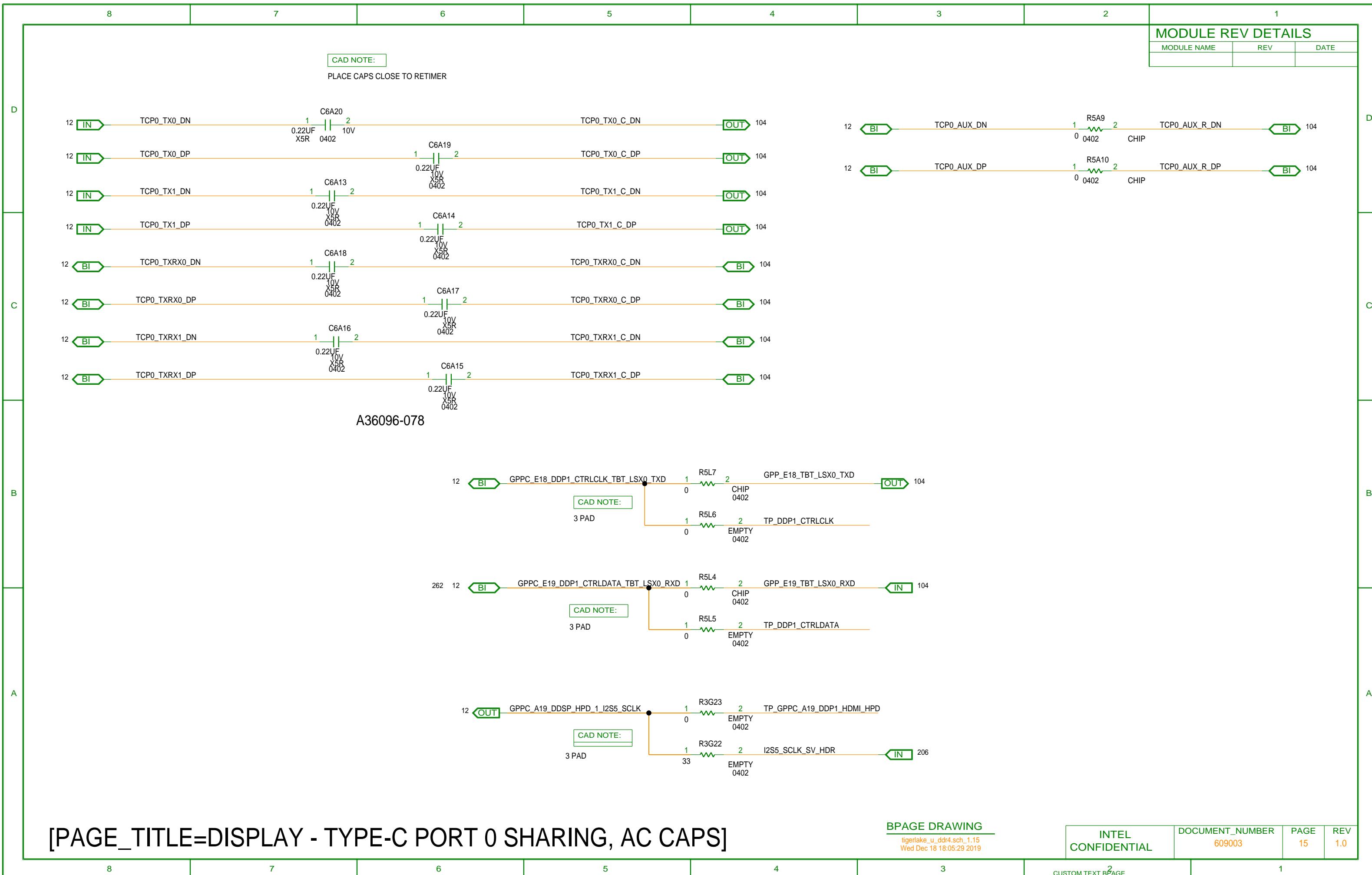


DESIGN NOTE:

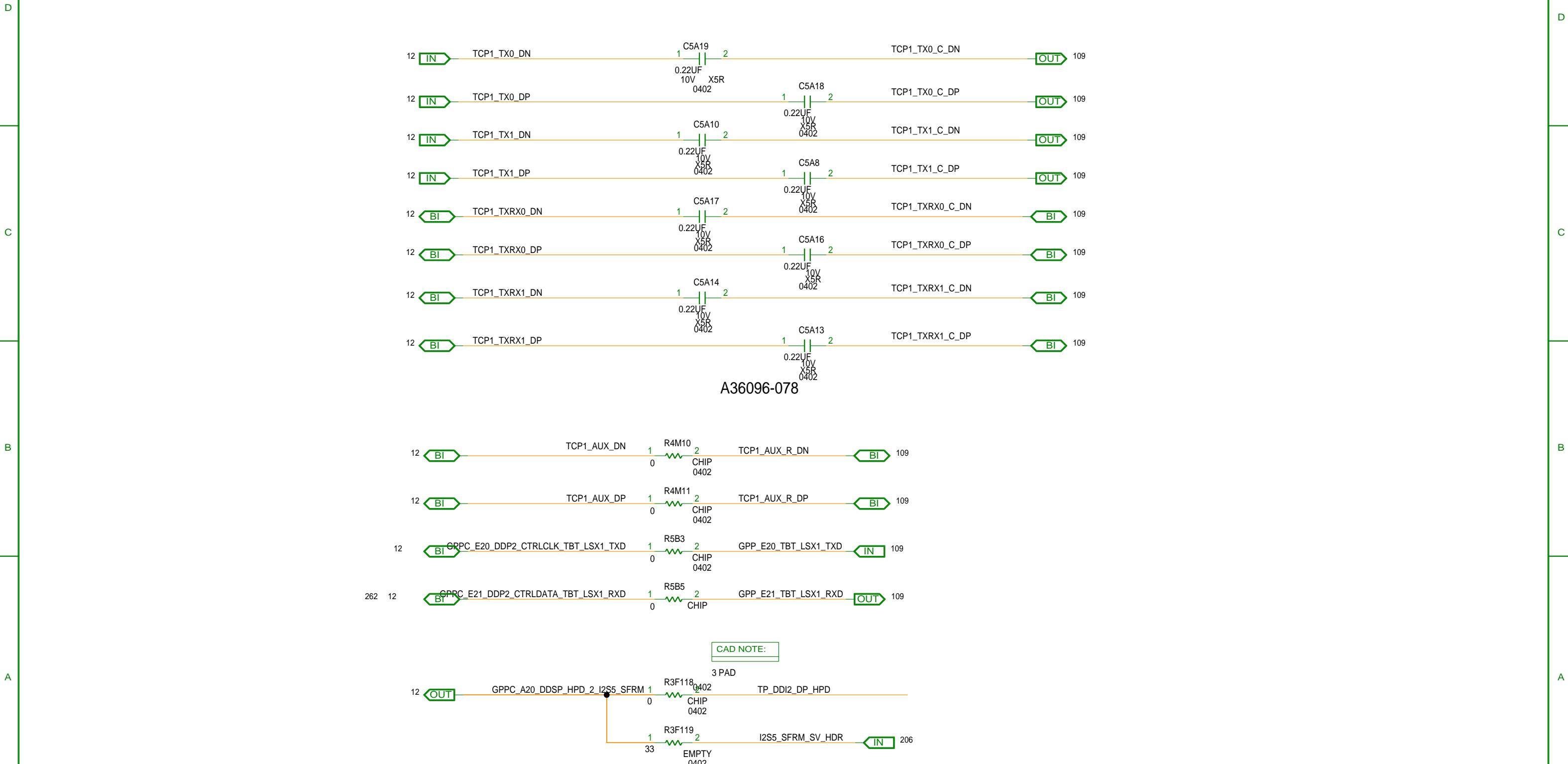
GPPC_A17=VDDEN, GPPC_A21=BKLT_EN & GPPC_A22=BKLT_CTRL







8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				



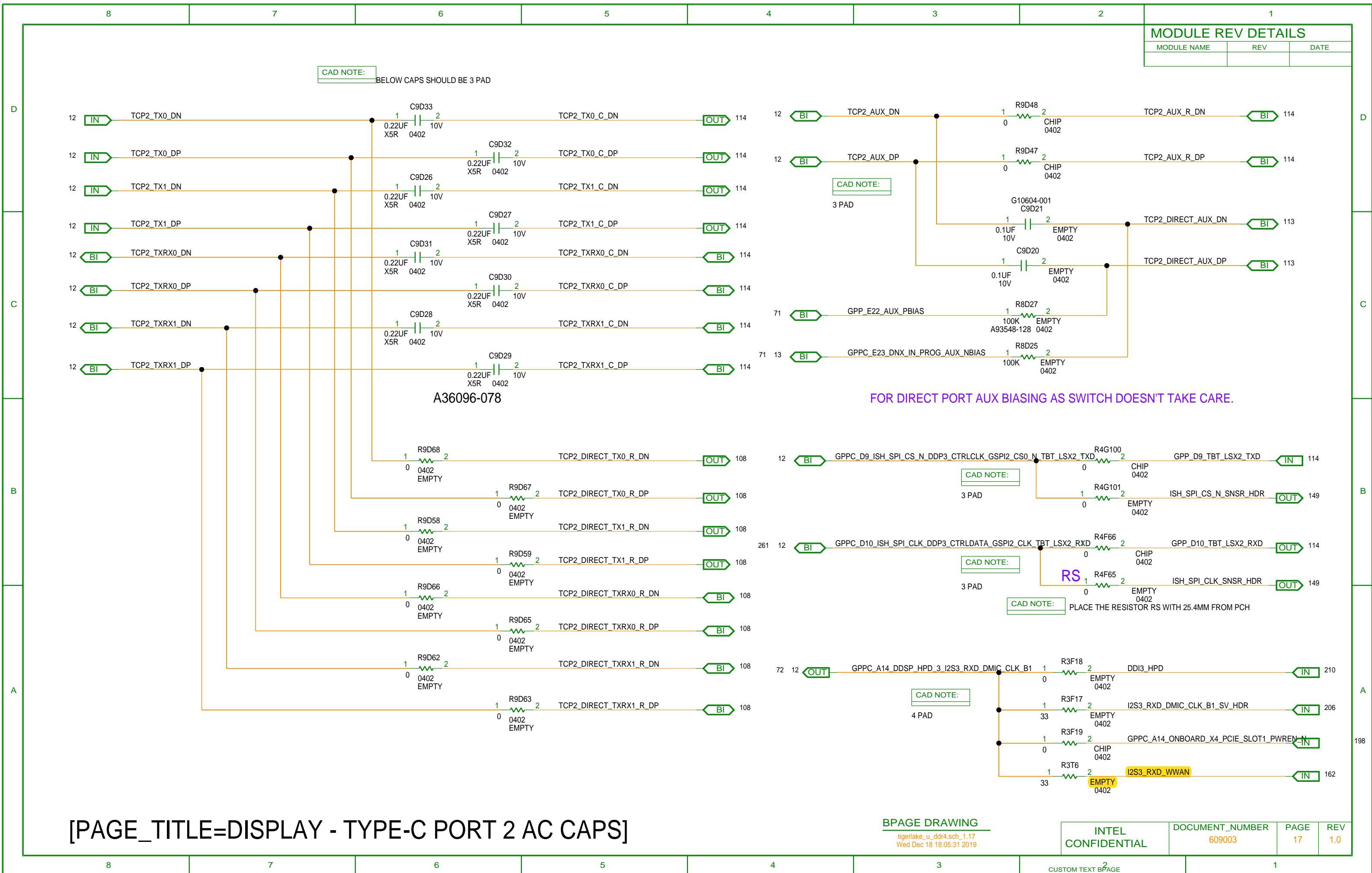
[PAGE_TITLE=DISPLAY - TYPE-C PORT 1 AC CAPS]

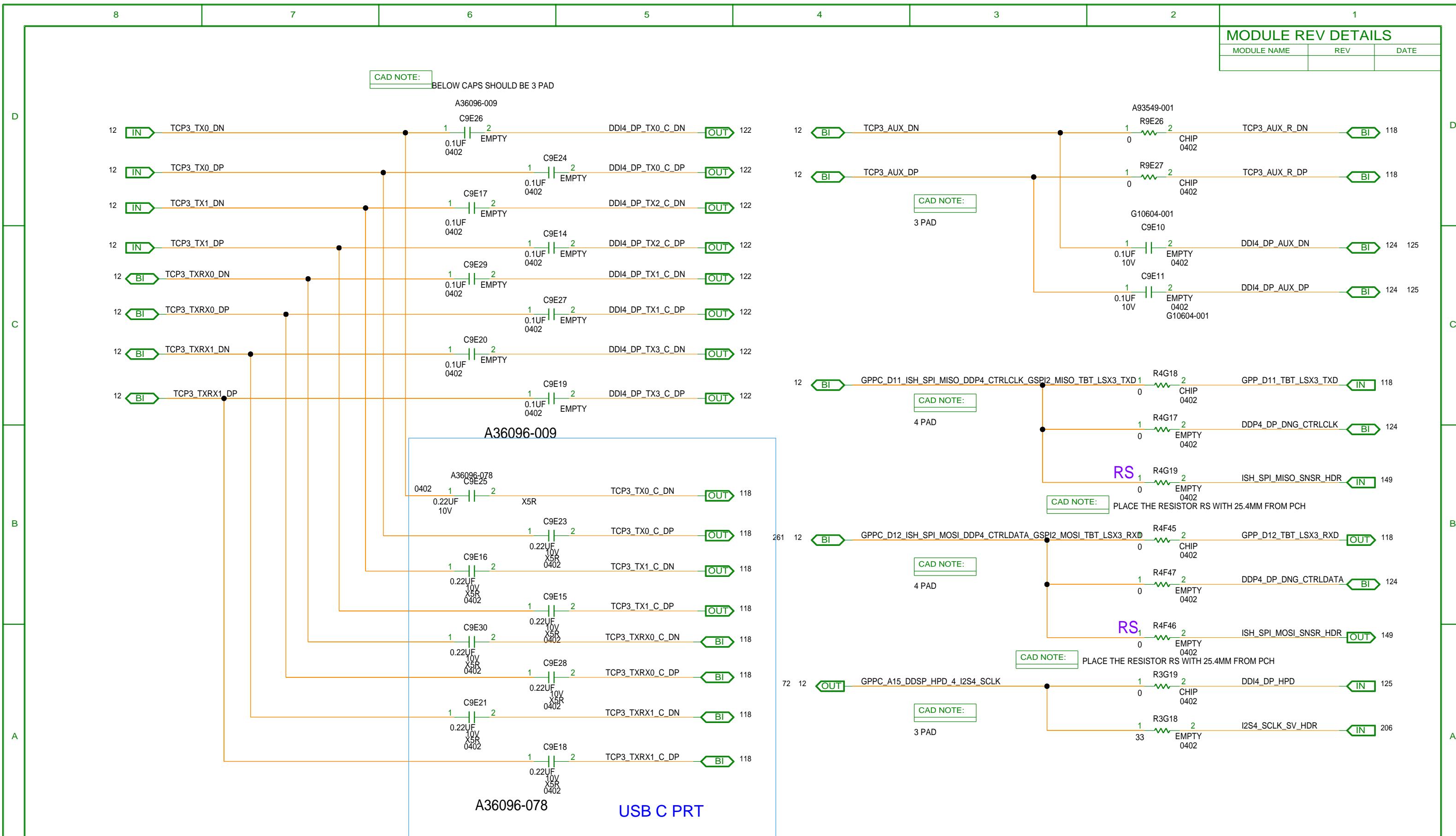
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Wed Dec 18 18:05:30 2019

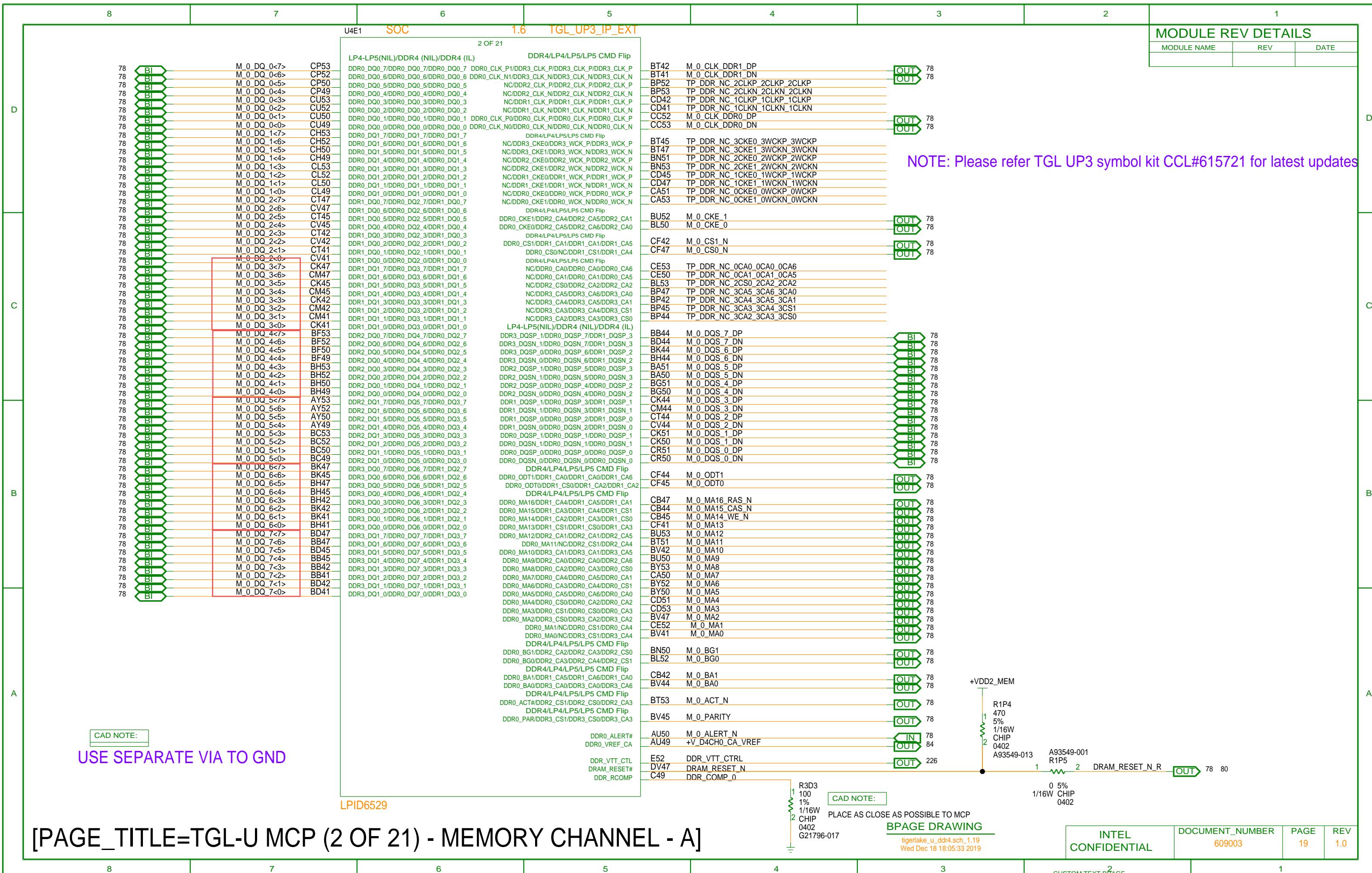
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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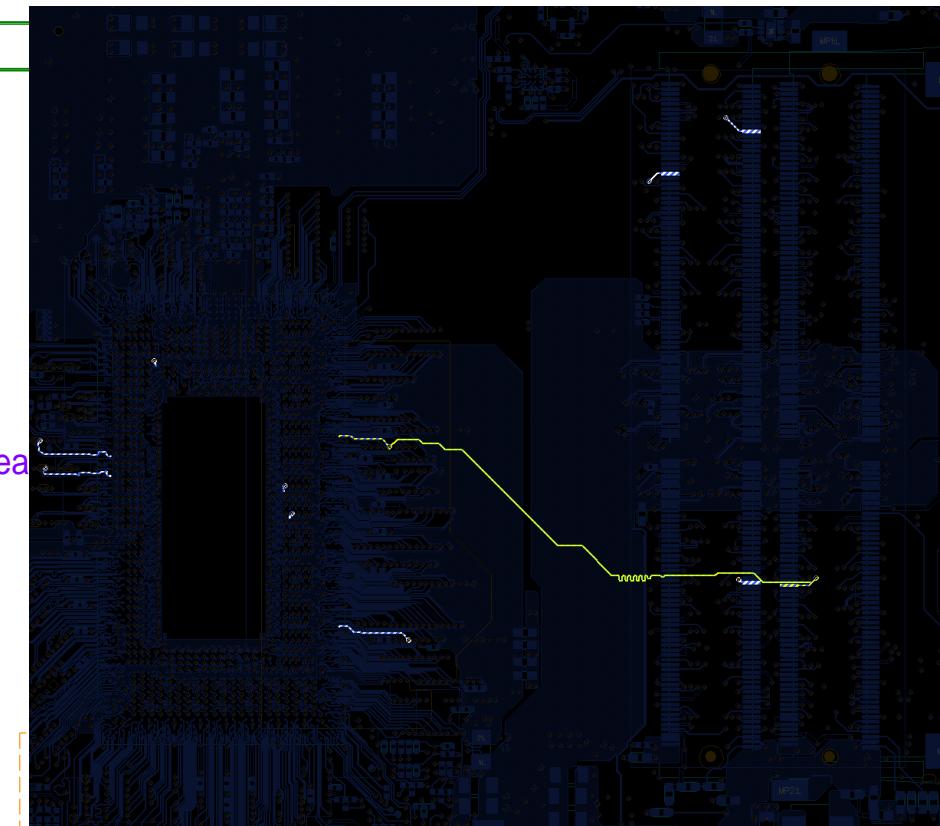
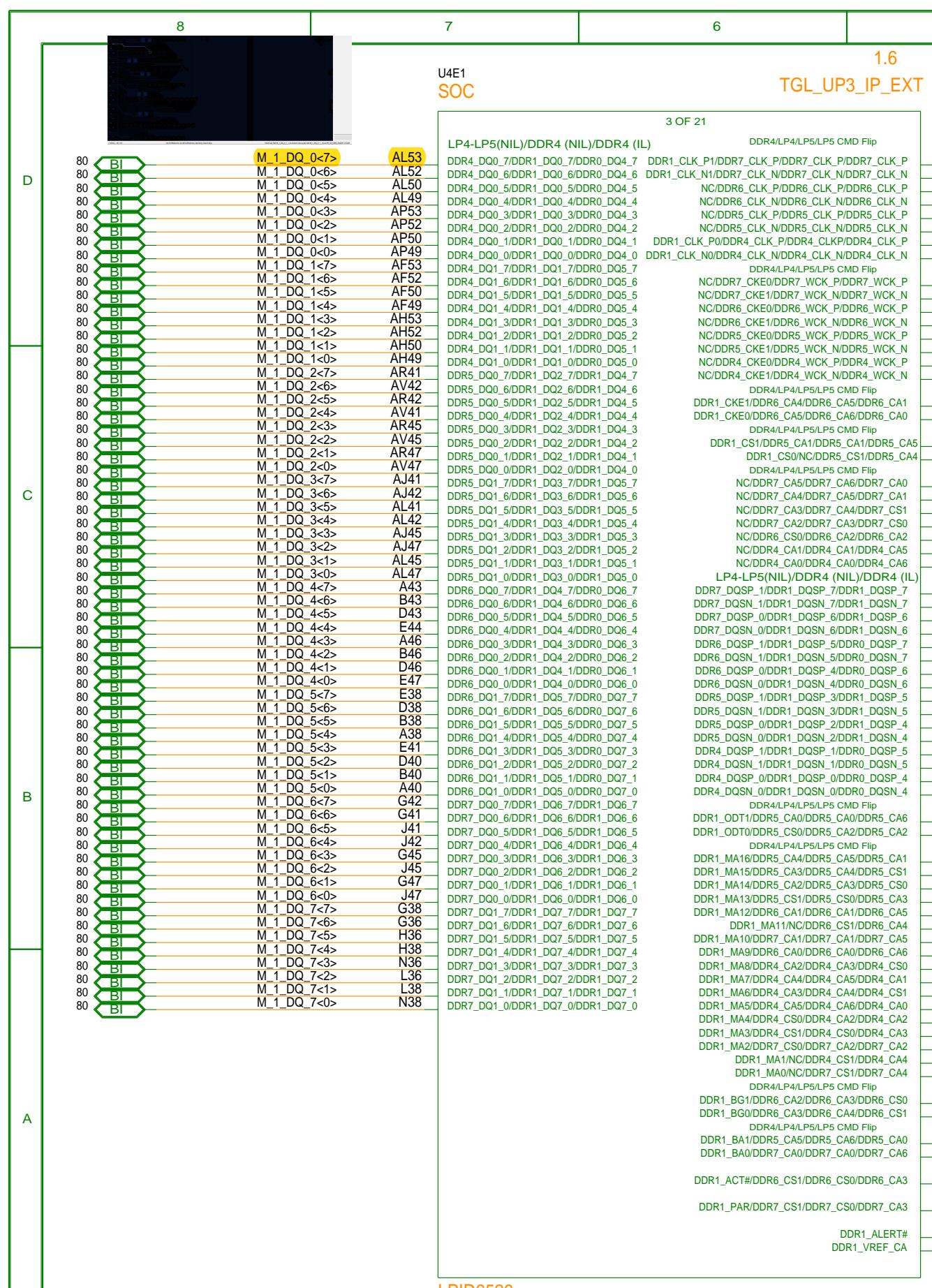
CUSTOM TEXT BPAGE

8	7	6	5	4	3	2	1
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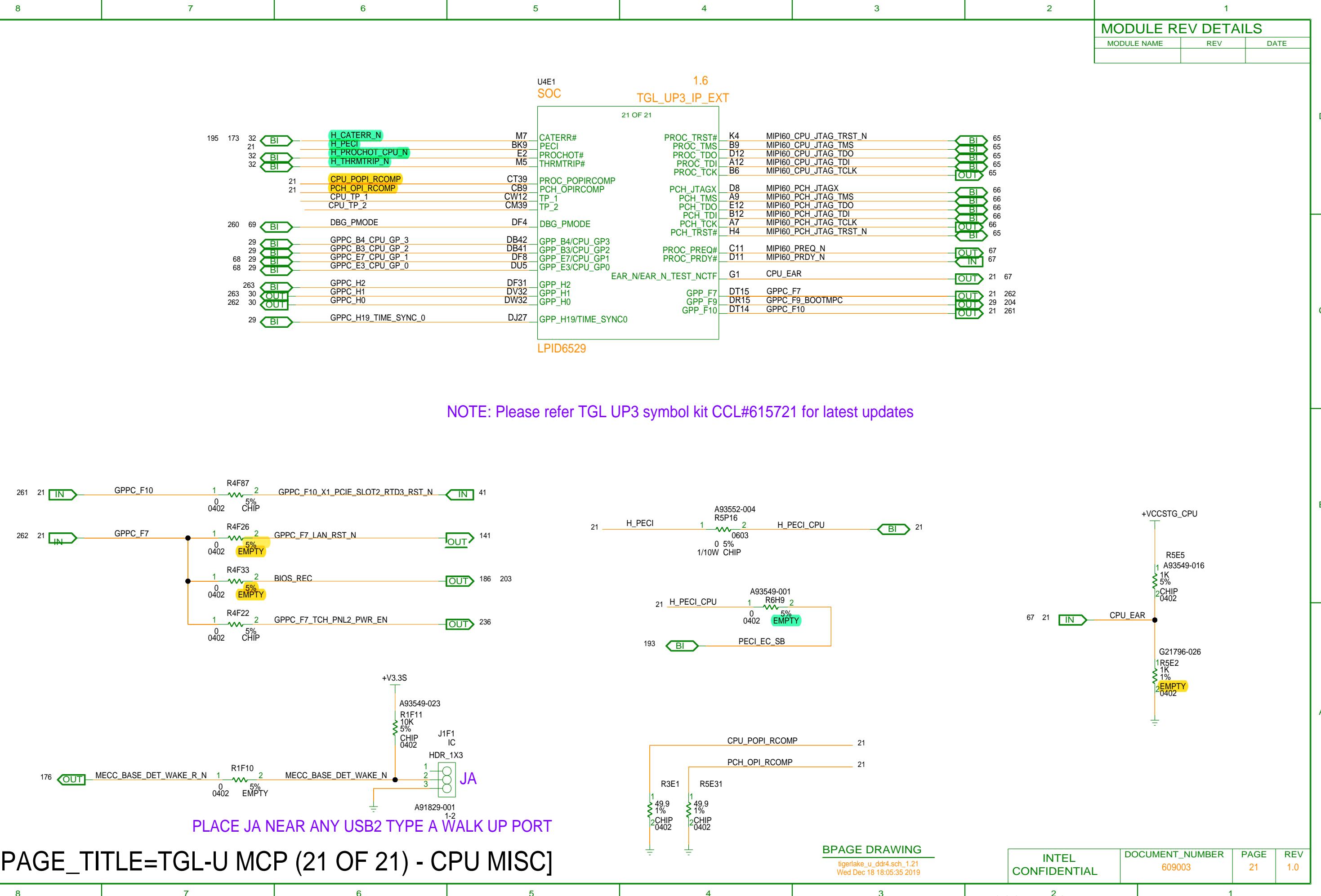


NOTE: Plea

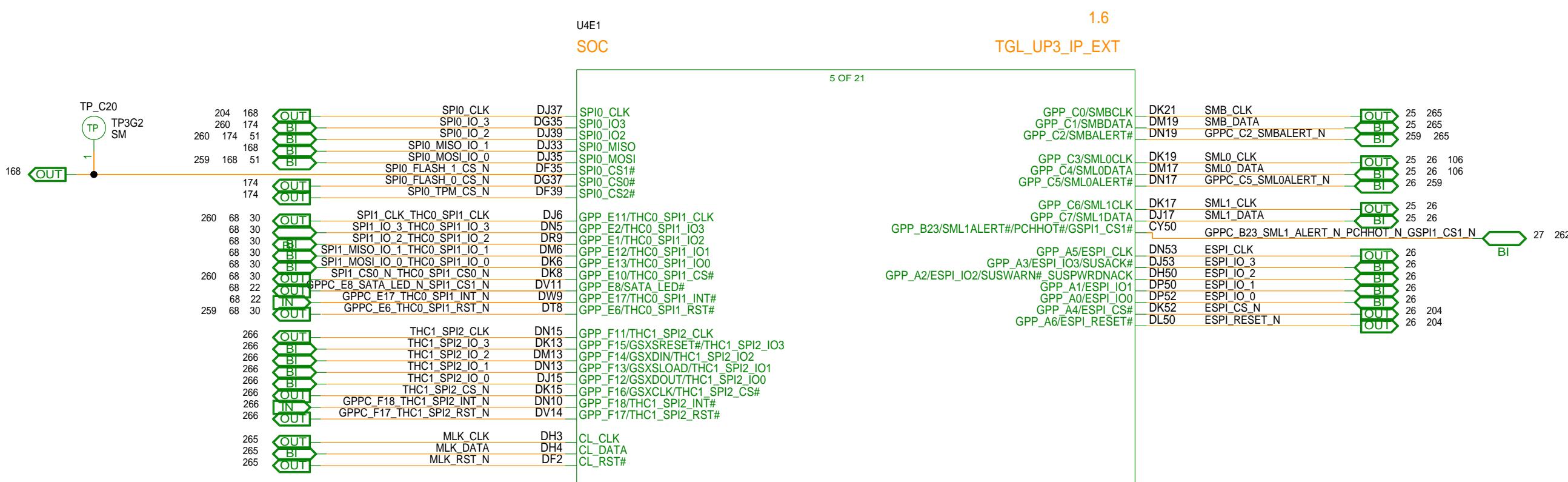
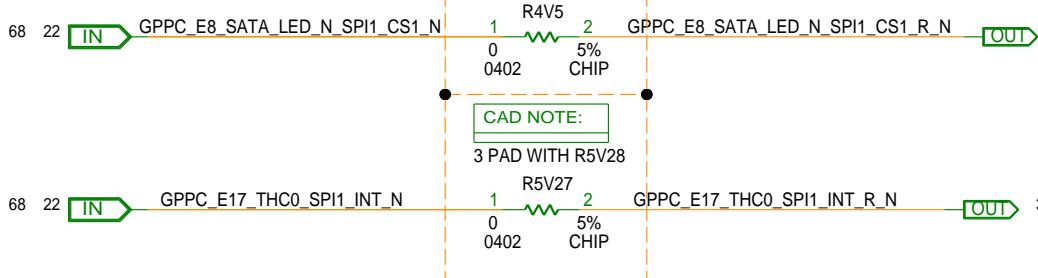
1.6 **U4E1**
TGL_UP3_IP_EXT **SOC**

4 OF 21
RSVD_2 DV24 RSVD_3 DW47 RSVD_4 DW49 RSVD_5 A48

LPID6529



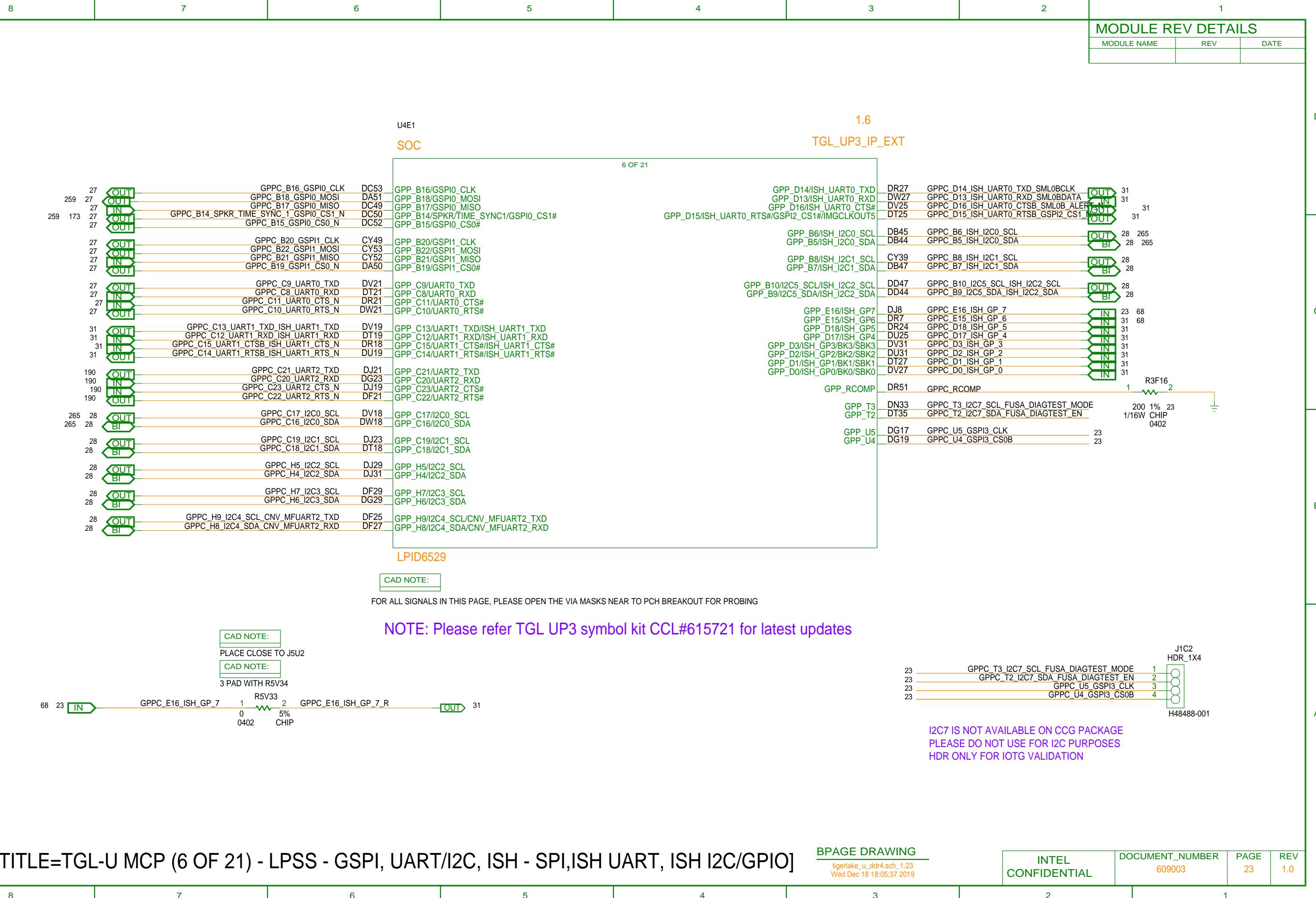
8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

CAD NOTE:
PLACE CLOSE TO J5U2CAD NOTE:
3 PAD WITH R4V4CAD NOTE:
FOR ALL SIGNALS IN THIS PAGE, PLEASE OPEN THE VIA MASKS NEAR TO PCH BREAKOUT FOR PROBING

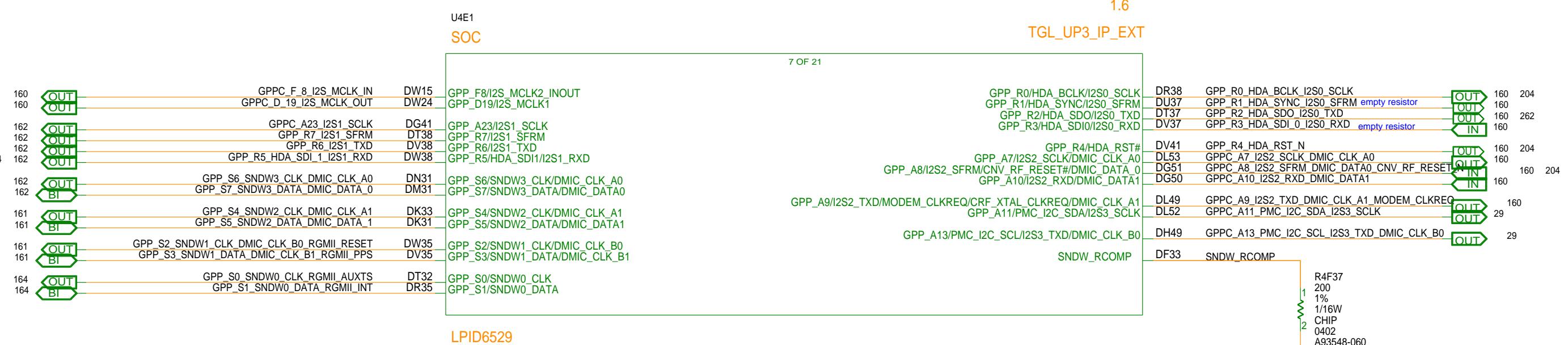
[PAGE_TITLE=TGL-U MCP (5 OF 21) - LSIO - SPI, ESPI, THC, MLINK, SMLINK, SMBUS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.22
Wed Dec 18 18:05:36 2019

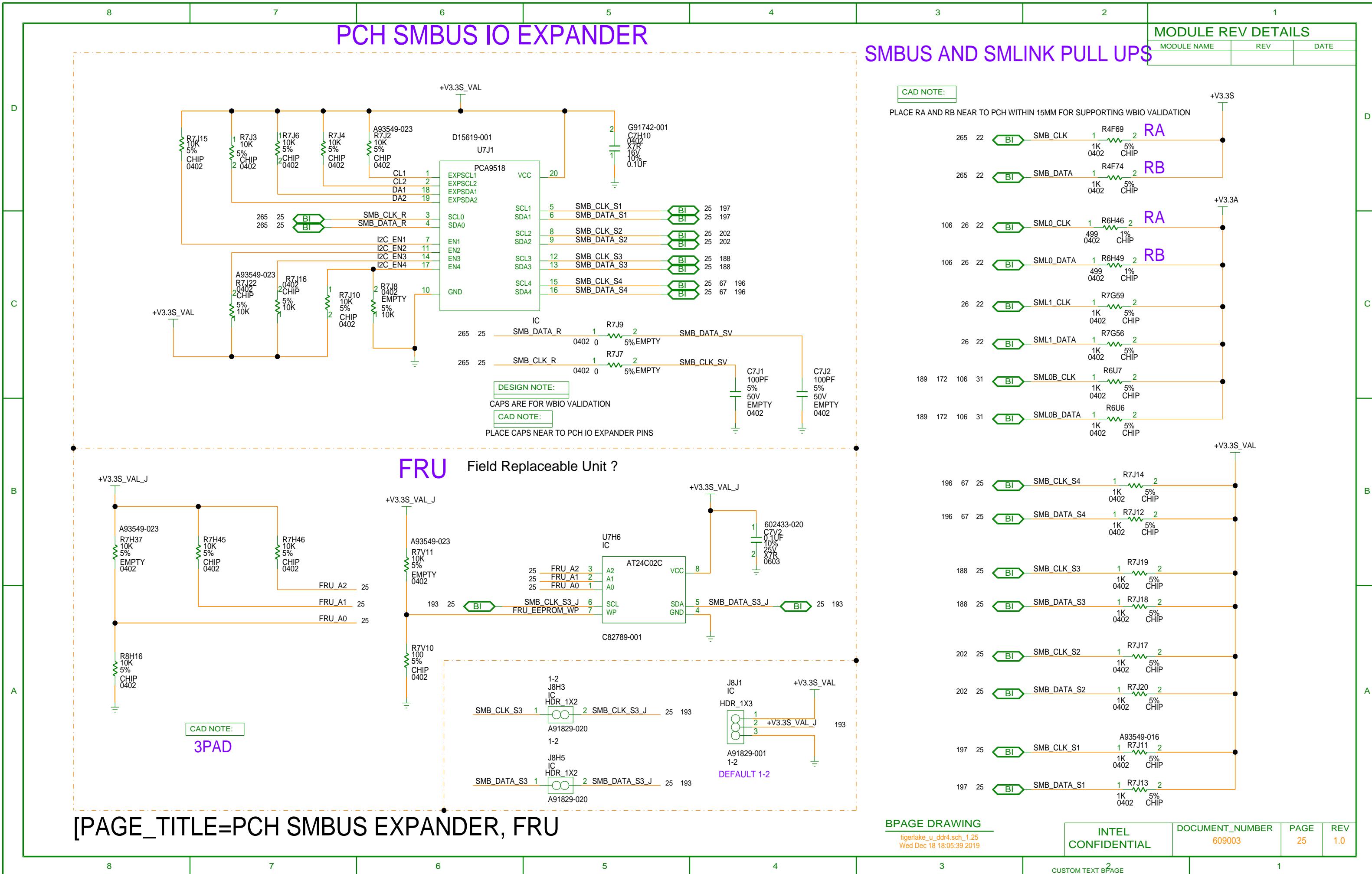
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	22	1.0	

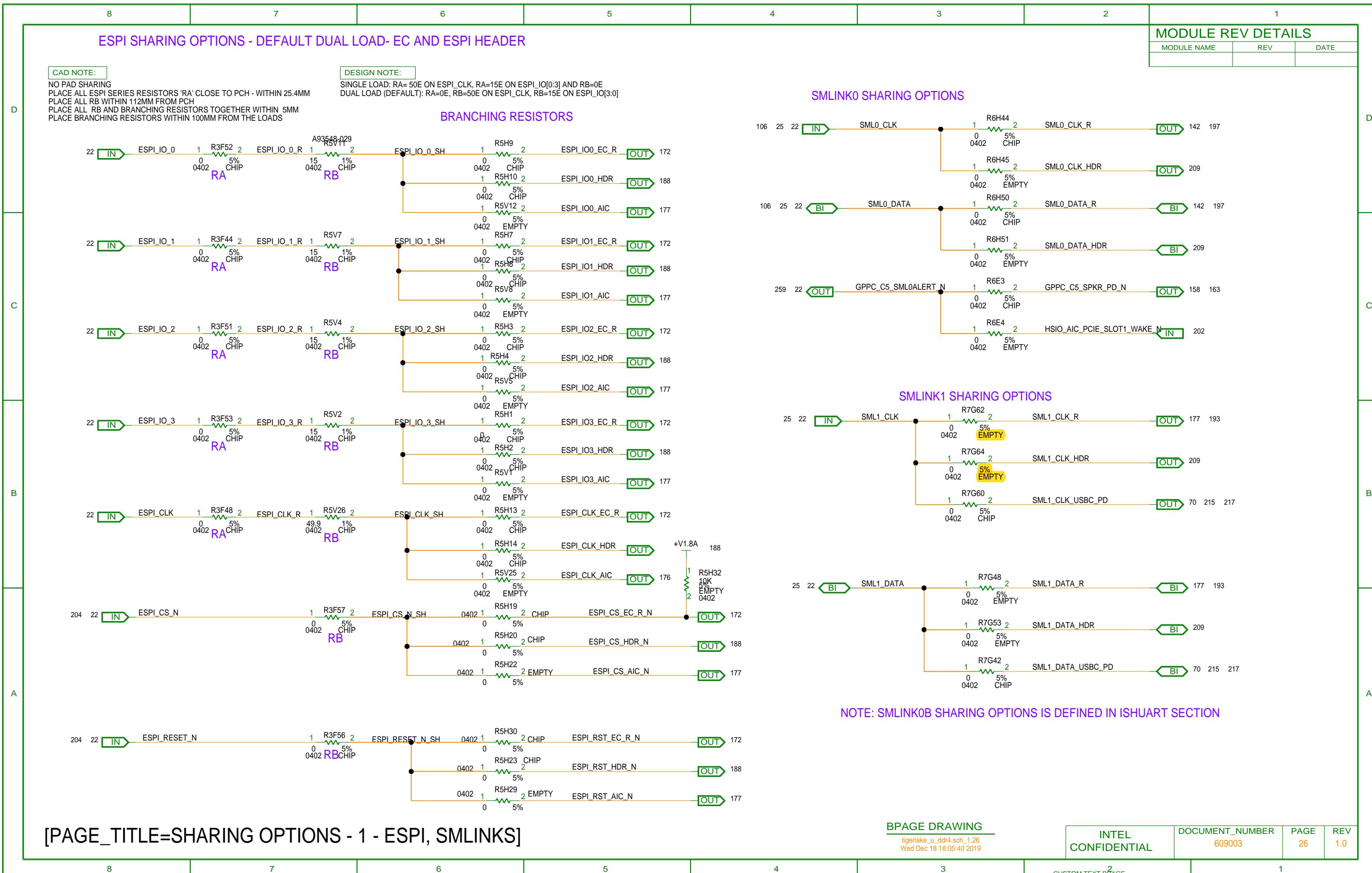


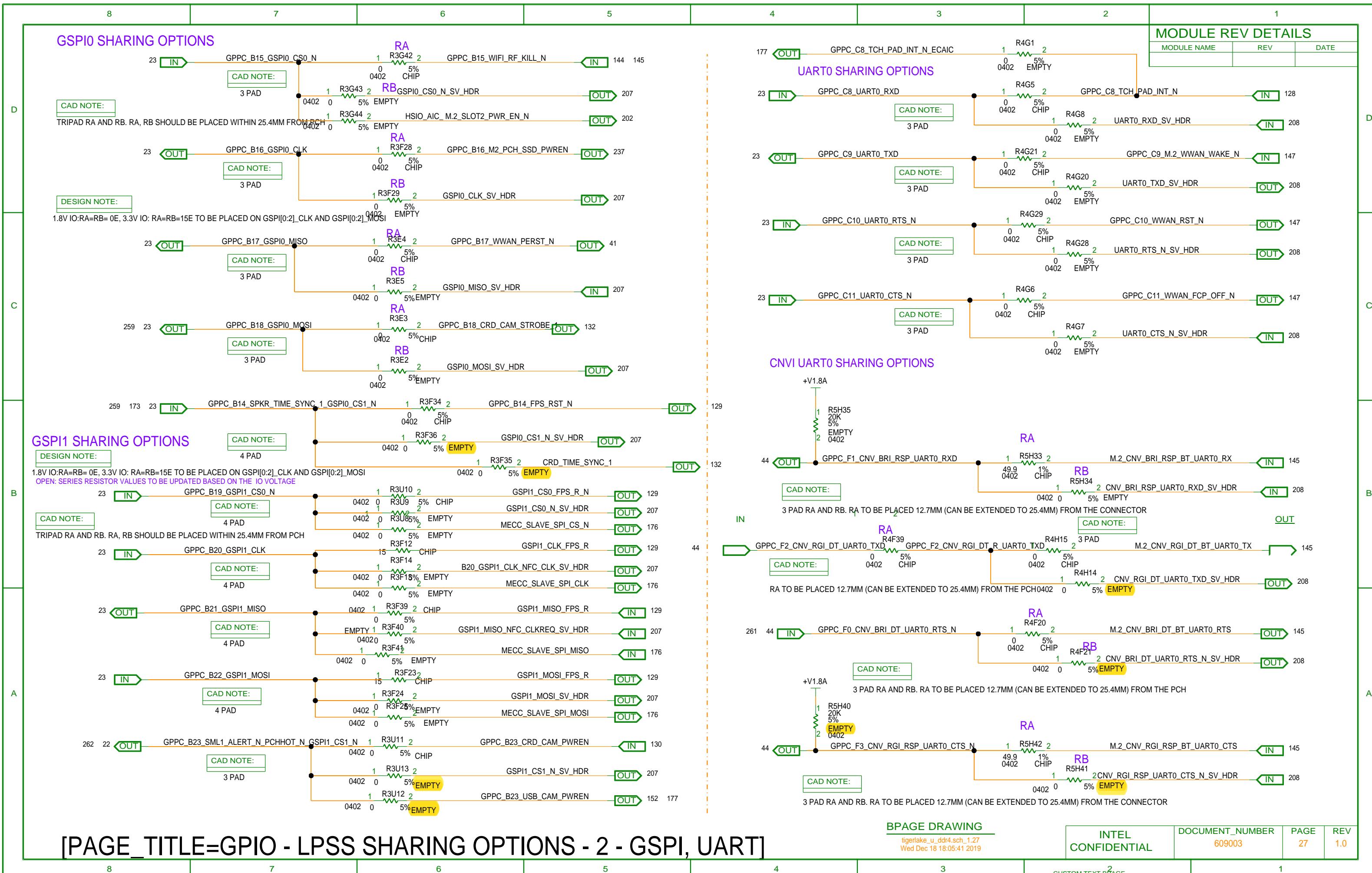
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MODULE REV DETAILS							

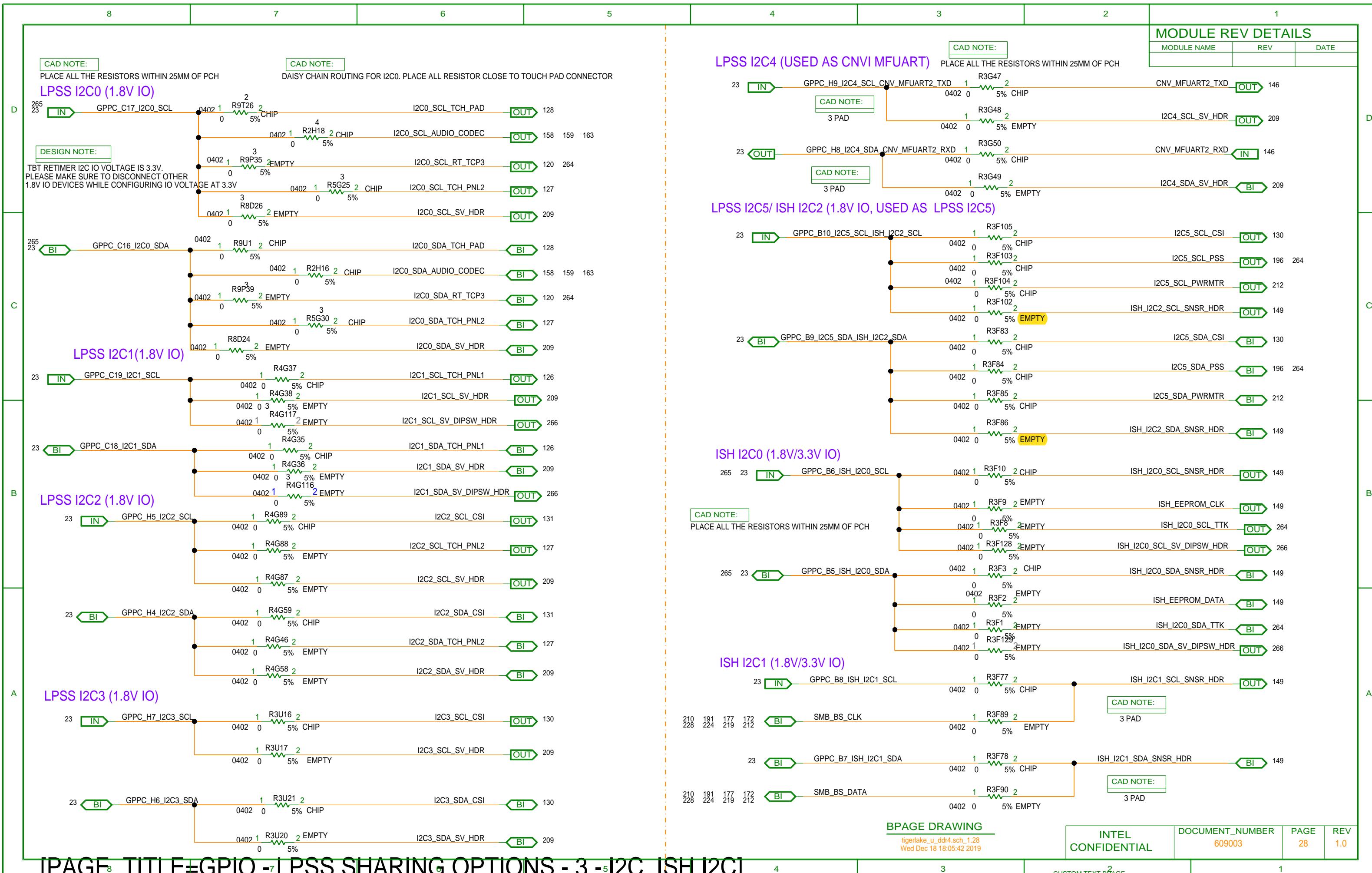


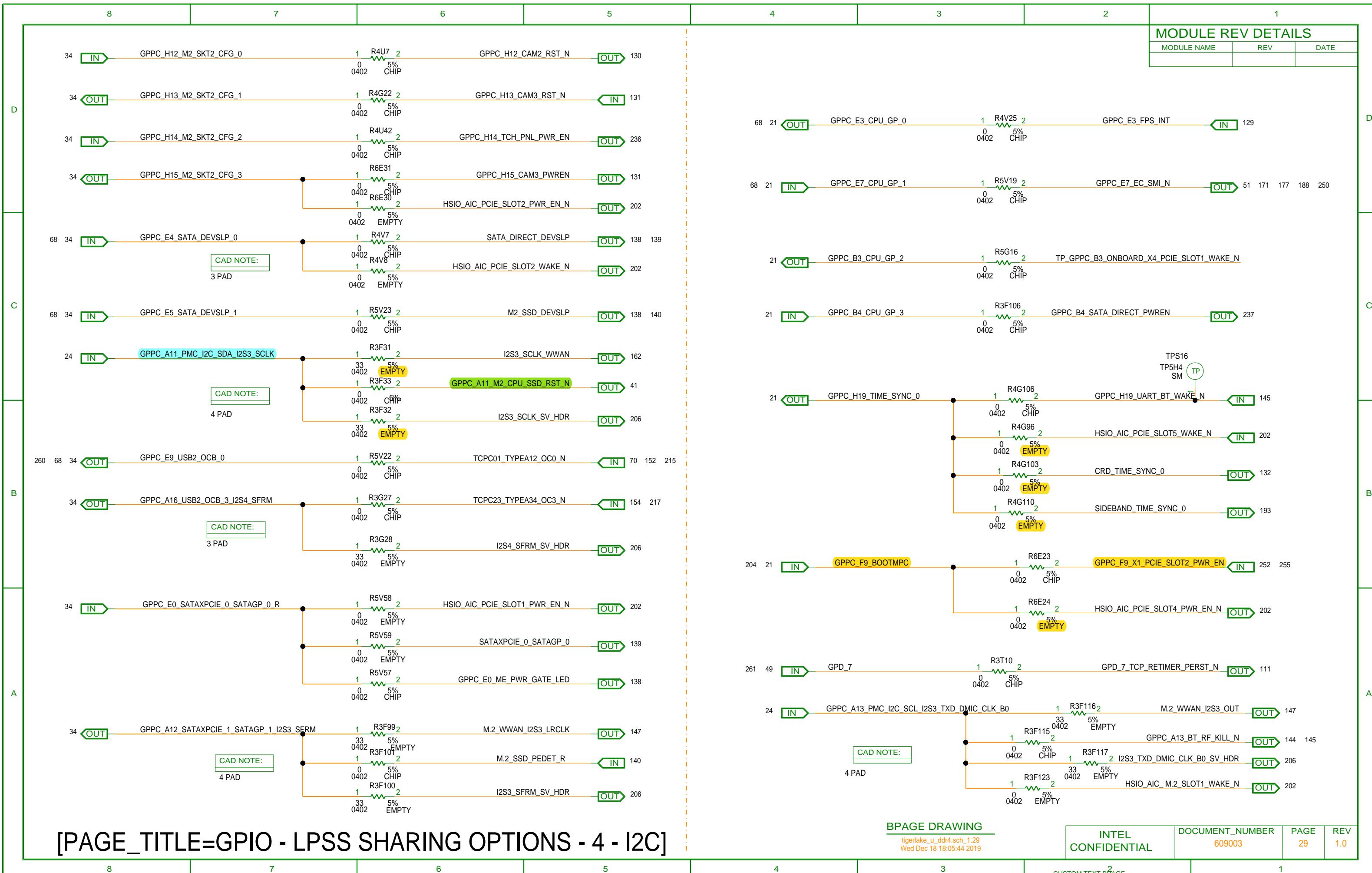
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

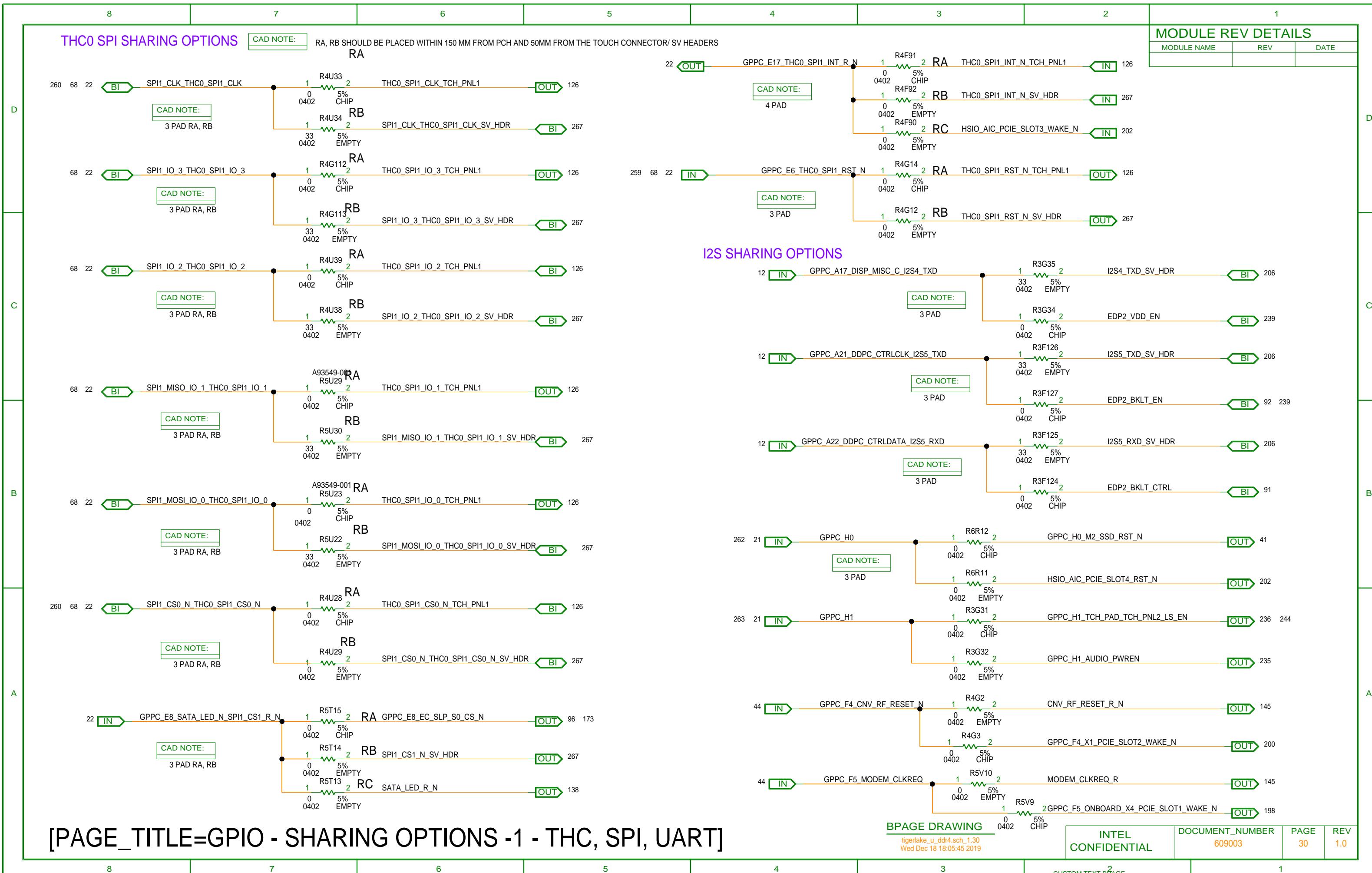


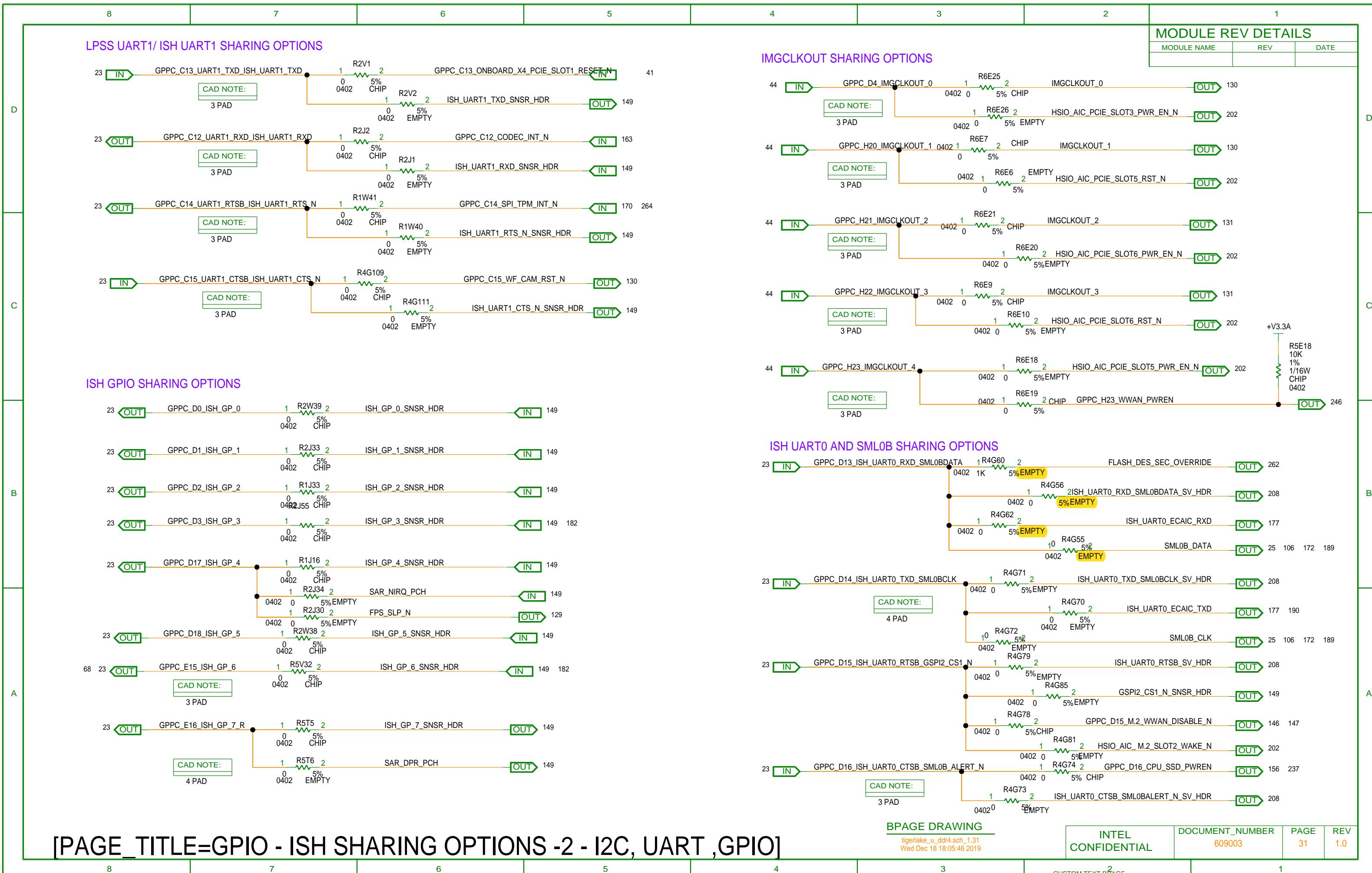






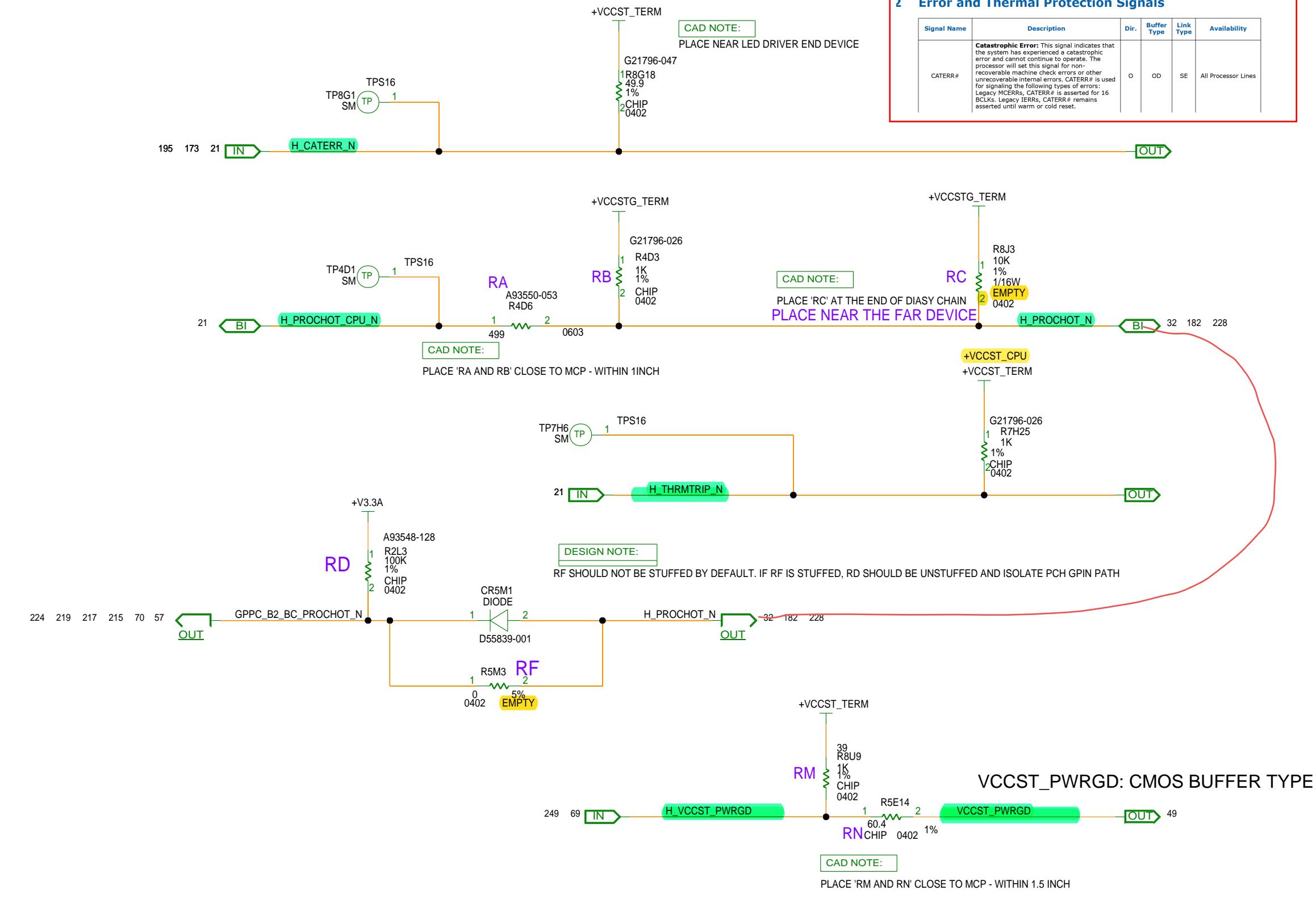






8	7	6	5	4	3	2	1
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CPU SIDEBAND SIGNALS

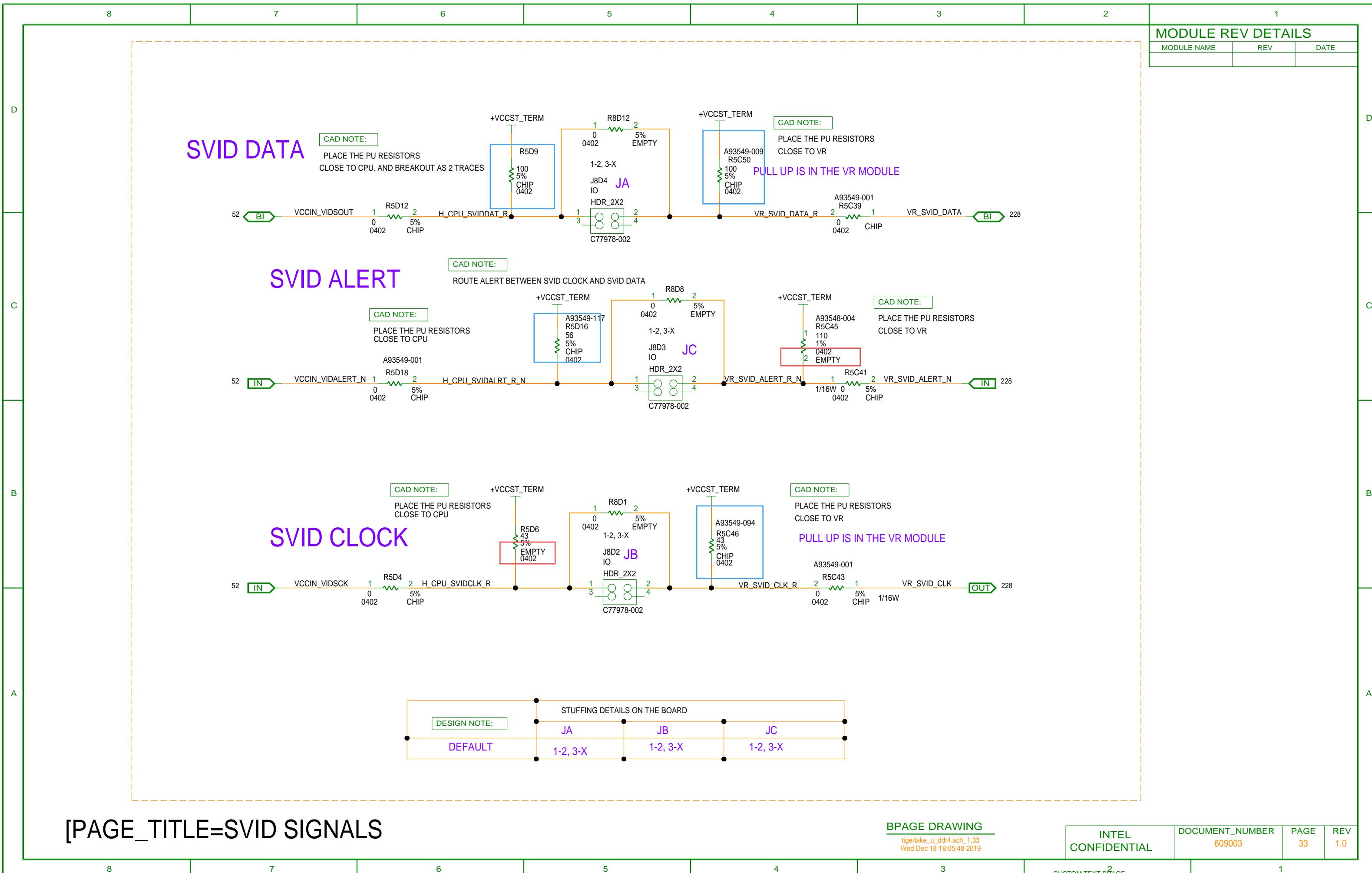


[PAGE_TITLE=GPIO - OTHER PCH GPIO SHARING OPTIONS - 1]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.32
Wed Dec 18 18:05:47 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 32	REV 1.0
CUSTOM TEXT 2 PAGE			

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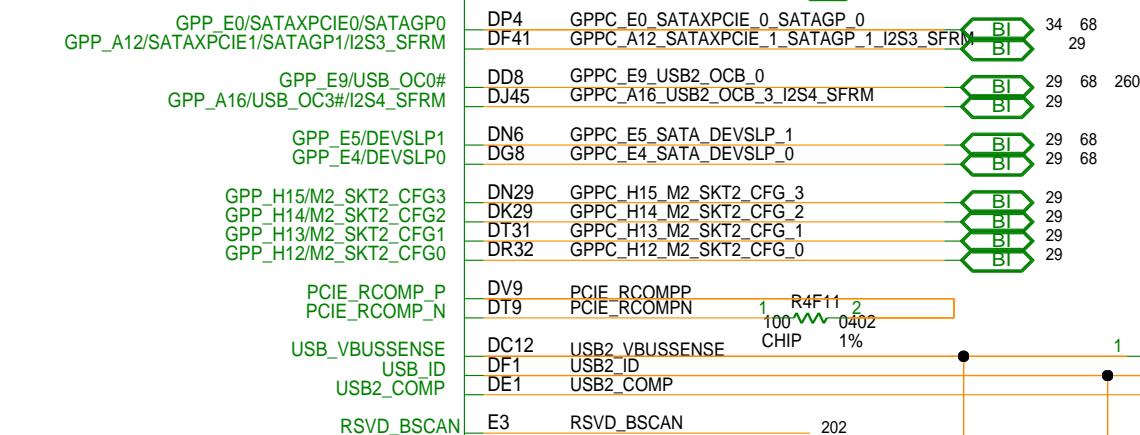
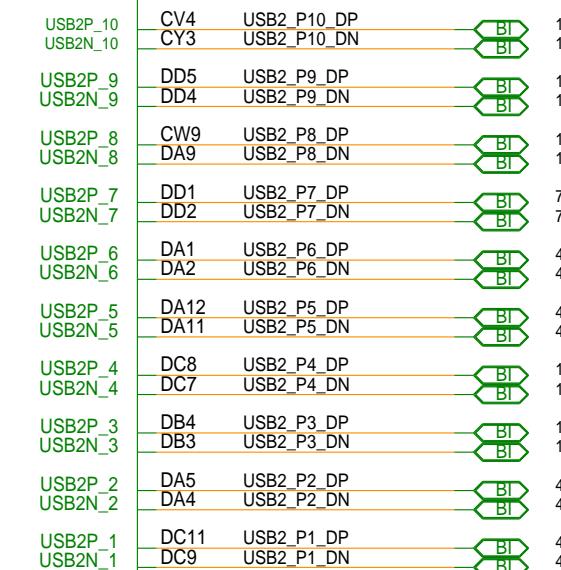
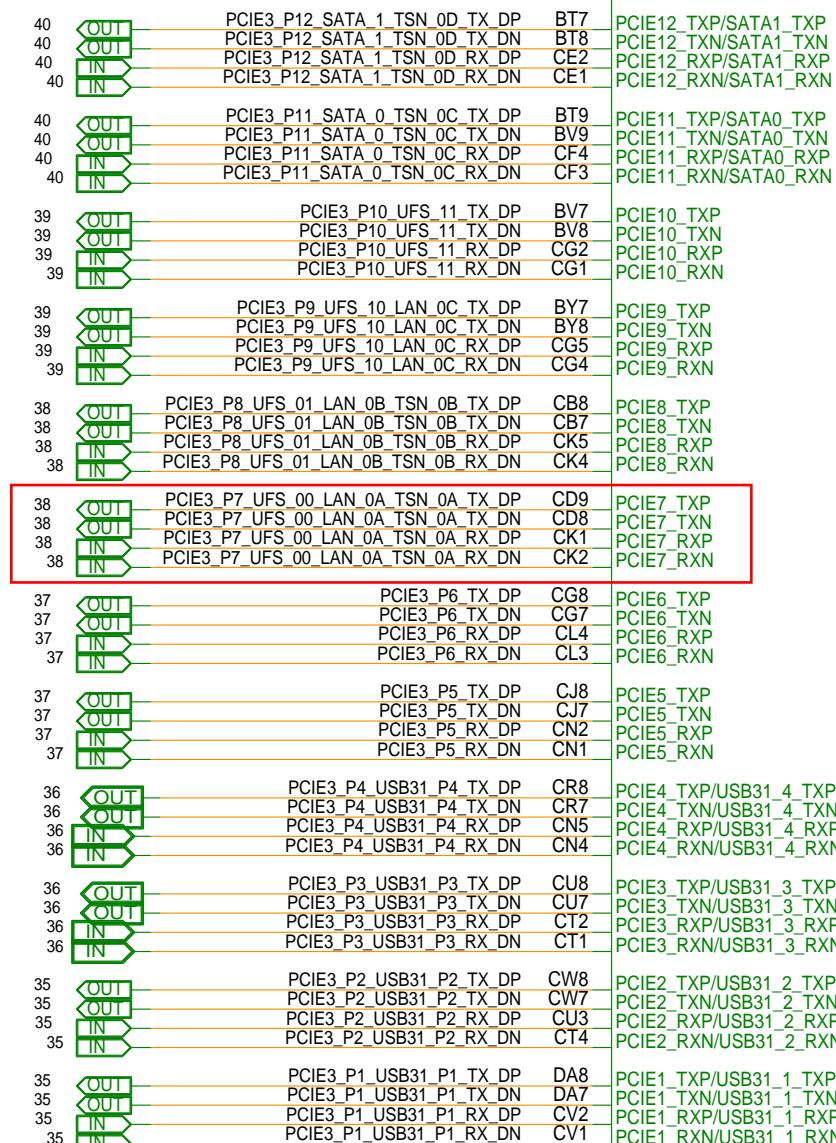
8	7	6	5	4	3	2	1
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MODULE REV DETAILS

MODULE NAME	REV	DATE

U4E1
SOC
1.6
TGL_UP3_IP_EXT

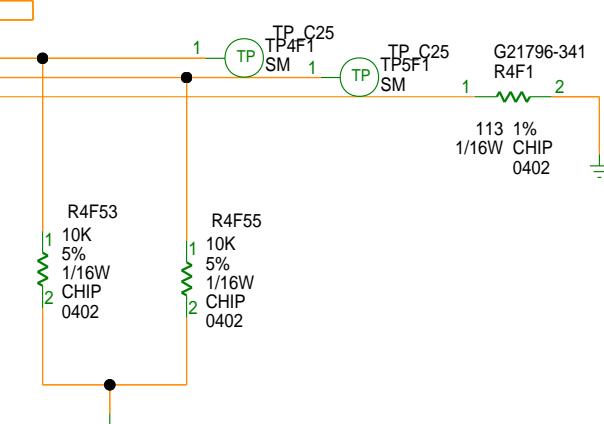
9 OF 21



PCIE_RCOMP_P
PCIE_RCOMP_N

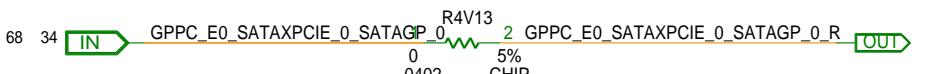
USB_VBUSENSE
USB_ID
USB2_COMP

RSVD_BSCAN



LPID6529

NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates



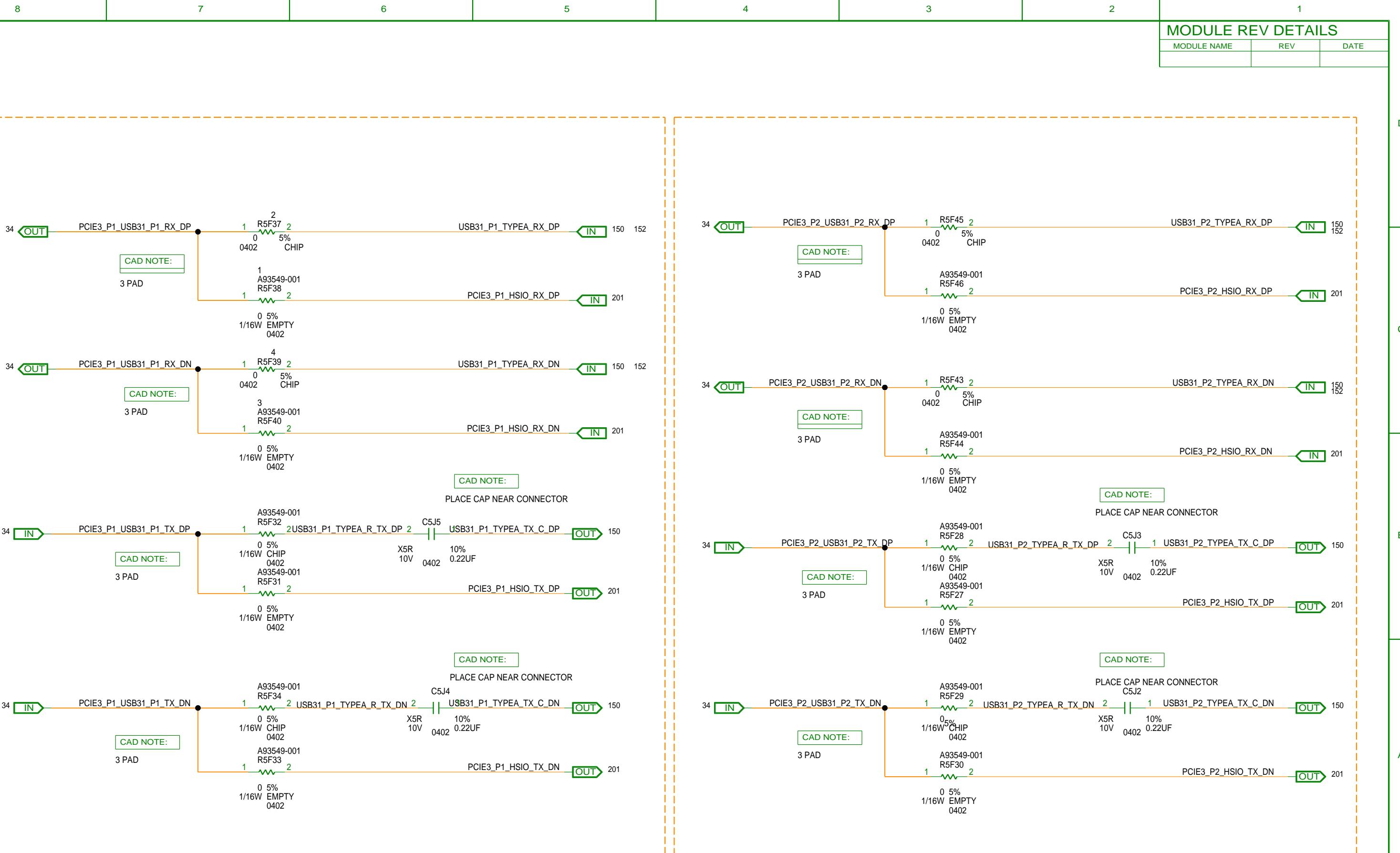
[PAGE_TITLE=TGL-U MCP (9 OF 21) - MODPHY

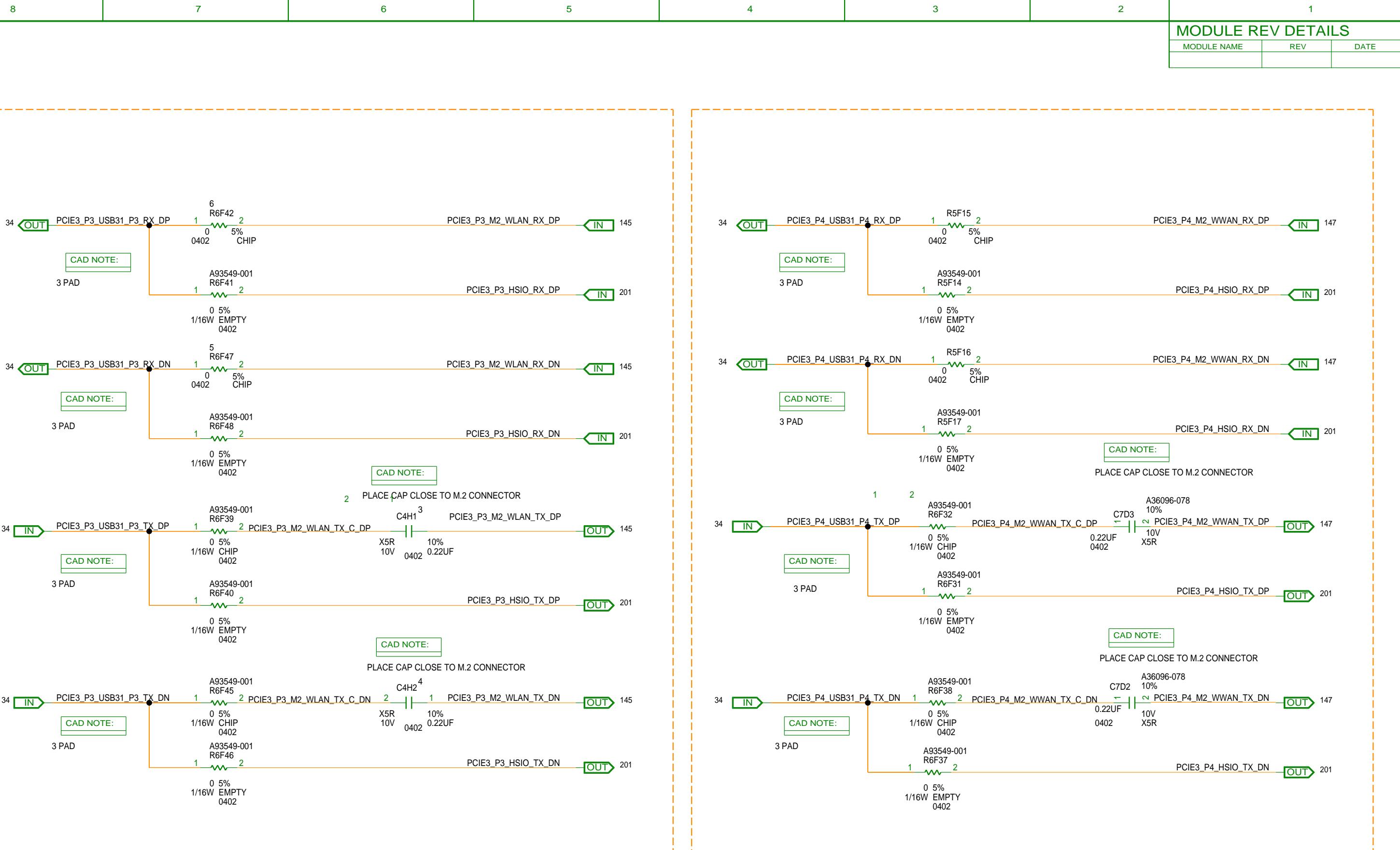
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tigerlake_u_ddr4.sch_1.34
Wed Dec 18 18:05:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	34	1.0	

CUSTOM TEXT B PAGE

1

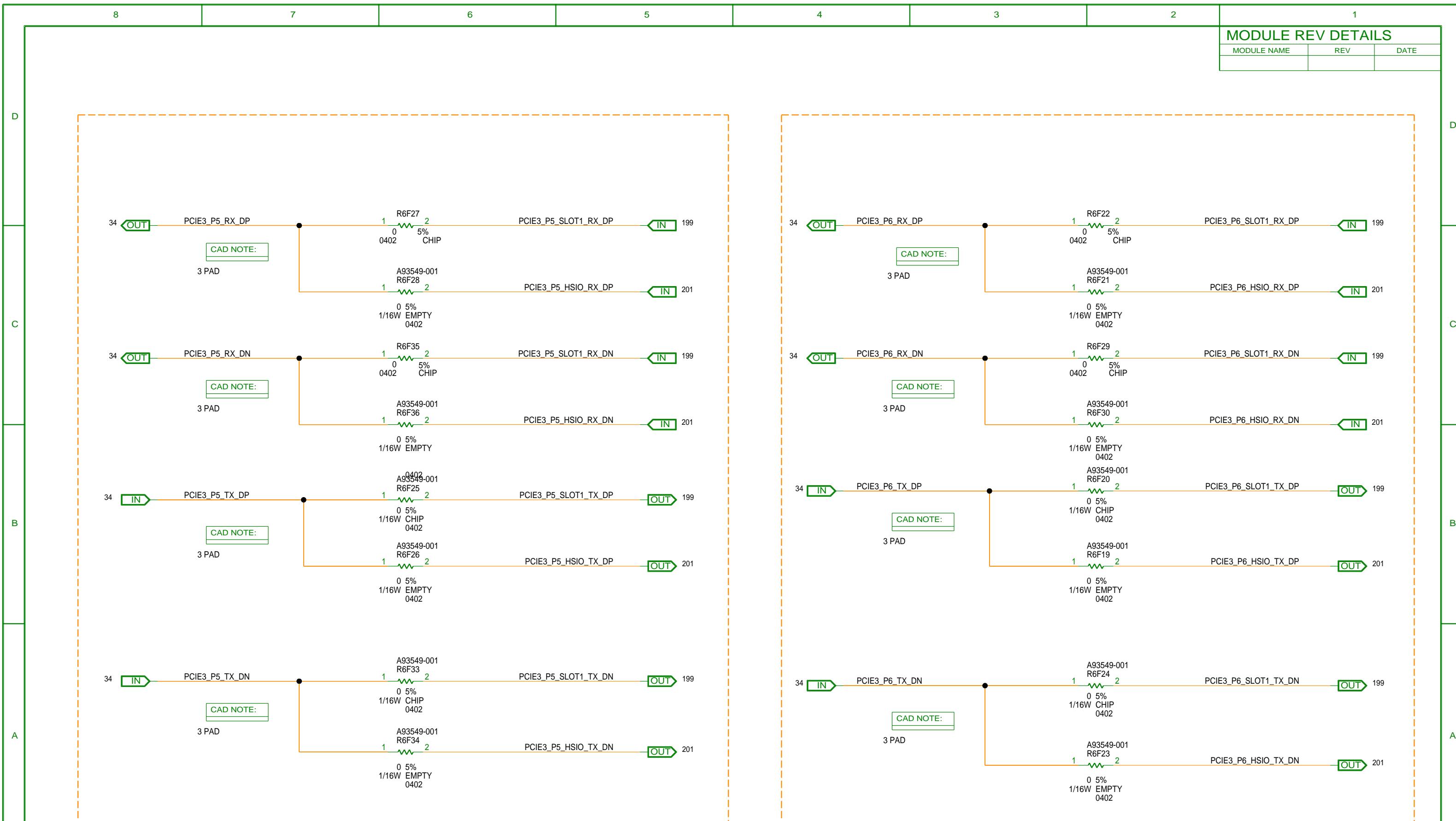




[PAGE_TITLE=PCIE PORT 3&4 SHARING OPTIONS, AC CAPS]

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tigerlake_u_ddr4.sch_1,36
Wed Dec 18 18:05:51 2019

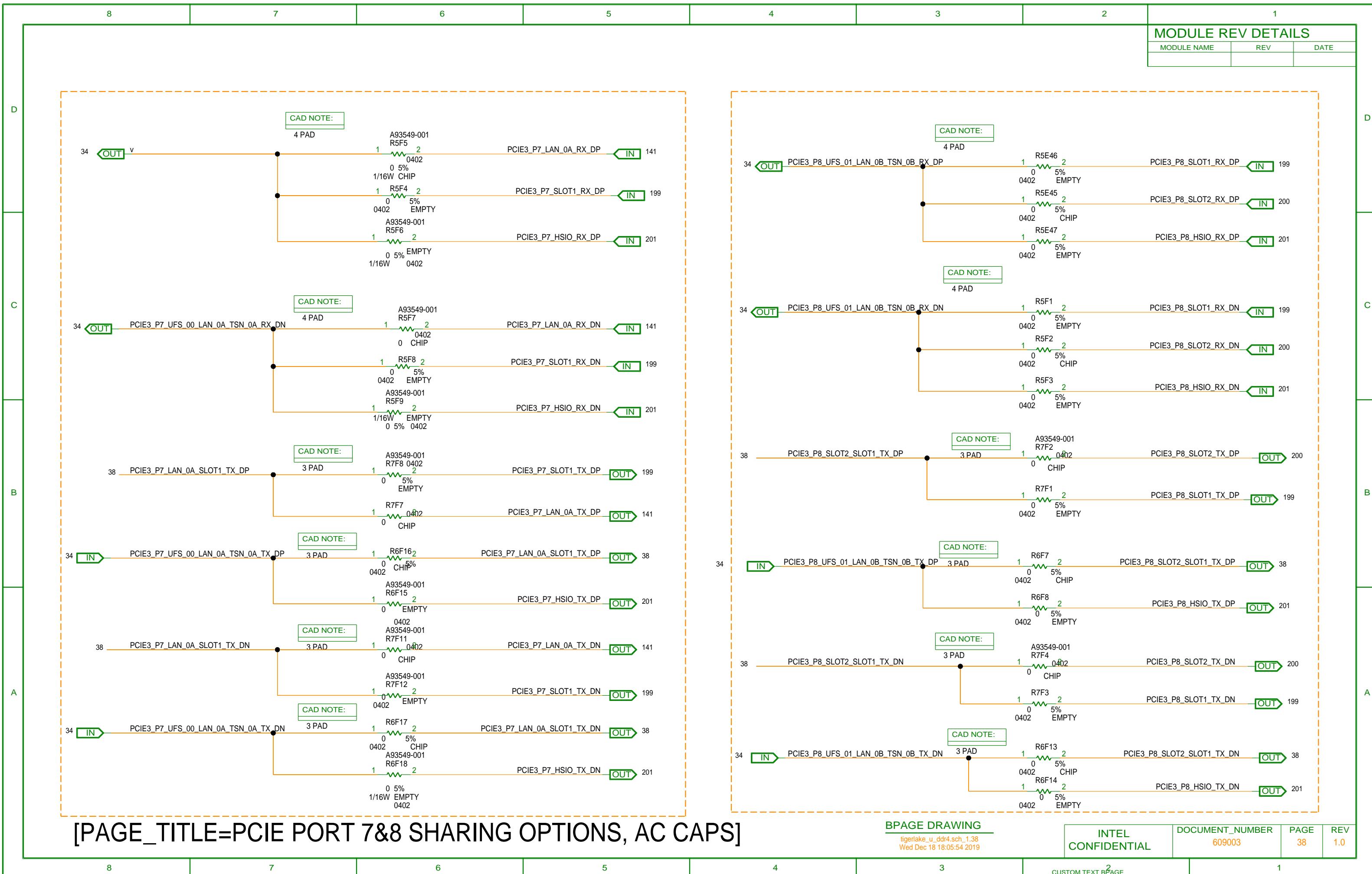
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 36	REV 1.0
CUSTOM TEXT BPAGE			



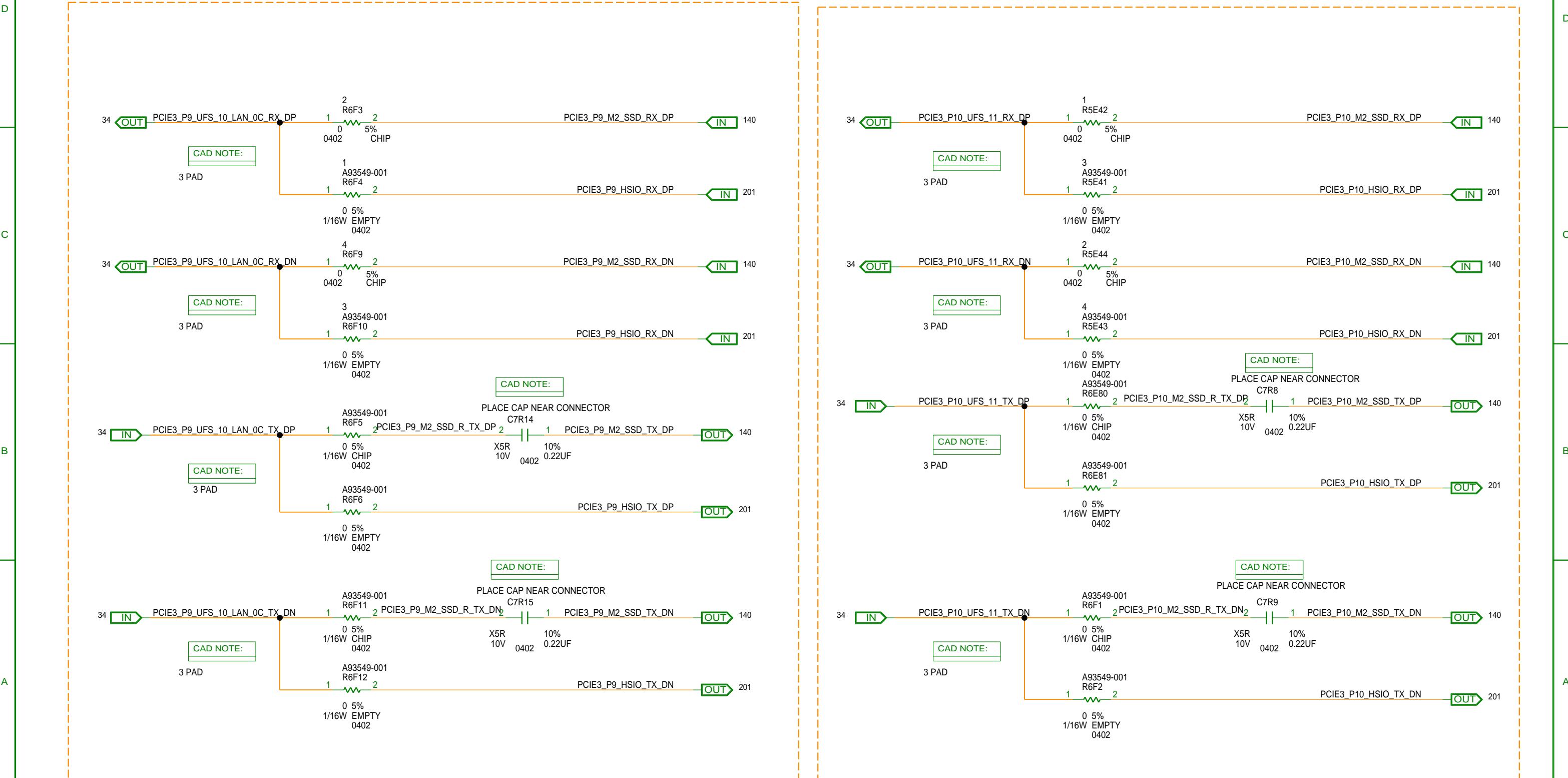
[PAGE_TITLE=PCIE PORT 5&6 SHARING OPTIONS, AC CAPS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.37
Wed Dec 18 18:05:52 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 37	REV 1.0
CUSTOM TEXT BPAGE			



8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME	REV	DATE					

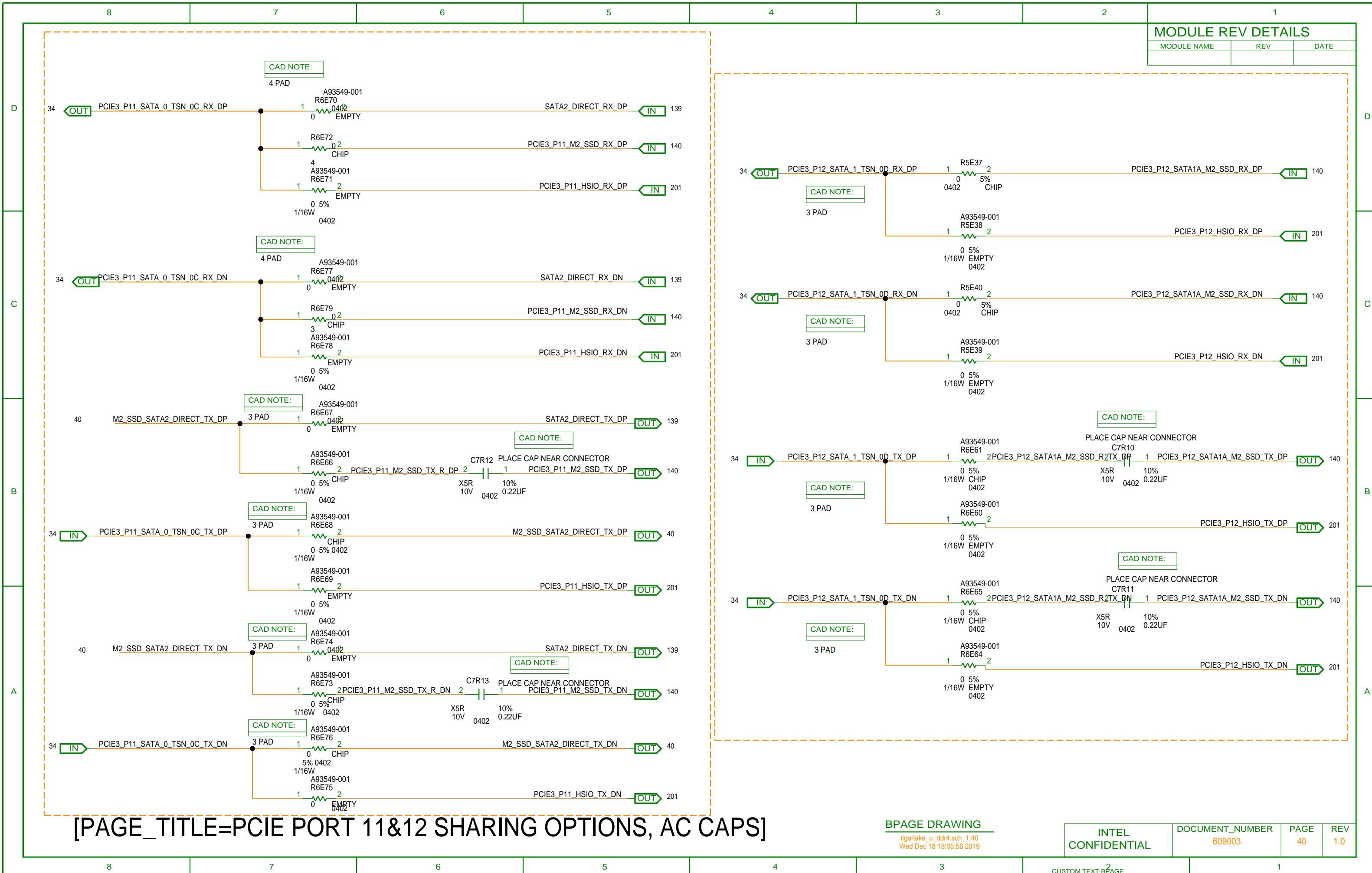


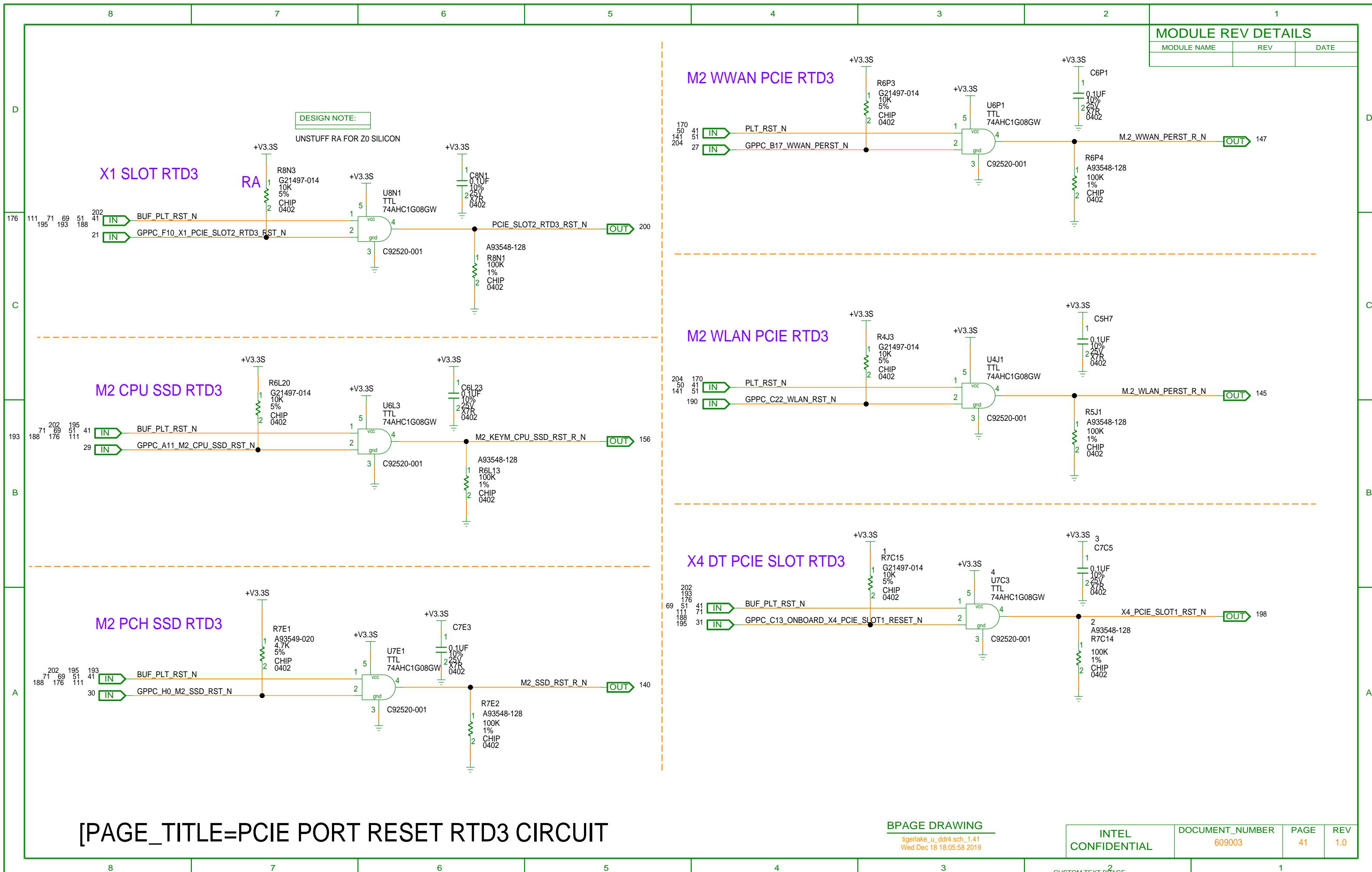
[PAGE_TITLE=PCIE PORT 9&10 SHARING OPTIONS, AC CAPS]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.39
Wed Dec 18 18:05:55 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	39	1.0

CUSTOM TEXT BPAGE





8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

D

D

C

C

B

B

A

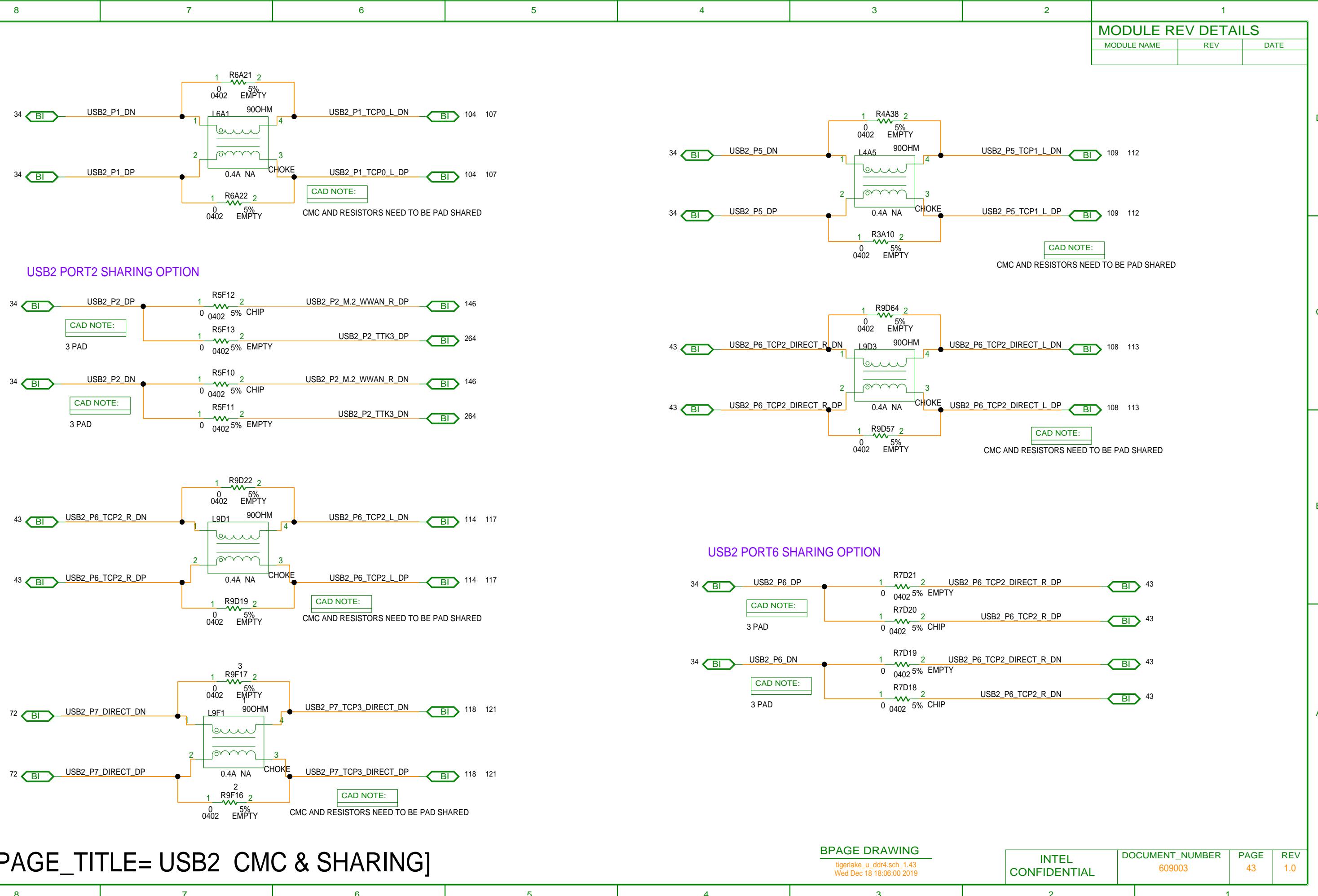
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[PAGE_TITLE=RESERVED]

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Tue Oct 15 12:49:02 2019

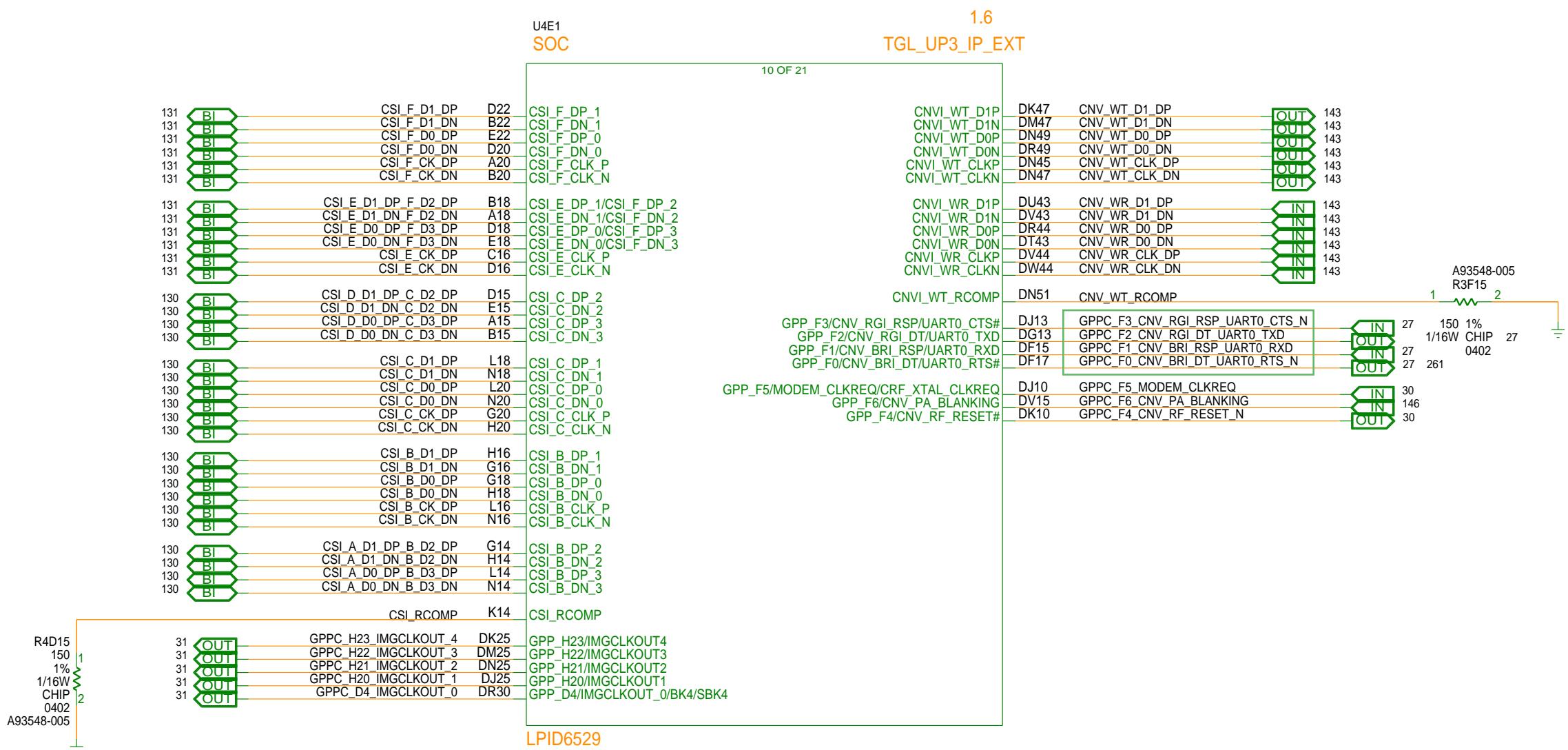
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	42	1.0

8	7	6	5	4	3	CUSTOM TEXT ² PAGE	1
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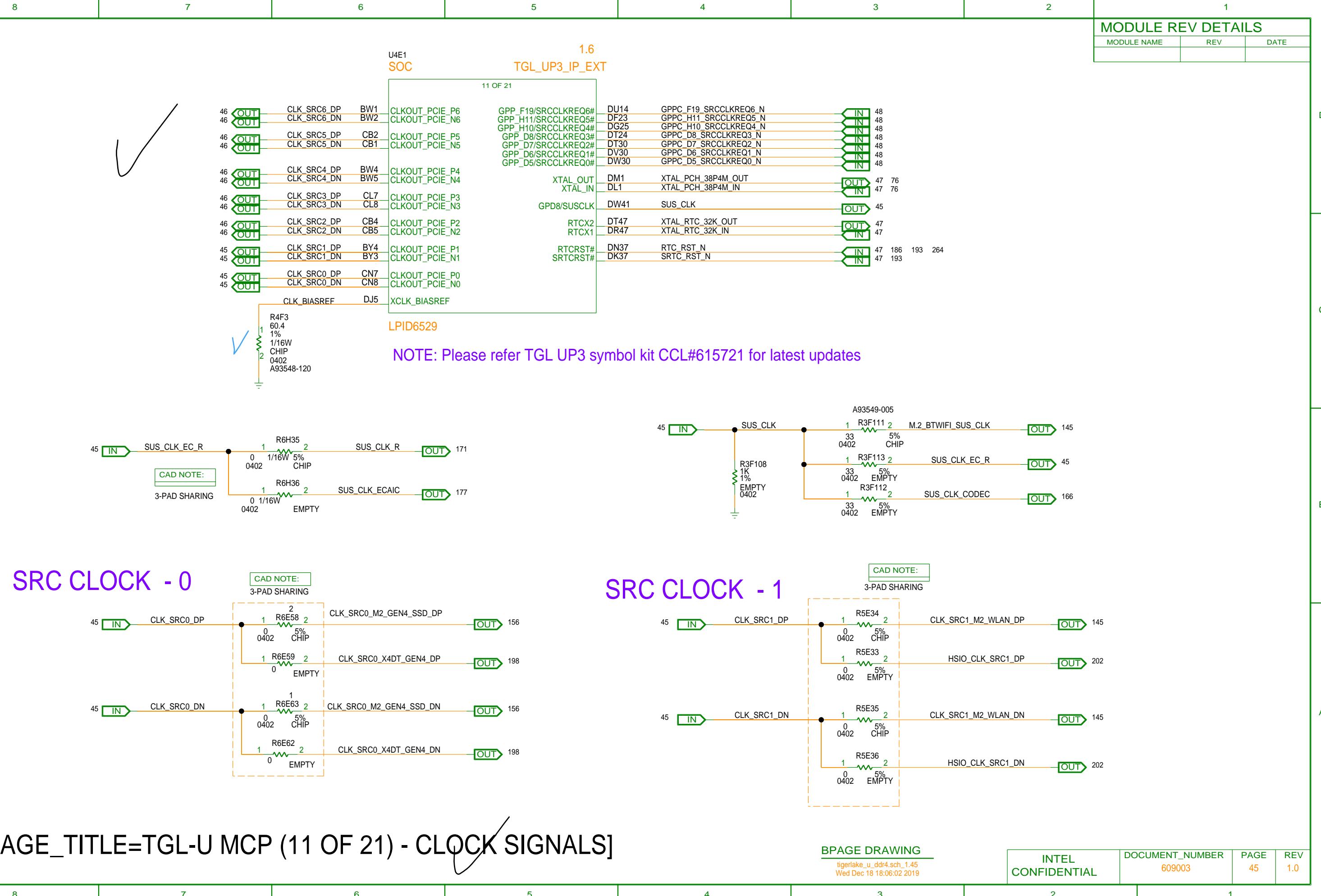


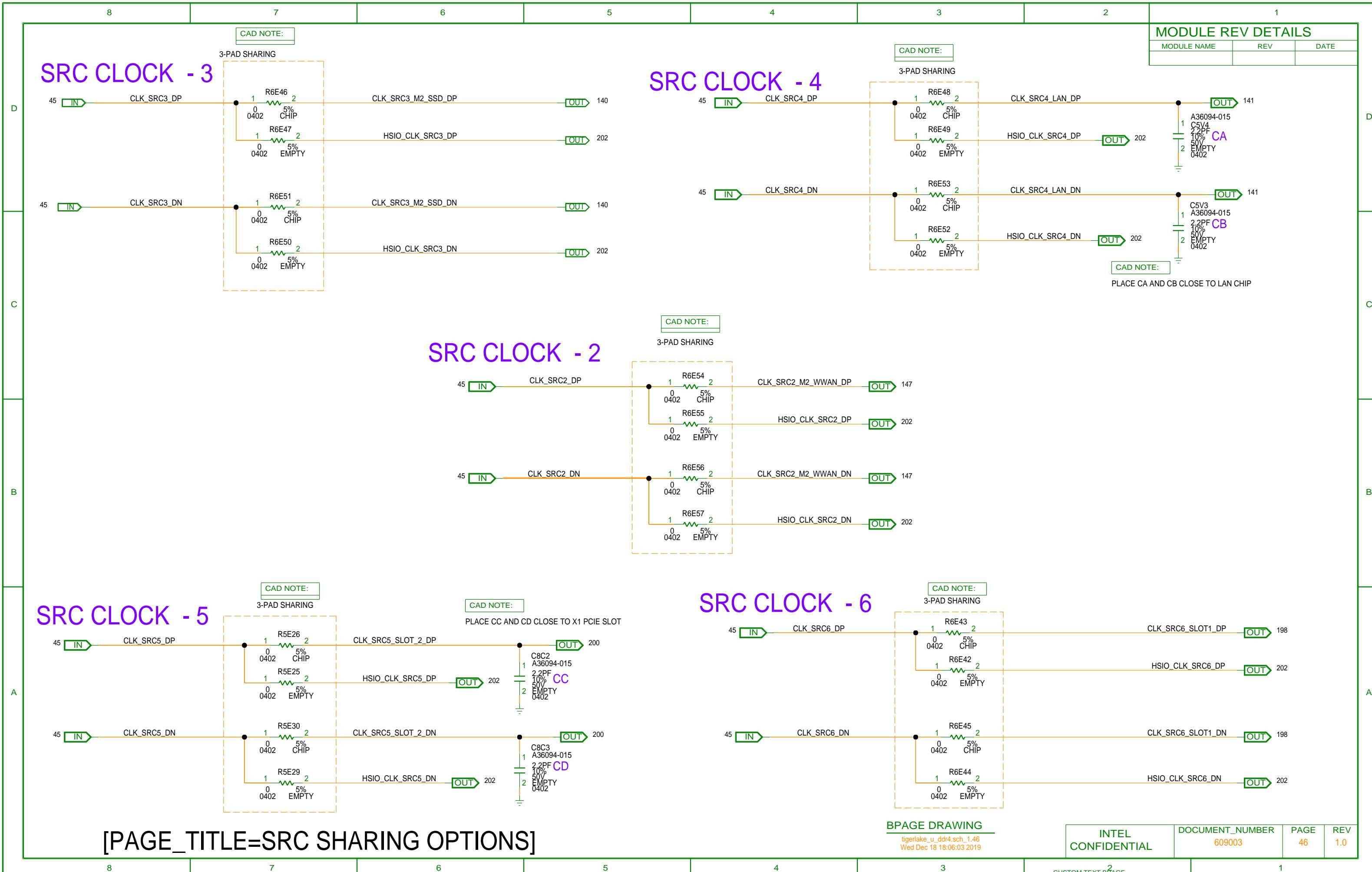
8	7	6	5	4	3	2	1
MODULE REV DETAILS							

DIDNT IMPLEMENT YET



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates





8	7	6	5	4	3	2	1
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MODULE REV DETAILS

MODULE NAME	REV	DATE

D

D

C

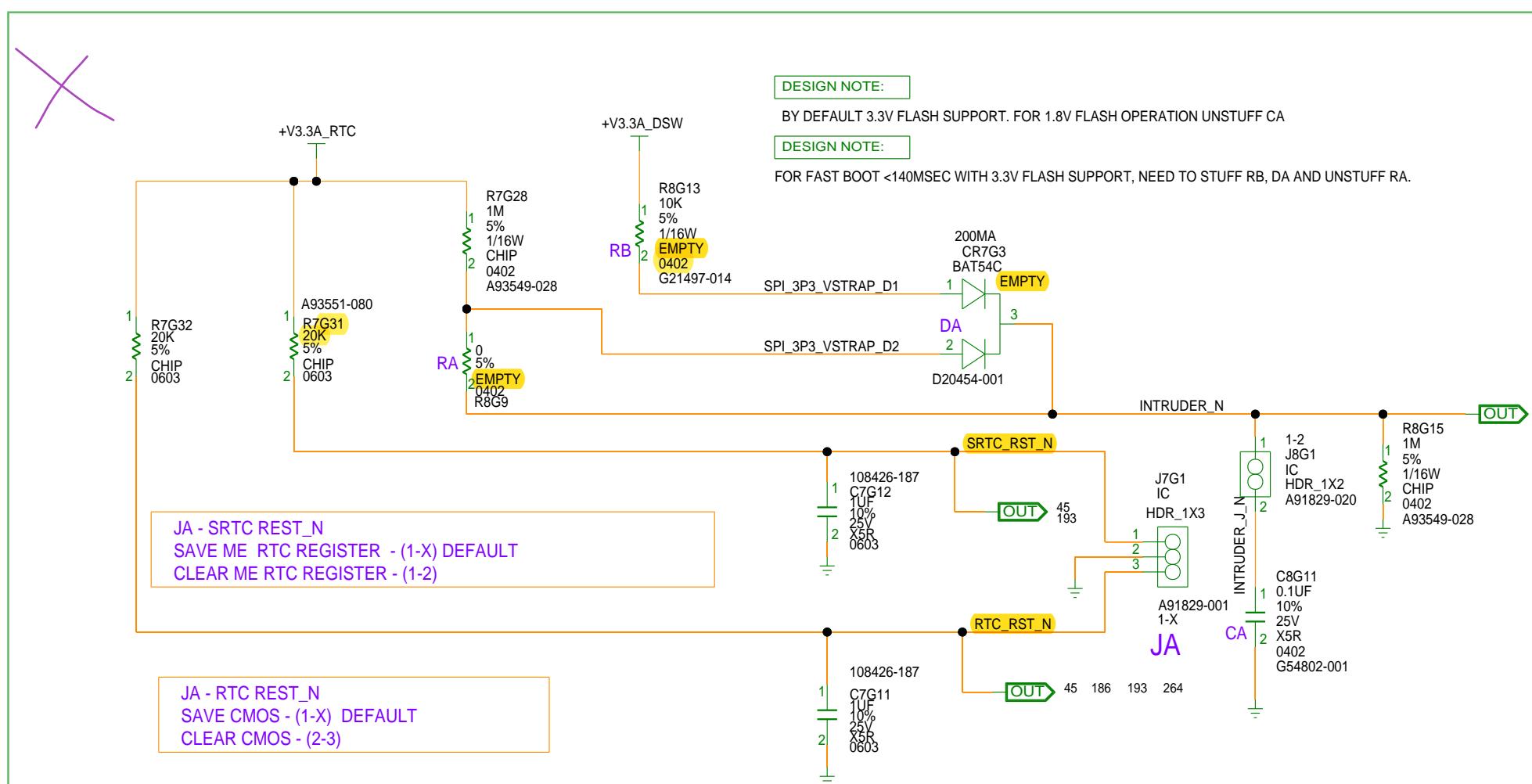
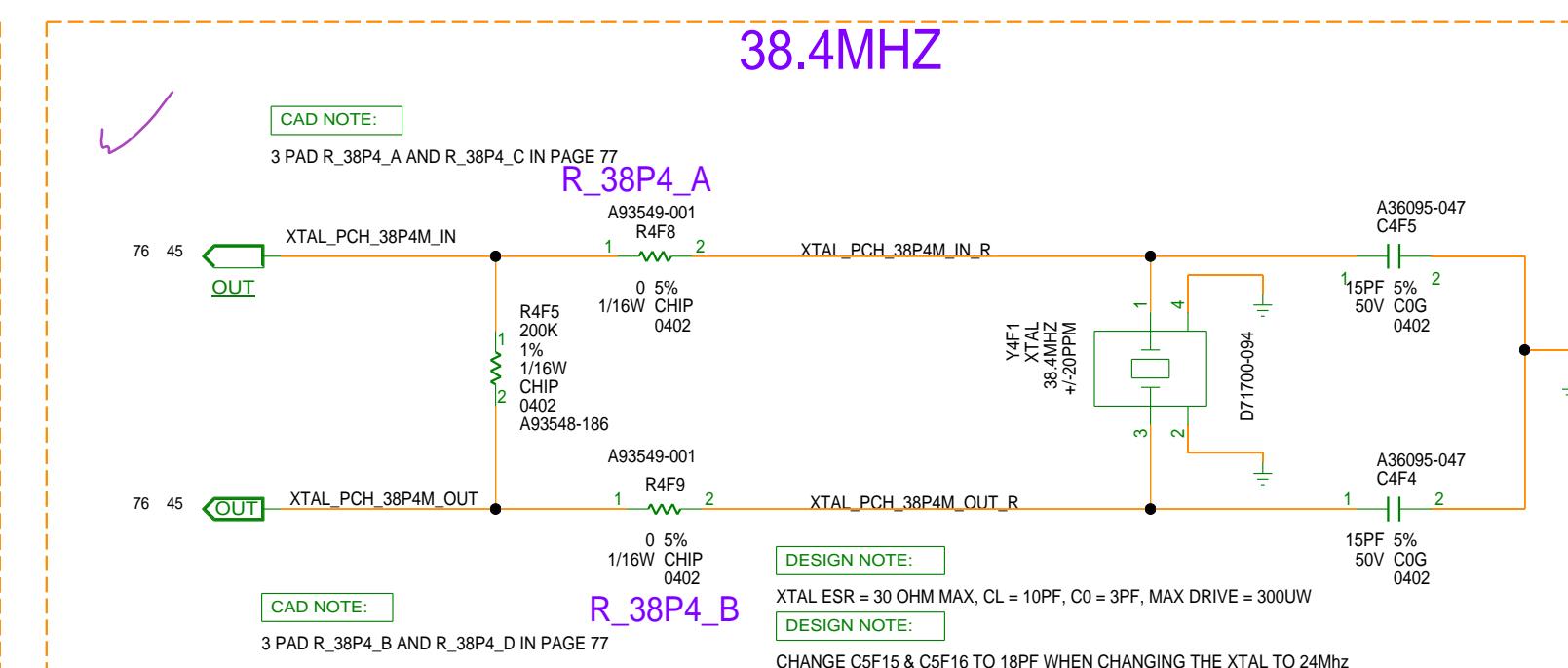
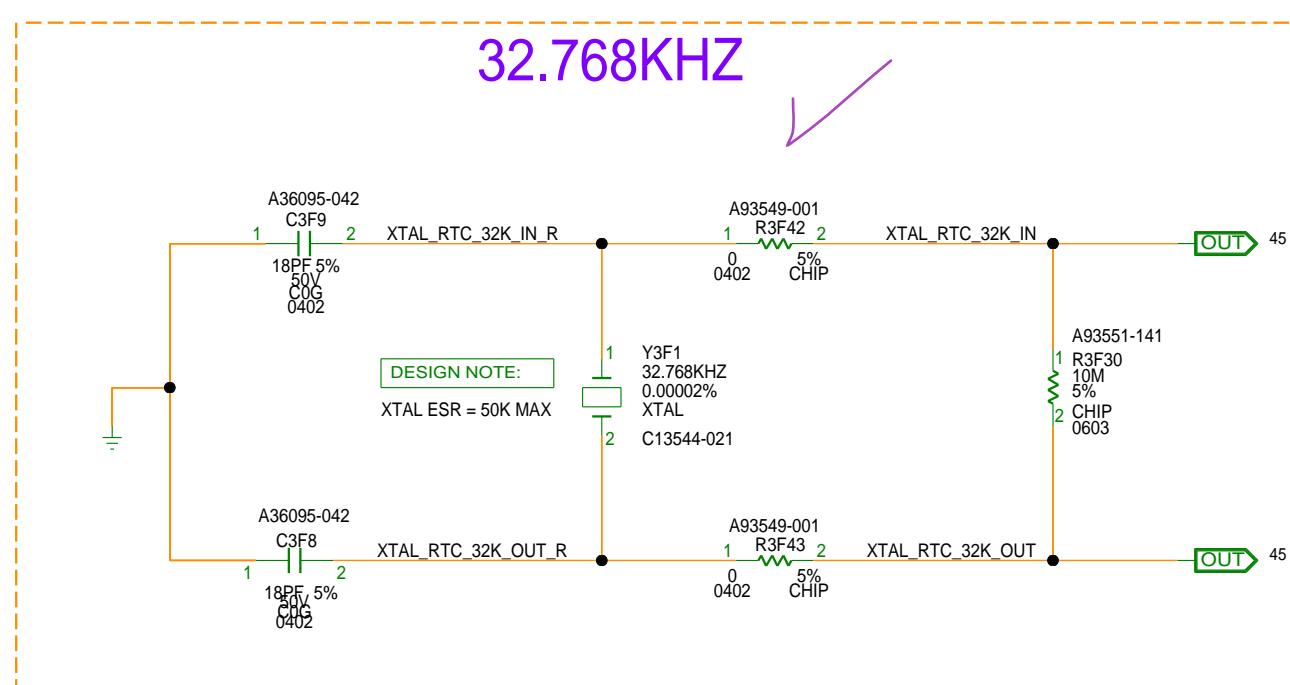
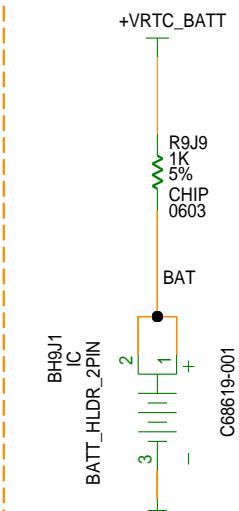
C

B

B

A

A

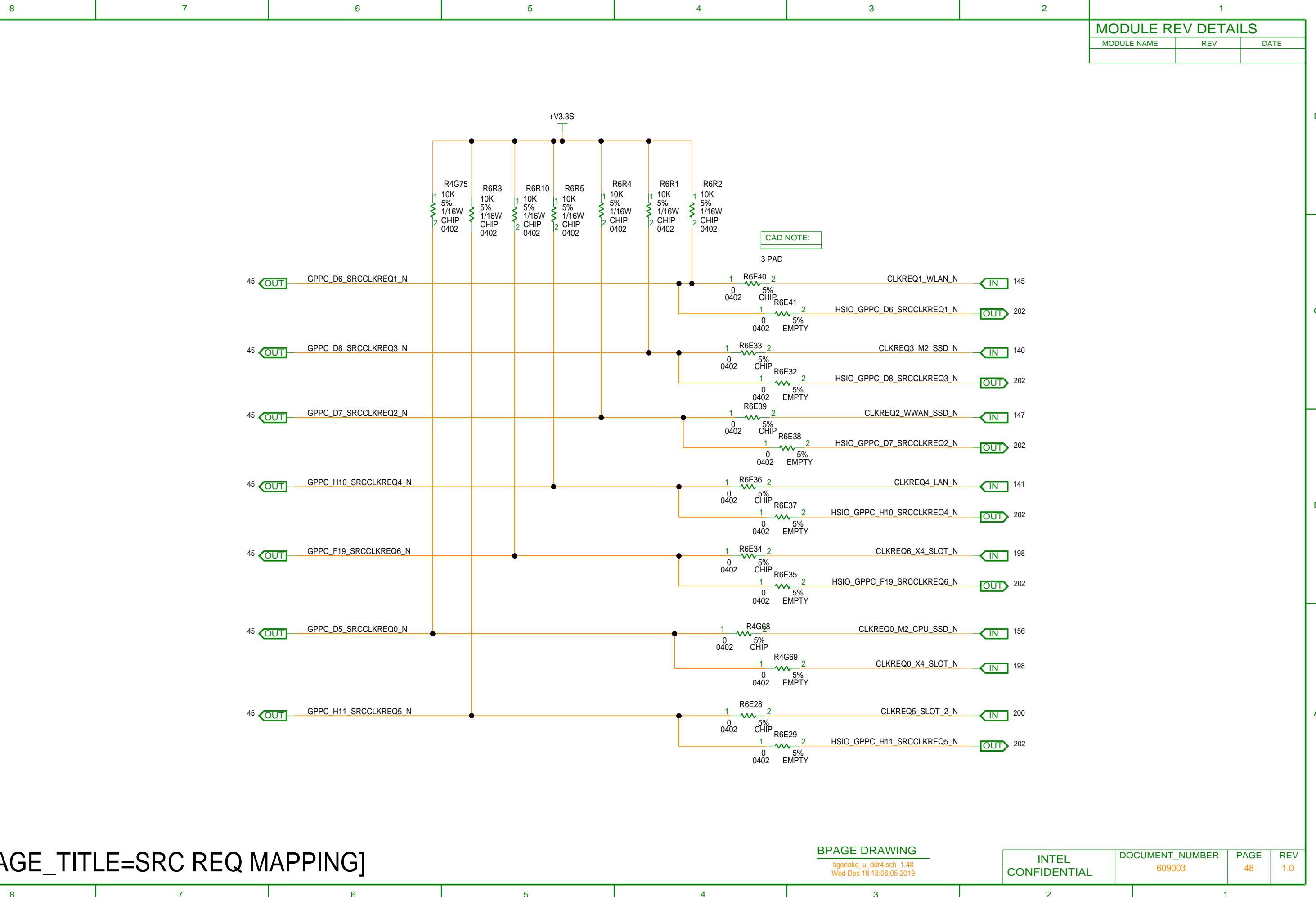
**+V3.3A_RTC GENERATION****[PAGE_TITLE=CLOCK - CRYSTAL]****BPAGE DRAWING**
tigerlake_u_ddr4.sch_1.47
Wed Dec 18 18:06:04 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 47	REV 1.0
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8	7	6	5	4	3	2	1
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CUSTOM TEXT BPAGE

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8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

D

D

C

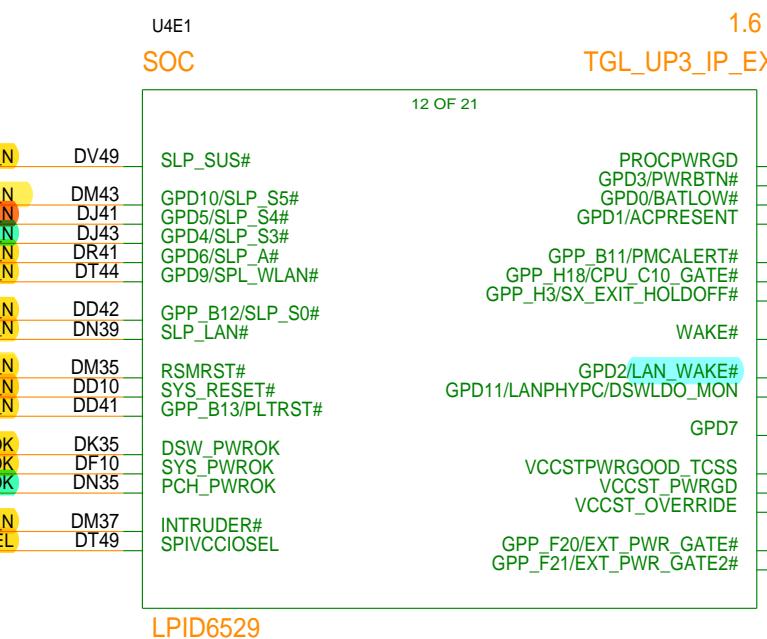
C

B

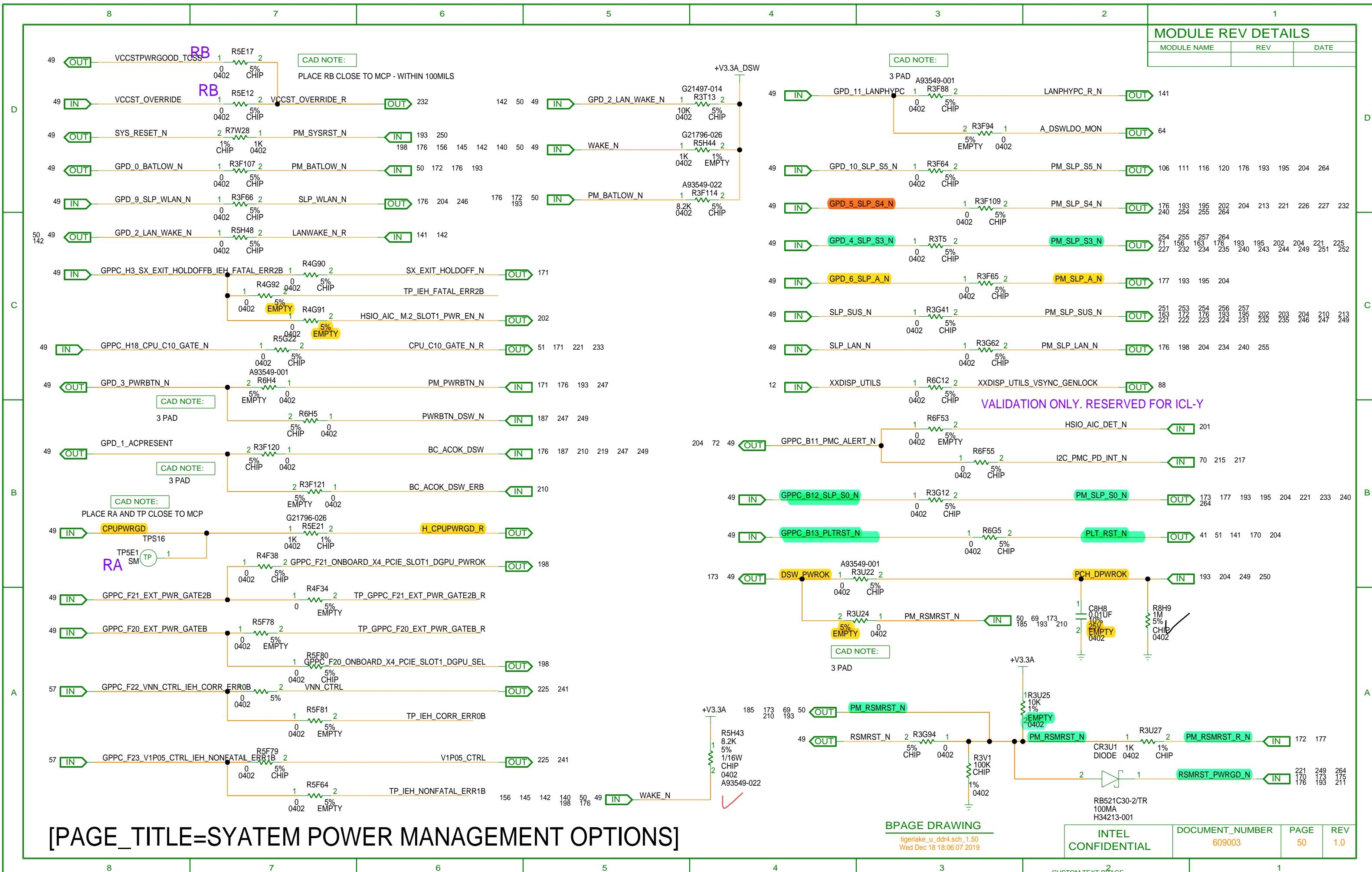
B

A

A

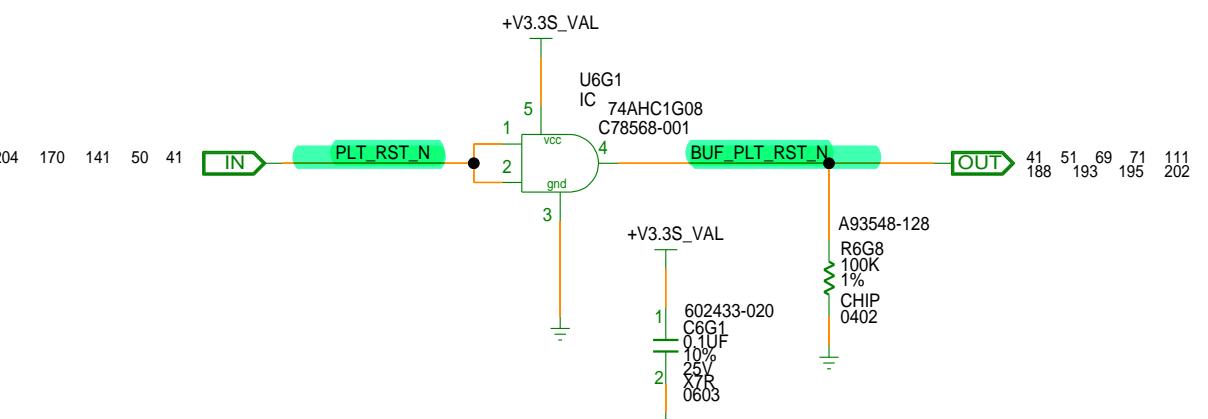


NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

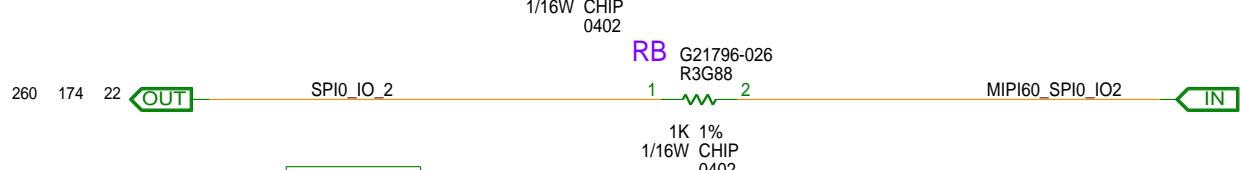
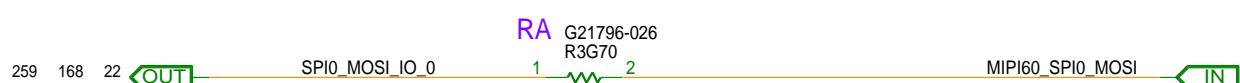
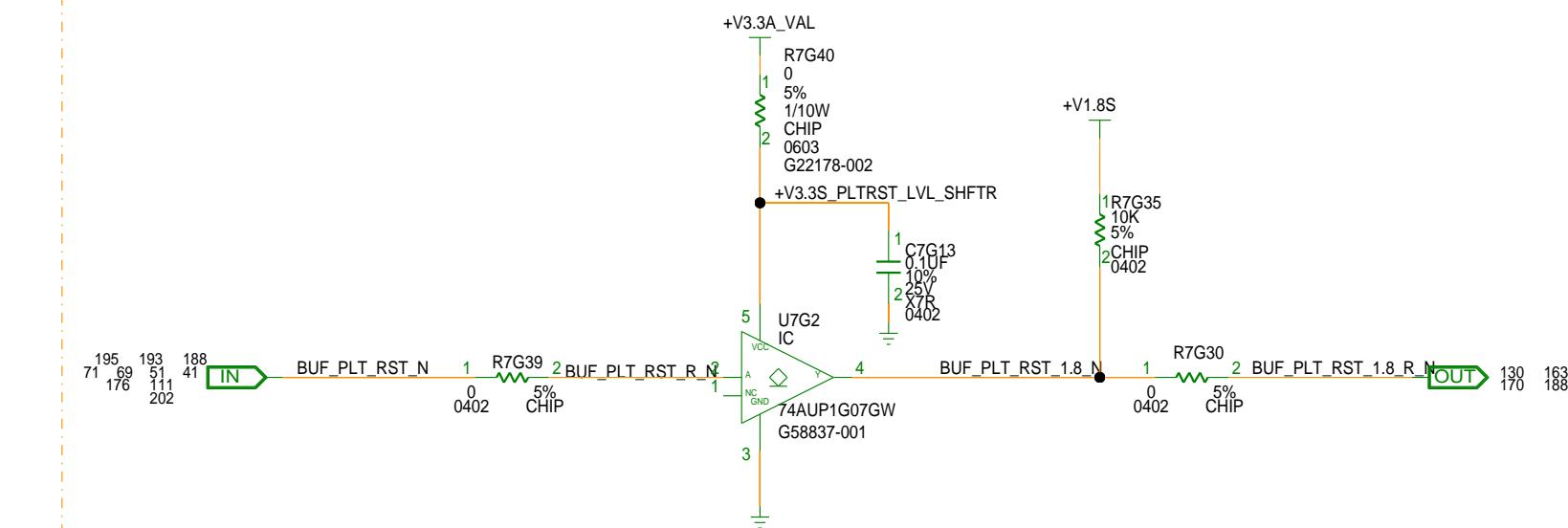


8	7	6	5	4	3	2	1
MODULE REV DETAILS							

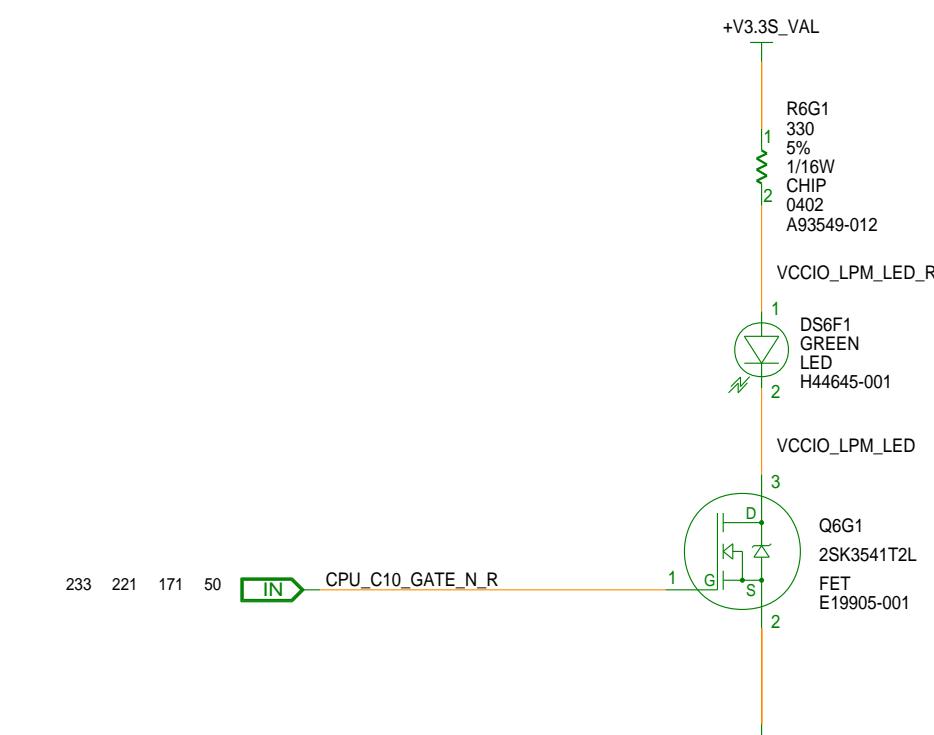
BUFFER TO REDUCE LOADING ON PLT_RST_N



PLATFORM RESET LEVEL SHIFTER - 3.3V TO 1.8V



CAD NOTE:
RA AND RB RESISTORS NEED TO BE PLACED NEAR TO MCP, WITHOUT STUB ON SPI



8

7

6

5

4

3

2

1

MODULE REV DETAILS

MODULE NAME	REV	DATE

D

D

C

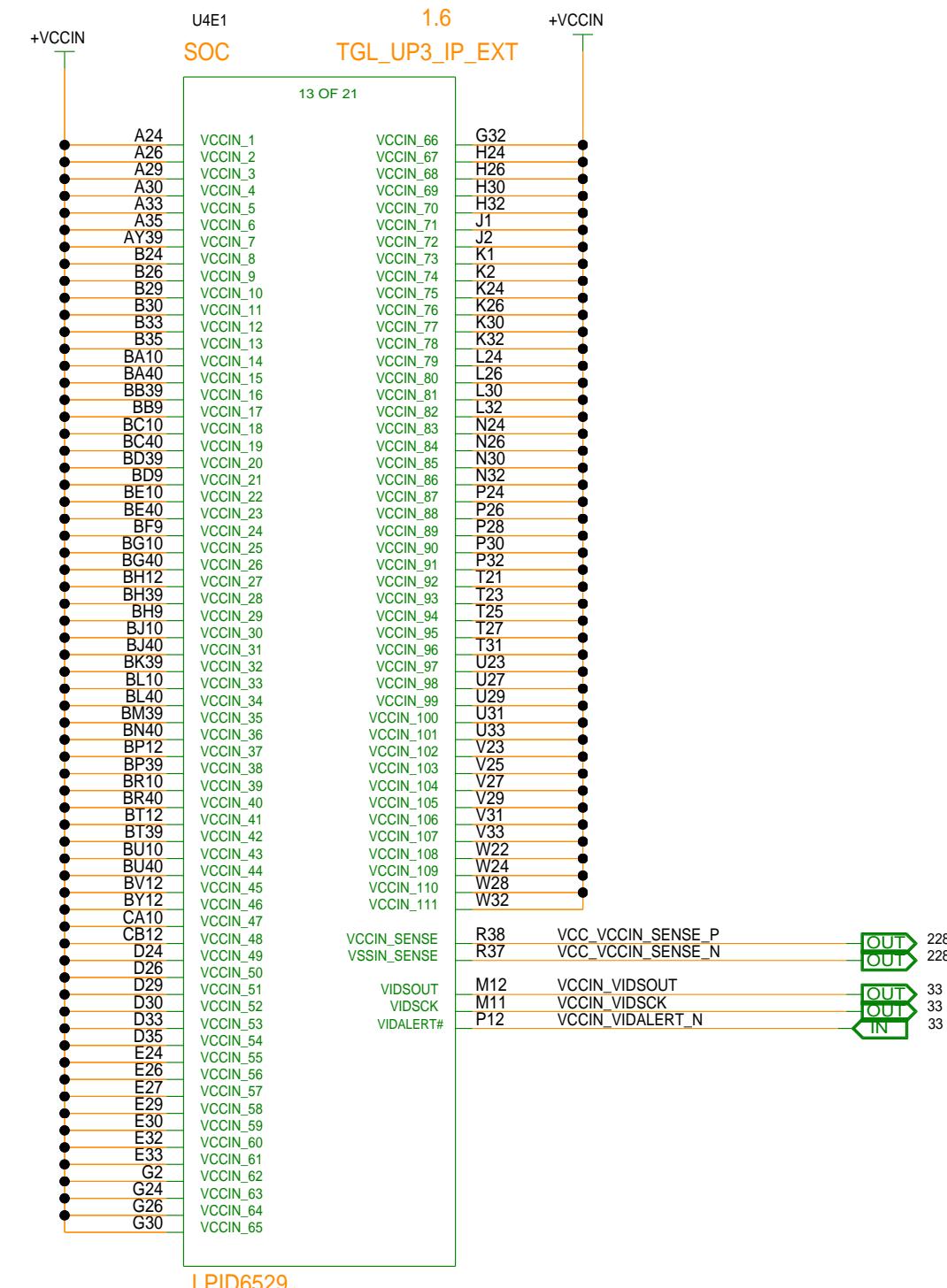
C

B

B

A

A



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL U MCP (13 OF 21) - CPU POWER 1 OF 2]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.52
Wed Dec 18 18:06:09 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	52	1.0

8

7

6

5

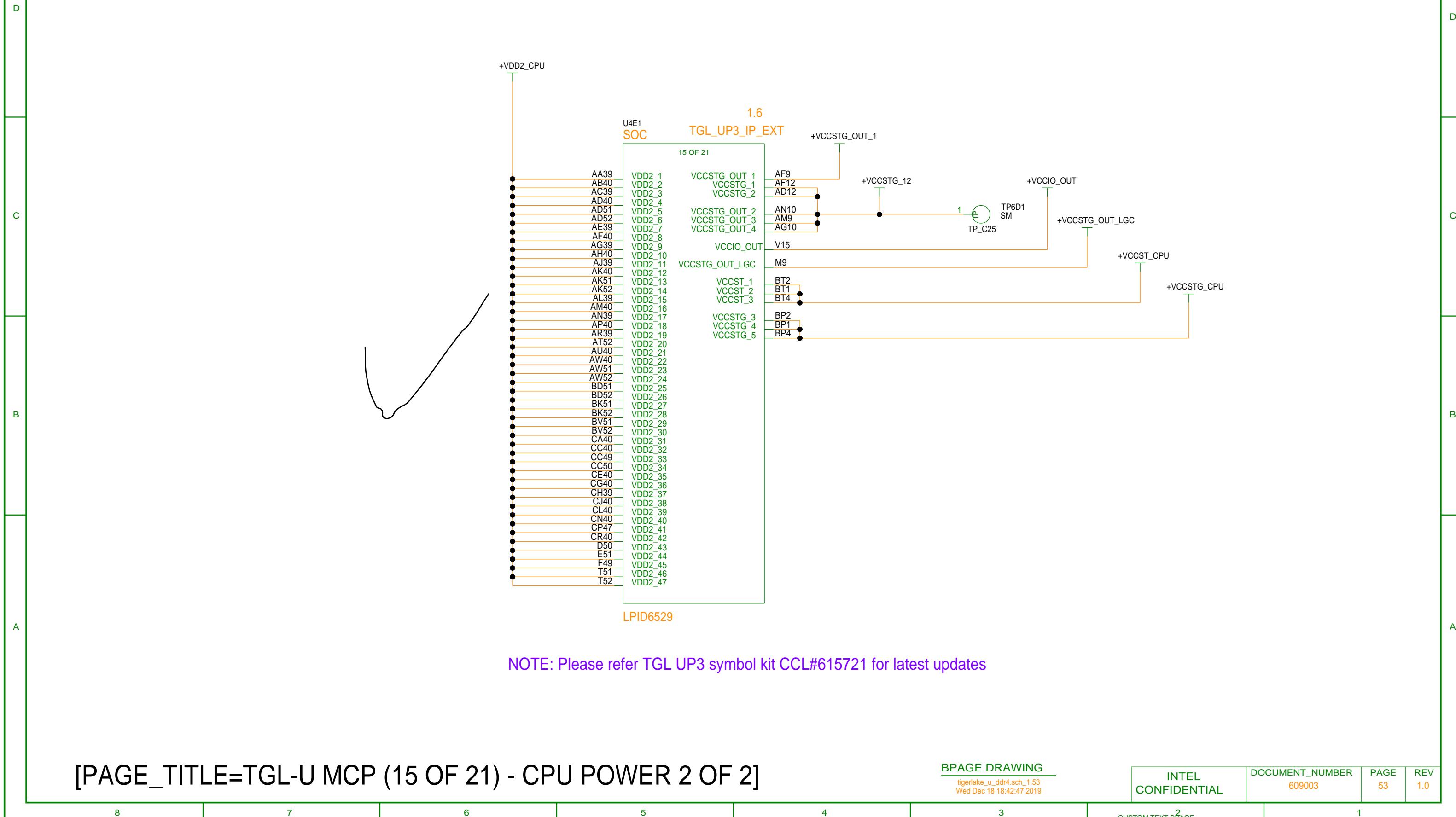
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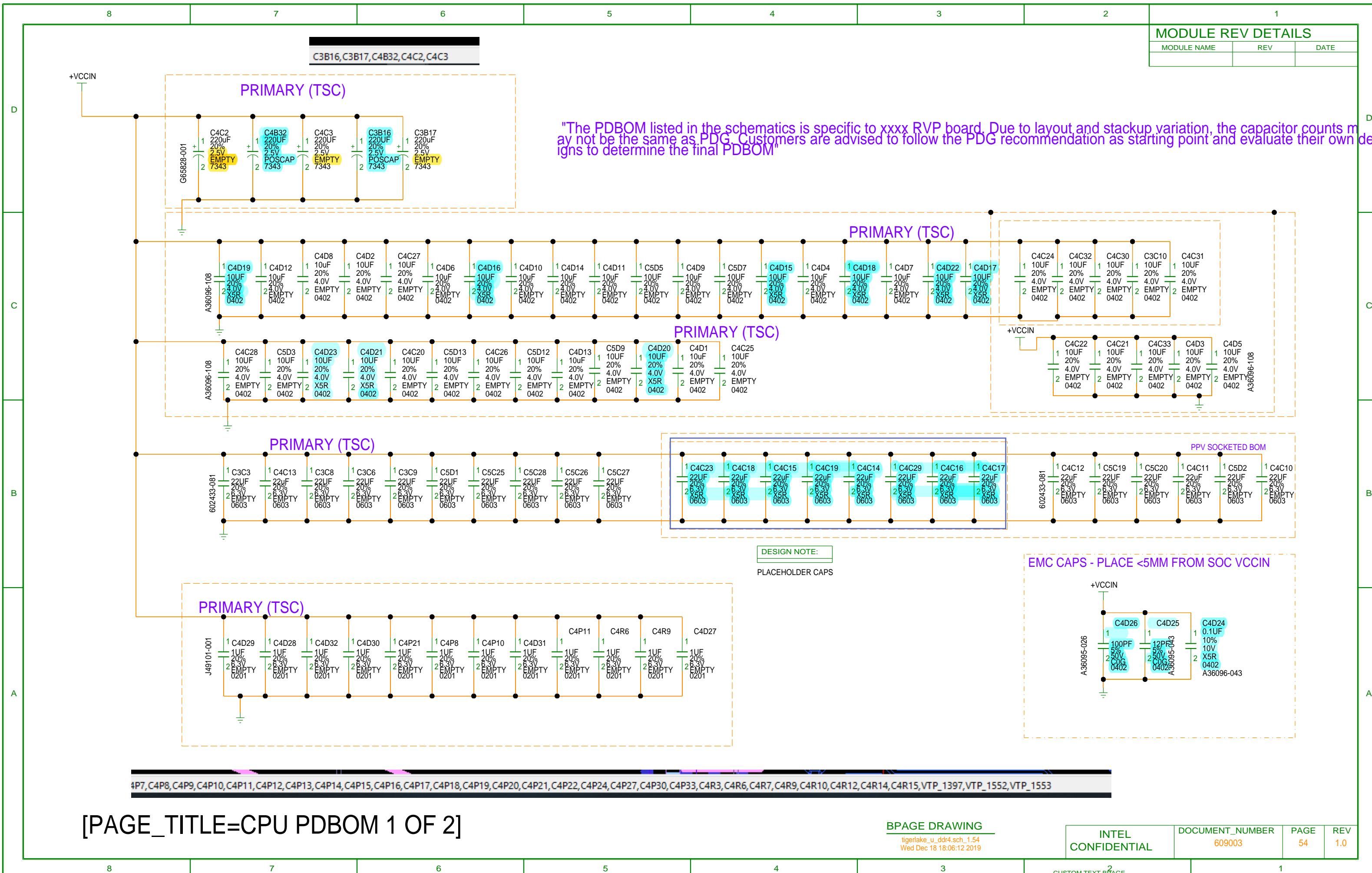
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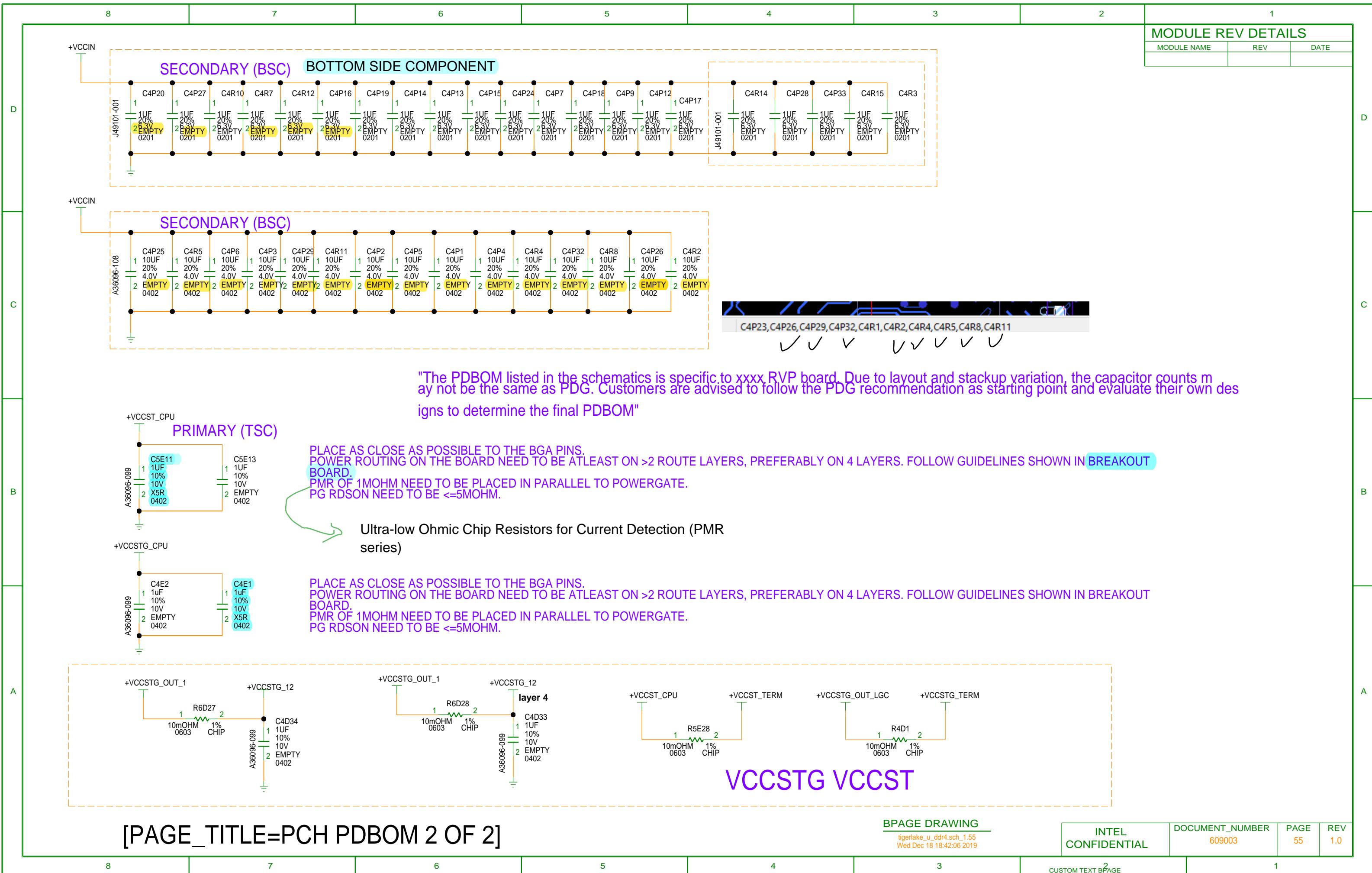
CUSTOM TEXT BPAGE

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8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				



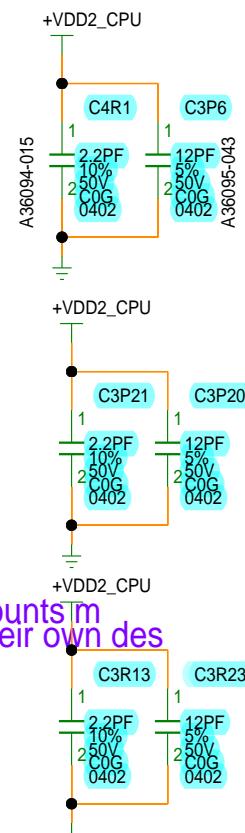




VDD2

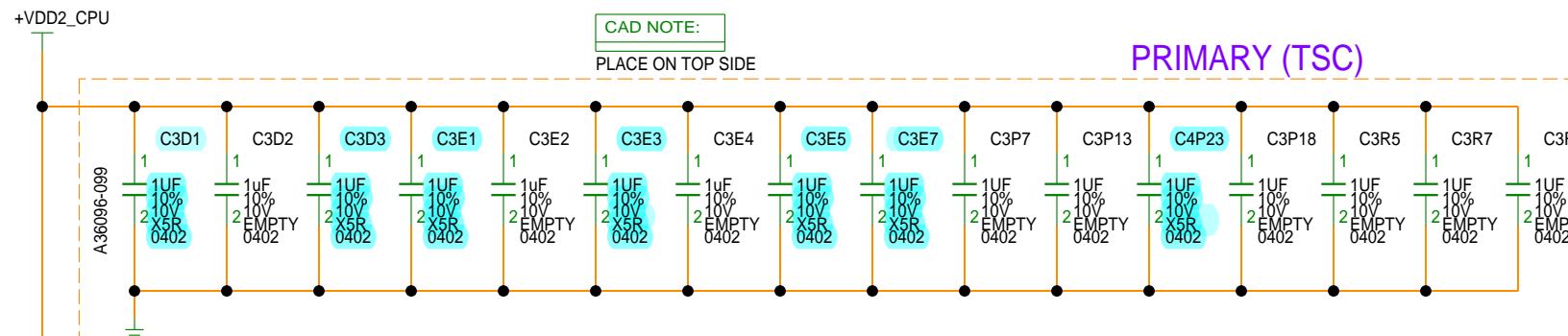
MODULE REV DETAILS		
MODULE NAME	REV	DATE

EMC CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART



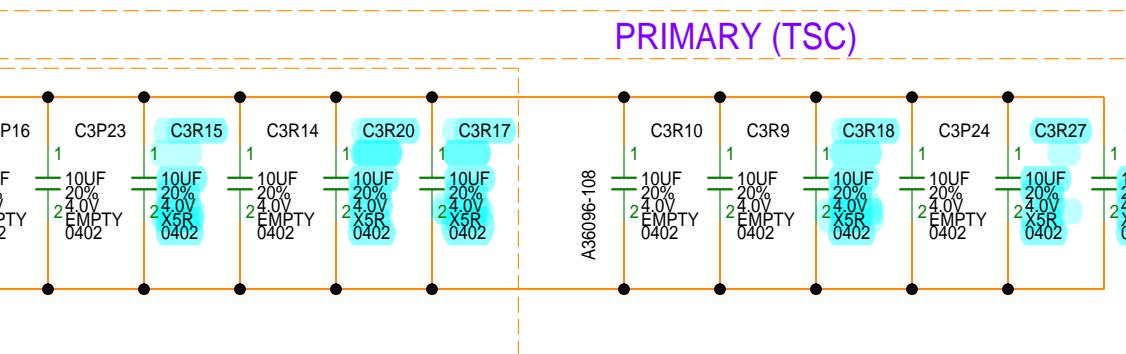
I put 10/16

PRIMARY (TSC)

CAD NOTE:
PLACE ON TOP SIDE

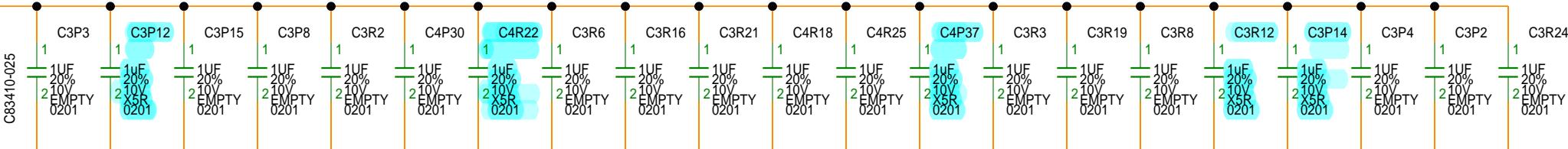
I put 12/16

PRIMARY (TSC)

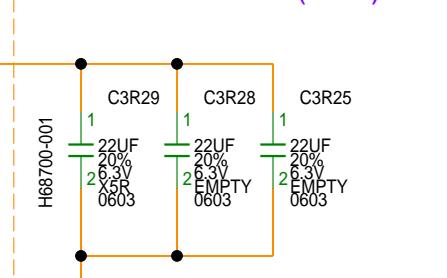
PRIMARY (TSC)
PLACE NEAR BOARD PMIC

The PDBOM listed in the schematics is specific to xxxx RVP board. Due to layout and stackup variation, the capacitor counts may not be the same as PDG. Customers are advised to follow the PDG recommendation as starting point and evaluate their own designs to determine the final PDBOM.

SECONDARY (BSC)

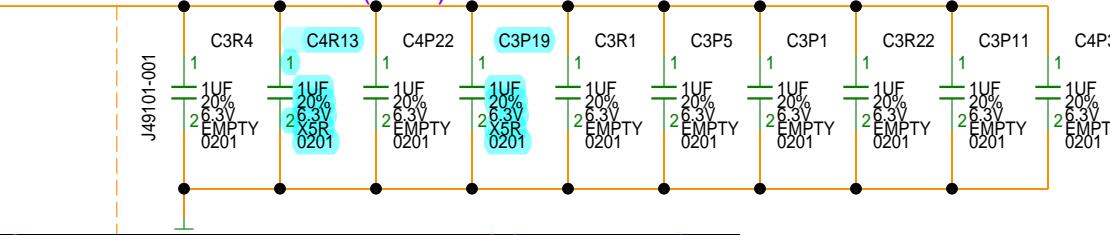


PRIMARY (TSC)



+VDD2_CPU

SECONDARY (BSC)



C3R2,C3R3,C3R6,C3R16,C3R21,C3R22,C4P30,C4P33,C4P34,C4P37,C4R3,C4R13,C4R18,C4R22,C4R25

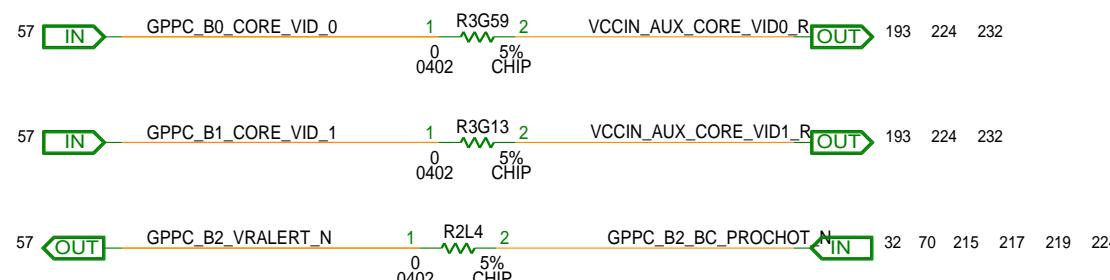
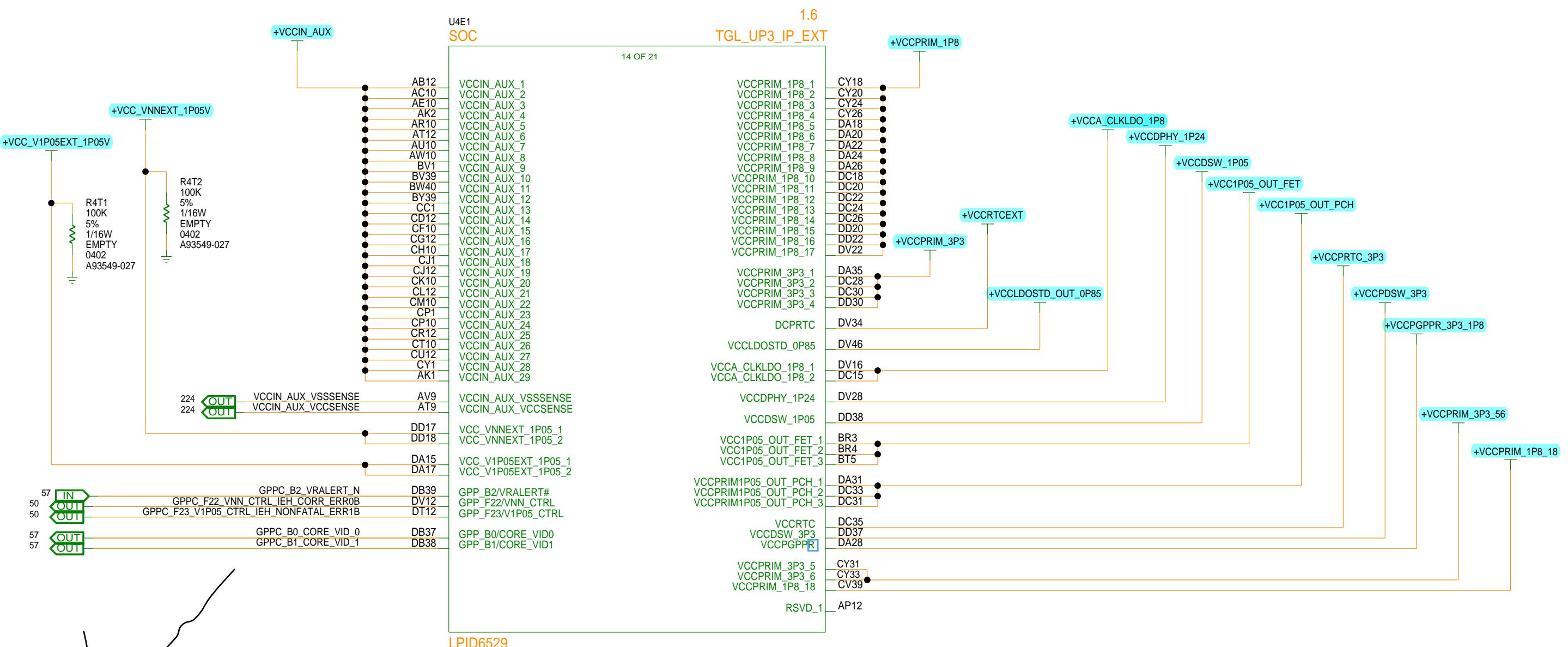
BPAGE DRAWING
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Wed Dec 18 18:06:14 2019

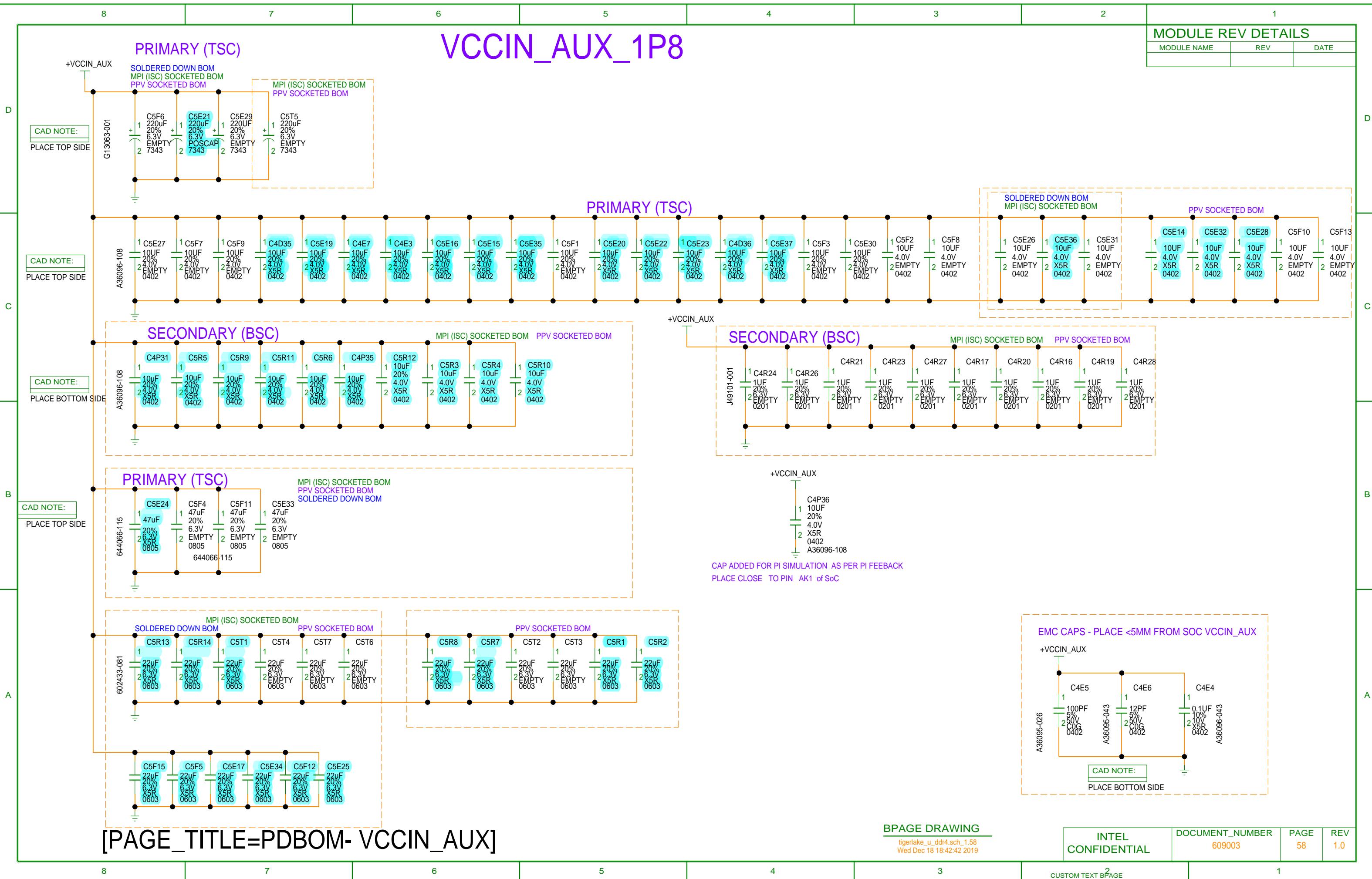
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	56	1.0

[PAGE_TITLE=CPU PDBOM 2 OF 2]

CUSTOM TEXT BPAGE

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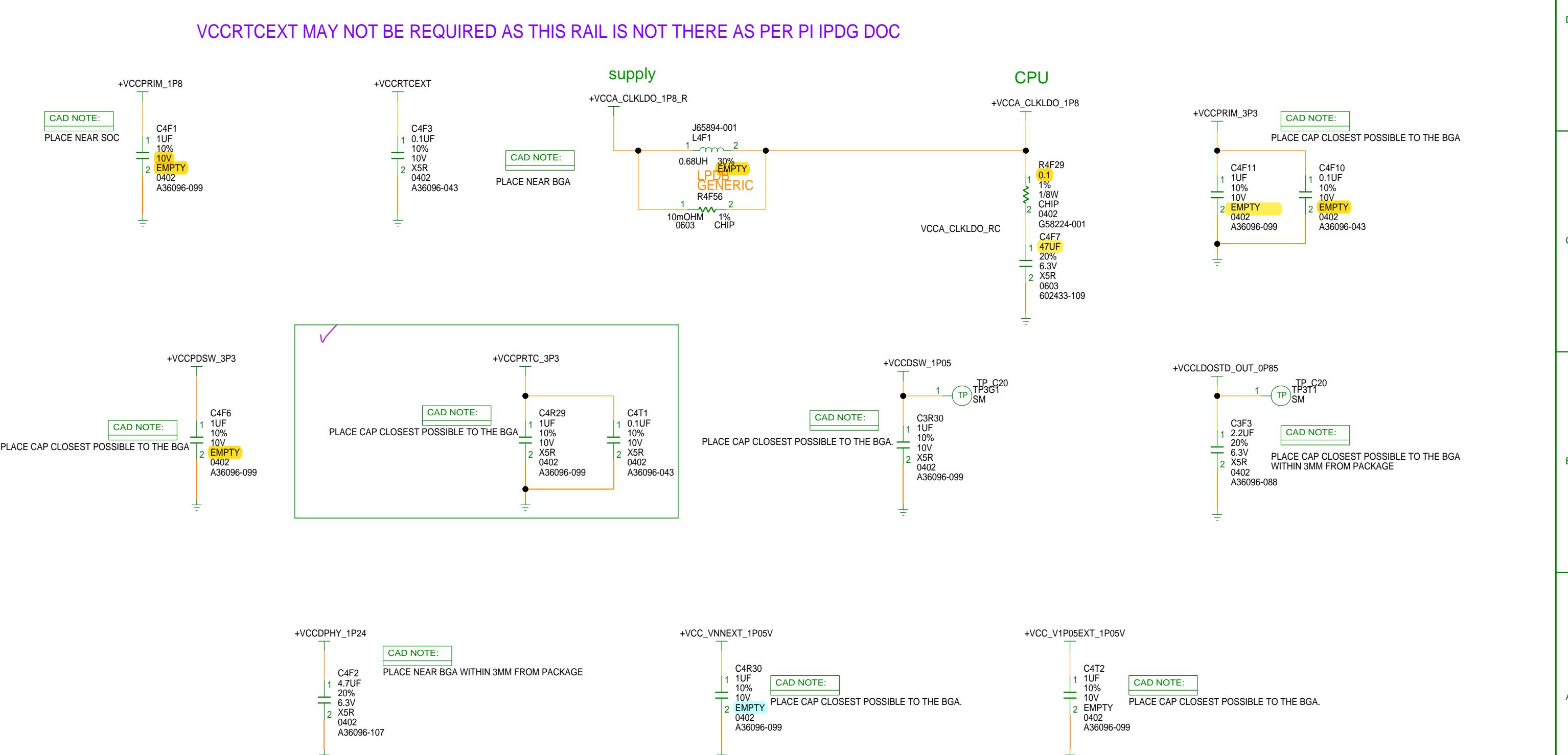


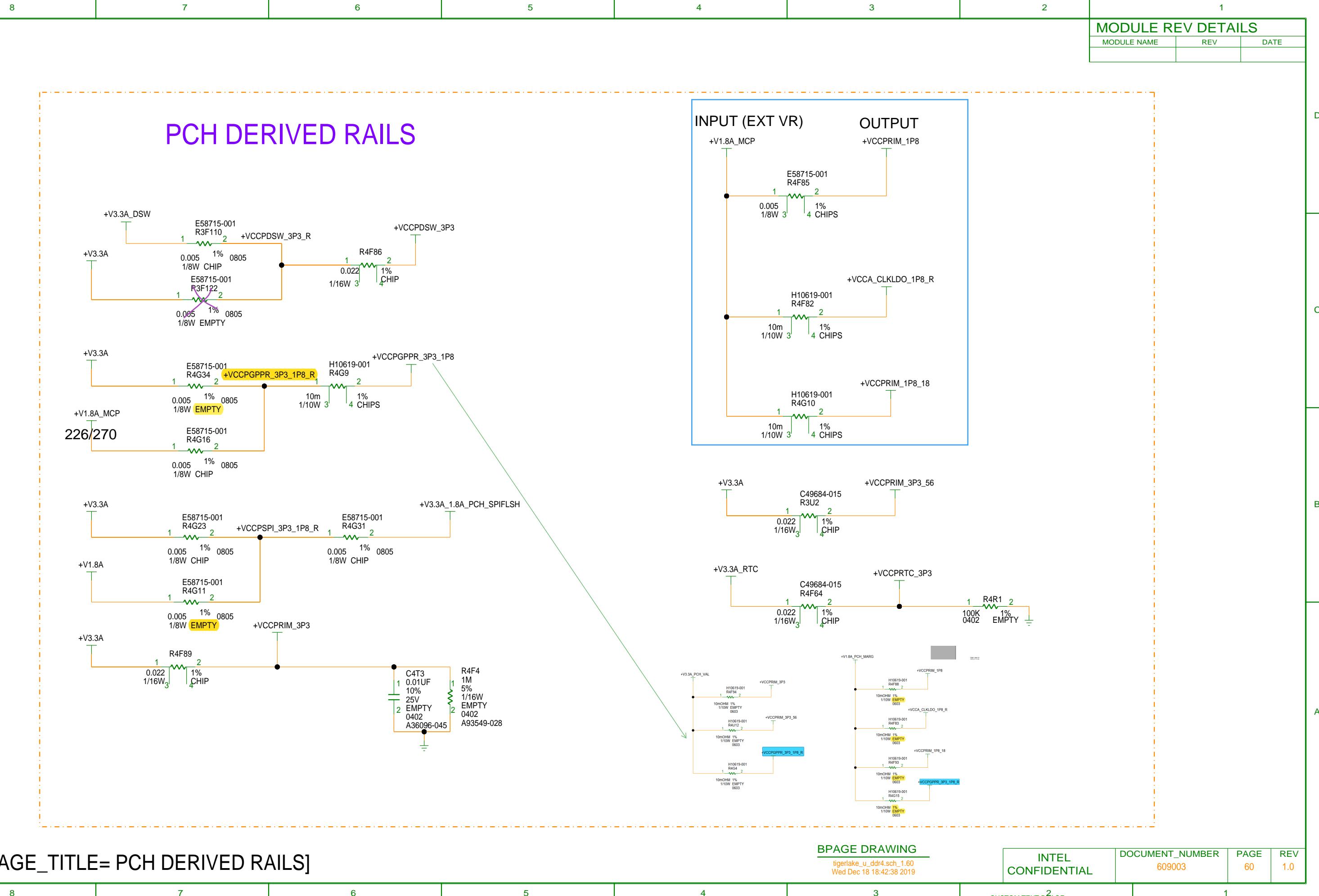


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MODULE REV DETAILS		
MODULE NAME	REV	DATE

VCCRTCEXT MAY NOT BE REQUIRED AS THIS RAIL IS NOT THERE AS PER PI IPDG DOC





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PCH MARGINING RAILS

MODULE REV DETAILS

MODULE NAME	REV	DATE

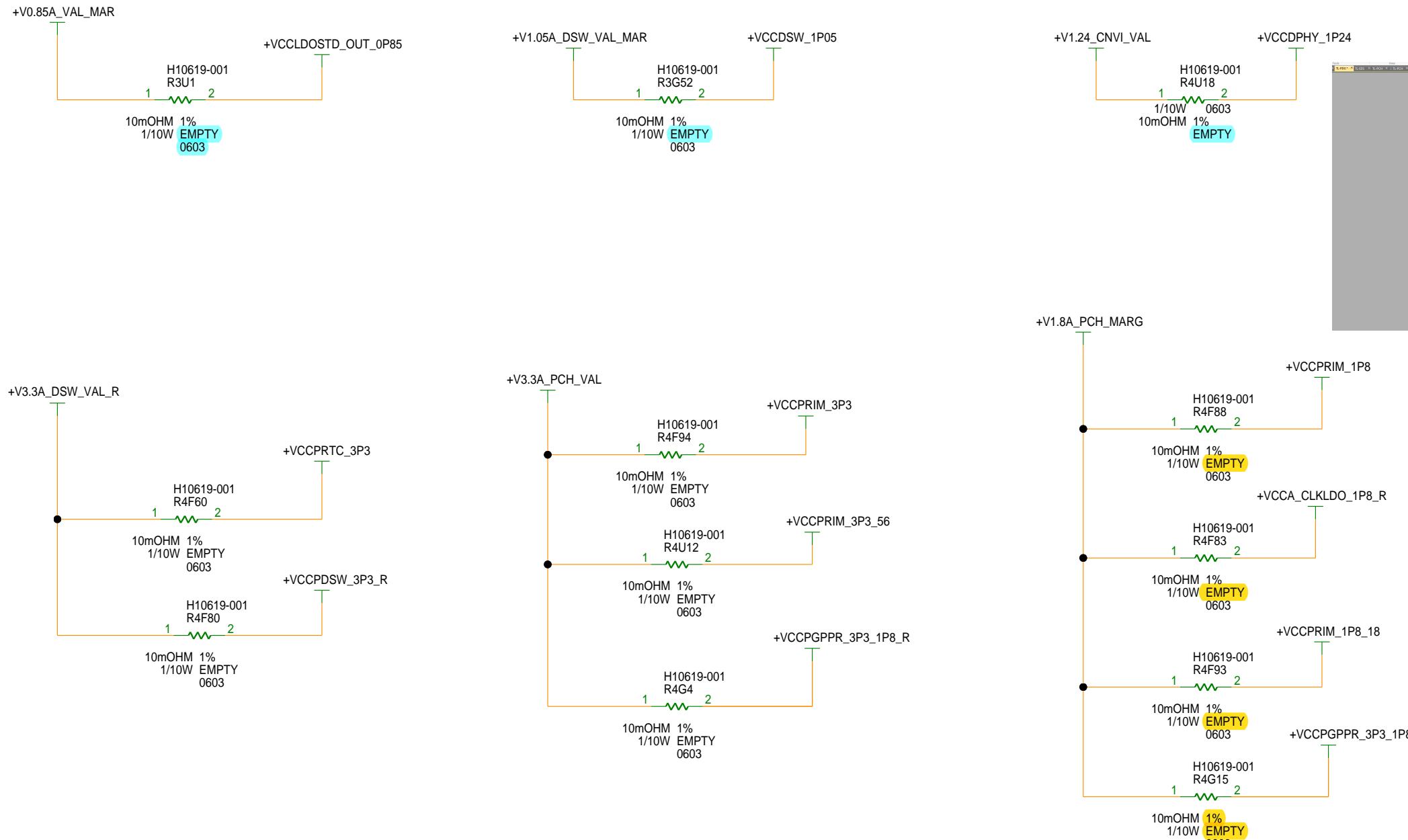


Table 237. No Direct Switching or No External Bypass Supported						
State Enable	Q1 CNVI	Q2 ISH	Q3 Type A	Q4 C-Link	Q5 SMBus	Q6 PHY PG
S02.0	Always Enable	-	-	-	-	-
S02.1	Always Enable	-	-	-	-	-
S02.2	-	-	NO	-	-	YES
S03.0	NO	NO	-	-	-	-
S03.1	NO	NO	-	-	-	-
S03.2	NO	NO	-	-	-	-
S03.3	NO	NO	NO	-	-	YES

Voltage Margining
Voltage margining allows bypass VRs to reduce their voltages depending on S03.x states. To enable this feature, VNN_CTRL and V1P05_CTRL GPIO pins should be configured. This feature can reduce power in Soix states.

Tiger Lake UP3 UP4 H35 UP3 Refresh Platform

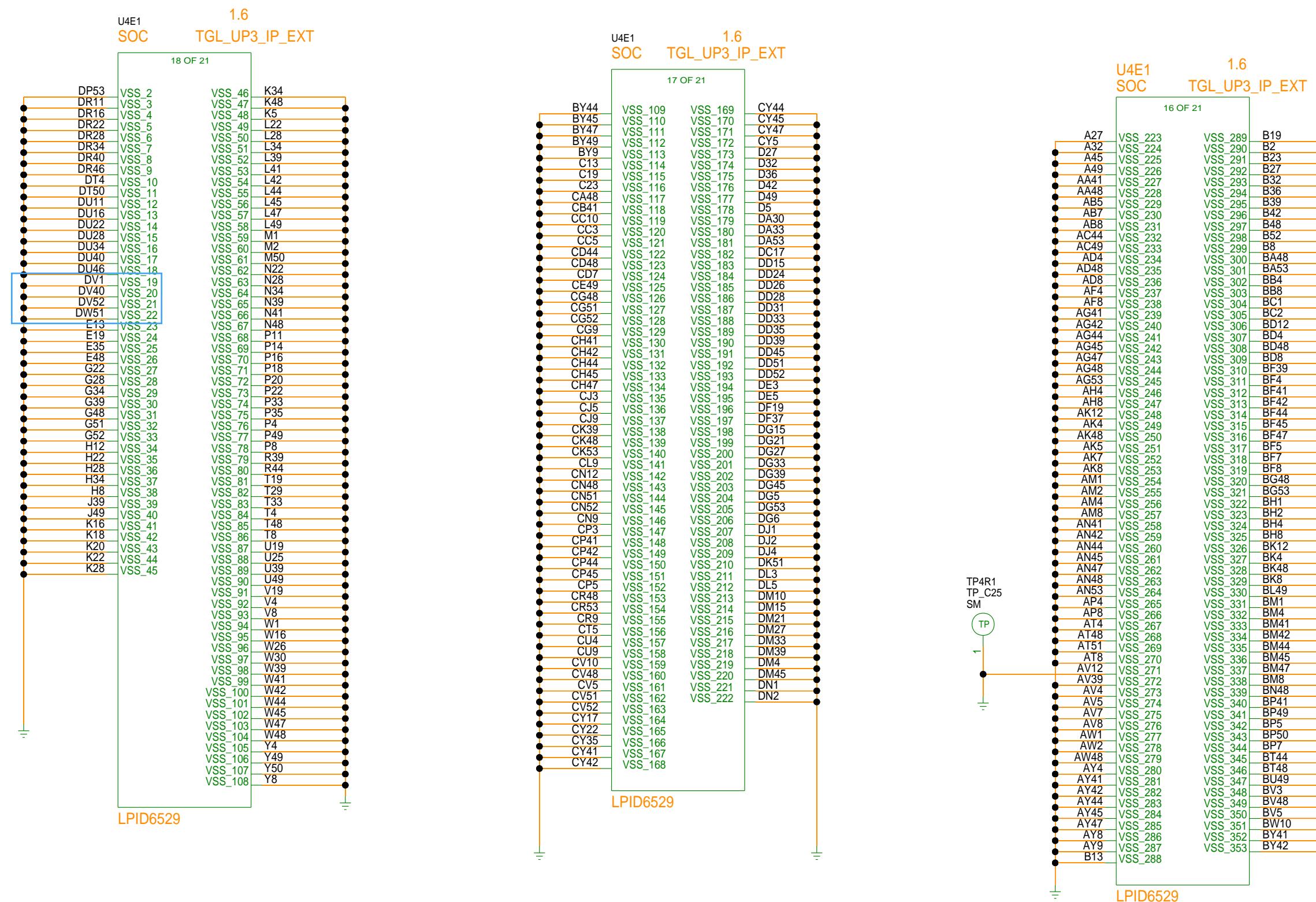
Document ID: 00000000000000000000000000000000

November 2020

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MODULE REV DETAILS

MODULE NAME	REV	DATE



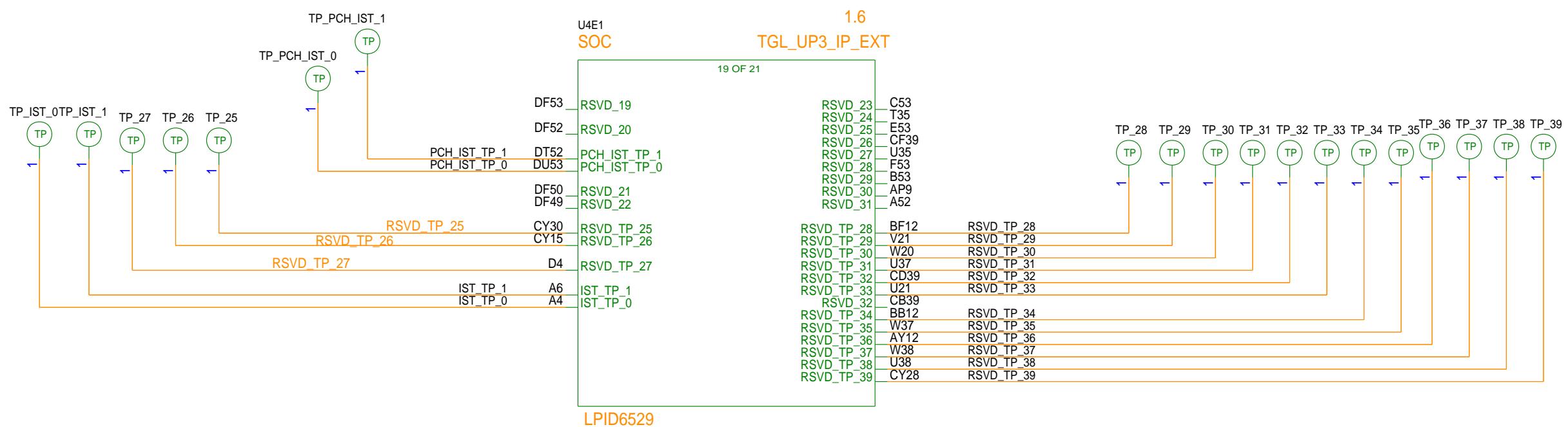
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE_TITLE=TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.62
Wed Dec 18 18:06:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 62	REV 1.0
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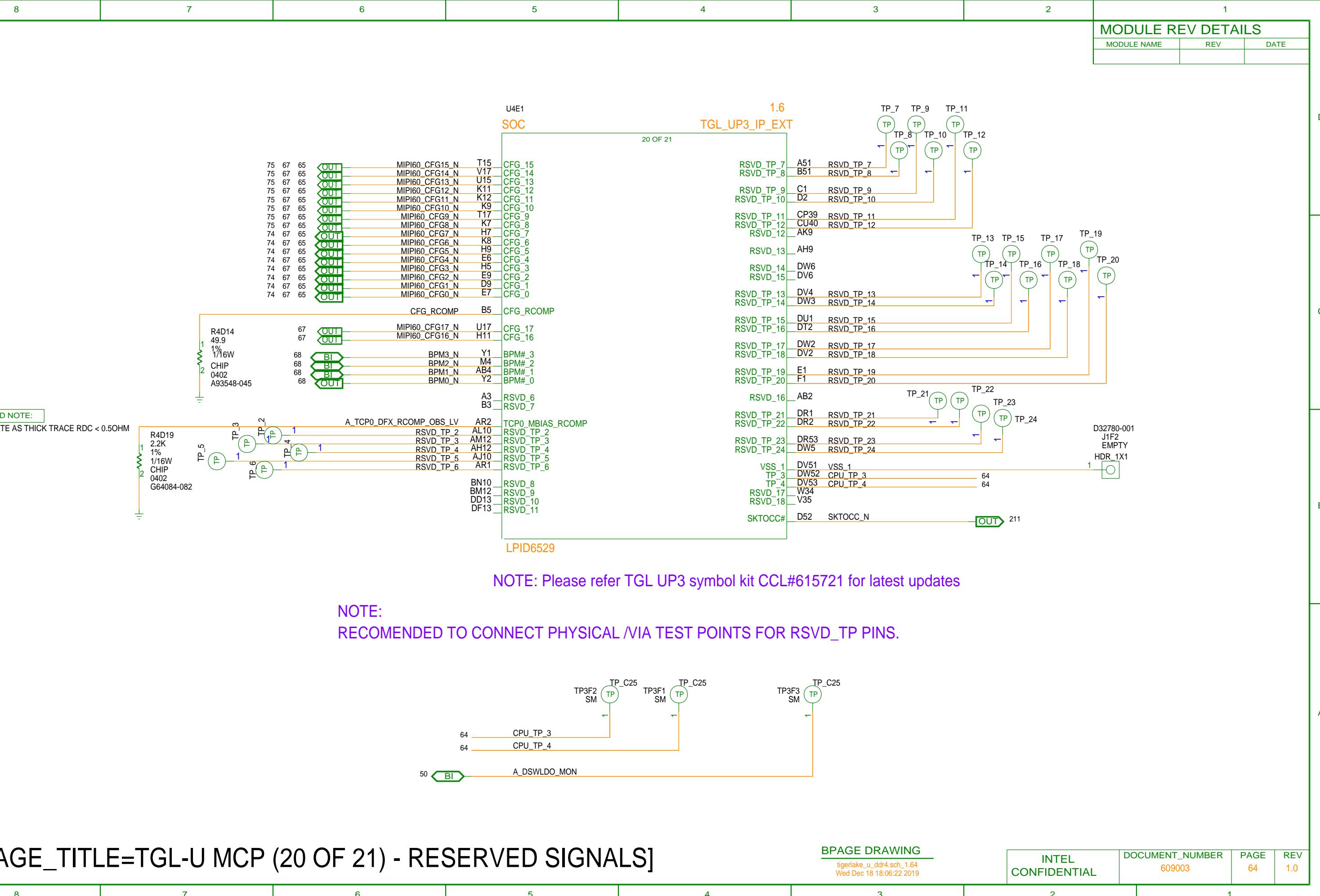
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MODULE REV DETAILS							



NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

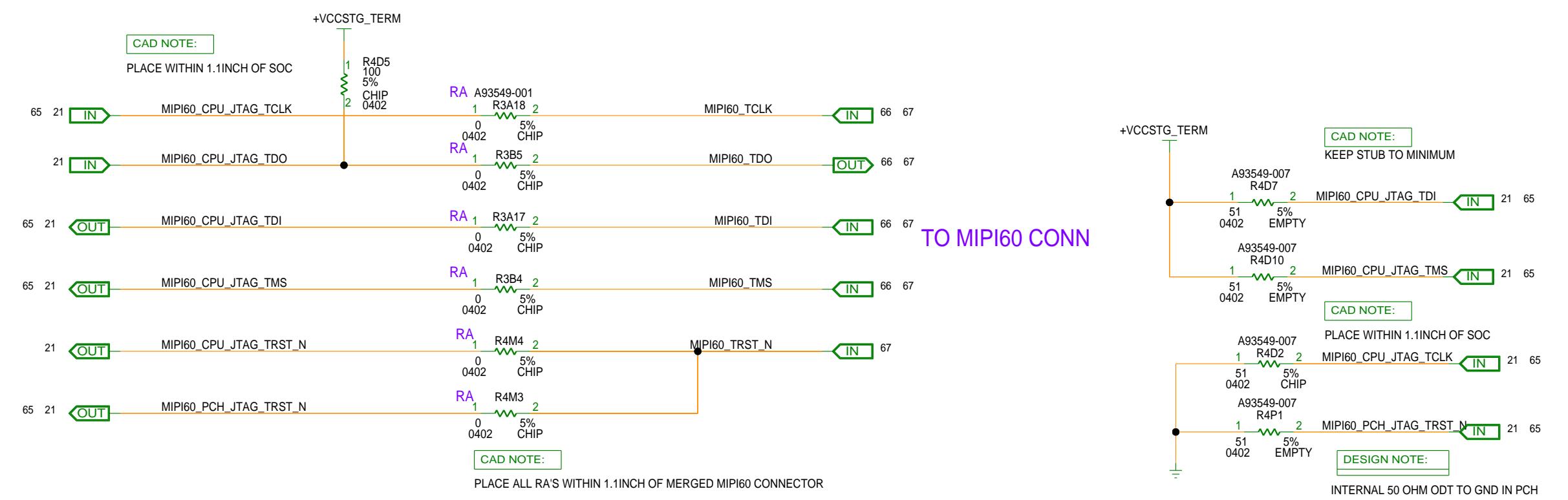
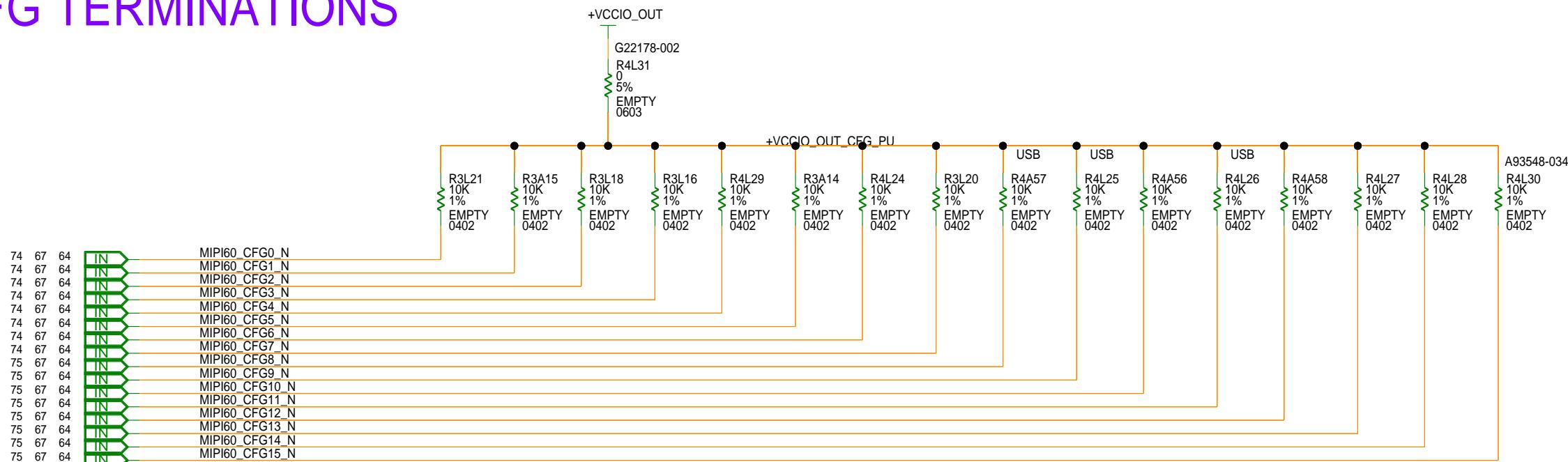
NOTE:

RECOMENDED TO CONNECT PHYSICAL /VIA TEST POINTS FOR RSVD_TP PINS.



8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME	REV	DATE					

CFG TERMINATIONS



[PAGE_TITLE=JTAG/CFG - CFG TERMINATIONS]

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.65
Wed Dec 18 18:06:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	65	1.0

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

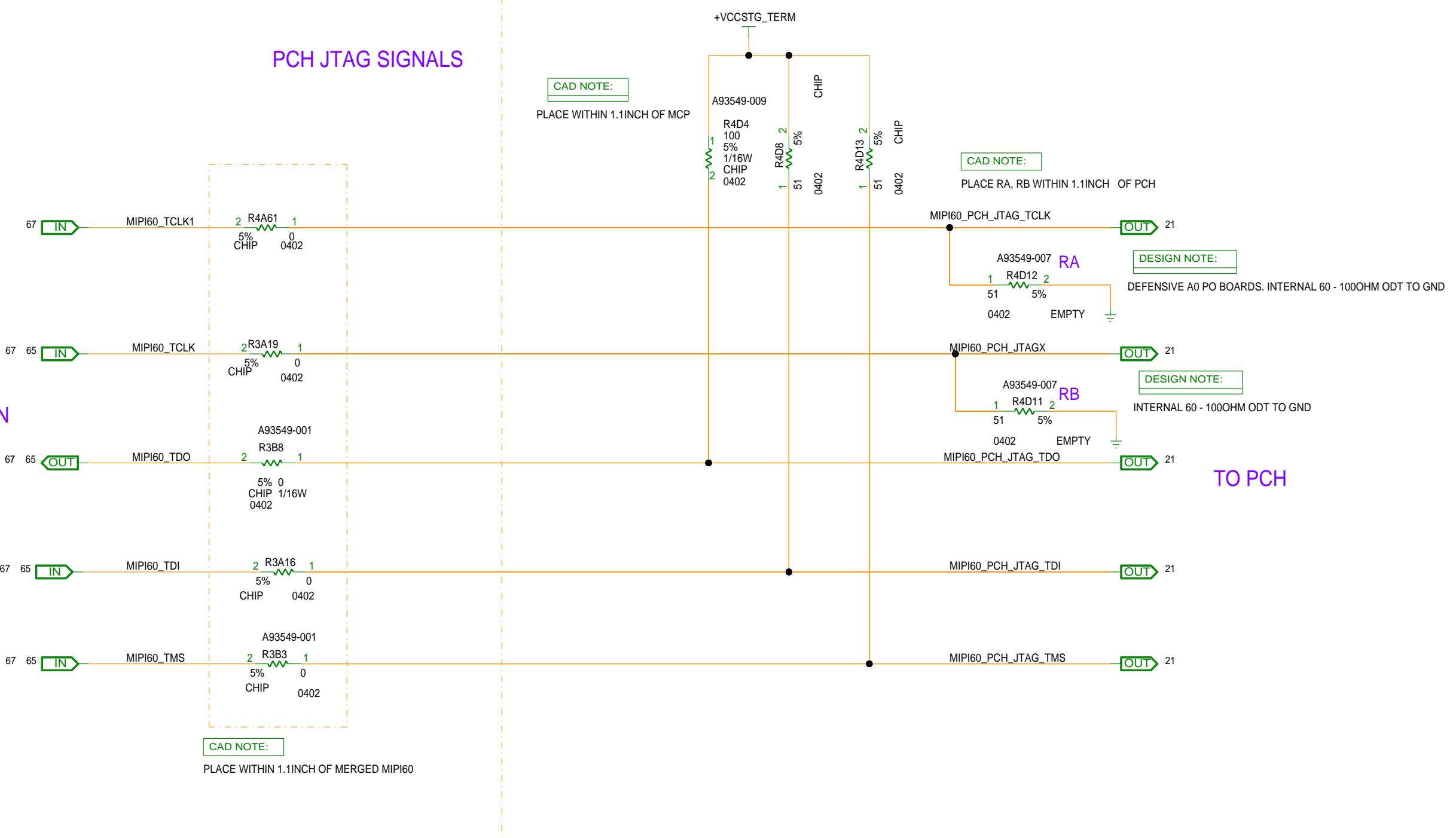
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PCH JTAG SIGNALS

TO MIPI60 CONN

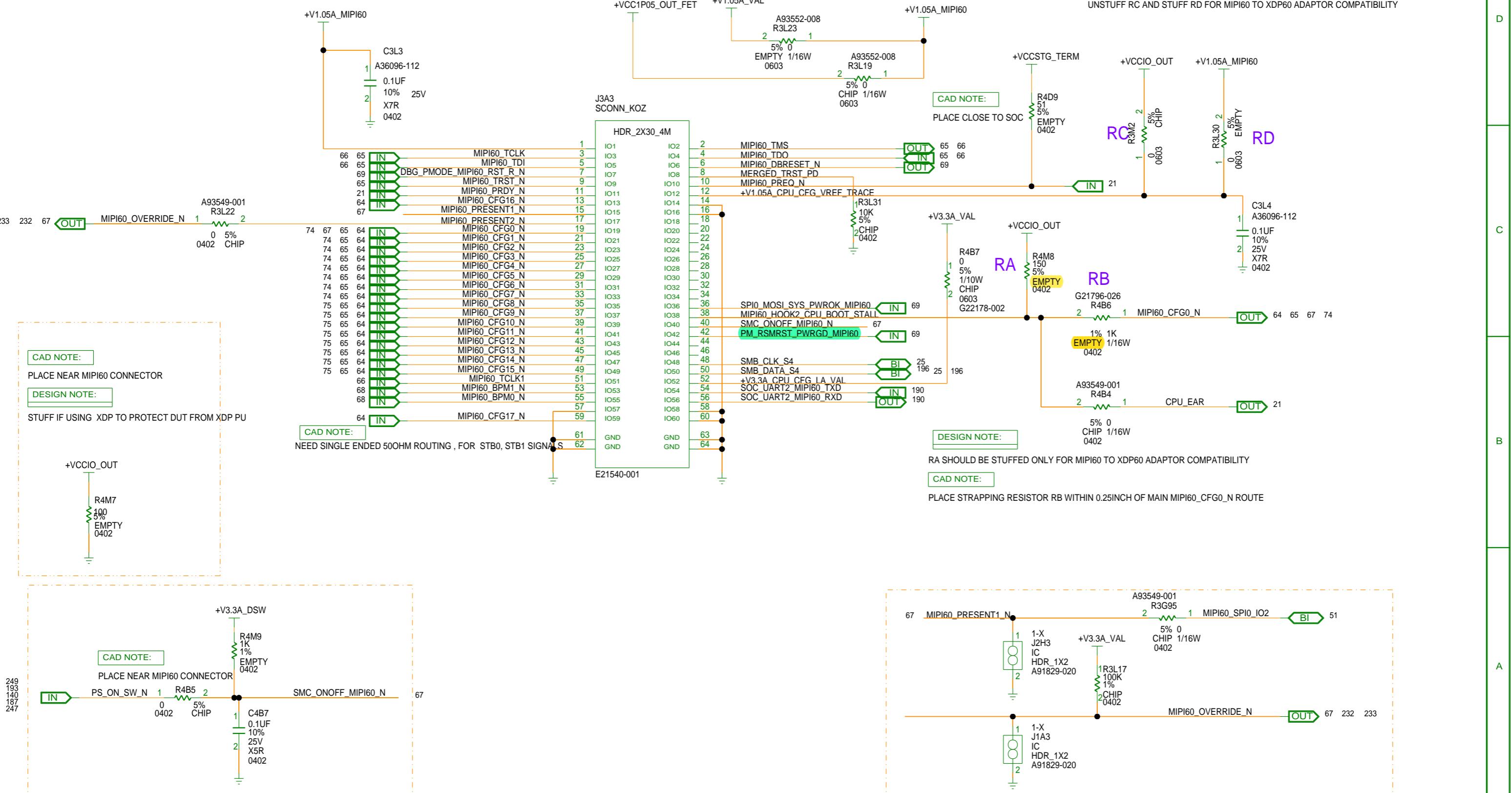
TO PCH

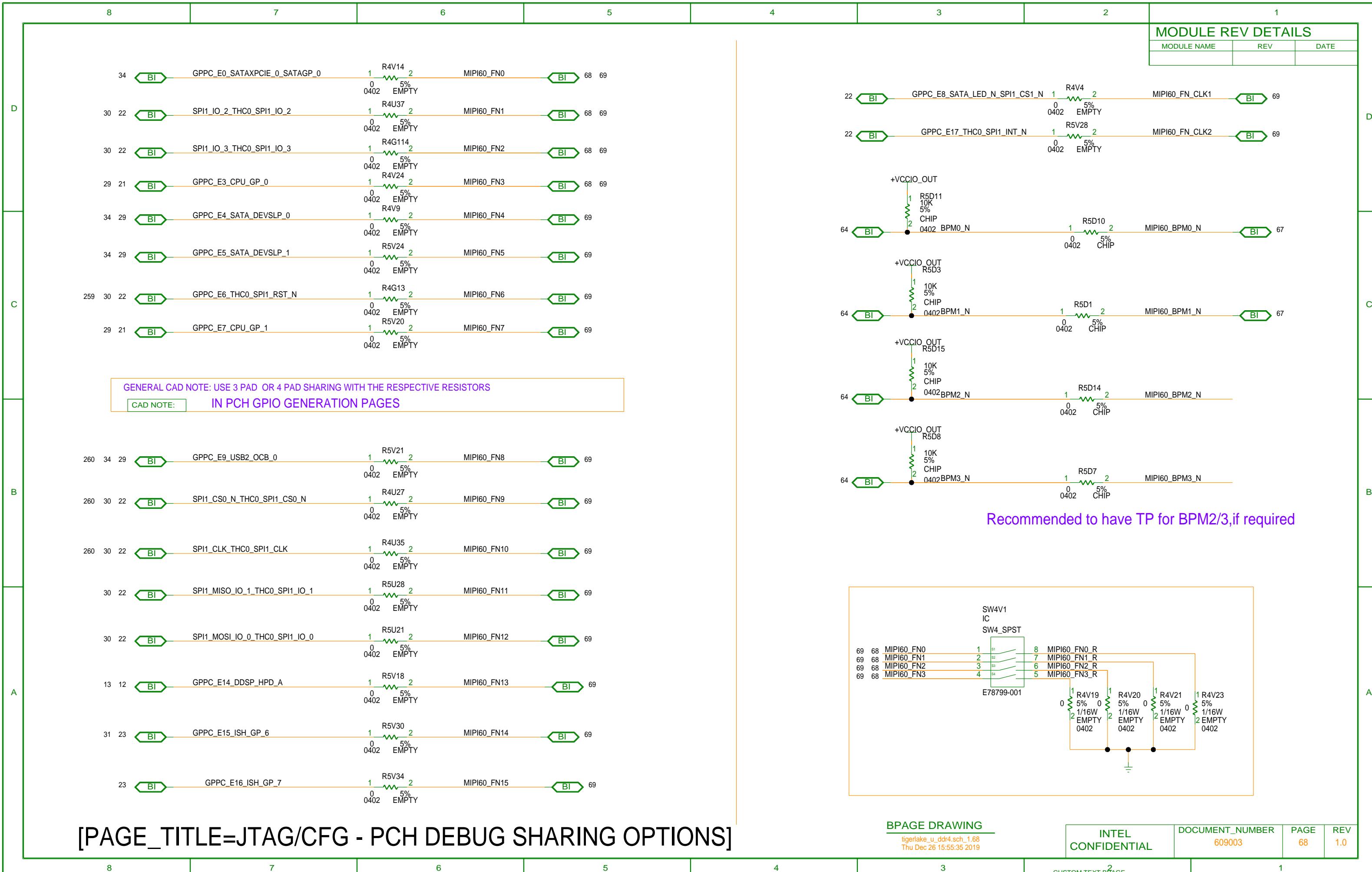


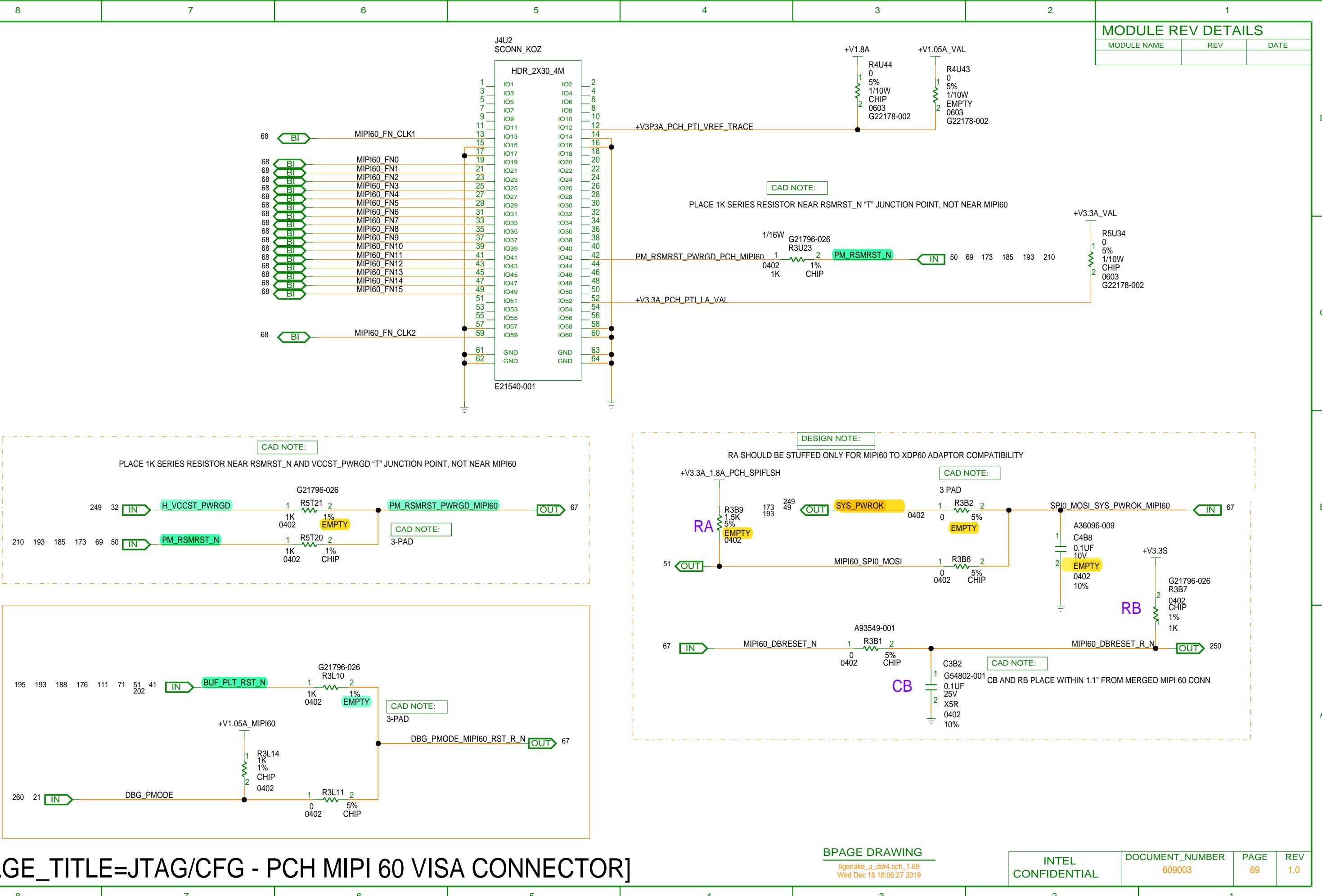
MIPI 60

MODULE REV DETAILS

MODULE NAME	REV	DATE





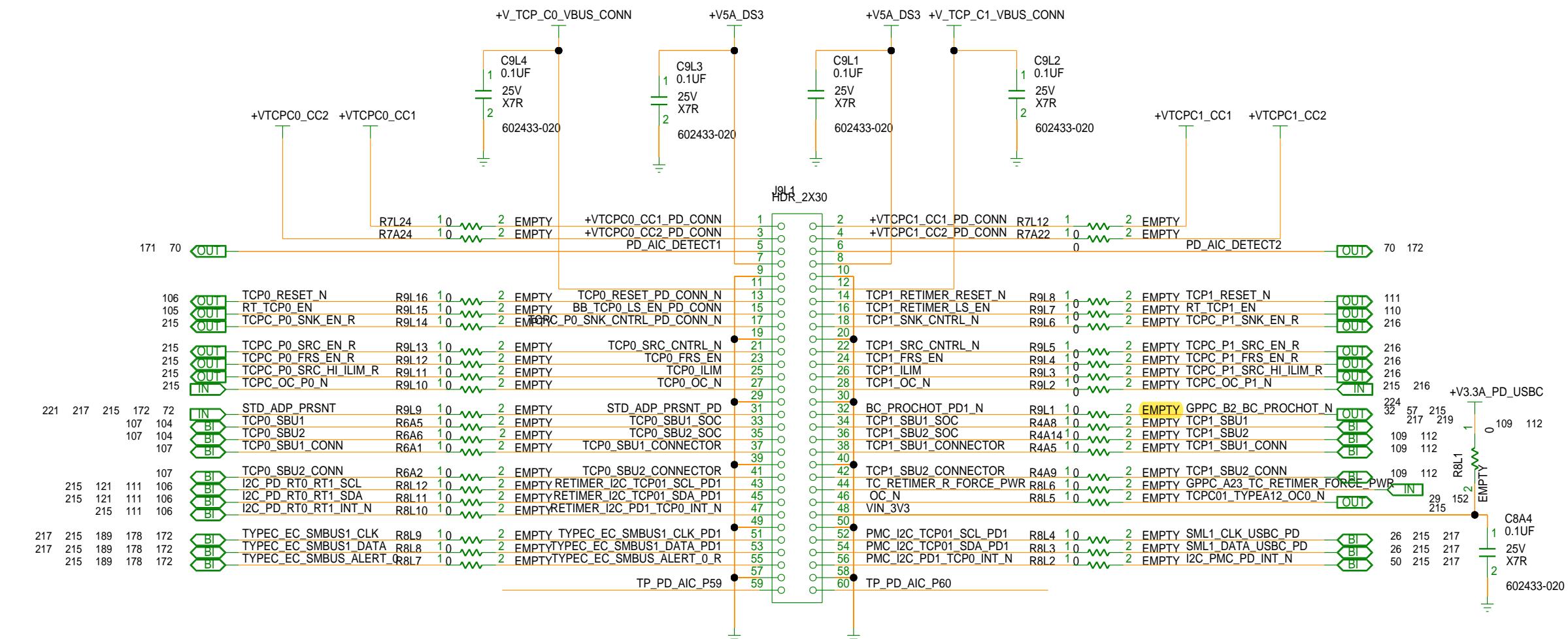


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PD AIC CONTROLLER

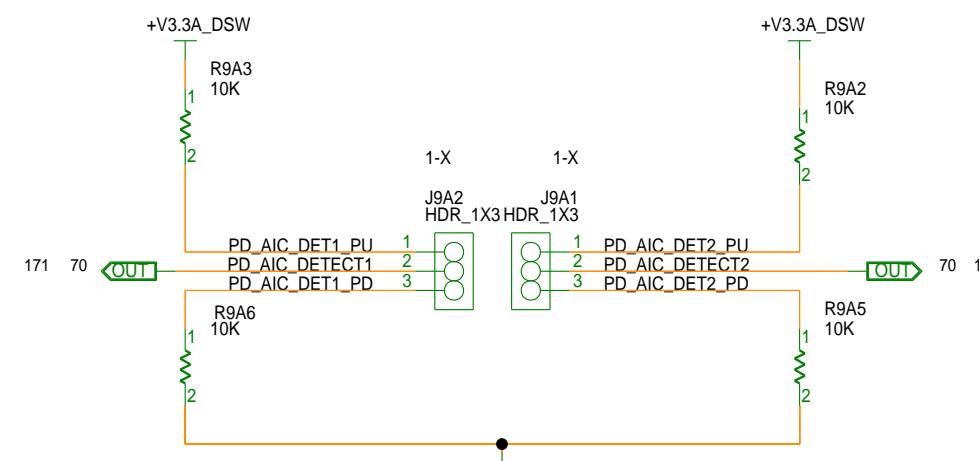
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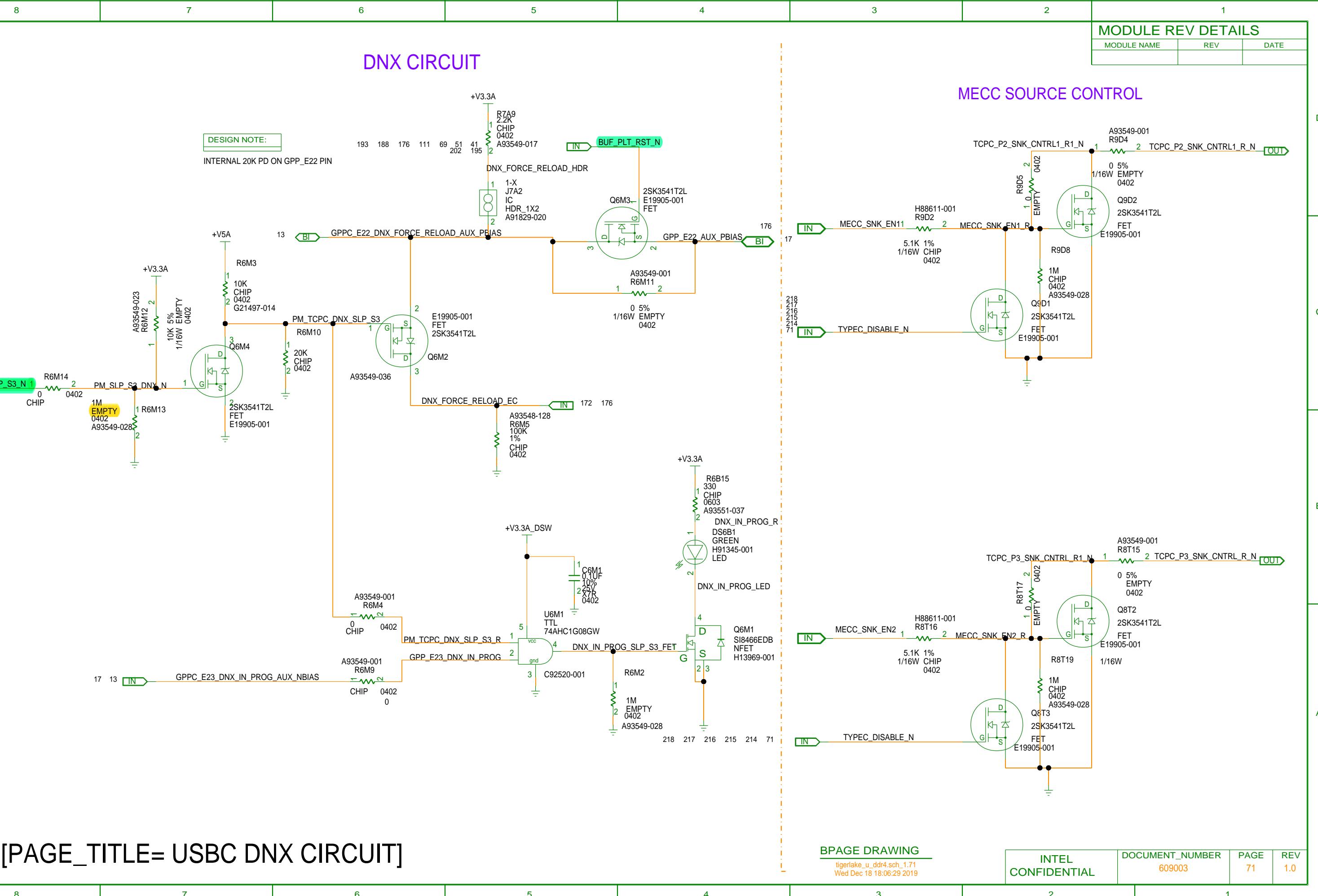
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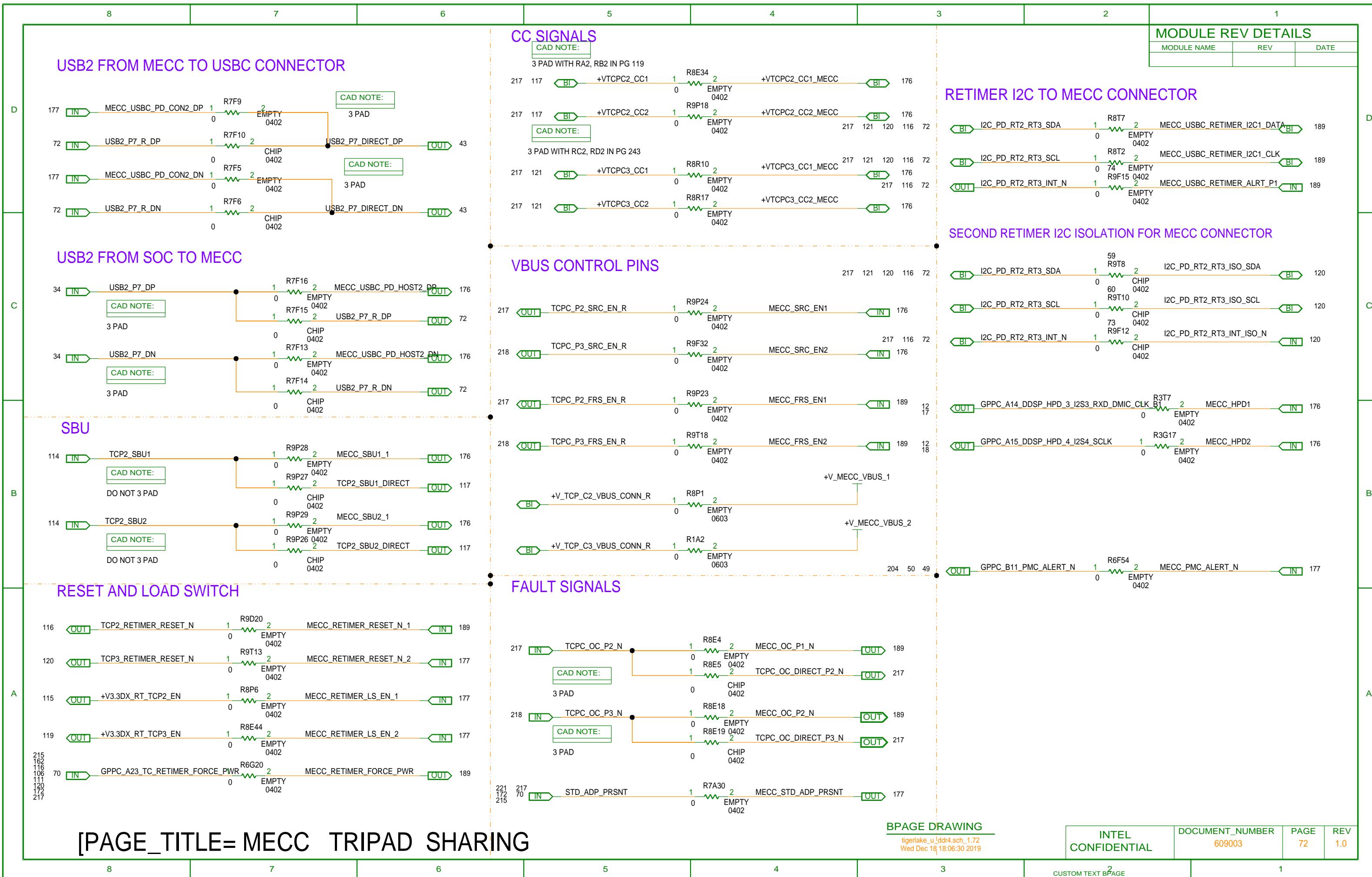


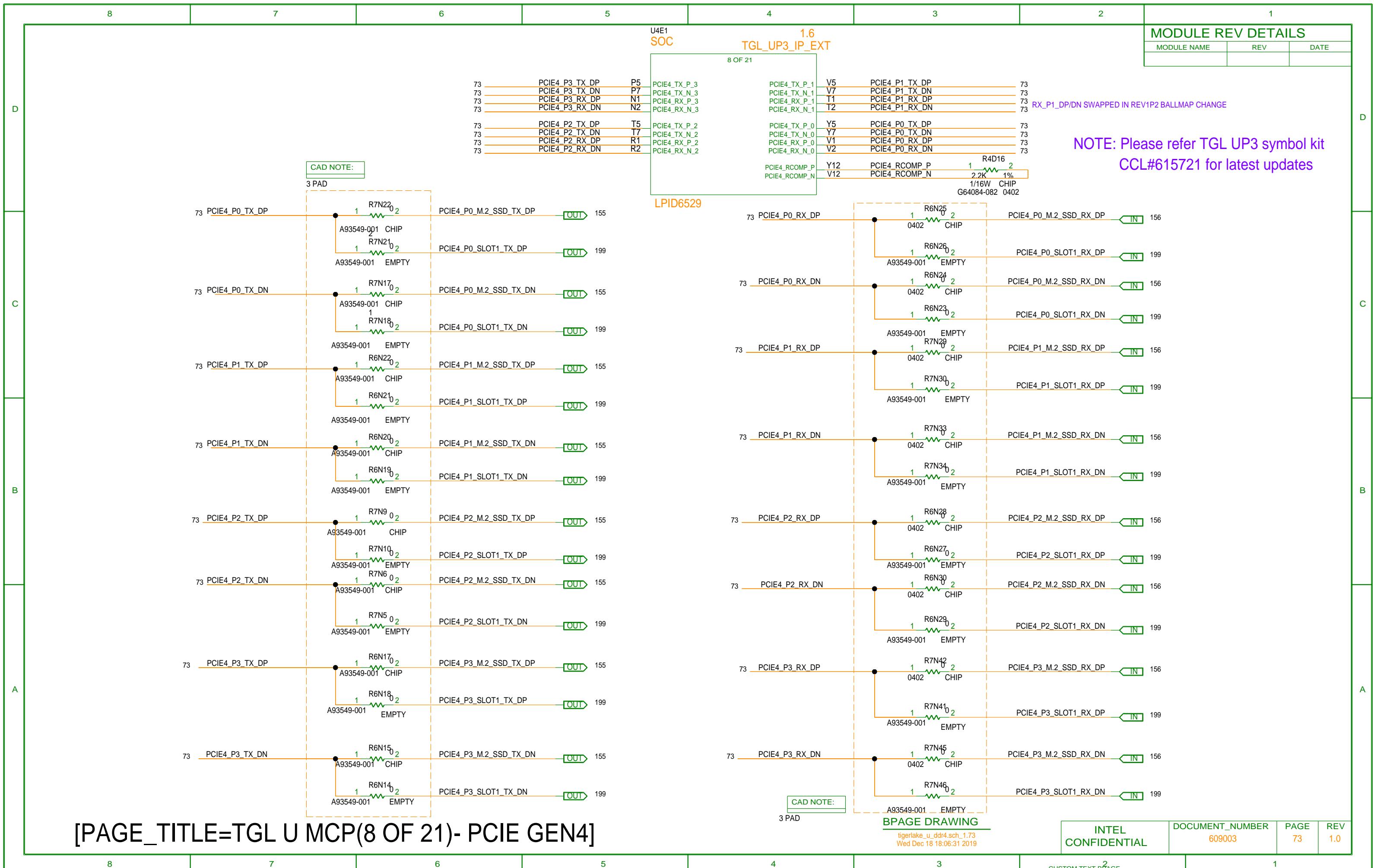
CAD NOTE:

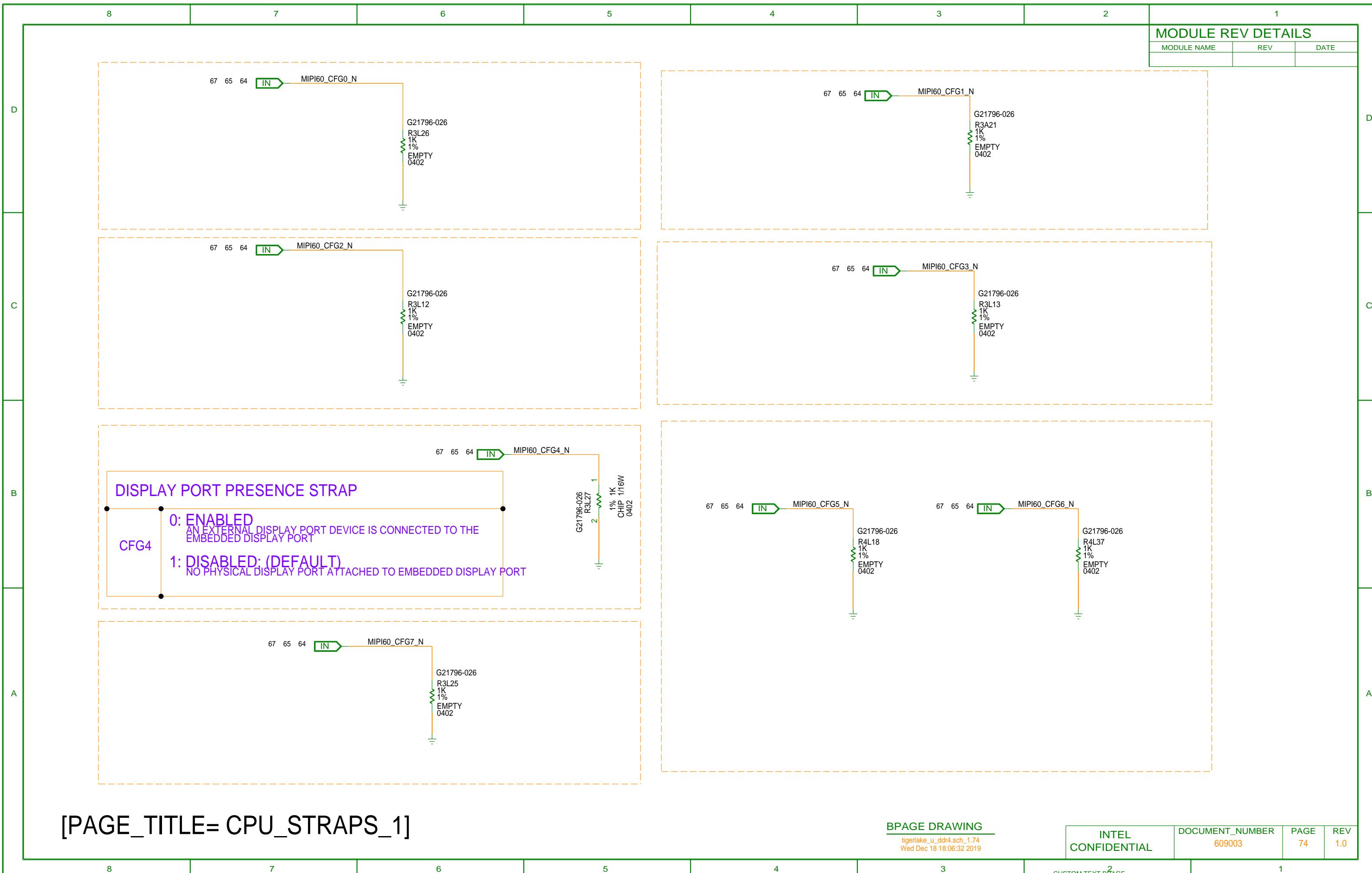
ALL THE RESISTORS IN THIS PAGE SHOULD BE TRIPAD WITH RESPECTIVE RESISTOR IN OTHER SECTION

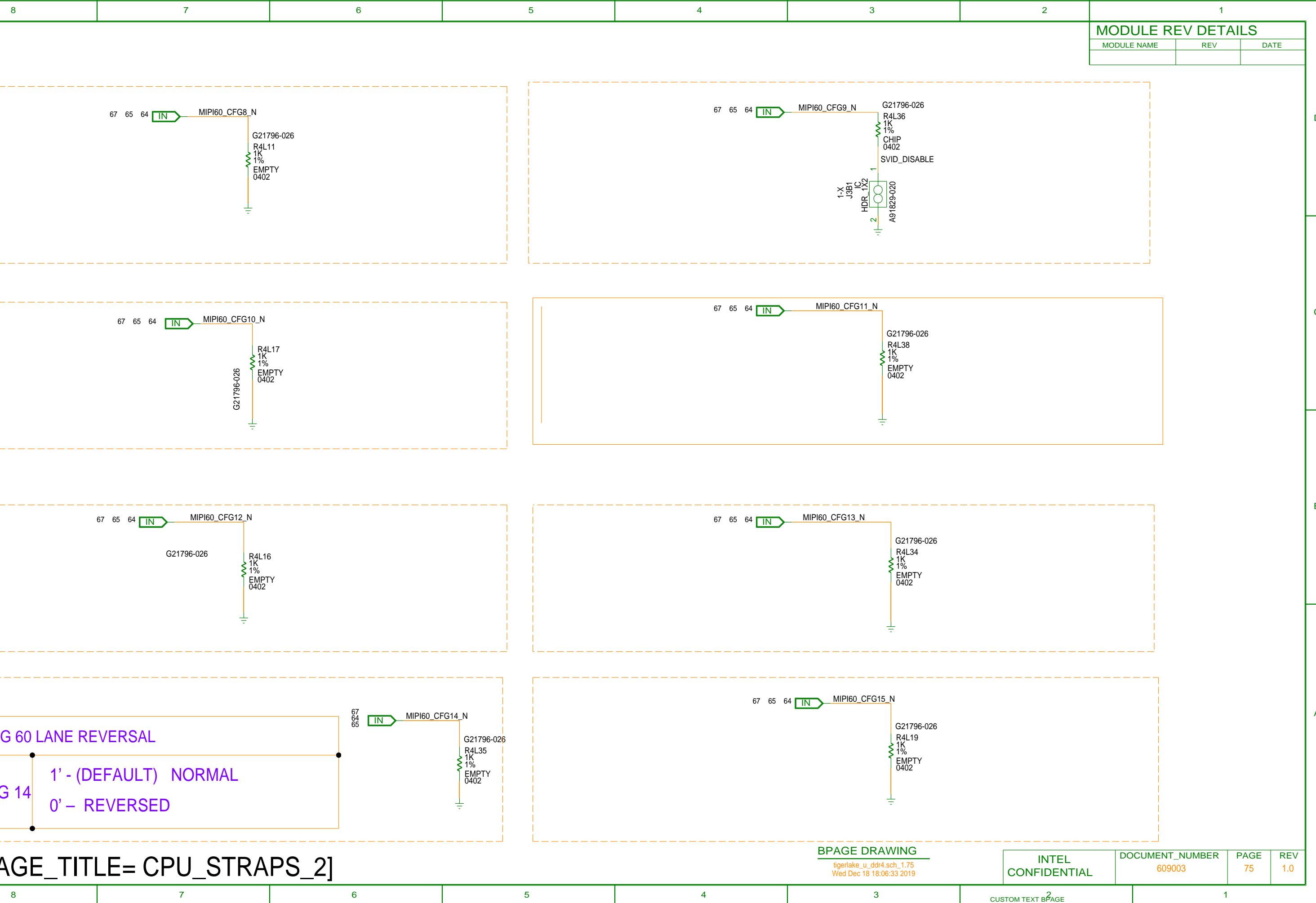






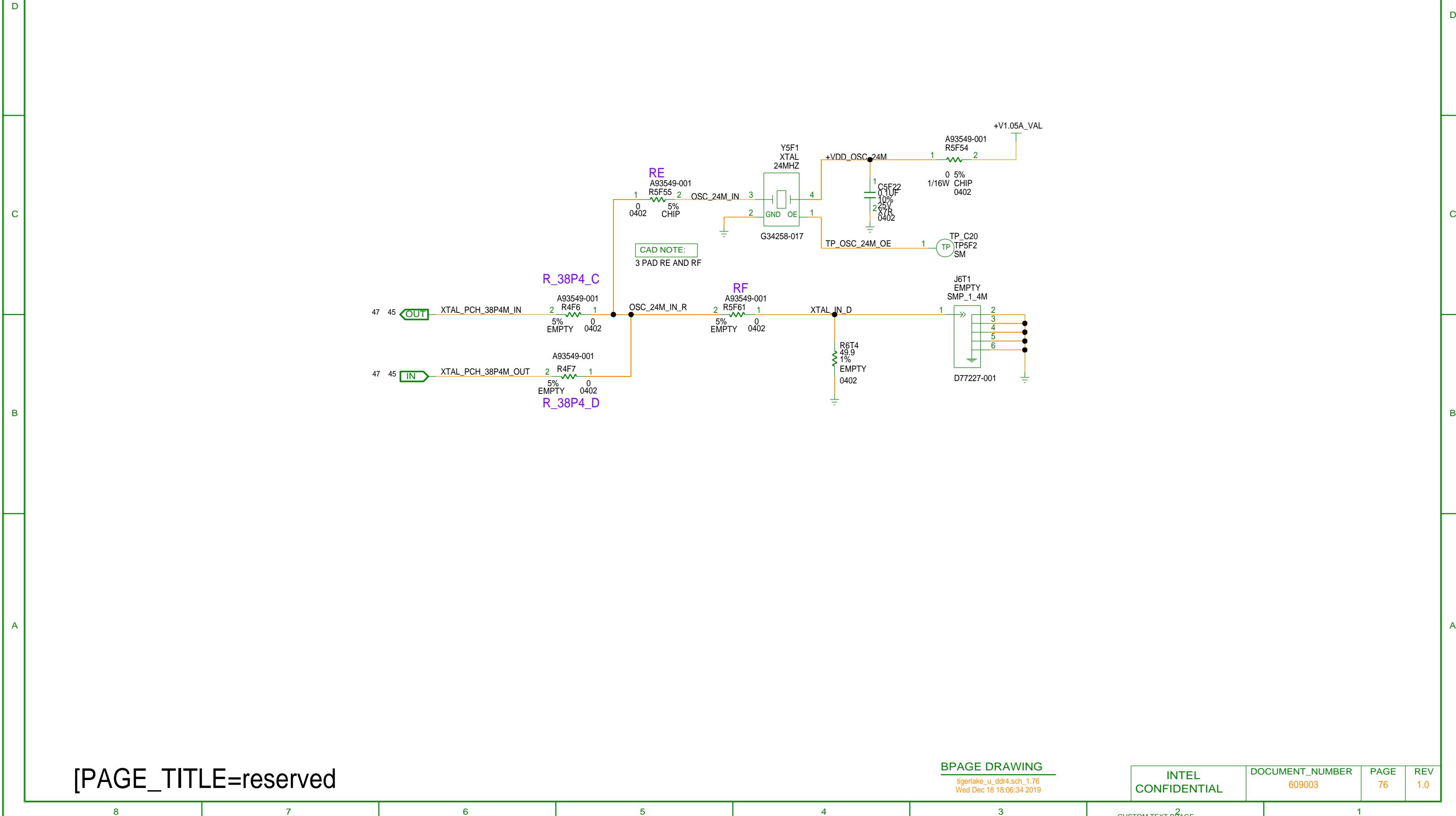






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MODULE REV DETAILS		
MODULE NAME	REV	DATE



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Wed Dec 18 18:06:34 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	76	1.0

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CUSTOM TEXT BPAGE

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MODULE REV DETAILS

MODULE NAME	REV	DATE

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tigerlake_u_ddr4.sch_1.77
Tue Oct 15 12:49:33 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	77	1.0

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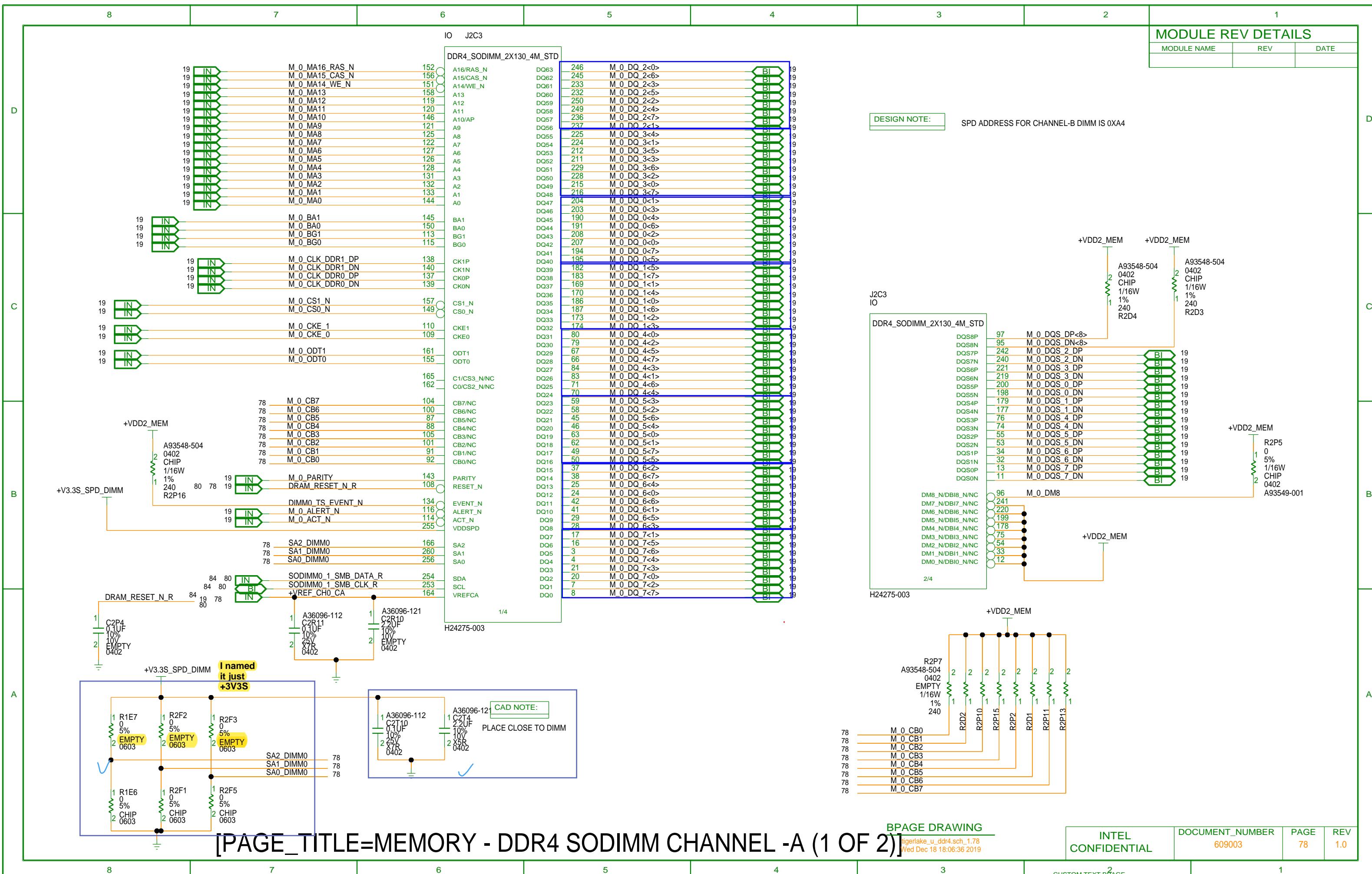
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CUSTOM TEXT ²BPAGE

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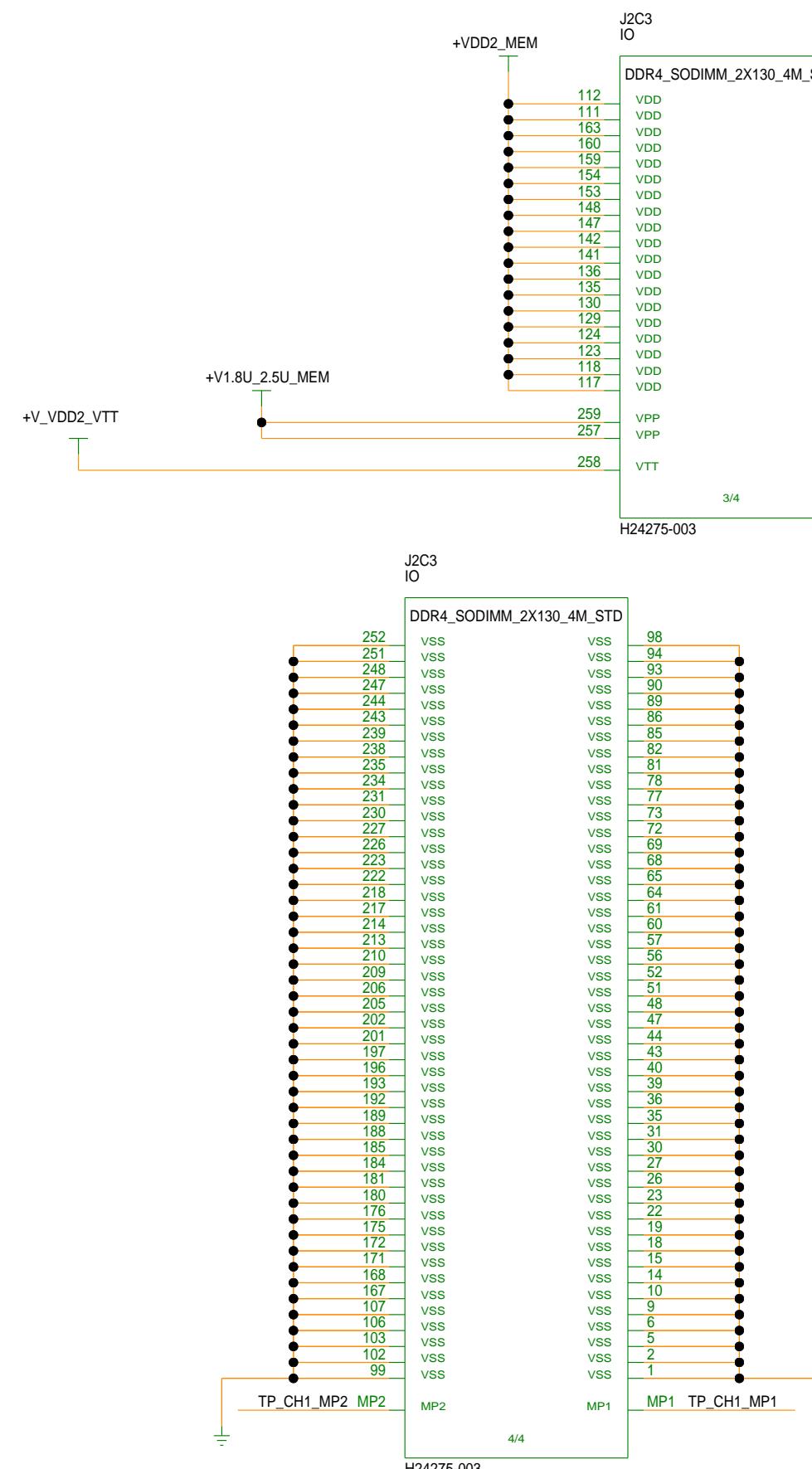
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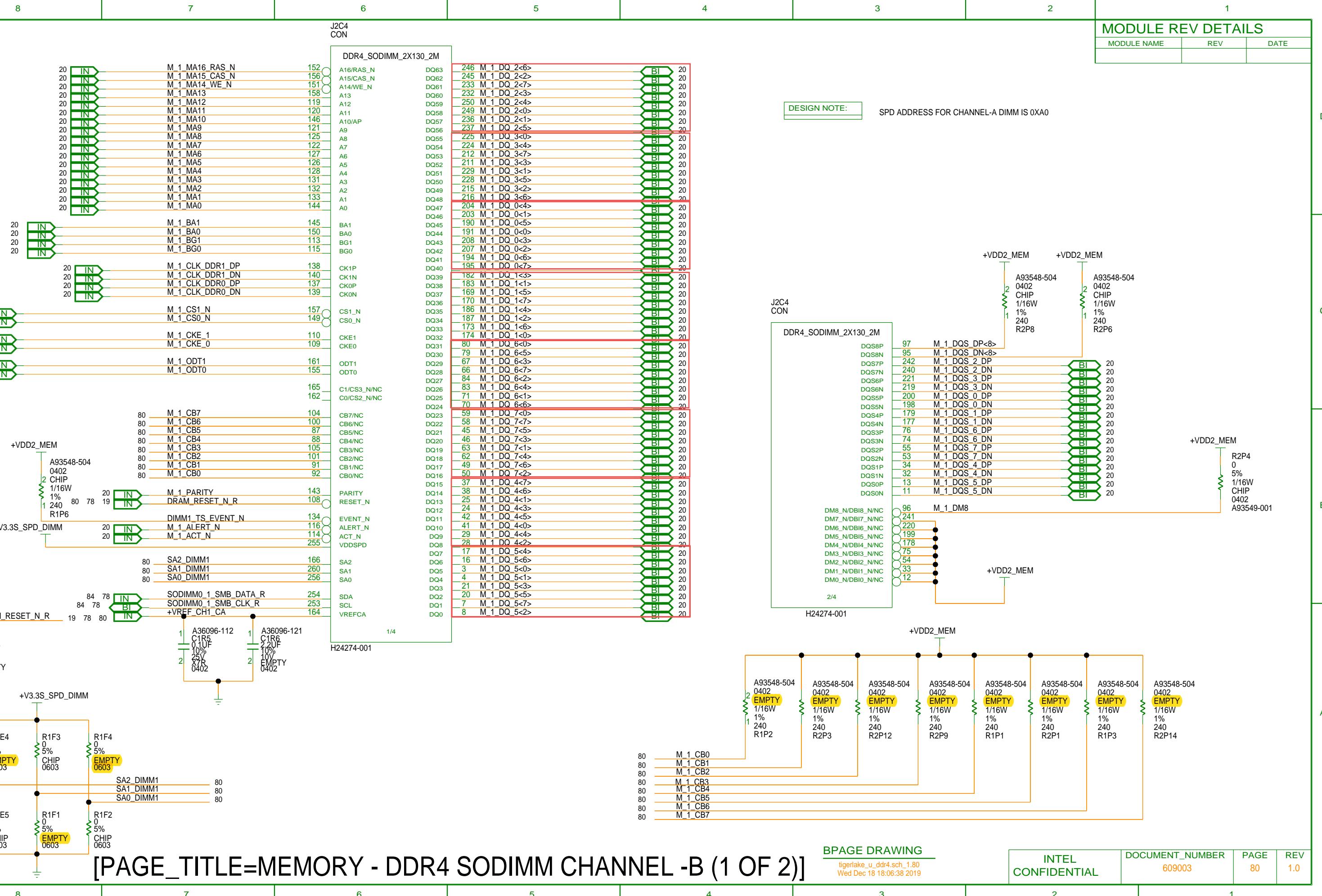
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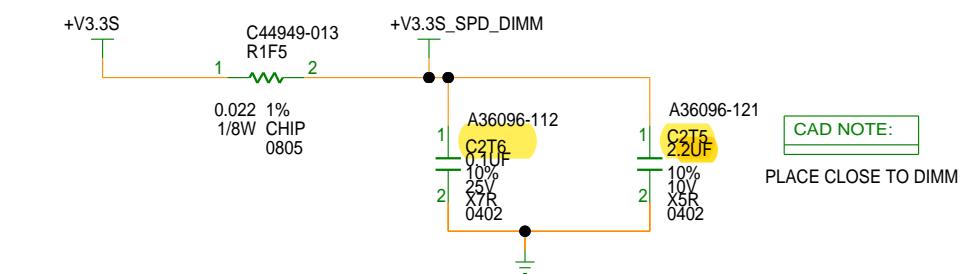
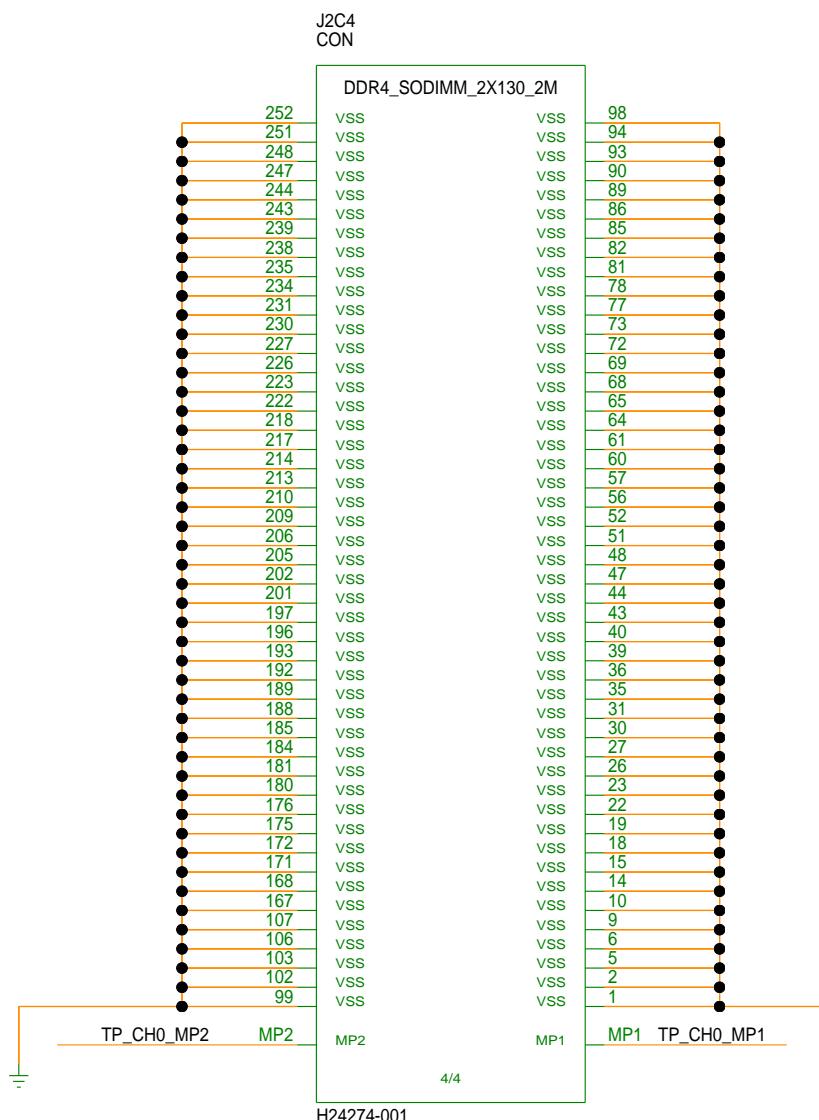
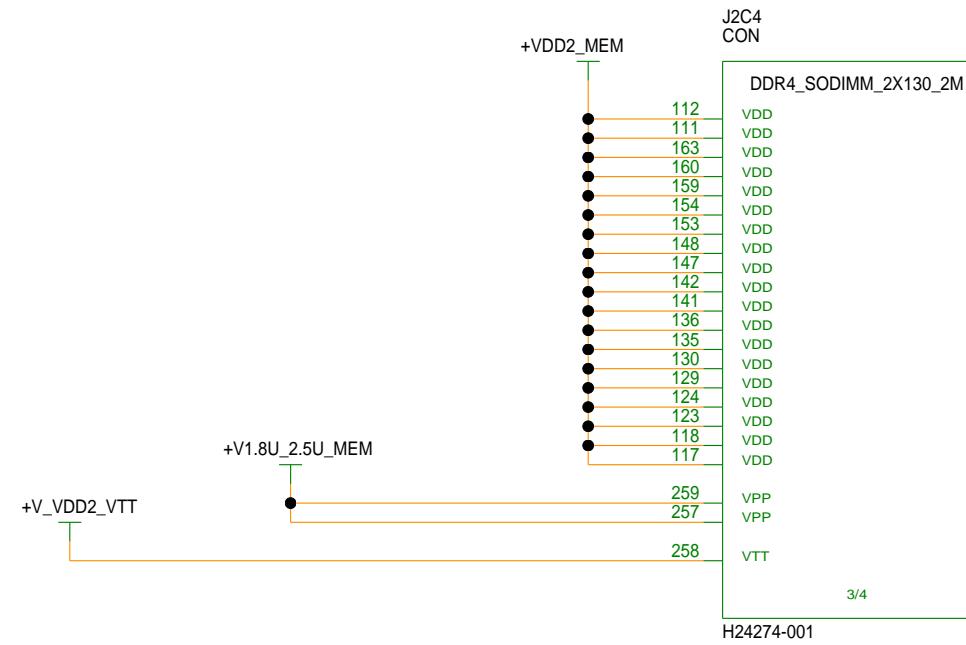
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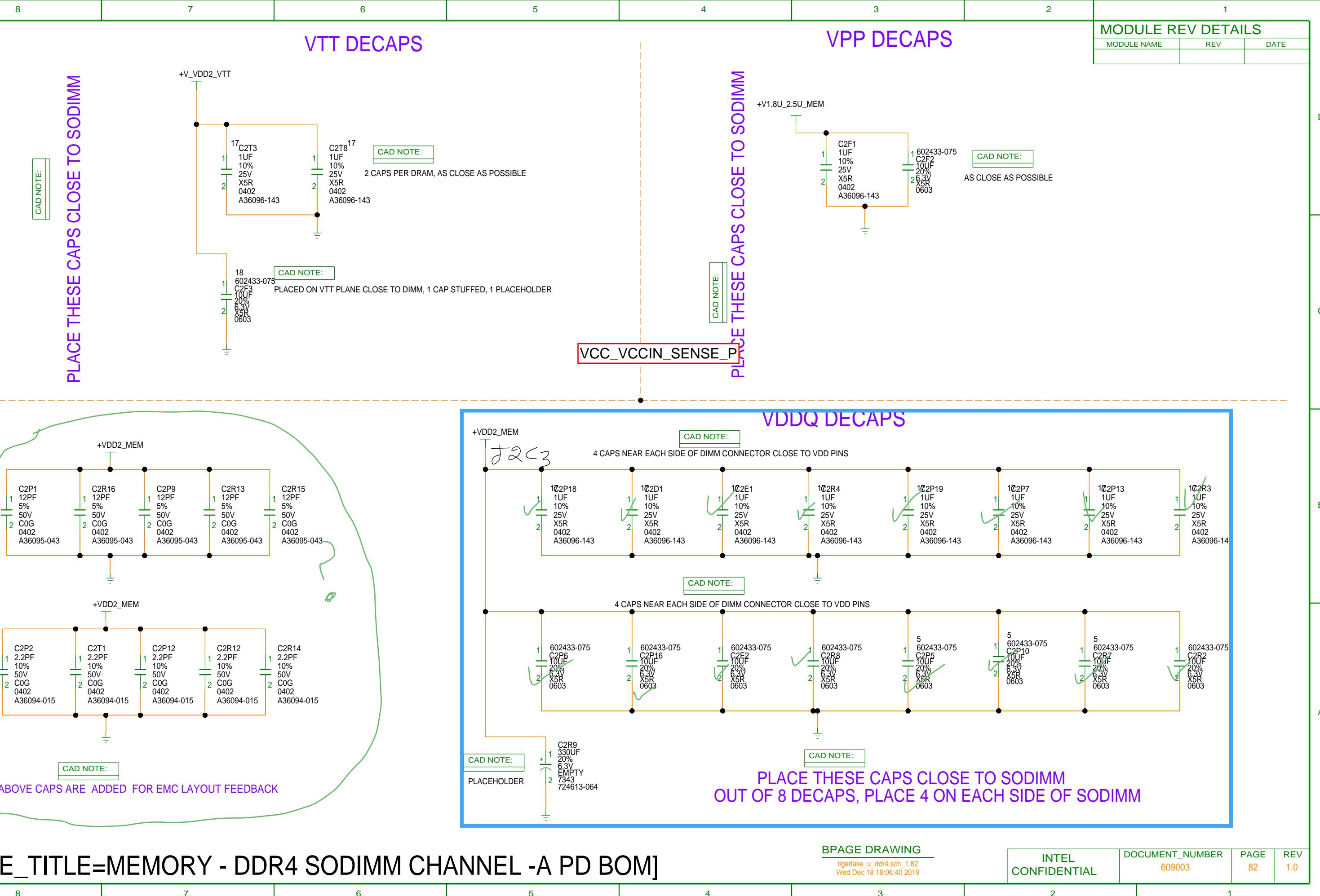
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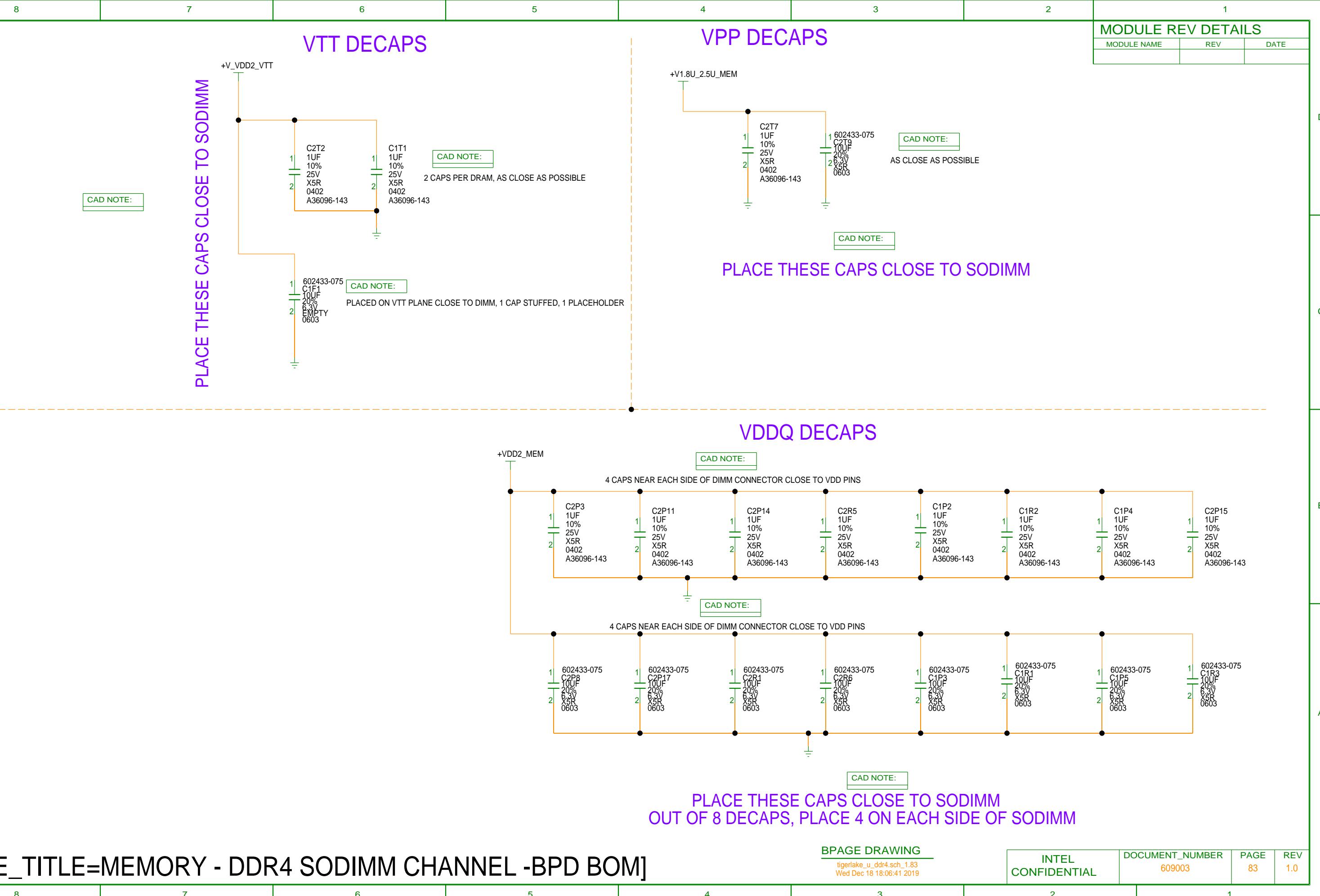


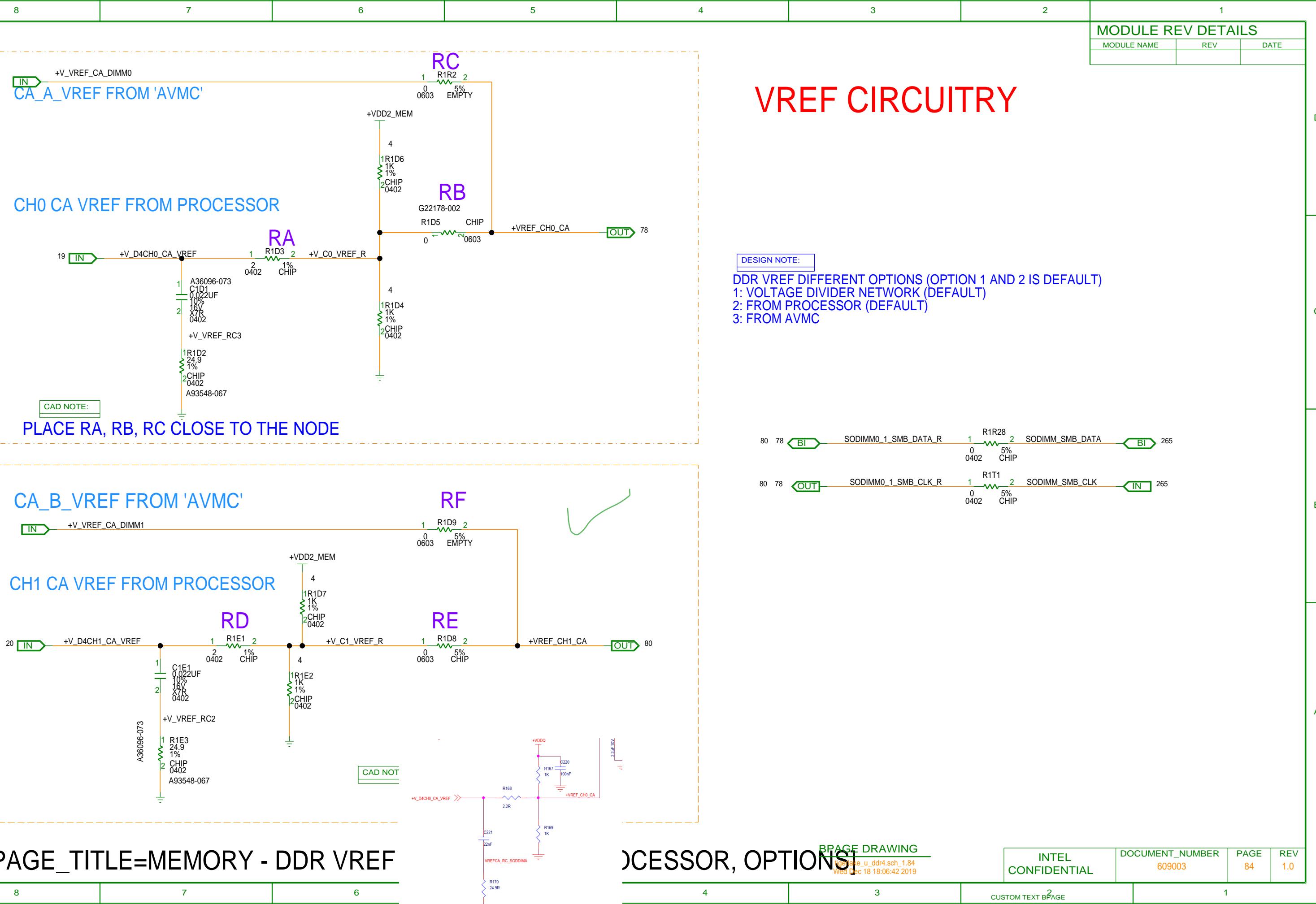


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MODULE REV DETAILS

MODULE NAME	REV	DATE

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Tue Oct 15 12:49:41 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 85	REV 1.0
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CUSTOM TEXT
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MODULE REV DETAILS

MODULE NAME	REV	DATE

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Wed Dec 18 16:29:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 86	REV 1.0
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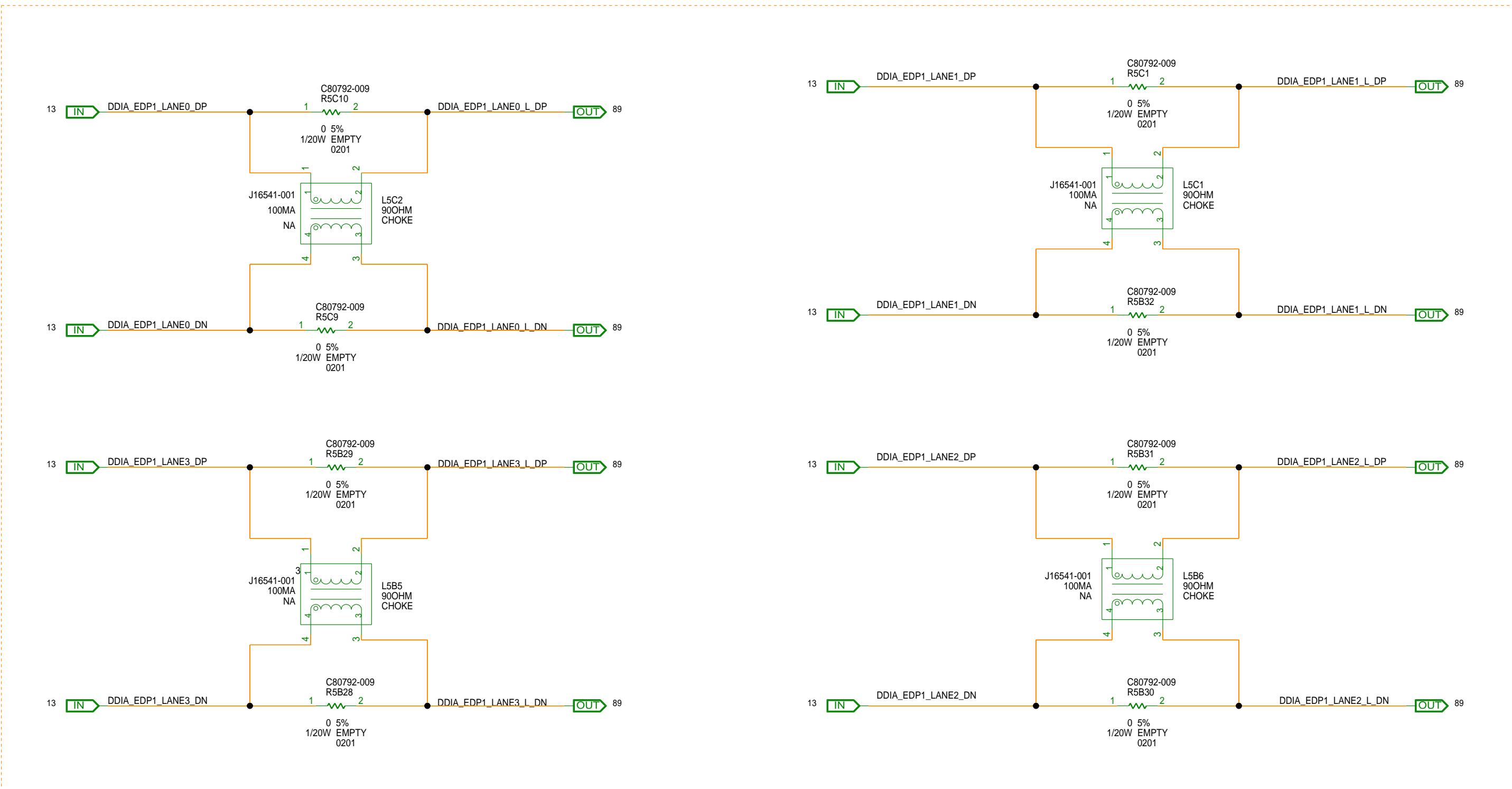
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CUSTOM TEXT
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MODULE NAME	REV	DATE					

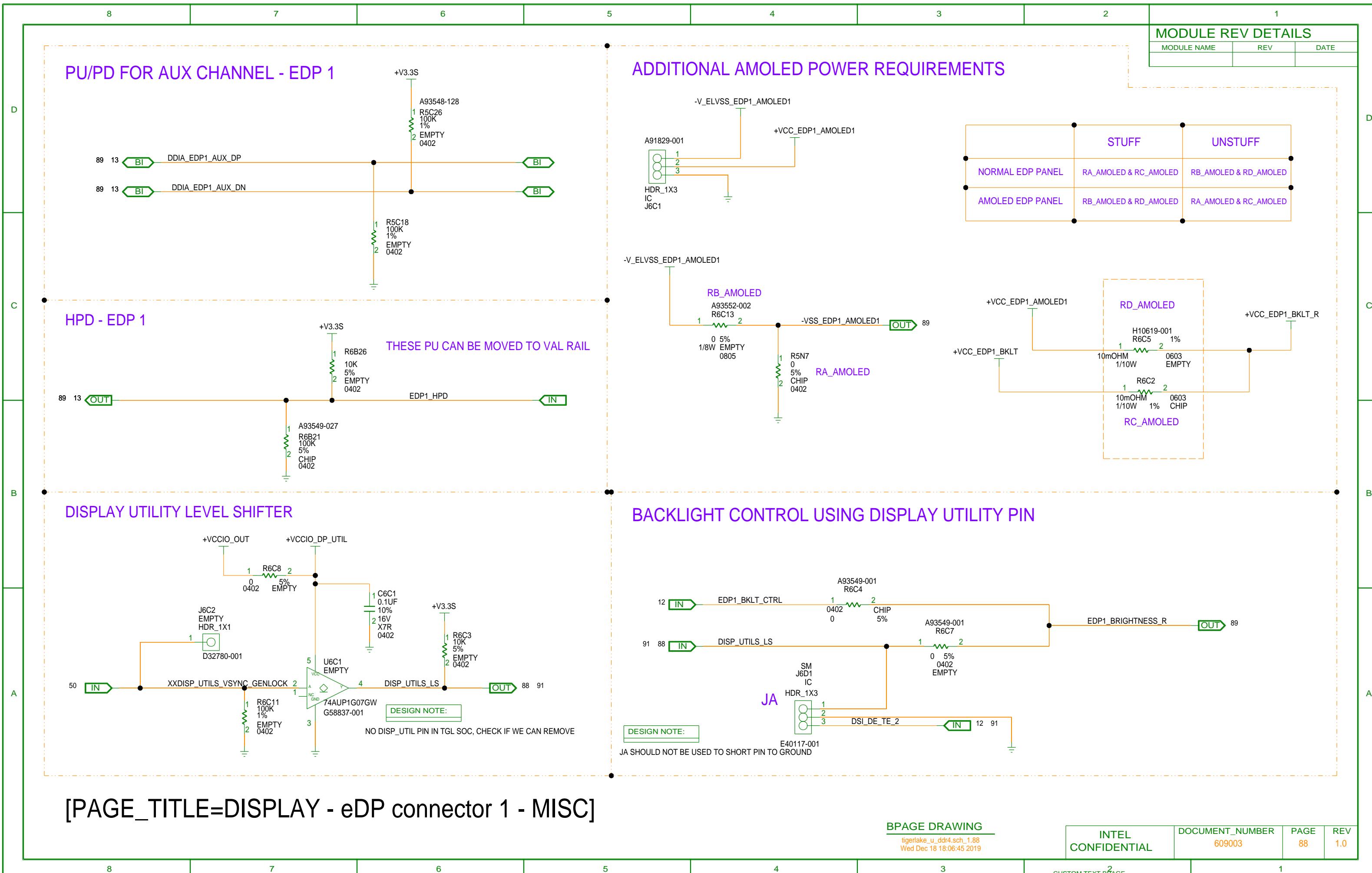
EDP CONNECTOR 1 - CMC



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Tue Oct 15 12:49:42 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 87	REV 1.0
CUSTOM TEXT BPAGE			



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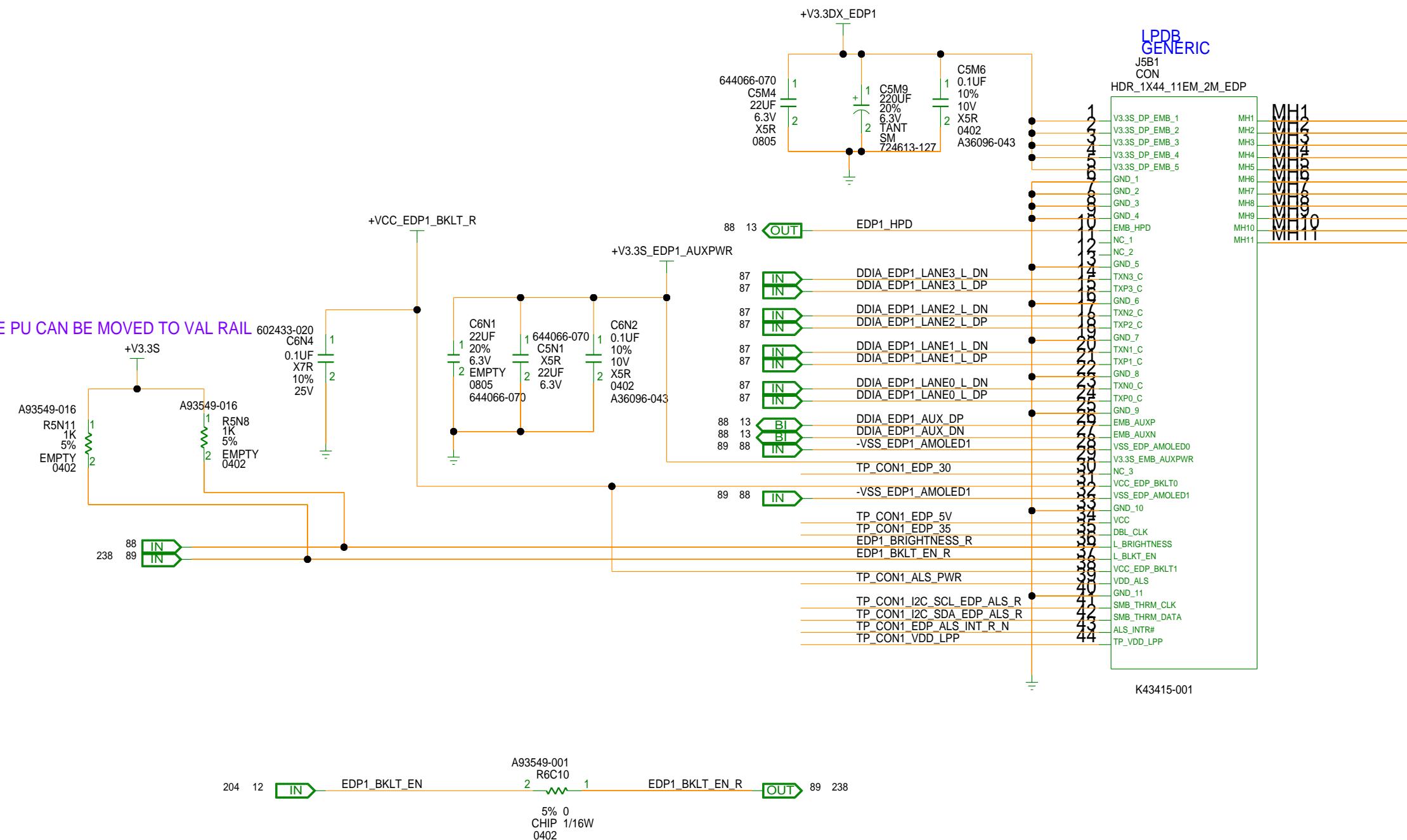
MODULE REV DETAILS

MODULE NAME	REV	DATE

EDP CONNECTOR 1

CHANGE TANT CAP TO LOWER VALUE

THESE PU CAN BE MOVED TO VAL RAIL



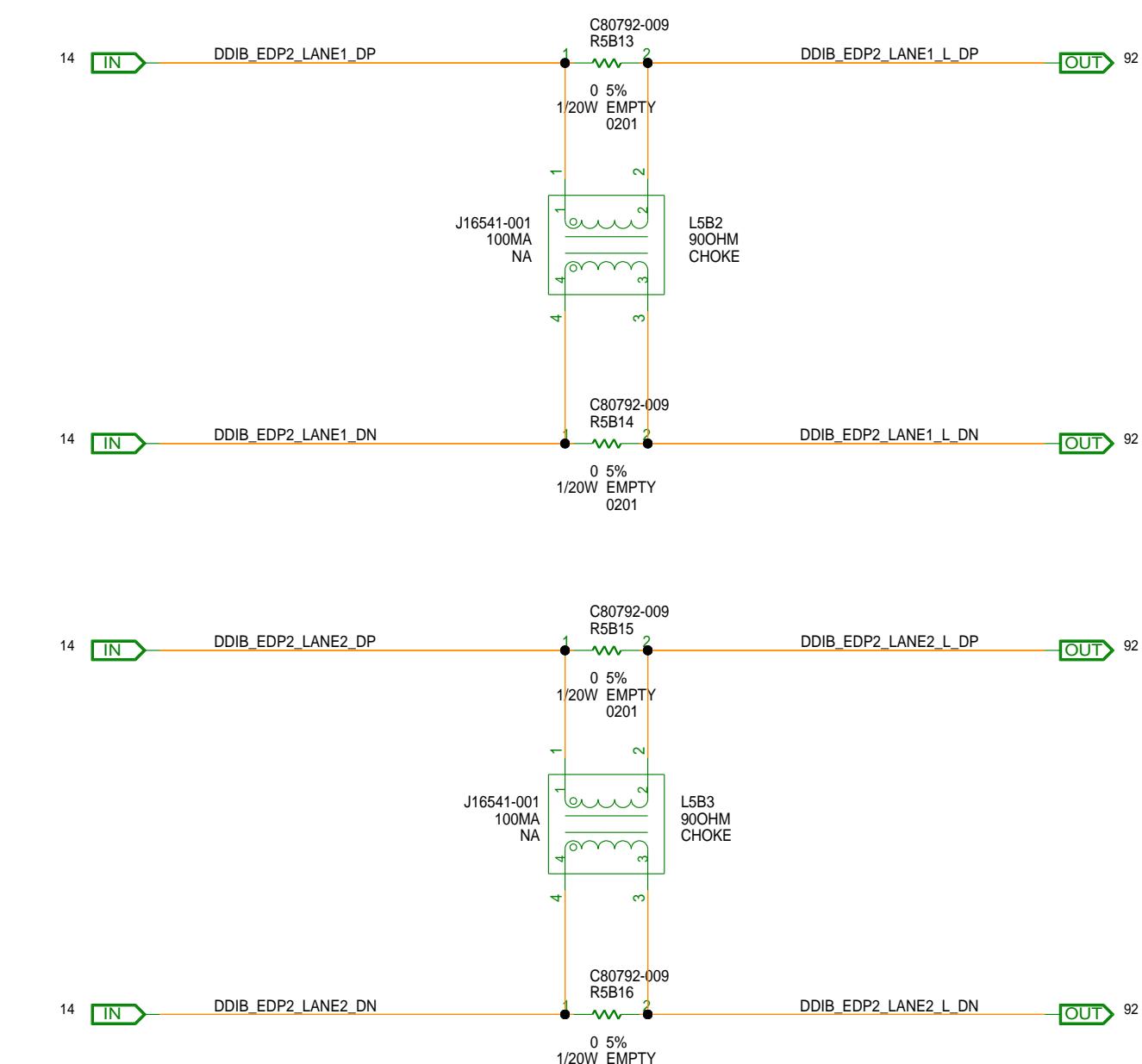
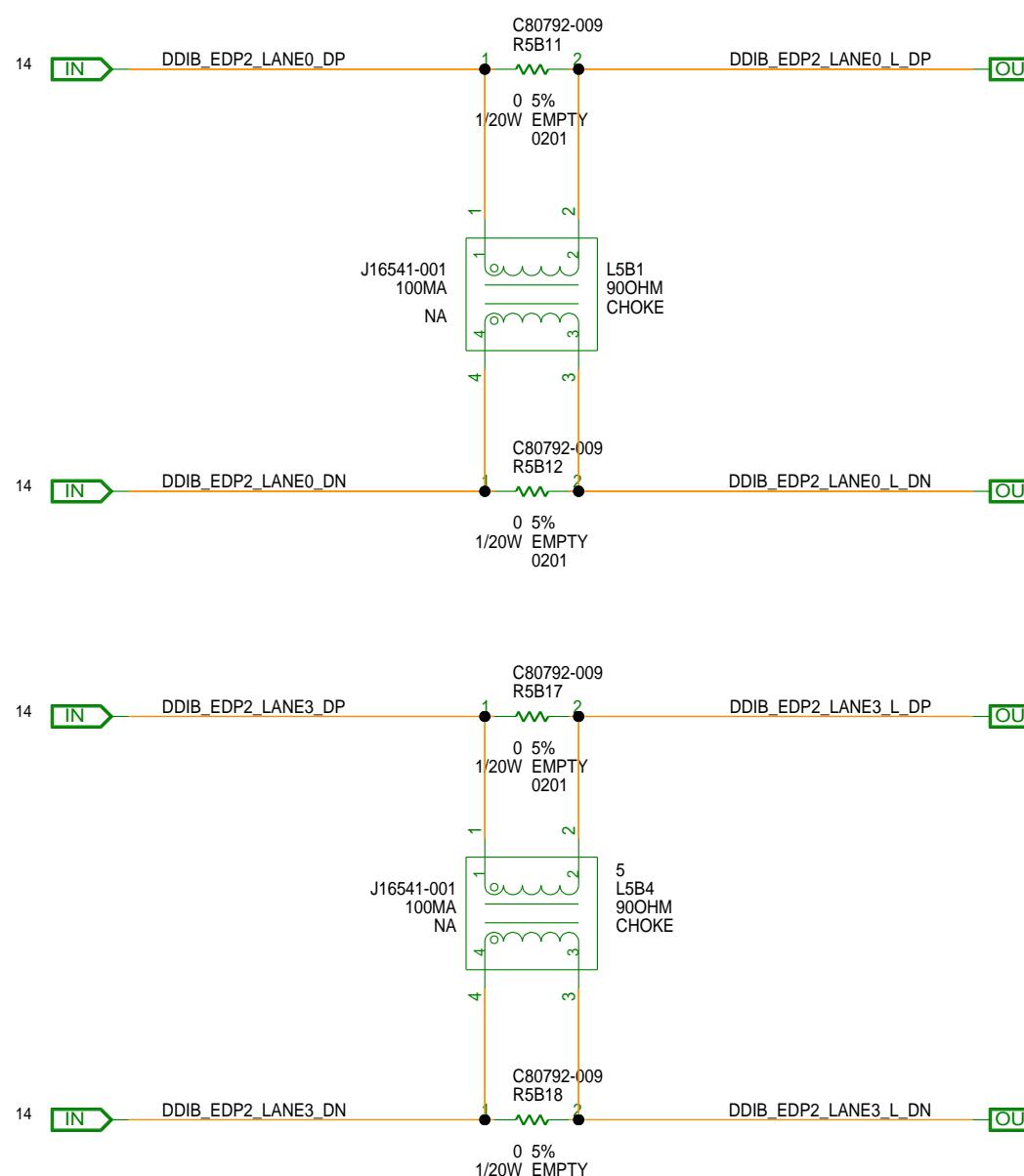
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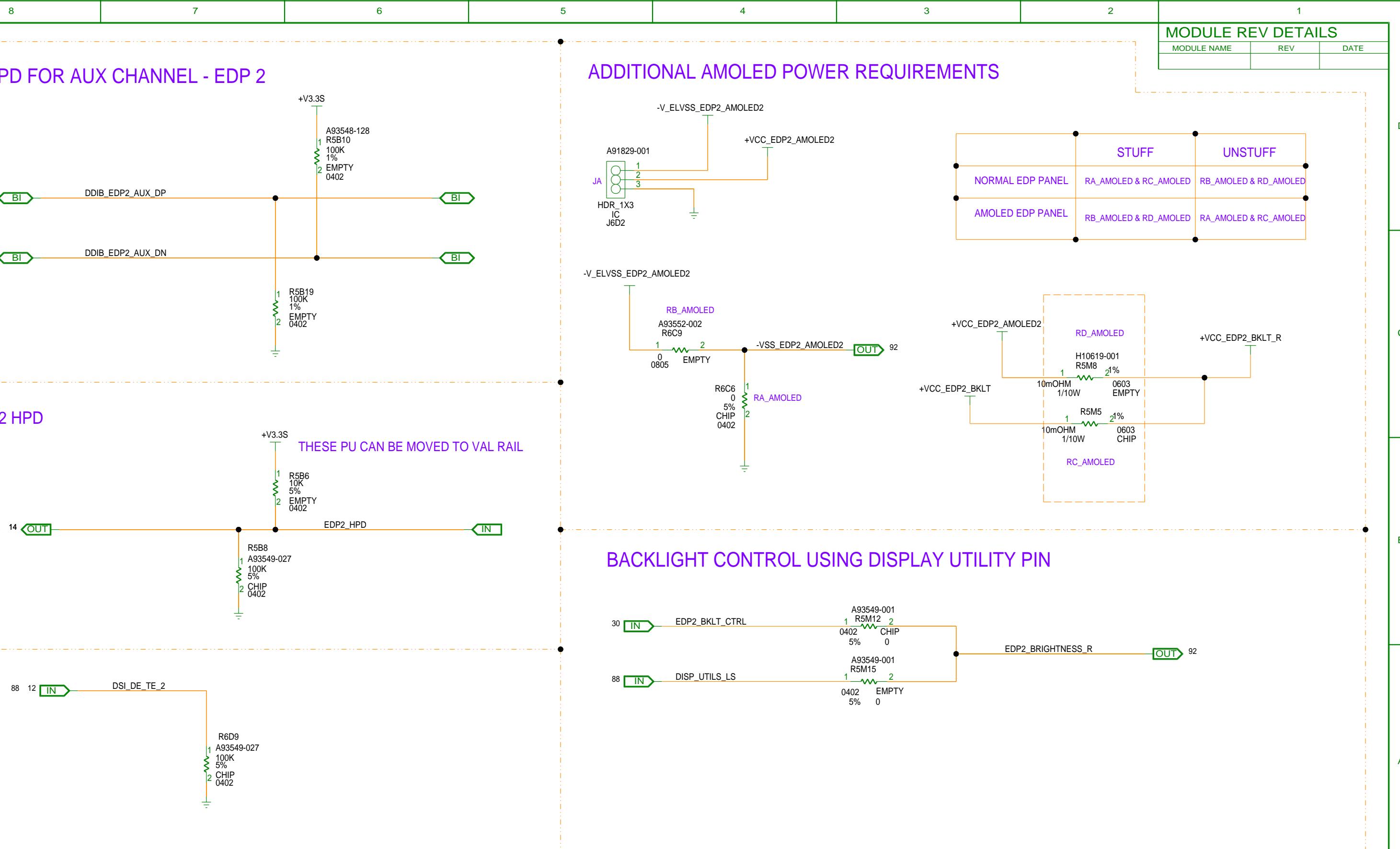
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Wed Dec 18 18:06:46 2019

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8	7	6	5	4	3	2	1
MODULE REV DETAILS						MODULE NAME	REV

EDP CONNECTOR 2 - CMC





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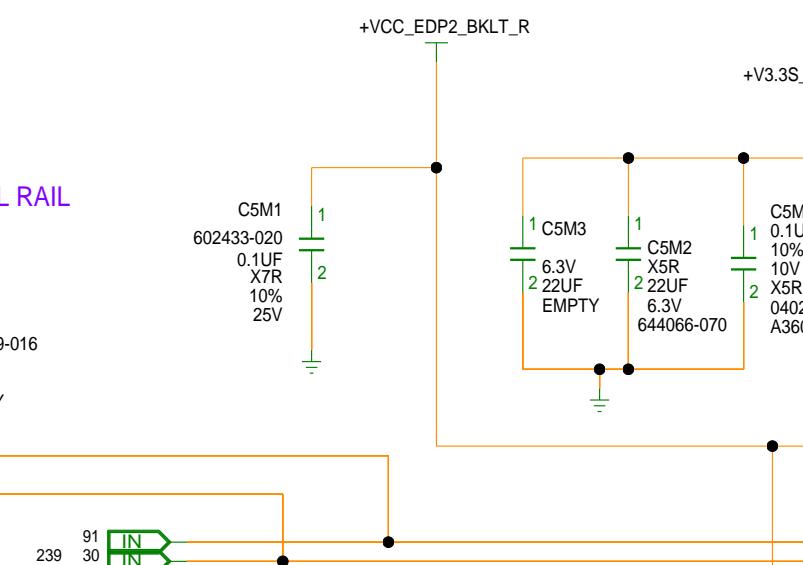
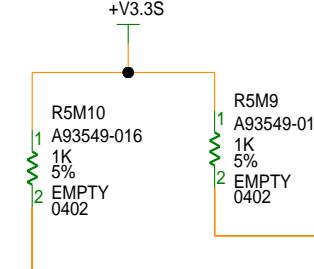
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MODULE REV DETAILS

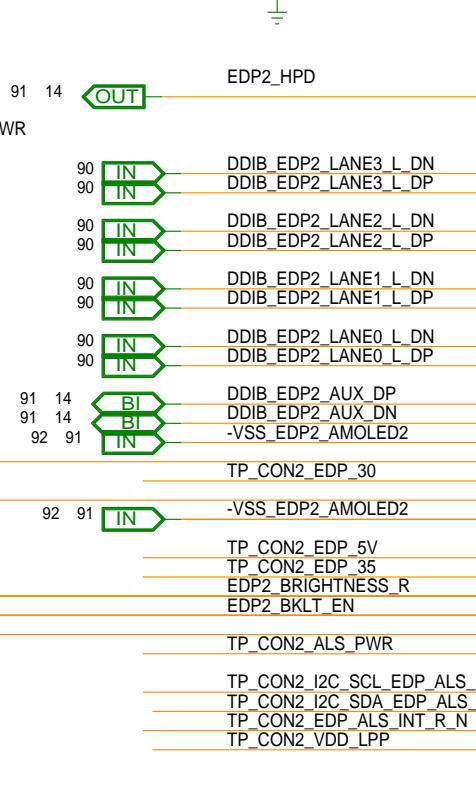
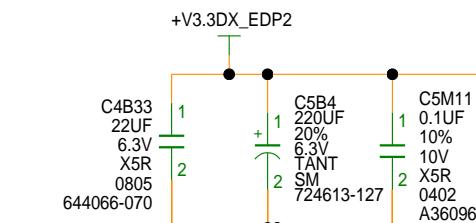
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EDP CONNECTOR 2

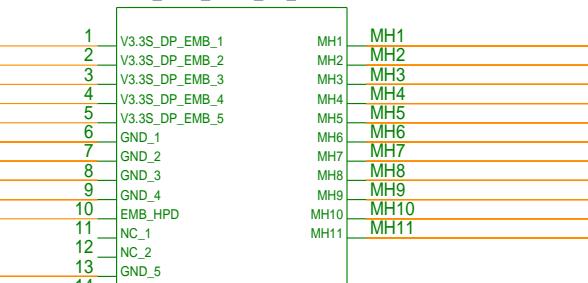
THESE PU CAN BE MOVED TO VAL RAIL



CHANGE TANT CAP TO LOWER VALUE



LPDB GENERIC

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K43415-001

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MODULE REV DETAILS

MODULE NAME	REV	DATE

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Tue Oct 15 12:49:48 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT ²BPAGE

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MODULE REV DETAILS

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[PAGE_TITLE=DISPLAY - RESERVE]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.94
Tue Oct 15 12:49:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 94	REV 1.0
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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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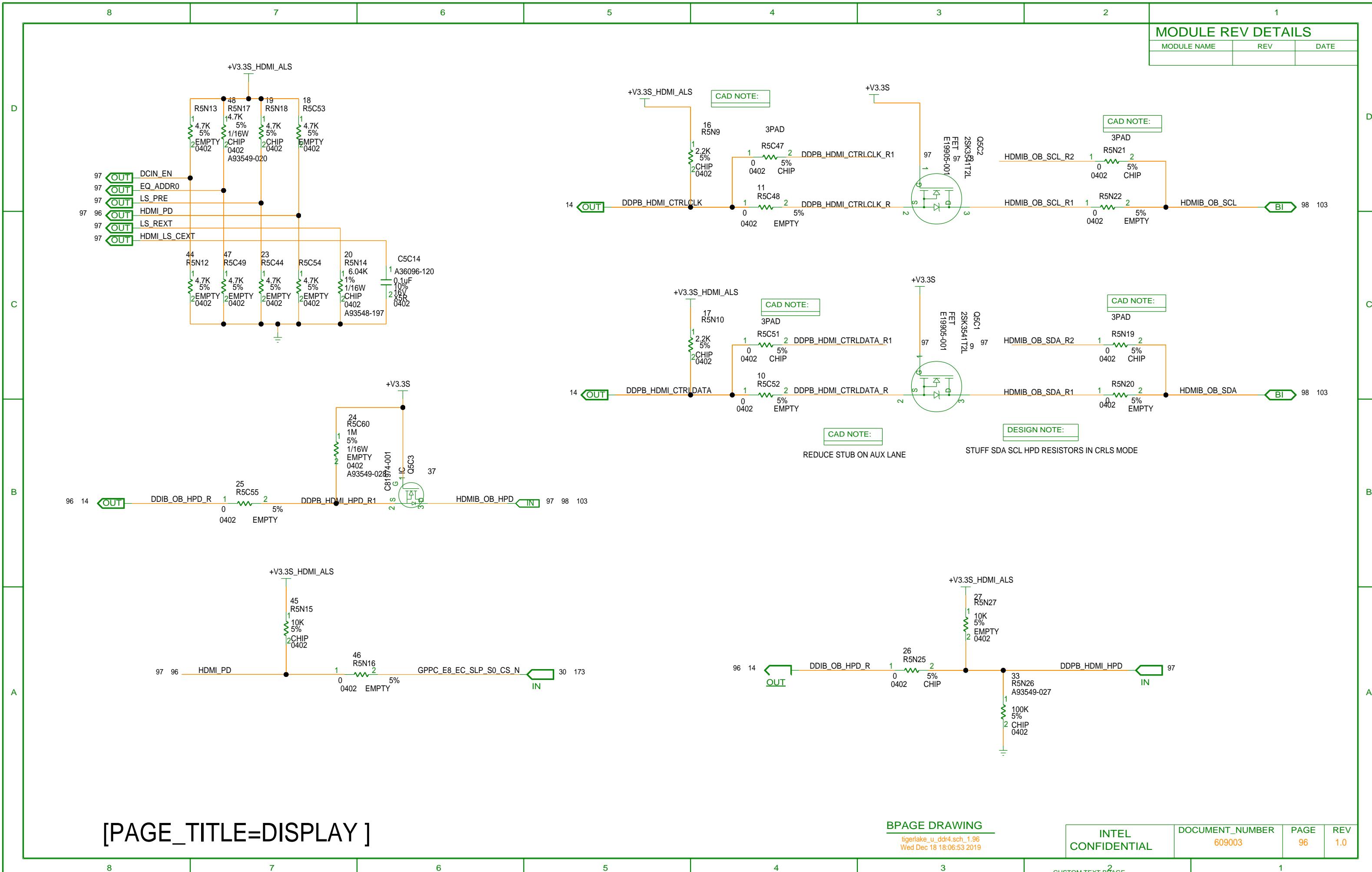
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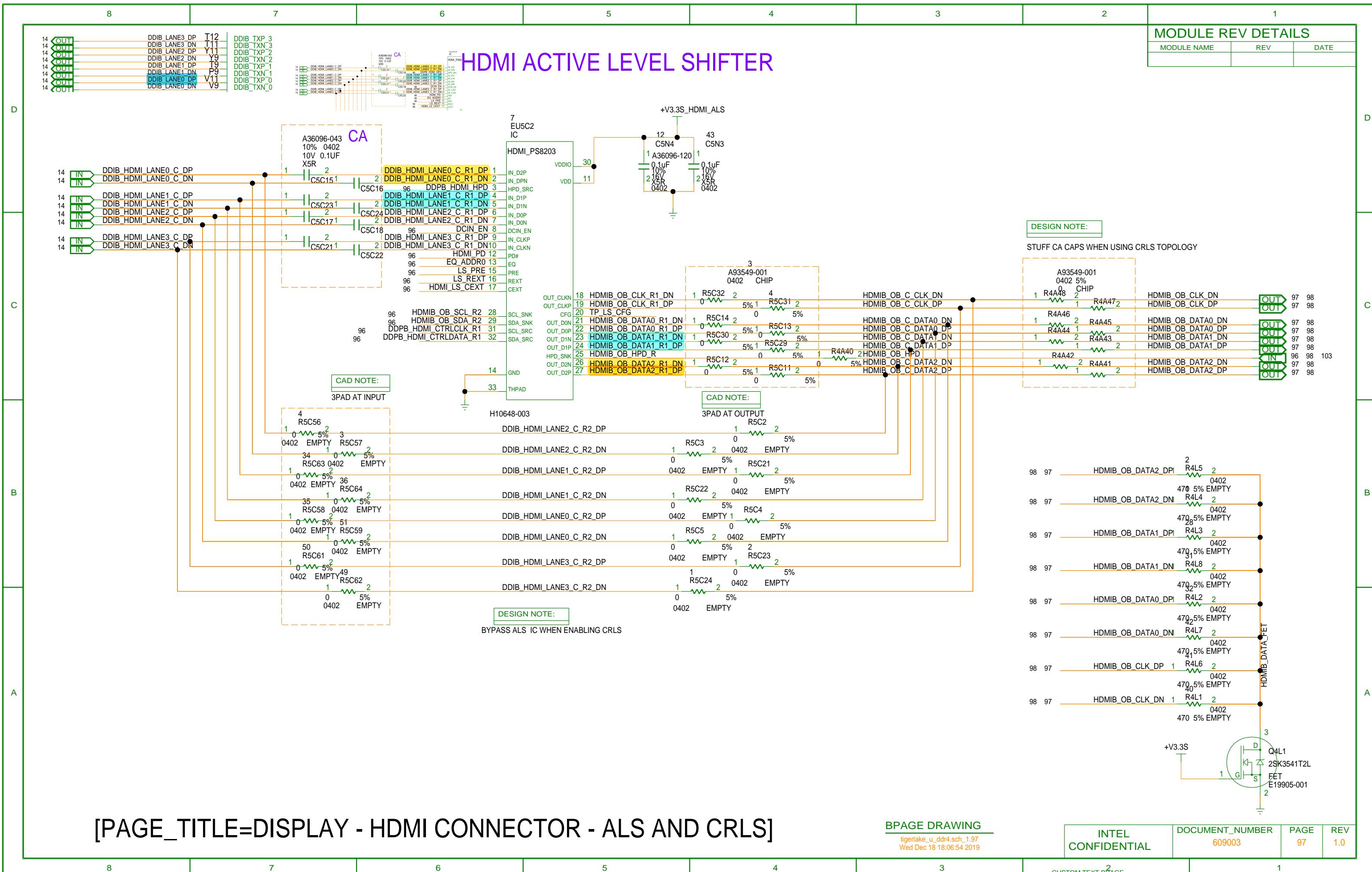
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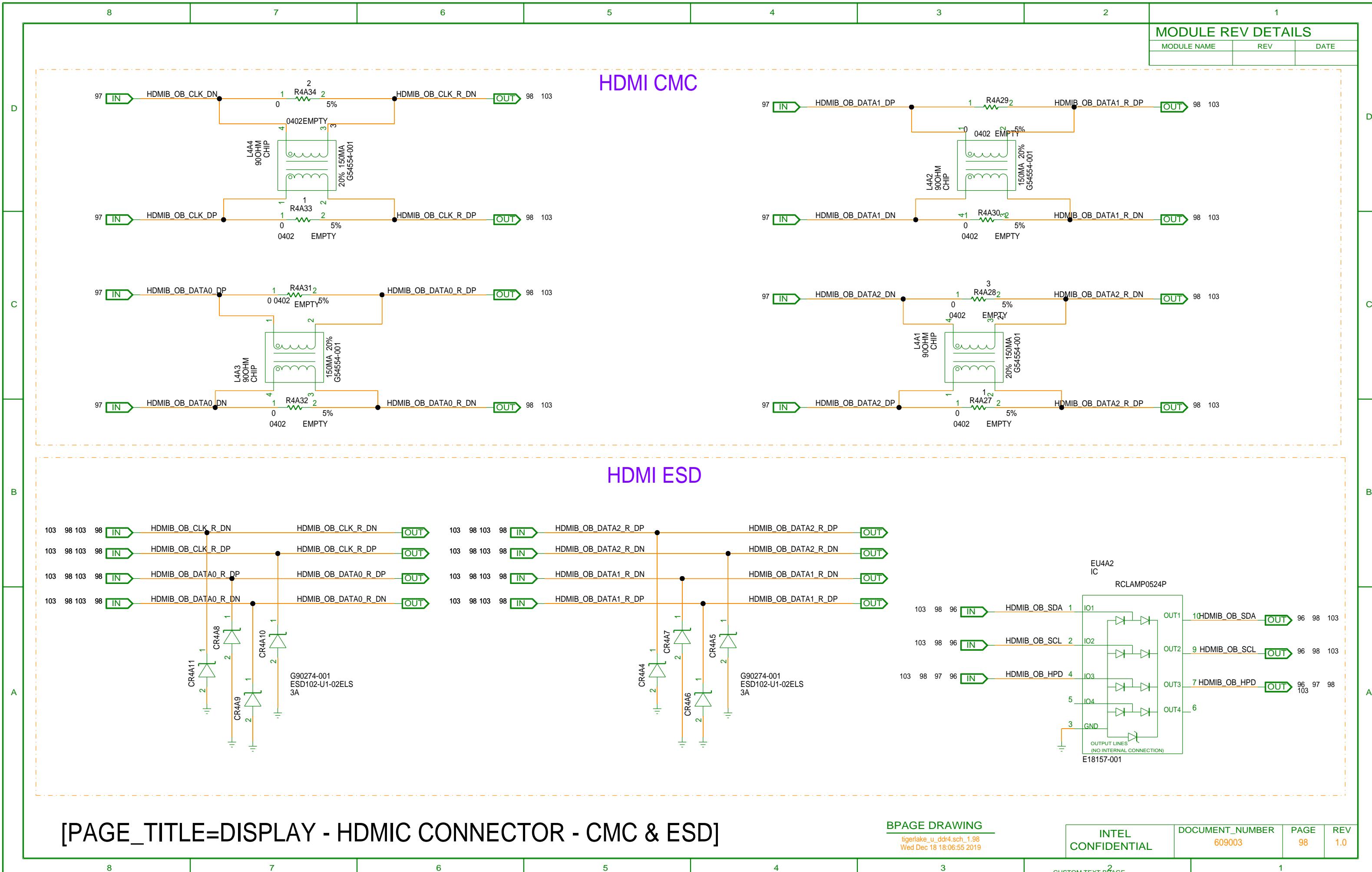
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Tue Oct 15 12:49:49 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 95	REV 1.0
CUSTOM TEXT 2 PAGE			1

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

DP CONNECTOR 2 - CMC

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[PAGE_TITLE=DISPLAY - DP CONNECTOR 2 CMC]

BPAGE DRAWING
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Tue Oct 15 12:49:53 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 99	REV 1.0
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CUSTOM TEXT 2 PAGE

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

DP CONNECTOR 2 - ESD

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[PAGE_TITLE=DISPLAY - DP CONNECTOR 2 - ESD]

BPAGE DRAWING
tigerlake_u_ddr4.sch_1.100
Tue Oct 15 12:49:54 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 100	REV 1.0
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

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[PAGE_TITLE=DISPLAY - DP CONNECTOR 2 - HDMI INTEROPERABILITY]

BPAGE DRAWING
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Tue Oct 15 12:49:55 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 101	REV 1.0
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8	7	6	5	4	3	CUSTOM TEXT 2 PAGE	1
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DISPLAY - DDI 1&2 HPD & CONNECTOR

MODULE REV DETAILS

MODULE NAME	REV	DATE

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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.102
Tue Oct 15 12:49:56 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 102	REV 1.0
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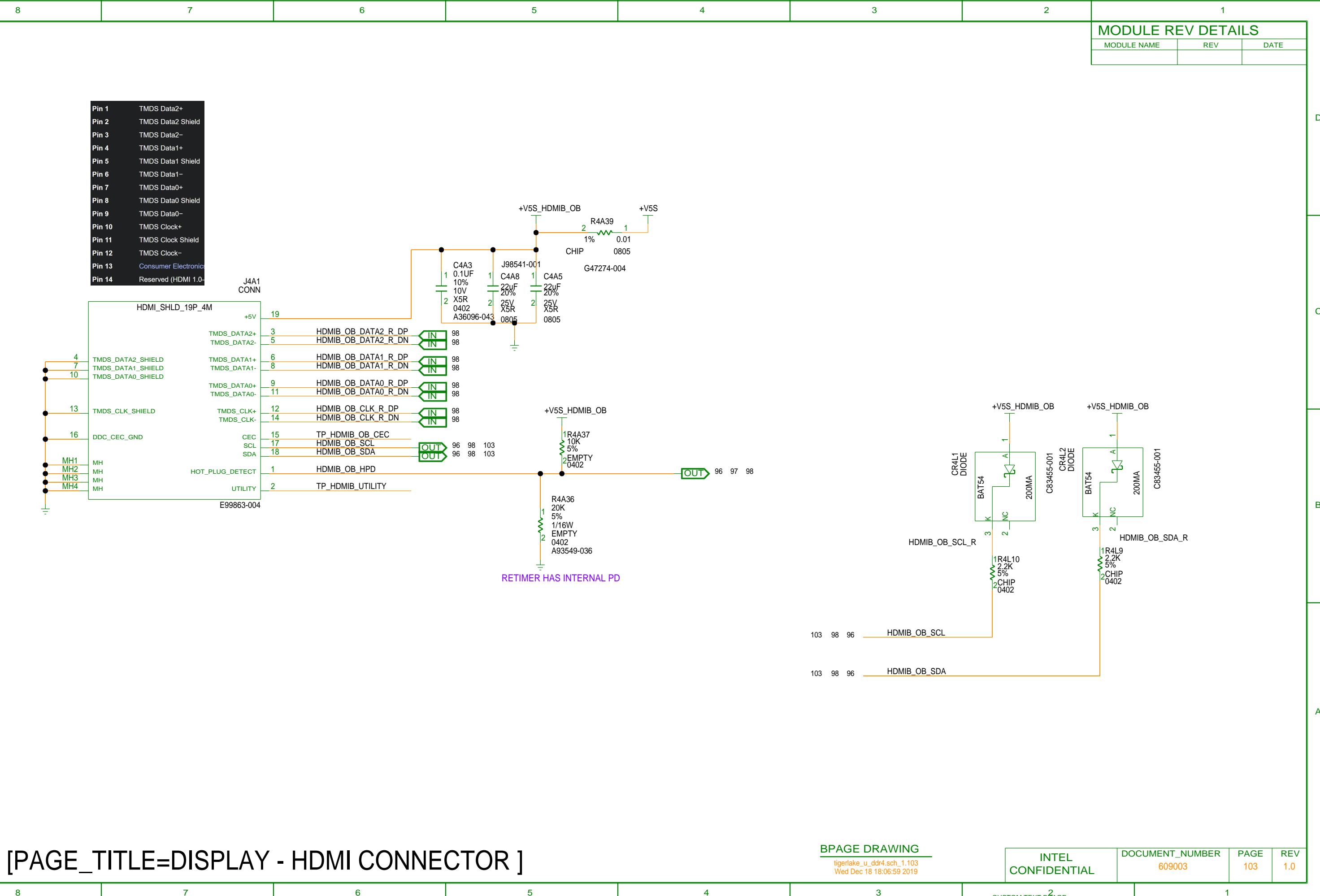
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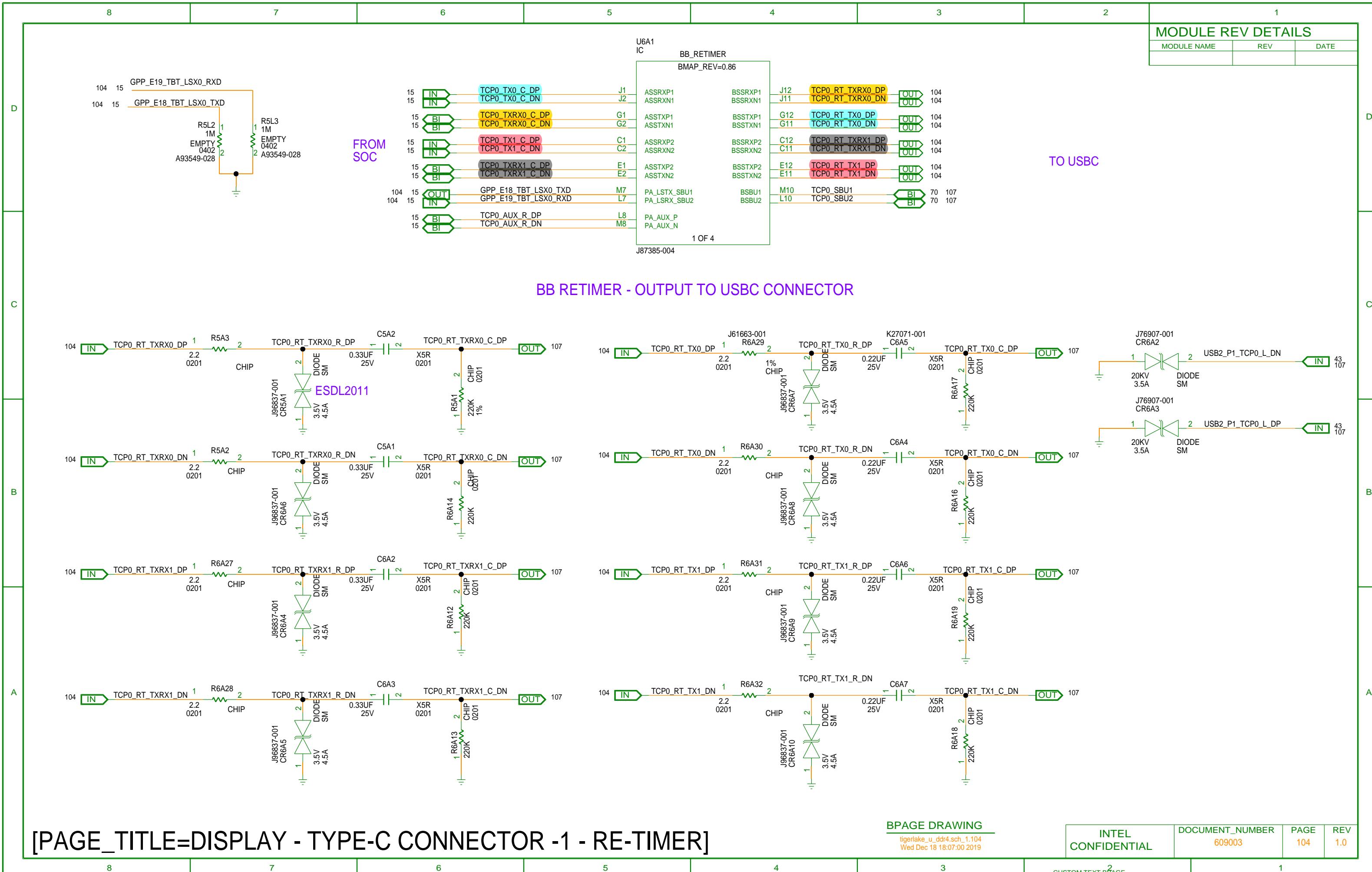
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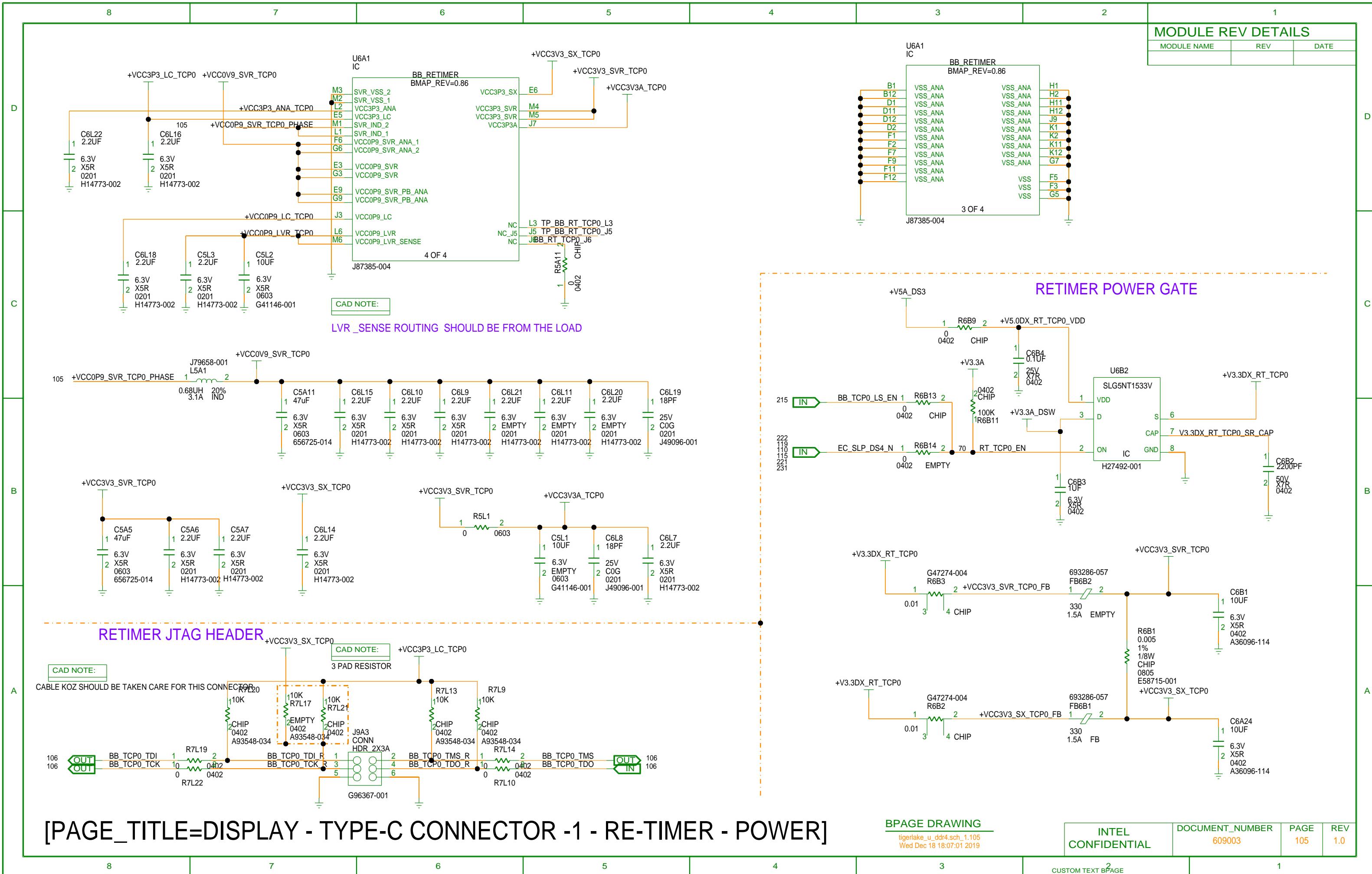
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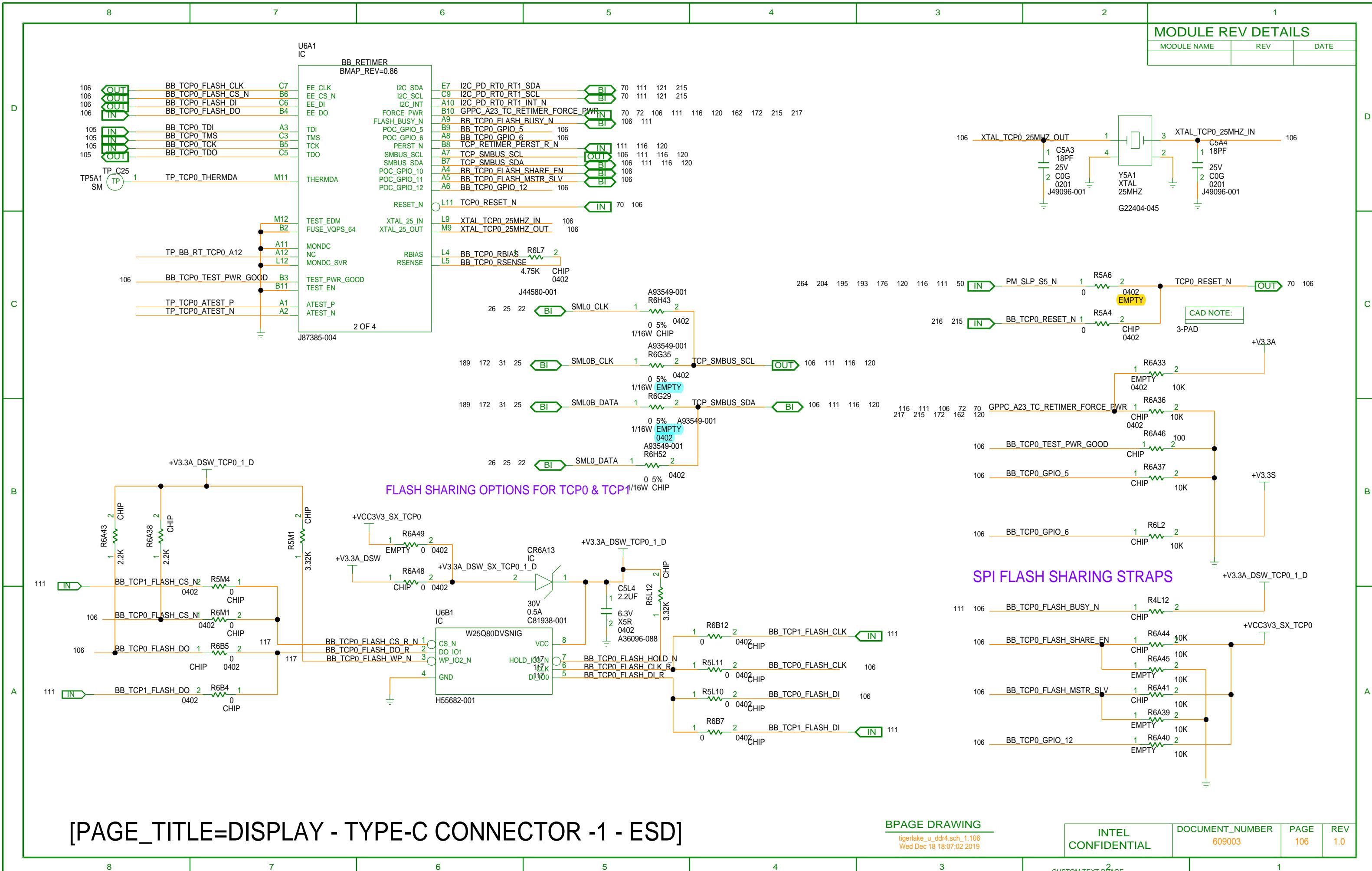
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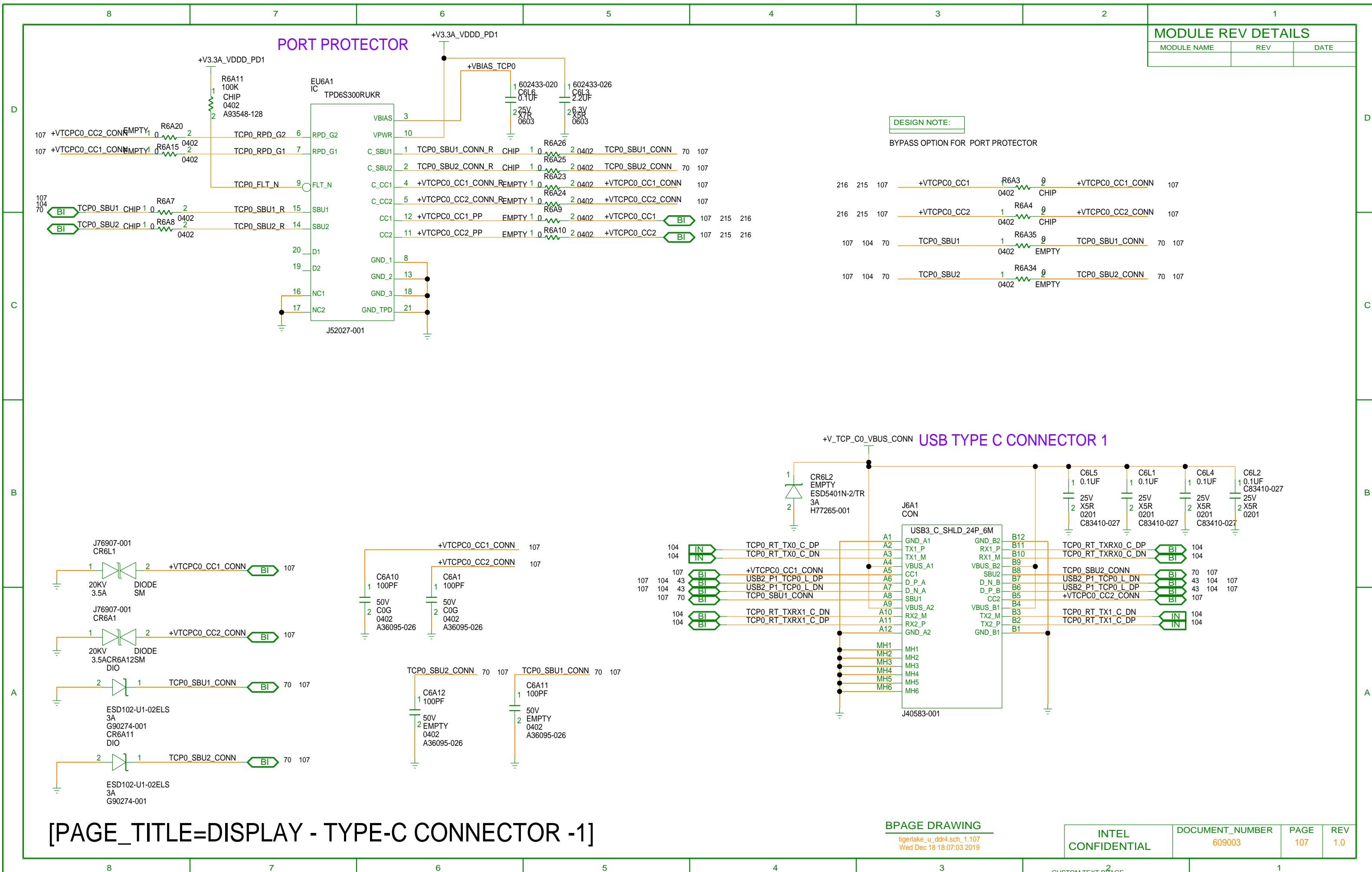
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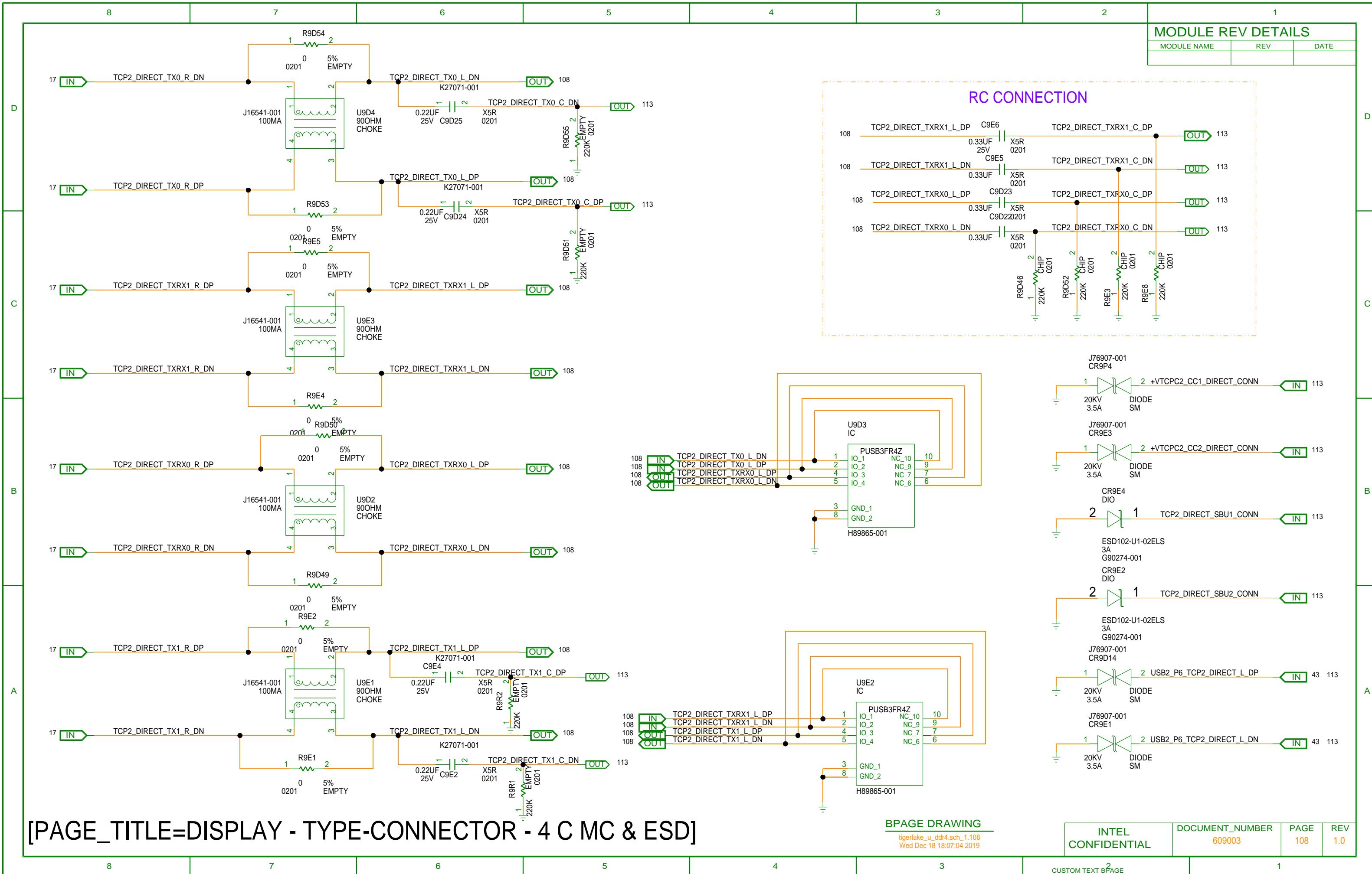


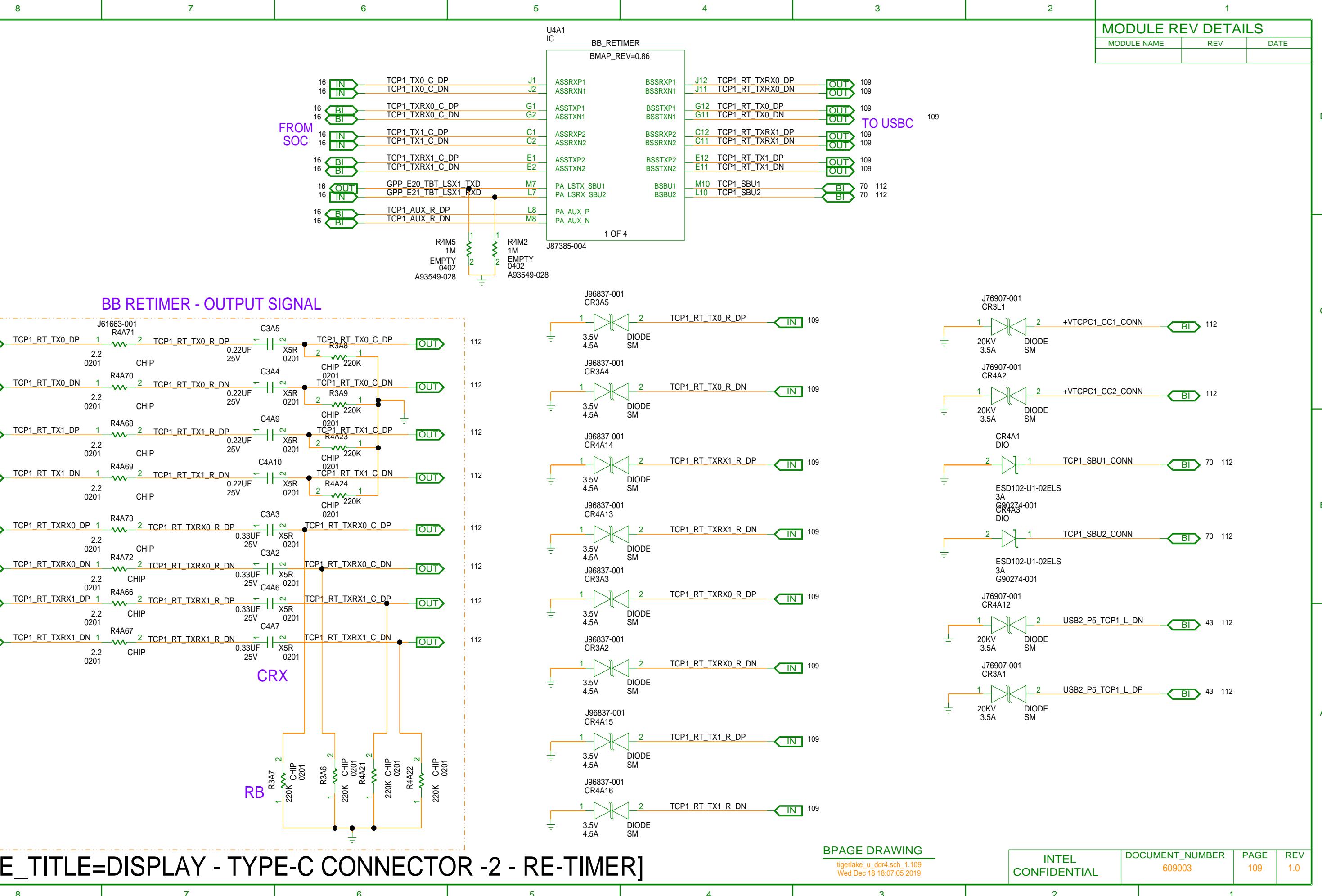


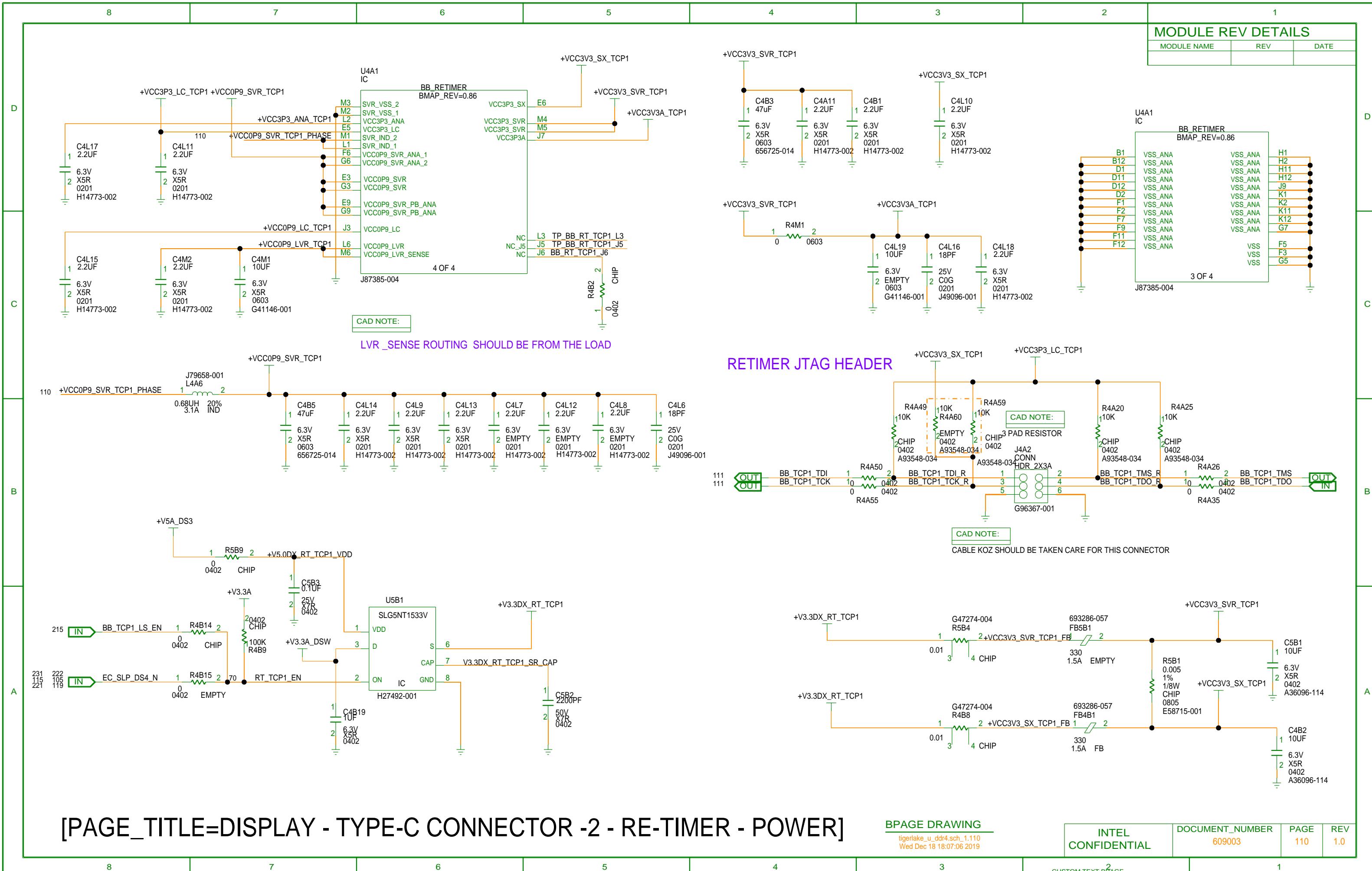


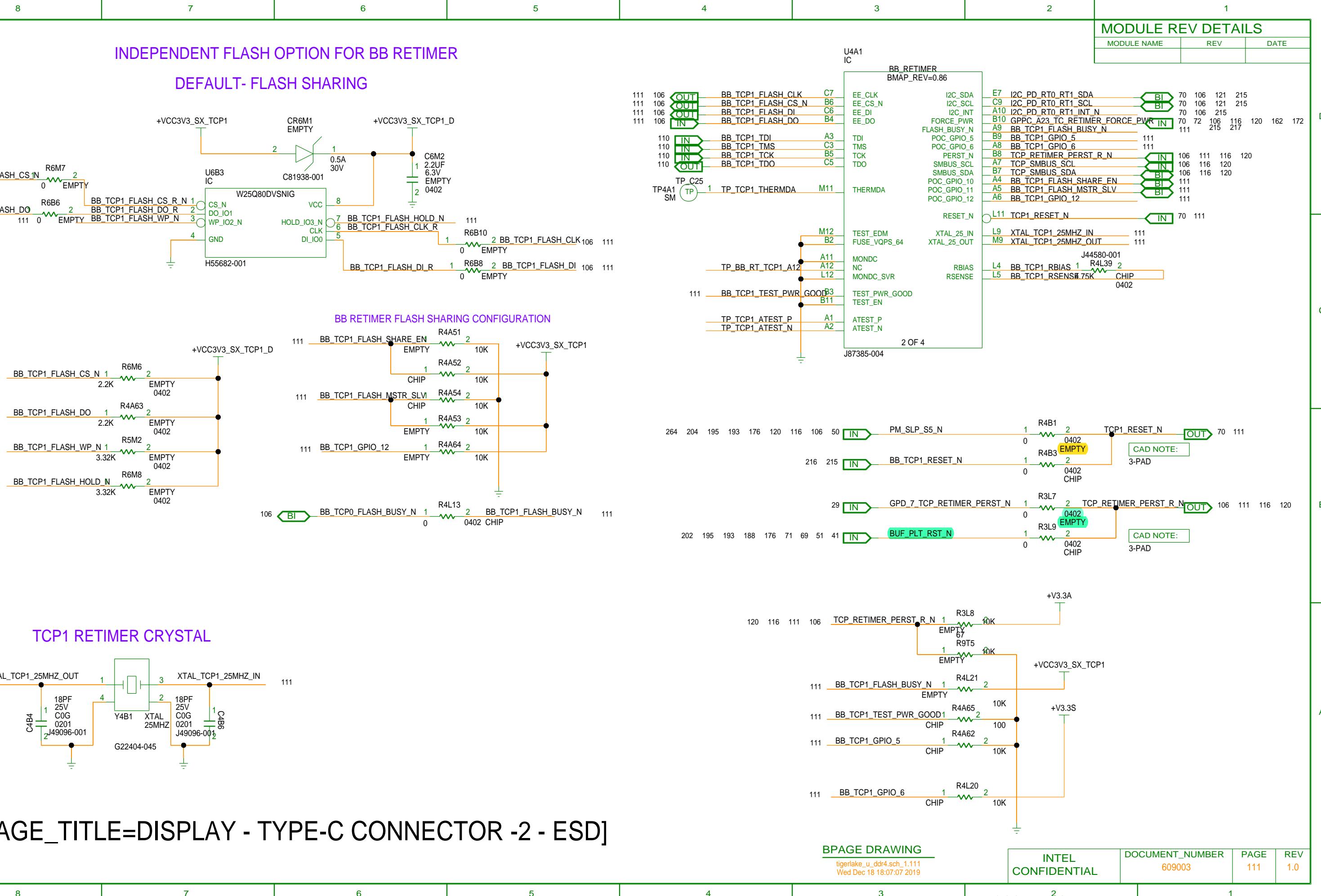


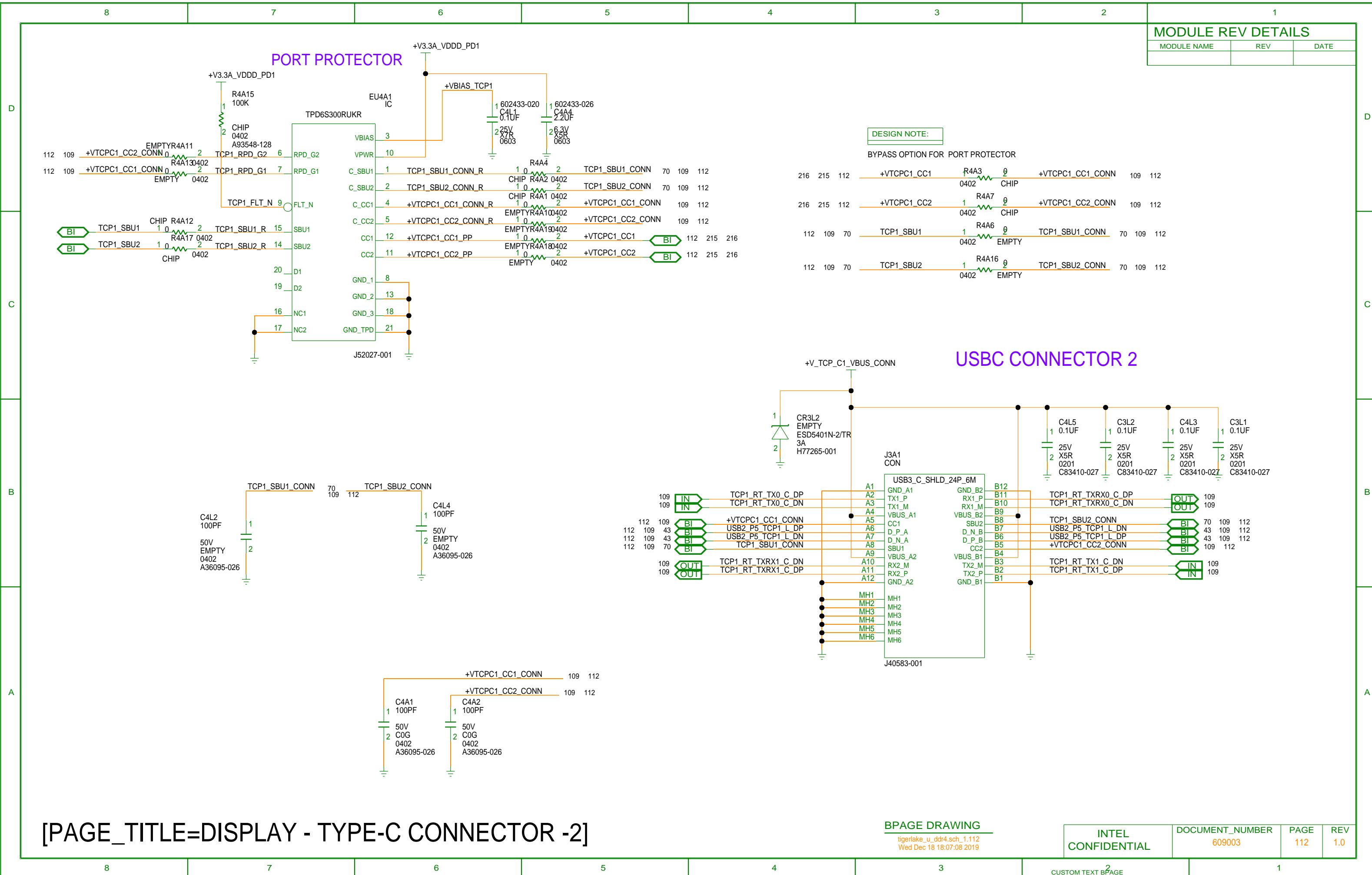


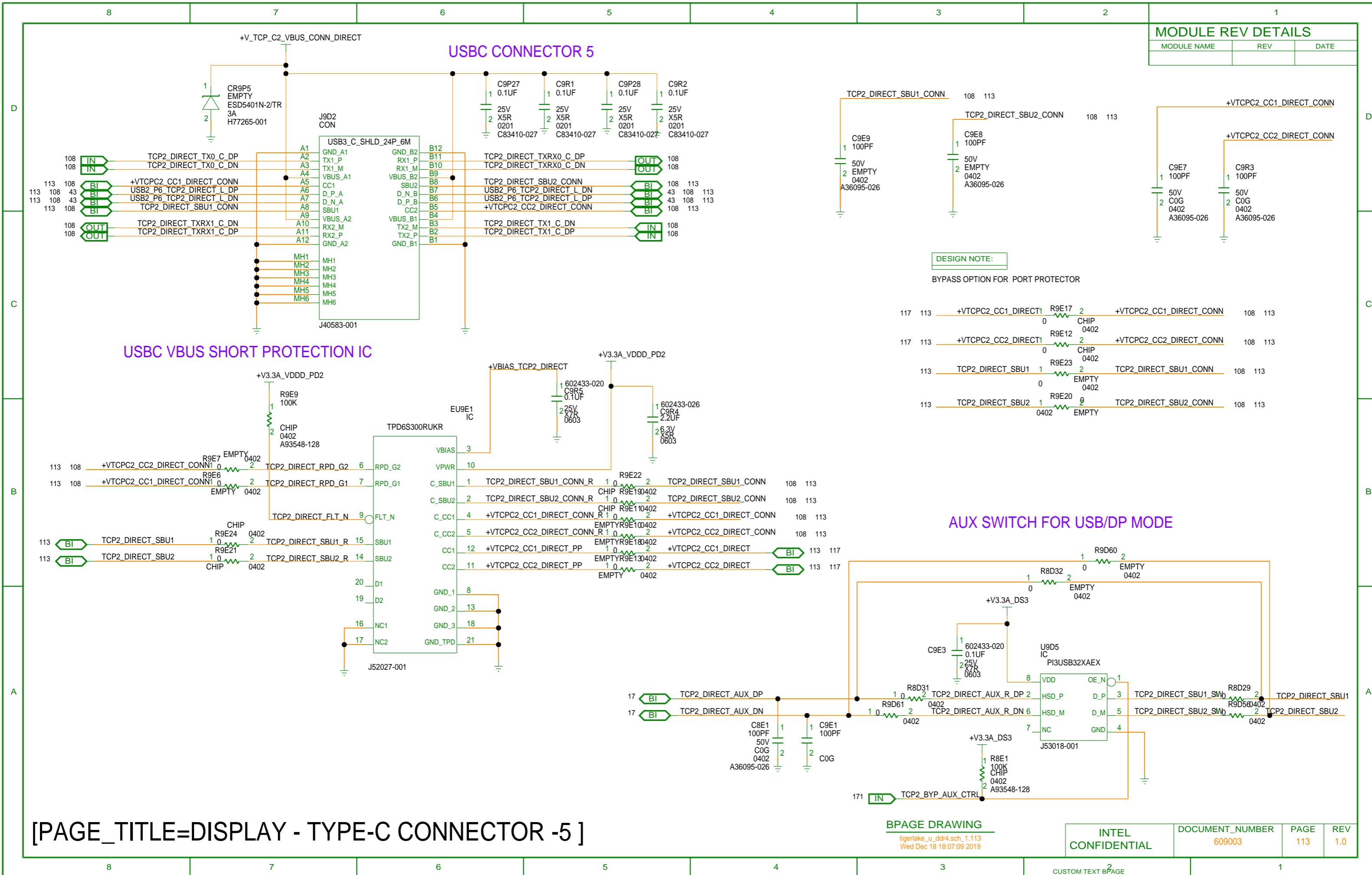


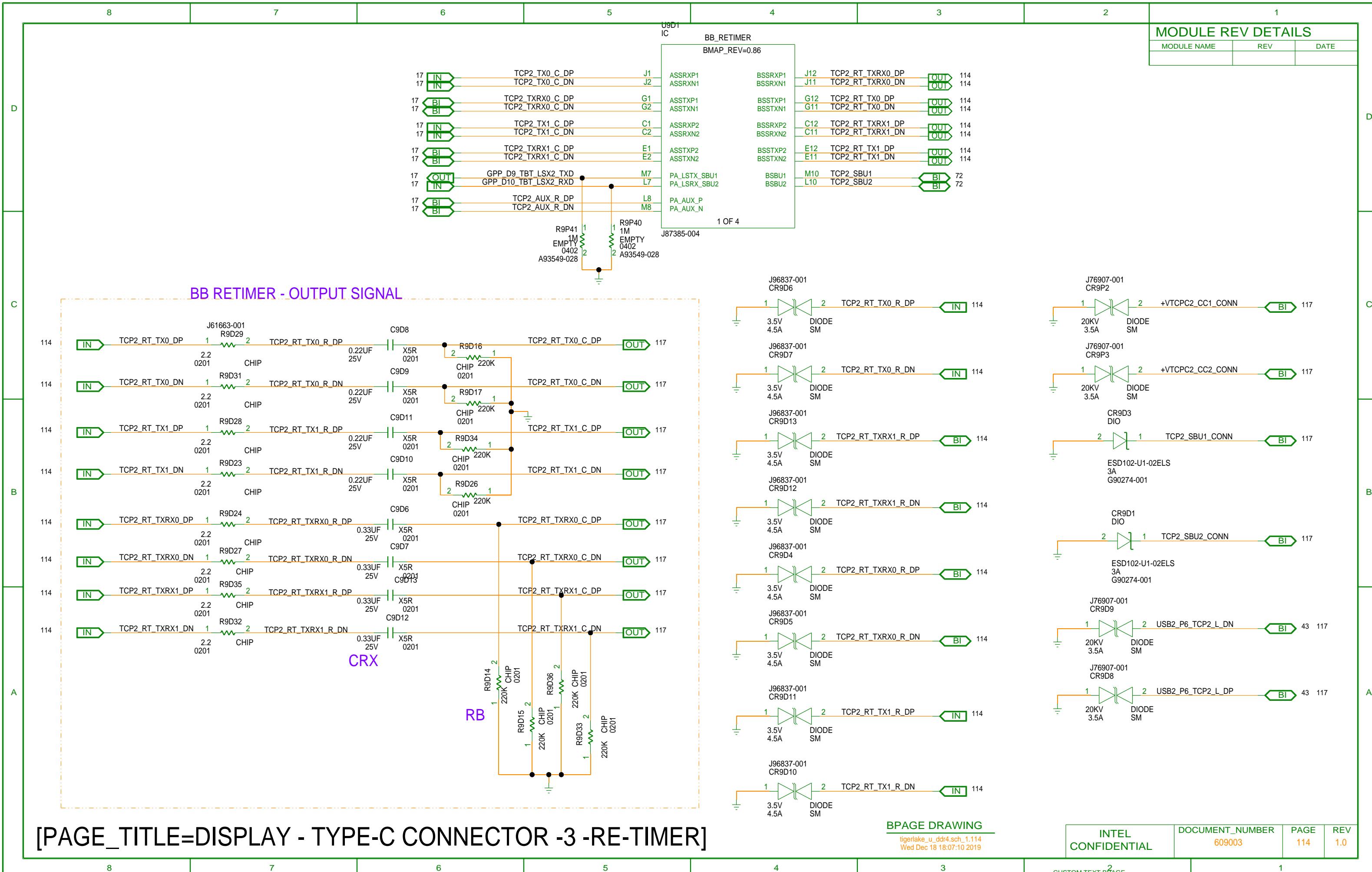


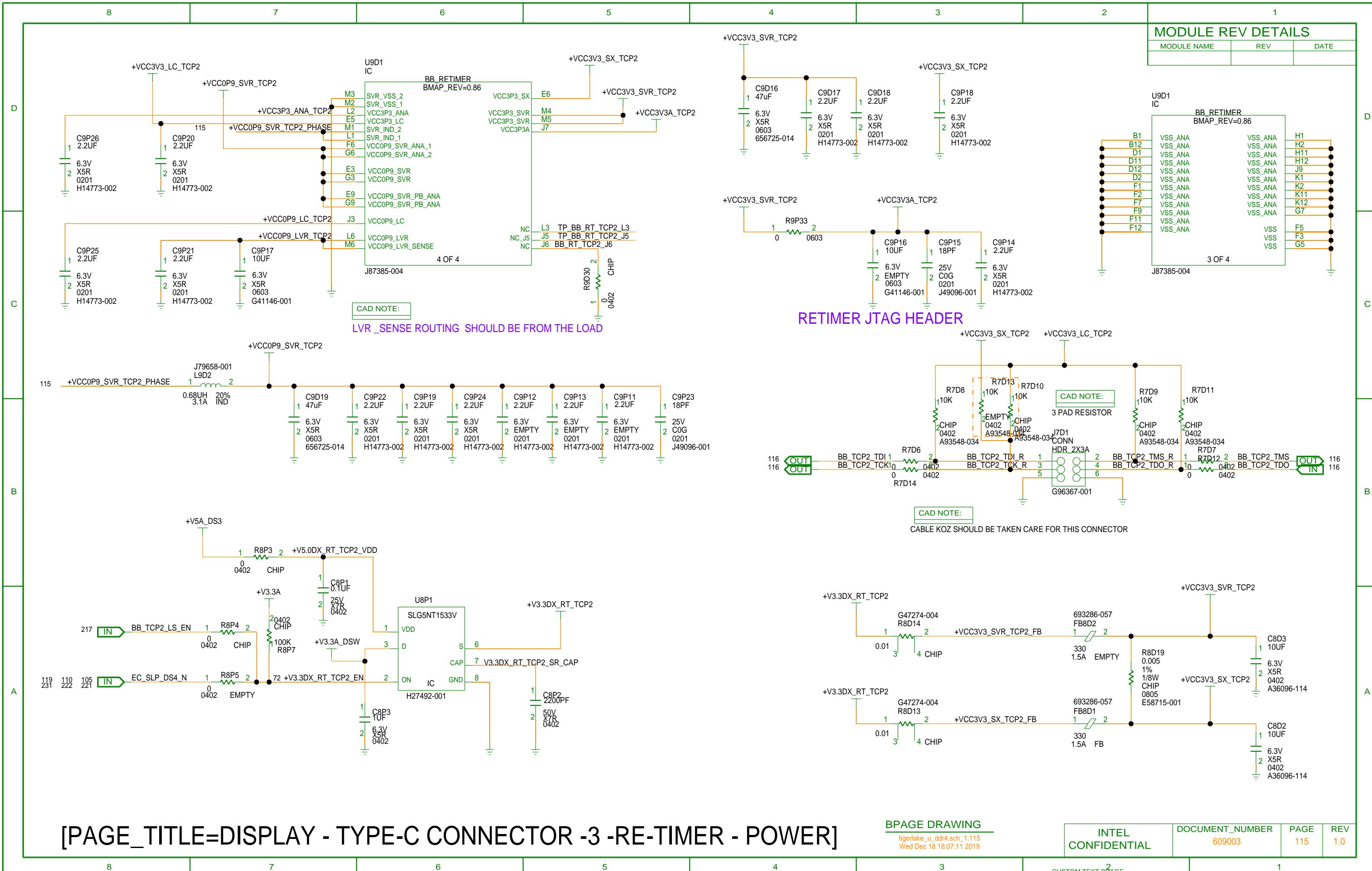


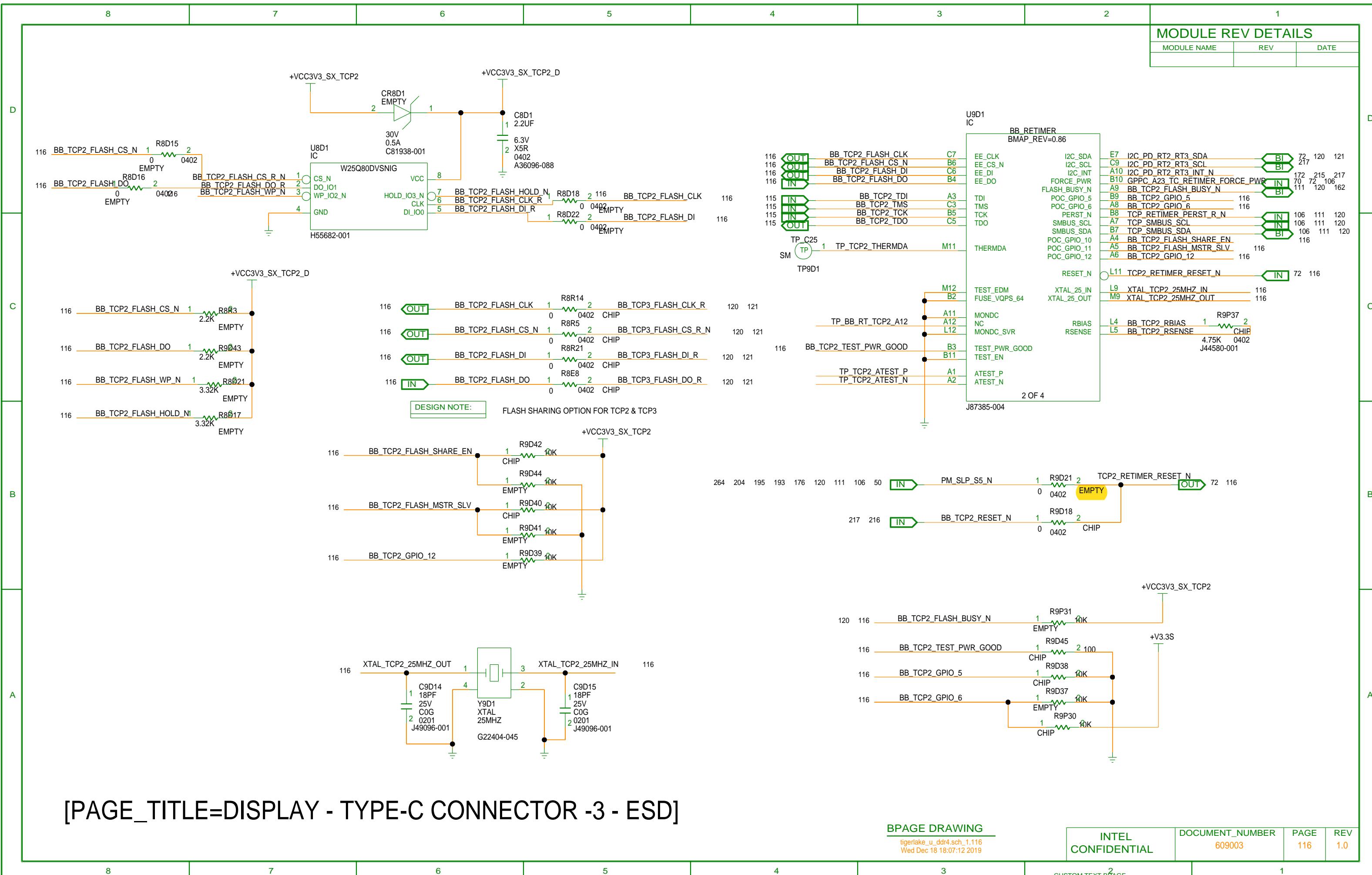


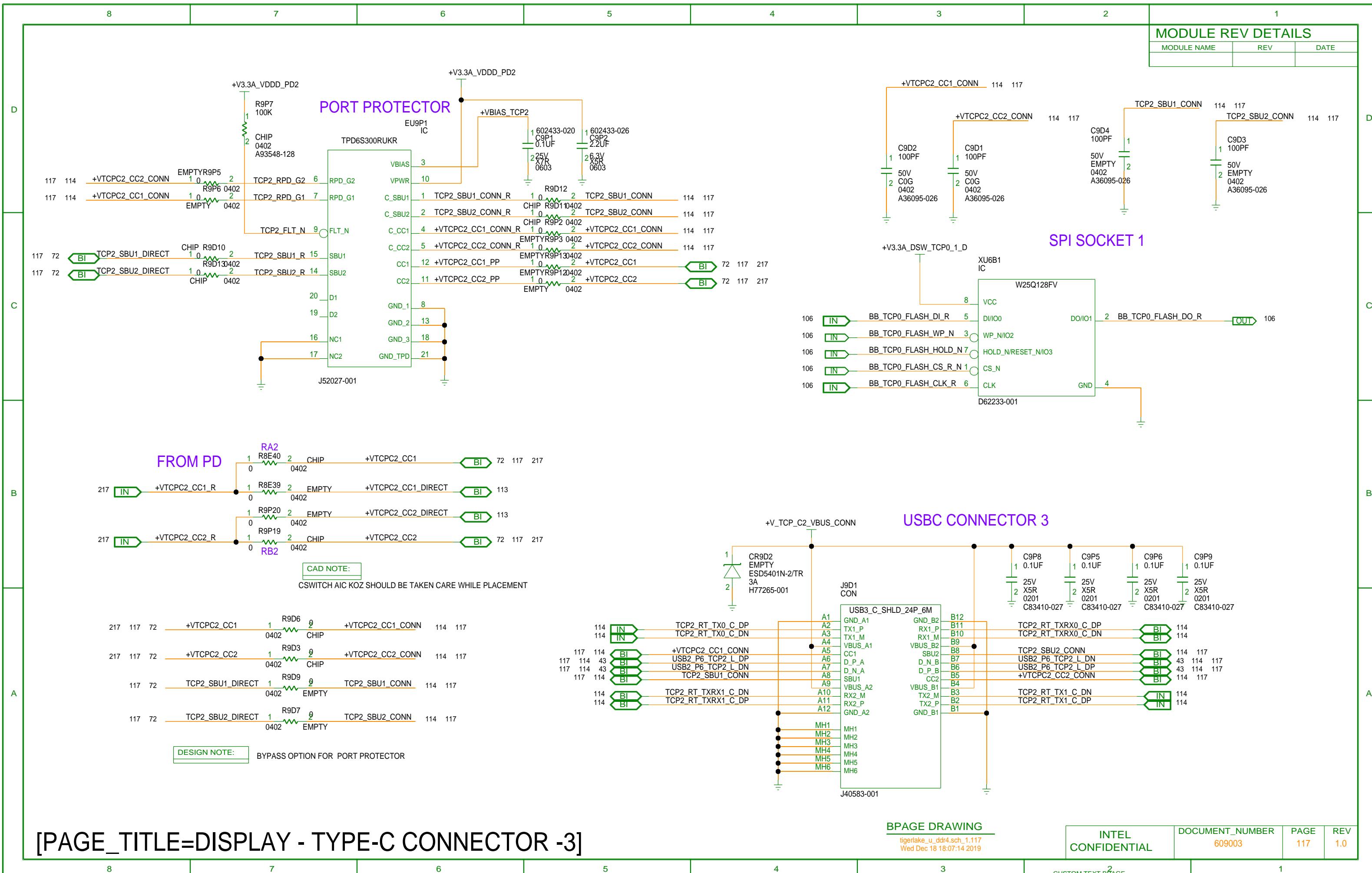


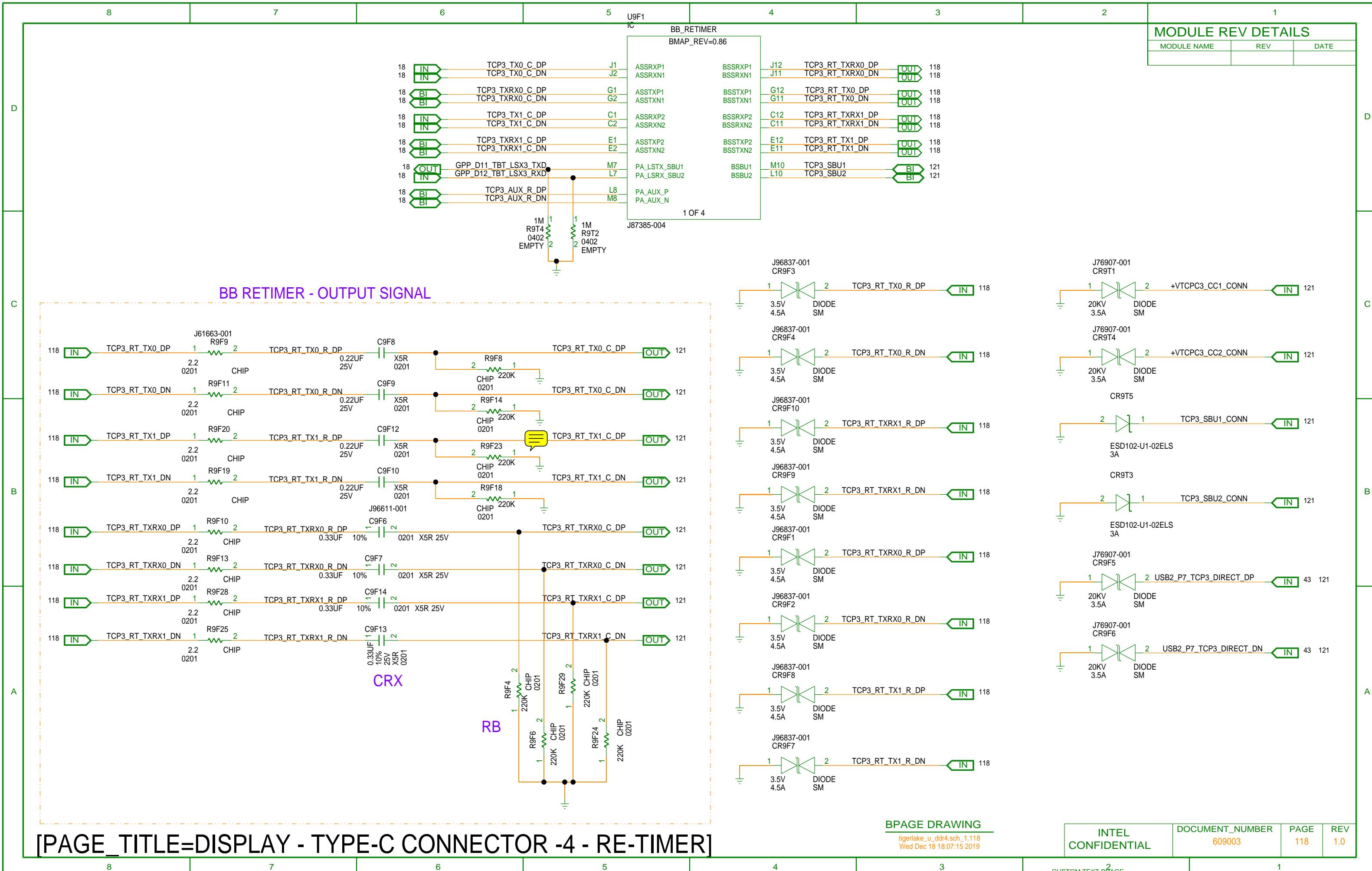


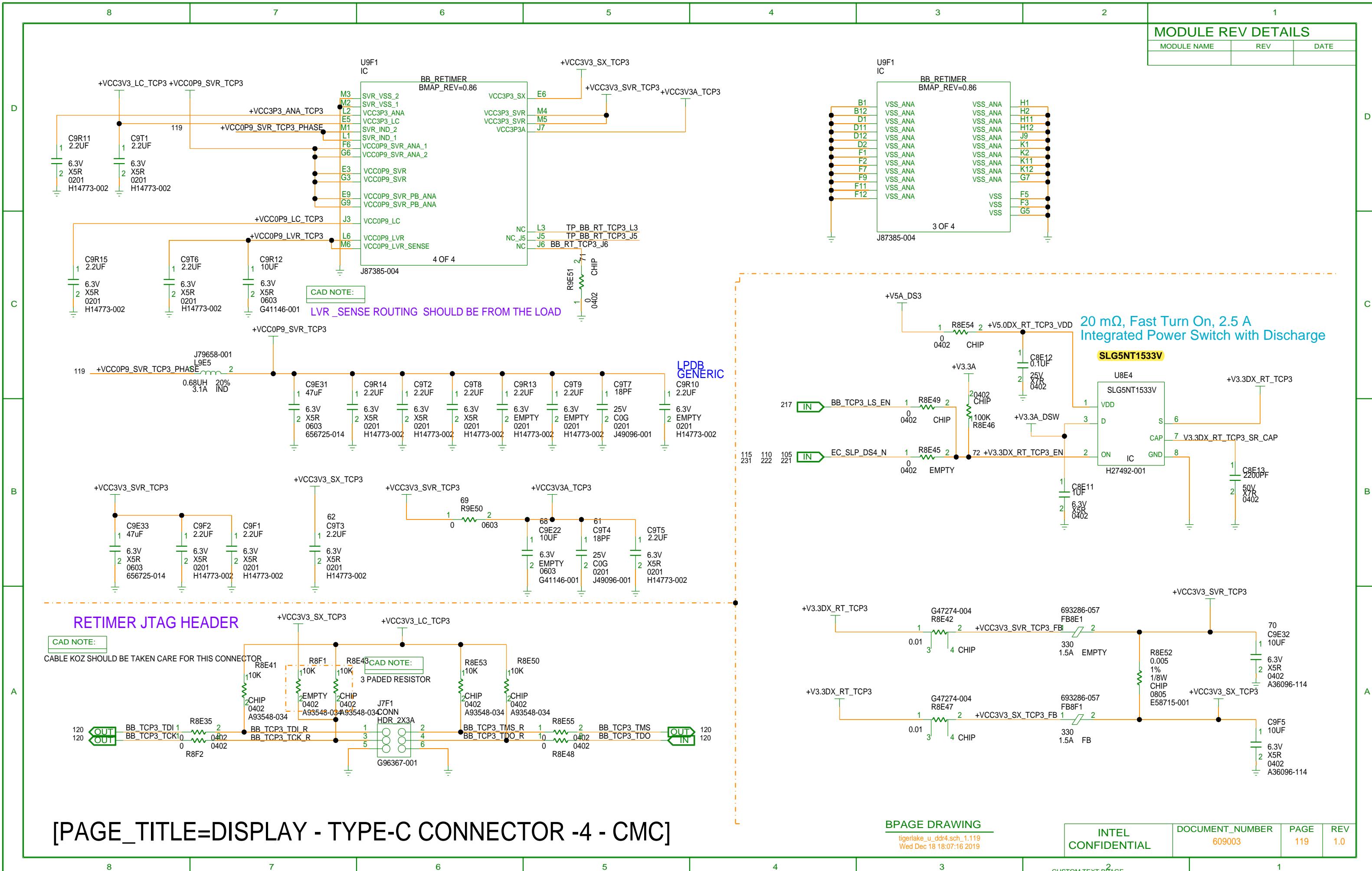


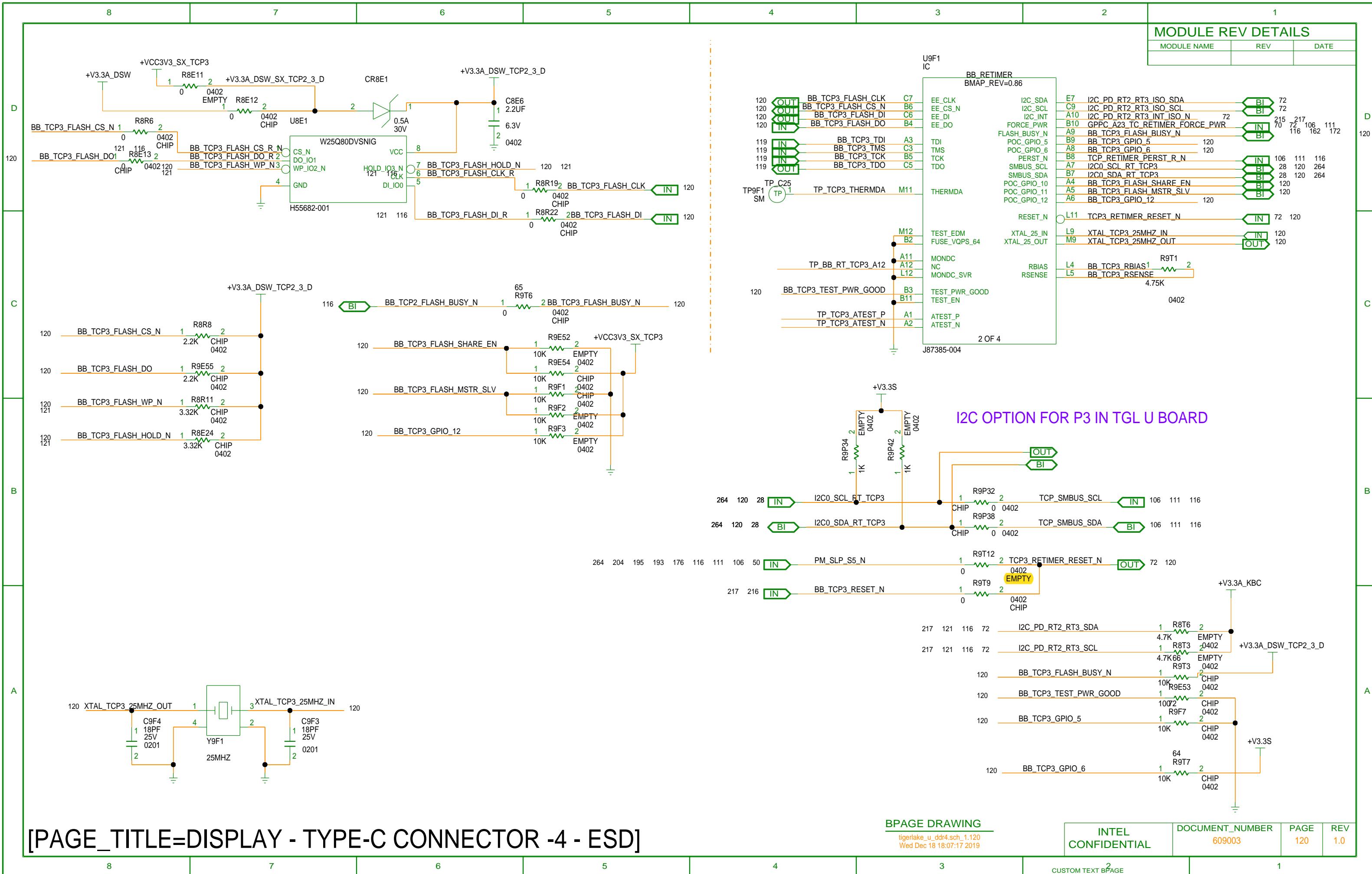


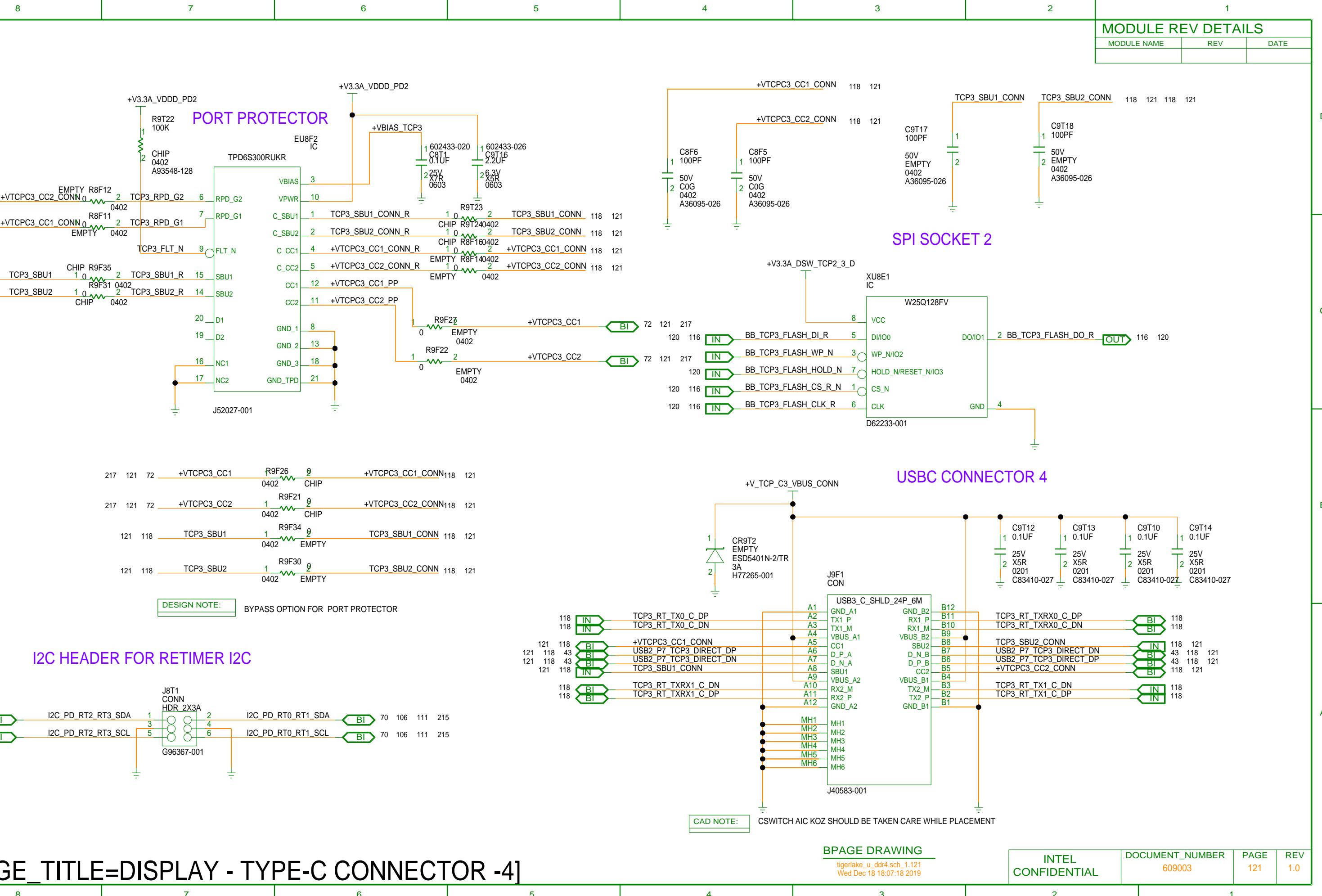


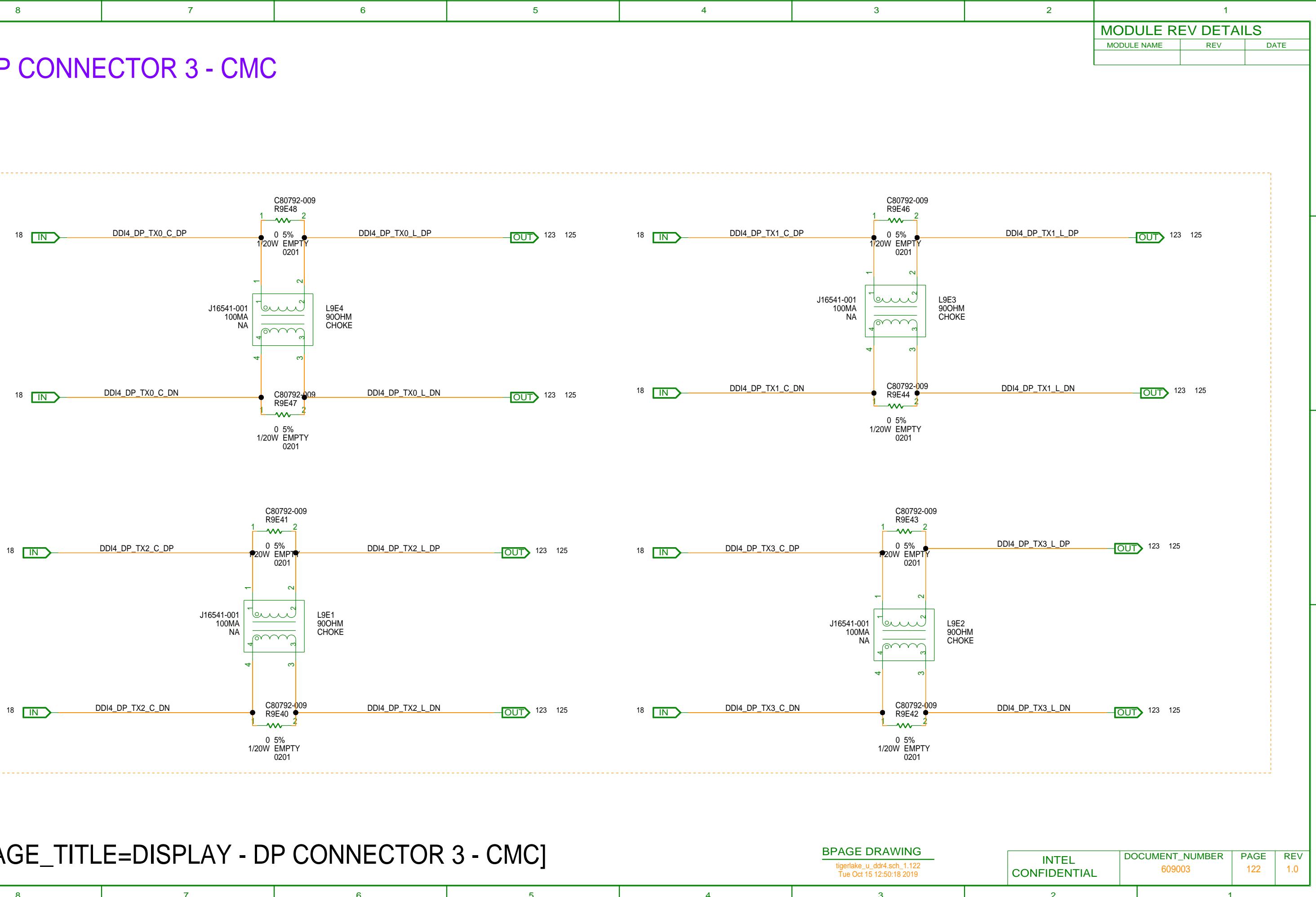








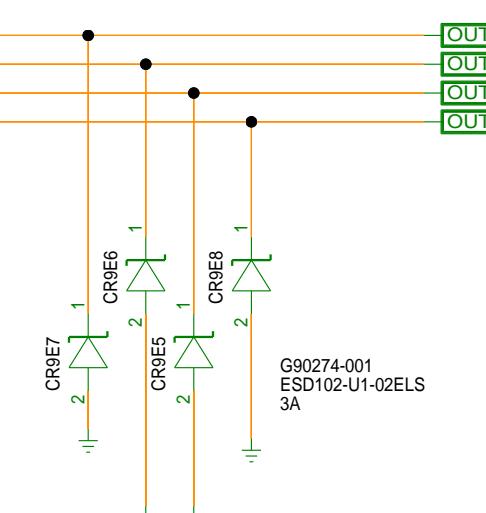
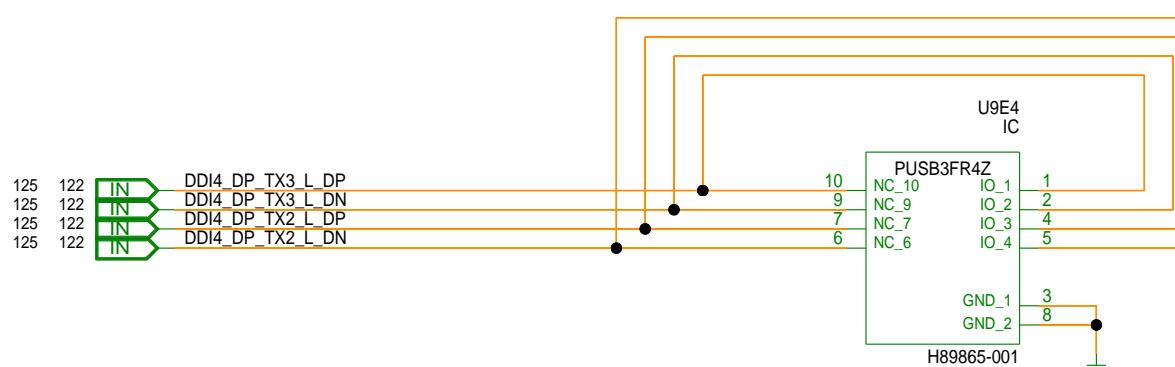
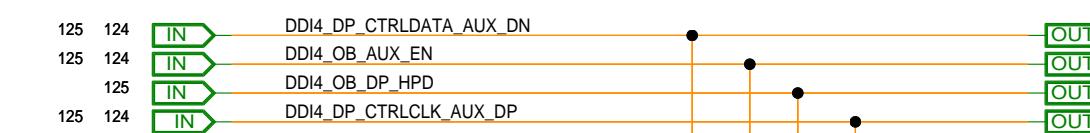
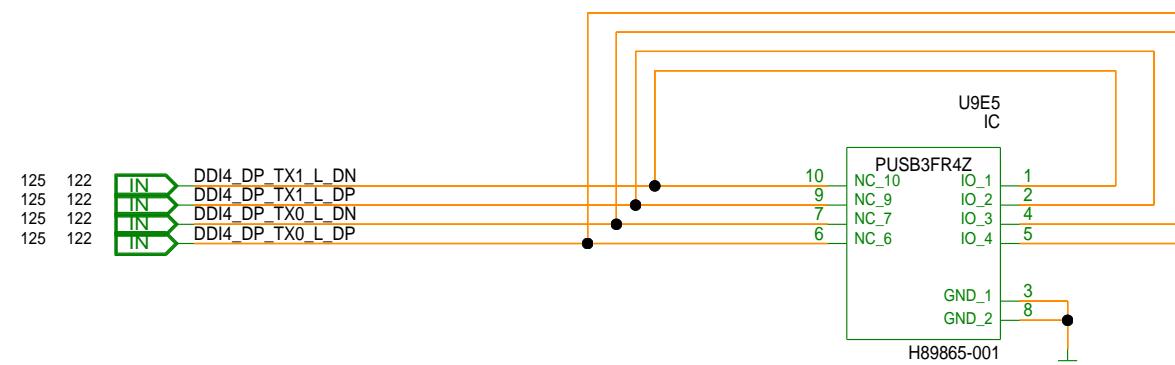




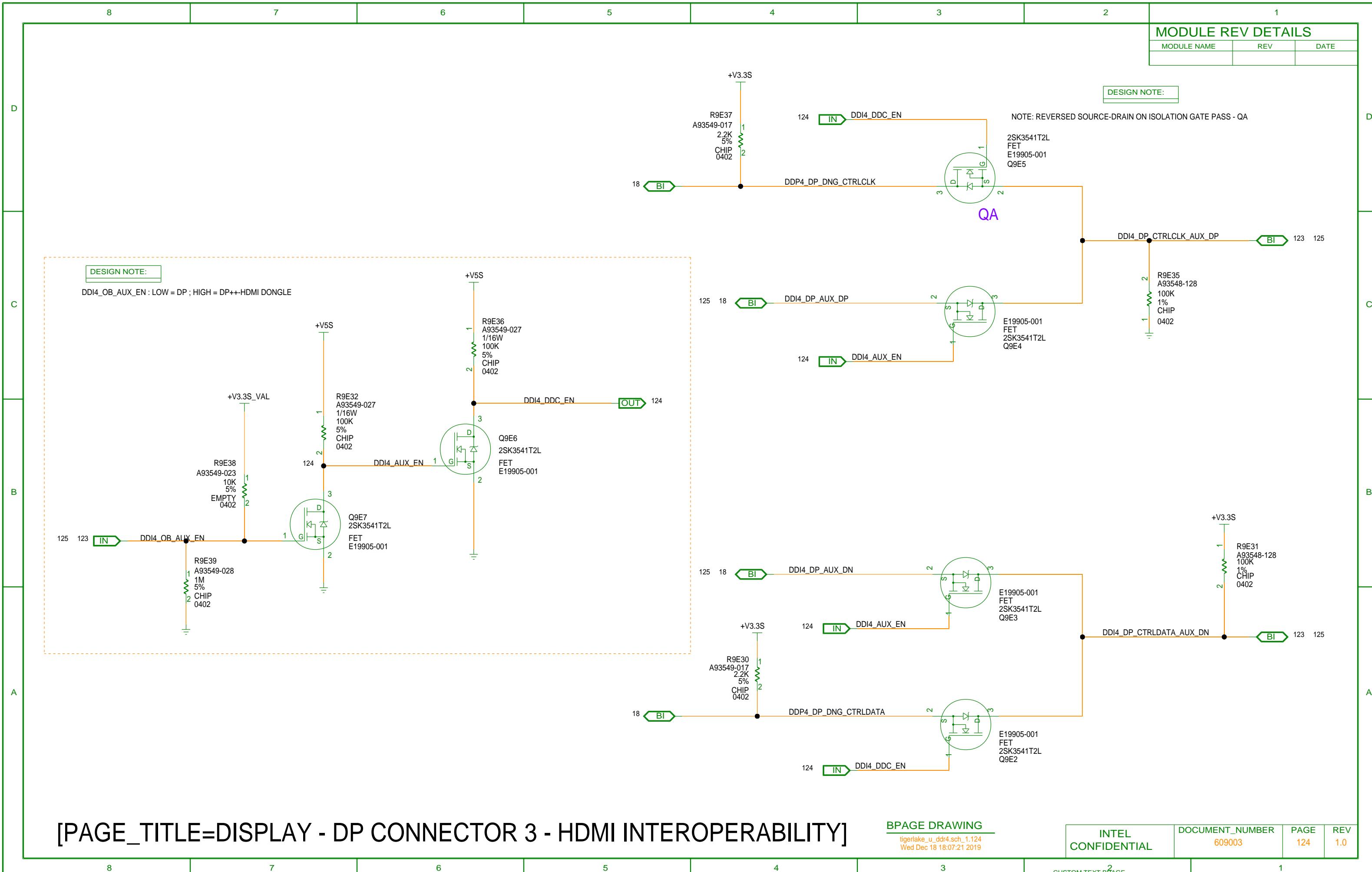
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DP CONNECTOR 3 - ESD

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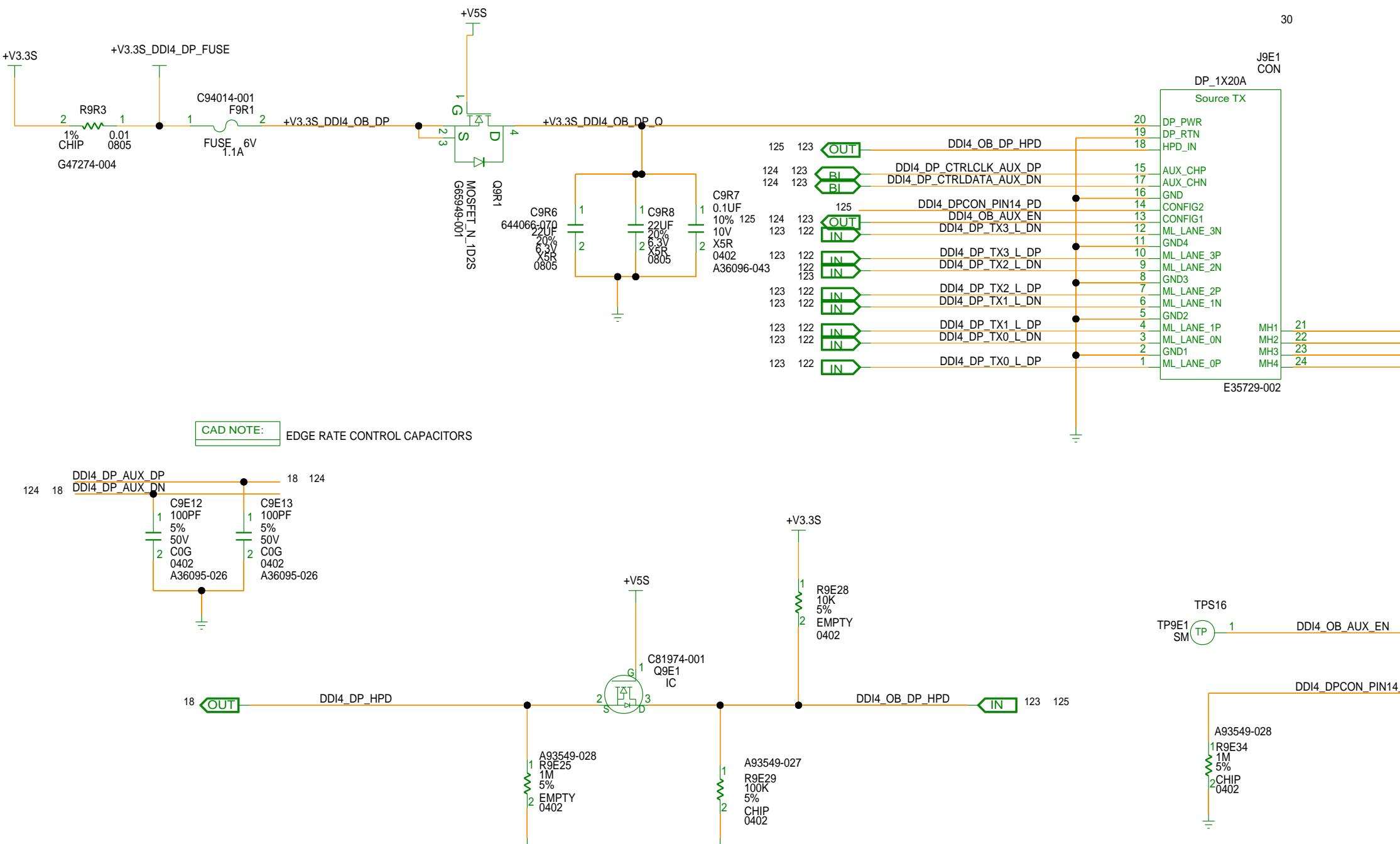


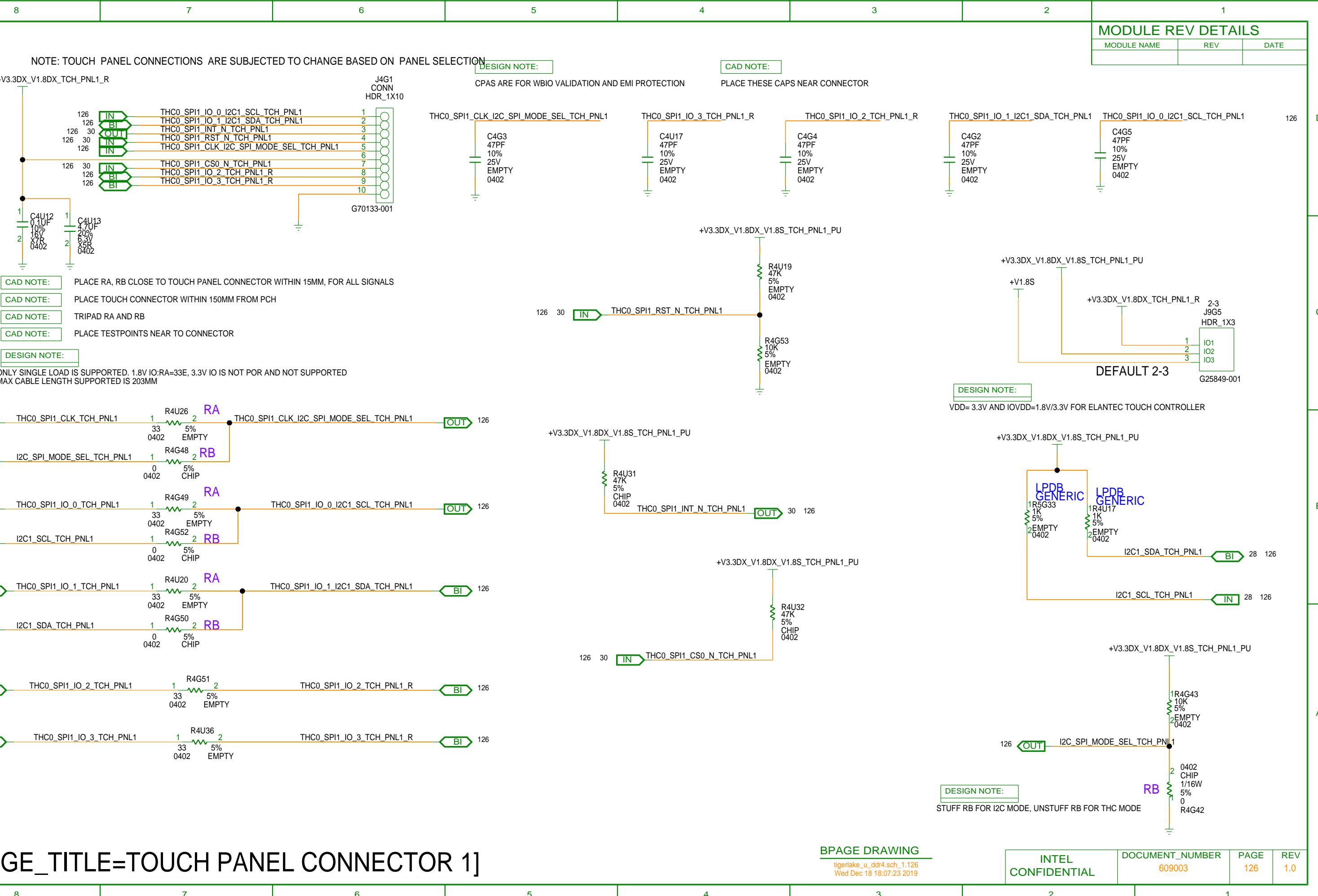
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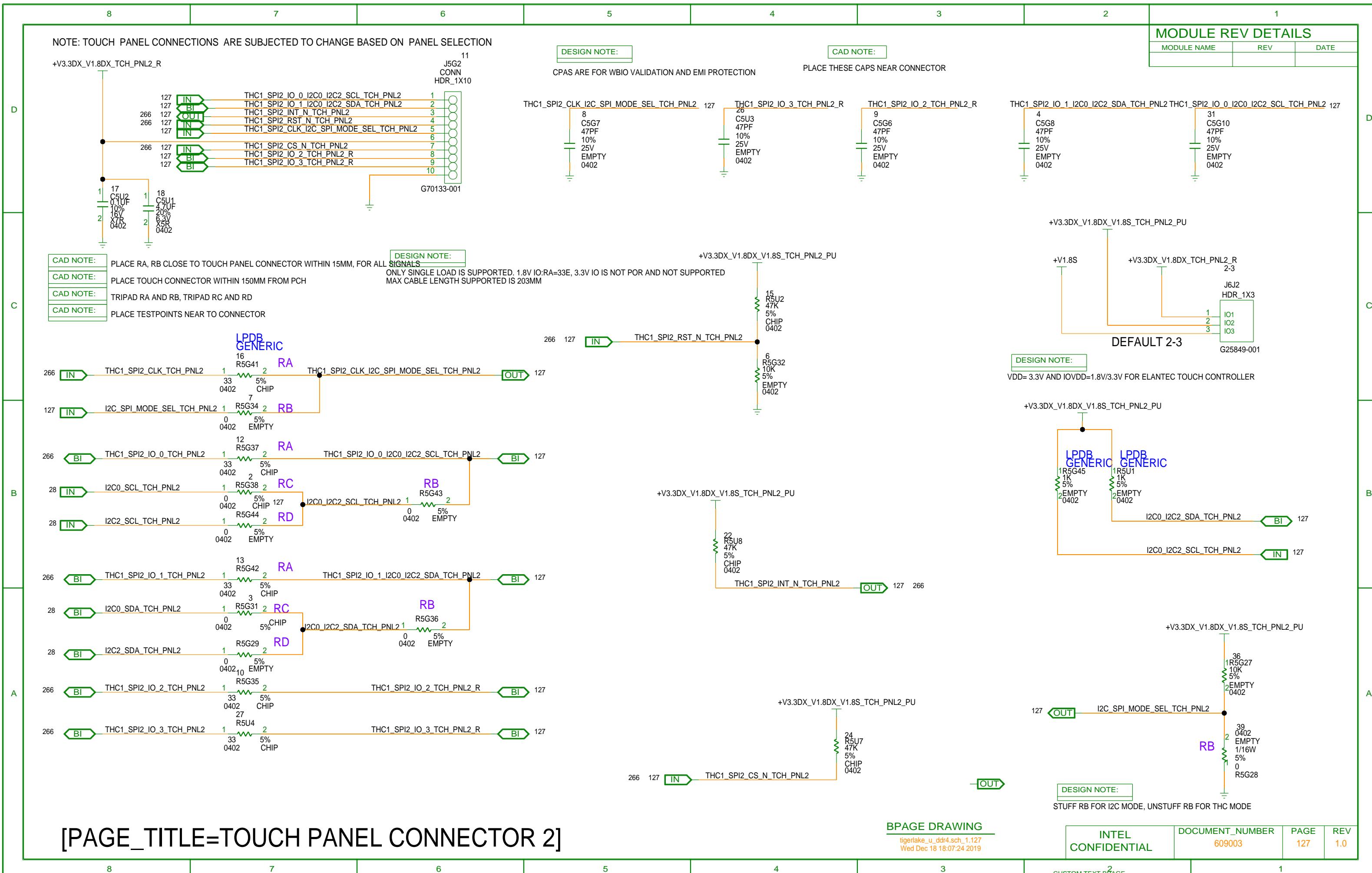


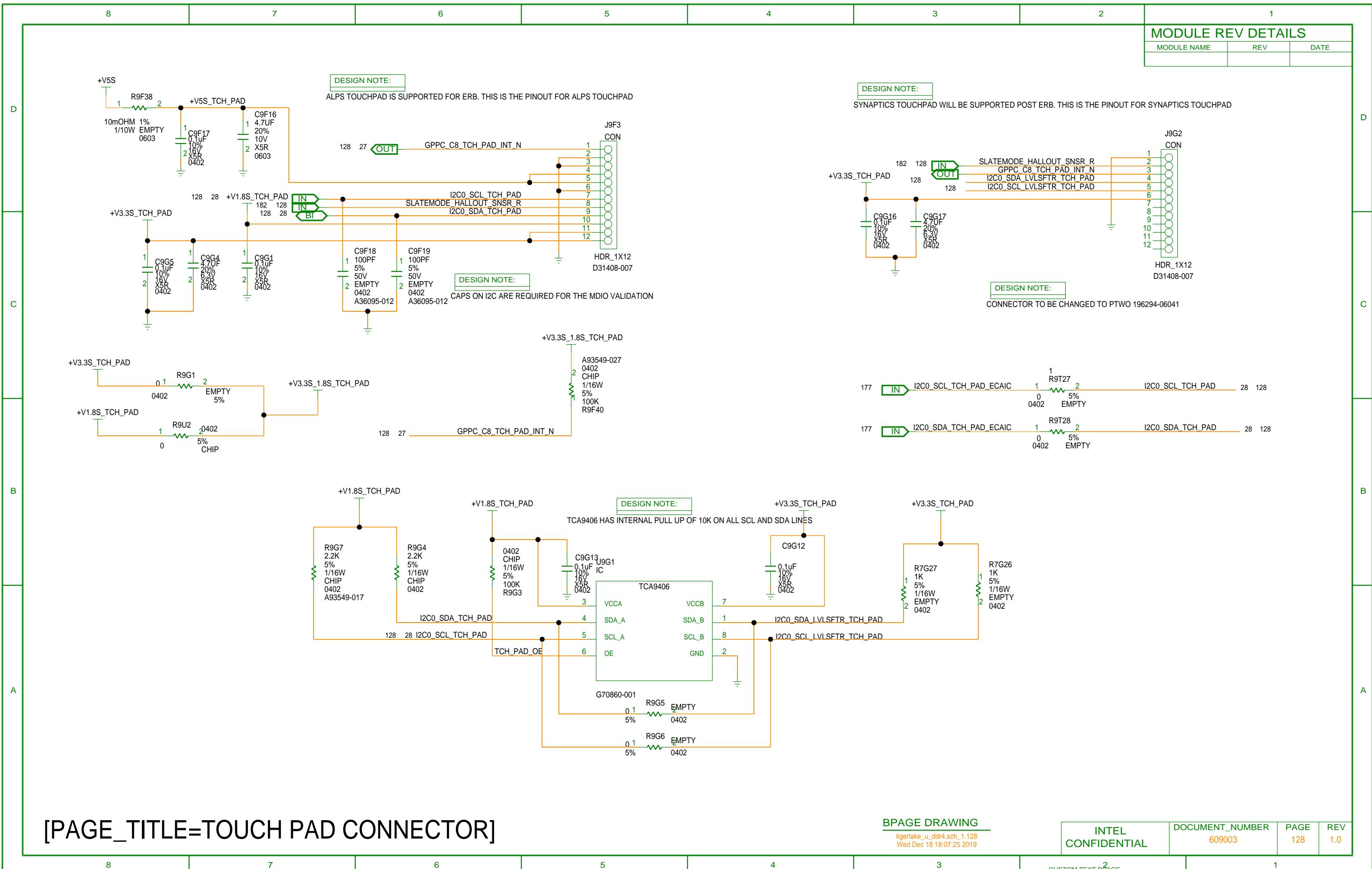
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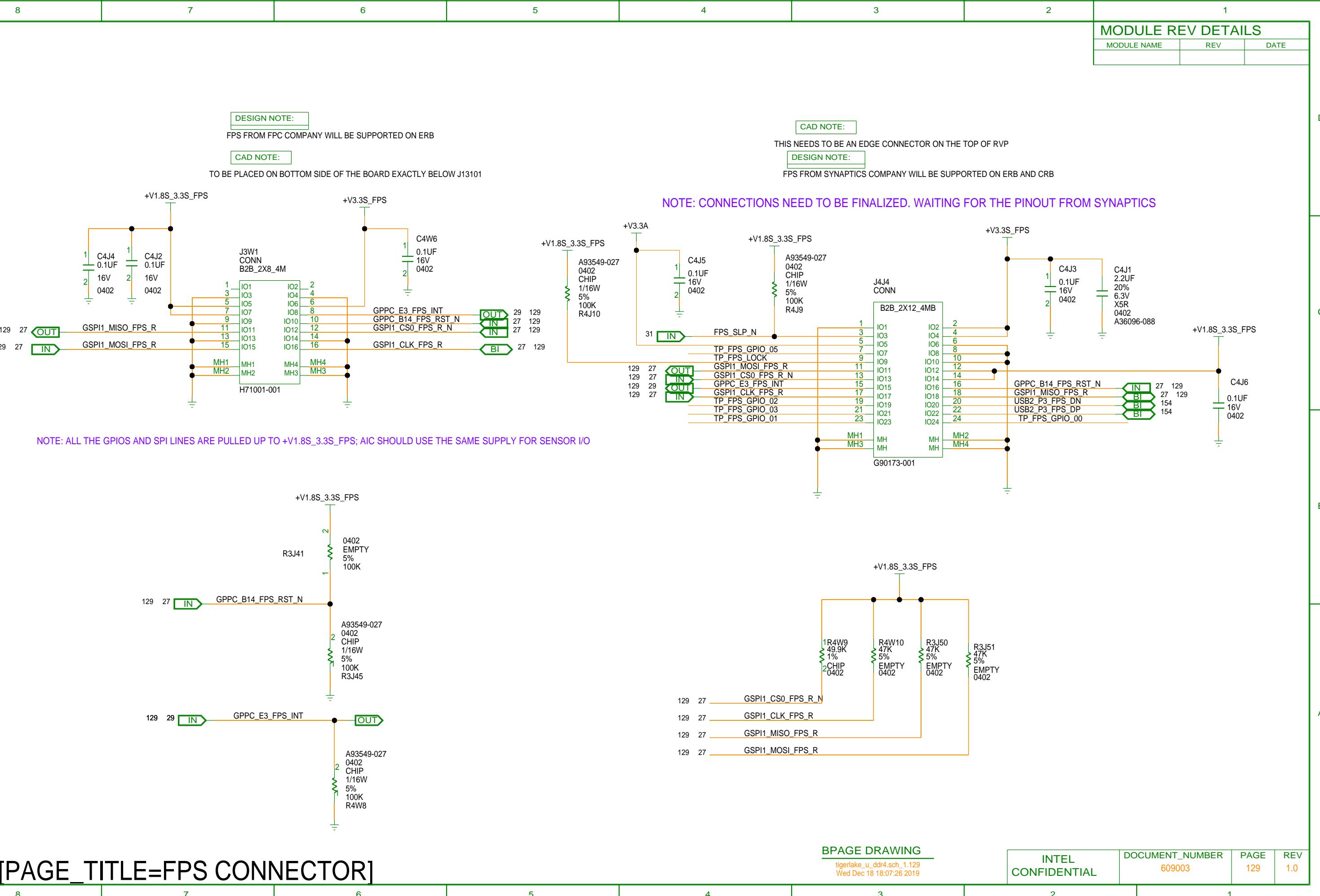
MODULE REV DETAILS		
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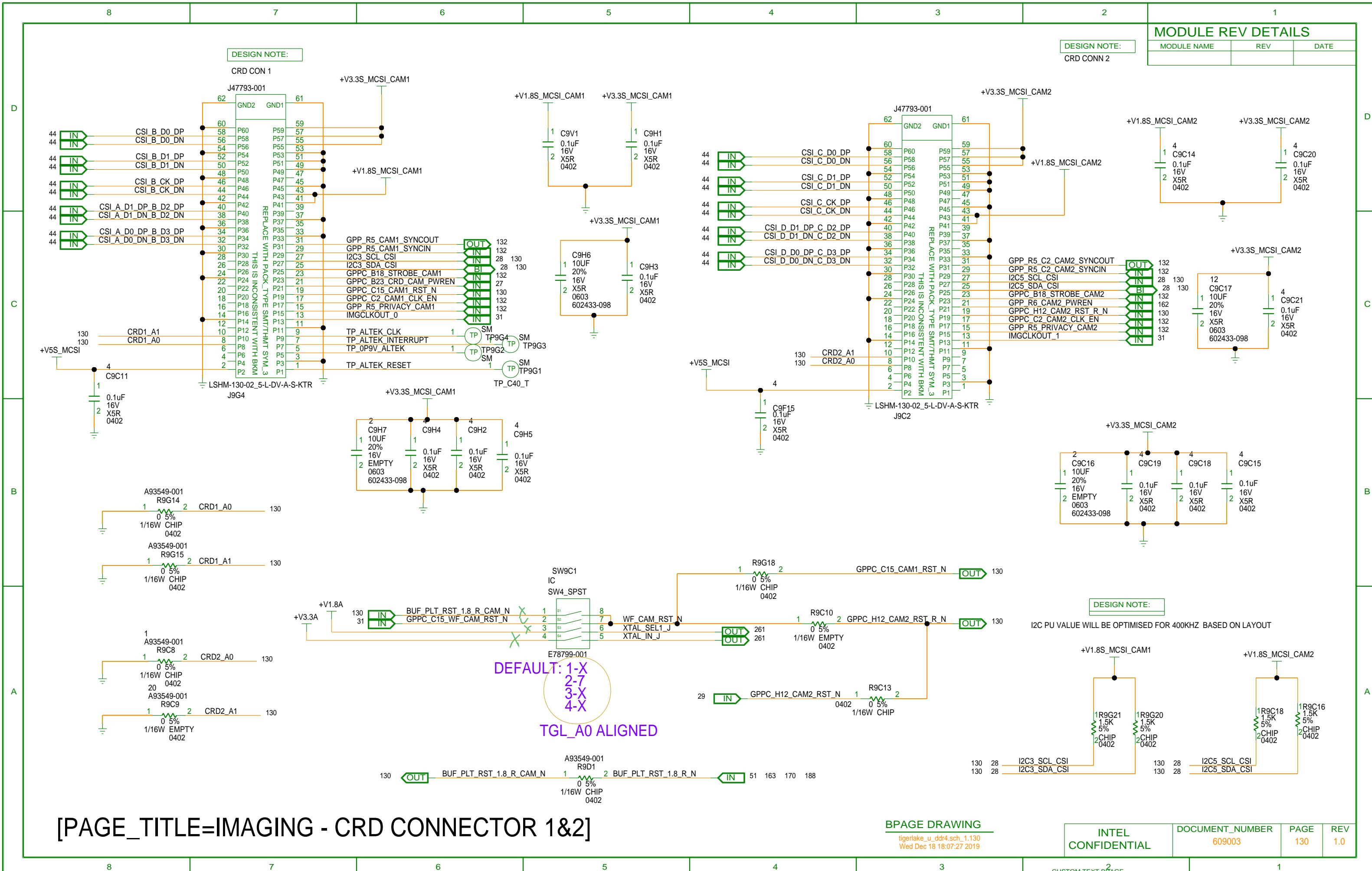








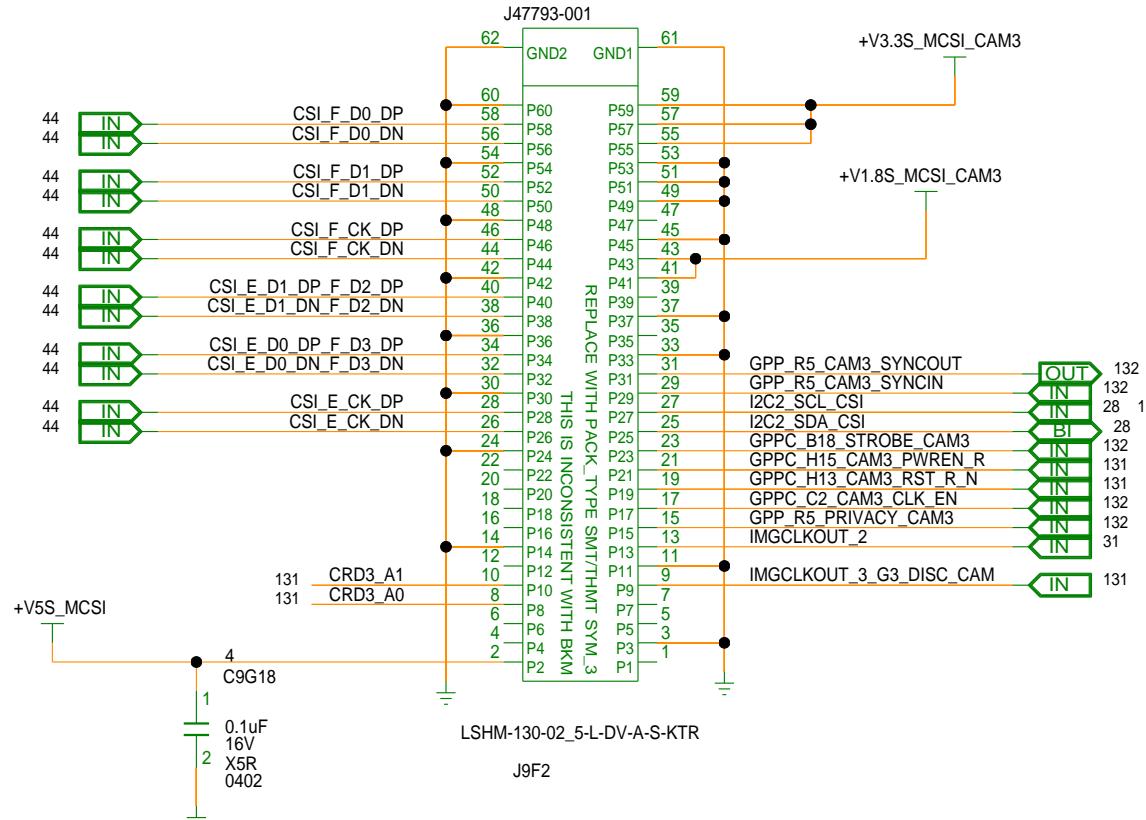




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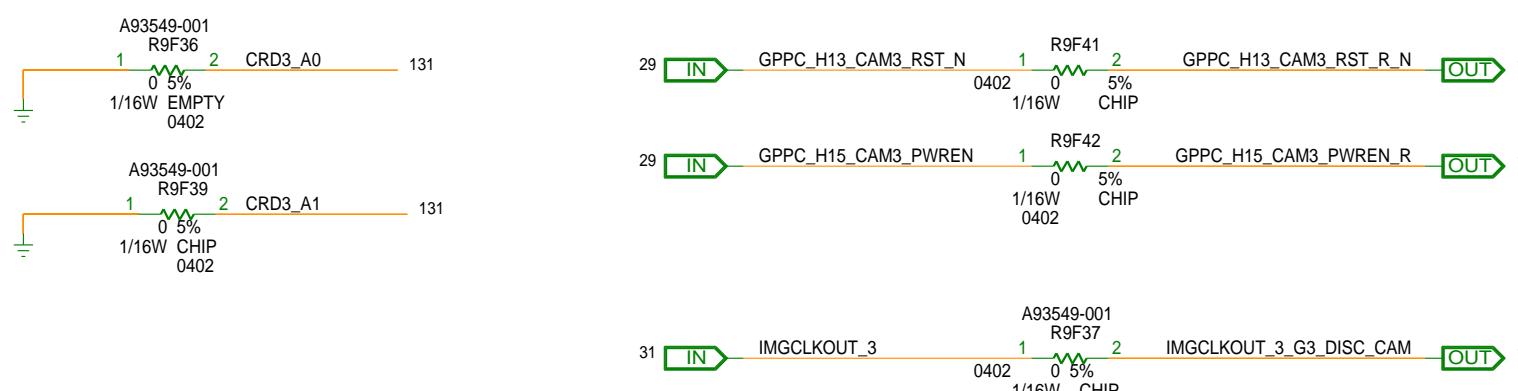
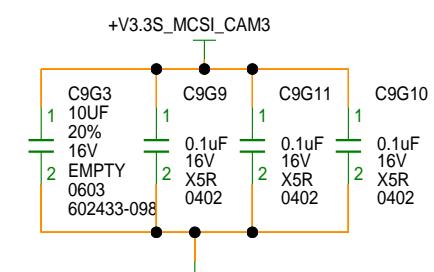
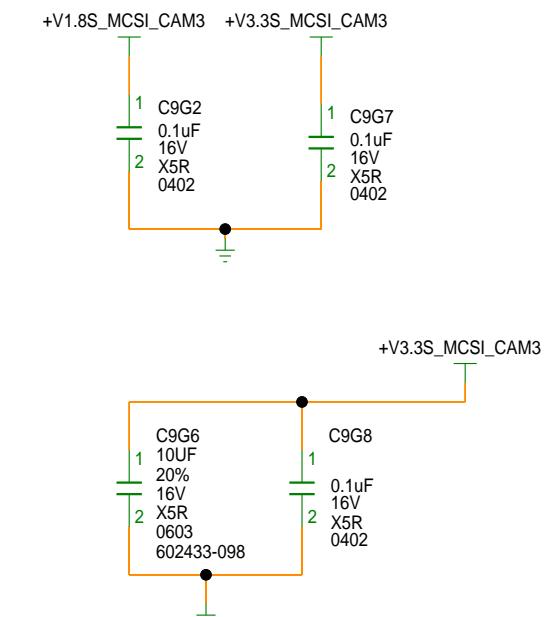
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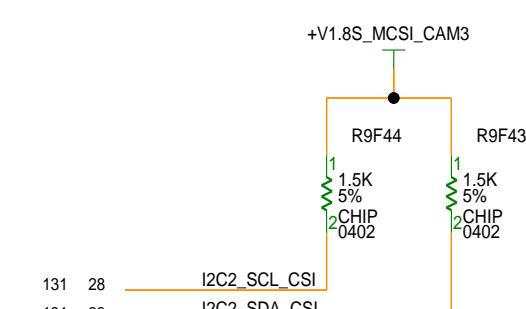


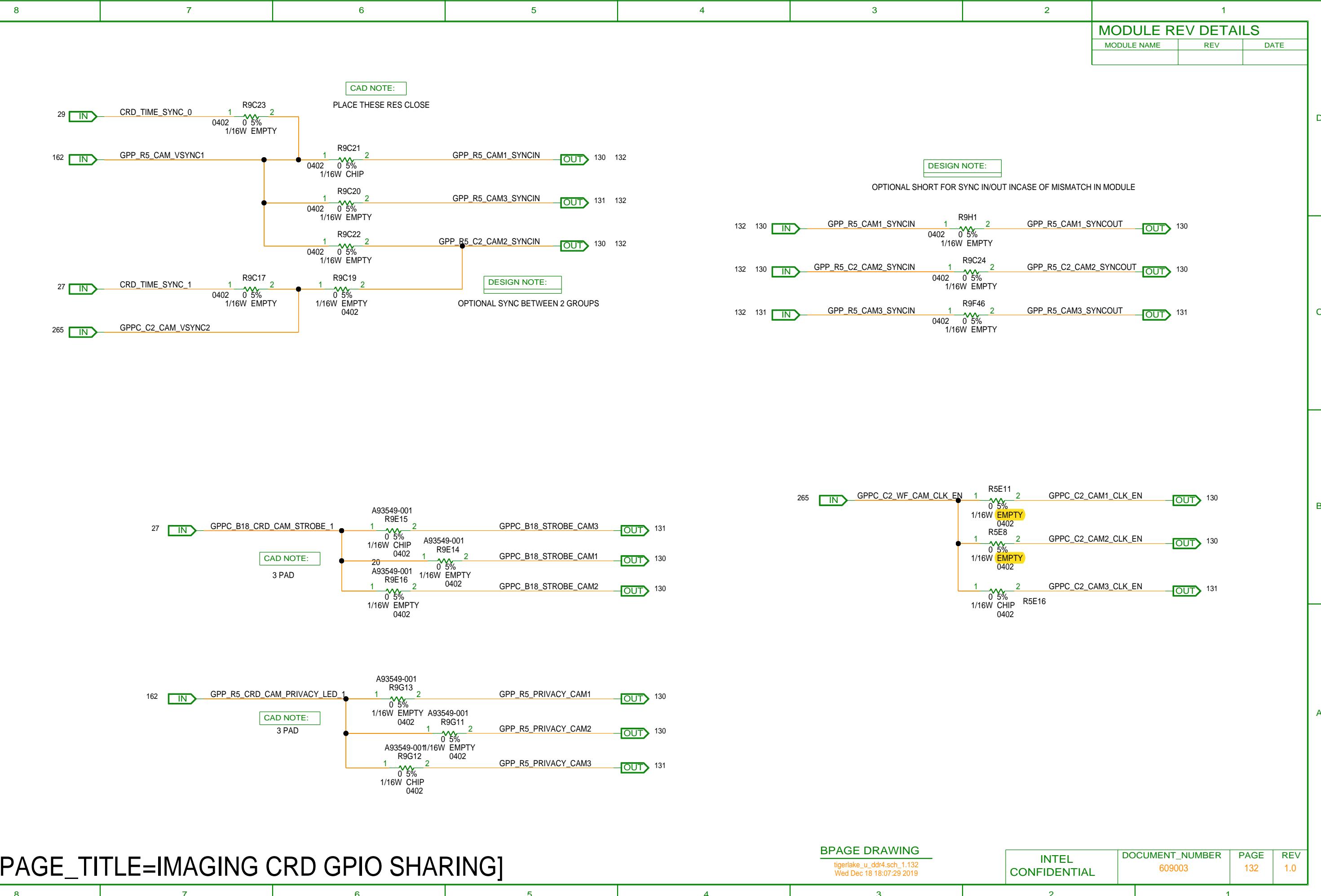
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MODULE NAME	REV	DATE



I2C PU VALUE WILL BE OPTIMISED FOR 400KHZ BASED ON LAYOUT





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MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 133	REV 1.0
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MODULE REV DETAILS

MODULE NAME	REV	DATE

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MODULE REV DETAILS

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CUSTOM TEXT ²
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8	7	6	5	4	3	2	1
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MODULE NAME		REV	DATE				

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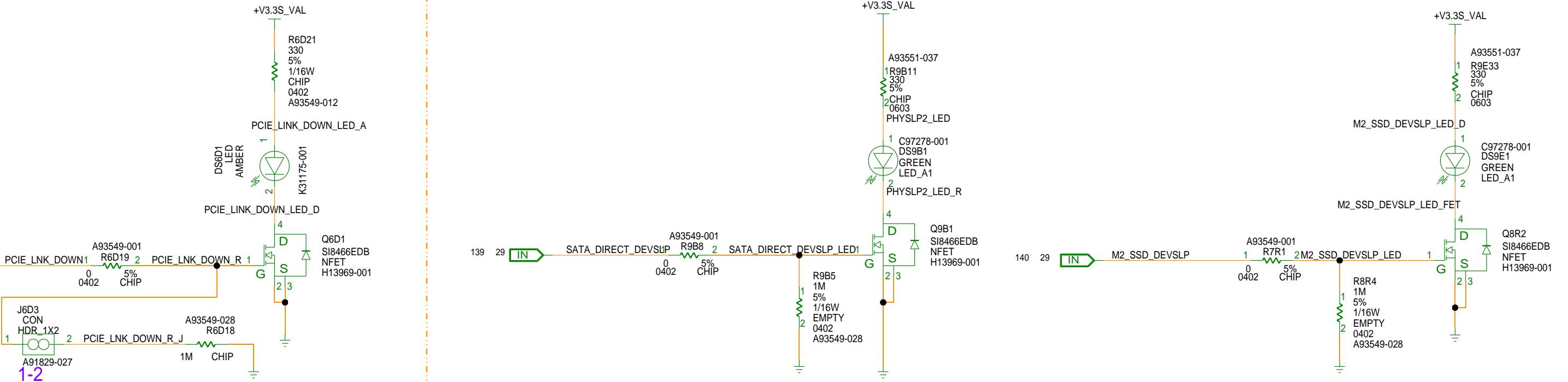
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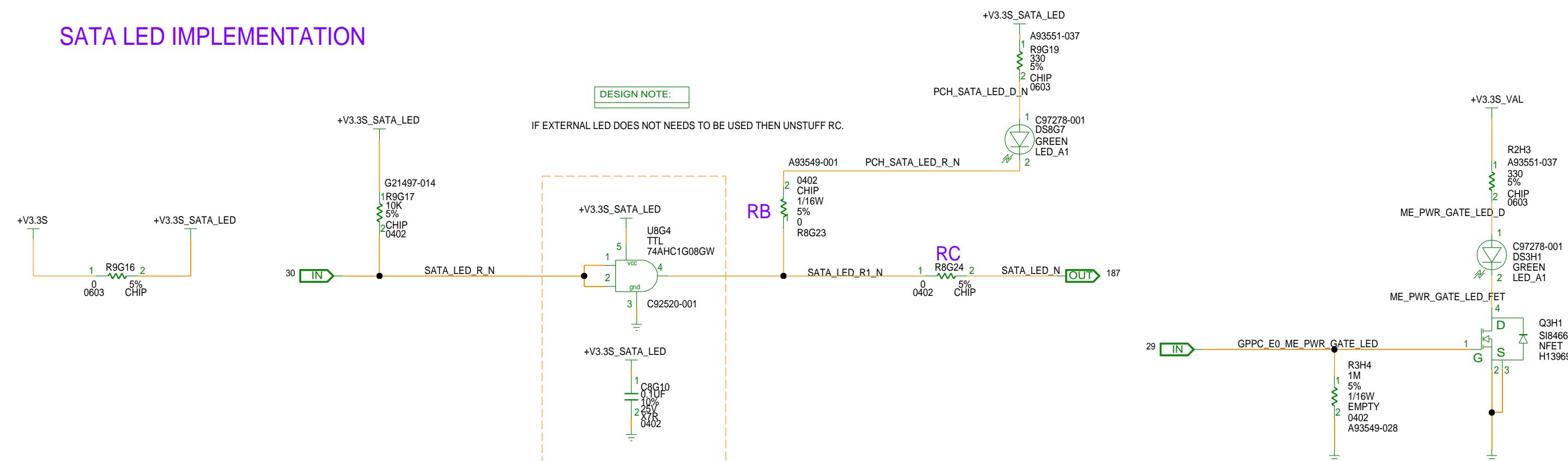
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SATA DEV SLEEP LED

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MODULE NAME	REV	DATE



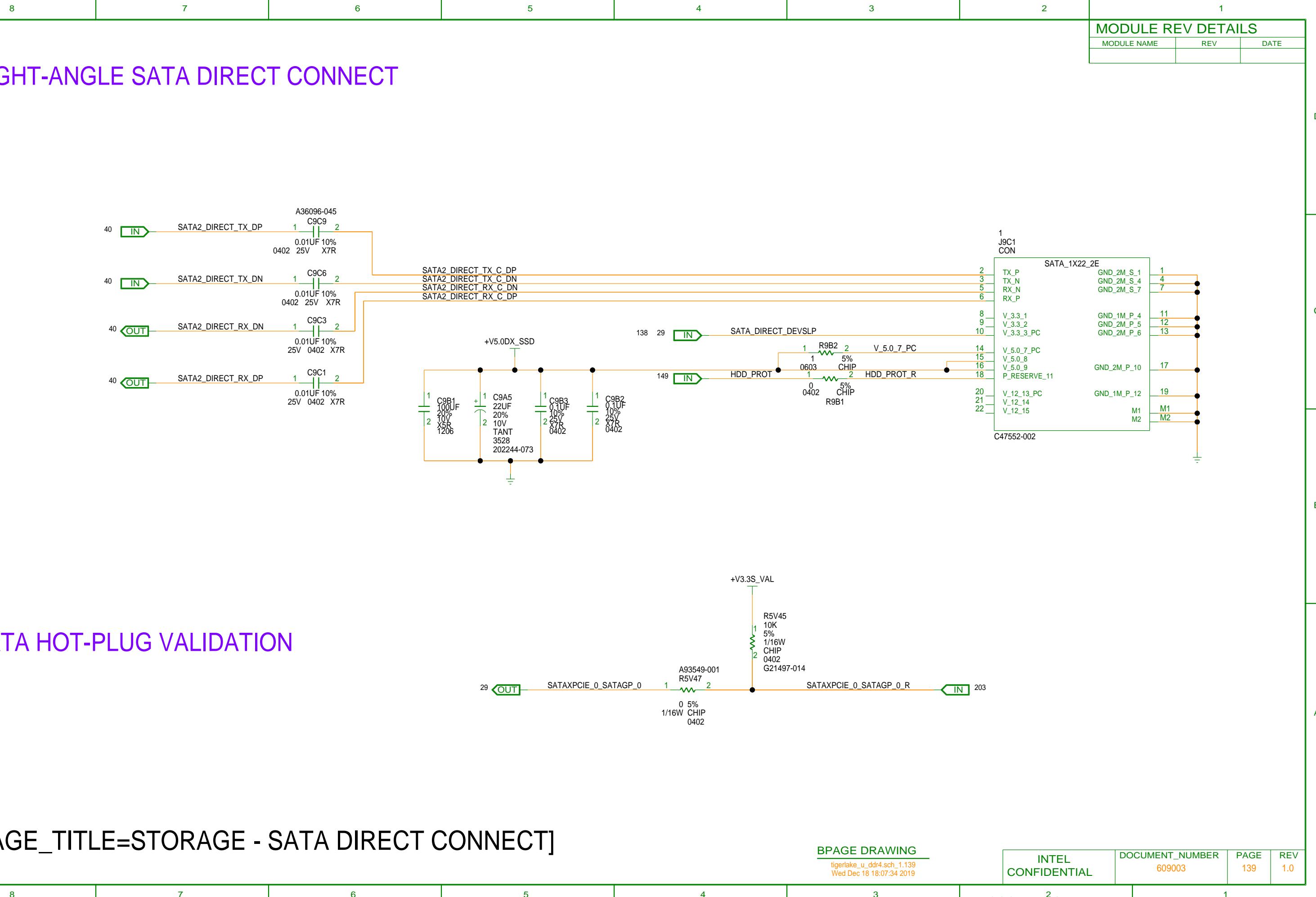
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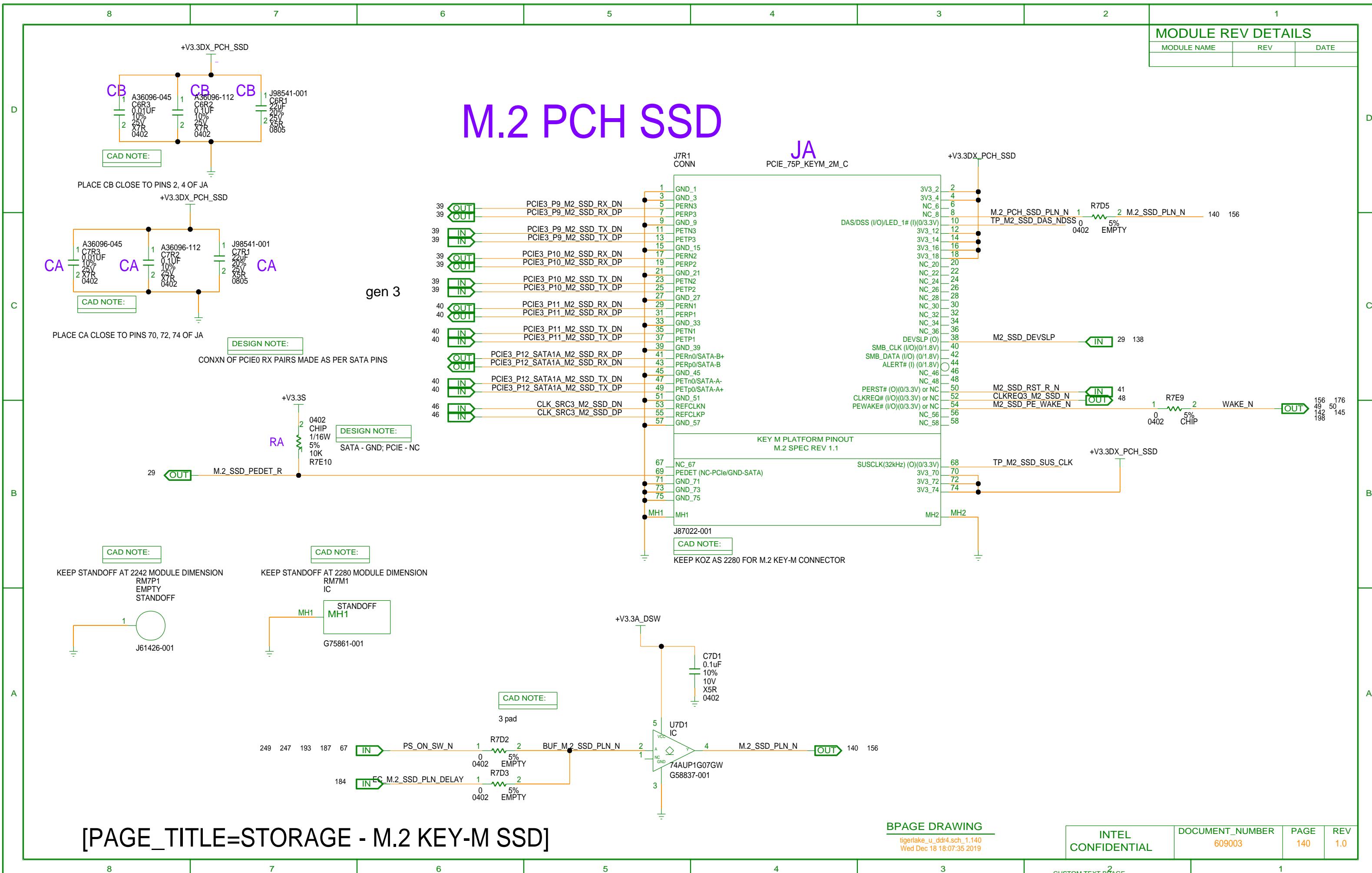


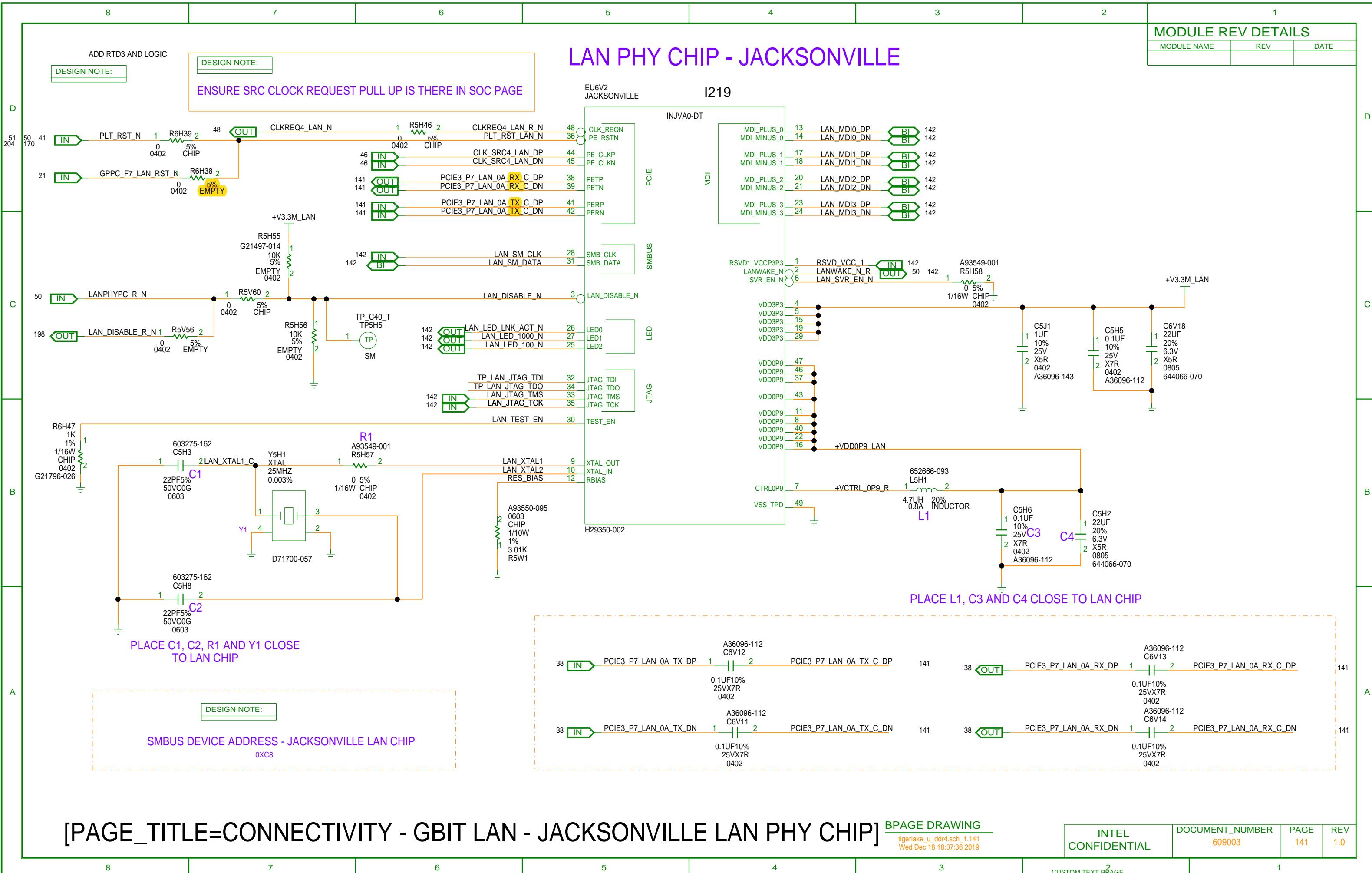
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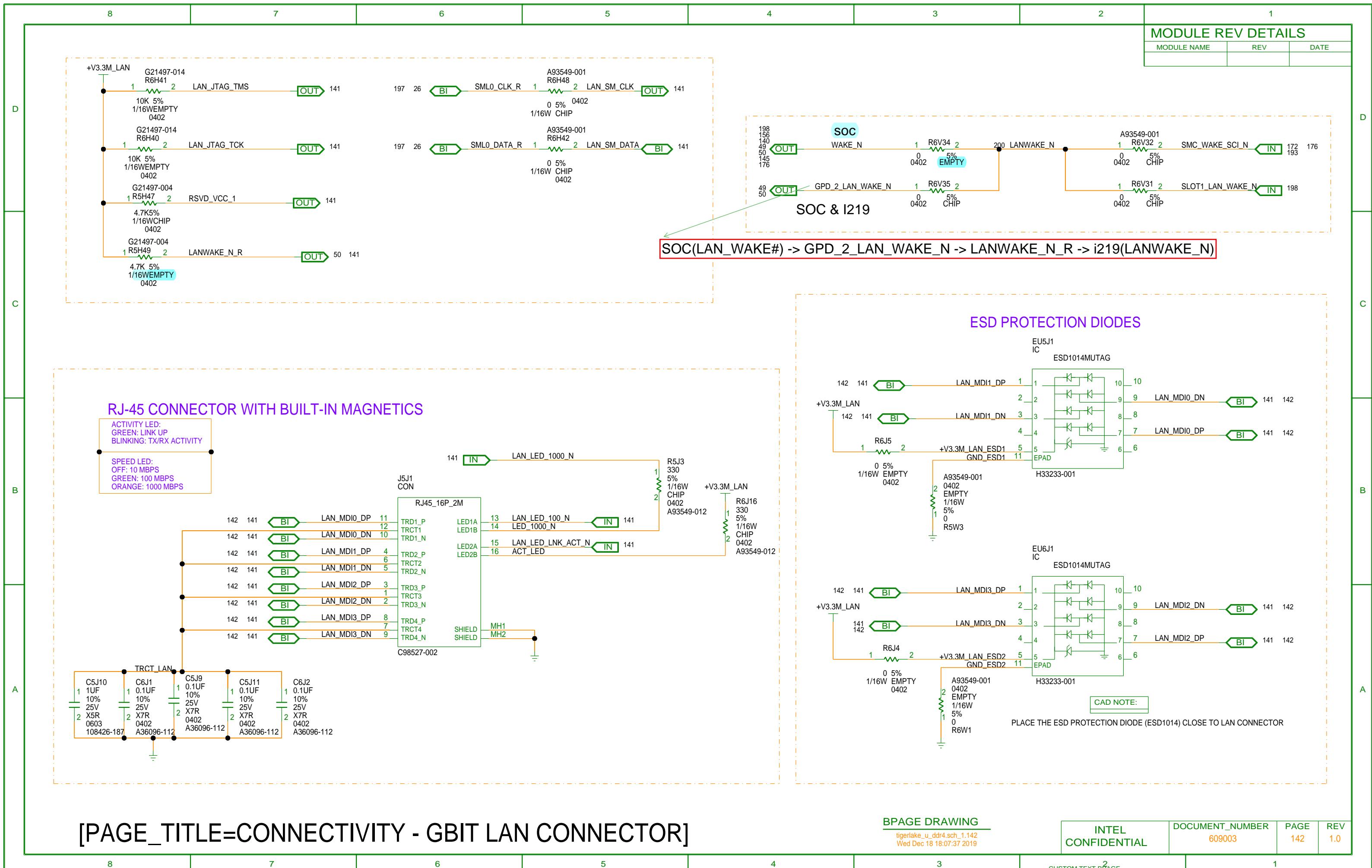
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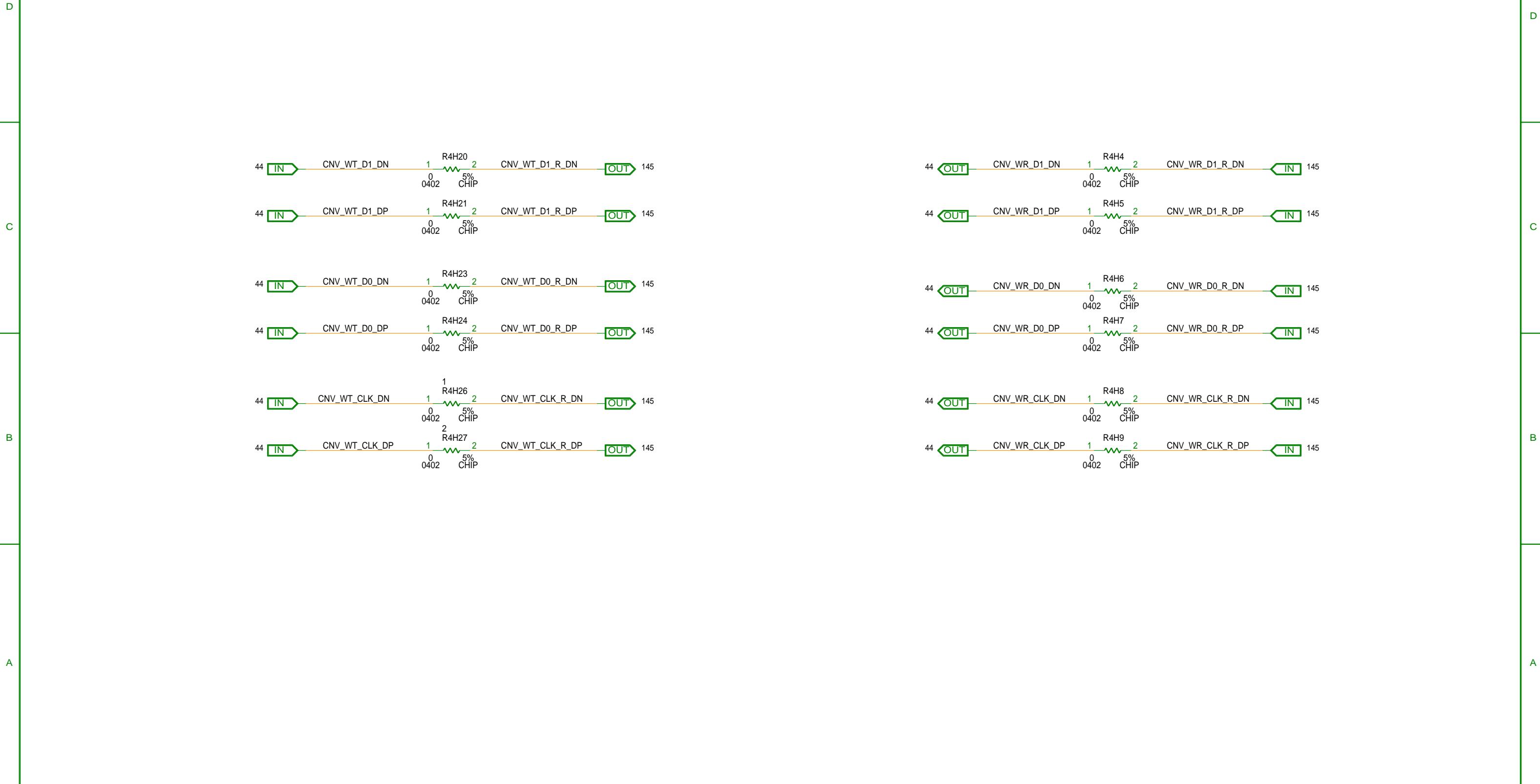








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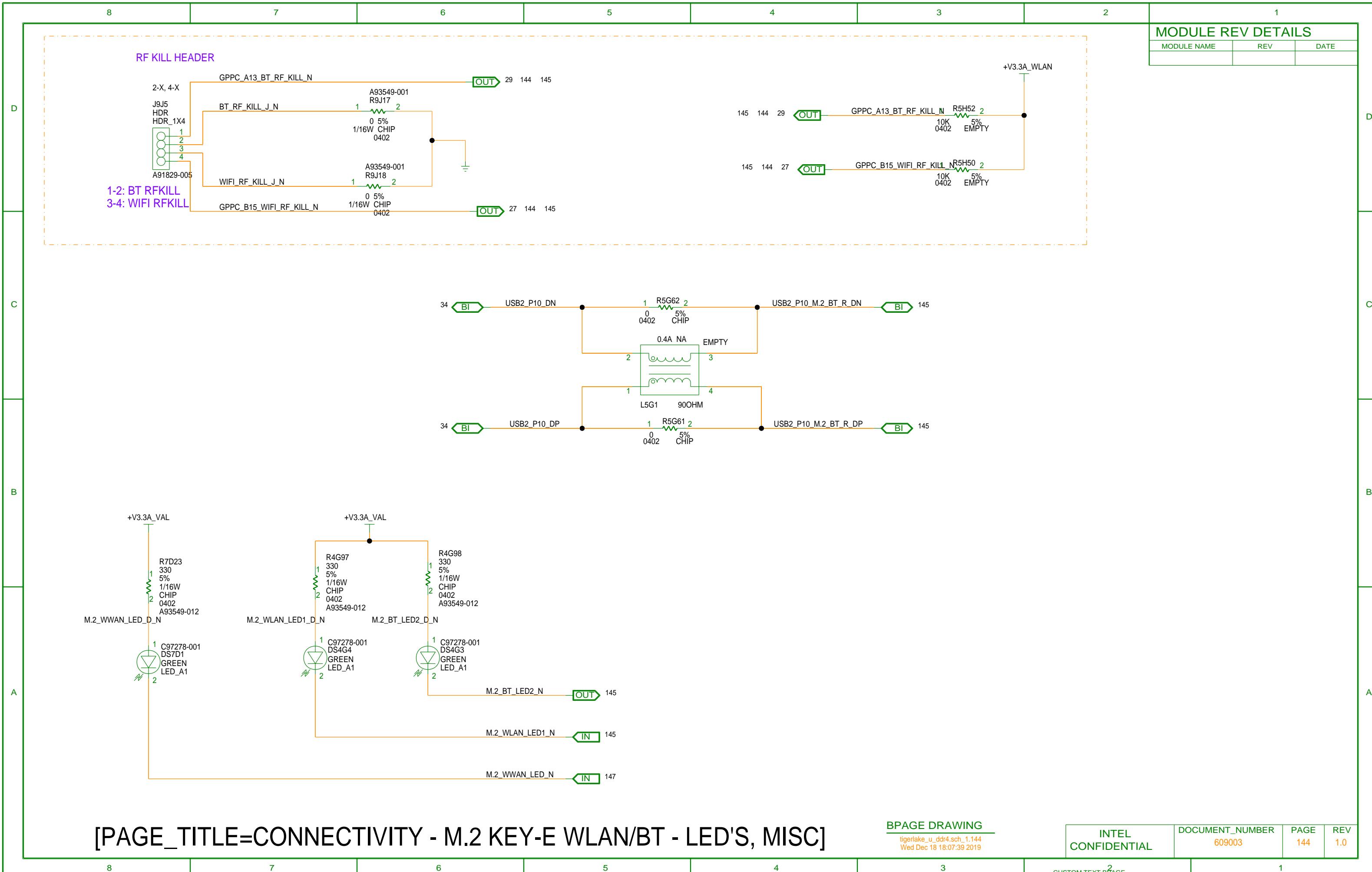


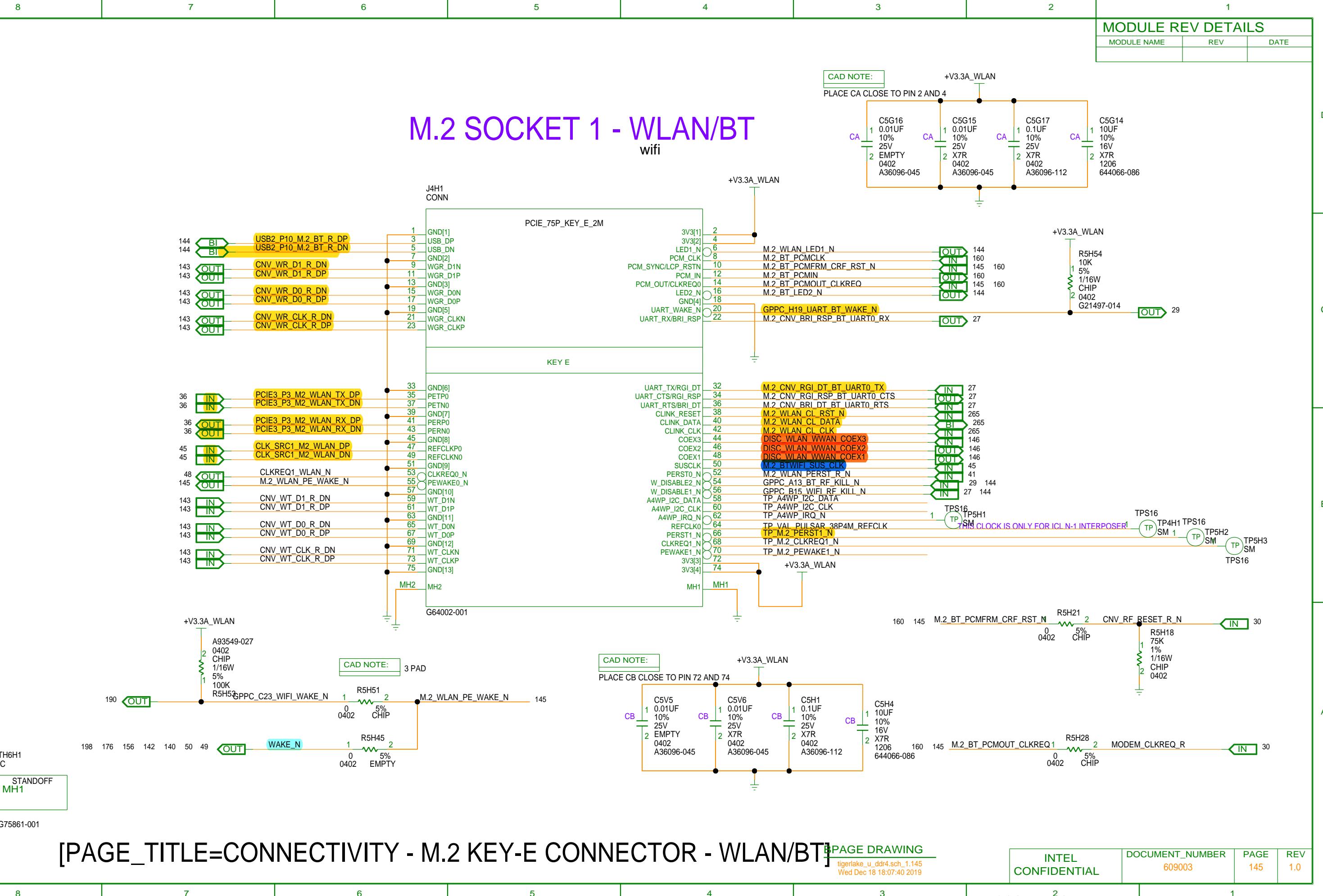
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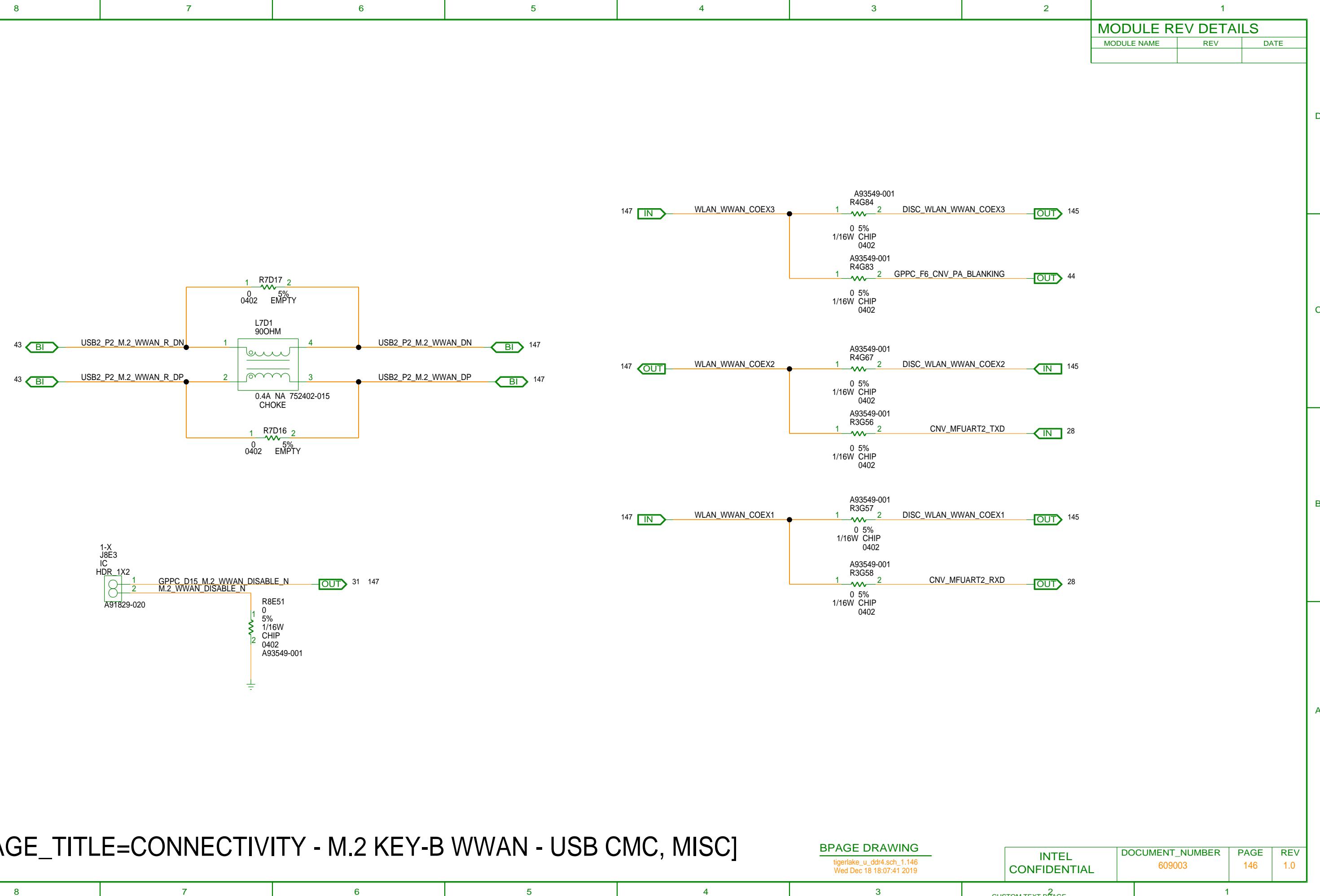
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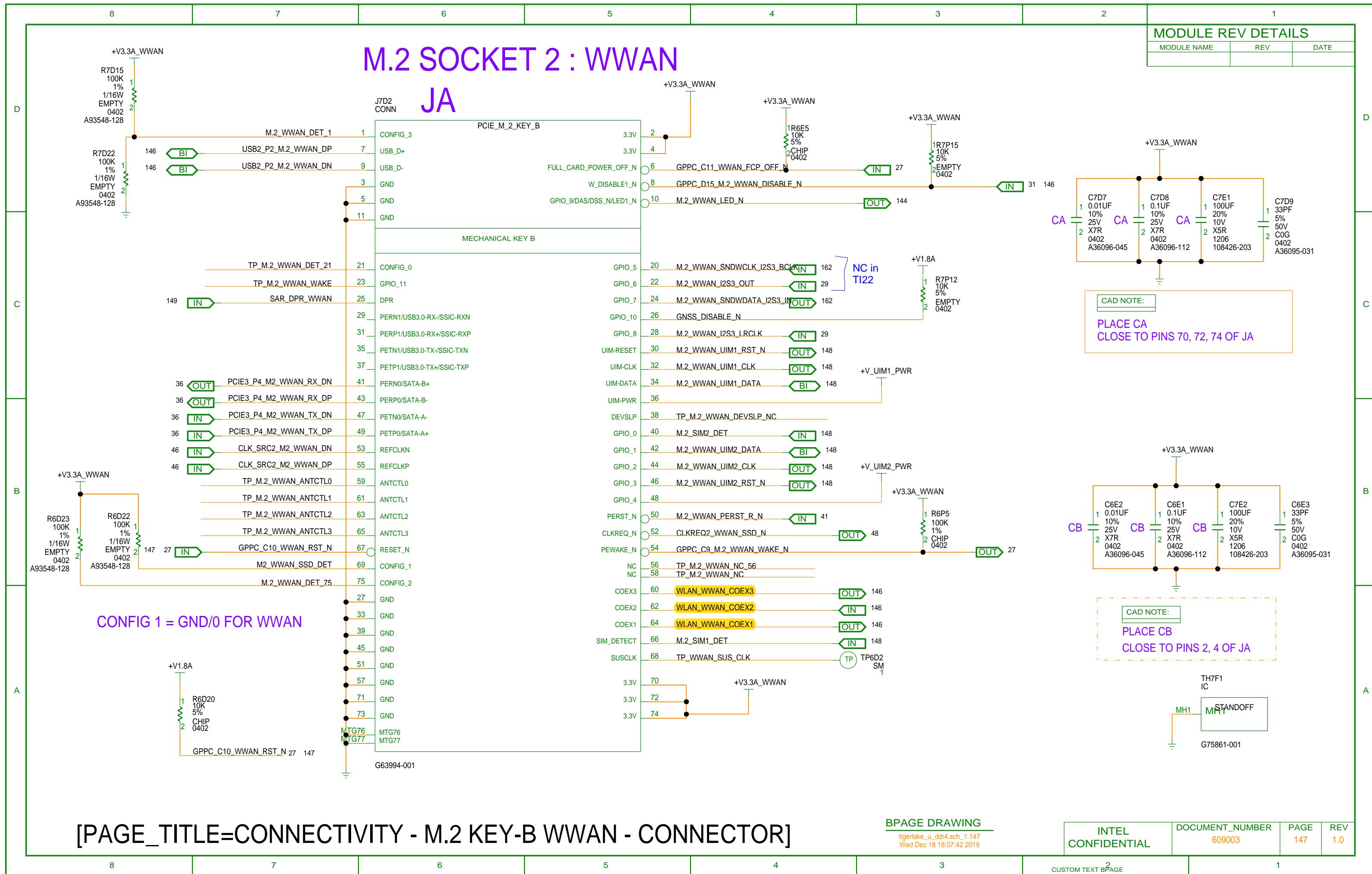
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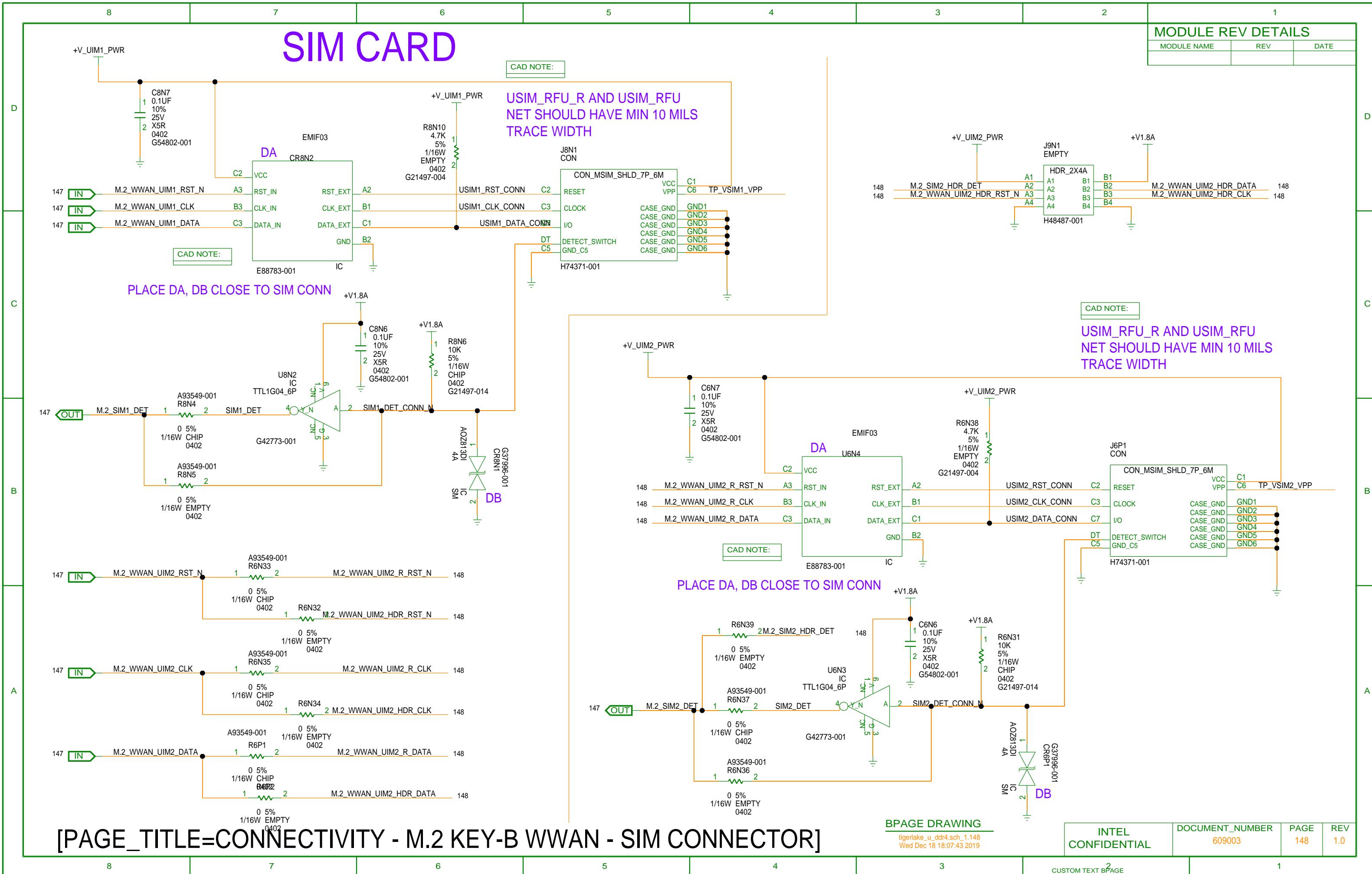
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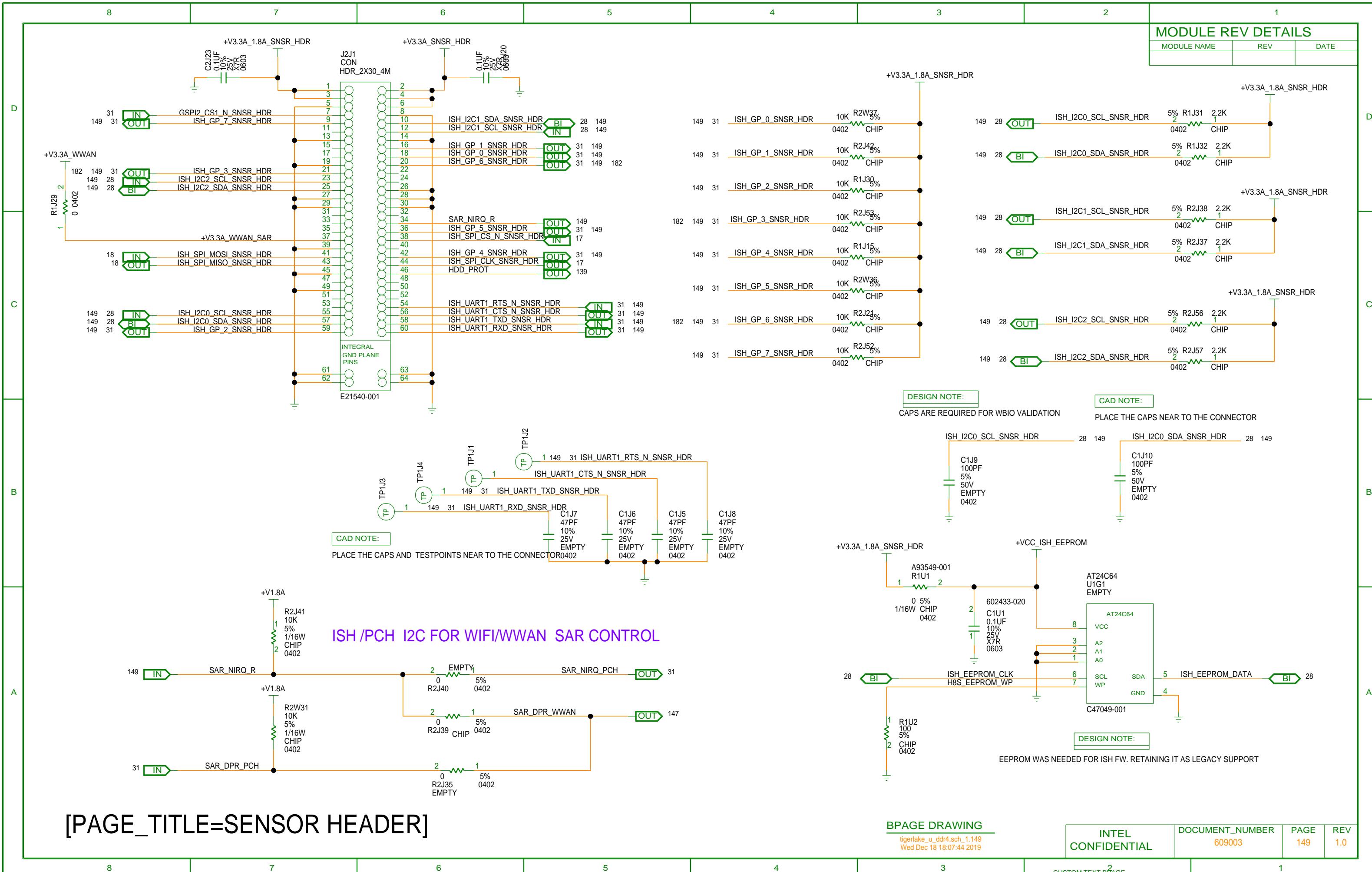






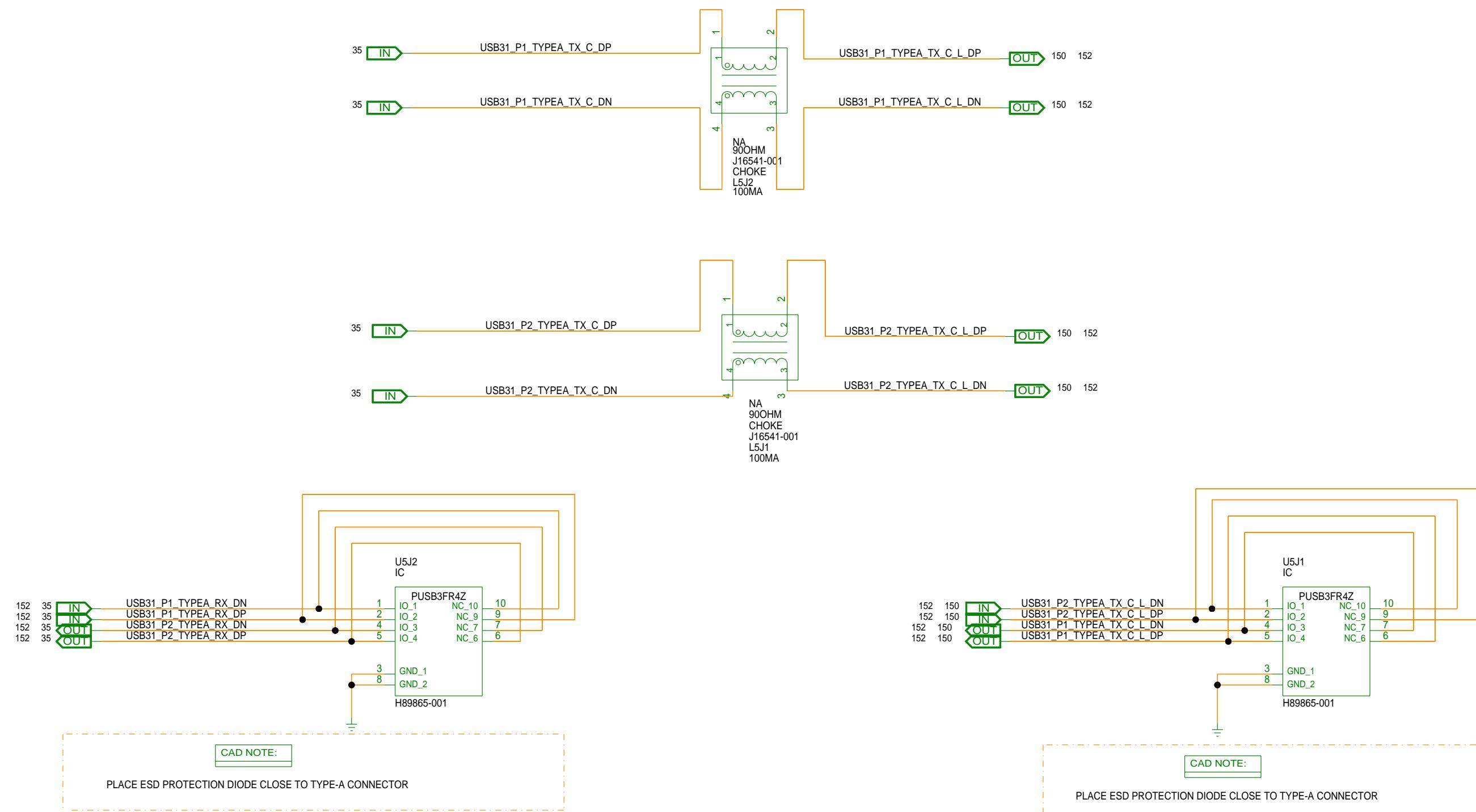


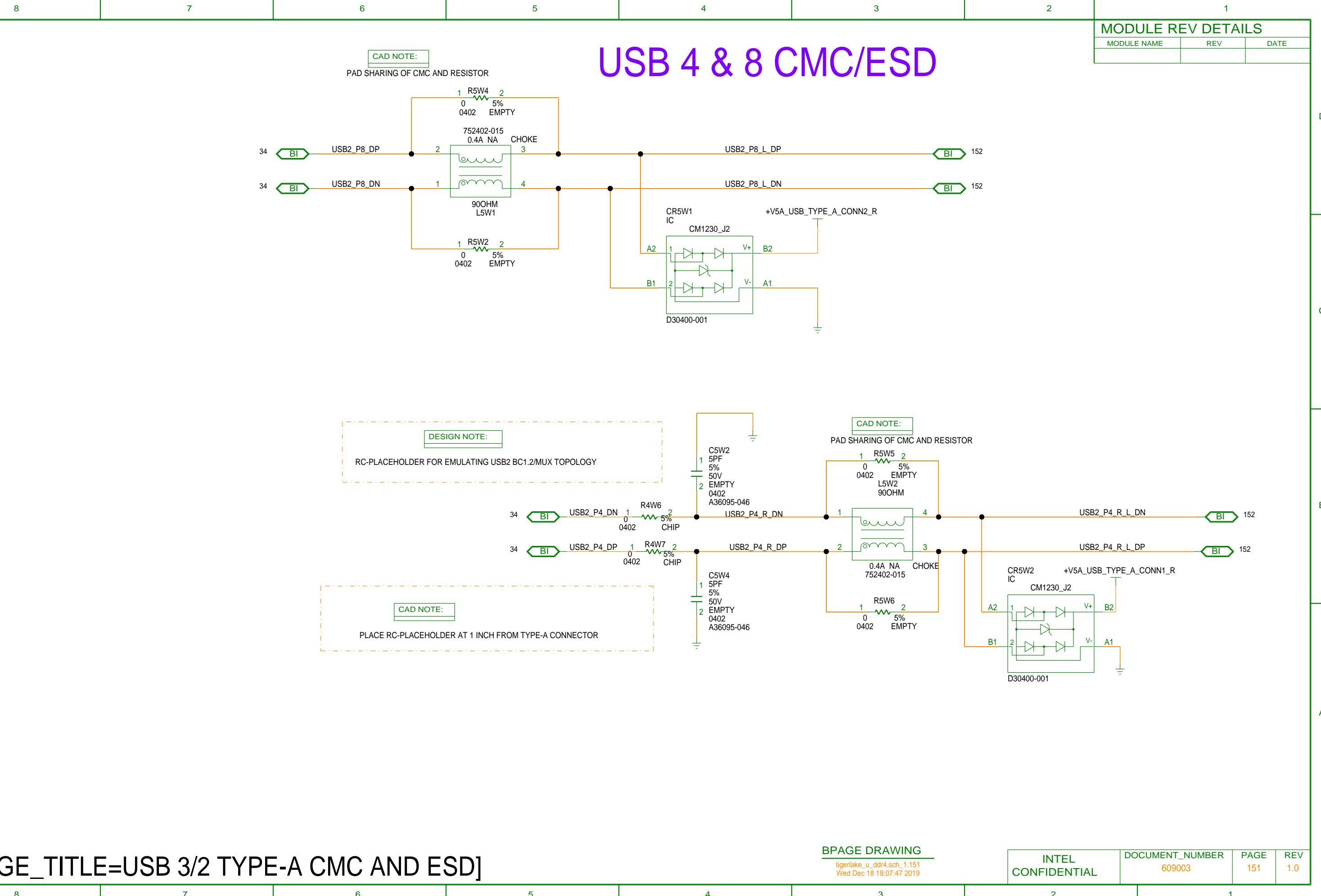


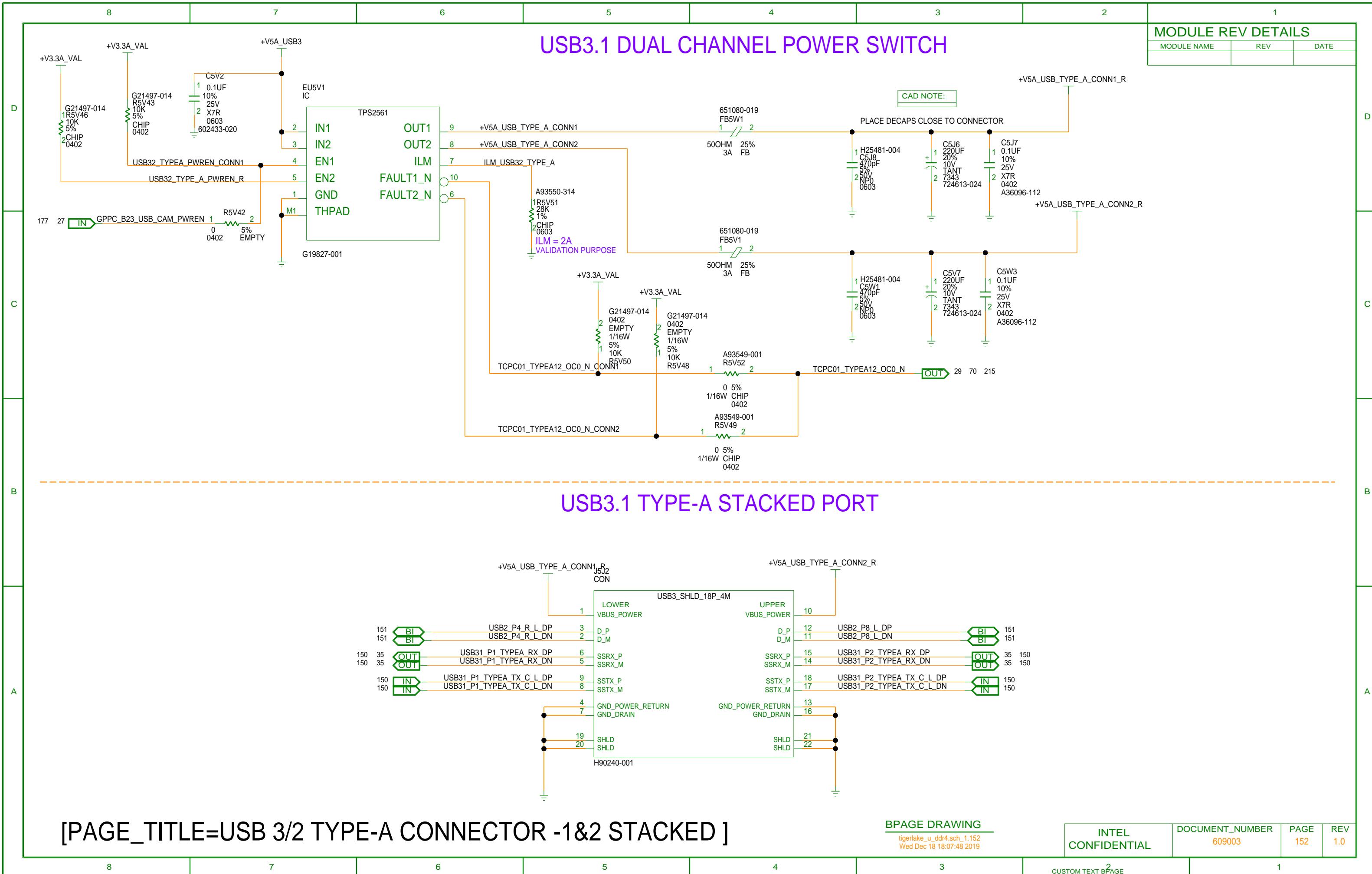


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USB3.1 CMC/ESD







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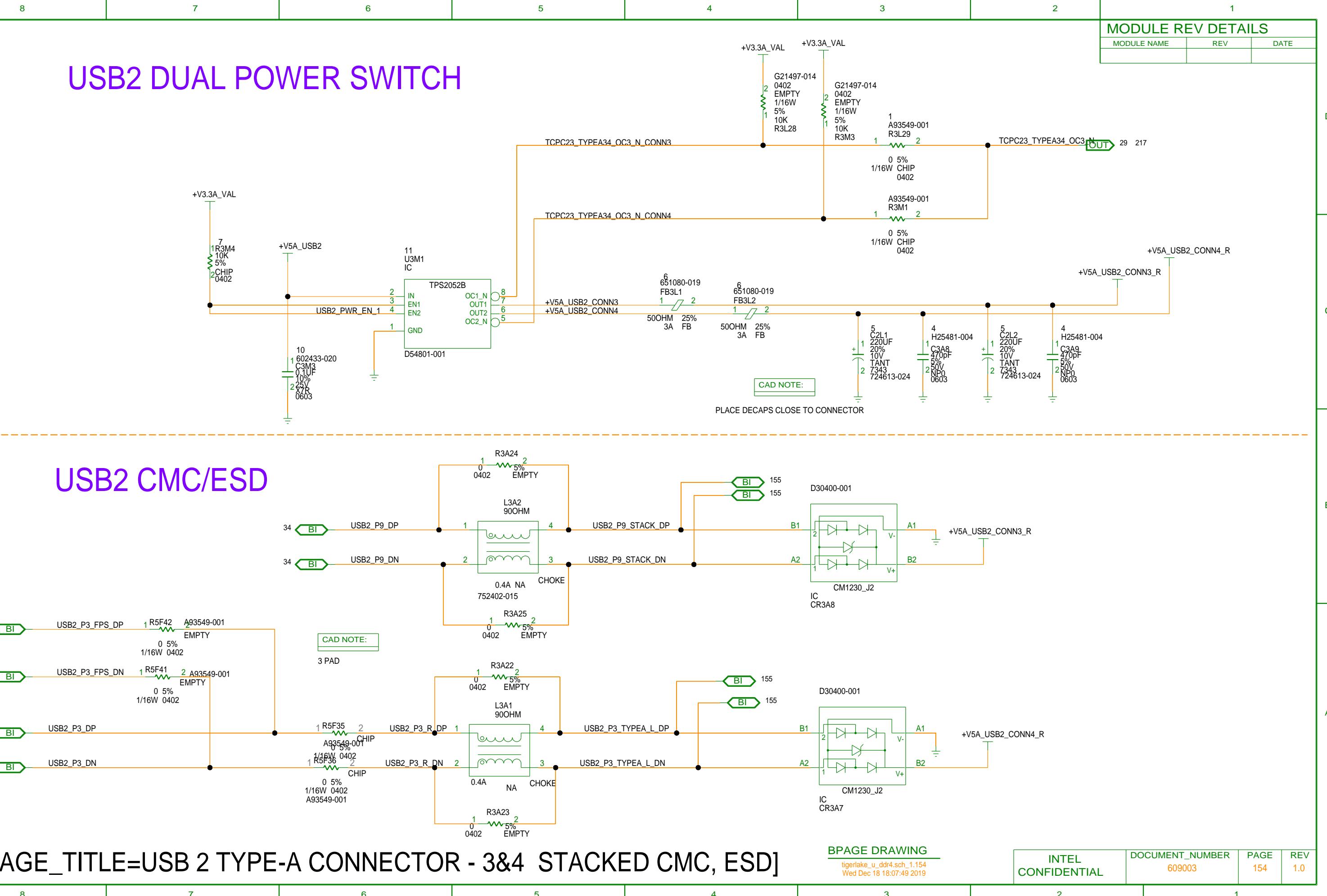
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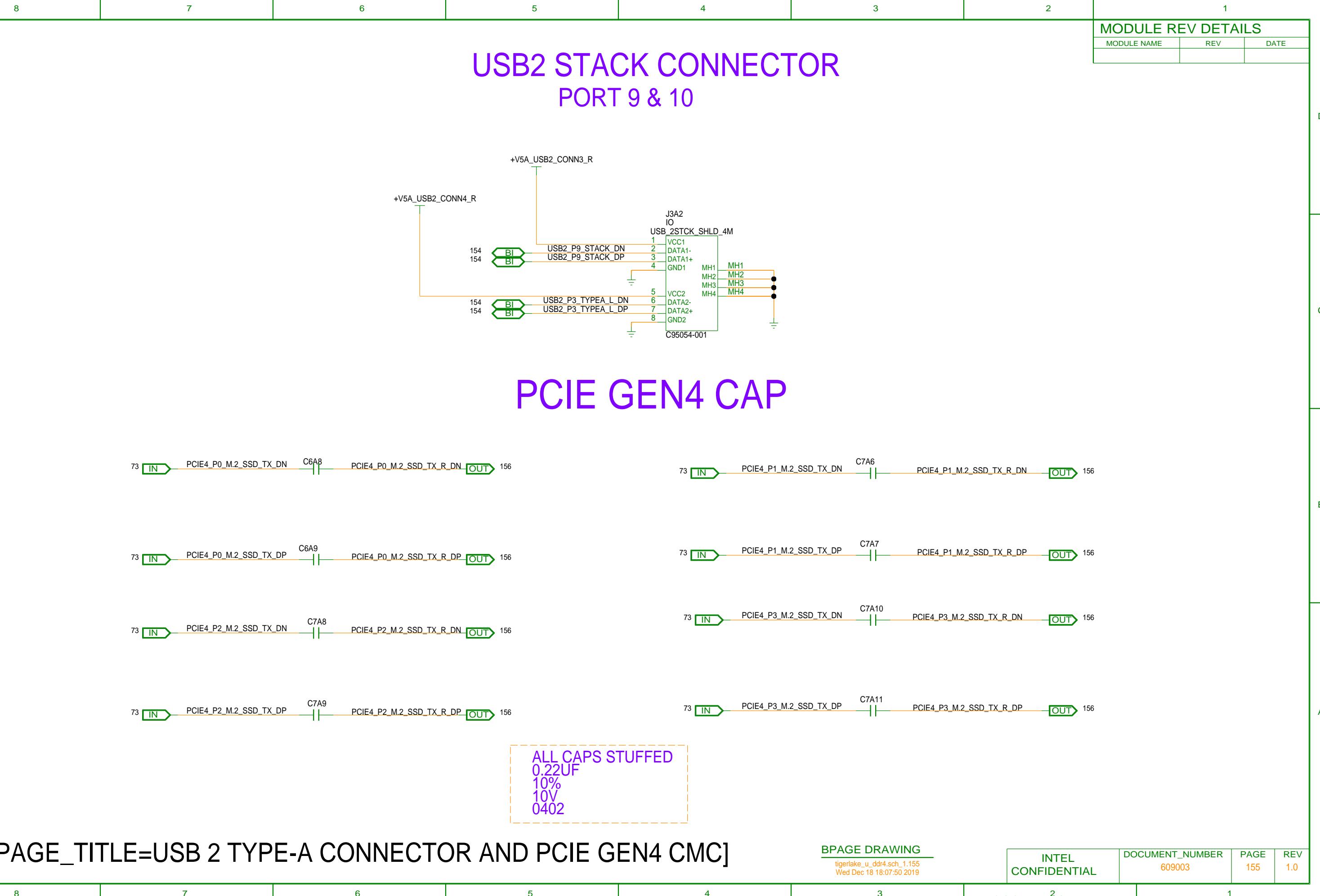
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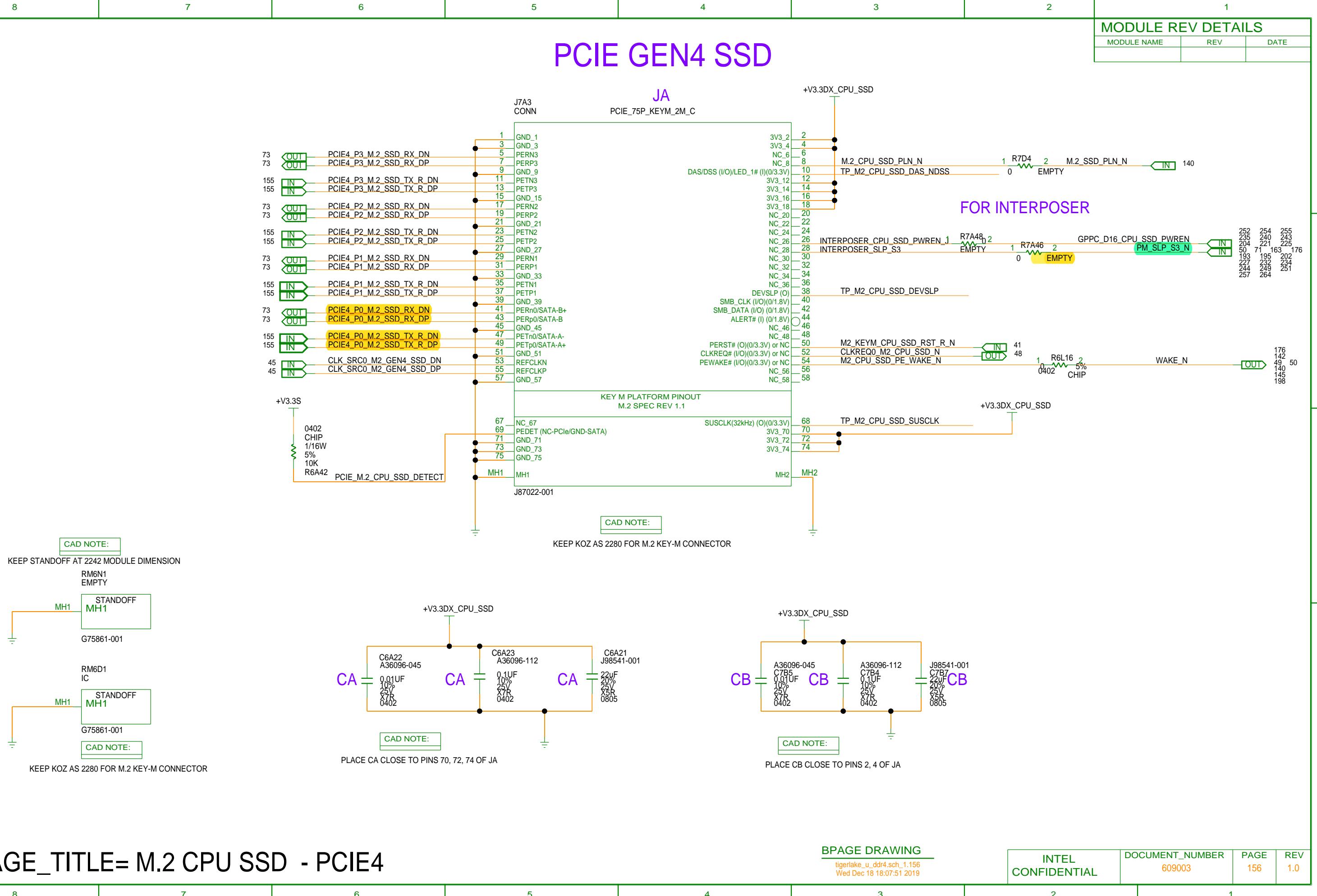
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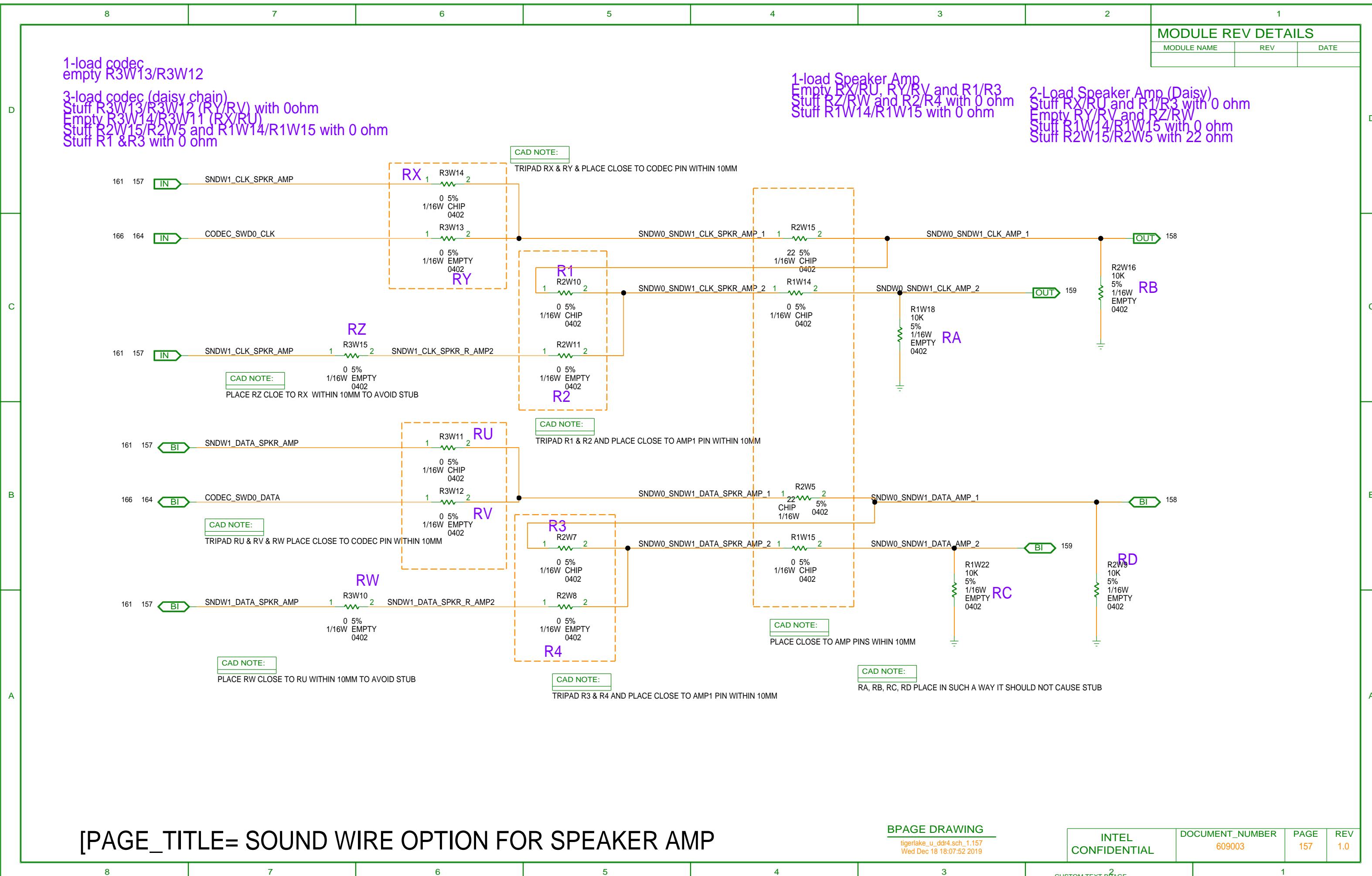
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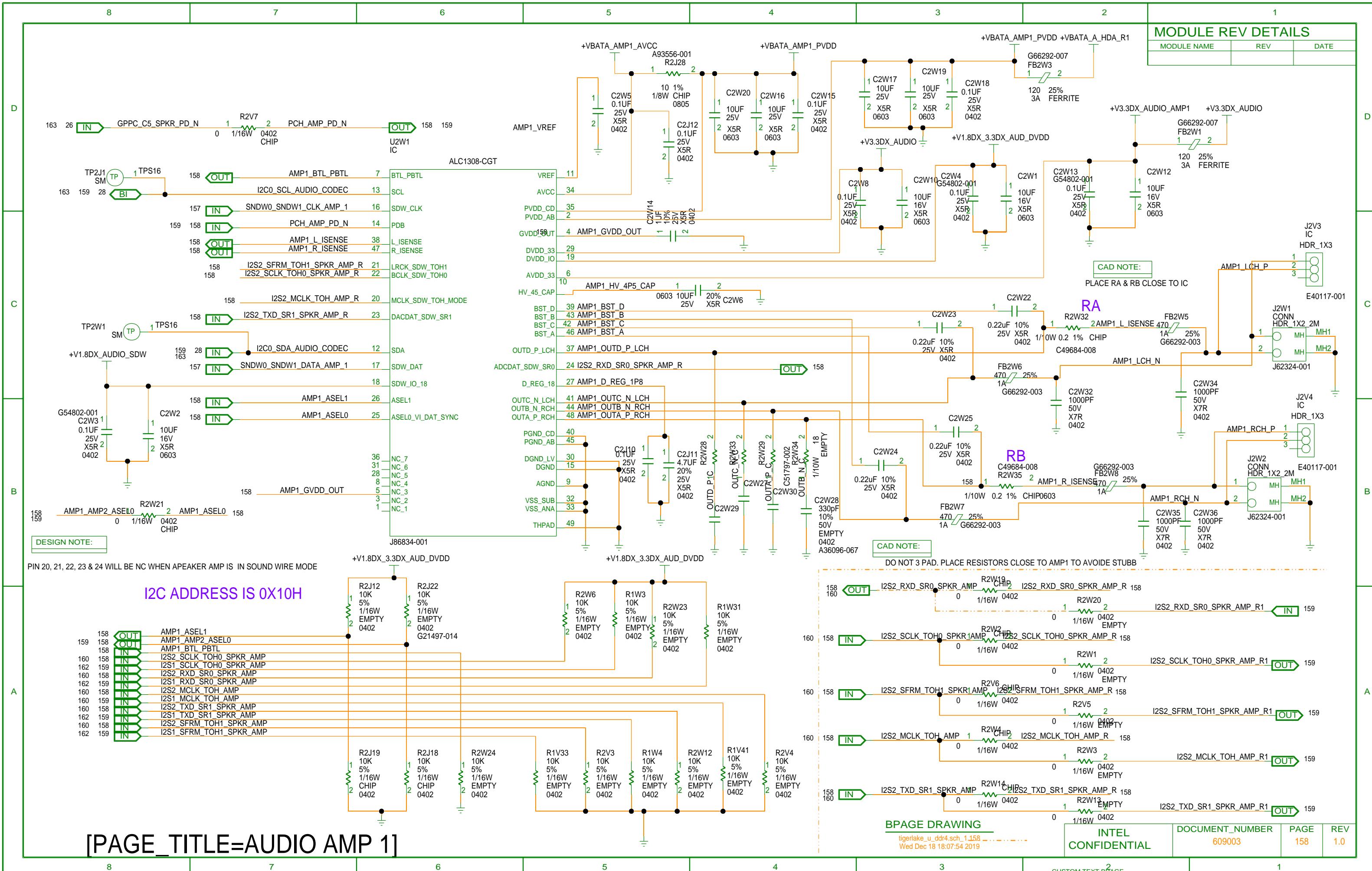
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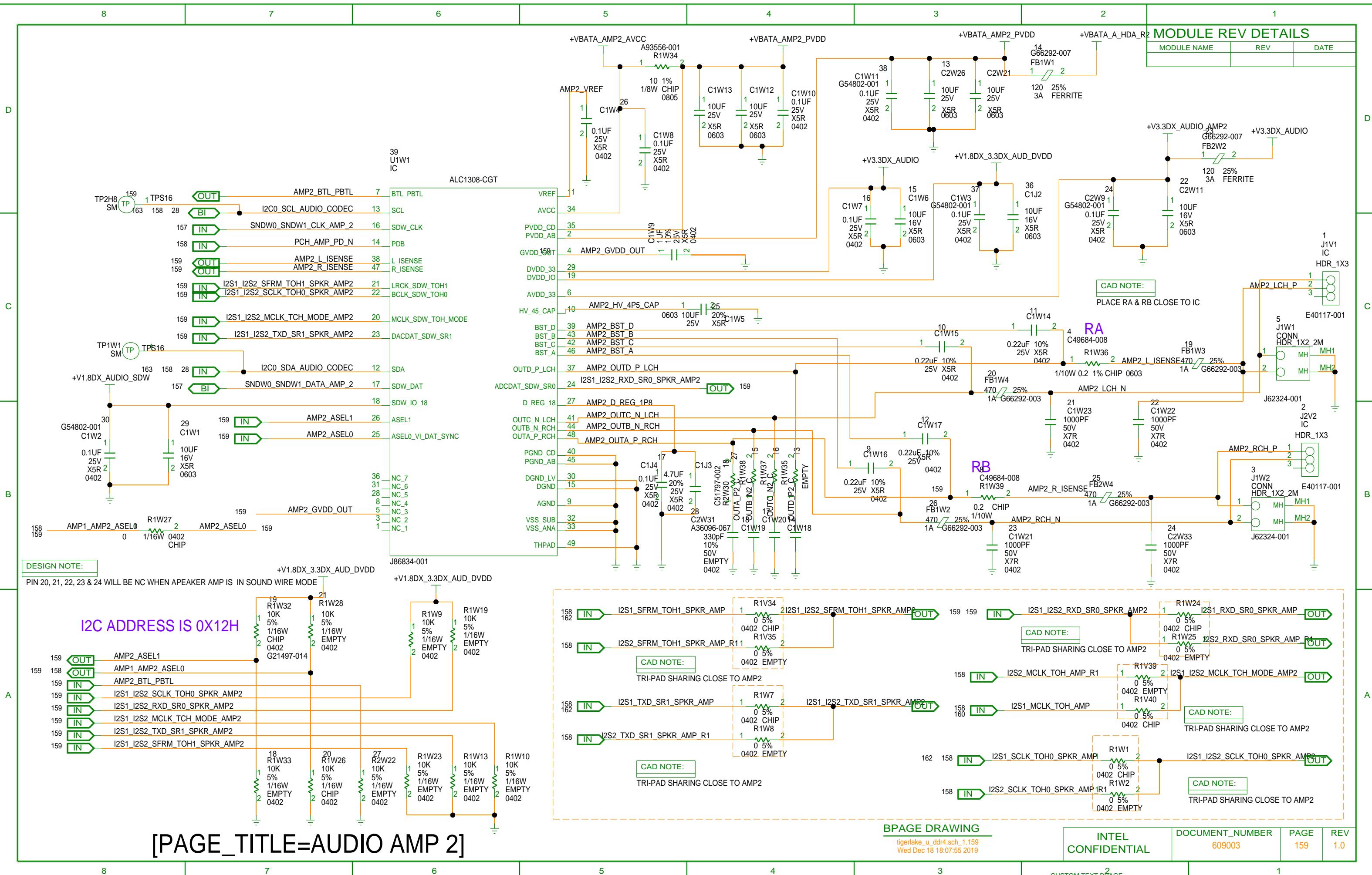


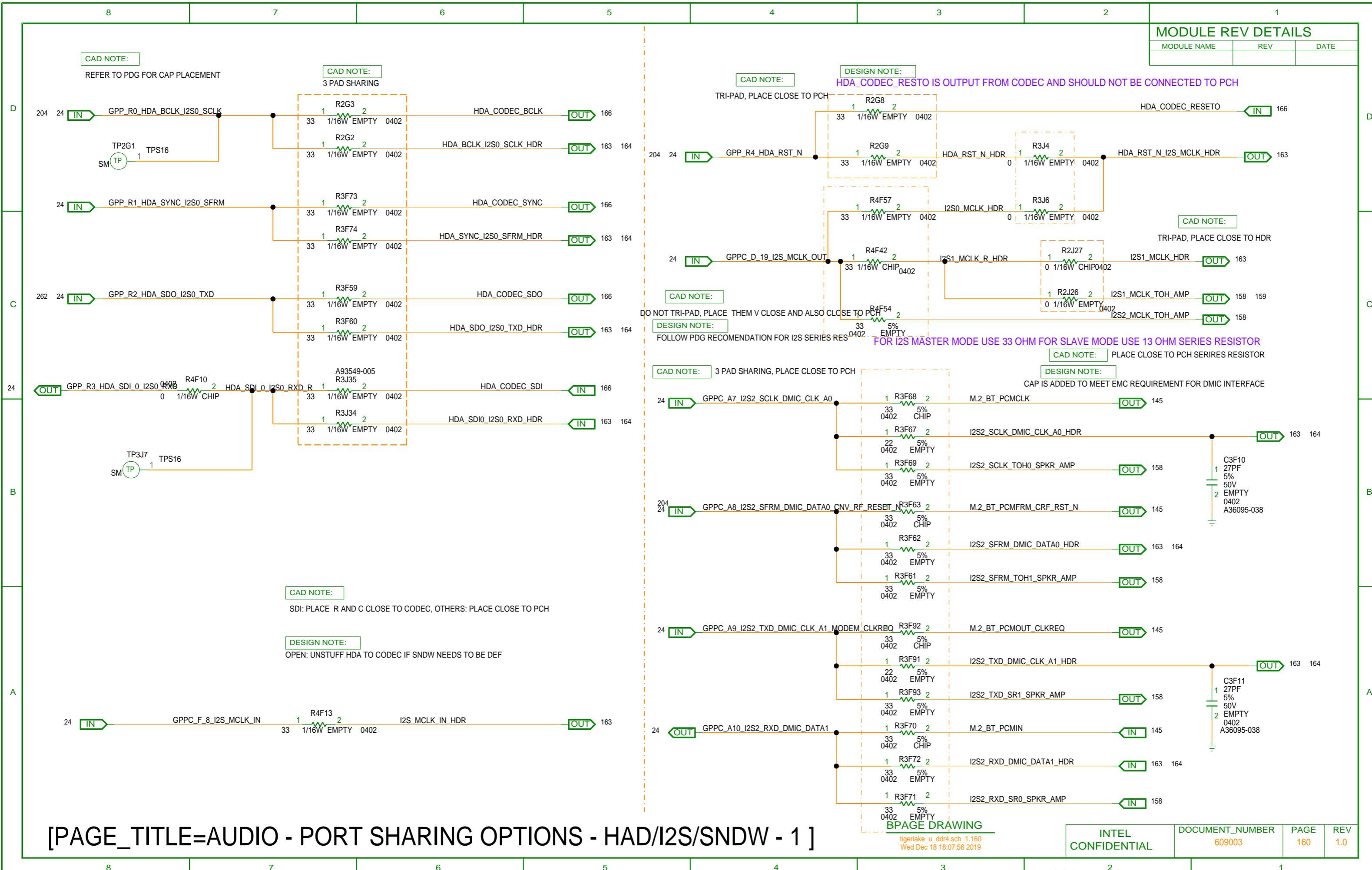


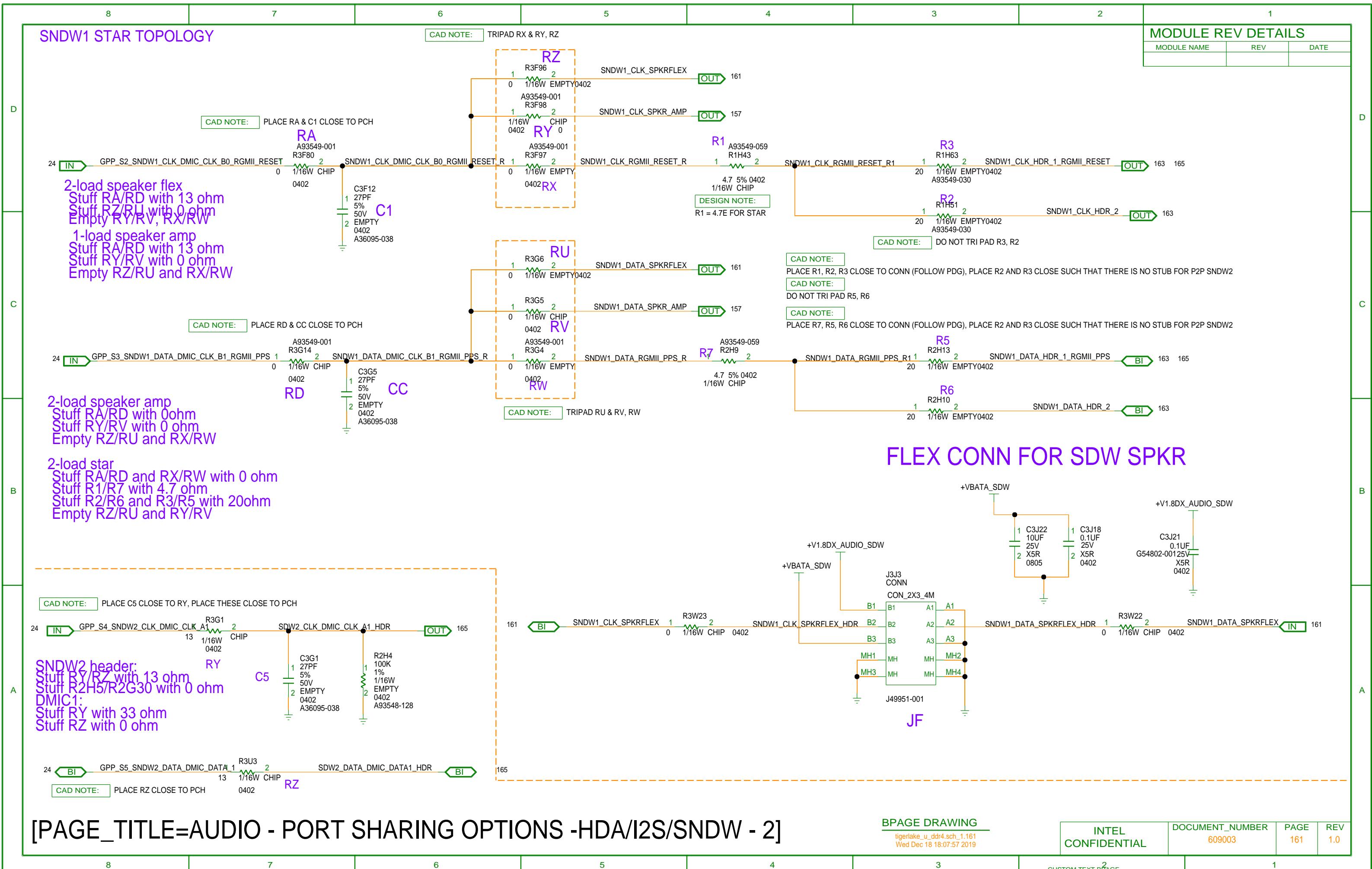


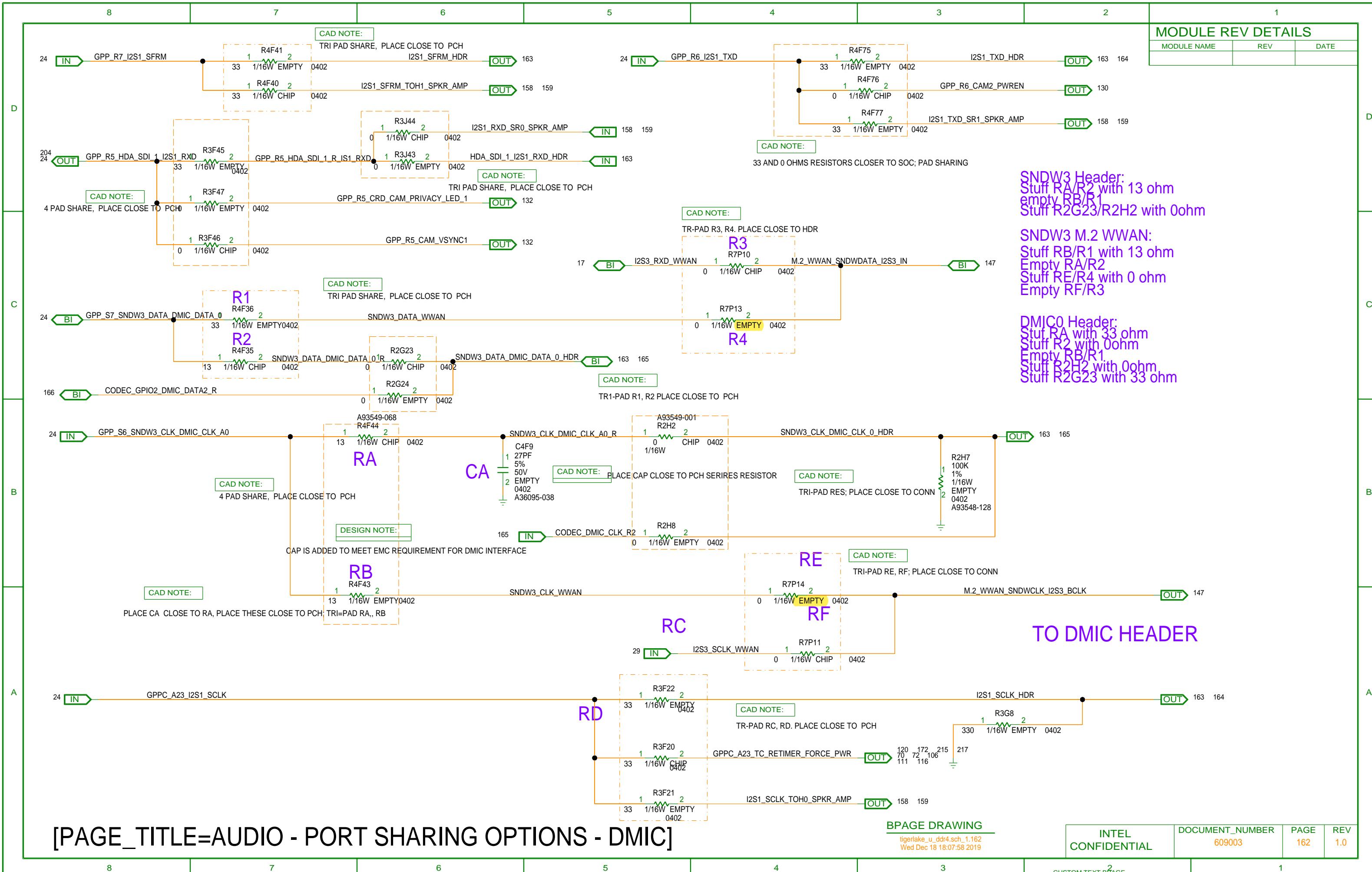


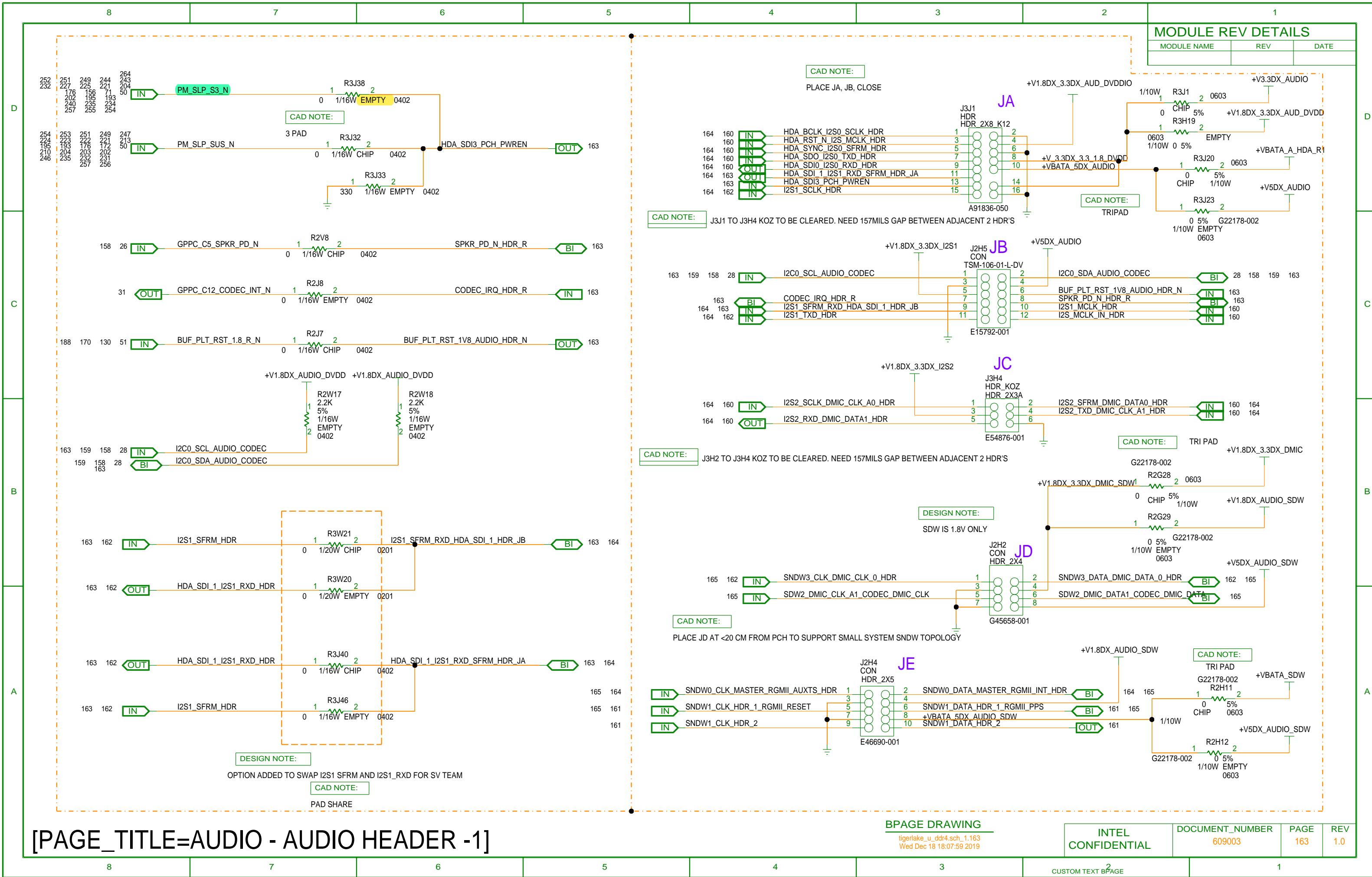








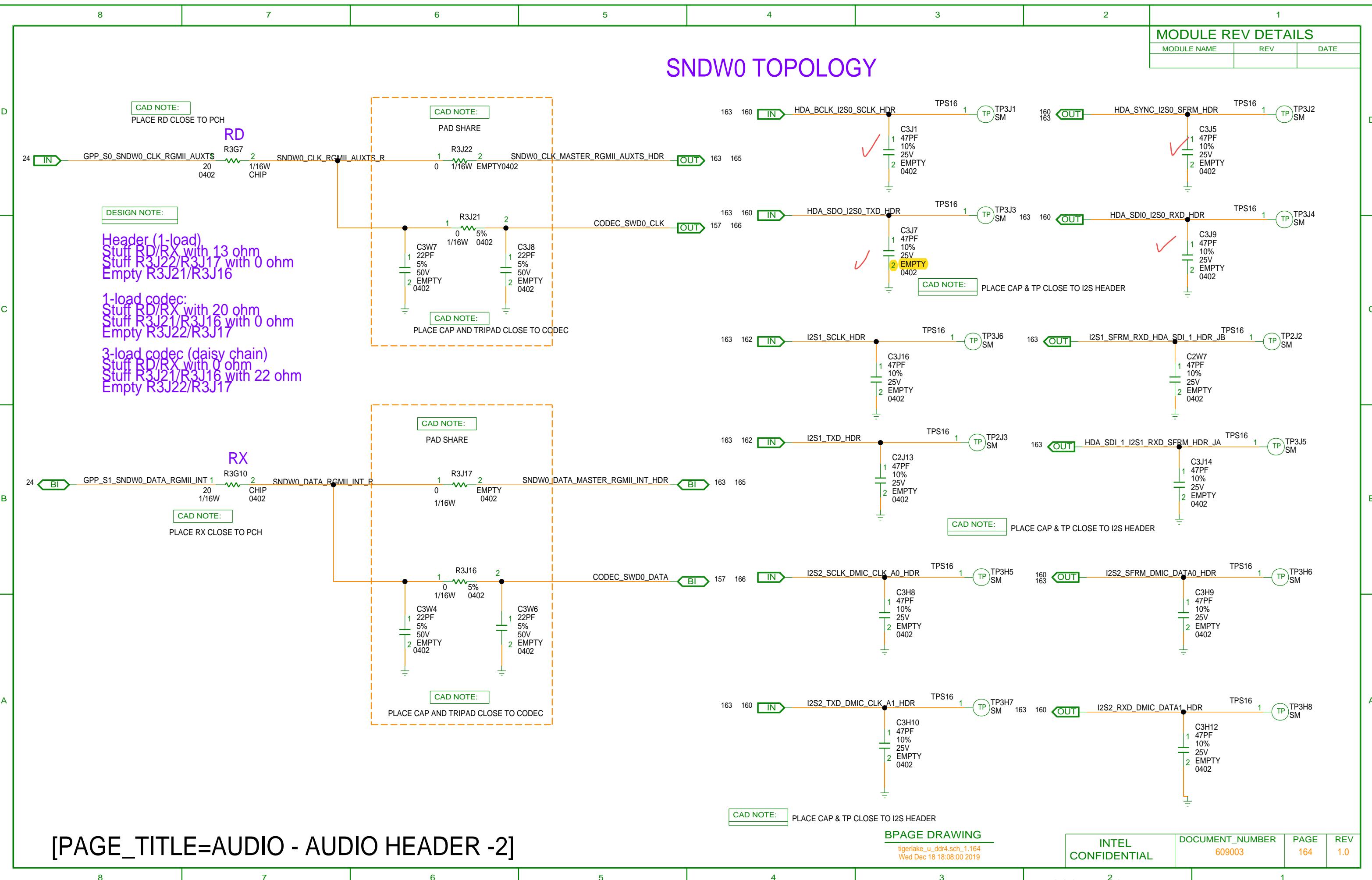


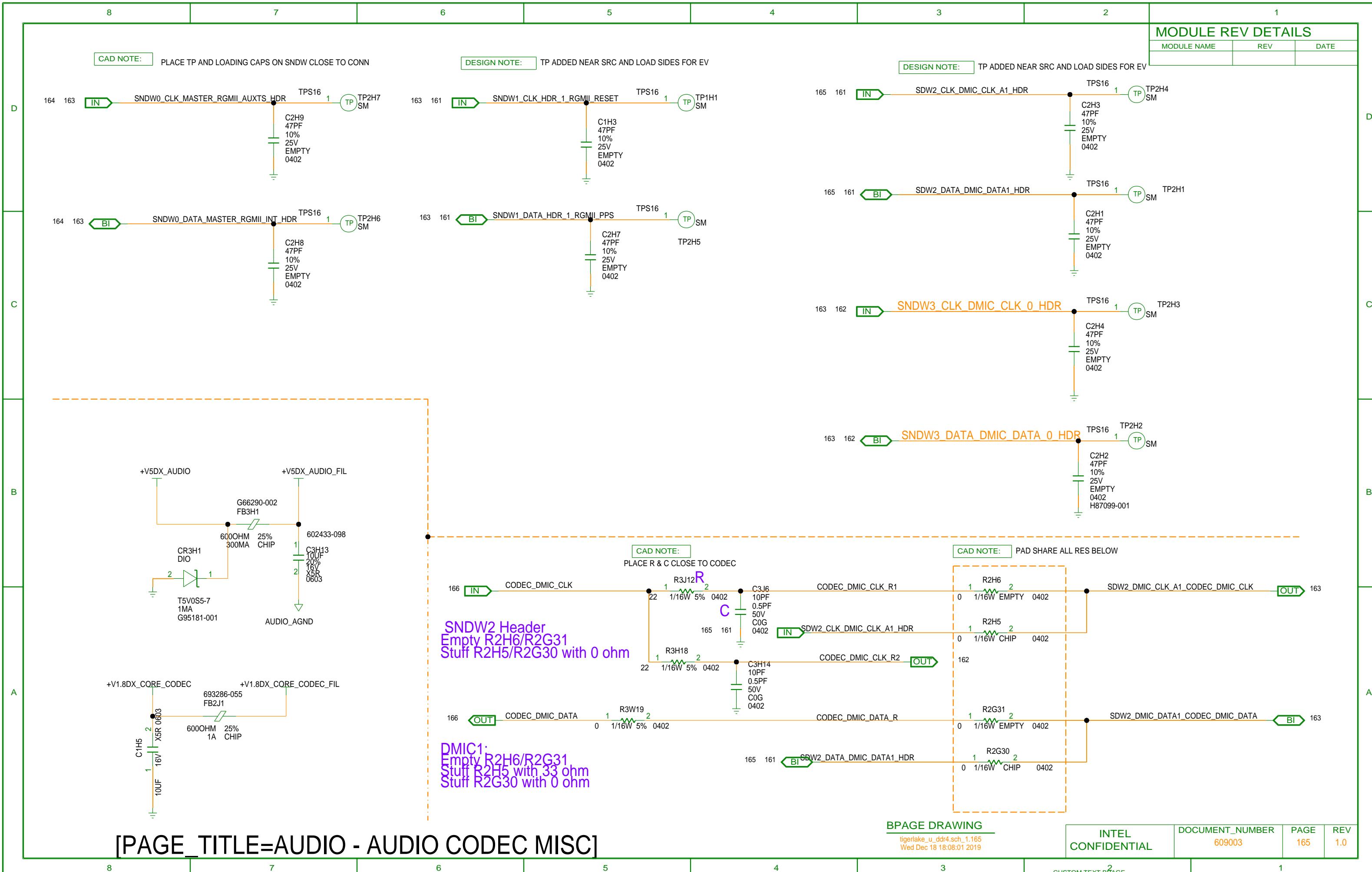


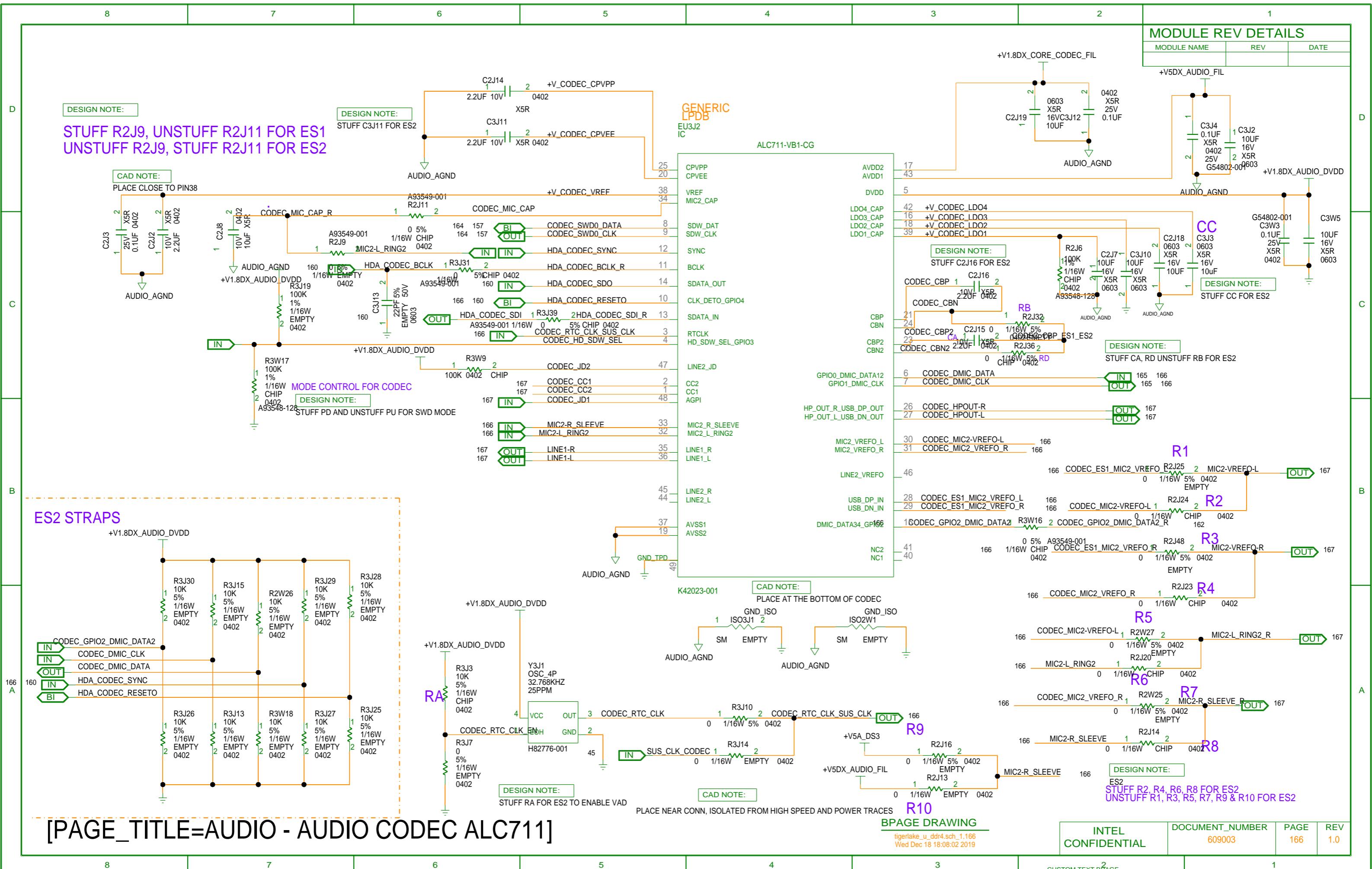
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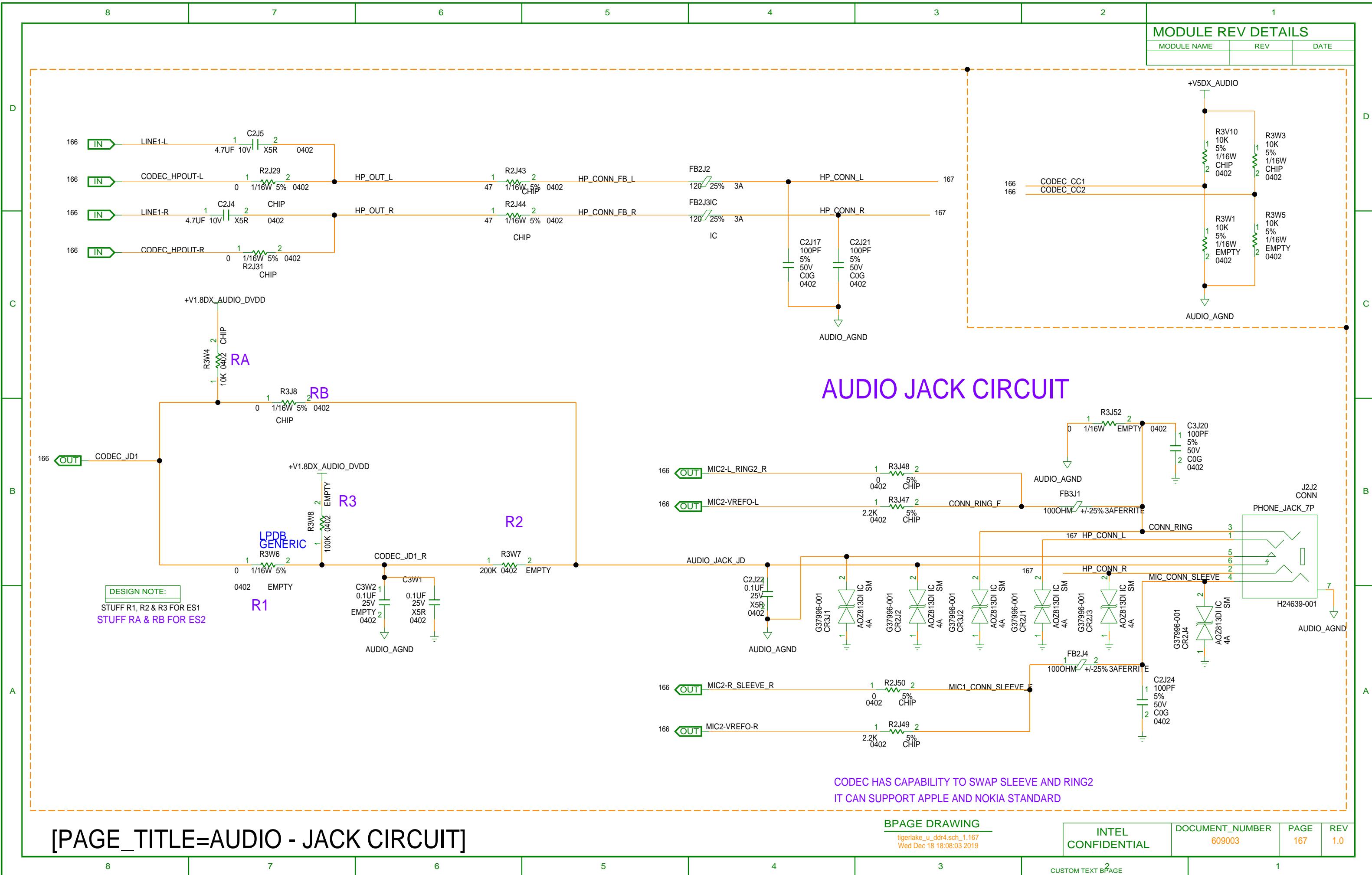
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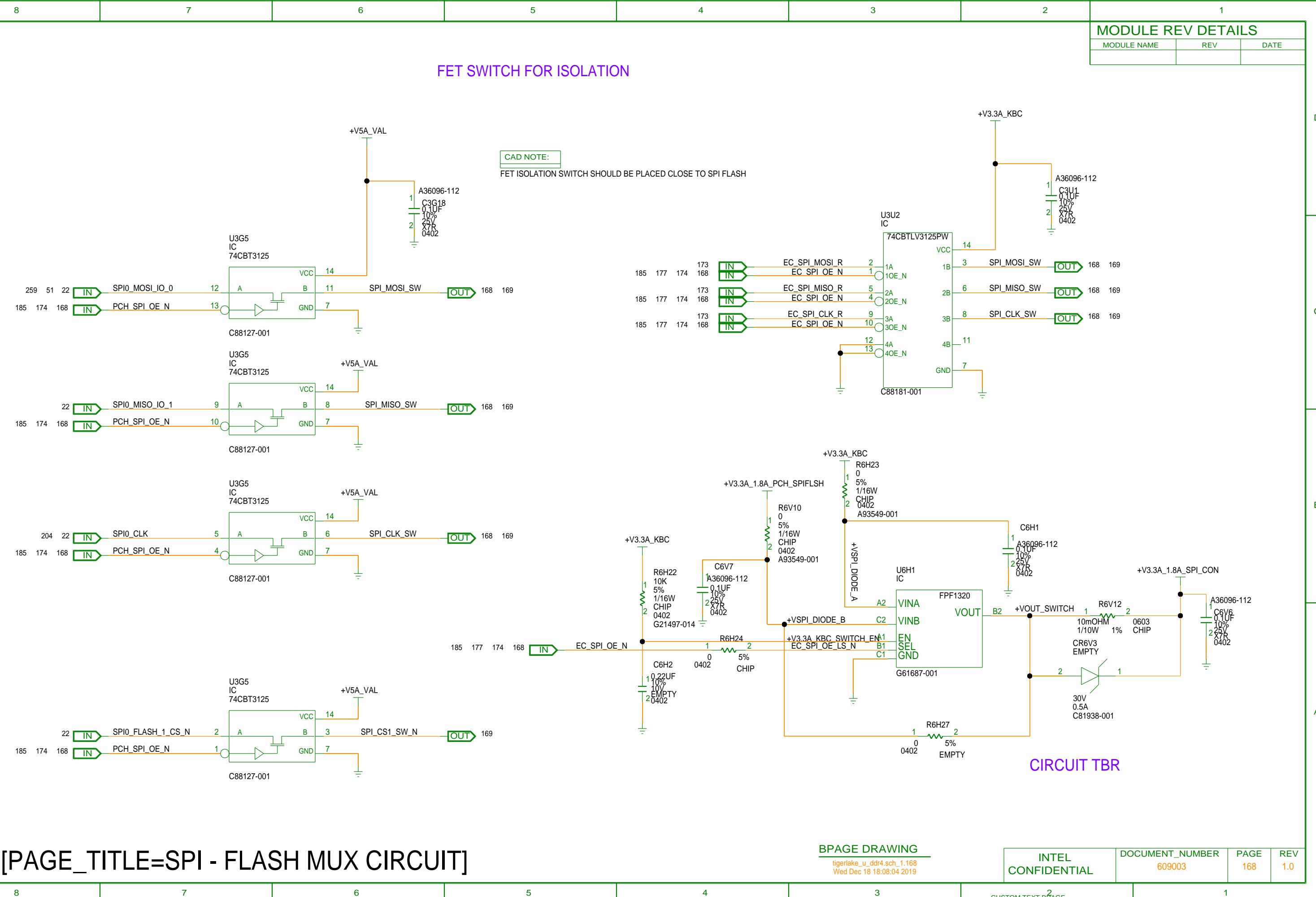
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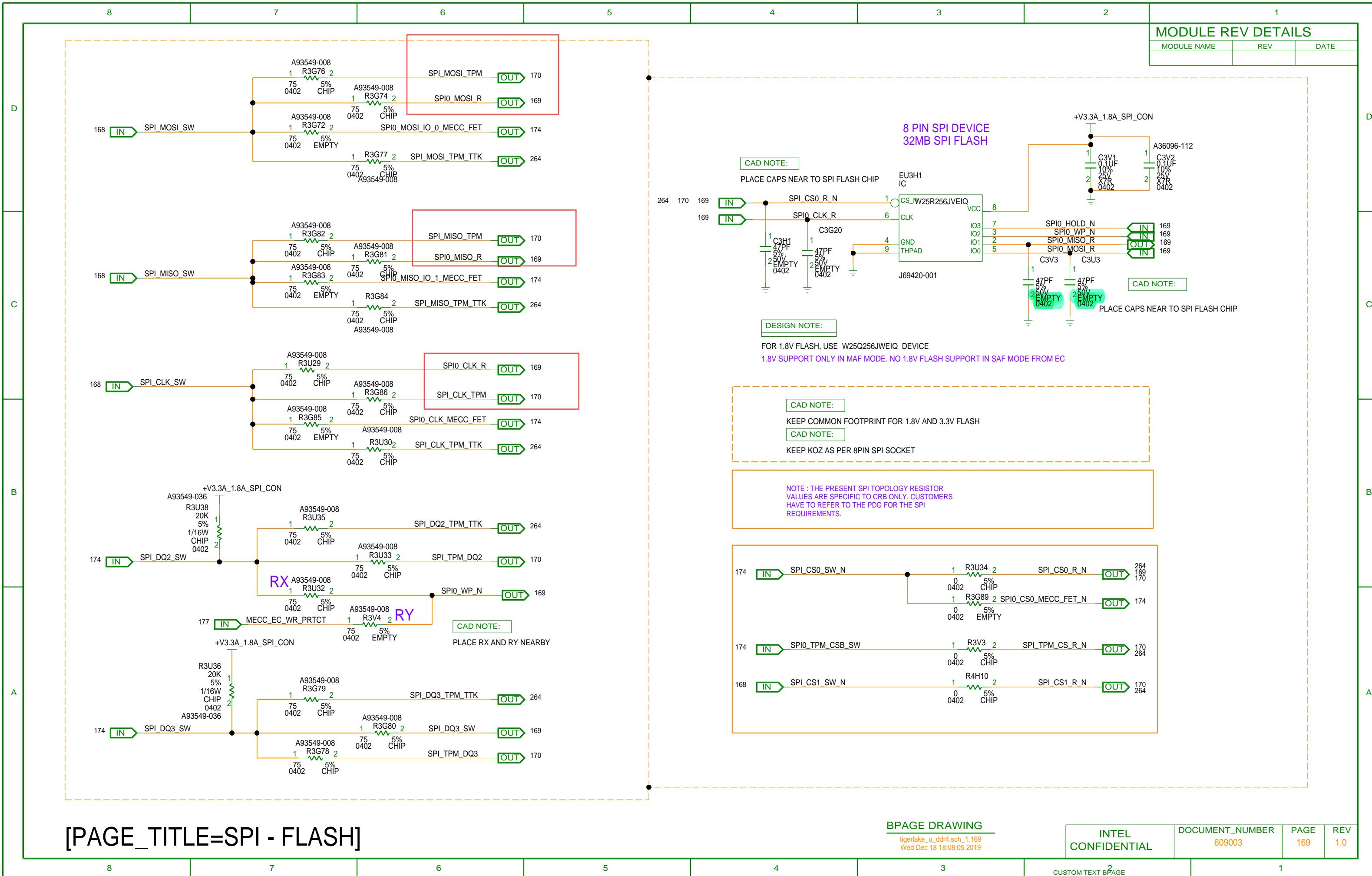












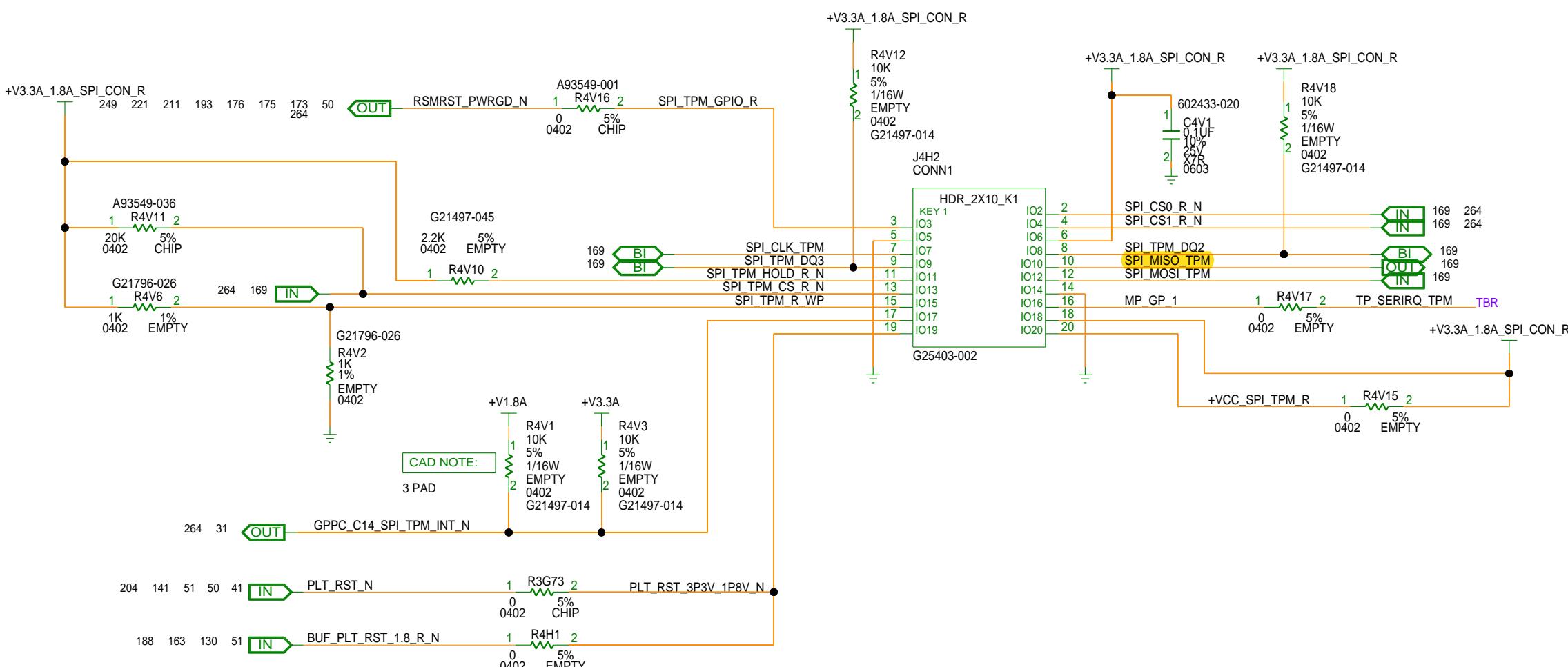
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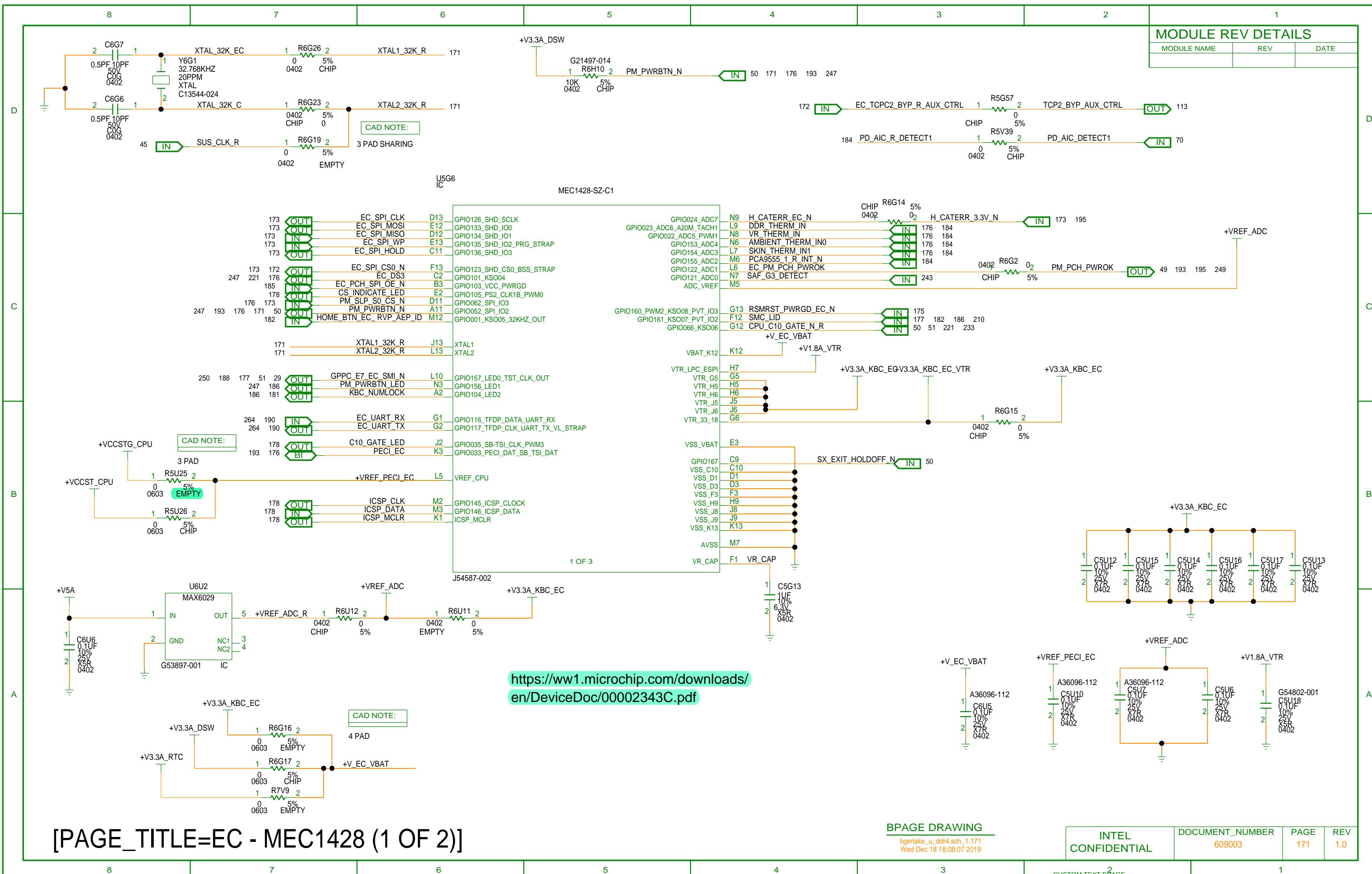
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MODULE NAME	REV	DATE

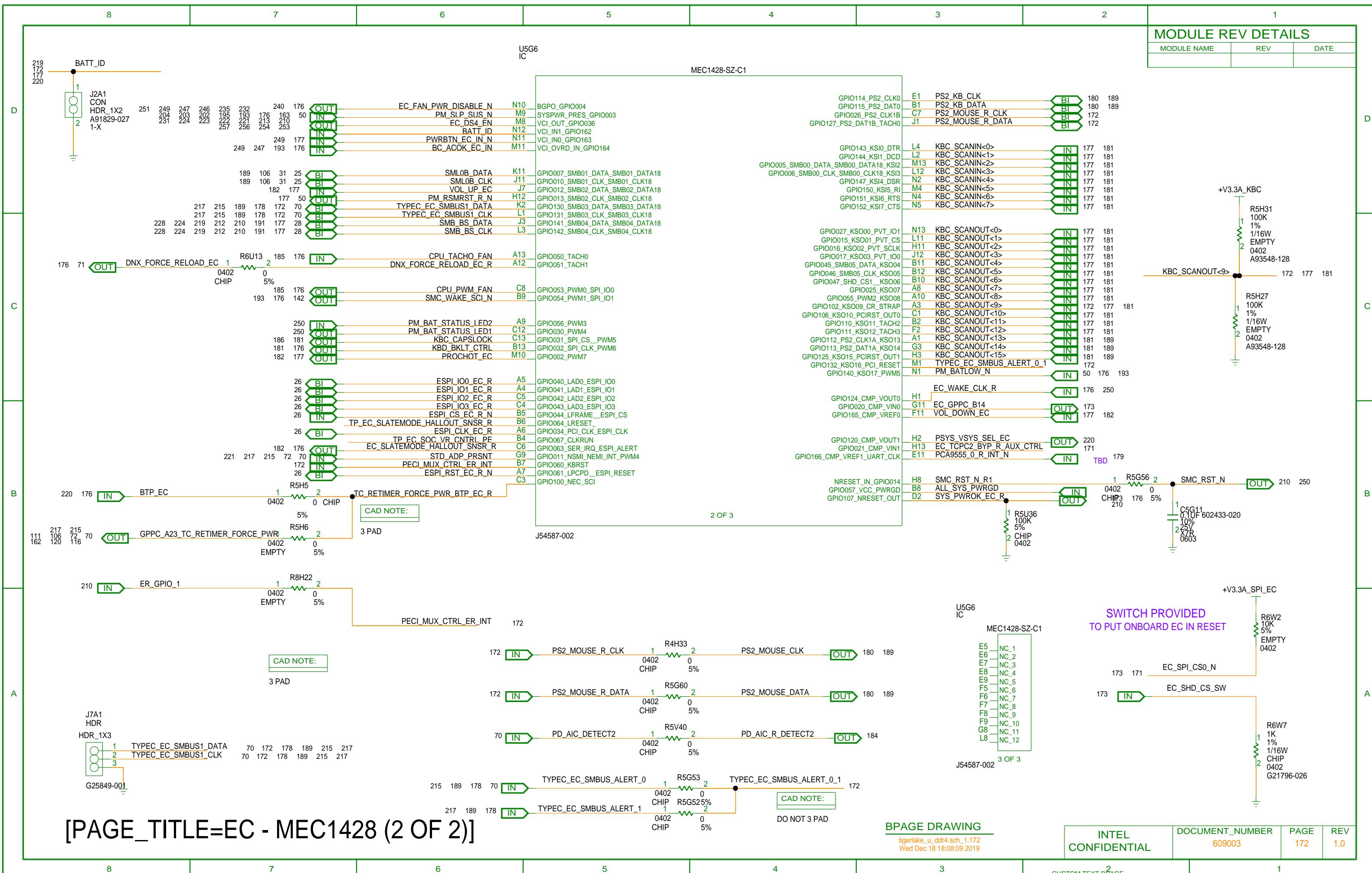
SF600 BASED SPI BASED TPM HEADER

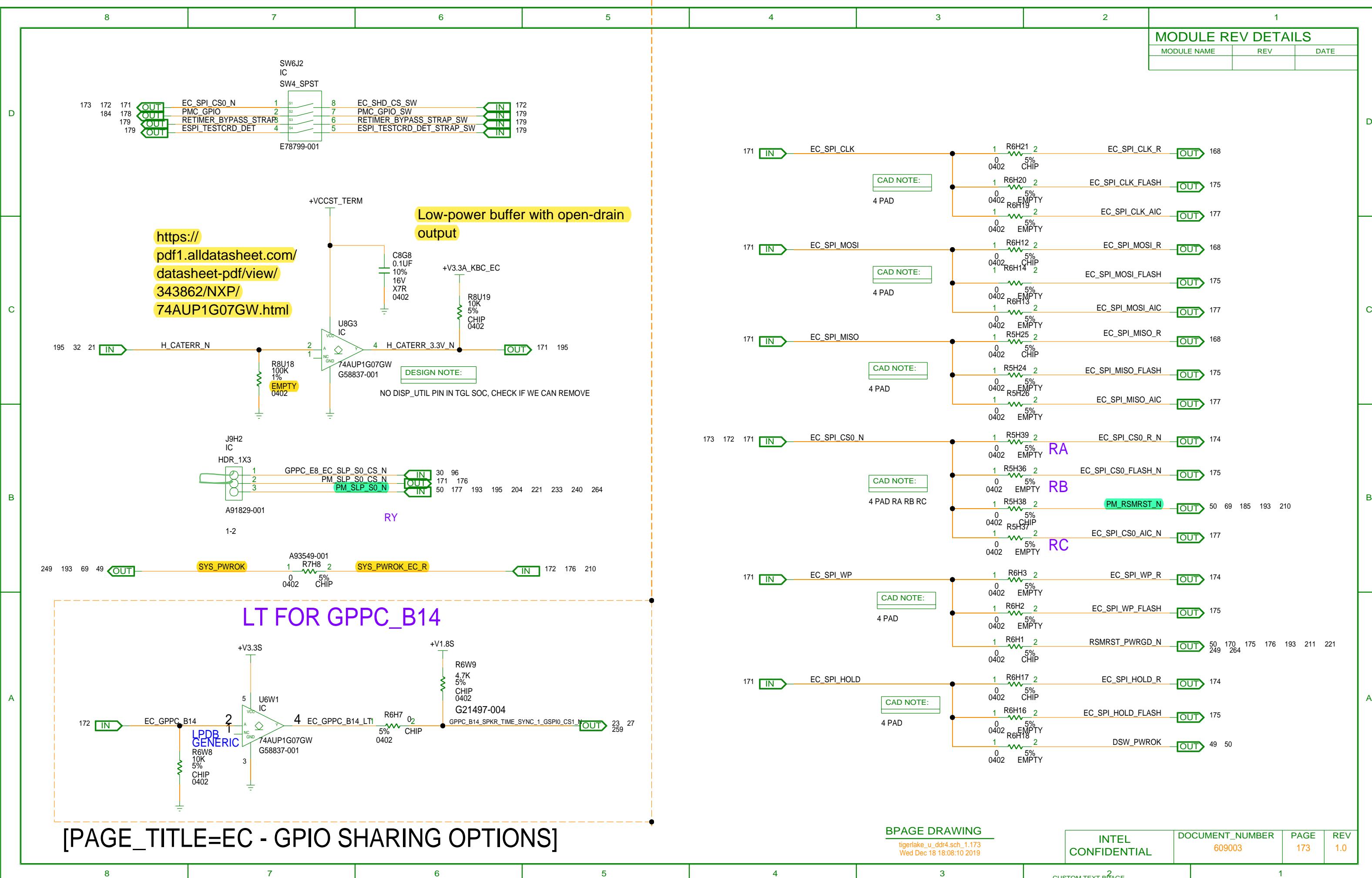
CAD NOTE:

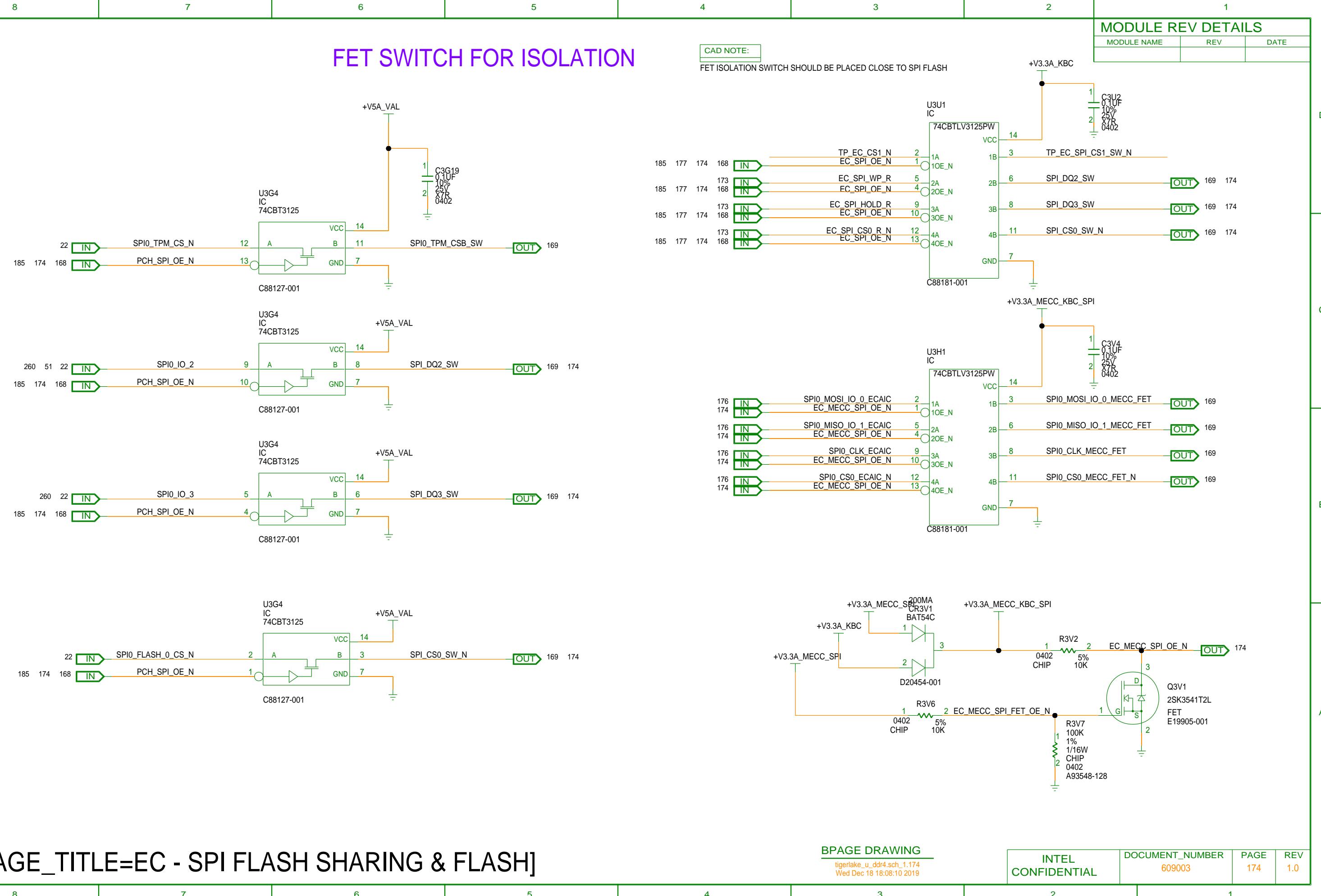
SPI0_FLASH_1_CS_N SIGNAL TO BE ROUTED 1.5 INCH MORE LENGTH THAN OTHER SPI0 SIGNALS







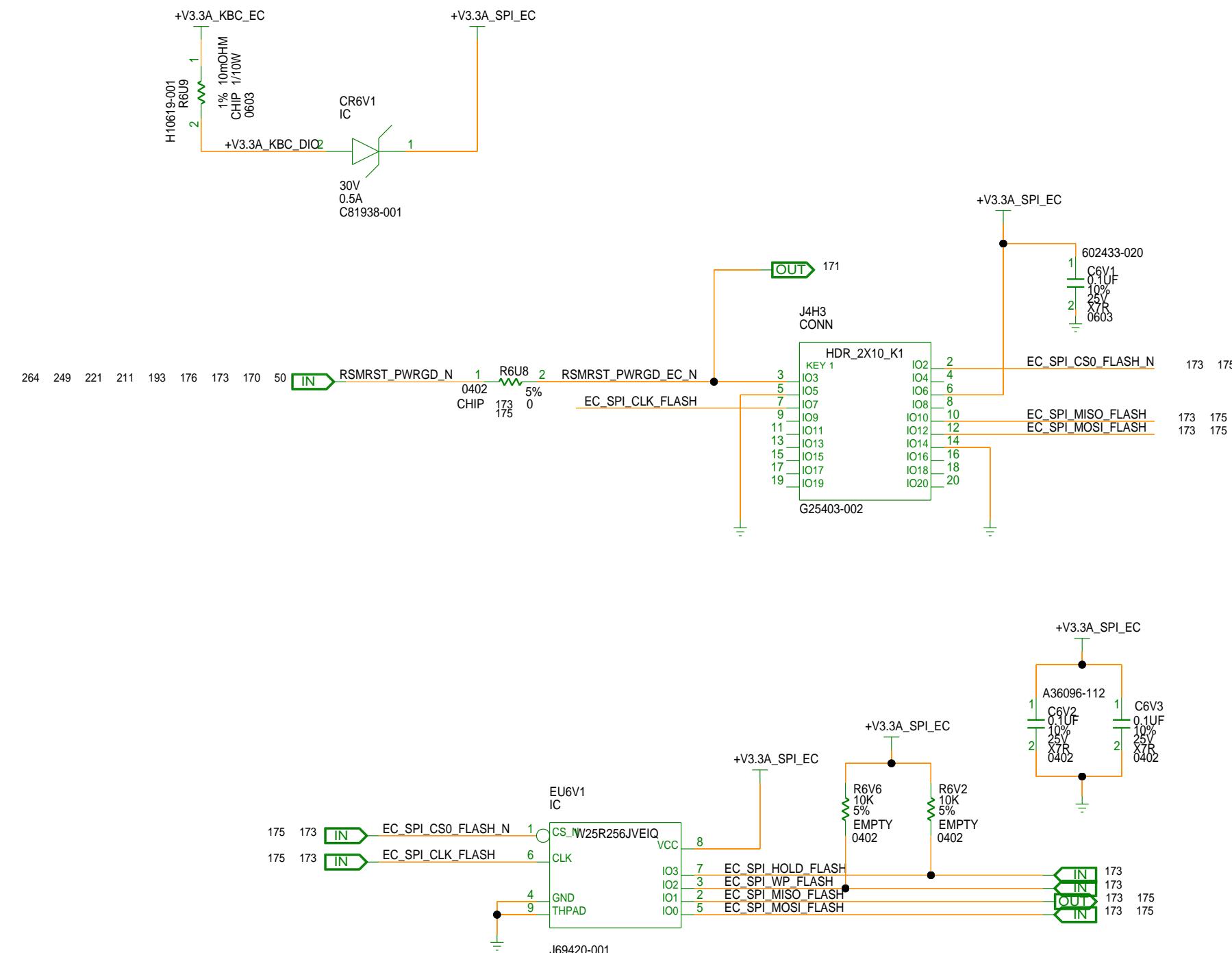




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SF600 BASED TPM HEADER (DEDICATED FOR EC)

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MODULE NAME	REV	DATE

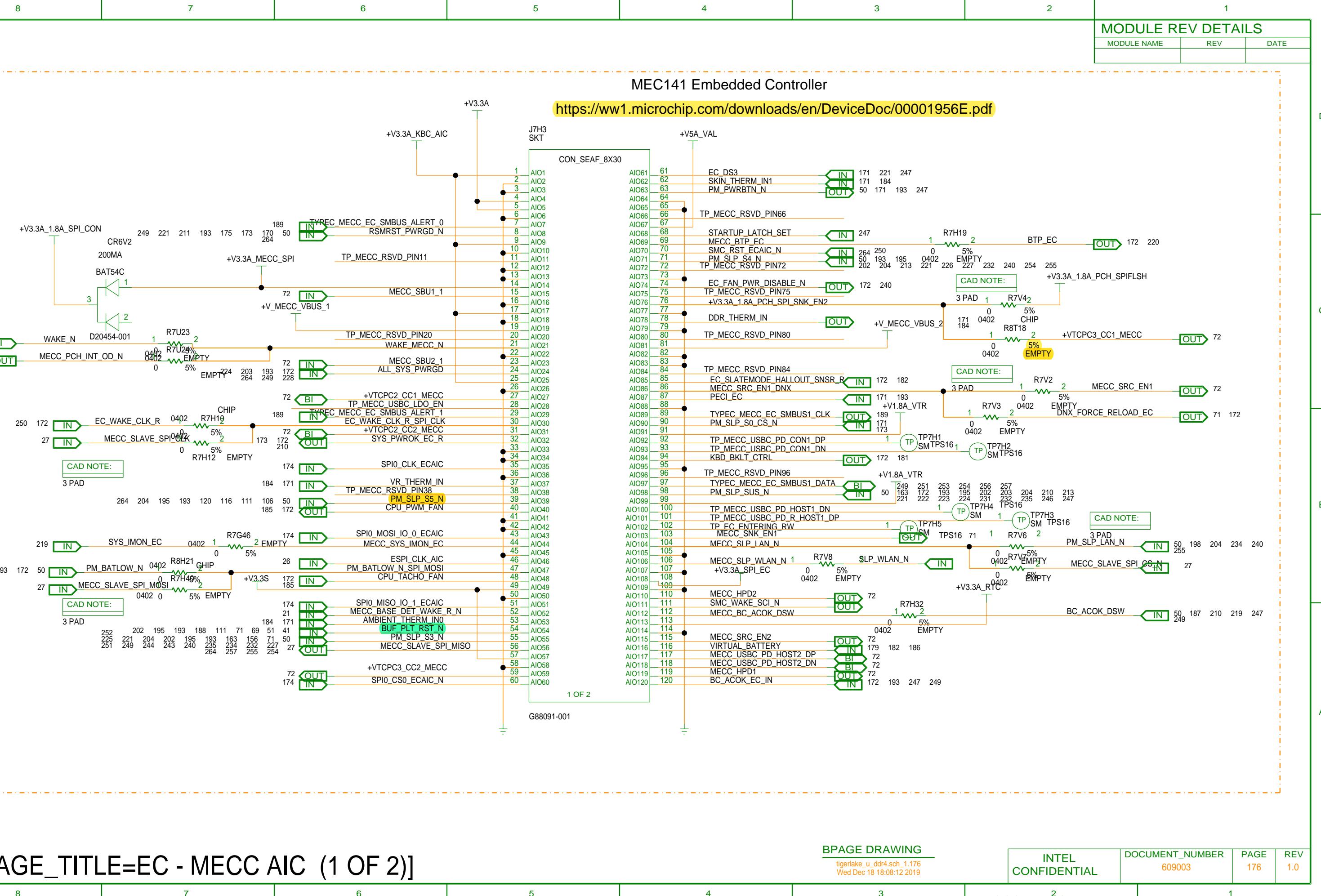


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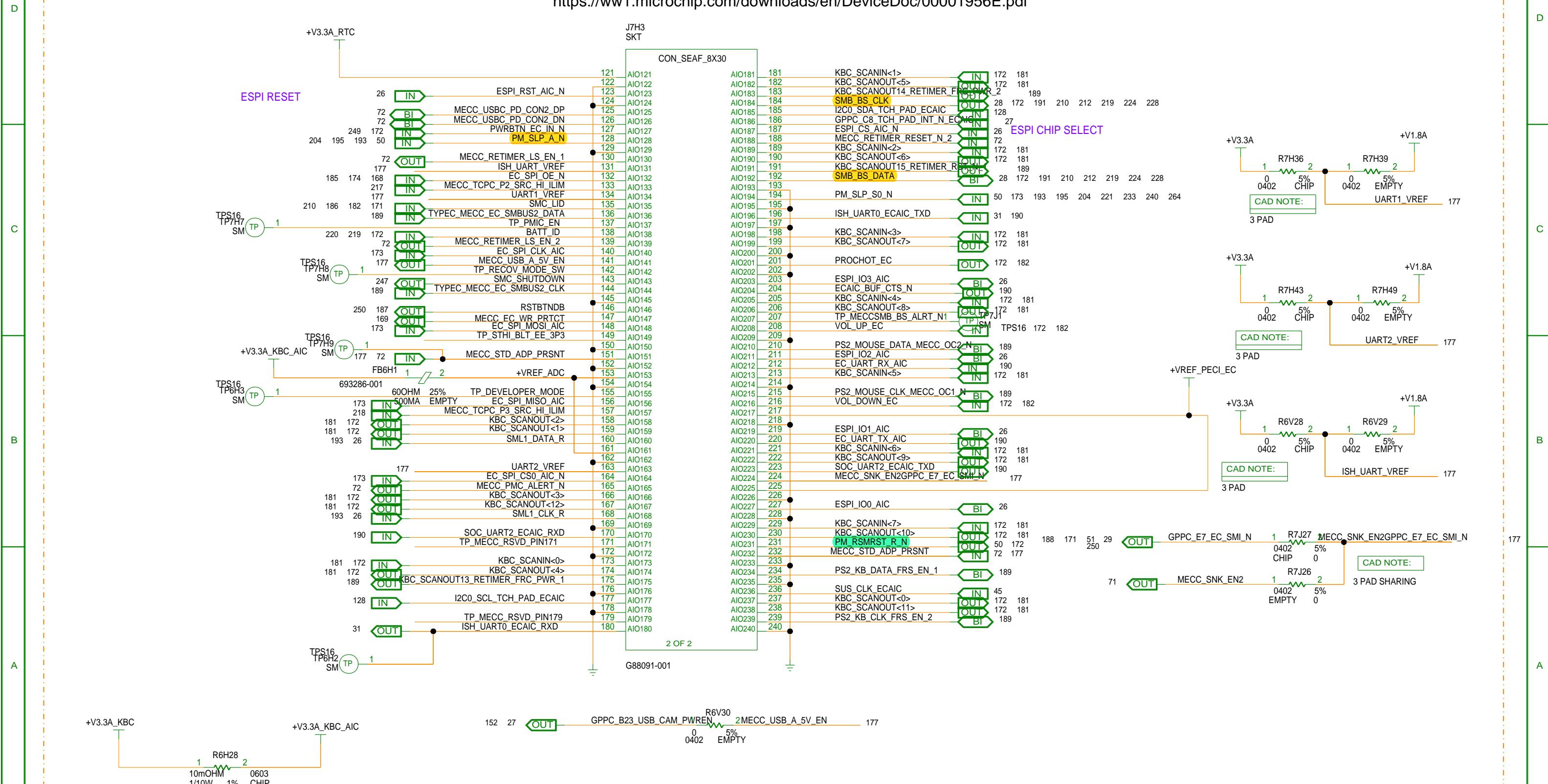
MEC140x/1x embedded

controller

<https://ww1.microchip.com/downloads/en/DeviceDoc/00001956E.pdf>

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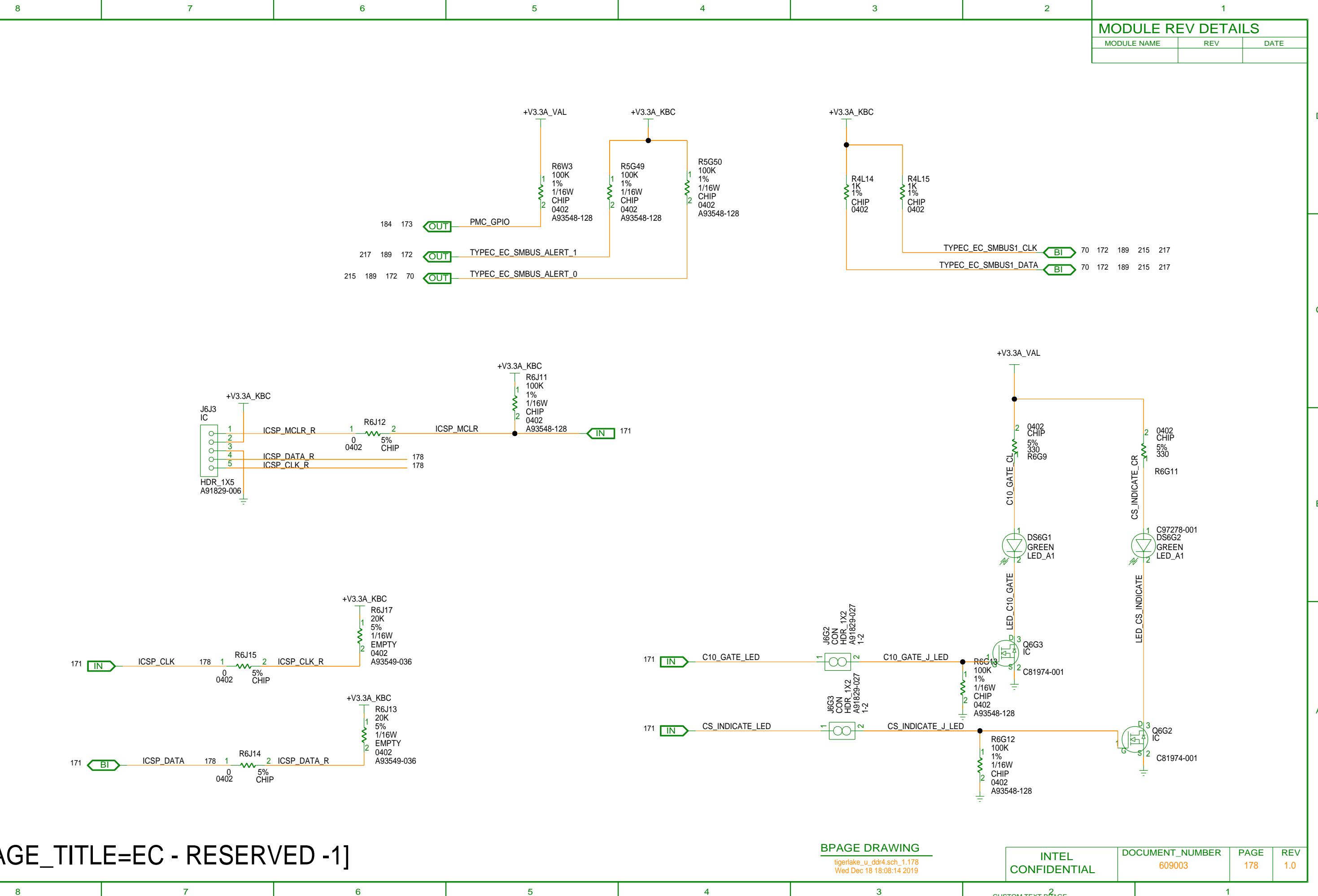
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 178	REV 1.0
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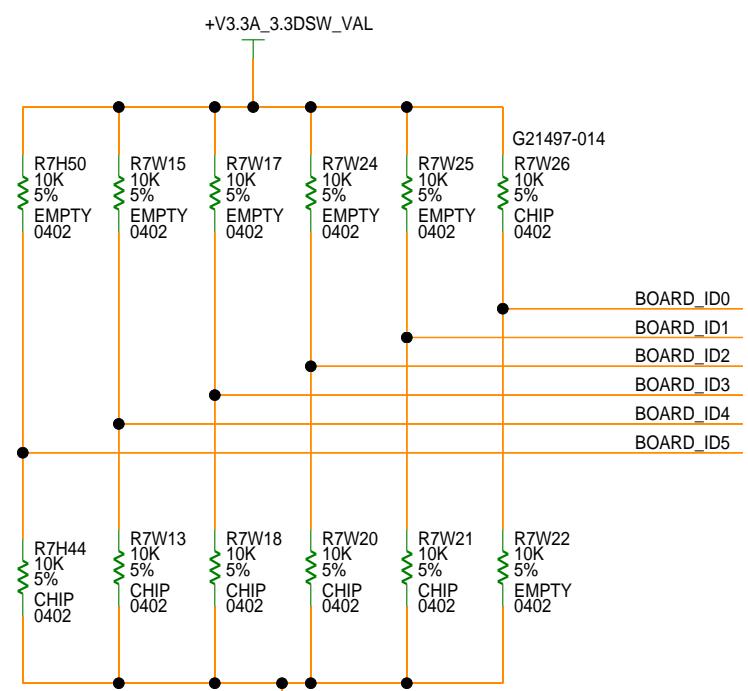
8 7 6 5 4 3 2 1

BOARD ID ,FAB ID & I/O EXPANDER

MODULE REV DETAILS

MODULE NAME	REV	DATE

BOARD REVISION



+V3.3A_3.3DSW_VAL

R7V21 10K 5% EMPTY 0402

R7V20 10K 5% CHIP 0402

R7W6 10K 5% EMPTY 0402

BRD_ID_A0

BRD_ID_A1

BRD_ID_A2

R7W1 10K 5% CHIP 0402

R7W2 10K 5% EMPTY 0402

R7W4 10K 5% CHIP 0402

R7V22 10K 5% CHIP 0402

R7V19 02

PCA9555_0_R_INT_IN

SMB_BS_IOEXP_CLK_R1

SMB_BS_IOEXP_DATA_R1

+V3.3A_3.3DSW_VAL

G21497-014

R7H6 1K 1% CHIP 0402

SPD_PRSNT_J

J7H2 CON HDR_1X2 A91829-027 1-2

SPD_PRSNT

179

R7H9 10K 5% CHIP 0402

179

+V3.3A_3.3DSW_VAL

G21796-026

R6W4 1 RETIMER_BYPASS_STRAP_SW

173

1% CHIP 0402

1/16W CHIP 10K 5%

R7W14 G21497-014

G21796-026

R6W5 ESPI_TESTCRD_DET_STRAP_SW

173

1% CHIP 0402

G21796-026

R6W6 1 PMC_GPIO_SW

173

1% CHIP 0402

ESPI_TESTCRD_DET

R7W16 G21497-014

173 179

+V3.3A_3.3DSW_VAL

0402 1/16W CHIP 10K 5%

173

BPAGE DRAWING

tigerlake_u_ddr4.sch_1.179

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DOCUMENT_NUMBER

609003

PAGE

179

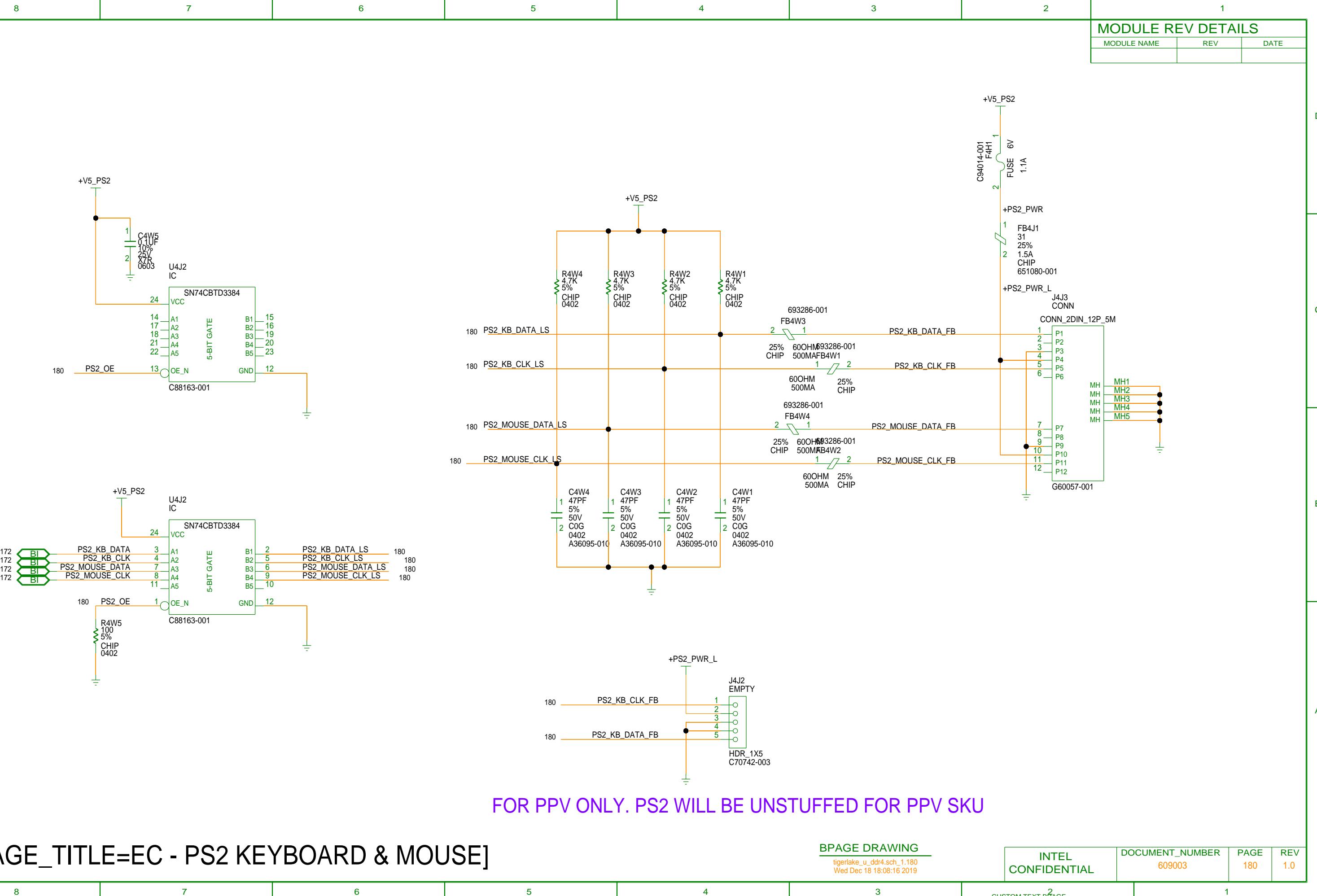
REV

1.0

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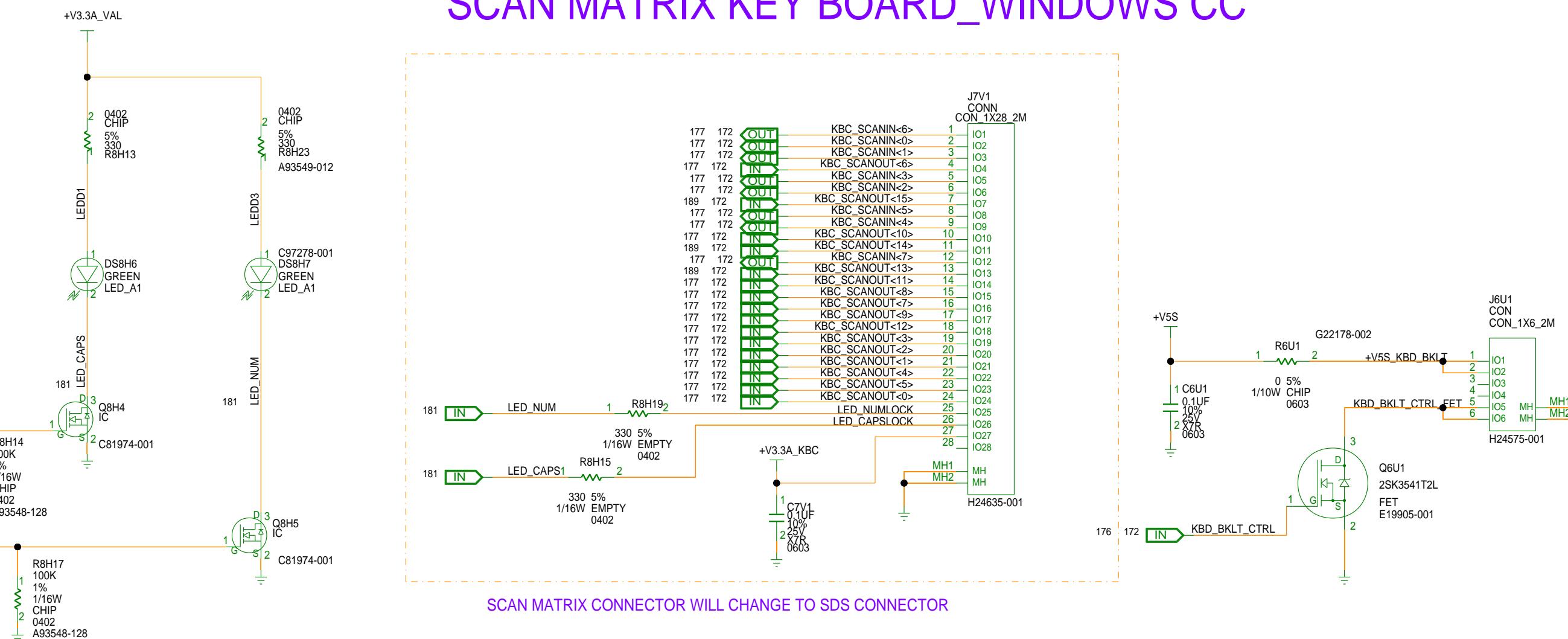
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8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME						REV	DATE

SCAN MATRIX KEY BOARD_WINDOWS CC

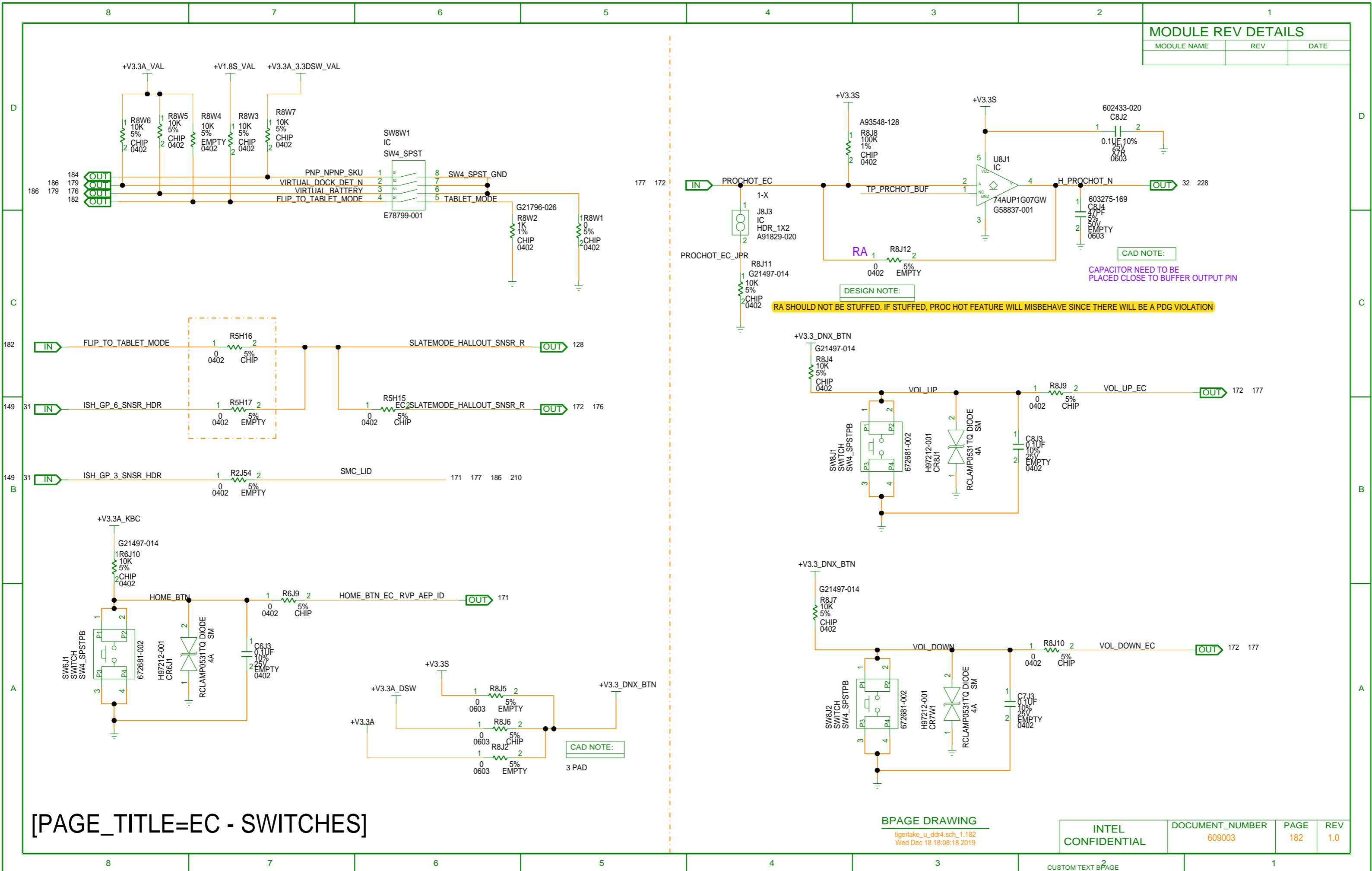


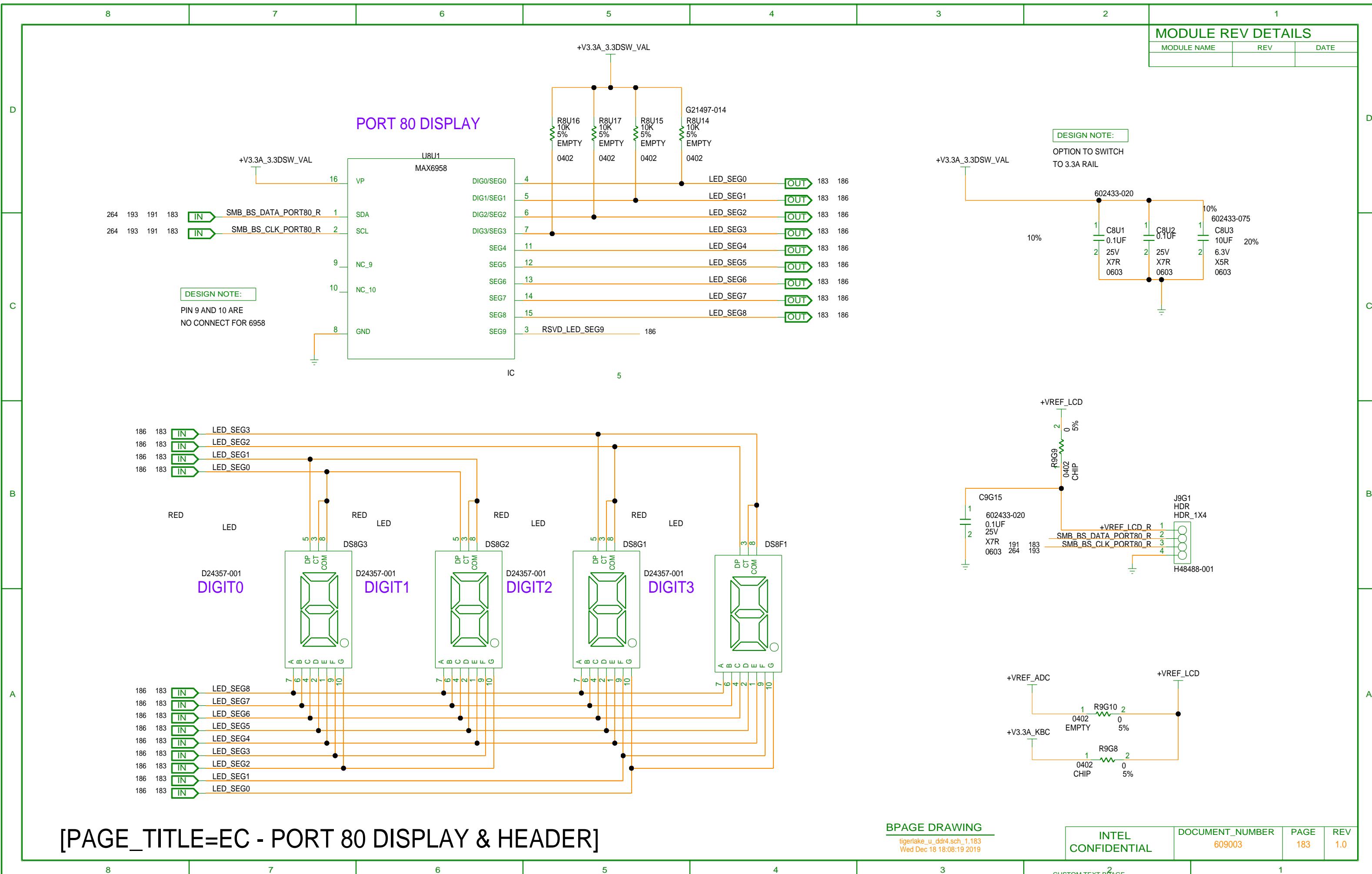
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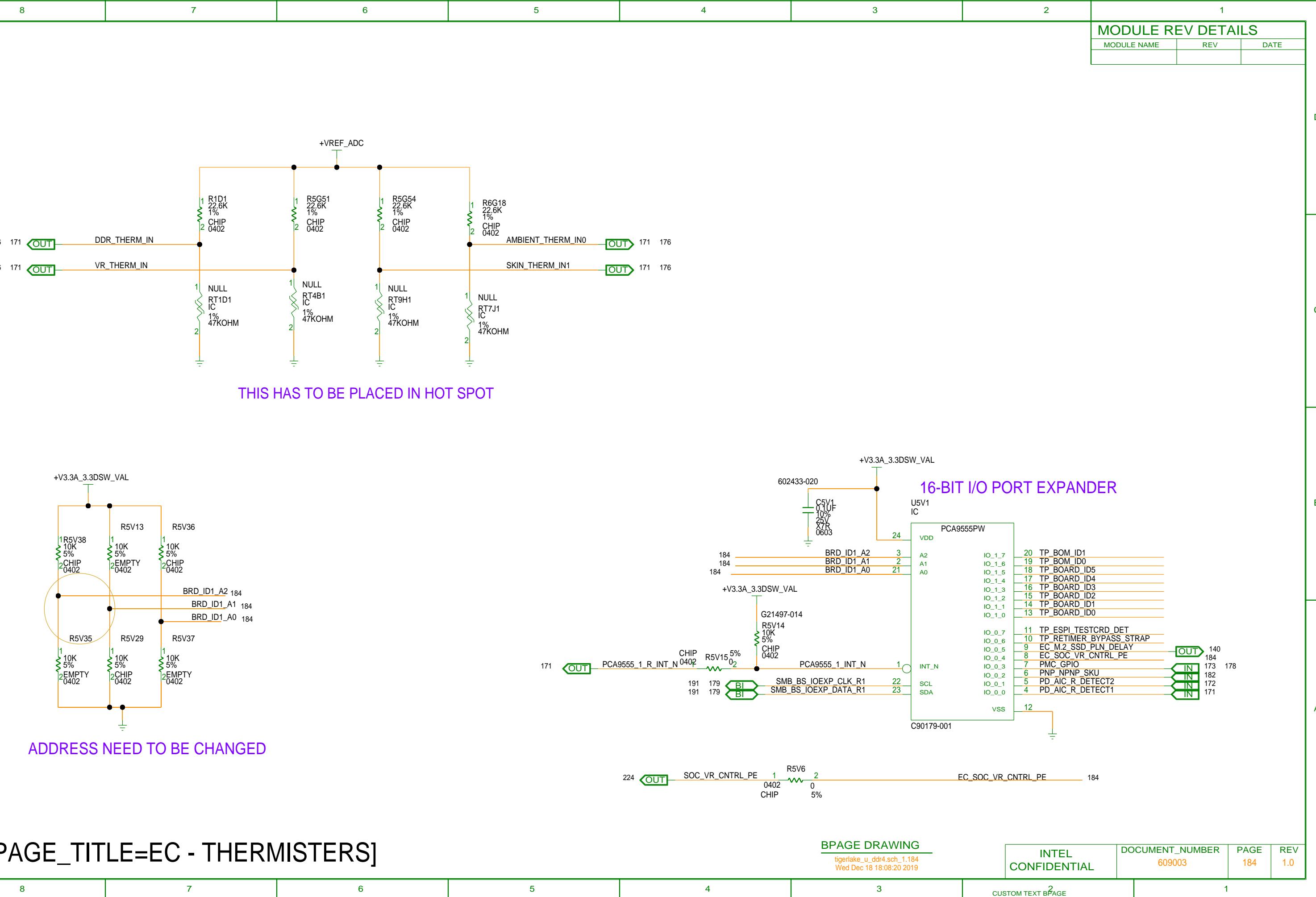
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Wed Dec 18 18:08:17 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 181	REV 1.0
CUSTOM TEXT BPAGE			1

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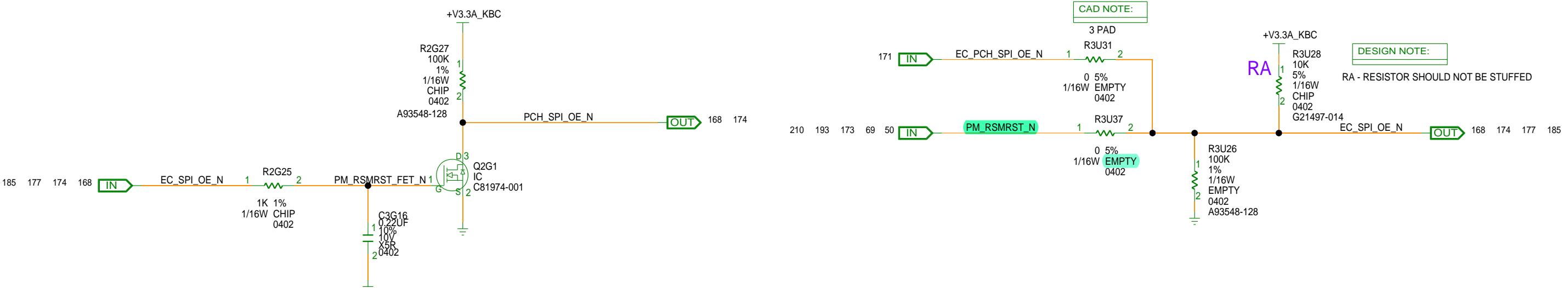
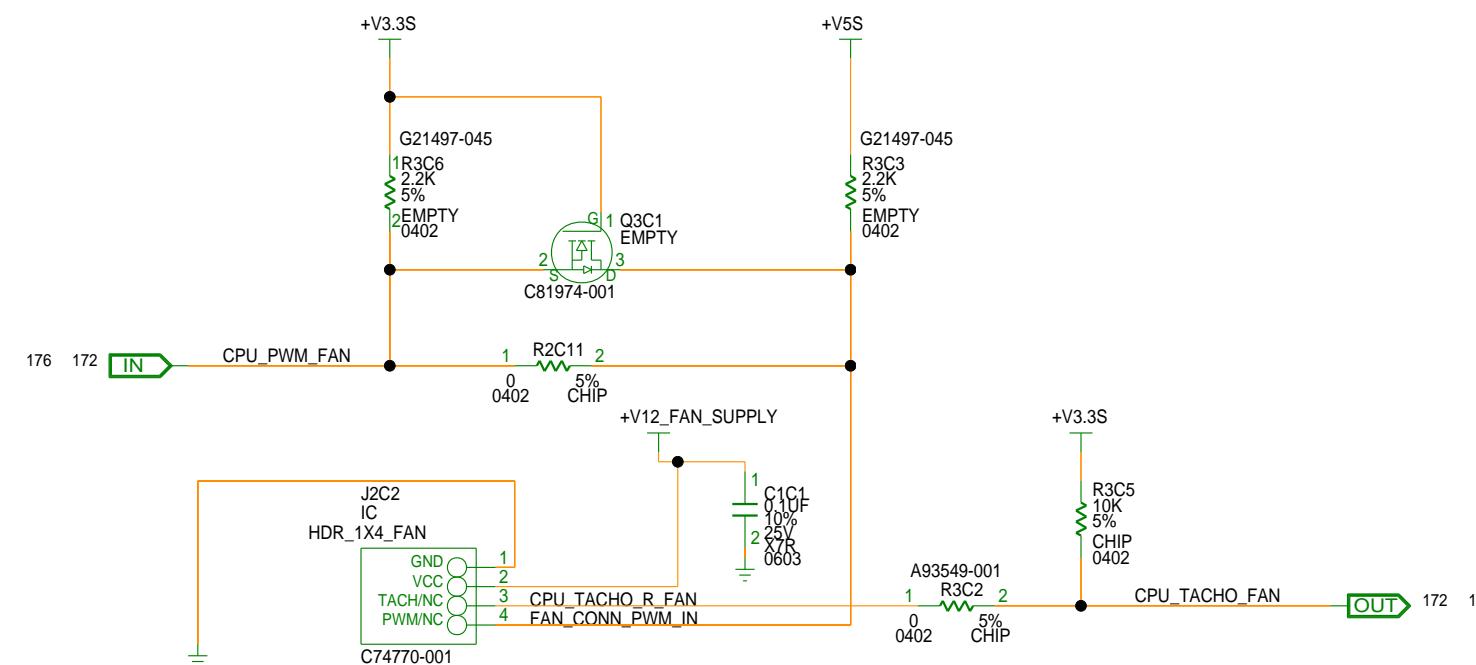




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MODULE REV DETAILS		
MODULE NAME	REV	DATE

PROCESSOR FAN CONTROL



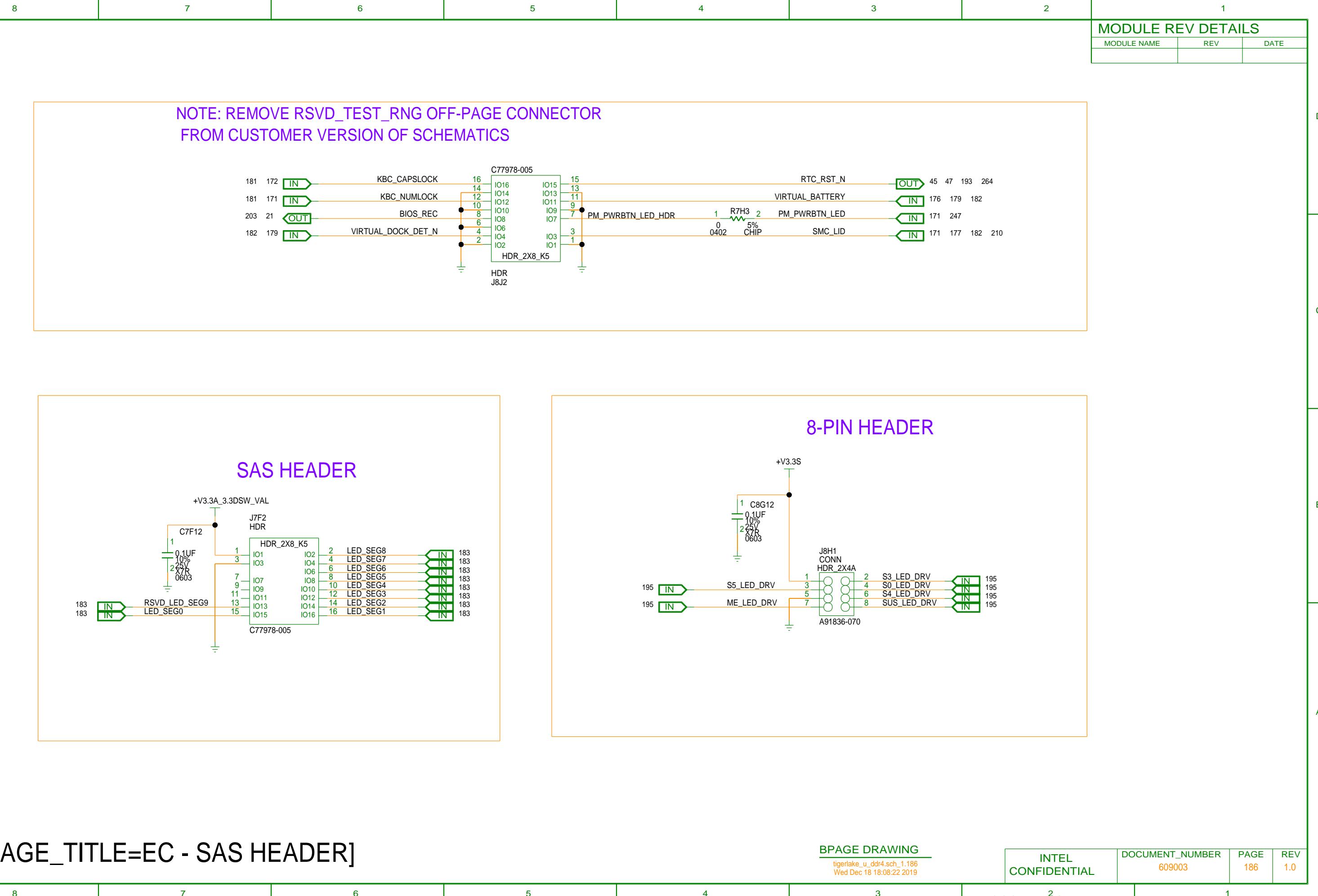
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Wed Dec 18 18:08:21 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	185	1.0

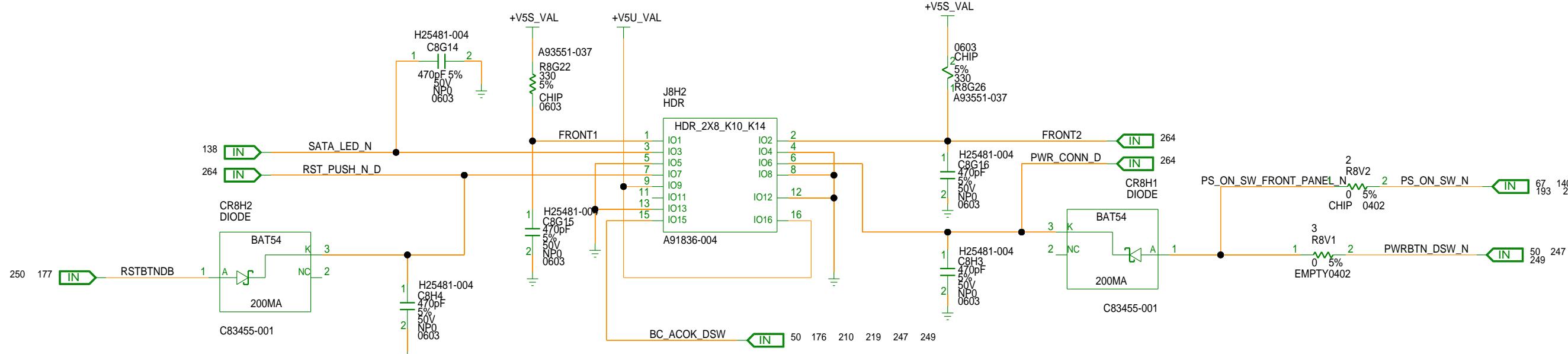
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8	7	6	5	4	3	2	1
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8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME						REV	DATE

FRONT PANEL HEADER



[PAGE_TITLE=EC - FRONT PANEL HEADER]

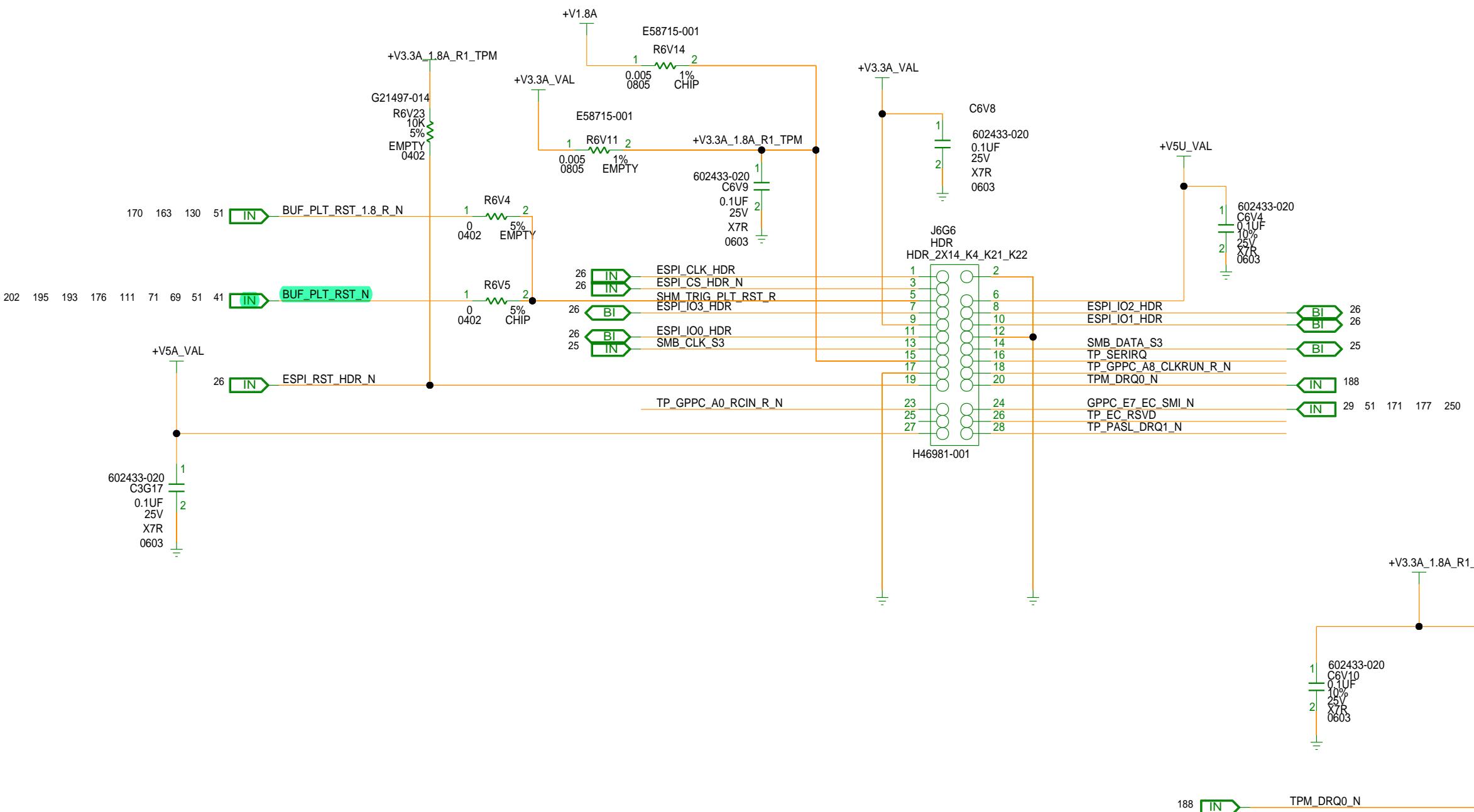
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Wed Dec 18 18:08:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 187	REV 1.0
CUSTOM TEXT BPAGE			1

8	7	6	5	4	3	2	1
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8	7	6	5	4	3	2	1
MODULE REV DETAILS							

ESPI BUS HEADER

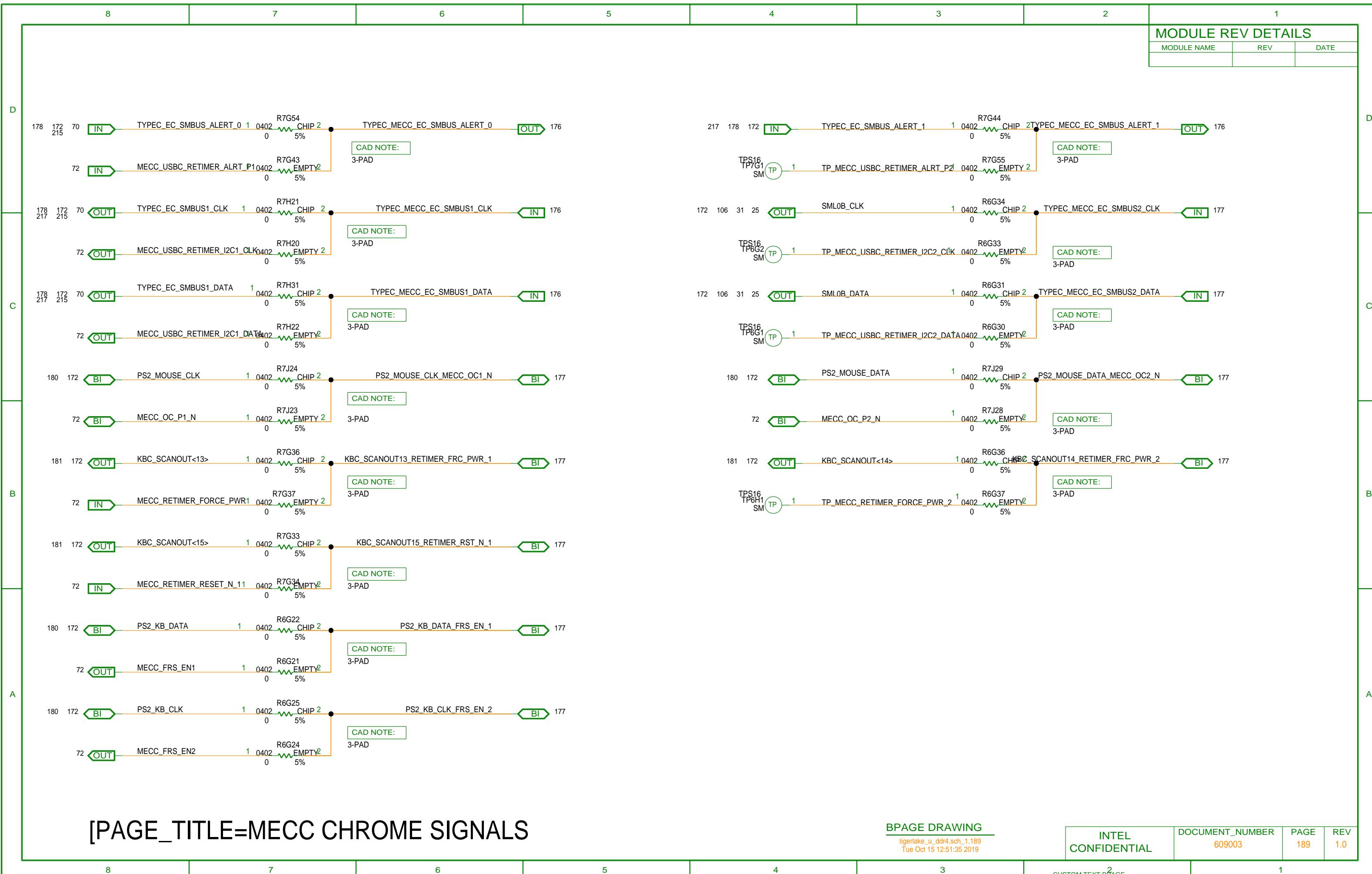


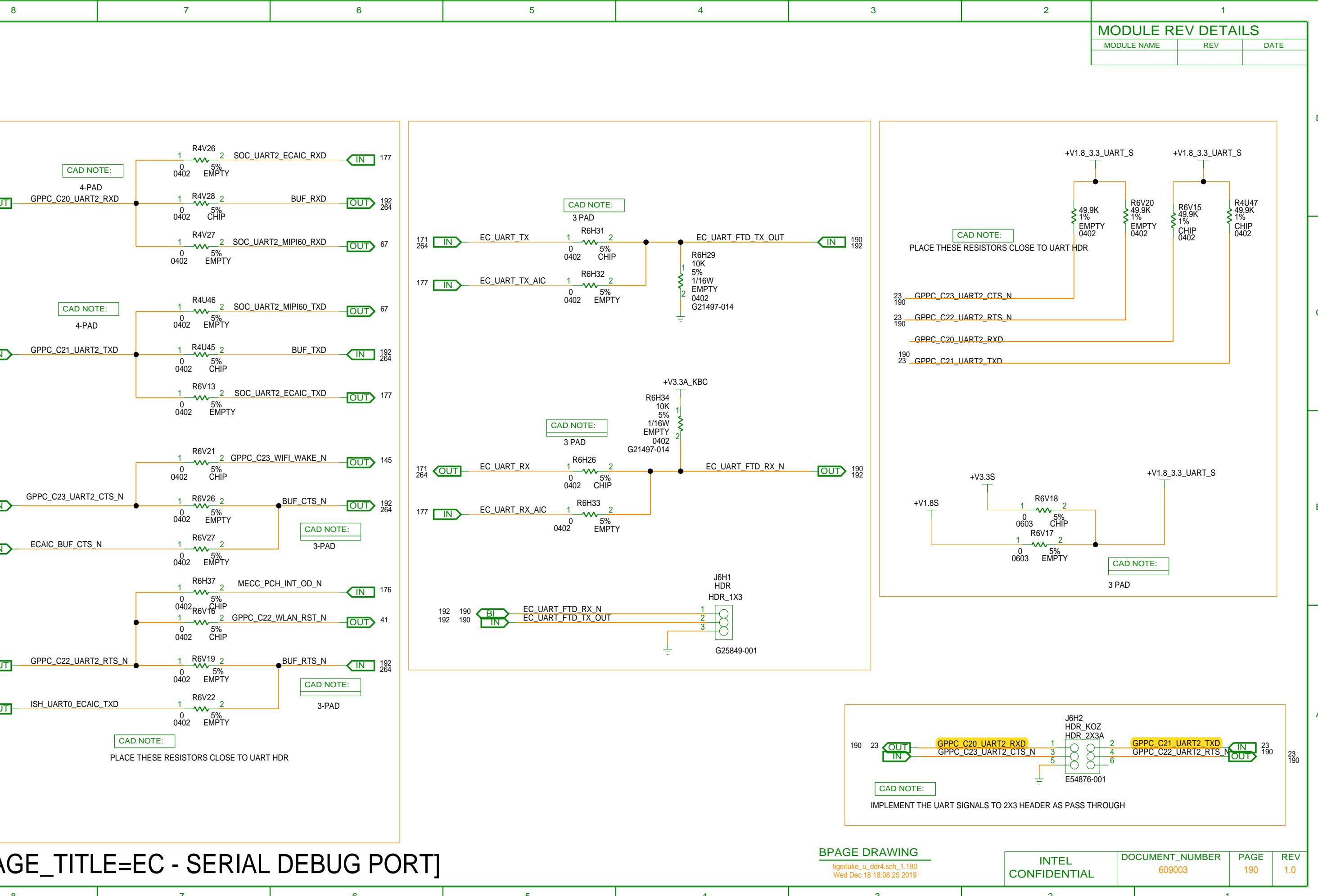
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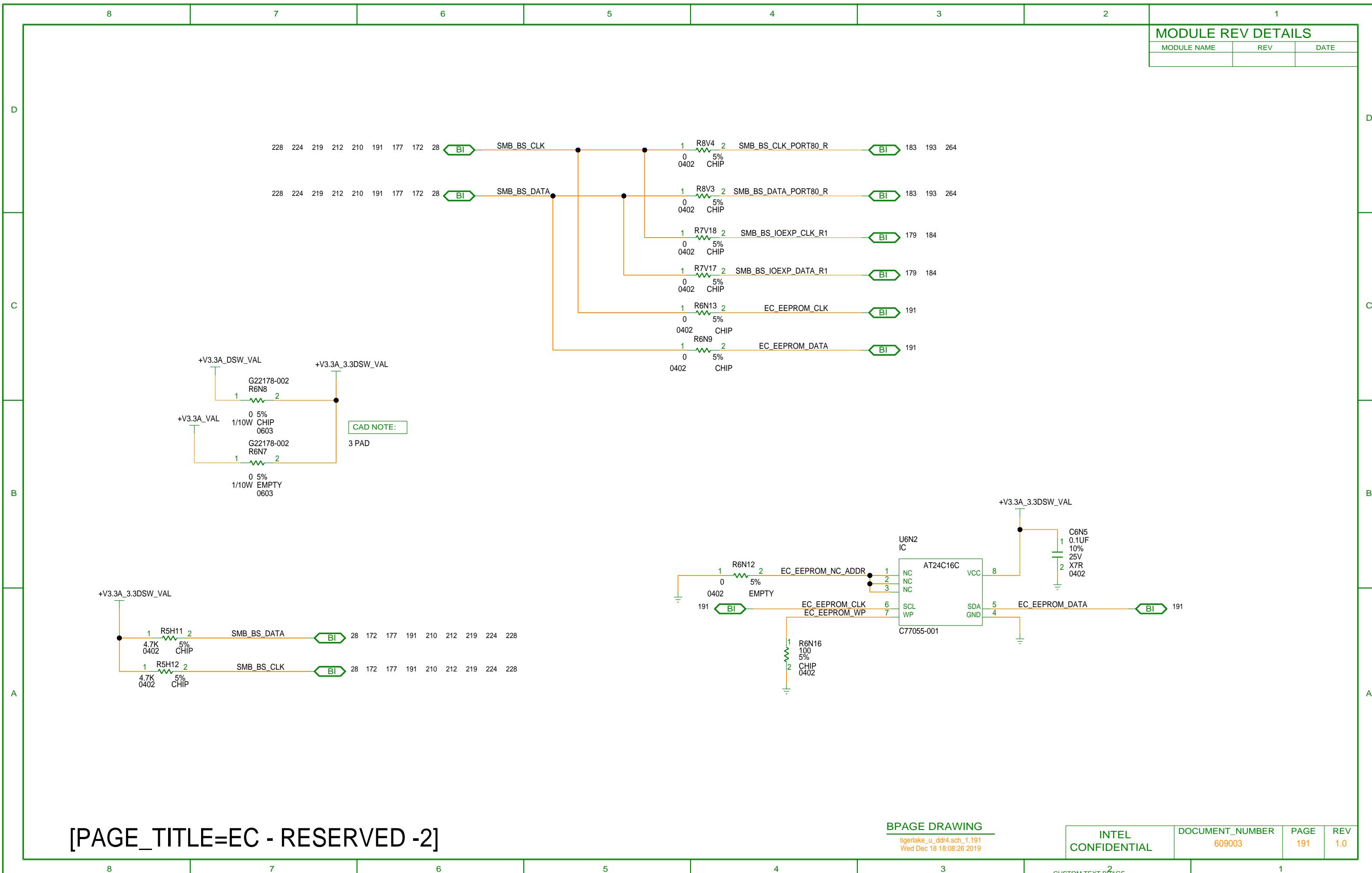
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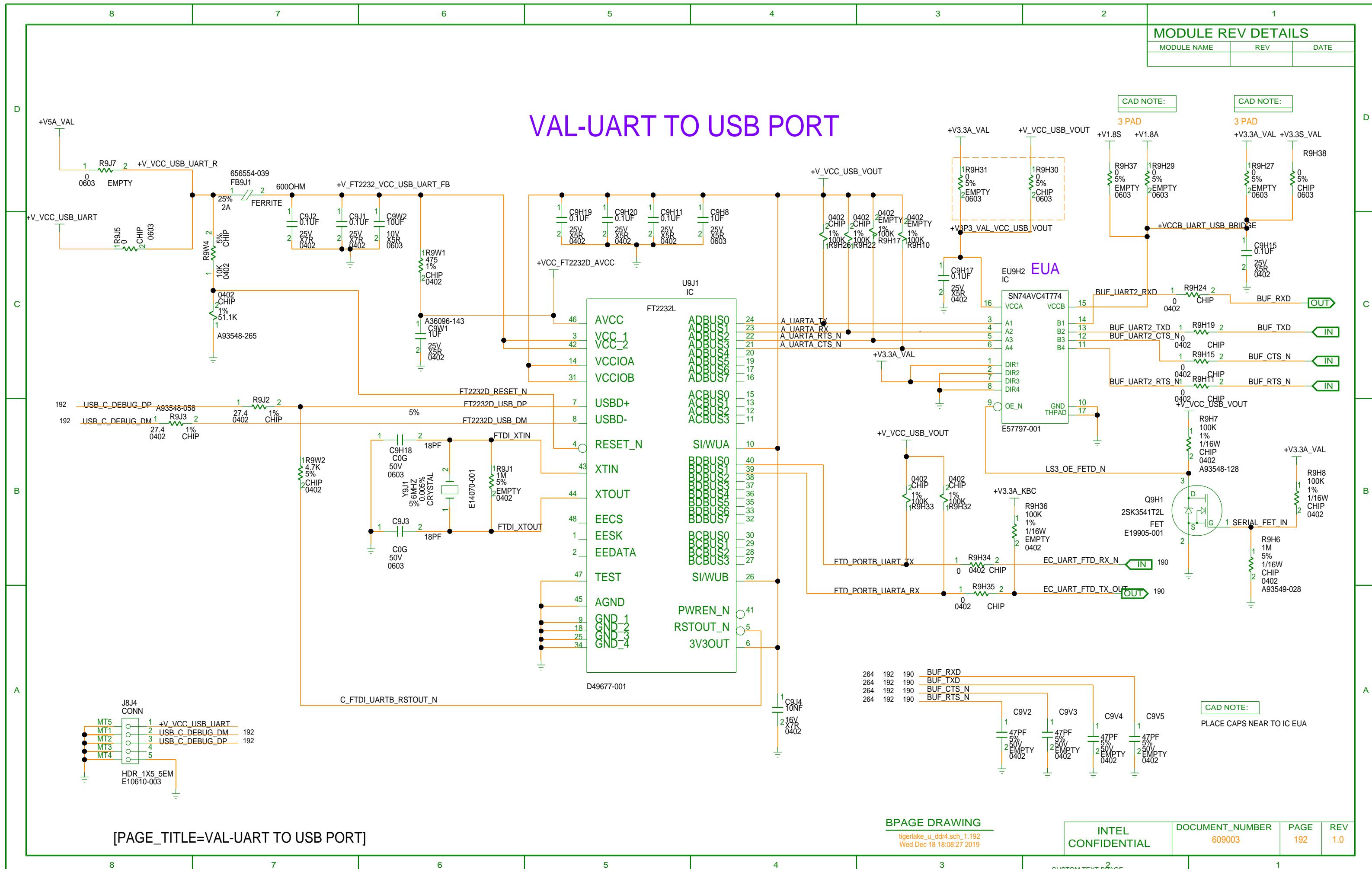
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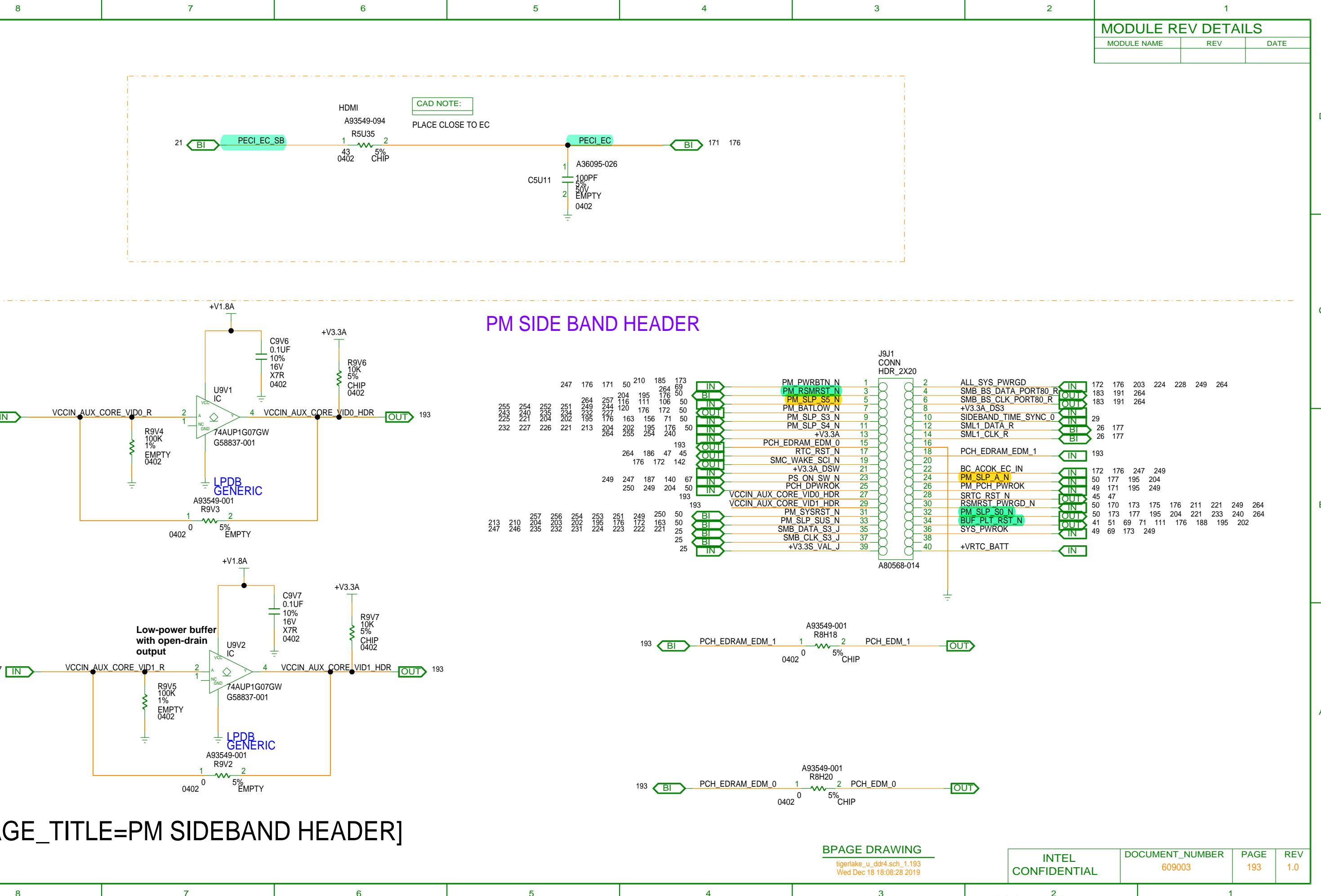
8	7	6	5	4	3	2	1
CUSTOM TEXT BPAGE							











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MODULE REV DETAILS

MODULE NAME	REV	DATE

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BPAGE DRAWING
tigerlake_u_ddr4.sch_1.194
Tue Oct 15 12:51:41 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 194	REV 1.0
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CUSTOM TEXT
2 PAGE

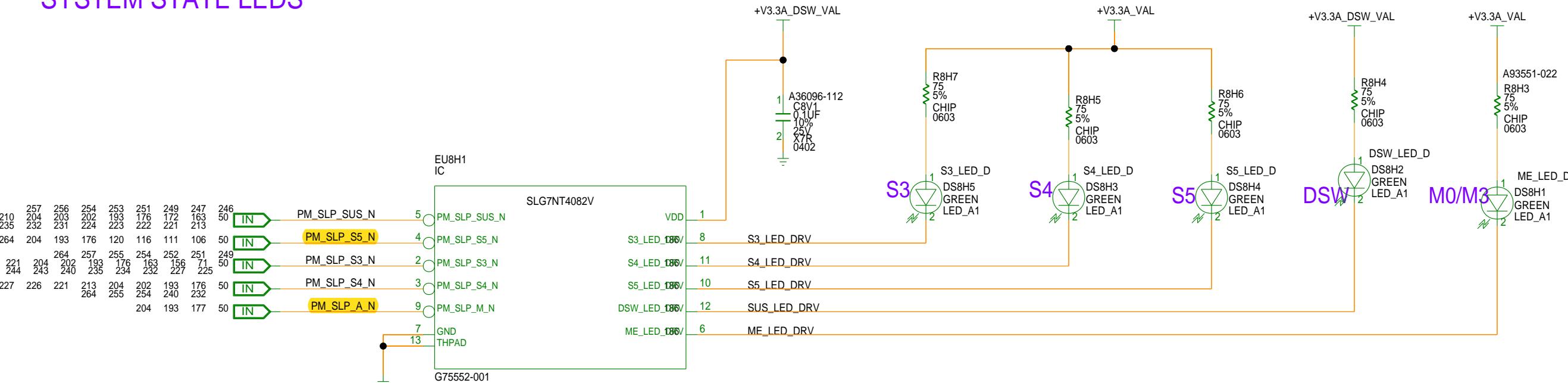
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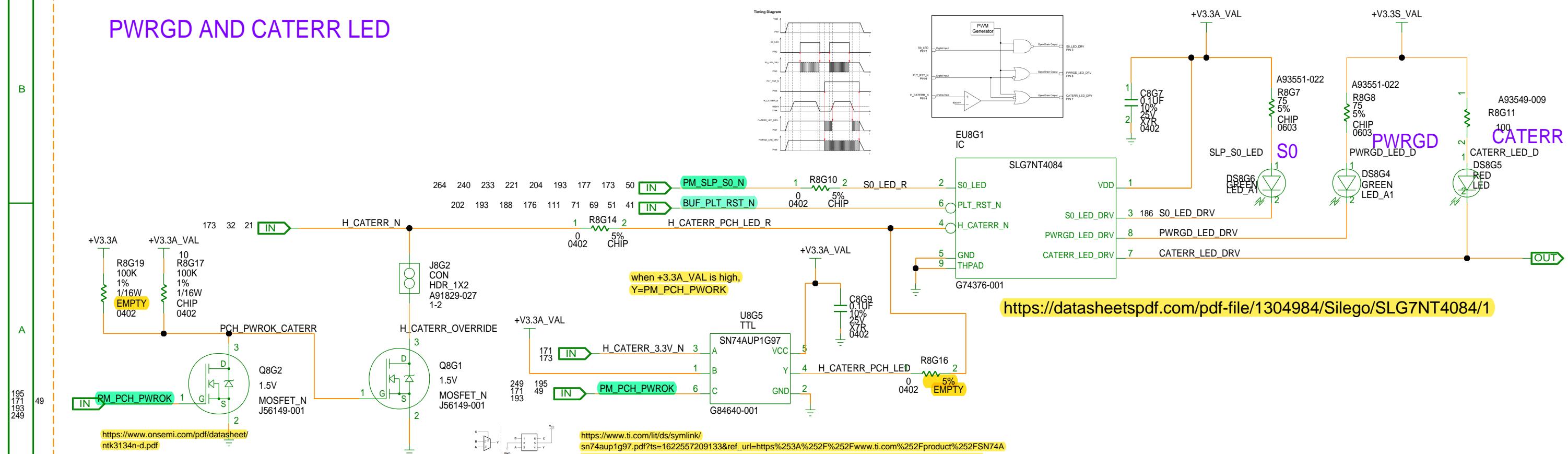
MODULE REV DETAILS

MODULE NAME	REV	DATE

SYSTEM STATE LEDS



PWRGD AND CATERR LED



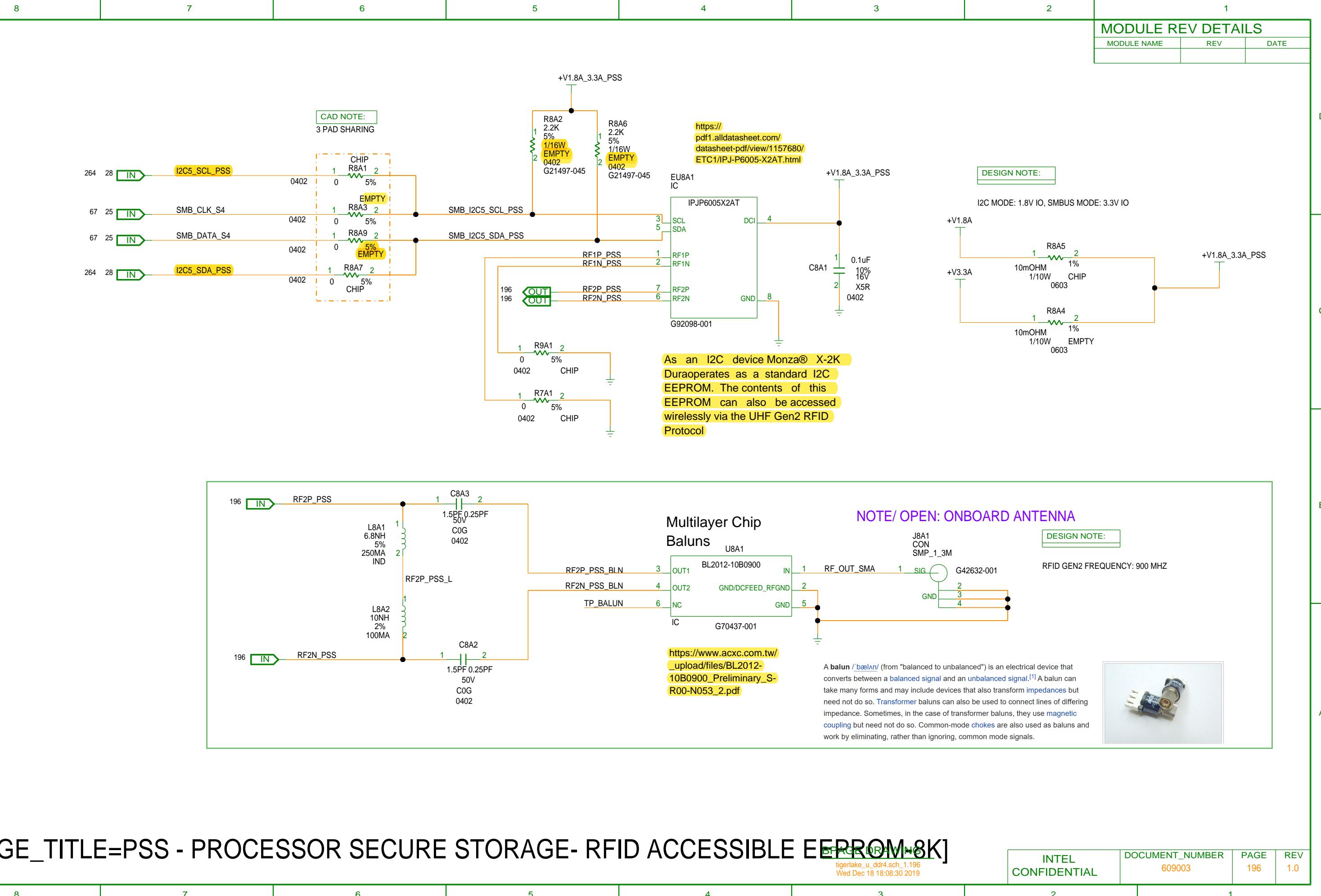
[PAGE_TITLE=SYSTEM STATE LED CIRCUITRY]

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Wed Dec 18 18:08:30 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	195	1.0	

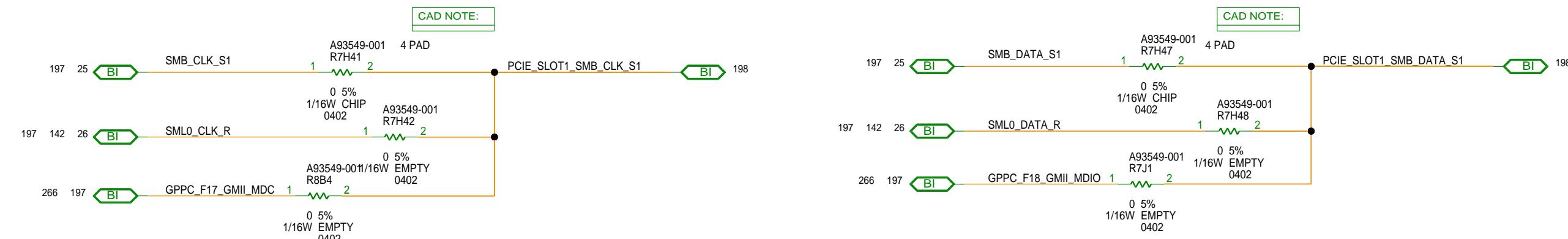
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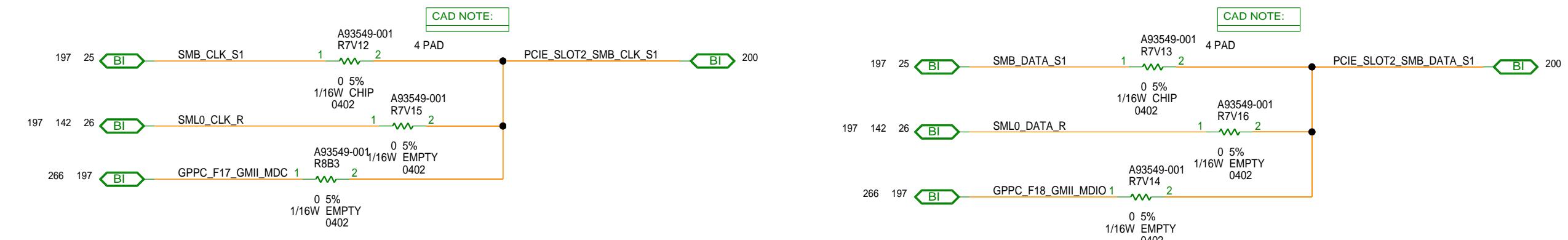


8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME				REV	DATE		

PCIE SLOT 1 SMB SIGNALS



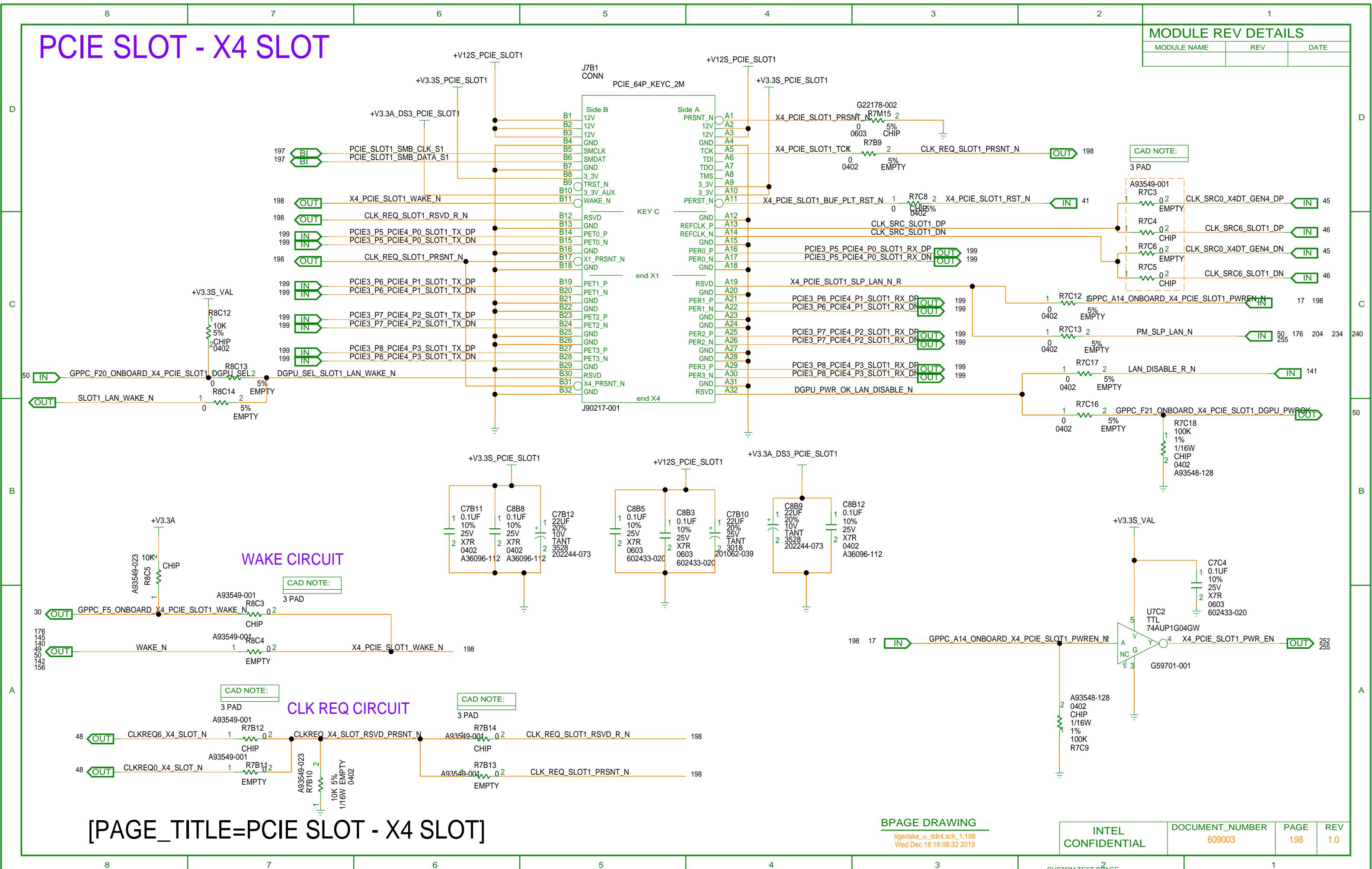
PCIE SLOT 2 SMB SIGNALS

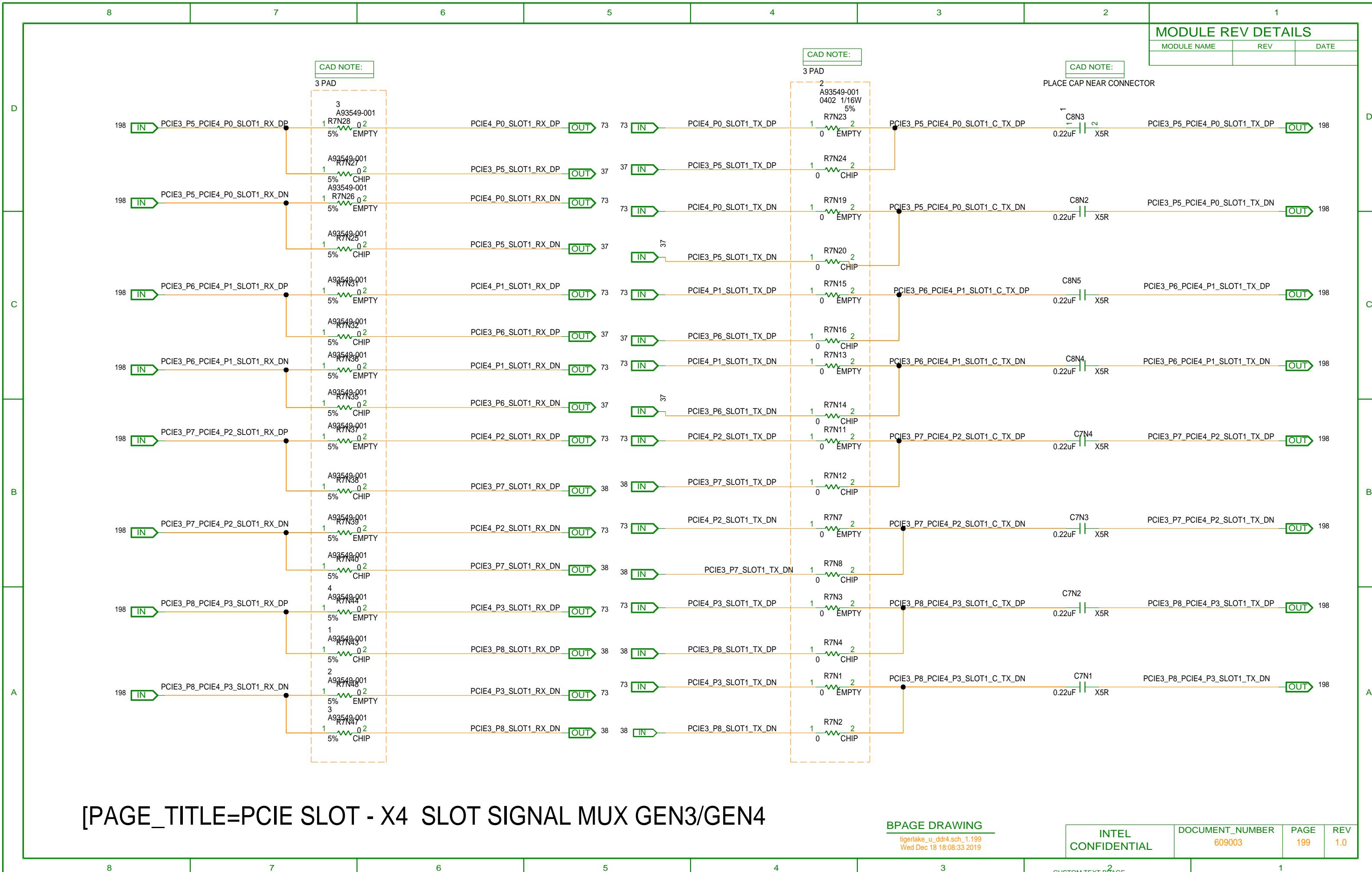


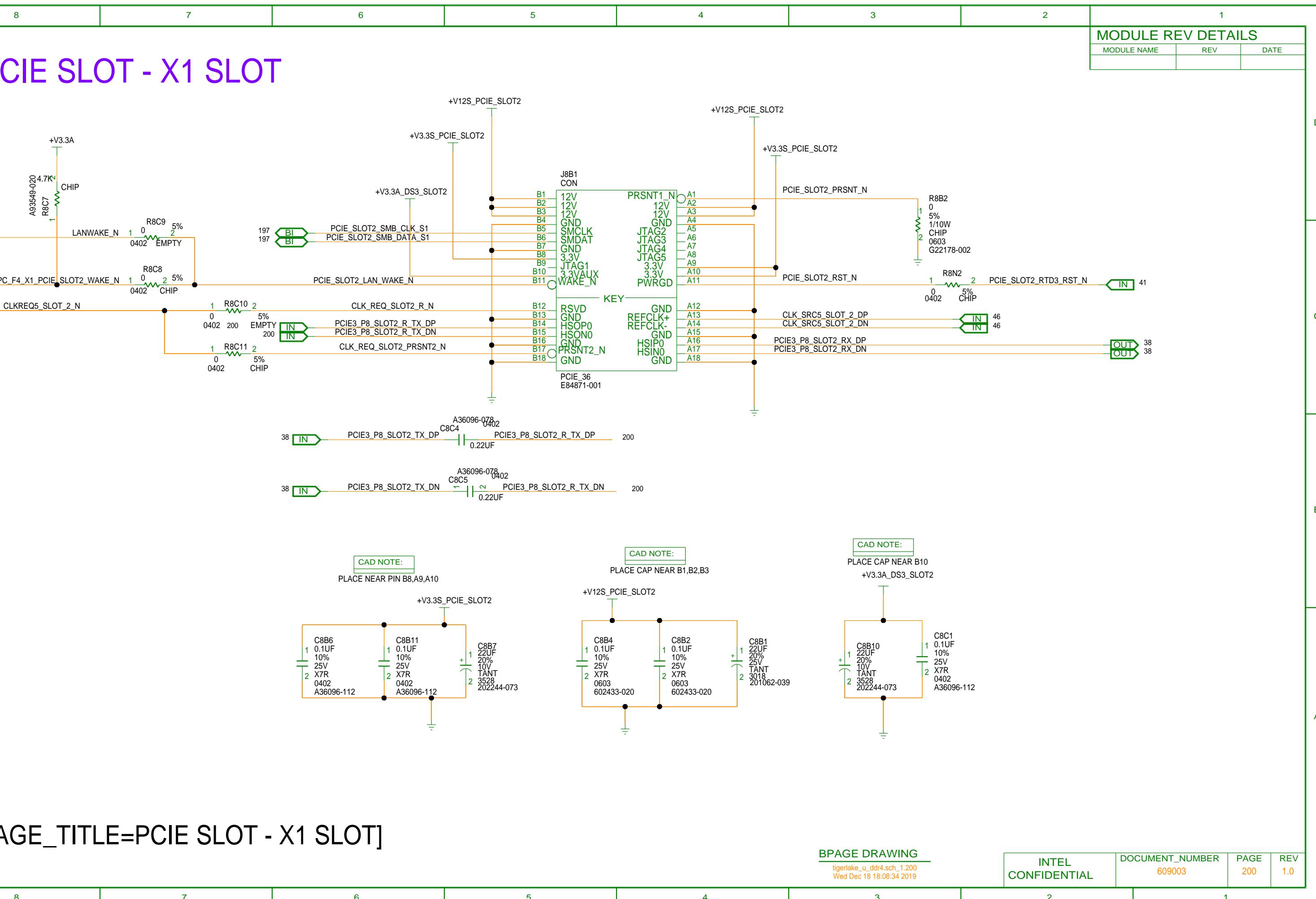
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Wed Dec 18 18:08:31 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 197	REV 1.0
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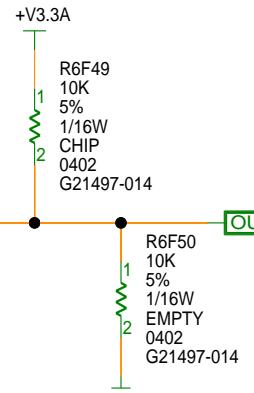
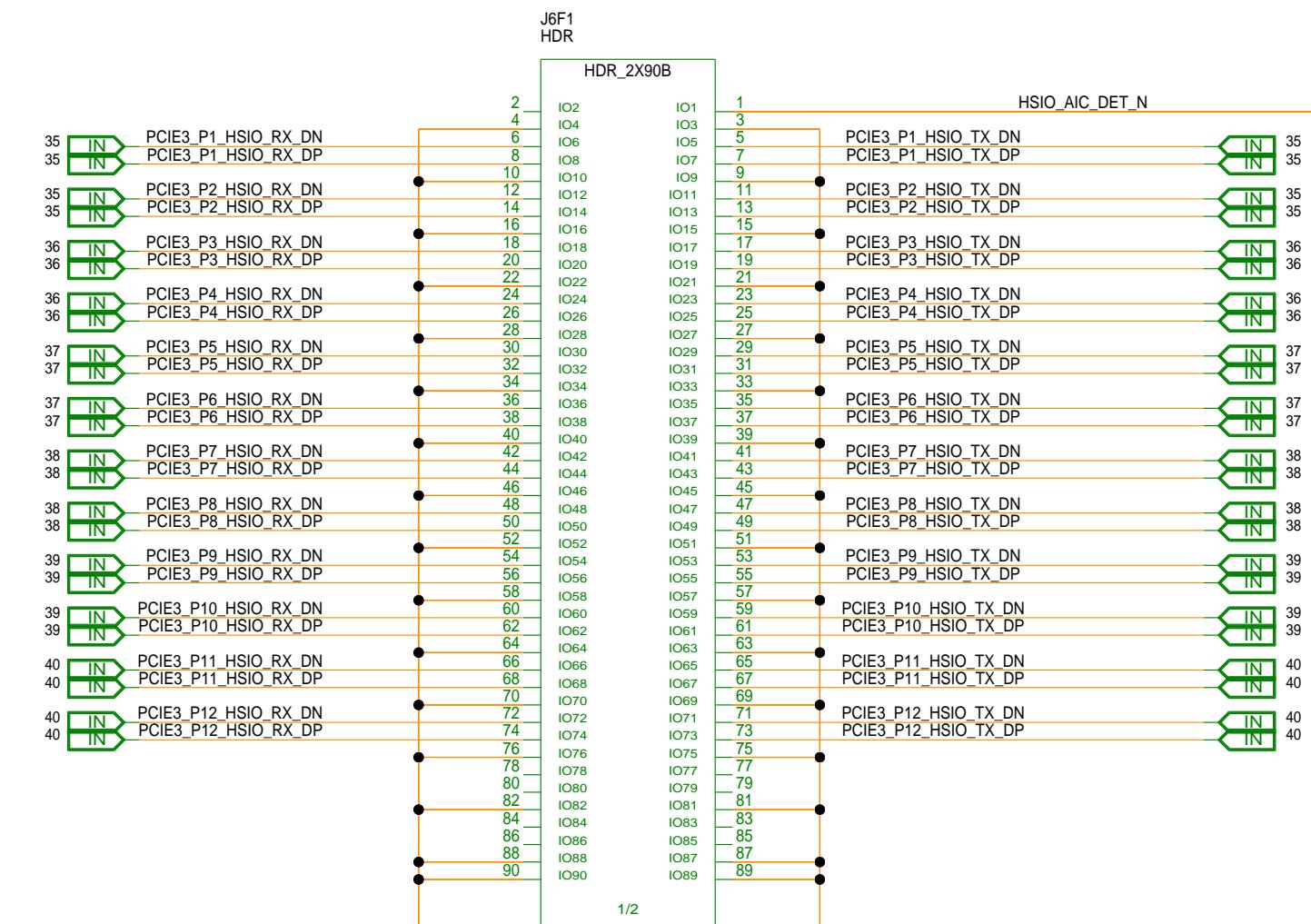
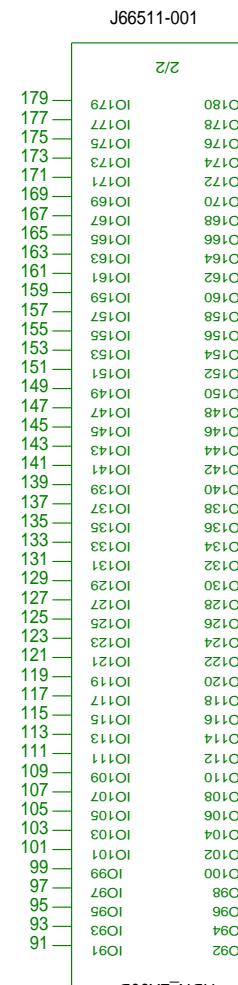






8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME						REV	DATE

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



D

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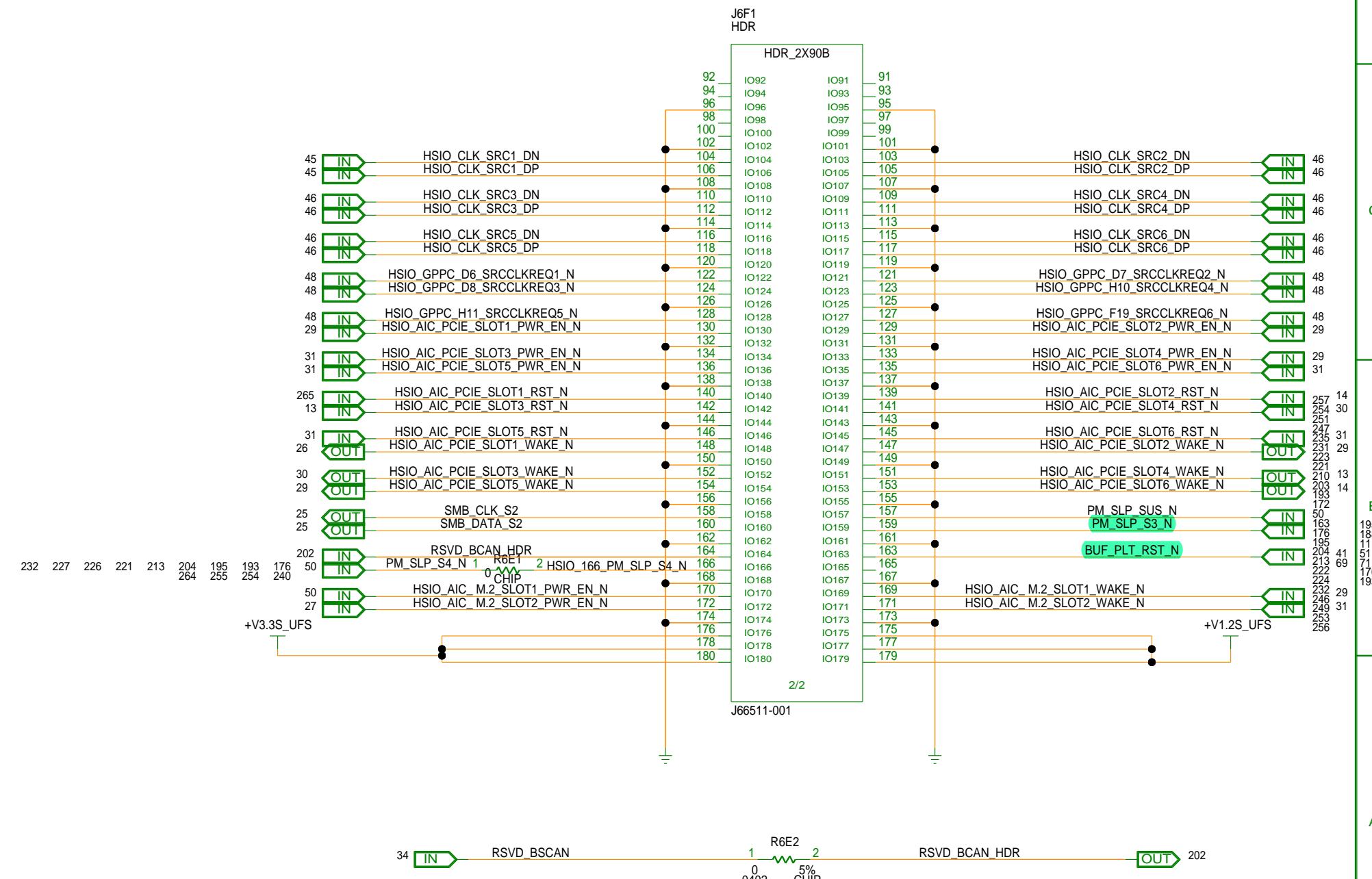
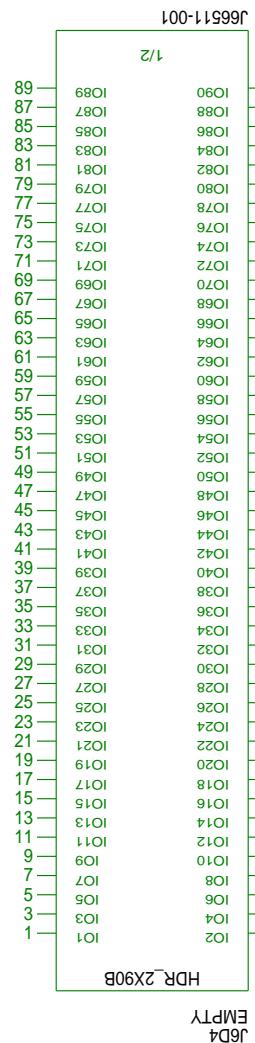
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8	7	6	5	4	3	2	1
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



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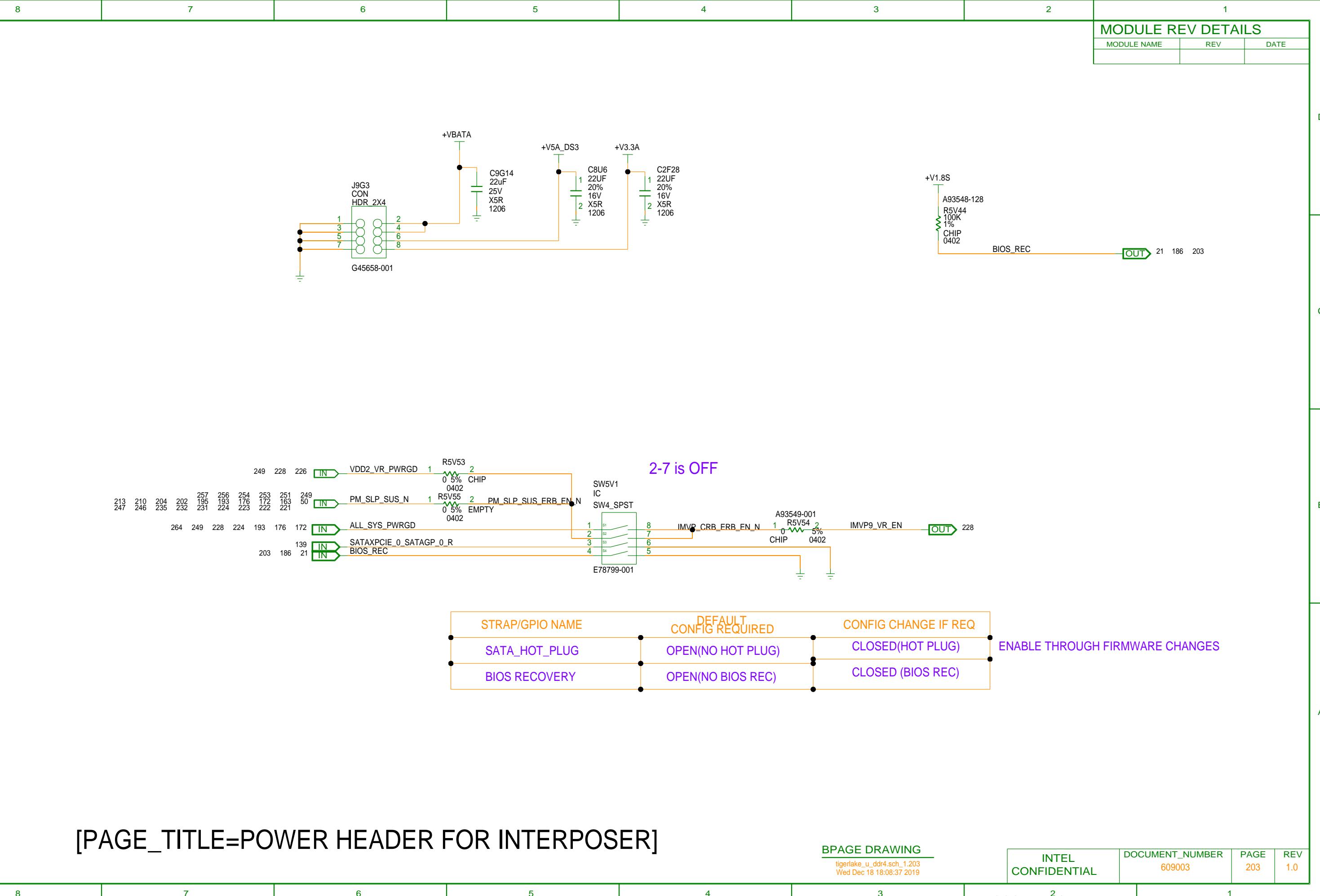
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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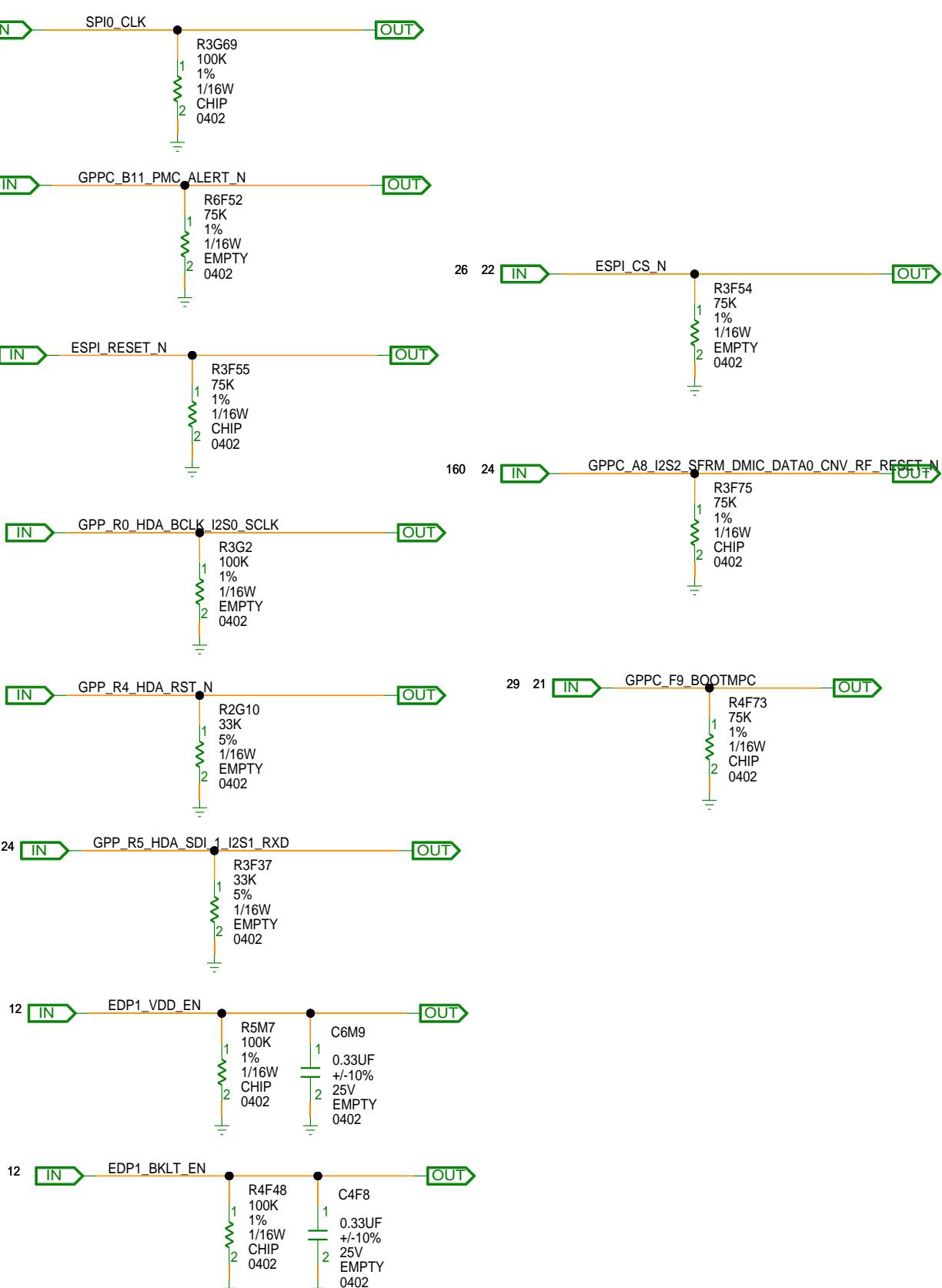
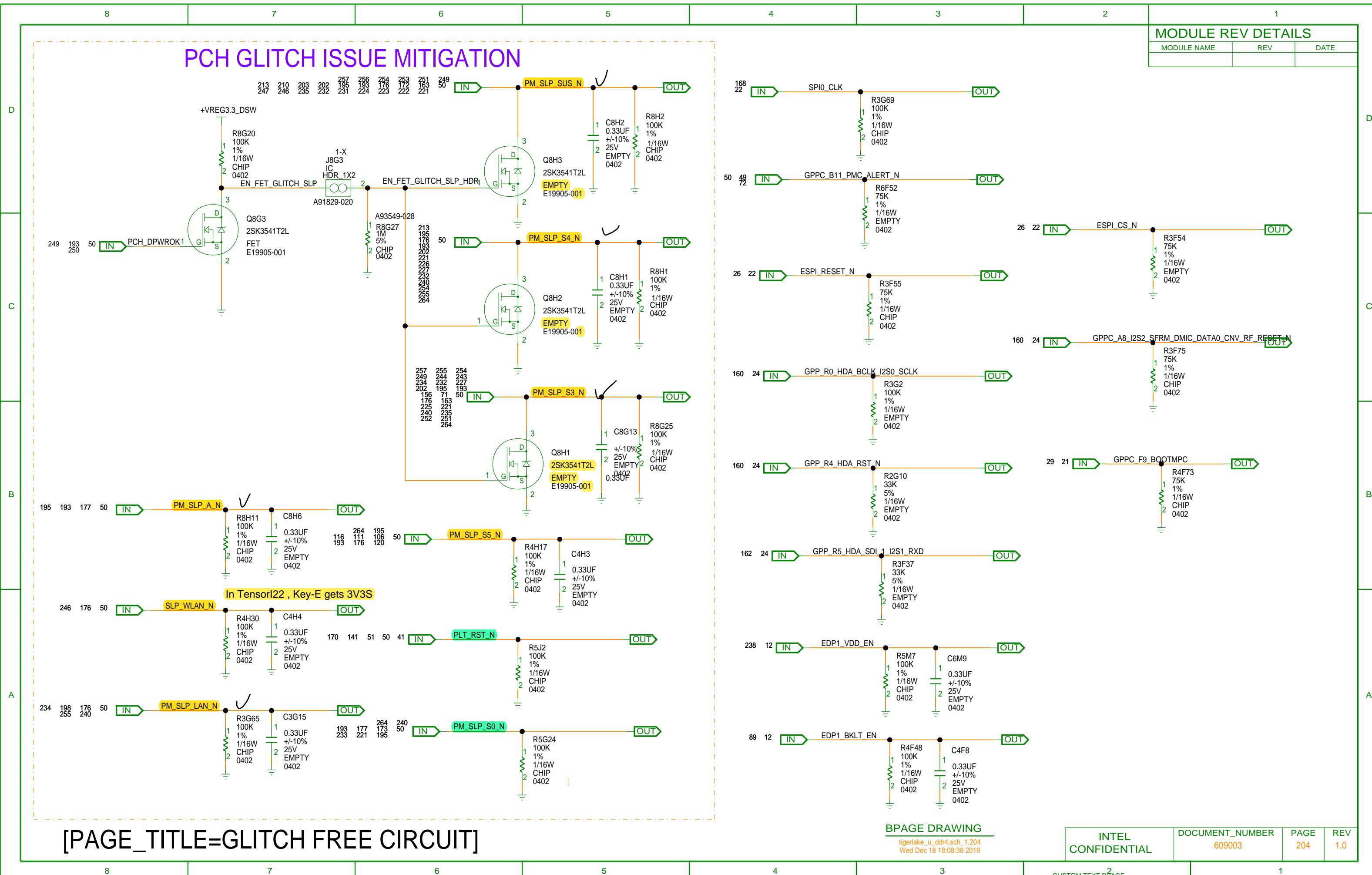
8	7	6	5	4	3	2	1
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CUSTOM TEXT B PAGE

1



PCH GLITCH ISSUE MITIGATION



8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

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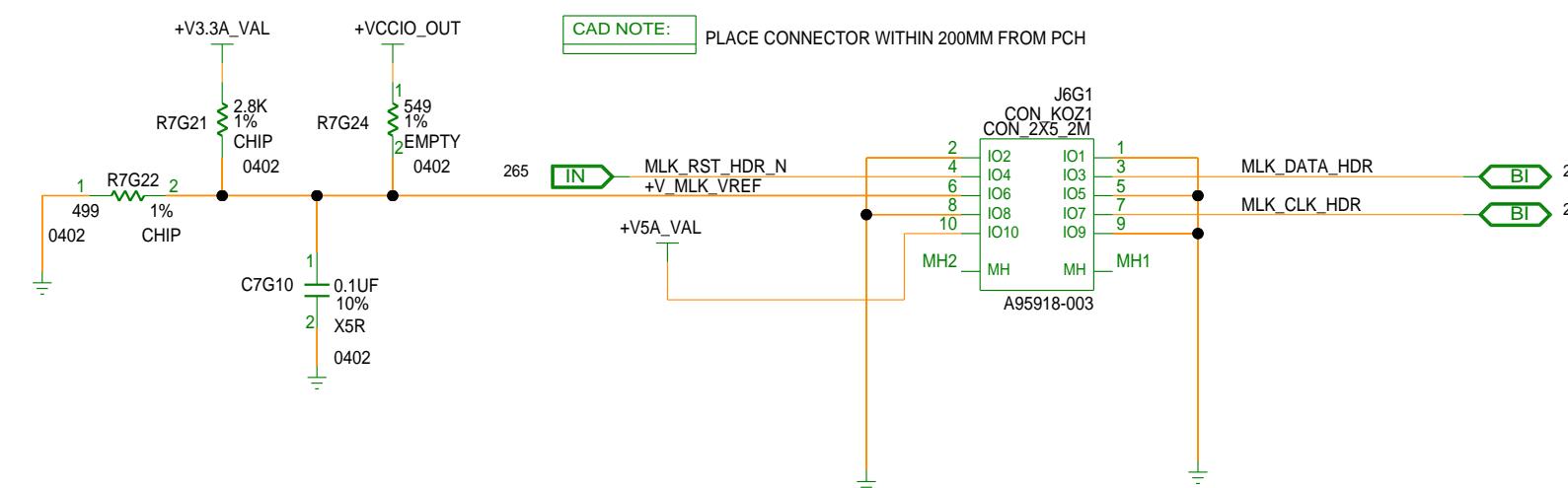
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MLINK HEADER



[PAGE_TITLE=MLX HEADER]

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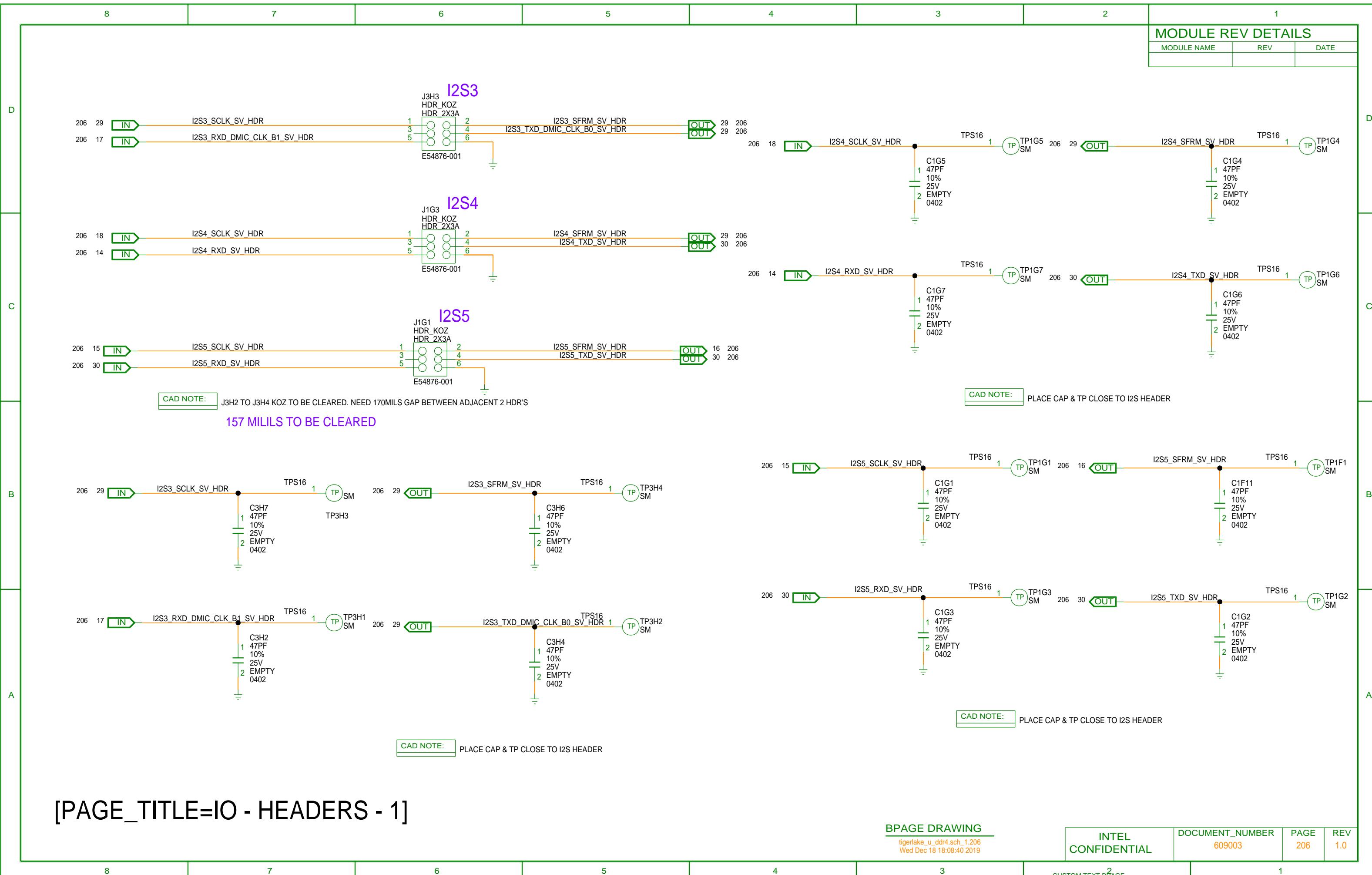
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Wed Dec 18 18:08:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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MODULE REV DETAILS

MODULE NAME	REV	DATE



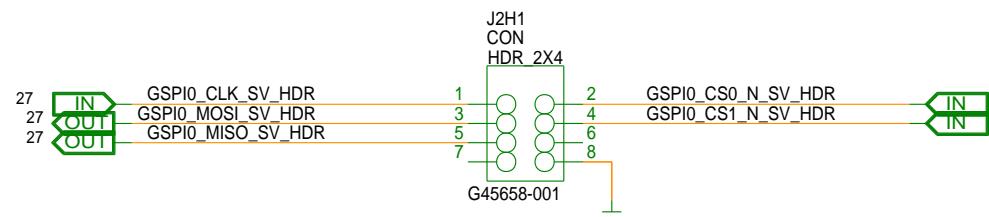
8	7	6	5	4	3	2	1
MODULE REV DETAILS							

CAD NOTE: MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

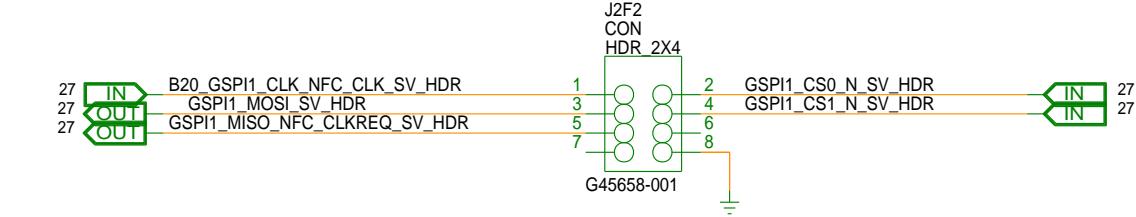
CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

GSPI0 HEADER



GSPI1 HEADER



GSPI2 IS AVAILABLE ON ISH SPI AND ISH UART HEADER
SPI1 IS AVAILABLE ON THC SV HEADER

8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

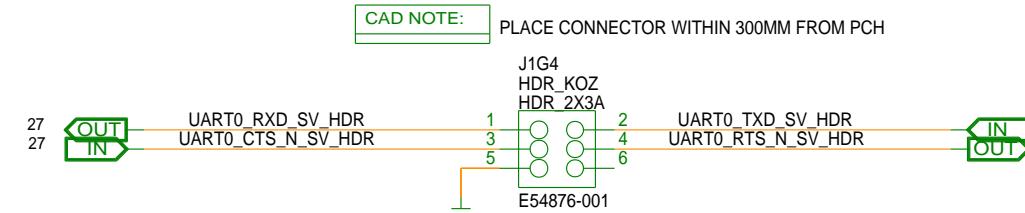
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D

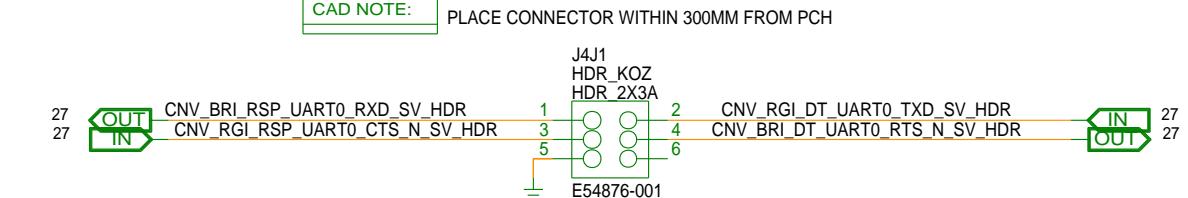
CAD NOTE:

MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

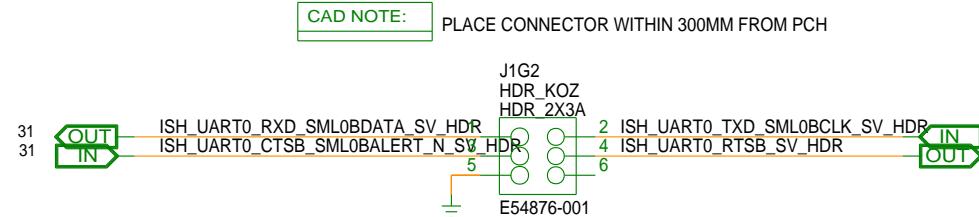
LPSS UART0 HEADER



CNV UART0 HEADER

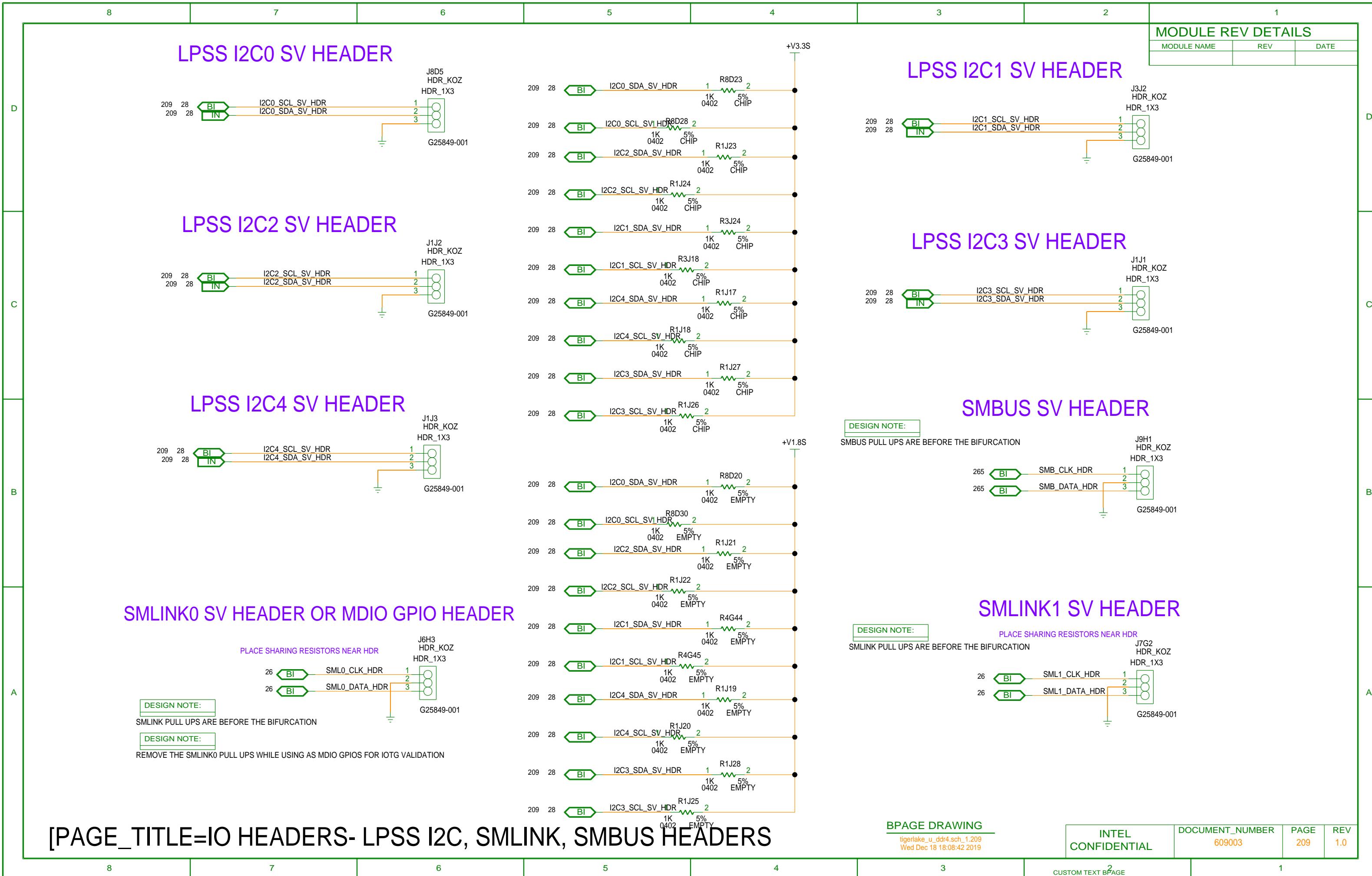


ISH UART0 / SMLINK0B HEADER



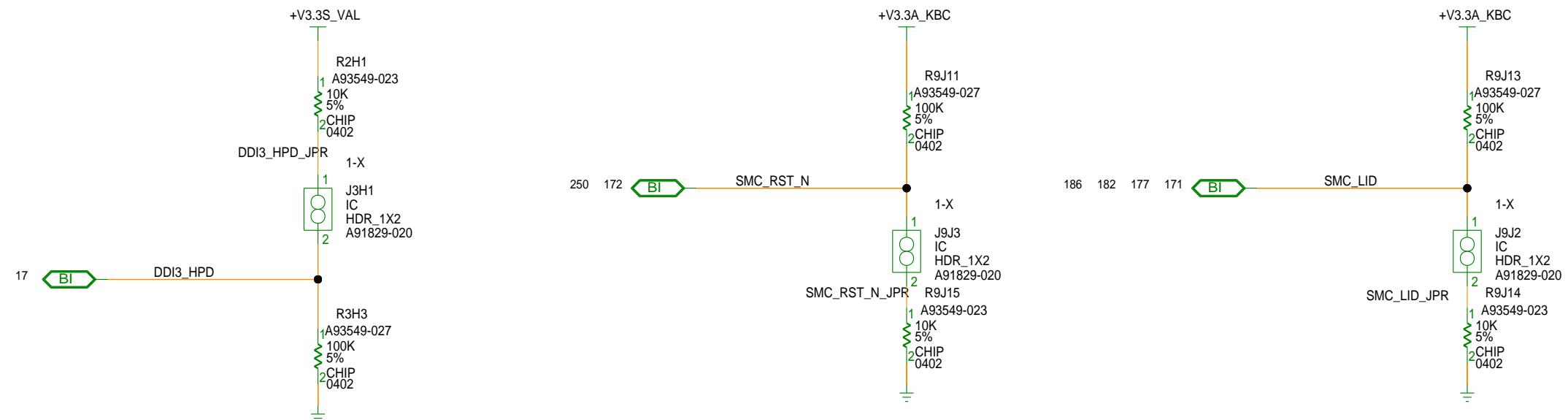
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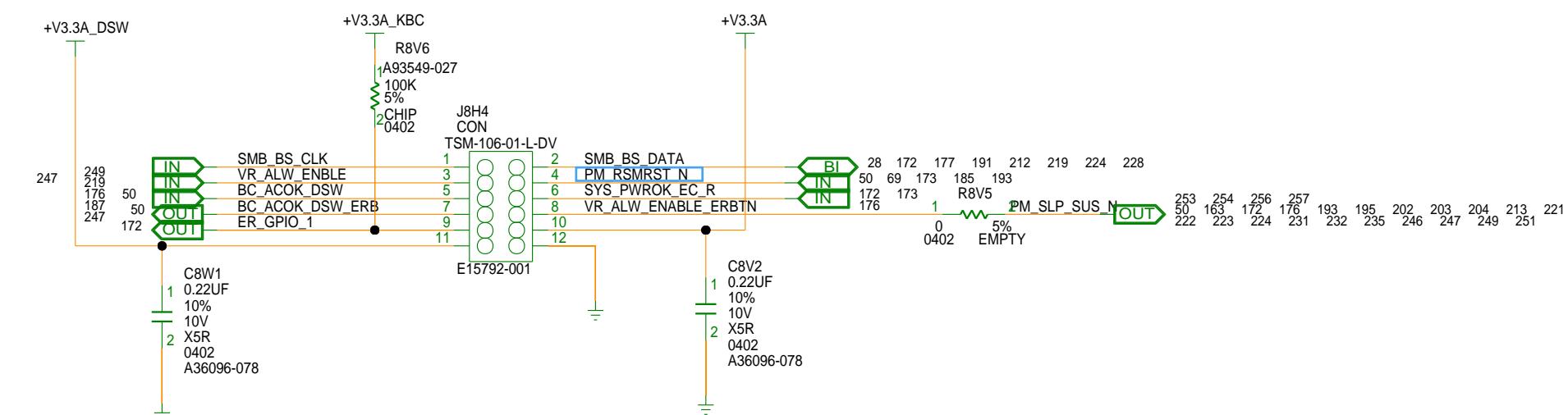


8	7	6	5	4	3	2	1
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JUMPERS FOR VALIDATION

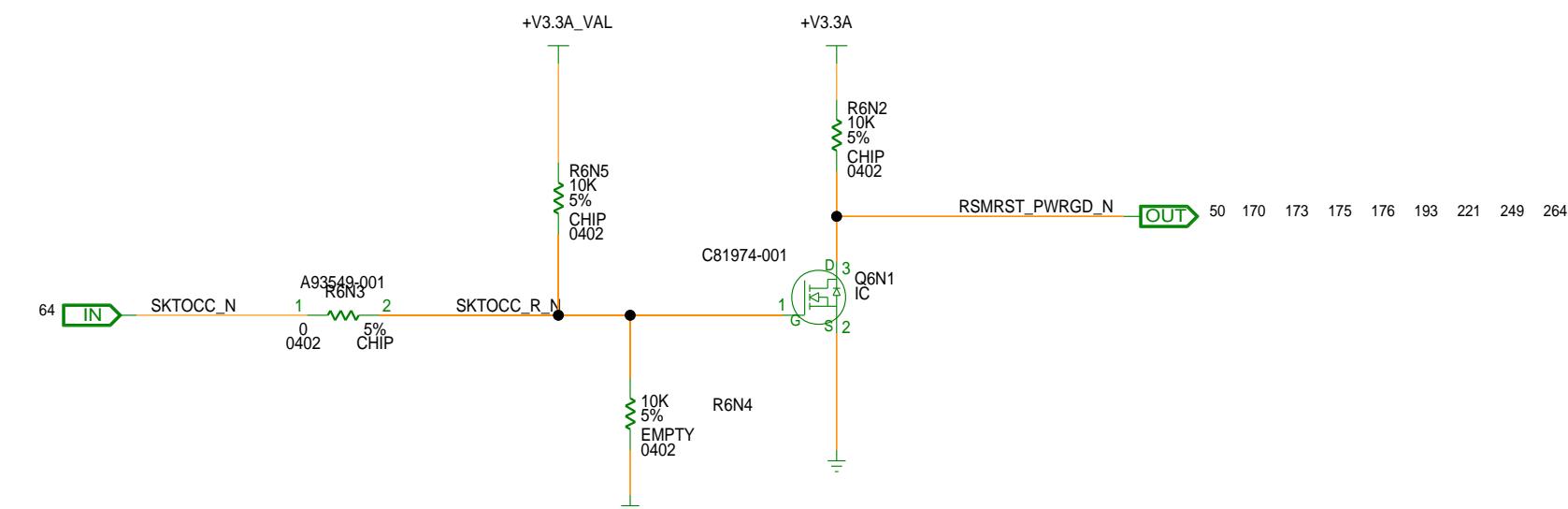


EYE RIVER VALIDATION HEADER



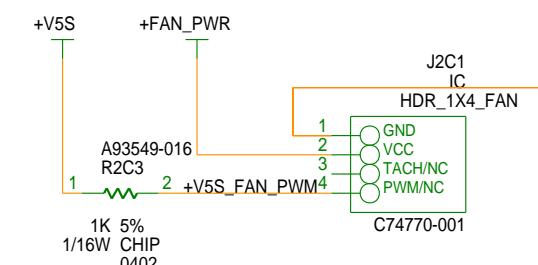
8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME		REV	DATE				

SKTOCC_N -> H_PRESENT_N (CPU DETECT,SKTOCC_N)



CONNECT TO A PROPER VSS PIN OF PCH
PROCESSOR & PCH PART DETECT

FAN HEADER



DESIGN NOTE:

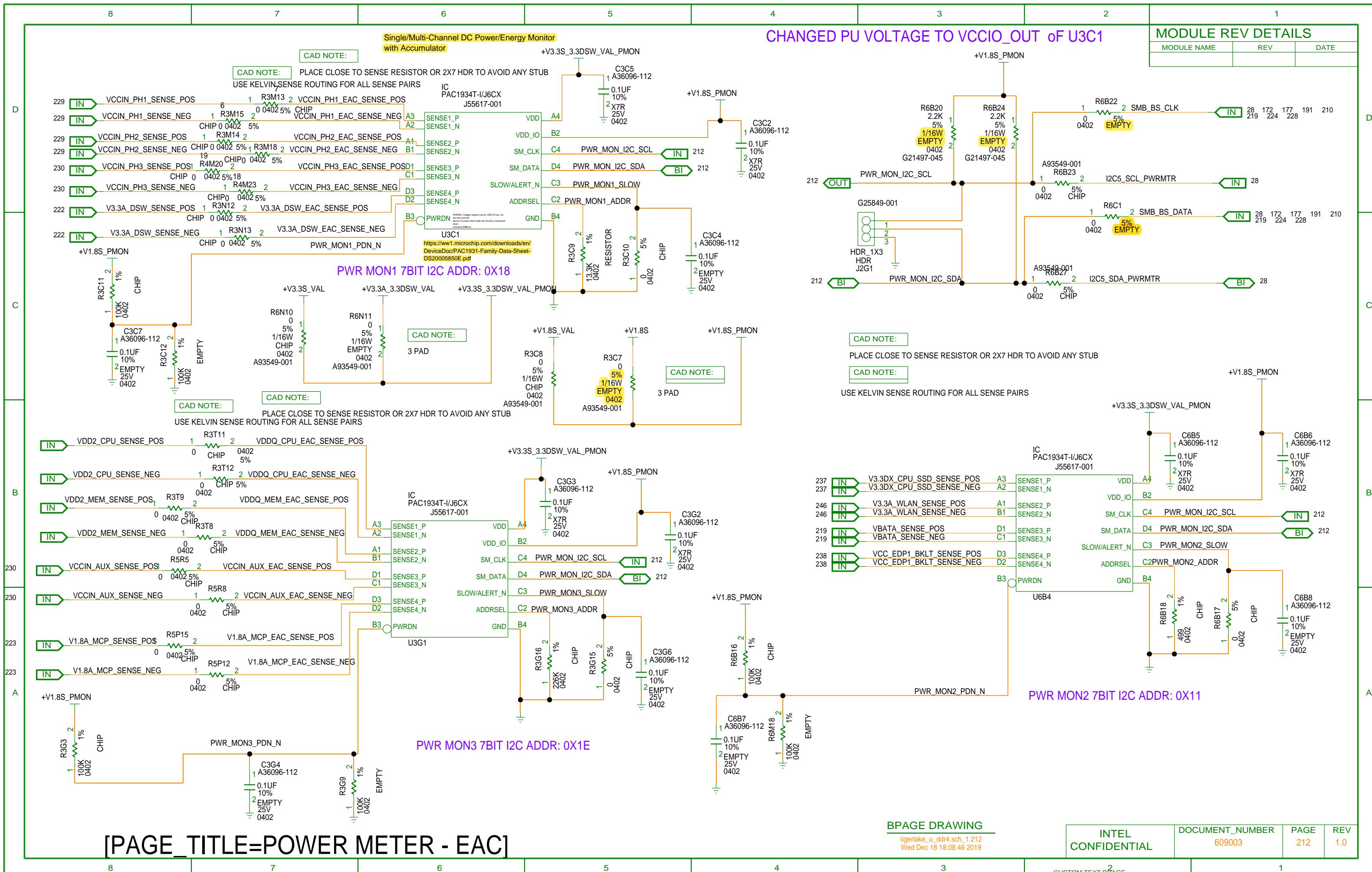
J2A4 FAN CONNECTOR ON & STANDBY(S3)

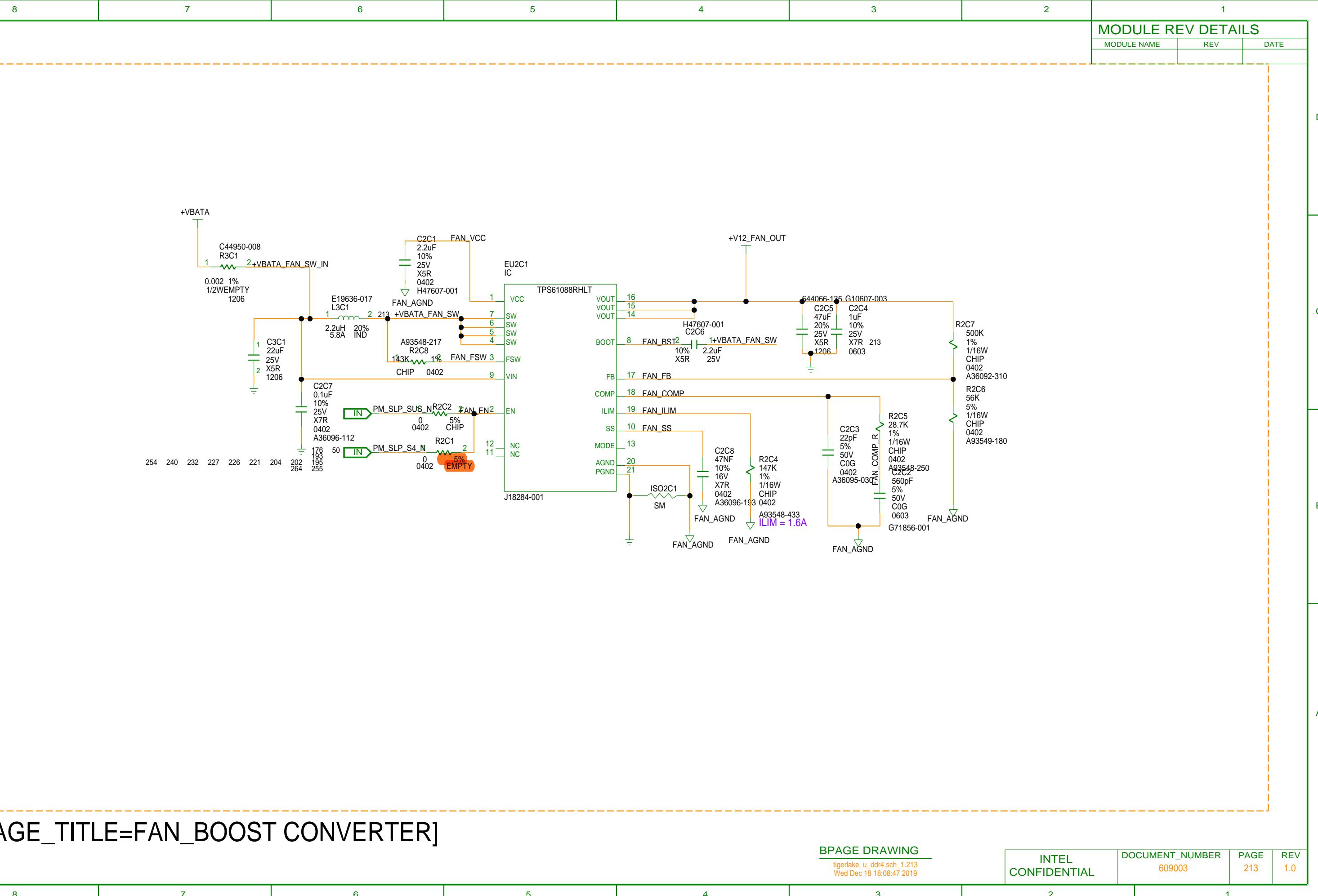
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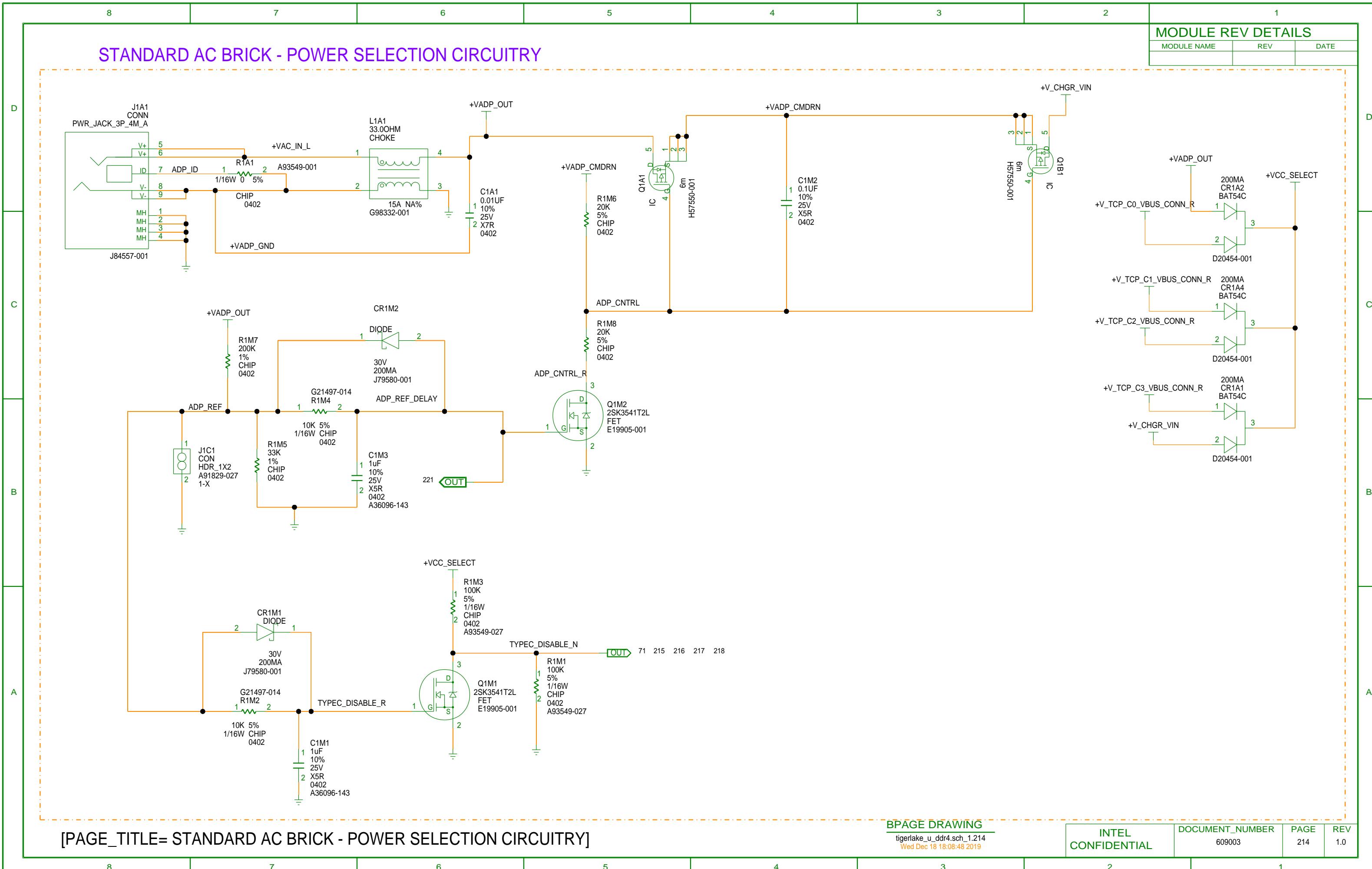
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tigerlake_u_ddr4.sch_1.211
Wed Dec 18 18:08:45 2019

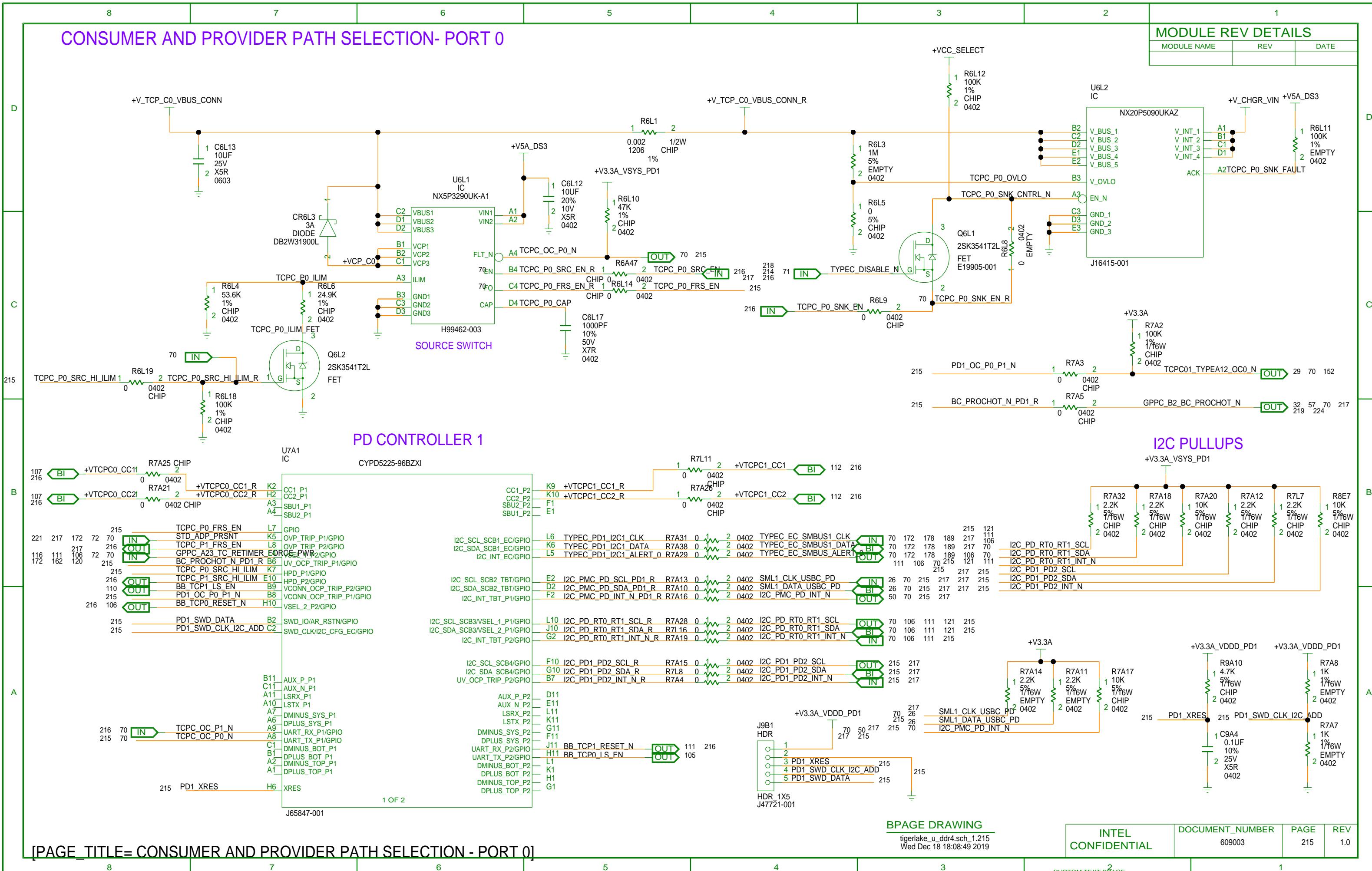
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 211	REV 1.0
CUSTOM TEXT 2 PAGE			1

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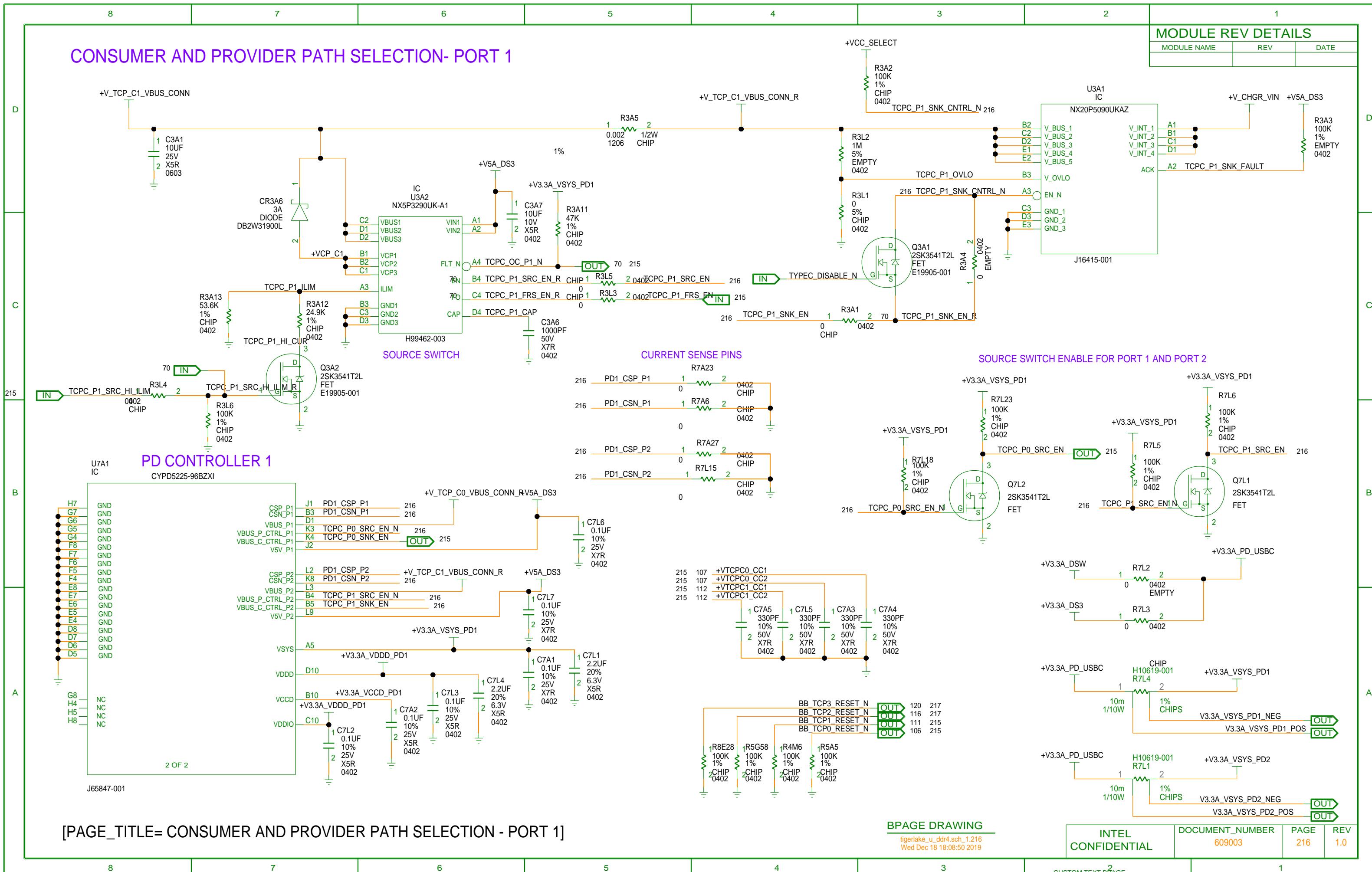


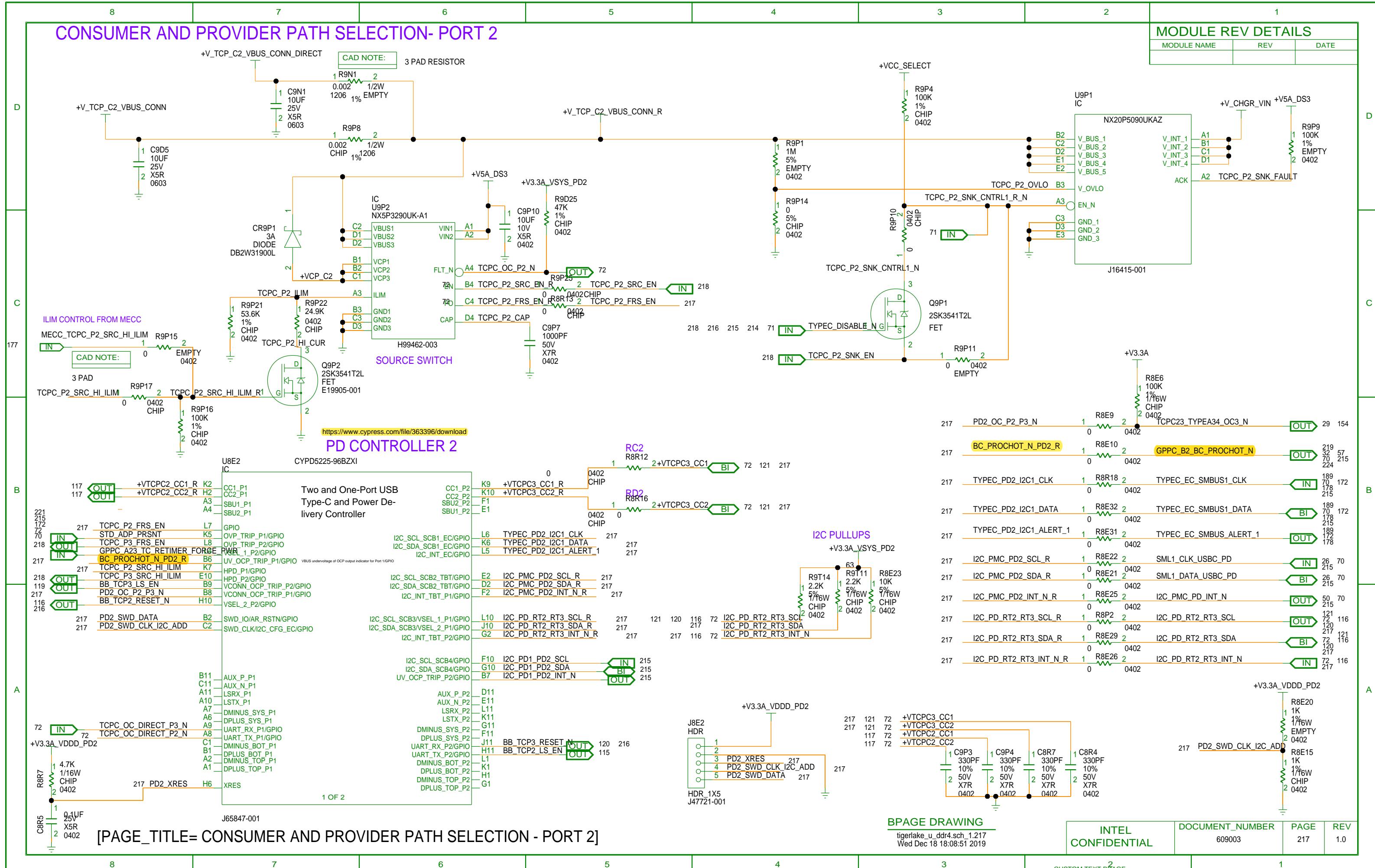


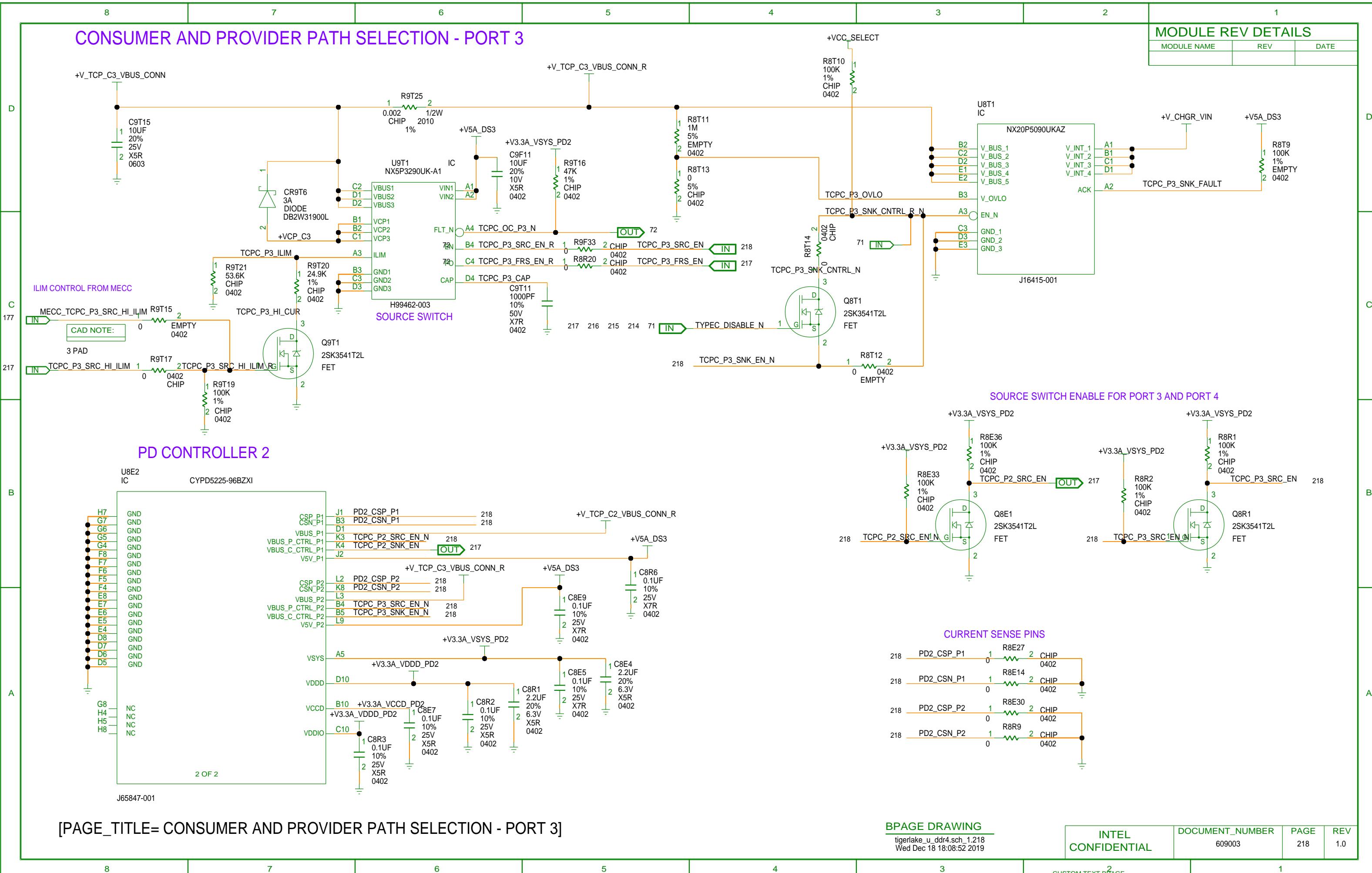
CONSUMER AND PROVIDER PATH SELECTION- PORT 1

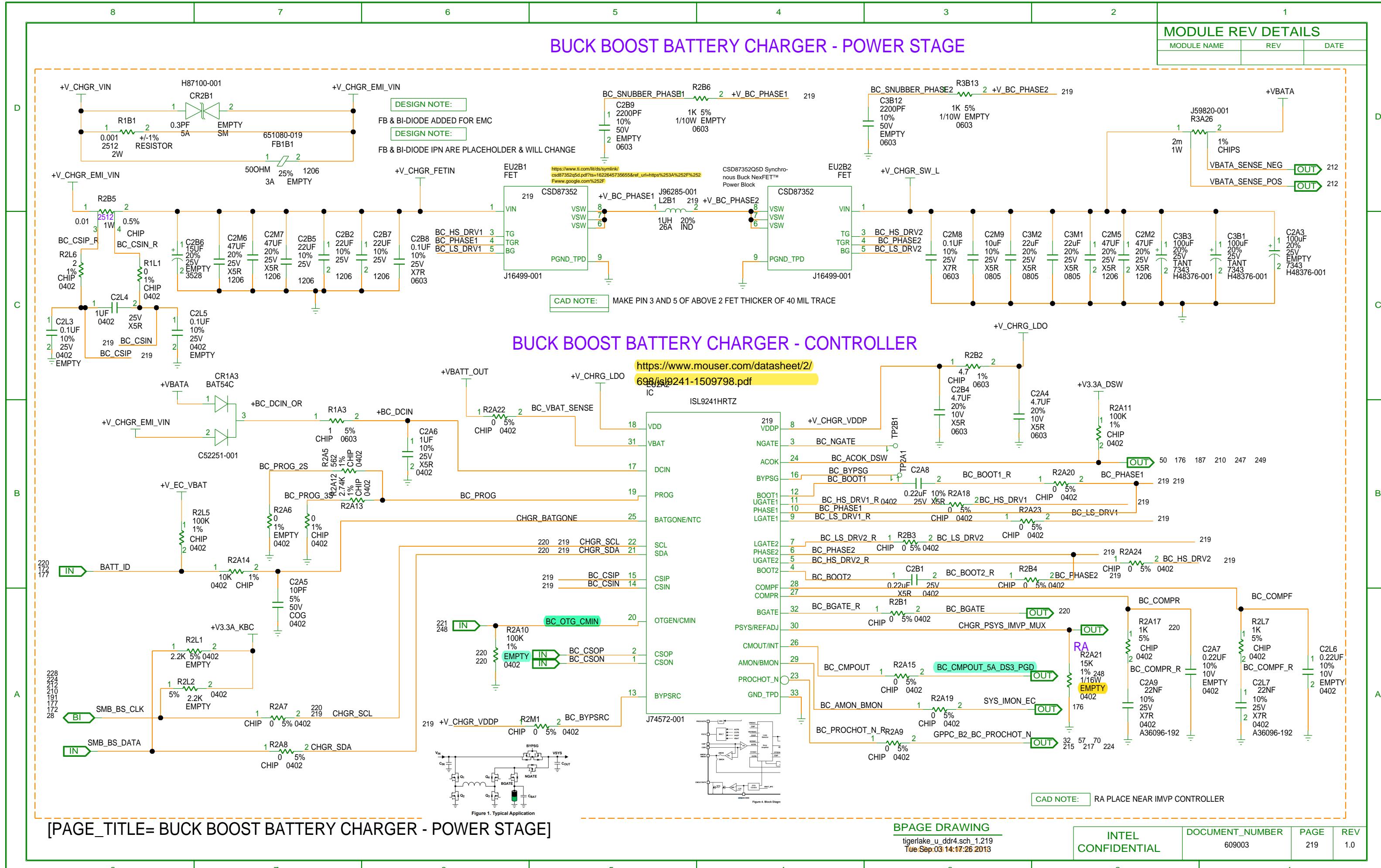
MODULE REV DETAILS

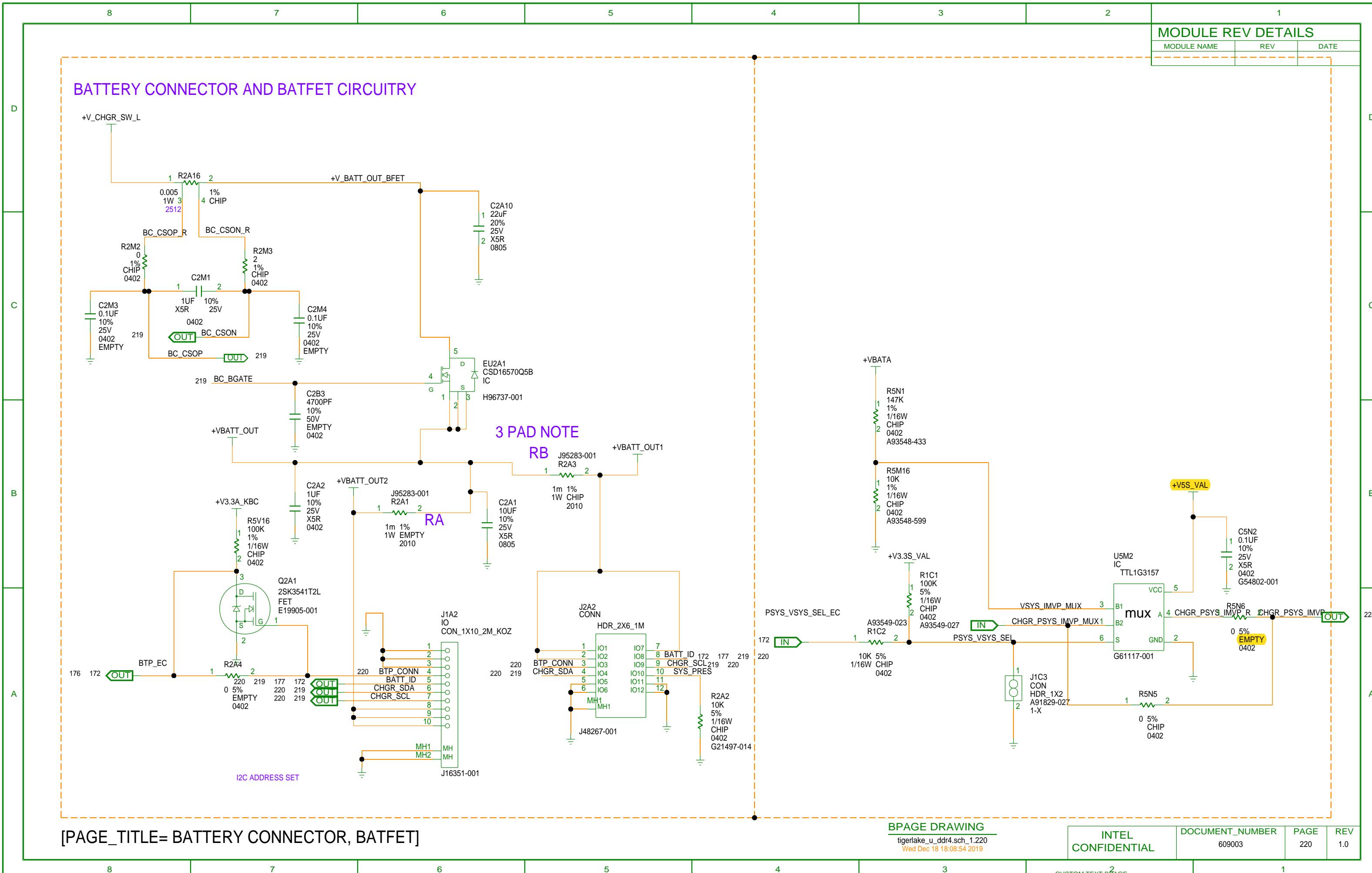
MODULE NAME	REV	DATE

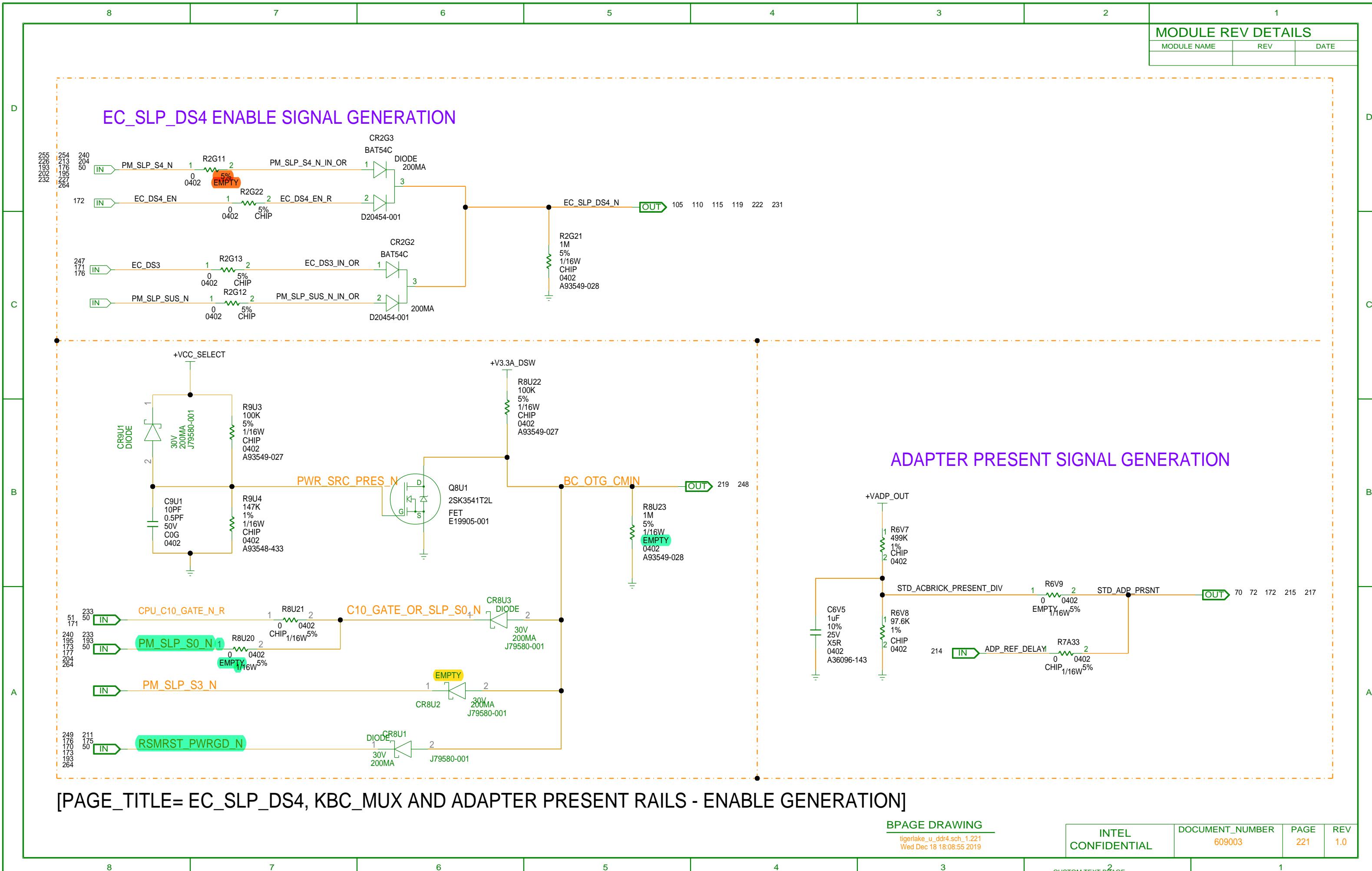


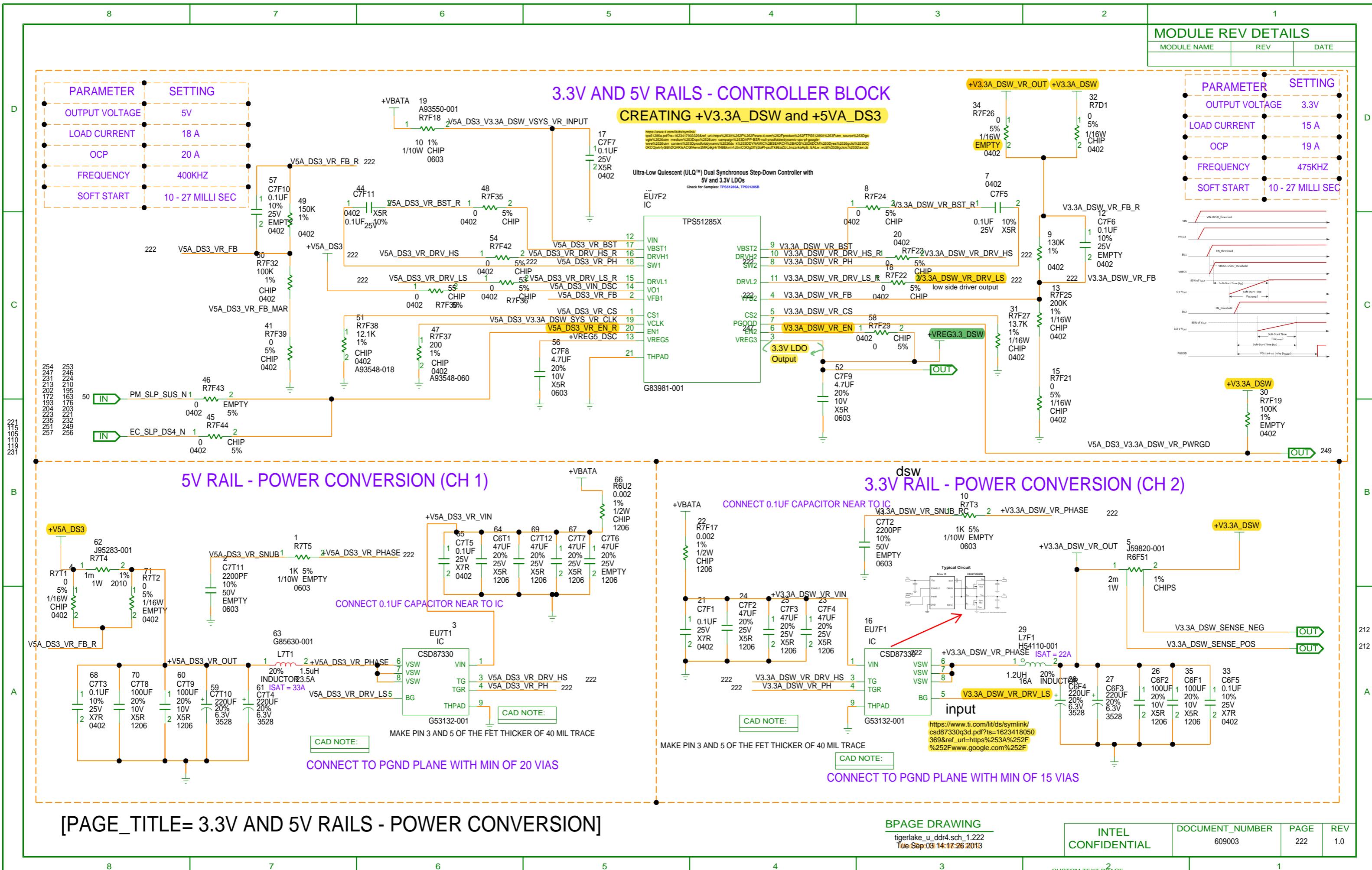


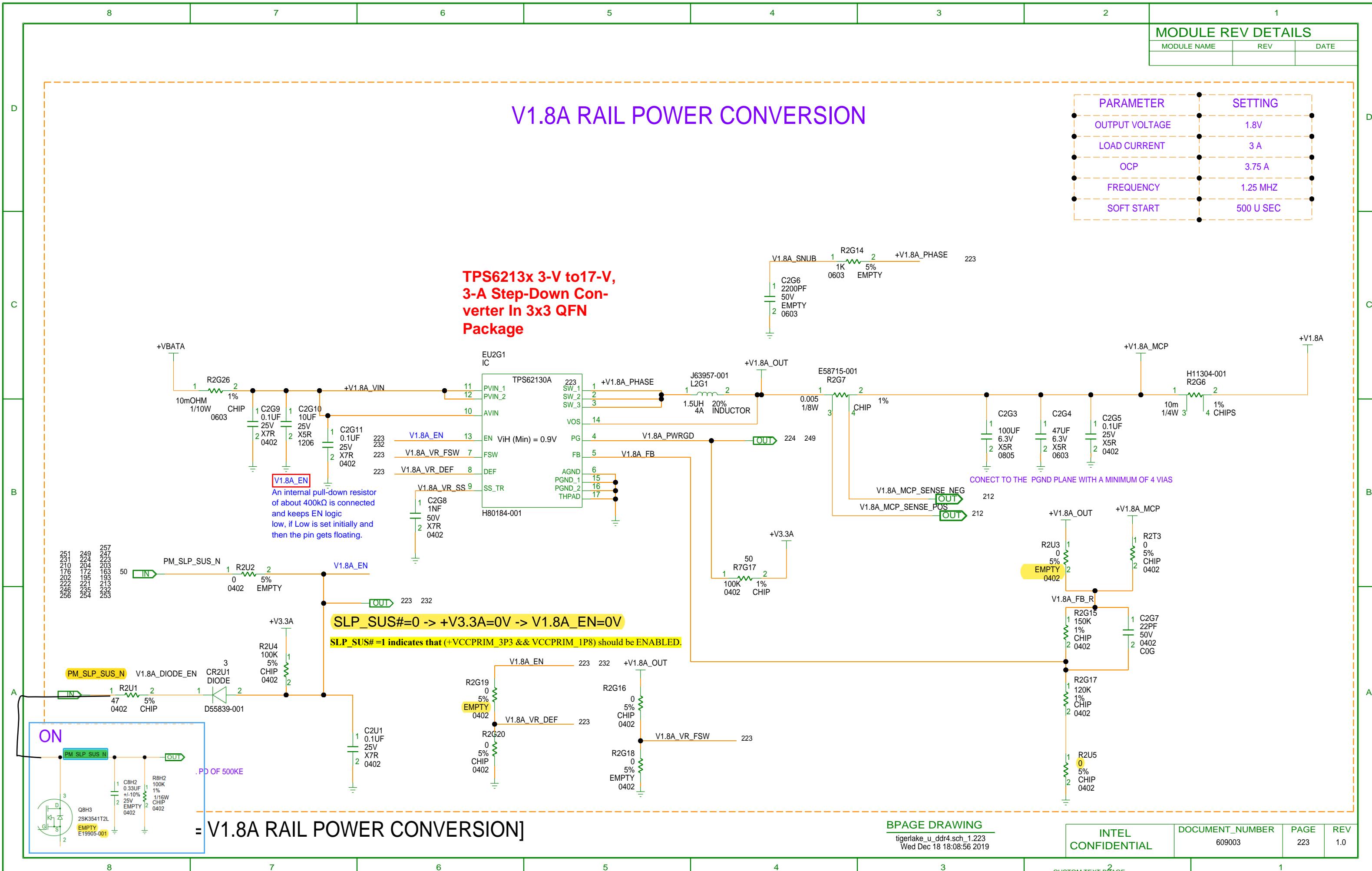


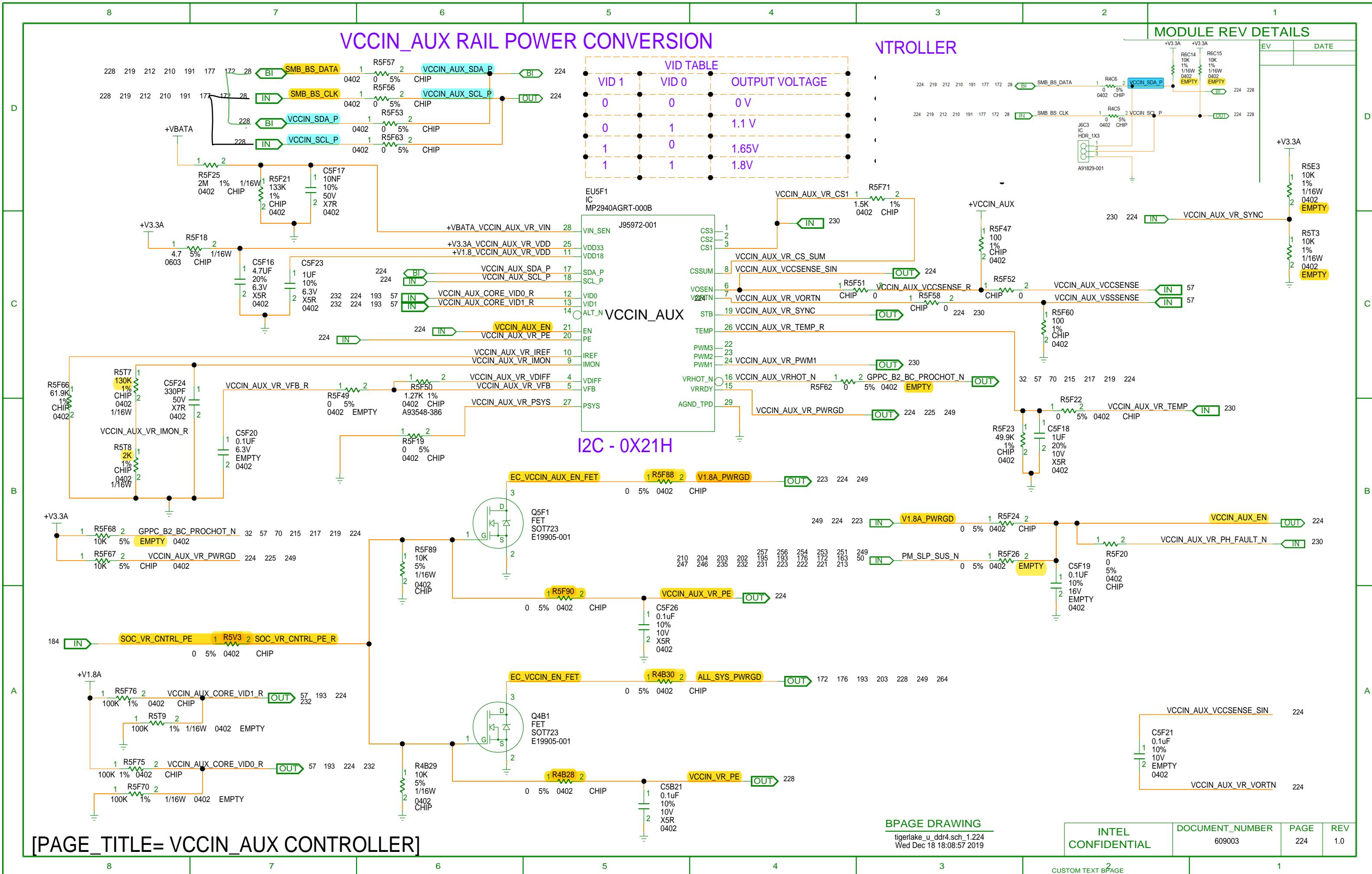


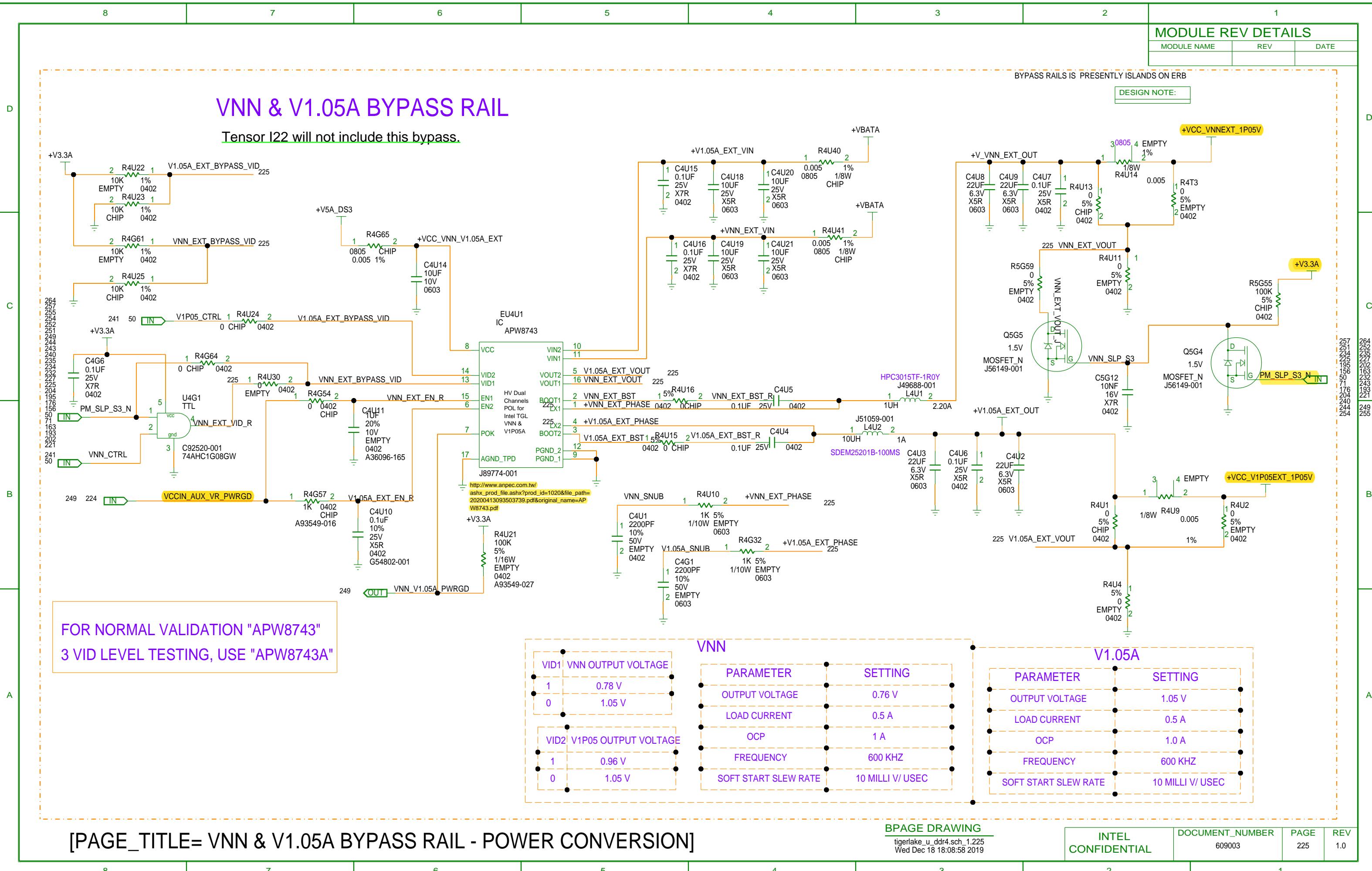


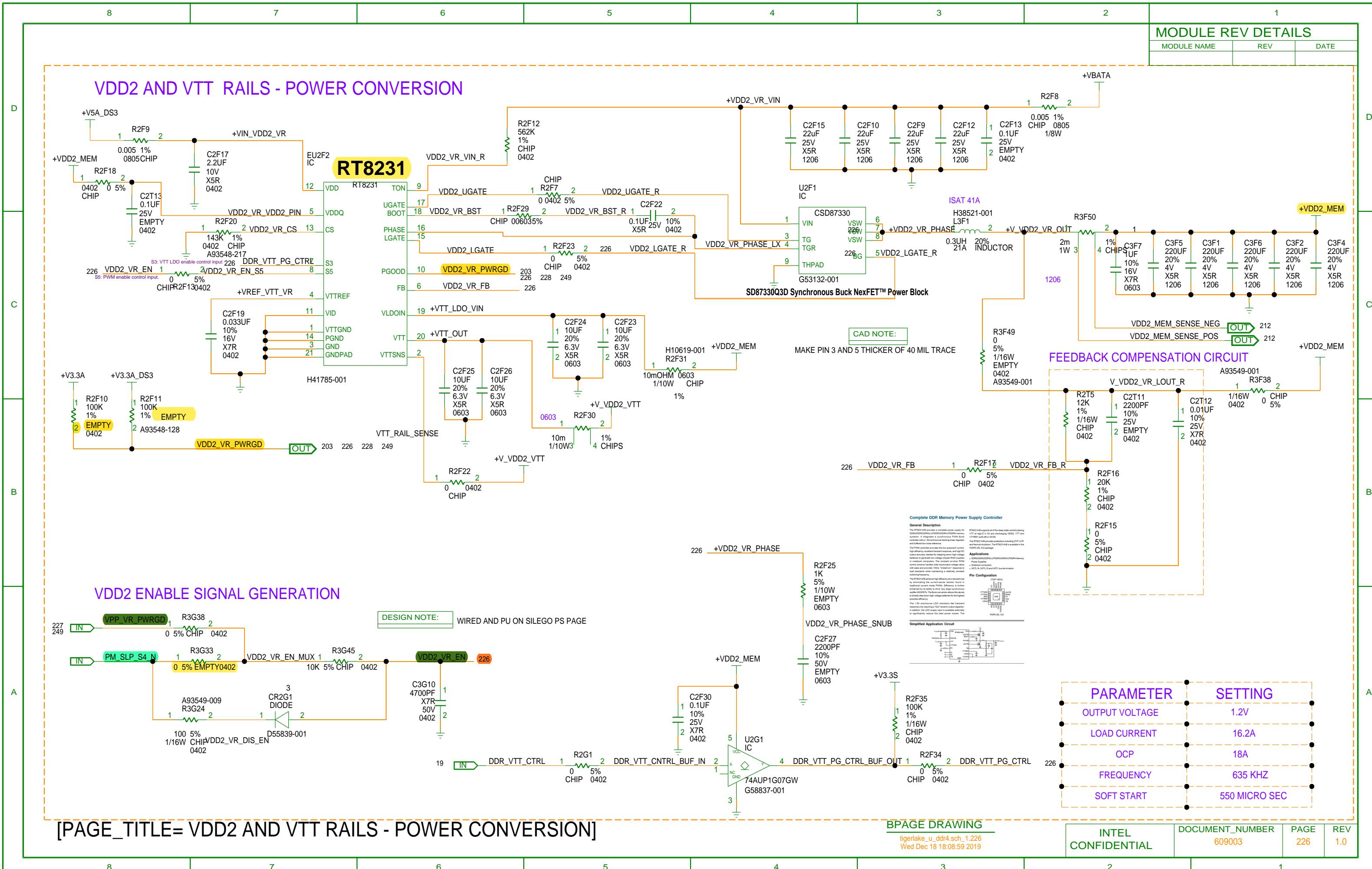


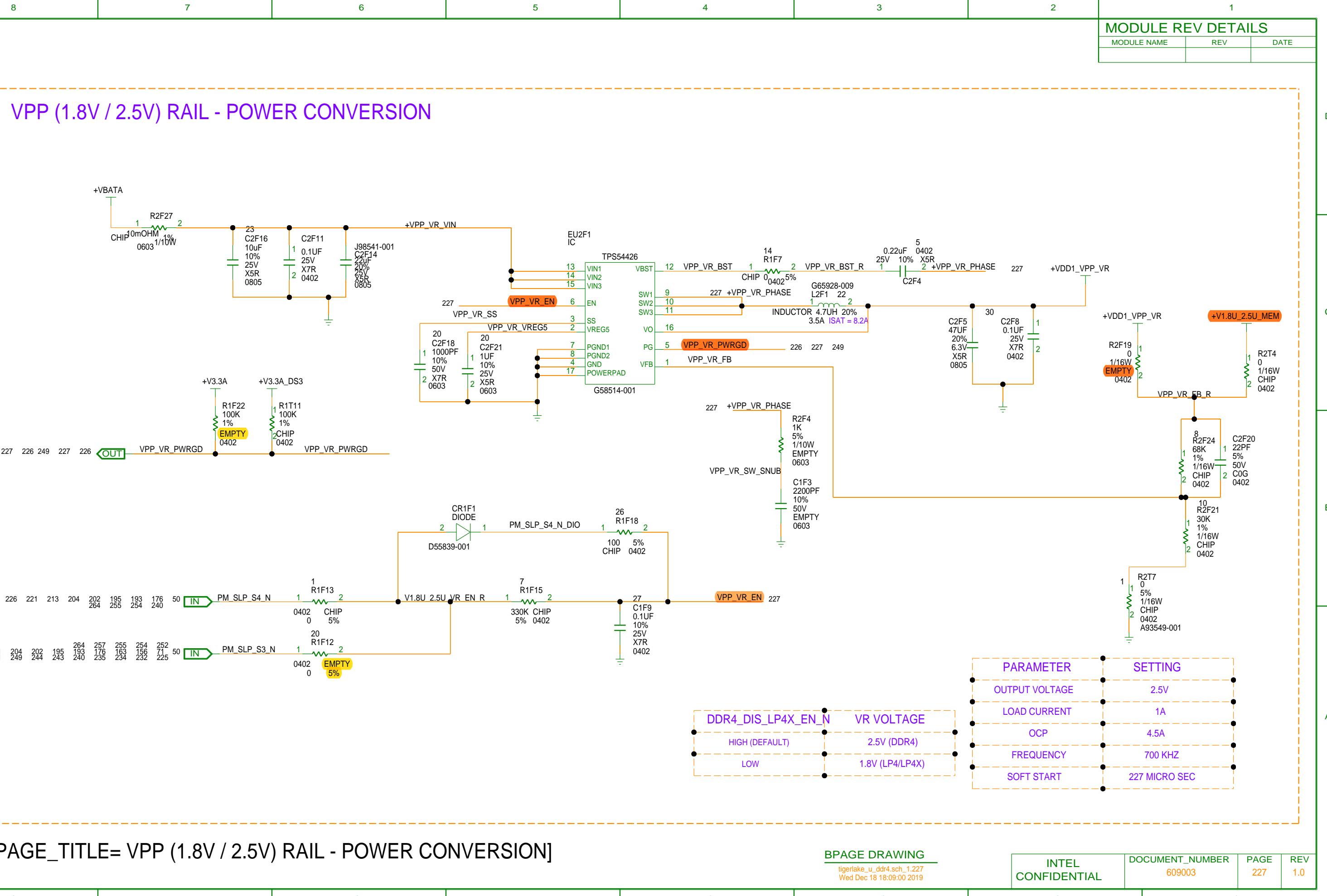


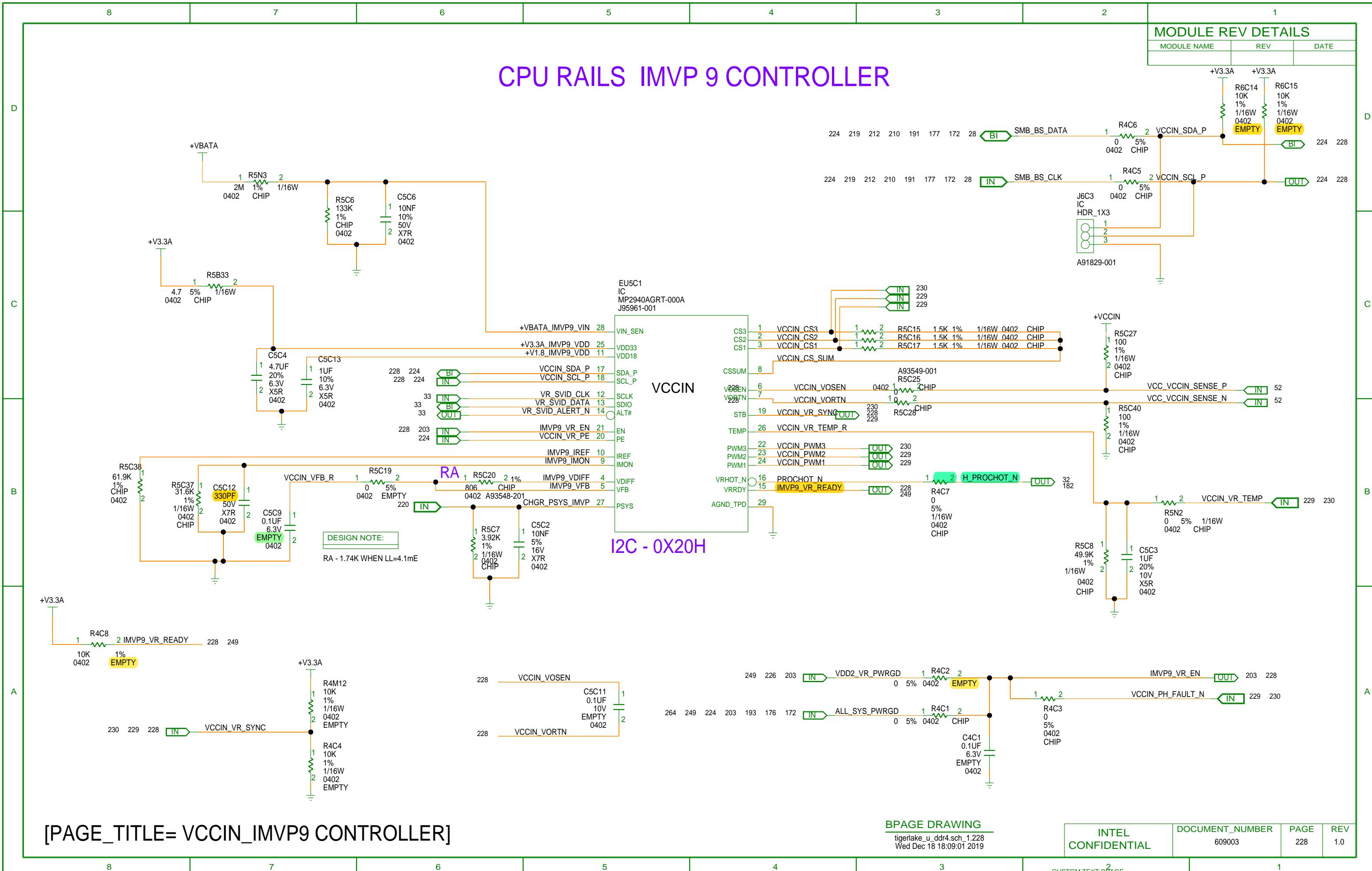


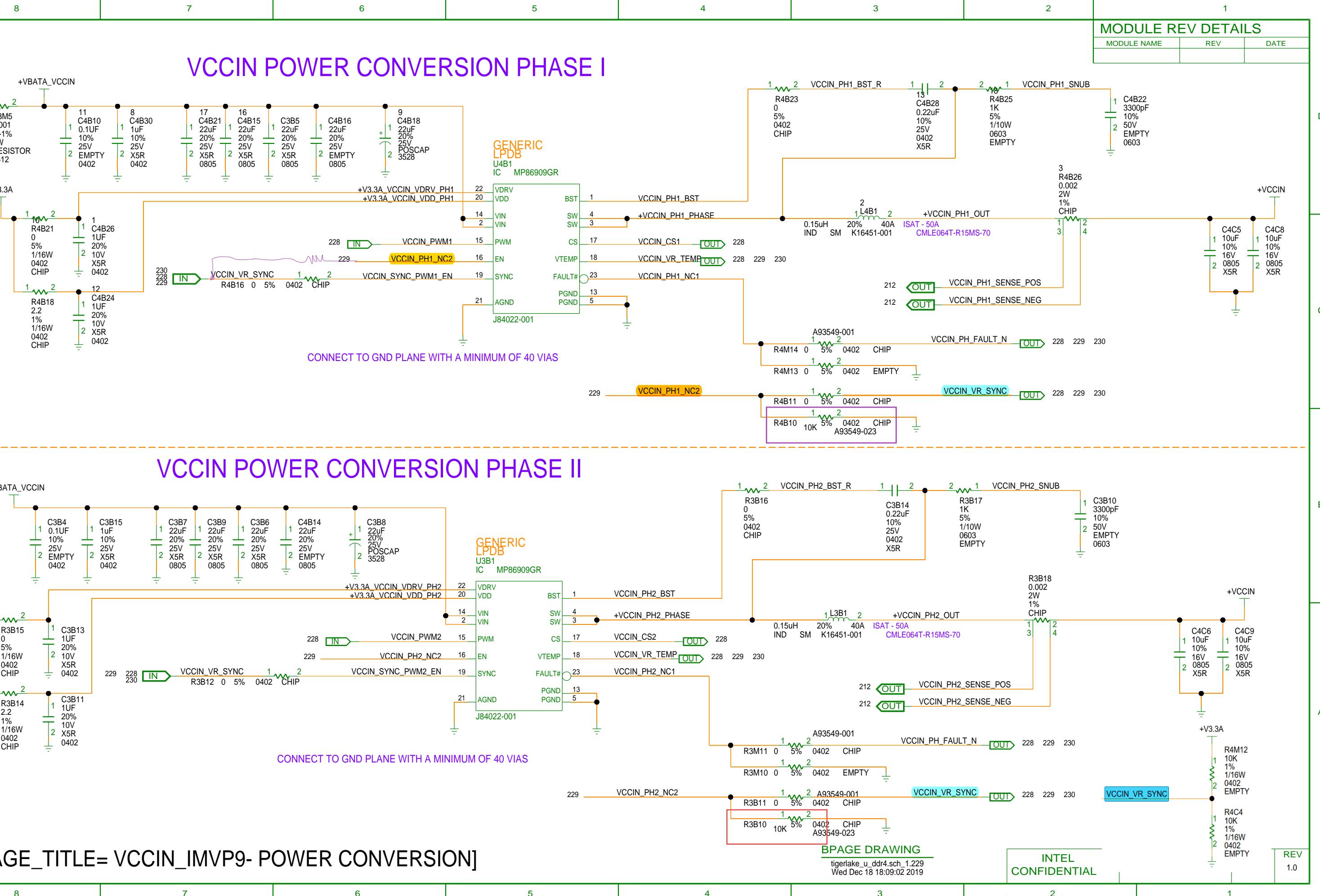








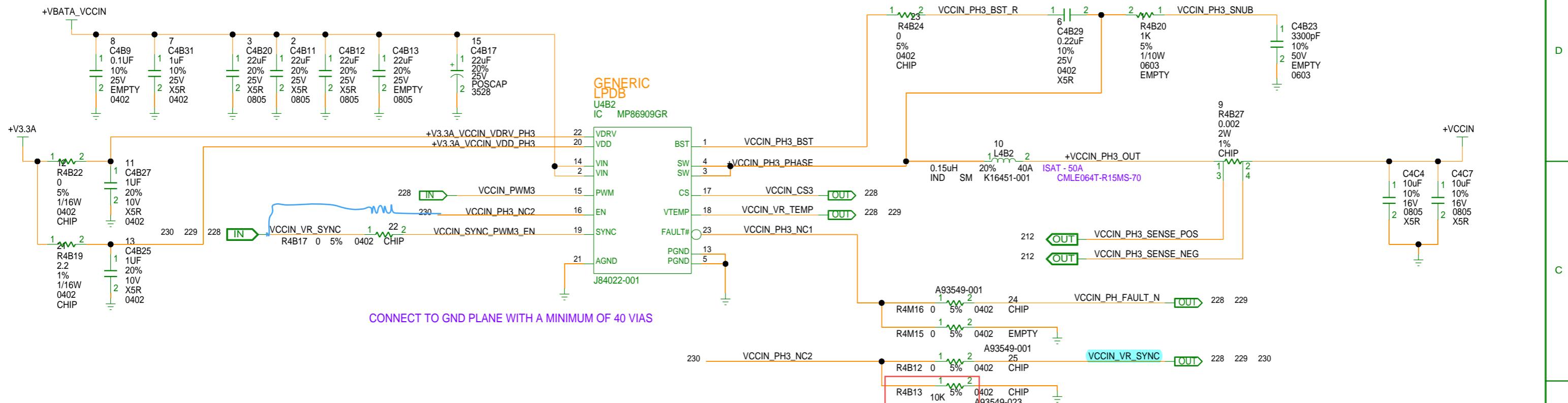




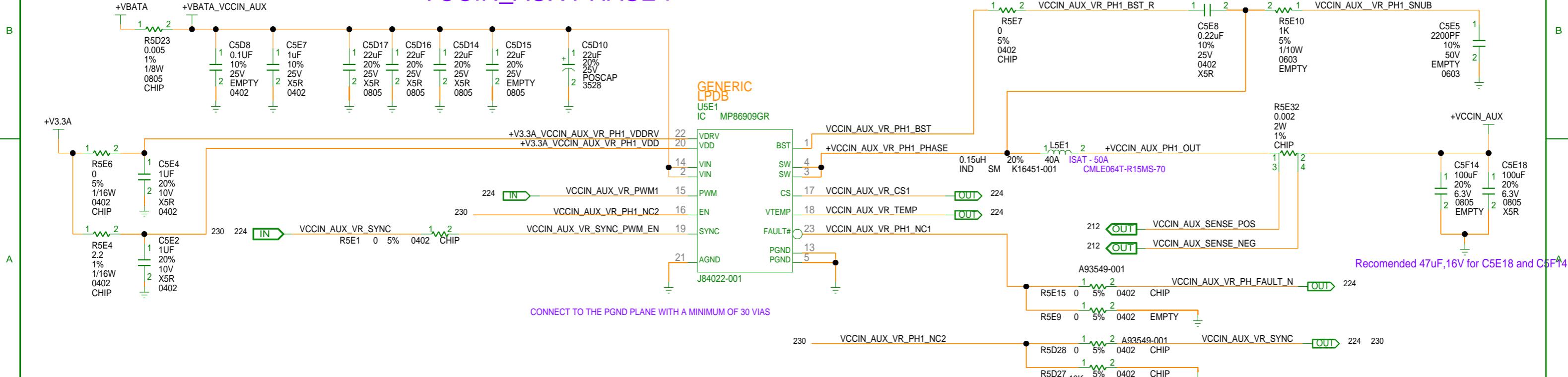
VCCIN POWER CONVERSION PHASE III

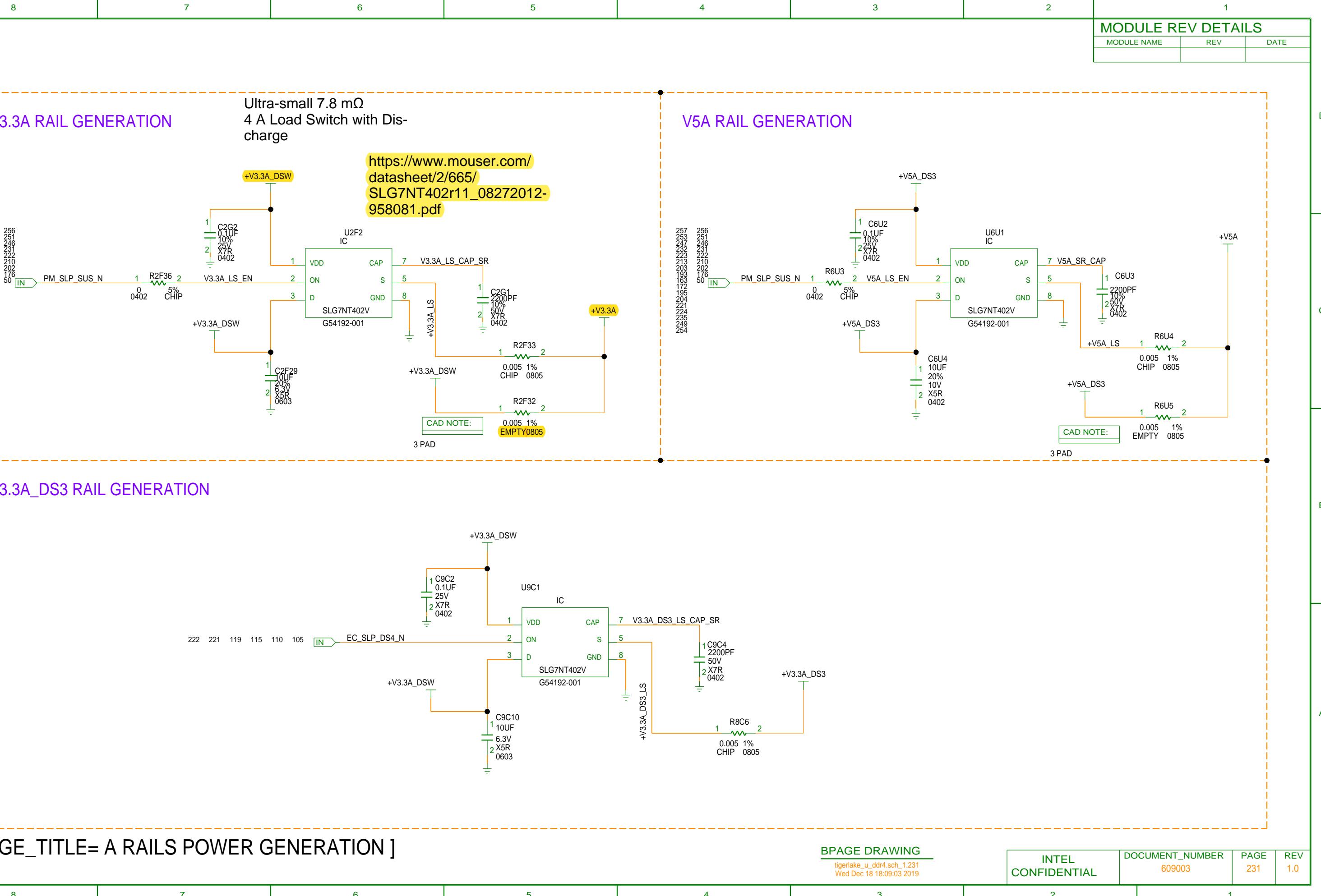
MODULE REV DETAILS

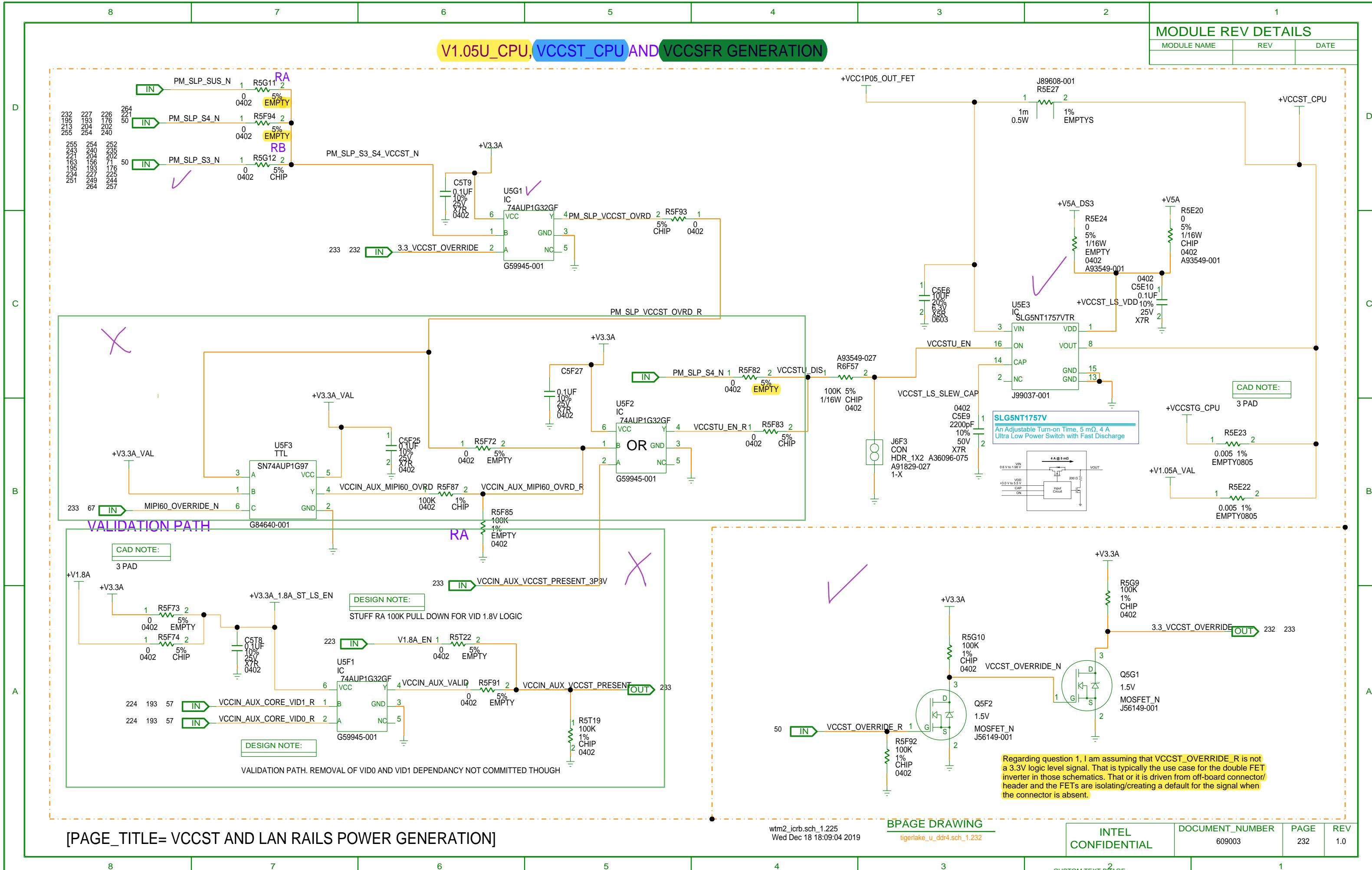
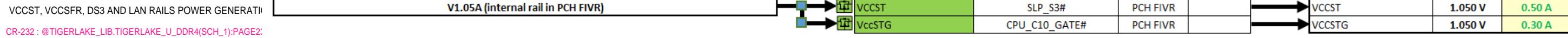
MODULE NAME	REV	DATE

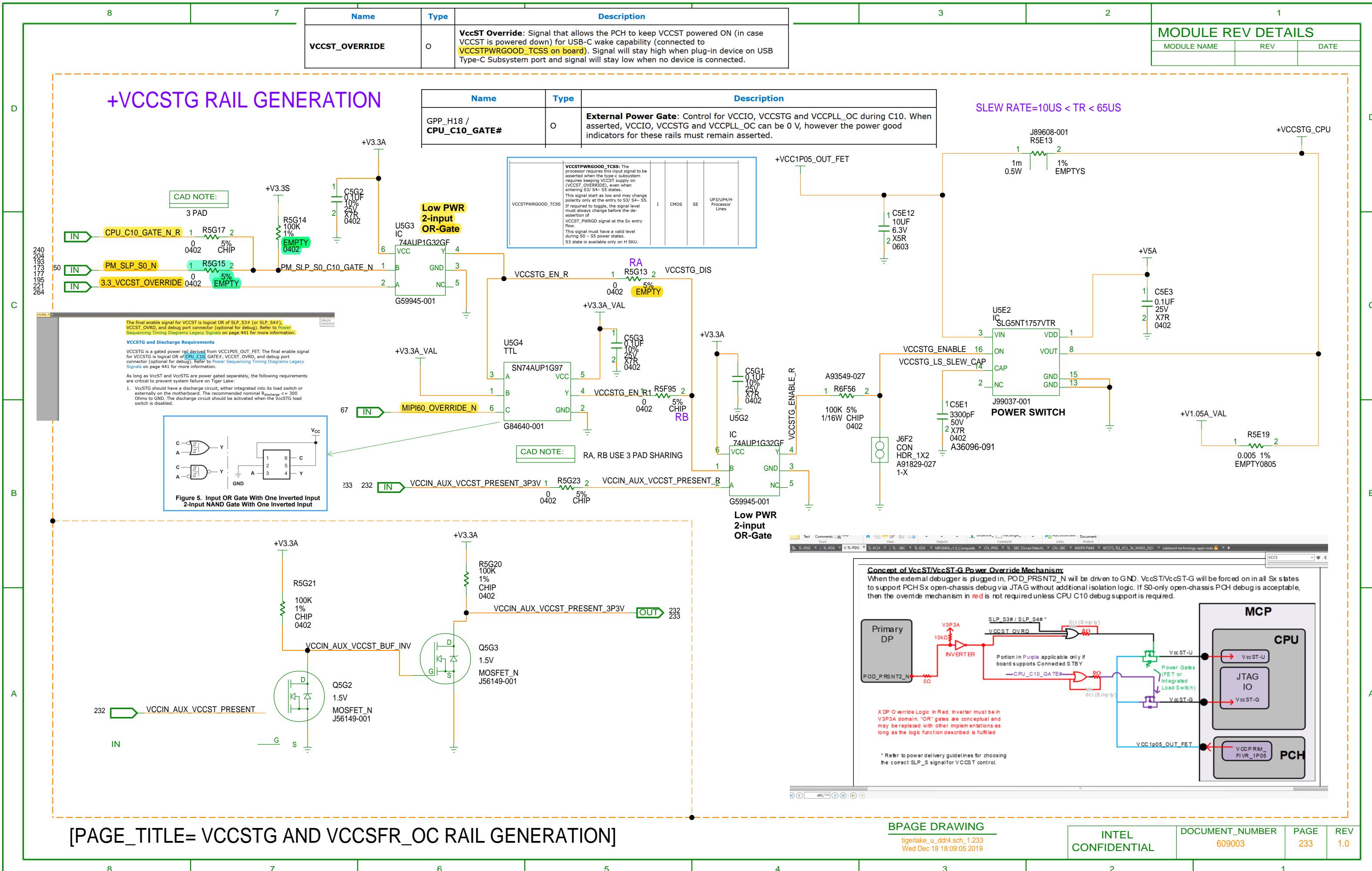


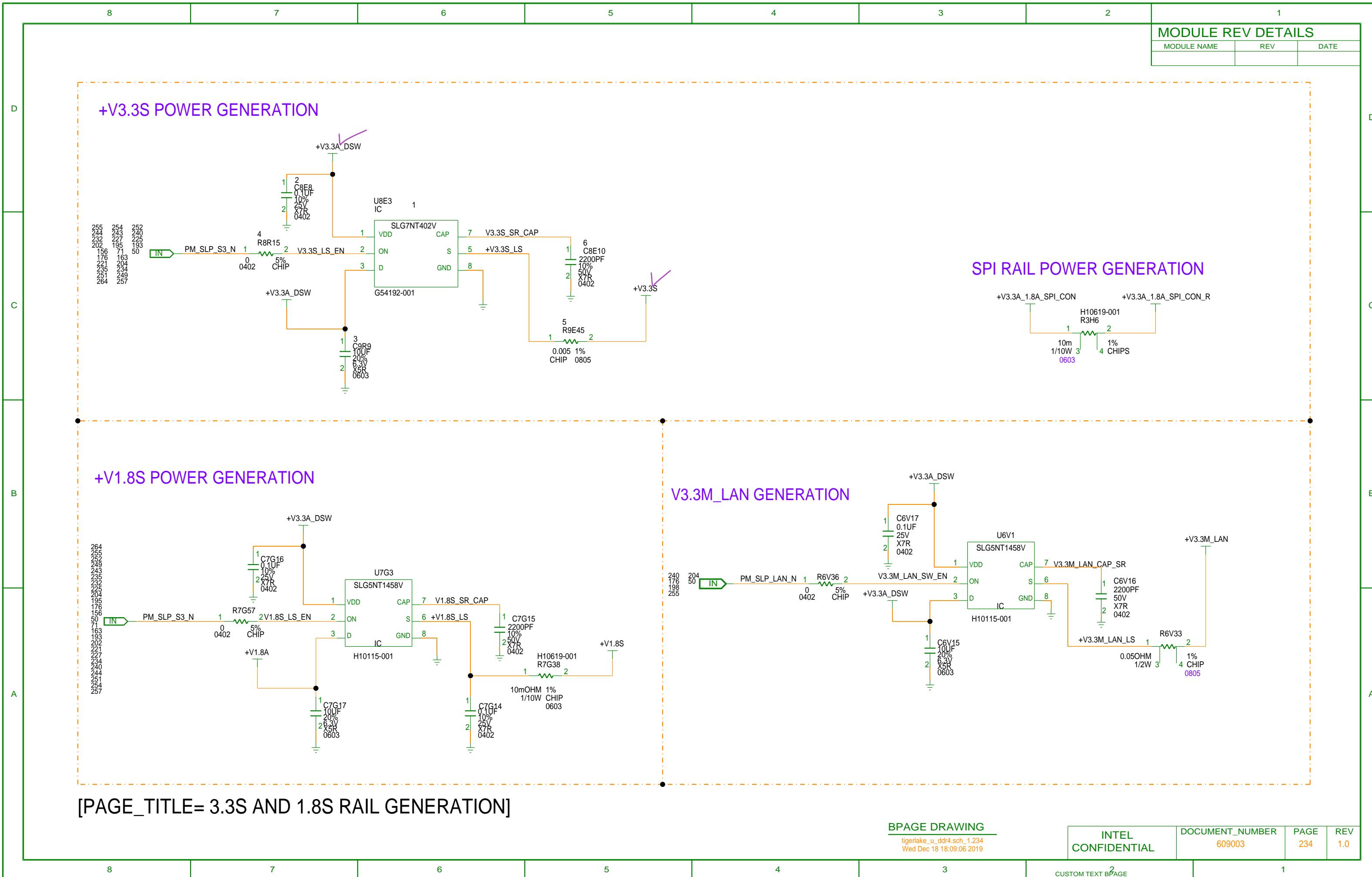
VCCIN_AUX PHASE I







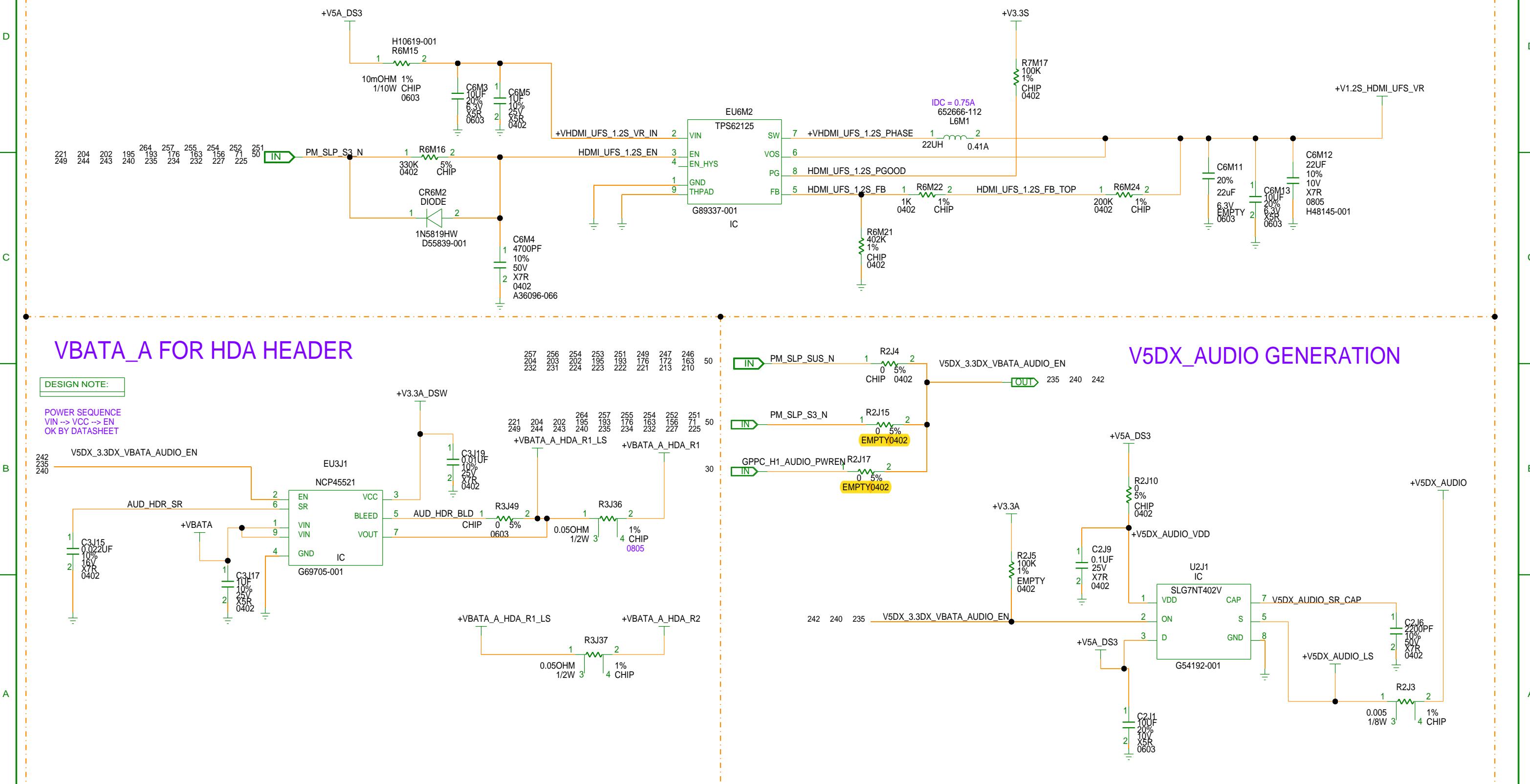




1.2V RAIL FOR HDMI AND UFS - POWER CONVERSION

MODULE REV DETAILS

MODULE NAME	REV	DATE



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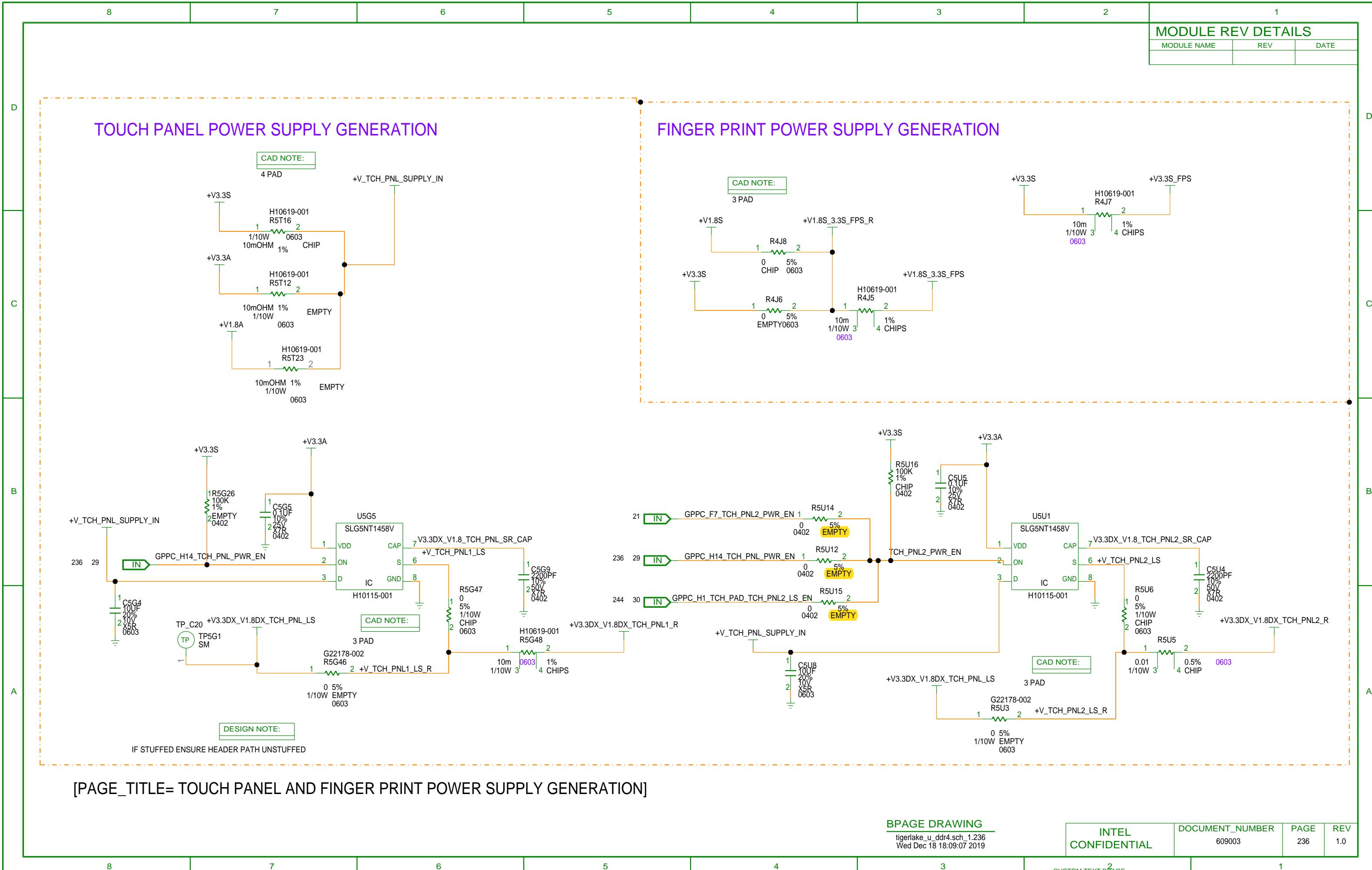
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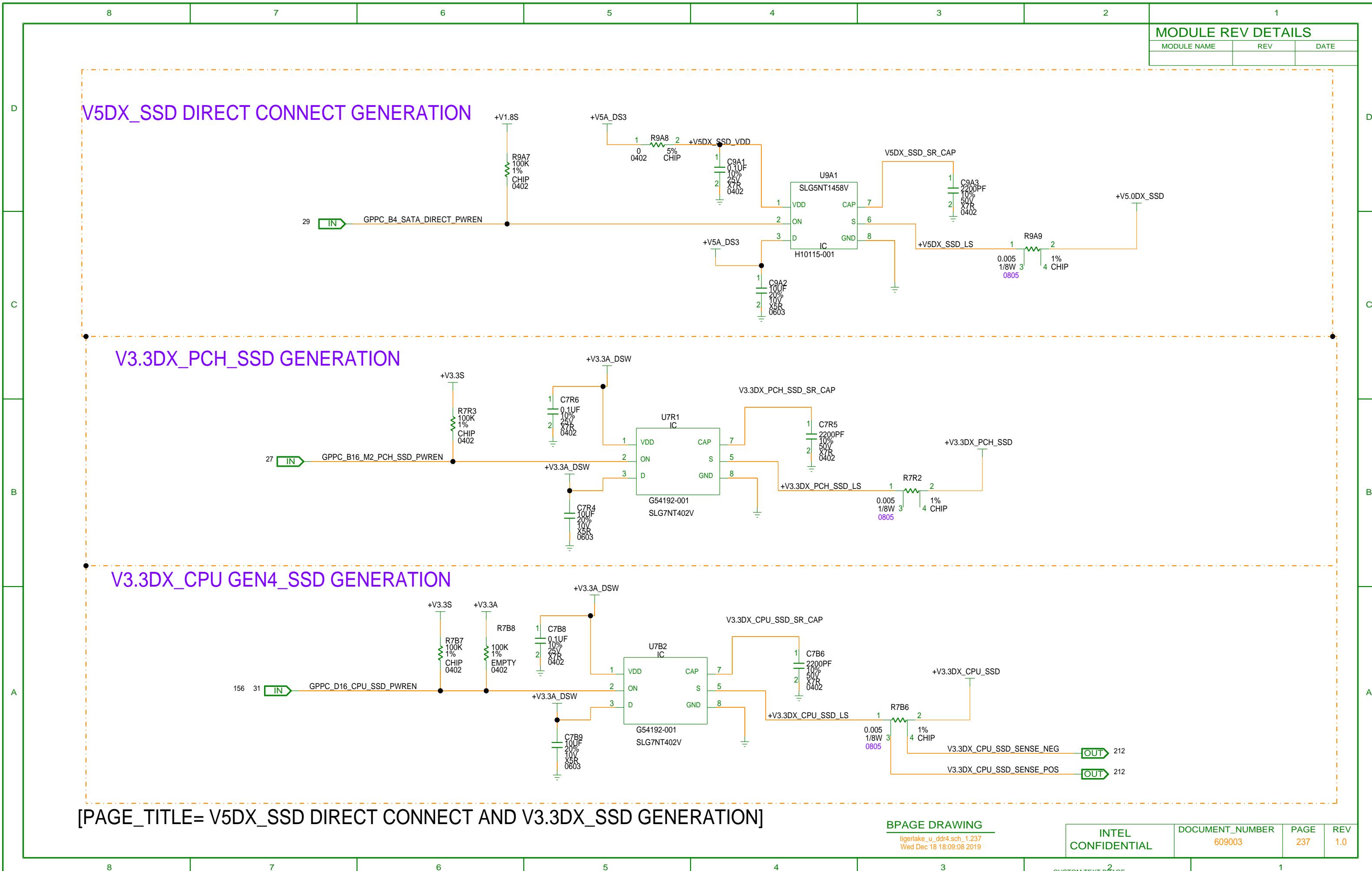
tigerlake_u_ddr4.sch_1.235
Wed Dec 18 18:09:07 2019

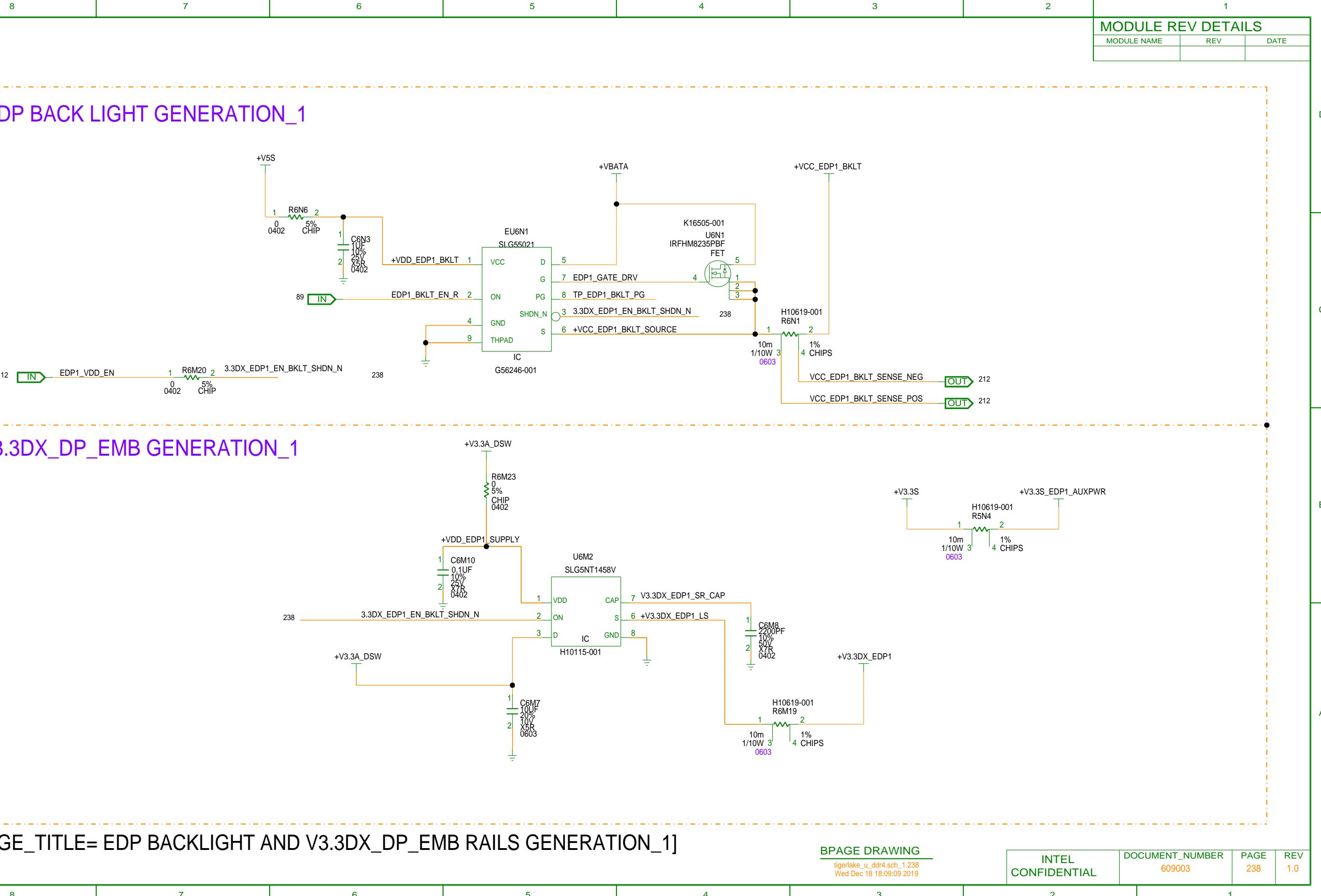
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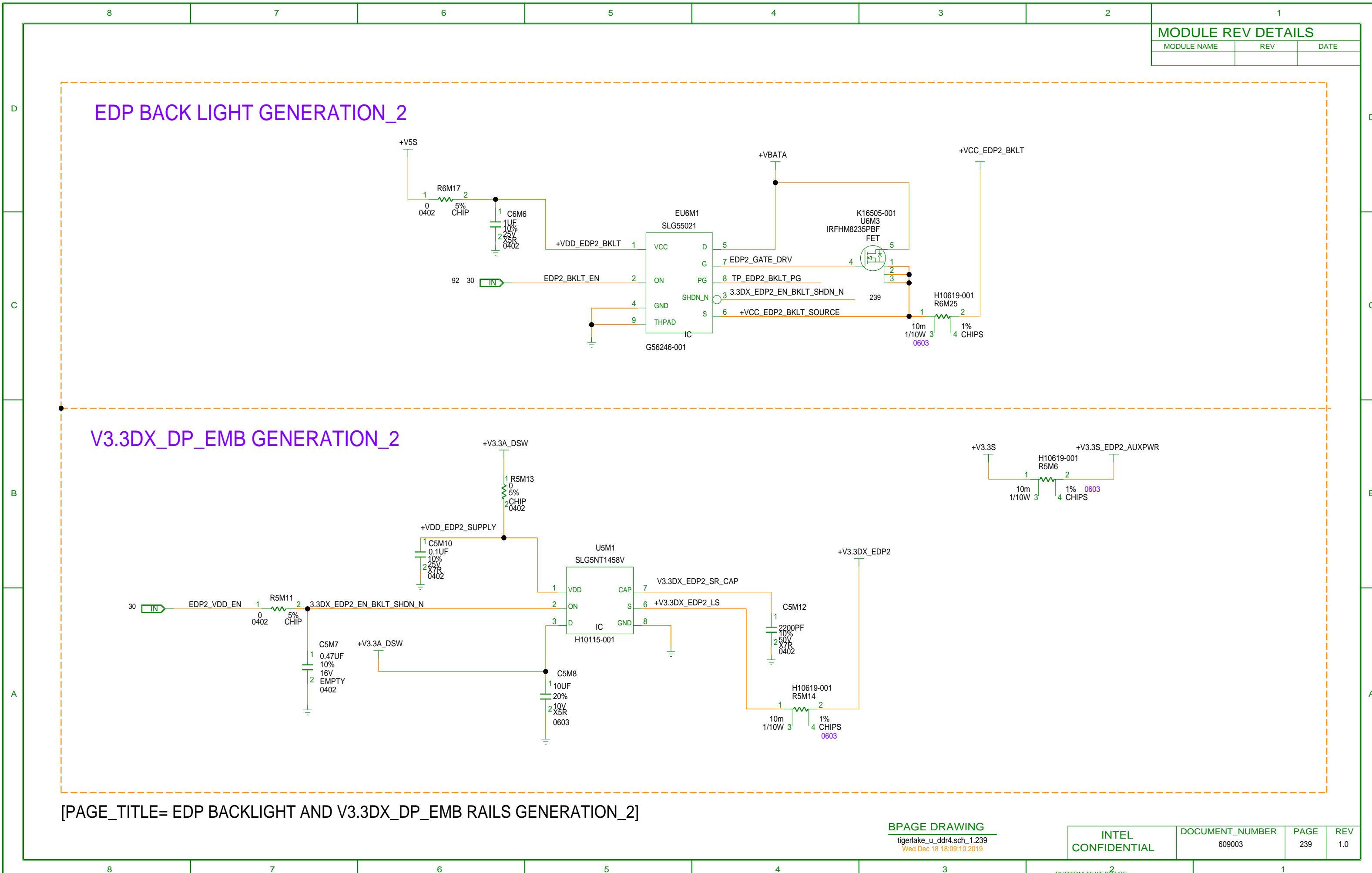
CUSTOM TEXT BPAGE

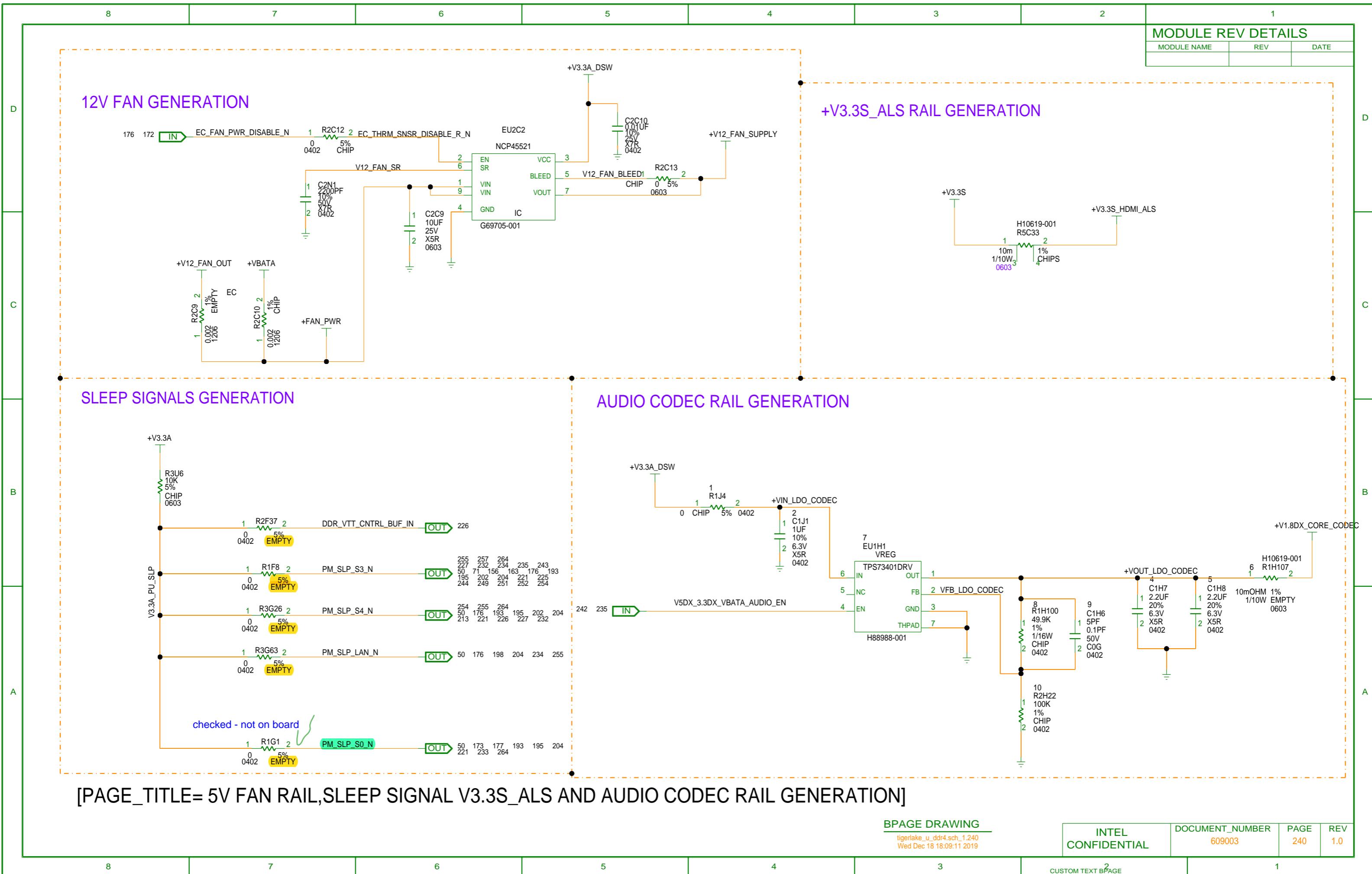
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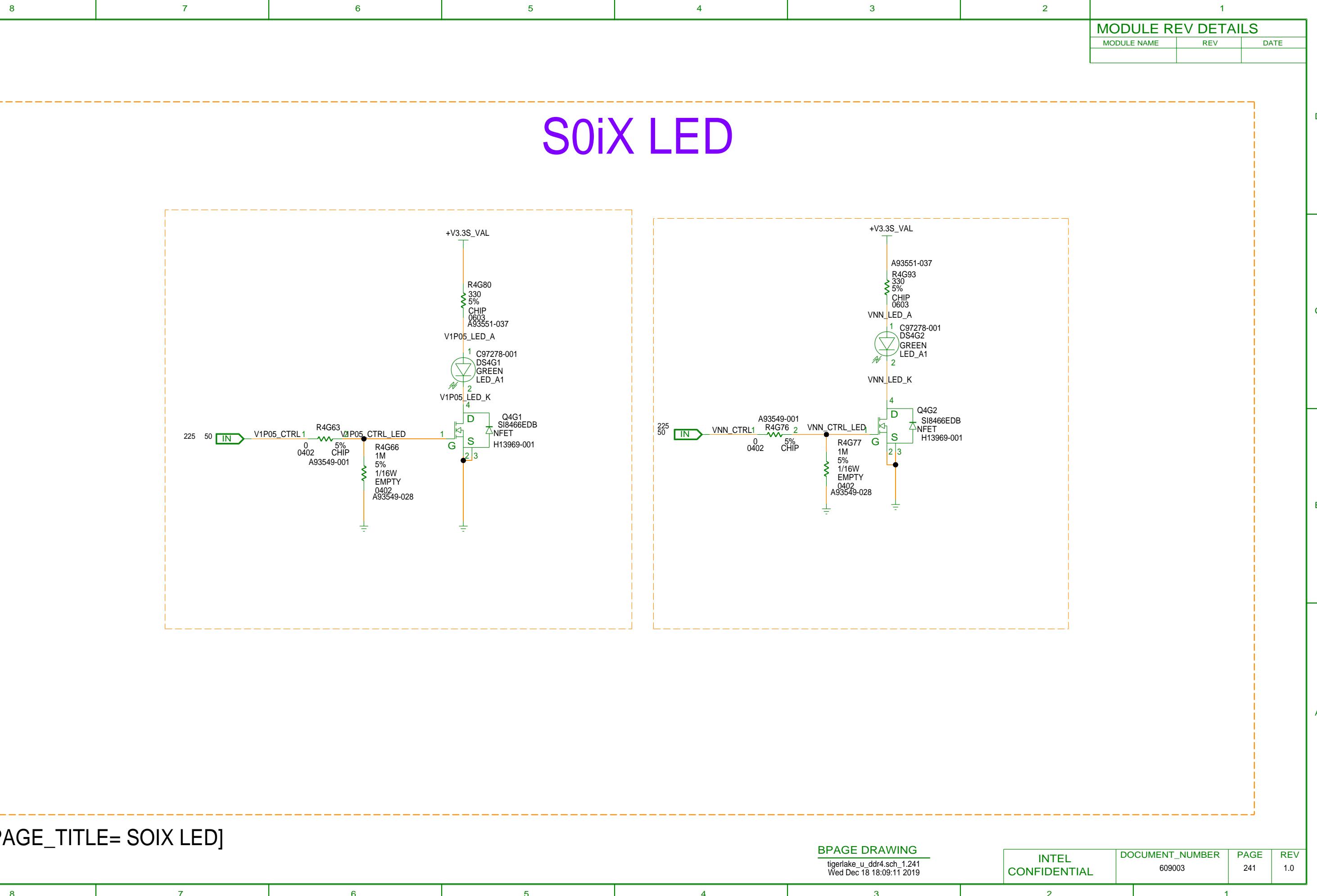


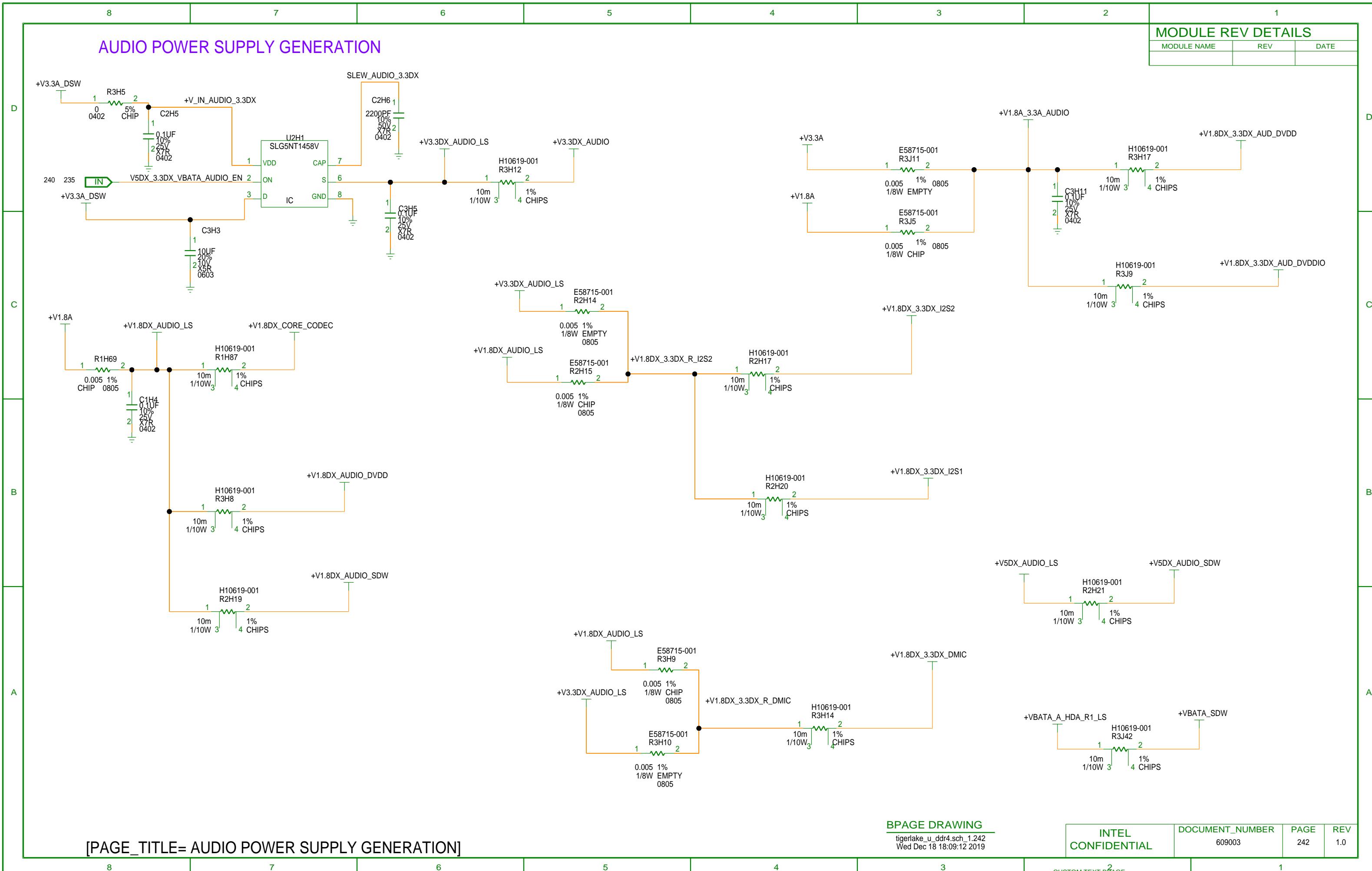


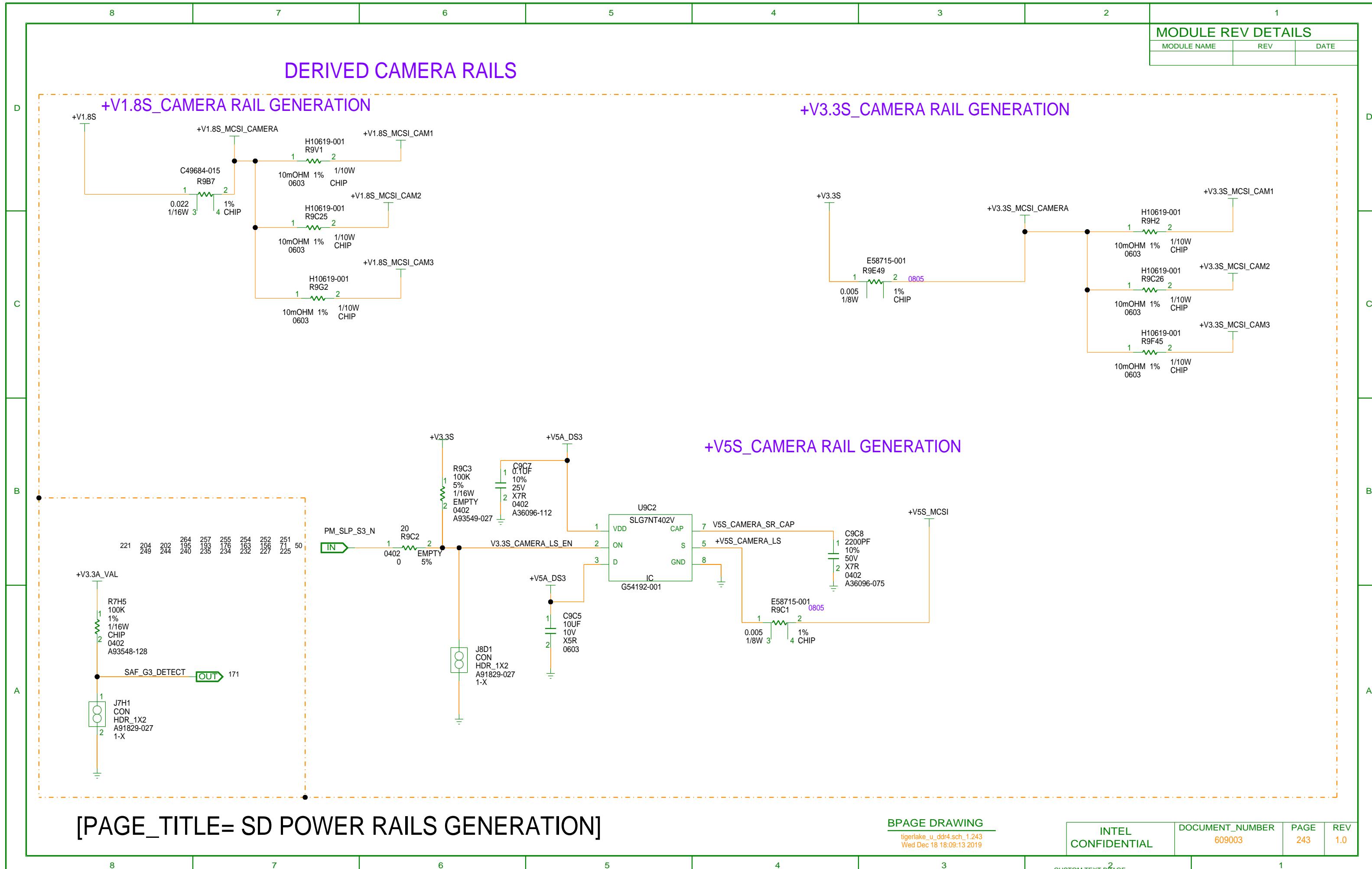


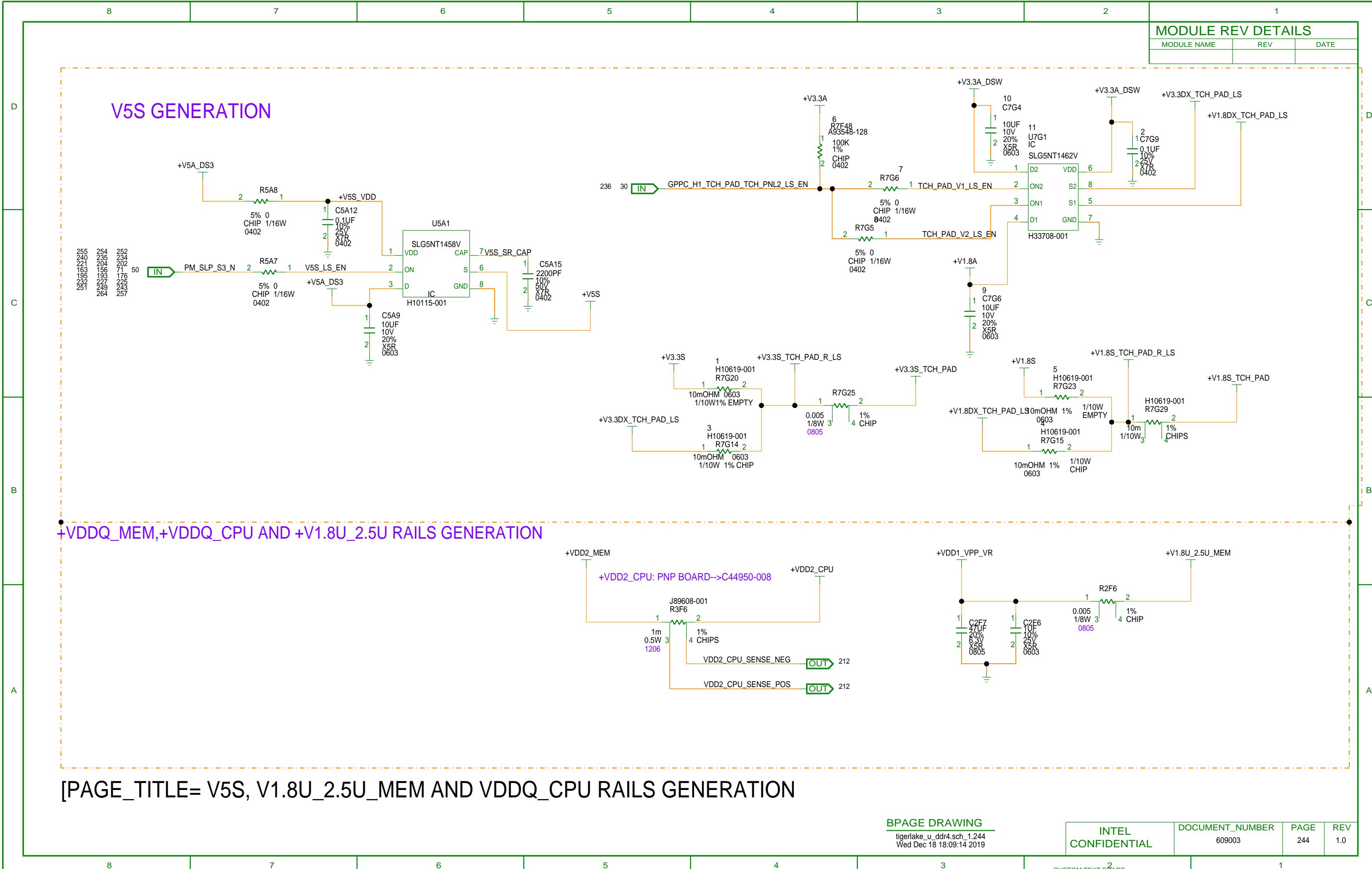






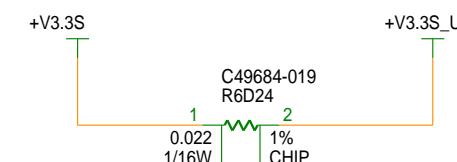
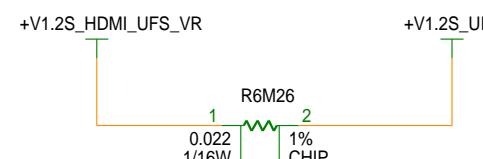
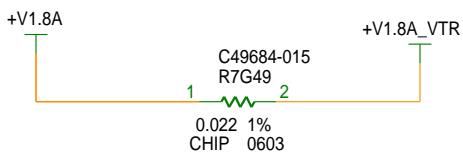
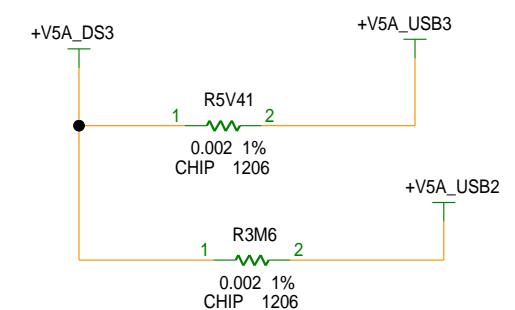
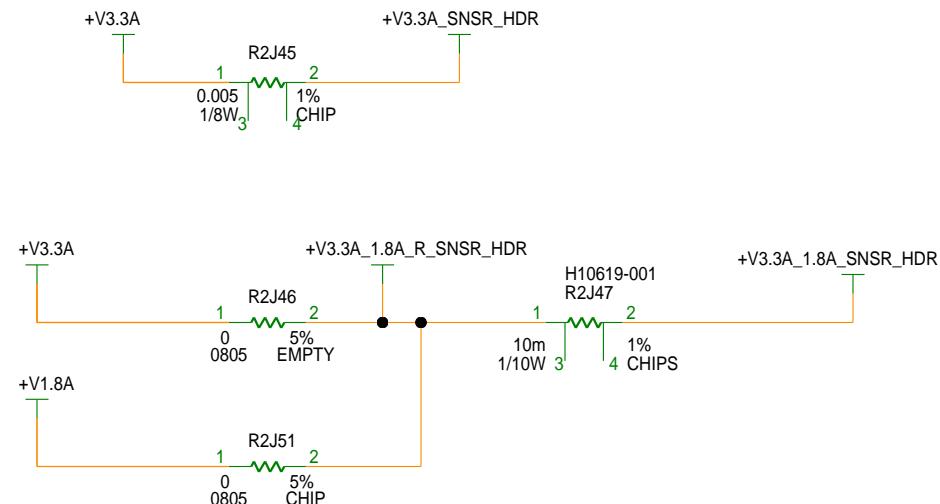
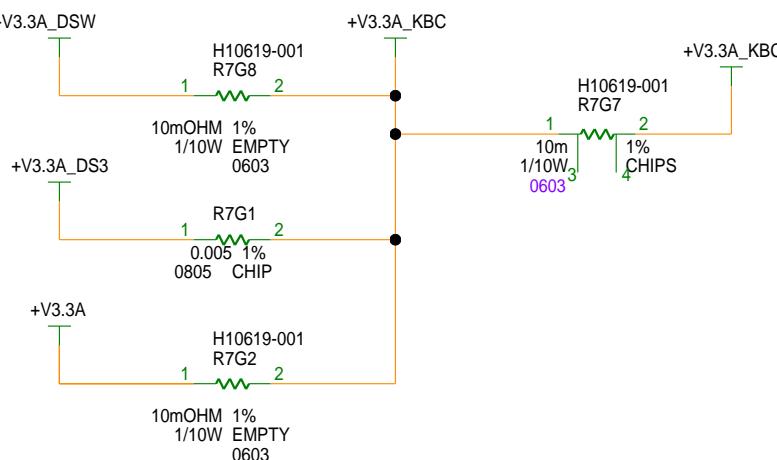


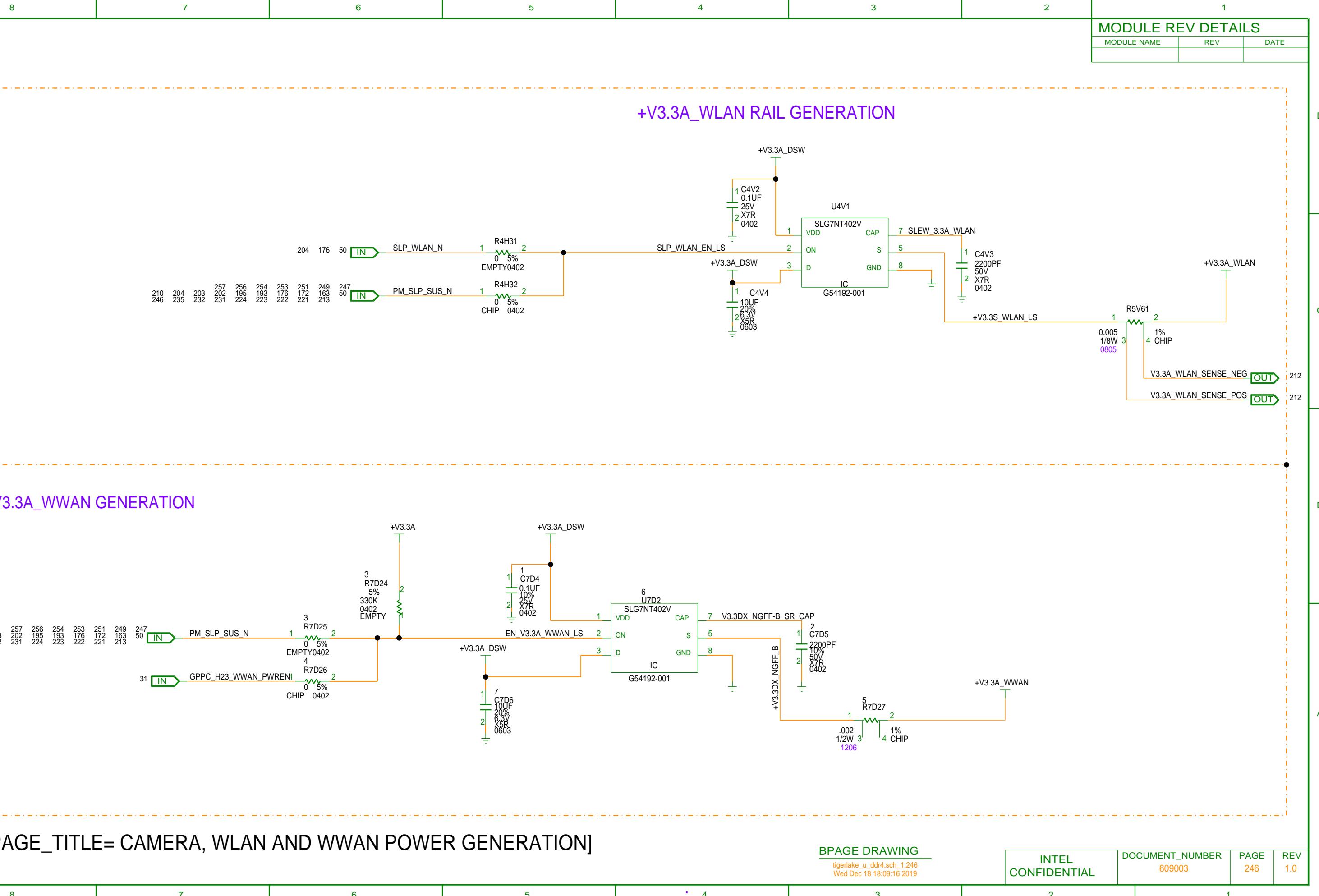


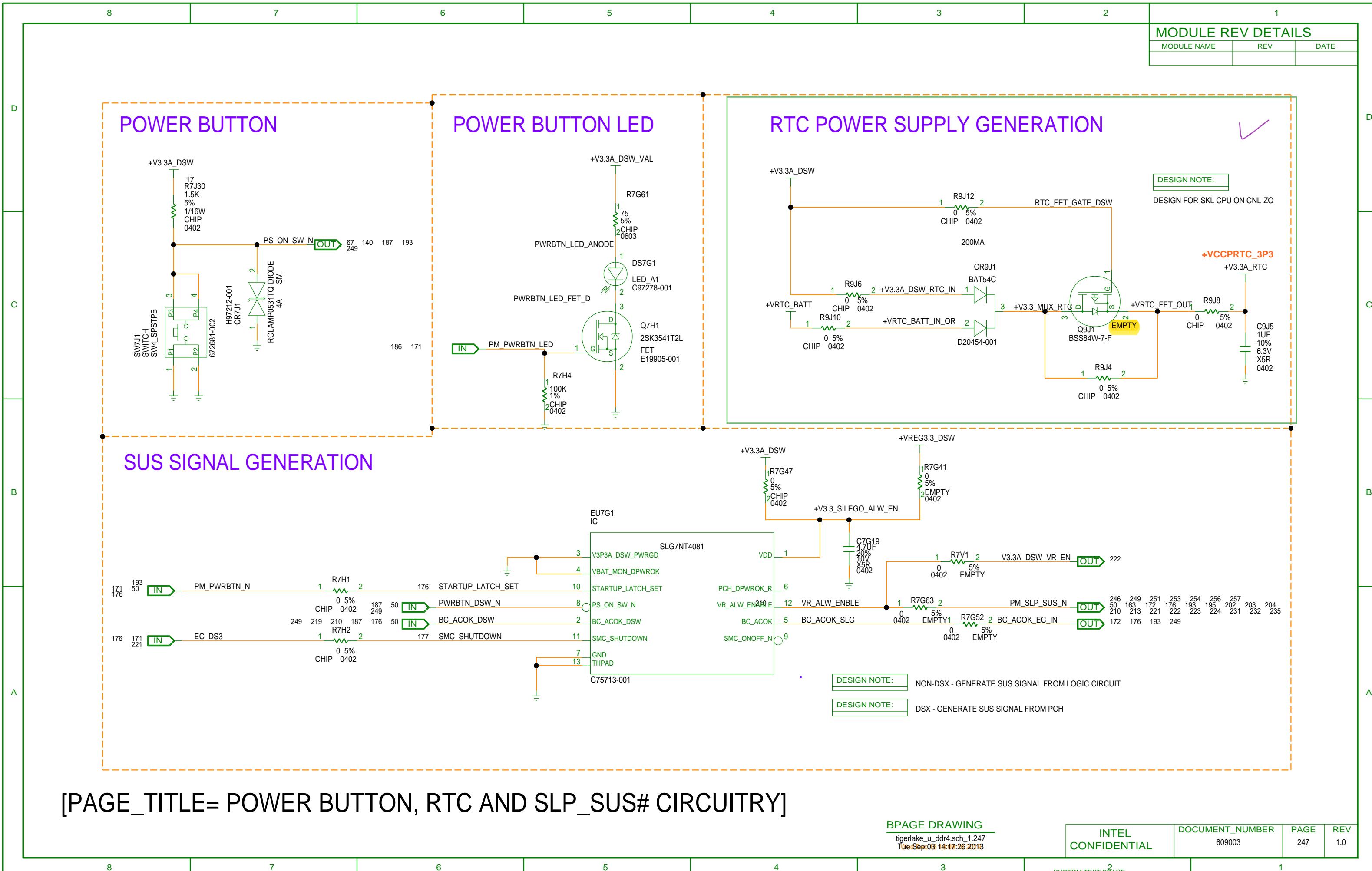


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MODULE REV DETAILS							

DERIVED POWER RAILS

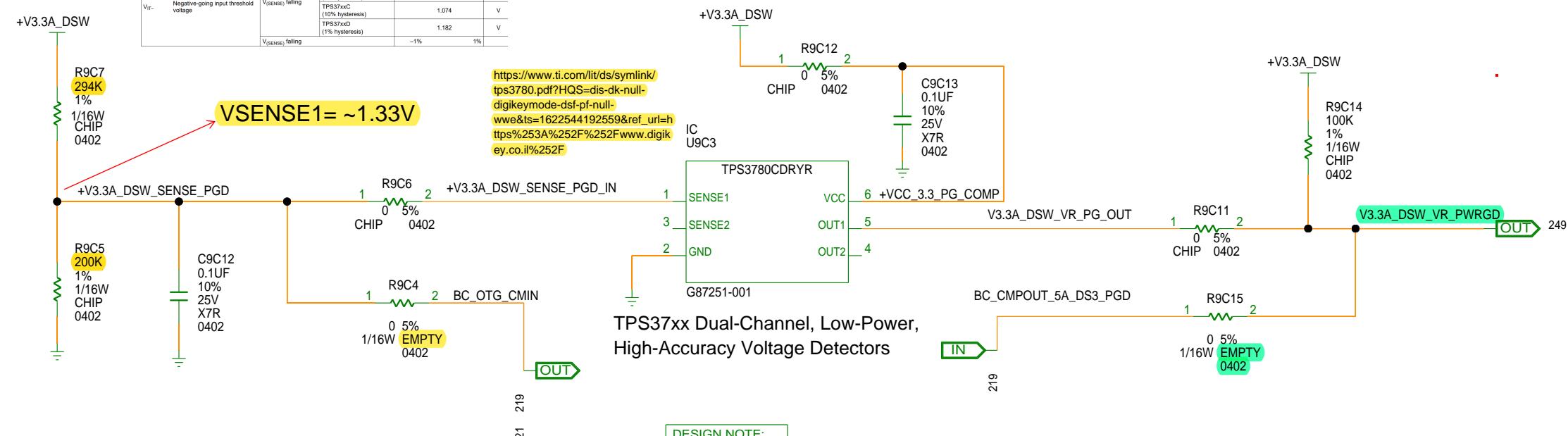
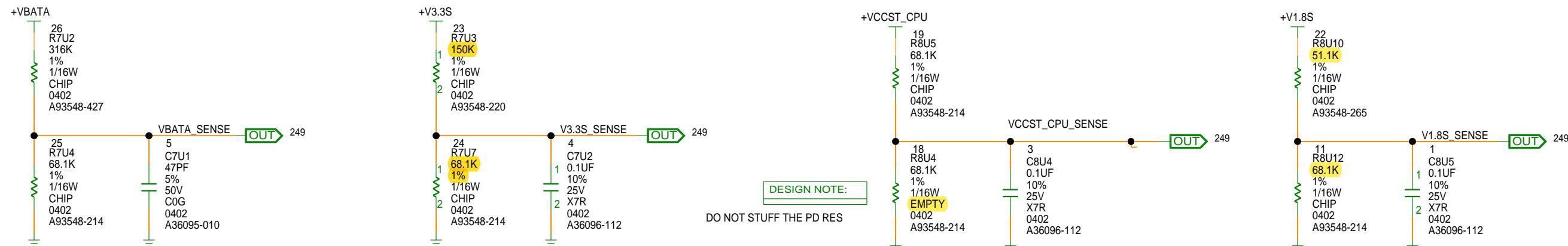






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MODULE NAME		REV	DATE				

POWER SEQUENCING LOGIC - PAGE I

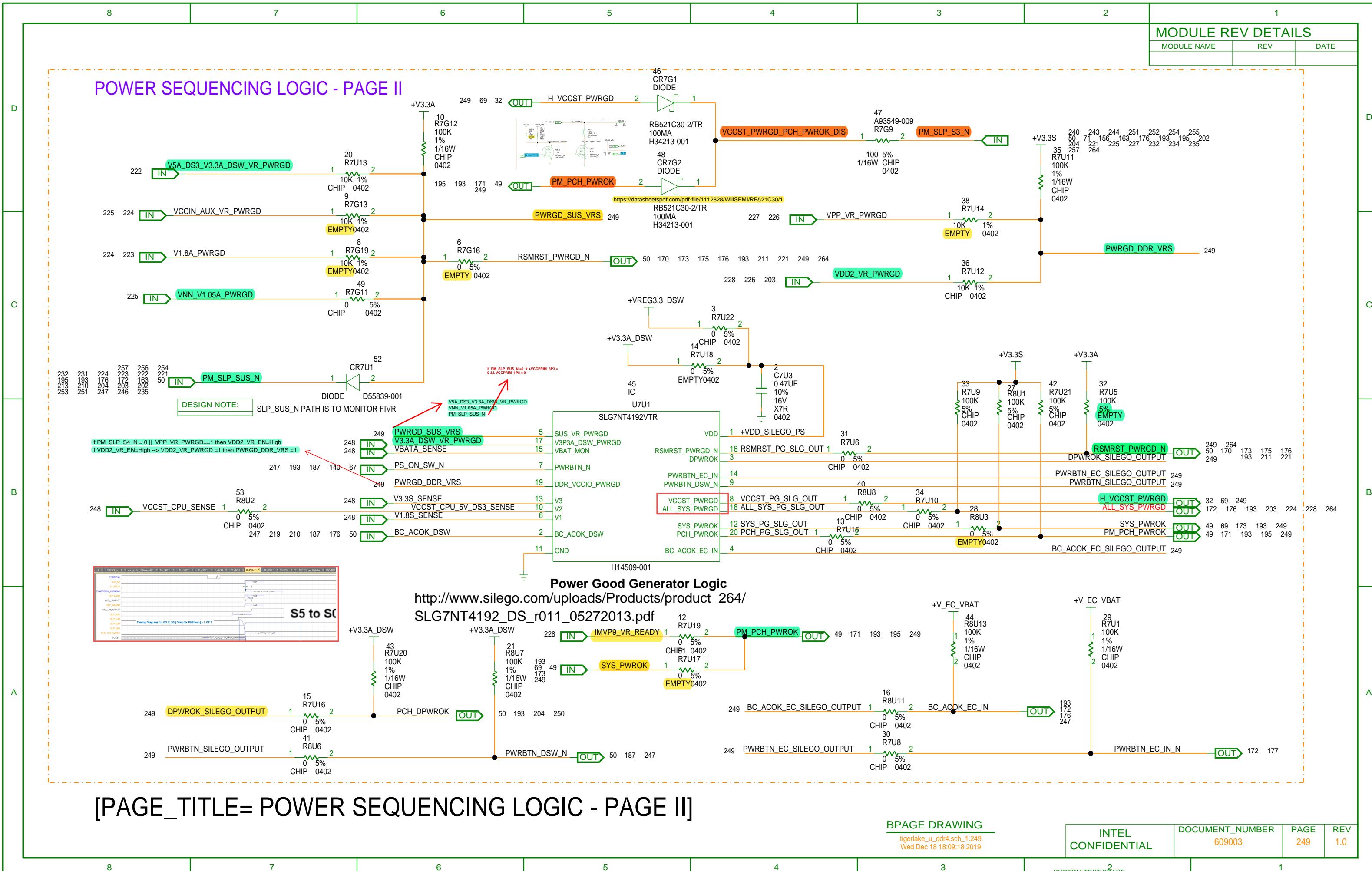


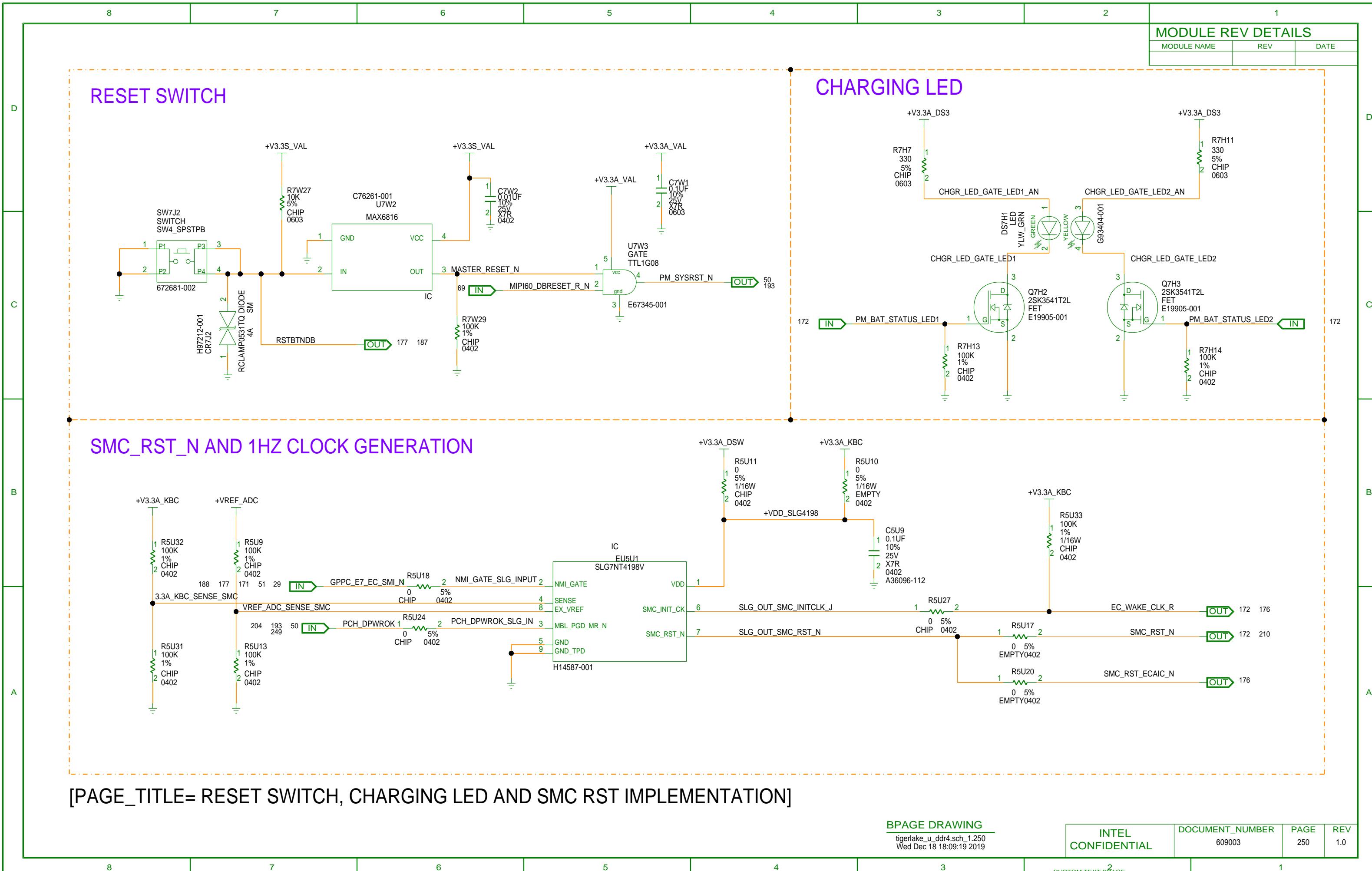
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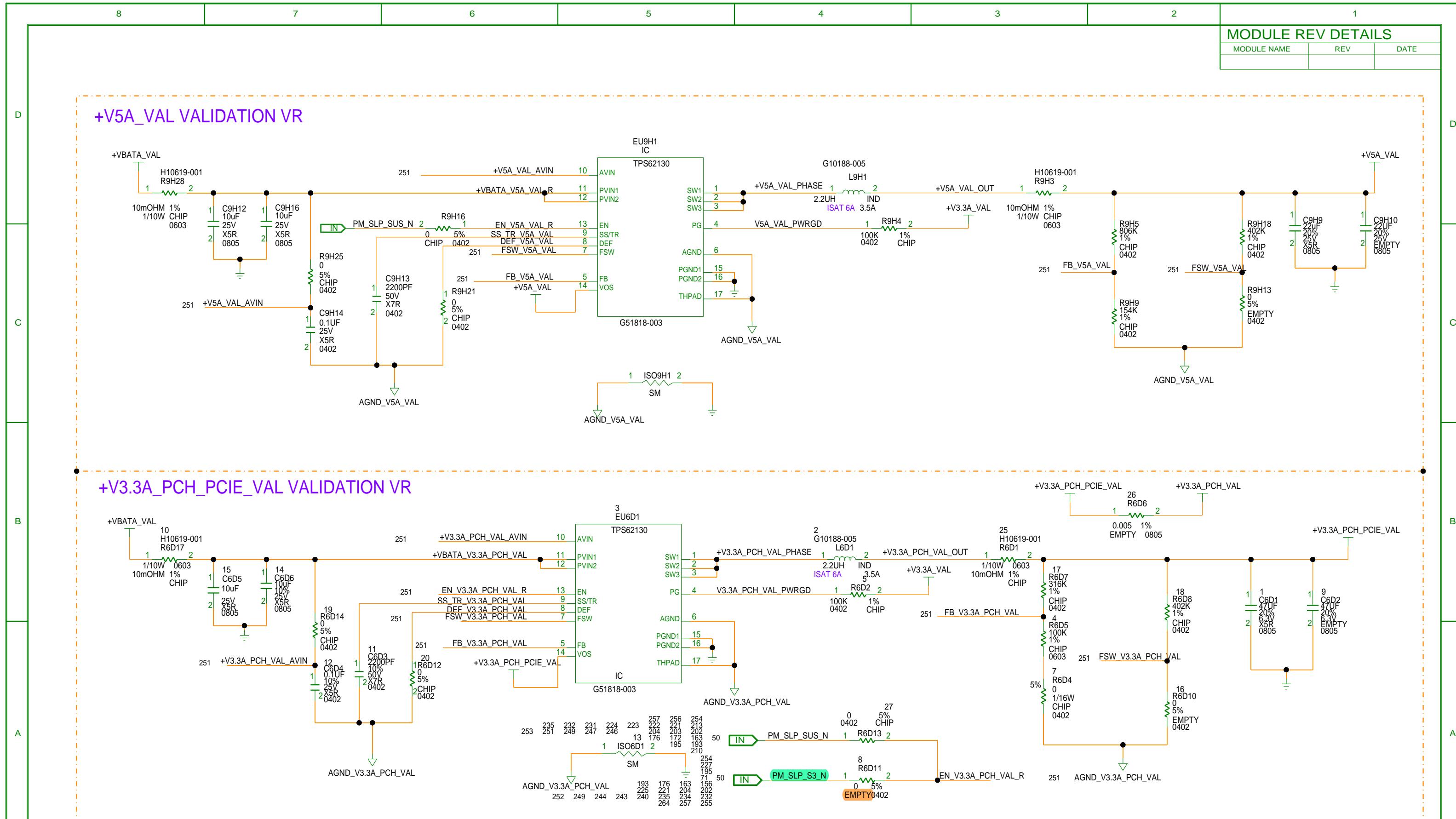
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Wed Dec 18 18:09:17 2019

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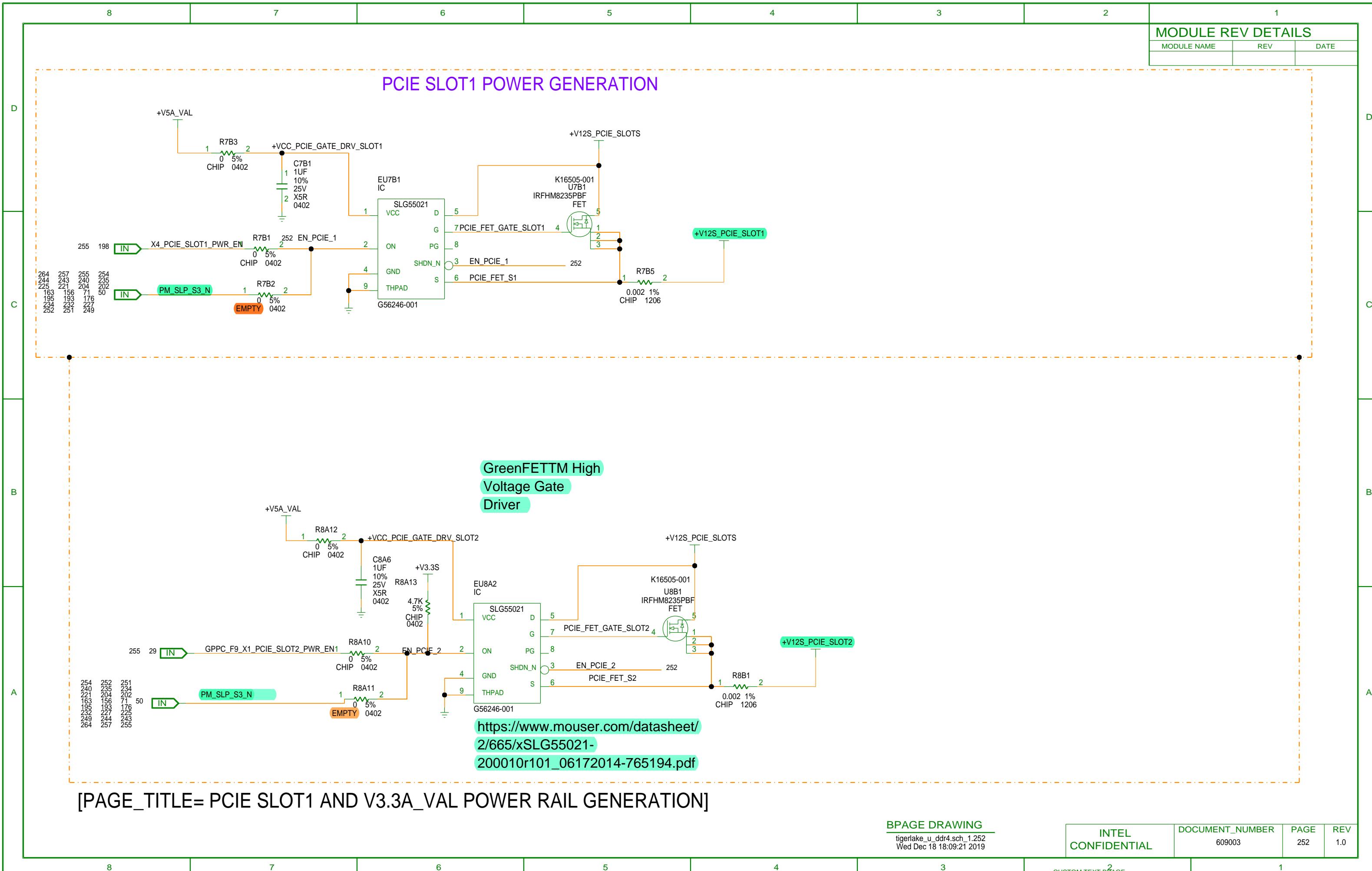


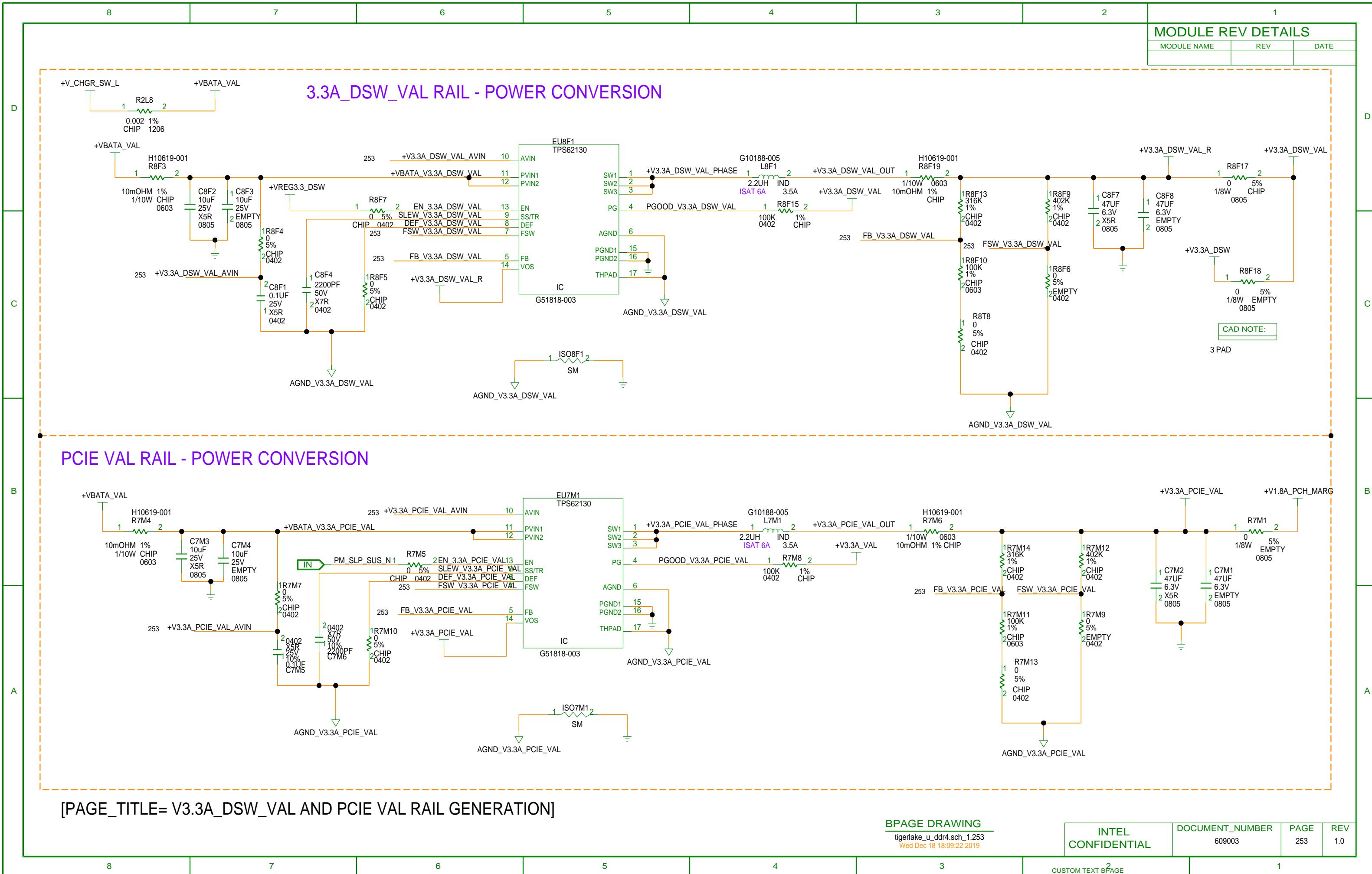
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tigerlake_u_ddr4.sch_1.251
Wed Dec 18 18:09:20 2019

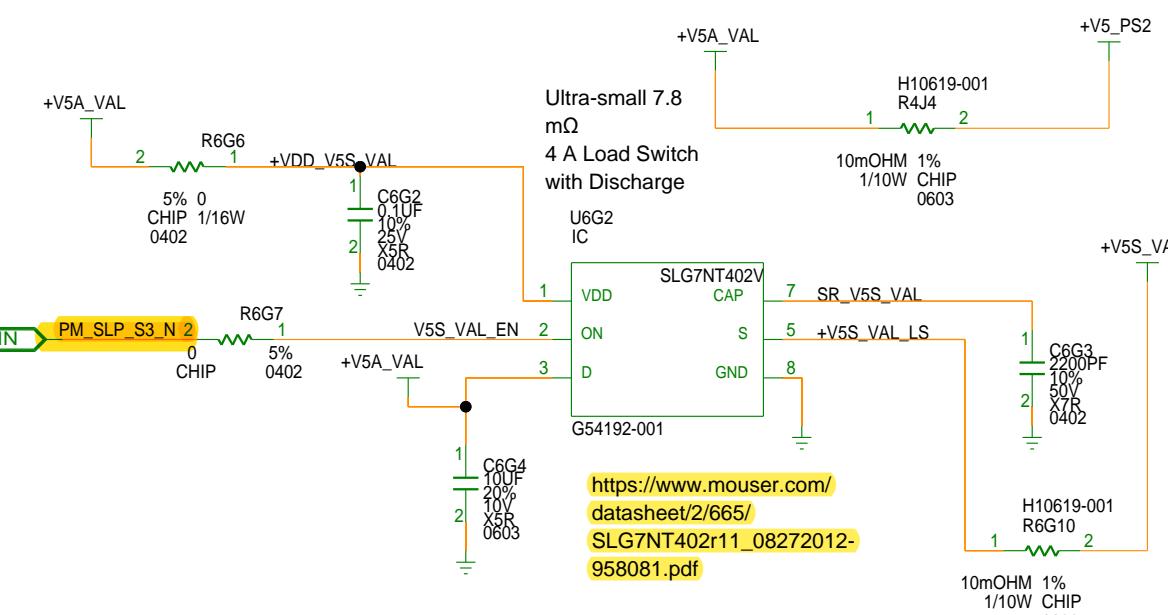
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 251	REV 1.0
CUSTOM TEXT PAGE 2		1	



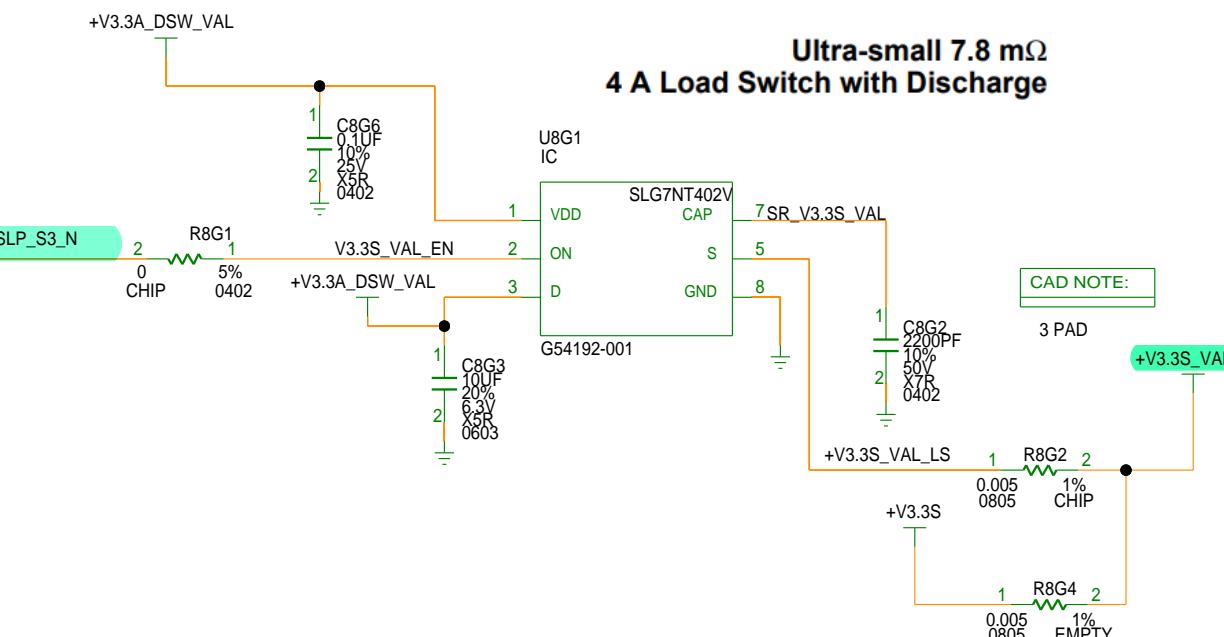


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MODULE NAME						REV	DATE

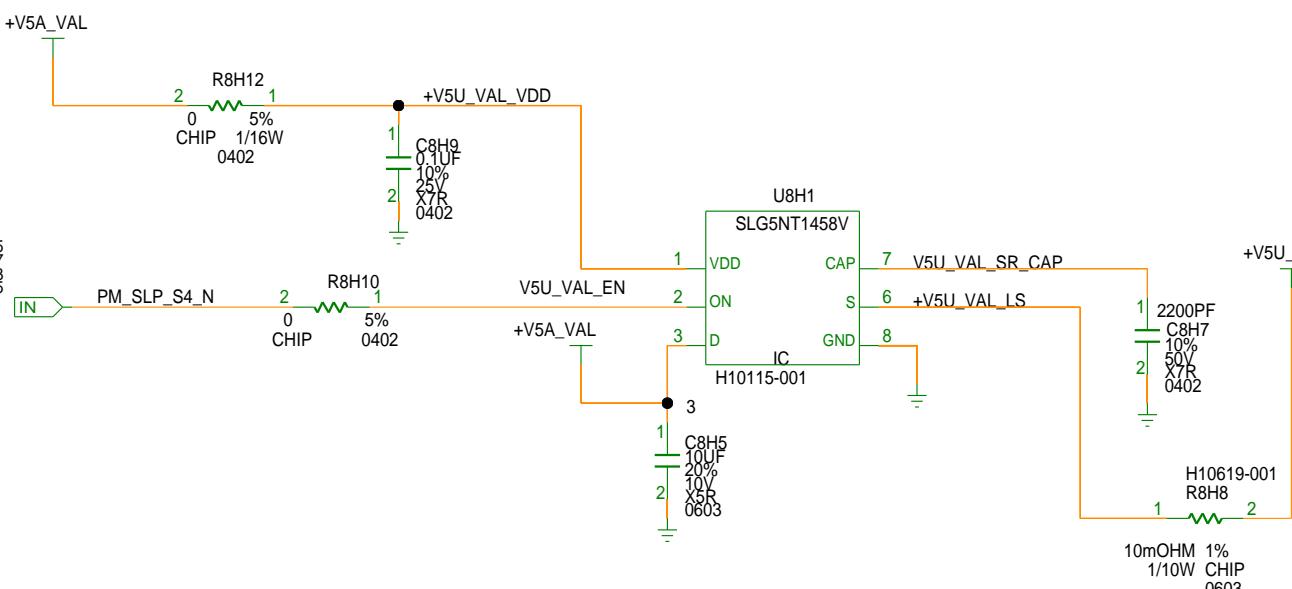
V5S_VAL GENERATION



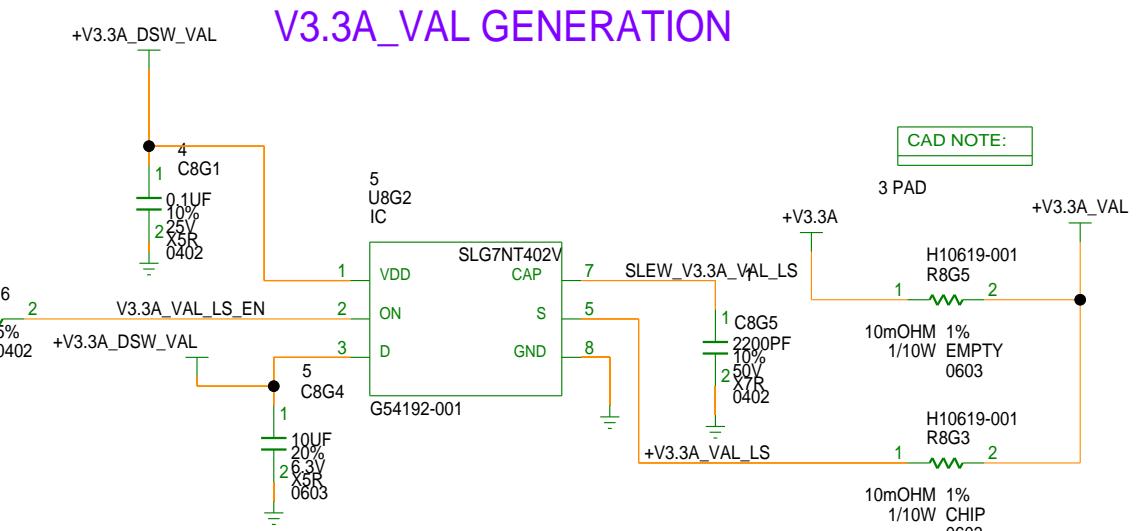
V3.3S_VAL GENERATION



V5U_VAL GENERATION



V3.3A_VAL GENERATION



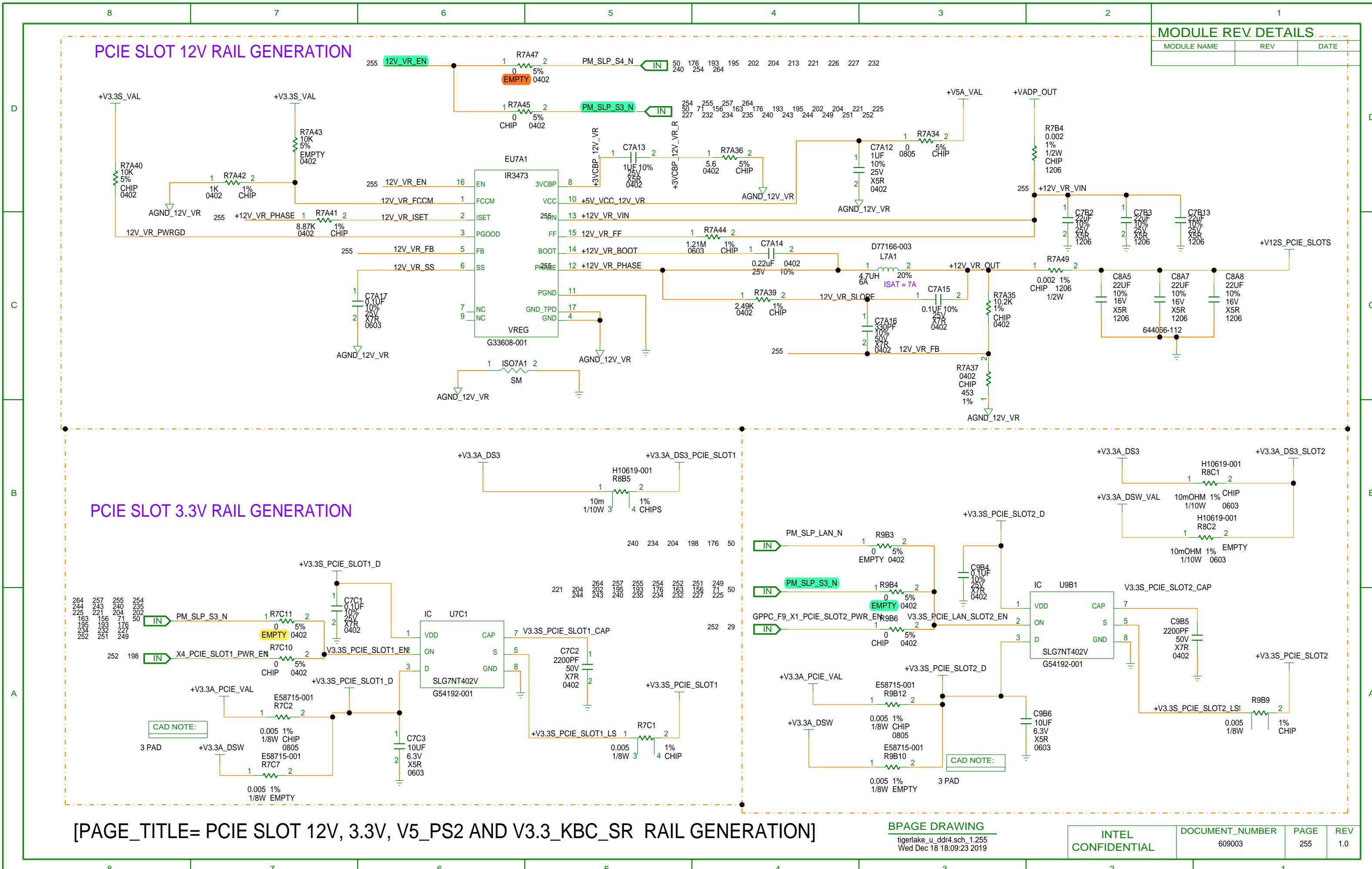
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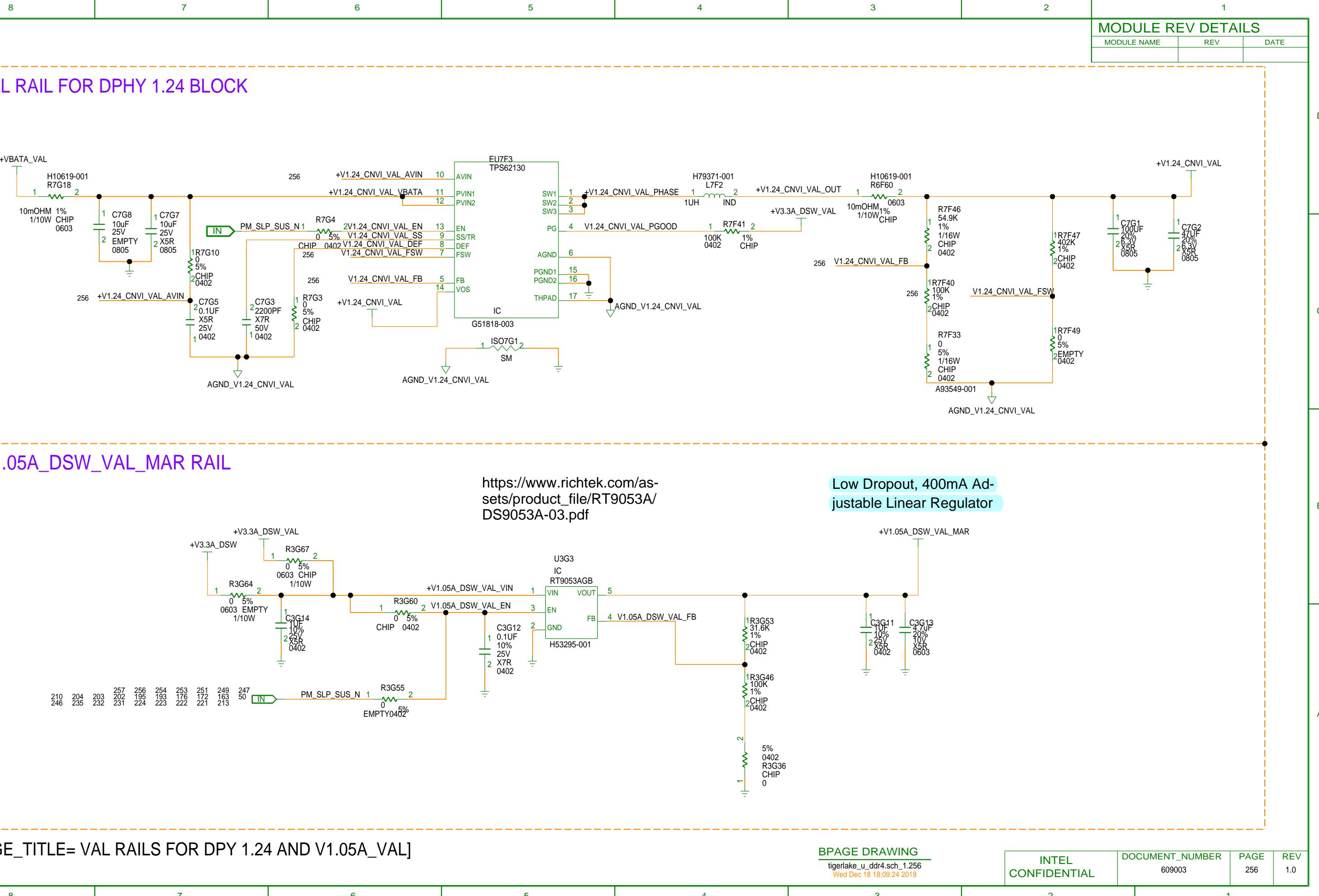
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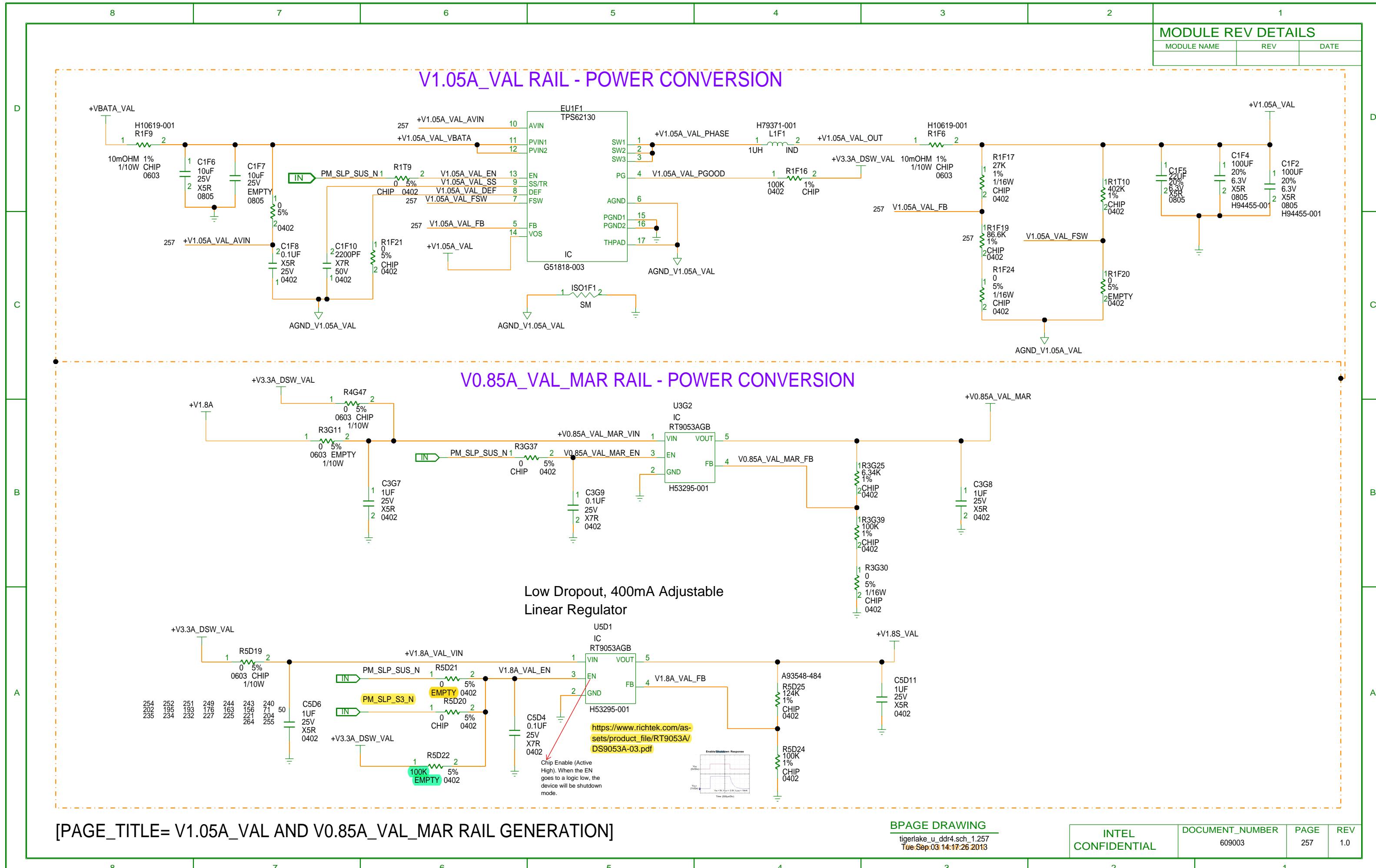
tigerlake_u_ddr4.sch_1254
Wed Dec 18 18:09:22 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT 2 PAGE







8	7	6	5	4	3	2	1
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

D

D

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MTG_HOLE
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GND=1,2,3,4,5,6,7,8
G39082-001

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 9
GND=1,2,3,4,5,6,7,8
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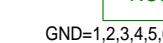
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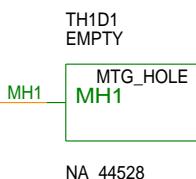
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MTG_HOLE
 9
GND=1,2,3,4,5,6,7,8
G39082-001

B

B

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MH9F1
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G39082-001



ADDED FOR MEMORY INTERPOSER

[PAGE_TITLE=MOUNTING HOLES]

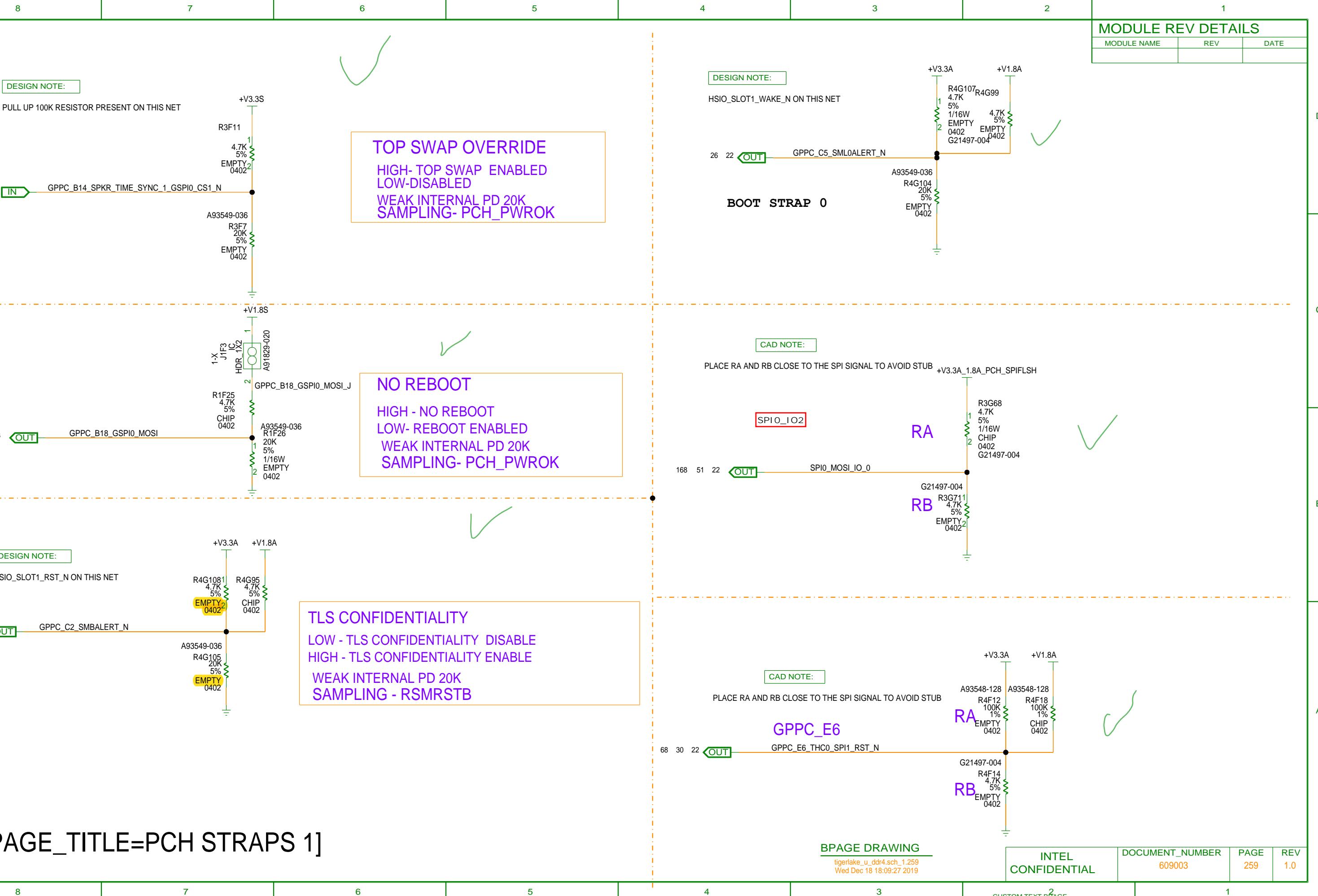
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Wed Dec 18 18:09:26 2019

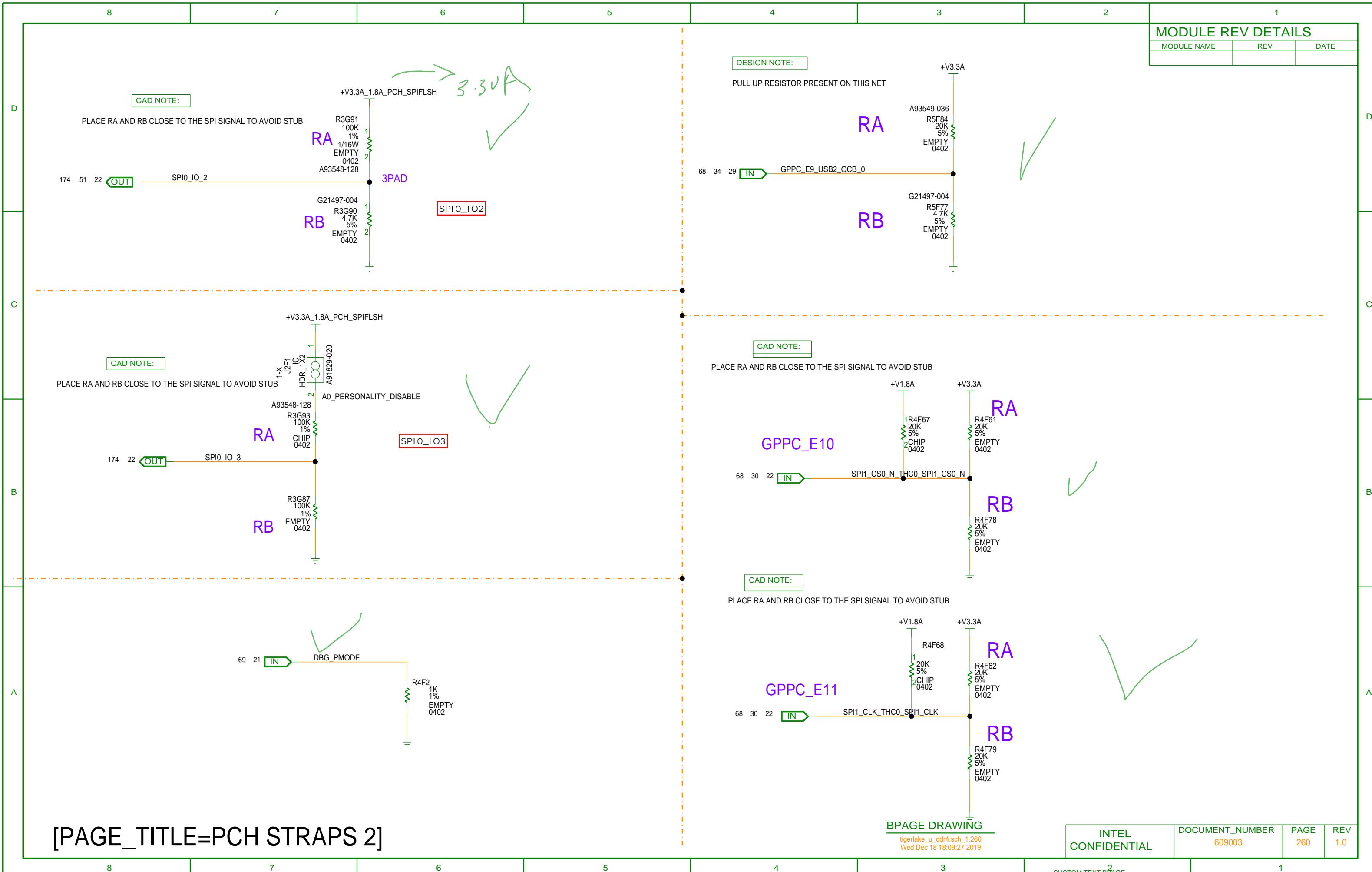
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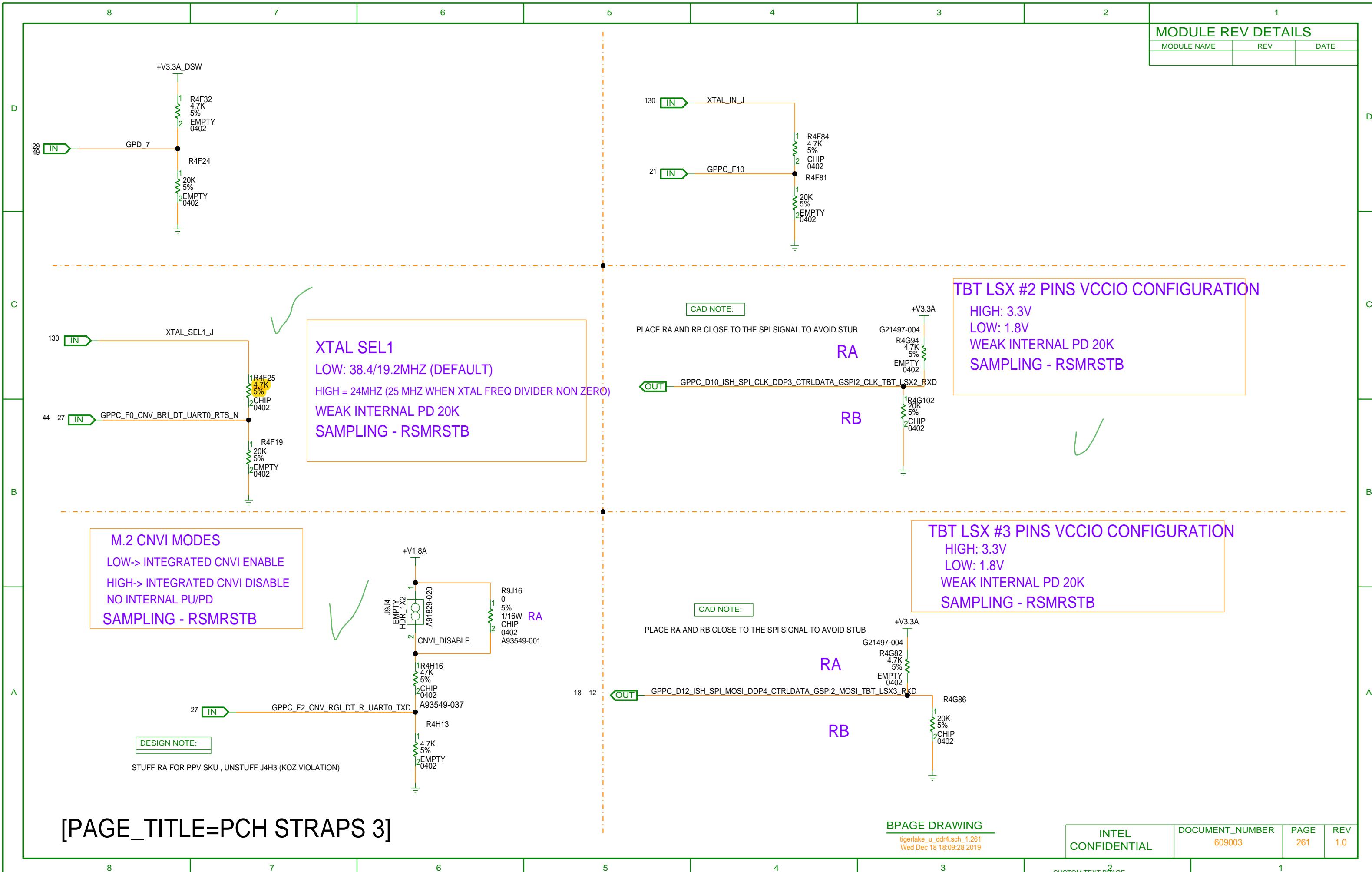
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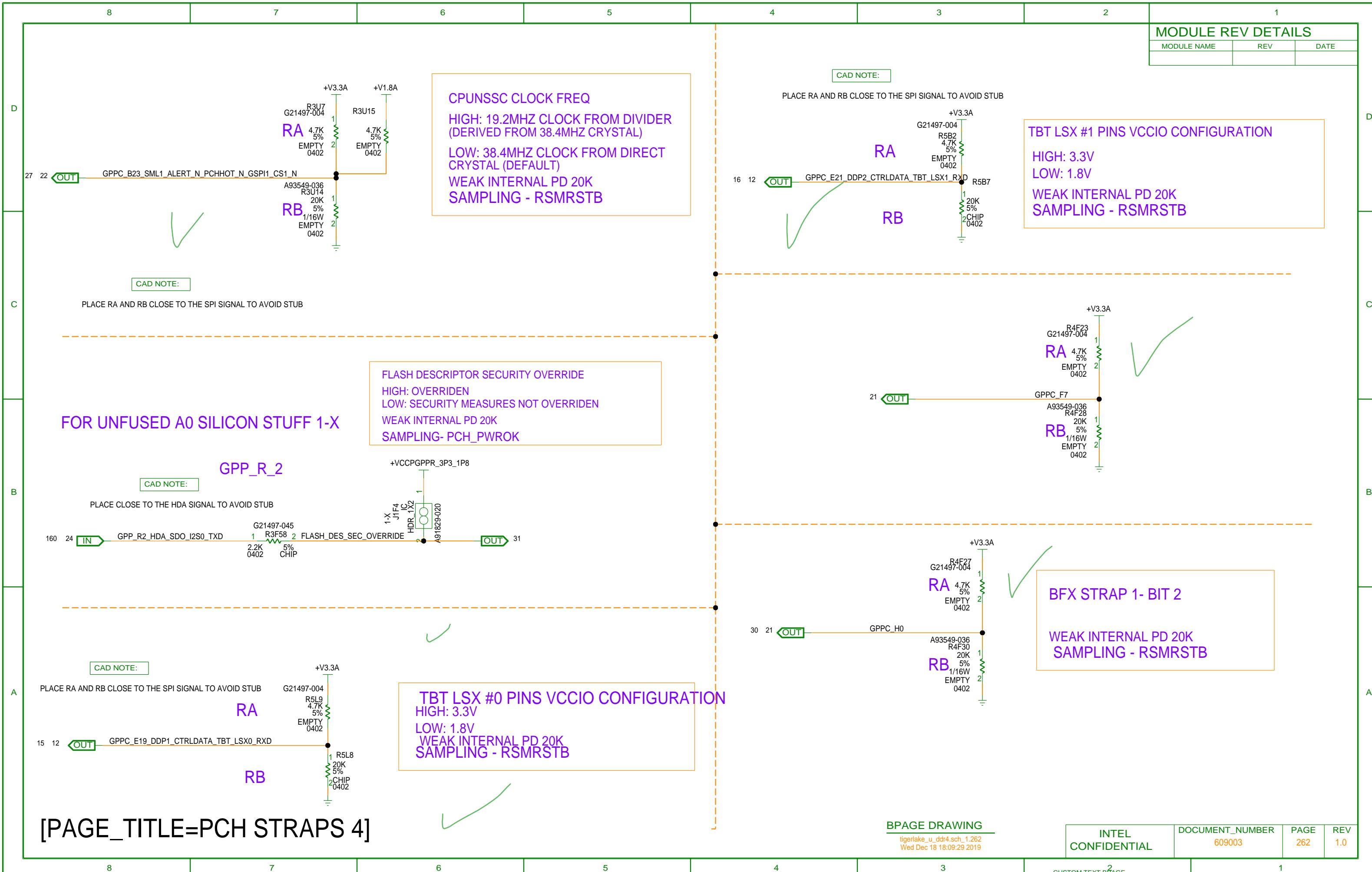
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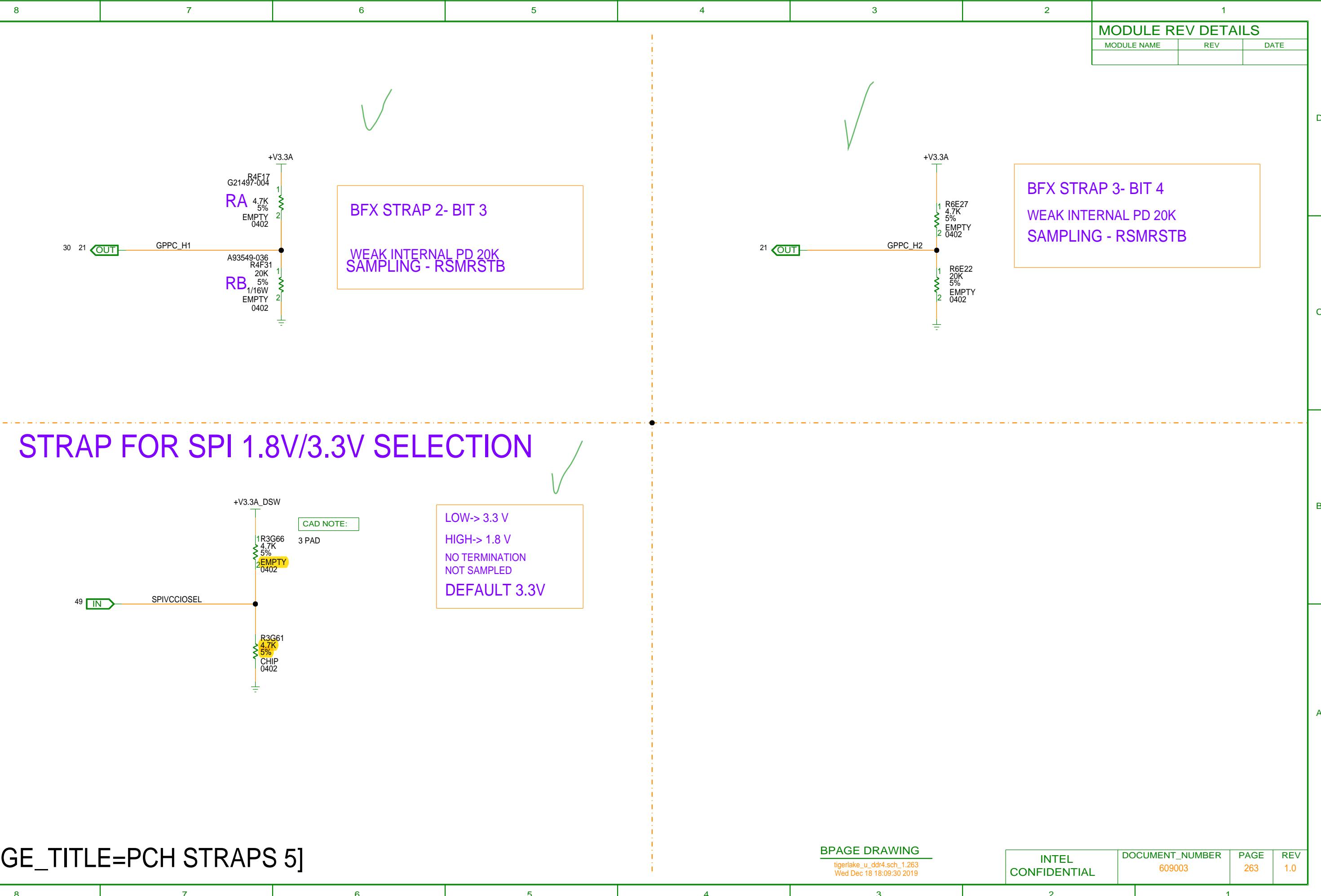
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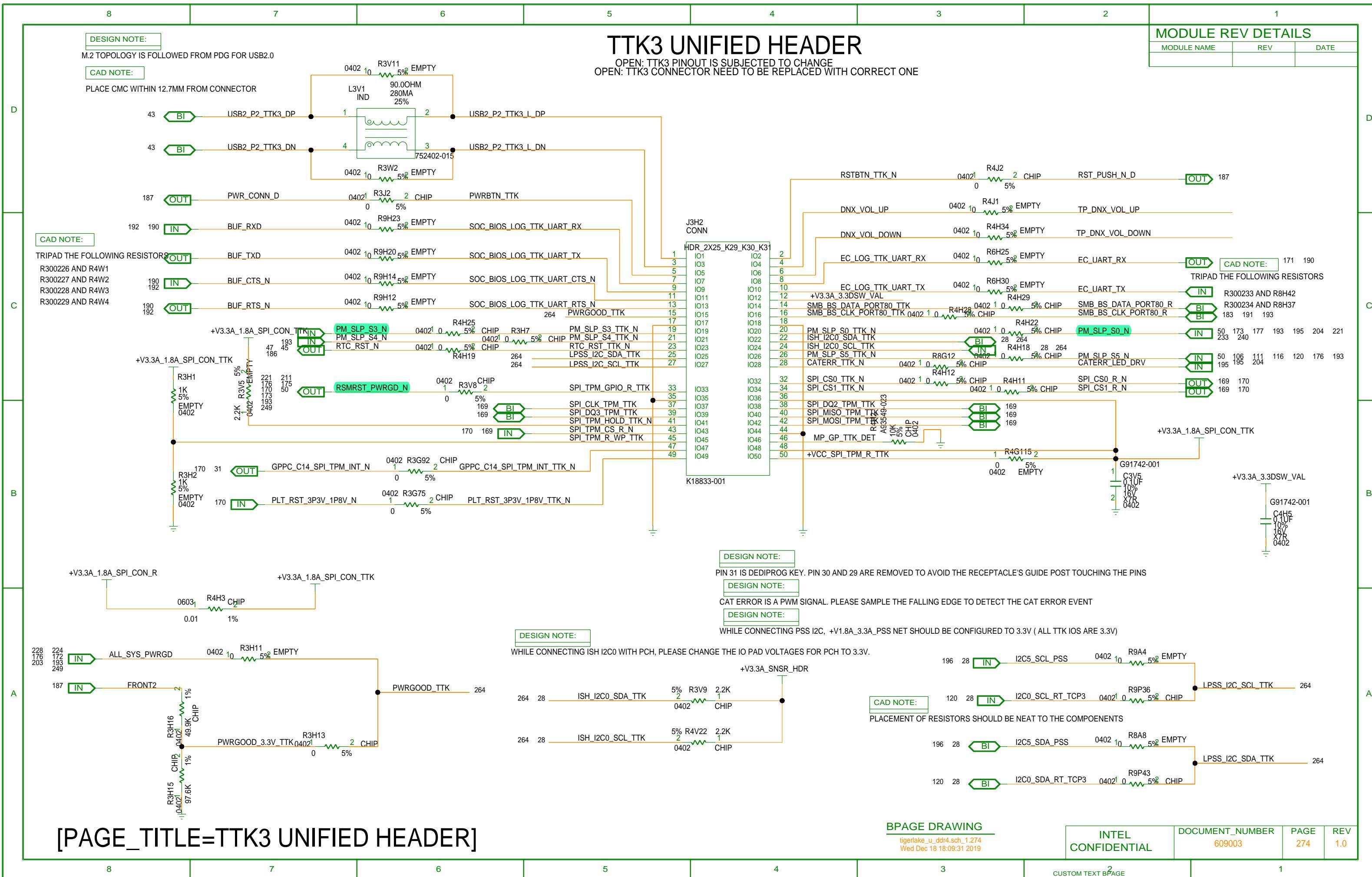


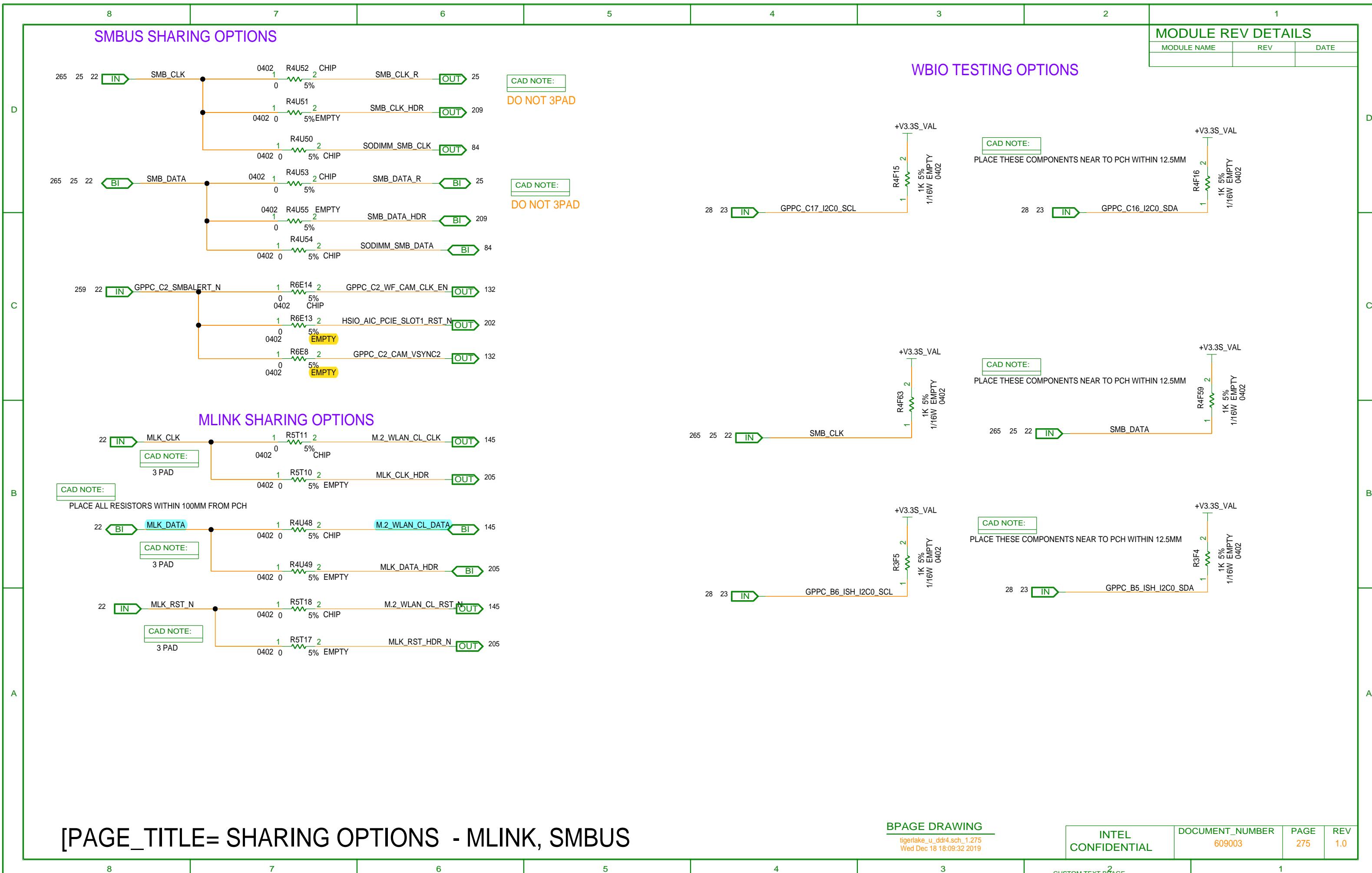


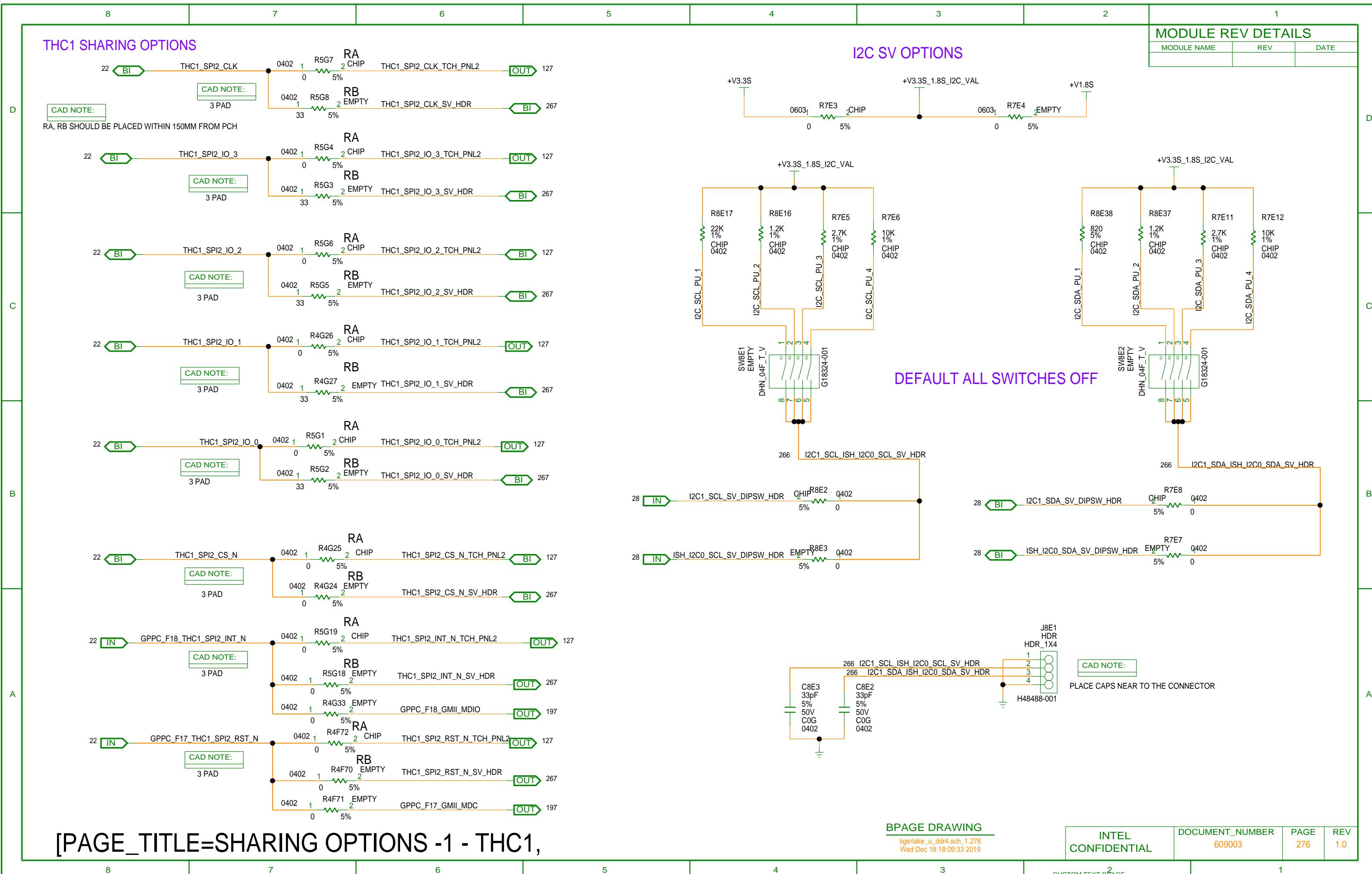












MODULE REV DETAILS		
MODULE NAME	REV	DATE

D

D

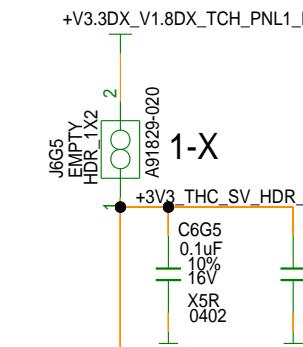
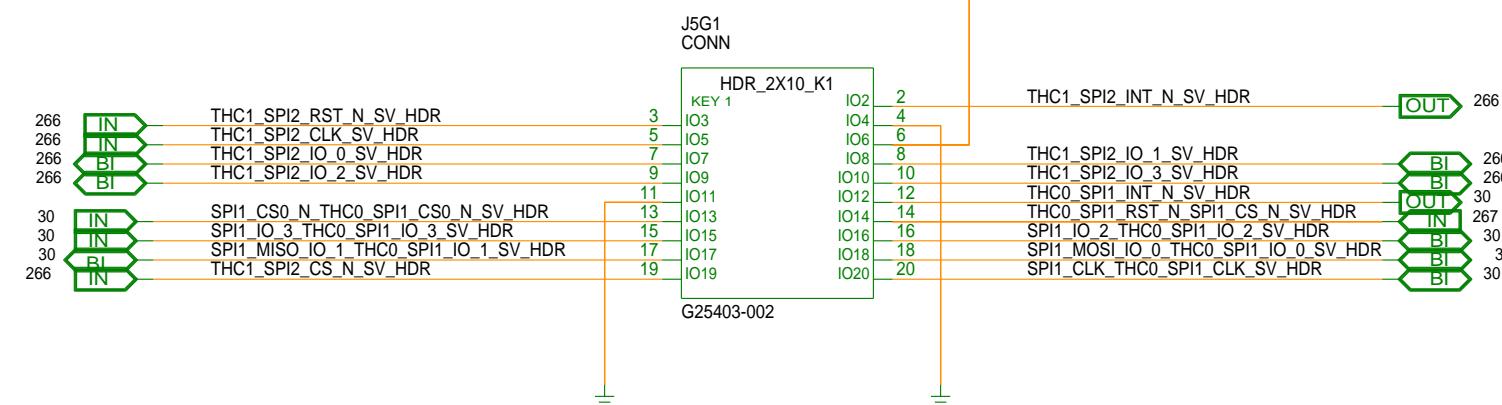
THC0 , THC1 AND SPI1 SV VALIDATION HEADER

DESIGN NOTE:

ONLY SINGLE LOAD IS SUPPORTED. 1.8V IO:RA=33E, 3.3V IO IS NOT POR AND NOT SUPPORTED
MAX CABLE LENGTH SUPPORTED IS 203MM

CAD NOTE:

PLACE RA CLOSE TO CONNECTOR WITHIN 25MM, FOR ALL SIGNALS
PLACE CONNECTOR WITHIN 250MM FROM PCH



DESIGN NOTE:

ON LKF, SPI1 CS1 AND THC0 RESET ARE MULTIPLEXED. HENCE SAME OPTION IS MAINTAINED VIA RESISTOR STUFFING REWORK ON TGL FOR UNIFICATION BETWEEN PLATFORMS

