CME
Customer Manufacturing Enabling
Manufacturing Advantage Services

Manufacturing with the Intel® Mobile Products: Apollo Lake and Apollo Lake-I

Revision 2.6
Q3 2016

The information contained in this document is for reference only. Manufacturing processes are unique, and may require unique solutions to ensure an acceptable level of quality, reliability, and manufacturing yield. Due to differences in equipment and materials, and product design, further process parameter modifications/optimization may be required to meet your quality, reliability, and manufacturing yield requirements.

Legal Disclaimer

A “Mission Critical Application” is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL’S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS, COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS’ FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications and roadmaps.

The products and services described may contain defects or errors known as errata which may cause deviations from published specifications. Current characterized errata are available on request.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

Forecasts: Any forecasts of requirements for goods and services are provided for discussion purposes only. Intel will have no liability to make any purchase pursuant to forecasts. Any cost or expense you incur to respond to requests for information or in reliance on any forecast will be at your own risk and expense.

Business Forecast: Statements in this document that refer to Intel’s plans and expectations for the quarter, the year, and the future, are forward-looking statements that involve a number of risks and uncertainties. A detailed discussion of the factors that could affect Intel’s results and plans is included in Intel’s SEC filings, including the annual report on Form 10-K.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting www.intel.com/design/literature.htm.

Intel technologies’ features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. **No computer system can be absolutely secure.** Check with your system manufacturer or retailer or learn more at **[intel.com].**

No computer system can be absolutely secure.

Intel technologies’ features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at Intel.com, or from the OEM or retailer.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Intel, the Intel logo, and Thunderbolt are trademarks of Intel Corporation in the U.S. and/or other countries.

* Other names and brands may be claimed as the property of others.

Revision Changes

- Revision 2.0:
  - Clarified throughout the document where information applies to both Apollo Lake and Apollo Lake-I (which has an IHS)
  - Added Land Pattern for Apollo Lake-I and edited tables for simplicity
  - Added Package Mechanical Drawing for Apollo Lake-I
  - Added Test Content to Module 5
  - Added ESD test data to Module 6

- Revision 2.5:
  - Updated the Package Mechanical Drawings (link)
  - Updated Apollo Lake-I Land Pattern (link)
  - Updated Apollo Lake Coplanarity Value (link)
  - Added Bottom Pocket Depth Dimension on Tray Drawing (link)
  - Updated Test section (link)
  - Updated ESD Comparison Table (link)
  - Added *Considerations During Thermal Solution Assembly/Disassembly* Slide (link)

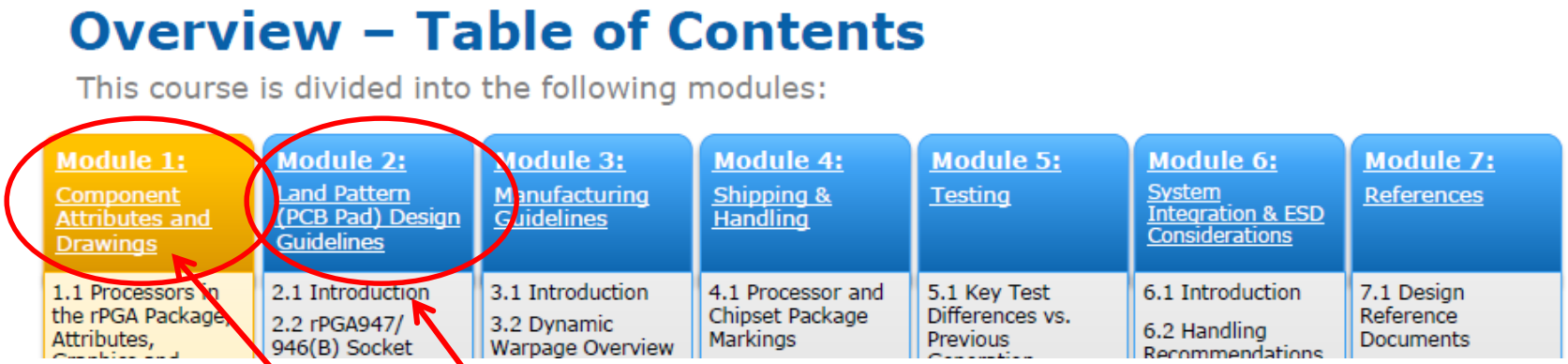
- Revision 2.6:
  - Updated Apollo Lake-I Land Pattern conversion from mils to um (link)

Acronyms Found in this Document

BGA	Ball Grid Array
CTF	Critical to Function
FCBGA	Flip Chip Ball Grid Array
HIC	Humidity Indicator Card
IHS	Integrated Heat Sink
MBB	Moisture Barrier Bag
MD	Metal Defined
MPPO	Modified Polyhenylene Oxide
MSL	Moisture Sensitivity Level
nCTF	Non Critical to Function
SMD	Solder Mask Defined
SMT	Surface Mount Technology
TAL	Time Above Liquidus
TFT	Thermoform Tray

Navigation Aids

Click on the house
to go to that Module's Table of Contents page.

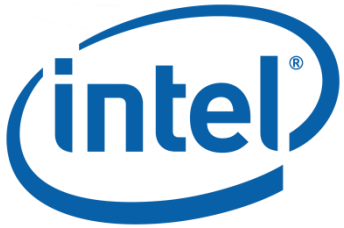


These headers are hyperlinked and link you to the appropriate Table of Contents for that other Module within the MAS document

Overview – Table of Contents

This course is divided into the following modules:

Module 1: Component Attributes and Drawings	Module 2: Land Pattern (PCB Pad) Design Guidelines	Module 3: Manufacturing Guidelines	Module 4: Shipping & Handling	Module 5: Testing	Module 6: System Integration & ESD Considerations	Module 7: References
1.1 Package Attributes 1.2 Package Mechanical Drawing	2.1 Land Pattern	3.1 Manufacturing Guidelines Introduction (e.g. HT dynamic warpage values) 3.2 Critical SMT Recommendations 3.3 Solder Paste Formulation 3.4 Paste Stencil Recommendations	4.1 Processor Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements	5.1 Intel® Trusted Execution Engine Firmware Overview 5.2 Manufacturing Test Reference Flow 5.3 Manufacturing Tools Update 5.4 Download and Execute (DnX) 5.5 DnX Triggers 5.6 Intel® Integrated Sensor Solution 5.7 Types of Calibration Process	6.1 ESD Considerations 6.2 Processors General Handling Recommendations 6.3 Thermal Solution Assembly / Disassembly considerations	7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Intel® Business Advantage Portal access Information



Module 1: Component Attributes and Drawings

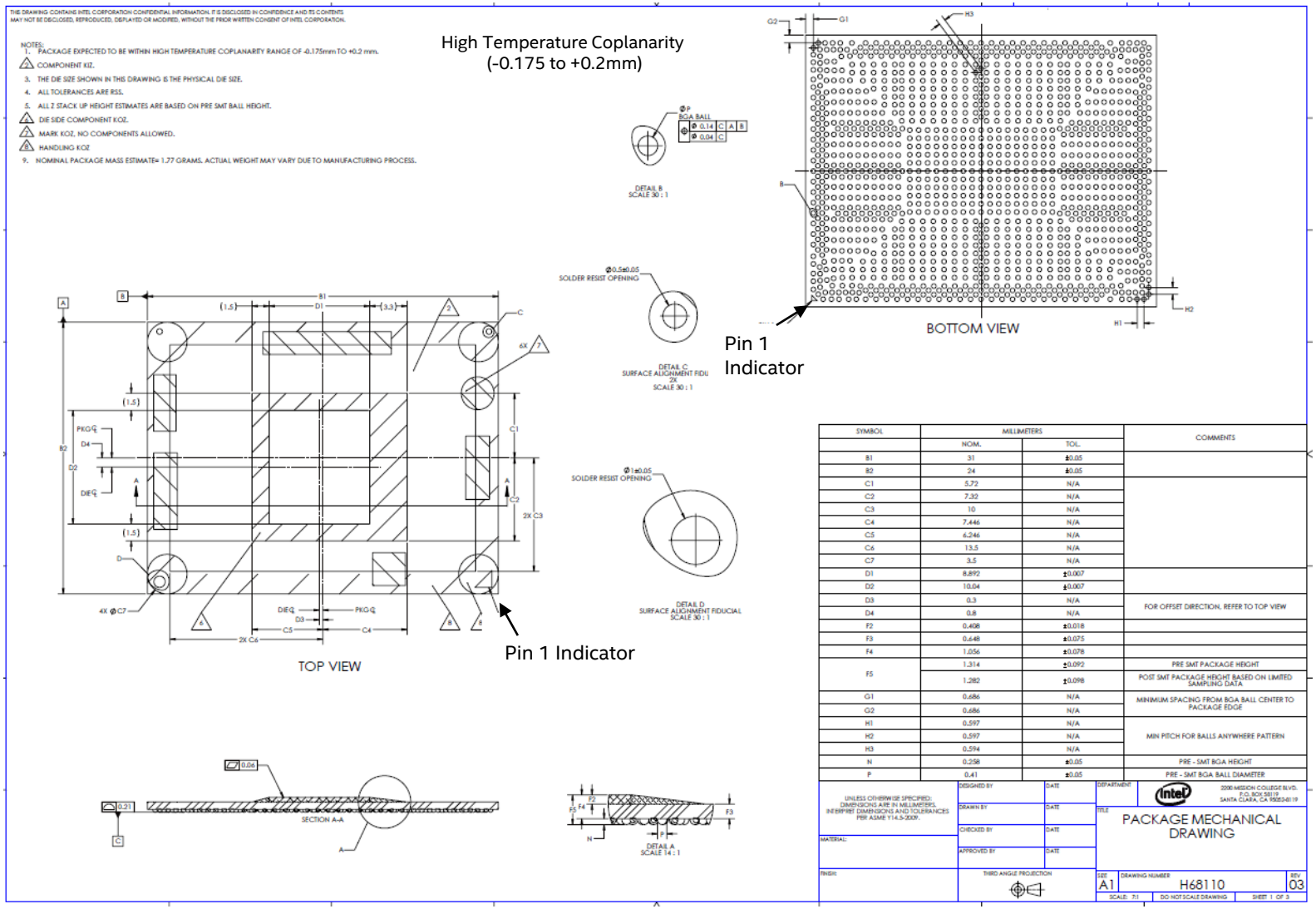
Manufacturing with the Intel® Mobile Products: Apollo Lake & Apollo Lake-I

MAS Rev 2.6, Q3 2016

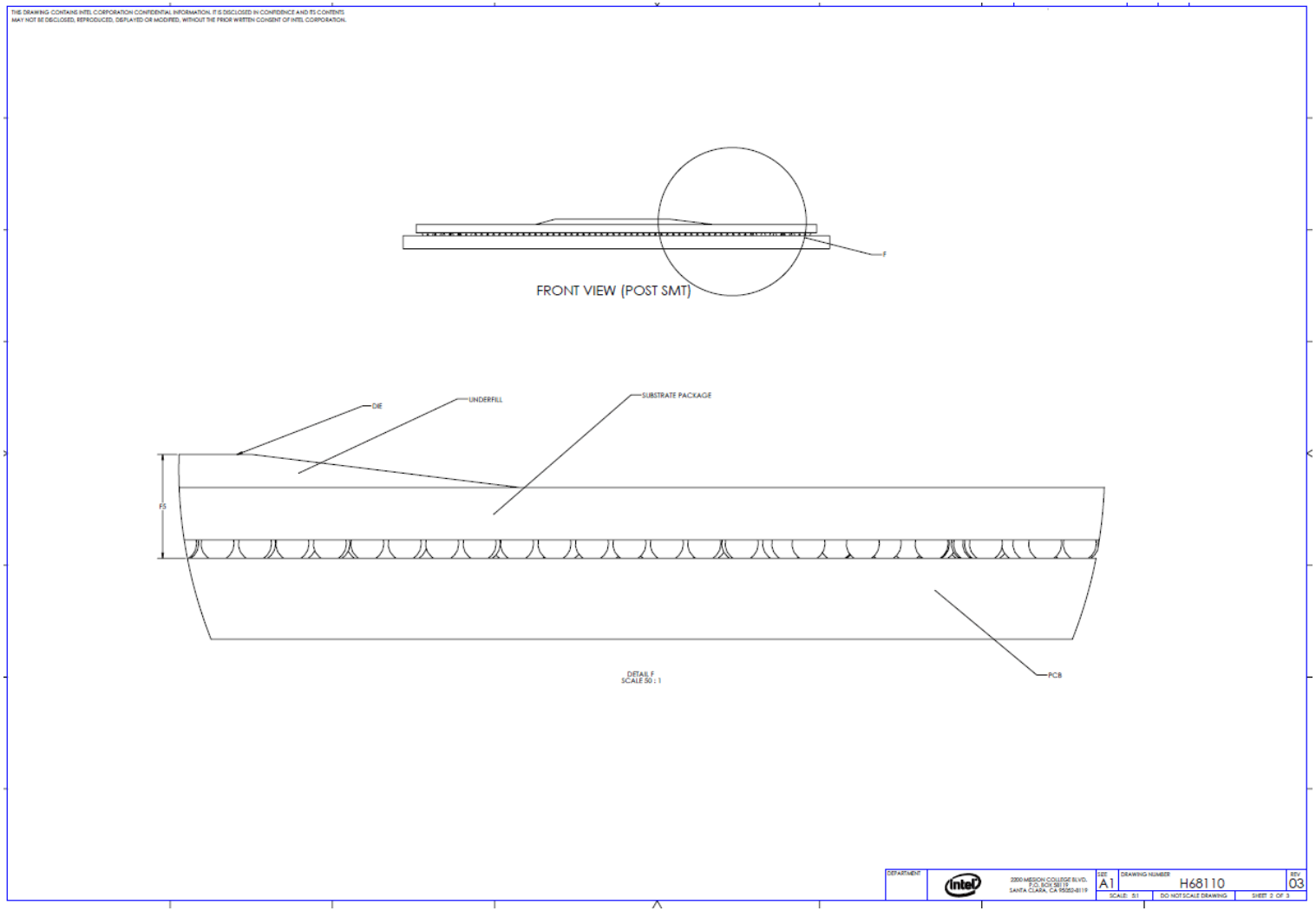
1.1 Component Attributes

Attribute	Apollo Lake	Apollo Lake-I
Package size	31 x 24mm^2 BGA	
Package z-height: Pre-SMT	1.31mm	2.43mm
Package z-height: Post SMT	1.28mm	2.39mm
Number of Pins	1296	
Raw ball diameter ball size (Pre-attach)	0.356mm (14mil)	
Ball diameter (Post- attach, pre-SMT)	0.41 ± 0.05mm (16.1mil)	
BGA minimum pitch	0.593mm	
Die size	8.89 x 10.04mm	
Die thickness	0.412mm	
Substrate thickness	0.648mm	0.718 mm
nCTF corner balls	7 per corner	
IHS	No	Yes

1.2 Package Mechanical Drawing: Apollo Lake (1 of 2)



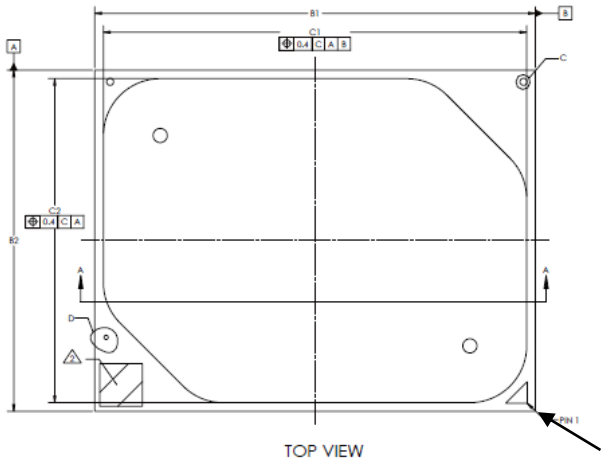
1.2 Package Mechanical Drawing: Apollo Lake (2 of 2)

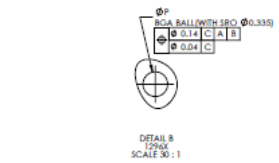


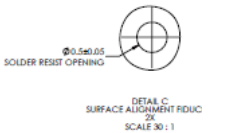
1.2 Package Mechanical Drawing: Apollo Lake-I (1 of 2)

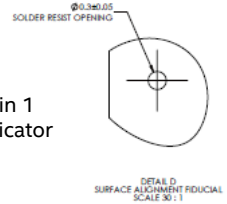
NOTES:
1. PACKAGE EXPECTED TO BE WITHIN HIGH TEMPERATURE COPLANARITY RANGE OF -XXX TO +XXXmm.
2. MARK KOZ. NO COMPONENTS ALLOWED.
3. ALL TOLERANCES ARE RSS.
4. ALL Z STACK UP HEIGHT ESTIMATES ARE BASED ON PRE SMT BALL HEIGHT.
5. NOMINAL PACKAGE MASS ESTIMATE= 7.859 GRAMS. ACTUAL WEIGHT MAY VARY DUE TO MANUFACTURING PROCESS.

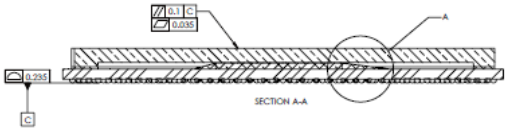
HT Coplanarity values to be available in future revision

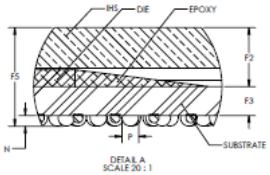


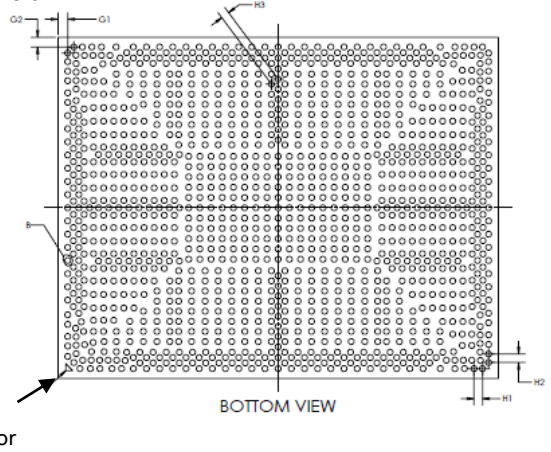












SYMBOL	MILLIMETERS		COMMENTS
	NOM.	TOL.	
B1	31	±0.05	
B2	24	±0.05	
C1	29.8	±0.1	
C2	22.8	±0.1	
F2	1.45	±0.055	
F3	0.718	±0.085	
F5	2.426	±0.113	PRE SMT PACKAGE HEIGHT
	2.394	±0.113	POST SMT PACKAGE HEIGHT BASED ON LIMITED SAMPLING DATA
G1	0.686	N/A	MINIMUM SPACING FROM BGA BALL CENTER TO PACKAGE EDGE
G2	0.686	N/A	
H1	0.597	N/A	MIN PITCH FOR BALLS ANYWHERE PATTERN
H2	0.597	N/A	
H3	0.594	N/A	
N	0.258	±0.05	PRE - SMT BGA HEIGHT
P	0.41	±0.05	PRE - SMT BGA BALL DIAMETER

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS. INTERPRET DIMENSIONS AND TOLERANCES PER: ASME Y14.5-2009

DESIGNED BY | DRAWN BY | CHECKED BY | APPROVED BY | DATE

MATERIAL:

FINISH:

THIRD ANGLE PROJECTION

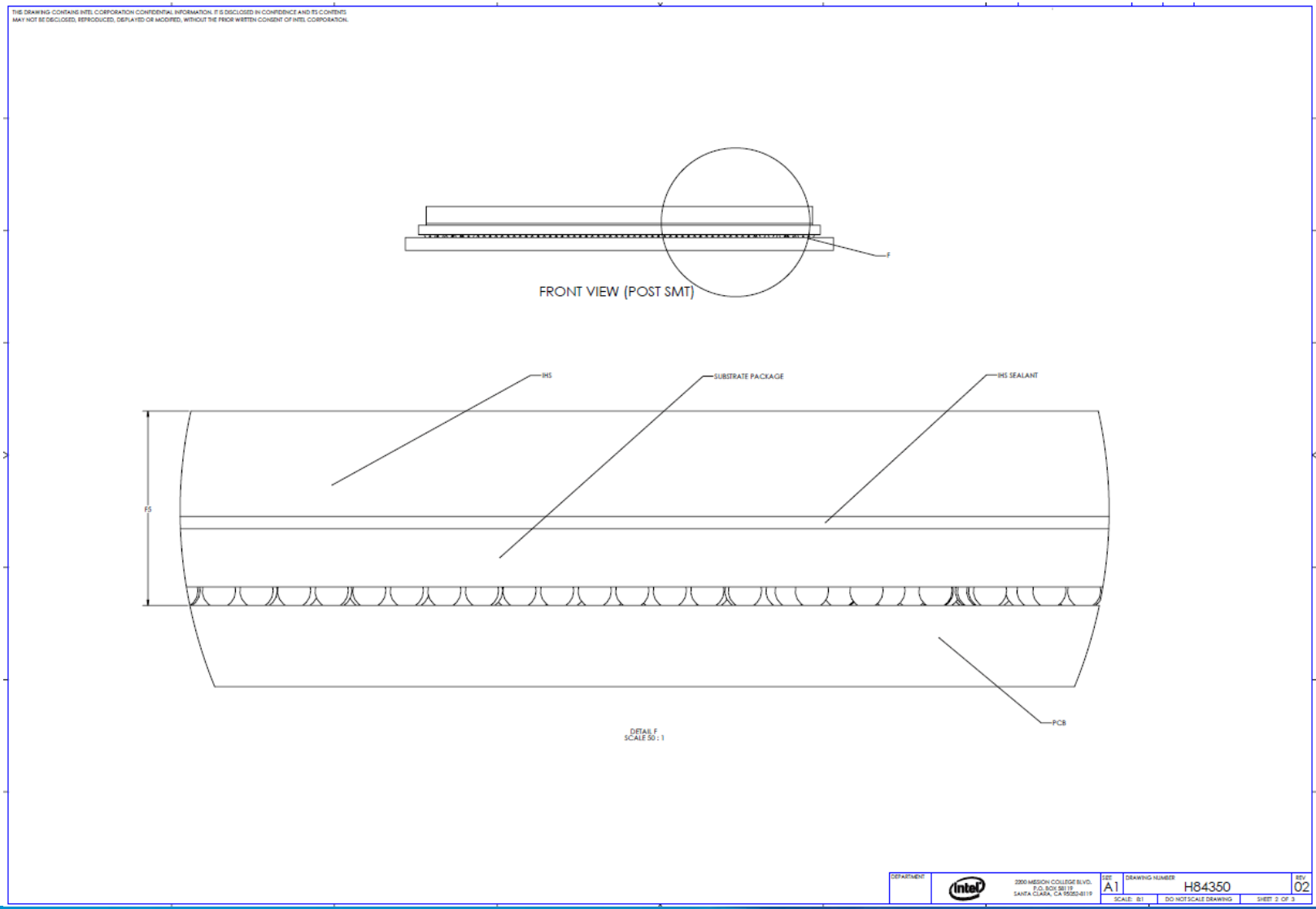
DEPARTMENT: intel 2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119

TITLE: PACKAGE MECHANICAL DRAWING

SIZE A1 | DRAWING NUMBER H84350 | REV 02

SCALE: 2:1 | DO NOT SCALE DRAWING | SHEET 1 OF 3

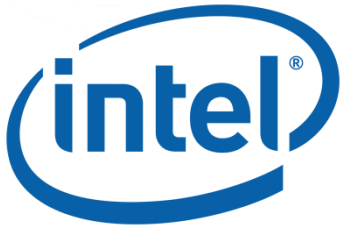
1.2 Package Mechanical Drawing: Apollo Lake-I (2 of 2)



Overview – Table of Contents

This course is divided into the following modules:

Module 1: Component Attributes and Drawings	Module 2: Land Pattern (PCB Pad) Design Guidelines	Module 3: Manufacturing Guidelines	Module 4: Shipping & Handling	Module 5: Testing	Module 6: System Integration & ESD Considerations	Module 7: References
1.1 Package Attributes 1.2 Package Mechanical Drawing	2.1 Land Pattern	3.1 Manufacturing Guidelines Introduction (e.g. HT dynamic warpage values) 3.2 Critical SMT Recommendations 3.3 Solder Paste Formulation 3.4 Paste Stencil Recommendations	4.1 Processor Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements	5.1 Intel® Trusted Execution Engine Firmware Overview 5.2 Manufacturing Test Reference Flow 5.3 Manufacturing Tools Update 5.4 Download and Execute (DnX) 5.5 DnX Triggers 5.6 Intel® Integrated Sensor Solution 5.7 Types of Calibration Process	6.1 ESD Considerations 6.2 Processors General Handling Recommendations 6.3 Thermal Solution Assembly / Disassembly considerations	7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Intel® Business Advantage Portal access Information

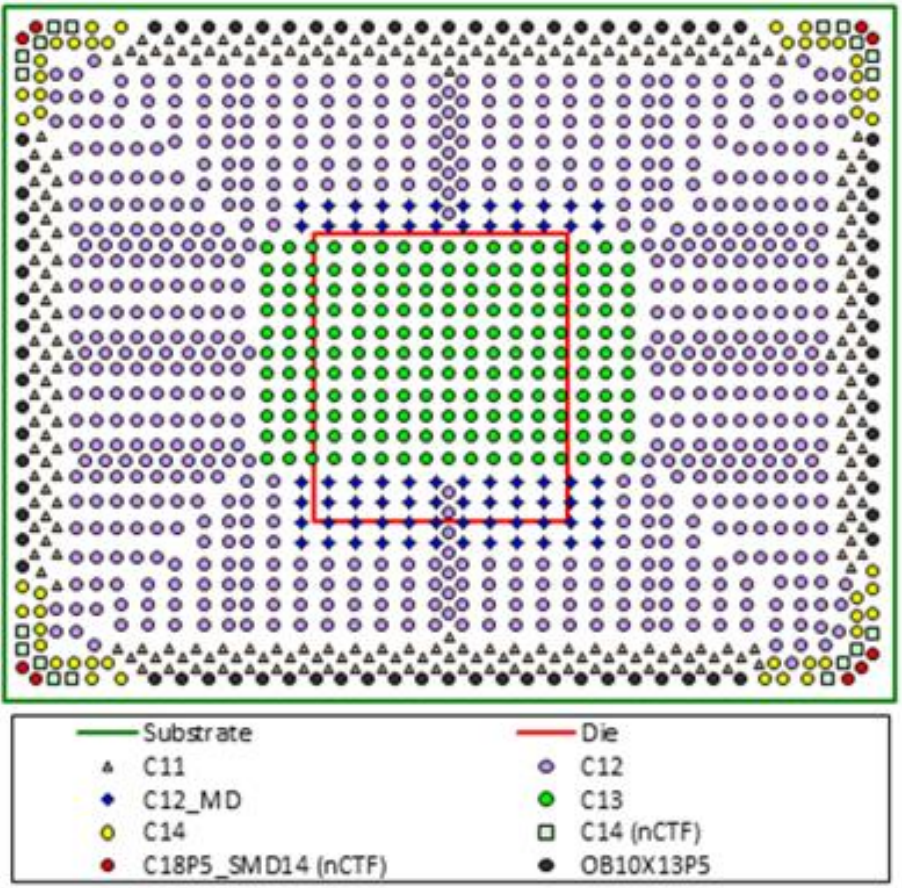


Module 2: Land Pattern (PCB Pad) Design Guidelines

Manufacturing with the Intel® Mobile Products: Apollo Lake & Apollo Lake-I

MAS Rev 2.6, Q3 2016

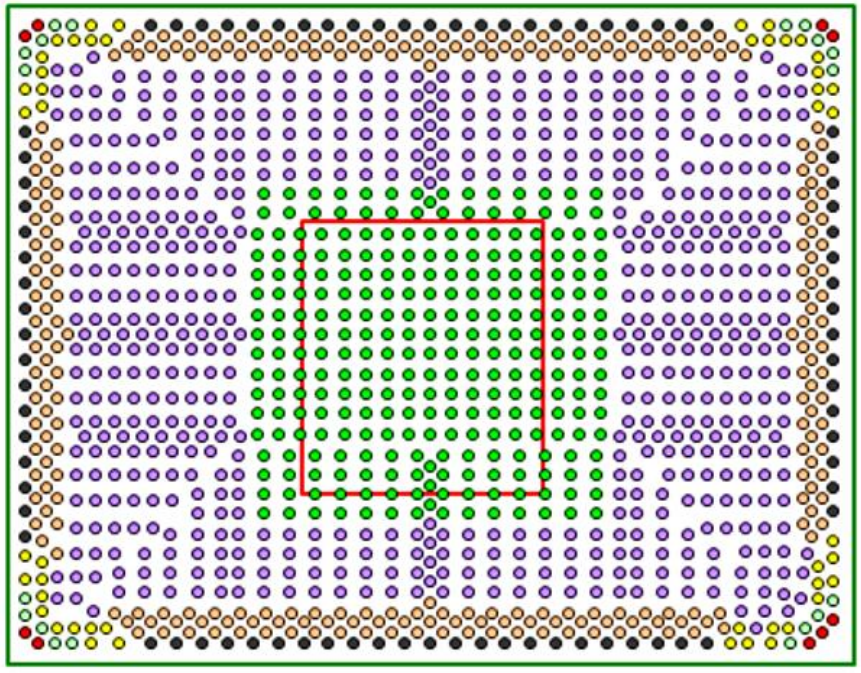
2.1 Land Pattern (Apollo Lake)



Pad Name	Count	Pad Type	Diameter	Comments
C18P5_SMD 14 (nCTF)	9	SMD	18.5 mil (470 um) pad, 14.5 mil (368 um) SRO	nCTF
C12_MD	72	MD	12 mil (305 um) pad, 16 mil (406 um) SRO	CTF
C11	251	MD / SMD	11 mil (279 um) pad, 15 mil (381 um) SRO 15 mil (381 um) pad, 11 mil (279 um) SRO	CTF
C12	631	MD / SMD	12 mil (305 um) pad, 16 mil (406 um) SRO 16 mil pad (406um), 12 mil SRO (305um)	CTF
C14	48	MD / SMD	14 mil (356 um) pad, 18 mil (457 um) SRO 18 mil (457 um) pad, 14 mil (356 um) SRO	CTF
C14 (nCTF)	19	MD	14 mil (356 um) pad, 18 mil (457 um) SRO	nCTF
C13	187	MD / SMD	13 mil (330 um) pad, 17 mil (432 um) SRO 17 mil (432 um) pad, 13 mil (330 um) SRO	CTF
OB10X13P5	79	MD	10x13.5 mil (254x343um) Oblong pad, 14x17.5 mil (356x445um) SRO	CTF
Total	1296			

The land pattern guidance provided on this page applies only to printed circuit board designs using Apollo Lake Package.

2.1 Land Pattern (Apollo Lake-I)

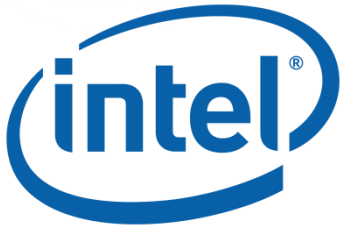


Pad Name	Count	Pad Type	Diameter	Comments
C18P5_SMD 14 (nCTF)	9	SMD	18.5 mil (470 um) pad, 14.5 mil (368.3 um) SRO	nCTF
C11	251	MD / SMD	11 mil (279.4 um) pad, 15 mil (381 um) SRO / 15 mil (381 um) pad, 11 mil (279.4 um) SRO	CTF
C12	615	MD / SMD	12 mil (304.8 um) pad, 16 mil (406.4 um) SRO / 16 mil pad (406.4um), 12 mil SRO (304.8um)	CTF
C14	48	MD / SMD	14 mil (355.6 um) pad, 18 mil (457.2 um) SRO / 18 mil (457.2 um) pad, 14 mil (355.6 um) SRO	CTF
C14 (nCTF)	19	MD	14 mil (355.6 um) pad, 18 mil (457.2 um) SRO	nCTF
C13_MD	275	MD	13 mil (330 um) pad, 17 mil (431.8 um) SRO In this region, **do not use SMD pads** – spoked or WTMD pads only to be used with trace width as follows; Pads with **1 trace**: **8 mil** trace width max Pads with **2-3 traces**: **6mil** trace width max Pads with **4 traces**: **5mil** trace width max	CTF [These pads are in the center of the package, under the die shadow]
OB10X13P5	79	MD	10x13.5 mil (254x342.9um) Oblong pad, 14x17.5 mil (355.6x444.5 um) SRO	CTF
Total	1296			

Overview – Table of Contents

This course is divided into the following modules:

Module 1: Component Attributes and Drawings	Module 2: Land Pattern (PCB Pad) Design Guidelines	Module 3: Manufacturing Guidelines	Module 4: Shipping & Handling	Module 5: Testing	Module 6: System Integration & ESD Considerations	Module 7: References
1.1 Package Attributes 1.2 Package Mechanical Drawing	2.1 Land Pattern	3.1 Manufacturing Guidelines Introduction (e.g. HT dynamic warpage values) 3.2 Critical SMT Recommendations 3.3 Solder Paste Formulation 3.4 Paste Stencil Recommendations	4.1 Processor Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements	5.1 Intel® Trusted Execution Engine Firmware Overview 5.2 Manufacturing Test Reference Flow 5.3 Manufacturing Tools Update 5.4 Download and Execute (DnX) 5.5 DnX Triggers 5.6 Intel® Integrated Sensor Solution 5.7 Types of Calibration Process	6.1 ESD Considerations 6.2 Processors General Handling Recommendations 6.3 Thermal Solution Assembly / Disassembly considerations	7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Intel® Business Advantage Portal access Information



Module 3: Manufacturing Guidelines

Manufacturing with the Intel® Mobile Products: Apollo Lake & Apollo Lake-I

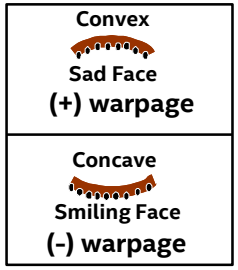
MAS Rev 2.6, Q3 2016

3.1 Manufacturing Guidelines
Introduction

- **Apollo Lake FCBGA High Temperature[1] (HT) package coplanarity (dynamic warpage) is shown below.**

High Temperature[1] (HT) FCBGA Package Coplanarity Range*		
Braswell (CHT-CR) FCBGA (mm)	**Component**	**Apollo Lake [1] FCBGA (mm)**
-0.150 to +0.135	N Series BGA Processor	-0.175 to +0.200

Sign Convention



*Values subject to change. Final values will be updated prior to QS shipments

- **Robust solder joint formation / high SMT yields are a function of many SMT parameters.**
  - Solder paste formulation, Solder paste volume, Reflow profile/environment, Pallet use, Package and Mother board warpage, etc…

Note:
- See the Manufacturing with Intel® FCBGA Components for Solder Joint Quality MAS for deeper training of warpage fundamentals.
- [1]Between lowest active temperature of the board paste to peak reflow temperature.
- [1] Value for Apollo Lake-I is TBD

3.2 Critical SMT Recommendations – Parameters

Intel Evaluated Solder Paste	No-clean, flux class ROL0 per J-STD-004. Alloy Sn/4Ag/0.5Cu or Sn/3Ag/0.5Cu. Metal content 89%.
Solder Joint Peak Temp	235°C to 250°C
Maximum Body and Substrate Temperature	Never exceed 260°C
Time Above ≥ 220°C (TAL)	40-90 sec for N_2 (0_2 < 3000 PPM) reflow 60-90 sec for Air reflow
Soak	Paste dependent. Consult paste manufacturer.
Rising Ramp Rate	Maximum 3°C per second.
Falling Ramp Rate	Maximum 3°C per second. Minimum 1°C per second from peak to 205°C.
Reflow Ambient	Intel uses Nitrogen reflow for better solderability and higher SMT yield margins (0_2 < 3000 PPM). Certified for 3x reflow
Pallet Support for Board Warpage	Clearance Recommendations: 1) Top of board height = top of pallet height (within tolerance ranges). 2) PCB to pallet edge clearance should be a minimum of 1 mm on each of the 4 sides.

Notes:

- Except for body temp, all temperatures are measured with thermo couples inside solder joints, for increased accuracy.
- This is Intel's reflow reference process practices and parameters are provided for reference purposes only, based on internal studies, and are not necessarily optimized. Mfg. processes are unique and may require unique solutions to ensure an acceptable level of quality, reliability, and mfg yield. Due to the differences in equipments and materials, process parameter modifications may be required to meet customer's quality, reliability, and manufacturing yield requirements.

3.3 Other Key Information

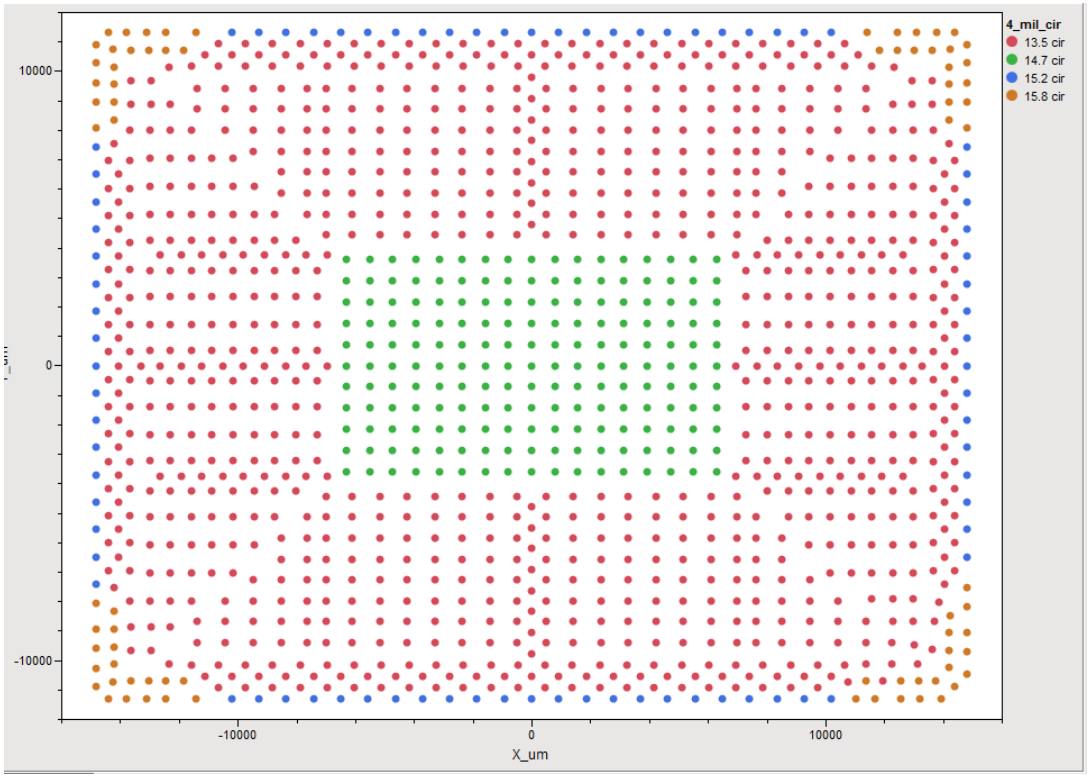
Solder Paste Print	In Alphabetical Order
Intel Evaluated Solder Pastes	Alpha OM363*, Alpha OM363H* Senju M705-GRN360-K2-VZH*, Senju M705-S101HF(N4)-S4* Shenmao PF606-P*, Shenmao PF606-P26*

Notes:

- See the Manufacturing with Intel® FCBGA Components for Solder Joint Quality MAS for deeper training of warpage fundamentals and information on solder paste performance testing.
- Disclaimer: Solder pastes results are derived from previous platform testing, which we deem comparable, and are provided for informational purposes only. Any sourcing decision is solely at the discretion of the Customer. Intel neither warrants, nor makes any representation whatsoever as to any supplier's products, including its availability, suitability, and reliability for the application for which this information is provided. Other pastes not listed above may perform better or worse based on customer SMT / board characteristics.
- *Intel, Intel® Core™ Processors, and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries. Other names and brands may be claimed as the property of others.

3.4 SMT Stencil Recommendation (Apollo Lake & Apollo Lake-I) (1 of 2) – 4 mils option

Stencil Thickness: 101.6 µm (4 mils) option Stencil Air Gap Design Rule: ≥ 177.8 µm (7 mils)		
Stencil Design (Aperture)	**Over-printing**	**Solder Paste Volume Target**
NCTF & CTF Corner Pads ● Round 15.8 mil (401.3 µm)	yes	0.0129 cu. mm (784 cu. mils)
BGA Body Pads ● Round 13.5 mil (342.9 µm),	yes	0.0094 cu. mm (573 cu. mils)
Die Shadow ● Round 14.7 mil (373.4 µm)	yes	0.0111 cu. mm (679 cu. mils)
Edge Pads ● Round 15.2 mil (386.1 µm)	yes	0.0119 cu. mm (726 cu. mils)



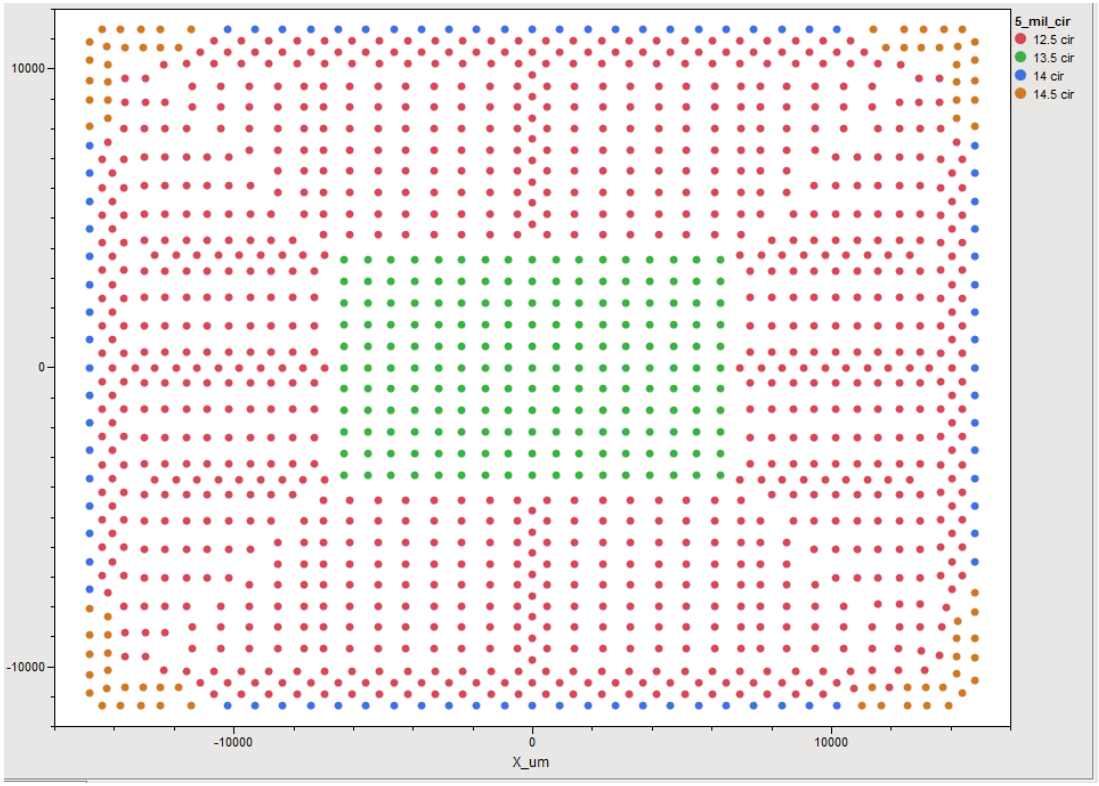
Notes:
- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- A minimum of ≥ 177.8 µm (7 mils) air gap is needed between adjacent stencil apertures to prevent solder joint bridging.
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.

3.4 SMT Stencil Recommendation (Apollo Lake & Apollo Lake-I) (2 of 2) – 5 mils option

Stencil Thickness: 127 µm (5 mils) option

Stencil Air Gap Design Rule: ≥ 177.8 µm (7 mils)

Stencil Design (Aperture)	Over-printing	Solder Paste Volume Target
NCTF & CTF Corner Pads ● Round 14.5 mil (368.3 µm)	yes	0.0135 cu. mm (826 cu. mils)
BGA Body Pads ● Round 12.5 mil (317.5 µm)	yes	0.0101 cu. mm (614 cu. mils)
Die Shadow ● Round 13.5 mil (342.9 µm)	yes	0.0117 cu. mm (716 cu. mils)
Edge Pads ● Round 14.0 mil (355.6 µm)	yes	0.0126 cu. mm (770 cu. mils)



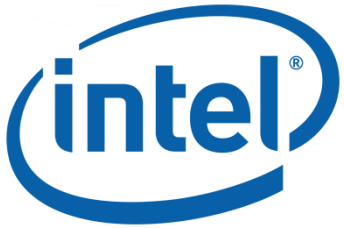
Notes:

- Reference Information Only.
- Design stencil opening to meet the theoretical volume requirements (above).
- A minimum of ≥ 177.8 µm (7 mils) air gap is needed between adjacent stencil apertures to prevent solder joint bridging.
- Always consider the impact to via capping requirements when enlarging apertures beyond 1:1.

Overview – Table of Contents

This course is divided into the following modules:

Module 1: Component Attributes and Drawings	Module 2: Land Pattern (PCB Pad) Design Guidelines	Module 3: Manufacturing Guidelines	Module 4: Shipping & Handling	Module 5: Testing	Module 6: System Integration & ESD Considerations	Module 7: References
1.1 Package Attributes 1.2 Package Mechanical Drawing	2.1 Land Pattern	3.1 Manufacturing Guidelines Introduction (e.g. HT dynamic warpage values) 3.2 Critical SMT Recommendations 3.3 Solder Paste Formulation 3.4 Paste Stencil Recommendations	4.1 Processor Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements	5.1 Intel® Trusted Execution Engine Firmware Overview 5.2 Manufacturing Test Reference Flow 5.3 Manufacturing Tools Update 5.4 Download and Execute (DnX) 5.5 DnX Triggers 5.6 Intel® Integrated Sensor Solution 5.7 Types of Calibration Process	6.1 ESD Considerations 6.2 Processors General Handling Recommendations 6.3 Thermal Solution Assembly / Disassembly considerations	7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Intel® Business Advantage Portal access Information



Module 4: Shipping & Handling

Manufacturing with the Intel® Mobile Products: Apollo Lake & Apollo Lake-I

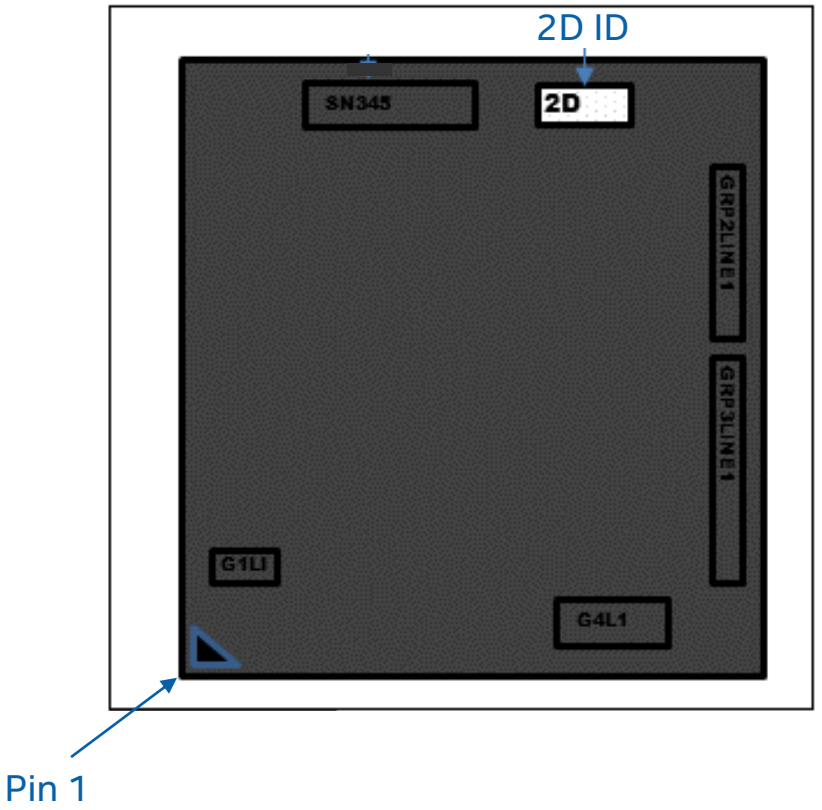
MAS Rev 2.6, Q3 2016

4.1 Package Marking

Mark Type	Mark Side
COMPONENT	TOP

Legend	Mark Text	Orient.
GRP1LINE1	◯	NORTH
GRP2LINE1	{FPO}	NORTH
GRP3LINE1	QKG4	NORTH
GRP4LINE1	{e1}	NORTH

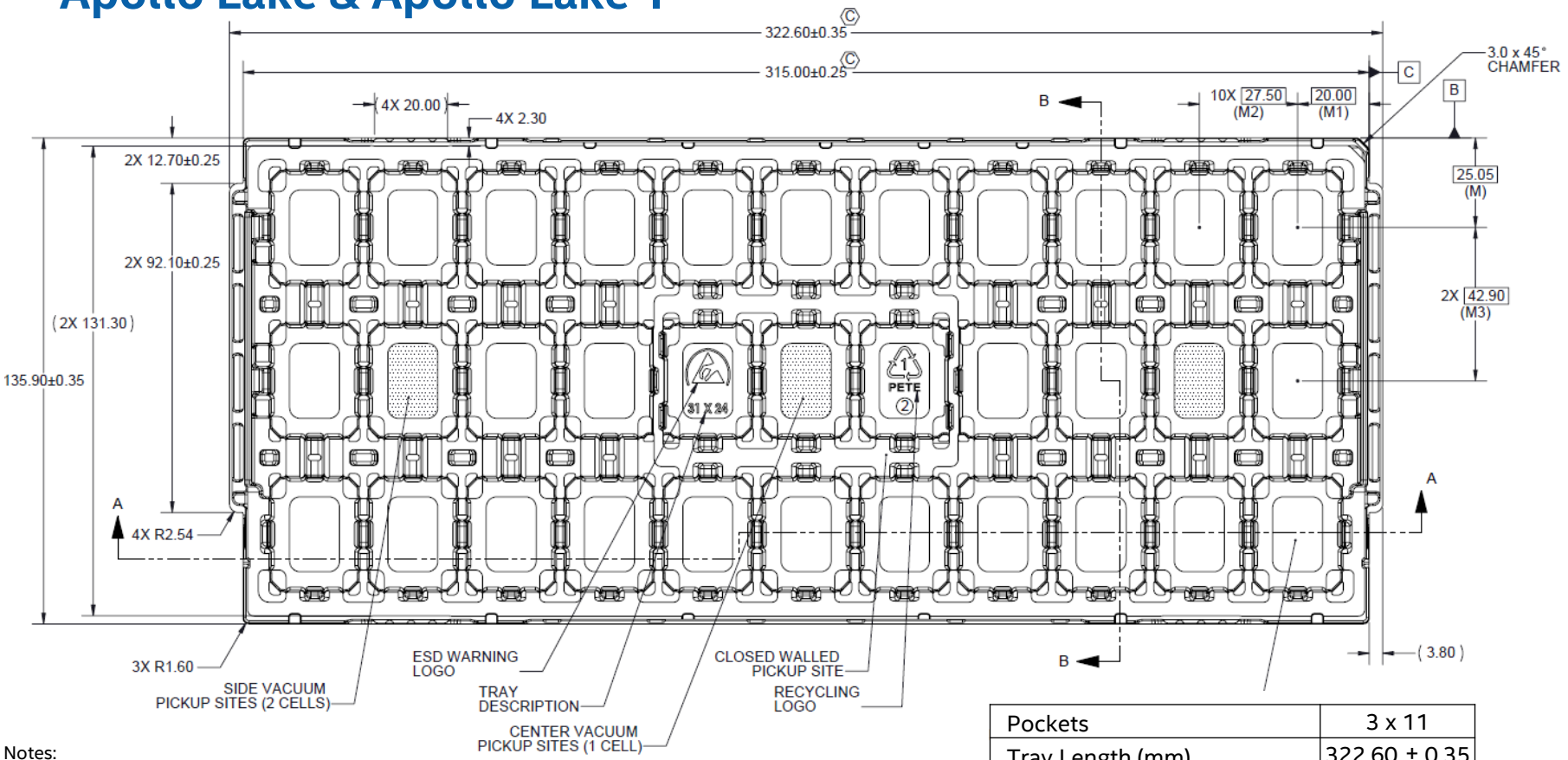
Max		
Groups	Lines	CL
4	1	8



Notes:
- For reference information only. Picture here for illustration only. Always refer to the latest product marking for final information.
- Sample marks shown here. Production markings should the same and be available in future revision.

4.2 Thermoform Tray TFT Drawing (1 of 3)

Apollo Lake & Apollo Lake-I



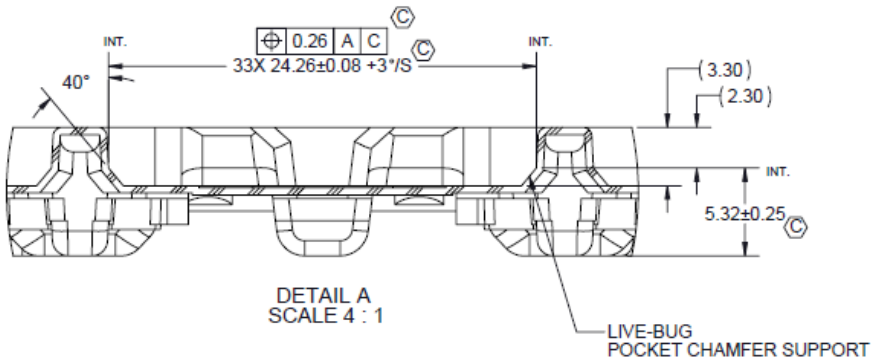
Pockets	3 x 11
Tray Length (mm)	322.60 ± 0.35
Tray Width (mm)	135.90 ± 0.35
Tray Thickness (mm)	7.62 ± 0.35
X Axis 1st Pick-Up Point (mm)	23.8
Y Axis 1st Pick-Up Point (mm)	25.05
X-Axis Pitch (mm)	27.5
Y-Axis Pitch (mm)	42.9

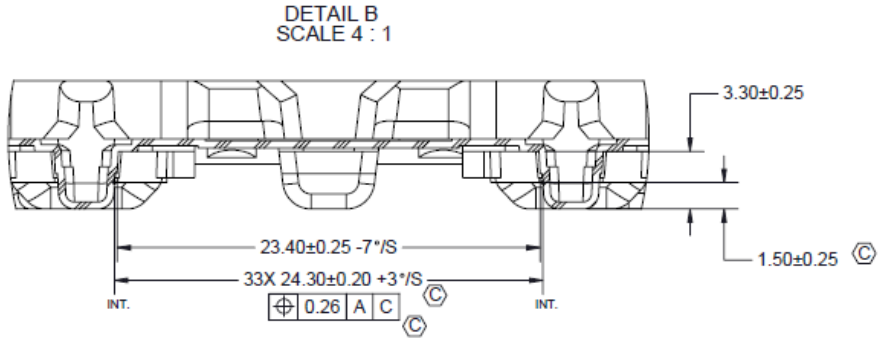
Notes:

- Information is for reference only and may change at any time.
- Intel Drawing #500275513 Rev 1
- The above Thermoform Tray (TFT) is made of Polyethylene Teraphthalate (PETE) and it is good to 50°C maximum, this is "printed" on the side of the TFT. However, a MPPO (Modified Polyhenylene Oxide) tray has a maximum temperature of 150°C can be used for baking. Our high temp tray supplier is Daewon (MPPO tray for this product has an Intel Part Number 500109920 / Daewon part number 1AK-3124-A19). Other similar trays may exist. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs.
- Daewon contact: relee@daewonusa.com

4.2 Thermoform Tray TFT Drawing (2 of 3)

Apollo Lake & Apollo Lake-I





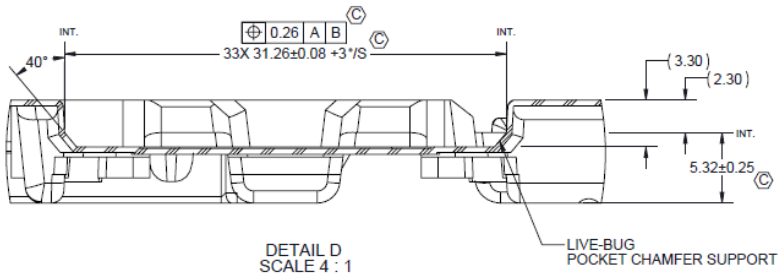
Notes:

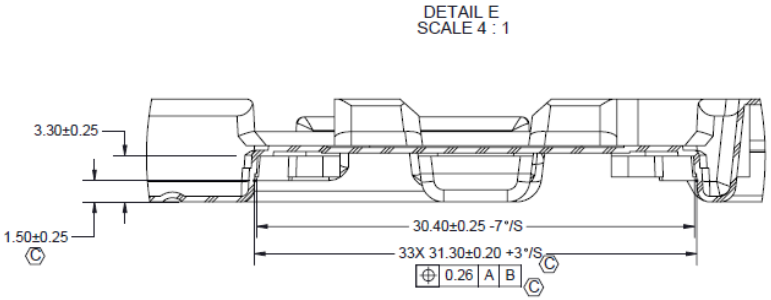
- Information is for reference only and may change at any time.
- Intel Drawing #500275513 Rev 1
- The above Thermoform Tray (TFT) is made of Polyethylene Teraphthalate (PETE) and it is good to 50°C maximum, this is "printed" on the side of the TFT. However, a MPPO (Modified Polyhenylene Oxide) tray has a maximum temperature of 150°C can be used for baking. Our high temp tray supplier is Daewon (MPPO tray for this product has an Intel Part Number 500109920 / Daewon part number 1AK-3124-A19). Other similar trays may exist. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs.
- Daewon contact: relee@daewonusa.com

Pocket X top dimension (mm)	24.26 ± 0.08
Pocket X bottom dimension (mm)	24.30 ± 0.20
Top Pocket Depth Dimension (mm)	3.30

4.2 Thermoform Tray TFT Drawing (3 of 3)

Apollo Lake & Apollo Lake-I





Notes:

- Information is for reference only and may change at any time.
- Intel Drawing #500275513 Rev 1
- The above Thermoform Tray (TFT) is made of Polyethylene Teraphthalate (PETE) and it is good to 50°C maximum, this is “printed” on the side of the TFT. However, a MPPO (Modified Polyhenylene Oxide) tray has a maximum temperature of 150°C can be used for baking. Our high temp tray supplier is Daewon (MPPO tray for this product has an Intel Part Number 500109920 / Daewon part number 1AK-3124-A19). Other similar trays may exist. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs.
- Daewon contact: relee@daewonusa.com

Pocket Y top dimension (mm)	31.26±0.08
Pocket Y bottom dimension (mm)	31.30±0.20
Bottom Pocket Depth Dimension	3.30

4.3 FCBGA Pre-SMT Bake Requirements

- **Moisture Concerns:** Moisture exposure in solder-down devices (e.g. BGA products) can lead to manufacturing defects.[1]
- **To avoid these humidity-related defects during SMT process, moisture needs to be removed from the product before SMT. As such, a pre-SMT Bake is recommended in either of these 2 conditions:**
  1. Humidity in the Moisture Barrier Bag (MBB) exceeds the level indicated by Humidity Indicator Card (HIC)[2] **or**
  2. The floor life[3] has been exceeded[4]
- **Three Pre-Solder Bake Options:[5]**
  1. High Temp Bake (using High Temp JEDEC Trays or no shipping media):
  2. Medium Temp Bake (using a Medium Temp JEDEC Trays or no shipping media.):
  3. Low Temp Bake (using Thermoform Tray or Tape & Reel media):

Package Body	Moisture Sensitivity Level (MSL)	High Temp Bake @ 125°C +10/-0 °C[6]		Medium Temp Bake @ 90°C + 8°/-0 °C ≤ 5% RH		Low Temp Bake @ 40°C +5/-0 °C ≤5% RH	
		Exceeding Floor Life by > 72 h	Exceeding Floor Life by ≤ 72 h	Exceeding Floor Life > 72 h	Exceeding Floor Life ≤ 72 h	Exceeding Floor Life by > 72 h	Exceeding Floor Life by ≤ 72 h
Thickness ≤ 1.4mm	3	Bake 9 hours	Bake 7 hours	Bake 33 hours	Bake 23 hours	Bake 13 days	Bake 9 days

Humidity Indicator Card (HIC)[1]

Desiccant

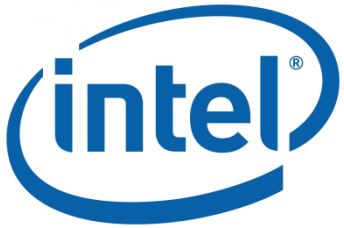
Moisture Barrier Bag (MBB)

Notes:
- [1] See JEDEC J-STD-033 for more details.
- [2] See JEDEC J-STD-033 for more details, including interpretation of HIC card.
- [3] Floor Life is defined per JEDEC STD-033 as the allowable time period between removal of moisture-sensitive devices from a moisture-barrier bag, dry storage, or dry bake and the solder process. Floor life is 168 hours at ≤30 °C/60% RH (for MSL3).
- [4] Floor life in the **open** MBB (out of MBB) depends on the product Moisture Sensitive Level (MSL). MSL rating is printed on the label of a standard intermediate box "LEVEL <N>" and on the on the label of a MBB "LEVEL <N>".
- [5] The MPPO (Modified Polyhenylene Oxide) tray for high temperature baking is bake able to 150C max. The Thermoform Tray (TFT) is made of Polyethylene Teraphthalate (PETE) and it is good to 50C MAX, this is "printed" on the side of the TFT. Intel does not endorse any specific tray supplier. Customers are encouraged to evaluate their requirements and identify tray suppliers based on their needs. For a MSL other than MSL 3, see JEDEC J-STD-033 for more details.
- [6] Baking for ≥48 hours at 125°C could lead to solder ball oxidation.

Overview – Table of Contents

This course is divided into the following modules:

Module 1: Component Attributes and Drawings	Module 2: Land Pattern (PCB Pad) Design Guidelines	Module 3: Manufacturing Guidelines	Module 4: Shipping & Handling	Module 5: Testing	Module 6: System Integration & ESD Considerations	Module 7: References
1.1 Package Attributes 1.2 Package Mechanical Drawing	2.1 Land Pattern	3.1 Manufacturing Guidelines Introduction (e.g. HT dynamic warpage values) 3.2 Critical SMT Recommendations 3.3 Solder Paste Formulation 3.4 Paste Stencil Recommendations	4.1 Processor Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements	5.1 Intel® Trusted Execution Engine Firmware Overview 5.2 Manufacturing Test Reference Flow 5.3 Manufacturing Tools Update 5.4 Download and Execute (DnX) 5.5 DnX Triggers 5.6 Intel® Integrated Sensor Solution 5.7 Types of Calibration Process	6.1 ESD Considerations 6.2 Processors General Handling Recommendations 6.3 Thermal Solution Assembly / Disassembly considerations	7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Intel® Business Advantage Portal access Information



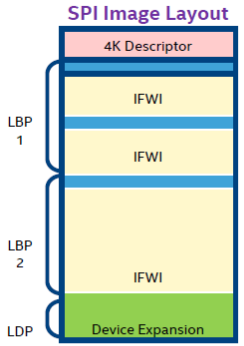
Module 5: Testing

Manufacturing with the Intel® Mobile Products: Apollo Lake & Apollo Lake-I

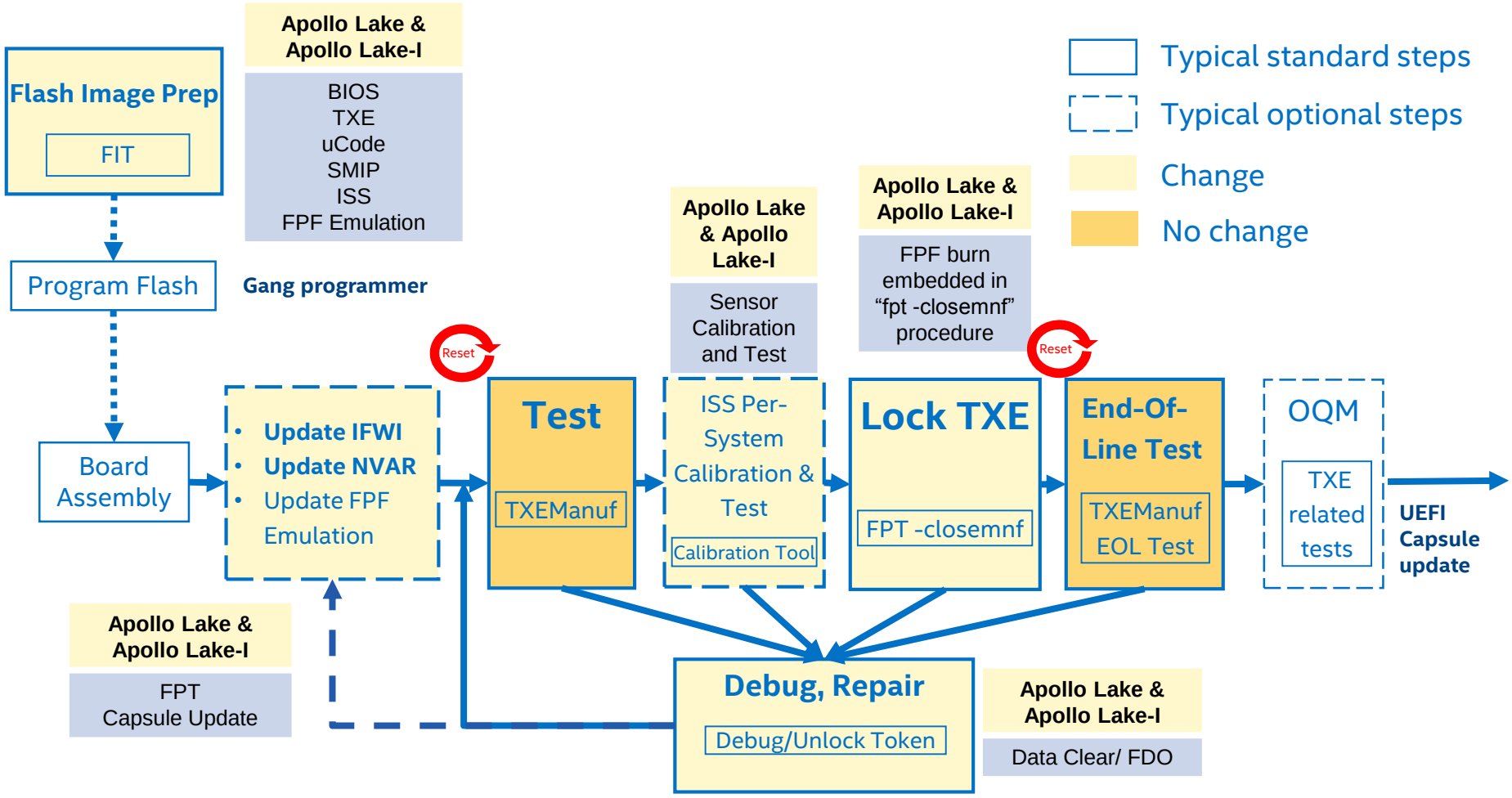
MAS Rev 2.6, Q3 2016

5.1 Intel® Trusted Execution Engine Firmware Overview

- The Intel® Trusted Execution Engine (TXE) Firmware package is a set of instructions that enable specific features to function on an SoC
- Features and capabilities are regulated thru SoC SKU and TXE FW
- Customers have to put the Intel® TXE FW code on the SPI (Serial Peripheral Interface) device
- SPI devices has a minimum flash size of 8MB



5.2 Manufacturing Test Reference Flow



Notes:

- Please refer to Manufacturing Test with Intel® Trusted Execution Engine FW MAS (Doc#: 564139) for more details on each stage
- When devices with fuses are returned to Intel, extra time can be required to determine if they are already fused or not, before analysis can begin. To avoid potential delays, keep fused and unfused parts separate, and mark them to identify them as Fused or Unfused before shipping to Intel.

5.3 Manufacturing Tools Update

Tool Name	Functionality	Usage	Changes (Intel® TXE 3.0)
Flash Image Tool (FIT)	Image Creation and SMIP Configuration	Pre-manufacturing	• Name change from FITc to FIT • New UI based on SPT • Places Tokens in IFWI • Create DnX Images • GPIO Profile Binaries • Uses Key manifests to verify sub partition binaries
Manifest Extension Utility (new)	Manifest Creation and Binary Signing	Pre- Manufacturing	• Produce a DnX image from an existing FW image
Flash Programming Tool (FPT)	• Programming Flash (SPI Only) • Setting/Retrieving Firmware Configuration • Closing Manufacturing • Provisioning RPMB	Manufacturing	• Token Management • Provision RPMB • Set global valid bit command removed • FPF interface removed
TXEManuf	• FW Validation check • FW configuration check	Manufacturing	• Configuration File format changed from txt to xml • Connectivity test on ISS • Add EOL tests for FPFs
TXEInfo	Diagnostic/Information Tool	Pre/Post Manufacturing (not an end user tool)	• Specific features change • Retrieve UEP (Unified Emulation Partition) • Add 3 columns for FPF status comparisons
Calibration Tool	Calibrate (A/G/M) sensors and test	Pre-Manufacturing (Per-Model) Manufacturing (Per-System)	• Support Full Rotation Calibration • Pre-Magnetic Environment Check • Calibration Test
Platform Flash Tool (DnX)	Download and program IFWI/OS images and Secure Tokens Tokens creation & management	Pre-Manufacturing Manufacturing Post-Manufacturing/Debug	N/A

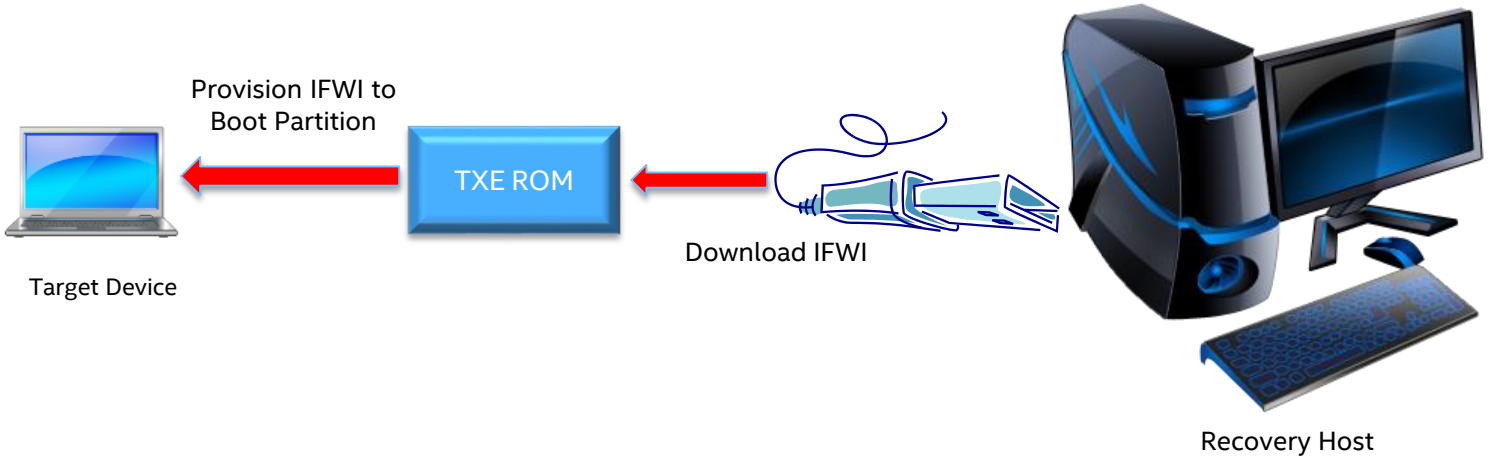
Tools are included on the Intel® TXE FW Kit released for Apollo Lake platform.
For more details on the use, please refer to System Tools User Guide

5.4 Download and Execute (DnX)

- Capability where TXE can use USB port to download content from another system
- Use the download content as an execution unit (ie. Content verification then execute) or as a data unit (ie. Writes the content to SPI like secure tokens)

Used Cases:

- Debug – Push OEM debug/Secure Token

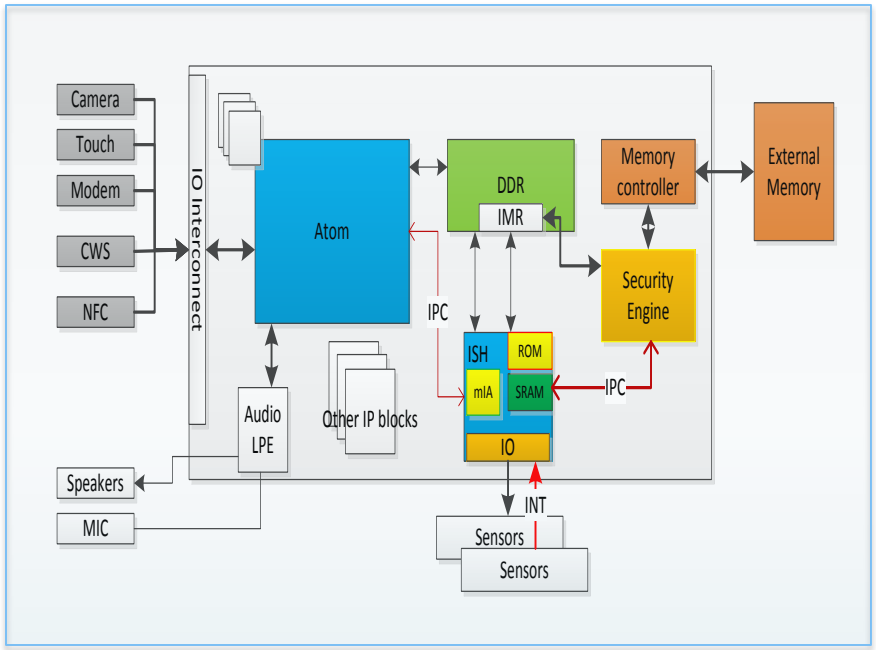


5.5 DnX Triggers

Use Case	Trigger	Intel® TXE Action Taken
Corrupted IFWI	TXE identifies IFWI corruption	TXE performs GRST and enters DnX mode
Token Push/Delete	USB cable detected in xDCI port	If USB cable detection timeout is > 0s(*) and USB cable is connected to xDCI port during boot, TXE will wait for USB enumeration from recovery host If timeout expires, TXE will continue boot
Token Push/Delete	User explicit trigger or thru HW straps	User presses the pre-defined key combinations or HW straps TXE ROM will check for HW strap If present, TXE will take DnX flow

Note (*): Default value of the timer, to enable the feature, timeout needs to be greater than 0 seconds

5.6 Intel® Integrated Sensor Solution



- Integrated Sensor Hub Hardware
- Operates together with Built-In Power Management
- Connects to CSE, IA and Memory via the main Fabric
- Supports Pre-OS boot initiated by the SEC
- BOM reduction thru integration
- Full Windows and Android compliance*
- Firmware Development Kit (FDK) for new algorithms, sensor vendors and sensor types

5.7 Types of Calibration

Full Calibration (Per-Model Calibration):

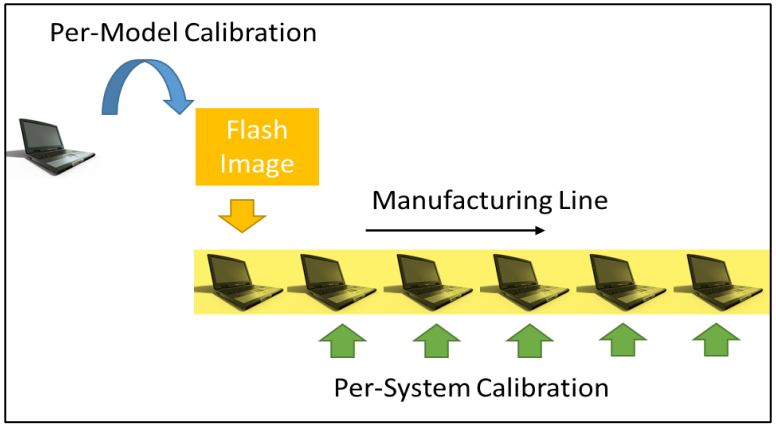
- Performed offline and measures sensor errors and determines sensor orientation based on sample of several systems (≥20)
- Assumes that the variation in systems at the manufacturing line are small and negligible
- Calibrates Accelerometer, Gyroscope, Magnetometer and Ambient Light Sensors (ALS)
- Calibration results are used to calculate average calibration file

Partial Calibration (Per-System Calibration):

- Performed at manufacturing line for all systems
- Typically required when variance on sensor errors are huge
- Performed to supplement accuracy and compensate for system variance set during full calibration
- 2 methods of Partial Calibration:
  - 4- step: calibrates accelerometer, gyroscope and ambient light sensors
  - Face-up (1-step): minimal calibration for gyroscope and accelerometer

Dynamic Calibration:

- Continuously done when the device is operational
- Adjust accumulated errors throughout the device lifetime



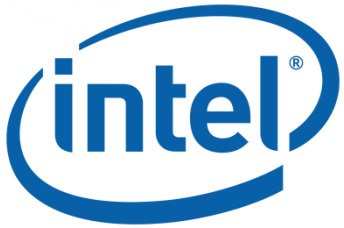
Boundary Scan Description Language (BSDL)

- The Apollo Lake BSDL is available on CDI, document reference # 563878
  - Note login require for CDI (Classified Design Information)

Overview – Table of Contents

This course is divided into the following modules:

Module 1: Component Attributes and Drawings	Module 2: Land Pattern (PCB Pad) Design Guidelines	Module 3: Manufacturing Guidelines	Module 4: Shipping & Handling	Module 5: Testing	Module 6: System Integration & ESD Considerations	Module 7: References
1.1 Package Attributes	2.1 Land Pattern	3.1 Manufacturing Guidelines Introduction (e.g. HT dynamic warpage values)	4.1 Processor Package Markings	5.1 Intel® Trusted Execution Engine Firmware Overview	6.1 ESD Considerations	7.1 Reference Documents
1.2 Package Mechanical Drawing		3.2 Critical SMT Recommendations	4.2 Component Packaging	5.2 Manufacturing Test Reference Flow	6.2 Processors General Handling Recommendations	7.2 Intel® Learning Network access Information
		3.3 Solder Paste Formulation	4.3 FCBGA Pre-SMT Bake Requirements	5.3 Manufacturing Tools Update	6.3 Thermal Solution Assembly / Disassembly considerations	7.3 Intel® Business Advantage Portal access Information
		3.4 Paste Stencil Recommendations		5.4 Download and Execute (DnX)		
				5.5 DnX Triggers		
				5.6 Intel® Integrated Sensor Solution		
				5.7 Types of Calibration Process		



Module 6: System Integration & ESD Considerations

Manufacturing with the Intel® Mobile Products: Apollo Lake & Apollo Lake-I

MAS Rev 2.6, Q3 2016

Acronyms Found in this Module

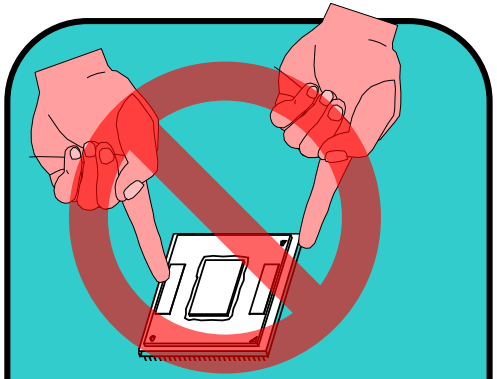
BKM	Best Known Method
CDM	Charge Device Model
ESD	Electro-Static Discharge
FACR	Functional Analysis Correlation Request
GP I/O	General Purpose I/O Pin
HBM	Human Body Model
LVDS	Low Voltage Differential Signaling

6.1 ESD Considerations
Apollo Lake Platform Component ESD Goal

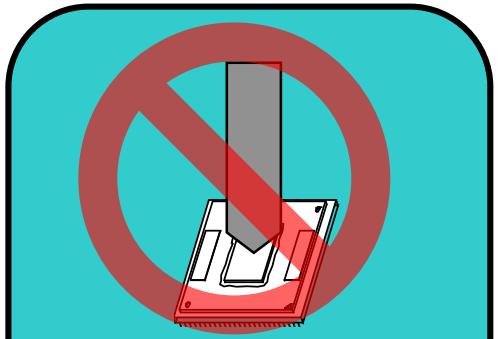
Intel® Atom™ processor x5-E8000 Platform Components[1]	Attributes		Apollo Lake & Apollo Lake-I Platform Components	
Stress Condition	**Stress Model**	**Spec #**	**Stress Condition**	**Test Results[2]**
±1000 V	ESD – Human Body Model	JS-001-2014	±1000 V	Pass
±500 V	ESD – Charged Device Model (Non-Performance Pins)	JESD22-C101	±500 V	Pass
±250 V	ESD – Charged Device Model (Performance Pins)	JESD22-C101	±250 V	Pass
1.5x VCC	Latch-up – Vcc	JESD78	1.5x VCC	Pass
Ipin = ±100 mA	Latch-up – I/O	JESD78	Ipin = ±100 mA	Pass

Notes:
- [1]Formally called Braswell
- [2]Testing will include the Apollo Lake Platform FCBGA processors and chipset.
- Reference Only. Refer to the latest rev of the Manufacturing with Intel® Products: ESD/EOS Awareness & Preparedness MAS.

6.2 Processors General Handling Recommendations

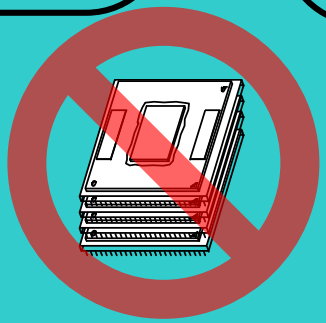


Avoid touching or pressing on the silicon die.

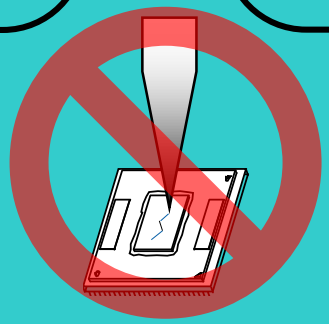


Avoid putting excessive force on the die.

Avoid introducing foreign material onto die surface.



Avoid smashing the balls, don't coin-stack units.

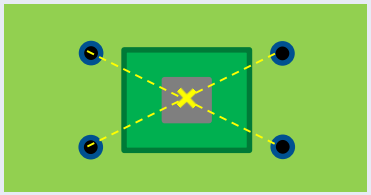


Avoid scratching die.

6.3 Apollo Lake Considerations During Thermal Solution Assembly/Disassembly

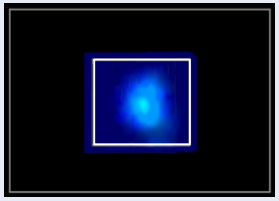
Design to ensure static compressive load at CPU die center after thermal solution assembly/disassembly.

√



Ensure the load is distributed on the dies during testing and thermal solution assembly/disassembly of Intel Component.

√

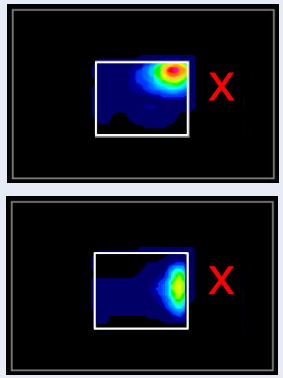


Use Module 4 in this document for package handling best practices.

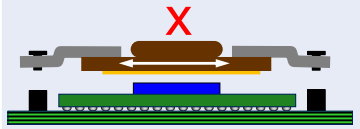
Collect mechanical quality and reliability validation data to risk assess each thermal solution design.

Avoid static load concentration at die edge or die corners after thermal solution assembly/disassembly. This can lead to die damage.

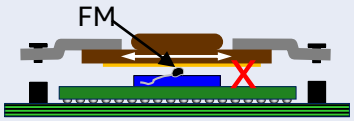
Avoid load concentration at die edge or die corners during testing and thermal solution assembly/disassembly of Intel Component. This can lead to die damage. Some of the factors influencing load magnitude and distribution are:
1) Loading Center, 2) TIM type, 3) excess warpage of cold plate, 4) misaligned TIM dispense from die areas, 5) non-SOP screw assembly/disassembly sequence, 6) thermal solution tilting during assembly/disassembly.



Avoid sliding or dynamic lateral movement or rotational movement of the thermal solution on the die during assembly/disassembly. This can lead to die damage.



Avoid foreign material (FM) deposited on the die/ thermal solution surfaces, that can lead to load concentration during thermal solution assembly/disassembly. This can lead to die damage.

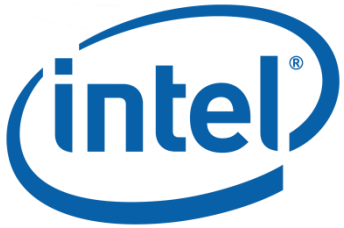


Please note that all the diagrams are example images and not inclusive and representative of all possible scenarios.

Overview – Table of Contents

This course is divided into the following modules:

Module 1: Component Attributes and Drawings	Module 2: Land Pattern (PCB Pad) Design Guidelines	Module 3: Manufacturing Guidelines	Module 4: Shipping & Handling	Module 5: Testing	Module 6: System Integration & ESD Considerations	Module 7: References
1.1 Package Attributes 1.2 Package Mechanical Drawing	2.1 Land Pattern	3.1 Manufacturing Guidelines Introduction (e.g. HT dynamic warpage values) 3.2 Critical SMT Recommendations 3.3 Solder Paste Formulation 3.4 Paste Stencil Recommendations	4.1 Processor Package Markings 4.2 Component Packaging 4.3 FCBGA Pre-SMT Bake Requirements	5.1 Intel® Trusted Execution Engine Firmware Overview 5.2 Manufacturing Test Reference Flow 5.3 Manufacturing Tools Update 5.4 Download and Execute (DnX) 5.5 DnX Triggers 5.6 Intel® Integrated Sensor Solution 5.7 Types of Calibration Process	6.1 ESD Considerations 6.2 Processors General Handling Recommendations 6.3 Thermal Solution Assembly / Disassembly considerations	7.1 Reference Documents 7.2 Intel® Learning Network access Information 7.3 Intel® Business Advantage Portal access Information



Module 7: References

Manufacturing with the Intel® Mobile Products: Apollo Lake & Apollo Lake-I

MAS Rev 2.6, Q3 2016

7.1 Reference Documents

The reader of this document should also be familiar with the material and concepts presented in the following documents:

Title	Intel® Learning Network [1]	CDI Document Number[2]
Manufacturing with the Intel® Mobile Products: Apollo Lake & Apollo Lake-I [**THIS DOCUMENT**]	resource_00014654	561676
Manufacturing with Intel® FCBGA Components for Solder Joint Quality MAS	resource_00007663	506474
Manufacturing Test with Intel® Trusted Execution Engine (TXE) 3.0 for Apollo Lake and Broxton Platforms	resource_00014853	564139
Apollo Lake Platform – Thermal Mechanical Design Guide	NA	559048
Intel® Ball Grid Array Component Board Level Adhesive MAS	resource_00007671	506556
Manufacturing with Intel® Products: ESD/EOS Awareness & Preparedness MAS	resource_00006787	515426
Intel® Manufacturing with Intel Components Strain Measurement for Circuit Board Assembly MAS	course_00010136	550235
Manufacturing with Intel® Products: Rework Guidance for Ball Grid Array (BGA), Package on Package (PoP), and Sockets	resource_00009699	541231

Notes:

- [1]Intel® Learning Network - http://learn.intel.com
- [2]The CDI # can be searched for under Documents Tab in the Intel® Business Portal (IBP) - https://businessportal.intel.com
- Contact your Intel representative for all document access questions.

7.2 How CNDA* Customers Access Documents from the Intel® Learning Network

1. Open your internet browser and go to http://learn.intel.com
2. Either log in using an existing account, or choose and 'click here' to setup a new account.
3. Register your new Intel® Learning Network account by setting up a username and password; complete the registration and profile requirements. Please use your company email address as part of the registration process.
4. Contact your local Intel representative for training on how to access Manufacturing Advantage Services (MAS) collaterals (such as this document) on the Intel® Learning Network. By default, you may not be able to see all MAS collaterals until access is provided by your Intel representative.

If you do not know your local Intel representative, and have questions about accessing MAS materials, please contact us by emailing us at:

ask.quality@intel.com

* CNDA = Corporate Non-Disclosure Agreement

7.3 How CNDA Customers Access Documents from the Intel® Business Portal

- Intel® Business Portal is an external secure portal that provides Intel customers with customized access to confidential Intel information and applications.
- To access documents in Intel® Business Portal, please contact your Intel Field Representative.
- Visit https://businessportal.intel.com

Note: CNDA = Corporate Non-Disclosure Agreement.

CME
Customer Manufacturing Enabling
Manufacturing Advantage Services