Table 45-1. CFL Interface Signals List (Sheet 4 of 4)

Name	Source	Destination	Description
CPU_C10_GATE#	CPU	Platform	Power gating control to turn off VCCSTG, VCCIO and VCCPLL_OC in C10

Table 45-2. CFL Power Sequence Related Power Rails

Name	Source	Destination	Description
VCCRTC	Platform	PCH	3.05-V supplies for PCH RTC Well. This power is not expected to be shut off in any of the sleep states unless the RTC battery is removed or completely drained.
VCCDSW_3p3	Platform	PCH	3.3-V supply for Deep Sx wells. If Deep Sx is not supported on the platform, tie to VCCPRIM_3p3
VCCPRIM_1p0/1p8/3p3	Platform	PCH	PCH I/O and Misc rails 1.0/1.8/3.3V (Primary Well)
VCCSPI	Platform	PCH	1.8V/3.3-V supply for the SPI IO. This rail must be powered when VCCPRIM is powered.
VCC	Platform	Processor	Processor core rail
VCCST	Platform	Processor	Sustain voltage for processor in Standby modes
VCCPLL	Platform	Processor	CPU PLL power rails
VCCPLL_OC	Platform	Processor	CPU digital PLL power rails
VCCGT	Platform	Processor	Sliced graphics power rail
VCCGTx[1]	Platform	Processor	Unsliced graphics power rail
VCCIO	Platform	Processor	IO power rail
VDDQ	Platform	Processor	CPU Memory power rail, voltage dependent on memory technology
VPP	Platform	Processor	CPU Memory power rail, voltage dependent on memory technology
VCCSA	Platform	Processor	System Agent power rail

45.3 Power States

Table 45-3. System with M3 State Supported (Sheet 1 of 2)

Rails	S0/M0	S0ix/ M-off[16]	S3/M3	S3/M-off	S4 & S5/M3	S4 & S5/ M-off	Deep S3	Deep S4/ S5	G3[1]
RTC Well	ON	ON	ON	ON	ON	ON	ON	ON	ON
3.3V_DSW	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	ON	ON	ON	ON	ON	ON	OFF	OFF	No Power
V3.3A	ON	ON	ON	ON	ON	ON	OFF	OFF	No Power
V1.8A	ON	ON	ON	ON	ON	ON	OFF	OFF	No Power
V1.0A	ON	ON	ON	ON	ON	ON	OFF	OFF	No Power
V3.3M[3]	ON	OFF	ON[11]	OFF	ON[11]	OFF	OFF	OFF	No Power
V1.8M[3]	ON	OFF	ON[11]	OFF	ON[11]	OFF	OFF	OFF	No Power
VDDQ	ON	ON	ON	ON	OFF	OFF	ON	OFF	No Power
V2.5U	ON	ON	ON	ON	OFF	OFF	ON	OFF	No Power
VCCST[13]	ON	ON	ON [19]	ON [19]	OFF[5]	OFF[5]	OFF	OFF	No Power
VCCPLL	ON	ON	ON[7, 19]	ON[7, 19]	OFF[5]	OFF[5]	OFF[5]	OFF	No Power

Table 45-3. System with M3 State Supported (Sheet 2 of 2)

For Devices that should be turned off completely when entering sleeping mode

Rails	S0/M0	S0ix/ M-off[16]	S3/M3	S3/M-off	S4 & S5/M3	S4 & S5/ M-off	Deep S3	Deep S4/ S5	G3[1]
V3.3S	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCPLL_OC[13]	ON	OFF[17]	ON[8, 19]	ON[8, 19]	OFF	OFF	OFF[8]	OFF	No Power
VCC	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCGT/VCCGTx	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCIO	ON	OFF[17]	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCSA	ON	OFF[17]	OFF	OFF	OFF	OFF	OFF	OFF	No Power

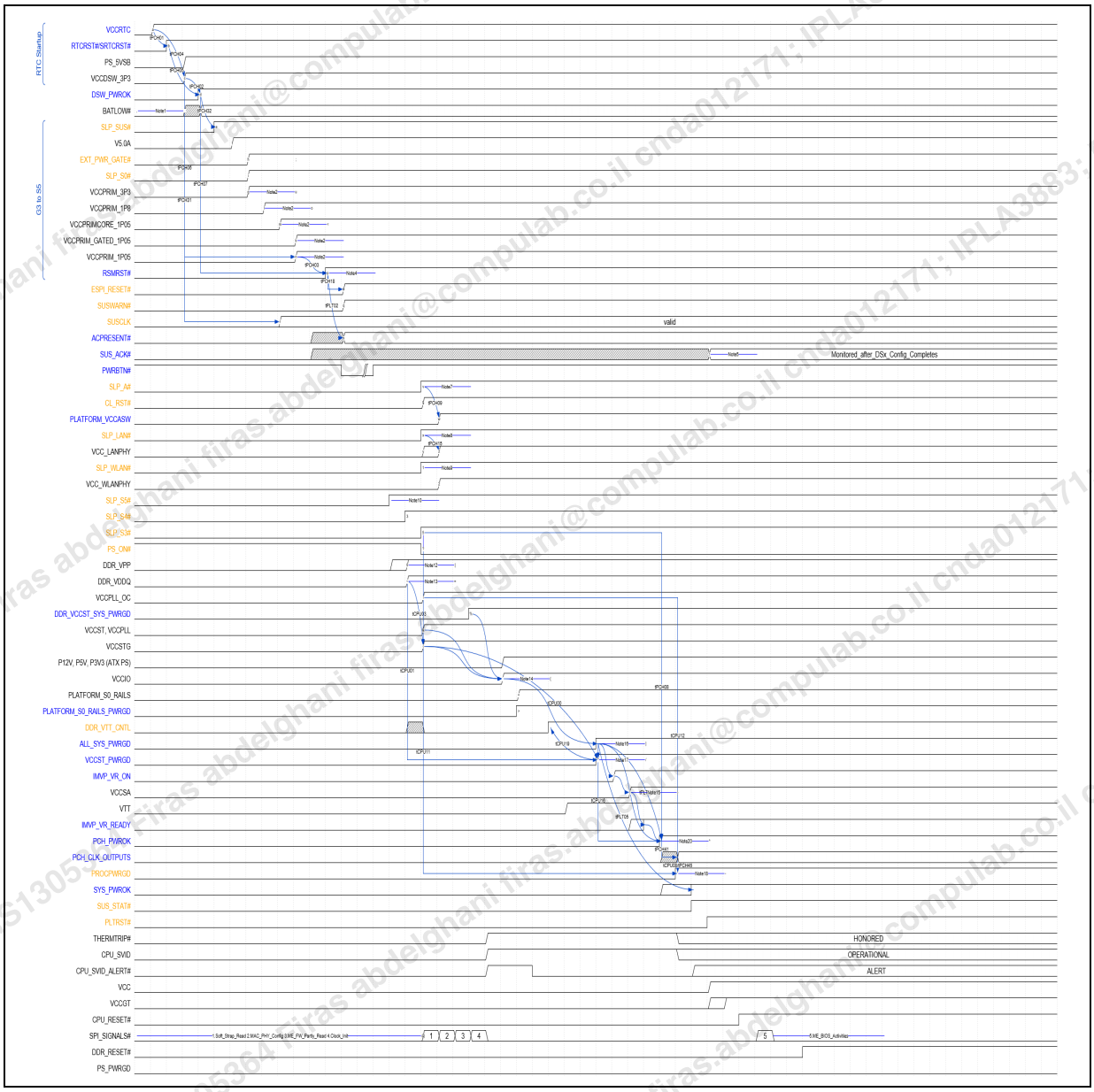
Notes:
1. The state of the system without RTC well powered can also be considered G3.
2. NA
3. V3.3M and V1.8M are platform rails used by external devices which ME operates during Sx/M3 states. These rails are not use directly by the CPU/PCH, and are not present on non-M3 supported systems
4. NA
5. VCCST, VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 46, "Platform Debug and Test Hooks".
6. NA
7. VCCPLL is allowed to be OFF in this power state, but it is generally assumed to be ON since it is powered from the same source as VCCST. VCCPLL should never be ON while VCCST is OFF
8. VCCPLL_OC is allowed to be turned off during S3 if it is not powered directly from VDDQ
9. NA
10. For no M3 support on external devices, V3.3M/V1.8M will be OFF in Sx/M3
11. VCCOPC_1p8 may be left on in Sx with minimal leakage.
12. NA
13. Assume SLP_S0# and CPU_C10_GATE# have asserted from the PCHThis supply is expected to be OFF during states where SLP_S0# is asserted. It may be left on during this condition, but the SoC will not achieve it's lowest power consumption. Specific power up latencies apply when exiting this stateVCCST should be "on whenever VCCPLL_OC is "on". VCCPLL_OC must be "off" whenever VCCST is "off", pay special attention particularly for systems supporting DS3.
14. For additional power savings in S3, refer Section 45.5, "Additional Power Optimizations with Respect to VCCST Rail in S3"

45.4 Power Sequencing Timing Diagrams—Legacy Signals

Table 45-4. Legend for Signals in Transition Waveforms

Color/Legend	Comments
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform
Signal Names	Voltage rails or chip-to-chip buses
Grey Highlight	Indicates unstable state

Figure 45-3. Timing Diagram for G3 to S0/M0 [Deep Sx Platform] (Sheet 1 of 2)



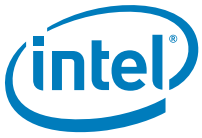


Figure 45-3. Timing Diagram for G3 to S0/M0 [Deep Sx Platform] (Sheet 2 of 2)

Notes:

1. PCH will sample BATLOW# on the rising edge of DSW_PWROK for DSx Systems
2. Refer section TBD details on PCH prime rail-to-rail power and power down dependencies
3. For a DSx system, PCH will ignore SUSACK# until after SUSWARN# is valid
4. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
5. On first exit from G3, SLP_A# de-asserts with SLP_S3# de-assertion
6. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#
7. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
8. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
9. VCCST and VCCPLL can remain powered during S4 and S5 pwr states for board VR optimization. VCCST may also remain powered in S4 and S5 for debug purposes. Refer to debug port design guide for more details.
10. Only required with LPDDR3 and DDR4 memory configurations
11. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
12. VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps.
13. IMVP VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
14. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
15. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD and / or SLP_S3# in their generation. This ensures during failure events, both signals de-assert at the same time
16. NA
17. When “Power Button” is the trigger for wake or sleep event for the system
18. The Platform should ensure that PCH_PWROK does not glitch when RSMRST# is de-asserted
19. PS has a wide range of specifications, which may affect boot latency
20. Use of DDR_VTT_CNTL to control VTT power gate is optional for additional power savings in Idle power states. If not used, VTT should be controlled by SLP_S3#

power up

Figure 45-4. Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)

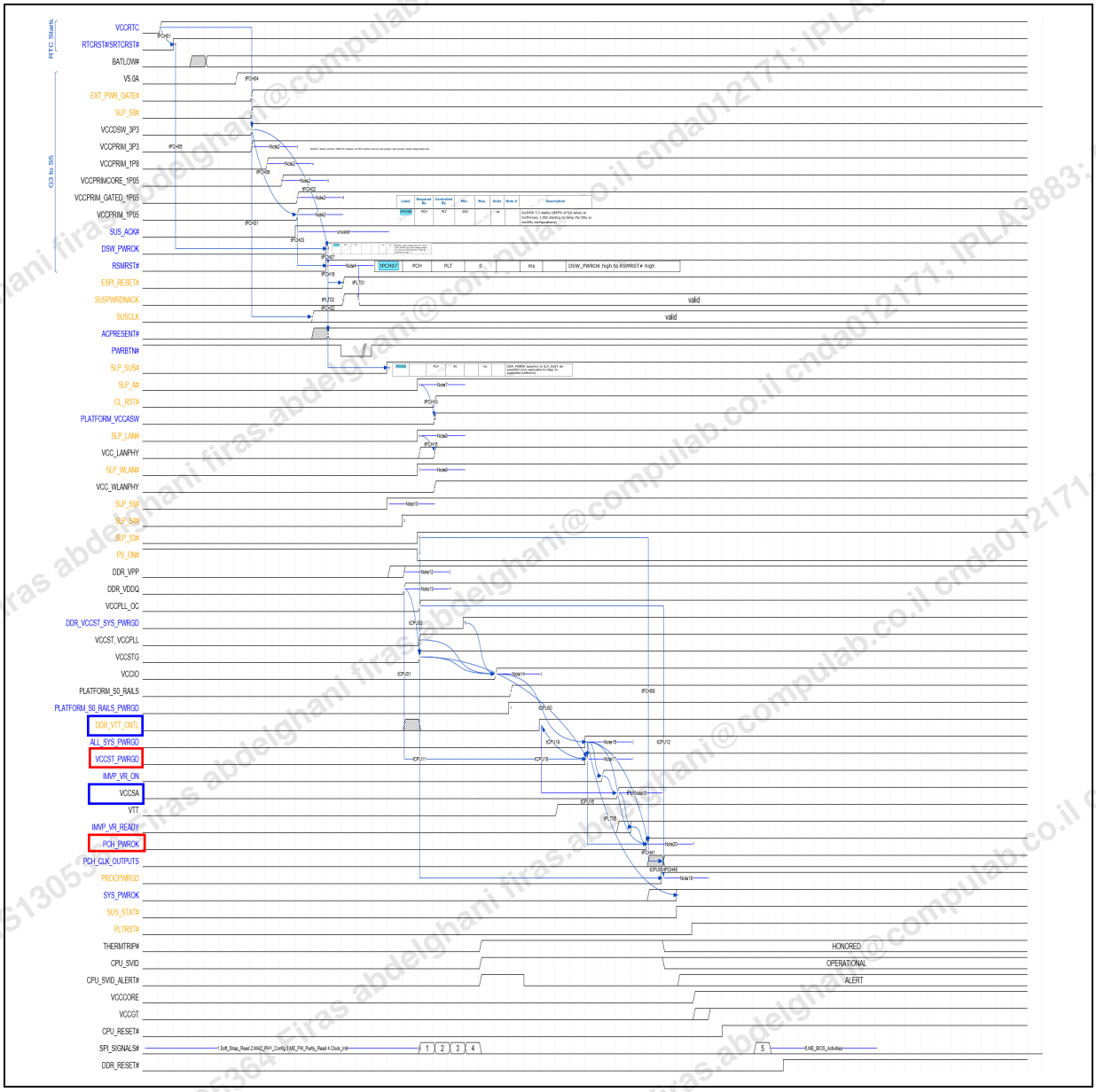


Figure 45-4. Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 2 of 2)

Notes:

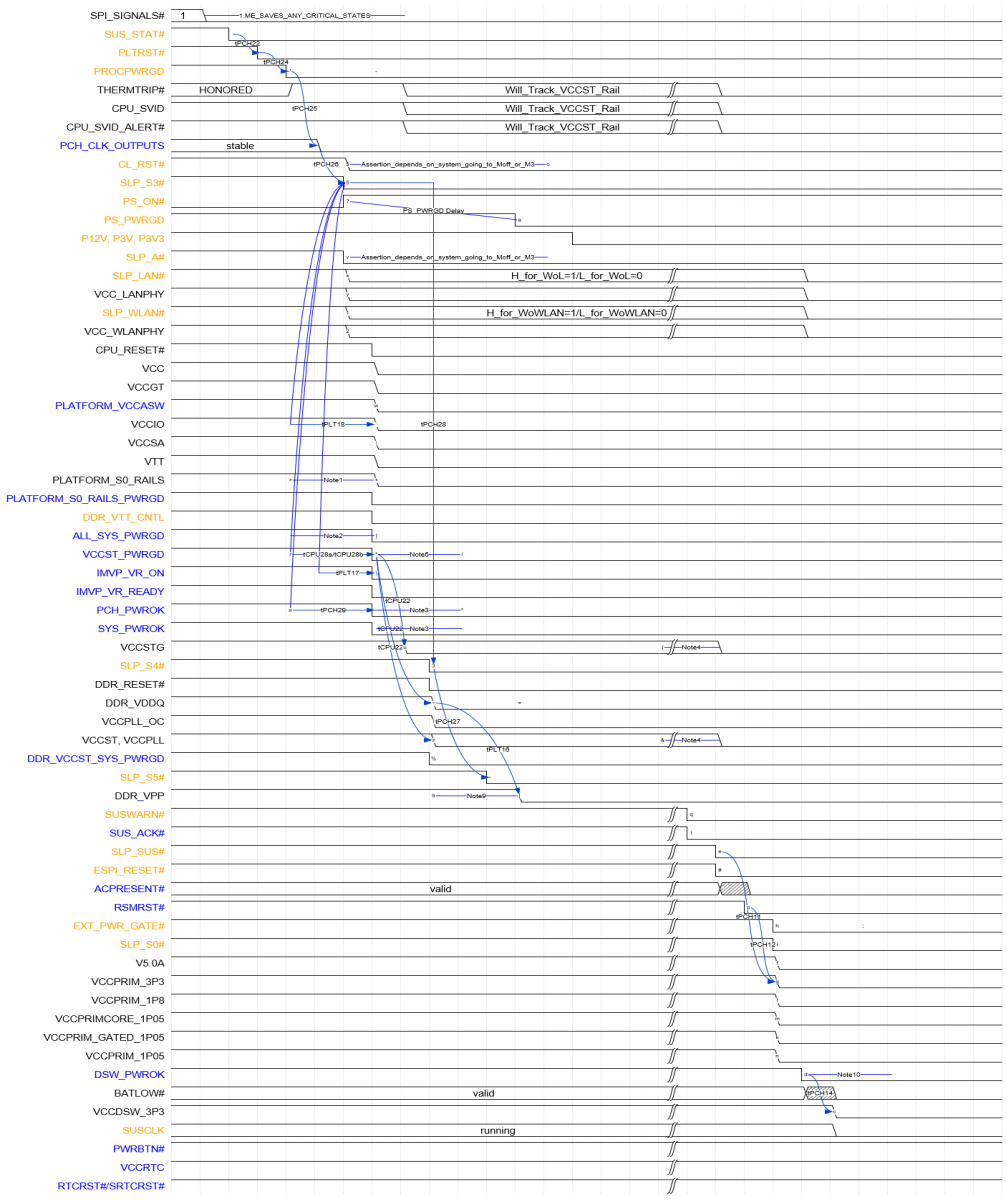
1. SLP_SUS# is ignored in Non-DSx systems
2. Refer section TBD for details on PCH prime rail-to-rail power and power down dependencies
3. For a non-DeepSx system DSW_PWROK and RSMRST# go high at the same time (connected on board)
4. For a non-DeepSx system SUS_ACK# will rise with prime voltage rail powering the VCCPGPPA power pin due to weak internal pull-up.
5. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
6. On first exit from G3, SLP_A# de-asserts with SLP_S3# de-assertion
7. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#
8. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
9. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
10. VCCST and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST may also remain powered in S4 and S5 for debug purposes. Refer to debug port design guide for more details.
11. Only required with LPDDR3 and DDR4 memory configurations
12. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
13. VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps
14. IMVP VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
15. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
16. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD and / or SLP_S3# in their generation. This ensures during failure events, both signals de-assert at the same time
17. NA
18. When "Power Button" is the trigger for wake or sleep event for the system
19. The Platform should ensure that PCH_PWROK does not glitch when RSMRST# is de-asserted
20. PS has a wide range of specifications, which may affect boot latency
21. Use of DDR_VTT_CNTL to control VTT power gate is optional for additional power savings in Idle power states. If not used, VTT should be controlled by SLP_S3#

Additional Notes:

The state of the SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.

- SUSPWRDNACK
  - — *Platform not supporting M3* - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3. Else, EC has an option to do whatever it wants with the SUS Rails
  - — *Platform supporting M3* - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3 **OR** SLP_A# is de-asserted **OR** it is the first 200mS after SUS Rails power has been applied. Else, EC has an option to do whatever it wants with the SUS Rails
- Primary rails and Deep Sx Rails should **never** be active while VccRTC rail is inactive.

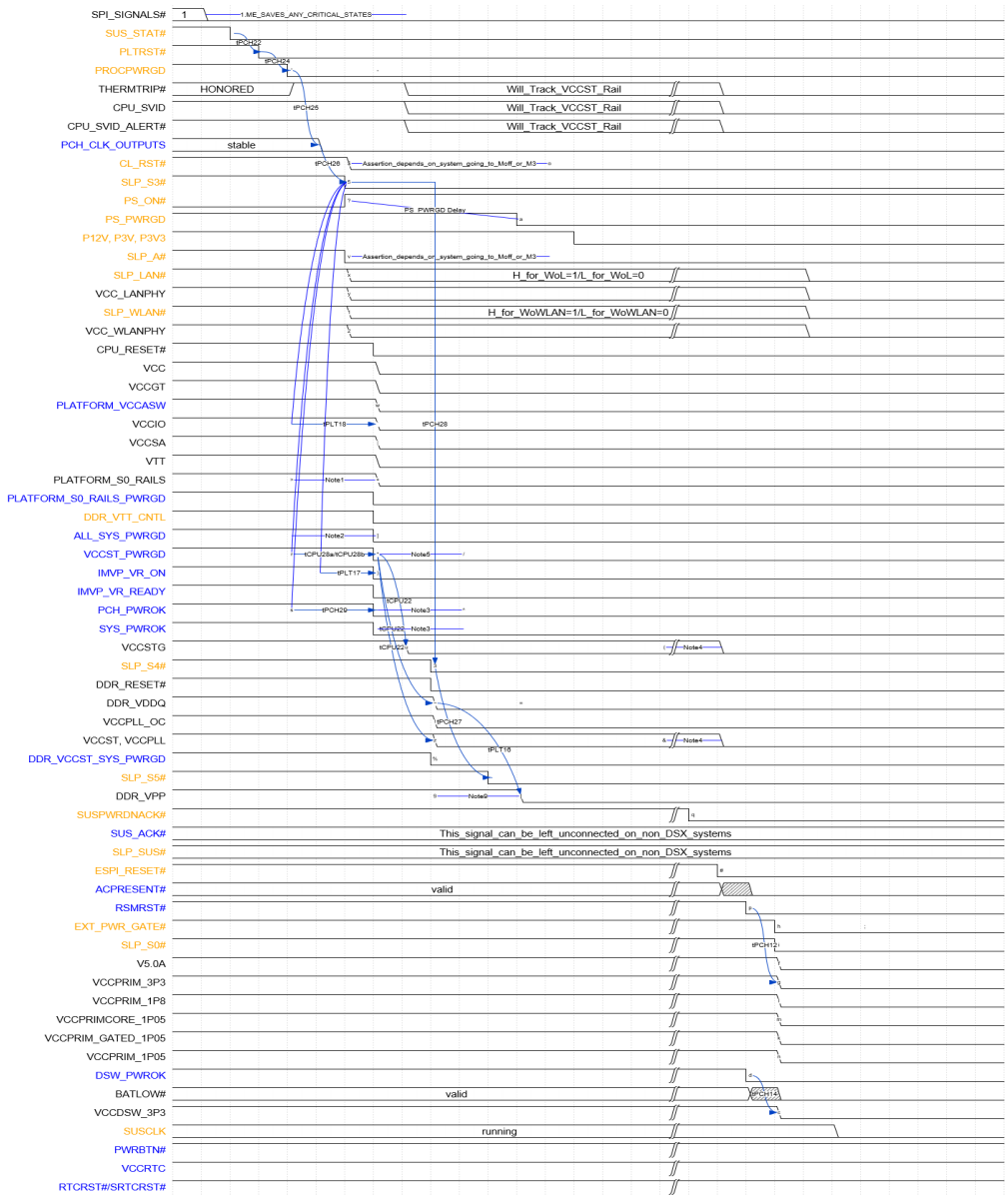
Figure 45-5. Timing Diagram for S0/M0 to G3 [Deep Sx Platform]



Notes:

1. These are all the processor S0 non-Core rails. Includes the rails like 3.3-V/5-V platform rails, etc.
2. This represents the overall Power-Good signal including the platform rails mentioned in Note (1)
3. Signal may drop before or after SLP _S4# / SLP_S5 # / DDR_RESET# assertion
4. VCCST and VCCPLL may remain powered during Sx power states for Debug support and platform VR optimization. Platform designers will need to account for proper power rail management with external devices and circuity to avoid leakage path scenarios.
5. VCCST_PWRGD signal must deassert in all Sx / DSx states, regardless of the status of the VCCST rail
6. PCH waits for SUS _ACK# to deassert before proceeding with Deep S4/S5 flow. If SUSWARN#/SUS_ACK # handshake is not used, these signals are tied on the board
7. High for WoL=1, Low forWoL=0
8. High for WoWLAN =1, Low for WoWLAN = 0
9. Present on LPDDR3 and DDR4 systems only. Must ramp down ***AFTER*** VDDQ has ramped down
10. Refer to Section 45.6.2, "RSMRST#/DSW_PWROK Special Considerations"

Figure 45-6. Timing Diagram for S0/M0 to G3 [Non-Deep Sx Platform]



Notes:

1. These are all the processor S0 non-Core rails. Includes the rails like 3.3-V/5-V platform rails, etc.
2. This represents the overall Power-Good signal including the platform rails mentioned in Note (1)
3. Signal may drop before or after SLP _S4# / SLP_S5 # / DDR_RESET# assertion
4. VCCST and VCCPLL may remain powered during Sx power states for Debug support and platform VR optimization. Platform designers will need to account for proper power rail management with external devices and circuity to avoid leakage path scenarios.
5. VCCST_PWRGD signal must de-assert in all Sx / DSx states, regardless of the status of the VCCST rail
6. PCH waits for SUS _ACK# to deassert before proceeding with Deep S4/S5 flow. If SUSWARN#/SUS_ACK # handshake is not used, these signals are tied on the board
7. High for WoL=1, Low forWoL=0
8. High for WoWLAN =1, Low for WoWLAN = 0
9. Present on LPDDR3 and DDR4 systems only. Must ramp down ***AFTER*** VDDQ has ramped down

Figure 45-7. Timing Diagram for Warm Reset (Host Partition Reset w/o Power Cycle)

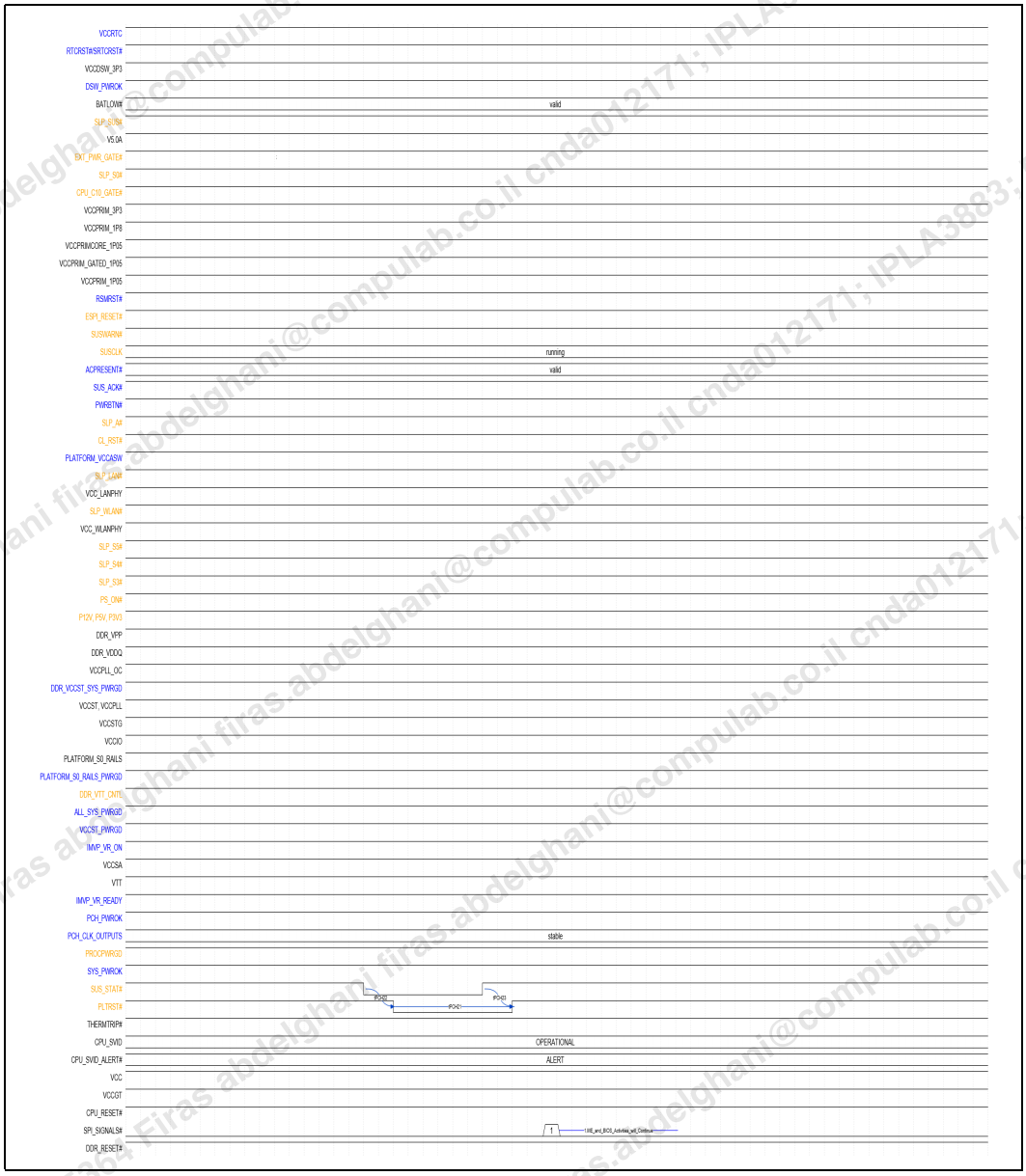
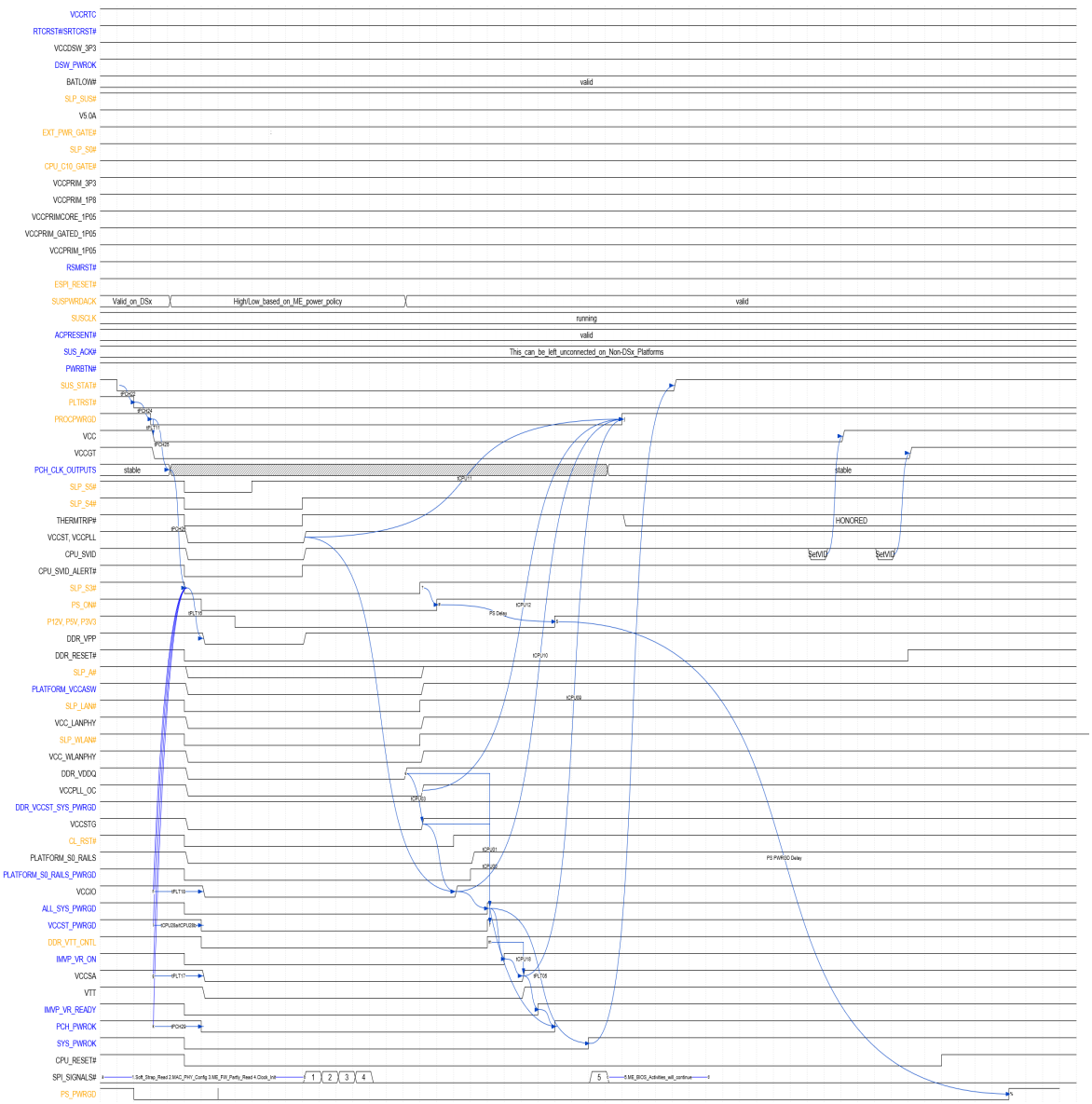


Figure 45-8. Timing Diagram for Cold Reset (Host Partition Reset w/ Power Cycle) and Global Reset [Non-Deep Sx Platform]



Notes:

1. Present on LPDDR3 and DDR4 systems only. Must ramp down AFTER VDDQ has ramped down
2. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
3. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may end up after SLP_S3# de-assertion due to VR ramp timing and configuration
4. VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps
5. IMVP VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
6. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
7. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time

45.4.1 Power Sequencing Timing Requirements

The following table defines the timing parameters used in the timing diagrams in previous sections. The timing parameters are put into three categories: tCPU, tPCH, and tPLT. tCPU parameters are mostly required by the processor, tPCH parameters are required or controlled by the PCH, and tPLT parameters are mostly controlled by the platform.

Table 45-5. Platform Sequencing Timing Parameters (Sheet 1 of 7)

Label	Required By	Controlled By	Min.	Max.	Units	Note #	Description
tCPU00	CPU	PLT	1		ms	6, 7, 26	VCCST ramped and stable to VccST_PWRGD assertion
tCPU01	CPU	PLT	1		ms	6, 7	VDDQ ramped and stable to VccST_PWRGD assertion
tCPU02	CPU	PLT		No limit	ms	26, 43	VCCST ramped and stable before VDDQ stable **Note**: tCPU02 and tCPU03 are mutually exclusive, and only one of the parameters needs to be met depending on the rail order of VCCST/VCCSTG and VDDQ.
tCPU03	CPU	PLT		25	ms	26, 43	VDDQ ramped and stable before VCCST stable **Note**: tCPU02 and tCPU03 are mutually exclusive, and only one of the parameters needs to be met depending on the rail order of VCCST/VCCSTG and VDDQ.
tCPU04	CPU	PLT	0		ns	26, 31	VCCST must always ramp with or earlier then VCCSTG. VCCST >= VCCSTG at all times during ramp.
tCPU05	CPU	PLT	100		ns		VDDQ ramped and stable before VCCSA/ VCCIO ramps
tCPU06	CPU	PLT	100		ns	27	VCCST ramped and stable before VCCSA/ VCCIO ramps.
tCPU07	CPU	PLT	No Req	No Req	ns		VCCSA ramped and stable before VCCIO stable **Note:** this timing is to explicitly call out that there is no timing requirement between VCCSA and VCCIO.
tCPU08	CPU	PCH	1		ms	8	PCH CLK outputs stable and CPU VRs stable/ ready to PROCPWRGD assertion
tCPU09	CPU	PLT	1		ms	23	VCCSA stable before PROCPWRGD
tCPU10	CPU	PLT	1		ms	23	VCCIO stable before PROCPWRGD
tCPU11	CPU	PLT	1		ms	23	VCCPLL stable before PROCPWRGD
tCPU12	CPU	PLT	1		ms	23	VCCPLL_OC stable before PROCPWRGD
tCPU16	CPU	PLT	0		ns	32	VCCST_PWRGD assertion to PCH_PWROK assertion
tCPU18	CPU	PLT	0	35	us	34	DDR_VTT_CNTL (was DDR_PG_CTL) assertion to DDR VTT supplied ramped and stable while PLTRST = H (de-asserted).
tCPU19		CPU	0	100	ns	9	VccST_PWRGD assertion to DDR_VTT_CNTL (was DDR_PG_CTL) asserted.
tCPU20	CPU	PLT + PCH		500	ms	10	THERMTRIP# assertion until VCC, VCCGT, VCCSA, VCCIO VRs are disabled and not sourcing power.
tCPU21	CPU	PCH		1	ms		THERMTRIP# assertion until PCH issues global reset and assertion of SLP_SX signals

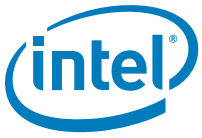


Table 45-5. Platform Sequencing Timing Parameters (Sheet 2 of 7)

Label	Required By	Controlled By	Min.	Max.	Units	Note #	Description
tCPU22	CPU	PLT	1		us		VCCST_PWRGD de-assertion to either VDDQ, VCCST below specification for normal S0 to Sx transitions. Recommend VCCST_PWRGD goes low with SLP_S3#.
tCPU23	CPU	PCH	TBD		us	45	PROCPWRGD de-assertion to either VCC* below specification for normal S0 to Sx transitions
tCPU26	CPU	PLT	10	65	us	11	CPU_C10_GATE# de-assertion to VCCSTG stable Note: CPU_C10_GATE# de-assertion to VCCST also needs to meet max 65us on cold boot
tCPU27	CPU	PLT	10	240	us	11	CPU_C10_GATE# de-assertion to VCCIO stable
tCPU28a	CPU	PLT		200	us	36	SLP_S3# assertion to VCCST_PWRGD de-assertion
tCPU28b	CPU	PLT	0		us	37, 38	VCCST_PWRGD low to VCCST dropping 5% of nominal value
tCPU29	CPU	PLT		100	mV/us	13, 25	Processor power rail instantaneous slew rate.
tCPU33	CPU	PLT		240	us	11	CPU_C10_GATE# de-assertion to VCCPLL_OC stable
tPCH01	PCH	PLT	9		ms	1, 47, 48	VccRTC = 2.0V to the point in time where voltage on the RTC resets equals 0.65 times the voltage present on the VccRTC rail during ramp. This measurement should be made from VccRTC = 2.0V to the first of RTCRST# or SRTCRST# reaching 0.65 * VccRTC
tPCH02	PCH	PLT	10		ms		VccDSW stable (@95% of full value) to DSW_PWROK high
tPCH03	PCH	PLT	10		ms		VccPrimary stable (@95% of full value) to RSMRST# high
tPCH04		PCH	9		ms	29, 42	VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with coined RTC battery
tPCH48		PCH	30		ms	29, 42	VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with coinless RTC
tPCH05	PCH	PLT	1		us	42	RTCRST# high (voltage above ViH_min) to DSW_PWROK high (when voltage crosses ViL_max such that internally it might be resolved as a logic '1')
tPCH06	PCH	PLT	200		us		VccDSW 3.3 stable (@95% of full value) to VccPrimary 1.05V starting to ramp (for DSx or nonDSx configurations)
tPCH07	PCH	PLT	0		ms		DSW_PWROK high to RSMRST# high
tPCH08	PCH	PLT	1		ms		SLP_S3# de-assertion to PCH_PWROK assertion

Table 45-5. Platform Sequencing Timing Parameters (Sheet 3 of 7)

Label	Required By	Controlled By	Min.	Max.	Units	Note #	Description
tPCH09	PCH	PLT	2, 4, 8, 16		ms		SLP_A# high to PCH assuming ASW rails are stable (95% of full value)
tPCH10	PCH	PLT	400		ns	4, 5	PCH_PWROK low to VCCIO dropping 5% of nominal value
tPCH11	PCH	PLT	100		ns		SLP_SUS# asserting to VccPRIM dropping 5% of nominal value
tPCH12	PCH	PLT	400		ns	5, 24	RSMRST# asserting to VccPRIM dropping 5% of nominal value
tPCH13	PCH		0		ms	14	RTCRST# asserting to VccRTC dropping 5% of nominal value (this applies only when RTC battery is removed)
tPCH14	PCH	PLT	400		ns	4, 5	DSW_PWROK falling to any of VccDSW, VccPrimary dropping 5% of nominal value
tPCH15	PCH	PLT		20	ms		SLP_LAN# (or LANPHYPC) rising to VccLANPHY high and stable
tPCH18		PCH	90		us		De-assertion of RSMRST# to De-assertion of eSPI_RESET# on exit from G3 (DSx platforms only), or exit from DSx
		PCH	95		ms		De-assertion of RSMRST# to De-assertion of eSPI_RESET# on exit from G3 (Non-DSx platforms only)
tPCH20	PLT	PCH	-100		ns		DDR_RESET# assertion to SLP_S4# assertion (*The negative minimum timing implies that* DDR_RESET# *must either fall before SLP_S4# or within 100 nS after it*).
tPCH21		PCH	Note 39		ms	39	Warm Reset PLTRST# assertion duration time
tPCH22		PCH	210		us		SUS_STAT# active to PLTRST# active
tPCH23		PCH	60		us		SUS_STAT# de-assertion to PLTRST# de-assertion
tPCH24		PCH	30		us		PLTRST# assertion to PROCPWRGD de-assertion
tPCH25		PCH	10		us		PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF. This timing is programmable (Range = 10us, 100us, 1ms, 10ms). Default is set to 10 us.
tPCH26		PCH	1		us		CLKOUT_BCLK turning OFF to SLP_S3# assertion
tPCH27		PCH	30		us	33	SLP_S4# assertion to SLP_S5# assertion
tPCH28		PCH	30		us	33	SLP_S3# assertion to SLP_S4# assertion
tPCH29		PCH	0		ms		SLP_S3# assertion to PCH_PWROK deassertion
tPCH31		PCH		tPCH02 + tPCH32	ms	15, 44	VccDSW3p3 ramped and stable until SUSCLK is stable. SUSCLK will start before the max timing, but will not be guaranteed valid until max timing is met
tPCH32		PCH	95		ms		DSW_PWROK assertion to SLP_SUS# de-assertion (only applicable to Deep Sx supported platforms).

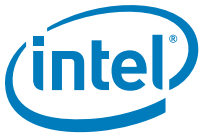


Table 45-5. Platform Sequencing Timing Parameters (Sheet 4 of 7)

Label	Required By	Controlled By	Min.	Max.	Units	Note #	Description
tPCH33		PCH	0, 99		ms	16	PCH_PWROK high to PLTRST# de-assertion. This timing is set by the PCH via Soft strap settings.
tPCH34	PCH	PLT		50	ms		All PCH Primary Rails should ramp up within this window.
tPCH35	PCH	PLT		100	ms	20	All PCH Rails should ramp down within this window.
tPCH36	PCH	PLT		100	mV/us		PCH Power rails instantaneous slew rate
tPCH37	PCH	PLT	5		mV/us	21	MPHY / SRAM Supply instantaneous slew rate
tPCH41	PCH	PCH	1		ms		PCH_PWROK high to PCH clock outputs stable
tPCH42	PCH	PLT		10	mV/us		VCCPRIM_Core slew rate during VID change
tPCH43	PCH	PLT	95		ms	28	DSW_PWROK assertion to PWRBTN# monitored
tPCH44	PCH	PLT	500		us		tPCH09 expiring to CL_RST# high
tPCH45		PCH	1, 5, 50, 100		ms	41	Clock outputs stable to PROCPWRGD assertion to processor. Timing set by PCH via Soft Strap settings
tPCH46		PCH	1, 2, 5		ms	41	PROCPWRGD and SYS_PWROK High to SUS_STAT# de-assertion. **NOTE:** Timing can be adjusted through the FIT tool
tPCH47	PCH	PLT	0		ms	46	RCIN# de-asserted to PCH_PWROK assertion
tPLT01		PCH	200		ms	2	RSMRST# de-assertion to SUSPWRDNACK valid. Timing set by PCH.
tPLT02			0	90	ms		RSMRST# de-assertion to ACPRESENT valid (not floating). **NOTE:** This is only for platforms not supporting Deep Sx state
				0	ms		RSMRST# de-assertion to ACPRESENT valid (not floating) [For platforms supporting Deep Sx state]. **NOTE:** ACPRESENT is a powered input to the PCH while in the Deep Sx state (that is, when DSW_PWROK=1 and RSMRST#=0). The PCH implements a weak pull-down on ACPRESENT while RSMRST#=0 such that the input is observed as 0 if not driven actively by the board during this time. If driven actively by the board to 1 while in Deep Sx and if the PCH is enabled to treat the ACPRESENT indication as a wake event from Deep Sx, then the PCH will power up the Primary well.
tPLT04	CPU/PCH	PLT	1		ms	3, 19	ALL_SYS_PWRGD assertion to PCH_PWROK. This timing must be controlled on the platform.
tPLT05		PLT	Platform dependent	No limit		18	ALL_SYS_PWRGD assertion to SYS_PWROK. This timing must be controlled on the platform. SYS_PWROK provides a platform/EC mechanism to stall the PCH de-assertion of PLTRST# to the platform. Different platform components may have difference timing requirements from when their power rails are stable until their respective reset signal can de-assert. Platform designer should adjust this timing based on their specific platform requirements. Example, if the platform only has mini-PCIe* devices requiring a 1 ms delay from power rails stable to PCIe* reset de-assertion, then the minimum value for ALL_SYS_PWRGD assertion to SYS_PWROK can be reduced to 1 ms. If SYS_PWROK asserts before PCH_PWROK, no additional delay will be added by the PCH to delay PLTRST# de-assertion and the final timing value will be subject to internal PCH timing parameters.

Table 45-5. Platform Sequencing Timing Parameters (Sheet 5 of 7)

Label	Required By	Controlled By	Min.	Max.	Units	Note #	Description
tPLT11	CPU	PLT		500	ms		SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA <100mV.
tPLT14		PCH	4		s		Power cycle duration time; programmable via PM_CFG.PWR_CYC_DUR bit.
tPLT15	PLT (MEM)	PLT		200	us	40	SLP_S4# assertion to VDDQ EN Low (VDDQ VR disabled). Memory dependent, refer JEDEC requirements
tPLT16	PLT (MEM)	PLT	30		ms	30	VDDQ ramp down to start of VPP ramp down when entering S4 and lower. This is not SOC requirement but a recommended timing to help meet the JEDEC sequencing requirements. Platform designers are responsible for making sure their designs meet the power sequencing requirements for the memory technology used in their designs.
tPLT20	PLT (MEM)	PLT	2.5		ms	30	VPP ramped to VDDQ start of ramp when entering S0 at power up. This is not SOC requirement but a recommended timing to help meet the JEDEC sequencing requirements. Platform designers are responsible for making sure their designs meet the power sequencing requirements for the memory technology used in their designs.
tPLT17	CPU	PLT		200	us	35	SLP_S3# assertion to IMVP VR_ON de-assertion
tPLT18	CPU	PLT		200	us	35	SLP_S3# assertion to VCCIO VR disabled
tPLT19	PLT	PLT		10	us	22	RSMRST_PWRGD# or SLP_SUS# assertion to RSMRST# assertion

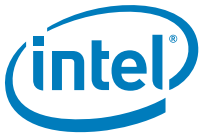


Table 45-5. Platform Sequencing Timing Parameters (Sheet 6 of 7)

Label	Required By	Controlled By	Min.	Max.	Units	Note #	Description

Notes:

1. PCH Primary Rails must never be active while VCCRTC is OFF
2. RSMRST# should be de-asserted for at least 200ms before PCH will consider SUSPWRDNACK valid.
3. PCH can delay de-assertion of PLTRST# with a soft strap setting. Refer tPCH08 and tPCH09 and the SPI Programming Guide for more details.
4. For catastrophic/surprise power failures only.
5. For surprise power down cases, if DSW_PWROK is de-asserted (tPCH14) before DSW3.3 **and** any other Prim rails droop out of spec, there is no risk of RTC corruption (assuming VCCRTC was previously powered and VCCRTC# is de-asserted) and this spec can be ignored
6. VCCST_PWRGD has no edge rate requirement, but edges must be monotonic.
7. VCCST_PWRGD must accurately reflect the state of VCCST and must not glitch when VCCST, or VDDQ power is applied. Additionally, VCCST_PWRGD must track to the state of PCH_PWROK on the platform. When PCH_PWROK de-asserts during S0 --> Sx transitions, then VCCST_PWRGD must also de-assert.
8. Processor's PROCPWRGD is not expected to be used externally on the platform, but is available for monitoring.
9. CPU will assert DDR_VTT_CNTL after VCCST_PWRGD crosses its threshold point on rising edge, which will typically be around 0.5*VccST but can be anywhere between Vil to Vih levels.
10. It is strongly recommended that the SLP_S3# be a qualifying input signal to ALL_SYS_PWRGD logic, which drives IMVP VR_ON inputs. Additionally, it is recommended that SLP_S3# also qualify the EN control to the VCCIO power supply
11. NA
12. NA
13. Applies to all CPU power supply rails
14. There are no perceived functional failures if this minimum is violated since all data is lost anyway when VccRTC drops. The only real requirement is to avoid driving a high signal level into the powered down device for an extended period of time, assuming an external device(s) on a different power supply then VCCRTC is driving RTCRST# or any other RTC well input signal.
15. SUSCLK is now powered in DSW well.
16. PCH can delay de-assertion of PLTRST# with a soft strap setting. If tPCH33 is not enabled, the platform is responsible for controlling the assertion timing of PCH_PWROK and SYS_PWROK in such a way that it satisfies platform component timing requirements of power stable to reset de-assertion. Refer SPI Programming Guide for more details. On a platform level this timing doesn't necessarily need to meet 99ms, PCH soft straps guarantees a min of 99ms.
17. NA
18. Example, if the platform only has mini-PCIe* devices requiring a 1 ms delay from power rails stable to PCIe* reset de-assertion, then the minimum value for ALL_SYS_PWRGD assertion to SYS_PWROK can be reduced to 1 ms. If SYS_PWROK asserts before PCH_PWROK, no additional delay will be added by the PCH to delay PLTRST# de-assertion and the final timing value will be subject to internal PCH timing parameters.
19. PCH_PWROK assertion assumes all the following CPU and PCH voltage rails are ramped and stable **except** for: VCC, VCCGT, VCCGTx, VCCOPC, VCCEOPIO
20. No Ramp down requirement between rails. All VRs should stop regulation based on SLP_SUS# signal, or another common shutdown signal
21. NA
22. 10us max limit is an estimation and will vary based on platform VR and EC implementation details. Platform designers are responsible for ensuring that tPCH12 is not violated during normal DSx entries based on EC and VR response times to assertion of SLP_SUS# and/or RSMRST_PWRGD#
23. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD. Therefore, the platform is only responsible to have these rails ready a minimum of 0ms before PCH_PWROK assertion
24. Applicable to all power down sequences where Prime well rails are turned off and to emergency power loss. Refer RSMRST#/DSW_PWROK Special Considerations section for more details.
25. Only applicable to SKUs with OPC support
26. If VCCSTG and VCCIO supplies are merged together as a single supply, then VCCSTG/VCCIO supply must also satisfy this requirement
27. If VCCSTG and VCCIO supplies are merged together as a single supply, then the timing requirement is between VCCST/ VCCSTG/VCCIO and VCCSA

Table 45-5. Platform Sequencing Timing Parameters (Sheet 7 of 7)

Label	Required By	Controlled By	Min.	Max.	Units	Note #	Description

Notes: (cont)

28. Applicable to all G3 exits where GEN_PMCON_B.AG3E=1. The PWRBTN# must assert for at least 16ms after the minimum tPCH43 timing before PCH will detect PWRBTN# as a wake event
29. For scenarios where the coin-cell is dead or missing, the PCH can electrically tolerate the VCCRTC and VCCDSW/VCCPRIM 3.3V supplies ramping simultaneously with VCCDSW/VCCPRIM 3.3V leading VCCRTC by ~0.2 – 0.3V (i.e. voltage drop associated with the coin cell Schottky diode circuit). These scenarios are not allowed as typical power sequencing scenarios, and are expected to be very infrequent. In these scenarios, glitch-free signal operation on DSW signals can not be guaranteed when the platform is configured for DSx mode. Likewise, glitch-free signal operation on DSW and PRIM well signals can not be guaranteed when the platform is configured for non-DSx mode
30. Generally, JEDEC specifications require VPP >= VDDQ for both power up and power down sequences. This timing parameter is a suggested value as ensure this requirement is met on power down, but systems designer must account for other platform level considerations such as output decoupling, discharge circuits, etc that can alter this relationship.
31. VCCST supply is typically controlled by SLP_S4#, and VCCSTG supply is typically controlled by SLP_S0# AND SLP_S3#. Since the timing delay between SLP_S3# and SLP_S4# deassertion during a S4/S5 à S0 transition can be small (defined by tPCH28), OEMs may need to take extra steps to ensure this timing is met. Example, power gates of equivalent slew rate may be required on both VCCST and VCCSTG supplies. Alternatively, a small timing delay path might be required on the SLP_S3# path of the VCCSTG power gate enable
32. VCCST_PWRGD should start to assert no later than when PCH_PWROK asserts; however, VCCST_PWRGD may lag completing its ramp with respect to PCH_PWROK by up to 20us
33. Not applicable to eSPI mode, refer to the eSPI Compatibility Specification (RDC#508740) for eSPI implementations
34. Only applies to configurations that use DDR_VTT_VCTRL signal to enable/disable VTT VR and only applies after PLTRST# has de-asserted (ie, S0). VTT must be completely ramped and ready for full load at or before the de-assertion of PLTRST# on Sx -> S0 transitions.
35. Timing to VR being disabled, not until the VR is fully ramped down
36. S0 to S3 transition with VCCST powered in S3 state
37. S0 to Sx transition with VCCST unpowered in Sx
38. Recommend not to exceed 200us delay with respect to SLP_S3#
39. During a warm reset sequence, the PCH sequencing flows will internally re-execute several timing parameters and tpch45 and tpch46 are two of the parameters that are re-executed. tPCH45 and tPCH46 are primarily for G3/DSx/Sx -->S0 flows, but they are executed for cold boot, cold reset, and warm reset. The nominal setting for these timings is partially controlled by the setting of SPI soft straps associated with tPCH45 and tPCH46. The minimum possible PLTRST# assertion time will be equal to the soft strap settings for tPCH45 + tPCH46. The maximum PLTRST# assertion time is not guaranteed across all warm reset cycles, but the typical worst case assertion time is approximately equal to (tPCH45 soft strap setting) + (tPCH46 soft strap setting) + 20ms.
40. This is a platform timing recommendation to help ensure that memory device power down sequencing requirements between VDDQ and VPP are likely to be met (refer tPLT16). This is not a requirement for the CFL SoC itself. Refer to the JEDEC LPDDR3 and DDR4 power down sequencing requirements for more details
41. This parameter is programmable, refer to the Flash Descriptor Record in the SPI Programming Guide in the ME firmware package
42. For the dead RTC coin cell and coin cell-less with depleted main battery RTC cases where the 3.3DSW ramps and powers the RTC well, the board designer should set the 3.3DSW rail stable to DPWROK assertion delay (tPCH02) for = 30ms. This is required to ensure that SRTCRST# and RTCRST# de-assert after VCCRTC is stable, but before DPWROK assertion. Failure to meet this requirement may result in DPWROK asserting with, or before, SRTCRST# and RTCRST# reach VIH, which is a sequencing violation and can result in a non-booting system scenario. Refer Section 30.2 (Real Time Clock Topology Guidelines) and Section 59.3.13 (RTC Circuit) for SRTCRST# and RTCRST# RC timing network details
43. tCPU02 and tCPU03 are mutually exclusive, only tCPU02 or tCPU03 needs to be met
44. SUSCLK stable means the clock is toggling and is within it's defined parameters. This timing spec is applicable to all G3 exits, excluding the G3 exit immediately following the ramp of VCCRTC, which may have a longer delay
45. This does not concern platform design, this is internal to SOC.
46. RCIN# is expected to be low in S3 and lower, but can be kept high in S3 through S5 without issue. RCIN# low in S3 and lower will not cause an INIT#. This requirement does not preclude the platform for asserting RCIN# after PLTRST# de-assertion when entering S0.
47. C3 and C4 Capacitors used in the RTC external circuit should be evaluated with regards to aging, voltage and temperature characteristics to ensure reliable operation in the intended operating environment. See section 13.1.3 RTC External RTCRST# Circuit.
48. For measurement details, reference RTC Reset Timing Technical Advisory - RDC#610459.

Additional Notes:

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- DDR_RESET# behavior does not directly track the state of VDDQ rail. For DDR_RESET# to assert properly on surprise power failure, the VDDQ VR pwrgood output should be an input into the logic generating PCH_PWROK