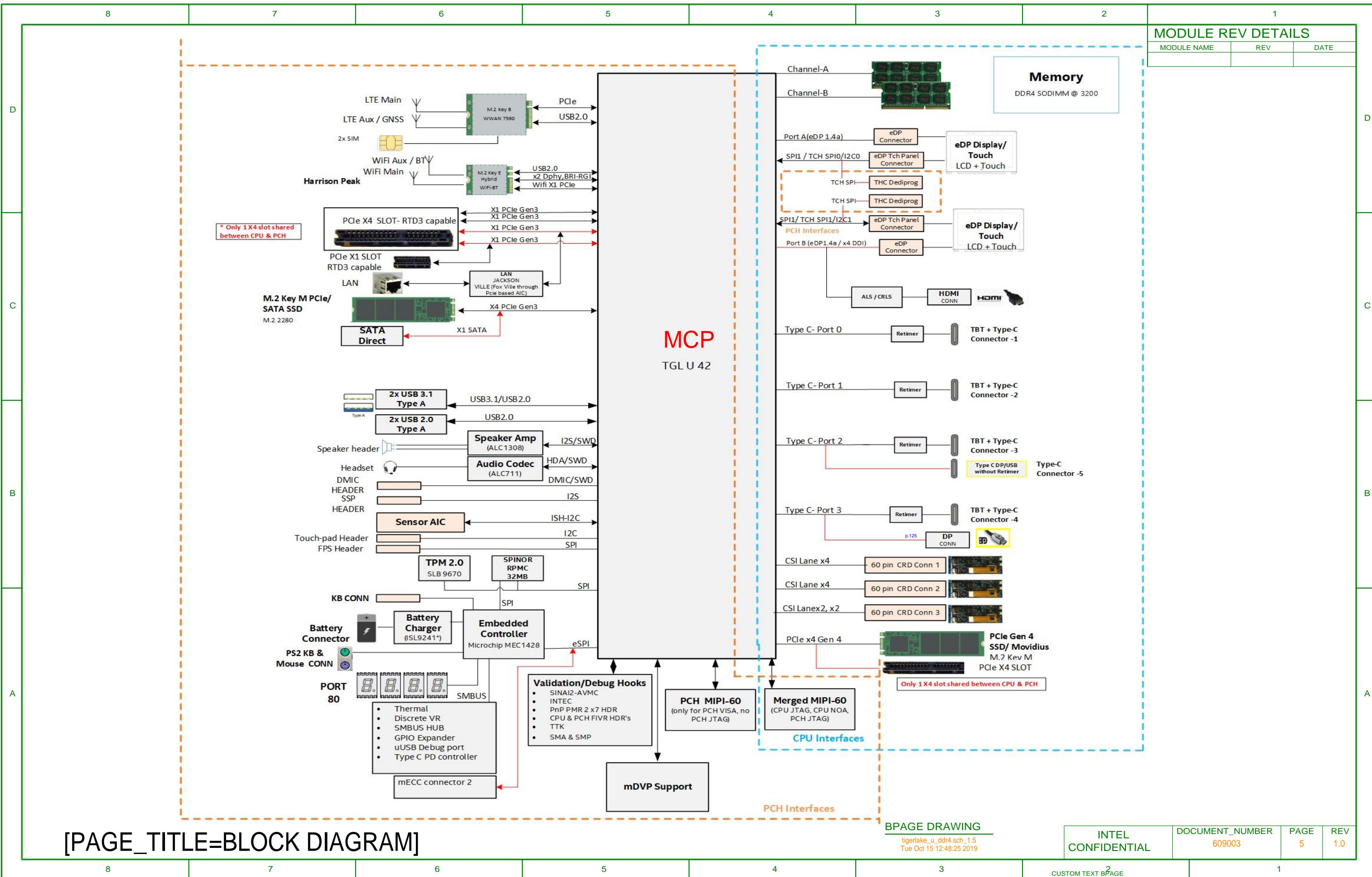


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[2. INDEX -1]				[48. GPIO - ISH GPIO SHARING OPTIONS - 1]			MODULE NAME
[3. INDEX -2]				[49. TGL-U MCP (12 OF 21) - SYSTEM POWER MANAGEMENT]			REV
[4. INDEX -3]				[50. SYSTEM POWER MANAGEMENT OPTIONS]			DATE
[5. BLOCK DIAGRAM]				[51. PLATFORM RESET BUFFER]			
[6. LED DISCRIPTION]				[52. TGL-U MCP (13 OF 21) - CPU POWER 1 OF 2]			
[7. Z0 VS A0 PINLIST]				[53. TGL-U MCP (15 OF 21) - CPU POWER 2 OF 2]			
[8. TABLE - MPHYS MAPPING]				[54. CPU PDBOM 1 OF 2]			
[9. ALC711 ES1 vs ES2]				[55. CPU PDBOM 2 OF 2]			
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[12. TGL-U MCP (1 OF 21) - DISPLAY & TYPE-C (TBT/DISPLAY)]	✓			[58. RESERVE]			
[13. DISPLAY - DDIA - PORT AC CAPS]				[59. PCH PDBOM 1 OF 2]			
[14. DISPLAY - DDIB - PORT SHARING, AC CAPS]				[60. PCH DERIVED RAILS]			
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[16. DISPLAY - TYPE-C PORT 1 AC CAPS]				[62. TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)]			
[17. DISPLAY - TYPE-C PORT 2 AC CAPS]				[63. TGL-U MCP (19 OF 21) - FIVR DEBUG]			
[18. DISPLAY - TYPE-C PORT3 SHARING, AC CAPS]				[64. CPU FIVR DEBUG HEADER]			
[19. TGL-U MCP (2 OF 21) - MEMORY CHANNEL - A]				[65. TGL-U MCP (20 OF 21) - RESERVED SIGNALS]			
[20. TGL-U MCP (3 OF 21) - MEMORY CHANNEL - B]				[66. JTAG/CFG - CFG TERMINATIONS]			
[21. TGL-U MCP (4 OF 21) - CPU MISC]				[67. JTAG/CFG - MERGED JTAG OPTIONS]			
[22. TGL-U MCP (5 OF 21) - LSIO - SPI, ESPI, THC, MLINK, SMLINK, SMBUS]				[68. JTAG/CFG - CPU/PCH MERGED MIPI 60 CONNECTOR]			
[23. TGL-U MCP (6 OF 21) - LPSS - GSPI, UART, I2C, ISH-SPI, ISH UART, ISH I2C, ISH GPIO]				[69. JTAG/CFG - PCH DEBUG SHARING OPTIONS]			
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[25. PCH SMBUS EXPANDER, FRU]				[71. PD AIC CONNECTOR]			
[26. SHARING OPTIONS - 1 - ESPI, SMLINKS]				[72. USB-C RSVD]]			
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[31. GPIO - ISH SHARING OPTIONS -2 - I2C, GPIO]							
[32. GPIO - OTHER PCH GPIO SHARING OPTIONS - 1]							
[33. SVID SIGNALS]				[79. FLEX CONNECTOR]			
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[35. PCIE PORT 0&1 SHARING OPTIONS, AC CAPS]				[81. MEMORY - DDR4 SODIMM CHANNEL -A (2 OF 2)]			
[36. PCIE PORT 2&3 SHARING OPTIONS, AC CAPS]				[82. MEMORY - DDR4 SODIMM CHANNEL -B (1 OF 2)]			
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[40. PCIE PORT 10&11 SHARING OPTIONS, AC CAPS]				[86. MEMORY - DDR VREF CIRCUITRY -1 - PROCESSOR, OPTIONS]			
[41. PCIE PORT RESET RTD3 CIRCUIT]				[87. MEMORY - DDR4 SODIMM & LPDIMM CONN PINOUT]			
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[44. TGL-U MCP (10 OF 21) - CSI2, CNVI]				[90. DISPLAY - eDP connector 1 - MISC]			
[45. TGL-U MCP (11 OF 21) - CLOCK SIGNALS]				[91. DISPLAY - eDP connector 1]			
[46. SRC CLOCKS ]				[92. DISPLAY - EDP CONNECTOR 2 - CMC]			
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RefDes	LED Description
DS4G1	V1P05_CTRL
DS4G2	VNN_CTRL
DS8H5	S3 STATE
DS8H3	S4 STATE
DS8H4	S5 STATE
DS8H2	DSW STATE
DS8H1	M0/M3 STATE
DS3H1	ME PWR Gate

RefDes	LED Description
DS8H6	CAPS LOCK
DS8H7	NUM LOCK
DS7G1	POWER BUTTON
DS7H1	BAT STATUS LED

RefDes	LED Description
DS8G6	SLP S0 LED
DS8G4	PWRGD
DS8G5	CATERR
DS6G1	C10 GATE
DS6G2	CS INDICATE

RefDes	LED Description
DS9B1	SATA Direct connect DEVSLP
DS9E1	M.2 SSD DEVSLP
DS8G7	SATA ACTIVITY
DS6D1	PCIE LINK DOWN
DS4G4	WLAN
DS4G3	BT
DS7D1	WWAN

Error Type	Error Code	Caps Lock LED (DS9H2)	Scroll Lock LED (DS7G1)	Num Lock LED (DS9J1)
No Error	0	Off	Off	Off
RSMRST_PWRGD_N	1	Off	Off	Flash
PM_SLP_S5_N	2	Off	Flash	Off
PM_SLP_S4_N	3	Off	Flash	Flash
PM_SLP_S3_N	4	Flash	Off	Off
PM_SLP_M_N	5	Flash	Off	Flash
ALL_SYS_PWRGD	6	Flash	Flash	Off
PLT_RST_N	7	Flash	Flash	Flash
DOCK_SYS_PWRGD_N	8	On	On	Flash
SUSWARNB	9	On	Flash	On

Note: KSC Thermal Shutdown is indicated by flashing of Num\_Lock and Caps\_Lock LEDs alternatively.  
DS7G1 acts as led indication for error code in case of any error otherwise works as power button LED

[PAGE\_TITLE= LED DISCRIPTION]

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8	7	6	5	4	3	2	1				
D							MODULE REV DETAILS				
D		MODULE NAME		REV		DATE					
C											
B											
A											
Interface	WHL	TGL									
Board ID											
PCIE Gen4 – DEKEL PHY	No	Yes									
TYPE C	No	Yes									
XTAL_IN	24MHz	38.4MHz									
Memory	1 Channel	2 channel									
CSI	No	Yes									
No.	Changes	WHL	TGL		Status						
1	XXDP_COMP	24.9 ohm PU to VCCIO	24.9 ohm PU to VCCIN /+VCC1P05_OUT_FET (default) on extra added pin on one of the spare pins of TGL_A0.		implemented						
2	XXDDR_COMP[0]	121 ohm PD	121 ohm PD on Pin DW 49		implemented						
3	XXDDR_COMP[1]	80.6 ohm PD	80.6 ohm PD on pin DW47		implemented						
STRAP											
4	SVID DISABLE STRAP	J3B1 to 1-2	J3B1 to 1-X		WIP						
5	GPPC_F10	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K		WIP						
6	GPPC_F0*	High, SW9C1 Switch closed, 4.7K PU	LOW, Internal PD 20K		WIP						

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							MODULE REV DETAILS			
							MODULE NAME    REV    DATE			
<b>TGL-U 42 ROW RVP's Mphy Allocation</b>										
PCIe Controller		Lane #	Flex IO		HSIO Topology 1 (Default)	HSIO Topology 2	HSIO Topology 3 (SV SKU)			
x4 Controller 1		Lane 0	PCIE3_1_USB31_1							
		Lane 1	PCIE3_2_USB31_2							
		Lane 2	PCIE3_3_USB31_3							
		Lane 3	PCIE3_4_USB31_4							
x4 Controller 2		Lane 4	PCIE3_5		Lane 0 for x4 PCIe slot		x4 PCIe Slot			
		Lane 5	PCIE3_6		Lane 1 for x4 PCIe slot					
		Lane 6	PCIE3_7_LAN_0A_UFS_00		Jacksonville Gbe LAN					
		Lane 7	PCIE3_8_LAN_0B_UFS_01		x1 PCIe Slot					
x4 Controller 3		Lane 8	PCIE3_9_LAN_0C_UFS_1_00		M.2 Key M x4 SSD(Lane reversal for x4 PCIe)	SATA Direct Connect	HSIO Connector			
		Lane 9	PCIE3_10_UFS_1_01							
		Lane 10	PCIE3_11_SATA_0							
		Lane 11	PCIE3_12_SATA_1							
x4 Controller 4 (Gen 4 North side)		CPU Lane0	CPU_PCIE_0		M.2 Key M x4 SSD	x4 PCIe Slot				
		CPU Lane1	CPU_PCIE_1							
		CPU Lane2	CPU_PCIE_2							
		CPU Lane3	CPU_PCIE_3							

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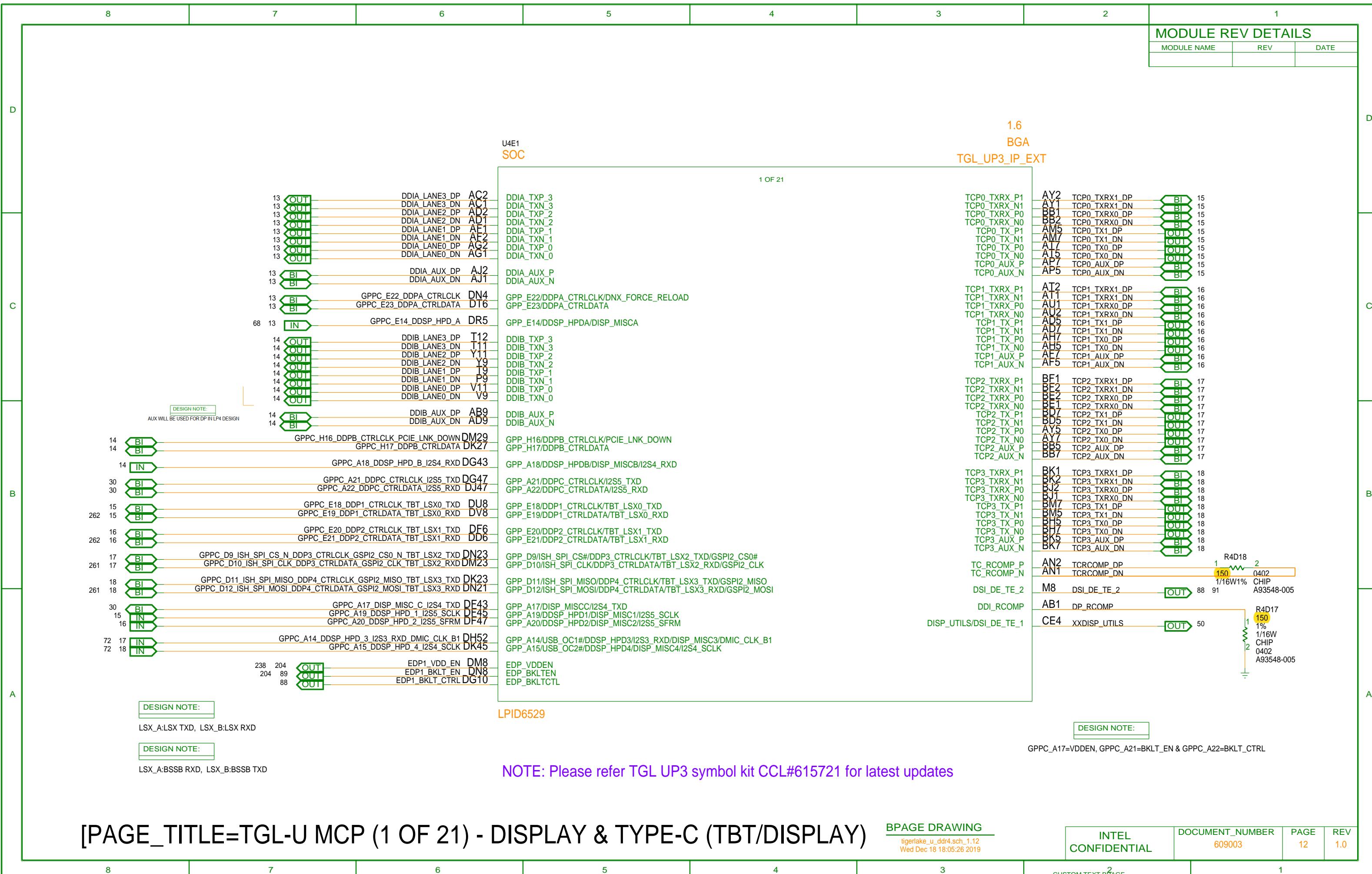


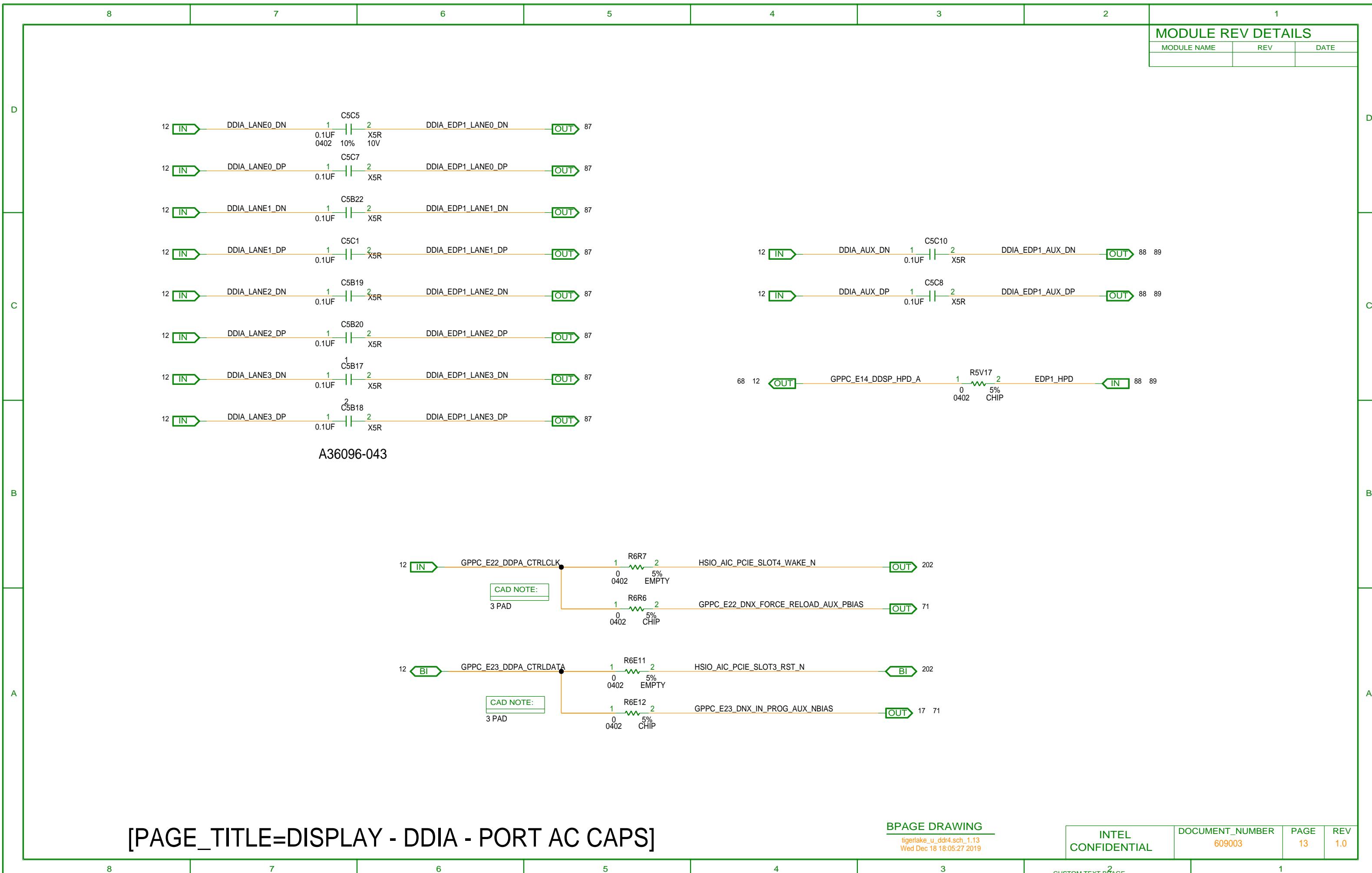
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MODULE NAME	REV	DATE

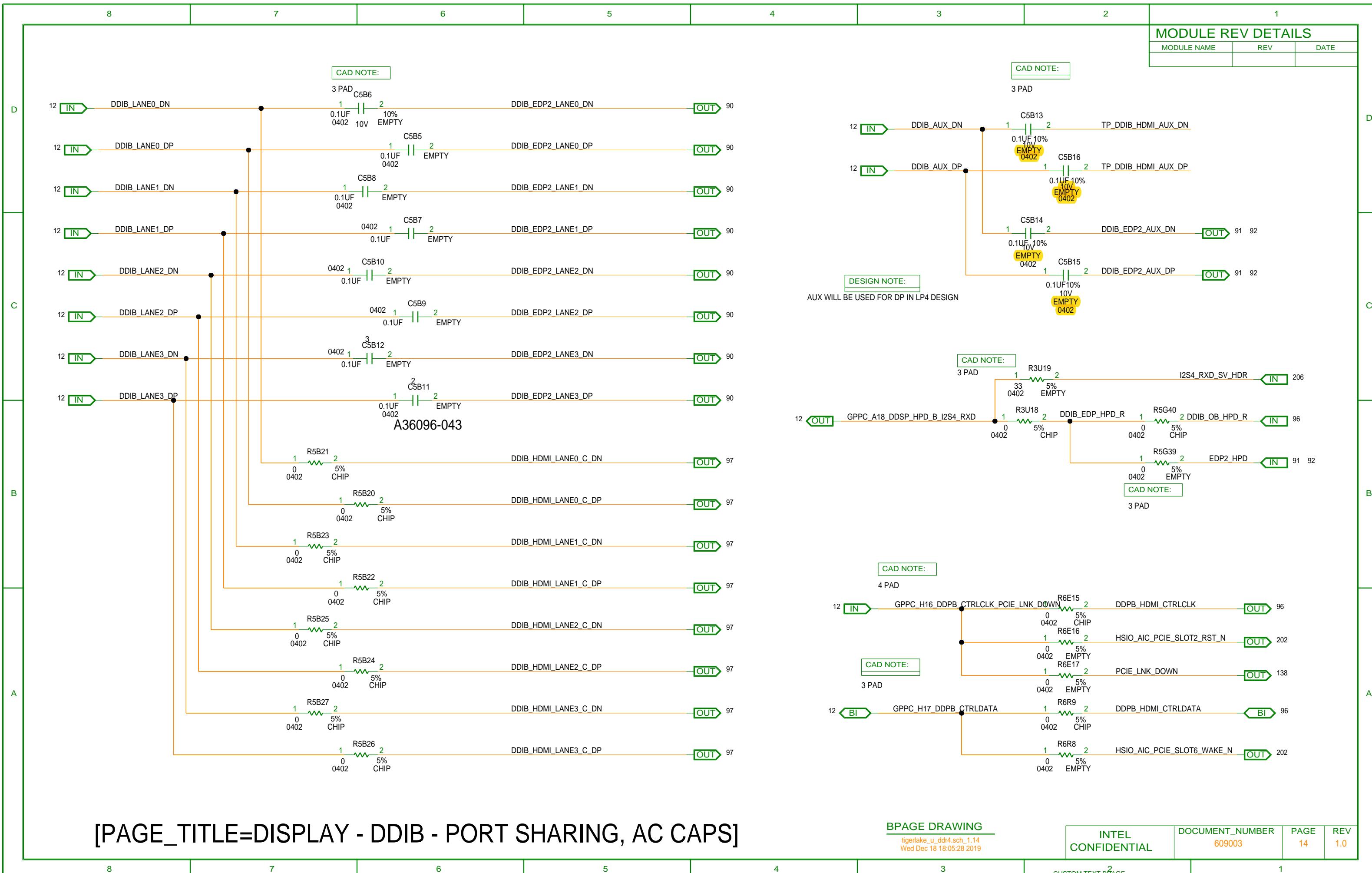
D	RefDes	Jumper Description	Default
	J1A3	MIPI60 OVERRIDE N	'1-X'
	J2H3	MIPI60 PRESENT1 N	'1-X'
	J1C1	TYPEC DISABLE	'1-X'
	J1F3	NO REBOOT STRAP	'1-X'
	J1F4	FLASH DESCRIPTOR SECURITY OVERRIDE STRAP	'1-X'
c	J3B1	SVID DISABLE STRAP	'1-X'
	J1F4	A0 PERSONALITY STRAP	'1-X'
	J3H1	DDI3 HPD	'1-X'
	J9J5	BT RF KILL N, WIFI RF KILL N	'1-X,3-X'
	J9J4	CNVI Disable	'1-2'
	J5U1	TOUCH PANEL POWER SUPPLY GENERATION	'1-2'
	J8J3	PROCHOT EC JPR	'1-X'
	J9J3	SMC_RST_N JPR	'1-X'
	J9J2	SMC_LID JPR	'1-X'
	J8D2	SVID CLOCK	'1-2,3-X'
	J8D3	SVID ALERT	'1-2,3-X'
	J8D4	SVID DATA	'1-2,3-X'
	J8G3	PCH GLITCH ISSUE MITIGATION	'1-X'
	J7G1	SRTC/RTC CLEAR CMOS JPR	'1-X'
	J7H2	SPD_PRSNT JPR	'1-2'
	J8H3	FRU SMB CLK S3	'1-2'
	J8H5	FRU SMB DATA S3	'1-2'
	J6J1	PECI_MUX_CTRL_SNI_R	'1-X'
	J8J1	FRU POWER SUPPLY	'1-2'
	J6G4	H_PECI_CPU JPR	'1-X'

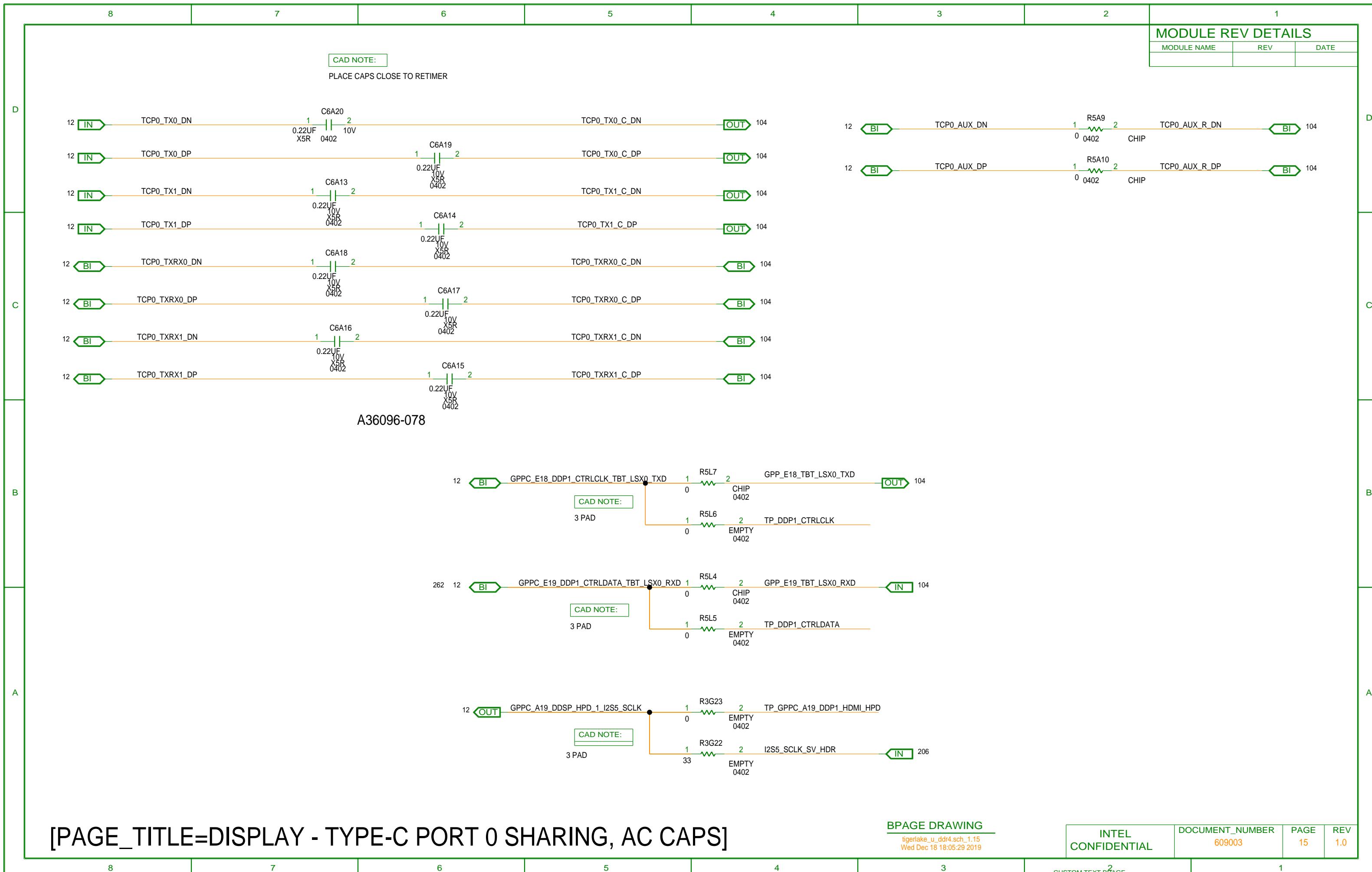
D	RefDes	Jumper Description	Default
	SW4V1	MIPI60 FN[0:3]	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
c	SW5V1	1 - VDDQ_VR_PWRGD - IMVP_VR_EN 2 - ALL_SYS_PWRGD - IMVP_VR_EN 3 - SATAXPCIE_0_SATAGP_0_R 4 - BIOS_REC	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
	SW6J2	1 - EC_SHD_CS_SW 2 - NC 3 - RETIMER_BYPASS_STRAP 4 - ESPI_TESTCRD_DET	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)
	SW9C1	1 - BUF_PLT_RST_1.8 - WF_CAM_RST_N 2 - WF_CAM_RST_ND - WF_CAM_RST_N 3 +V1.8A - XTAL_SEL1_J 4 +V3.3A - XTAL_IN_J	1-8(OFF); 2-7(ON); 3-6(OFF); 4-5(OFF)
	SW8W1	1 - PNP_NPNP_SKU 2 - VIRTUAL_DOCK_DET_N 3 - VIRTUAL_BATTERY 4 - FLIP_TO_TABLET_MODE	1-8(OFF); 2-7(OFF); 3-6(OFF); 4-5(OFF)

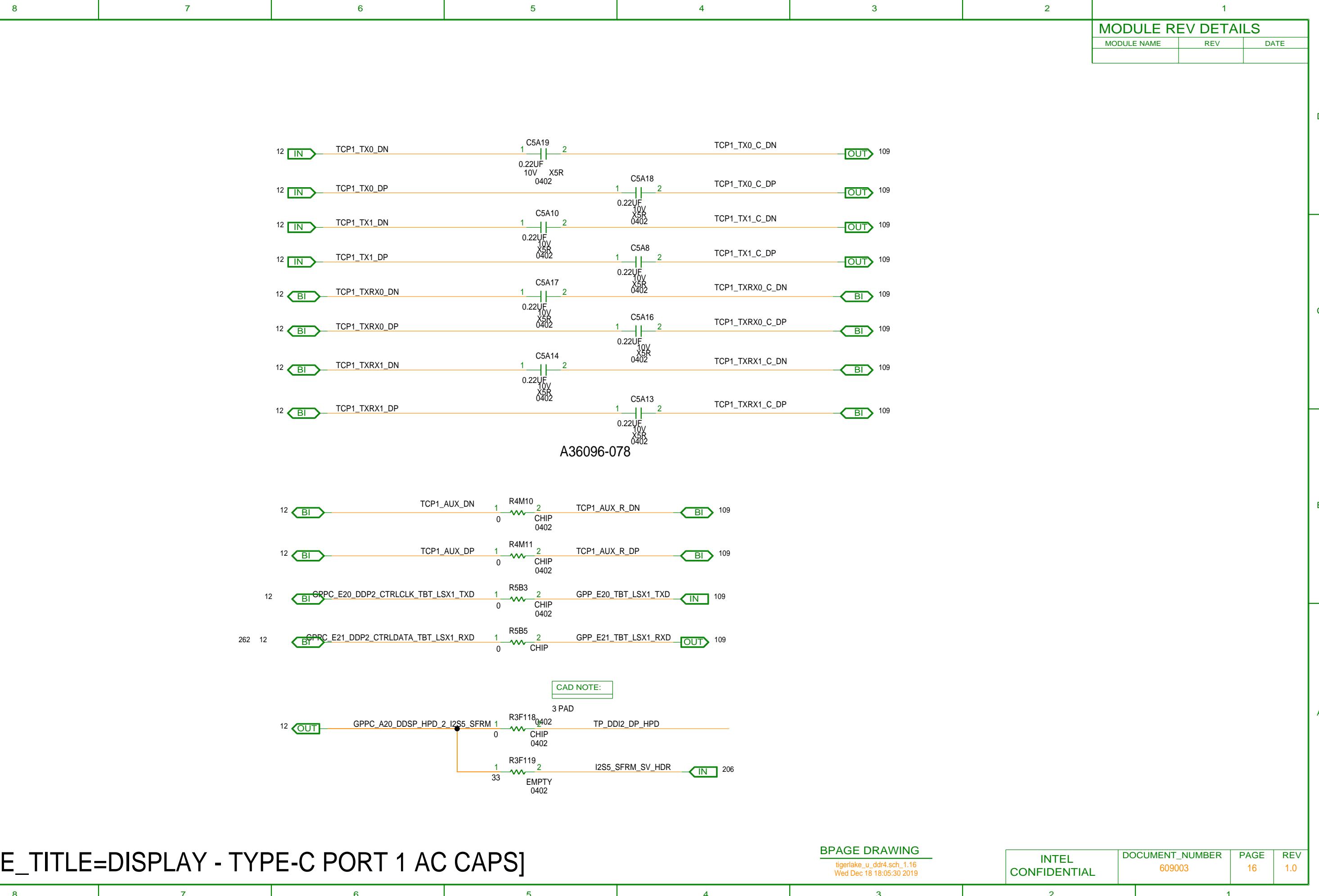
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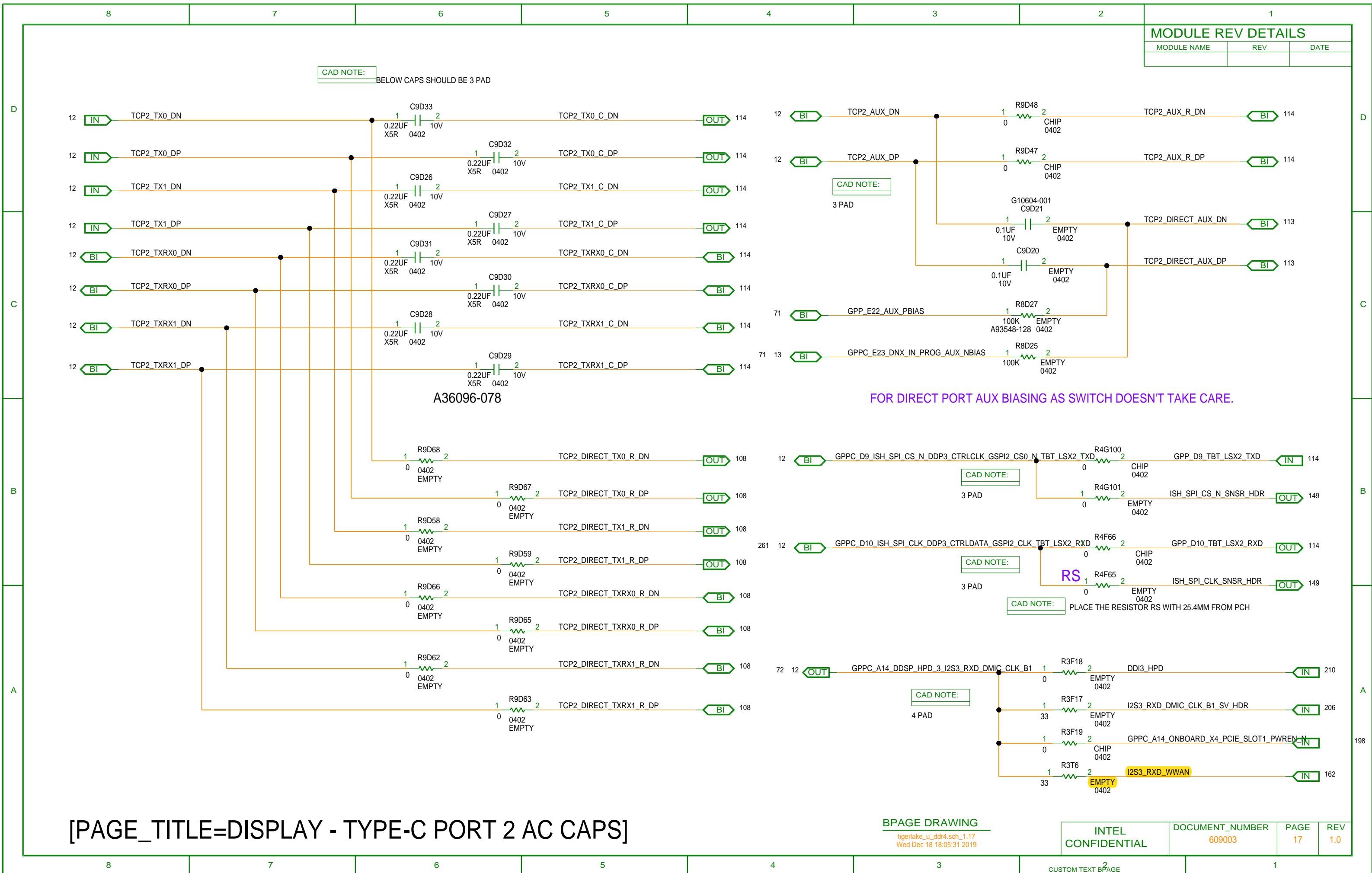


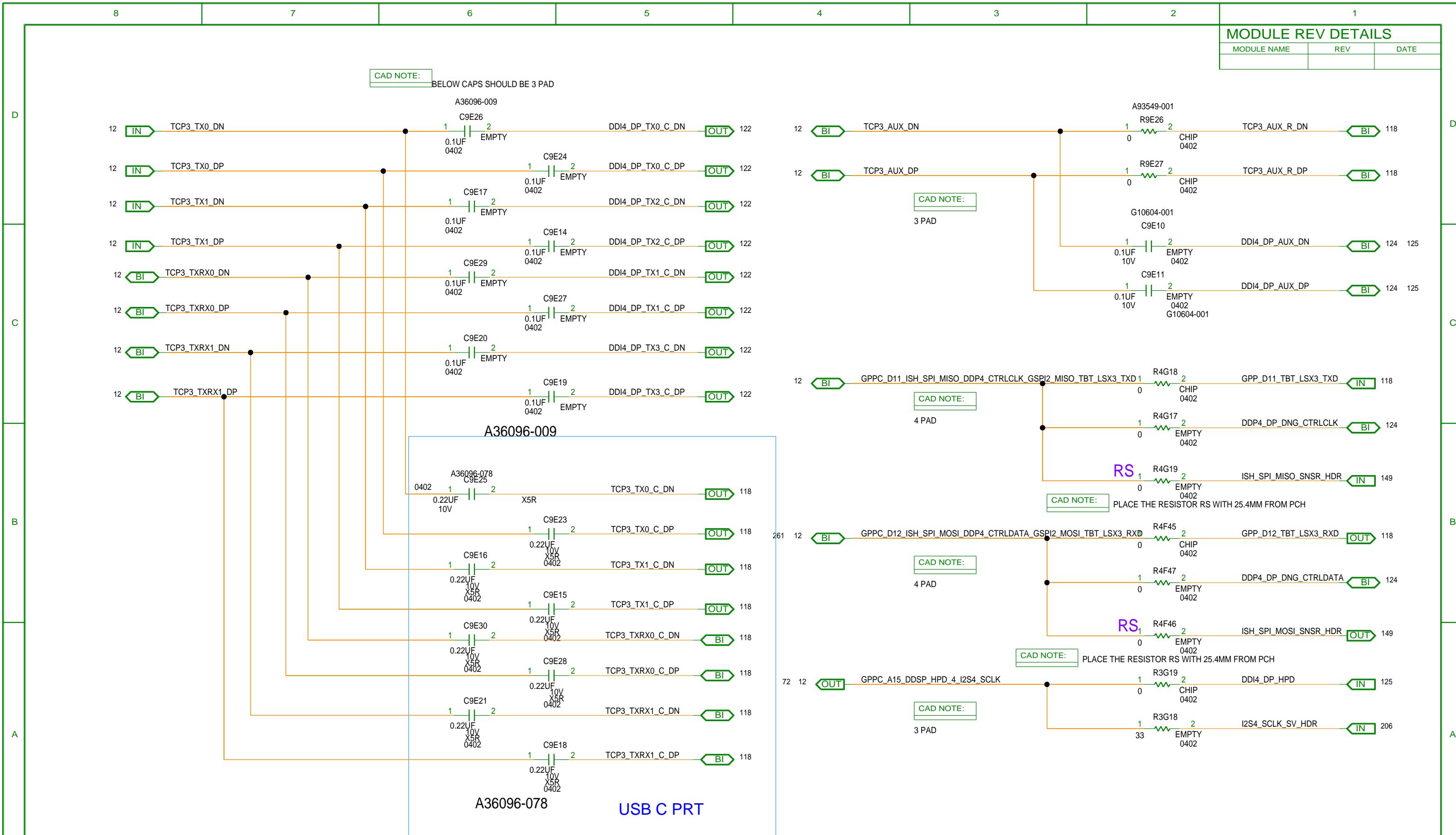


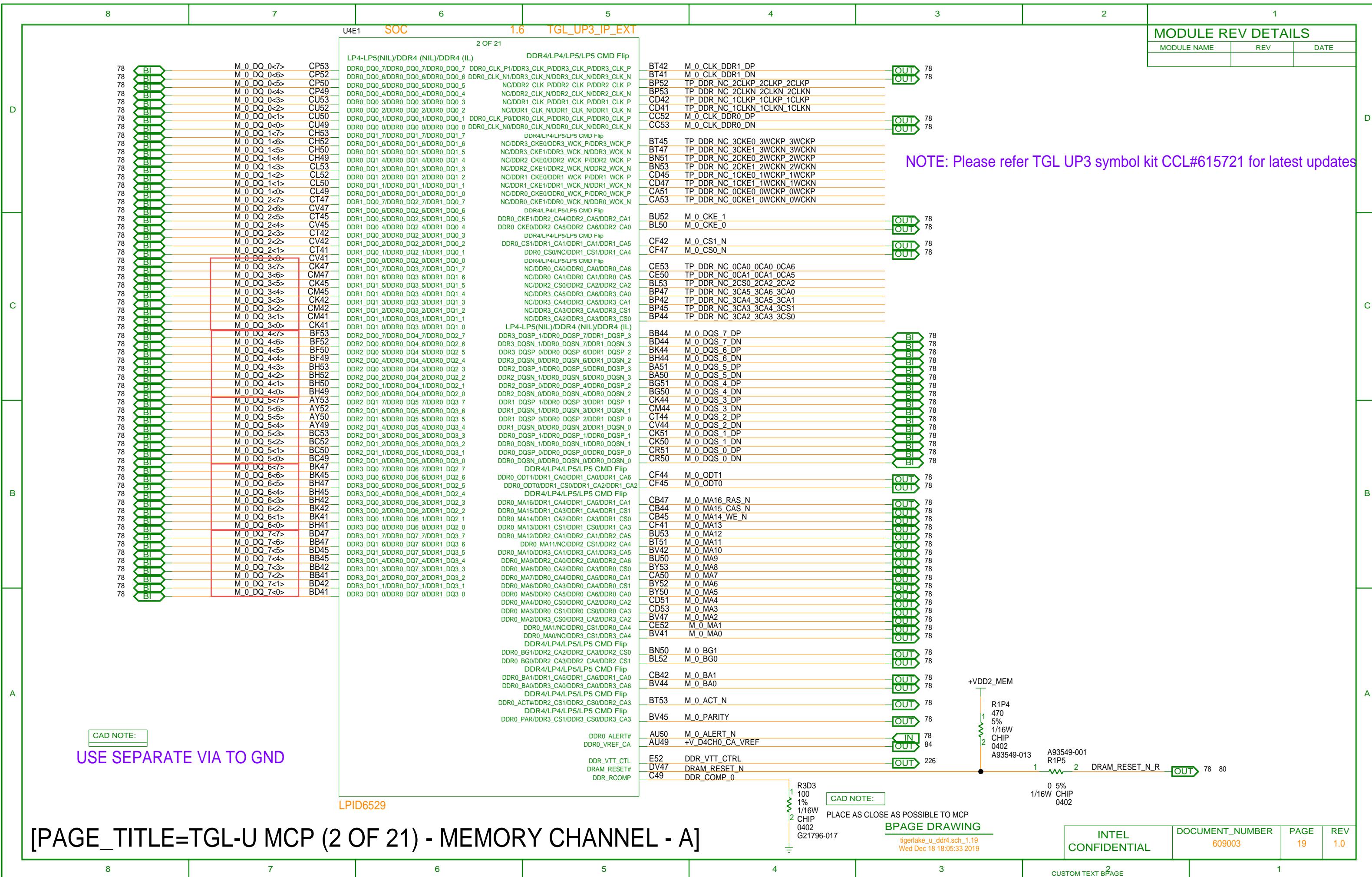


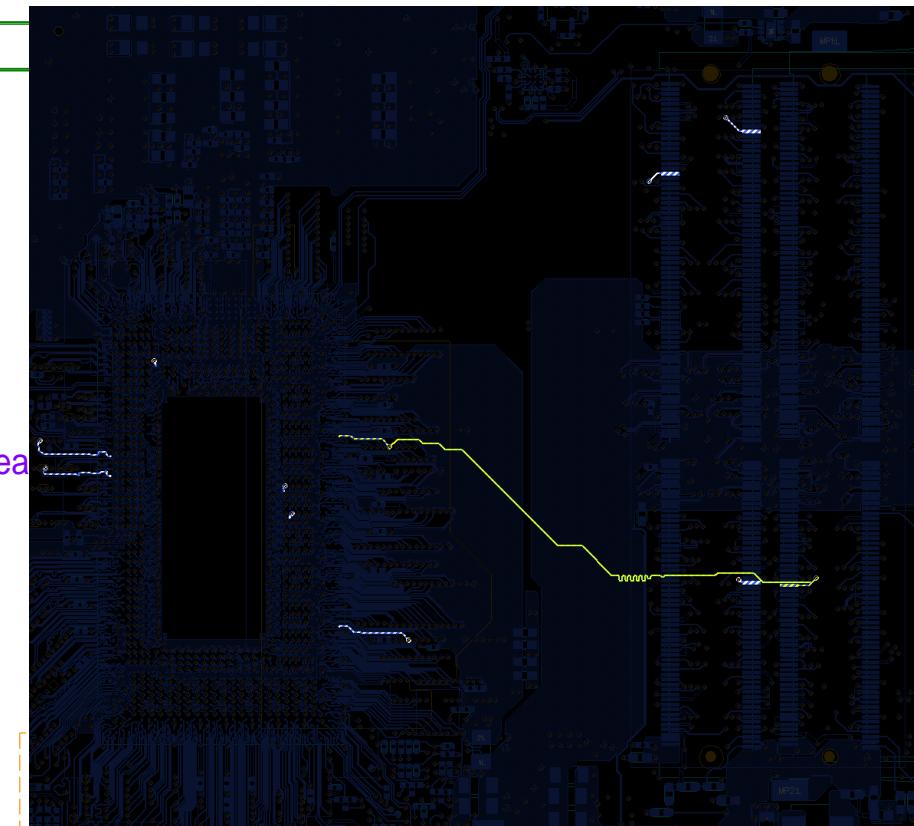
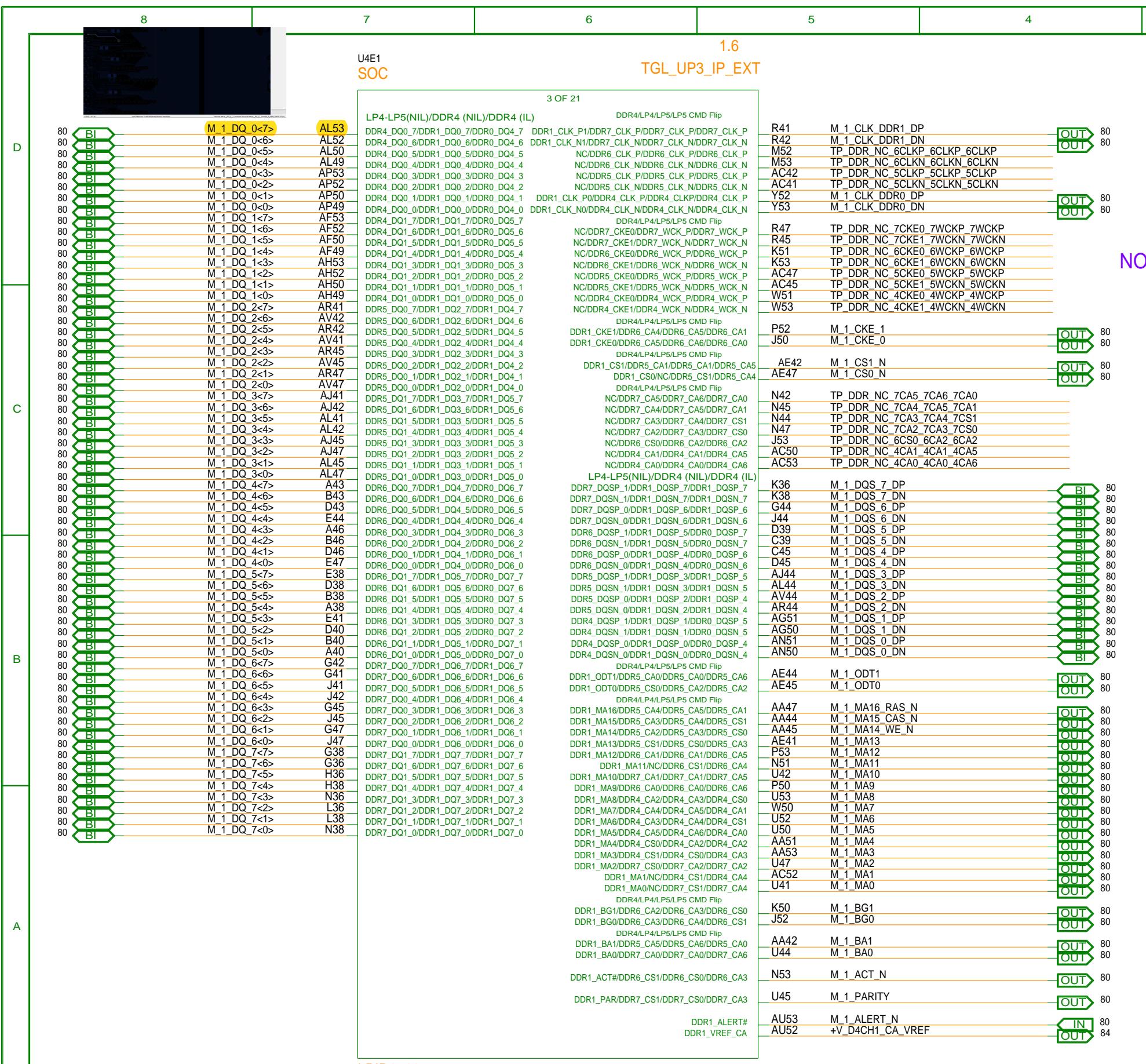








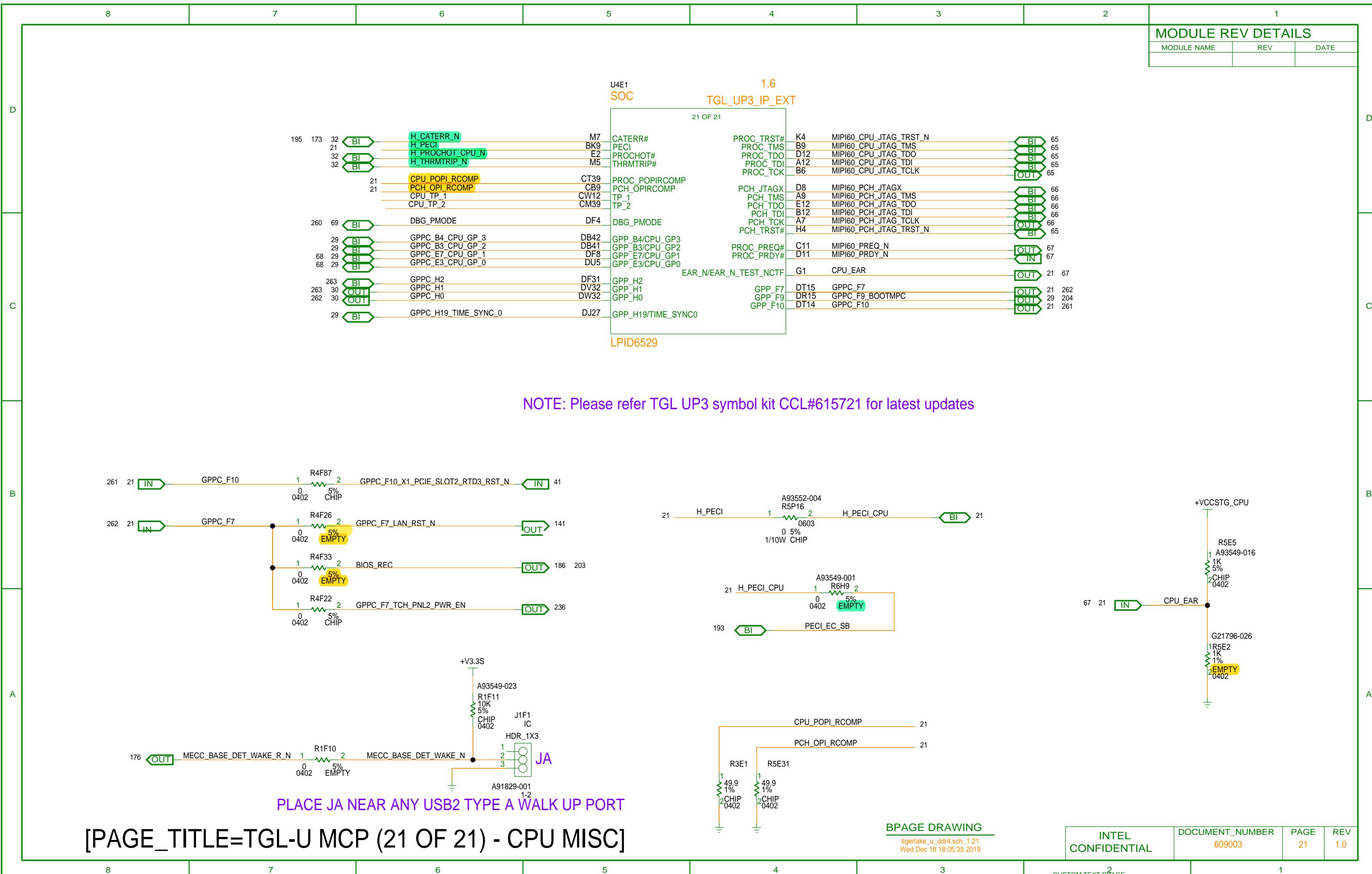




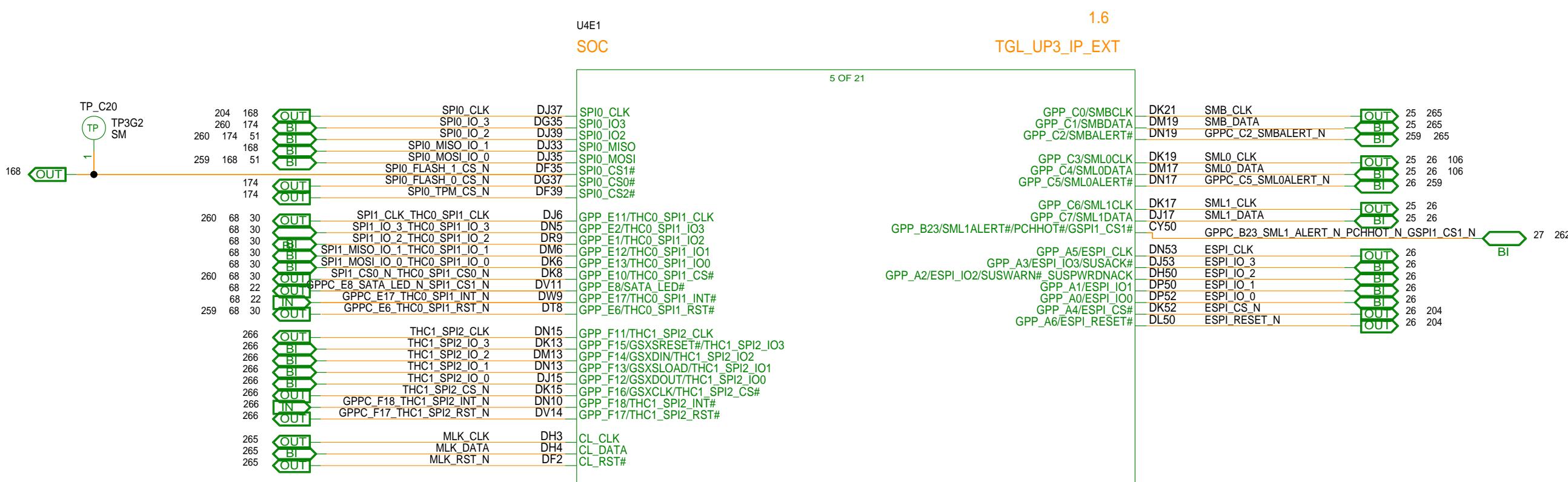
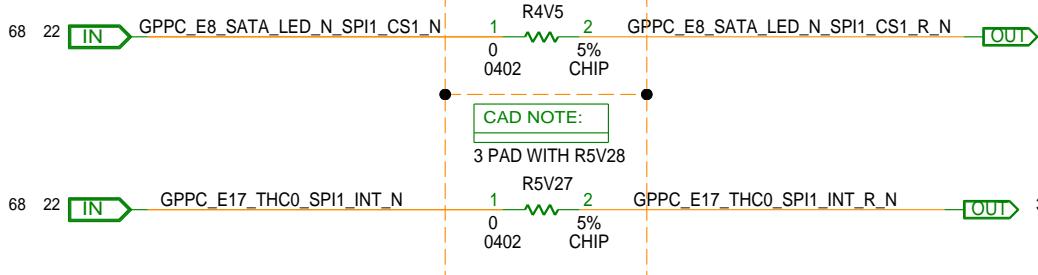
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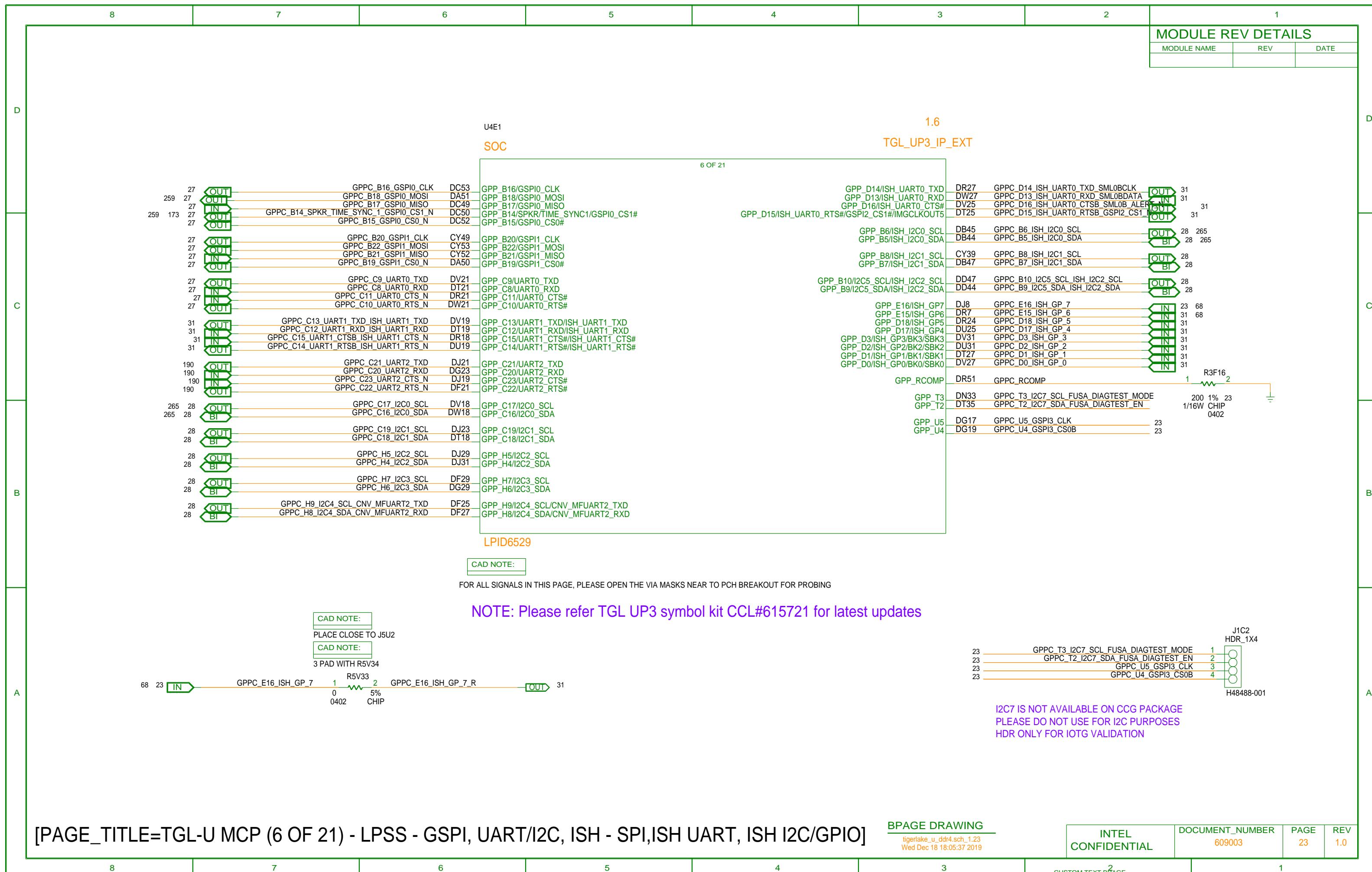
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<b>MODULE REV DETAILS</b>							
MODULE NAME						REV	DATE

CAD NOTE:  
PLACE CLOSE TO J5U2CAD NOTE:  
3 PAD WITH R4V4CAD NOTE:  
FOR ALL SIGNALS IN THIS PAGE, PLEASE OPEN THE VIA MASKS NEAR TO PCH BREAKOUT FOR PROBING

[PAGE\_TITLE=TGL-U MCP (5 OF 21) - LSIO - SPI, ESPI, THC, MLINK, SMLINK, SMBUS]

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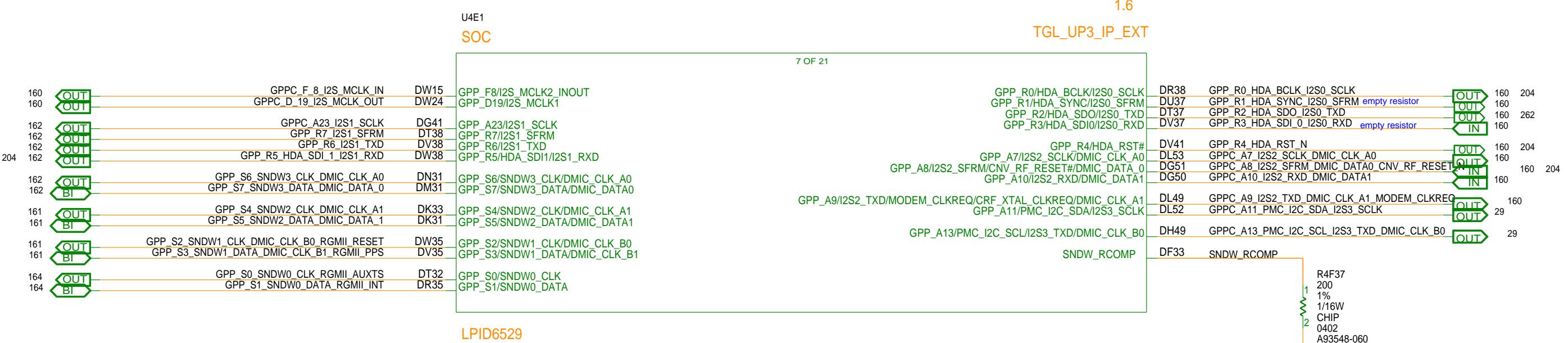
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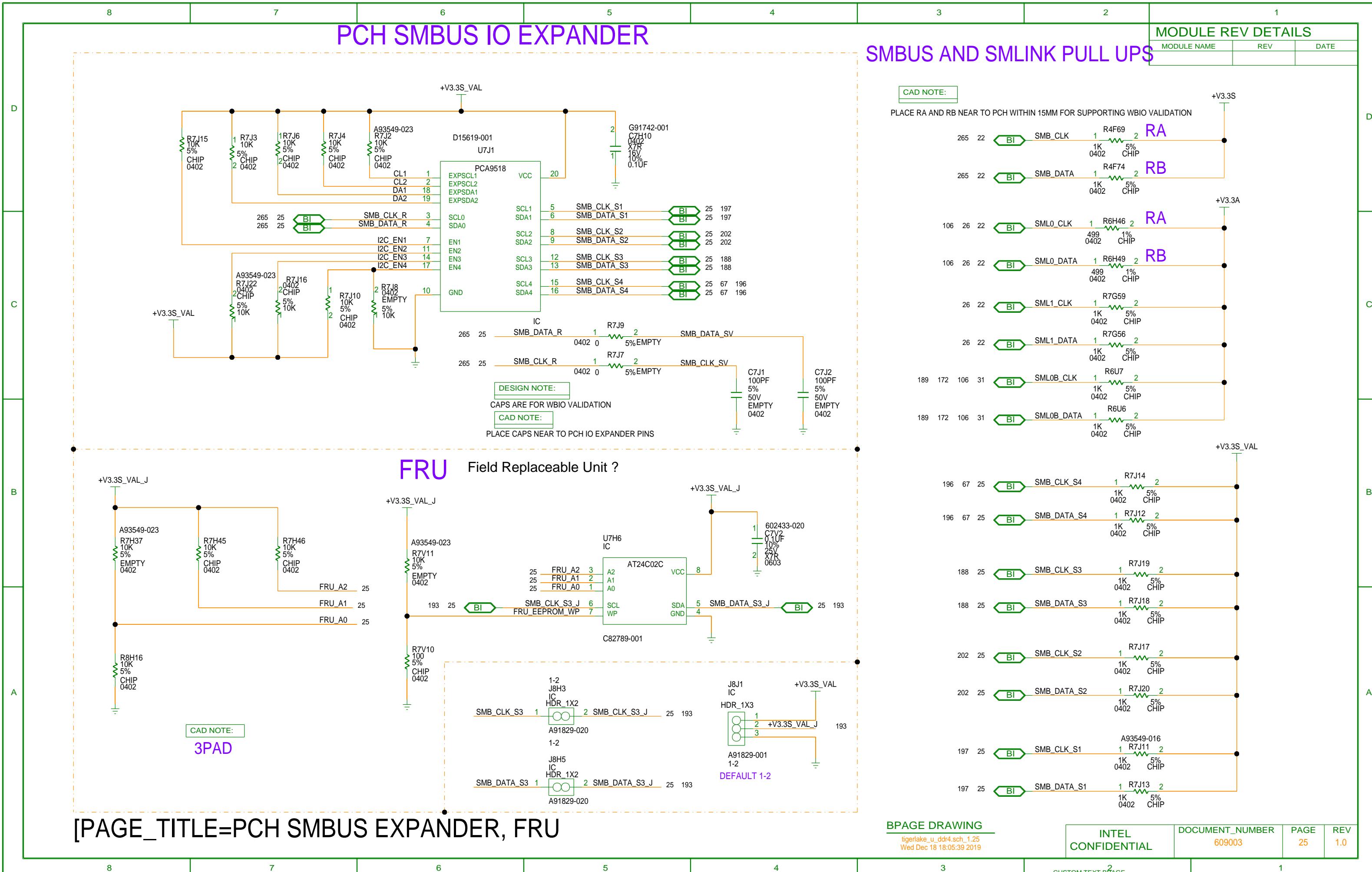
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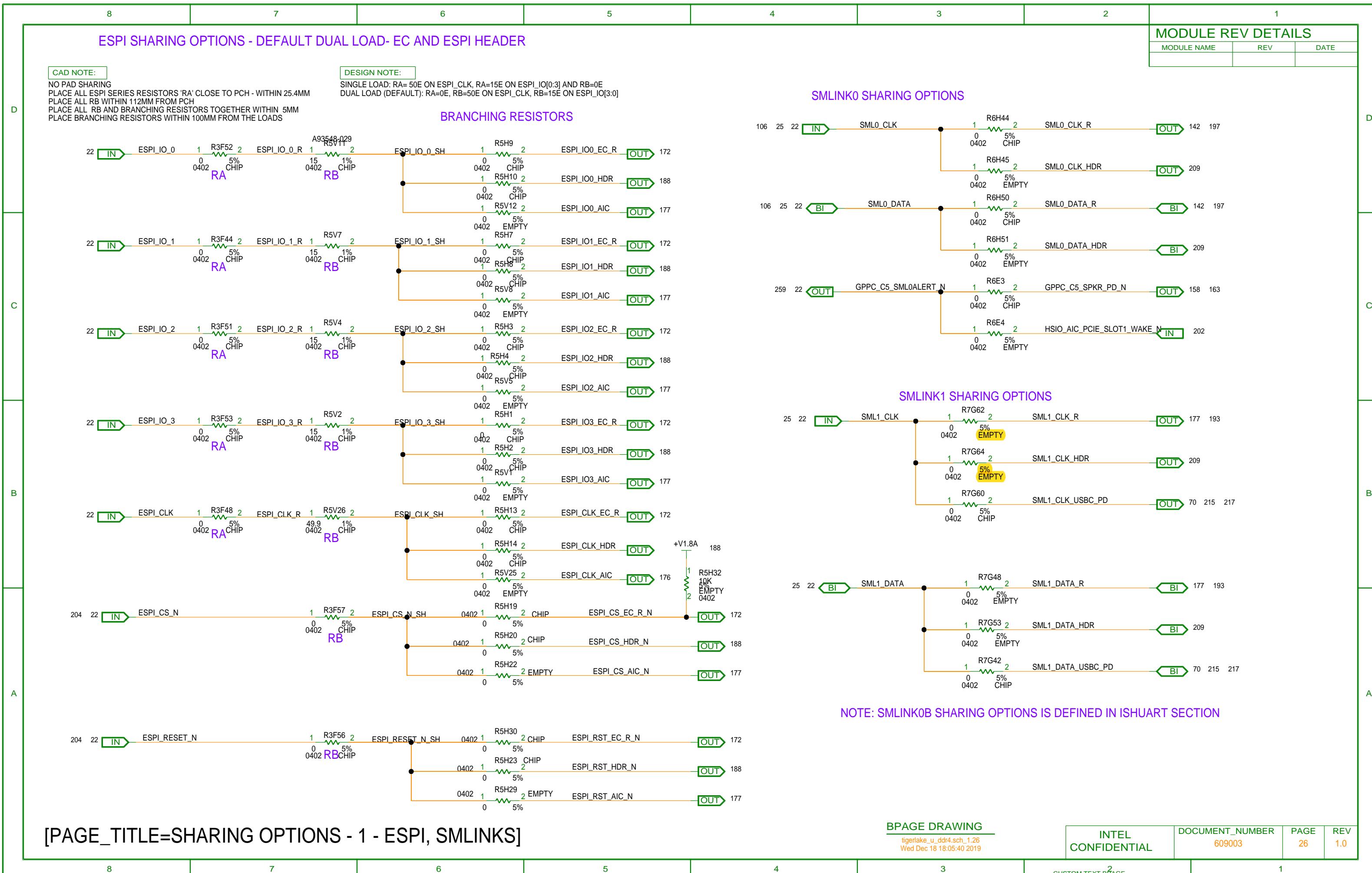
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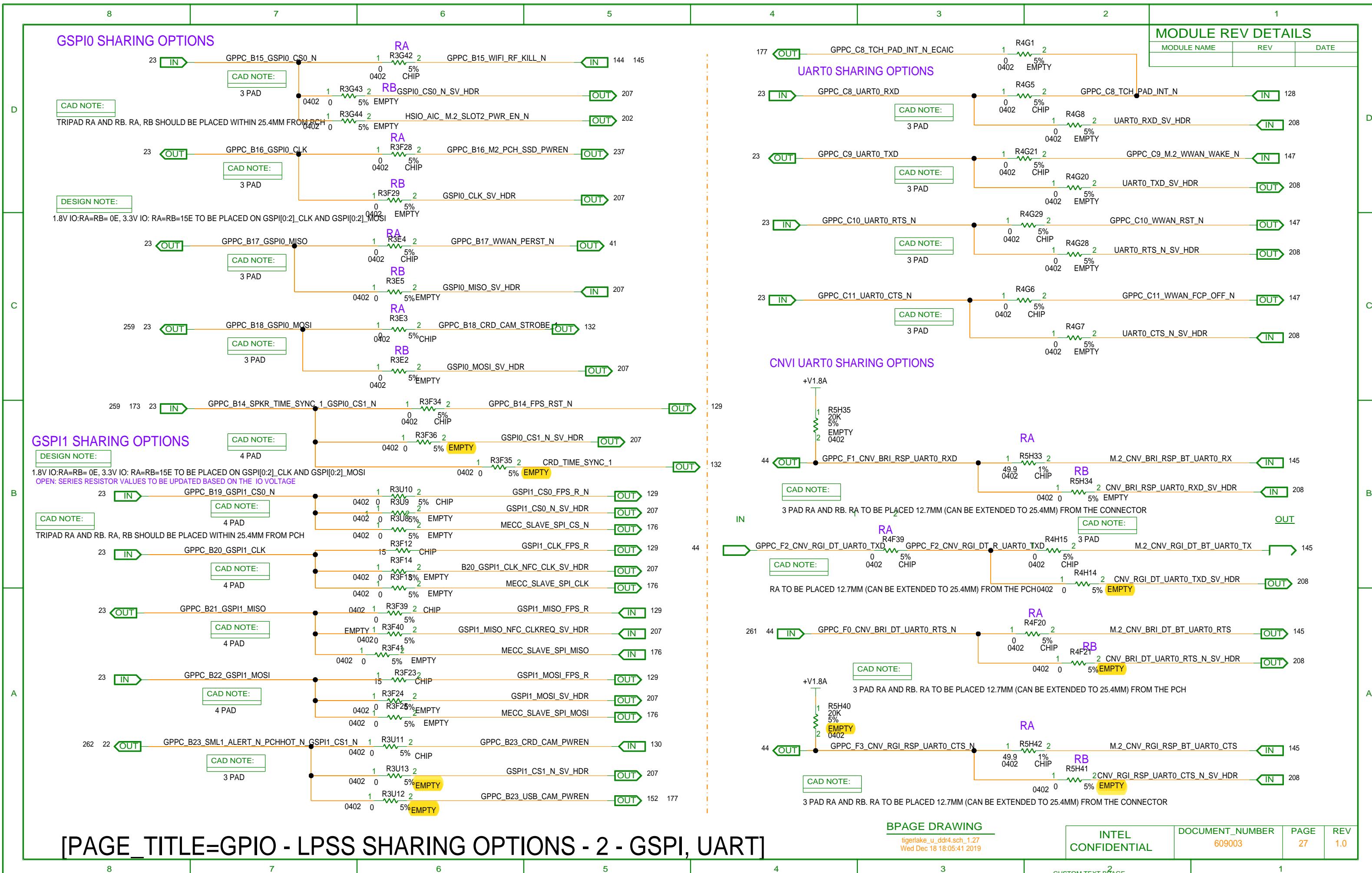
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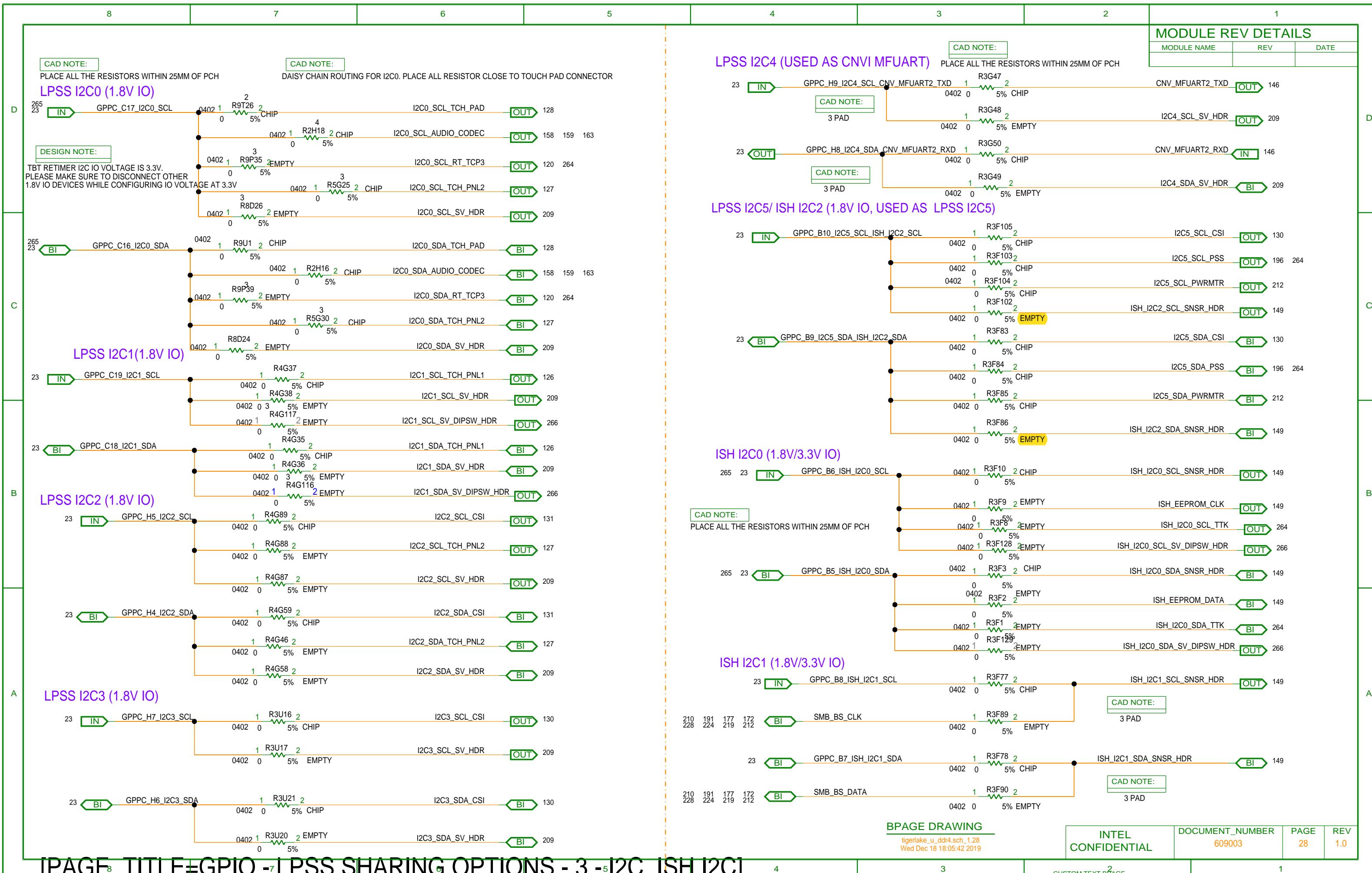


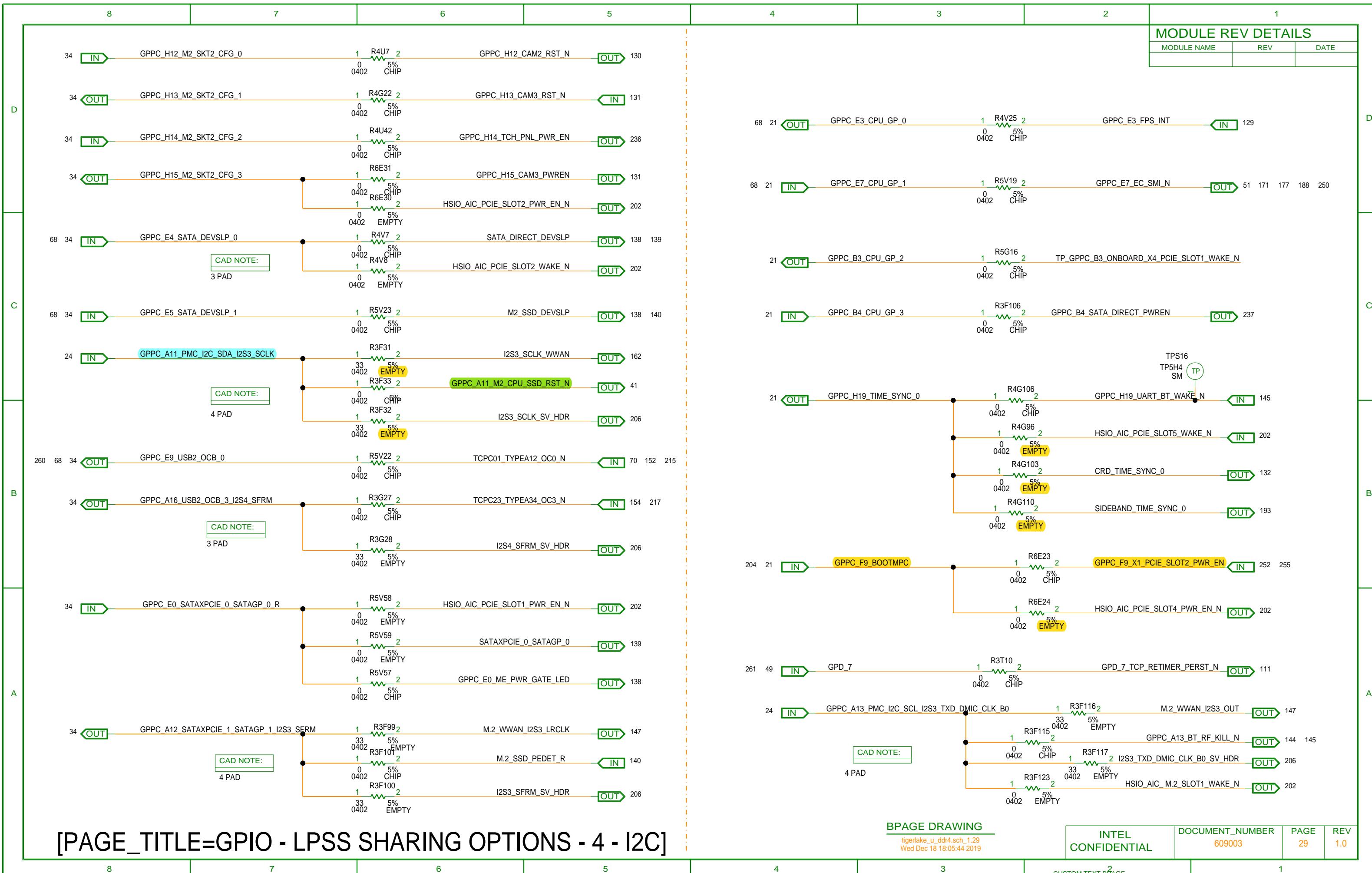
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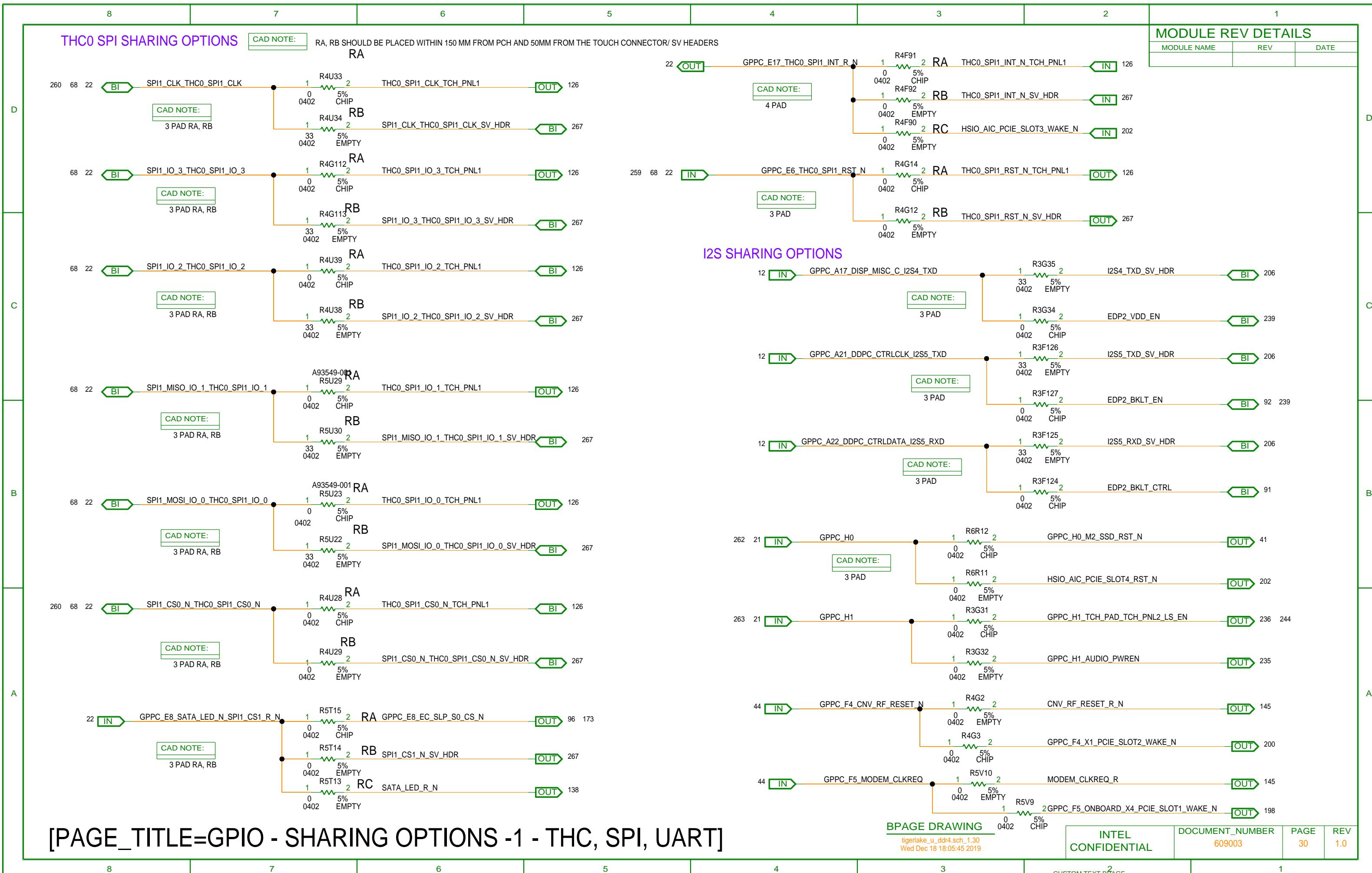


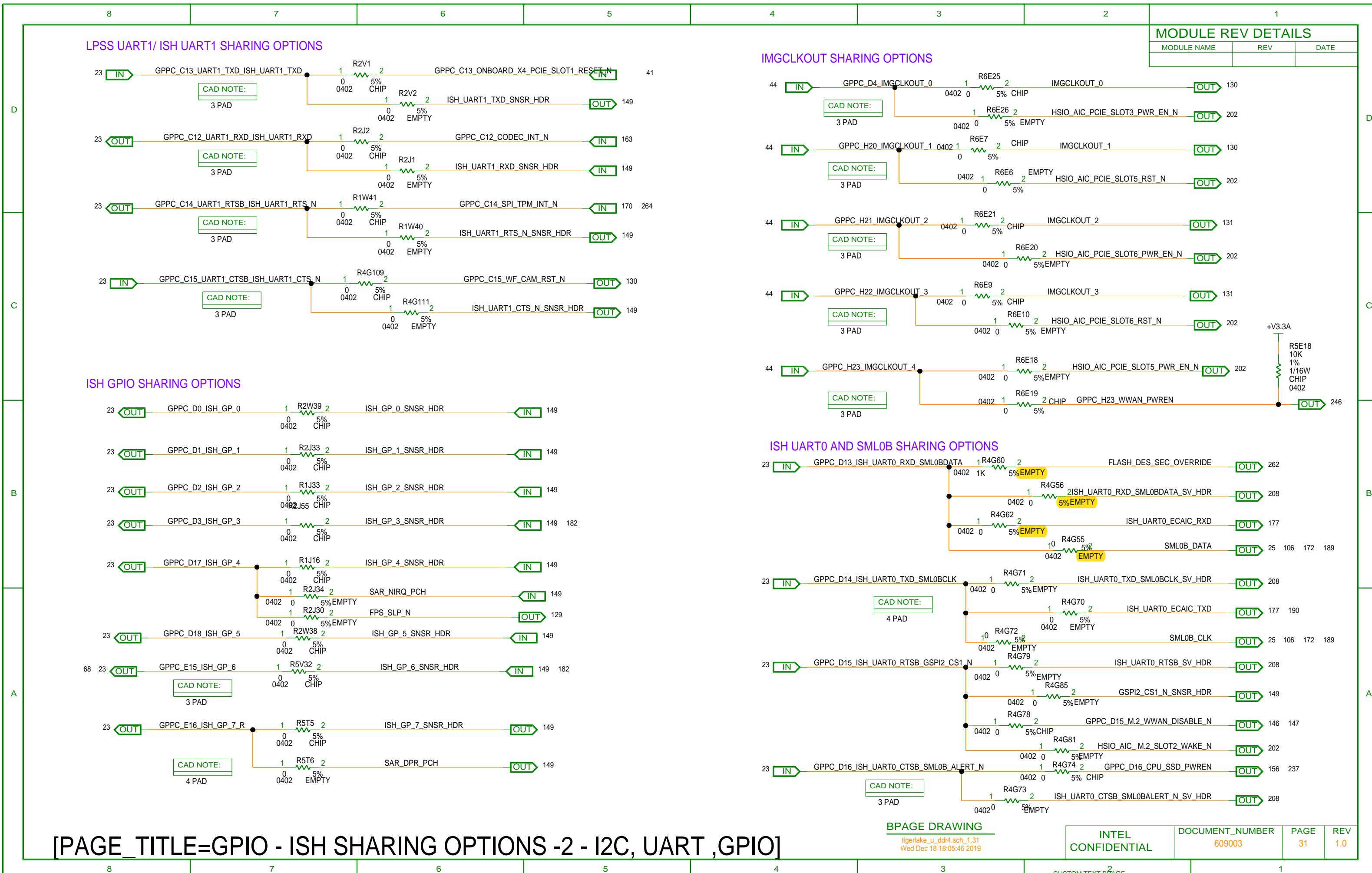






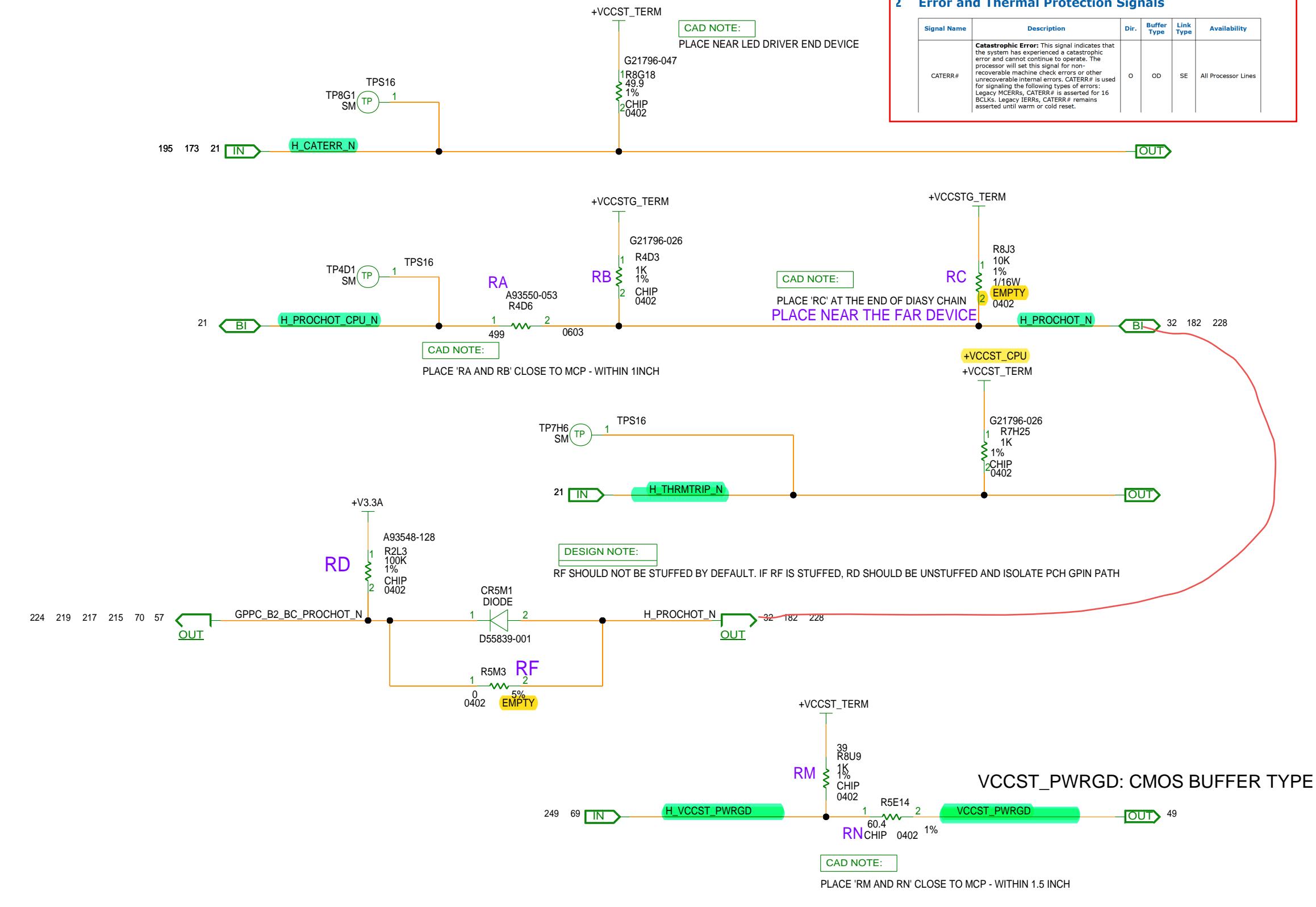






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# CPU SIDEBAND SIGNALS

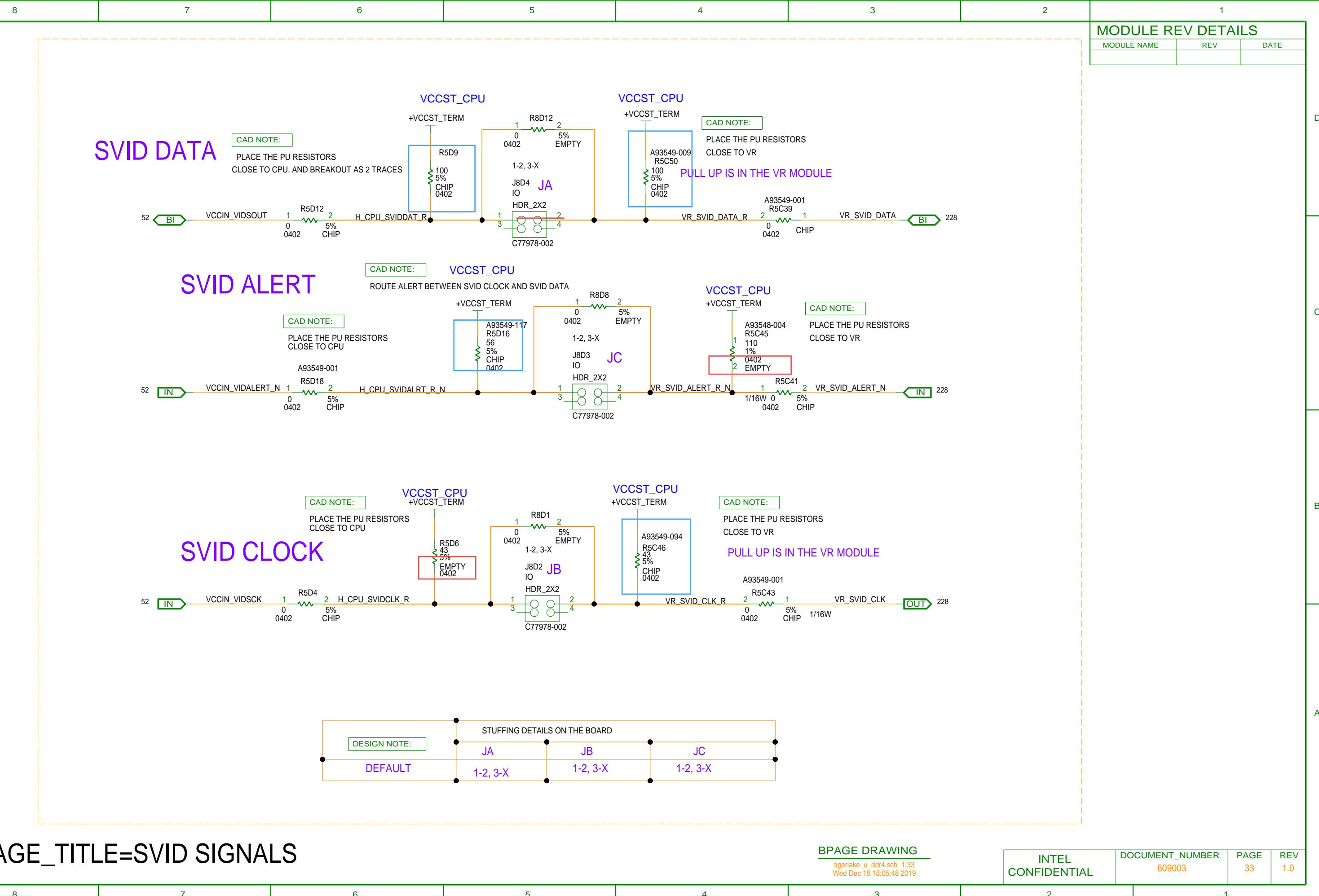


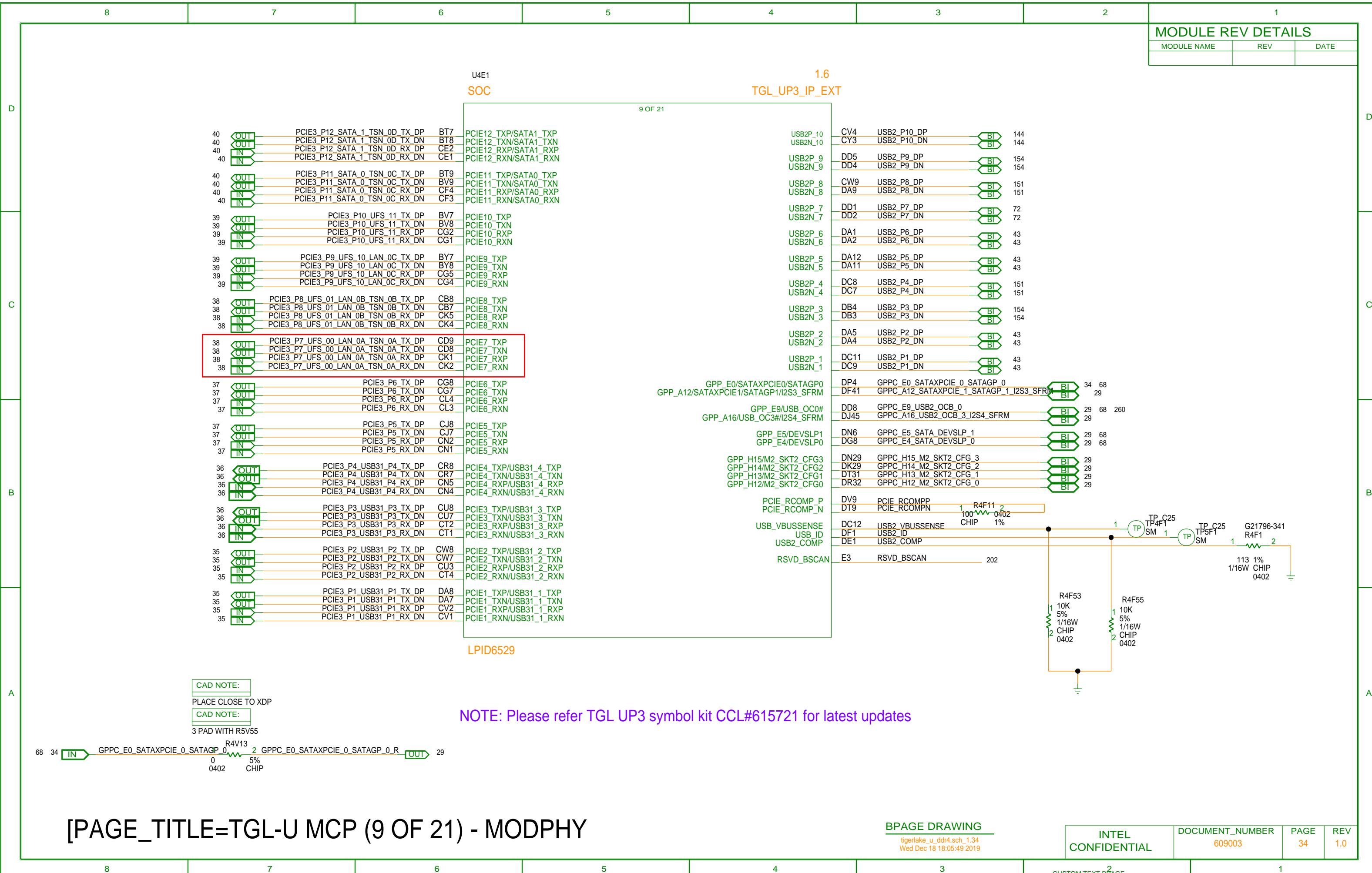
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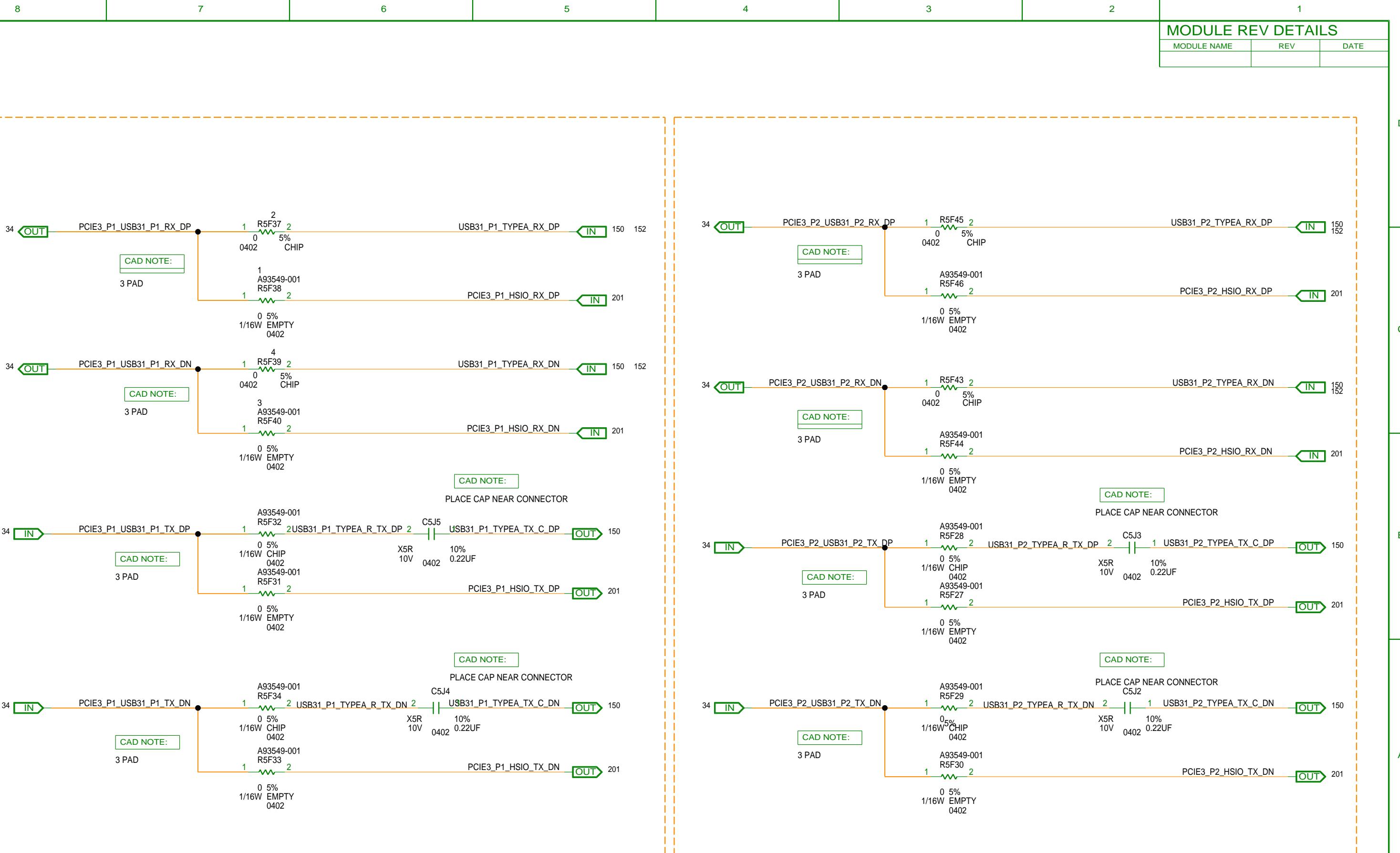
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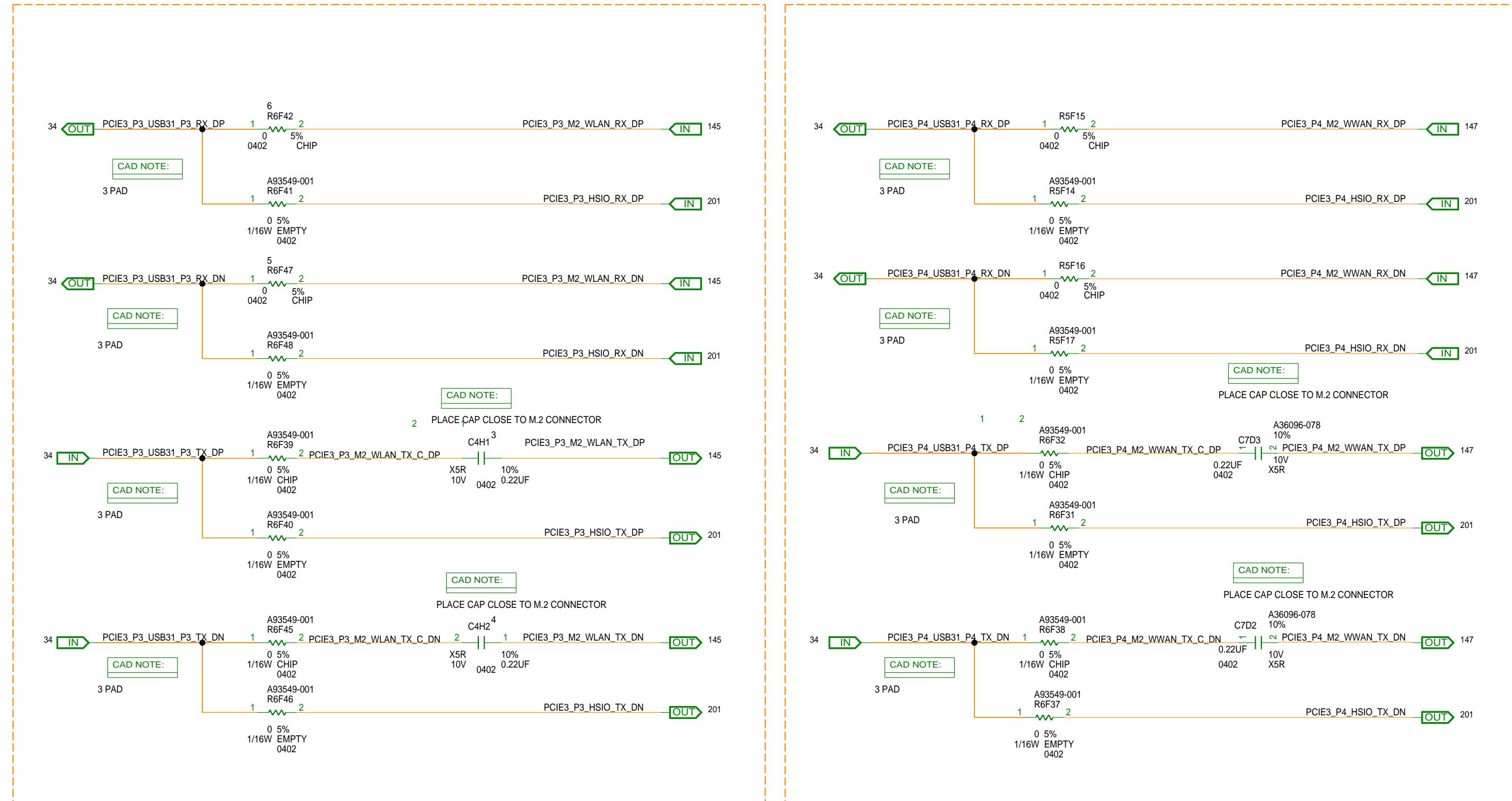
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MODULE NAME	REV	DATE					



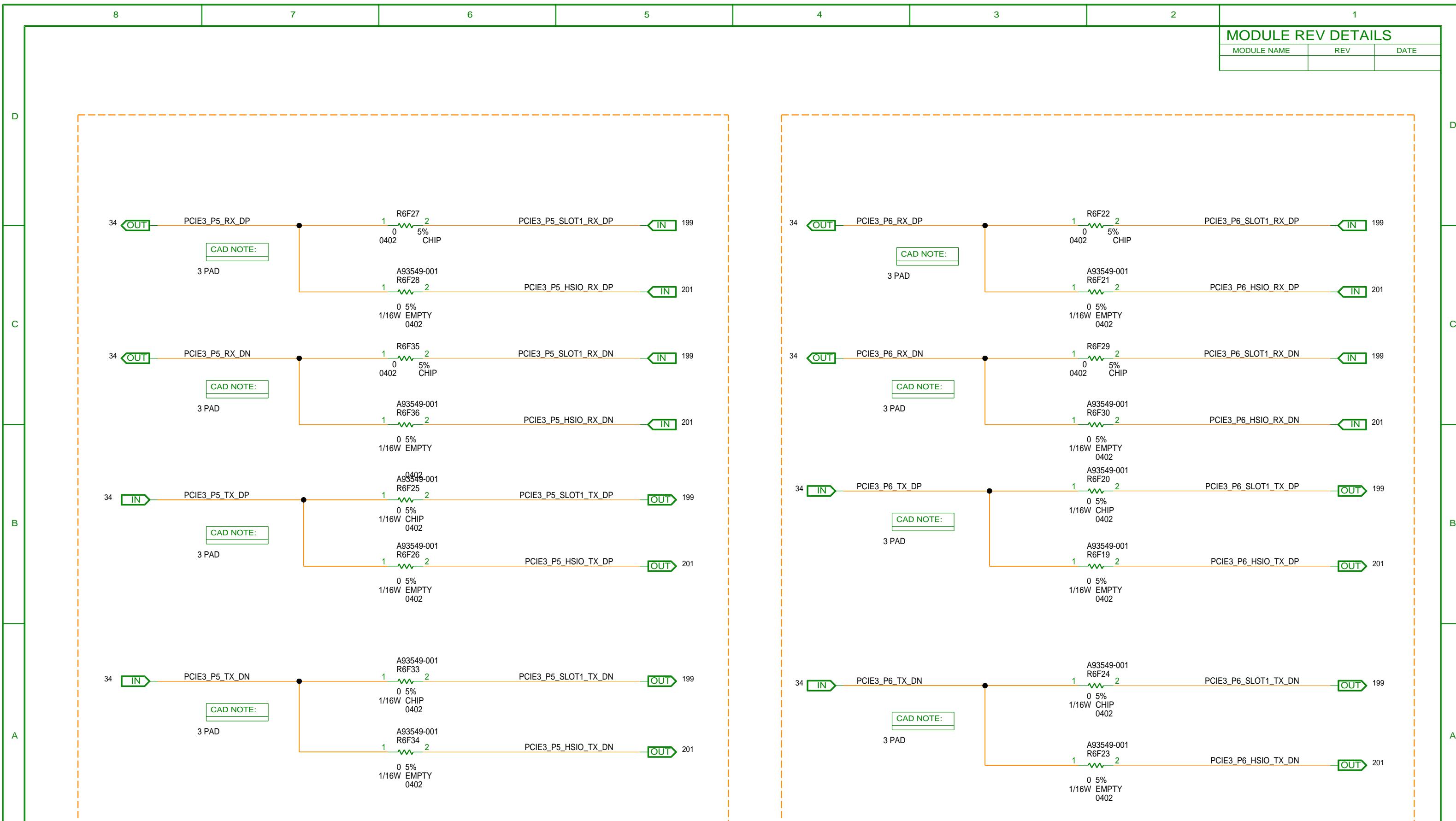
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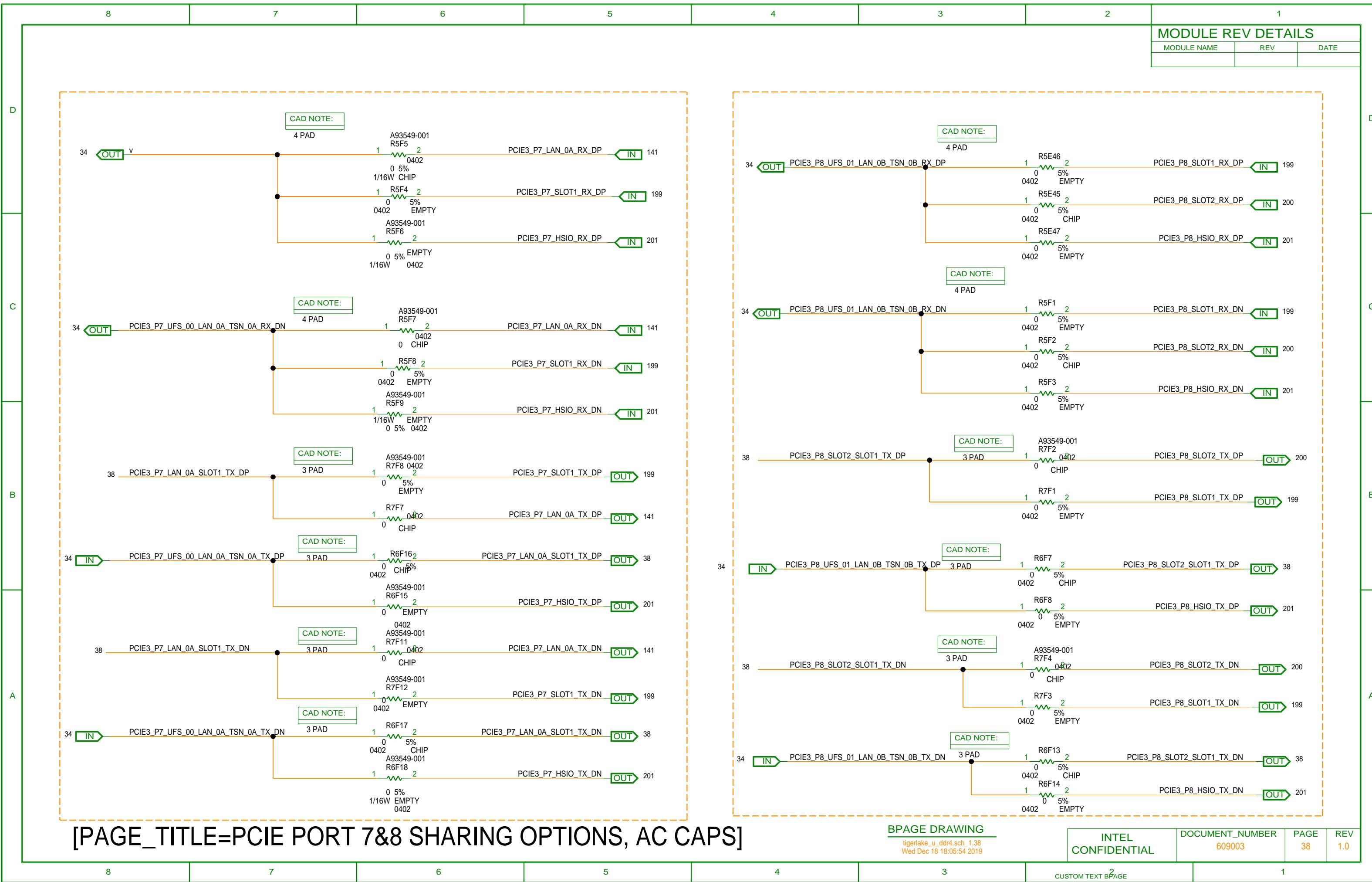
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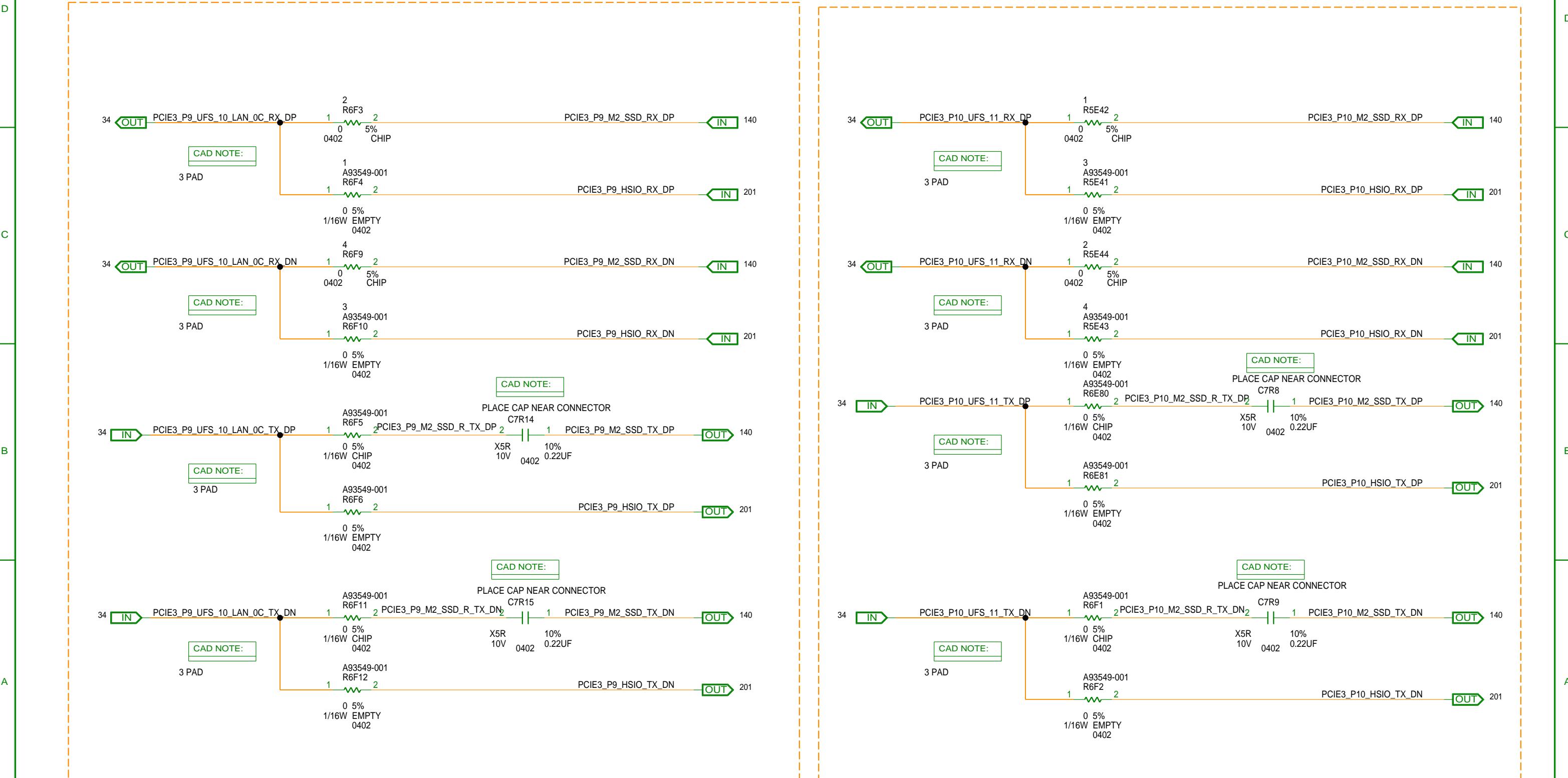
[PAGE\_TITLE=PCIE PORT 5&amp;6 SHARING OPTIONS, AC CAPS]

BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.37  
Wed Dec 18 18:05:52 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 37	REV 1.0
CUSTOM TEXT 2 PAGE			



8	7	6	5	4	3	2	1
MODULE REV DETAILS							
MODULE NAME	REV	DATE					

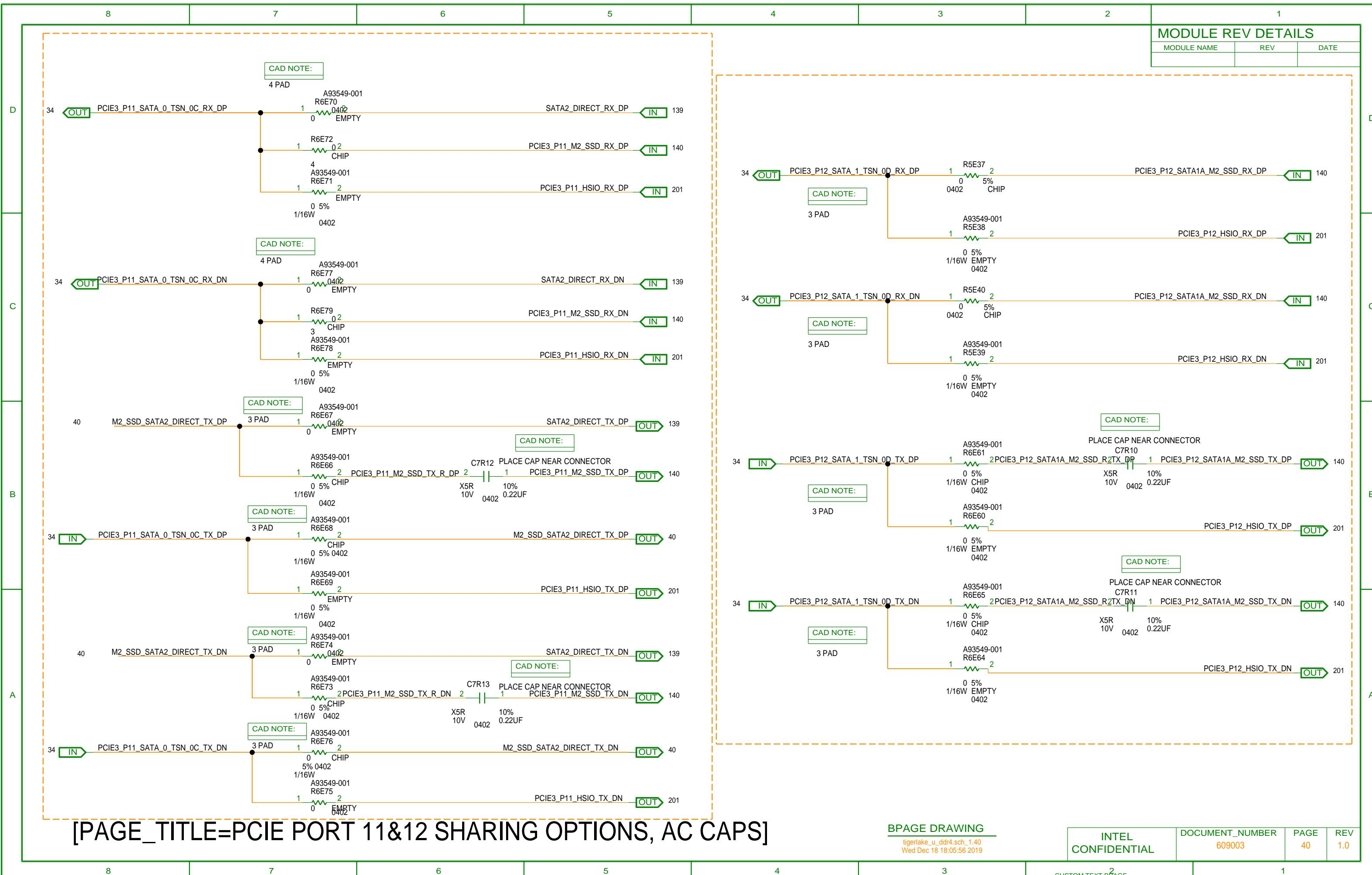


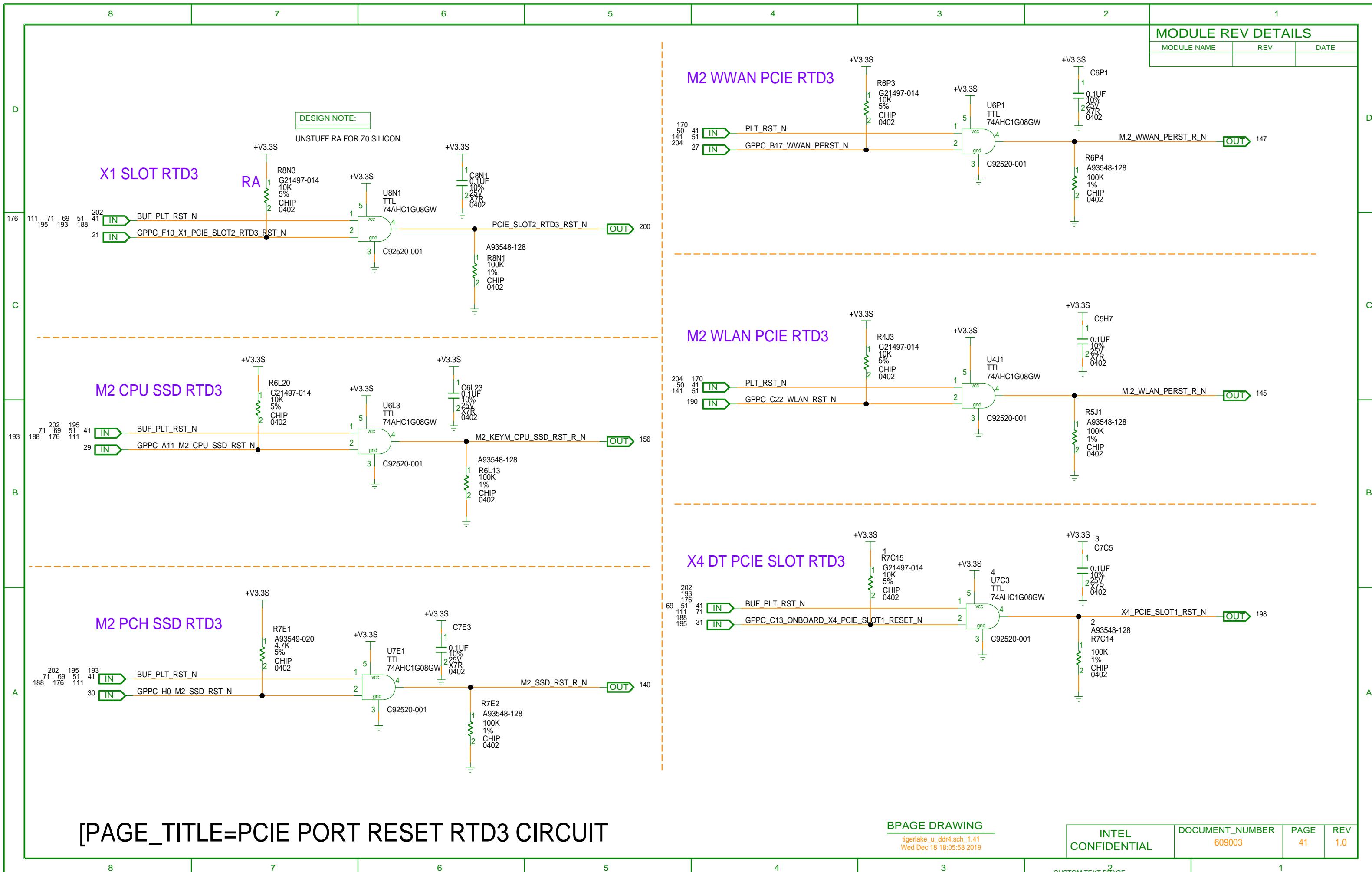
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BPAGE DRAWING  
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Wed Dec 18 18:05:55 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	39	1	1.0

CUSTOM TEXT BPAGE





8	7	6	5	4	3	2	1
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MODULE NAME		REV	DATE				

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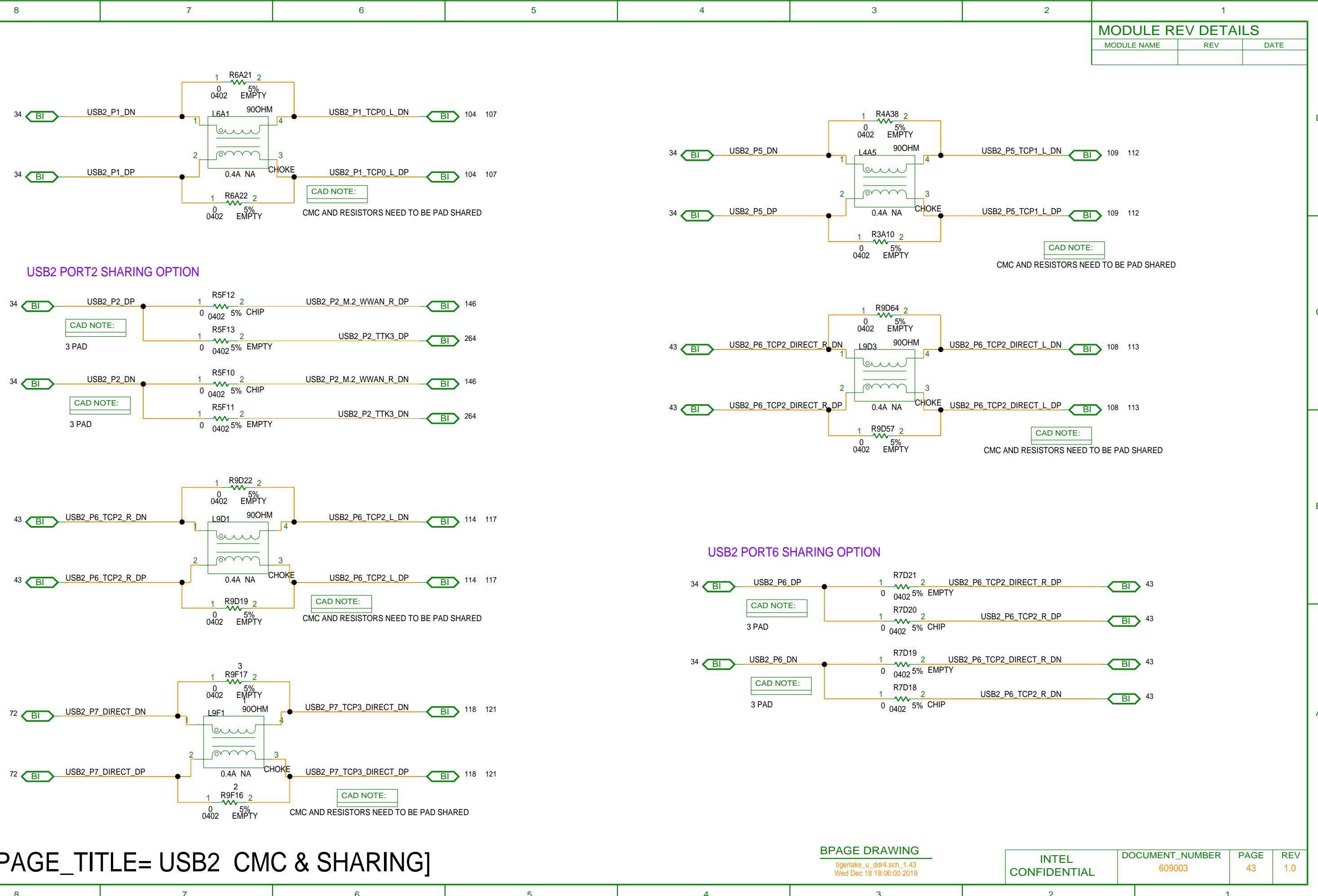
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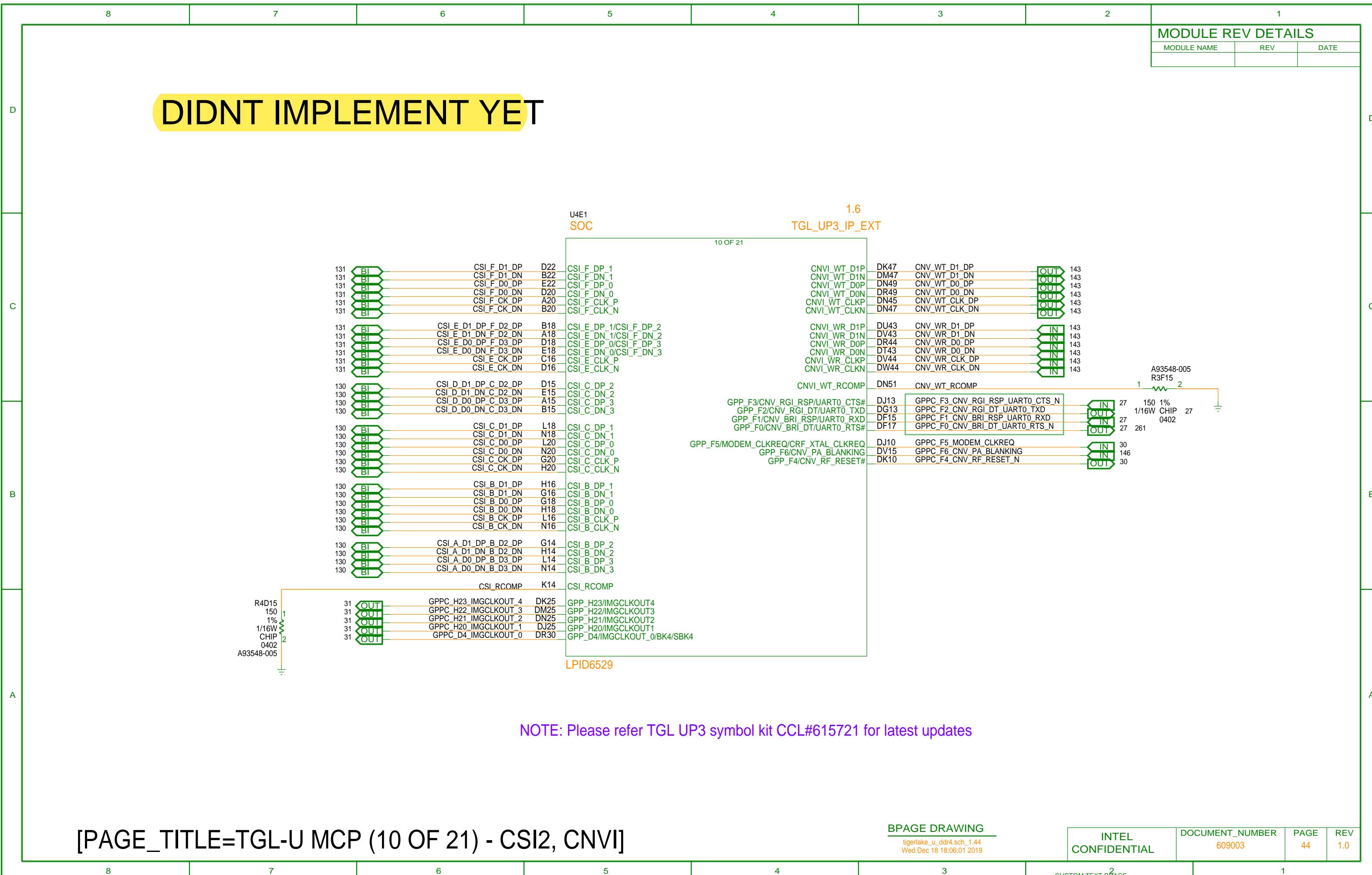
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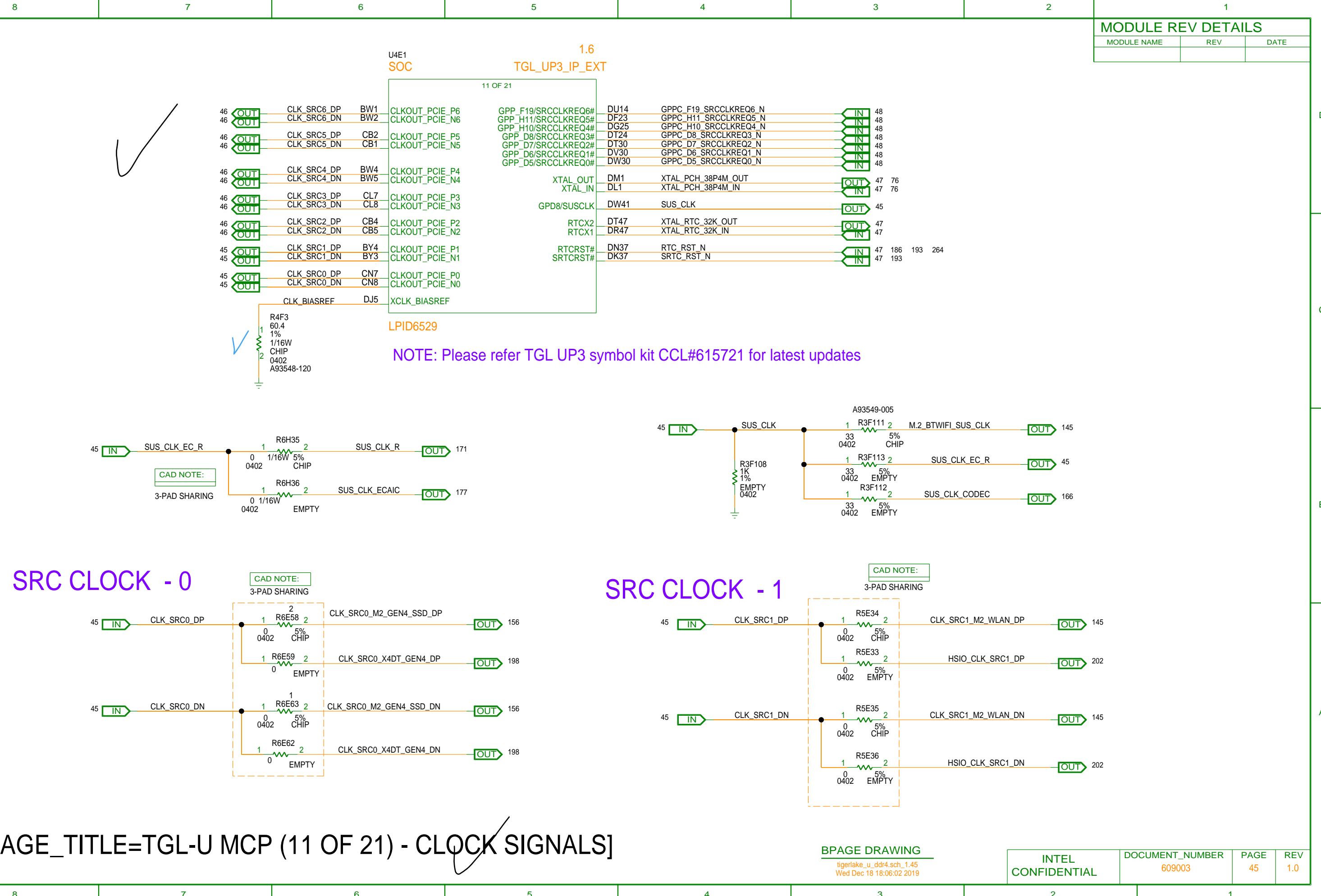
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Tue Oct 15 12:49:02 2019

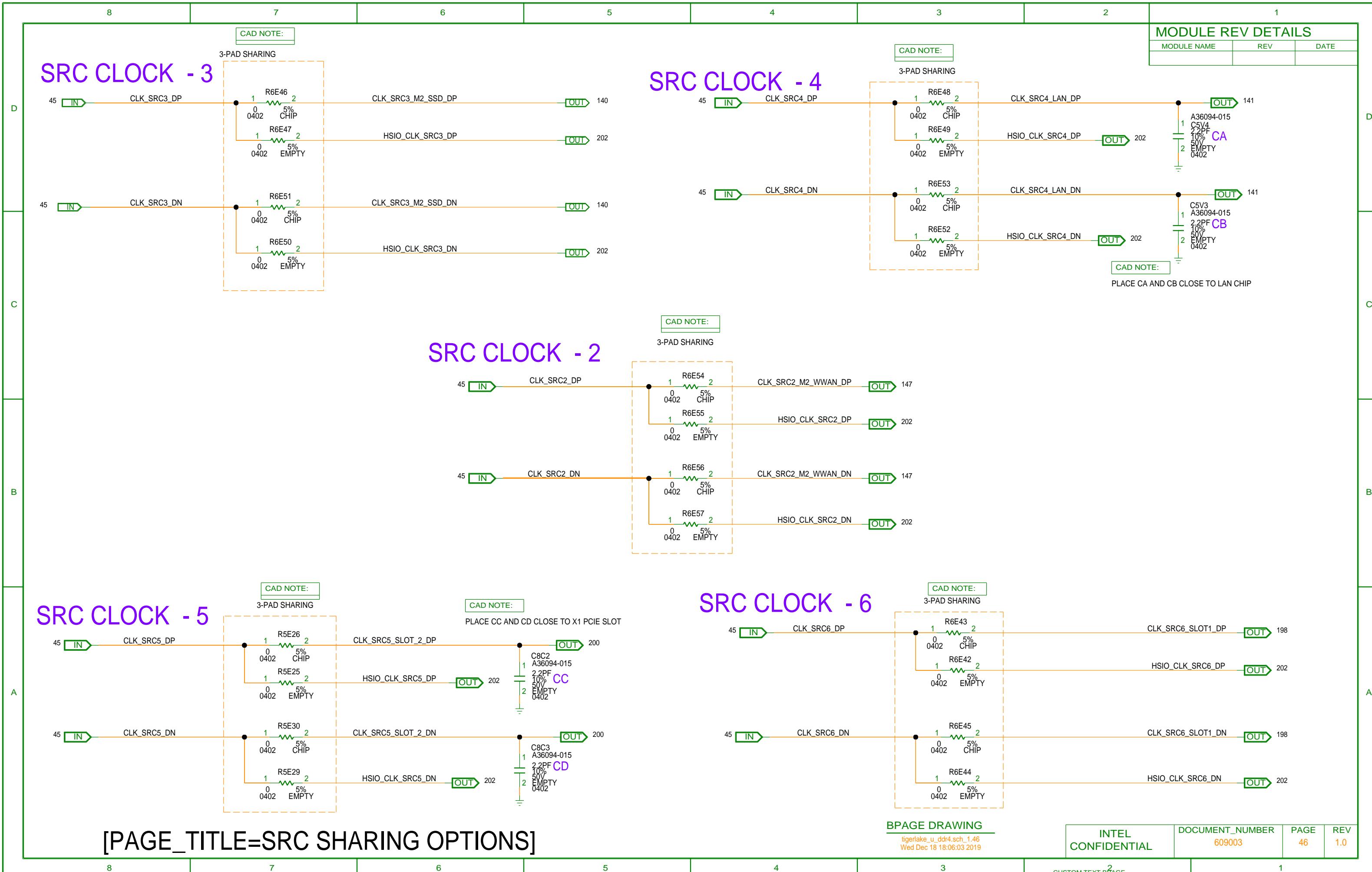
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	42	1.0

8	7	6	5	4	3	CUSTOM TEXT <sup>2</sup> PAGE	1
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8	7	6	5	4	3	2	1
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**MODULE REV DETAILS**

MODULE NAME	REV	DATE

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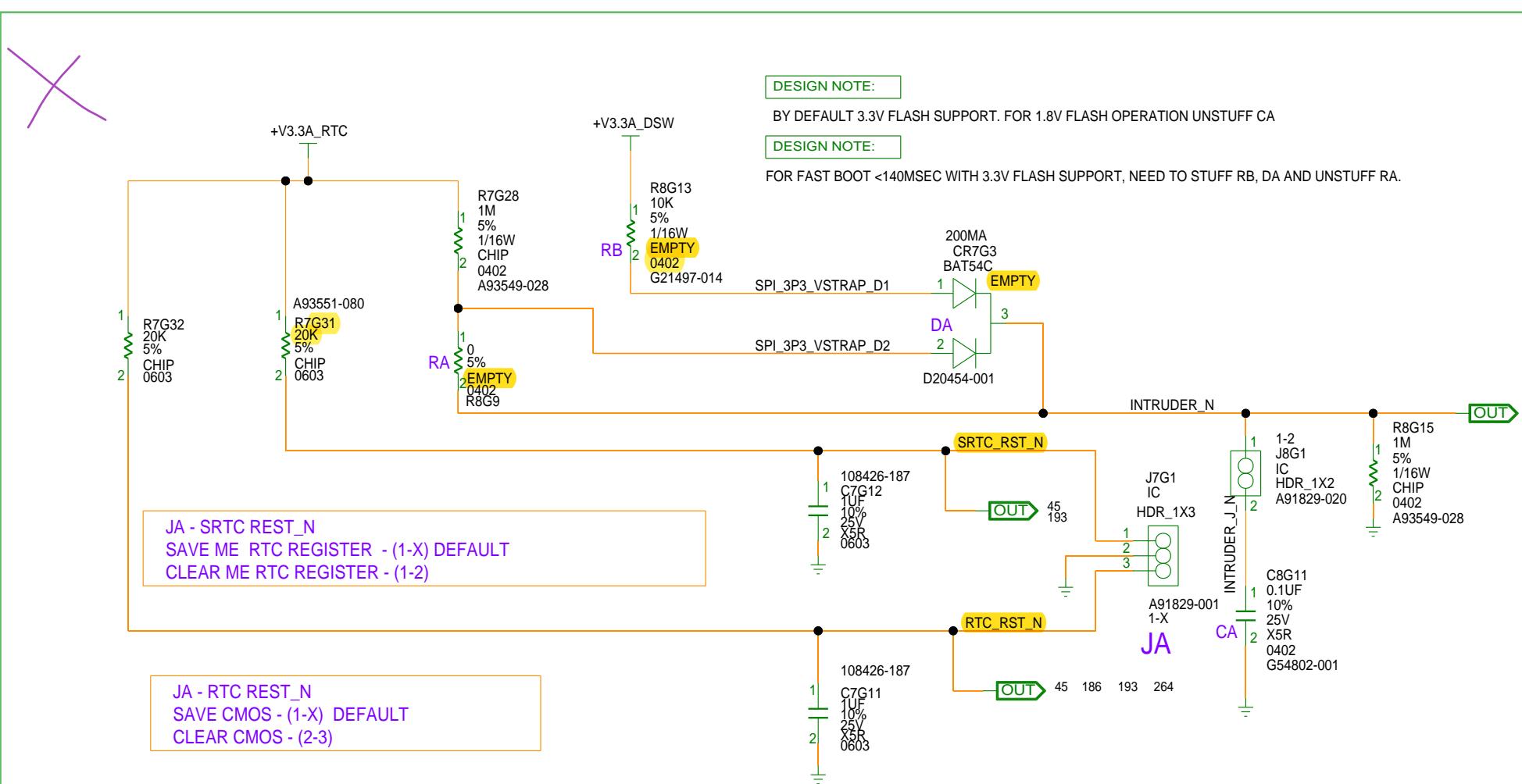
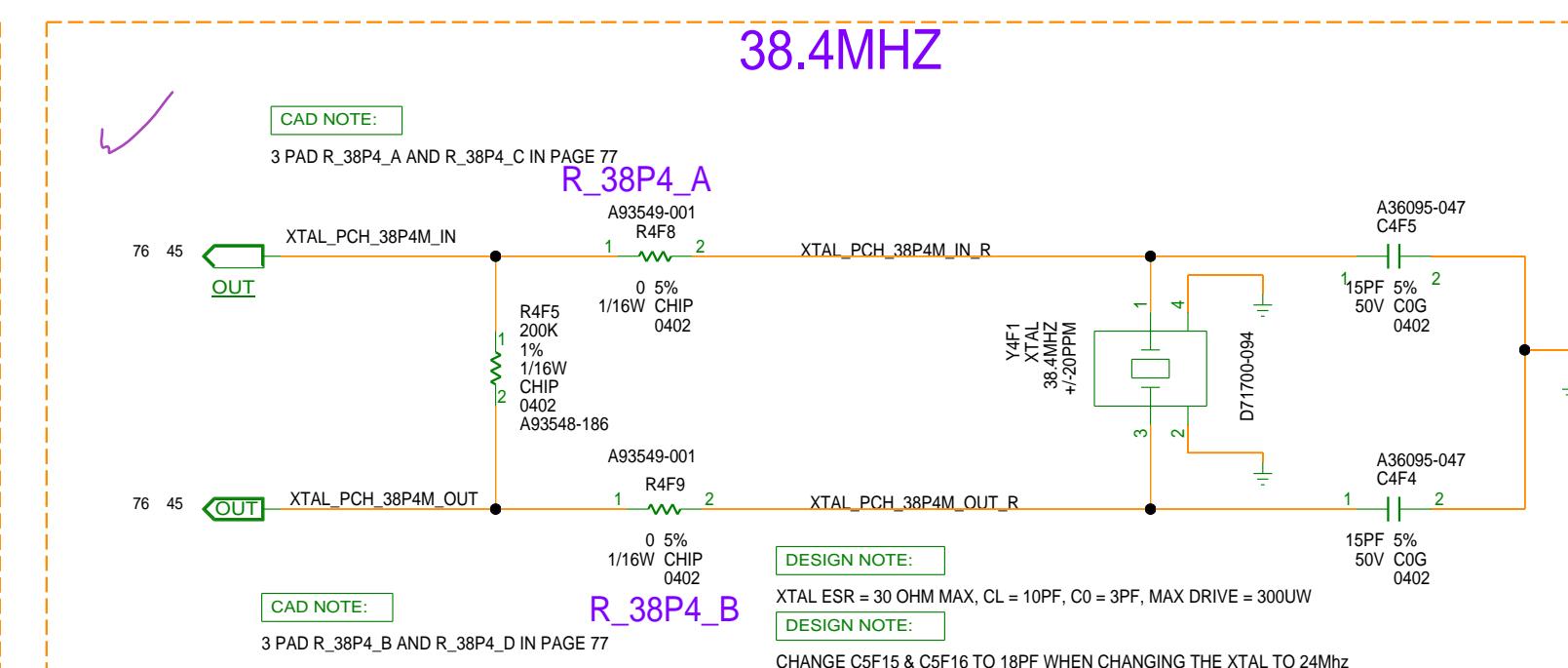
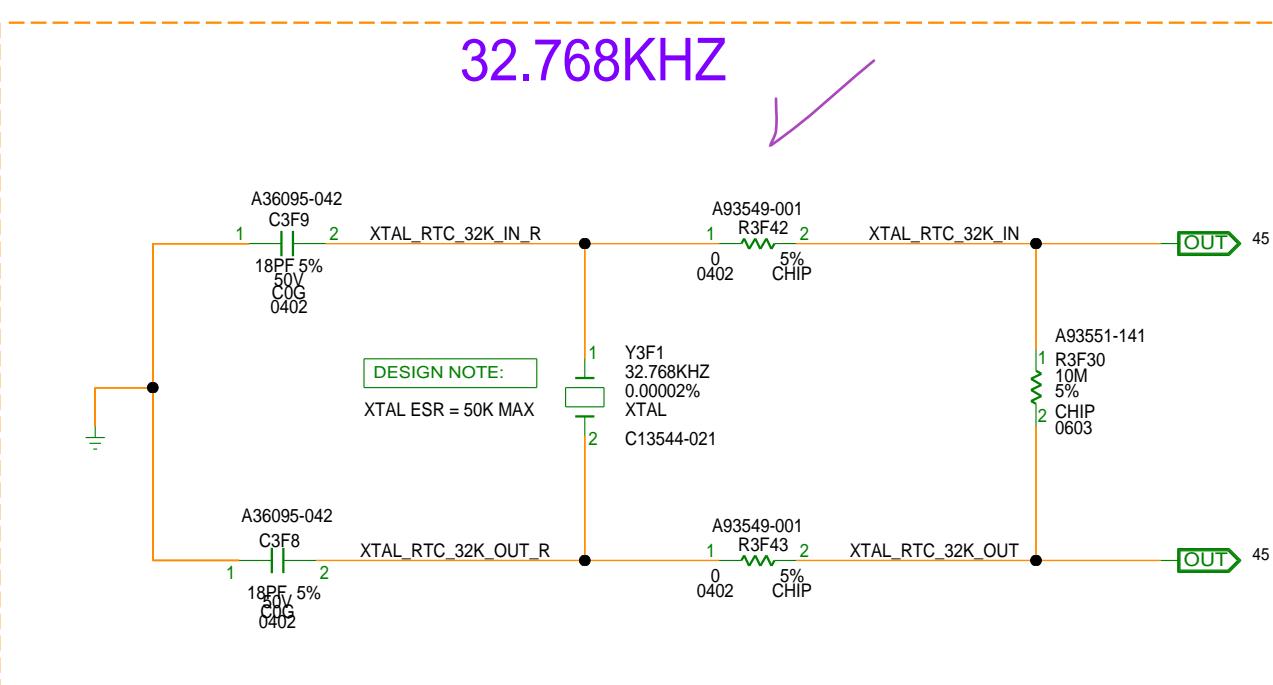
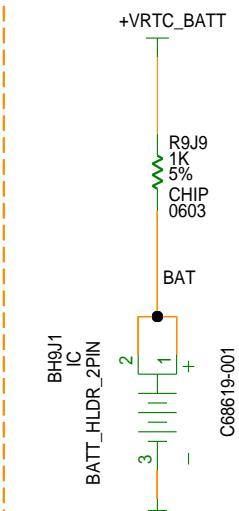
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**+V3.3A\_RTC GENERATION**

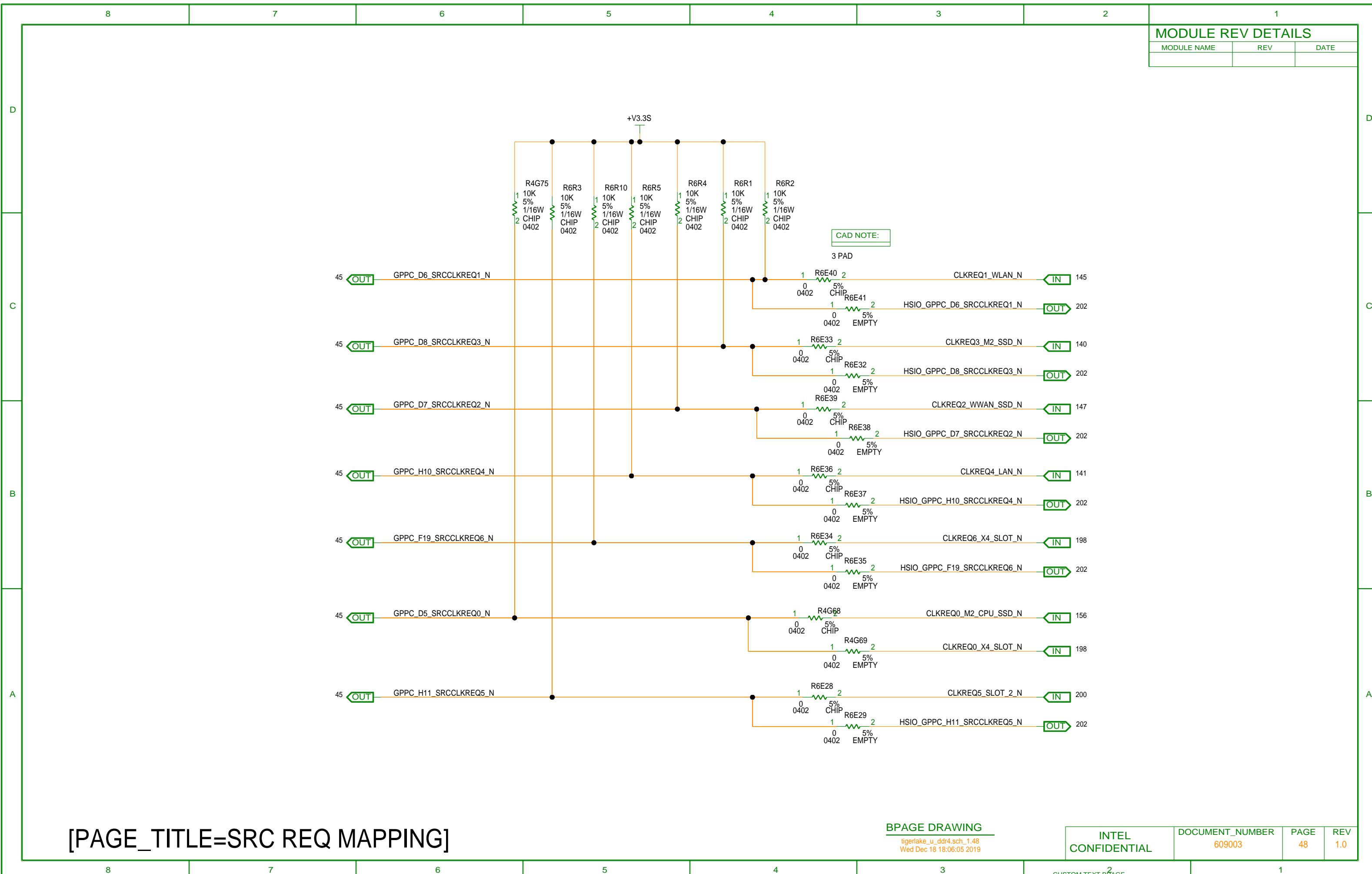
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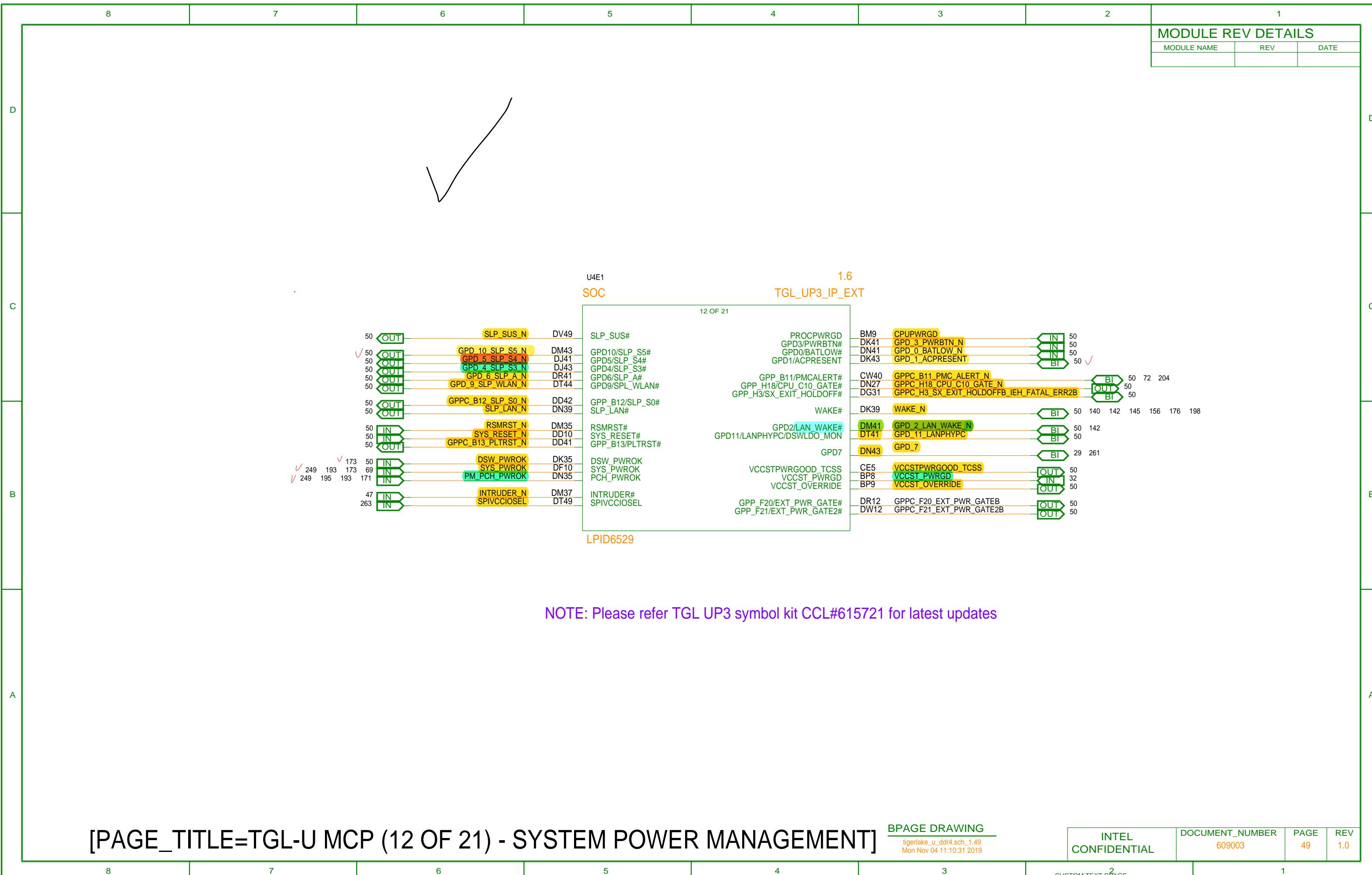
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Wed Dec 18 18:06:04 2019

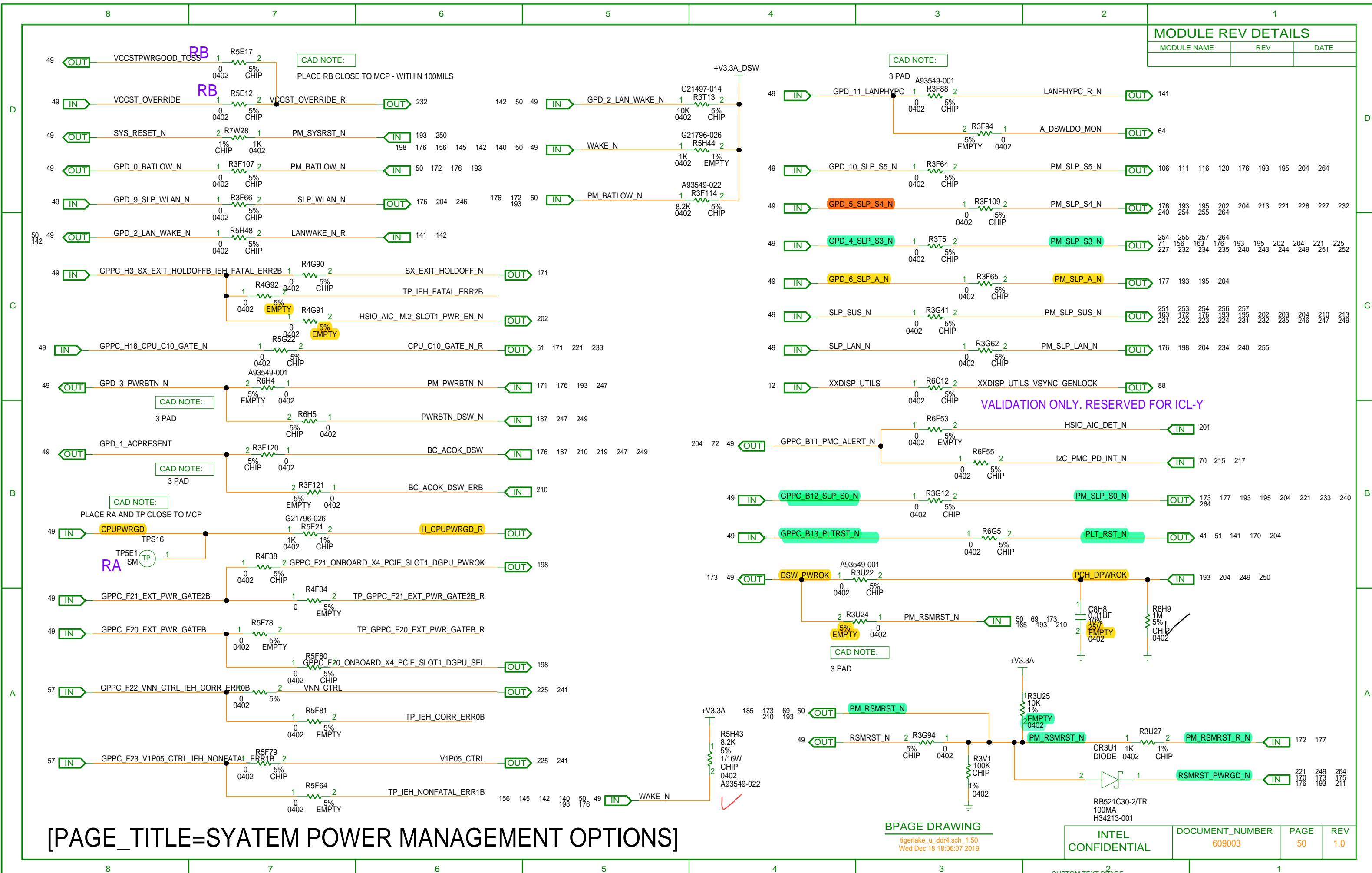
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
INTEL CONFIDENTIAL	609003	47	1.0

8	7	6	5	4	3	2	1
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CUSTOM TEXT BPAGE

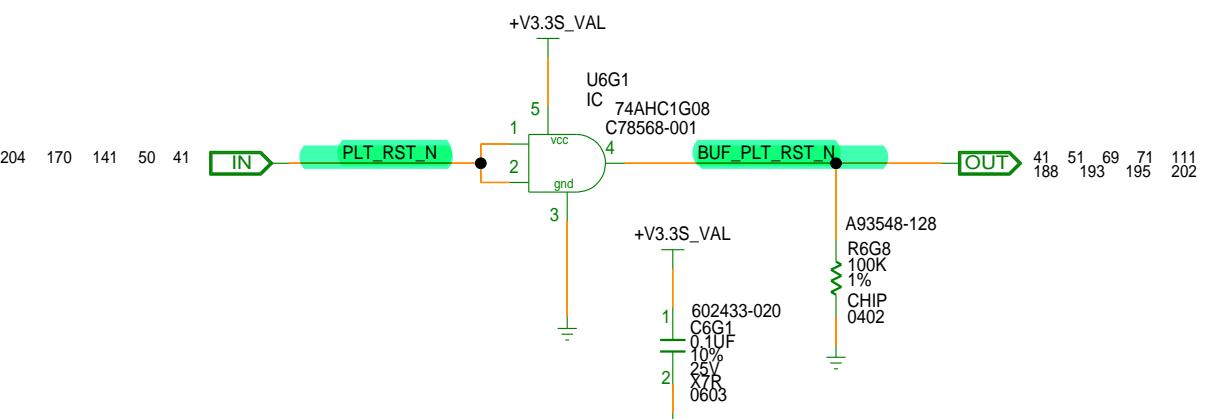
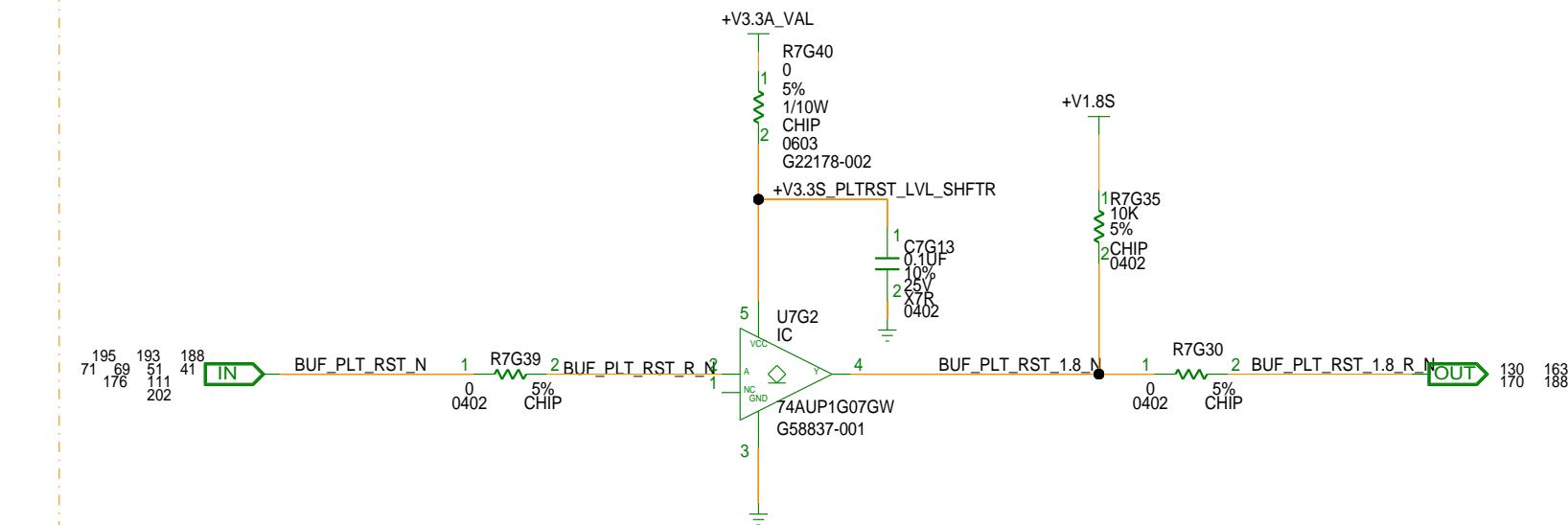






8	7	6	5	4	3	2	1
<b>MODULE REV DETAILS</b>							

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**BUFFER TO REDUCE LOADING ON PLT\_RST\_N****PLATFORM RESET LEVEL SHIFTER - 3.3V TO 1.8V**

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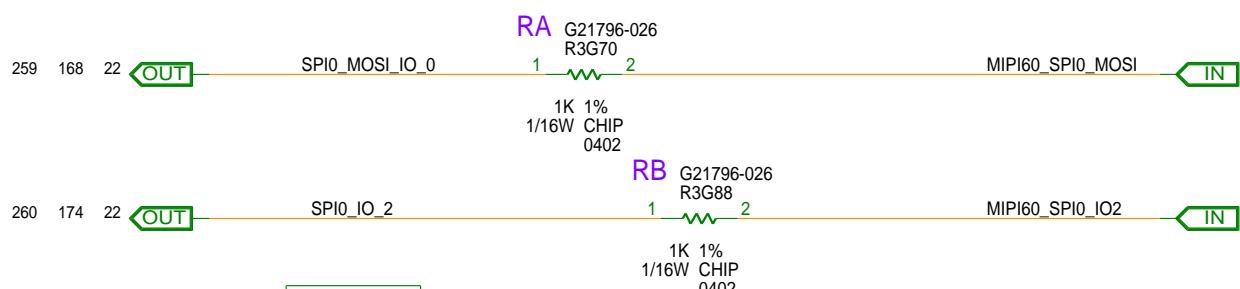
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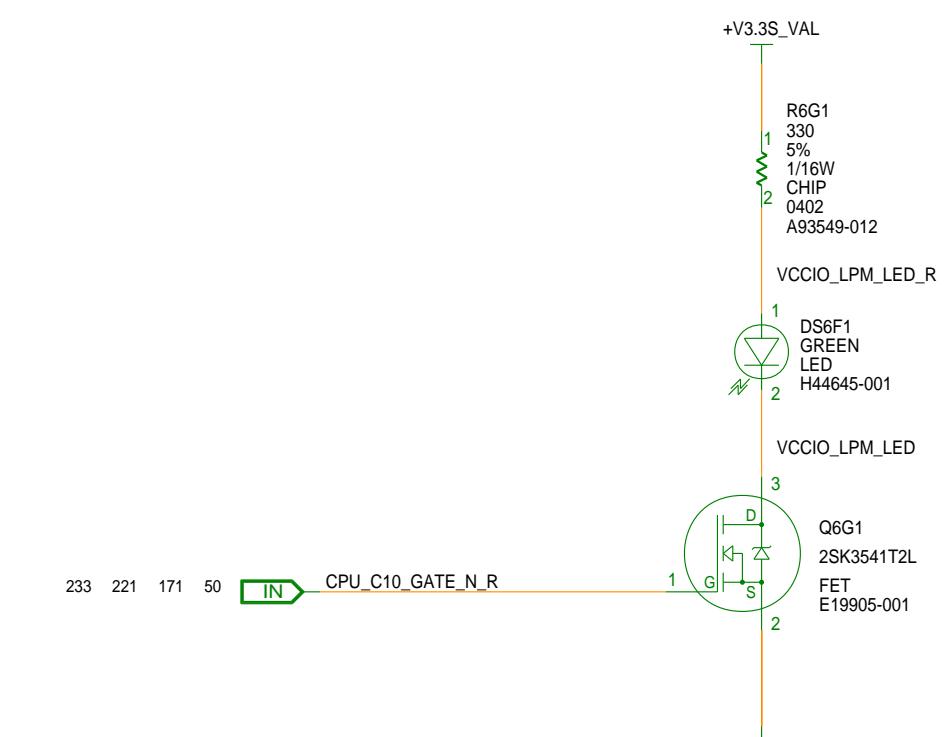
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**CAD NOTE:**  
RA AND RB RESISTORS NEED TO BE PLACED NEAR TO MCP, WITHOUT STUB ON SPI



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**MODULE REV DETAILS**

MODULE NAME	REV	DATE

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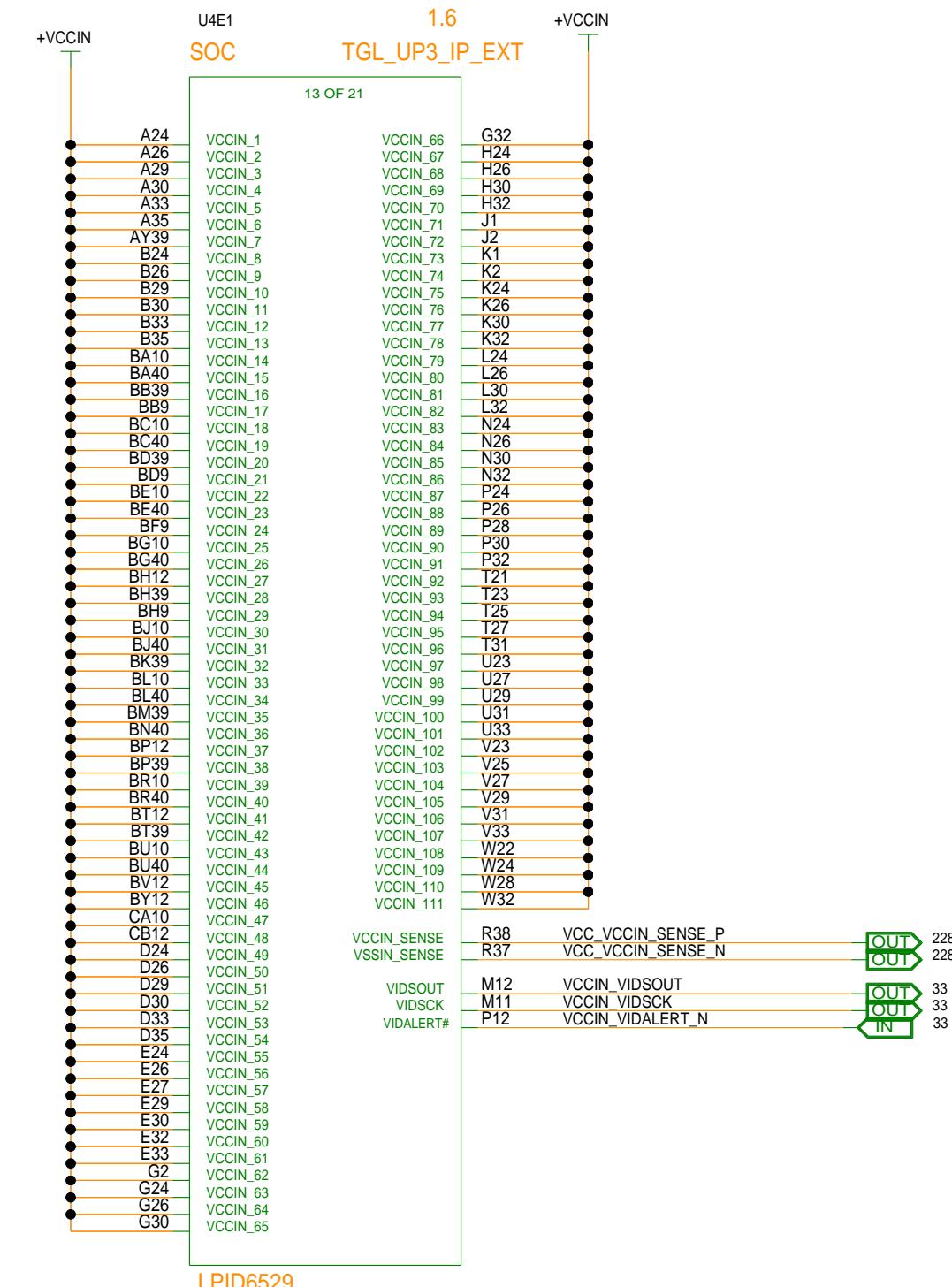
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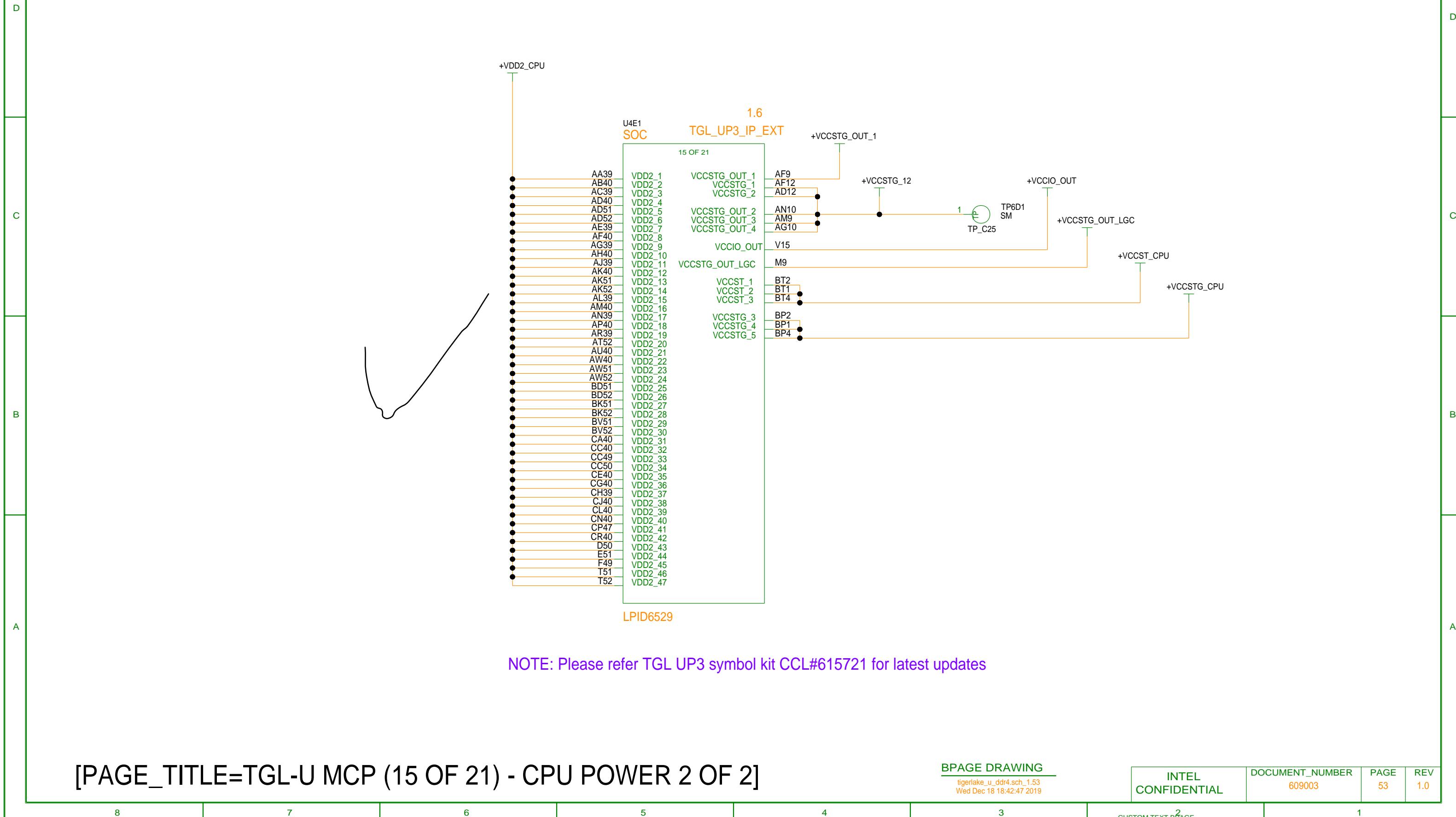
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

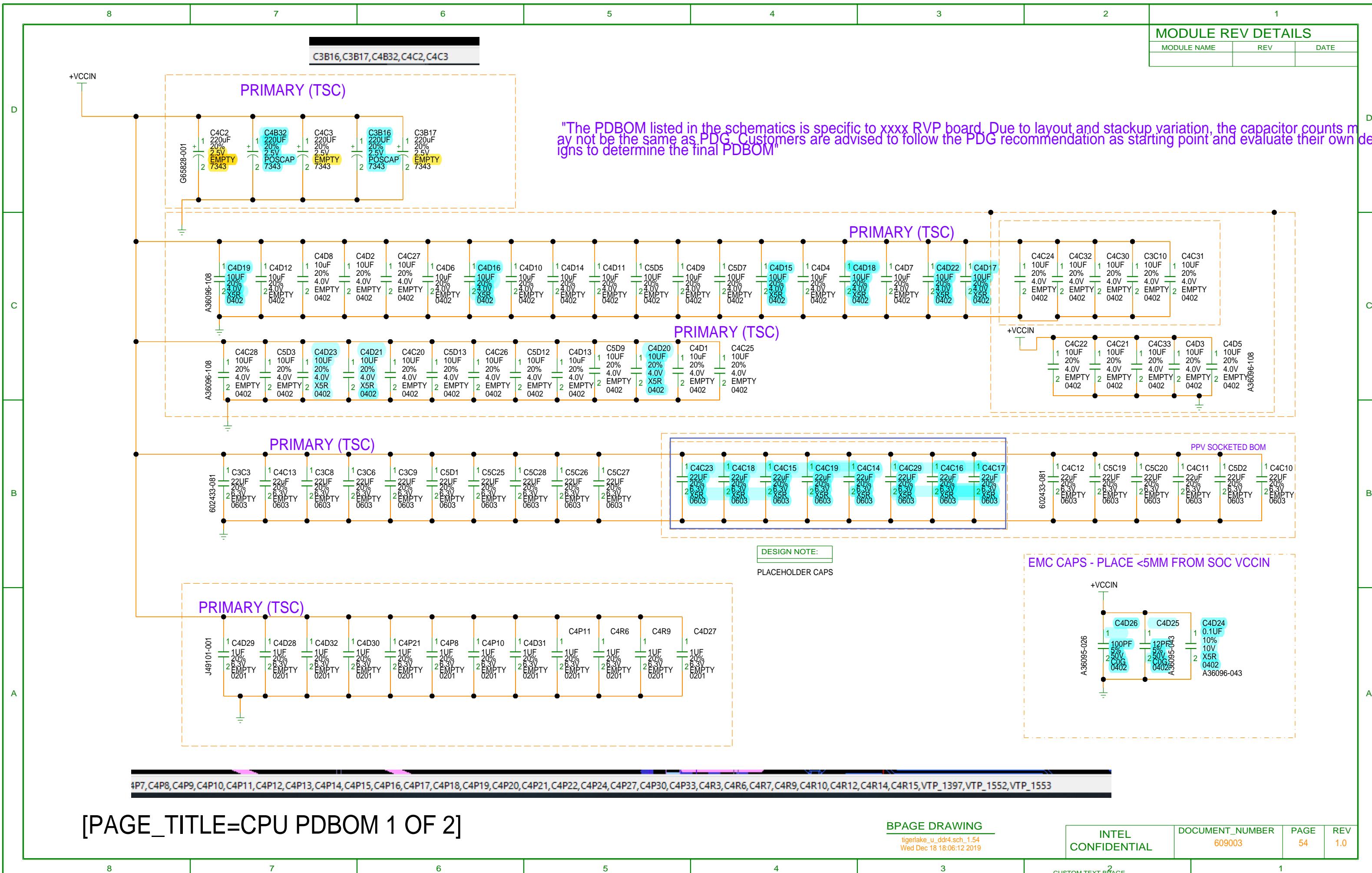
[PAGE\_TITLE=TGL U MCP (13 OF 21) - CPU POWER 1 OF 2]

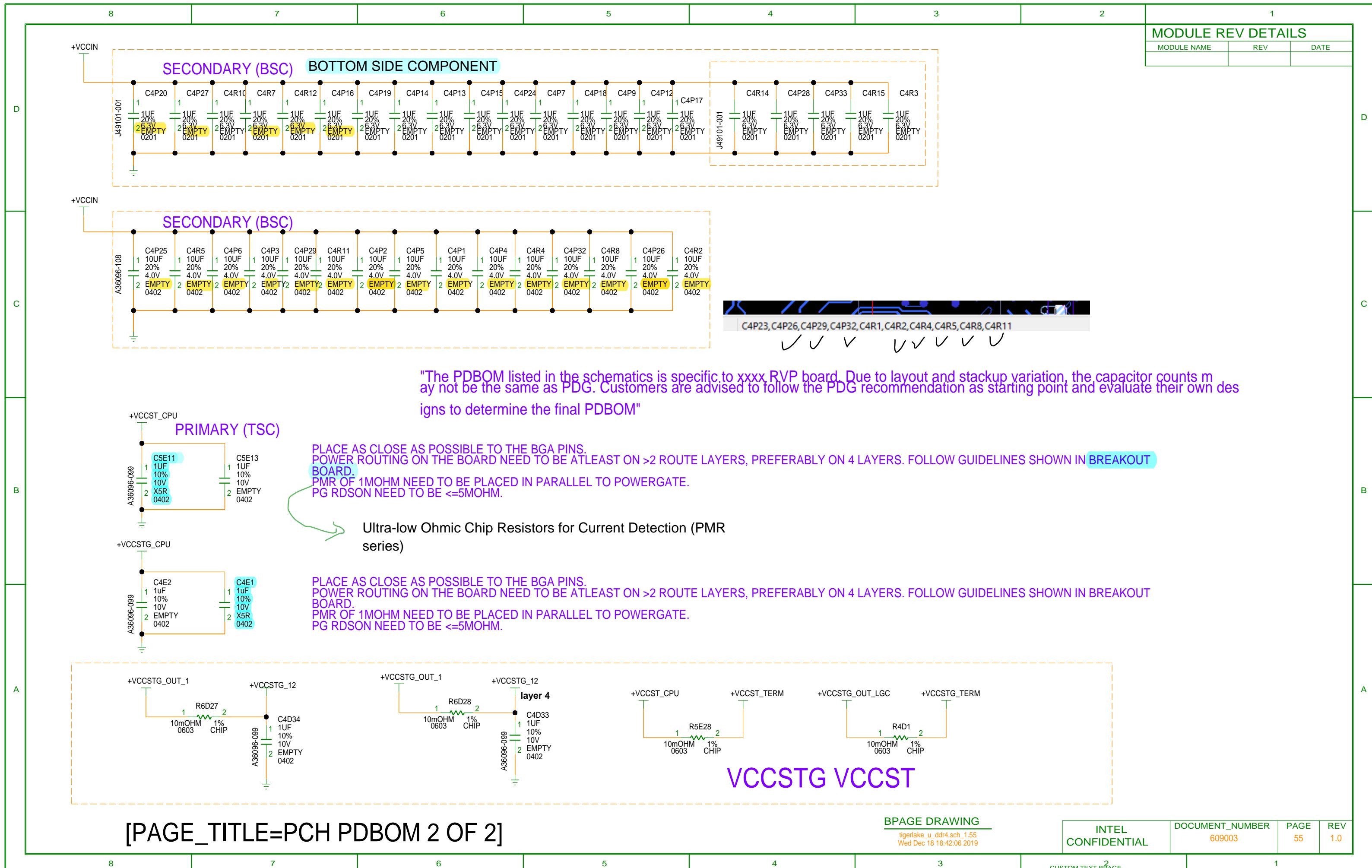
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Wed Dec 18 18:06:09 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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8	7	6	5	4	3	2	1
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MODULE NAME		REV	DATE				



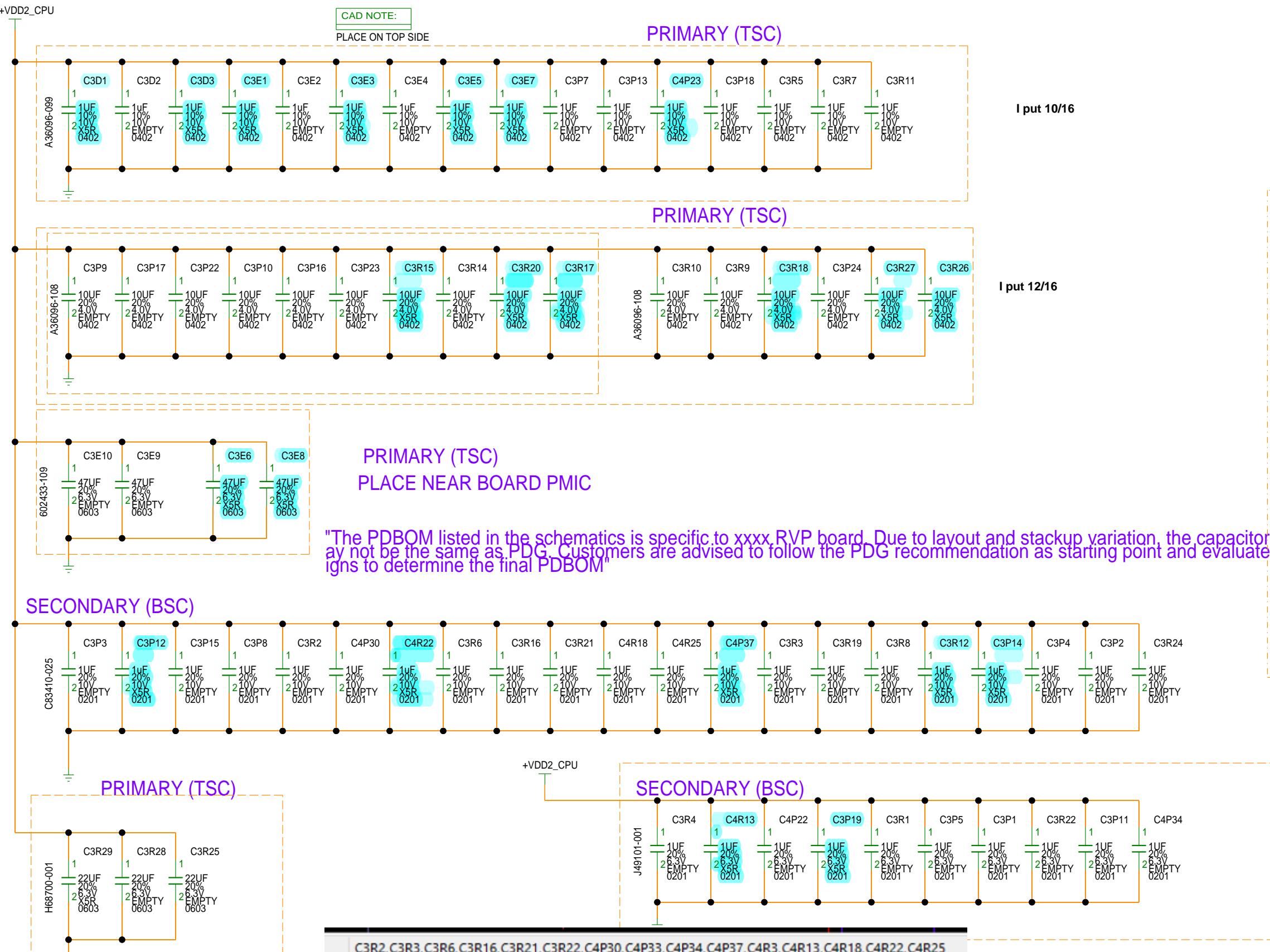




VDD2

MODULE REV DETAILS		
MODULE NAME	REV	DATE

EMC CAPS - PLACE &lt;4MM FROM SOC VDDQ, WITH EACH PAIR &lt;12MM APART



[PAGE\_TITLE=CPU PDBOM 2 OF 2]

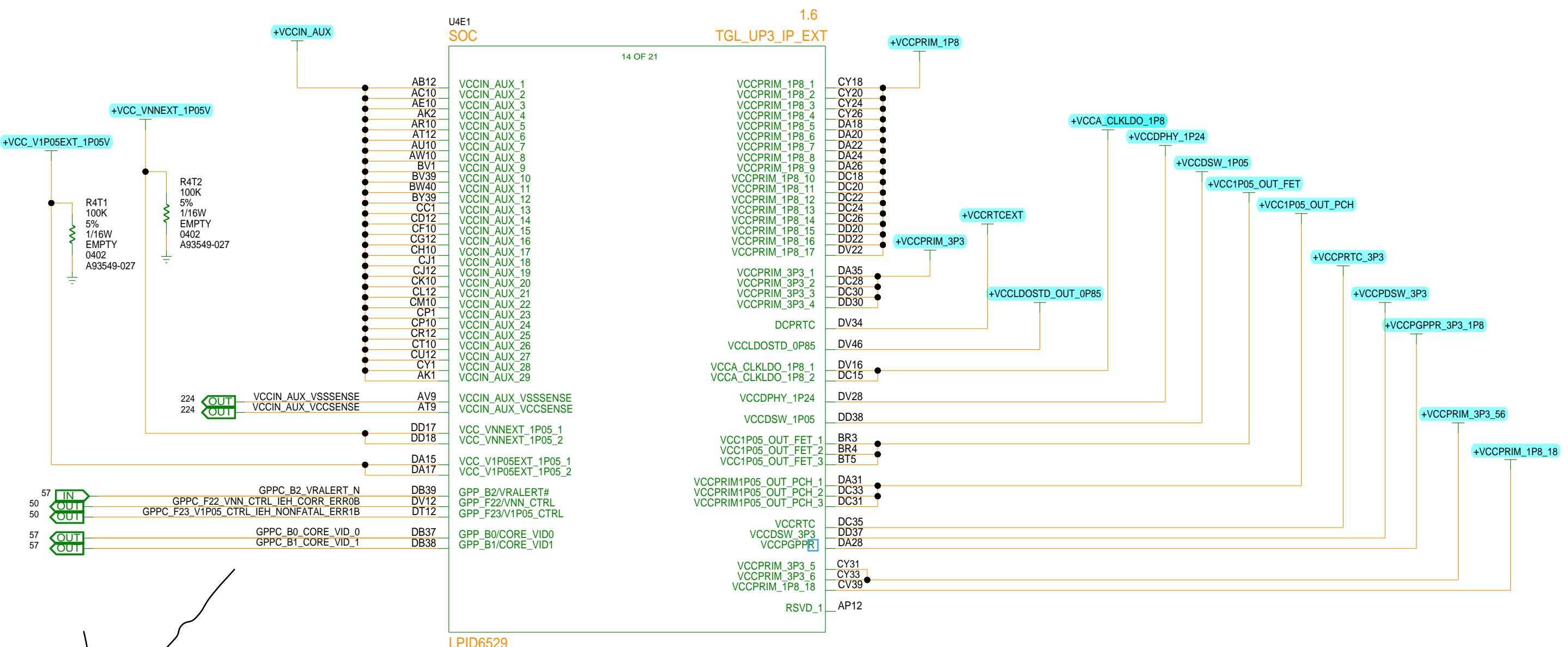
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	56	1.0

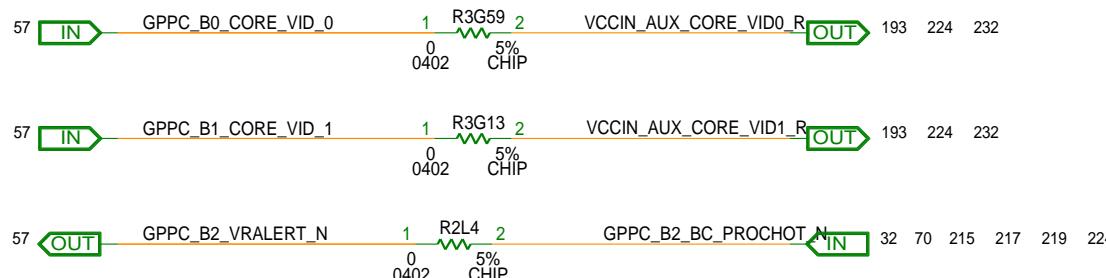
CUSTOM TEXT BPAGE

8 7 6 5 4 3 2 1

8	7	6	5	4	3	2	1
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NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

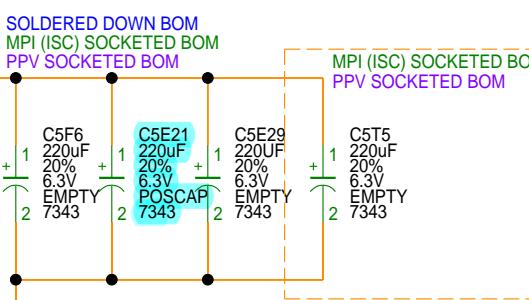


# VCCIN\_AUX\_1P8

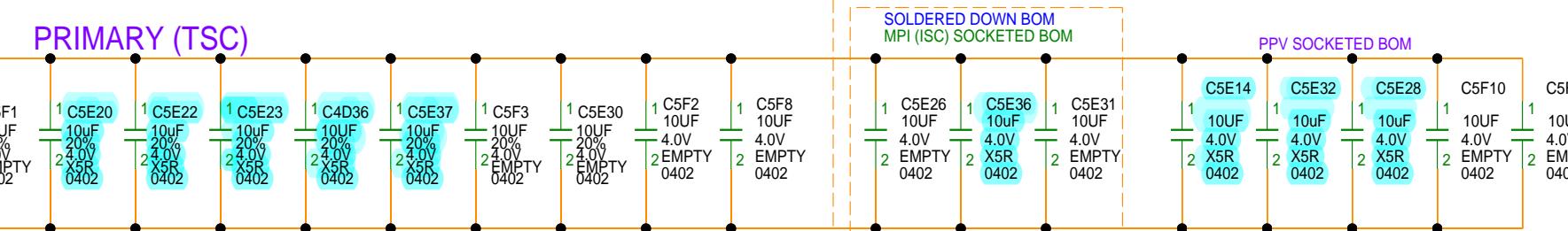
## MODULE REV DETAILS

MODULE NAME	REV	DATE

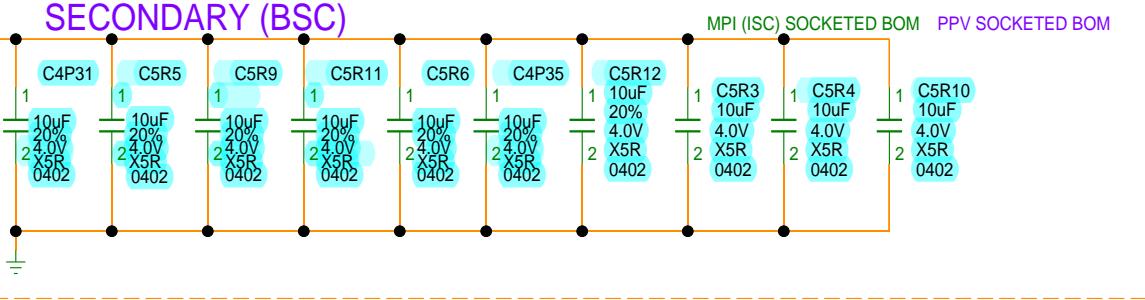
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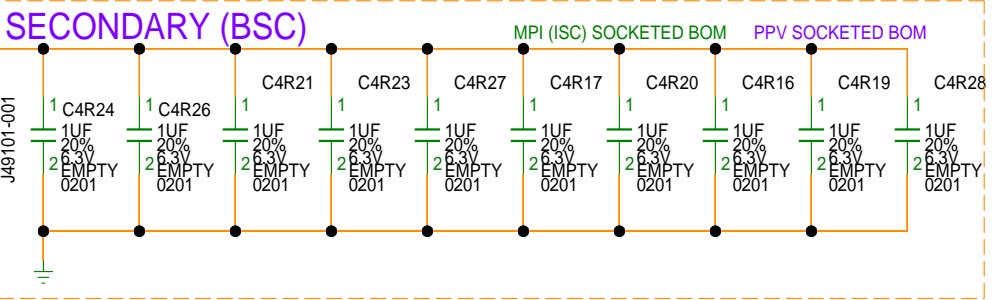
### PRIMARY (TSC)



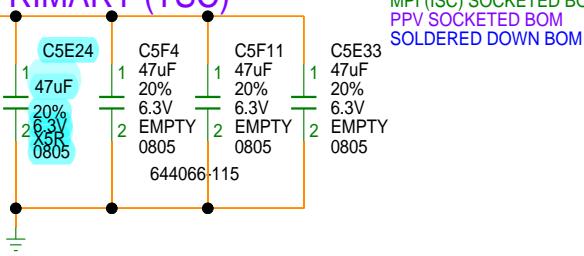
### SECONDARY (BSC)



### SECONDARY (BSC)

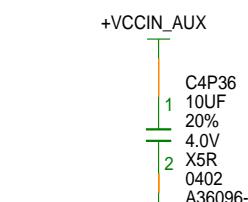


### PRIMARY (TSC)

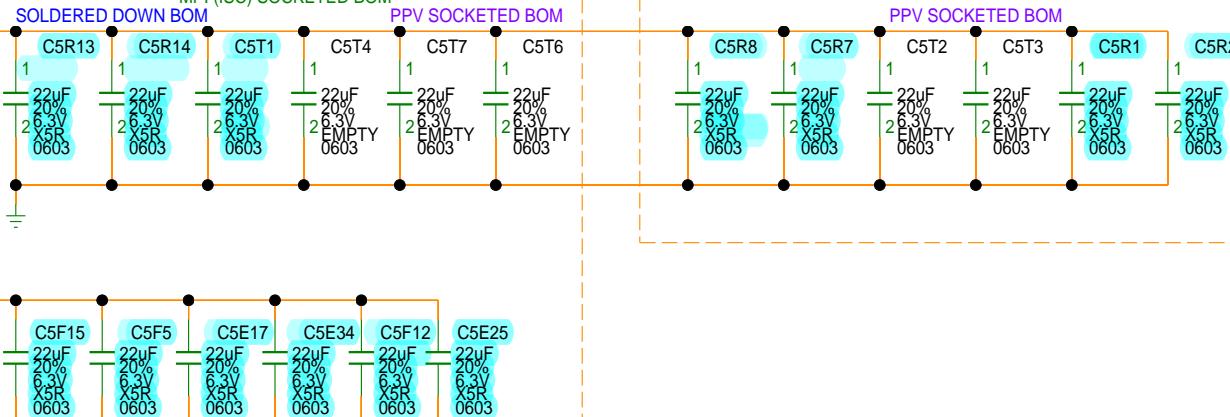


+VCCIN\_AUX

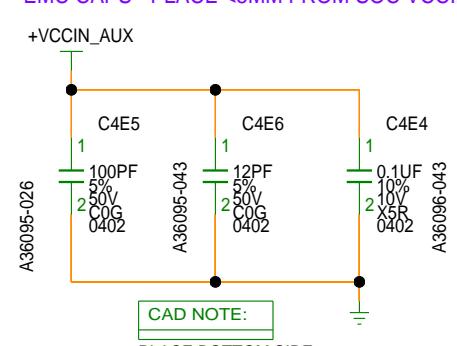
CAP ADDED FOR PI SIMULATION AS PER PI FEEDBACK  
PLACE CLOSE TO PIN AK1 of SoC



### SOLDERED DOWN BOM



### EMC CAPS - PLACE <5MM FROM SOC VCCIN\_AUX



[PAGE\_TITLE=PDBOM- VCCIN\_AUX]

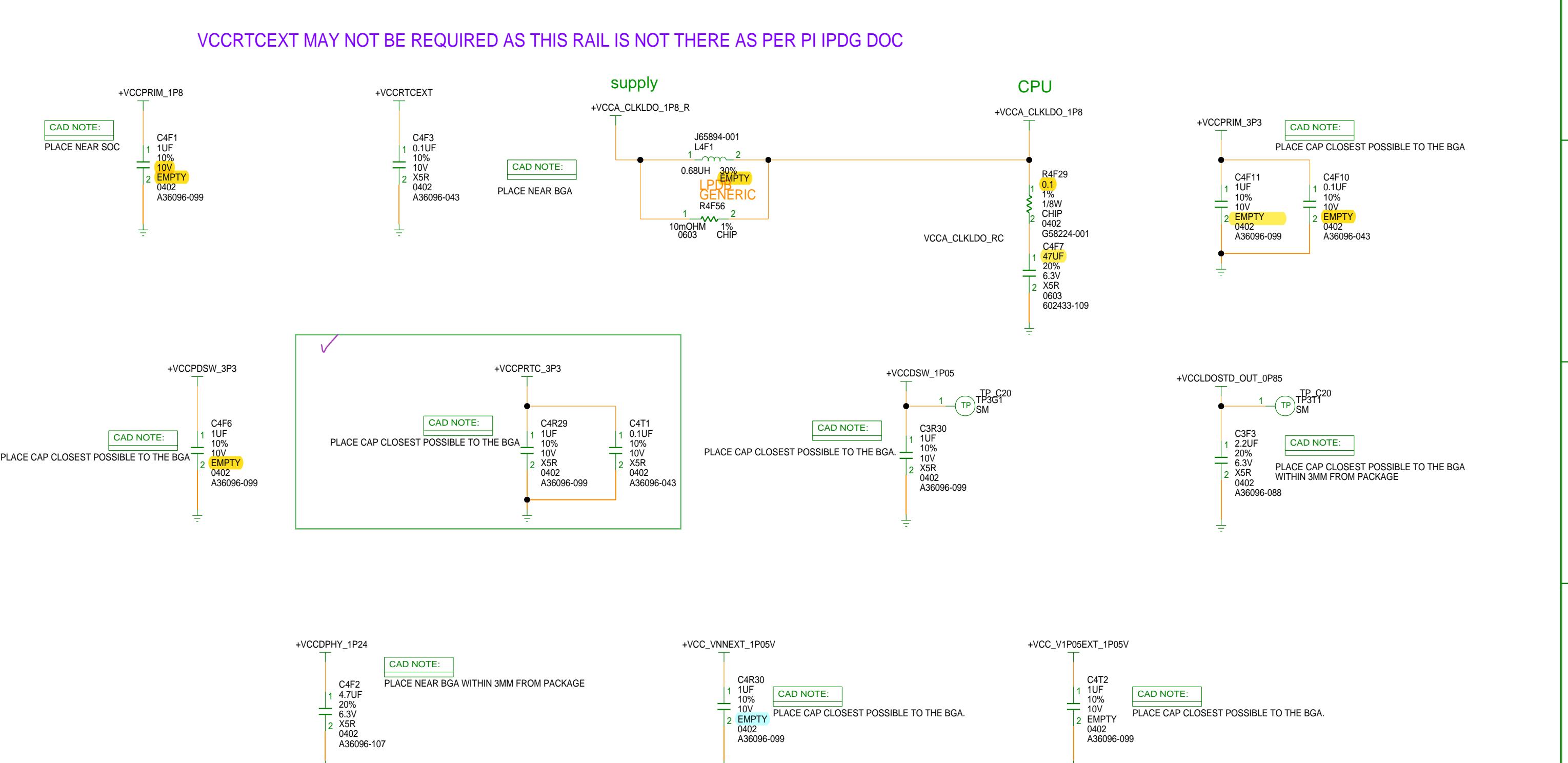
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Wed Dec 18 18:42:42 2019

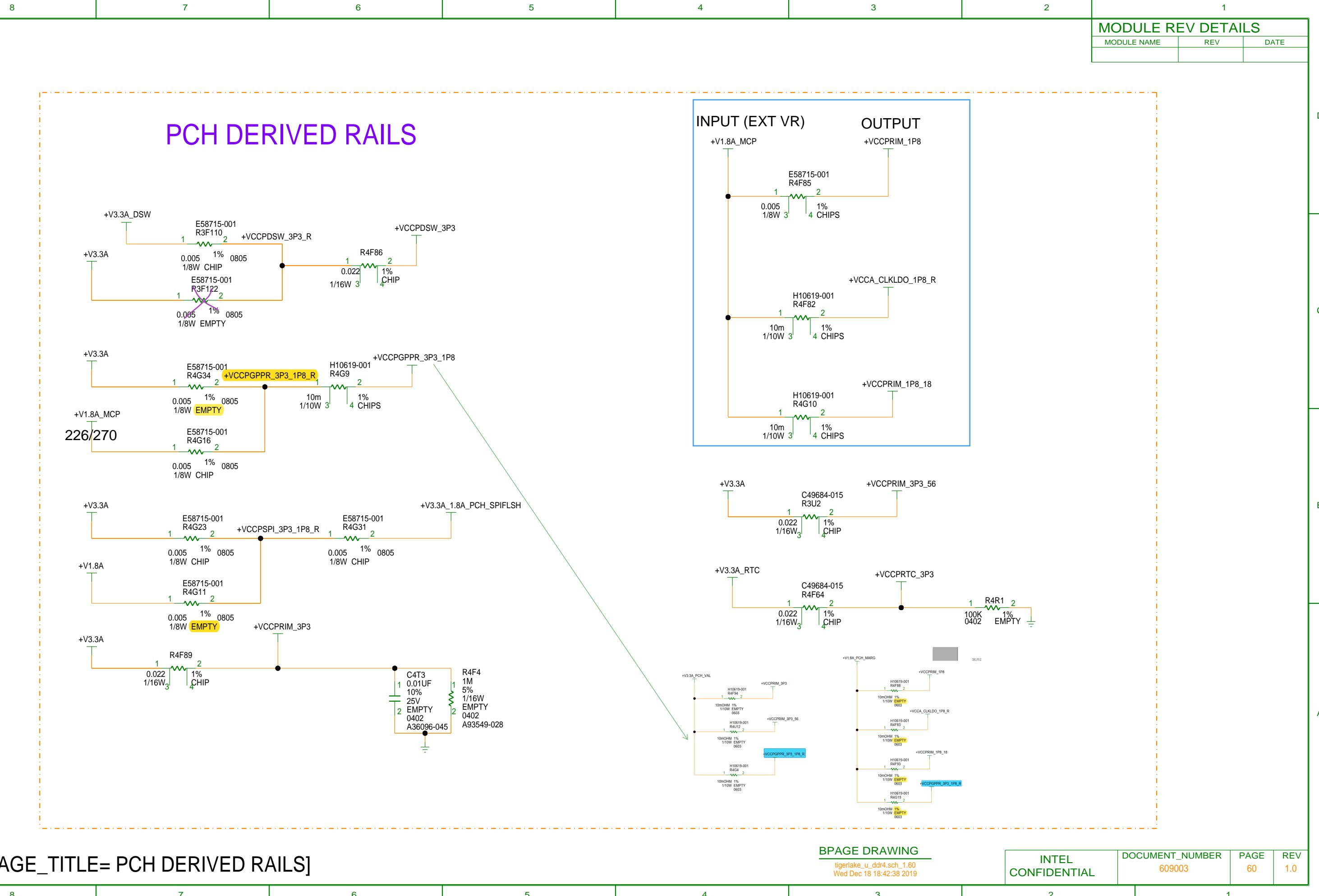
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	58	1.0	

CUSTOM TEXT BPAGE

8	7	6	5	4	3	2	1
<b>MODULE REV DETAILS</b>							
MODULE NAME		REV	DATE				

VCCRTCEXT MAY NOT BE REQUIRED AS THIS RAIL IS NOT THERE AS PER PI IPDG DOC





8	7	6	5	4	3	2	1
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# PCH MARGINING RAILS

## MODULE REV DETAILS

MODULE NAME	REV	DATE

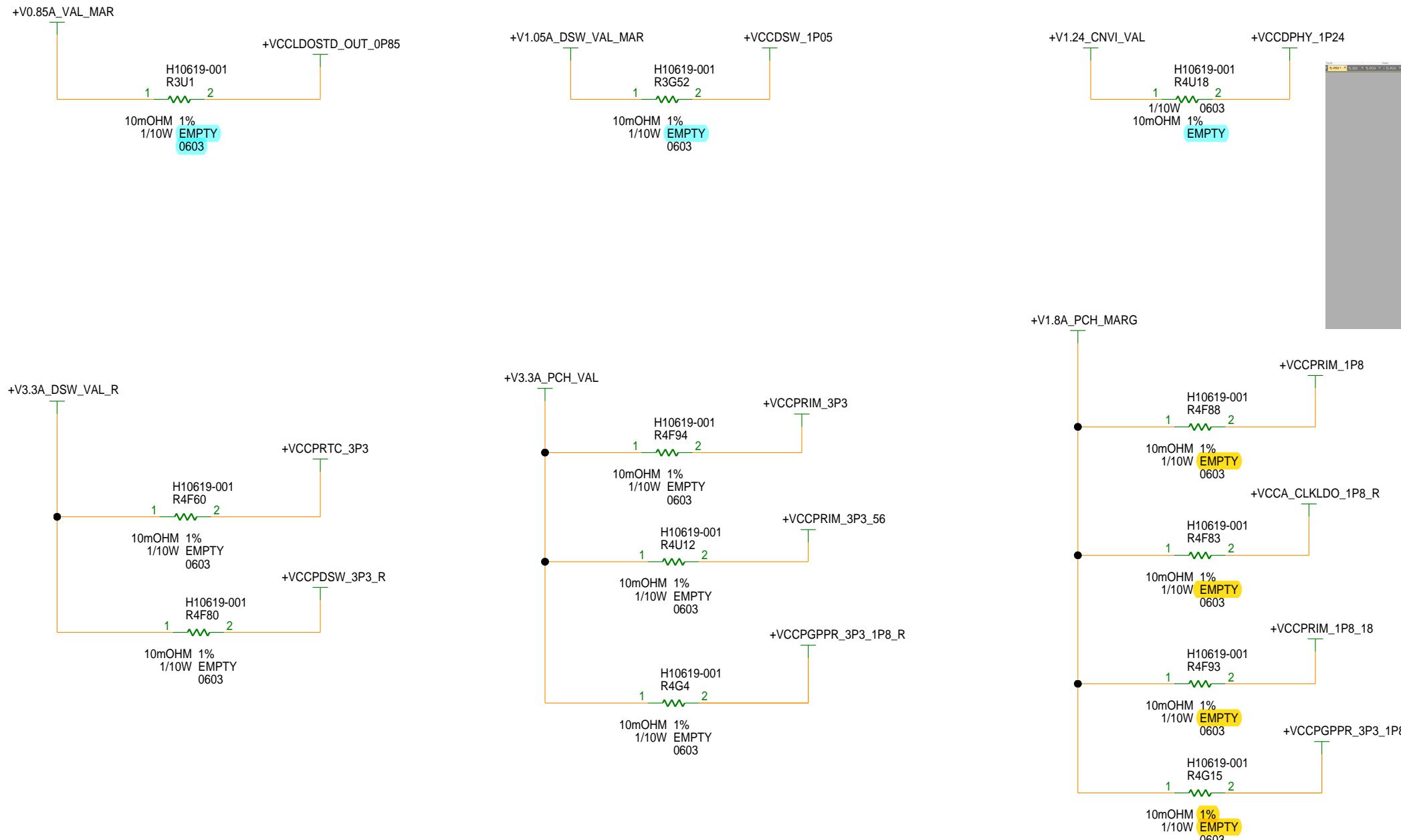


Table 237. No Direct Switching or No External Bypass Supported						
State Enable	Q1 CNVI	Q2 ISH	Q3 Type A	Q4 C-Link	Q5 SMBus	Q6 PHY PG
S02.0	Always Enable	-	-	-	-	-
S02.1	Always Enable	-	-	-	-	-
S02.2	-	-	NO	-	-	YES
S03.0	NO	NO	-	-	-	-
S03.1	NO	NO	-	-	-	-
S03.2	NO	NO	-	-	-	-
S03.3	NO	NO	NO	-	-	YES

**Voltage Margining**  
Voltage margining allows bypass VRs to reduce their voltages depending on S03.x states. To enable this feature, VNN\_CTRL and V1P05\_CTRL GPIO pins should be configured. This feature can reduce power in Soix states.

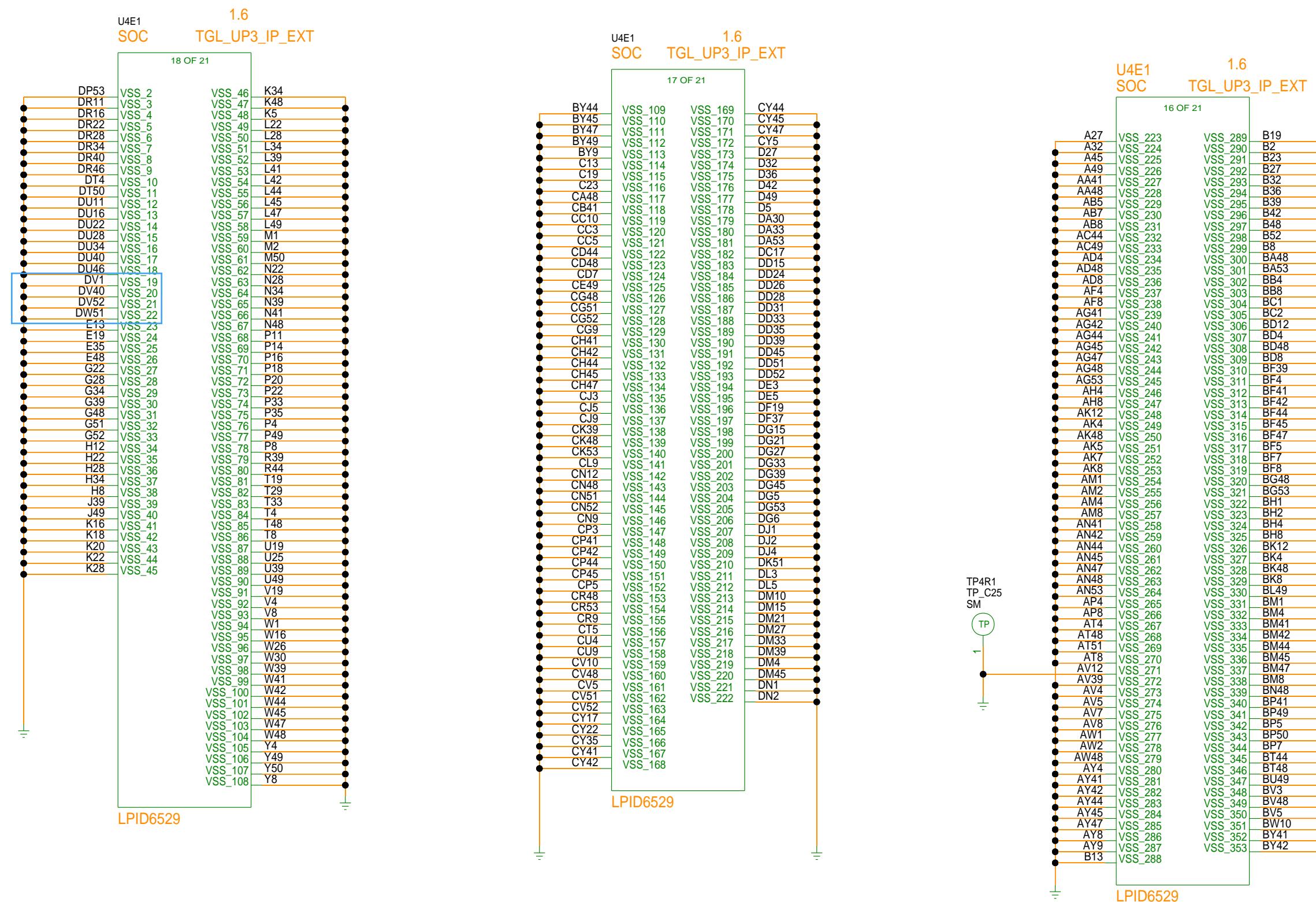
Tiger Lake UP3 UP4 H35 UP3 Refresh Platform

November 2020

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**MODULE REV DETAILS**

MODULE NAME	REV	DATE



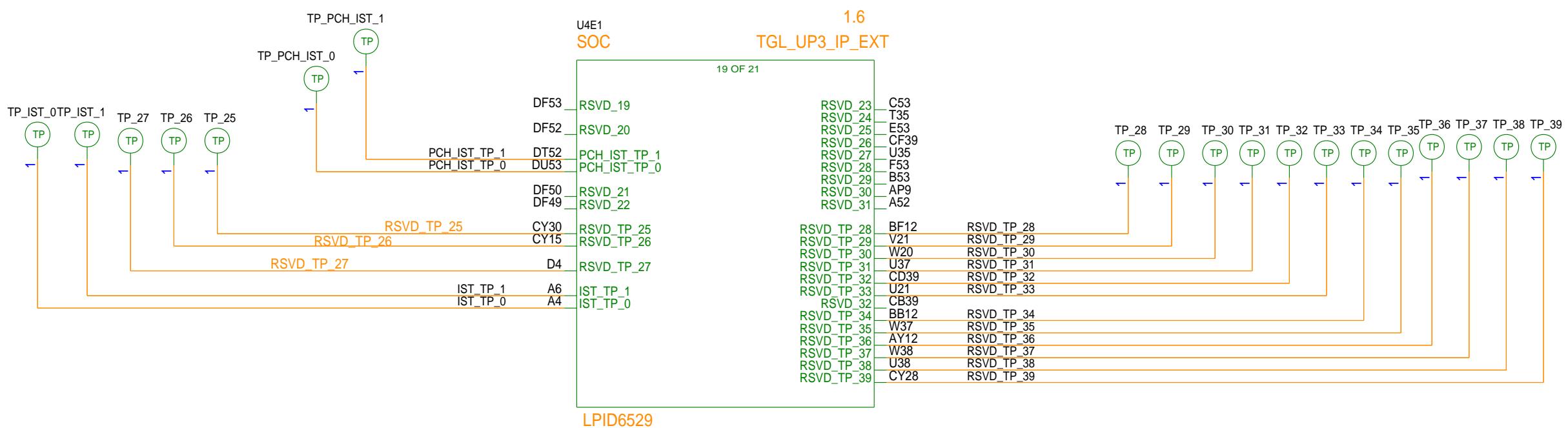
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

[PAGE\_TITLE=TGL-U MCP (16,17,18 OF 21) - GND (1 OF 3)]

BPAGE DRAWING  
tigerlake\_u\_ddr4.sch\_1.62  
Wed Dec 18 18:06:20 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
609003	62	1.0	

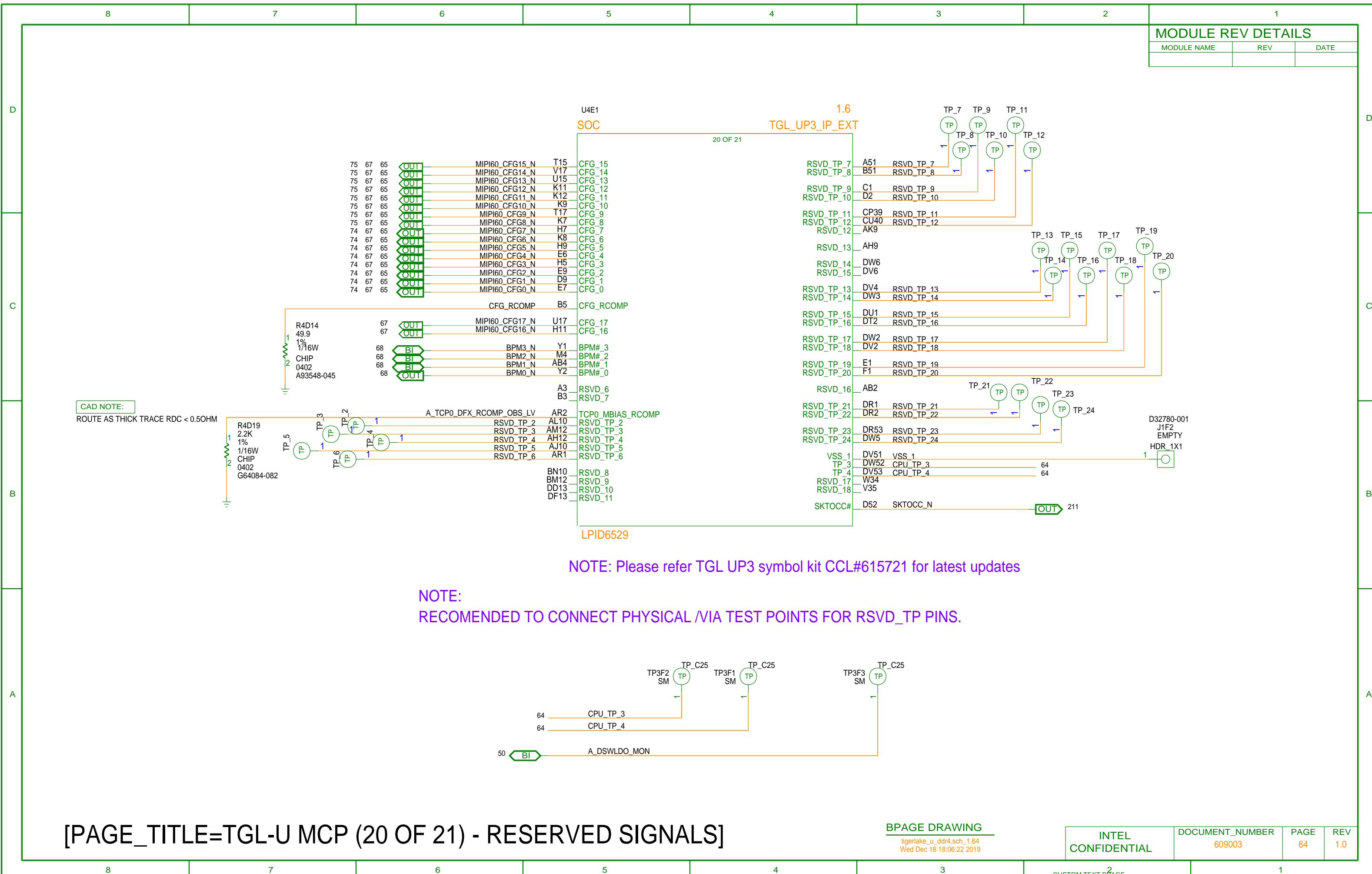
8	7	6	5	4	3	2	1	
<b>MODULE REV DETAILS</b>						MODULE NAME	REV	DATE



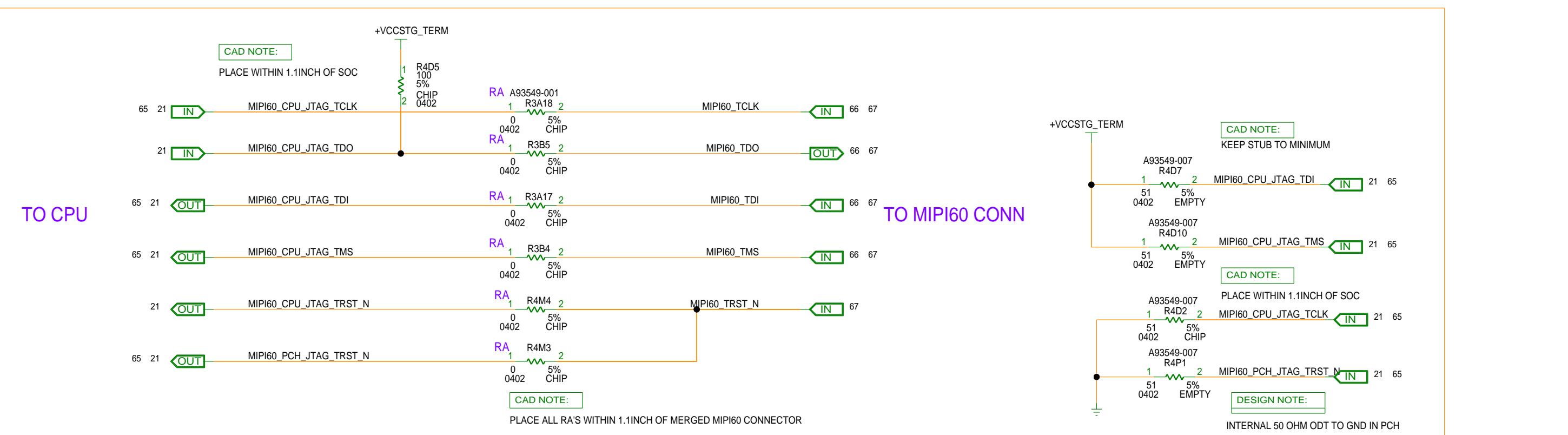
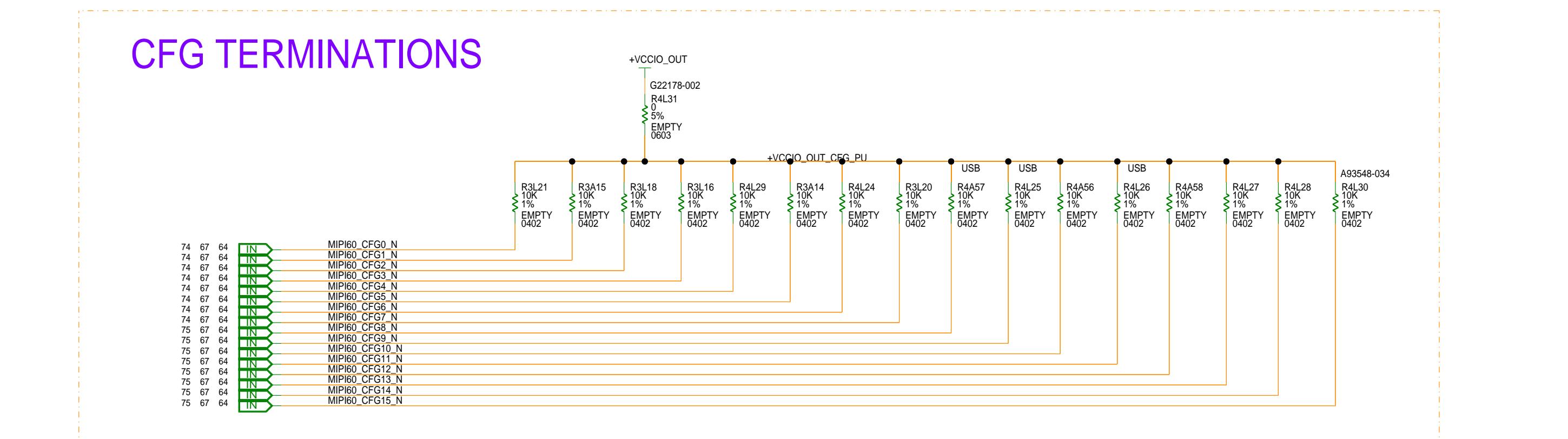
NOTE: Please refer TGL UP3 symbol kit CCL#615721 for latest updates

NOTE:

RECOMENDED TO CONNECT PHYSICAL /VIA TEST POINTS FOR RSVD\_TP PINS.



8	7	6	5	4	3	2	1
<b>MODULE REV DETAILS</b>							

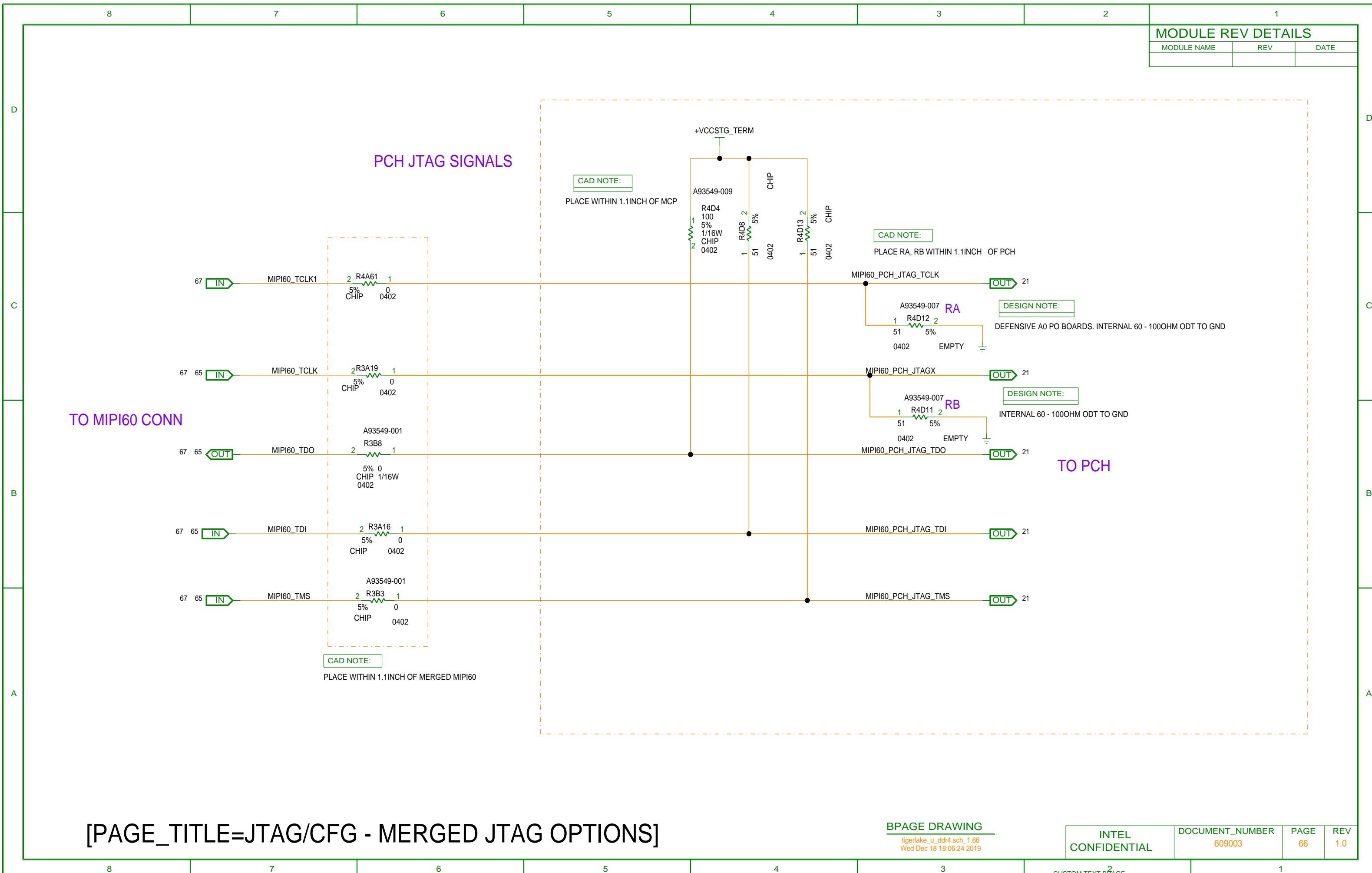


[PAGE\_TITLE=JTAG/CFG - CFG TERMINATIONS]

BPAGE DRAWING

tigerlake\_u\_ddr4.sch\_1.65  
Wed Dec 18 18:06:23 2019

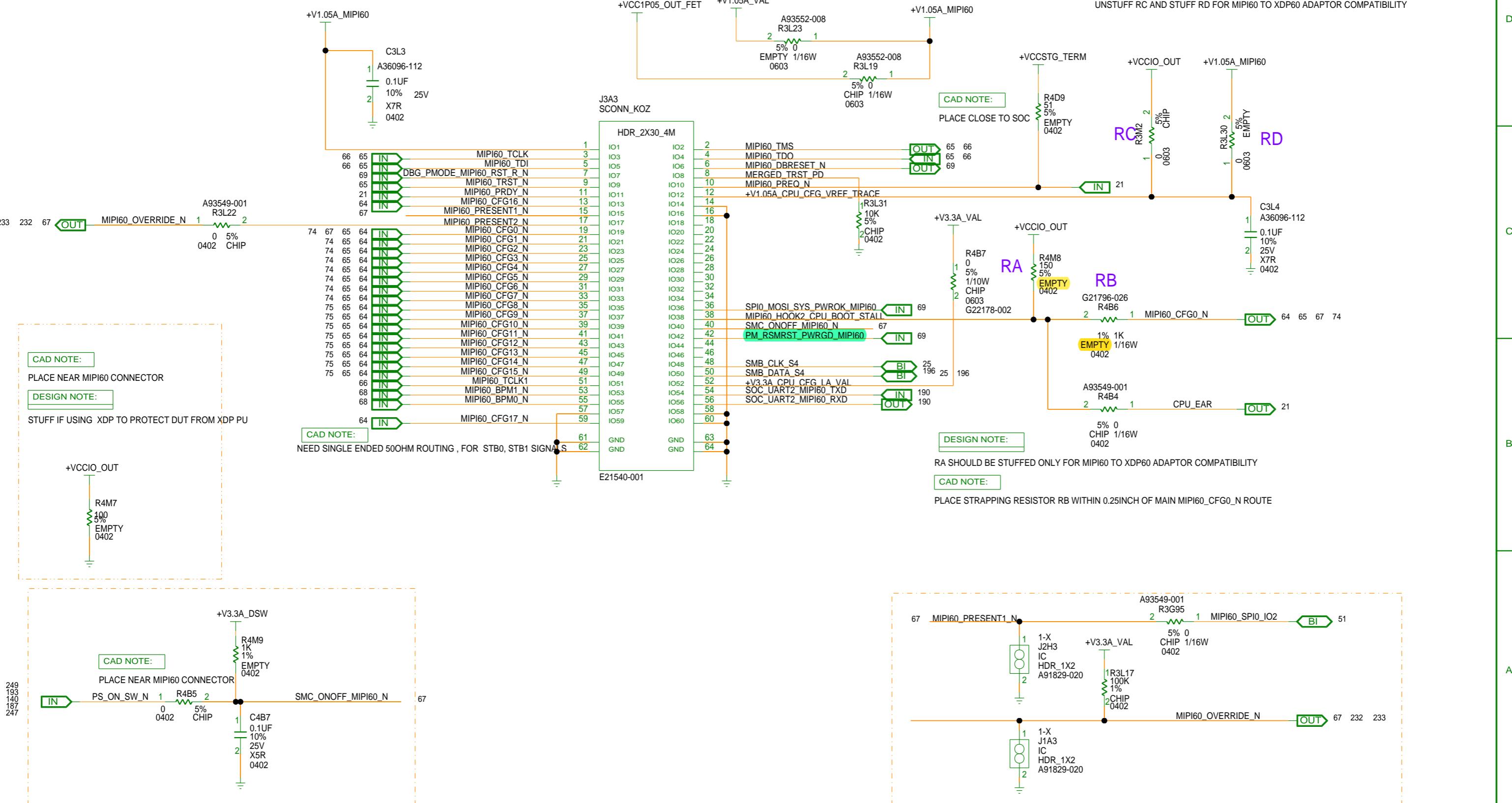
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	65	1.0

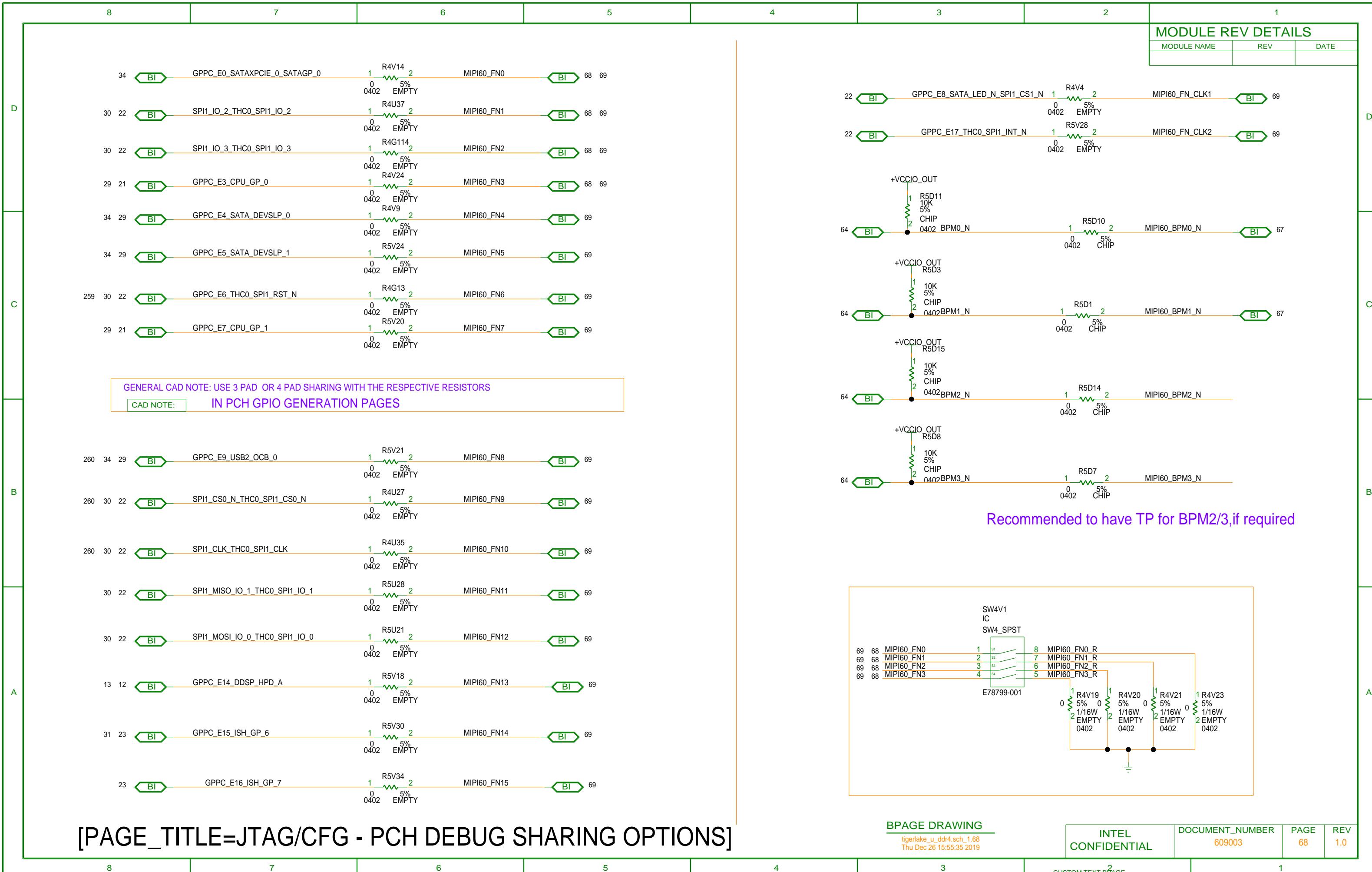


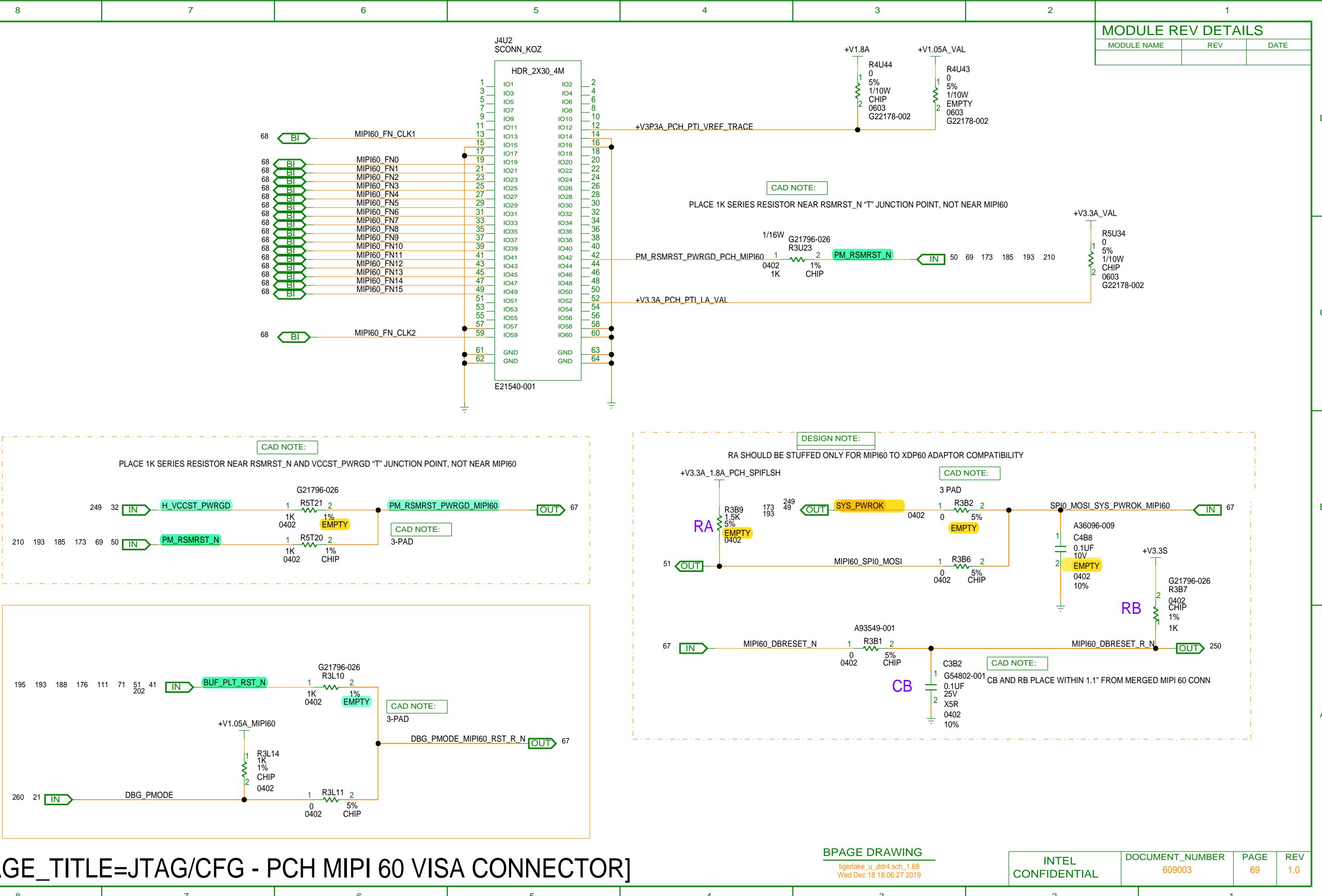
# MIPI 60

## MODULE REV DETAILS

MODULE NAME	REV	DATE





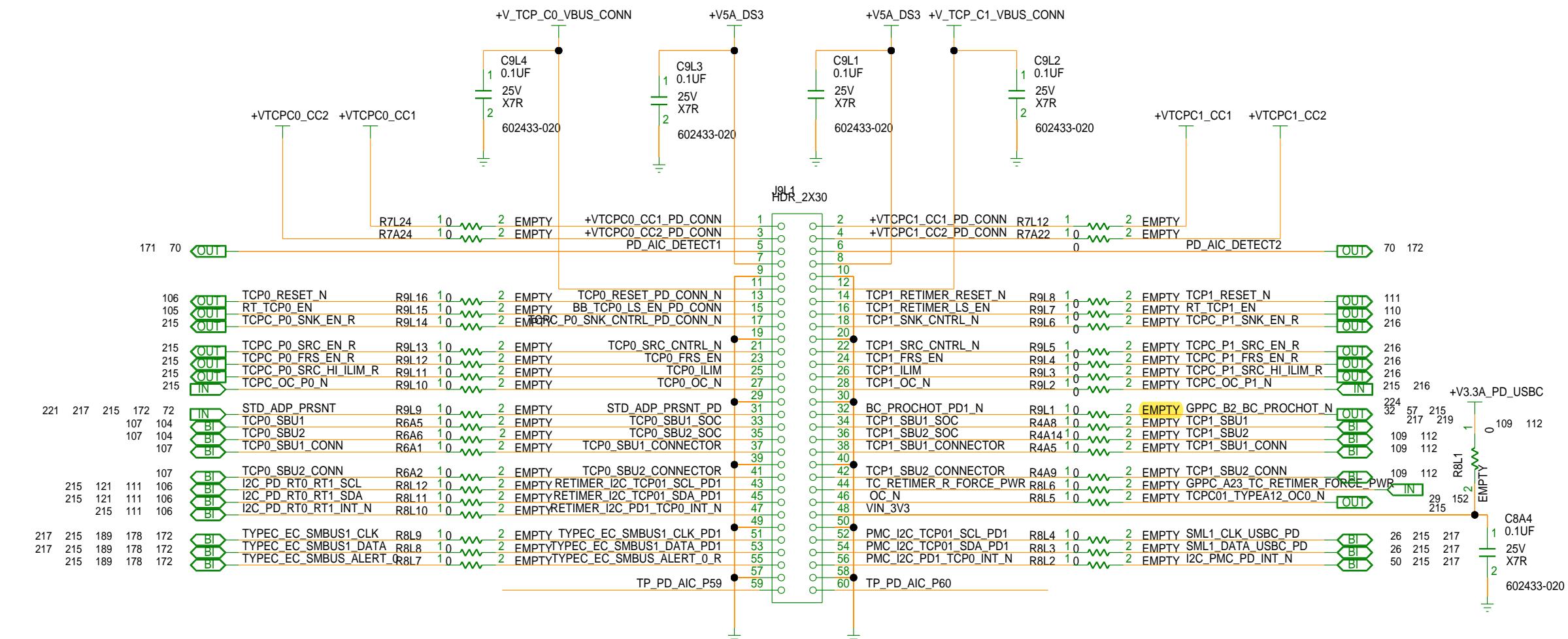


8	7	6	5	4	3	2	1
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# PD AIC CONTROLLER

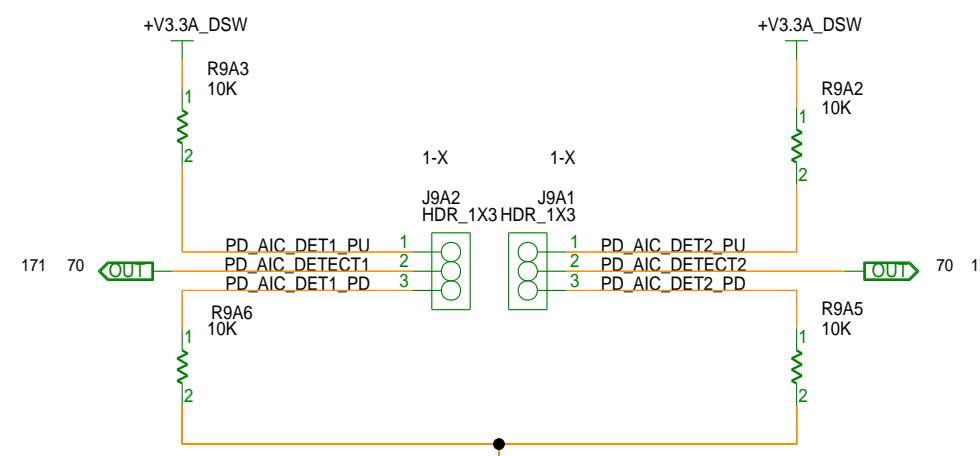
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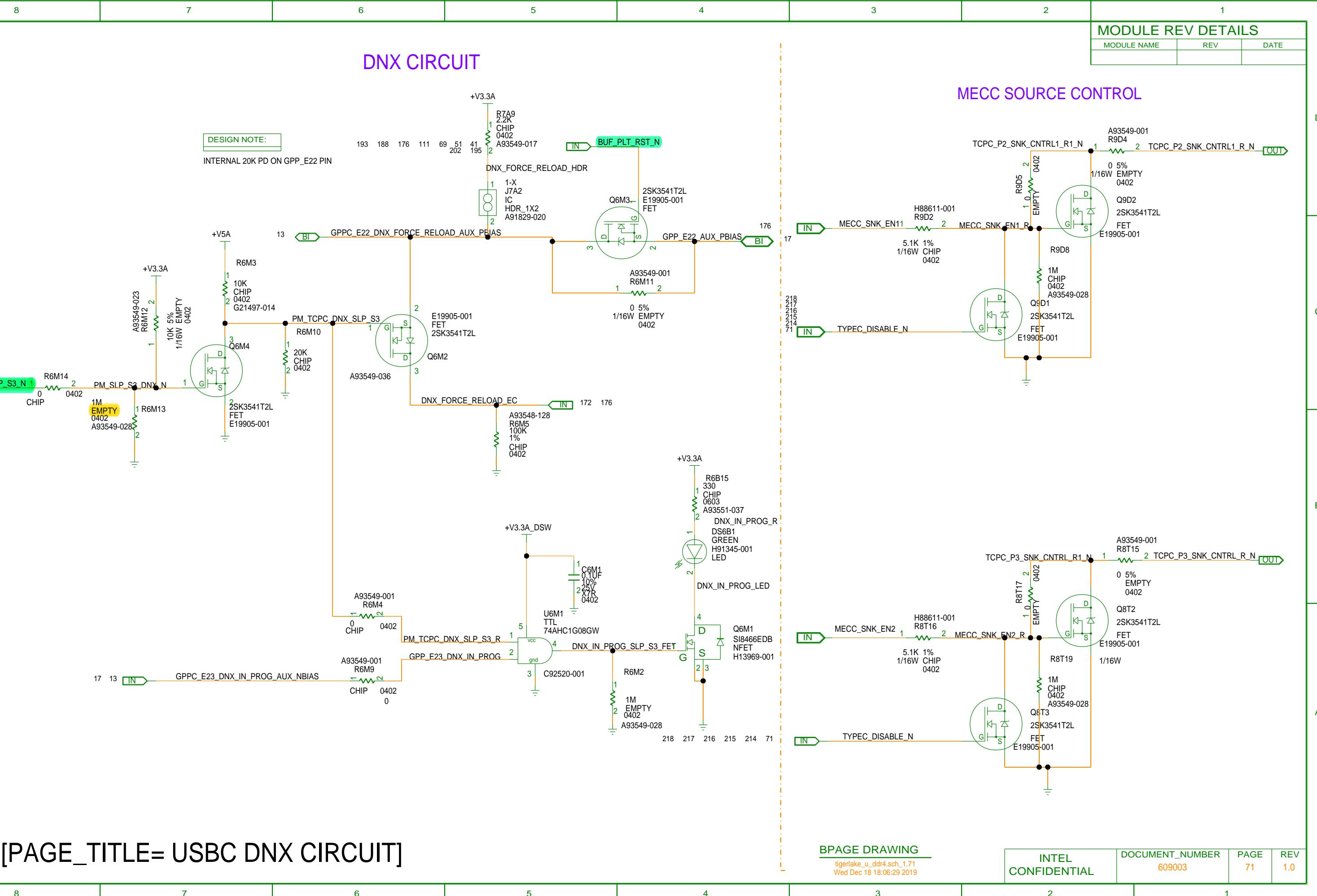
MODULE NAME	REV	DATE

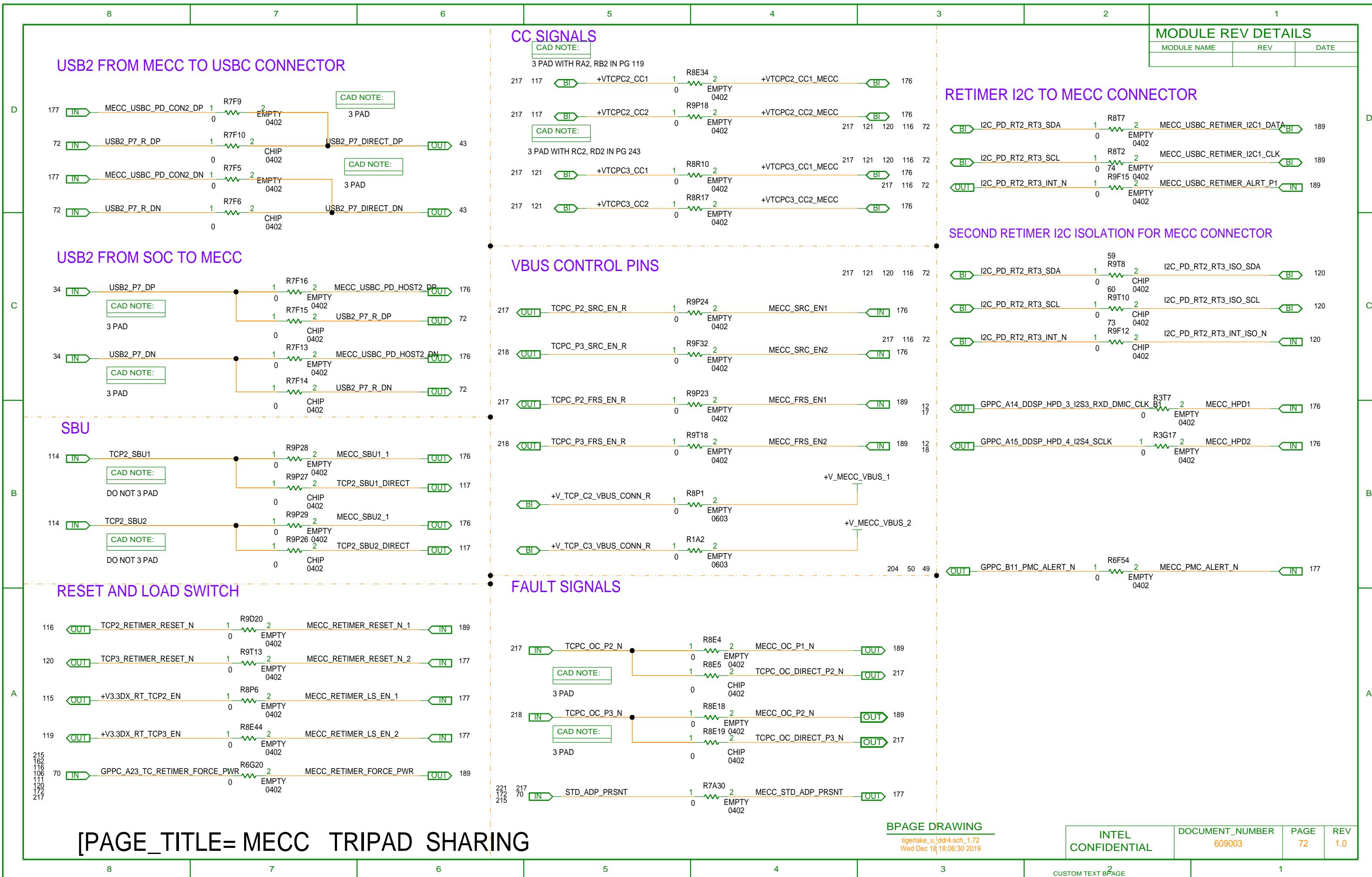


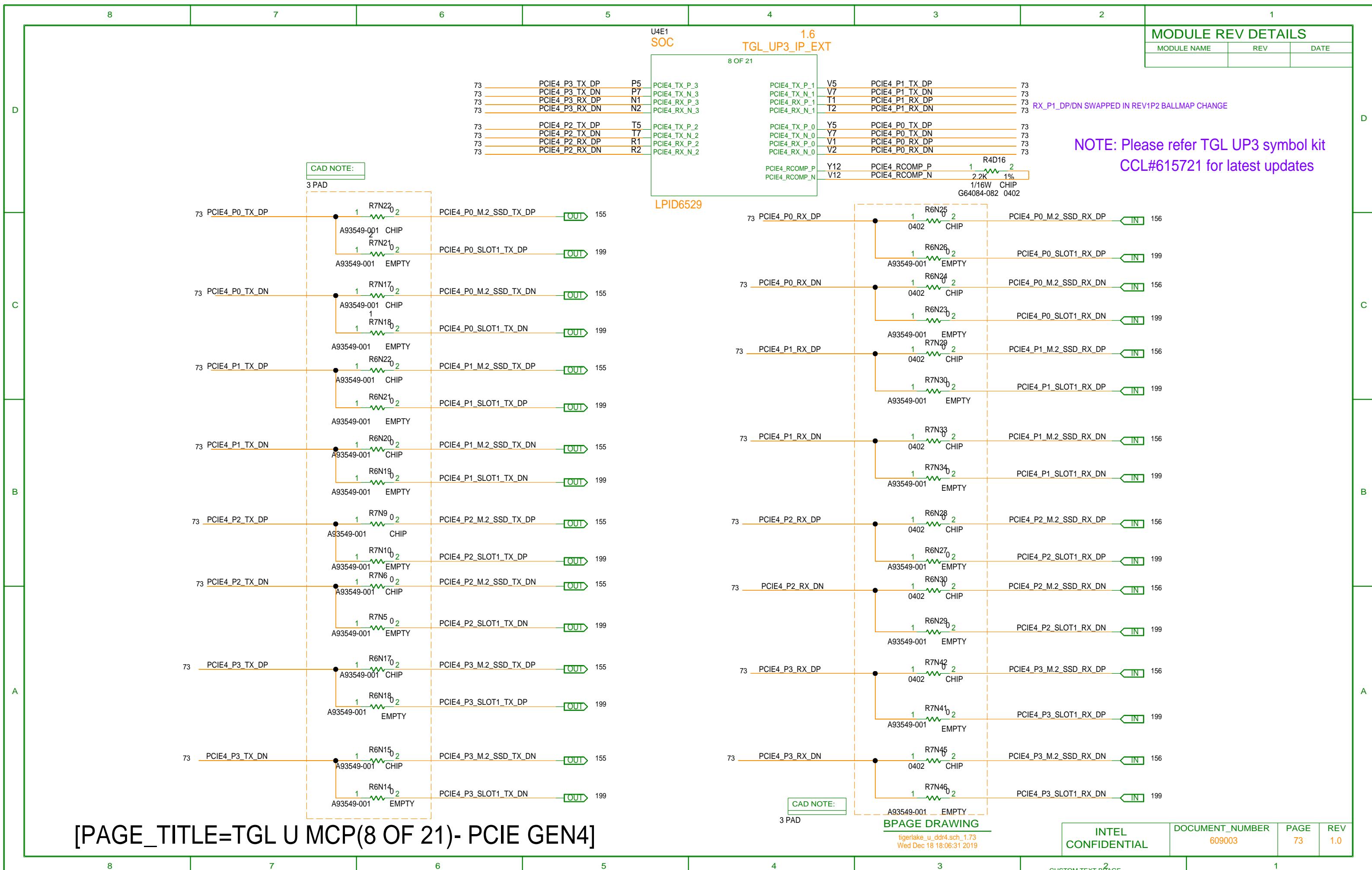
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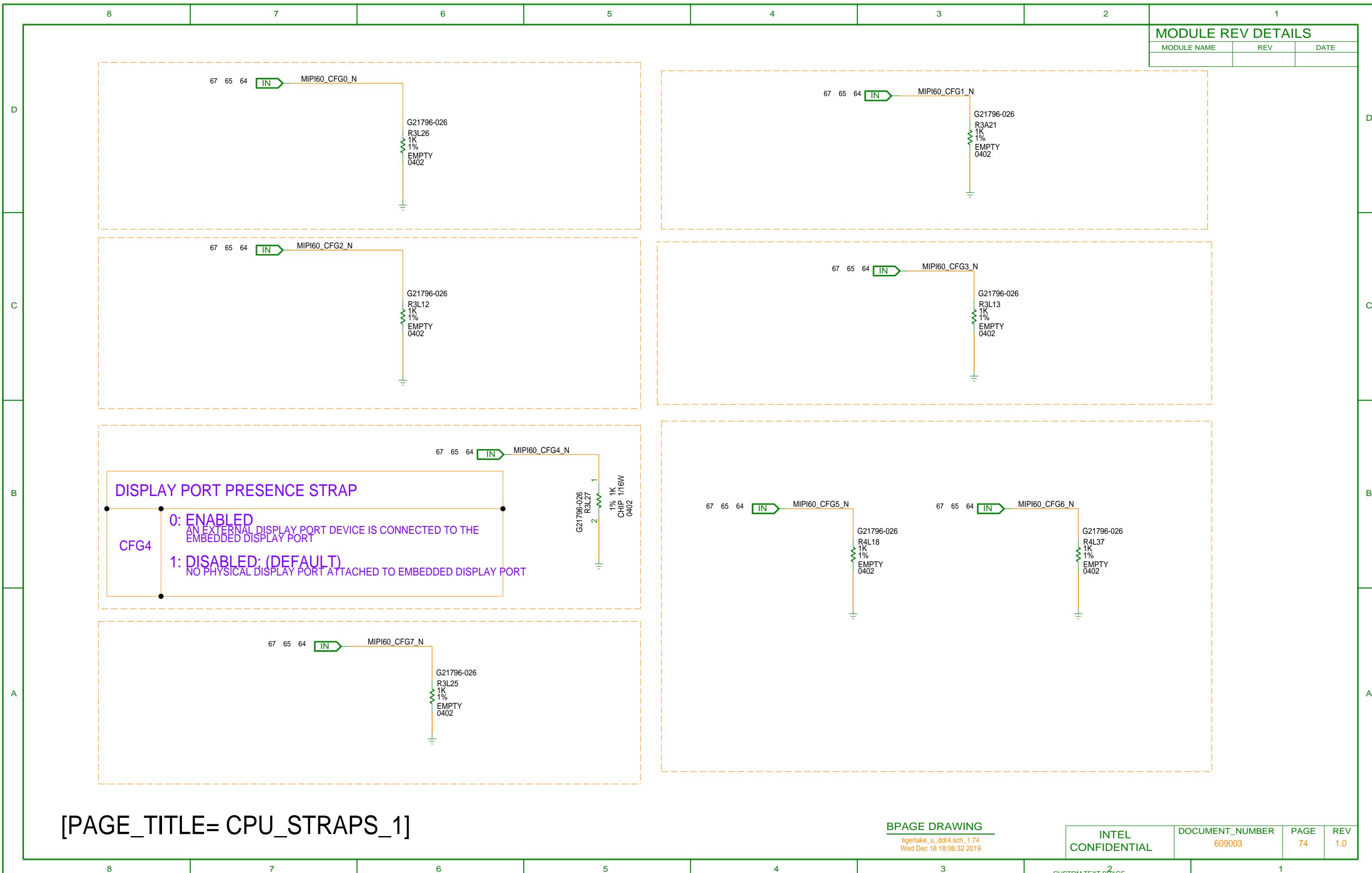
ALL THE RESISTORS IN THIS PAGE SHOULD BE TRIPAD WITH RESPECTIVE RESISTOR IN OTHER SECTION

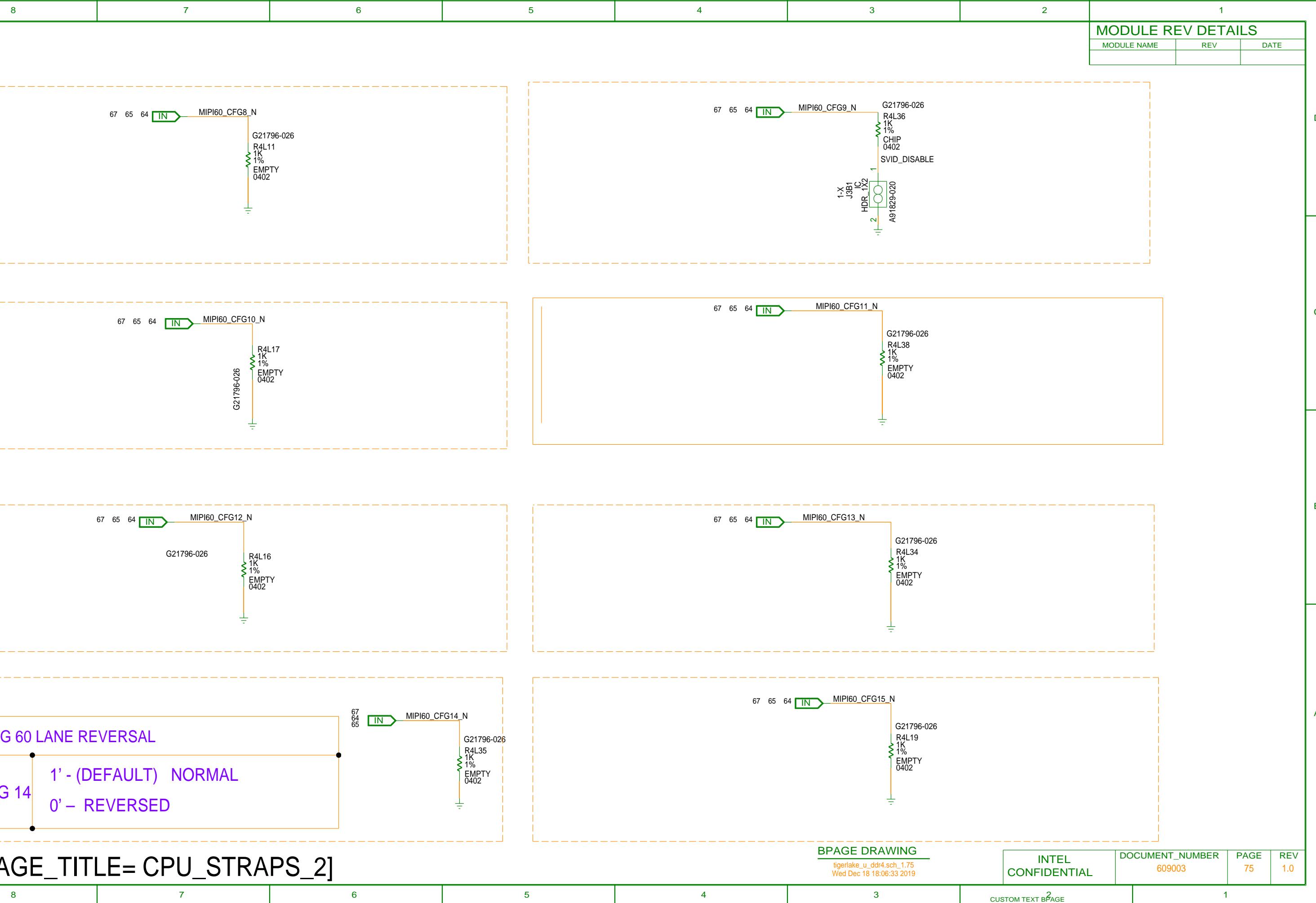






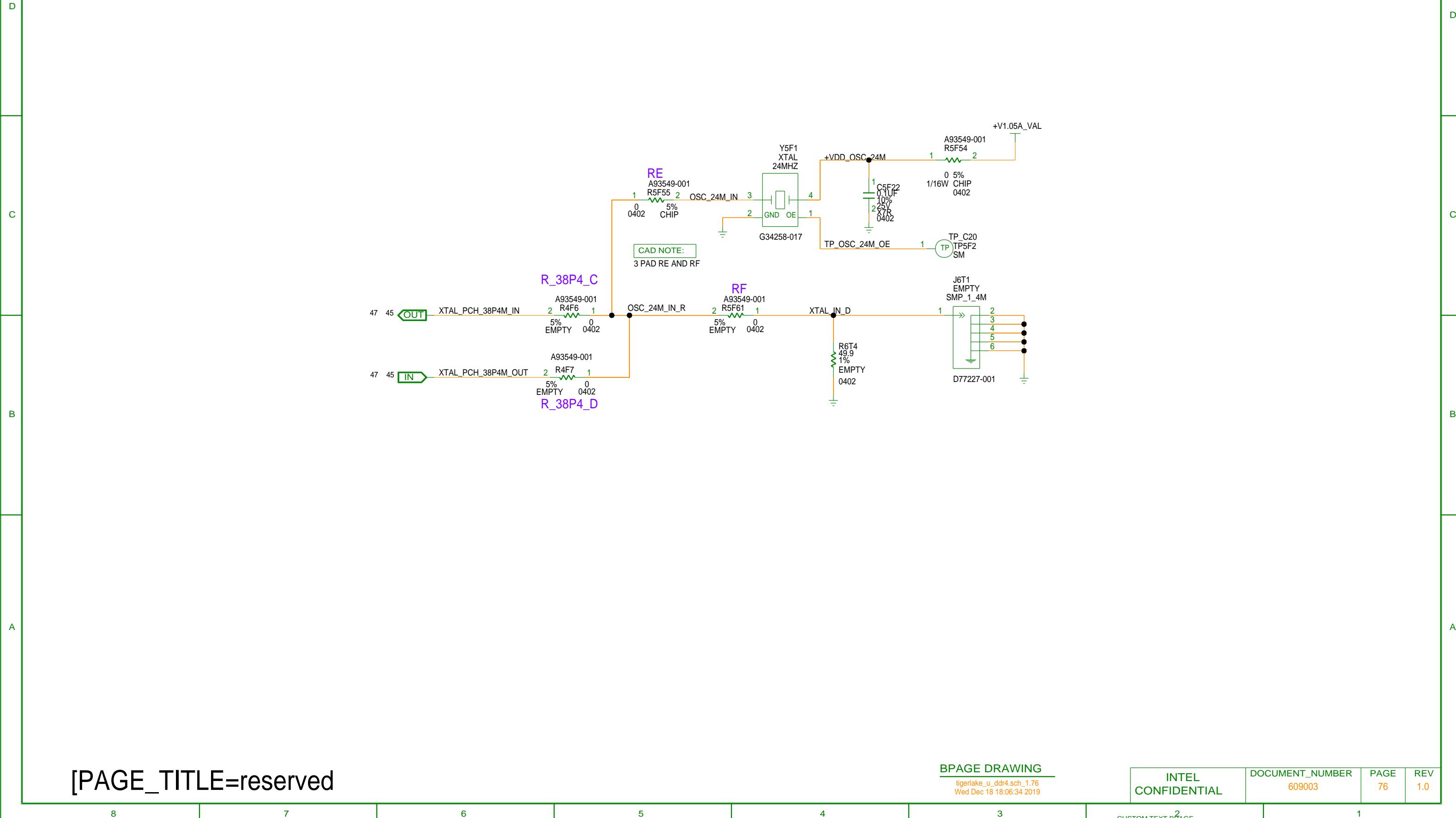






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MODULE REV DETAILS		
MODULE NAME	REV	DATE



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tigerlake\_u\_ddr4.sch\_1.76  
Wed Dec 18 18:06:34 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	76	1.0

8	7	6	5	4	3	2	1
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CUSTOM TEXT BPAGE

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**MODULE REV DETAILS**

MODULE NAME	REV	DATE

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**[PAGE\_TITLE=RESERVE]**BPAGE DRAWING

tigerlake\_u\_ddr4.sch\_1.77  
Tue Oct 15 12:49:33 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	609003	77	1.0

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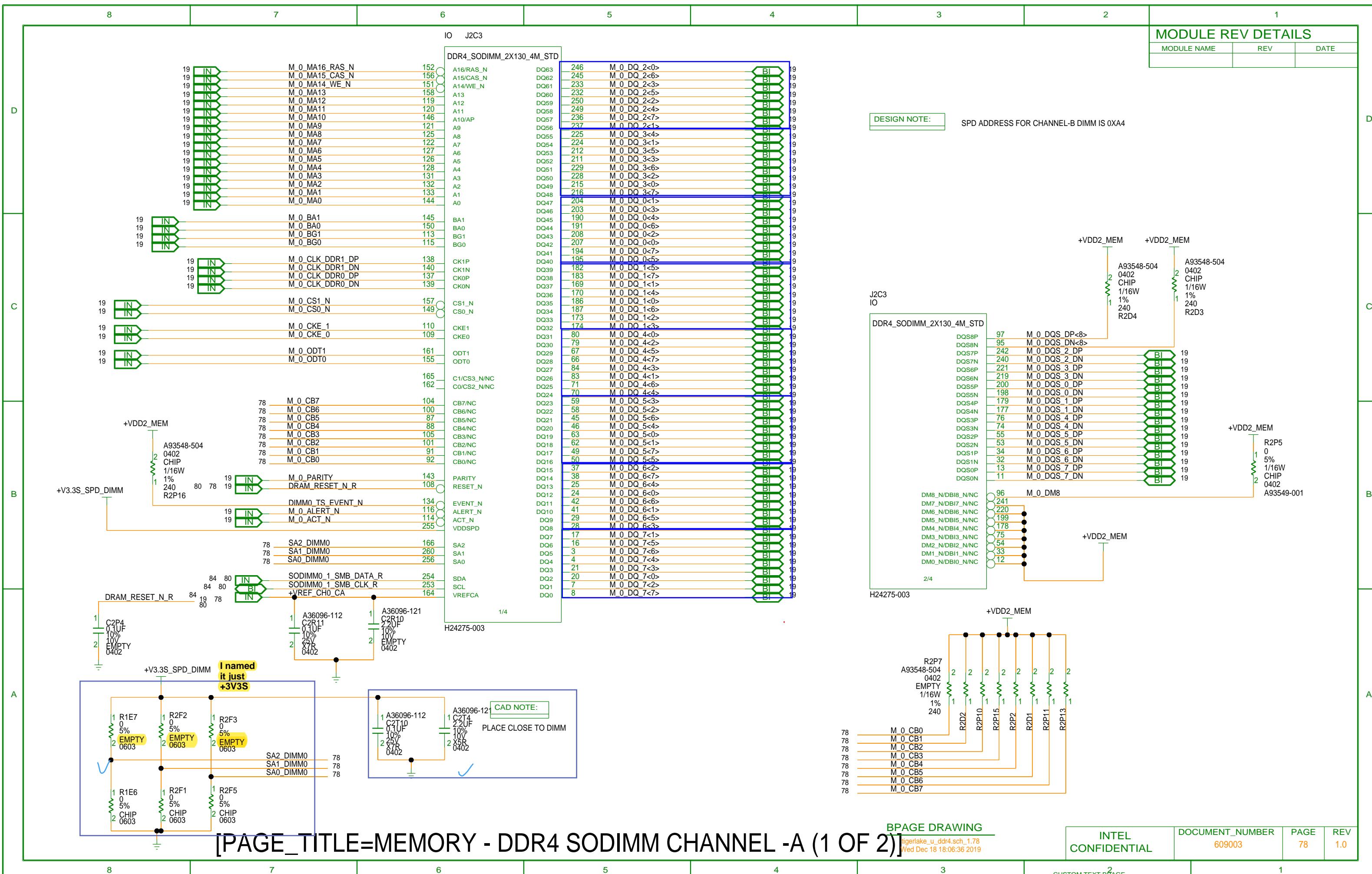
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CUSTOM TEXT 2 PAGE

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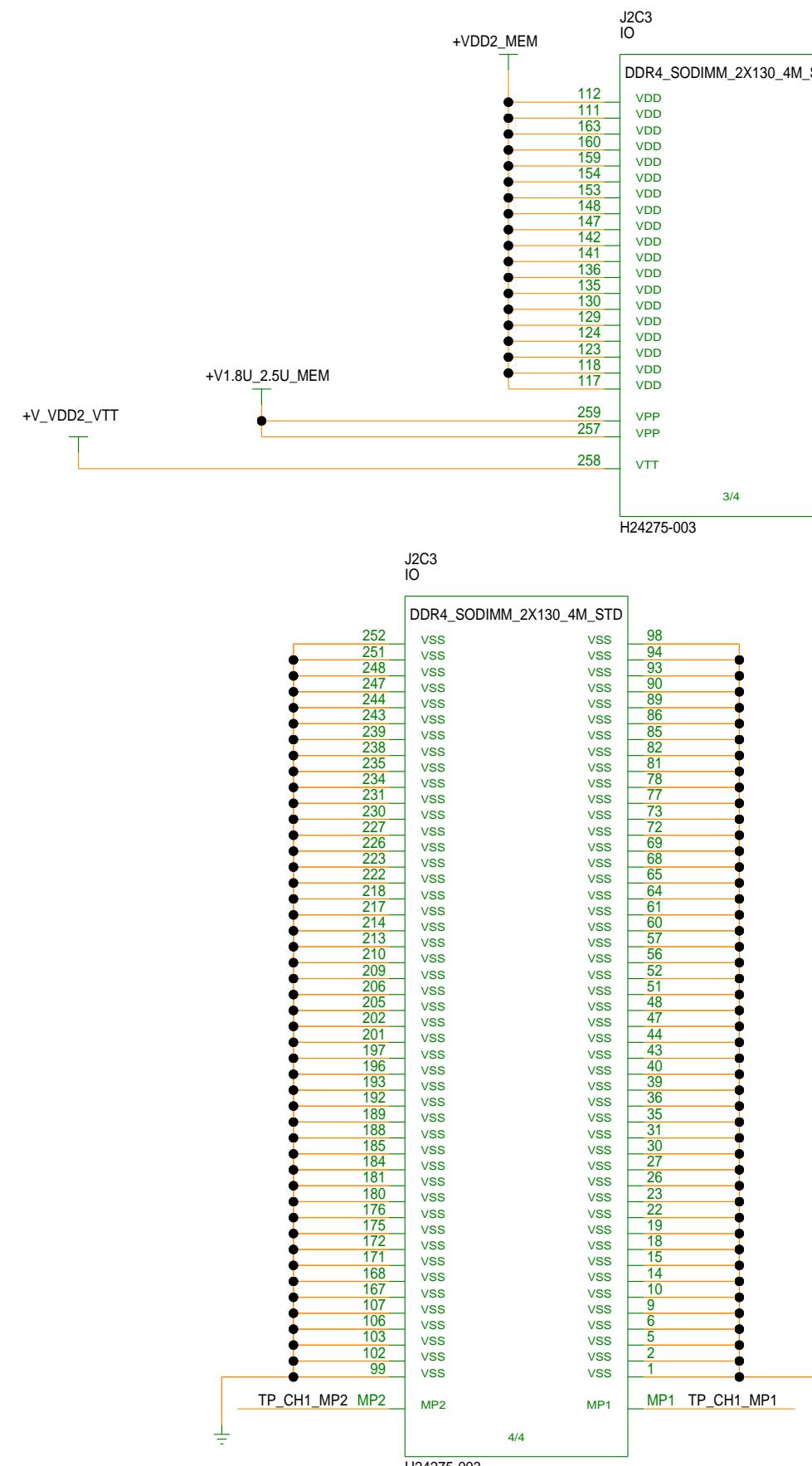
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**MODULE REV DETAILS**

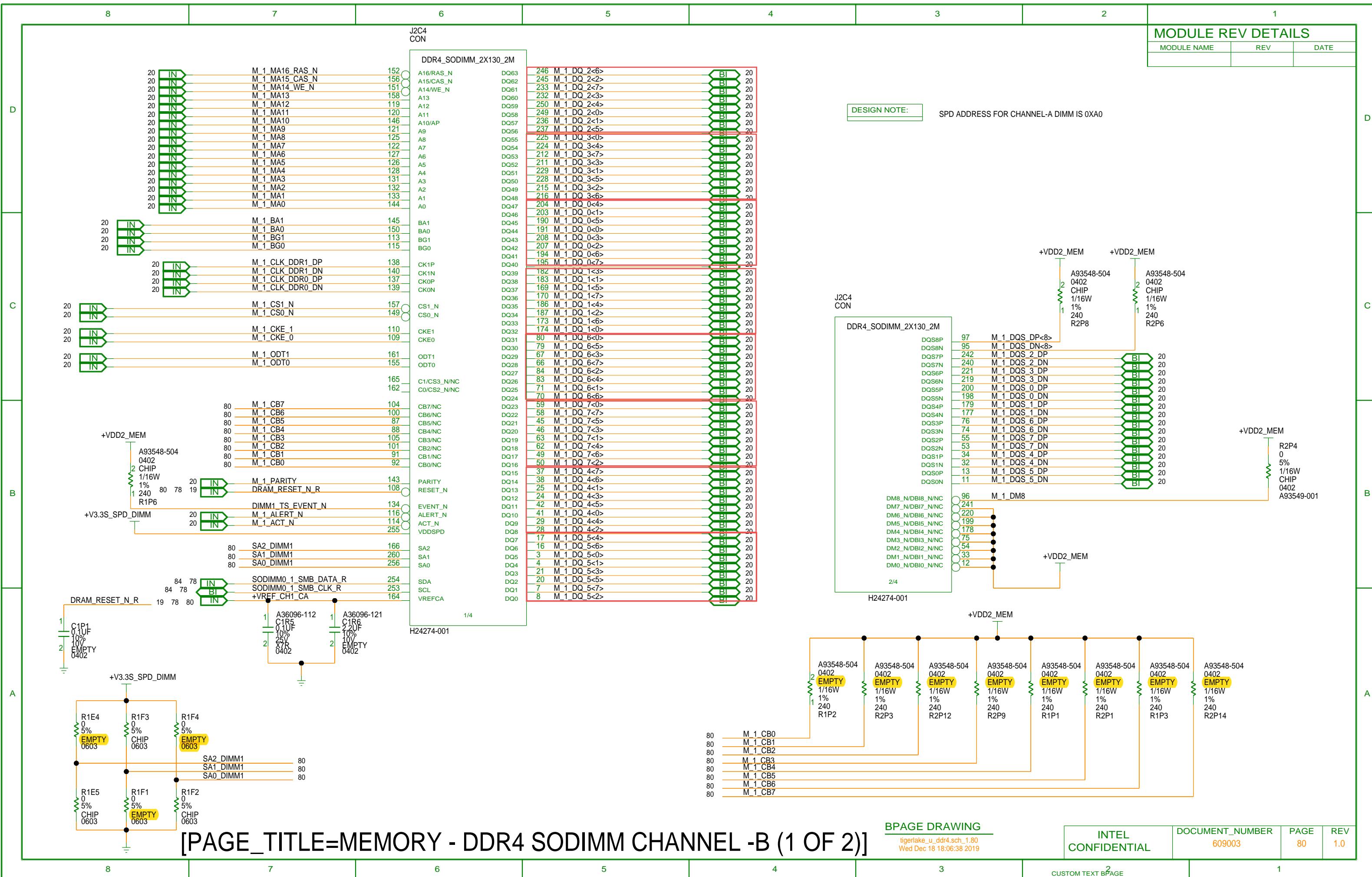
MODULE NAME	REV	DATE

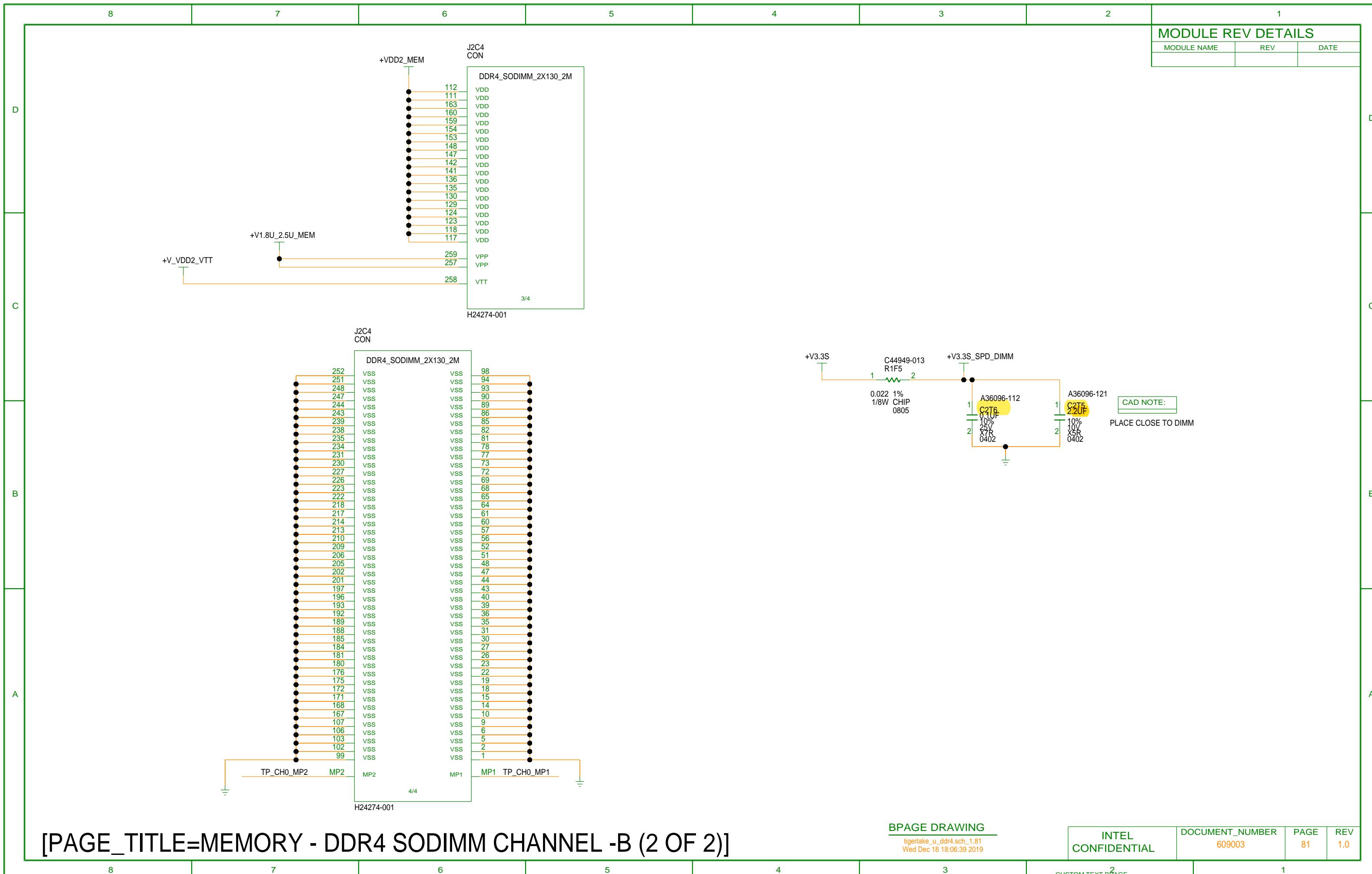


[PAGE\_TITLE=MEMORY - DDR4 SODIMM CHANNEL -A (2 OF 2)]

**BPAGE DRAWING**  
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Wed Dec 18 18:06:37 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 79	REV 1.0
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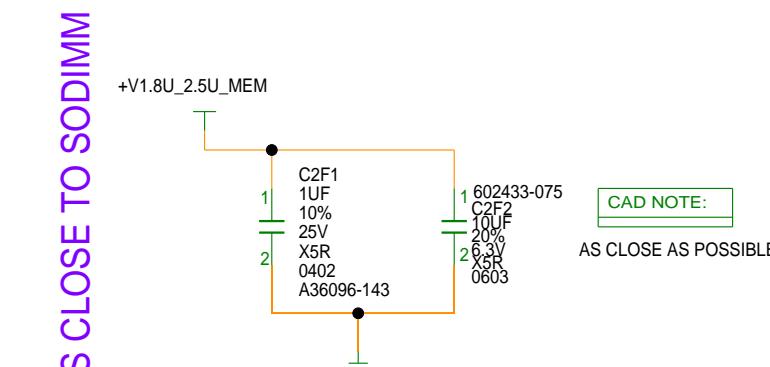
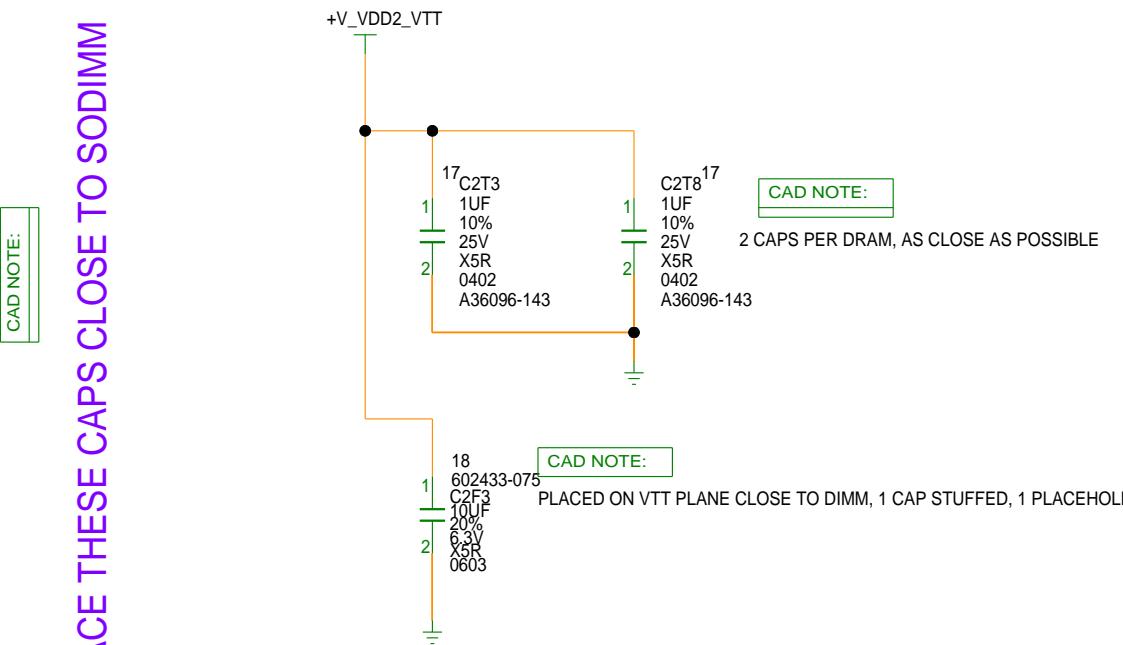
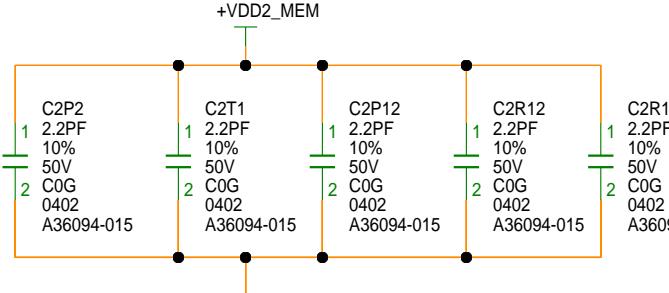
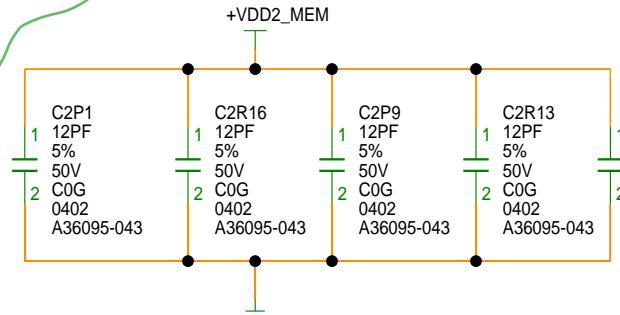
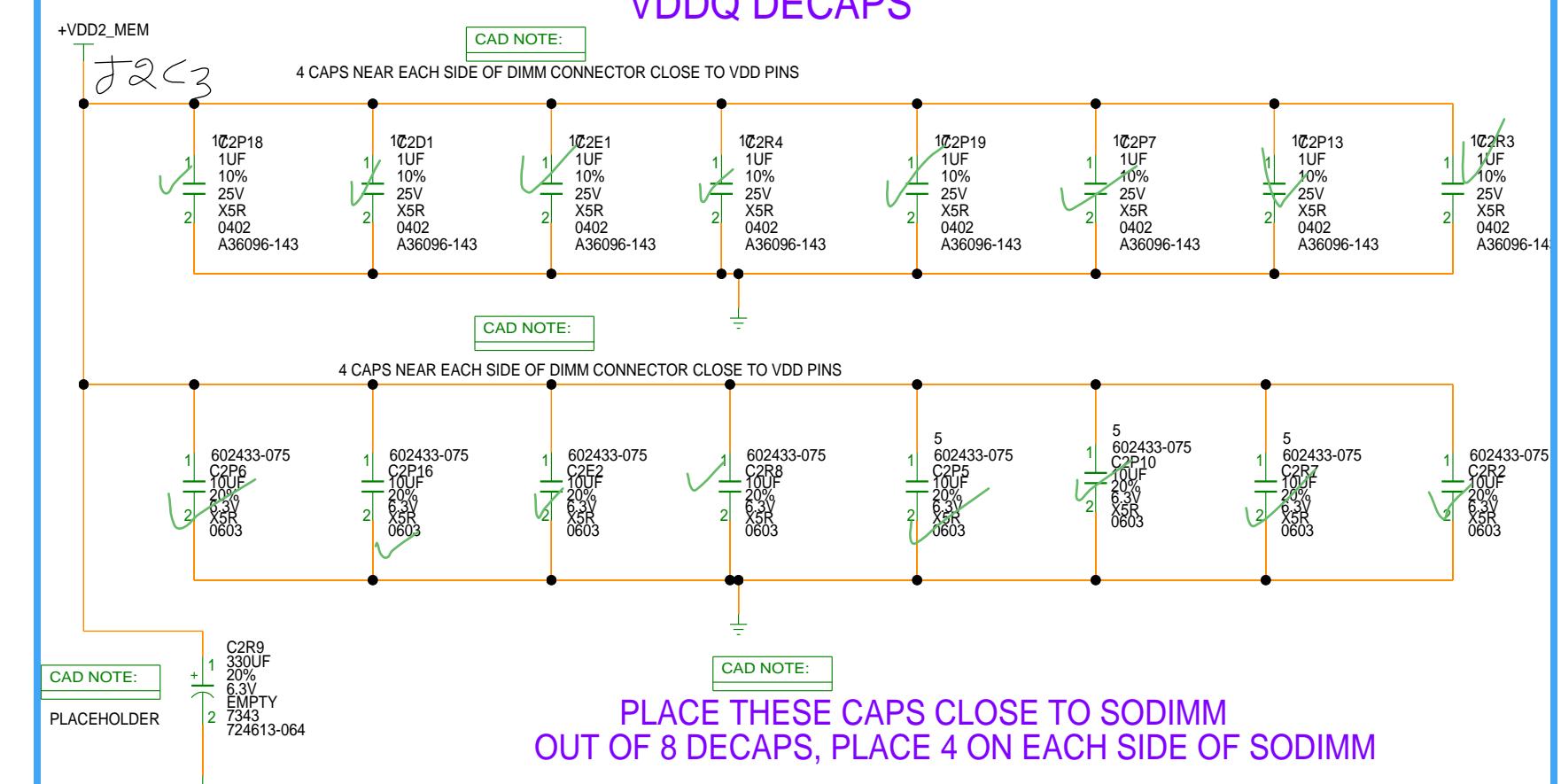


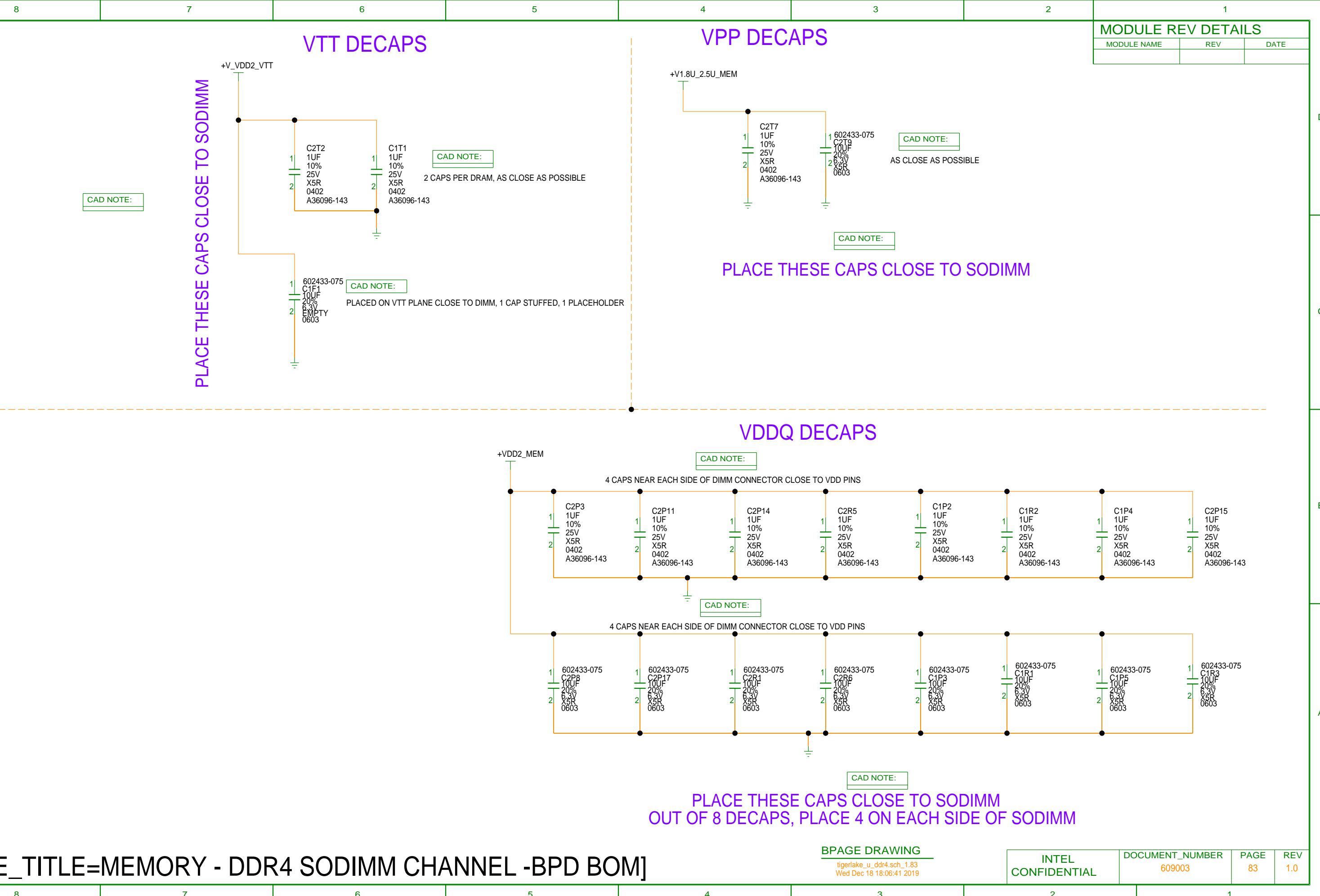


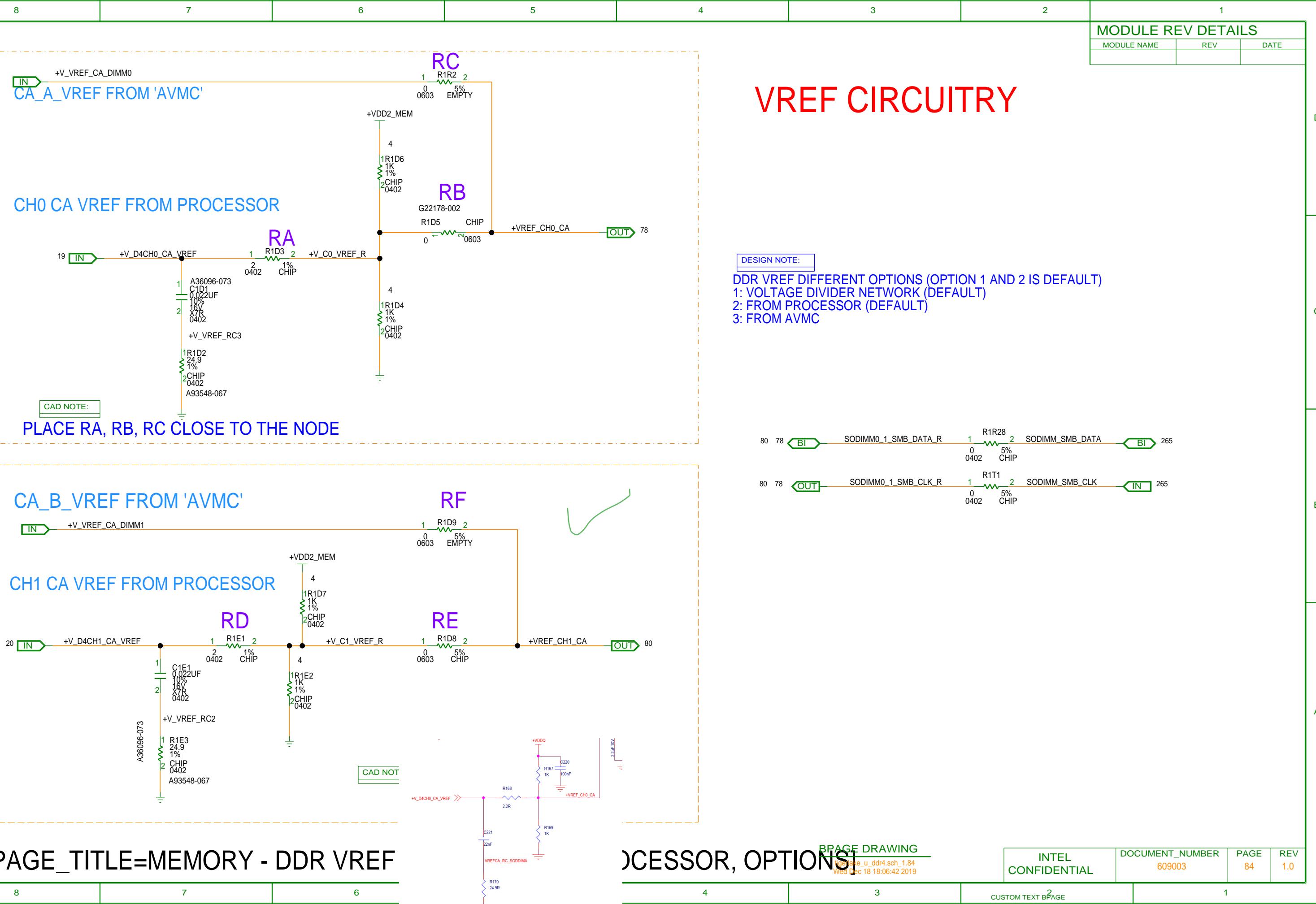
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**VTT DECAPS****VPP DECAPS****MODULE REV DETAILS**

MODULE NAME	REV	DATE

**PLACE THESE CAPS CLOSE TO SODIMM****B****CAD NOTE:**  
ABOVE CAPS ARE ADDED FOR EMC LAYOUT FEEDBACK**VDDQ DECAPS**





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**MODULE REV DETAILS**

MODULE NAME	REV	DATE

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Tue Oct 15 12:49:41 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 85	REV 1.0
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CUSTOM TEXT  
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MODULE NAME		REV	DATE				

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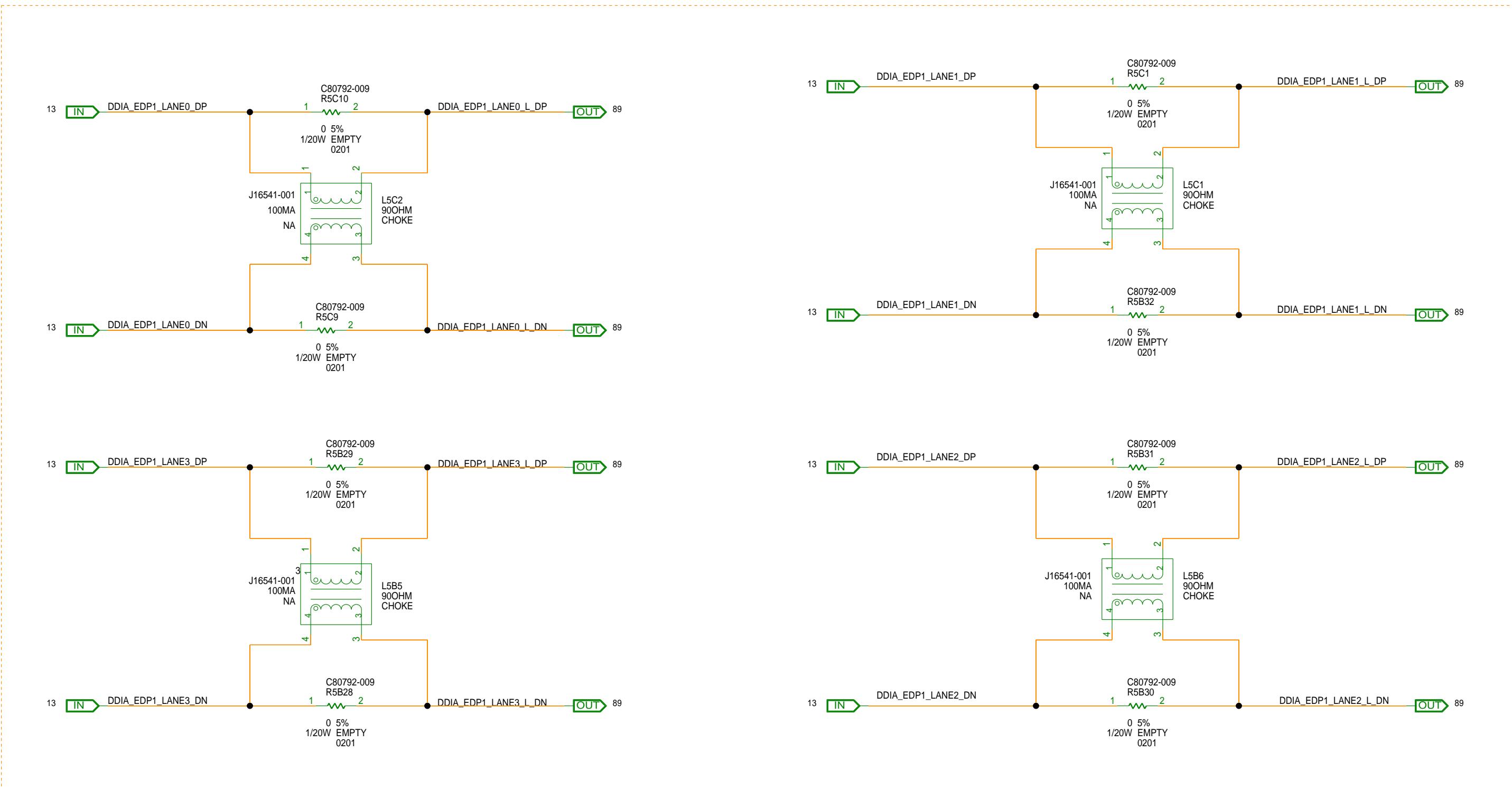
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 86	REV 1.0
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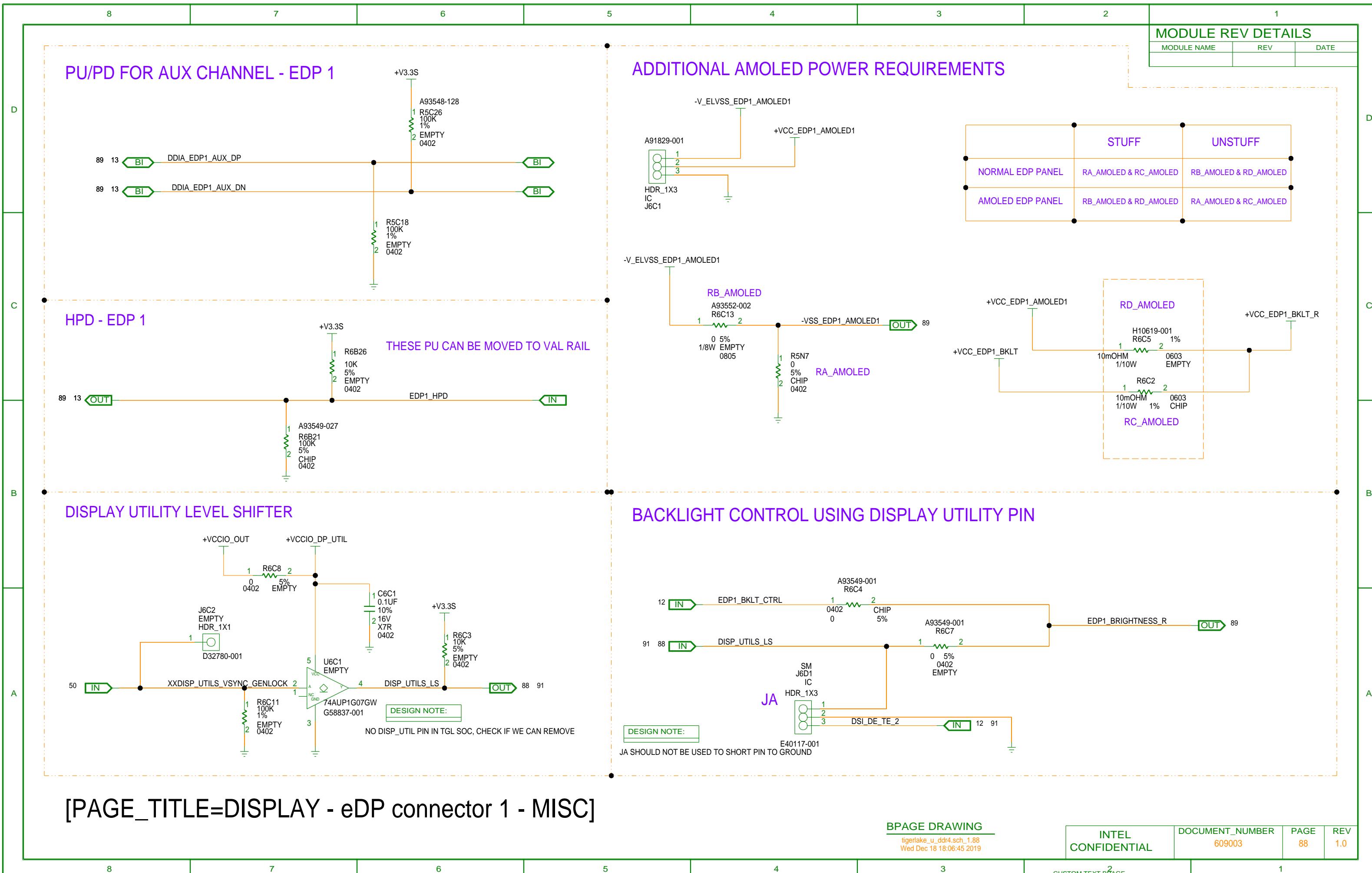


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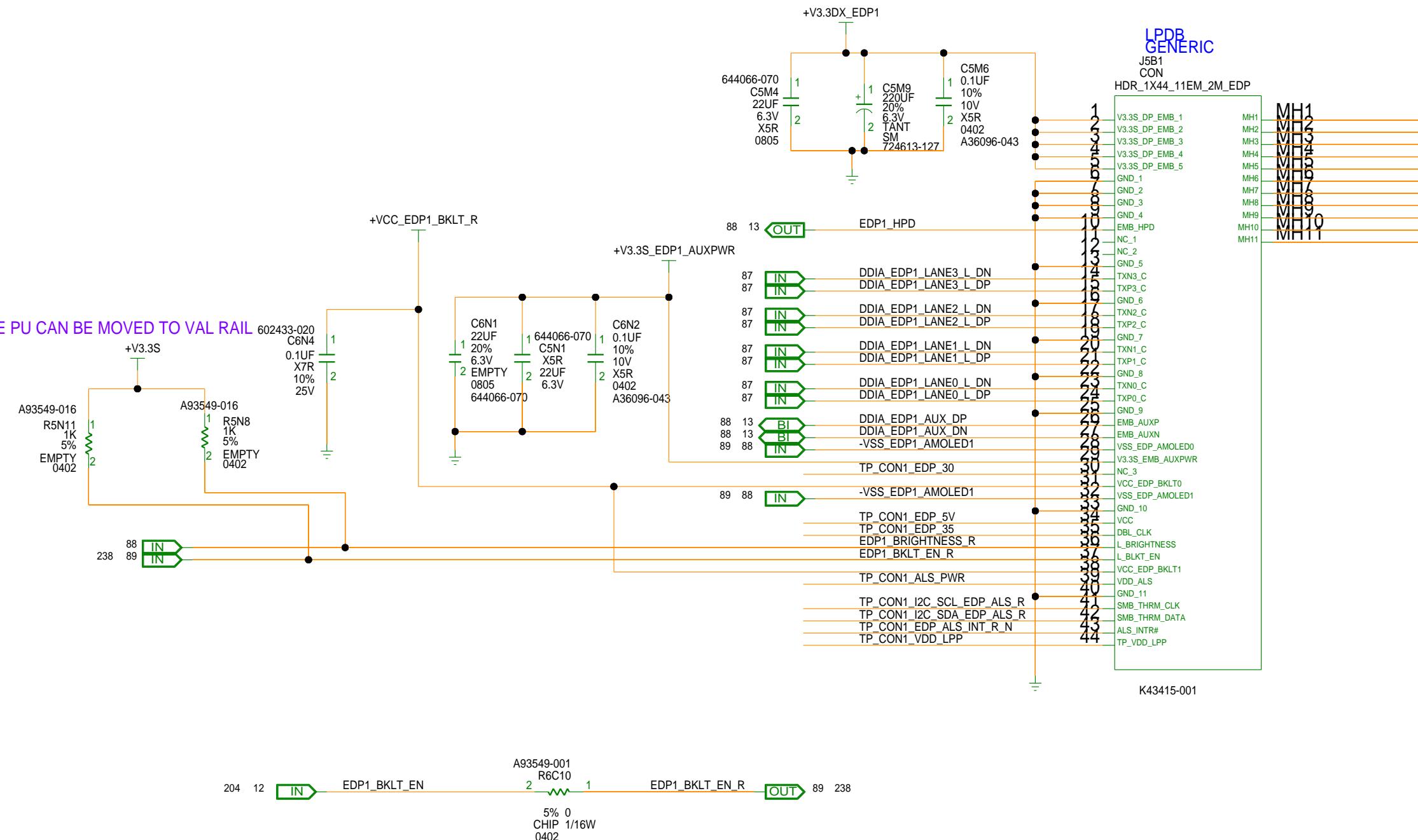
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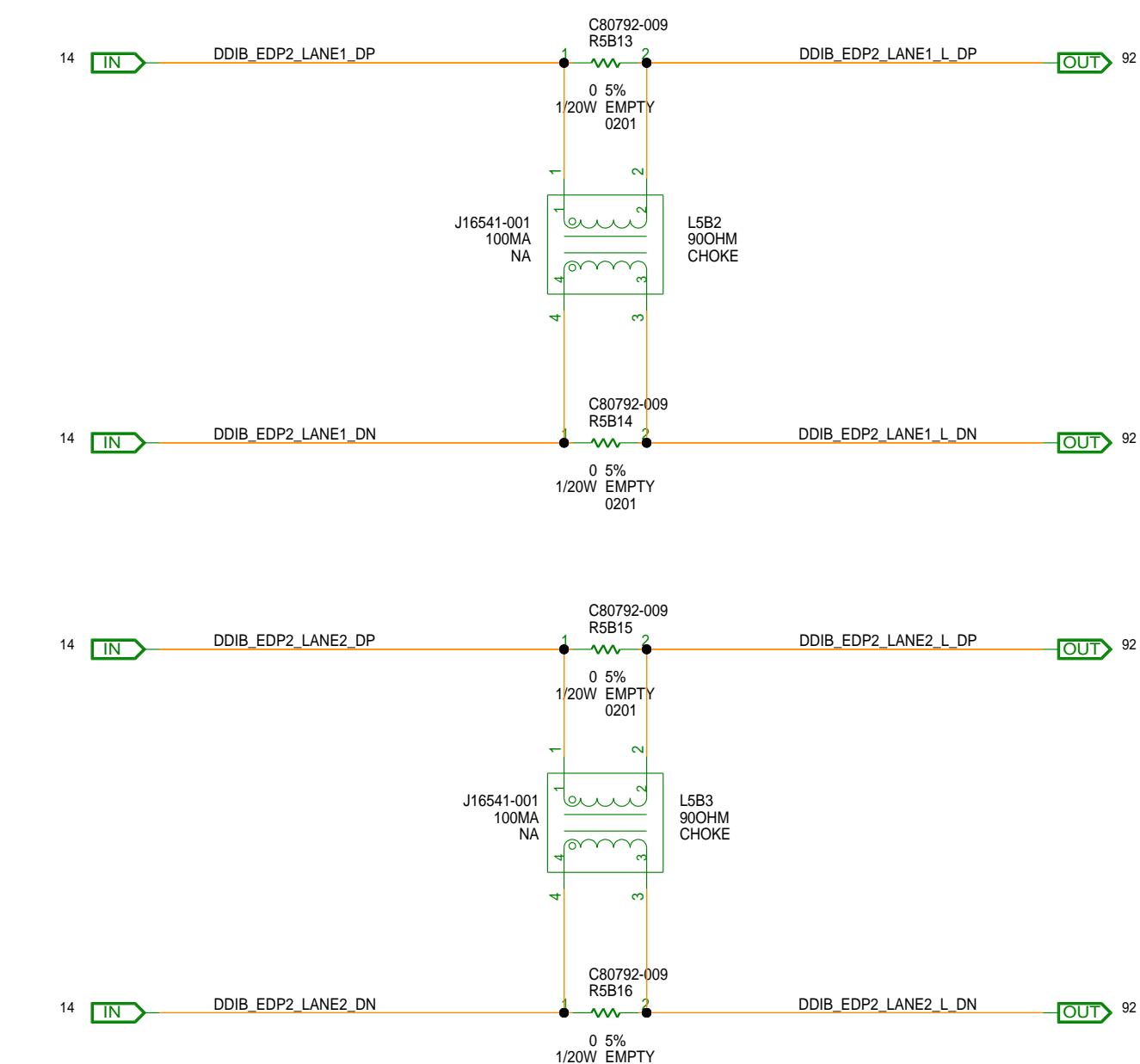
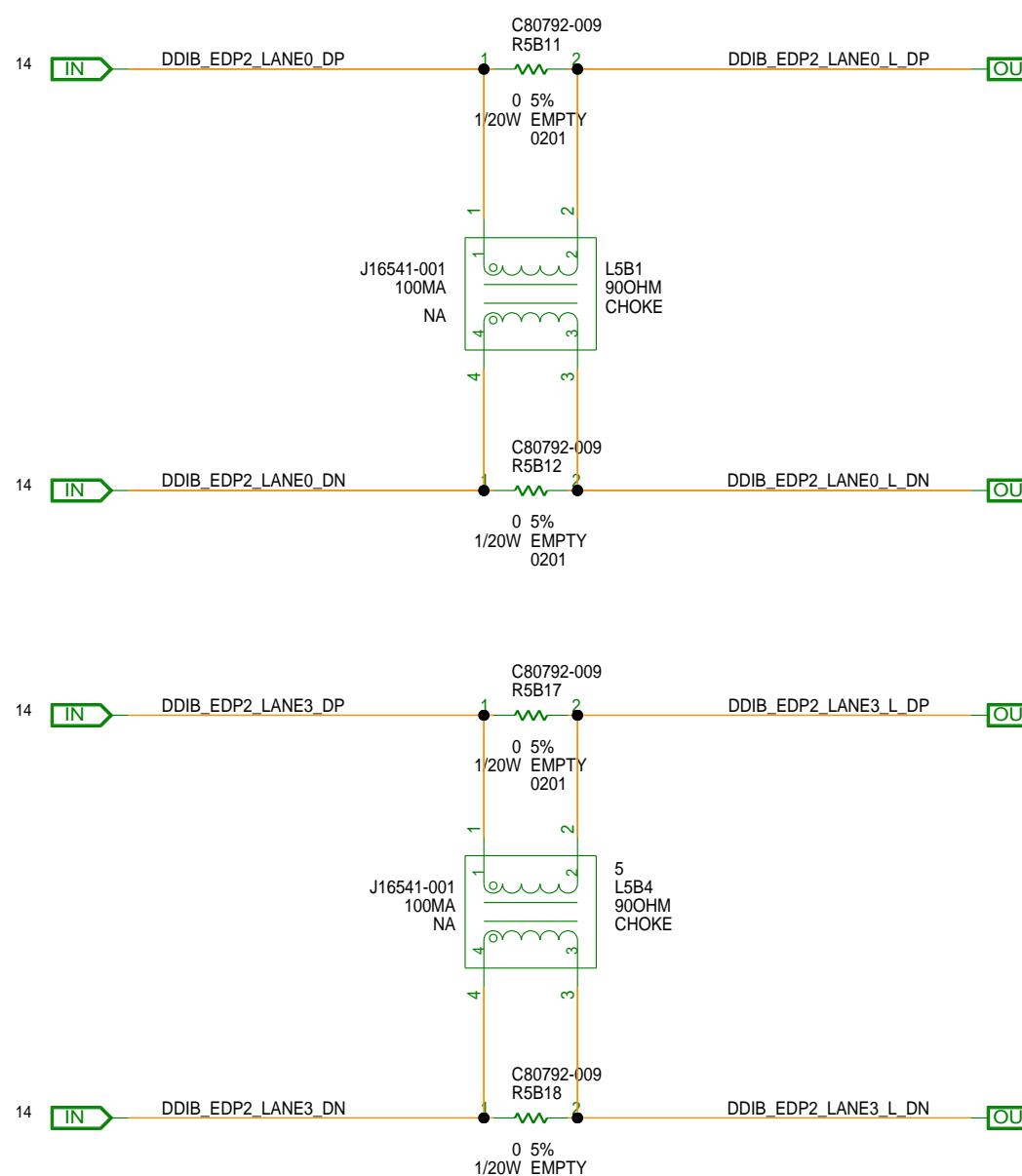
CHANGE TANT CAP TO LOWER VALUE

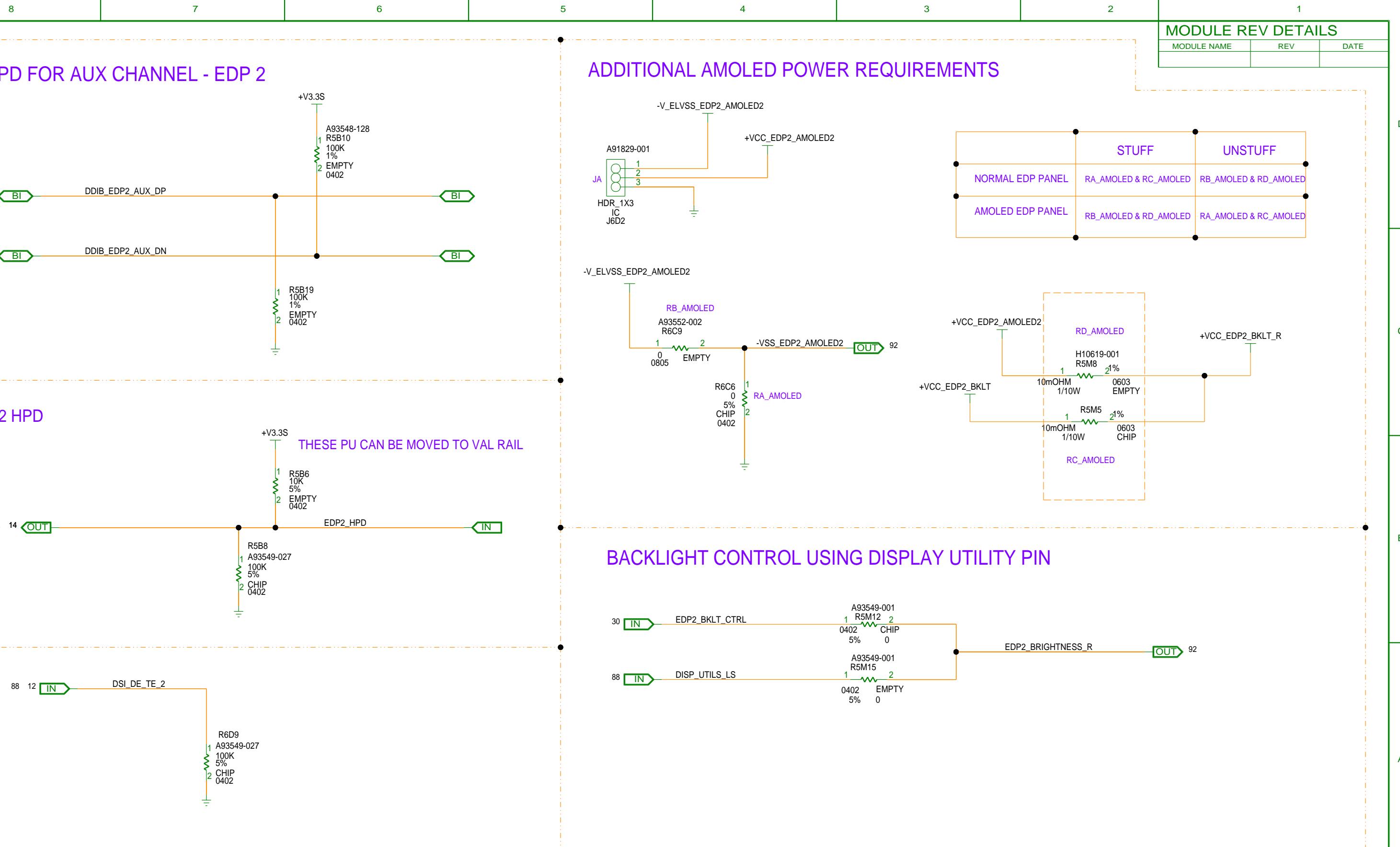
THESE PU CAN BE MOVED TO VAL RAIL



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MODULE NAME						REV	DATE

# EDP CONNECTOR 2 - CMC





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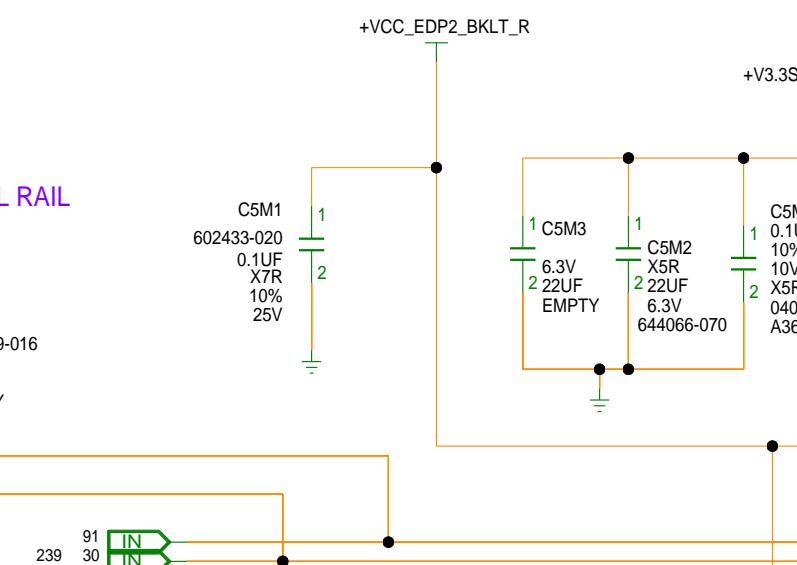
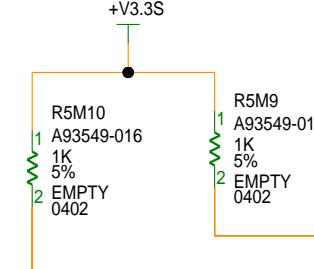
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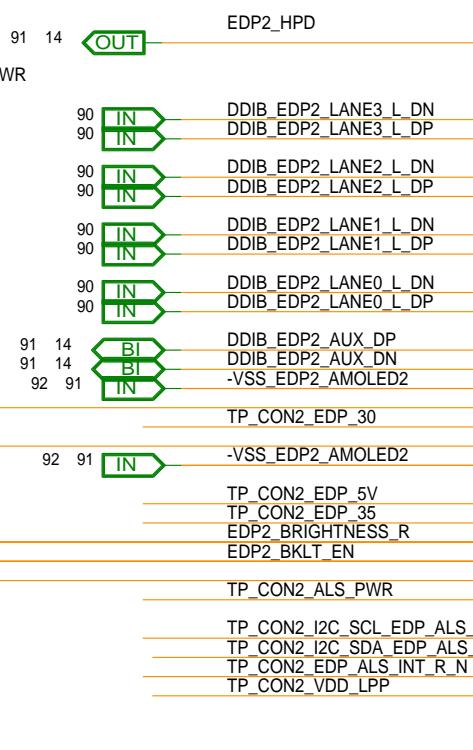
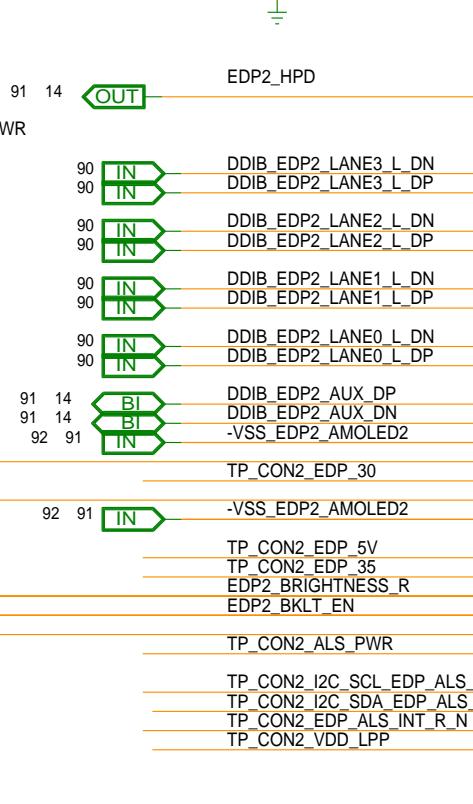
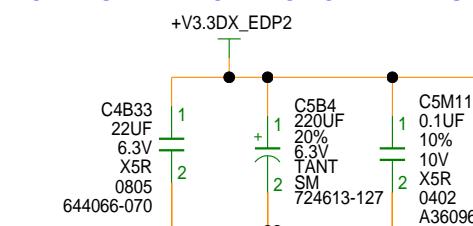
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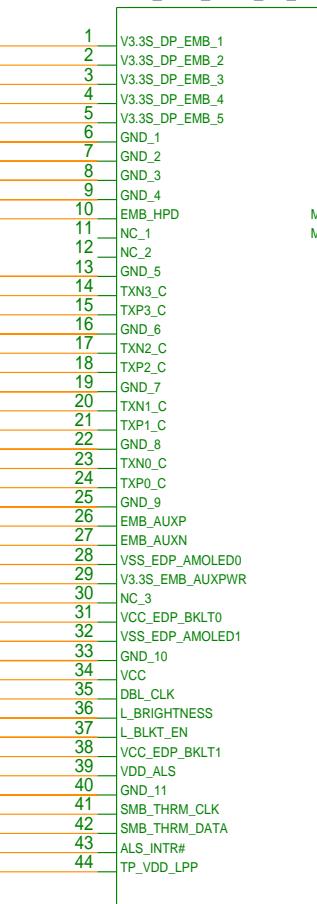
THESE PU CAN BE MOVED TO VAL RAIL



CHANGE TANT CAP TO LOWER VALUE



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**MODULE REV DETAILS**

MODULE NAME	REV	DATE

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CUSTOM TEXT <sup>2</sup>B PAGE

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**MODULE REV DETAILS**

MODULE NAME	REV	DATE

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CUSTOM TEXT <sup>2</sup>BPAGE

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MODULE NAME		REV	DATE				

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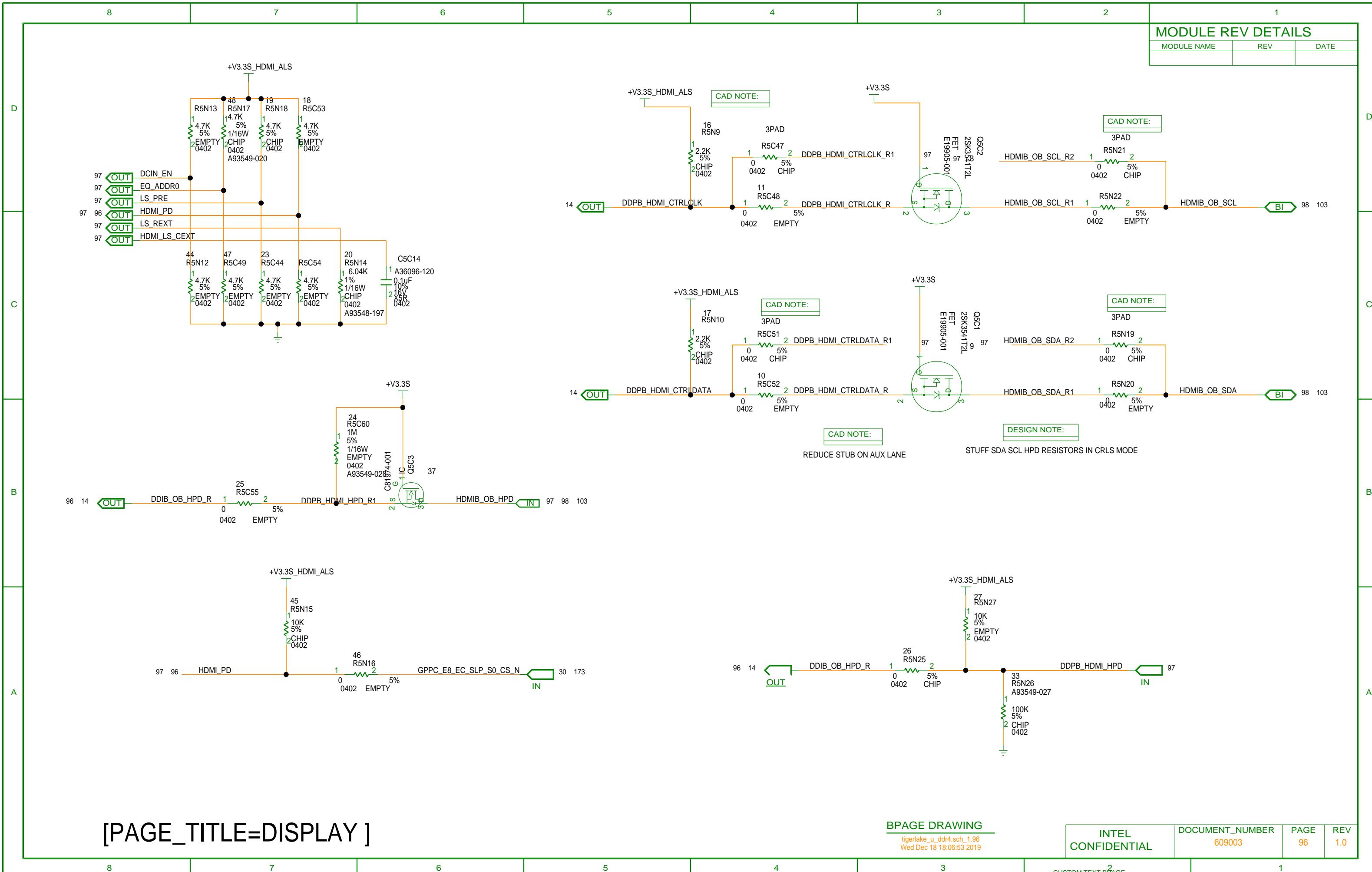
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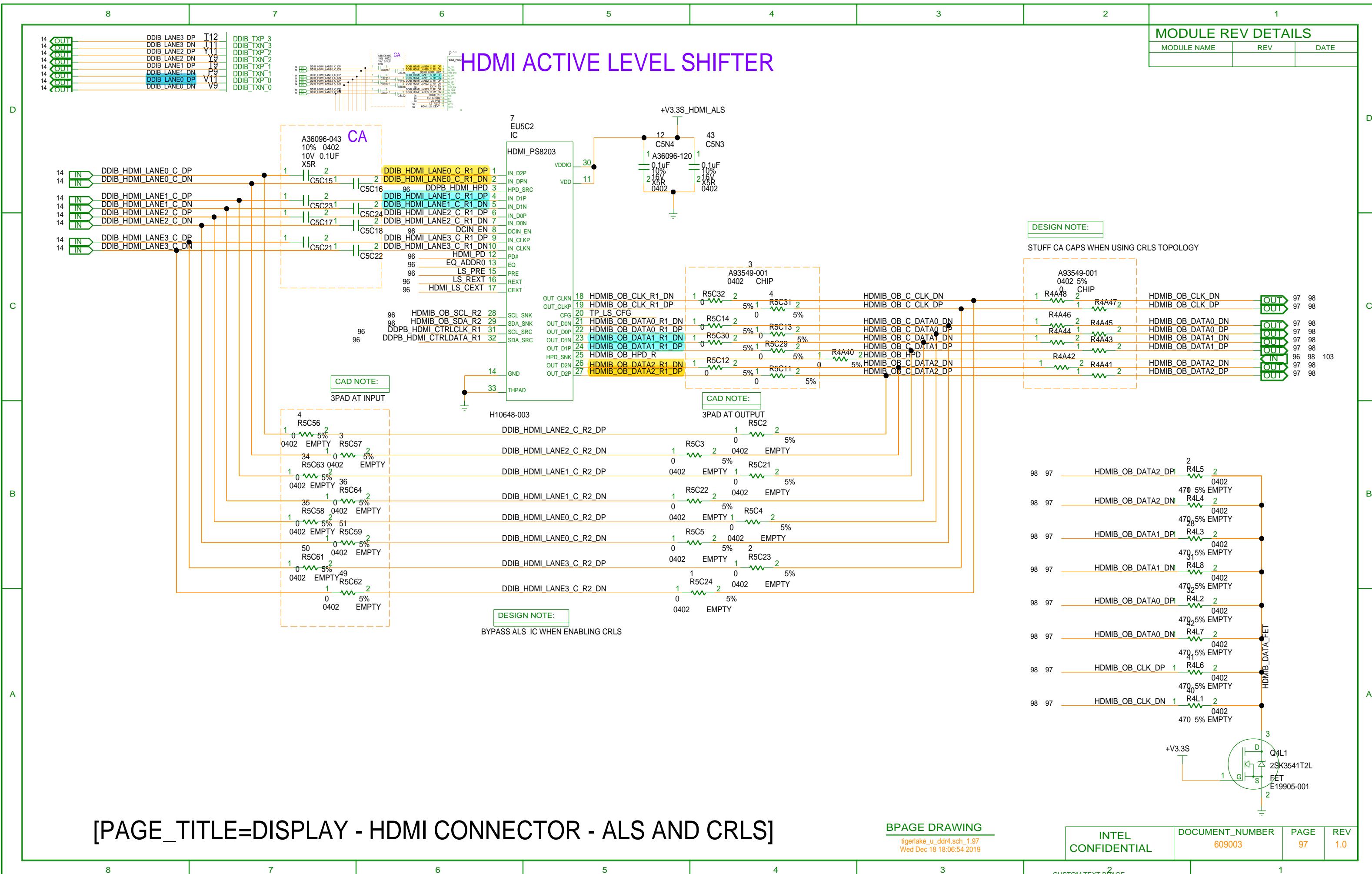
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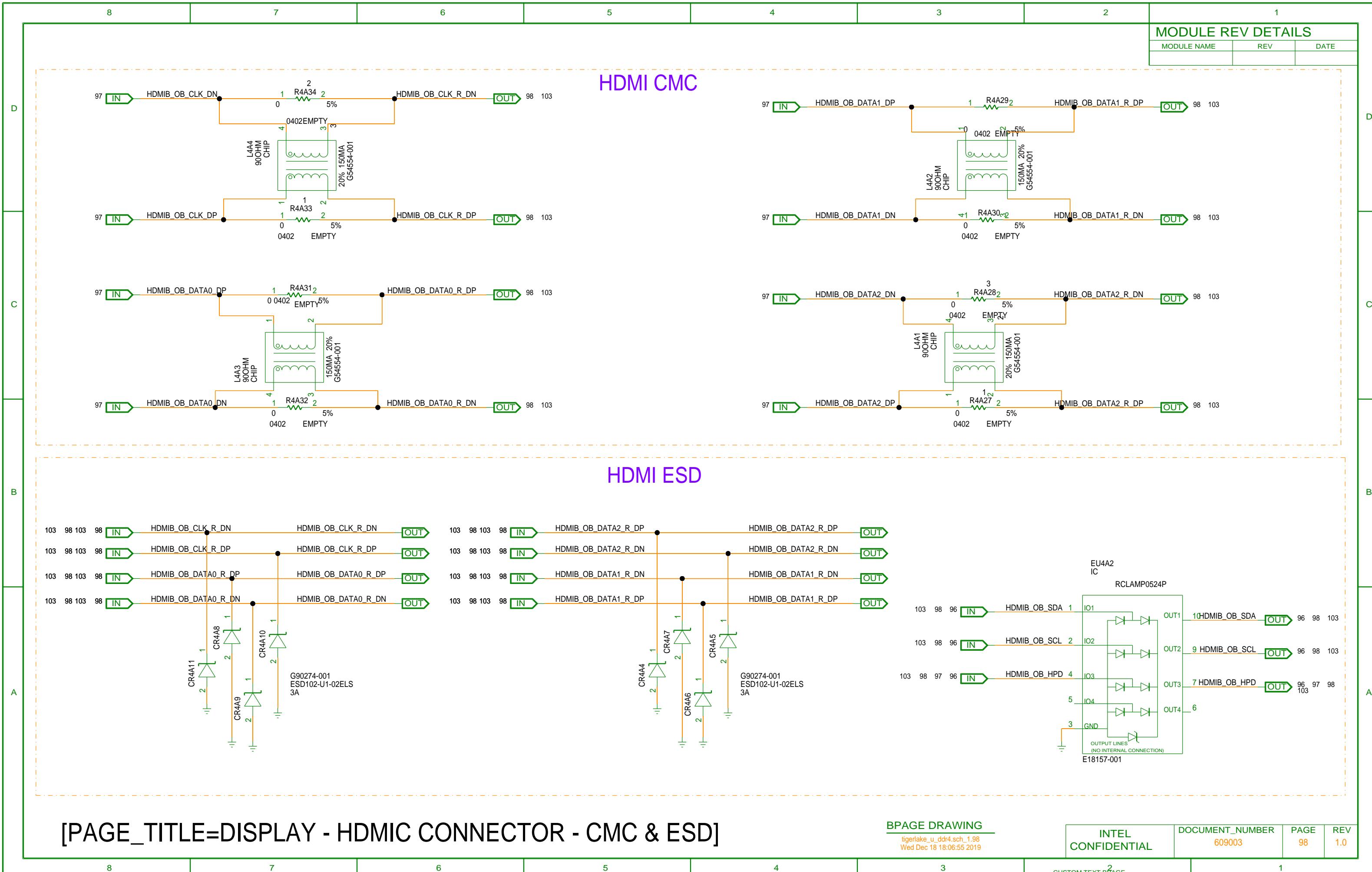
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 95	REV 1.0
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MODULE REV DETAILS		
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Tue Oct 15 12:49:53 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 99	REV 1.0
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CUSTOM TEXT 2 PAGE

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

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CUSTOM TEXT  
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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 101	REV 1.0
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**MODULE REV DETAILS**

MODULE NAME	REV	DATE

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INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 102	REV 1.0
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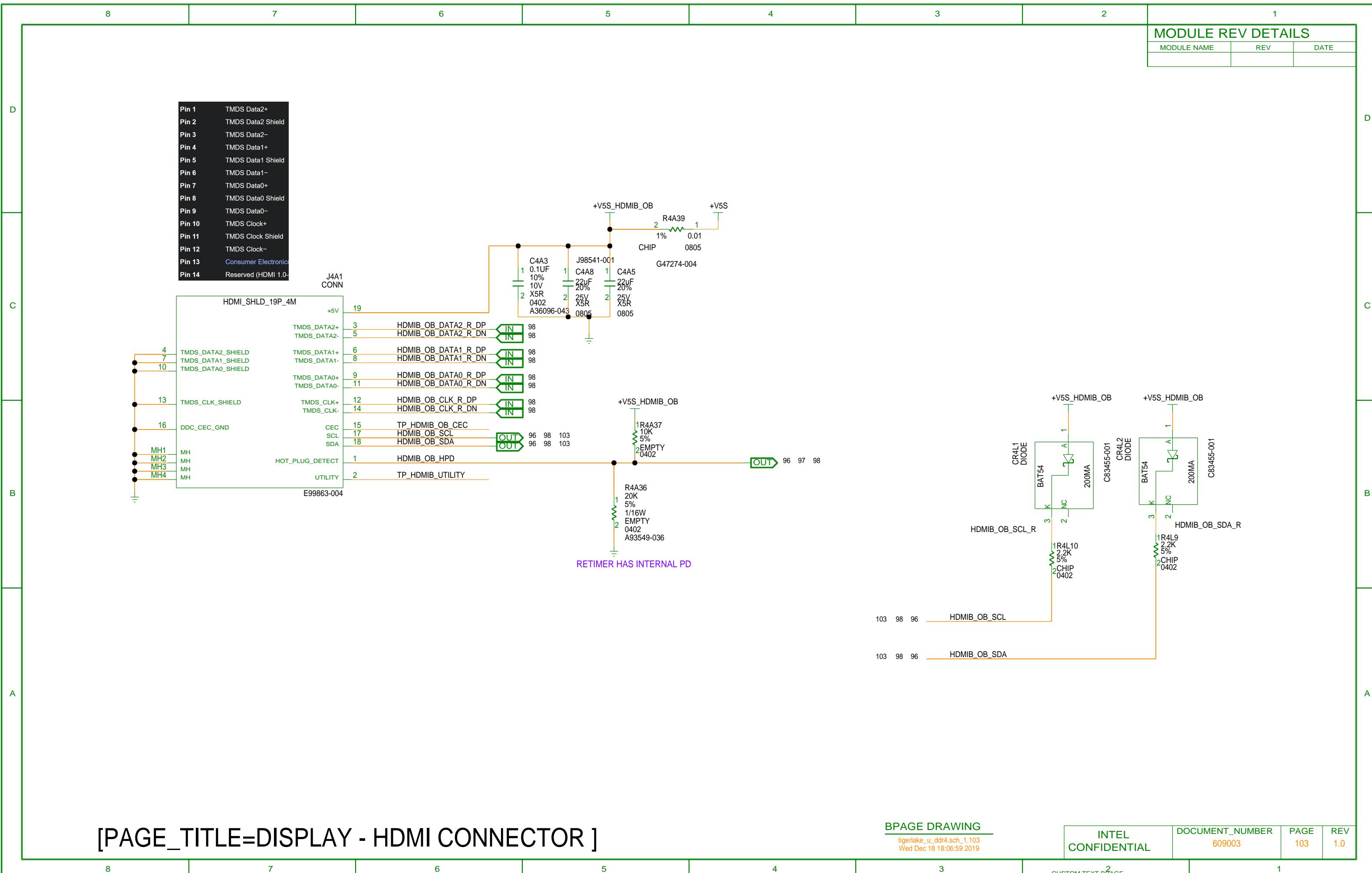
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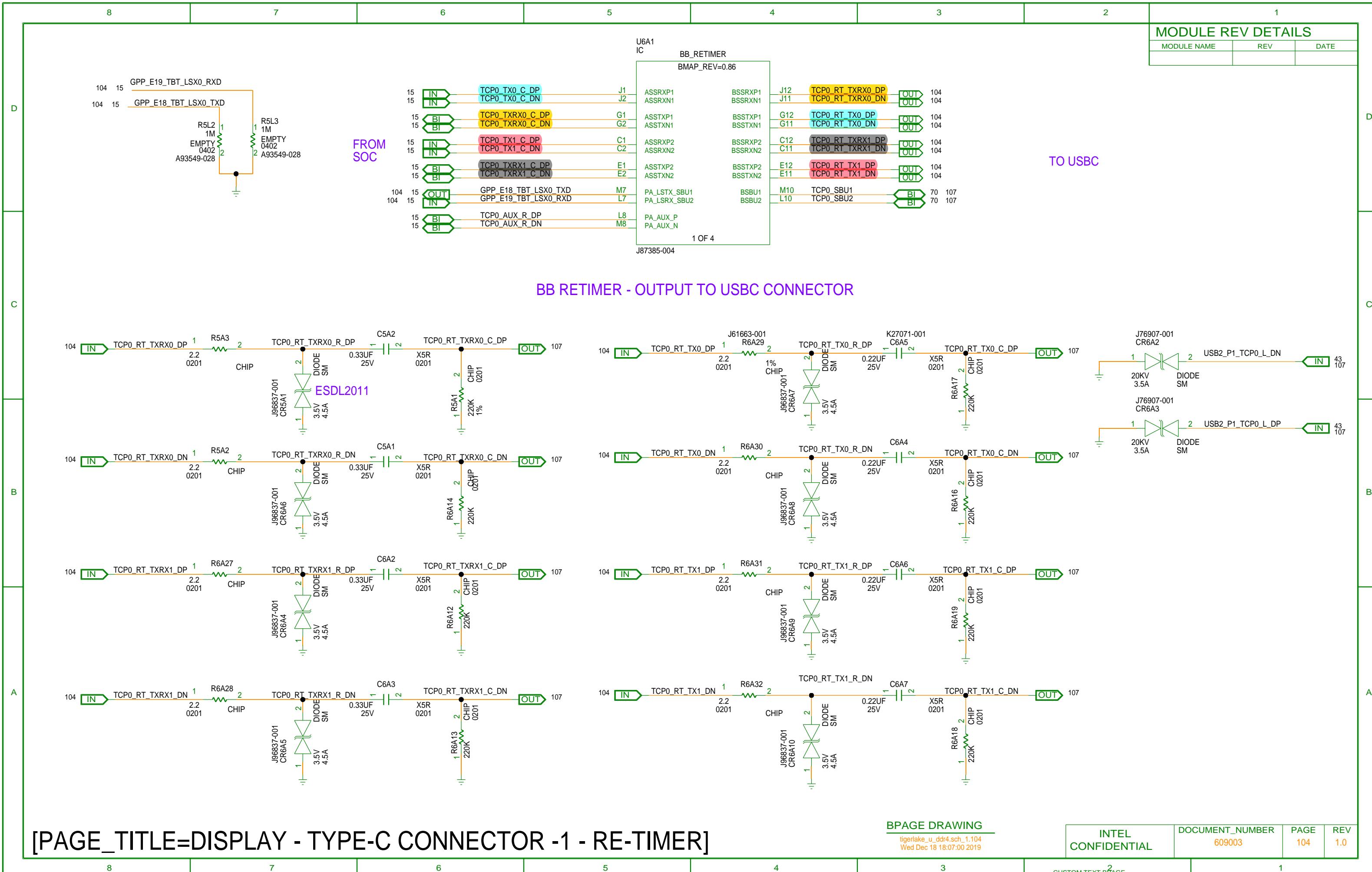
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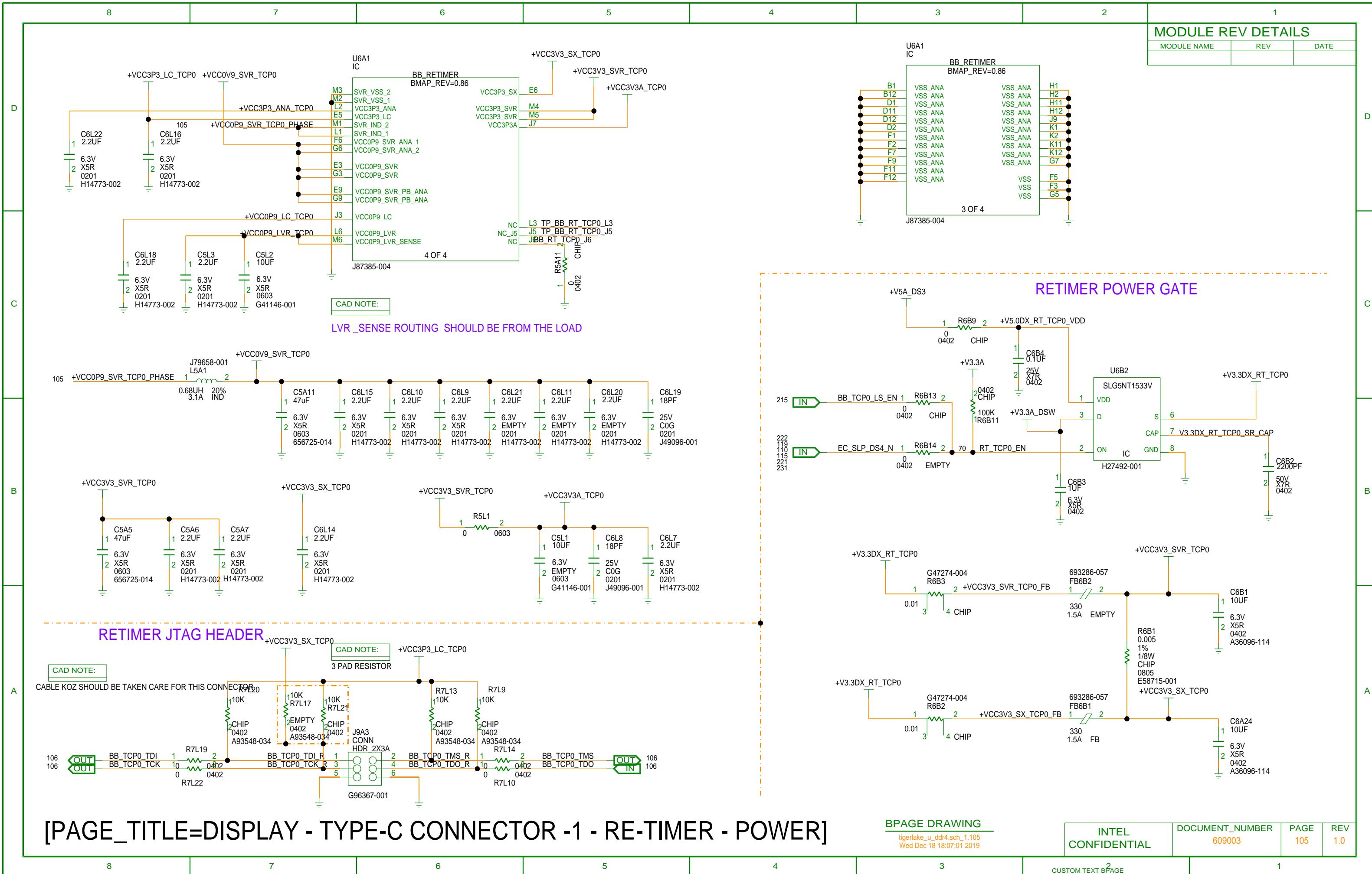
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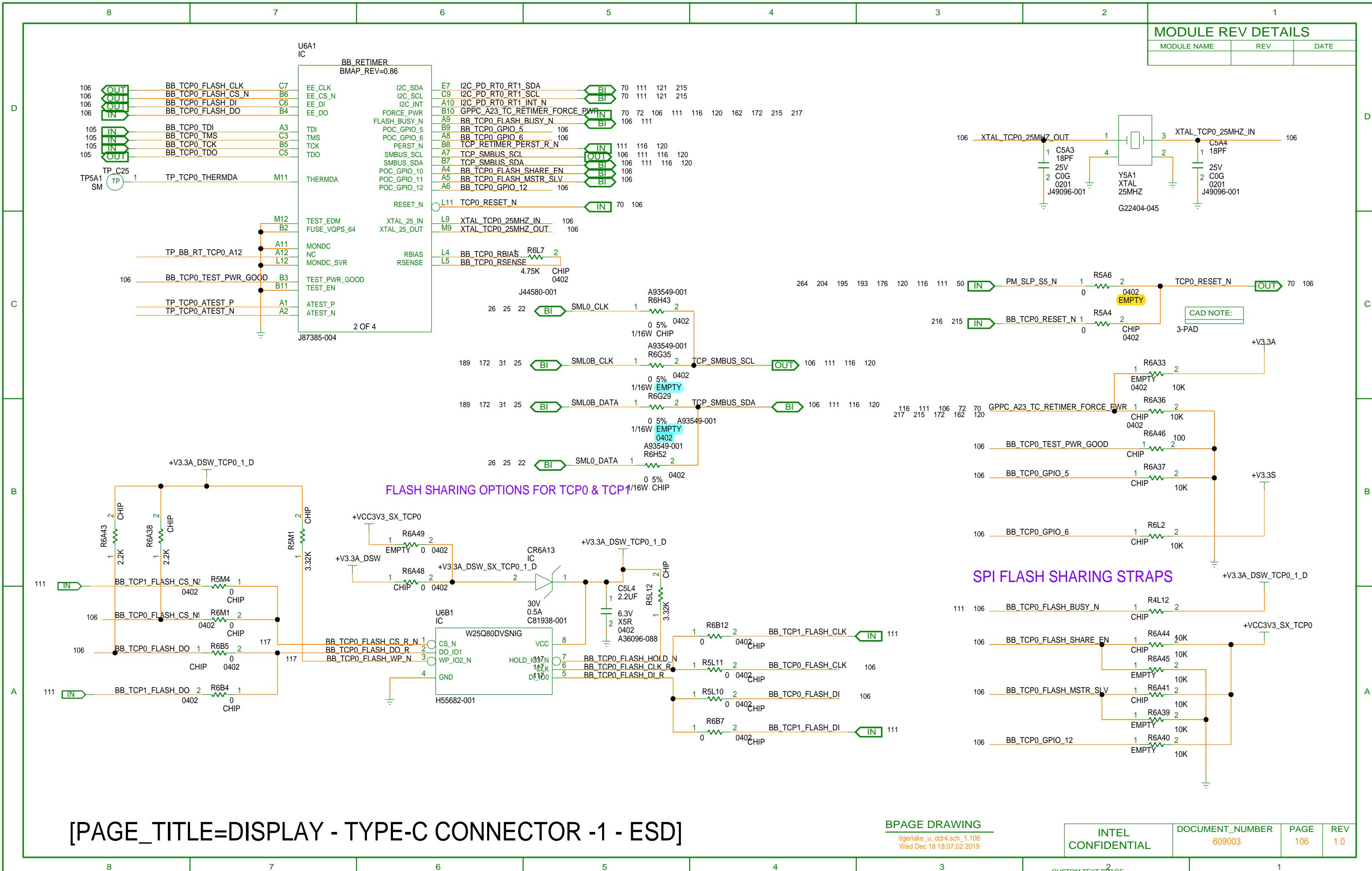
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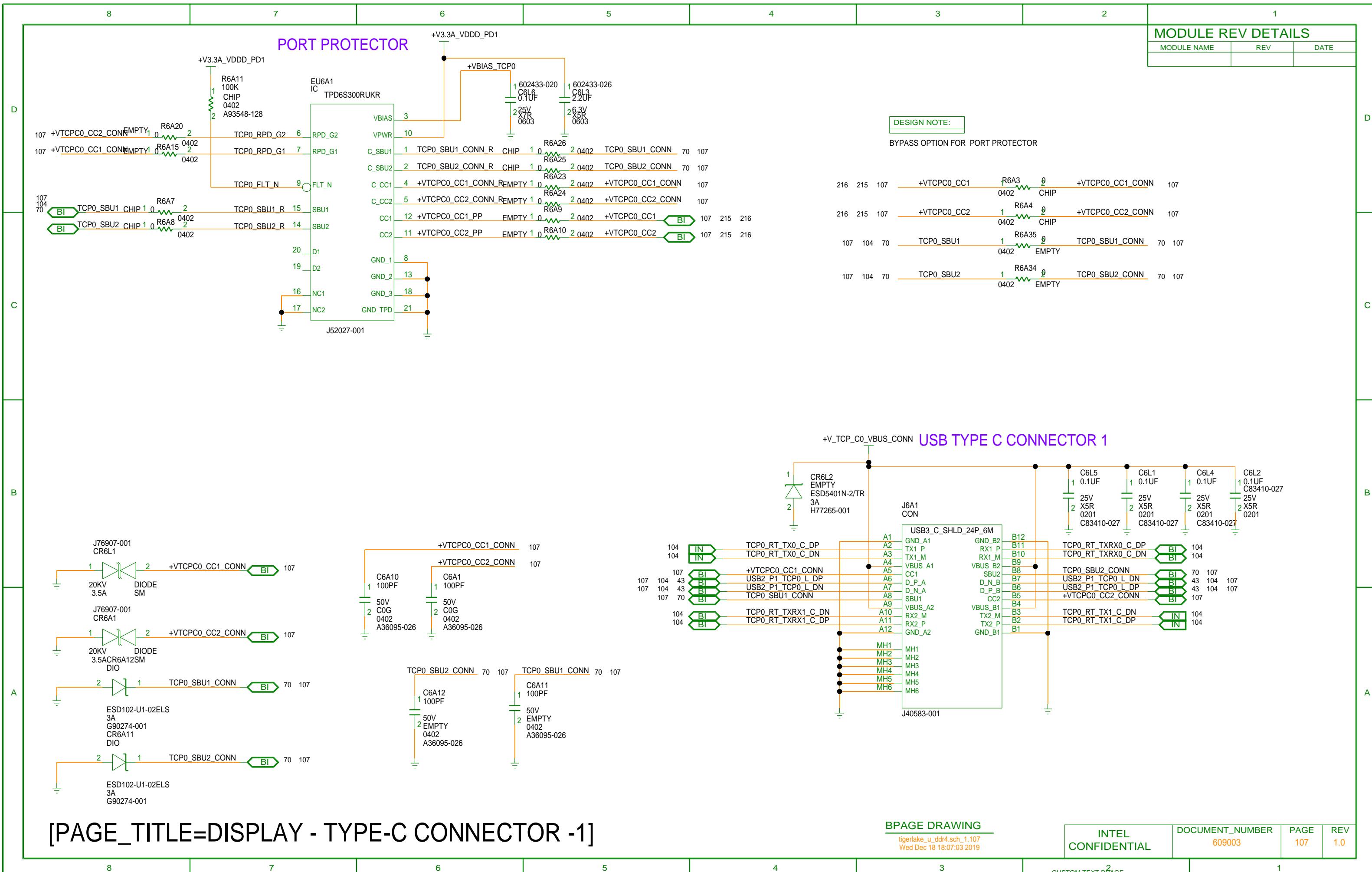
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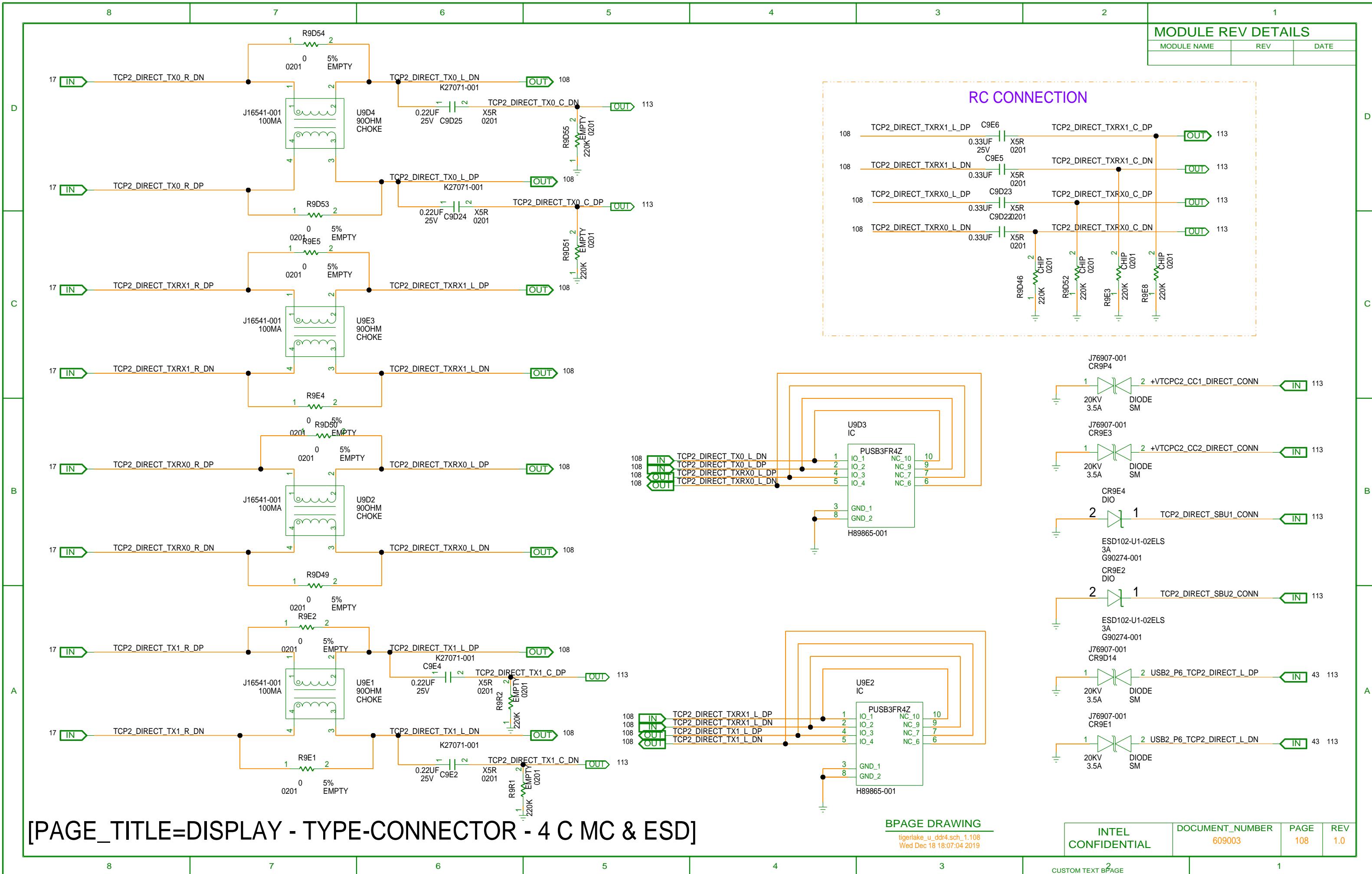


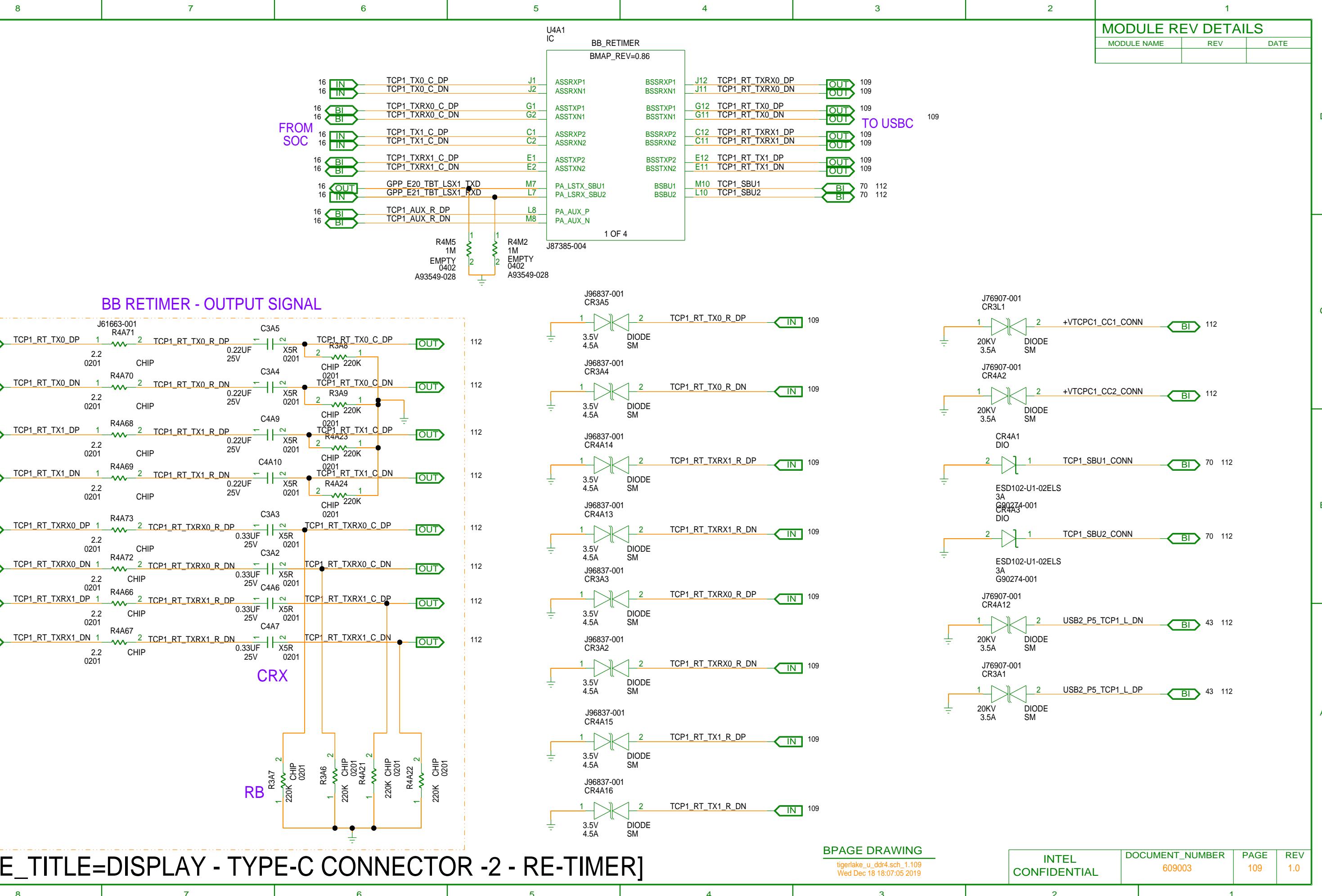


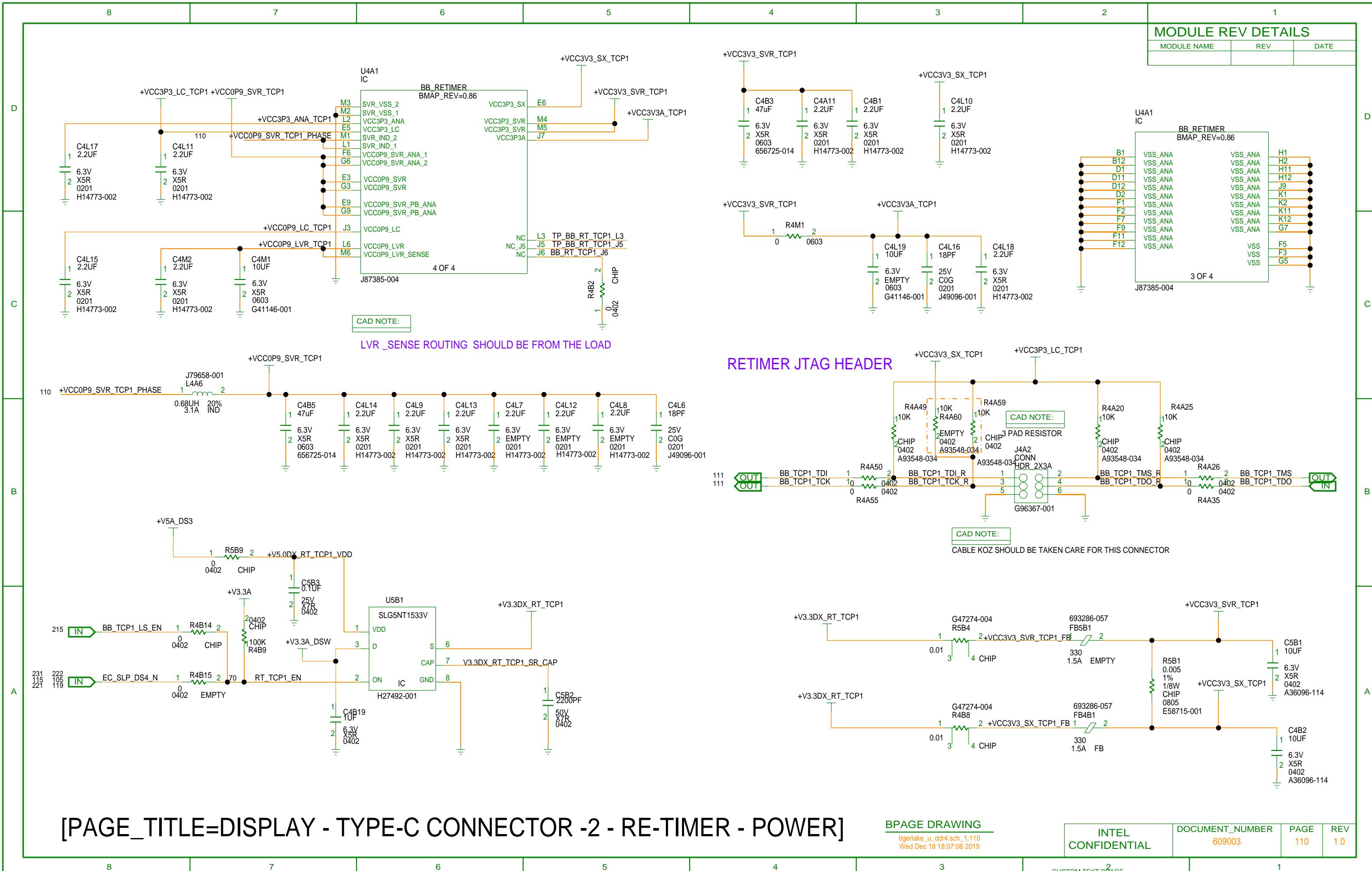


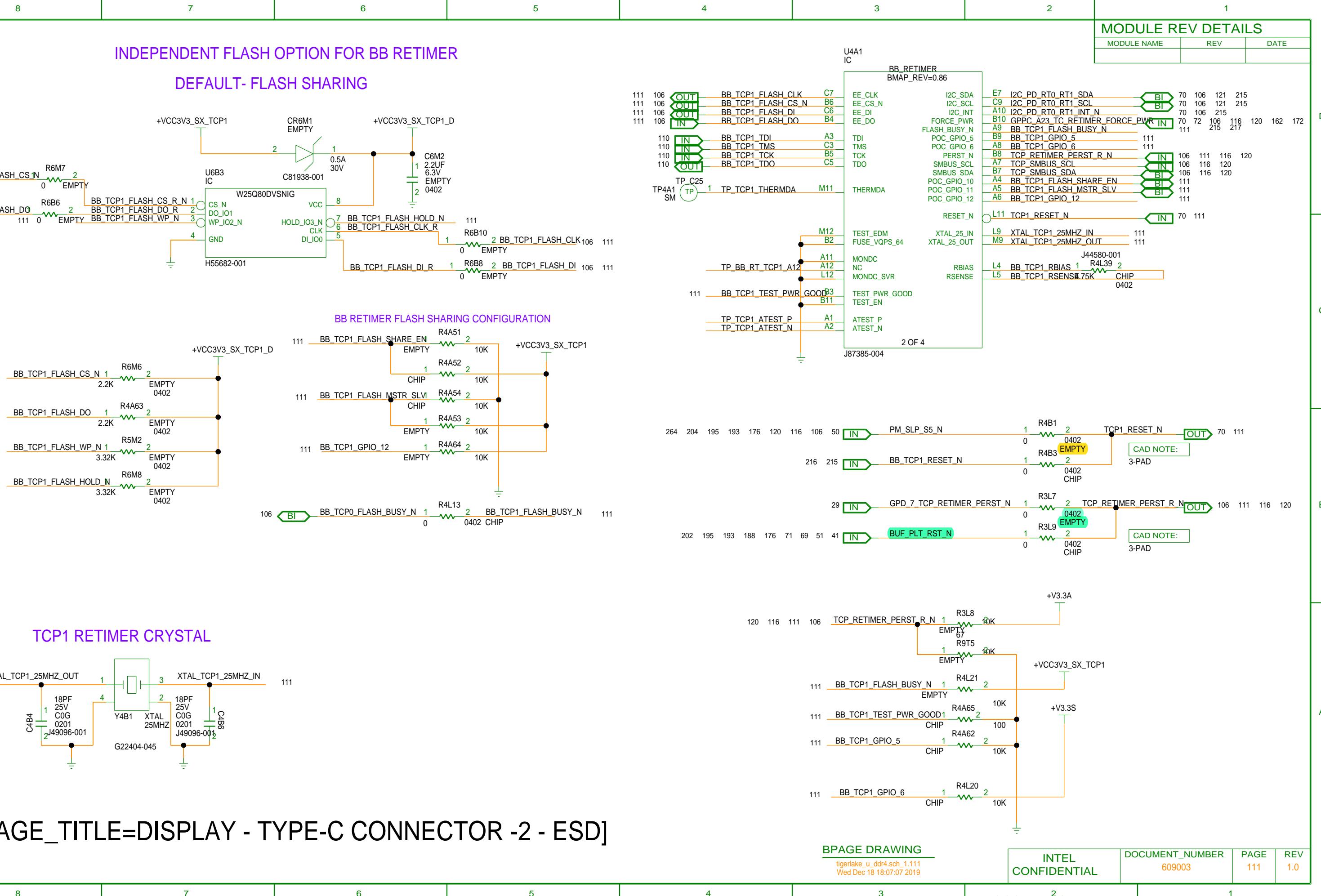


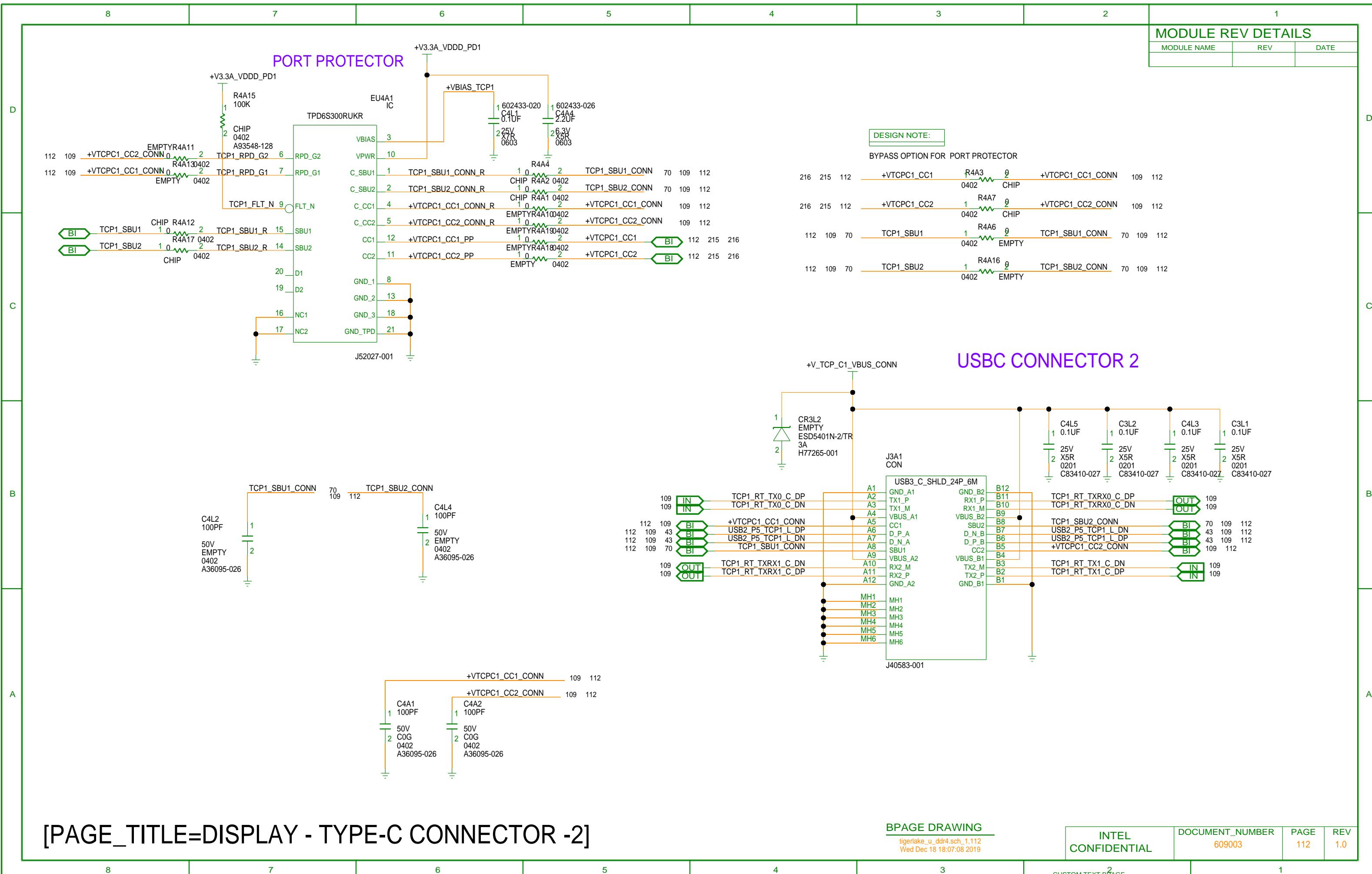


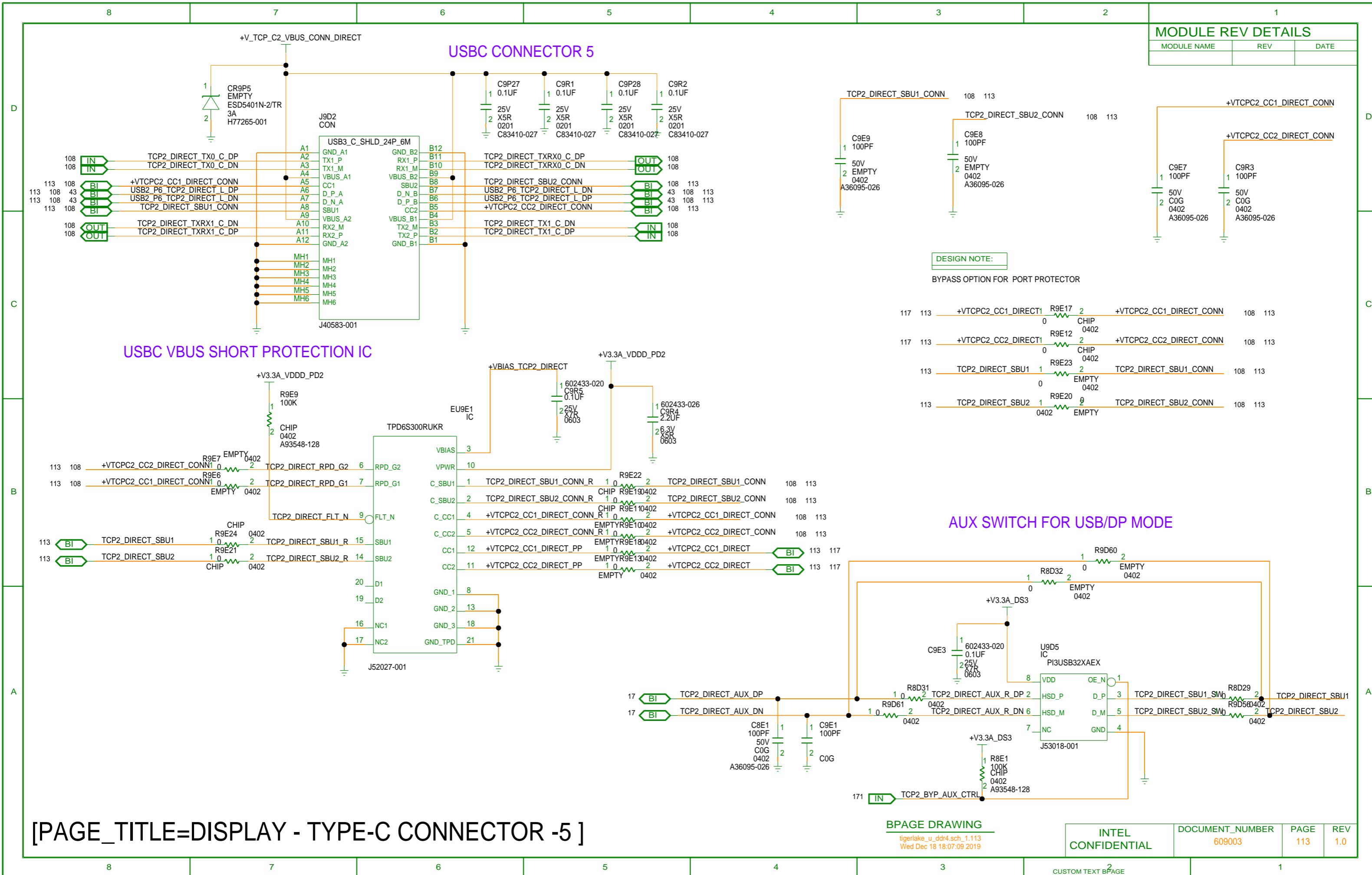


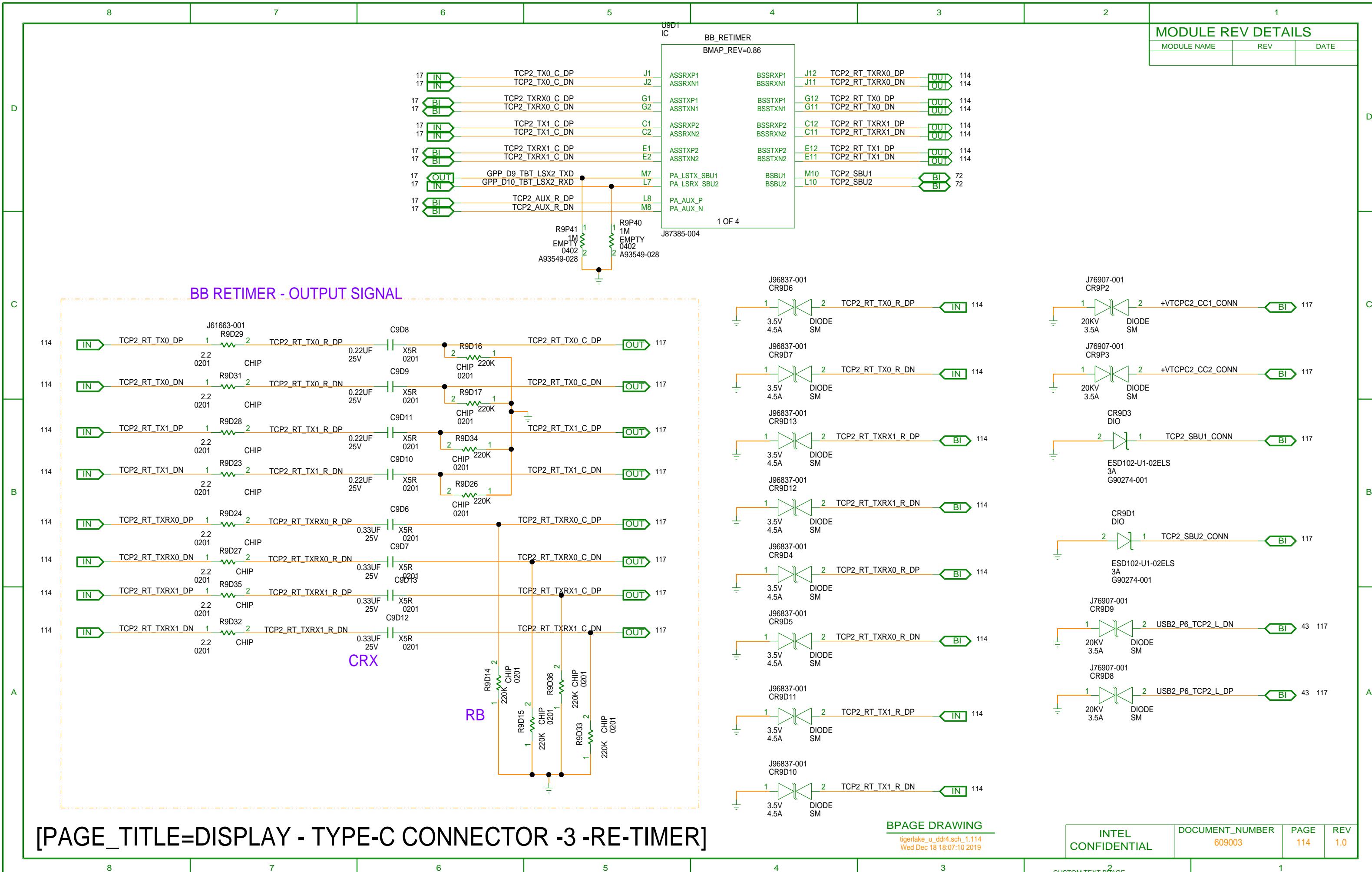


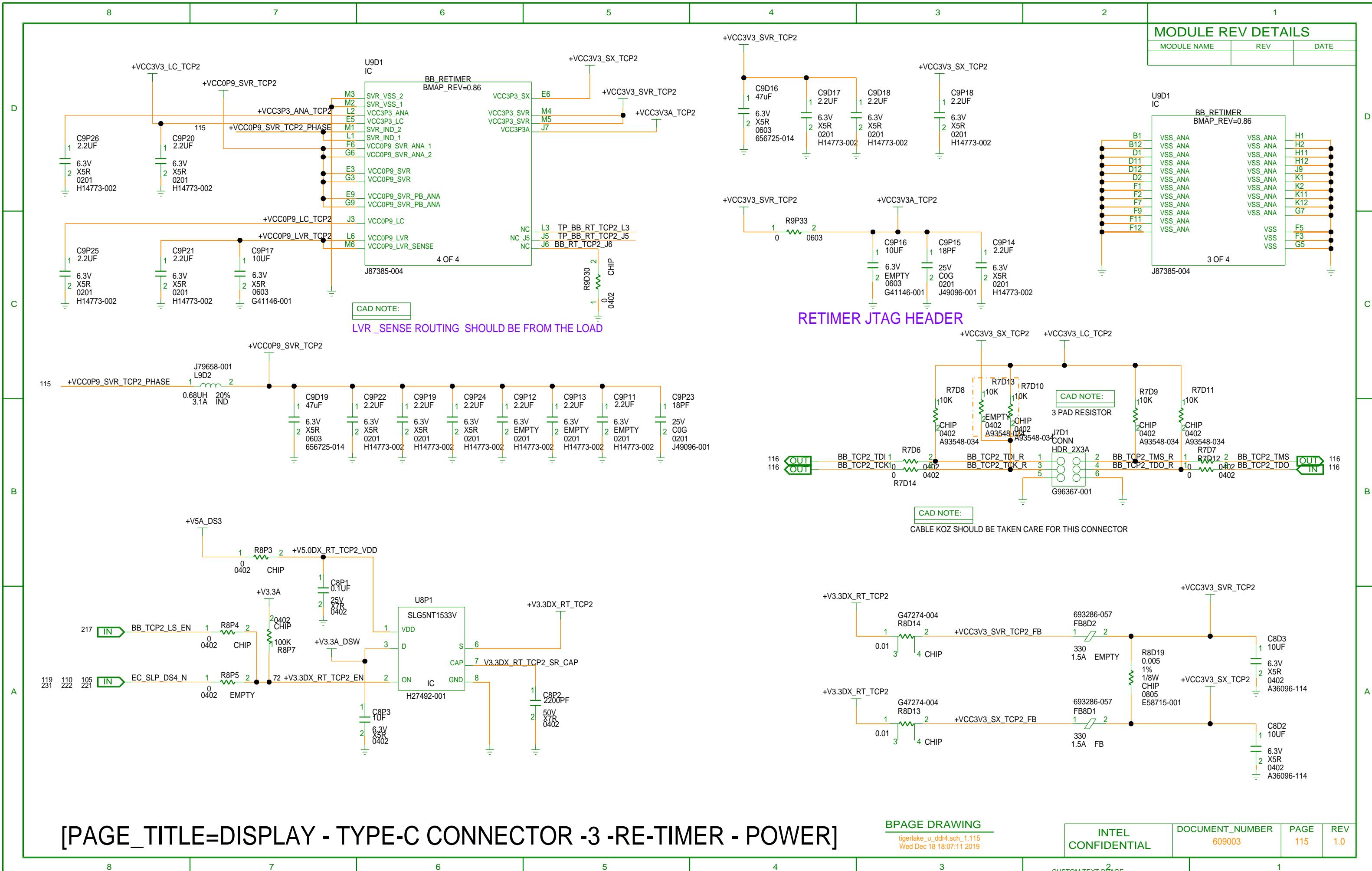


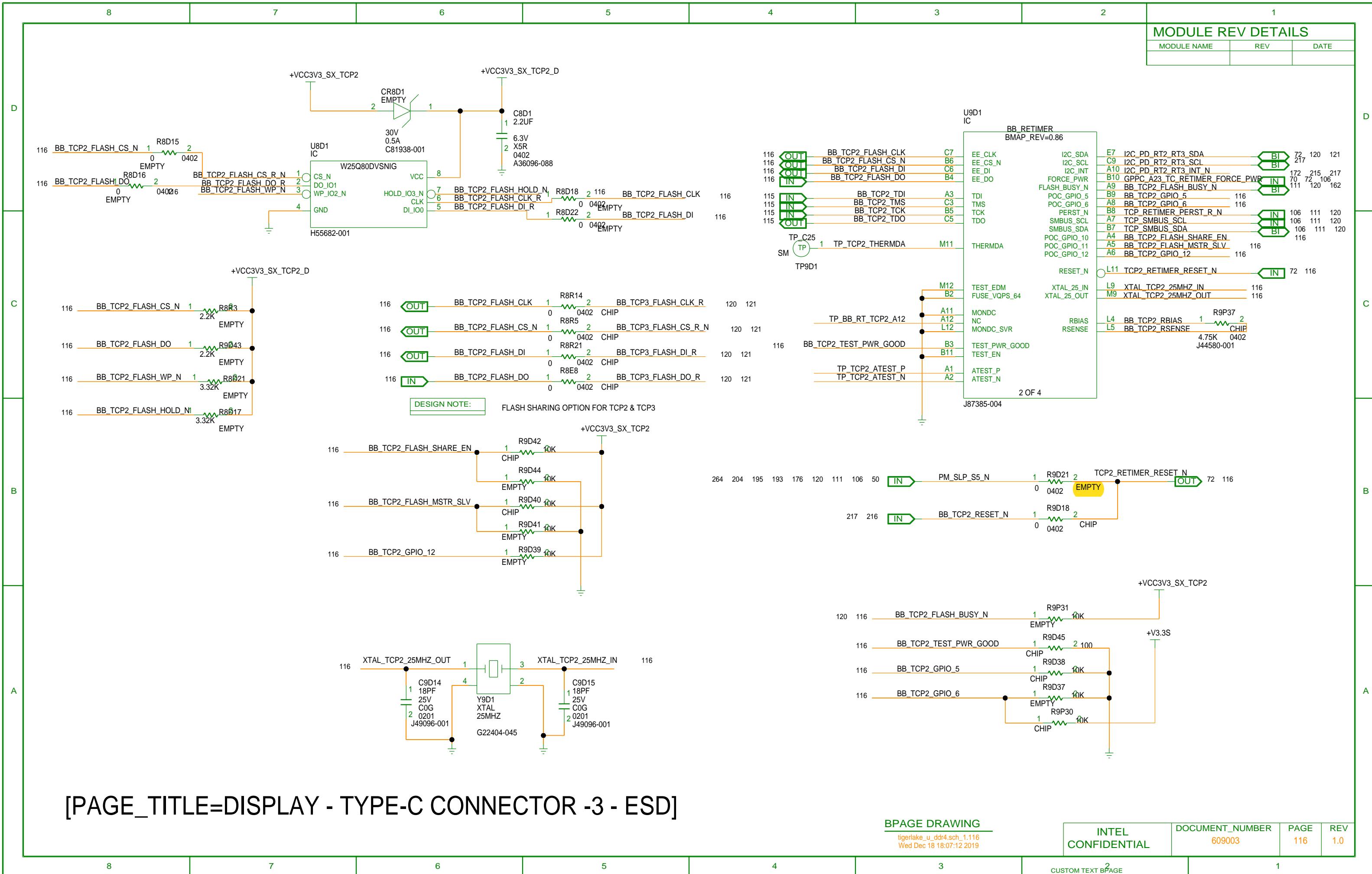


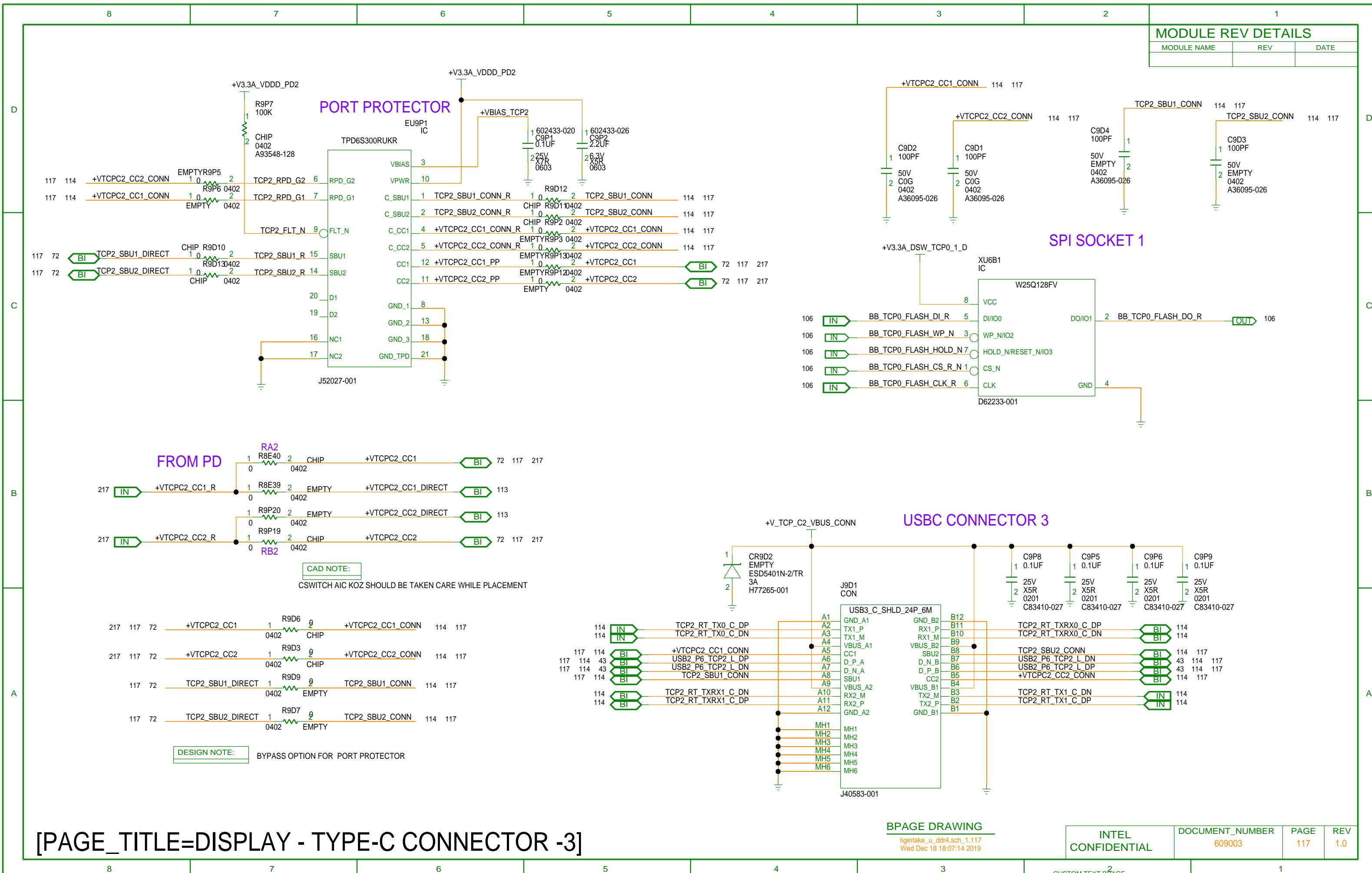


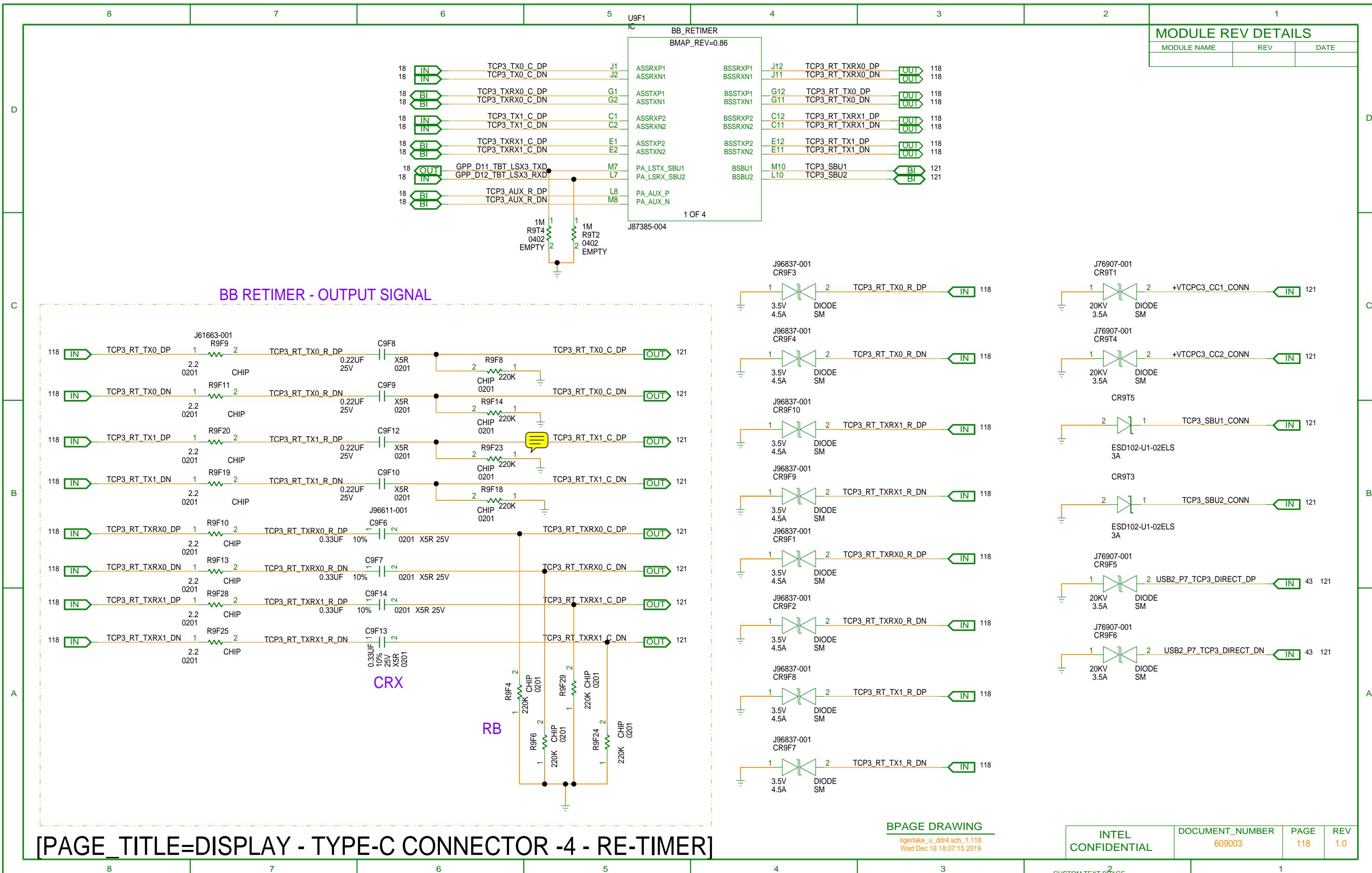


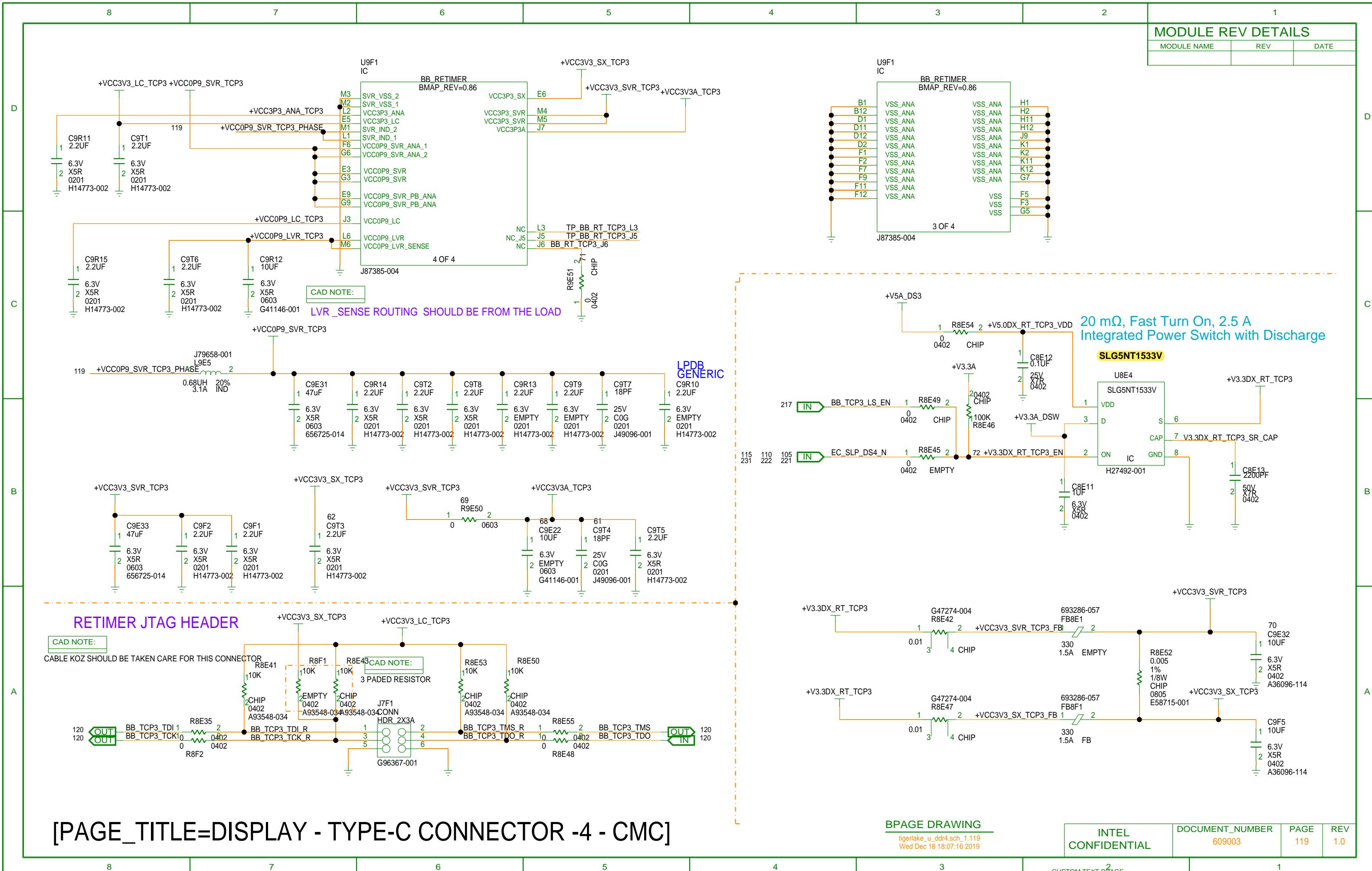


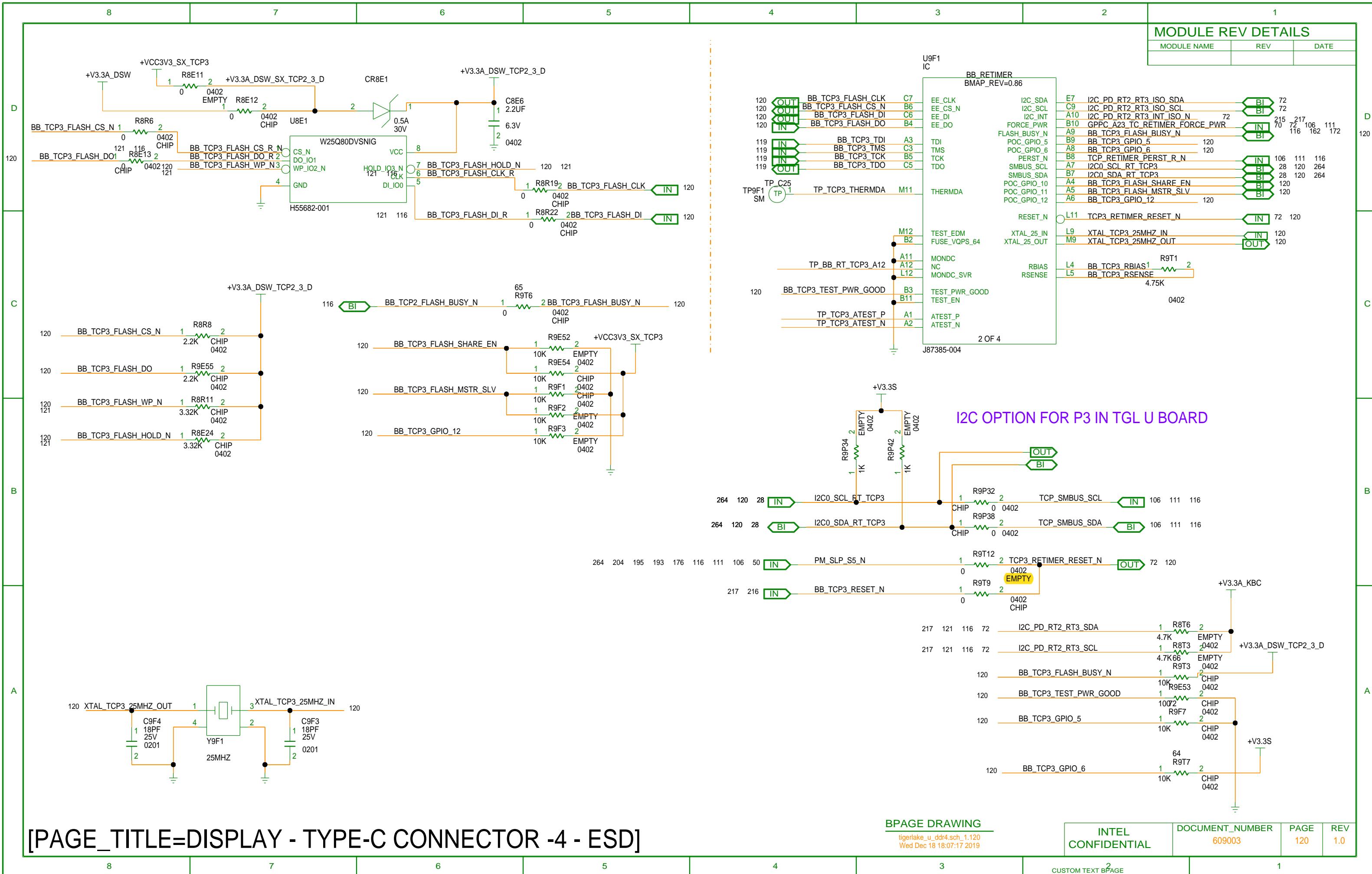


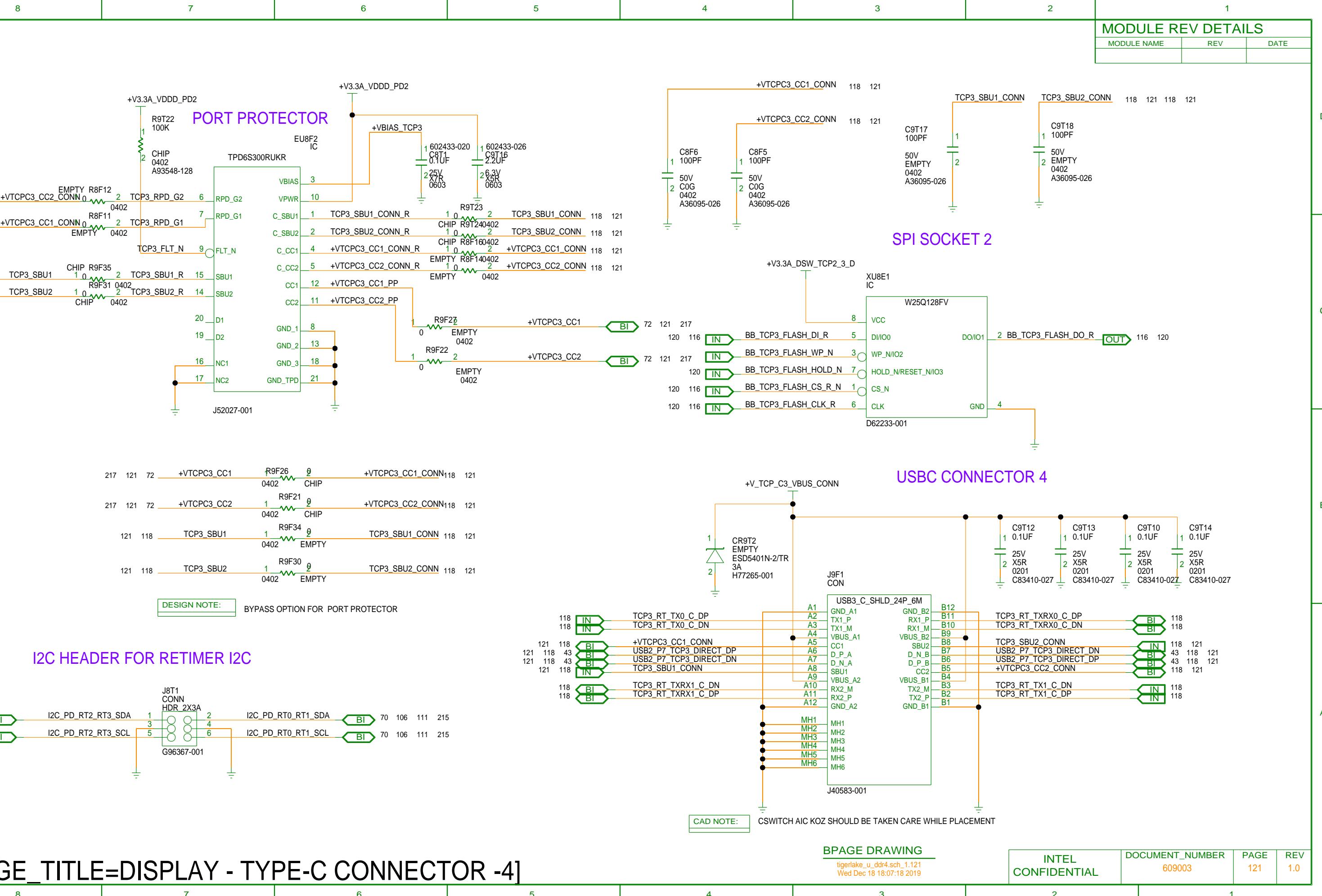


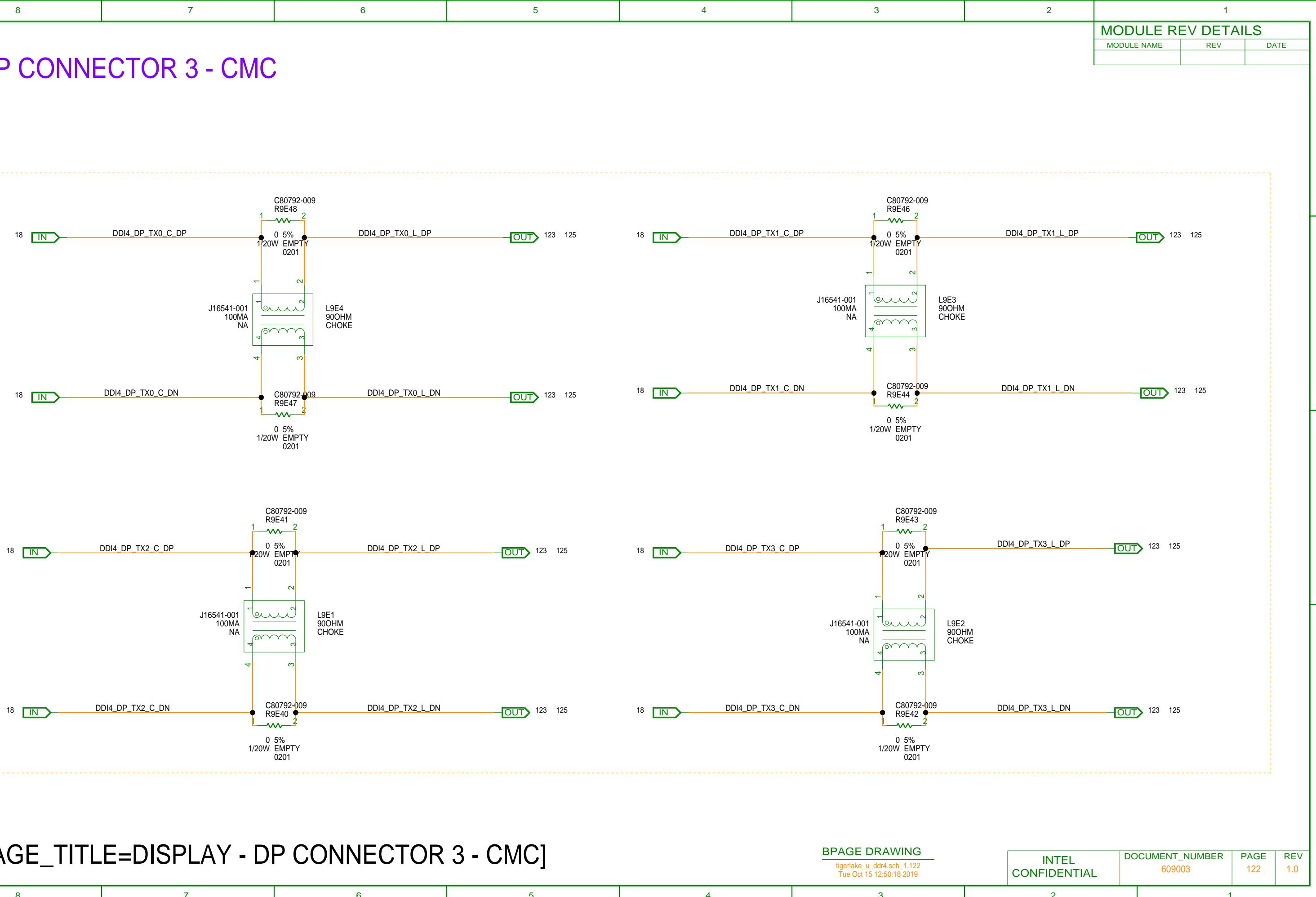








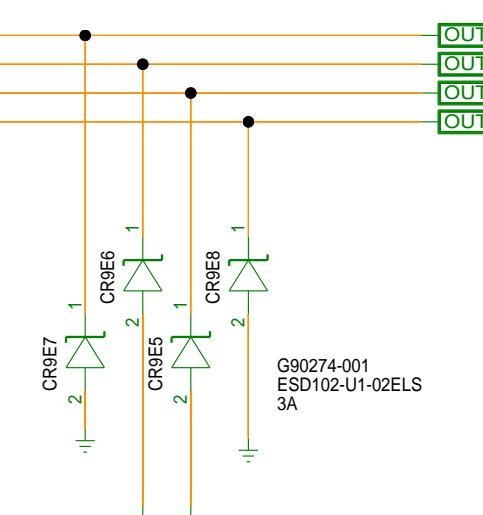
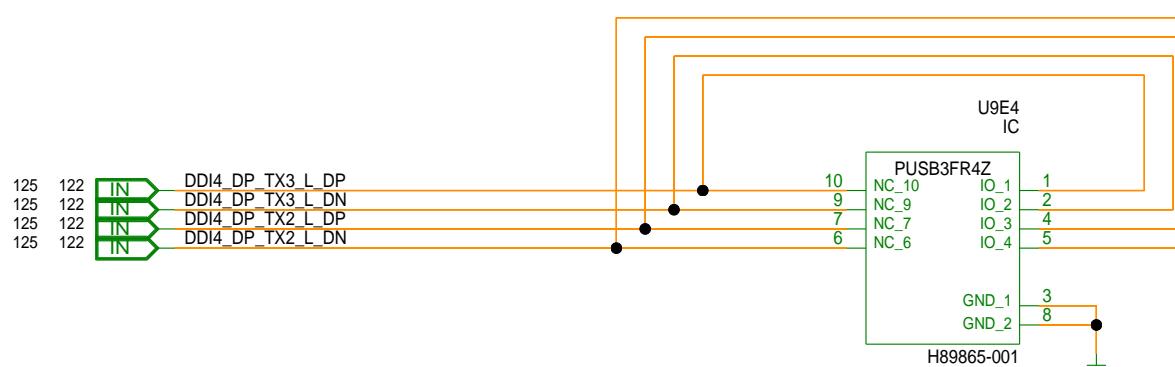
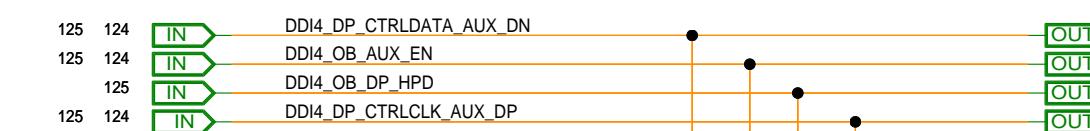
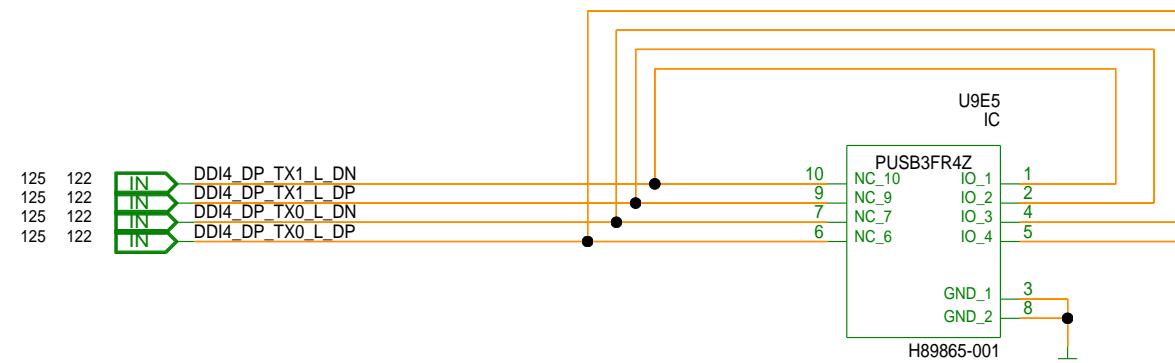




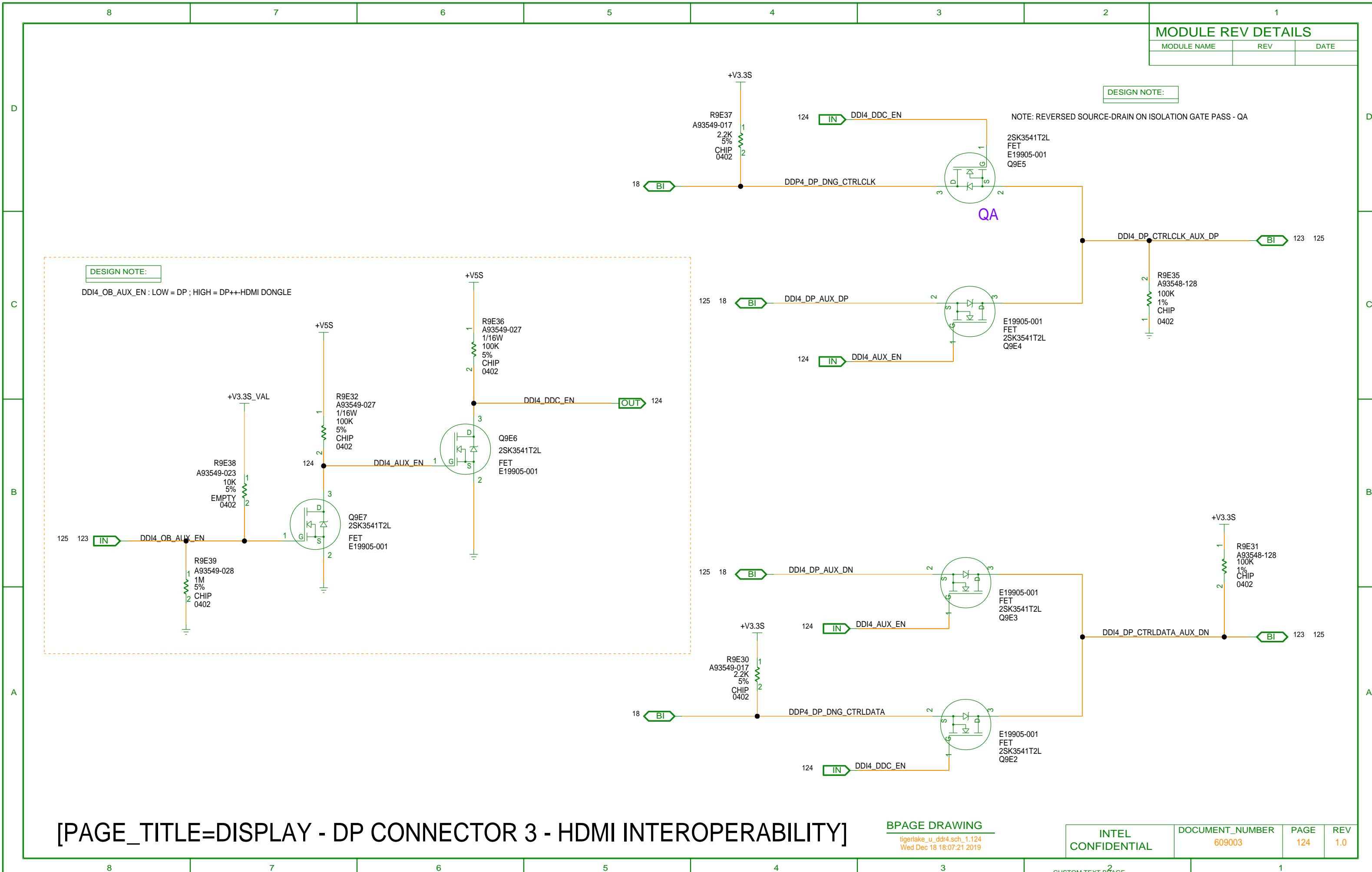
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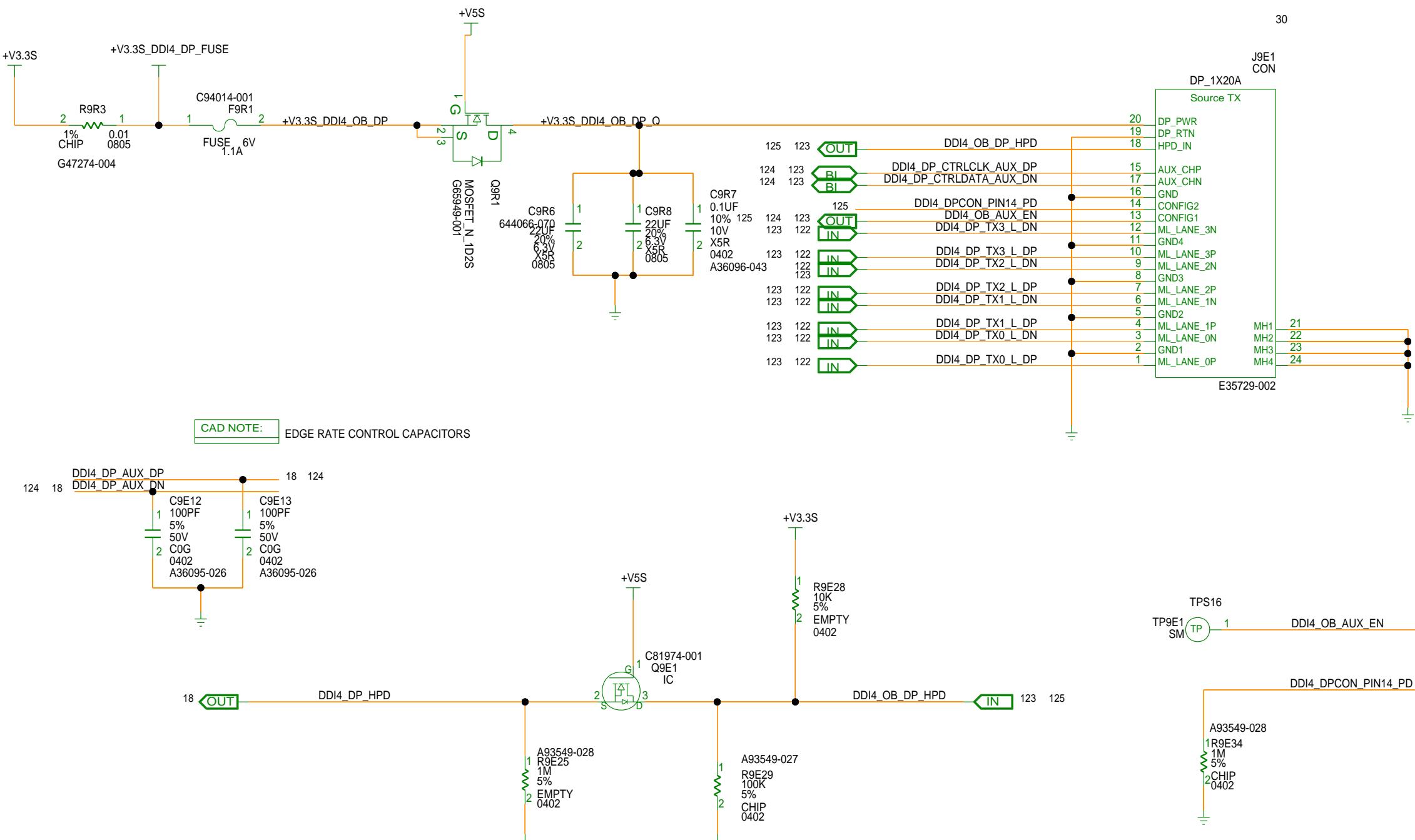


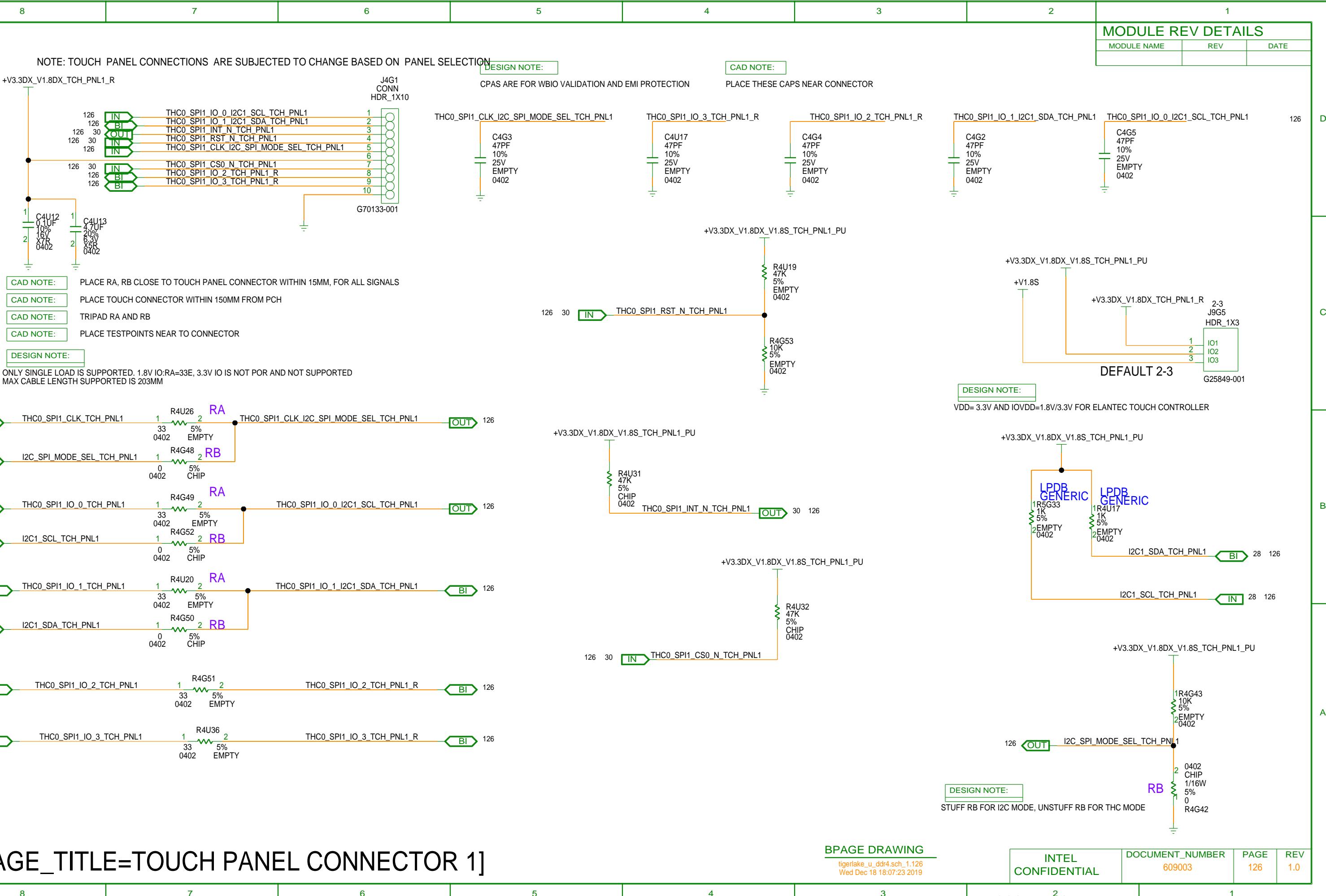
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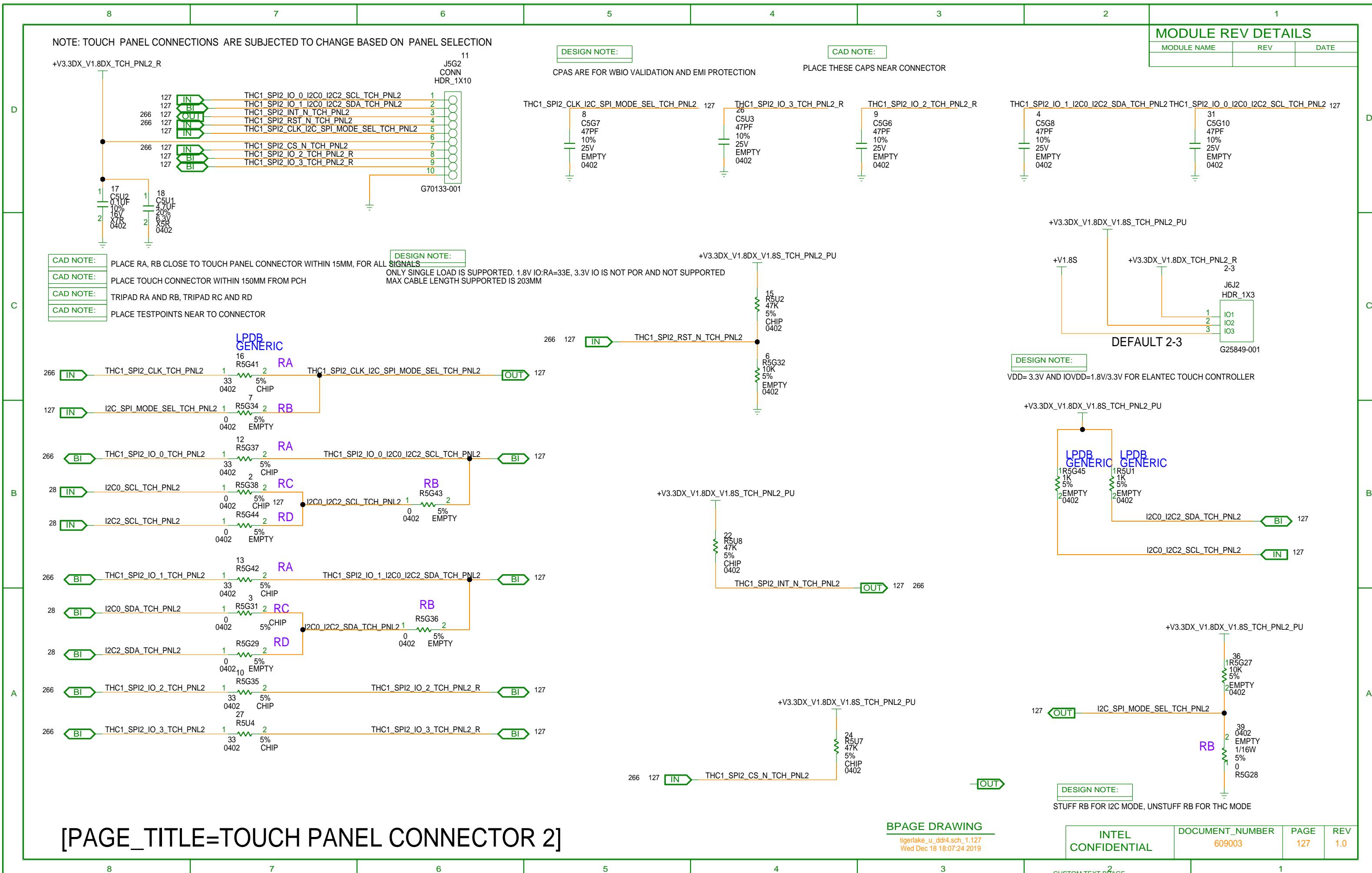


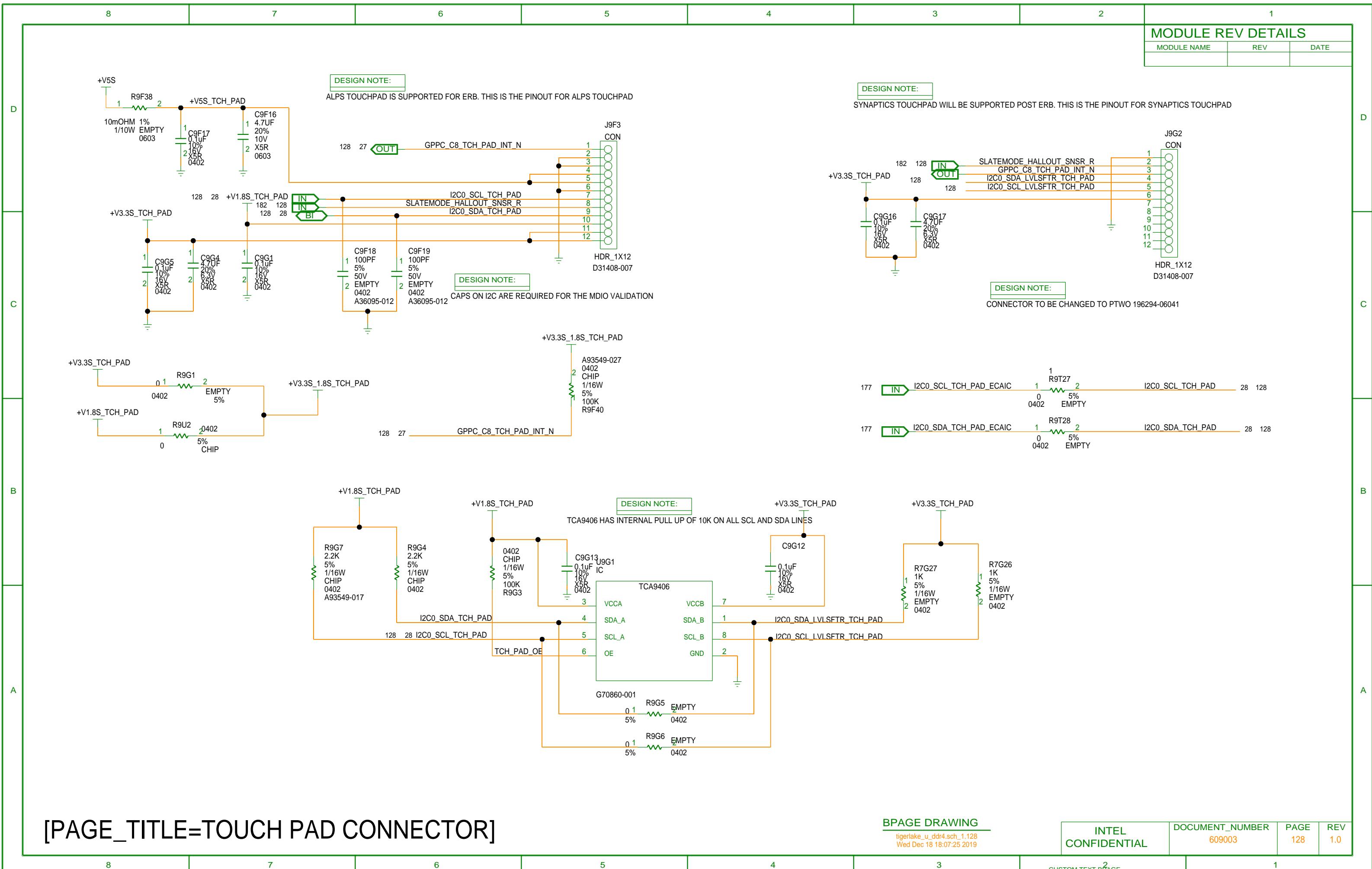
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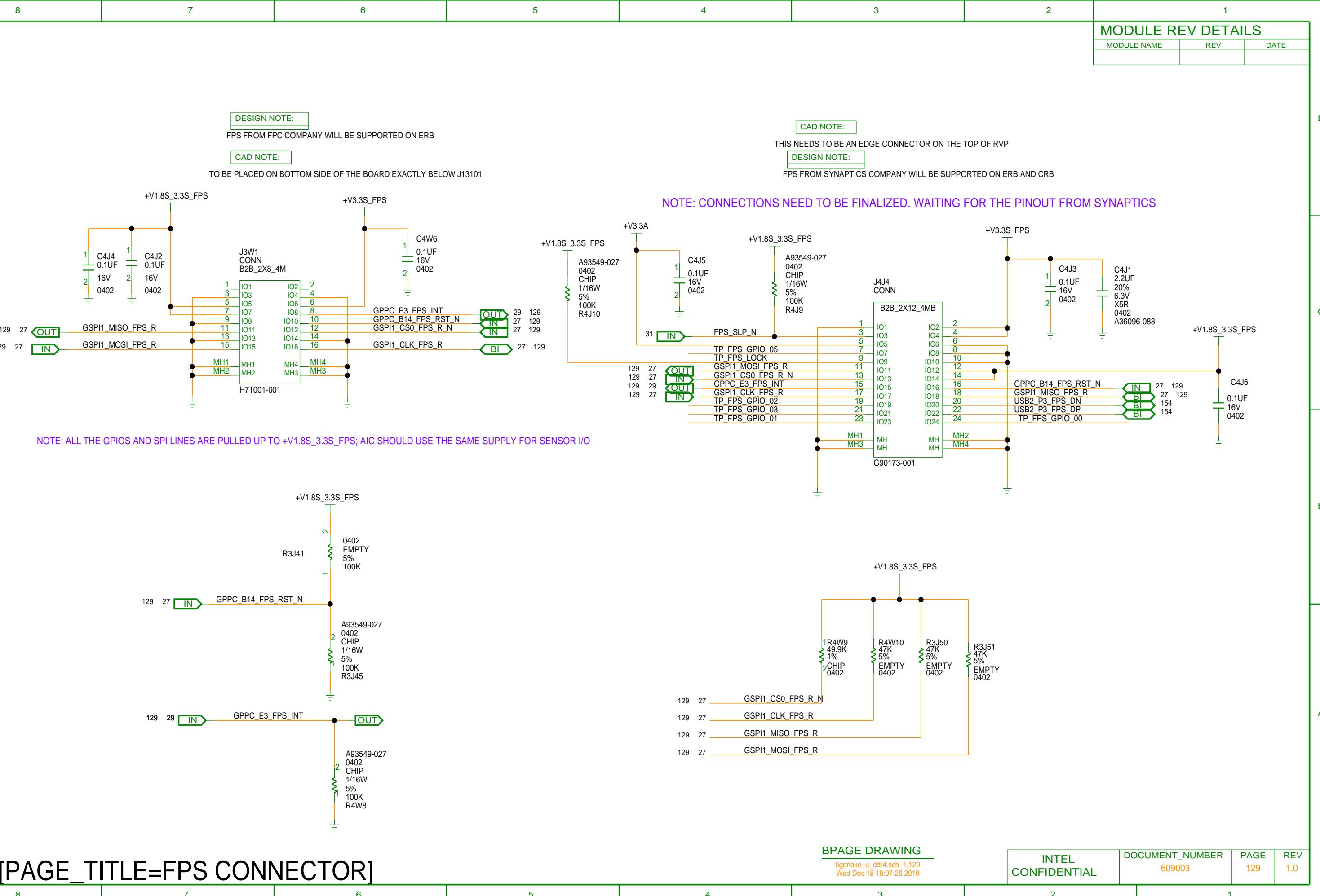
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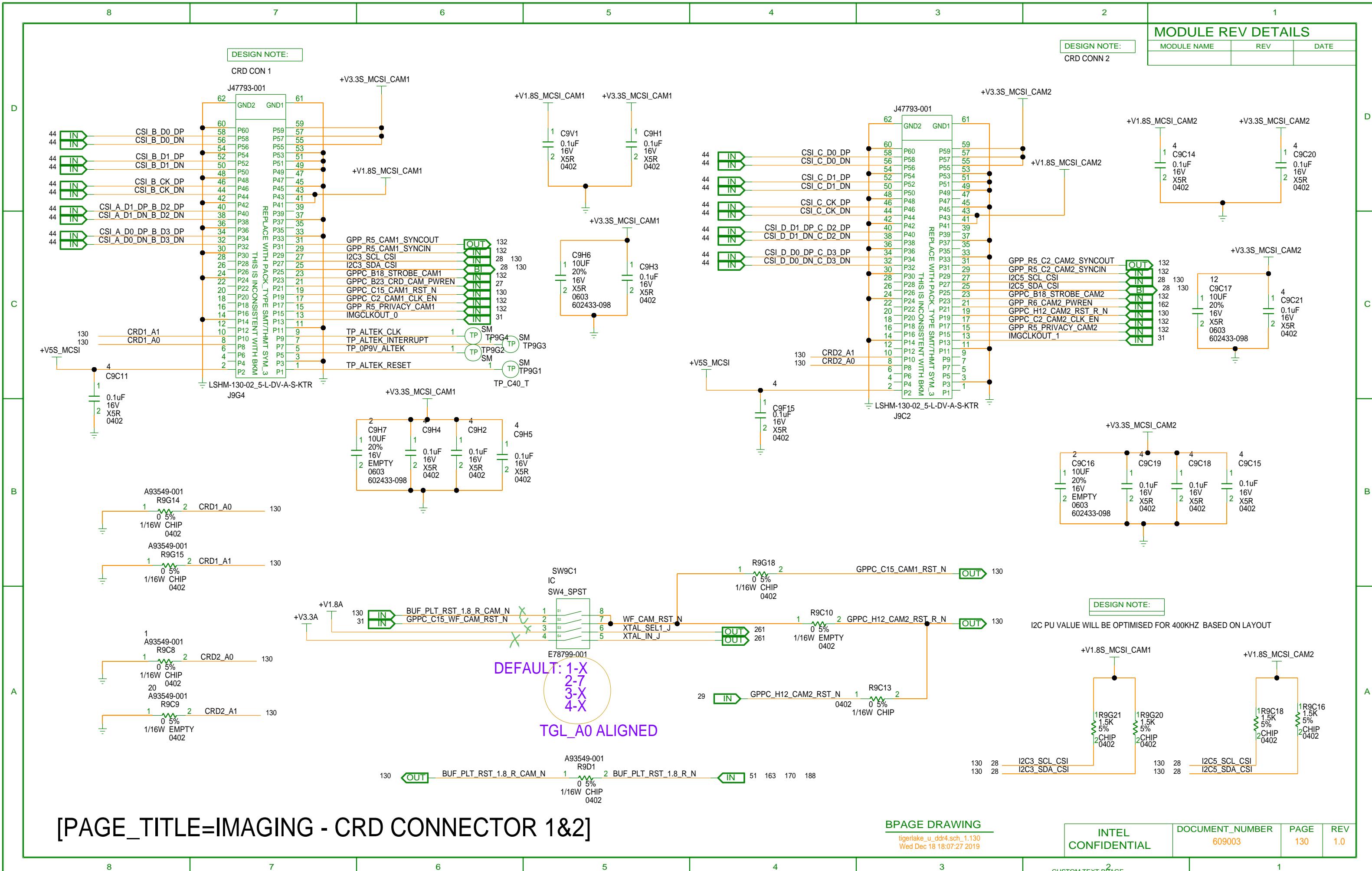


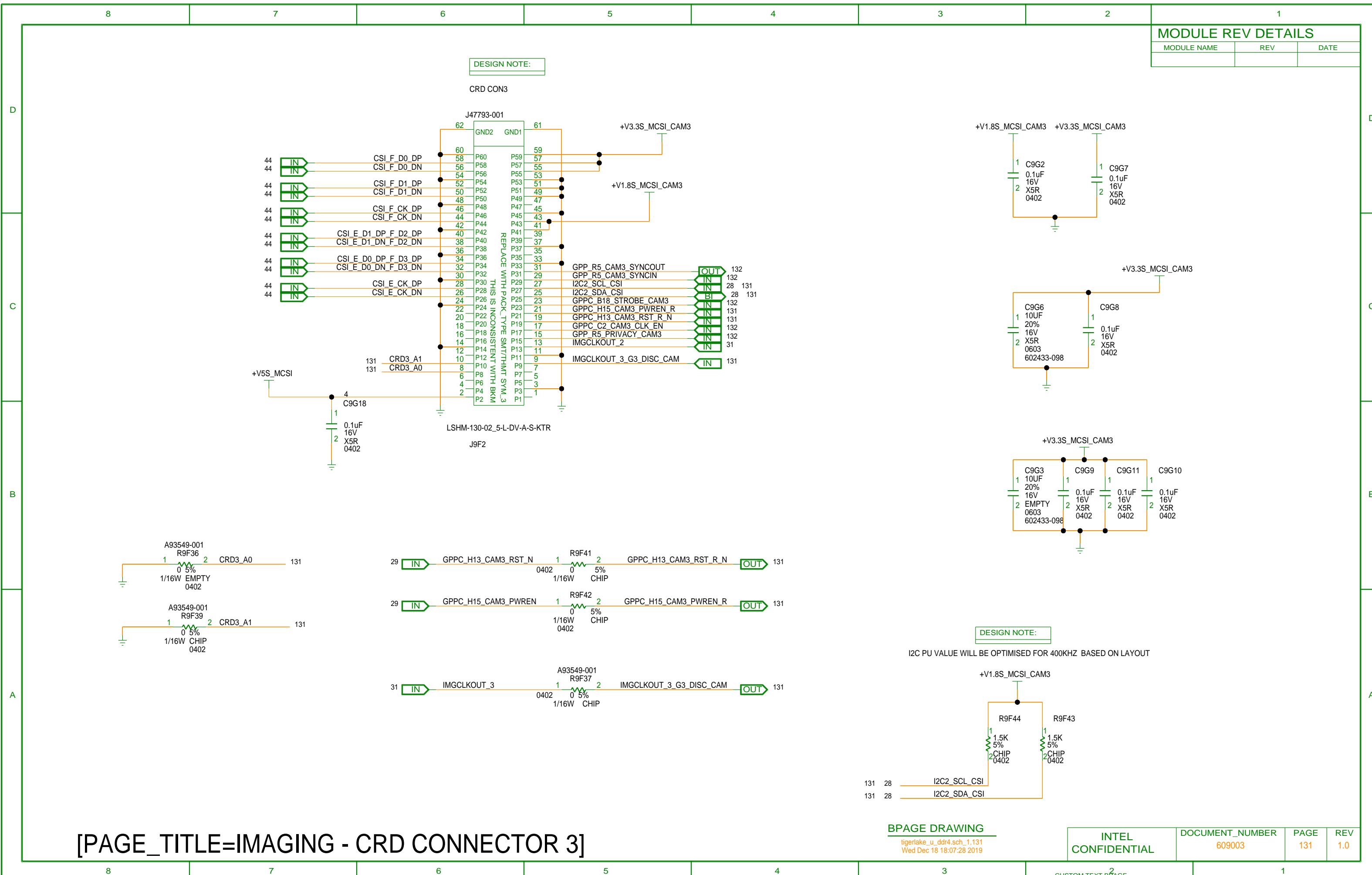


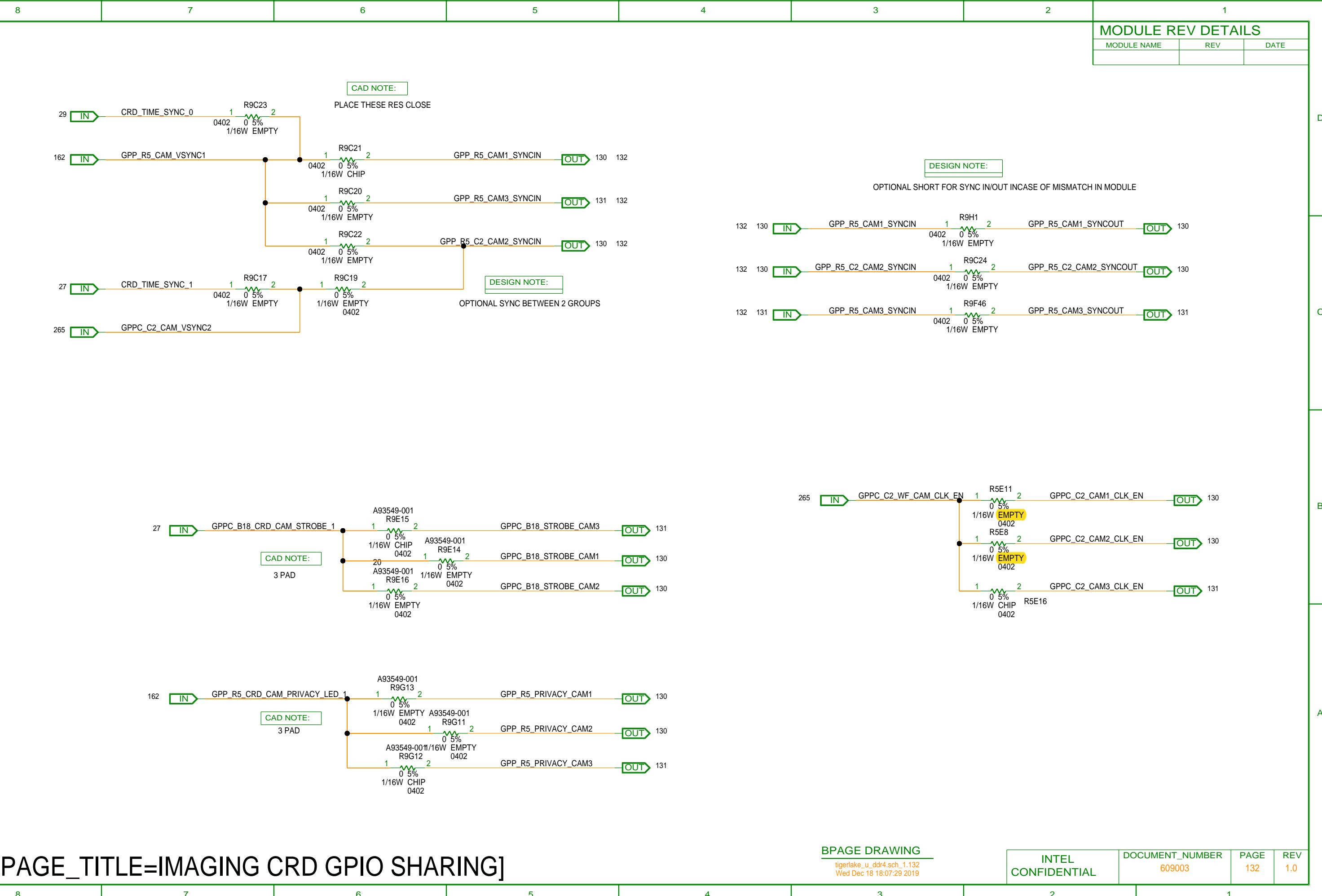












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**MODULE REV DETAILS**

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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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**MODULE REV DETAILS**

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**MODULE REV DETAILS**

MODULE NAME	REV	DATE

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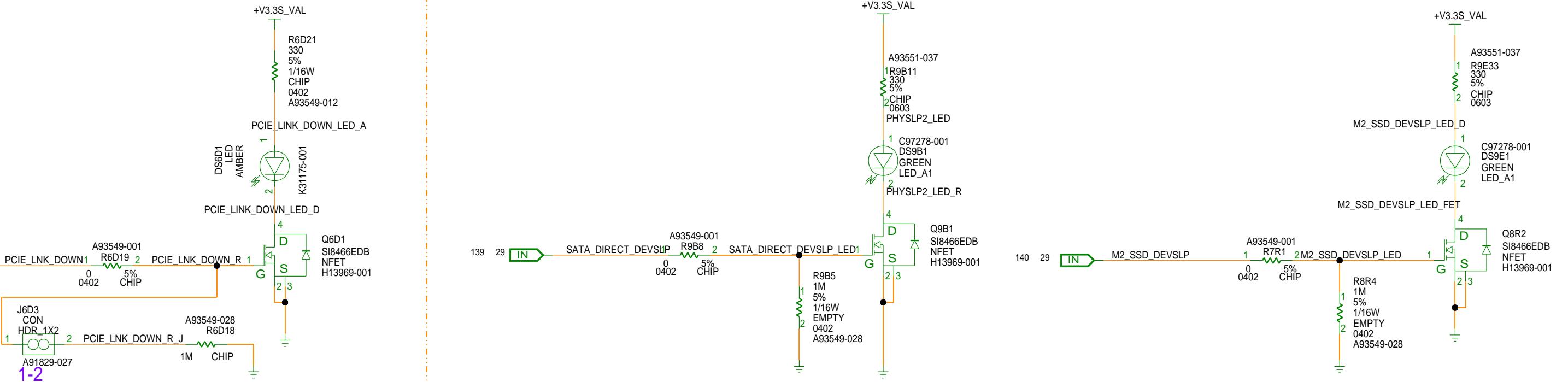
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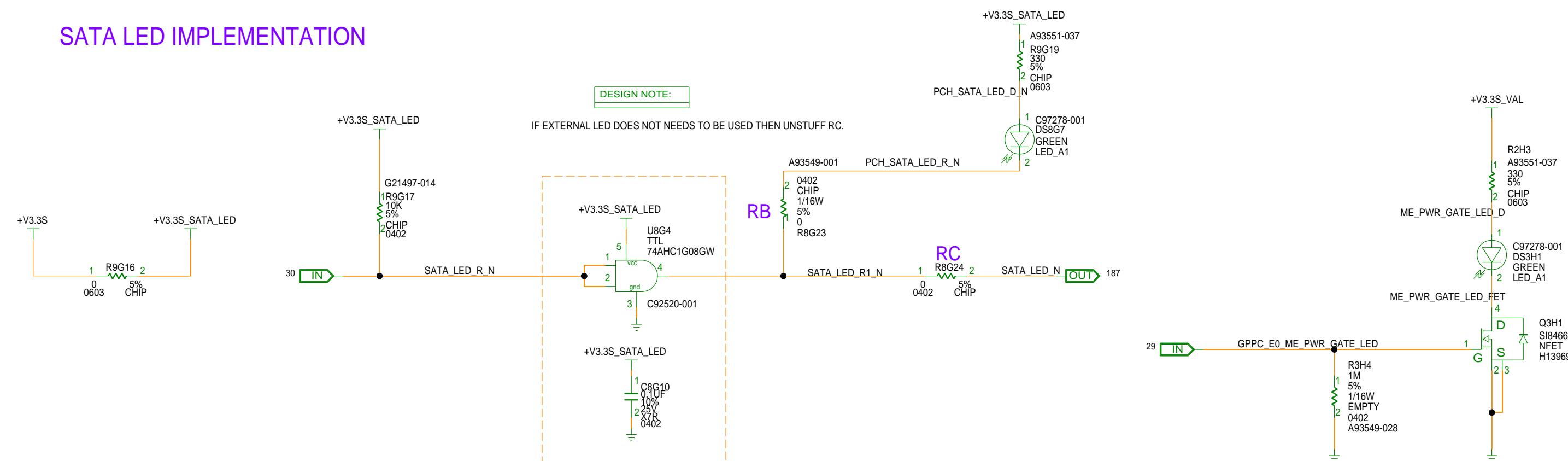
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## SATA DEV SLEEP LED

MODULE REV DETAILS		
MODULE NAME	REV	DATE



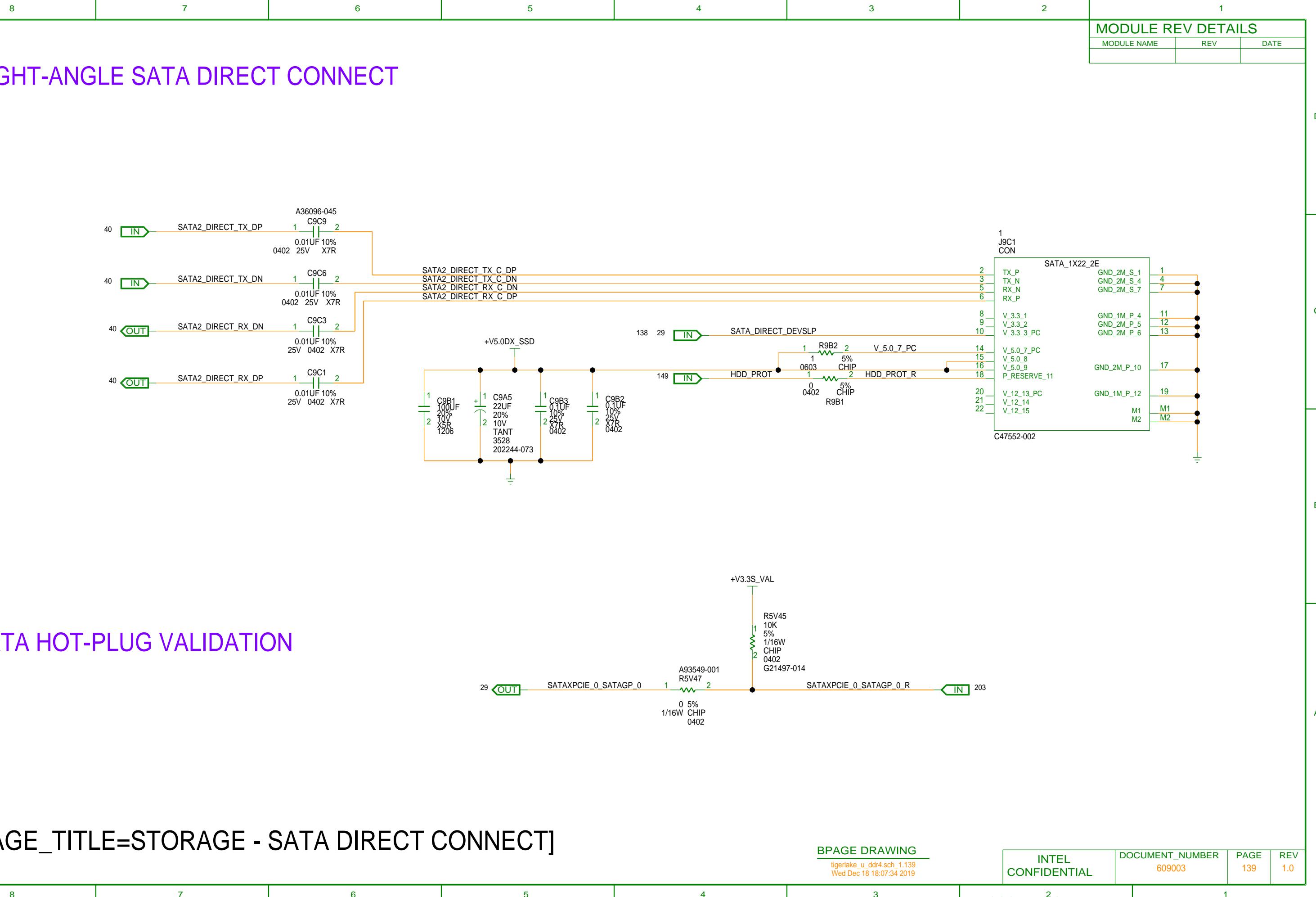
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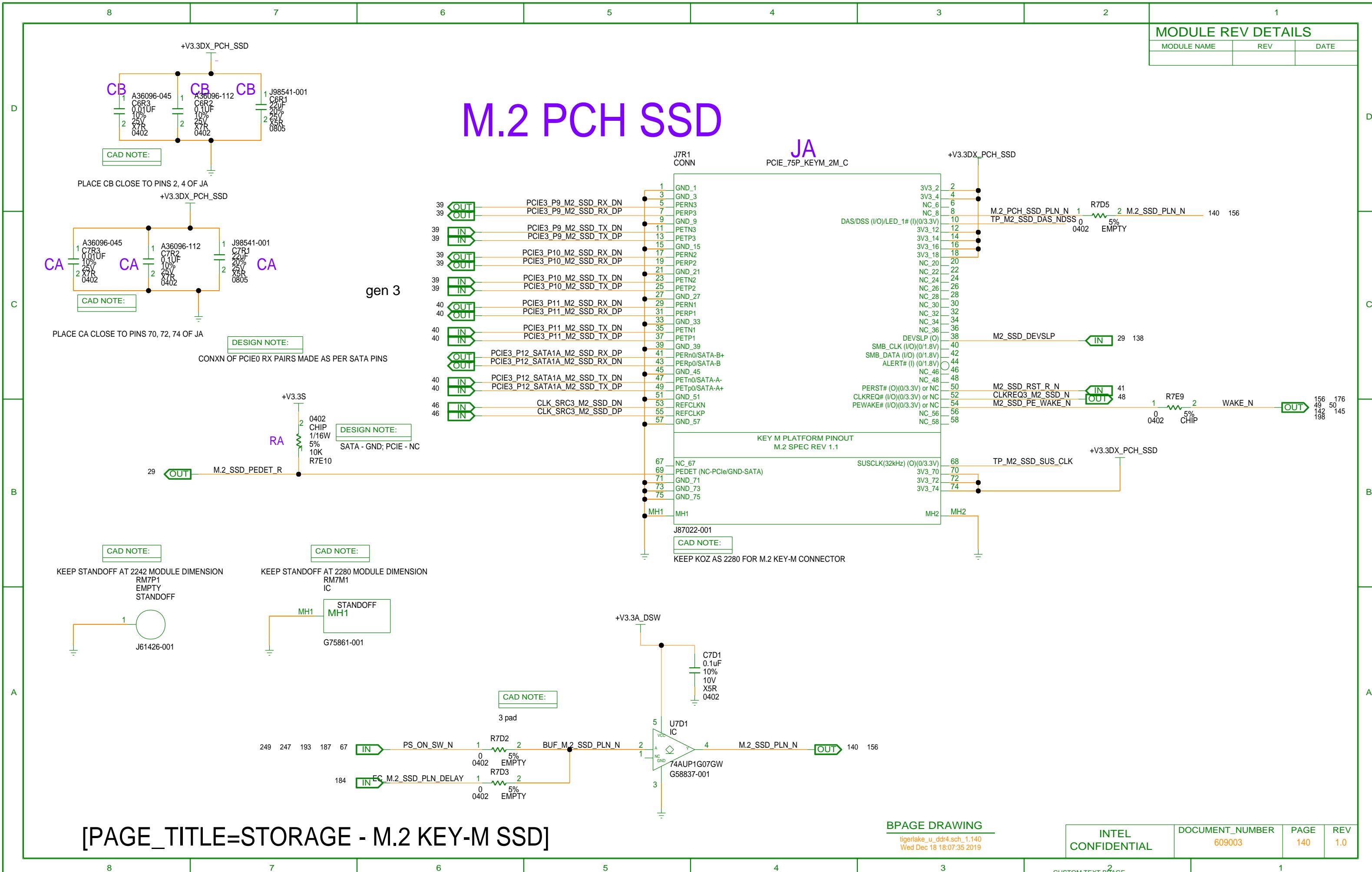


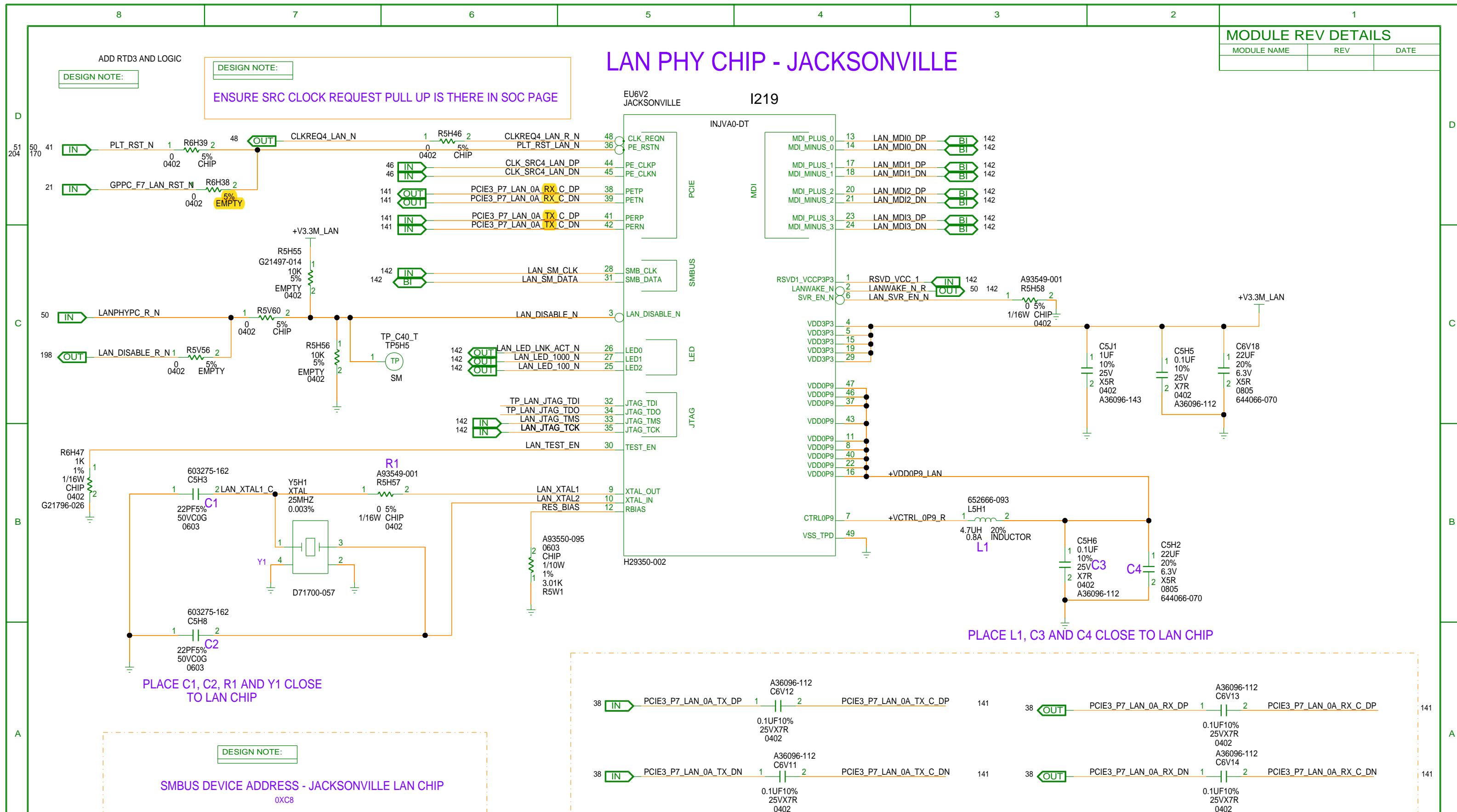
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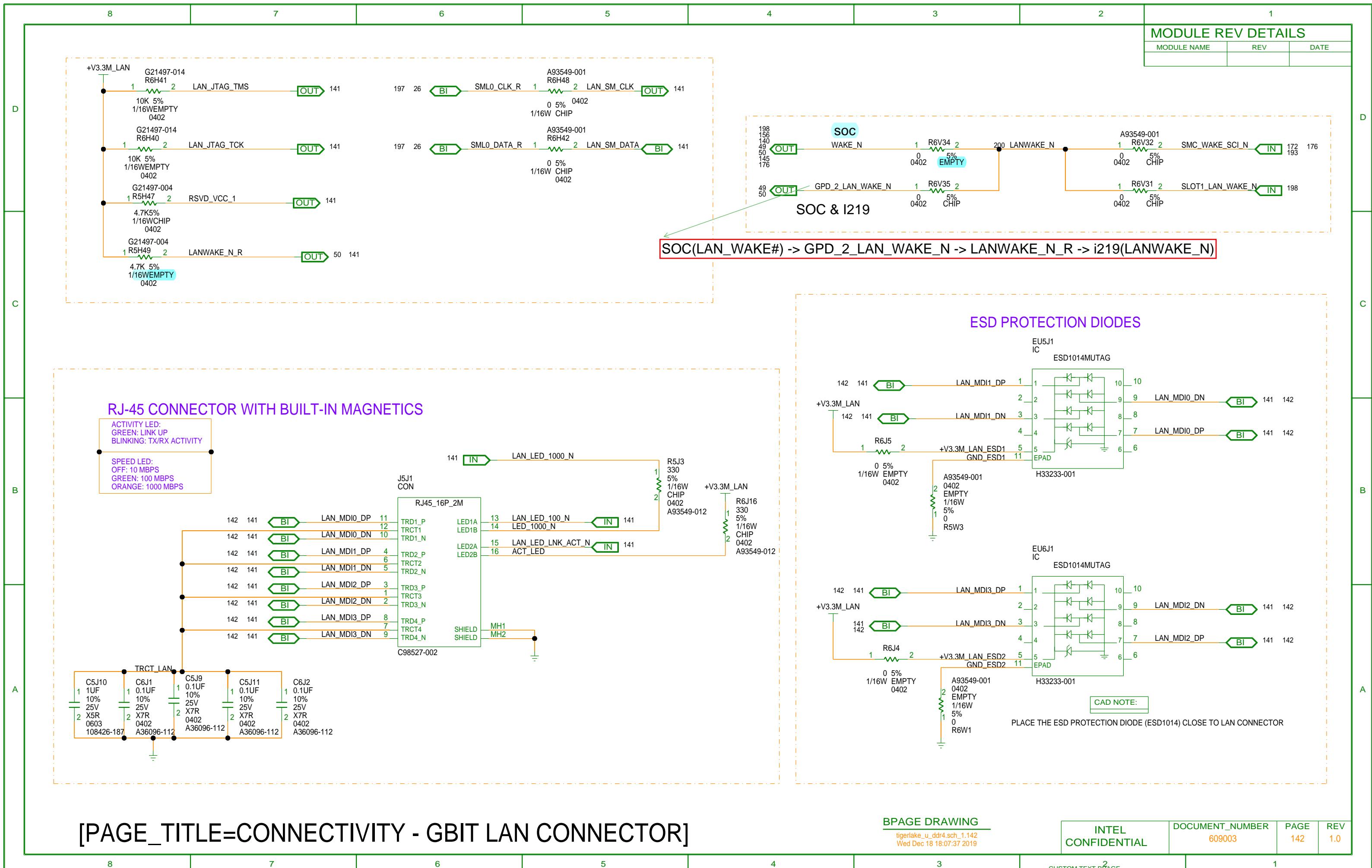
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Wed Dec 18 18:07:33 2019

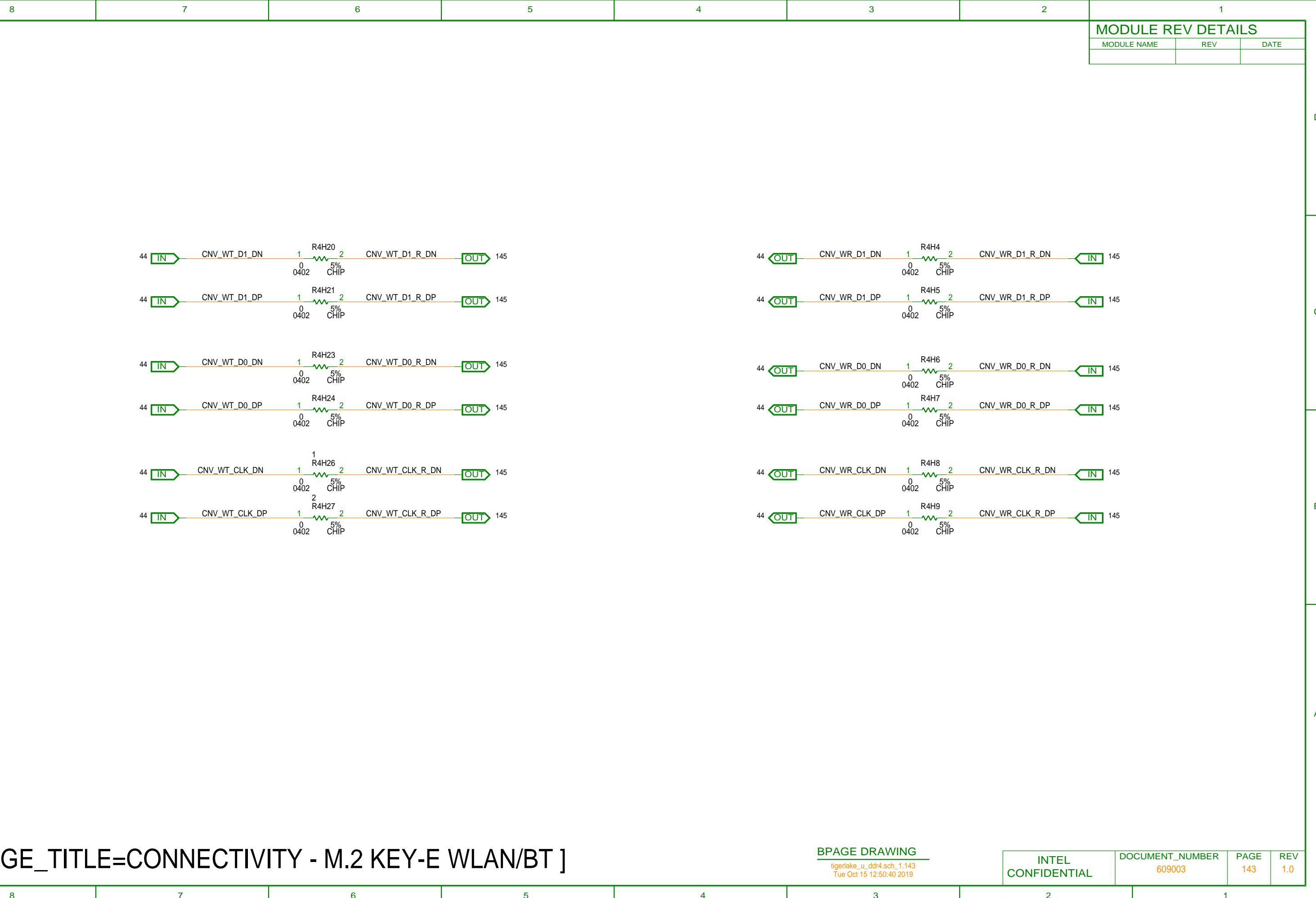
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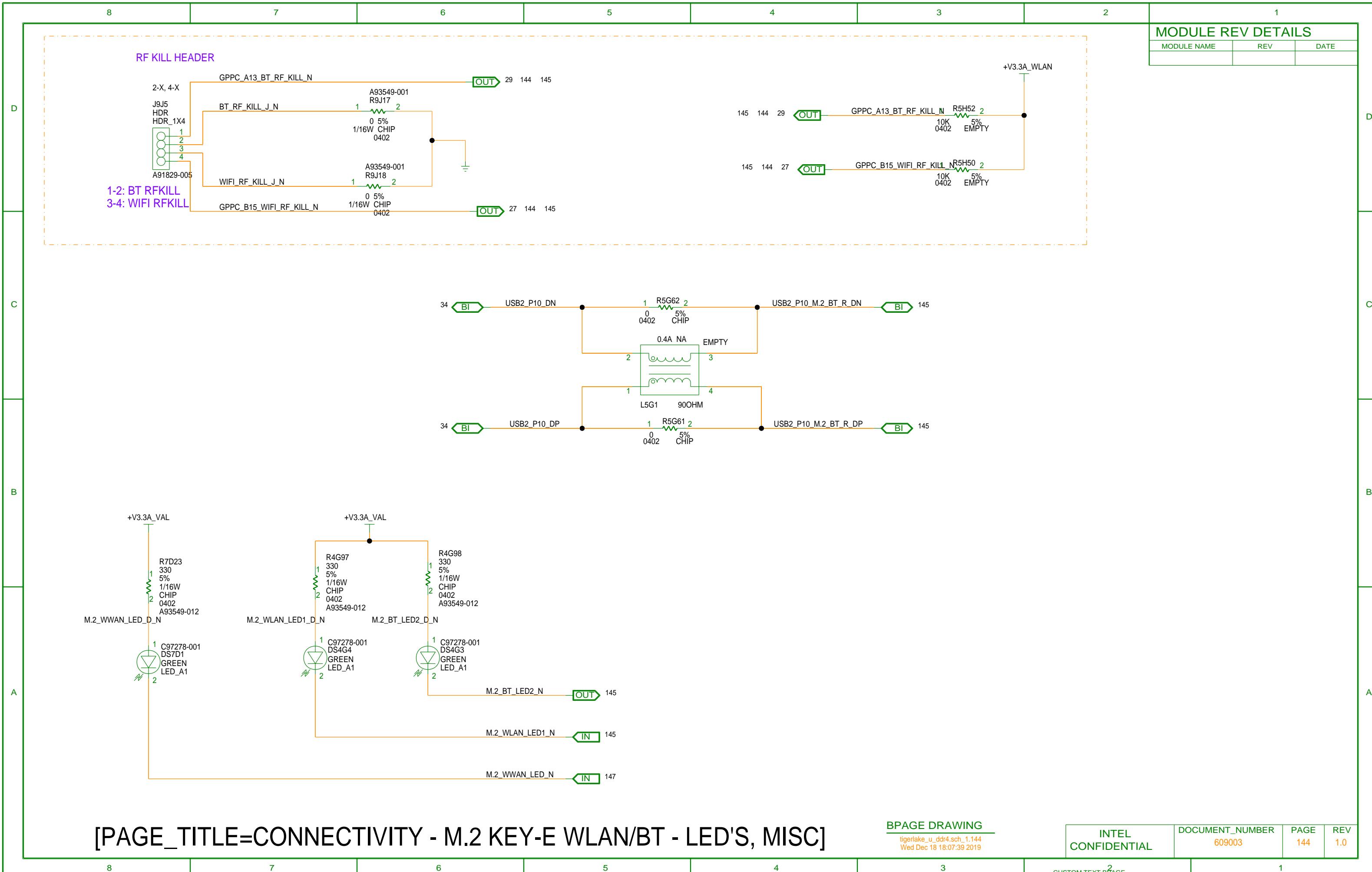










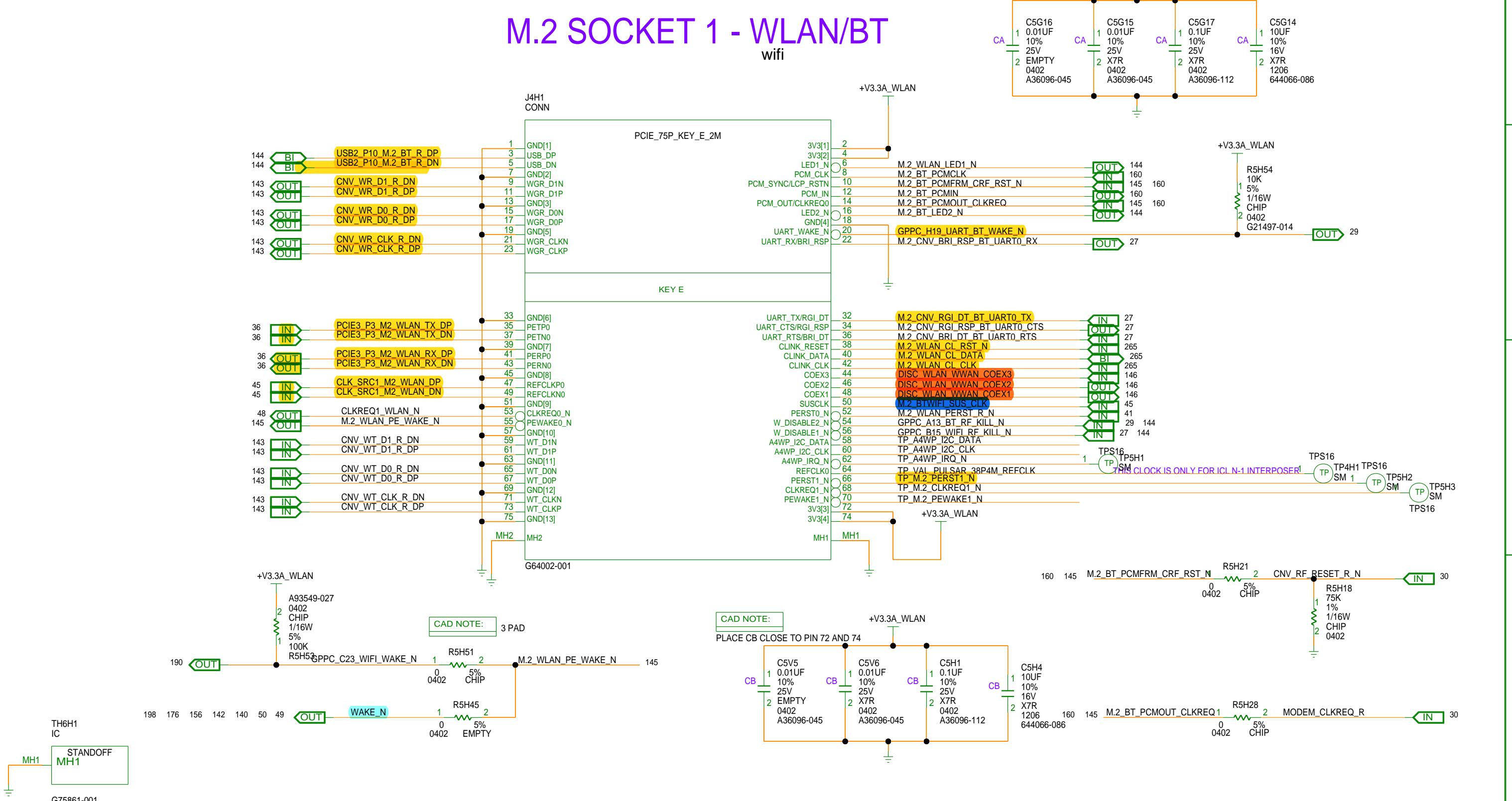


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MODULE REV DETAILS		
MODULE NAME	REV	DATE

## M.2 SOCKET 1 - WLAN/BT

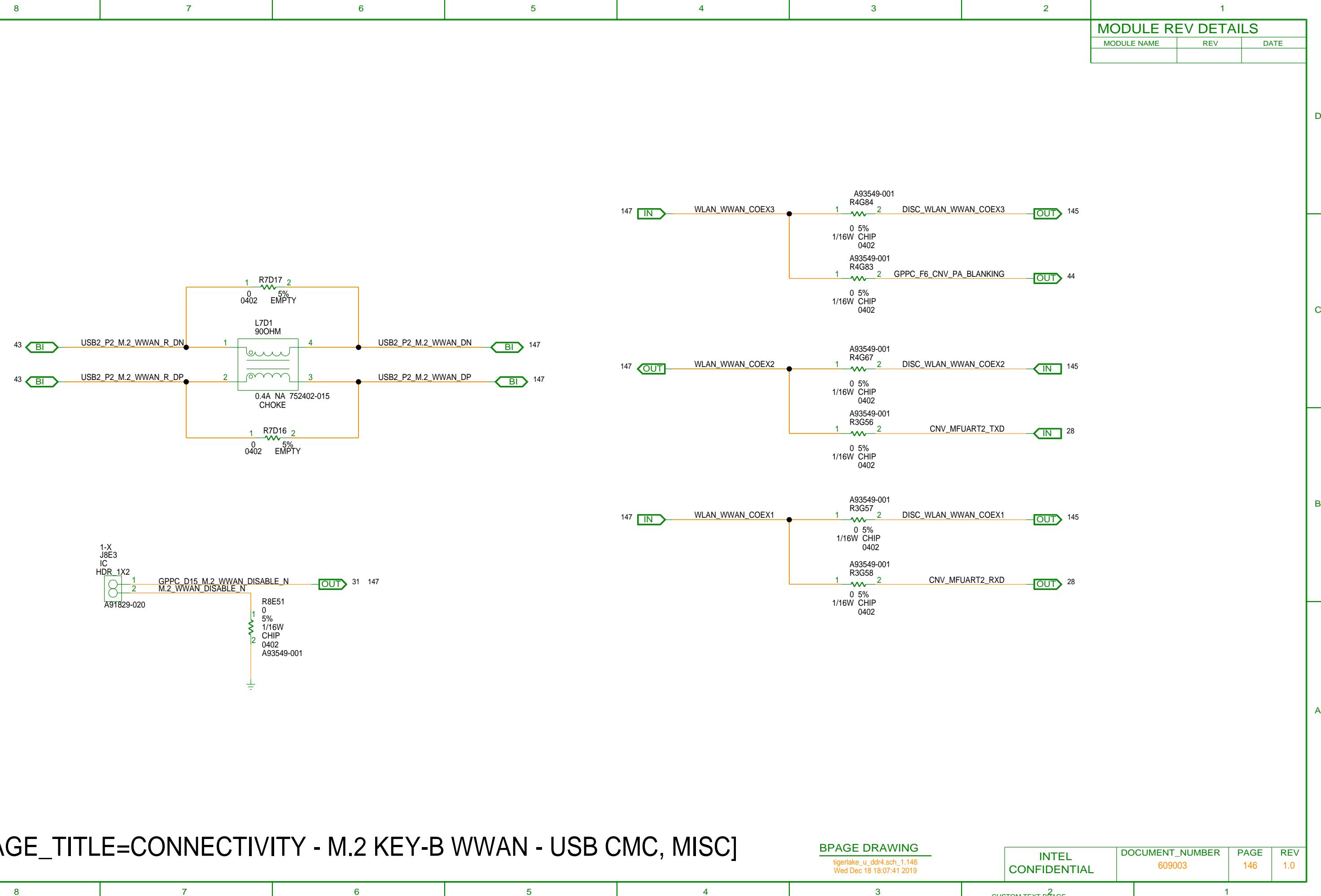
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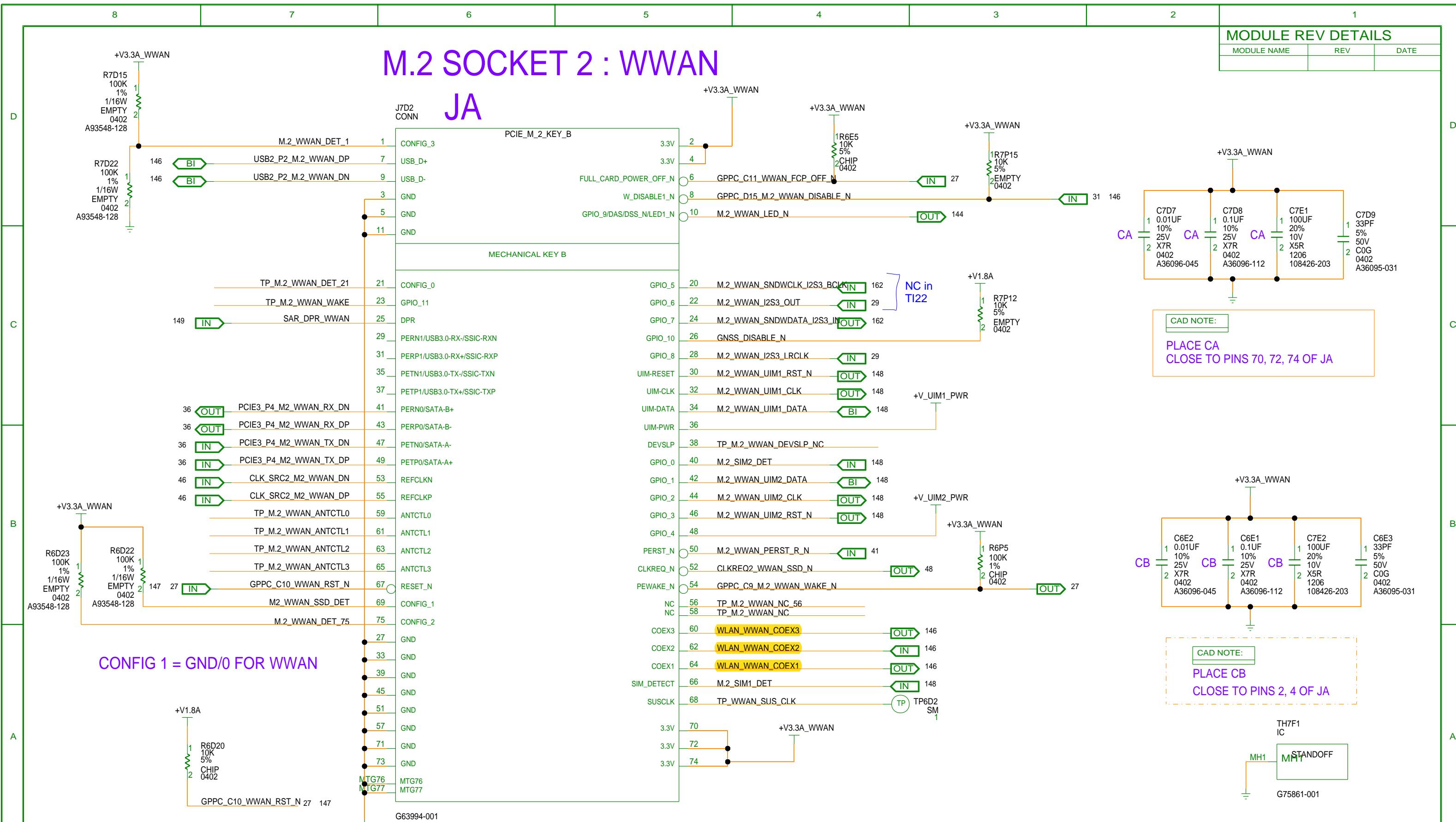


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INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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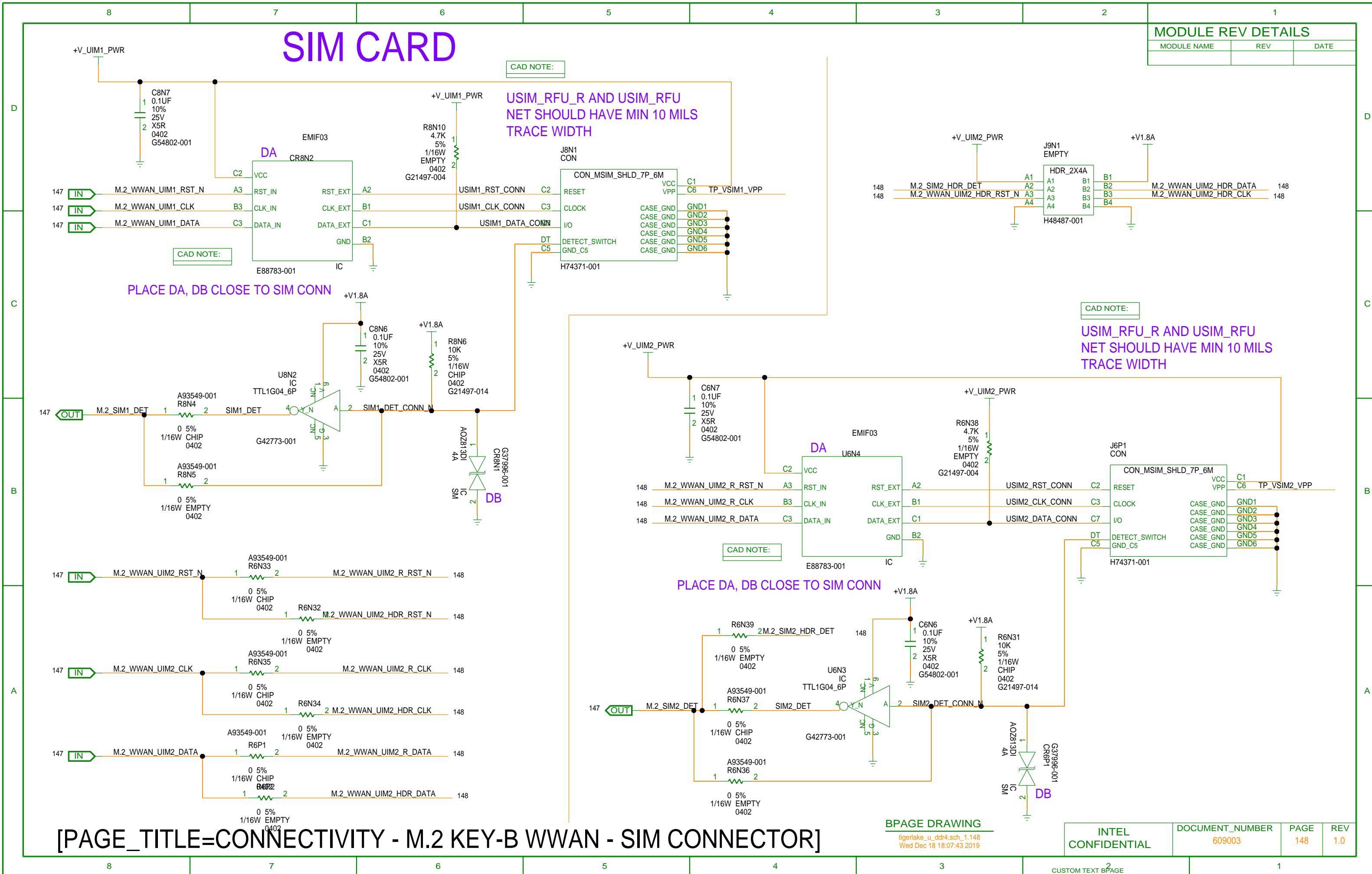
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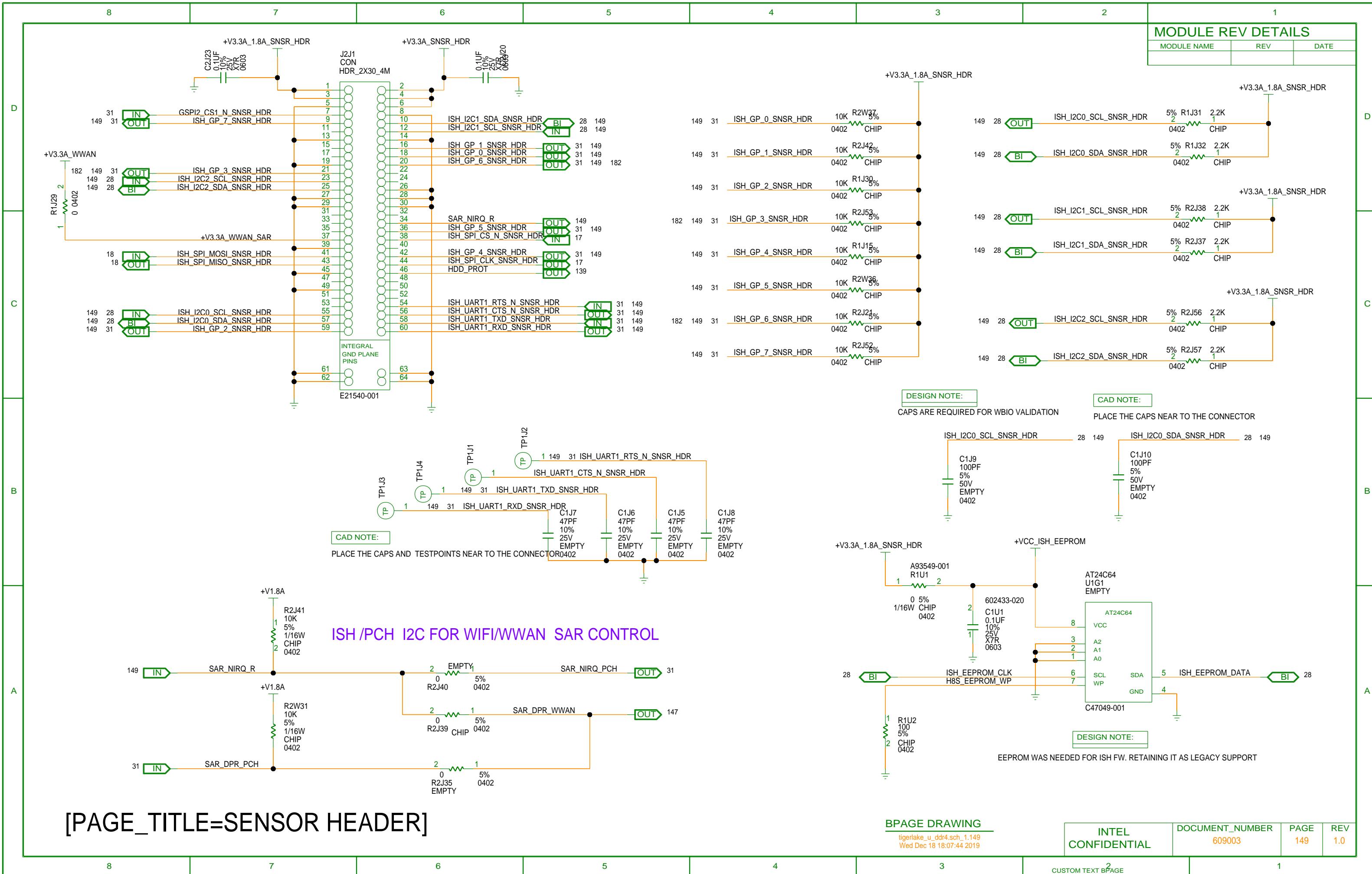
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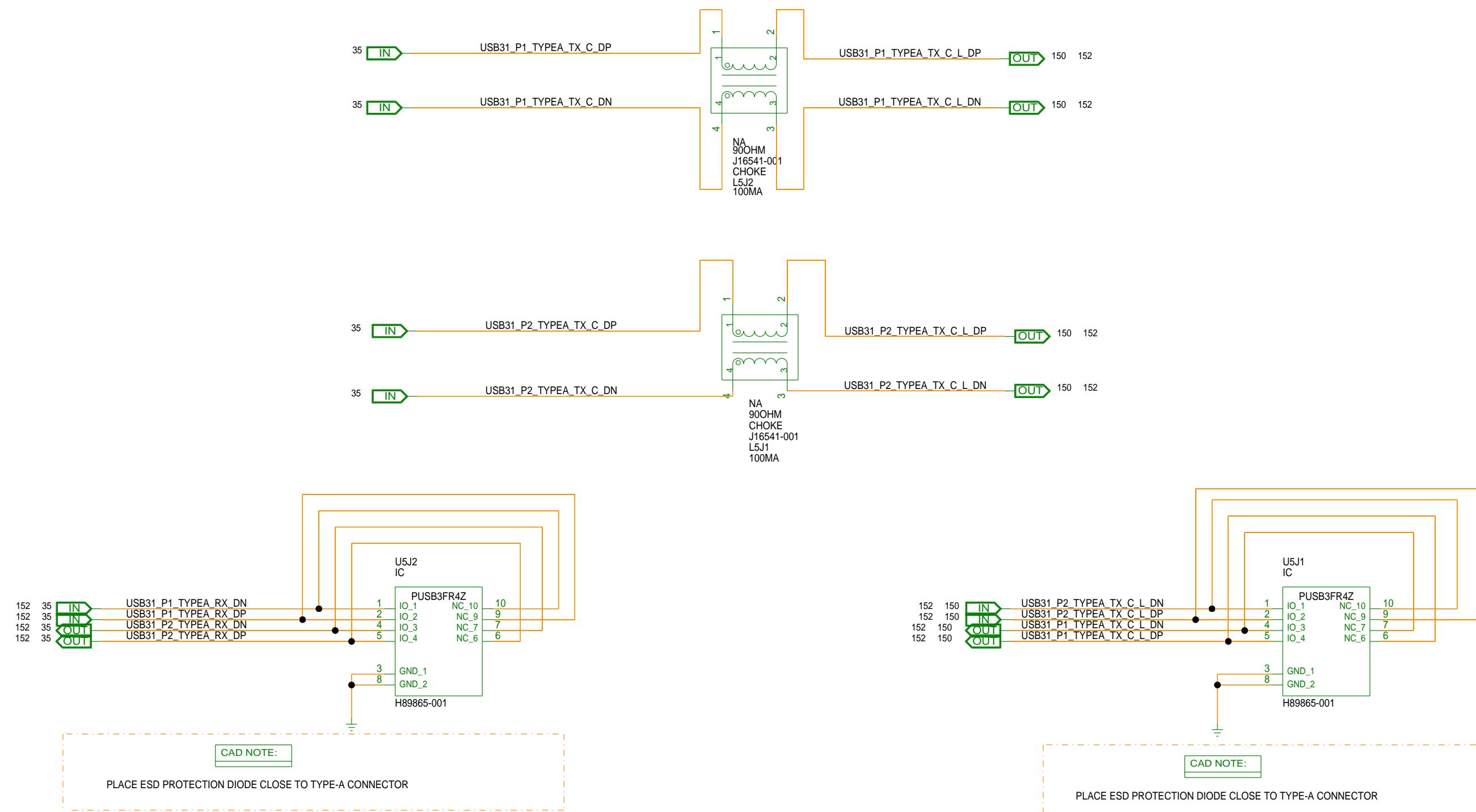
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 147	REV 1.0
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<b>MODULE REV DETAILS</b>							

# USB3.1 CMC/ESD

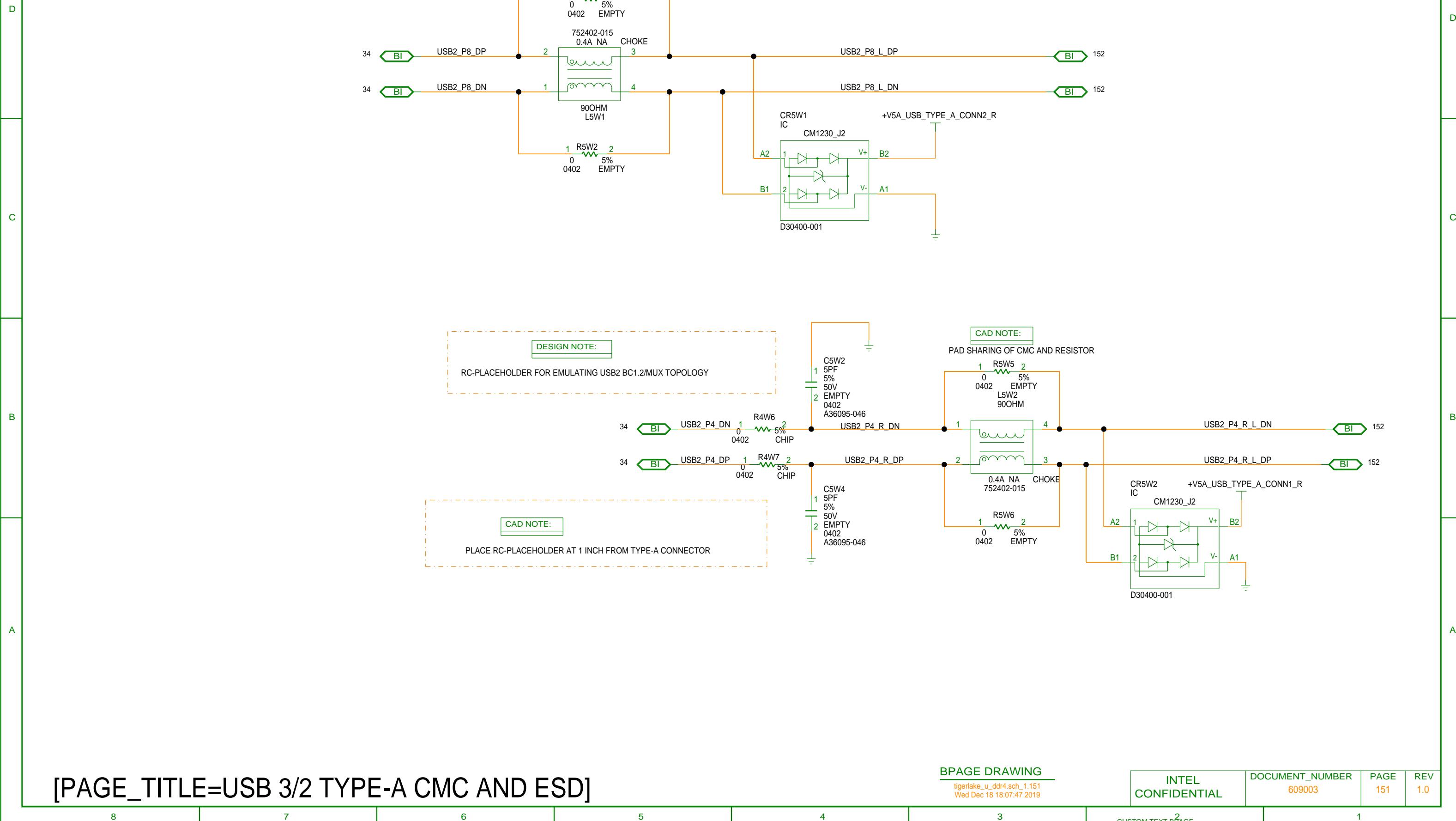


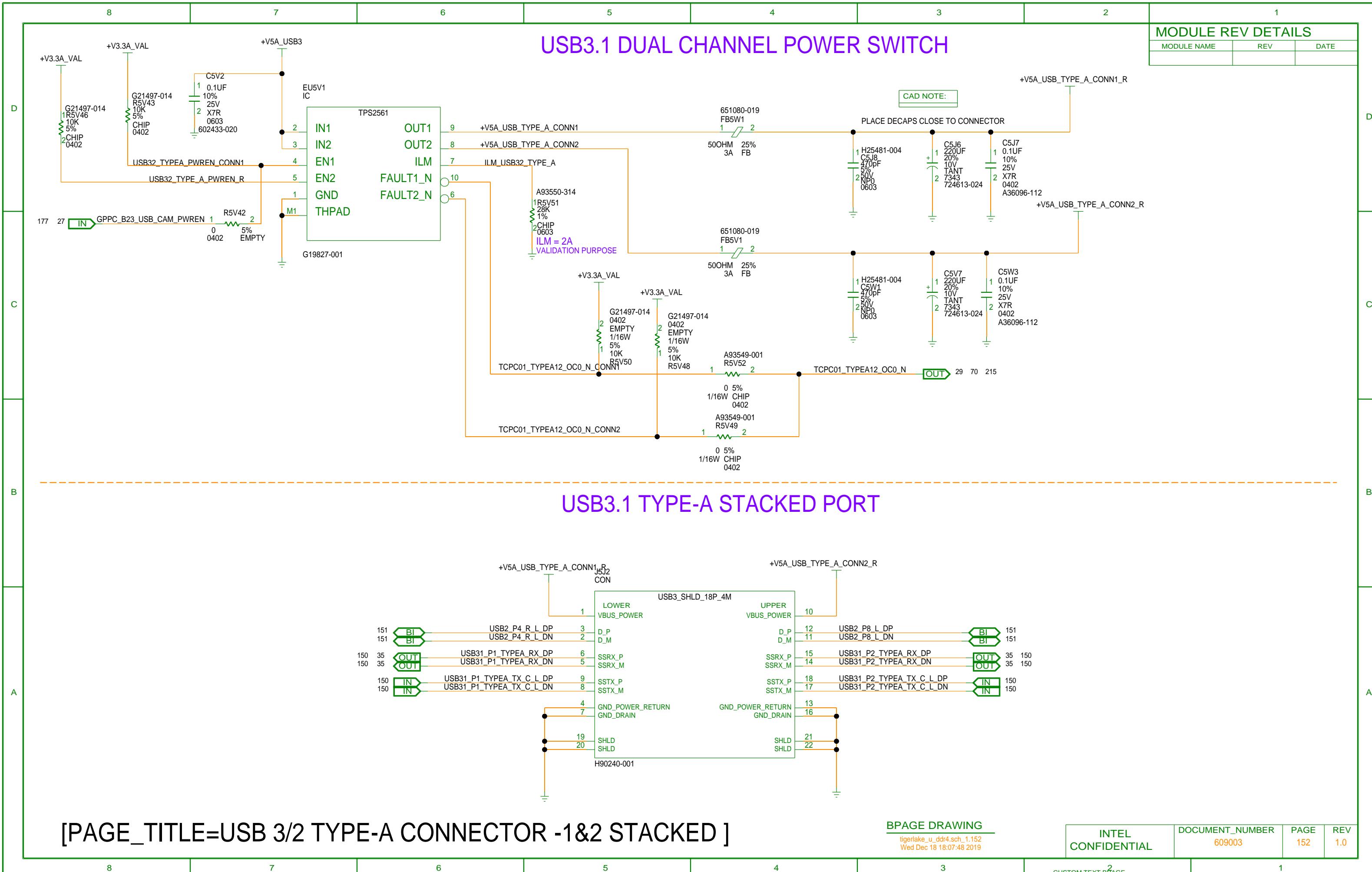
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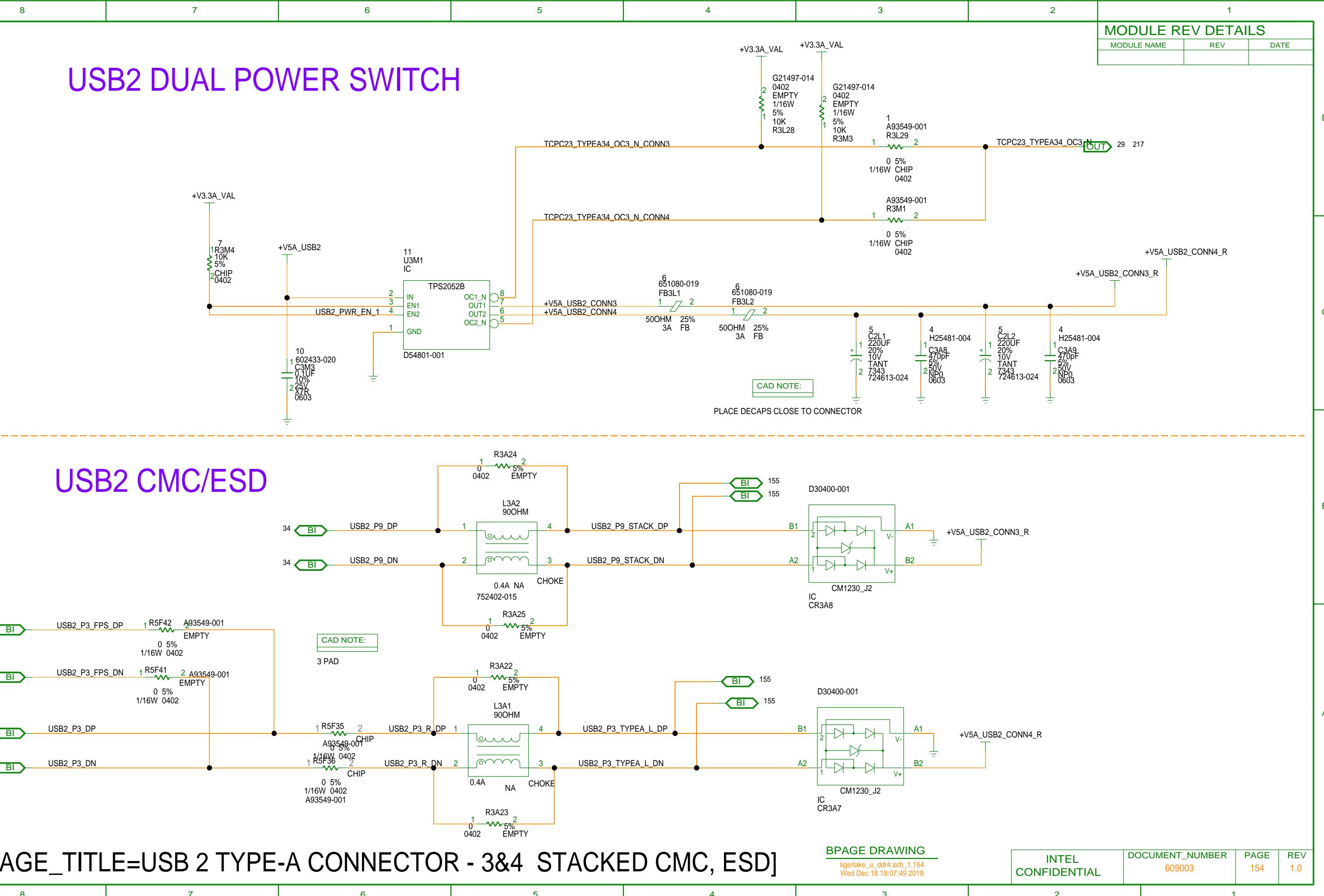
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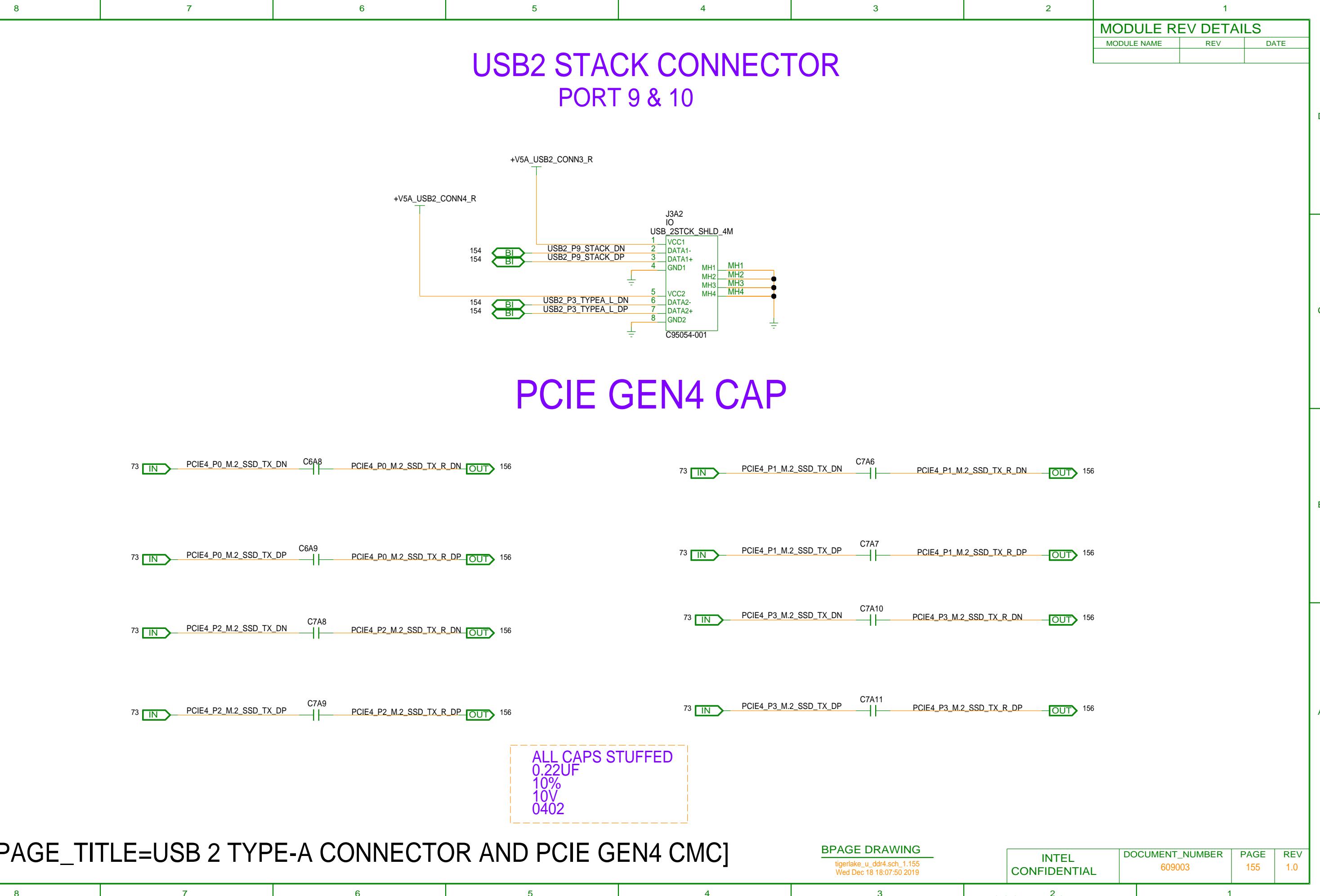
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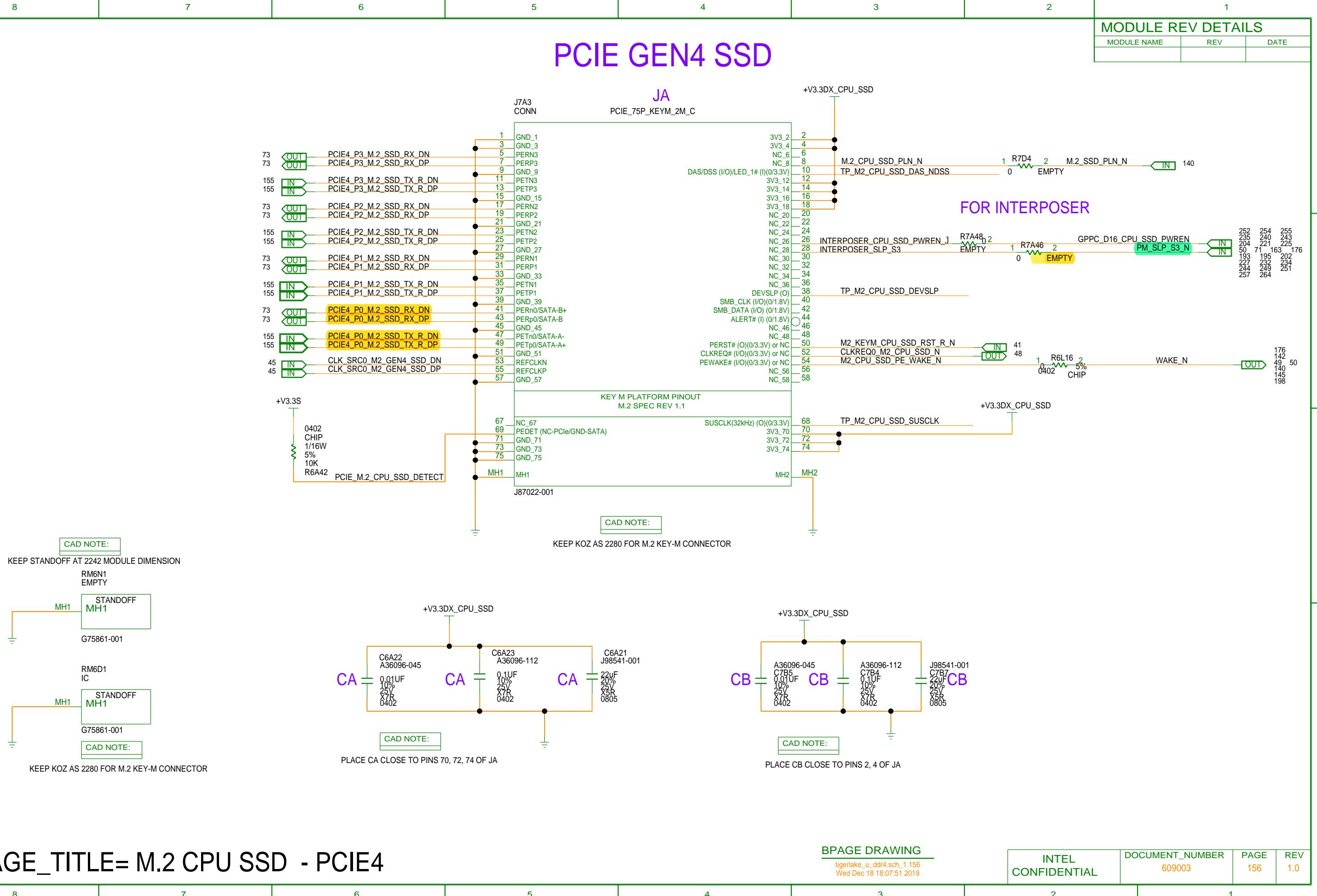


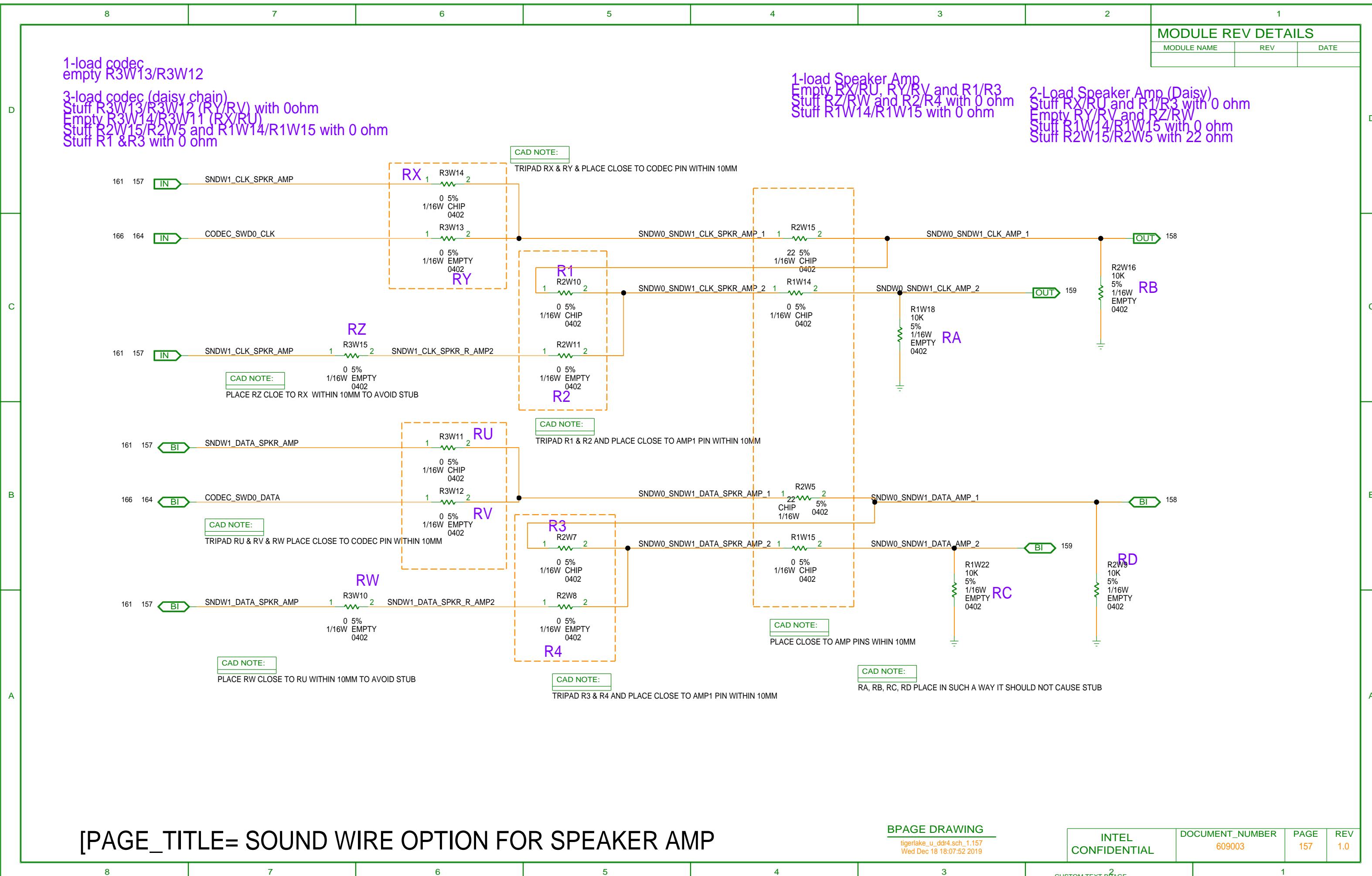


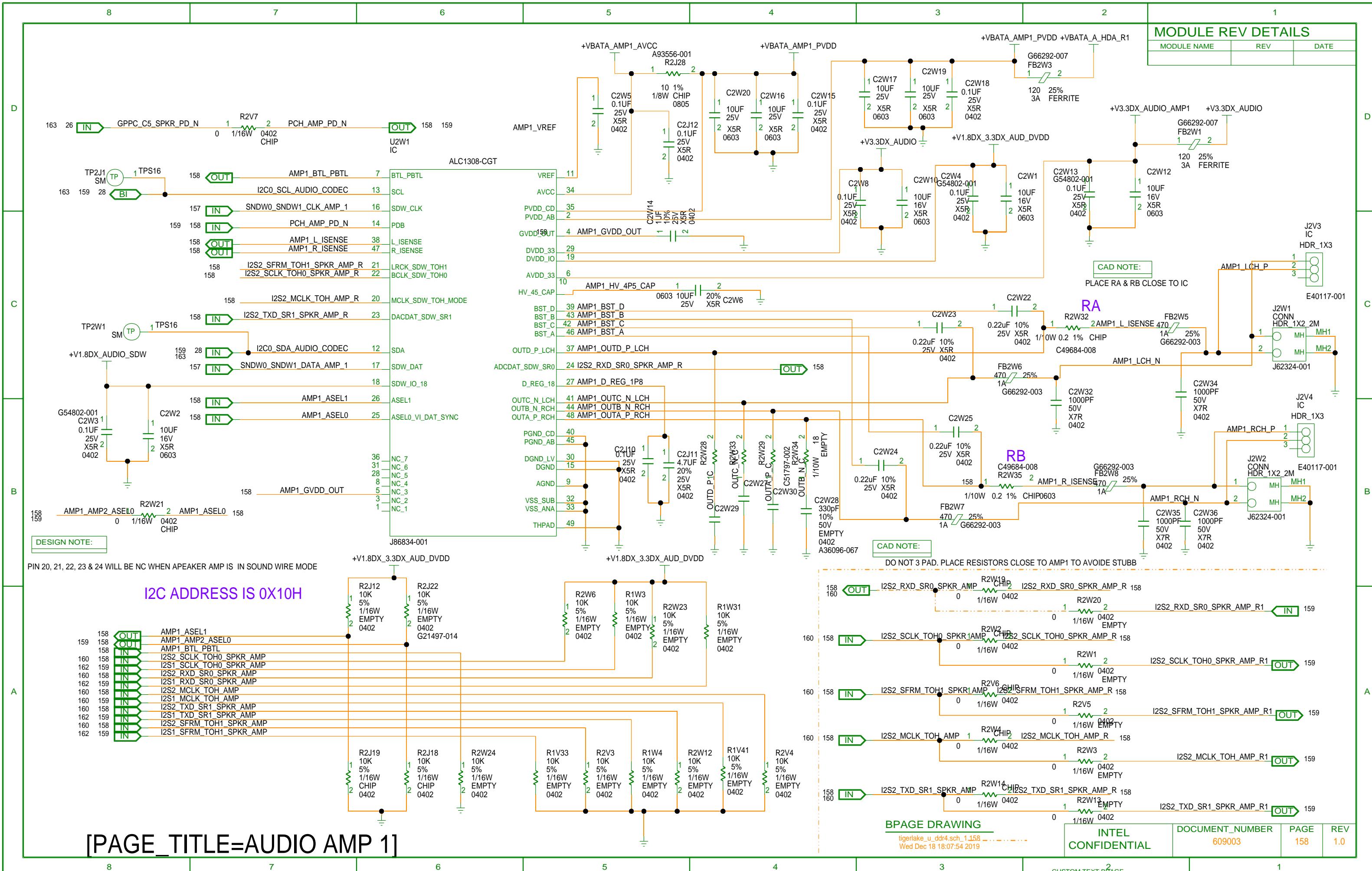
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MODULE NAME	REV	DATE											
D							D						
C							C						
B							B						
A							A						
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8	7	6	5	4	3	CUSTOM TEXT <small>2</small> PAGE	1						

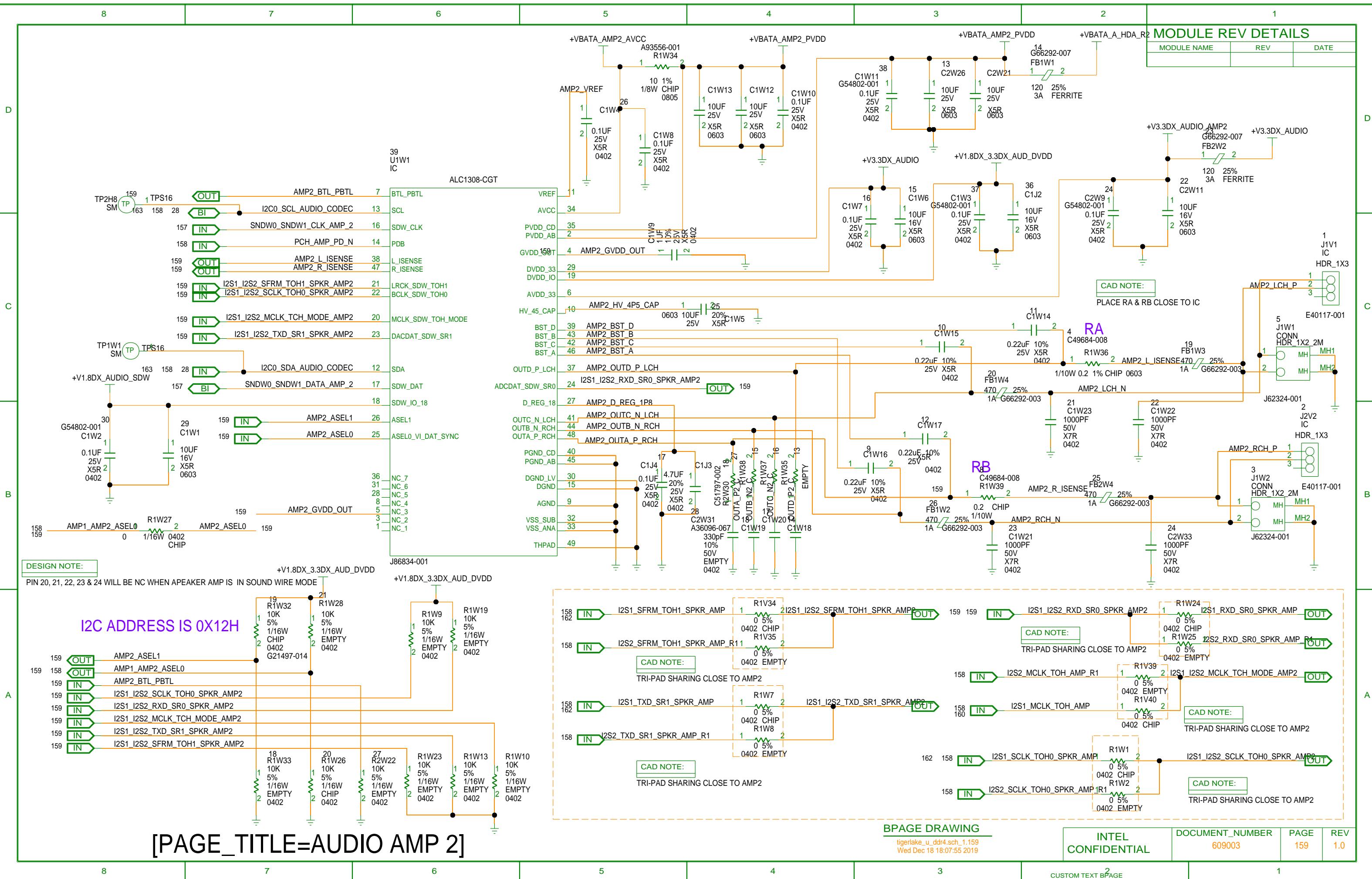


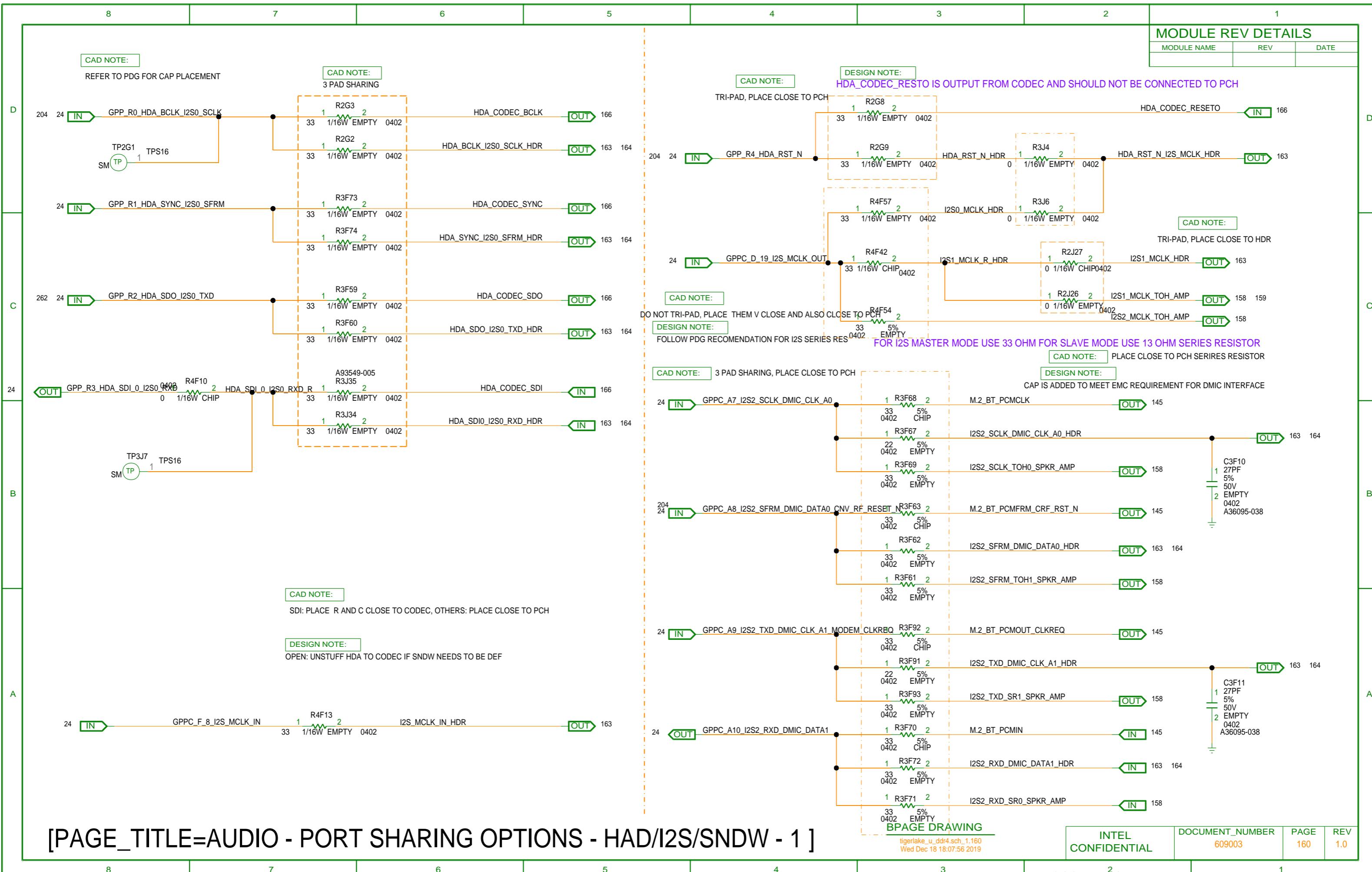


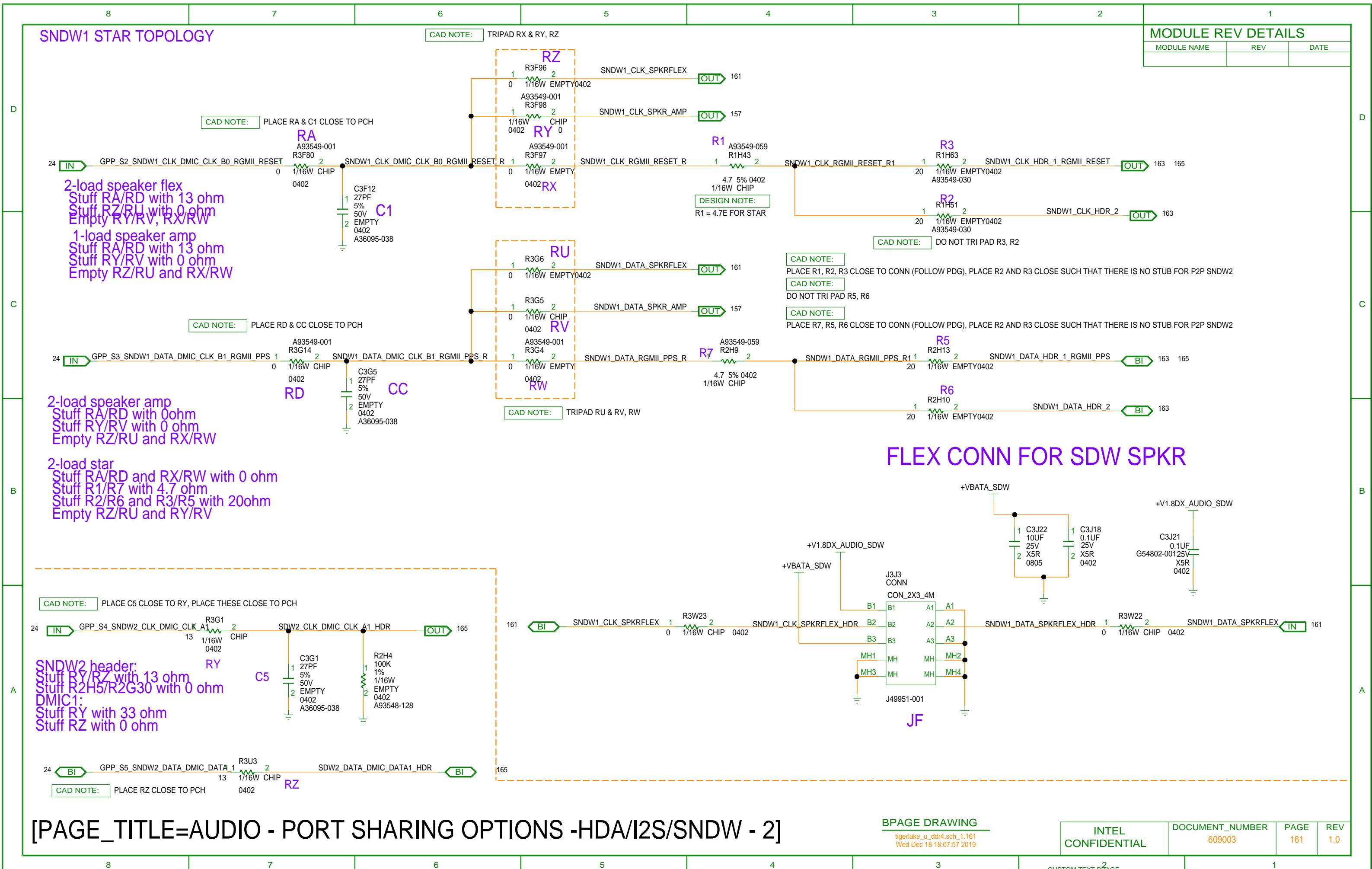


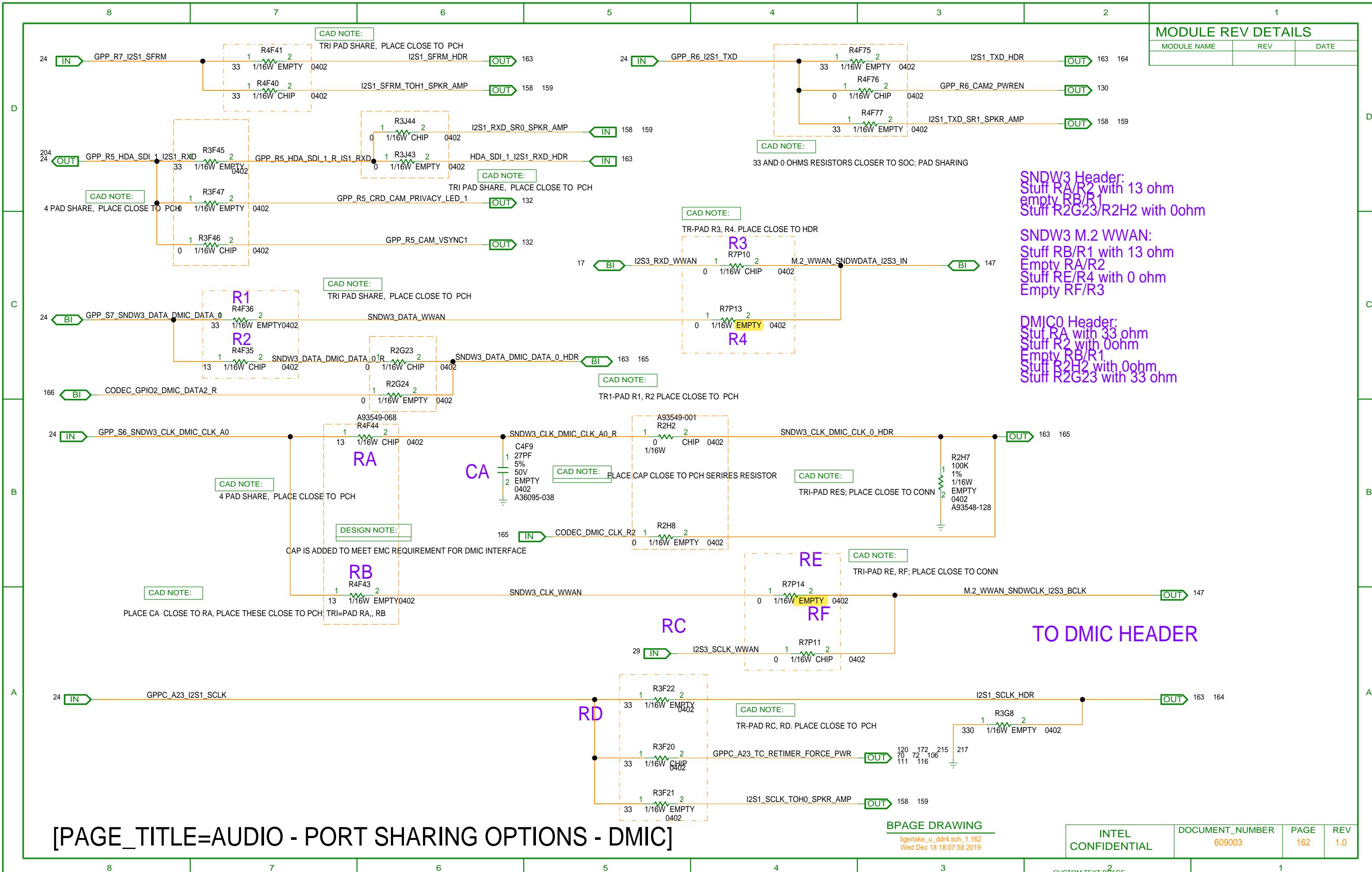


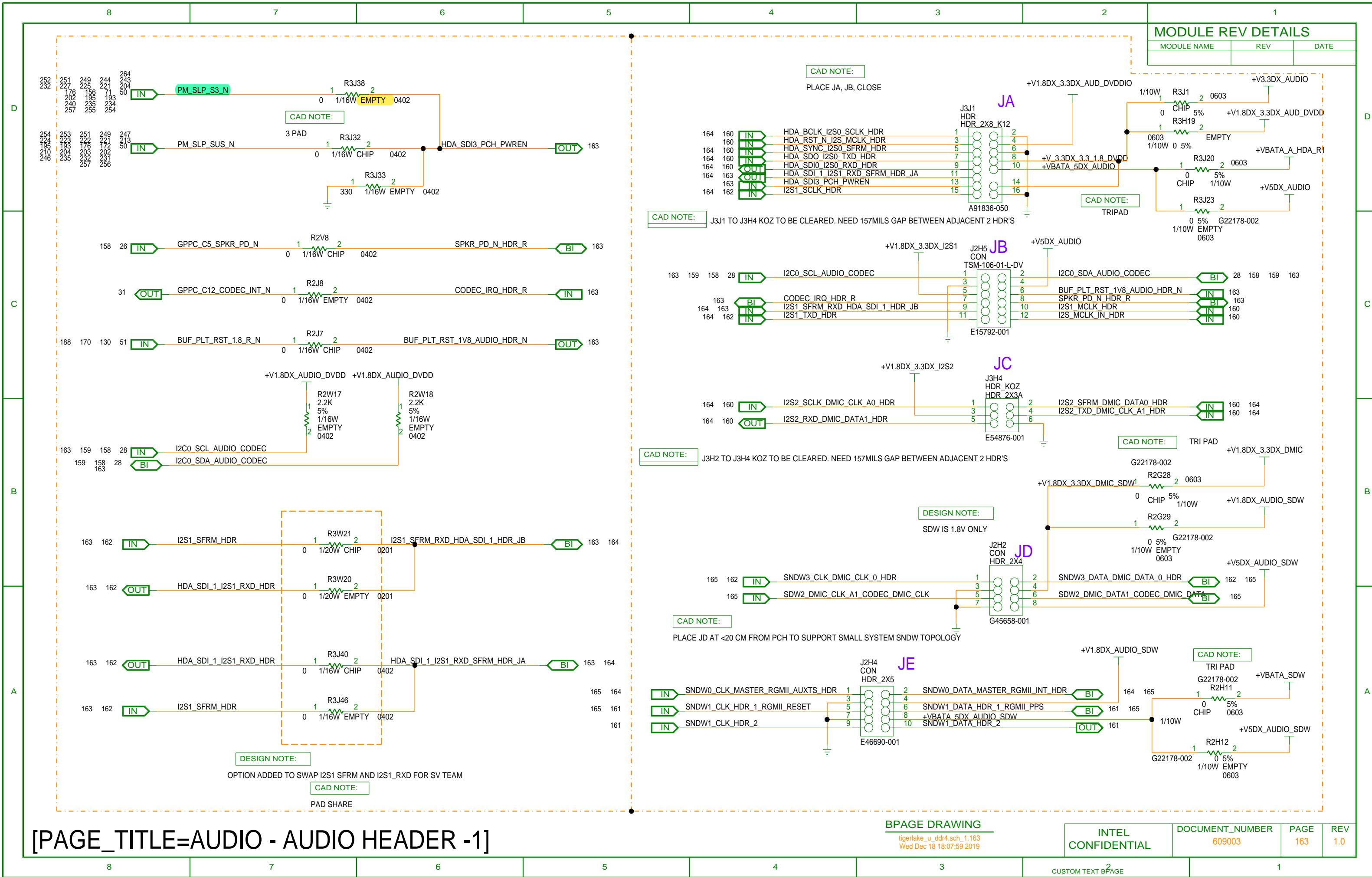


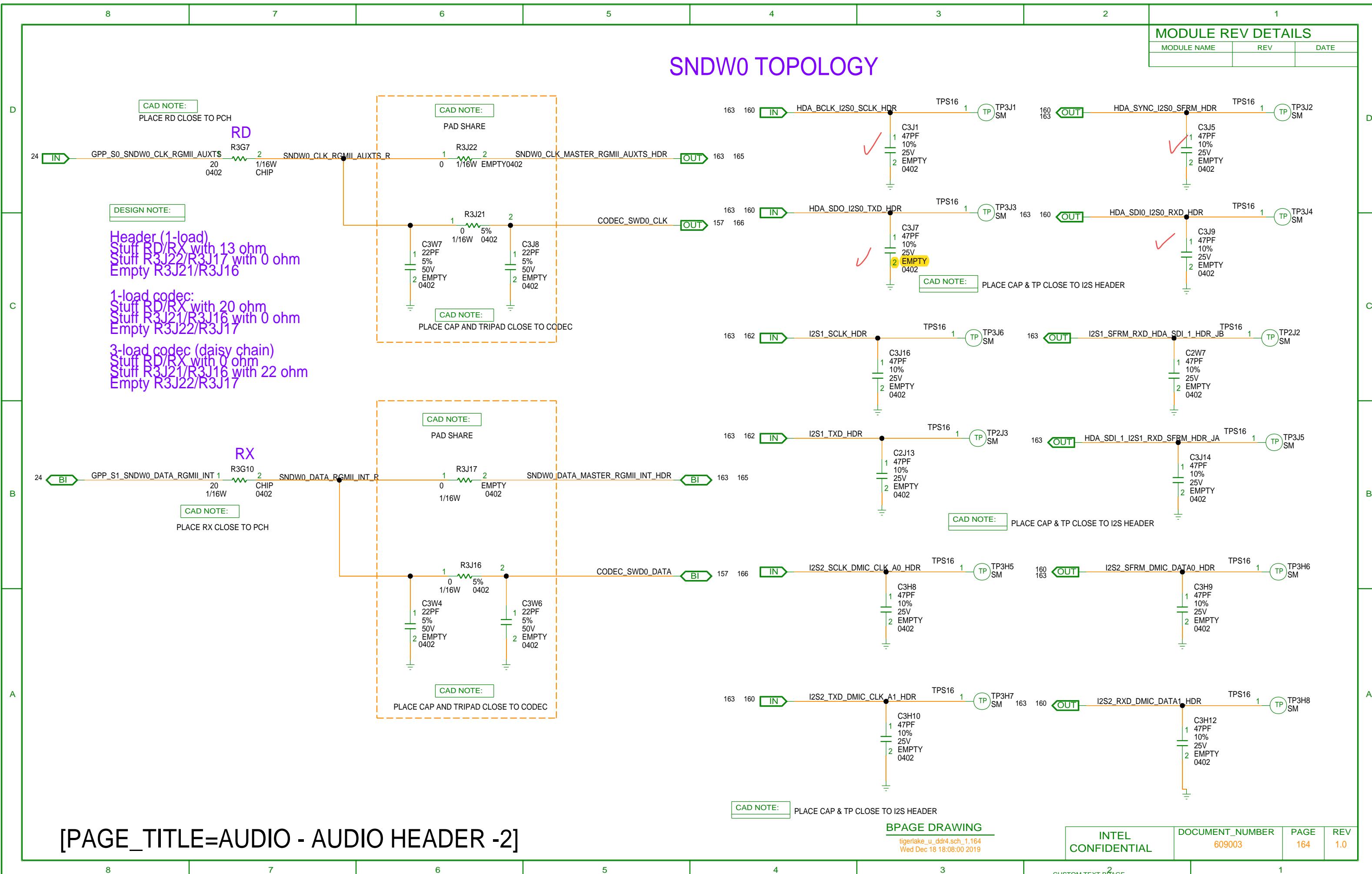


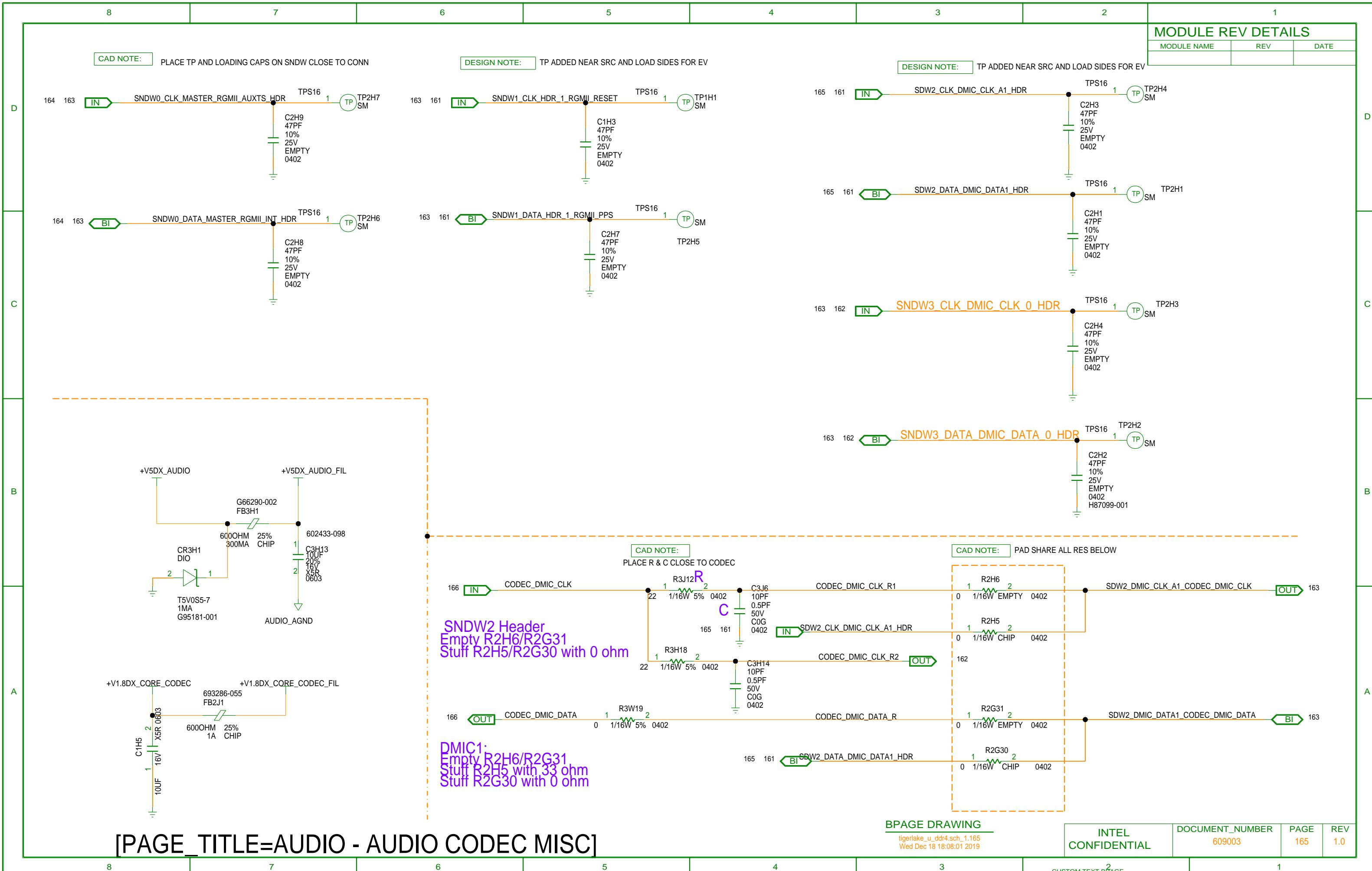


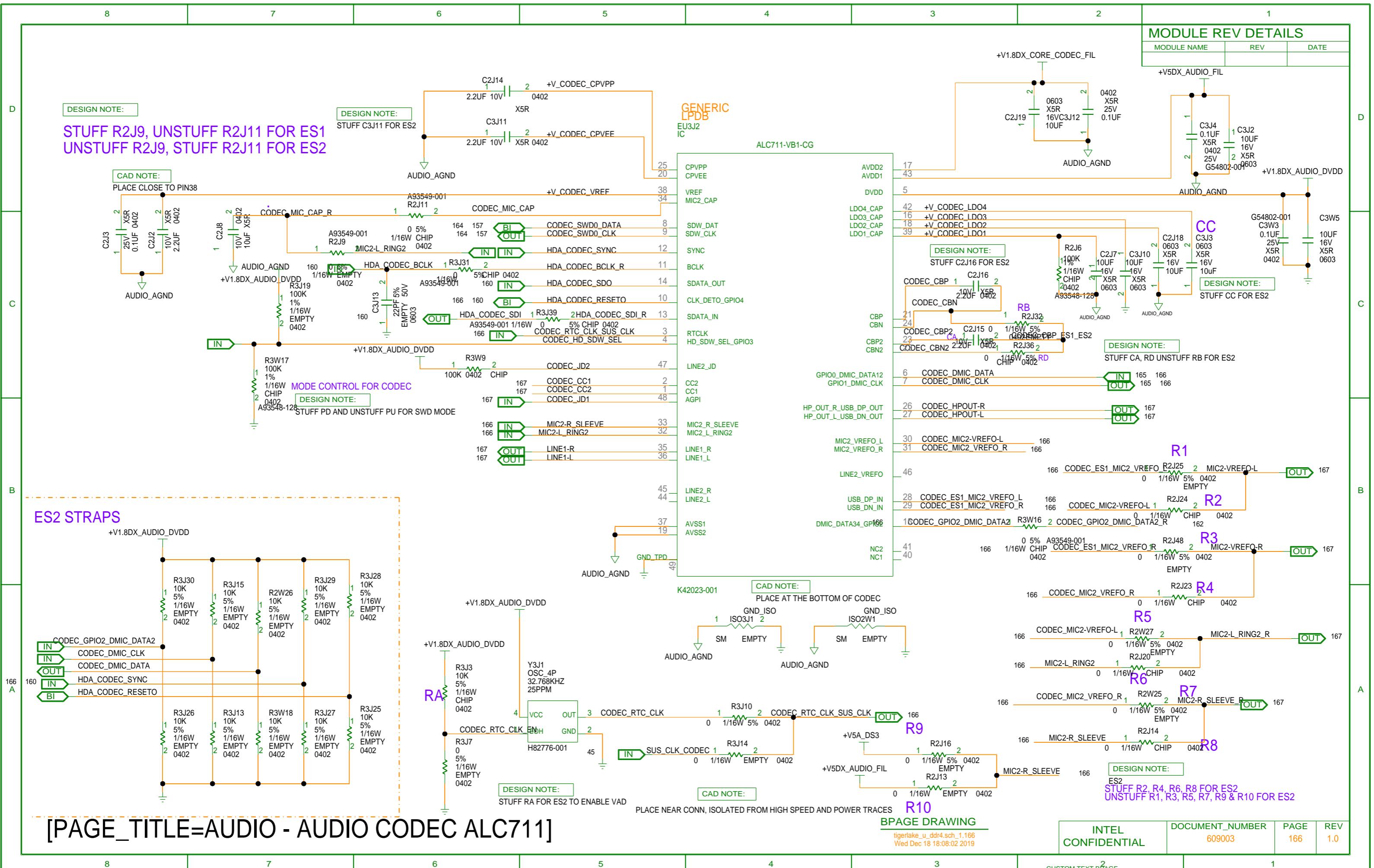


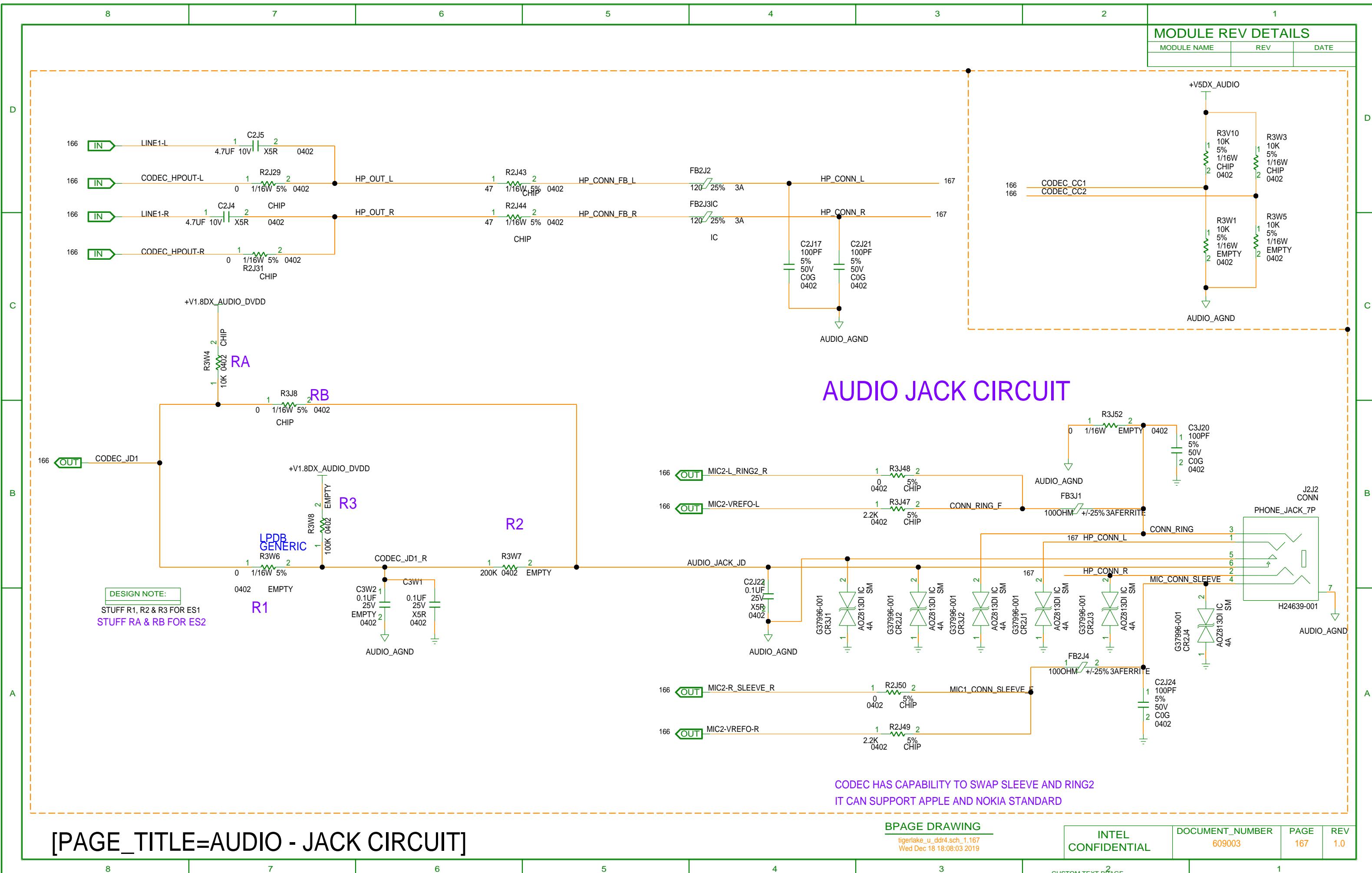


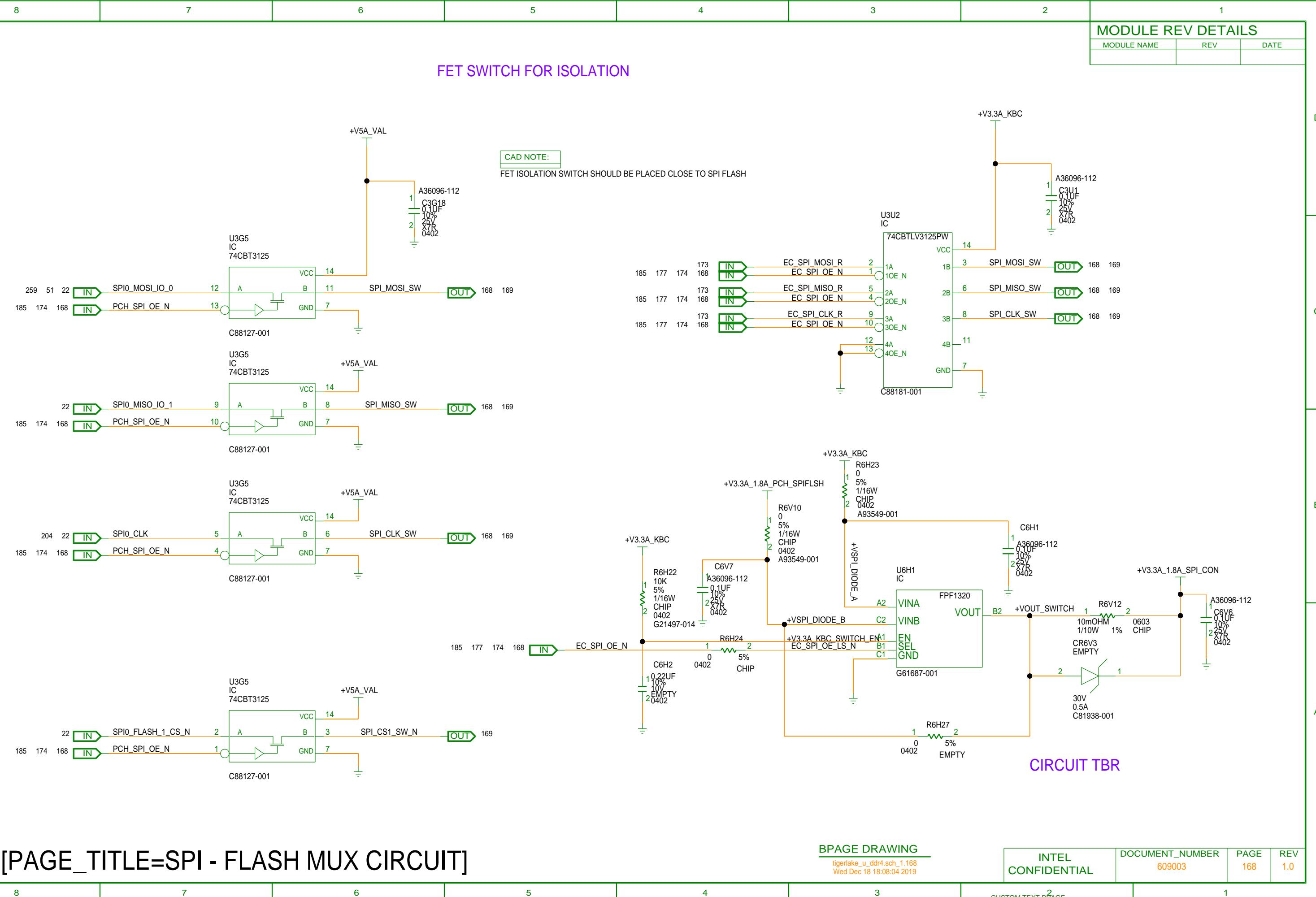


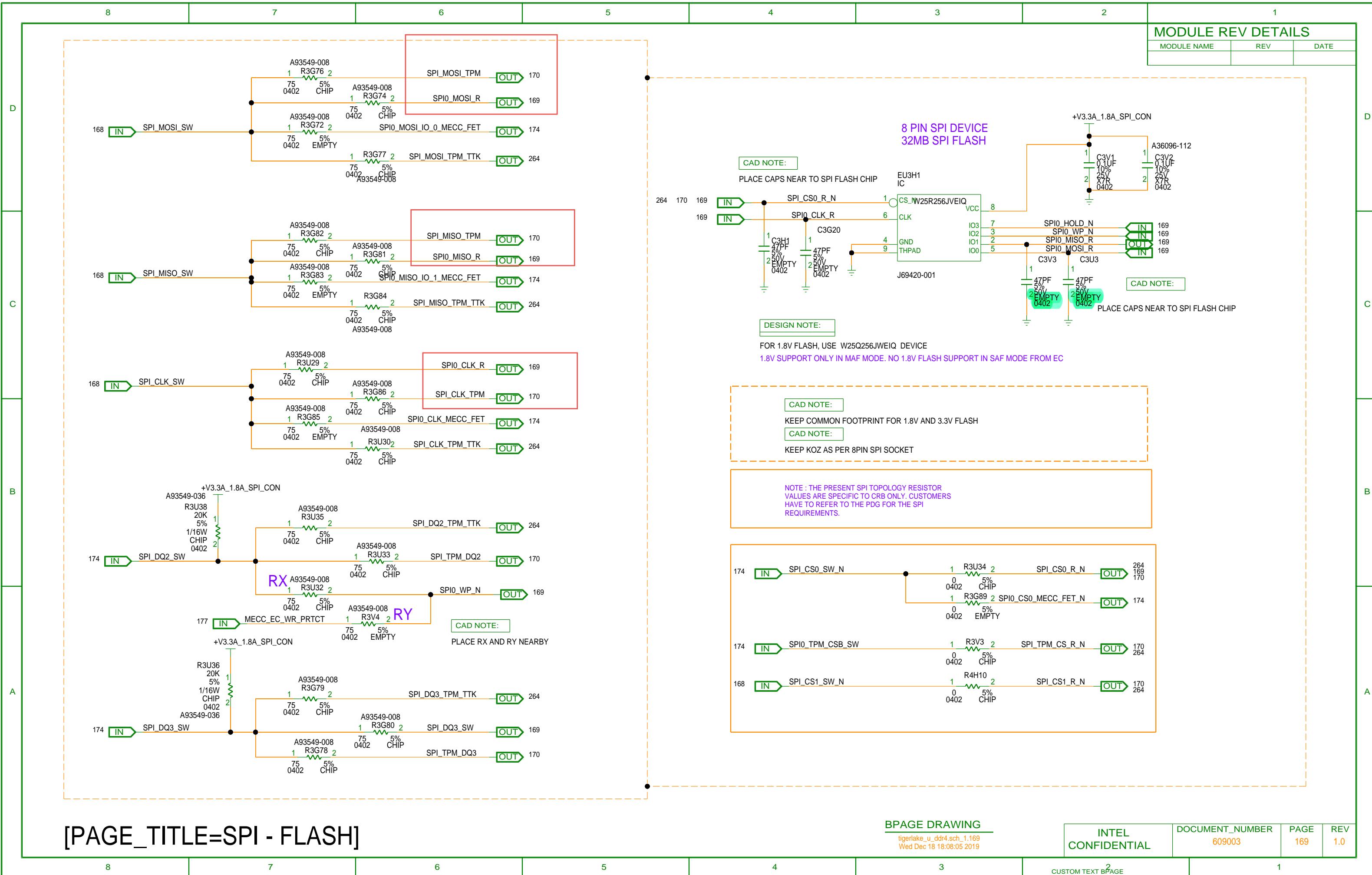


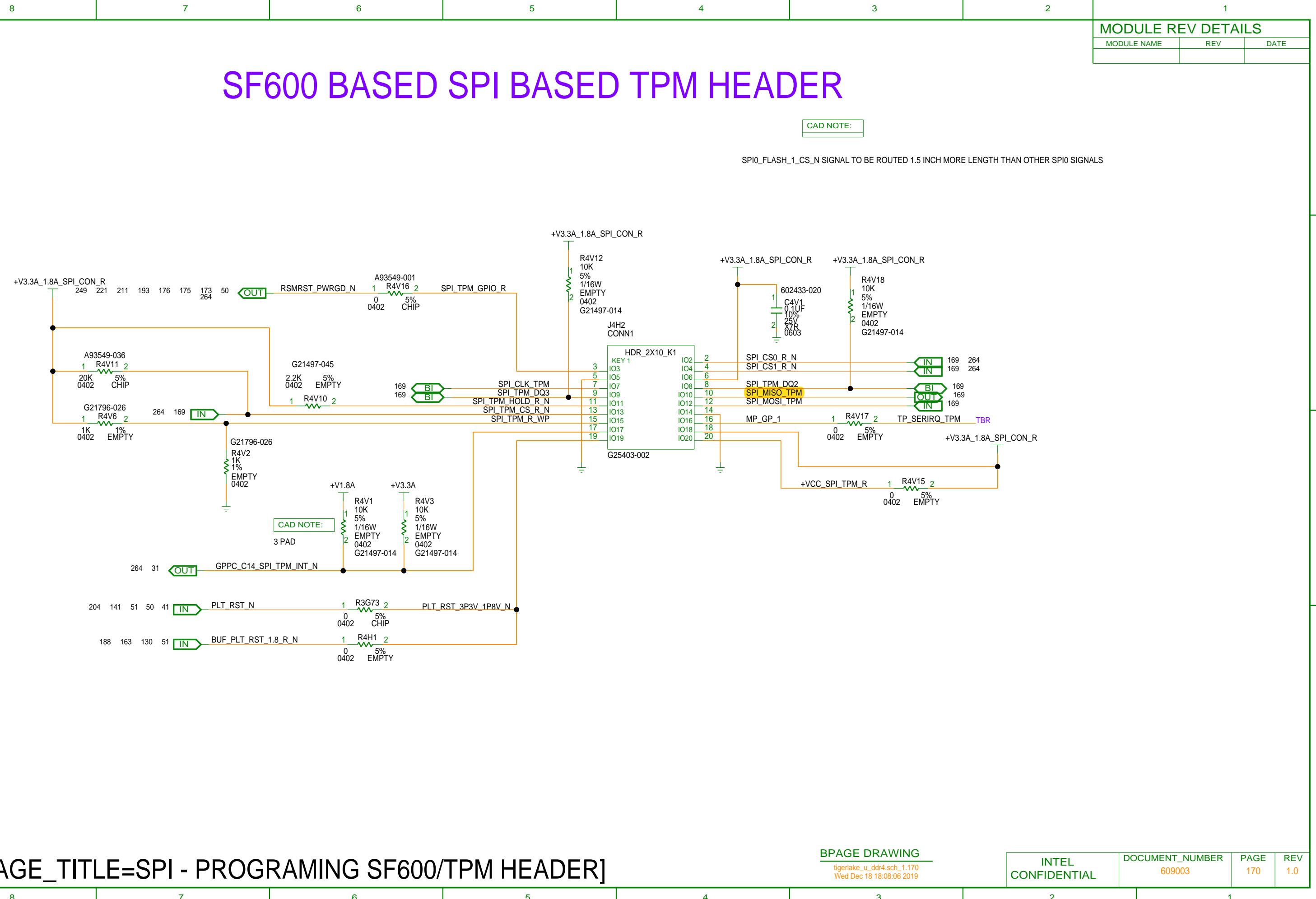


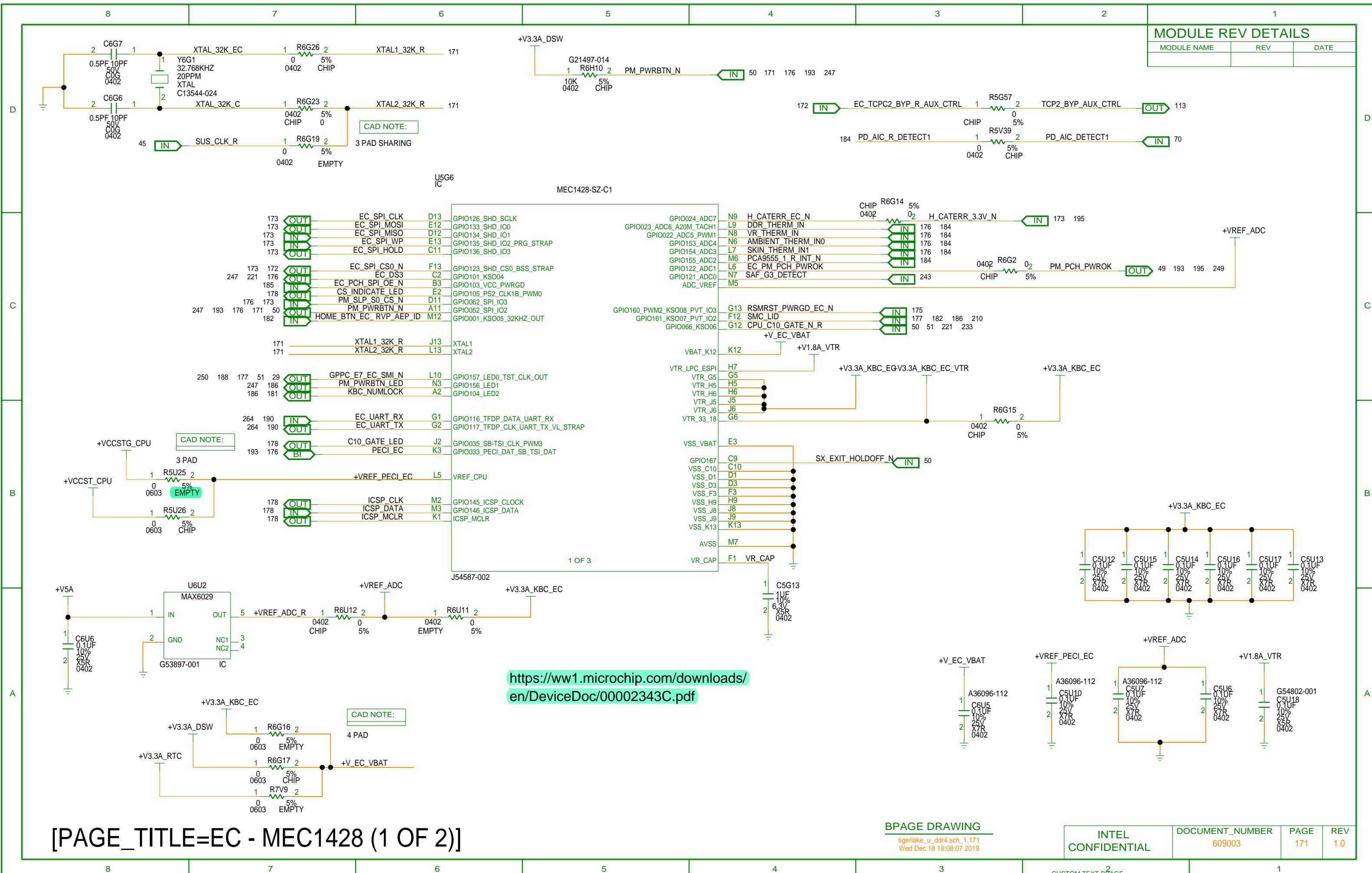


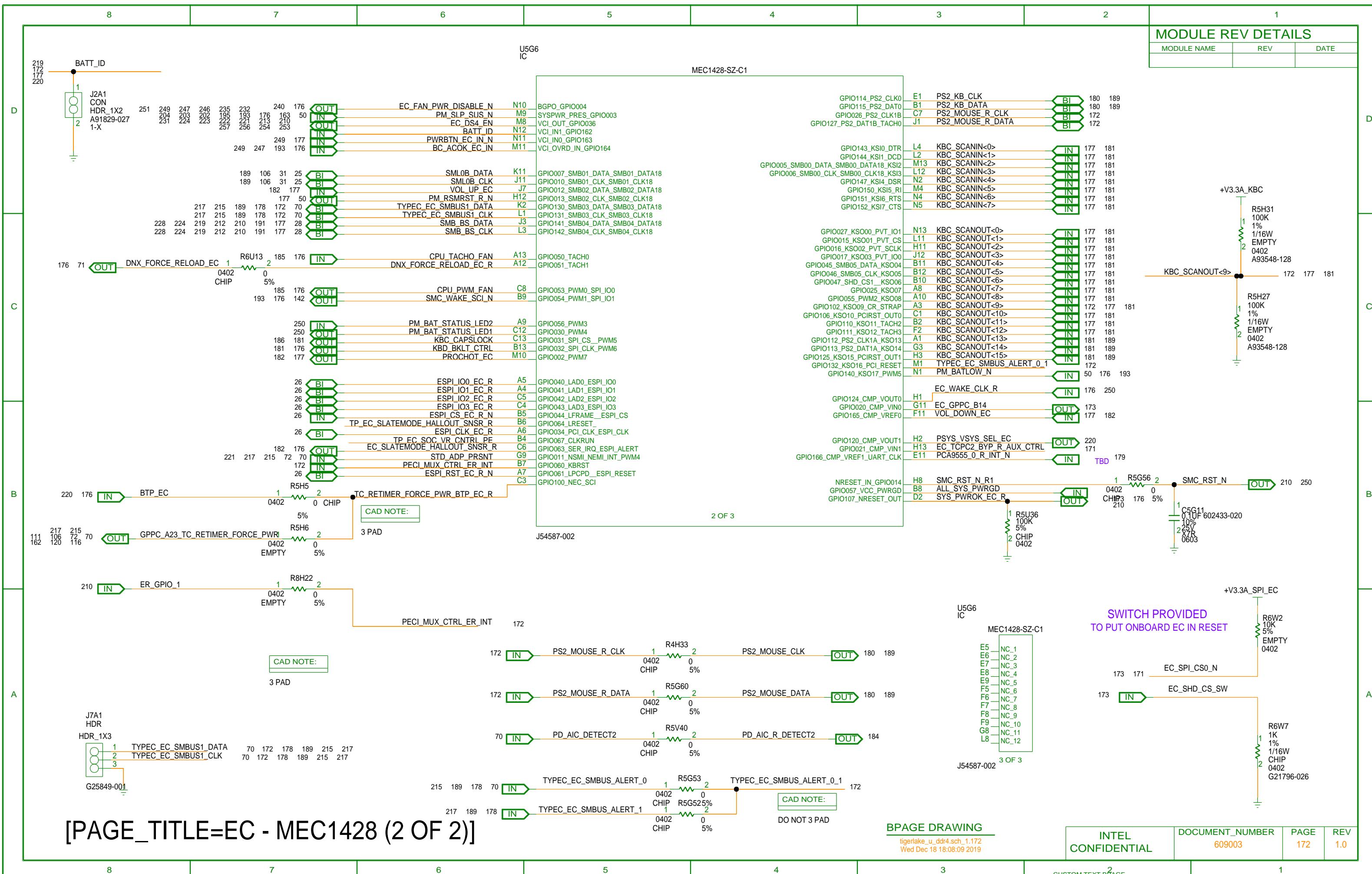


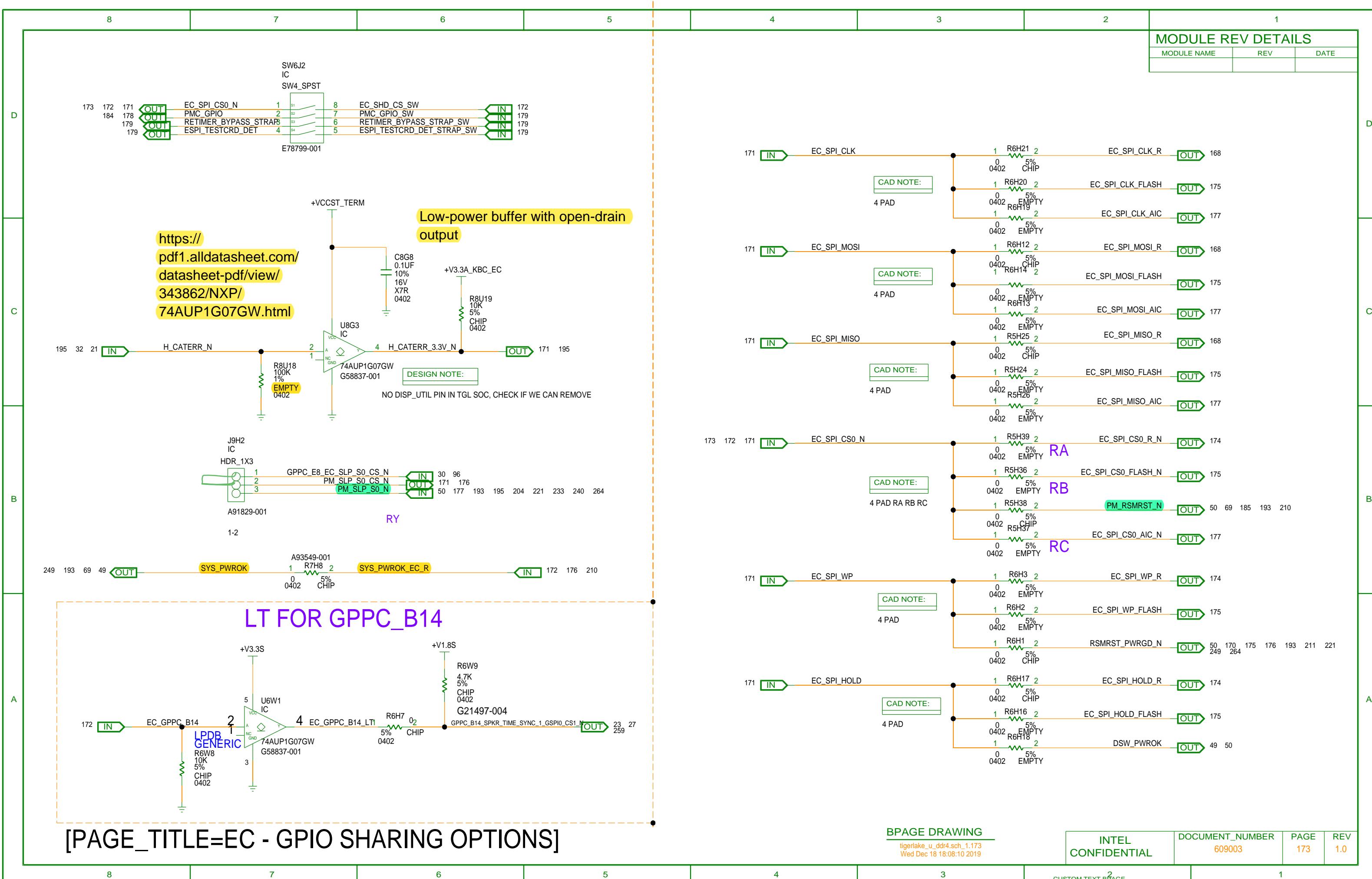


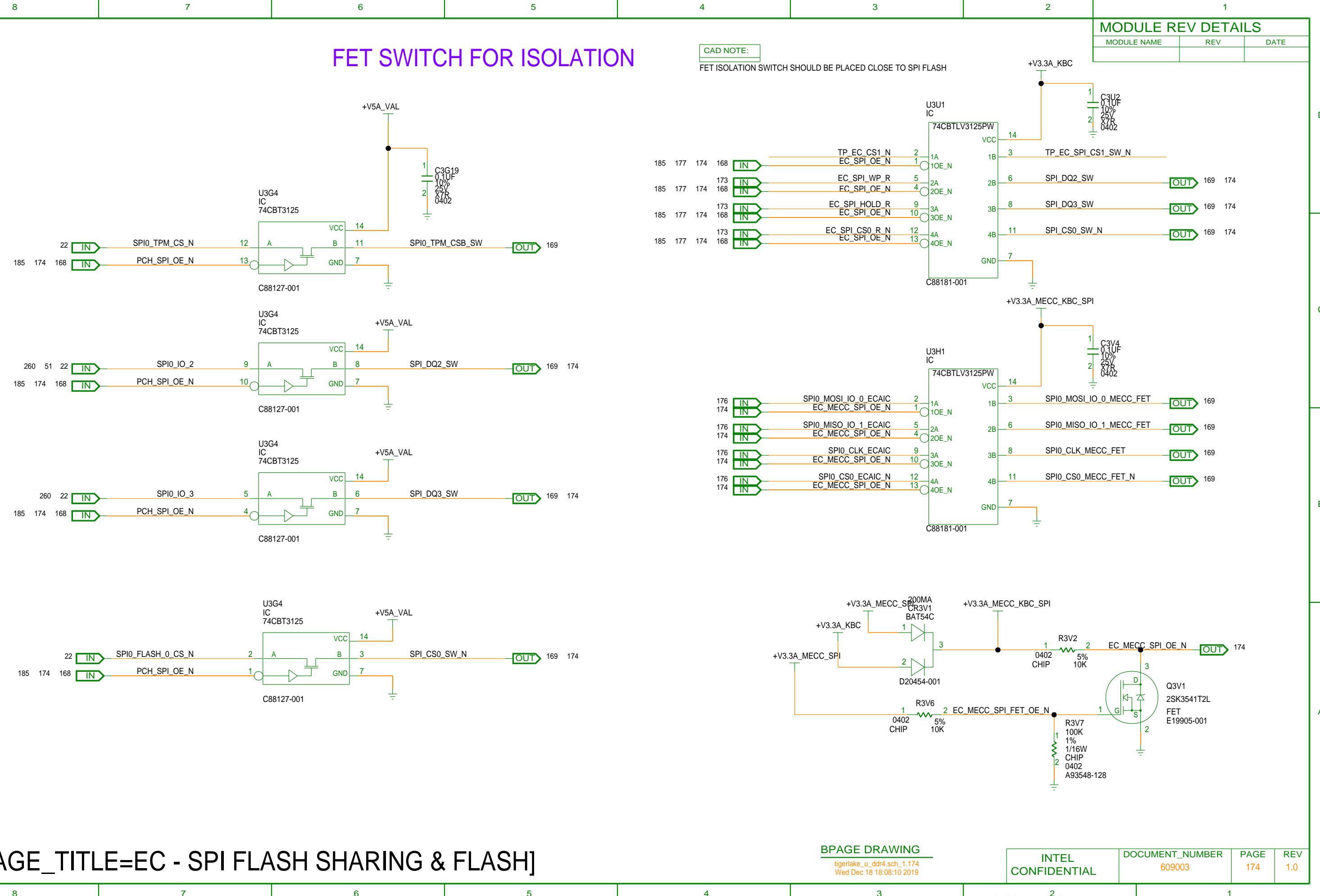






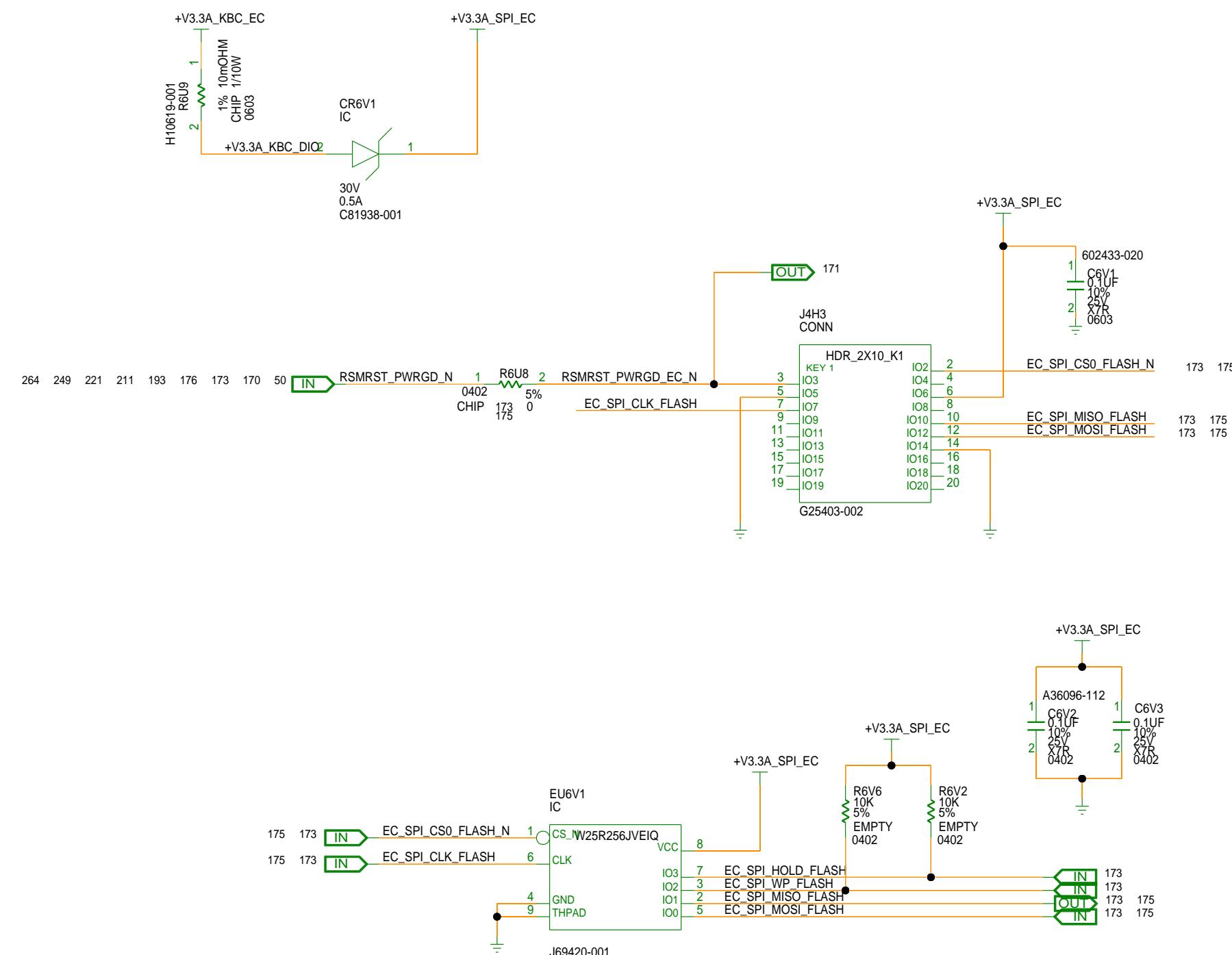






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MODULE NAME	REV	DATE



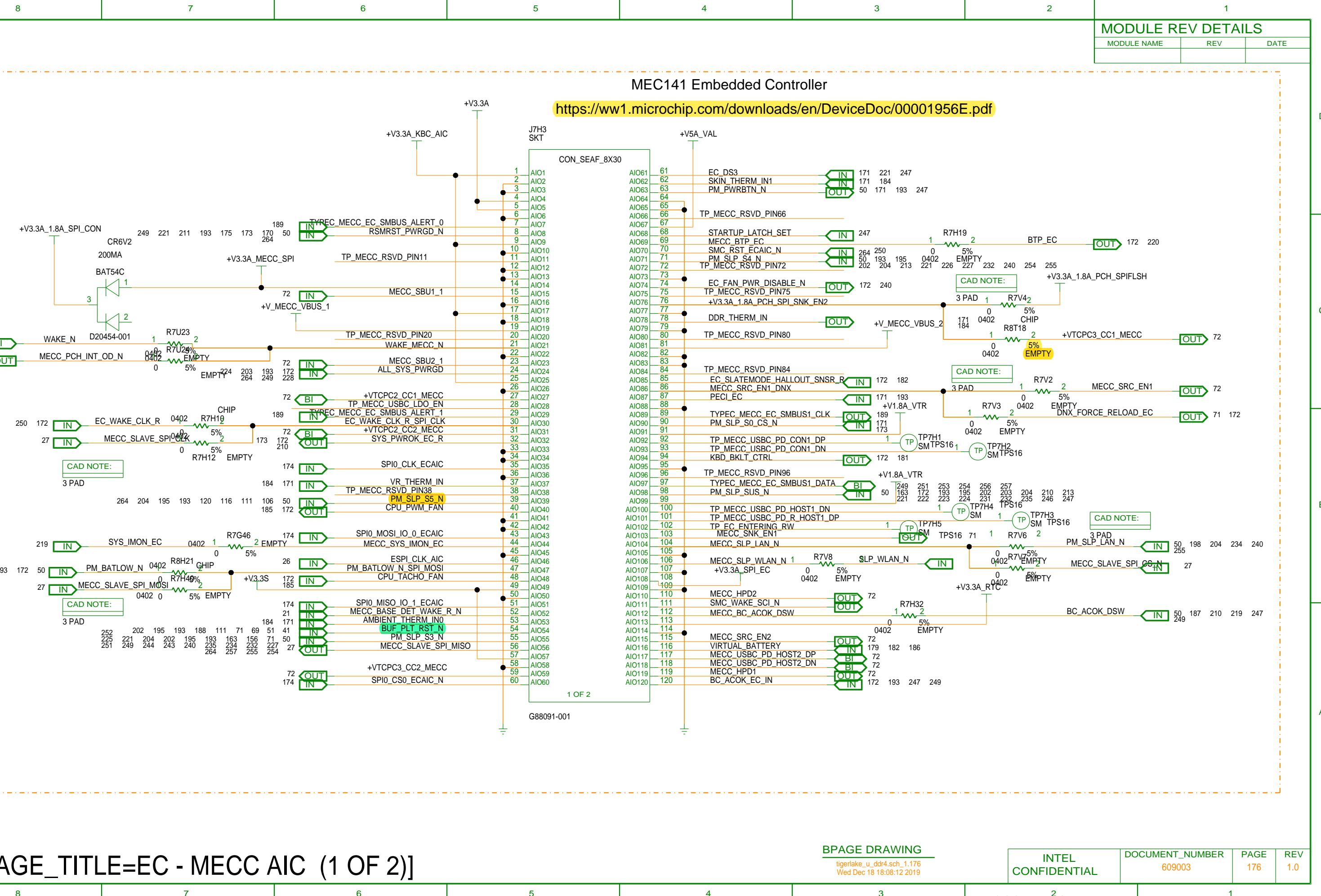
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Wed Dec 18 18:08:11 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 175	REV 1.0
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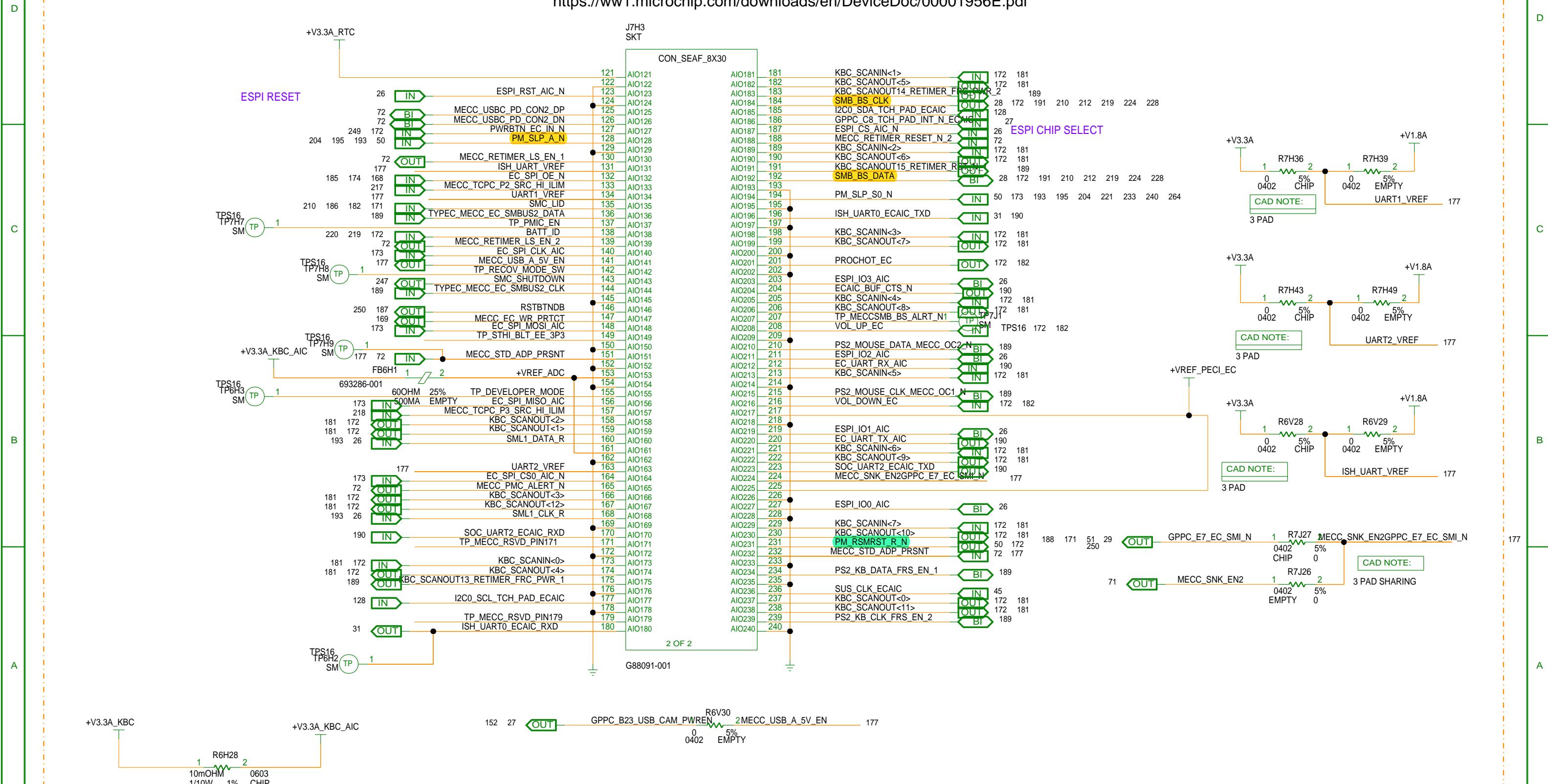
## MEC140x/1x embedded

controller

<https://ww1.microchip.com/downloads/en/DeviceDoc/00001956E.pdf>

## MODULE REV DETAILS

MODULE NAME	REV	DATE



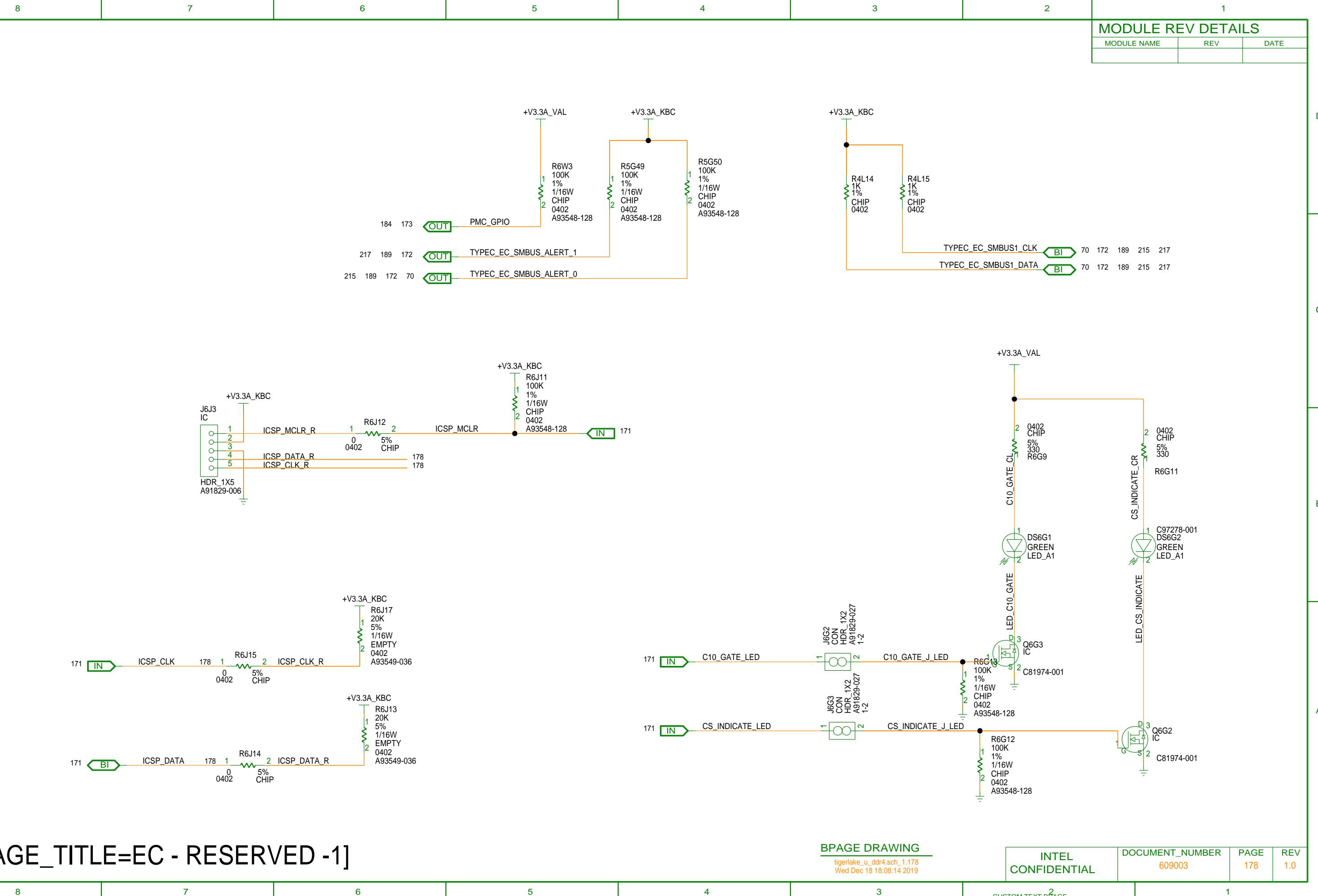
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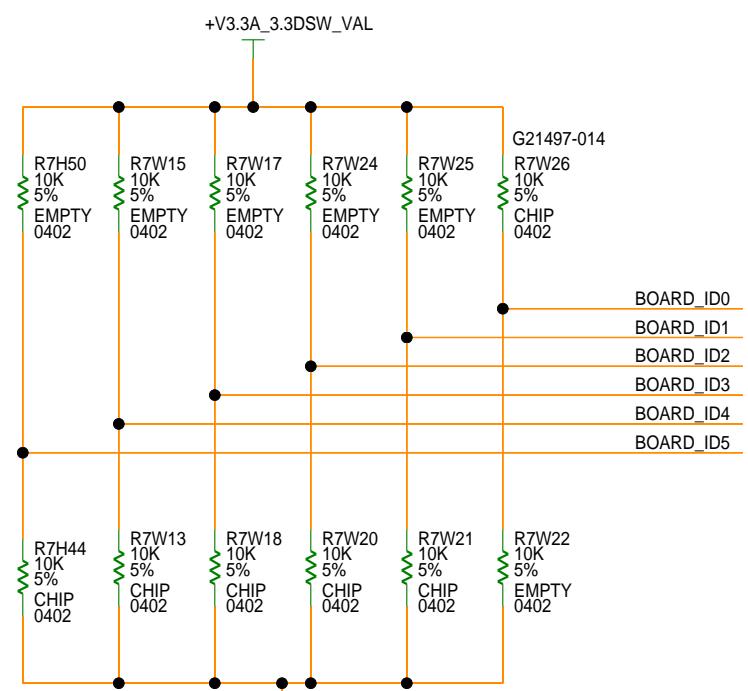
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## BOARD ID ,FAB ID &amp; I/O EXPANDER

## MODULE REV DETAILS

MODULE NAME	REV	DATE

## BOARD REVISION



+V3.3A\_3.3DSW\_VAL

R7V21 10K 5% EMPTY 0402

R7V20 10K 5% CHIP 0402

R7W6 10K 5% EMPTY 0402

BRD\_ID\_A0 179

BRD\_ID\_A1 179

BRD\_ID\_A2 179

R7W1 10K 5% CHIP 0402

R7W2 10K 5% EMPTY 0402

R7W4 10K 5% CHIP 0402

G21497-014

BOARD\_ID0 179

BOARD\_ID1 179

BOARD\_ID2 179

BOARD\_ID3 179

BOARD\_ID4 179

BOARD\_ID5 179

R7V22 10K 5% CHIP 0402

R7V19 02

PCA9555\_0\_R\_INT\_IN

PCA9555\_0\_INT\_M

SMB\_BS\_IOEXP\_CLK\_R1 22

SMB\_BS\_IOEXP\_DATA\_R1 23

+V3.3A\_3.3DSW\_VAL

G21497-014

R7H6 1K 1% CHIP 0402

SPD\_PRSNT\_J

J7H2 CON HDR\_1X2 A91829-027 1-2

SPD\_PRSNT 179

R7H9 10K 5% CHIP 0402

+V3.3A\_3.3DSW\_VAL

R7W12 10K 5% EMPTY 0402

R7W23 10K 5% EMPTY 0402

R7W11 10K 5% EMPTY 0402

BOM\_ID2 179

BOM\_ID1 179

BOM\_ID0 179

R7W10 10K 5% CHIP 0402

R7W19 10K 5% CHIP 0402

R7W9 10K 5% CHIP 0402

1/16W CHIP 10K 5% 0402

ESPI\_TESTCRD\_DET 173 179

R7W16 G21497-014

+V3.3A\_3.3DSW\_VAL

C7V3 0.1UF 25V X7R 0603

602433-020

+V3.3A\_3.3DSW\_VAL

U7W1 IC PCA9555PW

VDD

A2

A1

A0

IO\_1\_7

IO\_1\_6

IO\_1\_5

IO\_1\_4

IO\_1\_3

IO\_1\_2

IO\_1\_1

IO\_1\_0

IO\_0\_7

IO\_0\_6

IO\_0\_5

IO\_0\_4

IO\_0\_3

IO\_0\_2

IO\_0\_1

IO\_0\_0

11 ESPI\_TESTCRD\_DET

10 RETIMER\_BYPASS\_STRAP

9 VIRTUAL\_DOCK\_DET\_N

8 VIRTUAL\_BATTERY

7 SPD\_PRSNT

6 FAB\_ID1

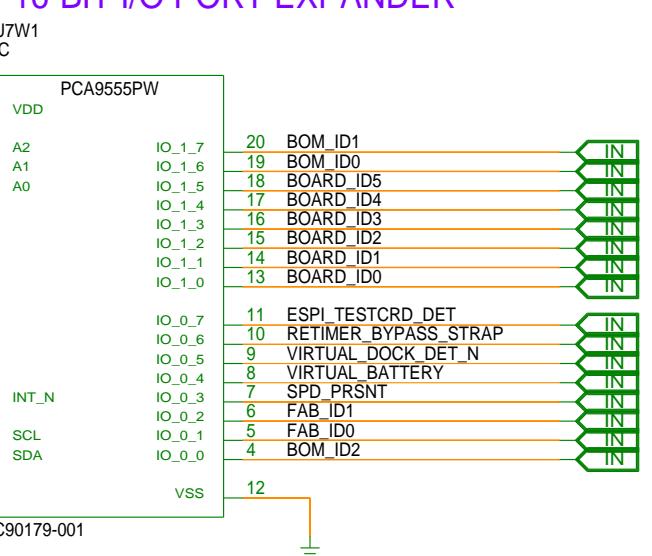
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4 BOM\_ID2

12 VSS

C90179-001

## 16-BIT I/O PORT EXPANDER

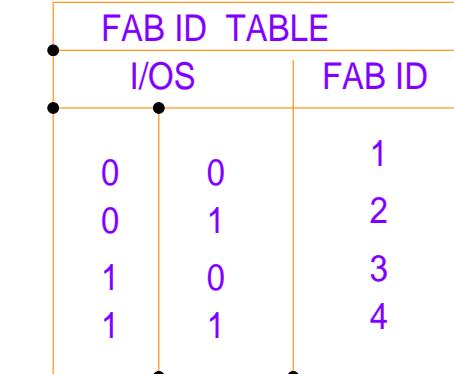
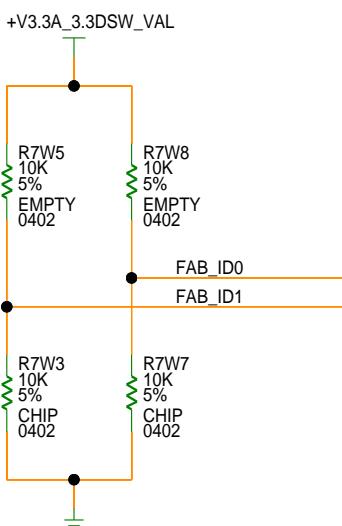


## SLAVE ADDRESS

0 1 0 0 A2 A1 A0 R/W

FIXED PROGRAMMABLE PCA9555 ADDRESS

## FAB REVISION



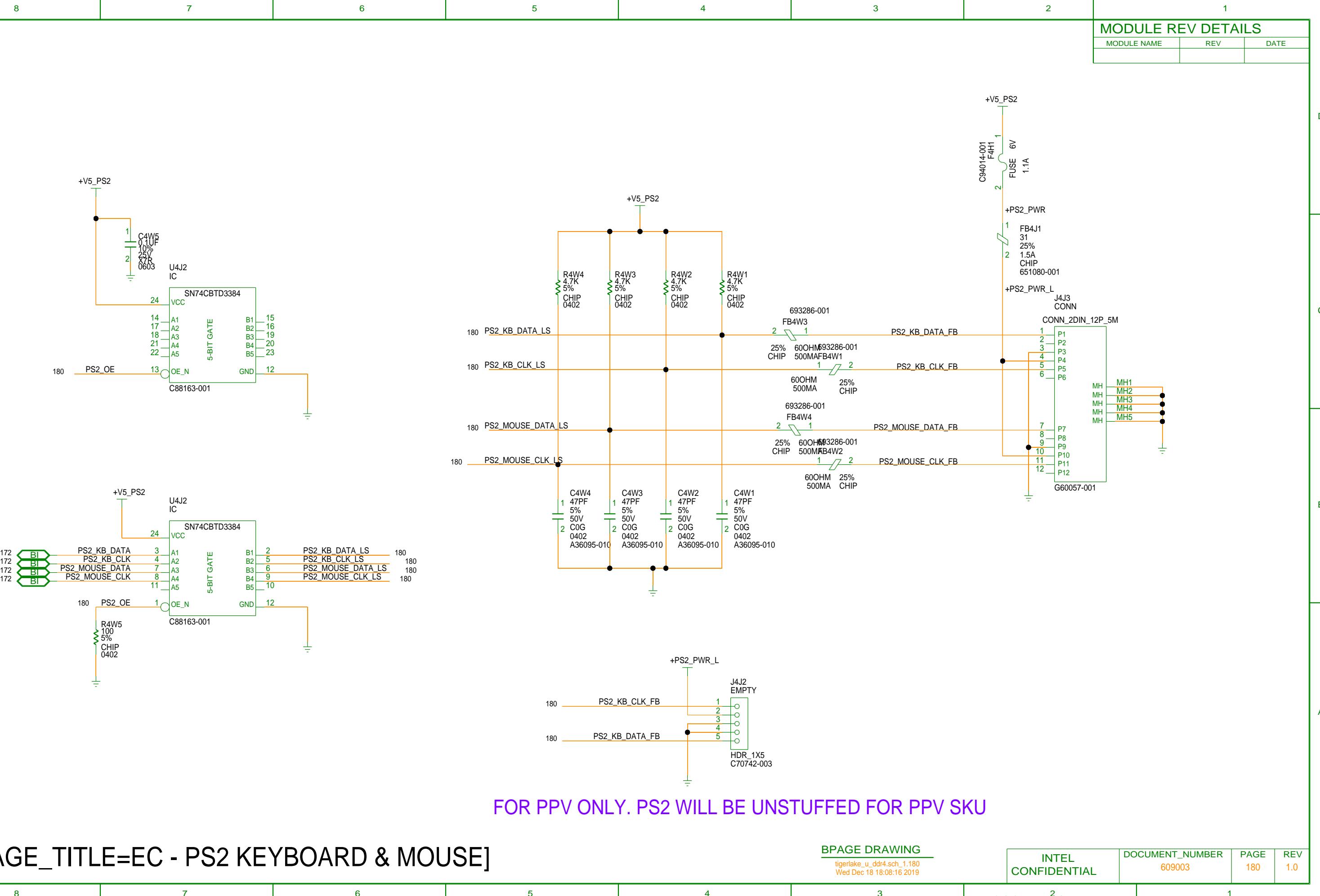
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Wed Dec 18 18:08:15 2019

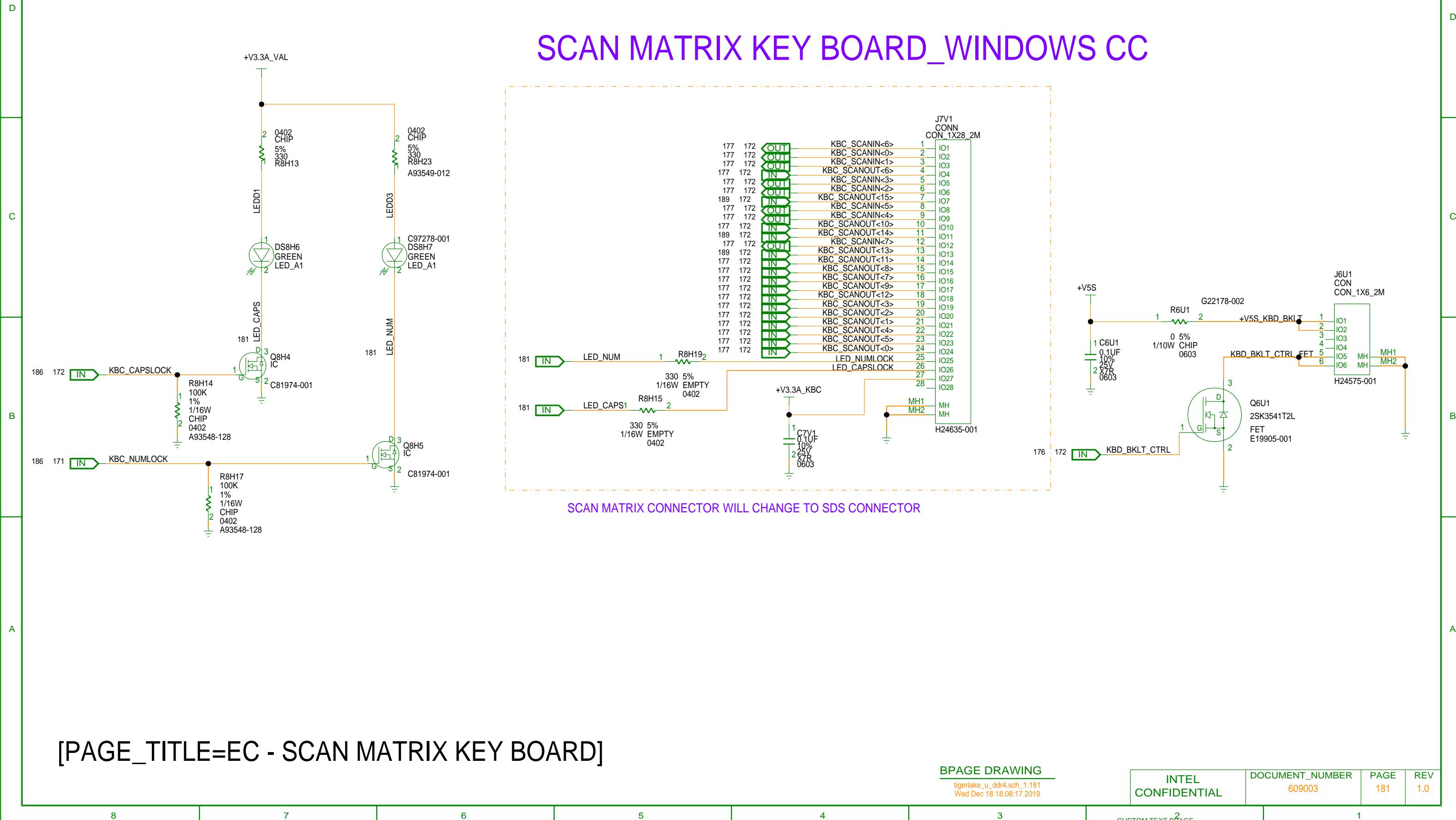
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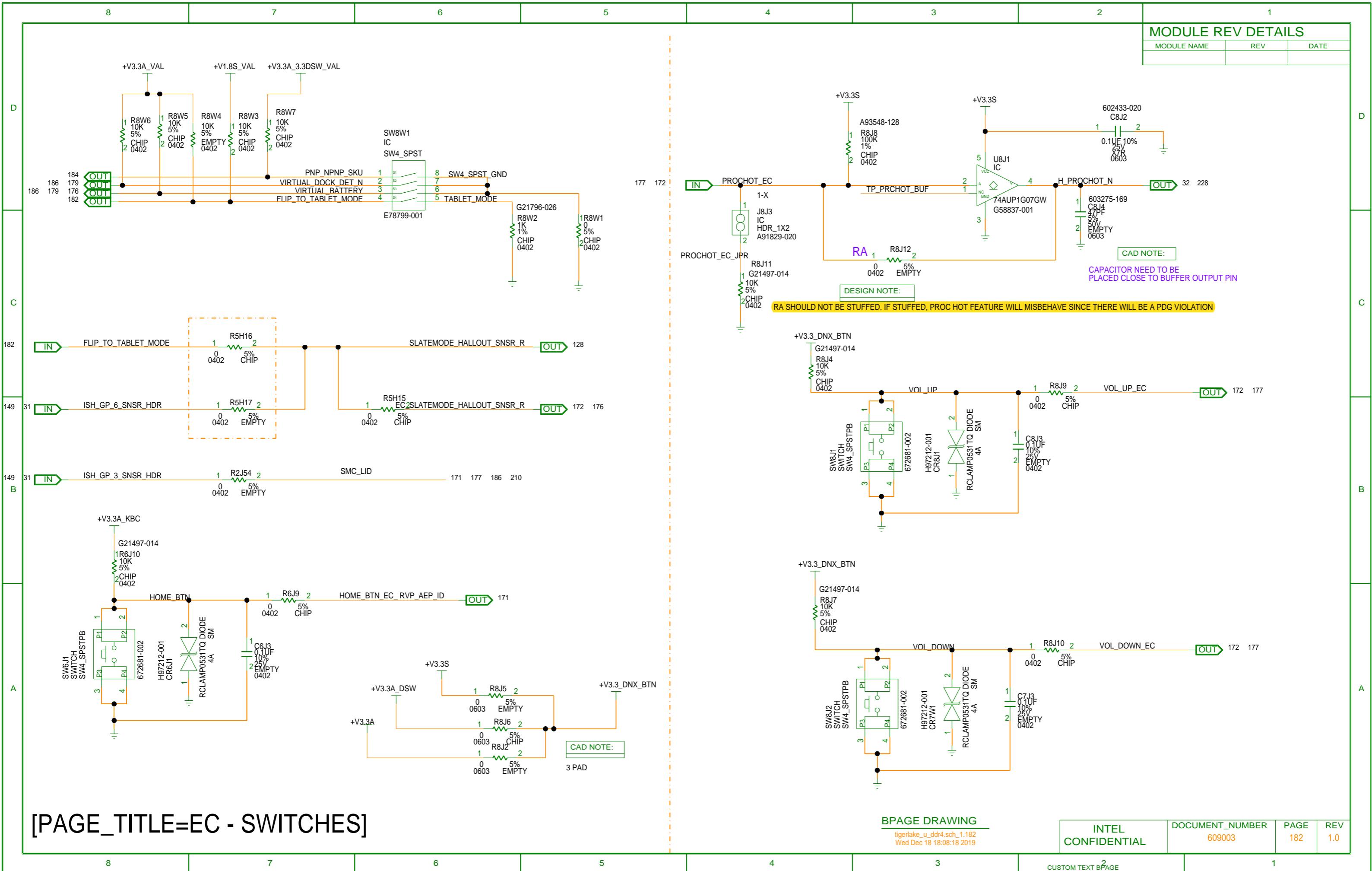
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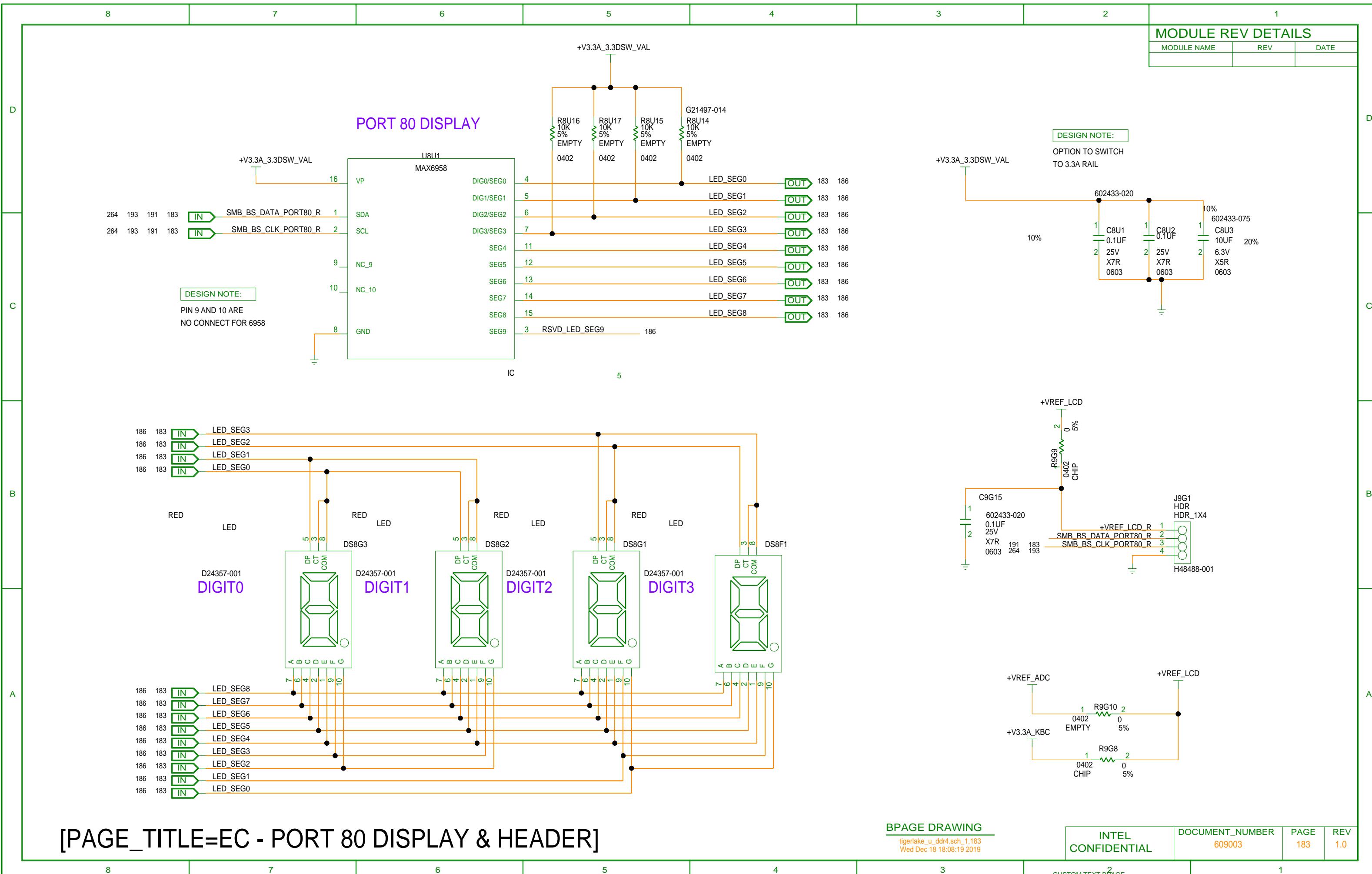
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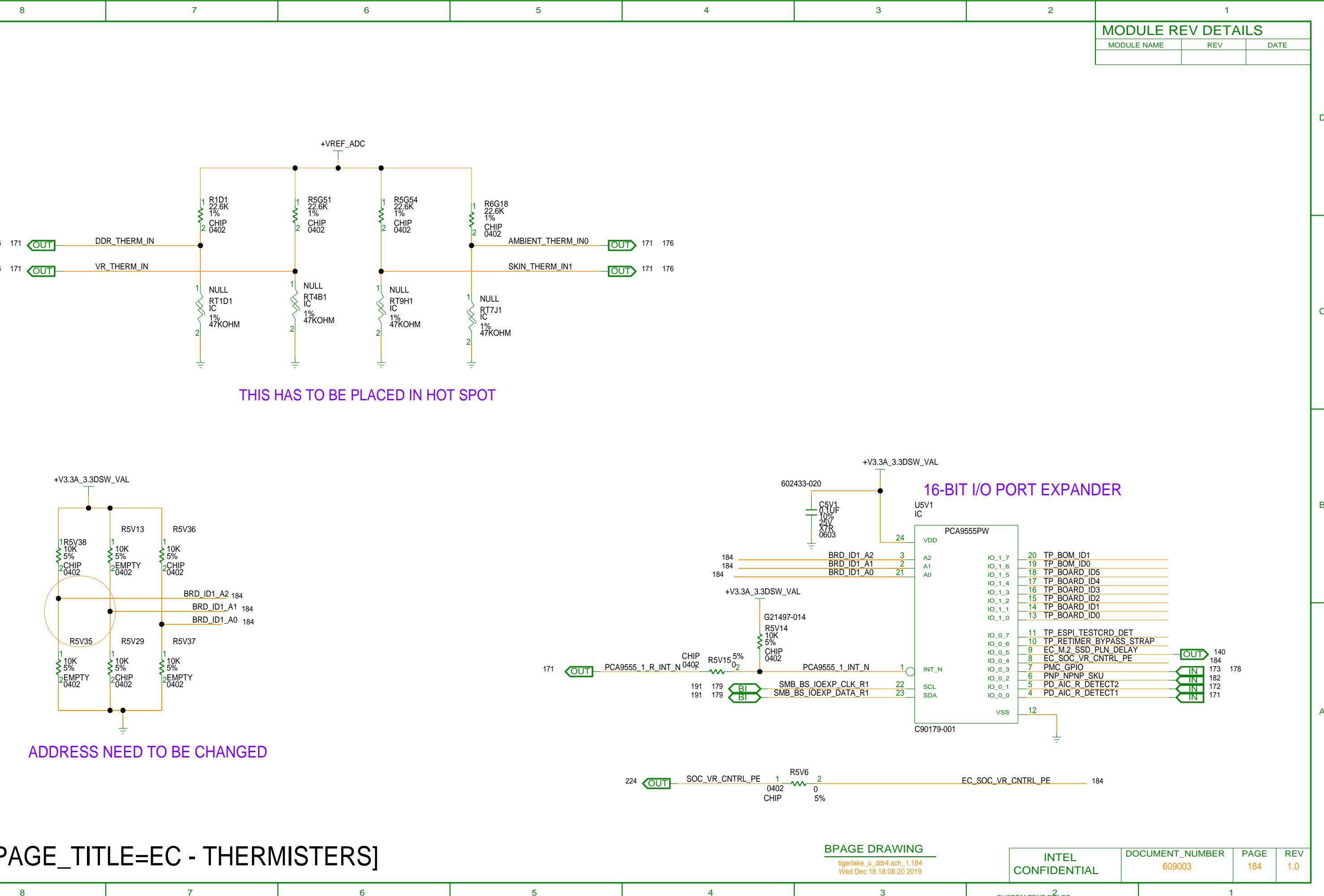


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MODULE NAME		REV	DATE				







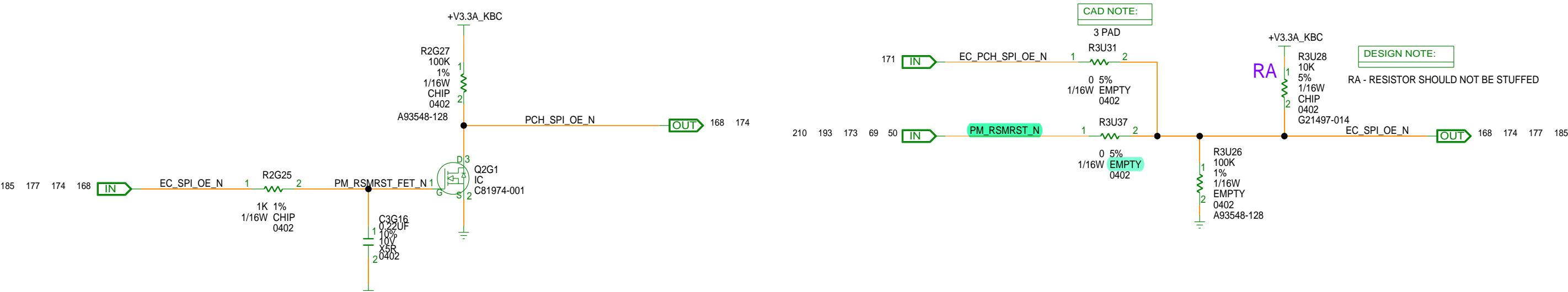
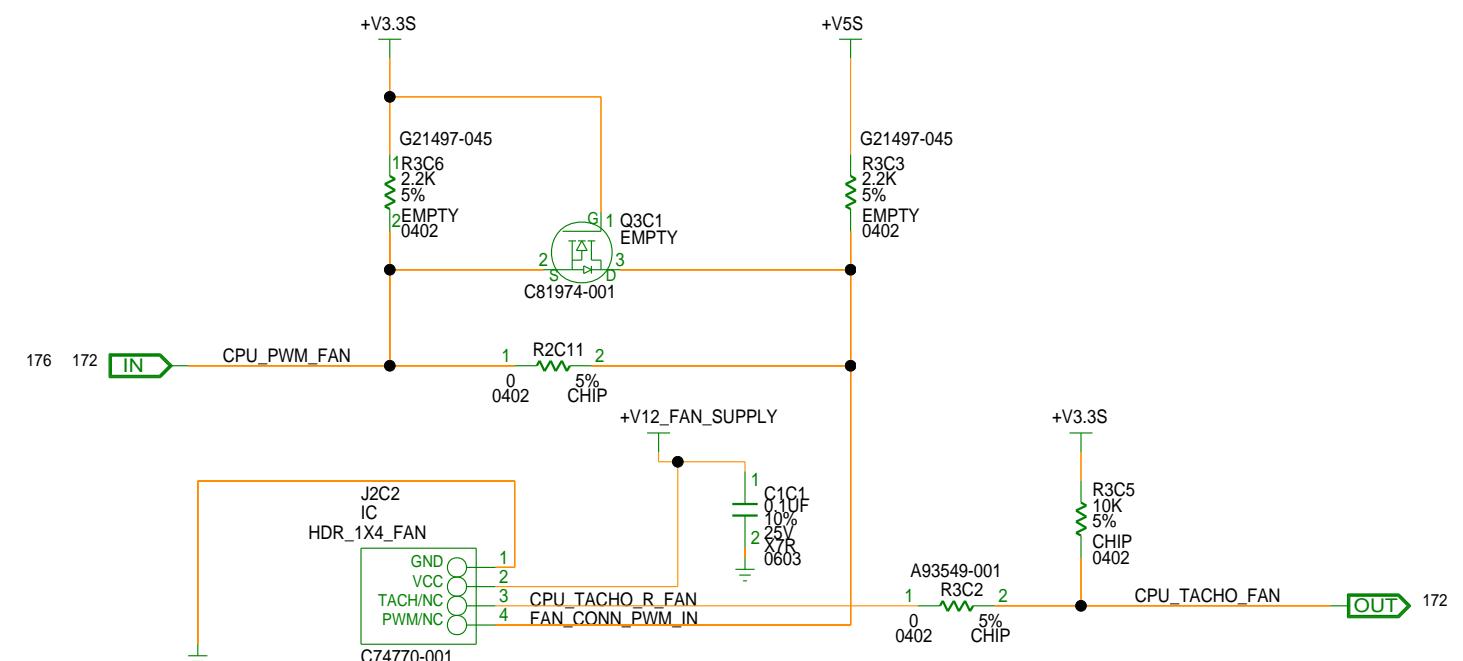


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## MODULE REV DETAILS

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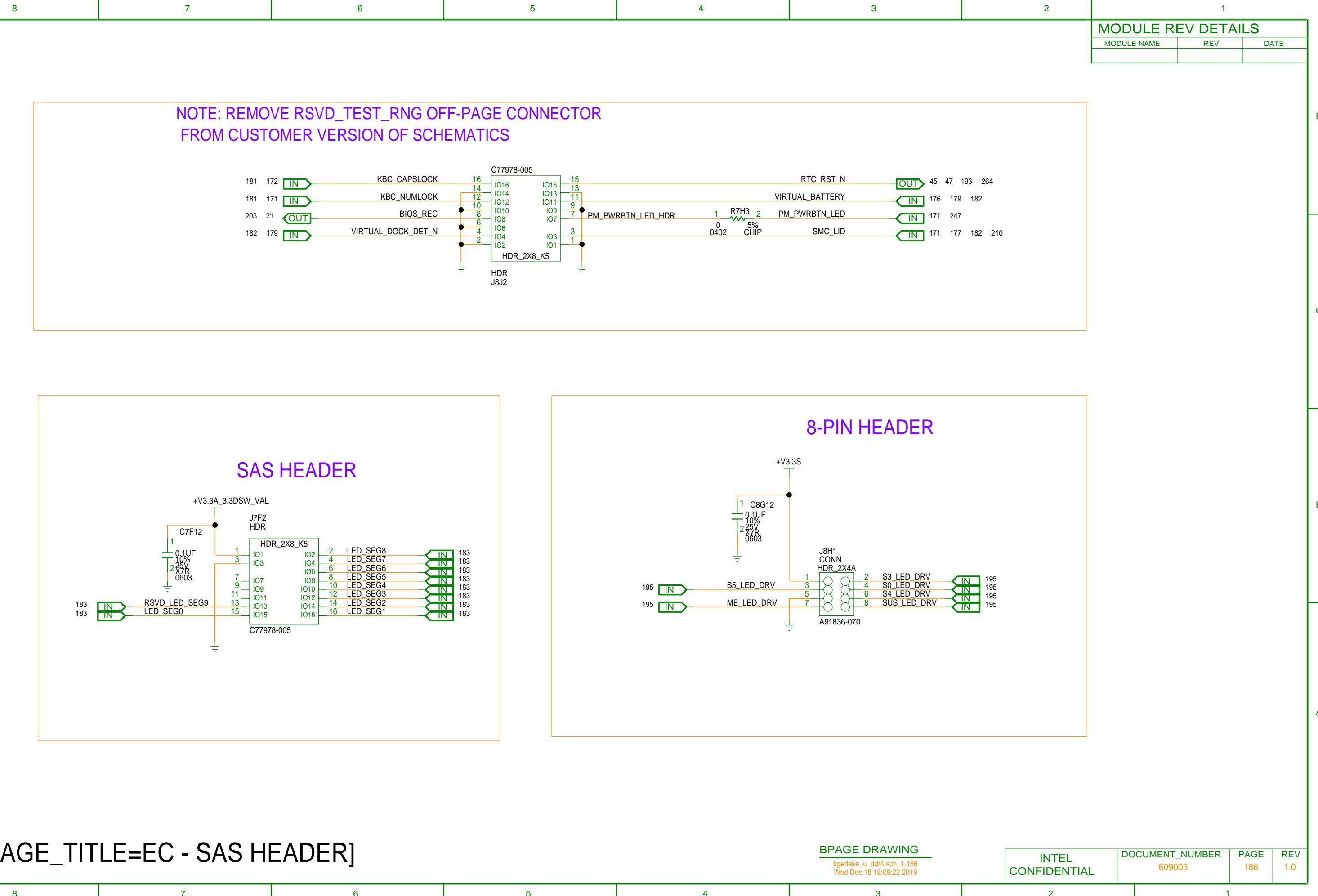
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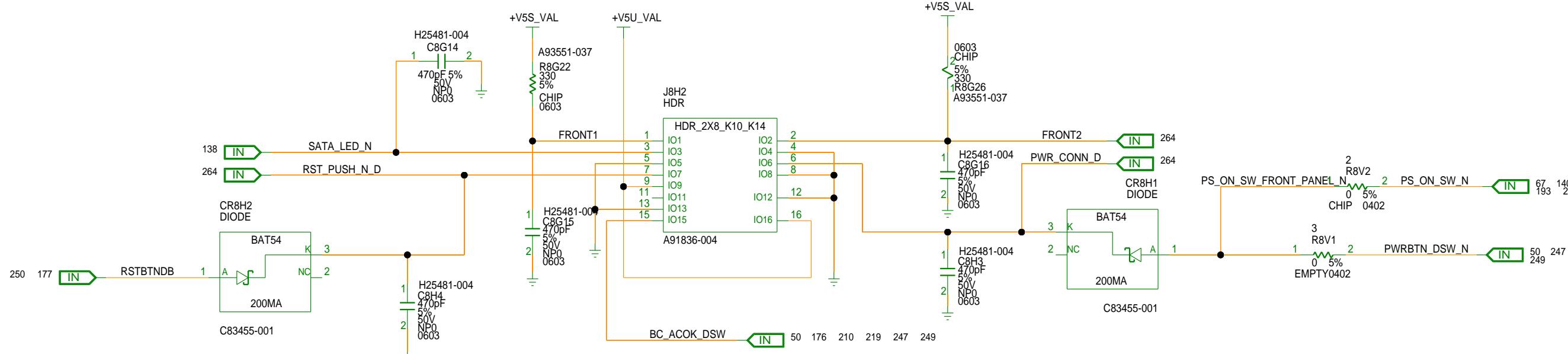
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Wed Dec 18 18:08:21 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 185	REV 1.0
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MODULE NAME						REV	DATE

## FRONT PANEL HEADER



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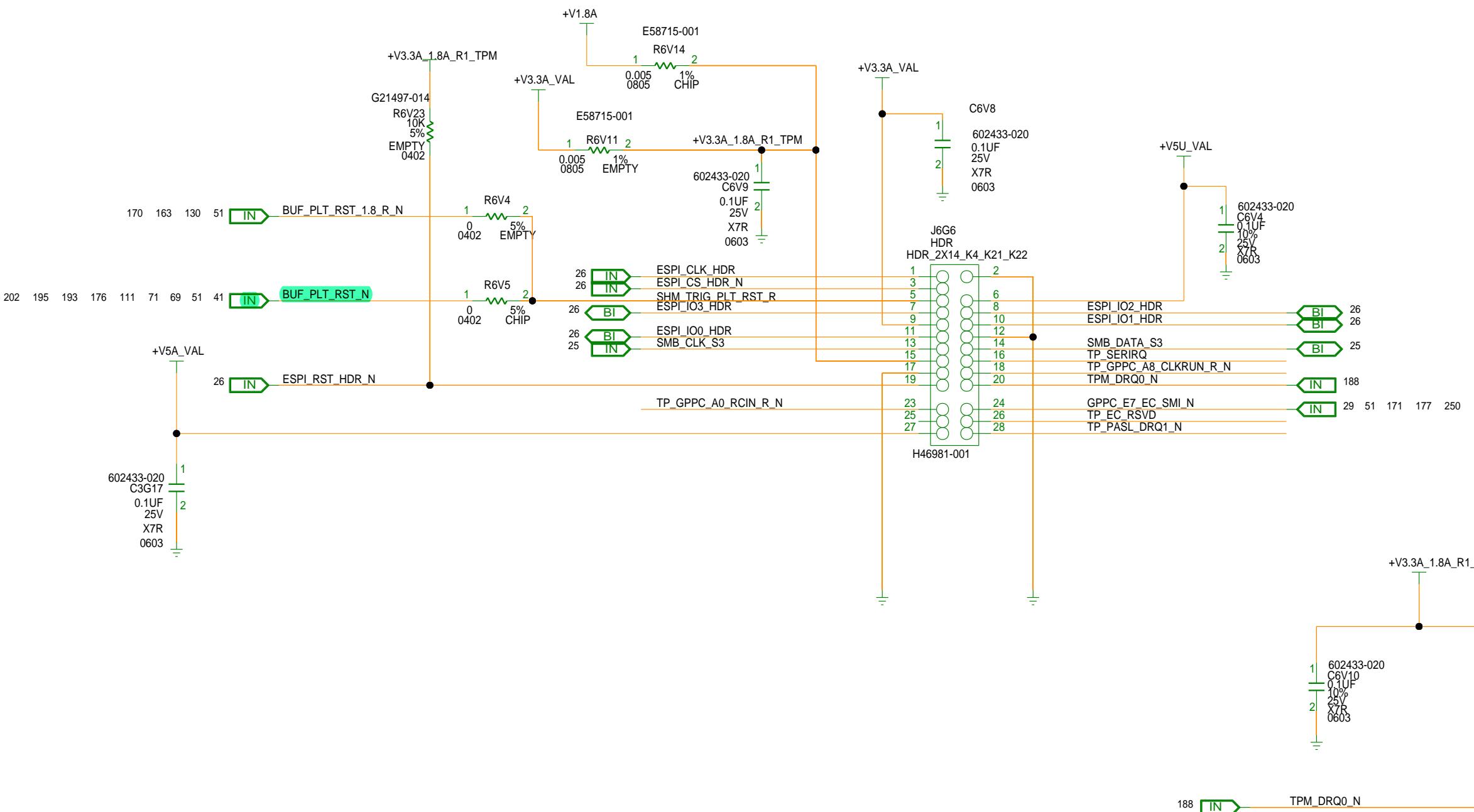
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Wed Dec 18 18:08:23 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 187	REV 1.0
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# ESPI BUS HEADER



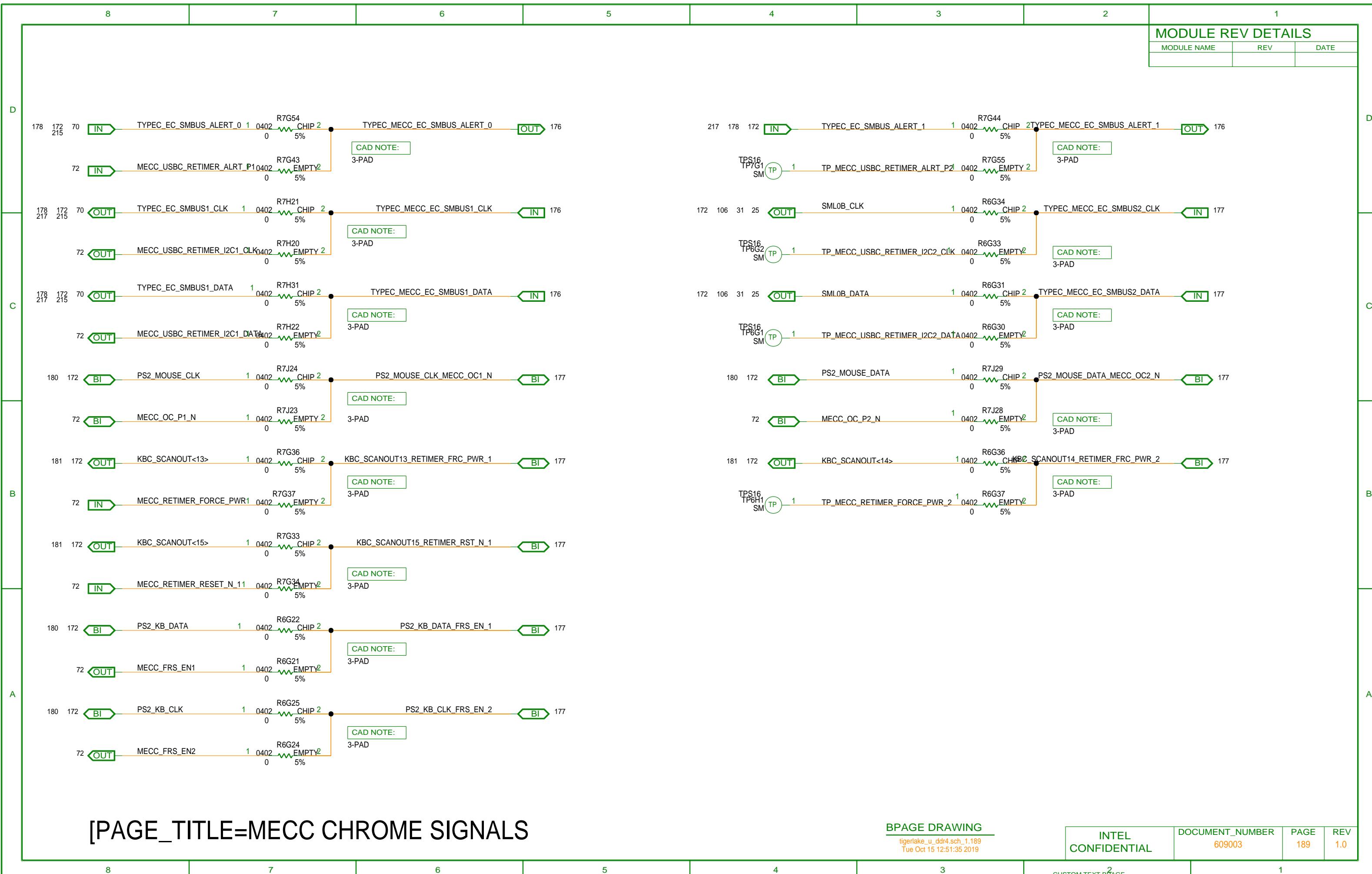
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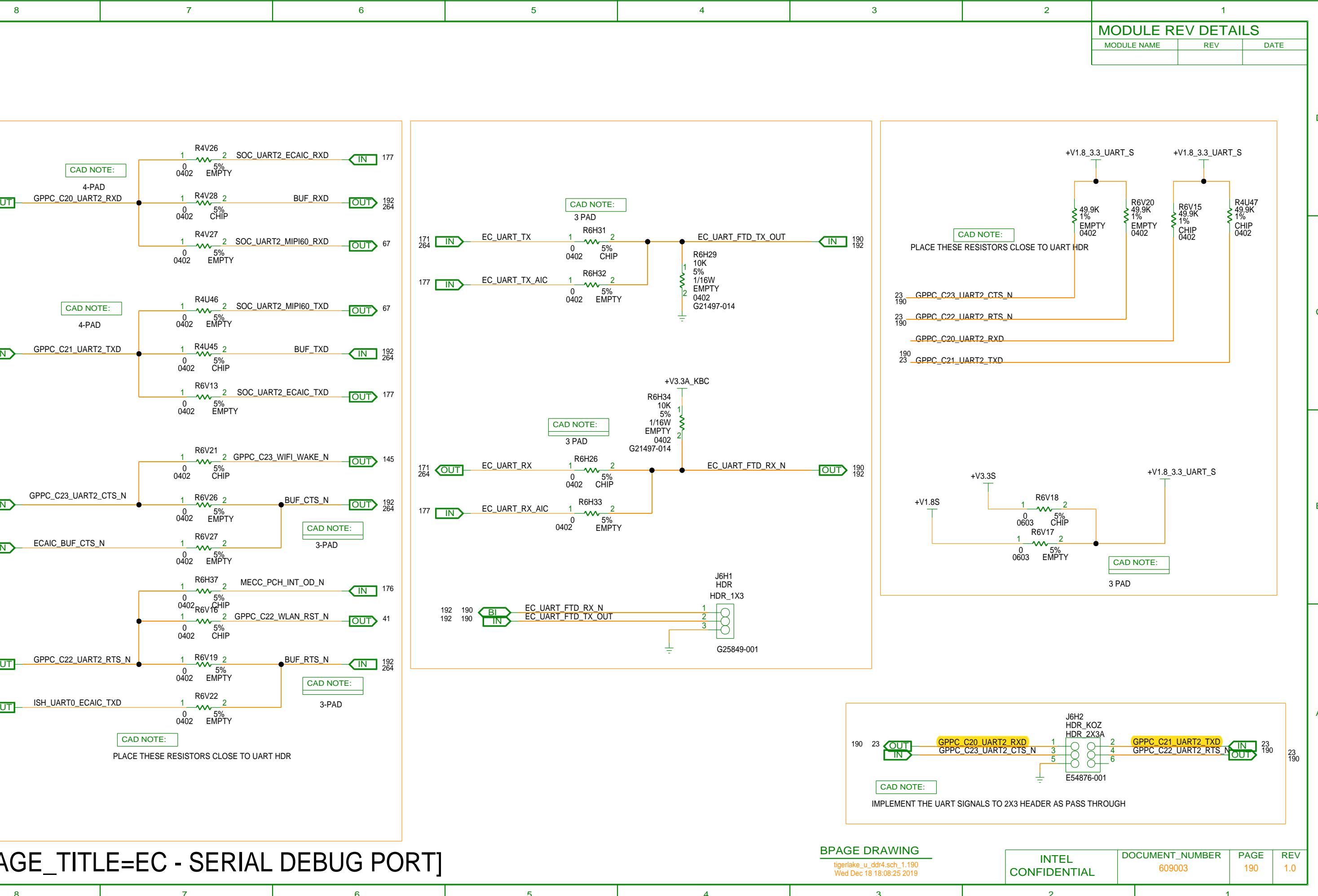
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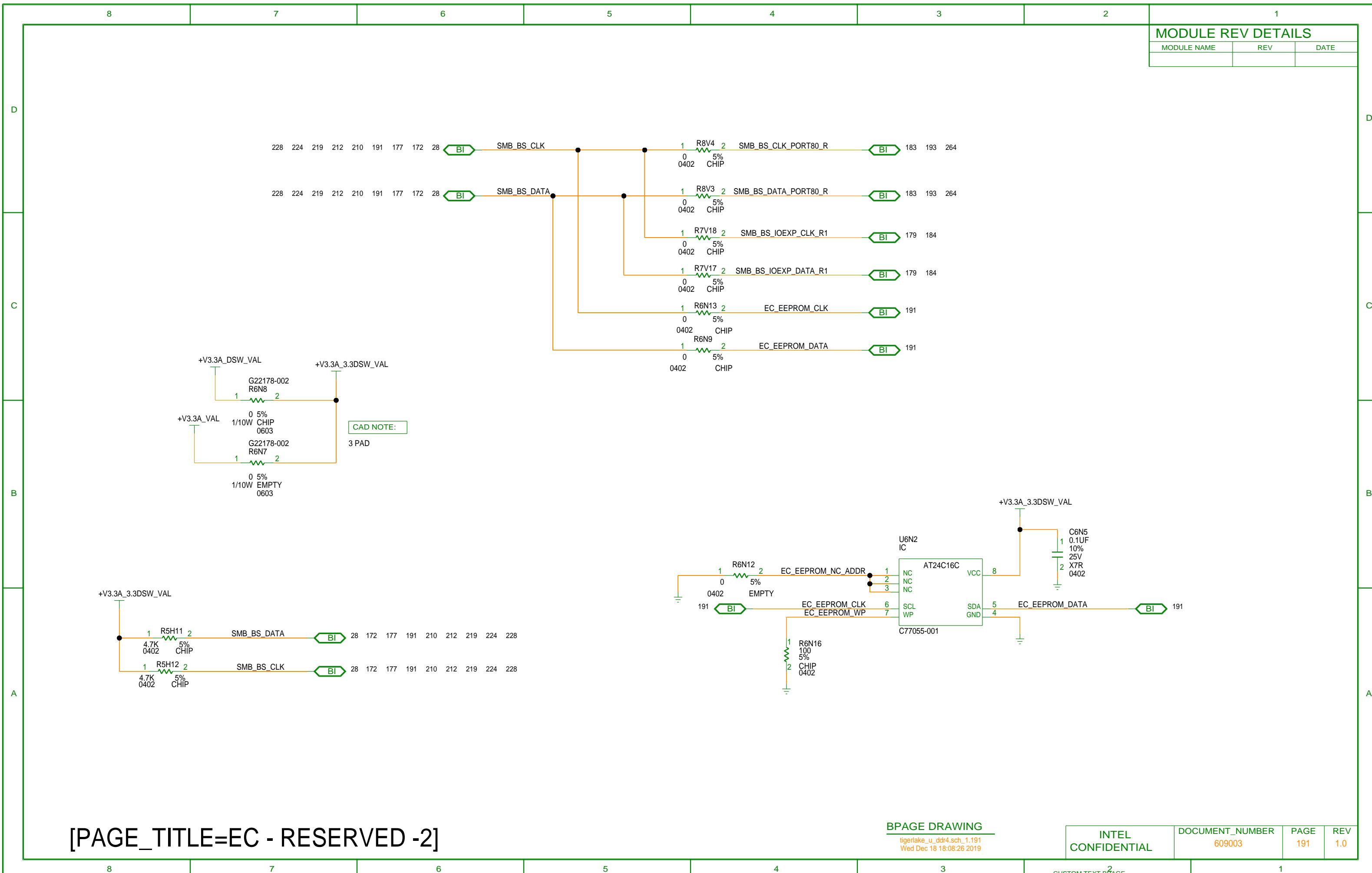
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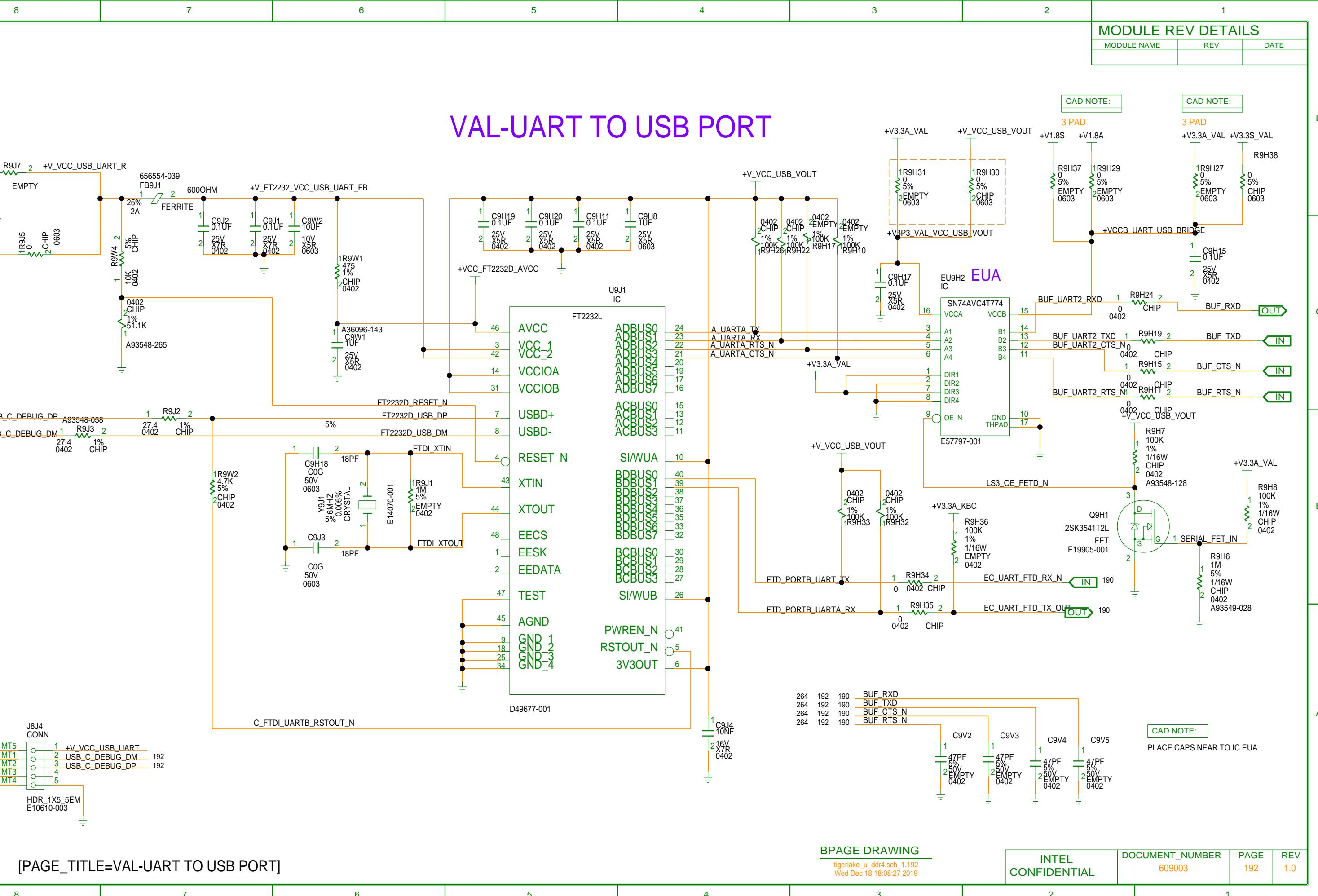
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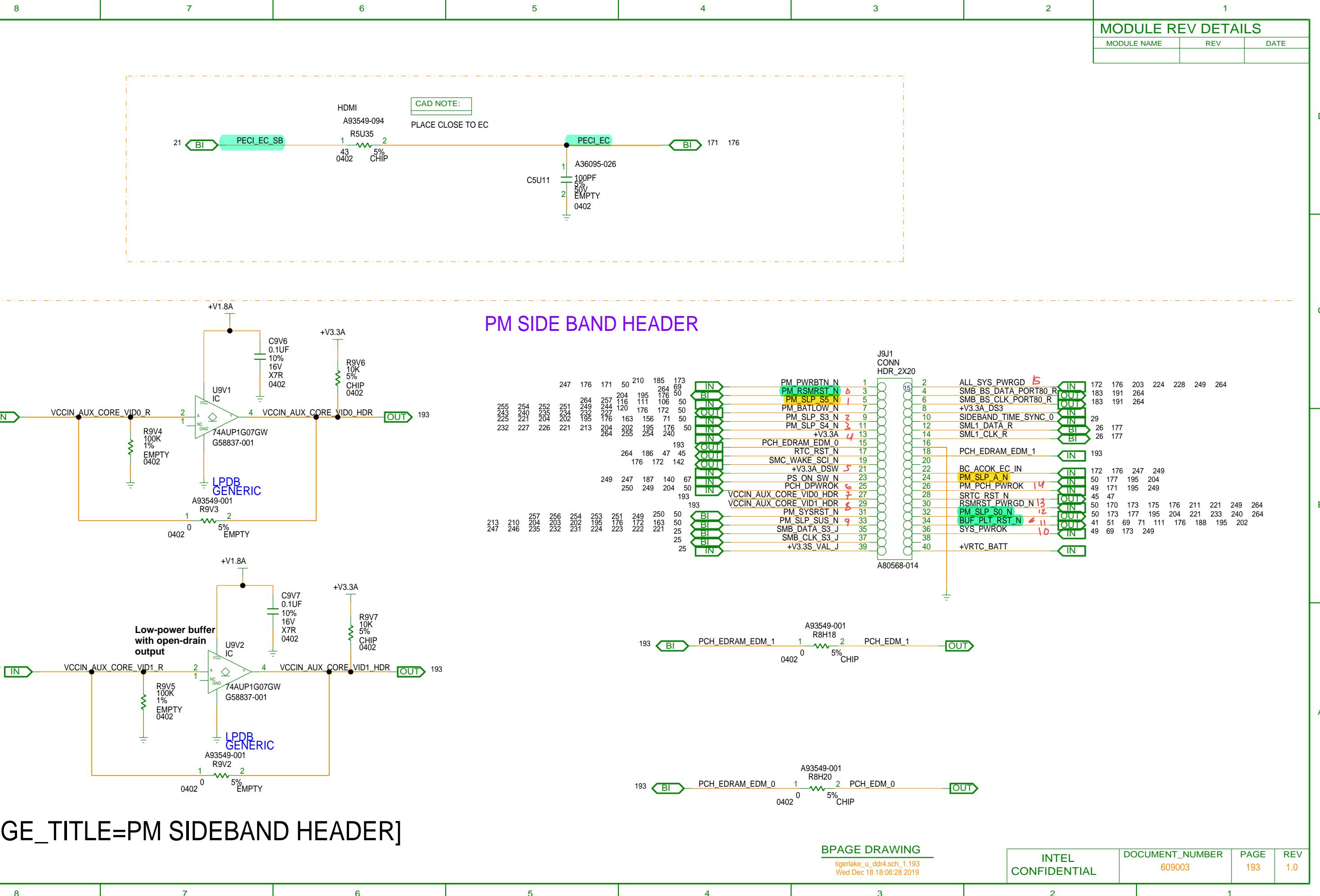
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MODULE NAME		REV	DATE				

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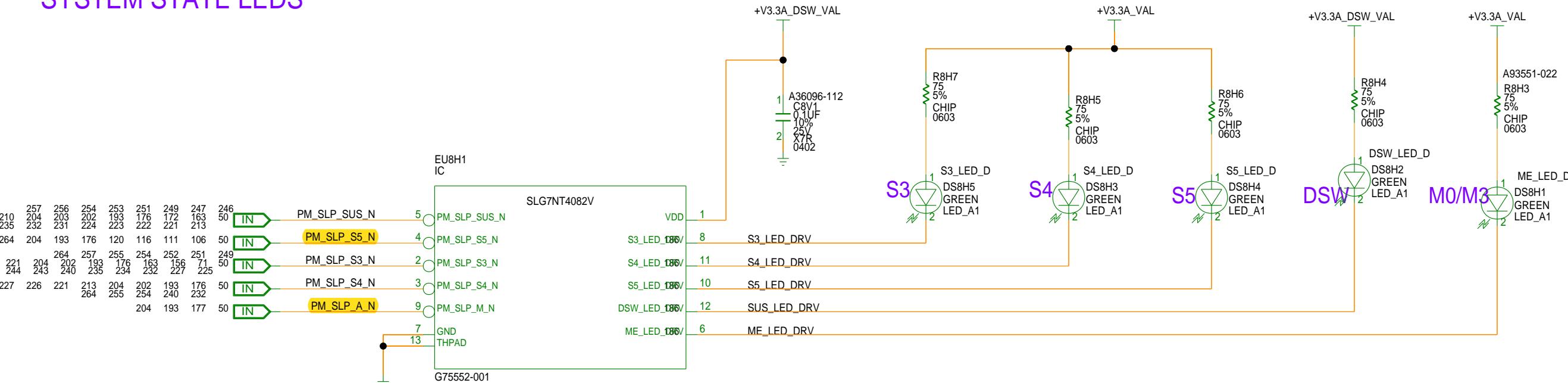
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 194	REV 1.0
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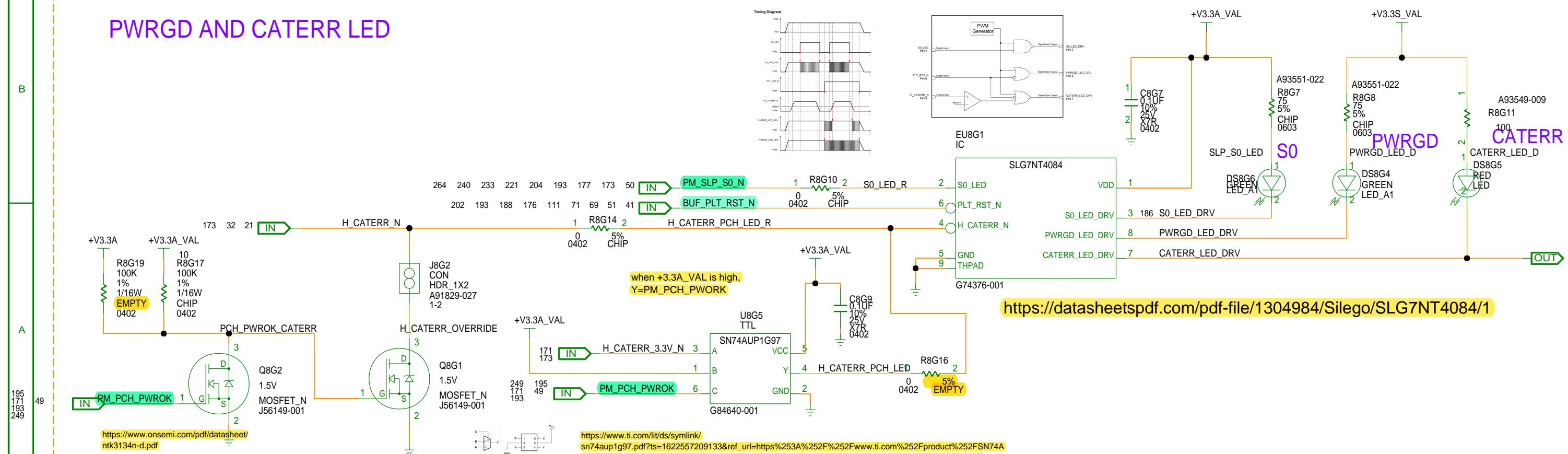
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MODULE NAME	REV	DATE

## SYSTEM STATE LEDS



## PWRGD AND CATERR LED



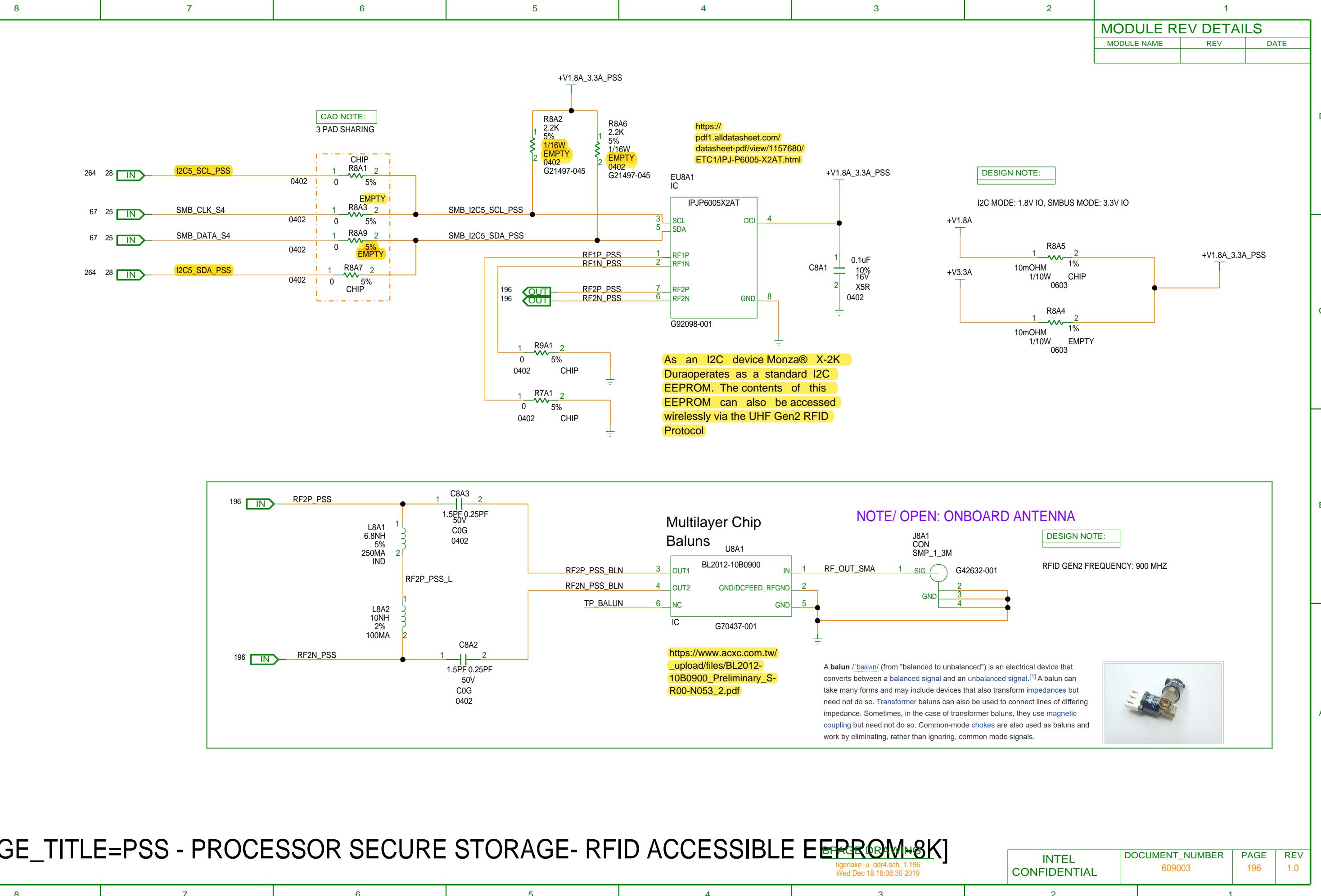
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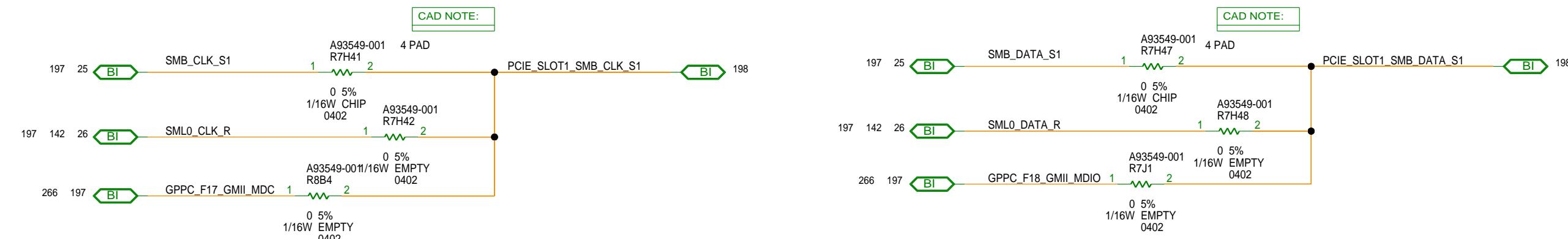
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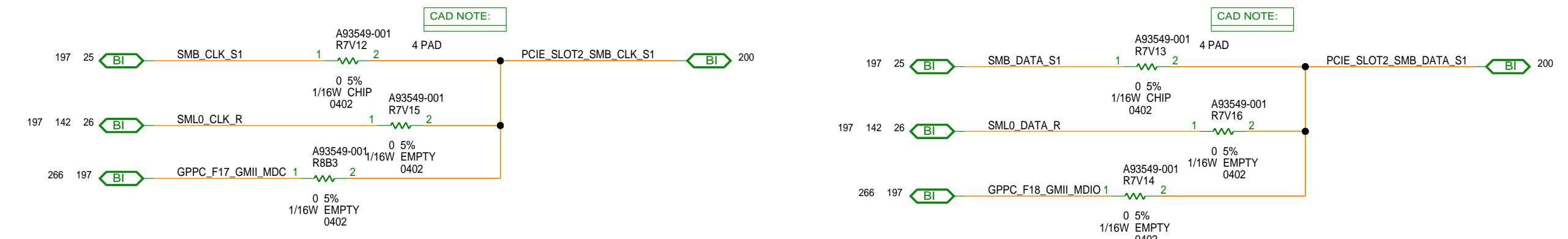


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MODULE REV DETAILS							
MODULE NAME				REV	DATE		

## PCIE SLOT 1 SMB SIGNALS



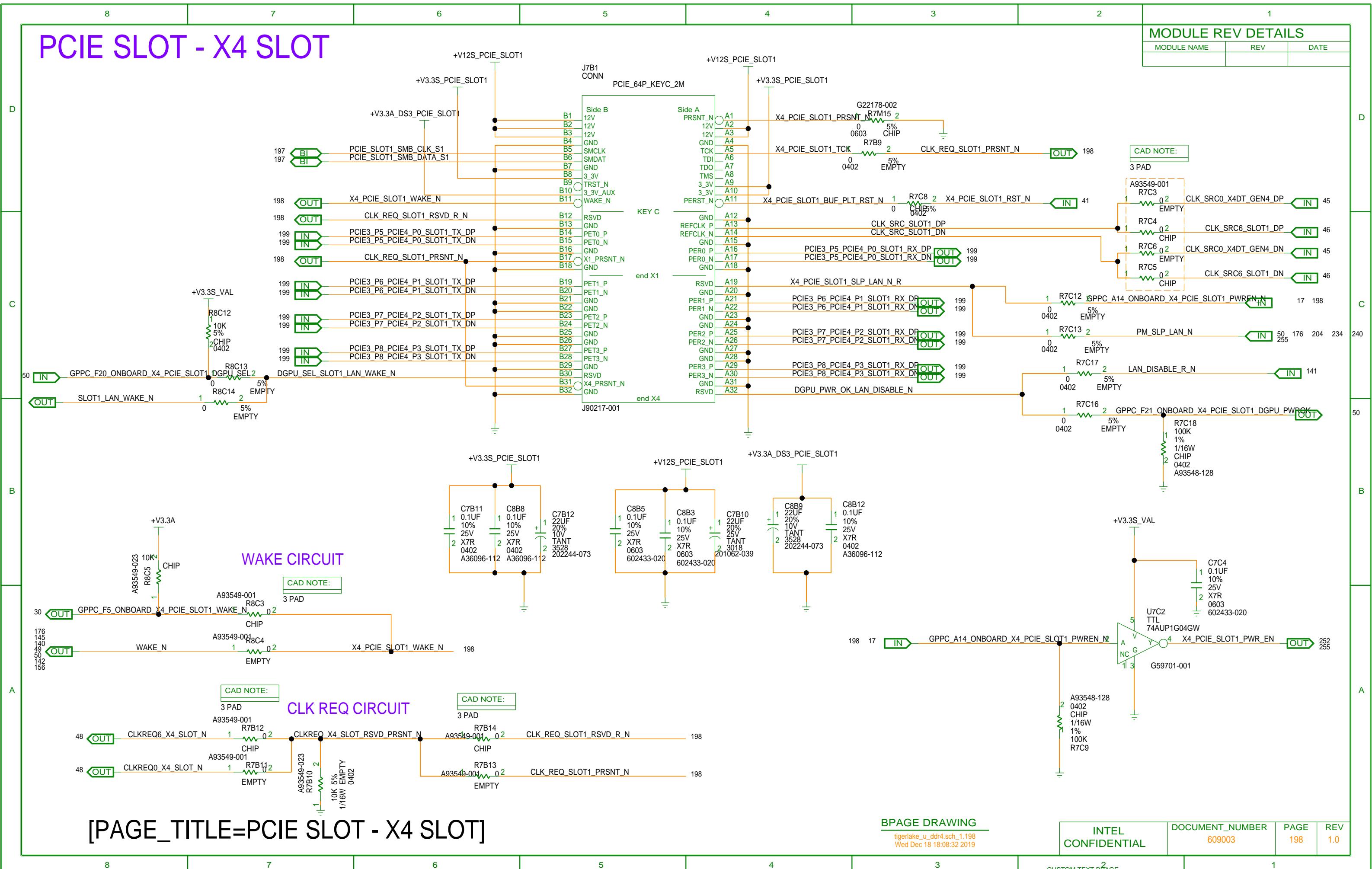
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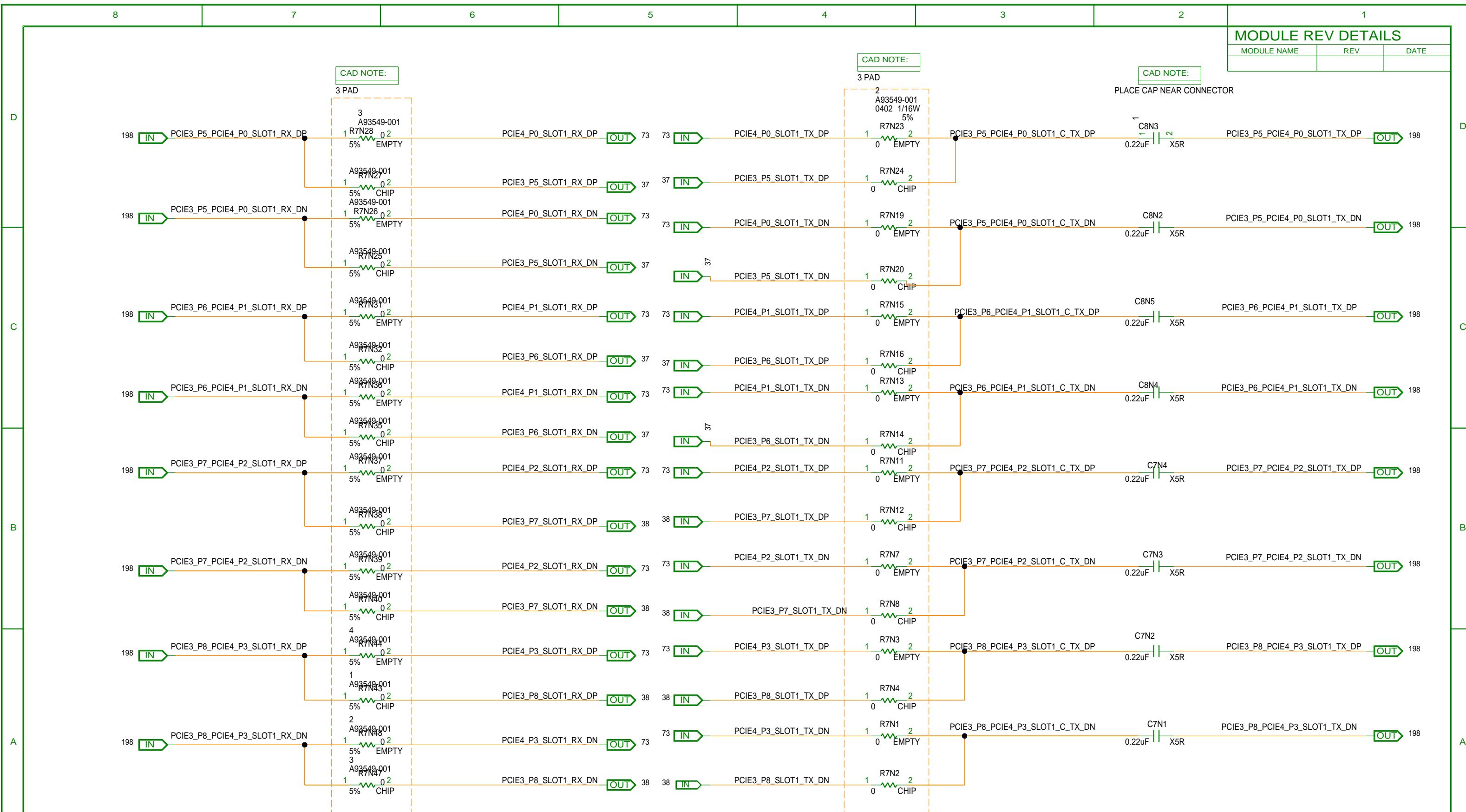


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Wed Dec 18 18:08:31 2019

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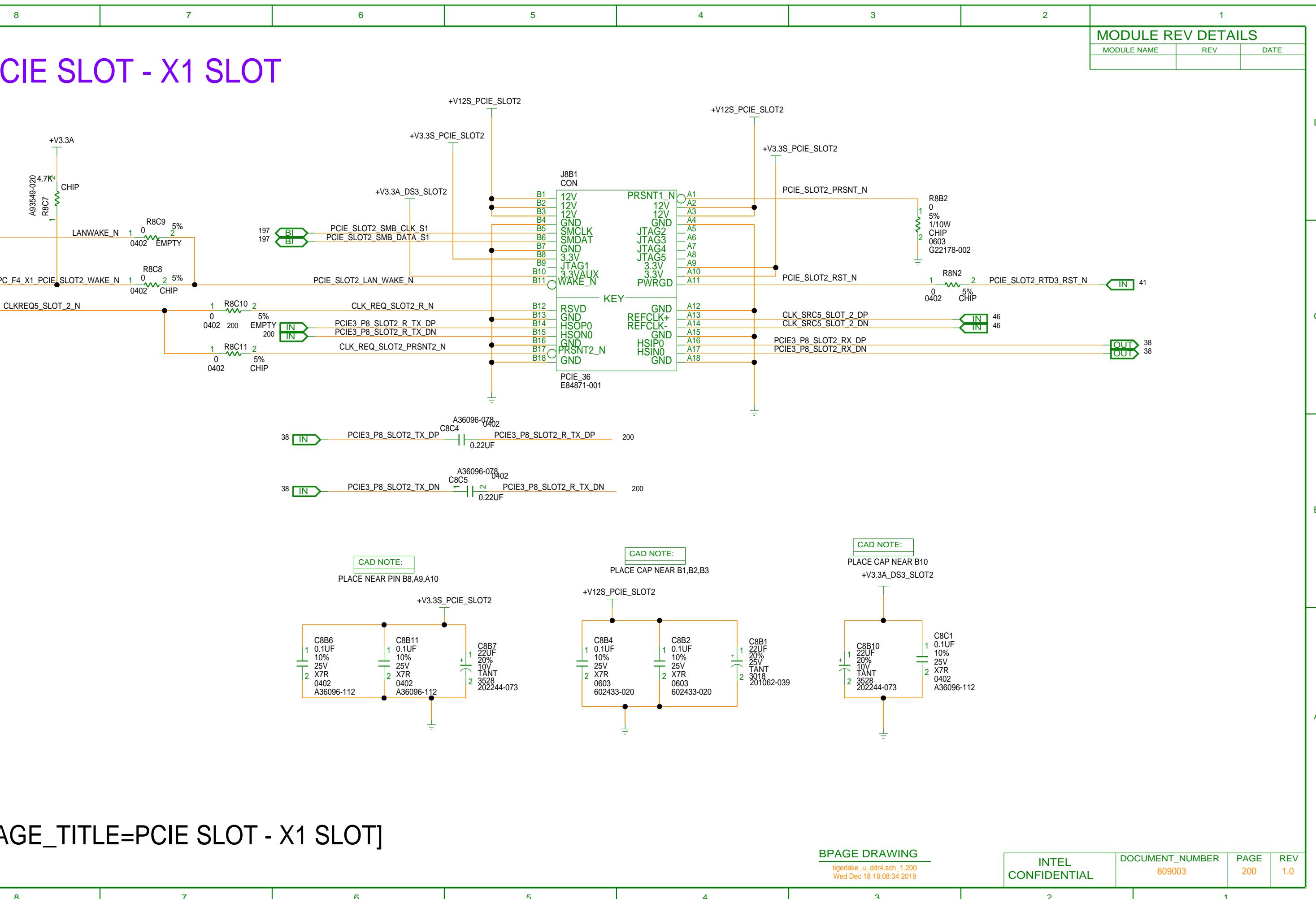
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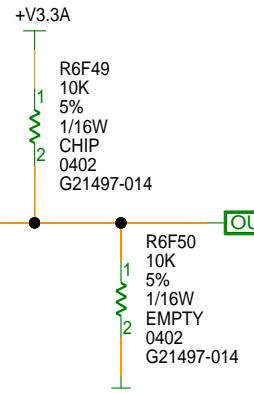
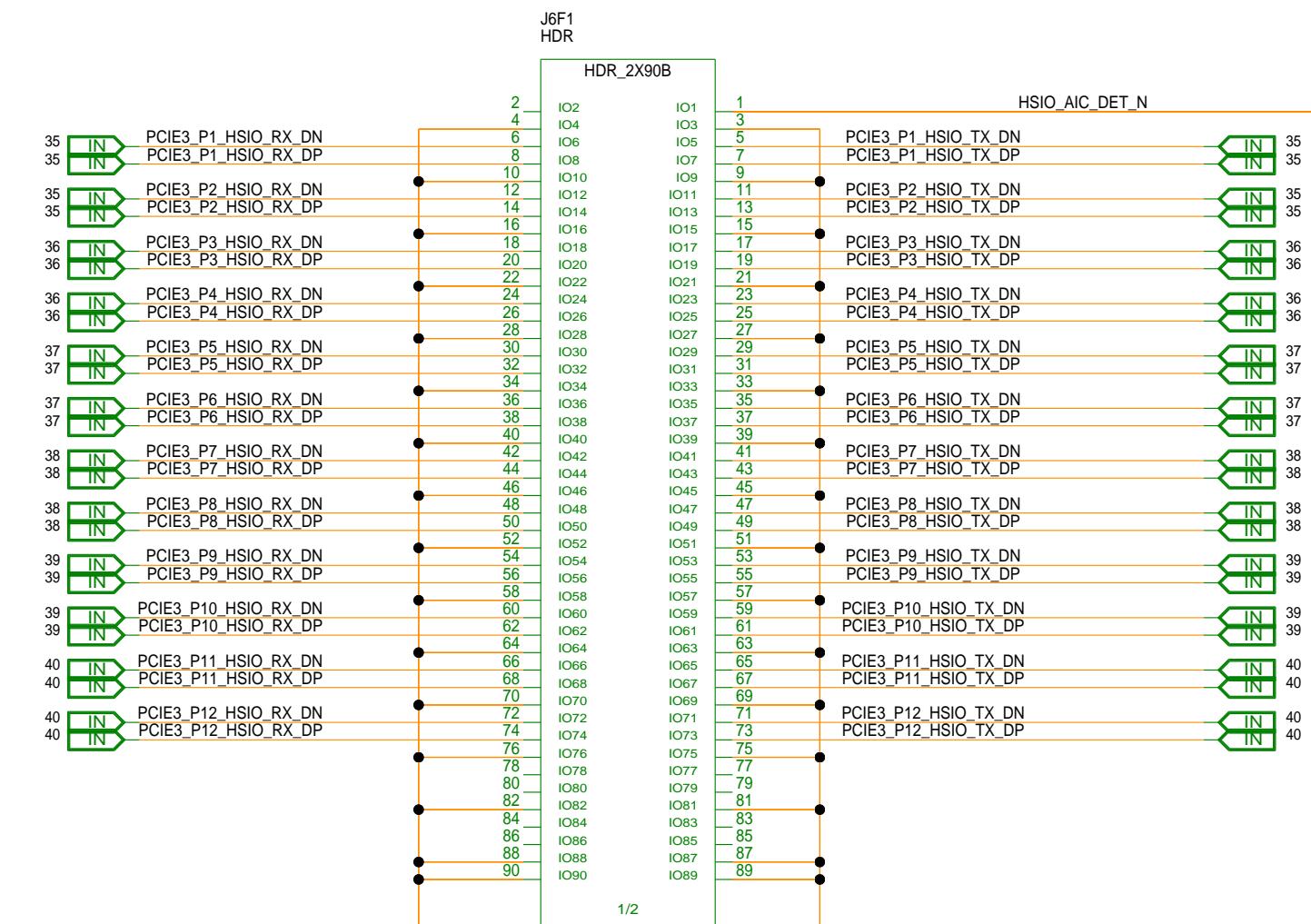
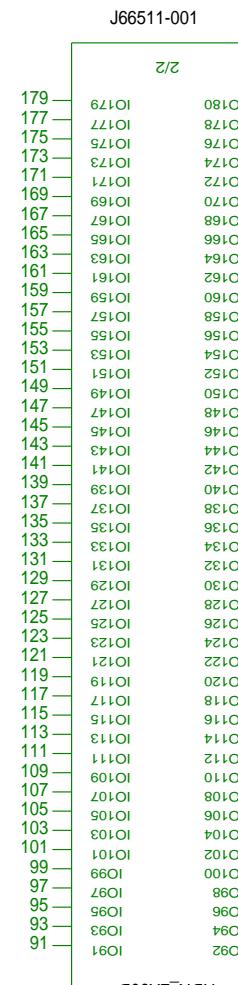
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Wed Dec 18 18:08:33 2019

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2		1	



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MODULE NAME				REV	DATE		

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV



D

D

C

C

B

B

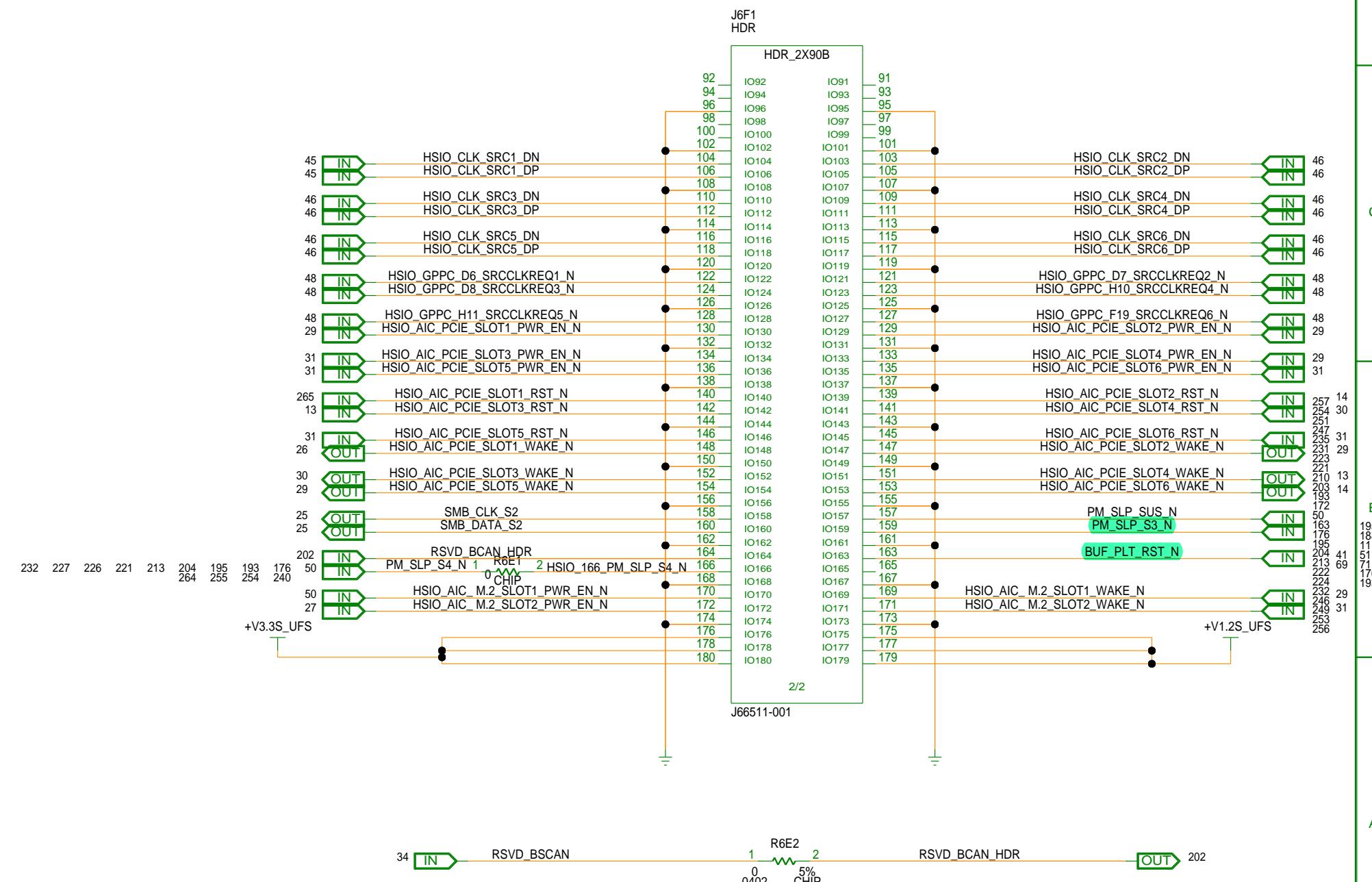
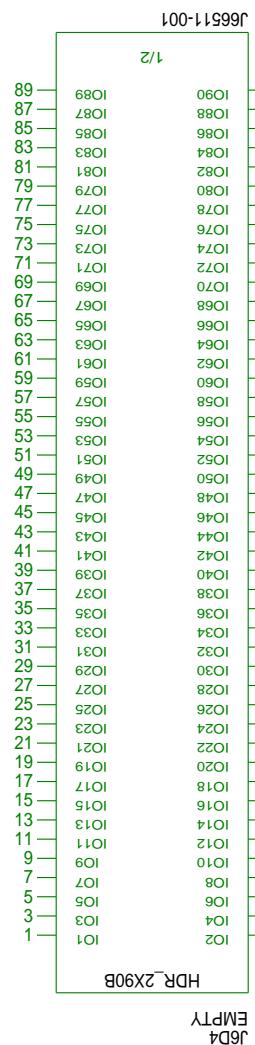
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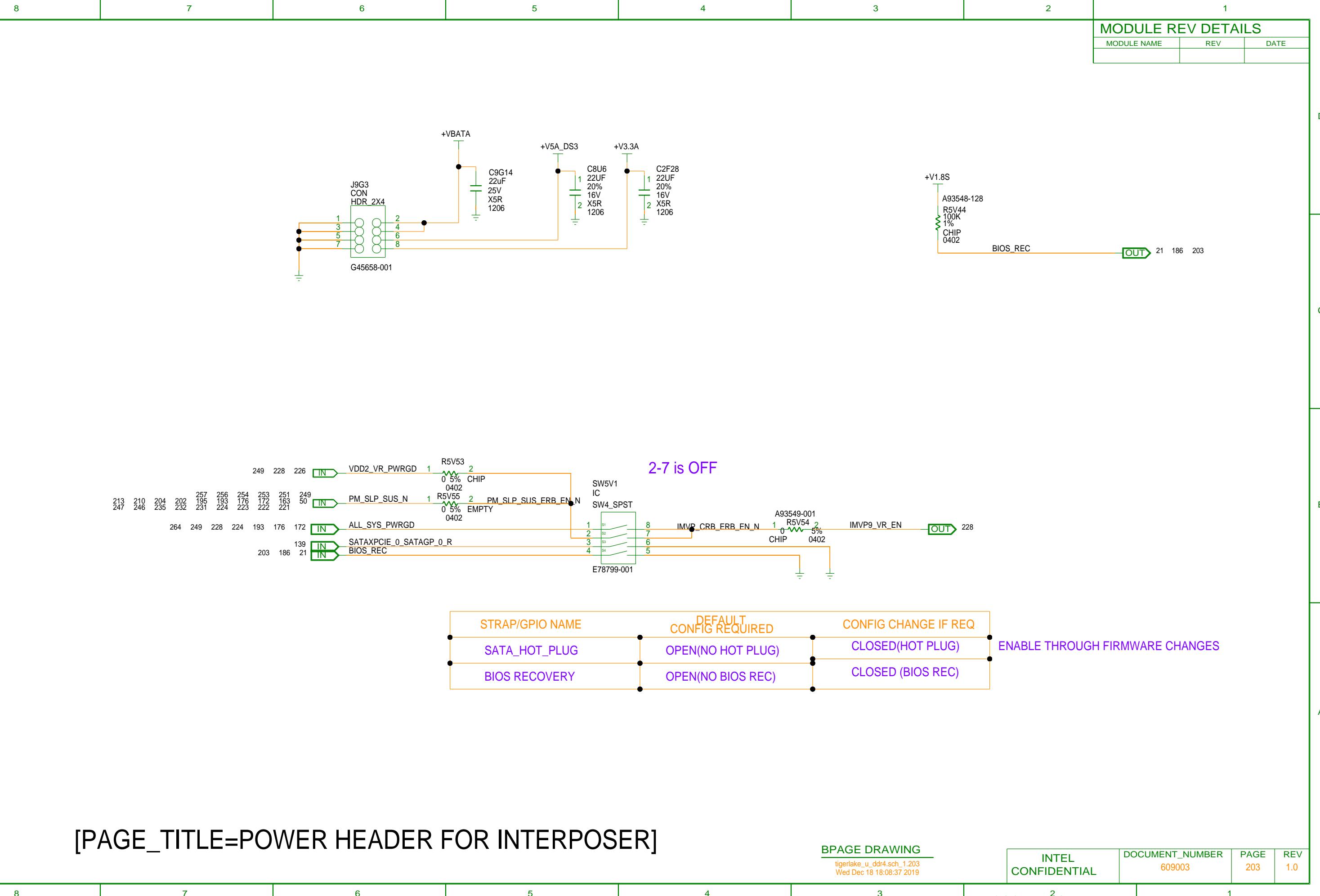
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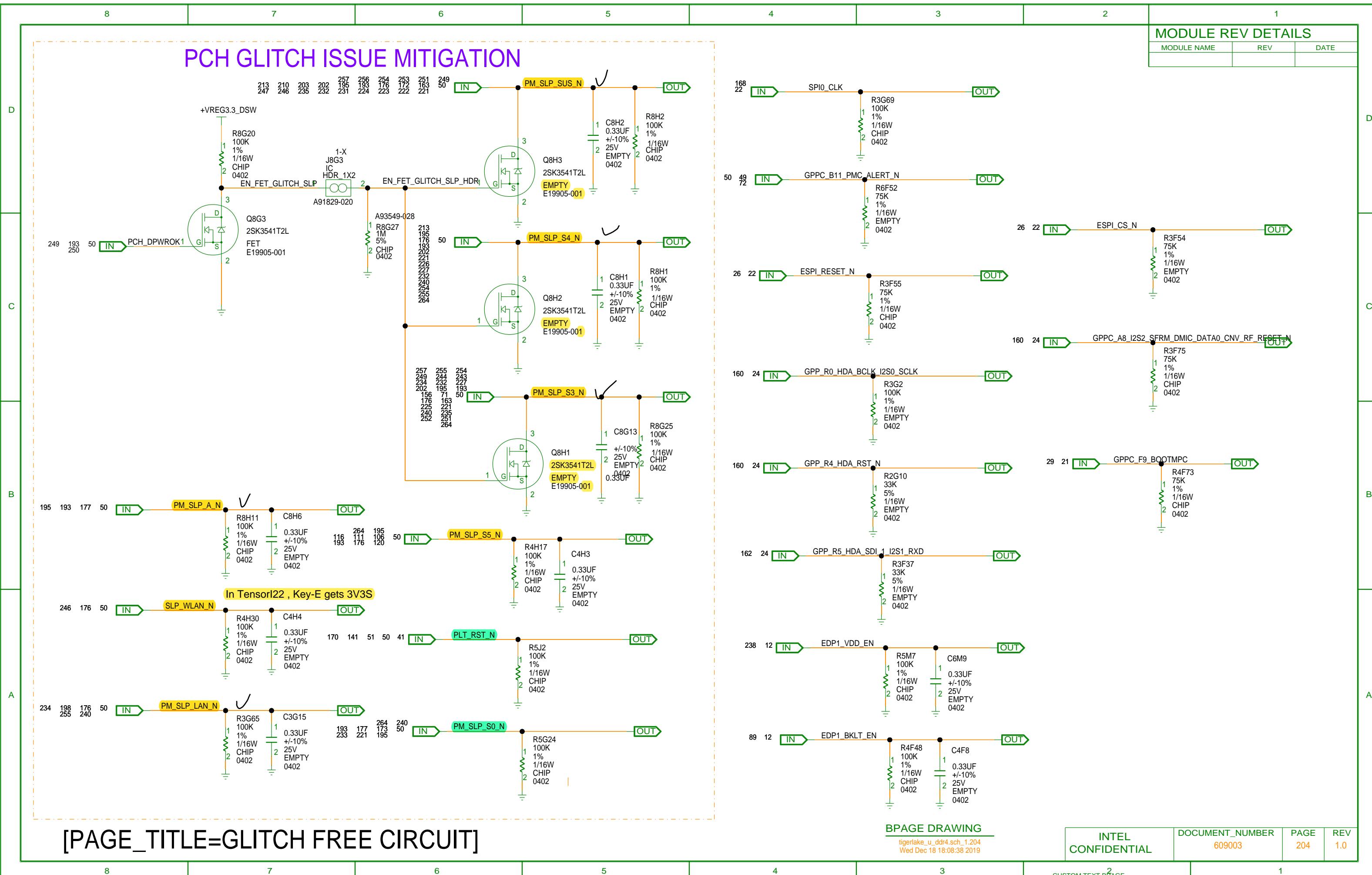
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MODULE NAME	REV	DATE

180 DEGREE REVERSE FP OVERLAP ONLY FOR PPV





# PCH GLITCH ISSUE MITIGATION



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MODULE NAME		REV	DATE				

D

D

C

C

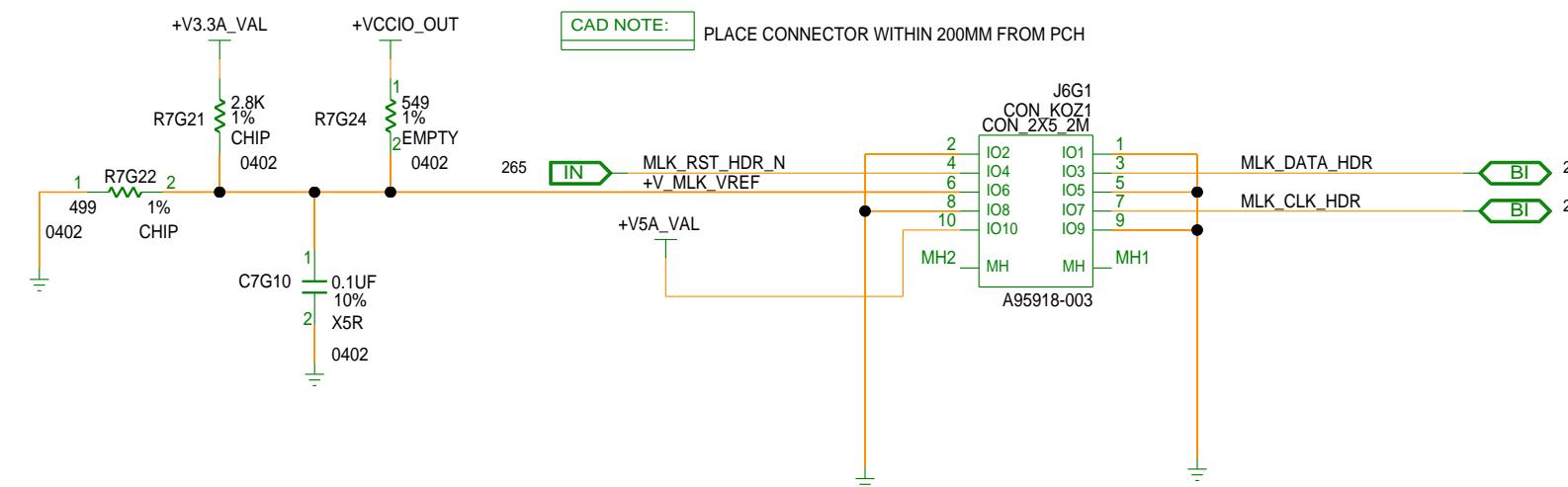
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## MLINK HEADER



[PAGE\_TITLE=MLX HEADER]

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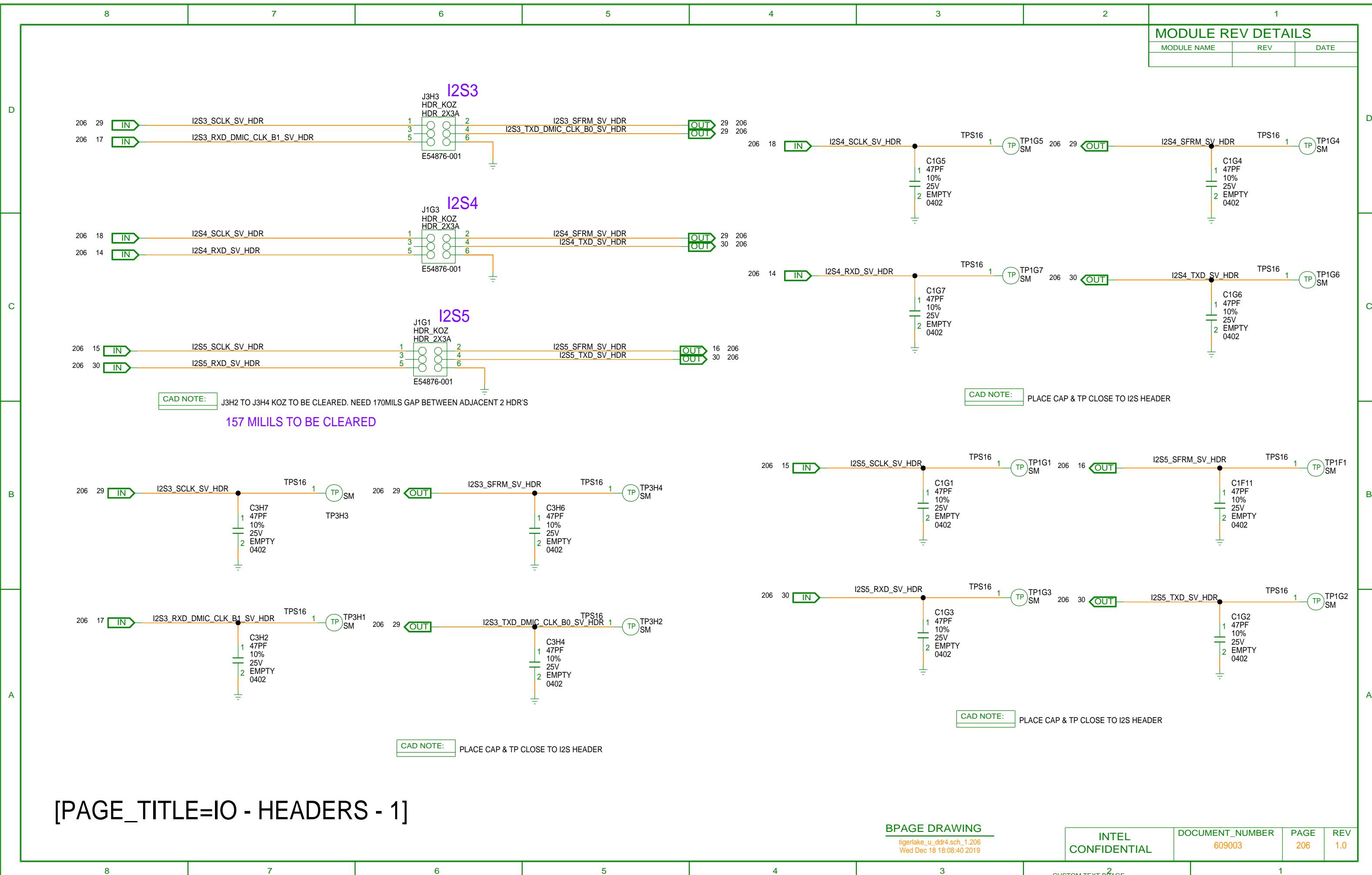
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Wed Dec 18 18:08:39 2019

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MODULE NAME	REV	DATE



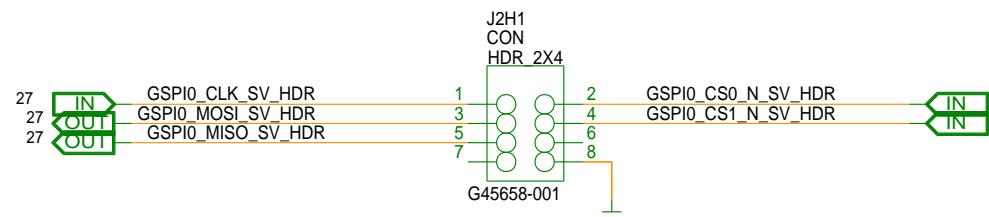
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CAD NOTE: MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

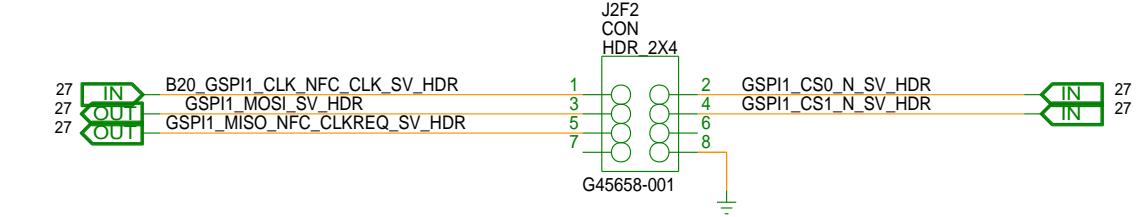
CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

CAD NOTE: PLACE CONNECTOR WITHIN 200MM FROM PCH

## GSPI0 HEADER



## GSPI1 HEADER



GSPI2 IS AVAILABLE ON ISH SPI AND ISH UART HEADER  
SPI1 IS AVAILABLE ON THC SV HEADER

8	7	6	5	4	3	2	1
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

D

D

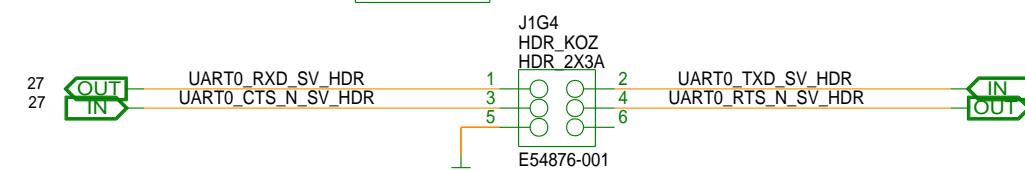
CAD NOTE:

MAINTAIN 5MM GAP BETWEEN THE CONNECTORS IN THIS PAGE

## LPSS UART0 HEADER

CAD NOTE:

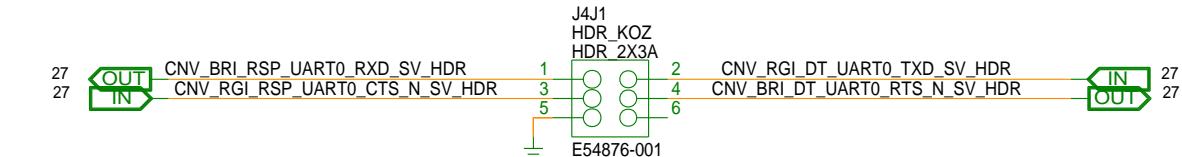
PLACE CONNECTOR WITHIN 300MM FROM PCH



## CNV UART0 HEADER

CAD NOTE:

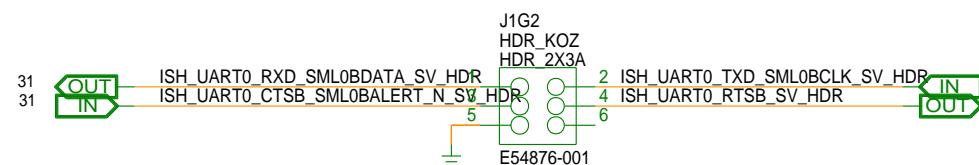
PLACE CONNECTOR WITHIN 300MM FROM PCH



## ISH UART0 / SMLINK0B HEADER

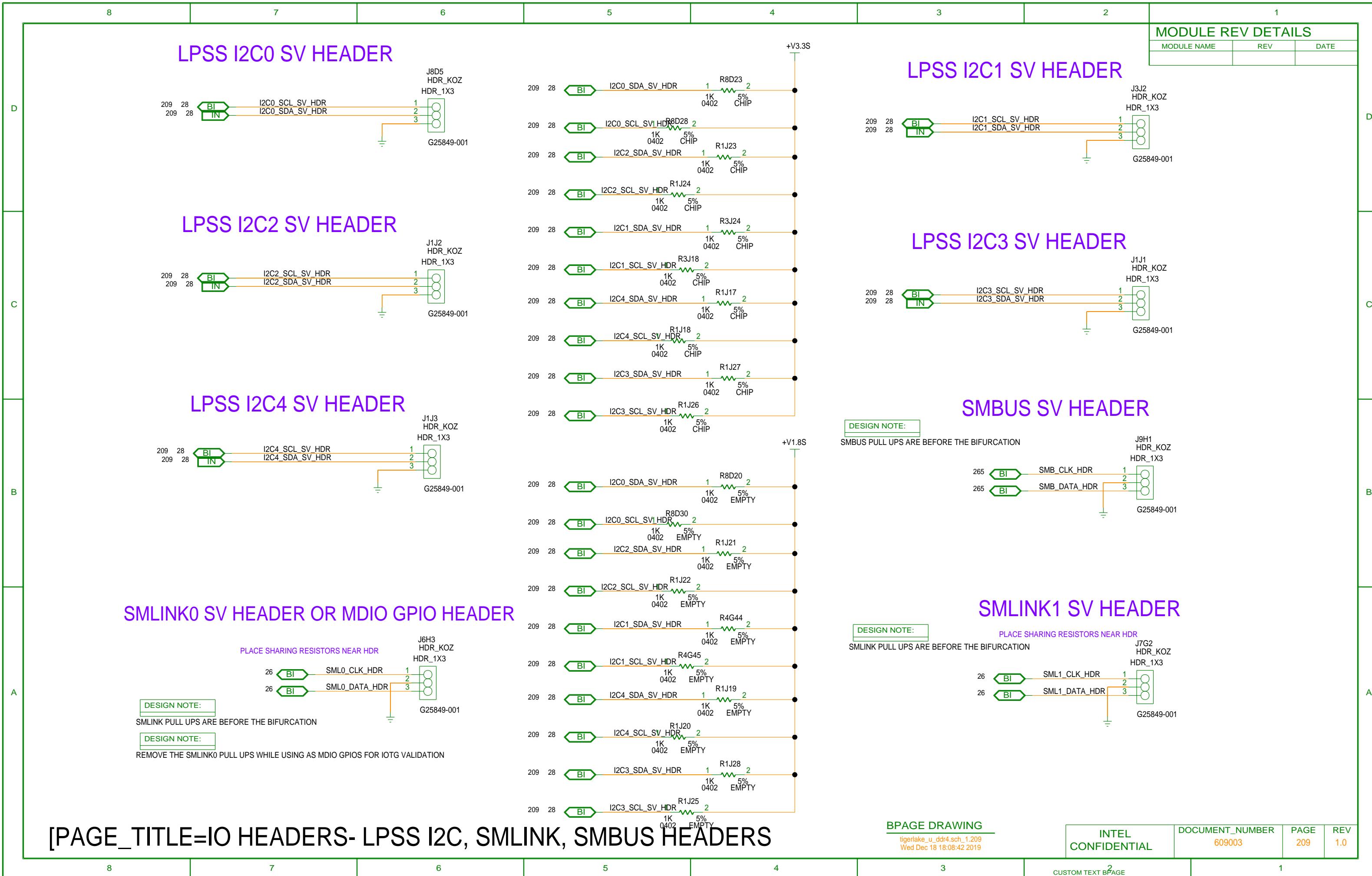
CAD NOTE:

PLACE CONNECTOR WITHIN 300MM FROM PCH



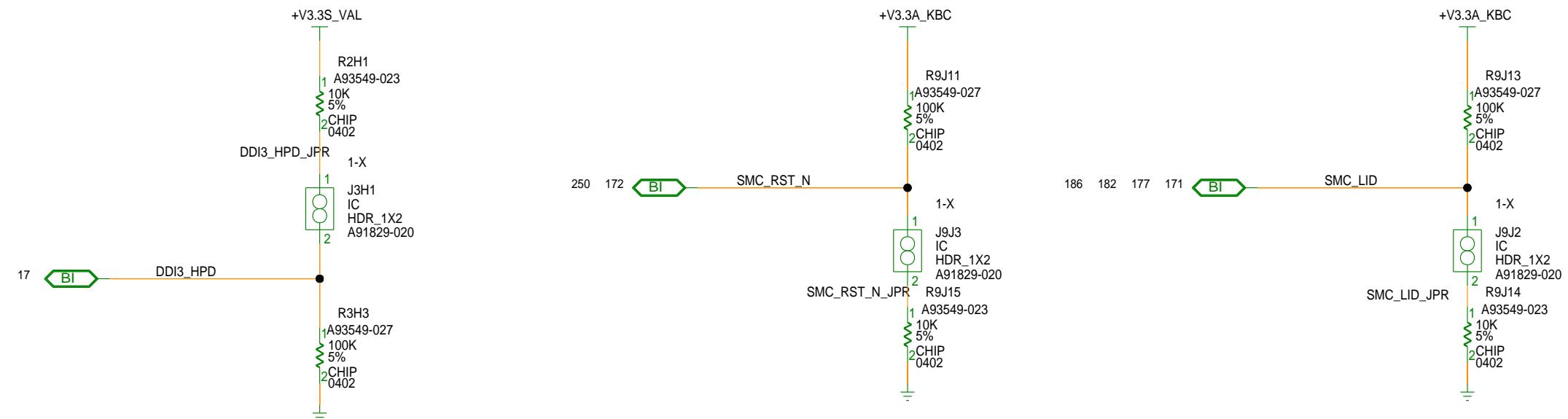
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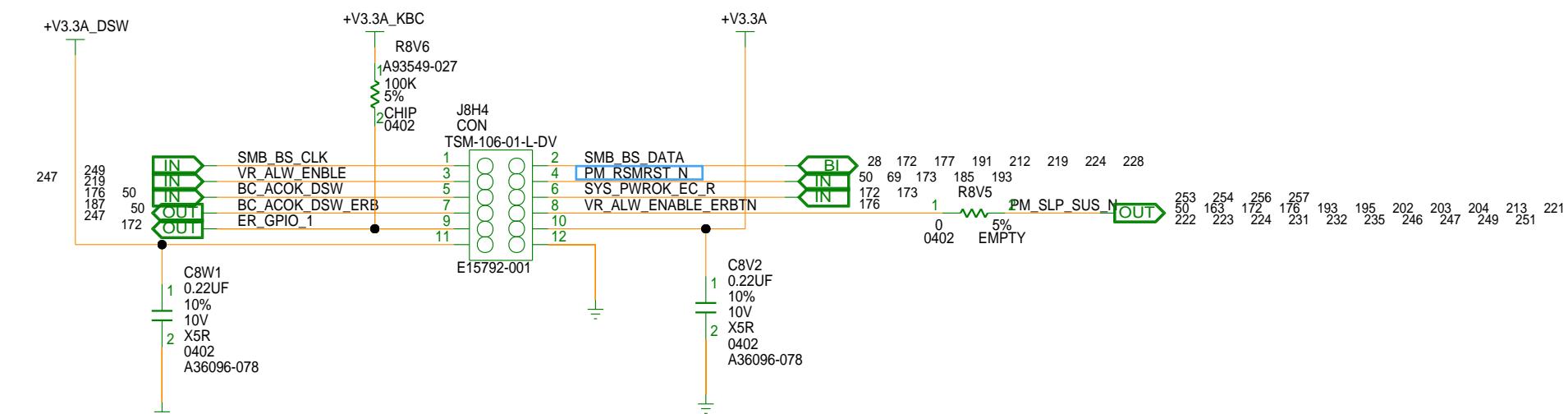


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## JUMPERS FOR VALIDATION

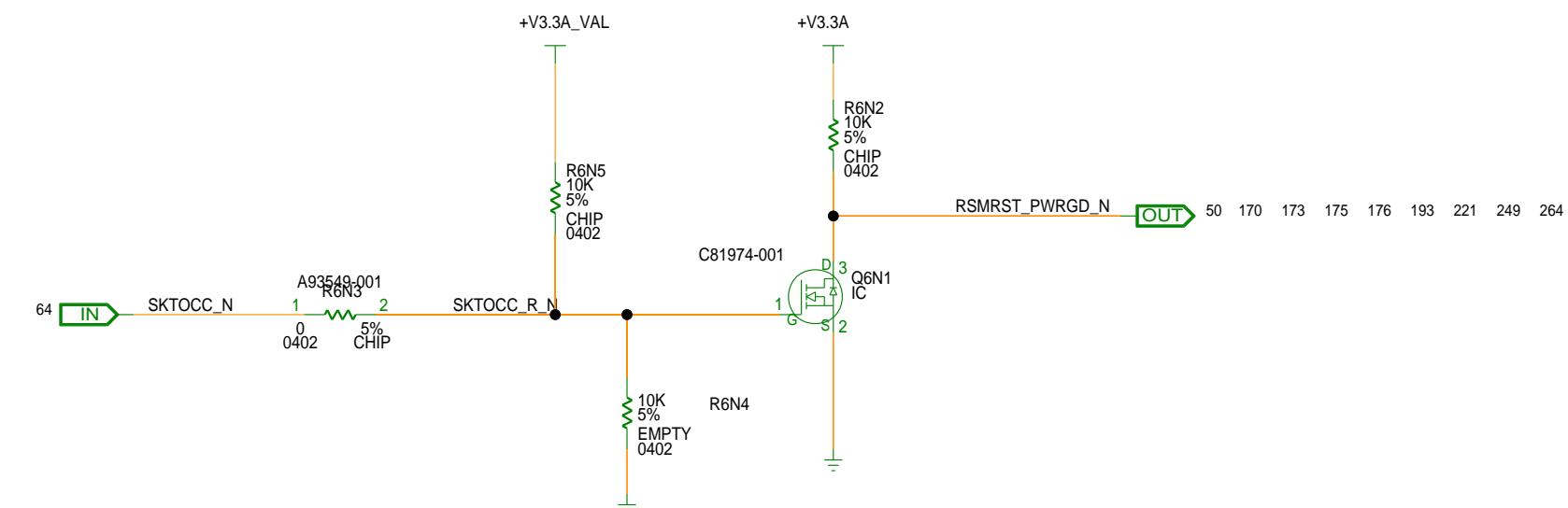


## EYE RIVER VALIDATION HEADER



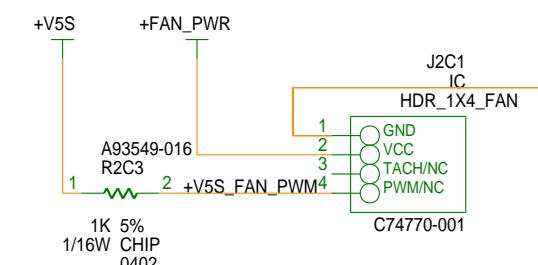
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MODULE NAME		REV	DATE				

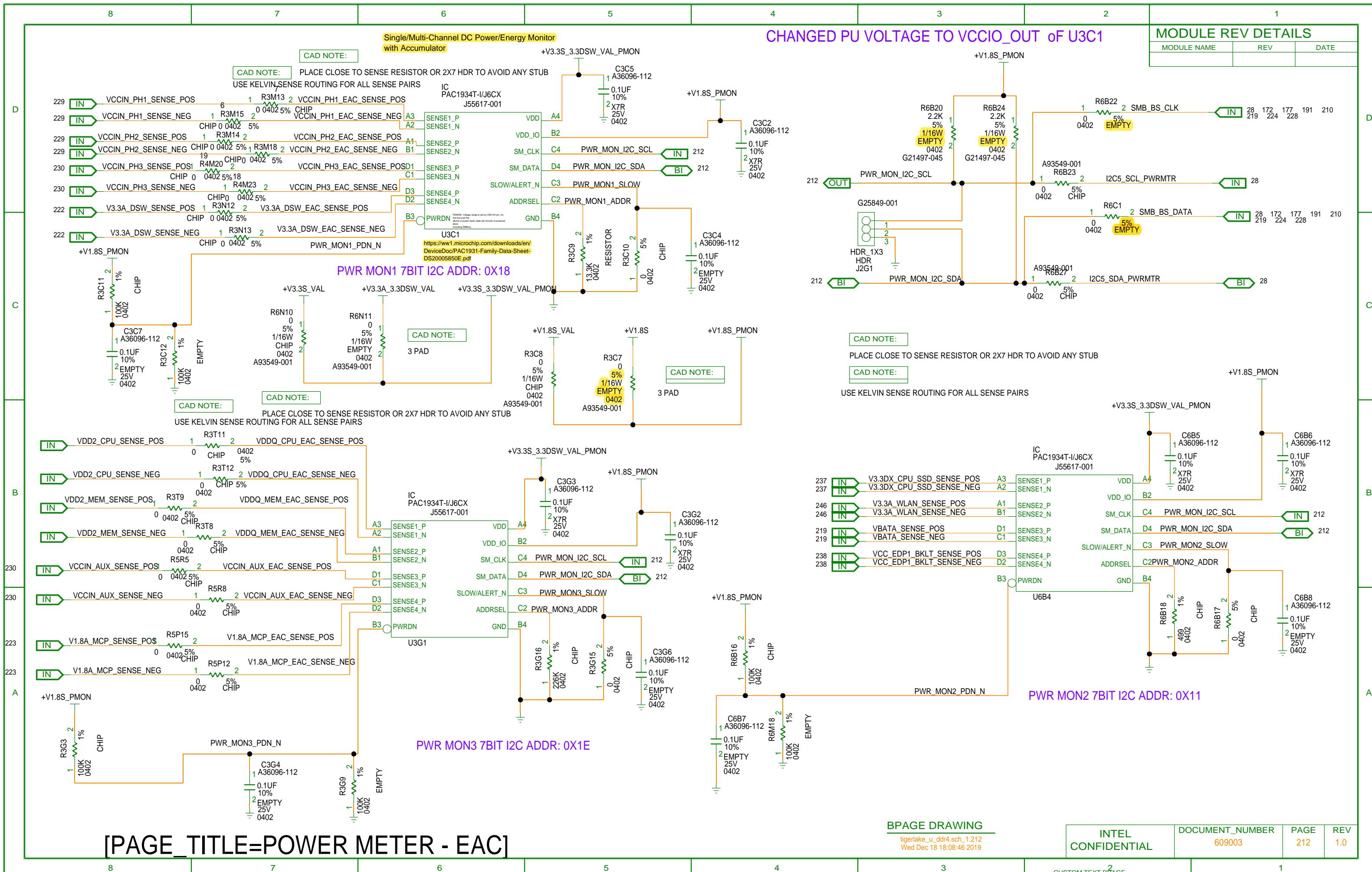
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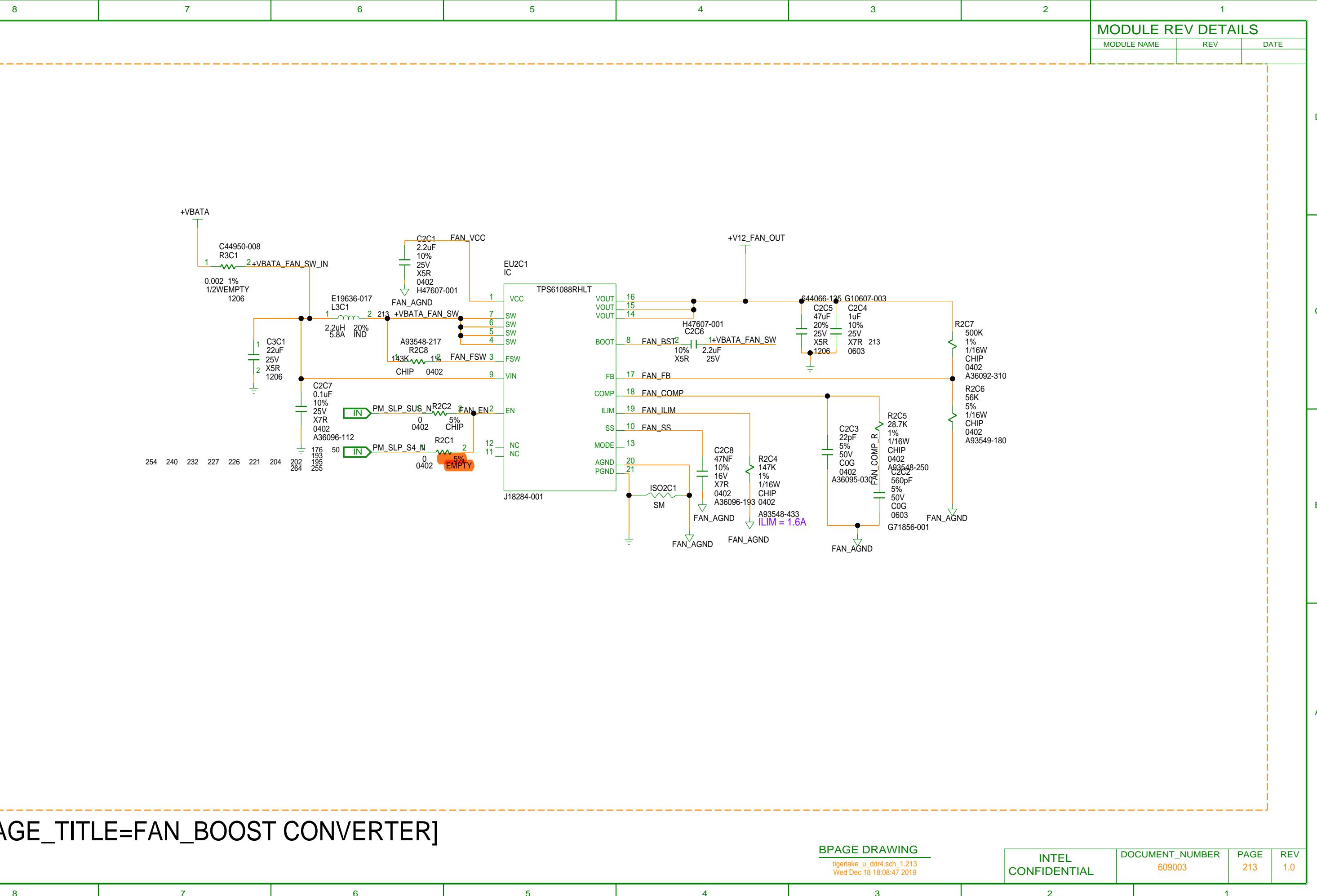


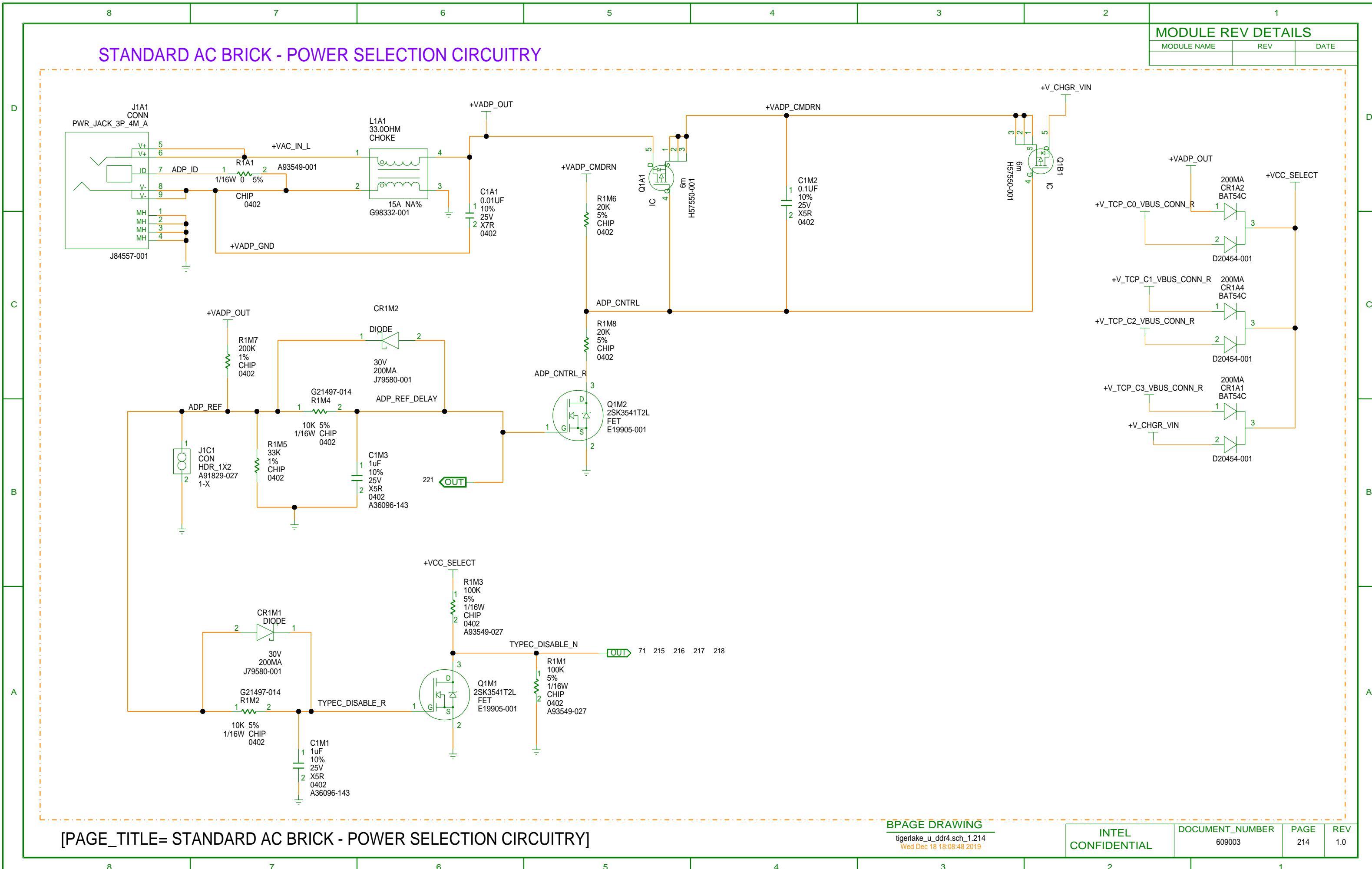
CONNECT TO A PROPER VSS PIN OF PCH  
PROCESSOR & PCH PART DETECT

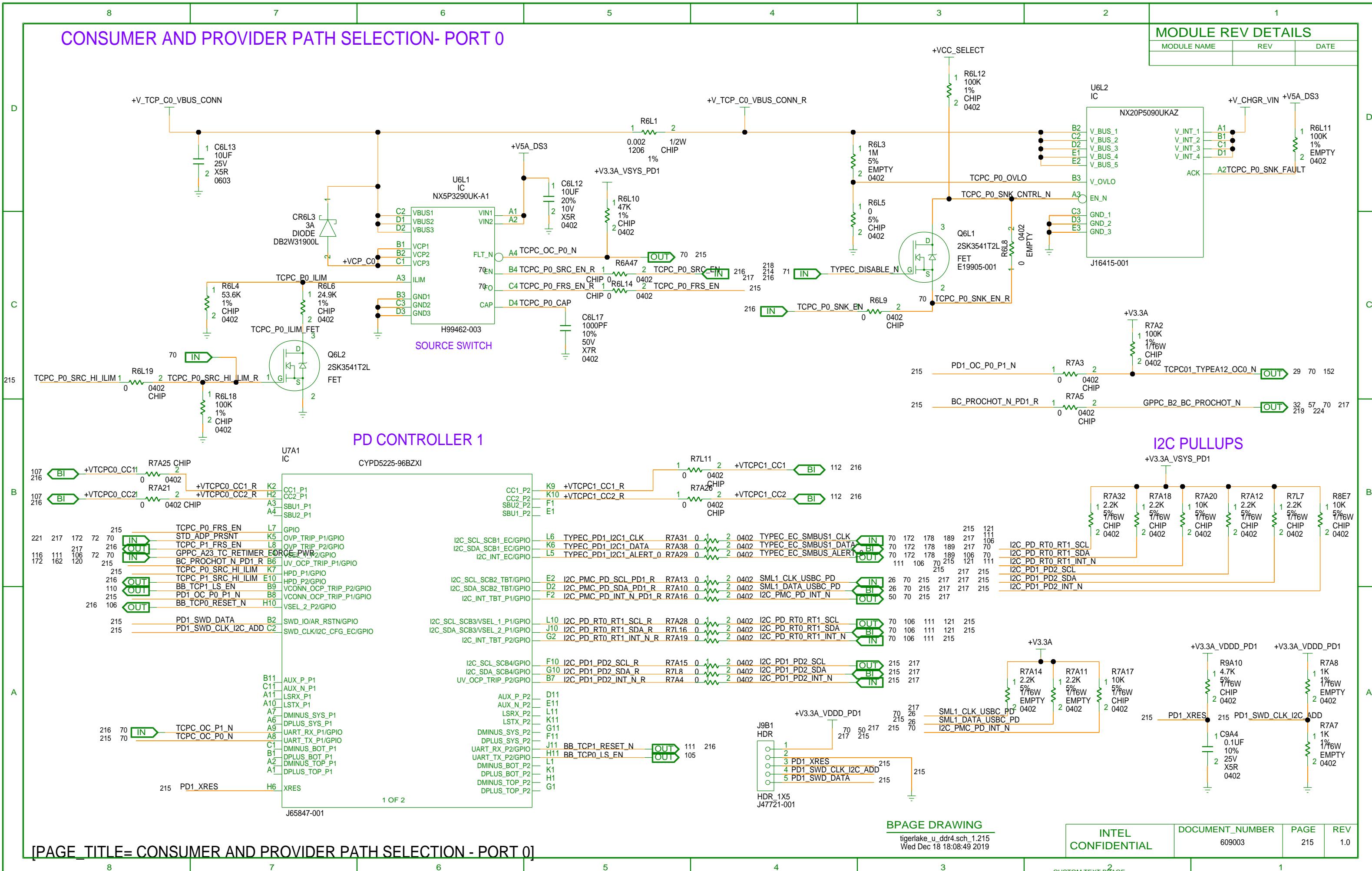
## FAN HEADER







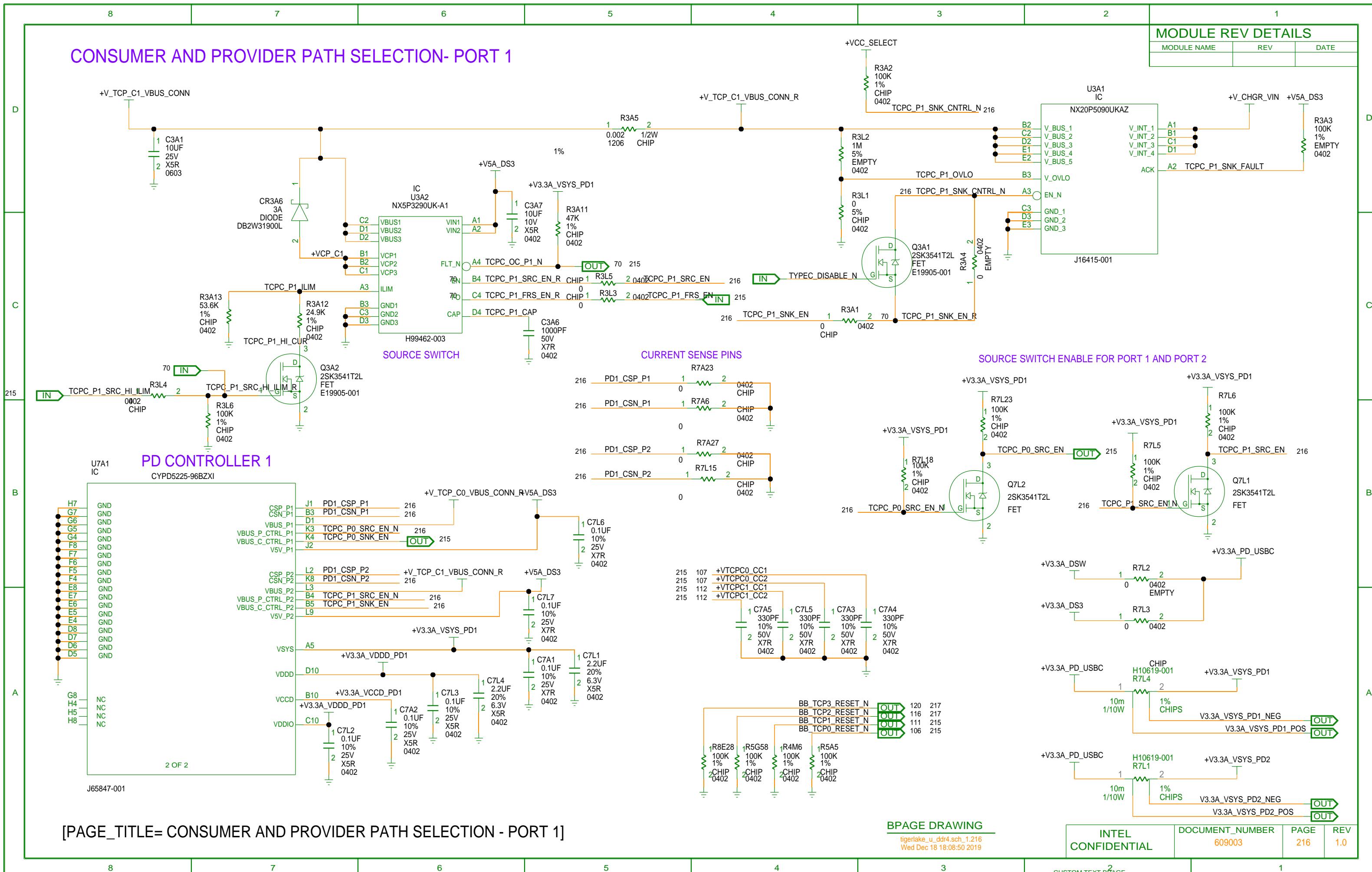


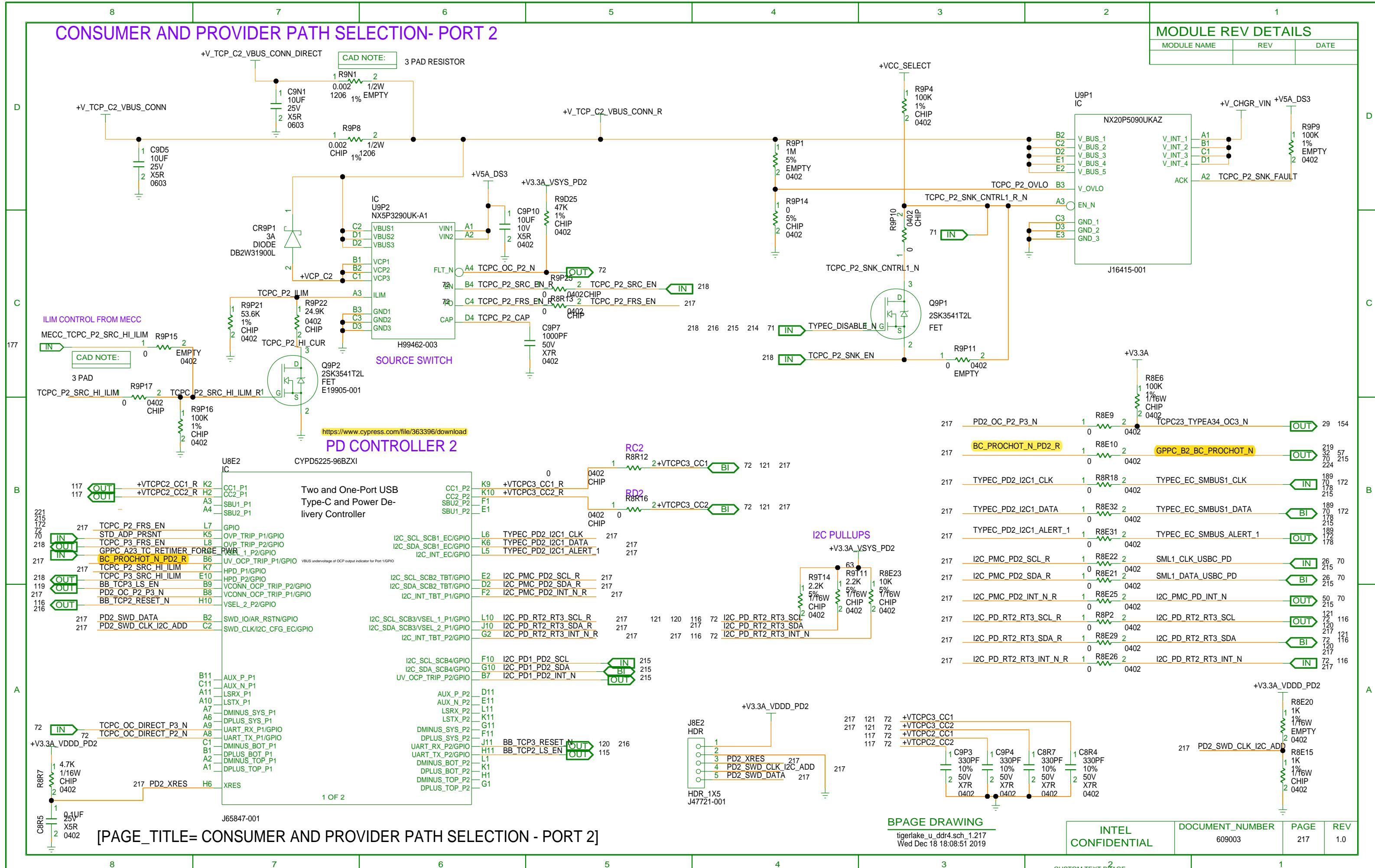


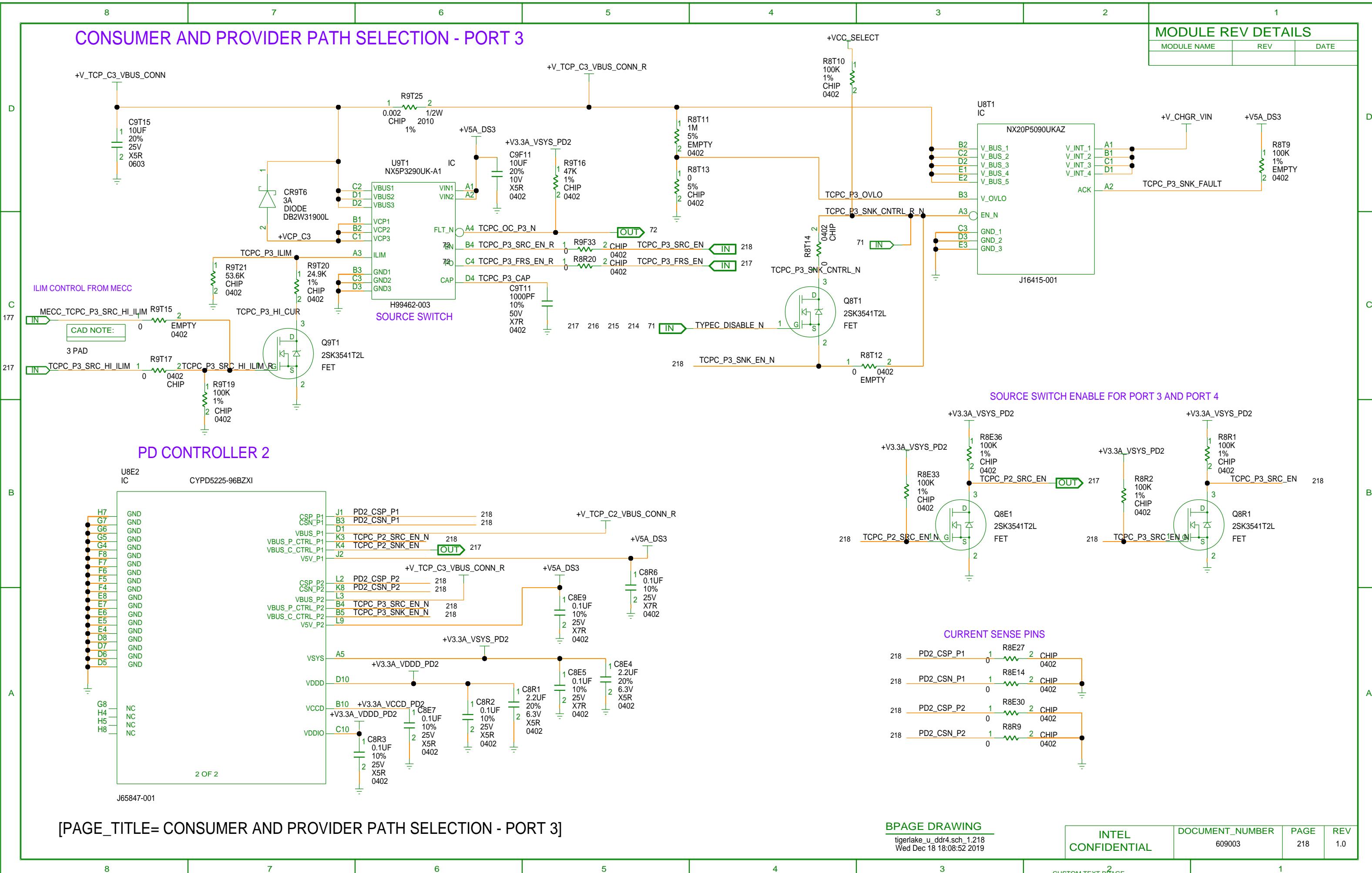
## CONSUMER AND PROVIDER PATH SELECTION- PORT 1

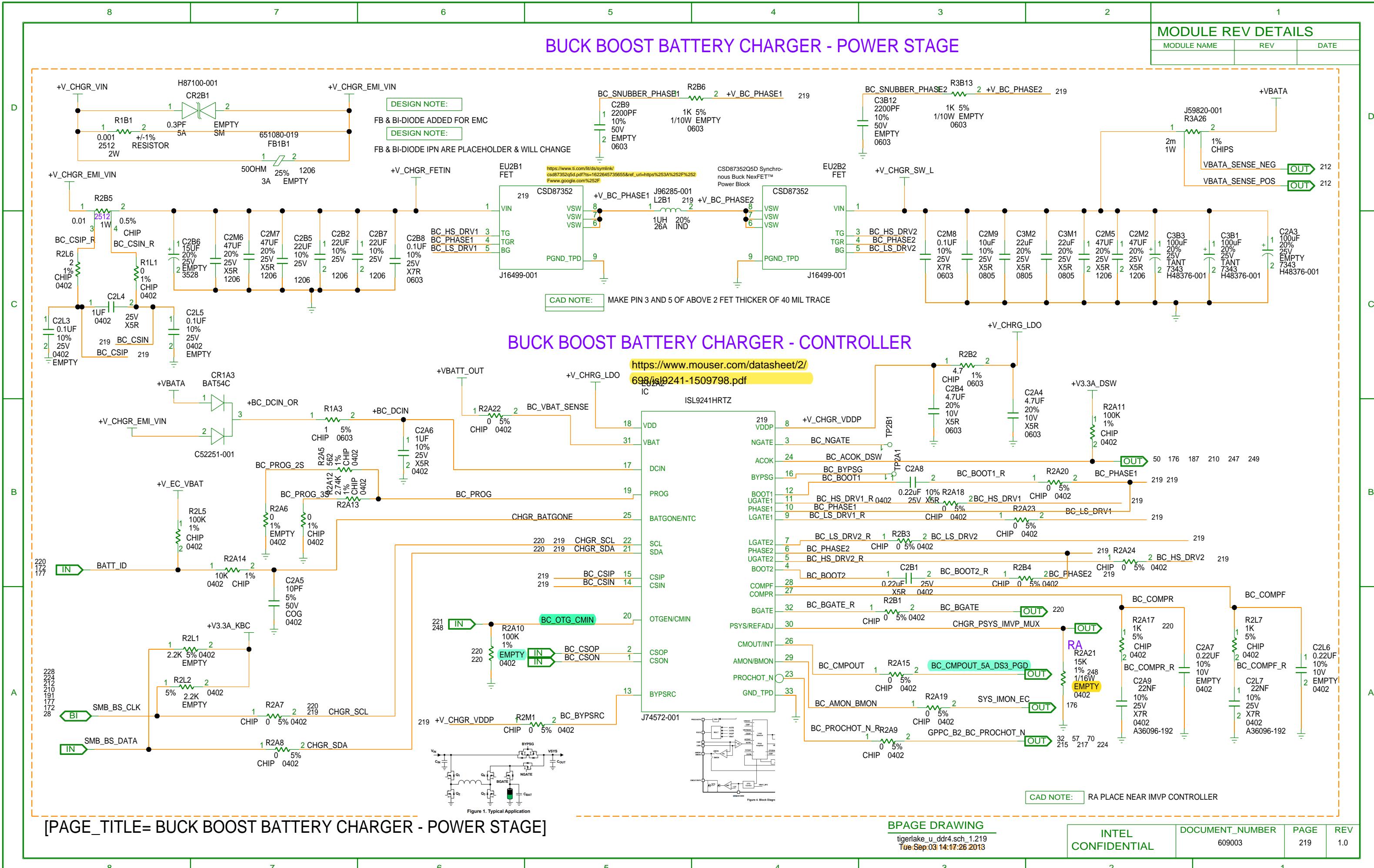
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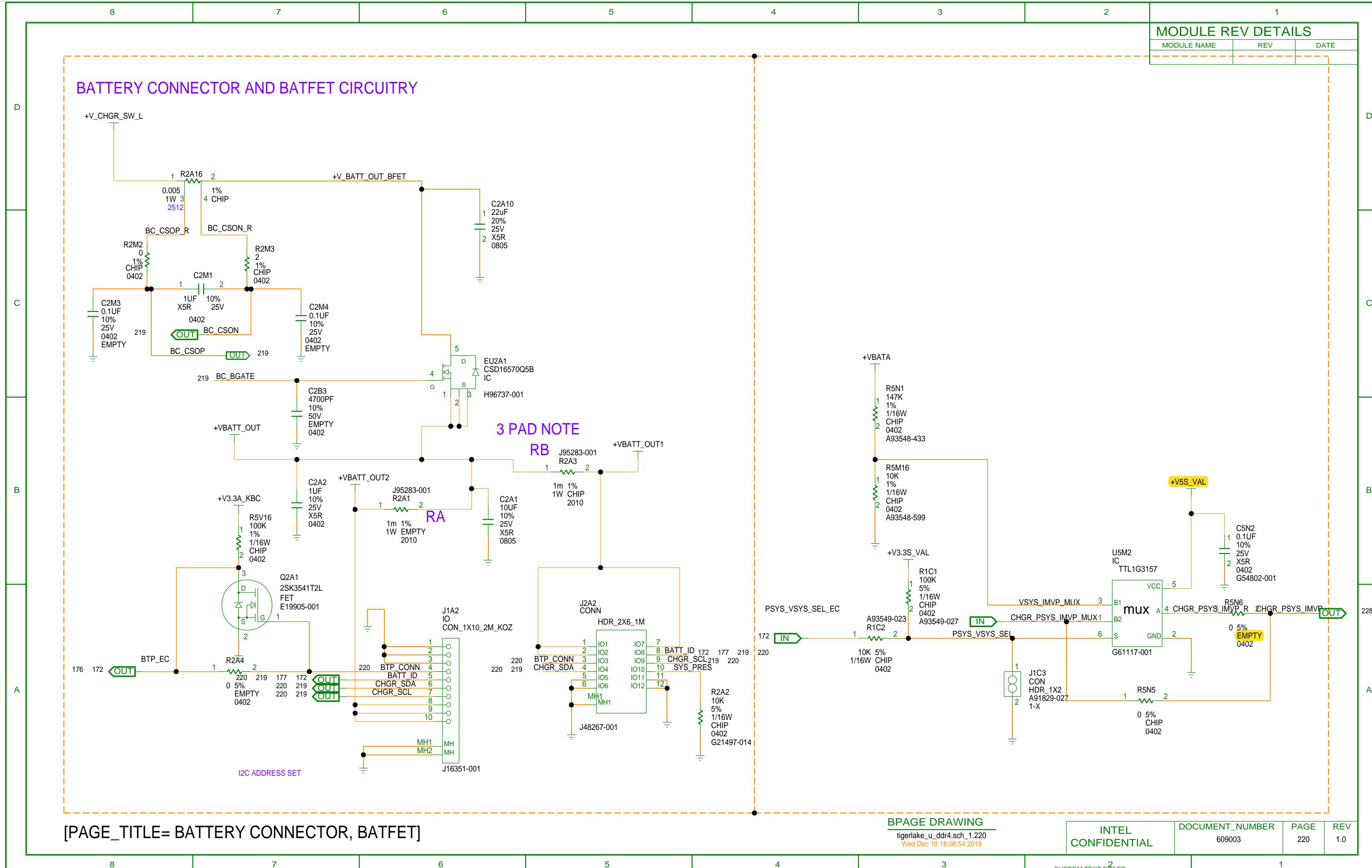
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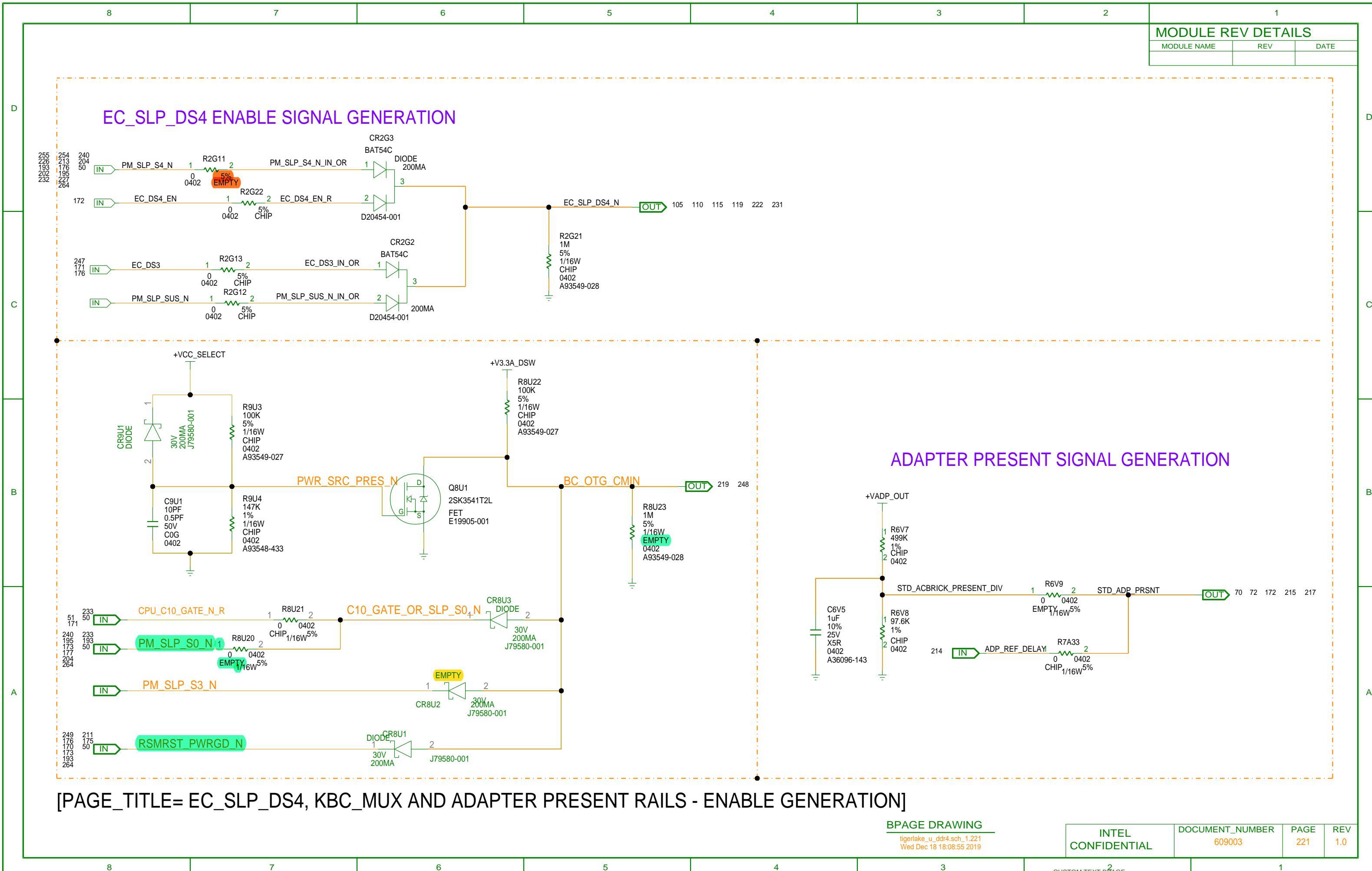


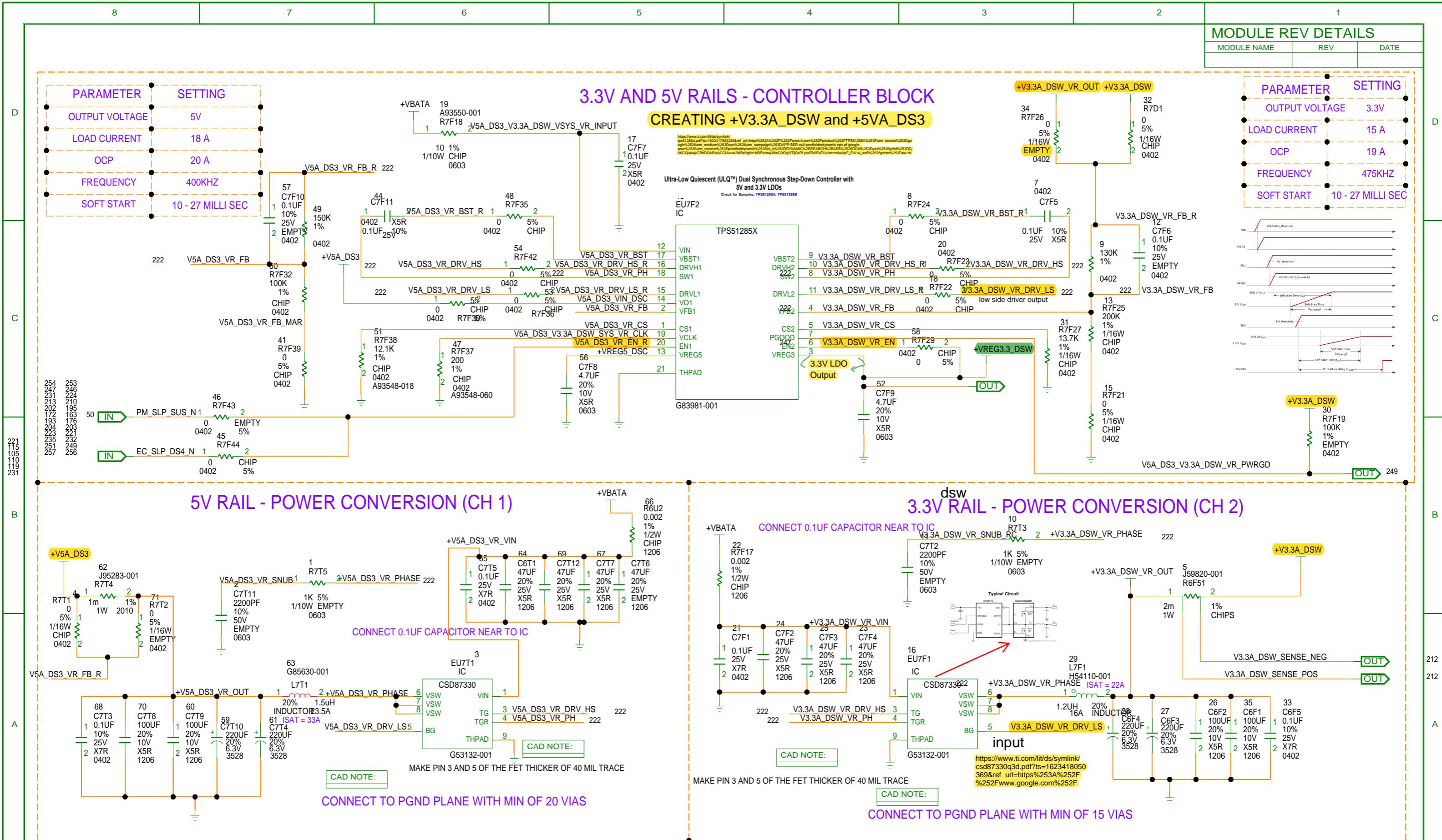












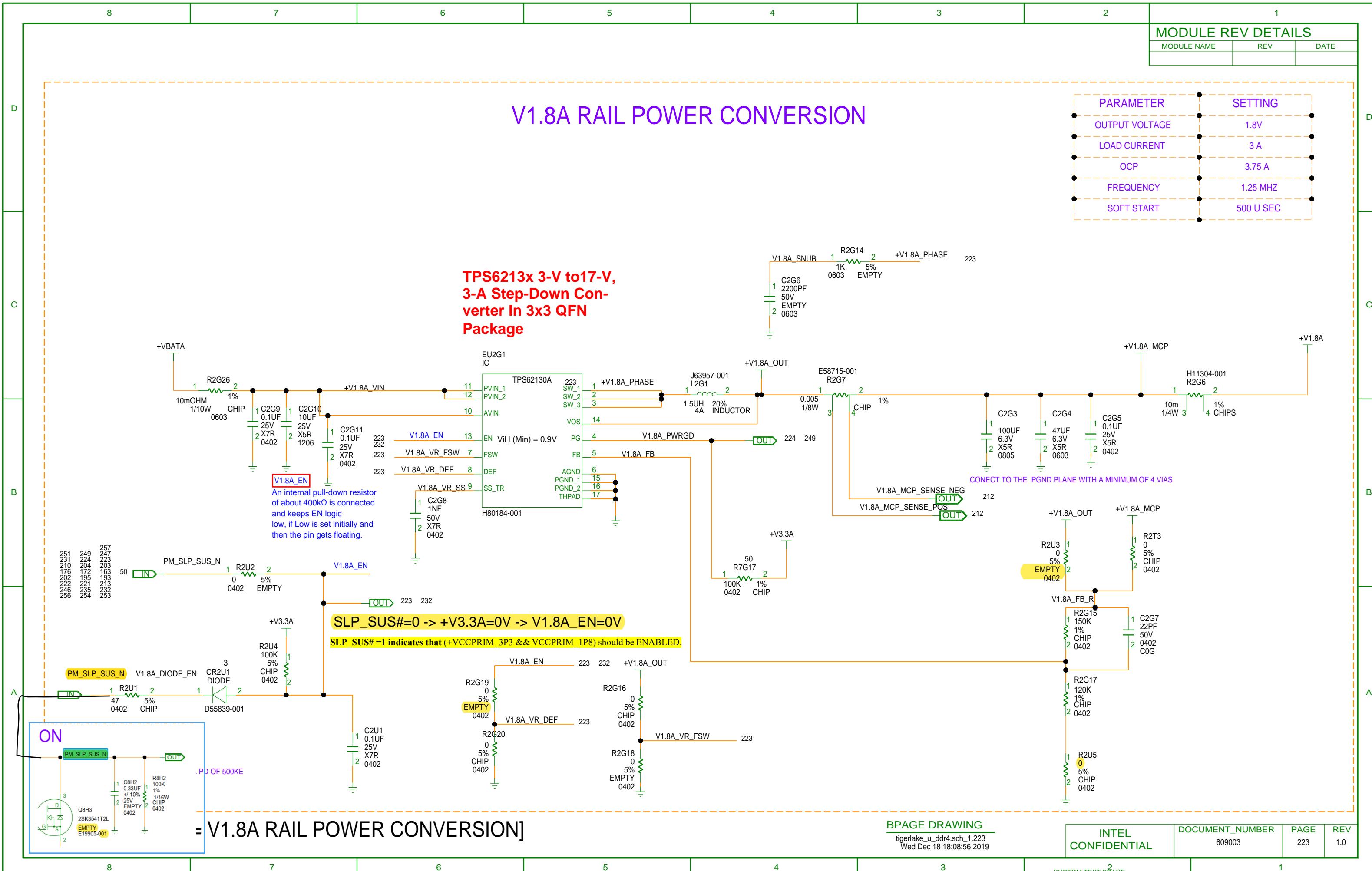
[PAGE TITLE= 3.3V AND 5V RAILS - POWER CONVERSION]

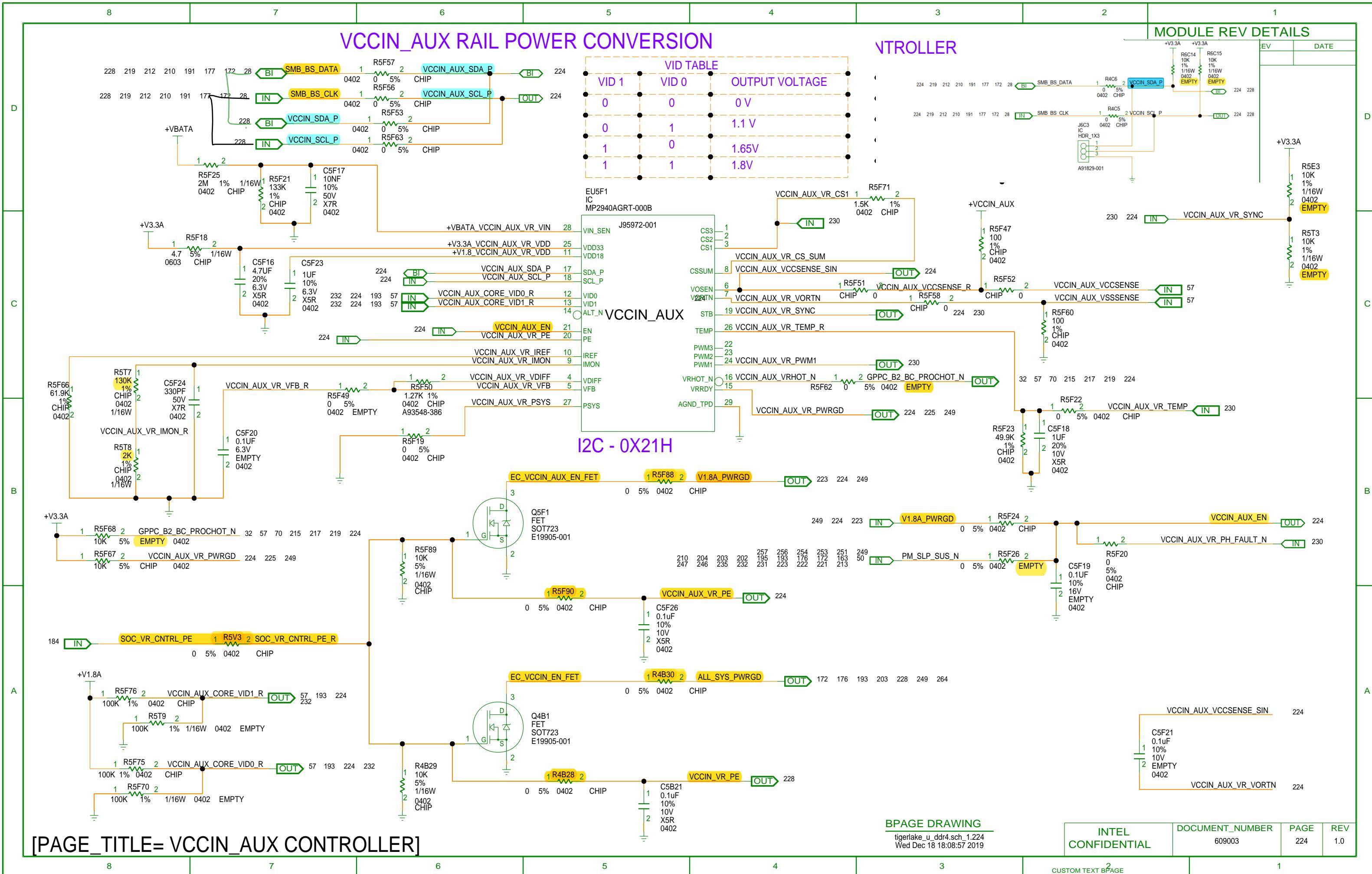
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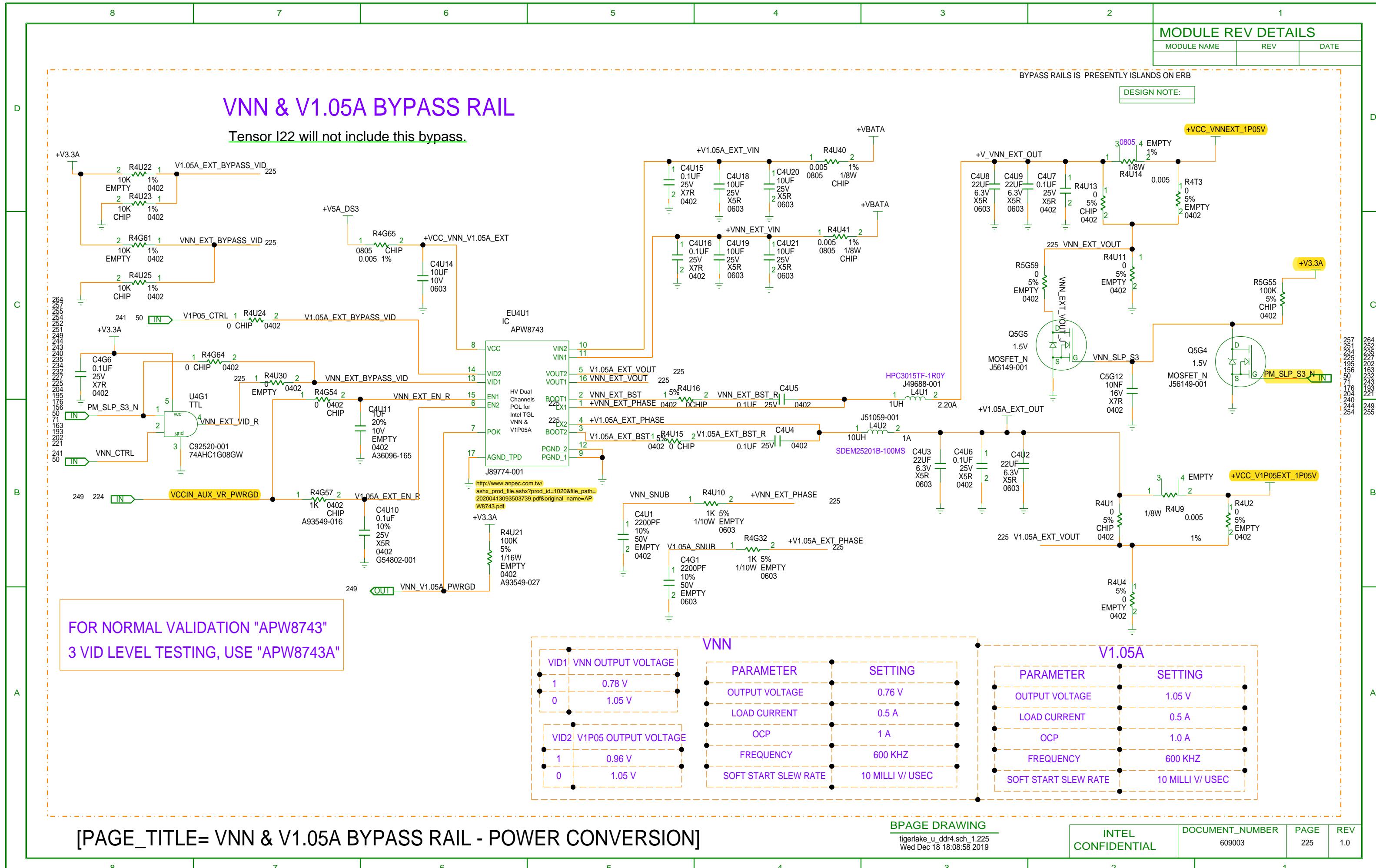
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CONFIDENTIAL

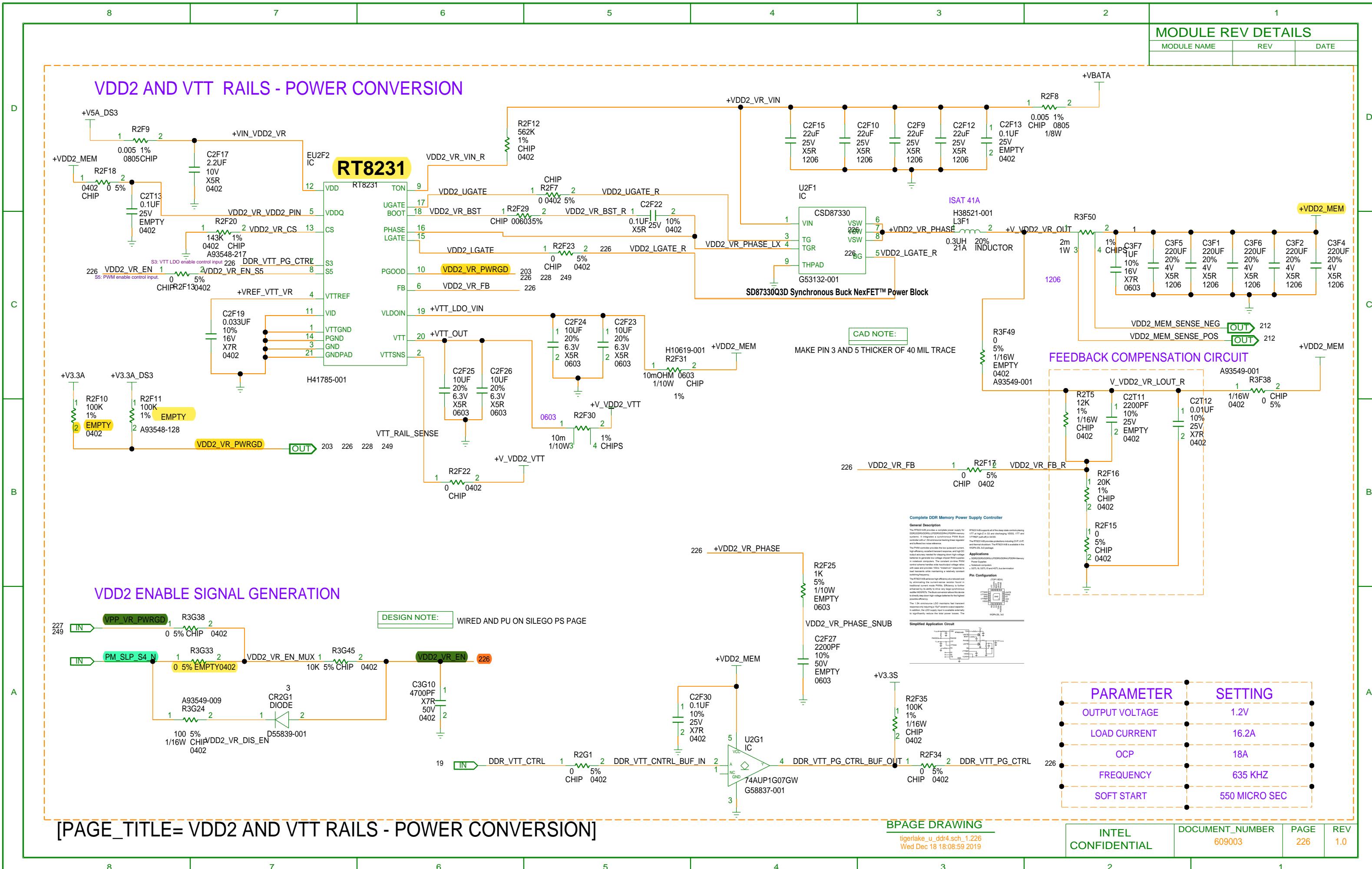
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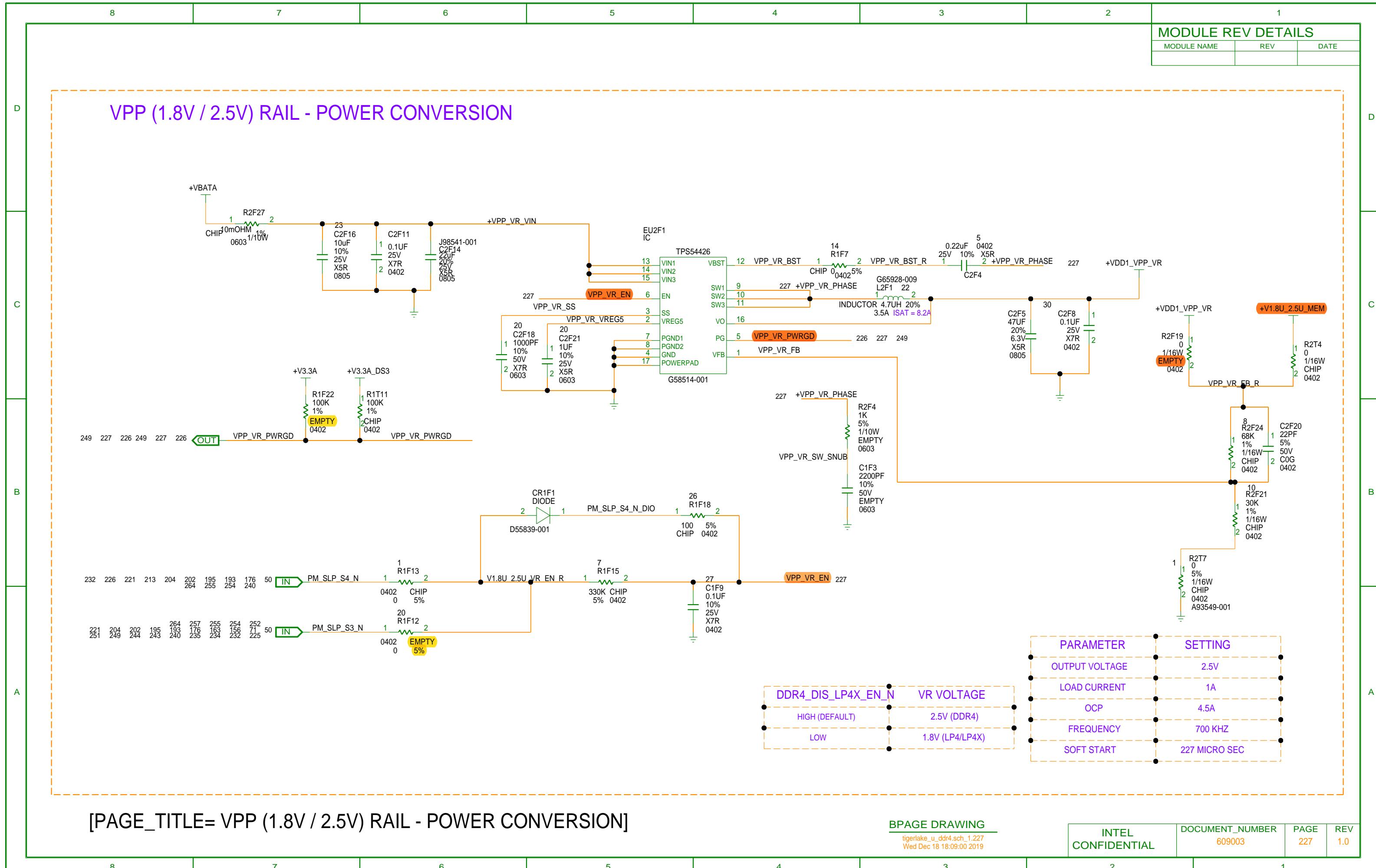
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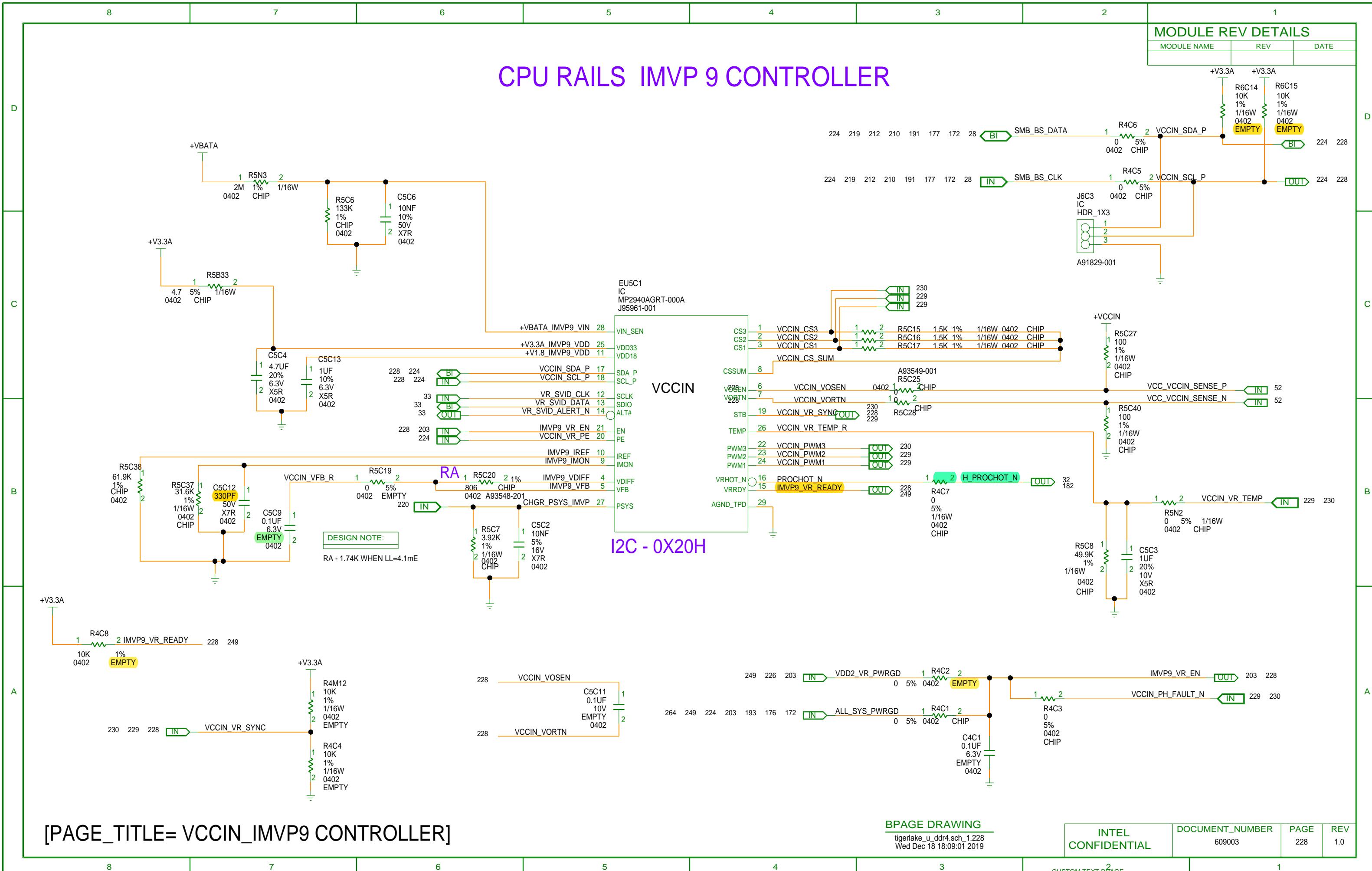


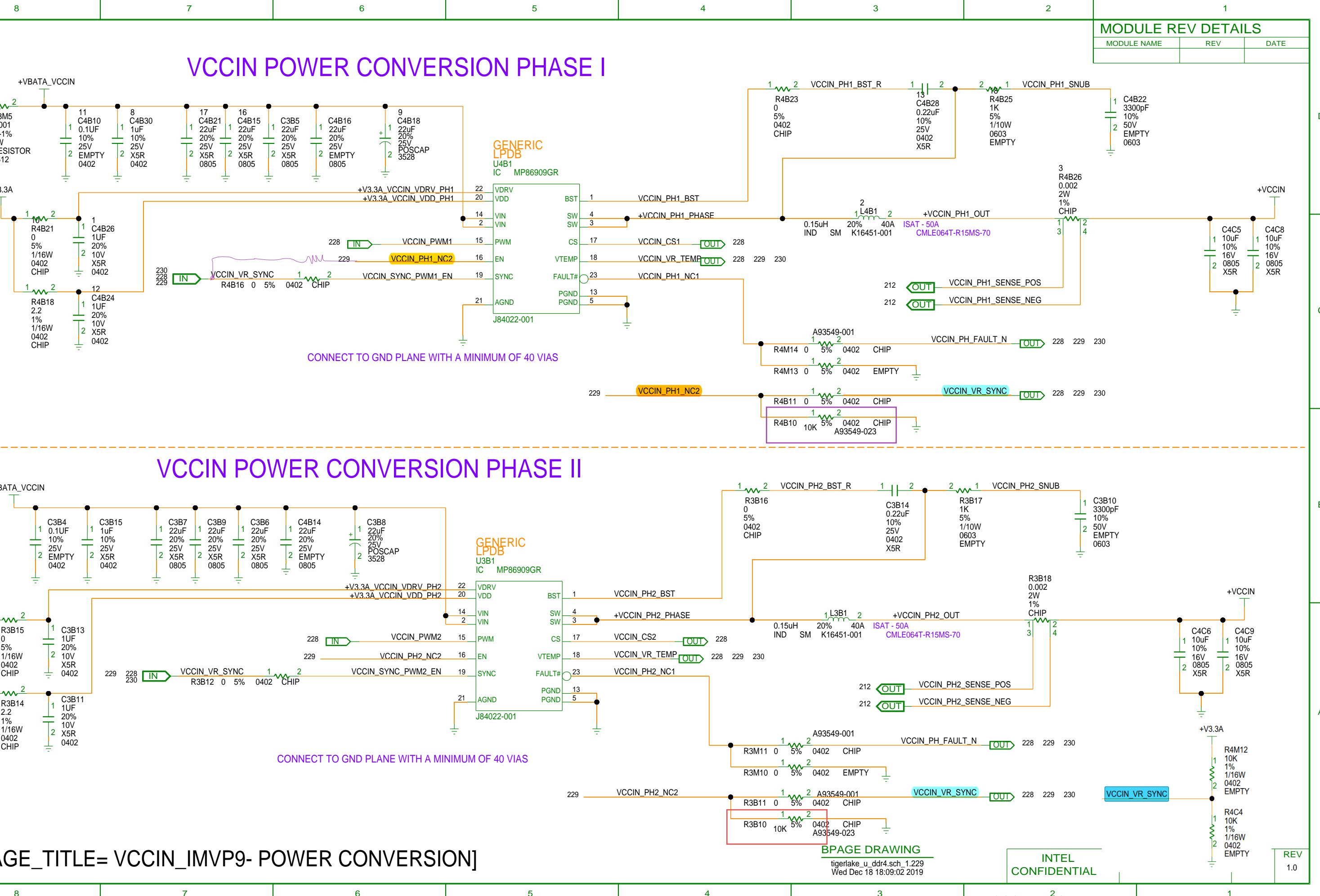








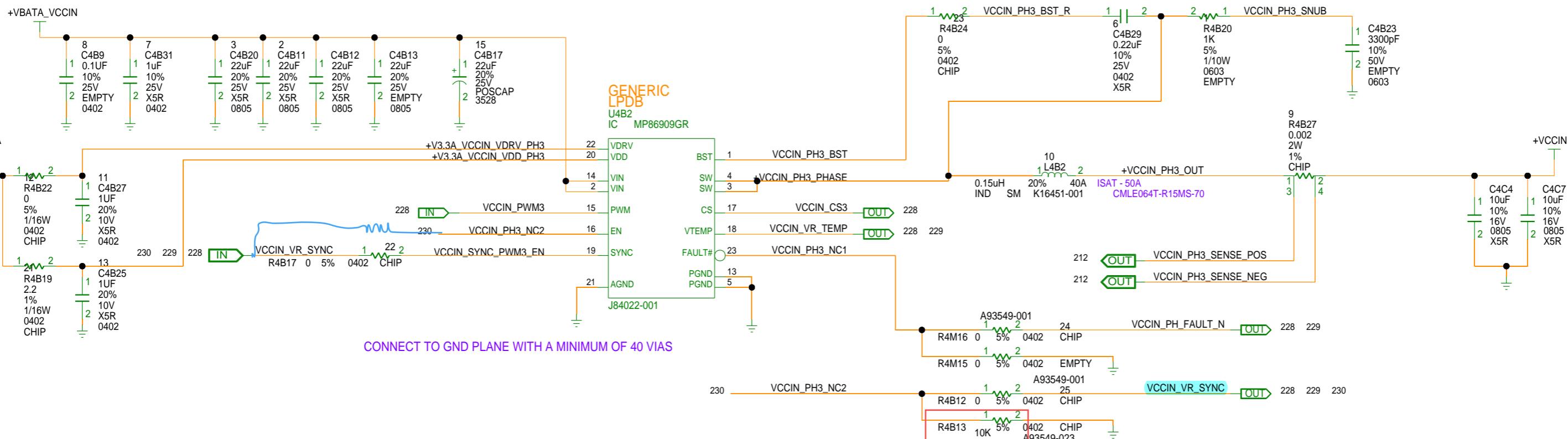




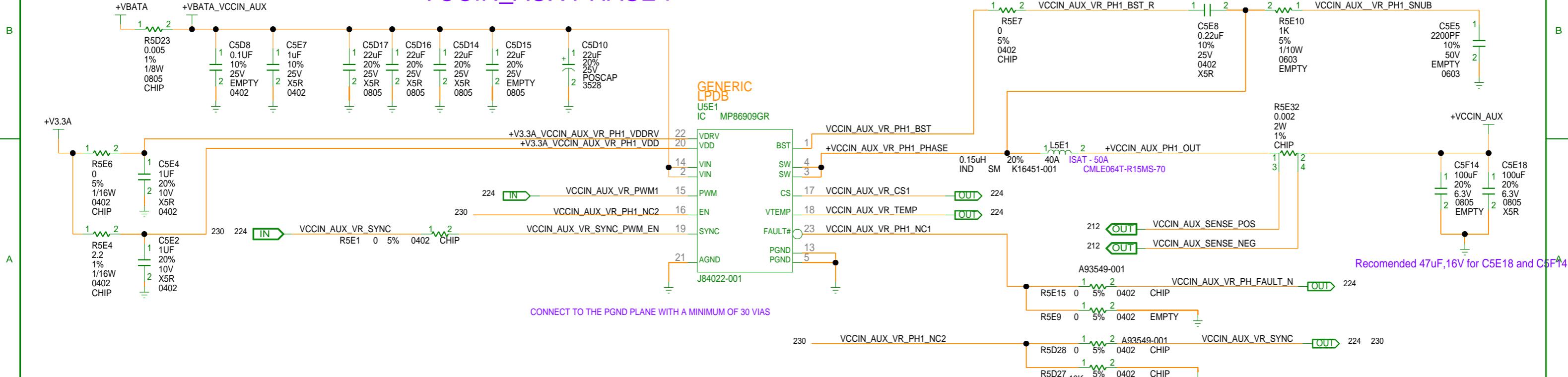
# VCCIN POWER CONVERSION PHASE III

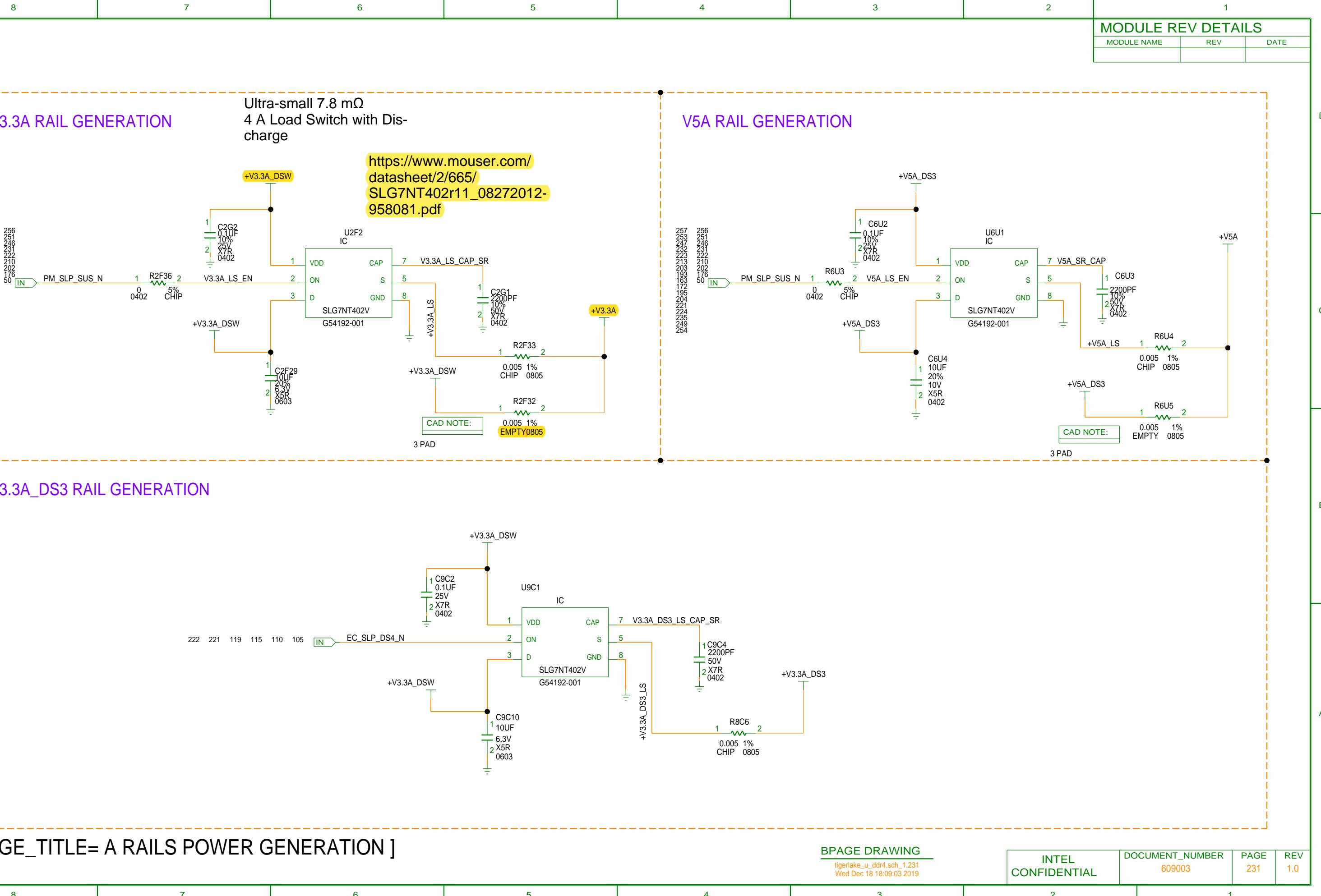
## MODULE REV DETAILS

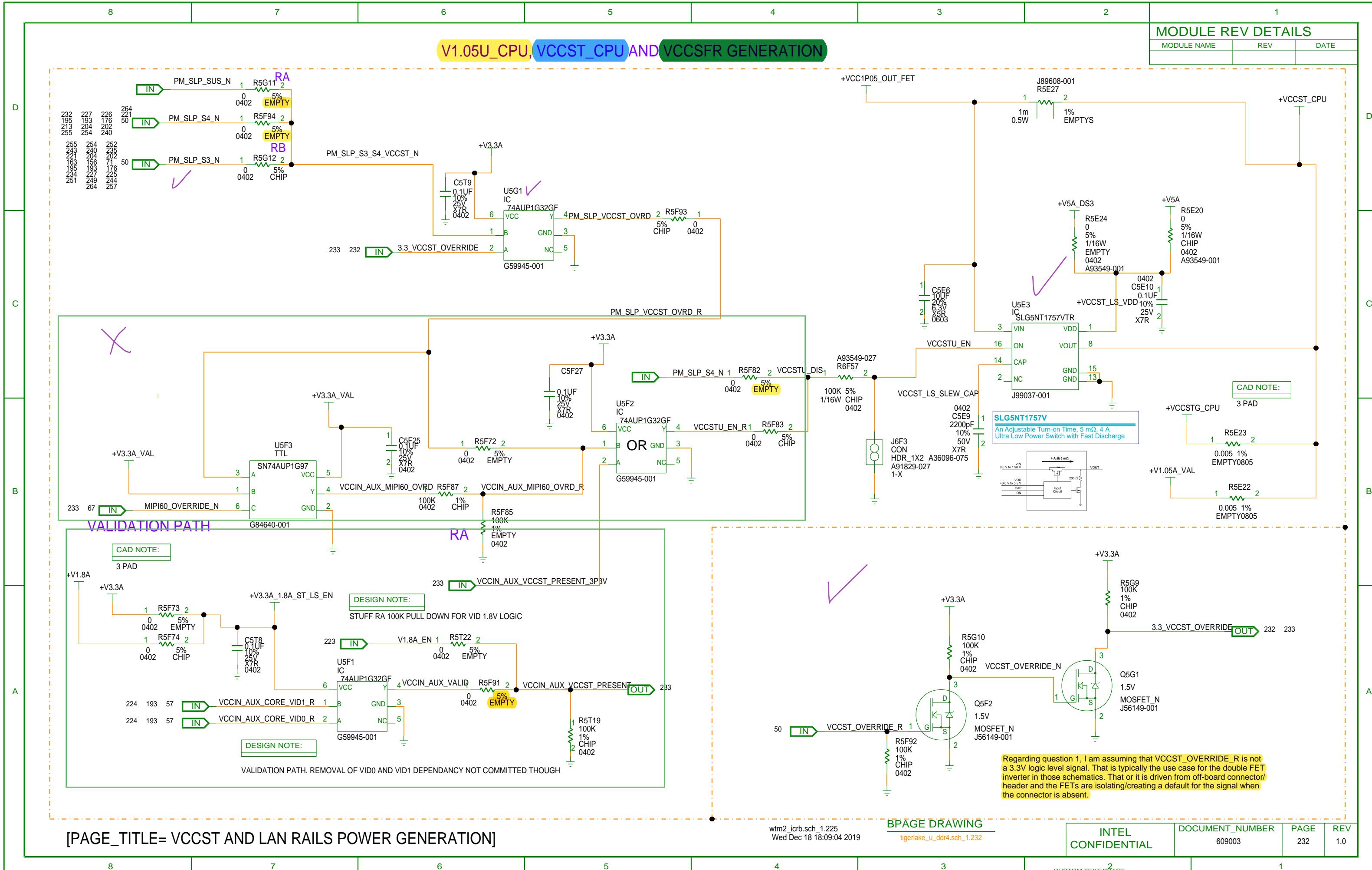
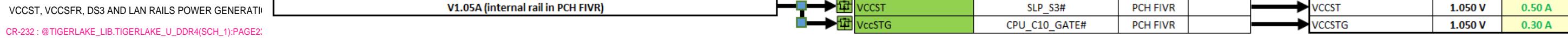
MODULE NAME	REV	DATE

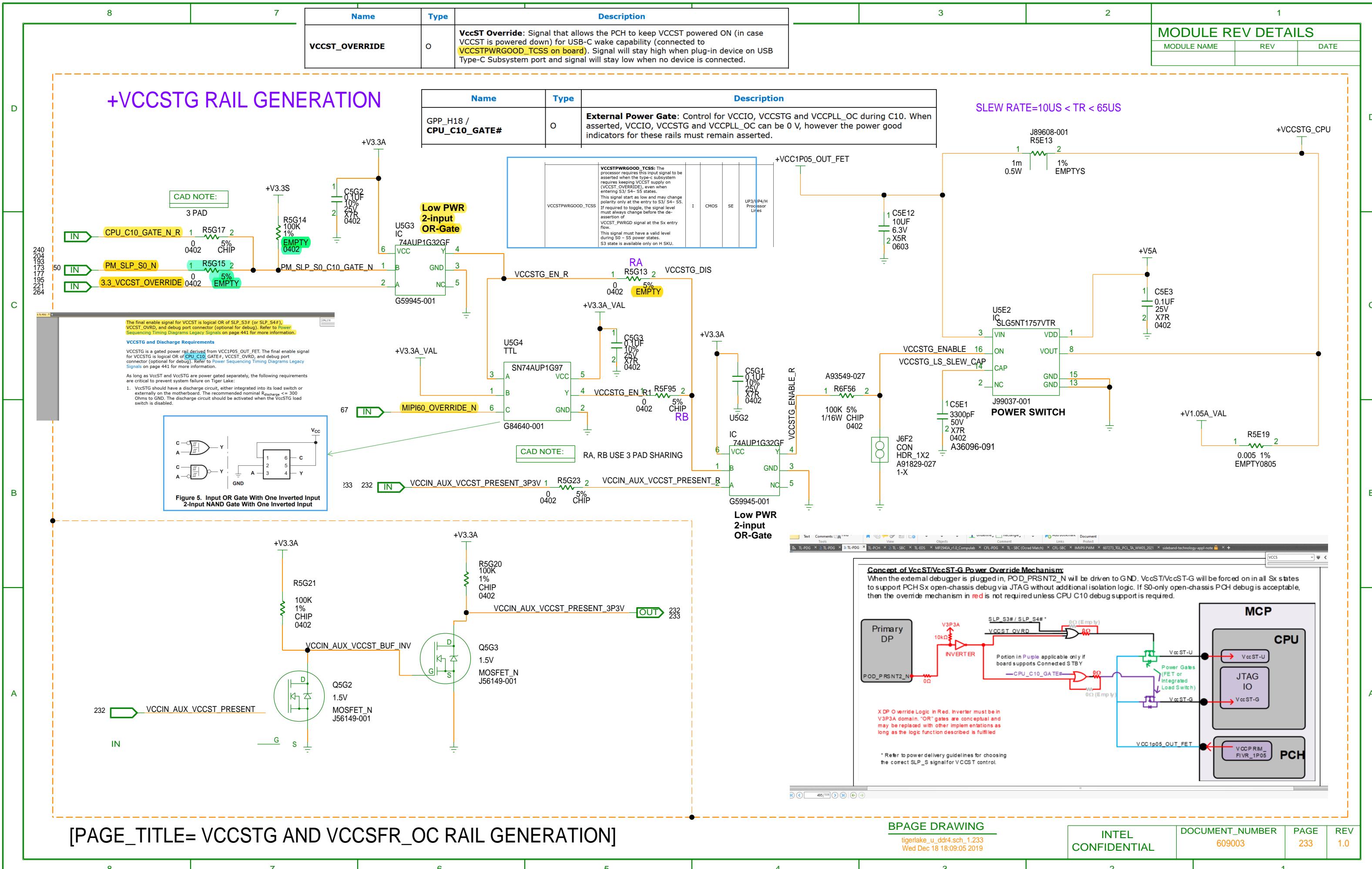


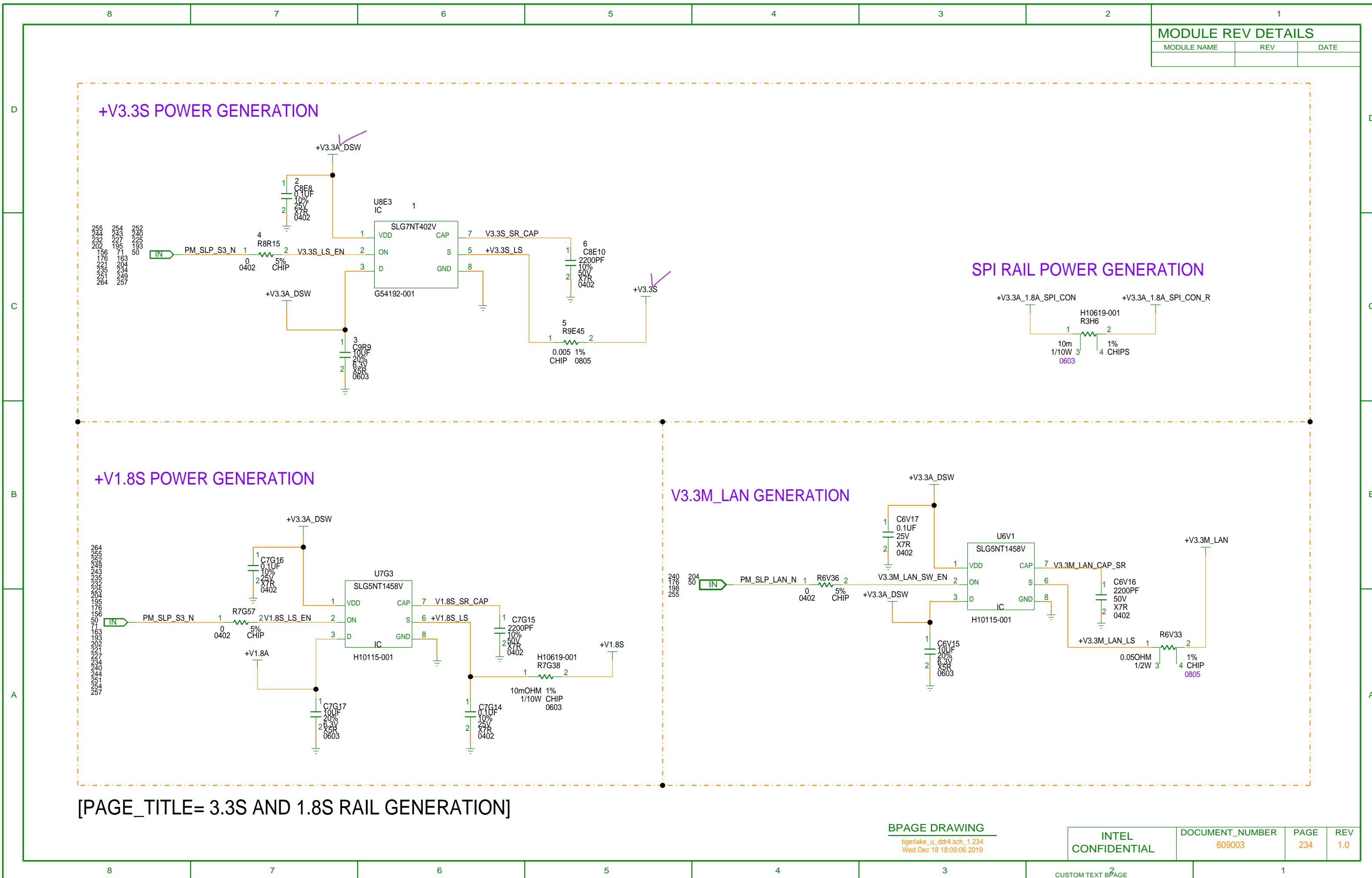
# VCCIN\_AUX PHASE I







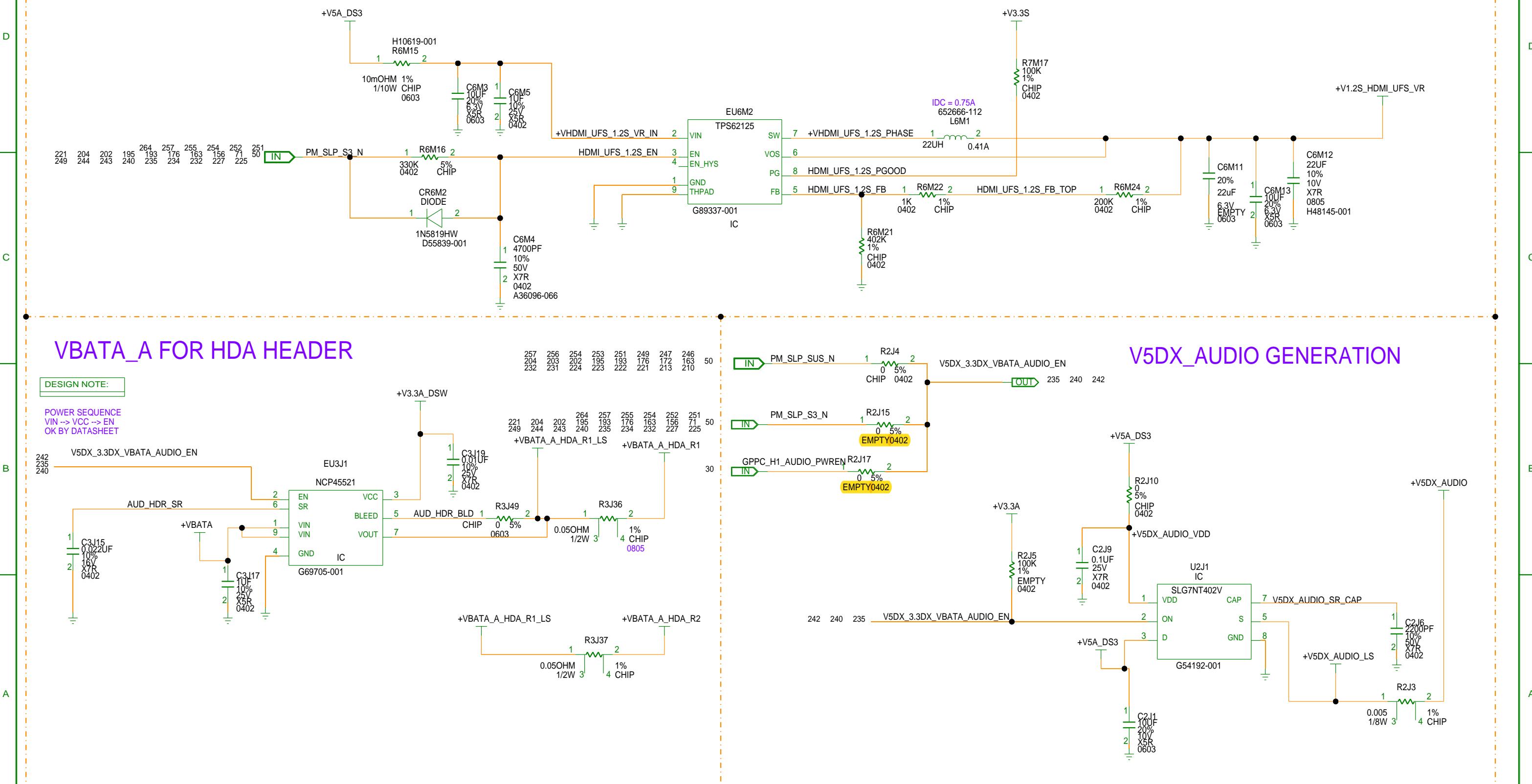




## 1.2V RAIL FOR HDMI AND UFS - POWER CONVERSION

## MODULE REV DETAILS

MODULE NAME	REV	DATE



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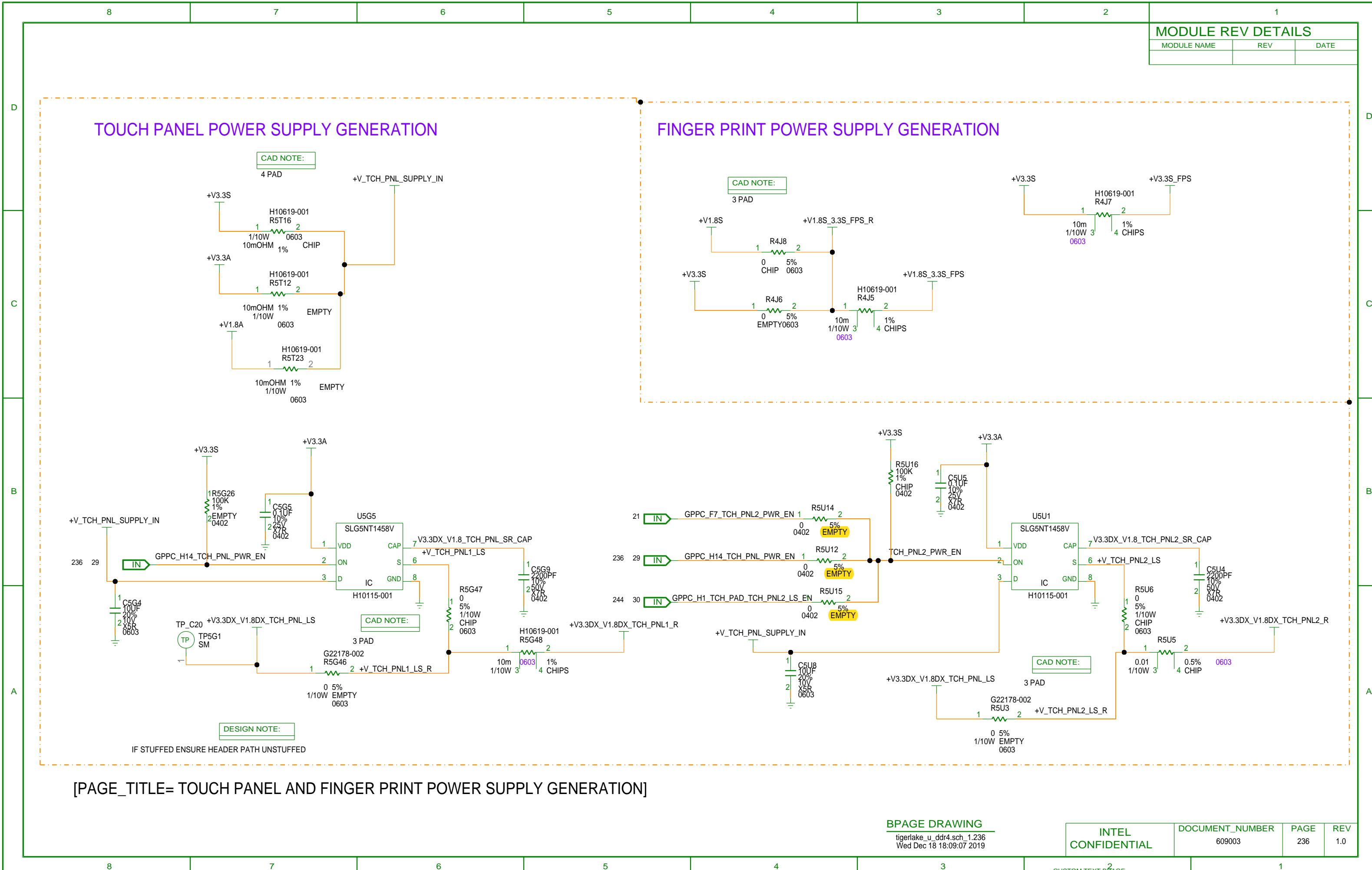
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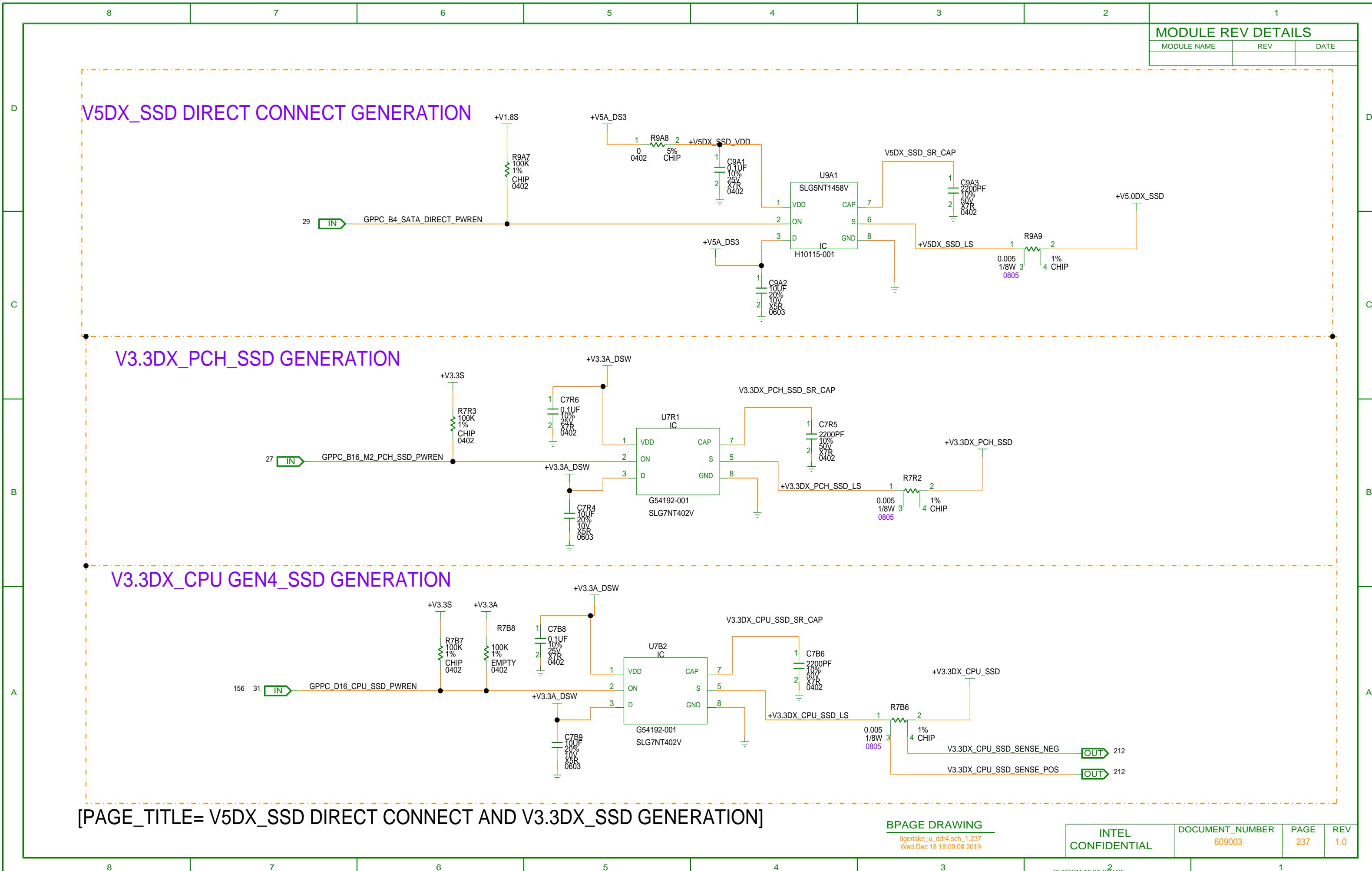
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Wed Dec 18 18:09:07 2019

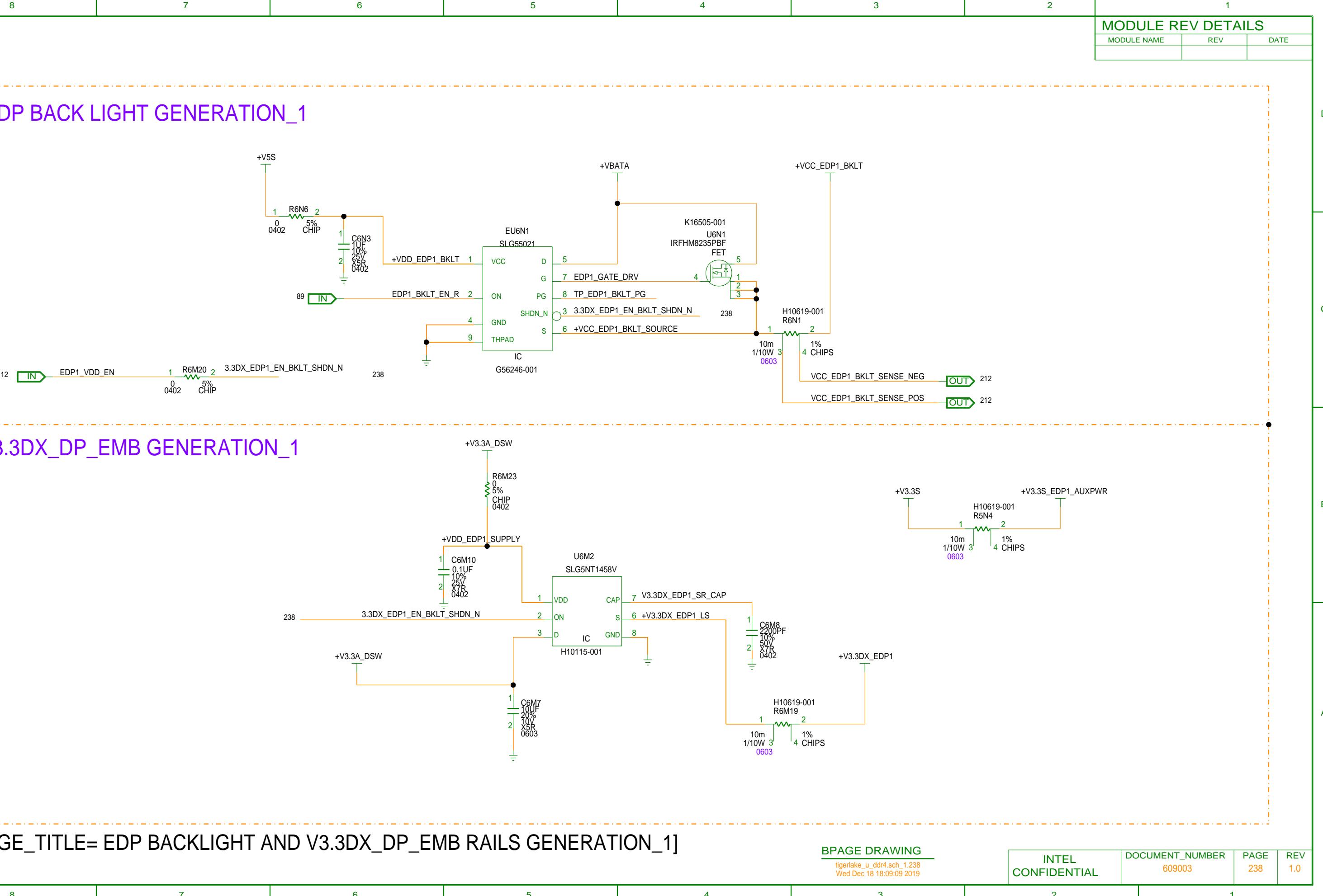
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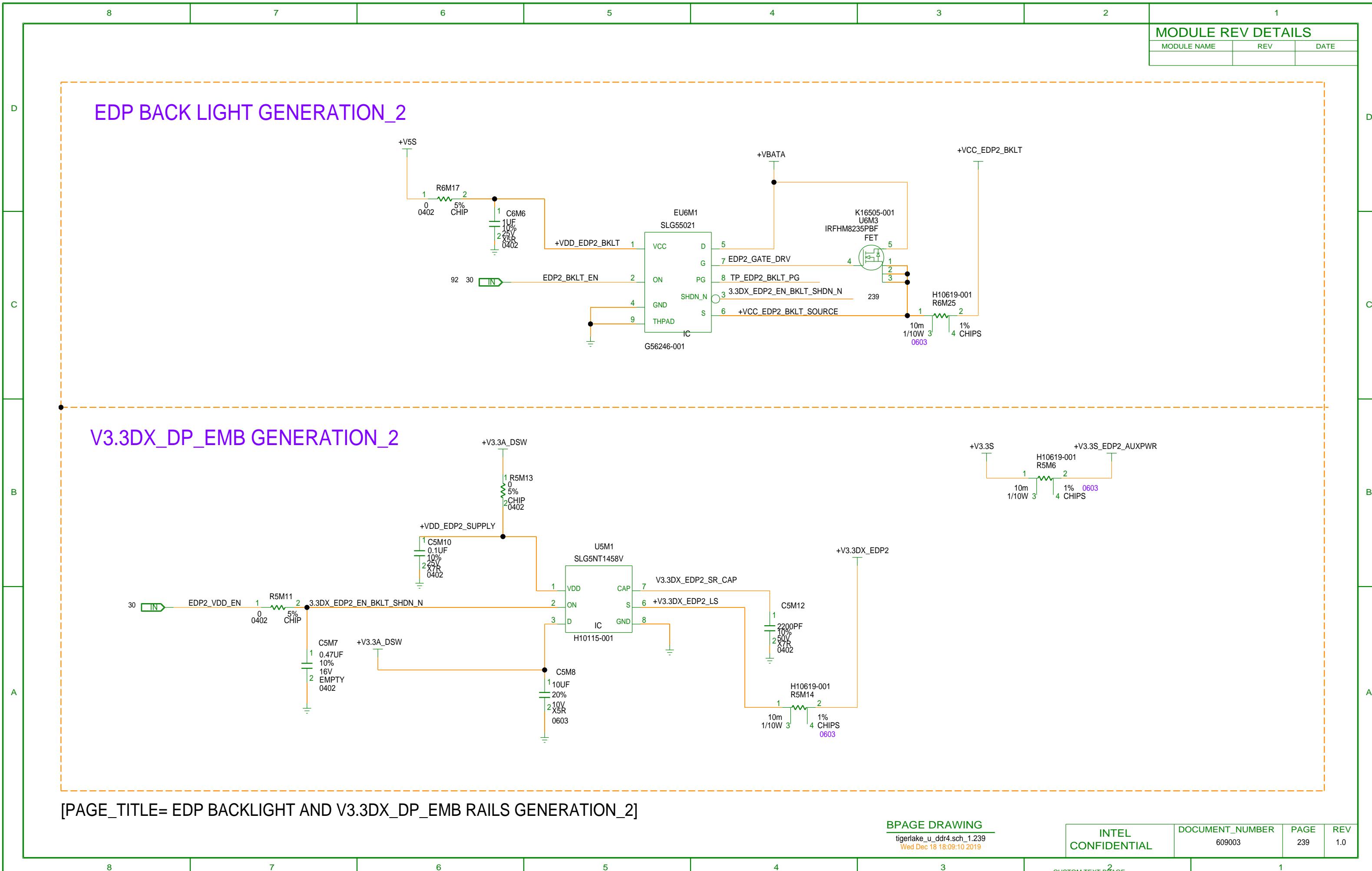
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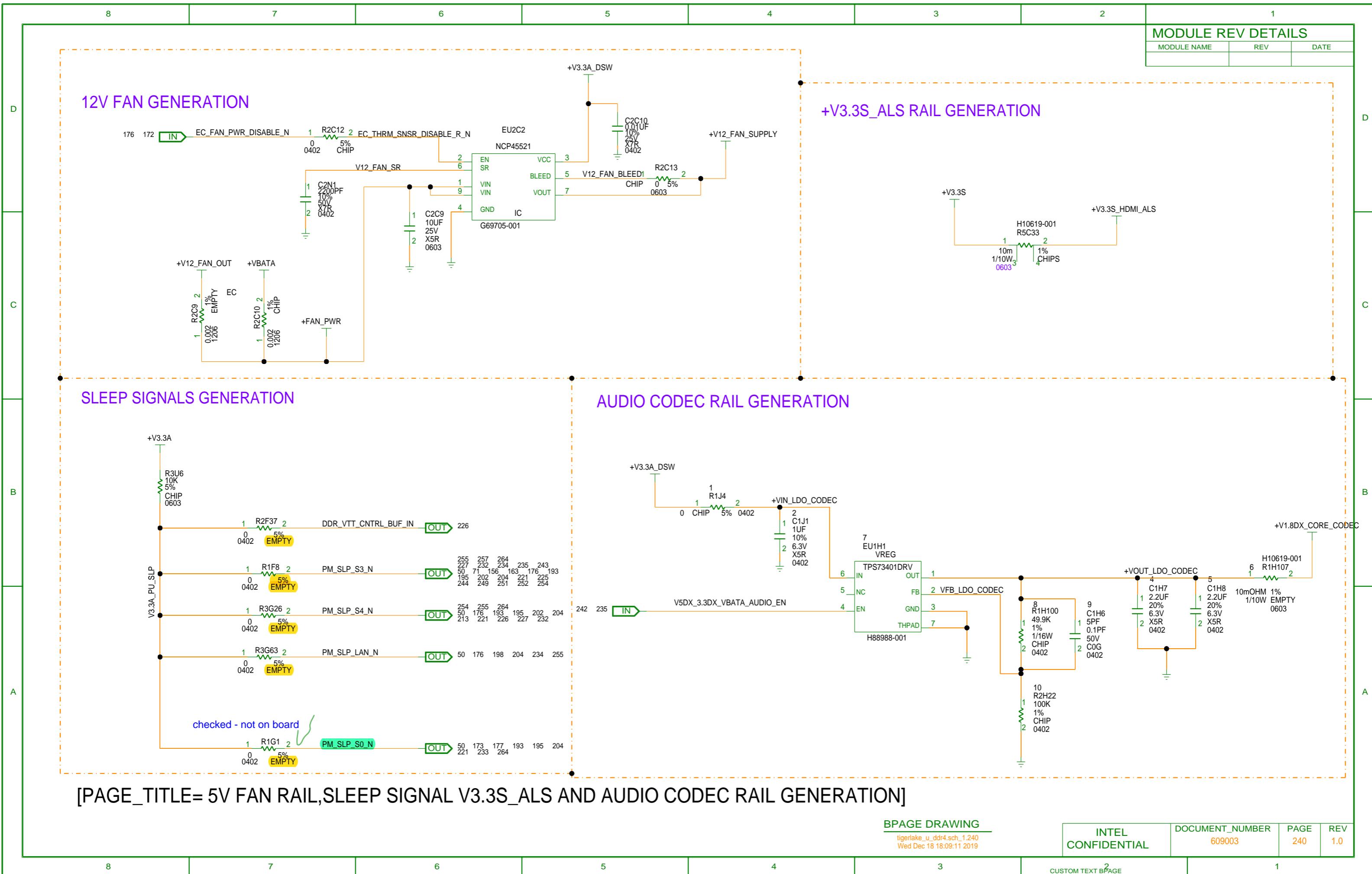
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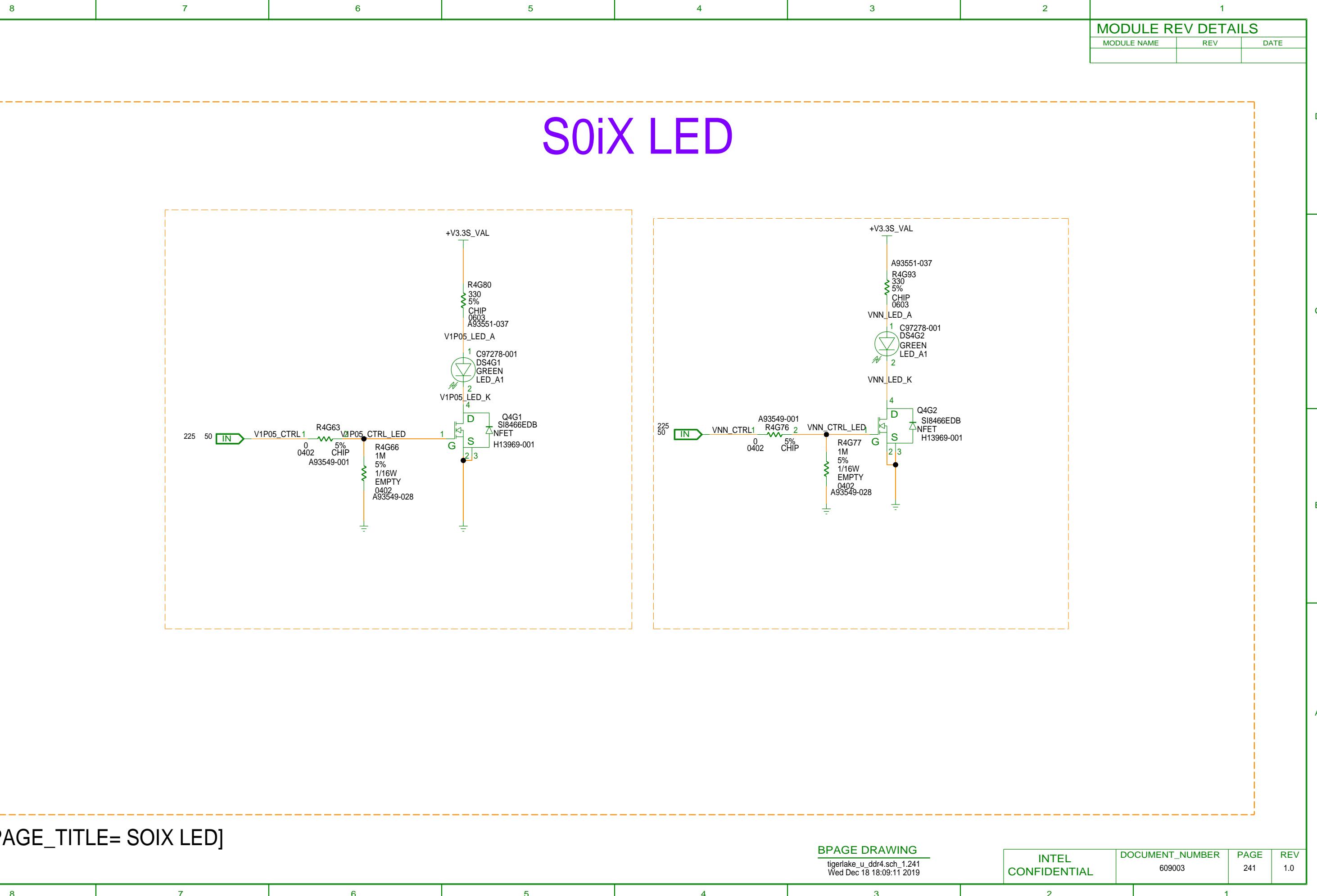


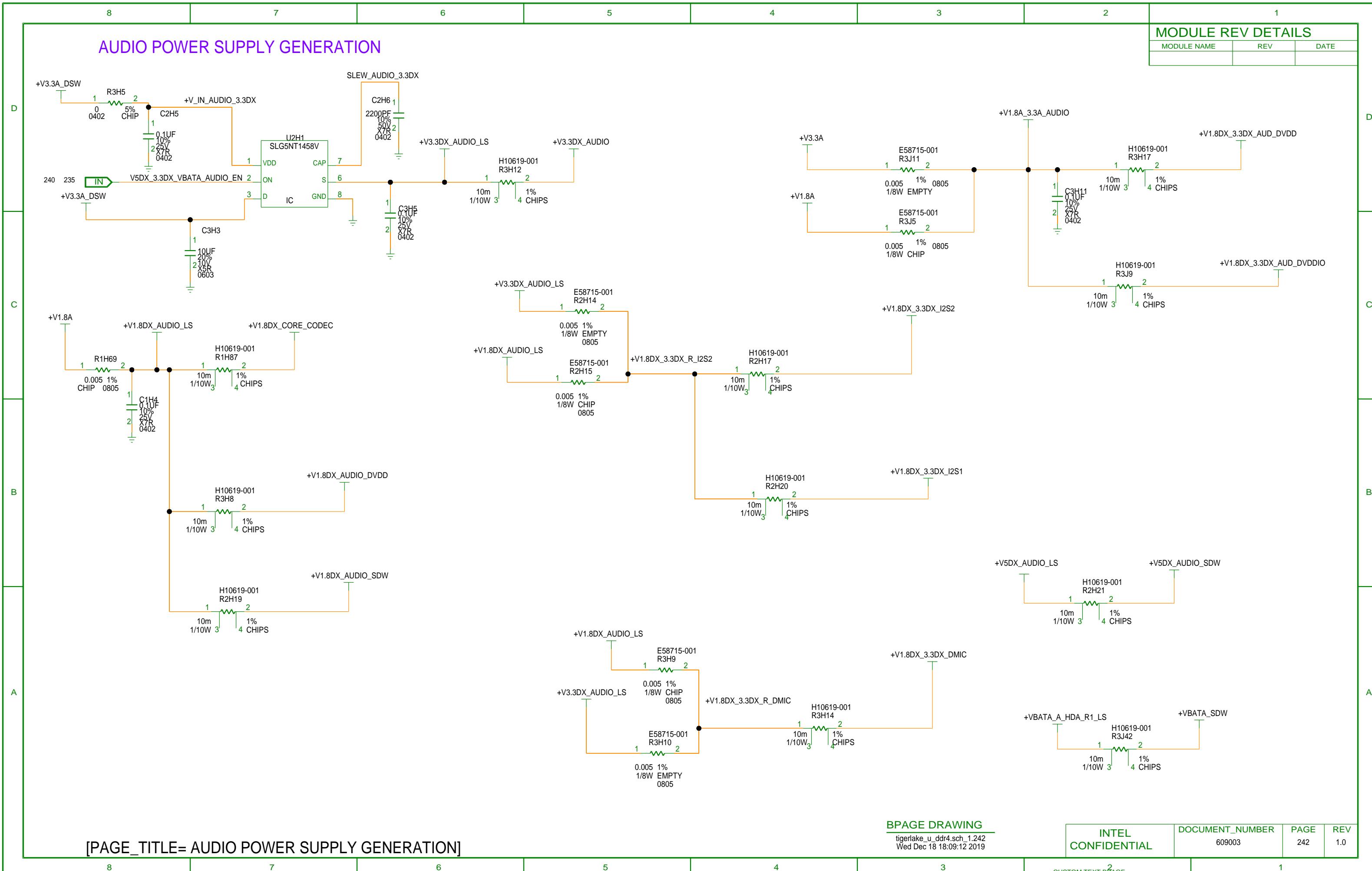


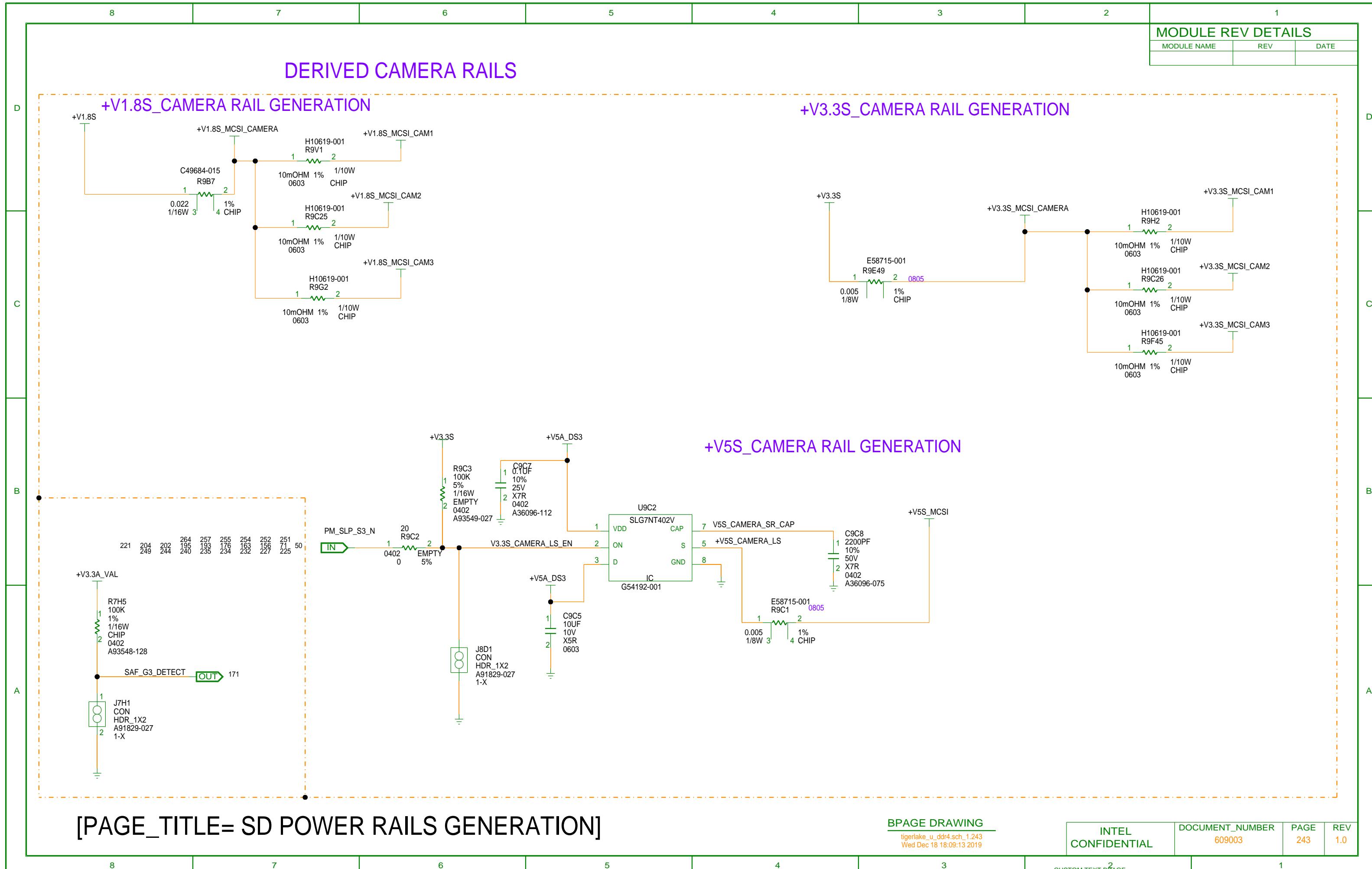


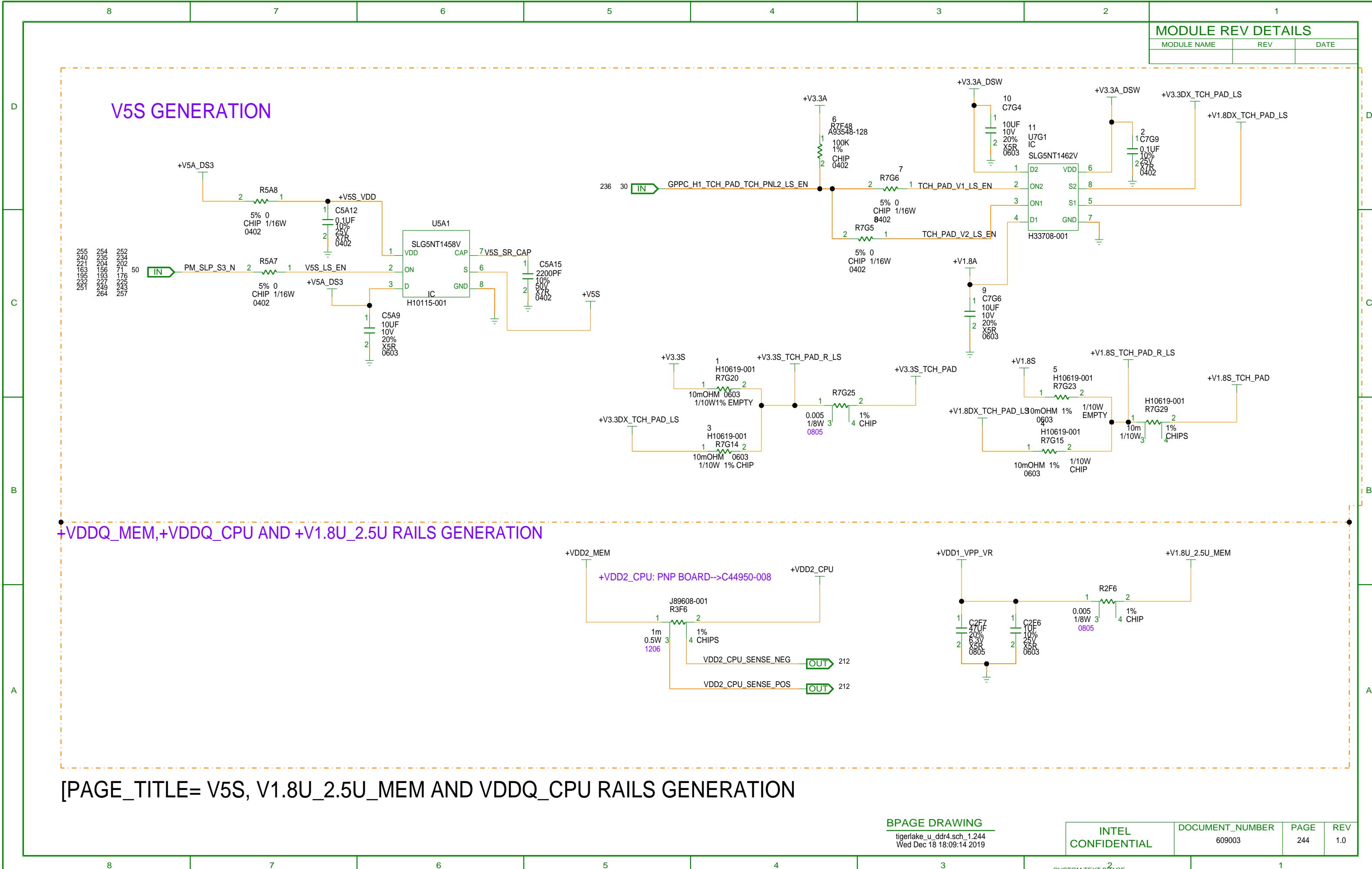






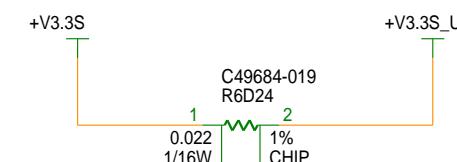
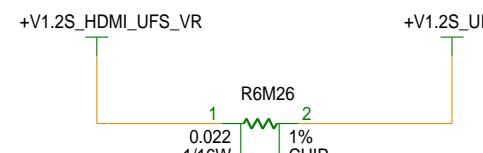
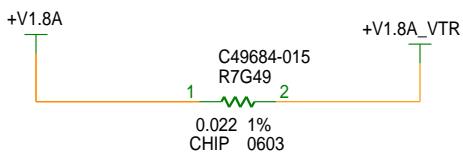
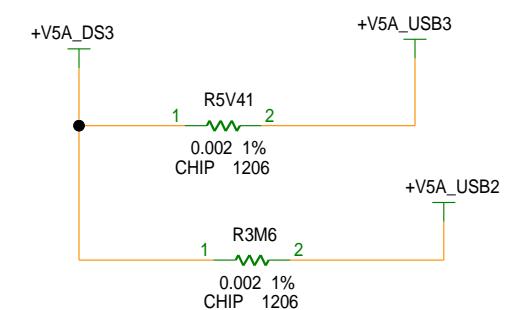
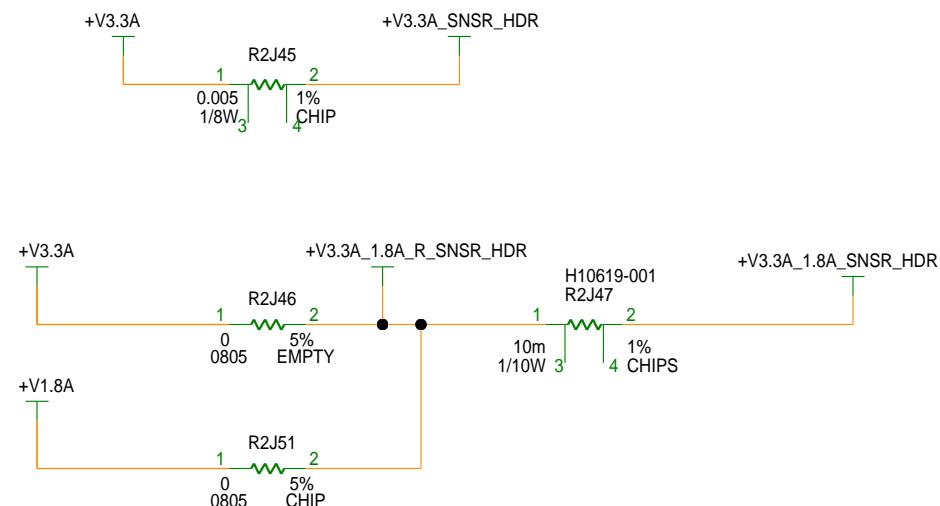
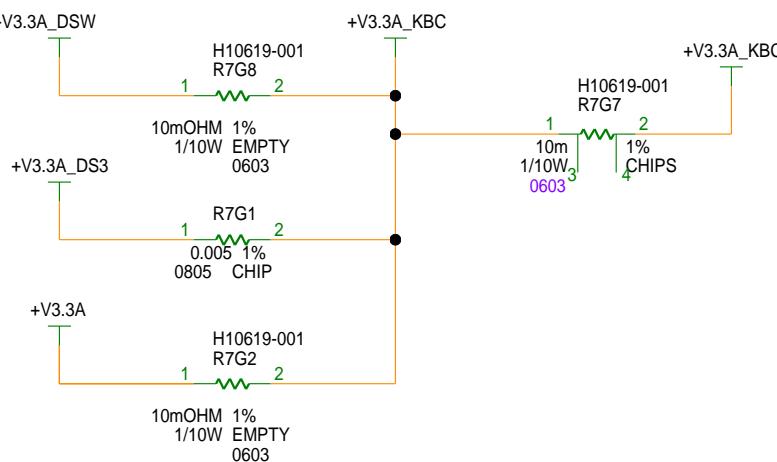


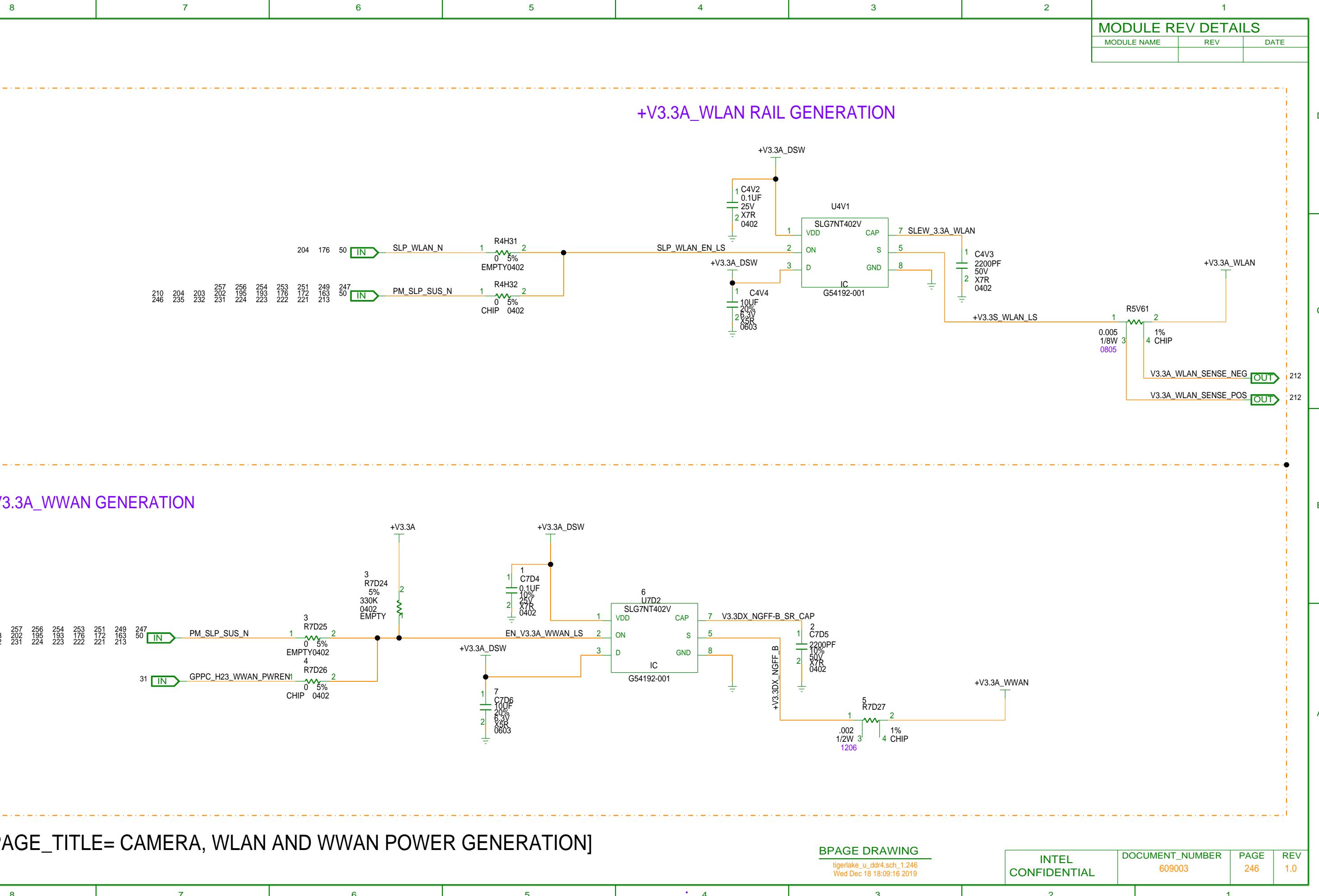


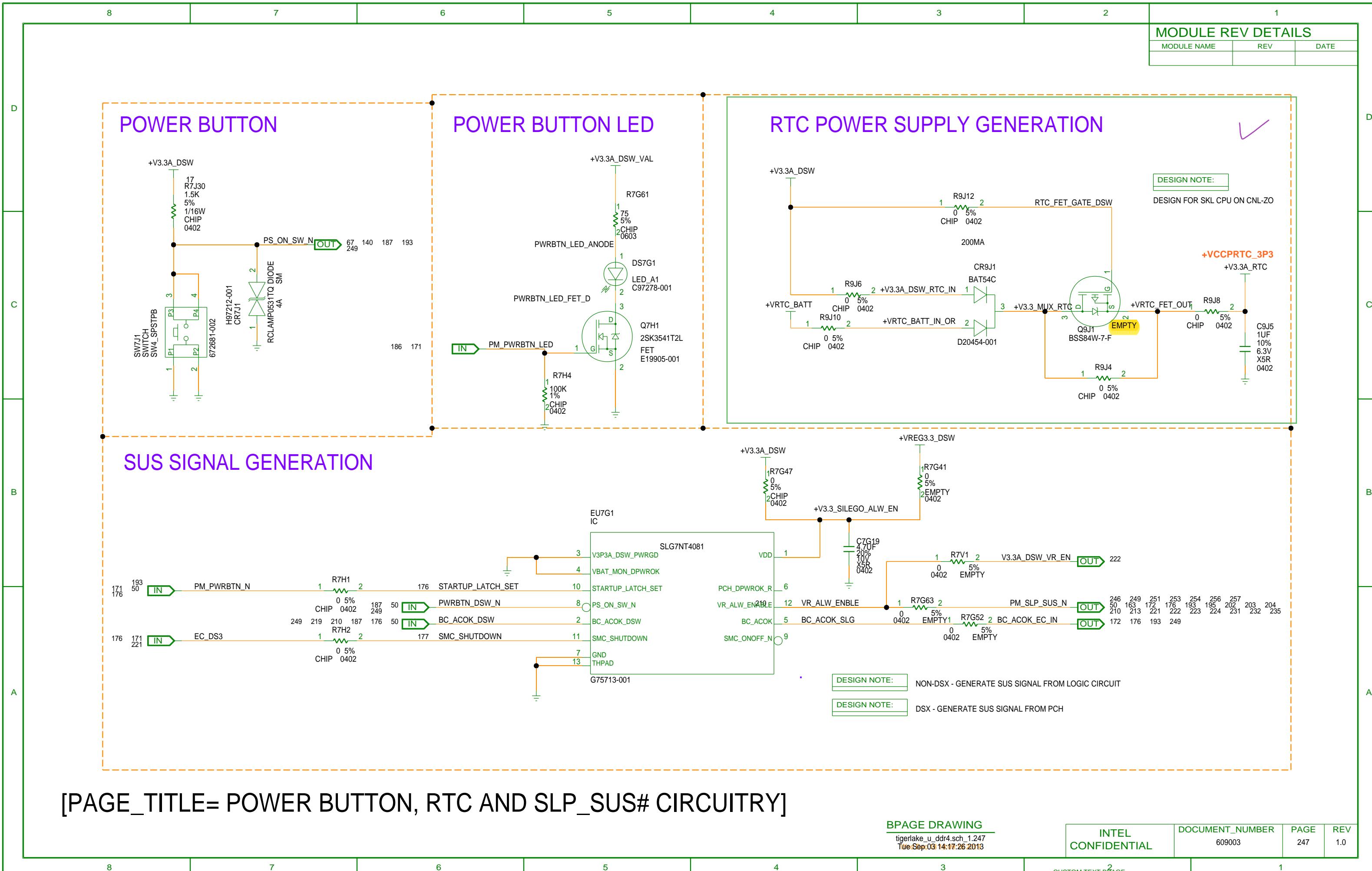


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<b>MODULE REV DETAILS</b>							

## DERIVED POWER RAILS

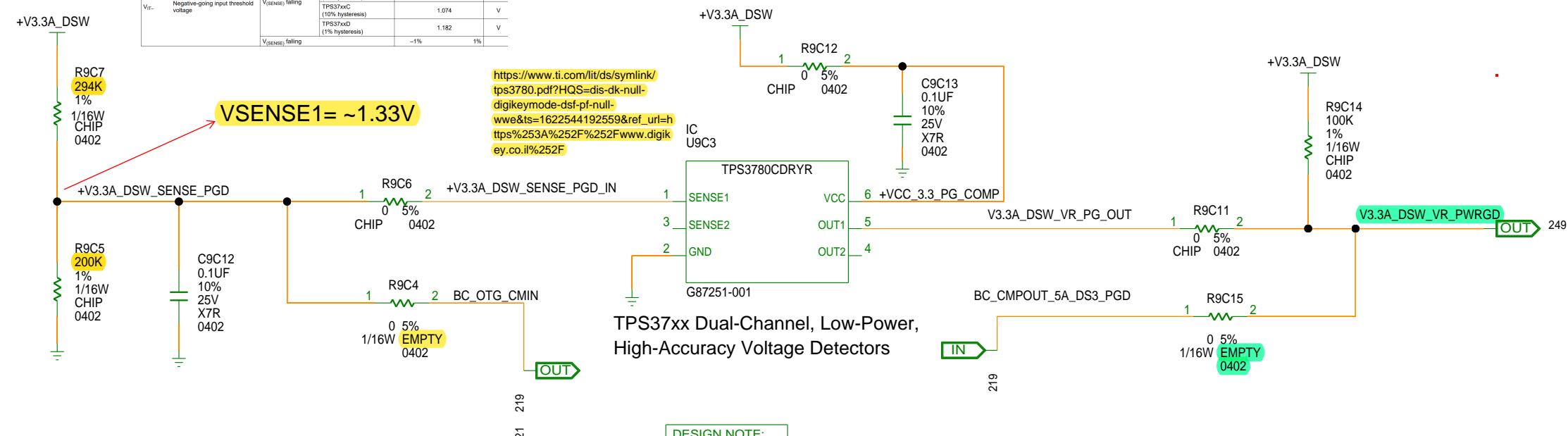
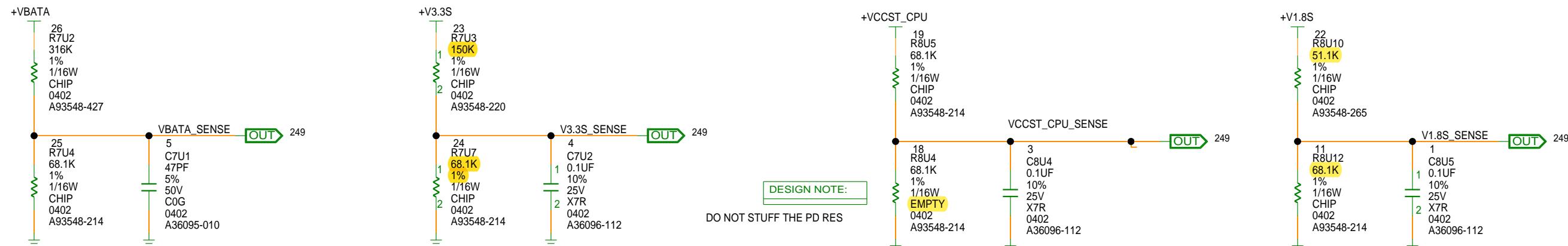






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MODULE NAME						REV	DATE

## POWER SEQUENCING LOGIC - PAGE I

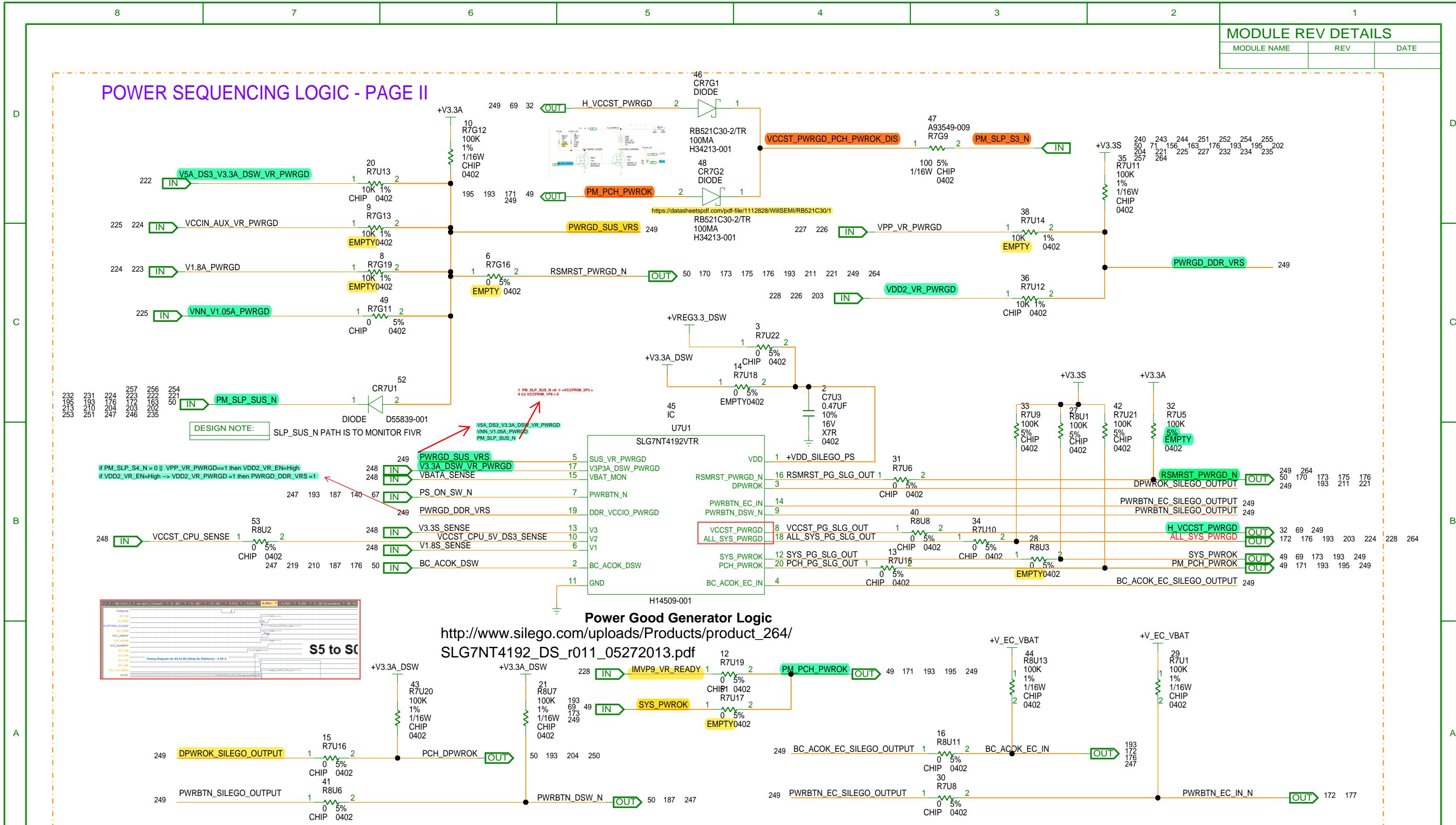


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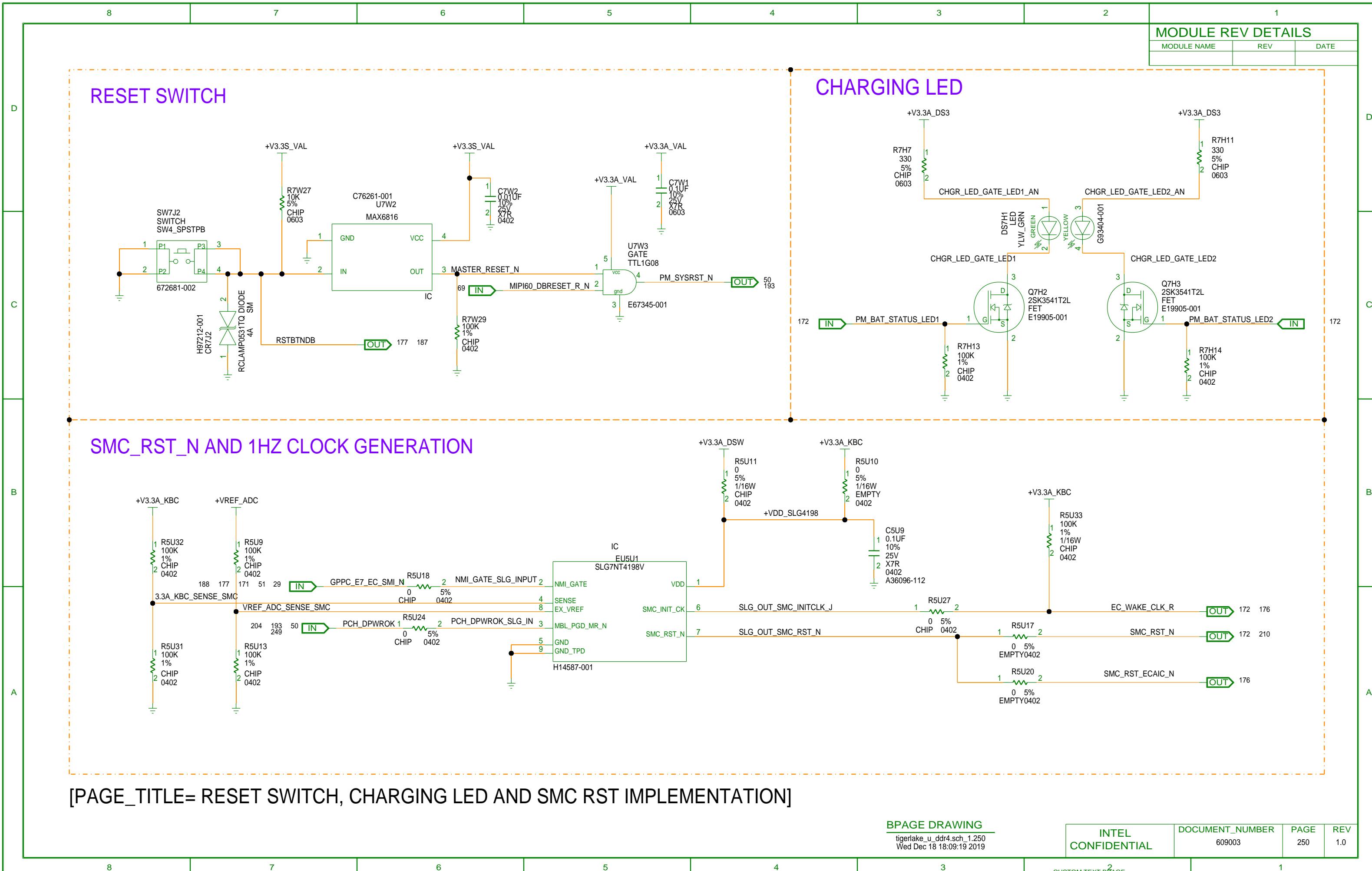
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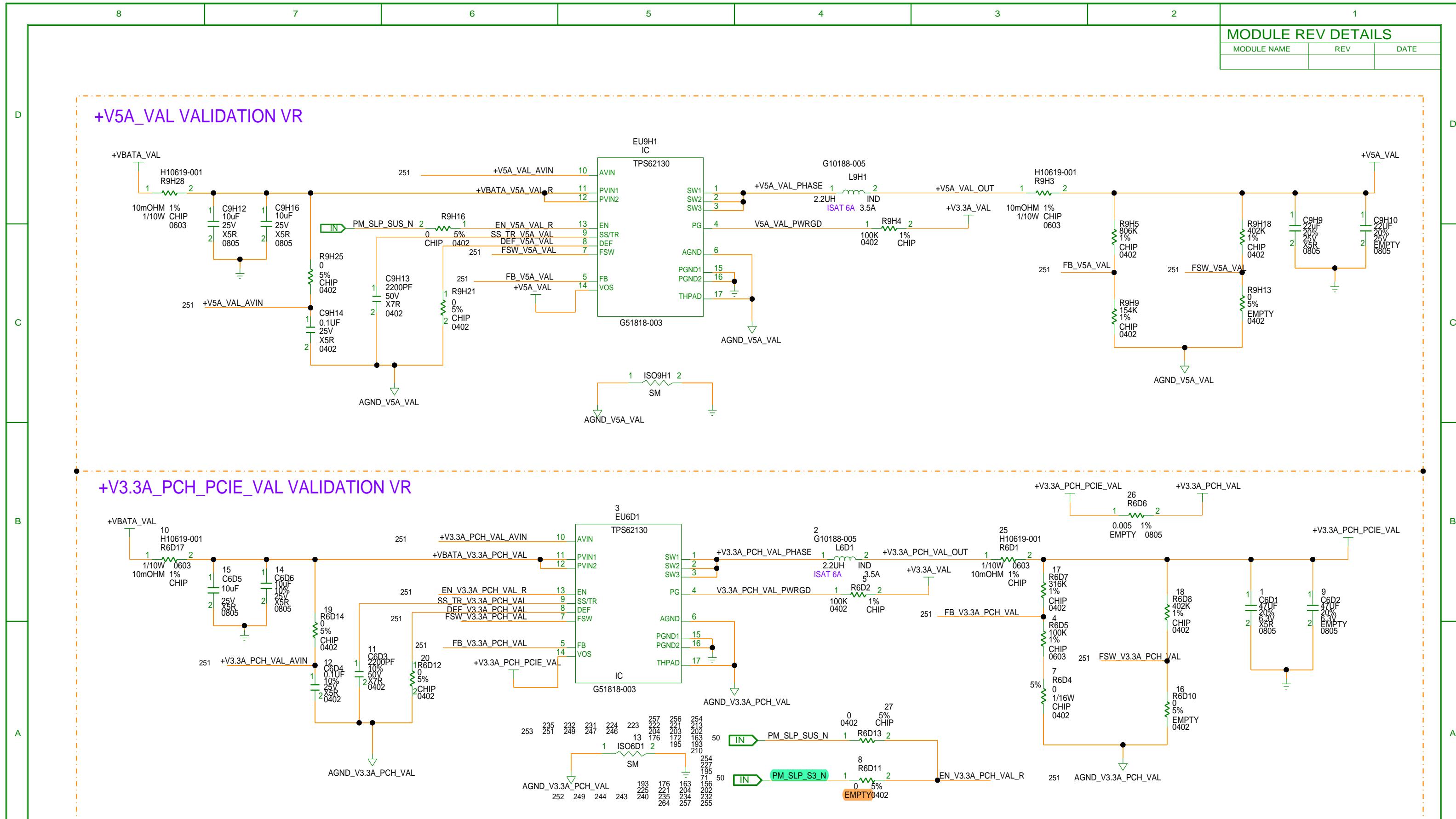


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Wed Dec 18 18:00:18 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 249	REV 1.0
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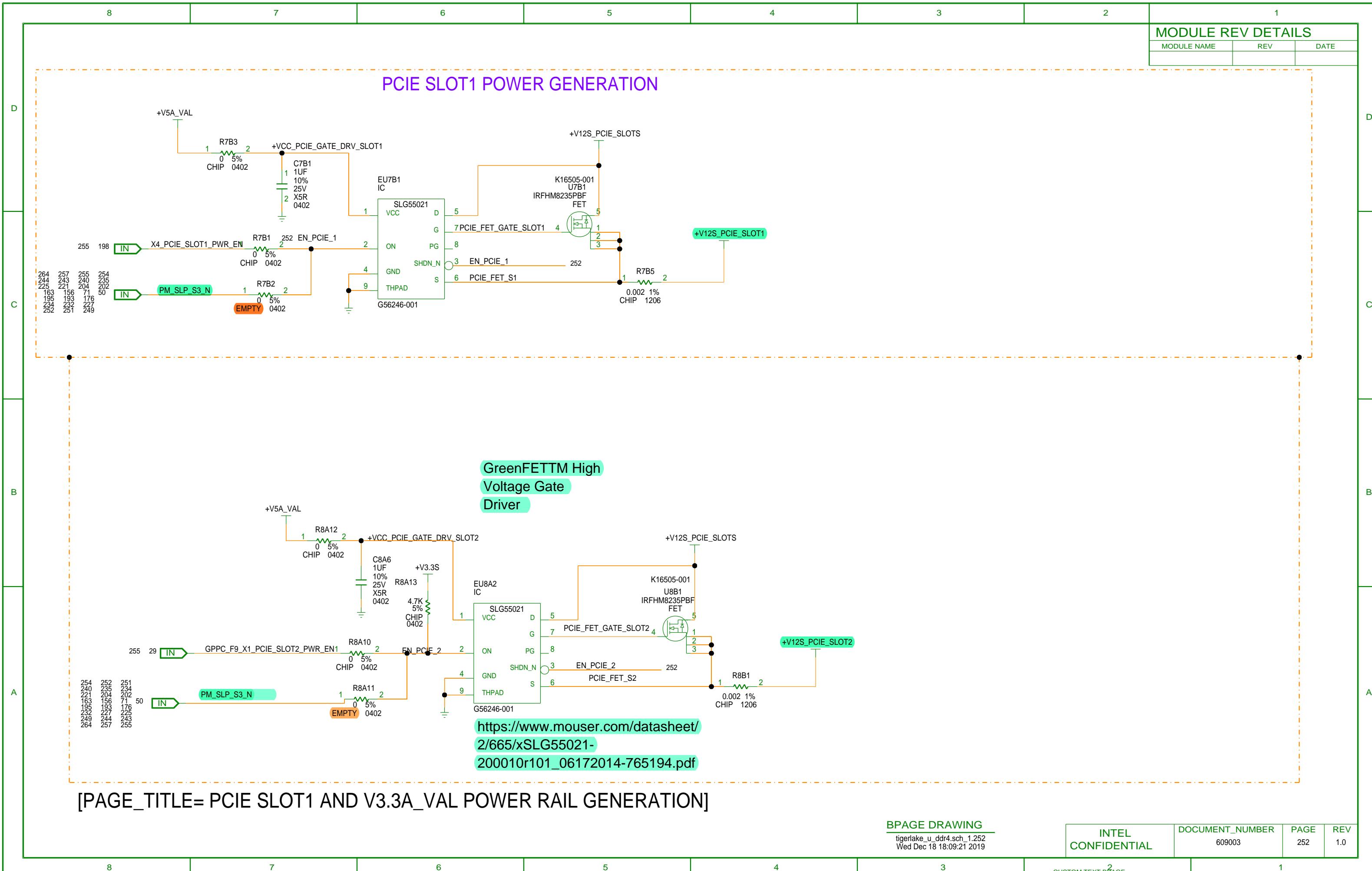


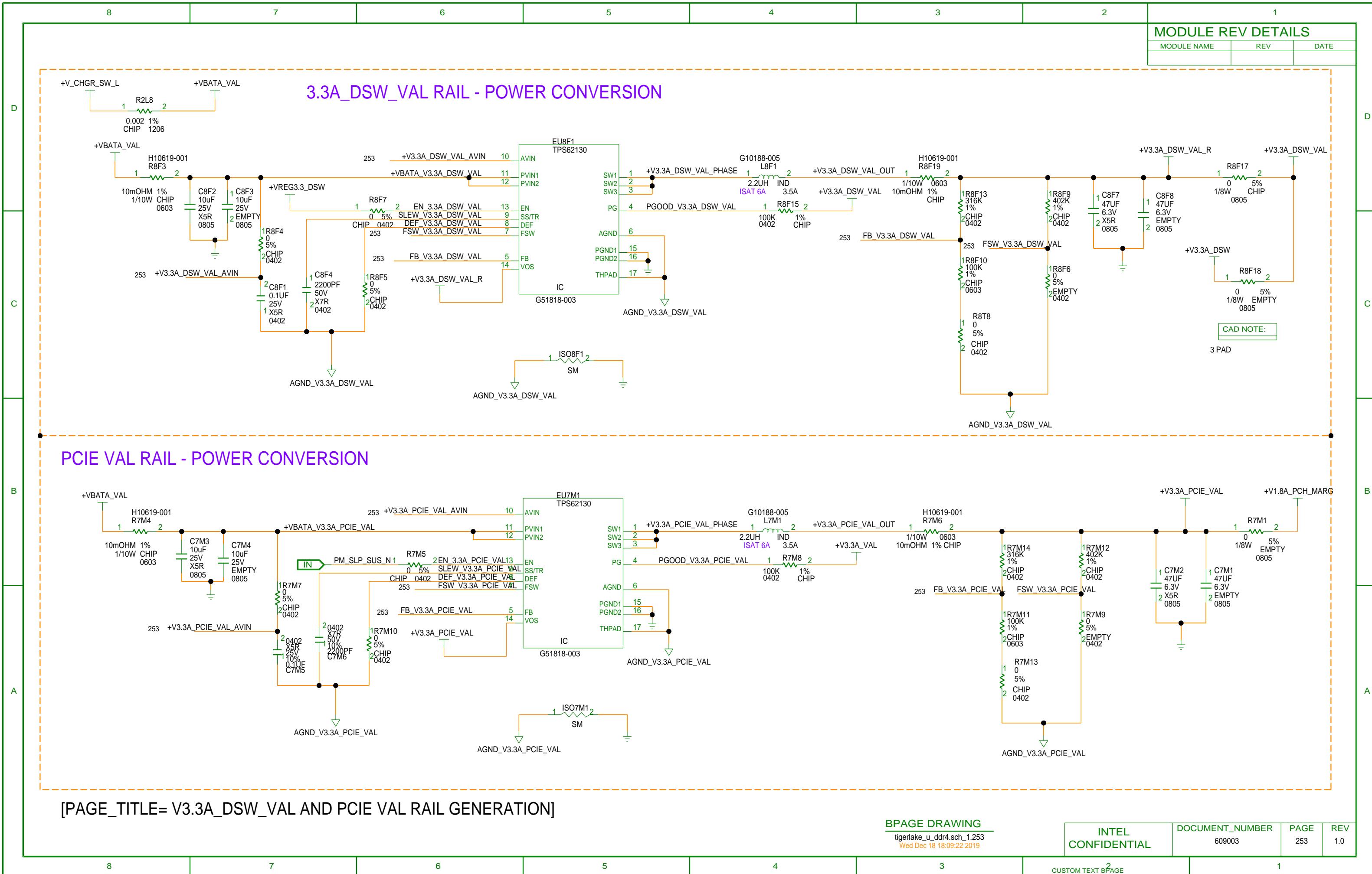
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BPAGE DRAWING

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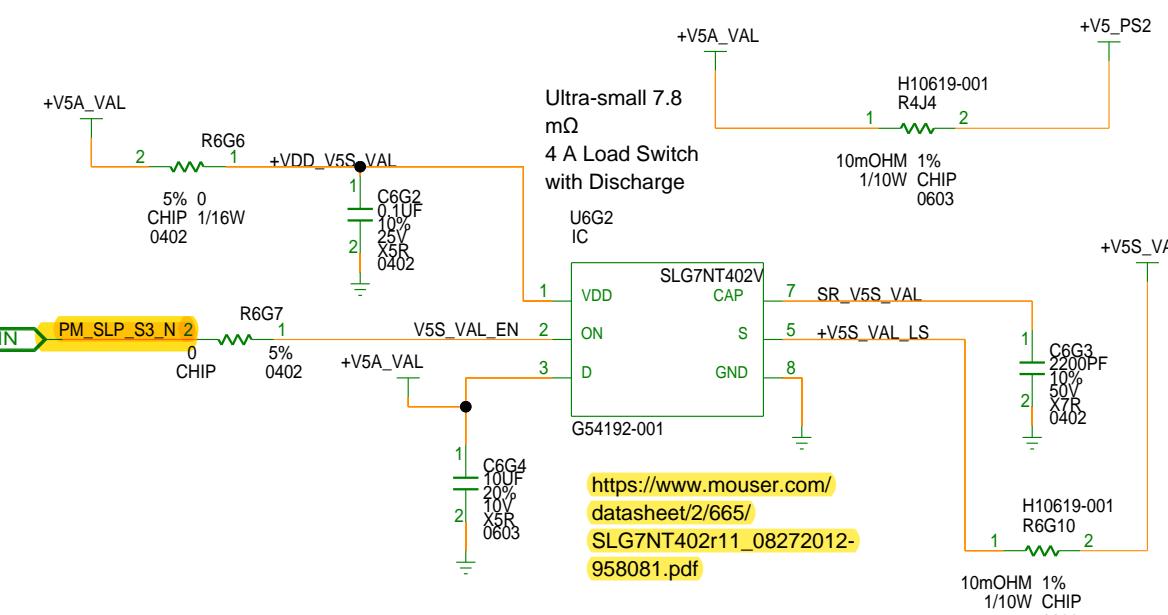
INTEL CONFIDENTIAL	DOCUMENT_NUMBER 609003	PAGE 251	REV 1.0
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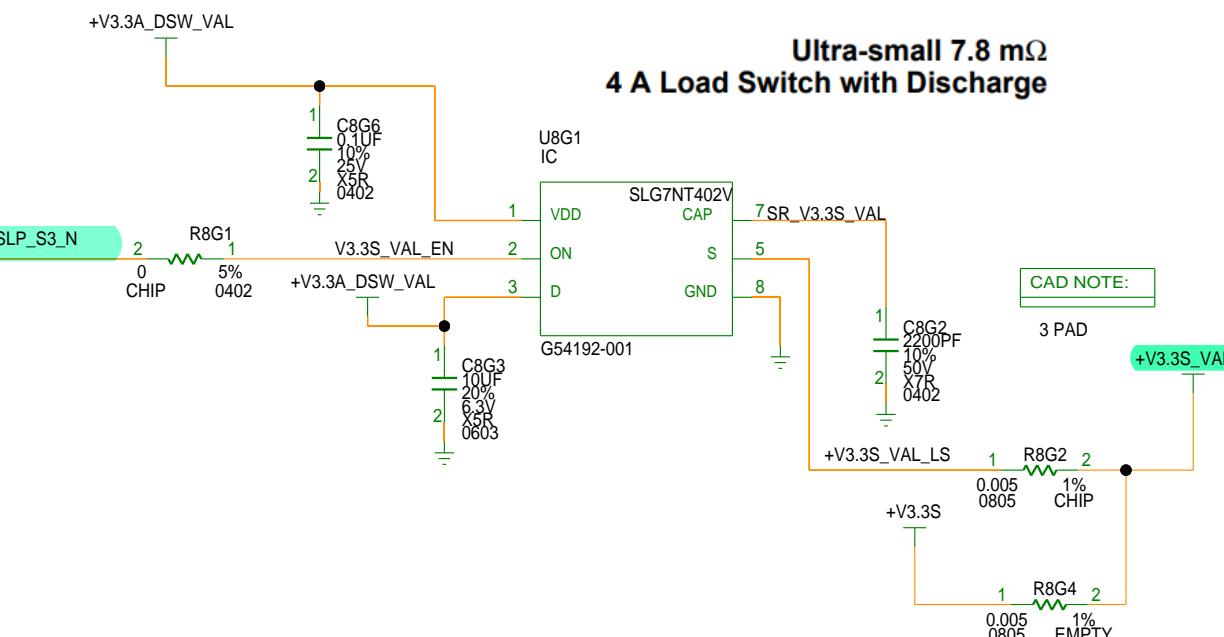


8	7	6	5	4	3	2	1
<b>MODULE REV DETAILS</b>							
MODULE NAME						REV	DATE

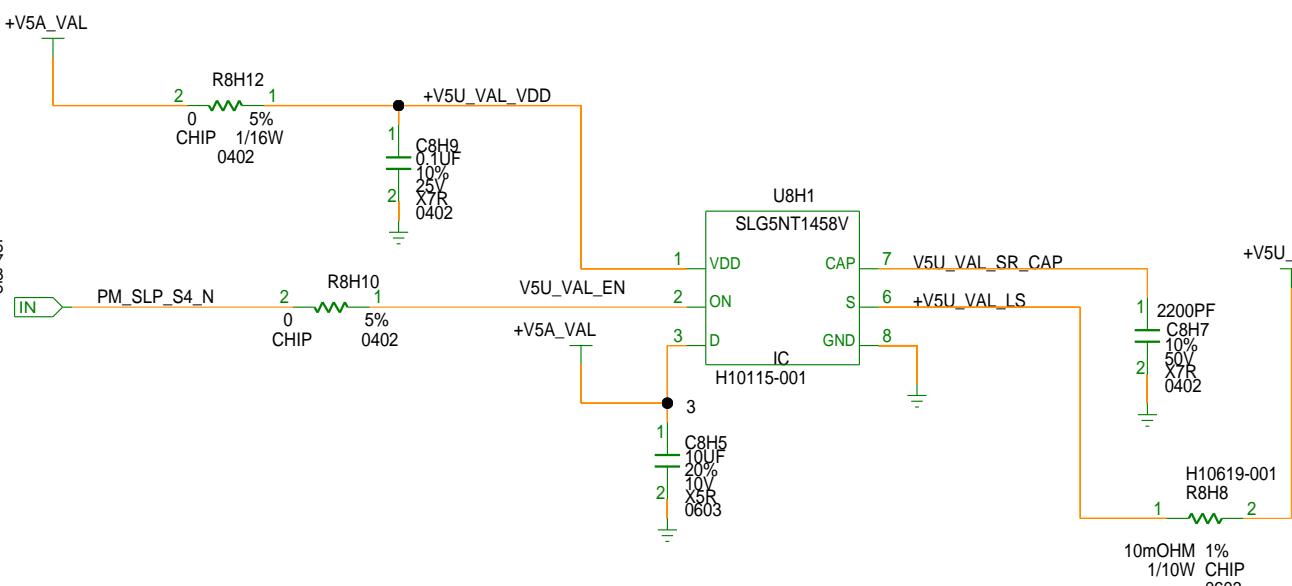
### V5S\_VAL GENERATION



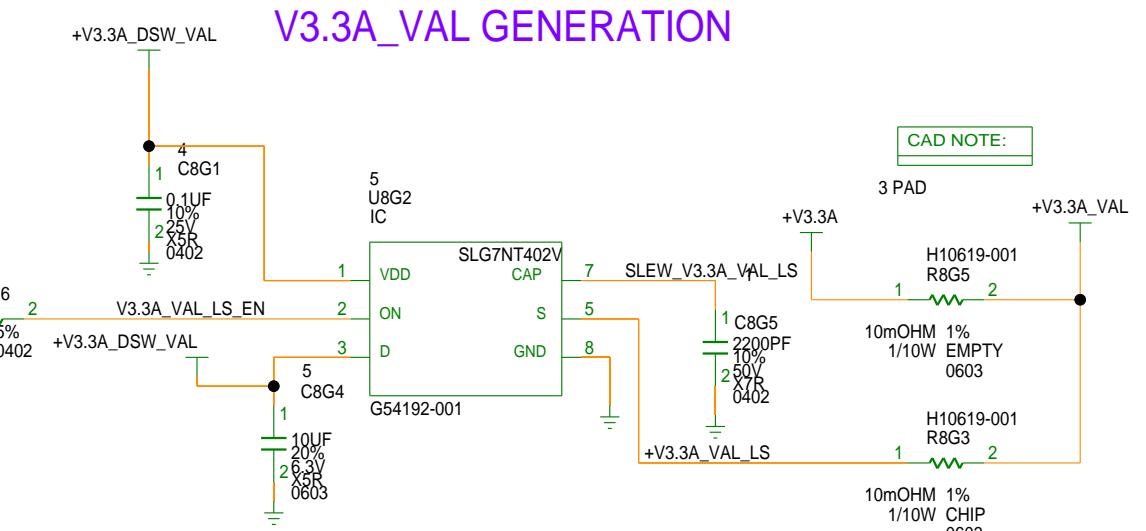
### V3.3S\_VAL GENERATION



### V5U\_VAL GENERATION



### V3.3A\_VAL GENERATION



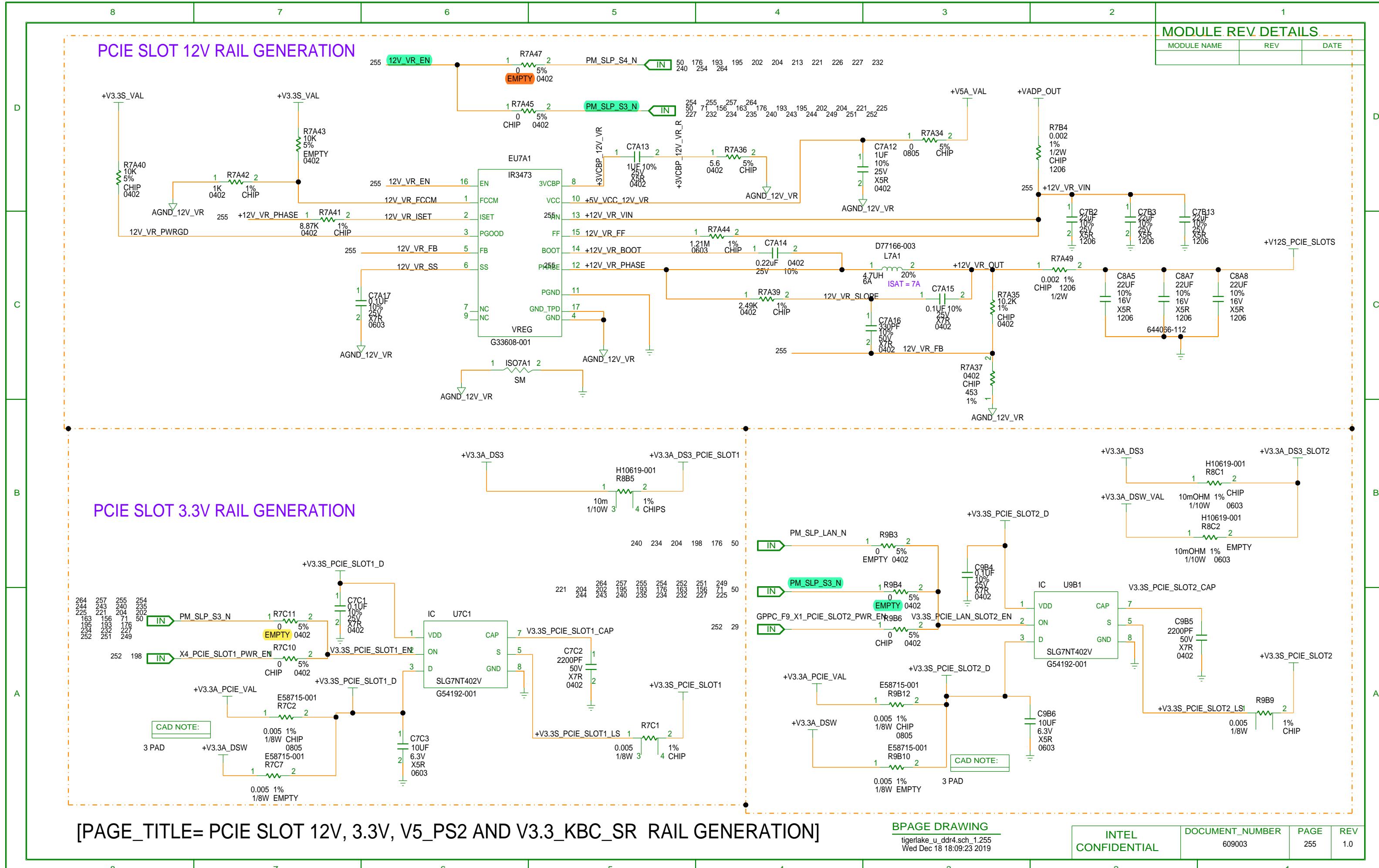
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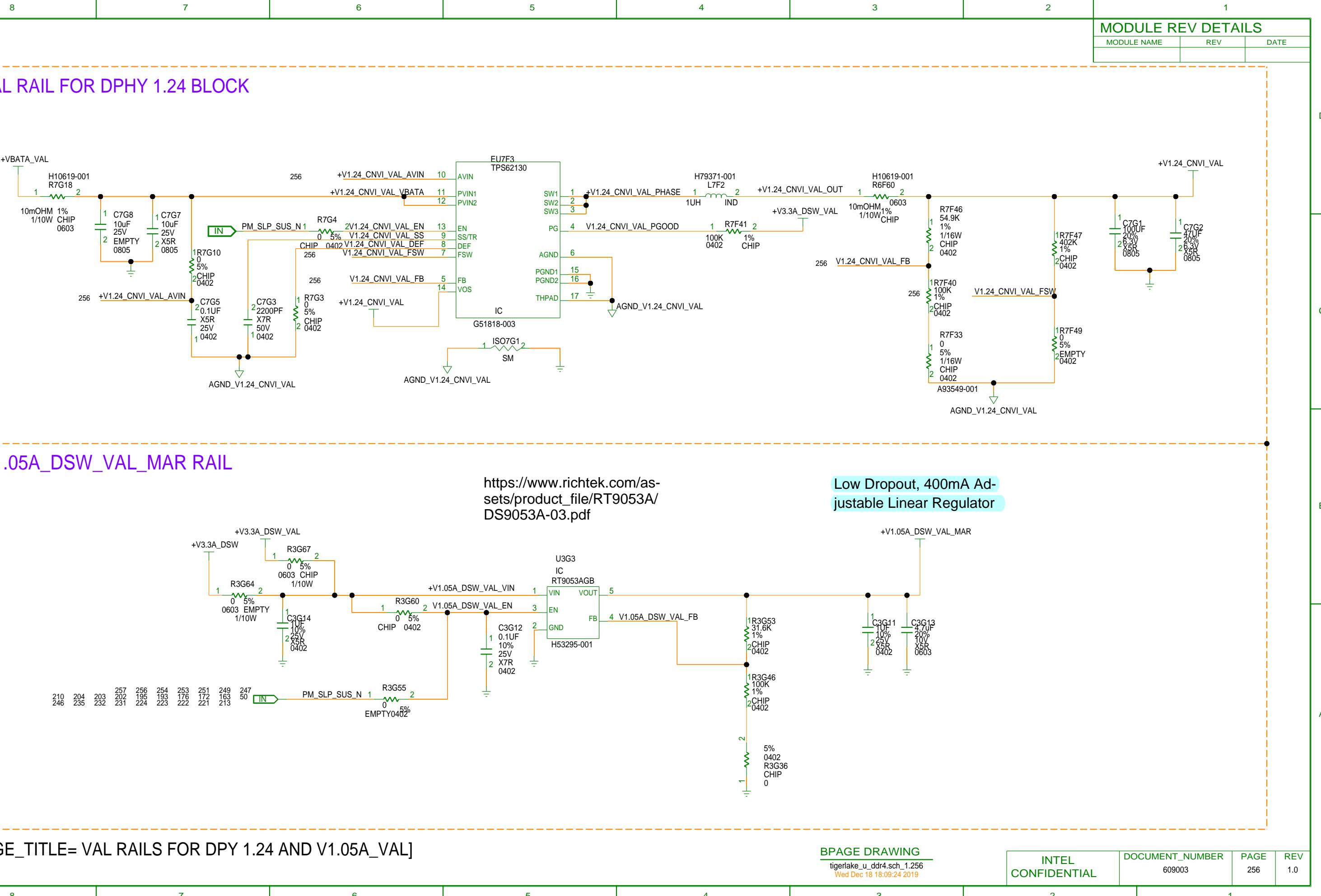
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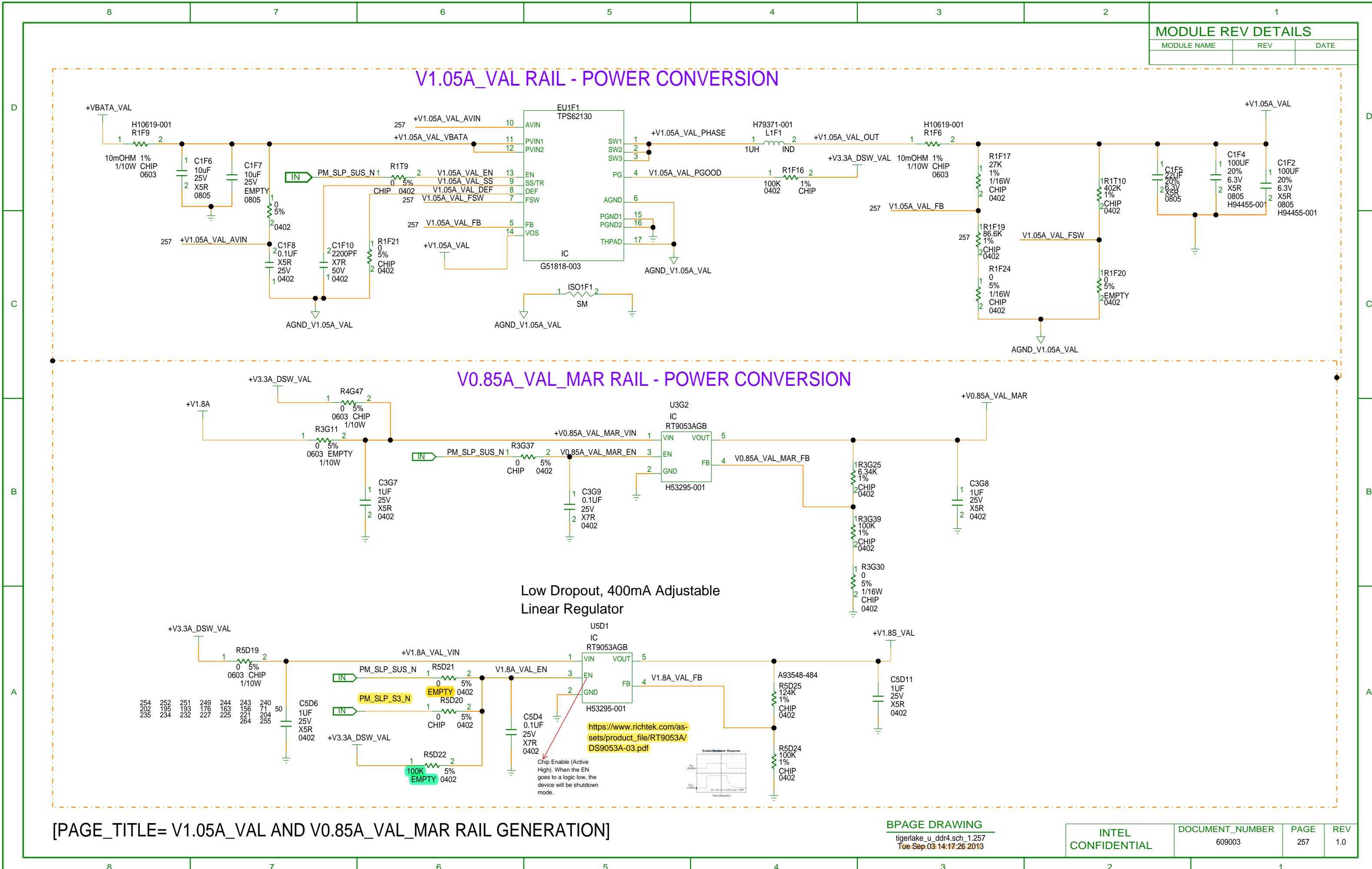
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Wed Dec 18 18:09:22 2019

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CUSTOM TEXT 2 PAGE







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MODULE REV DETAILS		
MODULE NAME	REV	DATE

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D

STF\_MTG\_HOLE  
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MH6J1  
MTG\_HOLE  
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G39082-001

STF\_MTG\_HOLE  
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GND=1,2,3,4,5,6,7,8  
G39082-001

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G39082-001

STF\_MTG\_HOLE  
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 9  
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G39082-001

C

C

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GND=1,2,3,4,5,6,7,8  
G39082-001

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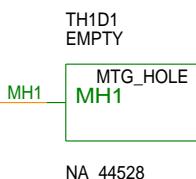
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G39082-001

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MTG\_HOLE  
 9  
GND=1,2,3,4,5,6,7,8  
G39082-001

B

B

STF\_MTG\_HOLE  
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ADDED FOR MEMORY INTERPOSER

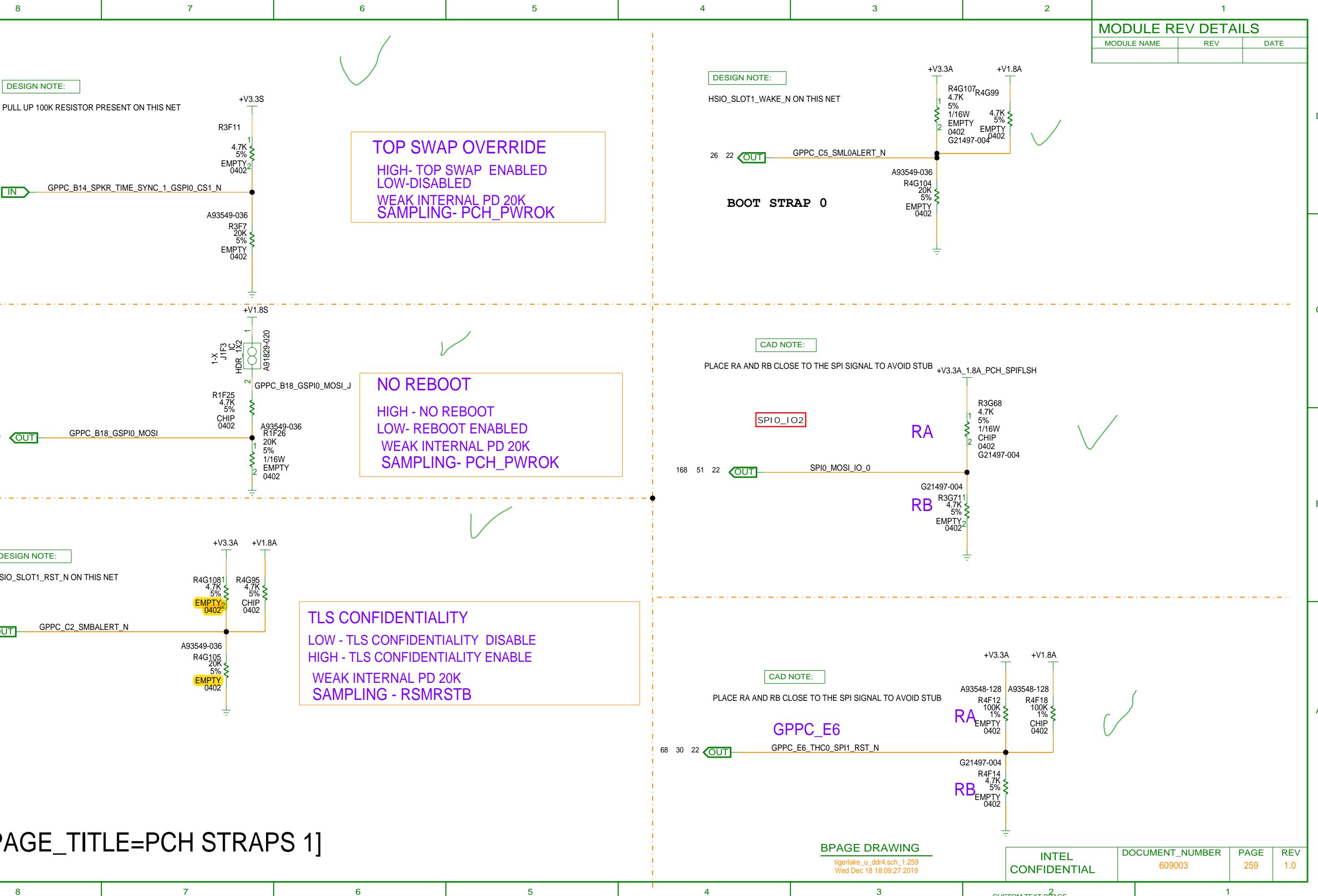
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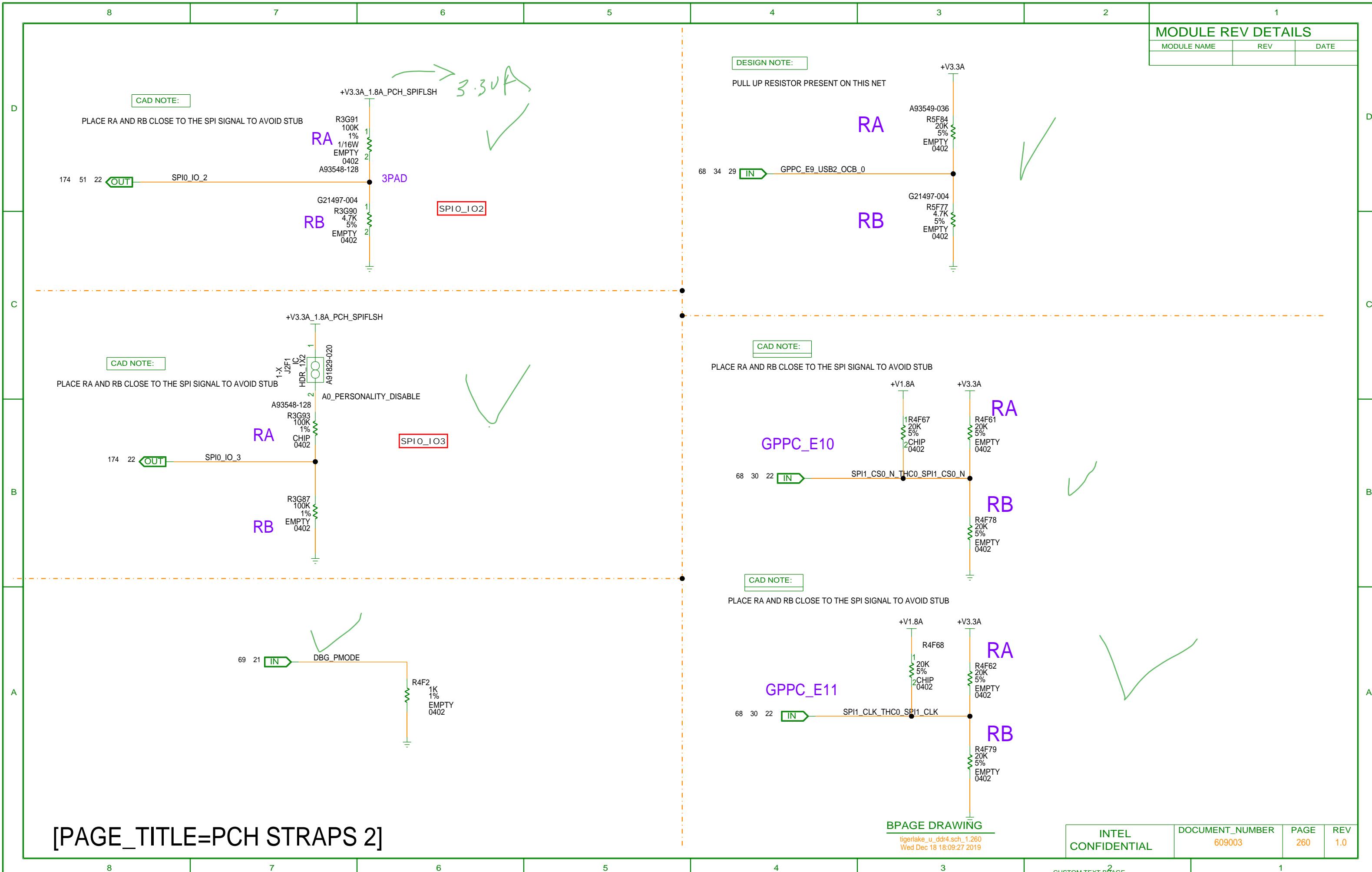
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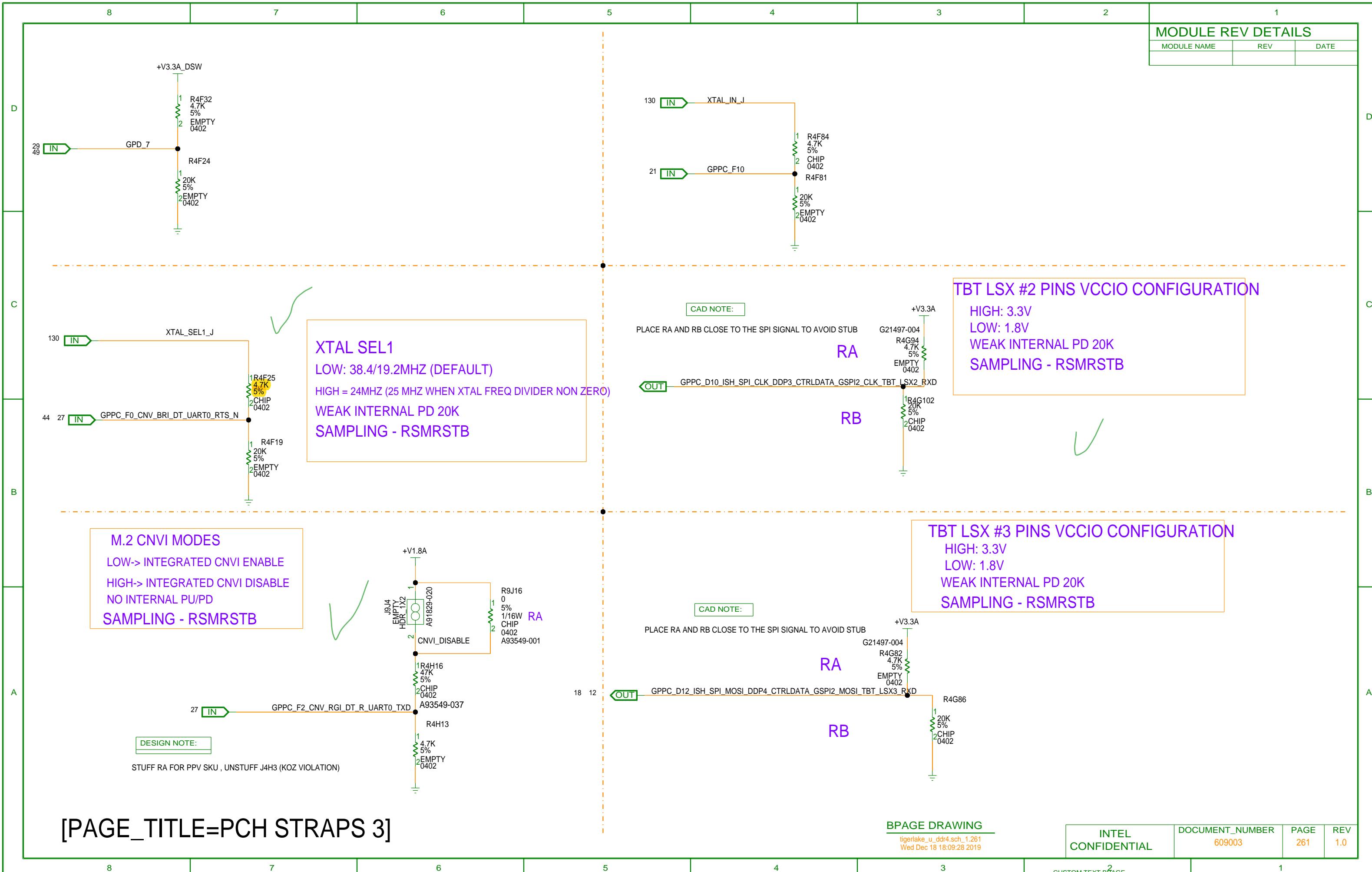
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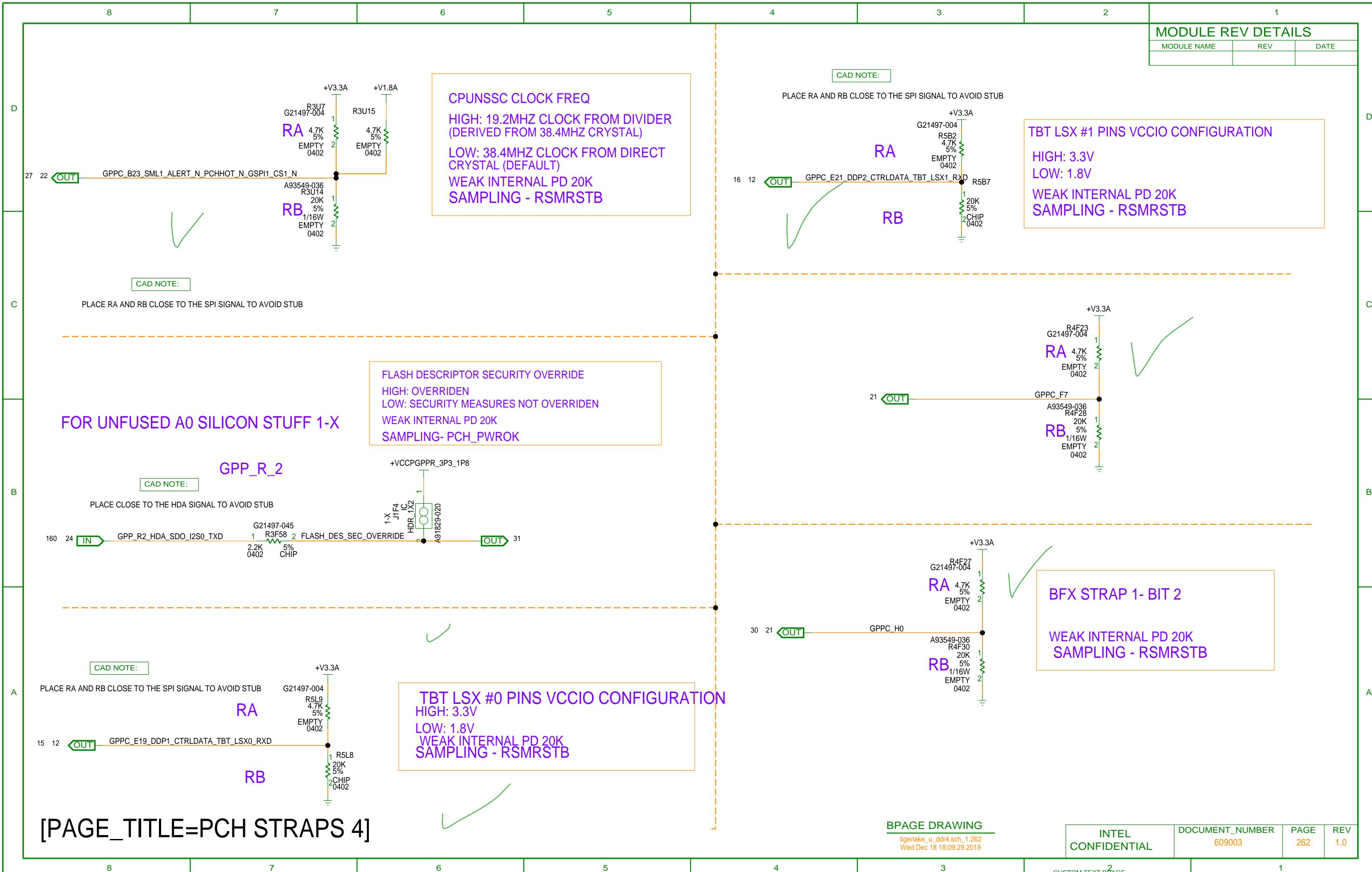
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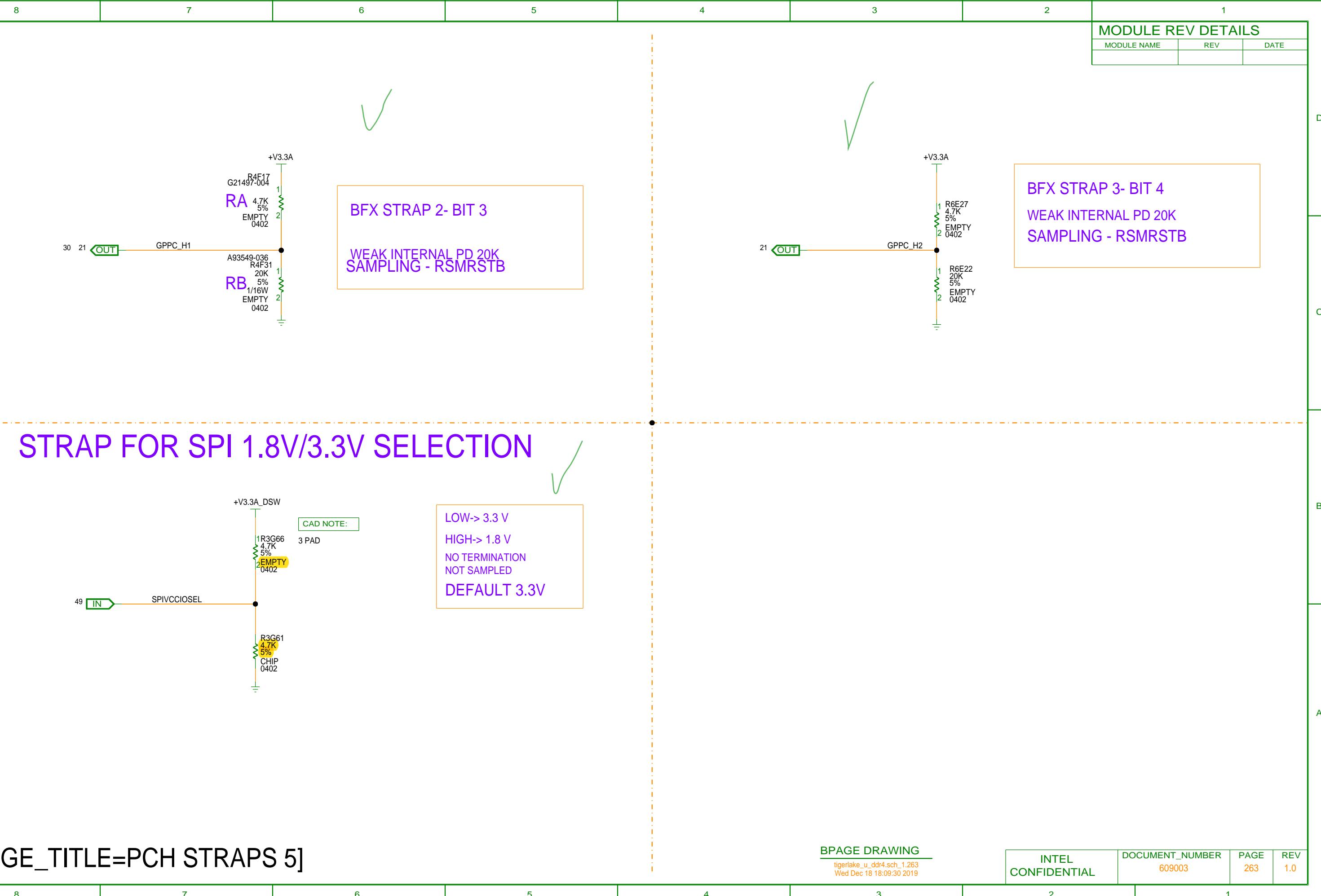
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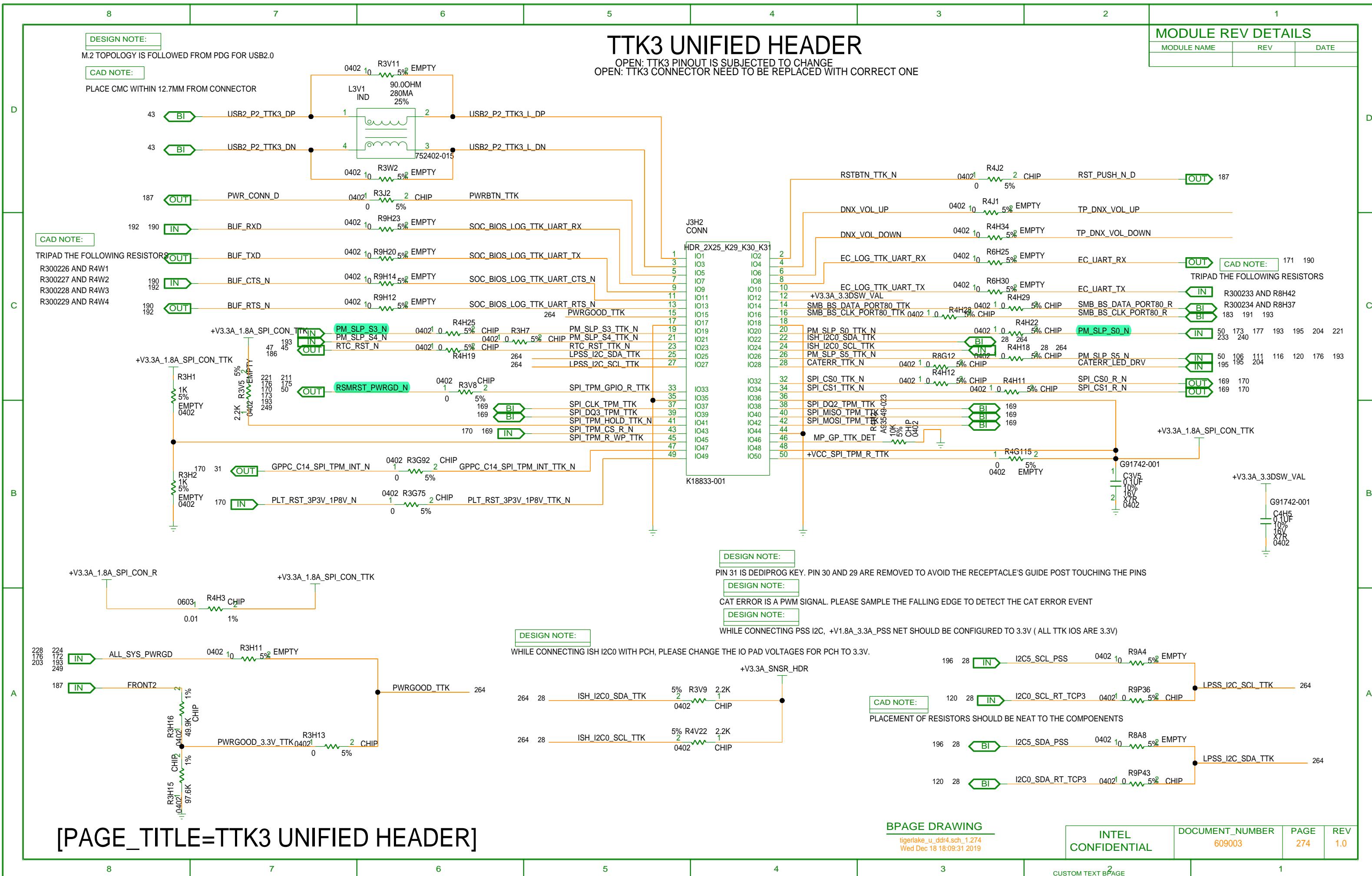


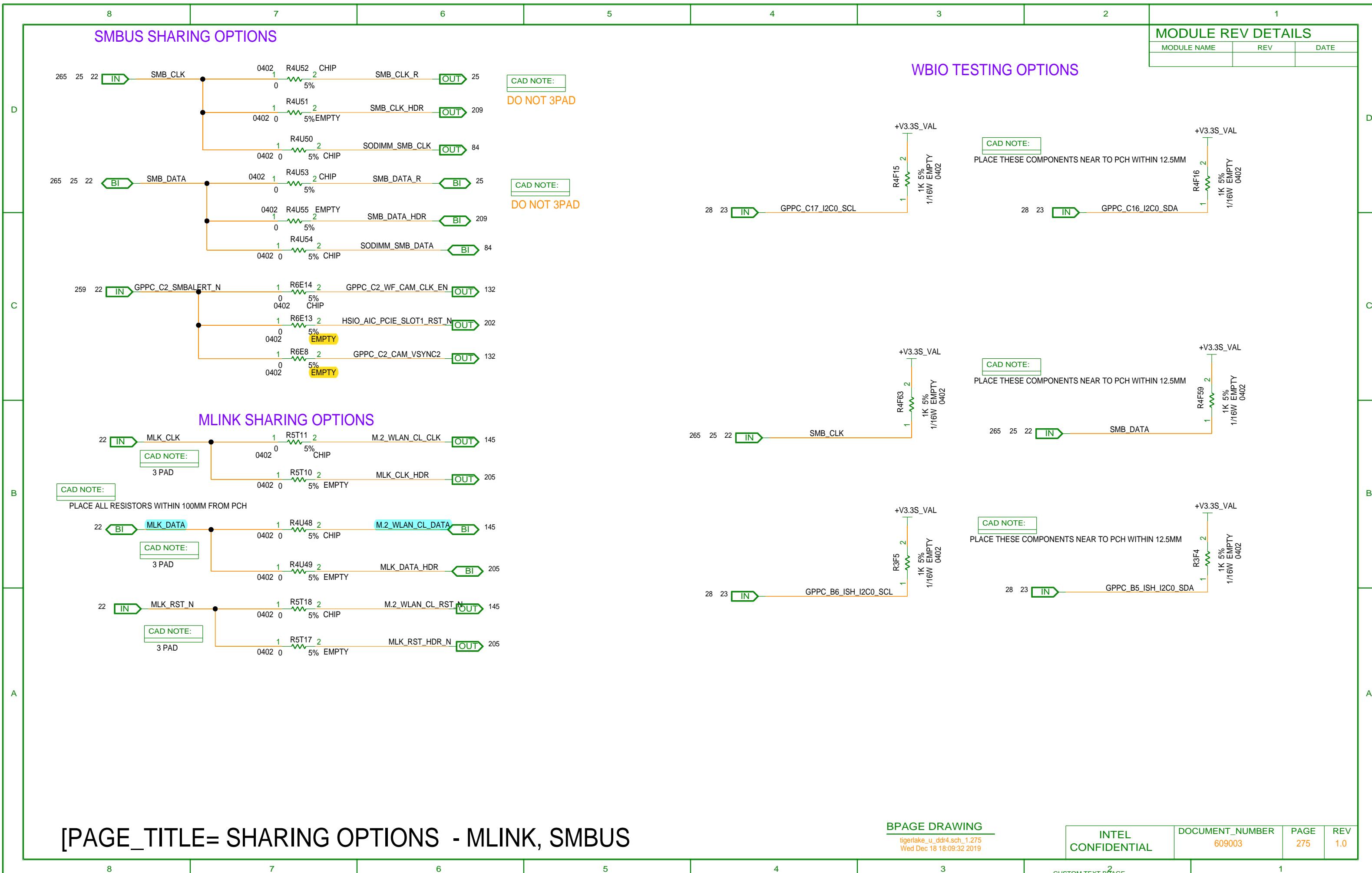


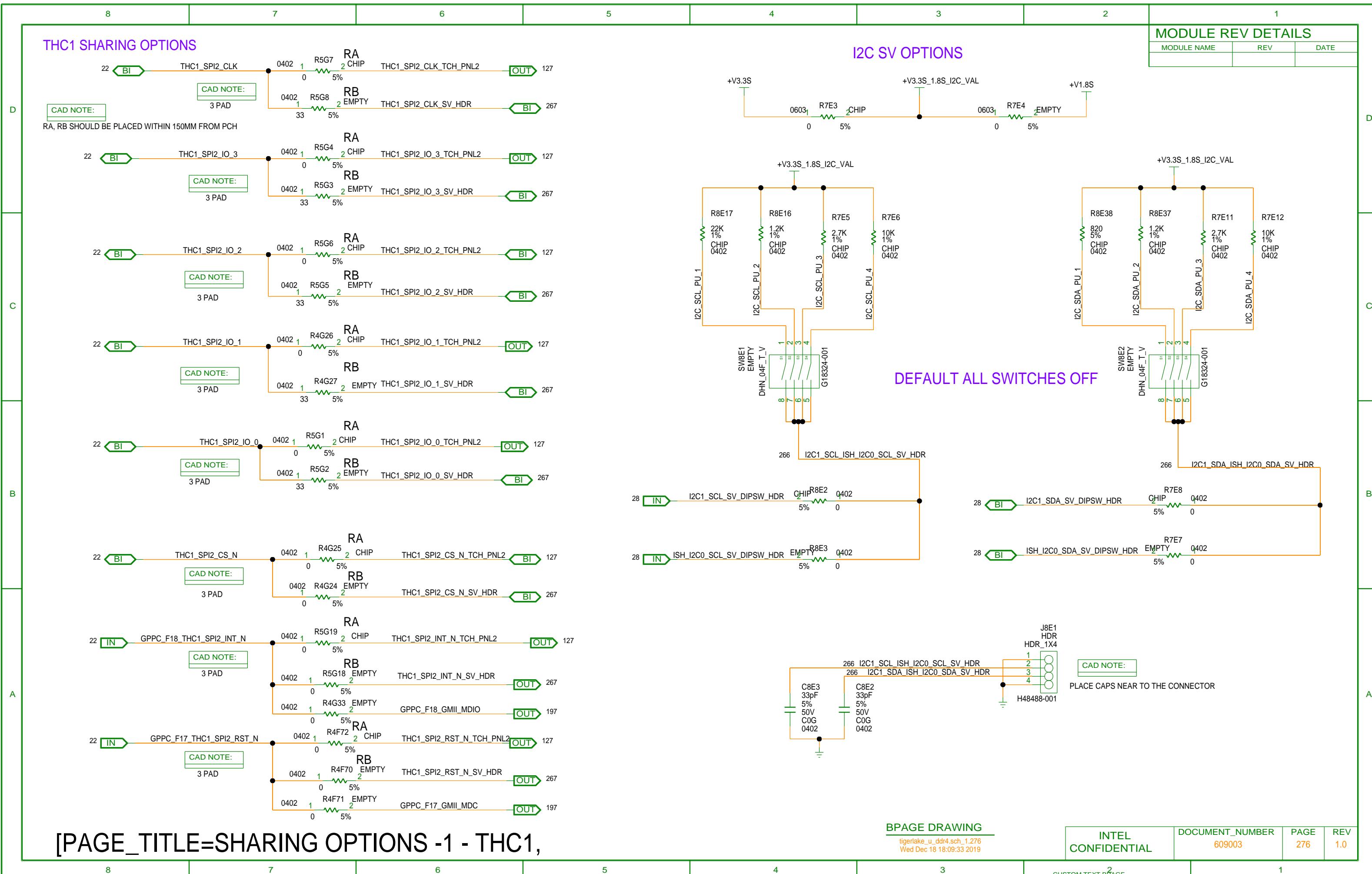












MODULE REV DETAILS		
MODULE NAME	REV	DATE

D

D

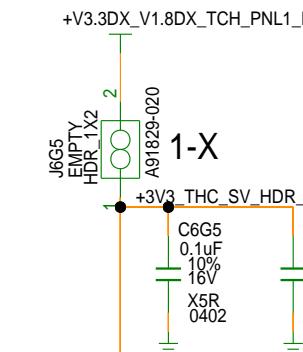
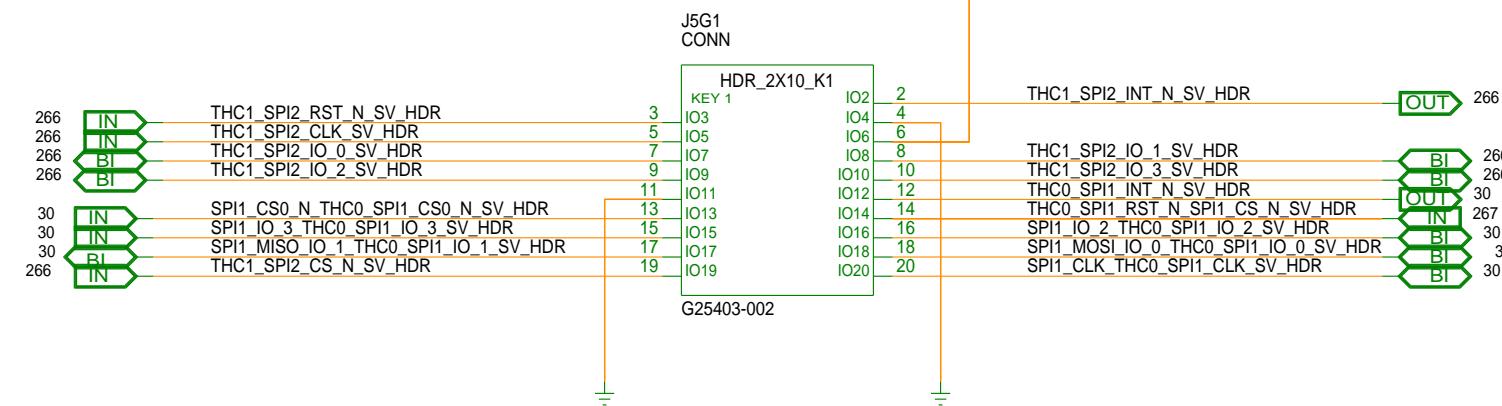
## THC0 , THC1 AND SPI1 SV VALIDATION HEADER

**DESIGN NOTE:**

ONLY SINGLE LOAD IS SUPPORTED. 1.8V IO:RA=33E, 3.3V IO IS NOT POR AND NOT SUPPORTED  
MAX CABLE LENGTH SUPPORTED IS 203MM

**CAD NOTE:**

PLACE RA CLOSE TO CONNECTOR WITHIN 25MM, FOR ALL SIGNALS  
PLACE CONNECTOR WITHIN 250MM FROM PCH



**DESIGN NOTE:**

ON LKF, SPI1 CS1 AND THC0 RESET ARE MULTIPLEXED. HENCE SAME OPTION IS MAINTAINED VIA RESISTOR STUFFING REWORK ON TGL FOR UNIFICATION BETWEEN PLATFORMS

