Lab 7 (100 points): Sequential Logic Design

Objectives

- Use the sequential logic design process to design a three-bit counter.
- Learn how to use D/JK/T Flip-Flops in VHDL.
- Use the testbench to validate the designed code before implementation.

Demo Due: It will be graded in the last 30 min of your lab session.

Submission:

Submit the followings

1. State table
2. Logic circuit you design
3. your_design.vhd files for FF and design
4. your_design_tb.vhd files for Testbench of your simulation
5. .xdc file for your pin assignment
6. screenshots of your post synthesis simulation waveform

Lab

In this lab assignment,

A) You will first design, 3-bit counter with input (push button). Whenever the button is pressed, count up by one.
   a. Create state table.
   b. Derive the optimized expression for chosen FF(D/JK/T).
   c. Draw your circuit.
B) Write a VHDL code for FF.
C) Functionally simulate, and implement a flip-flop (Write the testbench).
D) If the waveform is correct, you can move the next step.
E) Implement 3-bit counter by using flip-flops. You are supposed to use three FF with necessary gates. Write a VHDL code.
F) Functionally simulate your VHDL code of your design. Test all the possible case, see the Figure 1.

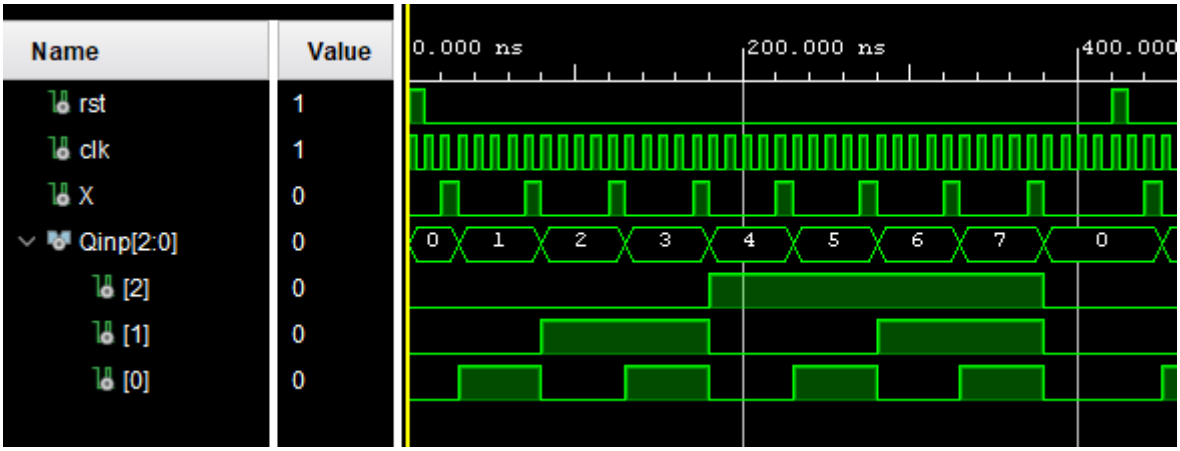

Figure 1 Example of acceptable simulation result. X is the push button, Qinp is the output of the circuit. You do not need to add reset.

G) If the waveform is correct, assign pin numbers to the input and output signals of your designed circuit (create .xdc file). Pick one push button for the input, use 3 LEDs for the outputs and use clk as a clock.

Grading Criteria:

1. (20 points) Create the state table and derive the optimized/minimized Boolean expression in sum of products form (D/JK/T flip-flops all are accepted).

2. (20 points) Write the VHDL code and simulate your FF design.

3. (30 points) Implement 3-bit Counter. Functional verification with behavioral simulation: Write a testbench to functionally simulate.

2. (20 points) Synthesize your design. Write .xdc file to assign the pins. Functional verification with post synthesis simulation.

3. (10 points) Ready to demo on the board (Generate Bitstream).