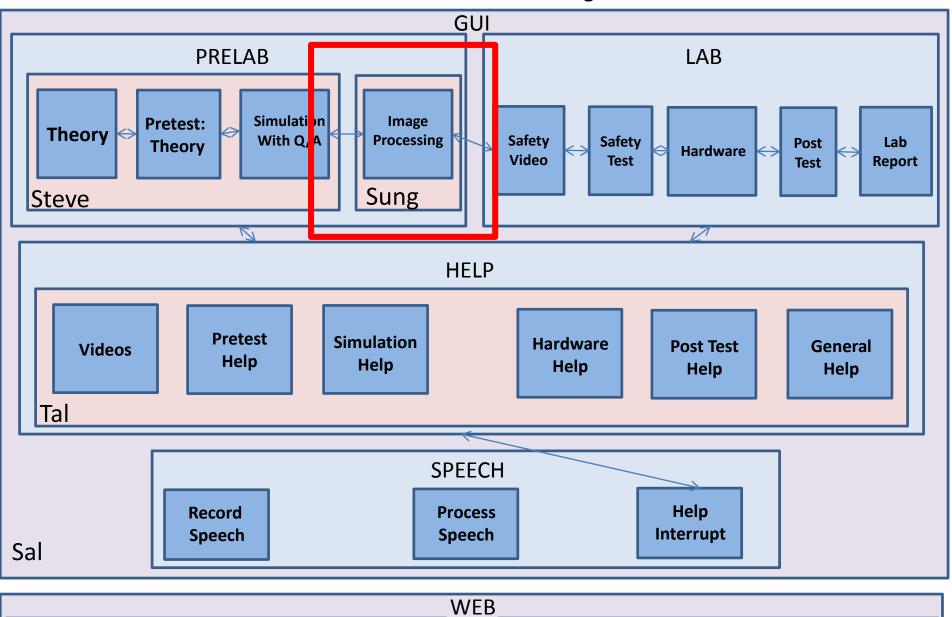
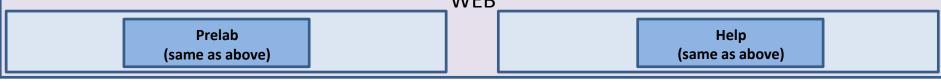
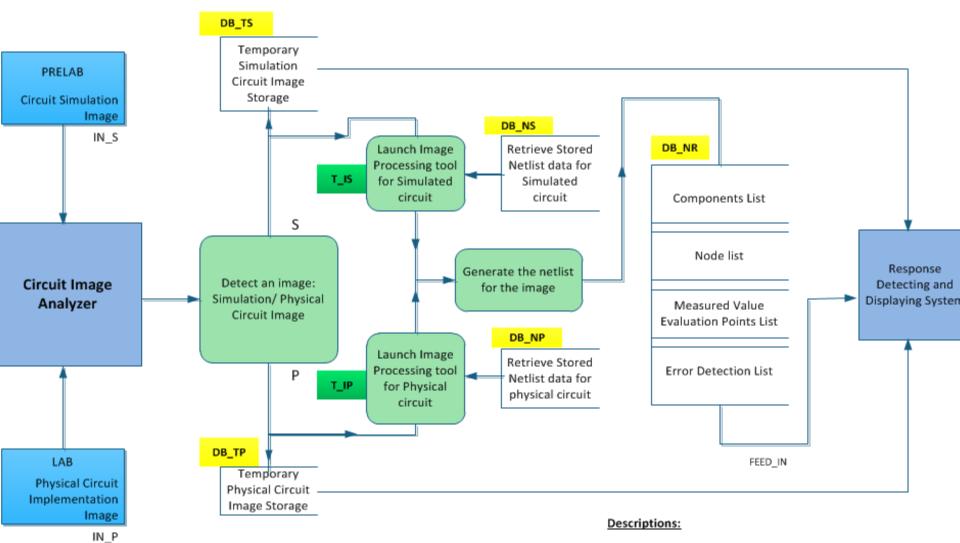
### VLA Functional Block Diagram

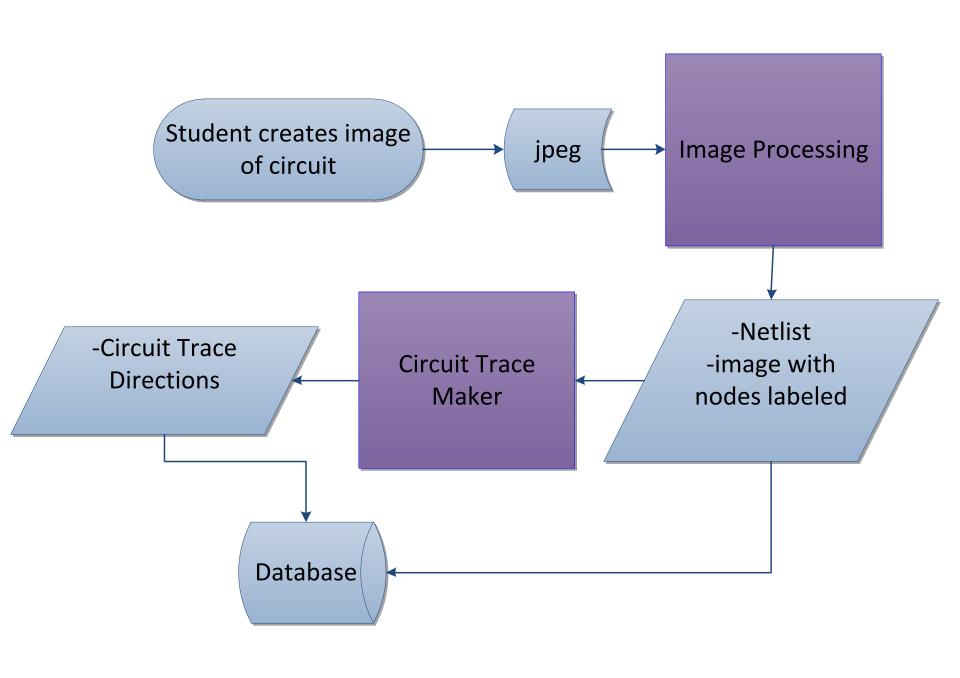




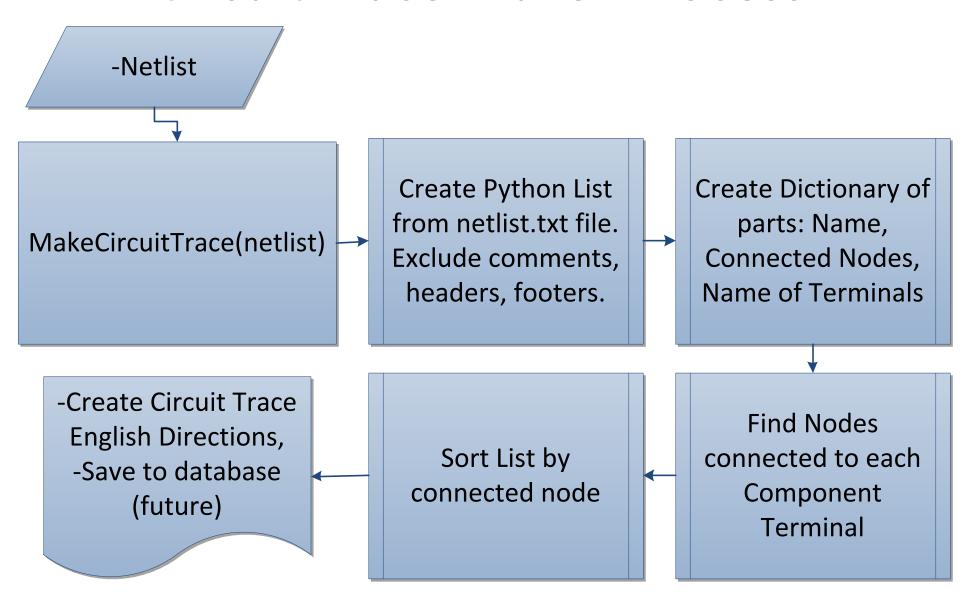
#### **Circuit Image Processing System Schematic**



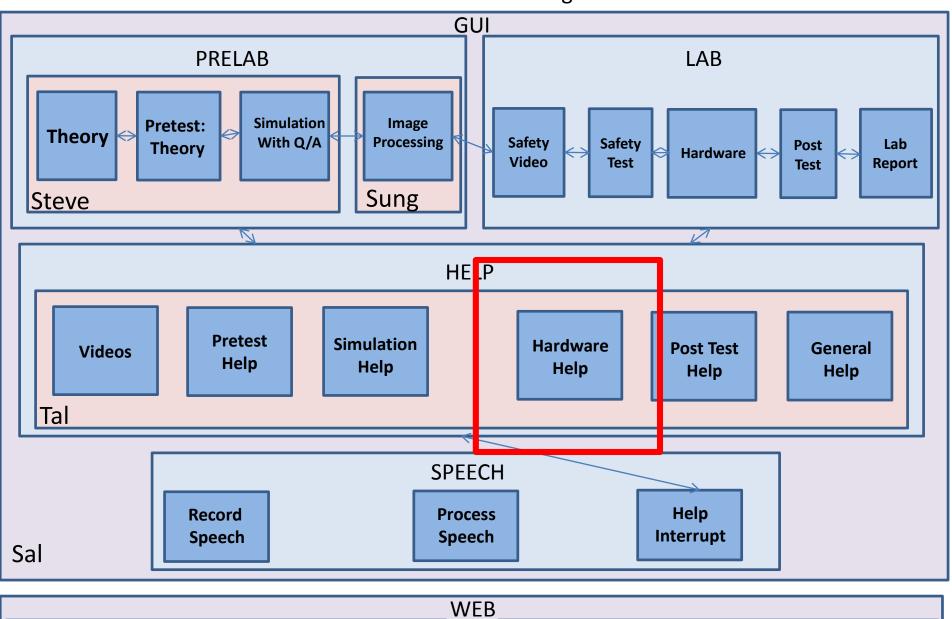
- 1. IN\_S: Input Simulated Circuit Image
- 2. IN\_P: Input Physically Assembled Circuit Image
- 3. DB\_TS: Database-Temporary Storage of Simulated Circuit Image
- 4. DB\_TP: Database-Temporary Storage of Physical Circuit Image
- 5. DB\_NS: Database-Prestored Netlist Data for Simulation
- 6. DB\_NP: Database-Prestored Netlist Data for Hardware Circuit
- 7. DB\_NR: Database-Netlist Result from Analysis

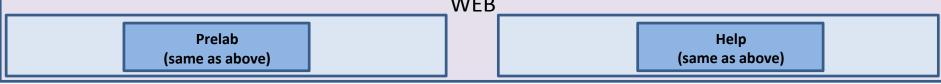


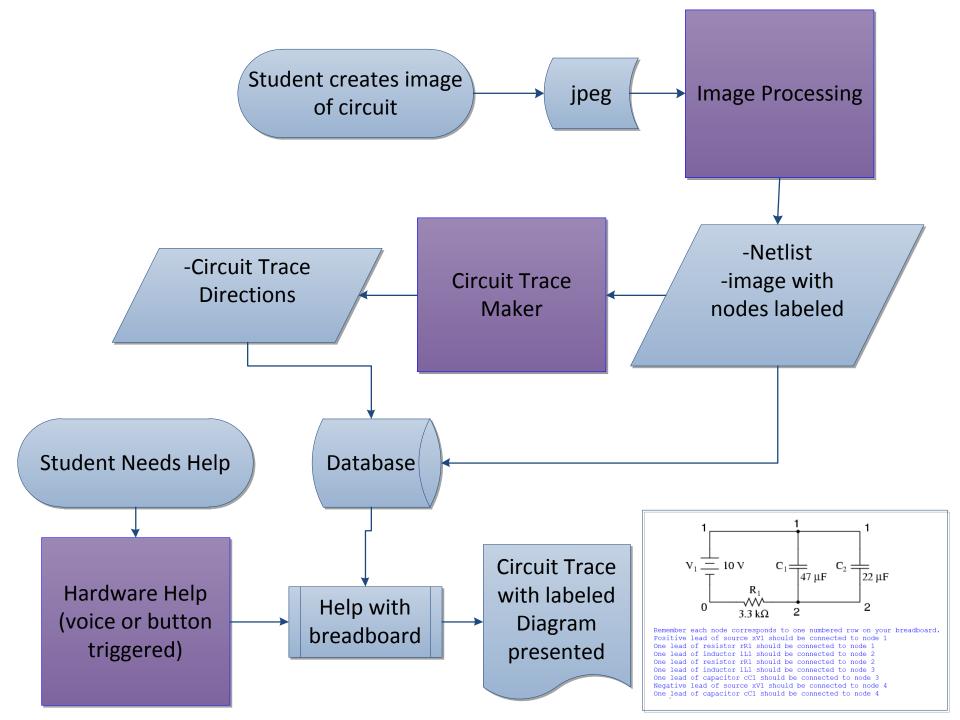
### Circuit Trace Maker Process



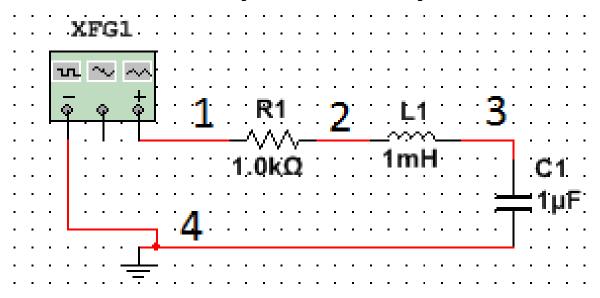
#### **Functional Block Diagram**





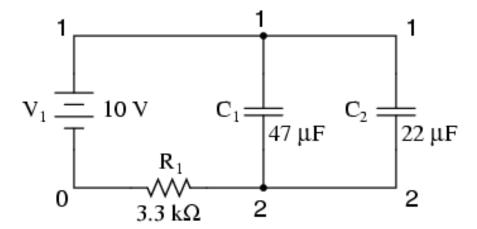


## Sample Output



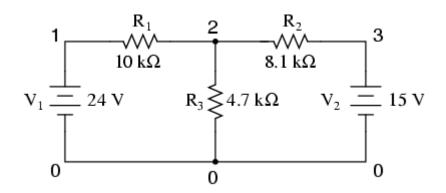
```
Remember each node corresponds to one numbered row on your breadboard. Positive lead of source xV1 should be connected to node 1 One lead of resistor rR1 should be connected to node 1 One lead of inductor lL1 should be connected to node 2 One lead of resistor rR1 should be connected to node 2 One lead of inductor lL1 should be connected to node 3 One lead of capacitor cC1 should be connected to node 3 Negative lead of source xV1 should be connected to node 4 One lead of capacitor cC1 should be connected to node 4
```

## Sample Output



```
Remember each node corresponds to one numbered row on your breadboard. Negative lead of voltage source v1 should be connected to node 0 One lead of resistor r1 should be connected to node 0 Positive lead of voltage source v1 should be connected to node 1 One lead of capacitor c1 should be connected to node 1 One lead of capacitor c2 should be connected to node 1 One lead of capacitor c1 should be connected to node 2 One lead of resistor r1 should be connected to node 2 One lead of capacitor c2 should be connected to node 2
```

# Sample Output



```
Remember each node corresponds to one numbered row on your breadboard. Negative lead of voltage source v1 should be connected to node 0 Negative lead of voltage source v2 should be connected to node 0 One lead of resistor r3 should be connected to node 0 Positive lead of voltage source v1 should be connected to node 1 One lead of resistor r1 should be connected to node 1 One lead of resistor r1 should be connected to node 2 One lead of resistor r2 should be connected to node 2 One lead of resistor r3 should be connected to node 2 Positive lead of voltage source v2 should be connected to node 3 One lead of resistor r2 should be connected to node 3
```